Toward the Next generation of Non Volatile Phase-Change Memory Targeting Ultra-Low Power Consumption

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Nouvelle génération de mémoire à changement de phase non volatile pour des applications à très basse consommation

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Contents

List of Symbols

Symbol	Measure Unit	Designation
$\vec{E}$	$[V\,m^{-1}]$	Electric field vector
E	$[V\,m^{-1}]$	Electric field intensity
h_a	$[m]$	Amorphous thickness
I_m	$[A]$	Melting current
I_0	$[A]$	AC current amplitude
I_{cell}	$[A]$	Current in the cell
I_R	$[A]$	RESET current
$\vec{J}$	$[A\,m^{-2}]$	Current density vector
J	$[A\,m^{-2}]$	Current density intensity
J_R	$[A\,m^{-2}]$	RESET current density
k_{th}	$[W\,m^{-1}\,K^{-1}]$	Thermal conductivity
$k_{th,eff}$	$[W\,m^{-1}\,K^{-1}]$	Effective thermal conductivity
P	$[W]$	Electrical power
P_l	$[W\,m]$	Power per length unit
q	$[W\,m^{-2}]$	Thermal flux
Q	$[W\,m^{-3}]$	Power density
R_0	$[\Omega]$	Line resistance
R	$[\Omega]$	Resistance value
R_i	$[\Omega]$	Interfacial resistance
R_{Load}	$[\Omega]$	Load resistance
R_{ON}	$[\Omega]$	Resistance of the cell in the ON-state
R_{RESET}	$[\Omega]$	RESET resistance of the device
R_{SET}	$[\Omega]$	SET resistance of the device
R_{th}	$[K\,W^{-1}]$	Thermal resistance
t_{ox}	$[m]$	Dielectric layer thickness
T_g	$[s]$	Glass temperature
T_m	$[K]$	Melting temperature
T_C	$[K]$	Crystallization temperature
v_g	$[m\,s^{-1}]$	Growth speed
V_0	$[V]$	AC voltage amplitude
V_ω	$[V]$	Amplitude of the voltage first harmonic
$V_{3\omega}$	$[V]$	Amplitude of the voltage third harmonic
V_{cell}	$[V]$	Voltage drop on the cell
V_H	$[V]$	Holding voltage
V_I	$[V]$	Initialization voltage
V_{pulse}	$[V]$	Voltage applied
V_{TH}	$[V]$	Threshold voltage
z_{melt}	$[m]$	Coordinate at which T = 930 K is reached in the phase-change layer
z_{heater}	$[m]$	Coordinate at which T = 930 K is reached in the heater

α	$[K^{-1}]$	Temperature coefficient of resistance
ΔT_0	$[K]$	Amplitude of temperature oscillations
ρ	$[\Omega\, m]$	Resistivity
σ	$[S\, m^{-1}]$	Electrical conductivity
σ_r	$[S\, m^{-1}]$	Electrical conductivity during READ
σ_{ON}	$[S\, m^{-1}]$	Electrical conductivity of the ON-state
ω	$[s^{-1}]$	Angular frequency

Glossary

Acronym	Designation
BEOL	Back End Of Line
BL	Bit Line
CVD	Chemical Vapor Deposition
CMOS	Complementary Metal Oxide Semiconductor
FEM	Finite Element Method
FDSOI	Fully Depleted Silicon on Insulator
EDX	Energy-Dispersive X-ray Spectroscopy
GST	$Ge_2Sb_2Te_5$
GGST	Ge-rich $Ge_2Sb_2Te_5$
HCP	High Current Population
HXPES	Hard X-ray PhotoEmission Spectroscopy
IV	Current vs Voltage curve
IGS-PCM	Inter Granular Switching Phase-Change Memory
IL-PCM	Interfacial Layer Phase-Change Memory
LCP	Low Current Population
MPTR	Modulated PhotoThermal Radiometry
NMOS	Negative Metal Oxide Semiconductor
PCM	Phase-Change Memory
PCL	Phase-Change Layer
PECVD	Plasma Enhanced Chemical Vapour Deposition
QLC	Quad-Level Cell
RI	Resistance vs Current curve
RT	Room Temperature
SNC PCM	Self-Nano Confined Phase-Change Memory
SEE	Single Event Effect
SET-opt	Optimized SET pulse
SET-FT	SET pulse with Fall Time
SLL	SuperLattice-Like
TBR	Thermal Boundary Resistance
TCR	Thermal Coefficient of Resistance
TDTR	Time Domain Thermo Reflectance
TID	Total Ionization Dose
TEM	Transmission Electron Microscopy
VBM	Valence Band Minimum
WL	Word Line
XRD	X-Ray Diffraction
XRR	X-Ray Reflectometry

Introduction

Context

During the last decades, the number of objects connected has drastically increased and more than hundreds of billions of devices are expected to be connected in 2050 (Fig. 1). In this scenario, storing a large amount of information in a small space represents a primary necessity, leading to a growing interest in the development of memory systems suitable for the new generation of electronic devices featuring high scaling.
Nowadays, all the electronic accessories have a memory system based on a von-Neumann architecture, with the computing and the storage units physically separated and organized according to a specific hierarchy. The top of the hierarchy is occupied by the working memory, which is used to perform the logic operations. This memory is represented by the Static or Dynamic Random Access Memory units (SRAM and DRAM, respectively) which are fast, expensive and volatile. While, the bottom of the hierarchy, is occupied by NAND Flash and NAND Solid State Drives as well as by Hard Disk Drives (HDD), which are slow, cheap and non-volatile, hence able to store the information even when the power is off, unlike the volatile ones. Therefore, storage memories are used to store the data not directly used, allowing an easier access to them when needed. The gap between the top and the bottom of the hierarchy consists in a three order of magnitude difference in terms of access time and one order of magnitude in cost (Fig. 2). Nevertheless, despite the difference in tasks and requirements fulfilled, they both rely their functionality on charge storage, making them not suitable to satisfy the scaling requirements demanded by the market. Indeed, different studies report an impact on data sensing and data retention when reducing the size of charge-based devices [1, 2]. Moreover, Flash memories present low radiation tolerance, ruling out the possibility to use them for aerospace applications.
The scaling limit in charge based technology can be solved either with sophisticated design solutions (as in the 3D NAND supported by Samsung, Micron and Toshiba) or with the use of microcontrollers and error correction codes. Nevertheless, these improvements could not provide a memory featuring high scalability along with low power consumption at reduced cost and ensuring radiation hardness. With this aim, innovative memory technologies were developed, namely the resistive non-volatile memories (NVM). These are two-terminal devices were the information storage relies on the change of the resistive state in an active material, sandwiched between two electrodes. The NVMs are able to combine the accessibility of DRAM with the non-volatility of Flash, filling the gap between working and storage memories (Fig. 2), and making them the ideal candidate for Storage Class Memory (SCM) applications.
The resistive non-volatile memories are classified according to their working principles.

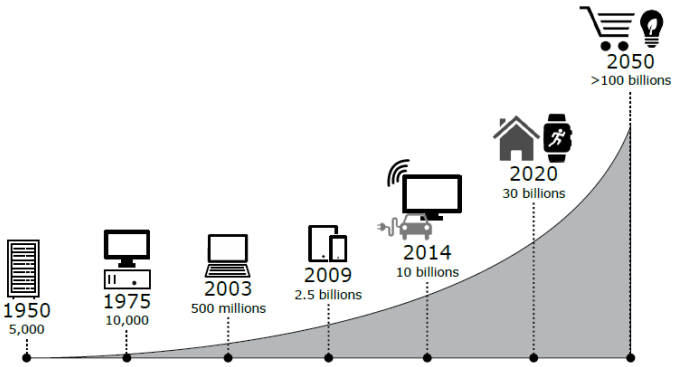

Fig. 1. Timeline of the number of connected objects. More than 100 billions objects are estimated to be connected in 2050 [3].

The most promising solutions include:

- Resistive Memories (RRAM) which are based on a reversible dielectric breakdown mechanism;
- Magnetic Memories (MRAM) which store the information in magnetic domains;
- Phase-Change Memories (PCM) where a chalcogenide material is used to store the bit by a reversible switching from the amorphous to the crystalline state.

These memory technologies can be implemented in both embedded and stand-alone applications. The comparison of the new generation NVMs performance with respect to the charge based stand-alone and embedded counterpart is reported in Fig. 3 and Fig. 4, where the best performance for each feature is represented by the higher value on the respective axis on the chart. Some of the parameters used in the comparison are:

- *write/read speed*, which refers to the time needed to save/have access to the information;

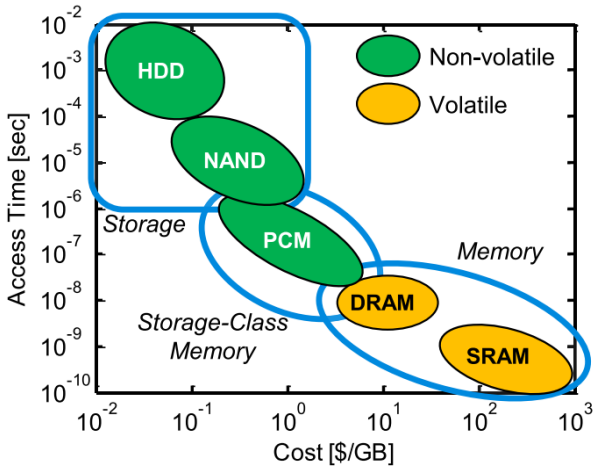

Fig. 2. Access time as a function of the cost for both volatile and non-volatile memories. Emerging NVMs, like PCM, can fill the performance gap [4].

- *write energy*, which accounts for the energy needed to save an information;
- *endurance*, which refers to the number of program/erase operations before facing the device degradation.

In terms of stand-alone applications, PCM ensures lower costs and higher density compared to RRAM and MRAM competitors. More precisely, PCM became the leading technology after the commercialization of the 3DXPoint by Intel in 2017. This state-of-the-art PCM technology is characterized, in fact, by a latency one thousand times higher than NAND flash and by a density ten times higher than DRAM. Moreover, its non-volatility guarantees a reduction in the amount of DRAM needed to maintain a high bandwidth (i.e., rate at which the processor read/store the data in the memory), hence reducing the cost and the power used by the whole system [5]. This has been witnessed in 2019 when the Intel Optane memory H10 with SSD came into commercialization. It co-integrates a 3DXPoint with a Quad-Level Cell (QLC) 3DNAND (i.e.,4 bit per cell) ensuring high performance at low latency and cost. Further improvements on the Optane memory are ongoing in order to achieve a higher density and storage performance. In particular, IBM is developing a three-bit per cell PCM chip; while a second generation of Optane (expected for the end of 2020) will be based on a four layer stack used to replace the two layered version already on the market.
In terms of embedded applications, the emerging NVM have still limited market. As described in Fig. 4, among the new generation of NVM, MRAM owns the best features with high endurance and low writing energy. However, the cost and the reliability at high temperature are also two crucial factors to take into account for industrialization, positioning PCM as the main MRAM competitor. Indeed, the better thermal stability achieved in PCM by the chalcogenide material engineering [6] brought to the development of a PCM device based on a 28 nm FDSOI by STMicroelectronics, which is supposed to get in the market at the beginning of next year. Therefore, PCM represents the undeniable breakthrough in the present storage scenario featuring properties of both DRAM and Flash, presenting an advanced state in terms of development and industrialization in SCM [7] as well as in embedded PCM-based microcontrollers for

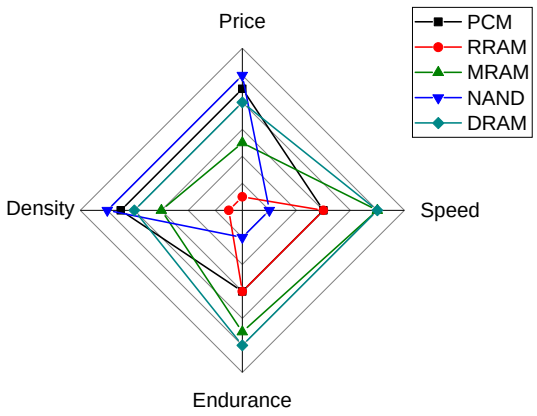

Fig. 3. Performance comparison of different NVM technologies with respect to NAND and DRAM for stand-alone applications.

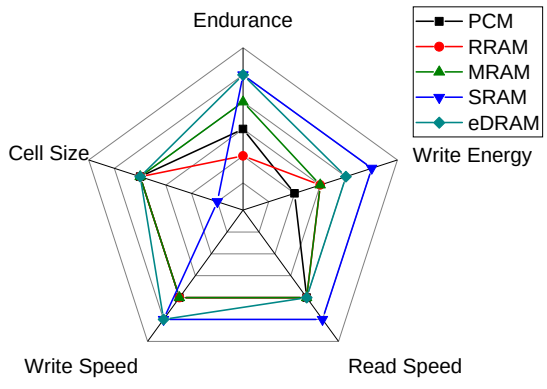

Fig. 4. Performance comparison of different NVM technologies with respect to SRAM and eDRAM for embedded applications.

automotive applications [8]. Furthermore, since the discovery of phase-change materials and PCM, a high radiation tolerance was foreseen [9] expanding the fields of application for this technology.

Objectives of this work

Since all the electronic based systems need a power supply to assure their functionality, the development of low power devices is the main target of the modern technology. This represents a big challenge for PCM since this technology is characterized by the higher writing energy among the emerging NVM (see Fig. 4). Indeed, the lowest programming current demonstrated in PCM is of 30 μA on 256 Mb [10], to be compared with less than 10 μA achieved at array level in both RRAM [11] and MRAM [12].
In this scenario, the objective of this thesis is to contribute to the development of the next generation Non-Volatile PCM targeting ultra-low power consumption. Since PCMs rely on Joule Heating, the thermal optimization of the device represents a key point for investigation. In this work, the thermal optimization of the cell is carried out by the interplay of three different aspects:

- The thermal conductivity characterization of both dielectric and conductive materials that i) are currently integrated, ii) present interesting properties and are potential candidates for integration in next generation PCM devices;

- 3D electro-thermal simulations of PCM devices, allowing to describe the temperature profile in the memory cell and to further investigate the main parameters to be tuned in order to improve the thermal performances of the cell;

- The electrical characterization of PCM devices (e.g., programming current, speed, endurance) to define the performance of different state-of-the-art PCM configurations and their ability to reach low-power operations.

In Chapter 1, the basic working principle of Phase-Change Memories will be introduced. Then an overview of the approaches proposed to reduce the programming current in PCM will be described in Chapter 2.
Chapter 3 will focus on the measurement of material thermal conductivity. At first, theoretical models will be presented. Then, the setup of a 3ω method and its optimization will be described. Furthermore, the validation of the measurements on a set of materials will be reported, comparing the resulting thermal conductivity values to those obtained by another method (Modulated Photothermal Radiometry) at the Institut de Mecanique et d' Ingenierie (I2M) de Bordeaux and at the Laboratoire National de Metrologie et d'essais (LNE) in Paris.
The measured thermal conductivity values were exploited in a numerical model, based on finite-element simulations. A parametric study on the Wall-based PCM will be presented in Chapter 4. In particular, the electro-thermal response of the PCM device subjected to an external voltage pulse will be described, and the influence of the material and geometrical properties will be investigated to identify the optimal conditions for low-power PCM applications.
Chapter 5 reports the results obtained via the electric tests performed on different

low power solutions. The results will involve a discussion on the PCM performances by coupling the electric test with the device electro-thermal simulations and physico-chemical analysis performed on the programmed devices. We will mainly focus on i) the importance to tune the encapsulation layer thermal conductivity in Wall based PCM; ii) the 50 μA and size-independent RESET current achieved thanks to an interfacial GeN layer on 4kb matrice and its potentiality to be further scaled; iii) the possibility of alternative current reduction solutions for PCM low power performance and iv) the impact of material and architecture engineering on PCM radiation hardness. Finally, potential future directions of investigation will be provided.

Chapter 1

Phase-Change Memory

The Phase Change Memory functionality relies on the reversible switching from a high resistive state to a low resistive state of the phase-change material deposited between the two electrodes. Therefore, PCM performance depends on the phase-change material properties.
In this chapter, the main features of phase-change materials are introduced, dealing with an analysis on the crystalline structure and of the nature of the crystallization mechanism taking place during the amorphous-to-crystalline transition. The difference in the conduction mechanism between the two phases is also addressed.
We than move our focus on the Phase-Change Memory device and first introduce the strategy to write/erase an information in a device. The electro-thermal model driving the device functionality is then introduced to trigger possible path for PCM optimization.

1.1 Phase-change materials and phase-change mechanism

During the 1960s, Ovshinsky first presented the existence of a switching mechanism when a phase-change material is subjected to an external voltage [15]. This mechanism causes the transition from a high resistive state (amorphous phase) to a low resistive state (crystalline phase), introducing the concept of information storage in the two phases of the material. The transition between the amorphous and the crystalline phase is evidenced by a characteristic resistance vs temperature curve (Fig. 1.1): as soon as the crystallization temperature (T_c) is reached, the material electrical resistivity suddenly drops. In this section, we will present at first the phase-change materials chemical composition. After that, we will focus on their crystalline structures and on the principle underling the atomic rearrangement, which enables the crystalline-to-amorphous and amorphous-to-crystalline phase transitions.

1.1.1 Crystalline structure and phase transition

Phase-change materials belong to the family of chalcogenides, which are compounds of chalcogens (e.g. sulphur, selenium or tellurium) with electropositive elements or organic radicals. The most used phase change materials are ternary chalcogenides based on a Ge-Sb-Te alloy. The ternary diagram of a Ge-Sb-Te system is shown in Fig. 1.2 where each of the three apexes represents one of the elements composing the alloy. Each point of the diagram is referred to a specific Ge-Sb-Te composition, defined by the correspondent atomic percentage value reported along the three axis. Modifying the material composition, it is possible to tune its properties and, consequently, the performance of the device in which it will be integrated. From the application point

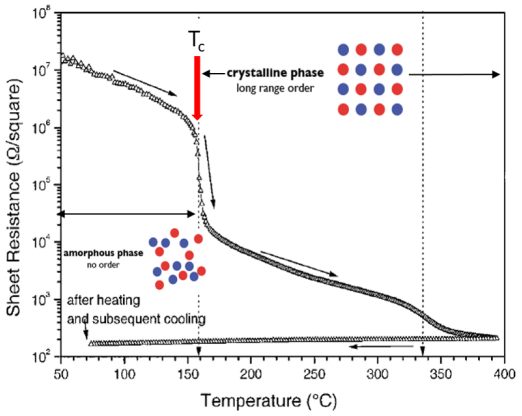

Fig. 1.1. Characteristic resistance vs temperature curve for a phase-change material. When the crystallization temperature (T_c) is overcome, the material reorganizes in a crystalline phase, resulting in a drop of the electrical resistance [13].

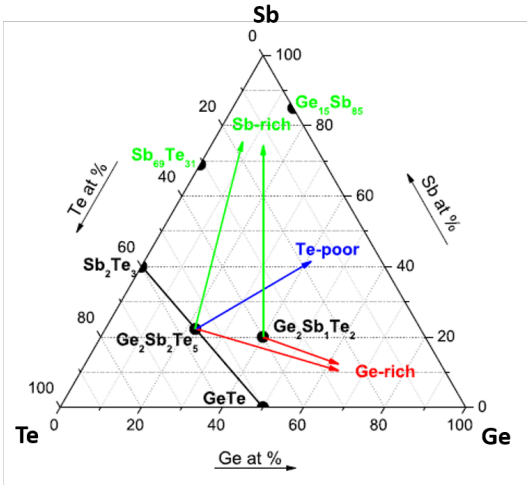

Fig. 1.2. Ternary Ge-Sb-Te phase diagram [14].

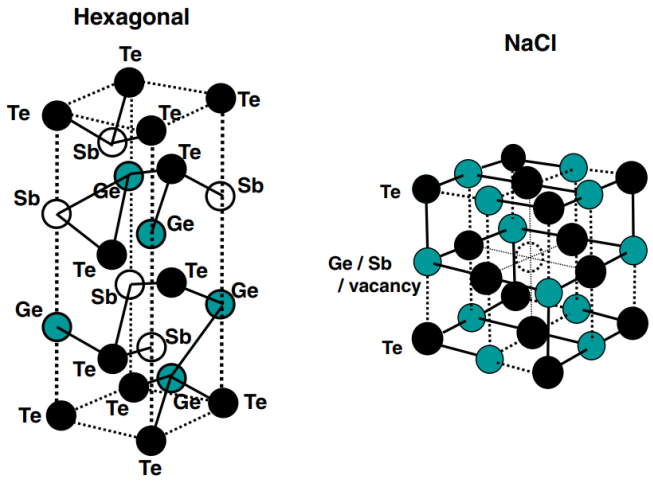

Fig. 1.3. Representation of the hexagonal crystal structure and the metastable NaCl structure [17].

of view, compounds characterized by high crystallization temperature and speed are desired [16]. Materials belonging to the GeTe-Sb_2Te_3 pseudobinary system (indicated by the black line in Fig. 1.2) present this features. In particular, the most used chalcogenides for non-volatile memories applications are GeTe and $Ge_2Sb_2Te_5$ (GST).
The crystalline structure of phase-change materials can be either hexagonal (hcp) or face-centered cubic (fcc). As an example, the schematic representation of these two structures is reported in Fig. 1.3 for GST. The GST hexagonal structure is made up of three unit cells, characterized by a rhombic top and bottom plane with vertex angles of 60° and 120°. The major covalent bonds in the unit cell are arranged in even-numbered rings and are represented in the schematic as black lines connecting the atoms. The non uniform arrangement of the atoms requires a long heating time to allow the material to rearrange its atoms in the hexagonal configuration. On the contrary, by heating up the material in a small time range (i.e., nanoseconds to microseconds), the most probable crystalline arrangement is the metastable NaCl-like structure [17] (Fig. 1.3). When $Ge_2Sb_2Te_5$ is in this metastable NaCl-like structure, the Te atoms take the place of Cl sites while Ge and Sb randomly occupy the Na sites with 20% of vacancies. In the unit cell of the metastable NaCl-like structure, the vacancy site is highlighted by the dashed circle situated at the center of the cubic cell. Therefore, when the GST undergoes the phase transition, it organizes at first into a face centered cubic (fcc) structure, then into the hexagonal one. A description of the atomic rearrangement taking place during the phase transformation is reported in Fig. 1.4. The transition from the crystalline to the amorphous phase occurs only if the material is melted via Joule heating and then rapidly quenched back to room temperature. On the contrary, to recover the crystalline state, the material faces the threshold switching phenomenon. At this point, the Joule heating generated in the material allows the crystallization if the temperature achieved in the system favors the atomic reorganization.
The optimal condition to get the amorphous to crystalline phase-change depends on the material composition, hence on the type of crystallization mechanism driving the resistive transition, as will be described in more details in the next section.

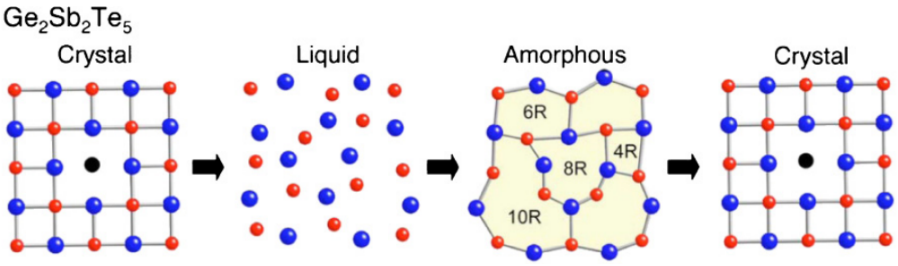

Fig. 1.4. Description of the phase-change transition. At first, crystallne material has to undergo a melting process. Setting a sufficiently high cooling rate, the amorphous phase is then obtained. On the contrary, the crystalline state can be achieved exclusively with a specific temperature profile which favor the atomic reorganization [17].

1.1.2 Crystallization mechanism

The crystallization mechanism in chalcogenide materials follows the classical nucleation theory developed by Gibbs [18] and is based on the thermodynamic description of a system made up of a crystalline cluster evolving in an amorphous matrix. At the beginning of the crystallization mechanism the created clusters are small and unstable (i.e., crystal nucleation) until some of them are able to increase their radius above a critical dimension at which they become stable nuclei and can grow to macroscopic crystals (i.e., crystal growth). The time needed to reach the critical size is called transient or incubation period. Therefore, a long transient period inhibits the material crystallization.
Dependending on the mechanism dominating the phase transition, chalcogenides are classified in nucleation dominated or growth dominated materials. In nucleation-dominated materials, the crystalline state is achieved when the nucleation rate (number of critical nuclei formed per unit time in a unit volume of the material) is high enough to fill the entire volume, leading to an increase of the material conductivity. The nucleation is defined as homogeneous when the probability of nucleus formation is constant in the entire volume under investigation; while it is defined as heterogeneous when the presence of interfaces, boundaries or defects can favor the nucleation in these regions. Therefore, melt-quenching or thermal pre-treatment could modify the crystallization speed [5, 19].
In growth-dominated materials, both nucleation and growth occur but the nucleation rate is small enough to do not significantly contribute to the crystallization mechanism. Growth is associated to the possibility of the atoms to reorganize at the interface between the amorphous and the crystalline region. The amorphous to crystalline transition takes place only if each atom is able to overcome a certain energy barrier, resulting in a reduction of the overall energy of the system. The growth speed (v_g) can be determined by considering a combination of the probability of the atom to remain in its amorphous state and the probability for it to undergo the phase transformation. The two crystallization mechanisms has been studied in phase-change materials. Particularly, Lee et al. [19] exploit the difference in reflectance between the crystalline and amorphous phase to monitor the crystallization process by pump-probe laser measurements and Atomic Force Microscopy (AFM). In this study, two materials were investigated and compared: GST and AgInSbTe (AIST). As shown in Fig. 1.5 a, the

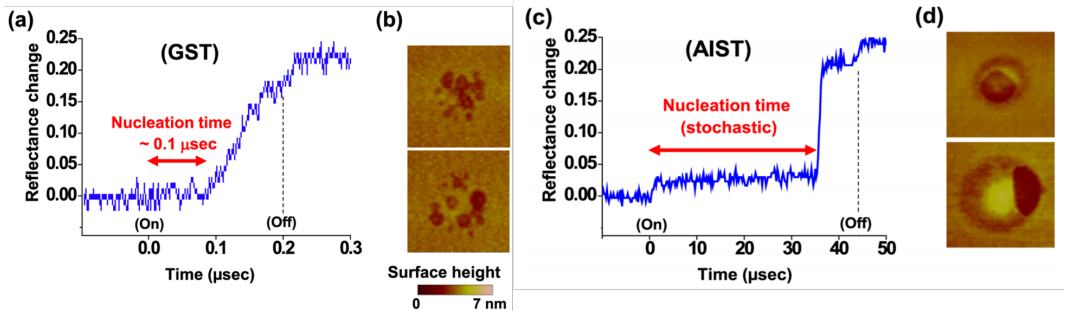

Fig. 1.5. a) Reflectance change of GST obtained with a laser spot diameter of around 1 µm. A reflectance change is observed after 0.1 µs, b) Atomic Force Microscopy (AFM) analysis of the GST sample after laser exposure, shows the multiple supercritical nuclei growing individually. c) Reflectance change of AIST obtained with a laser beam diameter of 2 µm. In AIST, the nucleation time is stochastic and longer than GST (tens of µs). d) AFM measurements on AIST highlights thegrowth phenomenon from a single supercritical nucleus [19].

GST reflectance remains constant during a nucleation time of 0.1 µs. After that, it increases monotonically, indicating the formation of multiple super-critical nuclei which grow up separately as can be observed in Fig. 1.5 b. The area is not completely filled with nuclei since the crystallization has been interrupted by turning off the pump-laser before the full crystallization of the layer. For AIST, instead, the nucleation time is ten times higher than in GST. During this time, the material try to generate some nucleus in a stochastic way before facing a rapid crystallization, as witnessed by the abrupt change in reflectance reported in Fig. 1.5 c. The AFM analysis on the sample is reported in Fig. 1.5 d where the growth from a single supercrytical nucleus is evidenced.

1.1.3 Conduction mechanism in amorphous and crystalline phase

In 1976 the discovery of localized states in the energy gap of amorphous chalcogenide materials [22] paved the way for the study of the conduction mechanism in both the amorphous and crystalline state by the quantum semiconductor theory. Furthermore, the investigation of both the optical and electrical properties of phase-change materials gave the possibility to predict the band structure of the two phases. The absorption coefficient of GST as a function of the photon excitation energy is reported in Fig. 1.6. The steep reduction of the absorption coefficient at lower energy is an evidence of the band edge. In particular, the optical gap evaluated for the amorphous phase has been associated to the presence of Urbach tails, decaying exponentially due to the presence of localized states generated by the disorder in the amorphous matrix, as stated by the Anderson theory [20]. The position of the Fermi level has been, instead, investigated by Hard x-ray photoemission spectroscopy (HXPES) which allows to detect the density of state in the valence band with respect to the Fermi level. The HXPES spectra of the amorphous and crystalline phase as a function of the energy are reported in Fig. 1.7 for both GST and GeTe. The energy zero along the x-axis coincides with the Fermi level. The valence band minimum (VBM) is closer to the Fermi level in the crystalline phase with respect to the amorphous for both the materials. This is in accordance with the higher electrical conductivity typical of the crystalline state. The deep valence band in

crystalline GST indicates the possibility to have an almost metallic conduction (i.e., degenerate semiconductor). On the other end, the amorphous phase presents a bandgap of 0.8 eV (i.e., a VBM at 0.4 eV), as an evidence of its intrinsic semiconductor nature characterized by a Fermi level pinned at midgap. Further studies evaluated the hole concentration in crystalline GST by the measure of the Hall coefficient [20] [23], demonstarting an acceptor-like band in accordance with the 20% of vacancies typical of the fcc GST.
The density of state and band schematic argued from the previous studies is reported in Fig. 1.8 along with the current vs voltage curve associated to both phases of the material. The crystalline phase is represented as a degenerate semiconductor since the Fermi energy lies between a defect band and the maximum of the valence band with low density of free carriers even at low temperature (10^{19}-10^{20} cm^{-3} at T = 5 K [20]) highlighting the tiny energy difference between valence and defects band. Hence, as soon as the temperature is increased, the amount of carriers involved in conduction increases drastically giving rise to a metallic conduction mechanism. This behavior is reported in the IV curve, where a typical Ohmic (V = RI) trend is evidenced for a crystalline material. In the amorphous phase, instead, the material can be considered as an intrinsic semiconductor with the Fermi level in the middle of the gap. This is mainly due to the presence of band tails in the valence band caused by lone-pairs or other defects, such as dangling or distorted bonds (e.g. Ge-Ge bonds in GST), which generate localized states in the material. Therefore, the conduction mechanism of an amorphous material is completely different from the crystalline one. This is evidenced in the experimental IV curve where the amorphous characteristic is firstly non-linear.

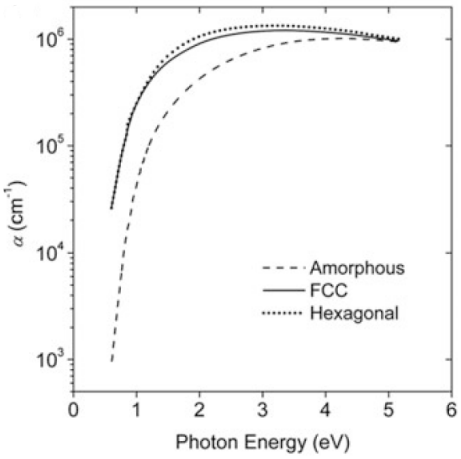

Fig. 1.6. Measured absorption coefficient α as a function of photon energy for amorphous and crystalline GST [20]. The presence of a band edge is evidenced by the steep reduction of the absorption coefficient at low energy.

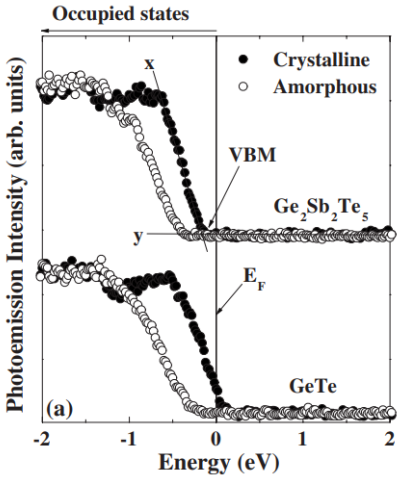

Fig. 1.7. HXPES spectra for GST (top) and GeTe (bottom) in the amorphous and crystalline phases [21], highlighting that the Valence Band Minimum (VBM) is closer to the Fermi level (Energy = 0 eV) for crystalline phase with respect to the amorphous

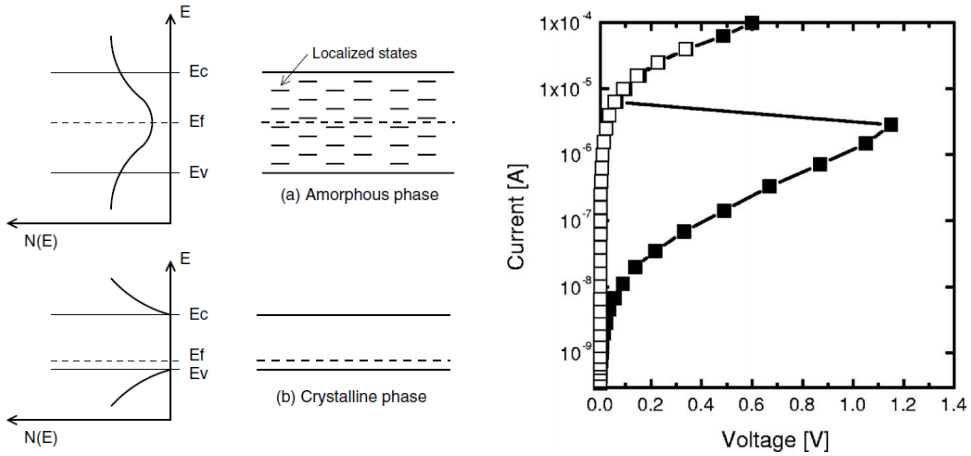

Fig. 1.8. (left) Density of state and band schematic for a chalcogenide material in a) amorphous phase and b) crystalline phase [23]. (right) Current vs voltage characteristic associated to both the crystalline (empty squares) and the amorphous (filled squares). The IV obtained for a RESET state presents a snap back, hence a threshold voltage at 1.2 V [26].

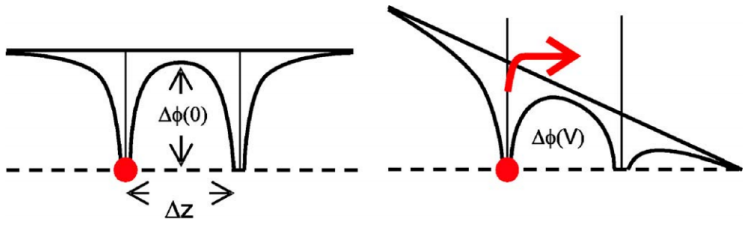

Fig. 1.9. Representation of the trap-limited conduction mechanism. The traps states modeled as potential wells with height $\Delta\phi(V)$ and distance Δz are reported (left) at zero applied voltage (V = 0) and (right) under an external voltage. The latter induces a barrier lowering and a consequent increase of the hopping probability to a neighbor cell when a small thermal excitation is induced in the system [23].

Indeed, the current increases following an exponential law until the onset of the threshold switching phenomenon, where the curve evidences a snap-back. After that, the two curves get superimposed (i.e., ON-state) as an effect of the phase transition. The conduction mechanism associated to the non-ohmic region before the threshold switching (i.e., OFF-state) can be ascribed to different phenomena [24]. Nevertheless, the one that is most commonly attributed to a high trap density material is the Poole-Frenkel mechanism. This is based on the electronic hopping generated by the thermal excitation between two trap states, usually modeled as a potential well with a height $\Delta\phi$ and distance Δz (Fig. 1.9). When an external voltage is applied to the system, the hopping probability increases exponentially giving rise to a current [25]:

$$I = I_0 e^{\beta V} \tag{1.1}$$

where β and I_0 are constants depending on the trap distance and barrier height. When a potential is applied to a system with high density of traps (small Δz), the barrier height reduces to $\Delta\phi(V)$ in accordance with the following relation:

$$\Delta\phi(V) = \Delta\phi(0) - qF\frac{\Delta z}{2} = -qV\frac{\Delta z}{2u_a} \tag{1.2}$$

with $\Delta\phi(0)$ being the energy barrier when no external voltage is applied to the system (Fig. 1.9), q the elementary charge, F the electric field and u_a the amorphous chalcogenide thickness.

1.1.4 Threshold switching

The IV curve of an amorphous chalcogenide (Fig. 1.8), described in the previous section, shows an instantaneous change in the material conductivity at a specific voltage (V_{th}). It represents the onset of the threshold switching phenomenon, which leads to have two different currents values associated to the same applied voltage. These two values are referred to the OFF and ON-state of the material.
The threshold voltage V_{th}, represents the transition between these two states. The origin of the threshold switching mechanism was longly debated in the years. Recently, Ielimini et al. [26] described the threshold switching as based on the non-equilibrium distribution generated by a relatively high electric field applied to the system. In particular, in this conditions, the electrons can access traps states at higher energies due to tunneling or thermal emission or energy gained by the external field. In general, the relaxation process counterbalances the gain in kinetic energy keeping the system in the equilibrium state. Nevertheless, in a system with trapped electrons, the relaxation process can involve phonon emission and impurity ionization (i.e., a high-energy carrier can transfer part of its energy to a carrier trapped at a deep level). Hence, the kinetic energy is shared among more exited electrons, leading to a non-equilibrium distribution of carriers. This scenario is reported in Fig. 1.10, where $u_{a,OFF}$ is the region where the Fermi level represents the highest occupied trap state at equilibrium. This is

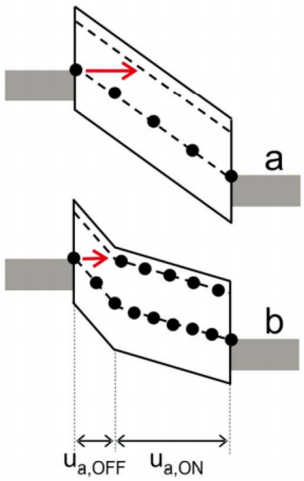

Fig. 1.10. Potential profile and electrons energy distribution in an amorphous chalcogenide material a) below and b) above threshold switching. At low current, the system is in equilibrium (OFF), while at high current a non-equilibrium condition takes place in a part of the layer characterized by an increase in the conductivity ($u_{a,ON}$) [26].

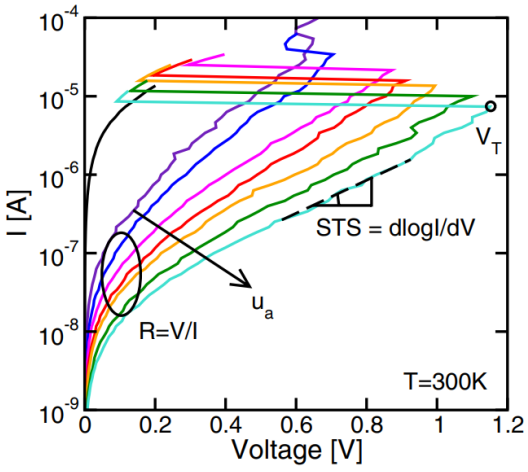

Fig. 1.11. Current vs voltage characteristic measured for devices characterized by an amorphous volume of different thickness (u_a). The thickness and resistance increase induces a decrease of the subthreshold slope (STS), leading to an increase of the threshold voltage [27].

considered as an OFF layer since the population is still controlled by the equilibrium statistic (i.e., no conduction switching is possible). Along the thickness $u_{a,ON}$, instead, the non-equilibrium distribution results in a high conductive regime. Therefore, the two regions are characterized by different electric fields even if the same current is flowing into them. This gives rise to the voltage drop in Fig. 1.8. In particular, the applied voltage is splitted in the two regions as:

$$\phi = F_{OFF}u_{a,OFF} + F_{a,ON}u_{a,ON} \tag{1.3}$$

with F_{OFF} and F_{ON} respectively the electric field in the OFF and ON layers. Furthermore, $u_{a,OFF}$ is independent from the amorphous layer thickness since it obeys the following relation:

$$u_{a,OFF} = \frac{E_{T2} - E_{T1}}{qF_{OFF}} \tag{1.4}$$

where E_{T2} is the energy of the deep trap aligned with the Fermi level and E_{T2} is a shallow trap close to the conduction band edge. Therefore, an increase in the overall amorphous thickness will not impact $u_{a,OFF}$. It will cause, instead, the increase in $u_{a,ON}$ and the decrease in the voltage across it. As a consequence, the gap between F_{OFF} and F_{ON} will be enhanced, resulting in a higher V_{th}. The IV curves associated to devices having different amorphous thicknesses are reported in Fig. 1.11. This highlights the threshold voltage increase with the amorphous thickness as well as it evidences the increase of the resistance and the decrease of the ratio between the current and the voltage variation (i.e., dlogI/dV), defined as the sub-threshold slope (STS). The correlation between the V_{th} and the amorphous thickness represents a parameter of valuable interest especially when the chalcogenide material is integrated in a device, as it will be presented later in this work.

1.2 Phase-change memories

Phase-Change Memories (PCM) are two terminal devices where a phase-change material layer is sandwiched between two electrodes and the difference in resistivity between the two phases is used to store the information. In general, the amorphous phase is associated to the logic state 0 (RESET) while the crystalline phase corresponds to the logic state 1 (SET). The information is stored with a write operation that induces a resistance switch in the material through the application of an external voltage pulse. The SET and RESET write operations are schematized in Fig. 1.12. The amorphization is ensured by a voltage pulse high enough to induce the melting of the phase-change material inside the device (T > T_{melt}, where T_{melt} is generally around 650 °C) and with sharp pulse edges to maintain the disordered atom arrangement, achieved during melting, even when the material is cooled down back to room temperature. Indeed, during the fast quenching the atoms mobility is small enough to prevent the atomic rearrangement. To switch the material from the amorphous to the crystalline phase, instead, the voltage pulse should be able to keep the temperature in the fast crystallization regime long enough to ensure the re-crystallization of the whole amorphous region. Therefore, the crystallization process is characterized by a longer pulse edge (i.e., fall time) with respect to the amorphisation. Hence, the temperature profile control inside

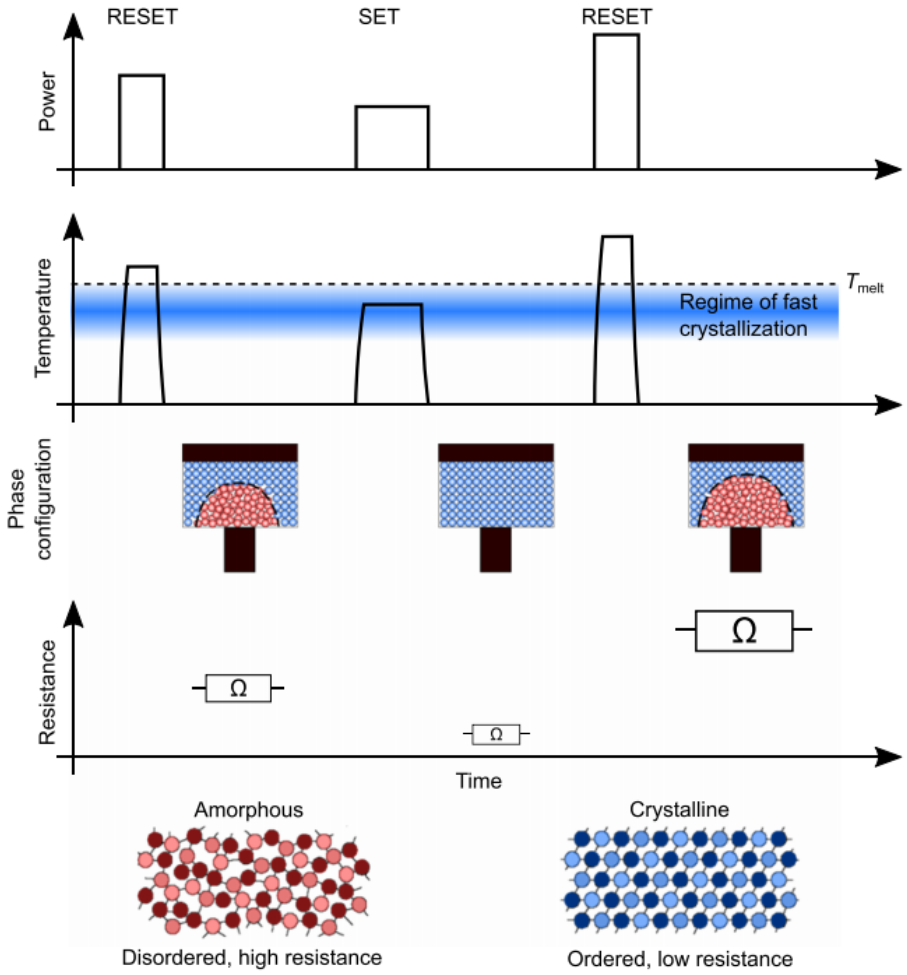

Fig. 1.12. Representation of the writing principle of a PCM cell, with a comparison of the power, temperature profile, phase configuration and resistance during the SET and RESET programming conditions. The RESET pulse heats the material above the melting temperature and it leads the memory in an high resistive state (amorphous phase) when rapidly quenched back to room temperature. By tuning the power used during the programming pulse, the final RESET resistance can be modulated. The SET pulse, instead, heats the material up to the crystallization temperature and cool the system down with a specific speed which enable the atomic reorganization to a low resistive state [28].

the cell is fundamental to achieve an accurate storage of the information. To be noted that during the writing operation the voltage pulse need to have an amplitude higher than the threshold voltage ($V > V_{th}$).
The programmed state can then be read through a read operation. This step retrieves the information stored in the cell (i.e., amorphous or crystalline state). The read operation consists in the application of a voltage pulse low enough to do not modify the memory state: the voltage amplitude should be smaller than V_{th}. Nevertheless, even if a $V < V_{th}$ is used, the information retrieved by a read operation can assume different values dependently on the time and temperature at which the measurement is performed. This effect mainly occurs in material being in the amorphous phase. Indeed, when the material is in this phase, it can face a structural relaxation, which macroscopically leads to the resistance drift towards higher values, due to the thermally

activated nature of the electric transport, typical of the materials in these phase. At room temperature, the resistance (R) evolution in time (t) is described by a power low as follows:

$$R = R_0\left(\frac{t}{t_0}\right)^{\nu} \tag{1.5}$$

were R_0 represents the resistance at t = 0 (t_0) and ν is the drift coefficient, which is material dependent.
Moreover, the pulse used to SET the memory cell is not always capable to completely crystallize the material. Therefore, most of the time, the SET state is referred to a poly-crystalline state of the material. In this condition, the structural relaxation can occur at the grain boundaries between crystalline grains [29]. Furthermore, it has been demonstrated that the drift coefficient is temperature dependent. It increases linearly with temperature [30] until nucleation and growth take place, leading the resistance to decrease back to the starting value [29]. To be noted that, unlike the RESET state, the SET drift could cause the resistance window to reduce, hindering the programming of the cell.

1.2.1 Electro-thermal analysis

The PCM working principle is based on the coupling between i) an *electric* contribution, due to the voltage applied and the current flowing in the device and ii) a *thermal* contribution, associated with the temperature rise in the system due to the Joule heating.

1.2.1.1 Device functionality

The typical IV and RI (resistance vs current) characteristics of a PCM cell are reported in Fig. 1.13 and Fig. 1.14, respectively. The curves are reported for both a PCM device initially in the crystalline phase (empty markers) and amorphous phase (filled markers). When the material is crystalline, the IV curve follows a ohmic behavior for low applied voltages. Increasing the voltage, the material is heated up by Joule

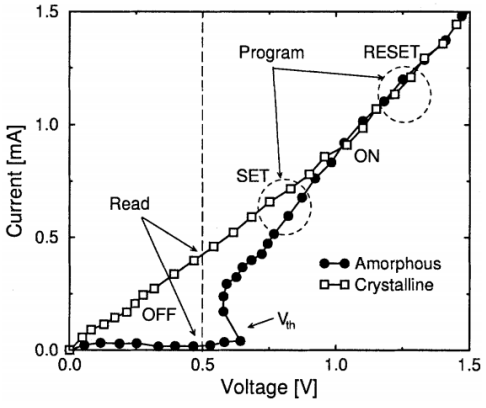

Fig. 1.13. Current as a function of voltage for a PCM device in SET state (empty squares) and RESET state (filled black dots) [31].

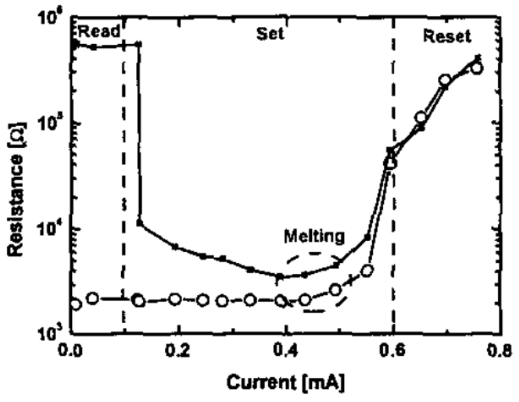

Fig. 1.14. Resistance as a function of current for a PCM device in SET state (empty cyrcle) and RESET state (filled black squares) [32].

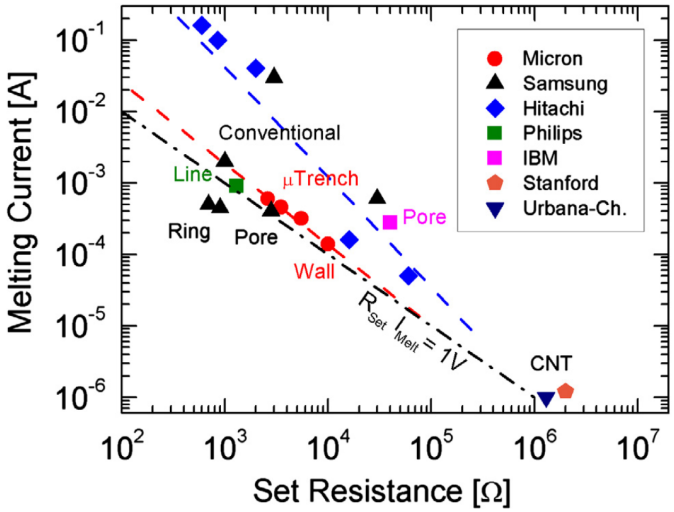

Fig. 1.15. Melting current as a function of the SET resistance compared for different architectures presented in literature, showing a linear correlation between the two parameters. [33]

heating. As a consequence, its atomic arrangement get drastically modified when the melting temperature is reached. This induces the onset of the ON-state, evidenced by a change of slope in the IV curve. The PCM resistance at this stage is called ON resistance (R_{ON}). In general, it represents the bottom electrode resistance since the melted phase-change layer contributes marginally to R_{ON}. After melting, the material can reach the amorphous phase through a rapid quenching. It is important to notice that in a PCM device, the abrupt cooling will not always result in a resistance increase: if the interface between the chalcogenide and the bottom electrode is not completely covered by the melted region, the residual crystalline zones play the role of conductive paths, thus contributing the most to the final resistance value (i.e., in the equivalent electric circuit, the conductive paths are modeled by a resistance in parallel to the melted region one).
On the contrary, when the initial state of the material is amorphous, the IV characteristic follows the non-ohmic behavior according to Eq. 1.1, until the onset of the threshold switching (V_{th}). This will result in an abrupt reduction of the resistance, as reported in Fig. 1.14. At this point, the material reaches the ON-state, where the device can partially SET, if the active material achieves a temperature in the range of favorable crystallization. At this stage of the programming operation, the crystalline order achieved depends on the shape of the pulse used to program the cell. Therefore, the measured resistance could be higher than the SET value, as it is shown, for example, in the SET region of Fig. 1.14. Independently from the initial state, when the full region above the bottom electrode is melted, the material can be either programmed in RESET or in SET, depending on the shape of the applied pulse: a short fall time will RESET the device (as in Fig. 1.14) while a long fall time will SET it.
The PCM can be described by looking at two parameters controlling its functionality:

- the melting current (I_m), which is directly related to the device power consumption

- the SET resistance (R_{SET}), which refers to the material conductance in the crys-

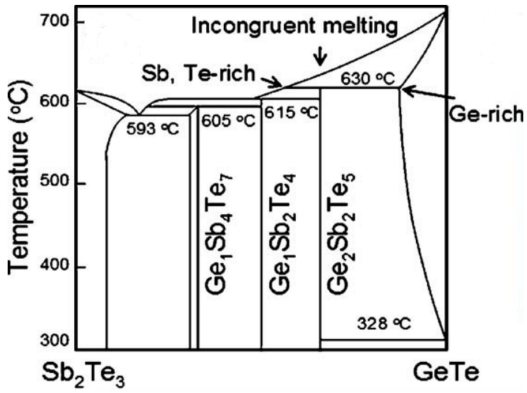

Fig. 1.16. Phase diagram along the tie-line Sb_2Te_3-GeTe [34]

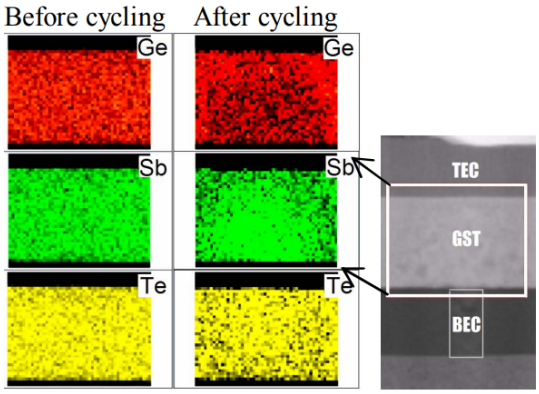

Fig. 1.17. Comparison of Energy Dispersive X-ray spectroscopy (EDX) performed before and after cycling. The analysis shows that after cycling the Sb atoms are pulled down to the bottom electrode/GST interface and the Ge is placed in the surrounded area [35]

talline state. This resistance is also associated with the contact area between the chalcogenide material and the bottom electrode when devices with the same active layer are compared.

The relation between I_m and the SET resistance for different PCM cell architectures is reported in Fig. 1.15 [33]. The trend evidences that the higher is the SET resistance, the lower is the current needed to melt the material. Therefore, device scaling is a suitable solution to reduce the melting current in PCM. As a matter of fact, shrinking all the device dimensions by a factor k, the electrical and thermal resistance (defined in the next section) increase of k, while I_m should decrease of the same factor, enabling better power performances [33]. In addition, using a low current to induce the phase change is particularly advantageous for the chalcogenide material aging. Indeed, the use of high programming current can be detrimental for the material upon multiple programming of the memory state, since it generates a non-uniform reorganization of the material inside the programmed region. This phenomenon is known as material segregation.

Phase segregation

Studying the behavior of a GST based PCM after a programming cycle at temperature higher than $T_{c,GST}$ [34], S. W. Nam et al. demonstrated that the GST faced a phase separation into a Sb-Te-rich region and a Ge-rich one. Considering the pseudobinary phase diagram between Sb_2Te_3 and GeTe reported in Fig. 1.16, the phase separation can be explained by a non-congruent melting in the ternary compound: at 630 °C a Sb-Te-rich phase begins to melt, while the Ge-rich phase is solid between 630 °C and 650 °C. Furthermore, a poor electrical contact between the electrode and GST can further enhance the heat generation, pulling the Ge atoms away from the liquid region. The same behavior has been observed by comparing EDX images on GST based PCM [35]. As shown in Fig. 1.17, the material reorganization results in:

- a Sb-rich region close to the bottom electrode contact, which improves the contact

area with the phase-change layer and can potentially induce a reduction in the SET resistance along cycling;

- a Ge-rich region moving towards the external part of the Sb-rich region;

- an almost unchanged Te distribution in the overall layer.

Further studies demonstrated that the material segregation is dependent on the polarity applied to the device [36]. When the cell is subjected to a standard forward bias condition, the Sb-rich region locate in contact with the bottom electrode and it is surrounded by Ge-rich region, as described above. Crespi et al. [37] developed an atomic migration model based on Wall structure PCM which is in accordance with the experimental behaviour: the Ge and Sb segregation is a result of the themal diffusion, while the Te atom displacement is electrif field driven.
Materials not belonging to the stoichiometric tie-line face phase segregation as well. In particular, Ge-rich GST starts to segregates during its re-crystallization. In this case, first a GST or Sb-rich phase (i.e $Ge_1Sb_4Te_7$ or the $Ge_1Sb_2Te_4$) is formed due to its lower T_c; then, further crystallization induces a Ge-rich residual amorphous with a composition more similar to $Ge_3Sb_2Te_6$ or the $Ge_4Sb_2Te_7$, which is known to have a higher crystallization temperature (see Fig. 1.16 and Fig. 1.2) [38]. Whereas, in Sb-rich GST [39], the Sb in excess does not fill up the vacancies of the NaCl-type structure: the material is quite similar to GST and the Sb in excess remains amorphous by increasing its concentration at the grain boundaries.
However, this undesirable phenomenon is not always detrimental for the device. In fact, when the cell faces a stable elemental segregation, the device performance can be improved, particularly the endurance. As an example, Sb-rich confined PCM demonstrated the highest endurance in PCM, reaching 2 10^{12} cycles. In this case, a complete material segregation occurs in the first set of ten switching operations. As a result, a Sb-rich region is located close to the bottom electrode and it does not evolve throughout the cycling, avoiding both voids generation and further material segregation, ensuring the higher endurance [40]. The material segregation has also been exploited to develop Inter-Granular Switching PCM (IGS PCM) featuring both low power (i.e., programming current of 30 μA) and high endurance (10^{11} cycles) [10]. Unlike conventional memories, the IGS PCM is a multi-grained structure where the phase-change spreads only in the inter-grain regions. Therefore, the programmed volume is limited and the write energy reduced.
In conclusion, the material segregation is a phenomenon taking place in all the PCM devices. Nevertheless, by tuning the material composition, it can be finely controlled and exploited to improve the PCM performance depending on the target application.

Exploting segregation: from $Ge_2Sb_2Te_5$ to Ge-rich GST

The most commonly used phase-change material is $Ge_2Sb_2Te_5$. Nevertheless, it is not suitable for all the possible applications that PCM can fulfill. As an example, the use of PCM for automotive applications requires a stability of the amorphous phase for 10 years at 150 °C. This target cannot be attained by GST, due to its low crystallization temperature (around 150 °C). For this reason, different materials lying on the Sb_2Te_3-GeTe tie-line gained the attention of the scientific community. Some of

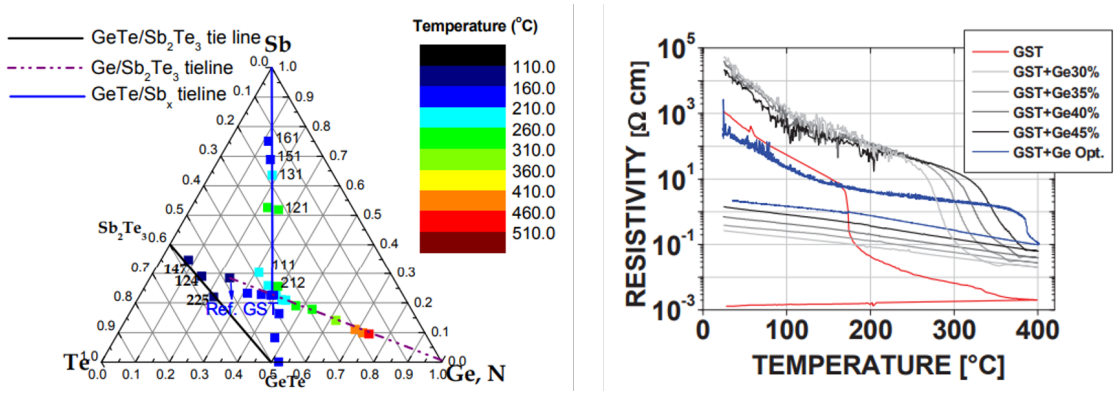

Fig. 1.18. (left) Crystallization temperatures T_x as a function of compositions in the Ge-Sb-Te ternary phase diagram [41].(right) Resistivity versus temperature for $Ge_2Sb_2Te_5$ and Ge-rich GST thin films, showing the increase of the crystallization temperature with increasing Ge content [42].

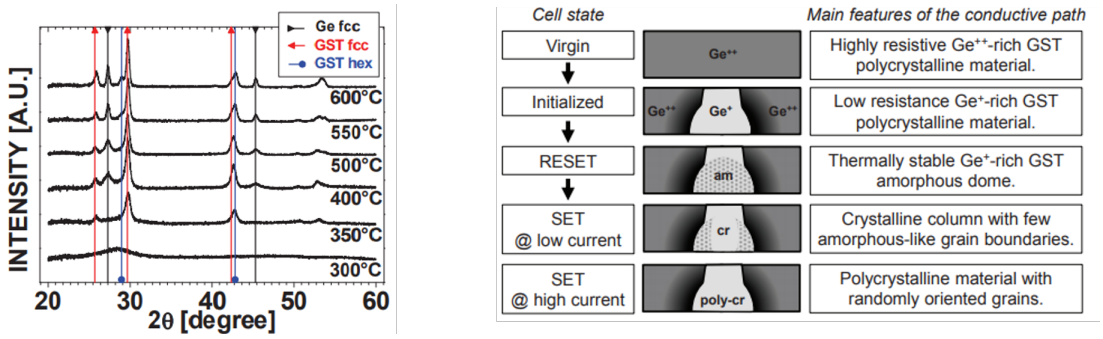

Fig. 1.19. X-ray diffraction (XRD) spectra of GST+Ge45% film after annealing at different temperatures, showing the phase separation of Ge and GST. Schematic of the composition and shape of the active volume during the programming of Ge-rich GST. [41].

the materials investigated are reported in Fig. 1.18, along with their crystallization temperature. It is evident that the Ge content can increase the crystallization temperature with respect to GST. This is further confirmed by the resistivity vs temperature analysis performed on different compositions obtained by increasing the Ge content in GST. In fact, the alloy with the higher Ge content demonstrates a crystallization temperature increase of more than 100 °C (which ensures a better thermal stability) as well as an increase of the crystalline state resistivity. These two features of Ge-rich GST compositions are advantageous when targeting automotive applications [43]. The higher crystallization temperature is explained by the increase of the tetrahedral Ge-Ge bonds induced in Ge-rich alloys [44] [45]. As a result, the material has a more disordered structure, leading to a higher material resistivity and a slower crystallization mechanism [46].
XRD spectra performed at different temperature on GST enriched with 45% of Ge is reported in Fig. 1.19. These show that the material crystallizes at 350 °C and segregates in crystalline GST (fcc or hcp) and fcc Ge. An evidence of the material segregation induced in programmed PCM devices is reported in Fig. 1.19, where the phase-change material reorganization results quite similar to the one observed in GST (Fig. 1.17). At first, the highly resistive Ge-rich material is initialized: part of the Ge is moved out from the active area, while the rest is kept inside it, therefore, the programmed

region is still made up of a Ge-rich alloy. Consequently, the RESET state presents a high thermal stability, differently from the GST-based PCM. The Ge-rich composition achieved a data retention up to 10 years at 185 °C, which is above the requirements for automotive applications. The SET state of Ge-rich PCM, instead, is characterized by amorphous-like grain boundaries/randomly oriented grains (Fig. 1.19), resulting in the increase of the SET resistance drift coefficient with respect to GST based devices.

1.2.1.2 Electo-thermal properties

The electro-thermal behavior of the cell can be described by a classical heat transfer model in stationary conditions:

$$\nabla \cdot q = Q \tag{1.6}$$

where q is the thermal flux which obeys the Fourier's law of heat transfer:

$$q = -k_{th} \nabla T \tag{1.7}$$

and Q is the power density represented by the Joule heating induced by the external voltage applied to the cell:

$$Q = \vec{J} \cdot \vec{E} \tag{1.8}$$

In the previuos equations, k_{th} represents the thermal conductivity and $\vec{E}$ is the electric field ($\vec{E} = \vec{J}/\sigma$). Both the thermal and electrical conductivity are temperature dependent in the phase-change layer. By coupling Eq. 5.13 with Eq. 5.13 and Eq. 5.13, it is possible to predict the temperature achieved in a specific position of the memory thanks to the following expression:

$$\nabla^2 T = -\frac{J^2}{k_{th}\sigma} \tag{1.9}$$

Furthermore, it is possible to define the thermal resistance (R_{th}) of a PCM cell by considering the simplified Fourier equation:

$$\Delta T = P_{cell} R_{th} \tag{1.10}$$

where ΔT is the temperature achieved in the system with respect to room temperature and P_{cell} is the power injected in the system to obtain a specific ΔT, defined as:

$$P_{cell} = R_{ON} I^2 \tag{1.11}$$

where I is the current flowing in the system. The evaluation of R_{th} provides a quantitative estimation of the thermal efficiency of a PCM cell. Therefore, from Eq. 1.10 follows that the higher is R_{th}, the smaller the power needed to achieve a specific temperature in the cell. Hence, the variation in temperature inside the device can mainly be ascribed to: i) the thermal resistance of the device, which is dependent on the temperature variation of k_{th} and σ for the active layer and the material in contact with it ii) the device geometry, since the current required to achieve the melting at a specific J depends on the SET resistance. Consequently, the thermal conductivity of the materials used in the PCM as well as the device structure have a crucial role on the PCM performances. These aspects will be describe in detail later in this work, respectively

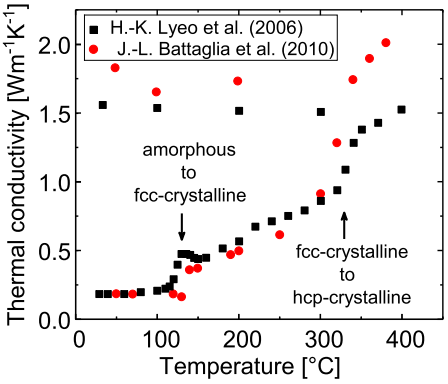

Fig. 1.20. Temperature dependent thermal conductivity values measured by TDTR by Lyeo et al. [47] and TDTR by Battaglia et al. [48]

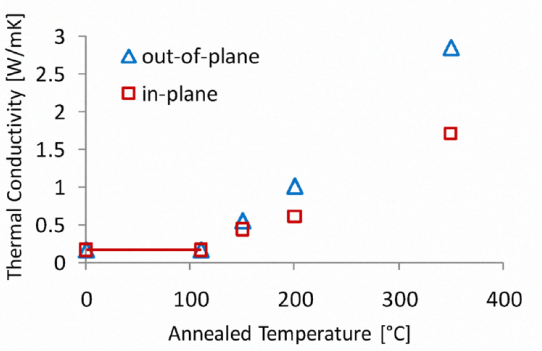

Fig. 1.21. In-plane and out-of-plane thermal conductivity values for GST at different annealing temperatures. The coefficient of thermal anysotropy is one for the amorphous GST, while it increases with annealing time, reaching for both a cubic and hexagonal GST a value of 0.6 [49].

in the next paragraph and in Ch.2.

Thermal conductivity characterization

The thermal conductivity of the phase-change materials and of those being in direct contact with it, plays a key role in the device functionality. Indeed, a small variation in k_{th} can cause a significant change of the temperature profile inside the cell, affecting the device performance. For this reason, the interest to characterize the thermal conductivity of the materials involved in the PCM devices has increased. In particular, the measured thermal conductivity value can enable an accurate electro-thermal modeling of the memory [50], that can be exploited both to predict the device performance and to propose innovative solutions to improve it.
The two most used methods to evaluate the thermal conductivity of conductive and non-conductive layers are: the 3ω method and the Modulated Photothermal Radiometry (MPTR). The former is based on an electric measurement performed via the contact of the probes on an electrode heater deposited on top of the tested material. The latter, is a contactless method. It is based on the optical measure of the radiation emitted by the sample, in response to a photothermal excitation by a laser beam.
In the first studies, the out-of plane thermal conductivity of phase-change materials has been evaluated at room temperature and a thermal annealing was used to carry the material either in the crystalline or in the amorphous phase before their characterization [51]. Lately, the test procedure have been improved and the thermal conductivity measurements has been performed under a continous temperature increase, allowing the thermal conductivity characterization during the phase transition. The GST thermal conductivity evaluated with the 3ω method showed a $k_{th} \sim 0.14$ $\mathrm{Wm^{-1}K^{-1}}$ in the crystalline phase and $k_{th} \sim 0.39$ $\mathrm{Wm^{-1}K^{-1}}$ for the amorphous one [50].
In the same way, H.-K. Lyeo et al. [47] and J.-L. Battaglia et al. [48] used non-contact methods (time-domain termoreflectance (TDTR) and Photo-Thermal Radiom-

etry, respectively) to measure the thermal conductivity evolution in temperature for $Ge_2Sb_2Te_5$. The results, reported in Fig. 1.20, present comparable trend, with a first k_{th} increase in correspondence of the amorphous to crystalline transition and a second one at around 350 °C, in line with the fcc to hcp-crystalline transition. Furthermore, in both cases, the thermal conductivity remains stable at 1.6 $Wm^{-1}K^{-1}$, when the material is characterized at room temperature after the same annealing thermal budget. These results are comparable with other works reporting the thermal conductivity on both amorphous GST ($k_{th} \sim 0.2$ $Wm^{-1}K^{-1}$) [51] [52] and fcc-crystalline GST ($k_{th} \sim 0.5$ $Wm^{-1}K^{-1}$) [51] [53]. Moreover, the transition temperatures from amorphous to crystalline and crystalline to hexagonal are consistent with the one observed in resistivity versus temperature measurements [54].
The small differences in the amorphous k_{th} values, follow the minimum thermal conductivity approximation [55] [47]. It assert that in disordered crystals the presence of structural defects does not impact the thermal conductivity value obtained by modeling phonon transport as a system of localized oscillators. In addition, this is in accordance with the hypothesis of phonon driven thermal transport for amorphous GST [56]. Therefore, the small k_{th} variation observed can only be addressed to the partial re-crystallization of the amorphous [57] or to the presence of thermal boundary resistance (when the effective thermal conductivity is measured [58]). On the contrary, the crystalline phase transport is mainly dominated by electrons [56]. Furthermore the low k_{th} glass like values obtained for the crystalline GST are not surprising. Indeed, these are typical values for materials having a high concentrations of vacancies [55], which is the case in crystalline GST, as observed by Kolobov et al. [59]. Fig. 1.20 further shows that, unlike the amorphous to fcc transition, the fcc to hcp is really gradual. Lyeo et al. ascribed the phenomena to an evolving mixture of cubic and hexagonal GST, in the range of temperature investigated.
However, it is important to underline that all the presented works, independently from the method used, do not investigated temperatures higher than 400 °C, while the melting temperature of GST is around 600 °C. The impossibility to reliably test at high temperature is caused by the thermal diffusion effect, which can impact the temperature profile [60] or cause the sublimation of the layer along with the electrode cracking [61]. Recently, with the optimization of the device structure and the development of highly scaled devices based on different thermal propagation mechanisms, raised the interest in the evaluation of the in-plane thermal conductivity. A first study performed on GST shows that the thermal conductivity anysotropy (i.e., ratio between in-plane and out-of plane k_{th}) in crystalline GST assumes values within 0.65 and 0.8 (Fig. 1.21). The phenomena is currently ascribed to the columnar grain structure of GST generated during the material annealing [62] [63] [49]. Nevertheless, further investigation are on-going to confirm this hypothesis.

Thermal boundary resistance

Another factor influencing the thermal properties of the PCM cell is the thermal boundary resistance (TBR). This arises from the partial transmission of heat carriers across an interface [65] and, importantly, it is not negligible with respect to the thermal resistance of the material itself. As an example, the TBR at the GST/Si interface (10^{-7} Km^2W^{-1}) is comparable to the R_{th} of a 100 nm thick hcp-GST [64]. In addition, the

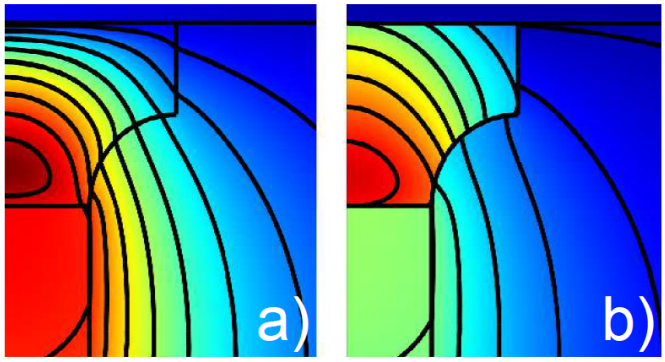

Fig. 1.22. Comparison of the temperature profile reached inside a memory cell a) with and b) without Thermal Boundary Resistance (TBR). When the TBR is taken into account, the temperature is more concentrated at the heater/chalcogenide interface [64]

impact of TBR represents a problem when dealing with thermal conductivity measurements. Indeed, the final thermal conductivity of a sample depends on the thickness of the tested material [58]: TBR has an higher impact on the final k_{th} for decreasing film thickness. Fig. 1.22 reports a comparison of the simulated temperature profile reached inside a memory cell in presence and absence of TBR. This demonstrates that the TBR plays an important role not only on the thermal performance of the device but also on the electrical one. Namely, it reduces its RESET current by moving the point of maximum temperature (i.e., hot point) toward the electrode/phase-change layer interface. Nowadays, the main challenge is to get an exact value for the thermal boundary resistance at particular interfaces. As a matter of fact, different models has been presented so far (e.g. classical mismatch model [66], metal-non metal TBR [67], metal-metal TBR [68]), but there is still not an accurate one able to describe the thermal transport at interfaces for different materials and temperatures.
In conclusion, the reliable measurement of the thermal boundary resistance at specific interfaces remains a current challenge. Despite many models have been proposed so far, they lack an accurate description of the thermal transport at the interface of different materials and for different temperatures. PCM technology would for sure benefit from TBR enginnering improvements; however, considerable efforts are still required to accurately investigate and characterize TBRs in PCM devices.

1.3 Chapter summary

Phase-Change Memories are two terminal devices where a phase-change material is sandwiched between two electrodes. Thanks to the threshold switching phenomenon, the phase-change materials undergo a phase transition, leading the material to an highly conductive state. Since the change of phase is reversible, then the two resistive states of the material are used to store the information. The high resistive state is associated to the logic state 0 (RESET), while the crystalline phase corresponds to the logic state 1 (SET).
The most common used phase-change material is GST, but it cannot ensure the desired properties for all the applications demanded by the market. Indeed, its low crystal-

lization temperature cannot fulfill the automotive application requirements. In this scenario, the higher crystallization temperature and resistivity of Ge-rich GST are exploited to achieve data retention up to 10 years at 185 °C, above the requirements for automotive applications.
Furthermore, to attain the crystalline-to-amorphous or amorphous-to-crystalline phase transition it is necessary to overcome the material melting temperature. After melting, the final state of the material depends on the amount of time given to the atoms to rearrange: a rapid quench will result in an amorphous phase, while the crystalline phase is obtained when the system has a sufficient time to recover the long range order. As a result, the amorphous-to-crystalline transition is the slower between the two. In particular, phase-change materials can be further classified based on their crystallization mechanism (nucleation or growth dominated), which define the speed of the phase transition.
In addition, the analysis of the band structure of the two phases highlights the difference in their conduction mechanism. The crystalline phase behaves as a degenerate semiconductor while the amorphous phase is described by a trap dominated conduction, commonly associated to a Pool-Frenkel like mechanism.
Since every programming operation involves the temperature increase above the phase-change material melting temperature, the electro-thermal analysis of the device represents an essential point for the understanding of the device functionality. As a matter of fact, it evidenced the necessity to reduce the programming current of the device in order to reduce as much as possible the power consumption and the material aging. In this direction, the characterization of the thermal conductivity of the phase-change layer and the other materials in its contact represent a crucial stepping stone to ensure accurate numerical models, able to reliably predict the device behavior and to propose further improvement to the device structure. The different strategies to develop low power PCM will be presented more in detail in the next Chapter.

Chapter 2

Phase-Change Memory challenges

One of the main challenges in Phase-Change Memory is the reduction of the programming current. Indeed, most of the power generated during the writing operation is dissipated in the surrounding of the active volume and only 1% is used to store the information.
In this chapter, the main sources of heat losses in a PCM device will be presented, discussing the need for a thermal engineering of the cell. The discussion will be focused on the main solutions proposed so far in the literature: i) modification to the structure; ii) the engineering of the interfaces between the phase-change layer (PCL) and the surrounding materials; iii) the tuning of the phase-change material composition.
Finally, a short digression on PCM targeting aerospace applications will be presented, discussing a potential link between radiation hardness and device geometry.

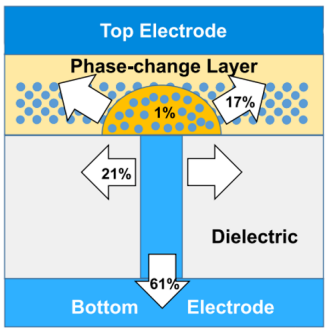

Fig. 2.1. Scheme of a PCM cell with arrows indicating the heat losses in the different regions of the cell. The main loss is the one through the bottom electrode. Only 1% of the injected power is used to program the cell [4].

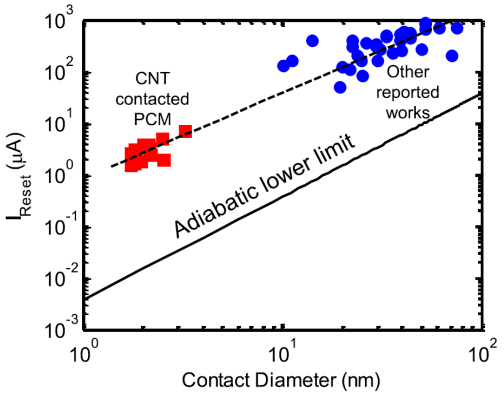

Fig. 2.2. RESET current as a function of the contact area between the heater and the phase-change layer. RESET current scales linearly with the contact area. As a reference, the adiabatic lower limit (assuming no heat losses) is also reported [69].

2.1 PCM engineering targeting low power consumption

The basic PCM cell is called mushroom or planar structure and it is made up of a patterned bottom electrode (or heater) and a planar phase-change layer deposited over the heater. In this structure a dielectric material is deposited in the regions where the phase-change layer is not in direct contact with the heater (see Fig. 2.1).
S.M. Sadeghipour et al. [70] first carried out a simulation study on the basic PCM cell, showing the spacial heat dissipation in the different components of the cell when the device is under programming conditions. As a result, they demonstrated that 61% of the heat generated during the programming of the cell flows in the bottom electrode, while 21% is dissipated through the dielectric which is in contact with the heater, and 17% is lost in the phase-change layer surrounding the active region. Therefore, only 1% of the energy generated by the application of the voltage pulse is used to program the cell (Fig. 2.1). In addition, the current used to bring the device in the RESET state (i.e. RESET or programming current) is dependent on the contact area between the phase-change layer and the bottom electrode. In fact, the comparison of experimental results available in literature, brought out the linear correlation between these two parameters (Fig. 2.2). Importantly, even if the contact area is reduced down to 20 nm, as with the Carbon Nano-Tube (CNT) contacted PCM, the experimental results are still far from the adiabatic lower limit [69], which assumes that all the power injected in the system is used to store the information (considering the ideal situation of an infinite thermal boundary resistance placed at the interfaces of the phase-change material). In particular, the RESET current is two to three orders of magnitude higher in the experimental results with respect to the simulated adiabatic lower limit performances, independently from the contact area dimension. Therefore, further engineering of the PCM device can be promising for the improvements of the thermal performance, allowing the PCM to work at a lower power. In particular, the main goal of this optimization is to keep a high temperature in the active volume in order to achieve the melting of the material at the lowest current possible, while

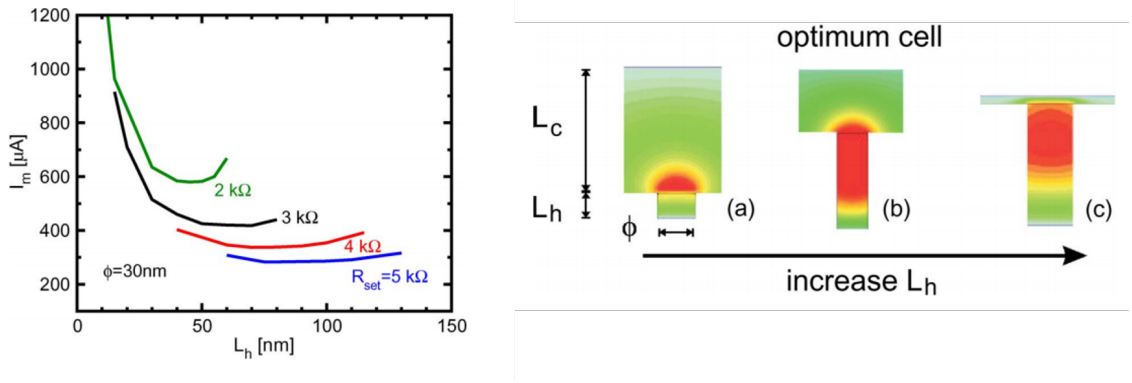

Fig. 2.3. left) Melting current (I_m) as a function of the heater length (L_h) for a fixed heater diameter $\phi = 30$ nm at different SET resistances obtained by tuning the phase-change layer thickness (L_c). right) Simulated temperature distributions in mushroom-type PCM cells for different non-isotropic scaling conditions.

ensuring a quick cool down of the active region to reach a reliable amorphisation. Even if these two requirements sounds contradictory, many research groups proposed different strategies to improve the thermal performances of the cell, which will be presented in the next paragraphs.
At first, the linear trend between the RESET current and the contact area suggests the contact area scaling as a strategy to attain low power performance. This can be realized either by the development of new device structures or by the use of a non-conductive interfacial layer interposed between the phase-change material and the bottom electrode. These solutions will be analyzed in more details in Section 2.1.1 and Section 2.1.2, respectively. In addition, as highlighted in Fig. 2.1, a relevant amount of heat is lost through the materials in close contact with the active layer. This lead to consider the material engineering as a further aspect to be investigated and optimized. In fact, tuning the material properties, the device thermal resistance will be modulated and, as a consequence, its electro-thermal response. At the moment, these solutions represent independent directions of research, but the final aim would be to be able to integrate more solutions in the same device, achieving the optimization of specific performance, depending on the targeted application.

2.1.1 Device structure engineering and scaling

The first studies performed on the device structure engineering were mainly based on the analytical and numerical analysis of a mushroom PCM. This architecture was extensively studied by modeling the PCM with its equivalent circuit [73]. The study highlights the advantage of device scaling, considering the fabrication constraints such as the fabrication of high aspect ratio structures as well as the difficulty to achieve a good uniformity in thin layers. This analysis demonstrates that, under isotropic scaling by a factor k (i.e., the interface between heater and phase-change layer (ϕ), the chalcogenide thickness (L_c) and the heater height (L_h) are all scaled by the same value), the thermal, SET, RESET and ON-resistances scale of the same factor. On the contrary, the RESET current and the power dissipated scale with a factor $1/k$ [32], enhancing the device thermal performance.

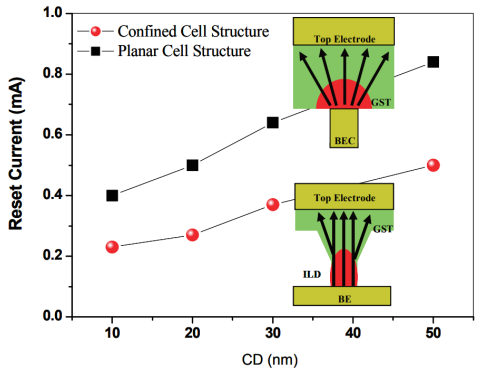

Fig. 2.4. Comparison between a planar and a confined architecture in terms of RESET current as a function of the contact diameter (CD). The confined structure presents a reduction in the programming up to 50%, independently from the CD [71].

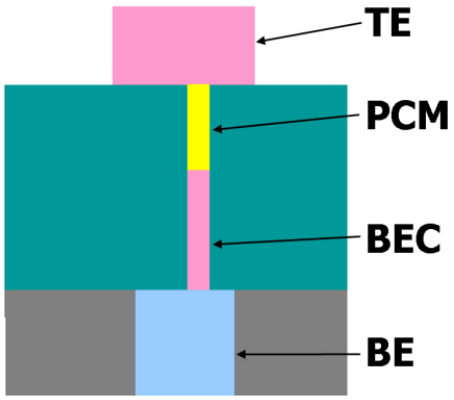

Fig. 2.5. Scheme of a dash-confined structure characterized by the self-alignment of the phase-change material (PCM) with the bottom and top electrodes (TE and BE). A bottom electrode contact (BEC)is deposited in the same pore of the phase-change material [72].

A non-isotropic scaling was also investigated. It has been obtained by changing ϕ, L_c, L_h in an independent way. The dependency of the melting current as a function of the heater height for different SET resistances (i.e., L_c tuned with respect to L_h to keep the same resistance value) is reported in Fig. 2.3,left. Interestingly, tuning a single characteristic dimension of the device leads to a significant reduction of the melting current. The non-isotropic structures exhibit an important difference in the temperature profile, depending on the L_c and L_h parameters (Fig. 2.3,right). This can be strictly related to the impact of the different aspect ratio on the thermal resistance of the overall system. In this scenario, the optimum cell is considered the one having the hot point closer to the interface between heater and phase-change layer, since this represents the region where the information is stored (Fig. 2.3,right).
The advantage of using a scaled mushroom cell was also evidenced via experimental study. The engineering of this specific architecture reduced the RESET current from 1 mA, achieved with a 180 nm PCM [74], to 700 µA in a 60 nm one [75]. In addition, further studies opened the possibility to store multiple bits in the same device [76].
Different architectures were studied as a replacement of the standard mushroom-like PCM. The main solutions presented can be classified in two main groups: *built-in heater* and *self-heating* PCM.

Built-in heater PCM

Built-in heater structures optimize the PCM power consumption by investigating the reduction of the contact area between the electrode and the phase-change material and can be subdivided into three main categories: pore-type (and dash-type), trench-type and Wall-based PCM.
The pore-type PCM was firstly introduced by Pirovano et al. [32], featuring a 50% reduction in the programming current with respect to a standard planar cell, as evidenced in Fig. 2.4. The structure is basically characterized by a phase-change layer (PCL) deposited in a pore, which is opened inside an insulation layer. Therefore, the dimension of the active region is related to the pore size. Its dimension defines, as a consequence,

the RESET current. In this type of architecture, the deposition of GST with standard sputtering processes is challenging in terms of conformity, especially when the pore dimension presents a high aspect ratio. A novel GST deposition process based on in-situ deposition/etch/deposition method was presented [77], demonstrating an excellent conformity and ensuring a better contact with the top electrode. In addition, the PCM fabricated with the new process shows a RESET current reduction down to around 500 μA and endurance up to 10^9 cycles. Further investigation led to the first demonstration of a high aspect ratio pore-like PCM obtained with GST deposited by Chemical Vapour Deposition (CVD) [71]. It features a RESET current of less than 260 μA and endurance up to 10^8 cycles without failure.
An innovative pore-like PCM was introduced in 2015 [72]. It consists of a phase-change layer and a bottom electrode contact deposited and aligned in the same pore, as shown in Fig. 2.5. This structure is defined "dash-type" PCM and it is fabricated by filling the recessed dash-type bottom electrode with CVD-PCM. This structure can be scaled down to 7.5 nm width and 30 nm depth while still ensuring high performances.
The μ-trench like PCM, instead, was firstly presented in 2005 [78]. In this architecture, the contact area between the heater and the phase-change layer is defined by the intersection of a thin vertical semi-metallic heater with a trench (called μtrench) in which the GST is deposited (Fig. 2.6). The great advantage of this solution is the easy size tuning, since the μ-trench dimension is defined by sub-litho techniques while the heater thickness by standard film deposition. A μ-trench device integrated with a 0.18 μm CMOS process demonstrated a RESET current of 600 μA and endurance up to 10^{11} cycles. Few years later, the suitability of such solution for the fabrication of high density arrays with programming currents of around 400 μm was also presented [75]. The structure was then further optimized by the use of a self-aligned pattern strategy, which simplified the integration process and still allowed a RESET current of 300 μA [79]. Later, the trench-type PCM was further improved by the development of a novel architecture, where a better contact between the phase-change layer and bottom electrode was ensured by the Chemical Mechanical Polishing (CMP) taking place in the fabrication steps before the deposition of the chalcogenide layer. This is known as Wall based PCM and it is able to integrate 1 Gb of PCM with a RESET current of just 200 μA on 45 nm PCM [80]. A scheme of this structure is reported in Fig. 2.7a).

Self-heating PCM

The self-heating PCM relies its functionality on the self-heating of the phase-change layer. In general, since both the electrical and the thermal conductivity of a calcogenide increases with temperature, the use of this structure can require higher current density. Nevertheless, its geometry can be tuned to refine the working point condition. In this family, the two main architectures developed are the *pillar* and the vertical *Wall*.
In the *pillar*, the active layer consists of a parallelepiped directly connected with the top and the bottom electrodes. In this case, the programming current can be tuned by modifying the aspect ratio of the chalcogenide layer. However, their programming current is still too high, with $\sim$ 3 mA demonstrated in [81] for a 45 nm PCM. This limitation led to the development of a second type of self-heating PCM, the *self-heating Wall*. This architecture present a structure similar to the built-in heater Wall but with the heater directly replaced by the phase-change layer. In this way, the contact area

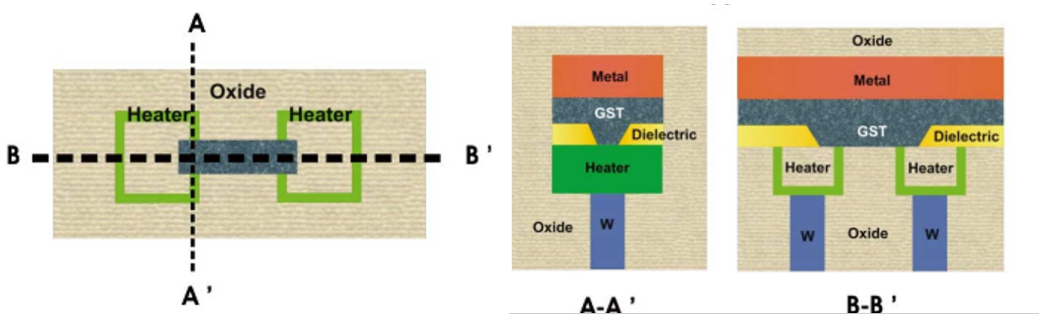

Fig. 2.6. Cross-section and top view of the μ-trench structure where the GST is deposited in a stripe over a thin metallic heater [82].

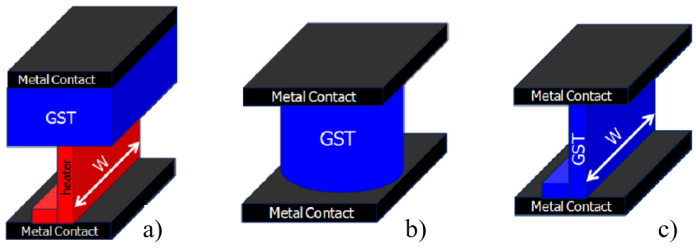

Fig. 2.7. Scheme and TEM image of different PCM architectures: a) Wall b) pillar c) self-heating Wall (sidewall) [81].

between the electrode and the phase-change layer deposited by CVD get reduced.

A comparison of three of the device architectures presented, i.e., a) *Wall*, b) *pillar* and c) *self-heating Wall* (Fig. 2.7), was performed by Boniardi et al. [81]. This detailed study on the integration process and on the thermal behavior of each of these architectures identified the heater-based Wall architecture as the one ensuring the best trade-off between process integration and performance and still showing many possible knobs for optimization.

2.1.2 Phase-Change material encapsulation

The use of an encapsulation layer for phase-change materials was first introduced when these materials, in a nanoparticles format, were under investigation for thermal energy storage applications [83, 84]. In particular, coating phase-change materials nanoparticles with an encapsulation layer provided better thermal performances.
In PCM devices, heat losses phenomena are amplified by the the presence of the materials in direct contact with the chalcogenide layer (i.e. dielectrics or metals), which have a thermal conductivity at least one order of magnitude higher than the PCL one. As a consequence, the heat is dispersed in the surrounding, rather than being confined in the active layer, where the storage of the information occurs. Therefore, the PCL encapsulation is fundamental to ensure a better thermal efficiency of the device. Until now, different works focused on the engineering of the interfaces between the PCL and the surrounding materials. The main solution involves the optimization of the interface between the phase-change material and the bottom electrode, since it has the higher

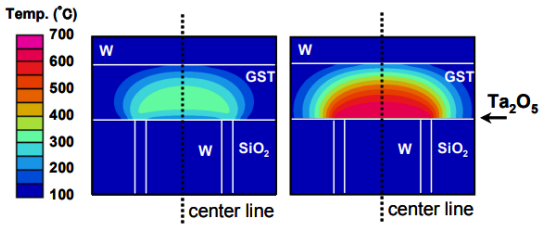

Fig. 2.8. Comparison of the temperature distribution achieved in the memory cell left) without and right) with a 2 nm thick Ta_2O_5 interfacial layer. In presence of the interfacial layer, more heat is retained at the heater/PCL interface, improving the device thermal performances [85].

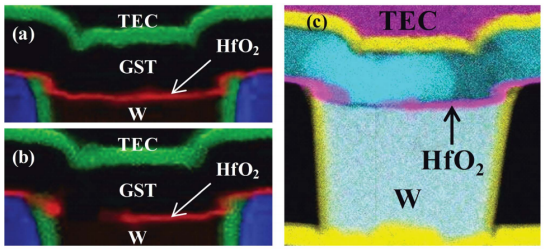

Fig. 2.9. Cartography of the EDX spectra performed on a cell with a 8 nm thick HfO_2 interfacial layer: a) in as-deposited condition; b) after initialization, evidencing the constriction created in the HfO_2; c) after programming in RESET state, highlighting an accumulation of antymony in the active volume (light blue region) [86].

contribution to the heat losses [4]. In the following, the PCL encapsulation strategies developed so far will be presented, discussing separately the top electrode and dielectric engineering as well as the optimization of the phase-change material.

2.1.2.1 Bottom Electrodes engineering

The 61% of the power injected in a planar PCM cell is lost through the bottom electrode (Fig. 2.1). To guarantee an efficient heating of the PCL, recent studies proposed the use of electrodes materials characterized by a high electrical resistivity and a thermal conductivity as low as the phase-change material one [87]. Nevertheless, a PCM cell integrating a high resistivity heater can present incomplete material crystallization along with an intrinsic total resistance increase. This is ascribed to the higher value assumed by the heater resistance [88].
The introduction of a thin Ta_2O_5 layer to improve the adhesion between the bottom electrode and the calchogenide layer brought to the discovery of Ta_2O_5 as a thermal barrier. Indeed, it boosted the heat concentration in the bottom part of the PCM (Fig. 2.8) with almost 80% of current reduction. Importantly, these performances were obtained without any modification to the fabrication process and the electrode material used.
Due to these promising results, further improvements to the materials and layer thicknesses were investigated. Among the materials proposed, fullerene [89] and TiO_2 [90, 91, 92], were integrated in different thicknesses configurations up to 30 nm. Fullerene C_{60} exhibits a better PCM thermal insulation due to the large mismatch in vibrational spectra, resulting in a RESET current reduction of about 70% with respect to the structure without the C_{60} layer. Nevrtheless, the introduction of a supplementary layer causes an extra series resistance added to the device. In particular, this can impact the device reliability, especially when the interfacial layer is thicker than 10 nm. Therefore, the interest in working with 2D materials has increased and the use of graphene has been tested [93, 94]. In such devices, a 40% reduction of current was registered. Basically, the graphene layer behaves as a thermal barrier in the out-of plane direction and reduce the heat losses in the in-plane one.
The mechanism of current reduction due to the presence of a thick-3D interfacial layer

was explained only in 2011 by Q. Hubert et al. [95]. The comparison between a 4 nm TiO_2 and a 3 nm HfO_2 interfacial layer demonstrated the need of a forming initialization step, which makes the dielectric layer conductive. The mechanism consists in the application of a specific voltage (higher than the interfacial layer breakdown voltage) to the PCM, in order to create a filament in the interlayer, linking the GST with the heater. During the creation of the filament, part of the GST melts and diffuses towards the bottom electrode through the filament itself. This leads to a reduced contact area between the phase-change material and the heater, ensuring a reduced volume of material involved in the phase-change transition during the device programming operations. The filament generated in PCM integrating 8 nm HfO_2 is presented in Fig. 2.9.
In summary, the use of a thin interfacial layer (smaller than 10 nm) is an attractive solution to achieve a scaled contact area PCM at low cost (i.e. no additional lithographic step), preserving at the same time the device performance (low series resistance). This solution is a valid alternative to the use of highly resistive bottom electrode materials, which can make difficult the SET operation due to an incomplete material crystallization.

2.1.2.2 Top electrode engineering

The top electrode represents a further cause of heat losses compromising the PCM efficiency. When a high current is used to program a device, important dispersion in the top electrode can generate an erase failure in the not selected neighbor cell. In particular, Fig. 2.10 shows the formation of conductive paths in the central cell, previously in RESET state, when a RESET current is used to program the two neighbor ones [96]. This phenomenon is called thermal cross-talk and it assumes a relevant role when the cell is scaled down.
A possible solution to this problem rely on the optimization of the PCL/top electrode interface. Indeed, the integration of a capping layer can help to retain the heat inside the phase-change layer [97]. For this reason, the use of a carbon capping layer can be particularly advantageous, since its thermal conductivity can be easily tuned by its deposition temperature [98]. The active region in the device integrating the C layer (Fig. 2.11b) is more flat and is characterized by a higher maximum temperature with respect to the one without it (Fig. 2.11a). This effect is due to the better heat confinement inside the chalcogenide, which reduces the heat dissipation through the top electrode.
Another solution has been lately presented and it consists in the use of superlattices as a replacement of the top electrode material. Lu et al. [99] first presented the TiN(5 nm)-W(5 nm) superlattice as electrode material for low power applications. The structure has been lately further improved by the study of TiN-W superlattice in different configurations, obtained by modifying the thickness ratio between the two materials [100]. The best stack is the one ensuring a low thermal conductivity as well as a low electrical resistivity, since this will avoid heat losses and high self-heating of the cell, respectively. In general, both conditions are respected in superlattice since i) the phonon scattering at the interfaces between the two materials reduces the thermal conductivity and ii) the electrical resistivity of the superlattices already tested is three orders of magnitude lower than the PCL one.
All the presented solutions are competing to lower the thermal cross-talk in the next

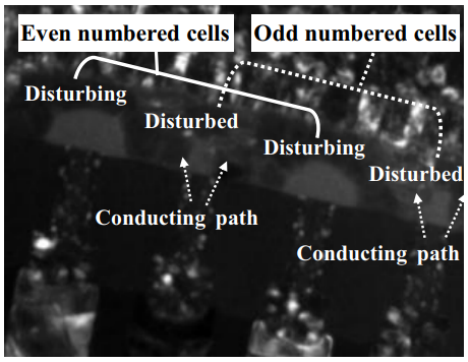

Fig. 2.10. Characterization of the reset volume size in three adjacent cells. Conductives paths are observed in the central cell along with a reduction of the amorphous volume compared to the neighbour cells. The programming of he even numbered cells is inducing a disturbance to the odd numbered ones, which are pre-programmed in RESET [96].

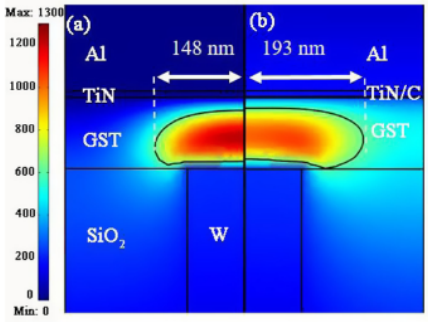

Fig. 2.11. Temperature profile comparison of a cell in RESET state a) without and b) with carbon layer. The solid black line represents the limit of the melted region in the two structures. It evidences a more pronounced horizontally-extended region which can ensure a lower programming current when a top C layer is integrated [98].

generation PCM devices.

2.1.2.3 Dielectric engineering

Among the possible boundary interface improvements to optimize the thermal management in PCM, the PCL/dielectric interface represents the less investigated one. Most probably, this is linked to the distance of the dielectric layer from the point of maximum temperature, where most of the Joule heating is generated. Furthermore, in a planar structure, the dielectric has only a second order impact on the device thermal losses: just 21% of the power is lost in the dielectric, compared with 61% dispersed in

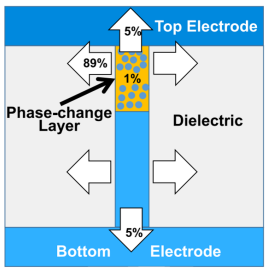

Fig. 2.12. Scheme of a dash-confined cell with arrows localizing the heat losses in the different regions of the structure. The main loss is the one through the dielectric surrounding the pore filled with phase-change material. Only 1% of the injected power is used to program the cell [4].

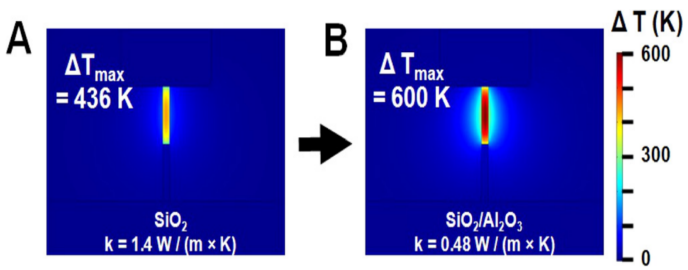

Fig. 2.13. Simulated temperature profile achieved in a dash-confined cell with A) SiO_x and B) SiO_x/Al_2O_2 as dielectric surrounding the phase-change material and the bottom electrode, respectively. The lower thermal conductivity of SiO_x/Al_2O_2 leads to a higher temperature in the active layer hence a better thermal efficiency [4].

the bottom electrode (Fig. 2.1).
Nevertheless, the development of new confined architectures changed the electro-thermal response of the cell. As a matter of fact, electro-thermal simulations showed that in a dash-type phase-change memory the 89% of the injected power is lost in the dielectric. This caused to shift the focus towards this region of the PCM device (Fig. 2.12). The dielectric engineering was first exploited in 2015 with the development of a vacuum-isolated self-aligned nanowire (NW). In this structure, the chalcogenide material was deposited in a nanowire shape between the top and the bottom electrode contact. The NW was deposited in a semispherical cavity obtained by etching the SiO_2 layer, previously deposited. The vacuum-insulated NW presented a ten times lower RESET current with respsect to a planar cell, mainly due to the absence of heat conduction in the lateral direction where the active region was surrounded by the vacuum [101].
More recent studies on industrial-like devices compared the impact of two superlattice-like dielectrics as a replacement of the standard SiO_2, generally used in the integration of dash-type PCMs: SiO_2/Al_2O_5 and SiO_2/Si_2N_4 [102]. They first measured the thermal conductivity of SiO_2/Al_2O_5 and SiO_2/Si_2N_4 in different thicknesses ratio, from 100 K to 500 K. The two stacks present respectively a 64% and 15% thermal conductivity reduction with respect to SiO_2. The authors suggested that the discrepancy in the thermal conductivity values can be related to the difference in film quality and to the finite interface thermal boundary resistance in the superlattice structure. Therefore, SiO_2/Al_2O_5 was chosen as a replacement of SiO_2, due to its lower thermal conductivity. In addition, the electro-thermal analysis of the device was simulated to compare the temperature distribution generated at a specific power injected for SiO_2/Al_2O_5 based devices, with respect to the SiO_2 based ones (Fig. 2.13). The cell integrating the multilayer stack attains a 38% higher heating as a proof of the lower power required to switch the device. Given the promising simulation results, the solution was integrated in real devices [103]. A 60% reduction in energy used to RESET the cell was confirmed. This result is encouraging and increases the interest in the engineering of the dielectric materials directly in contact with the phase-change layer.

2.1.3 Phase-change material engineering

The Phase-Change Memory performance rely on the properties of the material used as an active layer. Several studies investigated the device functionality for different active layer material composition. This section will be mainly focused on the materials that demonstrated improvements in the thermal response of the cell.
A shared strategy among the different solutions proposed in the literature is the phase-change material doping. In 2003, Hwang et al. [105] doped the standard GST with different concentrations of Nitrogen (N). N doping increases the thermal confinement inside the layer ensuring a 30% RESET current reduction with respect to undoped GST. The N doping was tested and showed a thermal efficiency improvement in different PCM architectures [77]. Oxygen doping [106] also represents a good candidate for thermal improvement since it reduces the GST grain size, ensuring a better thermal stability of the active layer. In particular, SiO_x doping induces an increase of the SET resistance and a consequent lowering of the RESET current. Such effect was associated to the lower thermal conductivity and higher crystallization temperature measured for

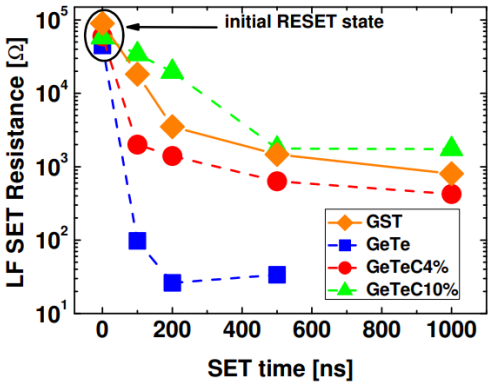

Fig. 2.14. Performance comparison for different materials: GST, GeTe and C-doped GeTe (GeTeC4% and GeTeC10%). GeTeC10% has a SET speed comparable with GST while requiring less than half of its programming power [104]. The point correspondent to 0 ns reports the initial resistance value of the PCM in RESET state.

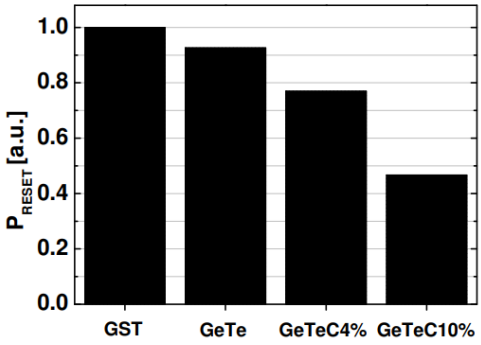

Fig. 2.15. Comparison of the mean RESET power required to program the PCM for different active materials: GST, GeTe and C doped GeTe (GeTeC4% and GeTeC10%). The RESET mean values are normalized with respect to the GST ones [4].

materials having the higher concentration of oxygen in SiO_x.
Carbon doping, instead, offers an important current reduction (around 50%) but a lower crystallization speed with respect to GST [107]. To avoid the degradation of the SET speed when a C doping is introduced in the active layer, material in principle faster than GST were considered, like those belonging to the GeTe-Sb_2Te_3 tie-line. Some works exploit the doping of GeTe with Carbon [104] and Sb_2Te_3 with Ti. In particular, carbon-doped GST in different percentages (4% and 10%) was studied. Its performances were compared with those of GeTe and GST. The high SET speed of GeTe (200 ns) led to a speed comparable to the GST one when a 10% carbon doping was introduced in the GeTe layer (Fig. 2.14) along with a RESET power reduction of more than 50% with respect to GST, as reported in Fig. 2.15.

Ti doped Sb_2Te_3, instead, presented both a higher SET speed and RESET power reduction up to 78% compared to GST. The power reduction in this case has been ascribed to an atomic rearrangement, responsible for the creation of strong Ti-Te bonds, compared to the weaker Te-Sb one. The Te-Sb bonds are easily breakable compared to the Ti-Te ones, promoting a low-power RESET operation [109]. Further studies aimed to optimize the Ti content in the composite material. Interestingly, in the higher Ti concentration analyzed ($Ti_{0.56}Sb_2Te_3$), the thermal conductivity reduces from $\sim$ 0.7 $Wm^{-1}K^{-1}$ in Sb_2Te_3 to 0.2 $Wm^{-1}K^{-1}$ [108]. The decrease of the thermal conductivity with Ti doping is suitable for low power applications, since it improves the thermal response of the device. The k_{th} of both the crystalline and the amorphous layer as well as the temperature profiles simulated in all the investigated compositions are reported in Fig. 2.16. Furthermore, the Ti doping i) increases the crystallization temperature, which is fundamental to have an amorphous phase more stable in temperature; ii) reduces the material roughness, which is linked with the strong reduction in grain size with Ti content; iii) reduces the density variation between amorphous and crystalline phase, resulting in a longer lifetime of the device; iv) increases the speed

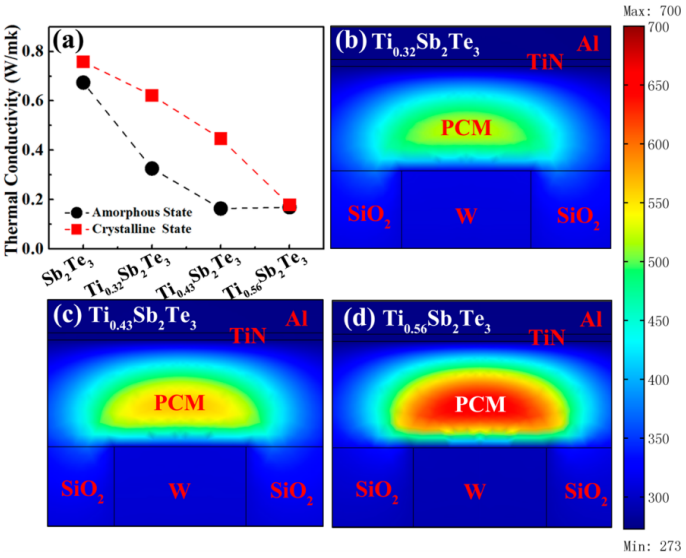

Fig. 2.16. (a) Comparison of the thermal conductivity value in the amorphous and crystalline phase of Sb_2Te_3 pure and doped with different Ti concentrations. Simulated temperature distributions achieved in the memory when programmed in RESET state for (b) $Ti_{0.32}Sb_2Te_3$, (c) $Ti_{0.43}Sb_2Te_3$, and (d) $Ti_{0.56}Sb_2Te_3$ layers, respectively [108].

till 10 ns thanks to the smaller grain size [108]. The Ti doped Sb_2Te_3 solution was integrated in 40 nm node technology [110] still showing an improvement in the device performances, making it promising for the next generation of low power PCM.
An alternative to the material doping is given by the integration of SuperLattice-Like (SLL) active layers. The idea is to create a multilayer structure by the repetition of two materials. To achieve the best performances in PCM, the multilayer is made up of a material with a high crystallization speed and the other with low crystallization speed, but high stability. This allows the final device to have at the same time high speed and good stability [111]. Furthermore, the phonon scattering at the interfaces between the different layers of the superlattice induces a reduction of the overall k_{th} [112, 113], enabling, at the same time, a better thermal response. Therefore, the surface roughness between the two materials is among the key parameters to be accounted for SLL-based PCM [114].
Multilayers represent an attractive strategy for the possibility to tune their electrical properties by modifying the thickness and the materials used in the stack [115]. One of the most studied SLL structure is the repeated GeTe-Sb_2Te_3 bilayer stack [111], having a 30% lower thermal conductiviy with respect to the single layer GST. This solution favors a current reduction of the 62% and a faster crystallization speed (Fig. 2.17) with respect to GST. A more detailed analysis of the SL based PCM performance, evidenced a better thermal efficiency with respect to the conventional device, mainly attributed to the one order of magnitude difference in thermal resistance between the two structures [116]. Moreover, the SLL structure is stable even after 10^5 cycles as demonstrated by Transmission Electron Microscopy (TEM) analysis reported in Fig. 2.18.

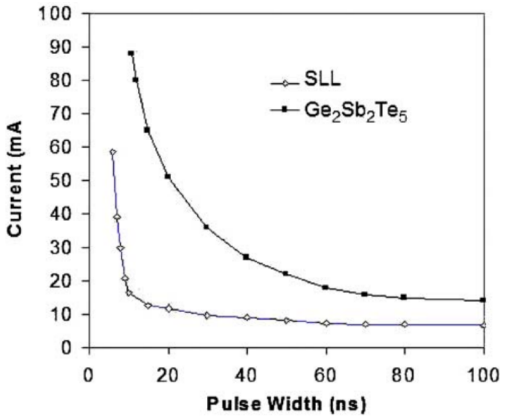

Fig. 2.17. RESET current as a function of pulse width for both superlattice and GST, showing the higher crystallization speed of SLL [111].

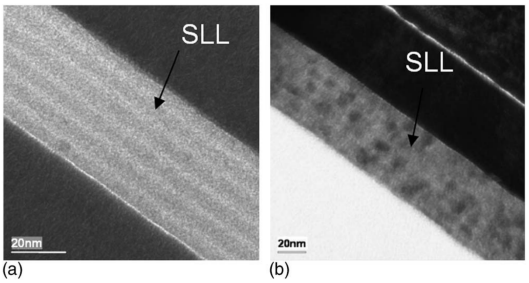

Fig. 2.18. Transmission electron microscopy (TEM) images showing the device a) as fabricated and b) after 100 000 programming cycles [111].

2.2 PCM for aerospace applications

As previously discussed, the device structure and the materials integrated in the PCM must be adapted according to the targeted application. For instance, in Section 1.2.1.2, the Ge-rich GST was presented as an alternative active material able to attain the requirements for automotive applications (i.e., stability of the amorphous phase for 10 years at 150 °C). Similarly, aerospace applications necessitate for device capable to withstand ionizing radiation.

After the discovery of some anomalies in the satellite functionality in 1975 explained as a consequence of their interaction with cosmic rays [117], the effect of radiation on memory devices was investigated experimentally [118]. This study boosted the interest in the device engineering in terms of information storage mechanism, feature size, array architecture and peripherical circuitry optimization.

In general, ionizing radiation creates electron-hole pairs that can generate a transient current (Single Event Effects or SEE) or interface states (Total Ionizing Dose or TID), modifying the standard working principle of the device. In floating gate memories, such as NAND and NOR Flash, the impinging particle can create electron-hole pair, causing a shift in the device threshold voltage. This lead to soft errors (i.e., transient errors).

Unlike Flash, PCM are not based on charge storage and, as a consequence, have high tolerance to radiation. This feature was foreseen since the discovery of phase-change materials [9]. Ab initio molecular-dynamics simulations demonstrated that the radiation hardness of GST is mainly associated to a small variation in the atoms distribution after irradiation. This is explained by the highly flexible bonding and the high percentage of void volume within the material, responsible of its reorganization within 15 ps after the collisions [119]. Furthermore, a particle hitting on a PCM induces a current variation which is generally negligible with respect to the standard current used to program the cell (order of μA). Therefore, one of the main limitations for the radiation hardness in PCM arrays is represented by the radiation impact on the CMOS external circuitry, not on the memory itself. This phenomenon was well evidenced in [120],

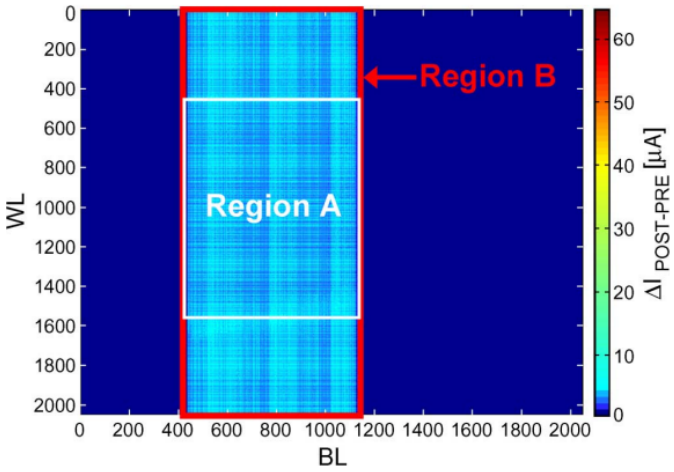

Fig. 2.19. Color map of the difference between the cells current measured before and after irradiation ($\Delta I_{POST-PRE}$) of a MOS-chip array by 30 Mrad SiO_2 proton beam. Region A is the irradiated zone and Region B is the area where a change in cells current higher than 1 μA was measured with respect to the pre-irradiation condition [122].

where 4Mbit PCM arrays were subjected to protons and heavy ions radiations: even if just part of the array was irradiated, the difference between the current measured before and after irradiation was higher than 1 μA in all the devices belonging to the same Bit Line (BL) or Word Line (WL) (Fig. 2.19). This result was mainly ascribed to the leakage current increase in the affected selectors. When the effect of TID has been studied on the same devices, just small variations between the distribution before and after the exposure were found. This was associated to the degradation of part of the phase-change layer, which anyway was not compromising the device functionality (i.e. the SET and RESET distributions were slightly impacted by radiation but still well separated). In addition, a study performed on PCM integrated with radiation-hardened CMOS evidenced the appearance of failure just associated to the external circuit [121].

Lately, the effect of the radiation on scaled devices was explored. The tolerance to radiation was still effective for as small as 90 nm PCM in 128Mbit [123]; nevertheless, the first evidence of information loss were identified in 45 nm Wall structure PCM devices. The devices were tested under two different conditions: i) terrestrial exposure, tested by the use of a wide energy spectrum neutrons beam and ii) heavy ions, to examine the space environment. As a result, neutron exposure did not generate any disturb, while the heavy ions irradiated device showed a measurable difference in the programmed state. The loss of the information took place when the ions beam was characterized by high fluences ($\sim 10^{10}$ iones/cm^2) and an impinging angle along the Word Line direction was used. In particular, the most significant disturb was measured for an impinging angle of 60° and only for devices previously programmed in SET (i.e. crystalline) state. The observed phenomenon could be related to a partial amorphisation of the phase-change layer. Whereas, no influence was triggered when the angle was settled along the BL, mainly due to the device structure. Indeed, in the structure analyzed in this work, the interface between the heater and the phase-change layer is rectangular, with the longer side oriented along the WL. Therefore, the authors do not provide a clear explanation of the degradation mechanism observed in PCM, simply

suggesting that it could be related to the device geometry. This increases the interest to test the radiation effect on state-of-the-art PCM devices integrating different materials and architectures to get a more clear overview on the radiation effect and to possibly detect further device improvements, targeting PCM aerospace applications.

2.3 Chapter summary

An important amount of the power injected in the Phase-Change Memory during the programming operation of the cell is dissipated in the surrounding materials. This is mainly caused by the difference in the thermal conductivity between the phase-change layer and the dielectric/metals directly in contact with it. Due to the linear relation existing between the programming current and the PCL/bottom electrode contact area, the device scaling represents the first approach to reduce the power consumption of the cell. Nevertheless, even considering devices down to the nanoscale, the performance are still far from the adiabatic lower limit. In addition, the fabrication of highly scaled devices requires aggressive lithographic step, rising the costs of the final product.
In this framework, the thermal engineering of the device represents a further direction for the development of the next-generation PCM. With this aim, different PCM architectures were presented and their performances compared. As a result, the heater-based Wall architecture was denoted to be the structure ensuring the best trade-off between process integration and performance, while still showing many potential knobs for optimization. Nevertheless, electro-thermal models showed that structural improvements do not lead to a significant reduction of the programming power of the cell, further evidencing the importance of tuning the properties of the materials surrounding the active layer (i.e., the phase-change layer encapsulation).
One of the most encouraging solutions described is the use of a 3D dielectric based interfacial layer (between 3 nm and 10 nm). Here, the creation of the filament in the interfacial layer links the heater with the GST and induces a reduction of the contact area, hence of the programmed region and power used. This is the ideal strategy to achieve a contact area scaling without any impact on the final cost. Another approach discussed in this chapter is the tuning of the dielectric directly in contact with the active layer. A SiO_2/Al_2O_5 multilayer integrated in a dash-type PCM showed a 60% reduction in the RESET energy. This result increases the interest in further optimization of the dielectric properties.
As anticipated in Chapter 1, the device structure and the materials integrated in the PCM need to be adapted according to the targeted application. In this chapter, the main studies performed on the PCM targeting aerospace applications were presented. First studies carried out on PCM integrated with CMOS evidenced the appearance of failures exclusively associated with the external circuit. Nevertheless, first traces of information loss were registered when the Wall size got reduced down to 45 nm. The information loss in this case was mainly associated to the rectangular shaped heater/PCL interface, because it arises only when the radiation impinges on the device at a specific angle parallel to the sub-lithographic dimension of the Wall. This phenomenon leads to a possible degradation of the information in highly scaled PCM under radiation exposure. Moreover, this proofs the need to analyze the radiation tolerance of PCM devices, especially in state-of-the-art architectures.

Chapter 3

Thermal conductivity of dielectric and conductive layers

As already presented in Ch. 1 and Ch. 2, the thermal conductivity of the materials involved in the PCM devices represents a crucial parameter to tune the electro-thermal performance of the device. Therefore, in this work, the thermal conductivity of materials integrated in state-of-the-art PCM devices was measured. This represents a valuable step for the electro-thermal simulation of the devices and for the interpretation of the electrical characterization results in the following part of this work.
Different techniques were developed in the literature for measurements of the thermal conductivity, such as the 3ω method and the Modulated Photothermal Radiometry (MPTR).
A 3ω test bench for the measure of the thermal conductivity of dielectric materials at room temperature was available in our laboratory. Nevertheless, the materials integrated in PCM devices include both conductive and non-conductive layers. In addition, being the PCM functionality based on Joule heating, a characterization of the thermal conductivity as a function of temperature is required. With this aim, the existing setup was optimized to ensure reliable and accurate measurements in different temperature conditions.
In this chapter, the electrode and the device stack composition were optimized in order to perform accurate 3ω thermal conductivity measurements at room temperature and at high temperature in both conductive and dielectric layers. In parallel, four theoretical models published in the literature were compared to identify the most accurate one for thermal conductivity evaluation. Finally, the 3ω test bench was validated by performing thermal conductivity measurements on the same samples by using two established MPTR setups at Institut de Mecanique et d' Ingenierie (I2M) de Bordeaux and at the Laboratoire National de Metrologie et d'essais (LNE) in Paris.

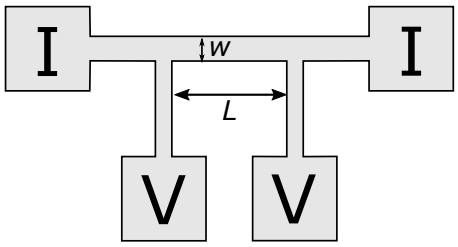

Fig. 3.1. Pattern of the electrode mask used for 3ω devices. In this method, the current (I) is applied at the external pads while the voltage response (V) is read in the two inner ones.

3.1 Thermal conductivity measurements by the 3ω method

3.1.1 The 3ω method

The 3ω method was first introduced by Cobino et al. [124] to characterize the thermal diffusivity of metal filaments for light bulbs applications. It was successively exploited by D. G. Cahill in 1986 [125] to measure the thermal conductivity of dielectric materials and later extended to non conductive ones [126].
This technique relies on a metal layer acting both as a heater and a thermometer, since it allows to heat the sample and to measure the amplitude of thermal heating induced in the underling materials.
To evaluate the out-of-plane component of the thermal conductivity, the electrode is patterned according to the scheme reported in Fig. 3.1. It consists of four pads connected to a thin line of length L and width w. The two external pads are used to deliver the current (I) while the other two are used to read the voltage (V) response generated by the resistance/temperature oscillation in the material.
To characterize the material, an AC voltage signal of amplitude V_0 is applied to excite the electrodes at a specific frequency ω. This causes an AC current of amplitude I_0 expressed as:

$$I(t) = I_0 cos(\omega t) \tag{3.1}$$

The current applied in correspondence of the two external electrodes (see Fig. 3.1) leads to a temperature rise in the sample, due to Joule heating. The power generated in the heater is:

$$P(t) = I^2(t)R_0 = \frac{I_0^2 R_0}{2}[1 + cos(2\omega t)] \tag{3.2}$$

where R_0 is the line resistance at room temperature. Since at small frequencies the temperature in the system varies in the same manner as the power generated, it is possible to express the temperature variation as:

$$\Delta T = \Delta T_{const} + \Delta T_0 cos(2\omega t + \phi) \tag{3.3}$$

with ΔT_{const} a constant, ΔT_0 the amplitude of the temperature oscillations and ϕ the phase difference with respect to the power generated. The periodic heating oscillation generates, as a consequence, the oscillation of the electric resistance in the metal line at a frequency 2ω:

$$R(t) = R_0[1 + \alpha(T)\Delta T] \tag{3.4}$$

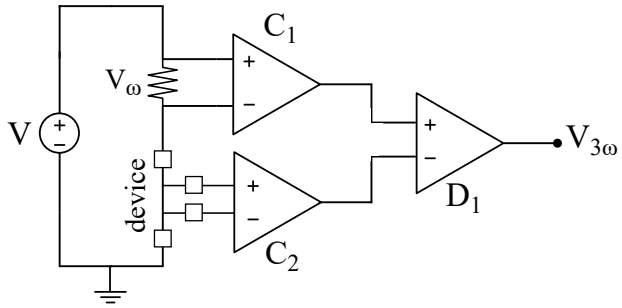

Fig. 3.2. Simplified scheme of the electronic circuit used for 3ω measurements. The channels C_1 and C_2 are used to balance the amplitude of the ω component so that the differential lock-in amplifier (D_1) can give in output just the third harmonic component.

with α being the temperature coefficient of resistance.
The Ohm law can be used to evaluate the potential response ($V(t)$) from the $I(t)$ and $R(t)$ values previously introduced:

$$V(t) = R(t)I(t) = I_0R_0[1 + \alpha(T)\Delta T_{const}]cos(\omega t) + \\ + \frac{I_0R_0\alpha(T)\Delta T_0}{2}[cos(3\omega t) + \phi] + \frac{I_0R_0\alpha(T)\Delta T_0}{2}[cos(\omega t) + \phi] \tag{3.5}$$

The first term is not dependent on the voltage amplitude and phase. It is typically three orders of magnitude higher than the other terms since the temperature coefficient of resistance is of the order of 10^{-3}. In addition, the third term has the same frequency component as the first one. As a result, the second term is the best one to be used in the evaluation of both the temperature amplitude and the phase of the thermal waves. It is dependent on 3ω, which represents the third order harmonic. Its amplitude is expressed as:

$$V_{3\omega} = \frac{I_0R_0\alpha(T)\Delta T_0}{2} \tag{3.6}$$

The measure of V_ω in correspondence of the two internal pads allows the evaluation of the amplitude of the temperature oscillations induced in the device (ΔT_0) which in turns gives the possibility to extrapolate the thermal conductivity of the tested material.
A schematic of the electronic circuit used to measure V_ω is reported in Fig. 3.2. The voltage at the inner pads can be expressed as a sum of the fundamental contribution plus its third harmonic, as in Eq. 3.5, while the voltage drop at the series resistance has the same fundamental frequency of the applied voltage. Hence, the V_ω signal is subtracted from the device signal (V_ω+$V_{3\omega}$) in order to get the final $V_{3\omega}$ component. The 3ω method is one of the most used in literature since it allows to resolve a signal variation associated to a temperature change of less than one degree, making it suitable especially for thermal conductivity measurements performed at temperatures ranging from 30 K to 300 K. The main drawback is represented by the electrodes which i) adds a thermal resistance to the material under test and ii) increases the heat flux at higher temperature inhibiting good probe-metal contact when the temperature is raised.

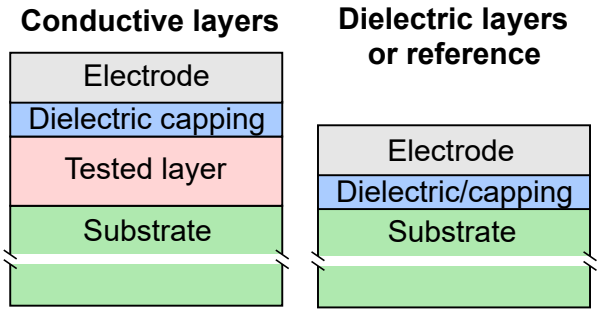

Fig. 3.3. Scheme of the cross-section of both the conductive and dielectric/reference structures. Notice that the thicknesses reported for the layers are not in scale.

3.1.2 Models for thermal conductivity measurements

Different methods are presented in literature to evaluate the thermal conductivity of non-conductive layers at room temperature. In general, when the thermal conductivity of a dielectric layer is measured, the sample is deposited in between the substrate and the electrodes (Fig. 3.3). Whereas, when a conductive layer is measured, it is necessary to add a dielectric layer (i.e., capping layer) of thickness t_{ox} between the tested layer and the patterned electrodes. The capping is used to avoid a distortion of the heat generated in the conductive layer, due to the possible parasitic currents flowing into it during the characterization. Its thickness is set to prevent the development of a leakage current while avoiding additional contributions to the thermal resistance of the device. Normally, the measure of the thermal conductivity of a conductive layer ($k_{th,film}$) requires a reference device made up of a capping layer deposited on top of the substrate Fig. 3.3. This allows to isolate the conductive layer contribution by subtracting the signal measured on the reference from the one generated by the sample integrating the conductive material to be tested.
Four methods were presented in the literature for thermal conductivity measurements, as described in the following:

The slope method

The slope method (M1) was developed to evaluate the thermal conductivity in dielectric materials [125] [128] [127] and it was then extended to conductive layers [126]. This method involves the measurement of the 3ω voltage component on both the reference and the device integrating the material specimen.
As a first step, the temperature oscillation generated in the heater due to the substrate is evaluated. Chaill [125] first expressed the temperature oscillations at the interface between the substrate and the heater as follows:

$$\Delta T_0 = \frac{P_l}{\pi k_{th}} \left[-\frac{ln(2\omega)}{2} + \frac{1}{2} ln(\frac{D}{b^2} + \eta - \frac{i\pi}{4}) \right] \tag{3.7}$$

The equation is obtained by assuming a 1D heat propagation. It considers the heater as a line source (i.e., the thermal wave penetration depth is large compared to the heater width w) and the substrate as a semi-infinite medium (i.e., the substrate thickness is greater than the penetration depth). Borca-Tasciuc et al. [126], instead, presented a

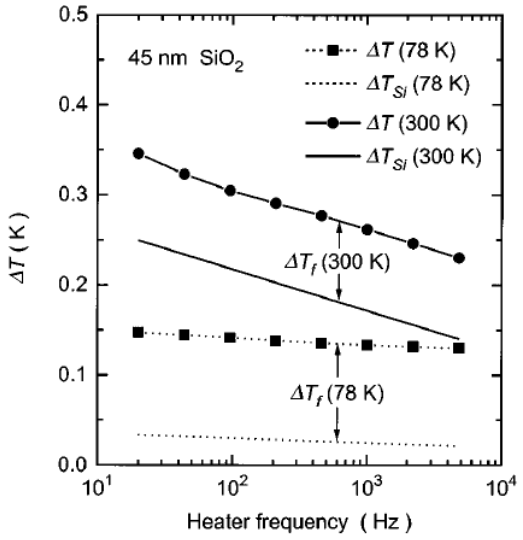

Fig. 3.4. Amplitude of the temperature oscillations (ΔT) as a function of the applied current frequency. ΔT is the sum of the Si substrate ΔT_{Si} (solid line for measurements at 300 K and dashed line for measurements at 78 K) and the film ΔT_f temperature drop [127].

theoretical model to express ΔT_0 based on a 2D heat propagation model:

$$\Delta T_0 = \frac{P_l}{\pi k_{th}} \int_0^\infty \frac{1}{\sqrt{k_{xy}x^2 + \frac{i2\omega}{\alpha(T)}} tanh(\sqrt{k_{xy}x^2 + \frac{i2\omega}{D}} t_0)} \frac{sin^2(\frac{Wx}{2})}{\frac{Wx}{2}^2} dx \tag{3.8}$$

where P_l is the power per unit length, k_{xy} described the xy plane thermal conductivity anisotropy in the Si substrate, D is the thermal diffusivity, t_0 the thickness of the substrate layer and x the distance from the heater.
Since the dielectric film deposited is thinner than the substrate, the final ΔT measured in the device is nothing more than the sum of the substrate contribution (ΔT_{Si}) and a constant film contribution (ΔT_{film}), independently from the frequency. Hence, the difference between the ΔT generated by the 3ω signal (evaluated from Eq. 3.6) and the theoretical ΔT_0 evaluated from Eq. 3.7 or Eq. 3.8, provides the amplitude of the temperature oscillation linked only to the contribution of the material specimen. Fig. 3.4 presents a typical trend for the temperature oscillation amplitude as a function of the frequency when a 45 nm layer of SiO_2 deposited on a silicon substrate is measured.
Finally, the thermal conductivity of the dielectric layer ($k_{th,ox}$) can be estimated by looking at the slope of the real part of the generated temperature increase as a function of the logarithm of the applied frequency:

$$k_{th,ox} = \frac{t_{ox} P_l}{\Delta T_{ox} w} \tag{3.9}$$

When a non-conductive layer is measured, the final k_{th} is recovered by taking into account i) the value of $k_{th,ox}$ in the reference device; ii) the difference in temperature increase between the sample and its reference; iii) the power per unit length value used to perform the measurements on the new sample. Therefore, the total temperature increase due to both the substrate and the dielectric layer ($\Delta T_0 + \Delta T_{ox}$) in a 2D heat

transfer model can be expressed as:

$$\frac{P_l}{\pi k_{th}} \int_0^\infty \frac{1}{\sqrt{k_{xy}x^2 + \frac{i2\omega}{\alpha(T)}} tanh(\sqrt{k_{xy}x^2 + \frac{i2\omega}{D}} t_{Si})} \frac{sin^2(\frac{Wx}{2})}{\frac{Wx}{2}^2} dx + \frac{t_{SiN} P_l}{k_{th,SiN} w} \tag{3.10}$$

and the final thermal conductivity be:

$$k_{th,film} = \frac{t_{film} P_l}{\Delta T_{film} w} \tag{3.11}$$

Differential method with reference (M2)

This method involves the measurement of the 3ω voltage ($V_{3\omega}$) component on the reference and on the sample, as for the previous approach. However, this work flow requires both the measurements to be performed at the same power P_l, thus allowing to evaluate the thermal conductivity without modeling the substrate thermal conductivity. Indeed, the thermal conductivity of the material under test can be estimated as [126]:

$$k_{th} = \frac{t_{film}}{2} \left[\left(\frac{2V_{3\omega} w}{P_l \alpha(T) V_\omega} \right)_{R+F} + \left(\frac{2V_{3\omega} w}{P_l \alpha(T) V_\omega} \right)_R \right]^{-1} \tag{3.12}$$

where the subscript R stands for reference and F for film.

Differential method without reference (M3)

In this strategy, the thermal conductivity of a film can be obtained by comparing the 3ω voltage generated in two samples having different conductive layers thicknesses. The difference between the temperature oscillations of the two devices provides a k_{th} value of a layer characterized by a thickness equal to the difference between the two. For instance, if the thicknesses of the conductive layers used are 100 nm and 200 nm, the method provides:

$$k_{th,film} = \frac{t_{film} P_l}{\Delta T w} \; where \; \Delta T = \Delta T_{200nm} - \Delta T_{100nm} \tag{3.13}$$

Method 4

Method 4 (M4) uses the same set of input measurements of M3. First, an effective thermal conductivity (k_{eff}) is evaluated by using a procedure similar to the first step of M1: here the $V_{3\omega}$ signal generated is associated to the whole stack at once (i.e., overall k_{th} of substrate plus tested dielectric material). With this method, the thermal conductivity is extracted by first measuring devices integrating a target layer of different thicknesses (t_{film}). This step is used to remove the contribution of the interface resistances from the final k_{film} value. Indeed, for each integrated thickness, the thermal resistance can be expressed as:

$$R_{th} = \frac{t_{film}}{k_{film}} + R_i \tag{3.14}$$

with R_i the total interface resistance of the layer including its contact with the electrode and with the substrate. The plot of the thermal resistance as a function of the material thickness allows the evaluation of i) the total interface resistance contribution (R_i) from the y-intercept; ii) the thermal conductivity from the inverse of the slope [58]. An example of this extrapolation process from 3ω measurements is reported in Fig. 3.5 for material with two thicknesses values (100 nm and 200 nm).

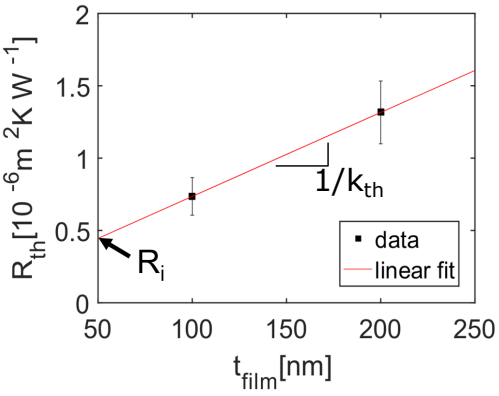

Fig. 3.5. Thermal resistance R_{th} as a function of the GGST thickness (t_{film}). The linear fit allows the evaluation of the interface thermal resistance (R_i) from the intercept and of the k_{th} from the inverse of the slope.

3.1.3 Experimental setup

A schematic of the circuitry used to perform the 3ω measurements is reported in Fig. 3.2. The AC voltage signal applied to the device is generated by an ultra-pure sinewave oscillator (Model 4402B). The use of a highly accurate generator is necessary because the measured $V_{3\omega}$ is thousand of times smaller than the fundamental frequency [129]. This oscillator is particularly suitable for our application since it is able to apply a signal at frequencies ranging between 1 Hz to 110 kHz with a typical distortion of less than 0.0005%.
A resistance $R_s = 10\ \Omega$ is connected in series with the device because it oscillates at the same frequency of the applied voltage, hence it can be used to cancel the ω component and isolate the measured third harmonic (see Section 3.1.1). The equivalence between the amplitude of the fundamental component generated by both the device and the series resistance is done by tuning the parameters of the amplifier in series with a multiplying digital-to-analog converter, which constitutes C_1 and C_2, schematized in Fig. 3.2. Indeed, once the voltage drop on R_s is measured, the current of amplitude I_0 flowing into it, hence in the device, can be evaluated. By activating one or the other channel, it is possible to get access separately to the voltage drop value on R_s or R_0. This allows the evaluation of the device resistance, thus the values of the parameters to set in C_1 and C_2 to balance the two fundamental amplitudes and to get an accurate signal differentiation, which guarantees a pure 3ω component. The acquired signal is digitized and the final value acquired is the root mean square voltage evaluated over $\sim$ 100 periods.
Since I_0 and R_0 are now known, it is possible to evaluate the amplitude of the AC power generated (Eq. 3.2) per unit of length (P_L):

$$P_L = \frac{I_0^2 R_0}{2L} \tag{3.15}$$

which is a key parameter for the final k_{th} evaluation. The same procedure is performed for seven different frequency values ranging from 1 Hz up to 1 kHz.

3.1.4 Device structure optimization

In this section, the optimization of the device stack to allow both room temperature (RT) and high temperature measurements is reported. Furthermore, the main results obtained on different conductive and dielectric layers integrated in state-of-the-art PCM will be presented.
At first, the electrode engineering is required to perform accurate thermal conductivity measurements. In particular, the tuning of w with respect to L is necessary to guarantee that the penetration depth of the generated thermal wave is large enough with respect to the heater width (1D heat propagation condition). Moreover, the choice of the electrode material plays an important role in 3ω devices, since its properties can tune the amplitude of the generated signal. In the next sections, these geometrical and material optimization aspects will be discussed in more details.

3.1.4.1 Electrode size optimization

The electrode design is fundamental in 3ω devices to ensure the validity of the theoretical model describing the thermal wave generated in the sample.
In this work, the electrode is characterized by a 2 mm length and a width ranging from 5 µm up to 50 µm. The optimal electrode size is chosen by comparing the thermal conductivity value of a material specimen for each width. For this aim, a Ge-rich GST (GGST) layer of both 100 nm and 200 nm, deposited on Si substrate and with a 25 nm SiN capping layer is used. The Au based electrode is deposited on the stack along with a thin 15 nm Ti layer as adhesion between the dielectric and the metal.
Before performing the standard 3ω measurements, the conformity of the metal deposition is verified by measuring the electrode resistance as a function of the width. As an example, the measurements performed on Au electrode (Fig. 3.6) shows that, as expected, the resistance decreases with the electrode width. In addition, the resistivity results independent from the electrode width, and assumes a constant value of $\sim$ 4.34 µΩ cm. This result is comparable with the median of the resistivity based on literature values and evaluated for the Ti/Au stack ($\sim$ 4.38 µΩ cm), confirming the conformity of the layer.
After the data acquisition, the k_{th} is evaluated by the four methods presented in Section 3.1.2. The results are reported in Table 3.1. The values associated to a 5 µm width are not reported since the generated signal amplitude in this condition is too high. In this case, the calibration of C_1, C_2 and D_1 had a significant impact on the error propagation, resulting in a low accuracy measure. Table 3.1 shows that k_{th} can assume slightly different values depending on the w used. The spread between the values measured on a 100 nm and a 200 nm thick GGST is more significant for a w of 10 µm. While both 20 µm and 50 µm show a more consistent k_{th} value when compared for the various thicknesses and models. Furthermore, the measure of the 50 µm width device showed that the amplitude of the acquired signal was quite small and too close to the instrument sensibility, compromising the accuracy of the final result.
In conclusion, this analysis demonstrated that the devices characterized by an electrode width of 20 µm are the optimal ones for the thermal conductivity measurements on our test bench.

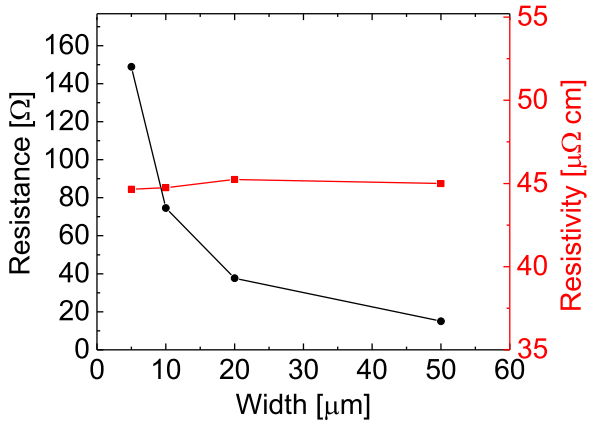

Fig. 3.6. Electrode resistance measurements as a function of its width. The data allows the evaluation of the electrode resistivity reported in red on the same plot. Since the resistivity assumes comparable values for different electrode sizes, it is possible to confirm the uniformity of the electrode deposition on the tested devices.

device		**M1**	**M2**	**M3**	**M4**	
w [μm]	t_{film} [nm]	k_{th} [$Wm^{-1}K^{-1}$]	k_{th} [$Wm^{-1}K^{-1}$]	k_{th} [$Wm^{-1}K^{-1}$]	k_{th} [$Wm^{-1}K^{-1}$]	R_i [$n\Omega$]
10	100	0.16	0.15	0.10	0.12	46
	200	0.13	0.12			
20	100	0.19	0.18	0.17	0.17	155
	200	0.18	0.17			
50	100	0.20	0.22	0.21	0.23	155
	200	0.21	0.22			

Table 3.1. Thermal conductivity evaluated with the four data analysis methods presented in Section 3.1.2. The measurements are performed on devices having L = 2 mm, w ranging from 10 μm to 50 μm, a conductive layer of 100 nm and 200 nm and an Au based electrode.

3.1.4.2 Electrode material optimization

The choice of the electrode material is fundamental to maximize the amplitude of the $V_{3\omega}$ signal generated. By combining Eq. 3.6, Eq. 3.7 and Eq. 3.15, $V_{3\omega}$ can be expressed as:

$$V_{3\omega} \propto I_0 R_0 \alpha P_l \propto I_0^3 R_0^2 \alpha = \left(\frac{V}{R_0 + R_s}\right)^3 R_0^2 \alpha \tag{3.16}$$

and defining $r_0 = R_0/R_s$:

$$V_{3\omega} \propto \alpha \frac{{r_0}^2}{(1+r_0)^3} \tag{3.17}$$

Therefore, $V_{3\omega}$ is dependent on the heater resistance R_0 (i.e,. its resistivity ρ, width w, thickness and length L) and on its temperature coefficient of resistance (α). The identification of the optimal electrode material relies on the characterization of the candidate metals, considering, in particular, both the resistivity and the temperature coefficient of resistance at room temperature. The obtained values are reported in Table 3.2 and

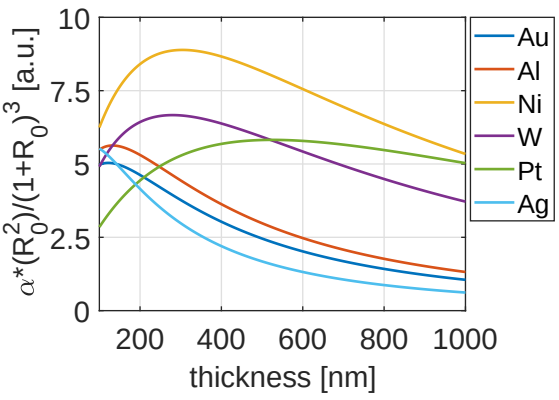

Fig. 3.7. Signal amplitude as a function of the metal thickness for L = 2 mm and w = 20 µm.

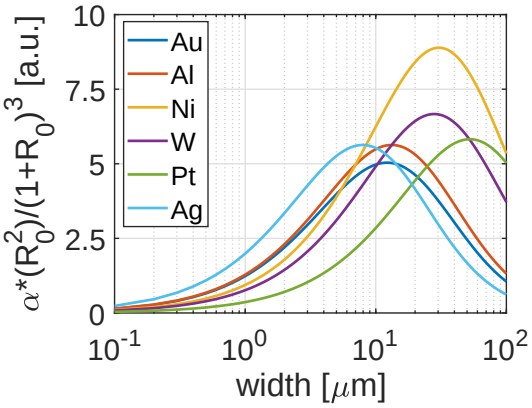

Fig. 3.8. Signal amplitude as a function of the metal width for L = 2 mm and a 200 nm thickness.

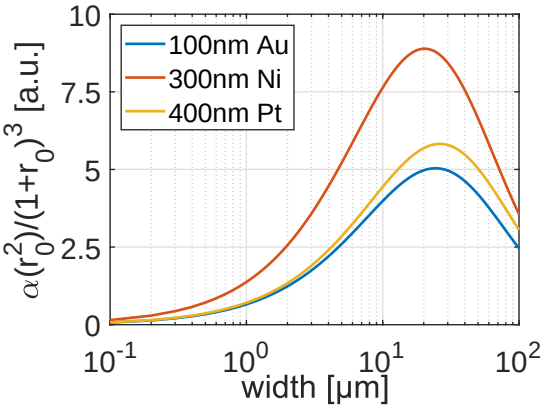

Fig. 3.9. Optimization of the signal amplitude for different heater metals characterized by w of 20 µm. The signal is maximized for 100 nm in Au, 300 nm in Ni and 400 nm in Pt.

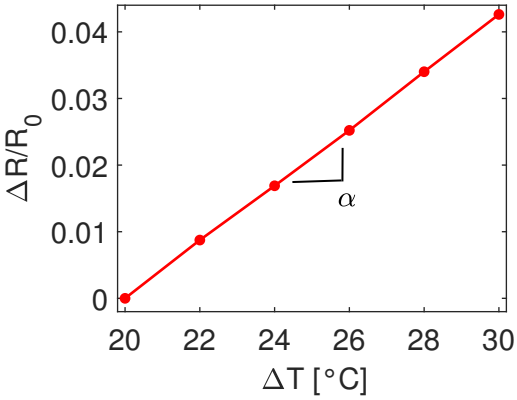

Fig. 3.10. Plot of $\Delta R/R_0$ as a function of ΔT used to extract the temperature coefficient of resistance (TCR) associated to the device tested.

they are plugged into Eq. 3.17 to estimate the expected signal amplitude. In particular, the dependency of the amplitude on the metal thickness and width, was characterized respectively, for a fixed width of 20 µm (Fig. 3.7) and thickness of 200 nm (Fig. 3.8). The materials available for deposition and featuring the best performance in terms of signal amplitude are Au, Ni and Pt. Therefore, their thickness was independently engineered to guarantee the maximal signal amplitude at $w = 20$ µm. As a result, the best electrode thicknesses result: 100 nm for Au, 300 nm for Ni and 400 nm for Pt based electrode.

The higher signal in the range of widths investigated is ensured by Ni based electrodes (Fig. 3.9). Therefore, it represents the material selected to perform the thermal conductivity measurements at room temperature.

material	ρ $[10^{-8}\ \Omega\ m]$	α $[10^{-3}\ K^{-1}]$
Au	2.44	3.4
Al	2.65	3.8
Ni	6.09	6.0
W	5.60	4.5
Pt	10.50	3.3
Ag	1.59	3.8

Table 3.2. Resistivity (ρ) and temperature coefficient of resistance (α) values at room temperature for different metals.

3.1.4.3 Characterization of the temperature coefficient of resistance

Combining the value reported in Table 3.2 with the trends in Fig. 3.7 and Fig. 3.8, it is evident that the temperature coefficient of resistance α has an important contribution to the signal amplitude: the higher it is, the higher the signal generated by the electrode. On the contrary, the resistivity has only a secondary contribution. For instance, Pt ($\alpha = 3.3\ 10^{-3}\ \mathrm{K}^{-1}$) has a signal amplitude comparable with those of Al and Ag (both having $\alpha = 3.8\ 10^{-3}\ \mathrm{K}^{-1}$), even if they show one order of magnitude difference in resistivity with respect to Pt (Table 3.2). As a consequence, the measure of the temperature coefficient of resistance is of relevant importance to guarantee an accurate thermal conductivity evaluation.
The direct evaluation of α is possible since it is defined as the variation in resistance (ΔR) induced in the metallic heater when the temperature is increased of 1 K (ΔT). It can be expressed as:

$$\alpha = \frac{1}{R_0}\frac{\Delta R}{\Delta T} \tag{3.18}$$

and it can be obtained experimentally by measuring the electrode resistance as a function of the temperature. With this aim, the device is placed on a hot chuck. A temperature range between 20 °C to 30 °C is considered for room temperature k_{th} measurements. The slope of the linear fit of $\Delta R/R_0$ as a function of ΔT gives the temperature coefficient of resistance value for the device/electrode tested. An example of this procedure is reported in Fig. 3.10 for the case of a Ni-based electrode, characterized by an $\alpha = 4.2 \cdot 10^{-3}\ \mathrm{K}^{-1}$ at room temperature.

3.1.5 Identification of the best workflow for k_{th} evaluation

The four methods presented in Section 3.1.2 will be here applied and compared to choose the most suitable for the thermal conductivity evaluation. The analysis is based on the GGST thermal conductivity measure. The calcogenide layer is capped with SiN, hence an SiN reference structure is also measured.
In Method 1 (M1), since the tested material is a conductive layer, the k_{th} of the SiN used as a reference is firstly evaluated. The amplitude of the temperature oscillation associated to the substrate plus film contribution is obtained plugging α, the device resistance (R_0) and the current amplitude (I_0) into Eq. 3.6 . The results are represented

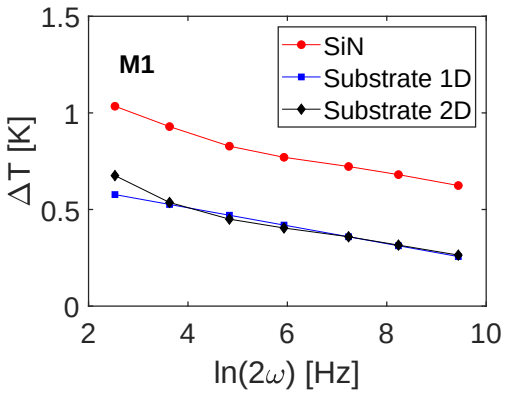

Fig. 3.11. Amplitude of the temperature oscillation (ΔT) measured on SiN as a function of the logarithm of the frequency and the simulated thermal response of the substrate considering both a 1D and 2D heat conduction across the device, used for method M1. In the 2D model, the coefficient of asymmetry of the k_{th} of the substrate is considered equal to 1.16.

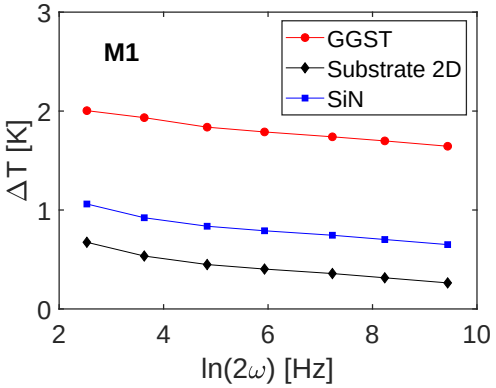

Fig. 3.12. Amplitude of the temperature oscillation measured on GGST (100 nm) as a function of the logarithm of the frequency and thermal response of the SiN and of the substrate (2D model) by using the k_{th} obtained by Fig. 3.11, used for method M1.

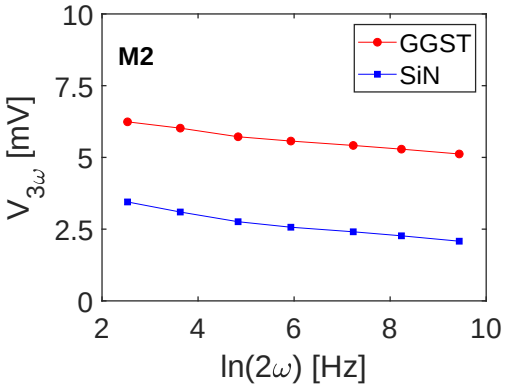

Fig. 3.13. Amplitude of the 3ω signal $V_{3\omega}$ measured on both GGST (100 nm) and SiN reference as a function of the logarithm of the frequency used for method M2. The k_{th} is evaluated by considering the difference between the two amplitudes. The direct evaluation of the amplitude of the temperature oscillation is not needed in this method.

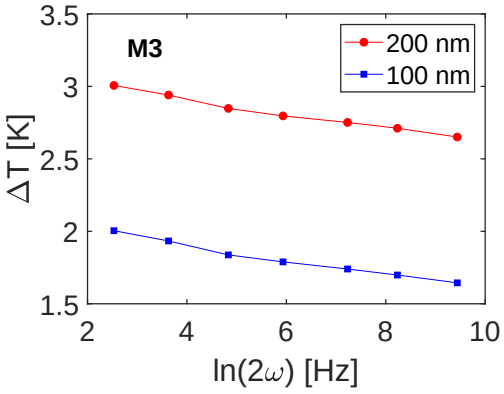

Fig. 3.14. Amplitude of the temperature oscillation measured on GGST (100 nm and 200 nm) as a function of the logarithm of the frequency used for method M3. The difference between the two signals is considered as the signal of a sample having the thickness equal to the one obtained by the difference of the two thicknesses measured (i.e., 100 nm in this case).

by the red values in Fig. 3.11. In the same plot it is also reported the theoretical value for the amplitude of temperature oscillation associated to the substrate contribution for both the 1D (Eq. 3.7) and 2D (Eq. 3.8) heat propagation conditions. In the 2D model a thermal conductivity anysotropy of 1.16 is considered in the Si substrate [130]. It is evident that the 2D model is the more accurate among the two, since it correctly describe the signal response at small frequencies. In these conditions, indeed, the penetration depth is too high with respect to the substrate thickness therefore the condition of a 1D heat propagation along the thickness of the sample does not hold. It results in

a linearity rupture taking place in the ΔT increase with the logarithm of the frequency. Therefore, the 2D heat conduction model is the one selected and used for the analysis in the following part of this work. The $k_{th,SiN}$ value obtained is then plugged in Eq. 3.10 to model the SiN contribution to the temperature oscillation. The obtained values are reported in Fig. 3.12 along with the temperature oscillation of the GGST sample which was evaluated according to Eq. 3.6. In M1, the standard deviation associated to the final thermal conductivity value is affected by a double error propagation: the first associated to the $k_{th,SiN}$ and the second related to the final $k_{th,GGST}$ evaluation, which impacts significantly the accuracy of the extrapolated value with this method.
In Method 2 (M2), instead, the GGST thermal conductivity can be directly measured from the $V_{3\omega}$ signals without evaluating the temperature amplitude generated in the sample. Eq. 3.12 was used to evaluate the thermal conductivity directly from the signal acquired and reported in Fig. 3.13 for both the GGST and the reference.
In Methods 3 and 4 (M3 and M4), two set of measurements are required but here they are referred to GGST devices having a different thickness (100 nm and 200 nm in this case). Therefore, the input power used to perform the test should be the same in both devices in order to have a reliable comparison. The amplitude of the temperature oscillation were evaluated and reported in Fig. 3.14. Eq. 3.13 was used for the $k_{th,GGST}$ evaluation associated to a layer having a thickness equal to the difference between the thicknesses of the two layers measured (i.e., 100 nm).
According to M4, instead, the GGST effective thermal conductivity was evaluated, as in M1; then, the final k_{th} was extracted from a linear interpolation of the thermal resistance as a function of the two GGST thicknesses (100 and 200 nm), as presented in Section 3.1.2.
The four methods under investigation are compared analyzing the GGST thermal conductivity mean value and the associated dispersion ($\sigma_{k_{th}}$) for each one of them. The results are reported in Fig. 3.15 and Fig. 3.16. The standard deviation on the final k_{th} value is obtained by the use of the propagation of uncertainty based on the 0.2 mV sensitivity of the generator and a 10% error associated to the length L and the oxide thickness value. The uncertainty on the other quantities is considered negligible.
As shown in Fig. 3.15, the k_{th} values obtained by the use of the four methods are compatible and distributed around 0.18 $Wm^{-1}K^{-1}$. It is interesting to note that the result obtained with M4 is fully compatible with the other values, even if it is obtained with a linear interpolation of just two points, making it not statistically valuable since no standard deviation can be associated to it.
A resume of the four methods is reported in Table 3.3. It shows that M1 and M3 are the less accurate because of their higher coefficient of variation (CV), with respect to M2. For M1, the main contribution to the CV comes from the preliminary evaluation of the substrate k_{th}, which adds a further step to the error propagation. In M3, instead, the higher uncertainty is related to the intrinsic error introduced by performing two different GGST measurements. Method 2 shows the lowest standard deviation and CV: 0.02 $Wm^{-1}K^{-1}$ and 6%, respectively. This is because the k_{th} is calculated directly from the 3ω signal acquired, avoiding the error contribution related to the use of different combined measurements and data analysis steps. Therefore, M2 represents the most accurate method.
Finally, M4 can be further optimized measuring GGST layers with higher thicknesses,

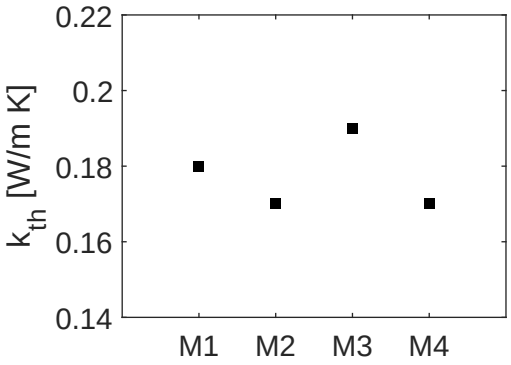

Fig. 3.15. Thermal conductivity mean values calculated with the different 3ω methods presented.

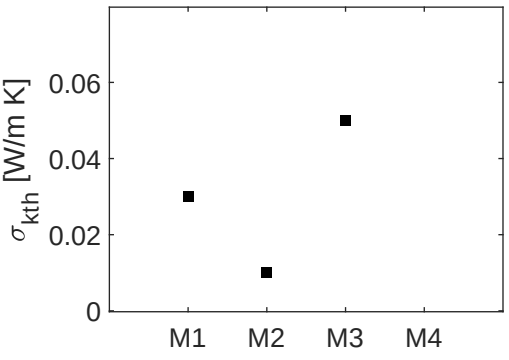

Fig. 3.16. Representation of the error ($\sigma_{k_{th}}$) for the different methods presented. M4 does not have an associated error because the k_{kth} comes from a linear interpolation done on only two points.

which increases the number of points used in the linear interpolation and hence ensures a more accurate estimation of k_{th} (in particular thanks to the removal of the interfacial resistances contribution) and to associate a standard deviation to its value. As a consequence, M4 can be considered the best one if more than two thickness values are used to determine the material properties. This is the method used to evaluate the thermal conductivity of the dielectric layers reported in the next section.

Method	Input measurements	Data Analysis step	k_{th} $[Wm^{-1}K^{-1}]$	CV [%]
M1	2	2	0.18 ± 0.03	16
M2	2	1	0.17 ± 0.01	6
M3	2	1	0.19 ± 0.05	26
M4	2	2	0.17	-*

Table 3.3. Comparison among the four methods investigated, highlighting that M2 is the most accurate method.
* A CV can be assigned when more than two thicknesses values are considered.

3.1.6 Measurement at room temperature

The 3ω measurements at room temperature were performed on different dielectric and conductive layers used in PCM.

Measurements on dielectric materials

In the framework of the development of low power PCM devices, the investigation of dielectrics characterized by a low thermal conductivity contribute to the improvement of the thermal performance of the device. The most common low thermal conductivity dielectric materials are: SiO_2 (1.4 $Wm^{-1}K^{-1}$), SiN (1.05 $Wm^{-1}K^{-1}$) and

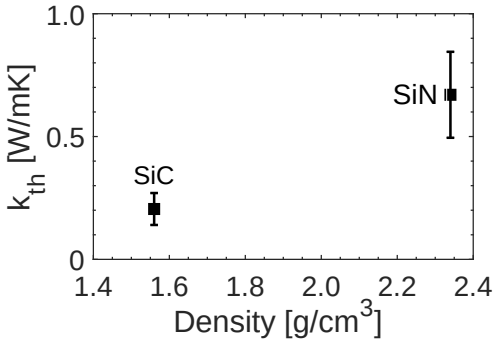

Fig. 3.17. Thermal conductivity of SiN and SiC as a function of their density.

SiC (0.3 $Wm^{-1}K^{-1}$). In general, SiN is used to encapsulate the PCM. Nevertheless, SiC is also compatible with the PCM integration process. In addition, the k_{th} can be further adapted by tuning the material properties, for example by modulating the material density or doping the material itself, the amount of defects will increase, reducing its thermal conductivity.
In this work, improved SiN and SiC encapsulation layers, resulting from an optimized fabrication process, will be integrated in a Wall-based PCM to compare their performances. Their k_{th} characterization can guarantee a more reliable electro-thermal modeling of the cell as well as can support a better understanding of the electrical performance of these devices.
The tuned SiC and SiN based layers were measured by X-Ray Reflectometry (XRR) technique for the evaluation of the layer density and by 3ω method to obtain their thermal conductivity value. The thermal conductivity measurements were performed on SiC and SiN layer having a thickness of 100 nm and 200 nm. The k_{th} values obtained are reported in Fig. 3.17. Interestingly, the engineered SiC layer presents a lower density than the SiN one. As a result, its thermal conductivity is accordingly lower, assuming a value $\sim$ 70% lower than in SiN.

Measurements on GST and GGST

The materials integrated as active layers in the PCM devices investigated in this work are, instead, GST and GGST. The thermal conductivity of a chalcogenide material is temperature dependent due to the phase transition, therefore its value at room temperature depends on the phase of the material (i.e., on the maximum temperature of the fabrication process used). In the device analyzed in this section, the electrode is deposited with a high temperature process (T $\sim$ 300 °C), therefore the thermal conductivity measurements at RT for GST ($T_c \sim$ 150 °C) and GGST ($T_c \sim$ 370 °C) are referred to the crystalline GST and amorphous GGST, respectively.
The measurements are performed for four thicknesses (i.e., 100 nm, 200 nm, 300 nm and 400 nm) of both a GST and a GGST layer deposited on a Si substrate and with a 25 nm capping layer.
The GST thermal conductivity was already widely studied in the literature. Nevertheless, its evaluation can allow a more accurate simulation of the PCM device fabricated in our laboratory. For fcc-crystalline GST, the measured value is of $0.56 \pm 0.03\, Wm^{-1}K^{-1}$, compatibly with the results previously reported in literature $\sim 0.50 \pm 0.03\, Wm^{-1}K^{-1}$ [48]).

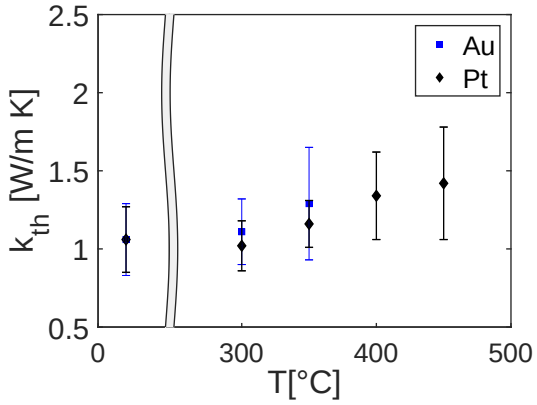

Fig. 3.18. Thermal conductivity of SiN in temperature for different heaters: Au, Pt. Pt allows the acquisition of the signal up to 450 °C, while Au only up to 350 °C.

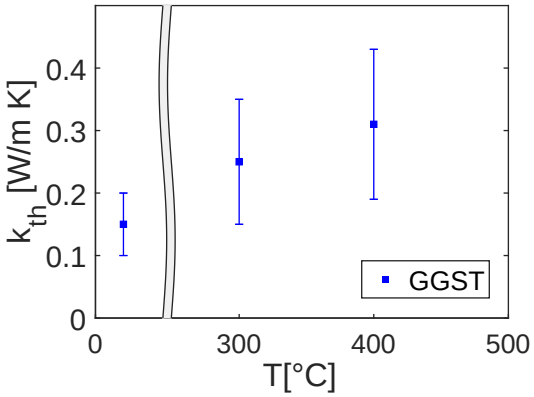

Fig. 3.19. Thermal conductivity of GGST in temperature using Pt as metal for the heater.

The thermal conductivity value of GGST, instead, has not been proposed yet. The measured value is of 0.30 ± 0.03 $Wm^{-1}K^{-1}$. The lower value obtained for GGST with respect to GST is not surprising. Indeed, differently than GST, GGST is in the amorphous phase.

In conclusion, all the parameters acquired for the characterization of the dielectric and chalcogenide materials at RT are summarized in the following Table 3.4:

material	k_{th} $[Wm^{-1}K^{-1}]$	σ_{th} $[Wm^{-1}K^{-1}]$
SiN	1.39	0.12
SiC	0.41	0.05
GGST	0.30	0.03
GST	0.56	0.03

Table 3.4. Thermal conductivity (k_{th}) and standard deviation (σ_{th}) for the four materials tested at room temperature.

3.1.7 Results at high temperature

The thermal conductivity of phase-change materials undergoes a one order of magnitude variation when the temperature is increased up to 400 °C. The phase transformation induces a strong change in the electro-thermal performance of the device.
Given the importance to estimate the material k_{th} as a function of temperature, the test bench must be adapted and validated for high temperature measurements. In particular, a hot chuck is installed to guarantee a homogeneous heating of the device as well as an accurate temperature control. Furthermore, the electrode reliability under high-temperatures conditions (up to 450 °C) will be investigated, testing the three different electrodes previously selected (Au, Ni, Pt) for the measurement of the SiN

thermal conductivity. As shown in Fig. 3.18, Pt resulted the only electrode allowing the signal acquisition up to 450 °C. Indeed, Ni faces delamination when a temperature higher than 350 °C is reached, while in Au the signal to noise ratio get highly reduced, making the measurements less reliable at the same temperature. In particular, the signal in the Au based electrode was unstable and the voltage amplitude measured was of the order of 300 μV, which corresponds to the instrument sensitivity.
It is worth to notice that the Au signal could not be further optimized by tuning its thickness. In fact, Fig. 3.7 shows that it reaches the plateau of maximum signal at 200 nm, which is the thickness integrated in our devices. The low signal to noise ratio observed in Au with respect to the other electrodes is in accordance with its lower signal amplitude predicted in Fig. 3.9. The Pt performances are expected since it is a material characterized by a high melting temperature and resistance to oxidation [131].
The result can be further explained by comparing the coefficient of thermal expansion (β) of the Ti layer used as adherence between the electrode and the tested material, and the electrode itself. The values of the coefficient of thermal expansion for the three electrodes investigated, reported in Table 3.5, show that the value of the coefficient is the same for Pt and Ti, while a mismatch is reported for the other two electrodes with respect to Ti. As a result, using a metal having the same thermal stress as Ti represents a key factor to avoid delamination and to favor the signal acquisition at high temperatures.
Once the bench was validated with the measure of the SiN thermal conductivity at high

material	β $[10^{-6}\ K^{-1}]$
Ti	9
Ni	13
Au	14
Pt	9

Table 3.5. coefficient of thermal expansion (β) found in literature for the different metals used as electrodes

temperatures, the same experimental settings were used to test chalcogenides materials. First, we checked the possibility to measure the k_{th} of GGST up to 450 °C. Fig. 3.19 reports the measurements performed on 3ω devices based on a 200 nm thick GGST layer integrated with a Pt heater deposited at room temperature, ensuring both materials to be in the amorphous phase. This time it was possible to acquire the signal up to 400 °C (see Fig. 3.19). At higher temperatures, since the material is getting closer to its crystallization temperature, it is subjected to a volume variation. This induces some mechanical stress on the heater, making the measurements less reliable (i.e., the acquired signal is unstable and it does not obey the theoretical model anymore.
The measures reported in Fig. 3.19 shows an increase of k_{th} from $\sim 0.15\ Wm^{-1}K^{-1}$ at room temperature up to $\sim 0.3\ Wm^{-1}K^{-1}$ at 400 °C . This trend is compatible with the k_{th} increase already reported in literature for other chalcogenide materials (in GST it increases from $\sim 0.2\ Wm^{-1}K^{-1}$ in the amorphous phase to $\sim 0.5\ Wm^{-1}K^{-1}$ in the fcc-crystalline one [47] [48].

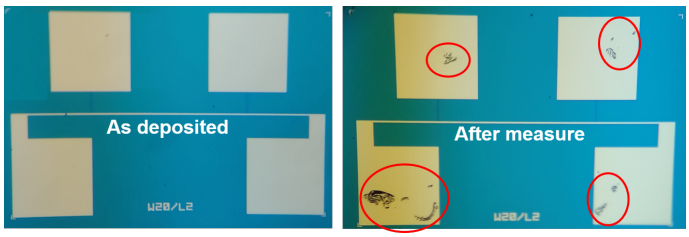

Fig. 3.20. Electrode appearance before (as deposited) and after measurement in SiO_2 based devices. The red circle evidences the effect of the local delamination taking place after measure.

The same phenomenon is observed on GST based devices. However, due to the lower crystallization temperature of GST with respect to GGST, it was not possible to get a reliable signal already at 150 °C.
A further possibility to optimize the system is represented by the engineering of the material used as a capping layer of the tested chalcogenide. This approach relies on improving the adhesion between the target layer and the electrode through the integration of new dielectric materials, as discussed in the next section.

3.1.7.1 Dielectric layer engineering

In the framework of the capping layer optimization, SiO_2 and GeN were explored since both are compatible with chalcogenides and typically show good adherence with them. The two candidate dielectrics were compared by measuring the thermal conductivity of both GST and GGST in temperature. The signal generated in SiO_2 based devices was unstable and local delamination occurred in the surrounding of the probe position, as can be observed in Fig. 3.20. Therefore SiO_2 cannot be considered a good candidate for 3ω measurements. Differently than SiO_2, the GeN capping-based devices demonstrated good adherence with both the chalcogenide layers.
The thermal conductivity of both GST and GGST was measured at room temperature and after annealing at 450 °C to trigger possible effects on the electrode. The results are summarized in Table 3.6.
In addition, the thermal conductivity evolution in temperature was tested on a 300 nm

T [$°C$]	**GST** [$Wm^{-1}K^{-1}$]	**GGST** [$Wm^{-1}K^{-1}$]
Room temperature	0.17 ± 0.01	0.27 ± 0.01
After annealing at 450 °C	0.95 ± 0.15	0.46 ± 0.04

Table 3.6. Thermal conductivity of both GST and GGST at room temperature and after annealing at 450 °C, measured with 3ω devices capped with GeN.

thick GST device. The measured values are reported in Table 3.7. The unstable signal measured at 150 °C was directly related to the material transition from the amorphous to the fcc-crystalline phase. Interestingly, once the temperature was beyond the sample crystallization temperature, it was again possible to acquire the signal, as demonstrated by the k_{th} measure at 250 °C. Nevertheless, the signal became again unstable at a temperature of 350 °C, which coincides with the temperature at which the transition from

T [$°C$]	**GST** [$Wm^{-1}K^{-1}$]
RT	0.17 ± 0.01
150	unstable signal
250	1.15 ± 0.16
350	unstable signal
Back to RT	0.27 ± 0.02

Table 3.7. GST thermal conductivity in temperature obtained for a 300 nm thick GST layer and a GeN capping layer, demonstrating the possibility to measure the thermal conductivity of a chalcogenide material in temperature apart from the specific temperature range where the change of phase is taking place (i.e., 150 °C and 350 °C for GST (Fig. 1.20)

fcc-crystalline to hcp-crystalline phase happens. The two transition temperatures are comparable with the values reported in literature [47, 48]. Furthermore, when the device is cooled down from 350 °C to room temperature, it was again possible to acquire the signal and to estimate the k_{th} value. Notably, the value after cooling is lower than the one obtained on the material as deposited. This trend is in accordance with literature [48].
In conclusion, the GeN based device allows the k_{th} measure of the electrical conductivity in temperature, exept for the region corresponding to the phase transition. This prevents the detection of the thermal conductivity variation during the change of phase. However, this problem can be attenuated by waiting a sufficient amount of time to make the crystallization mechanism stable before signal acquisition.

3.2 Thermal conductivity measurements by MPTR

3.2.1 Method description

The modulated photo-thermal radiometry enables the evaluation of the thermal conductivity by the measure of the infrared radiation emitted by the surface of a sample excited by an external photo-thermal source. The method was firstly proposed by Cowan [132] and then developed by Nordal [133]. According to the method, the infrared radiation generated by a material can be expressed by the Stefan Boltzmann law:

$$M = \epsilon\sigma T^4 \tag{3.19}$$

$$T = \Delta T + T_0 \tag{3.20}$$

where ϵ is the material emissivity, σ is the constant of Stefan Boltzman, ΔT the temperature induced in the system due to the external excitation and T_0 the initial temperature of the sample.
In order to simplify the thermal conductivity evaluation, the ΔT is kept significantly small (of the order of few K), so that the variation of emittance can be expressed as a linear function of the temperature variation induced in the material:

$$\Delta M = 4\epsilon\sigma T_0^3 \Delta T \tag{3.21}$$

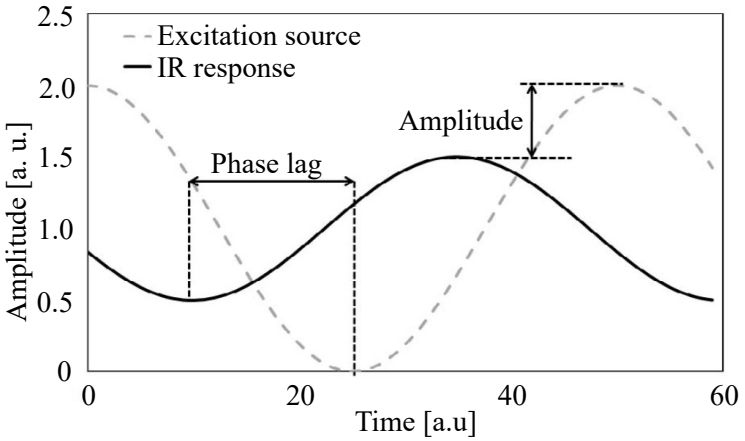

Fig. 3.21. Example of the amplitude and phase variation of the emitted beam with respect to the excitation one.

In the experimental set-up, a laser beam (radius $\sim$ 1mm) generates a uniform heating of the excited area. The thermal radiation emitted is measured and converted in an electric signal, which is characterized by a low signal/noise ratio due to its small amplitude. Therefore, in MPTR, the analysis is always performed in the frequency domain. The amplitude and phase of both the excitation source and the infrared radiation emitted by the sample are measured with a lock-in amplifier. The result of a typical measurement is reported in Fig. 3.21. The measurements are performed in a high frequency domain ($\geq$ 1 kHz) where the thermal wave penetration depth is negligible with respect to the radius of the excited region (e.g., penetration depth of 50 μm for a frequency of 1 kHz) therefore a 1D heat transfer model can be assumed. Nevertheless, when the tested sample features a submicrometric thickness, the photon flux absorption can go beyond the surface of the sample. In addition, if the material is tested at high temperature, it can face phenomena such as evaporation or oxidation. As a consequence, the characterization of submicrometric layer as a function of temperature requires the deposition of a metallic layer on top of the material under test. This metallic layer acts as an optical transducer by converting the photon flux in a heat flux. The integrated optical transducer needs to satisfy different conditions, such as: stability at high temperatures, low reflectivity with respect to the laser beam and proper emissivity. Furthermore, its thickness need to be smaller than i) the thickness of the tested material and ii) the penetration depth. For this reason, the most suitable materials are the noble metals.
The MPTR set-up for the thermal conductivity characterization in temperature is reported in Fig. 3.22. The amplitude of a laser beam used as an excitation source is modulated in amplitude with an acousto-optic modulator (AOM) in a frequency range between Hz and MHz. The modulated signal impinges the device placed on a sample holder under a controlled atmospheric condition to avoid possible material deterioration. The infrared signal emitted by the sample is collected and focused via a multiple-mirrors system to an infrared detector. At the same time, the signal coming out from the acousto-optic modulator is measured with a photodiode (PD detector in Fig. 3.22) and it is used as a reference for the evaluation of both amplitude and phase. A combination of a mathematical model with experimental data allows the calculation of the

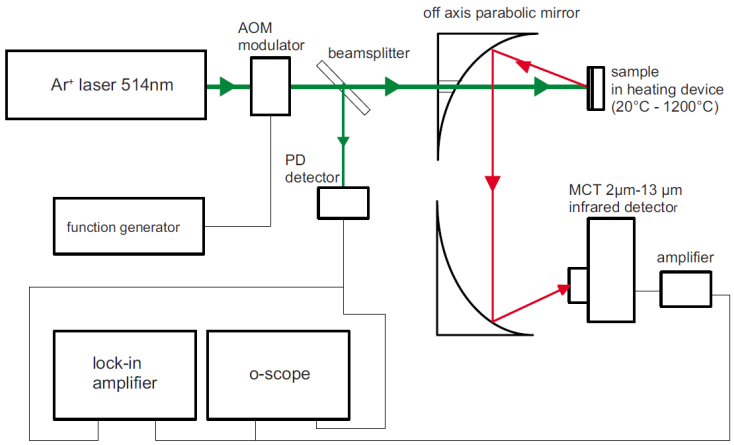

Fig. 3.22. Schematic representation of the Modulated Photothermal Radiometry bench test [48].

thermal resistance for devices having different sample thicknesses, hence of the thermal conductivity. It is performed by matching the experimental data (amplitude and phase of the emitted signal) with a theoretical model thorough the Levenberg-Marquard algoritm [134] [135].
The main limitation of the MPTR technique is that it can be applied only to materials that can absorb an optical excitation. Furthermore, the need of an optical transducer, introduces an additional thermal resistance which needs to be taken into account in the theoretical model, increasing its complexity. As a plus, the emitted radiation is dependent on the device roughness, which need to be properly controlled.
Since the sample used to perform MPTR measurements is made up of a substrate, the layer to be measured and an electrode, the evaluation of the thermal conductivity is extracted by measuring devices with different thicknesses. This allow the evaluation of both the k_{th} value and the interface resistances contribution by making use of the method M4, already presented in Section 3.1.2.

3.2.2 Measurements on GST and GGST

Within the framework of a collaboration with the Institut de Mecanique et d' Ingenierie (I2M) de Bordeaux, measurements on GGST were performed for temperature up to 500 °C using the MPTR test bench developed by Battaglia et al. [48].
The device structure for MPTR is made up of a GGST layer of variable thicknesses (from 100 nm to 400 nm) deposited on a Si substrate and capped with a Pt electrode. Unlike the 3ω method, in MPTR the electrode does not require any specific patterning and it is deposited at room temperature. The same samples along with GST based ones, were also tested at the Laboratoire National de Metrologie et d'essais (LNE) in Paris to measure their thermal conductivity at RT, 450 °C and after cooling the samples back to RT.
The aim of the test was to evaluate the evolution of the GGST k_{th} in temperature, not yet known in literature, with the use of validated test benches. These results can further serve as a reference to validate the 3ω test bench developed in our laboratory at CEA-LETI.

3.2.2.1 Measurements at I2M in Bordeaux

The thermal conductivity of GGST is measured by testing four thicknesses: 100 nm, 200 nm, 300 nm and 400 nm. The measurements are performed in the frequency range going from $\sim$ 800 Hz up to $\sim$ 5 kHz. The temperature was, instead, measured in 12 points between 50 °C and 500 °C and back to room temperature with an heating rate of 25 °C/min. For each temperature point, the linear regression of the thermal resistance (R_{th}) as a function of the material thickness allowed the evaluation of the thermal conductivity. The standard deviation associated to the thermal conductivity value is obtained as the statistical error on the slope on the linear fit. The k_{th} value at room temperature resulted to be of 0.30 $\pm$ 0.03 $Wm^{-1}K^{-1}$. Its value increases up to 1.22 $\pm$ 0.16 $Wm^{-1}K^{-1}$ at 500 °C.

3.2.2.2 Measurements at LNE in Paris

Both GGST and GST based samples, integrating the four thicknesses were measured at the LNE in Paris. A value of 0.16 $Wm^{-1}K^{-1}$ was obtained for GST samples and 0.30 $Wm^{-1}K^{-1}$ for GGST at room temperature. The samples were heated up to 450 °C with an heating rate of 10 °C/min. At 450 °C, GST presented a thermal conductivity of 1.45 $Wm^{-1}K^{-1}$, while GGST of 0.84 $Wm^{-1}K^{-1}$, revealing the higher degree of crystallization reached in GST at this temperature. The value assumed after annealing (i.e., back to RT) is instead of 0.85 $Wm^{-1}K^{-1}$ for GST samples and of 0.70 $Wm^{-1}K^{-1}$ for GGST. The reported decrease in the thermal conductivity value is in accordance with the trend already presented in literature for chalcogenide materials (Fig. 1.20).

3.3 3ω method vs MPTR results comparison

The thermal conductivity of both GST and GGST were measured as a function of temperature by the use of different techniques and measurements protocols. At first, to support the results discussion, it is relevant to point out the main differences between the experimental workflows. In particular, the measurements at I2M were performed from RT up to 500 °C with an heating rate of 25 °C/min; at LNE, instead, the k_{th} was first evaluated at room temperature, than at 450 °C and finally after annealing, with an heating rate of 10 °C/min; in LETI, the measurements were performed before and after annealing at 450 °C , with an heating rate of 40 °C/min. The results for both GST and GGST are summarized respectively in Fig. 3.23 and Fig. 3.24.
The measurements performed for GST at LETI and LNE are reported in Fig. 3.23 where they are compared with literature. The values obtained for the as deposited samples are in line with literature. Furthermore, the measures performed after annealing at 450 °C both at LETI and at LNE provide comparable results. Nevertheless, this value diverges from literature. This difference can be ascribed to the different experimental condition, more precisely to the maximum temperature and cooling rate used.
The measurements performed on GGST in the three laboratories are instead reported in Fig. 3.24. The temperature dependent k_{th} measurements performed at I2M highlight the presence of a phase transition between 400 °C and 450 °C, in accordance with

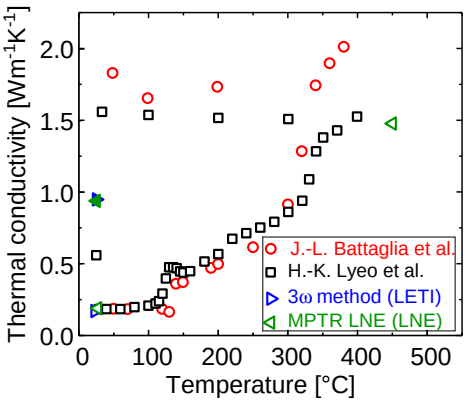

Fig. 3.23. Comparison of the GST thermal conductivity values measured in LETI and at LNE with literature (Lyceo et al. [47] and Battaglia et al. [48]). The filled traingles represents the values obtained after annealing at 450 °C.

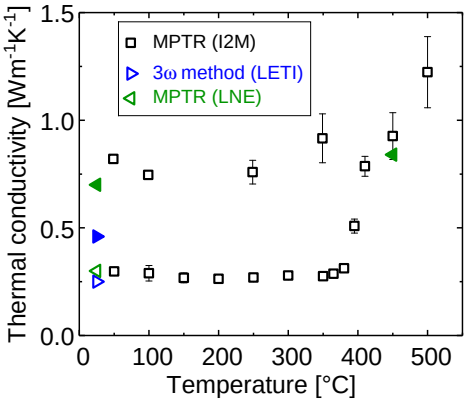

Fig. 3.24. GGST thermal conductivity values measured in the different laboratories as a function of temperature. The filled traingles represents the values obtained after annealing at 450 °C.

the GGST crystallization temperature [42]. The larger errorbar associated to the k_{th} values between 400 °C and 500 °C is linked to the slightly different shape of the R_{th} vs temperature curve during the crystallization for the different thicknesses analyzed.
The measurements performed by MPTR in the two laboratories are compatible, while an evident mismatch in the k_{th} after annealing is evidenced for the device measured in LETI. This can be explained by the different heating rate used to perform the annealing: the faster ramp used at LETI provides a shorter time with respect to the other protocols for the material to arrange in a crystalline structure. To be noted that the same phenomenon does not occour for the GST based devices because its crystallization temperature ($\sim$ 150 °C) is smaller with respect to the annealing temperature used.
In conclusion, the comparable results obtained by different methods allowed to validate the LETI test bench. The comparison between the methods further evidences the importance to use the same heating rate to ensure that the chalcogenide material is in the same phase and have the same k_{th} value.

3.4 Chapter summary

In this chapter, the workflow for thermal conductivity measurements on different PCM components were discussed. In particular, the implementation and optimization of an experimental setup for 3ω thermal conductivity measurements at room temperature and high temperatures was described. At first, the electrode design and material properties were investigated to achieve the optimal data acquisition and to ensure the best signal to noise ratio. As a result, a 2 mm long and a 20 µm wide Nickel electrode was selected for room temperature measurements.
However, Ni electrode faces delamination at 350 °C, therefore the electrode was further optimized to guarantee the material characterization at high temperature and Platinum was identified as the most suitable material for this application.
Furthermore, the device stack was modified to deal with the instability arising during the characterization of chalcogenide materials for temperatures beyond the crystal-

lization one. Notably, the SiN capping layer was replaced by GeN. Unlike SiN, GeN showed a better adherence with chacogenides at high temperature and avoided the metal delamination, ensuring a stable signal even beyond the material crystallization temperature.
Four published methods for thermal conductivity evaluation were also compared. The study showed that the most promising method is based on the interpolation of the thermal resistance as a function of the material thickness. This allow to get rid of the interface thermal resistances contribution from the final thermal conductivity value.
The thermal conductivity of GST and GGST as well as of dielectric materials was measured. The test bench in LETI was validated comparing the obtained k_{th} results with those measured on the same devices by MPTR on established test bench. Nevertheless, the comparison pointed out that 3ω signals were unstable in correspondence of the phase transition. However, this limitation can be overcome by introducing a waiting time for the crystallization mechanism to stabilize before performing the signal acquisition.
In conclusion, the optimization and validation of a 3ω setup in LETI can open the possibility for testing novel candidate dielectric or chalcogenide materials to be integrated in the next generation PCM devices. Furthermore, an accurate k_{th} value can support a reliable numerical simulation of the electro-thermal phenomena in the PCM device and can support the interpretation of electrical testing on the devices, as will be described in the next chapter(s).

Chapter 4

Electro-thermal simulations

The main advancements in the optimization of the PCM device targeting low-power applications are based on the numerical simulation of the PCM cell behavior. Indeed, the investigation of the temperature profile generated in a memory at a specific applied current is very informative to determine the main sources of heat losses inside it, as presented in most of the study reported in Ch. 2.
In this chapter, a numerical study of the electro-thermal behavior of the state-of-art Wall-based PCM devices will be presented. At first, the simulation tool will be described. Then, different models will be discussed for the description of the thermal and electrical conductivity behavior as a function of temperature. Importantly, the thermal conductivity values, experimentally measured as discussed in the previous chapter, were included to provide a more accurate description of the PCM thermal behavior. Furthermore, the geometrical and material properties of the heater and adjacent dielectrics were investigated, allowing to identify the main features influencing the PCM performance as well as to propose the guidelines for the fabrication of the next generation low-power Wall-based Phase-Change Memories.

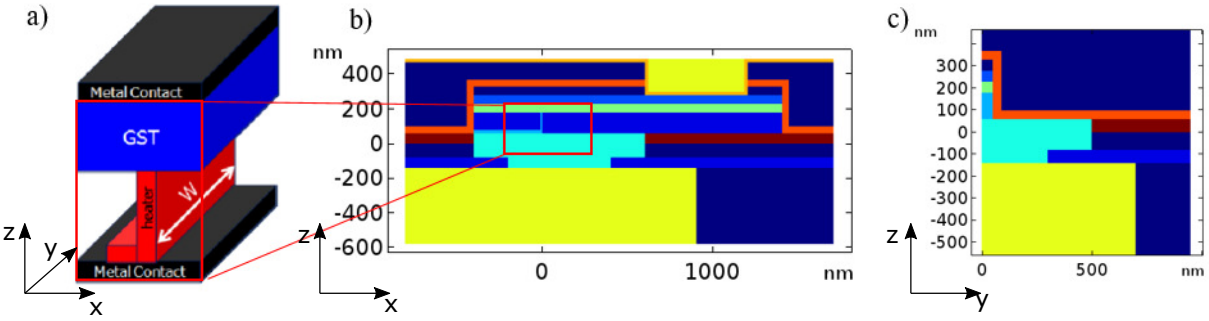

Fig. 4.1. Schematic of a) the 3D structure of the Wall-based PCM [81] and a section b) perpendicular and c) parallel to the width of the heater of the structure simulated with COMSOL Multiphysics.

4.1 Geometry and mesh

In Ch.2, the heater-based Wall structure (Fig. 4.1a) was presented as the state-of-the-art PCM architecture, featuring the best trade-off between process integration and performance. Therefore, this structure was chosen as the architecture of interest for the simulation of the electro-thermal phenomena described in this chapter as well as for the electrical characterization presented in Ch. 5.
The simulated structure consists of a cube including the entire device stack limited by the bottom and top electrode contacts, which is integrated between the Metal 4 (M4) and the Metal 5 (M5) layer. The xz and yz planes of the simulated 3D structure are reported in Fig. 4.1a and Fig. 4.1c). Since the heater of the Wall-based PCM has width $w = 80$ nm, height $h = 120$ nm and thickness $t = 10$ nm (see Fig. 4.1), it cannot be considered as semi-infinite, therefore, an accurate modeling of the performance can be ensured only by 3D simulations. Nevertheless, this PCM architecture is symmetrical with respect to the xz plane located at half of the heater width, enabling to investigate only half of the structures and leading to a reduction of the computation time.
Following the device geometry settings, the mesh was defined to support the geometry spacial discretization into elements over which the equations are solved. The mesh-size was defined as a trade-off between the result resolution and the computation time. Furthermore, there is a minimum number of meshing points to be defined to ensure an accurate convergence as well as a reliable result, especially for the domains with high aspect ratio (e.g. heater): generally, the smaller side of the high aspect ratio domains should be meshed with at least a mesh point every one fifth of its length. Given the variety of blocks size and aspect ratio in a Wall-based PCM, the mesh is engineered as a function of both their size and the distance from the active region where the core of the physics is taking place: first of all, the heater was manually meshed using the minimum mesh size; after that, all the materials in contact with it were meshed with an automatic *finer* option in the solver, which generated a maximum element size of 13 nm. In the M4 electrode only a few mesh points were defined, since it is both far from the active layer and has a large volume (1700 nm x 1400 nm x 440 nm) with respect to all the other features of the memory. Furthermore, it should be noticed that the mismatch between the maximum mesh size between two adjacent domains, was automatically adjusted by the simulation tool, creating a gradient between the two. Following this procedure, the whole geometry was meshed resulting in domains having

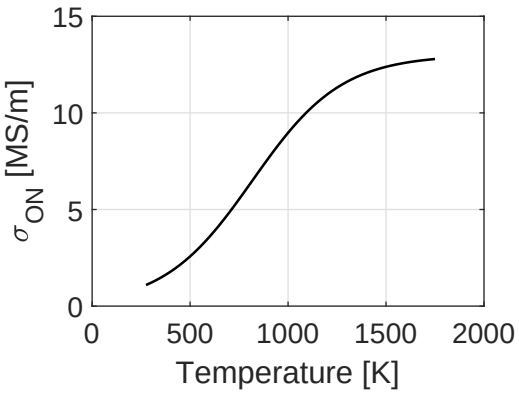

Fig. 4.2. Profile of the electrical conductivity as a function of temperature, used to simulate the behavior of the cell during the first step of the study, which corresponds to the programming of the cell (*write* operation).

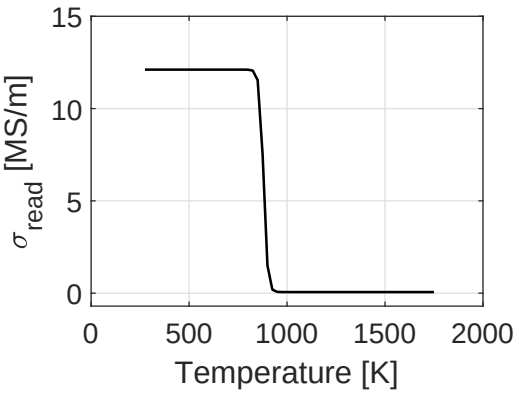

Fig. 4.3. Plot of the electrical conductivity as a function of temperature model, used in the second step of the simulation study, which corresponds to the reading operation.

sizes in between 2 nm and 67 nm.

4.2 Stationary electro-thermal model

The temperature distribution generated in the device as a result of the application of an electric pulse can be evaluated by solving a coupled system of partial differential equations, describing the electro-thermal phenomena in the device. These include the current conservation equation (Eq. 4.1) and the stationary heat transfer equation (Eq. 4.2):

$$\nabla \cdot \vec{J} = 0 \tag{4.1}$$

$$\nabla \cdot (-k_{th} \nabla T) = \frac{J^2}{\sigma} \tag{4.2}$$

The simulation study was divided in two steps: at first, the equations were solved to get the temperature achieved in the memory when a specific current density is applied to perform the *write* operation; then, the obtained temperature profile was used as input to estimate the final resistance of the device, when a low voltage pulse ($V_{read} = 0.1$ V) is used to read the resistance state (*read* operation). Both studies were performed by considering:

- a plane of symmetry parallel to the xz plane in the middle of the Wall width (y = 0, see Fig. 4.1);

- Dirichlet boundary conditions (i.e., V = 0 and T = 273.15 K) for the top and bottom electrode interface;

- Neumann boundary condition on both electrical potential and temperature for all the lateral interfaces, to account for both electrical and thermal insulation of the system.

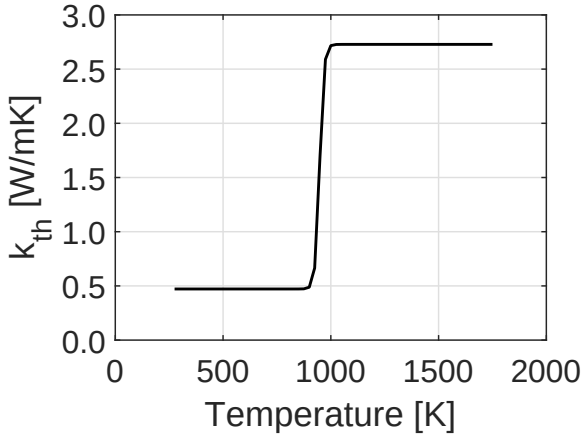

Fig. 4.4. Profile of the thermal conductivity model as a function of temperature used to simulate the phase-change layer thermal property.

The electrical and thermal conductivity in the chalcogenide material are temperature dependent, hence the system is strongly-coupled and based on a non-linear set of equations which COMSOL solves in a self-consistent way with a non-linear Newton solver. The temperature dependence of both the electrical and the thermal conductivity models used to simulate the *write* and *read* operations are reported in the following sections.

4.2.1 Electrical conductivity

The electrical conductivity was modeled during the *write* and *read* operations by two distinct equations. In particular, during the *write* operation, the electrical conductivity of the crystalline and of the amorphous ON-phase can be described by the same equation [136, 137]. This is in accordance with the superposition of the IV characteristic (Fig. 1.13) for these two states. In addition, the same equation was used to model the system for temperatures above the melting value. This is justified by the experimental evidence of a continuous transition at T $\sim T_m$ [138]. The equation used to model the chalcogenide electrical conductivity was:

$$\sigma_{ON}(T) = \frac{A_e}{2}[tanh(B_eT + C_e) + D_e] \tag{4.3}$$

where $A_e = 1.3{\cdot}10^4$ Sm^{-1}, $B_e = 0.0022$ K^{-1}, C_e = -1.8 and $D_e = 1$. These values were obtained following a tuning process to constrain the SET resistance value at room temperature and the conductivity after melting at $\sim$ 3 Ωm [138]. The temperature dependent electrical conductivity profile used to simulate the device during the *write* operation is reported in Fig. 4.3. The transition from low to high electrical conductivity in correspondence of the melting temperature is considered smoother with respect to the actual physical phenomenon, to guarantee the convergence of the solver. The implementation of $\sigma_{ON}(T)$ in the electro-thermal model enables the evaluation of the temperature achieved in each point of the simulated geometry.
On the contrary, the *read* operation was based on the hypothesis that the entire PCL region crossing the melting temperature during the *write* operation undergoes the change

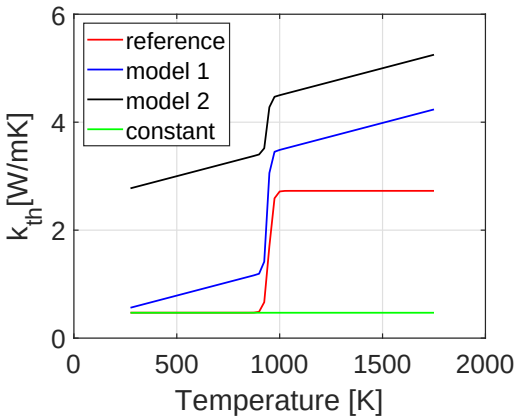

Fig. 4.5. Comparison of different thermal conductivity models implemented in the simulation tool.

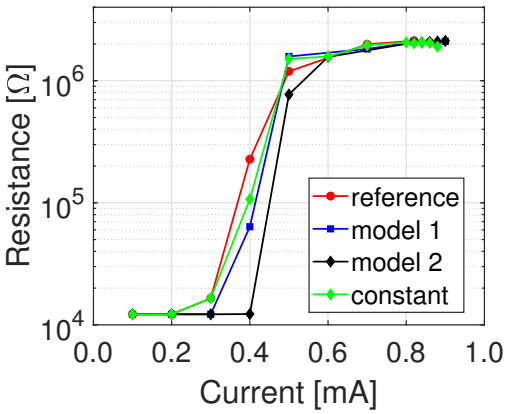

Fig. 4.6. Comparison of the resistance vs current curves simulated by the use of the four k_{th} models presented in Fig. 4.5.

of phase from the crystalline to the amorphous phase. Therefore, the function was modeled by assuming the conductivity to be σ_{ON} at room temperature while dropping to the value assumed in the amorphous phase for temperatures above T_m. Also in this case, the transition between the two equations was kept smooth to avoid convergence issues. The model used is reported in Fig. 4.3 and it is described by the following equation:

$$\sigma_{read}(T) = \frac{A_r}{2}[D_r - tanh(B_r T + C_r)] \tag{4.4}$$

where A_r = 1.205·10^3 Sm^{-1}, B_r = 0.05 K^{-1}, C_r = -44 and D_r = 1.01.

4.2.2 Thermal conductivity

The temperature dependence of the phase-change layer thermal conductivity was modeled in a similar way as $\sigma_{ON}(T)$ [137]. This was indeed expressed as:

$$k_{th}(T) = \frac{A_t}{2}[tanh(B_t T + C_t) + D_t] \tag{4.5}$$

where A_t = 2.566 Wm^{-1}K^{-1}, B_t = 0.051 K^{-1}, C_t = -48.359 and D_t = 1.418. These values were obtained following a tuning process to match the value of the thermal conductivity at room temperature with the k_{th} of the chalcogenide material in the crystalline phase ($\sim$ 0.5 Wm^{-1}K^{-1}) and ensuring an abrupt transition to higher values ($\sim$ 2.7 Wm^{-1}K^{-1}) around the melting temperature, in accordance with the results reported in [139]. The thermal conductivity versus temperature plot used in this work is reported in Fig. 4.4 and it represents the reference for the following investigations presented in this work.

Impact of the thermal conductivity model on the electro-thermal simulations

The thermal conductivity model presented in Eq. 4.5 assumes a constant k_{th} value before and after the melting temperature (Fig. 4.4). Nevertheless, the experimental results presented in the literature show an increase of the thermal conductivity with

temperature up to 400 °C [47, 48]. In this section, the impact of the thermal conductivity expression on the RI curve obtained from the PCM electro-thermal model will be presented. In particular, the reference model (Eq. 4.5) will be compared with two further models that take into account the k_{th} increase with temperature.
The first model (i.e., model 1) considers a linear increase of the k_{th} both before and after the phase-change material melting temperature (T_m = 930 K), by keeping the thermal conductivity at room temperature as well as the k_{th} increase in correspondence of the melting temperature unchanged with respect to Eq. 4.5. The RI resulting from this model is reported in Fig. 4.6 and compared with the previous model (reference). Before reaching the RESET state, the resistance value assumed by model 1 is smaller or equal to the reference one. This difference can be ascribed to the slightly higher thermal conductivity of model 1, which reduces the thermal efficiency of the cell, reducing the amount of volume brought at a temperature above T_m.
In model 2, instead, the k_{th} at room temperature is significantly increased up to about 3 $Wm^{-1}K^{-1}$ and a temperature dependency similar to model 1 is defined before and after the melting temperature. Since the value assumed by the k_{th} is higher than in model 1, the measured resistance at small currents values resulted lower than in the two cases previously presented. Therefore, when a constant k_{th} is assumed below melting (as in Eq. 4.5), the overall resistance measured could be overestimated.
Furthermore, it can be noted that the RESET resistance is independent from the model used. To confirm this, a simulation was performed considering a constant thermal conductivity in the range of temperature investigated. The value of the constant was chosen to match the one assumed by the reference model at room temperature (Fig. 4.5). The resulting RI output, reported in Fig. 4.6, does not show any significant difference in the resistance profile with respect to the other models investigated.
In conclusion, the simulated resistance is independent from the k_{th} model at $T > T_m$. Nevertheless, an accurate model for the phase-change layer thermal conductivity evolution in temperature is required, especially for temperature below the melting one. This is further confirmed by considering that the active volume is in direct contact with the part of PCL that does not take part to the phase transition (i.e., characterized by the properties of the PCL at room temperature), which controls the thermal losses in the surrounding of the active region. This represents a further reason for measuring and investigating the thermal conductivity of the phase-change materials integrated in our PCM devices, as already presented in Ch.3.

4.3 Parametric study

The geometrical and physical properties of a PCM device can be improved to obtain a more efficient programming of the cell. As already discussed in Ch. 2, the materials directly in contact with the phase-change layer are the ones playing a crucial role in determining the generated temperature profile in the PCM.
In this section, 3D electro-thermal simulations will be presented with the aim to optimize the electro-thermal response of the cell and to provide the main guidelines for the development of the next generation low-power PCM.
The components having the major influence on the electro-thermal behavior of the cell are (Fig. 4.7):

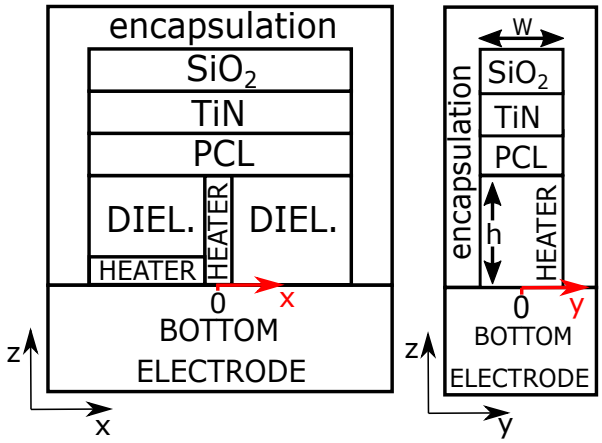

Fig. 4.7. Scheme of the zx and zy planes of the simulated Wall-based PCM. The Wall width is $w = 80$ nm, while h is the heater height . As a reference, the origin of the x and y axis is reported in red.

- the phase-change layer, since the thermal properties of the material not involved in the programming operation can influence the thermal confinement of the active region;
- the encapsulation layer, which is in direct contact with both the heater and the PCL in the zy direction;
- the heater, which is responsible for the PCL heating;
- the dielectric in direct contact with the heater (labelled as DIEL. in Fig. 4.7), which impacts the heat losses along the x axis and, as a consequence, potentially affects the heater thermal efficiency.

An investigation on the PCL thermal conductivity model was discussed in the previous section, demonstrating the need for an accurate PCL thermal conductivity measure for temperature lower than the material melting temperature. Furthermore, the encapsulation layer effects on the PCM performance will be treated in Ch. 5.
Here, the analysis will be focused on the heater and on the adjacent dielectric in contact with it, investigating, in particular, the temperature profile in the PCM in response to increasing supplied currents. In particular, to describe the temperature profile achieved in the device, the isotherms reaching the melting temperature $T_m = 930$ K in both the PCL and the heater were analyzed and their distances from the PCL/heater interface (i.e., z = 0), namely z_{melt} and z_{heater}, were measured (Fig. 4.8). The area lying between z_{melt} and z = 0 represents the programmed region or active volume; the region between z_{heater} and z = 0 provides a more accurate description of the temperature profile evolution as a function of the programming current; the region between z_{melt} and z_{heater} is defined as the *hot point*.
The analysis was performed by investigating the evolution of z_{melt} and z_{heater} both at the center of the cell (x = 0, y = 0, see Fig. 4.7) and on the PCL/encapsulation interface (x = 0, y = w/2, defined as *border*, see Fig. 4.7) as a function of the applied current. The analysis of both the center and the border is fundamental to define the melting current I_m, i.e., the current value at which the entire PCL/heater interface

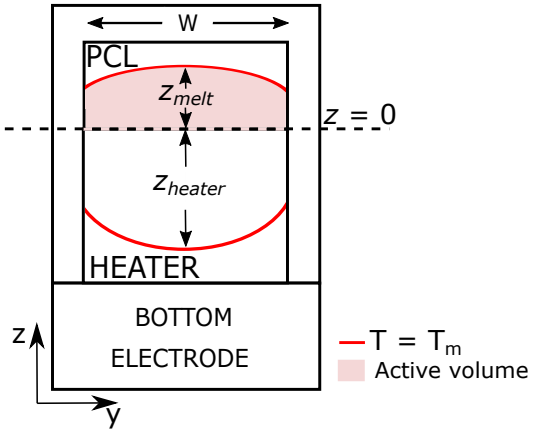

Fig. 4.8. Scheme of the zy plane of the simulated Wall-based PCM, highlighting the main parameters defined to investigate the thermal performance in different regions of the cell.

crosses the phase-change material melting temperature.
The influence of both the heater and the dielectric properties on the PCM programming conditions were investigated by independently considering the following parameters: the heater height, its electrical resistivity and the thermal conductivity of the dielectric surrounding the heater. The results of this study are reported in the following sections.

Heater height optimization

The analysis was performed for three heater height values: 80 nm, 120 nm, 160 nm. Fig. 4.9 reports the evolution of z_{melt} (filled markers) and z_{heater} (empty markers) at the *center* of the cell and on the *border* as a function of the applied current. The dashed line at z = 0 represents the interface between the heater and the phase-change layer. The melted region at the center of the cell is not influenced by the heater height (Fig. 4.9a). On the other hand, the modulus of z_{heater} increases for increasing applied currents, with a rate dependent on the heater height: at a current of 0.6 mA, z_{heater} assumes a value of -100 nm for $h = 160$ nm, while it reaches -25 nm for $h = 80$ nm. Therefore, increasing the heater height, the propagation of the *hot point* towards the heater is favored, causing, as a result, z_{heater} to cross the z = 0 interface at a lower current with respect to the other cases analyzed.

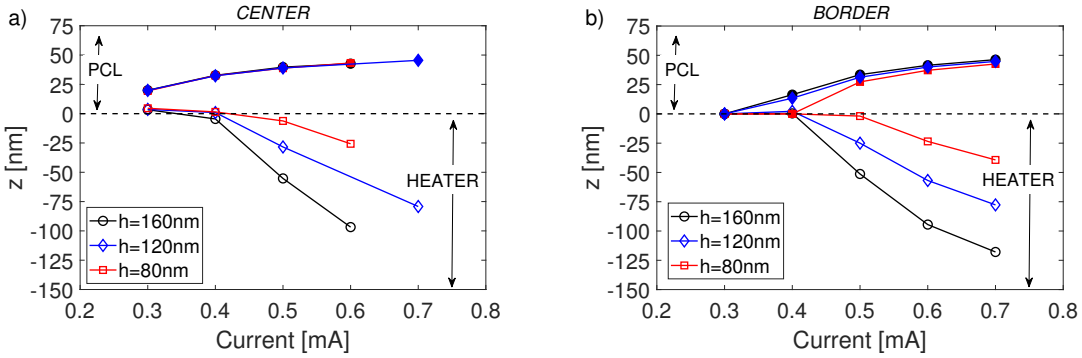

Fig. 4.9. Evolution of z_{melt} (filled markers) and z_{heater} (empty markers) a) at the *center* and b) on the *border* as a function of the applied current in devices characterized by different heater height. The dashed line represents the interface between the heater and the phase-change layer (i.e., $z = 0$).

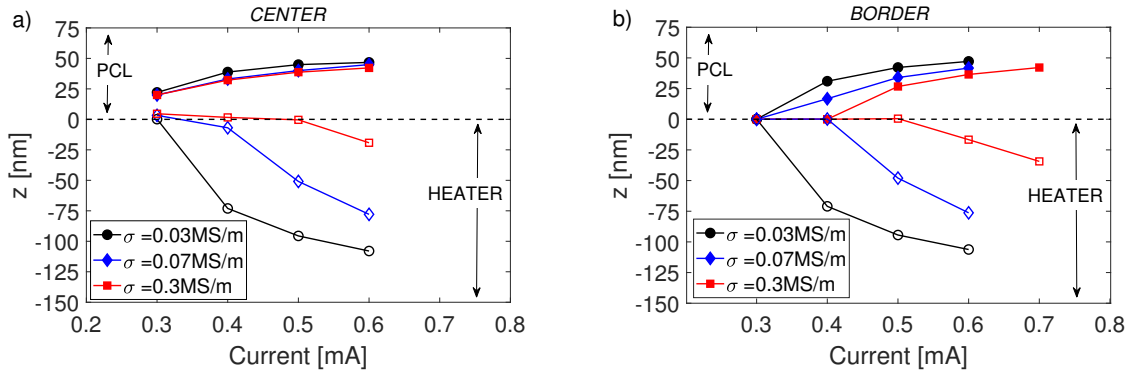

Fig. 4.10. Evolution of z_{melt} (filled markers) and z_{heater} (empty markers) a) at the *center* and b) on the *border* as a function of the applied current in devices characterized by different electrical conductivity of the heater. The dashed line represents the interface between the heater and the phase-change layer (i.e., $z = 0$).

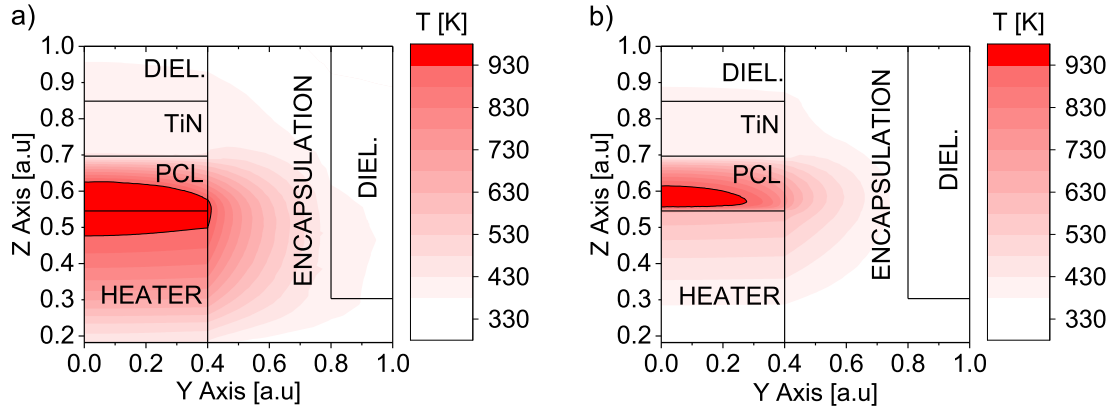

Fig. 4.11. Temperature profile achieved in the cell using a heater having electrical conductivity of a) 0.03 MS/m and b) 0.3 MS/m at the same applied current. The former demonstrates the achievement of the melting along the whole interface and a wide region characterized by a temperature above 930 K. The latter, instead, shows that the applied current is far from the I_m, since the hot point is restricted to a narrow region in the PCL.

Furthermore, the analysis of the cell border (Fig. 4.9a), gives an insight into the temperature gradient along the y direction, allowing to identify the I_m. The melted region on the border is comparable for $h = 120$ nm and $h = 160$ nm, both presenting a melting current at 0.4 mA. The thermal response for h = 80 nm, instead, is shifted towards higher currents (0.5 mA), suggesting that a Wall PCM with a smaller heater is less thermally efficient.

Optimization of the heater electrical conductivity

A similar approach was exploited to investigate the influence of different heater electrical conductivities, considering the following values: 0.03 MS/m, 0.07 MS/m and 0.3 MS/m.

The evolution of z_{melt} and z_{heater} at the *center* of the cell and on the *border* are reported as a function of the applied current in Fig. 4.10. The results follows the same trend showed for the previous parametric study. In particular, the temperature profile is propagating more easily towards the heater as soon as the electrical conductivity

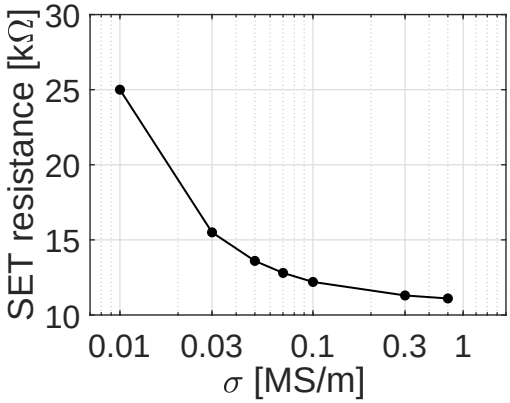

Fig. 4.12. SET resistance as a function of the heater electrical conductivity, showing that the SET resistance increases by reducing the heater electrical conductivity.

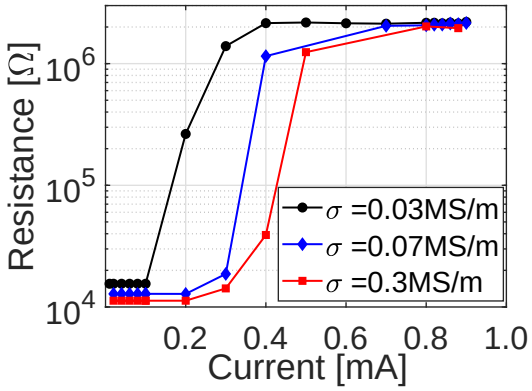

Fig. 4.13. Resistance as a function of current simulated for PCM devices feauring different heater electrical conductivities. A low electrical conductivity induces an increase of the SET resistance along with a reduction of the melting current.

value is reduced.
Furthermore, the temperature profiles in the zy-plane achieved with an electrical conductivity of 0.03 MS/m and 0.3 MS/m for the same applied current are reported in Fig. 4.11. The black line in the plot represents the 930 K isotherm contour. The difference between the two thermal responses is evident: on one side, the low electrical conductivity allows a wider melted region with a more uniform temperature propagation along the y axis; on the other side, the higher electrical conductivity reduces the thermal efficiency of the cell and results in a smaller melted volume, fully localized inside the PCL, preventing the resistance increase.

Both the heater height and its electrical conductivity define the heater resistance and, as a consequence, the SET resistance of the PCM. As an example, the simulated SET resistance value as a function of the heater electrical conductivity is reported in Fig. 4.12. It evidences that a difference of one order of magnitude in the electrical conductivity can cause a 10 kΩ change in the SET resistance value. In this case, the increase in the SET resistance is a consequence of the increase in the heater resistance, therefore, a higher SET resistance corresponds to a higher Joule heating for the same applied current. This is in accordance with the thermal profile previously described (Fig. 4.11).
Furthermore, both Fig. 4.9 and Fig. 4.10 show that the thermal response of the cell is independent from the electrical and geometrical parameters at the lowest applied current (0.3 mA), while the temperature profile gets significantly affected with increasing currents, resulting in different resistance vs current characteristics. This effect is directly linked to the Joule heating dependence on the squared power of the applied current. The simulated RI curves for different electrical conductivity values are reported in Fig. 4.13, highlighting both the increase of the SET resistance (in accordance with Fig. 4.12) and the reduction of the current required to achieve the RESET state. The observed increase in the SET resistance observed does not represent a limitation in the technology, since a resistance window of two order of magnitude is still demonstrated for low electrical conductivity values (Fig. 4.13).

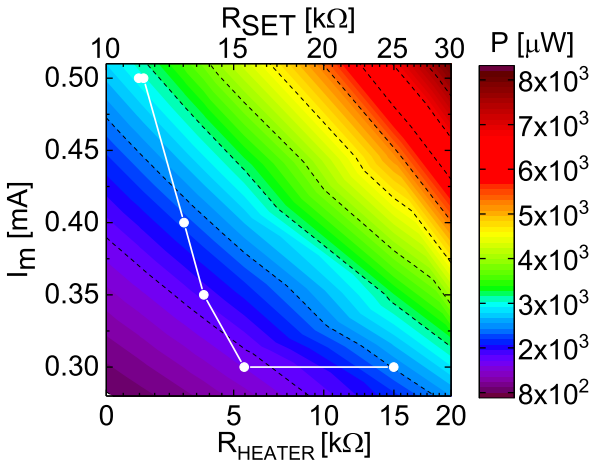

Fig. 4.14. Contour plot of the power required to program a 80 nm Wall-based PCM as a function of the melted current (I_m) and the heater resistance (R_{HEATER}), which is directly linked with the SET resistance (R_{SET}). The white line represents the I_m as a function of R_{HEATER} for the simulated structure with different electrical conductivity values, showing the saturation of the melting current for increasing heater resistances. The optimal working conditions are obtained for a $R_{HEATER} = 5$ kΩ, which corresponds to the onset of the I_m saturation.

A better analysis of the electro-thermal performance can be obtained by looking at the main parameters controlling the PCM functionality: the melting current and the SET resistance. Since devices with the same active layer are here compared, the heater resistance (R_{HEATER}) plays the same role as R_{SET}. The white plot reported in Fig. 4.14 shows that I_m decreases with the increase of the heater resistance until it reaches a saturation value at 0.3 mA. The saturation observed can be explained by taking advantage of the temperature profiles reported in Fig. 4.11. In particular, the low resistive heater (Fig. 4.11a) shows a higher temperature gradient along the y direction with a hot point localized slightly above the PCL/heater interface. On the contrary, the higher heater resistance (Fig. 4.11a) shows a wider hot point, which is spreading more significantly towards the heater and is characterized by a more uniform temperature gradient in the y direction. Therefore, as soon as the heater resistance is further increased, the hot point will considerably move inside the heater, generating a temperature profile almost constant along the y direction. At this point, an additional increase in the resistance value will not induce any relevant change in the uniformity of the final temperature profile along the y axis, as a proof that the saturation condition is attained. Hence, the saturation phenomenon observed reveals that the temperature profile inside the PCL cannot be further improved when the resistance overcome a specific value.
In addition, the saturation condition could result in thermally inefficient PCM devices when a too high SET resistance is considered. As an example, the contour plot in Fig. 4.14 is used to display the power required to reach the melting condition for a specific R_{HEATER} (or R_{SET}). It reveals that the device having an heater resistance of 15 kΩ presents the same melting current of the one with $R_{HEATER} = 5$ kΩ, but its programming power is higher. In conclusion, it is important to define the lower heater resistance guaranteeing the lower melting current. This is a key point to prevent power losses during the programming operation of a PCM. For the Wall-based

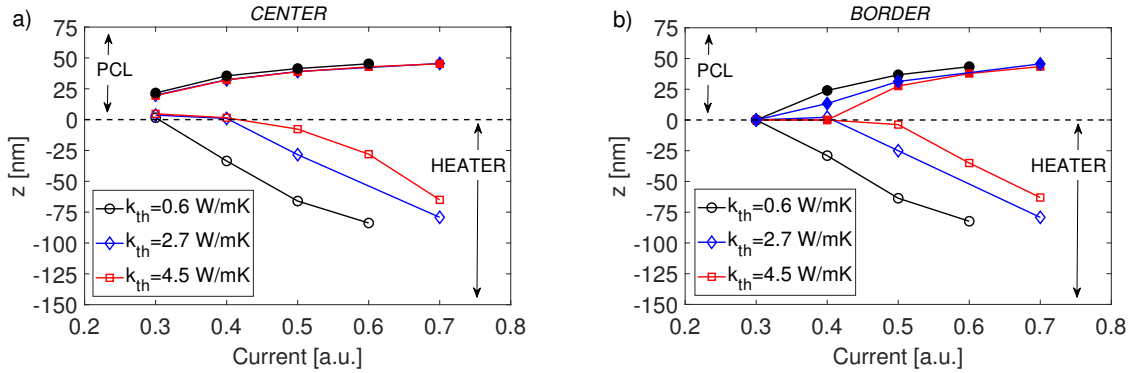

Fig. 4.15. Evolution of z_{melt} (filled markers) and z_{heater} (empty markers)a) at the *center* and b) on the *border* as a function of the applied current in devices featuring different thermal conductivity values for the dielectric surrounding the heater. The dashed line represents the interface between the heater and the phase-change layer (i.e., $z = 0$).

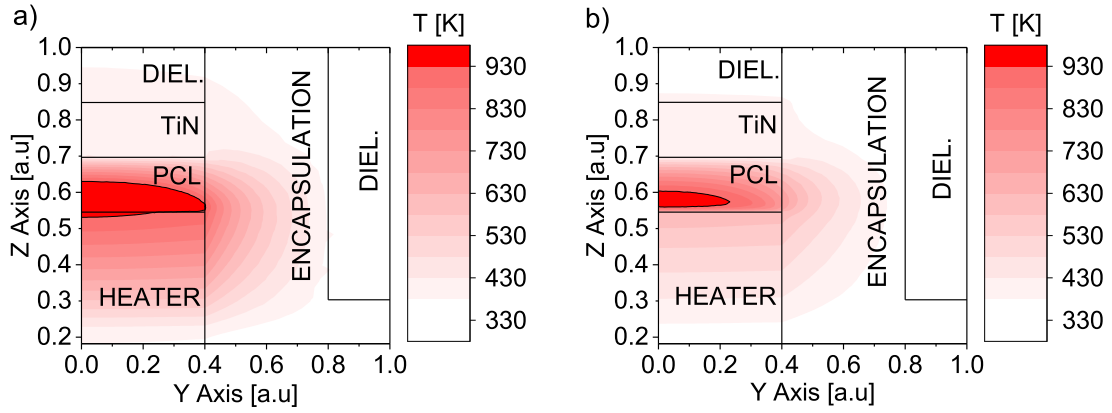

Fig. 4.16. Temperature profile achieved with a dielectric thermal conductivity of a) 0.6 $Wm^{-1}K^{-1}$and b) 4.5 $Wm^{-1}K^{-1}$ for the same applied current. The smaller thermal conductivity value demonstrates that the melting is reached along the whole interface. Furthermore, this condition presents a wider melted region with respect to the higher k_{th} one, which, instead, is characterized by an hot point still localized in the PCL (i.e, far from the I_m).

PCM investigated in this study, the working point is represented by a cell having a heater resistance of 5 kΩ, corresponding to a melting current of 0.3 mA (see Fig. 4.14).

Dielectric thermal conductivity optimization

The effect of the thermal conductivity of the dielectric surrounding the heater is here studied by carrying out the same type of analysis previously performed for the heater height and electrical conductivity.

The evolution of z_{melt} and z_{heater} at the *center* of the cell and on the *border* are reported as a function of the applied current in Fig. 4.15. Also in this case, the main differences in the thermal response of the PCM are identified in the value of z_{heater}. Indeed, in Fig. 4.15a z_{heater} assumes a value of $\sim$ -75 nm at an applied current of 0.6 mA for the smaller value of k_{th}, while it is equal to -25 nm for the higher thermal conductivity simulated at the same programming current. This demonstrates that the thermal efficiency of a PCM cell is lower when the heater is surrounded by a high k_{th} dielectric material. The thermal losses along the y direction are confirmed by the z_{melt}

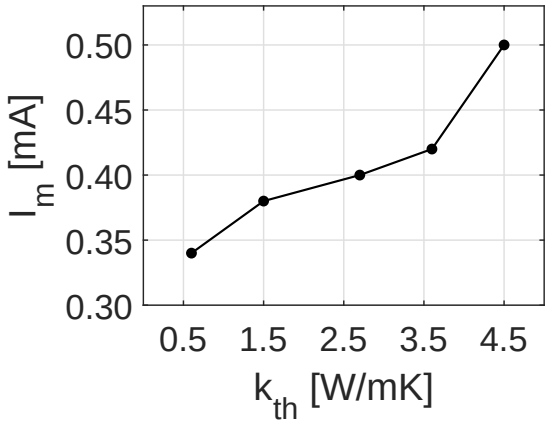

Fig. 4.17. Simulated melting current as a function of the dielectric thermal conductivity showing the increase in melting current (almost 150 µA) when the k_{th} is increased from 0.6 $Wm^{-1}K^{-1}$ to 4.5 $Wm^{-1}K^{-1}$.

values reported in Fig. 4.15a. Indeed, for k_{th} = 4.5 W m^{-1} K^{-1}, a melted region is generated only when a current of 0.5 mA is applied, which is 0.1 mA higher than the melting current reported for the other k_{th} values tested.
The different response is better highlighted by looking at the temperature profile in the zy-plane achieved with a thermal conductivity of 0.6 $Wm^{-1}K^{-1}$ and of 4.5 $Wm^{-1}K^{-1}$ at the same applied current (Fig. 4.16). The black line in the plot represents the 930 K isotherm contour. The temperature profile in the smaller thermal conductivity value shows that the melting condition is already reached in the whole PCL/heater interface. Whereas, the higher thermal conductivity presents a tiny melted region inside the PCL and slightly above the PCL/heater interface, demonstrating that the current investigated is distant from the I_m. In addition, the simulated melting current as a function of different dielectric thermal conductivities is reported in Fig. 4.17. It shows that I_m increases with the dielectric k_{th}.
As a result, tuning the dielectric thermal conductivity value represents a possible strategy to reduce the power consumption in PCM devices: a smaller k_{th} reduces the heat loss through the material surrounding the heater, enabling a uniform temperature increase at the heater/PCL interface.
As a matter of comparison, the I_m values acquired for the study performed in Section 4.2.2, where different k_{th} equations are used to model the PCL thermal conductivity, are reported in Table 4.1. It can be observed that, even if model 1 (k_{th} at room temperature of $\sim$ 0.3 $Wm^{-1}K^{-1}$) and model 2 (k_{th} at room temperature of $\sim$ 3 $Wm^{-1}K^{-1}$) have a relevant difference in the k_{th} value, the I_m remains the same. As a result, for the Wall-based PCM device studied in this work, the thermal conductivity of the dielectric surrounding the heater has a stronger effect on the final performance of the device with respect to the phase-change layer one. Therefore, in this case, the PCL thermal conductivity plays a marginal role in the device eletro-thermal performance.

PCM k_{th}model	I_m [mA]
model 1	0.5
model 2	0.5
constant	0.4
reference	0.4

Table 4.1. Simulated melting current for each of the k_{th} model presented in Section 4.4.

4.3.1 Discussions and conclusions

The parametric study described in this section showed the importance of the optimization of the device design as well as of the physical properties of the materials.
Interestingly, it was demonstrated that the choice of a low thermal conductivity dielectric layer surrounding the heater can enhance the thermal performance of the device. Indeed, this generates a more uniform temperature gradient along the y direction in the phase-change layer, resulting in a lower melting current. Furthermore, it showed that the heater resistance plays an important role in the electro-thermal response of the cell. Its value was tuned by varying the heater height and its electrical conductivity.
In general, the use of a higher heater resistance is preferable since it reduces the I_m, but, beyond a threshold resistance value, an increase in the heater resistance does not cause a further reduction in the melting current. This leads to an increase of the power consumption inside the PCM (Fig. 4.14). It is hence important to find the good trade-off between melting current, heater resistance and power consumption.
As a consequence, the fabrication of the next generation low power PCM will require to first identify the resistance value at the onset of the I_m saturation phenomenon. In the current work, this condition is fulfilled by an heater resistance of 5 kΩ, associated with a melting current of 0.3 mA. Secondly, the height or electrical conductivity of the heater must be tuned to guarantee the desired resistance value. In this step, a change in the electrical conductivity of the material involves a study on new materials, which have to be compatible with chalcogenides, ensuring good conformity and adherence with the PCL. Therefore, such investigation represents a tough and time-consuming study. On the contrary, the height tuning procedure requires less efforts than the material engineering, since the only constraint is represented by the maximum heater height. This is, in fact, associated to: i) the difficulty to reliably fabricate high aspect ratio structures; ii) the distance between the bottom and top metal layers (M4 and M5) where the PCM is integrated. Therefore, in the process of the heater resistance optimization, it is suggested to first fix the heater height at its maximum limit, then to optimize the material electrical resistivity, if the first step is not enough to reach the targeted resistance.
The optimal heater resistance for the Wall-based PCM simulated in this work (contact area of 80 nm x 10 nm and heater electrical conductivity of 10^5 S/m) is 5 kΩ. The first step of the procedure previously presented suggests that the heater height should be of 400 nm. Nevertheless, such a tall heater cannot be integrated in a 80 nm Wall-based PCM, since, in this case, it is not possible to ensure a conform etching of the whole PCM stack with a so high aspect ratio. A possibility to achieve the same result, avoiding the material engineering, is to consider an heater 200 nm high and with a surface

of 80 nm x 5 nm, which does not change the technology node and is reliable in terms of fabrication. In this procedure of resistance tuning, it is preferred to keep constant the Wall width since it determines the PCM node, hence no change in the device scaling is forced. Nevertheless, while targeting highly scaled devices (i.e., devices with a smaller contact area), the electrode material engineering will become necessary to satisfy the constraint imposed on the resistance value.

4.4 Optimization of the electrical conductivity model

The resistance vs current curve simulated using the electro-thermal model presented in Section 4.2 gives rise to a steep transition from SET to RESET. Furthermore, in this curve, the RESET state remains unchanged when the current is further increased (e.g. Fig. 4.13), as an evidence of an almost fully amorphized PCL. Nevertheless, the electrical tests (presented in the next chapter) show a RI curve where the high resistive state is reached via a gradual increase of the resistance as a function of the applied current. This highlights a mismatch between the experimental data and the simulated curve for applied current values above I_m.
The temperature profile in the zy-plane obtained with the use of the reference model (Section 4.2.1) is reported in Fig. 4.18. The black line in the plot represents the 930 K isotherm contour. In particular, the temperature profiles obtained in the cell after the application of i) a current I_m (Fig. 4.18a) and ii) a current 100 μA higher than I_m (Fig. 4.18a) are presented. Fig. 4.18a shows that, at the melting condition, the hot point is centered close to the PCL/heater interface and most of the chalcogenide is above the melting temperature. Furthermore, increasing the current, the temperature profile presents a significant variation of the amorphous thickness, which reaches a value of about 15 nm at the border with the encapsulation layer (Y = 0.4 a.u.). This result demonstrates that keeping the hot point at the interface between the PCL and the heater can i) ensure a uniform melting at this interface and ii) generate an abrupt transition from SET to RESET due to the substantial amount of material melted after a slight increase in the applied current.
Nevertheless, as anticipated at the beginning of the section, this behavior is not representative of the physical phenomena occurring in the device, where the transition from the SET to the RESET state is more gradual. The difference between the simulated and the electrical results can be attributed to the electrical conductivity model used in the study. Indeed, the model introduced in Section 4.2.1 considers the electrical conductivity as only dependent from the temperature, while it is also activated by the electric field [136], with an exponential dependence. This exponential relation is expected to affect the device behavior for increasing applied currents: the electric field contribution results in the increase of the phase-change layer electrical conductivity, thus in a reduction of the PCL resistance. Such lower resistance value will displace the hot point towards the heater, giving a different electro-thermal response of the cell.
In the previous simulations, the electric field contribution was neglected to facilitate the computing. Indeed, implementing the dependency of σ from both T and the electric field increases significantly the computation time and makes more difficult to reach the convergence, due to the not smooth equation considered. Therefore, the electric field contribution was integrated in the temperature-dependent expression, thus keeping the

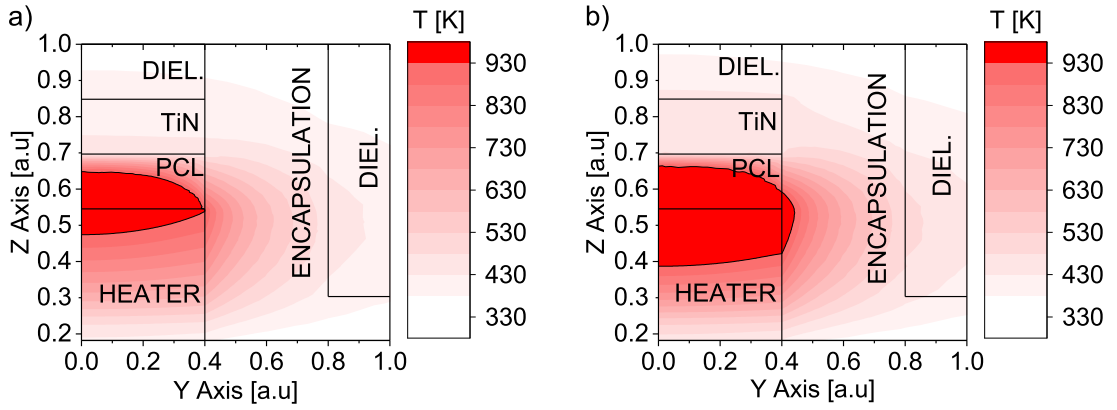

Fig. 4.18. Temperature profile achieved in the cell a) at the melting current and b) 100 µA beyond the I_m are applied b). The hot point covers the entire interface and it mainly propagates in the PCL, with a 15 nm height at the border with the encapsulation (Y = 0.4 a.u.).

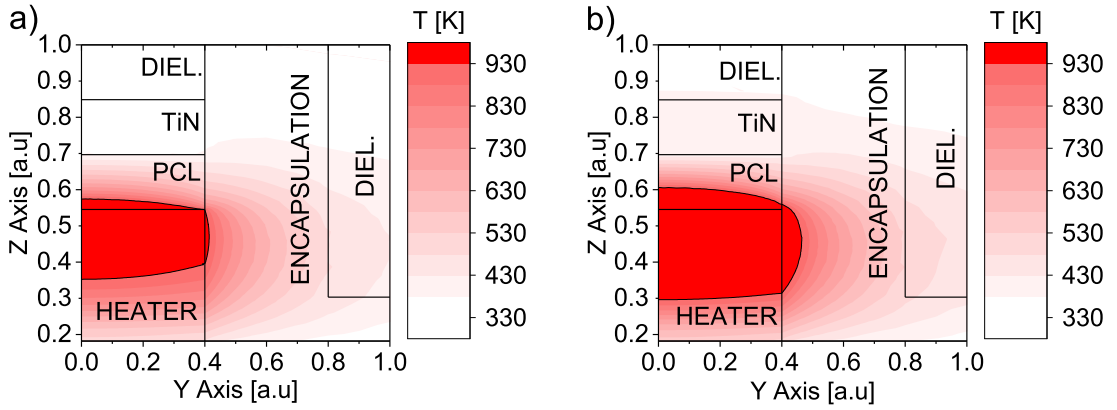

Fig. 4.19. Temperature profile achieved in the cell a) at the melting current and b) 100 µA beyond the $I_m$are applied b) in a PCM device where the PCL electrical conductivity is modeled to account for the electric field activated conduction. The hot point spreads mainly in the heater and the height of the melted region is increased of just 5 nm from the melting condition at the border (Y = 0.4 a.u.).

model only dependent on a single variable. With this aim, at first the electrical conductivity was modeled before ($\sigma_c(T)$) and after melting ($\sigma_{ON}(T)$) using an electrical conduction model expressed as a function of two physical parameters (i.e., conduction activation energy and conduction coefficient), as already presented in literature. The two expressions describing the thermal conductivity are:

$$\sigma_c(T) = e^{-\frac{B_c}{kT}+A_c} \tag{4.6}$$

$$\sigma_{ON}(T) = e^{-\frac{B_{ON}}{kT}+A_{ON}} \tag{4.7}$$

where $B_c = 0.14$, $A_c = \log(3{\cdot}10^5)$, $B_{ON} = 0.45$, $A_{ON} = \log(6{\cdot}10^6)$ [140]. To perform the study, the two models were unified in a single equation by an arcotangent function, which allows for a smoother transition between the two equations and ensures the convergence of the solver.

The temperature profile in the zy-plane obtained with the new model is reported in Fig. 4.19, where the black line represents the 930 K isotherm contour. As before, the temperature profiles are shown at the melting condition (Fig. 4.19a) and for a current

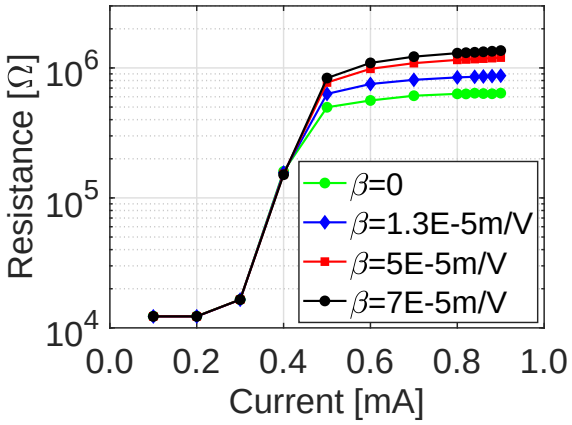

Fig. 4.20. Simulated resistance vs current plot reporting the effect induced in the RI characteristic when the expression in Eq. 4.8 is used to model the electrical conductivity in the *read* operation. The values of the activation coefficient (β) influences the resistance values at high current.

100 μA higher than I_m (Fig. 4.19a). The melting condition along the entire interface is here obtained for an applied current of 0.92 mA, twice higher than the I_m obtained in the previous model (Fig. 4.18a). Furthermore, the center of the hot point is localized in the heater with only a small portion of the PCL melted. Moreover, the temperature profile at the higher current presents a tiny variation of the amorphous thickness, which reaches a value of about 5 nm at the border with the encapsulation layer (Y = 0.4 a.u.), resulting in a smaller active volume with respect to the first model. This is a demonstration that the amorphous thickness, hence the resistance, increases more slowly in the new model when the system is subjected at the same current increase. Therefore, the new model allowed to achieve i) a higher value of melting current and ii) a more gradual resistance increase. These effects are both linked to the important spreading of the hot point in the heater. Indeed, in this case, an important amount of power is dissipated to heat up the heater, retarding the current at which the I_m condition is fulfilled. In addition, the distance of the hot point center from the PCL/heater interface makes the temperature profile more uniform and reduces the amorphous thickness increase with the applied current.

By testing this model, it was thus possible to confirm that the electric field dependence on the electrical conductivity model cannot be considered a second order effect in PCM functionality. Nevertheless, the model developed in this section provides a too high melting current with respect to the experimental one. Therefore, the integration of the electric field dependence is fundamental to get an accurate matching of the simulated curve with the experimental data. As a matter of fact, the implementation of this complete model in the simulation tool would enable, at first, an expression of the conductivity in accordance with the reference model (i.e., low electric field will not impact the electrical conductivity), allowing a low melting current. Increasing the current, instead, the electrical conductivity will abruptly increase with an immediate displacement of the hot point center from the PCL/heater interface to the heater. This leads to a gradual increase of the resistance in the second part of the curve.
Another contribution to the gradual transition characterizing the experimental RI curve can be associated to the electrical conductivity model used to read the resistance state

of the cell. Indeed, it should also be considered dependent from the electric field. An electric field dependent σ_r is developed and implemented in the simulation tool, to trigger the possible variation it can generate in the final RI curve. With this aim, the electrical conductivity value at temperatures above T_m was defined as:

$$\sigma_{OFF}(T) = \frac{\sigma_{ON}}{\alpha}(T)e^{\sqrt{\beta E}} \tag{4.8}$$

where the parameter α is a function of the resistance window and β is a coefficient defining the impact of the electric field on the final conductivity. The simulated RI characteristics for different β are reported in Fig. 4.20. This shows that a more gradual resistance increase with current is achieved after melting when a stronger dependency from the electric field is considered.

4.5 Chapter summary

In this chapter, 3D electro-thermal simulations were performed to investigate and predict the contribution of the main parameters influencing the PCM performance.
At first, it was demonstrated that the final resistance achieved in the memory is dependent on the model used to describe the phase-change material thermal conductivity evolution for temperatures lower than T_m. On the contrary, the k_{th} value above the chalcogenide melting temperature does not impact the programming operation.

Furthermore, the parametric study on the heater height and its electrical conductivity highlighted the importance to fabricate a Wall-based PCM having an optimal resistance value. Such value is the one guaranteeing the best trade-off between melting current and power used to program the cell. As a result, a set of optimal parameters were defined for the development of the next generation Wall structure: $h = 200$ nm, $w = 80$ nm and $t = 5$ nm (i.e., $R_{HEATER} = 5$ kΩ).

Different thermal conductivity values for the dielectric surrounding the heater were investigated, showing that the thermal efficiency of the cell is improved if the k_{th} of the dielectric layer is reduced. Indeed, a lower thermal conductivity value reduces the heat losses through the material surrounding the heater and enables a uniform temperature increase at the heater/PCL interface. This decreases the current at which the melting of the entire interface occurs. As a consequence, the melting current increases with k_{th}.

The comparison of the melting current obtained for the different PCL k_{th} models showed that I_m assumes almost the same value independently from the model considered. Therefore, it demonstrates that, in a Wall-based PCM, the PCL thermal conductivity has only a marginal role on the device electro-thermal performance.

Finally, the PCL electrical conductivity model was improved to guarantee a gradual transition of the resistance above I_m, thus matching the experimental evidences. Despite making the computation faster, considering the electrical conductivity as an exclusive function of the temperature cannot describe the programming dynamic of the memory, which requires the hot point, centered close to the PCL/heater interface, to suddenly shifts down in the heater as soon as the device crosses the melting conditions. To improve upon this, an electrical conductivity model integrating an explicit dependence from the electric field is required.

Chapter 5

PCM current reduction and thermal optimization

As already introduced in Ch. 2, the current reduction in PCM represents one of the main challenge for this technology, leading the scientific community to address the problem by the development of new thermal engineered devices. The most promising solutions presented so far are based on: i) the tuning of the thermal conductivity of the dielectric layer in direct contact with the phase-change material, which controls the heat losses in the surrounding of the active layer; ii) the use of a 3D dielectric interfacial layer, which decreases the contact area between the phase-change layer and the heater, due to a soft breakdown mechanism; iii) the integration of Ti doping in Sb_2Te_3 materials used as active layers, which are characterized by a low thermal conductivity, hence they can retain the heat inside the cell.
Based on these results, the performance of different thermally engineered PCM devices will be explored in this chapter. In particular, the investigated structures consists of: i) the integration of an SiC encapsulation layer all around the PCM; ii) the use of a 10 nm GeN interfacial layer; iii) different stack based on a TiTe/GST active layer.
The electrical characterization of 4kb arrays integrating the first couple of these solutions are supported by 3D electro-thermal simulations as well as TEM/EDX analyses performed on programmed devices/materials. It enabled the definition of the best features for each of the PCM structure, even in terms of aerospace applications.

5.1 Electrical characterization

The electrical characterization of PCM devices relies on the accurate measurement of the current and resistance values over different orders of magnitude, since their resistance window could span over up a maximum of five orders of magnitude. Furthermore, the test bench must allow the control of the fall time of the applied pulse independently from its rise and width. Indeed, pulses with a fall time as small as few ns are required to quench (and RESET) the device, while a long fall time (of the order of 10 µs), is necessary to SET it. Moreover, to compare the performance of different PCM devices, a set of parameters driving the PCM electro-thermal behavior are estimated. In particular, the most informative are: the minimum fall time to reliably SET the device (i.e., the SET speed), the cycling endurance and the retention of the stored information.
In this section, the devices and the experimental set-up used for the PCM electrical characterization are introduced. Furthermore, the main testing protocols implemented to compare the PCM performance will be presented.

5.1.1 Devices

The state-of-the-art Wall-based PCM devices were integrated in the Back-End-Of-Lines (BEOL) fabrication of the LETI Memory Advanced Demonstrator (MAD), which consists of a 200 mm wafer based on front-end 130 nm CMOS technology from STMicroelectronics. The PCM device BEOL process was performed in LETI cleanroom. The devices were fabricated with different wall widths (50 nm, 80 nm, 100 nm, 200 nm, 300 nm) and in three different configurations: single device (1R), device in series with a transistor (1T1R) and 4kb matrices, which allowed the statistical parameters evaluation.
The 1T1R device consists of a PCM integrated in contact with the drain of the NMOS addressing transistor fabricated in series with the device and used to tune the value of the maximum current that can flow in the memory. The channel of the transistor integrated in series with the memory had a 130 nm length and different possible widths,

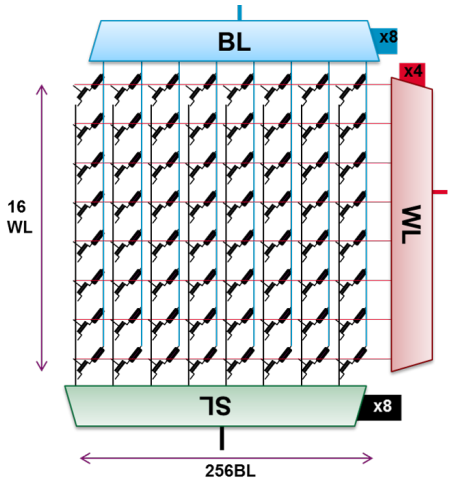

Fig. 5.1. Schematic representation of a 4kb PCM array (8 columns by 4 rows), showing both the Bit Line (BL) and the Word Line (WL) of the array.

with the role of fixing the value of the saturation current for each transistor. In this work, a channel width of 6700 nm was used to supply a maximum current of 3.8 mA to the device, while a 660 nm was chosen to achieve a finer control in current, when up to 300 µA were supplied.
The TiN pads had a rectangular shape of 50 µm x 90 µm and were fabricated in the Metal 5 layer of the integration. In 4kb arrays, the 4096 devices were addressed with the use of a 256 (Bit Line) by 16 (Word Line) matrix (see Fig. 5.1), which required the use of 8 pads for the Bit Line and 4 for the Word Line. Three further pads were then included for the Drain, Bulk and Ground connections.

5.1.2 Test set-up

The electric tests were performed by applying a voltage pulse (programming pulse V_{pulse}) and reading the current flowing into the device (programmng current I_{cell}). The resistance value was then retrieved by measuring the current flowing into the device when a low-voltage READ pulse was applied.
In the framework of this work, the PCM devices were integrated in 1R, 1T1R or 4kb matrices. Each configuration required a specific testing set-up, as described in more details in the next paragraphs.

1R devices

The measurements on single cells (1R) made use of a load resistor (R_{Load}) in series to the device Fig. 5.2. This had the role to both limit the current flowing in the cell (i.e., following the electrical spike occurring when the material switches to the ON-state) as well as to measure the current flowing in the device during the application of the pulse. The voltage was applied by a pulse generator (Agilent 81110A), which generates pulses in the timescale between 2.5 ns and 100 ms, allowing the independent modulation of their rise, width and fall time. The waveform was acquired with a Tetronix TDS 744A os-

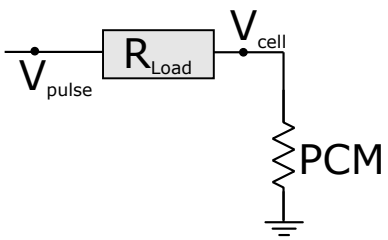

Fig. 5.2. Schematic representation of the electrical circuit used to test 1R devices. A resistor R_{Load} is used in series with the PCM device.

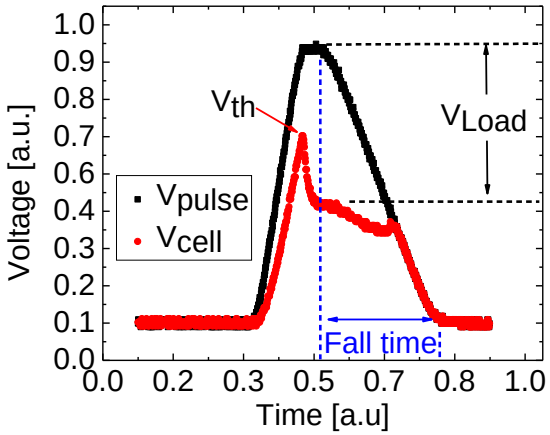

Fig. 5.3. Typical waveforms for the applied (V_{pulse}) and measured (V_{cell}) voltages. V_{Load} is the voltage drop on the load resistor, while V_{th} is the threshold voltage of the cell. The fall time of the applied pulse is also highlighted.

cilloscope having a fast 2GS/s sample rate. This enabled the evaluation of the voltage drop on the load resistor (V_{Load} = V_{pulse} - V_{cell}) and of the current flowing in the device, by:

$$I_{cell} = \frac{V_{pulse} - V_{cell}}{R_{Load}} \tag{5.1}$$

where V_{cell} is the voltage measured on the PCM device.
An example of the voltage waveforms applied and measured on the device is reported in Fig. 5.3. In particular, at low voltages, the entire voltage drops on the cell, while when the threshold voltage is reached, the cell switches to the ON-state (i.e., a highly conductive state) causing a voltage divider between PCM and R_{Load}. At this point, the value of the load resistance defines the amount of current flowing in the device. The value of R_{Load} used in this work is of $\sim$ 1 kΩ.
The PCM resistance value was retrieved by a low voltage pulse applied by an Agilent 4156C, which has a resolution of 1 fA in current and 0.2 μV in voltage.

1T1R devices and 4kb matrices
In 1T1R devices and matrices, the load resistance was not used. Indeed, in both cases, the maximum current flowing in the device was tuned through the transistor channel width and the potential drop between the gate and the source. In this configuration, the programming pulse was applied between the drain and the source of the transistor, where the source is short circuited with the transistor bulk (V = 0 V).
A B1500A Semiconductor Device Parameter Analyzer was used to apply single pulses or train of pulses and to allow the current/voltage read with a sampling rate of 5 ns. This set-up enabled read operations in up to five different current ranges (1 μA, 10 μA, 100 μA, 1 μA, 10 μA), thus ensuring an high resolution of the measure independently from the resistance value.
The test on 4kb matrix (schematically represented in Fig. 5.1) included a Keithley 230 Programmable Voltage Source, which provided a drain power supply to the whole matrix. This represented the maximum applicable voltage to electrically characterize 4kb matrix and its value was fixed at 4.5 V. The programming pulses were addressed to each device of the matrix by an Arduino board connected with a 25 Poles based D-Sub metal hood. This was performed in an automated way, by setting each entrance of the WL and BL with a sequence of logic 0 and 1.
In both matrices and 1T1R devices the read was performed at a voltage of 0.6 V to ensure the minimal potential drop between the drain and the source of the series transistors.

The three set-up can be used either in manual or automated mode, with the use of a 200 mm Cascade Microtech (12000-5378) probe system. Automated operations were preferred for testing 1R or 1T1R devices, since it allows a faster statistical analysis. A Python code was also used to control the probes motion along the different positions on the wafer as well as to implement the different testing protocols described in more details in the next section.

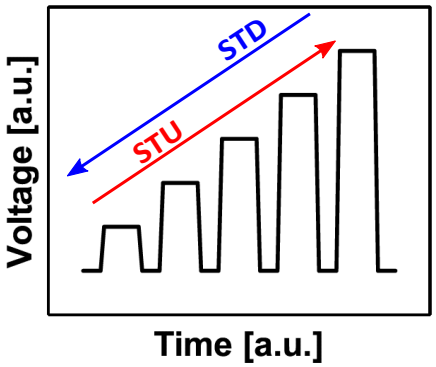

Fig. 5.4. Schematic representation of the staircase up (STU) and staircase down (STD) testing procedures.

5.1.3 Testing protocols

The electric test of PCM devices was performed through the application of single pulses or train of pulses to the memory. The choice of the pulse sequence and the definition of the amplitude, rise, width and fall time (FT) for each of its element plays a fundamental role in the investigation of the PCM performance and allows the comparison among different types of PCM.
The primary test performed on a PCM device is based on a single SET and RESET pulse. In this work, the standard pulse used to RESET the cell had a rise/width/fall time of 10/300/10 ns, while the SET had a longer FT, typically 1000 ns. A complete IV or RI characteristic was obtained when a sequence of these pulses is considered. The procedure mainly used in this chapter is the so-called staircase sequence: sequence of pulses with a specific rise/width/fall time were consecutively applied, with each pulse having an amplitude either higher (staircase-up or STU) or smaller (staircase-down or STD) with respect to the previous one. A scheme of this procedure is reported in Fig. 5.4. It is worth to clarify that the SET resistance achieved with a STD sequence is, in general, lower than the one obtained with a single SET pulse. This is due

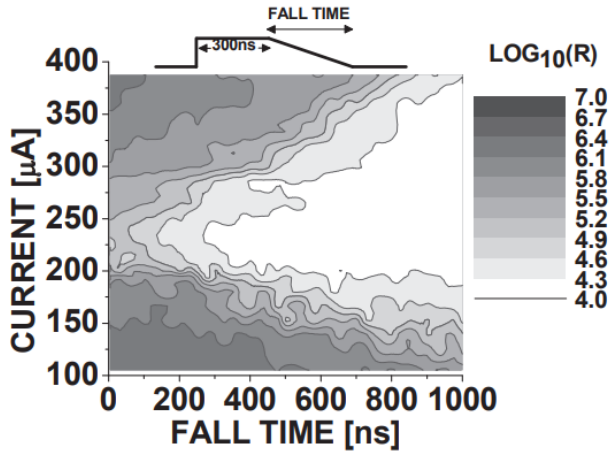

Fig. 5.5. SET speed carthography showing the evolution of the measured resistance (in grey scale) as a function of the pulse fall time (x-axis) and of the current (y-axis) [42]. It highlights that the shorter pulse ensuring a reliable SET of the device requires a current of $\sim$ 200 μA and a fall time of $\sim$ 350 ns.

to the cumulative effect of the staircase procedure.
Both the staircase and single pulse sequences can be adjusted depending on the PCM device parameter under investigation, such as: SET speed, endurance, retention. Furthermore, the same set-up can be used in quasi-static mode to acquire the sub-threshold IV characteristic of the device. All these test procedures will be described in the next paragraphs.

SET speed
The minimum fall time and current values required to efficiently SET the memory (i.e., SET speed) can be evaluated by setting a RESET pulse before each element of the STU sequence and repeating the same test for increasing FT. The introduction of a pre-pulse prevents the cumulative phenomenon typical of the staircase procedures. An example of this procedure is reported in Fig. 5.5. It highlights that the shorter pulse ensuring a reliable SET of the device requires a current of $\sim$ 200 μA and a fall time of $\sim$ 350 ns.

Endurance
The endurance defines the maximum number of transitions between the amorphous and the crystalline phase, keeping a distinction between the two programmable states. A RESET and SET pulses were repetitively applied and the resistance value was measured after a fixed amount of logarithmically spaced cycles in order to monitor the evolution of the two states and to identify an eventual failure.

Data retention
Data retention after annealing at specific temperatures represents a fundamental parameter to determine the device suitability for automotive applications. In this work, the data retention was performed on 4kb matrices by first programming two matrices, in SET and RESET state, respectively, and then monitoring the resistance evolution after baking the device for one hour at increasing temperatures, until triggering a RESET failure.

Quasi-static testing - sub-threshold IV
The IV curve acquired for $V < V_{th}$, can describe the type of conduction taking place in the material. In particular, this test can identify whether a SET pulse was effective to fully crystallize the active volume. Indeed, if the device is not in its minimum SET state, the IV curve will follow a non linear Poole-Frenkel conduction model, rather than an Ohmic characterisic.

5.2 Encapsulation layer effect on PCM performance

Since an important part of the heat is dissipated into the insulator surrounding the PCM, an example of thermal confinement improvement was recently investigated for a PCM planar structure, using a low thermal conductivity SiO_2-Al_2O_3 multilayer [103], as already introduced in Section 2.1.2. However, the use of oxide based dielectrics in scaled state-of-the-art PCM devices can lead to interactions with the phase-change material that could be detrimental for the device performance (e.g., data retention) [141][142].

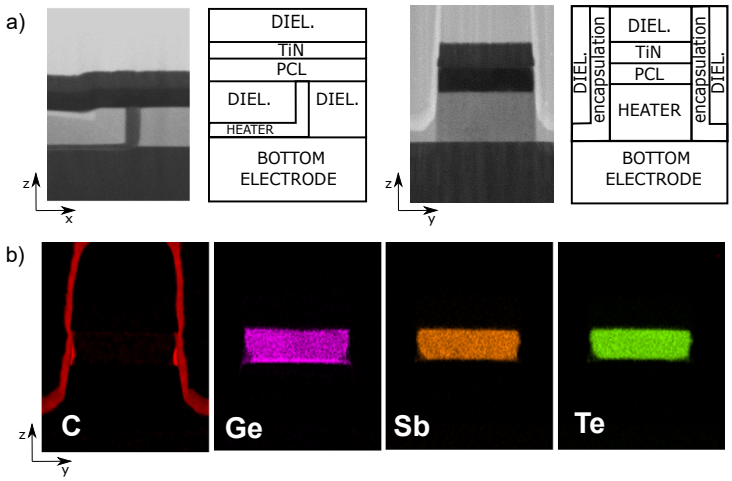

Fig. 5.6. a) Simplified description of the Wall-based PCM device. TEM images on the zx and zy planes performed on a nominal 300 nm device are reported along with the structure description. It further shows the location of the encapsulation layer, the Phase-Change Layer (PCL) and the dielectrics (DIEL.); b) TEM/EDX analysis on a nominal 300 nm device describing the SiC based encapsulation (C mapping) and the localization in the stack of the phase-change material layer (Ge, Sb and Te mappings) in the zy-plane.

In Ch. 3 we presented that SiC has a 70% lower k_{th} with respect to SiN. Therefore, both SiC and SiN were integrated in state-of-the-art PCM to compare their performance. The two encapsulation layers were deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) all around the PCM, after the etching of the memory stack, which was based on a GGST alloy integrated by sputtering from a single target. The location of the encapsulation layer can be clearly observed in the TEM images reported in Fig. 5.6, which represents the zx and zy view of the PCM along with a scheme specifying the different components of the memory stack. The Wall width in the y-direction of the tested devices is of 80 nm. The TEM/EDX analysis of an as fabricated device (w = 300 nm), performed along the xy plane, shows the perfect encapsulation of the PCM by the SiC layer (i.e. C mapping) and the localization into the memory stack of the phase-change material (i.e., Ge, Sb and Te mappings).
The structure was widely investigated in terms of electric performances on 4kb array, electro-thermal simulations and a theoretical model supported by physico-chemical analysis on the programmed devices, giving the possibility to describe the programming dynamics taking place in the cell. An insight to each one of this aspects will be provided in the following sections.

5.2.1 Electric test

Preliminary functionality tests were performed on both 80 nm 4kb SiC and SiN encapsulated PCM, by repetitive programming in SET and RESET state. The cumulative distributions for both the resistance states are reported in Fig. 5.7a. Both SiC and SiN functionality were confirmed and a higher resistance window is obtained for SiC-PCM. To better understand the difference between the programming dynamics of the two devices, the resistance evolution as a function of the applied current was acquired for the 4kb array and the results are reported in Fig. 5.7b. The characteristic was obtained

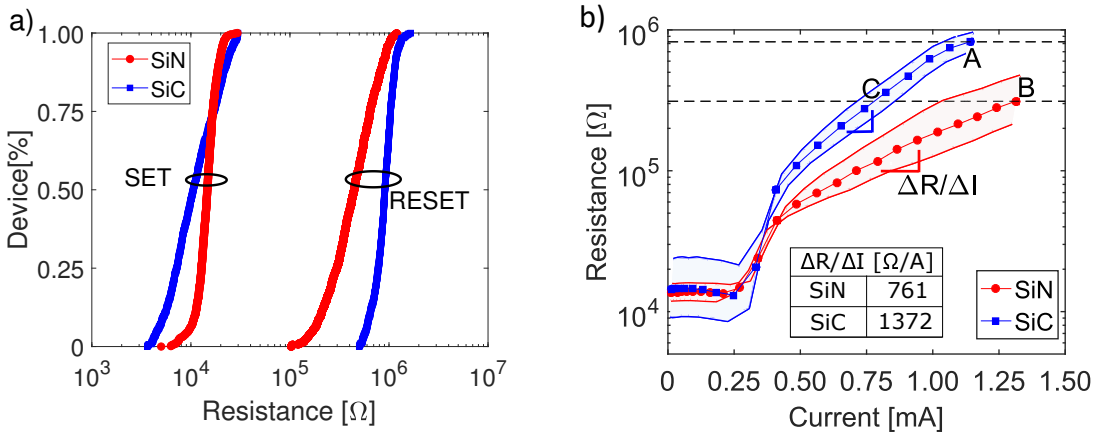

Fig. 5.7. a) Cumulative distributions for the SET and RESET resistance states measured in as fabricated 4kb arrays for both SiN and SiC encapsulation layers; b) Resistance as a function of the programming current for 4kb PCM arrays based on GGST with respectively SiN and SiC as encapsulation layers. The different $\Delta R/\ \Delta I$ slope is reported in the table, being higher for SiC-PCM. Points A (SiC) and B (SiN) represent the RESET state for our PCM devices, achieved without degrading the cell characteristic (i.e., over-RESET phenomenon). Point C represents for SiC-PCM, the current at which it is obtained the same resistance value of the RESET state of SiN-PCM.

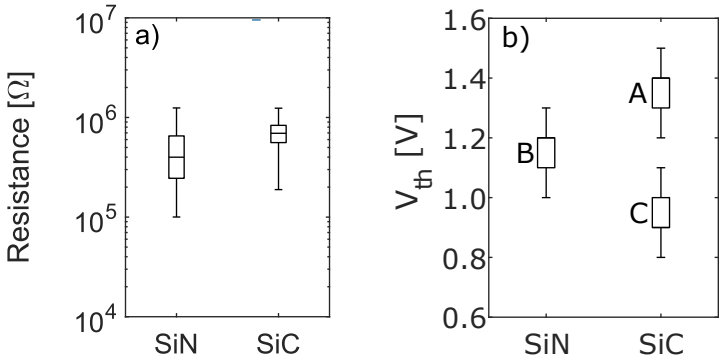

Fig. 5.8. a) Resistance distribution measured in 4kb arrays with a SP of 1 mA for both SiN and SiC-PCM. SiN devices feature a lower resistance value and a higher dispersion wrt SiC; b) Threshold voltage V_{th} for SiN and SiC-PCM measured for resistances achieved with A, B, C conditions reported in Fig. 5.7b. V_{th} measured in the devices programmed in the RESET state, is lower for SiN (B) than for SiC (A). On the contrary, V_{th} is reduced in SiC based PCM programmed at the same resistance value (C) of the RESET state of SiN based PCM (B).

by firstly program the devices in the SET state with a squared pulse (SP), which is a pulse having rise/width/fall times of 10/300/10 ns. The resistance increase towards the RESET state was achieved with a staircase-up sequence of SP's of increasing amplitude with steps of 0.1 V. Below the melting current (i.e., the current at which the resistance starts to increase) the characteristics appear overlapping. At higher current, the impact of the encapsulation can be observed. A RESET current (i.e., current needed to achieve the RESET state) reduction of $\sim 15\%$ was measured in SiC-PCM, which also showed a steeper variation of the resistance for the same current increase. It leads to a higher resistance for SiC with respect to SiN, achieved for the same current value of 1 mA, as reported in Fig. 5.8a. It means also a higher thickness of the amorphous volume (h_a) created in the SiC cell (i.e., $R \propto h_a$) [81][27], suggesting that for SiN-PCM

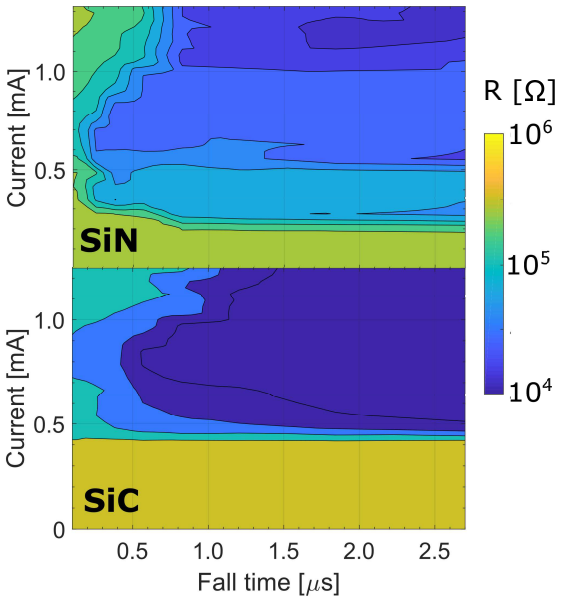

Fig. 5.9. SET programming cartographies: programmed resistance is represented as a function of the pulse fall time (pulse width = 300 ns) and of the pulse current for both SiN and SiC based PCM. SiC device reaches the lower resistance state with a pulse fall time of 1 μs and a current value of 0.6 mA, whereas SiN needs at least 1.6 μs and a current higher than 1 mA.

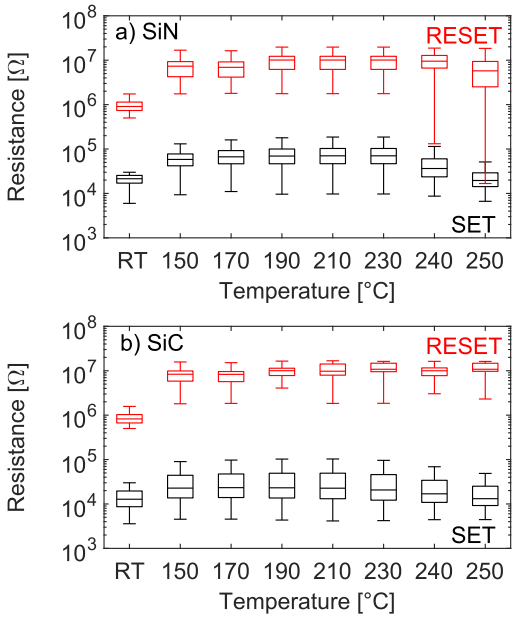

Fig. 5.10. Data retention performed by isochronal annealing of 1h at increasing temperatures on SET and RESET states for a) SiN and b) SiC. SET state was programmed with same pulse shape in both devices. SiC-PCM can retain RESET data up to more than 1 hour at 250 °C, while SiN-PCM shows a degradation of the information starting at 240 °C. SET state is affected by a higher drift of the resistance in SiN-PCM.

the increase of the amorphous volume is lower with respect to the SiC based PCM for the same current increase. Moreover, the variability of the resistance value appears lower in SiC with respect to SiN.

The hypothesis of a higher h_a in SiC with respect to SiN based PCM, was confirmed by measuring the threshold voltage (V_{th}) in the two devices. Indeed, since the threshold switching mechanism is electric field driven, as soon as an increase of V_{th} is observed, it is correlated with an increase of the amorphous thickness ($V_{th} \propto h_a$, as presented in Section 1.1.4). Fig. 5.8b shows that the V_{th} measured for the devices programmed in the RESET state (point A and B in Fig. 5.7b) is higher for SiC than for SiN (i.e., higher h_a). Moreover, if the SiC cell is programmed at a resistance value close to the one of SiN-PCM RESET state (point C in Fig. 5.7b), V_{th} is reduced with respect to point A, supporting the hypothesis that the shape of the amorphous dome created in the two devices is different, likely impacted by the different thermal conductivity of the two encapsulation layers.

The analysis of the SET programming speed performed on 100 nm devices is reported in the SET cartographies of Fig. 5.9. The test was performed by acquiring the resistance achieved in the cell after the application of a RESET pulse followed by a SET pulse (with a fixed pulse width of 300 ns, and increasing fall time and intensity). The higher RESET resistance was confirmed in SiC devices, which also showed the best performance in terms of SET speed. The enhanced thermal confinement in SiC-PCM can be responsible for a slower temperature decrease (wrt SiN) in the phase-change

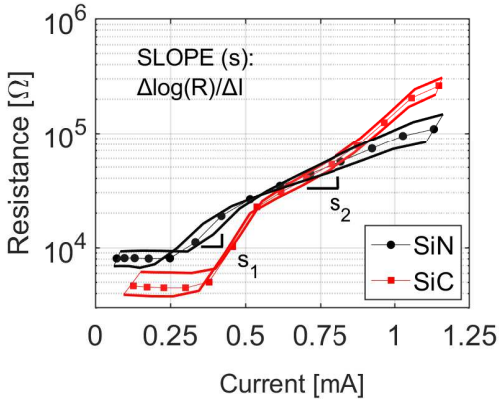

Fig. 5.11. Resistance as a function of the programming current for 4kb PCM arrays based on GGST with respectively SiN and SiC as encapsulation layers, obtained with a staircase-up sequence applied after a pulse with a long fall time (minimum SET state).

material during the fall time of the pulse applied, making the SET operation more efficient.
Data retention test was performed on both SET and RESET states by isochronal annealing of 1h at increasing temperatures, from 150 °C up to 250 °C (Fig. 5.10). The population of 2kb devices inside the 4kb arrays was considered for both SET and RESET states, for SiC and SiN devices. Devices with SiN encapsulation showed a higher SET drift up to 230 °C (i.e., increase of the resistance towards higher values), probably related to a lower programming SET efficiency (i.e., less crystallization degree), as previously shown in SET cartographies. Degradation of the RESET state starts at 240 °C in SiN-PCM, showing a total 25% of failures at 250 °C. On the contrary, SiC-PCM retains 100% of RESET data even after the annealing of one hour at 250 °C. This result can be explained by a more uniform amorphous volume achieved in PCM cells with an enhanced thermal confinement provided by the low conductivity SiC-based encapsulation.

The drift observed in both SiC and SiN based devices suggests that the test protocol used to program the device (i.e., single SET pulse plus staircase-up) was not able to fully crystallize the material. This could be the main cause of the different slopes observed in the RI curve after melting (i.e., cumulative effect generated by the staircase-up sequence). Therefore, the devices were programmed with another test protocol. First, the cell was pre-cycled with ten SET/RESET pulses. Then, the devices were programmed in the SET state with a pulse having a long fall time (SET-init) in order to achieve the lowest possible SET resistance state (i.e. rise/width/fall times equal to 10ns/300ns/10µs) for both SiC and SiN cells. The resistance increase towards the RESET state was obtained with a staircase-up sequence of squared pulses (SP) of increasing voltage amplitude, having rise/width/fall time equal to 10ns/300ns/10ns, pre-programming the device in the SET state with a SET-init pulse before each SP. The results are reported in Fig. 5.11. The different starting SET resistance between SiC and SiN based PCM is likely related to a different Ge expulsion during the forming operation [143] and the likely presence of residual amorphous regions due to the different thermal isolation, as it will be confirmed in following analyses. The different starting

material	s_1 $[dec/A]$	s_2 $[dec/A]$
SiC	3413	1742
SiN	1961	953

Table 5.1. Slopes s_1 and s_2 for both SiC and SiN devices, obtained from the RI characteristics reported in Fig. 5.11.

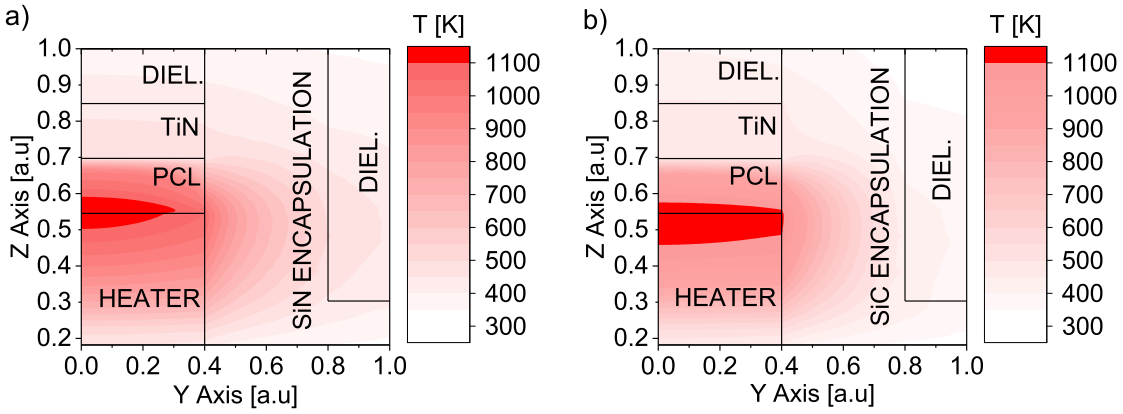

Fig. 5.12. Temperature profile simulated for both a) SiN and b) SiC based PCM for the same applied current. The SiC device presents a more uniform temperature profile along the y-direction and a temperature gradient oriented along the z-axis.

resistance influenced the value of I_m (i.e., first detection of resistance increase in the RI curve) that appears slightly lower in SiN than in SiC, in line with the trend reported in previous works [33]. Nevertheless, the gradual resistance increase with current is still evidenced and both curves present two slopes after reaching I_m, identified as s_1 and s_2. Their values are reported in Table 5.1, demonstrating a steeper resistance increase in SiC-PCM due to its higher s_1 and s_2 with respect to SiN-PCM. This result confirms that the phenomenon taking place in the tested devices is intrinsically driven by the different encapsulation layer used in the two structures.

5.2.2 Electro-thermal simulations and TEM/EDX analyses

3D electro-thermal simulations in COMSOL Multiphysics were performed to analyze the impact of the encapsulation on the PCM cell, by exploiting the SiC and SiN thermal conductivities previously measured. The methods and parameters used are described in previous works [137]. Being the structure symmetric with respect to the z-axis in the zy-plane, only half of the structure is simulated. The temperature profile achieved in the two systems is reported in Fig. 5.12. The volume and the shape of the region reaching a temperature higher than 930 K (i.e., melting temperature of the phase-change material) is not the same in the two structures. In SiC the melted region in the PCL is larger and more uniform along the y axis, while in SiN the temperature decreases moving from the center (y = 0 a.u.) to the heater/encapsulation interface (y = 0.4 a.u.). This leads to a more uniform thickness of the amorphized volume in SiC with respect to SiN based devices, explaining the higher RESET resistance in SiC-PCM programmed

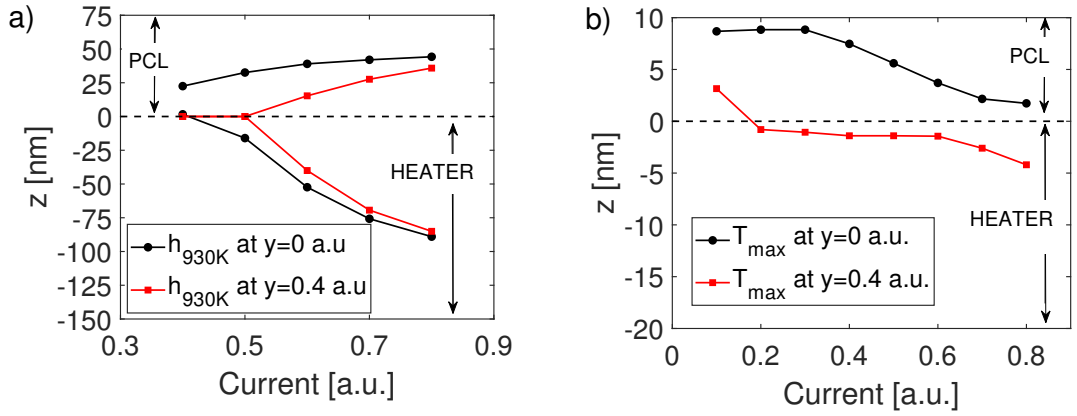

Fig. 5.13. Evolution of a) the melted region thickness h_{930K} and b) the maximum temperature T_{max} achieved at the center of the cell (y = 0 a.u.) and at the PCL/encapsulation interface (y = 0.4 a.u.) as a function of the applied current in SiN devices. The dashed line represents the interface between the heater and the PCL.

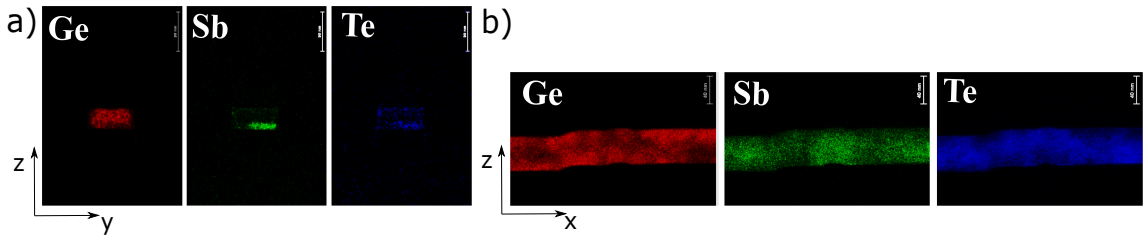

Fig. 5.14. TEM/EDX analyses performed on SiN encapsulated PCM programmed in RESET state. The elemental maps represent the distribution in the PCL of the three elements: Ge, Sb, Te in both a) zy and b) zx plane. The non uniformity of the programming in SiN devices is evidenced in particular in the zy plane analysis, where elements are not uniformly distributed over the heater/PCL interface.

at 1.2 mA (Fig. 5.11). A more specific analysis is presented in the next subsections for both SiN and SiC, describing in detail how the temperature profile changes in the PCM device as a function of the programming current.

SiN encapsulation

In order to understand the temperature profile achieved in the device, we analyzed the isotherms reaching 930 K in both the PCL and the heater and measured their distance from the PCL/heater interface (h_{930K}). The evolution of h_{930K} in the PCL and in the heater at the center of the cell (i.e., y = 0 a.u.) and at the PCL/encapsulation interface (i.e., y = 0.4 a.u.) are reported as a function of the applied current (Fig. 5.13a). SiN based PCM starts to melt at the center of the heater width for an applied current of 0.4 a.u., whereas the melting at the PCL/encapsulation interface is achieved at 0.6 a.u. Only at high current the melted thickness becomes homogeneous on the heater surface, and the heat propagation in the heater becomes really important. The position of the maximum temperature (T_{max}) along the z-axis during the programming operations in both previous analyzed regions of the cell (i.e., y = 0 a.u. and y = 0.4 a.u) is reported in Fig. 5.13b. At low current, T_{max} is localized inside the PCL at both y positions, while at increasing current the scenario changes: in the center we observe a gradual localization of T_{max} at the PCL/heater interface, while at the PCL/encapsulation interface

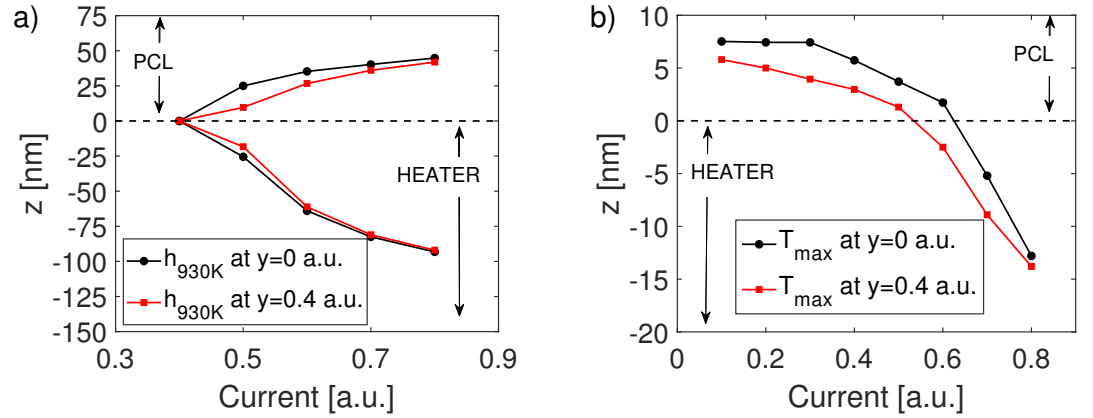

Fig. 5.15. Evolution of a) the melted region thickness h_{930K} and b) the maximum temperature T_{max} achieved at the center of the cell (y = 0 a.u.) and at the PCL/encapsulation interface (y = 0.4 a.u.) as a function of the applied current in SiC devices. The dashed line represents the interface between the heater and the PCL.

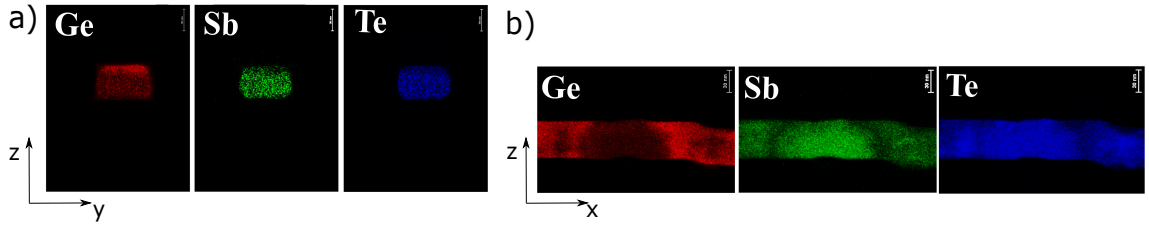

Fig. 5.16. TEM/EDX analyses performed on SiC encapsulated PCM programmed in RESET state. The elemental maps represent the distribution in the PCL of the three elements: Ge, Sb, Te in both a) zy and b) zx plane. A good uniformity of the temperature profile achieved in the device during the programming operation is confirmed in both planes.

T_{max} is already inside the heater. TEM/EDX images acquired along zx and zy plane of SiN devices programmed in the RESET state are reported in Fig. 5.14. The EDX maps along the zy plane (Fig. 5.14a) shows a not uniform active region on the top of the heater, well evident in the Sb map, compatible with what observed in simulations. On the contrary, along the zx plane (Fig. 5.14b), the elemental distribution results to be more homogeneous due to the signal integration along the whole lamella thickness, which confirms a higher elemental profile change mainly only along the y-axis. A slight evidence of the shape of the active region is however present in the Sb and Te maps.

SiC encapsulation

Same analyses performed for SiN are reported here for SiC in Fig. 5.15 (simulations) and Fig. 5.16 (TEM/EDX). The melting of the PCL is reached for both center and border at 0.5 a.u. with a h_{930K} evolution at increasing current almost identical at both y positions. This confirms that the thickness of the melted region (i.e., that becomes amorphous volume after the RESET pulse application) is uniform over the heater/PCL interface along the y-direction, as expected from Fig. 5.12b. The position of T_{max} (Fig. 5.15b) at increasing current corroborates the good homogeneity of the temperature distribution along the y-axis in the cell (i.e., well matched behavior between center and border). As observed for SiN, at low current T_{max} is localized in the

PCL, while it shifts inside the heater when the programming current is increased. The TEM/EDX of a RESET cell along zy plane (Fig. 5.16a) shows a uniform elemental distribution over the heater/PCL interface in all the Ge, Sb and Te maps. Moreover, the active volume is clearly evidenced along zy plane (Fig. 5.16b) since uniformly achieved on the whole heater/PCL surface (y-direction) and along the whole lamella thickness (of ~ 100 nm), with an elemental distribution compatible with previous works [144, 143]. Such homogeneity, achieved thanks to SiC encapsulation, is in agreement with simulations results.

5.2.3 Electro-thermal theoretical analysis and discussions

The double slope behavior evidenced in the RI characteristic of both devices in Fig. 5.11, can be correlated to the different programming scenario that is achieved in the cell for different current amplitudes. As observed in simulations, the transition of the temperature hottest point from the PCL to the heater, is the origin of the double slope. In first approximation, the electro-thermal behavior of the cell in 2D along the zy plane was described as previously reported [81]. The resistance value R achieved in the PCM device after the pulse application was expressed as a function of the amorphous thickness obtained in the cell:

$$R \simeq \int_0^{h_{am}} \rho_{am} \frac{dz}{\pi z \ w} \propto ln(h_{am}) \tag{5.2}$$

where h_{am} is the amorphous thickness, ρ_{am} the resistivity of the amorphous phase and w the width of the heater along the y direction. A uniform semi-cylindrical amorphous shape over the heater was considered. In such system, the heat distribution is driven by the stationary heat transfer equation, that can be simplified as:

$$\frac{\partial^2 T}{\partial z^2} \simeq -\frac{\rho_{ON} \ I^2}{k_{th,eff}} \tag{5.3}$$

where ρ_{ON} represents the device resistivity when the PCL is melted during the pulse application, T is the temperature along the z-axis, $k_{th,eff}$ is the effective thermal conductivity associated to the overall system, while I is the current applied to the device and which has the role to induce a specific temperature profile inside the cell thanks to the current density J achieved at the PCL/heater interface ($I = Jwt$ with t the heater thickness along the x-axis). The height of the melted region was assumed to be equal to the height of the amorphous final region ($h_{930K} = h_{am}$), therefore, from Eq. 5.3:

$$\Delta T_i \propto \frac{I^2}{k_{th,eff}} h_{am}^2 \tag{5.4}$$

where ΔT_i represents the temperature increase achieved at the heater/PCL interface with respect to room temperature. The following correlation between h_{am} and I is then valid:

$$\frac{dh_{am}}{dI} \propto \frac{\sqrt{\Delta T_i \ k_{th,eff}}}{I^2} \tag{5.5}$$

Furthermore, from the known correlation between power (P) and temperature, results:

$$\Delta T_i = R_{TH} P \propto R_{TH} I^2 \tag{5.6}$$

where R_{TH} is the global thermal resistance of the device. Both the expression of I obtained from Eq. 5.6 and the linear proportionality between R_{TH} and the reciprocal of the effective thermal conductivity of the system ($k_{th,eff}$) were plugged into Eq. 5.5 as follows:

$$\frac{dh_{am}}{dI} \propto \frac{R_{TH}\ \sqrt{k_{th,eff}}}{\sqrt{\Delta T_i}} \propto \frac{1}{\sqrt{k_{th,eff}}} \tag{5.7}$$

This correlation is in agreement with expectations, namely that the thickness of the amorphous region achieved in the cell at a specific current increases when the thermal conductivity of the surrounding materials is reduced. Therefore, since the resistance R depends on h_{am}, the slope of the RI curve of Fig. 5.11 (i.e., s_1 or s_2) can be finally correlated to the thermal conductivity of the system:

$$s = \frac{d\ ln(R)}{dI} = \frac{d\ ln(R)}{dh_{am}} \frac{dh_{am}}{dI} \propto \frac{1}{\sqrt{k_{th,eff}}} \tag{5.8}$$

The electrical results obtained from 4kb matrices were performed on totally equivalent devices, except for the different encapsulation layer. This enabled the validation of the relation in Eq. 5.8, by calculating the ratios between the slopes in Table 5.1 and correlating them with the ratios between the measured thermal conductivities. Therefore, the ratio between the two s_1 in SiC and SiN, and the two s_2 should depend only on the ratio between the thermal conductivities of the two materials. This was confirmed by the following calculation:

$$\frac{s_{1,SiC}}{s_{1,SiN}} = \frac{s_{2,SiC}}{s_{2,SiN}} = \frac{\sqrt{k_{th,SiN}}}{\sqrt{k_{th,SiC}}} \sim 1.8 \tag{5.9}$$

This evidences that the difference between the evolution of SiC and SiN RI curves is strongly related to the value of the thermal conductivity of the encapsulation layer which is in direct contact with the PCL and the heater. Therefore, the choice of the encapsulation layer is fundamental in the tuning of the zy plane temperature profile of a Wall-based PCM and further optimization can allow an even steeper slope in the RI curve, leading to a current reduction for the RESET operation.
The lower uniformity along y-axis observed in SiN devices can explain the lower I_m found in Fig. 5.11 with respect to SiC. Indeed, some amorphous residuals featuring low thermal conductivity could be generated by such non-homogeneous temperature profile, reducing the current needed to melt the active volume in the PCL. The amorphous residuals are compatible also with the increased SET resistance in SiN devices with respect to SiC.
Another validation of Eq. 5.8 was obtained by comparing the transition from s_1 to s_2 observed in both encapsulation layers. The hypothesis, confirmed in simulations, supports a transition of T_{max} from the PCL at low currents towards the heater at higher currents. This is an effect which depends on both the phase-change material electrical resistivity evolution in temperature and the amount of PCL that triggers the melting during the programming operations. Based on such hypothesis, the main change between the two regimes, in terms of materials surrounding T_{max}, would be along the x-axis, since along the y-axis the encapsulation dielectric remains unchanged. Indeed, when T_{max} is inside the PCL, it is surrounded by the phase-change material

itself along x-axis, as it is visible in the zx scheme of Fig. 5.6. In such case, the thermal conductivity of the PCL influences s_1. On the contrary, when T_{max} is localized inside the heater, it is surrounded by a SiN based dielectric (referred as "DIEL." in the scheme of Fig. 5.6) along the x-axis, with an effect on s_2. Such SiN is of the same nature as the one used for the encapsulation (i.e., PECVD) with equivalent thermal conductivity. The ratio between s_1 and s_2 is equivalent in both SiC and SiN devices:

$$\frac{s_{1,SiC}}{s_{2,SiC}} \sim \frac{s_{1,SiN}}{s_{2,SiN}} \sim 2 \tag{5.10}$$

This confirms the hypothesis of the equivalent origin of the transition between the two slopes in both encapsulation layers, namely the change of position of T_{max} at increasing current. Therefore, it would mean that:

$$\frac{s_1}{s_2} = \frac{\sqrt{k_{th,SiN}}}{\sqrt{k_{th,PCL}}} \sim 2 \quad \rightarrow \quad k_{th,PCL} \sim 0.37\ W/mK \tag{5.11}$$

This result is in agreement with previous works reporting the thermal conductivity of fcc GeSbTe alloys [145, 146]. The GGST faces phases segregation after BEOL process [143, 144], therefore, the thermal conductivity value found in our calculation is in agreement with the presence of grain boundaries and residual amorphous regions in the PCL, outside the active volume. In addition, since the thermal conductivity of crystalline Ge is higher than the fcc GeSbTe one, the thermal transport in the GGST system should be driven by the GeSbTe phase segregated, justifying the $k_{th,PCL}$ value obtained in Eq. 5.11.
This last result highlights the high importance of the engineering of the dielectrics surrounding the heater in a Wall structure, in order to make the programming operation more efficient. For a given PCL, the thermal conductivity of the encapsulation layer influences the steepness of s_1, while the thermal conductivity of the dielectrics surrounding the heater influences s_2. In a Wall PCM structure featuring a highly resistive heater element, T_{max} is localized inside the heater at each programming current. As a result, the slope s_2 dominates the RI characteristic and the engineering of the dielectrics surrounding the heater becomes fundamental to drastically reduce the programming current.

5.2.4 Discussions and conclusions

In this section, the optimization of the thermal confinement of a heater based Phase-Change Memory (PCM) integrating a Ge-rich Ge Sb Te alloy (GGST) by the engineering of the encapsulation dielectric layer was presented. In particular, the lower thermal conductivity of a SiC based encapsulation layer, demonstrated an improvement of the thermal confinement during the programming operations of the device. Thanks to electrical characterization, the performance of thermally improved PCM devices was investigated, showing higher programming efficiency, higher SET programming speed and data retention higher than one hour at 250 °C. The results were supported by 3D electro-thermal simulations and TEM/EDX analyses, which linked the effects of the higher thermal confinement achieved in SiC-PCM to the shape of its amorphous volume.

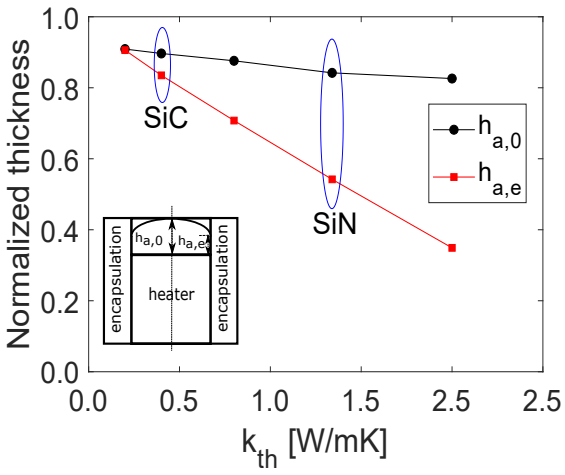

Fig. 5.17. Simulation of the evolution of the thickness of the amorphous volume in the PCM as a function of the k_{th} of the encapsulation layer, in the middle ($h_{a,0}$, i.e., h_a calculated at y = 0) and at the edge of the PCM ($h_{a,e}$, h_a at the encapsulation layer interface y_e). Programming efficiency at low k_{th} values (i.e., in SiC-PCM) is confirmed by the achievement of a more homogenous amorphous layer (center wrt edge).

This result grown the interest to study the PCM thermal response while further reducing the encapsulation layer thermal conductivity. Therefore, a simulation study was performed by looking at thermal conductivity values ranging from 0.2 W/mK up to 2 W/mK, to evidence the temperature profile evolution with k_{th} and trigger the advantage to reduce the k_{th} value below the SiC one.
The evolution of the simulated thickness of the amorphous region respectively in the middle ($h_{a,0}$) and at the edge ($h_{a,e}$) of the phase-change material as a function of the encapsulation layer k_{th} is reported in Fig. 5.17. The amorphous volume becomes more uniform when the k_{th} of the encapsulation layer is reduced below 0.4 W/mK. Nevertheless, the simulation suggests that reducing the k_{th} beyond this value does not represent anymore a great advantage in Wall-based PCM, since the active volume is already close to have a constant amorphous thickness (i.e., $h_{a,0} \sim h_{a,e}$).
In addition, the proposed theoretical electro-thermal model described the temperature profile evolution in the cell during the programming operation, exploiting the key parameters controlling the electro-thermal response of the device. In particular, it was demonstrated that the thermal conductivity of the PCL (in the zx-plane) and of the encapsulation (in the zy-plane) influence the temperature distribution in the device when the hot point is localized in the PCL. While the dielectrics material surrounding the heater in both the directions control the temperature response at higher current values (i.e., when the point of maximum temperature is moved in the heater). This result highlights the fundamental role played by the dielectric materials in direct contact with the heater, especially when the heater is highly resistive (i.e., the hot point lies in the heater since the beginning of the programming of the cell).

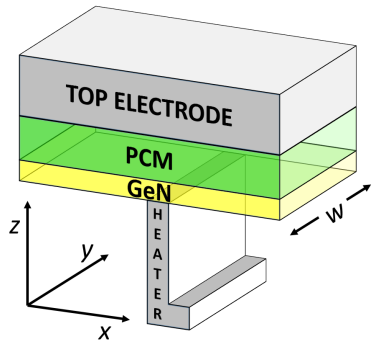

Fig. 5.18. Simplified schematic of the as fabricated SNC-PCM Wall device based on a GeN/GeSbTe stack.

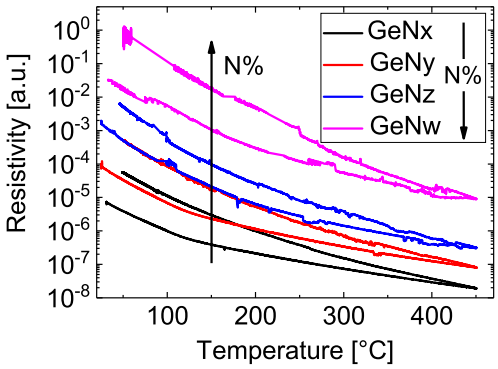

Fig. 5.19. N concentration tuning in GeN layer. The higher the N concentration from x to w, the higher the resistivity.

5.3 GeN interfacial layer

Several solutions were proposed so far with the aim to reduce the programming current in PCM as already mentioned in Ch. 2. Despite the promising results, these solutions still rise doubts about the technology cost, its scalability in industrial devices, the material evolution control during Back-End-Of-Lines (BEOL) fabrication steps, and the material degradation along cycling especially in scaled PCM. PCM stacks based on oxide interfaces was proposed to reduce the programming current [95], but without scaling capability demonstration and a possible detrimental oxygen impact on the integrity of the chalcogenide material [141][142]. In this work, a Self-Nano-Confined PCM (SNC-PCM) solution is proposed. It is based on an optimized oxide-free GeN/GeSbTe stack integrated in state-of-the-art Wall PCM (Fig. 5.18). The SNC-PCM functionality relies on the soft breakdown of the GeN layer performed as a first step (i.e., initialization) on as fabricated devices. The reliability of such electrical initialization depends on the layer uniformity, its resistivity and the tuning of the electric field required. The GeN layer was engineered by exploiting different N contents and thicknesses in order to tune its resistivity, the electric field needed to initialize the layer, and its stability at high temperature targeting the BEOL compatibility and best device performances. The resistivity as a function of temperature measured by the four point probe method is reported in Fig. 5.19 and it shows the increase of the resistivity with N content. An intermediate N content was finally chosen for integration in electrical devices, featuring the right compromise in terms of resistivity even after annealing at 450 °C. The GeN/GeSbTe optimized stack was integrated by magnetron sputtering in 4 kb arrays of state-of-the-art Wall-based PCM devices fabricated in the BEOL of the fabrication of LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology, for statistical electrical parameters evaluation. The devices have a nominal width (w) ranging from 50 nm up to 300 nm and their electro-thermal behaviour is studied in details by the use of both electric test and 3D simulations.

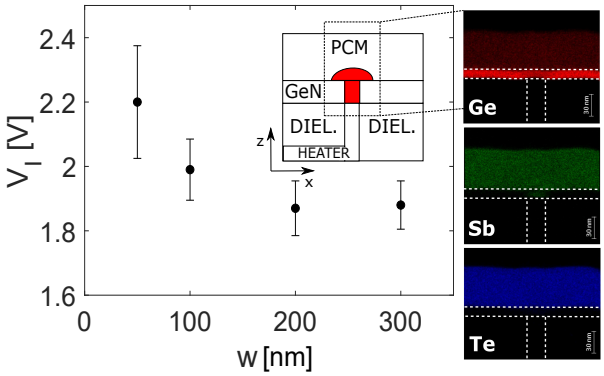

Fig. 5.20. left) Mean and $\pm 1\sigma$ values for the initialization voltage (V_I) measured in arrays as a function of w); right) TEM/EDX (xz plane) analysis of a device initialized at 1.2 mA, showing the SNC phenomenon and the absence of elemental segregation. The inset schematizes the shape of the active volume of the SNC-PCM.

5.3.1 Electric test

Preliminary tests were performed on 4 kb arrays to confirm the GeN layer integrity and the device functionality. The initialization voltage (V_I), used to supply the Bit Line of the arrays, showed a slight evolution and a low variability with respect to w (Fig. 5.20). The slight decrease of V_I observed while increasing w is associated to the known phenomenon of materials dielectric strength change with material shape and size [147]. The inset in Fig. 5.20 describes the initialization mechanism, showing in red the region involved in the programming of the cell after the initialization procedure (i.e., the active volume). The TEM/EDX analysis after initialization reported in the same figure confirms the diffusion of Ge, Sb and Te in the GeN constriction with the formation of a GeSbTe confined region without facing any material segregation. This supports the

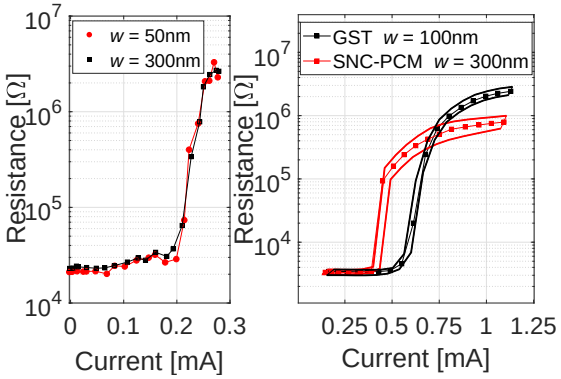

Fig. 5.21. left) 1T1R RI characteristics for 50 nm and 300 nm devices obtained with 10/300/10ns staircase pulses. Size-independency of SNC mechanism is here verified with I_R of about 250 µA; right) Median and $\pm 1\sigma$ values for RI data comparing the behavior of a SNC-PCM (with w equal to 300 nm) with respect to standard PCM (w equal to 100 nm) based on $Ge_2Sb_2Te_5$ (GST).

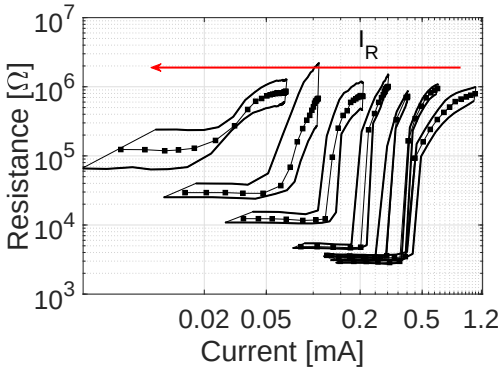

Fig. 5.22. Median and $\pm 1\sigma$ values for the RI characteristics in log-log scale obtained in 4 kb arrays at different I_Rs. SNC-PCM devices demonstrate a programming current reduction down to 50 µA.

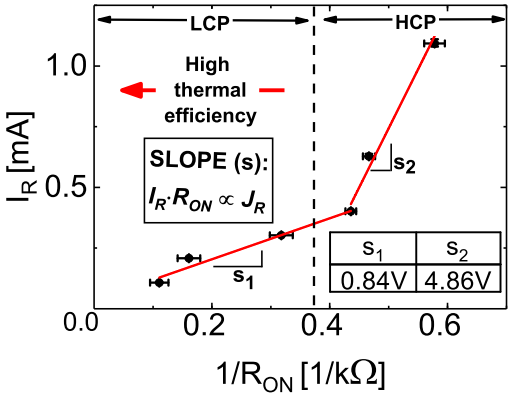

Fig. 5.23. Median and $\pm 1\sigma$ values for the RESET current (I_R) as a function of the inverse of the dynamic device resistance (R_{ON}) in 4 kb arrays. The different slopes evidence the lower current density (J_R) needed to program devices initialized with low I_R (LCP) with respect to the ones for which a high I_R is used (HCP). A lower slope in LCP population is highlighting a better thermal efficiency of the programming operation in such SNC-PCM devices.

idea that the SNC mechanism is taking place in our devices.
Resistance as a function of current characteristics of 1T1R devices initialized at 250 µA demonstrated that the SNC-PCM mechanism is independent from the device size w (Fig. 5.21 left)), showing identical RI for device widths of 50 nm and 300 nm when initialized with the same current. The main advantage is that the mechanism can be tuned by controlling the current that flows in the device during the initialization step thanks to the transistor integrated in series to it. Therefore, the initialization step had the role to define both the critical dimension (CD) and the RESET current of the devices. The initialized devices were firstly programmed in the SET state with a squared pulse SP (i.e., rise/width/fall time equal to 10 ns/300 ns/10 ns). The resistance increase towards the RESET state was obtained with a staircase-up sequence of SPs of increasing amplitude with steps of 0.1 V.
Furthermore, in Fig. 5.21 the RI characteristics obtained in 4 kb arrays for SNC-PCM are compared with respect to the standard GST cell. It shows that the same programming current in both the devices (1.2 mA) is obtained only if the w of a standard cell is reduced by a scale factor of three. The steeper SET-RESET transition in SNC-PCM is a particular evidence of the confined structure achieved thanks to the initialization step, while the lower RESET resistance is associated to the dominant contribution of the GeN resistance in parallel with the GST programmed region.
By tuning the current at the initialization, it was possible to obtain seven different RI characteristics (Fig. 5.22) and show that the SNC mechanism can take place down to RESET current of 50 µA. The SET resistance increase at low I_R is a clear evidence of the smaller diameter achieved during the initialization process. The use of smaller transistor can allow a more slight tuning of the current values and can potentially give the possibility to initialize and program the device with a lower current.
By taking into account the inverse proportionality between the dynamic resistance of the devices (R_{ON}) and the area of the initialized confined region of the GeN layer, it is possible to consider:

$$I_R \cdot R_{ON} \propto J_R \tag{5.12}$$

where I_R is the RESET current and J_R is the associated current density. The I_R as a function of the inverse of R_{ON} is reported in Fig. 5.23, which highlights the evolution of J_R in the different device populations. The data can be divided in two regions each one characterized by a different slope (s_1 and s_2). The lower value of s_1 is correlated to the J_R reduction in devices belonging to the Lower Currents Population (LCP) leading to a better thermal efficiency with respect to the devices in the High Currents Population (HCP).
The analysis on the SET programming speed is reported in the SET cartographies of Fig. 5.24 performed on 1T1R devices from LCP (I_R equal to 100 µA) and HCP (I_R equal to 1.2 mA). The test was performed by acquiring the resistance achieved in the cell after the application of a RESET pulse followed by a SET pulse (with a fixed pulse width of 300 ns, and increasing fall time and amplitude). The dashed lines in the figure represent a linear fit used to evaluate the current over time ratio (dI/dt) needed during the pulse fall time to reliably SET the cell (i.e., to decrease the resistance value threefold with respect to the RESET state). The optimal dI/dt (i.e., dI/dt_{SET}) ratio was more than two times lower in devices belonging from LCP, revealing the need of an optimized SET pulse to fulfill the specific requirement.
Data retention tests on RESET and SET states were performed for the two populations LCP and HCP under investigation. Both the standard SET and the optimized SET were compared in terms of retention. The RESET state (Fig. 5.25) shows a comparable behavior for both the high and low initialization currents, with a resistance drift at 85 °C and a beginning of recrystallization at 200 °C, confirming the preservation

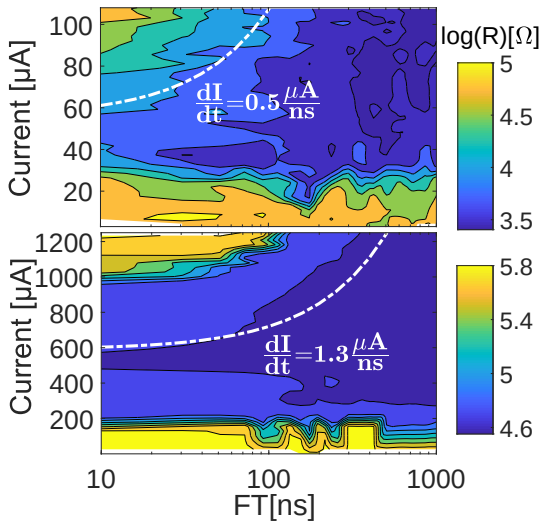

Fig. 5.24. SET cartographies showing the SET resistance evolution as a function of the pulse fall time (FT) (x-axis) and of the pulse current (y-axis). The results are reported for top) a 1T1R device initialized at 100 µA and bottom)1.2 mA. The slope dI/dt needed to reliably SET the cell (i.e., equal to dI/dt_{SET} used to achieve a 3x RESET resistance lowering) is more than two times lower in SNC-PCM owning to LCP.

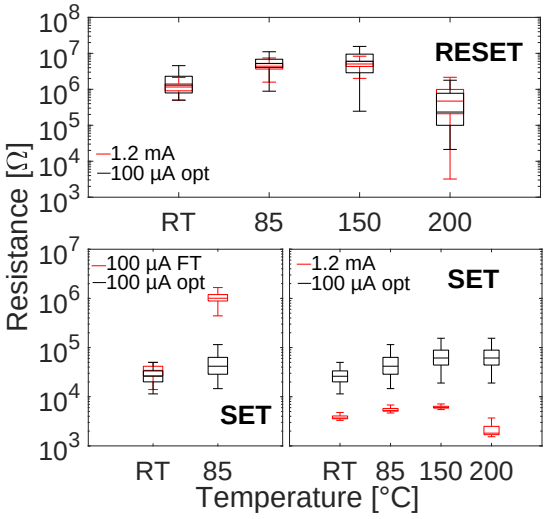

Fig. 5.25. top) RESET and bottom) SET data retention performed by isochronal annealing of one hour at increasing temperatures on 4 kb arrays with I_R of 1.2 mA and 100 µA. The RESET retention performances are comparable for the two SNC-PCMs. SET stability is ensured by SET-opt protocol, since a standard FT strategy leads to a high resistance drift already at 85 °C.

of the material properties even in nm-scale SNC-PCM. The comparison between the standard (SET-FT) and optimized SET (SET-opt) showed that the optimized SET protocol helps reducing the resistance drift faced as soon as the temperature is increased, certifying the higher crystalline homogeneity obtained in the confined region of the SNC-PCM device with respect to the standard pulse.
The result achieved with the optimized pulse is also evidenced in the subthreshold conduction analysis (Fig. 5.26). In particular, the LCP device programmed with a SET-opt procedure revealed a reliable ohmic behavior, comparable with the device initialized at higher current and programmed with a standard pulse. On the contrary, the 100 µA device programmed in SET state with a standard pulse showed an exponential conduction, that can be correlated with a non-uniform crystalline or partially amorphous structure having trap-dominated conduction [26].
The endurance was performed to study the material evolution along cycling for two LCP devices (i.e., initialized at 200 µA, 650 µA) and one HCP device (i.e., initialized at 1200 µA). The comparison was made detecting when the resistance window starts to be reduced in particular because of the RESET resistance decreasing. The percentage of devices facing such starting of degradation is reported as a function of cycling in Fig. 5.27. It shows that the degradation starts at 10^6 cycles for devices with I_R equal to 650 µA and 1200 µA (HCP), while in SNC-PCM featuring the lower I_R (LCP) the same order of degradation was observed only at 10^8 cycles. To be noted that in all the tests performed, all the devices kept at least a resistance window of one order of magnitude after 10^6 cycles. Furthermore, the measured degradation was accelerated by the use of the same pulses (RESET: 10 ns/300 ns/10 ns and SET: 10 ns/300 ns/10 µs) for the three populations at the maximum I_R. Therefore, this result is even more representative of the high reliability of SNC-PCM devices, that could feature higher endurance if benefiting of optimized or intelligent cycling algorithms [148]. The resistance evolution

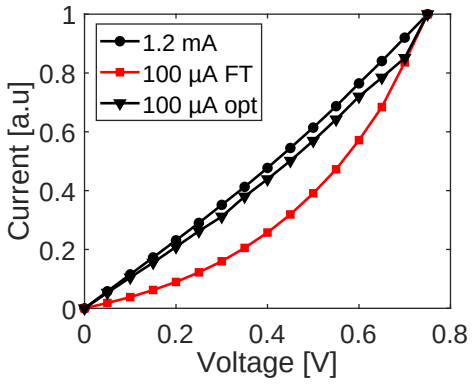

Fig. 5.26. Normalized subthreshold IV curves for 1T1R devices programmed at 1.2 mA (HCP) and 100 µA (LCP). The device from the LCP are programmed with both a standard SET (100 µA FT) and an optimized SET (100 µA opt) protocol. The ohmic behavior observed in HCP devices is achieved in LCP ones only with optimized SET protocol.

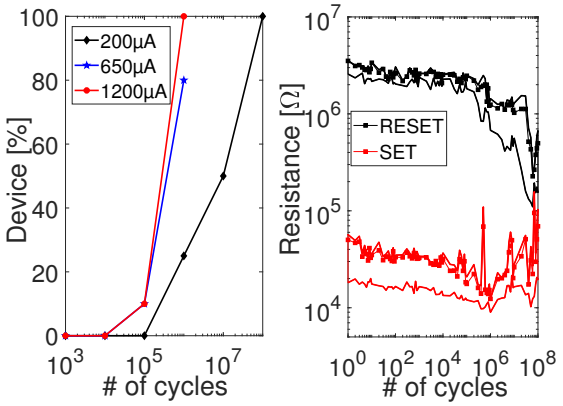

Fig. 5.27. Device endurance analysis showing the statistics for the starting of the resistance window degradation, detected as a 3x reduction of the starting RESET resistance, for three different values of initialization current I_R. Ten devices has been tested for 650 µA and 1200 µA population and four for the 200 µA due to their best endurance performance up to 10^8 cycles.

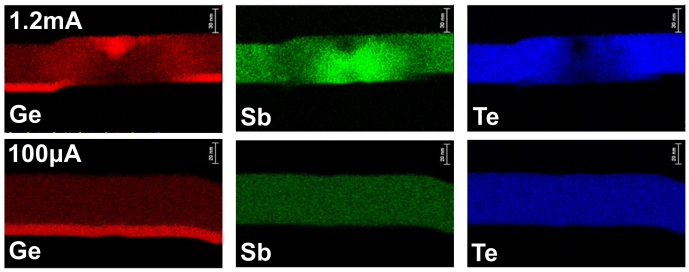

Fig. 5.28. TEM/EDX Ge, Sb and Te cartographies for SNC-PCM cycled 10^6 times, respectively at top) 1.2 mA and bottom) 100 µA. At 1.2 mA the GeN layer degrades along cycling with strong elemental segregation. On the contrary, 100 µA device does not show signs of degradation (programmed region not visible because of its nm-dimension).

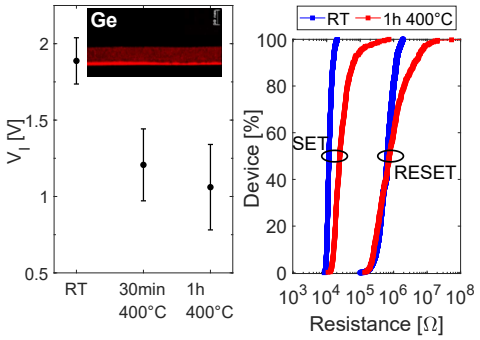

Fig. 5.29. Results of BEOL like thermal stress at 400 °C. GeN layer integrity is confirmed by TEM/EDX analysis (inset). V_I is lowered at around 1 V after annealing. SNC mechanism is preserved, as demonstrated in SET/RESET distributions for I_R = 200 µA, compared before and after annealing.

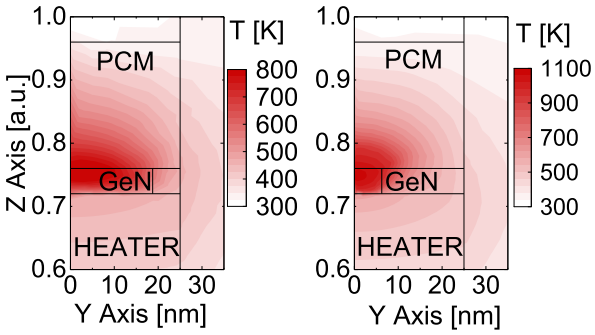

Fig. 5.30. Temperature profile simulated for SNC-PCM with CD of left) 37.5 nm and right) 12.5 nm using the same current density J. Higher temperature is achieved in smaller SNC-PCM thanks to its higher thermal efficiency.

along cycling for a RESET current of 200 µA is reported in Fig. 5.27, highlighting the type of RESET lowering observed independently from the initialization current applied (i.e., the same RESET lowering mechanism is taking place at a different number of cycles).

The device degradation under cycling was studied by TEM/EDX cartographies, performed on devices cycled up to 10^8 cycles for both I_R of 1.2 mA and of 100 µA (Fig. 5.28). The analysis confirmed the higher level of segregation triggered after 10^6 cycles in HCP devices, while no sign of degradation appeared in LCP where the GeN layer was still uniform after cycling. To be noted that the signal reduction due to the presence of the filament is quite small in the device programmed at 100 µA , because of the signal integration along the width of the lamella used for the analysis.

The SNC-PCM stability was verified after a BEOL like thermal budget of 1h at 400 °C. By increasing the annealing time, the GeN layer faced a structural reorganization [149], which induced the V_I lowering (Fig. 5.29). Nevertheless, the TEM/EDX image (inset) and the SET/RESET distribution for 200 µA cells showed that the GeN layer integrity is kept even after an annealing of one hour at 400 °C and the devices can be programmed with a similar resistance window.

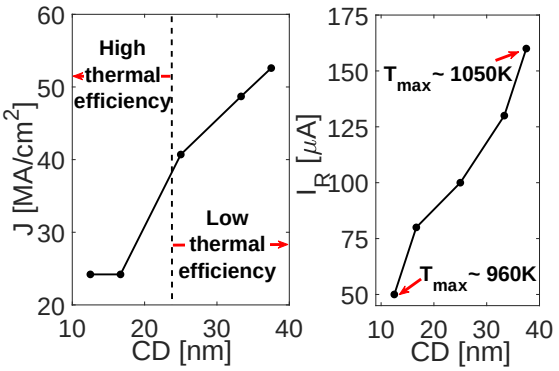

Fig. 5.31. left) Simulated J needed to achieve the melting of the material as a function of CD. J is lower in small CD in accordance with Fig. 5.23; righ) simulated I_R as a function of CD, showing that the maximum temperature (T_{max}) achieved during RESET operation is lower for smaller CD. The CD extracted at a I_R of 50 µA is of around 12 nm.

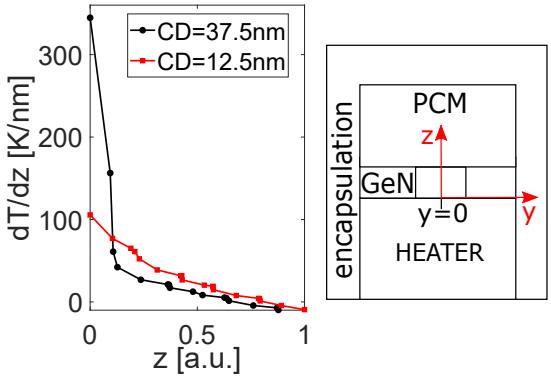

Fig. 5.32. Simulated temperature gradient along z-axis (dT/dz) in the confined region of SNC-PCM (at y = 0) for two devices featuring different CD size. A higher temperature homogeneity (i.e., lower dT/dz) is achieved in highly scaled confined SNC-PCM featuring small CD.

5.3.2 Electro-thermal simulations

3D electro-thermal simulations were performed in COMSOL Multiphysics [137] and run on SNC-PCM with different critical dimensions.
Fig. 5.30 represents the temperature profile reached in the PCM at the same current density J for devices having a CD of 12.5 nm (representative of the LCP) and of 37.5 nm (representative of the HCP). A higher maximum temperature is achieved in devices with the smaller CD, highlighting the higher thermal efficiency of SNC-PCM featuring lower I_R.
Fig. 5.31 shows that the simulated current density at the melting of the PCM material increases with CD, in accordance with experimental results previously reported in Fig. 5.23. Furthermore, it highlights that the higher J leads to a higher maximum temperature, which is likely responsible for a faster degradation of the material, as observed in the endurance tests and TEM/EDX image (Fig. 5.27 and Fig. 5.28) of the devices initialized with high I_R. Moreover, the analysis performed on the temperature uniformity inside the constriction generated in the GeN layer, showed a lower temperature gradient dT/dz (i.e., higher uniformity) in devices with small CD (Fig. 5.32). This result can be directly linked with the difference in the dI/dt ratio presented in Fig. 5.24. Indeed, when an electric pulse is applied to a PCM device having a specific R_{th}, the temperature increase ΔT (i.e., T-T_0, with T_0 being room temperature) is proportional to the current flowing into it, according to the following relation:

$$\Delta T = R_{th} R_{ON} I^2 \tag{5.13}$$

During the application of the pulse, both temperature and current are time dependent variables, hence their variation in time can be expressed as:

$$\frac{d}{dt}(T - T_0) = \frac{d}{dt} R_{th} R_{ON} I^2 = 2 I R_{th} R_{ON} \frac{dI}{dt} \tag{5.14}$$

During the pulse fall time, the solid-liquid boundary evolution in time (dz/dt) needs to descend with a rate lower or equal to the crystallization speed (v_g), to achieve a reliable SET. This condition can also be expressed as:

$$\left(\frac{dT}{dz}\right)^{-1}\frac{dT}{dt}\bigg|_{SET} \leq v_g \tag{5.15}$$

where dT/dz represents the temperature gradient along z. Hence, in order to reliably SET the device, at least the equality of Eq. 5.15 should be satisfied. By combining Eq. 5.14 with Eq. 5.15 it is possible to find out that the current over time rate reduction during the fall time of the SET pulse need to satisfy the following condition:

$$\frac{dI}{dt}\bigg|_{SET} \propto v_g\frac{dT}{dz} \tag{5.16}$$

Therefore, the improved temperature uniformity in smaller CD observed in our simulations (Fig. 5.32) explains the lower dI/dt_{SET} measured in devices initialized at low current and featuring small CDs. This result supported the need for an optimized SET protocol in extremely confined devices, like in SNC-PCM.

5.3.3 Discussions and conclusions

The PCM integrating a GeN interfacial layer demonstrated a RESET current reduction down to 50 μA, without any dependence on the device size when integrated in a 130 nm CMOS technology (i.e., no need of aggressive lithography to achieve low power). This result is very encouraging since previous work performed on PCM arrays presented a minimum RESET current of 100 μA achieved either with not scaled devices (critical dimension CD equal to 200 nm) [150] or extremely scaled one (CD equal to 20 nm) [151] but expensive because of complex fabrication. The results presented in this section are supported by detailed Transmission Electron Microscopy (TEM) images, Energy-dispersive X-ray spectroscopy (EDX) analyses and 3D TCAD electro-thermal simulations, revealing an effective scaling of the analyzed PCM down to about 12 nm with endurance tested up to more than 10^8 cycles.
The devices tested in this work are integrated with a 130 nm transistor technology, therefore, it is not possible to ensure a fine current control for values lower than 50 μA. As a consequence, it is not possible to define the minimum current required to ensure the device working principle. Nevertheless, the integration of this solution on a smaller technology node open the possibility to generate a stronger self nano-confined phenomenon due to a finer control in current during the initialization step, which can lead to even lower power performances.
Furthermore, the devices feature high stability and integrity even during BEOL fabrication (one hour at 400 °C) which makes them suitable for industrial applications.
The SNC-PCM shows high versatility: it can both be used for high or low density applications (i.e., it is size independent), while keeping the working principle still reliable. Moreover, the structure can be further optimized by tuning the N content and thickness of the GeN layer, which define the initialization voltage.

5.4 PCM for aerospace applications: tolerance to radiation

As mentioned in Section 2.2, the radiation tolerance in phase-change materials and PCMs was foreseen since their discovery [9], due to their storage mechanism not based on charge as in Flash Memories; nevertheless, further studies described some possible degradation mechanisms associated to radiation effect which are not yet fully understood and could impact the PCM depending on its device structure, in particular in highly scaled devices. Therefore, it is interesting to investigate weather the scaled PCM devices fabricated in CEA-LETI with a 130 nm CMOS technology can be affected by radiations, to target aerospace applications. In this thesis, the heavy ion radiation effects on the structural changes of the material successively integrated as active layer is firstly investigated. Then, SET and RESET states evolution under different irradiation fluences in 4kb arrays is presented and correlated with the morphological analysis previously performed on the active layer material. Furthermore, a standard PCM stack is compared with the GeN interfacial layer PCM one (SNC-PCM) to trigger a possible dependence of the performance from the different device architecture. All the heavy-ion irradiation experiments reported in the following sections were performed at the beam facility of GSI Darmstadt (Germany).

5.4.1 Radiation effect on GST alloys structure

The evolution of amorphous (as deposited) and crystalline (obtained by annealing at 450 °C for 15 min) structures of phase-change layers under ion beam irradiation was investigated by XRD and TEM/EDX analyses. The 100 nm thick films were deposited on Si substrate and protected from air exposure by a 10 nm SiN encapsulation layer. The samples were irradiated with Au ions with an energy of 1.635 GeV at different fluences (from 10^9 up to 10^{13} ions/cm^2) with a constant flux of $3{\cdot}10^8$ ions/(cm^{2}s).
The evolution of the as deposited GST and GGST structures with increasing beam fluence is reported in Fig. 5.33a and Fig. 5.33b. The analysis shows a crystallization of GST toward a cubic phase between $5{\cdot}10^{10}$ and 10^{12} ions/cm^2 (Fig. 5.33a. The crystallization triggered at high fluences is confirmed by TEM and nano-diffraction analysis (Fig. 5.34a revealing the growth of large crystals in the system, compatibly with the sharpness of the XRD peaks detected. Most probably the two main mechanisms that are competing in the material structure when subjected to ions irradiation are: i) the breaking of crystalline bonds; ii) a localized temperature increase that could induce nucleation and growth phenomena, if the temperature reached is higher than the T_c. XRD results for GST seems to confirm that the second mechanism is predominant at the investigated fluences. In GGST, on the contrary, the amorphous phase is preserved even at high fluences, confirming the higher thermal stability of the material. Fig. 5.33c and Fig. 5.33d show the XRD patterns of GST and GGST layers annealed at 450 °C. The annealing brings the GST in the hexagonal phase (h) that is preserved (Fig. 5.33c up to high fluences. However, at $5{\cdot}10^{12}$ ions/cm^2 a broadening and shift of the hexagonal peaks is observed, confirming the competition between bonds breaking and recreation. In GGST (Fig. 5.33d), the Ge and GST cubic peaks, detected after the annealing, are gradually vanishing above 10^{12} ions/cm^2. It indicates an overall

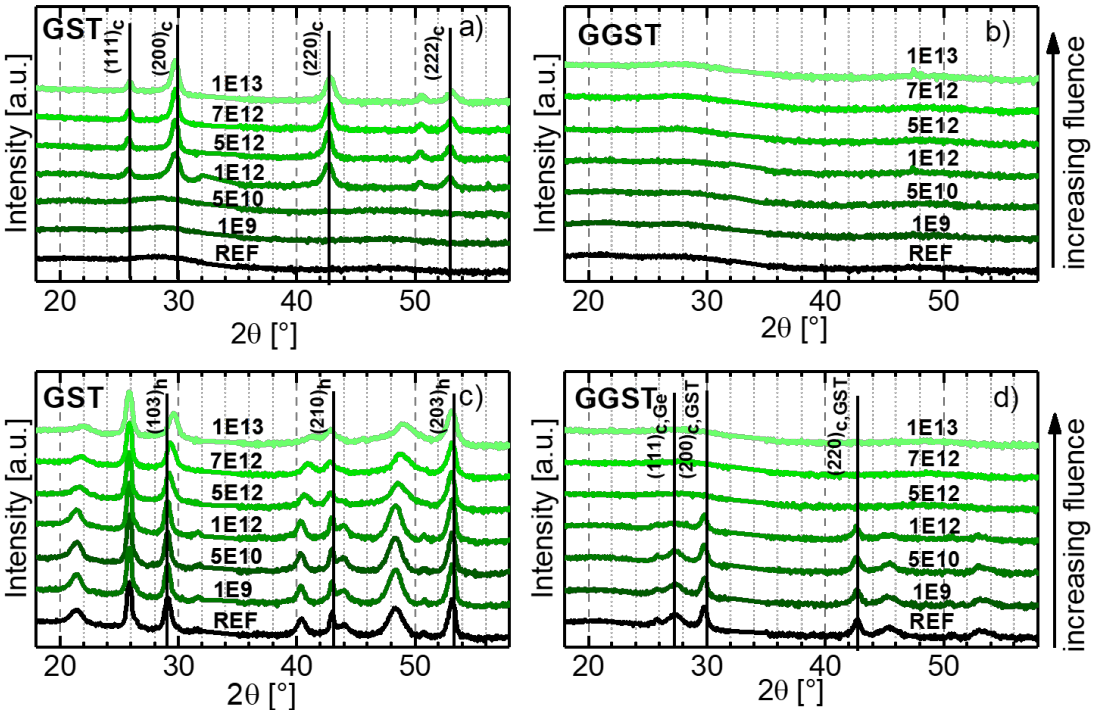

Fig. 5.33. XRD patterns of a) GST and a) GGST amorphous layers before (REF) and after irradiations at increasing fluence (reported in the spectra in ions/cm^2). XRD peaks corresponding to GST cubic phase are highlighted; XRD patterns of c) GST and d) GGST crystalline layers (after annealing at 450 °C 15min) before (REF) and after irradiations at increasing fluence (reported in the spectra in ions/cm^2). XRD peaks corresponding to the GST hexagonal phase (h,GST) are highlighted in a) and GST cubic (c,GST) and Ge cubic (c,Ge) phase in b).

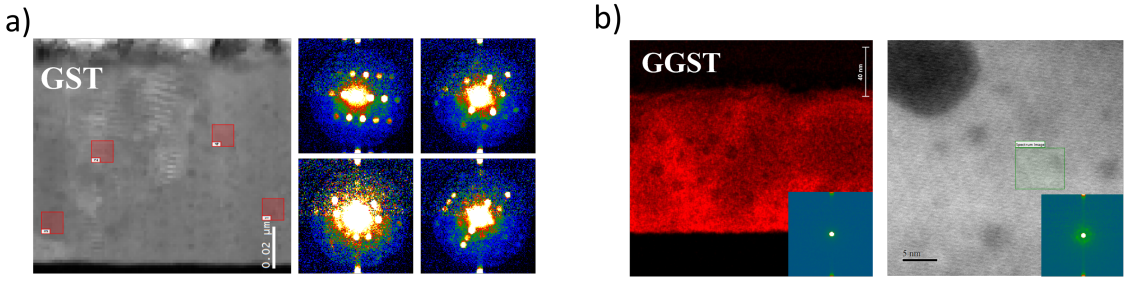

Fig. 5.34. a) TEM and nano-diffraction patterns analyses of as-deposited amorphous GST after irradiation at a fluence of 10^{13} ions/cm^2. It evidences the creation of a crystalline structure with large crystalline grains; b) TEM/EDX and nano-diffraction patterns analyses of crystalline GGST after irradiation at a fluence of $7 \cdot 10^{12}$ ions/cm^2; b)-left) the Ge segregation, induced by annealing, remained unchanged after irradiation; b)-right) the main irradiation impact is on the crystalline morphology with the reduction at nm scale of the crystals size, as evidenced by few and low intensity nano-diffraction patterns identified.

amorphisation of the crystalline phases, which is known to induce phase separation in GGST.

TEM/EDX analysis (Fig. 5.34b) performed on the irradiated samples confirms the preservation of the segregated morphology of GGST even after irradiation. However, almost no crystalline patterns are detected. By pushing nano-diffraction patterns analysis at its limit, few and low signal nm-scale features can be highlighted, confirming

a residual polycrystalline nature of both Ge and GeSbTe phases and the macroscopical amorphisation process observed by XRD, extremely impacted by irradiation at high fluences. The preserved short range order in the layer, can be the origin of the XRD feature observed between 25° and 35°, present also in several chalcogenide amorphous layers. Since the crystallization in GGST is slower with respect to standard GST (i.e., at the origin of GGST higher thermal stability), the impact of irradiation on GGST crystalline samples can be interpreted as a confirmation of the higher bonds breaking rate with respect to nucleation and growth.

5.4.2 Radiation effect on 4kb PCM

The behavior of 4kb matrices integrating both GST and GGST based PCM were investigated and compared before and after irradiations at different fluences. Moreover, the standard GST stack was compared in terms of radiation tolerance with the SNC-PCM presented in Section 5.3. PCM arrays programmed in both SET and RESET state were read after irradiation experiments at fluences of 10^9, $5{\cdot}10^{10}$ and 10^{12} ions/cm^2, with same experimental conditions described in Section 5.4.1. All the arrays irradiated

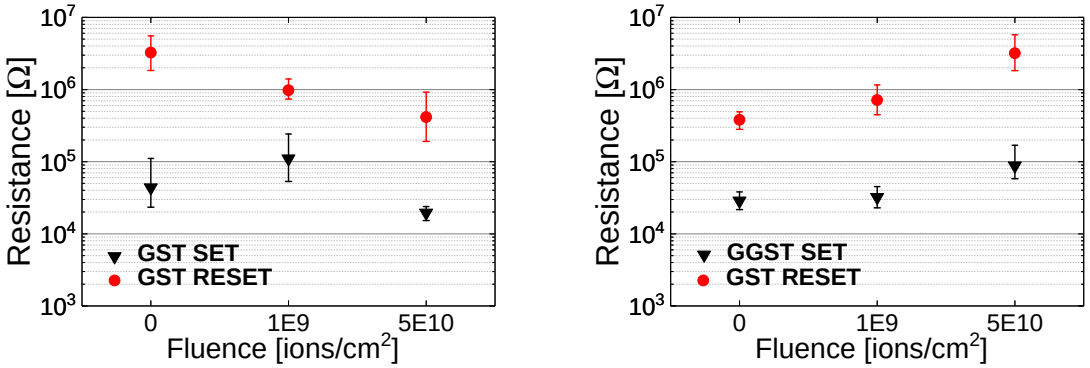

Fig. 5.35. Median and $\pm\sigma$ for SET and RESET distributions in GST and GGST 4kb arrays before and after irradiations at increasing fluences.

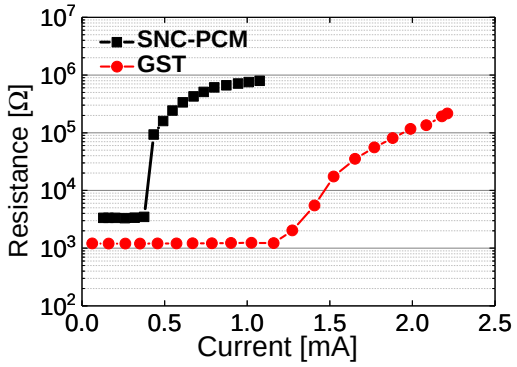

Fig. 5.36. Resistance vs Current characteristics comparing a standard GST device with an SNC-PCM. SNC-PCM shows a high current reduction wrt GST in devices featuring same critical dimension

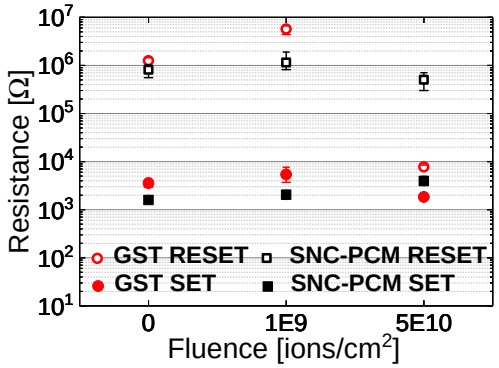

Fig. 5.37. Median and $\pm\sigma$ for SET and RESET distributions in GST and SNC-PCM 4kb arrays before and after irradiations at increasing fluences.

at 10^{12} ions/cm^2 showed the inaccessibility of the PCM cells due to the strong impact of heavy ions on the addressing circuitry. It is worth to notice that, in this work, the use of high fluences in a short time induces a higher damage of CMOS devices and external circuitry with respect to an harsh radiation environment situation where the fluence and the flux are generally smaller [122]. All the data reported in the following discussions are hence referred to the two lower fluences.
The median and $\pm\ \sigma$ for the SET and RESET distributions measured in GST and GGST arrays are reported in Fig. 5.35. The analysis was performed on devices with an electrode area of 10^{-3} μm^2. The SET state in GST faces a structural relaxation at a fluence of 10^9 ions/cm^2, highlighted by the increase of the resistance, whereas it shows a reduction (i.e., recrystallization) at a resistance comparable with the initial one at $5{\cdot}10^{10}$ ions/cm^2. This is in agreement with the incoming crystallization observed in the material analysis at high fluences. The loss of the programmed state is more evident in the GST RESET resistance value that decreases with increasing fluence, due to the incoming crystallization of the amorphous phase. On the contrary, both SET and RESET states in GGST show structural relaxation (known to be higher wrt GST [29]) at both fluences. The higher thermal stability of GGST hinders the crystallization phenomena and the loss of information even at a fluence of $5{\cdot}10^{10}$ ions/cm^2. Indeed, both the resistance window and the amorphous phase in the RESET state result to be preserved.
Finally, the radiation tolerance of a standard GST stack is compared with an innovative SNC-PCM stack integrated in Wall devices featuring an electrode area of $3{\cdot}10^{-3}$ μm^2. The advantageous lower programming current in SNC-PCM is highlighted in Fig. 5.36 and achieved thanks to the intrinsic active volume reduction in this structure. SNC-PCM shows a higher radiation tolerance with respect to GST Fig. 5.37. Indeed, while the SET state remains stable in both stacks at all fluences, the RESET state shows a complete recrystallization at $5{\cdot}10^{10}$ ions/cm^2 with the loss of the resistance window in standard GST stack. SNC-PCM on the contrary preserves a good resistance window even at the highest fluence. Indeed, a higher thermal stability is expected in reduced amorphous chalcogenide volumes, due to a reduced nucleation rate. Moreover, the reduced electrode effective surface of a SNC-PCM, makes the device less sensible to local heating phenomena that could be induced by ion interactions with the electrode/phase-change material interface [152][153].

5.4.3 Irradiations conclusions

In this section, a comparison between the radiation tolerance of GST and GGST phase-change materials is presented. The two main competitive mechanisms induced by irradiation are highlighted thanks to the physico-chemical analyses on irradiated amorphous and crystalline layers. These mechanisms are: the bonds breaking and the crystallization induced by local temperature increase. As a resut, GST faces a dominant crystallization at high fluences, while GGST, being more thermally stable, features a higher structural relaxation and a gradual reduction of the long range order, which is demonstrated by the gradual loss of the crystalline structure.
The analysis performed on state-of-the-art 4kb PCM array demonstrated the higher radiation tolerance of GGST devices with respect to the GST one, showing no recrystal-

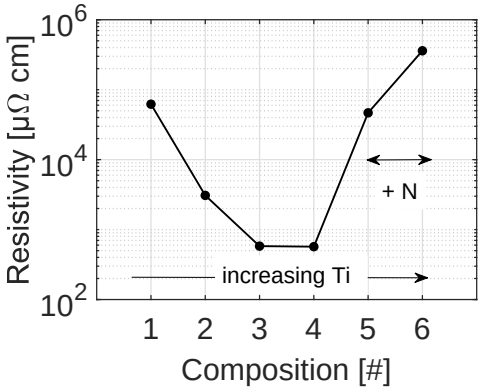

Fig. 5.38. Resistivity of the different TiTe composition developed in order to tune the electrical and the thermal properties of the material. Ti content is increasing from composition one to six. Composition 5 and 6 required some nitrogen (N) during the deposition process to guarantee the stability of the layer.

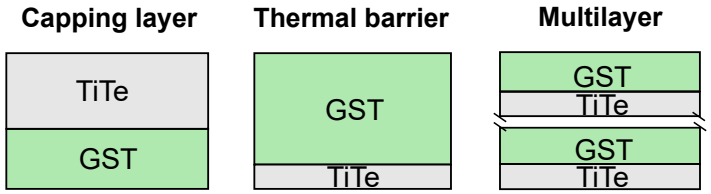

Fig. 5.39. Schematic of the main configurations of TiTe/GST stacks integrated in 60 nm Wall-based PCM for electrical characterization.

lization of the amorphous phase (RESET) even at a fluence as high as $5{\cdot}10^{10}$ ions/cm^2. While, the study on the radiation effects on different architectures (i.e., standard GST and SNC-PCM) confirms the benefit of a reduced PCM device size against heavy ion irradiation impacts.
These results enable to consider both the phase-change material engineering and the contact area scaling as two possible solutions to improve the radiation tolerance, even at extremely high fluences. In terms of material optimization, the chalcogenide materials with a high temperature stability are among the most suitable to achieve the target, as witnessed by the GGST performance.
Furthermore, it is fundamental to notice that our test are performed at a flux three order of magnitude higher than the lower limit imposed by the ESCC (European Space Component Coordination) heavy ion test guidelines, which evidence that the device analyzed in this work are subjected to a more harsh condition with respect to a real aerospace environment.

5.5 TiTe/GST based PCM

The doping of Sb_2Te_3 with Ti was presented as a strategy to reduce the RESET power up to 78% compared to GST based devices [109]. Furthermore, the development of $Ti_1Sb_2Te_5$ based PCM demonstrated a low power RESET operation due to the formation of $TiTe_2$ nano-lamellae in the crystalline phase of the active volume. The

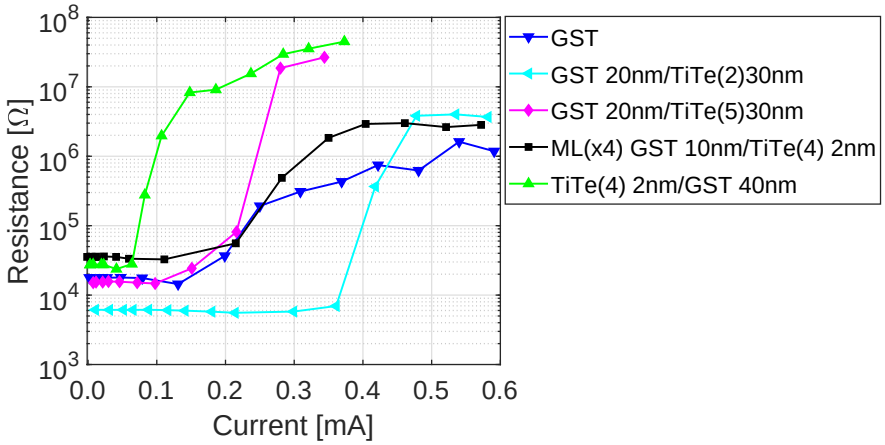

Fig. 5.40. Resistance as a function of current curve for different TiTe based PCM comparing their performance with respect to the GST based device. TiTe(4) used as a thermal barrier ensure a huge current reduction wrt to the other structure analyzed.

nano-lamellae are characterized by a low thermal and high electrical conductivity, opening the way to $TiTe_2/Sb_2Te_3$ multilayer based PCM as devices featuring ultra low-power consumption [154]. Nevertheless, the low crystallization temperature of Sb_2Te_3 represents an issue for the amorphous stability in temperature [155]. In addition, from the fabrication point of view, it is difficult to guarantee a good adhesion between Sb_2Te_3 and $TiTe_2$. Therefore, Sb_2Te_3 was replaced with GST to fabricate GST/TiTe based PCM. Exploiting this active layer stack can be rather interesting, especially if different TiTe stochiometry are investigated.
The resistivity as a function of the compositions (labeled with numbers from 1 to 6, with increasing Ti content) is reported in Fig. 5.38. The couple of compositions with the higher Ti concentration required some nitrogen (N) during the deposition process to guarantee the stability of the layer. The study of the electrical resistivity in temperature demonstrated that the most stable composition to be used as an active layer was the number 4 (i.e., TiTe(4)). Nevertheless, TiTe(5) and TiTe(2) were considered interesting materials to be used as both i) capping layer, to reduce the thermal losses through the top electrode and ii) thin thermal barrier at the interface between the PCL and the heater, to boost the thermal confinement at the interface between heater and PCL, where the information is stored (Fig. 5.39). On the contrary, TiTe(6) and TiTe(1) were not integrated in final devices, since TiTe(6) has a too high electrical conductivity, while TiTe(1) has an electrical conductivity comparable with TiTe(5) but it is characterized by a higher thermal conductivity (i.e., no thermal improvements), due to the lower content of Ti in it.
Dealing with the material presented, different configurations were suggested and studied: the use of TiTe i) as a capping layer; ii) as a thermal barrier; iii) in a multilayer stack with GST (see Fig. 5.39). The proposed solutions were integrated in 60 nm 1R Wall-based PCM. The resistance versus current curves obtained with a standard staircase up sequence on the integrated devices are reported in Fig. 5.40 where the RI of a GST cell is also reported as a reference. The most interesting performance in terms of programming current reduction is obtained with a 2 nm TiTe(4) used as a thermal

barrier and a 40 nm GST active layer. Indeed, this structure presents a 100 μA reduction in the melting current with respect to the GST structure.
The multilayer structure studied here is made of 10 nm GST and 2 nm TiTe repeated four times. Its RI characteristic is quite similar to the GST one, most probably because the programmed region involves just one layer of TiTe, which does not change significantly the composition of the active material itself.
The TiTe(2) and TiTe(5) were used as 30 nm capping layers on top of a 20 nm GST. The lower concentration of Ti in TiTe(2) made it less thermally efficient, because of its higher k_{th}, leading to the increase of its thermal resistance and, as a consequence, of its melting current, which is almost 200 μA higher with respect to the GST based devices. On the contrary, TiTe(5) shows an RI comparable with the GST one (i.e., similar melting current), leading to consider that the thermal conductivity of the two is comparable. Nevertheless, both TiTe(2) and TiTe(5) structures present a steeper transition from SET to RESET with respect to GST, which makes the TiTe(2) based structure to finally have a RESET programming current 50% lower than the GST based one. The steeper SET to RESET transition can be explained by the higher resistivity ($\geq$ 500 μΩ cm) of the TiTe compositions investigated with respect to the GST (10 μΩ cm). Indeed, the higher resistivity in TiTe devices induces the hot point to be closer to the PCL/heater, ensuring a more uniform temperature gradient and an abrupt amorphisation of the PCL, as presented in Section 4.4.
This preliminary study grown the interest to investigate two other TiTe based configurations: i) use of a multilayer structure by reversing the stack analysed in this section (i.e., TiTe deposited at the interface with the electrode, so that it can play the role of thermal barrier) and ii) integration of 2 nm TiTe(5) as a replacement of the 2 nm TiTe(4) thermal barrier, since its smaller k_{th} value can further decrease the PCM power consumption.

5.6 Chapter summary

In this chapter, the electro-thermal performance of three thermal engineered PCM are investigated to understand the key parameters controlling the device working principle and to be able to provide some guidelines for the next generation PCM device.

At first, the *SiC-PCM*, which integrate a SiC ($k_{th} \sim 0.4$ $Wm^{-1}K^{-1}$) encapsulation layer all around the PCM was studied. It demonstrated an higher temperature stability (i.e., more than one hour at 250 °C), better programming efficiency (steeper SET to RESET transition) and higher SET programming speed. These results were explained by the enhanced thermal confinement provided by a low k_{th} encapsulation layer, which causes a more uniform amorphous volume during the RESET operation. Nevertheless, a simulation study performed on state-of-the-art 80 nm Wall-based PCM, highlighted the existence of a minimum k_{th} value at which the height of the amorphous volume is constant. As a consequence, it is of no interest to further decrease the k_{th} below 0.4 $Wm^{-1}K^{-1}$ in the devices studied in this work, since it will not result in better power performance of the cell.
Furthermore, a theoretical model was proposed, revealing the correlation between the slopes of the RI characteristics and the thermal conductivities of the materials con-

stituting the PCM device. The model was validated by using the measured thermal conductivities of the dielectrics surrounding the PCL and the heater, and the PCL thermal conductivity available in literature. Finally, a demonstration of the strong impact of the dielectrics thermal conductivities was provided, suggesting a path towards ultra low power next generation PCM devices.

The second solution considered in this chapter is the *SNC-PCM*, which integrate a 10 nm GeN interfacial layer between the heater and the phase-change layer. It showed a RESET current reduction up to 50 μA, independently from the device size. This result was achieved thanks to the better thermal confinement of the cell, which allowed to RESET the device with a lower density of current. This leads the GeN/GST devices initialized at low currents to be more performing in terms of endurance cycles with respect to the one initialized at a higher one. Interestingly, the integration of this solution on a smaller technology node can generate a stronger self nano-confined phenomenon linked to the finer tuning of the current during the initialization step, which can lead to even lower power performances. Furthermore, the devices featured high stability and integrity even during BEOL fabrication (one hour at 400 °C) which made them suitable for industrial applications.
This solution is quite promising because of its versatility: it can both be used for high or low density applications, while keeping the working principle still reliable. Moreover, a further tuning of the N doping or thickness of the GeN layer can allow a even better control of the initialization current.

Furthermore, the *GST/TiTe PCM*, which integrated various combinations (i.e., different thicknesses and number of layers) of a TiTe layer with GST, was explored. The most promising among the stack investigated was represented by the structure integrating a 2 nm TiTe(4) layer with a 40 nm GST one. In this configuration, the TiTe(4) layer acted as a thermal barrier, resulting in a 100 μA reduction in the melting current value. This preliminary study, suggested two novel configurations to address the low power requirement in PCM. These are: i) the TiTe/GST multilayer structure, where the TiTe is integrated at the interface with the heater and ii) the TiTe(5) as a replacement of TiTe(4) thermal barrier in GST based PCM device.

Finally, the performance of GST, GGST and GeN/GST based PCM were compared in terms of their tollerance to radiation. The study demonstrated the higher radiation tolerance of GGST devices with respect to GST based one: the RESET state of GGST based PCM do not recrystallize even at a fluence as high as $5{\cdot}10^{10}$ ions/cm^2. Therefore, the phase-change material engineering represents one of the possible solutions to improve the radiation tolerance even at extremely high fluences: materials with a high temperature stability are among the most suitable to achieve this target. Finally, the investigation of the radiation hardness in SNC-PCM, confirmed the benefit of a reduced PCM device size against heavy ion irradiation.
These opened the possibility to consider materials with higher crystallization temperature and scaled PCL/heater interface to ensure a higher radiation hardness in PCM devices.

Conclusions and perspectives

In a world transitioning to the digital era, the necessity to store a large amount of information in a limited space is becoming increasingly crucial, thus requiring the miniaturization of the single device to increase the memory density.
Currently, the most diffused memory technology is the Flash, which relies on single charge storage, making it not suitable to fulfill the scaling requirement at low cost and, at the same time, to ensure high tolerance to radiation. These limitations can be overcome by a novel paradigm of memory technology, namely the Non-Volatile Resistive Memory (NVRM). In this two terminal device, an active material, sandwiched between two electrodes, is capable to change its resistive state allowing the data storage.
Among the most promising NVRMs, Phase-Change Cemories (PCMs) stood out for their versatility. As a matter of fact, they entered the market addressing SCM applications, and, with the development of the Ge-rich GST alloy, they achieved outstanding data retention, suitable for the embedded automotive applications. Furthermore, they are characterized by high tolerance to radiation. Nevertheless, the scientific community is committed to further improve the PCM performance. In particular, a main challenge is the reduction of the programming current. As a matter of fact, only 1% of the injected power is used to program the cell, due to the high percentage of heat dissipated in the surrounding of the active volume [4, 70]. Several approaches have been proposed so far, leveraging the device fabrication and the cell architecture [156], the material [10] and the interfaces engineering [93]. Despite the promising results, these solutions still raise doubts about their cost, the scalability in industrial devices, the control of the material evolution during Back-End-Of-Lines (BEOL) fabrication steps as well as the material degradation along cycling.

This work aims to contribute to the development of the next generation low-power Phase-Change Memory. Here the thermal optimization of the PCM cell is carried out along three main axis: the thermal conductivity characterization of both dielectric and calchogenide materials, the 3D finite-elements simulation of the electro-thermal phenomena controlling the PCM functionality and, finally, its electrical characterization.
As demonstrated in previous works, thermal conductivity plays a crucial role on the PCM electro-thermal performance. Therefore, the reliable k_{th} measurements can provide more accurate electro-thermal simulations which can support the interpretation of the electrical characterization results. With this aim, an existing test bench in CEA-LETI was optimized and validated, comparing the obtained temperature-dependent thermal conductivity results with those measured on the same devices at the Institut de Mecanique et d' Ingenierie (12M) de Bordeaux and at the Laboratoire National de Metrologie et d'essais (LNE) in Paris. The validation of the set-up in LETI represents a fundamental stepping stone to boost future research works in the laboratory. In par-

ticular, as a result of the optimization process, different technical improvements were proposed: i) the integration of a Pt electrode; ii) the introduction of a GeN dielectric capping layer deposited between the material specimen and the electrode; iii) the definition of the optimal measurements protocol, ensuring the removal of the interface resistances contribution to the measured k_{th}.

In Ch. 4, a 3D numerical study based on finite-element method has been presented. In particular, the electro-thermal phenomena regulating a 80 nm Wall-based PCM were investigated, with the aim of providing guidelines for the design of next-generation PCM targeting low-power consumption. The heater resistance and the thermal conductivity of the adjacent dielectric material in direct contact with it were identified as the components influencing the most the electro-thermal response of the cell. On the contrary, it was proven that the phase-change layer thermal conductivity has a limited contribution to the PCM performance. Furthermore, the gradual increase of the resistance value, characterizing the experimental RI curve above the melting point, was modeled by introducing the electric field dependence in the phase-change material electrical conductivity model.

In Ch. 5, the analysis of the electrical performance of different thermal engineered PCM solutions has been investigated by supporting the electric test with the thermal conductivity measurements, the physico-chemical analysis and the electro-thermal simulations performed on the same structures. Interestingly, the use of SiC as encapsulation layer has been proposed as a potential solution for a better thermal efficiency of the cell as well as improved retention performances (i.e., higher than one hour at 250 °C) and higher SET programming speed. Moreover, it was proven that a GeN interfacial layer can allow an important downscaling of the PCM technology thanks to the programming current control at the initialization step. This solution led to the lower programming current population at 50 μA, endurance up to 10^8 cycles and perfect integrity after BEOL thermal budget, definitely combining BEOL process compatibility, performance reliability, low power programming and scalability at array level. Finally, the preliminary study performed on the use of TiTe thin layer as a thermal barrier demonstrated that it can be a promising solution for low-power PCM devices.
Furthermore, previous studies on the PCM radiation hardness suggested a possible relation between the PCM architecture/size and its tolerance to radiation. In the framework of a collaboration with the GSI Darmstadt (Germany), suitability for aerospace applications of scaled PCM devices fabricated in LETI with a 130 nm CMOS technology was investigated. With this aim, at first, the heavy ion radiation effects on the structural changes of the materials integrated as active layer was tested. Then, the evolution of the SET and RESET states under different irradiation fluences in 4kb arrays was correlated with the morphological analysis previously performed on the active layer material. This demonstrated that the GeN/GST and the GGST-based PCM were more tolerant to radiation than the GST one: in the former, the better performance was associated to the smaller contact area generated during the creation of the filament, while for GGST the results were explained by its higher thermal stability with respect to GST. In conclusion, the analysis identified the materials with high crystallization temperature and the devices with a scaled PCL/heater interface as those presenting higher tolerance to radiation.

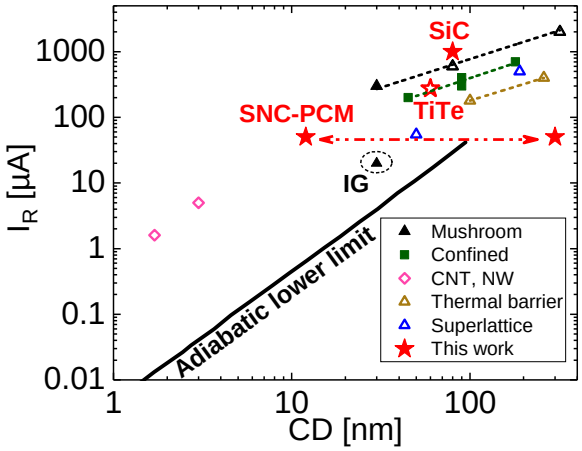

Fig. 5.41. Reset current as a function of the device critical dimension for different PCM architectures. The filled marks refer to results validated at array level, while the empty ones indicate tests performed on single devices.

Fig. 5.41 compares the solutions investigated in this work with the technologies proposed in the literature, using as a benchmark parameter the RESET current (I_R) as a function of the device critical dimension (CD). The filled markers indicate the results validated at array level, while the empty ones refer to the analysis performed on single devices. In addition, the trend-line for the main classes of strategies presented in literature (i.e., mushroom, confined and thermal barrier) are represented by dashed-lines, while the black line indicates to the adiabatic lower limit, evaluated for a mushroom type cell [69]. The plot highlights that the current optimization can result either from the contact area (i.e., CD) reduction or the PCM architecture (i.e., device thermal resistance). In particular, the trend-line associated to the PCM integrating thermal barriers [85, 91] features the lowest programming current and it is the closest to the adiabatic lower limit condition. This result is consequent to the optimization of the temperature profile at the interface between the bottom electrode and the phase-change material, where the thermal barrier is integrated. The integration of a thin TiTe layer as a thermal barrier in a confined PCM lies, instead, on the same trend-line as standard confined devices [6, 80, 157, 158]. Nevertheless, its performance can be improved by reducing the percentage of Ti in the TiTe layer, as discussed in Ch. 5. This would reduce the layer thermal conductivity and improve the temperature at the bottom electrode interface, reducing the device programming current.
Importantly, the most promising solution is represented by the SNC-PCM. It enhances the device performance independently from the technology node (i.e., the same current is achieved with different CDs, as evidenced by the horizontal doubled-headed arrow), enabling the CD to scale down to nanometer scale, thanks to an innovative and lithography-free GeN/GST based device. This structure overcomes the mushroom cell adiabatic lower limit at a CD of 100 nm, due to the size-independent nature of its working principle. This result is even more valuable if combined with the integration in a smaller technology node, which can ensure a finer tuning of the current delivered to the cell below 50 µA, lowering both the programming current and the device CD.

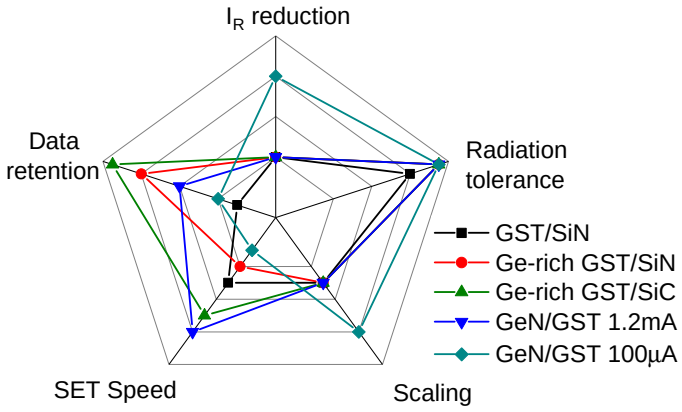

Fig. 5.42. Comparison of the different solution investigated in this work with respect to the GST based PCM.

The functionality of this structure at extremely low currents was confirmed by the study performed on carbon nanotube (CNT) [159] and nanowire (NW) [160] based PCM, which can achieve a reliable programming with a CD of ∼2 nm. Therefore, the SNC-PCM can potentially perform better than the intergranular (IG) based PCM. A further approach to be investigated in a SNC-PCM is the integration of the tuned TiTe thermal barrier between the heater and the GeN layer. This would improve the SNC-PCM thermal resistance, hence reducing the programming current.

An overview of the different solutions presented in this thesis is reported in Fig. 5.42, were their comparison with the standard GST-based PCM is performed. Ge-rich SiC and Ge-rich SiN-based PCM present the best performances for embedded applications, with data retention of one hour at respectively 230 °C and 250 °C, and high radiation tolerance. On the contrary, the other solutions are more suitable for stand-alone applications. In particular, the GeN/GST initialized at 100 µA fits better the requirements for high density and extremely low current applications, while the GeN/GST initialized at 1.2 mA is more suitable for faster SET speed requirements. As a result, the use of a SiC-based encapsulation layer can improve the SET speed of the GeN/GST initialized at 100 µA, making it even more versatile. Moreover, replacing the standard GST with a Ge-rich alloy can improve the data retention of the SNC-PCM, enabling its use for embedded applications.

A further aspect to consider when targeting high cell density and low-power requirements is the thermal boundary resistance (TBR). As a matter of fact, this increases when scaling down the PCM cell, thus affecting its performances [33]. Furthermore, the TBR value can face a one order of magnitude discrepancy, depending on the layer deposition temperature and its roughness [161]. Therefore, an accurate measure of the TBR at the heater/PCL interface (i.e., the interface closer to the programming region) ensures reliable numerical predictions on the behavior of scaled PCM devices. In this framework, the validation of the 3ω bench test is valuable since it allows the direct measure of the TBR value on materials integrated in the PCM device. For instance, in the case of a TiN heater integrated with a GST chalcogenide layer, it is

possible to develop a TiN/GST/TiN multilayer stack [61] and use the optimal measurement workflow (presented in Ch.3) to evaluate both the GST thermal conductivity and the thermal boundary resistance at the TiN/GST interface. In addition, with the device scaling, the geometrical non idealities will have a stronger impact on the final performance of the cell, hence they should be properly accounted to enable reliable simulations. With this aim, a tool that is getting a foothold in this field is the software Synopsys, which allows to build the geometry by taking into account the fabrication process steps by step.
Finally, the experimental and numerical tools developed in this work, along with the integration and characterization of novel technological solutions to reduce the PCM power consumption, represent a step forward towards a mature, reliable and versatile PCM memory, combining optimal electro-thermal performances with the strict market requirements.

List of publications associated to this work

Conference proceedings

[1] A. L. Serra et al., "Heavy-ions radiation effects on 4kb Phase-Change Memory", *Radiation and its Effects on Components and Systems (RADECS)*, 2020.

[2] A. L. Serra et al., "Heavy-ions radiation effects on 4kb Phase-Change Memory", *Nuclear And Space Radiation Effects Conference (NSREC)*, 2020.

[3] A. L. Serra et al., "Outstanding Improvement in 4Kb Phase-Change Memory of Programming and Retention Performances by Enhanced Thermal Confinement", *2019 IEEE 11th International Memory Workshop (IMW)*, 2019.

[4] A. L. Serra et al., "Optimization of 3ω Method for Phase-Change Materials Thermal Conductivity Measurement at High Temperature", *32nd IEEE International Conference on Microelectronic Test Structures*, 2019.

[5] G. Lefèvre et al., "TEM and EDX Analyses of Thermally Improved Phase-Change Memory by Optimized Encapsulation Layer", *European Materials Research Society (E-MRS)*, 2020.

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[8] A. L. Serra et al., "Innovative Low Power Self-Nano-Confined Phase-Change Memory", *IEEE Transaction on Electron Devices* (accepted).

[9] A. L. Serra et al., "Phase-Change Memory Electro-Thermal Analysis and Engineering Thanks to Enhanced Thermal Confinement", *Solid-State Electronics* (submitted).

Patent applications

[10] A. L. Serra, C. Sabbione, G. Navarro, G. Bourgeois, "Procédé de programmation d'une mémoire à changement de phase" (submitted).

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Title: New generation of Non-Volatile Phase-Change Memory targeting ultra-low power consumption

Abstract:

In a world transitioning to the digital era, the necessity to store a large amount of information in a limited space is becoming crucial. Therefore, the device down-scaling and the consequent increase in the memory density are highly relevant. The most diffused memory technology, i.e., the Flash, is not suitable to fulfill the scaling requirements at low-cost. As an alternative to Flash, recently, Non-Volatile Resistive Memories (NVRMs) were developed. One of the most promising NVRMs in terms of scalability is the Phase-Change Memory (PCM); however, it lacks thermal efficiency since only 1% of the energy generated during the programming of the cell is used to store the information.

In this work, the thermal optimization of the cell is carried out by focusing on three main aspects: i) the measurement of the thermal conductivity of the materials integrated in the device; ii) the 3D electro-thermal simulations identifying the main sources of dissipation in the cell; iii) the electrical characterization.

As a result, different approaches for thermally-engineered state-of-art PCM were proposed, targeting low-power automotive or aerospace applications.

Key Words: Phase-Change Memory, thermal conductivity, electro-thermal simulations.

TITRE : Nouvelle génération de mémoire à changement de phase non volatile pour des applications à très basse consommation

Résumé :

Dans un monde de plus en plus bâti sur la technologie, le besoin de stocker une grande quantité d'informations dans un espace limité devient considérable. La miniaturisation des dispositifs de mémoire unitaire devient nécessaire pour l'augmentation de la densité de stockage. La technologie mémoire la plus courante, c.-à-d., la technologie Flash, devient de plus en plus problématique à cause des limitations intrinsèques de la mise à l'échelle. Parmi les solutions les plus intéressantes pour remplacer la mémoire Flash, on trouve les mémoires résistives non volatiles (ou NVRMs). Parmi les NVRMs, la plus prometteuse en termes de mise à l'échelle est la mémoire à changement de phase (PCM). Néanmoins, la PCM manque d'efficacité thermique puisque seulement 1% de l'énergie générée pendant la programmation est effectivement utilisée pour programmer la cellule mémoire. L'amélioration des performances thermiques des cellules PCM est donc fondamentale pour réduire considérablement l'énergie engagée pendant la programmation.

L'objectif principal de ce travail est de contribuer au développement de la prochaine génération de PCM. Les études se sont concentrées sur trois axes principaux : i) la caractérisation de la conductivité thermique de différents matériaux intégrés dans un dispositif PCM ; ii) les simulations électrothermiques en 3D qui donnent la possibilité de déterminer les sources principales des pertes de chaleur dans la cellule mémoire ; iii) la caractérisation électrique. Plusieurs dispositifs à l'état de l'art ont été proposés, chacun ayant un meilleur confinement thermique pour des applications automobile ou aérospatiales.

Mots Clés : mémoires à changement de phase, conductivité thermique, simulations électrothermiques.