A Methodology for designing SiC and GaN device based converters for automotive applications

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Abstract

Wide band-gap (WBG) devices enable power converter designs at higher frequency, power density, and efficiency, as compared to silicon-based converters. The coexistence for SiC (Silicon Carbide) and GaN (Gallium Nitride) devices in the ranges 600-900 V motivates a specific study of these components and the development of methods to perform better selection relying on the application, particularly for automotive applications. The proposed methodology starts with static and dynamic tests performed on SiC and GaN devices to validate their models. GaN power devices allow the building of the most integrated converters. Here, an instrumented PCB (Printed Circuit Board) is developed to measure and estimate switching losses including the measurement points needed for this purpose. The parasitic elements of the PCB layout extracted by ANSYS Q3D and the measurement instrument models are also included in the simulation model. Thus, by means of an experimentally validated model, it will be possible to evaluate the total losses in an optimized circuit without probes. Meanwhile, for SiC devices, an evaluation board is used, and an estimating method for inductance parasitic extraction is performed. The switching loss estimation is an important step for power converter design. Moreover, the consequences of faster switching on the gate driver design and board layout generate new challenges for WBG-based converters. An accurate switching loss estimation is a helpful step because it allows for the adjustment of different circuit layouts based on the simulation results. However, the instrumented PCB does not predict the switching losses in an optimized converter, but only on the instrumented PCB. The simulation enables the prediction of switching losses in more realistic converters. Finally, a simulation for each target device (SiC and GaN) is developed considering the main parasitic elements and the measurement instrument models. Thus, the switching losses are computed and compared to experimental results. Since the whole system is validated, to compare the SiC and GaN devices for automotive applications, an optimized DC-DC converter simulation is used for comparing each device under different operation points of the converter.

Résumé

Les componsants à large bande interdite ou WBG permettent de concevoir des convertisseurs de puissance à des fréquences, des densité de puissance et des efficacités plus élevées, par rapport aux convertisseurs à base de silicium. La coexistence de dispositifs SiC et GaN dans la gamme 600-900 V motive une étude spécifique de ces composants et le développement de méthodes pour effectuer une meilleure sélection en fonction de l'application, notamment pour les applications automobiles. La méthodologie proposée commence par des tests statiques et dynamiques effectués sur des dispositifs SiC et GaN afin de valider leurs modèles. Les dispositifs GaN permettent de construire les convertisseurs les plus intégrés. Un PCB instrumenté a été développé pour mesurer et estimer les pertes en commutation, incluant les points de mesure nécessaires à cet effet. Les éléments parasites du schéma PCB extraits par ANSYS Q3D et les modèles de sondes de mesure ont été également inclus dans le modèle de simulation. Ainsi, au moyen d'un modèle validé expérimentalement, il a été possible d'évaluer les pertes totales dans un circuit optimisé, sans sondes. Pour les dispositifs SiC, une carte d'évaluation a été utilisée et une méthode d'estimation pour l'extraction des éléments parasites a été effectuée. L'estimation des pertes en commutation est une étape importante pour la conception du convertisseur de puissance. Les conséquences d'une commutation plus rapide sur la conception du driver de grille et la disposition de la carte génèrent de nouveaux défis pour les convertisseurs basés sur les dispositifs WBG. Une estimation précise des pertes en commutation est une étape utile car elle permet d'ajuster différentes configurations de circuits en fonction des résultats de la simulation. Cependant, le PCB instrumenté ne prédit pas les pertes en commutation dans un convertisseur optimisé, mais uniquement sur le PCB instrumenté. La simulation permet de prédire les pertes en commutation dans des convertisseurs plus réalistes. Une simulation pour chaque dispositif cible (SiC et GaN) a été développée en considérant les principaux éléments parasites et les modèles d'instruments de mesure. Ainsi, les pertes en commutation sont calculées et comparées aux résultats expérimentaux. Étant donné que l'ensemble du système a été validé, afin de comparer les dispositifs SiC et GaN pour les applications automobiles, une simulation d'un convertisseur DC-DC optimisé a été utilisée pour comparer chaque dispositif sous différents points de fonctionnement du convertisseur.

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CHAPTER 1

General Introduction

1.1 Wide Bandgap Power Devices

The current trends in power electronics have been focusing on higher efficiency and power density of power converters. For several years, Si-based power MOSFETs (Metal Oxide Semiconductor Field-effect Transistor) have dominated the field of power converter design in the low-to-medium voltage categories. However, this technology is reaching its theoretical performance limits, which means that new technologies should be implemented to achieve better performing power electronics devices. In this context, the wide bandgap devices, like SiC and GaN, are strong candidates to fulfill these new requirements [1–3].

Moreover, these devices allow for the realizing of high-frequency and high-efficiency power converters. Compared to silicon power devices, the higher breakdown field of a WBG semiconductor allows for the building of thinner layers in the device, resulting in a lower specific ON-resistance [4]. A smaller die size implies lower input and output capacitance, thus a faster switching transient is achieved. SiC MOSFETs provide the highest voltage, current, and temperature capabilities, whereas the GaN HEMTs (High Electron Mobility Transistor) offer the highest efficiency and switching speed for power converter applications.

However, these improvements bring new challenges when it comes to the loss

measurements of the converters based on WBG devices [5–8]. The comprehensive analysis of the impact of the wiring parasitic elements and instruments modeling in terms of good measurement should be performed to achieve an accurate switching loss estimation, which is the focus on this thesis.

1.2 Wide Bandgap Devices for Automotive Applications

In the context of the electric vehicles, one of the most important objectives is to develop more powerful power circuits with maximum efficiency and power density. The reduction in the size of the components suggests two variables: the switching frequency and the development of new semiconductor technologies. Figure 1.1 shows an overall schematic of a powertrain in an electric vehicle.

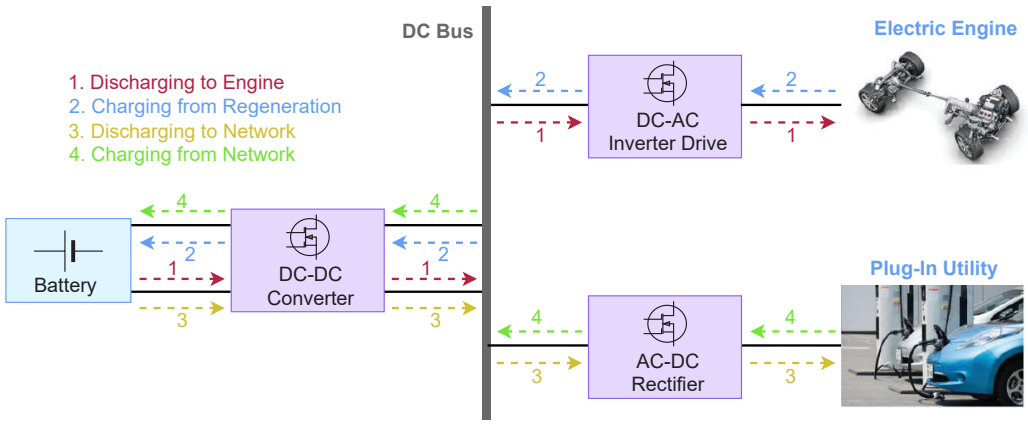


Figure 1.1: An universal DC-DC converter for a plug-in electric vehicle adapted from [9].

The first aim is to increase the powertrain supply voltage of the electric vehicle to beyond 400 V, the usual voltage for electric vehicle batteries today. This would reduce the current in the IGBT (Insulated Gate Bipolar Transistor) chips of the inverter, and consequently the amount of Si used, thus decreasing the total cost. In addition, the integration of the inverter into the motor, allowing for a common cooling system, will be explored in the future. The second equally important objective is to improve the inverter energy density (regarding volume and weight), as well as the switching frequency increasing of

DC-DC power converters. The operating modes of a DC-DC power converter on board an electric vehicle are enumerated as follows [9].

1. Acceleration/Generation: The battery provides power for the electric motor. The converter input is the battery, and the output is the DC bus. At this level, the converter works in boost mode.

2. Braking/Regeneration: The vehicle has negative torque, and thus, there is the regeneration of power to the battery. The converter input, in this case, is the DC bus, and the output is the battery.

3. Vehicle-to-Grid (V2G): The battery supplies power to the grid. The electric vehicle is connected to the network.

4. Battery charging: The vehicle is connected to the network which supplies power.

The WBG technology integrated into DC-DC converters on electric vehicles brings several positive characteristics such as a lower total loss (conduction and switching losses), higher temperature operation, allowing for the use of simpler cooling systems, high integration level due to the WBG devices being smaller than Si-based power switches, and a high level of parasitic elements optimization.

1.3 Research Motivation and Objectives

The main motivation of this thesis is following the new power device technologies towards better integration of WBG semiconductors in automotive applications. The coexistence for SiC/GaN devices in the range 600-900 V motivates a specific study of these components and the development of methods to per- form better selection relying on the application. In this thesis, a protocol for comparison between SiC and GaN devices based on switching loss estimation is discussed. Further, models validation is performed for the power devices, parasitic elements, and voltage/current probes. Here, the development of a method of switching loss estimation considering the main system elements is important for power converter design.

The initial research topic in this thesis is to perform the characterization of the wide bandgap devices to obtain their static, dynamic, and switching characteristics. The characterization results are compared to both the datasheet and simulations for model validation. The impact of the gate and loop inductance of the PCB used for switching characterization is analyzed, and some extracted values obtained from the simulation tool are validated by measurement tests. Subsequently, measurement instrument models (voltage and current probes) are developed to evaluate their impacts on switching transient. Finally, the switching loss estimation is performed considering only dissipative elements from SPICE models of each target device, and a comparison aiming at an automotive application is discussed.

1.4 Thesis Organization

Based upon the research objectives described above, this thesis is organized as follows:

In **Chapter 2**, the state of the art regarding this thesis is presented. Here, a comprehensive overview of SiC and GaN technologies and gate driving methods are explained. The general static and switching characterization processes that are applicable to WBG devices for model validation are discussed. Finally, the switching loss estimation study is presented, aiming at automotive applications.

In **Chapter 3**, power devices characterization is performed in static and dynamic states to validate SPICE models. The goal of this section is to compare datasheet, simulation, and experimental results for different WBG devices at ambient temperature and under high temperature operation.

In **Chapter 4**, an instrumented PCB is presented to analyze the switching transient of GaN HEMT devices. The analysis of the main parasitic elements of the PCB is then performed to develop an accurate simulation regarding the switching behavior. Moreover, measurement instrument (voltage and current probes) models are developed to verify the impact on the switching transient.

In **Chapter 5**, switching validation for the GaN HEMT device is presented.

Furthermore, switching loss estimation is performed using the traditional method of calculation (V-I product) and considering only dissipative elements. A comparison between SiC and GaN devices is performed, aiming at a specified automotive application.

CHAPTER 2

State of the Art

2.1 Silicon Carbide Power Device

Silicon (Si) technology exhibits some limitations for applications at high voltage (HV) and high temperature (HT). Si-based power electronics applications are limited to 150 °C and can endure only 10 kV blocking voltages. In addition, the switching speed limitation of Si components (few kHz) becomes an issue for higher frequency operation. Meanwhile, the high switching speed is suitable for reduced capacitor and inductor sizes, lower system cost, and overall efficient system performance [2]. Further, the high power density capability of WBG power devices with the potentially fast switching and low losses make them suitable for automotive applications where performance and low weight are key to the development of more compact power converters.

2.1.1 SiC Technology Overview

Power switch performance is based on the physical properties of semiconductor materials. The breakdown voltage, maximal operating temperature, ON-resistance, and switching speed are some of the main characteristics that define the performance of a power device [10]. In Table 2.1, the electronic properties of the main semiconductor materials for power application at an ambient temperature (300 K) are shown.

Silicon carbide belongs to wide bandgap semiconductor. This means that for a

semiconductor material, the bandgap energy between the valence conduction bands is wider than that of silicon devices. Table 2.1 shows the advantages of the SiC devices in regards to power devices made out of silicon material. The critical field of SiC is about 10 times more important than Si material, which means that for the same voltage, a power switch based on SiC material has a drift region 10 times thinner than a device based on Si material [2]. The new requirements for power switches match the emergence of WBG semiconductors (SiC and GaN), which promise to meet these requirements with better physical properties compared to silicon. In this thesis, both the SiC and GaN devices in the industrialization phase were chosen.

Table 2.1: Comparison of properties of semiconductor materials. [11, 12]

	Silicon	4H-SiC	GaN	Diamond
Bandgap E_G (eV)	1.12	3.26	3.39	5.7
Intrinsic Concentration n_i (cm^{-3})	1.4×10^{10}	8.2×10^{-9}	1.9×10^{-10}	1×10^{-22}
Electron Mobility μ_n ($cm^2/(V \cdot s)$)	1400	950	1500	4500
Critical Electric Field E_C (MV/cm)	0.23	2.2	3.3	10
Thermal Conductivity ($W/(cm \cdot K)$)	1.5	3.8	1.3	20
Electron Saturation Speed $v_{sat,n}$ ($10^7 cm \cdot s^{-1}$)	1	2	2.3	3
Relative Electric Permittivity ϵ	11.8	9.7	9	5.7

The breakdown voltage V_{BR} is expressed in Equation (2.1), where W_{drift} is the drift zone thickness, and E_C is the critical breakdown field [13].

$$V_{BR} = \frac{W_{drift} E_C}{2} \tag{2.1}$$

The wide bandgap materials have a higher critical breakdown field when compared to the Si devices, therefore for the same drift thickness, these devices are capable of supporting higher voltages. Due to these characteristics (wide bandgap), the specific ON-resistance (R_{ON}) is lower than that of the silicon components. The Equation (2.2) shows the relation between the breakdown voltage and ON-resistance [10].

$$R_{ON} = \frac{4 V_{BR}^2}{\epsilon_0 \epsilon_r \mu_n E_C^3} \tag{2.2}$$

Where ϵ_0 is vacuum permittivity , and ϵ_r is the material relative permittivity.

Figure 2.1 shows that for devices based on silicon carbide material the ON-resistance could be up to 1000 times lower than that of devices based on silicon material. This approach is due to SiC devices having drift region (W_{drift}) 10 times lower and a doping concentration (N_D) about 100 times higher than Si devices.

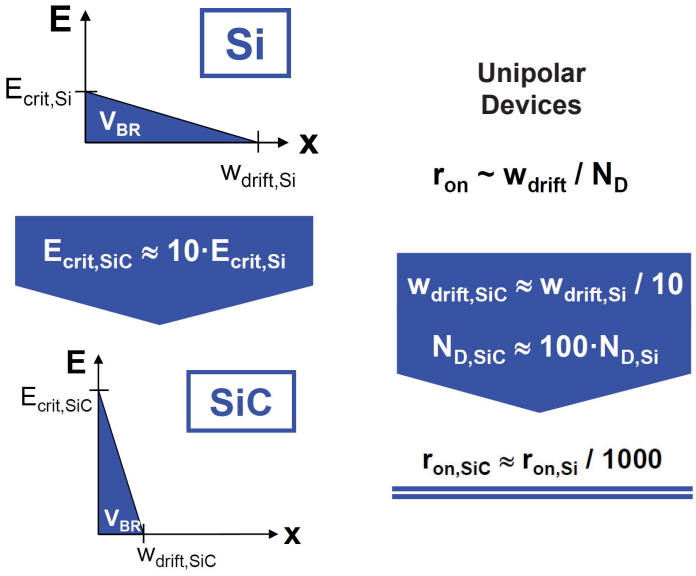


Figure 2.1: Relations between breakdown voltage and ON-resistance for Si and SiC devices [2].

The wide bandgap of SiC, a higher distance between the valence and conductor bands of the material, allows for a higher withstanding of temperature variations, ensuring its properties as a semiconductor. The leakage current is considerably lower, due to the low carrier intrinsic concentration.

The device processing technology of SiC devices is already at a mature level. Its common application is related to the field of high-power electronics where reliability has a major role. Nowadays, these devices have been used in up to 1.7 kV applications due to their higher-voltage capability and switching performances [14].

A typical SiC MOSFET structure is presented in Figure 2.2. Normally, the SiC devices are doped by an N-channel because it benefits from the higher electron mobility. The gate is insulated by an SiO2, layer and is led to a

positive potential with respect to the source. This positive potential generates an electric field in SiO2 which attracts the electrons towards the interface oxide/channel by means of electrons accumulation. The holes in the P+ zone are also driven by an electrostatic effect. The electric current can then pass through this channel, towards the drain. During the blocking state, the inverse voltage is mainly supported by the N layer. A high-voltage transistor needs a larger N layer and is weakly doped, namely more resistive. Thus, there is an important trade-off between ON-resistance and the maximum blocking voltage supported by the power device [15].

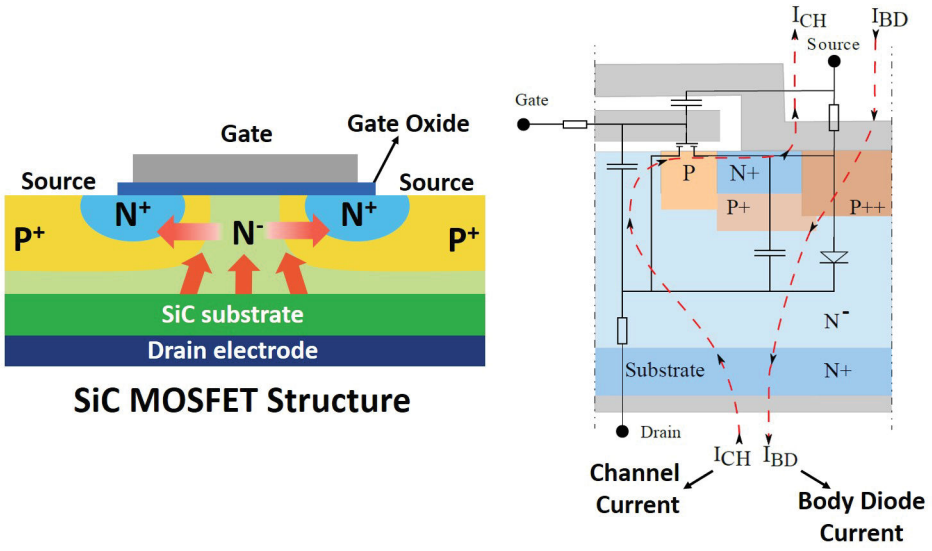


Figure 2.2: Typical SiC MOSFET structure and its parasitic elements adapted from [16, 17].

Here, tt is also important to highlight the presence of a body diode between the layers, N^+ and P^+, as seen in Figure 2.2, which prevents the turning-ON of the bipolar transistor during the OFF state. This diode is quite useful in power converters, because of its rapid response and capability of conducting a nominal current of the device [16]. In Table 2.2, the SiC power devices used in this thesis are presented.

Table 2.2: Some characteristics of the SiC power devices used in this thesis.

Parameter	Symbol	Manufacturer		Unit
		CREE	Rohm	
Part Number	P/N	C3M0060065K	SCT3030AL	-
Drain Source Voltage, max.	V_{DS}	650	650	V
Continous Current, max	I_{DS}	37	70	A
Gate Voltage, max	V_{GS}	19	22	V
Thermal Resistance, junction-case	R_{thJC}	0.99	0.44	°C/W
Gate Threshold Voltage, typ.	$V_{GS(th)}$	2.3	4.15	V
On-state Resistance, typ.	$R_{DS(on)}$	60	30	mΩ
Gate resistance	$R_{G,int}$	3	7	Ω
Input capacitance	C_{iss}	1020	1526	pF
Output capacitance	C_{oss}	80	89	pF
Reverse Transfer capacitance	C_{rss}	9	42	pF
Total Gate Charge	Q_G	46	104	nC

2.1.2 Gate Driver for SiC Power Devices

SiC MOSFETs are voltage driven via a control board, commonly called a driver board. Indeed, the main role of this board is to control the passage from the blocked state to the ON state. Other features are also added, such as protection of power switches and galvanic isolation between the central processing unit and the power stage. This control board is mainly composed of a driver and an isolated power supply [18, 19].

2.1.2.1 Gate Driver Fundamentals

The gate driver is considered as an interface that controls the charge and discharge of the gate input capacitance (C_{ISS}) to allow for the switching of the transistor. SiC MOSFETs operate with a gate source voltage of about $+20\,\mathrm{V}$ for the ON state, and $-5\,\mathrm{V}$ for the OFF state. Electrical isolation and level shifting are other functions of the gate driver [18]. In Figure 2.3, a basic structure for a gate driver controlling a switch can be seen.

The driver circuit acts directly on the dynamics of the switching (dV_{DS}/dt and dI_{DS}/dt). This is directly related to electromagnetic disturbances and switching losses. Further, fast voltage switching also becomes a noise source and generates the common mode current on the MOSFET substrate, power supply, and electrical network. Likewise, fast current switching generates overvoltage on parasitic inductances (L_D and L_S), besides electromagnetic disturbances between the power and control loops [20].

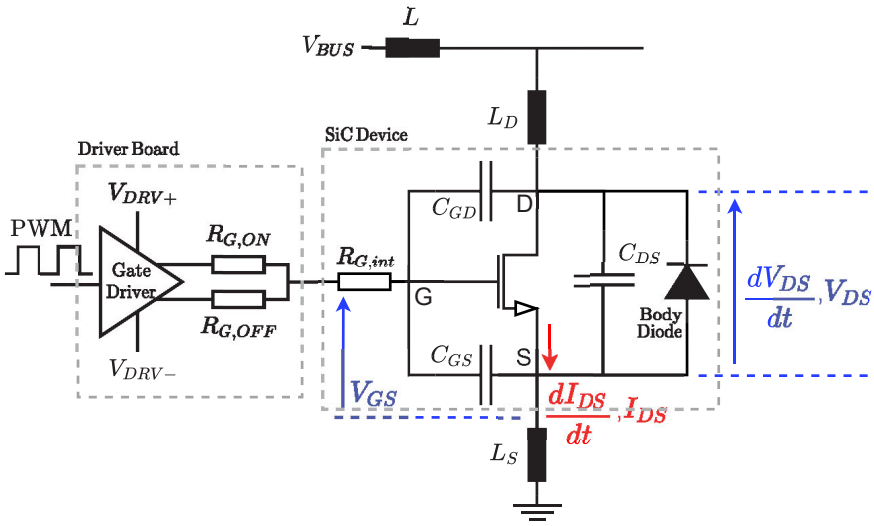


Figure 2.3: SiC MOSFET with parasitic elements and the associated gate driver adapted from [14].

The lower transconductance compared to power devices based on Si material involve a larger gate source voltage (V_{GS}) to optimize performance in the linear region. Therefore, it is possible to yield the lowest ON-resistance and thus decreases conduction losses. A V_{GS} between 15 V and 20 V is required to achieve the lowest V_{DS} saturation [20]. The low threshold voltage (V_{TH}) and fast switching speed of SiC devices need a negative V_{GS} during the OFF state, normally between -5 V and -2 V. Thus, the false turn-ON phenomenon can be prevented [14].

2.1.2.2 Characteristics and Design

The isolated power supply is the bulkiest part of a driver board, and its function is to provide sufficient power to drive a MOSFET while ensuring the requested galvanic isolation with the central processing unit. The more important parameters to be considered in terms of power supply design are maximum isolation voltage, input/output voltage, nominal power and isolation capacitance [19]. In Figure 2.4, examples of power supplies are presented, and in Table 2.3, the summary of their characteristics can be seen. Based on a comparative study, the Murata NXJ1S1212MC power supply exhibits the lowest insulation capacity, and is also the most compact in volume.

Most manufacturers of integrated circuits tend to implement electrical isola-

Figure 2.4: Some examples of isolated power supplies for driver transistor applications.

Table 2.3: Benchmarks of some isolated power supplies for driver transistor application.

Manufacturer	XP Power	Murata	Murata	RECOM Power
Reference	IHA0112D05	NTV1205MC	NXJ1S1212MC	RH-1205D
Isolation Voltage (kV)	6	3	4.2	3
Input/Output Voltage (V)	12/05	12/05	12/12	12/05
Nominal Power (W)	1	1	1	1
Isolation Capacitor (pF)	10	50	2.5	20

tion directly in the driver chip. Thus, the function of driving the MOSFET is ensured, as well as the electrical isolation between the DSP (Digital Signal Processor), connected to the low-voltage ground plane, and the power switches, which are referenced to the high-voltage ground plane [20]. In Figure 2.5, the drivers of two different manufactures are presented. In Table 2.4, the comparison of some characteristics of the drivers tested in this thesis are presented. Further, other references for different gate drivers are presented in [21].

Table 2.4: Comparison of the characteristics of two isolated drivers from Infineon and Silicon Labs for SiC devices.

Manufacturer	Infineon	Silicon Labs
Reference	1EDI60N12AF	SI8261BCD-C-IS
Isolation Voltage (kV)	1.2	5
CMTI (V/ns)	100	50
Source/Sink Current (A)	10/9.4	1.8/4
UVLO (ON/OFF)	9.1/8.5	8.4/7.9
Rise time (ns)	10	5.5
Fall time (ns)	9	8.5
Propagation Delay (ns)	120	60
Low/High Output Resistance (Ω)	1.5/3	0.8/2.6
Package	PG-DSO-8-51	SDIP-6

To implement galvanic electrical isolation, the driver from Silicon Labs use

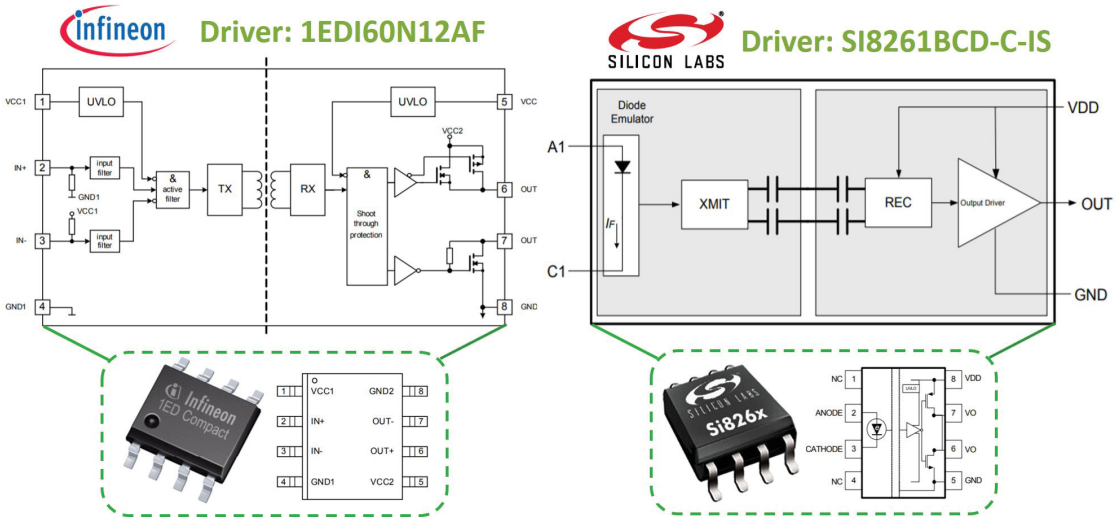


Figure 2.5: Functional block diagram of drivers from Infineon and Silicon Labs for SiC devices.

opto-coupling technology, while the driver from Infineon uses an isolated coreless transformer, allowing for the achievementt of a higher CMTI (Common-Mode Transient Immunity) [20]. Moreover, the complexity level of a driver is proportional to the number of functions accumulated in the device, implying more energy consumption. Thus, a trade-off during project conception should be performed to ensure a better solution.

2.2 Gallium Nitride Power Device

Gallium nitride is a wideband gap semiconductor that presents a larger energy bandgap than silicon carbide. Initially used for radio frequency (RF) applications, the GaN HEMT started to be used in 2004 while still assembled on SiC substrates. Nowadays, the substrates are replaced by silicon material, thus decreasing the production cost for GaN devices. Moreover, while the use of GaN components is similar to traditional MOSFETs, some care should be taken regarding the assembling, due to the reduced size of GaN-based devices. In this context, currently, PCB manufacturing technology has been developing and is already capable of designing high performance assemblies.

2.2.1 GaN Technology Overview

In Figure 2.6, the basic structure of GaN HEMT is presented. The main part of this structure is the AlGaN (Aluminum-GaN alloy, $20-30\,\text{nm}$) and GaN ($1-3\,\mu\text{m}$) heterojunction. This interface, the so-called 2DEG (Two-dimensional Layer of High-Electron Mobility), consists of the path (drain source) through which the electrons current flows. This phenomenon is a result of the crystal voltage polarity (between gate and source), which features an electric field. The silicon substrate forms the base plate of the device, and can also be built with other materials such as SiC, sapphire, or diamond. Here, the high thermal conductivity of SiC material and a better crystal lattice agreement with GaN makes the SiC substrate more attractive for GaN power devices. However, the growth of GaN on an Si wafer is cheaper, and is thus most suitable for industrial applications, due to the very high production capacity and low cost of silicon material. In order to deposit the GaN layer on the substrate, a buffer layer must be deposited to create an interface for strain relief between the GaN layer and the material outside [22].

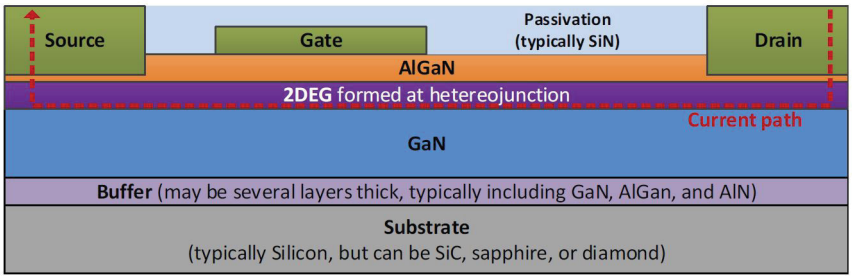
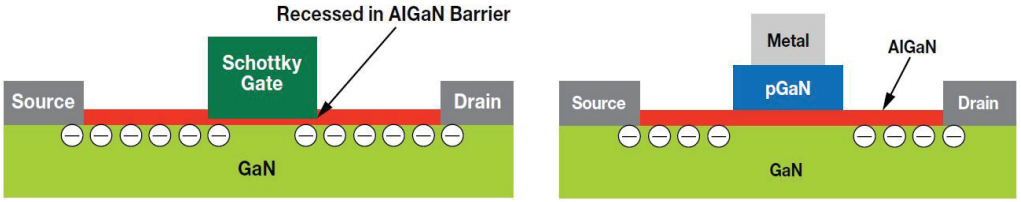


Figure 2.6: Basic structure of depletion-mode (normally-on) lateral GaN HEMT [3].

Normally-ON devices are not desirable in power electronics due to reliability concerns. Nowadays, normally-off power devices are built by shifting the threshold voltage (V_{TH}) positively, to make an enhancement-mode device. In Figure 2.7, the enhancement-mode structure can be seen for the two main different techniques. In Figure 2.7(a), the recessed gate is performed by thinning the AlGaN (Aluminum Gallium Nitride) barrier layer that is located above the 2DEG. Consequently, the voltage generated by the piezoelectric fields (AlGaN and 2DEG interface) is reduced, making this voltage lower than the voltage of the Schottky gate metal, which is a condition for having a normally-OFF device. Moreover, the recess must be performed accurately with an excellent

depth precision, in order to leave the 2DEG layer intact and precisely control the threshold voltage. In Figure 2.7(b), the pGaN gate is achieved by adding positive charges on the pGaN layer, which implies that a voltage larger than that generated by the piezoelectric effect. Therefore, a positive gate bias turns ON the 2DEG channel [3, 22].



(a) (b)

Figure 2.7: (a) Recessed gate e-mode transistor structure and (b) p-type GaN layer on top of the AlGaN [23].

The most popular technologies for GaN HEMT development in power electronics are E-mode HEMT (enhancement-mode HEMT) and GIT (Gate Injection Transistor). Both structures consist of the addition of a P-doped layer (AlGaN) beneath the gate that will locally deplete the 2DEG zone and consequently make the transistor naturally-OFF. However, the GIT solution is performed by fine-tuning the super-lattice buffer and the GaN epitaxial growth in order to relieve the stress, thus building resistive contact between the P-doped layer and AlGaN [22].

2.2.1.1 Current Collapse

The GaN transistor used for medium/high-voltage applications introduces a phenomenon called current collapse, which causes an increase in ON-resistance proportionally to the applied blocking voltage and the voltage pulse width (trapping time), as can be seen in Figure 2.8. According to the results presented in [4], the $R_{DC(on)}$ values may increase up to 4 after bias time of 1 ms, depending on the drain source voltage applied.

The physical mechanisms associated with the dynamic ON-resistance is the charge trapping close to the drain terminal, at the moment the device is in the OFF-state. An electric field between the gate and drain is formed, causing the charges of impurities in the surface passivation. During the following

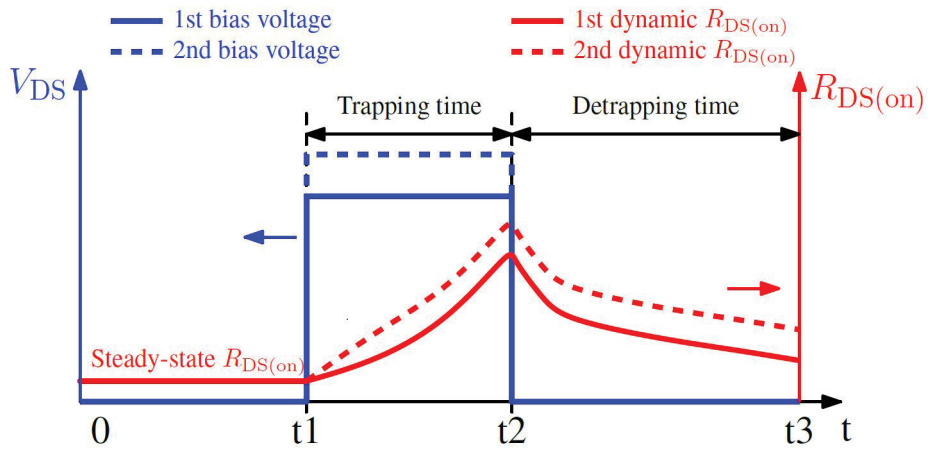


Figure 2.8: Dynamic $R_{DS(on)}$ values in function of applied V_{DS} due to trapping effects [24].

ON-state, the trapped region behaves like a virtual gate, increasing the resistance of the 2DEG channel ($R_{DC(on)}$). In addition, there is also the presence of "hot electrons" trapped in the buffer layer, which further increases the ON-resistance. In Figure 2.9, the mechanisms causing dynamic $R_{DC(on)}$ in GaN devices is described. This phenomenon is also related to the junction temperature of the device. For power converters, the switching frequency and duty cycle also have a strong effect on the overall increase in dynamics $R_{DC(on)}$, showing that these parameters define the behavior switching on the power device [22].

To mitigate the current collapse effect, field plates are used to balance the gate drain electric field, as seen in Figure 2.10. Normally, the substrate is internally connected to the source of the GaN switch, which helps in reducing the dynamic ON-resistance. In order to create a higher electric field to attenuate the trapping effect on 2DEG, Panasonic has proposed a solution called by HD-GIT (Hybrid Drain - Gate Injection Transistor). Further, Infineon uses the same technology for their GaN devices. An additional p-GaN layer is connected to the drain terminal, by generating a positive charges (holes) injection under the drain in order to face the current collapse. Theses positive charges generate an electric field that compensates for the hole generation in the buffer layer, thus, a more uniform region in regard to the resultant electric field can be achieved. Moreover, the holes emitted by the p-GaN connected to the drain recombine with the "hot electrons" during the following ON-stage [25].

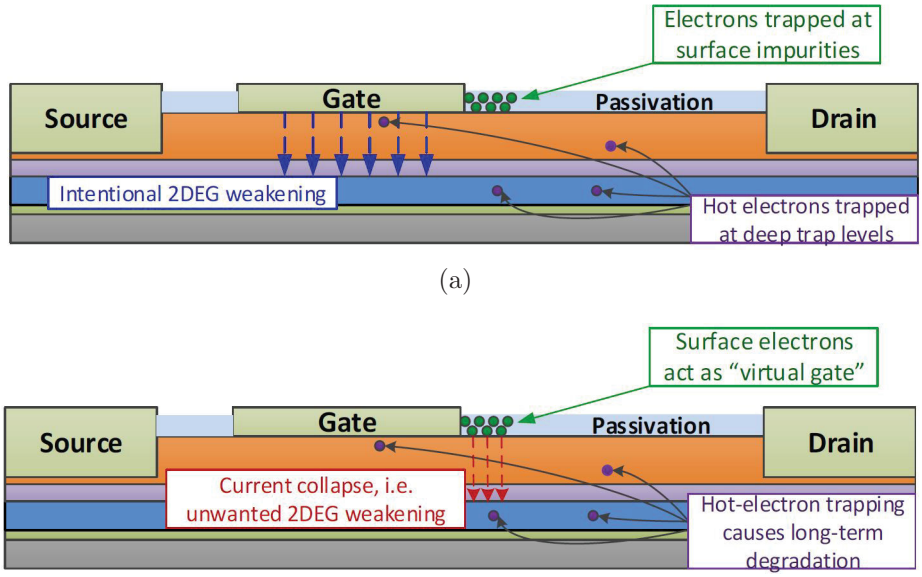


Figure 2.9: (a) Charges trapping when the blocking voltage is in OFF-state and (b) Consequences of trapped charges during the following ON-state [22].

In Figure 2.11, the convention structure and the HD-GIT are presented. In Table 2.5, are presented the GaN power devices used in this thesis.

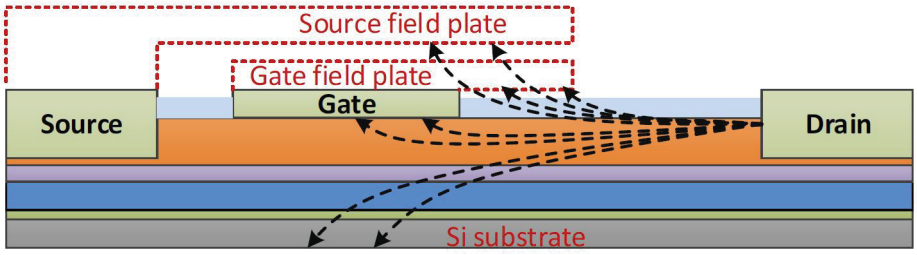
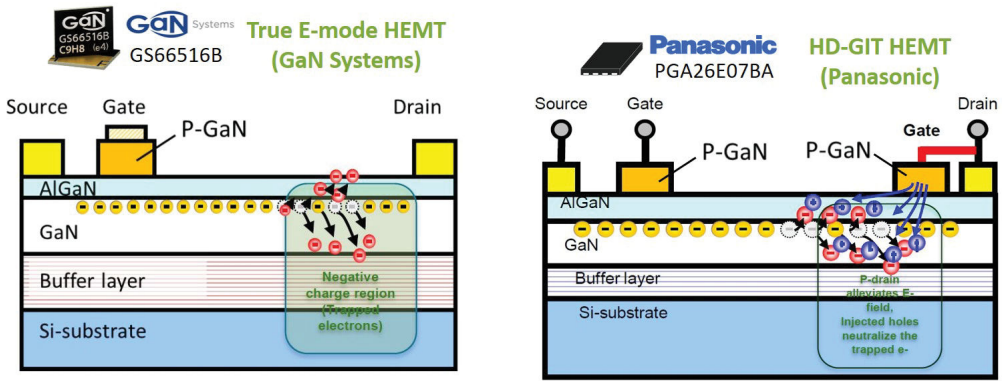


Figure 2.10: Field plates reshaping the gate drain electric field to mitigate current collapse [22].



(a) (b)

Figure 2.11: (a) Conventional e-mode GaN, and (b) Hybrid-Drain GIT for GaN-HEMT adapted from [26].

Table 2.5: Some characteristics of the GaN power devices used in this thesis.

Parameter	Symbol	Manufacturer			Unit
		Panasonic	Infineon	Gan Systems	
Part Number	P/N	PGA26E07BA	IGT60R070D1	GS66516B	-
Technology	-	HD-GIT	HD-GIT	True E-mode	-
Drain Source Voltage, max.	V_{DS}	600	600	650	V
Continuos Current, max	I_{DS}	31	31	60	A
Gate Current, max.	I_G	50	40	N/A	mA
Gate Voltage, max	V_{GS}	N/A	N/A	7	V
Thermal Resistance, junction-case	R_{thJC}	1	1	0.27	°C/W
Gate Threshold Voltage, typ.	$V_{GS(th)}$	1.2	1.2	1.7	V
On-state Resistance, typ.	$R_{DS(on)}$	55	56	25	mΩ
Gate Resistance	$R_{G,int}$	0.78	0.6	0.3	Ω
Input Capacitance	C_{iss}	380	405	518	pF
Output Capacitance	C_{oss}	72	71	126	pF
Reverse Transfer Capacitance	C_{rss}	0.3	0.4	5.9	pF
Total Gate Charge	Q_G	5	5.8	14.2	nC

2.2.2 Gate Driver for GaN

The gate driver design for GaN transistors is equivalent to the drive method for SiC MOSFETs. However, there are more specific requirements, as the threshold voltage of a GaN device is about 1-2 V [22]. The driving of GaN devices based on the e-HEMT and GIT-HD technologies is performed in different ways. The gate electrodes of the structure e-HEMT have a very high input impedance, and control of the device is accomplished by voltage. For the structure GIT-HD, the thin p-type layer added on the drain and gate layers acts as physical PN junction diodes. In this section, the fundamentals of

gate driver for GaN devices will be described.

2.2.2.1 Gate Driver Fundamentals

GaN transistors controlled by a voltage source (GaN Systems devices) have maximum positive (+7) and minimum negative voltage (−10) limits that can be applied to the gate electrode with respect to the source. However, these limits should be avoided to prevent damage to the device. A typical gate bias values for GaN e-HEMT are −3/6 V for the blocking and conducting states, respectively. This positive voltage bias is chosen in order to optimize the ON-resistance (R_{ON}) [27]. The intrinsic characteristics of the GaN power transistors imply some design considerations for gate drivers, especially at a high switching frequency. Here, two important design points are the false turn-ON and oscillations at the gate level [28].

In Figure 2.12, the basic structure for driving a GaN e-HEMT mode is presented. Separate resistors ($R_{G,ON}$ and $R_{G,OFF}$) are used to control the turn-ON and turn-OFF states, thus defining the slew rate. In this context, GaN Systems recommends a $R_{G,ON}/R_{G,OFF}$ ratio higher than 5 to 10 to minimize the Miller effect. A lower gate voltage operation is needed when compared to Si devices, as the gate capacitance of GaN devices is much lower than that of power switches made of Si material [29].

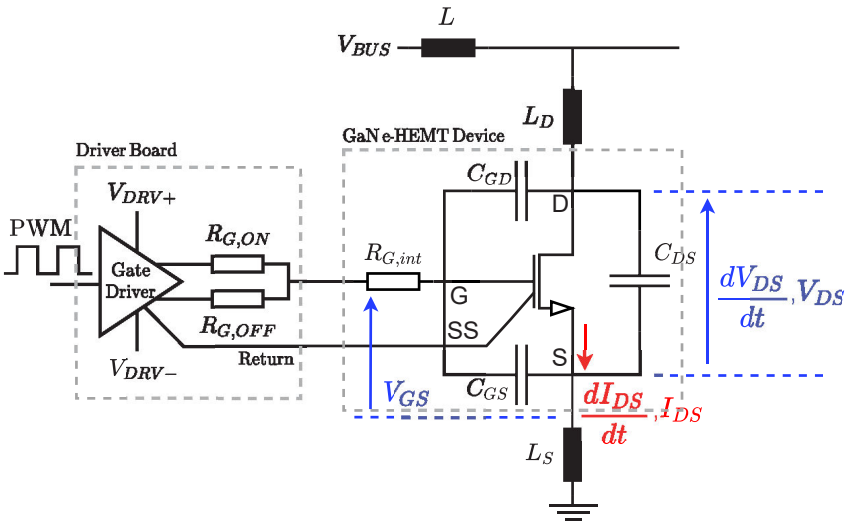


Figure 2.12: GaN e-HEMT with parasitic elements and the associated gate driver adapted from [27].

The GaN GIT-HD is a p-GaN type with a non-isolated gate that requires a constant gate current in the ON state. Thus, the device presents the gate input characteristics of a diode [30]. An RC network is used to provide two parallel paths to the gate, as seen in Figure 2.13. A low impedance path is composed of the speedup capacitance (C_S), which provides a high current at turn-ON/OFF, and the ON resistor ($R_{G,ON}$). These two components have the function of adjusting the gate current peak. Here, a high resistor (R_{ig}) is used to determine the steady state ON gate current. A negative gate voltage is guaranteed by the speed-up capacitor, that prevents the false turn-ON phenomenon. Further, the OFF resistor ($R_{G,OFF}$) prevents excessive gate voltage during turn-OFF [31].

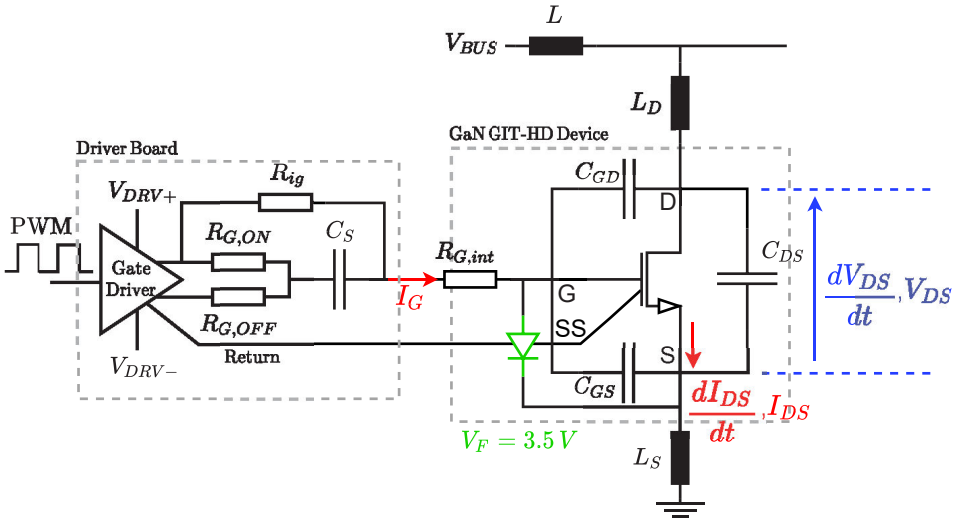


Figure 2.13: GaN GIT-HD with parasitic elements and the associated gate driver adapted from [31].

2.2.2.2 Characteristics and Design

To better understand the behavior of the gate driver, the LCR series resonant tank between the GaN device and gate driver can be seen in Figure 2.14. The equivalent resistance of the path driver/transistor, gate inductance, and equivalent capacitance of the driver/transistor constitute the resonant elements. An external resistor (R_G), as low as possible, should be used in order to reduce the speed switching. However, there is a compromise with oscillations and overshoot voltage at the gate. The higher this resistor is, the lower is the res-

onance effects. To attenuate these disturbances, the overall resistance $R_{G(eq)}$ must be equal or higher than the value given by the Equation (2.3) [32].

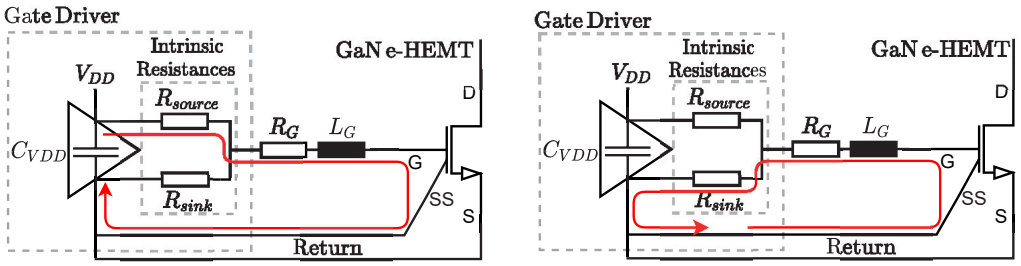
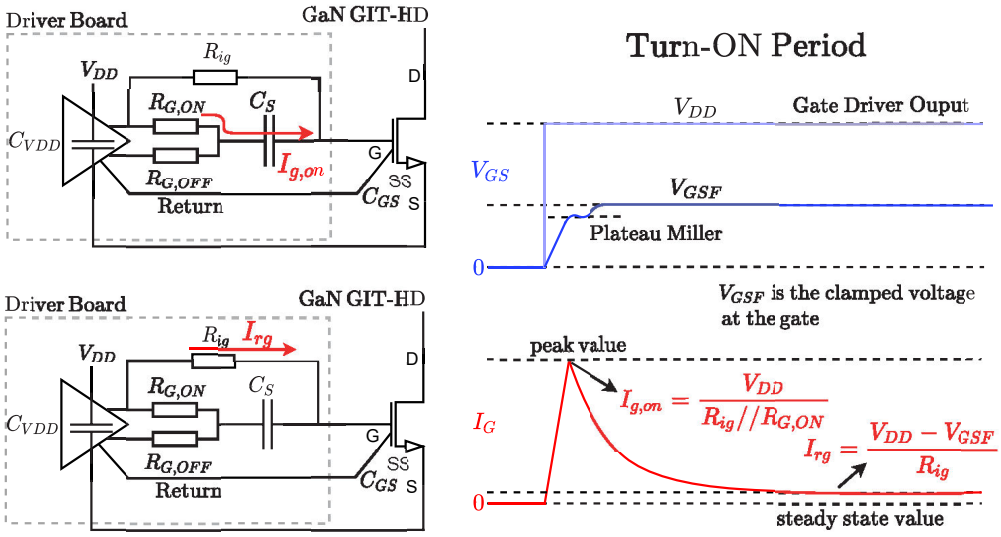


Figure 2.14: (a) Resonant loop formed between the gate driver and GaN device during turn-ON and (b) turn-OFF [32]. The red arrows represents the current direction.

$$R_{G(eq)} \geq \sqrt{\frac{4L_G}{C_{GS}}}, \text{ where } C_{GS} \text{ is the gate source capacitance.} \tag{2.3}$$

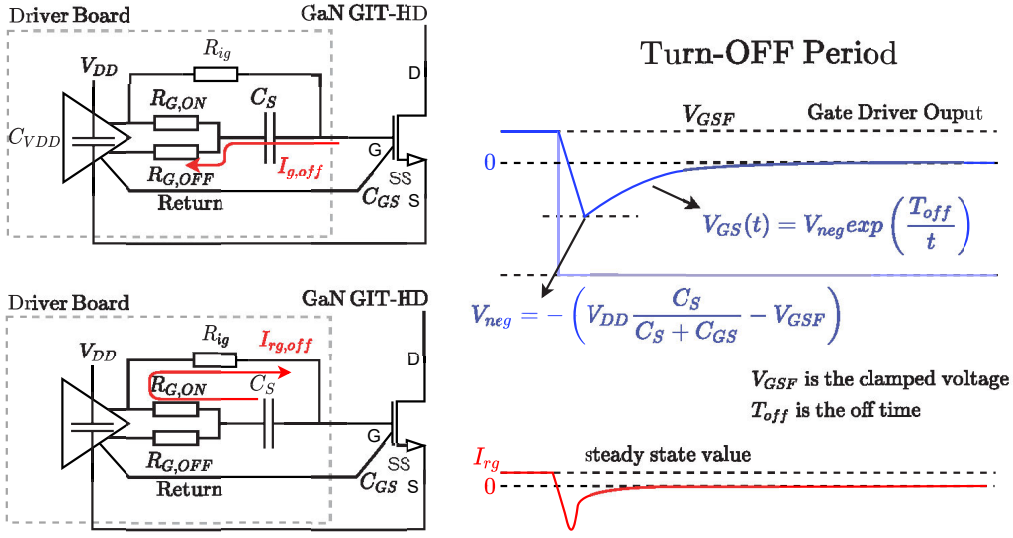
The GaN device based on GIT technology has a PN junction diode formed between the gate and source layers, and therefore a current must continuously be supplied to the diode to maintain the ON-state [33]. In this mode, the gate voltage is clamped at the bias voltage of the intrinsic diode (V_{GSF}). In Figure 2.15, the current mode gate driver, and the voltage and current waveforms for turn-ON transient are presented. A speed-up capacitor (C_S) is used to produce a gate current peak during the turn-ON transient. The ON resistor ($R_{G,ON}$) associated with the speed-up capacitor sets a time constant for the dynamic current [34]. The gate current peak value ($I_{g,on}$) can be adjusted by the ON resistor, and the gate current steady value is controlled by the resistor R_{ig}. These equations are shown in Figure 2.15. In Figure 2.16, the current mode gate driver, and the voltage and current waveforms for turn-OFF transient are presented. During this period, a negative bias is applied in order to attenuate the false turn-ON phenomenon [33].

Additionally,the equations associated with the drive components design are also shown in Figure 2.16. For the conception of the passive elements, it is important to consider the trade-off between having a faster switching or a good level for electromagnetic interference attenuation.



(a) (b)

Figure 2.15: (a) Current-mode gate drive circuits for gate injection transistors, and (b) the turn-ON transient gate voltage and current waveforms adapted from [33, 35].



(a) (b)

Figure 2.16: (a) Current-mode gate drive circuits for gate injection transistors, and (b) the turn-OFF transient gate voltage waveforms adapted from [33, 35].

The GaN e-HEMT power device controlled by voltage requires a low Under-voltage Lockout (ULVO) to prevent erroneous operation during transience be-

tween ON and OFF states. Therefore, the driver from Silicon Labs (Si8271AB) is used in this thesis. Gate drivers for GIT devices must supply a large gate current during the switching transient; thus a higher source/sink current is suitable, and the driver from Infineon (1EDB7275F-IS) was chosen. In Figure 2.17, the drivers from two different manufactures are presented. In Table 2.6, the comparison of some characteristics of the drivers can be seen. While there are other manufacturers for gate drivers presented in [21]. The drivers from Silicon Labs and Infineon meet the requirements for the different GaN device technologies.

Moreover, the fast switching of the GaN devices requires a carefully chosen gate driver. Characteristics such as intern resistance, rise/fall time of the pull-up/source, and pull-down/sink should be considered for driver selection. To avoid limitations on the switching speed during the overlap times, the rise/fall time should be lower than the turn-ON and turn-OFF delay times of the GaN device [36].

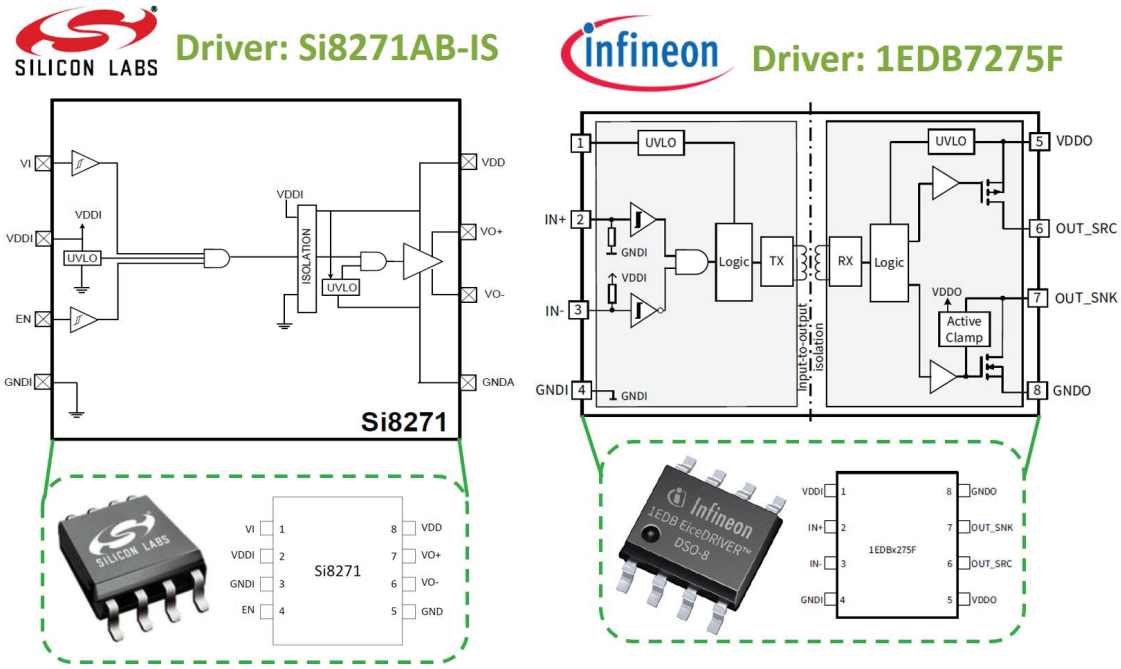


Figure 2.17: Functional block diagrams of drivers from Infineon and Silicon Labs for GaN devices.

Table 2.6: Comparison of the characteristics of two isolated drivers from Infineon and Silicon Labs for GaN Devices.

Manufacturer	Silicon Labs	Infineon
Reference	Si8271AB	1EDB7275F-IS
Isolation Voltage (kV)	2.5	3
CMTI (V/ns)	200	300
Source/Sink Current (A)	1.8/4	5.2/9.2
UVLO (ON/OFF) (V)	3.5/3	4.2/3.9
Rise Time (ns)	10.5	6.5
Fall Time (ns)	13.3	4.5
Propagation Delay (ns)	60	45
Low/High Output Resistance (Ω)	1/2.7	0.48/0.95
Package	SO-16	DSO

2.3 Electrical Characteristics of WBG Devices

This section introduces the general static and switching characterization processes that are applicable to WBG devices in terms of model validation.

2.3.1 Static Characterization

The static characterization phase consists of estimating the performance of the devices when in conduction or blocking states. However, the losses in the blocking state represent only a small part of total losses. The procedure of static characterization is performed according to the delivery of controlled pulses to the DUT (Device Under Test). Thus, the impact of the control signal on the transistor behavior is measured, by means of the analysis of the power channel. To limit the self-heating of the device, pulses of short duration are used ($< 500\,\mu$s) at a low frequency. In this case, it can be assumed that the junction temperature is equal to the package temperature (ambient) of the device [37]. In Figure 2.18, the Keysight B1505A Power Device Analyzer used for WGB characterization can be seen.

The characterization of a semiconductor device depends on the operating temperature. Normally, an additional heat plate can be used to heat the DUT, thus defining its junction temperature. A thermocouple attached to the device is used for measurement. The command signals sent to the DUT are performed by a GPIB (General Purpose Interface Bus). The performance evaluation of a power semiconductor device includes the DC (current-voltage relation) and

AC characteristics (impedance). In other words, the blocking capability, output and transfer characteristics, ON-state resistance, and reverse I-V curve can be evaluated [5].

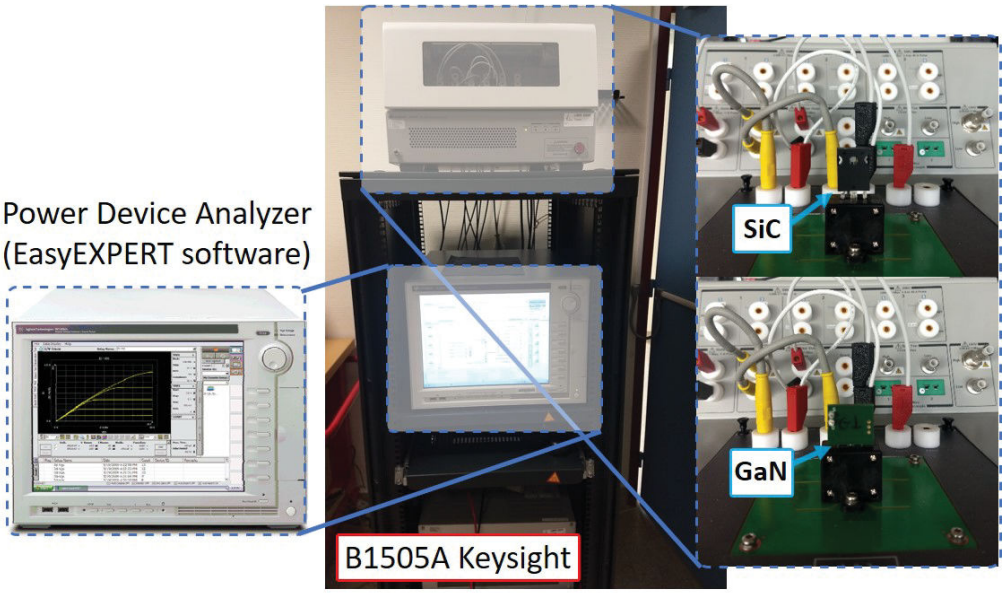


Figure 2.18: Curve Tracer Keysight B1505A for power device characterization.

An accurate measurement is directly related to some concerns before the tests are started. The wiring resistance can increase the gate resistance of the device, therefore Kelvin sensing should be used to eliminate this error. Furthermore, a fixed temperature needs to be ensured during the measurement, through the use of a heatplate, mainly for I-V characterization where a duty cycle smaller than 0.5 % should be defined. Simultaneously, the measurement data should be saved almost instantly to avoid junction temperature changes [5].

The blocking capability is one of the main characteristics of a power device, which is directly related to its lifetime. The drain source breakdown voltage (BV_{DSS}) is usually defined as the voltage that generates 250 μA drain leakage currents for SiC devices, considering the gate source terminals short-circuited [38].

In Figure 2.19, the output and transfer characteristics of a semiconductor power device are shown. Initially, the gate source voltage (V_{GS}) is lower than the threshold voltage (V_{TH}), therefore the transistor is OFF and the drain cur-

rent (I_{DS}) is zero, for any drain source voltage (V_{DS}) applied. The transistor is ON at the moment when V_{GS} is higher than V_{TH}. When $V_{DS} < V_{GS} - V_{TH}$, the relation $I_{DS}(V_{DS})$ is linear and its slope indicates the ON-resistance (R_{DS}). Subsequently, when $V_{DS} > V_{GS} - V_{TH}$, the drain current reaches its saturation value, causing $I_{DS}(V_{DS})$ to become non-linear (saturation region). In the saturation or linear region, the optimum value of the gate voltage should be applied to the device in order to produce an R_{DS} in the channel resistance that is as small as possible with maximum drain current flowing through the power device switch [39].

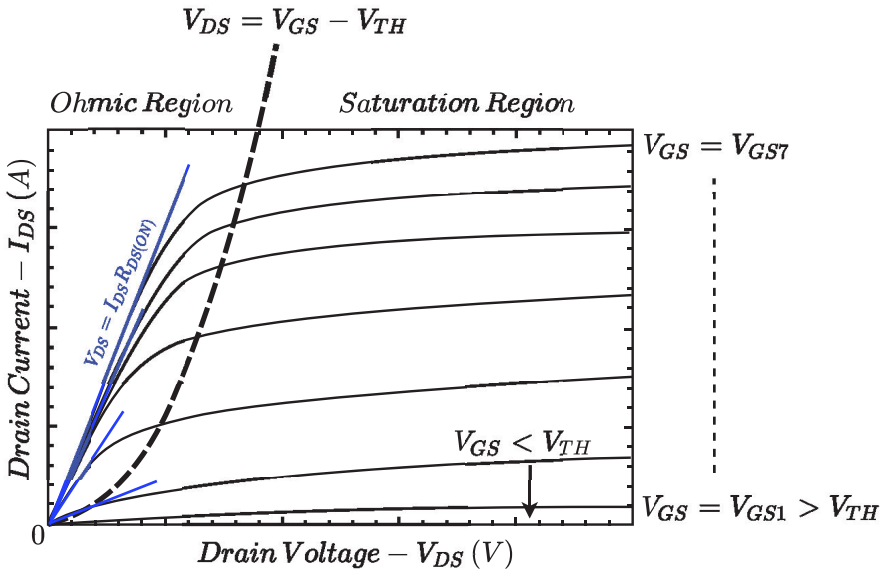


Figure 2.19: Static characteristic example of a metal–oxide–semiconductor field-effect transistor (MOSFET) (adapted from [39]).

The semiconductor power device behaves like a nonlinear current source controlled by the gate and drain source voltages during the steady state. When the transistor is ON, it operates in the ohmic region in order to limit its conduction losses. The gate source voltage and the junction temperature affect the physical behavior directly, given that in this region, the transistor becomes a variable ON-resistance $R_{DS(on)}$. When V_{GS} increases, $R_{DS(on)}$ decreases. However, it is necessary to respect the electrical limitations for the applied gate voltage.

The transfer characteristics of a power device depicts the drain current (I_{DS}) for a range of gate voltages (V_{GS}) with a fixed drain voltage (V_{DS}). The

value of (V_{DS}) should be chosen in the saturation region up to the maximum tested gate voltage. In Figure 2.20, an example of transfer characteristics for SiC and GaN devices for different temperatures can be seen. The main goal of this characteristic is to verify the threshold voltage (V_{TH}), voltage that the transistor starts to conduct, the forward transconductance (g_m), and the Miller voltage, the gate voltage at which a power device achieves a plateau before starts conducting [22]. For exemple, for the GS66516B GaN Systems device, the threshold voltage is obtained when I_{DS} equals 14 mA, for example. The transconductance can be calculated by the ratio between the variation of I_{DS} and V_{GS}, as seen in Figure 2.20. During the turn-ON stage, the Miller voltage is verified when V_{DS} starts to decrease.

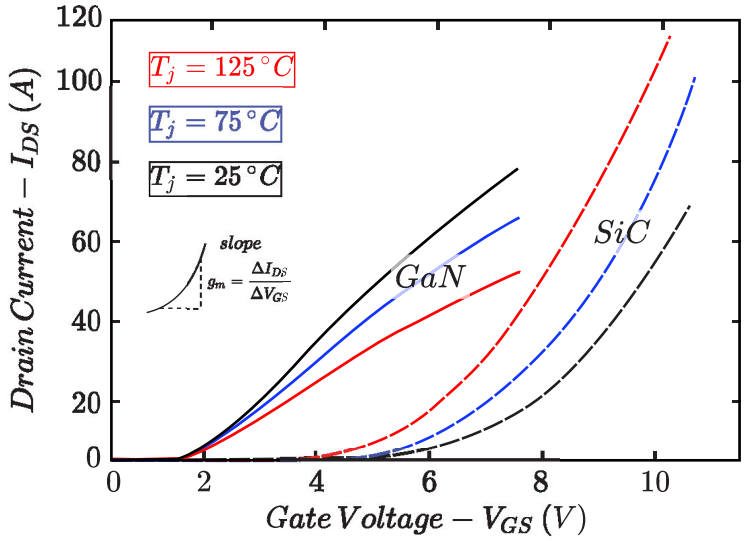


Figure 2.20: Example transfer characteristics of SiC and GaN devices adapted from [22].

2.3.2 Capacitance Characterization

The switching of a power device represents the dynamic behavior during transitions between OFF and ON states. During these phases, the capacitance values of the power switch influence the current and voltage waveforms. In Figure 2.21, an equivalent sub-circuit of a power transistor can be seen. The model consists of voltage-controlled current sources related to the voltages applied on terminals (drain, gate, and source), series resistors dependent on the junction temperature (T), and the capacitances. Meanwhile, the capacitance

values directly depend on the terminal voltages and decrease when the applied voltage increases [39].

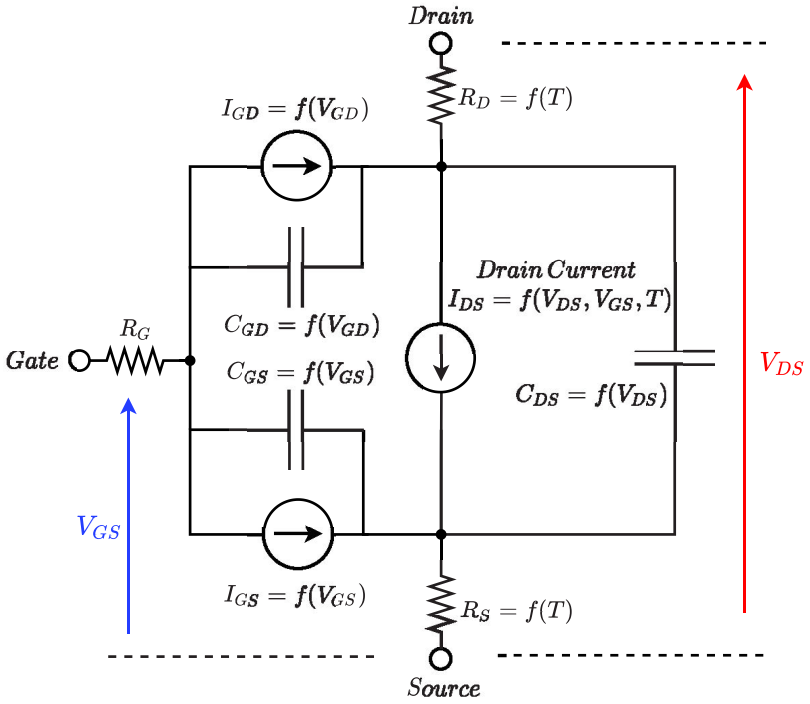


Figure 2.21: Nonlinear electrical model of a power MOSFET adapted from [39].

The intrinsic model shown in Figure 2.21 presents the current sources I_{GD} and I_{GS} for leakage current modeling. For simplification, the GaN device is treated as a power MOSFET in regard to its capacitance.

The capacitance voltage curves can be measured using the Keysight B1505A, as seen in Figure 2.18. The capacitances measured by the power device analyzer are formed by the gate oxide layer and PN junctions within the MOSFET. The sum of the junction capacitances is defined as input capacitance ($C_{ISS} = C_{GD} + C_{GS}$), the gate drain capacitance C_{GD} is called reverse transfer capacitance C_{RSS}, and the sum of the gate drain and drain source capacitances is defined as the output capacitance ($C_{OSS} = C_{GD} + C_{DS}$). The dynamic behavior of the power transistor is defined by these parameters. In this context, the reverse transfer capacitance (C_{GD}), also called by Miller's capacitance, is a nonlinear function of voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit [40].

As seen in Figure 2.22, the capacitance drops drastically in the lower voltages and then decreases very slowly as the drain source voltage continues increasing. The input capacitance is the sum of the Miller and the gate source capacitances, as previously mentioned. The Miller capacitance is strongly dependent on the drain source voltage, thus C_{ISS} is as well. However, the gate source capacitance component is not significantly affected by variations in drain source voltage. Therefore, the input capacitance curve is typically very flat in comparison to the other capacitance characteristics [5].

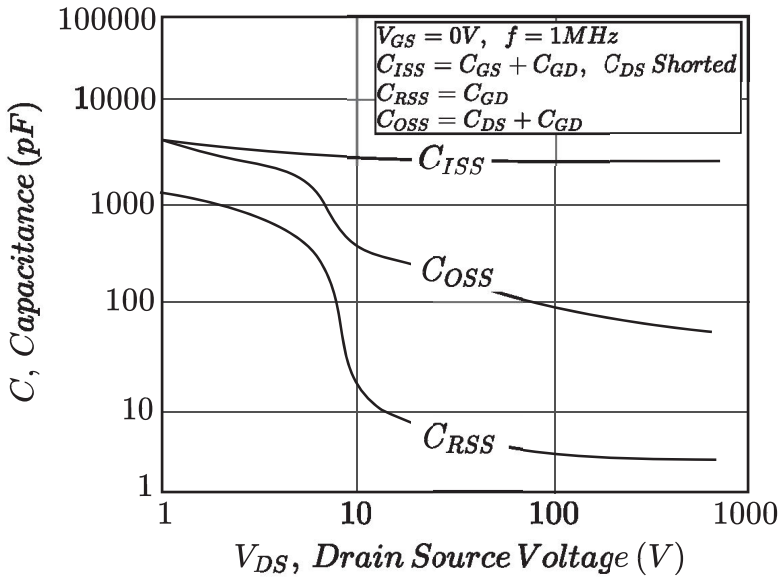


Figure 2.22: Typical capacitance characteristics of a power MOSFET [5].

While these capacitances have an important role on the switching losses, they are also involved in the parasitic resonances that arise during the switching transition, influencing the overall spectrum of the electromagnetic noise level, EMC (Electromagnetic Compatibility)aspects [41]. For instance, the output capacitance (C_{OSS}) has a strong interaction with the power loop inductance associated with the PCB design.

2.3.3 Switching Behavior

The performance of power semiconductors is related to the switching transient. The main important dynamic characteristics involve switching energy loss, transition parameters (rise time, fall time, and curve slope), dynamic spikes, and parasite ringing [42]. In order to understand the switching behavior of

a power MOSFET in a one-leg inverter (schematic for DPT), the switching transient is analyzed in an ideal case, without the consideration of parasitic elements. This approach allows for the better understanding of which variables are most important when it comes to comparing power semiconductor devices. Here, it is important to highlight that switching behavior is related to the parasitic capacitances, and thus the magnitude and relation between each variable C_{GD}, C_{GS}, and C_{DS} defines the performance switching of the power MOSFET device. Further, for the SiC device switching, the diode recovery time of the low side switch should be also considered.

The switching waveform of the power MOSFET **turn-ON process** is presented in Figure 2.23 [5, 43].

Time span 1: The input capacitance (C_{ISS}) of the power device is charged and the gate source voltage (V_{GS}) increases from 0 to V_{TH}. In this first step, most of the gate current is charging the C_{GS}. Simultaneously, C_{GD} is charging with a low gate current. During this time, the switch has not started conducting yet, and thus this period is called the turn-ON delay.

Time span 2: In this time period, V_{GS} has reached V_{TH}, and therefore the device starts conducting current. During this period, the drain source voltage (V_{DS}) is kept constant and equal to V_{DC} due to the output capacitor (C_{OSS}). When the drain source current (I_{DS}) reaches its nominal value, supplied by the DC current source, this phase is ended.

Time span 3: The drain source voltage (V_{DS}) starts decreasing from the initial value V_{DC}. This period is mainly characterized by the charging of the Miller's capacitor (C_{GD}) by the gate current, and thus the voltage V_{GS} is kept almost constant and equals to $V_{plateau}$. Simultaneously, the stored energy of C_{oss} is discharged. This phase ends when V_{DS} drops to the final value of $R_{DS(on)}I_L$.

Time span 4: The last stage of the turning-ON aims to reduce the ON-resistance. The gate voltage (V_{GS}) increases to $V_{GS(on)}$, which is higher than $V_{plateau}$, in order to provide a low channel resistance. During this period, both capacitors C_{GD} and C_{GS} are charged, and the drain source voltage (V_{DS}) is still reduced as the ON-resistance decreases.

The description of the power MOSFET **turn-OFF process** is similar to the turn-on process, as can be seen in Figure 2.24 [5, 43].

Time span 1: The input capacitance (C_{ISS}) of the power device is discharged, and the gate source voltage decreases from $V_{GS(on)}$ to $V_{plateau}$.

Time span 2: In this period, the saturation region is achieved, once that V_{GS} is equal to $V_{plateau}$. This phase ends when V_{DS} reaches the DC bus voltage (V_{DC}).

Time span 3: The device is in the linear region, and the drain current (I_{DS}) drops to a value near zero, which is defined as the end of this period. During this interval, the drain source voltage (V_{DS}) blocks the DC bus voltage (V_{DC}).

Time span 4: During the last stage of the turning-OFF, V_{GS} reaches zero, while the stored charge of the input capacitance keeps discharging. The drain source voltage and current remains constant.

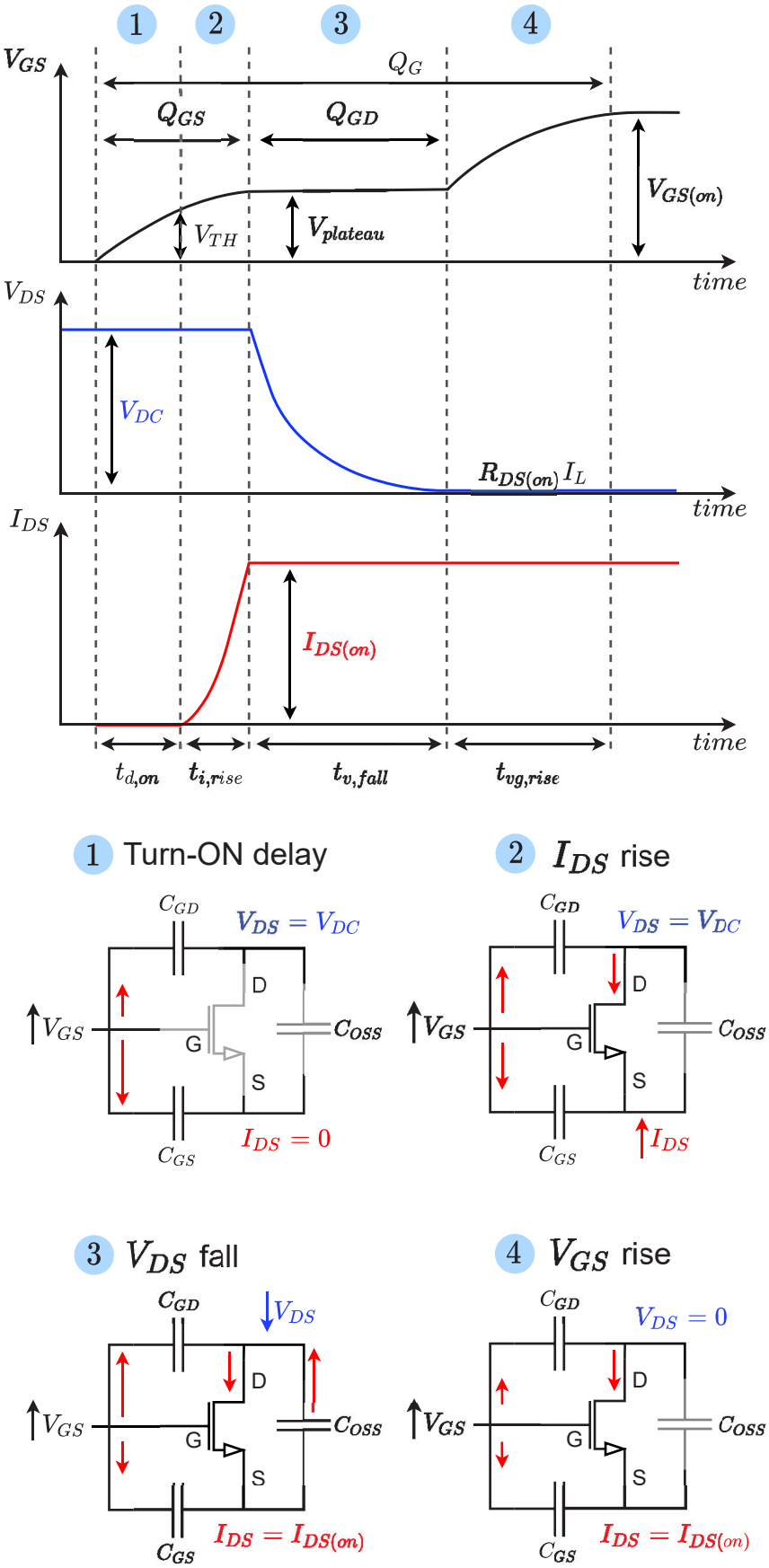


Figure 2.23: Ideal turn-ON process for a power MOSFET adapted from [5,43].

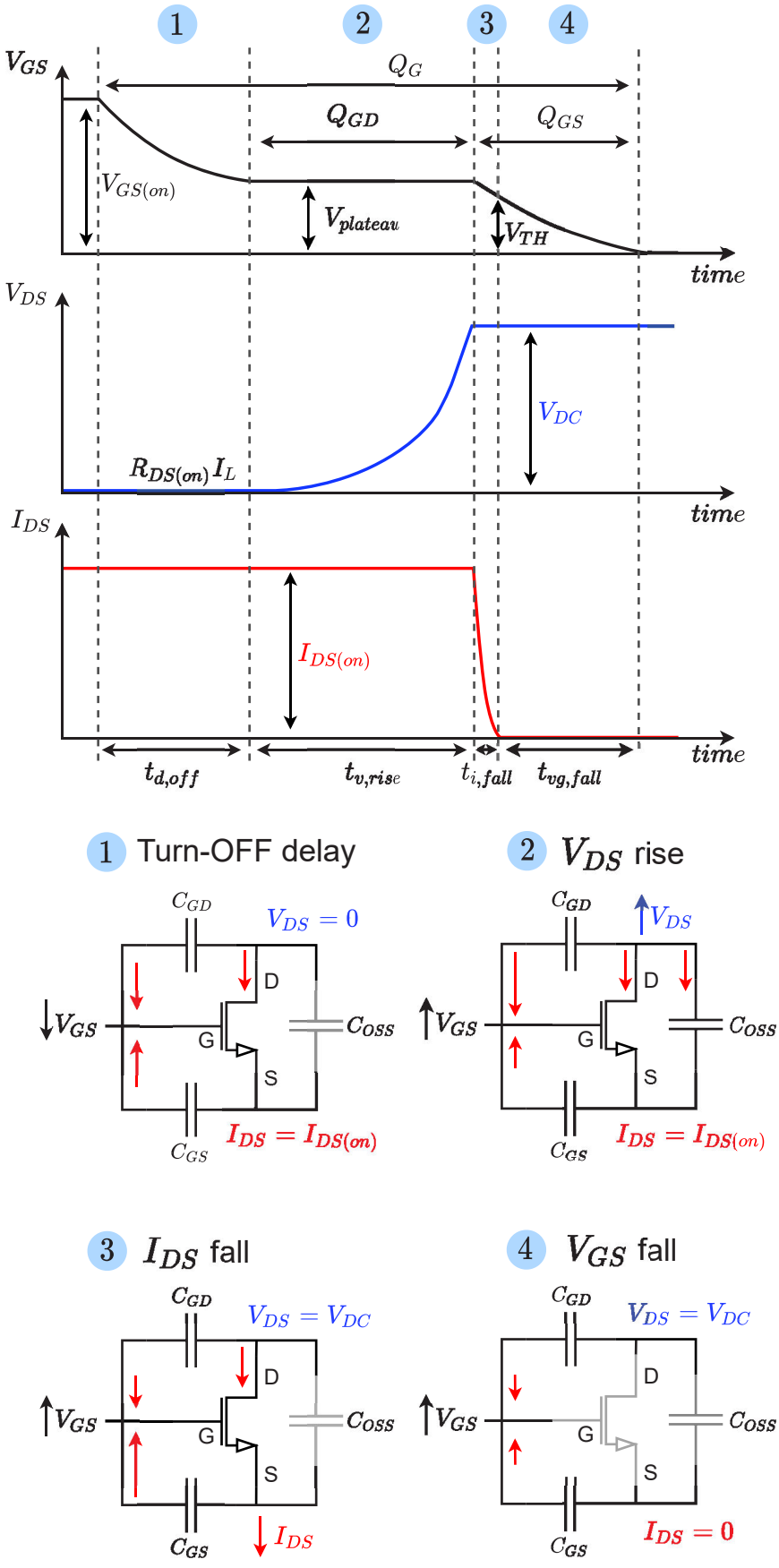


Figure 2.24: Ideal turn-OFF process for a power MOSFET adapted from [5, 43].

Table 2.7: Description of time variables presented in Figure 2.23 and Figure 2.24.

Symbol	Description	Phase
$t_{d,on}$	Turning-ON delay	Turn-ON
$t_{i,rise}$	Current rise time	
$t_{v,fall}$	Drain voltage fall time	
$t_{vg,rise}$	Gate voltage rise time	
$t_{d,off}$	Turning-OFF delay	Turn-OFF
$t_{v,rise}$	Drain voltage risetime	
$t_{i,fall}$	Current fall time	
$t_{vg,fall}$	Gate voltage fall time	

The switching waveform presents some disturbances when parasitic elements are considered in the circuit. These elements correspond to inductance, capacitance and resistance parasitics associated with the design conception of the PCB and interaction between circuit components.

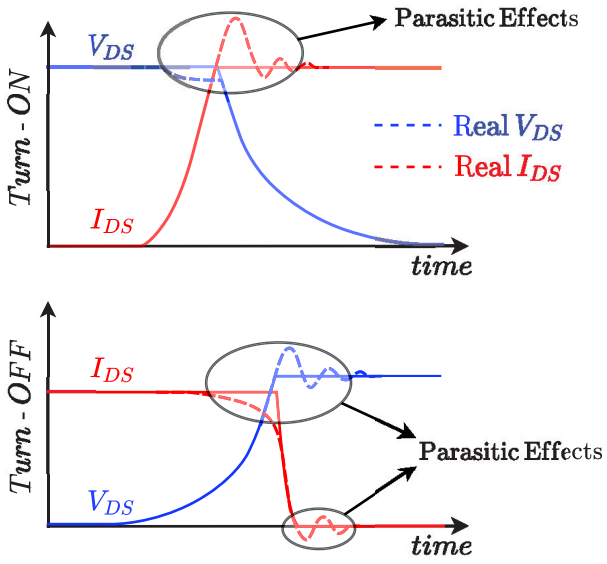


Figure 2.25: Effects of parasitic elements on the MOSFET switching waveforms adapted from [5].

In Figure 2.25, the ideal waveforms and a V_{DS} and I_{DS} considering non-idealist effects can be seen. These effects include the current spike during the turn-ON and voltage spike during the turn-OFF, as well as oscillations in the switching waveforms and increases in the path resistance of the power device.

The ringing presented in Figure 2.25, for example, is related to the resonance between the output capacitance (C_{OSS}) and power loop inductance [5, 44, 45].

2.3.4 Crosstalk Consideration

Crosstalking is a phenomenon in which one device is turned-ON due to the dv/dt on its Miller capacitance when the complementary device in the same phase leg is intentionally turned-ON. This conduction is performed from the DC bus through the saturated channels of both devices [46]. This phenomenon, also called the Miller effect, can be prevented by slowing down the turn-ON transient, namely that with a higher turn-ON gate resistance. However, this implies an increase in switching losses [22]. Another solution for crosstalk mitigation based on an active gate driver for SiC devices is demonstrated in [47]. For GaN devices, drivers provide low impedance during turn-OFF and separate paths (two output channels) during switching transitions, which allows for the use of a low OFF resistor [22]. An active approach for Miller effect attenuation in GaN devices is presented in [48]. Integrated gate drivers on both devices operate in a high frequency to mitigate crosstalk. The control device is actively controlled to create less crosstalk on both transients, by means of the adjustment of the gate impedance increasing the interference immunity.

Figure 2.26 the interaction between two switches in a switching cell is illustrated. In this topology, performed for DPT switching, the upper device (S_{HS}) behaves like a freewheeling diode. The main device is the lower switch (S_{LS}).

During the turn-ON of the low side switch, the rise of the drain source voltage (V_{DS}) on the high side switch induces a current on the Miller capacitance (C_{GD}). This current (I_{miller}) generates an overvoltage on the gate drive impedance ($R_G L_G$) of S_{HS}. At this moment, if the gate voltage overcomes the threshold of the power device, S_{HS} may start to conduct (false turn-ON). During the turn-OFF of the low side switch, the V_{DS} rise induces a Miller current towards the low side driver, which increases the gate voltage on S_{LS}, potentially causing a false turn-ON. Here, the V_{DS} fall of S_{HS} generates a negative peak V_{GS} on the high side switch (S_{HS}) [36, 46].

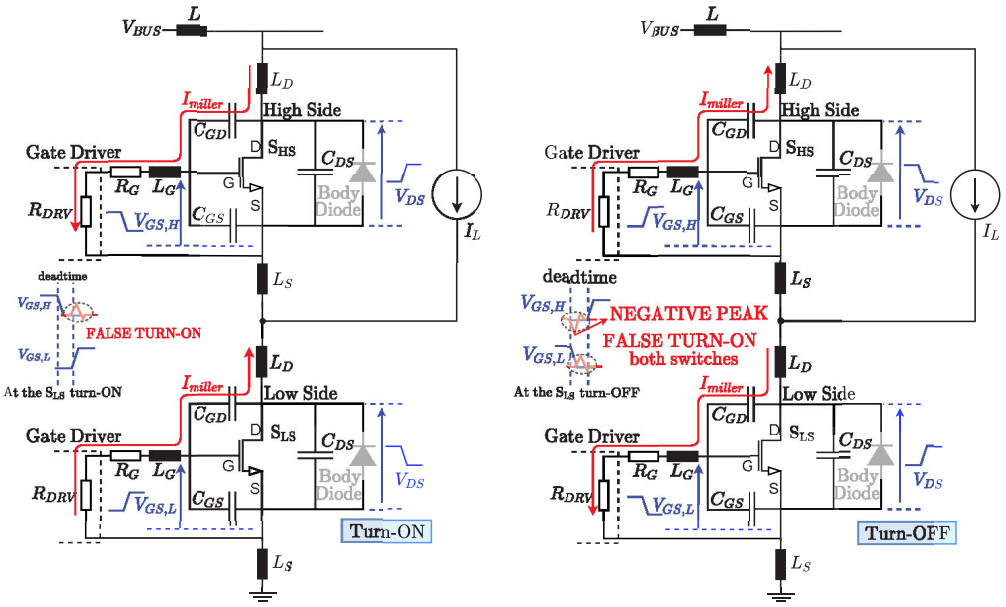


Figure 2.26: (a) Mechanism causing crosstalk interference at the turn-ON transient of the lower switch, and (b) at the turn-OFF transient of the lower switch adapted from [46, 48].

2.4 Switching Loss Estimation

Accurate estimation and modeling of the switching losses are essential to design converter power systems, mainly for operations with a high switching frequency. Furthermore, the volume of the cooling system is directly impacted by the amount of energy to be dissipated [49]. Moreover, while the WBG devices bring several advantages regarding performances, the switching of these devices is most sensitive to disturbances from parasitic elements related to the package and circuit board design.

For a simplified approach, a typical hard-switching ON transition for GaN e-HEMT is presented in Figure 2.27. The low side switch (S_{LS}) is the main switch, and the high side switch (S_{HS}) is the synchronous switch. Initially, the load current flows through S_{HS}. During the period in Figure 2.27(a), the diode-like reverse channel of S_{HS} starts the reverse conduction (deadtime initial point). Subsequently, the current commutation starts from the S_{HS} to the main device (S_{LS}), Figure 2.27(b). Here, once the current in S_{LS} achieves

the nominal load current, the voltage $V_{DS,LS}$ starts decreasing immediately, Figure 2.27(c). At this interval, the switching loss contribution comes from the DC current source (I_{load}), and the output capacitance of the high/low side switch ($I_{oss,HS}$ and $I_{oss,LS}$) [50]. The output capacitance $C_{DS,HS}$ is charged with the current from the DC bus and decoupling capacitors, whereas $C_{DS,LS}$ is discharged [36]. Finally, in Figure 2.27(b), the ON transition of S_{LS} is concluded. The low reverse recovery charge for SiC devices allows for the neglecting of the recovery time effect associated with the body diodes.

In the turn-OFF transient, the switch channel can totally stop conducting, before the end of the transient. In Figure 2.28, a typical hard-switching OFF transition for GaN e-HEMT is presented.

Initially, the load current flows through S_{LS} until the gate voltage reaches the Miller voltage, Figure 2.28(a). During this interval, shown in Figure 2.28(b), the load current begins to charge the output capacitance of the low side switch ($C_{DS,LS}$) and to discharge the output capacitance of the high side switch ($C_{DS,HS}$). Once the Miller plateau is achieved and $C_{DS,LS}$ is charged, the current in S_{LS} starts to decrease, Figure 2.28(c). Finally, in Figure 2.28(d), the OFF transition of S_{LS} is concluded [36].

However, the switching losses are more difficult to compute than conduction losses due to the short transition time between ON and OFF states. Moreover, to achieve an accurate switching loss estimation, the simulation waveforms should be as close as possible to experimental measurements. A precise loss estimation is useful to design the cooling system, calculate the efficiency, and define optimal operation regions of power converters [51]. The switching energy losses of a power switch are formed by the overlap of the voltage and load current on the device, as shown in Figure 2.27(e) for the turn-ON transition, and Figure 2.28(e) for the turn-OFF transition.

Equation (2.4) shows the time interval integral of the product voltage and current, power supplied to the switch. According to the first law of thermodynamics, the energy variation in a system is equal to the sum of the input power minus the losses. In a cycle, as for a DC-DC converter in a steady state, the energy supplied to the switch is equal to the losses. Thus, to fix this error source, the switching loss estimation is performed by the sum of turn-ON and

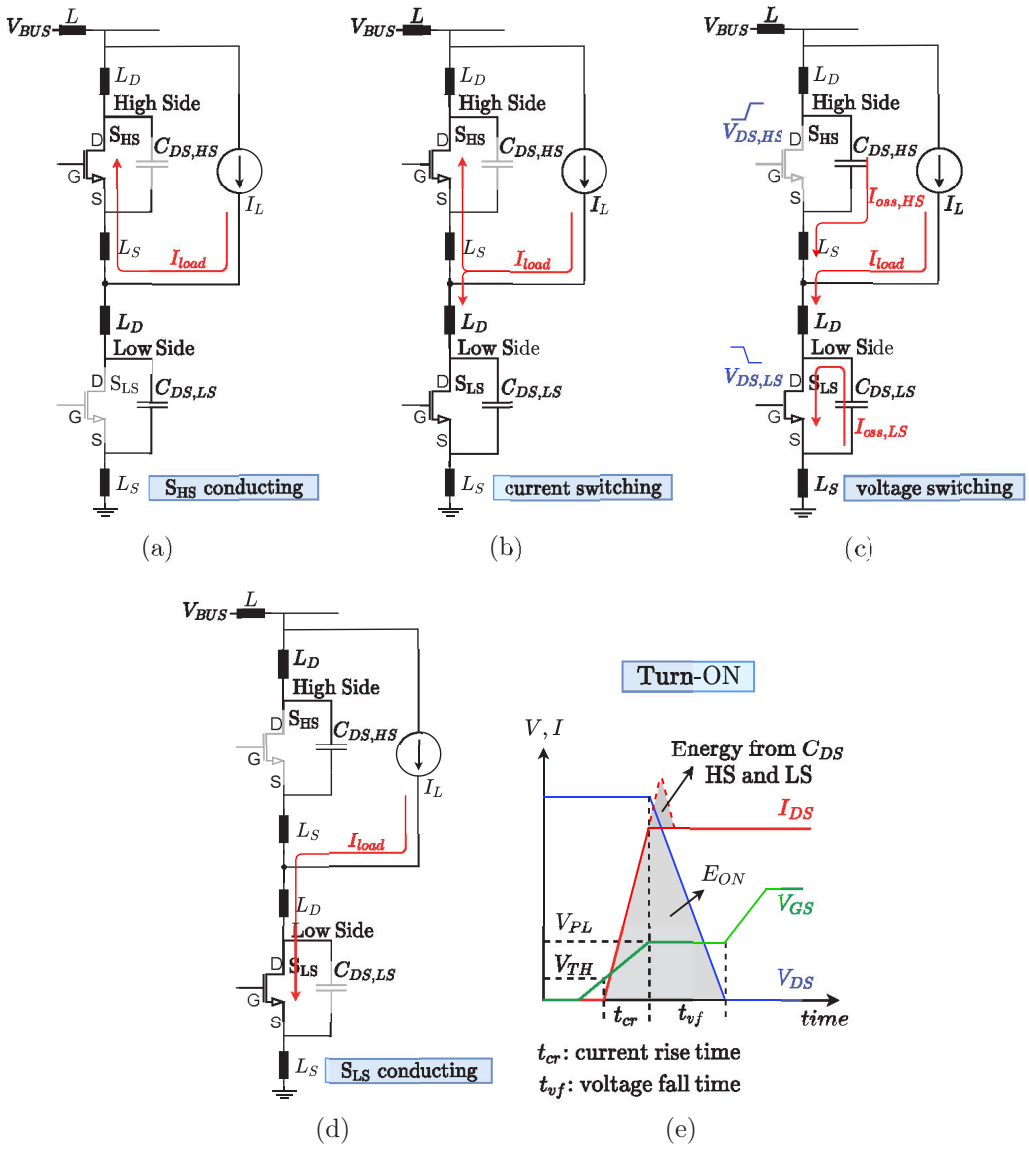


Figure 2.27: Hard-switching ON transition in a phase leg, (a) S_{HS} conducting, (b) Current commutation, (c) Voltage commutation, (d) SLS conducting, and (e) waveforms transient adapted from [50].

turn-OFF energies in a cycle, during a switching characterization test.

The switching loss during the ON state is the dominating part and is basically related to the parasitic capacitances of the switching cell circuit (synchronous switch, passive components, and printed circuit tracks) and the output capacitance of the main device [52]. Equation (2.5) and Equation (2.6) describe the switching energy due to the output capacitance ($C_{OSS} = C_{DS} + C_{GD}$) of the

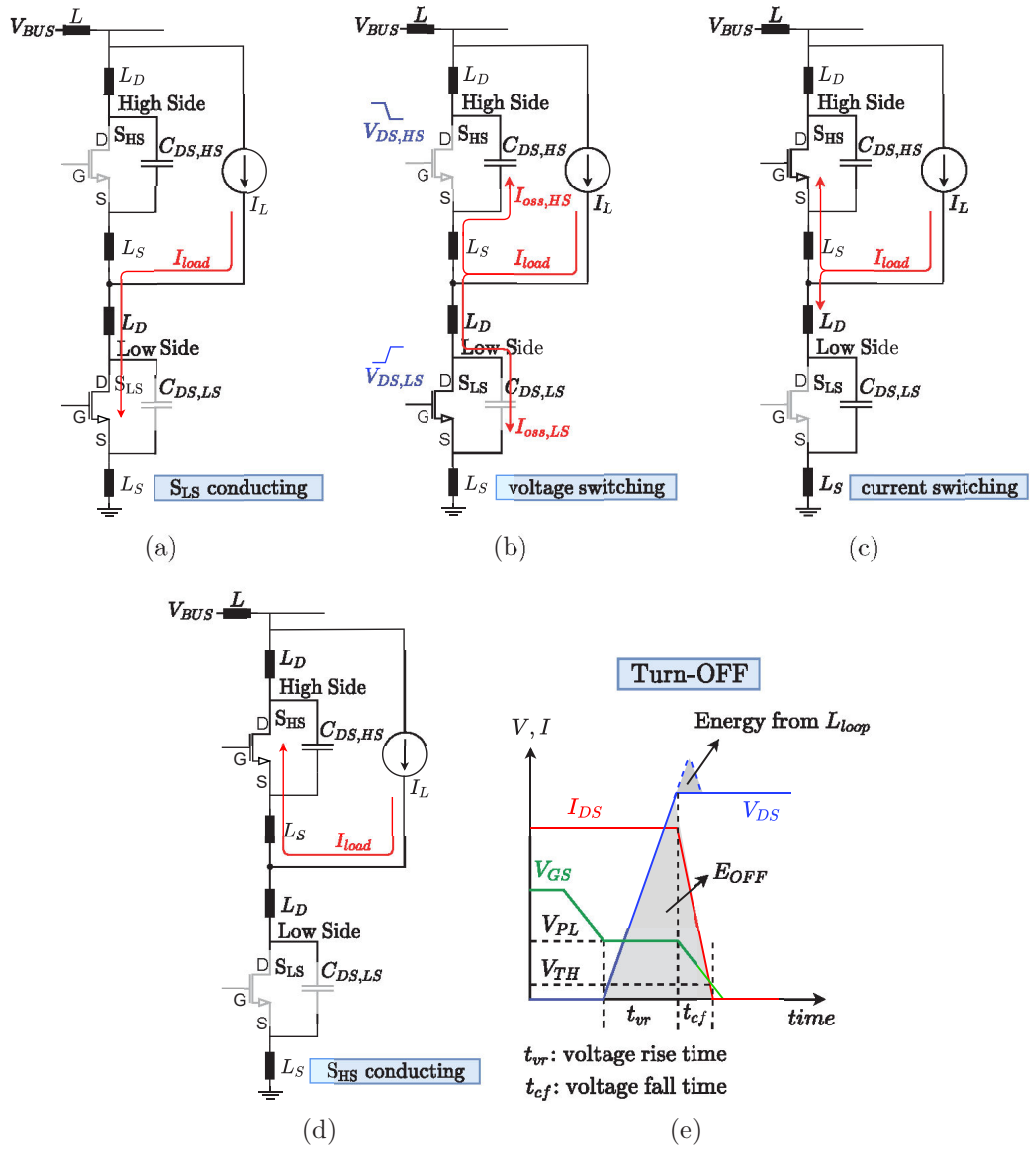


Figure 2.28: Hard-switching OFF transition in a phase leg, (a) SLS conducting, (b) Voltage commutation, (c) Current commutation, (d) S_{HS} conducting, and (e) waveforms transient adapted from [50].

main and synchronous switches, respectively. For the OFF state, part of the drain source current is used to charge the drain source capacitance (C_{DS}), and therefore the OFF switching losses are lower than that of the ON switching losses [50, 51]. Meanwhile, for a DC-DC converter, Equation (2.8) represents

the switching losses of a power device.

$$P_{sup(ON,OFF)} = \int_0^t V_{DS} \cdot I_{DS}\, dt, \text{ where [0,t] is the switching interval.} \quad (2.4)$$

$$E_{C_{OSS,LS}} = \int_0^{V_{BUS}} V_{DS} \cdot C_{OSS,LS}(V_{DS})\, dV_{DS} \quad (2.5)$$

$$E_{C_{OSS,HS}} = \int_0^{V_{BUS}} (V_{BUS} - V_{DS}) \cdot C_{OSS,LS}(V_{DS})\, dV_{DS} \quad (2.6)$$

$P_{SW(loss)} = f_{SW} \cdot (E_{SW(ON)} + E_{SW(OFF)})$, where f_{SW} is the switching frequency. (2.7)

$$P_{SW(loss)} = \frac{1}{2} V_{BUS} I_{load} (t_{ON} + t_{OFF}) f_{SW} \quad (2.8)$$

The energy stored in the output capacitance for WBG devices is much lower than that for devices based on Si material, which yields lower switching losses and better efficiency in hard switching applications.

Analytical models are also used for switching loss estimation. One of the most popular analytical loss models is the piecewise linear model presented in [53]. In [54] an approach also based on linearized MOSFET models is performed. With a faster switching carried out by the WBG devices, the parasitic elements modeling have become fundamentals for an accurate losses estimation, thus several experimental studies [55, 56] were conducted to improve the base analytical models. In [57] is considered the effect of low parasitic inductance, the non-linearity of junction capacitances, and non-linearity of transconductance. A set of equations are used to model switching transitions in order to obtain an equivalent circuit based on controlled sources and parasitic elements. A new method for calculating the average switching power losses of a MOSFET is proposed and described in [51]. This method is based on an algorithm for selecting a proper switching loss model, and the correct sampling of voltage and current waveforms. The comprehensive analysis of the impact of the wiring parasitic elements is performed in [8]. Experimental results are used in order to check the model accuracy of measuring instruments (voltage probe, shunt and current transformers). This approach allows validating the models used in Spice simulation, and thus estimating the switching losses more accurately.

2.5 WBG Devices for Automotive Application

Increasing efficiency in power conversion systems is the main goal in the current scenario of growing energy consumption. In fact, energy consumption is expected to increase by about 40 % worldwide in the next 20 years [58]. In this context, the devices (SiC and GaN) can reduce switching losses, leading to an increase in efficiency. Due to their wider band gap compared to those made of Si, these devices have the potential to operate in harsher environments, for instance, at high voltages and temperatures [59]. Moreover, several application areas can be identified as having a significant market for the usage of WBG devices: power supplies for data centers, renewable energy generation, motor drives for industrial applications, rail traction, and hybrid and electric vehicles [60]. However, in this thesis, automotive applications are the main focus.

2.5.1 Comparison of WBG Power Devices

The behavior of semiconductor materials varies between an insulator and a metal. Bound electrons take up distinct energy levels around the atomic nucleus, with two bands being the most important: the valence and conduction bands. The electrons presented on the valence band can move up to the conduction band, allowing for current flow. However, the energy needed for this displacement (bandgap) is much greater for WBG devices than those made of silicon [61].

In Figure 2.29, the potential applications of GaN devices in power electronics in the low/medium are shown. For comparison, the typical range application of the SiC devices is also indicated. In the range of 600 V-900 V, the coexistence of SiC/GaN power devices is noticeable, given that this range is suitable for automotive applications (DC-DC bus at 400 V) and PV grid connected inverters (200 V-400 V) [62]. The high frequency operation and system downsizing for power converters based on GaN material, and the high thermal conductivity and reliability of converters based on SiC material indicate competition between these devices, mainly for automotive applications due to the exigence of high power density. For high-voltage applications (1.2 kW),

the GaN devices depend on the development of vertical devices (cost reduction) and improvement of the quality of the material [62]. For example, base plate substrates of GaN components based on silicon carbide can improve thermal conductivity, but the manufacturing cost is still too high [3]. Several studies have shown that despite the higher cost of WBG devices compared to silicon, the increase of efficiency and reduction of the cooling system and passive components, can be enough to justify the implementation of WBG power devices [63, 64].

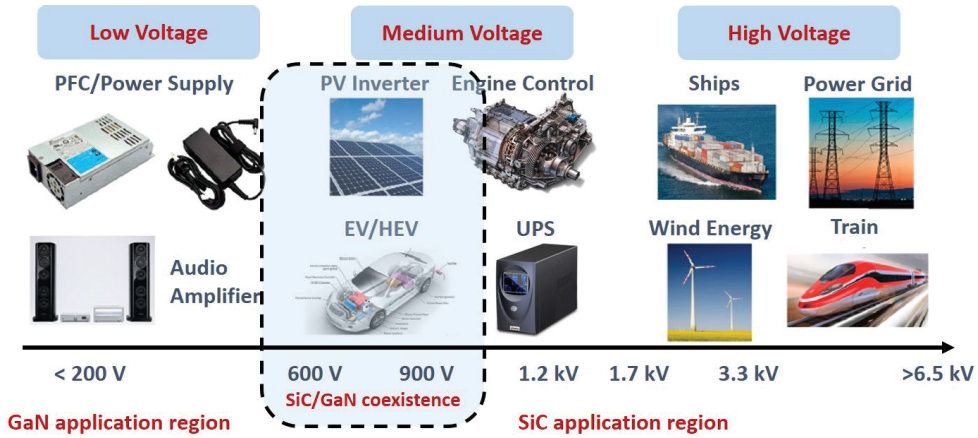


Figure 2.29: Possible applications of GaN power devices as a function of the voltage. The range of applications of SiC devices is also shown for comparison (adapted from [62]).

Moreover, SiC devices have a higher breakdown voltage operation and advantages in reliability tests (compared to the GaN), whereas GaN devices allow for working in higher frequencies, as they also have lower switching/conduction losses [65]. In Figure 2.30, the application domains of WBG devices is presented. The range around 100 kHz and 10 kW defines a middle point of the intersection region between SiC and GaN applications. In this context, several aspects have to be analyzed in order to decide which technology should be used such as project cost, available manufacturing techniques, the implemented cooling system, and the required level of power density. About the reliability of these devices, the SiC has a worst behavior compared to the Si-based devices, mainly due to its gate oxide, while the GaN devices are yet worst, seen the collapse current phenomenon associated with their conduction channel structure. However, the low drop voltage and fast switching of the WBG devices are suitable characteristics for several applications, such as

automotive systems.

A promising application for GaN devices is data center products such as servers, data storage, network devices, and power supply, because of their continuous energy consumption and the high integration level required. The reduced size of power converters operating in higher frequencies enables a higher number of servers per station. At the overall efficiency level reached by GaN-based converters, it is estimated that it takes about three years to return the added cost due to GaN device usage, which is undertaken by saving electricity [60].

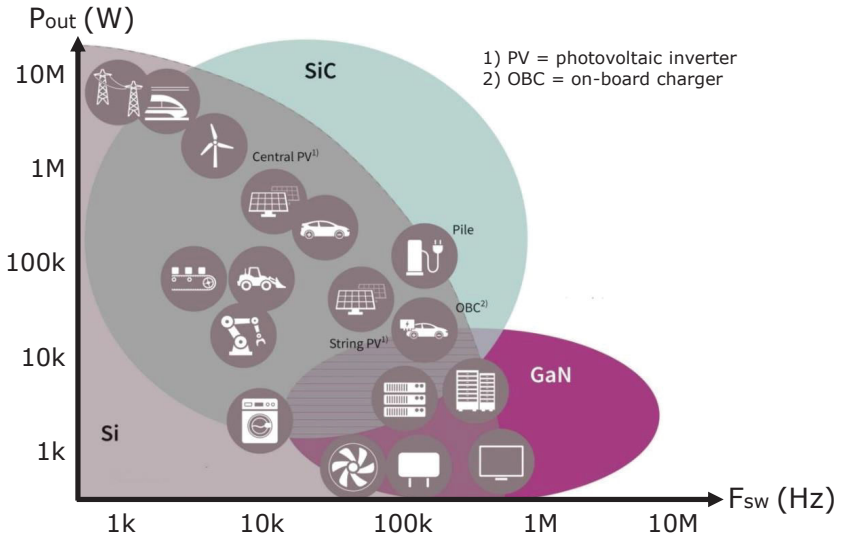


Figure 2.30: Semiconductor material power and frequency regions [66].

The conduction losses have an important contribution to total losses in power converters, mainly in terms of high-power applications. Figure 2.31 represents the ON-resistance as a function of the breakdown voltage for SiC and GaN components.

The border area around 1000 V shows an intersection region for WBG applications. Before this area, the reduced channel resistance offered by the GaN device allows lower conduction losses to be obtained. Nevertheless, in voltages higher than 1000 V, the required chip size to withstand this voltage level implies a specific ON-resistance (theoretical resistivity of an epitaxial layer that is lightly doped), which is more elevated than that of SiC switches. This is related to the technology maturing achieved in SiC device manufacturing.

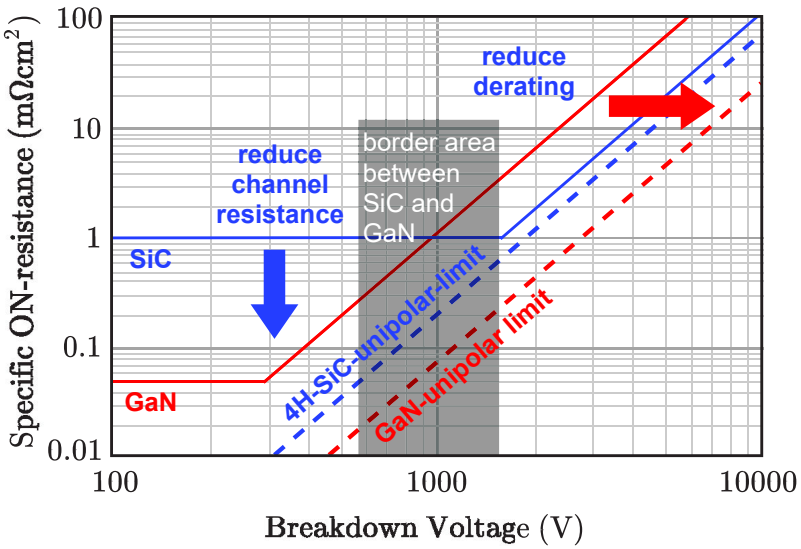


Figure 2.31: Specific ON-resistance: SiC versus GaN [2].

For a reasonable comparison between SiC and GaN in this area, the required relation of operation frequency and power level should be ensured. In other words, the conduction/switching losses at the temperature that the power converter operates at are used as comparative parameters [7,8]. In the field of automotive applications, the conventional DC-DC converter and the inverter in the powertrain use 650 V Si-IGBTs or MOSFETs [67]. DC-AC motor driver inverters are most compatible with SiC devices due to their operating temperature and low switching frequency (10-20 kHz), whereas DC-DC chargers are a good application for GaN devices due to their high frequency operation (up to 500 kHz) and power density requirements [60].

The comparison of the physical properties of Si, SiC, and GaN components is presented in Figure 2.32. The electron saturation and mobility are directly related to the maximum frequency operating ranges. Therefore, the GaN devices can operate in higher frequencies [68].

The critical electric field is the most important property as it allows for the building of smaller size power devices by implying lower switching/conduction losses. Moreover, the GaN material performs better in comparison with other materials. However, the higher thermal conductivity for SiC allows the power device to operate in temperatures higher than those of GaN and Si, considering the same cooling system [68].

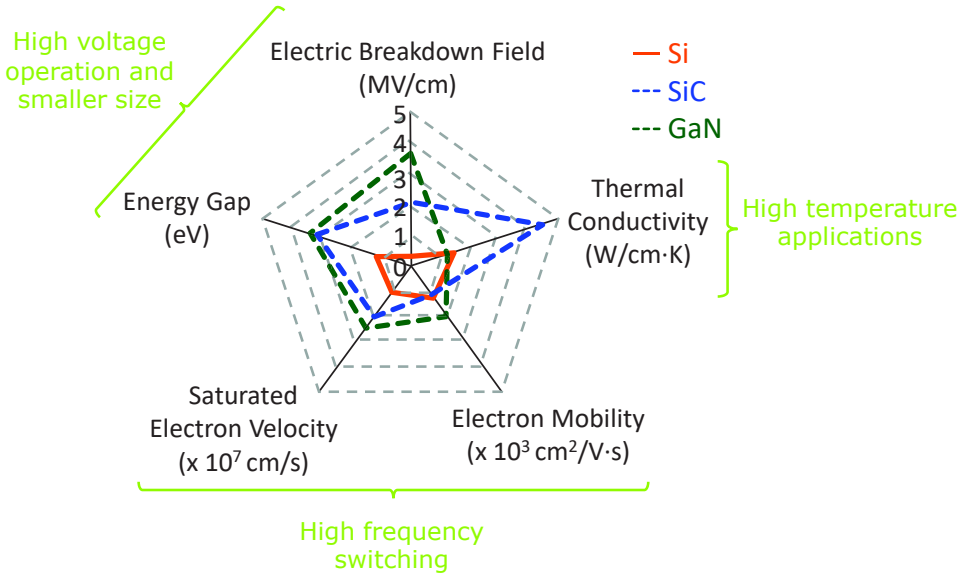


Figure 2.32: Comparison between Si, 4H-SiC, and GaN components (adapted from [22]).

The ON-resistance is a temperature dependency parameter because the path of electrons becomes more resistive due to the increase of particle movement. In terms of SiC MOSFETs, the drift region increases its resistance with the temperature, but the characteristic conduction of the channel generates a compensating effect. Meanwhile, the GaN HEMTs are more sensitive to temperature changes due to the temperature coefficient of the 2DEG [23]. An advantage of this temperature dependence is for power converters with parallel GaN devices, as the positive temperature coefficient helps in the balancing current [69]. In Figure 2.33, a comparison of normalized ON-resistance as a function of temperature is shown for SiC and GaN devices.

The lower gate charge of GaN devices, when compared to SiC devices, allows for faster switching, as seen in Figure 2.35. When turning-ON, the former is up to 4 times faster than SiC and in when turning-OFF, it is up to 2 times, but with similar $R_{DS(on)}$ [71]. This switching speed relation also depends on the driver parameters and PCB design. Faster switching transition implies to lower switching loss. Figure 2.35 shows a comparison of switching losses of two similar devices (nominal voltage and ON-resistance).

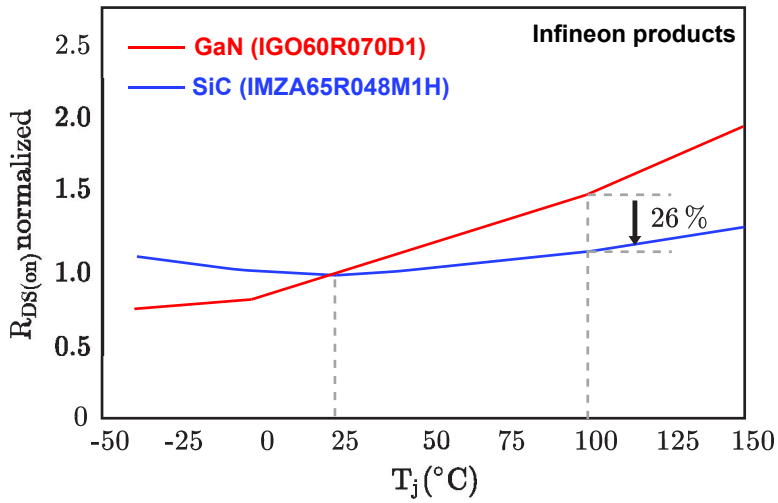
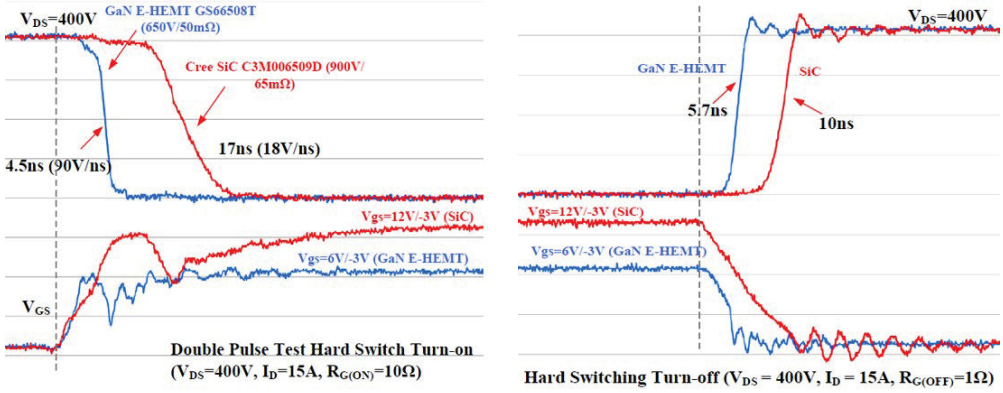
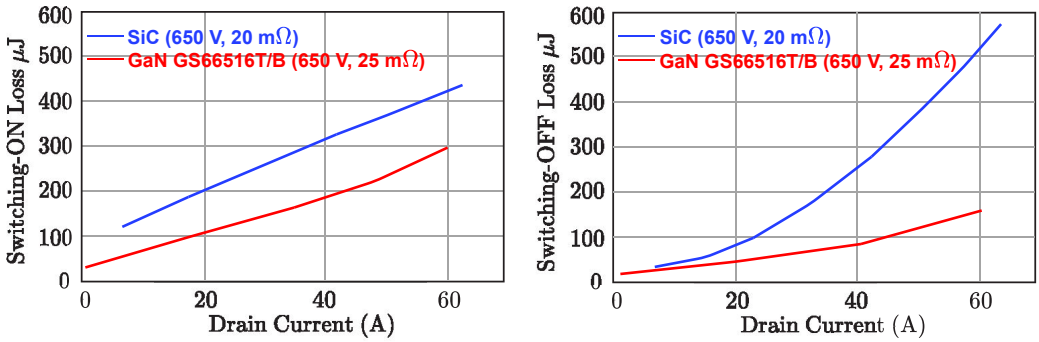


Figure 2.33: Comparison of the ON-resistance as a function of the semiconductor temperature for transistors, SiC MOSFETs and GaN HEMTs [70].



(a) (b)

Figure 2.34: DPT hard-switching of SiC and GaN devices: (a) turn-ON, and (b) turn-OFF transients [71].



(a) (b)

Figure 2.35: Switching loss of GaN and SiC devices that are 650 V rated with similar ON-resistance [72].

2.5.1.1 Figure of Merit

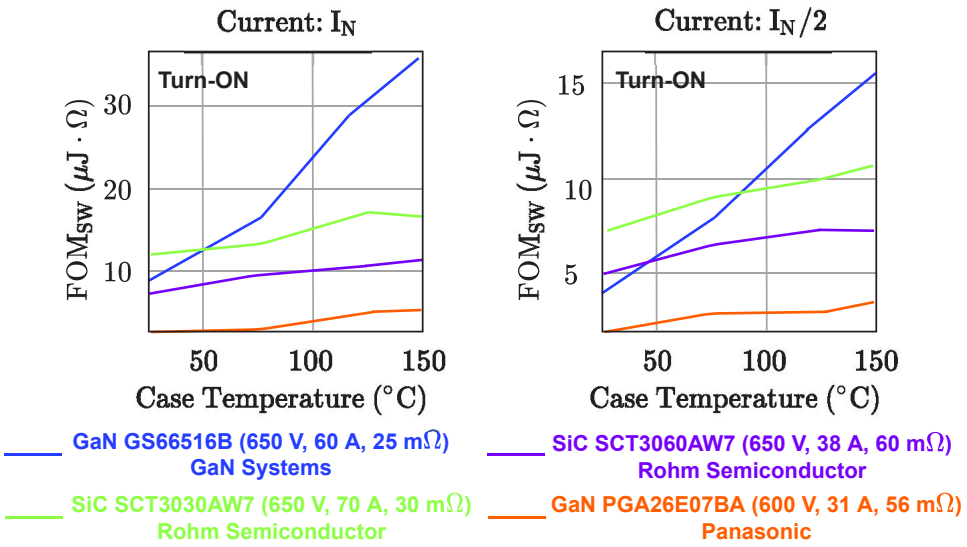
The automotive environment is characterized by high temperatures operation of power converters (up to 125 °C). To study the SiC and GaN devices in this condition, a switching FOM (Figure of Merit), FOM_{SW}, is defined in [7]. The product of ON-resistance and switching losses ($R_{DS(on)} \cdot E_{SW}$) for different temperatures allows a better understanding of the switching losses related to the temperature level. A DPT setup is used for the characterization of the switching behavior. In Figure 2.36, the results of the turn-ON and turn-OFF operations are presented for different SiC and GaN devices.

The GaN Systems device presents a strong temperature dependency behavior, mainly due to its enhancement-mode structure in terms of the 2DEG channel. The turn-ON losses dominate the total losses and until 50 °C, this device offers a lower FOM_{SW} compared to SiC devices. The GaN from Panasonic presents a better performance compared to the other devices, mainly due to its HD-GIT technology. In general terms, the GaN devices have advantages regarding losses, when compared to the SiC devices. However, the conditions can change at higher temperatures and different operating points (frequency and load) [7].

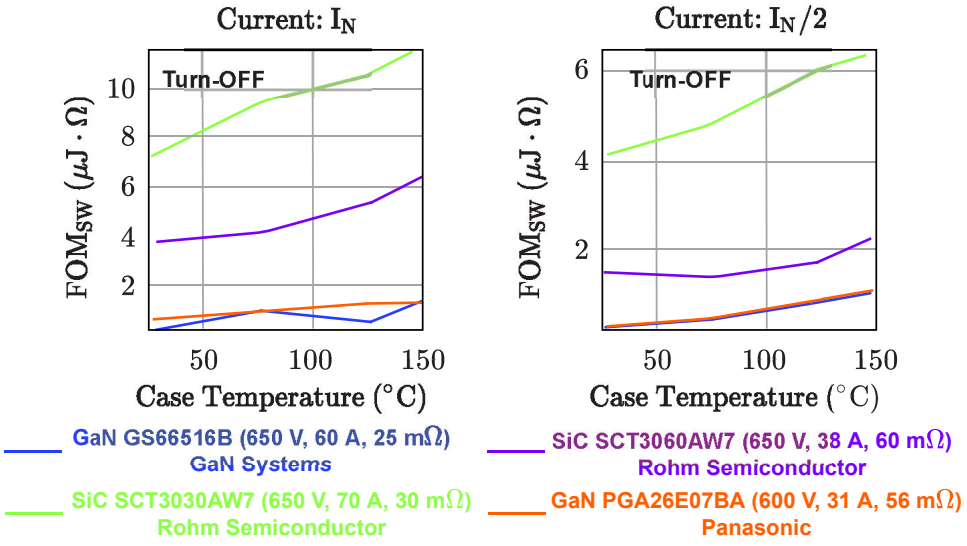
In [68], a comparison of different technologies of Si, SiC, and GaN was performed by SPICE simulation. An H-bridge inverter of output power greater than 1 kW and switching frequency of 13.56 MHz was implemented. The efficiency of the inverter based on GaN device was 13 % and 6 % greater than those of the converter based on Si and SiC, respectively.

The potential advantages of a power device can be evaluated with the Figure of Merit (FOM) concept. Moreover, the properties of semiconductor materials helps evaluate the power device performance, and many classic FOMs have been used to compare SiC and GaN as materials [73]. Furthermore, switching FOMs (ON-resistance times switching energy) are used in both SiC and GaN commercial devices [7].

In Table 2.8, three important FOMs are presented. The Baliga's Figure of Merit (BFM) evaluates the capability of a device to hold a blocking voltage, while maintaining a low specific ON-resistance [74]. Due to the higher



(a)



(b)

Figure 2.36: Experimental results: FOM temperature dependency during the (a) turn-ON and (b) turn-OFF stages at $V_{BUS} = 400\,V$ (adapted from [7]).

breakdown voltage, GaN devices perform better when compared to SiC. The Keys Figure of Merit (KFM) allows for the evaluation of the thermal and high frequency performance of the materials [75]. For KFM, SiC devices present better behavior, given that they have a thermal conductivity up to 3 times higher than GaN devices. Meanwhile, the Johnson Figure of Merit (JFM) indicates performance based on the high frequency and power of the materi-

als [76]. The GaN devices perform better, due to the higher breakdown field and higher saturation velocity as compared to SiC components.

Table 2.8: FOM for SiC and GaN components [62].

Figure of Merit	Si	4H-SiC	GaN
BFM	1	842	3175
KFM	1	4.61	1.6
JFM	1	576	2304

The figure of merit for WBG comparison in terms of energy losses is performed by the product of ON-resistance and another variable that indicates switching losses. In Table 2.9, these variables are the total switching losses of the device ($E_{ON,OFF}$), gate charge (Q_G, related to required gate drive power) and the dissipation of stored energy in output capacitance (E_{OSS}). The lower the FOM, the lower the losses. By comparing SiC and GaN devices with similar $R_{DC(on)}$ and nominal currents, the better performance of the GaN component at ambient temperature is visible.

Table 2.9: Figures of merit for 650 V/600 V rated switches in the differing semiconductor technologies. Values found in the datasheet.

Dynamic FOM	GaN Systems (GS66516B)	Panasonic (PGA26E07BA)	Rohm (SCT3030AL)	CREE (C3M0060065K)	Unit
$R_{DS(on)} \cdot E_{ON,OFF}$	3775	n/a	8400	8880	$(m\Omega \cdot \mu J)$
$R_{DS(on)} \cdot Q_G$	355	280	3120	2750	$(m\Omega \cdot$ C)
$R_{DS(on)} \cdot E_{OSS}$	425	392	510	900	$(m\Omega \cdot \mu J)$

The slow down factors of the growth market for GaN devices are mainly the cost and reliability concerns. GaN devices operate at a higher switching speed than SiC, which has much higher electron mobility, but their thermal conductivity is lower than SiC (up to 3 times less), so their power density potential is limited. Thus, the higher the nominal power for the converter, the higher is the match with SiC devices [61].

2.5.2 Automotive Application

The great challenge for the automotive industry is to decrease Greenhouse Gas Emissions (GHG) from vehicles. In this context, the electrification of vehicles has been rapidly increasing and power electronics has the function of making power converters increasingly efficient. Moreover, the advanced

research on electric vehicles (EVs) tends towards zero carbon emission [77], and the outlook for electric vehicle sales is rather positive, as can be seen in Figure 2.37. In 2020, 4.7 % of new passenger cars were electric vehicles, which represents a total of 3.1 million sold units. Further, new research from Canalys indicates that 48 % of passenger car sales will be electric vehicles by 2030 [78].

The WBG semiconductors offer several advantages that allow higher performance levels when compared to the standard Si technology. Higher operating temperatures, voltages, and maximum power can reduce the total losses, dimensions, and weights of electric vehicles, thus increasing the efficiency of the power electrical system. Each WBG device has its advantage depending on the application in the electric vehicle [79]. It is important to note that to design a power converter based on WBG devices, some care is required, such as optimizing the gate driver design and PCB layout, as well as implementing efficient thermal management [80].

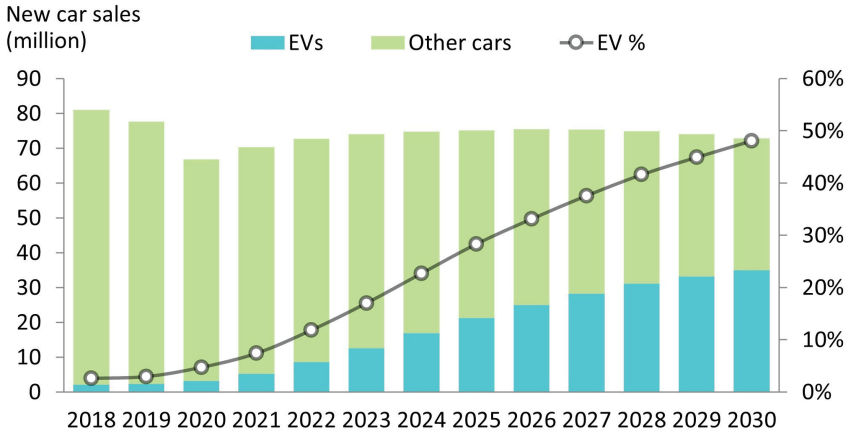


Figure 2.37: Outlook of global passenger car sales and electric car market shares [78].

In general, the EVs are divided according to how electricity is used to power the vehicles into three basic categories: Battery Electric Vehicles (BEVs), Plug-in Hybrid Electric Vehicles (PHEVs) and Hybrid Electric Vehicles (HEVs). In a BEV, the energy is fully electric and the battery is charged by an On-Board Charger (OBC) or external electric power source, besides the regenerative braking process. The PHEV is powered by an Internal Combustion Engine (ICE) and an electric battery. The external charging is possible by a

plug-in, and the batteries are powered similarly to the BEVs. Similarly, in an HEV, the power also comes from an ICE and a set of electric batteries, but the vehicle does not require a plug-in for external powering. Here, the batteries are charged via regenerative braking and optionally by an electric assist motor to the ICE.

The ecosystem of the electric vehicle can be seen in Figure 2.38. The traction High Voltage (HV) battery is powered by an OBC, which is in control of the energy flow between the charging station and the DC busbar. This charger must have high efficiency and high power density for minimum size. Due to the WBG devices and their high-power integration, more compact OBCs can easily be implemented [81].

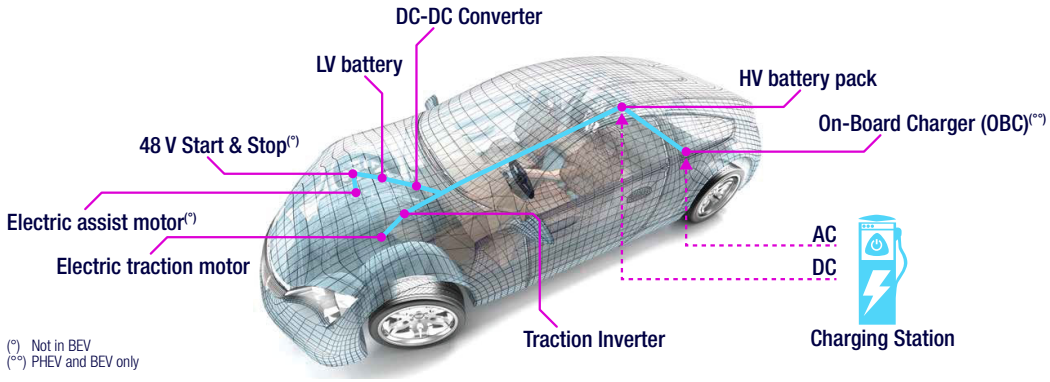


Figure 2.38: Block diagram of an electric vehicle powertrain [81].

The electric motor determines the driving behavior and is controlled by an inverter (DC-AC conversion) connected to the DC busbar. The robustness to withstand a harsh environment, low switching losses, and high thermal efficiency make SiC devices a strong candidate for this application. From the HV battery, a step-down chopper is used to generate the standard voltage (12/48) for the low-voltage battery used to power auxiliary circuits. Meanwhile, in a PHEV, there is still a high current DC-AC inverter that has the function of shunting down and restarting the internal combustion engine, thus reducing the operation time of the engine and improving fuel economy [81].

In an electric vehicle, the storage system is connected to the DC link. A bidirectional DC-DC converter can be used to provide a steady voltage on the busbar, which is the input of the motor inverter. Moreover, to improve the

efficiency of the DC-DC converter and reduce its size, the higher frequency operating allowed for GaN-based converters shows potential benefits. The HV battery is in the range of 200 V-400 V, thus the 650 V GaN switches now available in the market ideally match this application. The wireless charging is composed of coils to create a magnetic field that transfers the power towards the EV. Higher power amplifiers using GaN technology allows the wireless system to operate in a larger impedance range [67]. In Figure 2.39, concepts of power converters based on WBG devices are presented.

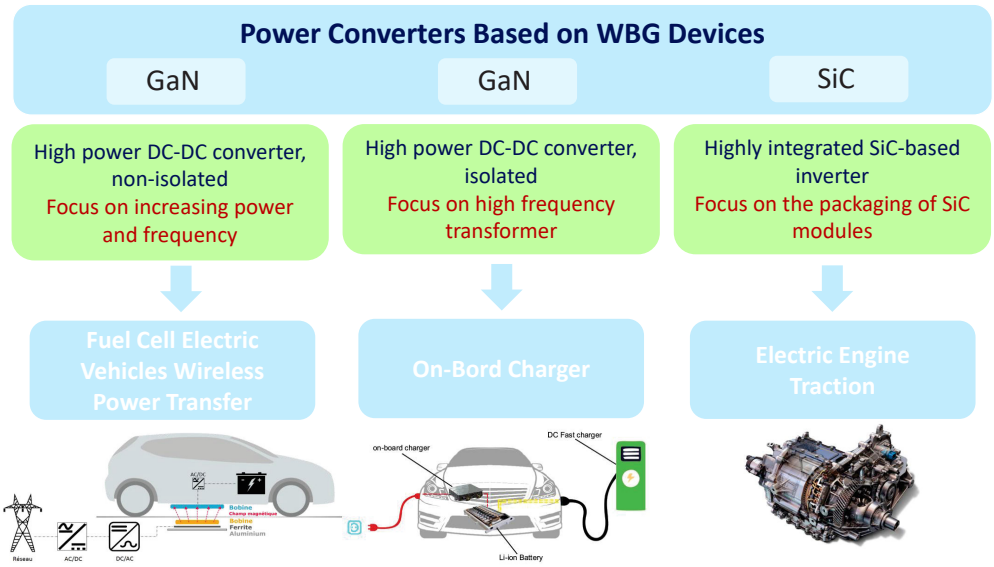


Figure 2.39: Typical power converters based on WBG devices (from VEDECOM).

The EV charging system may be present on-board the vehicle. A DC-DC isolated power converter is suitable for this application, thus the high frequency switching allows for designing high frequency transformers by highly reducing the converter size. The Power Factor Correction (PFC) converter, used between the charging station and the isolated DC-DC of the charger, includes filters that can also be reduced by the higher switching frequency [67, 82].

High-speed and low-inductance motors may be used in electric vehicles, allowing for the improvement of global efficiency. However, the switching losses of the inverter increase with the frequency, thus WBG devices are also suitable for this application. In particular, SiC devices are most compatible with this application, due to their higher thermal conductivity and high integration level presented by the power modules available in the market [67, 82].

Conclusion and Perspectives

The main subjects treated in this thesis were discussed in this chapter to offer a comprehensive approach to WBG devices in automotive applications. Initially, a SiC and GaN technology overview was performed, including the gate driver fundamentals presented by each power device. As part of the models validation used for simulation, the electrical characteristics are discussed, focusing on static and dynamic characterization methods. The switching behavior and switching loss estimation were also discussed for the later performance comparison of power devices. Finally, the benefits and drawbacks of the WBG technologies applied in electric vehicles were presented.

The WBG devices perform better in power converters due to their higher switching frequency, thermal conductivity, integration level. A comprehensive study on the SiC and GaN technologies helped clarify the reasons for their better performance in comparison to Si material. Moreover, even though WBG devices have a higher cost, high power integration and energy saving due to the high efficiency of power converters are aimed for automotive applications. It is important to highlight that the manufacturing price of these components has been decreasing over time. Nevertheless, for vehicle electrification, WBG devices are a key technology and can be expected to make EVs more efficient and economical in the near future.

CHAPTER 3

Power Device Characterization

The power device characterization is performed in static and dynamic modes for SPICE model validation. The characterization of WBG devices should be performed finely to develop reliable models in the simulation. The output and capacitance characteristics are obtained as part of the model validation. Moreover, the test protocol should be performed carefully, given certain characteristics of WGB devices such as a high sensibility on the gate, trapping effect and low threshold voltage. For instance, the measure of the drain leakage current characteristic could modify the I-V response due to the trapping/detrapping within the GaN components. Therefore, the output and capacitance characteristic tests are performed for two different samples, and without any previous leakage current measurements [8]. The goal of this section is to compare datasheet, simulation and experimental results for different WBG devices at ambient temperature and under operation at maximum temperature. The devices for the tests are presented in Table 3.1. For each device, two samples were used. The transistor characteristics are measured with a Curve Tracer Keysight B1505A (500 A - 10 kV), shown in Figure 3.1.

3.1 Static Characterization

The static characterization phase involves in estimating the performance of the devices when in conduction or blocking modes. This procedure was previously described in Section 2.3. The first test performed concerns to output

Table 3.1: Selected power semiconductor devices with typical properties.

Component	Manufacturer	Material	Type	Vnom (V)	Inom (A)	$R_{DS(ON)}$ ($m\Omega$)
GS66516T Samples: G1;G2	GaN Systems	GaN	eHEMT	650	60	25
PGA26E07BA Samples: P1;P2	Panasonic	GaN	GiT	600	26	56
SCT3030AW7 Samples: S3;S4	Rohm	SiC	MOSFET	650	70	30
C3M0060065K Samples: W1;W2	CREE	SiC	MOSFET	650	30	60

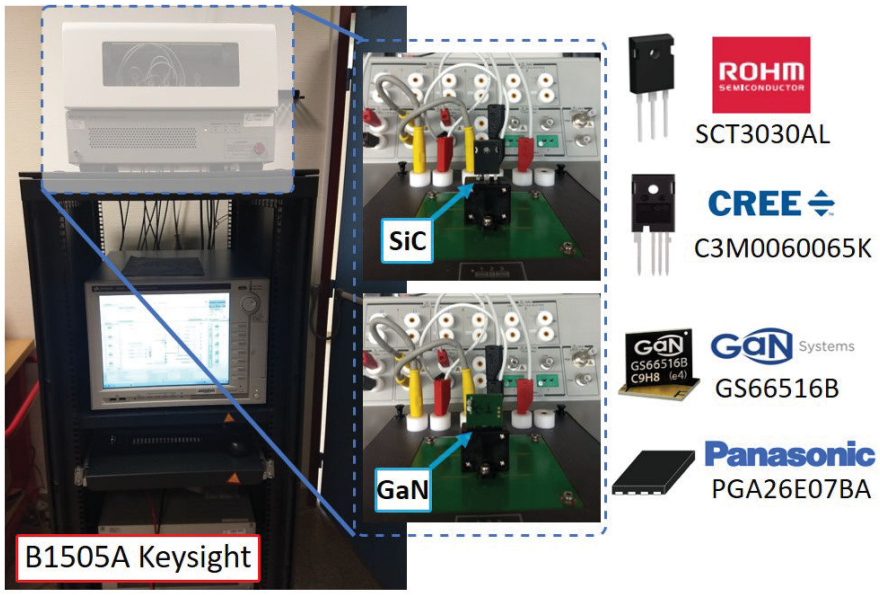


Figure 3.1: Curve Tracer Keysight B1505A and the devices used in this study. For GaN devices, a small PCB board connect TO247 package was used.

characteristics. The drain current (I_{DS}) is plotted versus the drain source voltage (V_{DS}) for different gate source voltages (V_{GS}). This allows the understanding and modeling of the trajectories during the switching transient. Figure 3.2 illustrates the turn-ON and turn-OFF trajectories for the ideal condition, namely without considering parasitic elements [5]. The second test deals with the transfer characteristics. The drain current (I_{DS}) is plotted in function of the gate source voltage (V_{GS}) under a constant drain source voltages (V_{DS}). With this test, it is possible to verify the threshold voltage V_{TH}, voltage at which the switch starts conducting.

During the turning-ON, seen in Figure 3.2(a), phases 1 and 2 represent the time taken to achieve the Miller plateau. Phases 3 has a constant V_{GS}, and phase 4 defines the switching final point. For the turning-OFF, the inverse

scenario can be adopted as an explanation. Here, a good correlation between the output characteristics in simulation and experimental results is important to validate the power device models and to obtain an accurate switching loss estimation.

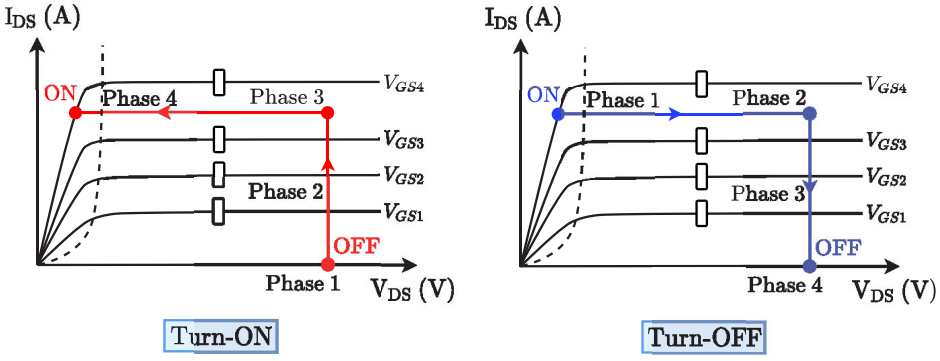


Figure 3.2: Ideal switching trajectories. (a) Turning-ON, (b) turning-OFF adapted from [5].

The output characteristic of the device need to be accurately measured without any self-heating effect. The linear mode for I-V graph is represented by the region where drain source voltage is below the limit $V_{gs} - V_{th}$. This region is important for a good estimation of the ON-losses. If the drain source voltage is above $V_{gs} - V_{th}$, the curve represents the saturation region, which is important for a good estimation of the switching losses [83–86]. The capacitance characteristic defines the energy amount involved in the device during a switching, which is a fundamental element the model validation.

The GaN devices were mounted on a PCB board to fit the B1505A slot. The tests were also performed at high temperature, close to the maximal junction temperature (given in datasheet) of each power device. For this, a hot plate was used and directly connected to the device package. For GaN Systems devices, the initial tests at ambient temperature were performed with the G1 sample during the first thesis year. Later, some tests with the hot plate were undertaken to tune the setup for high temperature tests. It is possible that these tests could have degraded the samples. However, the G2 sample presented a behavior more similar to the datasheet and simulation results, as shown in Figure 3.3. Thus, a good trending pattern is verified even at a high

temperature. In Section A.1, the output characteristics were overlaid for both samples to verify the equivalent behavior.

The Panasonic device used for both temperature tests was the same: P2 sample. By analyzing the results presented in Figure 3.4, it is possible to verify optimistic datasheet results to compare simulation and experimental results. The threshold voltage was adjusted in the SPICE model from Panasonic, allowing for a better correlation between simulation and measurements. A possible explanation could be related to a high-performance sample used by manufacturers during their tests. The high temperature tests were performed more carefully, using an air-flow furnace to avoid the device heating.

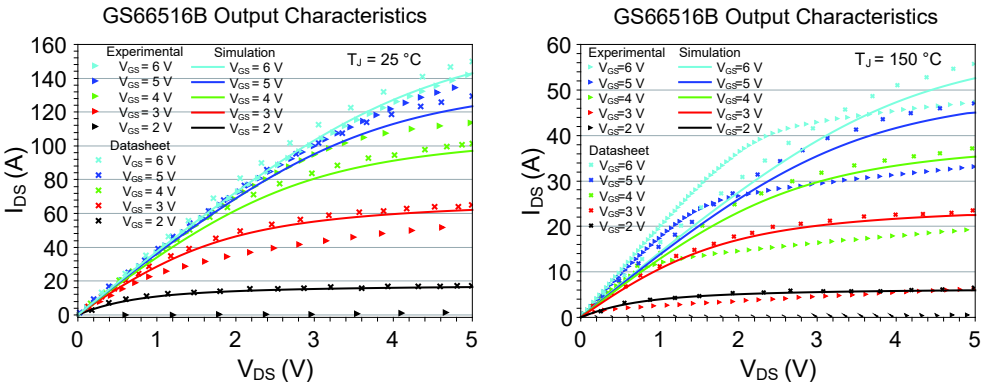
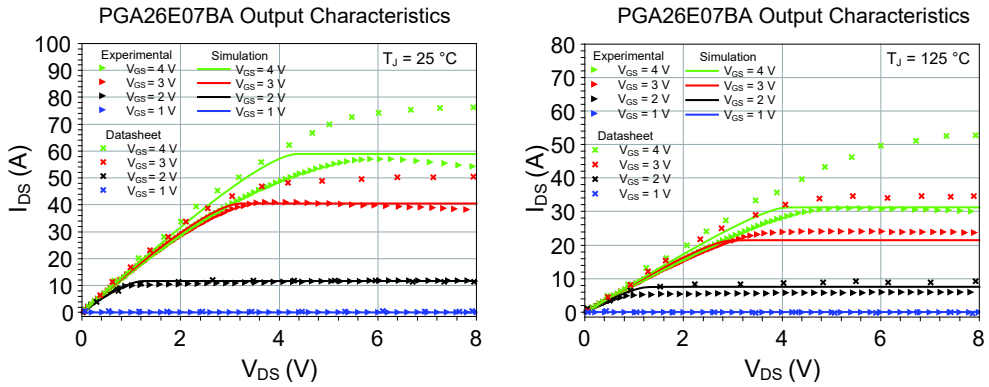


Figure 3.3: GS66516B (GaN Systems): (a) Output characteristics - sample G1 - at ambient temperature ($T_J = 25\,°C$) (measurement date: 09/09/2019) and after heating - sample G2 - ($T_J = 150\,°C$) (measurement date: 20/07/2021).

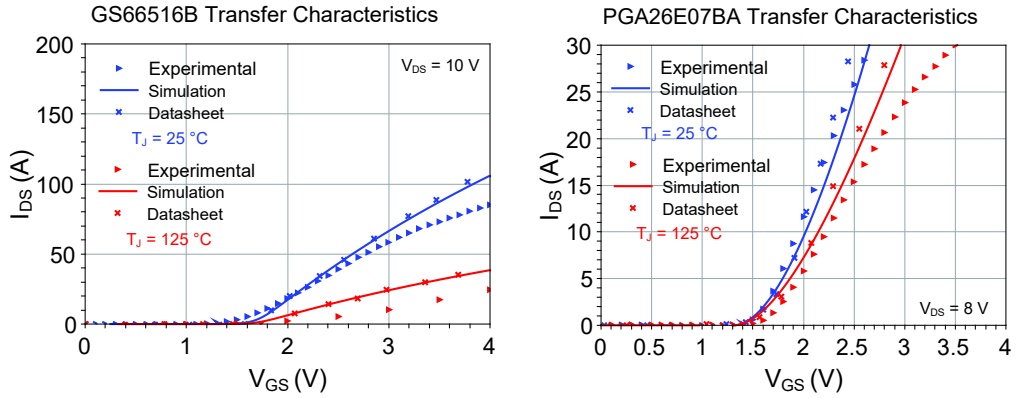
The transfer characteristics were also plotted for both GaN devices (GaN Systems and Panasonic), as can be seen in Figure 3.5. At high temperatures, the threshold voltage tends to increase according to the GaN technology datasheet, as well as the simulation and experimental results. However, there were some differences between the experimental and simulation results. The tests performed at different dates contributed to this difference.

The temperature is a key factor that influences the power device behavior and the total losses. The ON-resistance temperature dependency for both GaN devices is presented in Figure 3.6. A monotonously increasing trend can be seen from the ambient temperature up to 150 °C. Each measurement was



(a) (b)

Figure 3.4: PGA26E07BA (Panasonic): (a) Output characteristics at ambient temperature ($T_J = 25\,°C$) (measurement date: 09/09/2019) and after heating ($T_J = 125\,°C$) (measurement date: 20/07/2021). Sample P2 was used for both tests.



(a) (b)

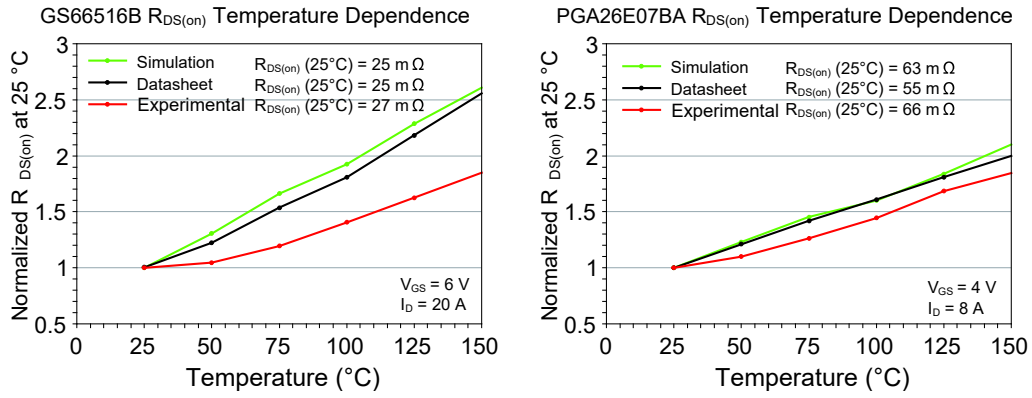
Figure 3.5: (a) Transfer characteristics of GS66516B (GaN Systems) and (b) for PGA26E07BA (Panasonic).

performed at about 30% of the nominal current and at the specified datasheet gate source voltage.

According to Figure 3.6(a), the GaN Systems device presents a ON-resistance variation that is about 2.5 times the ambient temperature for simulation and datasheet values. As previously mentioned, the experimental data were extracted from a perhaps degraded component and it is subject to inaccuracies. For the Panasonic device, an ON-resistance variation of about 2 times the am-

bient temperature was verified based on the datasheet, as well as simulation and experimental results, as seen in Figure 3.6(b). This indicates a better performance at high temperatures as compared to the GaN Systems device.

ON-resistance temperature dependence is important in estimating the power device behavior for conduction loss estimation in a DC-DC converter.



(a) (b)

Figure 3.6: (a) ON-resistance temperature dependence of GS66516B (GaN Systems) and (b) for PGA26E07BA (Panasonic). The resistance values are normalized as a function of T_J.

The static characterization was also performed for the SiC devices (Rohm and CREE), listed in Table 3.1. A good correlation was achieved between datasheet, simulation and experimental results, as can be seen in Figure 3.7 and Figure 3.8. However, the current state of development of SiC technology offers simulation models closer to experimental results. By analysis of the output characteristics for SiC devices, a convergent saturation state between simulation and experimental data can be seen, what indicates a good switching loss estimation.

However, the high temperature tests for the CREE device could not be performed due to a technical problem with the air-flow furnace connected to the Curve Tracer (B1505) and a lack of time. The small variation for the output characteristics of SiC devices at high temperature, when compared to GaN devices, showed a better performance for high current applications. The transfer characteristics of both SiC devices are presented in Figure 3.9. Unlike the GaN devices, the threshold voltage decreases with the increase in temperature. This

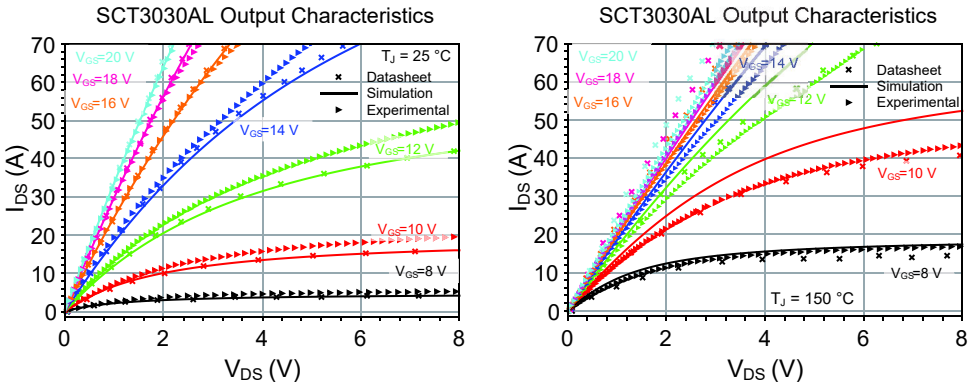


Figure 3.7: SCT3030AL (Rohm): (a) Output characteristics - sample S4 - at ambient temperature ($T_J = 25\,°C$) (measurement date: 09/09/2019) and after heating - sample S3 - ($T_J = 150\,°C$) (measurement date: 20/07/2021).

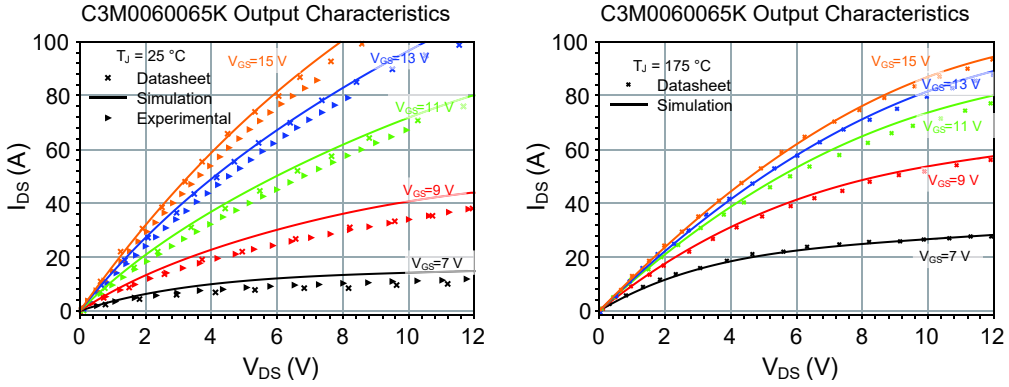
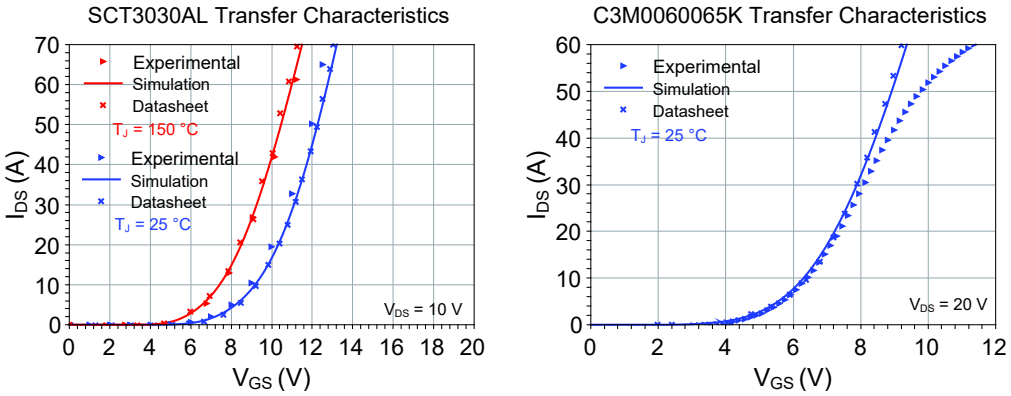


Figure 3.8: C3M0060065K (CREE): (a) Output characteristics - sample W1 - at ambient temperature ($T_J = 25\,°C$) (measurement date: 09/09/2019). Due to technical problems, the tests at high temperature could not be performed.

can generate a more sensitive turning-ON for the device when operating at high temperature. However, a good correlation between datasheet, simulation, and experimental results was verified for the SiC devices, at ambient and high temperatures.

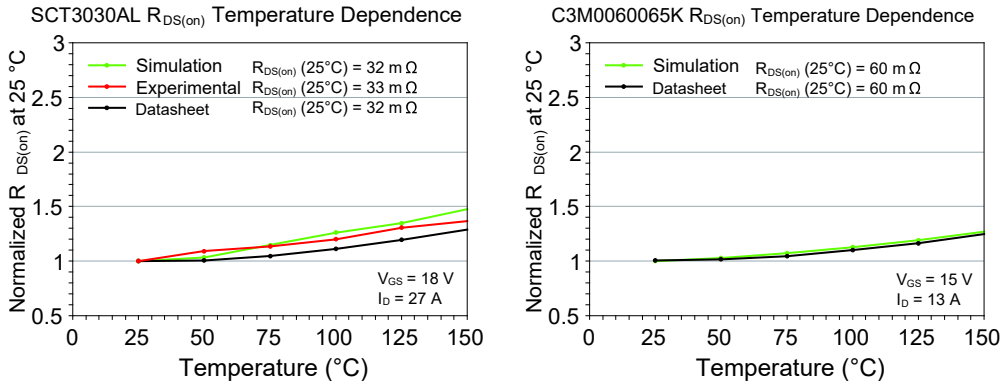
According to Figure 3.10(a), the SiC Rohm device presents an ON-resistance variation of about 1.4 times the ambient temperature for the datasheet, simulation and experimental values. For the SiC CREE device, a ON-resistance



(a) (b)

Figure 3.9: (a) Transfer characteristics for SCT3030AL (Rohm) and (b) for C3M0060065K (CREE).

variation about 1.3 times the ambient temperature is verified for datasheet and simulation results, as shown in Figure 3.10(b). This indicates higher stability for temperature variation as compared to the GaN devices. In other words, the conduction losses increase less with the temperature than for GaN technology.



(a) (b)

Figure 3.10: (a) ON-resistance temperature dependence for SCT3030AL (Rohm) and (b) for C3M0060065K (CREE). The resistance values are normalized as a function of T_J.

3.1.1 Protocol Test for GaN devices

During measurements, it was noticed that the output characteristic of the GaN component was modified if a drain leakage current characteristic was measured just before the output characteristics [87]. The leakage current test consists of a gate-source voltage applied to hold the switch to remain turned-OFF (0 V, in this study). Simultaneously, a drain-source voltage is applied to slowly increase its value (up to 400 V). For example, Figure 3.11 shows that the curve for the gate voltage equal to 2 V was significantly modified. This effect is due to the trapping/detrapping (current collapse) associated with the GaN components [24, 88, 89].

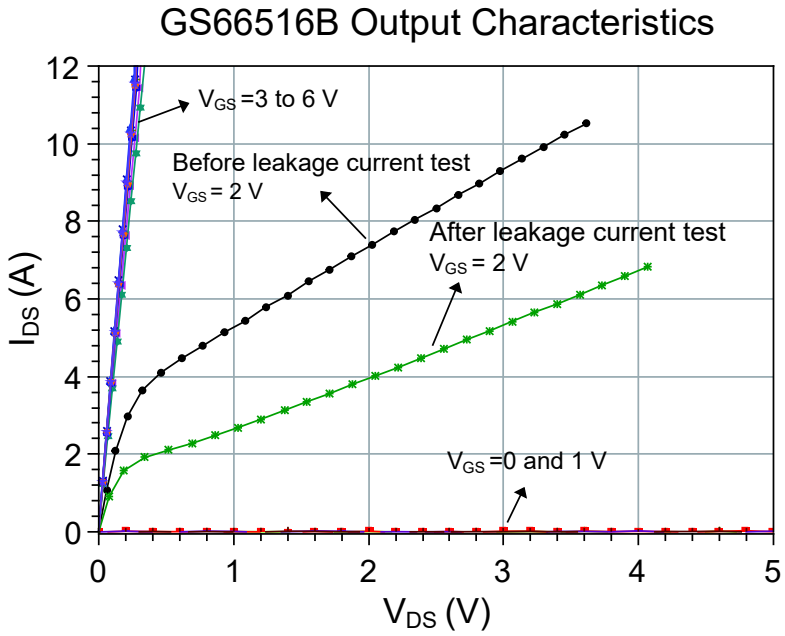


Figure 3.11: Output Characteristics for GS66516B GaN Systems.

This is an important point that will be considered for the measurements. To avoid this phenomenon, our protocol includes a measurement of the transfer characteristics from −8 V to 4 V (gate source voltage) just before performing the output characteristic test. In this manner, the fact of applying a negative bias voltage attenuates the trapping effect on AlGaN layer. The drain source ON-resistance is measured from Figure 3.11. Hence, at the ambient temperature and before the drain leakage test, it was found 22.3 mΩ. Thereafter, the ON-resistance increased up to 23.5 mΩ.

3.2 Capacitance Characterization

The capacitance charging evolution with the voltage defines the dynamic characteristics of the power device [85]. The junction capacitance values (C_{DS}, C_{GD} and C_{GS}) influence the current and voltage waveforms, and they are rather important in obtaining good modeling of the switching transient, as previously discussed in Section 2.3. The simplified setups for each capacitance measurement are presented in Figure 3.12. The measurements are performed with a Curve Tracer Keysight B1505A.

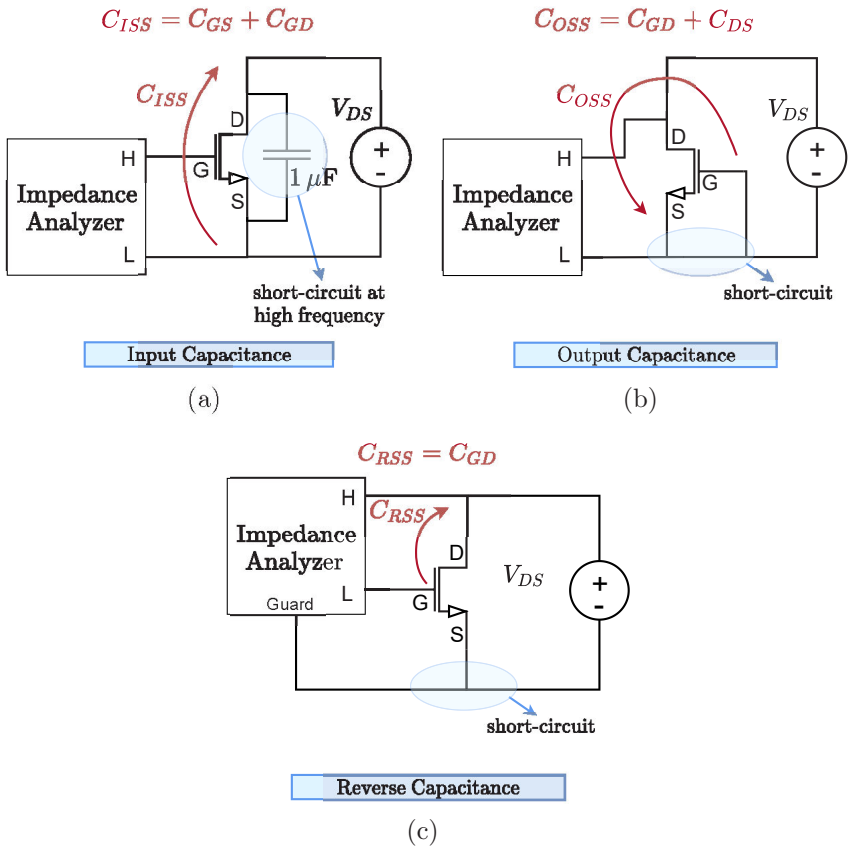
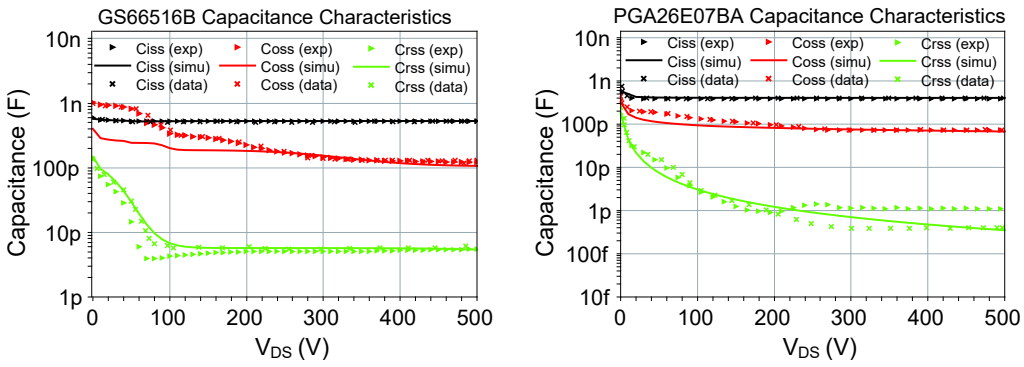


Figure 3.12: Test setups for characterization of junction capacitance, including (a) input capacitance (C_{ISS}), (b) output capacitance (C_{OSS}), and (c) reverse capacitance (C_{RSS}) adapted from [5].

The capacitance values are expressed with the lumped values (C_{ISS}, C_{OSS} and C_{RSS}) for ease of measurements. Moreover, applying a voltage directly on the switch terminals may generate error sources and even false turn-ON events. In Figure 3.12(a), it is possible to verify a large capacitance (1 μF)

used to cause a short-circuit for AC signals (high frequency signals) between drain-source terminals. In Figure 3.12(b), the Impedance Analyzer is connected to the drain-source terminals of the switch, and the gate-source is short-circuited. The reverse capacitance is obtained by connecting the Guard terminal of the Impedance Analyzer to the source terminal of the device. The AC current that flows into this terminal is neglected by the equipment. As seen in Figure 3.12(c), only the gate drain capacitance is measured, given that all currents that flows into the Guard terminal are ignored. The circuits for simulation performed in LTspice were built based on these schematics, and a ground is used to simulate the Guard terminal.

The input capacitance modeling must be precisely performed, since it determines the switching speed, consequently influencing the switching losses. The Miller capacitance (C_{RSS}) is the main component for cross conduction effect, as demonstrated in the dynamic characterization tests [5]. Moreover, a good correlation was found for the comparison between the datasheet, simulation, and experimental results for the GaN devices, as shown in Figure 3.13. This implies that, for switching loss estimation, the SPICE models present a behavior close to that of the device used for the tests. The capacitance characteristics for SiC devices is also presented in Figure 3.14. As previously mentioned, due to the development state of the SiC technology, it is reasonable that their manufacturers present more reliable SPICE models and a better match between the simulation and experimental results.



(a) (b)

Figure 3.13: (a) Capacitance characteristics of GS66516B (GaN Systems) and (b) for PGA26E07BA (Panasonic).

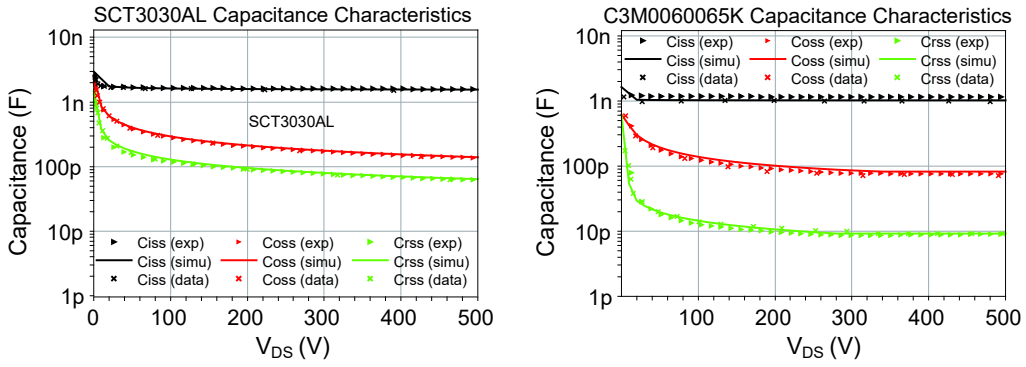


Figure 3.14: (a) Capacitance characteristics of SCT3030AL (Rohm) and (b) for C3M0060065K (CREE).

The gate capacitance component is not strongly affected by the variation with drain source voltage, thus causing a flat response of the input capacitance as verified for all power devices [83]. Moreover, C_{ISS} modeling is important to understand the dynamic switching waveform (thus, loss estimation) and for gate driver selection. The output characteristic is highly nonlinear with respect to drain source voltage, and it is responsible for a part of the losses during the switching transient, as previously discussed. The reverse capacitance is directly related to the cross-conduction effect between the two switches of the same commutation cell and, thus, its modeling is rather important to improve the accuracy of simulation models.

3.3 Conclusion and Perspectives

The comparison between experimental and simulation results presented a good correlation. The static and dynamic device characterization allows for the validation of the SPICE models to be used in the switching mode. Thus, with some adjustments of the threshold voltage, switching loss estimation can be performed by using the manufacturers' available models.

The development level of SPICE models for SiC devices is evident, mainly due to the fact of these components have been commercially available for some time. However, the GaN devices are still subjected to large variations between simulation models and experimental tests.

CHAPTER 4

Switching Behavior Characterization

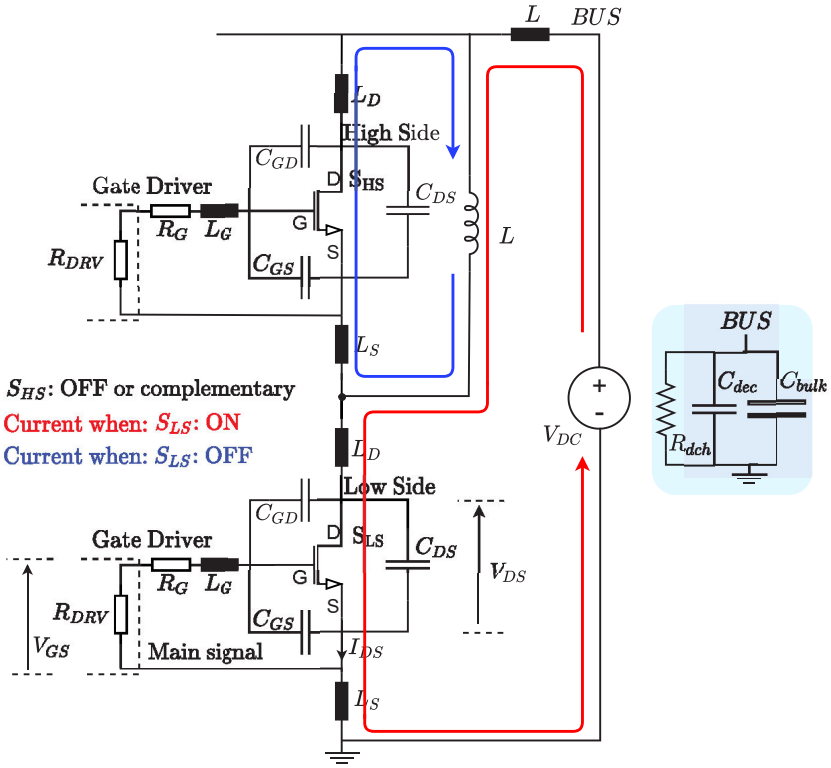
4.1 Instrumented PCB for GaN Devices

The need to increase power electronic performances has motivated the development of new research on semiconductor devices, such as GaN HEMT switches. They are promising components for fast switching, and high efficiency, thus high-power density module design [22]. To study these new devices, an instrumented PCB was developed including the measurement points needed for this purpose. The parasitic elements of the PCB layout extracted by ANSYS Q3D and the models of the measurement instruments were also included in the simulation model. A one-leg GaN-based power module was also analyzed regarding to oscillations at the middle point voltage, and the impact of the parasitic elements modeling was verified by comparing simulation and experimental results.

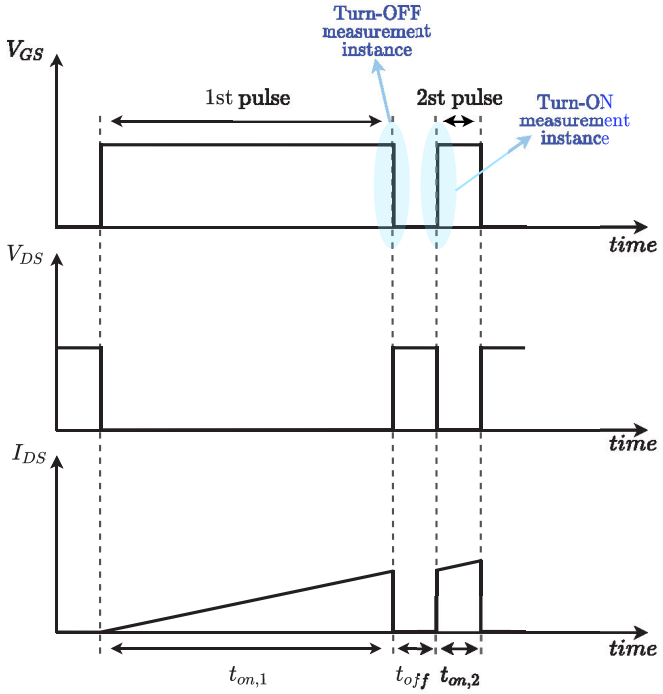
4.1.1 Switching Characterization

The switching characteristics of a power semiconductor illustrate its performance during switching transient. Some parameters are important to highlight when it comes to evaluating a power device in dynamic operation including switching energy, dynamic spikes, parasitic ringing, and voltage/current slope.

The DPT (Double Pulse Test) is widely used to analyze the switching behavior of a power device, due to its simple circuit implementation [42, 90–92]. The main focus of the DPT is to characterize the dynamic performance of the power switch, without the influence of self-heating, thus, the applied pulses should be short. In Figure 4.1, the basic electrical schematic and typical waveforms for DPT can be seen.



(a)



(b)

Figure 4.1: DPT: (a) Electrical schematic of DPT characterization and (b) typical waveforms adapted from [42, 91].

Two pulses are sent to the lower switch (S_{LS}) that is connected in series with an inductive load (L). During the first pulse ($t_{on,1}$), a positive V_{GS} is applied to S_{LS}, thus the DC voltage is on the load inductor. The current starts to increase linearly, considering the inductor is at the linear region, and remains at a constant value, due to the high time constant. The pulse ends when the suitable current value is reached (I_{DS}). During t_{off}, the inductor current flows through the high side switch (S_{HS}), with reverse conduction (diode-like behavior). During the second pulse ($t_{on,2}$), the rising edge serves to evaluate the turn-ON switching behavior of S_{LS}. Afterwards, the second pulse is ended, and the current goes down to zero due to the loss dissipation of the load inductor [42, 91]. At the end, the switching behavior under the same voltage/current are obtained.

An experimental implementation of DPT can be seen in Figure 4.2. The DPT Board represents the main part of the system, compound by components such as bulk/decoupling capacitors, gate drives, power switches, and charge. Peripheral interfaces also integrate the DPT system such as a pulse generator to generate the signals required for controlling, power supplies, a computer for programming and data processing, and data reading equipments (measurement instruments and oscilloscope).

The current during the first pulse is provided by the load inductor (L). Its value should be large enough to limit the current variation during the switching transient. From the electrical circuit of Figure 4.1, and the fundamental inductor equation, prettyrefeq:dpt1 can be written to design the inductor, in such a manner so as to ensure a current nearly constant when the lower switch (S_{LS}) is OFF [93].

$$L \geq \frac{V_{DC}}{\Delta I_L} t_{SW} = \frac{V_{DC}}{k_{\Delta i} I_L} t_{SW} \tag{4.1}$$

where ΔI_L is the current variation on the inductor, t_{SW} is the switching time of the power device, $k_{\Delta i}$ is the current percentage during the switching transition, and V_{DC} and I_L refer to the DC bus voltage and current load.

Regarding Equation (4.1), the inductor design is undertaken by considering the maximum DC voltage applied and the minimum current through the DUT. Furthermore, the inductor value can not be too large, because this implies a

longer first pulse duration, which may cause a temperature rise during the DPT, mainly for devices with reduced physical dimensions.

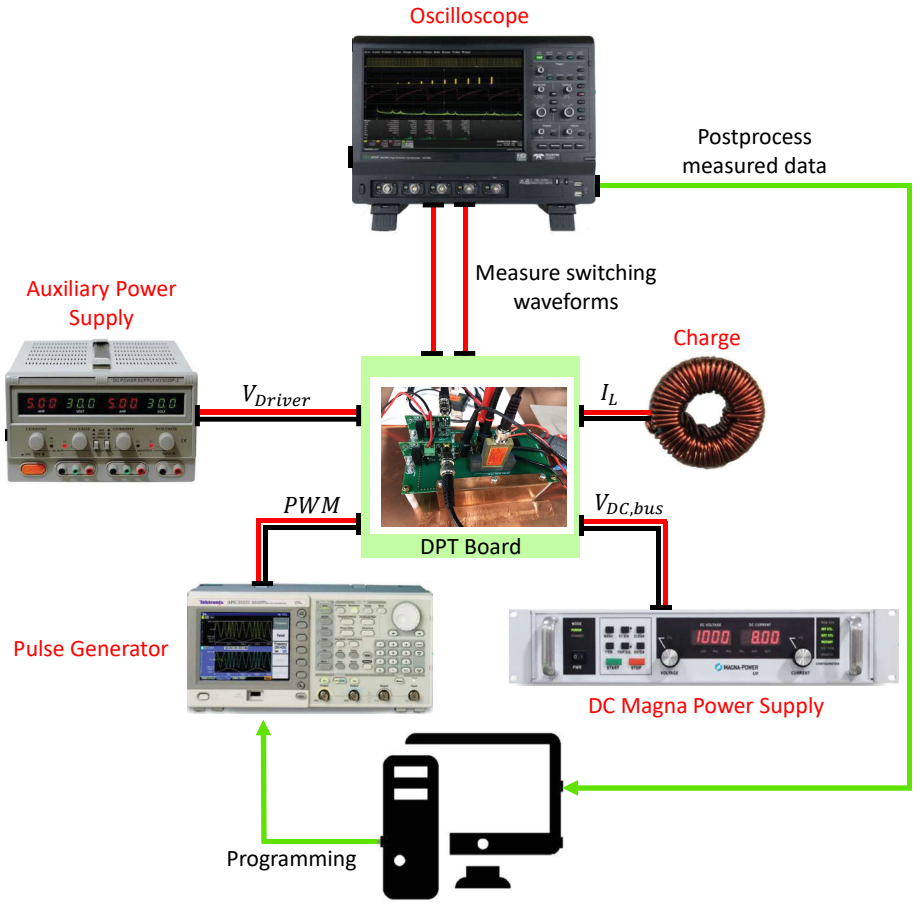


Figure 4.2: Physical implementation of DPT.

The DC bus voltage (V_{DC}) is supplied by a DC Magna Power Supply (XR1000V-8.0A). Current rating of this voltage source can be much lower than the maximum characterization current for the DUT, due to the use of a bulk capacitor which provide the required current. The bulk capacitance is designed to limit the voltage variation on bus (ΔV_{DC}) when the energy flows from the capacitor bank (electrical energy) to the load inductor (magnetic energy) during the first pulse. Considering a lossless energy transfer, Equation (4.2) can be derived based on the conservation of energy principle. Consequently, Equation (4.3) can be used to design the lower limit for bulk capacitor value [42, 93].

$$\frac{1}{2}C_{bulk}V_{DC}^2 - \frac{1}{2}C_{bulk}(V_{DC} - \Delta V_{DC})^2 = \frac{1}{2}LI_L^2 \tag{4.2}$$

$$C_{bulk} \geq \frac{LI_L^2}{(2V_{DC} - \Delta V_{DC})\,\Delta V_{DC}} = \frac{LI_L{}^2}{(2 - k_{\Delta v})\,k_{\Delta v} V_{DC}{}^2} \approx \frac{LI_L{}^2}{2k_{\Delta v} V_{DC}{}^2} \tag{4.3}$$

where ΔV_{DC} is the DC link voltage drop on the bulk capacitor, and $k_{\Delta v}$ is the voltage variation percentage. However, normally, film or electrolytic capacitors are used for the DC link due to their high available capacitance and high energy density. Further, the use of several parallel capacitors are advised to have a low stray inductance design [42].

Moreover, the decoupling capacitor (C_{dec}) is selected to provide transient current and attenuate overvoltage, due to the parasitic elements, during the switching transient. The overvoltage relies on the ratio between the decoupling capacitor and the switch output capacitance (C_{OSS}). When this relation becomes superior to 100, the overvoltage on bus bar decreases considerably, and thus Equation (4.4) can be used to design the decoupling capacitor.

$$C_{dec} \geq 100 C_{OSS} \tag{4.4}$$

Furthermore, the decoupling capacitors should have a lower Equivalent Series Inductance (ESL), thus ceramic capacitors are suitable for this application.

A discharge resistor is introduced on the DC bus to dissipate the remaining energy stored in the bulk capacitor. A trade-OFF between power loss dissipated by the discharge resistor, and the discharge time, as seen in the Equation (4.5) should be considered for its design.

$$P_{R_{dch}} = \frac{V_{DC(max)}^2}{R_{dch}} \text{ and } C_{buck} R_{dch} = T_{discharge} \tag{4.5}$$

where $V_{DC(max)}$ is the maximum DC voltage applied, and $T_{discharge}$ is the discharge time constant.

4.1.2 Instrumented PCB

Considering the high switching-speed of GaN device, the experimental test results are sensitive to the layout design of the PCB and parasitic management. In Figure 4.3, the design of the instrumented PCB can be seen. The power stage is separated from the gate driver implemented in two dedicated boards. The power loop inductance has a strong contribution to the power loop ringing

and overshoot voltage, causing reliability issues and EMI (Electromagnetic Interference) [42]. The tracks $+V_{DC}$ and $-V_{DC}$ are designed to have the maximum area, reducing coupling inductance effects. However, the width of the conduction track can not be arbitrarily increased because of the influence of parasitic capacitance formed with the ground plane [94]. Moreover, the decoupling capacitors are placed as close as possible to the power devices to minimize the power loop. The shunt used for current measurement is placed on the inverted sense. The negative terminal enables the source terminal of the low side switch to share the same potential with the earth ground. In this manner, when measuring the drain source voltage on the low side switch, the disturbances added by the shunt can be neglected, being read exactly the voltage on the switch package [42]. Further, the gate loop should be minimized as much as possible, due to the parasitic inductance presented in this loop that may generate overshoo at gate source terminals. For the instrumented PCB, a large distance between the driver PCBs and the power device gate is seen due to the added measurement instrument (current transformer).

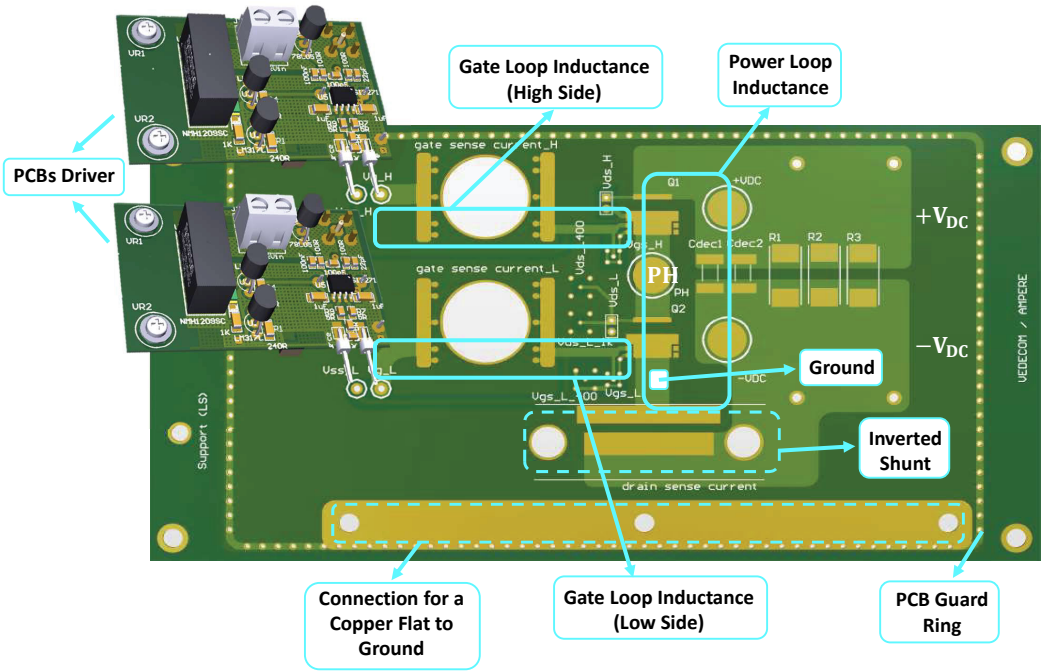


Figure 4.3: Instrumented PCB and design of gate drivers.

A large track is also designed to connect an external cooper flat with the bench ground plane. This helps in reducing the ground resistance for high

frequency currents, and also in creating uniform distribution of capacitance for the entire board. Moreover, a PCB guard ring is implemented in order to mitigate surface stray inductance and leakage currents. This technique allows conducting currents, that would flow to other components, towards a defined surface (ground plane, for instance), thus improving the signal integrity [91].

Further, the developed PCB is instrumented to measure voltages (drain-source and gate-source) and currents (gate and drain-source) on the low side switch, as shown in Figure 4.4. The command circuit is connected from another PCB, positioned at ninety degrees in order to obtain the lowest coupling effect between the power and drive circuits. Furthermore, a ground plane connected to the earth is used to minimize the mutual inductance values. In Table 4.1, the measurement instruments are described, and in Table 4.2, the main components of the evaluation board are shown.

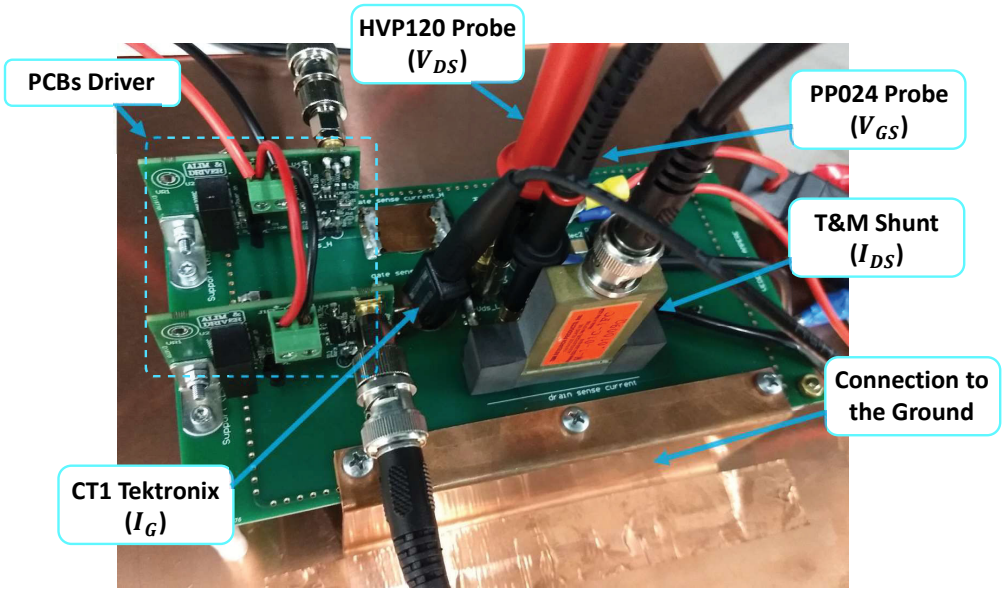


Figure 4.4: PCB developed for the DPT with the GaN components behind the voltage probes. Load inductor out of picture: 100 μH.

Table 4.1: List of measurement instruments used in this study.

Probe Reference	Manufacturer	Usage	Symbol
PP024	Lecroy	Gate Source Voltage	V_{GS}
HVP120	Lecroy	Drain Source Voltage	V_{DS}
W-1-01C-1FC	T&M Research	Drain Source Current	I_{DS}
CT1	Tektronix	Gate Current	I_G

In general, the prototype is performed under the conditions presented in the Table 4.3. Here, a negative gate source voltage is applied for the turn-OFF in order to attenuate false turn-ON events. The results are performed within the voltage range of (100 - 400) V, that offers a current range of (4.3 - 18.3) A, applied on a load inductor of 100 μH. In Figure 4.5, the physical implementation and all the components used for the tests are presented.

Table 4.2: List of main components.

Component	Function	Manufacturer	Description
GS66516B	Power Device	GaN Systems	650 V, 60 A, 25 mΩ
SI8271	Gate Driver	Silicon Labs	5 V_{OUT}, 1.8/4 A
MKP1848C71060JY5	Bulk Capacitor	Vishay	100 μF $\pm$ 5%, 600V_{DC}, Film
2220Y6300105KXTWS2	Decoupling Capacitor	Knowles Syfer	1 μF $\pm$ 10%, 630V_{DC}, Ceramic
3550100KJT	Discharge Resistance	TE Connectivity	100 kΩ $\pm$ 5%, 5 W, ThickFilm

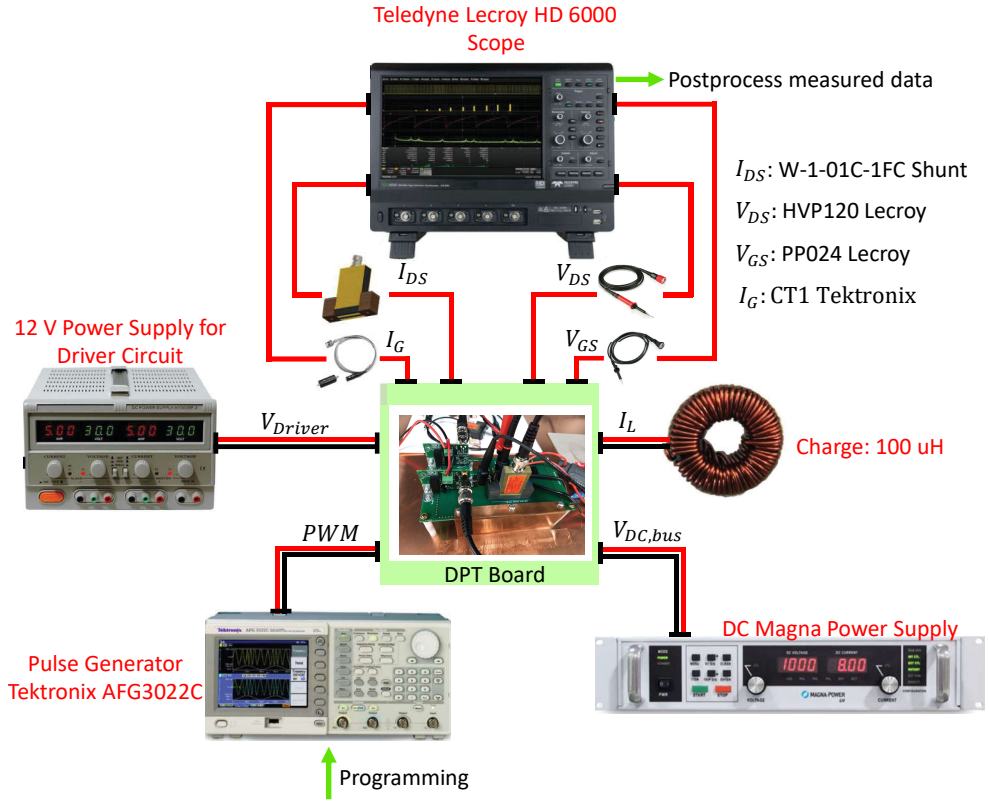
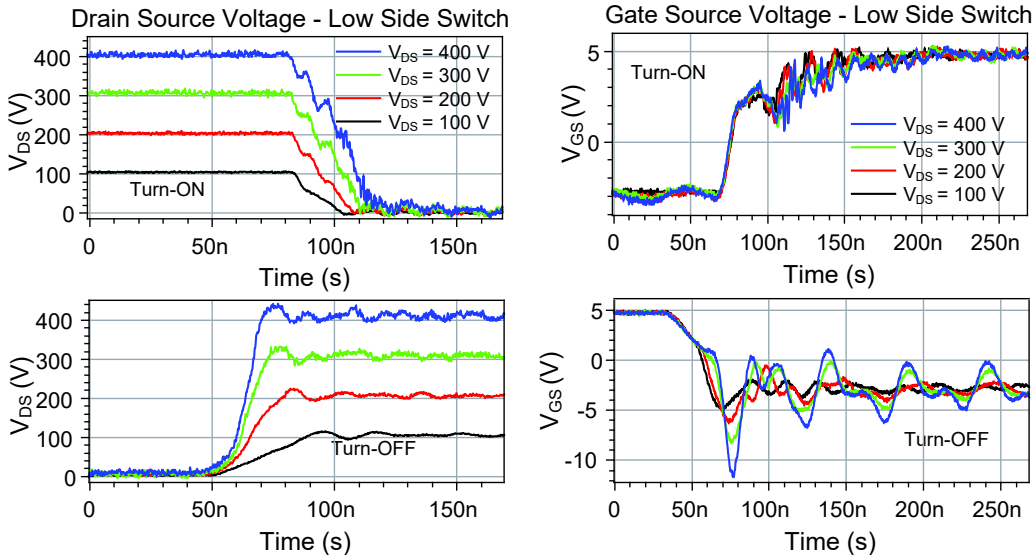


Figure 4.5: Physical implementation of DPT.

In

Table 4.3: Test conditions.

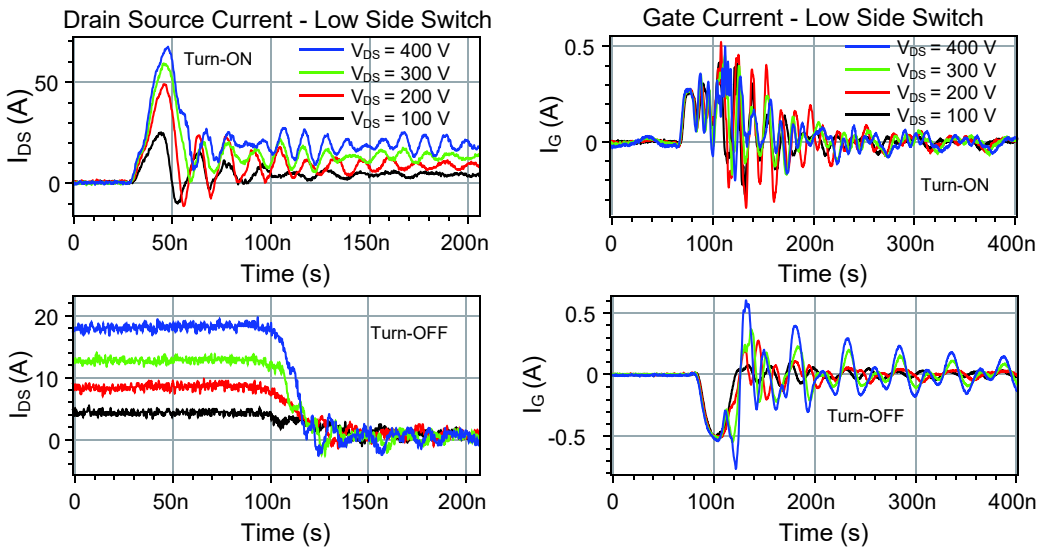
Parameters	Value	Unit	Description
V_{Driver}	12	V	Auxiliary Power Supply
V_{GS}	$5/-3$	V	ON/OFF Gate Source Voltage
R_{ON}/R_{OFF}	10/1	Ω	ON/OFF Resistors
$T_{on,1}/T_{on,2}$	10/2.5	μs	First/Second Pulses
T_{off}	2.5	μs	OFF time



(a) (b)

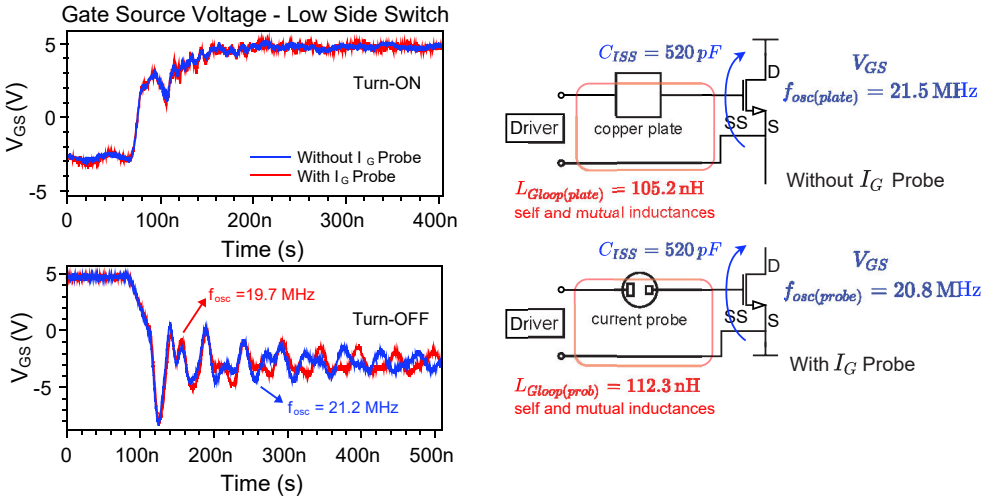
Figure 4.6: Experimental results obtained from instrumented PCB. Waveforms of the low side switch: (a) V_{DS} and (b) V_{GS}.

In Figure 4.8(a), the effect on V_{GS} due to the measuring of the gate current can be seen. Some disturbances are detected, however the waveform remains nearly the same. The main oscillation frequencies obtained by the FFT (Fast Fourier Transform) applied on the measured V_{GS} indicates a resonance effect between the input capacitance of the switches and the gate loop inductance. In Figure 4.8(b), calculus is used to confirm this proposition. Therefore, by adding a probe current for I_G measurement, the impact on signals is limited.



(a) (b)

Figure 4.7: Experimental results obtained from instrumented PCB. Waveforms of the low side switch: (a) I_{DS} and (b) I_G.



(a) (b)

Figure 4.8: Experimental results: (a) Analysis of gate source voltage V_{GS} considering the impact of using a current probe for I_G measurement. (b) Main oscillation frequency from V_{GS} for both cases: without and with I_G probe. Test condition: 300 V and 12.6 A.

4.1.3 Analysis of Parasitic Elements

The analysis of parasitic elements is important to ensure an accurate switching loss estimation. This analysis is realized by considering three main elements on the SPICE simulation: the GaN component SPICE model (GS66516), measurement instrument models, and parasitic elements from the 3D wiring model. In Figure 4.9, the circuit for the DPT and its measurement points are presented. A copper plate is used as the track path when only the gate current on the low side switch is measured. Several critical parasitic parameters could be identified and investigated in terms of their individual effect through the GaN device switching test. Moreover, to better understand the parasitic element impact on drain source current/voltage waveforms, a parametric simulation is performed. In this study, the two main loops of the PCB is adopted to analyze the electrical behavior of the power device: the effect of the power loop (L_{Ploop}) and gate loop inductance (L_{Gloop}). For this approach, the simulation does not consider the parasitic inductance added by the shunt. In Figure 4.10 and Figure 4.11, the results of the power/gate loop inductance variation can be seen during the turn-ON and turn-OFF stages, respectively.

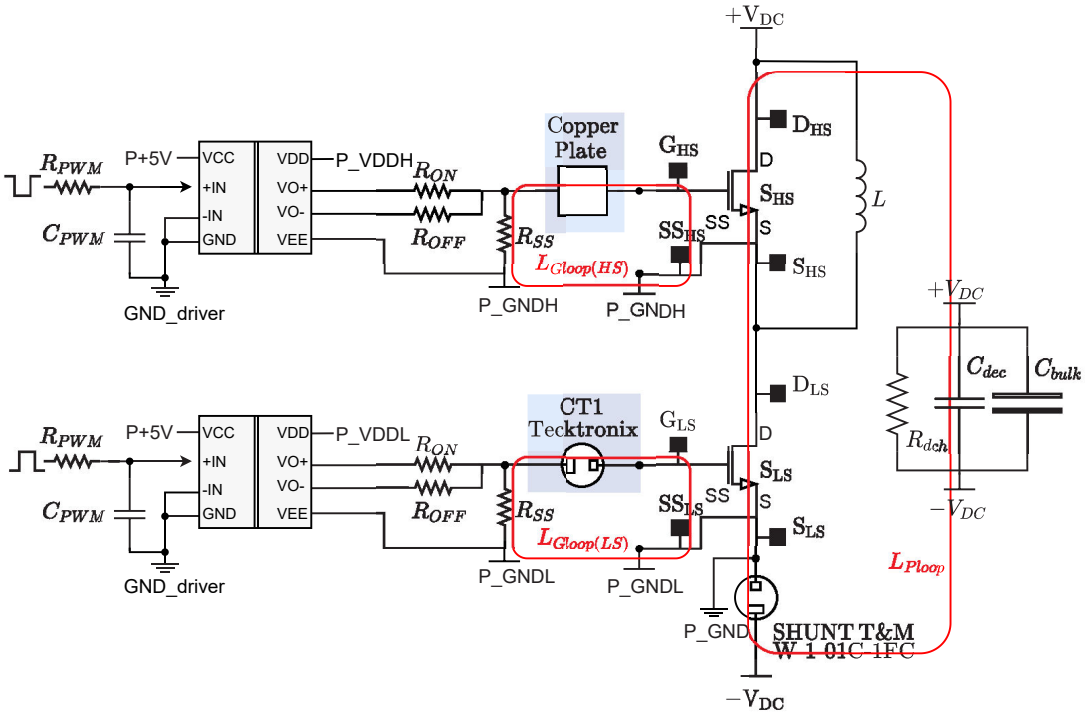
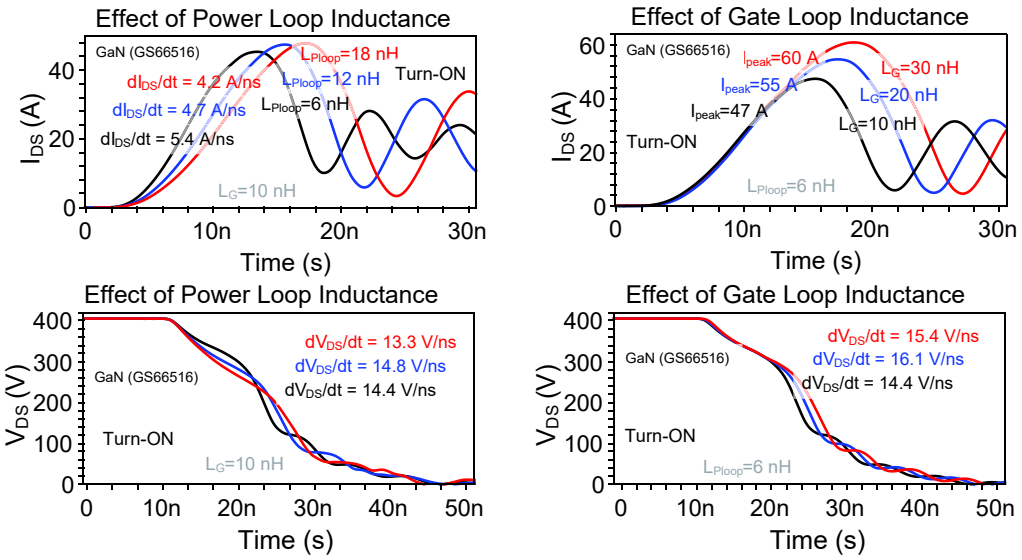
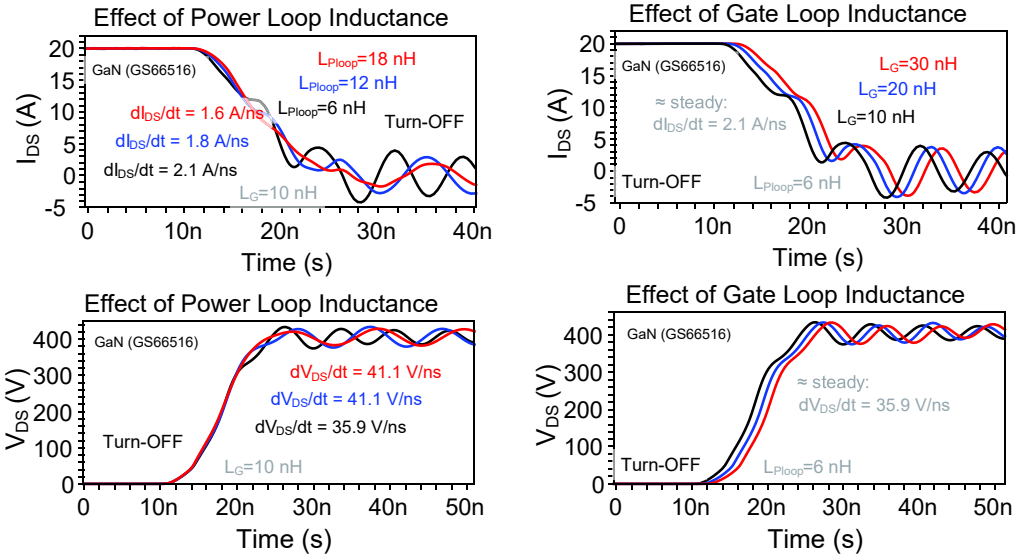


Figure 4.9: Schematic showing all measurement points used in the tests, as well as the two main-loop inductance values of the instrumented PCB.



(a) (b)

Figure 4.10: During turn-ON: (a) Effect of power loop inductance on current/voltage waveforms on low side switch (S_{LS}). (b) The same analysis for the gate loop inductance variation. Simulation parameters: $V_{BUS} = 400\,V$, $I_L = 20\,A$, $V_{GS} = +5/-3\,V$, $R_{ON;OFF} = 10;0\,\Omega$.



(a) (b)

Figure 4.11: During turn-OFF: (a) Effect of power loop inductance on current/voltage waveforms on low side switch (S_{LS}). (b) The same analysis for the gate loop inductance variation. Simulation parameters: $V_{BUS} = 400\,V$, $I_L = 20\,A$, $V_{GS} = +5/-3\,V$, $R_{ON;OFF} = 10;0\,\Omega$.

The turn-ON transient is more sensitive than the turn-OFF transient to changes in power/gate loop inductance. Therefore, the ON transient is used as a reference for comparison with the values obtained from the measurements. The simulation analysis allows observing that the current slope should be synchronized with the experimental test by means of power loop inductance adjustment. Afterwards, by considering the current peak reference, the gate loop inductance could be adjusted in order to match the experimental results.

A LC circuit is formed by the resonance between the power loop inductance and output capacitance of the power device, by causing parasitic ringing in current/voltage waveforms, as shown in Figure 4.10(a). Furthermore, the switching current speed slows down with the increase of power loop inductance. The overvoltage on both switches (lower and upper) is directly associated with the network formed by the power loop inductance and the output capacitor of the device in the turning-OFF stage. Meanwhile, the gate loop inductance has an important influence during the ON transient of the low side switch (S_{LS}). During this stage, the gate inductance on the complementary switch (S_{HS}) accentuates the cross-conduction effect on this switch, by causing a false turn-ON, which explains the transient current rise seen in Figure 4.10(b). During the OFF transient (S_{LS}), a transmission line is constituted by the gate loop inductance and the input capacitor of the power device, thus as the gate inductance increases, a delay is added on current/voltage waveforms, as seen in Figure 4.11(b).

The characterization of electrical parasitic of interconnects, busbars, and cables is commonly performed using a tool called ANSYS Q3D Extractor. A 3D lumped matrix RLC can be extracted in order to realize a simulation along with the global electrical schematic of the circuit board or power module [95]. A good parasitic performance prediction aims to maximize the power converter efficiency, and also to understand some oscillations and disturbances associated with the switching process. The solver technology used by ANSYS Q3D is based on the Finite Element Method (FEM) for meshing and integral equation solvers, by implementing a surface mesh to calculate the high frequency behavior of conductive structures [96]. This software enables the extraction of frequency-dependency partial inductance (PEEC) [97], resistance, and capacitive coupling between different conductors. In Figure 4.12, a flowchart is

presented describing the parasitic simulation process step by step. Initially, the 3D model is designed on ANSYS SpaceClaim, a CAD (Computer Aided-Design) tool for 3D modeling, or the layout is imported from an electronic design software such as Altium Design. In ANSYS Q3D, some considerations should be defined to ensure an accurate simulation is performed: sink/source positions, what it defines the current sense in the track, the NETs, electrical regions with the same potential defined in the ANSYS Q3D environment, and a proper mesh definition, all of which lead to an accurate simulation of the 3D geometry [96].

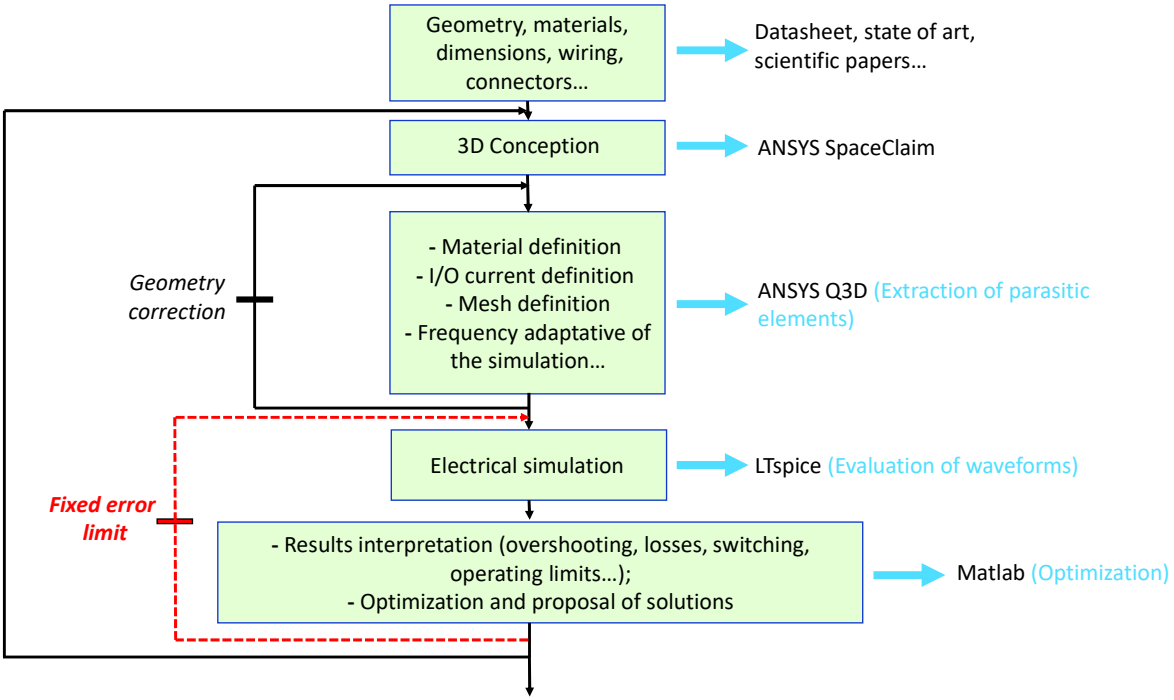
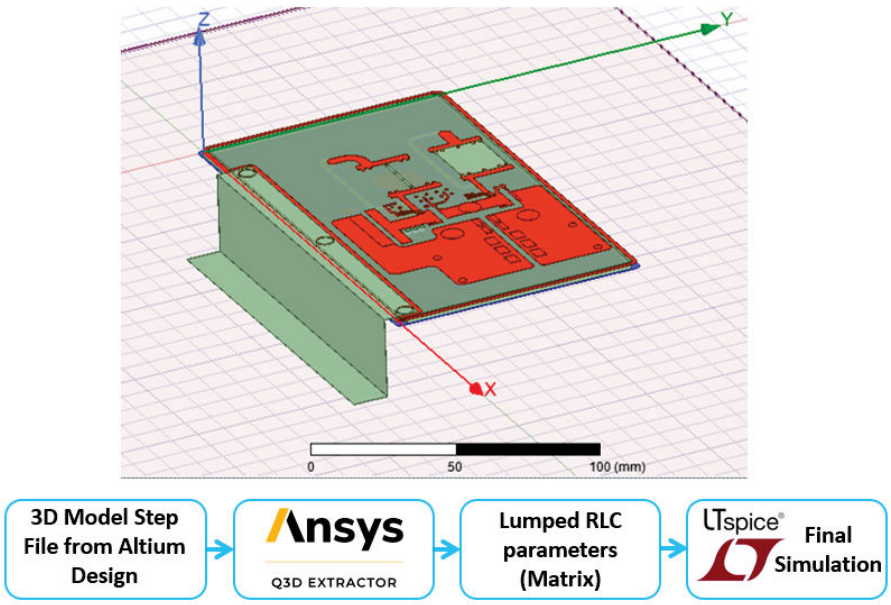


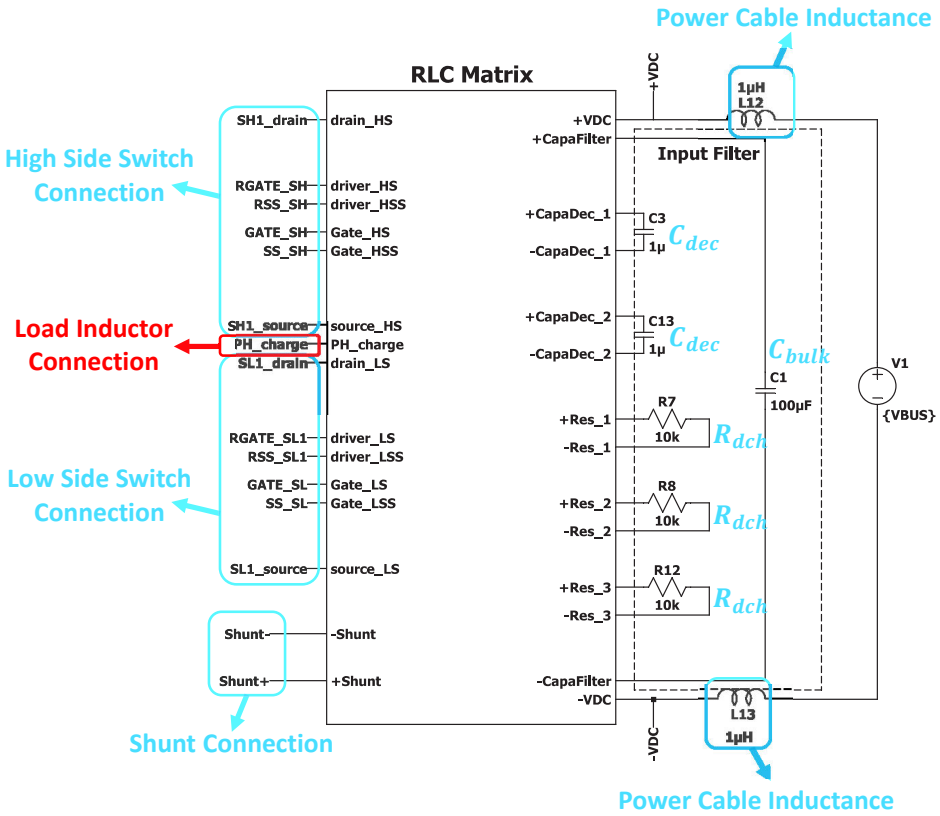
Figure 4.12: Flowchart for the extraction of parasitic elements from the circuit board adapted from [95].

The 3D model, seen in Figure 4.13(a), is imported from Altium Design and simulated using ANSYS Q3D to extract the RLC parasitic matrix, seen in Figure 4.13(b). Some issues regarding surface intersection and high difficulty associated with mesh operation could manifest at the moment of parasitic extraction. To bypass these issues, the connection between the top and bottom layers is undertaken using a solid shape instead of traditional vias, electrical connection between different layers in a physical electronic circuit. This procedure makes the mesh process solution easier. Also, for design settings, the

option material override is selected. This option allows some intersections to be solved automatically in the mesh [95].



(a)

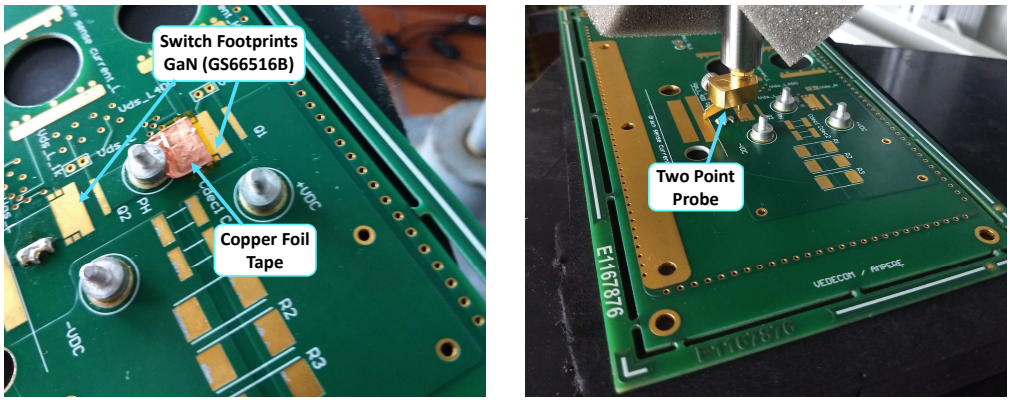


(b)

Figure 4.13: (a) Instrumented PCB simulation performed on ANSYS Q3D and (b) Lumped RLC matrix simulated on LTSpice.

The matrix presented in Figure 4.13(b) is added to the global electrical schematic, seen in Figure 4.9), built on LTSpice. This matrix is generated at an adaptive frequency of 100 MHz, using the definition from ANSYS for the main frequency analysis, which is enough to verify disturbance effects on the switching transient of GaN devices [42]. Two inductance values of 1 μH are used to represent the power cable inductance, and the passive components (resistors and capacitors) are also added beside the power source (VBUS).

Next, the power loop parasitic elements are extracted from the instrumented PCB shown in Figure 4.3. Further, the E4990A Impedance Analyzer is also used to measure these parasite inductance values in order to validate the parasitic inductance elements numerically extracted by ANSYS Q3D. In Figure 4.14, the test bench is shown with the instrumented PCB, without welded components.



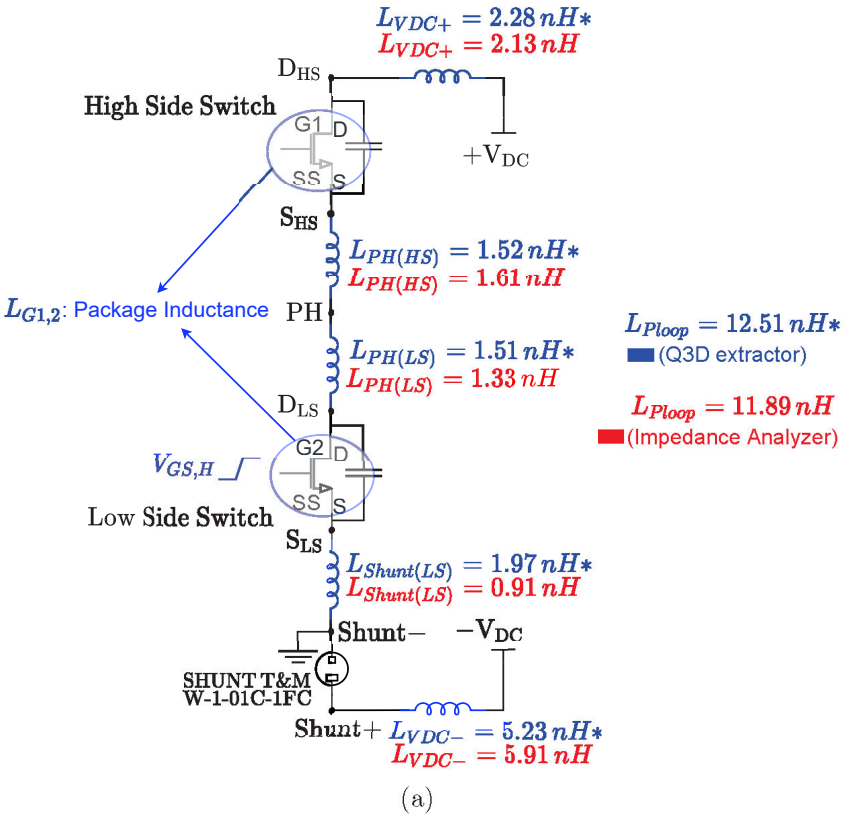
(a) (b)

Figure 4.14: Test bench for parasite inductance measurement with the E4990A Impedance Analyzer. (a) A cooper foil is used to facilitate the contact with the probe, (b) The inductance measurement between the shunt and source of the low side switch.

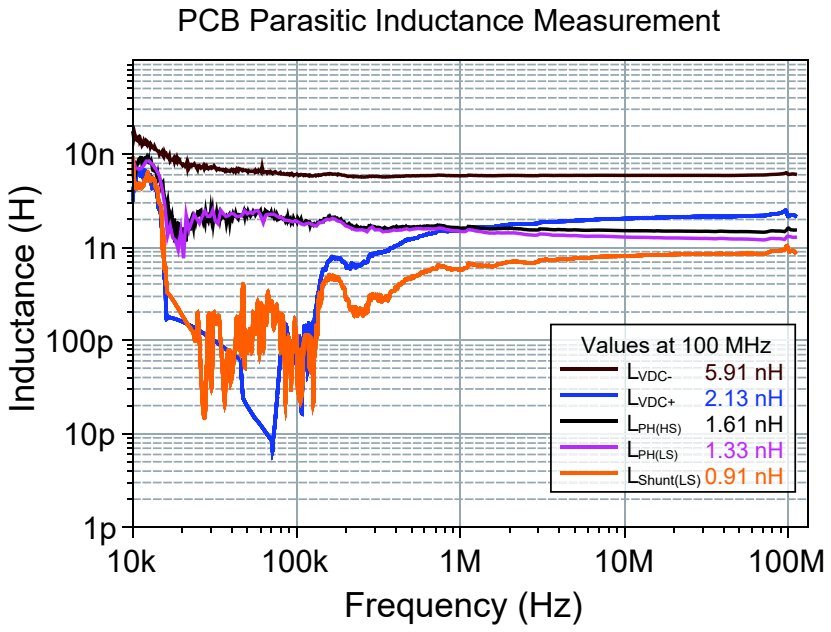
However, during the simulation performed on ANSYS Q3D, some issues were faced. More specifically, numerical problems, which generate a too large simulation time, associated with complex regions for mesh operation were detected. Further, a ground (GND) region is also an important element to define the current path through the 3D model. As the instrumented PCB has a specific ground at the low side switch source, the GND was defined as a common

NET, instead of using the standard GND definition, by defining a SOURCE and SINK for the current path, the definitions found in ANSYS Q3D to specify the input/output current by a conductor. Moreover, while the parasitic element solution is suitable for a specified bandwidth, the ANSYS Q3D is only able to export a simple frequency. Thus, the frequency of 100 MHz is defined based on the switching speed of the GaN devices. Thus, as the ANSYS Q3D is not a multilayer software, a geometry as simple as possible should be used for simulation.

The comparison between the simulation and experimental results can be seen in Figure 4.15. The results found through the experimental test shows a good correlation with the inductance values extracted by the Q3D Extractor, by showing a good estimation. In this case, the power loop does not consider the package inductance of power devices, and only the PCB tracks are simulated and measured.



(a)



(b)

Figure 4.15: (a) Comparison between the parasitic inductance extracted by ANSYS Q3D and experimental values. (b) Parasitic inductance measurement obtained by an E4990A Impedance Analyzer.

4.2 Modeling of Measurement Instruments

The use of an oscilloscope and some electrical measurement instruments are subject to the observability problems. When used as an external component to analyze a circuit, some disturbances can appear and cause experimental errors. The Heisenberg uncertainty principle was the first physical theory on this subject, that studied an electron position and momentum. At the engineering level, when doing a parallel analysis between the study of electrons and the voltage/current measurements, this principle is also valid and, in fact, any attempt to measure a certain variable can generate system disturbances.

In power electronics, voltage and current measurements are very important for waveform analysis or power losses estimation. The classical method DPT [98, 99] for characterizing power devices should also be implemented using accurate measurement instruments.

WBG exhibit better performance when compared to Si power devices due to their superior critical electric field. This allows for lower ON-resistance and parasitic capacitance values. However, these improvements bring new challenges when it comes to the loss measurements of the converters based on WBG devices [5–8].

However, the measurement instrument models are not provided by the manufacturers, thus, due to the inaccuracies associated with voltage/current probes, a reasonable electrical model must be used for the simulation of the full system. This allows for a better understanding of the added disturbances to the system and te estimation of the true behavior of a realistic converter, without added perturbations [42]. The measurement instruments used in this study are presented in Table 4.4. The main goal is to develop accurate models for the measurement instruments, by means of a simple procedure. In this manner, the comparison between simulation and experiment results can be performed for model validation and the estimation of switching losses.

Moreover, the electrical variables, gate source voltage (V_{GS}) and drain source voltage (V_{DS}), exhibit different magnitudes. For V_{GS}, a simple passive probe is used, and for V_{DS}, a high voltage passive probe should be chosen, once the overvoltages can reach values higher than 400 V [98]. The gate current (I_G)

Table 4.4: Measurement instruments used in this work.

Voltage/Current Probes	Manufacturer (Reference)	Measured Variable	Description
Passive Voltage Probe	Teledyne Lecroy (PP024)	Gate Source Voltage (V_{GS})	Bandwidth: 500 MHz Input Voltage: 400 V Attenuation: 10x
High Voltage Passive Probe	Teledyne Lecroy (HVP120)	Drain Source Voltage (V_{DS})	Bandwidth: 400 MHz Input Voltage 1000 V Attenuation 100x
AC Current Probe	Tektronix (CT1)	Gate Current (I_G)	Bandwidth: (25k-1G) Hz Max. Peak Pulse Current: 12 A Sensitivity: 5 mV/mA
Current View Resistor	T&M Research (W-1-01C-1FC)	Drain Source Current (I_{DS})	Bandwidth: 800 MHz Max. Energy: 20 J Series Resistor: 0.01 mΩ

is characterized by presenting high oscillation frequencies, besides having a low magnitude [100]. An insulated measurement should also be performed, given that the switch gate is not grounded. Therefore, an AC current probe is suitable for this application [101]. For the drain current (I_{DS}), a shunt resistor is enough for the measurement [102].

4.2.1 Passive Voltage Probe Modeling

Measurement instruments should have a minimum impact on the tests and maintain adequate signal fidelity for the measured variable. Basically, three characteristics are suitable when a probe is used to measure voltage: high bandwidth and accuracy with enough voltage range. Likewise, some points should be considered when selecting a probe, such as input impedance, frequency response, total delay, and maximum input voltage. The concept of a high-performance probe is based on connection ease and convenience, high signal fidelity, behavior like an open circuit, and high noise immunity [103, 104].

The interface design between the PCB and probe connection is a source of disturbs. Here, the ideal condition is performed when the loop between positive and negative terminals is as low as possible. Several high frequency applications use SMT (Surface-Mount Technology) connections to connect the tip probe directly on the PCB, without the use of wire for ground lead. Likewise, it is possible to achieve the shortest ground lead provided with the probe [105, 106].

The voltage probe represents a load that has the capacity to draing the circuit current. Therefore, it could be concluded that a suitable voltage probe must have infinite impedance, representing an open circuit to the test point. Moreover, the AC analysis shows that a probe is represented by distributed inductors, capacitors, and resistors, as seen in Figure 4.16. The interaction of all the elements produces a probe of the total variable impedance with signal frequency [104]. Therefore, it is necessary to have a good modeling of the system, to understand and minimize the impact of the probe's passive components [103].

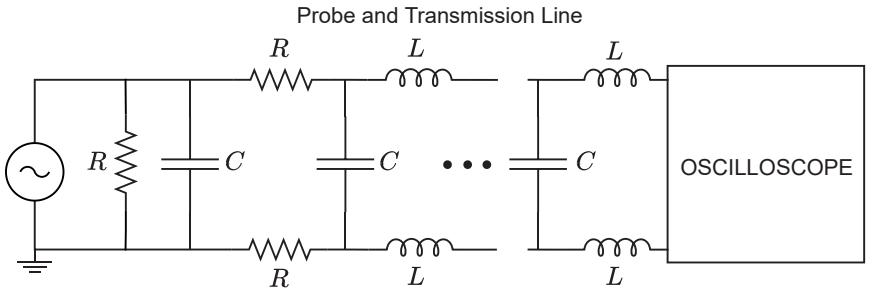


Figure 4.16: Distributed R, L, and C for AC signals [104].

The cable is modeled by a transmission line, as seen in Figure 4.16, which represents a sequence of line elements (R, L and C). It is formed of distributed inductance/capacitance, propagation delay, and signal reflections. More details about transmission model validation and oscilloscope circuit can be found in Section C.1.

A realistic simulation is ever desired by converter designers in order to estimate electrical behavior, calculate losses and protect circuits design. By considering the greatest number of disturbing sources in a simulation, a voltage probe model should be included as an important part of the system. A classical electrical model of a voltage probe is shown in Figure 4.17.

The signal source is modeled by an AC source voltage in series with internal resistance [103]. Then, a parallel circuit compound by a resistive/capacitive divider is used to define the attenuation between the input and output of the probe. The voltage attenuation ($Attn$) of 10, for instance, used for some voltage probes, is achieved by using R_{probe} equals to 9 MΩ, given that the resistance inside the scope equals 1 MΩ in the high impedance mode. In this

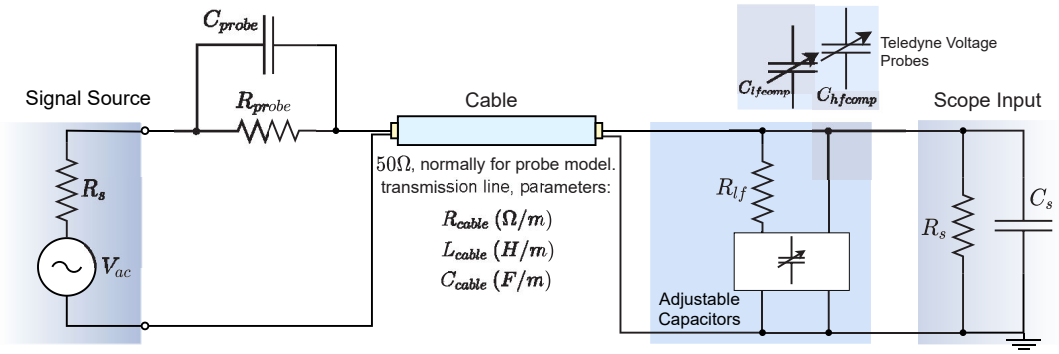


Figure 4.17: Generic simple model for a voltage probe adapted from Teledyne Lecroy [105].

manner, a voltage divider is defined. The capacitor C_{lfcomp} has function of adding a zero in the frequency response of the low-pass filter, formed between the resistors R_{probe} and R_{cable}, and the parallel resultant capacitance along the probe, providing a flat response. The compensation capacitors ($C_{lfcomp} + C_{hfcomp}$) are selected to maintain the factor 1/9 between C_{probe} and the total sum of all capacitances from cable to scope input [103].

The first step to design a passive probe is to verify the voltage attenuation, that will be used to define the resistance ratio, as mentioned previously. Subsequently, cable parameters should be extracted from the datasheet of the cable type used by the probe. For instance, a coaxial cable, normally used by voltage probes, has about 95 pF/m and 237 nH/m [103]. These values are included into the transmission line model. At the end, the probe parameters C_{hfcomp} and R_{cable} are adjusted using its bandwidth limit and ringing tolerance as can be seen in Figure 4.18. A resistor (R_{lf}) in series with C_{lfcomp} is added to impact on the voltage ringing, thus, by acting only as an adjust parameter for the simulation.

The beginning of region A represents the probe behavioral in "DC operation". Its attenuation level is defined by the resistance ratio R_s/R_{probe}. For the case of 10:1 attenuation, this ratio is equal to 1/9. Whereas the frequency increases, the capacitor impedance starts to dominate and the ratio between the probe capacitance (C_{probe}) and the sum of all system capacitances begins to gain importance. The region B is closely related to R_{cable} and R_{lf}, defined in such a way that is has a ringing tolerance of about 30 %, 3dB, not to be reached. In

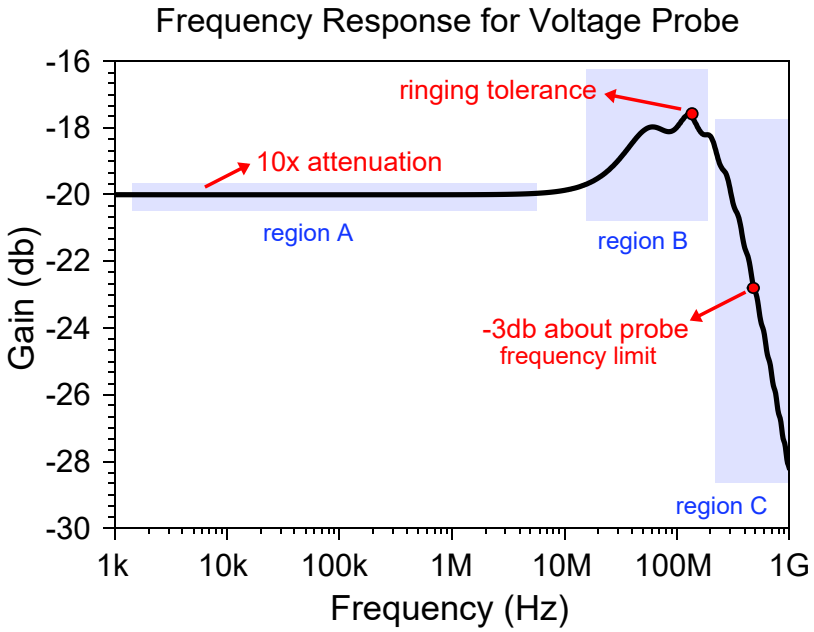


Figure 4.18: Frequency response emphasizing each operation region (simulation from PP024 voltage probe).

the region C, the main component is C_{hfcomp}, the high frequency compensate capacitor. Its value is defined using the concept that, from the upper limit frequency established by probe bandwidth, the waveform skew is maximum in order to represent the attenuation at upper frequencies specified by the probe manufacturer [104].

The resistor R_{lf} corresponds to a series resistance with the low frequency capacitor, as previously mentioned. Its value impacts the influence caused by C_{lfcomp}. Therefore, for a high resistance, C_{lfcomp} acts later within the frequency axis by allowing a shift from $-3\,\mathrm{dB}$ towards higher frequencies. Thus, it can be possible to adjust the limit frequency indicated by the probe manufacturer. It is important to note that for 10x attenuation probes, due to the presence of a large input capacitor, the capacitor C_{hfcomp} should have a small value. In this case, R_{lf} has less influence on the response frequency.

The equivalent circuit, shown in Figure 4.19, provides the resistor and capacitor divider that defines the response for low frequency. To have a flat response, it is mandatory to respect the Equation (4.6). This condition ensures a transformation ratio independent of the frequency [103].

$$\frac{R_s}{R_{probe}} = \frac{C_{probe}}{C_{total} + C_s} = \frac{1}{Attn - 1} \tag{4.6}$$

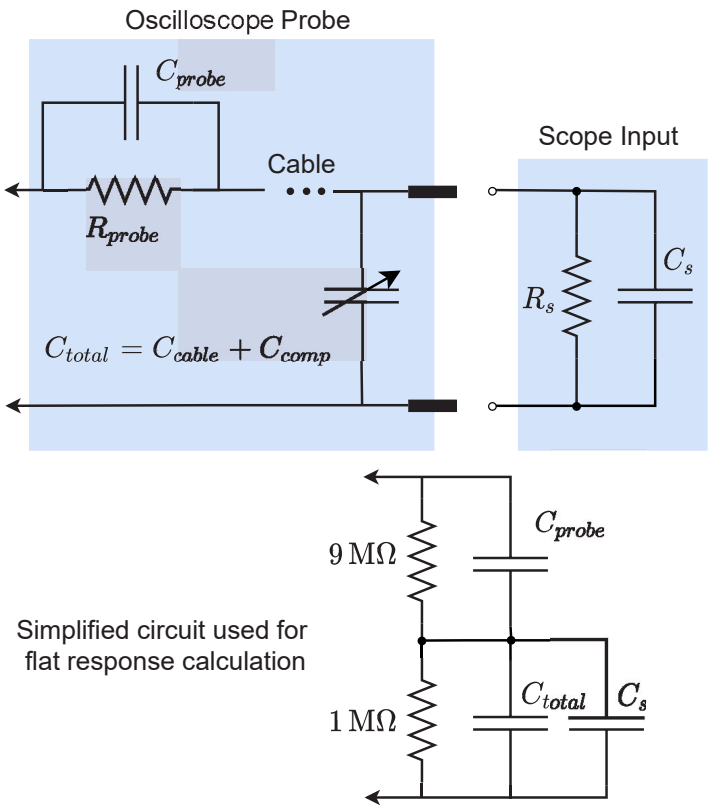


Figure 4.19: Oscilloscope probe circuit (10:1 attenuation) with the equivalent circuit adapted from [105].

The compensation effect is performed for low and high frequencies. The low frequency compensation should be realized by applying a 1 kHz square wave. Forthwith, the adjusting of C_{lfcomp} is performed in order to obtain a perfect square wave that is seen by the scope. This match allowed for the same time constant along the probe. For the high frequency compensation, the cable impedance and scope input capacitance affect the signal waveform directly. However, at a very high frequency, the inductance parasitic into capacitors (from the cable and scope) causes an unintended inductive effect. To attenuate this effect, the C_{hfcomp} acts as an alternative route for high frequency currents. The adjust protocol is performed by applying a 1 MHz square wave (< 0.7 ns rise time) [104], and then by adjusting the capacitor values in order to minimize the overshooting [105]. In Figure 4.20, a flowchart is presented to show the voltage probe model development.

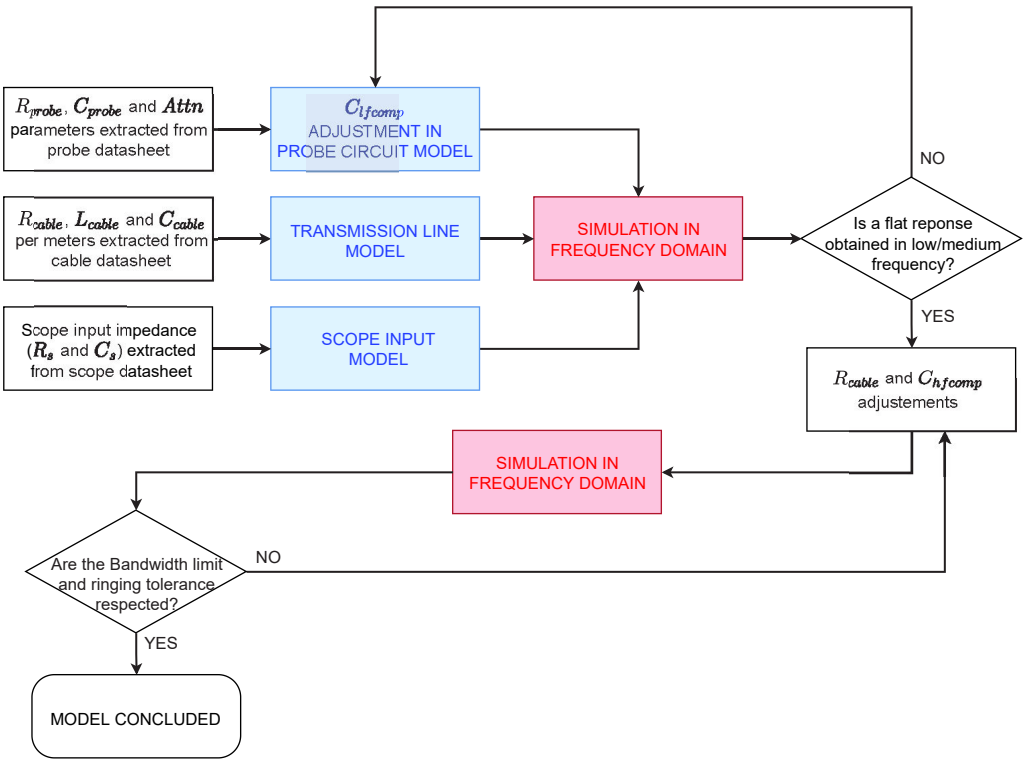


Figure 4.20: Flowchart for voltage probe model development.

4.2.1.1 PP024 Teledyne Lecroy

To analyze the impact of using a medium voltage probe, the Teledyne Lecroy PP024 is selected. Its specifications are given in Table 4.5. Among the main characteristics, it is important to highlight the frequency range of the probe that ensures signal fidelity, and the compensation range. The scope input capacitance must be within this range. Otherwise, the probe will be unable to compensate scope capacitance effect at a high frequency [107].

The PP024 Lecroy offers a bandwidth of 500 MHz. As the scope used, Teledyne WaveSurfer 10, has a BW of 1 GHz, the lower value between the probe and scope bandwidths has the more dominant effect on the system. In this case, the overall system bandwidth is 500 MHz.

Table 4.5: Specifications for Teledyne PP024 Passive Probe.

Model	ATTN	Input Imped.		B/W	Rise Time	Lenght	Compensation range
		R (MΩ)	C (pF)	(MH)	(ps)	(m)	(pF)
PP024	10x	10	10	500	700	1.3	10 - 20

Moreover, a constant relation between resistive and capacitive divider has to be set, as seen in the case of 10x probe. First, the main step to set a probe model is to choose a transmission line model to represent the cable [103]. In this context, the LTspice simulator has a model called LTRA available in its library, as explained above. As the capacitance and inductance parameters can be found in the cable datasheet, the only tunable variable is the cable resistance [104, 105]. Moreover, it appears that this probe manufacturer uses very specific cables. A simulation is performed in the step mode with the HF cap (C_{hfcomp}) and cable resistance (R_{cable}) as variable parameters. Therefore, a few probable combinations are achieved for the specified bandwidth. In practical terms, for the PP024 passive probe, a range frequency of 495-505 MHz is set up, and the frequency responses with an attenuation value around $-23\,dB$ provide the optimal combinations. Hence, the next step is to verify the ringing effect. Normally, it should not exceed -17 dB. Lastly, the LF cap (C_{lfcomp}) is adjusted to reach the $10x$ attenuation. Whereas the signal frequency increases, the parallel capacitance LF decreases, and therefore the input impedance also decreases [105]. The simulated schematic is seen in Figure 4.17, and the Table 4.6 presents the parameters used in the simulation.

Table 4.6: Parameters used for PP024 voltage probe simulation.

Variable	Value	Unit	Description
C_{probe}	10	pF	Input Capacitor
R_{probe}	9	MΩ	Input Resistor
R_{cable}	150	Ω	Distributed Resistors
L_{cable}	237	nH	Distributed Inductors
C_{cable}	95	pF	Distributed Capacitors
C_{lfcomp}	5.5	pF	LF Capacitor
R_{lf}	15	Ω	LF Resistor
C_{hfcomp}	0.1	pF	HF Capacitor
R_s	1	MΩ	Scope Resistor
C_s	16	pF	Scope Capacitor
$Delay$	6.16	ns	Delay added by cable

The input impedance profile can be seen in Figure 4.21. An error percentage of about 15 % between datasheet and simulation was found. This profile is important because it demonstrates the insertion impedance that is parallel to the device under test. In Figure 4.22, the frequency response can be seen as well as the important points emphasized as a guide to the model design.

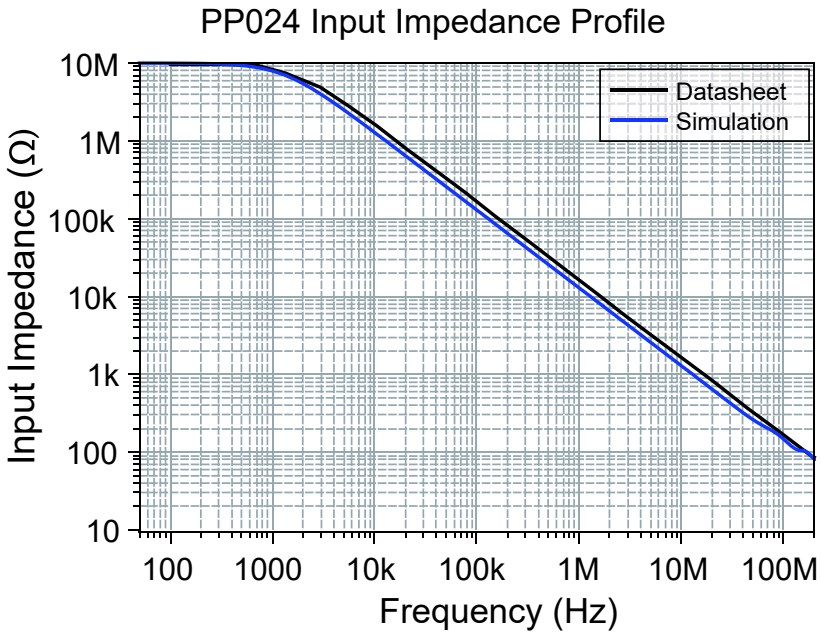


Figure 4.21: Comparison between datasheet and simulation for the PP024 probe model.

For power electronic applications, the voltage probe impedance at low/medium frequencies is very important because of the switching frequency of power converters. For higher frequencies, the harmonic components associated with the fast switching are the main elements for measurements. With the emergence of the wide bandgap devices, the switching speed increases even more. Thus, the characterization of these devices, based on a system that includes the measurement instruments, becomes essential to obtain accurate results.

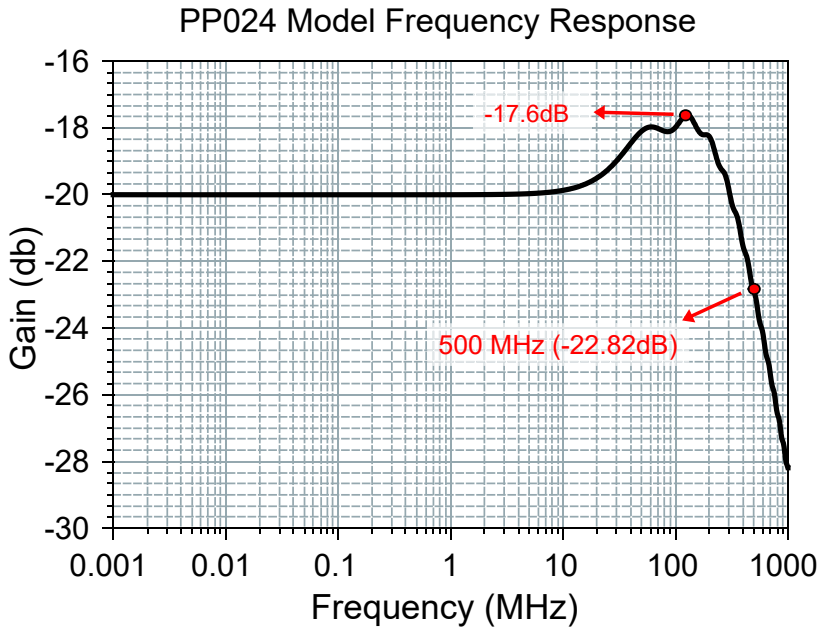


Figure 4.22: Frequency response for the PP024 model validated in LTspice.

4.2.1.2 HVP120 Teledyne Lecroy

To analyze the impact of using a high-voltage probe, the Teledyne Lecroy HVP120 is selected. Its specifications are seen in Table 4.7. This probe has a 100:1 attenuation and low input capacitance that allows for the achievement of higher input impedance values and more accurate frequency responses. Ideally, high input impedance prevents circuit overloading and reduces power dissipation. Furthermore, as WBG devices exhibit lower output capacitance when compared to silicon-based devices, the parallel capacitor added by the probe should be as low as possible.

Table 4.7: Specifications of the Teledyne HVP120 High Voltage Passive Probe.

Model	Attn.	Input Imped.		B/W	Rise Time	Length	Compensation Range
		R (MΩ)	C (pF)	(MHz)	(ps)	(m)	(pF)
HVP120	100x	50	7.5	400	900	2	10 - 50

The electrical schematic can be seen in Figure 4.23. The components with arrows on top could be physically adjusted by a screwdriver. The R_{dc} value is adjusted about 1 MΩ to obtain 100:1 voltage ratio. Initially, the low-frequency compensation is calculated by defining C_{lfcomp} due to the Equation Equation (4.7). In this way, the 100:1 voltage ratio is also obtained in frequency values below the probe bandwidth. Additionally, parasitic capacitances are

added to simulate the distributed capacitors along the transmission line. Table 4.8 presents the parameters used in the simulation.

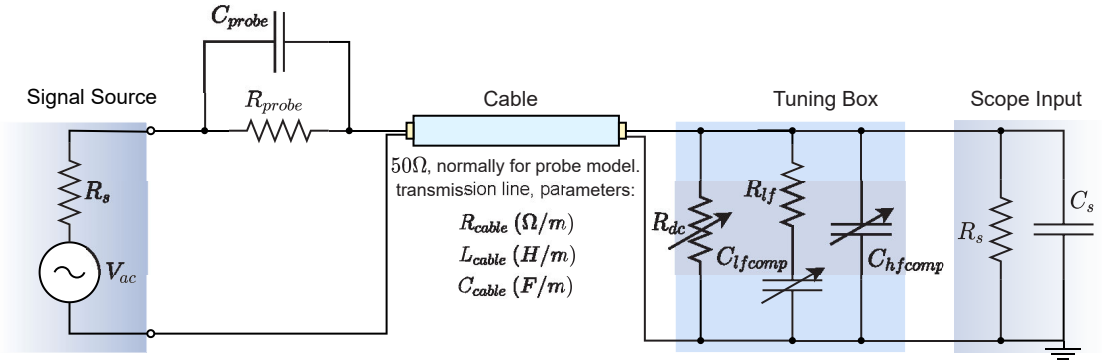


Figure 4.23: Electrical model for the HVP120 high voltage probe.

Table 4.8: Parameters used for HVP120 voltage probe simulation.

Variable	Value	Unit	Description
C_{probe}	7.5	pF	Input Capacitor
R_{probe}	50	MΩ	Input Resistor
R_{cable}	120	Ω	Distributed Resistors
L_{cable}	237	nH	Distributed Inductors
C_{cable}	95	pF	Distributed Capacitors
C_{lfcomp}	422	pF	LF Capacitor
R_{lf}	40	Ω	LF Resistor
C_{hfcomp}	115	pF	HF Capacitor
R_{dc}	1	MΩ	DC Resistor
R_s	1	MΩ	Scope Resistor
C_s	16	pF	Scope Capacitor
$Delay$	9.49	ns	Delay added by cable

$$\frac{C_{probe}}{C_{cable} + C_s + C_{lfcomp}} = \frac{1}{Attn - 1},\ Attn = 100 \tag{4.7}$$

To obtain a satisfactory model, a resistor is added in series with C_{lfcomp} to shift the cutoff frequency of the system towards the probe bandwidth. In Figure 4.24, the output voltage for various R_{lf} values can be seen. For a null resistance value, the cutoff frequency achieved is far from that defined by the manufacture probe. The suitable output response corresponds to the maximum damping effect and simultaneously to the constant attenuation on -40 dB as the inferior boundary. The second step for probe modeling is to define C_{hfcomp}. This capacitor aims to tune the response frequency of the

probe at $-43\,\mathrm{dB}$. Its value should be considerably lower than C_{lfcomp} to ensure that the impedance decreases at a higher cutoff frequency, given that the loop formed by cable resistances and its value has a lower time constant. Simulations with values variation (parametric simulation) allowed for the definition of optimum values for the compensation capacitances, following the new relation established by Equation (4.8).

$$\frac{C_{probe}}{C_{cable} + C_s + C_{lfcomp} + C_{hfcomp}} = \frac{1}{Attn - 1},\ Attn = 100 \tag{4.8}$$

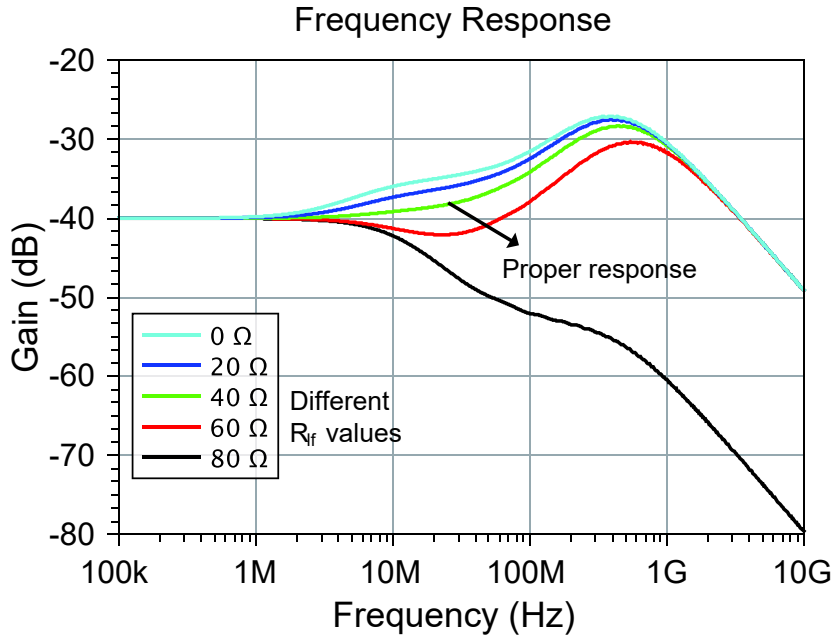


Figure 4.24: Frequency response for different values of R_{lf} and $C_{lfcomp} = 422\,pF$.

Next, input impedance is verified with a E4990A Impedance Analyzer. The tip probe is connected on the high side and the ground on the low side (references from Analyzer), after which the function averaging factor is set in precision mode to obtain more accuracy. In Figure 4.25, a good correlation between the simulation and datasheet for the input impedance can be seen. This is the suitable behavior, given that the impact on simulation caused by the voltage probe on the circuit should be represented. To ensure that the correct bandwidth provided by the manufacturer, the gain is plotted to verify the attenuation at $-43\,\mathrm{dB}$, as seen in Figure 4.26.

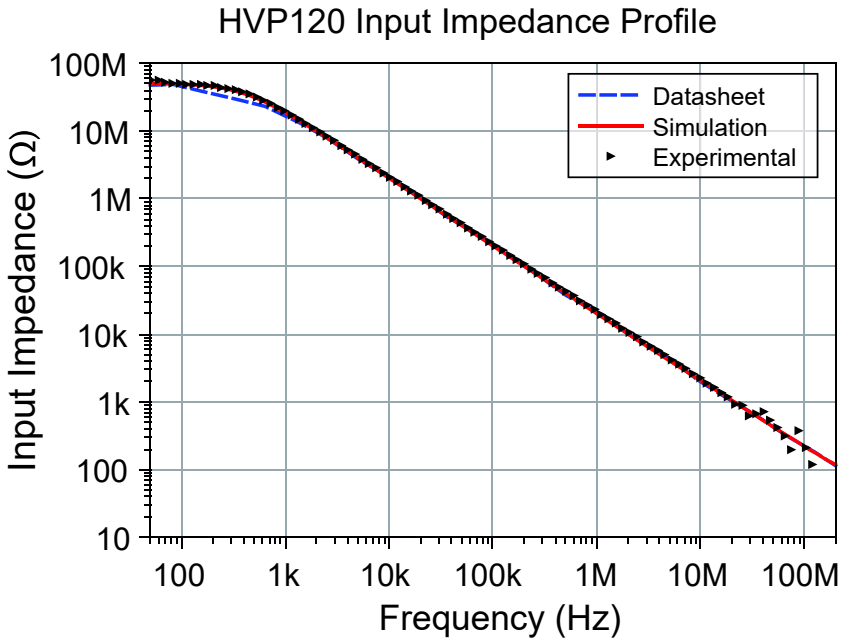


Figure 4.25: Comparison between datasheet and simulation input impedance for the HVP120 probe.

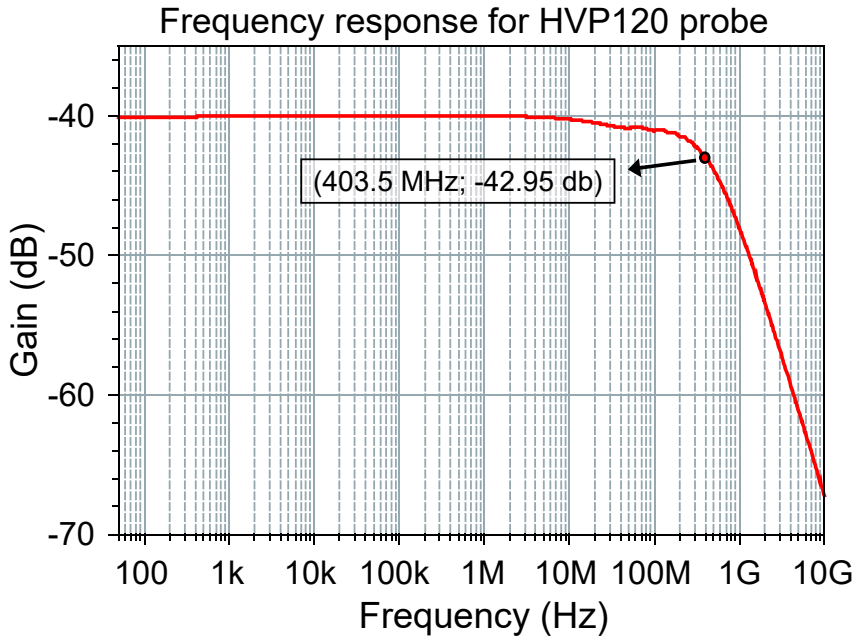


Figure 4.26: Frequency response for model validation.

4.2.2 AC Current Probe

The current probes are based on a current transformer, with CT1/CT2 probes from Tektronix. Further, the working principle focused on the induced effect

established in secondary winding by an alternating current from the primary conductor. In power electronics, for accurate current measurements, some constraints must be satisfied, such as a fair current shape response, enough bandwidth to cover the bandwidth of the measured signal, and low interference on the device under test. These probes are useful for measuring high-frequency currents with minimum circuit loading and for insulated measurements [101]. The current sensors based on Faraday's Law of induction have been widely discussed [108], and also allowed for the building of the CT probes used currently. The main equations for the CT model design and a two-stage current transformer proposal are also presented as an improvement suggestion for usual CT probes [101]. The calculation of coupling capacitance in high-frequency transformer windings is also essential for developing an accurate modeling and has been discussed to some extent [109].

The advantage of using the AC current probe based on a current transformer is the easy insertion into the circuit and low sensitivity to EMI. However, its limitation is linked to direct currents that can saturate the core. For gate current measurements, the direct current is not as important as its AC component, caused by parasitic elements. Therefore, a good result can be obtained when DC current is neglected, and the AC component is a variable in the analysis.

First, a transformer model is implemented in LTspice, as shown in Figure 4.27, to verify the circuit behavior before using it in the full system. Here, it is important to define the mutual inductance as an expression in terms of the two coils' self-inductance L_p and L_s, as seen in Equation (4.9).

$$L_m = k\sqrt{L_p L_s} \tag{4.9}$$

where k is the coupling coefficient, $0 < k \leq 1$. This coefficient determines the coupling level between the primary and secondary coil. In this case, it is assumed that the flux is entirely concentrated, and therefore $k = 1$.

Moreover, a real transformer model can be approached by adding leakage inductance and resistance on the primary and secondary sides, as seen in Figure 4.27 [110,111]. The datasheet of an AC current probe normally provides the total leakage inductance (L_{lk}). Therefore, assuming that $L_{lkp} + L_{lks} = L_{lk}$ and replacing L_{lks} with its reflect value on the primary side, Equation (4.10)

can be written as follows [112].

$$L_{lkp} = \frac{L_{lk}a^2}{a^2 + 1} \tag{4.10}$$

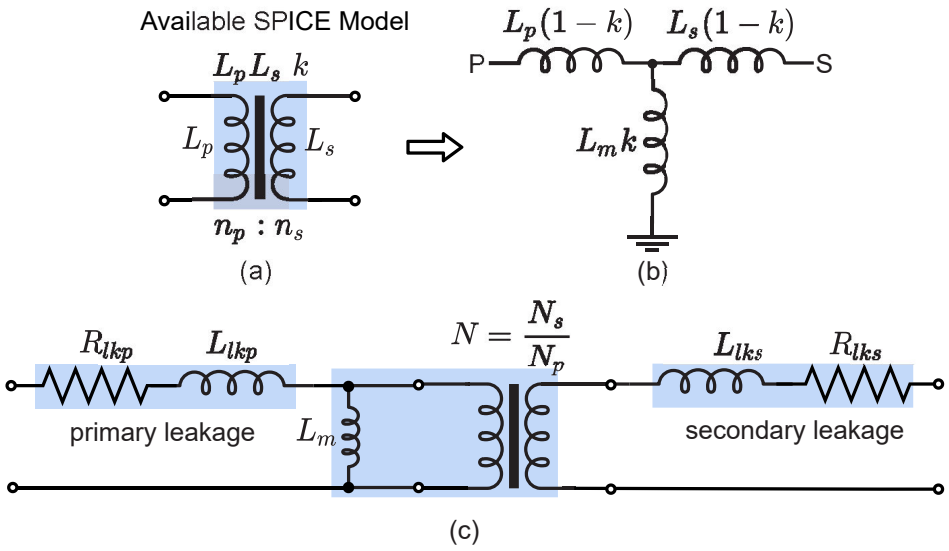


Figure 4.27: (a) The coupled inductors of the available SPICE model. (b) The equivalent circuit. (c) Real transformer built by adding some components to the coupled inductors model adapted from [112].

The simulated circuit can be seen in Figure 4.28 ,and the parameters used for the simulation are presented in Table 4.9. Moreover, the transformer is modeled based on the bond graph model and the classical schematic for current transformers [113]. Following the circuit, a resistance load is added for ratio correction, given that the level current is attenuated to the output. The cable model is also implemented, and finally, a resistance is used to represent the input 50 Ω from the scope [114].

Subsequently, the low-frequency is verified in simulations and compared to datasheet values, to verify whether an adjustment is necessary. Next, to calculate the low-frequency cutoff (f_L), Equation (4.11) is obtained. More details are presented in Section B.1. The simulation of the frequency response is compared to the datasheet and can be seen in Figure 4.29.

$$f_L = \frac{R_{DC}}{2\pi L_m} \tag{4.11}$$

where R_{Leq} is the output equivalent resistance, and L_m is the magnetizing transformer inductance.

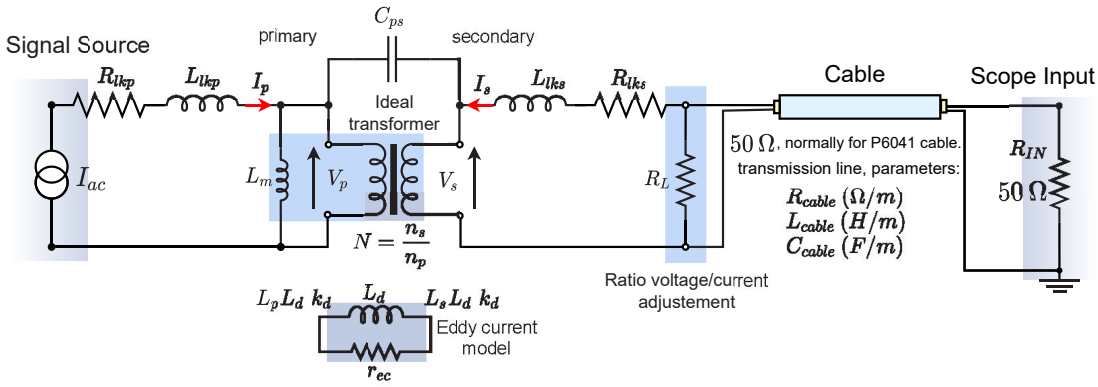


Figure 4.28: Circuit model proposed for CT1/CT2 probes from Tektronix [101].

The injection of AC current by a signal source helped define the lower bandwidth of the system, by the analysis of the output signal on the scope input set up in the 50 Ω termination. A model for the P6041 cable allowed for the direct connection to the oscilloscope. In Figure 4.30, a flowchart is presented to clarify the CT probe model development.

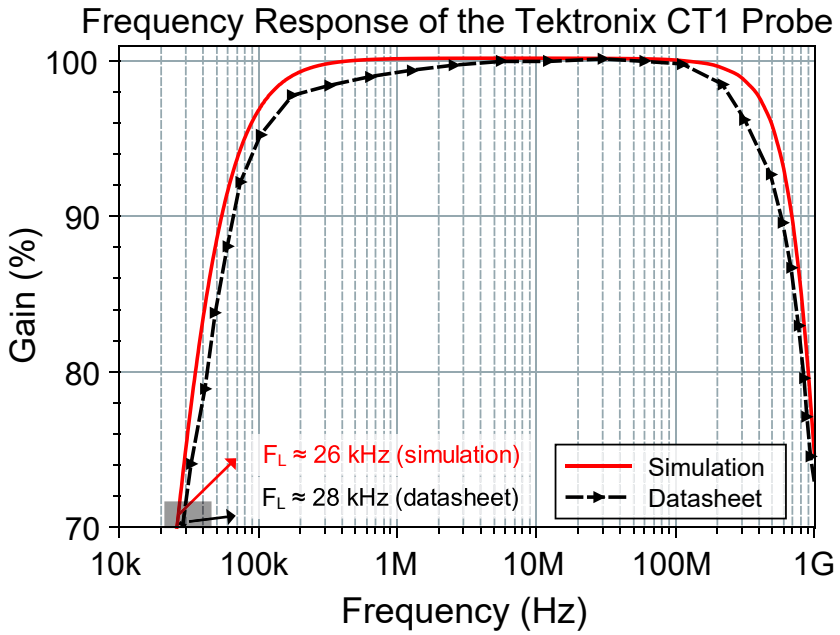


Figure 4.29: Comparison of the CT1 frequency response between the simulation model (Figure 4.28) and datasheet.

Table 4.9: Parameters used for CT1 probe simulation.

Variable	Value	Unit	Description
R_{lkp}	1	mΩ	Primary Leakage Resistor
L_{lkp}	1	nH	Primary Leakage Inductor
L_m	6	uH	Magnetizing Inductor
C_{ps}	13	pF	Coupling Capacitor
L_p	L_m	uH	Primary Winding Inductor
L_s	L_m/a^2	uH	Secondary Winding Inductor
L_d	L_m	uH	Eddy Current Inductor
k_d	1	-	Eddy Current Coupling
r_{ec}	10	Ω	Eddy Current Resistor
N	5	-	Transformation Ratio
L_{lks}	5	nH	Secondary Leakage Inductor
R_{lks}	5	mΩ	Secondary Leakage Resistor
R_L	51.5	Ω	Loading Resistor
R_{cable}	50	mΩ	Distributed Resistors
L_{cable}	237	nH	Distributed Inductors
C_{cable}	95	pF	Distributed Capacitors
R_{IN}	50	Ω	Scope Resistor
$Delay$	4.75	ns	Delay added by cable

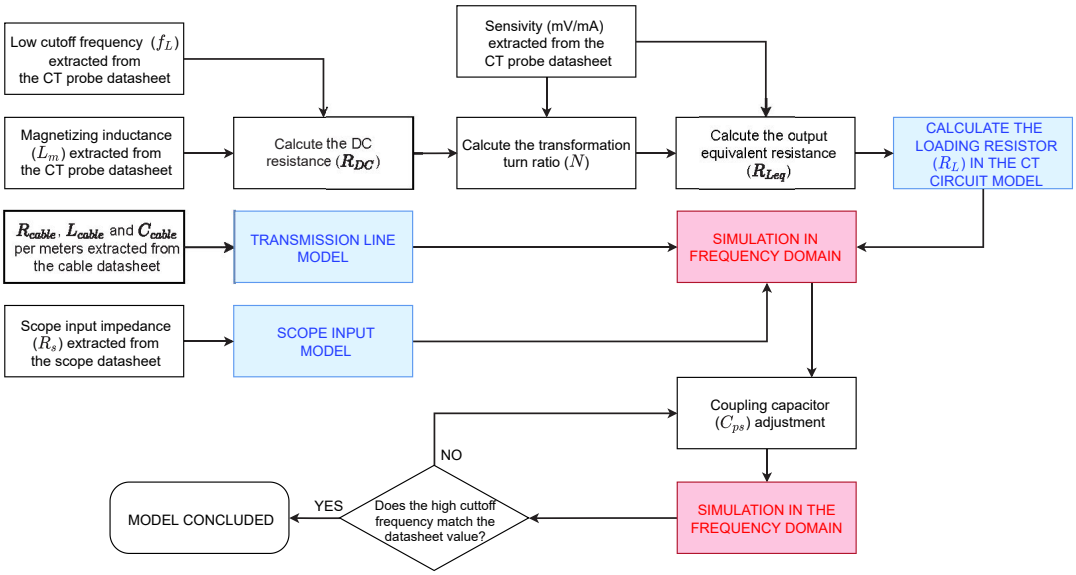
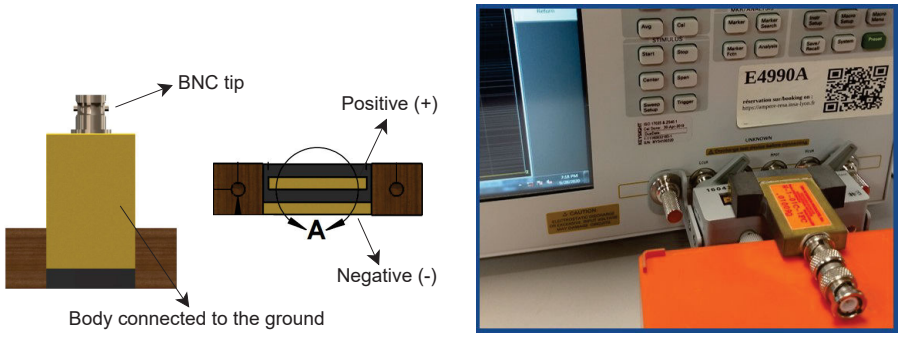


Figure 4.30: Flowchart for CT probe model development.

4.2.3 Current Viewing Shunt Resistor

The Current Viewing Resistor (CVR) is a high bandwidth sense resistor (low-value) used for current measurement on a low side switch. In addition, there is no insulation between the circuit being tested and the device under test, which allows better performance in terms of bandwidth, nevertheless, the shunt must be grounded [108]. The main disturbances on the switching cell caused by a CVR is the additional inductance introduced by the coaxial shunt body and extra PCB traces [102, 115, 116]. The CVR used in this study is the W-1-01C-1FC Clamping Type from T&M Research, seen in Figure 4.31(a). It is a shunt rated at a bandpass 800 MHz and $E_{max} = 20\,J$ thus, there are no issue for pulsing tests. Moreover, the accuracy of a shunt is related to the ambient temperature, due to its internal resistance, and the degrading effects caused by transient temperature rise during measurements [116]. Meanwhile, a detailed introduction and the electrical schematic of current sensors based on Ohm's Law of resistance are presented in [108]. Tests in high frequency switching using GaN-based circuits have been widely performed [102, 115]. In simulation level, some papers have shown the importance of considering the PCB parasitic elements to simulate the test board [8, 102, 115]. A shunt with a minimum inductance and a high signal fidelity is thus necessary and has been studied by means of new geometry configurations [116].

Here, an LTspice simulation is implemented to evaluate the impact on the current signal when using a CVR. The simulation is performed by using a current step function and a simple model for oscilloscope. Furthermore, the cable model is also added. The schematic can be seen in Figure 4.32. The value for insertion inductance found into the shunt is estimated with an impedance analyzer, as seen in Figure 4.31(b). In Figure 4.33, a flowchart is presented to clarify the CT probe model development.



(a) (b)

Figure 4.31: (a) Small terminating type CVR series W 5 watt (W-1-01C-1FC). (b) Shunt connected to the E4990A Impedance Analyser.

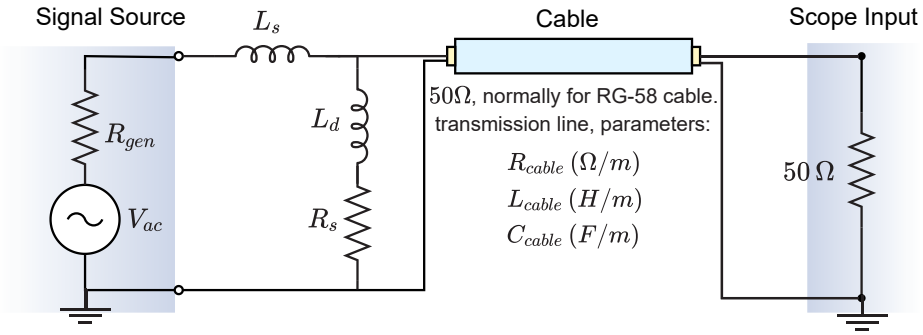


Figure 4.32: Circuit model of a current shunt resistor simulated in LTspice.

Table 4.10: Parameters used for T&M Shunt simulation.

Variable	Value	Unit	Description
L_s	2.4	nH	Shunt Inductor
L_d	0.1	pH	Leakage Inductor
R_s	10	mΩ	Shunt Resistor
R_{cable}	5	mΩ	Distributed Resistors
L_{cable}	237	nH	Distributed Inductors
C_{cable}	95	pF	Distributed Capacitors
R_{IN}	50	Ω	Scope Resistor

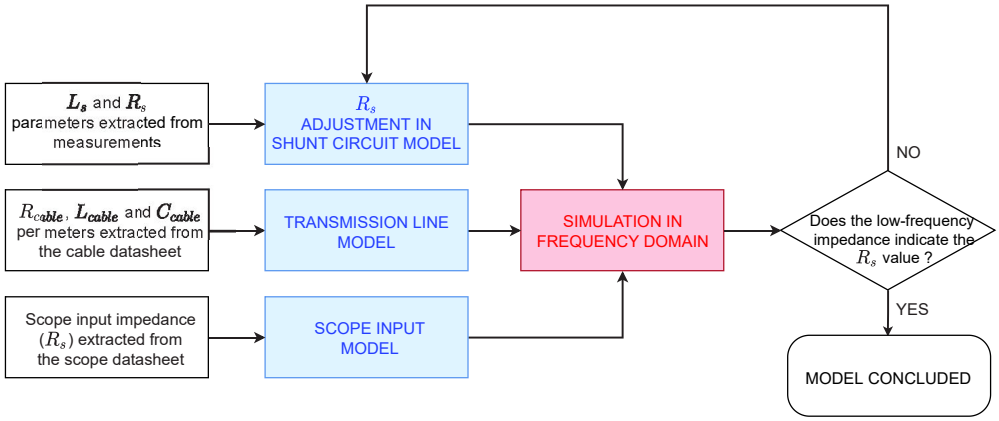


Figure 4.33: Flowchart for T&M Shunt model development.

A good comparison between simulation and experimental data can be seen in Figure 4.34. Here, the insertion inductance was about 2.4 nH at high frequency range, by validating the developed SPICE model. For the resistance calculation, the B1505A Curve Tracer is used due to the high accuracy required to measure the low shunt resistance. The results are seen in Figure 4.35. The calculated current (I_{cal}) was obtained from a linearization method of the injected current (I_{drain}), supplied by the Curve Tracer, that flows through the shunt.

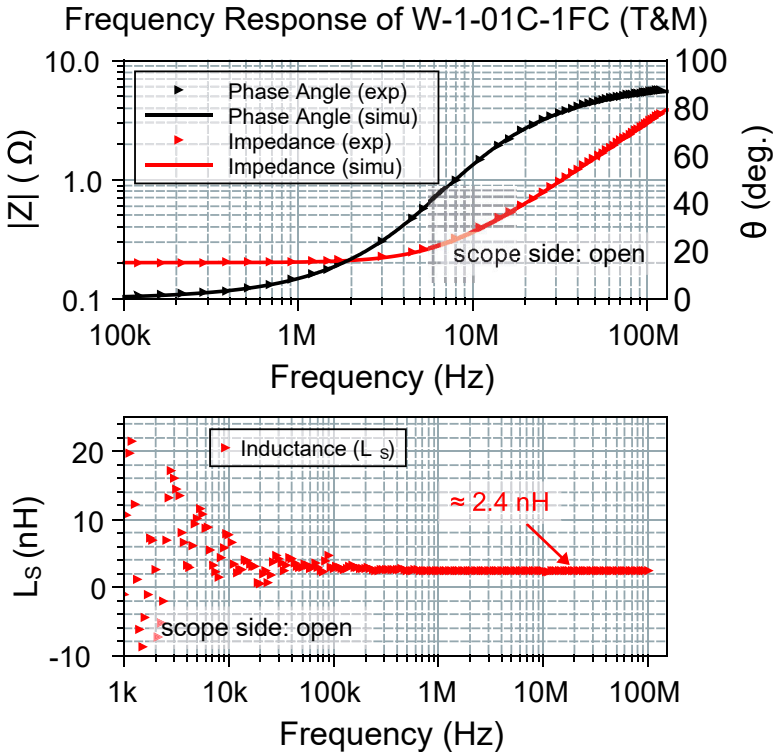


Figure 4.34: Frequency response of shunt W-1-01C-1FC. The experimental results are compared to the model simulation (accuracy of 10 %) [117].

In Figure 4.36, a delay between input and output signals due to the signal propagation in the cable length can be seen. For the input of the shunt simulation, a measured voltage (CVR variable) from a switching cell was used. Thus, the ratio current/voltage of 100 can be verified. In LTspice simulation, the delay value can be also verified, when a shunt resistor model is used. Therefore, it possible to conclude that a phase correction is mandatory for an accurate switching loss estimation.

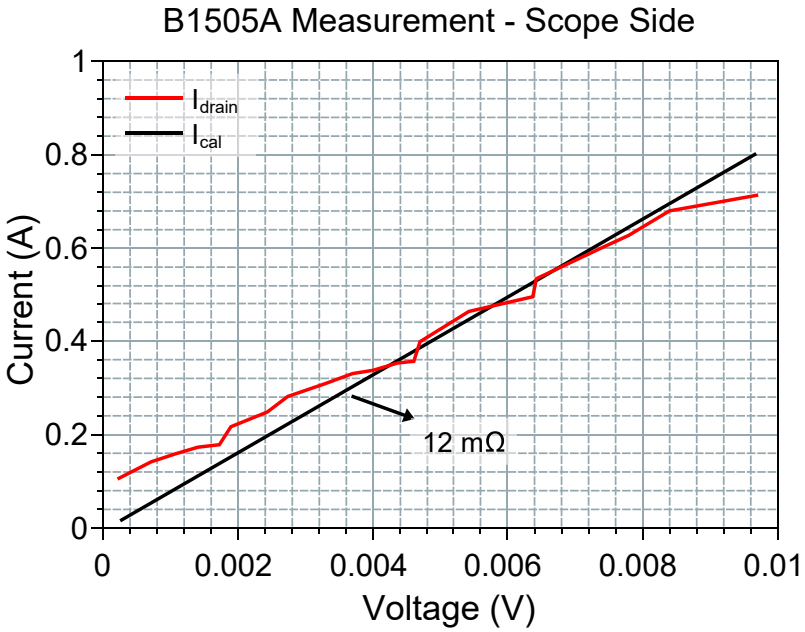


Figure 4.35: Shunt resistance calculated at 10 mΩ with a Curve Tracer.

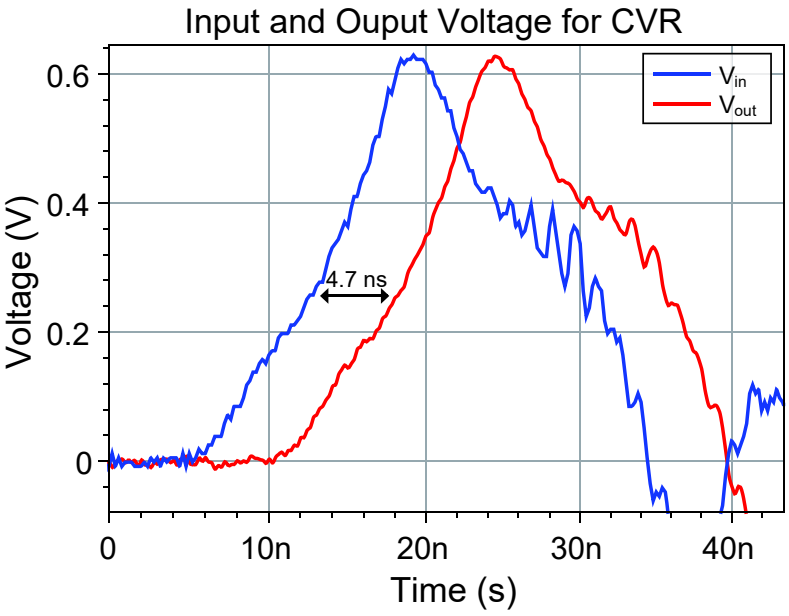


Figure 4.36: Comparison between input and output signals of a CVR.

4.3 Analysis of Electromagnetic Disturbances

4.3.1 Parasitic Element Modeling of a Power Module based on GaN Devices

This chapter aims to evaluate a GaN-based power module for automotive applications. To this end, simulations and experiments were performed on a classical DPT bench. In regard to EMC, the oscillations on the V_{DS} after device turn-OFF are quite important. The comparison between a simulation without considering the 3D wiring model and one considering the wiring elements are presented. The impact of the parasitic element modeling is seen through the resonance frequencies found. The GaN Systems evaluation board consists of a motherboard and an IMS module, as can be seen in Figure 4.37.

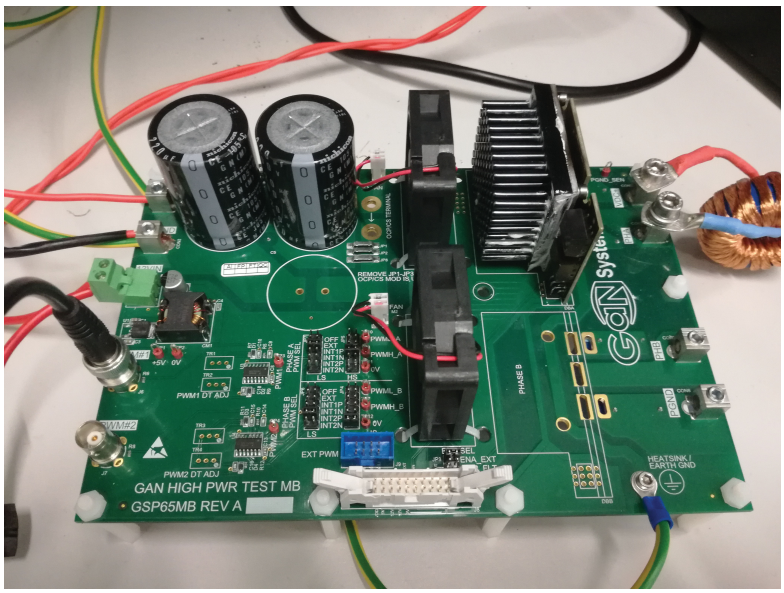


Figure 4.37: Evaluation board from GaN Systems.

The implemented configuration is an one-leg inverter with two power devices by switch. For all tests, a switching frequency of 100 kHz was first defined. Several pulse tests are then applied on GaN GS66516B under different load currents. To realize the measurements, a differential ISOVU probe TIVH08/TIVH08L with a bandwidth equal of 800 MHz is used. This probe is chosen due to the high frequency of oscillation seen on GaN components. As

can be seen in the Figure 4.38, a good correlation is verified between the simulation and test results for a nominal condition at 100 V and 35 A. Table 4.11 presents the three main oscillation frequencies detected by FFT applied on the voltage midpoint.

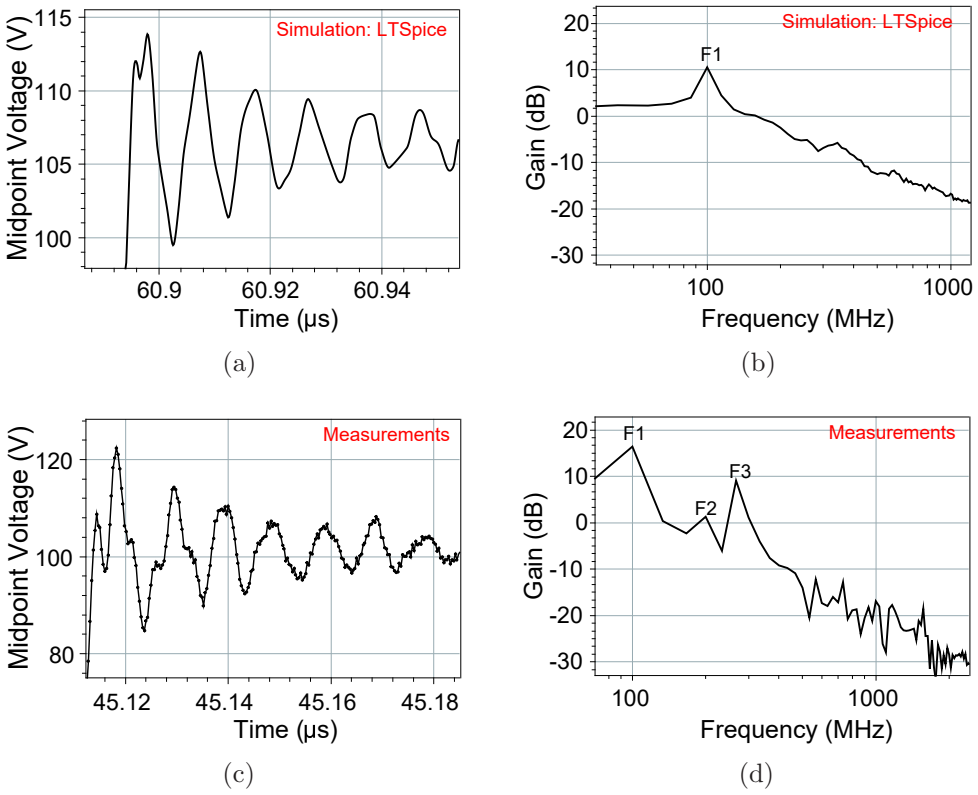


Figure 4.38: Condition test: 100 V and 35 A. (a) Midpoint voltage from simulation and (b) its FFT. (c) The voltage on the midpoint from measurement results and (d) its FFT from the measurement results.

Table 4.11: Comparison between simulated and measurement results under the following conditions: 100 V and 35 A.

Parameters:	LTSpice	ISOVU Probe
Overshooting (V)	114	122
Rise time (ns)	6.4	6.8
Freq. 1 (MHz)	100	100
Freq. 2 (MHz)	n/a	199
Freq. 3 (MHz)	n/a	267

While the frequency at 100 MHz is seen on the simulation and with the ISOVU probe, additional ringing frequencies are detected, but not on the simulation.

This is the first evidence of the parasitic elements due to PCB tracks. Further, another experimental test is defined, but at 400 V, with the aim of verifying the ratio between the output capacitor and the power loop inductance, given that this capacitance changes with the voltage applied. In Figure 4.39 and Table 4.13, the results are presented.

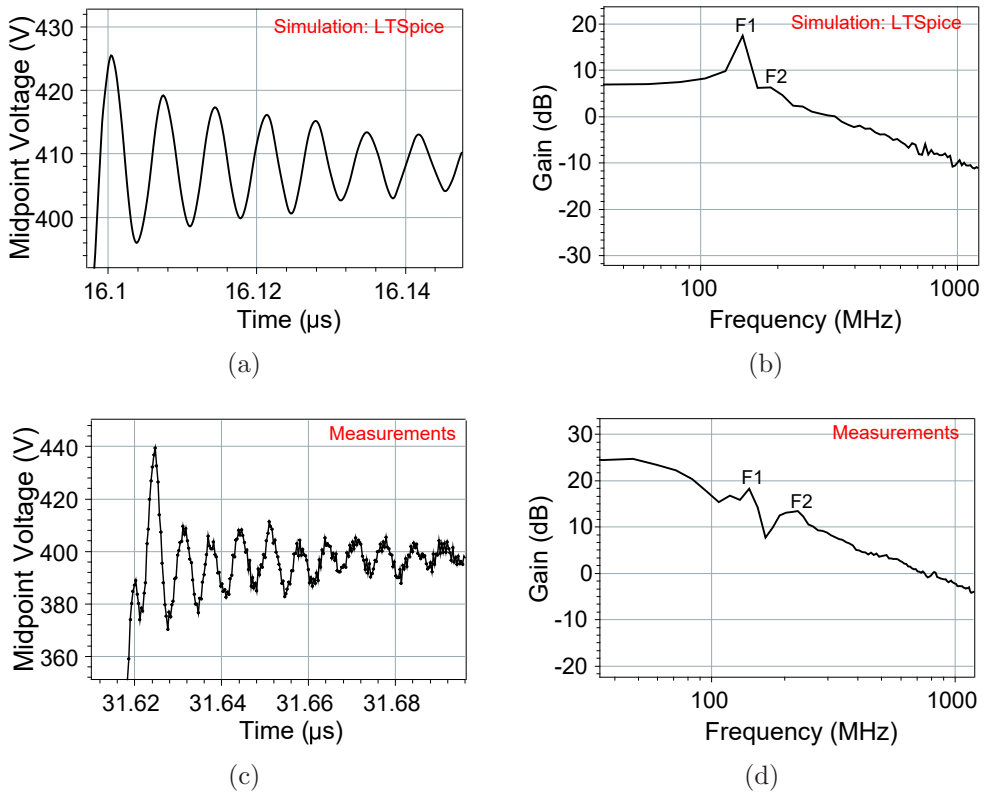


Figure 4.39: Condition test: 400 V and 41 A. (a) Midpoint voltage from simulation and (b) its FFT. (c) The voltage on the midpoint from measurement results and (d) its FFT from the measurement results.

Table 4.12: Comparison between simulated and measurement results under the following conditions: 400 V and 41 A.

Parameters:	LTSpice	ISOVU Probe
Overshooting (V)	425	438
Rise time (ns)	7.7	11.4
Freq. 1 (MHz)	146	144
Freq. 2 (MHz)	n/a	223
Freq. 3 (MHz)	n/a	n/a

As can be seen in the simulation and test results of Figure 4.38 and Fig-

ure 4.39, after the switch turn-OFF, there is an oscillation at the frequency $1/(2\pi\sqrt{LC})$ between the output capacitor of the switch (2×300 pF@100V and 2×150 pF@400V) and the parasitic inductance. This oscillation at the frequency $1/(2\pi\sqrt{LC})$ is a well-known effect and is, for example, expressed with GaN in the reference [118]. Meanwhile, in the LTspice simulation, the parasitic power loop inductance is adjusted at 100 V in order to ensure that the first frequencies of the measurement and simulation match at 100 MHz. Without having to readjust the parasitic inductance value ($\mathrm{L} = 4.1\,\mathrm{nH}$), a matching frequency for simulation and tests at 400 V, around 140-150 MHz, is also obtained. It is important to note that the LTspice simulation shows an exponential decrease in the oscillation, while the measurements in Figure 4.39 do not show an exponential decrease.

Based on the experimental results, the conclusion is that for higher oscillation frequencies, a considerable gap exists between their values and amplitudes. Therefore, it is necessary to add lower capacitances and inductances in the simulation to achieve accurate oscillation simulations at higher frequencies.

4.3.2 3D Model of the Power Loop Inside the Simulation

As the voltage and current increase, the parasitic effects become more evident and new oscillation frequencies can be observed. To understand the measurement of oscillations containing multiple frequencies, a 3D model of the power loop was included inside the LTspice simulation. The power module is modeled using the ANSYS SpaceClaim, after which the ANSYS Q3D Extractor is used to extract the parasitic elements [118].

To model the power module, some factors should be considered. More specifically, the geometry is initially built on SpaceClaim and then exported to Q3D Extractor. Before running the simulation, it is mandatory to verify whither there are some contacts between the objects of the 3D model as all intersections must be eliminated. Another important point is the definition of the NETs (regions with the same electrical potential). Simplified regions imply an easier mesh operation, and consequently with fewer possibilities of errors in the simulation. It is also necessary to define the frequency when there are

mainly surface currents on the device. This is the definition from ANSYS Q3D for path currents through the geometry. For this case, 150 MHz was used. Further, when using ANSYS Q3D simulation in LTSpice, PCB trace modeling allows us to see higher frequencies on switching waveforms. This is very important for switching loss estimation and knowing where the design of the converter should be improved [119].

Moreover, two operation points at 400 V and 71 A/110 A are defined. It is important to emphasize the variation of the midpoint voltage waveforms between 41 A, 71 and 110 A operation, as seen in Figure 4.39, Figure 4.40, and Figure 4.44.

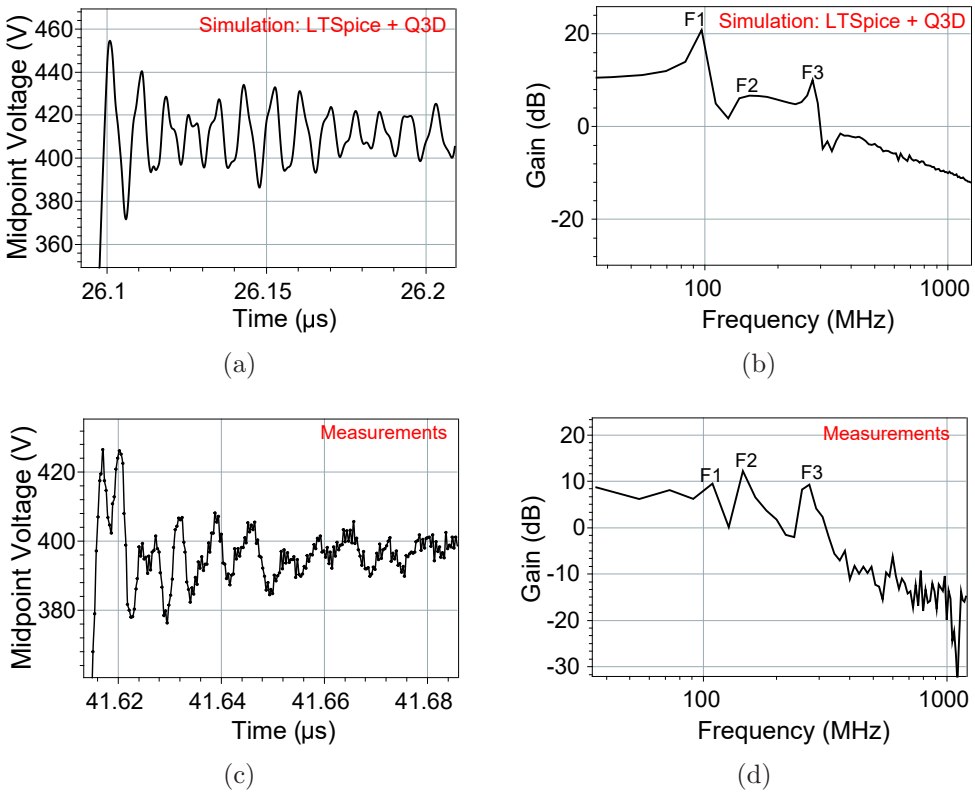


Figure 4.40: Condition test: 400 V and 71 A. (a) Midpoint voltage from simulation and (b) its FFT. (c) The voltage on the midpoint from measurement results and (d) its FFT from the measurement results.

The simulation (LTSpice with Q3D) and the test results show similar behavior with a non-monotonous decrease of the oscillation amplitude. This can be explained by the mutual inductance effect and the accurate calculation

Table 4.13: Comparison between simulated and measurement results under the following conditions: 400 V and 71 A.

Parameters:	LTSpice + Q3D	ISOVU Probe
Overshooting (V)	454	426
Rise time (ns)	6.7	8.7
Freq. 1 (MHz)	98	108
Freq. 2 (MHz)	157	146
Freq. 3 (MHz)	275	272

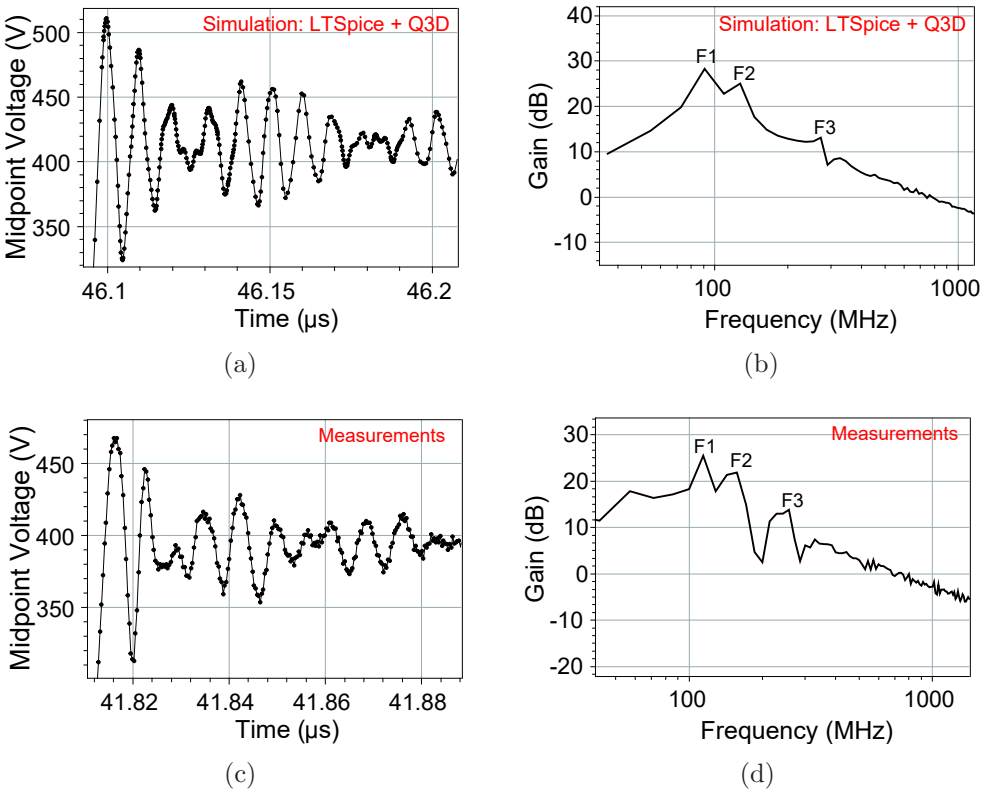


Figure 4.41: Condition test: 400 V and 110 A. (a) Midpoint voltage from simulation and (b) its FFT. (c) The voltage on the midpoint from measurement results and (d) its FFT from the measurement results.

Table 4.14: Comparison between simulated and measurement results under the following conditions: 400 V and 110 A.

Parameters:	LTSpice + Q3D	ISOVU Probe
Overshooting (V)	510	466
Rise time (ns)	6.5	8.5
Freq. 1 (MHz)	92	113
Freq. 2 (MHz)	127	154
Freq. 3 (MHz)	270	250

of parasitic elements performed by the 3D Model. Stray impedances are extracted by using the Q3D Extractor and providing RLC elements with the same solver by combining the finite element method and the method of moments. In the end, a good frequency match for the operation points evaluated can be reached.

The differences found in the switching frequencies for different level currents at the same voltage can be related to the mutual inductance effect. When the current level that crosses a track increases, the mutual inductance effect with another conductor is highlighted. The strong voltage overshoot value is related to the power commutation loop, as well as the distance between the decoupling capacitors and the IMS power module. In this context, it would be ideal to use the capacitors as close as possible to the switches [120].

4.3.3 Parasitic Analysis

The modeling of partial inductance is based on the 3D model of the power module, on different current paths defined by the position of the Q3D excitation, and on the distance between conductors due the coupling effect [121]. In Figure 4.42, the modeling of the power module performed on the SpaceClaim and Q3D Extractor can be seen. The system is composed of three main parts: a PCB driver, IMS power, and a heat sink.

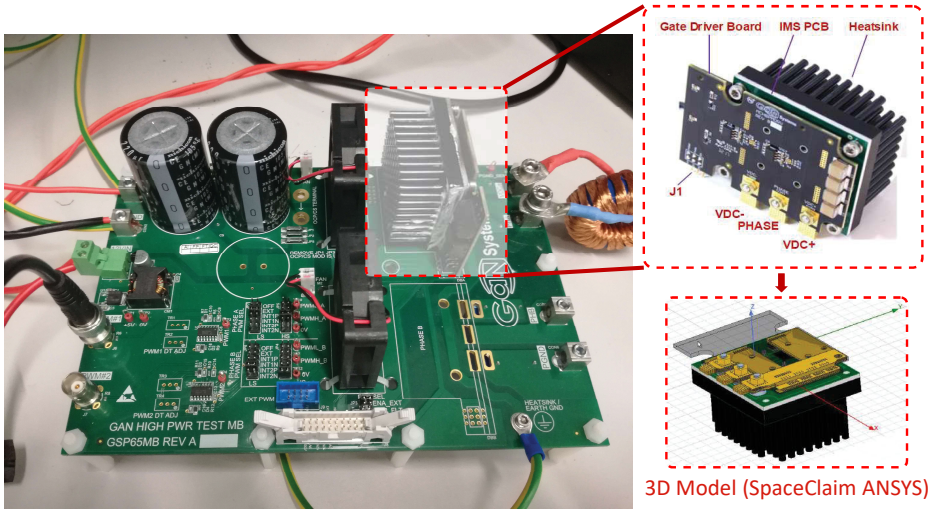


Figure 4.42: GaN System power module in the ANSYS Q3D Extractor.

Moreover, parasitic capacitance is another very important part of the PCB de-

sign. As the voltage applied on the switches increases, the output capacitance decreases. Therefore, it is possible to observe higher oscillation frequencies. Further, the common mode capacitances have influences from a frequency of 200 MHz, and this is seen by the values from the capacitance matrix generated by ANSYS Q3D. To understand the role of the parasitic elements, the impact of the layout between the middle point and the drain of the low side switch was analyzed, as seen in Figure 4.43.

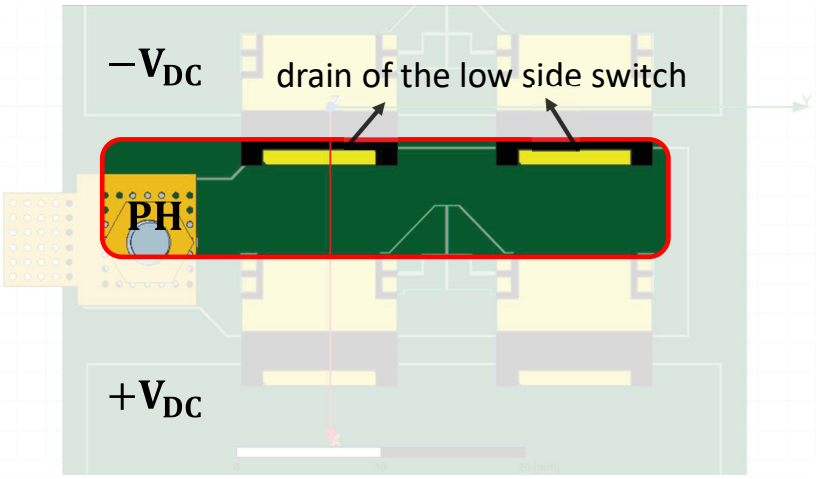


Figure 4.43: IMS layout between the middle point and the drain of the low side switch.

In Figure 4.44(a), it is possible to see the coupling at 100 MHz due to the power loop inductance and the equivalent output capacitance as well as the associated parasitic elements. Similarly, in Figure 4.44(b), it is clear that the coupling for a frequency of 280 MHz is due to a resonance between the equivalent inductance (L_{eq} = 9.1 nH) on the drain low side switch and the parasitic capacitance. In this case, the equivalent inductance is calculated considering the self and mutual inductance on the power commutation loop. Also, the capacitance of only one switch is considered to explain the 280 MHz frequency. It is possible because when the power module operates in a high current level, the unbalanced current becomes more evident [122].

In Figure 4.45, it is possible to see that the equivalent inductance adjusts the drain source voltage (V_{DS}) to match the middle point voltage waveform (V_{PH}). These components are directly linked to the paths of disturbances in common mode, and therefore the modeling of these components is essential

in the prediction of voltage disturbances [123]. Further, the influence of the parasitic element L_{eq} can be demonstrated using a superposition of voltage waveforms, as per Equation (4.12).

$$V_{ph-calc} = V_{DS} + L_{eq}\frac{dI_d}{dt} \tag{4.12}$$

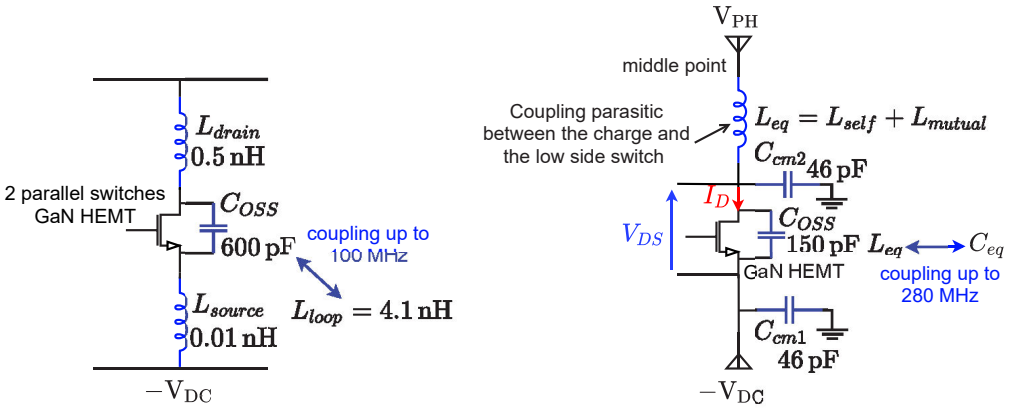


Figure 4.44: (a) Electric diagram of the resonant loop at the frequency of 100 MHz for an applied voltage of 100 V, and (b) Electric diagram of the low side switch and parasitic elements associated with an applied voltage of 400 V.

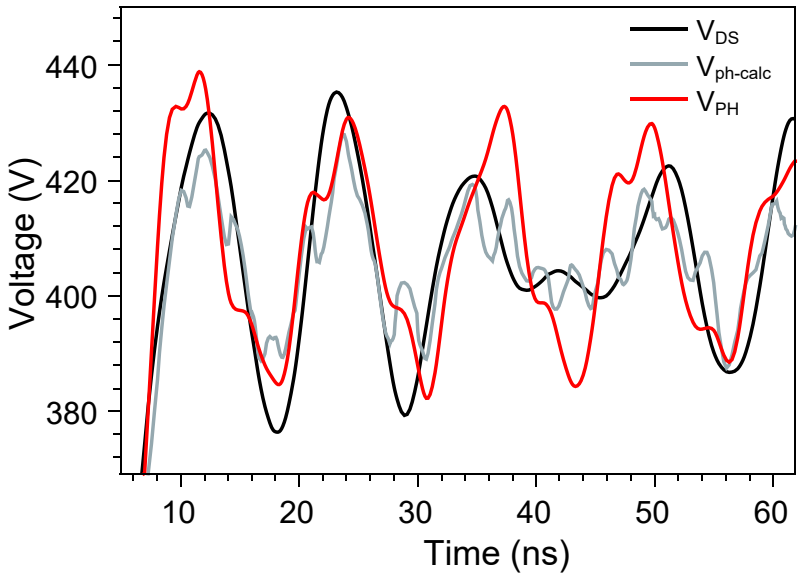


Figure 4.45: Comparison between drain-source voltage (V_{DS}), middle point voltage (V_{PH}), and its calculated value ($V_{ph-calc}$).

The base principle considered in this approach is to consider the three main resonant frequencies in the voltage waveforms of the middle point and drain-source. Here, good results have been found by simulation. Moreover, the values of the estimated elements have been compared to the ones extracted by the numerical tool. Clearly, the use of a 3D model for the extraction of the parasitic elements improves the simulation and measurements fitting.

Further, the analysis of the electromagnetic disturbance is easier in the frequency domain than in the time domain. In the frequency domain, it is simpler to see which frequency bands make more contribution to the source of electromagnetic disturbance, and thus to determine a solution to reduce the disturbances.

4.4 Conclusion and Perspectives

The comprehensive analysis of the impact of the wiring parasitic elements can improve the accuracy of switching loss estimation. Furthermore, by means of experimental results, the need for a good modeling of instrument measurements and a 3D Model for parasitic extraction was verified. Moreover, a simulation considering the power and gate loop inductance can yield a good match with experimental data. This approach allowed for the validation of all models used in the SPICE simulations, and thus made it possible to more accurately evaluate the overall efficiency of converters based on GaN components, including those that will be not instrumented.

Moreover, the parasitic analysis of the GaN-based power module aimed to view the three main resonant frequencies in the voltage waveforms of the middle point and drain-source. Here, good results were found by simulation. Next, the values of the estimated elements were compared to the ones extracted by a numerical tool. Thus, it is clear that the use of a 3D model for extraction of the parasitic elements improves the simulation and measurement fitting.

Meanwhile, the analysis of the electromagnetic disturbance is easier in the frequency domain than in the time domain. In the former, it is easier to observe which frequency bands make more of contribution to the source of electromagnetic disturbance and thus to determine a solution to reduce the

disturbances.

Overall, a comprehensive study about the measurement instruments used for WBG devices allows for the understanding of the impact of each element on circuit loading. In this context, a clear protocol for measurement instrument modeling was presented. The fast-switching speed of GaN devices requires this modeling to achieve an accurate simulation. The comparison between the datasheet, simulation and experimental tests presented a good correlation in relation to input impedance characteristics. Therefore, the impedance seen by the circuit can be estimated in a global simulation. Furthermore, the frequency responses of the models was also simulated to compare them with datasheet limits showing a bandwidth quite close to the specification of the measurement instruments.

CHAPTER 5

Switching Loss Estimation

5.1 Switching Validation

The high power density capability of WBG power devices with the potentially fast switching and low losses make them suitable for automotive applications where performance and low weight are keys to the development of more compact power converters. GaN power devices exhibit a better performance as compared to those made of Si due to their superior critical electric field and high electron mobility in the 2DEG channel. This allows for lower capacitance values and therefore, high-speed commutation, in addition to having a lower on-resistance. However, these improvements bring new challenges when it comes to the loss measurements of the converters based on GaN material. Moreover, the SiC devices allow higher voltage operation and, due to their fast switching (high dv/dt and di/dt), the same issues found in the GaN devices in terms of losses estimation are also detected.

The experimental results are used to validate the SPICE model of the device and for loss estimation. Moreover, with the validated model, it will be possible, through simulation, to evaluate the losses in an optimized circuit without measurement probes [5, 118]. In Figure 5.1, the full schematic is presented including all measurement instruments used for the tests, input filter for the DPT, and drivers for GaN devices. Currently, GaN devices have the fastest switching capability among power devices on the market, and thus, they are

chosen to validate the device model and the measurement instrument models. The relevance of the parasitic elements becomes high due to this fast switching speed. Figure 5.2 shows the main inductance values used for simulation. Next, the gate loop inductance (L_{Gloop}) is extracted from ANSYS Q3D, the package inductance of the power devices package (L_{SW}) is obtained from the datasheet, and the shunt insertion inductance and the power loop inductance were measured using an Impedance Analyzer. The power loop inductance is also simulated using ANSYS Q3D to validate the extraction method.

The first simulation in LTspice is performed without considering the measurement instruments modeling. Afterwards, all measurement instrument models are added to show the disturbing effect on GaN switching by means of the comparison with experimental results. Figure 5.3 and Figure 5.4 present the global simulation and experimental results considering the delay compensation added by the cable length.

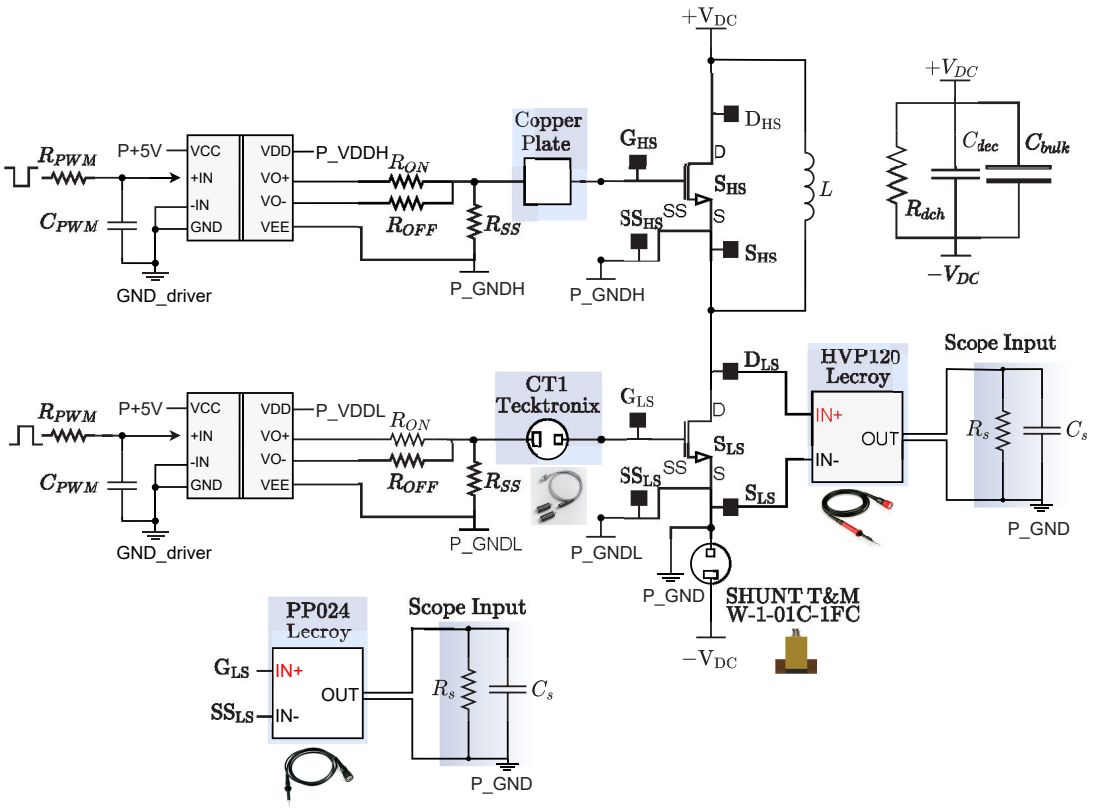


Figure 5.1: Schematic showing all measurement instruments used for the tests. Parameters: GaN Systems GS66516B – R_{ON},R_{OFF},R_{SS}: $(10, 5, 10\text{k})\ \Omega$ and V_{GS}: $(+5, -3)$ V.

As shown in Figure 5.3(a), the drain source voltage (V_{DS}) without the probe model has a lower fall time. Moreover, after adding the model, the waveform of the voltage presents a better correlation. During the turning-OFF, by analyzing the simulation, the resonance frequency is higher when the voltage probe model is not used. If the probe models are used in the simulation, the equivalent parallel capacitance on the switch is higher therefore, the resonance frequency is lower at $(1/(2\pi\sqrt{LC}))$. Moreover, it is important to mention the presence of the shunt, which increases the power loop inductance. As seen in Figure 5.3(b), the oscillations seen in the experiment are not detected by simulation, probably due to the lack of some parasitic capacitors and common-mode current modeling. The effect of the shunt is seen in Figure 5.4(a). The simulation that includes the shunt model presents a higher current rise time as well as a higher peak value, which becomes it closer to the values measured. In Figure 5.4(b), the simulation of the current transformer CT1 can be seen. It is noticeable that the resonate effect generated by the current transformer is mainly related to the parasitic effect presents at the windings. For the experimental results, the oscillations on gate current are more evident however, an explanation was not found for this situation. In Table 5.1, the description of the variables and curves obtained during the tests is presented. The waveforms of experimental results are fitted with simulation for comparison effects. The influence of the measurement instruments on the switching waveforms is more than an added gain and delay. Some perturbations linked to the parasitic elements are also apparent. All these disturbances influence the estimation of the energy losses during the transient time.

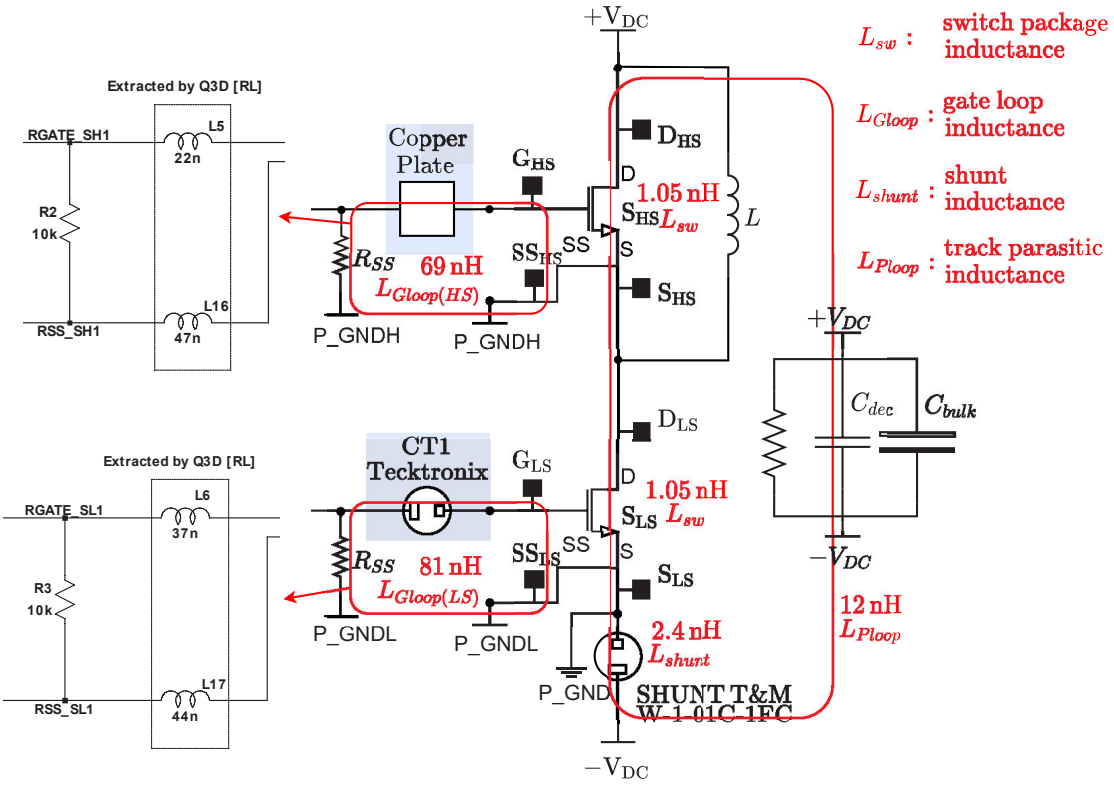
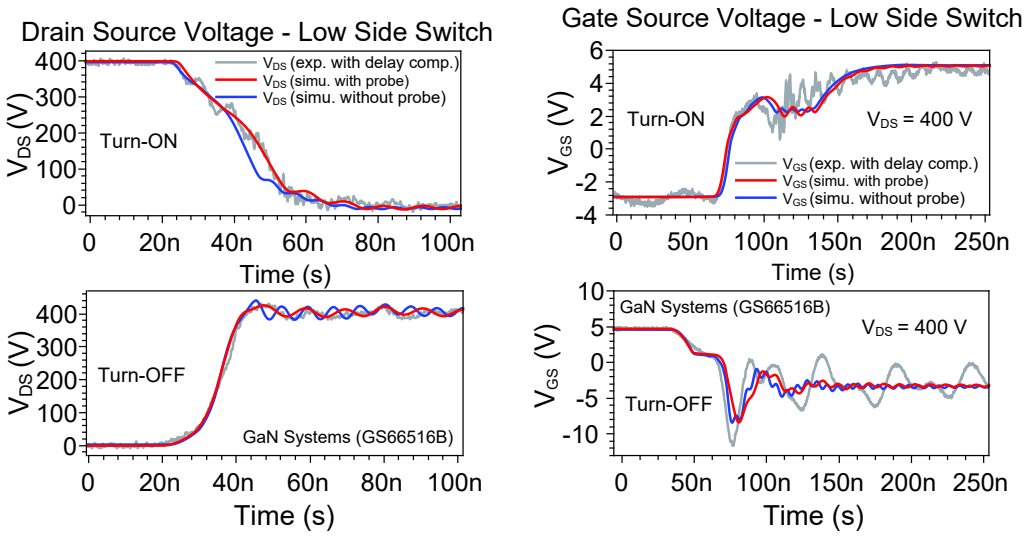


Figure 5.2: Schematic showing the main inductance of the circuit board: gate and power loop, GaN package, and the shunt insertion. ESL (Equivalent Series Inductance) of the ceramic capacitor (C_{dec}) is negligible.

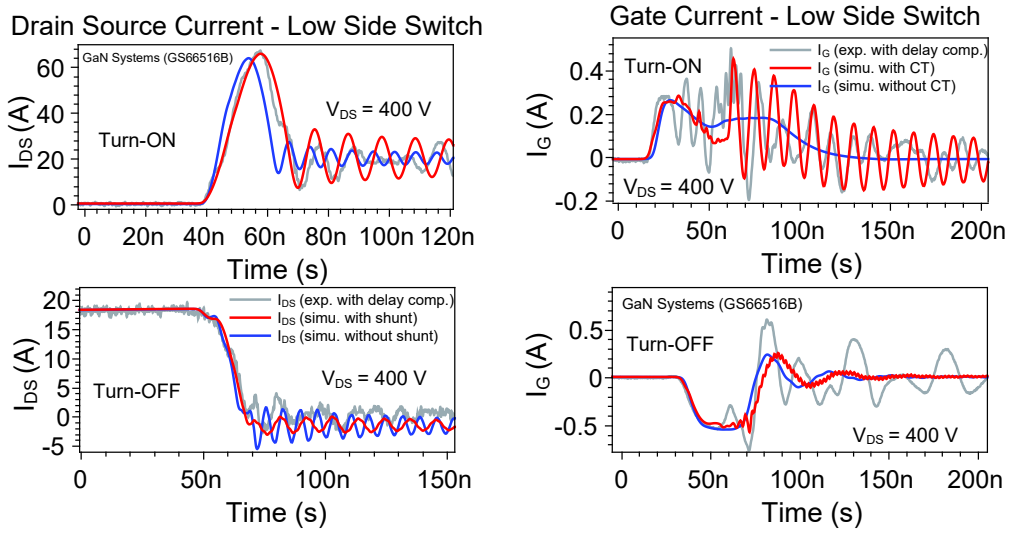
The drain source and gate voltage comparison of the global simulation with experimental results are also performed for other operation points, as seen in Figure 5.5 and Figure 5.6. At 100 and 300 V, the oscillations are highlighted with the simulation, and this could be related to issues with the device model accuracy or simulation parameters. The drain and gate currents are presented in Figure 5.7 and Figure 5.8. By analyzing the results for other applied voltages, it is clear that the turn-ON presents a better correlation with the simulation than turn-OFF. This could be related to the absence of parasitic capacitance in the simulation. Regardless, the turn-ON losses dominate the total switching losses, thus, finally, the added error from turn-OFF losses computation could be neglected.

The gate voltage of the high side switch was also measured using a differential ISOVU probe TIVH08/TIVH08L. Furthermore, a comparison between the experimental results obtained from the HVP120 and the ISOVU probes for



(a) (b)

Figure 5.3: (a) Drain source voltage comparison (probe used: HVP120 Teledyne Lecroy) and (b) gate source voltage comparison (probe used: PP024 Teledyne Lecroy) for GaN Systems devices (GS66516B).



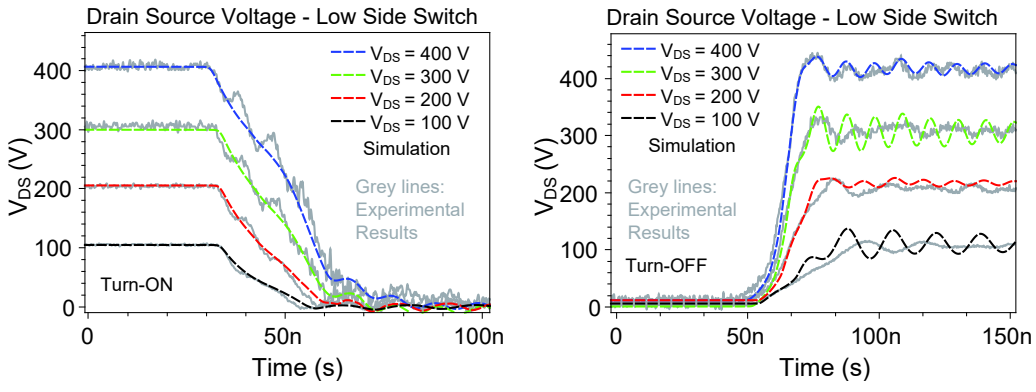
(a) (b)

Figure 5.4: (a) Drain current comparison (shunt used: W-1-01C-1FC TandM) and (b) gate current comparison for GaN Systems devices (GS66516B). Transformer used: CT1 Tektronix.

Table 5.1: Description of the variables and curves contained in Figure 5.3 and Figure 5.4. All measurement instruments are presented in Table 4.1.

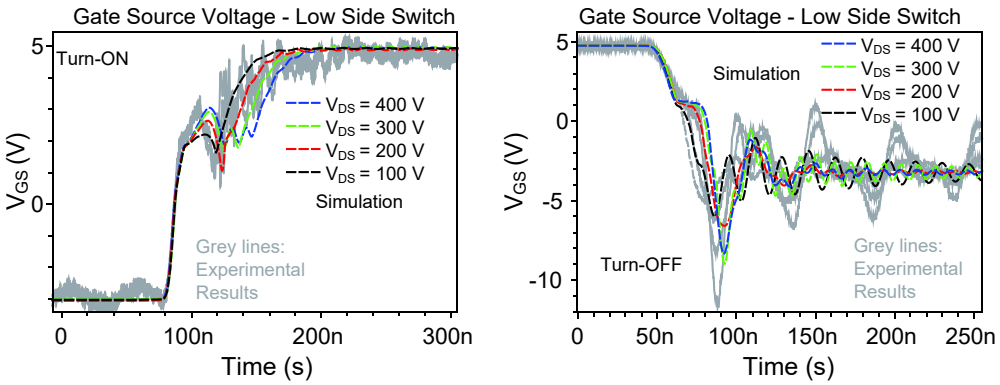
Variable	Legend Color	Definition	Description
V_{DS} (V)	Grey	Drain source Voltage	Experimental results. Probe delay compensation is performed for signal synchronization.
	Red		Simulation considering the HVP120, shunt, and other probe models.
	Blue		Simulation without measurement instrument models.
V_{GS} (V)	Grey	Gate source voltage	Experimental results. Probe delay compensation is performed for signal synchronization.
	Red		Simulation considering the PP024, shunt, and other probe models.
	Blue		Simulation without measurement instrument models.
I_{DS} (A)	Grey	Drain source current	Experimental results. Probe delay compensation is performed for signal synchronization.
	Red		Simulation considering the T&M shunt model and other probe models.
	Blue		Simulation without measurement instrument models.
I_G (A)	Grey	Gate current	Experimental results. Probe delay compensation is performed for signal synchronization.
	Red		Simulation considering the CT model, shunt, and other probe models.
	Blue		Simulation without measurement instrument models.

the drain source and gate voltages is presented. All curves are included in Section D.1. A very good fitting is found except for the following operation points: 100 and 300 V.



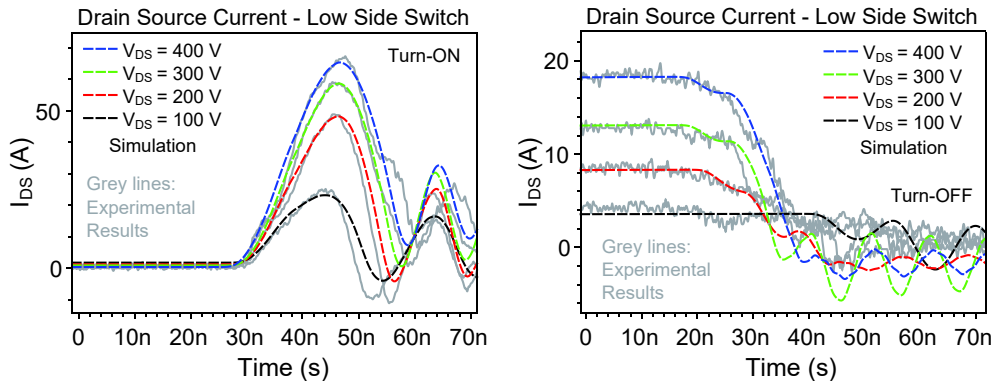
(a) (b)

Figure 5.5: (a) Turn-ON and (B) turn-OFF drain source voltage comparison with experimental values for GaN Systems devices (GS66516B).



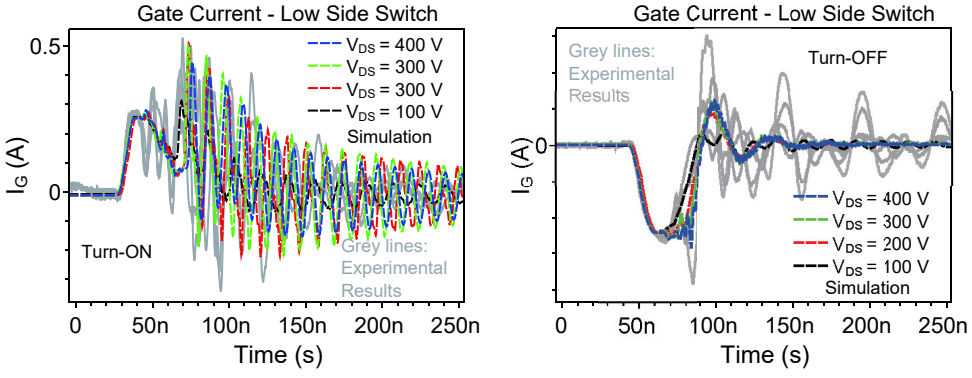
(a) (b)

Figure 5.6: (a) Turn-ON and (B) turn-OFF gate source voltage comparison with experimental values for GaN Systems devices (GS66516B).



(a) (b)

Figure 5.7: (a) Turn-ON and (B) turn-OFF drain current comparison with experimental values for GaN Systems devices (GS66516B).



(a) (b)

Figure 5.8: (a) Turn-ON and (B) turn-OFF gate current comparison with experimental values for GaN Systems devices (GS66516B).

5.2 Loss Estimation Based on a Validated Model

The development of a method that allows the estimation of switching losses is important for the design of converters. Additionally, due to the fast switching, the effect of circuit parasitic elements is extremely important. For this reason, a good method used by converter designers is to analyze, by using simulations, the device switching behavior under the influence of circuit parasitic elements before performing the physical circuit. This is especially helpful because it allows for the adjustment of circuit layouts or comparison of different layouts based on the simulation results [50].

To evaluate the switching losses in hard switching mode, the high side GaN switch is driven by a negative voltage (−3 V), thus behaving like a diode, with also a capacitive current through C_{DS}. The turn-ON period starts with the charging time of the input capacitance (C_{ISS}). Once the V_{GS} reaches the threshold voltage, the low side switch can begin to conduct current. This phase is finished when the drain current reaches the steady value for the inductor current. Just after, the drain-source voltage starts decreasing (period of voltage plateau) for as long as the Miller capacitance (C_{RSS}) is discharged. In addition, it is important to point out that there are parasitic effects that directly influence the oscillations detected during switching [5, 42].

During the turning-ON of a hard-switching, the effective current through the low side switch is a result of the sum of parasitic currents and the charge inductor current, as seen in Figure 5.9(a), causing a spike current effect. The energy associated with the output capacitance of both switches (C_{OSS}) and (C_{qOSS}) is discharged towards the 2DEG channel of the low side switch. Furthermore, the PCB parasitic capacitance (C_{pcb}) and the intrinsic capacitance associated with the inductor (C_{pl}) should be considered. Both elements generate high-frequency currents towards the low side switch and are voltage-dependent. Meanwhile, for turning-OFF, the drain current is equal to the load current minus the currents related to the parasite capacitance values, as seen in Figure 5.9(b) [50].

The GaN GS66516b SPICE model developed by GaN Systems is based on mea-

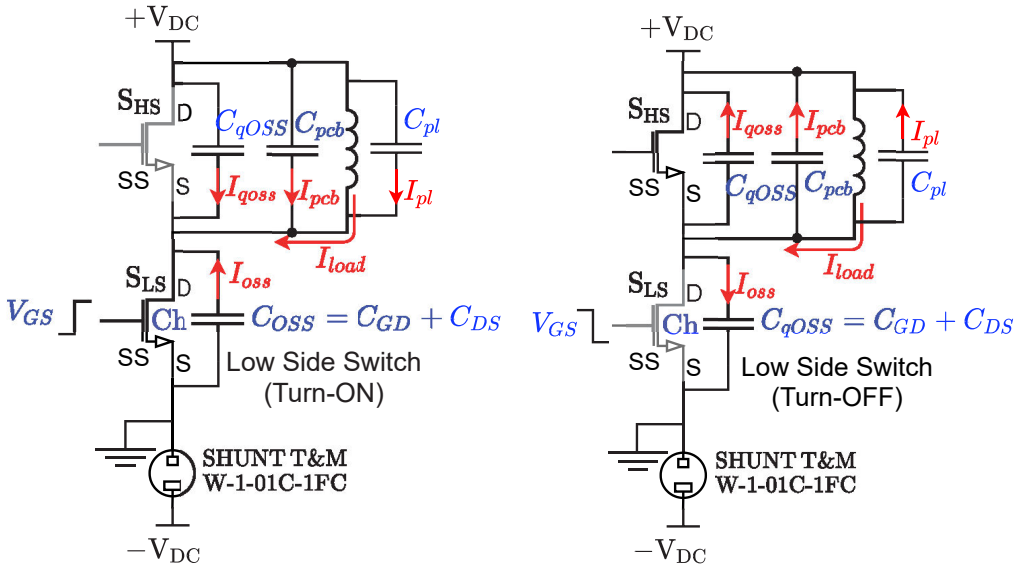


Figure 5.9: (a) Current distribution during turning-ON (low side switch). (b) Current on low side switch while turning-OFF.

sured characteristics. The functional block diagram presented in Figure 5.10 is developed based on the nonlinear electrical model of a power MOSFET and the SPICE code of the GaN power device. The diagram consists of input resistance (R_D, R_G and R_S) for each terminal; capacitance values associated with the different layers of the power device; intern resistors of the channel (R_{drain2} and $R_{source2}$); and a behavior voltage representing the 2DEG channel ($bswitch$).

However, the traditional method - voltage times current - at the terminal switch could generate spurious values due to the intern capacitive elements of the power device. Thus, by using the schematic presented in Figure 5.10, only the dissipative elements, heating sources such as resistors, and the channel (non-linear resistance), should be used for switching loss estimation. In the LTspice simulator, the options to save subcircuit node voltages and device currents must be enabled. By calculating the product of V-I directly for each resistance of the diagram and the behavior voltage source, the final value of switching loss is achieved. In Figure 5.11, the comparison between the traditional method, V-I product, and the computation using only dissipative

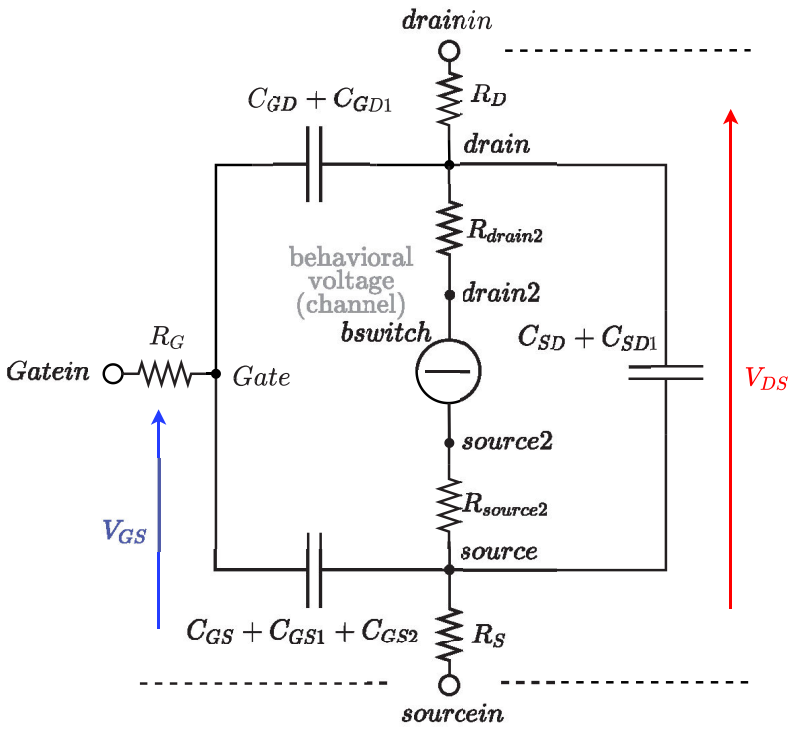
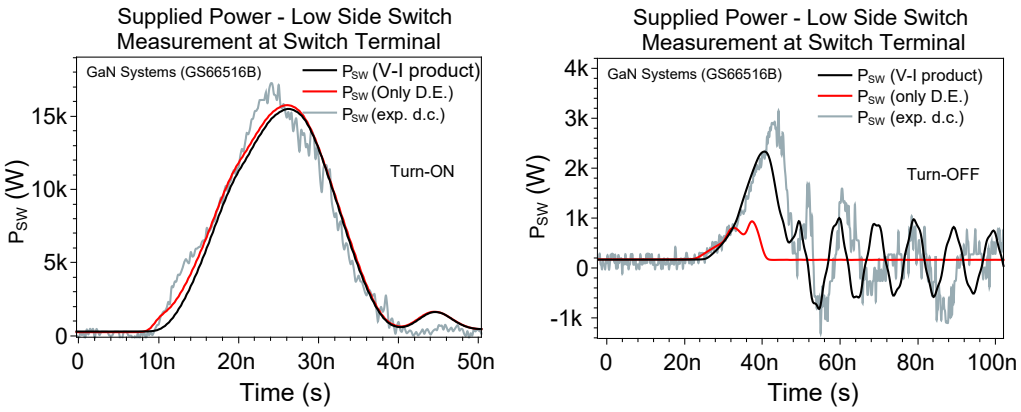


Figure 5.10: Nonlinear electrical model of a GaN HEMT for switching loss estimation adapted from [39].

elements can be seen. The difference is more evident for the turn-OFF period due to the oscillation associated with the resonance between capacitance and parasitic inductance.

The switching loss and the supplied energy present different values for fast switching devices. According to the first law of thermodynamics, the energy variation in a system is equal to the sum of the input power minus the losses. More specifically, in a cycle, as for a DC-DC converter in a steady state, the supplied energy is equal to the losses. Thus, to fix this error source, the switching loss estimation is performed by the sum of turn-ON and turn-OFF energies in a cycle during a switching characterization test. The sum result of turn-ON and turn-OFF energies is nearly the same, with a maximum error percentage about of 0.86 %, which confirms the approaching performed. In Table 5.2 the comparison between the two methods presented can be seen.

The loss estimation is performed using three different simulations. The first is a simple simulation, which included a switch SPICE model (GS66516B), driver



(a) (b)

Figure 5.11: Power supplied by the Low Side Switch (S_{LS}) obtained from the V-I product and by considering only the dissipative elements (D.E.) on switch model simulation. For this case, the losses are always positive. The experimental data is presented with delay compensation (d.c.).

Table 5.2: Comparison between switching loss estimation methods evaluated in this thesis. The simulation performed considers the measurement instrument models and the parasitic elements ($m_i + PE$).

Operation Points (V|A)	Turn-ON (μJ) Simulation		Turn-OFF (μJ) Simulation		Sum: Turn-(ON+OFF) (μJ) Simulation	
	V-I Product	Only Dissipative Elements	V-I Product	Only Dissipative Elements	V-I Product	Only Dissipative Elements
100 | 4.3	9.4	12.1	3.2	0.1	12.6	12.2
200 | 8.5	50.8	57.5	6.8	0.2	57.6	57.7
300 | 12.6	123.8	134.1	14.0	2.0	137.8	136.1
400 | 18.3	243.9	259.0	24.7	7.3	268.6	266.3

circuit, power loop inductance ($L_{Ploop} < 0.1\,\text{nH}$, thus a negligible value), and the equivalent circuit (RLC) for the load inductor. The ESL of the capacitor is also added to the capacitor models. For the second simulation, the measurement instrument models (voltage probe, shunt, and current transformer) are considered to add the delay effect from the cable length and disturbances associated to the impedance insertion. Also, the gate loop parasitic inductance (L_{Gloop}), extracted by ANSYS Q3D, is added to the simulation, and the power loop inductance obtained from measurement is adopted thus, $L_{Ploop} = 12\,\text{nH}$. In this case, the simulation corresponds to the schematic showed in Figure 5.2. Last, a simulation is performed by adding the full matrix from ANSYS Q3D (RLC) coupled with the electrical circuit of the instrumented PCB, including

the probe models. A brief description of the simulations is shown in Table 5.3.

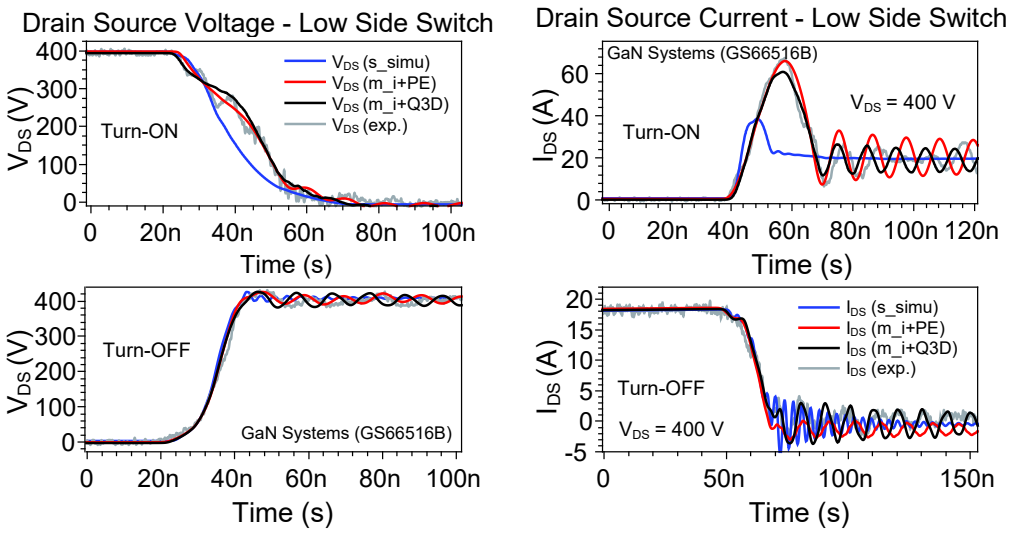
Table 5.3: Description of the simulations performed for comparison with the experimental results.

Legend	Definition	Description
s_simu	Simple simulation	Simple simulation without the measurement Instrument models and extracted parasitic elements.
m_i+PE	Measurement instruments + parasitic elements	Simulation with the measurement Instrument models and parasitic elements: Gate and total power loop inductance.
m_i+Q3D	Q3D matrix	Simulation considering the parasitic elements Full matrix extracted from Q3D.
exp.	Experimental	Experimental results. As seen on oscilloscope.
exp. d.c.	Experimental w/ delay comp.	Experimental results. Delay compensation is performed for signal synchronization.

The parasitic elements of the passive and active devices and geometry of the PCB layout determine the total power loop inductance on the circuit. In addition, it is important to highlight that there are parasitic effects that directly influence the oscillations detected during the switching time [91]. The parasitic elements introduced by the test board and measurement instruments can overshadow the device behavior and lead to erroneous measurements.

In Figure 5.12, the comparison between the performed simulations and the experimental data can be seen. Based on these results, it is clear that the simulation, which includes the power and gate loop inductance extracted by ANSYS Q3D, can be used to calculate the switching losses. The modeling of parasitic elements and measurement instruments allows us to achieve a good correlation between simulation and experimental results. However, some issues regarding the Q3D simulation must be noted: the large amount of time taken for processing in the simulator, the need for an accurate 3D model for parasitic extraction, and convergence errors from the interaction between the electrical SPICE models (transmission line and power device), and the RLC Q3D matrix at the computing instant.

Moreover, the power supplied to the power device is calculated using the V-I product at the scope input terminal, namely using the measurement instrument models (see Figure 5.1). The results can be seen in Figure 5.13(a) and Figure 5.13(b) for turn-ON and turn-OFF states, respectively. Both simulations, ($m_i + PE$ and $m_i + Q3D$), present good correlation with the experimental data. However, the delay added by the cable length becomes an error



(a) (b)

Figure 5.12: (a) Drain source voltage comparison for simulation and experimental results. (b) Drain-source current comparison for simulation and experimental results.

source for power estimation. Therefore, a measurement is also performed directly at the switch terminal by using only the dissipative elements of the power device model, as can be seen in Figure 5.13(c) and Figure 5.13(d). The width of the switching power triangle increases with the power loop inductance. Moreover, the width and height of the switching power triangle also increase with the gate loop inductance of the high side switch. In this context, the delay added by the cable length of the measurement instruments and the disturbances found on the shape of the drain source voltage are also strong elements that contribute to good switching loss estimation.

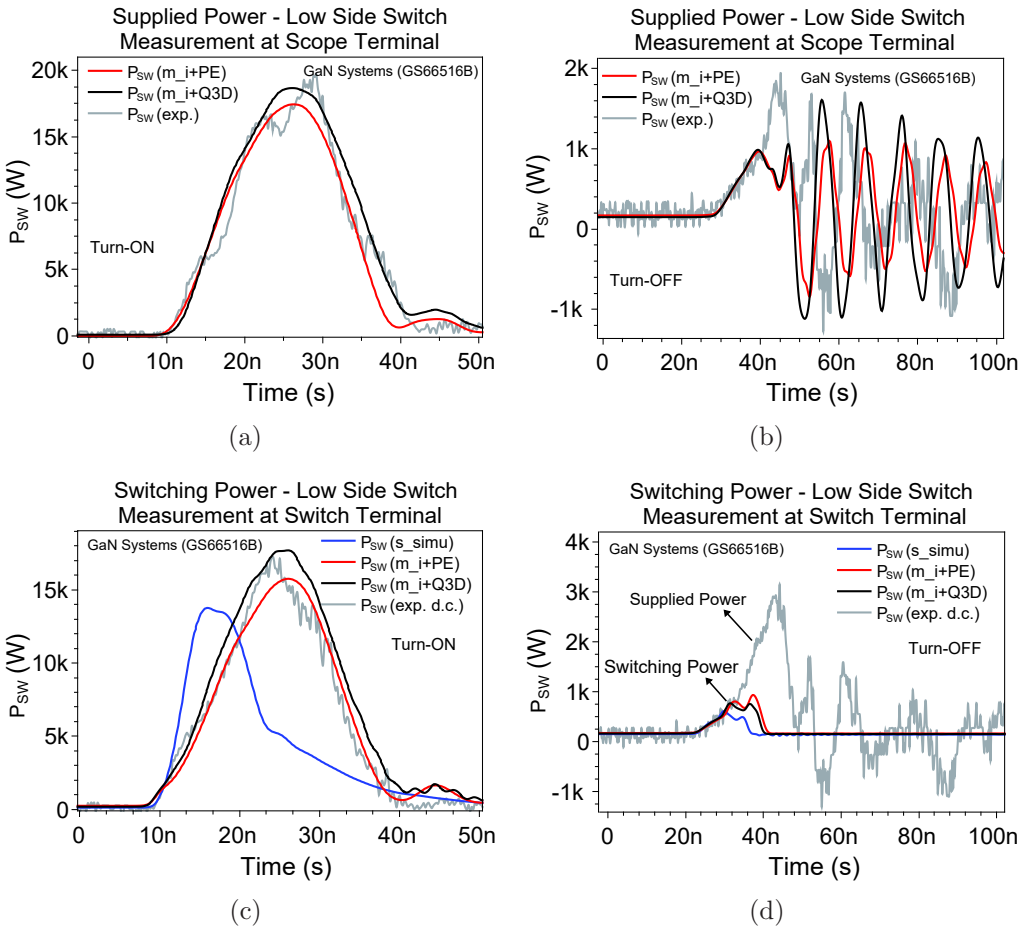


Figure 5.13: (a) and (b) Power supplied by the Low Side Switch (S_{LS}) obtained from the V-I product at the scope terminal, seen in Figure 5.1. (c) and (d) Switching power calculated by considering only dissipative elements on the switch simulation model and the experimental data with delay compensation.

The difference between each delay added by the shunt and voltage probes defines the delay compensation. Meanwhile, the propagation speed of traveling waves through the transmission line is defined by a function of the cable inductance and capacitance, and can be deduced from the Telegrapher's equations. More details are presented in Section C.1. Where L_L and C_L represent the inductance and capacitance of the cable. After calculating the propagation speed and knowing the cable length l and its wavelength λ, the added delay due to the probe can be estimated by using Equation (C.2). Initially, by using Equation (C.2), the propagation time is calculated and applied in the SPICE model of the measurement instrument.

$$u = \frac{1}{\sqrt{L_L C_L}} \text{ and } \lambda = uT \Rightarrow \tau = l\sqrt{L_L C_L} \tag{5.1}$$

For the GaN evaluation board, the delay compensation is equal to 4.75 ns, due to the signal delay difference of the HVP120 voltage probe and W-1-01C-1FC shunt. This calculation is performed by subtracting the delay from the voltage probe of the shunt.

Next, the switching energy calculation is estimated using the signals from the switch terminal and the scope circuit, in order to compare the effect caused by the measurement instruments. For the experimental results, a new column (Delay Comp.) is calculated by shifting the voltage signal at 4 ns towards the left of the time axis, thus implementing an advance on the signal. This value corresponds to the delay between voltage and current waveforms read directly on the oscilloscope.

Some switching energy values are shown in Table 5.4 and Table 5.5 for the turn-ON and turn-OFF periods, respectively, for different operation points. The columns -Probe Models- and -Simple Simulation- indicate simulations where a negligible power loop inductance ($L_{Ploop} < 0.1$ nH) is defined. For the column -Adding L_{Ploop} and L_{Gloop}-, the measured/simulated values for power and gate loop inductance are used, as seen in Figure 5.2.

Table 5.4: Switching energy of GS66516B for the turn-ON period.

Operation Points (V | A)	Turn-ON (μJ)								
	Simple Simulation	Probe Models		Adding L_{Ploop} and L_{Gloop}		With full Q3D		Experimental	
		Switch	Scope	Switch	Scope	Switch	Scope	Delay Comp.	Scope
100 | 4.3	10.9	10.6	12.1	12.1	15.2	13.9	17.1	10.1	15.2
200 | 8.5	41.3	42.3	49.8	57.5	73.1	67.4	82.6	51.6	71.6
300 | 12.6	88.7	98.3	113.8	134.1	165.5	163.0	189.2	136.5	171.8
400 | 18.3	161.2	172.4	209.3	259.0	305.6	288.5	322.4	261.8	314.7

Table 5.5: Switching energy of GS66516B for the turn-OFF period.

Operation Points (V | A)	Turn-OFF (μJ)								
	Simple Simulation	Probe Models		Adding L_{Ploop} and L_{Gloop}		With full Q3D		Experimental	
		Switch	Scope	Switch	Scope	Switch	Scope	Delay Comp.	Scope
100 | 4.3	0.2	0.1	1.9	0.1	2.0	0.1	1.8	7.47	4.5
200 | 8.5	0.8	0.2	2.6	0.2	3.0	0.2	3.2	13.3	9.5
300 | 12.6	1.1	1.6	4.4	2.0	5.5	1.6	5.7	20.2	11.8
400 | 18.3	3.8	6.0	7.7	7.3	8.3	6.4	10.8	36.8	19.9

The switching energy values obtained from simulation moved closer to experimental data when the extracted gate and loop inductance are included. For the column -Switch-, the computation is performed using only the dissipative elements of the power device model, and the reading is performed at the switch terminals (drain and source), as previously mentioned. The columns -Scope- present the energies from the V-I product. In Table 5.4, the switching energies for both simulations, (m_i + PE) and (m_i + Q3D), show coherent values with the experimental data. The turn-OFF switching energies, as shown in Table 5.5, has considerable discrepancies with experimental values. It is also important to highlight that as the experimental computation for switching energy is performed by means of the V-I product, the charge of C_{OSS} is also included in the experimental switching OFF energy. Further, the oscillations present during turn-OFF and the absence of some parasitic elements could generate some additional erroneous values. Moreover, the common mode current and the coupling between the driver and power circuits could explain this difference in the values, given that their modeling is not shown.

The turn-ON energy dominates the total energy thus, the errors related to the turn-OFF energy have a low impact on the total switching loss estimation. In Table 5.6, the total switching energy is presented to eliminate the issues related to the V-I product applied on the experimental results and the -Scope- column.

Table 5.6: Total switching energy of GS66516B.

Operation Points (V | A)	Turn-ON (μJ)+Turn-OFF (μJ)								
	Simple Simulation	Probe Models		Adding L_{Ploop} and L_{Gloop}		With full Q3D		Experimental	
		Switch	Scope	Switch	Scope	Switch	Scope	Delay Comp.	Scope
100 | 4.3	11.1	10.7	14.0	12.2	17.2	14.0	18.9	17.5	19.7
200 | 8.5	42.1	42.5	51.7	57.7	76.1	67.6	85.8	64.9	81.1
300 | 12.6	89.8	99.9	118.2	136.1	171.0	164.6	194.9	156.7	183.6
400 | 18.3	165.0	178.4	217.0	266.3	313.9	294.9	333.2	298.6	334.6

The simulation (m_i + PE) presents a maximum error percentage of about 13 % at 100 V, and a minimum error percentage of about 6 % at 400 V. For the simulation (m_i + Q3D), a maximum error percentage of about 4 % at 100 V, and a minimum error percentage of about 1 % at 400 V. These values evidence the need for a good parasitic estimation and measurement instruments modeling for an accurate switching loss estimation.

5.3 SiC and GaN Devices for Automotive Application

To compare these power devices, the switching characterization is performed for model validation. Afterwards, a simulation considering the same power and gate loop inductance is performed for each device, which allowed for the evaluation of the switching performance under equal conditions. A FOM based on static ON resistance and switching losses is used as the main comparison element [7]. With the validated models, it is possible to develop a DC-DC converter simulation for each power device and compare their performance for an automotive application at 200-400 V for different charge levels [6, 50, 118, 124]. The comparative analysis of the devices in a DC-DC operation is performed by focusing on the switching FOM.

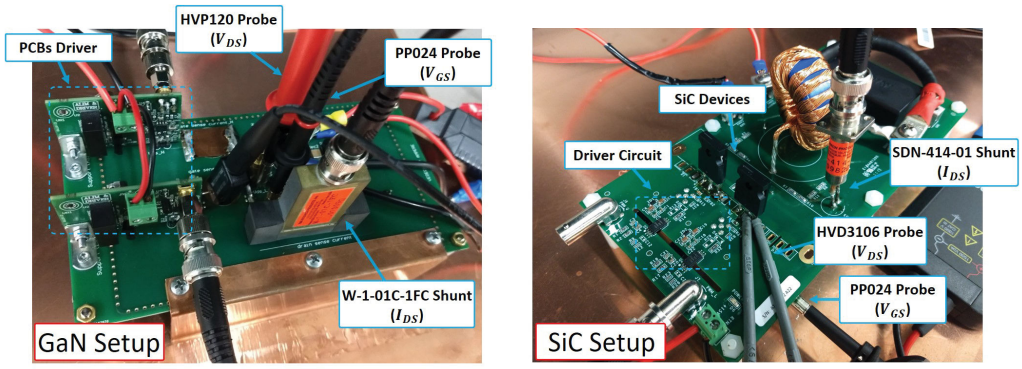
5.3.1 Switching Characterization for Model Validation

Switching behavior is analyzed by a DPT setup, as can be seen in Figure 5.14. The devices chosen with nominal voltage of 650 V are presented in Table 5.7. Moreover, an instrumented PCB is built for the GaN dynamic tests, given that the impact of parasitic elements is relevant for this technology. For the SiC components, an evaluation board from CREE is used. The waveforms of voltage, current, and power switching losses are compared during a DPT for the different operating points.

Table 5.7: Selected power semiconductor devices with typical properties.

Component	Material	Type	Vnom (V)	Inom (A)	Rdson ($m\Omega$)	Driver	Ron; Roff (Ω)
GS66516T	GaN	eHEMT	650	60	25	Si8271 @-3/+6	10; 1
SCT3030AW7	SiC	Mosfet	650	70	30	Si8261 @-3/+18	4; 0
C3M0060065K	SiC	Mosfet	650	30	60	Si8261 @-3/+18	4; 0

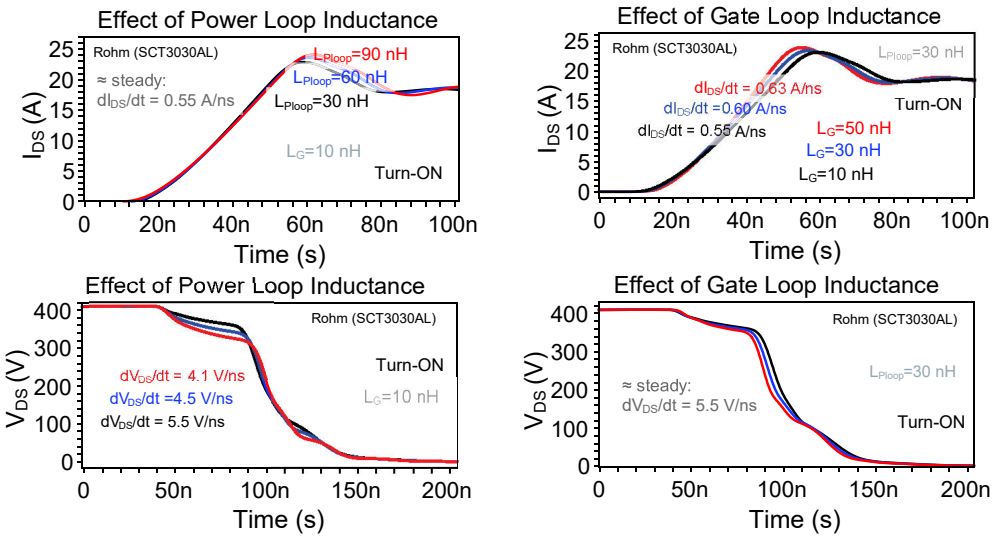
To validate the simulation models, a comparison of voltage and current waveforms is undertaken. In this study, two main elements are used to achieve a good correlation between simulation and experimental results: the effect of the gate and power loop inductance. For the GaN simulation, the drain current slope is fitted with the experimental test by means of the power loop inductance value. Afterwards, by considering the drain current peak reference, the



(a) (b)

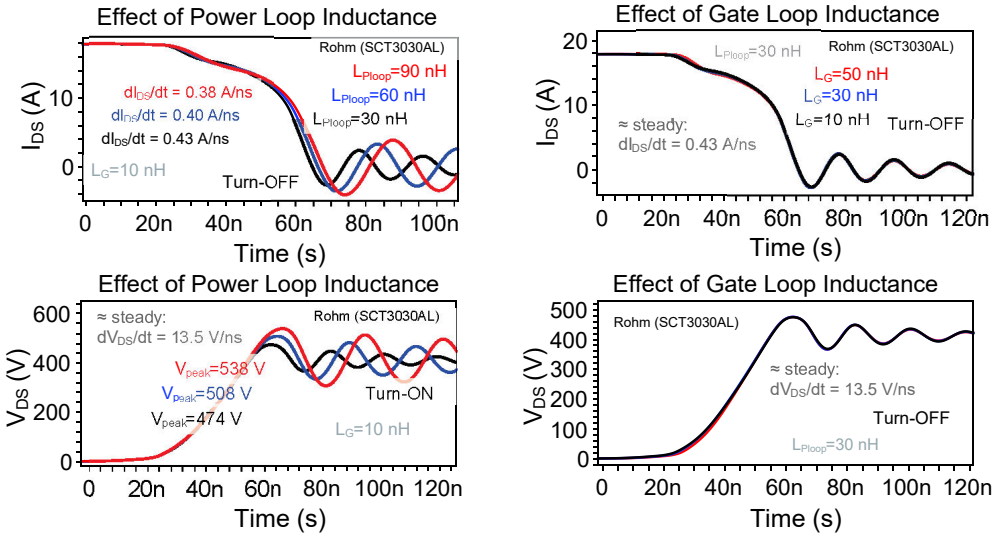
Figure 5.14: (a) Instrumented PCB developed for switching characterization of GaN components. (b) Evaluation board KIT-CRD-3DD12P adapted for SiC components.

gate inductance is adjusted. The simulation results were previously discussed in Section 4.3. For the SiC simulation, the effect of power loop inductance variation on current slope is less pronounced therefore, the gate inductance is initially modified, after which the power inductance is adjusted. The circuit test topology used for SiC and GaN validation follows the same concept (one-leg inverter), but the PCB used for the SiC devices has not an optimized design since it comes with an evaluation test board. Hence, to perform the simulation comparison, the power and gate loop inductance are defined as same values (Section 5.3.2). The simulation results can be seen in Figure 5.15 and Figure 5.16, for the turn-ON and turn-OFF states, respectively. The current turning-ON regarding gate loop inductance changes presents more sensitivity than the turn-OFF transient. Thus, the synchronization with the experimental values is started by the comparison of the current slope during turn-ON, defining the gate loop inductance in simulations. In this context, the power loop inductance is deduced by using the comparison of drain source voltage for the turn-OFF transient with the experimental data. The comparison between the performed simulations and the experimental data for switching of GaN and SiC devices can be seen in Figure 5.17.



(a) (b)

Figure 5.15: During turn-ON: (a) Effect of power loop inductance on current/voltage waveforms on the low side switch (S_{LS}). (b) The same analysis was undertaken for the gate loop inductance variation.



(a) (b)

Figure 5.16: During turn-OFF: (a) Effect of power loop inductance on current/voltage waveforms on low side switch (S_{LS}). (b) The same analysis was undertaken for the gate loop inductance variation.

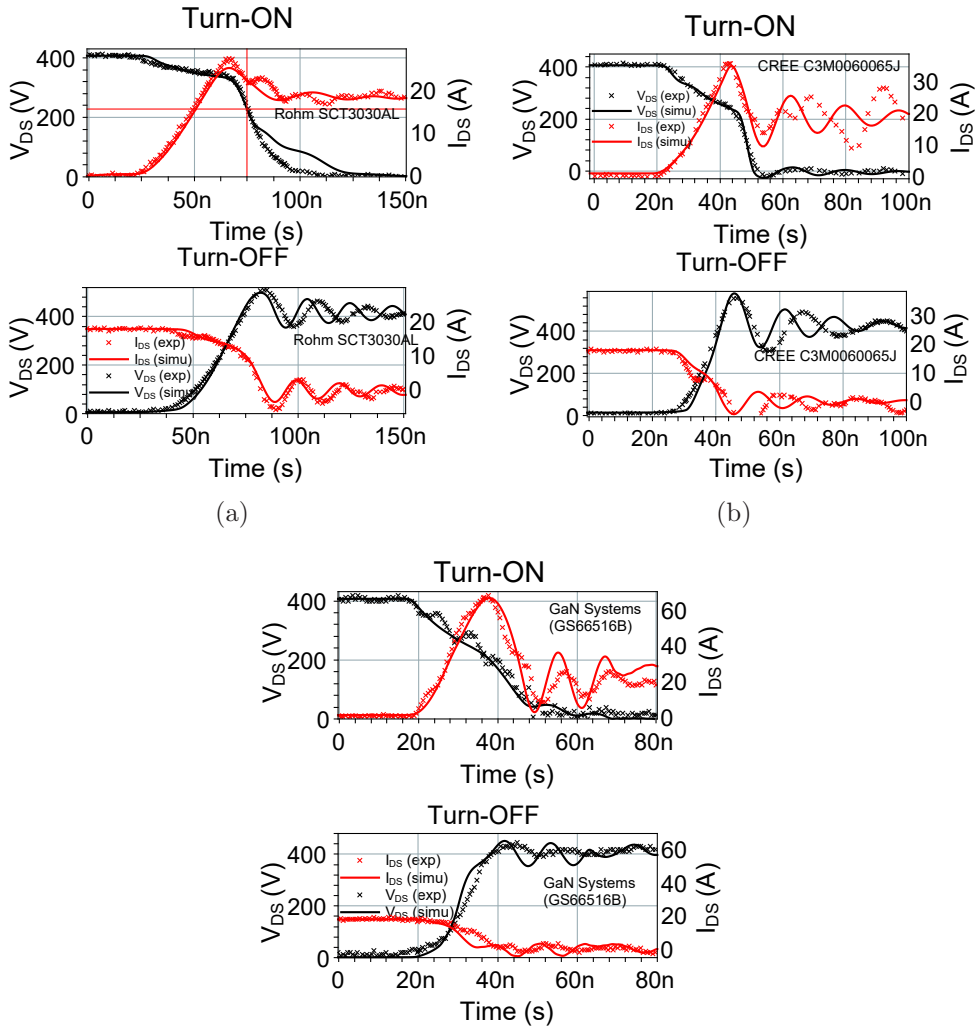


Figure 5.17: Switching behaviour comparison for (a) SCT3030AL (Rohm), (b) C3M0060065K (CREE), and (c) GS66516B (GaN Systems).

Moreover, the loss estimation is performed using a simulation that considers the switch SPICE model, driver circuit, power and gate loop inductance (L_{Ploop}, L_{Gloop}), and the electrical circuits of the measurement instruments (voltage probe and shunt). In this case, the total power loop inductance is estimated by the sum of the inductance values associated with the PCB tracks, switch package, and shunt. The ESL is not considered in the simulation for the power loop inductance sum, given that low ESL coupling capacitors are used in parallel with the GaN-based switches. For the SiC-based evaluation

board, the power loop inductance estimation is undertaken considering the total inductance of the power loop.

The difference between each delay added by the shunt and voltage probes defines the variable delay compensation. The propagation speed of traveling waves through the transmission line is defined by a function of the cable inductance and capacitance, and can be deduced from the Telegrapher's equations, as previously mentioned. For the GaN evaluation board, the delay compensation equal to 4.75 ns due to the signal delay differences between the HVP120 voltage probe and W-1-01C-1FC shunt. For the SiC evaluation board, this value is 8.9 ns due to the HVD3106 voltage differential probe and SDN-414-01 shunt. This calculation is performed by subtracting the delay from the voltage probe and shunt. In the experimental results, by reading the values on the oscilloscope and performing a signal synchronization that referenced the gate source voltage, the delays are approximately equal to 4 ns and 9.4 ns for the GaN and SiC evaluation boards, respectively.

Table 5.8 presents the switching loss values for the GaN device under different operation points. At 400 V, the error percentage between simulation and experimental data for total switching losses is about 6 %. In Table 5.9 and Table 5.10, the same results are presented for the SiC devices. The maximal error percentage for total switching loss estimation at 400 V is about 9 %, between the simulation and experimental results. The column -Switch- represents the signal read directly at the device, and the column -Scope- the variable is read after the measurement instrument model. The error differences between SiC and GaN can be attributed to the fact that GaN devices have more sensitivity to delay compensation, because of their faster switching speeds. Additionally, some high frequency disturbances did not considered could generate more impact on GaN components. In this context, given that the experimental and simulation results present a good correlation, it is reasonable to state that a good switching loss estimation can be achieved.

5.3.2 Switching Characteristic Comparison

The comparison between different power devices is commonly achieved by using different FOMs. In automotive DC-DC applications, a high frequency

Table 5.8: Switching loss energy of GS66516. Parameters: $L_{Ploop} = 16.5\,\text{nH}$ and $L_{GLoop} = 81\,\text{nH}$.

Operation Points (V|A)	Turn-ON (μJ)				Turn-OFF (μJ)			
	Simulation		Experimental		Simulation		Experimental	
	Switch	Scope	Delay Comp.	Scope	Switch	Scope	Delay Comp.	Scope
100 | 4.3	12.1	15.2	10.1	15.2	0.1	2.0	7.47	4.5
200 | 8.5	57.5	73.1	51.6	71.6	0.2	3.0	13.3	9.5
300 | 12.6	134.1	165.5	136.5	171.8	2.0	5.5	20.2	11.8
400 | 18.3	259.0	305.6	261.8	314.7	7.3	8.3	36.8	19.9

Table 5.9: Switching loss energy of SCT3030AL. Parameters: $L_{Ploop} = 58.5\,\text{nH}$ and $L_G = 30\,\text{nH}$.

Operation Points (V|A)	Turn-ON (μJ)				Turn-OFF (μJ)			
	Simulation		Experimental		Simulation		Experimental	
	Switch	Scope	Delay Comp.	Scope	Switch	Scope	Delay Comp.	Scope
100 | 3.6	8.9	12.9	11.7	16.2	2.9	1.1	2.6	1.2
200 | 7.5	45.7	61.7	53.2	70.2	11.2	3.6	13.0	4.5
300 | 12.8	131.8	172.1	141.7	181.8	40.4	16.8	42.3	19.8
400 | 17.5	282.7	357.2	296.3	375.4	96.5	44.5	101.5	54.3

Table 5.10: Switching loss energy of C3M0060065K. Parameters: $L_{Ploop} = 58.5\,\text{nH}$ and $L_G = 30\,\text{nH}$.

Operation Points (V|A)	Turn-ON (μJ)				Turn-OFF (μJ)			
	Simulation		Experimental		Simulation		Experimental	
	Switch	Scope	Delay Comp.	Scope	Switch	Scope	Delay Comp.	Scope
100 | 3.6	2.8	7.5	4.2	10.6	1.6	0.3	1.4	0.5
200 | 7.5	19.7	35.7	23.4	40.0	4.0	0.7	2.7	0.7
300 | 12.8	44.2	85.8	62.2	98.3	15.7	2.6	9.3	1.0
400 | 17.6	102.7	173.9	128.7	196.4	37.3	9.1	23.4	3.6

performance is suitable, given that the sizes of the passive components decrease proportionally. To compare the different switches in terms of switching losses, a simulation is performed by considering the same values for power loop ($L_{Ploop} = 6$ nH) and gate inductance ($L_{Gloop} = 10$ nH). This is possible due to the fact that each model was validated in static, dynamic, and switching characterization by means of experimental tests.

Further comparability is reached by adding a conduction loss term namely switching FOM thus, in this manner, the product between total switching energy and ON-resistance is plotted ($E_{total} \cdot R_{DS(on)}$) [7]. The results for different currents are shown in Figure 5.18. To study the thermal behavior with the aim of automotive applications, the switching losses and mentioned FOM are also plotted at 125 °C, by using the ON-resistance at this temperature provided from the dataset. Figure 5.18(a) and Figure 5.18(b) present the turn-ON and turn-OFF energies, respectively.

As expected, the switching losses increase with higher current levels. Figure 5.18(c) shows the lower total switching losses for the CREE device (C3M0060065K) at both the analyzed temperatures. This is related to this device having a lower nominal current compared to the other devices, and thus a lower charge is required for the switching process. In Figure 5.18(d), the effect of adding a conduction loss factor becomes evident in the better performance of the GaN HEMT device (GS66516) at 25 °C . This is associated with the fact that the GaN having a lower ON-resistance and a capacitance value proportionally lower than SiC devices. However, due to the strong temperature dependency of the ON-resistance presented by the GaN HEMT, its switching FOM significantly increase at 125 °C. If the power switch does not operate at high temperatures, the GaN device performed better than the SiC devices, as seen in Figure 5.18(d).

5.3.3 Automotive Application

The performance of power converters relies on the switching and conduction losses of power devices, given that lower power losses ensures maximum efficiency, high power density, and downsizing of the heat sink and cooling circuit [125]. Thus, the WBG devices are promising candidates for automotive applications. A typical DC-DC converter for an on-board charger can operate within a current range of 10-20 A, for a specification rated at 200-400 V for 3.6 kW. A boost converter simulation for each target device is performed under different frequencies and power levels. Thus, by considering the same conditions for parasitic elements, the more adaptable device to an operating point can be named.

In Figure 5.19 the synchronous boost converter is presented as well as the current waveforms during transient period that is referenced Q_{SW}. The turn-ON losses dominate the total losses because when the switch is turning-ON, the discharge current from the output capacitor (C_{dec}) goes through the switches. Furthermore, the voltage fall time (turn-ON) of the switch is higher than its voltage rise time (turn-OFF) [52]. As seen in Figure 5.19, during the turn-ON transient, the main switch (Q_{SW}) has higher losses than the complementary switch (Q_{sync}). This is related to the turn-OFF moment of (Q_{sync}). Moreover, the initial value of ($i_{Q_{sync}}$) is equal to the inductor current (i_L), and this

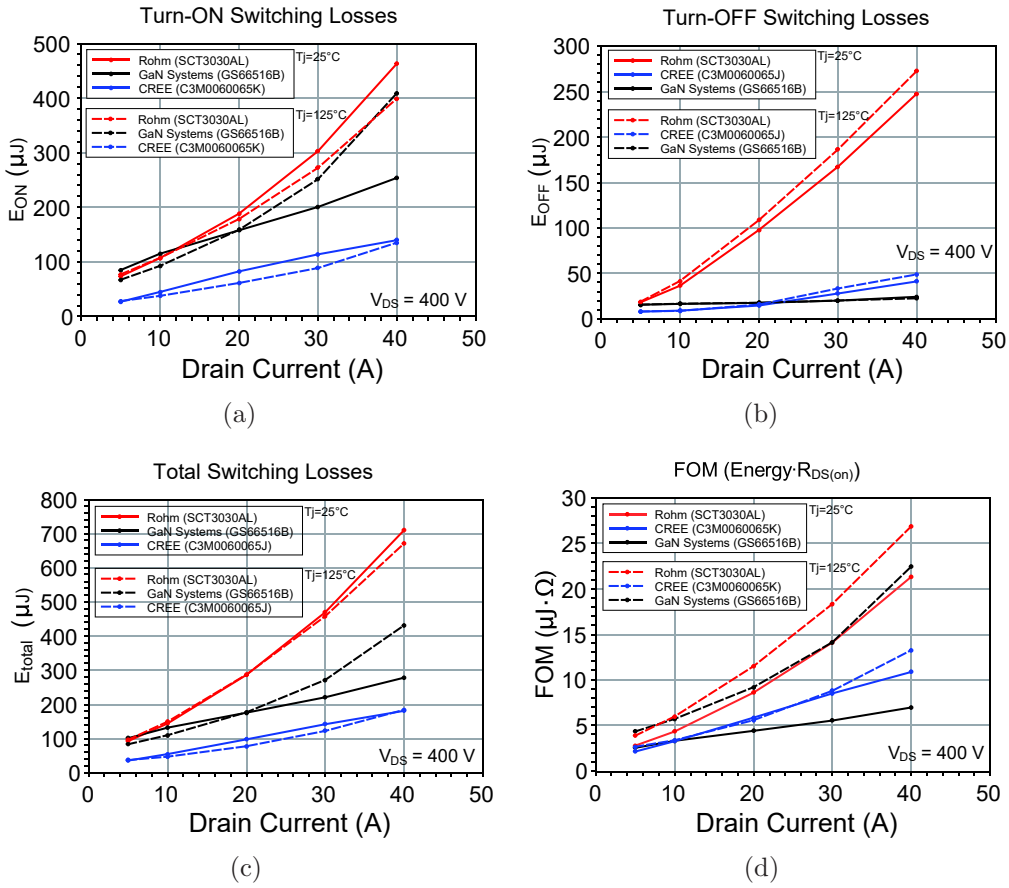


Figure 5.18: (a) The turn-ON, (b) turn-OFF, and (c) total switching losses. (d) Switching FOM (the lower the better) at different current levels. Simulation parameters: GaN Systems GS66516B – R_{ON},R_{OFF}: $(10, 1)$ Ω and V_{GS}: $(+6, -3)$ V; Rohm SCT3030AL – R_{ON},R_{OFF}: $(0, 0)$ Ω and V_{GS}: $(+18, -3)$ V; CREE C3M0060065K – R_{ON},R_{OFF}: $(2.5, 2.5)$ Ω and V_{GS}: $(+15, -4)$ V. These parameters were extracted from the datasheets.

current must load the output capacitance of the synchronous switch (Q_{sync}), which decreases the channel losses. The reverse conduction also has a more resistive path, hence current peaks less accentuated are achieved.

The total losses are estimated by a SPICE simulation. In Figure 5.20, the total power losses on switches can be seen. All simulations are performed at 25 °C and 125 °C as junction temperatures. At 100 kHz, for an input power up to 2.5 kW the SiC CREE presents lower losses, due to its faster switching capability. As the power increases, the ON-resistance for SiC CREE starts

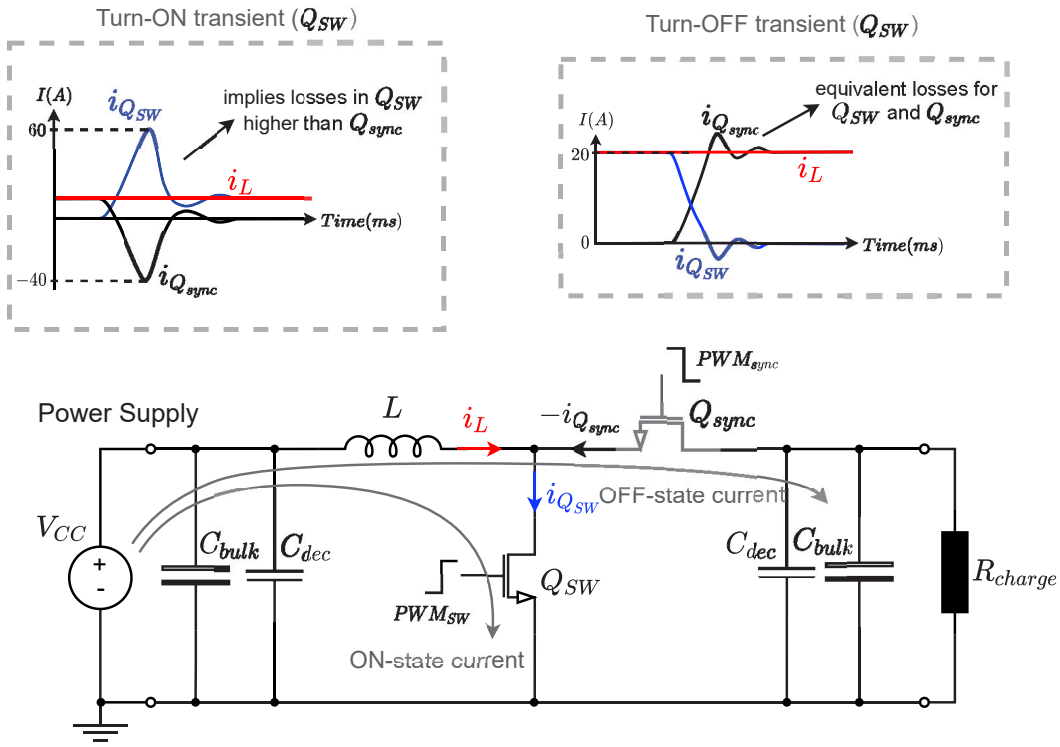
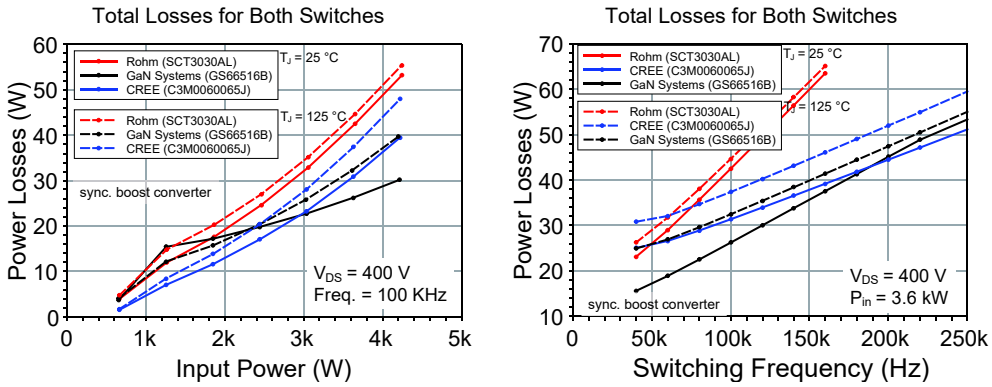


Figure 5.19: Boost converter in switching transient.

to increase and becomes increasingly pertinent in terms of total losses estimation. Thus, the GaN Systems device becomes the more efficient, given its inferior ON-resistance. Regarding the behavior at high temperature, all devices show higher losses. The GaN HEMT presents the more accentuated difference among devices, due to its strong temperature dependence, as previously discussed. Nevertheless, as shown in Figure 5.20(b), for a nominal power rated at 3.6 kW, the GaN-based boost converter exhibits the lower total losses in the considered switching frequency range.



(a) (b)

Figure 5.20: (a) Total power losses for Q_{SW} and Q_{sync} versus (a) input power and (b) switching frequency.

5.4 Conclusion and Perspectives

The comprehensive analysis of the impact of the wiring parasitic elements can improve the accuracy of switching loss estimation. Furthermore, by means of experimental results, the need for a good modeling of instrument measurements and a 3D Model for parasitic extraction was verified. In this context, a simulation considering the power and gate loop inductance values can yield a good match with experimental data. Further, this approach allows for the validation of all models used in SPICE simulations, and thus the more accurate evaluation of the overall efficiency of converters based on GaN components, including those that will not be instrumented.

Moreover, the methodology of turn-ON current synchronization allows a maximum error percentage for the total switching losses of about 13 % for GaN devices and 9 % for SiC devices. Regarding the total losses and the preliminary results, the comparison of switches showed that, for the considered switching frequency, the GaN HEMT device exhibits better performance for the 3.6 kW DC-DC proposed automotive application.

General Conclusions and Perspectives

Thesis Project

WBG device characterization is important to better understand their electrical characteristics in order to develop high efficiency power converters. This thesis was mainly focused on the static and dynamic characterization of SiC and GaN devices for automotive applications, namely DC-DC converters. Furthermore, the switching characteristics were also verified with SPICE model validation. Four different devices (SiC and GaN) were chosen with a nominal voltage about 400 V, which is a value commonly used for batteries in EV vehicles. The static and dynamic characteristics were performed using a Curve Tracer B1505A Keysight.

To further investigate the main elements that can contribute to the switching transients, an instrumented PCB for the GS66516B GaN Systems device was developed. The DPT was performed in order to obtain the current and voltage variables of the main switch. This PCB offered an interface to connect all the measurement instruments (voltage probes, shunt, and current transformer) needed for the device model validation. Moreover, the main parasitic elements were also analyzed by experimental (with an E4990A Impedance Analyzer) and simulation tests. Hence, the power/gate loop inductance was verified as fundamental elements to obtain an accurate simulation.

Next, the model validation for SiC devices was performed using an evaluation board from CREE. The main parasitic inductance was extracted using an estimation method that was examined using the instrumented PCB that was

previously developed. Here, the power/gate loop inductance was defined based on the match between simulation and experimental results.

The switching loss estimation using a validated model of GaN Systems device was performed. The measurement instrument models, wiring elements, and device SPICE models were considered for simulation. However, the traditional method that multiplies the voltage and current at the switch terminal, which is used for switching loss estimation, could generate spurious values due to the internal capacitive elements of the power device. Thus, a method considering only dissipative elements of the switch was implemented.

Moreover, the comparison between different power devices is commonly achieved by using different FOMs. To compare the different switches used in this thesis, a simulation is performed by considering the same values for power/gate loop inductance. Further comparability was reached by adding a conduction loss term namely, switching FOM. Thus, in this manner, the product between total switching energy and ON-resistance was plotted. Finally, a typical DC-DC converter was simulated for each target device under different frequencies and power levels.

Conclusions

The static and dynamic device characterization helped validate the SPICE models to use them in the switching mode. Thus, with some adjustments in the threshold voltage, switching loss estimation can be performed by using the manufacturer's available models. The ambient/high temperature measurements showed a good correlation with the simulations performed in LTspice. Here, the relation between ON-resistance and temperature for each technology demonstrated the strong temperature dependence of GaN devices.

Moreover, the comprehensive analysis of the impact of the wiring parasitic elements could improve the accuracy of switching loss estimation. Furthermore, by means of experimental results, the need for good measurement instrument modeling and a 3D Model for parasitic extraction was verified. In this context, a simulation considering the power/gate loop inductance could yield a good match with experimental data. This approach helped validate all the SPICE

models used in the simulations, and thus more accurately evaluate the overall efficiency of GaN-based power converters.

This study about the measurement instruments used for WBG devices helped understand the impact of each element on circuit loading. To this end, a clear protocol for measurement instrument modeling was presented. The fast-switching speed of GaN devices requires this modeling to achieve an accurate simulation. The comparison between datasheet, simulation, and experimental tests showed a good correlation in terms of input impedance characteristics. Therefore, the impedance seen by the circuit could be estimated in a global simulation. Furthermore, the frequency responses of the models were also simulated to compare them to the datasheet limits, by using a bandwidth quite close to the specification for the measurement instruments.

Based on the results, it is reasonable to use the simulation that includes the power/gate loop inductance extracted by ANSYS Q3D to calculate the switching losses. The modeling of parasitic elements and measurement instruments allowed for a good correlation between the simulation and experimental results. The fact of not using the full matrix from Q3D, helps to decrease the simulation time.

The methodology used for the turn-ON current, along with the matching between simulation and experimental results, resulted in a maximum error percentage for the total switching losses of about 13% for GaN devices and 9% for SiC devices. Regarding the total losses and the preliminary results, the comparison of switches showed that for the considered switching frequency, the GaN HEMT device exhibited better performance for the proposed 3.6 kW DC-DC automotive application.

Here, it is important to note that SiC and GaN will keep evolving and improving in the next generations, and thus no definitive conclusion can be definitively made regarding the SiC and GaN comparison for the 3.6 kW - 400 V hard switching non-isolated converter application.

Perspectives

The study performed in this thesis helps to better understand the main factors that should be considered to achieve an accurate switching loss estimation. Validated models based on the experimental results were used to perform simulations regarding power/gate loop inductance in equal conditions for all devices tested in this thesis. Thus, a comparative study focusing on an automotive application could be performed. The total losses in a typical DC-DC converter was then used as comparative parameters to analyze different performances of WBG devices.

Regarding static and dynamic characterization, the constant development of the technology of WBG devices requires that these tests are performed simultaneously at ambient and maximal junction temperatures. Different samples had to be used to increase the measurement reliability, but mainly for GaN devices, given their relative development in the initial phase. However a better integration of the reliability constraints should be included in the future to design reliable and efficient power converters.

For switching characterization, the ideal condition would be an instrumented PCB for each target device (SiC and GaN). Thus, a precise parasitic element modeling could be performed. The measurement instrument modeling had also be carefully performed. Here, it is important to note that frequency response tests with a VNA (Vector Network Analyzer) can improve the developed models.

Further, a test platform for switching characterization where two slots would be used, one for the power devices (one-leg, two switches) and another one for the driver circuit, can improve the comparative study among WBG devices. In this situation, the same current/voltage probes could be considered for measurements.

Regarding the DC-DC converter for automotive applications, a final prototype was developed for the GS66516B GaN Systems device to validate the switching loss estimation for an optimal and non-instrumented case. Based on a validated simulation, the total losses would be calculated and compared to measurement results. However, due to some issues and lack of time, the

manufacturing the converter was not possible within this thesis period.

Moreover, certain signal disturbances obtained by measurement were not identified by the modeling and simulation analysis. Thus, the analysis should probably be extended to integrate the common mode current, particularly for the coupling between the gate driver and its associated power switch.

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Résumé étendu

Cette partie propose un résumé de synthèse en français du contenu du manuscrit.
This section offers an extended summary of the manuscript content in French.

Introduction générale

Les tendances actuelles de l'électronique de puissance se concentrent sur une efficacité et une densité de puissance plus élevées des convertisseurs de puissance. Depuis plusieurs années, les MOSFET de puissance à base de silicium ont dominé le domaine de la conception de convertisseurs de puissance en basse et moyenne tension. Cependant, cette technologie atteint ses limites de performances théoriques, ce qui signifie que de nouvelles technologies doivent être mises en œuvre pour obtenir de meilleures performances des dispositifs d'électronique de puissance. Dans ce contexte, les dispositifs à large bande interdite (WBG), comme le SiC et le GaN, se présentent comme de solides candidats pour répondre à ces nouvelles exigences [1–3].

Les dispositifs à large bande interdite permettent le développement de convertisseurs de puissance à haute fréquence et à haut rendement. Par rapport aux dispositifs d'alimentation en silicium, le champ de claquage plus élevé d'un semi-conducteur WBG permet de construire des couches plus fines du dispositif, ce qui entraîne une résistance à l'état ON spécifique plus faible [4]. Une taille de puce plus petite implique une capacité d'entrée et de sortie plus faible, ce qui permet d'obtenir un transitoire de commutation plus rapide. Les MOSFET SiC offrent les capacités de tension, de courant et de température plus élevées, tandis que les HEMT GaN offrent le rendement et la vitesse de commutation les plus élevés pour les applications de convertisseur de puissance.

Dans le contexte des véhicules électriques, l'un des objectifs les plus importants est de développer des circuits de puissance plus puissants avec une efficacité et une densité énergétique maximales. La réduction de la taille des composants suggère deux variables : la fréquence de commutation et le développement de nouvelles technologies de semi-conducteurs. La Figure .21 montre un schéma d'ensemble d'un groupe motopropulseur dans le véhicule électrique.

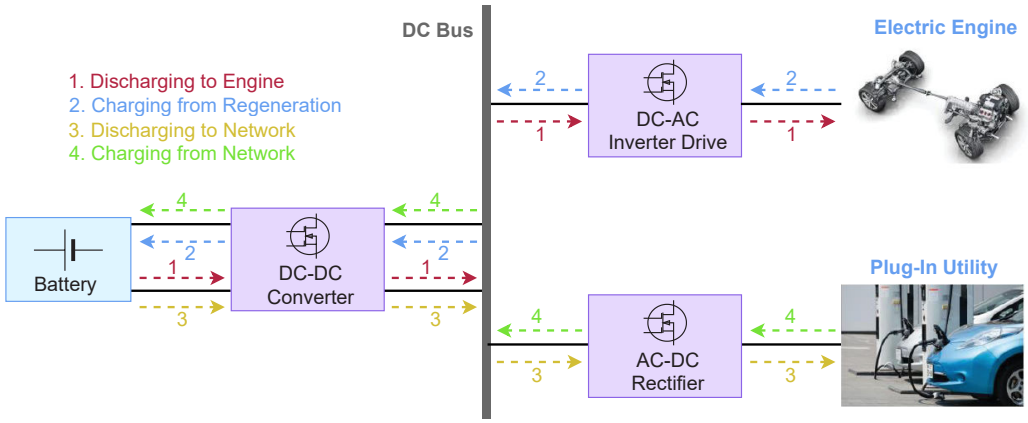


Figure .21: An universal DC-DC converter for plug-in electric vehicle adapted from [9].

Le premier objectif est d'augmenter la tension d'alimentation du groupe motopropulseur du véhicule électrique au-delà de 400 V, tension habituelle pour les batteries des véhicules électriques aujourd'hui. Cela réduirait le courant dans les puces IGBT de l'onduleur, et donc la quantité de silicium utilisée, diminuant le coût total. De plus, l'intégration de l'onduleur dans le moteur, permettant un système de refroidissement commun, sera explorée à l'avenir. Le deuxième objectif tout aussi important est d'améliorer la densité énergétique des onduleurs (en volume et en poids), ainsi que l'augmentation de la fréquence de découpage des convertisseurs de puissance DC-DC [9].

La principale motivation de cette thèse est de suivre les nouvelles technologies de dispositifs de puissance vers une meilleure intégration des semi-conducteurs WBG dans les applications automobiles. La coexistence de dispositifs SiC/GaN dans la gamme 600-900 V motive une étude spécifique de ces composants et le développement de méthodes pour effectuer une meilleure sélection en fonction de l'application. Dans cette thèse, un protocole de comparaison entre les dispositifs SiC et GaN basé sur l'estimation des pertes de commutation est discuté. La validation des modèles est effectuée pour les appareils de puissance,

les éléments parasites et les sondes de tension/courant. Le développement d'une méthode d'estimation des pertes de commutation tenant compte des principaux éléments du système est important pour la conception des convertisseurs de puissance.

Le sujet de recherche initial de cette thèse est d'effectuer la caractérisation des dispositifs à large bande interdite pour obtenir leurs caractéristiques statiques, dynamiques et en commutation. Les résultats de la caractérisation sont comparés à la fiche technique (datasheet) et les simulations pour la validation du modèle. L'impact de l'inductance de grille et de boucle de puissance du PCB utilisé pour la caractérisation de la commutation est analysé et certaines valeurs extraites obtenues à partir de l'outil de simulation sont validées par des tests de mesure. Par la suite, des modèles d'instruments de mesure (sondes de tension et de courant) sont développés pour évaluer leurs impacts sur les transitoires de commutation. Enfin, l'estimation de la perte de commutation est effectuée en ne considérant que les éléments dissipatifs des modèles SPICE de chaque dispositif cible, et une comparaison visant une application automobile est discutée.

Sur la base des objectifs de recherche décrits ci-dessus, cette thèse est organisée comme suit :

Dans le **Chapitre 2**, il est introduit l'étude générale utilisée dans cette thèse. Un aperçu complet des technologies SiC et GaN et des méthodes de pilotage de grille est présenté. Les processus généraux de caractérisation statique et de commutation qui sont applicables aux dispositifs WBG pour modéliser la validation sont discutés. Enfin, l'étude d'estimation des pertes de commutation est présentée en vue d'applications automobiles.

Dans **Chapitre 3**, la caractérisation des dispositifs de puissance est effectuée dans des états statiques et dynamiques pour la validation du modèle SPICE. L'objectif de cette section est de comparer la fiche technique, la simulation et les résultats expérimentaux pour différents appareils WBG à température ambiante et sous un fonctionnement à haute température.

Dans **Chapitre 4**, un PCB instrumenté est présenté pour analyser le transitoire de commutation des dispositifs GaN HEMT. L'analyse des princi-

paux éléments parasites du PCB est effectuée pour développer une simulation précise concernant le comportement de commutation. De plus, des modèles d'instruments de mesure (sondes de tension et de courant) sont développés pour vérifier l'impact sur les transitoires de commutation.

Dans **Chapitre 5**, la validation de commutation est présentée pour le dispositif GaN HEMT. De plus, l'estimation de la perte de commutation est effectuée en utilisant la méthode traditionnelle de calcul (produit V-I) et en ne considérant que les éléments dissipatifs. Une comparaison entre les dispositifs SiC et GaN est effectuée en vue d'une application automobile spécifiée.

Chapitre 2: Etat de l'Art

La technologie Silicium (Si) présente certaines limites pour les applications en haute tension (HT) et haute température (HT). Les applications d'électronique de puissance à base de silicium sont limitées à 150 °C et ne peuvent supporter que des tensions de blocage de 10 kV. De plus, la limitation de la vitesse de commutation des composants Si (quelques kHz) devient un problème pour un fonctionnement à plus haute fréquence. La vitesse de commutation élevée convient à des tailles de condensateur et d'inductance réduites, à un coût du système inférieur et à des performances globales plus elevées du système [2]. La capacité de densité de puissance élevée des dispositifs d'alimentation Wide-Band Gap (WBG) avec une commutation potentiellement rapide et à faibles pertes les rend adaptés aux applications automobiles où les performances et le faible poids sont essentiels pour le développement de convertisseurs de puissance plus compacts.

Les MOSFET SiC sont pilotés en tension via une carte de commande, communément appelée carte driver. En effet, le rôle principal de cette carte est de contrôler le passage de l'état bloqué à l'état ON. D'autres fonctionnalités sont également ajoutées, telles que la protection des interrupteurs de puissance et l'isolation galvanique entre l'unité centrale et l'étage de puissance. Cette carte de contrôle est principalement composée d'un driver et d'une alimentation isolée [18, 19].

Le pilote de grille est considéré comme une interface qui contrôle la charge

et la décharge de la capacité d'entrée de grille (C_{ISS}) pour permettre la commutation du transistor. Les MOSFET SiC fonctionnent avec une tension de source de grille d'environ +20 V pour l'état ON, et −5 V pour l'état OFF. L'isolation électrique et le décalage de niveau sont d'autres fonctions du pilote de grille [18]. Dans Figure .22, une structure de base pour un pilote de grille contrôlant un commutateur peut être vue.

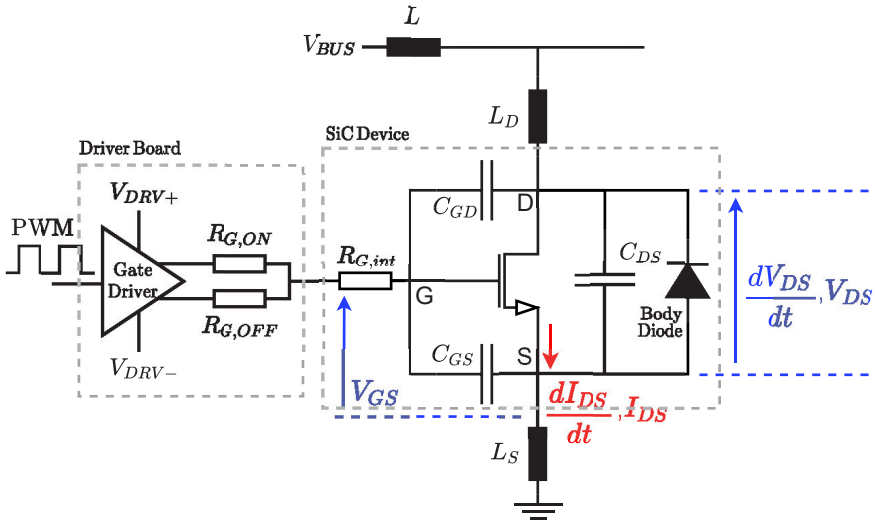


Figure .22: SiC MOSFET with parasitic elements and associated gate drive adapted from [14].

Le Nitrure de Gallium (GaN) est un semi-conducteur à large bande interdite qui présente une plus grande bande interdite énergétique que le Carbure de Silicium (SiC). Initialement utilisés pour des applications radiofréquences (RF), les GaN HEMT (High Electron Mobility Transistors) ont commencé à être utilisés en 2004 encore assemblés sur des substrats SiC. Actuellement, les substrats sont remplacés par du Silicium (Si), diminuant le coût de production des dispositifs GaN. L'utilisation de composants GaN est similaire aux MOSFET traditionnels, cependant certaines précautions doivent être prises en ce qui concerne l'assemblage, compte tenu de la taille réduite des dispositifs à base de GaN. De nos jours, la technologie de fabrication de PCB se développe et elle est déjà capable de concevoir des assemblages de haute performance.

Les technologies les plus populaires pour le développement du GaN HEMT dans l'électronique de puissance sont le HEMT en mode E (HEMT en mode d'amélioration) et le GIT (Gate Injection Transistor). Les deux structures con-

sistent en l'ajout d'une couche dopée P (AlGaN) sous la grille qui va appauvrir localement la zone 2DEG et par conséquent rendre le transistor naturellement OFF. Cependant, la solution GIT est réalisée en ajustant le tampon de super-réseau et la croissance épitaxiale de GaN afin de soulager la contrainte, en créant un contact résistif entre la couche dopée P et AlGaN [22].

La conception du pilote de grille pour les transistors GaN est équivalente à la méthode de pilotage des MOSFET SiC conventionnels. Cependant, il existe des exigences plus spécifiques, étant donné que la tension de seuil d'un appareil GaN est d'environ 1-2 V [22]. Le pilotage des dispositifs GaN basés sur les technologies e-HEMT et GIT-HD s'effectue de différentes manières. Les électrodes de grille de la structure e-HEMT ont une impédance d'entrée très élevée, et le contrôle du dispositif se fait par tension. Pour la structure GIT-HD, la couche mince de type p ajoutée sur les couches de drain et de grille agit comme des diodes physiques à jonction PN. Dans cette section, il sera décrit les principes fondamentaux du pilote de grille pour les dispositifs GaN.

Dans Figure .23, la structure de base pour piloter un mode GaN e-HEMT est présentée. Des résistances séparées ($R_{G,ON}$ et $R_{G,OFF}$) sont utilisées pour contrôler l'activation et la désactivation, définissant la vitesse de balayage. GaN Systems recommande un ratio $R_{G,ON}/R_{G,OFF}$ supérieur à 5 à 10 pour minimiser l'effet Miller. Une opération de tension de grille inférieure est nécessaire par rapport aux dispositifs Si, étant donné que la capacité de grille des dispositifs GaN est beaucoup plus faible que pour les interrupteurs de puissance basés sur le matériau Si [29].

La commutation rapide des dispositifs GaN nécessite un pilote de grille soigneusement choisi. Des caractéristiques telles que la résistance interne, le temps de montée/descente du pull-up/source et du pull-down/sink doivent être prises en compte pour la sélection du pilote. Pour éviter les limitations de la vitesse de commutation pendant les temps de chevauchement, le temps de montée/descente doit être inférieur aux délais d'activation et de désactivation du dispositif GaN [36].

La phase de caractérisation statique consiste à estimer les performances des dispositifs en conduction ou en état de blocage. Cependant, les pertes dans

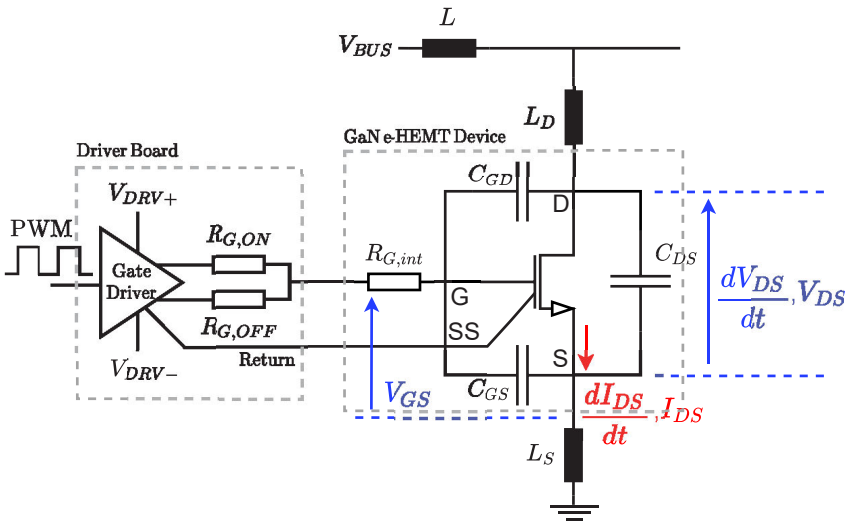


Figure .23: GaN e-HEMT with parasitic elements and associated gate drive adapted from [27].

l'état de blocage ne représentent qu'une petite partie des pertes totales. La procédure de caractérisation statique est réalisée en fonction de la délivrance d'impulsions contrôlées au DUT (Device Under Test). Ainsi, l'impact du signal de commande sur le comportement du transistor est mesuré, au moyen de l'analyse du canal de puissance. Pour limiter l'auto-échauffement du dispositif, des impulsions de courte durée sont utilisées ($< 500\,\mu$s) à faible répétition. Dans ce cas, on peut considérer la température de jonction égale à la température du boîtier (ambiante) du DUT [37].

Pendant ces phases, les valeurs de capacité de l'interrupteur d'alimentation influencent les formes d'onde de courant et de tension. Dans la Figure .24, on peut voir un schéma électrique équivalent d'un transistor de puissance. Le modèle se compose de sources de courant commandées en tension liées aux tensions appliquées aux bornes (drain, grille et source), de résistances en série dépendant de la température de jonction (T) et des capacités. Les valeurs de capacité dépendent directement des tensions aux bornes et diminuent lorsque la tension appliquée augmente [39].

Le modèle intrinsèque présenté dans la Figure .24 présente les sources de courant I_{GD} et I_{GS} pour la modélisation du courant de fuite. Pour simplifier, le dispositif GaN est traité comme un MOSFET de puissance en ce qui concerne sa capacité.

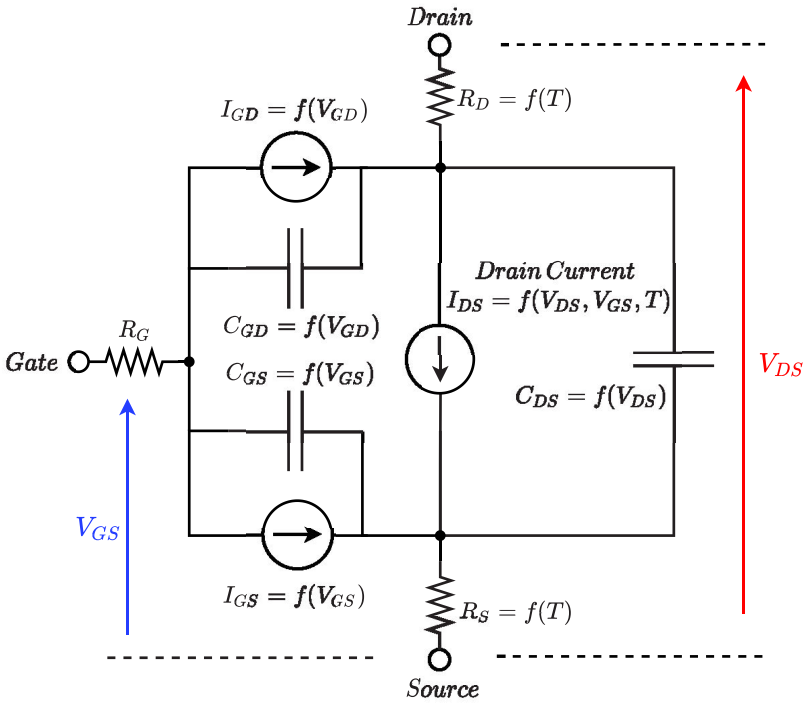


Figure .24: Nonlinear electrical model of a power MOSFET adapted from [39].

Les performances des semi-conducteurs de puissance sont liées au transitoire de commutation. Les principales caractéristiques dynamiques importantes impliquent la perte d'énergie de commutation, les paramètres de transition (temps de montée, temps de descente et pente de la courbe), les pointes dynamiques et la sonnerie parasite [42]. Afin de comprendre le comportement en commutation d'un MOSFET de puissance dans un onduleur à une branche (schéma pour Double Pulse Test), le transitoire de commutation est analysé dans un cas idéal, à savoir sans considération d'éléments parasites. Cette approche permet de mieux comprendre quelles variables sont les plus importantes lorsqu'il s'agit de comparer des dispositifs à semi-conducteurs de puissance. Il est important de souligner que le comportement en commutation est lié aux capacités parasites, qu'à l'amplitude et la relation entre chaque variable C_{GD}, C_{GS} et C_{DS} définit la performance de commutation de le dispositif MOSFET de puissance. Pour la commutation du dispositif SiC, il faut également tenir compte du temps de récupération de la diode du commutateur côté bas.

Une estimation et une modélisation précises des pertes en commutation sont essentielles pour concevoir des systèmes d'alimentation de convertisseur, prin-

cipalement dans le cas d'un fonctionnement à haute fréquence de commutation. De plus, le volume du système de refroidissement est directement impacté par la quantité d'énergie à dissiper [49]. Les dispositifs WBG apportent plusieurs avantages en termes de performances, cependant, la commutation de ces dispositifs est la plus sensible aux perturbations provenant d'éléments parasites liés à la conception du boîtier et du circuit imprimé.

L'augmentation de l'efficacité des systèmes de conversion d'énergie est l'objectif principal dans un scénario de consommation d'énergie croissante. En fait, la consommation d'énergie devrait augmenter d'environ 40 % dans le monde au cours des 20 prochaines années [58]. Les dispositifs à large bande interdite (SiC et GaN) peuvent réduire les pertes de commutation, entraînant une augmentation de l'efficacité. En raison de leur bande interdite plus large par rapport au matériau Si, ces dispositifs ont le potentiel de fonctionner dans des environnements plus difficiles, par exemple, à haute tension et température [59]. Plusieurs domaines d'application peuvent être identifiés comme ayant un marché important pour l'utilisation des dispositifs WBG : alimentations électriques pour centres de données, production d'énergie renouvelable, entraînements de moteurs pour applications industrielles, traction ferroviaire et véhicules hybrides et électriques [60]. Dans cette thèse, les applications automobiles sont au centre des préoccupations.

Le grand défi de l'industrie automobile est de diminuer les émissions de gaz à effet de serre (GES) des véhicules. Dans ce contexte, l'électrification des véhicules augmente rapidement et l'électronique de puissance a pour fonction de devenir des convertisseurs de puissance de plus en plus performants. Les recherches avancées sur les véhicules électriques (VE) tendent vers le zéro émission de carbone [77], et les perspectives de ventes de véhicules électriques sont plutôt positives, comme on peut le voir dans Figure 2.37. En 2020, 4.7 % des voitures particulières neuves étaient des véhicules électriques, ce qui représente un total de 3.1 millions vendus. Une nouvelle recherche de Canalys indique que 48 % des ventes de voitures particulières seront des véhicules électriques d'ici 2030 [78].

Les semi-conducteurs WBG offrent plusieurs avantages qui permettent des niveaux de performance plus élevés par rapport à la technologie Si standard.

Des températures de fonctionnement, des tensions et une puissance maximale plus élevées peuvent réduire les pertes totales, les dimensions et le poids des véhicules électriques, augmentant ainsi l'efficacité du système d'alimentation électrique. Chaque appareil WBG a son avantage en fonction de l'application dans le véhicule électrique [79]. Il est important de souligner que pour concevoir un convertisseur de puissance basé sur des dispositifs WBG, certaines précautions sont nécessaires, telles que l'optimisation de la conception du pilote de grille et de la disposition des circuits imprimés, ainsi que la mise en œuvre d'une gestion thermique efficace [80].

Les dispositifs WBG présentent de meilleures performances pour les convertisseurs de puissance grâce à leur fréquence de commutation plus élevée, leur conductivité thermique plus élevée et leur niveau d'intégration élevé. Une étude approfondie des technologies SiC et GaN a permis de comprendre les raisons de leurs meilleures performances par rapport au matériau Si. Même si les dispositifs WBG ont un coût plus élevé, une intégration haute puissance et des économies d'énergie en raison du rendement élevé des convertisseurs de puissance sont destinés aux applications automobiles. Il est important de souligner que le prix de fabrication de ces composants diminue avec le temps. Pour l'électrification des véhicules, les dispositifs WBG sont des technologies clés et on peut s'attendre à ce qu'ils rendent les véhicules électriques plus efficaces et économiques dans un avenir proche.

Chapitre 3: Caractérisation des Dispositifs de Puissance

La caractérisation du dispositif d'alimentation est effectuée dans des états statiques et dynamiques pour la validation du modèle SPICE. La caractérisation des dispositifs WBG doit être effectuée finement afin de développer des modèles fiables en simulation. Les caractéristiques de sortie et de capacité sont obtenues dans le cadre de la validation du modèle. Le protocole de test doit être effectué avec soin, compte tenu des propriétés uniques des dispositifs WGB. Par exemple, les caractéristiques du courant de fuite de drain pourraient modifier la réponse I-V en raison de l'effondrement du courant associé aux composants GaN. Par conséquent, les tests de caractéristiques de sortie et de capacité sont

effectués pour deux échantillons différents, et sans aucune mesure préalable de courant de fuite [8]. L'objectif de cette section est de comparer la fiche technique, la simulation et les résultats expérimentaux pour différents dispositifs WBG à température ambiante et sous un fonctionnement à température maximale. Les dispositifs à tester sont présentés dans Table .11. Pour chaque dispositif, deux échantillons sont utilisés. Les caractéristiques du transistor sont mesurées avec un Curve Tracer Keysight B1505A (500 A - 10 kV), Figure .25.

Table .11: Selected power semiconductor devices with typical properties.

Component	Manufacturer	Material	Type	Vnom (V)	Inom (A)	$R_{DS(ON)}$ ($m\Omega$)
GS66516T Samples: G1;G2	GaN Systems	GaN	eHEMT	650	60	25
PGA26E07BA Samples: P1;P2	Panasonic	GaN	GiT	600	26	56
SCT3030AW7 Samples: S3;S4	Rohm	SiC	MOSFET	650	70	30
C3M0060065K Samples: W1;W2	CREE	SiC	MOSFET	650	30	60

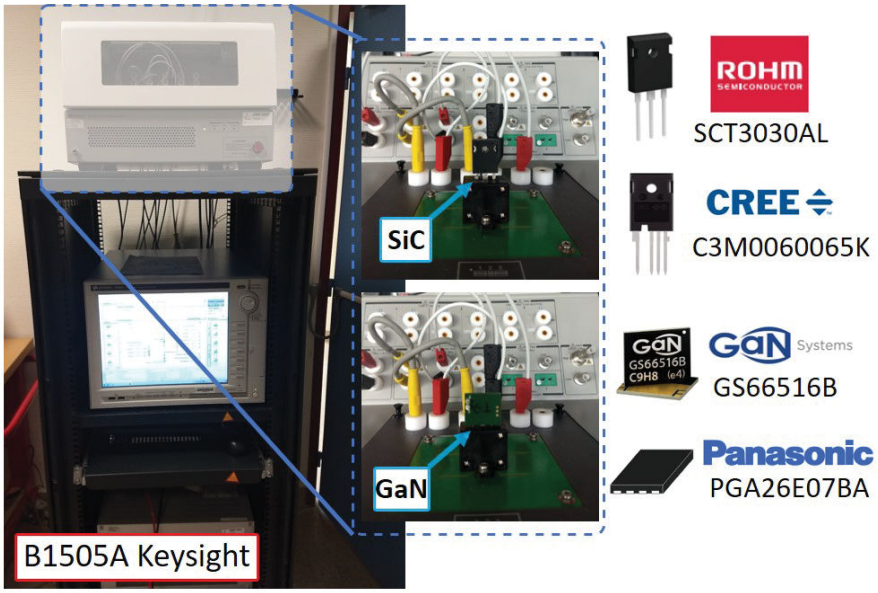


Figure .25: Curve Tracer Keysight B1505A and the devices used in this study.

Les dispositifs GaN ont été montés sur une carte PCB afin de s'adapter à l'emplacement B1505A. Les tests ont également été effectués à haute température, proche de la température maximale de jonction de chaque dispositif de puissance. Pour cela, une plaque chauffante est utilisée directement connectée au boîtier de l'appareil. Pour les dispositifs GaN Systems, les premiers tests à température ambiante ont été réalisés avec l'échantillon G1, au cours de

la première année de thèse. Plus tard, des tests avec une plaque chauffante ont été menés pour des tests à haute température. Ces tests ont probablement pu dégrader les échantillons. Cependant, l'échantillon G2 a présenté un comportement plus similaire avec les résultats de la fiche technique et de la simulation, vu à la Figure 3.3. Une bonne tendance est vérifiée même à haute température. Dans Section A.1, les caractéristiques de sortie ont été superposées pour les deux échantillons afin de vérifier le comportement équivalent.

Le dispositif Panasonic utilisé pour les deux tests de température était le même : échantillon P2. En analysant les résultats présentés dans Figure 3.4, il est possible de vérifier les résultats d'une fiche technique optimiste par rapport aux résultats de simulation et expérimentaux. Une explication possible pourrait être liée à un échantillon de haute performance utilisé par les fabricants lors de leurs tests. Les tests à haute température ont été effectués avec plus de soin afin de ne pas chauffer l'appareil.

Les caractéristiques de transfert ont également été tracées pour les deux dispositifs GaN (GaN Systems et Panasonic), comme on peut le voir dans la Figure 3.5. A haute température, la tension de seuil a tendance à augmenter pour la technologie GaN dans les fiches techniques, les simulations et les résultats expérimentaux. Une certaine différence entre les résultats expérimentaux et de simulation peut être remarquée, ce qui peut être expliqué par des composants avec des tensions de seuil différentes.

La caractérisation statique a également été réalisée pour les dispositifs SiC (Rohm et CREE), répertoriés dans la Table 3.1. Une bonne corrélation est obtenue entre la fiche technique, la simulation et les résultats expérimentaux, comme on peut le voir dans les Figure 3.7 et Figure 3.8. Ceci est raisonnable compte tenu du niveau de développement, actuellement, de la technologie SiC. En analysant les caractéristiques de sortie des dispositifs SiC, on remarque un état de saturation convergent entre la simulation et les données expérimentales, ce qui indique une bonne estimation de la perte de commutation.

Les tests à haute température du dispositif CREE n'ont pas pu être effectués en raison d'un problème technique avec la plaque chauffante connectée au Curve Tracer (B1505). La faible variation des caractéristiques de sortie des dispositifs SiC à haute température, par rapport aux dispositifs GaN, mon-

tre de meilleures performances pour les applications à courant élevé. Les caractéristiques de transfert des deux dispositifs SiC sont présentées dans Figure 3.9. Contrairement aux dispositifs GaN, la tension de seuil diminue avec l'augmentation de la température. Cela peut générer une mise sous tension plus sensible de l'appareil lors d'un fonctionnement à haute température. Cependant, une bonne corrélation entre la fiche technique, la simulation et les résultats expérimentaux est vérifiée pour les dispositifs SiC, à température ambiante et élevée.

La modélisation de la capacité d'entrée doit être effectuée avec précision, car elle détermine la vitesse de commutation, influençant par conséquent les pertes de commutation. La capacité de Miller (C_{RSS}) est le composant principal de l'effet de conduction croisée, comme démontré dans les tests de caractérisation dynamique [5]. Une bonne corrélation est trouvée pour la comparaison entre la fiche technique, la simulation et les résultats expérimentaux pour les dispositifs GaN, comme on le voit dans la Figure 3.13. Ceci implique que, pour l'estimation des pertes de commutation, les modèles SPICE présentent un comportement proche du dispositif utilisé pour les tests. Les caractéristiques de capacité des dispositifs SiC sont également présentées dans Figure 3.14. Comme mentionné précédemment, en raison de l'état de développement de la technologie SiC, il est raisonnable que leurs fabricants présentent des modèles SPICE plus fiables et proches des résultats expérimentaux.

La comparaison entre les résultats expérimentaux et de simulation présente une bonne corrélation. La caractérisation statique et dynamique des dispositifs permet de valider les modèles SPICE pour les utiliser en mode commutation. Ainsi, compte tenu de certains ajustements sur la tension de seuil, l'estimation des pertes en commutation peut être effectuée en utilisant les modèles disponibles par le fabricant. Le niveau de développement des modèles SPICE pour les dispositifs SiC est évident, principalement en raison du temps que ces composants sont sur le marché. Les dispositifs GaN sont encore soumis à de grandes variations entre les modèles de simulation et les tests expérimentaux.

Chapitre 4: Caractérisation du Comportement en Commutation

La nécessité d'augmenter les performances de l'électronique de puissance a motivé le développement de nouvelles recherches sur les dispositifs semi-conducteurs, tels que les commutateurs GaN HEMT. Ce sont des composants prometteurs pour la conception de modules de puissance à commutation rapide, à haut rendement et donc à haute densité de puissance [22]. Pour étudier ces nouveaux dispositifs, un PCB instrumenté a été développé comprenant les points de mesure nécessaires à cet effet. Les éléments parasites du schéma PCB extraits par ANSYS Q3D et les modèles des instruments de mesure sont également inclus dans le modèle de simulation. Un module d'alimentation à base de GaN à une jambe est également analysé en ce qui concerne les oscillations à la tension du point médian, et l'impact de la modélisation des éléments parasites est vérifié en comparant les résultats de simulation et d'expérimentation.

Compte tenu de la vitesse de commutation élevée du dispositif GaN, les résultats des tests expérimentaux sont sensibles à la conception de la configuration du PCB et à la gestion des parasites. Dans la Figure .26, on peut voir la conception du PCB instrumenté. L'étage de puissance est séparé du pilote de grille mis en œuvre dans deux cartes dédiées. Les pistes $+V_{DC}$ et $-V_{DC}$ sont conçues pour avoir une surface maximale, réduisant les effets d'inductance de couplage. Cependant, la largeur de la piste conductrice ne peut pas être augmentée arbitrairement en raison de l'influence de la capacité parasite formée avec le plan de masse [94]. Les condensateurs de découplage sont placés au plus près des dispositifs de puissance, minimisant ainsi la boucle de puissance. Le shunt utilisé pour la mesure de courant est placé en sens inversé. La borne négative permet à la borne source du commutateur côté bas de partager le même potentiel avec la terre. De cette façon, au moment de la mesure de la tension drain source sur l'interrupteur côté bas, les perturbations ajoutées par le shunt peuvent être négligées, étant lues exactement la tension sur le boîtier de l'interrupteur [42]. La boucle de grille doit être minimisée autant que possible, car l'inductance parasite présentée dans cette boucle peut générer un dépassement aux bornes de source de grille. Pour le PCB instrumenté, une distance considérable entre les PCB du pilote et la grille du dispositif de puis-

sance est observée en raison de l'instrument de mesure ajouté (transformateur de courant).

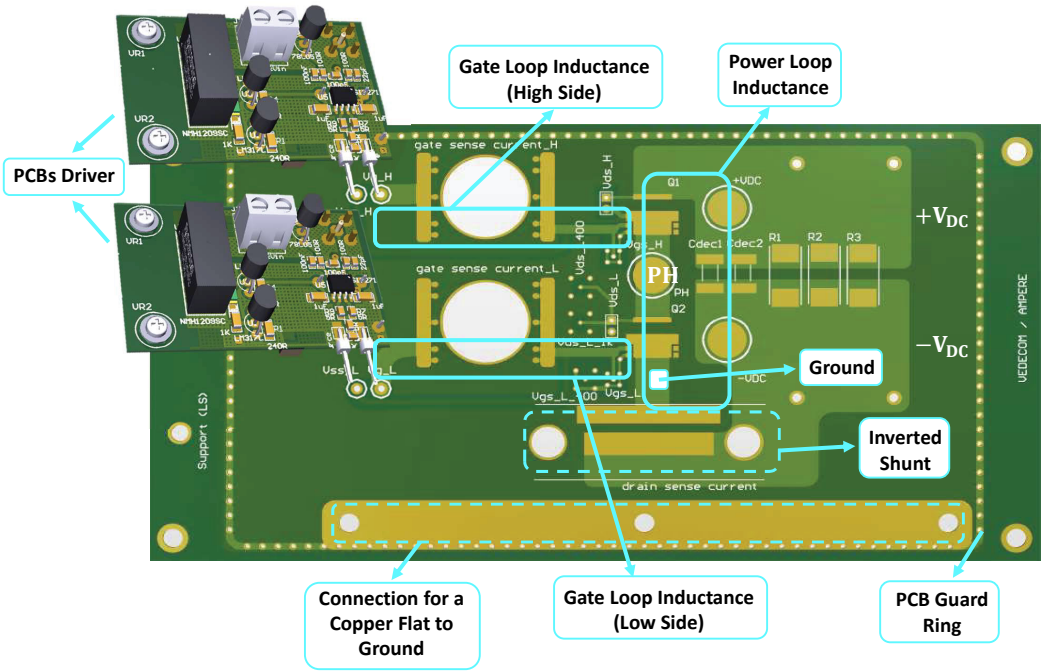


Figure .26: Instrumented PCB and gate drivers design.

L'analyse des éléments parasites est importante pour effectuer une estimation précise des pertes en commutation. Cette analyse est réalisée en considérant trois éléments principaux sur la simulation SPICE : le modèle SPICE du composant GaN (GS66516), les modèles d'instruments de mesure et les éléments parasites du modèle de câblage 3D. Dans Figure 4.9, le circuit du DPT et ses points de mesure sont présentés. Une plaque de cuivre est utilisée comme chemin de piste lorsque seul le courant de grille sur l'interrupteur côté bas est mesuré. Plusieurs paramètres parasites critiques ont pu être identifiés et étudiés sur leur effet individuel grâce au test de commutation de dispositif GaN. Pour mieux comprendre l'impact des éléments parasites sur les formes d'onde courant/tension drain-source, une simulation paramétrique est effectuée. Dans cette étude, il est adopté les deux boucles principales du PCB pour analyser le comportement électrique sur le dispositif d'alimentation : l'effet de la boucle d'alimentation (L_{Ploop}) et l'inductance de la boucle de grille (L_{Gloop}) . Pour cette approche, la simulation ne prend pas en compte l'inductance parasite ajoutée par le shunt. Dans Figure 4.10 et Figure 4.11, le

résultat de la variation de l'inductance de la boucle d'alimentation/grille peut être vu pendant l'activation et la désactivation, respectivement.

Lors de la simulation réalisée sur ANSYS Q3D, certains problèmes ont été rencontrés. Des problèmes numériques associés à des régions complexes pour le fonctionnement du maillage ont été détectés, ce qui génère un temps de simulation trop important. Une région masse (GND) est également un élément important pour définir le chemin actuel à travers le modèle 3D. Comme le PCB instrumenté a une masse spécifique à la source de commutation côté bas, le GND a été défini comme un NET commun, au lieu d'utiliser la définition GND standard, en permettant de définir une SOURCE et un SINK pour le chemin actuel, définitions trouvées dans ANSYS Q3D pour spécifier l'entrée /courant de sortie par un conducteur. De plus, la solution des éléments parasites est adaptée pour une bande passante spécifiée, cependant, l'ANSYS Q3D n'est capable d'exporter qu'une fréquence simple. Ainsi, la fréquence de 100 MHz est définie en fonction de la vitesse de commutation des dispositifs GaN. Le Q3D n'est pas un logiciel multicouche, donc une géométrie aussi simple que possible doit être utilisée pour la simulation.

La comparaison entre la simulation et les résultats expérimentaux peut être vue dans la Figure 4.15. Les résultats trouvés grâce au test expérimental montrent une bonne corrélation avec les valeurs d'inductance extraites par Q3D Extractor, en menant une bonne estimation. Dans ce cas, la boucle de puissance ne prend pas en compte l'inductance du boîtier des dispositifs de puissance, seules les pistes PCB sont simulées et mesurées.

L'utilisation d'un oscilloscope et de certains instruments de mesure pose des problèmes d'observabilité. Certaines perturbations peuvent apparaître et provoquer des erreurs expérimentales. Le principe d'incertitude de Heisenberg a été la première théorie physique sur ce sujet, en étudiant la position et la quantité de mouvement des électrons. Au niveau de l'ingénierie, en faisant un parallèle entre l'étude des électrons et les mesures de tension/courant, ce principe est également valable et, en effet, toute tentative de mesure d'une certaine variable peut générer des perturbations du système.

En électronique de puissance, les mesures de tension et de courant sont très importantes soit pour l'analyse de la forme d'onde, soit pour l'estimation des

pertes de puissance. La méthode classique DPT (Double Pulse Test [98,99]) de caractérisation des dispositifs de puissance doit également être mise en œuvre à l'aide d'instruments de mesure précis.

Les modèles d'instruments de mesure ne sont pas fournis par les fabricants, ainsi, en raison des imprécisions associées aux sondes de tension/courant, un modèle électrique raisonnable doit être utilisé pour la simulation du système complet. Cela permet de mieux connaître les perturbations ajoutées au système et d'estimer le comportement réel d'un convertisseur réaliste, sans perturbations ajoutées [42]. Les instruments de mesure utilisés dans cette étude sont présentés dans la Table .12. L'objectif principal est de développer des modèles précis pour les instruments de mesure, au moyen d'une procédure simple. De cette manière, la comparaison entre les résultats de simulation et d'expérience peut être effectuée pour la validation du modèle et pour estimer les pertes en commutation [5–8].

Table .12: Measurement instruments used in this work.

Voltage/Current Probes	Manufacturer (Reference)	Measured Variable	Description
Passive Voltage Probe	Teledyne Lecroy (PP024)	Gate Source Voltage (V_{GS})	Bandwidth: 500 MHz Input Voltage: 400 V Attenuation: 10x
High Voltage Passive Probe	Teledyne Lecroy (HVP120)	Drain Source Voltage (V_{DS})	Bandwidth: 400 MHz Input Voltage 1000 V Attenuation 100x
AC Current Probe	Tektronix (CT1)	Gate Current (I_G)	Bandwidth: (25k-1G) Hz Max. Peak Pulse Current: 12 A Sensitivity: 5 mV/mA
Current View Resistor	T&M Research (W-1-01C-1FC)	Drain Source Current (I_{DS})	Bandwidth: 800 MHz Max. Energy: 20 J Series Resistor: 0.01 mΩ

Les variables électriques, la tension de source de grille (V_{GS}) et la tension de source de drain (V_{DS}), présentent des amplitudes différentes. Pour V_{GS}, on utilise une simple sonde passive, et pour V_{DS}, il faut choisir une sonde passive haute tension, dès lors que les surtensions peuvent atteindre des valeurs supérieures à 400 V [98]. Le courant de grille (I_G) est caractérisé pour présenter des fréquences d'oscillation élevées, en plus d'avoir une faible amplitude [100]. Une mesure isolée doit également être effectuée, étant donné que la grille de commutation n'est pas référencée à la terre. Par conséquent, uun tore de mesure convient à cette application [101]. Pour le courant de drain (I_{DS}), une résistance shunt suffit pour la mesure [102].

L'analyse complète de l'impact des éléments parasites du câblage peut améliorer la précision de l'estimation des pertes de commutation. De plus, au moyen de résultats expérimentaux, la nécessité d'une bonne modélisation des mesures instrumentales et d'un modèle 3D pour l'extraction parasitaire est vérifiée. Une simulation tenant compte de la puissance et de l'inductance de la boucle de grille peut donner une bonne correspondance avec les données expérimentales. Cette approche permet de valider tous les modèles utilisés dans les simulations SPICE, et ainsi de pouvoir évaluer plus précisément l'efficacité globale des convertisseurs à base de composants GaN, même ceux qui ne seront pas instrumentés.

L'analyse parasite du module de puissance à base de GaN vise à considérer les trois principales fréquences de résonance dans les formes d'onde de tension du point milieu et du drain-source. De bons résultats ont été trouvés par simulation. Les valeurs des éléments estimés ont été comparées à celles extraites par un outil numérique. Il est clair que l'utilisation d'un modèle 3D pour l'extraction des éléments parasites améliore la simulation et l'ajustement de la mesure. L'analyse de la perturbation électromagnétique est plus facile dans le domaine fréquentiel que dans le domaine temporel. Dans le domaine fréquentiel, il est plus facile de voir quelles bandes de fréquences ont le plus de contribution à la source de perturbation électromagnétique et ainsi de déterminer une solution pour réduire les perturbations.

Une étude complète sur les instruments de mesure utilisés pour les dispositifs WBG permet de comprendre l'impact de chaque élément sur la charge du circuit. Un protocole clair pour la modélisation des instruments de mesure est présenté. La vitesse de commutation rapide des dispositifs GaN nécessite cette modélisation pour obtenir une simulation précise. La comparaison entre la fiche technique, la simulation et les tests expérimentaux effectués présente une bonne corrélation par rapport aux caractéristiques d'impédance d'entrée, donc l'impédance vue par le circuit peut être estimée dans une simulation globale. De plus, la réponse en fréquence des modèles est également simulée pour comparer avec les limites de la fiche technique, en montrant une bande passante assez proche de la spécification des instruments de mesure.

Chapitre 5: Estimation des Pertes en Commutation

La capacité de densité de puissance élevée des dispositifs Wide Band Gap (WBG) avec une commutation potentiellement rapide et de faibles pertes qui rend adaptés aux applications automobiles où les performances et le faible poids sont essentiels pour le développement de convertisseurs de puissance plus compacts. Les dispositifs de puissance GaN présentent une meilleure performance par rapport aux dispositifs de puissance Si grâce à leur champ électrique critique supérieur et leur mobilité électronique élevée dans le canal 2DEG. Cela permet d'avoir des valeurs de capacité plus faibles et donc une commutation à grande vitesse, en plus d'avoir une résistance à l'état passant plus faible. Cependant, ces améliorations apportent de nouveaux défis en ce qui concerne les mesures de perte des convertisseurs à base de matériau GaN. Les dispositifs SiC permettent un fonctionnement à tension plus élevée et, en raison de leur commutation rapide (forte dv/dt et di/dt), les mêmes problèmes rencontrés pour les dispositifs GaN dans l'estimation des pertes sont également détectée.

Les résultats expérimentaux sont utilisés pour valider le modèle SPICE du dispositif ainsi que pour l'estimation des pertes. De plus, avec le modèle validé, il sera possible d'évaluer par simulation les pertes dans un circuit optimisé sans sondes de mesure [118]. Dans Figure .27, le schéma complet est présenté, y compris tous les instruments de mesure utilisés pour les tests, le filtre d'entrée pour le test DPT et les pilotes pour les dispositifs GaN. Actuellement, les dispositifs GaN ont la capacité de commutation la plus rapide parmi les dispositifs d'alimentation sur le marché, ils sont donc choisis pour valider le modèle d'appareil et les modèles d'instruments de mesure. La pertinence des éléments parasites devient élevée en raison de cette vitesse de commutation rapide. Figure 5.2 montre les principales valeurs d'inductance utilisées pour la simulation. L'inductance de boucle de grille (L_{Gloop}) est extraite d'ANSYS Q3D, l'inductance de boîtier du boîtier de dispositifs d'alimentation (L_{SW}) est obtenue à partir de la fiche technique, et l'inductance d'insertion du shunt et l'inductance de boucle de puissance ont été mesurée par un analyseur d'impédance. L'inductance de la boucle de puissance est également simulée à

l'aide d'ANSYS Q3D pour valider la méthode d'extraction.

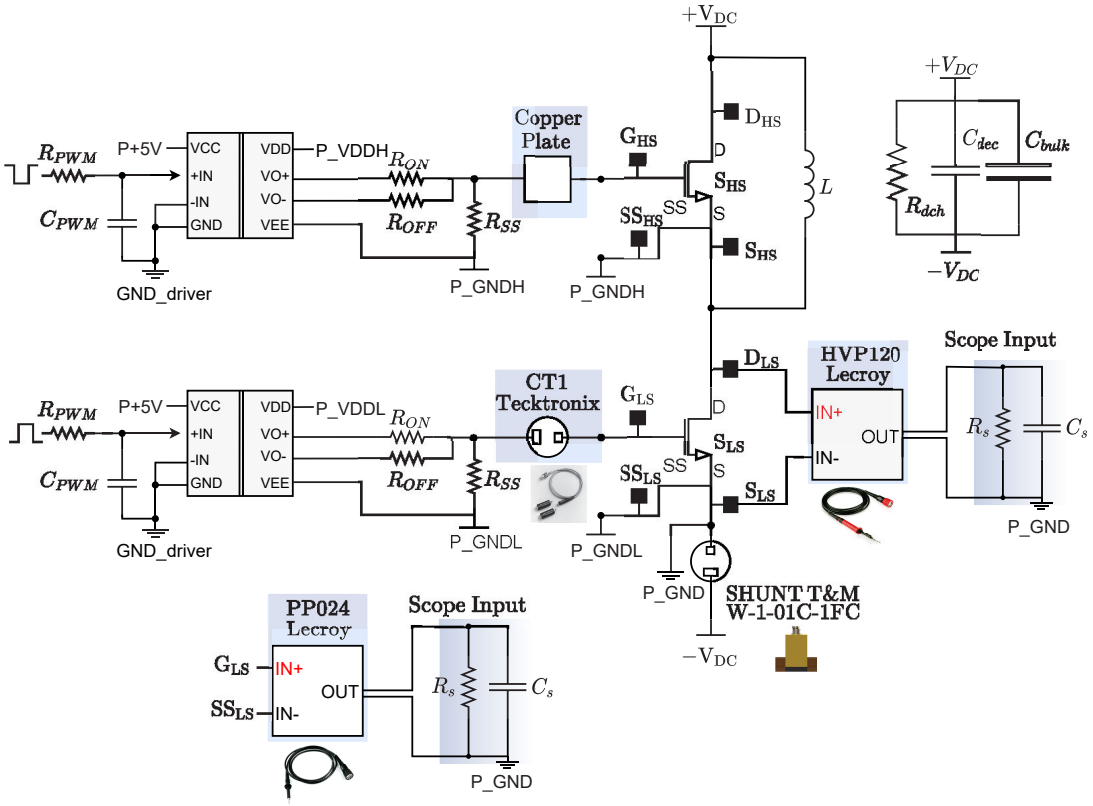


Figure .27: Schematic showing all measurement instruments used to the tests. Parameters: GaN Systems GS66516B – R_{ON},R_{OFF},R_{SS}: $(10, 5, 10\text{k})\ \Omega$ and V_{GS}: $(+5, -3)$ V.

Le développement d'une méthode permettant l'estimation des pertes en commutation est important pour la conception des convertisseurs. En raison également de la commutation rapide, l'effet des éléments parasites du circuit est très important. Pour cette raison, une bonne méthode utilisée par les concepteurs de convertisseurs consiste à analyser, à l'aide de simulations, le comportement de commutation du dispositif sous l'influence d'éléments parasites du circuit avant de fabriquer le circuit physique. Ceci est particulièrement utile car cela permet d'ajuster les topologies de circuits ou de comparer différentes dispositions en fonction des résultats de la simulation [50].

Le modèle GaN GS66516b SPICE développé par GaN Systems est basé sur des caractéristiques mesurées. Le schéma fonctionnel présenté dans la Figure .28 est développé comme pour le modèle électrique non linéaire d'un MOSFET de

puissance et du code SPICE du dispositif de puissance GaN. Le diagramme se compose de la résistance d'entrée (R_D, R_G et R_S) pour chaque borne ; des valeurs de capacité associées aux différentes couches du dispositif de puissance ; résistances internes du canal (R_{drain2} et $R_{source2}$); et une tension de comportement représentant le canal 2DEG ($bswitch$).

La méthode traditionnelle tension multipliée par le courant au niveau du switch pourrait générer des falses valeurs en raison des éléments capacitifs internes du switch. Ainsi, en utilisant le schéma présenté dans Figure .28, seuls les éléments dissipatifs, la source de chauffage tels que les résistances et le canal (résistance non linéaire), doivent être utilisés pour l'estimation de la perte de commutation. Dans le simulateur LTSpice, les options d'enregistrement des tensions de nœud de sous-circuit et des courants de périphérique doivent être activées. En effectuant le produit V-I directement pour chaque résistance du diagramme et la source de tension de comportement, la valeur finale de la perte de commutation est atteinte. Dans Figure 5.11, on peut voir la comparaison entre le produit de la méthode traditionnelle V-I et le calcul utilisant uniquement des éléments dissipatifs. La différence est plus évidente est la période de blocage en raison de l'oscillation associée à la résonance entre la capacité et l'inductance parasite.

L'énergie d'allumage domine l'énergie totale, ainsi les erreurs liées à l'énergie d'extinction ont un faible impact sur l'estimation de la perte de commutation totale. Dans Table .13, l'énergie totale de commutation est présentée pour éliminer les problèmes liés au produit V-I appliqué sur les résultats expérimentaux et sur la colonne "Scope".

Table .13: Total switching energy of GS66516B.

Operation Points (V | A)	Turn-ON (μJ)+Turn-OFF (μJ)								
	Simple Simulation	Probe Models		Adding L_{Ploop} and L_{Gloop}		With full Q3D		Experimental	
		Switch	Scope	Switch	Scope	Switch	Scope	Delay Comp.	Scope
100 | 4.3	11.1	10.7	14.0	12.2	17.2	14.0	18.9	17.5	19.7
200 | 8.5	42.1	42.5	51.7	57.7	76.1	67.6	85.8	64.9	81.1
300 | 12.6	89.8	99.9	118.2	136.1	171.0	164.6	194.9	156.7	183.6
400 | 18.3	165.0	178.4	217.0	266.3	313.9	294.9	333.2	298.6	334.6

Pour comparer ces dispositifs de puissance, la caractérisation de la commutation est effectuée pour la validation du modèle. Ensuite, une simulation considérant la même puissance et la même inductance de boucle de grille est

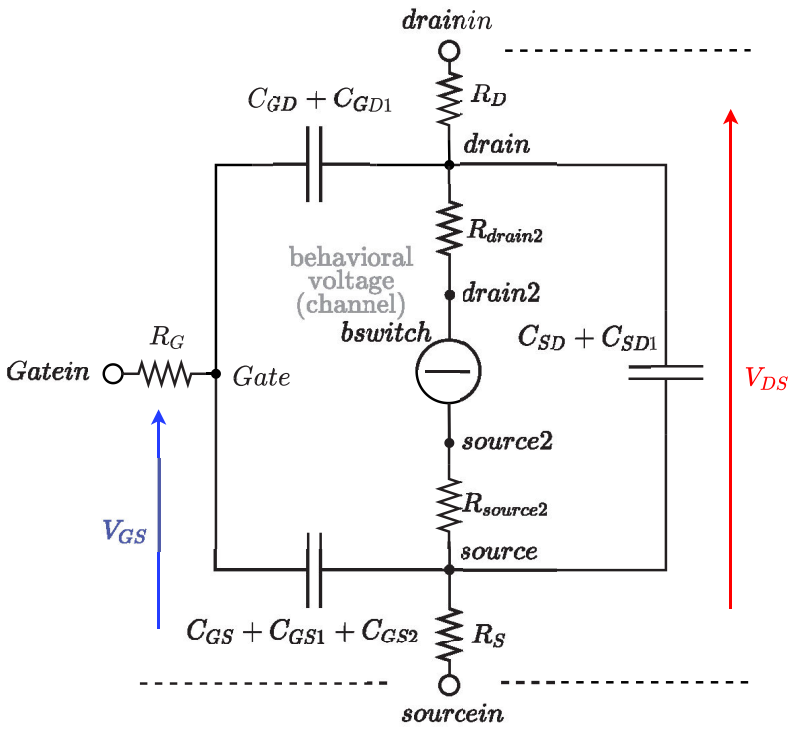


Figure .28: Nonlinear electrical model of a GaN HEMT for switching loss estimation adapted from [39].

effectuée pour chaque dispositif, ce qui permet d'évaluer les performances de commutation dans des conditions égales. Une figure de mérite (FOM) basée sur la résistance statique ON et les pertes de commutation est utilisée comme principal élément de comparaison [7]. Avec les modèles validés, il est possible de développer une simulation de convertisseur DC-DC pour chaque dispositif d'alimentation et de comparer leurs performances pour une application automobile à 200-400 V pour différents niveaux de charge [6,50,118,124] . L'analyse comparative des dispositifs dans un fonctionnement DC-DC est effectuée en se concentrant sur le FOM de commutation.

Comme prévu, les pertes en commutation augmentent avec des niveaux de courant plus élevés. La Figure 5.18(c) montre des pertes en commutation totales inférieures pour le dispositif CREE (C3M0060065K) aux deux températures analysées. Ceci est lié au fait que ce dispositif a un courant nominal inférieur à celui des autres dispositifs, donc une charge plus faible est requise pour le processus de commutation. Dans Figure 5.18(d), l'effet de l'ajout d'un facteur de perte de conduction devient évident la meilleure performance pour le

dispositif GaN HEMT (GS66516), à 25 °C . Ceci est associé au fait que le GaN a une résistance à l'état passant et une valeur de capacité proportionnellement inférieures à celles des dispositifs SiC. Cependant, en raison de la forte dépendance à la température de la résistance ON présentée par le GaN HEMT, son FOM de commutation augmente considérablement à 125 °C. Si l'interrupteur ne fonctionne pas à des températures élevées, le dispositif GaN présente de meilleures performances que les dispositifs SiC, comme on le voit dans Figure 5.18(d), pour le fonctionnement DC-DC spécifié.

Les performances des convertisseurs de puissance reposent sur les pertes en commutation et en conduction des dispositifs de puissance, étant donné que des pertes de puissance inférieures garantissent une efficacité maximale, une densité de puissance élevée et une réduction de la taille du dissipateur thermique et du circuit de refroidissement [125]. Ainsi, les dispositifs WBG sont des candidats prometteurs pour les applications automobiles. Un convertisseur DC-DC typique pour un chargeur embarqué peut fonctionner dans une plage de courant de 10 à 20 A, en considérant une spécification nominale de 200 à 400 V pour 3.6 kW. Une simulation de convertisseur boost pour chaque appareil cible est effectuée sous différentes fréquences et niveaux de puissance. Ainsi, en considérant les mêmes conditions vis-à-vis des éléments parasites, le dispositif le plus adaptable à un point de fonctionnement peut être nommé.

Les pertes totales sont estimées par une simulation SPICE. Dans Figure 5.20, les pertes de puissance totales sur les commutateurs peuvent être vues. Toutes les simulations sont effectuées à 25 °C et 125 °C comme température de jonction. Pour une puissance d'entrée jusqu'à 3 kW, le SiC CREE présente des pertes plus faibles, en raison de sa capacité de commutation plus rapide. Au fur et à mesure que la puissance augmente, la résistance ON pour SiC CREE commence à augmenter et devient de plus en plus pertinente sur l'estimation des pertes totales, ainsi le dispositif GaN Systems devient plus efficace, compte tenu de sa résistance ON inférieure. En ce qui concerne le comportement à haute température, tous les dispositifs présentent des pertes de commutation plus élevées. Le GaN HEMT présente la différence la plus accentuée entre les dispositifs, en raison de sa forte dépendance à la température, comme discuté précédemment. Néanmoins, comme le montre Figure 5.20(b), pour une puissance nominale de 3.6 kW, le convertisseur boost à base de GaN

présente les pertes totales les plus faibles.

L'analyse complète de l'impact des éléments parasites du câblage peut améliorer la précision de l'estimation des pertes de commutation. De plus, au moyen de résultats expérimentaux, la nécessité d'une bonne modélisation des mesures instrumentales et d'un modèle 3D pour l'extraction parasitaire est vérifiée. Une simulation tenant compte des valeurs de puissance et d'inductance de boucle de grille peut donner une bonne correspondance avec les données expérimentales. Cette approche permet de valider tous les modèles utilisés dans les simulations SPICE, et ainsi de pouvoir évaluer plus précisément l'efficacité globale des convertisseurs à base de composants GaN, même ceux qui ne seront pas instrumentés.

La méthodologie de fitting du courant de mise sous tension permet d'obtenir une erreur maximale pour les pertes de commutation d'environ 12 % pour les dispositifs GaN et 8 % pour les dispositifs SiC. Concernant le facteur de mérite de commutation et les résultats préliminaires, la comparaison des commutateurs montre que le dispositif GaN HEMT présente de meilleures performances pour l'application automobile DC-DC proposée.

Conclusions Générales et Perspectives

La caractérisation des dispositifs à large bande interdite est importante pour mieux comprendre leurs caractéristiques électriques afin de développer des convertisseurs de puissance à haut rendement. Cette thèse a été principalement axée sur la caractérisation statique et dynamique des dispositifs SiC et GaN pour les applications automobiles, à savoir les convertisseurs DC-DC. De plus, les caractéristiques en commutation sont également vérifiées pour la validation du modèle SPICE. Quatre dispositifs différents (SiC et GaN) ont été choisis visant une tension nominale d'environ 400 V, valeur couramment utilisée pour l'alimentation des batteries. Les caractéristiques statiques et dynamiques ont été réalisées avec un Curve Tracer B1505A Keysight.

Pour étudier plus avant les principaux éléments pouvant contribuer aux transitoires de commutation, un PCB instrumenté pour le dispositif GaN Systems GS66516B a été développé. Le test à double impulsion a été effectué

afin d'obtenir les signaux de courant et de tension de l'interrupteur principal. Ce PCB offrait une interface pour connecter tous les instruments de mesure (sondes de tension, shunt et transformateur de courant) nécessaires à la validation du modèle d'appareil. De plus, les principaux éléments parasites ont également été analysés par des tests expérimentaux (avec un analyseur d'impédance E4990A) et de simulation. Par conséquent, l'inductance de la boucle de puissance/grille a été vérifiée en tant qu'éléments fondamentaux pour obtenir une simulation précise.

La validation du modèle pour les dispositifs SiC a été effectuée et a utilisé une carte d'évaluation de CREE. L'inductance parasite principale a été extraite à l'aide d'une méthode d'estimation étudiée grâce au PCB instrumenté développé. L'inductance puissance/boucle de grille est définie sur la base de la correspondance entre la simulation et les résultats expérimentaux.

L'estimation de la perte de commutation à l'aide d'un modèle validé de dispositif GaN Systems est effectuée. Les modèles d'instruments de mesure, les éléments de câblage et les modèles des dispositifs SPICE sont pris en compte pour la simulation. La méthode traditionnelle tension multipliée par le courant à la borne du commutateur, utilisée pour l'estimation deq perteq en commutation, pourrait générer des falses valeurs dues aux éléments capacitifs internes du dispositif d'alimentation. Ainsi, une méthode ne considérant que les éléments dissipatifs du commutateur a été mise en œuvre.

La comparaison entre différents dispositifs de puissance est généralement réalisée en utilisant différentes figures de mérite. Pour comparer les différents commutateurs utilisés dans cette thèse, une simulation est réalisée en considérant les mêmes valeurs pour l'inductance puissance/boucle de grille. Une comparabilité supplémentaire est obtenue en ajoutant un terme de perte de conduction, à savoir le FOM de commutation, ainsi le produit entre l'énergie de commutation totale et la résistance ON est tracé. Enfin, un convertisseur DC-DC typique est simulé pour chaque appareil cible sous différentes fréquences et niveaux de puissance.

La caractérisation statique et dynamique des dispositifs a permis de valider les modèles SPICE pour les utiliser en mode commutation. Ainsi, compte tenu de certains ajustements sur la tension de seuil, l'estimation de la perte

de commutation peut être effectuée en utilisant les modèles disponibles par le fabricant. Les mesures de température ambiante/haute ont montré une bonne corrélation avec les simulations effectuées dans LTspice. La relation entre la résistance ON et la température pour chaque technologie a démontré la forte dépendance à la température des dispositifs GaN.

L'analyse complète de l'impact des éléments parasites du câblage peut améliorer la précision de l'estimation des pertes de commutation. De plus, au moyen de résultats expérimentaux, la nécessité d'une bonne modélisation des instruments de mesures et d'un modèle 3D pour l'extraction parasitaire est vérifiée. Une simulation tenant compte de l'inductance de boucle de puissance/grille peut donner une bonne correspondance avec les données expérimentales. Cette approche a permis de valider tous les modèles SPICE utilisés dans les simulations, et ainsi de pouvoir évaluer plus précisément l'efficacité globale des convertisseurs de puissance à base de GaN.

Une étude sur les instruments de mesure utilisés pour les dispositifs WBG a permis de comprendre l'impact de chaque élément sur la charge du circuit. Un protocole clair pour la modélisation des instruments de mesure a été présenté. La vitesse de commutation rapide des dispositifs GaN nécessite cette modélisation pour obtenir une simulation précise. La comparaison entre la fiche technique, la simulation et les tests expérimentaux effectués a présenté une bonne corrélation par rapport aux caractéristiques d'impédance d'entrée, donc l'impédance vue par le circuit a pu être estimée dans une simulation globale. De plus, la réponse en fréquence des modèles a également été simulée pour comparer avec les limites de la fiche technique, en montrant une bande passante assez proche de la spécification des instruments de mesure.

Sur la base des résultats, il est raisonnable de considérer la simulation qui inclut l'inductance de boucle de puissance/grille extraite par ANSYS Q3D pour calculer les pertes de commutation. La modélisation des éléments parasites et des instruments de mesure a permis d'obtenir une bonne corrélation entre la simulation et les résultats expérimentaux. Le fait de ne pas utiliser la matrice Q3D complète contribue au temps de simulation.

La méthodologie du courant de mise sous tension, correspondant aux résultats de simulation et d'expérimentation, permet d'obtenir une erreur maximale

pour les pertes de commutation d'environ 12% pour les dispositifs GaN et 8% pour le SiC dispositifs. Concernant le facteur de mérite de commutation (FOM) et les résultats préliminaires, la comparaison des commutateurs montre que le dispositif GaN HEMT présente de meilleures performances pour l'application automobile DC-DC proposée.

L'étude réalisée dans cette thèse permet de mieux comprendre les principaux points à considérer pour obtenir une estimation précise des pertes de commutation. Des modèles validés par des résultats expérimentaux ont permis d'effectuer une simulation dans des conditions égales, concernant l'inductance puissance/boucle de grille, pour tous les dispositifs testés dans cette thèse. Ainsi, une étude comparative portant sur une application automobile pourrait être réalisée. Les pertes totales dans un convertisseur DC-DC typique sont utilisées comme paramètres comparatifs pour analyser les différentes performances des appareils WBG.

Concernant la caractérisation statique et dynamique, le développement constant de la technologie des dispositifs WBG nécessite que ces tests soient effectués en même temps, pour la température ambiante et la température maximale de jonction. Différents échantillons devraient être utilisés pour augmenter la fiabilité des mesures, principalement pour les dispositifs GaN, compte tenu de leur phase initiale de développement relative. Cependant une meilleure intégration des contraintes de fiabilité devrait être incluse dans le futur pour concevoir des convertisseurs de puissance fiables et efficaces.

Pour la caractérisation de la commutation, la condition idéale serait un PCB instrumenté pour chaque dispositif cible (SiC et GaN). Ainsi, une modélisation précise des éléments parasites pourrait être réalisée. La modélisation de l'instrument de mesure doit également être effectuée avec soin. Des tests de réponse en fréquence avec un VNA (Vector Network Analyzer) pourront améliorer les modèles développés.

Une plate-forme de test pour la caractérisation de la commutation où deux slots seraient utilisés, un pour les dispositifs (une branche, deux commutateurs) et un autre pour le circuit de commande, peut améliorer l'étude comparative entre les dispositifs WBG. Dans cette situation, les mêmes sondes de courant/tension pourraient être envisagées pour les mesures.

Concernant le convertisseur DC-DC pour les applications automobiles, un prototype final a été développé pour le dispositif GaN Systems GS66516B afin de valider l'estimation de la perte de commutation pour un cas optimal et non instrumenté. Sur la base d'une simulation validée, les pertes totales seraient calculées et comparées aux résultats de mesure. Cependant, en raison de certains problèmes et du manque de temps, la fabrication du convertisseur n'a pas été possible au cours de cette période de thèse.

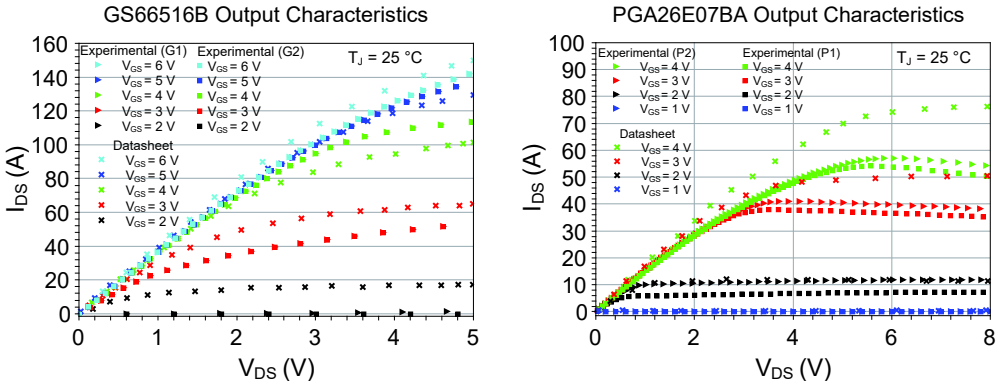
Certaines perturbations du signal obtenues par mesure n'ont pas été identifiées par l'analyse de modélisation et de simulation. L'analyse devrait probablement être étendue pour intégrer le courant de mode commun, en particulier pour le couplage entre le pilote de grille et son interrupteur de puissance associé.

ANNEX A

Output Characteristic for GaN Devices

A.1 GaN Systems and Panasonic - Different Samples

The output characteristics are overlaid for both samples to verify the equivalent behavior.



(a) (b)

Figure A.1: GS66516B (GaN Systems): (a) Output characteristics at ambient temperature ($T_J = 25\,°C$) for G1 and G2 samples. PGA26E07BA (Panasonic): (b) Output characteristics at ambient temperature ($T_J = 25\,°C$) for P1 and P2 samples.

ANNEX B

AC Current Probe

B.1 Current Transformer Modeling

In order to improve the Spice model used for transformer, an Eddy's current model is implemented [126]. By means of bond graph theory, the set of equations which represent a magnetic circuit can be used to build a bond graph model, Figure B.1 [127]. By this way, an electrical circuit can be achieved, as seen in Figure B.2.

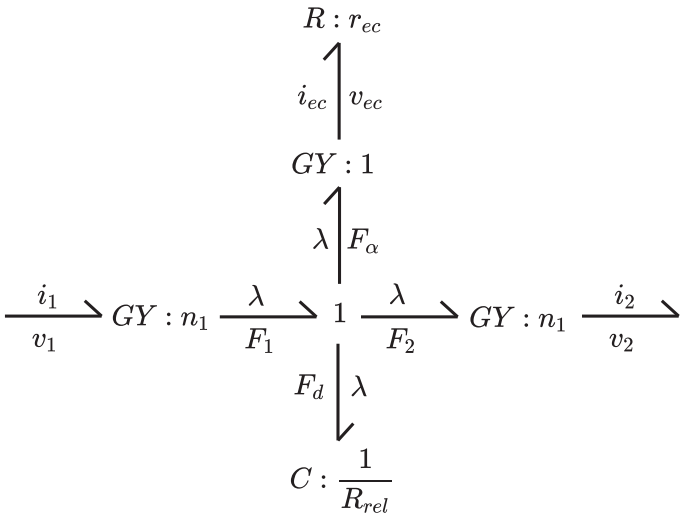


Figure B.1: Bond graph model with Eddy currents represented by a R-Element in the magnetic domain.

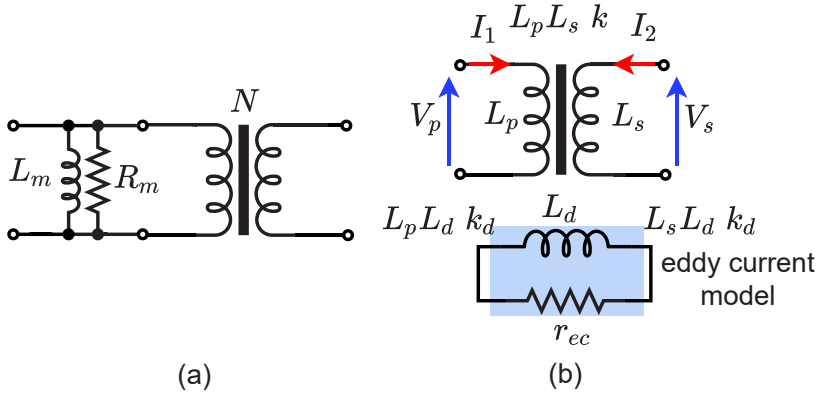


Figure B.2: (a) Circuit Spice model for a transformer and (b) considering the eddy current effect.

Initially, a low frequency model is developed for the current transformer based on the Ampere's theorem applied in Figure 4.28. The Equation (B.1) shows the DC resistance. The equivalent impedance of the circuit could be even performed by an extension towards medium frequency, as seen in Equation (B.2).

$$R_{DC} = \frac{R_{Leq}}{N^2}, \text{ with } R_{Leq} = R_L // R_{IN} \tag{B.1}$$

$$Z_{(\omega)} = \frac{V_p}{I_p} = \frac{jR_{DC}L_m\omega}{R_{DC} + jL_m\omega}, \text{ with } L_m = \mu_0\mu_r\frac{A_e}{L_e} \tag{B.2}$$

where R_{Leq} is the output equivalent resistance, N is the transformer turn ratio, R_L is the load resistor, R_{IN} is the scope input impedance, $V_{p,s}$ is the primary and secondary voltages, L_m is the magnetizing transformer inductance, μ_O is the air magnetic permeability, μ_r is the reversible magnetic permeability, A_e is the effective cross-section of the core and L_e is the effective length of the core.

For medium frequency, i.e a frequency higher than the low cutoff frequency of the probe, the impedance of the inductor is very high and it could be disconnect. Thus, the Equation (B.3) is obtained and it exhibits the voltage-to-current ratio of the probe (R_{probe}).

$$V_s = I_s R_{Leq} = I_p \frac{R_{Leq}}{N}, \text{ thus } R_{probe} = \frac{R_{Leq}}{N} \tag{B.3}$$

Calculating the low-frequency cutoff (f_L) when the frequency tends to zero, the following Equations B.4, B.5 and B.6 are obtained.

$$Z_0 = \lim_{\omega \to \infty} Z(\omega) = R_{DC}, \text{ therefore: } |Z(2\pi f_L)| = |Z(\omega)| = \frac{R_{DC}}{\sqrt{2}} \tag{B.4}$$

$$\left| \frac{j R_{DC} L_m \omega}{R_{DC} + j L_m \omega} \right| = \frac{R_{DC} L_m \omega}{\sqrt{R_{DC}^2 + L_m^2 \omega^2}} = \frac{R_{DC}}{\sqrt{1 + \dfrac{R_{DC}^2}{L_m^2 \omega^2}}} = \frac{R_{DC}}{\sqrt{2}}, \text{ so, when: } \frac{R_{DC}}{L_m \omega} = 1, \tag{B.5}$$

$$\text{that means: } 2\pi f_L = \omega = \frac{R_{DC}}{L_m}, \text{ finally: } f_L = \frac{R_{DC}}{2\pi L_m} \tag{B.6}$$

ANNEX C

Transmission Line and Oscilloscope Circuit

C.1 Transmission Line and Oscilloscope Circuit

The delay caused by a probe relies on the number of RLC cells, therefore it is related to the length of the cable. The propagation speed of traveling waves through the transmission line is defined by Equation (C.1) and can be deduced from the Telegrapher's equations [128].

$$u = \frac{1}{\sqrt{L_L C_L}} \tag{C.1}$$

Where L_L and C_L represent the inductance and capacitance of the cable. With the propagation speed calculated and knowing the cable length l and its wavelength λ, the delay due to the probe can be estimated by using Equation (C.2).

$$\lambda = uT \;\Rightarrow \tau = \frac{l}{u} \tag{C.2}$$

A transmission line is a long structure of conductors carrying a current. The

length of the transmission line must be considered due to its influence on the signal delay. In Figure C.1, a simplified model representing a transmission line is shown and used to the input impedance calculation.

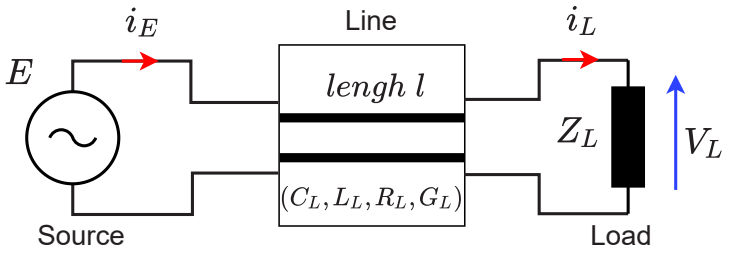


Figure C.1: AC powered line.

The theory behind the Telegrapher's equations can also be used to develop Equation (C.3) for input impedance of a cable. In Equation (C.4), the characteristic impedance is defined as a complex number, thus, following a good approaching, it is possible to simplify this model by doing the resistance and conductance equal to zero [104]. The cable used to voltage probes has a characteristic impedance of $50\,\Omega$ [104]. In Equation (C.5) is defined the propagation constant, being a complex number involving the characteristic variables of the transmission line [128].

$$Z_{IN} = Z_0 \left(\frac{Z_L + Z_0 tanh\,(\gamma l)}{Z_0 + Z_L tanh\,(\gamma l)} \right) \tag{C.3}$$

$$Z_0 = \sqrt{\frac{R_L + j\omega L_L}{G_L + j\omega C_L}} \tag{C.4}$$

$$\gamma = \sqrt{(R_L + j\omega L_L)\,(G_L + j\omega C_L)} \tag{C.5}$$

In the case of a lossless line, the terms R_L and G_L, resistance and conductance respectively, are null. Defining an angle $\theta = 2\pi l/\lambda$ and knowing that $\lambda = 2\pi u/\omega$, the relation $\theta = \omega l/u$ can be written, which yields an explicit expression of θ with respect to the frequency. Therefore, the Equation (C.3) can be rewritten as Equation (C.6).

$$Z_{IN}^{LL} = Z_{00}\left(\frac{Z_L + jZ_{00}tan\,(\theta)}{Z_{00} + jZ_L tan\,(\theta)}\right) \tag{C.6}$$

From this transmission line model of the case lossless, a simplified lossy input impedance can be written, by adding a resistive term, as shown in Equation (C.7).

$$Z_{IN}^{S} = Z_{IN}^{LL} + R_L l \tag{C.7}$$

To validate the SPICE transmission line model, a comparison of the input impedance (Z_{IN}), the simplified input impedance (Z_{IN}^{S}) and the LTRA (Lossy Transmission Line) model found in SPICE library (Z_{SPICE}) is performed to two different sort of cables [129, 130]. The first one is a RG-58 cable used to shunt resistor probes and AC current probes. The results can be seen in Figure C.2. A good correlation between the graphs (analytical and SPICE models) can be seen, thus, the SPICE model can be used for probes simulation. In Figure C.3, a mismatch about the simplified model and SPICE model is found, that is due to the higher resistance of coaxial cables used to voltage probes. Thus, it is possible to conclude that if the model deals with a low resistive cable, the simplified model is adequate, but in the case of a high resistive cable, it is necessary to use the overall transmission lines model to take into account conduction losses. Regardless, the LTRA SPICE model for transmission lines presents a good correlation with the analytical model.

A simulation in the time domain is also performed to verify the response of LTRA SPICE model regarding the delay and voltage attenuation. The validation is achieved by comparison with the Pi network model for the transmission line, given that this model represents the numerical discretization of the Telegrapher's equations [131]. In Figure C.4, the Pi-model response for different cells number can be seen. The delay of the cable should match with the theoretical value, given by the Equation (C.2).

The scope circuit for the high impedance mode is represented by a capacitor and resistor in parallel, for the low impedance mode only resistor can be used to the input circuit. In Figure C.5, an attenuator and amplifier system can

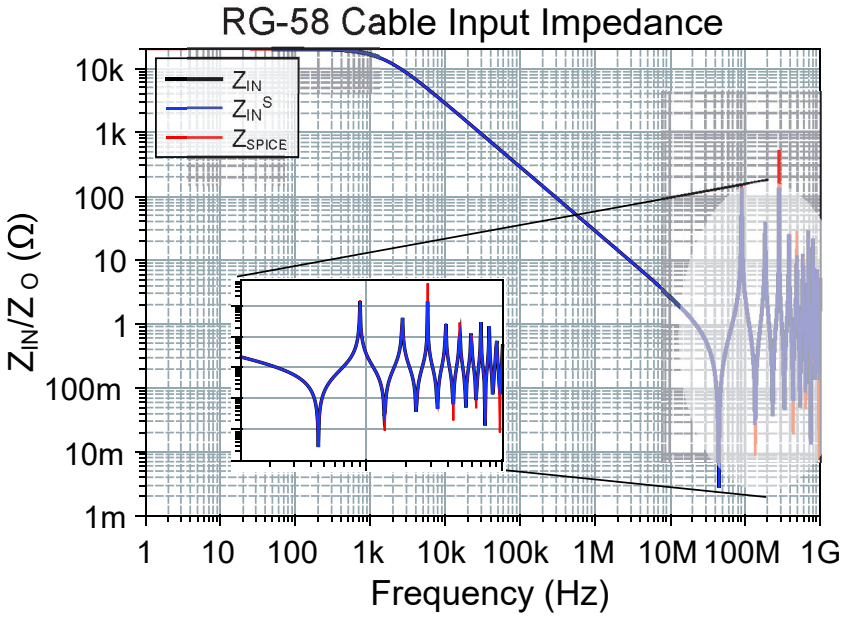


Figure C.2: Comparison of the input impedance (Z_{IN}), simplified model (Z_{IN}^{S}) and SPICE model (Z_{SPICE}). The result is standardized by $50\,\Omega$. For the load, values used are $R_S = 1\,M\Omega$ and $C_S = 16pF$.

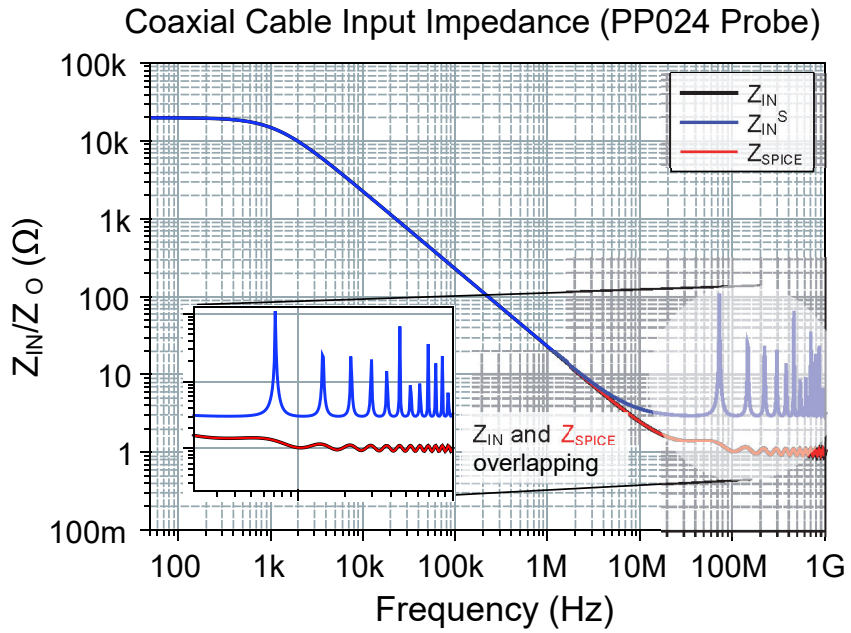


Figure C.3: Comparison of the input impedance (Z_{IN}), simplified model (Z_{IN}^{S}) and SPICE model (Z_{SPICE}). The result is standardized by $50\,\Omega$. For the load, values used are $R_S = 1\,M\Omega$ and $C_S = 16pF$.

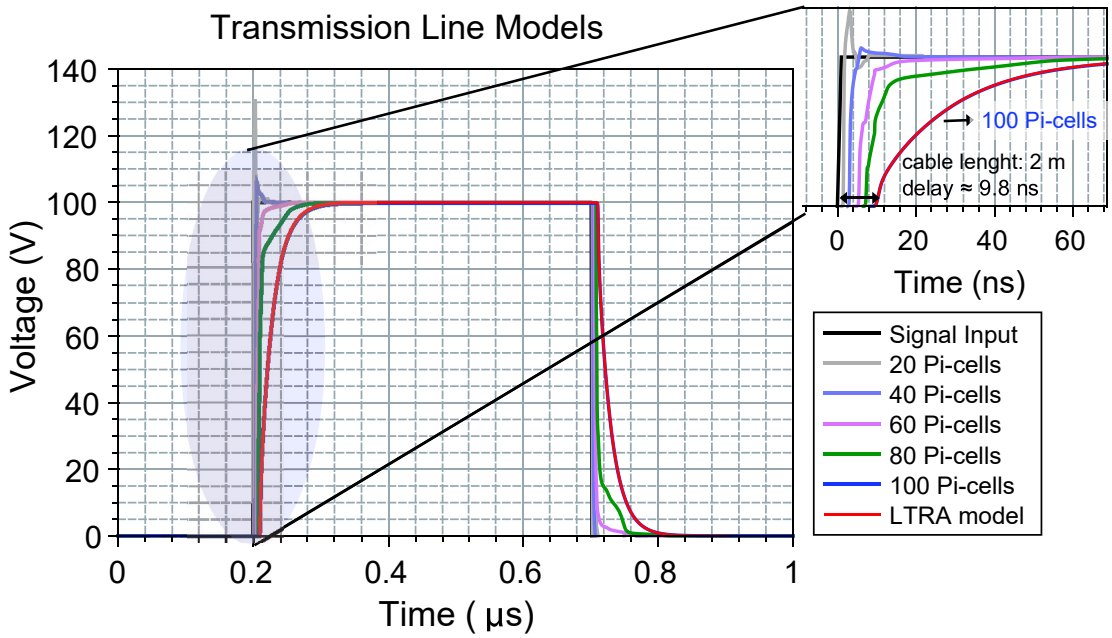


Figure C.4: Simulation of LTRA SPICE model and Pi-model for the transmission line.

be seen and they are used to ensure a maximum resolution signal towards the Analog-to-digital Converter (ADC) range. A switch inside the oscilloscope allows selecting between high impedance, when used to maximize the voltage for low speed signals, and 50 Ω impedance, used to minimize reflections caused when high speed signals are measured [114]. In case of low impedance mode selection, the capacitance value of the operational amplifier is considerably lower than the capacitance of the high impedance mode. Hence, its parasitic value can be neglected [104, 111].

Concerning the right use of an oscilloscope, a bandwidth frequency of five times greater than the frequency of the waveform being measured should be used [104, 111], besides that a high resolution is mandatory, mostly when devices under tests have high switching frequency, such as SiC and GaN components [5]. The rise time is also important to ensure an accurate measure, seen that for a cascading system, the impulse response is given by the convolution of the signals, Equation (C.8) [104, 111].

$$t_{rise} = \sqrt{t_{r,signal}^2 + t_{r,probe}^2 + t_{r,amp}^2} \tag{C.8}$$

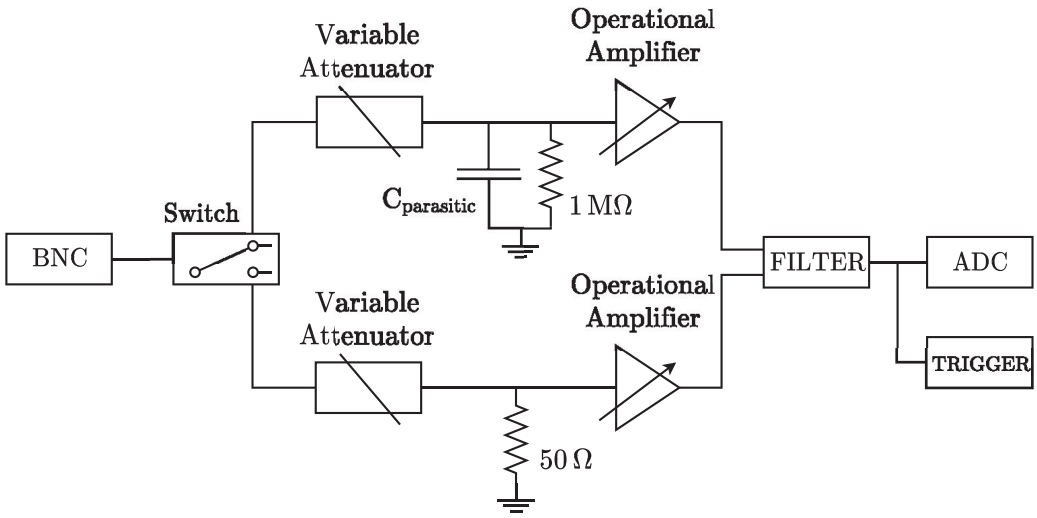


Figure C.5: Simplified electrical circuit for general oscilloscope adapted from [111].

Where $t_{r,signal}$, $t_{r,probe}$ and $t_{r,amp}$ are, respectively, the rise time added due to the measured signals, voltage probe and scope operational amplifier. The more stages are connected between the device under test and scope, the higher is the total time delay.

The sampling rate and bandwidth determine the faster switching transient that can be accurately measured. The primary frequency component can be estimated from the rise time of the signal being measured, according to the Equation (C.9). It recommends using an instrumentation that exceeds that bandwidth by a factor of three [99].

$$f_{(-3\text{dB})} = \frac{0.35}{min(t_r, t_f)} \tag{C.9}$$

Where $min(t_r, t_f)$ is the minimum value between rise and fall time of the measured signal.

Once the oscilloscope and probe are selected, the compensation of the measurements circuit in the oscilloscope should be performed, thought the turning capacitors used to compensate cable effect and scope input impedance.

ANNEX D

Switching Validation - ISOVU Probe

D.1 Gate Source Voltage of the High Side Switch

The high side switch of the leg-inverter circuit DPT is not isolated, thus a passive probe used for measurement would generate a short-circuit on the switch terminals. To solve this issue, differential ISOVU probe TIVH08/TIVH08L is used. The results for different voltage operation points are shown in Figure D.1.

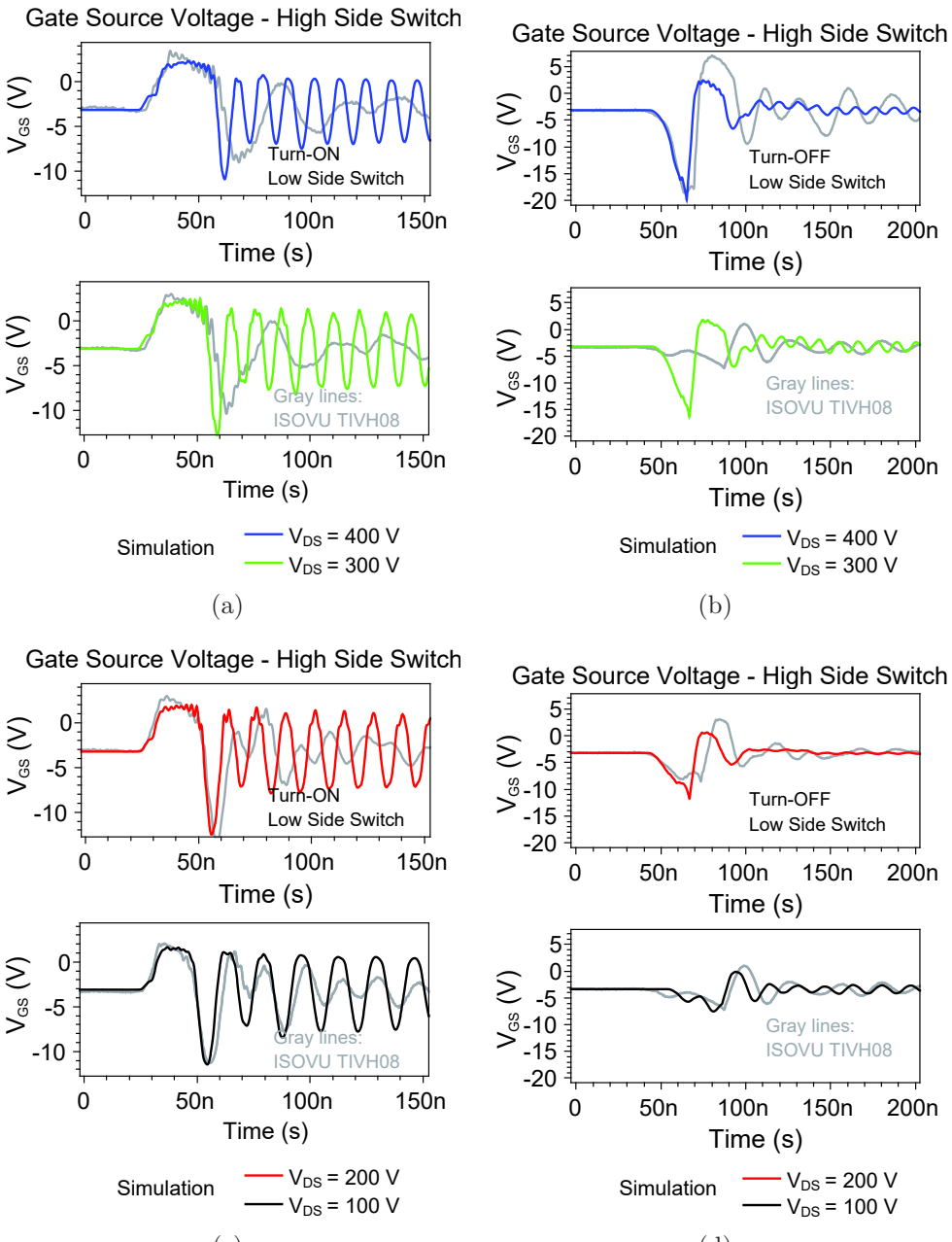
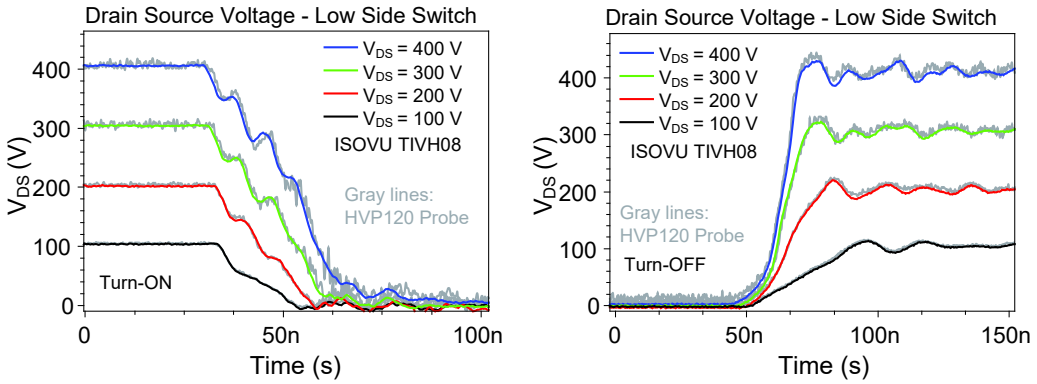


Figure D.1: Gate source voltage (V_{GS}) on high side switch measured by ISOVU TIVH08 at different drain source voltage (V_{DS}). The simulation is overlapped the experimental results.

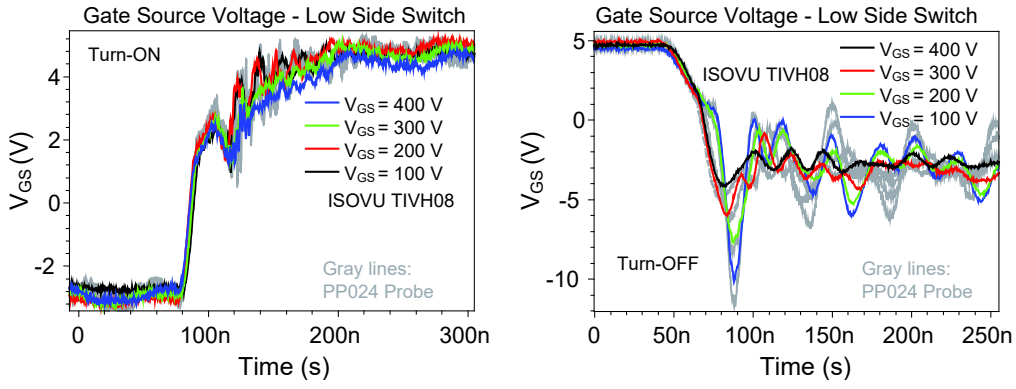
D.2 Comparison with HVP120 Voltage Probe

To verify the difference between passive and isolated probes for measurement of the low side switch voltage, both results are overlapped, as seen in Figure D.2 and Figure D.3 for drain and gate source voltage, respectively.



(a) (b)

Figure D.2: (a) Turn-ON and (B) turn-OFF drain source voltage comparison between experimental values of HVP120 passive probe and ISOVU TIVH08 for GaN Systems devices.



(a) (b)

Figure D.3: (a) Turn-ON and (B) turn-OFF gate source voltage comparison between experimental values of HVP120 passive probe and ISOVU TIVH08 for GaN Systems devices.

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : SOARES DE OLIVEIRA
(avec précision du nom de jeune fille, le cas échéant)

DATE de SOUTENANCE : 24/11/2021

Prénoms : Joao André

TITRE : A Methodology for Designing SiC and GaN Device Based Converters for Automotive Applications

NATURE : Doctorat

Numéro d'ordre : 2021LYSEI084

Ecole doctorale : EEA 160

Spécialité : Génie Electrique

RESUME :
Wide band-gap (WBG) devices enable power converter designs at higher frequency, power density, and efficiency, as compared to silicon-based converters. The coexistence for SiC (Silicon Carbide) and GaN (Gallium Nitride) devices in the ranges 600-900 V motivates a specific study of these components and the development of methods to perform better selection relying on the application, particularly for automotive applications. The proposed methodology starts with static and dynamic tests performed on SiC and GaN devices to validate their models. GaN power devices allow the building of the most integrated converters. Here, an instrumented PCB (Printed Circuit Board) is developed to measure and estimate switching losses including the measurement points needed for this purpose. The parasitic elements of the PCB layout extracted by ANSYS Q3D and the measurement instrument models are also included in the simulation model. Thus, by means of an experimentally validated model, it will be possible to evaluate the total losses in an optimized circuit without probes. Meanwhile, for SiC devices, an evaluation board is used, and an estimating method for inductance parasitic extraction is performed. The switching loss estimation is an important step for power converter design. Moreover, the consequences of faster switching on the gate driver design and board layout generate new challenges for WBG-based converters. An accurate switching loss estimation is a helpful step because it allows for the adjustment of different circuit layouts based on the simulation results. However, the instrumented PCB does not predict the switching losses in an optimized converter, but only on the instrumented PCB. The simulation enables the prediction of switching losses in more realistic converters. Finally, a simulation for each target device (SiC and GaN) is developed considering the main parasitic elements and the measurement instrument models. Thus, the switching losses are computed and compared to experimental results. Since the whole system is validated, to compare the SiC and GaN devices for automotive applications, an optimized DC-DC converter simulation is used for comparing each device under different operation points of the converter.

MOTS-CLÉS : GaN HEMT, SiC Devices, Switching Loss Estimation, Automotive Applications.

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