Design of a continuous time Delta-Sigma modulator for energy measurement using diamond detectors

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THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITE GRENOBLE ALPES

Spécialité : **NANO ELECTRONIQUE ET NANO TECHNOLOGIES**
Arrêté ministériel : 25 mai 2016

Présentée par

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préparée au sein du **Laboratoire de Physique Subatomique et Cosmologie de Grenoble (LPSC)**
dans **l'École Doctorale Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)**

Conception d'un modulateur Delta-Sigma à temps continu pour la mesure d'énergie utilisant des détecteurs diamant

Design of a continuous time Delta-Sigma modulator for energy measurement using diamond detectors

Thèse soutenue publiquement le **28 octobre 2021,**
devant le jury composé de :

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"To the courage of my Dad
The wisdom of my Mum
The ambitions of my Brothers
and the childish curiosity that is living within all of us.."

Acknowledgments

Throughout the writing of this dissertation, I have received a great deal of support and assistance. Our prophet Mohammed (peace be on him) said: He, who does not thank people, does not thank Allah (narrated by Ahmad and Tirmidhi).

I would first like to thank my advisors, Doctor Fatah-Ellah RARBI and Professor Olivier ROSSETTO, your expertise was invaluable in formulating the research questions and methodology. Your insightful feedback pushed me to sharpen my thinking and brought my work to a higher level. I am grateful to have the opportunity to work with both of you; I will never forget all your advises, discussions, jokes and moments of challenges, you made me love science more and more.

Besides my advisors, I would like to thank the rest of my thesis committee: Professor DALLET Dominique, Professor UHRING Wilfried, Professor BOURDEL Sylvain and Doctor DE LA TAILLE Christophe, for their insightful comments and encouragements, but also for the original questions, which incented me to widen my research from various perspectives.

My sincere thanks also goes to Doctor Marie-Laure GALLIN-MARTEL, Engineer Laurent GALLIN-MARTEL, Doctor Denis DAUVERGNE, and all theirs students and PhD candidates for the great discussions and clear explanations about Diamond detectors.

I would like to acknowledge my colleagues from the electronics departments in the LPSC, for their wonderful collaboration. I would particularly like to single out Mahfoud YAMOUNI, Emmanuel TOURBA, Jean-pierre SCORDILIS, Nicolas PONCHANT, Joel BOUVIER, Germain BOSSON, Yvan ODIEVRE, and Thierry DESCOMBES. Without you, things would not be that interesting, is not it?

I would also like to thank the youngsters in our department; the new engineers Julien BOUNMY and Oumaima JAAFOURA. Those who went for new adventures; Theo MABILON and Lucas TRIBOUILLOY (We still playing online games, right?).

In addition, my warmth thanks to all the students and colleagues from the administration and other departments (Special thanks to Thierry LAMY, Denis GRONDIN, Emmanuelle VERNAY, Audrey COLAS and Christine SERVOZ-GAVIN), my PhD candidate mates from the BIDUL Club and the communication department of CNRS ALPES and UGA Grenoble.

Moreover, I would like to thank my parents for their wise counsels and sympathetic ear. You are always there for me; your words never let me down in the hardest moments, thank you! To my brothers Hocine, Taqi-Eddine and BENBOUDIAF Merwan, I believe in you as much as you believe in me! Finally, I could not have completed this dissertation without the support of my friends, here in Grenoble: Mustapha TOUHAMI, Wissam BENJILALI, Mounder KOUICEM, Abdel-mounain AHMINE, Mohamed ZELOUFI, Hamza RIHANI, Housseyne NADOUR, Nassim LOUKKASS, Hadj MAHBOUBI and his wife, YOU ARE MY FAMILY HERE! My friends in others cities and countries Rafik SAAD, Younes AGGOUN (This man took the plane and came to my defence from TUNISIA! Man you made my day!), BOUCHAMA Abdelbari, BOKHARI Lamine, LYAMSI Ismail, MANSER Belkacem, Yacine and finally to the spirit of imagination, love and laugh D.A.R Aggy. All of you provided stimulating discussions as well as happy distractions to rest my mind outside of my research (w kess JUS).

I would not forget all the great people who keep inspiring me and making me enjoying the adventure of science: Nicola TESLA, Isaac NEWTON, Albert EINSTEIN, Carl Friedrich GAUSS, Muhammad Ibn Mūsā AL-KHUWĀRIZMĪ, Leonardo da VINCI, Behzad RAZAVI, Boris MURMANN, and the entire curious scientists from different eras who are seeking the knowledge through hard work and effort: "If I have seen further it is by standing on the shoulders

of Giants."[1]

[1] Isaac Newton

Conception d'un modulateur Delta-Sigma passe bas à temps continu pour la mesure d'énergie en utilisant des détecteurs diamant

Résumé

La conception des convertisseurs analogique numérique de type Delta-Sigma à temps continu est souvent considérée comme complexe et difficile. Elle nécessite des connaissances, de l'intuition, de la créativité et de l'expertise technique. Jusqu'à présent, ce type d'architecture n'apparaît pas dans le domaine de la conception des circuits électroniques intégrées pour la détection de particules. Pourtant, nous pensons qu'il peut apporter des solutions intéressantes, comme nous allons le montrer dans le cas des systèmes de mesure d'énergie.

Ce travail de thèse s'inscrit dans le cadre d'un projet de recherche intitulé DIAMASIC. Le but est de développer une électronique de lecture intégrée d'un système de détection hodoscope utilisant des détecteurs diamant dans le cadre de monitorage de faisceaux pour le traitement de tumeurs par hadronthérapie. Ce système doit permettre un étiquetage spatio-temporel des particules utilisées connu sous le nom « hadron » pour garantir la sécurité du patient pendant ce type de traitement. Cette électronique est composée de deux parties : un système de mesure de temps et un système de mesure d'énergie. Le design de ce dernier nécessite la conception d'un CAN.

Ce manuscrit synthétise les travaux de modélisation, conception et simulation d'un modulateur Delta-Sigma passe-bas à temps continu avec une bande passante de 10MHz (Peut atteindre 40 MHz) et visant une résolution de 8bits avec une consommation raisonnable. Dans un premier temps, nous avons réalisé une analyse des architectures possibles des différents modulateurs pour arriver à garantir le cahier des charges voulu. Suite à cette étude, nous avons proposé une topologie d'un modulateur de type CRFF "Cascaded Resonator Feed-Forward" du cinquième ordre avec un quantificateur interne d'une résolution de 3bits et un taux de sur-échantillonnage de 8. Pour valider ces choix et étudier l'impact des imperfections liées à chaque bloc, nous avons développé une méthodologie de modélisation basée sur le paradigme connu sous le nom du Model-Based Design (MBD) via des modèles graphiques SIMULINK et des scripts MATLAB. Cette approche nous a permis de spécifier les performances de chaque partie du modulateur et aussi de faire des optimisations en termes de complexité, stabilité et consommation. Les données extraites de la partie de modélisation sont utilisées dans la phase d'implémentation en technologie CMOS 130nm. Le dimensionnement théorique des transistors est réalisé en utilisant la méthodologie gm/Id. Les détails de cette méthode sont discutés pour la conception des amplificateurs utilisés dans le filtre de la boucle. Les résultats de différentes simulations électriques sont présentés, elles montrent que l'architecture proposée atteint une résolution de 8bits dans une bande passante de 10 MHz.

Finalement, une comparaison entre les résultats de modélisation et les différentes simulations électriques sur CADENCE a été présentée et l'écart de performance est discuté avec des propositions d'amélioration avant la fabrication du circuit.

Mots clés : Hodoscope, Diamant, détection des particules, circuit analogique, CAN, Delta-Sigma, temps continu, MBD.

Design of a continuous time low-pass Delta-Sigma modulator for energy measurement using diamond detectors

Abstract

The design of continuous-time Delta-Sigma analog-to-digital converters is often considered complex and difficult. It requires knowledge, intuition, creativity and technical expertise. Up to now, this type of architecture does not appear in the field of designing integrated electronic circuit for particle detection. However, we believe that it can provide interesting solutions, as we will show here in the case of energy measurement systems.

This thesis work is part of a research project entitled DIAMASIC. The aim is to develop an integrated readout electronics of a hodoscope detection system using diamond detectors in the context of beam monitoring for the treatment of tumors using hadrontherapy. This system must allow a spatio-temporal tagging of the used particles known as "hadron" to guarantee the safety of the patient during the treatment. This electronics is composed of two parts: a time measurement system and an energy measurement system. The design of the latter requires an ADC.

This manuscript synthesizes the modeling, design and simulation of a continuous-time low-pass Delta-Sigma modulator with a bandwidth of 10MHz (can reach 40 MHz) and targeting a resolution of 8bits with a reasonable power consumption. The first step was to analyze the possible architectures of different modulators in order to guarantee the desired specifications. Following this study, we proposed a topology for a fifth order CRFF (Cascaded Resonator Feed-Forward) modulator with an internal quantizer of 3 bits resolution and an oversampling rate of 8. In order to validate these choices and to study the impact of the imperfections linked to each block (non-idealities), we have developed a modeling methodology based on the paradigm known as Model-Based Design (MBD) through the use of SIMULINK graphical models and MATLAB scripts. This approach permitted us to specify the capabilities of each part of the modulator and also to make optimizations in terms of complexity, stability and power consumption. The data extracted from the modeling part are used in the implementation phase in a 130nm CMOS technology. The theoretical sizing of the transistors is done using the gm/Id methodology. The details of this method are discussed for the design of the amplifiers used to build the integrators of the loop filter. The results of different electrical simulations are presented, they show that the proposed architecture reaches a resolution of 8bits in a bandwidth of 10MHz.

Finally, a comparison between the modeling results and the different electrical simulations on CADENCE has been presented and the performance gap is analyzed and some solutions are proposed aiming for improvements before the fabrication of the circuit.

Keywords : Hodoscope, Diamond, particle detection, analog circuit, ADC, Delta-Sigma, Continuous time, MBD.

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List of Acronyms

$\Delta\Sigma$	delta-sigma
AAF	anti-aliasing filter
ADC	analog to digital converter
CM	common mode
CMOS	complementary metal-oxide-semiconductor
CT	continuous time
CT-DT	continuous time to discrete time
CVD	chemical vapor deposition
DAC	digital to analog converter
dB	decibel
dBFS	decibels relative to the full-scale input signal
DEM	dynamic element matching
DNL	differential non linearity
DR	dynamic range
DSP	digital signal processor
DT	discrete time
DWA	data weighted averaging
ENOB	effective number of bits
ELD	excess loop delay
FFT	fast Fourier transform
FoM	figure of merit
FS	full scale signal range (peak-to-peak)
GBW	gain bandwidth product
HD	harmonic distortion
IBN	in band noise
IC	integrated circuit
INL	integral non linearity

LP	low pass
LSB	least significant bit
MASH	multistage noise shaping
MIP	minimum ionizing particle
MSA	maximum stable amplitude
MSB	most significant bit
NMOS	N-type metal-oxide-semiconductor
NTF	noise transfer function
NRZ	non return to zero
OAR	organs at risk
Opamp	operational amplifier
OSR	oversampling ratio
pCVD	polycrystalline CVD
PDF	probability density function
PMOS	P-type metal-oxide-semiconductor
PSD	power spectral density
PVT	power voltage temperature
RMS	root mean square
RZ	return to zero
S/H	sample and hold
SAR	successive approximation register
sCVD	single crystal CVD
SFDR	spurious free dynamic range
SNR	signal to noise ratio
SNDR	signal to noise and distortion ratio
SQNR	signal to quantization noise ratio
SR	slew rate
STF	signal transfer function
THD	total harmonic distortion
TIA	Transimpedance amplifier

Introduction

"If you want to find the secrets of the universe, think in terms of energy, frequency and vibration."

— Nikola Tesla, inventor and engineer

DIAMOND is a large gap semiconductor material with very interesting physical properties for particle detection. This new generation of detectors is intended to be used for the design of a beam hodoscope with very high temporal resolution in the context of improving the performance of online monitoring systems in hadrontherapy. This latter is a novel cancer treatment method that proposes to use, in a number of clinical situations, light ion beams instead of X-ray beams as a means of irradiating tumors. It allows to generate advantageous dose deposition profiles compared to the X-ray beams used in the conventional radiotherapy. This dose deposition is described as a sharp profile in depth and called Bragg peak. Yet, this treatment method suffers from uncertainties about the actual path of the ions in the patient which is dangerous. Thus, various research groups are working to develop methods for online verification and monitoring of ion beams pathways.

In this context, the national collaboration CLaRyS[1] is developing detection methods for the online monitoring of ion pathways. The particularity of the work of this collaboration is that it proposes to add a beam hodoscope to the already developed gamma cameras. Its main goal is providing a spatial and temporal tagging of the used ion beams. Spatial tagging allows to obtain an image of the beam cross section and brings complementary information for the image reconstruction of the treatment. Temporal tagging enables an efficient rejection of the background noise caused by the detection of other secondary particles by the gamma cameras (mainly neutrons) by measuring the time difference between the moment of detection of the photon by the camera and that of the ion by the hodoscope. A temporal resolution of the order of 100 *ps* should be achieved to improve the efficiency and sensitivity of the monitoring system. This performance is not achievable with the classic scintillating fibers hodoscope. The collaboration has therefore chosen to develop a new hodoscope based on CVD (Chemical Vapor Deposition) diamond detectors.

Within the framework of these developments, DIAMASIC project is founded to build the custom integrated read-out electronics of this CVD diamond hodoscope. The final circuit is a multichannel ASIC composed of two systems: a time measurement system with a timing resolution of less than 100 *ps* and an energy measurement system based on an innovative ADC architecture. The developments presented in this dissertation are a part of the DIAMASIC project, it was carried out in the electronic department of the Laboratory of Subatomic Physics and Cosmology (LPSC) of Grenoble. It focuses on the modeling and the design of an ADC based on a continuous time low-pass Delta-Sigma modulator for the energy measurement system with a

[1] CLaRyS stands for "Contrôle en Ligne de la hAdronthérapie par détection de RaYonnements Secondaires", it is composed of four laboratories: le Laboratoire de Physique Subatomique et de Cosmologie (LPSC) de Grenoble, l'Institut des Deux Infinis de Lyon (IP2I Lyon), le Centre de Physique des Particules de Marseille (CPPM) et le Centre de Recherche en Acquisition et Traitement de l'Image pour la Santé (CREATIS) de Lyon.

bandwidth of 10 MHz (can reach 40 MHz), and targeting a resolution of 8 bits with a reasonable power consumption. This dissertation is organized as follows:

Chapter 1 describes the targeted medical application and the use of CVD diamond detectors. It starts with an introduction to the principles of hadrontherapy and the need of an hodoscope, followed by details about CVD diamond detectors and its response. The desired requirements of the ASIC are explained with emphasis on our contribution and results in the design of the timing measurement system. The chapter concludes with an explanation about the motivation to explore a new architecture for the energy measurement system.

Chapter 2 explains the basics of the analog to digital conversion and introduces the delta-sigma architecture and its features. At the beginning of this chapter, ADC performance metrics are illustrated followed by an analysis of its two classes: Nyquist-rate converters and over-sampling converters. After that, the principle of delta-sigma modulator is shown with a focus on its fundamental parameters. The two types of Delta-Sigma modulators, DT and CT, are then described and compared. The chapter concludes with a presentation of the different kinds of implementing high order modulators and the benefits of each one.

Chapter 3 deals with the system-level modeling and the use of the model-based design paradigm. A proposed workflow for the design of the CT modulator based on this approach is detailed and explained. At first, a block diagram of the chosen topology is introduced with the targeted specifications. Then, the integration of Schreier's toolbox is explained using a combination of MATLAB scripts and SIMULINK graphical models. Different scripts starting from synthesizing the modulator by calculating the various coefficients related to each stage, then followed by analyzing its behavior against different non-idealities of each building block are illustrated. The chapter concludes with an interpretation of the results of all these simulations.

Chapter 4 describes the transistor-level implementation using the g_m/I_d design methodology. It starts with an introduction of this methodology and its integration in our proposed workflow. An illustration of this step is discussed through the sizing of the amplifier used in building the various integrators of the modulator. Results of sizing and electric simulations of the loop filter in CADENCE are shown and discussed. The performances of the loop quantizer and the feedback DAC are analyzed as well. The chapter concludes with an examination of the performances of the proposed modulator and a comparison with the modeling results.

The dissertation ends with a general conclusion of the overall work performed during this thesis and makes suggestions for future work.

1 Overview of the application

In this chapter, the medical application of the designed readout electronics and its specifications are introduced. Details about this therapy, the technology of the detector and both timing and energy measurement systems are presented.

Contents

1.1 Hadrontherapy

1.1.1 Principles and challenges

Cancer is an uncontrolled growth of cells, which can invade and spread to distant sites of the human body. Cancers have severe health consequences and are leading cause of death. Early detection, accurate diagnosis, and effective treatments are key issues for cancer survival rates.
The three treatment options available today are surgery, chemotherapy and radiotherapy. In conventional radiotherapy, X-ray photons are used to deposit an accurate dose to the tumor. The major constrain in radiotherapy, is to spare the healthy tissues of the patient from the radiation and target directly the cancerous cells. As we see in figure 1.1 [1](depth curves are generally used to compare different types of techniques, this illustrates the evolution of the dose deposition of different particle beams as a function of the depth of interaction in the tissue, here, in water). X-rays deposit their energy and release the dose close to the surface of the target, we notice as well that the shape of the relative dose is not selective. Photons of higher energy, 6 to 18 MeV have more relative dose and a better penetration in the patient's body. With the progress in the nuclear science, charged particles (protons and carbon ions) known also as hadrons are aimed to be used in cancer treatment. These particles have a better dosage deposit location by comparison with the photons. They leave maximum of their energy at the end of their trajectory, which is known as the Bragg peak.

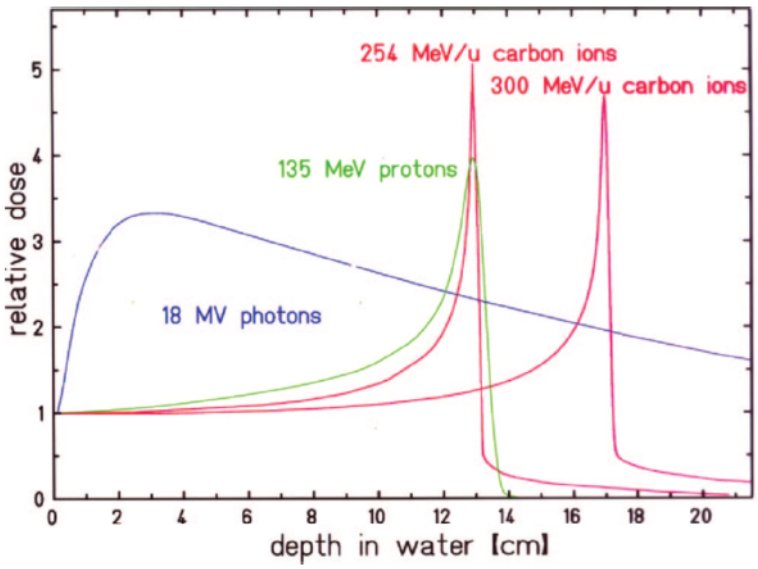

Figure 1.1: Comparison of the deposited dose yield of different ions in depth, extracted from [1].

The position of this pic can be controlled through the initial energy of the ions as shown in figure 1.2 [2].

From this, hadrontherapy is defined as a non-invasive external radiotherapy technique using light ion beams as a means of irradiating tumors. Thus, although figure 1.1 shows that the Bragg peak can be defined at an exact point, it is never really the case because of the statistical fluctuations on the path of the ions. The ion beams suffer from a longitudinal and transverse spatial dispersion governed by the so-called *straggling* [2].

Also, it should be noted that if the Bragg peak generated by a monochromatic ion beam is defined on a small thickness, the tumor volume to be treated can be several centimeters in diameter. In order to be able to irradiate uniformly the whole tumor volume, a spread-out Bragg peak (SOBP) is used as shown in figure 1.3. Several ion beams with decreasing energies are used to scan the tumor in depth from the distal peak (blue Bragg peaks in the figure).

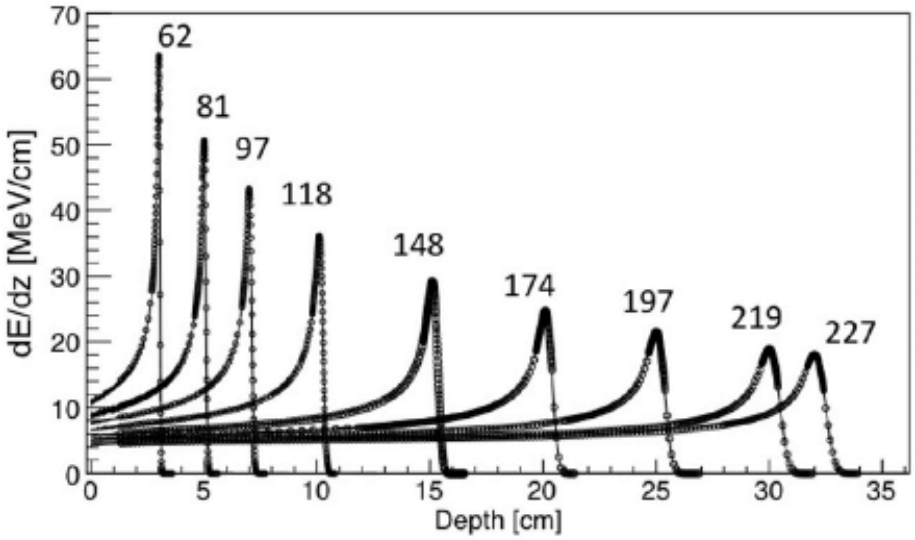

Figure 1.2: Evolution of the Bragg peak depth as a function of the initial energy (in MeV) of protons in water, extracted from [2].

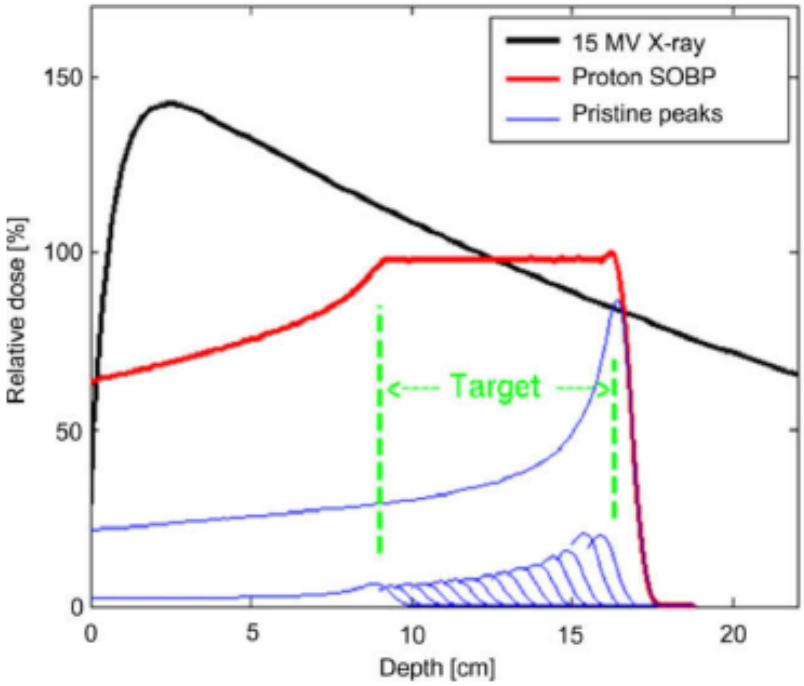

Figure 1.3: Illustration of the implementation of the spread-out Bragg peak, extracted from [3].

Although hadrontherapy represents an alternative solution to conventional radiotherapy that can be very interesting from a clinical point of view, its concrete implementation is not so ideal as shown above. One of the main limitations of hadrontherapy, is that it is not used to its full potential because of uncertainties about the path of the ions in the patient. Some of these uncertainties are inevitable and/or systematic and others are subject to possible improvement. An example of this problematic is shown in figure 1.4. It is assumed here that a tumor has developed in the patient's lung, close to the heart, which is an organ at risk (OAR).

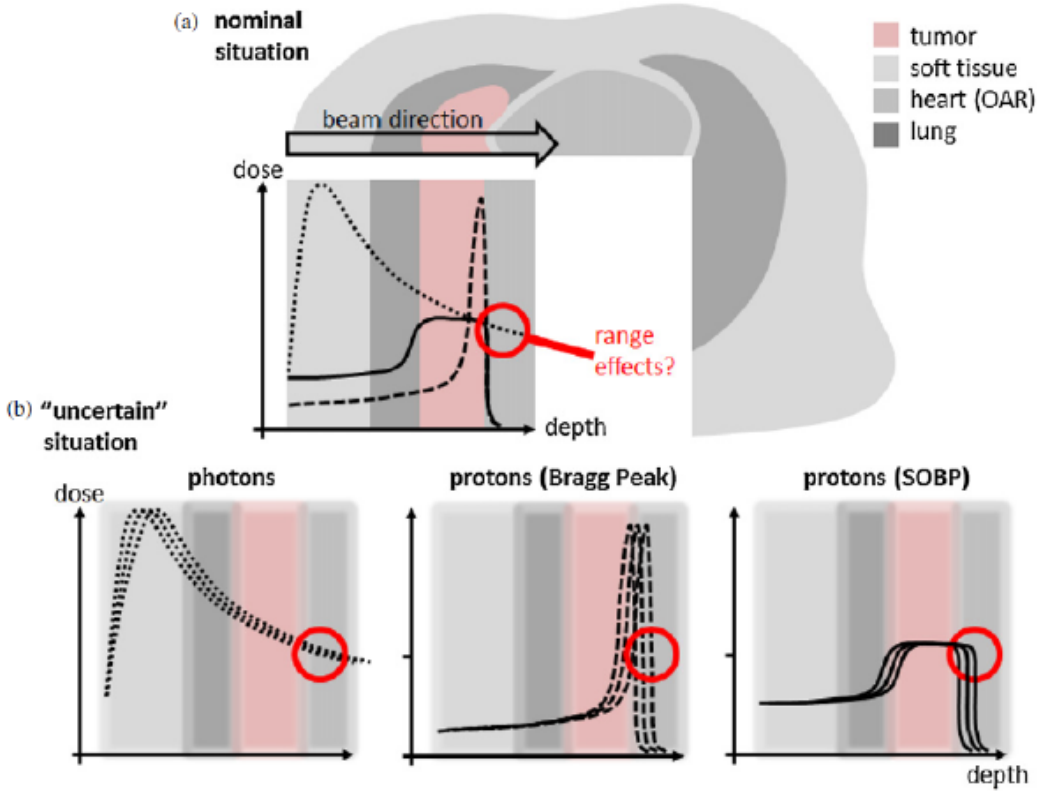

Figure 1.4: Exemple of the impact of uncertainties on the dose deposit for both conventional radiotherapy and hadrontherapy, extracted from [4].

As we can see, an error made in conventional radiotherapy treatment does not result in a major error in the dose deposition profile. Conversely, an error in the path of the ions in the patient can generate a double negative effect: an under-dosing of the tumor volume and an overdosing of the healthy tissue (so close to the OAR).

1.1.2 Online beam monitoring

At this level, it is obvious that the hadrons trajectory need to be carefully defined and specified for the safety of patients. The implementation of such control techniques is still an active research topic. Several ways are explored using different physical phenomena [4, 5, 6, 7].

The Bragg peak must be located in the targeted cells. An online monitoring system is required for checking hadrons trajectories. During a treatment by hadron therapy, a part of ions undergoes one or few nuclear fragmentations and emit a secondary gamma radiation. Detection of these secondary gamma radiations is the basis of the method used to localize the dose deposition into the patient. In figure 1.5 we see a proposed system for the trajectory detection of the particles in hadrontherapy.

This configuration uses an hodoscope for labeling the incoming ions providing both transverse coordinates beam location and time measurements. The compton camera consists of diffusion detectors (scatterer) and an absorption detector (absorber), which detects the secondary gamma rays following the nuclear fragmentation of hadrons in the patient's tissues. Gamma rays can be associated to the corresponding ion using very sharp time coincidences (less than 100 ps). More details about the compton camera can be found in [8, 9, 10]. For this study, we will focus on the hodoscope part of the system. these detector should be able to ensure three essential qualities:

- It must be position sensitive;

- It must have a good temporal resolution (at least of the order of 1 ns);
- It must be sufficiently resistant to radiation over time without any prohibitive variation in its performances.

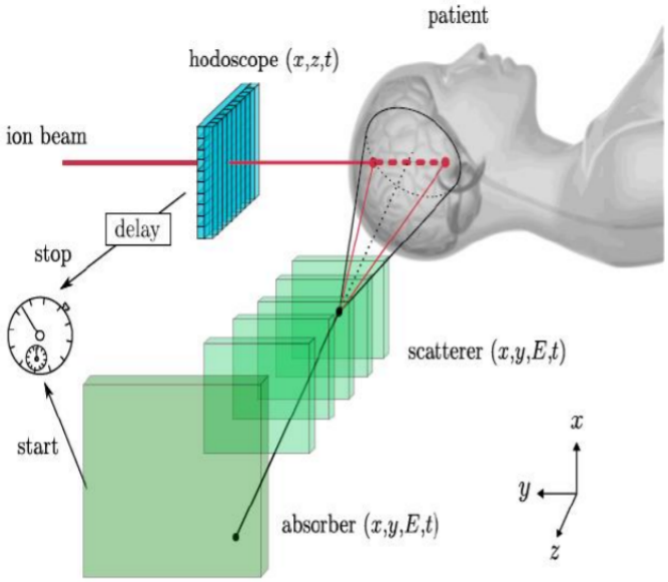

Figure 1.5: Schematic diagram of the contribution of spatial and temporal tagging provided by a beam hodoscope in the case of compton imaging for hadrontherapy.

Finally, it must be able to operate over a large dynamic range, from the detection of a single proton of 250 MeV to packets of a few hundred protons of 70 MeV (i.e., 2^9 of dynamic). The present hodoscope relies on an array of scintillating fibers which are coupled to multichannel photomultipliers tubes (PMT) as shown in figure 1.6. The performances of such a design are limited by the PMT admissible counting rate and the intrinsic radiation hardness of the scintillators which make it unsuitable for this application.

Figure 1.6: Photo of the hodoscope with scintillating fibers coupled to PMTs.

In order to overcome such difficulties, the CLaRyS collaboration has initiated different projects aiming to develop a new generation of hodoscopes using CVD (Chemical Vapor Deposition) diamond.

1.2 CVD diamond detectors

1.2.1 Diamond as a material

In theory, diamond is only composed of carbon and its exceptional properties and characteristics come largely from its crystal structure [11, 12]. For diamond, the proximity of the atoms in the crystal and the important overlap of the orbitals of neighboring atoms participate in the generation of an important gap of energy $E_g = 5.47\ eV$. Depending on the application, diamond is considered either as a large gap semiconductor or as an insulator. It also results in a very high displacement energy (43 eV) explaining the very high radiation resistance of diamond. Moreover, it is considered as an excellent thermal conductor, with a thermal conductivity of 2000 $W.m^{-1}.K^{-1}$. In addition, it can be subjected to very high electric fields thanks to its dielectric strength of $10^7\ V.cm^{-1}$. Diamond also has a very high resistivity ($> 10^{13}\ \Omega.cm$, allowing it to produce detectors with a very low leakage current at room temperature (typically of the order of one pA).

Table 1.1 resumes a comparison of the properties of diamond and silicon:

Table 1.1: Properties of Diamond Vs Silicon, extracted from [12].

Property	**Units**	**Diamond**	**Silicon**
Band Gap E_g	eV	5.47	1.12
Electron mobility μ_e	$cm^2/V.s$	1700	1420
Hole mobility μ_h	$cm^2/V.s$	2100	470
Saturation velocity	cm/s	2×10^7	1.4×10^7
Intrinsic carrier density	cm^{-3}	$< 10^3$	1.5^{10}
e/h pair energy	eV	13	3.6
Displacement energy	eV	37-47	15-20
Density	g cm^{-3}	3.52	2.33
Rad length X_0	cm	12.2	9.4
Dielectric constant ε_r	(relative)	5.7	11.9
Breakdown E-Field	V/μ m	1000	30
Resistivity	Ω/cm	$> 10^{15}$	$10^5 - 10^6$

Finally, diamond is of great interest for the development of fast detectors. The mobility and the saturation speed of its charge carriers are among the highest of the semiconductors. They also have the advantage of being relatively close to each other [13]. In addition to that, its dielectric constant of 5.7 is relatively low, this allows diamond detectors to have a very low capacitance compared to other semiconductors (at a given geometry), and thus enable very fast timing measurements.

1.2.2 CVD diamond for particle detection

a. Crystalline grades of diamond

Diamonds used to make particle detectors are often CVD diamonds. To date, three distinct crystalline grades of diamonds are produced by CVD and used for detector design:

- **Single-crystal CVD diamond (sCVD or sc-CVD)**
  They are made of a single homogeneous crystal, according to a precise crystallographic orientation (usually $< 100 >$ for detectors). They are produced by homoepitaxy: the seed

used is generally an ultra-pure monocrystalline diamond. They are commercially available for sensitive areas up to $4.5 \times 4.5\ mm^2$. Their small size together with their very high price represent the main limitation to their use [14].

- **Polycrystalline CVD diamond (pCVD or pc-CVD)**
  They are produced by heteroepitaxy. The use of substrates of a different chemical nature from diamond allows the production of much larger samples (up to $120 \times 120\ mm^2$). They are commercially available from various providers at a much lower price per unit area than the sCVD diamonds.

- **Heteroepitaxial diamond**
  The objective of heteroepitaxy on iridium (Diamond-On-Iridium: DOI) [15] is to allow the growth of large diamonds with electronic properties tending towards those of sCVD diamonds. This grade is still under development, early results show that there is still a large disparity in the quality of the samples produced, some DOI detectors have a response quality comparable to that of single crystal detectors. It was shown also that, in these DOI detectors, if the hole transport is realized with a very high quality, the electron transport is severely deteriorated. The cause of this deterioration of the electron signal is still unexplained [16].

b. Diamond as a solid state ionization chamber

Nowadays, diamond detectors are almost exclusively used as solid state ionization chambers. The principle of operation of an ionization chamber is based on the collection of free charges generated by the passage of an ionizing particle in a detection volume. This particle will give up part of its initial energy in the detection volume, thus generating a certain amount of charges proportional to the total energy deposit of the particle in the volume. Without the application of an external electric field, these free charges are likely to be recombined very quickly in the detector. To go against this recombination and generate a usable signal, an electric field is applied to the detection volume in order to make these charges drift. The displacement of these charges induces a current signal on the polarization electrodes. Figure 1.7 shows a simplified diagram of this system.

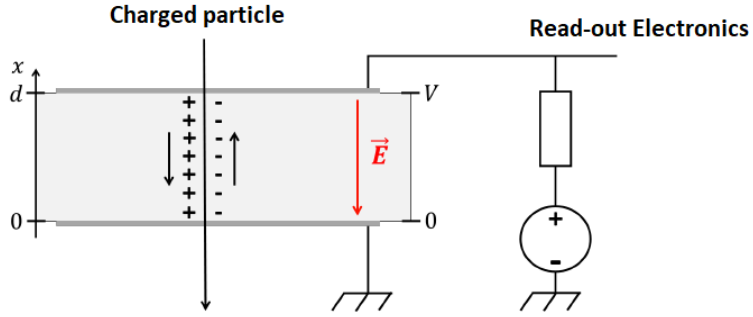

Figure 1.7: Concept diagram of a solid state ionization chamber based on a diamond detector.

In an ionization chamber, the electric field only allows the charges generated by the ionization to drift and does not allow the charges to be multiplied by the generation of electronic cascades. There is therefore no internal amplification of the primary signal in this configuration. The polarization electric field of a diamond detector in this case is generally a few $V.\mu m^{-1}$ (up to 10 $kV.cm^{-1}$). The measured signal corresponds in this case, to the signal induced by the displacement of charges under the effect of an electric field $E = \frac{V}{d}$, with V the value of the bias voltage and d the thickness of the diamond detector (case of a flat capacitor geometry). The induced signal can then be calculated using the Shockley-Ramo theorem [17, 18]. It states that

the current I_{ind} generated by the displacement of a free charge q at the drift speed $v_q = \|\overrightarrow{v_q}\|$ and induced on an electrode subjected to a unit potential ϕ_w:

$$I_{ind} = q\overrightarrow{v_q} \times \overrightarrow{E_w} \tag{1.1}$$

Where: $\overrightarrow{E_w} = -\overrightarrow{grad(\phi_w)}$ is called the weighting field.

In the case of a free charge in a polarized plane capacitor, we can also express the evolution of the induced current in time $I_{ind}(t)$. The most important drift time is that of a charge created at a distance d from the considered electrode and drifting towards this same electrode. If we note this time as $T_{e,h}$, we find $T_{e,h} = d/(\mu_{e,h}E)$. Since $v_h > v_e$ in CVD diamond, we distinguish then three temporal regimes [19]:

- When the two charge carriers drift ($t < T_h < T_e$):

$$I_{ind}(t) = \frac{-Q_0E^2}{2d^2}({\mu_h}^2 + {\mu_e}^2)t + \frac{Q_0E}{d}(\mu_h + \mu_e) \tag{1.2}$$

  where Q_0 is the inducted charge that corresponds to the Minimum Ionizing Particle (MIP).

- When only the electrons are still drifting ($T_h < t < T_e$):

$$I_{ind}(t) = \frac{-Q_0E^2}{2d^2}{\mu_e}^2 t + \frac{Q_0E}{d}\mu_e \tag{1.3}$$

- When the two carriers have stopped drifting:

$$I_{ind}(t) = 0 \tag{1.4}$$

A summary diagram of the inducted current generated by CVD diamond detectors is presented in figure 1.8.

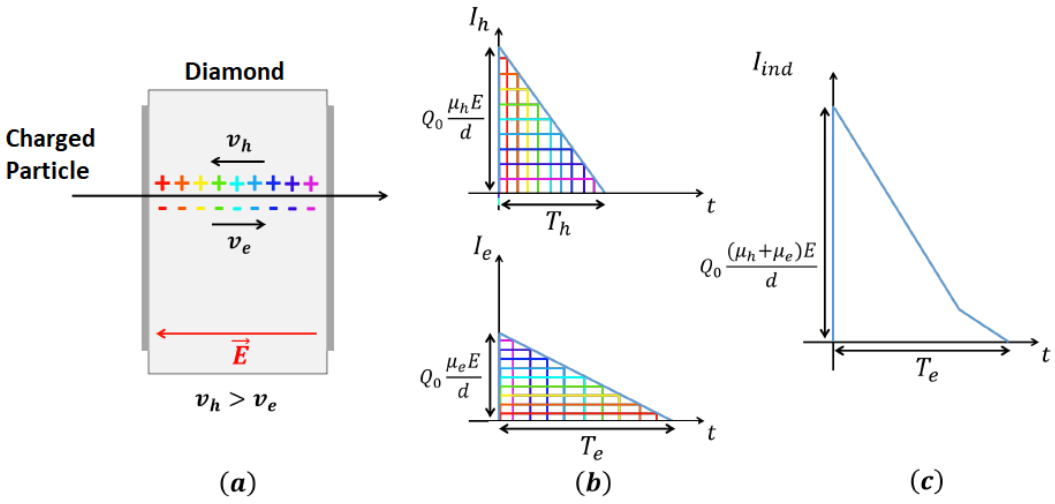

Figure 1.8: Summary diagram of the current induced in a diamond detector by a passing charged particle, extracted from [20]:
(a)A particle uniformly ionizes the medium along its path and the free charges begin to drift under the effect of the electric field;
(b)The drift of the two charge carriers induces a current of the same sign on the considered electrode;
(c)The total induced current on the electrode is the sum of the currents of the two charge carriers.

The signal generated by particles passing through the diamond is therefore triangular in shape when the transport of charges is done without parasitic effects (recombination and polarization).

1.2.3 CVD diamond Hodoscope

a. Specification of requirements

Within the framework of the CLaRyS-UFT project, a beam hodoscope demonstrator based on diamond CVD detectors is to be realized. To meet the objectives of the project, the demonstrator must meet the following specifications:

- A temporal resolution less than 100 ps;
- An overall count rate that can reach the 100 MHz;
- A very high resistance to radiation to guarantee a durable operation of the hodoscope in clinical conditions;
- A dedicated electronics capable of ensuring excellent temporal resolution over a very wide dynamic range (from a single 250 MeV proton to 60 MeV proton packets);
- A fast data transfer and processing, based on AMC40 acquisition boards using the μTCA standard and developed at the "Centre de Physique des Particules de Marseille (CPPM)".

To meet these requirements, the CLaRyS collaboration has decided to develop diamond hodoscope demonstrators based on stripped metallized CVD diamond detectors.

b. Details about the design

The segmentation of the detection surface into strips meets the need for two dimensional (2D) cross-sectional localization of the incident ion beam but also allows:

- A geometric definition of the lowest achievable spatial resolution, conditioned by the area defined by the intersection of two orthogonal strips;
- A distribution of the generated load on several reading channels, enables to improve the spatial resolution of the device to a value lower than the area described by the crossing of two orthogonal strips;
- A reduction of the constraints in terms of counting rate, the objective is to manage a counting rate of 10 MHz/channel;
- A reduction in the size of the electrodes, thus minimizing the input capacitance of the read-out electronics.

The main constraint associated with a segmentation in strips is the multiplication of the read-out electronics channels. This causes an increase in the complexity of these electronics and the resulting data processing. Moreover, this exposes the device to possible crosstalk issues between the different strips and leads to an increase in the system's power consumption (and the associated thermal dissipation). The segmentation of the detector surface also introduces non-metallized zones (inter-strip spaces) likely to cause a local defect of the charge collection, and thus of detection efficiency. Finally, at very low count rates, metallization on both sides in orthogonal directions exposes the detector to the risk of indetermining the position and number of ions that have interacted in a single event, this phenomena is known as "the ghost hits".

Figure 1.9 shows the design of the demonstrator as proposed by the collaboration. Depending on the quality and availability of crystals in terms of surface, we consider a demonstrator based on a single large diamond (a, left) or a demonstrator based on four small diamond detectors arranged in a mosaic (a, right) in order to cover a surface of at least 1×1 cm^2.

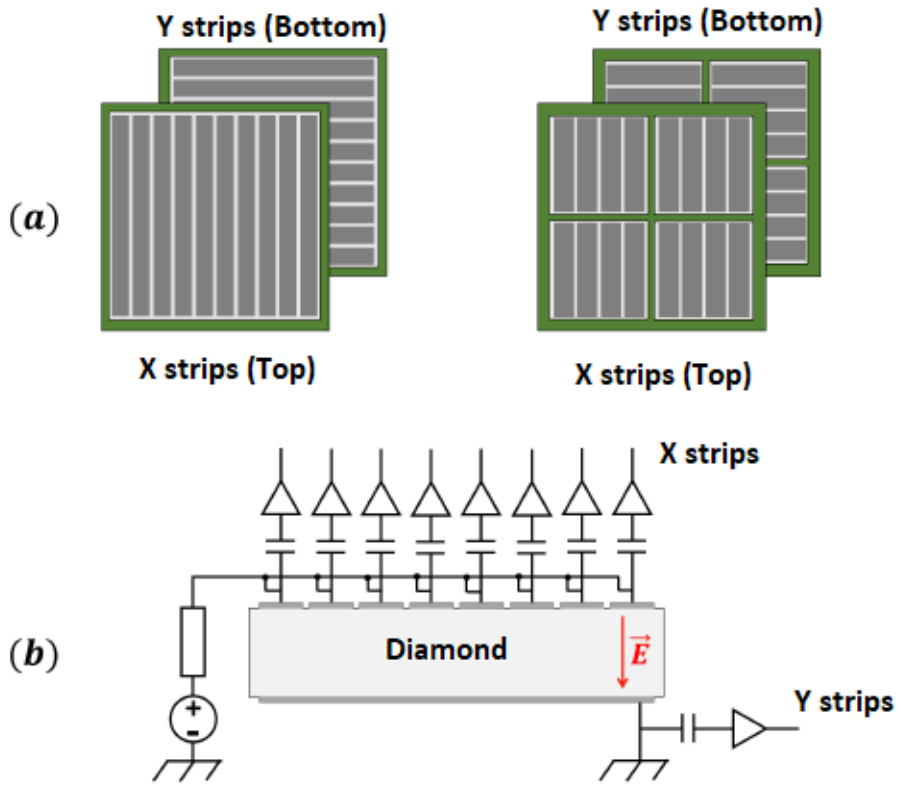

Figure 1.9: Concept diagram of the CVD double-side stripped metallized diamond beam hodoscope:
(a)The metallization by strips of large diamonds (left) or mosaic assembly of smaller diamonds (right);
(b)The coupling of the strips to their dedicated electronics on both sides of diamond.

In this configuration, the detector can be modeled as a current source with both a capacitor (C_d) and a resistor (R_d) in parallel of each other. We focus on the estimation of the equivalent capacitance of the detector (i.e. for a couple of two strips (x_i, y_i)). The resistor (R_d) is neglected because it is so high to be considered (several $T\Omega$) [21]. Using the dimensions of the detector shown in figure 1.10, the simplest estimation of the equivalent capacitance is:

$$C_d = \frac{A}{d} \times \varepsilon_0 \times \varepsilon_r \tag{1.5}$$

Where,

– A is the surface of the cross-section of the strips $[m^2]$;

– d is the thickness of the detector $[m]$;

– ε_0 is the electric permittivity of free space($\varepsilon_0 = 8.85418582e^{-12}$) $[F.m^{-1}]$;

– ε_r is the relative permittivity of the diamond ($\varepsilon_r = 5.7$).

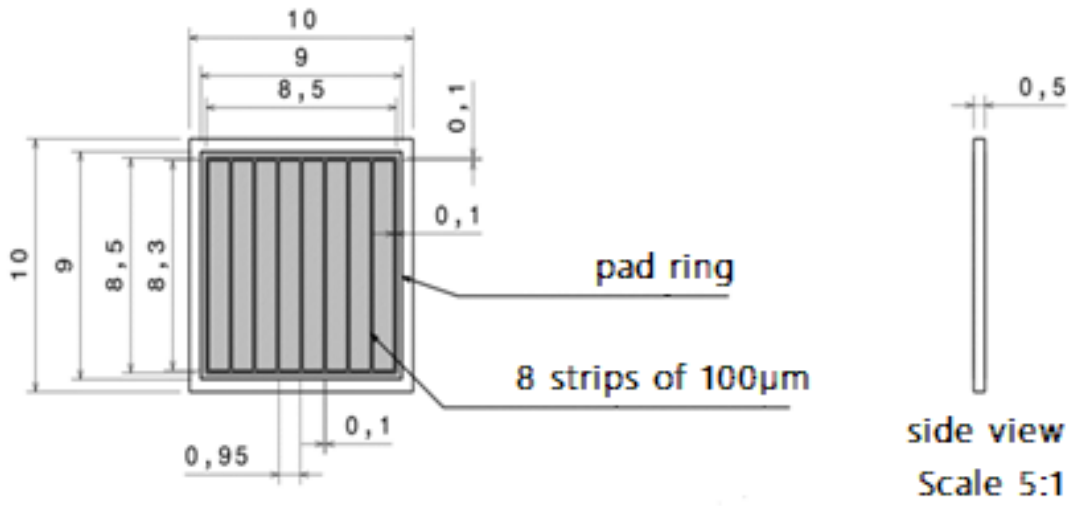

Figure 1.10: The proposed CVD Diamond detector dimensions.

Using this dimensions for diamonds with two different thicknesses, we found:

– For diamond with $d = 500\ \mu m$, the equivalent capacitor is $C_d = 795.8\ fF$;

– For diamond with $d = 300\ \mu m$, the equivalent capacitor is $C_d = 1.326\ pF$;

In the rest of this study, we mainly use diamonds of thickness $d = 300\ \mu m$, i.e. $C_d = 1.326\ pF$.

1.3 Read-out electronics for diamond detector

The proposed read-out electronics is composed of two systems: a high precision time measurement system and an energy measurement system as shown by the simplified diagram of figure 1.11. This configuration allows both temporal and space tagging exploring the potential of CVD diamond detectors and guaranteeing the targeted specifications detailed above. For this, the DIAMASIC project (CNRS/IN2P3) was launched, as a collaboration between two laboratories of the IN2P3 Institut: the LPSC Grenoble and th LPC Caen. This project is aiming to the study and design of a multichannel integrated electronics ASIC in CMOS 130 *nm* technology. The development of such electronics requires a low noise and a correctly defined bandwidth preamplifier stage followed by a fast discriminator with a performance exceeding the limitation of circuits known in the field such as NINO and PADI circuits [22, 23]. These two, for example, present limitations at the level of the minimum signal to be detected: a few tens of fC. They also have a temporal resolution limited to 80 ps. A second part of this electronics is the design of an energy measurement system known also as spectroscopy. We propose to achieve this in an innovative way by digitizing the signal as early as possible in our read-out electronics.

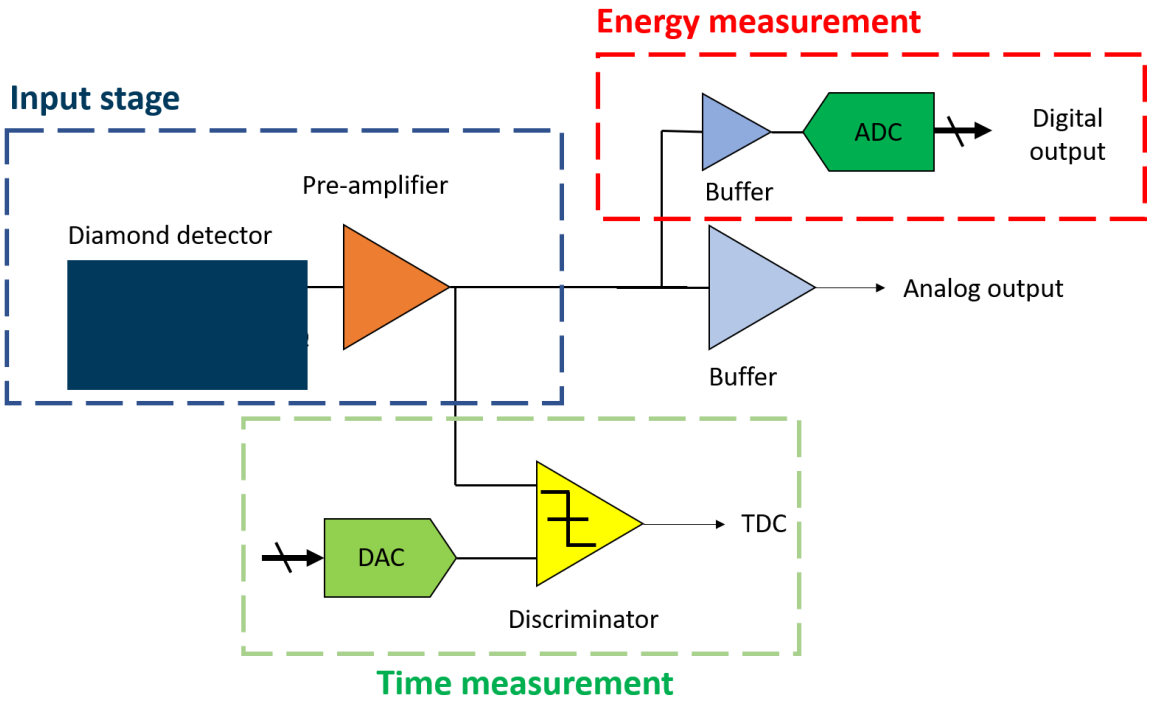

Figure 1.11: Simplified diagram of the proposed read-out electronics.

1.3.1 Contribution to the design of the time measurement system

We define a time measurement system as a Front End Electronics (FEE) for radiation detectors that targets a time to digital converter (TDC), figure 1.12 illustrates its different components.

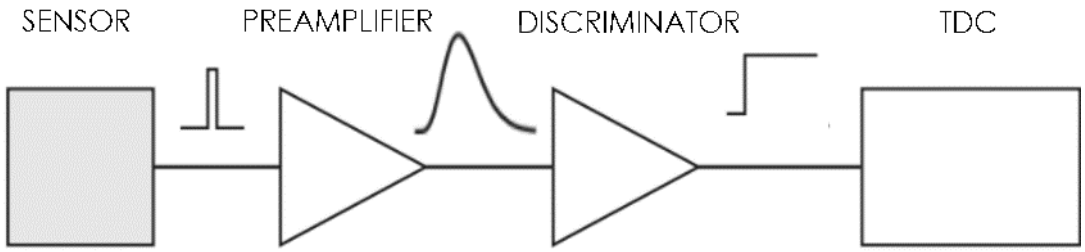

Figure 1.12: FEE diagram for radiation detectors, extracted from [24].

We focus on the input stage: the preamplifier, where we study the effect of its features on the final timing resolution. This latter is mathematically modeled as the maximum error of time defined using equation 1.6:

$$\sigma_t = \sqrt{\sigma_{Ji}^2 + \sigma_{TW}^2 + \sigma_{TDC}^2} \tag{1.6}$$

Where:

- σ_{TDC} is linked to the resolution of the TDC which depends on its architecture;
- σ_{TW} is related to the discrimination stage and known as the time walk [25];
- σ_{Ji} is usually associated to the noise of the preamplifier stage.

The σ_{Ji} represents the most critical element which we need to reduce to achieve high timing resolutions ($< 100\ ps$). During this study, this error will be considered as the criteria of the time resolution.

Few works have been done in the literature [26, 27] aiming to find the optimal possible values of the input impedance so to get the best performances. Classical studies suggest that having the lowest possible value of the input impedance will limit the time constant associated to the input node of the FEE. These criteria propose also to maximize the FEE bandwidth, which is usually deemed as the dominant parameter affecting the dynamic performance of the FEE. A recent study [27] shows that, these criteria (i.e. low R_{in} and high BW) do not represent the best solution in real situations; where the characteristics of the detector and the parasitic coupling inductance are taken into consideration.

In order to analyze precisely this, we developed a new mathematical model capable of obtaining the optimum values of R_{in} and BW of the FEE used for such high-resolution time measurement system ($< 100\ ps$). This allows us to make better design choices before going through many different electric simulations that usually take a lot of time and effort. The study is based on a design of a FEE for CVD diamond, which can detect a minimum charge of 5 fC from a pulse of few ns. The model is designed in MATLAB Simulink and compared to the measurements of our developed amplifier stage.

a. Electrical model of the system

The timing measurement circuit can be discribed as a system composed of two main parts: the electric equivalent model of the detector detailed above (check the subsection 1.2.3) and the FEE represented by its input impedance. We assume in our model that the input impedance is represented by its resistive component (R_{in}). This will be explained in subsection 1.3.1 where we detail the expression of the developed amplifier. We explore the effect of the value of R_{in} on the performance of the generated signal using a first model shown in figure 1.13. This can be seen as a first order system characterized by a time parameter τ as described in equation 1.7:

$$\tau = R_{in} \times C_d \tag{1.7}$$

A MATLAB Simulink model is developed to represent the response of the equivalent electric circuit of this model.

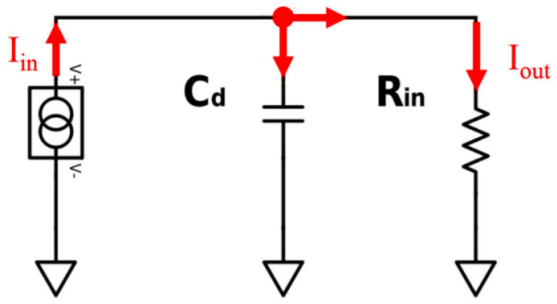

Figure 1.13: Equivalent electrical model of the input stage circuit.

Using this model, we can confirm the classical criteria that suggest the smallest input impedance to reach the fastest response. Unfortunately, this is not true for a real system; when the input impedance reaches a small value ($R_{in} < 20\ \Omega$), the system's response starts showing oscillations. This result indicates that the model used is not completely representing the real response of the system. A more accurate model is proposed adding the interconnection inductances of bonding wires between the detector and the FEE. It is illustrated in figure 1.14:

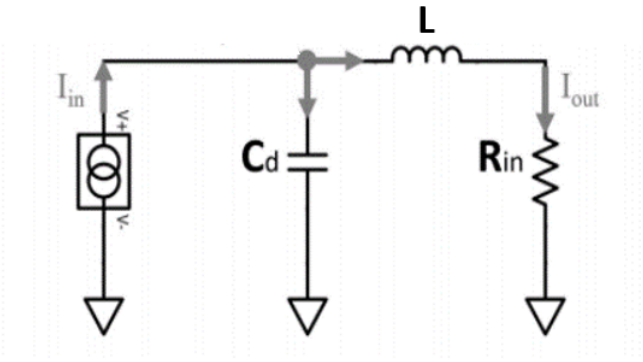

Figure 1.14: Precise equivalent electrical model of the input stage circuit with bonding wire inductance L.

Mathematically, this is modeled by the following transfer function:

$$H(p)_{\frac{I_{out}}{I_{in}}} = \frac{1}{1+(R_{in}\times C_d)\times p+(L\times C_d)\times p^2} \tag{1.8}$$

The response of a second order system depends on the value of the damping factor. In our case, we calculate this based on the classical model of a second order model:

$$H(p) = \frac{G}{1+\frac{2\times\xi}{\omega_0}\times p+\frac{1}{{\omega_0}^2}\times p^2} \tag{1.9}$$

Comparing equations 1.8 and 1.9, we find that the damping factor value is related to the value of the input impedance, the equivalent capacitance of the detector and the value of the parasitic inductance of the bonding wires as shown in equation 1.10:

$$\xi = \frac{R_{in}\times C_d}{2\times\sqrt{L\times C_d}} \tag{1.10}$$

When a second order system oscillates, we call it underdamped ($\xi < 1$) which is explained as the existence of a pseudo angular frequency, its value is related to the damping factor as demonstrated in the following equation:

$$\omega_d = \omega_n \times \sqrt{1-\xi^2} \tag{1.11}$$

To ensure the stability of the system and to avoid oscillations, the value of the damping factor must be slightly greater than 1 which means that the input impedance has to be limited. This explains why the classical criteria is not working for real situations. The optimum value of the input impedance is the one that allows us to have a damping factor $\xi > 1$: a fast system without oscillations. To investigate this optimum value, we plotted in figure 1.15 the evolution of the damping factor for different values of input impedance and parasitic bonding wire inductance (C_d is constant as calculated in 1.2.3).

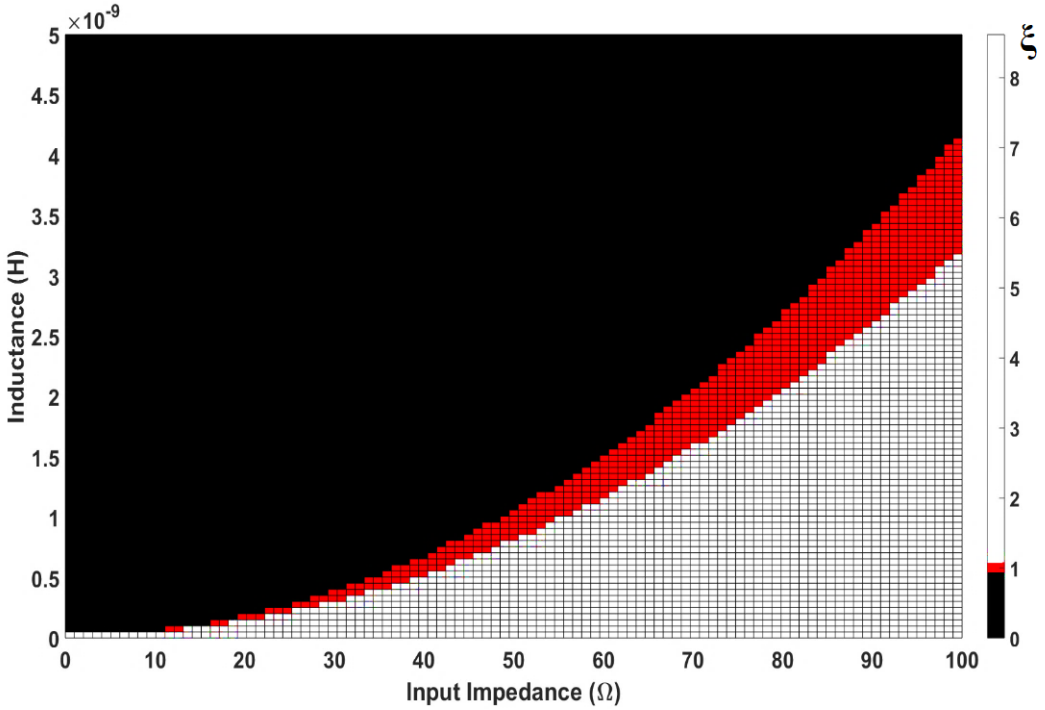

Figure 1.15: Values of the damping factor for different values of input impedance and parasitic inductance.

The optimum choice of the input impedance is to take the value that gives the closest damping factor to 1 according to the value of the estimated parasitic inductance. This allows us to obtain the fastest response avoiding any oscillations.

b. Bandwidth optimization

One of the critical challenges in designing FEE for systems with high accuracy of timing measurement is to find the suitable bandwidth. Usually, wideband systems are recommended [26, 27]. However, it becomes a bottleneck when it comes to low noise and low power consumption efficiency. So, one can ask: is it truly necessary for systems with high accuracy of timing measurement to be wideband? Here, an answer to this question is proposed based on the study of the RMS value of the timing jitter of the output FEE stage as a criterion of time performance.

When time is measured using discriminator systems [25], the timing jitter is classically defined as the ratio of the RMS output noise σ_n and the slope of the output signal $\frac{\partial V}{\partial t}$ [28]:

$$\sigma_{Ji} = \frac{\sigma_n}{\frac{\partial V}{\partial t}} \tag{1.12}$$

For such systems, this value is also estimated as shown in equation 1.13 [28]:

$$\sigma_{Ji} = \frac{T_{rise}}{SNR} \tag{1.13}$$

This equation shows that in order to minimize the timing jitter error, we need to minimize the rise time of the system to match the rise time of the detector and maximize the SNR.

For a preamplifier, the rise time is related to its bandwidth as illustrated in the following equation:

$$T_{rise} = \frac{0.35}{BW} \tag{1.14}$$

From this, we notice why it is classically recommended to choose wideband systems. The main issue in this choice is the fact that increasing bandwidth will lead to an increasing of the noise level, which will therefore decrease the SNR. Thus, the timing jitter will be degraded. We propose here to study a new kind of expression of the timing jitter equation with reference to equation 1.12.

The first step is to define the expression of the RMS output noise. In the case of a transimpedance amplifier (TIA), the equivalent output noise can be estimated using three parameters: the BW, the current input noise i_n and the gain of the amplifier G.

$$\sigma_n = G \times i_n \times \sqrt{\alpha \times BW} \tag{1.15}$$

Where:

– α is the multiplication factor of the Equivalent Noise Bandwidth (ENBW) as shown in table 1.2 [29].

Table 1.2: ENBW vs Filter order for low-pass filters.

Filter order	ENBW
1	$1.57 \times BW$
2	$1.11 \times BW$
3	$1.05 \times BW$
4	$1.025 \times BW$

The second step consists of approaching the value of the slope of the output signal, this approximation is the same used for equation 1.13:

$$\frac{\partial V_{out}}{\partial t} \approx \frac{V_{max}}{T_{rise}} \tag{1.16}$$

The maximum output of a TIA amplifier with a reference to its output is:

$$V_{max} = G \times I_{in_{max}} \tag{1.17}$$

The rise time at the output of the amplifier is defined as the convolution of all stages time responses in the signal path, and modeled by the following equation:

$$T_{rise} = \sqrt{T_{r1}^2 + T_{r2}^2 + T_{r3}^2} \tag{1.18}$$

Where:

– T_{r1} is the rise time of the detector signal;

– T_{r2} is the rise time of the input stage;

– T_{r3} is the rise time of the preamplifier stage.

Using the values of equation 1.15 and 1.16 in equation 1.13, we find a new mathematical equation for the timing jitter:

$$\sigma_{Ji} = \frac{i_n \times \sqrt{\alpha \times BW} \times T_{rise}}{I_{in_{max}}} \tag{1.19}$$

For a triangular shape signal with a time duration (T_d), and in terms of the charges generated by the detector ($Q_{in_{max}}$), this equation can be written as well as showing in the following equation:

$$\sigma_{Ji} = \frac{i_n \times \sqrt{\alpha \times BW} \times \sqrt{T_{r1}^2 + T_{r2}^2 + T_{r3}^2} \times T_d}{2 \times Q_{in_{max}}} \tag{1.20}$$

This new equation shows that the electronics is not the only factor that influence the value of the jitter. The performances of the detector do too (The current generated by the detector $I_{in_{max}}$ that depends on its characteristics: $Q_{in_{max}}$, T_d and T_{r1}) but since this later is so difficult to adjust, we focus only on the design choices of the electronics.

First, we studied the effect of having a wide bandwidth system. The plot of the evolution of the timing jitter for different values of BW is illustrated in figure 1.16. The timing jitter function is calculated for a system with the following values:

- $i_n = 13.2\ pA/\sqrt{Hz}$: this means that we manage to keep the maximum of the current input noise i_n below or equal to this value for every chosen BW);
- $T_{r1} = 350\ ps$, $T_{r2} = 100\ ps$, $T_{r3} = \frac{0.35}{BW}\ ps$;
- $I_{in_{max}} = 5\ \mu A$.

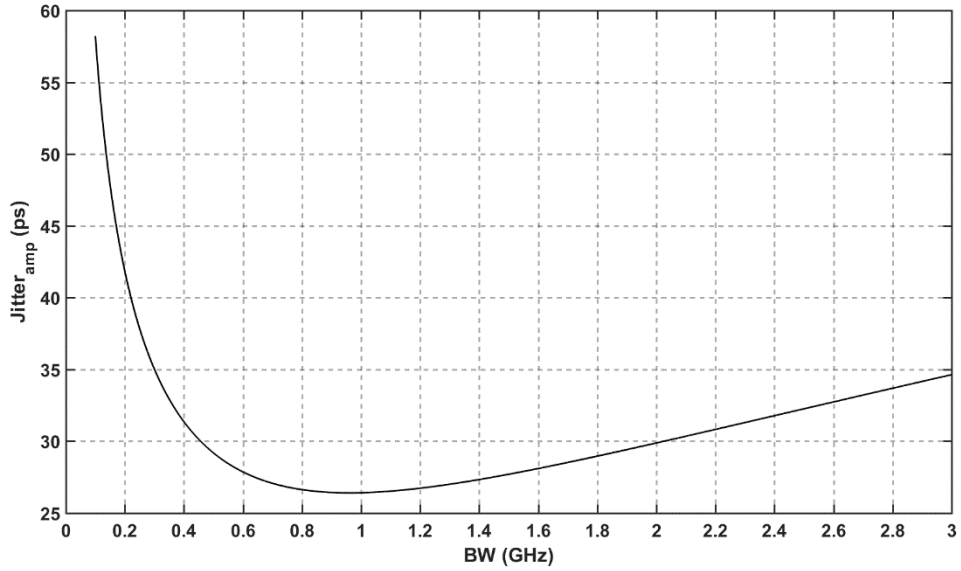

Figure 1.16: Timing jitter function according to the specs of the FEE.

Analyzing these results, we can clearly conclude that the effect of the bandwidth on the timing jitter is considerably weak. If we compare a system with a bandwidth of 2 GHz with a system of 500 MHz, we have barely an improvement of around 10 ps for a higher price of complexity in design (maintaining a low value of the current input noise i_n). It shows also the existence of an optimum value of the bandwidth for the lowest possible timing jitter. We identify it by using the second derivative test of equation 1.19 and we found:

$$BW_{optimum} = \frac{0.35}{\sqrt{T_{r1}^2 + T_{r2}^2}} \tag{1.21}$$

These results leaded us to our second study, where we analyzed the evolution of the value of T_{rise}: having wide bandwidth system will make the value of T_{r3} too close to the value of T_{r1} which is related to the input stage. This means that this stage will be more critical in the calculation of the final value. The input stage is represented as a second order system, since we guarantee the over-damped case, T_{r2} is estimated as shown in equation 1.22 [30]:

$$T_{r2} = \frac{1.8}{\omega} \tag{1.22}$$

where:

$$\omega = \frac{2 \times \pi}{\sqrt{L \times C_d}} \tag{1.23}$$

Thus, in the case of having a wide bandwidth, the value of the parasitic inductance must be taken into consideration since there is a strong correlation.

From these two analyses, we can clearly identify an optimum bandwidth for the targeted value of the timing jitter while minimizing the impact of the input stage.

c. Circuit implementation

In order to validate the new timing jitter expression: equation 1.19, a TIA was designed [31]. Its architecture is based on a common gate feedforward structure [31] as illustrated in figure 1.17:

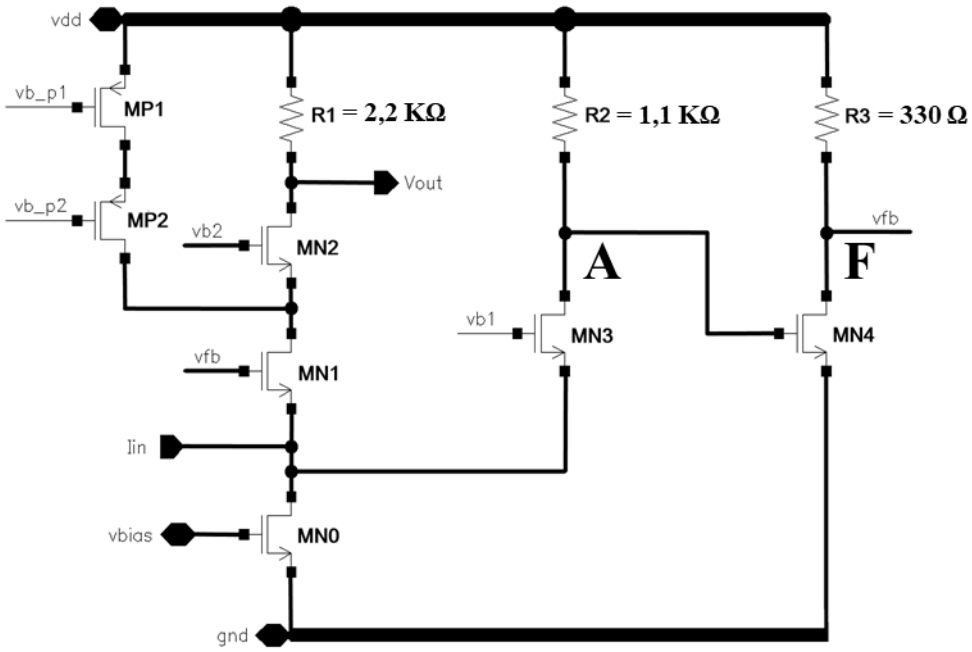

Figure 1.17: Common Gate Feedforward TIA architecture.

It is a common gate topology using a gain-enhancing feedforward path composed of the transistors MN_2 and MN_3. The transistor MN_1 provides the feedback path for the current amplification so that the transistors MP_1 and MP_2 will permit to boost the gain amplification by reducing the current flow through the resistor R_1. The transistor MN_0 is used as the current source to biasing the full amplifier.

In low power supply design, it is difficult to bias all transistors in saturated region. Therefore, in our design, the transistor MN_3 is inserted to shift the gate voltage of the transistor MN_4 to a higher level. Even at $1.2\,V$ power supply, all amplifying transistors are biased at a gate-to-source and drain-to-source voltage at least equal to $0.5\,V$. The transimpedance low frequency gain is provided by the resistance R_1 as:

$$\frac{V_{out}}{I_{in}} \approx R_1 \tag{1.24}$$

The input impedance of the TIA Z_{in} varies depending on the frequency, it can be described as following:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_{m_1} \times |A_1(f)| \times |A_2(f)|} \tag{1.25}$$

With $A_1(f)$ and $A_2(f)$ are respectively the gains of the second and third stages of the amplifier. The second stage is a common gate amplifier and the third stage is a common source amplifier, thus:

$$A_1(f) = \frac{g_{m_3} \times R_2}{1 + R_2 \times C_A \times p} \tag{1.26}$$

$$A_2(f) = \frac{-g_{m_4} \times R_3}{1 + R_3 \times C_F \times p} \tag{1.27}$$

Where:

- C_A and C_F are the equivalent capacitors at the nodes **A** and **F** respectively, shown in figure 1.17;
- g_{m_i} is the transconductance of each transistor MN_i.

Replacing equations 1.26 and equation 1.27 in equation 1.25 give us:

$$Z_{in} = \frac{(1 + R_2 \times C_A \times p) \times (1 + R_3 \times C_F \times p)}{g_{m_1} \times (R_2 \times g_{m_3} \times R_3 \times g_{m_4})} \tag{1.28}$$

This expression (equation 1.28) shows that Z_{in} has an imaginary component (which is proportional to the transimpedance gain and the bandwidth of the amplifier) represented by the two zeroes R_2 C_A and R_3 C_F which we can notice clearly on figure 1.18 (black dashed line). Yet, these two zeros take effect in high frequencies. We work in lower frequencies where the input impedance is only represented by its resistive component:

$$Z_{in} \approx \frac{1}{g_{m_1} \times (R_2 \times g_{m_3} \times R_3 \times g_{m_4})} \tag{1.29}$$

This explained clearly that we represented the input impedance as a resistor (R_{in}) in our theoretical model (part 1.3.1). Using this kind of topologies, allows us to get very low input impedance via the use of R_2 and R_3 (i.e., few ohm).

The bode diagram (black line), the input referred noise spectrum (grey point-dashed line) and input impedance (black dashed line) are illustrated in figure 1.18. The other key performance of the proposed TIA are detailed in 1.3.

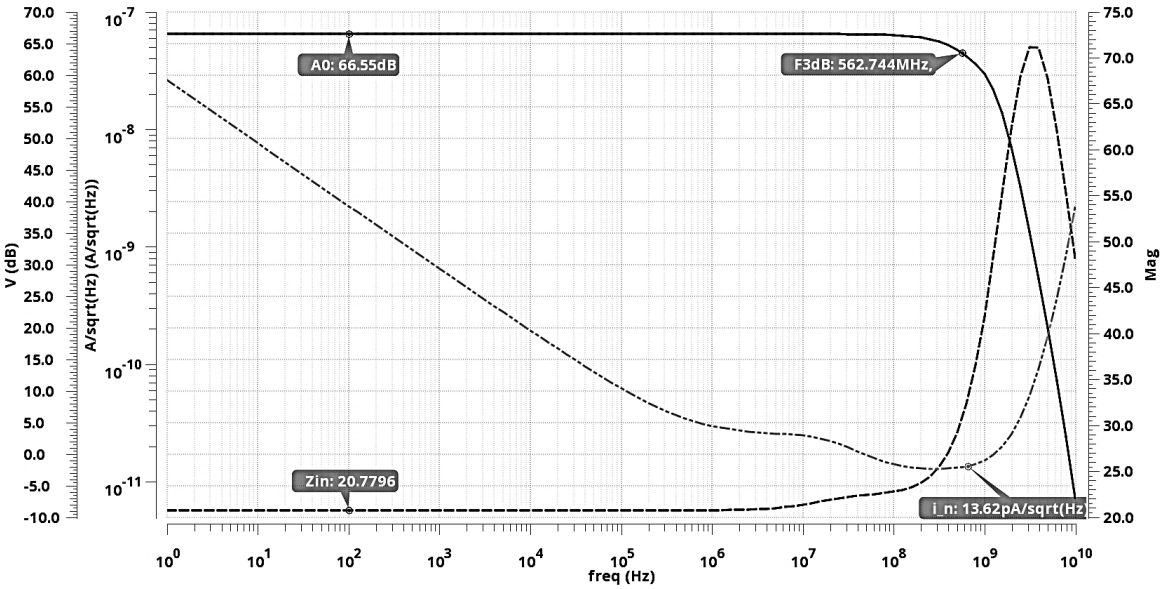

Figure 1.18: AC and noise extracted simulation results.

Table 1.3: Key parameters of the proposed TIA.

Parameters	values
TIA gain (dBΩ)	66.55 (2125 V/A)
DC input impedance (Ω)	20.78
TIA BW (f_{-3dB} MHZ)	562.74
i_n ($pA/\sqrt{Hz}$) @$\pi/2 \times f_{-3\,dB}$	13.62
Power consumption @1.2V (mW)	2.54

The second block of the timing measurement system is the discriminator stage. We decided to use a Leading-Edge Discriminator with a threshold low enough to be as close as possible to the pedestal signal since we guarantee a very low noise level. The circuit is designed as a cascaded wide band and low gain stages that is usually recommended for detectors with large signals [25].

d. Simulation and test results

In this first part, we illustrate by RC extracted simulation results the several issues of a very low input impedance Z_{in}. As mentioned earlier in the subsection 1.3.1, bonding wires can deteriorate the response of the TIA in accordance with low impedance. Figure 1.19 shows oscillation issues with a R_{in} of 20 Ω and several inductance values (5 nH, 10 nH and 20 nH).

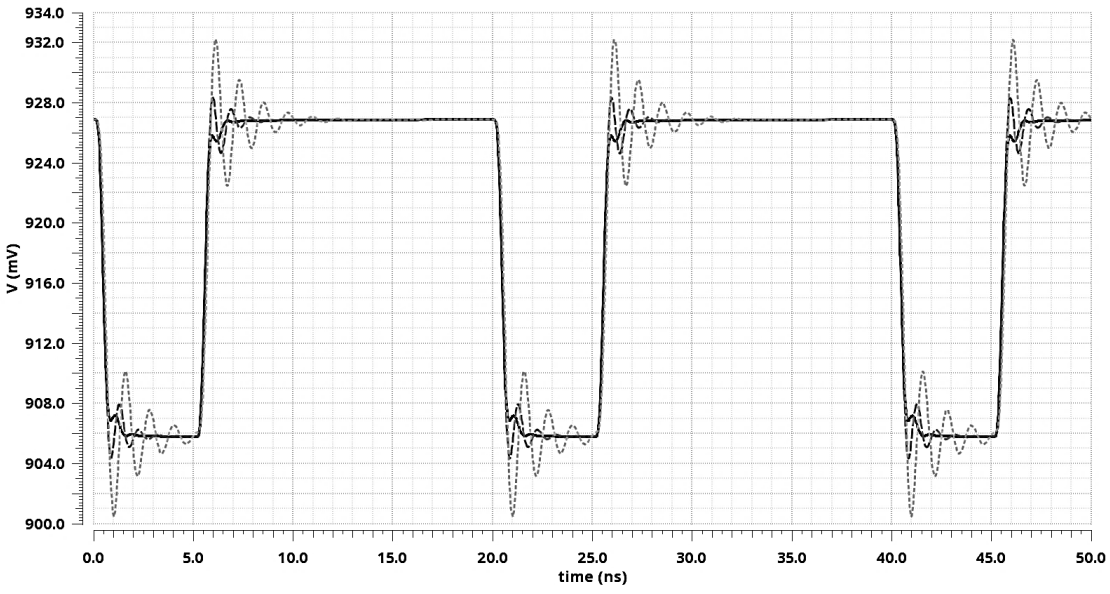

Figure 1.19: Extracted transient simulation of the TIA output with $R_{in} = 20$ Ω and several inductance values (5 nH (solid), 10 nH (dashed) and 20 nH (doted)).

To reduce this oscillation phenomena, we have to adapt the signal path and/or increase the input impedance. Unfortunately, in this last case the amplifier bandwidth will decrease. Figure 1.20 shows the case with an input impedance R_{in} of 50 Ω: the bandwidth of the TIA is reduced to approximately 400 MHz.

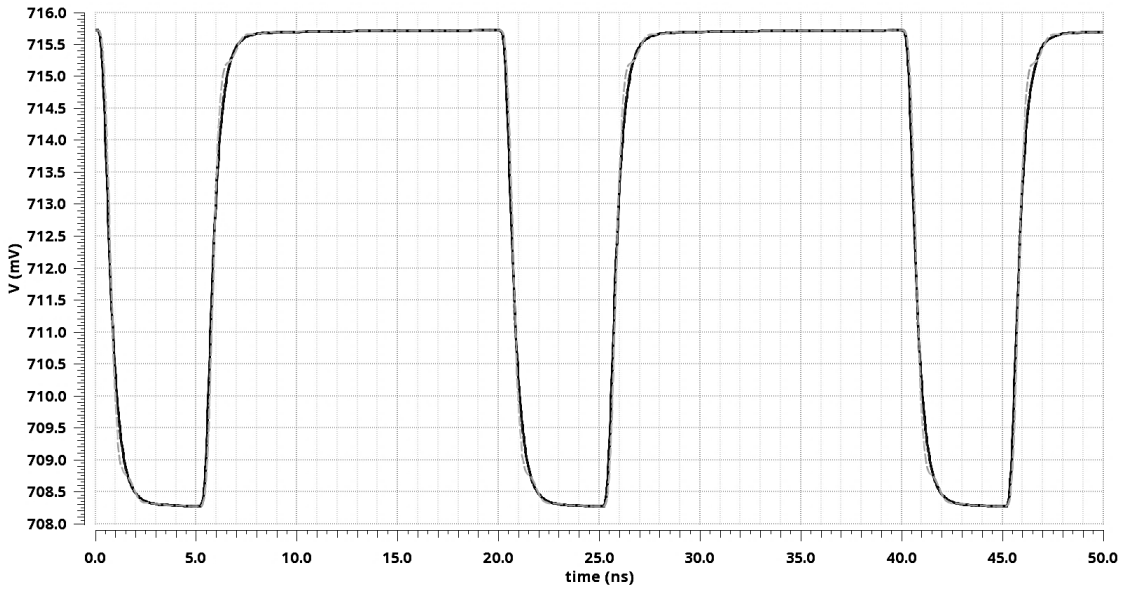

Figure 1.20: Extracted transient simulation of the TIA output with $R_{in} = 50\ \Omega$ and several inductance values (5 nH (solid), 10 nH (dashed) and 20 nH (doted)).

In a second time, we compared the measurement results of the timing jitter with both the classical formula (equation 1.13) and our new formula (equation 1.19).

The ASIC has been fabricated in a 130 *nm* CMOS technology and mounted directly on a PCB. It contains an 8 channels preamplifier-discriminator circuit [32] (both input and output are bonded). This PCB is mounted on a test card where the supply and bias are applied. Figure 1.21 shows a photo of the chip on board.

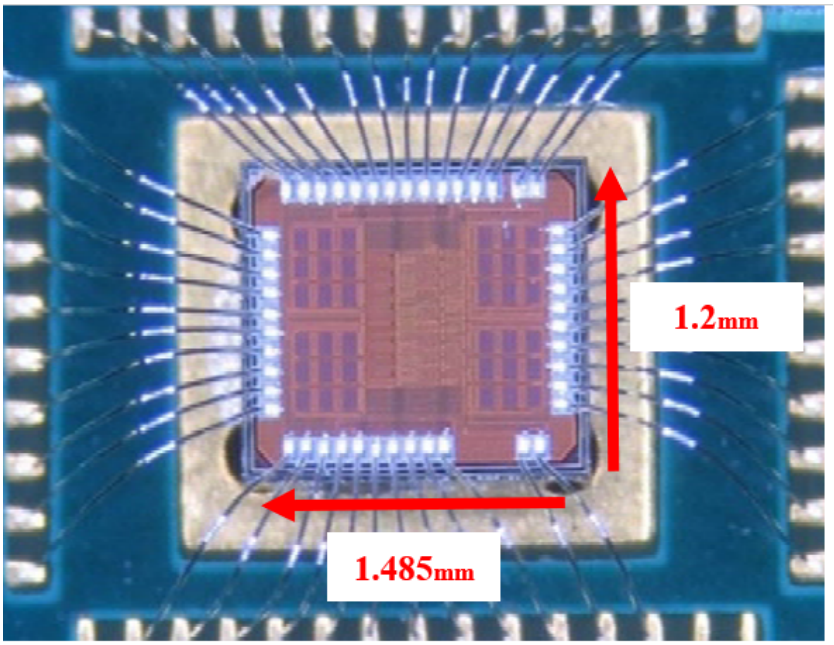

Figure 1.21: The ASIC of the proposed FEE.

For the test, we emulate the behavior of the detector by injecting different values of charges through a capacitor of 1 pF. The setup of the test is shown in figure 1.22.

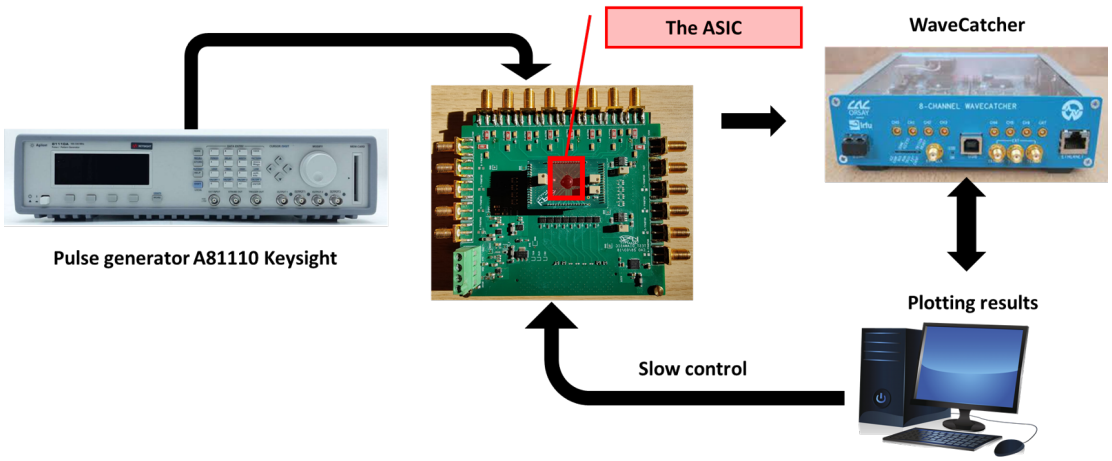

Figure 1.22: The testing setup for the measurements of the timing jitter.

We record the values of the output for 1000 tests with every input in order to estimate as precisely as possible the timing jitter. The result of the comparaison are shown in figure 1.23.

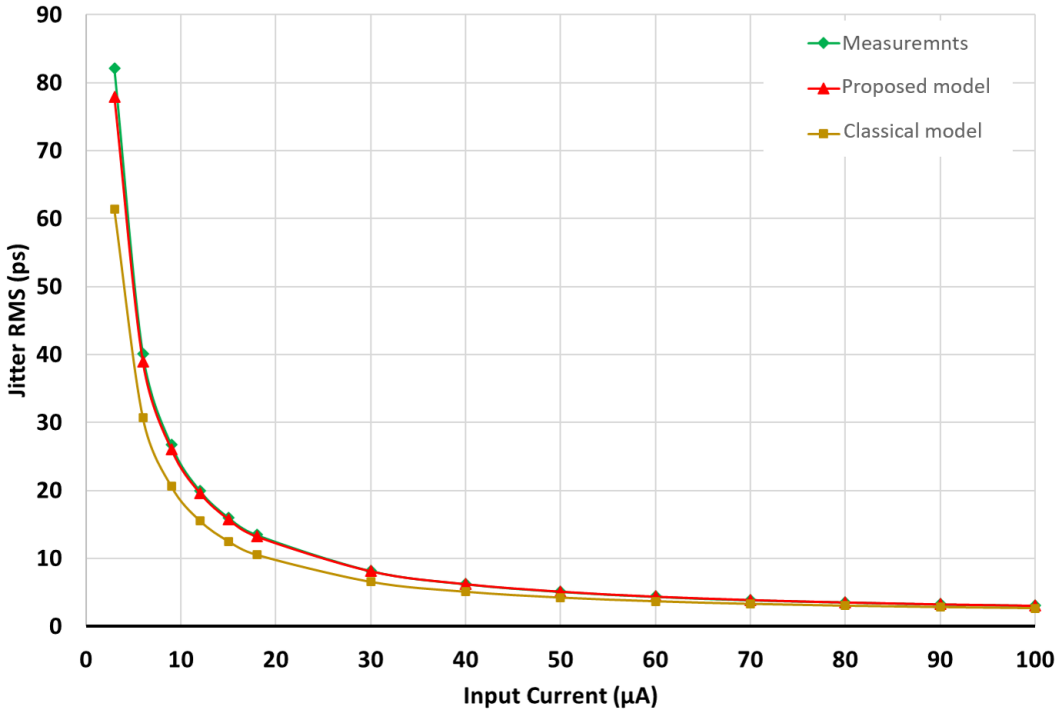

Figure 1.23: The values of the timing jitter: measured and calculated.

Figure 1.24 shows that our proposed model is more accurate than the classical one: Using the classical formula, we have an error that varies between 15% and 25% while the new formula has less than 5% error.

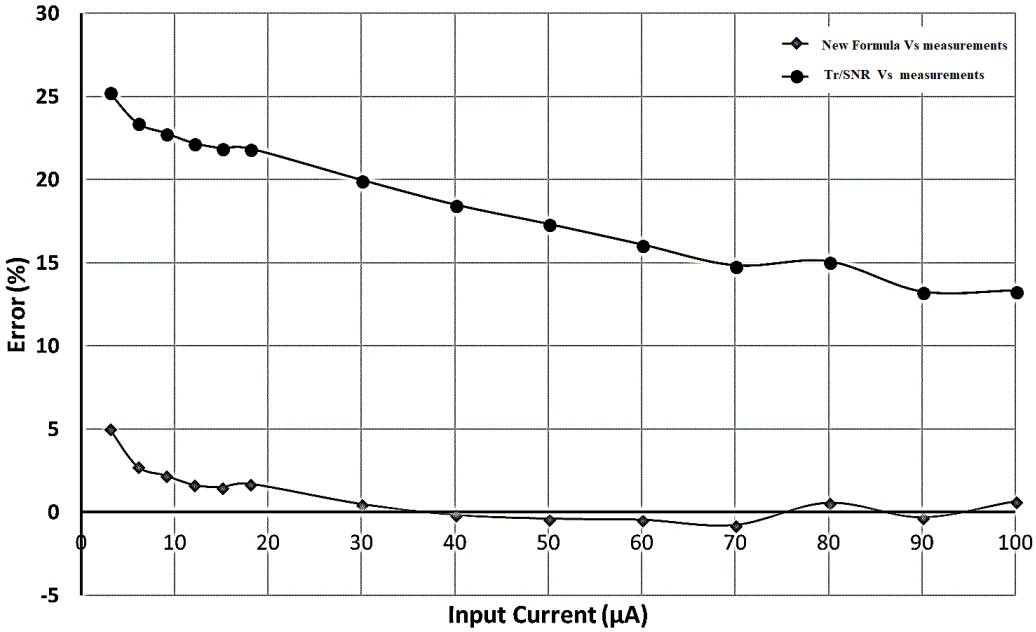

Figure 1.24: Comparison of the precision of the two formulas based on measurement results.

1.3.2 The energy measurement system

The second part of the read-out electronics is the spectroscopy circuit. It is used to estimate the deposited energy during the treatment. This class of systems are classically designed as shown in figure 1.25 (a). The problem with this topology is the analog shaping block, which represents a bottleneck when it comes to ensuring high accuracy and minimal variation between channels. It also limits the single chip integration with complexity, high power consumption and large area occupation. Moreover, with the continuous evolution of technologies (reduction of supply voltages), the design of such stages becomes more and more challenging.

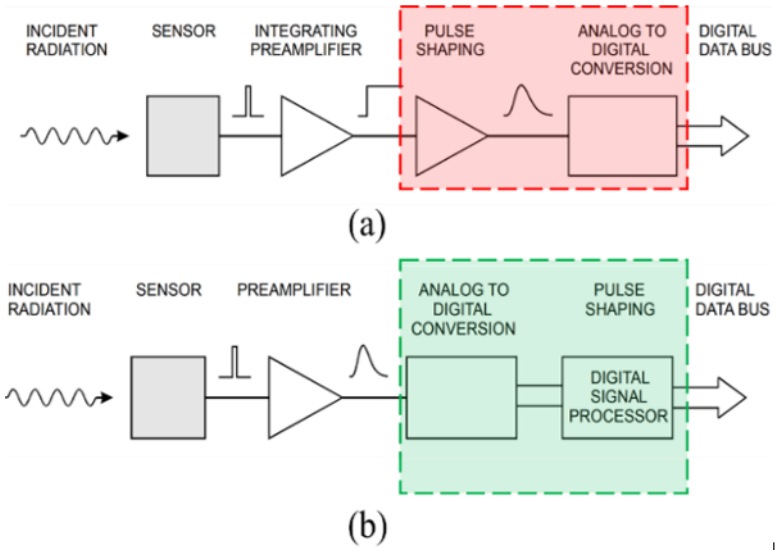

Figure 1.25: (a) Simplified diagram of the classical systems;
(b) Simplified diagram of the novel systems , extracted from [33].

The idea here (for the second topology) is to digitize the signal as soon as possible as

demonstrated in figure 1.25 (b). This new topology was presented for the first time in [33]. The author discussed the possibility of using a specific type of Analog-to-Digital Converters ($\Delta\Sigma$ ADCs) in order to open such possibility. He outlined as well its potential applications in the field of particle physics.

1.4 Motivation

The goal of this thesis, is to explore the possibility of implementing this novel topology. More precisely, studying, modeling and implementing the ADC part of it in a 130 *nm* CMOS technology. For this, we guarantee the specifications of the design of the CVD diamond hodoscope while making the proof of concept.

1.5 Summary

Throughout this chapter we have provided a detailed insight of the application of the targeted circuit and the technology of the detector. We introduced the need and specification of the read-out electronics and some of our contributions in the implementation of the timing measurement system. Finally, the concept of a new spectroscopy read-out electronics is shown. In this thesis, we propose to design the ADC of this novel concept. We address the main problematic of this type of ADCs in the modeling phase and we explain the use of modern g_m/I_d methodology to size the transistors of different stages. The results of electric simulation will be discussed to show the efficiency of this implementation before the fabrication of the ASIC.

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2

Introduction to analog to digital conversion

In this chapter, generalities about analog to digital converters are presented to build the necessary understanding of the thesis. Performance metrics, different classes of ADC and fundamental concepts of Delta-Sigma ADC are introduced and discussed.

Contents

2.1 ADC Performance Metrics

An analog to digital converter is a system used to interface the analog continuous world with the digital world enabling calculators to process and use information around us. Figure 2.1 shows different available ADC architectures that cover a wide selection of bandwidth and resolution requirements. A more detailed study is available in [1].

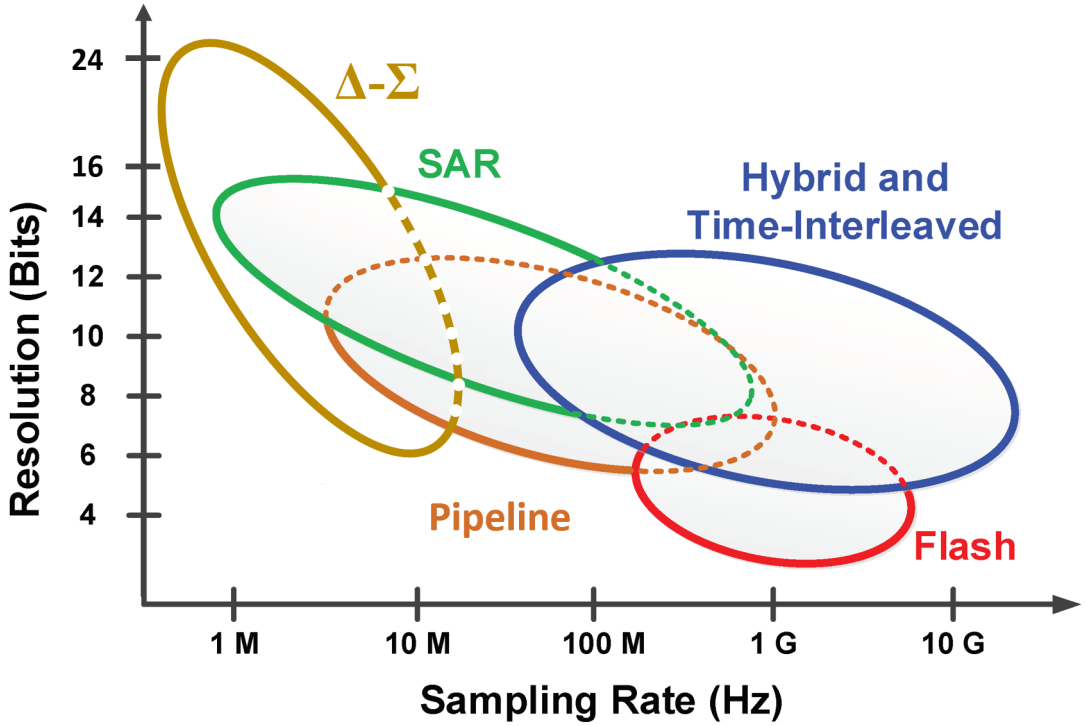

Figure 2.1: Overview of different ADC architectures operating ranges, edited from [2].

In this section, various parameters that characterize ADCs are briefly presented to give a better understanding of the different architectures and limitations. These metrics are divided into two classes: Dynamic parameters and static parameters, but first, we introduce the operating principle of the ADC which is called the quantization.

2.1.1 Quantization

In analog to digital conversion, the quantization process translates a continuous amplitude signal into 2^N discrete levels, where N denotes the quantization resolution. This parameter represents the number of bits used to describe the value of the digital output. The least significant bit (LSB) called also the quantization step of an ADC is calculated using this parameter as shown by the following equation 2.1:

$$A_{LSB} = \frac{FS}{2^N - 1} \tag{2.1}$$

where:
FS is the full-scale input range of the ADC. Figure 2.2 (a) shows an example of the DC output of an ideal 3-bit ADC.

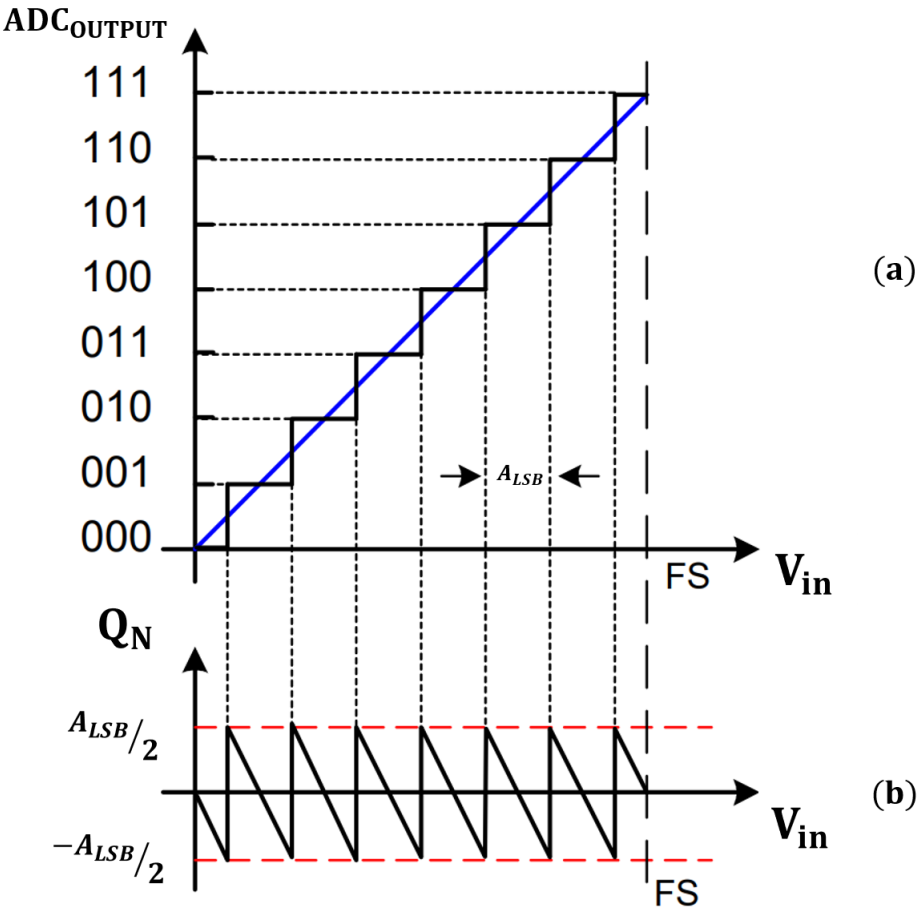

Figure 2.2: (a) Transfer function of a 3-bit ideal ADC;
(b) Quantization error of a 3-bit ideal ADC, edited from [3].

Here, we can observe that the quantization process is inherently nonlinear, since it maps a number of input samples into the same output level. This signal ambiguity is referred to as quantization error (Q_N) [4]. This error can be approximated by the equivalent linear model with additive white noise (as shown in figure 2.2 (b)), given the following conditions [5, 6]:

– the quantizer contains a large number of levels;

– the input signal spans all the quantization levels;

– the quantization process is assumed uniform;

– the quantization error is independent of the input signal.

For these conditions, the quantization error can be approximated as a quantization noise: a random process that has a uniform probability density function (PDF) in the range of $[-A_{LSB}/2, +A_{LSB}/2]$. The RMS value of this noise is described by the following equation [5, 6]:

$$Q_N = \frac{A_{LSB}}{\sqrt{12}} \tag{2.2}$$

2.1.2 Dynamic parameters

Dynamic parameters are used to measure the accuracy of ADCs when input signals are varying (in dynamic condition), they are obtained by calculating the FFT of the output data of the ADC with a "pure" sinusoidal input signal: i.e. the input signal should have a much better linearity than the ADC under characterization.

a. The Bandwidth (BW)

It represents the range of frequencies covered by the ADC. This parameter is used in the analysis of the dynamic behavior of the ADC.

b. The Output Data Rate (R)

It is the sampling frequency of the digital output f_s.

c. The Signal to Quantification Noise Ratio (SQNR)

It is the ratio of the output power to quantification noise power:

$$SQNR[dB] = 10\log_{10}(\frac{P_{sig.out}}{Q_N}) \tag{2.3}$$

This parameter is a representation of the resolution of an ADC, and it is linked to its value as expressed by equation 2.4.

$$SNR[dB] = 6.02 \times N + 1.76 \tag{2.4}$$

d. The Total Harmonic Distortion Value (THD)

It is the ratio of the RMS value of the harmonics produced by the ADC to the RMS level of a sinusoidal input signal near full-scale.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + ... + V_n^2}}{V_1} \tag{2.5}$$

This parameter is used to characterize the linearity of the ADC; the lower this value, the more linear is the ADC.

e. The Signal-to-noise-plus-distortion ratio (SNDR or SINAD)[1]

It is the ratio of the output power to the power of the noise sources in the in band (In Band Noise (IBN)).

$$SNDR[dB] = 10\log_{10}(\frac{P_{sig.out}}{Q_N + P_{har}}) \tag{2.6}$$

So basically, the SNDR is the sum of the SQNR and THD (equation 2.7).

$$SNDR[dB] = SQNR[dB] + THD[dB] \tag{2.7}$$

f. The Effective number of bits (ENOB)

It represents the effective resolution of the ADC and it is the equivalent of the SNDR in terms of bits.

$$ENOB = \frac{SNDR[dB] - 1.79}{6.02} \tag{2.8}$$

g. The Dynamic Range (DR)

It is the ratio between the maximum and the minimum amplitude converted correctly by the ADC. It is estimated using the following equation:

$$DR[dB] = 10\log_{10}(\frac{P_{sig.out,max}}{IBN}) = 10\log_{10}(\frac{\frac{V_{FS}^2}{2}}{2 \times IBN}) \tag{2.9}$$

[1] Signal-to-Noise Ratio and Distortion (SINAD)

h. The Spurious Free Dynamic Range (SFDR)

It is the ratio between the level of the input signal and the level of the largest distortion spur.

$$SFDR[dB] = 10\log_{10}(\frac{P_{sig.out}}{P_{har}}) \tag{2.10}$$

It is usually estimated based on the FFT spectrum of a digitalized sinusoidal signal as shown in figure 2.3.

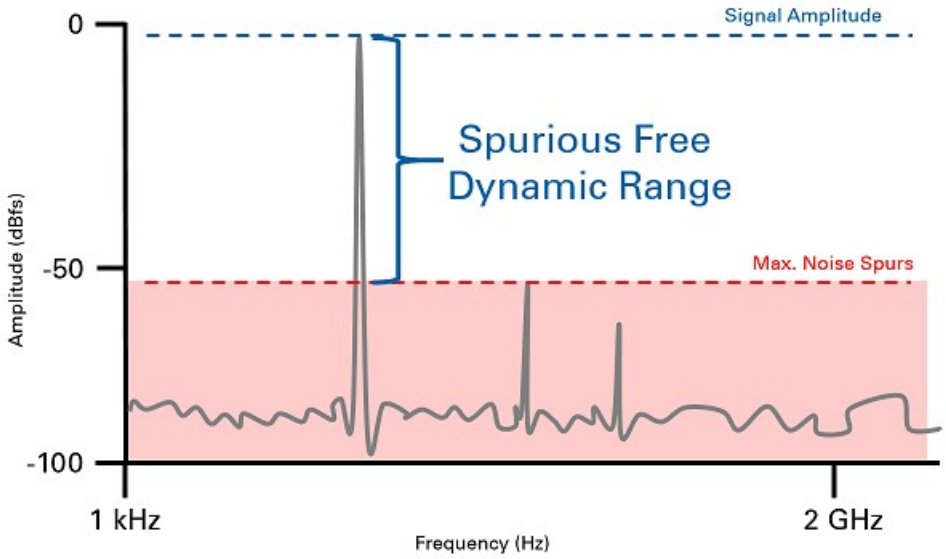

Figure 2.3: Exemple of the SFDR.

2.1.3 Static parameters

a. The offset error

It is the deviation of the output of the effective ADC's transfer function from the ideal ADC's transfer function. This deviation is constant for all values as illustrated in figure 2.4.

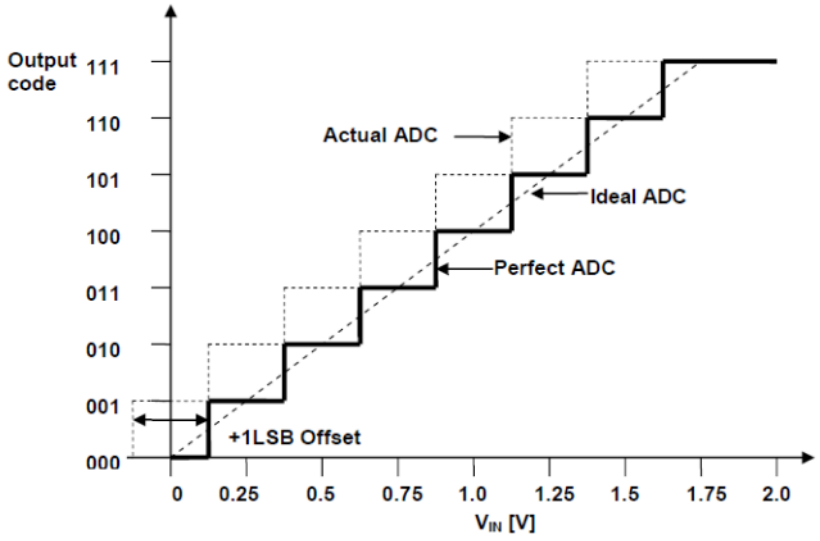

Figure 2.4: Exemple of the offset error, extracted from [7].

b. The gain error

Defined as the deviation of the slope of the output of the effective ADC's transfer function from the ideal ADC's transfer function one as shown in figure 2.5. This error is known to affect the DR of the ADC.

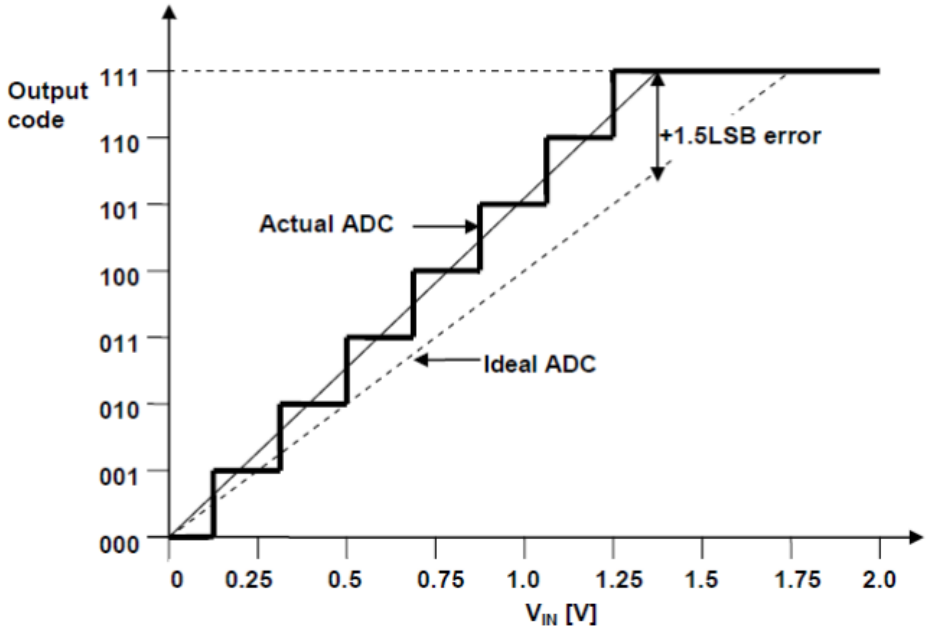

Figure 2.5: Exemple of the gain error, extracted from [7].

c. The Differential Non-linearity (DNL)

This parameter is defined for each digital word as the difference between its effective width and the ideal width (q=LSB):

$$DNL(k) = \frac{(X_{k+1} - X_k) - q}{q} \tag{2.11}$$

Where $(X_{k+1} - X_k)$ is the effective width of the digital word k. The minimum value of the DNL is -1 *LSB* which describe the case of a missing code $(X_{k+1} - X_k) = 0$. This means that an ADC with DNL error less than ± 1 *LSB* guarantees no missing code. Figure 2.6 illustrate an example of the DNL for a 3 bit ADC.

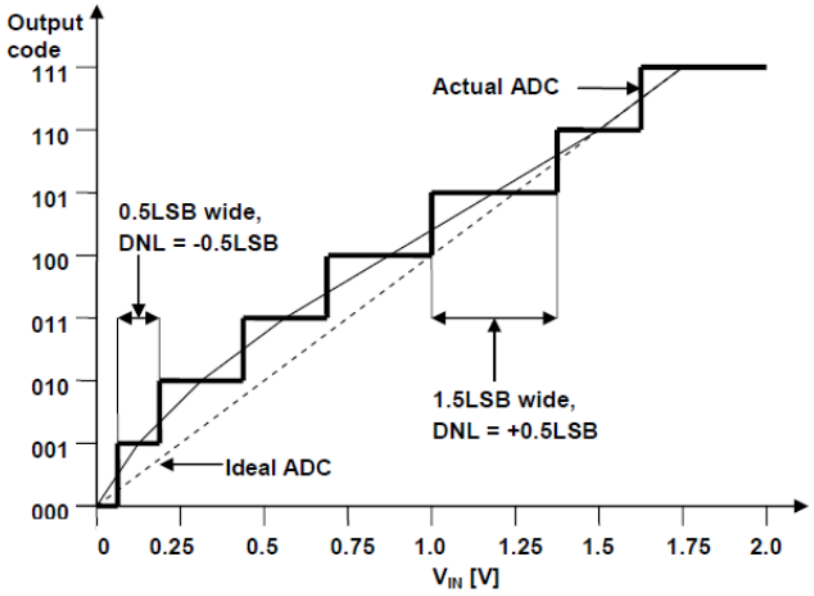

Figure 2.6: Exemple of the DNL, extracted from [7].

d. The Integral Non-Linearity (INL)

It describes the amount of the horizontal deviation of the curve that differences the effective ADC's transfer function from the ideal ADC's transfer function slope as shown in figure 2.7. For each code, the INL represent the cumulative sum of the Differential Non-Linearities (DNLs):

$$INL(k) = \sum_{i=0}^{k} DNL(i) \tag{2.12}$$

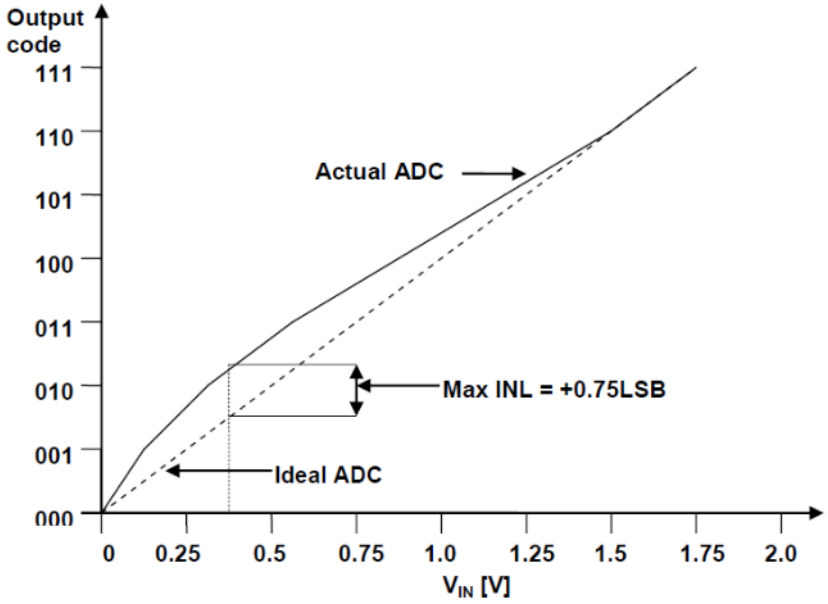

Figure 2.7: Exemple of the INL, extracted from [7].

e. The monotonicity

An ADC is monotonic when its output follows the direction of the input: the output increases with increases in the input, and never decreases (and vice versa). However, this does not guarantee that there will be no missing codes. Figure 2.8 shows an example of the monotonicity of a 3 bit ADC.

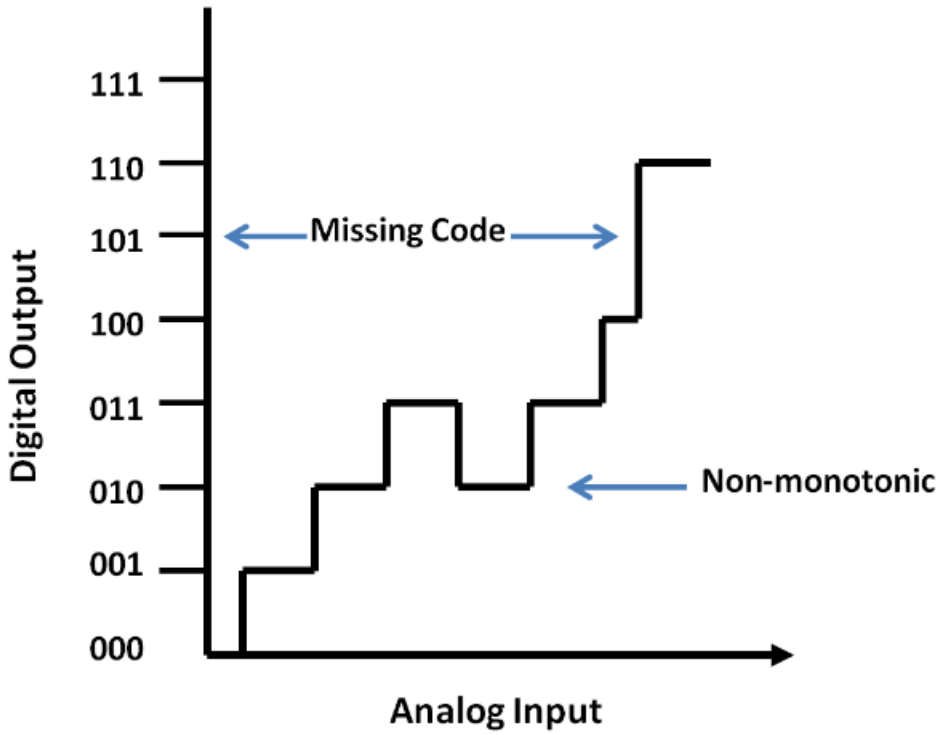

Figure 2.8: Exemple of the monotonicity of a 3 bit ADC.

2.1.4 The figure of merit FoM

This parameter reflects the efficiency of the ADC, it is used to describe the difficulty and complexity to achieve the requirements of the design of the ADC. There are two commonly used models to evaluate the FoMs of ADCs:

- The first one is called **"The Walden FoM"** described by the equation 2.13

$$FoM_{Walden} = \frac{P}{2^{ENOB} \times BW} \tag{2.13}$$

  Where: P is the power consumption of the ADC and BW is its bandwidth.

- The second one is **"the Schreier FoM"**[2], defined by the equation 2.14

$$FoM_{Schreier} = \frac{DR \times BW}{P} \tag{2.14}$$

[2]also known as "Rabii and Wooley FoM"

2.2 Class of architectures

ADCs can be divided into two classes: Nyquist-rate converters and over-sampling converters [5, 8]. The main difference lies in the compromise between ADC resolution and output sampling rate. A block diagram representation of a Nyquist-rate ADC and an oversampling Delta Sigma ADC (ΔΣ ADC) are illustrated in figure 2.9 (a) and (b) respectively.

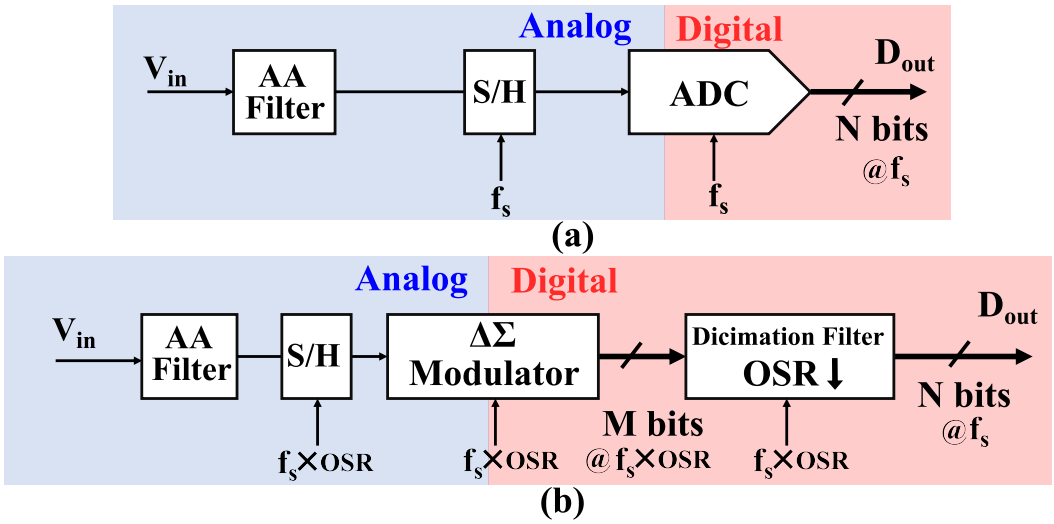

*Figure 2.9: **(a)**: Block diagram of a Nyquist-rate ADC;*
***(b)**: Block diagram ofan oversampling ADC.*

Comparing the two diagrams, the oversampling architecture requires more signal processing steps in order to digitize the information. These steps are related to the nature of the tradeoff between speed and resolution. The low-resolution high-speed digital signal in the output of the modulator block is filtered and down-sampled to achieve a high-resolution Nyquist rate signal. The benefits of this implementation will be explained and discussed below.

2.2.1 Nyquist-Rate Converters

A Nyquist-rate converter operates at the minimum sampling frequency necessary to digitize correctly the information of the entire considered input bandwidth. This sampling frequency is defined based on the famous "Nyquist criterion" that states a theoretical manner to uniquely reconstruct the signal. The criterion imposes a simple mathematical relation between a bandwidth (BW) and the minimum sample rate (f_s) [5]:

$$f_s > 2BW \tag{2.15}$$

Three of the most popular Nyquist-rate converters are SAR (successive approximation register), flash, and pipeline ADCs:

a. SAR ADC Architecture

A successive approximation register (SAR) ADC is based on the "Bisection method" (also called the interval halving method, the binary search method, or the dichotomy method) [9]. It is essentially built as a close loop system which is composed of a DAC, a digital control block and a single comparator that performs the binary search as shown in figure 2.10.

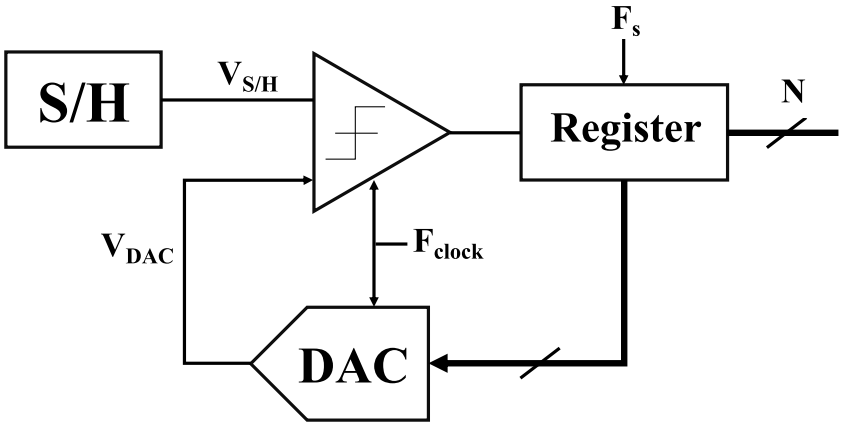

Figure 2.10: Block diagram of SAR ADC architecture.

This operation continues, approximating the input value with finer resolution each successive cycle until the least significant bit (LSB) is determined and the digital word is complete as illustrated in the example of figure 2.11.

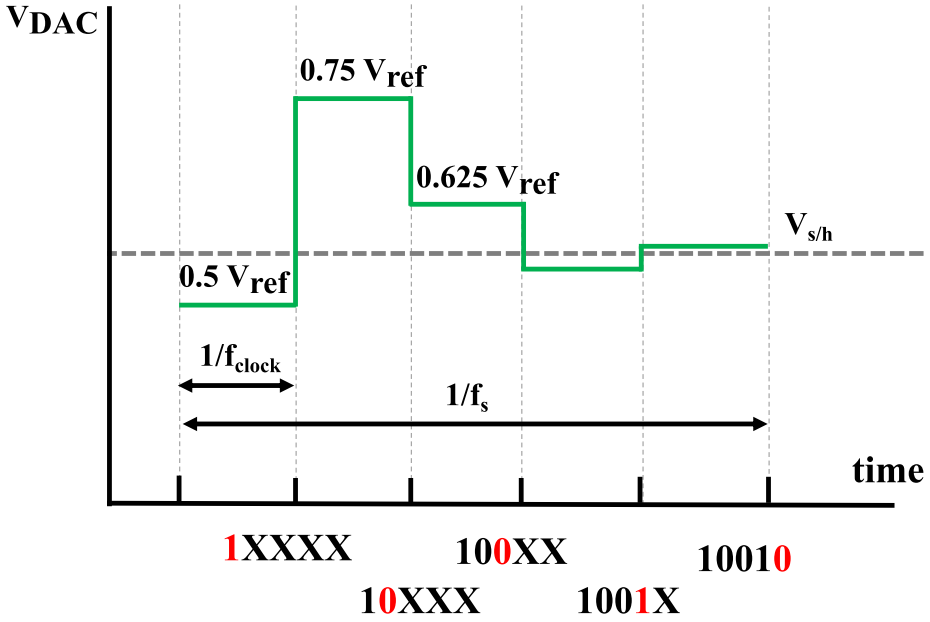

Figure 2.11: Exemple of an approximation sequence of a SAR ADC.

Since the SAR requires *N* cycles to produce an N-bit resolution output, the speed of state-of-the-art SARs is often limited to several MSPS [1]; however, this kind of architectures is known for its power efficiency due to the use of a single well-designed comparator and one DAC.

b. FLASH ADC Architecture

A flash ADC is constructed as a cascade of parallel comparators where the reference voltage system is a resistor-ladder [9] as illustrated in figure 2.12. This resistor-ladder is designed to divide the reference voltage into multiples of LSB in order to distinguish between inputs that differ by at least one LSB. The outputs of all the comparators then go into a thermometer encoder to convert it to a binary-weighted digital output.

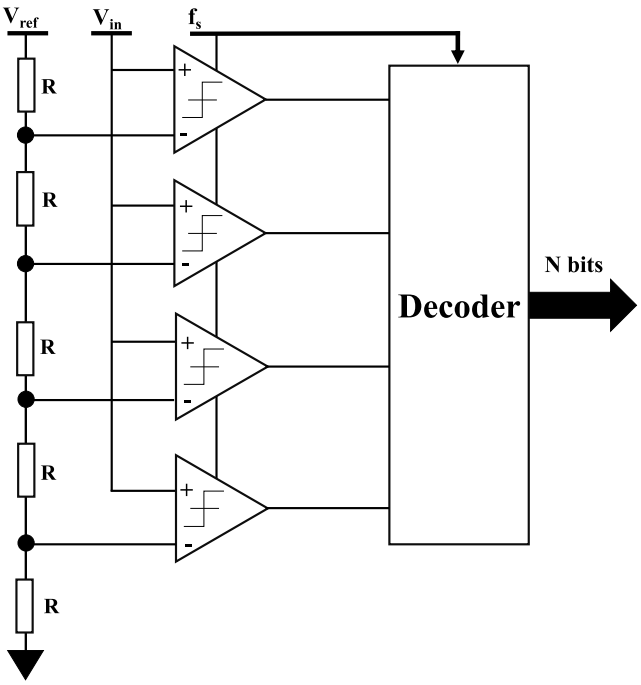

Figure 2.12: Block diagram of a FLASH ADC Architecture.

$2^N - 1$ comparators are required for a N-bit resolution flash ADC. With such inconvenient, this architecture is limited to low-resolution applications since every additional bit doubles the required number of comparators and hence, power consumption, total area, and the accuracy of each comparator [9]. Because of all this, flash converters are typically limited to 8-bit resolution.

c. Pipeline ADC Architecture

In behalf of using a comparator for every bit as in a flash ADC, the pipeline architecture employs multiple low-resolution flash conversion stages cascaded in series to form the pipeline as shown in figure 2.13.

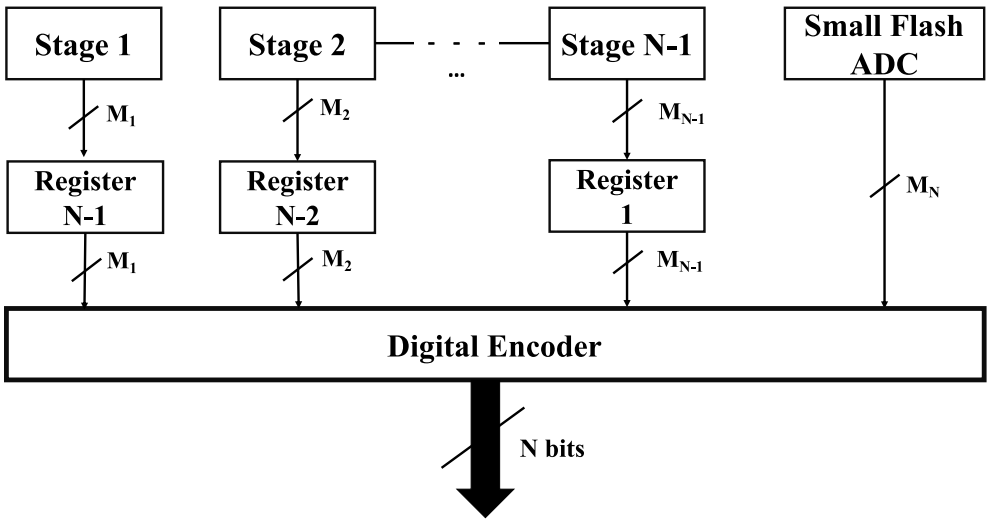

Figure 2.13: Block diagram of a PIPELINE ADC Architecture.

The architecture of each elementary stage is shown in figure 2.14. It is built from a first part based on a low-resolution flash ADC and a second part called "MDAC" (Multiply-DAC stage) composed of a DAC, an adder block and an amplifier.

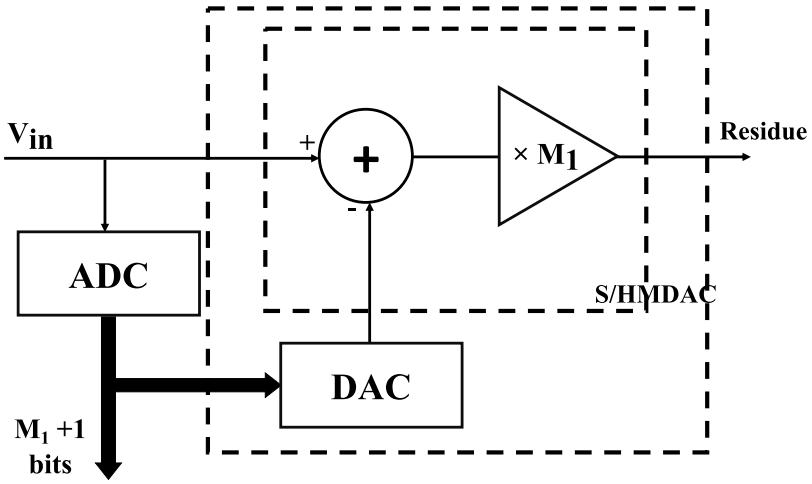

Figure 2.14: Block diagram of a MDAC.

Every stage in the pipeline receives an amplified residue of the previous stage [9]. This residue is the result of the subtraction of the quantified output (regenerated by the DAC of the previous stage) from the original input. This process is repeated as the signal passes through the pipeline until the LSBs are determined and the output of all the stages in the pipeline are combined using shift registers to form the total digital value.
Because of the simultaneity characteristic of the pipeline architecture, the ADC generates a digital word every clock cycle. This parallel processing allows the pipeline to offer high resolution at the full Nyquist rate of the converter. But the tradeoff is the latency of the pipe which is currently acceptable in many fields allowing the pipeline ADCs to become the standard in data conversion applications at 8-bit and higher resolutions for sampling rates from 5 MHz to 100 MHz [10]. Today this architecture can go up to 14 bits of resolution and more than 100 MHz of sampling rate [1].

2.2.2 Over-sampling converters

The different architectures presented above enable us to realize the analog to digital conversion for broadband signals where the frequency of sampling is limited to the Nyquist frequency. This second class of ADCs explore higher sampling frequencies than the Nyquist frequency. In order to present it properly, it is recommended to introduce the concept of oversampling first and its relashionship with the quantization error.

Above we explained that this error is approximated as white noise within a set of conditions. Thus, its power spectral density (PSD) $N_Q(f)$ is mathematically defined as [5, 6]:

$$N_Q(f) = \frac{A^2{}_{LSB}}{6 \times f_s} \tag{2.16}$$

Where:

- A_{LSB} is the physical value of the LSB related to its resolution N, defined by equation 2.1.
- f_s is the sampling rate of the ADC

We can see in figure 2.15 that the error spectrum is uniformly distributed over the band from 0 to $\frac{f_s}{2}$ which make the assumption that it is a white noise correct.

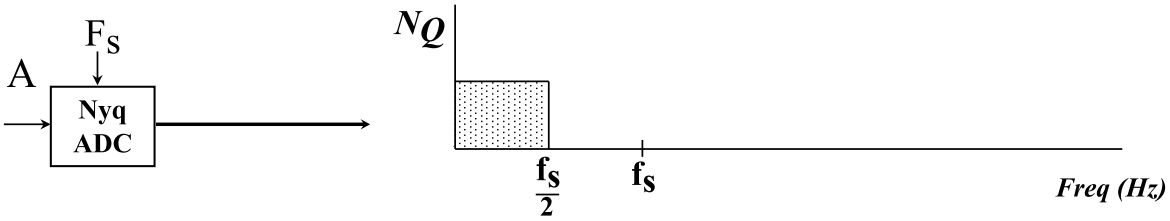

Figure 2.15: Power spectral density of quantization noise in Nyquist-rate ADC.

a. Oversampling

This concept is related to the quantization error defined above. It assumes that if we increase the sampling frequency over the Nyquist-rate, the error power will continue to spread uniformly over the new band, which reduce its density with the ratio of this sampling frequency over the frequency of Nyquist criterion. This ratio is called the oversampling ratio (OSR) [5, 11]:

$$OSR = \frac{f_s}{f_{s,nyq}} = \frac{f_s}{2f_b} \tag{2.17}$$

Now, if the output is filtered to the desired bandwidth (equals to the Nyquist frequency), the total power of the quantization noise is reduced as shown in figure 2.16.

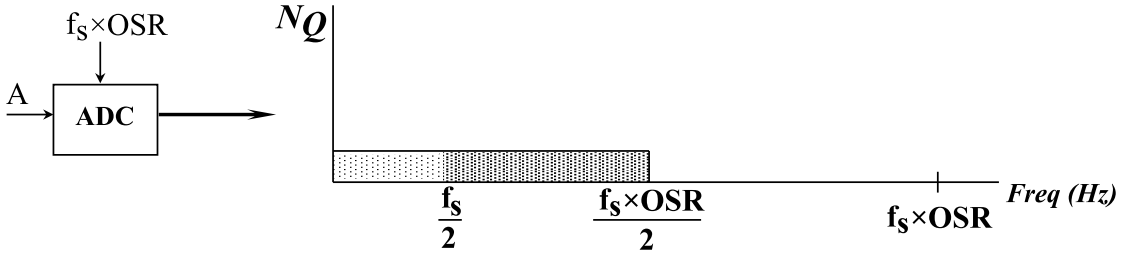

Figure 2.16: Power spectral density of quantization noise with oversampling.

Since the power of the input signal is not modified because we assume that its spectrum does not exceed the Nyquist frequency. The resulting in-band noise power density is given by:

$$N_Q(f) = \frac{A^2{}_{LSB}}{OSR \times (6f_b)} = \frac{N_{Q,Nyq}(f)}{OSR} \tag{2.18}$$

Using the same estimation, the maximum value of the SQNR achieved applying oversampling is (equation 2.19):

$$SQNR_{max}[dB] = 6.02 \times N + 1.76 + 10\log_{10}(OSR) \tag{2.19}$$

It shows that every time the OSR value is doubled, an improvement of 0.5 bit is achieved ($3\,dB/octave$). Here, we can notice that using simply the oversampling would never be sufficient. We need very high values of OSR in order to have a decent increase of ENOB. This leads to unfeasible hardware implementation due to the required high sampling frequency. A more efficient way to benefit from this concept is the use of the delta sigma modulation.

b. Delta Sigma ADCs

It was shown above that oversampling is used to boost the resolution using speed. The problem with this strategy is that speed is limited and we do not improve the resolution that much. This tradeoff can be extended by shaping the spectrum of the quantification noise.
Previously, the quantification noise had a flat spectrum. By pushing this noise outside the desired signal band as shown in figure 2.17, it improves considerably the resolution of the converter [11].

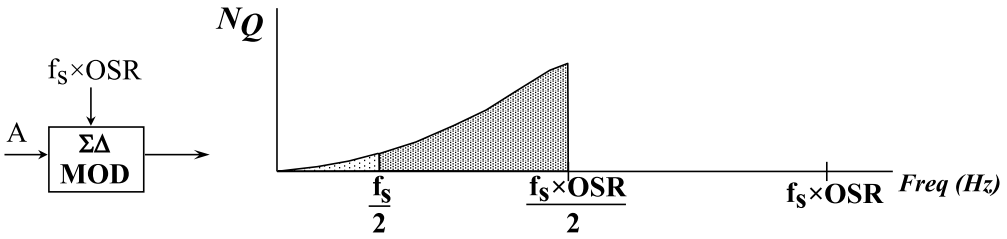

Figure 2.17: Power spectral density of quantization noise with oversampling and noise shaping.

The type of converter capable of applying such operation is the delta sigma ADC (ΔΣ ADC) [3] [8, 11]. In order to clearly explain the concept of noise shaping, a first order ΔΣ modulator illustrated in figure 2.18 will be used. It is composed of a filter (H(z)), internal ADC and an internal DAC for the feedback path. From this figure, the transfer function of H(z) which is a first order integrator is:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.20}$$

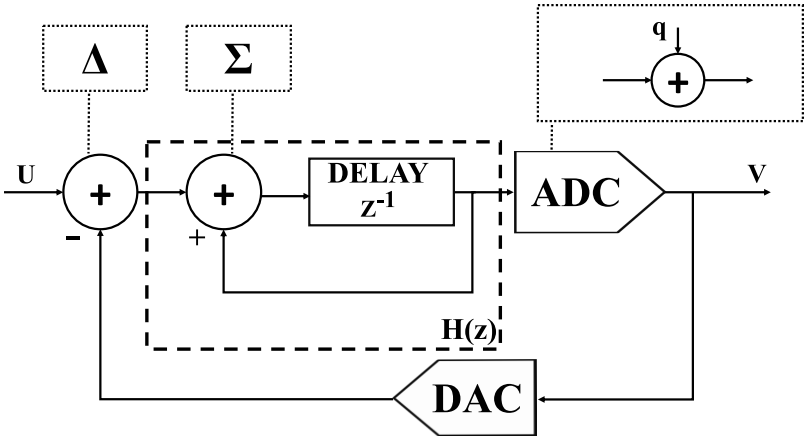

Figure 2.18: Block diagram of a ΔΣ ADC.

The best way to understand the mechanism of the ΔΣ ADC is to analyze its frequency domain representation. We can see that this system has two inputs U and q which means that we have two transfer function. The first function is related to the signal input, it is called the signal transfer function (STF) and in this case it is:

$$STF(z) = \frac{V(z)}{U(z)} = \frac{H(z)}{1 + H(z)} = z^{-1} \tag{2.21}$$

This shows that the input is transferred to the output without being affected. The second transfer function is linked to the quantification noise of the internal ADC. It is called the noise transfer function NTF and it is:

$$NTF(z) = \frac{V(z)}{Q(z)} = \frac{1}{1 + H(z)} = 1 - z^{-1} \tag{2.22}$$

The quantification noise is shaped by the first order high-pass filter represented by it is transfer function in equation 2.22. The degree of the modulator is related to the degree of the filter used to shape the quantification noise.

[3] The terms ΔΣ and ΣΔ are both used interchangeably. Historically, the term ΔΣ was used first, the difference precedes the accumulation operation. Thus, the first term is often preferred.

In this case, the SQNR is estimated to be [11]:

$$SQNR_{max}[dB] = 6.02N + 1.76 + 30\log_{10}(OSR) - 10\log_{10}(\frac{\pi^2}{3}) \tag{2.23}$$

From this equation 2.23, it is clear that we have a better improvement of the resolution compared to the oversampling only (see equation 2.19). It increases with the value of the OSR at a rate of 9 dB/Octave (1.5 bit/Octave). This result shows also that the performance of the first order ΔΣ modulator (in its simplest implementation, the loop ADC is simply a 1-bit ADC which is a comparator) is related directly to the OSR, which means the existence of a limit to the use of this modulator.

Moreover, it is important to note that oversampling converters have some interesting advantages over Nyquist-rate converters such as:

- **a simpler anti-alias filter** (and in some case, it is possible to take it off) due to the higher sampling frequency and the effect of the loop filter.
- **a more relaxed requirements for the analog circuitry** because of the effect of the loop filter, that attenuate many non-idealities and noise of the used analog blocks.
- **more flexibility** which is based on the the tradeoff between speed and resolution. An ADC can achieve a different resolution in a robust way just by changing the OSR. Also, the simplicity of its implementation.

C. Note about performance metrics for Delta Sigma ADC

Oversampling converters are characterized using AC specifications. The DNL and INL explained above cannot be correctly used since the output of an over- sampling converter depends on its previous state (Oversampling ADCs are not memoryless like Nyquist-rate ADCs) [12].

2.3 More about Delta Sigma ADC

In the previous section, a first order ΔΣ modulator was introduced to explain the concept of noise shaping. Here, a more detailed analysis is presented to clarify the fundamentals of this unique type of architecture followed by an introduction to our chosen topology.

2.3.1 Fundamental parameters: L, N, OSR

The example of the first order ΔΣ modulator shows that the improvement of the SQNR is linked to the value of the OSR (see equation). Yet, there is another parameter that impact the value of the SNR. Equation 2.24 shows the generic achievable SNR for a ΔΣ modulator [11]:

$$SQNR_{max}[dB] = 6.02N + 1.76 + (2L+1)\log_{10}(OSR) + 10\log_{10}(2L+1) - (2L)10\log_{10}(\pi) \tag{2.24}$$

This equation 2.24 introduces one more parameter: the order of the noise shaping L. In this case, the SQNR improves with the OSR at a rate of $6L+3\ dB/octave$ or $L+0.5\ bit/octave$. Figure 2.19 illustrates the value of SQNR for modulators with orders between $L=1$ (first order modulator using one integrator) and $L=8$. For example, for a modulator with an OSR of 64. Jumping from a first order loop filter (one integrator) to a second order modulator (two cascaded

integrators) will improve the SQNR by 30 *dB*: from 70 *db* to 100 *dB* as shown in figure 2.19. It is also important to not forget the impact of the internal quantizer resolution *N*.

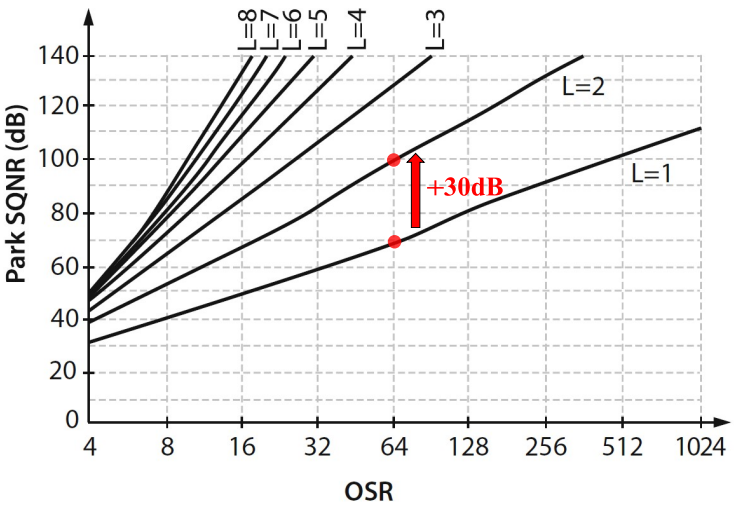

Figure 2.19: SQNR values for different orders of noise shaping and OSR value.

2.3.2 Discrete-time vs Continuous-Time Delta Sigma modulator

A ΔΣ modulator's loop filter can be whether implemented in discrete or continuous time [11, 8]; the main difference lies in the position of the sampling block. Figure 2.20 illustrates this.

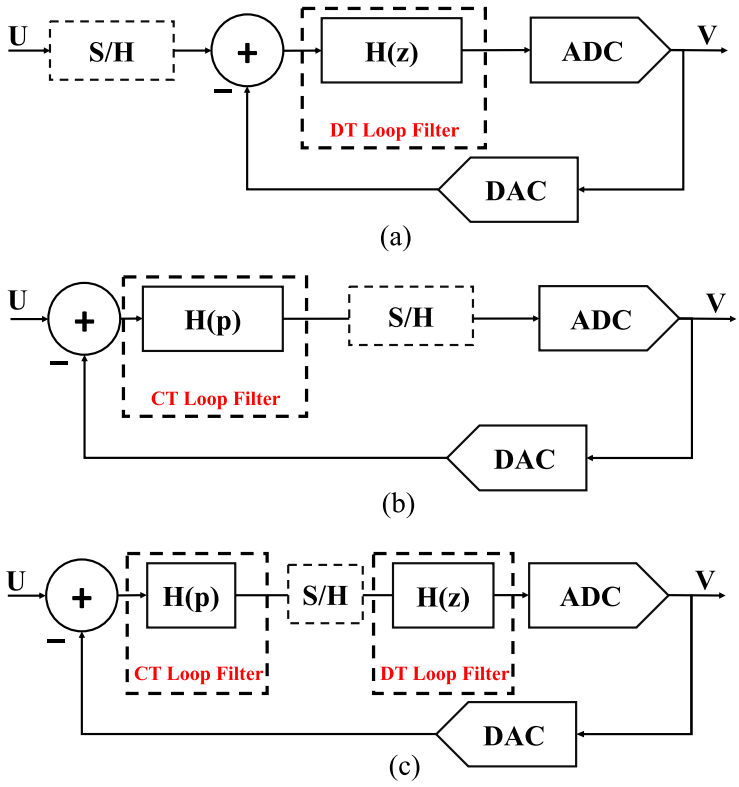

Figure 2.20: Implementation of a ΔΣ modulator with:
(a): DT loop filter;
(b): CT loop filter;
(c): Hybrid DT/CT loop filter.

In the DT case, the sampling block is located outside the loop (in the input) while it is inside the loop for the CT case. In the DT implementation, the loop filter H(z) is discrete time, implemented using switched-capacitor integrators. The feedback DAC is also designed using switched-capacitor architectures. While, in CT implementation, the loop filter is designed using continuous-time integrators. The feedback DAC can be implemented either in DT using switched-capacitor circuits or in CT using a current-steering architecture.

Recently, CT topologies have gained popularity in both academia and industry providing many interesting advantages over the DT ones. This renewed interest is mainly related to the simplicity of the sampler block and the inherent anti-aliasing feature due to the loop filter. Also, CT implementation is more power efficient more particularly in the case of wide band modulators because it requires less GBW for the integrators ($5 \times f_s$ in the case of DT, up to $1 \times f_s$ in the case of CT [13]).
A more detailed comparison [12] between the two implementations is presented in table 2.1

Table 2.1: Comparison of DT and CT ΔΣ modulation.

Performance	**DT**	**CT**
Sample rate	Filter scales to the sample rate, range of sample rates allowed	Sample rate is fixed within a window to fit to the filter shape
Jitter	Similar to normal sampling	When using current feedback it is more sensitive
Relative positions of poles and zeros in filter	Defined by capacitor ratios	Defined by the pairs of capacitors and resistors
Absolute value of filter parameters	Capacitor ratios and sample rate	Filter curve modulated by absolute spread of parameters
Relative and absolute accuracy of poles and zeros	<0.1%, 0.1%	0.5%, 15%
Single loop	Practical implementations are second order	Up to fifth order
Higher-order noise shaping	Cascade of lower order sigma delta modulators	Increase filter order
Linearity	Summation nodes and integrators	Mainly in first integrator
Opamp constraint	Runs at sample rate	Determined by filter
Power	In fast opamps	In linearity and noise of first integrator

2.3.3 High order Delta Sigma modulator

In this section, different implementations of high order CT ΔΣ modulators are presented. These architectures can be classified into two categories: single-loop and multiple loops as shown in figure 2.21 (a) and (b) respectively.

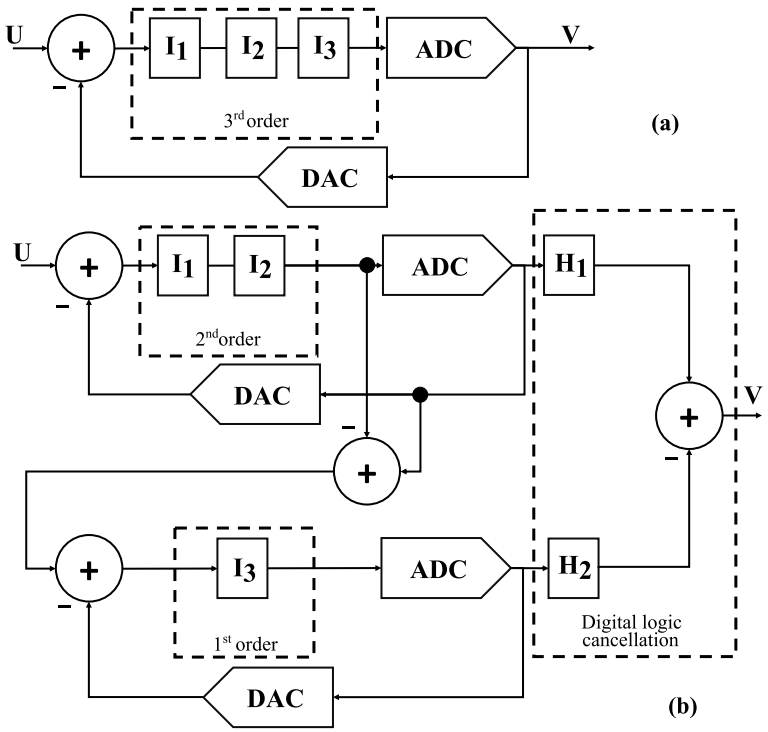

Figure 2.21: Example of implementation of a third order ΔΣ modulator:
(a): Single loop implementation;
(b): 2-1 MASH implementation.

a. Multiple-loop implementation (MASH)

In this implementation the noise shaping transfer function is decomposed into "low-order" stages as shown in figure 2.22. With this, high SQNR is achieved without affecting the stability of the system. This type of architecture is called Multi-stAge noise SHaping (MASH) structure [14, 11] because the shaping operation's order is the sum of every order stage used. To illustrate this, equation 2.25 describes the transfer function of the 2- 1 MASH modulator (When referring to a MASH ADC, the number of stages and the order of each stage are indicated. For example, a MASH 2-1 has two stages: the first stage is a second-order modulator, and the second stage is a first-order modulator) shown in figure 2.21 (b):

$$V = H_1 STF_1 \times U + (H_1 NTF_1 - H_2 STF_2) \times Q_1 - H_2 NTF_2 \times Q_2 \tag{2.25}$$

Where:

- STF_1 is the STF of the first stage
- NTF_1 is the NTF of the first stage
- Q_1 is the quantization error of the first stage
- STF_2 is the STF of the second stage
- NTF_2 is the NTF of the second stage
- Q_2 is the quantization error of the second stage

The digital logic cancellation block is designed to match the STF and NTF of the first and second stage as following:

$$H_1 = STF_2 \tag{2.26}$$

$$H_2 = NTF_1 \tag{2.27}$$

$$V = H_1 STF_1 \times U - NTF_1 NTF_2 \times Q_2 \tag{2.28}$$

With this, we achieve the order of the noise shaping without affecting the input signal. Moreover, if each stage uses second-order (or lower) noise shaping, the structure is guaranteed to be stable.

One of the most interesting characteristics of the MASH topology is the flexibility of design of each stage, since it can be implemented using different ADC types. This allows to achieve high SQNR at low OSR. Figure 2.22 shows the general representation of a MASH structure:

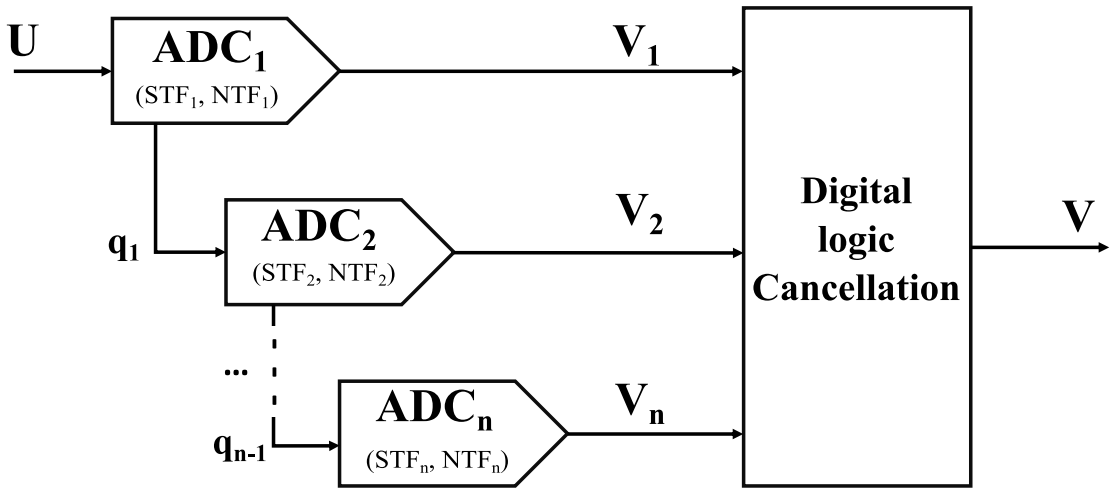

Figure 2.22: Block diagram of MASH Architecture.

As explained above, the error cancellation logic eliminates the quantization error of all stages except the last one giving a general output function represented by equation 2.29.

$$V = U \times STF_1 STF_2 ... STF_n + Q_n \times NTF_1 NTF_2 ... NTF_n \tag{2.29}$$

The main issue of the MASH structure is the design of this logic. In practice, it is delicate to achieve a full matching and cancel the error, this problem is called quantization noise leakage and it causes a degradation of the SQNR. Another downside is the requirement of the DC gain of the integrators that is more significant than the case of the single-loop. In the case of MASH structures with low OSR values, this gain needs to be at least in the range of OSR^M while in the case of single loop it is generally in the range of OSR.

b. Single-loop implementation

This type of architectures is built using a cascaded integrators structure in the direct path. The number of integrators represents the order of the modulator as shown in figure. Since the gain of the loop is very high, this implementation is known to be relatively robust against analog imperfections. Yet, in order to achieve high SQNR while maintaining the stability of the modulator, a system of compensation is needed. The goal is to introduce zeros in the open-loop transfer function to compensate the poles of the filter, this allows to have a robust phase margin. There are three kinds of compensation: feedforward, feedback and a combination of both [11, 14, 8] as illustrated in figure 2.23.

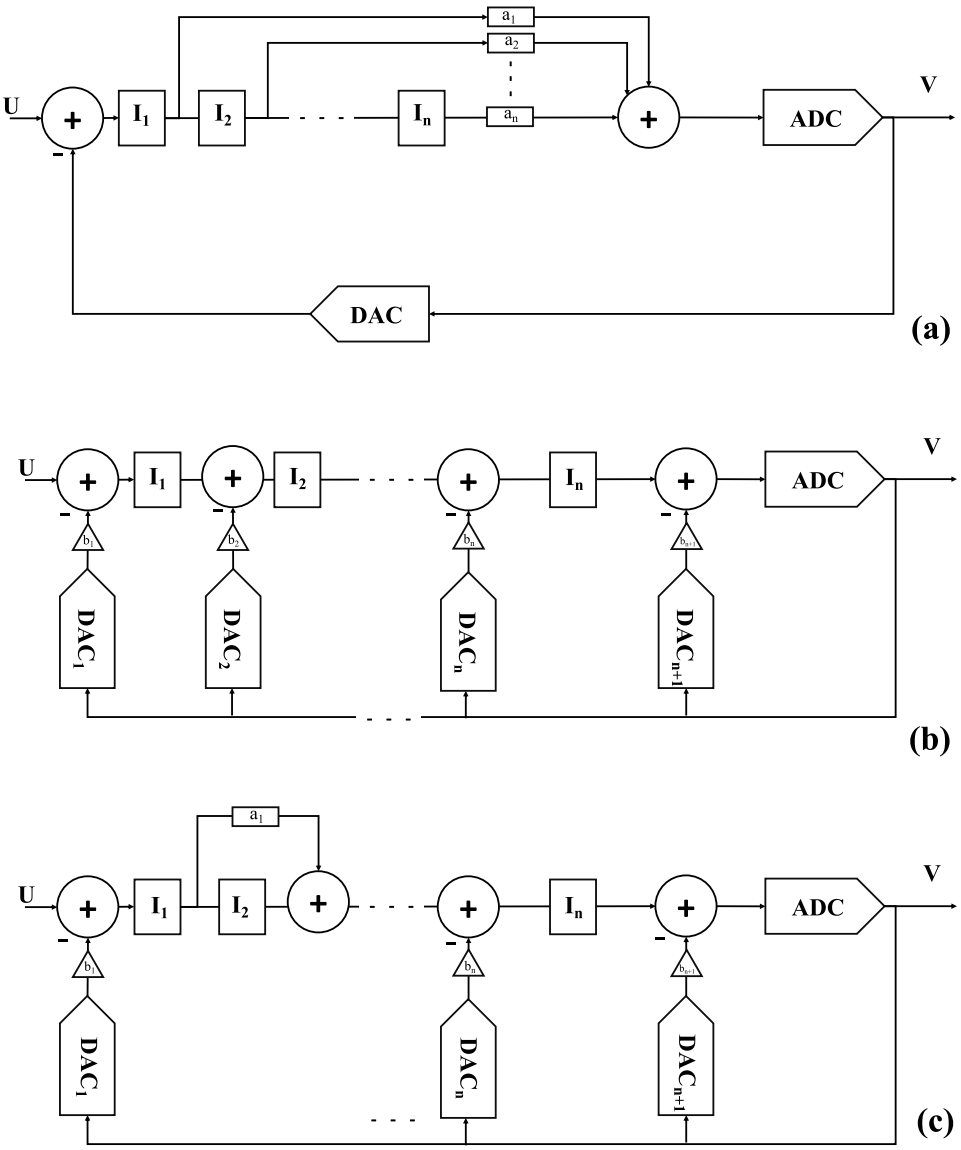

Figure 2.23: Different styles of compensation:
(a): Feedforward loop filter;
(b): Feedback loop filter;
(c):Mixed feedforward-feedback loop filter.

The feedforward implementation is more power efficient since the voltage swing of the integrators of the loop is directly linked to the reference voltage. It is also more linear, because there is a direct path between the input and the output, allowing the loop to filter the noise separately. Yet, this implementation decreases the anti-aliasing performance of the modulator due to the direct path between the input and the output, which requires adding an anti-aliasing filter. With this, the area and consumption of the modulator increases significantly.
In the other hand, the feedback implementation enhances the anti-aliasing feature of the modulator but it requires adding a DAC for every feedback coefficient which increases the power consumption. It also involves adding more requirement on the performances of the integrators because each output injected in the internal nodes affects linearity and stability.
A good tradeoff is the use of a mix between the two implementations in order to keep an acceptable power efficiency without losing the anti-aliasing performance.

2.4 Summary

We dedicated this chapter to introduce fundamentals about ADCs that are necessary for the comprehension of the thesis. We focused mainly on the presentation of the ΔΣ ADCs in the space of analog to digital conversion and the theoretical aspects of it. This information will be used to argument different choices for our proposed topology and to evaluate its performances.
In the next chapter, we introduce the proposed architecture and the methodology of behavioral simulation developed to study the imperfections of this topology. Non-idealities are identified and modeled allowing to check the effect of every design choice before going to the implementation. This reduces considerably the amount of time and effort applied during the schematic design phase.

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3

System level modeling

This chapter is dedicated to the presentation of the proposed topology, its specifications and the method of modeling used to extract different information about the behavior of each building block. Results of simulation using SIMULINK models are discussed.

Contents

3.1 Choice of topology

To respond correctly to the need explained in section 1.3, we are targeting the specifications summarized in table 3.1. We decided to work on slightly larger specifications than what is required in order to keep some tolerance for any cause of degradation.

Table 3.1: Proposed specifications of the CT ΔΣ ADC.

Parameter	**Value**
Signal bandwidth	40 MHz
OSR	8
Loop filter order L	5
Loop ADC resolution N	3 bit
Sampling frequency	640 MHz
Theoretical SQNR	80 dB
Linearity	<0.2%

The proposed topology is chosen to combine the benefits of the CT implementation and the single-loop one using a mixed feedforward-feedback compensation style which are detailed in the subsection 2.3.3. More details about the implementation are discussed below. Figure 3.1 illustrates a simplified block diagram of the proposed modulator.

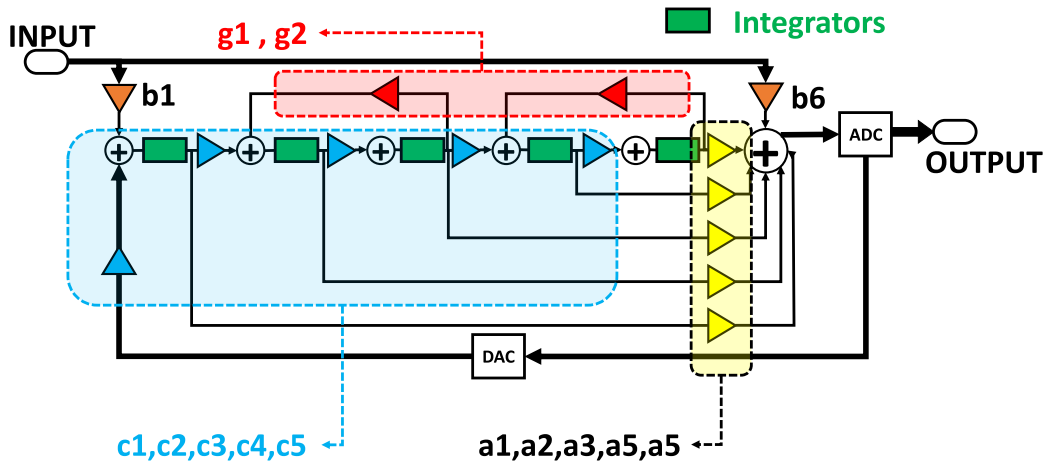

Figure 3.1: A simplified block diagram of the proposed CT ΔΣ modulator.

This type of architectures is known by "Cascaded Resonators Feedforward" or CRFF because it embedded not only integrators but also resonators (each resonator is composed of two cascaded integrators and a feedback path, in figure 3.1 the two resonators are identified by the feedback path coefficients g_1 and g_2 respectively) . To clarify this, we detail here the advantages of each choice:

- A very low OSR of 8 was chosen to limit the sampling frequency of the circuit at 640 MHz which is already challenging in both the design of the analog part and the digital part (the decimation filter). This allows us to achieve the targeted bandwidth while preserving the SQNR with the minimum increase of power consumption.
- A 3 $bits$ quantizer is used inside the loop to compromise the choice of a low OSR. This quantizer combined to a 5^{th} order loop filter guarantee the achievement of the targeted

specifications as calculated by equation 3.1.

$$SQNR_{max}[dB] = 6.02N + 1.76 + (2L+1)\log_{10}(OSR) + 10\log_{10}(2L+1) - (2L)10\log_{10}(\pi) \tag{3.1}$$

To validate this choice, we plotted the equation 3.1 for different values of OSR and degree of the modulator as shown in figure 3.2.

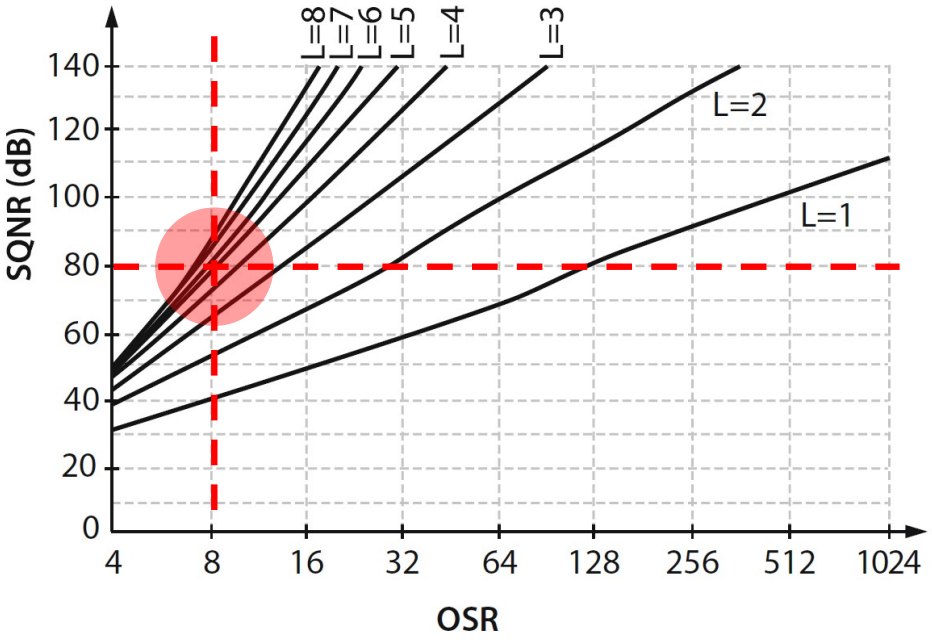

Figure 3.2: SQNR values for different key parameters.

It is already shown that the theoretical SQNR is usually chosen to be 10 – 20 dB higher than the required one in order to provide some tolerance for the inevitable degradation caused by the circuit non-idealities and to allow as much as possible of the noise budget for thermal noise.

- This allows us to benefit from both feedback and feed-forward advantages : we ensure more stability using the feed-forward paths to control the placement of the NTF's poles and zeros and thus the NTF gain. These paths also enables a small output swing of the first integrator (larger open-loop gain, and hence lower performance requirements on the following stages).
- Only one feedback DAC is enough for this architecture, limiting the source of non-idealities in the feedback path which are not filtered by the loop filter and affects directly the overall perfomance of the ADC. This allows also more area and power efficiency.

3.2 System-level simulation

In this section, we detail the approach used to simulate the behavior of the proposed topology. We are adopting a "top-down" design methodology approach. This choice involves the implementation of a mathematical model that describes the behavior of the system allowing us to define the specifications of each block and the study of the effect of every choice. This solution is implemented using MATLAB SIMULINK following a Model-Based Design approach.

3.2.1 Model-Based Design approach

Model-Based Design is a modeling paradigm that uses computational building blocks to represent continuous-time and discrete-time systems [1]. Instead of complex mathematical structures and extensive codes used in the traditional design methodologies, these models are implemented into a graphical environment allowing more flexibility and clarity of use such as SIMULINK. These enable us to achieve faster and more cost-effective development of complex control systems, signal processing, and communications systems.
Classically, the high-level design based on algorithm implementation (C or HDL) is done manually. This process is limited in terms of complexity, it takes a huge amount of time and results in a lot of ambiguities in terms of defining correctly the compromises and the impact of requirements on each other. Using Model-Based Design, we use the graphical blocks that models each function of the system to derive and analyze the low-level requirements which is so difficult or even impossible using the manual method. These models can be used to generate automatically an HDL representation of the system. Thus, the simulation results of the graphical model can be used to validate the HDL before going into the hardware implementation that will be used as a test bench for the transistor level implementation. This methodology allows us to reduce the amount of time and inefficiencies between these important design steps. Figure 3.3 shows a generic representation of the Model-Based Design workflow and the interaction between the results of every step.

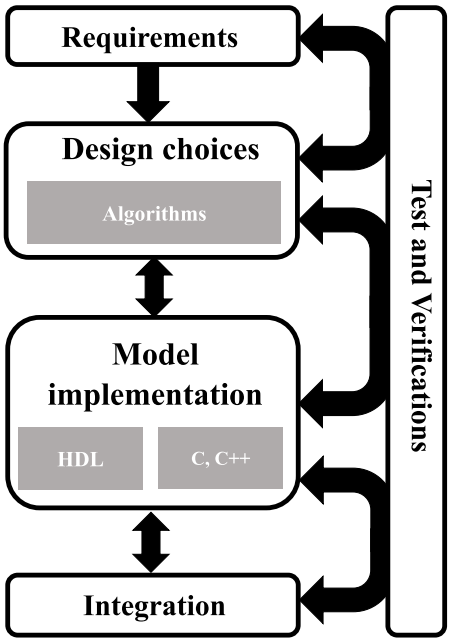

Figure 3.3: A generic representation of the Model-Based Design workflow.

Generally speaking, we can represent the modeling workflow of any systems in six steps:

- **Defining the architecture of the system**: Describing the system as a set of elementary functions to simplify the process. Every block/function will be modeled as a component. After the validation, the components will be integrated as a full system.
- **Identifying the features of the system**: Key-parameters, the different states of the system and the signals (inputs and outputs). We do this operation for every component of the system.
- **Mathematical modeling**: In this step, we use the extracted characteristics of the previous step to formulate the mathematical equations that describes every component of the system.

Usually, with a good decomposition, we manage easily to find this in the state of the art.

- **Building the model**: In our case, we use SIMULINK block diagram environment. It allows to translate the mathematical formulation into a graphical representation for every component of the system. After that we can integrate them into a complete model of the system.

- **Creating the simulation benches**: SIMULINK offers an interactive enviroment to implement different scenarios (changing parameters, defining inputs, debugging and tracking the flow of every function) to run the models. We will see also how to combine MATLAB scripts with SIMULINK to make more complex analysis simulations.

- **Validating the simulation results**: MATLAB and SIMULINK provide multiple toolboxes to analyze and evaluate the simulation results.

Figure 3.4 illustrates a flowchart of the implementation of these steps using Model-Based Design in the case of designing ASICs.

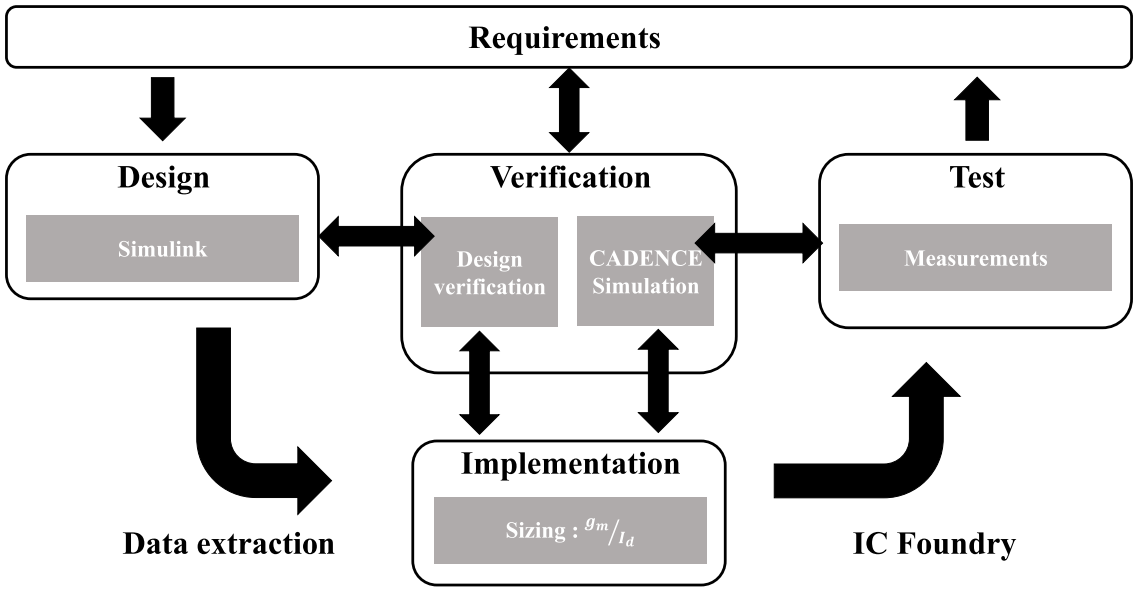

Figure 3.4: Flowchart of the implementation of Model-Based Design for ASIC design.

It should be noted that our proposed workflow is inspired from the development done in [2]. To improve the use of graphical models for more complex simulation and analysis, we decided to improve the workflow by control the simulations using developed scripts that describes different type of situation, from the synthesizing of the modulator to the study of the impact of the non-idealities linked to each building block. More precisely, combining SIMULINK with MATLAB scripts enables to simulate - given a set of conditions described in the scripts - the effect of the variations of each main parameter of the chosen topology. This permits to extract information about the critical parameters so we can optimize the design of each constructive block. A diagram of the interaction between MATLAB and SIMULINK in our proposed workflow is illustrated in figure 3.5.

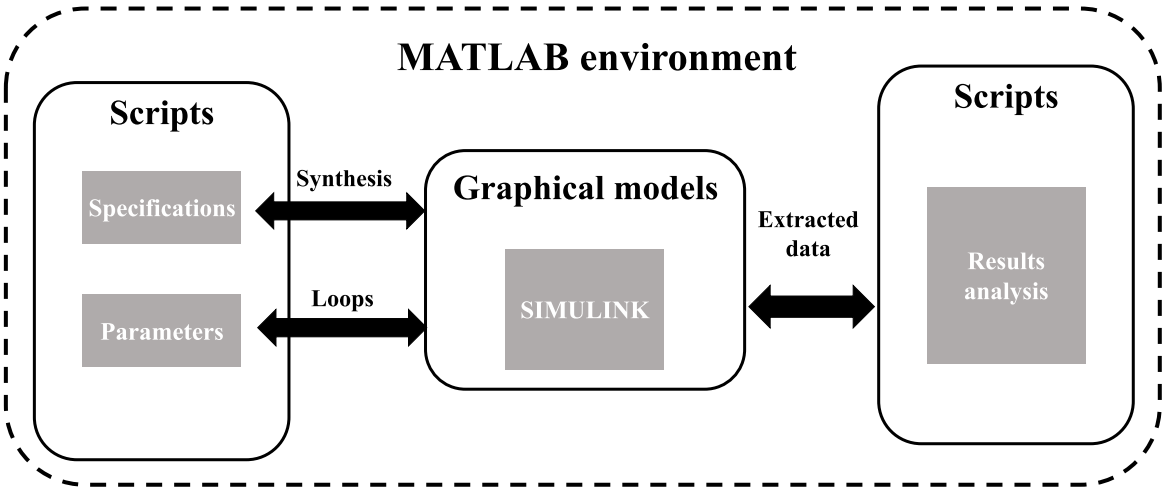

Figure 3.5: A diagram of the interaction between MATLAB and SIMULINK in our workflow.

3.2.2 Integration of Schreier's toolbox

As shown above, the first three steps of modeling requires a lot of experience and time to try different possibilities, in order to achieve the targeted specifications. In the case of high order CT $\Delta\Sigma$ architectures, this process is very difficult, due to the diversity of topologies and the complication of its mathematics. Fortunately, this process can be performed using a toolbox developed specifically for MATLAB. This famous toolbox is known as **"Schreier's Toolbox** [3] [1]. It is mainly used to synthesize complex L^{th} order modulator structures based on the NTF function. The toolbox is composed on more than 100 functions enabling:

- both discrete and continuous time modulator design;
- low-pass and band-pass modulators;
- support diffrent loop filters structures;
- synthesize loop coefficients for all these structures;
- simulate and analyze the modulator: stability, dynamic range scaling, SNR estimation and more.

In our case, we integrated this toolbox in the scripts used to generate the coefficients of the loop and extract useful information about the proposed architecture. Figure 3.6 shows the integration of this toolbox in our proposed workflow. The toolbox receives the requirements introduced by the user: type of the architecture, OSR, OBG, L and the bandwidth. It calculates the coefficients that we use to complete the graphical model of the modulator. After this phase, we can apply different testbenches on this model and analyze the obtained results.

This toolbox calculate the loop coefficients based on a set of parameters that describes the targeted architecture. This calculation is detailed in [3]. A simpler way to explain it is to use the flow chart illustrated by figure 3.7. Here we can observe the interaction between the different key functions of **Schreier's toolbox** in order to calculate the coefficients. We start by defining the OSR, the type of modulator (LP or BP), the resolution of the loop ADC and the OBG. The toolbox calculates a first NTF and map it to the proposed topology (in our case a CRFF). In the case of CT implementation, it takes into account the type of the DAC and calculate the state-space-description of the modulator which is represented by the matrix ABCD. This matrix is scaled and optimized

[1] Richard Schreier

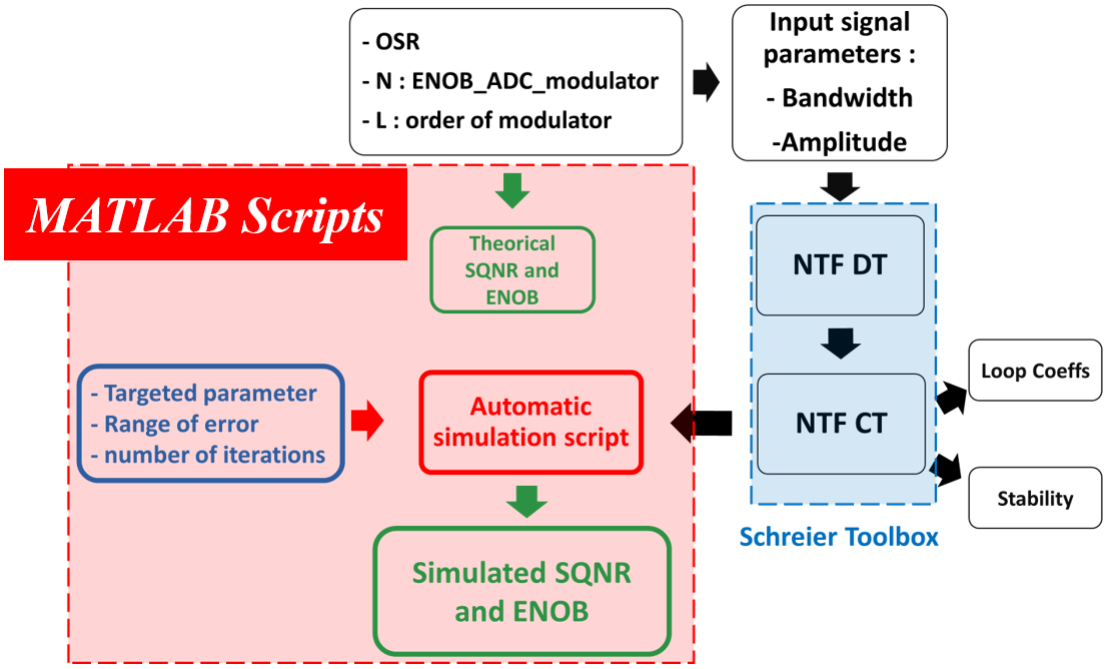

Figure 3.6: The integration of Schreier's toolbox in our proposed workflow.

to guarantee the stability of the modulator and used to redefine the NTF and in the prediction of the behavior of the modulator (Theoretical value of SQNR). It should be noted that the calculated coefficients of a CT structure are mapped to an equivalent DT values to be used in a discrete model in SIMULINK, this helps to accelerate the simulations [2, 3].

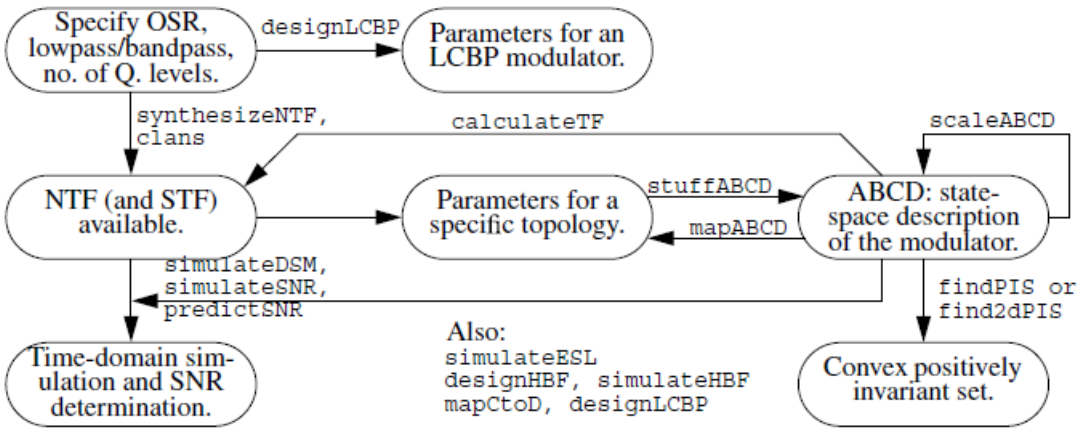

Figure 3.7: Flowchart of key Schreier's toolbox functions, extracted from [3].

3.2.3 SIMULINK model

The next step of modeling our proposed topology is to build it as a SIMULINK model. The first component to model is the core of this topology, which is the integrator. It should be noted that all the elementary blocks are availble by default in SIMULINK library. We used the same modeling blocks as described in [2].

As shown in figure 3.8 , the integrator is mainly build as a discrete ***Delay*** z^{-1} elementary

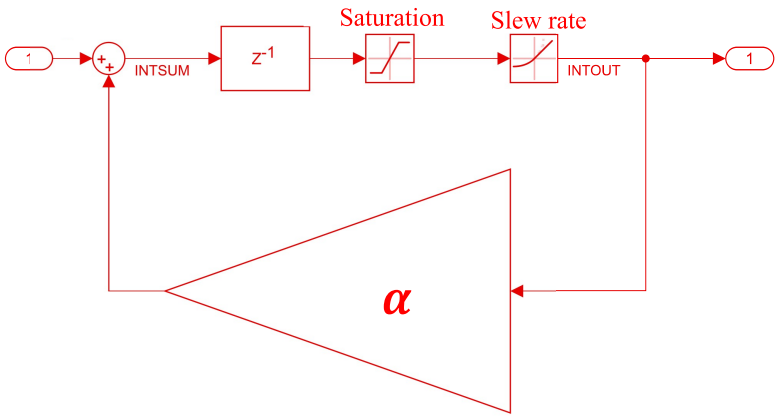

Figure 3.8: Graphical model of the integrator in SIMULINK.

block used in a feedback to an elementary ***adder***. To bring it closer to the real implementation of an analog integrator, we firstly considered adding the effect of the finite gain of the amplifier used in to implement it. This feedback coefficient is used to model the finite DC gain of the amp (A_0) with: $A_0 = 1/(1-\alpha)$. Thus, the transfer function of this block is:

$$H(z) = \frac{z^{-1}}{1 - z^{-1} \times \alpha} \iff H(z) = \frac{z^{-1}}{1 - z^{-1} \times \frac{A_0 - 1}{A_0}} \tag{3.2}$$

For A_0 high enough, the integrator can be seen as an ideal DT integrator. The equivalence between this and the CT integrator is shown further in the subsection 4.2.1.
After that, we represented other non-idealitites such as the saturation to the finite supply voltage (that causes the clipping effect) and also the slew rate using respectively a ***Saturation*** and ***Rate limiter*** default blocks. The values of all the parameters of these blocks are adjustable via the MATLAB scripts.

All the feedback and feed-forward paths are modeled as signals with gain blocks and elementary ***adders*** to subtract the values.

Th loop quantizer is modeled using the default SIMULINK ***quantizer*** block. This elementary block allows us to select the value of the LSB. We shifted the signal before and after the quantification using an elementary ***bias*** block in order to turn this quantizer to a mid-rise type. An elementary block of ***saturation*** is added to choose the resolution of the quantizer N by defining the value of the FS. Figure 3.9 illustrates this quantizer.

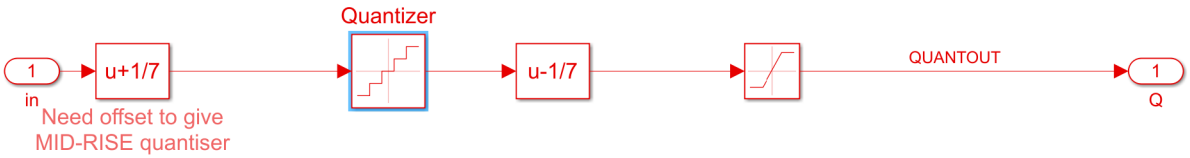

Figure 3.9: Graphical model of the Loop quantizer in SIMULINK.

In order to represent the equivalent nyquist rate sampled (non oversampled) reconstructed signal, we used ***the analog filter design*** block, which is available in SIMULINK in the ***DSP System toolbox***.

The full model of our proposed architecture -illustrated in figure 3.10- is used in a benchmark model that allows us to select several input signals and visualize and analyse its response.

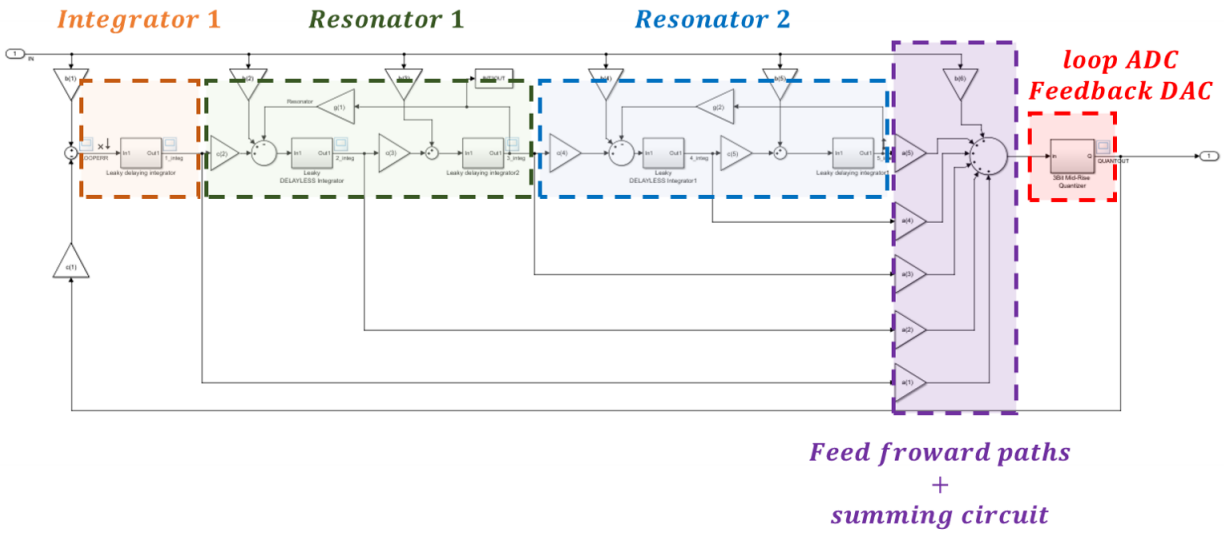

Figure 3.10: Graphical model of the proposed modulator in SIMULINK.

Figure 3.11 illustrate this benchmark model (with the modulator and the decimation filter). The different input signals will be presented in each study further in this document. The ***time scope*** block is used to monitor the transient response of the modulator in different interesting nodes. The values of the output are extracted to the workspace of MATLAB to apply signal analysis scripts using the SIMULINK block ***to workspace***.

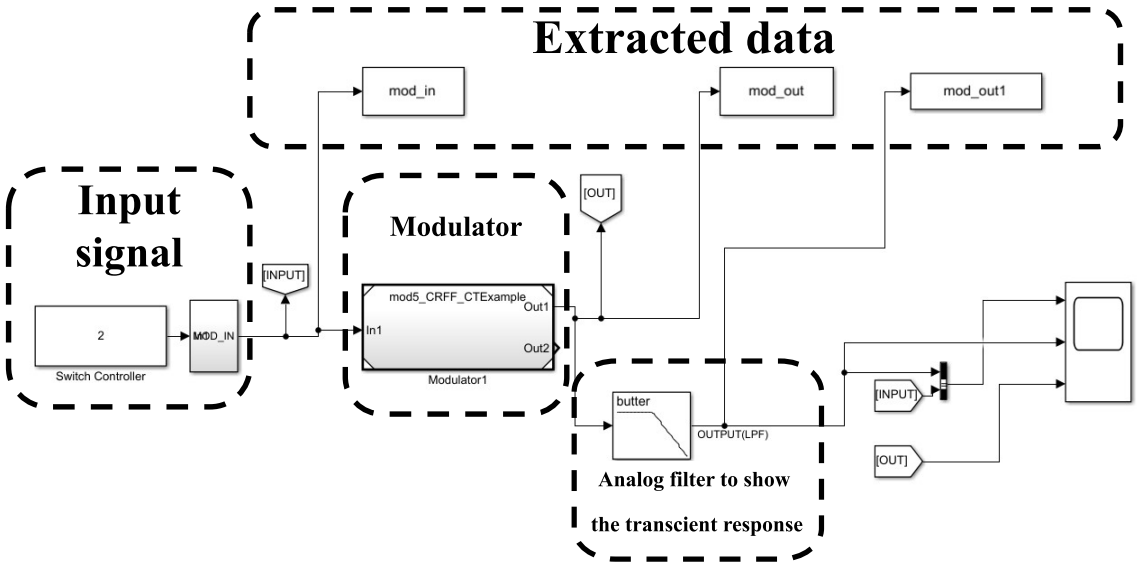

Figure 3.11: Graphical model of the proposed benchmark model in SIMULINK.

3.3 Simulations and results

As explained in the beginning of this chapter (figure 3.5), we combine the SIMULINK model with a set of scripts that enables us to analyze in a more efficient and deeper way the behavior of the proposed topology. In this section, we describe details about the scripts and we give an interpretation of the obtained results.

3.3.1 The script to synthesize the modulator

This script is used to calculate the coefficients of the modulator using **Schreier's toolbox**. It is composed of two parts:

- **A theoretical estimation algorithm**: we evaluate the theoretical impact of the choice of the main parameters (resolution of the loop ADC N, OSR and the order of the modulator L) on the SQNR using equation 3.1. In MATLAB, this equation is implemented using ***MATLAB Symbolic Math Toolbox***.

- **Executing Schreier's toolbox**: in this part, we define the type of the architecture then we run the **Schreier's toolbox** to obtain the coefficients and a predicted behavior of the proposed model. In order to validate this results, we inject this calculated values into SIMULINK model and we run a characterization simulation.

a. Algorithm

The algorithm of this script is illustrated below.

Algorithm 1: Synthesizing of the modulator

Input:

OSR // Oversampling ration
A_{in}, F_{in} // Sinewave input parameters
OBG // The out-of-band gains
L // Order of the loop filter
N // resolution of the loop quantizer
DAC // Type of the feedback DAC, in our case NRZ
$Modulator\ type$ // In our case CT, CRFF
K // Number of iterations
α // Parameter used to define different input amplitude levels

Output:

a_s, b_s, c_s, g_s // Calculated Coefficients using Schreier's toolbox
$SQNR_t$, $ENOB_t$ // Calculated SQNR and ENOB using equation 3.1
$SQNR_p$, $ENOB_p$ // Predicted SQNR and ENOB using Schreier's toolbox
$SQNR_s$, $ENOB_s$ // Calculated SQNR and ENOB for simulation

Function `SynthesizeMod(`OSR, A_{in}, F_{in}, OBG`):`
  Calculate $SQNR_t$, $ENOB_t$ using equation 3.1
  Execute Schreier's toolbox

  return a_s, b_s, c_s, g_s, $SQNR_t$, $ENOB_t$, $SQNR_p$, $ENOB_p$

Procedure `SimulateMod(`a_s, b_s, c_s, g_s, A_{in}, F_{in}, K, α`):`
  // In the case of simulating the behavior of the modulator for different amplitude levels $A_{in}(i)$, $K > 1$
  while $i \leq K$ **do**
    Inject a_s, b_s, c_s, g_s in SIMULINK Model
    Run Simulation using sinewave with $A_{in}(i) = FS - \alpha(i), F_{in} = 35\ MHz$
    Calculate $SQNR_s(i), ENOB_s(i)$ using the digital output of the model
    Increment i
  end
  return $SQNR_s(i), ENOB_s(i)$

b. Results of the script

The results of the theoretical estimation algorithm for an OSR of 8, a loop filter order of 5 and a loop quantizer of 3 *bit* applying equation 3.1, give us a theoretical SQNR of 80 dB which confirms the choice of the main parameters.

These parameters are injected into the SIMULINK model to run the **Schreier's toolbox**. The topology is defined as a CRFF type and the OBG value used is 3.7 [4]. The obtained coefficients are summed up in table 3.2. The obtained coefficients are used to calculate values for the component for the implementation of the modulator such as the values of resistors and capacitors. The toolbox plots the frequency response of the synthesized NTF and STF of the targeted modulator as shown in figure 3.12.

It plots also a theoretical prediction of the behavior of the system and the values of the SQNR for different amplitude levels. Both are illustrated in figure 3.13

Finally, it plots the DT equivalent pulse response of the CT loop filter that will be used to simulate the modulator. Figure 3.14 shows this.

Table 3.2: Coefficients of the loop filter.

Coefficient	a_i	g_i	b_i	c_i
1	4.4392	0.0493	0.2102	0.2102
2	6.3822	0.2762	0	1.1023
3	3.4840	-	0	0.9044
4	1.8533	-	0	0.7257
5	0.0382	-	0	0.4537
6	-	-	1.0000	-

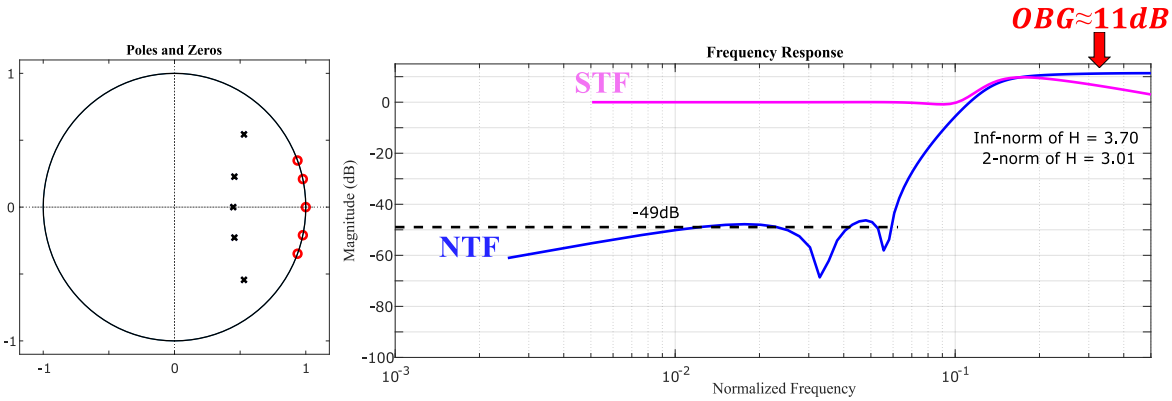

Figure 3.12: The frequency response of the synthesized NTF and STF of the targeted modulator.

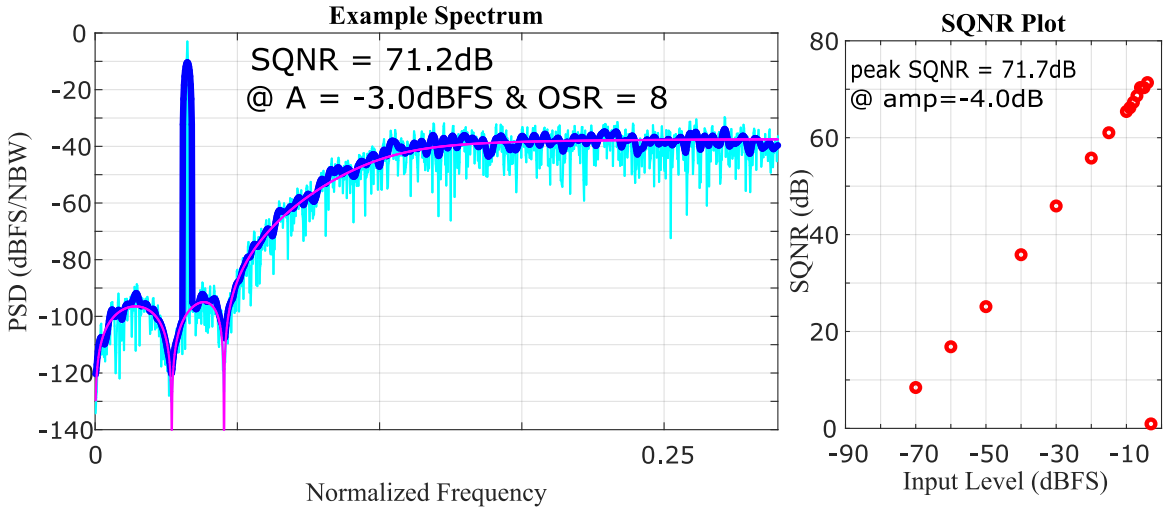

Figure 3.13: An example of the predicted behavior of the system and the values of the SQNR for different amplitude levels.

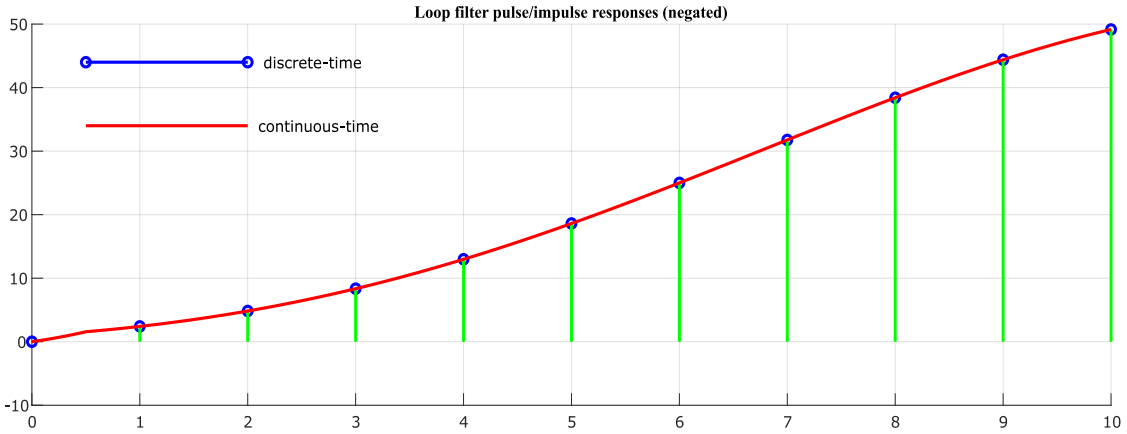

Figure 3.14: The DT equivalent pulse response of the CT loop filter.

c. Interpretation

Since we are proposing an architecture with a multi-bit quantizer and in order to achieve the required SNR, we are employing an aggressive NTF by targeting a high OBG value of 3.7 as shown in the frequency response of the NTF in figure 3.12. Here we can observe that the value of the OBG is around 3.7 (11.36 dB). Such large OBG (larger than the predicted value of 1.5 as predicted by Lee's criterion [5]) usually limits the DR of the modulator by reducing the maximum stable input amplitude (MSA) and it impacts also the stability. But it was shown in [4] that using multi-bit quantizer allows a higher OBG, which leads to aggressive noise-shaping with higher MSA. In our case, we decided to accept a lower MSA value of -3 $dBFS$ while ensuring an SQNR greater than 70 dB.

In order to ensure the stability, the final coefficients are calculated taking into consideration our choice of a CRFF architecture with zero spreading NTF [2]. The optimized zero/poles mapping shown in figure 3.12 is calculated using the optimizer algorithm of the **Schreier's toolbox**. In this figure, we can observe that the STF is flat in the useful band. The presence of the resonance peaks allows to obtain an aggressive NTF behavior. Moreover, the stability is ensured based on the positions of the poles (red circles are all within the unit circle) and the spreading of the zeros (x signs). This spreading reduces the total noise power in the signal band. Moreover, placing the poles nearer to the zeros reduces the out-of-band NTF gain, resulting in improved stability [3, 2, 6].

For CT $\Delta\Sigma$ modulators, the loop-filter is designed using a DT-CT transformation methodology [3, 2]. This implies the existence of an open-loop impulse response of a CT loop equivalent to a DT loop following this equation 3.3:

$$z^{-1}L_d(z) = L^{-1}P(s)L_c(s) \tag{3.3}$$

Where:

- $L_d(z)$ the equivalent DT Open-loop filter impulse response
- $L_c(s)$ the CT open-loop filter impulse response
- $P(s)$ the impulse response of the DAC pulse shape

Figure 3.14 illustrate this equivalence. It means that the DT synthesized modulator used for the simulation will behaves exactly as the CT targeted one. Thus, we can apply directly the results of the modeling phase into the implementation of the CT modulator.

The final step in this phase is the characterization simulation. We inject the calculated coefficients resumed in table 3.2 in the SIMULINK model. For the input, we use a sinwave with a frequency of around 35 MHz and an amplitude of $-3\ dBFS$ (For $FS = 1$, this amplitude is equal to 0.7079). Figure 3.15 shows the results of this simulation:

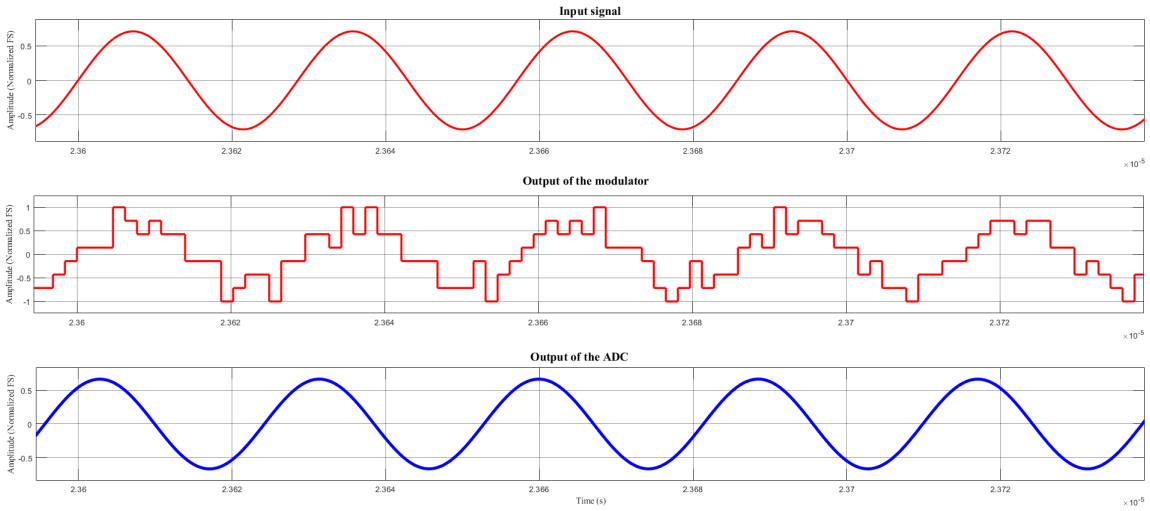

Figure 3.15: Transient response of the synthesized modulator for a sinwave input signal.

This quick check allows us to see that the output of the modulator is a multi-bit stream (we can distinguish 7 steps, which means N=3 bits) and applying this output to a LPF enables the extraction of a higher resolution digital output. To validate the performance of the modulator, we use this low resolution digital output to plot the PSD and estimate the SQNR and the ENOB of the simulated architecture. These values are calculated applying an ideal low pass decimation filter(LPF) at the frequency $f_s/2$, it is represented by the dashed blue line in figure 3.16.

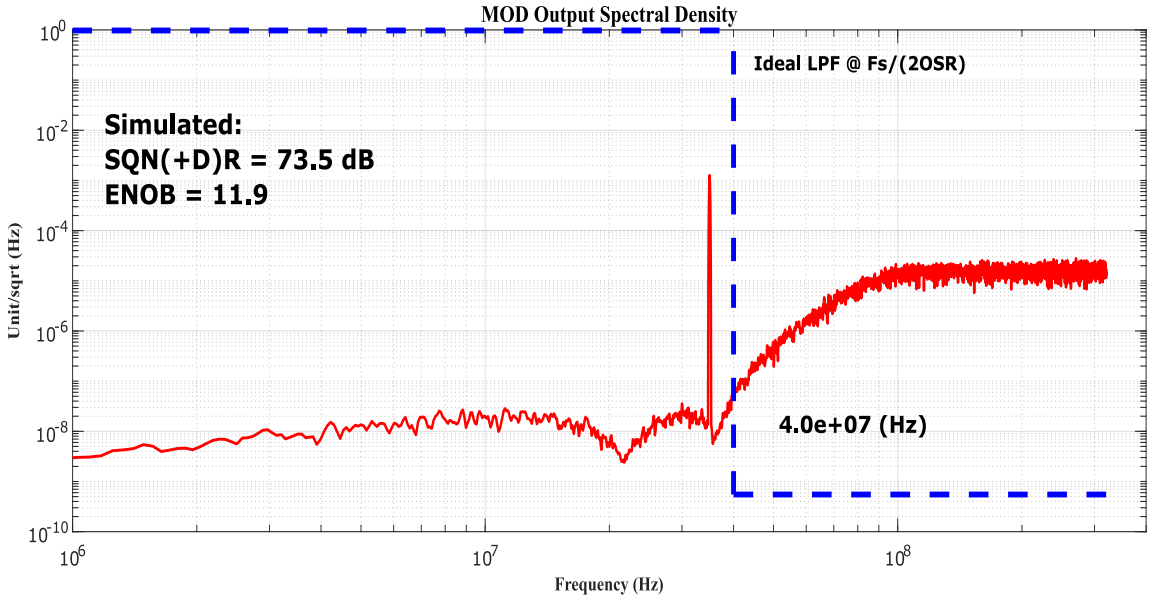

Figure 3.16: PSD of the proposed architecture with a sinewave input.

We observe here the impact of the NTF by shaping the quantization noise outside the useful band. It allows achieving a SQNR of 73.5 dB. These results confirm the predicted values of the

Schreier's toolbox, the slight difference is probably due to the algorithm of the estimation of the PSD. We also want to validate the behavior of the modulator for different amplitude levels. For this, we do multiple simulations using a sinwave with different values of the amplitude and we plot this against the predicted ones. Results are presented in figure 3.17

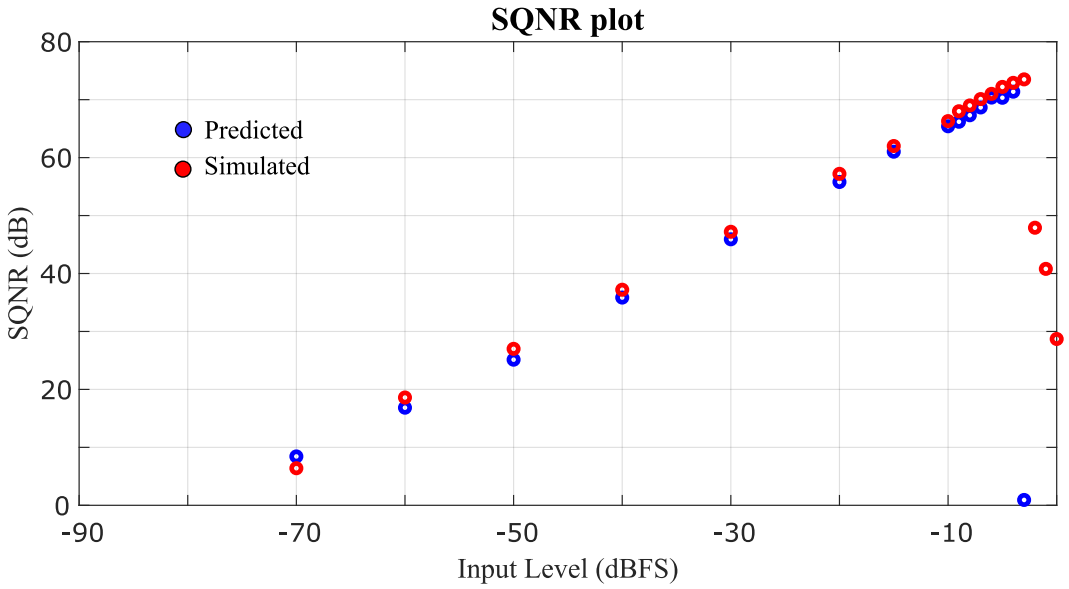

Figure 3.17: The simulated behavior vs the predicted behavior of the modulator for different amplitude levels.

We can clearly conclude that the proposed model is working as predicted by the theoretical analysis and the **Schreier's toolbox**. Thus,it can be used to study and design the targeted modulator.

3.3.2 The script of component dispersion effect

As an application to the feature of our proposed workflow explained above (check figure 3.5) , we propose a Monte-Carlo like simulation model, where we vary independently each parameter following a normal distribution function in a chosen range of error. Using this, we can simulate in this case, the effect of component dispersion (due to fabrication process) and the mismatch of the loop coefficients of the proposed modulator topology. Since we plan to use Opamp-RC integrators to meet the linearity requirement, we need to estimate the time constant shift due to the process variation of R and C values. We will show further the relationship between the coefficients and the RC values (in the subsection 4.2.1).
The variation of the coefficients, are calculated using the estimation represented by equation 3.4:

$$X_i = Xs_i \times (1 + \Delta p_i + \delta m_i) \tag{3.4}$$

Where;

- Xs_i is the synthesized parameter (detailed in table 3.2).

- Δp_i is the PVT error.
- δm_i is the mismatch error.

The simulations are all done using 10,000 iterations and a sinwave input signal with a frequency of 35 MHz and an amplitude of $-4\ dBFS$ (For $FS = 1$, this amplitude is equal to 0.6310). We explore these different combinations:

- $\Delta p_i = 20\%$ and $\delta m_i = 1\%$.
- $\Delta p_i = 20\%$ and $\delta m_i = 0$.
- $\Delta p_i = 0$ and $\delta m_i = 1\%$.
- $\Delta p_i = 5\%$ for critical parameters, $\Delta p_i = 20\%$ for others and $\delta m_i = 1\%$.

a. Algorithm

The algorithm of the script is illustrated below.

Algorithm 2: Monte Carlo like simulation for parameters dispersion

Input:
- a_s, b_s, c_s, g_s // Calculated Coefficients using Schreier's toolbox
- $\Delta p, \delta m$ // Process variation error, Mismatch error
- K // Number of iterations, in our case $K = 10000$

Output:
- a_i, b_i, c_i, g_i // Coeffs adding dispersion
- $SQNR_i$, $ENOB_i$ // Calculated SQNR and ENOB for every added dispersion

Function `GenerateDisp`(a_s, b_s, c_s, g_s, $\Delta p, \delta m$, K)**:**

while $i \leq K$ **do**
- Pick a random value $\Delta p_i \in [-\Delta p, \Delta p]$
- Pick a random value $\delta m_i \in [-\delta m, \delta m]$
- Calculate a_i, b_i, c_i, g_i using equation 3.4
- Increment i

end

return a_i, b_i, c_i, g_i

Procedure `SimulateDisp`(a_i, b_i, c_i, g_i, K)**:**

while $i \leq K$ **do**
- Inject a_i, b_i, c_i, g_i in SIMULINK Model
- Run Simulation using a sinus input with $f_{in} = 40\ MHz$
- Calculate $SQNR_i, ENOB_i$ using the digital output of the model
- Increment i

end

return $SQNR_i, ENOB_i$

b. Results of the script

To illustrate the results of this study, we plot the histogram for each combination and we calculate the standard deviation and the mean of the obtained SQNR values as shown in figure 3.18:

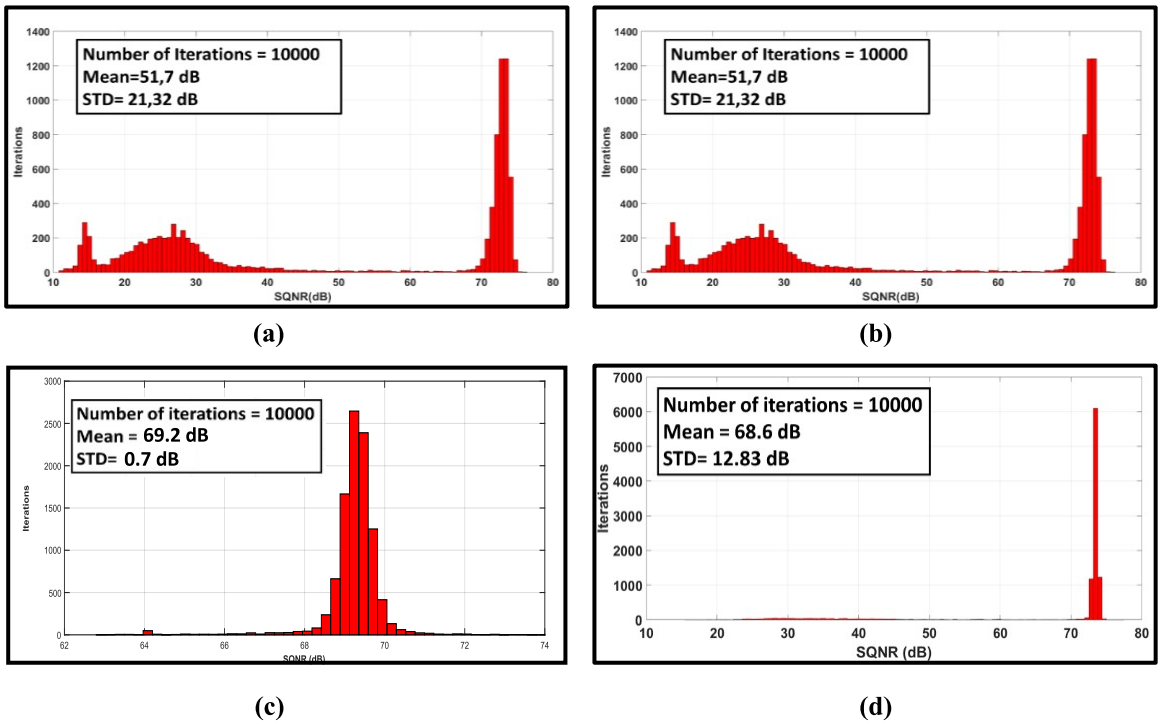

Figure 3.18: Histogram representation of SQNR values for:
(a): 10000 simulations with $\Delta p_i = 20\%$ and $\delta m_i = 1\%$;
(b): 10000 simulations with $\Delta p_i = 20\%$ and $\delta m_i = 0\%$;
(c): 10000 simulations with $\Delta p_i = 0\%$ and $\delta m_i = 1\%$;
(d): 10000 simulations with $\Delta p_i = 10\%$ and $\delta m_i = 0.5\%$ for critical parameters.

We also simulate the impact of this variation en each coefficients individually with $\Delta p_i = 20\%$ and $\delta m_i = 1\%$ in order to find the most critical coefficients. Table 3.3 resume the results of this study.

Table 3.3: SQNR mean and STD for each coefficient simulation.

Parameter	SQNR STD (dB)	SQNR mean (dB)
a1	18.3568	63.7435
a2	23.1711	54.1073
a3	13.4765	68.5378
a4	14.2273	66.5857
a5	3.908	72.8324
b1	21.869	56.2235
b6	4.8299	72.6386
c1	23.3454	58.9705
c2	4.4871	72.0013
c3	20.6108	61.3765
c4	10.339	69.8003

c5	5.4823	71.8419
g1	3.1724	72.8805
g2	3.1459	72.5700

c. Interpretation

We can observe that the modulator is not immune to this level of dispersions (as shown in figure 3.18 (a) which are mainly dominated by the PVT (illustrated by figure 3.18 (b) and (c)). These results lead to many questions.
In order to investigate this, we did a series of simulations to find the most critical parameters. This time, we applied the same dispersions on one parameter a time, and we kept the others as calculated by the **Schreier's toolbox** as explained above. For every simulation, we calculated the standard deviation and the mean of the obtained SQNR as a picture of the degree of impact of the dispersions. This study is summarized in table 3.3.
Based on these results, we can directly conclude that, for the coefficients a_1, a_2, b_1, c_1, which are the most critical (we can see a huge drop of SQNR with a high standard deviation of around 30% of the desired SQNR for these coefficients) this level of dispersions is problematic and it needs to be reduced. We assume that the main reason of this drop of SQNR is the saturation of integrators. Figure 3.19 shows the values of the maximum output swing of the first integrator plotted with the values of SQNR as a result of the dispersions applied on parameter a_1 for 100 simulations. The value of 450 mV is chosen to represent the maximum achievable swing.

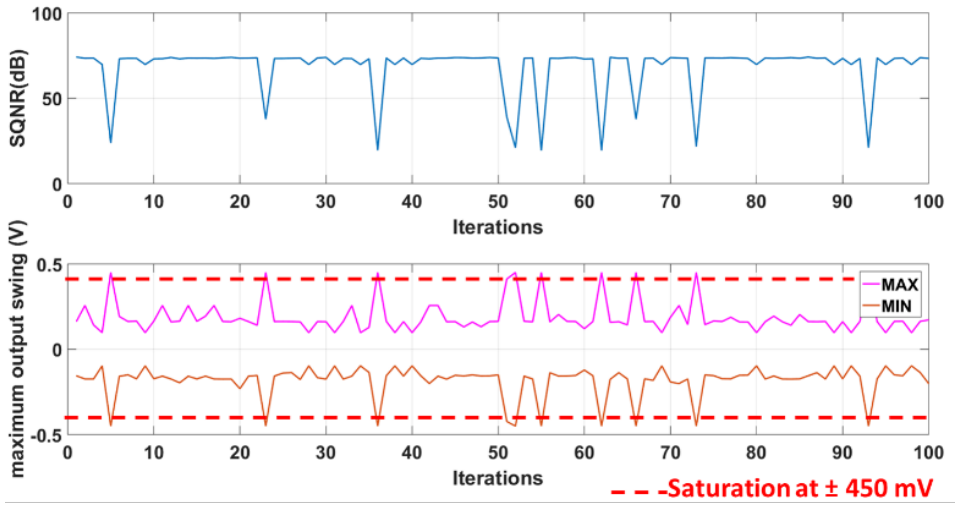

Figure 3.19: Maximum output swing of the first integrator Vs SQNR for a dispersion of $\Delta p = 20\%$, $\delta m = 1\%$ of the coefficient a_1.

To validate this hypothesis, we reduced the range of error to $\Delta p = 10\%$, $\delta m = 0.5\%$ for these critical parameters. Results of this simulation are presented in figure 3.18 (d). It is important to note also, that the most critical coefficients are the ones related to the input stage (mainly the first integrator) which needs to be carefully designed.
We conclude that in order to guarantee the desired specifications, these parameters must be correctly designed within a range of error as low as possible (we are targeting $< 10\%$).

3.3.3 The script of the amplifiers DC gain optimization

Another possibility to benefit from the proposed workflow, is to use it for optimizing the performances of our topology. Here, we focus on the DC gain of the amplifiers used in every integrator stage. By lowering the DC gain of some amplifiers and finding a suitable combination, we ensure the ENOB while gaining in terms of power consumption and complexity of the design. In the proposed case, values of the DC gain of stage 2 to 5 are varied between 85 to 5 with a step of 20. For stage 1 the gain is kept at 100 [7].

a. Algorithm

Algorithm 3: The optimization of the amplifiers DC gain

Input:
- G_0 // Initial value of the gain,in our case $G_0 = 105$
- ΔG // Gain step, in our case $G = 20$
- K // Number of iterations, in our case $K = 5$

Output:
- $SQNR_{(i,j,l,m,n)}, ENOB_{(i,j,l,m,n)}$ // Calculated SQNR and ENOB for every combination

Function `GenerateComb(`G_0, ΔG, K`)`**:**
- **while** $i \leq K$ **do**
  - Fix the DC gain of the first stage $G_1 = 100$
  - Increment i
  - **while** $j \leq K$ **do**
    - Calculate the DC gain of the second stage $G_2(j) = G_0 - \Delta G \times K$
    - Increment j
    - **while** $l \leq K$ **do**
      - Calculate the DC gain of the third stage $G_3(l) = G_0 - \Delta G \times K$
      - Increment l
      - **while** $m \leq K$ **do**
        - Calculate the DC gain of the forth stage $G_4(m) = G_0 - \Delta G \times K$
        - Increment m
        - **while** $n \leq K$ **do**
          - Calculate the DC gain of the fifth stage $G_5(n) = G_0 - \Delta G \times K$
          - Increment n
        - **end**
      - **end**
    - **end**
  - **end**
- **end**
- **return** G_1, G_2, G_3, G_4, G_5

Procedure `SimulateComb(`G_1, G_2, G_3, G_4, G_5, K`)`**:**
- **while** $i, j, l, m, n \leq K$ **do**
  - Inject G_1, G_2, G_3, G_4, G_5 in SIMULINK Model
  - Run Simulation using a sinus input with $f_{in} = 40\,MHz$
  - Calculate $SQNR_{(i,j,l,m,n)}, ENOB_{(i,j,l,m,n)}$ using the digital output of the model
  - Increment i, j, l, m, n
- **end**
- **return** $SQNR_{(i,j,l,m,n)}, ENOB_{(i,j,l,m,n)}$

b. Results of the script

We obtain for the proposed case a 5-dimensional matrix with 3125 values. We Firstly extract the combination that guarantees the highest ENOB. For that, we use a simple algorithm and we obtain these DC gain values summarized in table 3.4.

Table 3.4: Optimized DC gain values of each integrator.

Stage	DC gain values
Integrator 1	100
Integrator 2	25
Integrator 3	85
Integrator 4	65
Integrator 5	65

We injected these values in the synthesized model and run a functional simulation. Figure 3.20 shows the obtained result.

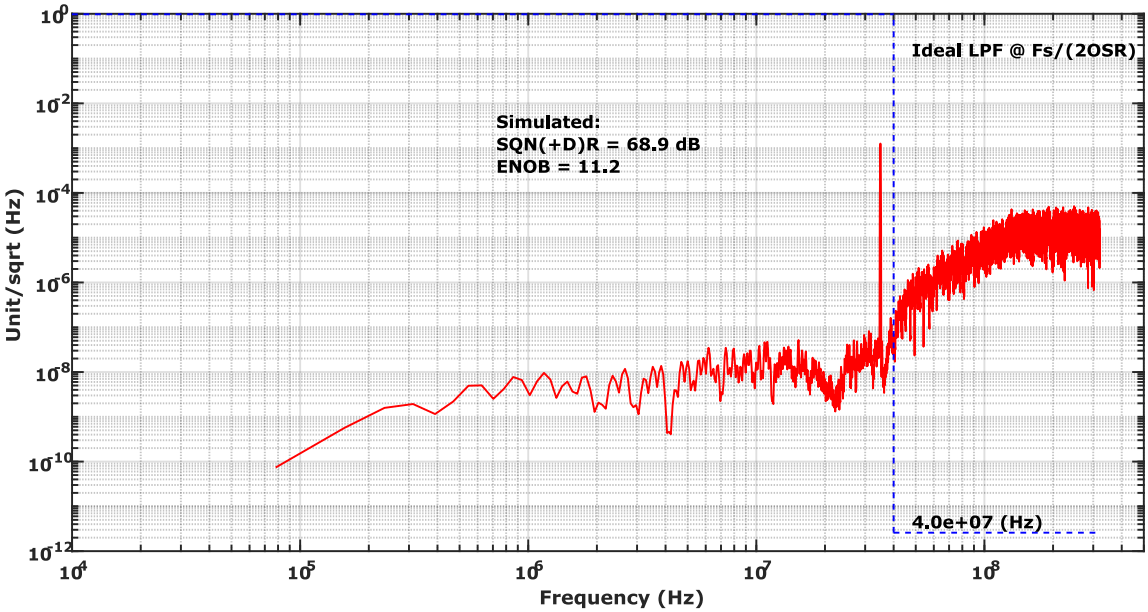

Figure 3.20: PSD of the modulator using the obtained DC gains.

In a second time, we plot the values of the ENOB for all the generated combinations. Figure 3.21 illustrates the obtained results.

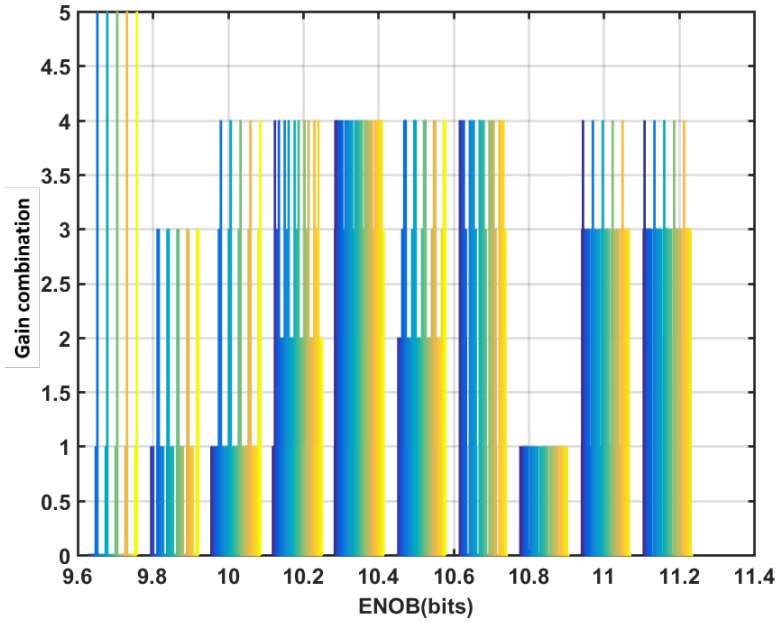

Figure 3.21: Histogram of the ENOB values for all the combinations.

c. Interpretation

We directly notice a drop of the ENOB as shown in figure 3.21 (for all the combinations, the obtained ENOB is smaller than the maximum achievable one at the MSI, see figure 3.16). Yet, taking the best case (figure 3.20) where we sacrifice around 5% of the maximum achievable ENOB, represents an interesting compromise in terms of optimizing the power conception (we expect a drop of more than 30%) and design complexity. It should be noted that these results are preliminary and should be investigated in depth for clearer explanations. Unfortunately, it is not the case here, due to time constraints, we decide to use the same amplifier to build all the integrators as detailed in the section 4.2. We believe that these results represent an important avenue for future improvements of our proposed topology.

3.3.4 Simulation of the ADC/DAC non-idealities

Another way to make use of the potential of the proposed methodology, is to employ it to estimate the impact of non-idealities of the loop ADC and the feedback DAC. This helps to define a tolerance range for these errors in the phase of physical implementation. The algorithm we used for this is similar to algorithm 2. Instead of changing the values of the coefficients, we use it to change the parameters of the 3 *bits* loop ADC and the 3 *bits* feedback DAC models. In the case of the ADC, since we plan to use a FLASH topology, the major imperfection comes from the offset of the comparators and the precision of the voltage references (resistors mismatch in the resistor ladder). We model this error through the following equation:

$$\Delta_V = \sqrt{V_{offset}^2 + \Delta_{V_r}^2} \tag{3.5}$$

Where:

- Δ_V is the total error;
- V_{offset} is the value of the offset of the comparator;
- Δ_{V_r} is the value of the error on the voltage reference (resistor ladder).

This value is generated using the same method in algorithm 2. We extract in each case the value of the ENOB and we calculate the loss comparing to the ideal case based on the mean value of the error. We also estimate the DNL for a reasonable chosen value: 3 mV.

For the DAC, we decide to use a current steering topology. The main issue of this choice is the error introduced from the mismatch of the current mirrors. This error is introduced in the same way explained above (algorithm 2) at the output of the DAC and its impact is analyzed through the estimation of its DNL and we compare it to the loss in the ENOB value.

a. Results of simulations

Figure 3.22 illustrates the results of the loss of the ENOB for different values of the error of the ADC.

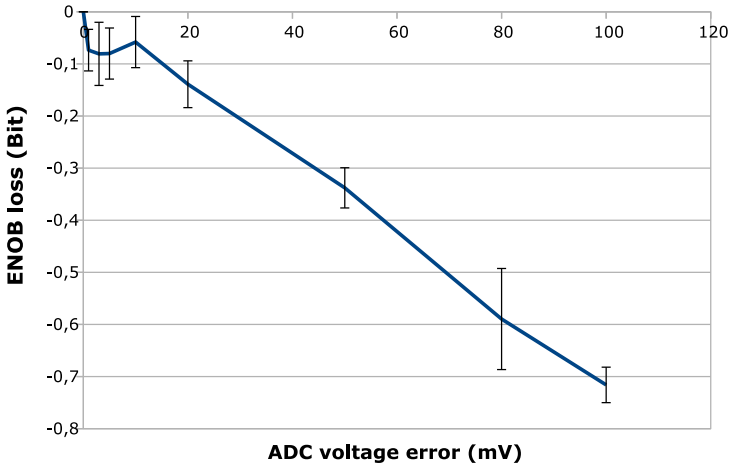

Figure 3.22: The loss in ENOB for different values of the ADC voltage error.

The results of the calculation of the DNL for a 3 mV error is shown below in figure 3.23. From this figure we can notice, that the DNL is limited to 0,06 LSB.

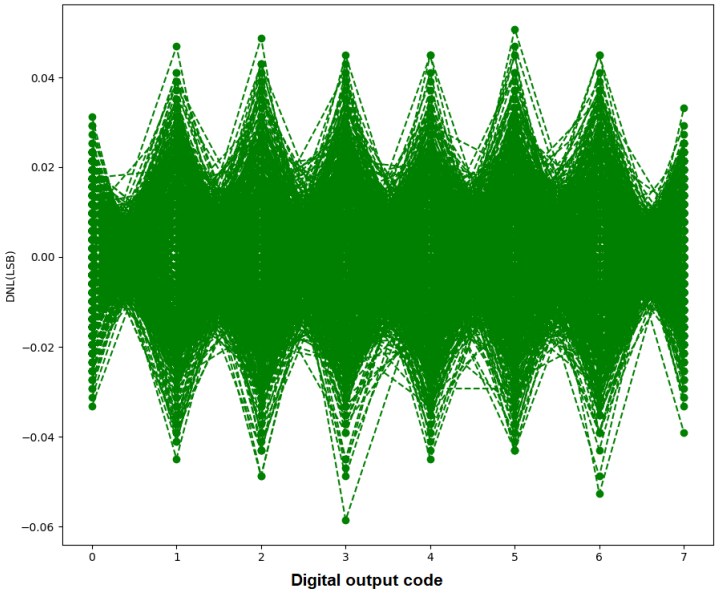

Figure 3.23: Extracted DNL values for a 3 mV ADC voltage error.

For the DAC, the loss of the ENOB is plotted as a function of its DNL as shown in figure 3.24.

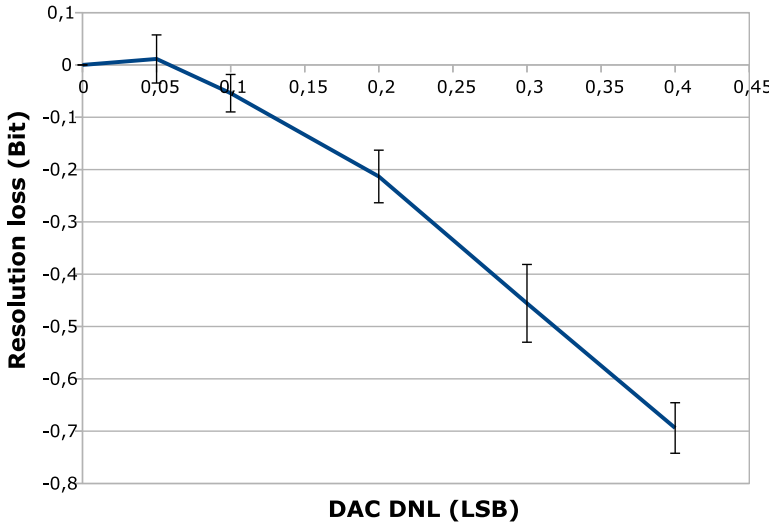

Figure 3.24: The loss of the ENOB as a function of DAC DNL.

b. Interpretation

First of all, this results constitute a good guideline to define the specifications of this two blocks and to validate the choice of both topologies. They also showcase that we have low constraints on the design of these blocks and we can tolerate an acceptable range of imperfections.

3.3.5 Simulation of the Excess Loop Delay (ELD)

One of the most critical issues for CT ΔΣ ADC topologies is known as the excess loop delay. It is identified as the delay between the loop quantizer clock edge and the change of the DAC output at the feedback point in the modulator. It is originally caused by the non-zero switching time of the transistors in the feedback path (Latches of the comparators and the transistors of the DAC). It was shown in [8] that this delay affects the equivalence between the CT and the DT representations of the loop and thus its performance (in-band noise, MSA, and DR). Authors explained also that high order LP designs seem more robust when it is designed using NTF prototyping because the value of the OBG is a parameter to be selected and it gives some immunity to the ELD.

Due to all this, it is necessary to analyze the behavior of our proposed structure in order to define the range of the ELD and thus design correctly the feedback path. To do that, we have to use a fully CT model. The DT integrators based on the ***Delay*** Z^{-1} blocks are replaced by the ***Transfer Fcn*** block which allows modeling a transfer function using the Laplace-domain variable ***s***.

Since ideally the DAC responds immediately to the quantizer clock edge which is the case of our model, we use a ***Transport Delay*** block to introduce the ELD in the feedback path.

a. Results of simulations

This simulation is done for 3 different OBG values. In each case, the ENOB is extracted as a function of the value of the ELD. Figure 3.25 illustrates the results:

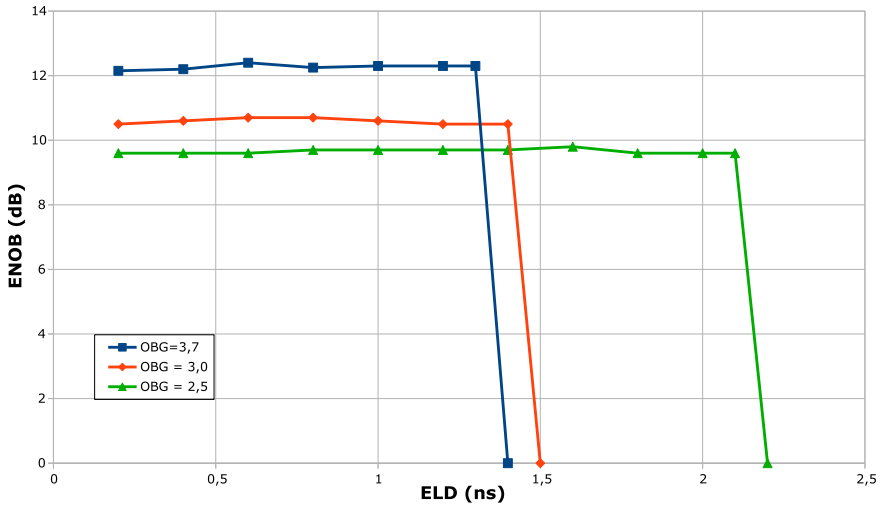

Figure 3.25: Response of the modulator for different values of the ELD using different values of the OBG.

b. Interpretation

These results are in accordance with the data published in [8]:

- we see clearly that the ELD affects the response of the modulator;
- when the ENOB equals zero, this means that it is unstable;
- we can tolerate more ELD using a lower value of the OBG by sacrificing the resolution (Lower ENOB value).

These results helps defining the speed requirements for the feedback path to ensure the proper operation of the modulator which is quite challenging.

3.4 Summary

In this chapter, we discussed a systematic high-level design approach based on the model-based design paradigm of our proposed architecture of the modulator. We explained the choice of the topology and we detailed the application our workflow enabling a full integration of the **Schreier's toolbox**. Moreover, we showed the synthesizing phase and its results and we discussed an application of the proposed workflow to analyse the effect of the dispersion of the loop coefficients. In addition to that, we showed the possibility to use the proposed workflow for the optimization of the parameters of the topology and we analyzed the case of the DC gain amplifiers for more energy efficiency. We also explained the use of this workflow to study other non-idealities of the other blocks, we extracted the specifications of the feedback path in terms of the voltage error of the ADC, the DNL of the DAC and the ELD. The next chapter will explain the use of all these extracted data for the sizing of transistors using g_m/I_d design methodology.

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4

Circuit-Level Implementation

This chapter deals with the implementation of each part of the modulator and the results of different simulations to validate it.

Contents

Important note

In this chapter, we decide to reduce the BW of the proposed modulator (first prototype) to 10 MHz which means a sampling franquency of 160 MHz (OSR=8). This is because we are not planing to integrate the decimation filter on the same chip for this first prototype. Thus, we cannot guarantee to extracted the data at a rate of 640 MHz to an external decimation filter (FPGA). In this chapter we explain that the results of chapter 3 are valid and the generated coefficients are the same.

4.1 g_m/I_d design methodology for sizing transistors

In this section, we detail the use of the g_m/I_d design methodology via precomputed Lookup Tables (LUTs) for the sizing of transistors used in different blocks of our proposed circuit.

4.1.1 Why the g_m/I_d design methodology?

Classically, the square-law model for CMOS transistors is the "text book". It has been used extensively to analyze and design analog and digital integrated circuits thanks to its simplicity yet its usefulness [1]. But this model suffers from a lot of limitations specially when it comes to short-channel transistors [1, 2]. Figure 4.1 illustrates these limitations. It shows the current density plot of a realistic sub-micron transistor, together with exponential and square-law approximations.

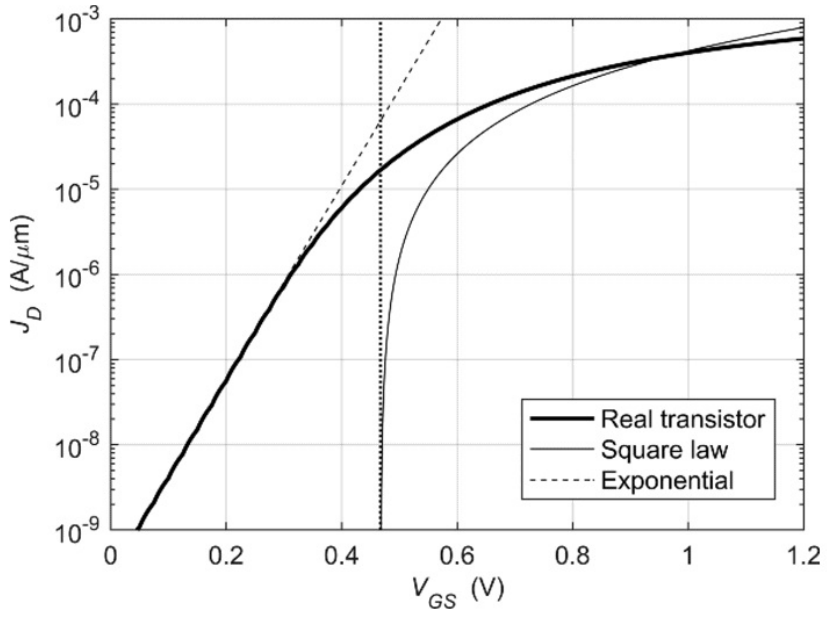

Figure 4.1: Current density of a minimum-length n-channel device in 65-nm CMOS technology versus V_{GS}. The dotted vertical line corresponds to the device's threshold voltage, extracted from [1].

Here, we can see that the square law does not match the response of a real transistor: it is not accurate for very large V_{GS} values (strong inversion), and completely invalid for both low V_{GS}

values (weak inversion) and moderate V_{GS} values (moderate inversion). This means that the obtained results of the hand analysis using the square law and the ones of the simulations using more complex device models [3] are totally different. Therefore, this situation leads designers to using a design workflow based on "tweakling" through iterative time-consuming SPICE simulators [1].

Switching to a g_m/I_d-based design methodology [4] allows to captures the relation between the fundamental function of the transistor (because fundamentally, a transistor is a voltage controlled current source), which is its transconductance g_m and its power consumption I_d. Thus, the g_m/I_d ratio represents in a systematic way the following equation [5]:

$$Transistor_{efficiency} = \frac{The\ wanted\ specifications}{The\ paid\ consumption} = \frac{g_m}{I_d} \tag{4.1}$$

It was shown in [1] that the g_m/I_d ratio is directly related to the most important analog specifications: speed, noise, efficiency, gain, swing and mismatch. Moreover, the range of values of g_m/I_d is very limited, typically between 0 to 30. We illustrate its values after we extracted the LUTs of the used technology (130 nm CMOS technology)in figure 4.2. Also, it is important to know that this does not differs much from a device to another and from a technology to another [5].

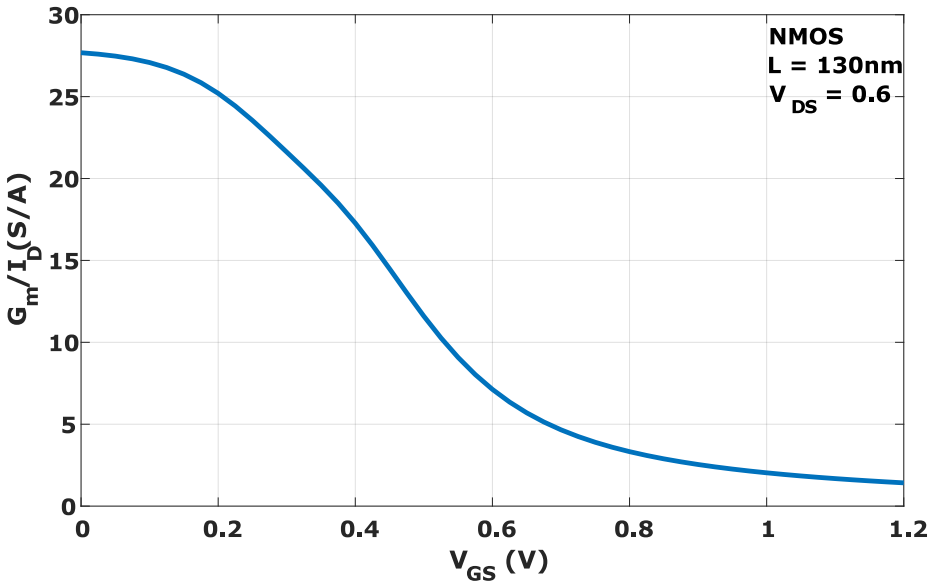

Figure 4.2: The extracted g_m/I_d values for different values of V_{GS} of our used 130nm CMOS technology.

Technically, the use of this design methodology is generically described in the following steps [1]:

Step 1: calculating the value of g_m from the design specifications.

Step 2: choosing the value of L:

- for high speed and small area, L should be **short**;
- for high intrinsic gain and better matching, L should be **long**.

Step 3: choosing a value of the g_m/I_d:

- for low power and large signal swing, g_m/I_d should be **large** (weak inversion);

- for high speed and small area, g_m/I_d should be **small** (strong inversion).

Step 4: Calculating the value of I_D using the obtained g_m and g_m/I_d.

Step 5: Extracting the value of W using the ratio I_D/W.

These steps can be applied directly in the case of a simple topology where calculating g_m is possible. In the opposite case, one can apply these steps for different values of g_m/I_d (different levels of inversion) and then analyze the results to find the suitable spots. More details about the application of these steps will be shown below in the sizing of the amplifier used for building the integrators.

4.1.2 Implementation of g_m/I_d design methodology via Precomputed LUTs in the design flow

In the subsection 3.2.1, we showed in figure 3.4 the integration of the procedure of g_m/I_d design methodology in the proposed workflow. This integration can be done either using an analytic method using model equations (typically EKV model [6]) such as the inversion coefficient (IC) based flows proposed by Binkley [7], Enz [8], and Sansen [9] and also the 2010 g_m/I_d-centric book by Jespers [10], or using of numerical method based on SPICE generated lookup table data. We decide to work with the second option because it more simple to integrate in the proposed flow while giving the closest response to real devices [1, 11].
The main idea in this approach, is to abstract the complex device models of modern devices in the form of LUTs. These LUTs are generated by the simulator for a set of reference devices once per technology. The designer can then use these LUTs to author systematic design plans for a circuit without invoking the simulator (through a systematic design approach), while achieving simulator-accurate results. Those tables store the device characteristics across its different degrees of freedom (DOFs). They can be generated for any type of devices and for different technologies. Here, we focus on a commercial 130nm 1P8M technology, which transistors are approached as a four-terminal device. Thus, its characteristics are controlled by three independent voltage differences: V_{GS}, V_{DS}, and V_{SB}. It depends on its sizing as well: the channel width (W) and the channel length (L). From this, its drain current (I_D), which is the primary dependent variable, can be written as a function of five independent variables (five DOFs):

$$I_D = f(W, L, V_{GS}, V_{DS}, V_{BS}) \tag{4.2}$$

For MOSFET, its characteristics are proportional to W for every operating region, which means we can reduce the DOFs to four and calculate the desired W using cross multiplication [11]. From this, we can generate the precomputed LUTs using a circuit simulator through a sweep for a reference device (a device with a reference W) and store any desired parameter such as: I_D, g_m, g_{DS}, C_{GG}, etc.

At this point, we can simply replace W with g_m/I_D (this is commonly called the g_m/I_D design methodology) to make a new set of DOFs (g_m/I_D, L,I_D) enabling us to [11]:

- determine the inversion level of the device using only the g_m/I_D ratio.
- find the suitable W from LUTs while keeping a constant g_m/I_D ratio which means the bias point is unchanged.
- accelerate the sizing phase, because the search range of g_m/I_D is limited and smaller compared to the range of W.

To summarize our proposed methodology, the designer will firstly choose a circuit topology that is expected to meet the requirements. To verify feasibility of this implementation and find the

best set of parameters, he will use the model-base design approach and build an interactive system level model. Finally, he will use the set of parameters extracted from the modeling phase (which ensures the targeted specifications) to decide the biasing and sizing values of every transistor of the chosen topology using the precomputed LUTs design methodology [1, 11].

4.1.3 Amplifier topology

Since we are working with opamp-RC integrators, it was shown in [12] that the Loop Unity Gain Frequency (UGF) of the first opamp and its DC gain affects the quantization noise floor below the BW of the modulator and its noise shaping performance. Moreover, [12] illustrates as well that a DC gain of 40 dB impacts negligibly these specifications (this is coherent with our systematic results obtained in the subsection 3.3.3). Concerning the UGF, it is true that in the case of a CT modulator, the integrators have a full clock period for settling which results in a GBW requirement that could be as low as the sampling frequency value f_s [13], yet we usually need to maximize its value beyond that (6 to 10 times f_s) in order to minimize the time constant error of the integrator (This is detailed in the subsection 4.2.1).

Thus, for a typical single-pole operational amplifier this means a UGF product over few GHz while ensuring that its parasitic poles must be above this frequency to provide stability (Phase marging $> 90°$). These requirements cannot be achieved using a single stage amplifier because the amplifiers are resistively loaded [14]. Therefore, we adopt a multistage architecture with a feedforward compensation. More precisely, a topology called "***two-stage opamp based on a feedforward compensation scheme with no Miller capacitor (No-Capacitor Feedforward (NCFF) compensation scheme)***", it was introduced and detailed in [15]. Figure 4.3 illustrates a block diagram of a single ended two stages NCFF opamp.

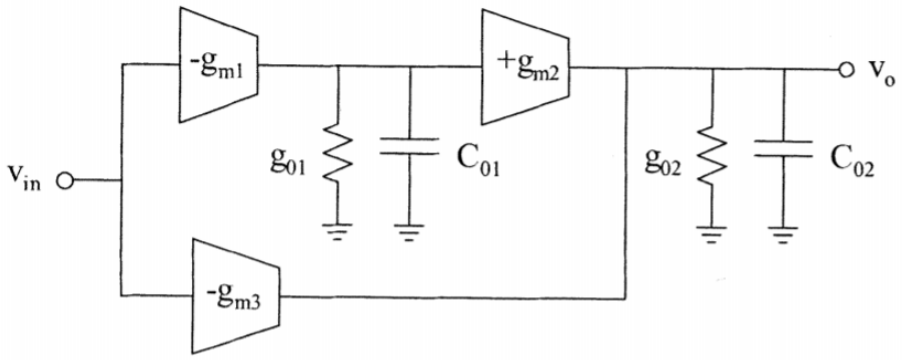

Figure 4.3: Block diagram of a single ended two stages NCFF opamp, extracted from [15].

In this topology we use the positive phase shift of a left-half-plane (LHP) zero created by the feedforward path without using any Miller capacity to improve the phase response enabling a high gain and high frequency requirements while ensuring good stability (High phase margin).

In order to be as close as possible to a perfect pole-zero cancellation case, we use the proposed model-based design methodology: this topology is modeled in SIMULINK using the standard transfer function "***Transfer Fcn***" blocks following the simplified diagram of figure 4.4.

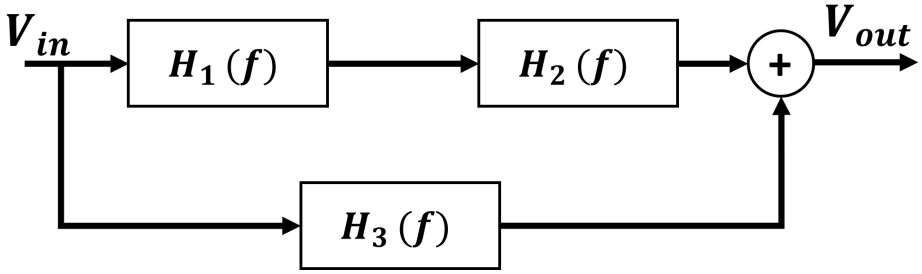

Figure 4.4: A simplified diagram of the SIMULINK model of the proposed opamp.

The required specifications of this topology for our application are summarized in table 4.1.

Table 4.1: Desired specifications of the proposed opamp.

Parameter	**Value**
Technology	130 nm
Bias current	Minimize
Consumption	$< 5\ mW$
DC gain	$> 35\ dB$
Load capacitance	100 fF
Loop Unity gain Frequency (UGF)	$> 5\ GHz$
Phase Margin	$> 90°$

Each block represent the transfer function of a differential amplifier, which can be mathematically described as a first order system with two key parameters: its DC gain (A_i) and its cutoff frequency (f_i) as shown in equation 4.3:

$$H_i(f) = \frac{A_i}{\frac{1}{2\times\pi\times f_i}\times p + 1} \tag{4.3}$$

It should be noted that H_2 and H_3 has the same cutoff frequency (f_i) because they share the same load.

Through this simplification, the total transfer function of the model of the opamp is represented by equation 4.4:

$$H_{total}(f) = \frac{A_1 \times A_2 + A_3 \times (1 + \frac{1}{\omega_1} \times p)}{(1 + \frac{1}{\omega_1} \times p)(1 + \frac{1}{\omega_2} \times p)} \tag{4.4}$$

By applying the model-based design paradigm to guarantee that we achieve the requirements (table 4.1) in terms of DC gain, UGF and Margin Phase, we made a MATLAB scripts to sweep the values of A_1, A_2, A_3, f_1 and f_2. Among the possible solutions, we chose the following values presented in table 4.2

Table 4.2: Extracted parameters from SIMULINK model.

Parameter	Value
A_1	16
A_2	5
A_3	12
f_1	62.5 MHz
f_2	167 MHz

The frequency response of the proposed topology with the chosen parameters is illustrated in figure 4.5:

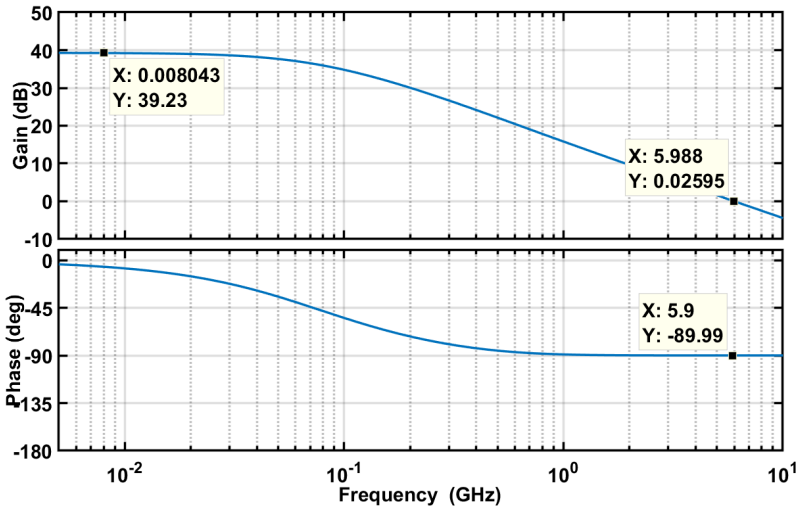

Figure 4.5: The frequency response of the SIMULINK model using model-based design.

We can see that the requirements are fulfilled using this configuration. A DC gain of 39.23 dB is achieved with a cutoff frequency of 6 GHz and a phase margin of 90°.

4.1.4 Example of amplifier sizing

The precomputed LUTS for the 130 nm 1P8M CMOS technology are already extracted and organized as explained above. A simplified schematic of the proposed opamp is shown in figure 4.6.

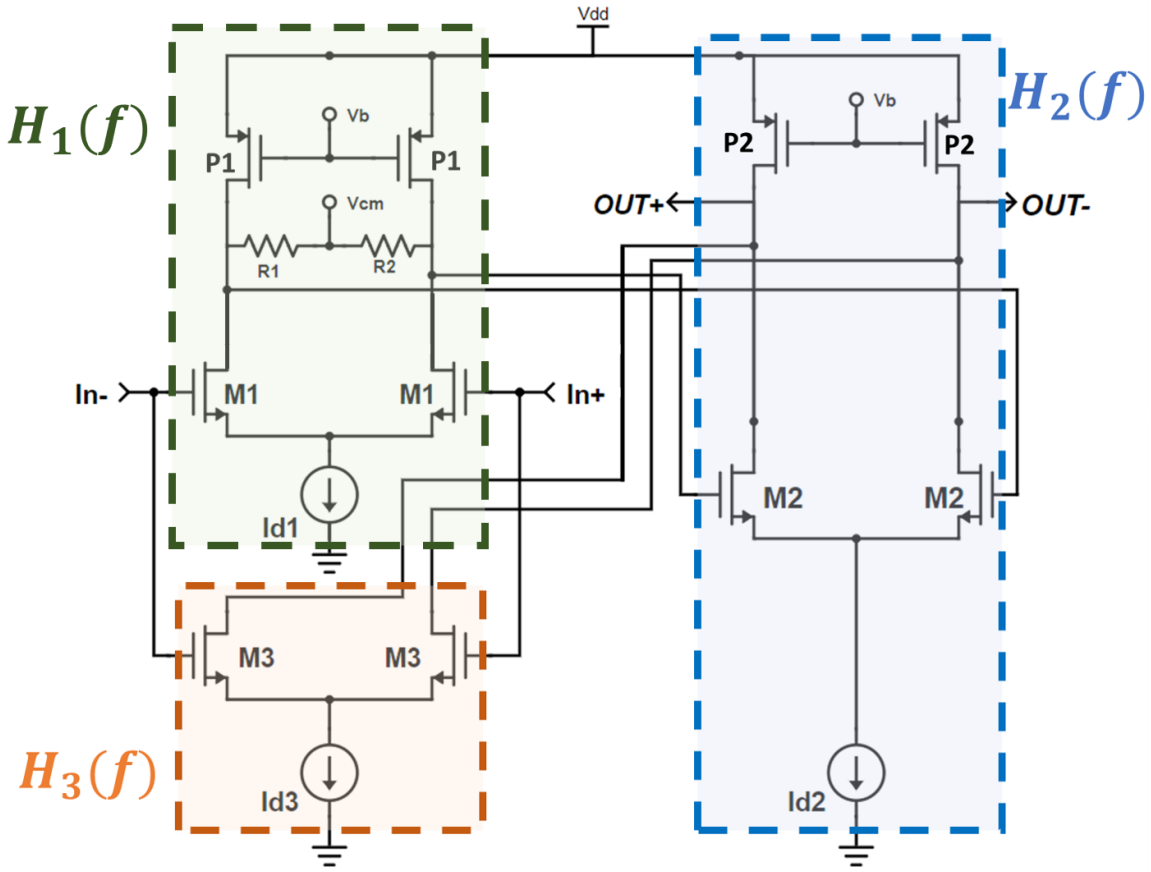

Figure 4.6: Simplified schematic of the proposed two-stages NCFF opamp.

Using the SIMULINK model and the small signal analysis, we can describe each stage using the following equations:

$$A_1 = \frac{gm_{M1}}{gds_{M1} + gds_{P1}} \tag{4.5}$$

$$A_2 = \frac{gm_{M2}}{gds_{M2} + gds_{P2} + gds_{M3}} \tag{4.6}$$

$$A_3 = \frac{gm_{M3}}{gds_{M2} + gds_{P2} + gds_{M3}} \tag{4.7}$$

$$\omega_1 = \frac{gds_{M1} + gds_{P1}}{CDD_{M1} + CDD_{P1} + CGG_{M2}} \tag{4.8}$$

$$\omega_2 = \frac{gds_{P1} + gds_{P2} + gds_{M3}}{CDD_{M3} + CDD_{M2} + CDD_{P2} + C_L} \tag{4.9}$$

With C_L the load capacitance at the output node.

By solving this set of equations with the obtained values of the modeling phase resumed in table 4.2, we can size each transistor using the precomputed LUTs. The example of sizing the first stage is shown in the following algorithm: (M_0 is the bias transistor represented as the current source Id_1 in figure 4.6).

Algorithm 4: Example of sizing the first stage using g_m/I_d design methodology via Precomputed LUTs

Input:

UGF_1, C_L // Selected from table 4.2 for the first stage

$g_m/I_{dM0}, g_m/I_{dM1}, g_m/I_{dP1}, V_{DSM0}, V_{DSM1}, V_{DSP1}$ // Chosen by the designer, initially we choose moderate inversion then we tune it for better results

L_{M0}, L_{M1}, L_{P1} // Chosen by the designer and can be tuned via LUTs

Output:

W_{M0}, W_{M1}, W_{P1}

A_{1calc}, UGF_{1calc} // Obtained DC gain and UGF after sizing

Function `SizeTrans`$(UGF_1, C_L, g_m/I_{dM0}, g_m/I_{dM1}, g_m/I_{dP1}, L_{M0}, L_{M1}, L_{P1})$**:**

- Extract gds_{M1} from LUTs using g_m/I_{dM1}, L_{M1} and V_{DSM1}
- Extract gds_{P1} from LUTs using g_m/I_{dP1},L_{P1} and V_{DSP1}
- Extract Id/W_{M0} from LUTs using g_m/I_{dM0},L_{M0} and V_{DSM0}
- Extract Id/W_{M1} from LUTs using g_m/I_{dM1},L_{M1} and V_{DSM1}
- Extract Id/W_{P1} from LUTs using g_m/I_{dP1},L_{P1} and V_{DSP1}
- Extract CDD/W_{M1} from LUTs using g_m/I_{dM1},L_{M1} and V_{DSM1}
- Extract CDD/W_{P1} from LUTs using g_m/I_{dP1},L_{P1} and V_{DSP1}
- Calculate gm_{M1} using C_L and UGF_1
- Calculate I_{dM1} using gm_{M1} and g_m/I_{dM1}
- Calculate W_{M0} using $2 \times I_{dM1}$ and Id/W_{M0}
- Calculate W_{M1} using I_{dM1} and Id/W_{M1}
- Calculate W_{P1} using I_{dM1} and Id/W_{P1}
- Calculate CDD_{M1} using W_{M1} and CDD/W_{M1}
- Calculate CDD_{P1} using W_{P1} and CDD/W_{P1}
- Calculate A_{1calc} using equation 4.5
- Calculate UGF_{1calc} using equation 4.8 // The value of CGG_{M2} is obtained after sizing the transistor M_2 using the same algorithm
- **return** $W_{M0}, W_{M1}, W_{P1}, A_{1calc}, UGF_{1calc}$

We use algorithm 4 implemented as a script in MATLAB to size the transistors of the three stages, the results of this operation are presented in table 4.3.

Table 4.3: The sizing of transistors of the proposed topology.

Transistor	W (μm)	L (nm)	g_m/I_d
M_1	31.8	250	23
M_2	180.3	150	20.5
M_3	84.3	150	16
P_1	11.22	500	10
P_2	78.8	150	7.5

Results of the AC electrical simulation of the opamp after the sizing for a load of $C_L = 1\ pF$ are illustrated in figure 4.7 (The thick dark line represents the gain plot and the dashed line represents the phase plot). We obtain a DC gain of 39.25 dB with a UGF of 5.56 GHz and a phase margin of 102°.

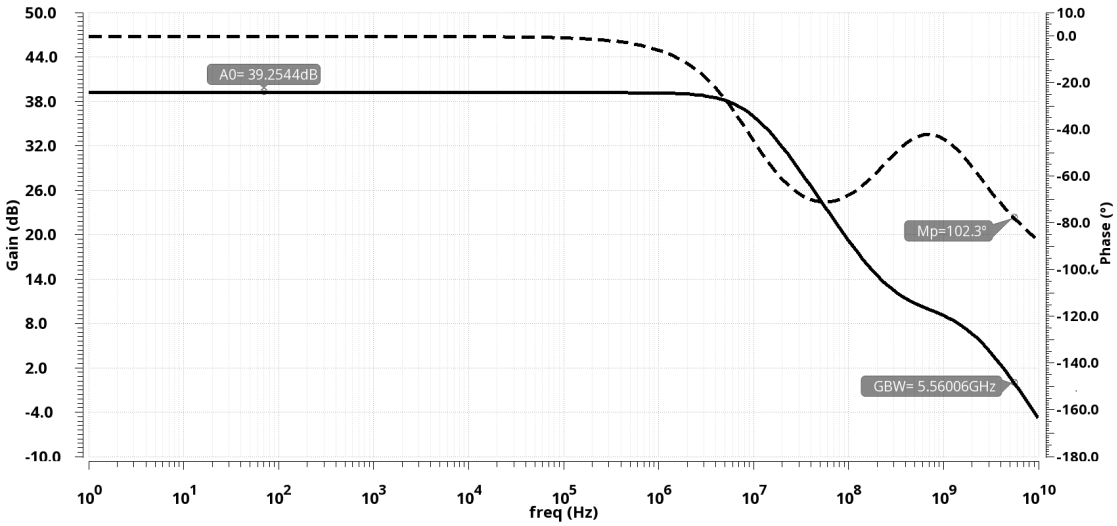

Figure 4.7: The frequency response of the proposed opamp.

A comparison between the required specifications and the obtained one from the electrical simulations are resumed in table 4.4.

Table 4.4: Design specifications of the proposed opamp.

Parameter	**Required**	**Modeling**	**Achieved**
Bias current	Minimize	-	3.66 mA
Consumption	$< 5\ mW$	-	4.4 mW
DC gain	$> 35\ dB$	39.23 dB	39.26 dB
Loop Unity gain Frequency (UGF)	$> 5\ GHz$	5.98 GHz	5.56 GHz
Phase Margin	$> 90°$	89.99°	102°

We can see that the results of this simulation are close to the modeling results (shown in figure 4.5 and the targeted specifications are achieved.

4.2 Loop filter

The loop filter of our modulator is composed of a first integrator stage followed by two resonator stages as shown in figure 4.8. All the integrators are built using RC-opamp structure instead of using gm-C cells or active gm-C cells to ensure high linearity performance, high dynamic range and better robustness for PVT and mismatch variations [16, 12]. More advantages of this choice will be shown further while explaining the implementation of the feedback DAC. In this section, we explain the circuit level implementation of the coefficients calculated in the section 3.3 for the three stages of the loop filter. Moreover we discuss the obtained performances of each stage using the results of the electrical simulations.

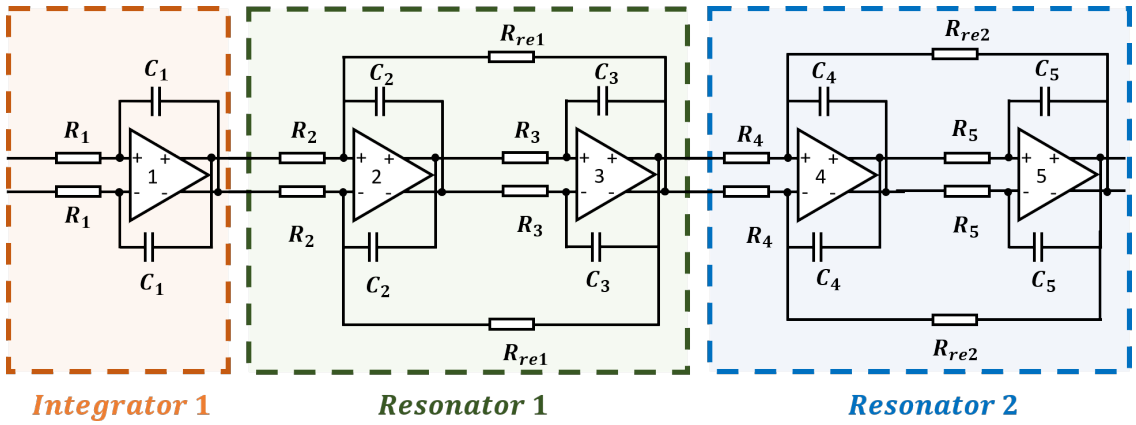

Figure 4.8: Circuit level structure of the loop filter.

4.2.1 Integrators sizing

We focus here on the design of the first stage integrator using the opamp detailed above in the subsection 4.1.4. Since we are using an RC-opamp structure, we need to find the suitable values of both R and C that guarantee an equivalent response to the modeling DT one. One more advantage of using the model-design approach through SIMULINK is to be able to extract individually the response of each stage. Before that, we show firstly the equivalence between the response of a DT integrator and a CT integrator as illustrated in figure 4.9 (the DT integrator is the same detailed in the subsection 3.2.3, we can observe the effect of the finite DC gain of the opamp).

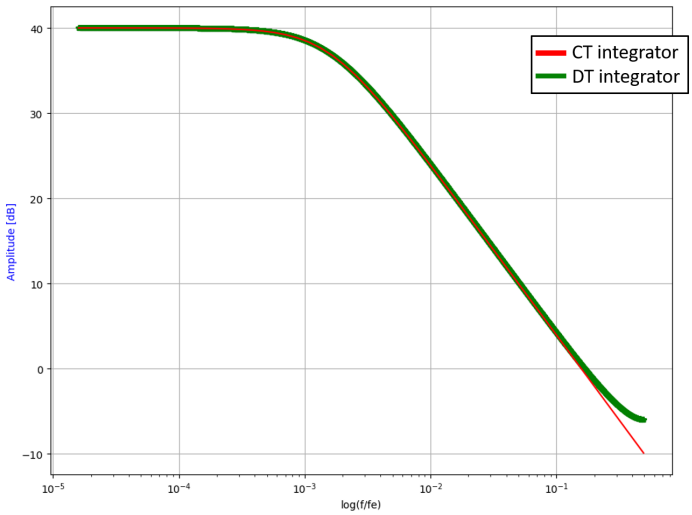

Figure 4.9: Comparison between the response of CT integrator and DT integrator (with a finite DC gain of opamp = 40 dB.

We can easily show mathematically that the transit frequency of an ideal unite DT integrator (without the effect of any coefficient) f_{TDT} as shown in figure 4.10 (a), and for a sampling frequency f_s is equals to:

$$f_{TDT} = \frac{1}{6} \times f_s \tag{4.10}$$

The transit frequency f_{TCT} in this case of an ideal CT integrator shown in figure 4.10 (b) is:

$$f_{TCT} = \frac{1}{2 \times \pi \times R \times C} \tag{4.11}$$

The equivalence between the two integrators is described by the following condition:

$$f_{TCT} = f_{TCD} \Longrightarrow R \times C = \frac{3}{\pi \times f_s} \approx \frac{1}{f_s} \tag{4.12}$$

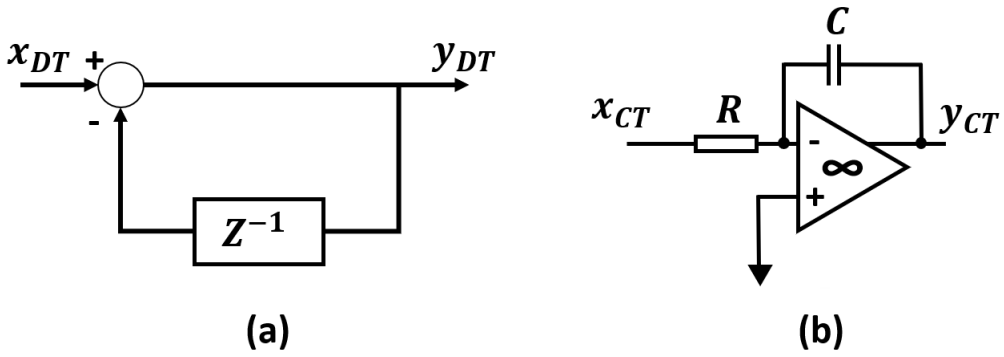

Figure 4.10: Simplified structure of an ideal CT integrator and an ideal DT integrator.

Using this result, we can directly use the performances of the SIMULINK model to size the integrator. Figure 4.11 shows the response of the first integrator of the proposed topology (without the effect of the input coefficients):

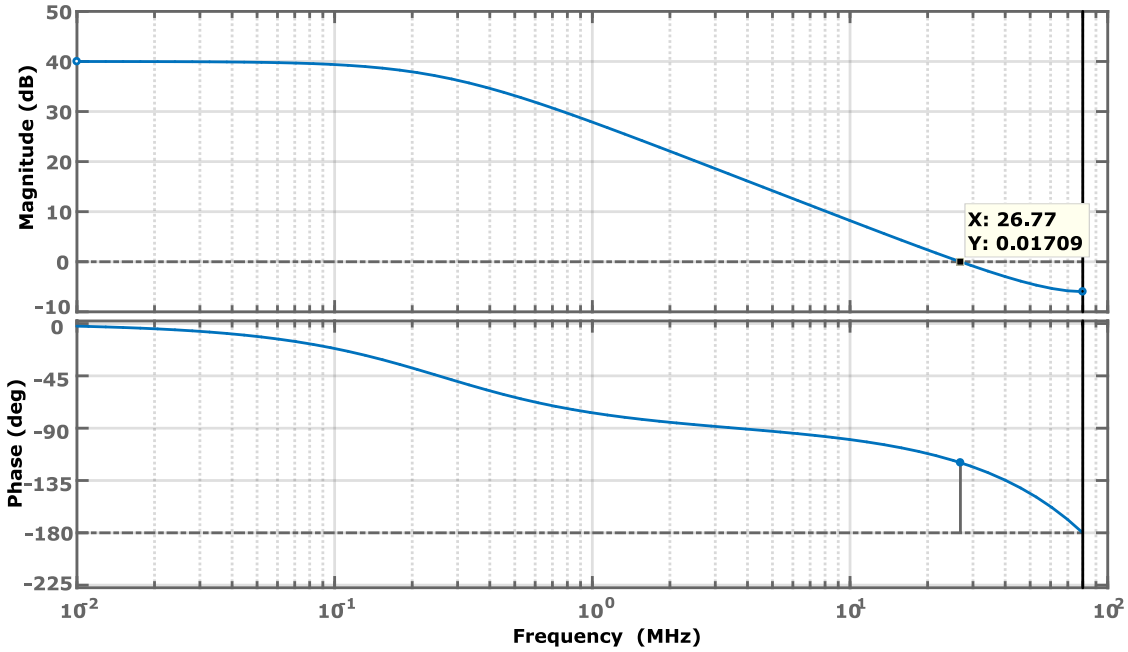

Figure 4.11: The frequency response of the first DT integrator.

Here we can see that because the sampling frequency is $f_s = 160\ MHz$, we expect a $f_{TDT} = \frac{f_s}{6} \approx 26\ MHz$ which is exactly the case. To calculate the values of R and C, we use the condition described by equation 4.12 and the result of the DT integrator: $RC = 5.96\ ns$. The values of R and C are chosen so we guarantee both an acceptable area (C value should be less than 1 pF) and an acceptable thermal noise (R in the range of few $K\Omega s$). Figure 4.12 illustrated the frequency response of the first CT integrator (shown in figure 4.8) using the opamp detailed in subsection 4.1.4.

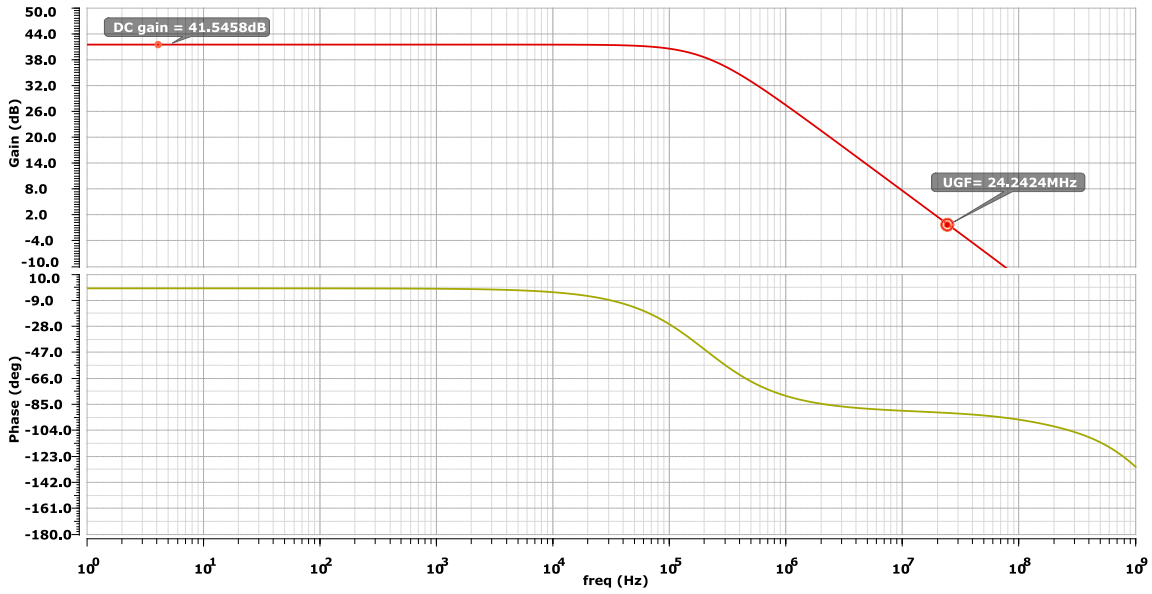

Figure 4.12: The frequency response of the first circuit level CT integrator.

We notice here that the f_{TCT} is not exactly equal to the expected value even with R and C chosen to ensure $RC = 5.96\,ns$. This difference is introduced by the finite bandwidth of the opamp (value of its UGF_{opamp}) as shown in figure 4.13.

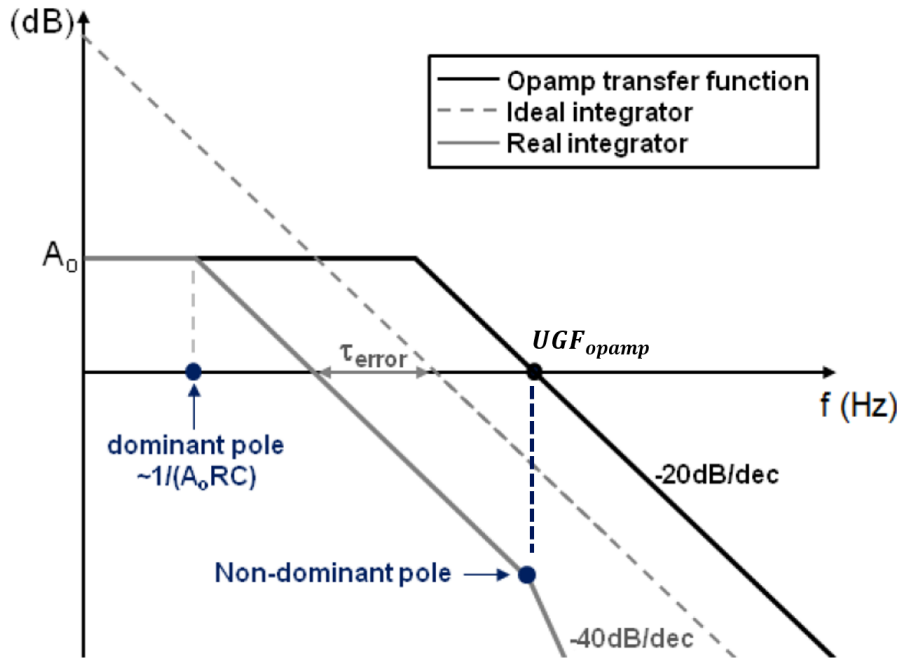

Figure 4.13: The frequency response of the first CT integrator, extracted from [12].

In the case of a real integrator (using an opamp with a finite DC gain A_0 and a finite bandwidth UGF_{opamp}) , its transfer function is [12]:

$$|H(p)| = \frac{A_0}{\left(\frac{A_0}{\omega_{TCT}} \times p + 1\right) \times \left(\frac{1}{UGF_{opamp}} \times p + 1\right)} \tag{4.13}$$

and the error introduced by the finite bandwidth UGF_{opamp}) is equals to [12]:

$$\omega_{error} = \left[\frac{\omega_{TCT}}{\omega_{TCT} + UGF_{opamp}} \times 100 \right] \% \tag{4.14}$$

By using the value of the UGF_{opamp} shown in table 4.4, we expect an error around 3%. Yet, here we have an error about 9%. We think this is caused by a degradation of the value of the UGF_{opamp} due to the resistive charge. To correct this error, we tune the value of the capacitor in order to obtain the right value of the f_{TCT}.

The next step is to implement the coefficient at the input of this first integrator (we focus here on the coefficient b_1 of the feedforward path shown in figure 3.1). Multiplying the input of an integrator by a coefficient is the same as shifting the f_T by the same value as illustrated in figure 4.14.

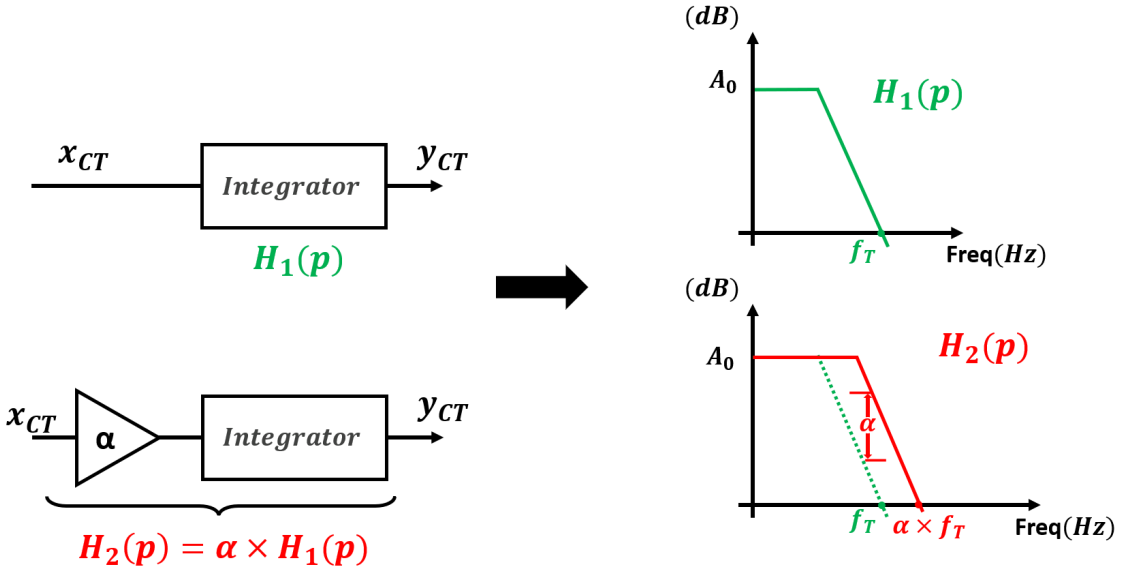

Figure 4.14: Simplified diagram of the impact of an input coefficient on the frequency response of an integrator.

To apply this, we simply change the value of $R \times C$. More precisely, we divide the value of R by the value of this coefficient.

4.2.2 Resonators sizing

To implement the resonators of the second and the third stages of the proposed architecture shown in figure 4.9, we follow the same method used in the sizing of the first integrator. Systematically, the first integrator of the resonator can be seen as a summing integrator. It adds the input signal applied through its coefficient, and the feedback signal applied through the feedback signal as shown in the simplified diagram in figure 4.15. The second integrator of the resonator is similar to the first stage. This simplification allows us to use the same equivalence between the DT SIMULINK model and the CT circuit level implementation explained for the first stage.

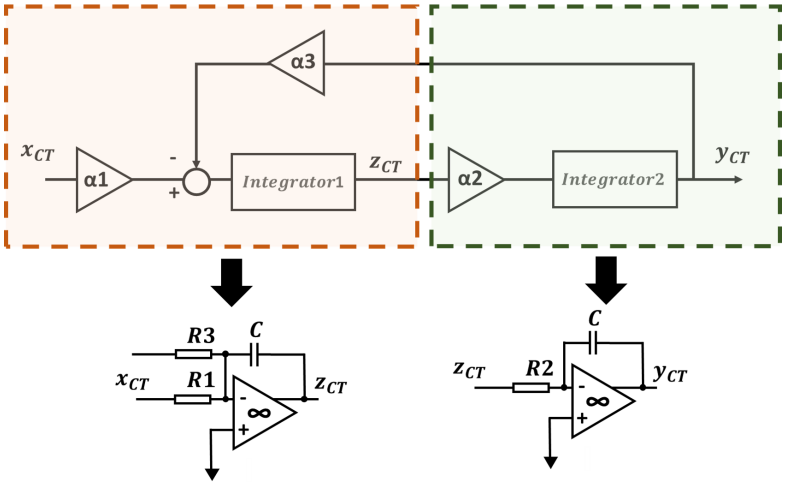

Figure 4.15: Simplified diagram of the implementation of the resonator.

We firstly use the performances of the SIMULINK model, here we show only the results of the first resonators which implies to the second resonator as well. Figure 4.16 illustrates the frequency response of the first resonator. The peak resonance of 47.5 dB is located at the frequency 5.4 MHz.

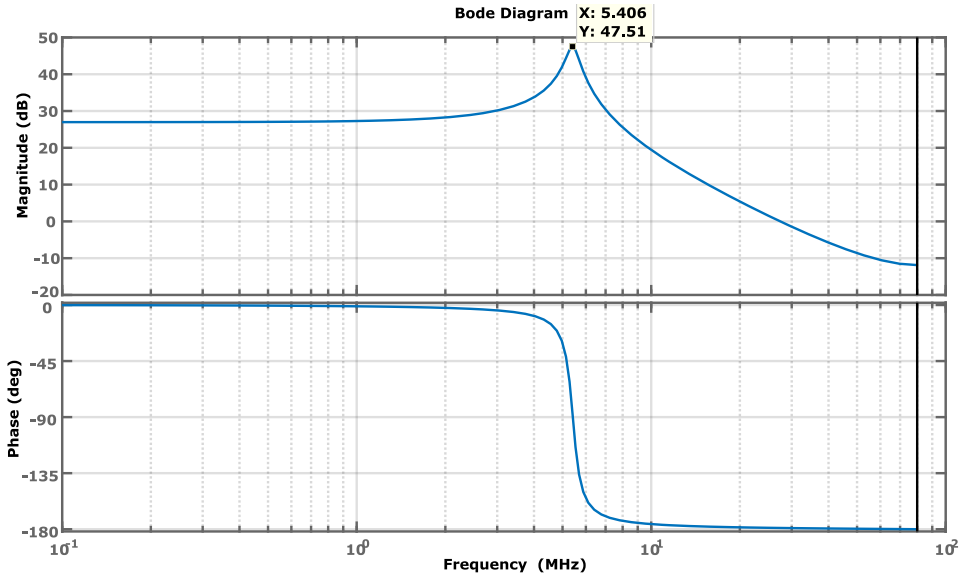

Figure 4.16: The frequency response of the first DT resonator.

The coefficients are implemented in the same way as the integrator, by calculating the values of the resistors. The opamp used is the same as well. The capacitor of integration for both integrators is equal and the same as the first stage integrator after the tuning phase. The frequency response of the implemented circuit of the resonator is shown in figure 4.17. It shows that the implementation of the CT resonator is successful and its performances are withing the expectations of the modeling results. The resonance peak of 49.1 dB is located at a frequency of 5.49 MHz and the slight difference in gain is related to the fact that the circuit level integrator has more DC gain: 41.54 dB against the modeling one with a DC gain of 40 dB as shown in figure 4.12.

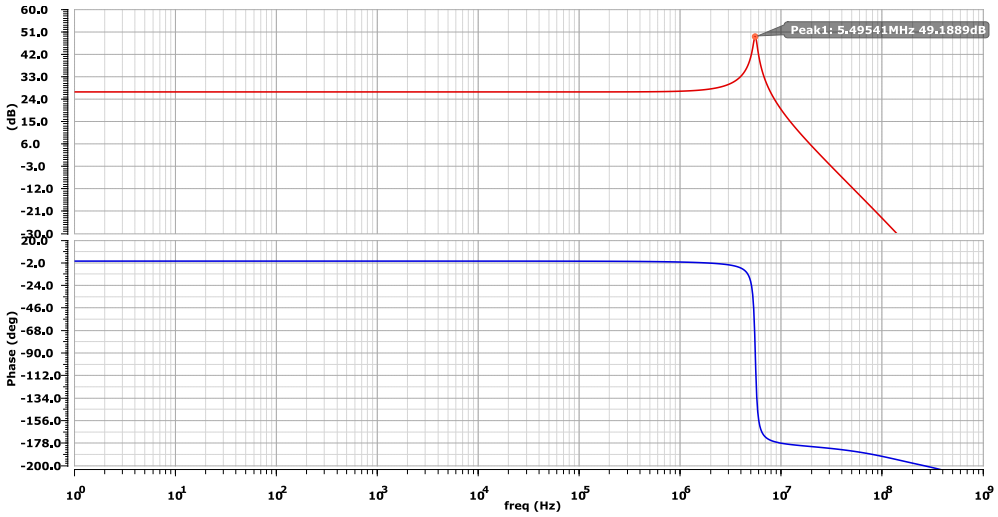

Figure 4.17: Electrical simulation of the frequency response of the first CT circuit level resonator.

4.2.3 Electrical simulation of the loop filter

The final step after the sizing phase is to validate the performances of the electrical simulation of the loop filter with the results of the modeling phase illustrated in figure 4.18. Here, we can observe the two resonance peaks at 5.4 MHz and 9.1 MHz respectively.

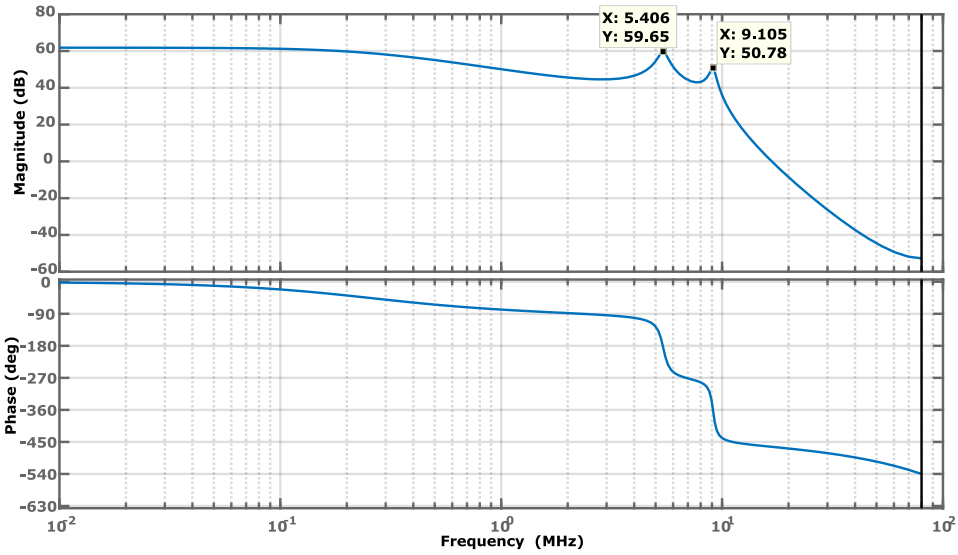

Figure 4.18: The frequency response of the first DT loop filter.

The frequency response of the CT loop filter is illustrated in figure 4.19. It shows that it follows precisely the behavior expected by the modeling results. Comparing the modeling results and the obtained results of the electrical simulations, the error on the gain of the peaks is about 3.7% and 2.2% respectively. The error on the frequencies of the peaks is about 3% and 17% respectively. We will see further that these errors are low enough to ensure a good performance of the modulator.

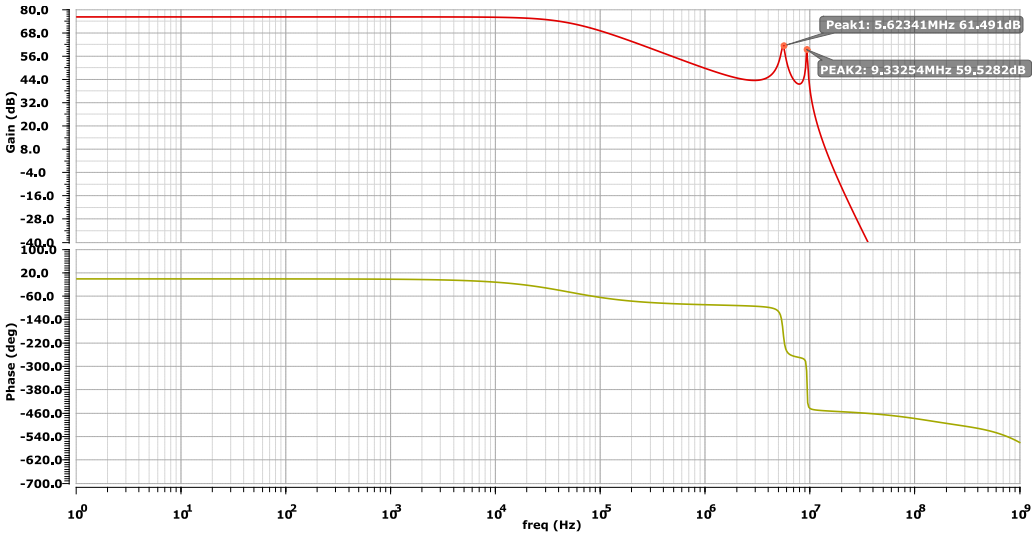

Figure 4.19: Electrical simulation of the frequency response of the CT circuit level loop filter.

4.3 Summing circuit

The summing stage is a critical block in our proposed topology. Its main function is to couple all the feedforward paths so to increase the signal swing in order to fully-load the quantizer. The proposed structure for this stage is based on a differential summing amplifier as illustrated in figure 4.20. It needs to guarantee a large bandwidth since the precision of the equivalence between the DT and CT loop transfer functions requires to maintain exactly one sampling period delay in the local feedback path. It needs as well a high DC gain to preserve the precision of the coefficients of the feedforward paths.

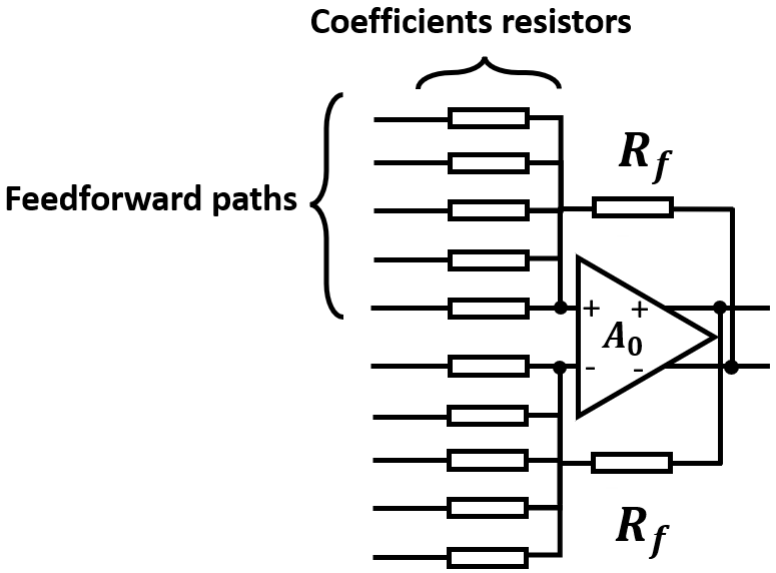

Figure 4.20: Simplified circuit level implementation of the summing stage.

It should be noted that the value of the feedback resistor is chosen carefully R_f to ensure

that the time constant formed with the capacitance at the amplifier summing node will not limit the performance of the amplifier [17]. The feedforward coefficients (named a_i coefficients in figure 3.1) are implemented as the ratio of each input resistor and the feedback resistor.

4.3.1 Amplifier topology and Sizing

For the summing amplifier, we use the same two stage NCFF opamp detailed in the subsection 4.1.3. The only diffrence is the use of a cascode stage for the implementation of the feedforward stage in order to minimize the miller effect. The proposed architecture is illustrated in figure 4.21.

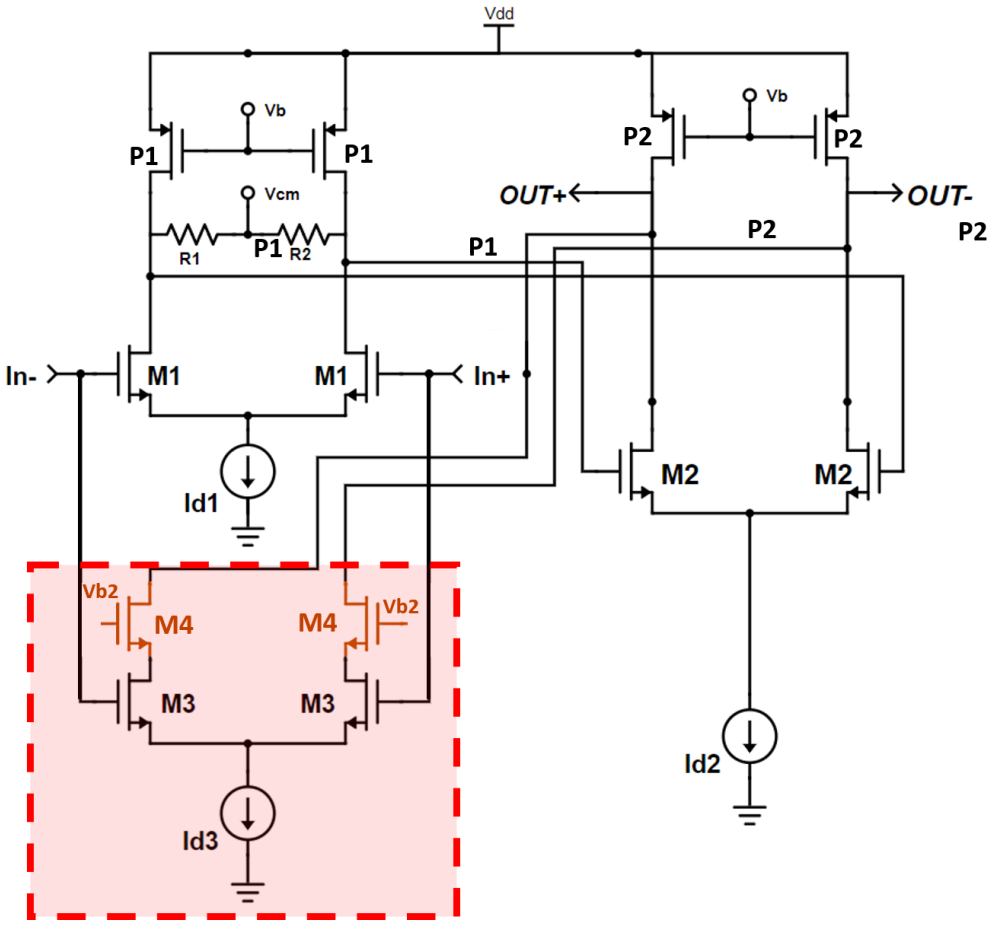

Figure 4.21: Simplified schematic of the proposed summing opamp.

4.3.2 Electrical simulations and results

We use the same design methodology to size the transistors of this summing-opamp: the g_m/I_d design methodology via Precomputed LUTs which is already discussed in the section 4.1. The results of this sizing using the MATLAB script based on algorithm 4 is summarized in table 4.5.

Table 4.5: The sizing of transistors of the proposed topology

Transistor	W (μm)	L (nm)	g_m/I_d
M_1	31.8	250	21
M_2	75	150	14.5
M_3	66.3	150	11.4
M_4	66.1	150	2.15
P_1	22.44	500	10.8
P_2	210	150	8.4

Results of the AC electrical simulation of the summing opamp after the sizing are illustrated in figure 4.22.

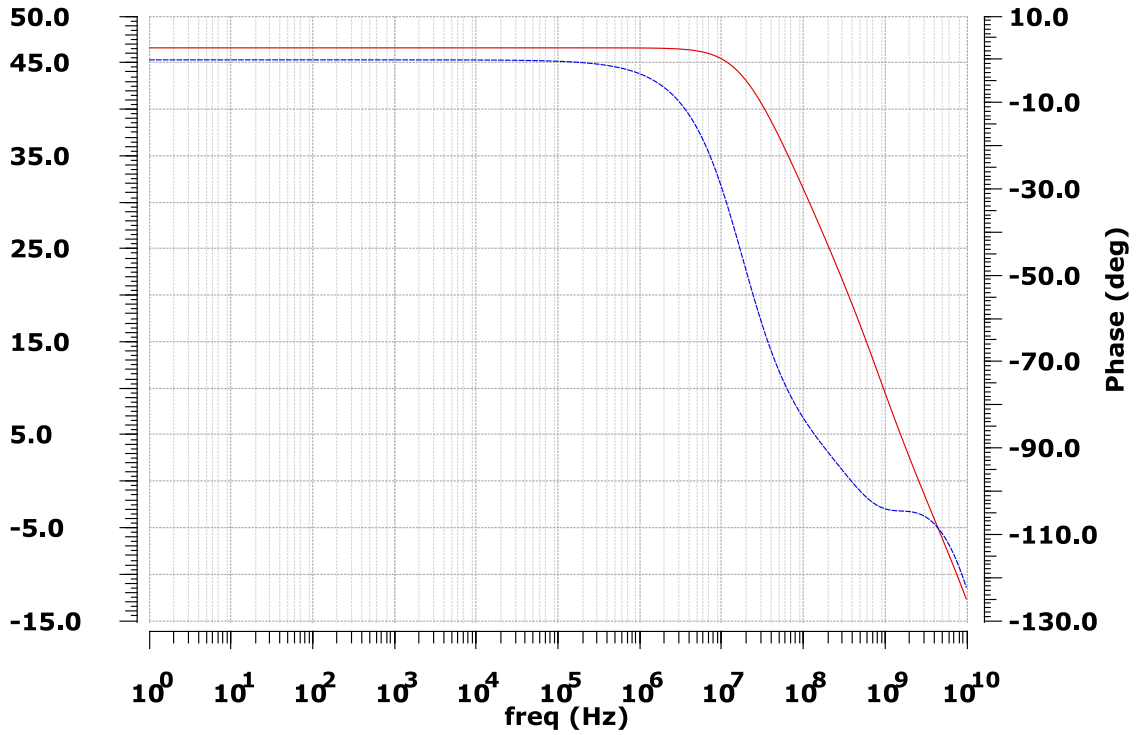

Figure 4.22: The frequency response of the proposed summing opamp.

Here, we can see that we achieve a DC gain of 46.5 dB and a UGF of 3 GHz. The stability is ensured with a phase margin higher than 80° and the power consumption is around 14 mW.

4.4 Loop Quantizer

For the loop quantizer, we decide to work with a 3 *bits* flash ADC for its simplicity of implementation and its speed (the quantizer needs to operate fast enough so that the digital output signals can settle in less than half a sampling period). Since this block is located at the back-end of the modulator, its non-idealities are suppressed by the loop filter, which generally results in very relaxed requirement.

4.4.1 Quantizer Architecture

The proposed 3 *bits* FLASH ADC consists of 7 differential comparator cells, and theirs reference voltages are generated from a 7-tap resistive ladder. Figure 4.23 shows a simplified schematics of this ADC.

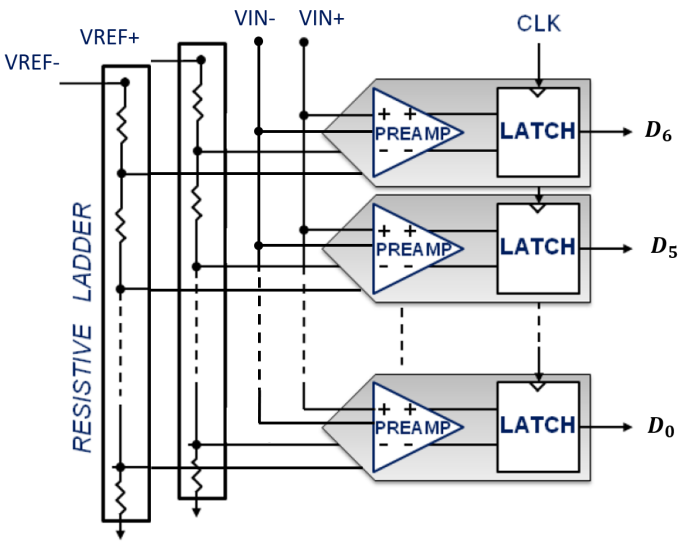

Figure 4.23: Simplified schematic of the proposed differential flash ADC.

Each comparator cell is composed of a preamplifier and a latch. It should be noted that details about the topology of the latch are not shown or discussed because this block was recovered from another project. In order to adapt it and make it suitable for this need, the preamplifier stage is added. It is an active loaded NMOS differential pair, a simplified version of its topology is shown in figure 4.24.

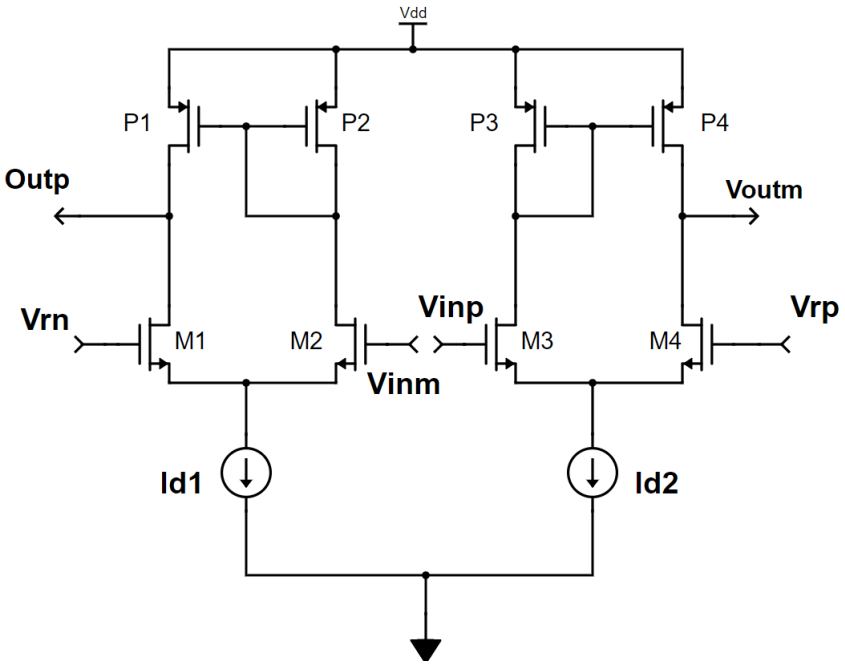

Figure 4.24: Schematic of the preamplifier.

The purpose of this stage is to compare the differential input signal with a differential reference signal, and amplify the difference. The input referred offset of the comparator is reduced now that the offset from the latch stage is divided by the gain of the preamplifier. It also isolates the latch kick-back noise from the the loop filter output. Table 4.6 summarizes the specifications of this preamplifier stage.

Table 4.6: Preamplifier key specifications.

Parameters	values
Power supply (V)	1.2
DC Gain (dB)	24.75
Loop Unity Gain Frequency (UGF) (GHz)	5.5
Load capacitance (fF)	20
Power consumption (μW)	466

It is important to mention that this chosen topology suffers from gain reduction when there is any common-mode (CM) difference between the input signal and the reference signal. This in turn increases the input-referred offset of the comparator. Figure 4.25 illustrates this issue. Here, we show the simulated preamplifier gain against the CM level difference between input and reference signals. In order to maintain a gain around 14 V/V, the CM levels of the reference and the input signals should be in a range of 10 mV of each other.

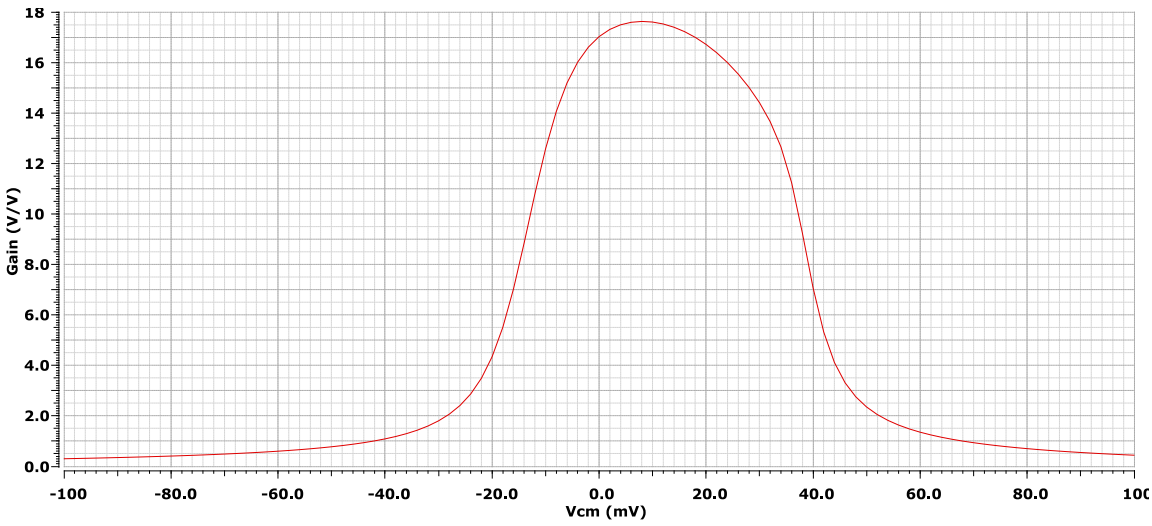

Figure 4.25: Gain variation versus CM difference between input and reference signals.

The input range of this quantizer is dictated by be the maximum output signal swing that the loop filter is capable of. In our case the single-ended signal swing of the loop filter can reach as high as 900 mV, hence the differential input range $[-900\ mV, +900\ mV]$. Based on this, we can estimate its LSB which is around 250 mV.

4.4.2 Simulations and results

As already shown in the subsection 3.3.4, this block suffers from two major imperfections, which are the offset of the comparators and the precision of the reference voltages. We use Monte Carlo simulations for both cases to estimate these values and compare it to the modeling results.

Figure 4.26 shows the results of simulations of the offset of the comparator and figure 4.27 illustrates the results for the reference voltages.

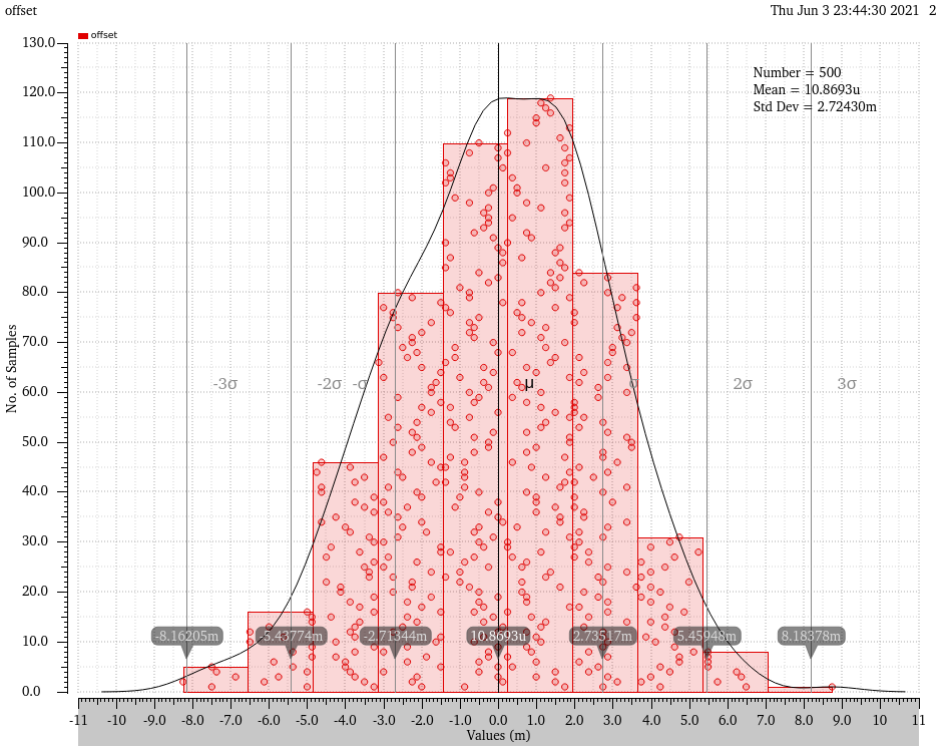

Figure 4.26: Histogram of the Monte Carlo simulations of the offset of the comparator.

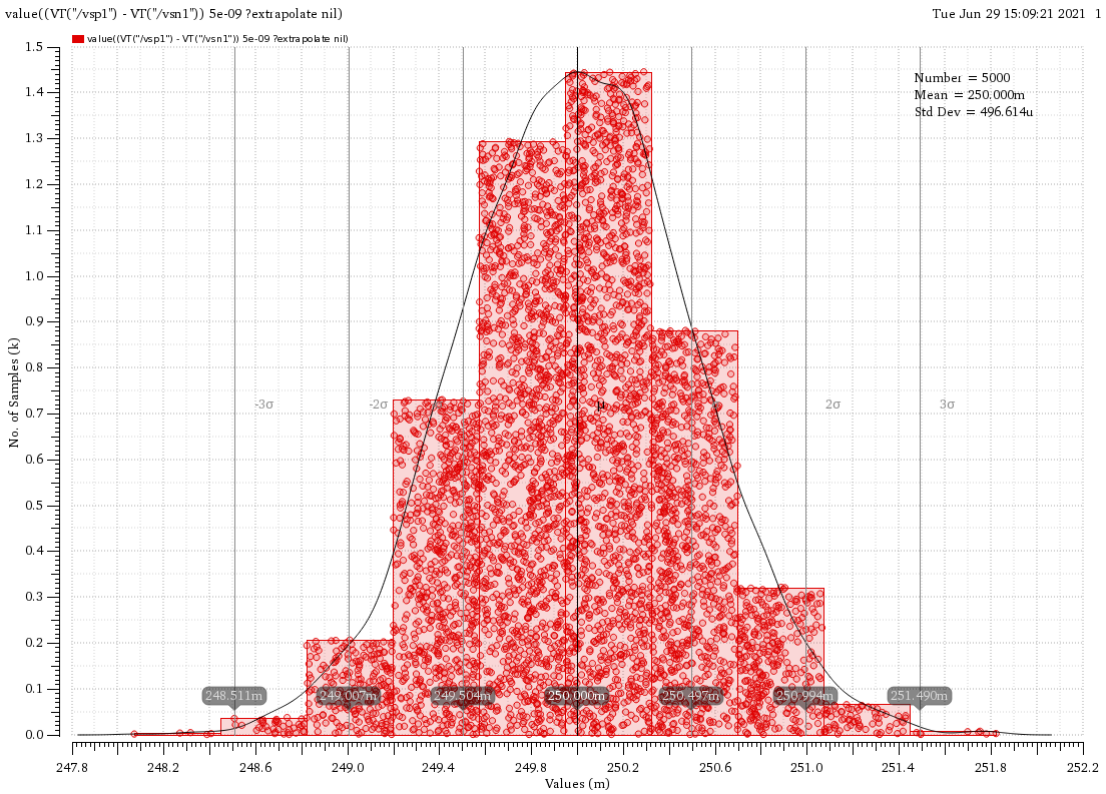

Figure 4.27: Histogram of the Monte Carlo simulations of the precision of the reference voltages.

These results shows that the offset of the comparators is the dominant imperfection (RMS values: 2.7 mV against 496.61 μV) . Comparing these results to the modeling results shown in the subsection 3.3.4, we expect a drop of the ENOB less than 0.1 bit. Table 4.7 summarizes the specifications of the proposed FLASH ADC.

Table 4.7: Loop quantizer key specifications.

Parameters	values
Type	FLASH
Sampling rate (MHz)	160
Response time of the comparator (worst case) (ps)	846
Power supply (V)	1.2
Power consumption(mW)	< 4.5

4.5 Feedback DAC

The feedback path of our modulator is mainly composed of the DAC that converts the thermometer code generated by the ADC to an analog signal that forms with the modulator input signal the setpoint of the loop. This value is determined directly by subtracting the modulator input signal and the DAC output via the coefficients c_1 and b_1 respectively (the topology is illustrated in figure 3.1 in section 3.1). The most efficient way to implement this operation is to change directly the value of the current that is integrated by the capacitor of the first integrator. The principle of this technique is shown in figure 4.28.

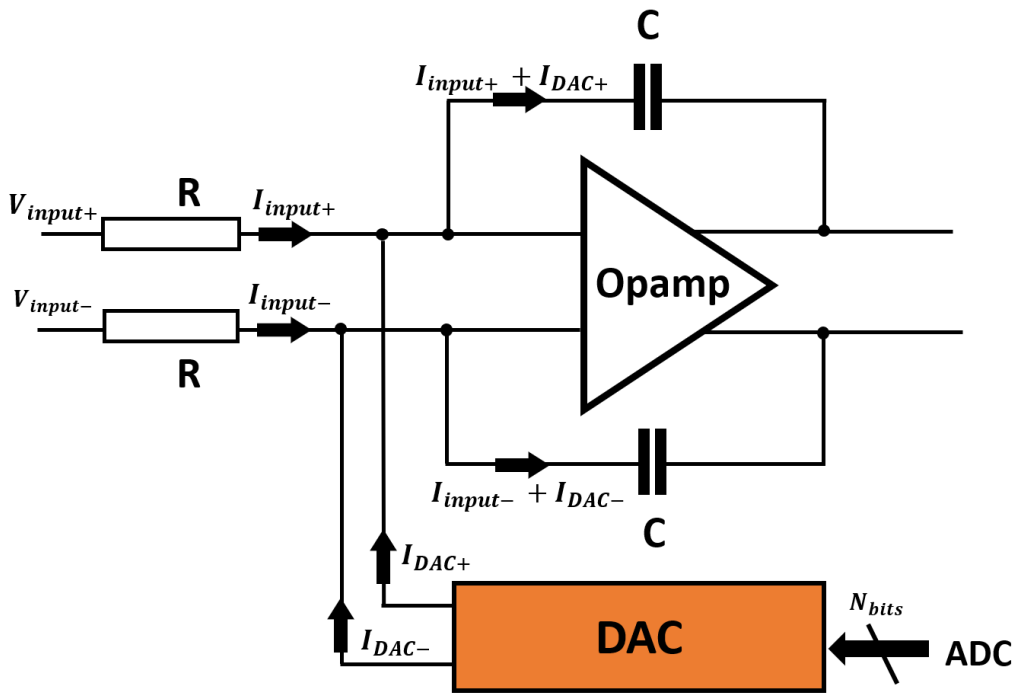

Figure 4.28: Simplified diagram of the implementation of the feedback DAC.

4.5.1 DAC Architecture

In order to implement the principle shown above, we decide to work with a 3 *bits* NRZ differential current-steering DAC [18]. It consists of 7 cells, each cell is composed of a differential switch and a tail current source (NMOS). All the cells are connected to a current mirror load (PMOS), as shown in figure 4.29.

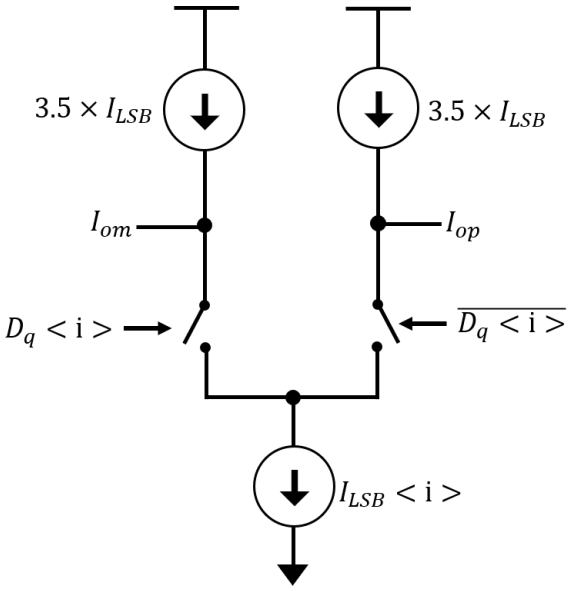

Figure 4.29: Simplified diagram of a differential current-steering DAC cell.

This topology allows us to minimize the delay between the DAC and the ADC (controlling the DAC directly using the thermometer code of the proposed ADC). It is also known to be one of the fastest topologies as well. Furthermore, using an RC-opamp as the first integrator makes the interfacing of the proposed DAC more efficient because its output terminals are connected to the virtual ground of the opamp which is ideally a zero-impedance node.

4.5.2 Simulations and results

Since the output signal of the proposed DAC is directly substracted from the modulator input, the impact of its non-idealities are not shaped by the loop filter and should be carefully analyzed. We already shown in the subsection 3.3.4 the results of the modeling of this imperfections in terms of mismatch and how it affects the DNL of the DAC. We used these results to validate the implementation.

Before that, it is important to mention, in the case of a current-steering DAC (figure 4.29). In order to correctly size the current mirrors, it is necessary to know the technological dispersions for the used 130 *nm* CMOS technology. It is known that the charges trapped in the gate oxides induce a random dispersion on the threshold voltages of the transistors. Thus, this dispersion causes an error on the current mirrors. We perform Monte Carlo simulations to characterize the error on these mirrors. The results are illustrated in figure 4.30. In our case, we retained the 2nd point on figure 4.30, which gives us an error of 0.4%.

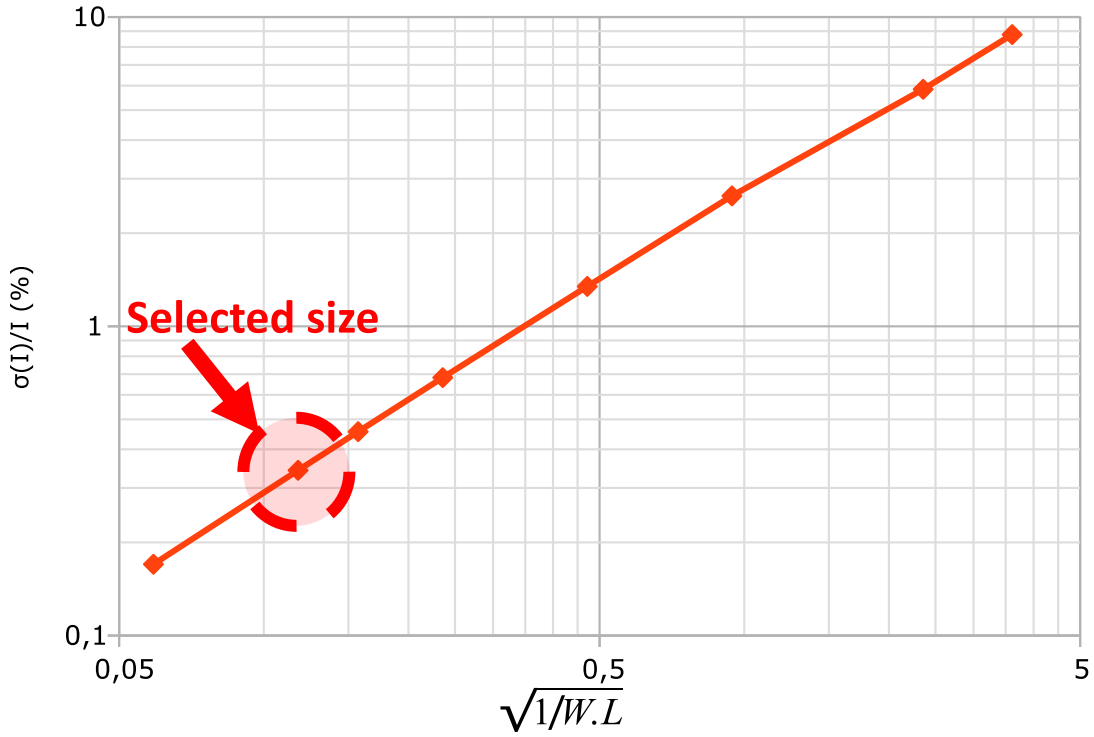

Figure 4.30: Technology matching for NMOS current mirror.

For the first simulation, we show the transient response of the proposed DAC without the imperfections of in terms of mismatch. The value of the LSB is calculated based on the value of the full scale of the ADC, the number of bits of the ADC/DAC (which is 3 in our case) and the coefficient c_1 which is equivalent to a resistor (detailed in the subsection 4.2.1) as shown in the following equation:

$$I_{LSB} = \frac{Fs_{ADC}}{2 \times (2^3 - 1) \times R_{c_1}} \tag{4.15}$$

with:

- $R_{c_1} = 47.57\ K\Omega$
- $Fs_{ADC} = 1.8\ V$ (V_{p-p} differential)

This gives us a value of $I_{LSB} = 2.7\ \mu A$. Figure 4.31 illustrate the results of this simulation. We can see that the proposed topology works well as a differential 3 *bits* DAC with the wanted LSB.

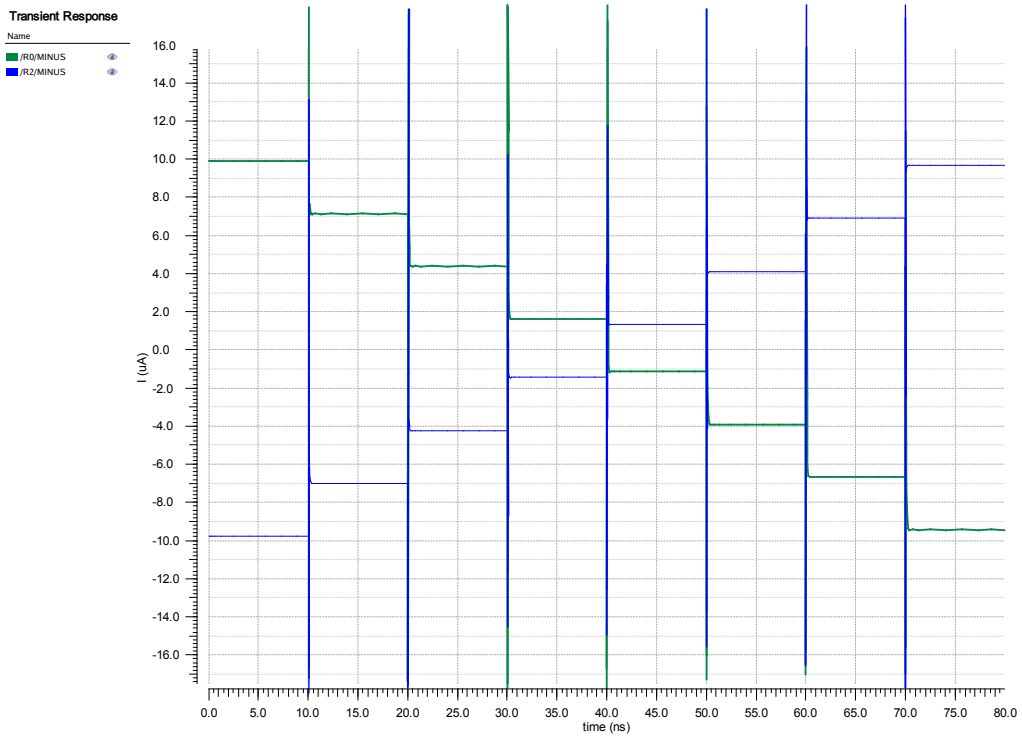

Figure 4.31: The transient response of the proposed feedback DAC.

The second simulation is to check the behavior of the DAC through Monte-Carlo simulations to simulate the impact of the current mismatch. Figure 4.32 illustrate the results of this simulations.

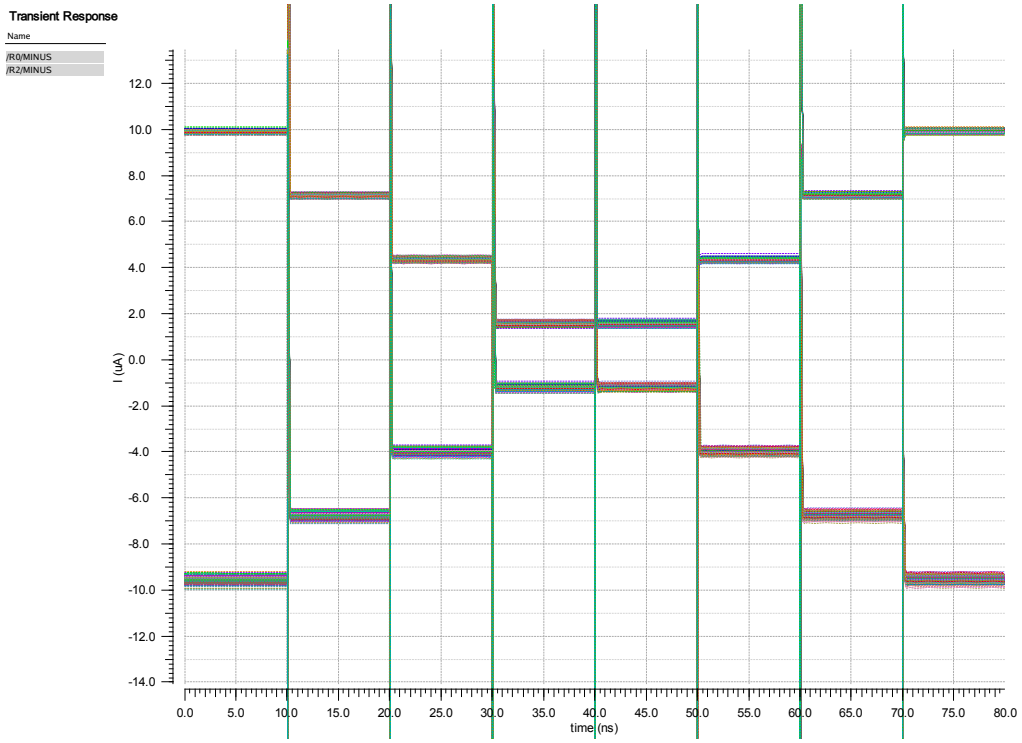

Figure 4.32: The transient response of the proposed feedback DAC through Monte-Carlo simulations.

We can see that the value of the LSB changes and it is not constant from a step to another. To

investigate this, we calculate the DNL for 500 runs. Results are shown in figure 4.33.

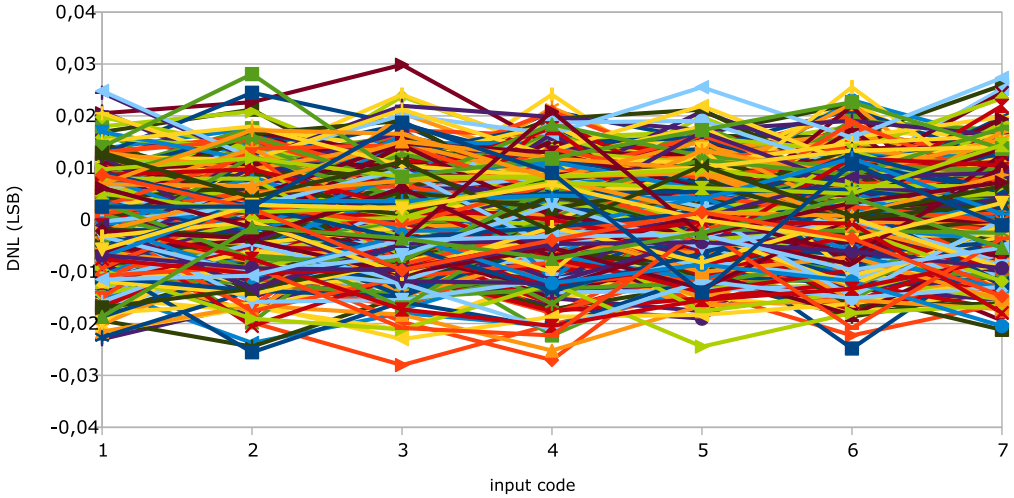

Figure 4.33: The values of the DNL for 500 *runs.*

Comparing these obtained values to the estimation of the drop of the ENOB (related to the DNL of the DAC) done in the subsection 3.3.4, we expect to have a degradation of less than 0.03 LSB. Table 4.8 summarizes the specifications of the proposed DAC.

Table 4.8: DAC key specifications.

Parameters	values
Type	NRZ
Settlement time (ps)	< 250
Power supply (V)	1.2
Current mismatch	$< 0.4\%$
DNL (LSB)	± 0.03
Power consumption(μW)	< 40

4.6 Full modulator Simulations

In this section we discuss the overall performance of the transistor level modulator and compare it with the modeling results. For stability reasons, we could not directly simulate the modulator using the integrators shown above. To enable it, we added a resistor in serie with the feedback capacitor of each integrator. This was detailed in [19] and it helps to restore a positive phase margin which leads to stability. Unfortunately, due to time constraint , we did not analyze in depth this solution. Yet, for all the results showing below, this solution is implemented and it works.

4.6.1 Electrical simulations

Here, we provide the transistor-level simulation results of the proposed 5^{th} order CT LP CRFF $\Delta\Sigma$ modulator. All the blocks are designed in a 130 *nm* CMOS technology. The sampling frequency is 160 MHz and the BW of the modulator is 10 MHz. Figure 4.34 illustrates the output PSD of the modulator.

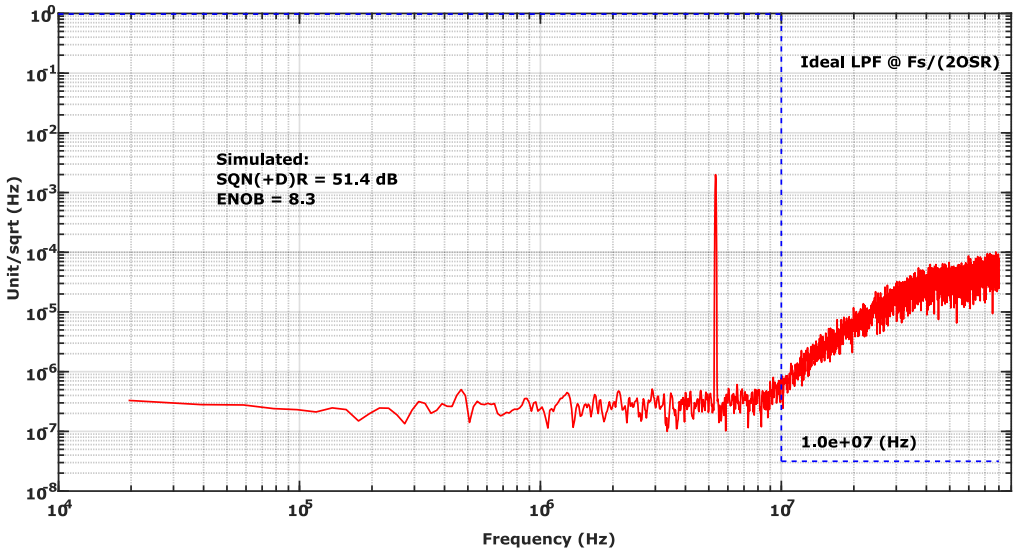

Figure 4.34: Simulated output PSD of the modulator with a -3 $dBFS$, 5.33 MHz input signal.

For this, we use a sinwave with an amplitude of -3 $dBFS$ (for a differential FS of 1.8V, the differential input amplitude is around 1.28 V) which is the MSA and a frequency of 5.33 MHz, the FFT is calculated for ($N_{FFT} = 8192$). We obtain a SNR of 51.4 dB or an ENOB of 8.3 $bits$.

In order to estimate the MSA and the DR of the modulator, we simulate the modulator using different input amplitude and we estimate the SNR in each case. Results of this process is illustrated in figure 4.35. We achieve a DR of 56 dB and a MSA at -3.5 $dBFS$.

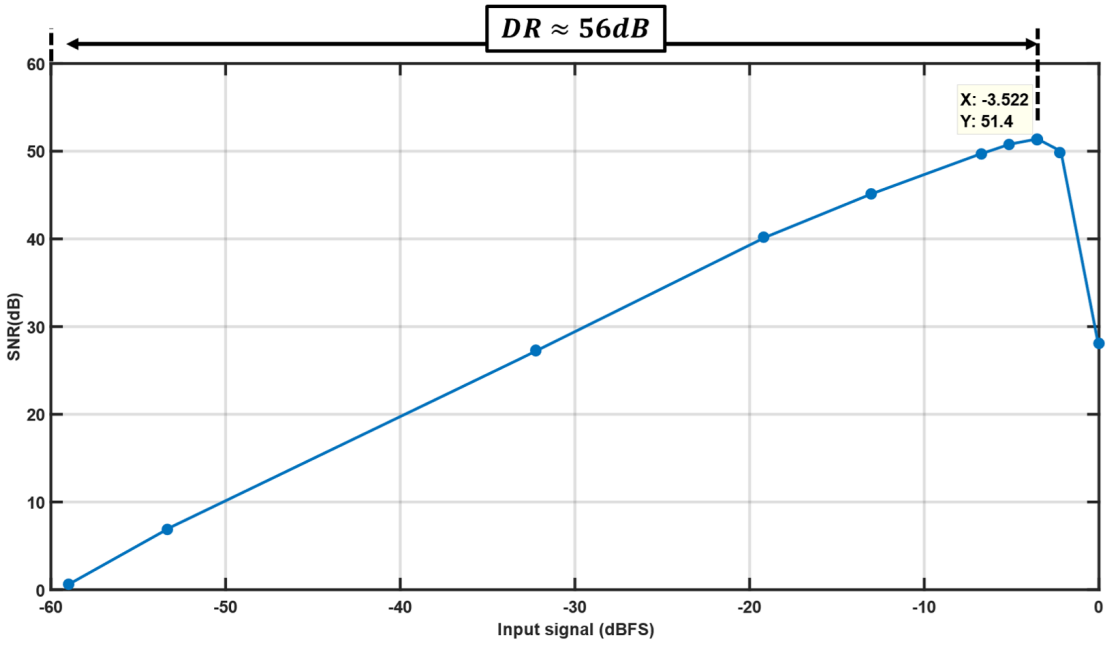

Figure 4.35: Simulated SNR versus input signal power.

4.6.2 Results discussion

Comparing the obtained results of the circuit level simulations and the modeling results, we observe a drop of around 20 *dB* for both the SNR and the DR. This was already expected, because it is recommended in [16, 20, 21] to choose the theoretical SQNR to be 10–20 dB higher than the one desired, in order to provide some tolerance for the inevitable degradation caused by circuit non-idealities.
To clarify the impact of each block on the overall degradation, we simulate the modulator in different situations where we swap the transistor level blocks with ideal blocks: For the integrators, we use an opamp based on the ***VCVS*** blocks, we use the same block for the ideal summing circuit. For the loop ADC and feedback DAC, we use verilogA models. The obtained ENOB in each case is summarized in table 4.9.

Table 4.9: Values of ENOB for each degradation source.

Model	ENOB
All blocks are ideal	10.2
All blocks are ideal except the summing block	10
All blocks are ideal except the loop filter integrators	10
All blocks are transistor level except the summing block	9.1
All blocks are transistor level except the DAC/ADC	8.9
All blocks are transistor level	8.3

This results shows that the maximum degradation is caused by the loop filter. The primary issue comes from the resistor in serie with the capacitor that degrades the quality of the loop filter response as shown in figure 4.36

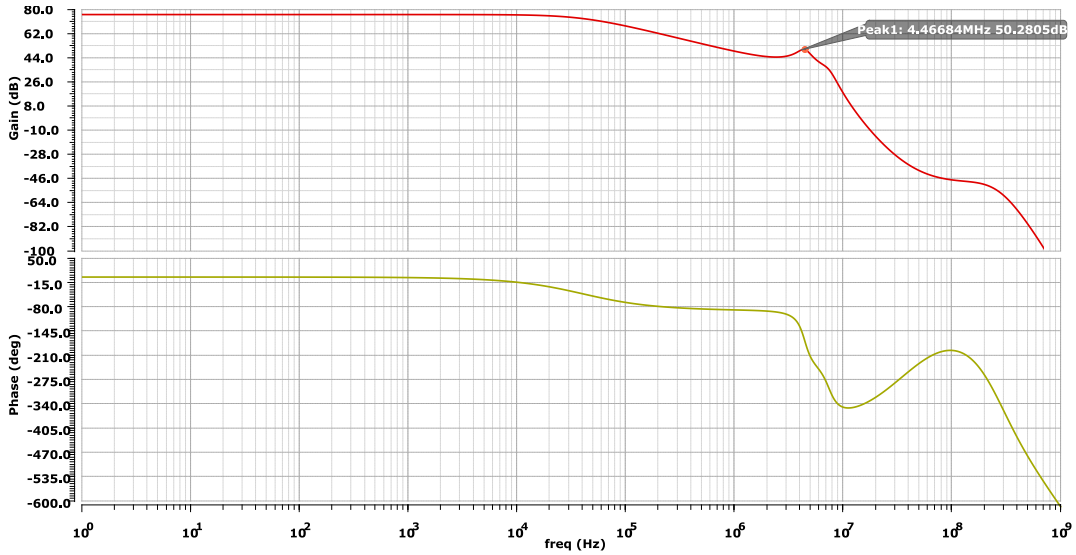

Figure 4.36: The frequency response of the circuit level loop filter using the resistor in serie with the feedback capacitor.

This issue can be minimized by tuning the coefficient resistors of each feedback path of both resonators. Unfortunately, due to time constraint we did not try this yet.

These results shows also the possibility to obtain a better ENOB by optimizing the summing block as well.

To conclude this discussion, the estimated power consumption from each building block is summarized in table 4.10.

Table 4.10: Static power consumption of the modulator.

Block	**power consumption details** (mW)	**Total** (mW)
Loop filter	5×4.4	22
Summing block	1×14	14
Loop ADC	7×0.47	3.3
feedback DAC	1×0.04	0.04
	TOTAL	**39,34**

The static power consumption is dominated by the the opamps of the loop filter and the summing stage as shown in figure 4.37.

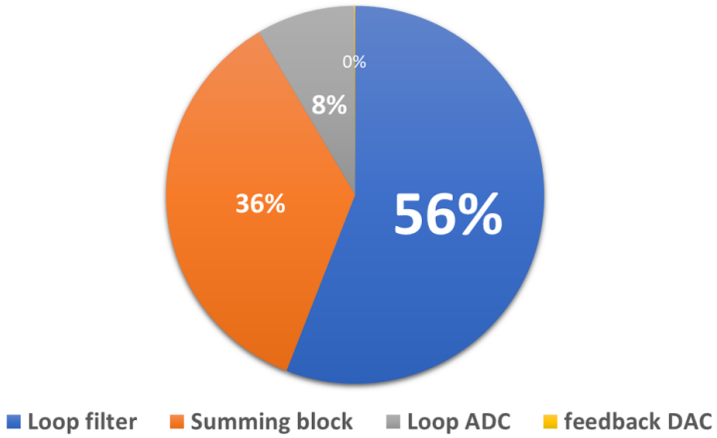

Figure 4.37: Breakdown of the power consumption among the main blocks of the modulator.

The achieved performances of this proposed topology are summarized in table 4.11

Table 4.11: Simulated modulator performance.

Parameter	**Achieved**
Technology	CMOS 130 nm
Architecture	5^{th} order CT LP CRFF $\Delta\Sigma$
Sampling frequency	160 MHz
Signal bandwidth	10 MHz
MSA voltage	$-3.5\ dBFS/1.2\ V_{p-p}$ (differential)
SNR	51.4 dB
ENOB at MSA	8.3 $bits$
DR	56 dB
Power supply	1.2 V
Power consumption	39.43 mW

4.7 Summary

In this chapter, details about the trasistor level design and sizing of each block are presented and detailed. We start by explaining the integration of the g_m/I_d design methodology via Precomputed LUTs in the proposed workflow and the choice of the topology of the opamps. To follow that, we provide details on the sizing of the integrators and resonators of the loop filter. We showed as well the structure and performance of the loop ADC and the feedback DAC. Results of simulations of the full modulator are detailed and discussed comparing it with the modeling results to validate the proposed topology. We achieve an ENOB of 8.3 $bits$ for an MSA of -3.5 $dBFS/1.2$ V_{p-p} (differential) with a signal bandwidth of 10 MHz and a power consumption of 39.43 mW.

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Conclusion and future work

Conclusion

In this thesis, a 5^{th} order CT LP CRFF $\Delta\Sigma$ modulator is proposed [1]. It is designed to be implemented in a 130 nm CMOS technology, achieving a signal BW of $10MHz$ (can achieve 40 MHz) and a SNR of 51.4 dB. We use an OSR of 8, which means a sampling frequency of 160 MHz. In this configuration, the power consumption is estimated around 39 mW.
This circuit is targeted to be used in building an ADC. It is proposed for a novel topology of an energy measurement system. Combined with a timing measurement system [2, 3, 4], the two construct the readout electronics of an hodoscope based on CVD diamond detectors and will be used for the enhancement of the efficiency of hadrontherapy [5].

On the system level, the complexity of designing CT is addressed using a proposed workflow. It is based on the model-design approach and the combination of SIMULINK graphical models with MATLAB scripts [6]. It allows the integration of Schreier's toolbox which ensures that the calculated coefficients guarantee the desired specifications and the stability of the modulator. Thus, an aggressive NTF is targeted using a 5^{th} order loop filter and a high OBG value of 3.7. This methodology allows as well to analyze different non-idealities of each building block in order to extract as much information as possible for the circuit level design phase. These results enables to validate the choice of the CRFF topology, the order of the loop filter, the resolution of the loop quantifier, and the type of the feedback DAC. It also provides important data on the tolerated values of the ELD and the most critical nodes in terms of PVT and mismatch [1]. Finally, this methodology provides tools to improve and study possible ways of optimization as shown in the case of the opamps DC gain.

On the circuit level, the design of integrators and resonators based on the NCFF topology [6] shows that these topology is suitable for the implementation of LP CT $\Delta\Sigma$ ADCs. The use of the g_m/I_d design methodology via Precomputed LUTs for the sizing of the transistors enables achieving good primary performance in terms of gain, bandwidth, stability and power consumption. The obtained modulator has an ENOB of 8.3 $bits$ for an MSI of $-3.5\ dBFS/1.2V_{p-p}$ (differential) with a signal bandwidth of 10 MHz and a power consumption of 39.43 mW.

Future work

For the current design, our efforts have been mainly on the system level design by proposing a workflow based on the model-based design paradigm, and the integration of the g_m/I_d design methodology via Precomputed LUTs for the sizing of the transistors [6]. Firstly, more work is needed in this phase, starting from the study of optimizing the DC gain of each integrator of the loop filter as we demonstrated. It shows promising results to increase power efficiency and to use simpler opamp topologies: by customizing the topology of each opamp at the lowest acceptable

requirements while guaranteeing the SNR and combining it with the integration of the g_m/I_d design methodology via Precomputed LUTs, we accelerate the transistor level implementation of a more energy efficient prototype. In addition to that, we need to investigate more critical non-idealities such as the impact of the clock jitter and the metastability of the quantizer [7, 8]. Moreover, extracting more data about the performance of the modulator is necessary to estimate more parameters such as the THD and the SNDR. Finally, working on the implementation of correction and compensation models is important to study and analyze future possibilities of optimization like the DWA (data weighted averaging) for the DAC, the correction of the time shift of the integrators [9] and the tuning of the coefficients with more realistic models of each building block. It is also important to think about a smoother transition between the modeling phase and the use of the g_m/I_d design methodology via Precomputed LUTs, one promising concept to try is shown in [10]. For the circuit implementation of the current design, the next step is to tune correctly the coefficients in order to correct the response of the loop filter. After that, working on the layout design and validating the obtained results via post-layout simulations. The final step is to test the circuit. This requires working on the implementation of different decimation filters in FPGA and preparing the test setup. In case the results are acceptable, it is important to test the circuit in a real use case with CVD diamond detectors.

For future designs, in terms of power efficiency, it seems interesting to investigate different ways of implementing the resonators such is the case of using single opamp resonators [11, 12]. Also, using a loop filter without the summing stage [13]. In terms of the SNR, analysing the possibility to increase the resolution of both the loop quantizer and the feedback DAC. Moreover, exploring other modulator topologies like the noise-coupled time-interleaving implementation [14] or VCO-based structures [15, 16]. In terms of our context, working on the implementation of custom decimation filter that suites the desired characteristics of detection [17] and also the possibility to control the STF behaviour of the modulator [18].

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