High Resolution Continuous Time ADC for Crystal-less Systems

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This thesis is entirely dedicated to the memory of Angelo Nagari.
Passed away too soon in 2018, just before this project started,
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I wish to all of you a good time reading this thesis and I really hope you will enjoy it.

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Résumé en Français

L'objectif du projet de thèse est de réaliser un Convertisseur Analogique-à-Numerique (CAN, ou ADC en anglais) pour applications audio à portabilité élevée, telles que USB-C, Wi-Fi ou Bluetooth, par exemple un microphone pour conférences. Pour ce type d'applications, qui visent une haute-dynamique et des très faibles consommations, un convertisseur sigma-delta à temps continu semble être le meilleur choix.

Toutefois, le bruit au repos de ce type d'ADC est impacté par le bruit d'horloge. Le problème est amplifié du fait que la synthèse d'horloge, en visant également des faibles consommations, est réalisée en ayant comme référence un oscillateur intégré et non pas un quartz, qui est connu pour avoir des faibles performances en bruit d'horloge notamment. Il est toutefois possible de réduire l'impact du bruit d'horloge sur des structures à temps continu grâce à des circuits de contre-réaction.

Selon les recherches bibliographiques, aucun travail n'a été effectué en utilisant une référence sans quartz avec un Sigma-Delta en temps continu d'ordre élevé. Il a aussi été tout de suite dévoilé le fait qu'il n'existe pas dans la littérature un modèle quantitativement fidèle pour la simulation du bruit d'horloge, ce qui est extrêmement important : vue la situation, il y a besoin d'un modèle très fin pour pouvoir quantifier l'impact du bruit d'horloge et l'efficacité des contre mesures connues. Il faut pouvoir tester le dimensionnement de ces dernières en vérifiant que la solution soit d'abord faisable, puis convenable sous le point de vue de la consommation en puissance et surface.

Toujours pour garder la conception simple et moins coûteuse en puissance et surface, le choix d'un quantificateur mono-bit ainsi qu'une fréquence de suréchantillonnage basse a été choisie. Toutefois, cela implique que l'ordre du modulateur sera élevé, notamment un quatrième ordre. Il est donc aussi important de vérifier que la stabilité soit garantie, surtout avec la présence du FIR-DAC qui rajoute des délais dans la transmission des signaux rebouclées.

Dans la littérature, il n'y a pas de critère de stabilité décrit pour les modulateurs d'ordre supérieurs à deux. Une situation d'instabilité peut être déclenchée par des signaux ou bruits injectés dans la structure qui amènent les états internes dans des combinaisons que la structure même n'est plus capable de compenser. Comme conséquence les états internes évoluent vers un pattern périodique où le modulateur se bloque définitivement. Ce dernier ne décrit carrément pas le signal d'entrée et ne pourra plus le faire, au moins que le modulateur soit redémarré dans des conditions opportunes.

Il faut donc explorer une solution qui permette d'empêcher le modulateur d'entrer dans des zones d'instabilité. En plus, lors d'un signal ou bruit qui normalement n'est pas gérable est injectée puis cesse d'exister, il faut que cette solution permette de représenter le signal d'entrée original correctement dans des délais de quelques échantillons. De cette manière, un éventuel son abrupte sera à une fréquence suffisamment élevée de ne pas pouvoir être entendu par l'oreille humaine.

Les deux aspects innovant principaux, c'est-à-dire, la gestion du bruit d'horloge et de la stabilité, ont été analysés en détail pendant la conception d'un modulateur sigma delta à temps continu mono-bit d'ordre quatre, qui a été ensuite réalisé sur silicium en technologie HCMOS9A et testé en laboratoire.

Abstract

The objective of this thesis is to design an Analog-to-Digital Converter (ADC) for high portability audio applications, such as USB-C, Wi-Fi or Bluetooth. An example can be a microphone for conferences. For this kind of applications, targeting a high dynamic range and low power consumption, a continuous-time sigma-delta modulator seems to be the best choice.

However, this kind of solution is severely impacted by clock jitter noise. Furthermore, a quartz-less clock is preferred in order to lower even more the power consumption, but this kind of clock generation circuit is known to have poor jitter performance too. The combination of the two reveals a scenario where an even more severe degradation is expected to be caused by jitter overall. There exist, however, techniques to reduce the impact of jitter on a continuous-time sigma-delta modulator.

The state of the art does not contain any work combining a continuous-time sigma-delta modulator and a quartz-less clock generation circuit, as well as it does not exist any quantitative jitter simulation model. The latter is extremely important to face this scenario, as sizing the circuit dedicated to jitter reduction can be carried out only with an accurate and quantitative inspection. This process revealed the feasibility of the project and its convenience under the point of view of power and surface consumption.

To further improve the latter two aspects, along with keeping the design as simple as possible, a single-bit quantizer and a low sampling frequency have been chosen. This implies that the order of the internal loop filter has to be high, in particular a fourth order was used. Assuring stability of the modulator becomes then of primary importance, in particular given that a FIR-DAC is present in the feedback path of the loop filter.

There exist no mathematical proof for stability criteria in the state of the art for what concerns modulators of order higher than two. An instability may occur if an ill signal or noise is injected in the modulator, which bring the internal states to subsequently assume values that the modulator itself is no more capable to compensate. The consequence is that the internal states evolve towards a periodic pattern on which the modulator is locked indefinitely. This pattern, of course, does not represent the input signal and never again will the modulator be able to, unless it is reset to a favorable initial condition again.

A solution preventing the modulator to enter an instability region is then mandatory. Furthermore, this solution should be able, in case of a signal impossible to manage was injected in the modulator, to represent the input signal correctly again within some samples. In this way, any abrupt sound will be at a frequency sufficiently high, in order not to be heard by human ear.

A quantitative jitter model to accurately verify the capability of the jitter reducing technique used and an empirical method ensuring stability are the two main innovations presented in this thesis. They have been analyzed in detail while designing a single bit, fourth order continuous-time sigma-delta modulator, which has been fabricated on silicon in HCMOS9A technology and measured in laboratory.

Contents

List of Abbreviations

ADC	Analog to Digital Converter
CAD	Computer-Aided Design
CIFB	Cascade of Integrators with Feed-Back (paths)
CIFB-FF	CIFB and additional Feed-Forward paths
CIFF	Cascade of Integrators with Feed-Forward (paths)
CIFF-FB	CIFF and additional Feed-Back paths
CMFB	Common Mode FeedBack
CTSDM	Continuous-Time Sigma-Delta Modulator
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DRM	Design Rule Manual
FFD	D-Flip-Flop
DR	Dynamic Range
DTSDM	Discrete-Time Sigma-Delta Modulator
ENOB	Effective Number Of Bits
FIR	Finite Impulse Response
FOM	Figure of Merit
FS	Full Scale (Range)
FSR	Full Scale Range
GBW	Gain-Bandwidth (Product)
LF	Loop Filter
LSB	Least Significant Bit
MSA	Maximum Stable Amplitude
NTF	Noise Transfer Function
OBG	Out-of-Band Gain
OPA	OPerational Amplifiers
OSR	Oversampling Ratio
PDM	Pulse Density Modulation
PWM	Pulse Width Modulation
PLS	Post-Layout Simulations
SC	Switched Capacitor
SDM	Sigma Delta Modulator
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SPL	Sound Pressure Level
SR	Slew Rate
THD	Total Harmonic Distortion

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Chapter 1

Introduction

1.1 Overview

Storing audio in digital format allows to have much more portable devices with respect to the analog counterparts. The difference in portability between having a single album on vinyl records (or a few records on a tape) and storing entire discographies from several authors on an hard drive is undeniable, especially if absolute quality of sound is not desired. Audio data such as that contained in songs or movies can be physically stored on smartphones or tablets, or even be downloaded or buffered from internet or cloud services; all of this made possible by having audio data on a digital support. If thinking beyond private use of audio data, anyone can figure himself the difference for companies and institutions if they had to store recorded conversations, meeting and conferences in audio tapes, rather than on hard drives. All of these reasons, even just at glance, justify making use of the digital world for audio purposes.

Recording and reproducing digital audio needs a conversion chain, respectively from analog to digital and from digital to analog. The conversion chain is the ensemble of circuit blocks necessary to get the digital equivalent of a physical (analog) signal, and vice versa. Generally, there is a device responsible of the latter which is different from the physical signal acquisition (microphone) or reproduction (speaker). This means the signal moving between acquisition/reproduction device and the rest of the chain is analog (very low voltage).

With newer technologies being developed through years, the portability of audio devices became even higher. Wi-Fi, Bluetooth, USB Type-C and any other kind of wireless or very low power audio applications brought up having very small stand alone recording/reproduction devices, such as wireless earpieces and very small wireless microphones for conferences.

The latter group of devices imply a fundamental change in interfacing analog and digital worlds and vice-versa. To visualize both cases, two examples, one with a microphone and one with a speaker, are represented in Fig. 1.1 respectively on top and bottom; each of the two are showing a first row where the medium carries an analog signal (jack cable) and a second row where the medium carries a digital signal (USB cable). The example is made for USB Type-C application which is at the base of the project of this thesis, but the medium can be the air, as is the case for wireless. In this thesis purpose, we shall also already begin to address from now on to the necessity of interfacing a microphone, that is, addressing to the case of an Analog-to-Digital conversion chain.

Moving the conversion chain on the physical acquisition device means integrating it with circuitry, which raises the following constraints:

- **Low Surface Budget:** the target is extreme portability, adding circuitry on the device should not make the final product cumbersome.
- **Low Power Consumption:** no continuous supply can be guaranteed with these kind of devices. For wireless applications it obviously relies on a battery. For USB Type-

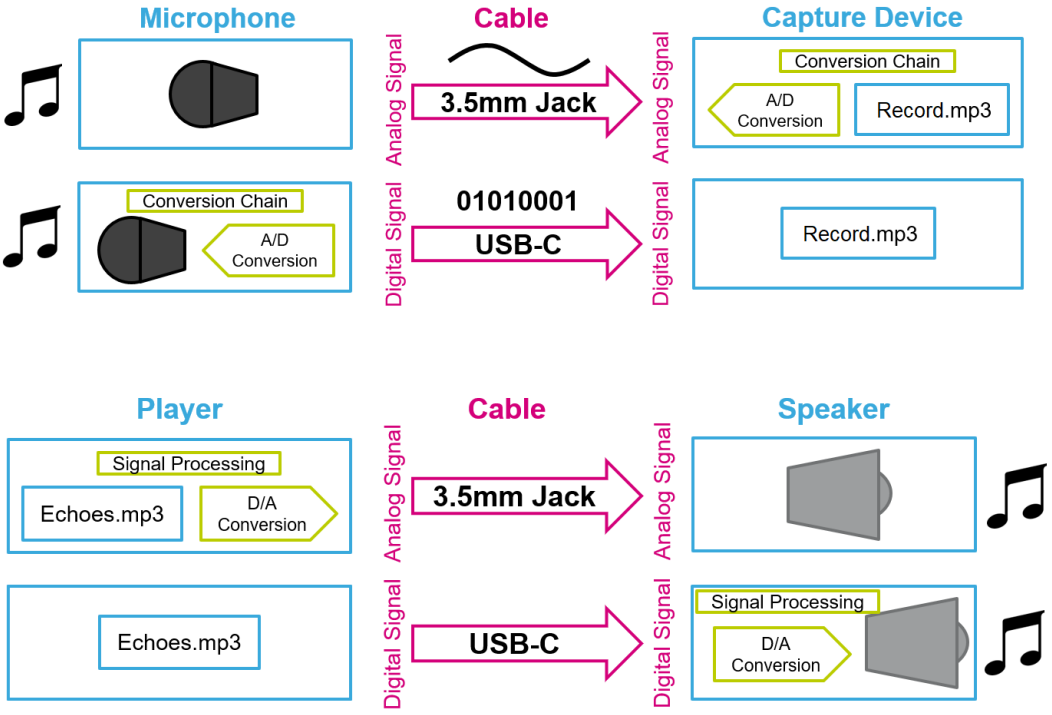

Figure 1.1: Conversion chain concept with an analog or a digital medium while interfacing a microphone (top) or a speaker (bottom).

C, the device is supposed to be possibly plugged in another battery supplied element (such as a laptop) and therefore current consumption is of primary importance as well.

- **Low Production Cost:** these kind of highly portable devices aim to replace those *analog-cabled* ones which can be very cheap to the customer. The price of the final product should not be excessively high, or the risk is not to be attractive with respect of the former and highly appreciated jack cables. This could be a challenge, given all what comes with the new circuitry to include.

This thesis focused on realising an Analog-to-Digital Converter (ADC), designed to take part in the conversion chain for an USB Type-C microphone. This design is also compatible to Wireless and Bluetooth applications.

1.2 Background

There exist many types of ADC, which nature and electrical behaviour make some of them suit a specific task better than others. Before getting started choosing the ADC type that will be used in this work, the application should be investigated: performance requirement define a series of constraints and specifications the ADC has to comply. Of course, a background on ADC types available to attain these objectives is also necessary. These two elements combined can drive towards proper choices.

Figure 1.2 shows this concept under the point of view of two important performance parameters for ADCs: equivalent number of bits (ENOB) and sampling frequency. The ENOB represents the resolution, or accuracy, the ADC can attain, while the sampling frequency is the number of samples per unit of time the ADC can provide as output. It is intuitive that having a converter which is at the same time accurate and fast is attractive, but it depends on the application; it is not always necessary to have both, some application need a very high speed but accuracy can be lower, some others, like audio, requires relatively low sample frequencies. The true performance of an ADC should rather be thought in the

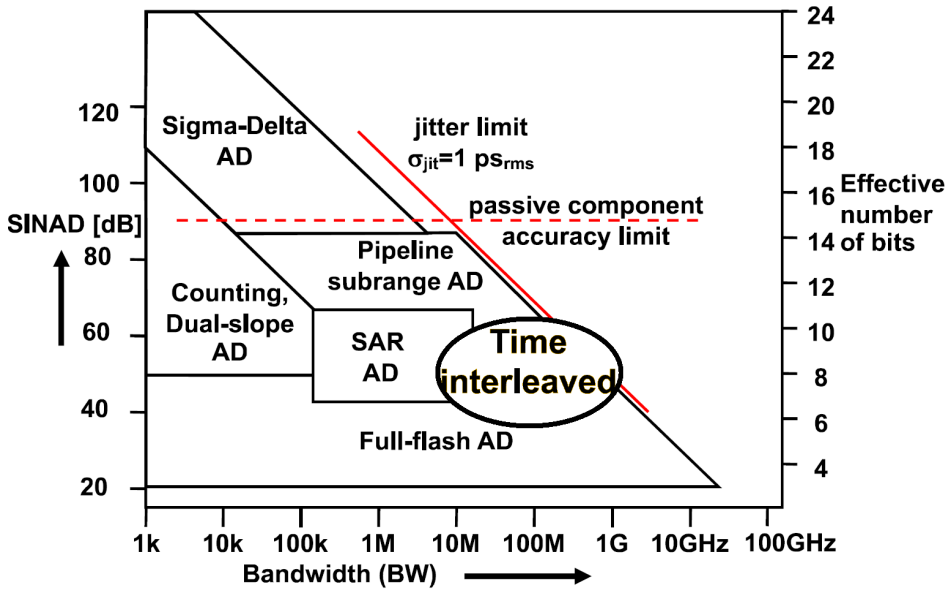

Figure 1.2: Performance trend for different ADC types [1] revealing the existence of *areas of competence* each family is suitable for.

context of the application it is conceived for, more details about the way to evaluate the performance of this work converter will be shown in Ch. 2, Sec. 2.4.2.

About converters themselves, in this section, concepts that are hereby just anticipated will be widely analysed in their own further chapters. Figure 1.2 can be kept as a reference up to Sec. 1.2.4 where the ADC choice for this work will be done and commented.

1.2.1 Audio Signal Processing

The target is converting an audio signal: this identifies a scenario with its own set of parameters to be monitored and performance requirements to be met.

First of all, we define the Dynamic Range (DR): this quantity is expressed in dB and represents the input power range between the weakest convertible signal s, before noise drown it, and the highest S, before distortion due to structure limit.

$$DR = S - s \tag{1.1}$$

The limit S, in the case of an electronic circuit, is nothing but the reference voltage swing, thus S is defined as in the ideal condition where distortion occurs only when there is physically no more *headroom* above the signal. Audio applications impose[1] a DR of 100dB: quality of sound at low input level is very important, especially in high crest-factor case and in the presence of long periods of silence. The crest factor of a wave is defined as follows

$$CF = 20\log_{10}\left(\frac{|v_p|}{v_{RMS}}\right) \tag{1.2}$$

where v_p is the peak amplitude of the wave and v_{RMS} is its RMS value. The minimum value possible is $CF = 1$ (for example, a square wave) and it increases as much as the wave contains a more *impulsive behavior*. If contemporary music is taken as an example, in verses or solos the crest factor is typically between $12 \div 15dB$, while during denser sections like verses with vocals the values will come down to the $9 \div 12dB$. The importance of having 100dB of DR in high crest factor cases can be better visualised thinking about listening to classical music. In this kind of music, there may often be silence during a certain period, with eventually sudden short interventions of musical instruments. It is easy to tell, the

[1] For some more detail see Sec. 1.2.3.

resulting audio wave recorded tend to have a high crest factor. In order to offer a high quality reproduction of these genre of musical acts to the audience, silence is an important aspect to be taken into account and human ear tend to be a quite severe judge.

1.2.2 A-Weighted Filter

Sound is perceived by human ear through the reception and translation of mechanical waves into electrical pulses the brain can decode. The physical information containing sounds is carried by pressure waves and the medium they travel through is the air.

Due to its biological structure, the human ear represents a natural frequency filter for these waves, with a passband from 20Hz up to 20kHz. This is clear from Fig. 1.3, which represents the famous Fletcher-Munson curves, also known as *equal-loudness curves*. Each curve is traced using sinusoidal tones of different loudness and frequency: every combination of these two the human ear perceives as equal in loudness (measured in phons) will lie on the same curve. The filter can be noticed not to be flat in the band of interest, with a gain between roughly 1kHz and 6kHz and attenuation outside this range.

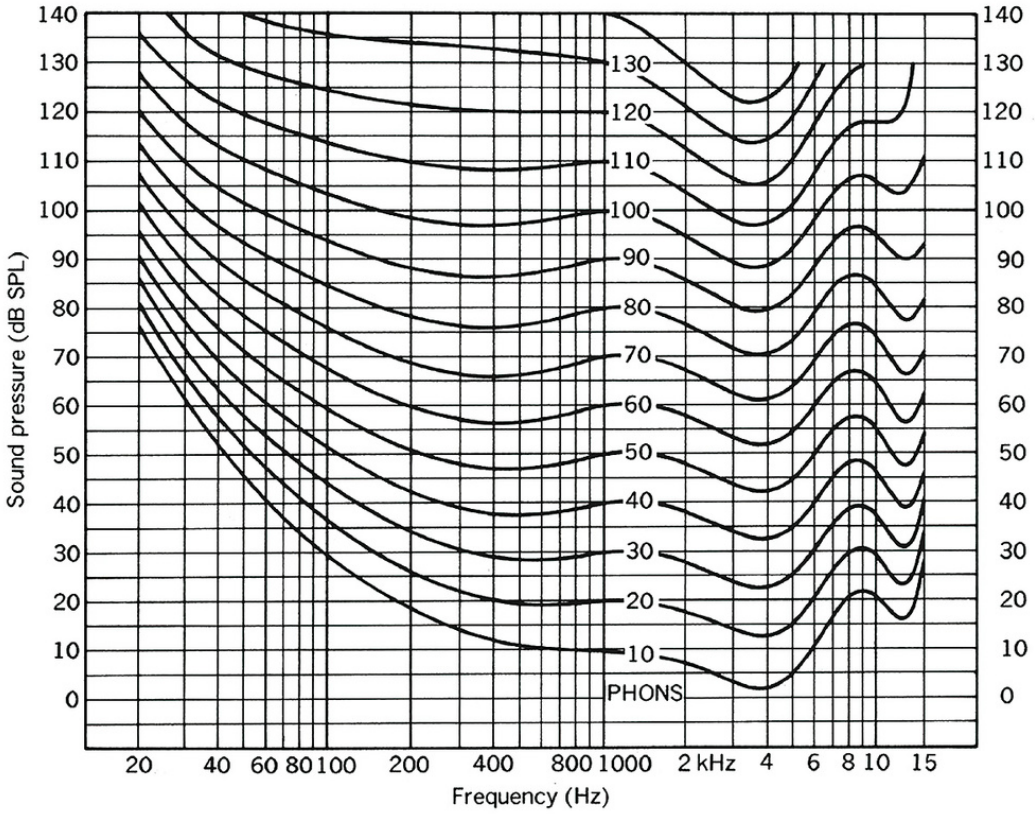

Figure 1.3: Fletcher-Munson Equal Loudness Curve

If capturing an audio signal targets post processing the record, then the "listener" is an electrical device, and data should be accurate with a flat filter in the band of interest. Otherwise, if audio data captured is to be directly listened by an human, a filtering can be done on the output, in order to weight each frequency power contribution. This allows not to overestimate a flat (thermal) noise for example: we know that the human ear significantly attenuates some frequencies which noise is therefore not of our interest. Calculating a Signal-to-Noise Ratio (SNR) of a human-ear-like-weighted output will result in a higher value with respect to a flat output over the same band.

The A-Weighted filter has been proposed in 1936 [2] [3] and the scientific community agree to use this standard when measuring audio performances which are not meant to be

post-processed. It is a fourth-order filter (Eq. 1.3) designed to emulate the $40Phons$ curve.

$$A = 10\log_{10}\left(\frac{K_1 \cdot K_3 \cdot f^8}{(f^2+f_1^2)^2 \cdot (f^2+f_2^2)^2 \cdot (f^2+f_3^2)^2 \cdot (f^2+f_4^2)^2.}\right)$$
$$f_1 = 20.598997Hz \quad f_2 = 107.65256Hz$$
$$f_3 = 737.86223Hz \quad f_4 = 12194.22Hz \tag{1.3}$$
$$K_1 = 2.242881 \cdot 10^{16} \quad K_3 = 1.562339$$

Several other filters exist, notably the ISO 226 standard [4] is becoming widely appreciated due to its more accurate fit with Fletcher-Munson curve. However, the community often find the simplicity of implementation of an A-Weighted filter more attractive than the accuracy benefits in implementing ISO 226 curve, considering the lack of accuracy acceptable.

Publications in audio converters do use A-Weighted values: in this work, unless otherwise specified, SNR values are reported in $dBAw$, meaning data is A-Weighted.

1.2.3 Interfacing Microphones

Entering in the details of the structure and performance of a microphone [5] is beyond the objectives of this work: instead, interfacing with this devices without compromising overall chain performance is the aspect we care about. A short commentary about this topic is in any case appropriate and also helps the reader in visualizing why this aforementioned constraint of $100dB$ least value for Dynamic Range is necessary.

In the table shown in Fig. 1.4, an insight on sounds intensity level is given. The dB_{SPL} unit is defined as the ratio between the measured sound and the Sound Pressure Level (from which the abbreviation SPL) represented by the value of $1\mu Pa_{RMS}$. This value is chosen as a reference for being the lowest $1kHz$ audible tone for human ear. After consulting Fig. 1.4, it emerges that $100dB_{SPL}$ is the range of interest for sound capture and reproduction, being able to distinguish sounds as low as $10 \div 20dB_{SPL}$ while the full-scale range (FSR) would be no higher than $110 \div 120dB_{SPL}$, as it would become dangerous for the ear.

Sound Level [dBSPL]	Examples	Risks
0	Hearing threshold for human ear (1kHz tone)	None
10	Target performance for recording studios and concert halls	
20	Good broadcast studio	
30	Very calm room	
40	Computer	
50	Quiet office, light traffic, refrigerator	
60	Conversational speech at 1m, TV	Upper limit for inexistent ear damage
70	Alarm Clock	
80	Vacuum cleaner	Long term exposure can lead to ear damage
90	Subway	
100	Blender	
110	Chainsaw	Uncomfortable feeling
120	Ambulance siren, rock concert	First level of possible hearing loss
130	Jackhammer	Pain threshold
140	Rock concert (Front row)	
150	Fighter jet engine at 30m	Chest begins to vibrate
160	Rifle shot at 1m	Eardrum burst
170	Howitzer cannon	
180	Rocket launch, Krakatoa explosion at 160km	Muscle tissues immediate damage
190	Sound waves become shock waves	

Figure 1.4: Intensity levels of various common sounds.

The 100dB specification has to apply for ADC dynamic range too, in order to guarantee the proper interface with those good quality microphones which allow sensing sounds in

the range just illustrated. A sound in dB_{SPL} is translated in a voltage through microphone sensitivity, reported in dB_v, and microphone DR is guaranteed by a proper SNR specification for the microphone itself. The DR, in this sense, represents our only concern in designing the ADC since the sensitivity of a microphone will be matched inserting a pre-amplifying stage inbetween: if we defined a full-scale (FS) voltage value for our ADC, then there would be a preamplifier with a gain such as to bring the highest voltage value the microphone would translate to correspond to FS. The two $100dB$ ranges between the highest and the lowest distinguishable sounds are then equalized.

1.2.4 Audio Converters

Audio converters in CMOS technologies are most likely to be implemented using Sigma-Delta Modulators (SDM), that are Oversampled converters, in particular, they are noise shaped. The main reason of this choice is that they are a family of converters capable of attaining a higher Dynamic Range (DR) with respect to Nyquist converters.

Pursuing this performance for Nyquist data converter is limited by matching in elements [6] : technology matching properties for devices impacts on the attainable accuracy. A SDM does not suffer such a limit and can attain 100dB of dynamic range.

Low-Power Audio Converters

Two archetypes of Sigma-Delta Modulators exist: Discrete-Time (DTSDM) and Continuous-Time (CTSDM). In the first category, the loop filter is implemented with Switched-Capacitor (SC) integrators: sampling operations occur in each stage of the modulator, in addition to the quantizer and the feedback DAC. In the second category, the loop filter is implemented with continuous time integrators such as Active-RC ones, continuously integrating charge: the only clocked devices are the quantizer and the feedback DAC.

If we added the keyword "Low-Power" to Audio Converters, indeed the best choice between the two will be a CTSDM. There are several advantages in this way: absence of sampling in integrators operations means that there is no need of a fast settling and this relax bandwidth and slew rate requisites for the operational amplifiers. Sampling operation still exist, but it is at the quantizer input: this allows an implicit antialiasing of the signal thanks to the continuous time loop filter lying in the path, avoiding the necessity of implementing a dedicated anti-aliasing filter at the input of the modulator, which would also be power consuming.

CTSDM are however sensible to jitter noise and to RC product spread. These problematics are different from a DTSDM and have to be addressed in order to take advantage of the lower power consumption of a Continuous-Time architecture.

1.3 Frame, Motivations and Objectives

CENTO is a Switched-Capacitor (SC) Fourth-Order Single-Bit Sigma-Delta modulator developed by STMicroelectronics *Analog, Mixed-Signal, Interfaces & ASIC Design Team*, in *Analog and MEMS Group* (AMG) for audio applications; being personally part of this team for this industrial thesis, it will be referred as *the ST Design Team* for short. This team is responsible of developing mainly front end analog solutions and interfaces for signal processing.

The group and division are now evaluating the possibility to target audio market focusing on low power portable devices such as those featuring USB-C, Bluetooth, WiFi. Such products need to draw as few current as possible and to keep dimensions under control. A Continuous-Time Sigma-Delta ADC is intrinsically less power consuming with respect to a Switched-Capacitor structure, but AMG does not have yet such an ADC in its audio portfolio. This project has been setup to study the feasibility and the advantages brought by using a Continuous-Time Sigma Delta Modulator for portable audio applications.

The main aspects under the point of industrial development are the following.

Since the solution for an audio data converter for portable devices has been already addressed with CENTO, the existing SC Modulator prototype, we agreed that the most efficient and interesting way for ST is to analyse a Continuous-Time conversion of the latter. In this frame, this work would be interesting if it was reporting a step-by-step method to illustrate the process. This would also offer documentation about any aspect a designer should be aware of during the conversion from a DT system to a CT itself. There is no innovation in this aspect, as the conversion from DT to CT of an SDM is a widely known and a lot of publications have been made on this subject: the will is to enrich the expertise of ST with a method that is not mastered at this very moment.

The objective for industrial application is to find the more efficient way to develop a product which will show itself robust for mass production. This implies a strict validation at 6σ of any parameter drift. For an industrial product, the standard temperature range is from -35°C to +125°C, while a $\pm 5\%$ drift in voltage supply (or simply the battery) is taken into account. There are also technological process variations, mismatch and corners behaving the same way, that is, with ranges in which the proper functioning of the circuit has to be guaranteed, but these ranges and specifications are reported in the appendix. In many occasions during the development the possibility to excel in performance has been traded for design simplicity, robustness and specific objectives such as minimizing current consumption. The privilege of a parameter or a performance over one another may change during the design process, in order to comply features with an "industrial" aspects: this concept is a key point to understand design choices made, which sometimes broaden the gap between our performance and state of the art. Details about these choices will be provided throughout this document.

A great part of this PhD research is about the analysis of a weak-point a CTSDM has over a DTSDM: its natural sensitivity to jitter. Also in this case, the objective is an efficient design flow to obtain a robust circuit. Literature offers a wide knowledge about the countermeasures, which help recover from this otherwise preponderant jitter degradation. The criteria used to choose which one is the most suitable for this work will also be explained further.

1.4 Proposed Solution

In this section, a brief overview of the CTSDM which has been realised is presented, to give a preview of what will be discussed in great detail through the whole manuscript.

As stated earlier, since the beginning there was the willing to keep as much as possible the architectural choices used for the former SC modulator: keep a fourth order, keep the same OSR, keep the single bit quantizer, the same coefficients and so on. Therefore, only the possibility of slight modification were assumed at an architectural level.

Of course, all of the latter should have been justified before validation. Some robust and efficient solutions[2] present in the literature demanded a comparison: for example, a certain amount of time was used to compare our solution with a Third Order CTSDM with a 16-level quantizer, which is widely appreciated in audio application. It is already worth mentioning that many features in our solution are appreciated in literature as well, even if with a less wide spread among the scientific community.

The solution proposed will finally reveal to be the starting one, with some differences. The feature we appreciated the most was kept: the quantizer will be a single bit one, which brings a lot of advantages and simplicity design-wise. A desired OSR of 3.072MHz needs a Fourth Order Loop Filter (LF) to recover signal-to-quantization-noise ratio (SQNR). The configuration is Cascade of Integrator with Feed-Back (CIFB) which allows to take advantage of empirical criteria studied in this team then partly explored in this thesis to obtain intrinsic stabilization of the modulator. For what concerns jitter immunity, a FIR-DAC will be placed

[2]References to these works are included in what will be discussed further, therefore they can be found in the proper section and chapter.

in the first stage feedback path[3], sized at 8-taps after all due jitter analysis.

1.5 Innovations

This thesis research brings basically two innovations: hereby they will be briefly introduced, while the details will be shown in the corresponding chapters.

The first one concerns taking into account jitter in simulations. The author has noticed that very few works in literature simulate jitter in a quite accurate way, preferring to show results with simple models such as white or Lorentz distributions or simple piece-wise-defined phase noise (PN) spectra like a lowpass with a single pole. Even fewer notable works have been done to convince the community that the statistical distribution of jitter noise injected in a SDM (even more for a CTSDM) is of fundamental importance. On the same modulator, injecting jitter noise with the same integrated spectral power has totally different outcomes if the distribution is different: for example, if the constant RMS budget has more power at low frequencies and lesser power at high frequency and in another simulation the exact contrary is done, the impact on modulator performance will be totally different.

In this work, jitter has been simulated in a quantitative way, where real PN spectra are used to inject properly distributed noise in the modulator. As a result, modulator performance versus jitter is accurate and there is no risk of overestimation, as it happens with the so appreciated and widespread white model for example.

The second is about stability of a fourth order SDM. Though there are many publications in literature, this topic is quite unexplored. There is no mathematical proof of high-order SDM stability, where by high-order, an order higher than 2 is intended. Some work propose rules or techniques to assure or improve stability, but some rules and results are not clear or it is not clear when can be applied or valid and in some cases there are even refutations of these achievements themselves. There exist instead a lot of methods to recover from instability in those cases when it inevitably occurs. These methods are all more or less abrupt, as they need to detect and intervene while the circuit is providing actual data. In audio application, quality of sound is fundamental and, as commented before, quality of silence is even more. These recovery methods define a time-span while data is corrupted and may generate abrupt sounds[4] which can make the experience of the listener worse: during a moment of silence it can be dramatically noticeable.

A work about stabilizing a fourth order (which was implemented in CENTO) was made by ST Design Team and tested on silicon, with a limited formal analysis. The available knowledge recorded for this method has been applied to this work, supplemented by a deeper formal analysis and allowing us to talk about having designed an intrinsically stable fourth-order SDM. It is the case even undergoing heavily stressing input signals[5]: the modulator can get back to a stable operation when a *normal* signal is injected again and, in any case, *odd-operation* shown by this modulator is the well known SNR saturation, never an instability.

Since stabilization was a secondary task in this thesis, material available is still limited, but with the time that could have been spent, an interesting insight and even more interesting starting points for further related work could be given. It is still to be considered that up to date there does not exist any work in literature that intrinsically stabilize an order higher than 2 with this level of confidence and against such a *violent* set of test signals, neither there exist a mathematical model to build something upon: this is an unexplored and not quite clear topic.

[3] In CENTO a 4-taps FIR-DAC is also present: since it is a DTSDM, this FIR is not meant to immunize the modulator from feedback, but just to relax constraints of the first stage OPAMP.

[4] This could be a sound as the known *click* or *pop*.

[5] Deltas, square waves, near-to-FS DC signals, over-FS amplitude periodic signals and other saturating signals

1.6 Organisation

This thesis work is organised on 6 chapters. The first two are theoretical, the third and fourth analyse behavioral level and the last two are technological and practical. Their titles and topics are as follows:

- 1 - Sigma Delta: basic concepts, theory and state of the art of sigma-delta modulation used for audio purposes are illustrated in this chapter, introducing, whenever it is possible and interesting to do so, some insight over upcoming challenges tied in with this particular work and circuit.
- 2 - Jitter Noise: since this was considered the main challenge and addressing jitter noise took a great part of time budget, an entire chapter is dedicated on this source of degradation, presenting the problem, circuit solutions and important simulation facts which are very interesting to highlight, as well as the accurate simulation method that has been developed to properly monitor jitter impact.
- 3 - Modulator Architecture: describes a phase of high-level considerations about system design of an audio sigma-delta modulator. Features such as architecture, modulator parameters, loop filter coefficients and electrical blocks implementation are here defined, justifying our choices contextualized to the frame we are in. This phase does not include any electrical implementation, but eventually takes into account high-level consequences of subsequent practical implementation.
- 4 - Stabilization Method: the flow of calculations and simulations necessary to empirically guarantee an intrinsic stabilisation for a high-order modulator, a very interesting topic given that there is no mathematical proof for intrinsic stability for sigma-delta modulators of order higher than 2: in this chapter there is a step by step explanation about what this work claims.
- 5 - Transistor Level Design: a second and low-level stage of design, where the challenge lies in practical implementation issues while realising the ensemble of features wanted and described before. The target is reaching a level of circuit robustness and yield suiting a possibly following industrial mass-production for a product.
- 6 - Results: a silicon prototype of this work has been realised in HCMOS9A technology, testchip measurement are presented and commented in this chapter, along with conclusion and purposes for the future.

Particularly long calculations and explanations or complicated figures will be kept aside from main text to find their place in the appendix section, this is done in order to keep the reading flow lighter.

Chapter 2

Sigma Delta Modulators

In this chapter, an overview on Sigma-Delta Modulators will be given, concentrating on the principle and theory of operation. First of all, a brief introduction of the system starting from its most simple description and the main parameters is given: these parameters represent the fundamentals to shape an implementation. The following stage is considering theoretical limits and sources of degradation, as well as leave a comment about the known methods to address these issues. The very implementations of these techniques will rather be carried out in the following chapters, a separation represent the application of all the available information *known a priori* (which is gathered here) to a specific case of design.

A presentation of the state of the art concerning audio applications will follow. It is a very important part preceding the design, integrating the theoretical knowledge with practical works realised about the same application targeted by this thesis. Studying the state of the art provides a lot of information about several techniques and implementations a designer can use to trace a path towards the performance desired. In the specific case of low power audio application, the Continuous Time implementation is preferred to Discrete Time because of intrinsic lower power consumption coming from the very nature of the internal loop filter. This choice makes the modulator vulnerable to jitter and the state of the art offers many solutions to this problem. Since the target of this work is low power consumption, each choice should be justified on the basis of power cost related criteria: the state of the art show important results which give a designer the proof about power consuming of different techniques, allowing to justify choices which may seem under-performing overall, but approach the most our real target.

The content of this chapter is therefore the set of necessary information preliminary to design, including simulation setup for performance verification.

2.1 Sigma Delta Modulators

Sigma-Delta Modulators may be used for analog-to-digital and for digital-to-analog conversion. These devices are based on oversampling and noise shaping. Oversampling Converters differ from Nyquist Converter in the frequency of operation: while Nyquist Converters take their name from the fact they sample at Nyquist frequency, Oversampled Converters take it by sampling at a factor of OSR (standing for Over-Sampling Ratio) of the latter. Oversampling indeed can improve SNR, but the real effectiveness of a Sigma-Delta is shaping quantization noise by the mean of a Loop Filter (LF). This concept will be better explained in Sec. 2.1.2.

Noise shaping allows to reach very high SNR values with respect to Nyquist Converters, for which the use of a Sigma-Delta is widely appreciated in many applications.

2.1.1 Motivations

Nyquist converters have their resolution limited by technological means. The resolution a Nyquist converter is able to reach, whichever architecture or implementation is used, relies

upon matching of elements discriminating the Least Significant Bit (LSB). These are either resistors or capacitors. The matching property available with existing technology makes it really hard to reach a very high number of bits, normally $12 - 14$ bits being already a challenging task since requiring trimming and/or auto-calibrating procedures. A 100dB DR, such as that needed in audio applications, correspond to $\simeq 16.32$ bits of ENOB. In order to obtain this value, the choice of a Nyquist data converter is generally avoided. While it is true that some Nyquist converters attaining 100dB do actually exist, the family of oversampling converters is the first solution to the problem.

Let us make a brief consideration which illustrates well the advantage in doing so. Given a bandwidth, a sinusoidal signal of frequency falling in it and amplitude equal to the ADC full scale, the maximum SNR (SNR_{MAX}) obtainable by a Nyquist converter on this signal is the following:

$$SNR_{MAX} = 6.02 \cdot N + 1.76 \tag{2.1}$$

where N is the number of bits in the converter.

In this case, the sampling frequency is considered as being the minimum necessary to respect the Nyquist criteria for sampling, that is, at least twice the bandwidth. If the sampling frequency becomes OSR times the Nyquist frequency, the maximum SNR is improved this way:

$$SNR_{MAX} = 6.02 \cdot N + 1.76 + 10\log_{10}(OSR) \tag{2.2}$$

Even if a challenging 14 bits was designed and a factor of 128 was taken as the oversampling ratio OSR, the maximum SNR of $107.1dB$ would be attained: this value is just theoretical and still does not take into account system distortion.

A Sigma-Delta Modulator does not suffer of the same technological limits of Nyquist converters and it allows to reach 100dB of DR more efficiently. This is why this modulator suits best our purposes. In the next sections, Sigma-Delta Modulators are presented starting from the overview and then going deeper and deeper into details all along the entire thesis.

2.1.2 Principle of operation

The generic structure of a Sigma-Delta modulator is given in Fig. 2.1. Basically it is a *Nyquist converter* preceded by a Loop Filter, both included in the forward path of a feedback loop. This system is clocked at a frequency f_S which is OSR times the Nyquist frequency, that means

$$f_s = OSR \cdot f_{Nyquist} = 2 \cdot OSR \cdot f_B \tag{2.3}$$

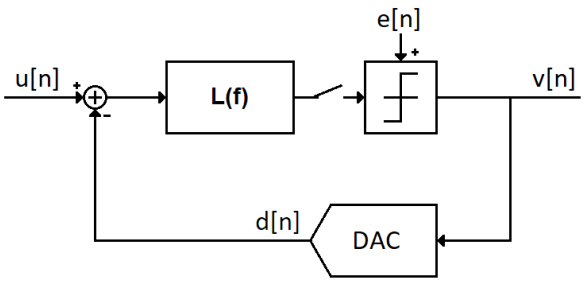

Figure 2.1: Basic Sigma-Delta block diagram.

The main problem of Nyquist converters, as introduced so far, is that the quantization noise has a lower limit, due to the maximum accuracy between circuit elements that can be obtained with the technology available today. The concept lying behind Sigma-Delta

Modulators is the possibility of shaping this quantization noise using a filter, but preserving the signal. In Fig. 2.1 it can be seen that the input signal $u[n]$ and the quantization noise $e[n]$ are injected in the system in two different places, which means that their transfer functions through the output will be different. The algebra of this system is often solved in the frequency domain, where the signals $u[n]$, $e[n]$ and $v[n]$ are represented by their frequency domain dual $U(z)$, $E(z)$ and $V(z)$. Some very trivial algebraic passages, rearrangements and redefinitions, bring to express V(z) as a combination of the signal U(z) and the noise E(z).

$$V(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \tag{2.4}$$

where, in fact, a Signal Transfer Function (STF) and a Noise Transfer Function can be highlighted. They have the following relation with the Loop Filter transfer function which will be called LF(z)

$$STF(z) = \frac{LF(z)}{1 + LF(z)} \simeq 1 \tag{2.5}$$

$$NTF(z) = \frac{1}{1 + LF(z)} \simeq \frac{1}{LF(z)} \tag{2.6}$$

The loop filter is an element with a very high gain in the band of interest, from which the approximation after the symbol $\simeq$ hold. To satisfy these requirements, the loop filter is usually composed of integrators with time constants and summing coefficients which composes the so-called modulator coefficients as shown in Fig. 2.2. Coefficients totally characterise the transfer functions NTF and STF at a behavioral level, which allows to easily work on preliminary SDM structure before design. All the quantization noise being shaped out of

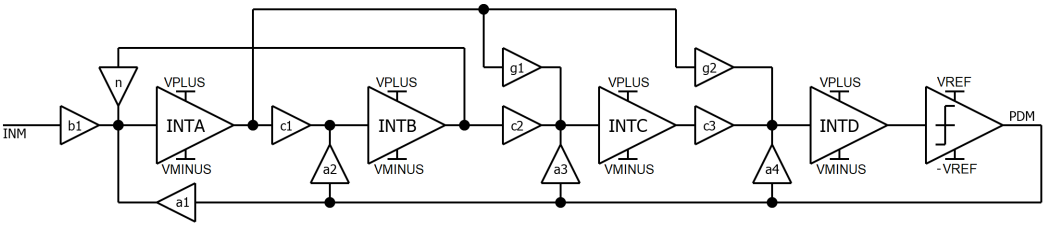

Figure 2.2: The diagram showing layout and coefficients for this work is taken as example of design scheme.

band will be of course filtered by a decimation filter afterwards. The term "decimation filter" reunite a SINC and a FIR filter, which are put in cascade and are always present at the output of any SDM. This is beyond the objective of this work which is limited to the modulator itself, but considerations about it will be eventually drawn to justify some choices.

This previous paragraph, however, highlighted the drawback of using an oversampled converter: while Nyquist converter have a 1-to-1 correspondence between input and output at step [n], SDM need to reconstruct the information through several samples, by the mean of the decimation filter.

Being an electronical circuit, of course performance degradation will be given by non-idealities and practical realisation (see further). In any case, at this moment the designer has to take an architectural choice: which shall be the oversampling frequency? The loop filter order? Shall a single bit quantizer be used or a multibit one? This will be considered in the following section.

2.1.3 Main Sizing Parameters

At this behavioral level, the parameters determining performance of the system are three: Oversampling Ratio (OSR), Loop Filter Order (L) and the Number of Bits in the Quantizer (b).

Assumptions and calculations which bring to the expression of SNR_{MAX} with respect to these parameters can be easily found in the literature [6]. It can just be stated at this point that, everything that is going to be explained further on in this work respect all the said assumptions[1]. It is just worth mentioning, among the latter, the following discussion before continuing: one of the important approximations is about stating that the error E(z) and the signal U(z) are uncorrelated. Though of course it is not the case, as each internal quantizer input voltage is determined[2], it is interesting to consider that instead, this voltage covers all the values corresponding to a quantizer output with a constant distribution. This can be done due to the fact that the system is oversampled: if the OSR is sufficiently high (>64) the error sequence can be assumed to be varying *fast* and randomly with respect to the signal, thus decorrelating the two. This allows to assume that E(z) does have a spectre

$$S_e(f) = \frac{\Delta^2}{12 f_s} \tag{2.7}$$

where Δ is the quantizer step (see further in Sec. 2.1.6) and f_s the oversampling frequency. All of this is what allows to finally evaluate SNR_{MAX}, but before to give this results, the next three sections will be presenting the as many main sizing parameters mentioned characterizing the SDM.

2.1.4 Filter Order

The benefits of cascading integrator stages within the internal Loop Filter of an SDM were analyzed for the first time in [7] by Candy, proposing the use of a second order, L = 2. The principle, in general, is the following: recalling Eq. 2.5 and 2.6, it is clear that the NTF will reject as much more inband quantization noise as the order of the filter increases. The theoretical NTF which are obtained varying the discrete L value may be found in Tab. 2.1: higher orders trade inband noise reduction for a rapidly growing out-of-band gain (OBG).

Order	NTF	Gain at $f_S/2$	$\|\|h\|\|_2^2 - 1$
1	$(1 - z^{-1})$	2	1
2	$(1 - z^{-1})^2$	4	5
3	$(1 - z^{-1})^3$	8	19
4	$(1 - z^{-1})^4$	16	69

Table 2.1: Theoretical Order-related characteristics for a SDM.

Figure 2.3 plots exactly these transfer functions contained in Tab. 2.1, once OSR and the number of bit in the quantizer has been fixed. It will be seen that the out of band behaviour of these noise transfer functions (NTF) will affect the performance, but under the point of view of inband quantization noise, the significant part of Fig. 2.3 lies just in the frequencies at the left of the grey line representing the baseband. The action of Oversampling combined with a more and more aggressive noise shaping order is clear in the band of interest.

Willing to contextualize as soon as possible also theoretical matters to our scenario, the out of band gain can be a serious issue while addressing the jitter noise problem: the higher the OBG, the higher the jitter noise contribution in our system. This will be seen in detail in Ch. 3.

Another fundamental problem with increasing filter order is instability. While first and second order SDM are respectively intrinsically and conditionally stable, there is no mathematical proof of a stability criterion for modulators of order higher than two. They are instead very vulnerable structures, which tend to never recover from an instability condition when they meet one. This issue is of primary importance because, it is not about performance degradation, it is really a matter of total malfunction: a SDM of Order 3 or higher that eventually falls into a state of instability, will never show data reflecting the input signal. It is then mandatory to properly study instability for the desired modulator, using a

[1] This is done to keep the reading smoother and the discussion focused on the design flow.
[2] Quantization noise in Sigma-Delta Modulator as mathematical system is completely deterministic.

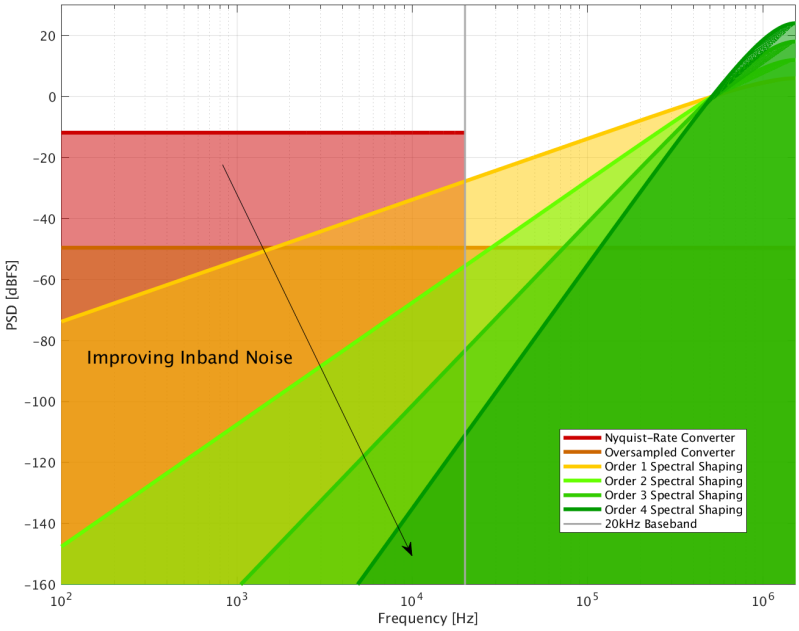

Figure 2.3: Comparison between inband noise for different kind of ADCs.

stabilisation method, being it a prevention or a recovery. All possible details about stability analysis and stabilization methods will be carried out in Ch. 5.

If all the issues are properly addressed or can be tolerated, modulator order is a powerful way to exploit OSR, as L contributes as the exponential of OSR itself. Each stage adds also a cost in power consumption, but it becomes lesser and lesser with order growth: in our case, since it will be shown that fourth order loop filter will be chosen, the fourth stage represents about the 10% of the total current consumption budget of the analog modulator.

2.1.5 Oversampling Ratio

Given a band of interest, Oversampling Ratio is defined as the multiple between the associated Nyquist frequency and the frequency the modulator is actually clocked. Referring to Eq. 2.10, OSR is very interesting, as already introduced in the last section, as it is raised to the power of $2L+1$ which makes the combination of these two rather powerful. Though already been discussing about limits for parameter L, if we looked at the system how is described so far, there is theoretically no fundamental inconvenient in taking very high OSR. System transfer functions are normalized such as the unit circle in the z domain is f_s. The key difference is at which normalized frequency the baseband will correspond and thus at which frequency the following decimation filter will be cutting off shaped noise.

The design strategy for OSR therefore lies in practical implementation and cost, as faster operation mean faster amplifiers, faster comparator, faster decimation filter. All of this should be checked for feasibility and power consumption.

Of course, once non-idealities are added, situation changes and another comment which must be made is, as seen in Sec. 2.1.4, that the OBG would be covering a wider spectrum if OSR increased: this would mean a higher integrated out of band noise value, which would be worse for jitter. This concept as well will be clear in Ch. 3.

2.1.6 Internal Quantizer Number of Bits

Let us first resume, using Fig. 2.4, the definition of the quantizer as a mathematical operation.

If we call y the input and v the output of a quantizer, the transfer function of this

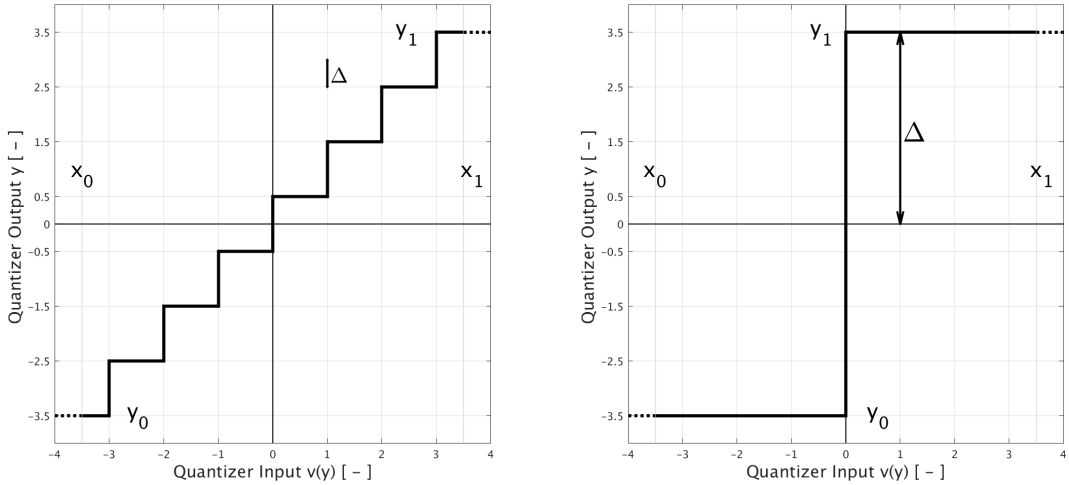

Figure 2.4: Example of an 8-level (3-bit) mid-step quantizer (left) and 2-level (1-bit) quantizer (right) transfer functions with quantization step Δ.

mid-step quantizer[3] is

$$v(y) = v_0 + \Delta \cdot \left\lfloor \frac{1}{2} + \frac{y - y_0}{2\Delta} \right\rfloor \tag{2.8}$$

Where v_0 is the lowest output the quantizer can represent, y_0 is the lowest input it can receive and $\lfloor \cdot \rfloor$ denotes the *floor function* which rounds a real number to its previous natural number. For the parameter Δ, one may choose to refer to Δ itself or to 2Δ. Using Δ means to think about the maximum error that can made while representing a continuous range of values with a discrete set of values. Using 2Δ, also denoted as LSB, we refer to the resolution of the quantizer (more generally of an ADC), that is, the smallest step between signals the quantizer can distinguish.

In practical implementation, both input y and output v are bounded between two values, one is of course the lower bounds just defined as y_0 (corresponding to v_0), while the upper bounds can be defined as $y_1 > y_0$ (corresponding to $v_1 > v_0$). The quantity $y_1 - y_0$ is called Full Scale Range (FS or FSR). A quantizer (or Nyquist ADC) is said to have b bits of resolution if the following holds

$$2^b - 1 = \frac{FS}{2\Delta} \tag{2.9}$$

In the example of Fig. 2.4, for the plot on the left $y_0 = v_0 = -3.5$, $y_1 = v_1 = 3.5$, $\Delta = 0.5$ and consequently $FS = 7$ meaning that this quantizer has 3 bits of resolution as Eq. 2.9 holds for $b = 3$. On the right plot, the same holds but $\Delta = 3.5$, so the quantizer is a single-bit as Eq. 2.9 holds for $b = 1$.

As introduced earlier, a quantizer is nothing more than a Nyquist ADC, thus it can be realised in any Nyquist ADC structure existing. The limits are also inherited, which means that tre parameter b is technically limited to about $12 \div 14$. It should however be noticed that the phylosophy of building a SDM is to shape the noise of a possibly low resolution quantizer. This being said, the inheritance from Nyquist converters is exactly the same when it comes to SQNR: the SNR is $6dB$ better[4] per bit in the internal quantizer. From the spectral point of view, the entire spectrum[5] is *shifted down* by $6dB$ per bit in the quantizer, also improving the scenario with respect to OBG.

Multibit choice is solid, widely studied and appreciated by designers, especially for continuous time application: increasing the number of quantizer levels has an important impact

[3]There exist mid-step and mid-thread quantizer. In this work a mid-step is used so it is the one which will be explained.

[4]Except from $b = 1$ to $b = 2$ for which the improvement is $9dB$.

[5]Signal of course excluded.

on jitter (the $6dB$ OBG downshift per bit will be at the base of quantizer jitter influence), to which Ch. 3 will again address. It can now be concluded that all the three main parameters for performance actually appear also as contributors to the modulator jitter performance.

The downsides of having a multi-bit over a single-bit is a matter of non-ideality, thus it will be explained in the following section.

2.1.7 Signal-to-Noise Ratio in SDM

As introduced in Sec. 2.1.3, an expression for the $\mathrm{SNR_{MAX}}$ can be calculated and it is reported in Eq. 2.10, for a sinewave input signal

$$SNR_{MAX} = \left(\frac{3 \cdot (2^b - 1) \cdot (2L + 1) \cdot OSR^{(2L+1)}}{\pi^{2L}} \right) \tag{2.10}$$

A graphical representation of it is also proposed in Fig. 2.5, where it can easily be told which combination of OSR and Loop Filter Order is above the 100dB plane intersection, that is, which of those combination are eligible to address our task. The designer is here

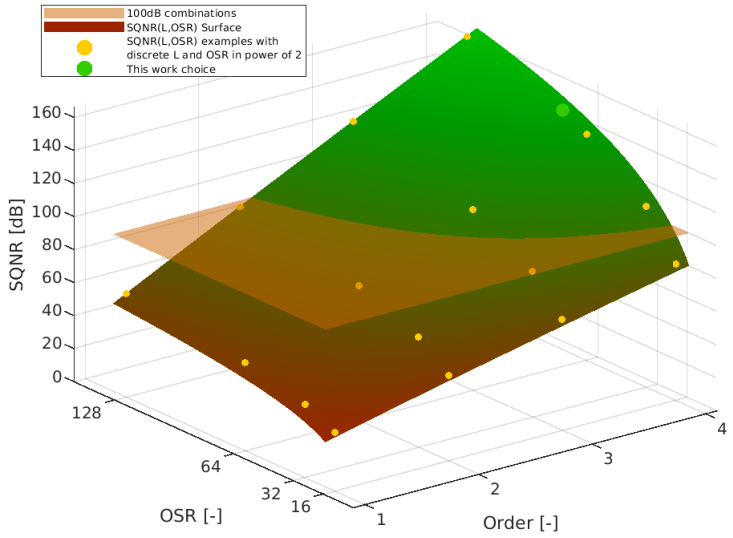

Figure 2.5: $SQNR(L, OSR)$ surface for a single-bit quantizer SDM with an input sinusoidal signal at Full-Scale. A 100dB constant surface is also shown, which represents our inferior-limit. Our work is also included in order to have a reference.

completely free to choose the path to walk by, being aware that each combination comes with its own challenge and non idealities.

A last general remark about non-idealities, before getting into details, is about the fact that this formula is a guideline which helps the designers to visualize how to combine the three fundamental parameters OSR, b and L. It is worth spending a word about the following: the scientific community agree on the good practice of designing an oversampled converter taking into account about $10 \div 15dB$ margin on the theoretical maximum SNR, in order to let quantification noise to be quite far from being the dominant noise source in the circuit. This, however, is intended to be based on simulations and not calculations resulting from Eq. 2.10. Let us take as an example this project architecture, for which the number of bits in the internal quantizer b=1, the Loop Filter Order L=4 and OSR=76.8: this results in $\mathrm{SNR_{MAX}} = 142.7$dB: this theoretical value is far from even the simplest behavioral simulation[6] of a full-scale sinusoidal input. Consequently, with respect to the 10÷15dB margin, the choice made at this step would not represent a $42.7dB$ of over-design, as only simulations can show the actual margin.

[6] In MATLAB/Simulink behavioral simulations without any non-ideality, SNR_{MAX} is around $120dB$

2.2 Non-idealities

Several non-idealities affect the performance of a SDM. They can either be due to imperfections in meeting the previously made assumptions or to physical implementation of the system. Their ensemble introduce new trade-offs in the calculation of sizing parameters.

Non-idealities represent a wide topic and this is why the ones presented in detail in this section have been selected among those which during the development of the SDM presented in this work, needed to be addressed more carefully than others. It is also worth commenting, alongside their presentation, about the way these non-idealities impact the modulator both in Discrete-Time and Continuous-Time case.

2.2.1 Real Amplifiers

A real amplifier introduces a lot of non-idealities in the integrators. Those which are concerning for a SDM are finite bandwidth (or more precisely finite gain-bandwidth (GBW)), finite open-loop gain (A_{ol}), finite slew-rate (SR), output current limit and differential offset, the last one being particularly important just about the first integrator. Calculations and design margins about these parameters are commented in literature [6] [8] [9] [10] and are quite straightforward: in order to visualize them, they are presented along this section briefly.

Finite GBW causes integrator gain errors and feedback loop delay, especially in CTSDM. It is normally desired to design Operational Amplifiears (OPA) to have GBW at least 10 times the oversampling frequency f_s of the modulator. It is also possible to compensate finite GBW by rearranging modulator coefficients [11]. While this may not be very effective if the previous margin on GBW is taken, it could really improve a situation where this value is kept even lower than f_S.

Open-loop gain (A_{ol}) is a finite quantity and causes the DC poles of the integrators to spread at higher frequency, leading to integrator gain errors. It has been proven, however, that in some cases, A_{ol} can be as low as OSR with acceptable degradation. This situation represents a behavioral aspect: usually designers choose much higher values, for a reason that will be explained in Ch. 6, Sec. 6.4.

Finite slew-rate of an amplifier causes not the the output nodes of the corresponding integrator, which carry the state information, to settle properly. This of course corrupts the integral for that given stage. It can be found [9] that SNR degradation begins to show up whenever, for any integrator n of the n-th stage, the following is not met

$$SR_n > 1.1\frac{2\Delta}{T_s}a_n \tag{2.11}$$

where 2Δ is still the feedback-DAC voltage step, and a_n is the feedback coefficient of stage n. Only the a_n coefficients are taken into account as they represent the steepest signal possible (a voltage step). This modifies what can be found in [9]: in Eq. 2.11, also non-unitary feedback coefficients due to scaling is taken into account.

Limited output current of the OPA can corrupt the output voltage of an integrator as well. The output stage of every OPA should be able to supply enough current to satisfy current calls from the output node, up to at least the SNR_{MAX} point. The maximum current the amplifier has to provide should be calculated beforehand.

Differential Offset in an OPA is caused by mismatch of the input pair transistors. The existence of a Differential Offset translates in the presence of a DC component in the loop injected at the input of an integrator. While the following stages are in a gain system and their contribution is mitigated, if the first stage shows a Differential Offset, the DC component generated at this point in the loop will be necessarily visible in the output spectrum as an idle tone [6] at the frequency

$$f_{\text{idle}} = f_s \frac{V_{OS}}{V_{FS}} \qquad for \qquad V_{OS} << V_{FS} \tag{2.12}$$

where V_{FS} is the FS-Range and V_{OS} is the differential offset voltage. With common implementation values, it can be often found that f_{idle} falls in the band of interest: an undesired tone is not comfortable for human ear and should therefore be avoided. More details about differential offset and its necessary countermeasure will be carried out in Ch. 6, Sec. 6.4, within an illustration of the whole design strategy for OPA, taking into account this section issues to be addressed, will be presented as well.

2.2.2 Coefficient Drift

Another very important issue in CTSDM, is RC Product Spread. In a CTSDM, synthesizing a coefficient K involves the product of the values of the feedback capacitor C_K and an input resistor R_K as follows:

$$K = \frac{1}{R_K \cdot C_K \cdot f_s} \tag{2.13}$$

Process variation cause independent drift on the two which may drift in any reciprocal direction. This topic will be part of Ch. 6, where in Tab. 6.2 these technology parameters of HCMOS9A are reported. As for now, it is just important to be aware that a worst case of 20% for resistors and 15% for capacitors can be found to be expected, at 6σ. A design at 6σ will therefore need a RC product compensation up to 35%. Since coefficient univocally define the NTF of a modulator, of course a drift in their values will make it change, as Fig. 2.6 shows. Any NTF is designed to have a certain inband-gain and it is normalized

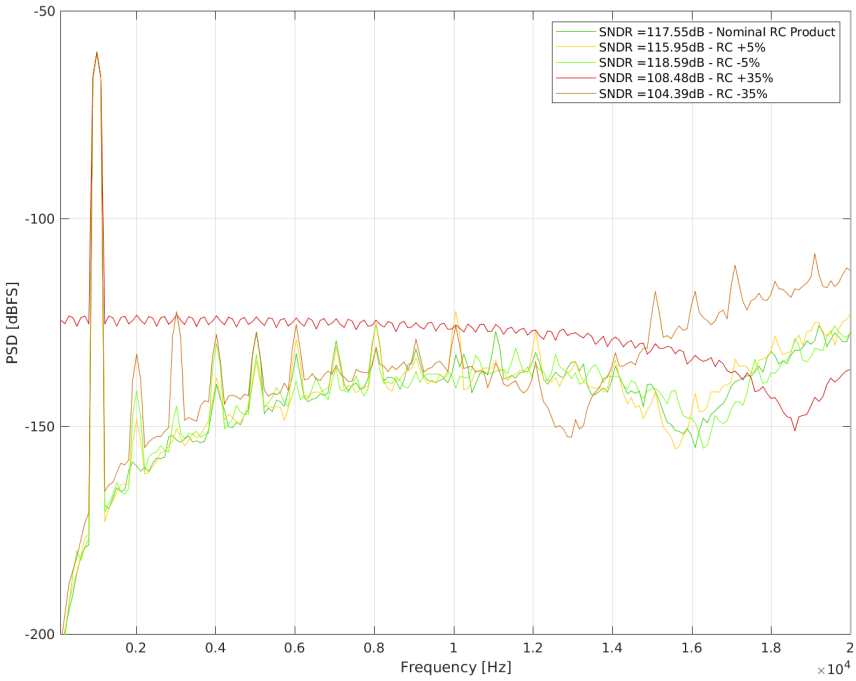

Figure 2.6: Theoretical RC Product drift, simulated at behavioral level. All coefficients have been rescaled by the corresponding percentage reported in the legend. *Up* and *down* HCMOS9A technology spread worst case show a remarkable SNR and spectrum degradation. 5% drifts are also reported to show that a margin of tolerance exist.

to f_s: once both resistor and capacitor drift is given, the overall drift will be the same for all the coefficients, which means that the NTF realised is now as it was normalized for a different f_s, as Eq. 2.13 states clearly.

Specifically, if all the coefficients values go down, the NTF is optimized for a lower f_s, which means that a part of the shaping slope falls in-band while it should not. The in-band integrated noise is now higher and the SNDR drops. If they go up, SNR improves at low input signal level, but at high level the integration constants have a higher ratio, which means a earlier saturation. In each case, there will be a tolerance range: this will define the RC spreads which cause limited or tolerable degradation.

The RC Product spread will be carried out specifically in Ch. 6, Sec. 6.6.

2.2.3 Quantizer

A quantizer is nothing but a Nyquist ADC, thus all of the knowledge about features and parameters which determine the performance of the latter can be inherited to set up the former. This is important at the point where the practical implementation is realised and a series of non-idealities are introduced.

Let us present as an example, for simplicity, a multi-bit quantizer circuit implemented with a flash ADC, whose structure is shown in Fig. 2.7. This circuit synthesize the transfer function in Fig. 2.4 (on the left). It is implemented by $2^b - 1$ comparators (in this specific case having b=3), each one of them comparing the input with a different *reference*, realised with a resistor voltage ladder. The latter corresponds to each *mid-step* in the the transfer function of Fig. 2.4 (on the left) and the values are $0, \pm 1, \pm 2, \pm 3$.

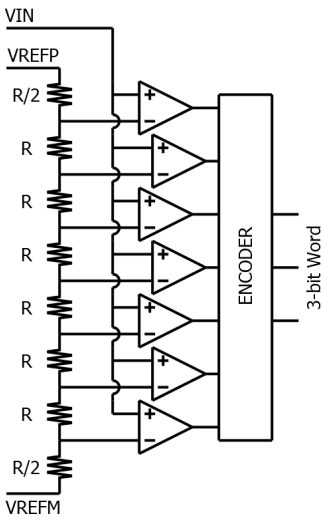

Figure 2.7: A flash 8-level (3-bit) ADC is used as a quantizer.

In a SDM, the quantizer is always paired with a feedback DAC, with matching number of bits. It translates the digital sample back to analog in order to be injected in the loop filter via feedback paths.

If we introduce element mismatch in quantizer and DAC, their transfer function becomes non-linear, as the mid-treads just seen shift from nominal values. This non-linearity is included in the loop, but for the quantizer its injection point is the same as the quantification error, while for the DAC it is not. This is why the first is noise shaped while the second appears in the spectrum, introducing a severe level of distortion. Since a loop structure is involved, mismatch between elements has not the same behavior as in Nyquist converters (as seen in Sec. 2.1.1): the degradation is not tolerable even with just 3 levels[7]. The employment of a countermeasure is mandatory: the most widely spread is Dynamic Element Matching (DEM) [12]. Since its implementation is not trivial, it has been decided to totally keep its explanation out of the purpose of this thesis, leaving the very interesting reference, a work by professor Ian Galton, that has just been cited. Some considerations about the costs it

[7]Formally, the first "multi-bit" one can create.

represents for the design will be analyzed in the chapters to come, referring to it just as a non-linearity recovery method for now.

At this point it can be already noticed that in the particular case when b = 1, that is, a single bit quantizer, none of the above apply: using a single comparator indeed implies having a higher Δ (Sec. 2.1.6) but since it is implemented by a single comparator, no linearity issues are met.

2.2.4 Jitter

Jitter is a non-ideality of the clock signal. Since this is a major issue in CTSDM such as this work, an entire chapter is dedicated to this non-ideality and to the techniques used to address it. At this level, I will give just a brief introduction of the topic, just to help the reader visualize some issues presented before Ch. 3.

Clock signal is provided by a dedicated circuit, which of course has its non-idealities and noise characteristics. This cause the clock to drift from a perfect "square-wave", the wave period T_s not being constant, but shifted[8] at every clock-tick by a certain time-value. Since

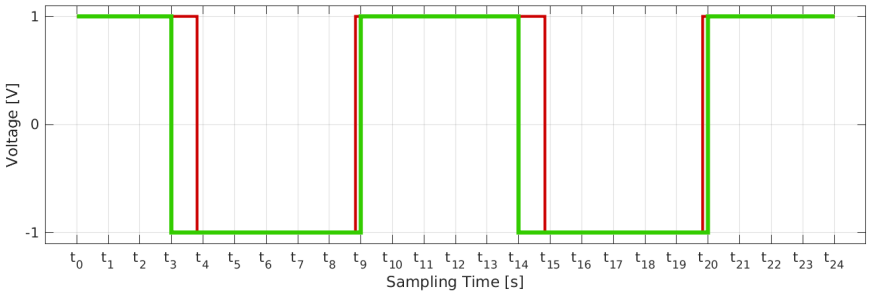

Figure 2.8: An ideal clock (green) and an exemple of the same clock affected by jitter noise (red).

in continuous time internal LF stages integrate over the whole period, a shorter/longer period will affect the feedback DAC waveform, integrating too few/too much charge respectively. The error can be calculating using Eq. 2.14.

$$\Delta Q[n] = \frac{(VREFP - VREFM) \cdot j[n]}{R_{DAC} \cdot (2^b - 1)} \tag{2.14}$$

Where $\Delta Q[n]$ is the charge error, during the n-th clock cycle, and R_{DAC} the resistance of the DAC, $j[n]$ is the timing-jitter (time-shift) from T_s at the n-th clock cycle, b is the number of bits in the quantizer. This error can dramatically reduce the overall SNR of a CTSDM, with a predominant contribution of Signal-to-Jitter-Noise Ratio (SJNR), thus needing absolute countermeasures to be used.

2.2.5 Excess Loop Delay and Quantizer Metastability

Whatever is the architecture chosen for the quantizer, comparators would always be present. When a real comparator is implemented, a delay between the sampling clock signal and the actual instant when the comparator resolves the input exist. In a CTSDM, as already seen in Sec. 2.2.4 the sample is determined by the integration during the whole period. Thus, if in the feedback pulse, that is, the waveform generated by the DAC since the commutation instant, a delay exists with respect to the rest of the paths in the LF, then the integral is corrupted.

The compensation known from textbooks is, once the delay t_c is known, to clock the DAC with $t_d \geq t_c$ and then basically compensate the proper LF coefficients. This compensation

[8] The time-shift definitions and properties will also be covered in Ch. 3.

is a scaling of the standard coefficients by a certain different polynomial in t_d for each of the coefficients.

To add a detail, actually there exist also another phenomenon concerning comparators decision and this is what is called Quantizer Metastability: the time needed for the comparator to resolve its input is not actually a fixed amount of time t_c, but it depends on the input magnitude. High input magnitude are faster to resolve, since most comparators scan their input with a differential pair. If this issue is not adressed, the statistical distribution of t_c can have an effect like jitter: an error proportional to ΔQ as in Eq. 2.14 would be committed, where $j[n]$ has to be substituted by $t_c[n] - t_d$. A solution is to simply choose beforehand a higher t_d such as a reasonable amount of statistical distribution is covered, with all consequent coefficient renormalization.

2.2.6 Thermal Noise

As in any circuit, thermal noise also makes its contribution in the SNR calculation. Amplifiers are always present to build the loop filter and while last stages are mitigated by being further elements of a *gain chain*[9], the first stage is quite important for thermal budget. Modulator coefficients are synthesized with sampled capacitors in DT, where resistor switch introduces 4kTR which aliases in kT/C noise, and with resistor with their $4kTR$ in CT.

The result of amplifiers and resistors (or switched capacitors) thermal noise combined is an inband flat and constant[10] noise floor, determined by sizing of all of these elements, and it can be visualized in Fig. 2.9 showing the comparison of the modulator simulated with and without it.

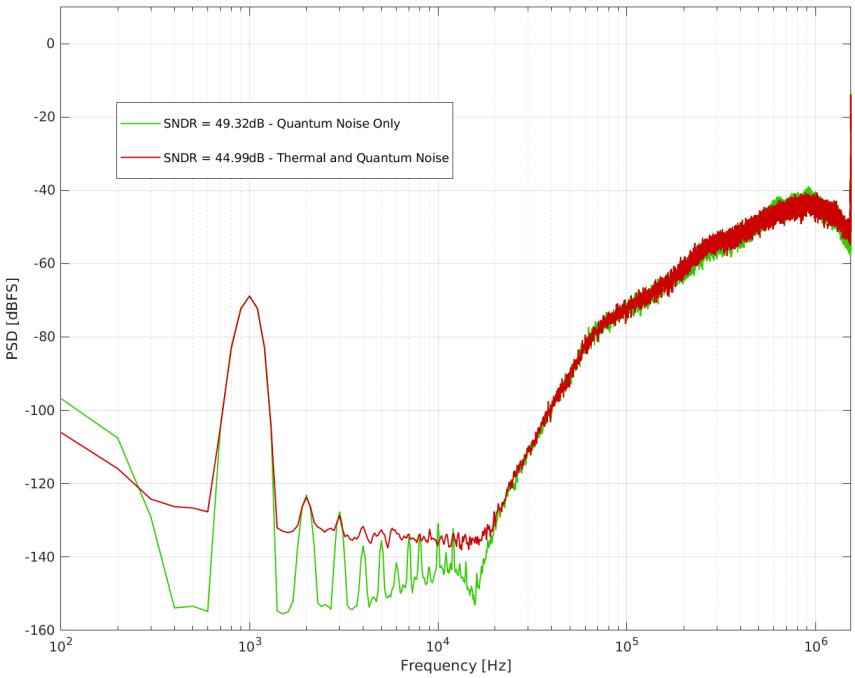

Figure 2.9: Two spectra in comparison, with and without Thermal Noise with the standard $1kHz$ $-60dBFS$ sinus input signal, simulations are electrical with ideal devices but amplifiers are real (transistor-implemented) and resistors do have a thermal noise model. Notice the Hanning 7-points window, for which the signal peak is about $7.5dB$ less than $-60dBFS$, as well as distortion and DC components showing up when changing from behavioral to electrical simulations.

[9] According to Friis formula for cascades of gain stages.
[10] With respect to input signal power.

2.2.7 Noise budget

The total input referred noise N of the modulator will depend on the quadratic sum of all the contributions, the same way the Signal-to-Noise Ratio will be expressed as:

$$N^2 = \sum_i N_i^2 = QN^2 + JN^2 + TN^2 + ... \tag{2.15}$$

Where "..." represents other "minor" sources of noise and degradation, as the most important and dominant contributions are Quantification Noise (QN), Jitter Noise (JN) and Thermal Noise (TN). Their signal to noise counterparts SQNR, SJNR and STNR can be used as well to compare performance.

The most popular procedure [13] is to let Thermal noise to be the dominant part of the sum. This is because there is likely a linear factor of 1 between integrated inband thermal noise and current consumption, whereas the reduction techniques for other major noise contribution in a SDM are more power efficient. To make an example: let us imagine a CTSDM modulator in which only loop filter resistors for coefficients synthesis are noisy: if an improvement of a factor of two in thermal noise is desired, this means that resistors should be halved and current flowing through them doubled. If gaining a factor of two on quantum noise was necessary, b, L, OSR or a combination of the three could be used and power consumption costs is generally lower in comparison, unless the performance had already been pushed far. Another way to improve quantization noise is to change the NTF, making it more aggressive: this choice can provide an improvement factor of 2 without affecting power consumption at all, the challenge would probably lie in realisation and stabilisation of such transfer function. All the latter arguments justify the $10 \div 15dB$ margin seen in Sec. 2.1.1 between target and behavioral simulation DR. Tt would be sufficient the target and the quantification noise floor for thermal noise to dominate, even if it is clear that it should be as *safely* close as possible to the target for power efficiency.

2.3 Simulating Sigma-Delta Modulators

The design of a Sigma-Delta requires extensive simulations to validate the choices. It could be at behavioral level, transistor level and Post-Layout Simulations (PLS). The wide mathematical backup literature about SDM available serves as a valuable guideline, but can not substitute even the most simple simulation. The opposite is also true: simulations should not be used without a theoretical backup and using simulations such as in a continuous trial and error attitude to completely drive design choice is a strategy that should be avoided. The best approach, in general, is to master a circuit and its characteristic from a theoretical point of view, then descending with complexity level towards the real electrical implementation, validating assumptions, design choice and sizing with simulations.

More specifically, the necessity of simulations since the highest level of description of Sigma-Delta Modulators is due to the fact that they are non-linear systems and also actually signal-dependent. All existing mathematical models are instead linearised and signal-independent. Simulations show the actual behavior of a SDM as they let the internal states evolve in time.

Graphically representing data is fundamental to the work of the designer, who needs to monitor several parameters. We are now showing in the upcoming sections the two kind of data which are the most consulted to evaluate this work performance and how they are represented.

2.3.1 Spectrum

A transient simulation is performed and a FFT is calculated [8] on the output bitstream of the modulator. Figure 2.10 shows an example taken from a behavioral simulation of our modulator. From this graphic, many informations can be told. Whenever a spectrum drifts from what we expect we may recognise typical symptoms which guide the designer to investigate in a certain direction. This is often the case while more and more accurate

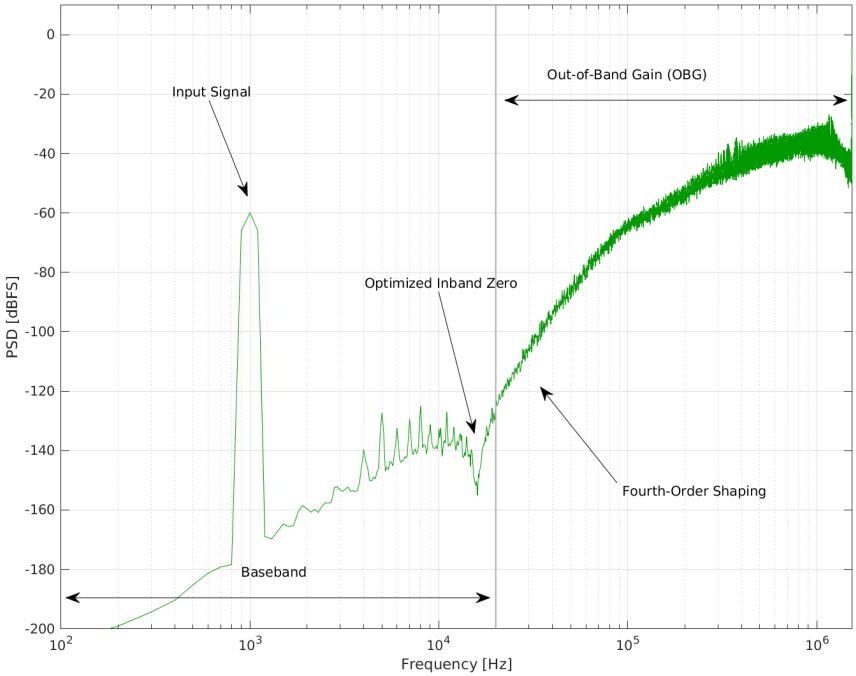

Figure 2.10: An example of spectrum for our 4th order SDM obtained by a behavioral MATLAB/Simulink simulation.

models are used. A clever method is, in fact, changing blocks from high level to low level one at a time, verifying that no mistakes were made. For example: let us imagine to be in that moment when a transistor-designed operational amplifier has to be put in the modulator. If the said amplifier had for any reason a specification not meeting the modulator exigence, we could surely see a spectrum different from what expected. In general, it is worth checking via simulation after any changes are made, whenever it is reasonable: transient simulations tend to become very long as circuit complexity grows[11].

Notice that even if every SNR calculation is about A-Weighted spectra, the non-filtered spectrum is the one which has to be visualized.

2.3.2 Dynamic Range Plot

This graphic plots the SNR with respect to the power of an input sinewave. The latter is often reported in dB with respect to Full-Scale (dBFS). The full scale is the maximum signal power before necessarily encountering distortion in ideal condition, that is, the signal whose power is such as having the amplitude swinging the ±VREF entire range.

An example about DR is shown in Fig. 2.11 where each point in the plot represents a simulation of the modulator, where just the input signal power changed: the corresponding SNDR measurement from the spectrum of each simulation is reported.

When describing the DR of an SDM in an audio context, the test sinus should be at the frequency of $1kHz$ for each of the simulations. This allows the signal to be processed by an A-Weighted gain of 1, thus not being affected, and the SNDR would then really be input power over noise.

Since the quantification noise is *fixed*, it is expected to have a straight line of equation

$$SNDR(P) = -N + P \tag{2.16}$$

[11] In our case, PLS simulation hit the record of 6 days, while noise-transient ("noisetran") simulations could last for 10-14 days (non-PLS, transistor level) for a simulated time-span of 14ms using 8 or even 16 processor cores. Notice that setting a certain level of accuracy in the simulator is necessary: less accuracy meant in many cases false results.

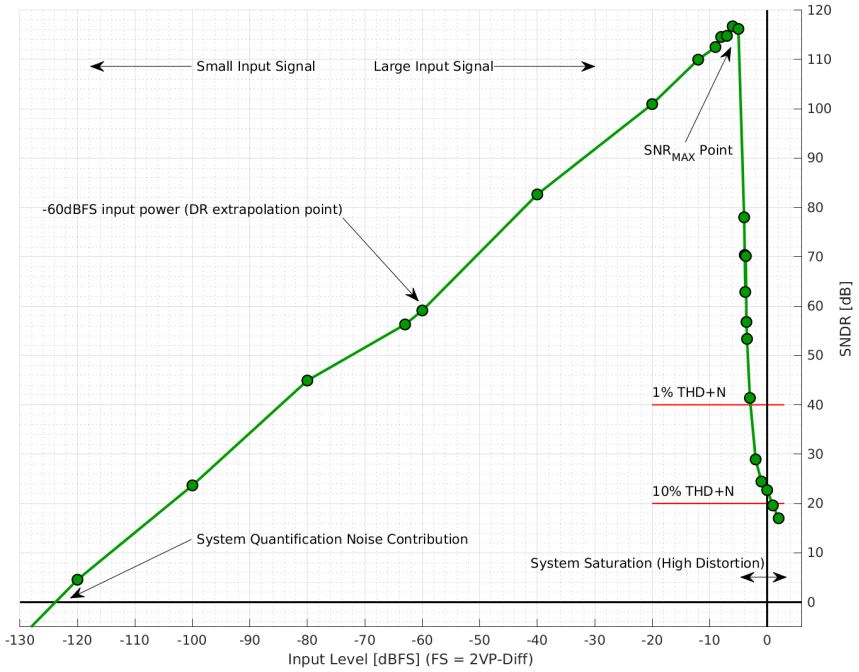

Figure 2.11: Sample DR Plot for our 4th order SDM obtained by several behavioral MATLAB/Simulink simulation at different sinusoidal input signal level.

Expressed in dB, where N is the integrated in-band noise level in dBFS and P is the input signal power expressed in dBFS as well.

This graphic is also very important and can give an overall point of view without having to check every single spectrum. A DR plot tend to need more points at large input signals, in order to monitor at which SNR_{MAX} point occurs, before the curve drops. It should be verified that the slope in Eq. 2.16 remains 1 up to an SNR_{MAX} value: seeing something different from Fig. 2.11 is symptom of system malfunction.

It is a common rule in audio application to calculate (extrapolate) the DR of a SDM as

$$DR = SNDR(-60) + 60 \tag{2.17}$$

therefore also expressed in dB.

If A-Weighting filter is desired, all of the latter values has to be substituted with the ones calculated on data extracted after the filter in each of the simulations, in which case, SNDR and DR become expressed in dB_{Aw}.

2.4 Notes About Simulation Conditions

In this section, some notes about working conditions and analysis are presented. These are concepts, setups and conditions the author wanted to keep as a sort of *standard* for all simulations, in order to make comparison straightforward.

2.4.1 Transient Simulations

All transient simulations done to obtain data such spectra and Dynamic Range, have many parameters in common in our application. They are all set up in order to verify performance about this specific work. They are therefore affected by audio-oriented insight necessities, filter settling times, particular inputs, which are all in fact simulation parameters specific for this modulator. A transient simulation is done in Cadence Virtuoso environment, with Eldo simulator from Mentor. It is set up to have a duration of 14ms, the input signal is at the frequency of f_{in} = kHz. It is common use to use 1kHz input signal frequency in

audio simulations, as it is a frequency where there is no attenuation nor amplification due to A-Weighted filter. Thus, A-Weighted filter will have no effect on input signal.

At the end of the simulation, FFT are applied to the output PDM node and to the A-Weighted PDM node. The FFT is calculated over 30720 points at a sampling frequency of $3.072MHz$, starting from $4ms$: this is done to allow A-Weighted filter to settle. This means analyzing 10 input signal periods, with 3072 points per period. There is no need to have a prime number of periods, as the noise is shaped. The resulting spectral resolution is therefore 100Hz. This value has been chosen as a good compromise between accuracy and simulation time: doubling the spectral resolution to 50Hz would improve reading the results, but would cost the double in simulation time, since double the number of points are needed. The accuracy obtained with 100Hz is sufficient. A Blackmann-Harris windows is always used. When simulation time is reasonable, the spectra are shown as an average over 16 spectra calculated over 16 different 10-periods. This makes these graphics cleaner and easier to read.

2.4.2 Performance Analysis

As stated earlier, standard evaluation rely on FFT performed on a 30720 samples simulation. As a consequence, the real part of the spectrum S(f) resulting from this calculation is actually represented by an array of 15360 points, which we will name S[n] in order to highlight the discrete nature of this quantity with respect to the continuous spectrum S(f). It covers all frequencies up to Fs/2 = 1.536MHz, therefore the spectral resolution is 100Hz. The signal-to-noise-and-distortion ratio (SNDR), by definition, represents the ratio between signal and noise power (defined as P_S and P_N respectively) in the band of interest. Working in audio domain, the latter is 20kHz. According to earlier assumptions, this baseband is represented by the first 200 points of the array and, due to windowing, the signal power is contained in 7 consecutive points centered on the value corresponding to 1kHz (that is: points from 7 to 13). Every other point in this part of the array is noise. So when calculating the SNDR given a spectrum data array, the formula applied to the output spectrum of our simulations will be

$$SNDR = \frac{P_S}{P_N} = \frac{\sqrt{\sum_{k_S=7}^{13} S[k_S]}}{\sqrt{\sum_{k_{N_1}=1}^{6} S[k_{N_1}] + \sum_{k_{N_2}=13}^{200} S[k_{N_2}]}} \tag{2.18}$$

Dynamic Range is extrapolated from a transient simulation with a -60dBFS input signal power. If the PDM is extracted after the A-Weighted filter, $\mathrm{SNDR_{AW}}$ may be specified and, once extracted, 60dB are added to the result to find the DR value (Aw). Also, plotting the complete DR curve is important to know the behavior of the modulator at low, medium and high input level. This is done by running the same simulation, changing the input level only. Then, each resulting SNDR from these simulations is plotted versus the input level itself. At -3dBFS a Total Harmonic Distortion (THD) higher than to 10% is not tolerated.

In order to give an index of modulator performance, a few Figures of Merit (FOM) exist. There are quite a lot of parameters involved in determining a good or degraded performance for a SDM: the design community has finally chosen to represent it by the combination of DR[12], *Nyquist* bandwidth and power consumption. This work falls among the "high resolution" SDM category: amongst all FOM expressions, Schreier FOM is the most suitable and is defined as follows

$$\mathrm{FOM_S} = \mathrm{DR} + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{P}}\right) \quad or \quad \mathrm{FOM_{S,SNR}} = \mathrm{SNDR_{MAX}} + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{P}}\right) \tag{2.19}$$

[12]Or sometimes the Maximum Signal-to-Noise (and Distortion) ratio ($SN(D)R_{MAX}$) obtained in the DR curve.

where BW is for Bandwidth and P for dissipated power.

While reporting modulator performance, it can often be found in literature that power dissipation of the voltage reference is not taken into account, while it should. However, since to provide a voltage reference a dedicated circuit exist, there is an aspect to be accounted for: the latter circuit may not be designed just to supply a *modulator-only circuit*, but it may also generate reference voltage and currents for a whole and more complex circuit, or it may not be optimized in current consumption. This is why, in order to evaluate a modulator FOM, just the current which is actually drawn from the reference should be expressed. In this manner, the FOM will be independent of the structure the voltage reference is implemented with. To go further, a comment should be also made on decimation. SDM are oversampled converters. While in Nyquist converters the output PDM is directly a representation of the instantaneous converted input, in an oversampled converter the output must be filtered of all the the shaped quantum noise present at those frequencies higher than the bandwidth and reconstructed over several samples as the one-to-one correspondence is no more valid. For this purpose, decimation filters are placed after modulator output. They are generally realised by combining a SINC and a FIR filter in cascade. Their power consumption is never taken into account in literature, as the analysis is *limited* to the modulator only. It is the case in this work too. However, sometimes lower performance in DR or FOM value may lie on the choice of keeping OSR low, made because a lower OSR means a less power consuming decimator. If this strategy is used by the designer, the benefits *a posteriori* cannot be seen by reading a FOM.

The state of the art for Audio performance FOM is above $170dB$ with the best works over $180dB$.

2.5 State of the Art

Once the background on ADC architecture is given, their theory of operation and their implementations is acquired, it becomes interesting to analyze the state of the art. There are often interesting works of the same domain or addressing the same issues one could came up with. Analyzing the state of the art is not just a phase, but it is a process which is kept open over the entire duration of this work because challenges can be found along all the design process. The state of the art does not only represent a matter of comparison between our ADC and those from the community, but also for addressing more specific issues. To make an example: not only one can find 100dB DR Audio SDM candidates, but also works on sub-circuits optimisation (comparators, feedback DACs), as well as methods for characterisation, mathematical approach and so on. This marks the importance of always keeping informed on the state of the art.

2.5.1 A Foreword on this Work

In this context, a foreword should be given: performance of our modulator would be subject to three practical facts, which are time factor, the ST Design Team objectives and industrial application orientated objectives.

Time factor - This work has to be backed up, developed and validated first on a behavioral level then to transistor level and finally on silicon. As any PhD thesis, the time limit for the project associated is of 3 years (specifically in our case may 2018 to April 2021). Constantly improving the design to keep up with works published becomes more difficult the more the modulator approaches to a finished state. Three years are a quite long span for new great innovations to be published, but the timetable shown in Appendix D may be helpful to visualize the growing rigidity the modulator in this work has against changes through time. The main goal of this work is to create a functional prototype on silicon and everything necessary to this task impose time budget and efforts concentration.

The ST Design Team objective - An *industrial* thesis, becomes concrete when a project proposal is visualized and defined. It is the "hosting" company which often propose a

subject or which anyway consider R&D on a certain topic valuable. In our case, there were no expertise about continuous-time archetype choice for SDM in the ST Design Team. This is one of the reasons for which this necessarily continuous-time related project raises ST interest. At the same time, a reasonable amount of time and efforts were to be dedicated for gaining expertise on continuous-time modulators.
Industrial application oriented objectives - as an industrial thesis, it is normal to find motivations, objectives and choices more oriented towards development rather than innovation. This kind of works represent the link between the academical point of view and the industrial one. This work is neither an innovation spearhead, nor a massively produced chip. It should not be a performance exasperated structure where everything is perfect (but only for samples *centered* in technology), nor should it be a mere design to simply address a task and have a proper yield. The spirit of this kind of work is to methodically apply *high-level* knowledge, checking its feasibility, to a reality which anyway mass production, requested by market.

Performance loss and known solution not used are mainly due to the latter three aspects of an industrial thesis. It is just the naturally encountered *set of rules* realization impose.

2.5.2 Common Design Choices

This being said, to reach a 100dB DR and achieve low power consumption performance, the state of the art offer generally certains sets of the main modulator parameters.

First of all, the architecture implementation: the most commonly found in publications, as briefly introduced earlier, is the continuous time implementation, with the exception of some recent works in discrete time and some hybrid modulators (generally with the first stages implemented with Active-RC and the last ones with Switched-Capacitor integrators).

OSR should be reasonable. Audio application fixes the baseband, so, in the state of the art, OSR represent a multiple of a value in the 20÷25kHz span of frequencies. A factor of 128 already translates in a 6MHz sampling frequency. Raising this value can rapidly cost in current consumption. A factor of about 64 can also usually be found, with modulators clocked therefore around 3MHz. This should not be thought as being only due to operational amplifiers band requirements. A really important fact is, in the state of the art we can find Figures of Merit (FoM) comprehensives of power consumption, but, eventually, not every contributor is properly accounted for. Examples are the decimation filter after the modulator, the eventual circuit needed in a multibit solution to translate the output samples to a Pulse Density Modulated (PDM) signal, and the voltage reference: sometimes these circuits contribution in power consumption does not appear in the total.

For what concerns LF order, generally a third order modulator is the most appreciated and more often found. If, indeed, combined with a multibit quantizer it can also keep OSR quite low. The cost of not using a multi-bit would clearly be a stage more or a higher OSR. This will be analysed in Sec. 2.6.

To conclude with the trends, generally the quantizer has likely $15 \div 17$ levels in multibit solutions. Modulators using a single-bit quantizer, as commented in Sec. 2.6.4, were not very attractive at the time this thesis began.

After this general overview, in the next Section some actual works are presented and commented.

2.6 Representative Modulators

There are plenty of modulators meant for audio applications present in the literature, the ones which have been chosen to represent the State of the Art are gathered in Tab. 2.2. It is worth mentioning a few motivations for some of these choices which, in general, have already been filtered through $100dB$ DR modulators.

Papers [14] [15] [16] [17] [18] represented the State of the Art at the beginning of this 3-years project. They have been chosen as representatives because they were interesting

Ref.	Tech Node [nm]	Supply [V]	SNDR [dB]	DR [dB]	BW [kHz]	Power [uW]	FOM (S) [dB]
[14]	350	5	105	114	20	68000	168.69
[15]	350	3.3	106	106	20	18000	166.45
[16]	180	0.7	95	100	25	870	174.58
[17]	40	2.5	90	102	24	500	178.81
[18]	180	5	99.5	101.3	20	1100	173.9
[19]	65	1.2	94.1	98.2	24	68	183.6
[20]	28	1.5	96	103	24	3000	172
[21]	180	1.8	106.4	108.5	20	618	183.6
[22]	160	1.8	106.5	109.8	20	440	186.4
[23]	65	1.2	101	103.5	24	134	186
[24]	160	1.6	91.3	103.1	20	390	180.2
[13]	180	1.8	98.2	103	24	280	182.3

Ref.	Year	Notes
[14]	2003	DT Fifth Order Multibit 17 Levels
[15]	2005	Hybrid CT/SC
[16]	2009	DT Multibit 18 Levels Second Order Chopper Stabilized
[17]	2011	Hybrid CT/SC Second Order 17 Level (5 Level Int.) DAC
[18]	2012	DT Multibit 15 Levels Third Order Spectral Shaped
[19]	2018	CT 1.5-bit Negative-R Assisted
[20]	2020	CT 7-bit up/down FIR DAC Chopper Stabilized
[21]	2020	CT Zoom
[22]	2020	DT Zoom
[23]	2020	CT Chopped Negative-R Tri-Level FIR-DAC
[24]	2016	CT Multibit 17 Levels
[13]	2013	CT Single-Bit Third Order FIR-DAC 12 Taps

Table 2.2: State of The Art for Sigma-Delta Audio Converters plus their Notes and Architectures. By SNDR, $SNDR_{MAX}$ is meant. FoM(S) is calculated wherever it was not explicitly written in the corresponding publication.

implementation of different and peculiar solutions, which have eventually been "historically" important for this reason.

At this point, it is worth commenting [14], which can be seen having the high modulator Order of 5. Its a high power consumption, is the price for a 114dB DR. The comment is: a 114dB DR is far above the 100dB target. Our objective is not to spend effort and power consumption for such a high DR. It is important to contextualize a FoM: the work in [14] has a quite low value of FoM with respect of others, but has clearly as objective a high DR. In the same way, targeting $100dB$ would eventually bring a lower FoM, as it depends on DR with a linear factor of 1, while the others performance parameters enter as log_{10}.

References [19] [20] [21] [22] [23] represent the State of the Art at the moment when the design phase of our modulator ended and the prototype was sent for realisation. It is interesting to see how the scientific community progressed during 3 years, at the time when this work was already finalised and no more modification would have been possible to consider. In fact, as it has been commented so far, it is also important to keep informed about the state of the art while advancing with the project: gathering information about the state of the art is a process which shall not just be restricted to an initial period.

Notice that the work from Lee, Jang and Chae [19] has been included even if it does not reach the target $100dB$ for DR: this was made because the power consumption is stunningly low! These seemed enough to worth a mention.

Finally, two special mentions are represented by De Berti, Malcovati, Crespi, Baschirotto, [24] and Sukuraman, Pavan [13] works. These are two modulators which represented the difficult choice between multi-bit and single-bit + FIR-DAC configuration for the quantizer at the very first phase of this thesis. They also used to represent the highest FOM values present in the literature at that time. In particular their performance in DR and

power consumption were very similar and excellent representative of our target. This actual difficulty in choosing between the two aforementioned architectures.

2.6.1 SC Examples

There exist some audio DTSDM and some of them indeed, especially recent ones, can reach very low power consumption. At the time this work began, T. Wang had published a work showing how a DTSDM [18] could consume power as low as $1100\mu W$ with 5V supply. Now, this value has been improved by the work of M. Jang et al. [23] whose power as low as $134\mu W$ from a supply of 1.2V. Furthermore, it can be noticed that today the best FOM in the state of the art is also to be attributed to a DTSDM, the one from Eland et al. [22].

The choice of a DTSDM is a robust one. For each signal feeding a Switched Capacitor Integrator, the loop filter coefficient is synthesized by ratios between the corresponding input capacitor and feedback capacitor: referencing to Fig. 2.12, the expression for a coefficient k is

$$k = \frac{CI \cdot V_{ref}}{CF} \tag{2.20}$$

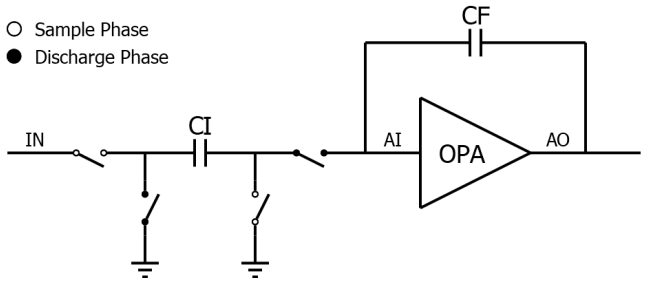

Figure 2.12: Coefficient Synthesis with Switched Capacitor (SC) integrators. Phase labels are intended when the corresponding switches are closed.

As always, in front of data, the analysis should be critic and take into account the context.

If a continuous time counterpart was to be designed, power consumption would be of course lower, that's a matter of signal at the input of each integrator. Impulsive waveform will need more bandwidth in the amplifier. Furthermore, the antialias filter power consumption is not even mentioned in DT budget when showing performances. This can be easily found, in a work of Sukumaran and Pavan [13] for the first case, consuming $280\mu W$ from a $1.8V$ supply and of Lee [19] for the second case, consuming an outstanding $68\mu W$. These candidates have been chosen because of the period of their publication (2013 and 2018), in order to make a comparison with [18] (2012) and [22] (2020) respectively.

Of course a CTDSM will suffer in design complexity, due to jitter issues and RC-Product spread.

2.6.2 Hybrid Continuous-Time/Discrete-Time Modulators

There have been attempts, both in academic and industrial environments, of using both Continuous-Time and Discrete-Time *blocks* in the same modulator. The representative of this category is [15], whose structure is shown in Fig. 2.13.

The idea is of course to combine both advantages, for example:

- using lower power consuming CT integrators in the most-consuming first stages of the LF
- lowering jitter impact by having a part realised in the naturally low jitter-sensitive DT fashion

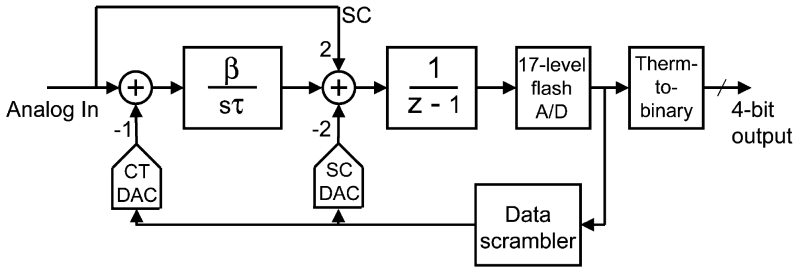

Figure 2.13: System diagram depicted in [15], the hybrid modulator from Nguyen, Adams, Sweetland and Chen.

- taking advantage of the antialias effect of a CT LF

Hybrid configuration does not seem to attract the community attention, but it is interesting to present this category. Work [15] still remains an efficient performing audio modulator, even if it is *a first attempt* and demands a quite high power.

The tendency remains to prefer a fully-CT or a fully-DT built modulator.

As introduced earlier, for what concerns audio application, the CT is preferred for its intrinsic lower power capability. The most important drawback of using a continuous time structure is a dramatic jitter noise sensitivity, which has been addressed in various different ways. Two of these techniques are particularly efficient and interesting therefore, a difficult choice has to be done between the two best candidates available at the moment this project started.

2.6.3 Continuous Time with Multi-Bit Quantizer

Having a Multi-bit quantizer is a widely appreciated solution as it is both helpful for SQNR and SJNR improvement. Increasing "b" parameter can be observed to improve both SQNR and SJNR. This would basically be the winner choice. It not only addresses jitter but it also allows to relax OSR and modulator order, as well as to improve system stability.

The drawback of using a multibit is circuit complexity: as introduced in Sec. 2.2.3, mismatch between elements has to be compensated.

Multibit quantizer solutions, along with their mismatch compensation techniques such as DEM, are robust and mastered solution.

Since the beginning, this work was oriented towards a single-bit quantizer implementation, choice which will be covered in Ch. 4, Sec. 4.3. The work from De Berti, Malcovati, Crespi, and Baschirotto put us in front of a complicated choice: single-bit with FIR-DAC solution (while promising results compliant with the target, was less spread and less covered by scientific backup) or a reference about a multi-bit quantizer based modulator obtaining the same results, with a strong knowledge-base. Remembering that the creation of a well performing prototype was mandatory and though the less knowledge available could have represent a risk, we decided to choose the first one.

2.6.4 Continuous Time with Single-Bit Quantizer and FIR-DAC

The main issue concerning a single-bit quantizer choice in a CTSDM is the extreme sensitivity to jitter. Without any countermeasures, the drop in the global SNR is dramatic. The idea to address jitter noise by the mean of introducing a FIR-DAC[13] in the feedback loop was first analysed by Oliaei in [25]. Feedback pulse shaping techniques were already known in [26] or in many other works used for other purposes (such as tone reduction, linearity and stability improvements).

[13]Since this structure is extensively explained in the next chapters, it hereby just cited as a jitter reduction solution.

In general, the community was not attracted by this solution, and at the time this thesis started, there was only very few works from Pavan which brought this architecture back on stage. Even though, many people are still neither convinced by the benefits this solution introduces nor by the reliability. The main concerns are about instability brought by introducing so many additional poles in the loop, as well as an additional delay in the loop. Of course, it can be stabilized[14], as it has been proven by early works just cited, revalued by Pavan [13] [27] [28] who also obtained excellent FOM.

Many additional CTSDM [29] [23] [20] featuring a single-bit with FIR-DAC solution have been developed early.

2.7 "Industrial" State of the Art

As it has already been commented during this chapter, industrial oriented design has different objectives, constraints and framework with respect to pure research. This is why it is interesting to report some examples of an "industrial state of the art", that is, products available on the market about audio low-power converters. Some meaningful circuits are proposed in Tab. 2.3, which references are their official and public datasheets. It can be noticed that some features are commonly desired in these kind of products:

- Multiple Channels: interesting for stereo purposes, or simply record more than one track, such as in a conference where several microphones are present on conference tables. This feature gives also the choice to interface analog microphones or twice as much digital microphones.
- Programmable sample rate: the classical Nyquist 48kHz audio bandwidth is available along with more or less wide bandwidths: 96kHz and 192kHz for even better audio experience and 16kHz or even 8kHz for *low-quality* communication (like phone calls or walkie-talkies).
- Multiple Voltage Supply: having the possibility of a "low power/high accuracy" compromise is often a feature available in a product. The user can program the chip in order to trade between least power consuming modes with lower performance up to very accurate yet more consuming ones.

These features come with a cost: additional circuitry is present to allow programming and this translates in higher power consumption and surface budget. More control blocks are also necessary, because a mass-market-oriented circuit has to obtain the so called "maturity" adequate to the use it is designed for. Maturity checks are severe tests which try the circuit capability of not incurring to any issue, such as malfunctioning, programming failures, parameter/performance drift over time. Some maturities are more severe than others, such as *automotive*: this level of maturity is necessary for the circuit to be used on vehicles and has a high number of severe constraint the circuit has to pass in order to obtain this qualification. Often there exist different version for automotive and non-automotive for the same circuit, in order to release the latter on the market while a solution is studied for the former to fit vehicle market. Between the two, there can be eventually performance loss either. This aspect should be taken into account as a plus-value while commenting the fom of a Sigma Delta inside an industrial circuit.

In Tab. 2.3, only a selection of stand alone ADCs based on Sigma-Delta Modulators have been chosen, to have the most comparable circuits possible: often ADCs are just part of a more complex circuit with more features than just data conversion. About the presence of more than one channel, the power consumption has been reported along with the number of active channels, in order to be able to estimate the "power consumption per channel", which is also used to calculate FOM.

All of the latter argument can be noticed to be affecting industrial circuits. They tendentially result to be more power consuming. By consequence they also tend to have lower

[14] As long as a reasonable number of FIR-DAC Taps is used, naturally.

Ref.	Price* [$]	Supply [V]	SNDR [dB]	DR [dB]	BW [kHz]	Power/Channel [uW]	FOM (S) ** [dB]
[30]	6.65	5	-	101	24	90000/2	158.27
[31]	5.95	2	107.3	115	27.7	19700/1	176.48
[32]	0.987	5	99	99	24	8600/1	163.46
[33]	2.74	3.3	106	107	24	11300/2	173.28

Ref.	Year	Notes
[30]	2008	Cirrus Logic - SC 5th Order Multi-Bit
[31]	2019	Analog Devices - Mostly Sensor-Oriented and for audio testing
[32]	2011	Texas Instruments - Single-Ended, Automotive Qualified
[33]	2019	Texas Instruments (Burr-Brown) - Quad Ch. Analog/8-Ch. Digital

Table 2.3: "Industrial" State of The Art for Sigma-Delta Audio Converters. While multiple setups are available for these products, in the table only one is reported. All values are TYPical.
*: for a placed order of 1kU on Mouser Electronics online store, data updated to Q1 2021.
**: FOM is not reported in industrial applications and datasheet, in this table it is calculated.

FOM with respect to pure research state of the art counterparts, year of manufacturing considered.

This work will not have to actually withstand any maturity check for mass market, but it is oriented, as presented in Sec. 2.5.1, towards gaining expertise and provide knowledge with the mindset of giving privilege to robustness, in preparation of a future use in mature products.

Chapter 3

Jitter Noise

Jitter Noise represented one of the most relevant parts of this work. A CTSDM is particularly sensible to jitter noise and our objective is to use a quartzless source for clock generation, which has poor jitter performance. These two facts define a challenging scenario and justify the importance of all the work done about jitter. The amount of information and time budget involved addressing jitter issue in this work surely deserve an entire chapter to be presented. Since jitter is a phenomenon that can be thought at behavioral level, the chapter is partly organised as the previous, with presentation and definition of jitter itself, insight on the parameters involved and any aspect that should be known prior to starting the design. The state of the art about jitter in CTSDM specifically is therefore also presented.

All of the previous could drive us to realize the necessity of a very accurate and quantitative jitter model, such as there are none existing in literature. Our objective is then to create a very accurate jitter model (which may be used as soon as at behavioural level) to describe how it affects our system and the effectiveness of jitter-reducing solutions. The task has been carried out with success and the model could be used to simulate our system with a jittered clock; the accuracy under the quantitative point of view allowed to choose, size and validate the jitter reduction technique known as FIR-DAC.

3.1 Timing Jitter and Phase Noise

Timing jitter is an uncertainty in the sampling instant. Let us suppose we have a sinusoidal input signal (Fig. 3.1) to be sampled. If our sampling instant shifts from the expected one, the signal is sampled at a different time the sampled signal has therefore a different value with respect to what it should be. This voltage error justifies the jitter effect to be defined as jitter induced noise.

A situation totally similar to the latter occurs in Discrete-Time SDM. The first stage in the signal path is a switched-capacitor integrator. A switching operation takes place at the input of the modulator and this corresponds to a sample and hold on the input signal. If the clock driving integrator switches is jittered, this signal will be affected by a noise induced by jitter.

There are two ways to define jitter: in the time domain using timing jitter and in the frequency domain using phase noise.

In the time domain, an ideal clock of period T_s samples at the following instants

$$t_n = n \cdot T_s \qquad n = 1, 2, ... \tag{3.1}$$

but if the clock is jittered, the expression becomes affected by a random time-shift $j[n]$, named timing jitter or absolute jitter [34], as follows

$$t_n = n \cdot T_s + j[n] \qquad n = 1, 2, ... \tag{3.2}$$

Here, $j[n]$ follows a certain distribution which in literature is usually approximated to be gaussian for simplicity. In this case, giving the RMS value of $j[n]$ completely characterize

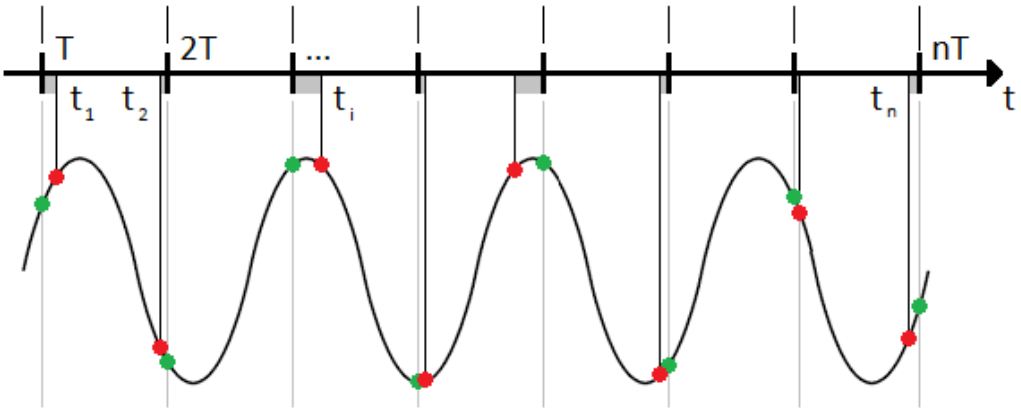

Figure 3.1: Jitter noise on a sinusoidal wave: a shift of the sampling instant means an error (red dots) on the sample (corresponding green dot) itself.

the jitter. There exist many other definitions [34] like cycle-to-cycle jitter or adjacent period jitter. They of course have their utility, but the one which is interesting for SDM is timing jitter.

To consider this signal in the frequency domain, let us take an ideal clock of period T_s, which can be identified by a corresponding sinewave of same frequency

$$c(t) = A\cos\left(\frac{2\pi}{T_s}t\right) \tag{3.3}$$

while a jittered clock can be described by adding a random phase to the periodic signal

$$c(t) = A\cos\left(\frac{2\pi}{T_s}t + \phi(t)\right) \tag{3.4}$$

Though the power spectral density (PSD) of $\phi(t)$ is sometimes called Phase Noise (PN), the following quantity is more often found to be called Phase Noise instead

$$L(f) = 10log_{10}\left(\frac{N(f)^2}{C^2}\right) \tag{3.5}$$

rather defining $N(f)$ as the power spectral density of $\phi(t)$ and addressing to it as *phase fluctuation*, while C is the carrier power. Since this definition represents a power with respect to the carrier of frequency $f_C = T_S^{-1}$, the value of L(f) is expressed in dBc. The distribution of L(f) represents the power at a certain frequency offset with respect to the carrier.

Both representations are useful and a designer can take advantage of the two. A jitter characteristic is usually reported in Phase Noise, time domain representation is however more familiar and intuitive. In addition, for transient simulation purposes, working in time domain is mandatory. Another important fact is that often, while describing the characteristics of a clock, just an RMS value is given for jitter specification. The latter should be always accompanied by a Phase Noise description, because it gives information about the frequency distribution of jitter. Otherwise, if it has to be used in calculations and simulations, only a white distribution can be assumed[1]. This can end up in approximations which are too inaccurate, bringing overestimation or underestimation in certain bandwidths. We will see further that in our case, power distribution in frequency of Phase Noise is a crucial information and the Phase Noise characteristic of the clock is of great impact on a CTSDM.

[1]Or eventually a distribution interpolated with simple filters

3.2 Jitter impact on CTSDM

Our SDM needs a clock signal in order to manage sample instants. Any clock generation method has to be electrically implemented, and therefore comes with its non-idealities. Noise in this kind of circuit translates in providing a jittered clock signal. Since this work combines a CTSDM, sensible to jitter, with a quartz-less clock generation, with expected poor jitter performance, completely mastering jitter is mandatory. The degradation of SNR can easily bring the DR much lower than 100dB, nullifying the efforts made in sizing the other contributions to noise budget.

To understand the importance of jitter on a CTSDM, let us examine the different impact it has on both Discrete-Time and Continuous-Time architectures. In a DTSDM, at the beginning of each period the following occurs: switches commute and the charge stored on sampling capacitors flow into feedback capacitors of their corresponding integrator. This is done according to an exponential law over time. When the following commutation occurs, most part of the charge has been successfully transferred as it can be easily visualized in Fig. 3.2 a). It has therefore limited impact on SNR. On this kind of modulator, jitter mostly

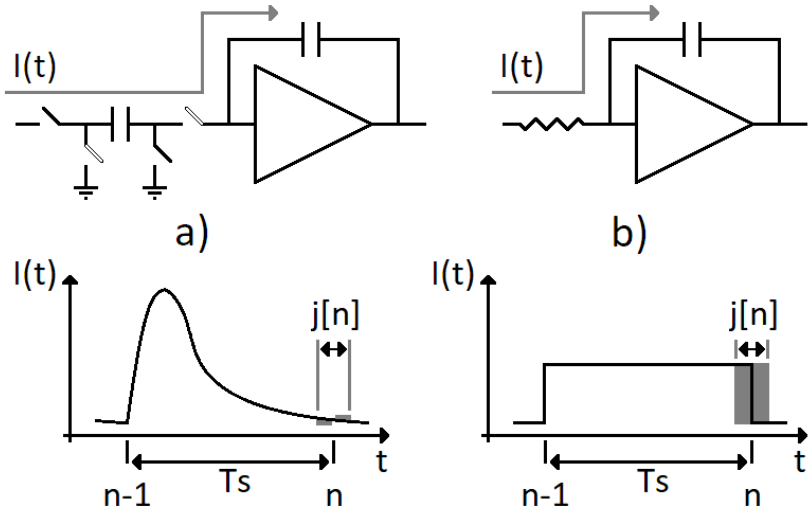

Figure 3.2: Different impact of jitter on CTSDM (b) with respect to DTSDM (a) graphically explained.

impact at the input sampling: just like in Fig. 3.1, it consists in an error committed on the sampling instant of the input signal itself.

In a CTSDM, the input is continuously fed in the loop filter and the only clocked components are the quantizer and the feedback DAC. Sample-and-hold operations occurs directly at the quantizer, therefore input signal sample-and-hold jitter effect is attenuated by the continuous time loop filter. The noticeable source of jitter is at the feedback DAC output. If we took a single-bit quantizer/feedback DAC as example to make it easier to visualize, as depicted in Fig. 3.2 b), the feedback coefficients would be implemented transferring charge from positive (or negative) reference through resistors R_{DAC} (corresponding to the resistor in the figure) towards the proper integrator. In that operation, the transfer rate (current flow) is constant all over the period. In this case, an uncertainty on the subsequent clock transition means transferring a constant and relatively large amount of charge. This contribution is therefore[2]

$$\Delta Q[n] = \frac{(VREFP - VREFM) \cdot j[n]}{R_{DAC}} \tag{3.6}$$

which is huge with respect to DTSDM and, due to the place in which it is injected, it

[2]Notice that the value of R_{DAC} is fixed by time constant of integrators and thermal noise specifications and cannot be chosen to be too high.

is not attenuated by the loop filter. In general, this represents a great degradation of the SNR.

Under a more quantitative point of view, two formulas resuming the approximate expressions for SJNR in DT and CT case are proposed, commented and then compared. In both of them, a white timing jitter distribution is assumed. First, the SJNR for DTSDM, easily found in literature [35], is given by the following formula:

$$SJNR_{dB} = 10\log_{10}\left[\frac{OSR}{4\pi^2\left(\frac{\sigma_\beta}{T_s}\right)^2\left(\frac{f_0}{f_s}\right)^2}\right] \tag{3.7}$$

Where σ_β is the timing jitter distribution variance and f_0 is the input signal frequency. A dependence upon signal frequency for SJNR emerges in this formula. In fact, this is due to the error which proportional to the derivative of the waveform. Given a sampling instant drift, the error is more important if the signal changes rapidly. In conclusion, a DTSDM suffers only from sample-and-hold jitter at the input.

An interesting formula which predicts jitter noise for CTSDM is given in [36]. This calculation is based the occurrence of transitions in the quantizer: if at the sampling instant a no-transition action is decided, there can be no error in the charge transferred, while every transition is shifted by timing jitter and produces an error. Intuitively, the more transitions will take place, the more affected by jitter induced noise the output will be. This argument is taken into account by the term $\sigma^2_{\delta y}$ in Eq. 3.8, which represent the variance of occurring transitions and depends on the characteristic of the DAC[3].

$$SJNR_{dB} = 10\log_{10}\left[\frac{OSR\cdot V_{in}^2/2}{\sigma^2_{\delta y}\left(\frac{\sigma_\beta}{T_s}\right)^2}\right] \tag{3.8}$$

More details about statistical considerations are contained in Reference [36], while the choice of the pulse itself for the CTSDM will be discussed in Ch. 4, Sec. 4.3. The last interesting comment is about the dependence of signal power: higher signal power improves SJNR, a weak signal will cause the quantizer to change state (and inject an error due to jitter) at almost every clock cycle. This may seem contradictory while looking at the spectrum of a jittered sine wave: we experience a "skirt" shape arising at the sides of the central sine bin which becomes more important as the signal power grows. We will see further that from the spectral point of view, this kind of modulation exists but is not relevant with respect to intermodulation with quantification noise. Concluding, in a CTSDM the jitter impact is rather due to the statistical nature of transitions.

Equations 3.7 and 3.8 put in comparison reveal to have two factors that characterize the dependency of SJNR from the DT or CT implementation individually, up to constants. For DT it is $(f_0/f_s)^2$ while for CT is[4] $\sigma^2_{\delta y}$. The first factor can be thought in its worst case where $f_0 = f_B$, that is, the input signal has the highest frequency possible at the edge of the band. Then the factor is simply $(\mathrm{OSR}/2)^{-2}$ which is in the order of 10^{-3} or lower, since by definition of SDM, the parameter OSR is at least 64. For CT, it will also be seen in Ch. 4, as previously commented, that the values of $\sigma^2_{\delta y}$ are in the order of $1 \div 10$. With this argument, in principle, a single bit modulator implemented in CT rather than DT would be 1000 times more sensitive to jitter. Of course there are cases where DT implementations suffer of jitter as well, and those are when the factor $\sigma_\beta/\mathrm{T}_s$ is low, that is, at very high frequency applications, where the performance limit of clock signals are met and σ_β cannot improve any further; the former argument represents a comparison between CT and DT implementation while all the other conditions remain the same.

[3] the values for $\sigma^2_{\delta y}$ are 2.80 for a NRZ, 8 for a RZ and 24.1 for a RZ and HRZ pulse DAC.

[4] Just assume $V_{in}^2/2$ as a constant for simplicity.

3.3 The Importance of Phase Noise Spectra

In the previous section, jitter impact on CTSDM has been explained in the time domain. In this section, the spectral point of view of introducing jitter in a CTSDM will be discussed. Several analysis of Jitter impact on CTSDM can be found in literature, but often for the sake of simplicity, examples, applications and simulations are shown for timing jitter with a white distribution. It is also true, that in many datasheet and specifications of clock references the reader can only find jitter characteristic as an RMS value [37] [38] [39] [40], in some other cases a piece-wise linear defined[5] Phase Noise spectrum with very few points [41] and it is instead very rare to find in datasheets a complete characterization of the spectrum [42] with a graphical representation. In any case, very few works have highlighted it, but the way jitter power is distributed over frequencies is of great importance for the output modulator spectrum [43]. In some cases, like ours, it can be crucial to properly evaluate design choices.

Obtaining a complete analysis of a CTSDM output spectrum, given an arbitrary Phase Noise spectrum is not trivial. A work from Edward and Silva-Martinez [44] is a complete and interesting work. It derives a formula which provides the output spectrum for a generic CTSDM, showing intermodulation effects between both signal

$$\begin{aligned}\Phi_{sj}(\omega) =& \overline{A^2 J^2} \cdot |JIR(\omega) NTF(\omega)|^2 \cdot \\ & \cdot \frac{1}{2} \left(|C(\omega + \omega_0)|^2 + |C(\omega - \omega_0)|^2 \right) \cdot \\ & \cdot |H_{ff}(\omega_0) NTF(\omega_0 T_s)(1 - e^{-j\omega_0 T_s})|^2\end{aligned} \tag{3.9}$$

and quantization noise:

$$\begin{aligned}\Phi_{qj}(\omega) =& \overline{Q^2 J^2} \cdot |JIR(\omega) NTF(\omega)|^2 \cdot \\ & \cdot \frac{1}{2\pi} \int_{-\pi}^{\pi} d\Omega \left| NTF(\Omega)(1 - e^{-j\Omega}) \cdot C(\omega - \Omega) \right|^2\end{aligned} \tag{3.10}$$

The output spectrum of the modulator takes into account various spectra and transfer functions. Basing on the model reported from [44] in Fig. 3.3, all the following participate to define the output spectrum as in Eq. 3.9 and 3.10: the Jitter Impulse Response JIR, the Noise Transfer Function NTF, the Phase Noise C and the loop filter forward-path transfer function H_{ff}. All of them have a frequency dependance. A NRZ DAC impulse response $D(\omega) = (1 - e^{-j\omega_0 T_s})$ is assumed, but this can be generalised to any DAC impulse response with proper modifications. The last parameters involved are the signal amplitude $\overline{A^2}$, the quantization noise power $\overline{Q^2}$ and the mean squared jitter normalized to clock period $\overline{J^2}$.

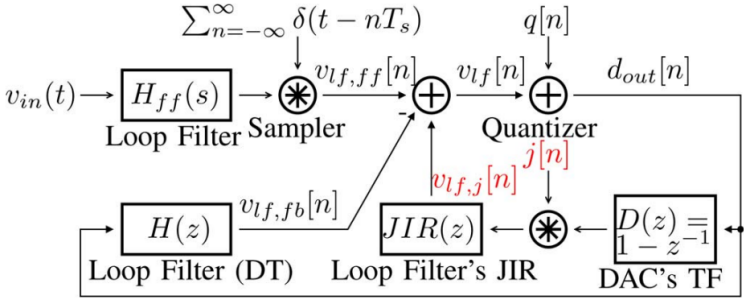

Figure 3.3: Frequency-domain model of CTSDM with NRZ DAC including jitter, from Edwards and Silva-Martinez [44].

A very important comment has to be made about Eq. 3.10 dependance by the intermodulation between the noise transfer function (NTF) and the PN spectrum (C). To help

[5] Few points of the type (magnitude [dBc], frequency [Hz]) are provided to reconstruct the spectrum.

visualizing this concept, a practical situation is anticipated in Fig. 3.4. As seen in Ch. 2 it is common in SDM, that the NTF has a high OBG to obtain low in-band noise. This means that in general, any PN spectrum will cause a great intermodulation product from out of band towards baseband. This is because the OBG of the NTF is actually high on a very wide range of frequencies. On the other side, the usually high Phase Noise values at low frequency for common clock generation circuits impact on a narrower band and its integrated contribution is less important.

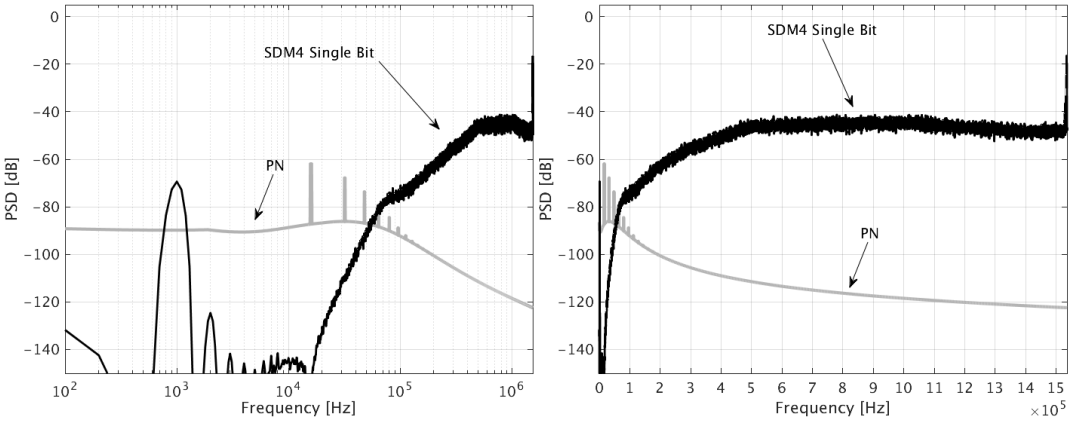

Figure 3.4: Example showing the NTF for our fourth order single bit modulator (electrically simulated) and a PLL phase noise spectrum compared in logarithmic (left) and linear (right) scale.

Some other interesting facts about this intermodulation mechanism and its impact can be found in Sec. 3.5.2 while commenting some models simulation and results.

3.4 Reducing Jitter Sensitivity in CTSDM

Several ideas to reduce jitter sensitivity of a CTSDM exist in the literature. Each of them may be a valid option a designer can consider. It is worth citing some of these methods.

3.4.1 Multi-bit Quantizer

The most robust and widely used technique is to use a multi-bit quantizer. The improvement on jitter is quite straightforward as shown in Fig. 3.5. Instead of having just two Feedback DAC states, as it is the case of a single-bit quantizer, there are several. By consequence, the voltage step of a feedback signal transition is less than a rail-to-rail one.

In fact, for a number of bit b in the quantizer/feedback DAC, the states are 2^b, that is, the voltage swing between two adjacent states is

$$\frac{VREFP - VREFM}{2^b - 1} \tag{3.11}$$

As shown earlier, the amount of error in the charge transferred is proportional to the voltage step when a transition occurs. Rearranging the example seen in Sec. 3.2 for the general case of a multi-bit structure we obtain

$$\Delta Q[n] = \frac{(VREFP - VREFM) \cdot j[n]}{R_{DAC} \cdot (2^b - 1)} \tag{3.12}$$

This translates directly in an improvement in the SJNR with growing number of bits in the quantizer

$$SJNR(b) = SJNR_1 + 3 + (b-1) \cdot 6 \quad [dB] \quad (b > 1) \tag{3.13}$$

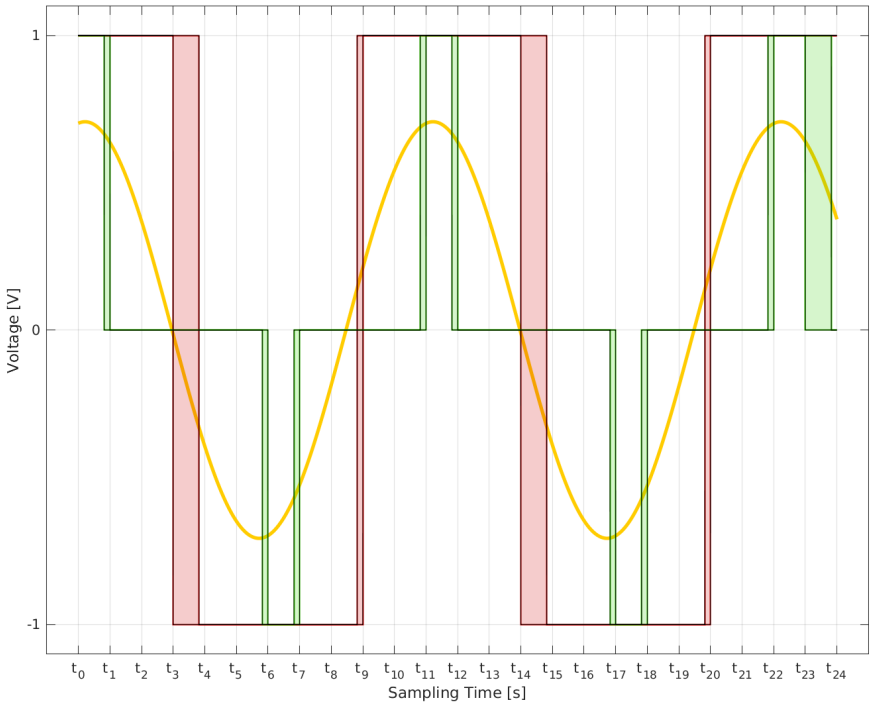

Figure 3.5: Different impact of jitter using a multi-bit or a single-bit quantizer explained. In this figure, a single-bit (red) and a 3-levels "multi-bit" (green) are shown sampling the same signal, then, marked with the same respective colours, they also sample at the same shifted values, for which the integrated difference is shown as coloured areas. The latter represents the severity of the error.

The same can be expressed in function of $N = 2^b$ that is, the quantizer levels

$$SJNR(N) = SJNR_1 + 3 + 6\log_2(N) \quad [dB] \quad (N > 2) \tag{3.14}$$

As seen in Ch. 2, Sec. 2.6.3, choosing a multi-bit is an SNR-wise win on all fronts. The downside of this structure is the necessity of distortion countermeasures, because DEM is surely surface and design effort consuming.

3.4.2 Multibit with PWM FIR-DAC filtered feedback

An interesting work from Colodoro and Torralba [45] tried to find a solution avoiding DEM. This is done by converting the output word of the multibit quantizer to a single-bit pulsewidth-modulated (PWM) signal at a higher rate (a factor of F with respect to oversampling ratio f_s), the latter being afterwards filtered by a FIR. FIR-DAC, as will be carried out later, allows a single-bit DAC signal (which the PWM is) to be used without severely degrading modulator performance due to jitter. The interesting fact in this implementation is that the non-linearity caused by having a multibit quantizer is not included in the loop. Hence, thanks to the topology, mismatch affecting the loop will only occur in the FIR. This can change the transfer function of the loop filter, but will not cause distortion. The price is an increased complexity due to the upsampled frequency $F \cdot f_s$.

3.4.3 Switched-Capacitor-Resistor DAC (SCR-DAC)

This technique [46] falls under the wider category of DAC Pulse Spectral Shaping. As the name suggest, it is based on making the DAC output signal exponentially decaying.

This is done by using a configuration like in Fig. 3.6. Under the point of view of jitter,

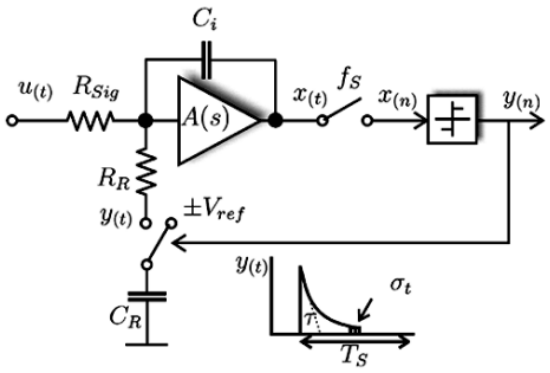

Figure 3.6: Schematic of a Sigma-Delta modulator with SCR feedback taken from Ortmanns, Gerfer and Manoli work [46].

the modulator can benefit of the advantages found in an SC implementation. However, the charge information is now contained in an impulsive signal, which has therefore to be supported by the amplifiers. This can happen only if the associated amplifiers can afford wider band and higher slew rate, which means a higher power consumption. Such a solution, costs taken into account, seems not to be coherent with the philosophy of exploiting the CT nature of the modulator and this may be the reason why this technique did not spread.

3.4.4 Some Other DAC Pulse Spectral Shaping Attempts

SCR DAC has been taken as example as it is the most iconic and intuitive in this category of jitter mitigation techniques. However, notice that, virtually, any function can be used as feedback [47]. Some other examples can be found in literature: it is worth mentioning SIN-DAC [48] switched current (SI) and switched-shaped current [49] (SSI) or even combination of the two [50] (SI+SCR). Often it can be found, that the downside in these techniques (which may represent some really clever attempts) is the complexity obtaining the function desired with the feedback pulse. The analysis of these works which did not find popularity or continued development is helpful to gather knowledge, realise the background of other people ideas and become quick-thinking about jitter.

Still, there is another DAC Pulse Spectral Shaping that had a different outcome. It is the case of the FIR-DAC, explained in the following section.

3.4.5 FIR-DAC

This technique also belongs to Pulse Spectral Shaping category, because it consist in filtering the output signal from the quantizer with a Finite Impulse Response (FIR) before feeding it back, as shown in Fig. 3.7 a). The detailed presentation, performance against jitter, all other benefits and comparison with the well affirmed multi-bit solution are carried on in Ch. 4, while we give a very brief preview here to complete the discussion about jitter sensitivity reduction techniques.

A FIR-DAC is characterized by a number of taps n and a set of n coefficients $\{d_i\}_{i=1,\dots,n}$ (Fig. 3.7 b)) which give n consecutive outputs to be summed up together, with a sample-delay between each. To easily visualize the principle of operation for this solution, let us take the simplest coefficient set: fix a number N of taps and make all the N coefficients equal to $1/N$. In this way, the output is actually what is called a moving average: at each sampling instant, the "N-times-old" sample leaves the place in the FIR to the new upcoming sample. Under the point of view of the time domain, since the average value of the N subsequent PDM outputs can only change by a factor $1/N$, the voltage step is equal to ΔV given in the following formula

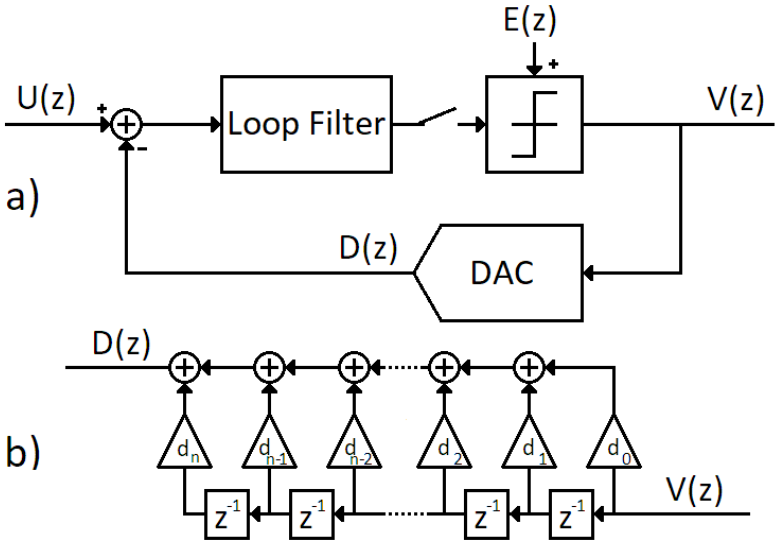

Figure 3.7: Inserting a FIR-DAC with n-Taps: in any SDM behavioral model (a) the traditional feedback DAC block can be substituted by the functional structure in (b), where D(z) is the average of n single-bit DAcs. In a real Active-RC implementation actually injects in the feedback node the sum of n currents of the single-bit DACs (not present in the figure).

$$\Delta V = \frac{VREFP - VREFM}{N} \tag{3.15}$$

If we move from the behavioral model to the Active-RC implementation of the integrators for a CTSDM, in place of summing this voltage directly on the node D(z), each FIR-DAC tap drives a single-bit resistive DAC (see Ch. 6, Fig. 6.1 for further details on the implementation) and the charge transfer error in presence of jitter is be

$$\Delta Q[n] = \frac{(\text{VREFP-VREFM}) \cdot j[n]}{R_{DAC} \cdot N} \tag{3.16}$$

Equation 3.16 has exactly the same functional structure as Eq. 3.6 for multi-bit case, where we traded a $(2^b - 1)$ factor for N. For what concerns jitter in the time domain[6], a FIR-DAC behave therefore exactly as having an N+1 levels multi-bit quantizer. On the basis of what has just been demonstrated, the designer finds that the two solutions bring exactly the same results in reducing jitter impact on the modulator: the choice of one over another is explained in great detail in Ch. 4, Sec. 4.7.6.

3.5 Simulating Jitter

Once jitter induced noise origin and effects are known, a model should be set up to simulate its outcome on our modulator. Our target is a high performance audio converter. The challenge in this work is that we are using a continuous time modulator, particularly sensible to jitter, with a quartz-less oscillator which is known to have poor jitter performance. In order to obtain the power consumption benefits *promised* by employing the CTSDM implementation, no over-compensations should occur, regardless of the jitter reduction technique used. Moreover, this practice needs a very accurate estimation of jitter. At this point, everything depends on the model and environment used for simulating the CTSDM.

[6] And for what concerns jitter in the time domain only.

3.5.1 MATLAB/Simulink Model

The use of MATLAB/Simulink environment to simulate SDM modulators is widely appreciated. It is an environment more suitable to fixed-step simulations, which reminds of the operation of a Switched-Capacitor SDM (DTSDM). Variable-step solvers are also present in MATLAB/Simulink, however, the Continuous Time case is often simulated with a fixed-step algorithm as well. In principle, the internal-states evolution is equivalent in DT and CT domains, from another point of view, there is a 1-to-1 equivalence [51] between each respective state for a CTSDM and a DTSDM describing the same NTF.

As stated earlier, timing jitter create an uncertainty in the sampling instant. The MATLAB/Simulink environment does not allow the user to add jitter to sampling instants as solvers are fixed-step. Blocks in Simulink update theirs outputs at each simulation step. If a variable-step solver was used, one should implement new blocks such as the step updates are subject to conditional signals. It is indeed necessary that the steps should be *shorter* than the order of magnitude of jitter, or the distribution will be cut in some values of timing jitter which are too small. However, this feature would add such a complexity to the simulation, that an electrical simulator would be more efficient.

This given, simulating a jittered clock while preserving the advantages of MATLAB/Simulink is actually possible. The error must just be modeled another way. The method presented in this section is widely used in models found in literature and is based on correcting the voltage value [52] [53] [54] [55] [56] on feedback paths. Feedback error $e(t)$ is calculated as follows: first, by differentiating the output $v[n]$ in the time domain (referring to the upcoming Fig. 3.8), the feedback variation is obtained, second, it is convoluted with timing jitter $j_c(t,n)$ as in Eq 3.17a.

$$e(t) = \sum_{n=-\infty}^{\infty} (v[n] - v[n-1]) \cdot j_c(t,n) \tag{3.17a}$$

$$j_c^{NRZ}(t,n) = u(t + j[n]T_s - nT_s) - u(t - nTs) \tag{3.17b}$$

$$j_c^{SCR}(t,n) = e^{-\omega_{SCR}(t-\alpha T_s)}(u(t - \beta T_s - nTs) - u(t + j[n]T_s - \beta T_s - nT_s)) \tag{3.17c}$$

Differentiating the output will give us the error injected per unit of time and it represents the amount of constant charge feeding back. This should be therefore multiplied by the timing error $j_c(t,n)$ which represents the timing jitter with the shape given by the feedback DAC. To give two examples of shapes $j_c(t,n)$, in Eq. 3.17b a standard NRZ DAC $j_c^{NRZ}(t,n)$ is assumed while an SCR-DAC $j_c^{SCR}(t,n)$ is used in Eq. 3.17c (where ω_{SCR}, α and β are parameters characterizing the SCR function). In these shapes, $u(\cdot)$ represents the "step" function and $j[n]$ is the time-shift from T_s during the n^{th} sample due to jitter.

The shape of the spectrum from which $j[n]$ are extracted is again of extreme importance to well evaluate the effective impact of jitter on our system. In fact, many works of those cited about modeling used a white distribution as spectrum, that is, Gauss-distributed. This is a really simple model. Consequently it might be a good method to give a first glance on how our output spectrum is impacted by jitter. It can also be used in the same manner to give a first glance to jitter reduction techniques behavior. However, this is far from being accurate, as it is based on the fact that drifting time intervals are Independent Identically Distributed (IID) Random Variables. This is not true for jitter noise, as at each sampling instant, drifting process has memory of the previous samples.

Very few works highlighted the importance of the jitter distribution impact on CTSDM [43] and custom accurately-modeling [57] jitter spectra. A white noise may represent a simple benchmark to put modulators in comparison, so it can be agreed that it may be used if presenting the state of the art on jitter reduction techniques (for example). On the contrary, if a modulator has to be contextualized in an industrial work or datasheet, the use of this approximate model is not a good practice. The frame where the modulator operates is of primary importance to take into account. If a certain clock jitter distribution is expected (like as if the performance of the clock tree is known), an efficient design and performance demonstration can only be carried out if the latter is accurately represented.

Some works propose to substitute the white "jitter model" block (always referencing to the upcoming Fig. 3.8) with one extracting Lorentz-distributed times to multiply the feedback variation, or to use lowpass filter the latter to emulate a PLL. The results are more realistic and these techniques will be carried out in the next section

3.5.2 Advanced MATLAB/Simulink Models

All the principles explained in the previous section (Sec. 3.5.2) are implemented in MATLAB/Simulink simulations using structures such as those shown in Fig. 3.8 where Eq. 3.17a is represented multiplying the differentiation of v[n] with a timing jitter extracted using a specific jitter model. This way, models implemented with Simulink and simulated with MATLAB can be easily improved, substituting a the white noise model (the first on top in Fig. 3.8) with other distributions [58]. It is sufficient to the differentiated $v[n]$ to be multiplied by differently processed Gauss-distributed extracted values, which means $j[n]$ follows a different distribution in each of the three models.

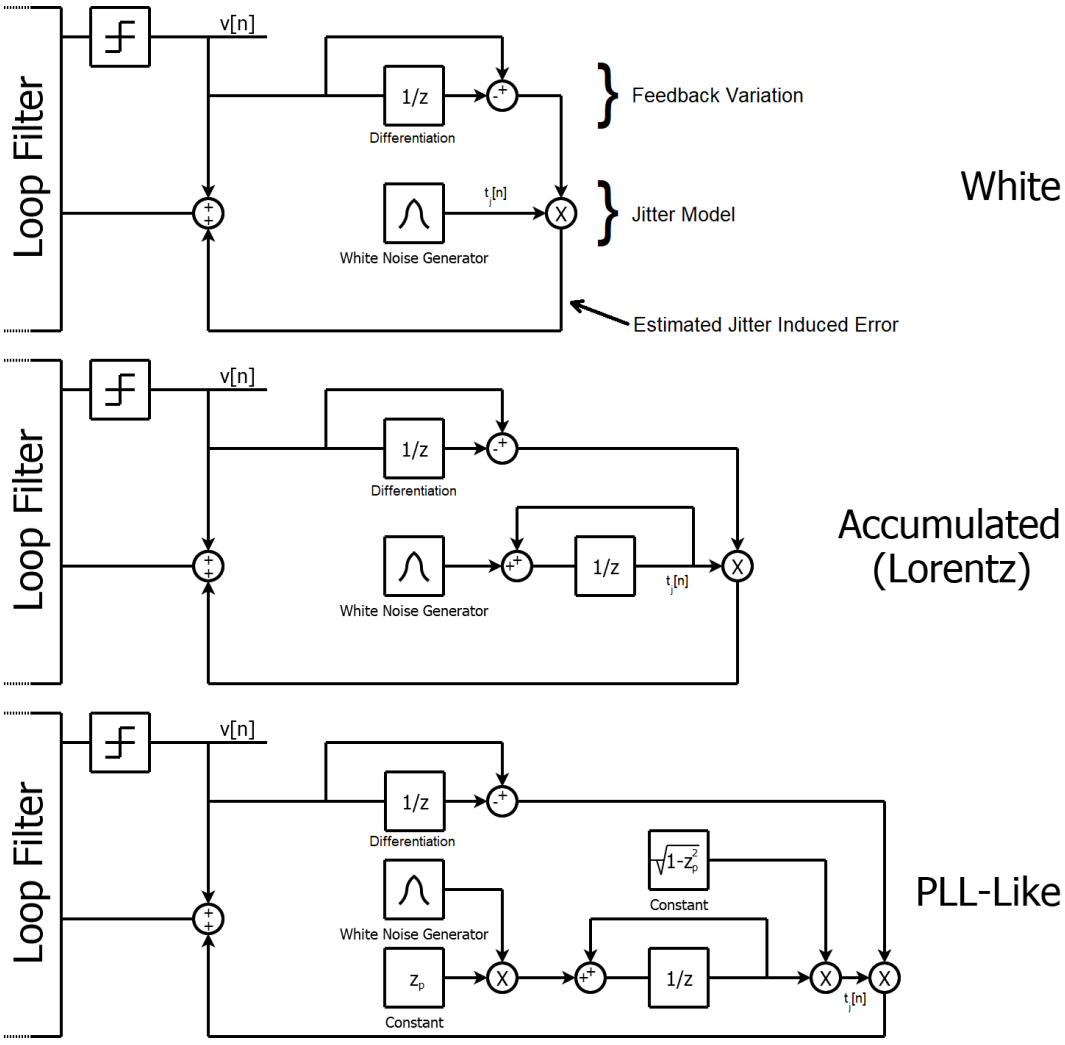

Figure 3.8: White, Accumulated and PLL-Like models implementations in Simulink for jitter distribution, to be simulated in MATLAB environment.

These block-built operations can be translated in having

$$t[n] = nT_s + j[n] \tag{3.18a}$$

$$t[n] = nT_s + \sum_{i=0}^{n} j[i] \tag{3.18b}$$

$$t[n] = nT_s + \sqrt{1 - z_p^2} \sum_{i=0}^{n-1} z_p^i j[n-i] \tag{3.18c}$$

with j[n] extracted in any case from a gaussian distribution of variance σ_j^2. The obtained distributions of time-shifts from nT_s are called white (Eq. 3.18a), accumulated (or Lorentz distributed, Eq. 3.18b) and PLL-Like (Eq. 3.18c). For the latter, it is supposed that an accumulated jitter is lowpass filtered to represent the PLL cutting frequency z_p. Notice that this is still a very high-level modelisation for a PLL.

The simulations results in the case of a fourth-order single-bit CTSDM are shown in Fig. 3.9. It is self-evident that the choice of a more or less refined model impact the simulation: the more refined is the model, the better higher frequencies are represented.

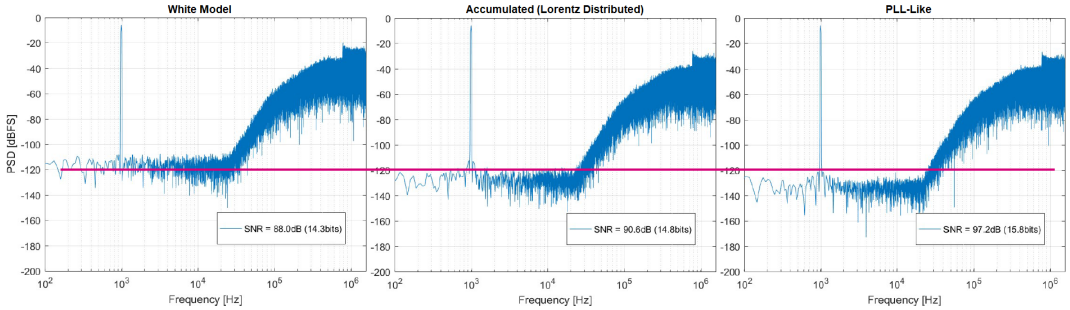

Figure 3.9: Comparison between MATLAB/Simulink jitter models with White (left), Accumulated (center) and PLL-Like (right) jitter distribution. The -120dB spectral density level is highlighted with a red line to better notice the noise floor changing. With the same modulator and simulating conditions, the more accurate the model, the lower the overestimation.

The discussion on the importance of jitter frequency distribution which was carried out all along the chapter will be finally concluded in Sec. 3.6 where the impact on CTSDM will be proven in detail.

3.5.3 Electrical Model

Simulating the CTSDM electrically with Eldo simulator and designing it in Cadence environment brings analysis to a physical meaning: jitter can be physically injected in the modulator by implementing a timing jitter distribution on the rising and falling edge of clock signal. If timing jitter is properly managed, this is the most genuine kind of simulation one can obtain, as it represents exactly what it is physically happening.

The definitive strong point of this modelisation is that, *as simply* as it has just been presented, the representation of jitter as by its very definition given at the beginning in Eq. 3.2 is exact and any jitter behavior can be arranged for simulation. This model is absolutely accurate and quantitative and obviously the most attractive that can be found, as long as the simulation time difference between an electrical simulator and an environment like MATLAB is accepted (about a factor of 5÷10 depending on the level of complexity of the electrical model).

This environment is preferred because of two main aspects. The first is directly relate to the concept just explained that, instead of a mathematical correction, jitter is represented physically as a time shift, allowed by the variable-step[7] differential equation solver algorithm. This means that jitter is represented genuinely as its exact definition. The second is that in practice, the electrical environment allows to use the jitter model presented at different levels

[7]Instead of the fixed-step as with MATLAB/Simulink.

of complexity of the circuit, from behavioral to circuit validation, not limiting to behavioral only. Fortunately, all of these features have to be negotiated with simulation time and there is no difference in complexity of implementation for jitter model in MATLAB/Simulink or in an electrical simulator. For instance, there is no need of simulating the clock tree with noise to obtain timing jitter, the pre-extracted values sequence represents the same distribution and can definitely be substituting this circuit, saving a great amount of time.

All the potential of this kind of simulation can be exploited only if all the set up concerning jitter is accurate: this argument is discussed in the next section, where the novel, accurate and quantitative model that has been developed on purpose is presented.

3.6 Jitter Model Used for Simulations

Having realistic, physical and genuine results is very appreciable, trading with simulation speed. The first ideal and light version of the modulator[8] takes, as just commented, 5÷10 times longer than approximate MATLAB/Simulink models to obtain a standard spectrum (Ch. 2, Sec. 2.4.1); this means about 30 minutes instead of a few minutes with computing power available today. On this subject, also notice that both a simulation with and without jitter require the same amount of calculations once the model is active/present in the system, thus their duration is roughly the same. In this section, the complete jitter model that has been created specifically for total accuracy is explained in detail.

3.6.1 Verilog-A Clock Generator

The code for a Verilog-A clock generator is written, in order to realise the system in Fig. 3.10. Without jitter, a square wave with a period of $T_s = 1/f_s$, that is the oversampling frequency of the modulator, is provided as voltage value: this is used as the *external* clock signal. A transition between the two states[9] will occur at $n \cdot Ts/2$ where n is an integer from 0 to a number $2 \cdot N_{SIM} - 1$ as to suit the simulation length[10] (that is, N_{SIM} is the number of clock periods $N_{SIM} = T_{SIM} \cdot f_S$).

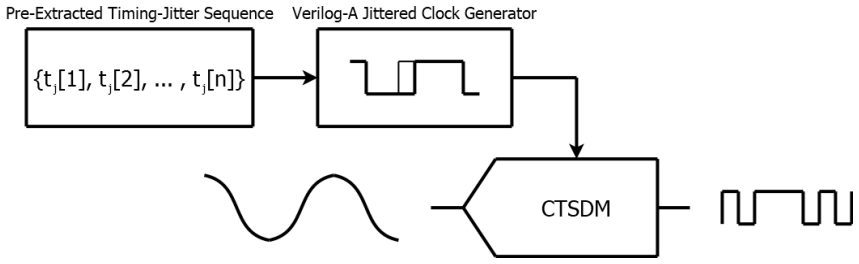

Figure 3.10: The logic lying beneath the jitter model created for quantitative simulations.

Jitter is introduced this way: before the simulation starts, there exist a source file containing $2 \cdot N_{SIM}$ timing jitter values. During simulation, Verilog-A clock generator is coded such as each clock transition instant t(n) is calculated as

$$t(n) = n \cdot T_s/2 + t_j(n); \tag{3.19}$$

where $t_j(n)$ is the n^{th} timing jitter value from source file and which is exactly the same expression as in Eq. 3.2. This argument is in favor of having set up a simulation which behaves exactly as jitter definition.

[8] Ideal Resistances, Ideal Capacitors, Ideal Switches, Verilog-A Ideal Operational Amplfiers (with selection of non-ideal behavior possible), Verilog A Clock Generation

[9] Notice that either the rising time or falling time has impact on the modulator: the other one has absolutely no impact as nothing in the circuit triggers, as long as the DAC is NRZ. Both of the two transition directions are always jittered for simplicity.

[10] For completeness: if the number of transitions are insufficient, the following will be zero until the simulation ends. This would corrupt jitter simulation making it meaningless.

Notice that this Verilog-A model, with the notion of source file that is pre-existent with respect to the simulation, is oriented towards representing an external source for clock signal. This approach fits with the concept of contextualization of the modulator, as there exist an external work that is fully characterised, especially in jitter performance, and the modulator has to be designed taking into account its working conditions.

Now it is up to have proper values of $t_j(n)$ in the source file, which will be covered in the next sections.

3.6.2 Following a proper distribution

The source file must contain timing jitter values extracted from a proper distribution, that is, they must correspond to a given Phase Noise Spectrum.

A spectrum represents in general an RMS characteristic with respect to frequency, therefore, while a timing jitter sequence has its associated PN Spectrum, a given PN Spectrum may correspond to several[11] different timing jitter sequences. This means that extracting a timing jitter sequence from a PN Spectrum let us simulate just one of its possible representations. If there exist the necessity or desire of testing more than a single possible scenario, one may use a set of different seeds[12] to extract different sequences, then initialize several simulations each with its own sequence.

The first step is to transform PN Spectra from RMS nature into random [57], in order to be able to obtain a timing jitter sequence from it. From a mathematical point of view, let us consider Eq. 3.5: by this definition, the spectrum L(f) is continuous, but data obtained by simulations or measurements[13] are a finite number of points which represent an integrated spectral power over a limited band. Thus, $\{L_i(f)\}_{i=1,...,N}$ will instead be an array of N elements, for which each element i represent the following relation with L(f):

$$L_i = \int_{f-\delta f}^{f+\delta f} df L(f) \qquad for \qquad i = 1, ..., N \tag{3.20}$$

In this formula, the N^{th} point represents the highest frequency f_s for which there exist a PN information (value), that is, $L_N = 2\delta f \cdot L(F)$. The relation $2\delta f = f_s/N$ is valid, making $2\delta f$ the spectral resolution.

Now we can introduce a random factor in this spectrum: just multiply each L_i by an uniformly distributed random phase. A public domain MATLAB function named *add_phase_noise* exists [59]: intended to fulfill another task which is adding phase noise to a given signal, it reveals to be very useful also for our needs. The function takes as an input a signal and a phase noise spectrum, the latter being a vector representing a piece-wise linear function. Then it adds phase noise to the signal vector, basing on the input spectrum, which is actually L_i.

To do this, each L_i is multiplied by a complex vector number of the form

$$\{Z_i\}_{i=1,...,N} = \frac{1}{\sqrt{a_i^2 + b_i^2}} \cdot (a_i + j \cdot b_i) \tag{3.21}$$

where a_i and b_i are two random real numbers extracted uniformly between the interval $[0, 1]$ (so, in fact, a phase). The new L_i is no more containing an RMS information, but a random one: performing an Inverse Fast Fourier Transform (IFFT) on this data, will produce a sequence of random phases jitter values following the original L_i.

3.6.3 Extract a Jitter Sequence for Simulation

Let us apply this algorithm to our case, for which a more specific explanation is needed. In this work, Pulse-Density Modulated (PDM) signals analysed are made of 30720 samples

[11] Actually, if both spectrum and phase of an FFT were provided, the relation would be bijective, but information is generally found under the form of RMS spectra.

[12] The number used to initialize a random number generation.

[13] MATLAB or electrical simulators spectrum vectors, .csv files, etc.

(Ch. 2, Sec. 2.4.1). This means the clock makes a number of transitions which is at least double this number of samples, without even taking into account the necessary initial settling time for filters (Modulator Internal Loop Filter, A-Weighted, FIR). On these considerations, a file containing a sufficient number N_{SIM} of timing jitter values should be provided (by sufficient it is meant it should cover all clock transitions expected during our simulation). It should be noticed that, PN Spectra used to extract the sequence are independent data coming from outside our work, which are therefore not meant to fit with desired N_{SIM} in general: it is up to *add_phase_noise* algorithm to interpolate the provided PN Spectrum in order to extract N_{SIM} values.

One last consideration: function *add_phase_noise* is meant to add an "input-distributed" phase noise to a given signal, returning directly the noisy signal. This means, our input signal will have to be a constant complex phase[14] if we want to obtain as an output just the random phases ϕ_i. It will be sufficient to do the following transformation

$$\delta t_i = \frac{\phi_i}{2\pi f_C} \tag{3.22}$$

where f_C is the clock sampling frequency, to finally obtain our timing jitter sequence made of δt_i, i.e., $t_j(n)$.

3.6.4 Application of the Model and Proven Strength of Accuracy

This Section shows the practical proof of both the importance of the PN spectrum injected in the CTSDM under examination and the opportunities of formulating accurate strategies thanks to the model that has been created. Different spectra are compared. They have been chosen to be the same as in the work from De Berti [43] in order to have coherence with a reference which can be used to contextualize all the frame. The very important aspect of these four sample distributions is that they have the same RMS value over the *oversampling band*. It has been made on purpose to highlight the importance to always provide a PN spectrum instead of an RMS value for what concerns interfacing a Sigma-Delta. These curves are shown in Fig. 3.11 top-left: there are three different piece-wise linear function with a more or less weight trade-off between low and high frequency and a white (gaussian) distribution, which is having of course a constant PN spectrum.

From each of these PN curves, a corresponding timing-jitter sequence is extracted following our model as previously shown in Sec. 3.6.1, Sec. 3.6.2 and Sec. 3.6.3. The histogram of the $t_j[n]$ extracted and a time representation are also shown in Fig. 3.11 in the top-right and center respectively. The difference between the three is self-evident in each graphic: it is expectable that a different behaviour will appear when this noise is injected in a CTSDM. This is shown in Fig. 3.11 in the bottom image. The modulator is a third-order 3-bit quantizer. This candidate modulator has been chosen to show the concepts just explained for two reasons. The first is because jitter impact reduction is almost uniform in frequency over the entire band (check back Ch. 2, Sec. 2.1.6 and for comparison for when it is not Sec. 3.7) , therefore this unequivocally highlight the role of PN spectrum. The second is that 3 bits are necessary to obtain a DR superior to $100dB$ for this modulator. Consequently, the danger of overdesign can be easily visualized and commented.

In fact, the impact of each spectrum on the modulator can be recognised in the well known inband flat noise arising. Coherently with the arguments proposed all along this chapter, the PN spectra with the least high-frequency distributed power are less severely impacting the modulator performance. For what concerns the limit case, that is, white noise, it occurs that it is the worst case possible[15] for overestimation. Commenting this situation is important, as white noise is also the most widespread model used to simulate jitter. A designer using this model would find a DR of $102.71dB$ even at this stage which a still high-level behavior simulation is performed. In practice, this means that jitter is totally dominating the budget, while thermal noise should do instead (also considering a

[14] This offset will then be subtracted from the extracted values of the sequence

[15] No "increasing" function are ever considered as a PN spectrum because they do not represent any existing clock generation device.

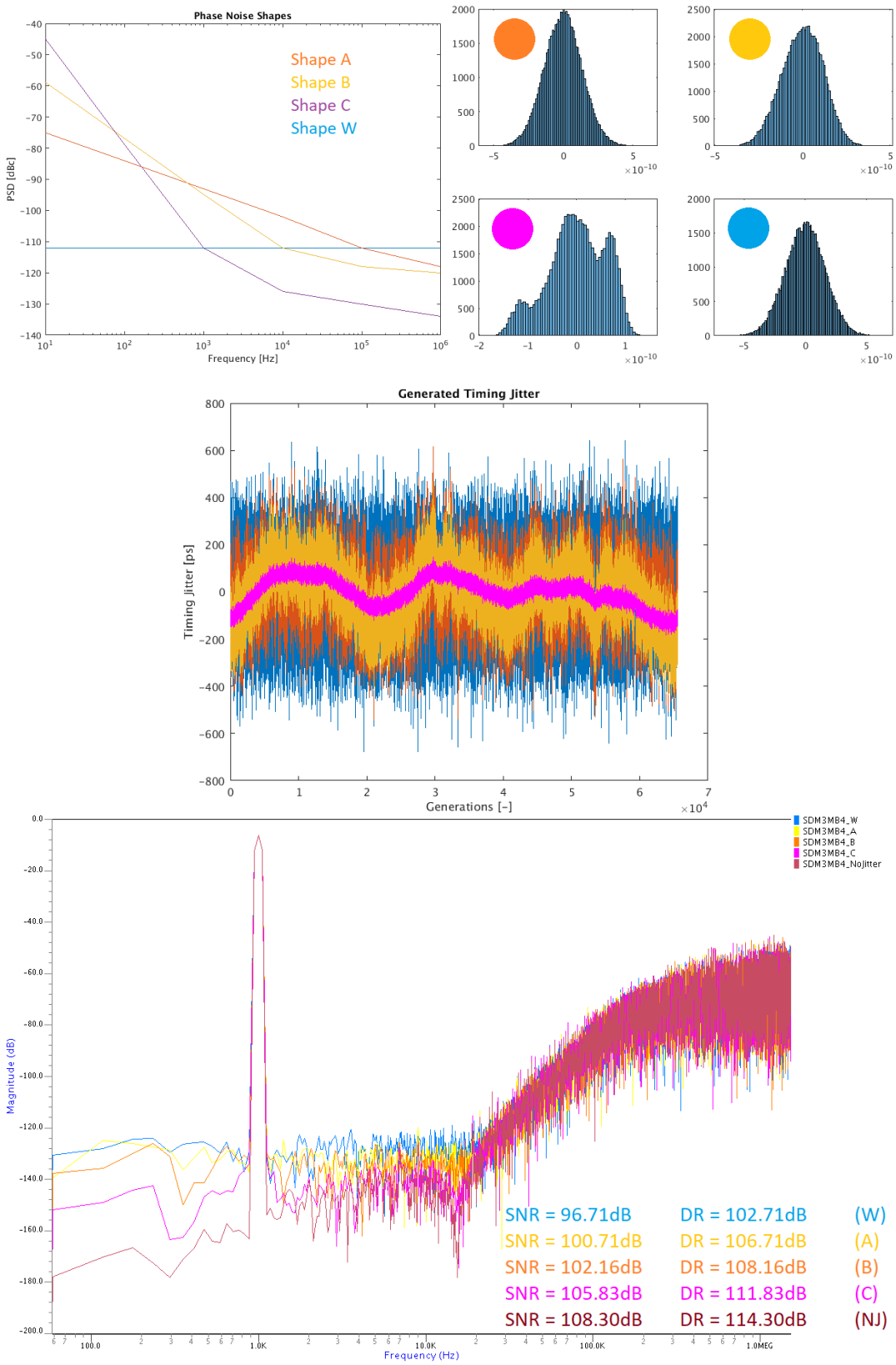

Figure 3.11: Different PN spectra (top left) generate different timing jitter distributions (top right and center) and lead to different performance degradation if injected in the same modulator (bottom).

safety margin on the target as it will better explained in Ch. 4, Sec. 4.2), as per the common strategy shown in Ch. 2, Sec. 2.2.7. This flow would bring to the conclusion that 3 bits are not sufficient, consequently having to be increased. Design effort also increases and eventually performance may become worse, in order to recover from a degradation that was actually just overestimated due to an inappropriate model choice for simulation.

The simulations done with this model allow to accurately simulate a *real and physical* jitter. Now it is a matter of choosing an appropriate PN spectrum.

3.6.5 Phase Noise Spectrum used for simulations

The PN Spectrum used for simulations will always be the same and it is shown in Fig. 3.12: this spectrum comes from an existing[16] PLL used for low-power audio purposes. It was specifically designed for quartz-less clock generation, in the specific case, it could generate frequencies using an SPI bitrate as reference. This spectrum is given as input to

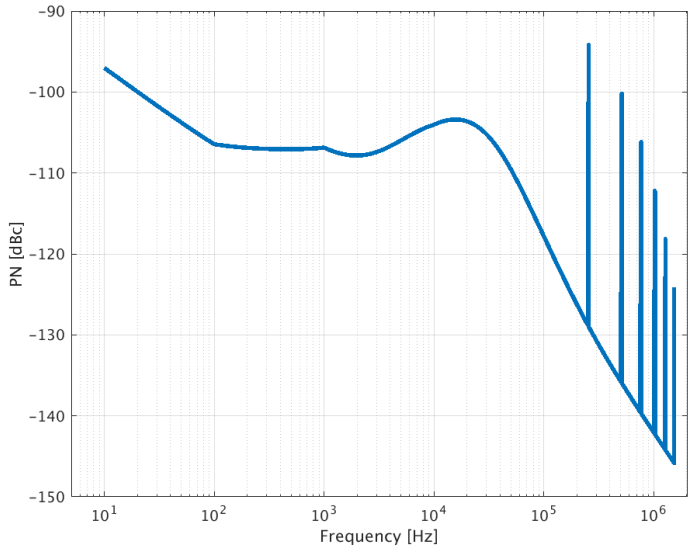

Figure 3.12: Spectrum of the PLL, specifically designed for low-power audio application, used to accurately simulate jitter impact on our CTSDM.

add_phase_noise function, in order to obtain its representation as timing jitter sequence: in Fig. 3.13 a brief analysis is shown. Rearranging in an histogram, it can be verified that the distribution of the extracted timing jitter sequence is not gaussian: the RMS value $\sigma_{\delta t_i} = 140.1767ps$ reported has a different signification than the corresponding value of a white distribution. To prove the effectiveness of this extraction procedure, an FFT is performed on the timing jitter sequence obtained and properly compared to the starting spectrum Fig. 3.13 (Lower Right), finding out that the frequency distribution of this random set of values is a good representation of the latter.

As discussed earlier, a seed can be changed during the generation to obtain a different sequence, which is still a representation of the same given PN Spectrum.

3.7 Important Contributions to CTSDM Design

To conclude this chapter, the benefits of using this model to the design of our modulator are reported. They are basically two and tightly related; in both cases electrical simulations are performed on the candidate modulator as described further in Ch. 4, that is, a continuous time, fourth order modulator clocked at 3.072MHz.

[16] This PLL exist on silicon, but its spectrum characterisation from a MATLAB script is used.

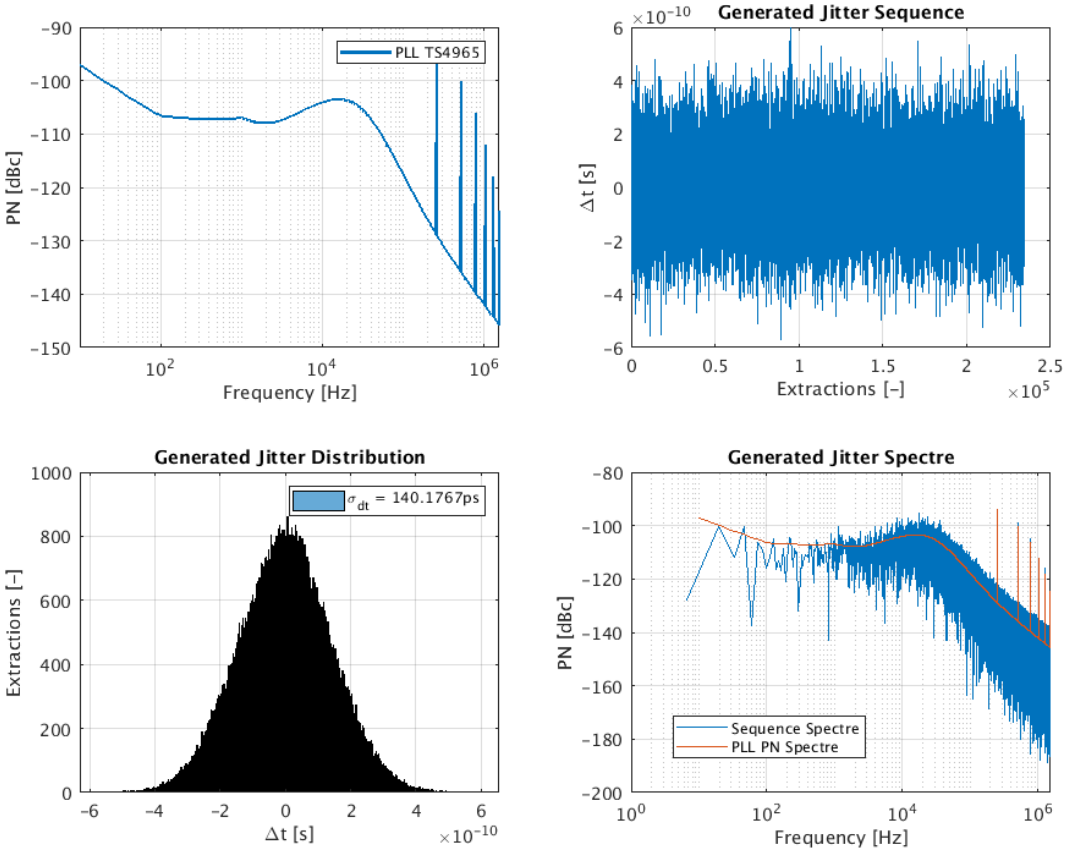

Figure 3.13: Timing jitter sequence extraction from Audio PLL PN Spectrum:
- Top Left: the given PN Spectrum
- Top Right: timing jitter sequence generated
- Bottom Left: histogram of the timing jitter sequence values (notice it is not Gauss)
- Bottom Right: Spectrum (FFT) of the obtained sequence (in comparison with the given PN Spectrum)

The first is about the difficult choice between multi-bit quantizer and single-bit FIR-DAC option. The two techniques introduced in Sec. 3.4.1 and Sec. 3.4.5 were explained from a time-domain point of view. After using our jitter model, the frequency domain can be commented, looking at FFT extracted from simulation. In Fig. 3.14, FFT are performed at the DAC output for both techniques and for a single bit quantizer, meaning a total of three simulations in the comparison. Conditions are exactly the same, only changing the DAC block between the three mentioned. A piece-wise function approximating the PLL PN spectrum introduced in Sec. 3.6.5 is also added in order to visualize the frequency distribution of jitter, which is of course the same for all three simulations.

From these spectra, the intermodulation between NTF and DAC pulse with Jitter can be understood and commented. The single bit case shows a high OBG which inevitably cause noise folding back into the band of interest. If the SNR is degraded too much, as it is probably the case for a CTSDM, using a multibit has the effect of lowering the magnitude of NTF at all frequencies (see Ch. 2, Sec. 2.1.6) so that the intermodulation is simply of lower magnitude as well, at any frequency. The FIR-DAC solution acts in a different way but the concept is the same. If N is the number of taps chosen, then N notches will appear in the oversampling band[17]. The OBG is again reduced, lowering the integrated contribution of jitter folding back to baseband. Once the whole integration is considered, the attenuation due to notches is confirmed to be comparable to that of multibit down-shifting, as long as

[17]From which the visible $N/2$ in the $f_s/2$ band

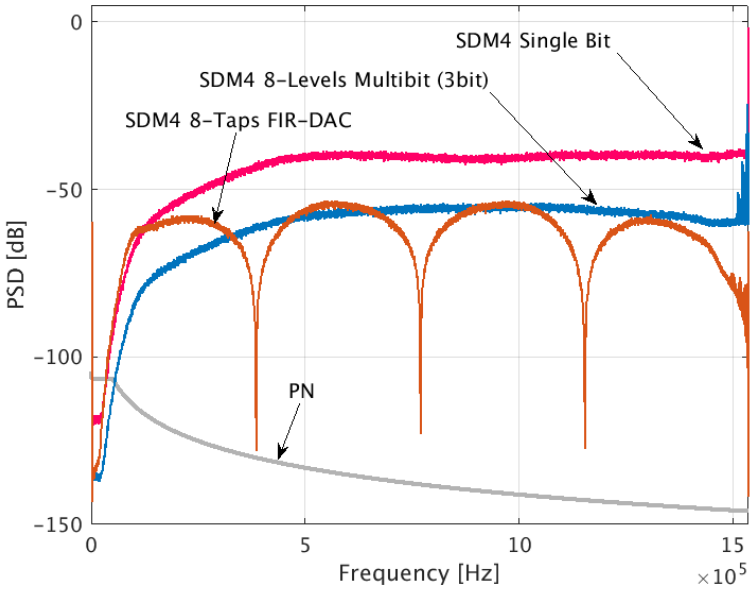

Figure 3.14: Spectra for a same modulaotor with different DAC outputs: single bit (magenta) quantizer, 3-bit quantizer (blue) and 8-taps FIR-DAC. The PN spectrum (grey) is also the same across all three simulations..

the number of taps and quantizer level respect $N_{levels} - 1 = N_{taps}$. The extracted DR on the output PDM spectrum (not shown in figure) is $107.19dB$ for 8-level multibit and $109.07dB$ for 8-taps FIR-DAC. Thanks to the accuracy of the model, we can confirm that multi-bit and FIR-DAC architectures have the same efficiency in reducing jitter noise impact.

The second benefit for the design flow, is also due to the absolute accuracy of the model. It has been shown that the number of taps in the filter can be accurately defined. Fig. 3.15 is the most significant demonstration of the interest of an accurate jitter model.The simulations performed are all in the same conditions, only changing the FIR-DAC number of taps $N = \{0, 2, 4, 8, 16\}$. The same real PLL PN Spectrum defined in Sec. 3.6.5 is injected as jitter noise. The results are shown in Tab. 3.1. To complete the comparison, the 4-Taps simulation has been done also injecting a white noise spectrum characterized by a variance of $\sigma_j^2 = 140psRMS$. This shows again the importance of using an accurate jitter model with the appropriate PN spectrum: the 4-Taps simulations reveals to be sufficiently reducing jitter impact on the modulator, whereas a far worse situation is found if a white noise spectrum is injected. It is even worse than the case with no jitter reduction at all, but with the proper PN spectrum. This accurate model shows quantitatively how much overestimation can be made if jitter is not simulated properly.

At this behavioral simulations stage, the information which could be fixed is that the modulator needs at least a 4-Taps FIR-DAC to have a SJNR compatible with the DR target. Since it is desired to have thermal noise to be the dominant source for SNR budget, 8 is finally the most suitable choice as the minimum number of taps, as 4 keeps SJ(Q)NR as low as 105.14dB, while thermal should be designed to be about 104dB (Ch. 6, Sec. 6.3). Now that the jitter reduction efficiency of the FIR-DAC is known, the design phase can continue evaluating all other impacts that choosing 8-Taps has on performance.

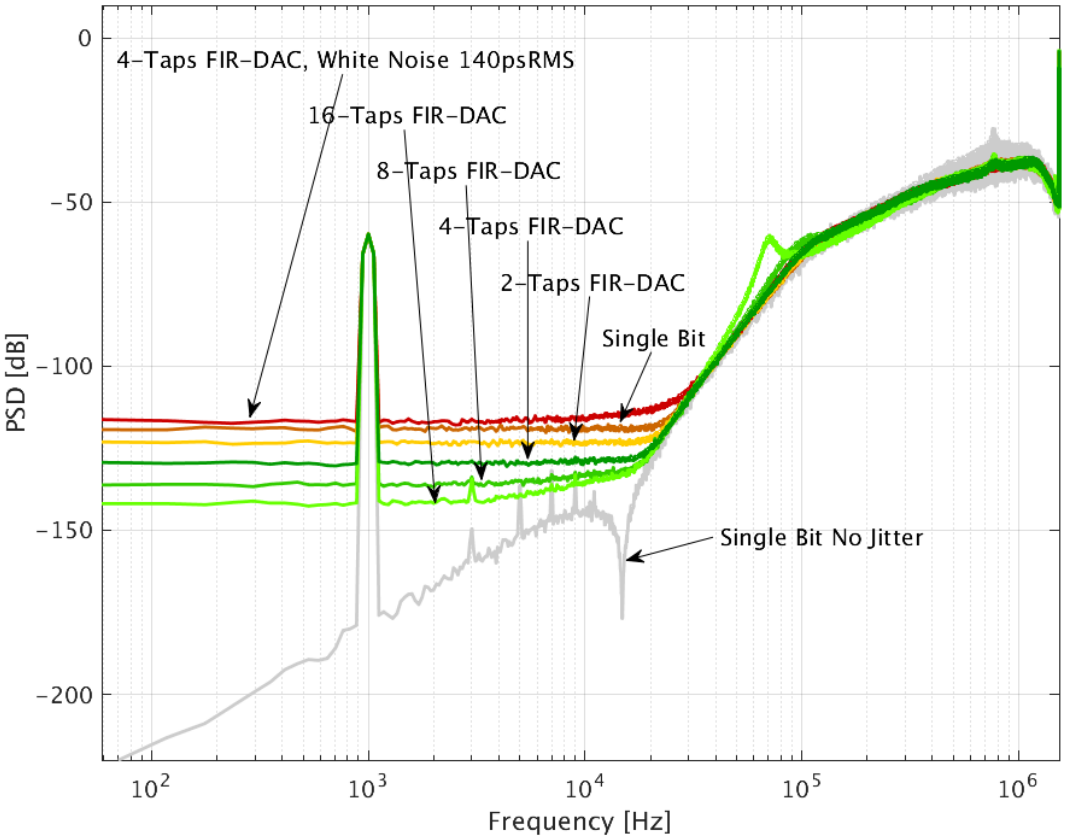

Figure 3.15: Same modulator simulated in same conditions and with the same jitter sequence from PLL PN spectrum, only the number of Taps in the FIR-DAC does change. The 4-Taps case is also simulated with a white distributed noise with the same RMS value of the PLL PN spectrum for comparison.

Table 3.1: Dynamic range with respect of the number of taps in FIR-DAC

Simulation	SNR dB	DR dB	DR+ [a] dB	DR+ 2^n [b] dB
Single Bit	35.62	95.62	-	-
2 Taps FIR-DAC	39.79	99.79	4.17	4.17
4 Taps FIR-DAC	45.14	**105.14**	9.52	5.35
8 Taps FIR-DAC	48.97	108.97	13.35	3.83
16 Taps FIR-DAC	50.24	110.24	14.62	1.27
No Jitter	56.24	116.24	-	-
4 Taps FIR-DAC (W140ps)	31.96	91.96	-	-

Improvement of DR with respect to:
[a]the single bit implementation.
[b]the previous power of 2 number of taps.

Chapter 4

Modulator Architecture

This chapter is dedicated to the description of our system architecture, starting from the previous SC version, focusing on the design objectives of our CT modulator, resuming and summing up peculiar negative and positive aspects of a parameter or characteristic and explaining why certain choices have been made over others.

First of all, the most desired feature was to keep the single-bit quantizer as in CENTO, due to its design simplicity and lower power consumption with respect to multi-bit implementations. Since a low OSR was also preferred, a high order of L=4 has been chosen to recover the SQNR.

The differences brought by a Continuous Time implementation with respect to Discrete Time have also been considered and documented, fulfilling also the interest of ST Design Team to have a DT-to-CT experience and of course, since lately designed ADC were mainly DT, to have knowledge about CT at first place.

A last part is of course the technical consequences of implementing a FIR-DAC, absolutely mandatory for jitter induced noise reduction since a single-bit quantizer represents the worst case possible face to jitter. From the state of the art, it emerges that multi-bit implementations as well, with respect to FIR-DAC, do have similar electrical benefits, such as relaxing the first stage amplifier performance constraint, and quite low power consumption. Therefore, the reason why the desired single-bit quantizer with FIR-DAC is used over a multi-bit solution should be motivated. A more detailed comparison could resolve this question, explaining which benefits are brought by discarding the solid multi-bit choice for the simple and design-friendly single-bit with FIR-DAC.

The choices of having a loop filter order L = 4 and FIR-DAC number of taps N = 8 (coming from previous chapter), have been decided to constitute the nomenclature for the name of the modulator; it has therefore been labelled CTSDM4FD8 (Continuous-Time Sigma-Delta Modulator of order 4, with a FIR-DAC long 8 taps).

4.1 A Foreword about CENTO

High portability audio application was already a subject which interested the ST Design Team. For what concern ADC, a DTSDM named CENTO was developed in 180nm HCMOS9A technology (further information about this technology in Ch. 6, Sec. 6.1): it is a fourth-order single-bit, with a 4-Taps FIR-DAC. This modulator has a DR of over 100dBAw drawing 1220μA from a 2.4V supply (considering both the modulator and reference), which means a power consumption of 2928μW. Oversampling frequency is 3.072MHz, which means an OSR of 76.8 relative to the 20kHz base-band.

In the DT case, jitter is not such an issue: FIR-DAC was implemented to relax specifications for the first Operational Amplifier, lowering power consumption.

A silicon prototype exists and has been tested previous to starting this work. In Fig. 4.1 the layout view is visible, showing a compact structure with an horizontal symmetry axis. The four stages occupy one after another the modulator area from left to right, followed

by the comparator and the FIR filter. Several biasing and signals whose necessity is shared between different zones of the circuit are routed all around.

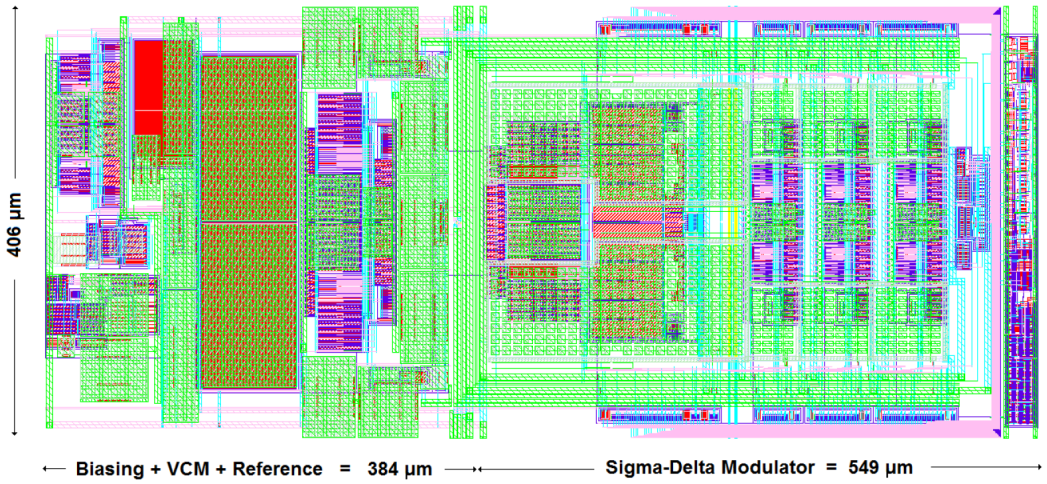

Figure 4.1: CENTO Layout. Modulator and reference block are both included.

4.2 Requested Performances Overview

The new modulator has to be designed in order to comply to the requested DR, considering all degradation sources combined, of at least 100dBAw in the audio band. The design of the decimation filter is not included in the purposes of this work.

The theoretical SNR limit should be dominated by thermal noise and a margin of 3dB in typical has been taken into account for possible degradation such as those due to actual implementation, technological spread, temperature and voltage drift; that is, the modulator has to be designed in order to have the noise contribution no higher than -103dBFS (A-Weighted) in typical conditions. Having fixed this limit, the other degradation sources like quantification noise, jitter noise, NTF drift (due to RC product spread), must have a contribution such as their squared sum with thermal noise will not affect the total for a great amount. In other words all degradation sources other than thermal noise will be designed to make a -110dBFS contribution or lower.

Modulator offset, caused mainly by first integrator input pair mismatch, causes tones to show up in the spectrum. Tones of this kind falling in the base-band worsen audio experience for the listener. The details about offset behaviour will be described in Ch. 6, Sec. 6.4 (in short, the offset value determines the frequency of the tone: the lower the value of the offset, the lower the frequency). Thanks to A-Weighting, the offset compensation can be such as to keep the tones at a maximum frequency of 500Hz where it is already attenuated by a factor of -3dB.

4.3 Main Modulator Parameters Choices

In the following sections, the main theoretical sizing parameters choice are investigated. We remember hereby that they are quantizer levels, loop filter order and oversampling ratio. About the advantages, disadvantages and motivation of the choices made, the following paragraphs are not meant to be exhaustive: new considerations will be discussed all along the following chapters.

Furthermore, this part is for what concerns main modulators parameters OSR, L and b, how b was privileged and OSR and L chosen respectively by consequence. The implementing architectural choices, such as the configuration, the modulator coefficients, the Continuous-

Time implementation and the FIR-DAC are explained in detail one at a time in Sec. 4.4, Sec. 4.5, Sec. 4.6 and Sec. 4.7, respectively.

Number of Bits in the Quantizer

In this section, the choice of the number of bits in the quantizer is explained, in particular, a multi-bit or a single-bit solution could be used. It is hereby justified why the single-bit was preferred, continuing with the consequent DAC choice which is strictly related to quantizer number of bits.

Single bit quantizers are indeed the most simple ones existing as they are implemented with a single comparator, providing just two possible states as output. The use of a single bit quantizer has been the favorite choice since the beginning (and even before, given CENTO architecture). The philosophy behind this choice lies in the simplicity of realisation, the intrinsic advantages and the absence of countermeasures which become mandatory with multi-bit quantizers.

Il semble que la perfection soit atteinte non quand il n'y a plus rien à ajouter, mais quand il n'y a plus rien à retrancher.	It seems that perfection is attained not when there is nothing more to add, but when there is nothing more to remove.

Antoine de Saint-Exupéry

The more complex the design is, the more time and effort has to be spent on the circuit for validation; this means of course a higher cost in every sense. Choosing simplicity whenever it is possible helps to lower the effort made by the designer, at the same time, any complex choice is accompanied by its own risks of implementation. The choice of simplicity is indeed even more preferred in an industrial context where the word simple is associated to robustness. This said, there are more other advantages and of course disadvantages of using a single-bit modulator.

As already introduced in the previous chapter, once comparators and circuits for reference voltage are realised on silicon, drifts and mismatch may occur and in a multibit quantizer thresholds at which comparators commute correctly may shift, individually. This means that some input ranges/intervals of values shift from being represented by a code to another.

So the first advantage is surely the so called *inherent linearity*. This property is a well known and interesting feature of having just 2 levels, because there would certainly exist a straight line passing through both these points.

A single bit provides directly a serial (PDM) output, while at the output of a multibit a bus of bits is present. The great majority of audio products interface with a serial single bit signal, which means that any multi-bit quantizer SDM will need a structure (actually a DAC) to reduce the bus word to a serial stream, adding of course more power consumption. A single-bit quantizer SDM does not need any other interfacing structure, as it is already providing a bit-stream (PDM) as output.

With a multi-bit quantizer, the scaling of the last stage is relevant, as the quantizer has to discriminate voltage intervals all along the output voltage swing of the last integrator. A single-bit quantizer is just a comparator with a threshold corresponding to half the last integrator output swing, so it operates *just on the sign* of the signal it receives as input. This makes the final stage scaling irrelevant, the designer may then choose the value of resistors and capacitors as it is more convenient.

NRZ Feedback DAC Pulse

The feedback DAC pulse type choice is very important for what concerns jitter; notice that the term *type* denotes a different concept with respect to spectral shaping. It applies on any number of bits (and to any number of taps in the FIR-DAC). The most common

feedback DAC pulse types, here considered and put in comparison, are the Non-Return-to-Zero (NRZ), the Return-to-Zero (RZ) and the Half-delayed-Return-to-Zero (HRZ) DAC pulse types and their characteristics are shown in Fig. 4.2 for a short PDM example (11010), highlighting all the transitions affected by jitter.

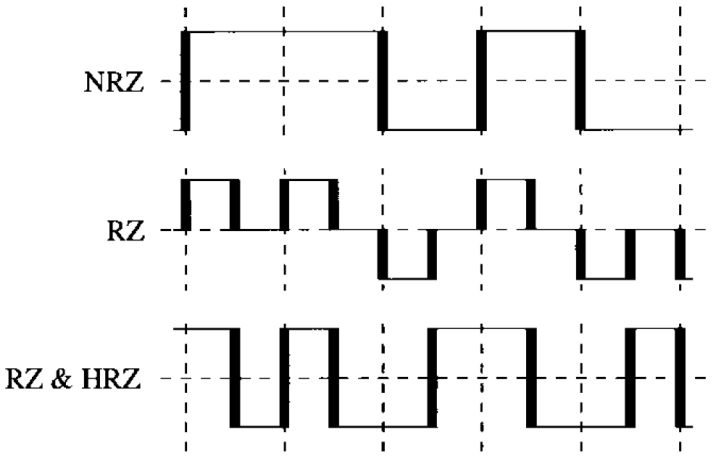

Figure 4.2: Error sequence energy in different types of modulator [36].

The NRZ type is the simplest type, consisting in transitioning from the previous to the next sample. An interesting fact about this implementation is that if two consecutive outputs are identical, no transition occurs at all. Specifically, in a single-bit a Full-Scale (FS) transition occurs only if the quantizer input signal changes sign.

The RZ type resets to half-FS-voltage at half the clock period, after actual transition for each sample: at each clock period, both a rising and falling edge are necessarily present. These transitions swing from half-FS to the quantizer output voltage corresponding to the input at that given instant. In a single-bit it means that, each clock period, a half-FS voltage swing transition appears in both a rising and falling edge. This DAC pulse type is used to avoid the asymmetry effects due to the difference between rising and falling edges.

The HRZ is just like the latter, but the whole process is half-delayed, that is, it occurs on the second half of the clock period. It is instead interesting to think about HRZ as a combination of both RZ and HRZ of opposite sign because they appear in some multifeedback band-pass modulators [36] and because of the following insight.

Let us consider the simplified jitter calculation for a CTSDM proposed in Ch. 3, Sec. 3.2, Eq. 3.8. It can be found that the SJNR depends on the term $\sigma^2_{\delta_y}$ which represents the statistical occurrence of a transition of the quantizer[1] and, consequently, the proportional energy injected by jitter. Still in the work from Cherry and Snelgrove [36], a very short sequence of bits is considered to make an example, demonstrating that the occurrence of transitions N result in different values of $\sigma^2_{\delta_y}$ for NRZ, RZ and HRZ (+RZ) of respectively 2.80, 8.00, 24.10 (factor that multiplies the voltage step). It is self evident that when jitter is the major issue, a NRZ should definitely be chosen and this discussion drove our choice this way.

In any case, for a single-bit quantizer, this is not even close to be sufficient to withstand jitter impact. Simulations carried on in Ch. 3 are clearly showing that all the advantages of using a single-bit are prevented by jitter degradation: at this point, the choice of using a multi-bit quantizer would be the only option, if another jitter reduction technique was not fitting the single-bit solution. The definitive choice of a single bit can only be validated in Sec. 4.7 where the FIR-DAC employment benefits on jitter are resumed.

[1] A single-bit, for further simplicity

Oversampling Frequency and Modulator Order

Consequently to the choice of using a single-bit quantizer, the SNR has the lowest contribution possible from the parameter b. It therefore has to be recovered (see Ch. 2, Sec.2.1.3) with Oversampling Frequency and Modulator Order. In order to assure the 100dB DR, there exist several combination of the latter two parameters OSR and L.

As seen in Ch. 2, Sec. 2.5.2, the sampling frequencies which are mostly found in audio SDM are around 3.072MHz and 6.144MHz, which represent an OSR factor around[2] 64 and 128 respectively.

The oversampling frequency of 3.072Mhz has been chosen for this work. Driving this choice is the awareness of the fact that, though the modulator block is the only object of the design, in a following complete circuit many others blocks clocked at this frequency would be present. Since low power consumption and low surface budget are to be thought on the overall device, a moderate OSR has been thought to be more convenient. To make an example: if we chose 6.144MHz as oversampling frequency, the decimator filter would operate at double the frequency, so this contribution would be at least the double. However, there are several other sources of power consumption concerning the clock tree that complicate the estimation. In any case, since the OSR choice affects the whole circuit instead of the modulator block only, it has been decided to prioritize this parameter over the modulator order.

Thus, since we preferred to fix both parameters b and OSR, the only remaining parameter L should now be sized consequently (Ch. 2, Sec. 2.1.7). Simulations at high level of modeling revealed that no less than a fourth order is required to ensure a convenient margin for SQNR. A fourth order noise shaping can be obtained either with a single stage fourth order internal loop or with two cascaded two-stage modulators, that is, a MASH-2-2 configuration. The MASH structure has been discarded since the beginning because, especially in a continuous time, it is difficult to match [60] the noise shaping transfer functions in order to obtain a proper noise cancellation. A single-stage fourth-order modulator was then chosen.

4.4 CIFB-FF Configuration

Most recent works prefer a Cascade of Integrators in Feed-Forward configuration (CIFF), eventually adding one additional feedback path (CIFF-FB). This is an advantageous structure as it allows to scale coefficients to have low absolute values, lowering *stress* on internal state nodes, such as voltage swing or current calls. This allows the amplifiers to economise on power consumption, eventually allocating just a few μA on each stage.

On the contrary, in our case a Cascade of Integrators in Feed-Back configuration with additional Feed-Forward paths (CIFB-FF) is used. This choice may appear to be against our guidelines: such structure implies having an important swing on internal nodes as well as current calls from amplifiers, which makes necessary to dedicate more power budget to them. This distancing from strictly keeping power consumption the lowest possible is all due to an empirical stability criterion which has been studied for high order SDM. The latter, if met, allows to guarantee that the high order modulator is intrinsically stable and that whichever abrupt signal or stimulation it receives, it can in any case immediately recover. The whole Ch. 5 is dedicated to stability and the aforementioned criterion, as for now, the concept lying behind this choice is that an intrinsic stability allows to recover from abrupt transition immediately, which means that the audio data will not contain possibly uncomfortable patterns for the listener, such as clicks and pops. It is therefore true that a loss in power consumption exists: referring to the upcoming Tab. 6.4 in Ch. 6 it can be noticed that current consumption of amplifiers is between $10 \div 100\mu$A, while in the state of the art, due to the lower swing found in CIFF structures, amplifiers can consume as low as in the $1 \div 10\mu$A range [61] . The quality of audio data is a feature that deserves more attention than less power consuming.

[2]These factors are labeled as 64 and 128 but it depends on which audio band is considered, 20kHz or 24kHz for example. In our case, all the considerations are made about a 20kHz band, so actually OSR = 76.8.

4.5 Modulator Coefficients

The NTF chosen for CTSDM4FD8 modulator is realised by properly setting the coefficients in the previously chosen structure, whose scheme is visible in Fig. 4.3. This transfer function is desired to be a fourth order, spreading just one complex conjugated zero couple in-band to improve SNR. The CIFB structure is fitted with two feed-forward paths, making it a CIFB-FF as introduced earlier, to improve stability (Ch. 5).

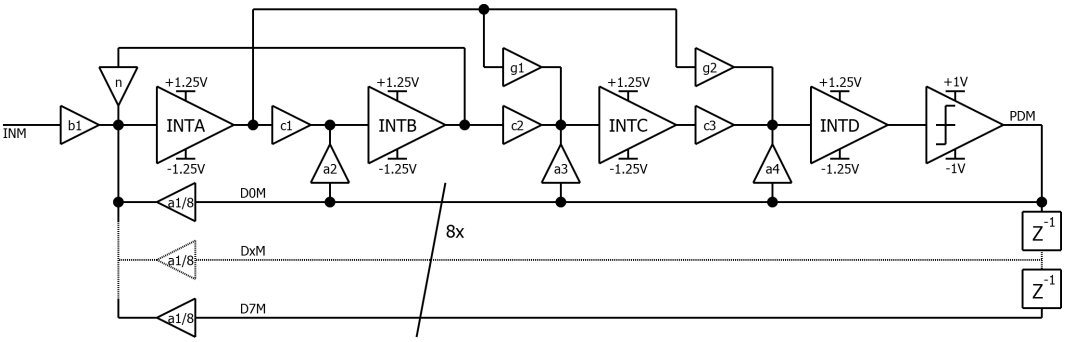

Figure 4.3: CTSDM4FD8 modulator layout and coefficients.

With the exception of the one labelled n, all coefficients correspond to those *classically* obtainable[3], reported in Tab. 4.1 expressed in two factors: the first is the actual modulator NTF synthesis coefficient and the second is the stage scaling.

Table 4.1: Modulator Coefficients

Label	*Value*	*Label*	*Value*
$b1$	$47/49 \cdot 9/50$	$c2$	$4/7 \cdot 7/15$
n	$*$	$a3$	$1 \cdot 7/15$
$a1$	$1 \cdot 9/50$	$g1$	$2/7 \cdot 7/15$
$c1$	$2/3 \cdot 1/4$	$c3$	$4/5 \cdot 5/12$
$a2$	$1 \cdot 1/4$	$a4$	$1 \cdot 5/12$
		$g2$	$2/5 \cdot 5/12$

The n coefficient is the one responsible of spreading the zero of the NTF from DC towards the band. This practice is very common in any SDM as it improves the inband noise figure, consequently the SNR as well. Providing an optimal positioning of the zeroes in the band of interest, the latter is always true and as the modulator order grows [62] the benefit become more and more interesting. The zero is spread by creating second order sub-structure within the loop filter by the mean of a path which coefficient n is calculated as follows:

$$\frac{1}{n} = \frac{f_s^2 \cdot c_1}{(2\pi \cdot 0.789 \cdot f_B)^2} \tag{4.1}$$

where f_B is the audio 20kHz bandwidth. In practice, the important part of this formula is that it is placing the zero doublet at a certain frequency in proportion to f_B: the coefficient 0.789 is chosen[4] to optimize the in-band integrated noise when a single zero-doublet is present.

[3] For example with Schreier Toolbox for sigma-delta design and simulation.
[4] On the 20kHz band it means having the in-band notch at 15.78kHz.

With these parameters, the NTF can be calculated (via MATLAB symbolic equations) and represented graphically in Fig. 4.4, where both a simple single-bit quantizer and the average operation provided by the FIR-DAC are included (the comparison between these two will be commented in Sec. 4.7.3). The following step is to simulate an SDM at behavioral level to verify the correct operation of the structure chosen. A standard simulation in

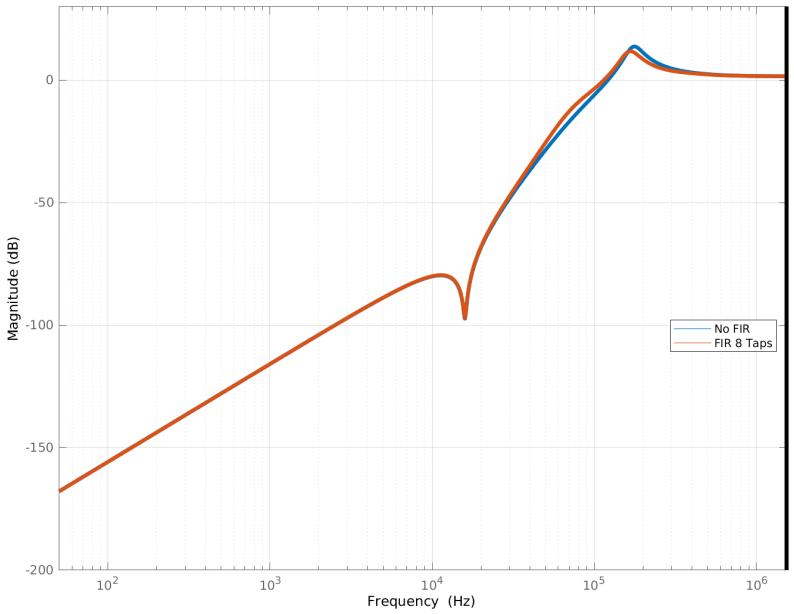

Figure 4.4: Calculated CTSDM4FD8 desired NTF, with and without FIR-DAC.

MATLAB with -60dBFS input signal manifests SNR=58.4dB, which means DR=118.4dB can be extrapolated; the point SNR_{MAX} occurs at an input signal power of -3dBFS. This is a valid checkpoint: next step is to perform electrical simulations, as will be seen in Ch. 6.

4.6 From Discrete-Time to Continuous-Time

At the very beginning of this work, the scenario is the existence of a correctly performing DTSDM prototype, for which a lower power consumption is desired. CTSDM are well known to be, due to the continuous-time nature, lower power consuming with respect of their identical DTSDM counterpart. That is, when the architecture step is validated, the designer has to choose to implement it either in Discrete-Time or Continuous-Time. Under the point of view of power consumption the choice is absolutely clear and this is why developing a continuous time version of CENTO is of great interest: if any design challenge relative to a CT implementation can be addressed successfully, lower power consumption is guaranteed with respect to the DT case. The benefit of the latter is twofold: it can demonstrate that the audio product associated with CENTO can be improved in power consumption and it can provide to the ST Design Team an expertise on CTSDM and DTSDM-to-CTSDM conversion flow, as nowadays all products have been designed and realised with a Switched-Capacitor implementation.

The reasons why there exist this intrinsic lower power consumption will be explained in detail in the following Section, along with all other possible advantages and disadvantages of the two opposite implementations. After that, everything that should be changed and adapted when converting a DTSDM to a CTSDM will be explained in the subsequent Sections.

4.6.1 Advantages

In a CTSDM, the loop filter is implemented with continuous time integrators, in our case Active-RC. The only sampling operation occurs at the quantizer, that is, the signal path goes through a lowpass-filter before being sampled. It is not the case in a DTSDM, where each stage is built in switched-capacitors and sampling occurs therefore at the very input of the modulator. This last scenario makes necessary to anti-alias filter the input signal before entering the sigma delta. In the CT case the same task is accomplished intrinsically by the internal loop filter itself [63] [64] for the structural reasons just cited, therefore no anti-alias filter is needed before the modulator, which means saving power and surface.

Another important advantage coming from the absence of the switching operations is about the circuit requirements for states evolution: at each sampling instant, in a DTSDM the internal states are updated by discharging sampling capacitors on feedback capacitors and the signal is therefore impulsive. It is then up to the amplifiers to provide that the charge is properly transferred without any loss. In CTSDM currents are continuously flowing through the internal loop filter and the charge information is then distributed all over the period, providing a smoother operation in the loop filter. This relaxes the requirements of bandwidth and slew rate of the amplifiers consequently allowing them to reduce power consumption. For example, the bandwidth could be in some cases (see Ch. 2, Sec. 2.2.1) as low as the oversampling frequency, while in the switched capacitor case a factor of 8-10 on the oversampling frequency is a proper bandwidth choice.

It is worth spending a word about feedback DAC pulse in a CTSDM: it is true that the waveform of a NRZ is impulsive, but still comparing with Ch. 2, Sec. 2.2.1, it can be found that having this signal to slew or have a slower rise time has a permissive margin of tolerance given that the whole period continuous integration is available.

4.6.2 Downsides

Due to the continuous operation, in a CTSDM each sample should be accurately integrated during the whole period. Then, there exist issues that do not necessarily affect or which impact is negligible in a DT implementation become of primary importance when moving to CT. These non-idealities have been already cited (Ch. 2, Sec. 2.2) and are resumed here in order to highlight these advantage-downside sections.

The major problem in choosing a CTSDM over a DTSDM is jitter: it has been explained in detail in Ch. 3 and it is really important for the designer to be aware that a great part of design effort will have to be dedicated to solve this issue while converting from DT to CT.

By the same integral corruption concept, Excess Loop Delay (ELD) seen in Sec. 2.2.5 has to be discussed. Audio applications SDM are clocked at a frequency in the order of MHz, so it is not difficult to design a comparator which is fast enough for a DT implementation: even with a half period delay, the charge information could have the time to be integrated on feedback capacitors of any integrator in the loop filter. It is not the case for a CTSDM where ELD must be taken into account (Ch. 6. Quantizer metastability has also been shown, as it is an issue which mechanism is similar to ELD and is as well a non-ideality affecting only CT implementations. The reason why DT is robust against quantizer metastability is because the integral information settles to a fixed value which is then sampled (refer to Ch. 3, Sec. 3.2), therefore, the comparator does have a larger amount of time to make its decision with respect to CT case, because the moment of the sampling period the information is processed is not relevant as long as it is successfully completed before the following sampling instant.

The other most relevant issue in a CTSDM, which is actually still, again, due to proper integration concept, is the technology spread on the RC product of each integrator, which causes the drift on coefficients and, consequently, on the NTF. In DTSDM coefficients are synthesized using capacitor ratios, which is the ratio between each capacitor of an input branch of an integrator and the corresponding feedback capacitor. When affected by technology spread, since all capacitors are designed with the same device kind, the drift will be moving all values in the same direction and by roughly a same factor, preserving the ratio,

leaving mismatch as the only (fairly controllable) preoccupation. In CTSDM, the devices are of a different nature (resistor and capacitor), they can therefore spread independently, forcing the designer to trim the RC Product.

4.6.3 Equivalent resistors and noise

If a DTSDM is available, to obtain a CT version from it, the designer could definitely think that it would be sufficient to substitute sampling capacitors with an equivalent resistor. Though the substitution operation is actually the *only* step, device-wise, necessary for DT-to-CT conversion, the value of the newly placed resistor is not immediate as proven by the following argument. The substitution principle lies on the fact that, during a single sampling cycle, a sampling capacitor may be thought as a device which is crossed by a current flow, while kept at a certain voltage difference. The charge exchanged is $Q = CV$, that gives a mean current of $I = CV/T_S$. This could be associated to the behaviour of a resistor of value

$$R = \frac{T_S}{C_s} = \frac{1}{f_s \cdot C_s} \tag{4.2}$$

and if this substitution was performed over all the input sampling capacitors present in the loop filter, the results would be to obtain an equivalent modulator. Notice that, however, the equivalence is not complete: by the principle of DT and CT state evolution equivalence, more steps should be taken [65] if we wanted to obtain the same exact modulator, that is to say, if we wanted a CT modulator that gives the same identical output of its DT counterpart sample-to-sample.

Moreover, intrinsically, thermal noise performance would not be the same. Let us calculate the Noise Ratio between a sampling capacitor and a resistor on the same band of interest:

$$\rho_N = \frac{N_{R,RMS}}{N_{C,RMS}} = \frac{\sqrt{\int_0^{f_B} df \overline{v_R^2(f)}}}{\sqrt{\frac{k_B T}{C_s}}} \tag{4.3}$$

We keep on hold Equation 4.3 to comment about the integral limits f_B: For Resistances, it is the very band of interest (20kHz audio), since out of band noise is filtered, while for a switched-capacitors circuit the integral gives the same result regardless of its limits, since the high frequency noise is aliased in the band. Notice also that this is done without considering A-Weighting filter, in order to highlight folding of high frequency noise in the base-band of a sampling operation. About the absence of the A-Weighting filter there is a Comment in the Appendix A. This therefore leads to:

$$\rho_N = \sqrt{\frac{\int_0^{f_B} df 4k_B T \frac{1}{f_s \cdot C_s}}{\frac{k_B T}{C_s}}} = \sqrt{\frac{\frac{4k_B T}{C_s}}{\frac{k_B T}{C_s}}} = 2 \tag{4.4}$$

This shows that the modulator will have the same thermal noise performances only if the resistors substituting sampling capacitors will have half the value of the equivalent resistors[5]. The only exception is the resistor synthesizing the n coefficient which has to respect the following condition

$$R_N = \frac{f_s \cdot c_1}{C_A \cdot (2\pi \cdot 0.789 \cdot f_B)^2} \tag{4.5}$$

because the value is uniquely determined by resonance of the second order structure.

[5]Consequently, integrators feedback capacitors values being doubled.

From this discussion, it emerges that when a direct DT-to-CT conversion is performed, the designer has to take into account a factor of 2 on thermal noise. The correct conversion flow is instead to substitute all input sampling capacitors with the corresponding resistor value divided by 2. Notice in particular, that all feedback capacitor have of course to be increased by a factor 2 as well. This should be absolutely taken into account to forecast surface budget, since, as explained in the next Sec. 4.6.4, the factor of 2 refers to the nominal value, but even more surface is necessary to implement proper trimming. To anticipate results obtained in Ch. 6, Sec. 6.6.2 an overall +170% is necessary for feedback capacitors with respect to the starting DT implementation.

4.6.4 RC Product Trim

As introduced so far, in a DTSDM the loop filter is Switched-Capacitor and coefficients are implemented through ratios between each input capacitor and the feedback capacitor of the corresponding integrator. All the capacitors can be implemented with the same kind of device chosen among those available in the design kit. Technology spread will affect all capacitors *in the same direction*, which means that the the ratio parameter has been robustly implemented.

In a continuous time implementation, let us consider a generic coefficient k: it is now synthesised by the RC-Product of its own integrator path, obeying to the following equation

$$k = \frac{1}{R_k \cdot C_k \cdot f_s} \tag{4.6}$$

Capacitors and resistors suffer from technology spread independently, so in this case the RC product will be the combination of the two. Given the normal technology spread values (Ch. 6, Sec. 6.6), there will likely be an intolerable change in the NTF. The designer has to trim the RC-Product according to the following two steps (explained hereafter and applied later in the transistor phase design, Ch. 6).

Step One: force a spread in R, C or both in a standard simulation (Ch. 2, Sec. 2.4.1) and determine what is the relative deviation which is tolerable, that is, the maximum deviation for which the subsequent drift in NTF which will not bring too much degradation (Ch. 2, Sec. 2.2.2).

Step Two: Trim the RC-Product in order to provide the necessary accuracy and to cover all the worst case combined spread of resistors and capacitors. Generally it is done by implementing programmable resistors or capacitors[6]. According to the calculation procedure, there will be a certain number of RC values possible with their own unique calibration code. These values shall be evenly spaced and the step between two subsequent values determines the accuracy. During this step, it is important to take into account any combination of spread and resistors and capacitors varying independently also determine absolute *upper* and *lower* worst case for the RC Product value. The accuracy of trimming also needs to be cared about. This last arguments will be clearer in Ch. 6, Sec. 6.6.2, which is dedicated to handle all of these aspects.

4.7 FIR-DAC

It has been highlighted many times in this work that jitter is a major issue for CTSDM and the analysis of its impact has been exhaustively covered in the previous chapters. In the same manner, the countermeasure has a great relevance with respect to other design choices. This is why the FIR-DAC has been dedicated a more detailed insight, carried on in this section. The characteristics of a FIR-DAC are first introduced, then the implementation (at high/behavioural level) is illustrated. After that, performance against jitter, the most interesting benefits and the particular attentions necessary to compensate the consequences

[6] It is quite obvious that the choice will be trimming capacitors, due to simplicity with respect to trimming resistors. This will be explained in detail in Ch. 6.

of including a FIR-DAC in the feedback path of a CTSDM will be reported.

An FIR-DAC is a DAC which, instead of updating the loop filter feedback signal with a 1-bit DAC, filters this 1-bit DAC output PDM through an analog-implemented FIR.

Coefficients of the FIR can in principle be optimized [25], but the effects of such procedure become visible with a very high number of taps. It will be clear from Sec. 4.7.3 that the lowest value possible for FIR-DAC number of taps N is preferred. The most interesting solution is to choose each of the coefficients to be equal to 1/N. This configuration is also known as performing a moving average. The reasons are manifold:

- The choice is solid, performing and extremely simple to understand and to implement
- Matching between coefficients is simpler to obtain, since each switch and resistor are devices with exactly the same physical characteristics
- Surface of the resistive feedback DAC results to be lower [13] than in the case with different coefficients. The resistors would have to be of different shapes and their placement would become more complex under the point of view of layout
- Thanks to the notches being evenly-spaced in frequency, the moving average implementation is compatible with chopping technique [66] if desired

The feedback signal will therefore be the average of the present and the past N-1 samples, where N is the number of Taps the FIR is designed with. Thanks to the simulations carried out in Ch. 3 shown in Fig. 3.15 and summed up in Tab. 3.1, the design choice for the FIR-DAC fitting this CTSDM is 8 taps. Since it can be noticed that 4 is sufficient to reach 100dB of DR, it is worth commenting that the simulations take into account jitter and quantization noise but not thermal noise. The choice of N=8 is done forecasting a square sum of the contributions with thermal noise, which will be carried out in Ch. 6. In order to ensure 103dB of DR (that is, 3dB of margin on the target) the 105dB obtained in Tab. 3.1 are not sufficient.

This choice of 8 for the parameter N completes the definition of our modulator, which has been chosen to be named CTSDM4FD8.

4.7.1 Implementation

This structure is implemented in a semi-digital way. It means that delays are D-Flip-Flops (FFD, digital elements) which drive the analog DAC switches. The FIR is realised as in Fig. 4.5 where it can be noticed that register holds samples alternating between Q and $\overline{Q}$ (NOT-Q). This is done to simplify the *analog VCM reset* condition at startup, where VCM is the analog common mode set at half the voltage supply. In fact, in the same figure it can be noticed that the reset signal is unique and at the circuit startup is as a matter of fact active. In a reset condition, each FFD does have $Q = 0$ and $\overline{Q} = 1$ no matter what D is nor at what phase of the clock C has as input. If each[7] FFD input D was connected to the previous FFD Q output, the reset condition would be "00000000" which means all DACs would be switched to negative reference voltage[8]. Since the modulator is most likely to be fed by VCM-centered signals (which are also eventually low input power), this would mean the filter needs some time to settle from the output analog value of -1V (lower reference voltage) to VCM at conversion startup. If D inputs are connected alternating each previous outputs between Q and $\overline{Q}$, the FIR reset condition is "01010101", consequently having half the DACs switched to negative reference and half to positive reference voltage. This sets the startup voltage at VCM. There is no drawback in this alternation, because the digital information in the even positions of the FIR filter is just negated: it can be simply negated again, in order to drive their DACs correspondingly.

Arguments about the implementation of the whole FIR-DAC structure will be concluded in Ch. 6.

[7] Except of course the first.
[8] Thinking of it as differential.

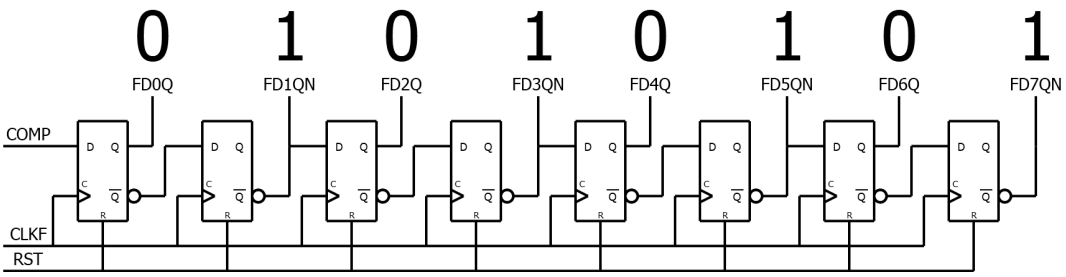

Figure 4.5: FIR-DAC FIR filter implementation with *analog-zero reset* feature.

4.7.2 Performance with Respect to Jitter

In chapter Ch. 3, jitter impact on a CTSDM has been studied. The principles of FIR-DAC jitter reduction and its efficiency have also been described. The conclusion drawn from the performed accurate jitter simulations is that under the point of view of jitter reduction, an 8-Taps FIR-DAC acts exactly as a 8-level (3-bits) multibit quantizer. How a FIR-DAC performs against jitter is just a matter of number of Taps in the FIR filter. Here, Fig. 4.6 is proposed to integrate Tab. 3.1 and show how SJNR improves from a spectral point of view. Each Tap in the FIR adds a notch in the spectrum. For N Taps, N notches are present in

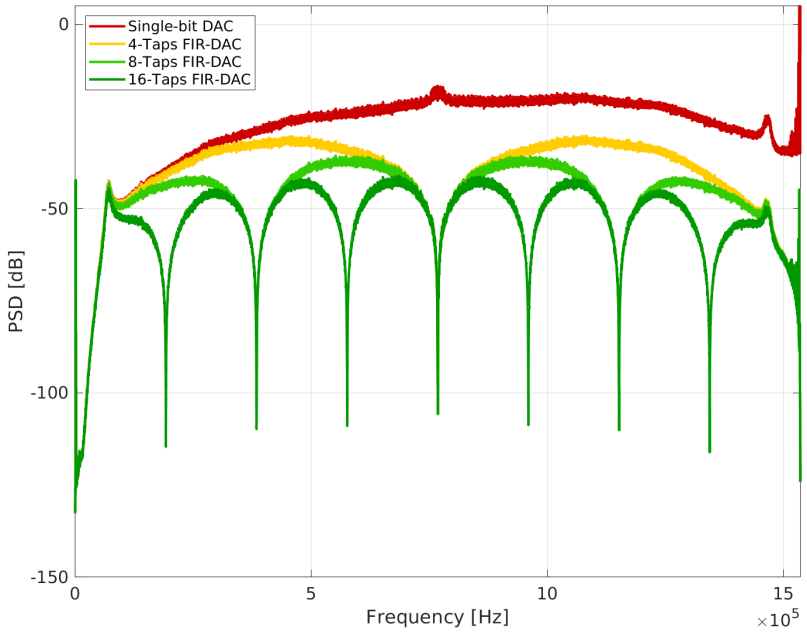

Figure 4.6: FIR-DAC output spectra for different number of taps N. Adding more notches lower the out of band gain of the NTF which intermodulates with jitter.

the 0 to f_s and their frequencies, as long as the coefficients are all the same and equal to 1/N, are

$$f_{n_k} = \frac{k}{N} \cdot f_s \qquad k = 1, ..., N \tag{4.7}$$

As N grows, the presence of more and more notches progressively lower the OBG, thus also the component of intermodulation with jitter phase noise spectrum folding back in the base-band is lower.

Chapter Ch. 3 ended in finding the minimum number of taps necessary to obtain a modulator capable of reaching 100dB dynamic range, which was 4. Then it has been fixed to 8 to assure thermal noise dominance in the budget. However, it has not been justified

why higher values of N have not been considered. The answer on the upper limit of Taps number N is explained in the next section.

4.7.3 Delay Impact on Modulator

Still referring to Tab. 3.1 in Ch. 3, the 16-Taps simulation seems to be a good outcome for our purposes. It is however better to keep the number of taps as low as possible once the jitter reduction specification is achieved. Indeed the longer the FIR filter is, the longer the delay between feedback and input signal will be. This delay leads to possible instability of the modulator, in first place, and performance-wise, to a modification of the NTF and STF. For what concerns the NTF, the representation found earlier in Fig. 4.4 shows an interesting comparison, as it allows to verify the drift occurring as the the 8 taps FIR-DAC is introduced. It can be noticed that, concerning the desired transfer-function, the influence of the FIR-DAC is tolerable. In Fig. 4.7 a wider comparison is shown, for both NTF and STF and for more examples of N.

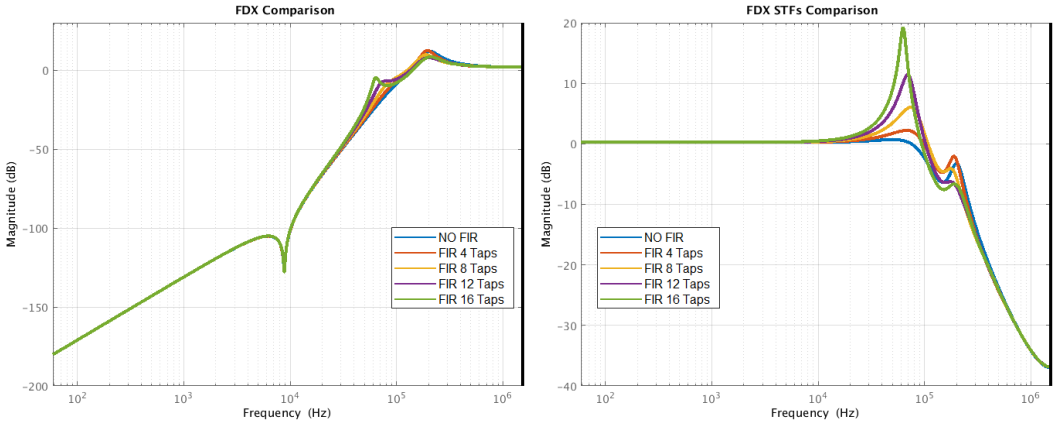

Figure 4.7: NTF and STF of CTSDM4FD8 calculated in MATLAB with symbolic equations with different number of Taps N in the FIR-DAC. As N grows, a more severe gain peaking arises.

The N=16 case is particularly interesting as the gain peak significantly increases.

In these transfer function analysis there is no trace of significant changes in-band, so this could erroneously lead to the point that the SNR would not be degraded by indefinitely augmenting N. However, a different behavior is instead visible once the modulator is simulated: referring to Fig. 3.15 it can be noticed that as N grows, a form of degradation occur at the edge of the audio band, next to the fourth order slope. This effect shows that the SJNR improvement while increasing N parameter *saturate*: from N=4 to N=8, for instance, the SJNR improvement is more advantageous than from N=8 to N=16 (still referring to Tab. 3.1). Notice that this also means that the theoretically expected improvement found in Eq. 3.14 reveals to be no more valid in actual simulations. Basing on these facts, it appears that simulations give complementary information to transfer function analysis.

This behavior has been investigated further in work [27], where a compromise has been found. That is, there exist a number of Taps N which is optimal, SNR-wise. There exist no mathematical proof of this existing minimum and its expression. As a conclusion, several simulations changing the parameter N should be performed and analysed in order to find the optimal value. The design method used for CTSDM4FD8 remains to choose the minimum number of taps possible, that is, the minimum value of N once a sufficient SJ(Q)NR is reached in simulation.

Delay Compensation

A delay compensation for the presence of a FIR-DAC has been already proposed in [25] [13] [27] and consists in two combined operations:

- add a compensating FIR-DAC on feedback path
- tune feed forward coefficients

This process can reveal itself to be complicated, with a lot of algebraic passages that can be found on [25] and [27] and that are *simpler* due to the fact that a single feedback path other than the first stage is present. These calculations are needed to define the new coefficients not only for the feed forward, but also for the compensating FIR-DACs, because even if the first stage FIR-DAC is chosen to have all coefficients equal to 1/N, the compensating are still to be calculated [25].

During this work, a study has been carried on concerning one of the two operations presented earlier in this section: tuning feed-forward coefficients. The outcome can be observed in Fig. 4.8: the NTF and STF are plotted for N=8 and also for N=16, where the gain peaking should be more severe. This is to show how changing the feed-forward coefficients g_1 and g_2 can compensate peaking introduced by the FIR-DAC. Alongside a

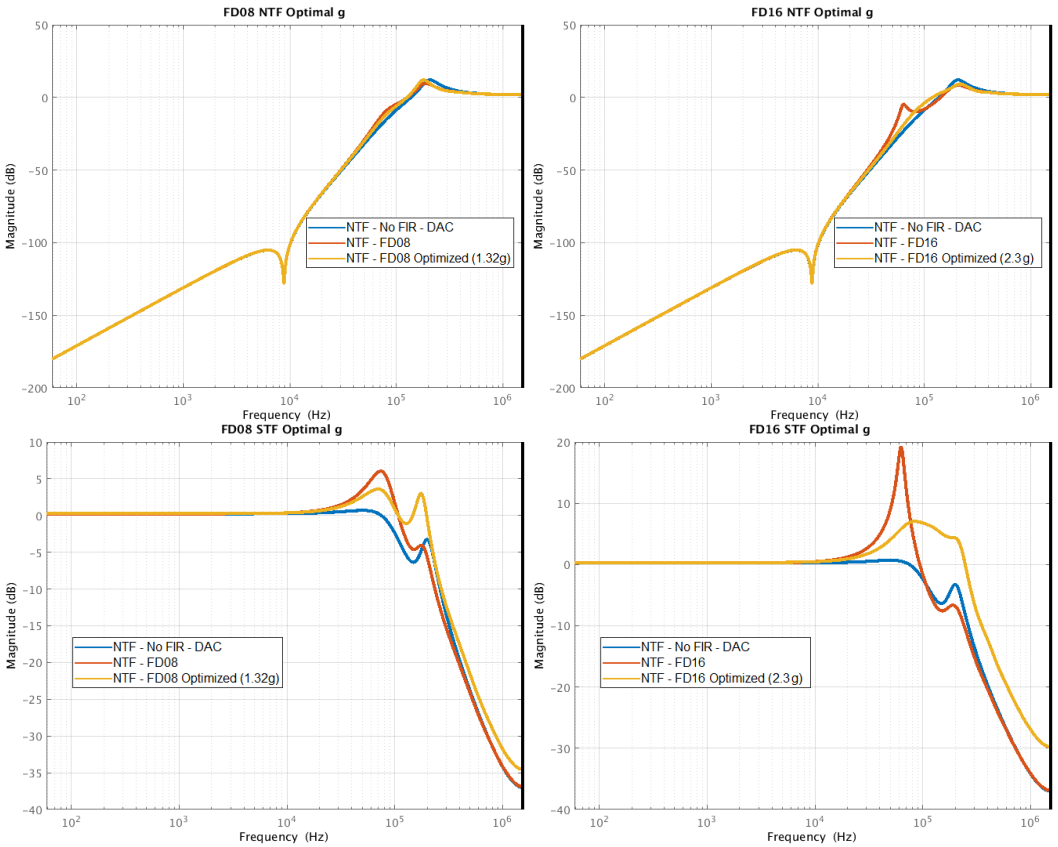

Figure 4.8: NTF (top row) and STF (bottom row) of CTSDM4FD8 calculated in MATLAB with symbolic equations with for the N=8 (left column) and N=16 case (right column). in the FIR-DAC. The best compensation combination of the two feed-forward paths coefficients shows a great improvement for N=16, while for N=8 it is less incisive in comparison.

matter of simplicity, another reason why g_1 and g_2 were not changed to compensate the delay is that the values chosen in Tab. 4.1 come from adapting the previous CENTO design. In particular, they are known to be determining stability conditions, in a way which will be explained in Ch. 5.

However, the most interesting aspect emerging from these transfer functions, is that the drift due to the 8-Taps FIR-DAC introduction is not important and leaves shaping and performance against quantization noise almost unchanged. This allows to avoid performing the other operation cited at the beginning of this section: adding a compensating FIR-DAC on feedback paths. This is an advantage since the structure is a CIFB-FF with four feedback

paths, meaning that three different additional FIR-DACs would be needed for compensation. A total of 24 coefficients would need to be found, since the compensating FIR-DACs must have the same number of Taps [27] in the FIR. It will be also self evident from Ch. 6, Sec. 6.10 that adding this structures would increase the outer region of the modulator layout by at least a factor of 4, eventually making connections unfeasible.

The choice about this point for CTSDM4FD8 remained tied with the concept of leaving the design the most simple possible, in-line with the *industrial* simplicity-robustness duality. Since, as already analysed for our modulator, the FIR-DAC did not reveal a significant drift neither in calculations nor in simulations, there was no need of any further compensation: here , again, while oriented towards the industrialisation of a circuit, the main objective is not to excel and optimize to the best every parameter or feature, but to guarantee a correct performance while best fitting the requisites under the point of view of costs, circuit complexity, power consumption, surface budget and so on.

4.7.4 First Stage Relaxation Benefit

Most benefits brought by the employment of a FIR-DAC are due to the average mechanism. Since the output is the average of the quantizer output with the previous N-1 samples, all the combinations of 0 and 1 in the 8 positions can provide a total of 9 different values[9]. They are also evenly spaced, highlighting 8 voltage intervals. This is visible in Fig. 4.9, as well as an example of transition. The benefits we are talking about lie on the fact that a transition is only possible between two adjacent levels, thus the voltage step is at maximum 1/8 of the FS. This is because of the shifting nature of the FIR, for which at each sampling

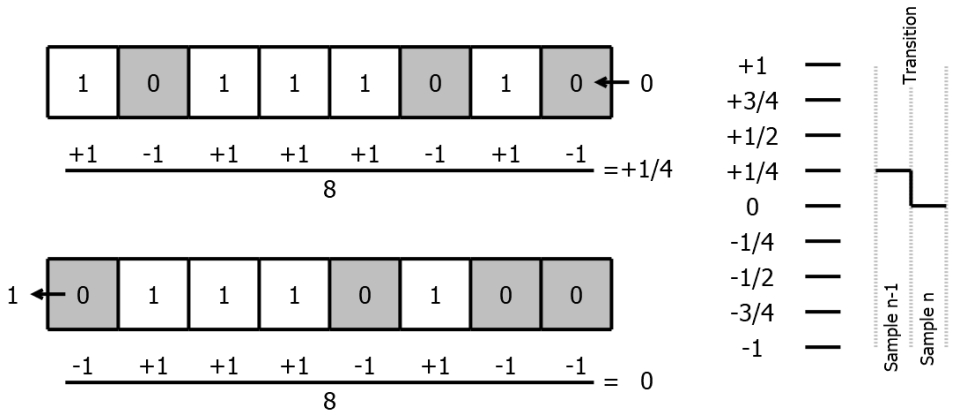

Figure 4.9: Example of 8-Taps FIR-DAC transition: since a change in the FIR is one bit worth at its maximum, the average can only change of 1/8 of the FS.

instant there are two possible scenarios:

- The subsequent sample entering the FIR is equal to the eighth sample about to exit: the average of the 8 values remains the same. The output does not change.
- The subsequent sample entering the FIR is opposite to the eighth about to exit: the average counts +1/-1 number of ones in the register with respect of the previous sample. The output changes of 1/8 of FS upwards or downwards regarding if a 0 was substituted by a 1 or vice-versa, respectively.

Since the shifting is one-in-one-out, there is no other possibility, meaning that the DAC output will never provide steps different from 1/8 of the FS. This has been seen to be efficient on reducing the impact of jitter, since the charge integrated will be lower. It has also benefits, as introduced, on the first stage amplifier. In practice, the amplifier will have

[9]From all-0 to all-1, permutations of same number of 1 and 0 in the 8 FIR places are equivalent, as they have the same sum.

to support 8 times less severe voltage step than with a simple single-bit. UGB and slew rate requirements are relaxed and power consumption can be saved in the first stage amplifier design.

A comment should be made about the others amplifiers. They receive an input by a single-bit DAC (since the FIR-DAC is only present beneath the first stage path) thus they do not have this benefits. This is sufficiently less relevant under the point of lowering power consumption, as the first stage is far more consuming than the following ones and it is therefore better to relax the former rather than the latter. A more detailed report about amplifiers power consumption will be carried out in Ch. 6.

4.7.5 Other Benefits

There are some other benefits, not power-consumption oriented, which are worth mentioning.

One of these benefits is for sure about quantizer metastability [67]: anytime the comparator cannot tell correctly whether the sample is 1 or 0 before it is locked, a 0 will be the default choice. However, it represents an error, as it is just the consequence of comparator being too slow: the input should be represented by a 1. Quantizer settling is averaged with 8 others samples and this lowers the impact of occurring of these errors. While details about this aspect have been chosen not to be reported in this work, it is true that it helps to keep the design phase simpler.

Another interesting fact is that, if the number of taps in the filter is even, the zero-voltage value (half-FS) can be represented by a state. With a power-of-two multi-bit quantizer (or an odd number of taps FIR) a constant zero value can only be represented by the mean over time of the two nearest greater and lower than zero states instead: the DAC tracks the value of 0 by transitioning between two values with average 0. This is a minor benefit because if we suppose a Sigma-Delta tracking a 0 DC signal, a dynamic behaviour on the internal states would in any case manifest (due to the very nature of a SDM). Thus in any case transitions with $\pm 1/8$ levels around 0 exist. The difference is that with an even-N taps FIR-DAC there exist a state which value is actually 0. Figure 4.10 shows the consequence of this concept graphically. As it has been just seen in Sec. 4.7.4, the output of the FIR-DAC

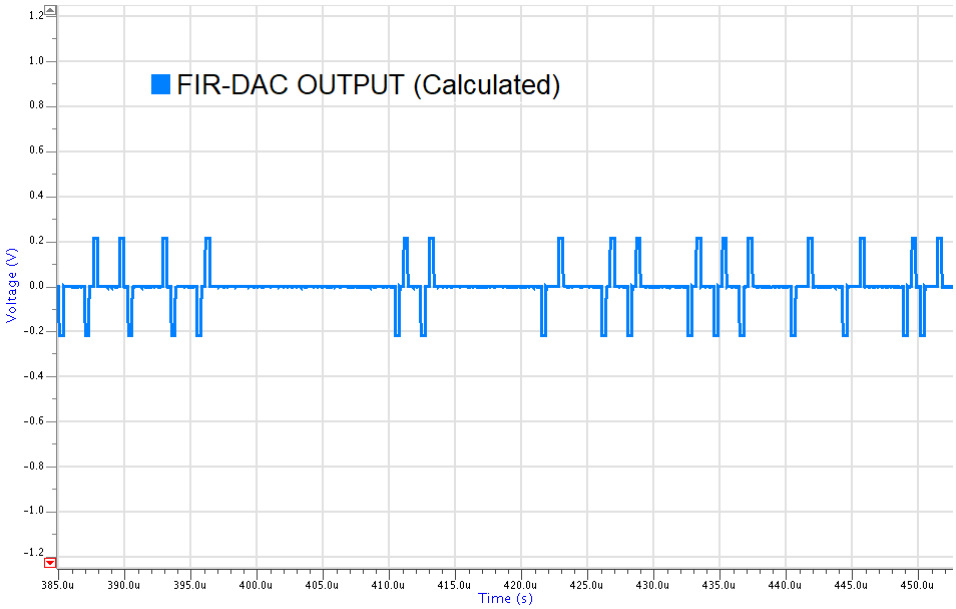

Figure 4.10: Extract of a transient simulation of CTSDM4FD8 modulator tracking a 0 DC signal. The FIR-DAC output is calculated as the average of individual DAC outputs, as there does not actually exist an output node and the average is implemented summing currents into the first integrator input node. The value of 0 appears more often than others and there are a significant amounts of samples for which no transition is experienced.

can happen not to transition and, in this context, it can tend to statistically show the 0 value.

4.7.6 Choice over Multi-bit Quantizer

An important part of this work was the attempt to use a single-bit quantizer. A multibit solution is the most appreciated in CTSDM because it has been proven to be robust against jitter and in general there is a vast documentation about how to implement a multi-bit solution. The single-bit solution has always been one of the targets as it was really appreciated in CENTO for its extreme simplicity of design and its lower power and surface budget requirements. Tab. 4.2 resumes all the benefits and downsides of both solutions.

Considering the same performance to be achieved by a modulator, it can be noticed, by focusing on all the power consuming points (marked with ⚡), that the single-bit solution is power saving. There are only two points where power cost is higher. The first is in UGB and slew rate requirements. However, the combination with a FIR-DAC with the same performance target of a multi-bit quantizer make the two solutions requirements for the first stage amplifier exactly the same. The second is SQNR recovery, which must be achieved by increasing the OSR or the Loop Filter Order. Also in this case, it will be seen when describing the power budget in Ch. 6, Tab. 6.4, that the SQNR recovery chosen for CTSDM4FD8, which consist of adding one stage in the loop filter, accounts for only 10% of the total consumption.

The final aspect that definitely puts the single bit with FIR-DAC choice at the first place for this work is the simplicity factor. There is no doubt about the lower effort necessary to design a single-bit quantizer solution over a multi-bit. Several design-friendly advantages are present: relaxed matching criteria, small and very low complexity comparator and DAC block to be designed, no DEM and no DEM algorithms [12] to be set up.

What is not there does not break.

Henry Ford

During the design phase, various issues and problems can arise and manifest in simulations. The procedure is then to find the responsible investigating the symptoms and attributing them to a specific device or to device groups which are present in the circuit. Reducing design efforts and complexity helps to keep these problems under control and avoids adding potential sources of malfunctioning and unexpected degradation.

	Multi-bit	Single-bit	FIR-DAC
	✗ Complexity of quantizer scaling exponentially with respect to number of bits	✓ Quantizer is as simple as just one comparator	
	✗ Feedback DAC is more complex consequently	✓ Feedback DAC is made of just single switches	
⚡	✓ Allows to keep lower OSR and LF order	✗ Forces higher OSR or LF Order to recover SQNR	
⚡	✗ Power efficient comparators are to be discarded in favor of accuracy	✓ The quantizer comparator may be designed to aim power efficiency	
⚡	✗ Mismatch and non-idealities heavily degrade performance, countermeasures such as DEM are mandatory	✓ Inherently linear	
⚡	✗ Last stage should have the highest swing possible to help with comparators mismatch	✓ The sign of the last stage output is the only necessary information, scaling can be chosen freely	
⚡	✓ Slew rate and UGB constraint relaxed thanks to a less important charge, given the smaller steps	✗ The full-scale step means a consistent feedback charge: a proper slew rate from amplifiers is necessary	✓ Moving average results in a lower charge transfer per transition, relaxing slew rate constraints and UGB for the first stage
	✓ High quantizer linearity (with DEM), easier to design loop filter for the modulator	✗ Loop filter needs optimisations for linearity purpose to avoid distortion	
	✓ Reduced jitter due to closer transitions	✗ Completely sensitive to jitter due to rail-to-rail transitions (it is the worst case)	✓ Averages jitter over a certain number of samples, reducing it
⚡	✗ Clock feeding several comparators	✓ Dynamic current is drawn by a single comparator	
	✓ Better modulator stability: possibility of using aggressive NTFs to keep in-band noise lower and even more relaxed constraints on OBG	✗ Maximally flat NTFs have to be smoother for stability purposes	
	✗ Delays if we use a SAR or Pipeline ADC to implement our quantizer (more severe ELD)	✓ Short delay for the quantizer comparator to make a decision (ELD-friendly)	
⚡	✗ provides a multibit word, translation circuit is necessary to eventually obtain a bitstream	✓ provides directly a bitstream, compatible with most market requests	

Table 4.2: Sum up of Multi-bit and Single-bit (+FIR-DAC) advantages and downsides.

4.8 Conclusion

Architectural choices represent an important high-level step while designing a Sigma-Delta Modulator. First, the desired performances have been identified: our main parameters are DR=100dB, quality of sound in general and lowest power and surface consumption possible, in this order. The combination of the three main high-level sizing parameters L, OSR and b, have been chosen in order to assure 100dB, with a margin of 10÷15dB in order to avoid falling below the target due to degradation encountered after implementation. Once the combinations are known, the design choice was oriented towards the least power/surface consuming. A single-bit solution was privileged, adding to the latter also the interesting feature of design simplicity. The OSR was also kept low for the same reasons, while the modulator order L was set to 4, ensuring a 100dB Dynamic Range.

The FIR-DAC countermeasure used to reduce jitter impact on our SDM has been analyzed in details, confirming the 8-taps choice found in Ch. 3.

Before moving on to transistor level design (Ch 6), there is an important point that has still not not been investigated in detail: modulator stability. As it has been highlighted during this chapter, it is the reason that drove the choices of CIFB-FF archetype and coefficient values. Since these choices represented a cost in current consumption, as seen in Sec. 4.4, a detailed motivation should be given. However, this topic presents such complexity, importance and interest, that it has been chosen to dedicate the upcoming Ch. 5 its entirety, before moving on to design the modulator at transistor level.

Chapter 5

Stabilization Method

In this chapter, an interesting feature of CTSDM4FD8 is presented. Since the quality of audio experience for the listener has always been the first in the priority list, the eventual instabilities which affect SDM with high order internal loop filters were a concern.

A high order loop filter SDM risks to becomes unstable once it is subject to some *stressful* signals. Its internal states space rapidly move towards a region of instability: this region contains all those states for which the SDM does provide corrupted data and cannot revert back to a normal operation. From this description, it is clear that instability should be absolutely avoided. To do so, stability is guaranteed through two possible and opposing methods: recovery and prevention. The definition of these two methods will be explained in detail during this chapter, as for now, it is interesting to know that there exist two categories in contrast.

The stabilization methods available at the moment of the realization of CTSDM4FD8 and which are unconditionally effective are all recovery methods. They are based on detecting the occurring of an instability and immediately engaging a recovery method, implemented with dedicated circuitry. During the time needed for this operation, the output data is in any case corrupted, generally producing abrupt sounds, like *pops* and *clicks* which are not comfortable for the listener.

An empirical stabilization method was developed for CENTO and was employed for CTSDM4FD8 as it is a very interesting feature for an audio SDM. This method is about prevention and allows, if all the conditions required are met, to obtain an intrinsically stable structure which is naturally capable of tracking a signal even right after an ill signal or disturbance ceases to be injected.

This chapter focuses on stability, which is crucial for high order SDM such as the fourth order CTSDM4FD8 designed in this work. Definition of the scenarios and what having a stability problem means will be the first aspects to be presented, followed by a collection of methods known from the state of the art. Once all the background is thus provided, the empirical stabilization method proposed, its application and the resulting intrinsic stability of CTSDM4FD8 will be presented in great detail.

Prevenire è meglio che curare. Prevention is better than cure.

Proverb (actually an international one)

5.1 Instability in Sigma-Delta Modulators

The Sigma Delta Modulator first appeared as a noise shaping solution for A-to-D conversion. It is basically a feedback structure with an integrator and a quantizer in the forward path. Simple to represent, yet peculiar in operation, it did not take long to realize that a double integration could be used instead of just a single [7] and the SNR of the system could greatly

be improved. Then, the state of the art moved towards studying the logic consequence of discovering double integration: adding even more integrators.

This practice, however, introduces instabilities in the loop filter. Instead of a single feedback 1/s path, there exist now several paths with different *speed*. The difference between the slowest 1/s and the fastest $1/s^L$ creates imbalance among internal states evolution. In particular, the last stage is very *fast* with respect to the previous ones, and the quantizer risks to enter a situation named "overload". The definition of this phenomenon is that which happens when the last stage saturates, in other words, if a sample exceeds the maximum amount of charge that can be integrated, it simply cannot be represented. The quantizer will provide the same compensation in the feedback path regardless of the severity of the saturation. This means that it is not possible to compensate the loop filter for a previous sample that saturated during a single period. Instead, eventually, several periods could be necessary to recover from saturation.

For more severe saturation, it can happen that the system is not capable to compensate soon enough before all the previous stages suffer from the same effect. The internal states become then impossible to control and the system provides corrupted data no longer corresponding to the input.

Despite these difficulties and risks, high order Sigma Delta are particularly appreciated because, as Tab. 2.1 in Ch. 2 shows, modulator order can reveal to be a very powerful parameter to improve the SNR. Furthermore, with scaling of CMOS technology, single bit quantizers are the most suitable solutions, but the worst choice for what concerns the parameter b in the SQNR (check back Eq. 2.10). It justifies the interest to recover by OSR or L. In audio application, no design is allowed to risk the occurring of a sustained SDM instability, as the output could be irremediably corrupted for the rest of its operation. All of these arguments initiated the series of works that may be found in literature trying to shed light on stabilization of high order SDM structures.

5.2 Definitions of Stability

About stability of SDM (which logic diagram reported again in Fig. 5.1), different definitions, can be found in literature. Most of the authors claim that it is the boundary coinciding with the point of Maximum Signal-to-Noise Ratio (MAX_{SNR}) while others claim that *instability* should be referred to as *saturation of limit cycle* [68] as in practical SDM, saturation level of LF stages is not high enough to get into unstable operation.

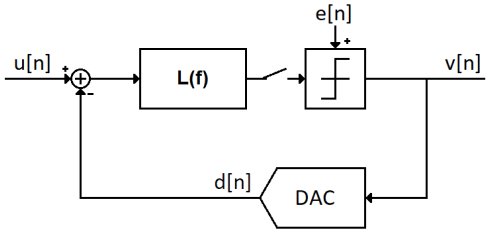

Figure 5.1: Basic Sigma-Delta block diagram.

Indeed, there exist a theoretical definition of stability for a Sigma Delta Modulator thought as a mathematical (behavioral) system, with discrete outputs (and feedback DAC values) and free internal states and it is the following [69]:

> *A Sigma-Delta Modulator is stable for a set of inputs if, given an initial state, for all inputs in the set a bounded sequence of states is generated.* (5.1)

By "free internal states" in the previous definition, it is meant to have an n-stages internal Loop Filter (LF) for which each output of the n integrators is free to assume unbounded real values. When it comes to realization, the circuit implemented in CMOS technology impose

a natural bound to any voltage variable involved: supply voltage. Having a lower and upper voltage limit means that Definition 5.1 is too general as the states will always be bounded to an interval of real states.

Though the behavioral unbounded model can be used to gain interesting information, in a practical SDM, instability is manifested as *long sequences of "ones" followed by long sequences of "zeroes"*.

5.3 Important Remarks

There are some important remarks regarding stability and definitions that should be discussed before moving on.

5.3.1 Single-bit and Multi-bit Categories

There are two cases for which stability should be studied separately: modulators with single-bit and multi-bit quantizer. Behaviour, criteria and results are not the same if one or the other case is investigated. The methods used to stabilize the two are also different. Since this work is about stabilizing a single-bit fourth order SDM, any argument about stability is to be referred and to be thought applicable to the single-bit category only.

5.3.2 Instability and System Saturation

There are two definitions in particular that may be found in literature which can result unclear: Maximum Stable Amplitude (MSA) and the Point of Maximum SNR (already seen to be denoted $\mathrm{SNR_{MAX}}$)

- The MSA is defined as the highest input power[1] the SDM can withstand before entering an instability condition.
- The $\mathrm{SNR_{MAX}}$ point is defined as the point in the DR where the maximum SNR is reached, before dropping due to saturation of the system. Of course, it is also associated to an input power after which, for higher amplitudes, the said saturation occurs. The situation is clear from Fig. 5.2.

Sometimes in literature the point of $\mathrm{SNR_{MAX}}$ is considered to be the MSA, as the SNR drop is considered an instability of the system.

The arguments and methods presented in this chapter refer to instability as an oscillatory condition from which the SDM may never recover. Though saturation of the system may be the starting point for an instability to occur, it is not true that a SDM which operates with an input level superior to $\mathrm{SNR_{MAX}}$ is unstable. It can definitely happen for a SDM to operate past the $\mathrm{SNR_{MAX}}$ input level and still provide a (saturated) meaningful output. Subsequently (at a later time), it can happen as well for the input power level to fall again below the $\mathrm{SNR_{MAX}}$ point, showing the expected SNR on the output from the one extrapolated in the DR plot. This situation happens when the value of MSA is higher than $\mathrm{SNR_{MAX}}$. There are of course cases where the two coincide, but the difference in definition still applies.

5.3.3 Recovery as a Central Point

Another important note that should result clear from the presentation of this method, is that the objective is to obtain a modulator ble to represent the input signal correctly within a very short delay[2] from the moment when an *ill* kind of signal that was injected ceases

[1] Like it can be often found for input signal power in general, also in the case of the MSA this level is usually expressed in dBFS.

[2] In audio application, for example, this tolerated delay should be thought as the shortest period audible, that is, a 20kHz disturb or a disturb that lasts 50μs. For a SDM clocked at 3.072MHz, this means that the disturb should cease before 76.8 (=OSR) samples.

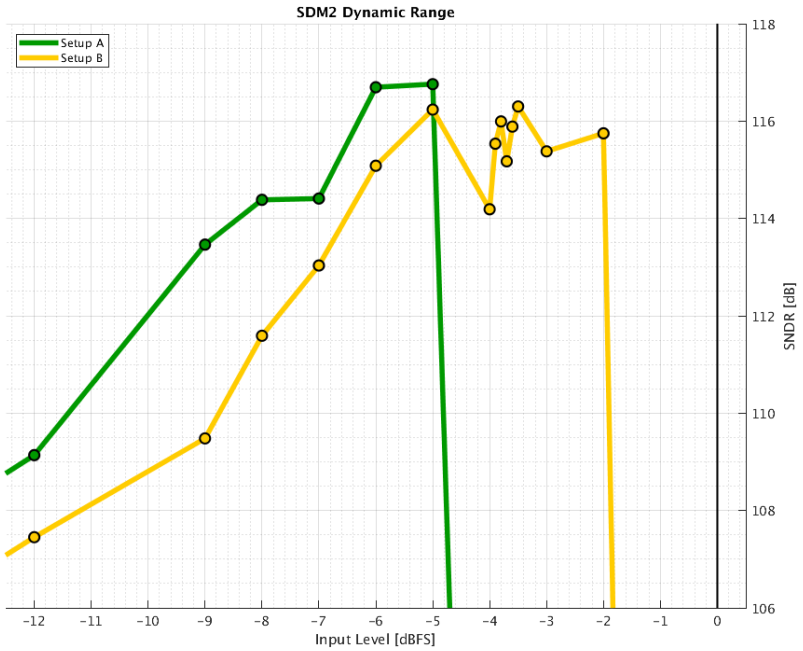

Figure 5.2: Two examples of SNR_{MAX} from two different arbitrary modulators. The points of SNR_{MAX} found in this representation are -5dBFS for Setup A (Green) and -2dBFS for Setup B (Yellow).

to exist. In other words, what is important is that when a normal signal is again provided after one that was not intended to be handled from the modulator, this modulator will get back to proper operation. Therefore, the central concept of this method is that stability is a synonym of a recovery capability and that its time is extremely short (in the order of a few samples).

Another comment is: in this chapter and inline with the novel stability method that will be proposed, this work absolutely avoids the philosophy of building an environment around an SDM such as no signals it could not handle are possible to be injected. In other words, the blocks surroundings the SDM are not designed in order to keep it safe from abrupt signals and disturb. For example, a common practice is to calculate an MSA in order to find which signals have too much power to be handled and, subsequently, the design and specifications are organised in order to avoid feeding the modulator with such signals. In this work, this path is discarded because any unpredicted and then unhandled disturb can put the SDM in jeopardy. The objective of this method is to guarantee stability under extreme stress, as this means that no other prevention nor recovery methods are to be implemented and the modulator should remain a simpler circuit. This argument is of extreme importance since it should be remembered that some kind of disturbance[3] may occur and if it is not handled, there is no way the SDM can recover from an instability.

5.4 State of the Art

Since the introduction of Sigma-Delta Modulators, some works about stability of these *peculiar* systems have been presented, with the attempt to characterize this behaviour and give stability criteria.

[3]That can be an unfortunate pattern of noise or an electromagnetic wave perturbing the circuit for example.

There are two remarkable results for low order modulators, which is a fundamental part of general knowledge about SDM:

- A first order modulator is always stable
- A second order modulator is conditionally stable

These two statements are intended with respect to input signal power and are found in textbook from literature [6] [8] accompanied by mathematical arguments.

Then, since the first appearance of Sigma-Delta Modulators with multiple integrations, not a single work could provide an absolutely complete mathematical evidence about stability of modulators of order three or higher. In literature, these kind of SDM, with an internal loop filter of order three or higher, are generally addressed as *higher order* or *high order* SDM. Their stability is today still an open discussion. The main reason is that sigma-delta modulators are *chaotic*[4] and non-linear systems. They are really complicated to represent, as there do not exist mathematical models capable of describing this peculiar systems.

Many attempts have been made to explore stability topic, most of them are based upon dividing the state space into subsets and studying trajectories within the said spaces separately from transitions between them [70] [71]. Others reorganise the topology of an Order L modulator into an equivalent structure made of L Order 1 "sub-modulators" [72], which is easier to describe for this purpose.

A fixed point in literature is the study from Schreier [73] who proposed an empirical analysis and commented about the state of the art at that time. This paper basically proves showing specific examples (mostly counter-examples) that any claim of mathematically proof of stability criterion was wrong or too/not enough restrictive.

The next Sections are showing the most known considerations and solution about stability. They are either prevention or recovery methods. Comments about these two categories will be proposed at the end of the presentation of all their representative, in Sec. 5.5. As a first step, let us define them. Prevention methods are based on criteria that allow to design a modulator in such a way that no instability would occur, ever, if all criterion are met. Recovery methods expect the eventuality for the modulator to enter a state of instability: their purpose is to firstly detect then correct this situation, returning to a proper operation.

5.4.1 Lee's Rule

Prevention method. This is a rule which first appeared in master thesis from Lee [74] and which offered a criteria on the NTF in order to assure stability of a high order SDM.

First, the infinity-norm of a transfer function H(ω) is defined.

$$||\cdot||_\infty = \max_\omega(H(\omega))) \tag{5.2}$$

Then, the "Lee's Rule" states that the following condition

$$||NTF(\omega)||_\infty < 2 \tag{5.3}$$

has to be respected in order to guarantee the stability for the modulator NTF.

The aforementioned work from Schreier [73] proved that this rule was inexact and not general. Some modulators could be found to be unstable while the condition was met and, vice versa, some others could be found to be stable while the condition was not met. So, there exist clear counter-examples which question this rule. This result can be used as a rule-of-thumb and it is actually very appreciated among designers to have a first hint on how to choose the NTF but, in any case, it cannot be used as a prevention method for a modulator to avoid stability.

Finding a condition just calculating a norm on the NTF was something designer found very interesting, so much so that other attempts have been made with other norms, for example with the euclidean $||NTF(\omega)||_2^2 < 3$ [75], but the results were analogous.

[4] They are actually, under the point of view of quantization noise, completely determined, but the complexity of studying such systems without approximations is, again, impossible with the mathematical instruments available. When approximating and using models, the system becomes chaotic.

5.4.2 Variable Gain Analysis

Prevention Method. A very interesting analysis on stability of SDM in general is to linearize the system and to study the position of poles with respect of the unit circle in a pole-zero plot. The only non-linear element in a SDM is the quantizer: it is substituted by a simple gain, followed by the addition of quantization noise. If the quantizer is multi-bit, it is simple to identify the gain of the mathematical function associated with it, but what happens in the case of a single bit? Since the mathematical function describing this element reduces to v = sign[y], the gain is undefined.

The analysis for the single bit case remain the same in its principle: the quantizer element is substituted by a gain, but in this case, several calculations on the system are performed varying the value of the said gain. This procedure is appropriate under a physical point of view because it is true that the quantizer can translate any continuous value at its input into +1/-1 at the output. Thus it is also true that the gain actually changes and depends on each sample.

Mapping poles and zeroes for a linearized structure varying the value of the gain which substitute the quantizer is called Variable Gain Analysis and it claims that a modulator is stable if all the poles of the system falls inside the unit circle.

Though this might be convincing and happens to be true for a very wide range of examples of high order modulators, unfortunately it reveals not to be true for every modulator. In the same spirit as in [73], there are counter-example which can be found. This statement is also made, for example, in a very interesting work from Hein and Zakor [76] where there is a comment about a modulator not having every pole inside the unit circle that is anyway found to be stable.

The same happens in CTSDM4FD8, whose Pole-Zero Map is shown in Fig. 5.3. If

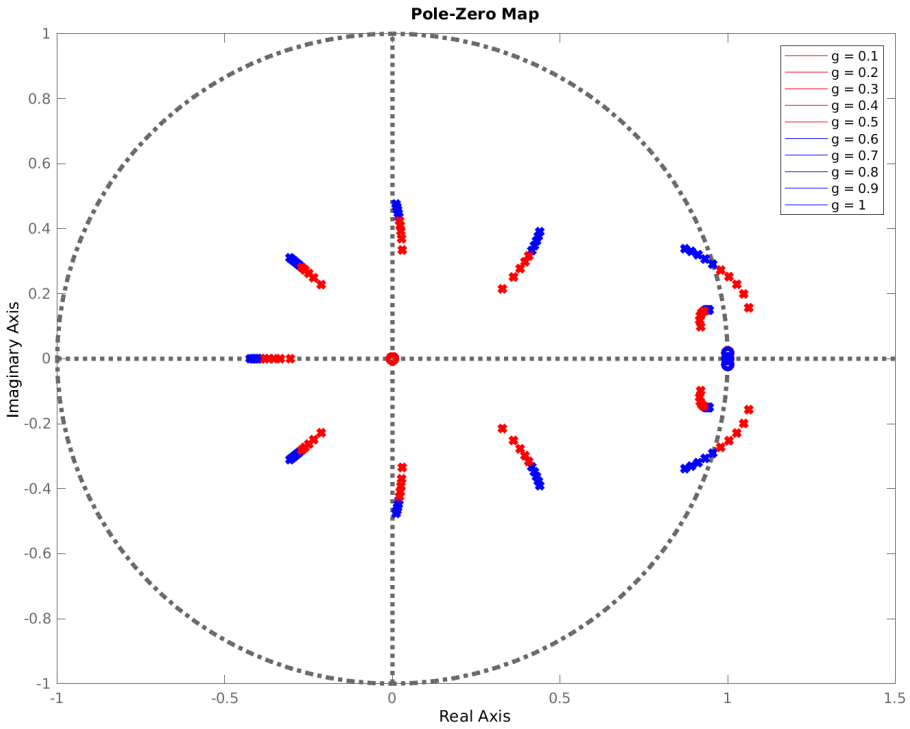

Figure 5.3: Pole-zero plot of CTSDM4FD8 with the variable gain method, according to which, every gain for which the poles are inside the unit circle (blue) are stable, while for those falling outside it (red) is not.

this method was true, the modulator would be unstable whenever the fourth-stage output (quantizer input) exceeded FS/2 in magnitude (that is, g=0.5). Of course it is not the case. There are many moments at which the output of the fourth integrator largely exceeds this

value, even reaching up to FS itself in certain simulations. However, the system remains stable and normal operation is guaranteed. An example of this situation is shown in Fig. 5.4, where one of the two outputs of the fourth integrator differential structure (see Ch. 6) can be noticed to go often past FS/2 (6.125V Single-Ended).

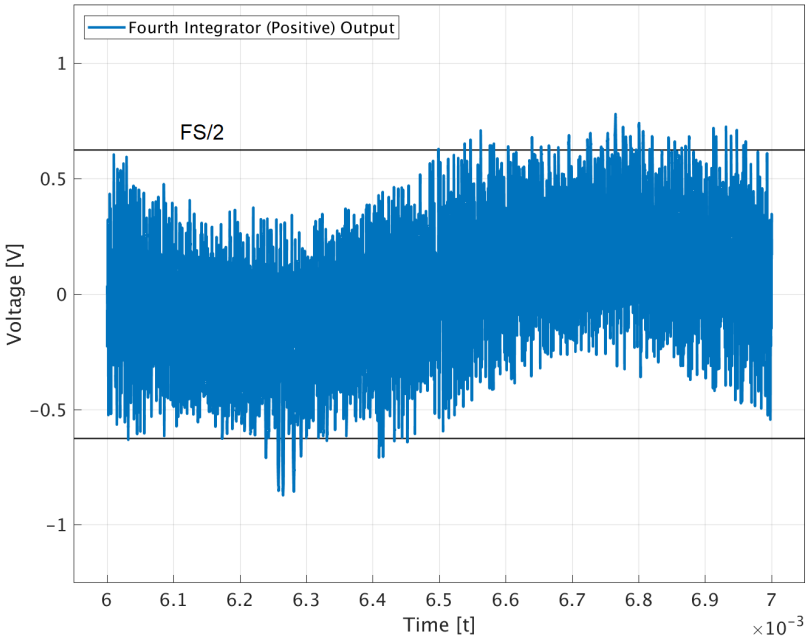

Figure 5.4: Part of a transient for one of the outputs of the differential fourth integrator of CTSDM4FD8 modulator. Though the Pole-Zero Map in Fig. 5.3 foresees instabilities for output magnitudes over FS/2, in the situation in this figure this value is exceeded several times and the operation is normal.

With these arguments, this method cannot be used as a prevention for stability with an unquestionable level of confidence as the condition has been proven by counter-examples and experience not to be necessary.

5.4.3 Hard Reset

Recovery method. Once an instability occurs and is detected, the concept of a hard reset is to simply immediately bypass normal modulator operation and force each internal state to a fixed value (generally, half FS). This method is very easy to implement as shown in Fig. 5.5, according to a patent from Wang [77]. In this integrator closeup, it is shown how every stage input and output are shorted to half supply voltage, to be released afterwards.

The concept lying behind this intervention is that the internal states are reset to a set of values which constitute a safe starting state in general. Once the signal becomes again such as it can be handled by the modulator, the reset is released and the system will find itself again in a normal state of operation.

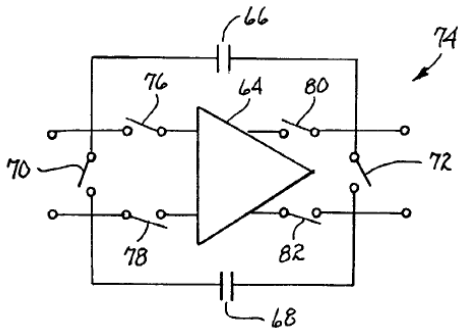

Figure 5.5: Integrator closeup for the hard reset method.

5.4.4 Local Loop Controlled Instability

Recovery method. This solution, whose architecture is depicted in Fig. 5.6, detects overloads and intervenes in each stage independently [78]. The intervention consist in a compensation of the currently defective stage, while a digital correction of data, basing on this same stage actual information, is as well performed *a posteriori*. The compensation consists in adding a current opposed to the one responsible of the overload of the stage. The digital correction is a manipulation performed on registered samples, based on how the detection was triggered by internal states evolution.

Notice that corrections are made on the output data. In the loop filter it does exist a compensation, but not a correction. The two are different because the compensation is just a countermeasure aimed to avoid overload of a given stage. This means that the state will not evolve as it naturally should and error will be produced. Such error is free to circulate in the loop filter, inevitably corrupting the evolution of the states. Any loop filter effect due to corrupted data that is not handled by digital compensation, will therefore appear in the output spectrum. This concept is explained with more details in Appendix A.

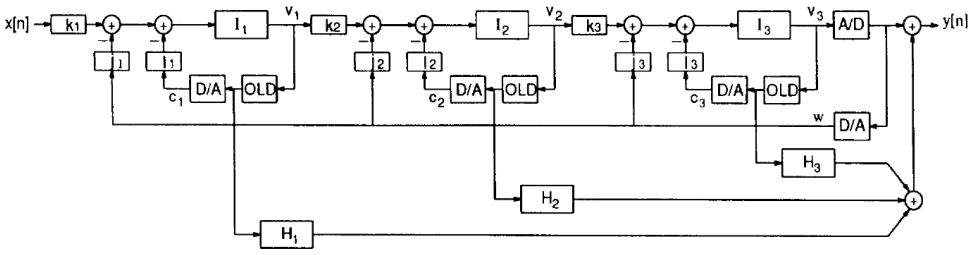

Figure 5.6: The high order single-stage single-bit oversampling ADC stabilized with local feedback loops.

5.4.5 Internal Linear Feedback

Recovery method. This patent [79] proposes to activate additional paths in the loop filter once an instability occurs. In the structure presented in the patent and reported in Fig. 5.7, a structure with just a single feedback path on the first stage is assisted by activating some additional feedback paths on following stages. It effectively change the topology of the loop filter: adding faster paths help to correct the ill behaviour of the modulator, with the attempt of preserving linearity as much as possible during the process.

Once the detector verify that the situation has returned to normal operation, the auxiliary paths are switched back out and the *standard* NTF is restored.

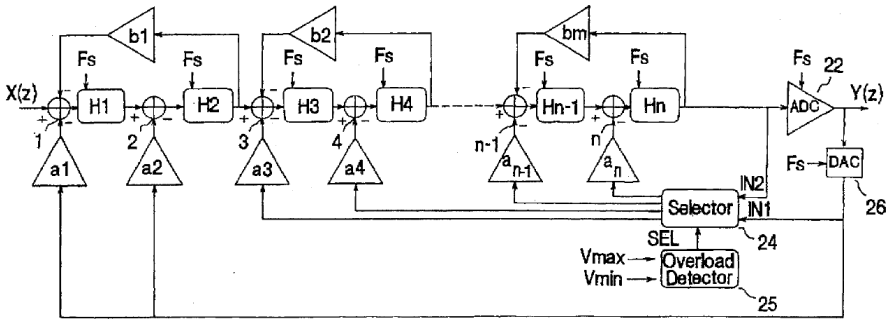

Figure 5.7: A structure activating additional feedback paths on detection of instability.

5.4.6 Order Reduction

Recovery method. A very interesting concept from a work from Pneumatikakis [60] consist in reducing the structure to a second order, switching out each stage (Fig. 5.8) following the second. The principle is that a second order is conditionally stable and the condition is simply for the input to have a magnitude lower than FS. Once the higher order stages are excluded from the circuit and the latter stability condition met for the remaining second order structure, the SDM recovers naturally and immediately. The higher order is then restored.

This method has a great advantage with respect to other recovery methods for what concerns the amount of time to recover: it does only depend on the detection. Then the recover is almost instantaneous, a matter of few samples.

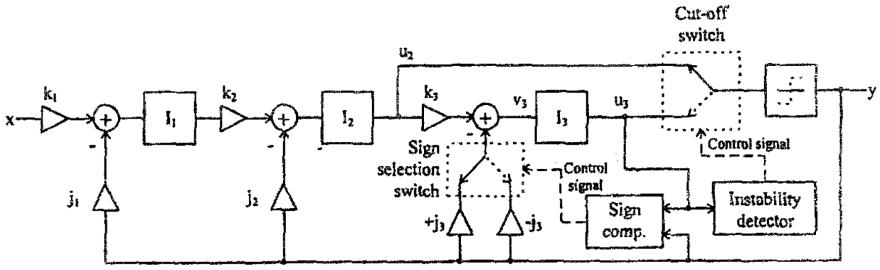

Figure 5.8: Third order Sigma-Delta Modulator stabilized by reducing the order of the loop filter.

5.4.7 Clipping

Prevention method. A very interesting study which, as it will be explained further, is based on a very similar principle to the stabilization method proposed in this thesis. The idea is to analyze the behavior of the internal states of a modulator focusing on the fact that they can just take a finite range of values [80] as in the model in Fig. 5.9, where each integrator output (internal state) is bounded by a clipper block.

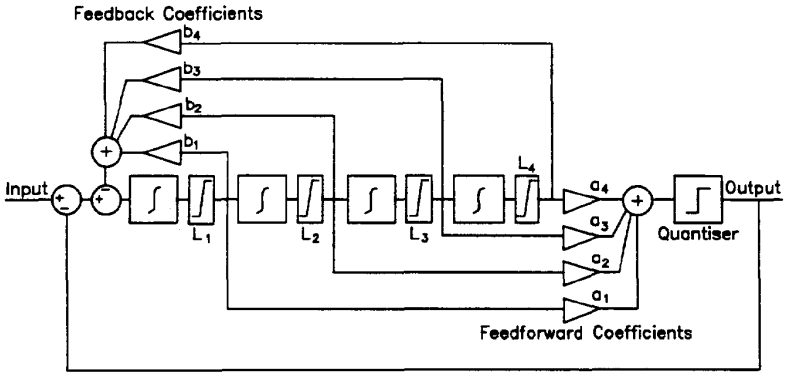

Figure 5.9: SDM Structure with saturating clippers (L_i) at each integrator output.

The analysis is about the L_i values of these clippers, which determine the values $\pm L_i$ at which each integrator output is bounded: in the paper, system stability is analysed in function of combinations of L_i, which may vary independently. The result is that these values, which of course represent voltages in the electrical implementation, could range from orders of magnitude of $1 \div 10$, in a model where 1 is the FS, or, the output of the quantizer is ± 1. These values are incompatible with a practical implementation.

It is nonetheless a very interesting work since correctly bounding SDM internal states is the path for stability, even if in this work the implementation is not feasible in an electronic sense, this opened to a lot more analysis.

At the time [80] was published, there existed also a previous contribution to this method from Adams, who made a very interesting remark [81]. He sees clipping the states as limiting the degrees of freedom of this chaotic system. By imposing boundaries, it happen to forbid certain sets of states which bring to instability regions.

Another interesting prior contribution [10] states that the stability of a modulator is determined by the combination of clipping and coefficient choice (and scaling) in general. This is the most similar concept found in literature to the one which is proposed in this thesis. As it will be commented again further, the structure proposed in [10] has been replicated and put under test, with the purpose of verifying its limits face to the method we propose. However, the structure actually pass the stability check of the benchmark we set up, that is, it respects by default the stability criteria needed by our method.

5.5 Comments and new Objectives

As it has been highlighted in Ch. 1 in audio applications, quality of sound is of primary importance, in order to guarantee a good sound experience to the listener. Sustained instability during time is of course not an option, so it must be either prevented or rapidly recovered. Recovery techniques are the most used: all the prevention techniques presented in the previous Sections could be found to be inaccurate or impossible to implement, so even if they can be used to set up a robust system, the eventuality of instability is still there and a recovery method shall be implemented as well, to assure no instability would never establish. In the case a SDM enters in a state of instability and then recovers, however, there is a time period during which data is corrupted. This, depending on the duration, severity and type of digital compensation behind it, can happen to produce pops and clicks, which are abrupt sounds and represent indeed a bad experience for the listener, especially those with the sharpest ears.

The best solution of course would then be a prevention method, which in principle avoids instability even if the modulator is put under stress by the most aggressive inputs. Once this stress is over, a normal operation is restored in very few samples (in the order of unity) and it does not even represent an instability since the SDM is tracking the input as it is[5]. Speaking

[5]It is rather the input that is maybe not what expected in this case.

about typical audio oversampling frequencies (Ch. 2, Sec. 2.5.2), the quantity *few samples* is far above the audio band, thus any abrupt sound is not audible by even the most sensible ear.

Such a method has been several time object of mathematical study, but non-linearity introduced by the quantizer, especially in the single-bit case, cause mathematical models to be defective and achieve just insights and partial results. Even if such works are of extreme importance, designers are forced to walk the path of empirical analysis.

To resume, our target, desired for audio application, is to have a method which allows the fourth order SDM to remain stable under the influence of the most stressful input signals: after the latter signal ceases and a normal one is again supplied, the system under consideration has to be capable to track the *healthy* signal in a time as short as few samples. This allows the abrupt sound produced in case of an ill signal to be *short* enough not to be heard from human ear.

5.6 Natural Saturation Stabilization Method

Due to the mechanism it is based on, the empirical stability method we propose has been decided to be named Natural Saturation Stabilization Method. It is basically about controlling three parameters and a quantity marked by a relation between them: supply voltage, reference voltage and feedback paths coefficients. The mechanism which keeps the system stable is directly related to amplifiers saturating, thus limiting the SDM internal states. The three parameters just named to be the ones to keep under control are actually those determining the gravity of the saturation event. In fact, it has been already seen during this chapter that whenever an internal state saturates, a loss of data occurs and an *inappropriate* feedback response is produced. This method has been investigated because we are convinced, that the tuning of the aforementioned three parameters allows the modulator reaction to sufficiently oppose to this saturation state.

The method has been originally investigated by Christian Fraisse, who was part of the ST Design Team during half of this thesis period and who is now in retirement, in the context of stabilizing CENTO. His work includes mainly the following two aspects: first, to discover that the specific relation between quantities in Sec. 5.7, Step 2, is a key value to take under control and second, the setting up of a simulation (Sec. 5.8.1) necessary for the application of the method. In this thesis, his work has been analysed, then formalized and integrated with new material and simulations obtained during the time dedicated to this research.

This procedure, as it is presented, may be thought as basically relying on integrator clipping and coefficient tuning, so that, by consequence, the method proposed can be thought to be the same as in the cited works about these two techniques, respectively [80] and [10]. These are very interesting and have some common principles with our method, but none of the two controls the physical quantity proposed further (Sec. 5.7, Step 2), a relation between the three parameters presented in this section and core of the method. Furthermore, while comparing our method to the two cited, the first is not possible to implement electrically in a circuit as it is presented and the second actually happens to meet criteria the method requires, as as it has been tested along CTSDM4FD8 for comparison. This fact means that its stability is justified from our point of view and that their modulator cannot ever be put in an unstable condition.

5.6.1 Method Flow

The Natural Saturation Stabilization Method is an empirical method and several checks and simulations are necessary for it to validate a structure. It is made of two aspects: Creating a Stable Modulator (Sec. 5.7) and Stability Benchmark (Sec. 5.8). The first aspect gives a step-by-step list of operations that should help the designer to properly choose the parameters V_S, V_R and a_i, while the second provides a set of two different simulations for support and verification while progressing throughout the first. This means, that there does not exist an order, but the two are tied one to the other and the process is about fixing

the structure one simulation at a time. The flow of actions and verification to follow is represented by the chart in Fig. 5.10.

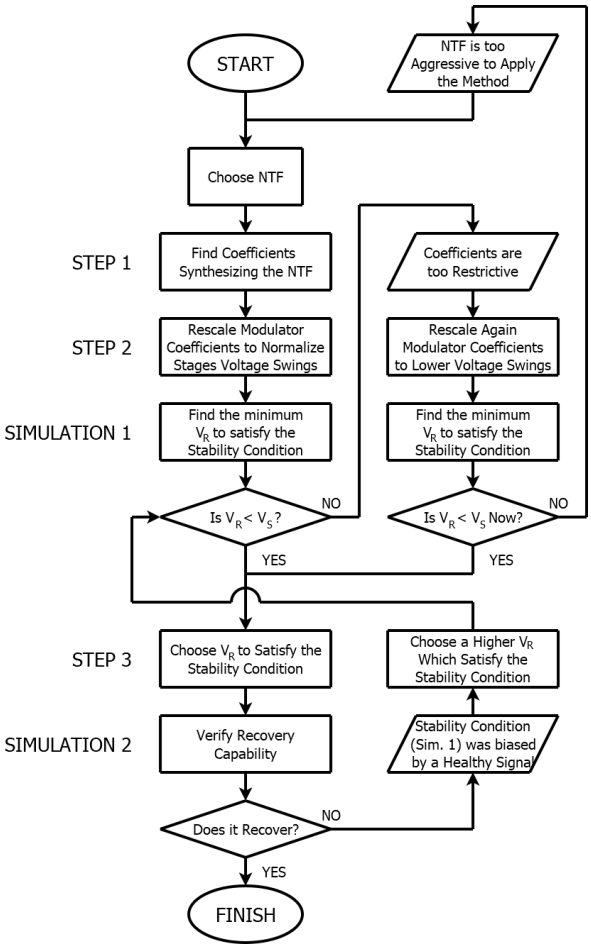

Figure 5.10: The flowchart illustrating the application of our proposed Natural Saturation Stabilization Method.

The amount of attempts the designer has to make within the flow depends on the NTF desired and the modulator topology chosen to implement it. Some NTF, especially those which are more *aggressive* tend to be difficult to stabilize and, contextualized within this method, maybe impossible, unfeasible or inconvenient.

The remaining sections of this chapter describe in detail all the steps just presented, with comments, insights and examples applied to CTSDM4FD8.

5.6.2 System Description

Before going further, a word about the model used to represents SDM under analysis should be spoken. Since stability of a modulator is all about the evolution of internal states, it can be studied on a really simple behavioral model. The advantage is undeniable: simulations are very fast and there is no drawback on accuracy. CTSDM4FD8 modulator in its most simple representation is reported in Fig. 5.11 and this is the structure that is analysed in this chapter. The parameters which appear in this diagram are all the same as in Tab. 4.1 in Ch. 4, unless otherwise stated or varying due to analysis.

For consistency it has been decided to show results of the modulator not normalising the frequency at 1Hz, but clocking at $f_s = 3.072$MHz. The same applies to transient simulations, reported in seconds.

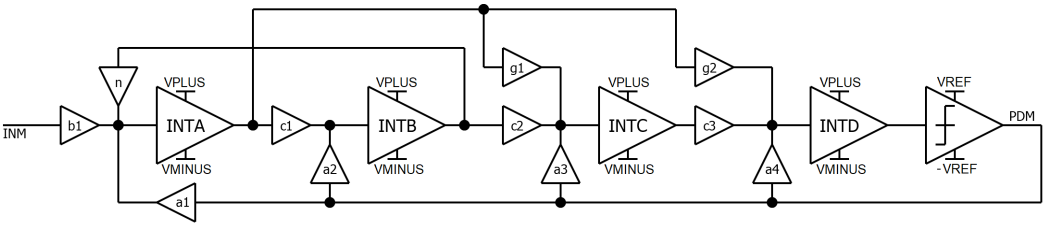

Figure 5.11: The Fourth-Order Single-Bit CTSDM behavioral model used in for stability analysis.

Just a few more words about the behavioral model of amplifiers. They are simple delay blocks (z^{-1}) with a clipped output. The clipping function is as simple as the following definition

$$V_o(V_i) = \begin{cases} V_S & if \quad V_i > V_S \\ V_i & if \quad V_i \in [-V_S, +V_S] \\ -V_S & if \quad V_i < V_S \end{cases}$$

implementing therefore a region of linearity restricted to the the voltage value range $[-V_S, +V_S]$ and saturating with an order 0 continuity (derivative is not continuous).

5.6.3 Simplified Notation

For a matter of simplicity, all non-transistor-level analysis have been set up as to preserve a symmetry centered in V=0. Supply voltages VPLUS/MINUS, reference voltage VREFP/M (referring to upcoming system description in Fig. 5.11) are therefore both with the same magnitude but with opposite sign. For now on but limiting to this chapter, let us therefore refer to VPLUS/MINUS and VREFP/M only as V_S (for "Supply") and V_R (for "Reference"), assuming that they have a corresponding opposite value and both are centered in 0. This is resumed in Tab. 5.1.

Notation	Simplified Notation Used	Design Value [V]	Description
VPLUS	V_S	$+1.25$	Supply Voltage (High)
VREFP	V_R	$+1$	Higher Reference Voltage
VCM	"0"	0	Common Mode Voltage
VREFM	$-V_R$	-1	Lower Reference Voltage
VMINUS	$-V_S$	-1.25	Supply Voltage (Low)

Table 5.1: Simplified notation for some of the modulator parameters, valid for this chapter.

5.7 Creating a Stable Modulator

In this section, the part of the method which addresses modulator sizing is described. All the actual parameters filling up the practical examples, visible in Fig. 5.11, are set, as it has already been commented, as in Tab. 4.1 of Ch. 4: the step-by-step procedure is in fact applied to CTSDM4FD8 modulator.

Step 1

The first step of this procedure is exactly the same as for any modulator: once the NTF desired is chosen, it consists in setting up the structure and coefficients to implement it. This is achieved with classical calculations or tools, like "Delta-Sigma Toolbox" from Schreier [6].

At this step the sigma delta cannot probably be simulated successfully yet, since the furthermost stages tend to have coefficients of orders of magnitude higher than first stages, but the system is already bounded[6] at a finite V_S.

Step 2

This step is also common to any SDM design and it consists in rescaling the (voltage) values covered by each integrator output. To obtain such renormalization, it is necessary to multiply each coefficient referring to the same integrator by the same gain (in the frame of CTSDM4FD8 specific design, this is shown in Ch. 4, Sec. 4.5).

Normally, this normalization allows, for a given input signal power, to have the same voltage swing on all internal nodes. The designer finds the values also in function of the maximum input signal power that prevents the swing to be greater than V_S, that is, during Step 2, the value of SNR_{MAX} is determined. In our case, the -3dBFS level is chosen: transient simulations confirm that no internal node ever reach $\pm V_S$, therefore, there is never a non-linearity contribution due to amplifiers model.

All of the latter, while integrated with our method, is done taking into account two facts. The first is that the rescaling process lines up with the voltage V_S, which is common for all the integrators. Notice that the analysis can be done with different V_S for a more general (mathematical) point of view, but this method is about actual design. The second is that following this method, the designer is aware that this operation can be performed taking into account the concept explained further in Step 3. This is important because at Step 2 we basically fix the coefficients a_i, which can be tuned/renormalized according to the specific controlling parameter defined in Step 3.

Step 3

In this last step, when V_S has been fixed by design specification (supply, battery...) and coefficients a_i have been set in Step 2, the designer should finally choose V_R satisfying the stability condition

$$1 < \frac{V_S}{V_R \cdot a_i} < M \qquad \text{for } i = 1, ..., L \tag{5.4}$$

Where M is a dimensionless quantity to be found via simulation (see further in Sec. 5.8.1) and is specific about the system itself. At this point, it is useful to define the quantity

$$Q_i := \frac{V_S}{V_R \cdot a_i} \tag{5.5}$$

so that Eq. 5.4 can be written as $1 < Q_i < M$ in short, valid for all i up to L, furthermore, the same equation will be eventually addressed as "the stability condition". The kind of simulation proposed to realise this step is the first one of the benchmark that will be described in Sec. 5.8.1.

It can be argued that, just under a mathematical analysis and point of view, with combinations where V_R is greater than V_S, Q_i becomes less than 1. In fact, Eq. 5.4, can be generalized to the more general Eq. 5.6

$$m < \frac{V_S}{V_R \cdot a_i} < M \qquad \text{for } i = 1, ..., L \tag{5.6}$$

With a new dimensionless parameter m appearing and having the same nature of M, just representing a lower bound instead. It is much more interesting to find M than m and the reason is simple: m generally happens to satisfy m<1, but a_i is never assigned values higher than 1 after rescaling of Step 2. In this condition, since V_S is the supply voltage of the circuit, there is no way that Q_i in expression Eq. 5.4. could be lower than 1 by any mean

[6] The only way for the system to be simulated succesfully and be stable, is to bound each stage to a different V_S as in [80].

due to V_R. Finding the values of m may only provide mathematical insights, but, again, this is not the objective of this chapter.

5.8 Stability Benchmark

Stability for the modulator is proven by subjecting it to a series of extensive simulations. The environment chosen is MATLAB/Simulink due to intuitive and control-oriented environment and advantageously short simulation time. MATLAB only simulations can be performed as well.

Notice that since these are behavioural simulations, the principle of equivalence between continuous and discrete time can be used and the solver can be set to be fixed-step, as it is customary when simulating discrete time modulators: at this stage, there are no continuous time related effects that matter. Therefore, there is no need to add this complexity and the analysis can be carried out on the discrete time equivalent.

The combination of the two different simulations proposed in the next two Sections is likely to be used extensively: since this is an empirical method, results are based on experience and speculation, on trial and error, on continuously taking steps back and modify parameters to find a stable setting.

After the explanation in the following Sec. 5.8.1 and Sec. 5.8.2, more details about the application of the method and important aspects to care about are illustrated in Sec. 5.8.3 and Sec. 5.8.4.

5.8.1 Simulation 1: Stability Condition Meeting Research

The first kind of simulation is about finding M and verifying that quantities Q_i respect the stability condition.

The basic concept is to start a simulation in a condition where Q_i does not respect the stability condition and then vary V_R until the condition is met. Meeting of the condition is something which has to be found graphically. In Fig. 5.12 an example where V_R starts from a value of 0.5V is shown. Notice that since M is not known a priori, V_R should be chosen to be *very low* in general, as it will be seen further in this formalization, in this example the value is sufficient not to meet the stability condition. In the first part of the simulation it can be noticed that the modulator is unstable and typical oscillations can be experienced. Then, the value of V_R is programmed to raise over time. There exist an instant t_s when the modulator starts to recover from instability. The corresponding value of V_R and consequently Q_i assume in that instant can be defined as $V_{R_{STAB}}$ and $Q_{i_{STAB}}$; then, the following is true

$$M = \max_i(Q_{i_{STAB}}) \tag{5.7}$$

It is possible that M is not found, as it can happen that V_R raised up to V_S and the instability is still there. In this case, the designer shall investigate and reorganise a_i in Step 2. If this does not come to a solution, probably the NTF chosen is too aggressive and a further step backward to Step 1 shall be done, releasing constraint on the NTF to realize.

On the contrary, it is very important to respect the basic concept and begin the simulation in a condition known to cause instability (which must be eventually forced). This is because it can happen that no oscillations are experienced even if the criterion is not met. The reason for this, is that the system did not happen to be stimulated in the *correct way*; this concept will be clearer in Sec. 5.8.5, where it will be highlighted that, while the stability condition is not met, a modulator starting its operation in some convenient conditions, can be brought out of control by an unfortunate stimulation and never come back to a correct operation again.

To sum up: there exist a control quantity $Q_i(V_R)$ that must be verified to be lower than a constant not known a priori, which has to be found using the variation of V_R itself.

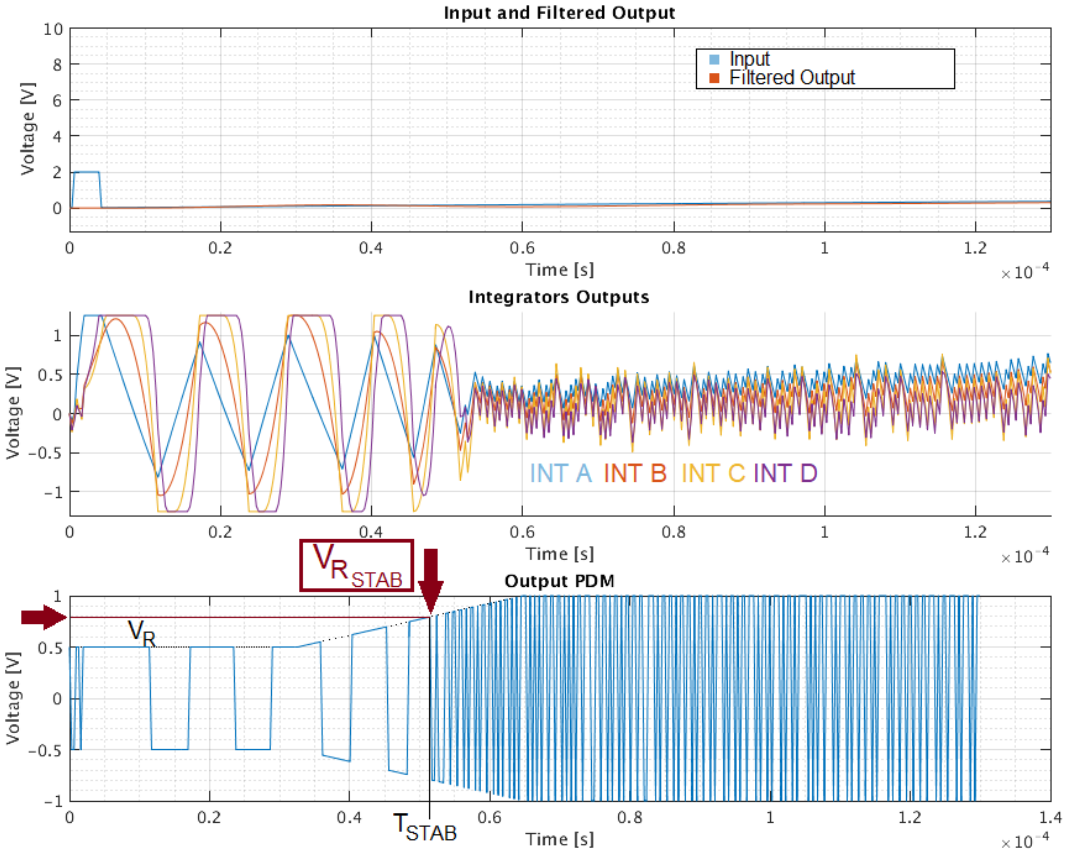

Figure 5.12: Stability Condition Meeting Research simulation. A value for V_R is deliberately chosen not to be meeting the stability condition. Then this value increases in time and once the condition is met, the designer can extrapolate data graphically. In this transient, $V_{R_{STAB}}$ can be found to be 0.69V.

5.8.2 Simulation 2: Recovery Capability Test

The second simulation verifies the recovery capability of the modulator and it is designed to severely put it under stress from a certain instant while operating in normal conditions.

In order to do so, the principle of action on the modulator is presented in Fig. 5.13. A stimulation meant to put the modulator into an instability condition is placed during a period (I) in the middle of the simulation: a period before (B) and after (A) are of the same length and start at the same input signal phase in order to perform two FFT which are coherent one with the other. This setup allows to compare the "before" and "after" ill

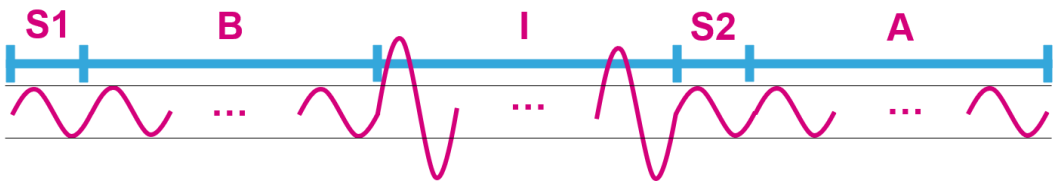

Figure 5.13: Recovery Test simulation. An ill input signal is injected in the modulator all along a period (I) in the middle of the simulation, while a period before (B) and after (A) are made identical to calculate two comparable FFT. Periods S1 and S2 are put before B and A in order to prevent settling unwanted information to be subject to FFT calculations.

input signal situations, with the possibility to eventually superimposing the spectra. Two single stabilization periods (S1) and (S2) are put just before B and A periods: this is more

than enough to allow the modulator to settle and the filters to react. It is necessary at the beginning of the simulation and after exiting instability, in order not to let transients affect the calculations of the two FFT.

5.8.3 Application of the method

In this section, the application of our method to prove CTSDM4FD8 stability under stressful signals is reported. The importance of applying both kind of simulations proposed in Sec. 5.8.1 and Sec. 5.8.2 will be clearer, as introduced earlier, in Sec. 5.8.5.

The first simulation, to search *when* (or whether) stability condition is met, has its results shown in Fig. 5.14: the modulator is unstable until $V_R = V_{R_{STAB}} = 0.67V$. Once this value is reached, a normal operation is established.

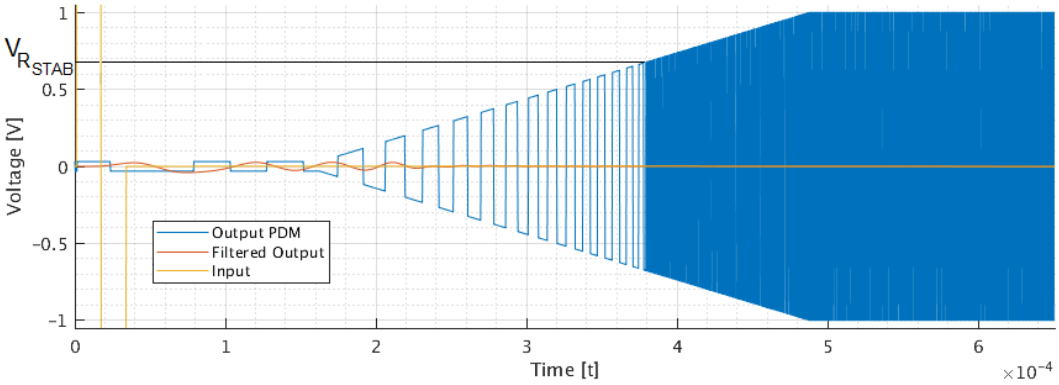

Figure 5.14: Stability condition meeting research simulation applied to CTSDM4FD8. The modulator is forced into instability, then recover once the condition is met for $V_R = V_{R_{STAB}} = 0.67V$.

At the very beginning, a *Dirac delta* (an impulsive signal) can be noticed to be implemented in order to be sure that the modulator is actually in a state of instability. This is confirmed by the pattern of the Output PDM (blue) visible in the figure, which clearly show an oscillatory behaviour.

Since in CTSDM4FD8 design VREFP/M = 1V, and since this value is greater than $V_{R_{STAB}}$, this simulation verify that the stability condition is met (for every stage).

At this point, however, the need of the second simulation, the recovery test, has shown up due to the following thought: in the first simulation, once the $V_{R_{STAB}}$ value is revealed, the input of the modulator is healthy. The second simulation verifies that if the stability condition is met and an ill signal is injected, the SDM is not going to become unstable. Figure 5.15 show the results of the simulation which were set up as explained in the diagram in Fig. 5.13. In the first column, to the left, corresponding to the period (B), the modulator behaves correctly, as we expected from Simulation 1, then, in this specific case, the ill signal chosen to be injected is a DC voltage value of 10 times the FS during all the (I) period, visible in the central column in the figure. Notice that basing on any concerning work in literature, it is expected that this signal is capable of sending any SDM in an unstable region, since in any modulator a value of MSA is discussed and it is always inferior[7] to FS. The following period (A), in the right column, shows again a correct operation instead: CTSDM4D8 has passed the test.

[7] In the author experience, no work stating MSA≥FS exist.

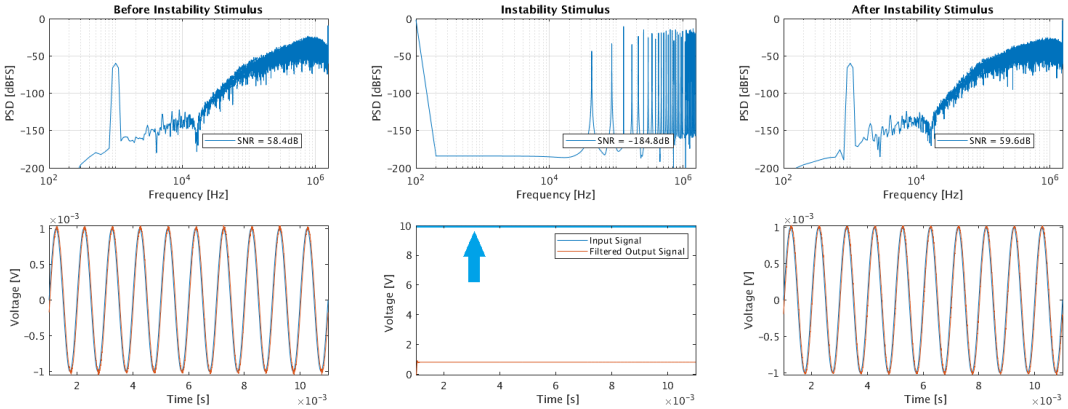

Figure 5.15: Recovery Test results: the left, center and right columns, represent period (B), (I), and (A) as defined in Sec. 5.8.2 respectively.

For completeness, a superimposition of the spectra and the transients of the left and right column is shown in Fig. 5.16, in order to easily verify that the two behaviours are almost identical, as desired. This two arguments close the check for stability this natural saturation stabilization method proposes.

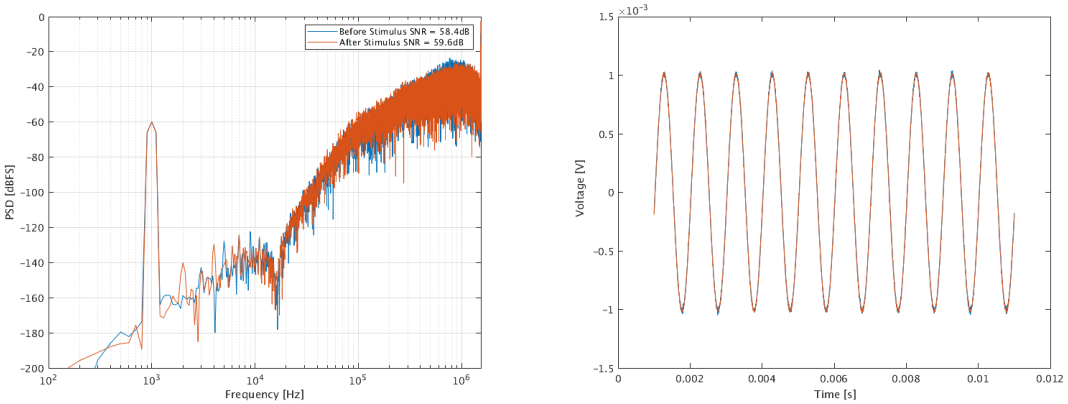

Figure 5.16: Superimposition of spectra and transients from the (B) and (A) periods of recovery test on CTSDM4FD8.

5.8.4 Precautions for Simulations Setup

There exist some precaution to keep in mind while performing Simulation 1: in order to find meaningful information regarding the stability condition, some combinations of effects, which can influence the value of $V_{R_{STAB}}$, should be avoided. These situations are reported in Appendix B. Basically, they are all about the fact that an SDM is a system which evolution over time is signal and evolution-itself dependent[8]. It is sure that, again, the key of success for these simulations, as typical in empirical studies, is the extensiveness of examples, the verification of many different scenarios with different test signals, amplitude, frequency, kind of stimuli to trigger an instability and so on.

5.8.5 Case of Criterion not Met

It is interesting to show the result of designing the modulator without respecting the stability condition. The example proposed below is simply based on keeping CTSDM4FD8 $V_R = 0.5V$. This means that the stability condition requested by this method is not met because V_R is lesser than $V_{R_{STAB}} = 0.67V$. The results are shown in Fig. 5.17.

[8]In the sense of those cases when some parameters may change, such as V_R in these discussions.

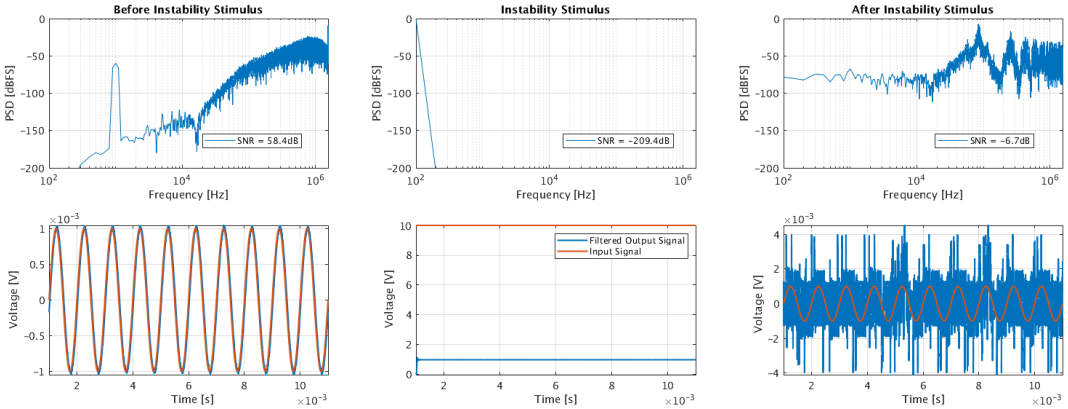

Figure 5.17: Recovery Test results in case the stability condition is not met. The modulator does not manage to recover after period (I) stimulus.

Notice that in order for the modulator to behave as normal in period (B), a low amplitude signal with no delta or forced instabilities is provided. This puts the modulator in the particular state of operating properly and in a stable way, while not meeting the stability conditions. The recovery test shows that after the stimulus which occurred during period (I), the modulator enters in an instability region and cannot manage to recover.

Also another clarification is worth spending some words: since the simulation has a finite duration, there is no way the designer can actually state that the modulator is not capable to recover *ever after*, but design-wise, a modulator should be considered not capable to recover in general if the time needed exceeds a certain period of time defined by common sense; indeed, if after 10ms, as it is the case in this simulation, the modulator has still not recovered, the situation is unacceptable and an action should be taken.

5.8.6 Finding M: sufficient, but not necessary.

About the common sense of the recovery time needed by the modulator, another interesting situation is shown in this section. It can happen that during the stability criterion meeting research (Simulation 1), no value of $V_{R_{STAB}}$ can be found: the situation under discussion is shown in Fig. 5.18, where both the classical version of CTSDM4FD8 modulator and another one obtained by only changing $VPLUS = V_S$ from 1.25V to 2V are put in comparison. Simulations are also performed in the same condition. It can be noticed that for $V_S = 2V$, the simulation does not find a $V_{R_{STAB}}$ as defined by the method, but some time after the value of $V_R = 1V$ has been reached, a stable operation can be noticed. The fact is that $V_{R_{STAB}} > 1$. It would have been found to be $1.03V$ if V_R raised higher than $1V$ during the simulation, but in this setting where V_R establishes at 1V, it emerges that stability is anyways reached after a short period. This configuration is confirmed to be stable also by the recovery test. Results for simulations showing $V_{R_{STAB}} = 1.03V$ and successful recovery test are not shown.

If we thought about the M value as defined by the method proposed, this means that the condition is sufficient, but not necessary. However, returning back to the concept of recovery time, the very definition assures that in any case stability is met if $V_{R_{STAB}}$ can be found and respected. Furthermore, this guarantees that a period of just a few samples is needed to recover from an ill signal, while no information about this amount of time can be told about the aforementioned particular case.

One last remark is about the sufficiency point of view. There is a question that could be raised about having $V_R \neq V_S$, because it is true that $V_{R_{STAB}} < V_S$ if it exist. The choice $V_R = V_S$ is always a good choice and it is easier to implement, why is it not used as default? The reason this choice was not made for CTSDM4FD8 (nor CENTO) is that a FS of 1Vpeak was desired, fixing V_R. Notice that matching $V_R = V_S$ changing instead V_S down to 1V,

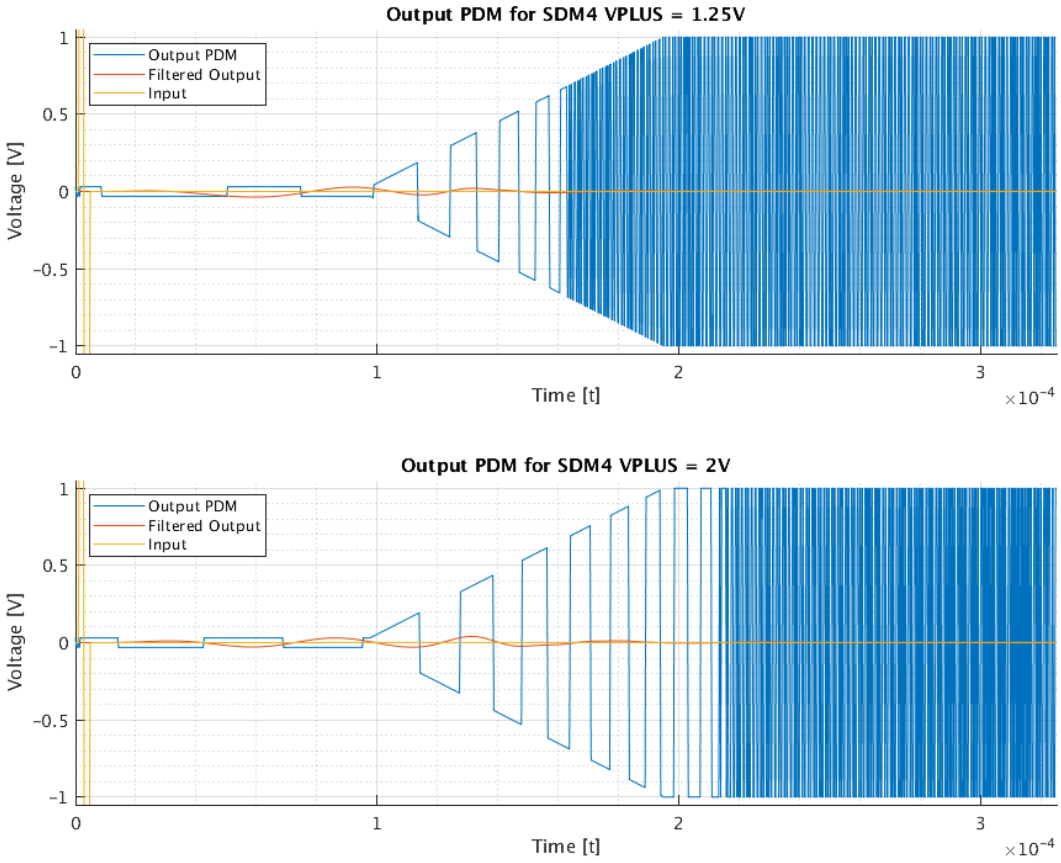

Figure 5.18: An example of situation explaining why the condition found is sufficient but not necessary: the normal configuration (top) is modified changing VPLUS from 1.25V to 2V. Though $V_{R_{STAB}}$ is not reached, the modulator becomes stable afterwards.

cannot be realised automatically for the following reason: while the values Q_i would not change due to the ratio V_S/V_R remaining constant, all the a_i should be rescaled in function of V_S. In this case, the values Q_i would change.

Choosing $V_R > V_{R_{STAB}}$ also gives a margin related to spread: combination of coefficient and supply drifts could statistically produce modulators with higher values of $V_{R_{STAB}}$, with the risk of incurring in instabilities due to conditions not met.

5.9 Conclusion

This chapter gave an overview about stability of SDM. Definitions, behaviour in case of instability and solutions found in the state of the art to avoid the modulator to persist operating in this situation have been presented in detail. A particular concern proposed in this work is about the latter: the solution can be of two kinds, that are, recovery and prevention method. The first detects an instability and acts in order to obtain a set of internal states that fall again in a region of stability, while the second guarantees that the SDM is capable of recovering an "ill" signal by its own. In audio applications, the second is far more appreciated due to the fact that there does not exist a time period while the recovery circuit has to detect and intervene. During this period, the signal is not well represented and abrupt sounds are sampled instead.

However, no solid mathematical backup exist for stability of high order SDM, making any attempt of prevention method (as they have been classified in this chapter) difficult to defend and eventually impossible to prove. In this work, an empirical method to stabilize a high order SDM has been explained in detail and applied to CTSDM4FD8, thus illustrating

its efficiency on a fourth order modulator. The study carried on within this thesis and presented in this chapter proved, with an empirical mindset and approach, that in no case a signal supposed to be impossible to handle by literature could drive our modulator in an instability region, provided that the proposed method is used.

The method has been developed basing on a CIFB structure and we did not explore an application/variant on a pure CIFF. This means that our structure would normally cost more in power consumption than the most popular CIFF structures. Hearing experience was, however, a priority with respect to power consumption, which is the reason why the highest cost in current of this structure has been accepted.

This important feature regarding CTSDM4FD8 modulator architecture concludes the high level stage of design, leading to the transistor level design phase, presented in the next chapter.

Chapter 6

Transistor-Level Design

This chapter is focused on the practical implementation of the circuit. The first step is to build it with technology devices available, which represent the *construction bricks* for all those structures whose functionalities and behaviors have been explained in the previous chapters. This procedure is carried out using Computer-Aided Design (CAD) and electrical simulators for subsequent validation.

The strategy during this procedure is to start from the circuit in its behavioural model, whose performance are known and validated. Then, devices or groups of devices are replaced with their electronic counterpart. At each substitution, the circuit performance is validated once again. This strategy allows to easily check the device that is eventually responsible of malfunctioning and performance degradation revealed by the simulation. Technological models are at a lower level with respect to behavioral and they take into account effects that are not visible at the previous higher level.

In this chapter, first, the technology used is introduced partially. The specific parameters of devices will be presented all along the chapter, whenever that specific device is involved in circuit performance. Not every aspect and challenge about this Transistor-Level Design phase will be reported, it has been decided to select only those which are the most peculiar and interesting. These will be therefore more or less related one with each other, therefore, they are just reported one by one, from Sec. 6.2 to 6.7. Their order in this chapter actually reflect the order in time these issues were encountered, studied or addressed.

The chapter then concludes presenting the final modulator parameters, its layout and the last validation step before the successful fabrication of a silicon prototype.

6.1 Technology Description

The prototype of this modulator is created on silicon using a 180nm technology named HCMOS9A [82]. This technology has been created from the digital-only technology HCMOS9: adding a double gate oxide (DGO) process, the 2.3nm became optional for digital circuit part, while a 8.5nm thick allowed to integrate analog parts capable of withstanding higher voltages. The digital part made with optional thin gate oxide is fixed at the maximum supply voltage of 1.2V, while the analog part can be supplied with 4.6V. Also high-voltage components are available, for which 20V supplies are possible to be used. Metallization choices range from 4 to 7, we chose to have 4 metals, as they are sufficient for our purpose.

It is a *mature* technology and models in the Design Kit are robust and accurate. The latter offer reliable representations for electrical simulations for all the devices available, between -35°C and +125°C: these temperatures are compatible with the standard industrial corners for Front-End (FE) manufacturing of this kind. The electrical circuit implemented is designed using Virtuoso Computer-Aided Design (CAD) tool.

Further technological characteristics necessary to the comprehension of design considerations will be shown during the chapter for the devices concerned.

6.2 Coefficients Synthesis

The behavioral structure presented in Fig. 5.1 (Ch. 4) has to be implemented electrically. The choice of architecture for each loop filter stage is to use Active-RC filters, obtaining the circuit in Fig. 6.1.

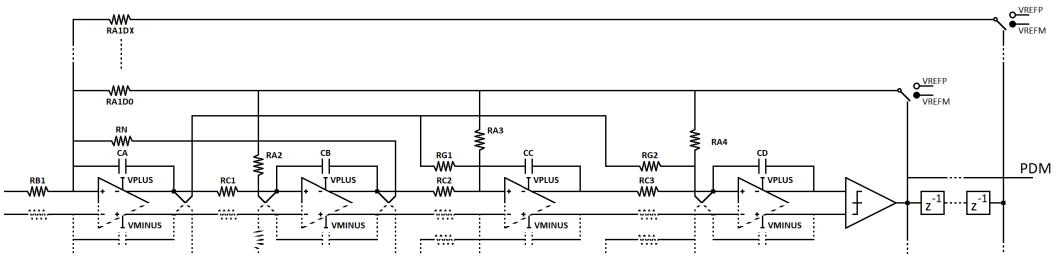

Figure 6.1: Schematic representation of CTSDM4FD8 circuit.

The relation in Eq. 6.1 must hold in order to obtain each coefficient k_i, synthesized by resistances and capacitors. For every coefficient, the labelling follow a general rule that has been decided to be k = a, b, c, g (and capitals) respectively for feedback, input, transmission and feed-forward coefficients and the subscript i = 1, 2, 3, 4 individuating the stage they are part of[1]. However, feedback capacitors are named A, B, C, D from stages from 1 to 4, to rapidly distinguish labelling from resistors.

$$k_i = \frac{1}{R_{k_i} \cdot C_{ST} \cdot f_s} \tag{6.1}$$

where the oversampling frequency is of course fixed $f_s = 3.072$MHz: the design choice will be to choose each of the resistance R_{k_i} and capacitor C_{ST} couples to obtain the requested product for each k.

There are two exceptions to Eq. 6.1. The first is that the a_1 coefficient also applies to the FIR-DAC. As a result, instead of single resistors (as in the case of RA2, RA3 and RA4 synthesizing the other feedback coefficients a_2, a_3 and a_4 respectively) there will be a parallel of 8 resistors. The following relation applies in this particular case

$$\text{RA1Dx} = \frac{8}{a_1 \cdot f_s \cdot C_A} \tag{6.2}$$

Where RA1Dx is the value of each of the 8 resistors, with [x] labelling them from 0 to 7. Notice that with this nomenclature, the delay with respect to the output PDM expressed in number of samples is highlighted. Of course, calculating the equivalent resistor due to the 8 elements in parallel, would give the value of the resistor to use in the case of the classic single-bit solution.

The second exception is about the path which creates the resonance necessary to spread a zero doublet from DC inside the bandwidth. The resistor R_N is calculated differently, referencing to Eq. 4.1 in Ch. 4 the implementation requires that

$$R_N = \frac{f_s \cdot c_1}{C_A \cdot (2\pi \cdot 0.789 \cdot f_B)^2} \tag{6.3}$$

where this time, besides coefficient c_1 and audio band $f_B = 20$kHz, the value of the first stage feedback capacitor C_A appears.

Once all the relations between coefficients and electrical devices are known, there are some aspects to take into account when making the decision on how to size capacitors and resistors.

Thermal noise budget - The first and most important is thermal noise and affect mostly sizing the first stage. Generally, the highest contributors in thermal noise are input resistors and some transistors present in the first stage amplifier (see further in Fig. 6.5)

[1] With the exception of g1 and g2 which only represents the lower and higher feed-forward path.

and most of the devices of subsequent stages are negligible. Input resistors will be basically fixing the choice for the first RC product.A detailed report about thermal noise calculations will be carried on in Sec. 6.3.

Upper and lower limits in capacitors size - This aspect is actually more about size of capacitors consequent to resistors choice, because resistors determine directly some features such as thermal noise floor and reference current consumption. The latter two performance parameters are in fact those proposed for this discussion.

For what concerns thermal noise floor, if the guideline is to reduce thermal noise as much as possible, then a small input resistor is needed and consequently, the size of the feedback capacitor of the first stage increases. As forecast in Ch. 4, Sec. 4.6.3, once the nominal value of the capacitor is identified, a +35% in value and size should be taken into account for trimming in HCMOS9A technology[2].

At the same time, there is also a lower bound on capacitors. For example, a high resistor value choice could be driven by reference power consumption on feedback paths. The highest the feedback paths resistors, the lowest the reference power consumption, since a lower current would flow through these paths. Consequently, the capacitors would decrease in value and the modulator would tend to experience a more severe distortion.

These two arguments of discussion, combined to the one just upcoming, will lead to the capacitors value decision explained just after.

Common feedback capacitor per stage - Each coefficient relative to a same stage share the same C_{ST}. This means that if a particular resistor is desired with an as high/as low as possible value, it should be noticed that also other resistors creating an RC product with the common stage feedback capacitor are constrained by this choice.

So, the choice for capacitors values was made dividing the modulator in first stage and subsequent stages. The first stage has been designed with the input resistor sufficient to have at least a -103dB floor, as it will be discussed further in Sec. 6.3. It is worth at this point to anticipate some numeric values given at the end of this Section and stored in Tab. 6.1, in order to proceed with this comment in a more clearer way. The input resistance value chosen to comply with the -103dB noise floor is 24kΩ, therefore a 74pF capacitance value is needed for the first stage feedback capacitor. It has been decided not to improve thermal noise via the input resistor, because with the +35% just discussed, the minimum total value possible for this design already reaches 97.2pF. This value has been forecast to use a great part of surface in the layout phase. The subsequent 3 stages are relaxed in term of thermal noise, the RC product can be realized with resistors of higher value, in order to keep a lower surface occupied by capacitors. The design choice was to keep all 3 capacitors of the last stages of the same value of 3pF in order to keep an easier CAD and subsequently layout implementation. This value is the least (margins considered and included) allowing at the same time to use the same value for all three and to avoid SNR degradation due to distortion.

Conflict with common mode feedback resistors of integrators - This aspect is especially related to "c_i" coefficients (stage-to-stage transmission coefficients). It is important to take into account what is actually inside the *black box* named OPA. Each integrator output not only feeds the following stage through RCn resistances, but are also connected the common mode feedback circuit of the OPA which, as it will be seen in Sec. 6.4, has been implemented with resistive inputs. If coefficients resistors were of the same order of magnitude of the common mode feedback, this circuit could draw significant current, consequently corrupting SDM operation.

Reminding that all of them have been chosen in order to replicate CENTO NTF, which performance was already known, the values used to implement CTSDM4FD8 coefficients electrically are reported in Tab. 6.1.

[2]As well as many other technologies: often the order of magnitude for technology spread is similar.

Table 6.1: Modulator Parameters

Label	Value	Unit	Label	Value	Unit
VPLUS/MINUS	±1.25	V			
VREFP/REFM	±1	V	RC1	660	KΩ
Fs	3.072	MHz	RA2	440	KΩ
C_A	72	pF			
C_B	3	pF	RC2	406	KΩ
C_C	3	pF	RA3	232	KΩ
C_D	3	pF	RG1	820	KΩ
RB1	24	KΩ	RC3	326	KΩ
RZS	708	KΩ	RA4	262	KΩ
RA1D0/.../7	200	KΩ	RG2	660	KΩ

6.3 Thermal Noise

As introduced in Ch. 2, Sec. 2.2.7, the design of CTSDM4FD8 is such as Thermal Noise is the dominant source in the total budget. In particular, the thermal noise floor is set at -103dBFS, with jitter and quantification noise no higher than -108dBFS, meaning roughly 50% thermal, 25% jitter and 25% quantification. It is self evident then, that this aspect should be quantitatively known and then controlled. For this purpose, the combination of two kind of simulations have been set up and considered. Their discussion and setup will be carried on in Sec. 6.5, after a comment about temperature drift in the next upcoming paragraph and Sec. 6.4 presenting the operational amplifiers (OPA). The OPA, more precisely the transistors composing them, represent the other source of thermal noise affecting the SDM to be introduced, along with arguments about resistances made so far.

Temperature Drift

Before presenting simulations, another non-ideality related to temperature has to be introduced: temperature drift. Temperature affects the behaviour of several devices. An important example is about resistors: resistance value of RHIPO resistors depends on temperature as follows

$$R = R_0\big|_{T_{ref}} \cdot \left(1 + TC_1 \cdot (t - T_{ref}) + TC_2 \cdot (t - T_{ref})^2\right) \tag{6.4}$$

where R_0 is the nominal value at standard temperature $T_{ref} = 27°C$ and, for HIPO resistors, $TC_1 = -2.7 \cdot 10^{-3}$ and $TC_2 = 6.3 \cdot 10^{-6}$ are the first and second order temperature coefficient respectively. This model, as per technology standard, is valid in the temperature range between -35°C and +125°C.

A design has to be robust on the whole temperature range. This means that each resistor value will experience a drift which is at the origin of two worst case ratios: we define the ratios $R_{TDH} = 1.192$ and $R_{TDL} = 0.796$ with respect to nominal value as the upper and lower worst case resistance value drifts due to temperature. Notice also that, since RHIPO resistors are polysilicided, the first order temperature coefficient is negative: this means that the highest value of resistance is obtained with the lowest temperature and vice versa, contrary to classic notions about metallic resistances.

The example about the resistor has been explained in details due to its direct impact on several aspects of modulator and circuit design, such as noise budget and RC-Product spread. All the *noisy* devices in HCMOS9A are in any case provided with models integrating thermal drift effects.

6.4 Operational Amplifiers

The four OPA used for each stage integrator have been studied and designed by the master student Massimo Morabito, during a 6 month internship. His task was to evaluate various OPA architectures in order to find the best in term of power consumption.

A remarkable advantage is that the four OPA can be designed specifically for their *context*: the environment is well defined by the design of the ADC. For example, capacitive and resistive charges are known for every stage, as well as output current requisites which can be forecast by electrical simulation with behavioral models. Other parameters such as slew rate, bandwidth and open loop gain can be individuated using the theoretical aspects linking Amplifiers performance specifically to Sigma-Delta, arguments that have already been presented in Ch. 2, Sec. 2.2.1. Applying this knowledge to our case give specific requests for OPA design of CTSDM4FD8. With respect to this last reference to the theoretical section, during the design phase where other non-idealities and details are unveiled, new constraints and considerations should complete the information available. For example, for what concerns open loop gain, it has been seen that a very low value (as low as OSR) can be sufficient. While a transistor implemented OPA is introduced, virtual grounds will no longer be identical, and the difference is proportional to $1/A$. This *aperture* in the virtual ground cause distortion and should be therefore kept low. This is why a more classic gain of 80dB is targeted: in Ch. 2, Sec. 2.2.1 it has been seen that there exist a lower limit, but then the value can be freely chosen to be higher and the SQNR is preserved. The benefit of choosing a higher value is that distortion is reduced according to the previous argument about dynamics on input voltage nodes. An important remark is that the value of 80dB, as for many other specifications all along the whole design at different levels, has been chosen based on ST Design Team experience. Of course it would be interesting to explore every single decision and optimize it, however, the 3 years time budget dedicated to this thesis as well as the 6 months for the internship, often had to be organized prioritizing a limited number of aspects, above all, concluding with the fabrication of a well performing silicon prototype. This is why the constraints we provided to create the framework of the internship guided Massimo to use values that were sufficient to fulfill their tasks.

Another interesting fact worth to mention about designing OPA specifically for CTSDM4FD8 is that the first stage bandwidth and slew rate requirements to withstand switching operation of feedback DAC paths are relaxed by a factor of 8 due to the presence of the FIR-DAC.

During the internship, several OPA architectures have been tested and the one which was finally chosen is reported in Fig. 6.2, with device dimensions for the first stage. It is a two-stage miller compensated. A cascoded structure is employed in the first stage and the Common Mode FeedBack (CMFB) circuit is realised adjusting the current flowing in the active load.

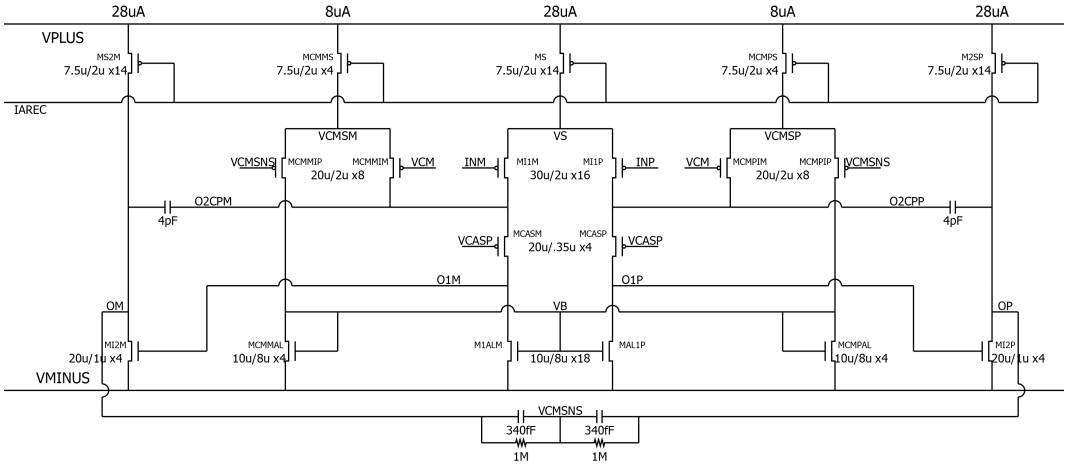

Figure 6.2: Schematic of the OPA implementing the first intagrator. The following 3 OPA have the same architecture, only changing in device sizing due to relaxed constraint.

The noise budget is also known: since resistors are fixed by modulator design (see Sec. 6.5.1 for more details), the thermal noise budget for the four OPA is known. The design can therefore be organised as to share this budget among the four OPA as to obtain the most power-efficient combination: more than the 85% of the thermal budget is placed on the first integrator.

All specific performance parameters of OPA in their final version are resumed in Appendix C.

OPA1 Offset Trim

Typical differential offset using PDOMOS50v devices of the HCMOS9A technology is in the order of the millivolt. Thanks to this forecast, Eq. 2.12 can be used, to realize that the expected tones appear in the audio bandwidth. Since this tone is audible, it is mandatory to employ a compensation technique in order to ensure a proper experience to the listener.

The offset can be easily measured and canceled digitally *a posteriori*. However, as it has been seen for compensation techniques for stability (Ch. 5, Sec. 5.4.4), the compensation is performed at the output, but not inside the feedback loop. An error would in any case circulate in the loop, corrupting the output. This is the reason why a compensation technique applied directly to the source is preferred for sigma delta modulators. The strategy to compensate offset exploits the following fact: the frequency of the tone generated is directly proportional to offset magnitude and the A-Weighted filter attenuates frequencies lower than 1kHz. An attenuation of -3.66dB is present at 460.8Hz, corresponding to $V_{OS} = 150\mu V$. The design choice is then to lower the offset to this value or less. To do this, the structure in Fig. 6.3 is used. Depending on the differential offset outcome in the input pair (not shown in the picture) a ratio of current is drawn away from the active loads M1ALM/P thanks to an array of transistors of different size, capable of drawing from 25nA to 1,575μA. This circuit allows to reduce any offset statistically possible to a maximum of $V_{OS} = 150\mu V$, which means $f_{IDLE} = 460.8Hz$.

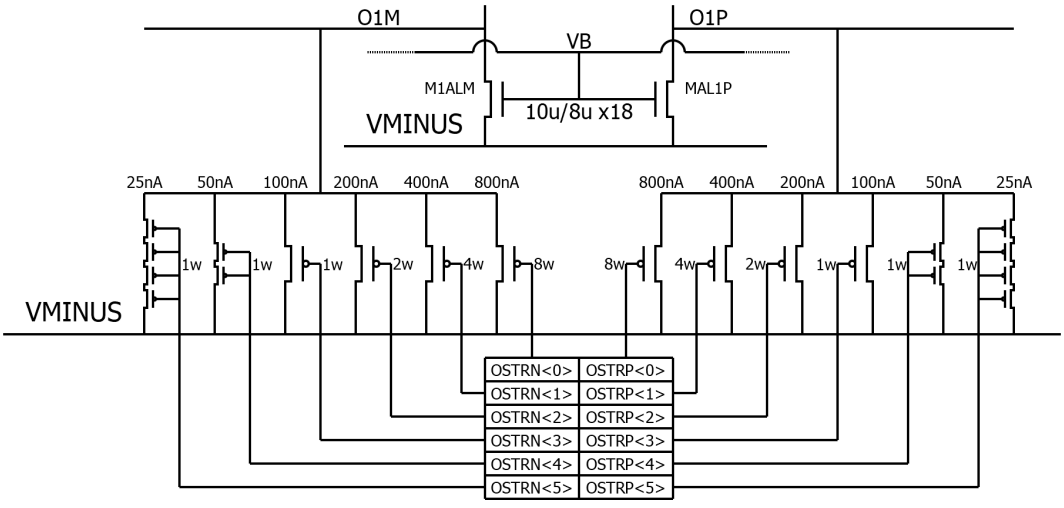

Figure 6.3: Offset compensation circuit for the first OPA. An array of 6 branches per side draw current away from active loads, thanks to transistors different in size. W is the "base-width" of each device. Currents in power of two from 25nA to 800nA can be combined.

6.5 Thermal Noise Simulations

In this Section, the two kind of thermal simulation used to quantify thermal noise within the budget and introduced earlier are presented. The first, analyzed in Sec. 6.5.1 consist in linearizing the system and run a frequency analysis, the second, explained in Sec. 6.5.2, is

a transient simulation with thermal noise sources. In this section, both simulations setups, results, insight provided and limits are explained in details.

6.5.1 Linearized System Analysis

The CTSDM4FD8 is *linearized* by removing the comparator, the FIR and recreating the loop by crossing the outputs of the fourth-stage integrator DOP/DOM back to the resistance parallels RA1DxM/P respectively as shown in Fig. 6.4.

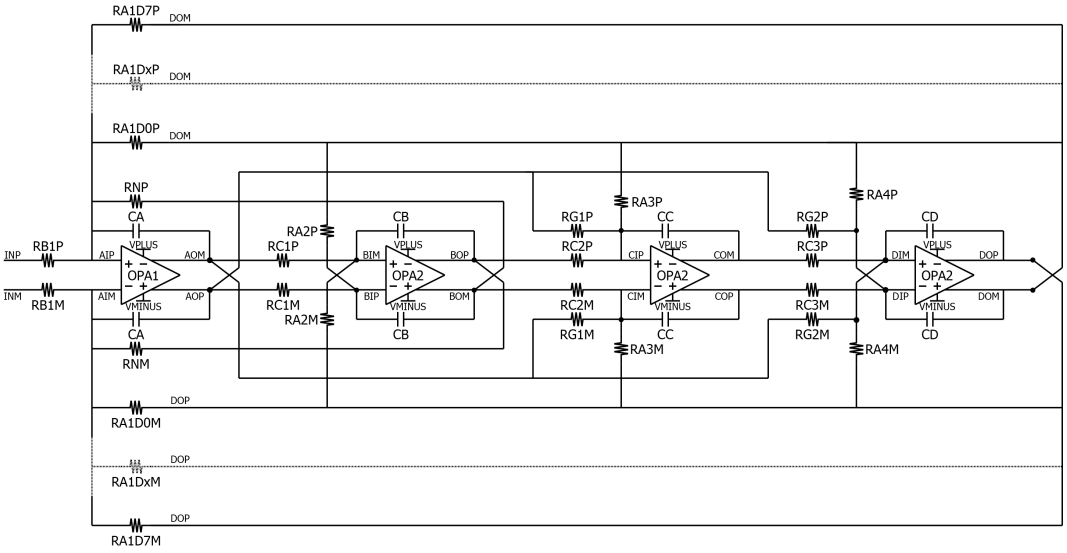

Figure 6.4: Schematic representation of CTSDM4FD8 circuit specifically designed for frequency analysis.

A frequency analysis named .AC is then performed. An .AC analysis is useful to determine transfer functions. There also exist other more specific kind of .AC analysis, in our case, we are interested to the one named .NOISE. In this frequency analysis, all devices provided with a noise model can be activated. The outputs produced are two spectra named .INOISE and .ONOISE which represent respectively the input and output referred noise spectrum.

There are just a few more adjustments linked with this specific circuit: the input is appropriately decomposed into a fully differential signal and then the quantity[3] DO=DOP-DOM is considered. The A-Weighted filter is added as well afterwards. The last adjustment is to consider a flat gain of 24/25 for the following reason: in fact, the necessity of this last step is that .INOISE is an unfiltered quantity. In order to have an A-Weighted result, .ONOISE must be considered, then referred to the input. Since the loop filter can be considered as a structure having a gain of RAD1x/(8·RB1), this last adjustment allows to compensate it in order to refer the whole A-Weighted system noise to the input.

Noise Contributors Forecast

When a .NOISE simulation is performed, a list of all noise contributors with their own contribution is created. Each device whose noise model was activated, will be shown in the list, in decreasing order of contribution: the most noisy devices may be therefore individuated and monitored by filling up tables like in Fig. 6.5.

In this representation, the situation at -35°C and +125°C standard temperatures are shown along with the 27°C room temperature. Data is expressed in V_{RMS} as it is the contribution over the band which was set up in the simulation. As it can be noticed, the first

[3]Notice that DO is not present in Fig. 6.4, but it is calculated within the complete bench set up in the CAD environment.

T [°C]	-35	T [°C]	27	T [°C]	125
Source	Contribution	Source	ontribution	Source	ontribution
	V		V		V
TOTAL AW	8.523E-06	TOTAL AW	8.568E-06	TOTAL AW	8.869E-06
STHNR dB	-104.40	STHNR dB	-104.35	STHNR dB	-104.05
OPA1.MAL1P	2.633E-06	OPA1.MAL1P	2.862E-06	OPA1.MAL1P	3.114E-06
OPA1.MAL1M	2.633E-06	OPA1.MAL1M	2.862E-06	OPA1.MAL1M	3.114E-06
RA2M	2.416E-06	RB1M	2.295E-06	RA1DxP (8x)	2.309E-06
RA2P	2.416E-06	RB1P	2.295E-06	RA1DxM (8x)	2.309E-06
RB1M	2.226E-06	RA1DxP (8x)	2.242E-06	OPA1.MI1M	2.731E-06
RB1P	2.226E-06	RA1DxM (8x)	2.242E-06	OPA1.MI1P	2.731E-06
RA1DxP (8x)	2.175E-06	OPA1.MI1P	2.166E-06	RB1M	2.363E-06
RA1DxM (8x)	2.175E-06	OPA1.MI1M	2.166E-06	RB1P	2.363E-06
RC1M	1.968E-06	RA2M	2.164E-06	RA2M	1.851E-06
RC1P	1.968E-06	RA2P	2.164E-06	RA2P	1.851E-06
OPA1.MI1M	1.858E-06	RC1M	1.762E-06	RC1P	1.507E-06
OPA1.MI1P	1.858E-06	RC1P	1.762E-06	RC1M	1.507E-06
RA3M	1.191E-06	RA3M	1.009E-06	OPA1.MCMMS	1.079E-06
RA3P	1.191E-06	RA3P	1.009E-06	OPA1.MCMPS	1.079E-06
RC2M	8.997E-07	OPA1.MCMMS	8.665E-07	RA3M	8.187E-07
RC2P	8.997E-07	OPA1.MCMPS	8.665E-07	RA3P	8.187E-07
OPA2.MAL1P	7.843E-07	RC2M	7.617E-07	OPA2.MAL1P	7.038E-07
OPA2.MAL1M	7.843E-07	RC2P	7.617E-07	OPA2.MAL1M	7.038E-07
OPA1.MCMMS	7.241E-07	OPA2.MAL1P	7.533E-07	OPA1.MCMPIM	7.014E-07
OPA1.MCMPS	7.241E-07	OPA2.MAL1M	7.533E-07	OPA1.MCMMIM	7.014E-07
RA4M	6.880E-07	OPA2.MI1M	5.738E-07	OPA1.MCMPIP	7.001E-07
RA4P	6.880E-07	OPA2.MI1P	5.738E-07	OPA1.MCMMIP	7.001E-07
RG1P	6.363E-07	RA4M	5.702E-07	RC2M	6.183E-07
RG1M	6.363E-07	RA4P	5.702E-07	RC2P	6.183E-07

Figure 6.5: Main contributors in thermal noise for -35°C, 27°C, +125°C. Each source is highlighted with colours depending to the stage they belong to: red for 1st, yellow for 2nd, green for 3rd and blue for 4th.

OPA active loads keep always their first position as most noisy elements of the circuit, followed by input resistors RB1, FIR-DAC resistors RA1Dx and first OPA input pair. Notice that while at -35°C, feedback resistors of the second stage RA2 appear as the second contributors. This is because since resistors are implemented with high resistivity unsilicided poly (RHIPO), the first order temperature coefficient is negative (Sec. 6.3). Then, consider RA2 = 406KΩ: there is a factor of ≃16 with respect to RB1 = 24KΩ as well as the parallel of the 8 RA1Dx which corresponds to "RA1" = 25KΩ. This means that the former will be in fact more affected by temperature coefficient than the latter, because the resistance value multiplied is 16 times higher.

In any case, these results can be found to be coherent to the fact, often invoked during this thesis, that the first stage contains the most important contributions while the following impact less on the total noise. In fact, considering the standard 27°C, the first 3 devices make 50% of the total budget, while the first most noisy device of the third stage appears once 85% of the noise budget has been represented.

This kind of simulation is very useful when sizing the modulator and then when organizing the share of thermal noise budget among the four OPA. The limit is that it is applied to an approximated (linearized) system which reflects just partially an SDM. A real insight about the spectral shaping mechanics is available using Noise-Transient simulations, explained in the next Section, where input resistor flicker noise is discussed.

6.5.2 Noise-Transient Simulations

Though really time expensive, this kind of simulation give genuine information about the contribution of thermal noise in a noise-shaped system. The command .NOISETRAN allows to activate noise models for those devices which do have one within the Design Kit and which

is activated. Activation of this model is in fact possible for each single device individually, or a category (same device, same "cell" and so on) and this is a very powerful option. Thermal models for this simulations automatically generate an array of independent sine wave sources, with evenly spaced frequencies and amplitude according to each frequency. This approximates the spectrum of noise the device would inject and this input is placed in the circuit as a part of that same device. There exist the possibility of changing the number of sine-wave generators that describe the spectra of each device whose model is activated during the simulation: the more the number of generators in the same bandwidth, the better the approximation, but simulation time will inevitably increase.

Even though simulation time is in the order of magnitude of several days, .NOISETRAN simulations really helped in design, the most relevant example is discovering input resistance flicker noise impact, which otherwise could never be addressed.

Input Resistance Flicker Noise

The resistance values of RHIPO resistors are defined in the CAD tool through geometrical attributes. From the Design Rule Manual (DRM), the resistivity per square micrometer $[\Omega/\mu m^2]$, also referred to as "sheet resistance", of a device is known (see further in Tab. 6.2) and the width (W) and the length (L) can be set to obtain that surface value necessary to implement the desired resistance value. Since the same rectangular surface can be obtained by several combinations of W and L, the most intuitive design choice would be to have W and L the least possible, to spare surface.

Performing a .NOISETRAN simulation reveals a situation such like in Fig. 6.6, where the red curve shows a 1/f shape. The green curve represents the situation after this issue was fixed, it will be explained just after the upcoming general remarks about this graphics and the discussion about what does the red curve represent.

This situation highlights also the importance of controlling performance over the entire dynamic range: this behavior manifests itself in an evident way only at high input level, as it can be seen in Fig. 6.7 (red curve). More details are available: this issue showed up once the behavioral resistance model were substituted by RHIPO models. Thanks to this observation, an hypothesis about a link with the model representation only was investigated.

Finally, the answer to this red curve degradation came from RHIPO characterization in HCMOS9A database: the model for thermal noise in transient simulation represent the following equation:

$$Si^2(f) = \frac{4kT}{R} + \frac{K_f}{WL} \cdot \frac{1}{f} \cdot I^{A_f} \tag{6.5}$$

Where $Si^2(f)$ is the noise spectral density (A^2/Hz), R is the resistance value (Ω), f is the frequency (Hz), I is the current crossing the resistor (A), k is the Boltzmann constant and A_f and K_f are the flicker noise model coefficients. They are extracted for each supported resistor. In our case, for the input resistance RB1: R=24kΩ , 30μA_p flow through at -3dBFS and for RHIPO resistors K_f=2.3·10^{-9} $\Omega\mu m^2$ and $A_f = 2$. From this formula it appears that a *flicker* component exist for HCMOS9A resistors[4] and the dependence from input power level results clear. It is as well clear that the way to decrease this contribution is to increase the WL product: the greater the area of the resistor, the lower the flicker noise.

A factor of 10 with respect to the minimum size was found to be optimal for RB1 as it can be seen looking at the yellow curve in Fig. 6.7. Even if it is clear from the high power input level part of the DR plot that RB1 is the major responsible for flicker impact, performance is actually fully recovered when all the other resistors are increased in surface by a factor of 2 with respect to their minimal size.

[4]The model is valid for all resistors available in the technology, with different K_f and actually the same A_f.

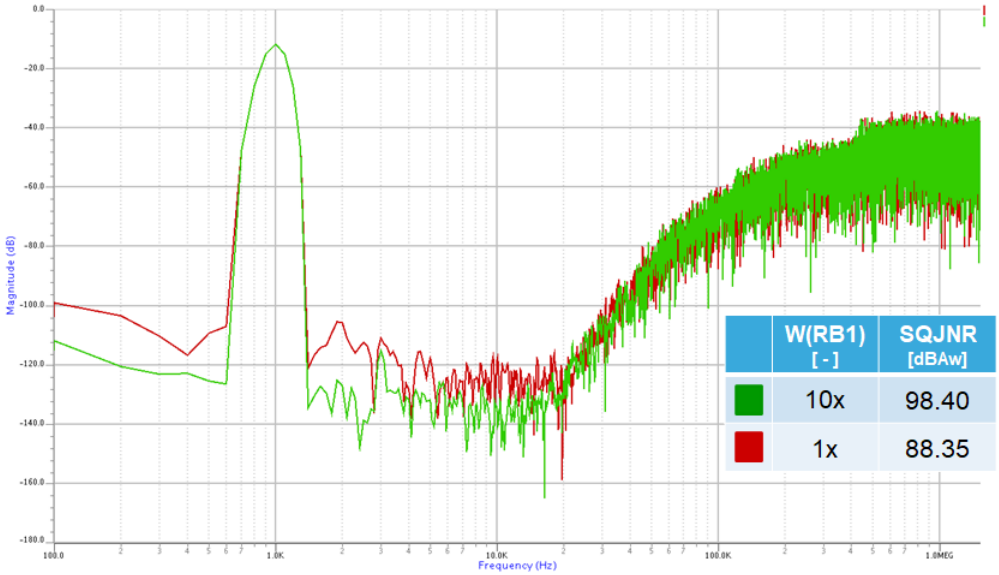

Figure 6.6: Flicker noise arising in-band in function of RHIPO resistors width W(RB1). Dynamic Range is compromised at high input power level if the least HIPO width allowed by technology rules is used (red curve). Adding a factor of 10 on both input resistors (green curve) recover this issue.

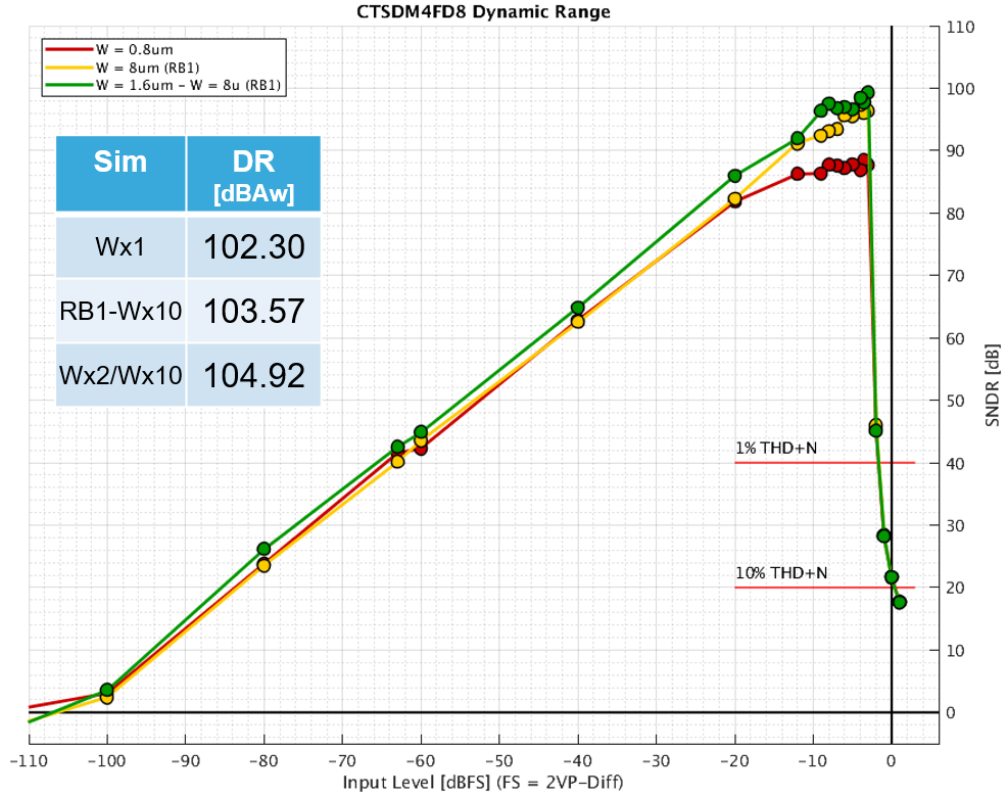

Figure 6.7: Dynamic Range using RHIPO resistors with a width W times the least allowed by technology. The examples reported are:
- Wx1 with minimal geometrical dimensions for all RHIPO resistors (red)
- RB1-Wx10 with increased width of RB1 of a factor of 10 (yellow)
- Wx2/Wx10 like the previous, but increasing all the other resistors by a factor of 2

6.5.3 Thermal Noise and Total Noise Budget

As presented at the beginning of this section about Thermal Noise (Sec. 6.3), thermal noise should be the dominant source and all other sources should be under control. An efficient graphical visualization can be given in Fig. 6.8, thanks to the results of the simulations just introduced. This image confirms that the budget has been respected and that thermal noise is still dominant: both jitter and quantification noise are lower than the 25% prefixed.

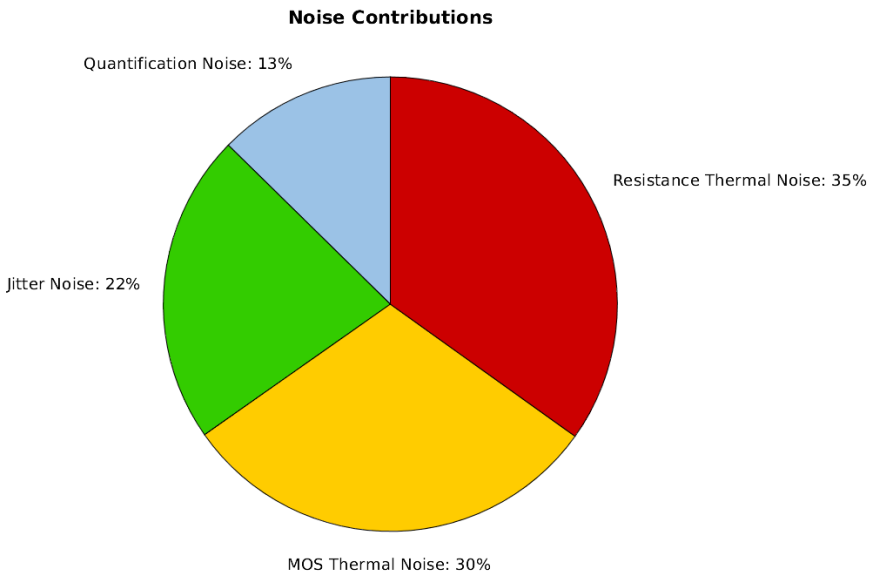

Figure 6.8: Noise Budget of CTSDM4FD8. Thermal noise value is the one found in .AC simulations, divided in Resistors and MOS contribution and summing up to 80.02% of the total.

6.6 R and C Spread

Spread is a non-ideality that affects nominal values for every device present in a circuit. The major issues selected to be presented in this section is about spreading of resistors and capacitors only. This is why only these two devices will be explained in details. As previously mentioned, when a device is designed, generally, geometrical characteristics are given. In the case of resistors and capacitors, W and L are specified such as the resulting area times the resistance or capacitance per unit area, respectively, gives the desired value. When manufactured, several causes can concur to cause this value to drift from nominal: statistical spread, lot (silicon wafer) spread and the impossibility of reproducing perfectly sharp shapes. These fluctuations in device parameters after fabrication on silicon is what is called technology spread and cannot be avoided. Statistical analysis is available and implemented in models, in order to allow the designer to simulate the circuit with spread impact. It is then an additional task for the designer itself to foresee the impact of spreading of the circuit after fabrication.

For HCMOS9A technology, spread expected on resistors and capacitors are reported in Tab. 6.2, showing that the nominal value chosen by the designer can drift up to 20% for HIPO resistors and 15% for MIM5f capacitors. Both devices are used for coefficient synthesis of CTSDM4FD8.

Table 6.2: Technology Spread Parameters

	Parameter	MIN [x/μm^2]	TYP [x/μm^2]	MAX [x/μm^2]	Notes
HIPO	ρ	4.8	6	7.2	Sheet resistance
MIM5f	C_0	4.25	5	5.75	Elementary MIM capacitance

6.6.1 Spread Influence on Thermal Budget

Since spread can happen to produce resistors which are up to +15% their nominal values, intuitively, thermal noise of each of these devices should increase to a worst case of +15%. This effect has to be combined with temperature drift and simulated in the whole context where also other noisy elements like transistors (or resistors with different Thermal Coefficients) are taken into account.

For completeness all cross-case (combinations) are shown in Tab. 6.3 where the worst case is represented by having +15% increased resistors at +125°C. These simulations reveal that the -103dB noise floor margin is still respected.

Table 6.3: Spread Influence on Thermal Budget

R [-]	T [°C]	ONOISE [μV_{RMS}Aw]	ONOISE [dBAW]
TYP	27	8.568	-104.35
MAX	-35	9.052	-103.88
MAX	27	9.041	-103.89
MAX	125	9.275	-103.66
MIN	-35	7.960	-104.99
MIN	27	8.067	-104.88
MIN	125	8.444	-104.48

6.6.2 RC-Product Trim

As it has been seen in Ch. 4, R and C spread represent a major issue in coefficient synthesis for a CTSDM. The combination of the two spreads, which are independent, may produce a spread on the RC product as high as ±35%. This value is impossible to handle and the NTF would change dramatically, compromising the entire design. The RC-Product should be trimmed such as it has a worst case drift of ±5.5%, value which was found in simulations shown in Ch. 2, Sec. 2.2.2.

To do so, the decision is to trim feedback capacitors. The advantages in doing so and not trimming the resistors are self-evident:

- capacitors are 8 devices in total, while resistors are 22: less circuitry is necessary
- resistors are to be trimmed using series of elementary resistors: switches used to trim add their non-idealities such as R_{ON} in series
- resistor matching is achieved (Sec. 6.9) by using elementary resistors in combinations of series and parallels. Achieving both trimming and matching technique require more design effort with respect to trimming capacitors

Capacitors are trimmed by substituting the monolithic nominal-value MIM5f capacitor by a an array of identical elementary capacitors C_E in parallel, as shown in Fig. 6.9.

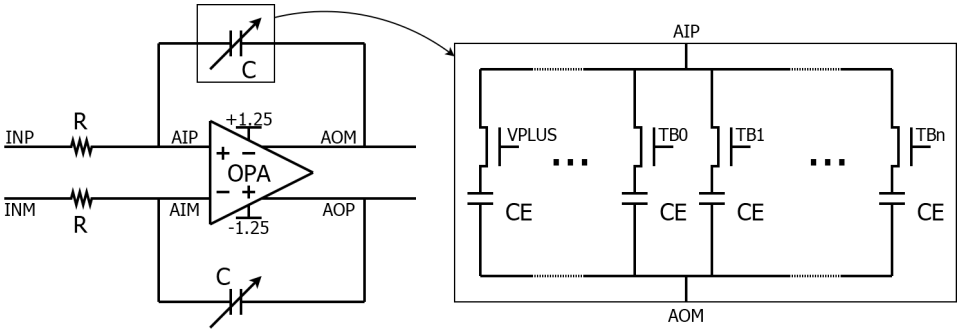

Figure 6.9: RC-Product trim proposed using a variable capacitor to place in each integrator feedback path. The value of the capacitor depends on how many elementary capacitors C_E are switched on.

The principle of operation is simple: capacitors C_E each have a corresponding switch and its state determines whether that specific elementary capacitor counts in the total parallel capacitance. This total value would be chosen as to compensate the spread on both R and C in order to obtain the nominal RC product. In order to do this, the variables which the designer can control in this array are the value of C_E and the number of switchable elements in the array N.

The value of each C_E determines the maximum coefficient spread after trim, or RC-Product spread tolerance, which, as it has been seen, should not be higher than 5.5% and the number of switchable elements should be as many as to cover the range between the two worst RC cases of ±35% with respect to nominal value needed.

Since a signal bus of log(N) bits is necessary to program the array, there exist another design-wise variable that has to be monitored: N_{FXD} denotes the number of fixed element of the array, that is, elements whose switch is statically connected to VPLUS. In fact, there is a minimum value of C that has to be represented[5], therefore, a number of switches would always be set to on. With this choice, only $N - N_{FXD}$ elements have to be actually switched. This last number is here defined as N_{SW}.

Before setting up the system of equations that determine these variables, one last important parameter has to be included and it is thermal drift: capacitors must also be capable of including resistance thermal drift in the range which divides the two worst cases.

With all of these arguments taken into account, the system of three equations necessary to find C_E, N and N_{FXD} is the following

$$\begin{cases} \boldsymbol{C_E} \cdot (1 + C_S) = 2 \cdot RC_{TOL} \\ (\boldsymbol{C_E} \cdot (1 - C_S)) \cdot \boldsymbol{N} \cdot (1 - R_S) \cdot R_{TDL} = 1 - RC_{TOL} \\ \boldsymbol{N_{FXD}} \cdot (\boldsymbol{C_E}(1 + C_S)) \cdot (1 + R_S) \cdot R_{TDH} = 1 + RC_{TOL} \end{cases} \tag{6.6}$$

Where variables have been noted in **bold** characters to distinguish them from all parameters: are maximum expected spread for capacitors C_S and resistors R_S, RC-Product spread tolerance RC_{TOL} that is the 5.5% value already commented, and the highest and lowest possible thermal drift for resistors R_{TDH} and R_{TDL} respectively. These parameters are all ratios (normalized to 1) and their values are the following

$$\begin{cases} RC_{TOL} = 0.055 \\ R_S = 0.20 \\ C_S = 0.15 \\ R_{TDH} = 1.192 \\ R_{TDL} = 0.796 \end{cases} \tag{6.7}$$

[5]That is, the +35% RC worst case.

Notice that the two thermal drift values are obtained by applying Eq. 6.4, in the cases t = 125°C and t = -35°C.

The solution to the system is the following

$$\begin{cases} CE = 0.0957 \\ N = 19 \\ N_{FXD} = 6 \\ (N_{SW} = 13, 4\text{bit}) \end{cases} \tag{6.8}$$

At this point, a design consideration can be made: a 4bit bus is the minimum size necessary to cover all worst case range and RC-Product spread tolerance, but only 13 switches ($= 19 - 6$ as by System 6.8) are actually coded in this solution. There is still place for 2, as 4bit can represent a thermometric code for 15 switches. The final choice for C_E, N and N_{FXD} is then

$$\begin{cases} CE = 0.0834 \\ N = 22 \\ N_{FXD} = 7 \\ (N_{SW} = 15, 4\text{bit}) \end{cases} \tag{6.9}$$

for which the schematic implementation is shown in Fig. 6.10. Notice that this configuration, considering the first equation of System 6.6, means that the modulator coefficients (or RC-Product) spread will be at maximum 4.8%.

An alternative explanation of this choice, obtained by solving a system of equations is provided graphically in Fig. 6.11 where the total capacitance value, expressed as a ratio of the nominal value, is shown as a function of the number of switched-on elements in the capacitors arrays.

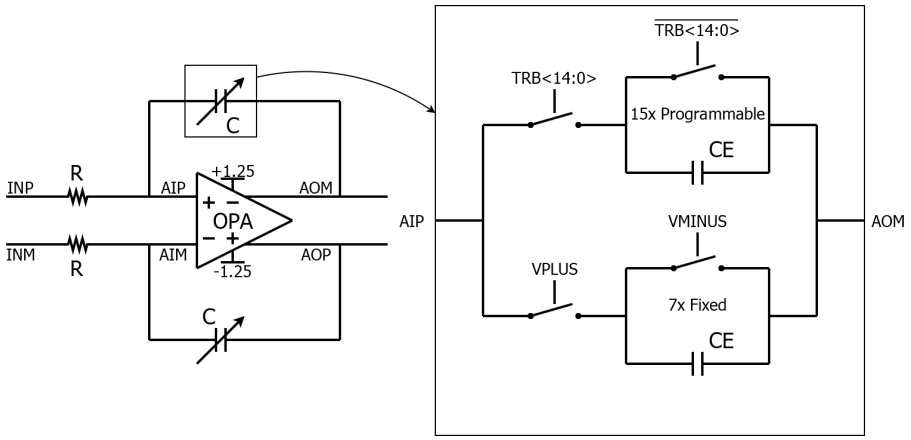

Figure 6.10: RC-Product trim proposed using a variable capacitor to place in each integrator feedback path.

The capacitance value needed to compensate remarkable corners are shown as colored horizontal lines: blue for typical and spread due to technology and red taking also into account temperature drift. The situation is easier to visualize if, as it is the case in the picture, the influence of resistance and capacitor independent process variation is broken down into two separate representations: lines take into account compensation necessary for resistors, while capacitor spread is represented by the three curves noted with circles. Each of the three shows the values covered in corner cases for capacitance. It is proven that 7 fixed capacitors are sufficient to compensate the worst case of RMAX, TMIN and CMAX, corresponding respectively to resistor spread case $1 + R_S$, temperature T=-35°C and capacitors spread case $1 + C_S$. At the same time, 22 elements all switched on can reach the opposite worst case of having RMIN, TMAX and CMIN, corresponding to $1 - R_S$,

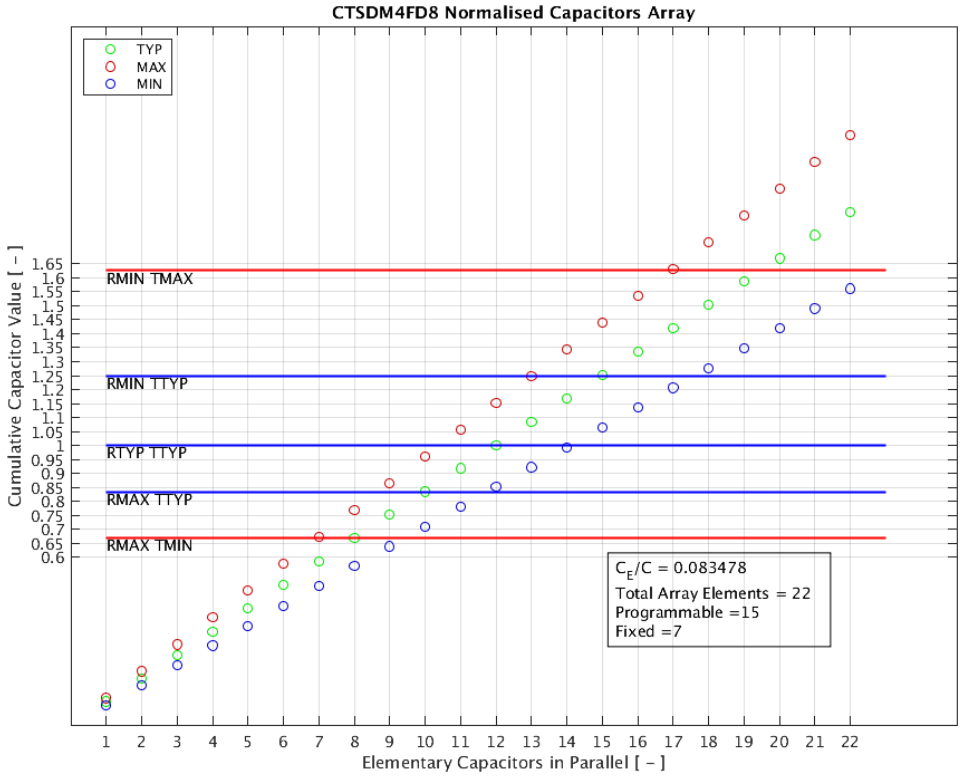

Figure 6.11: RC-Product trim concept. Blue lines mark the necessary capacitance value to compensate typical and spread RC-Product due to process variation, while the red lines take into account the combination of the latter with temperature drift. Circles represent the capacitance obtained (expressed as ratio with nominal) in function of the number of switched-on capacitors for the three capacitance corners.

T=+125°C and $1 - C_S$. In all-typical simulations, it can be noticed that 12 switched on elements are necessary, that is, 5 switchable elements should be on, individuating the standard trimcode of 1010. Since this is a prototype, the four bits trimcode bus will be available to be manually programmed externally.

An important remark has to be made about trimming to conclude this Section. The choice of nominal values of R and C are chosen taking into account the possible variation in temperature of thermal noise performance. It has been already seen in Sec. 6.5.1 and thus in Tab. 6.4. that this aspect has been verified. This and the he fact that there are no thermal noise measurements expected in this work, absolutely did not make us decide to accept a more relaxed trimming in order to obtain better performance. The objective of this industrial thesis is a feasibility study, therefore to design a circuit the most similar to a product possible. This of course meant to accept to increase current consumption, in order to be able to drive the largest capacitors. This stretch in OPA performance has been taken into account in the worst case study (also carried out during the internship) and all the four OPA have been designed to be able to withstand their own current calls while the whole capacitor array is switched on.

6.7 Switches Timing

For each feedback and FIR tap paths, a single-bit DAC is present. They are all implemented by a simple switch as the one shown in Fig. 6.12, for a total of 22 devices (11 per differential side, of which 8 for FIR-DAC, the remaining 3 for stages following the first).

It is of absolute importance for this device to avoid having both VREFP/M switches open at the same time, otherwise a short-circuit between the two references would take place. In

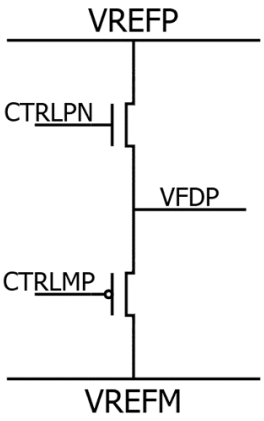

Figure 6.12: The elementary switch between VREFP/M. Each feedback path and FIR-DAC single-tap path does have one, for a total of 22 in the design. The selection of reference voltage to be transmitted to VFDP node is determined by the state of CTRLPN and CTRLMP.

fact, in many scenarios, other than this case, it may be desired to produce non-overlapping phases for a clock signal, in order to perform actions on devices with a fixed delay between each. For this purpose, non-overlapping phase generator circuits are available and at the base of the knowledge of an analog designer: this circuit will not be explained in details, what is important for this design is that distributing these non-overlapping phases to the appropriate switches will ensure that couples driving VREFP/M on the same VFDP node can never be "on" at the same time.

As long as FIR-DAC and classic feedback DAC circuits were behavioral, sharp clock signals were given and perfectly timed switch operations were performed, but a really important problem arose when non-overlapping phases, real switches and Flip-Flop based FIR filter have been implemented.

This is because the first implementation has been performed by simply substituting the models with their electrical circuit counterpart, just mentioned. The circuit looked like the one in Fig. 6.13. Equalizing techniques had been used to prevent different delays, for

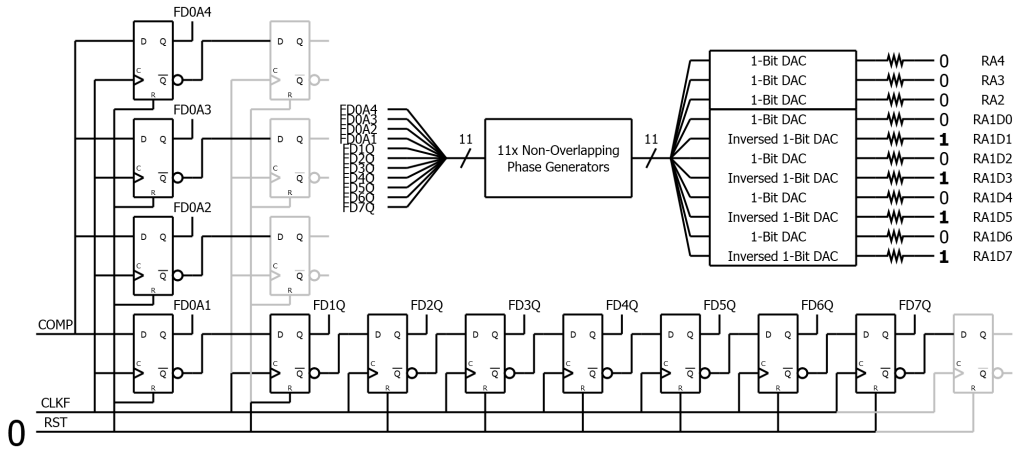

Figure 6.13: The behavioral model of the FIR-DAC has been implemented for the first time simply substituting each block with its electrical implementation.

example, adding dummies (appearing in light grey in Fig. 6.13) or using $\overline{Q}$ to feed the following FFD and Q to feed the DAC switch signal chain, inverting the logic signal for DACs in odd positions, as an alternative way to implement analog VCM reset.

Though in doing so there are no problem for integrators following the first, the presence of a FIR-DAC in the first stage means having different switching instants for the 8 DACs

due to the following asymmetries:

- high-to-low and low-to-high transitions in different FIR-DAC taps: they all sum up in the integrator input node but there exist a delay in crossing VCM due to eventually different ports charging different gates (notice it is a different consequence with respect of ISI).

- the "reset" feature (see Ch. 4, Sec. 4.7.1) of the 8-taps FIR-DAC which was cabled in order to have 01010101 as samples at startup: D-Flip-Flop are cabled alternating Q and QN as outputs, the rising/falling time are therefore different

These factors all together resulted as a jitter-like behavior (Fig. 6.14) with a very *unfortunate* distribution for a sigma-delta, which therefore degraded performances at an intolerable level.

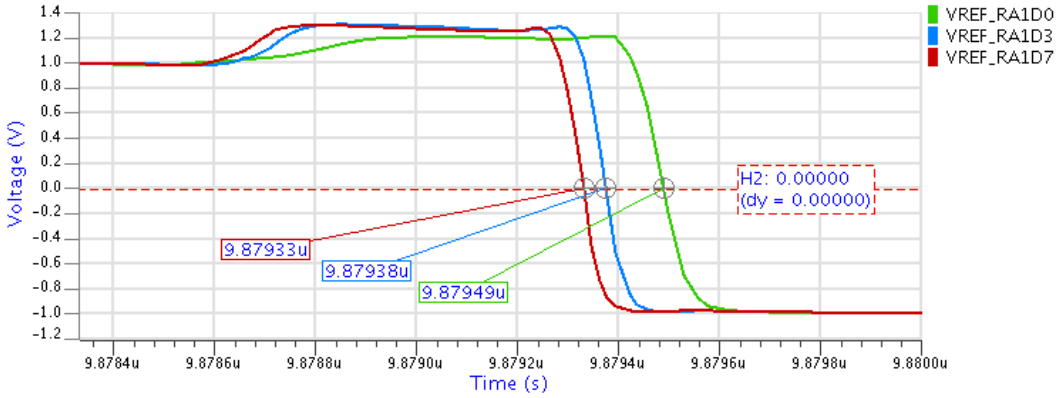

Figure 6.14: Transition example where tap 0, 3 and 7 should make the same transition, but they do not. Due to asymmetries, the blue and green curves switch with a delay of 44.49ps and 114.50ps respectively with respect of the red one. Current information flowing from FIR-DAC to first stage integrator suffers the same effect as jitter.

The solution has been found in developing a locking-logic block as in Fig. 6.15, which allowed to re-sample with a certain delay, re-aligning all the asymmetries and keeping the analog-VCM reset feature. The block contains just a D-Flip-Flop and 3 ports. a total of 22 blocks of this kind must be introduced.

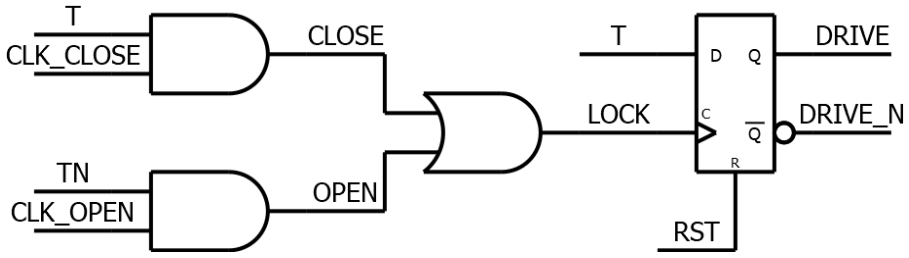

Figure 6.15: Sample Lock Logic Block. FIR-DAC sample is given on T and TN. the transition of DRIVE and DRIVE_N which are connected to switches gates, however, is managed by CLK_CLOSE and CLK_OPEN signals which re-align the sampling instant.

Performances have been restored successfully this way, however, a loss of 3dB over all the DR was experienced in jitter simulations. This took jitter to be an important contribution to the overall degradation, being at about the same level than Thermal noise, with a consequent loss of 3dB over the entire DR.

6.8 Modulator Final Values and Simulated Performance

The modulator is now in its final form. The dynamic range is presented in Fig. 6.16, where a performance simulation at the checkpoint before introducing analog FIR-DAC (before experiencing the 3dB loss) is also shown. This checkpoint is representative of the last modulator setup where overall performance fitted with what is expected from calculations.

The extrapolated DR values for simulations with jitter and thermal noise are $103.67\text{dB}_{\text{Aw}}$ before and $100.28\text{dB}_{\text{Aw}}$ after introducing the analog FIR-DAC. The DR of 100dB is therefore achieved as it was requested, but our design targeted to have a margin of at least 3dB on this parameter, exactly those lost after analog FIR-DAC implementation.

Power consumption has been fairly reduced with respect of CENTO: details on current budget are given in Tab. 6.4, where all sums up to a $1005.75\mu W$, reference power draw included.

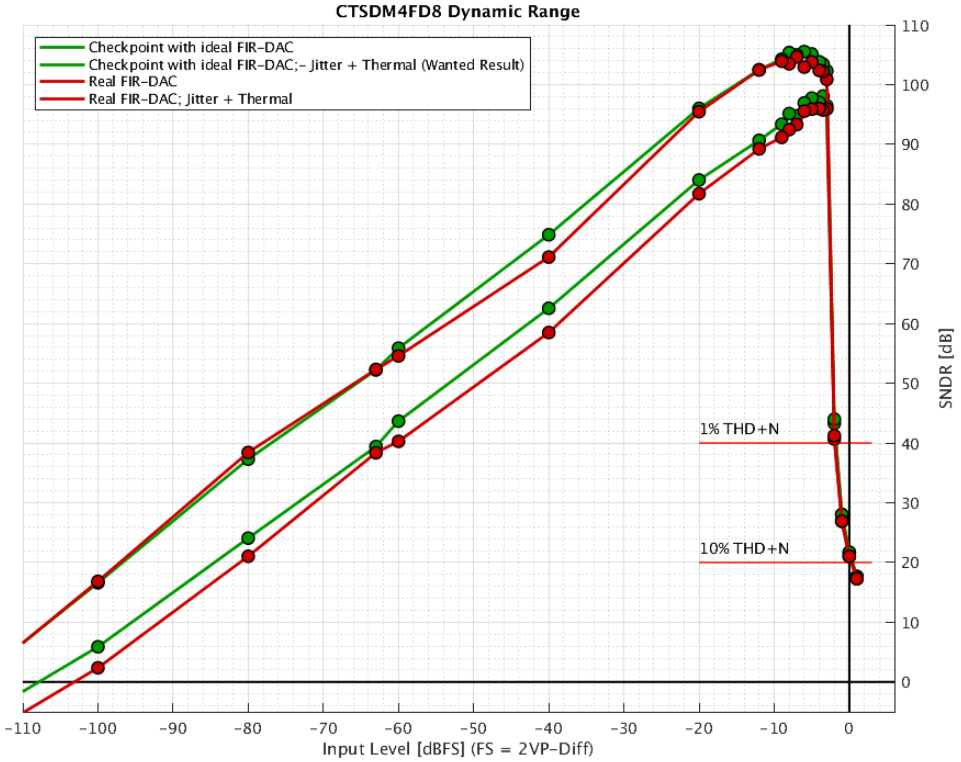

Figure 6.16: Modulator Performance without (top curves) and with jitter and thermal noise (bottom curves). Red curves show the actual situation, while green ones represent the last checkpoint inline with calculations.

6.9 Layout

Layout is the part of the design when all devices symbols used for simulations in the CAD environment are converted into information for material deposition during fabrication. That is to say, that each device geometries are *drawn* on another kind of view in actually the same CAD tool, representing the nominal physical characteristics of what is being fabricated. Layout of CTSDM4FD8 is shown in Fig. 6.17: the modulator size is $740\mu m\ x\ 450\mu m$ which makes a surface of $0.35mm^2$. Most of it is dedicated to first stage trimmed MIM capacitors being $72pF$ nominal each, which makes $132pF$ to guarantee the greatest trim value needed. Such a big capacitor is due to the low input resistance value of $24k\Omega$, necessary to contain thermal noise limit.

An horizontal axe of symmetry can be noticed, every stage and the comparator obey to

Q.ty [-]	Description [-]	Current Drawn [uA]	Total [uA]
	MODULATOR		
1x	Stage 1 OPA	100.00	100.00
1x	Stage 2 OPA	48.00	48.00
1x	Stage 3 OPA	38.00	38.00
1x	Stage 4 OPA	38.00	38.00
1x	Comparator	32.00	32.00
	REFERENCE		
2x	8x FIR-DAC Resistances	5.00	80.00
2x	A2 Coeff Res	2.27	4.54
2x	A3 Coeff Res	4.31	8.62
2x	A4 Coeff Res	3.82	7.64
	BIAS		
1x	Bias Circuit (OPAs)	25.00	25.00
1x	Bias Circuit (COMP)	8.00	8.00
2x	VCM Partition	6.25	12.50
		TOTAL	**402.3**

Table 6.4: Detailed power consumption of the Modulator and Reference. For reference buffer, only current drawn from supply by feedback resistors is taken into account. Drawn from a supply of 2.5V, the power consumption is 1005.75μW in total.

this rule. There is no need of symmetry neither in the circuit providing a delay between the comparator sampling and decision-lock instant, nor in the FIR-DAC, since their inputs and outputs are single-ended logic signals.

All capacitors are MIM, that means that they can be stacked over the active region, since they are all-metallic and created over metals M2, M3 and M4. In addition, all integrator feedback capacitors are shielded with M1: a metal plate of dimensions slightly greater than the shape of the capacitor is put just under the device, protecting it from parasitic couplings with devices below. The cost of this advantage is a parasitic capacitance of about 10%, however, the designer is aware of the presence of a +10% capacitance with respect to nominal value and can act consequently.

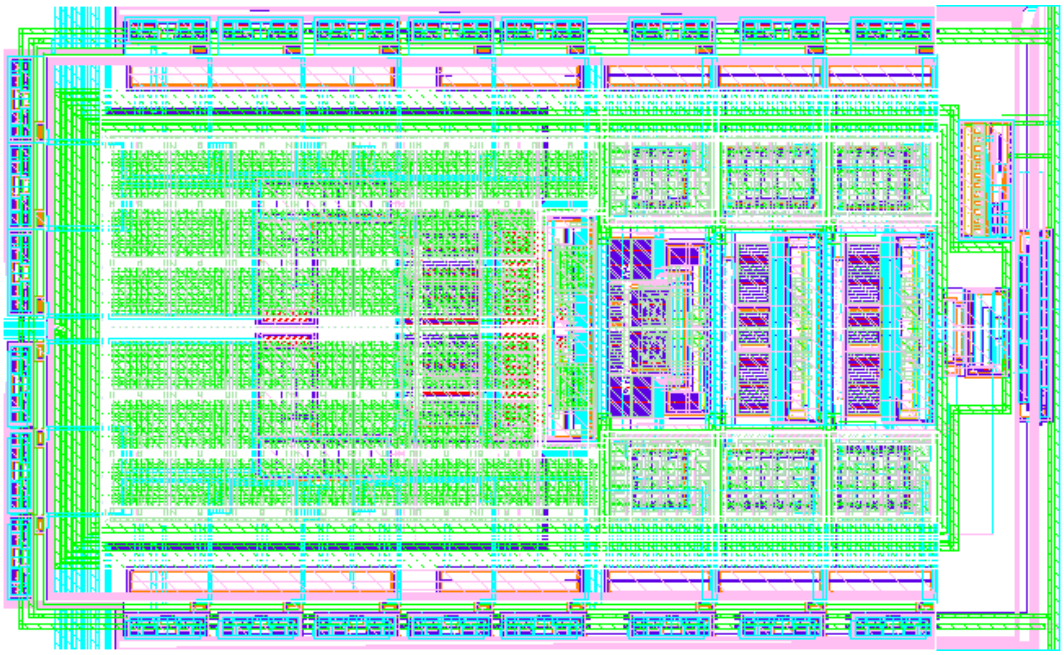

Figure 6.17: Modulator Layout. A big surface budget is dedicated to the two trimmable capacitors in the first stage, having $72pF$ as nominal value. The switches and their own dedicated re-sampling logic are situated on the outer ring forming an U shape.

Stacking of the capacitors over devices built on the substrate (transistors, HIPO resistors...) has not been completely exploited, instead, a space is exclusively dedicated for each stage. Space is in fact limited horizontally, while the whole height is used. This choice is based on layout simplicity, perfect surface efficiency is sacrificed in favor of a simpler routing, which also helps to limit parasitic capacitance and couplings on signal paths, which can be as short as possible.

In order to avoid degradation due to switches timing (just seen in Sec. 6.7) all the 8 paths connecting the FIR-DAC taps and their respective resistor are layouted to have the same length, eventually adding *serpentine* sections. Also in this case, the length of these wires itself is the the shortest possible, in order to reduce parasitic effects. By consequence, the 22 blocks containing the DAC switches and their own resample lock-logic are placed all around the whole four-stage central structure just described.

Once the layout was completed, the following step of simulation could be performed: Post-Layout Simulations are explained in the next section.

6.10 Back-End and Post-Layout Simulations

The Back-End phase is the last step of validation, during which Post-Layout Simulations (PLS) are performed and potentially several modification-simulation routines may be necessary.

Post-Layout Simulations are electrical simulations which use an extracted circuit based on the layout view. Instead of using device models as placed and sized in the design phase, geometrical and spatial information is considered and several devices are automatically generated, representing each real transistor, capacitance and resistance existing between nodes. During extraction, a cutoff parameter allows to generate a device under the a value condition: since the number of devices generated is generally very high, there is no need, for example, to simulate capacitors in the order of the atto-farad. Not including all negligible[6] information allows faster simulations.

To back up this Section, an example of investigation based on a PLS simulation is presented. The simulation concerned produced the spectrum shown in Fig. 6.18, where the red curve revealed a great performance loss once parasitic capacitance were extracted. Notice that every parasitic capacitance is extracted considering the worst case CC_MAX, regardless of the capacitors and resistors nominal values.

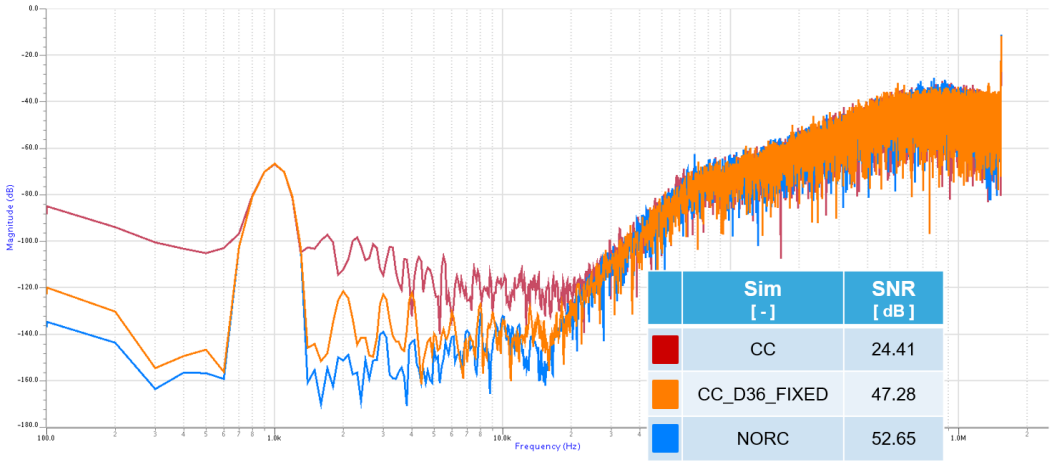

Figure 6.18: PLS simulation extracting parasites (CC, in red) reveals an unacceptable degradation. A fix (orange curve) has been necessary and was purely geometrical, layout oriented. A PLS extracted without parasitics is also shown for comparison (blue curve).

[6] The designer should be sure of the cutoff value is appropriate and not to underestimate parasitic.

After investigation on these parasitic, the issue was found in the FIR-DAC signal transmission from D-Flip-Flops to the resampling lock-logic blocks. These long parallel wires result in having a lot of parasitic capacitance and the consequence is a time constant so long that each DAC information cannot update on time.

The solution was found by dedicating more space between the wires and using alternatively metals M1 and M3, as it can be seen in Fig. 6.19. After adjustments following this path, the SQNR performance was restored, as in Fig. 6.18. Notice that the strategy is to *limit* the delay effect, of course, the blue curve representing the extraction without any parasitic, cannot be obtained as once parasitic capacitance are accounted for.

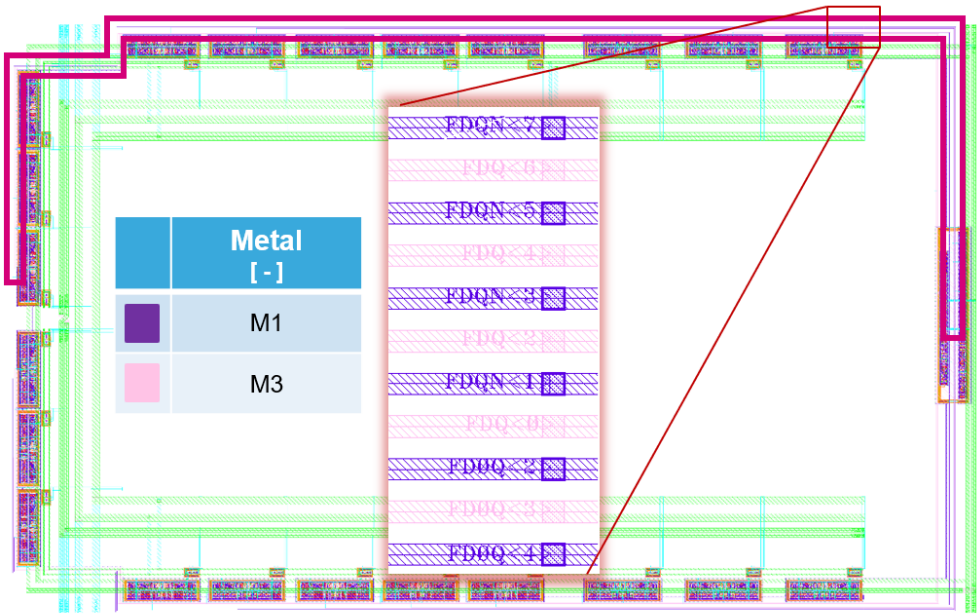

Figure 6.19: Solution to long delays on transmission lines between FIR-DAC D-Flip-Flops and resampling lock-logic blocks. Wires distance was increased and metals M1 and M3 were used alternatively to maximise the 3-Dimensional distance.

At this point, an important remark can be made: the choice of 8 taps instead of 16, that was already discussed in Ch. 3 and 4 and the general strategy of keeping the number of taps as low as possible is here even more justified. Not only the outer region in the layout would double in width, but it would not be that easy to fit the whole 8 additional lock-logic and DACs blocks for the first stage. From Fig. 6.17 it is easy to recognise the 8 blocks. The difficulty of fitting another 8 as well as it is evident from that figure.

Another interesting remark can be done about surface and noise budget aspects linked together. First, consider that the simulations presented in this section are not taking into account thermal nor jitter noise. Notice especially that thermal noise was designed to be dominant, so the NORC simulation (nominal, no parasitics) is in agreement with this guideline, since the quantization noise level in-band is -112.62dBAw. Needless to say, this noise level falling to -84.41dBAw of the CC (MAX) case was absolutely not acceptable. The outer ring fixes has been made keeping the size of the die constant and after having improved wire routing increasing their mutual distance, the noise level improved to -107.28dBAw, compatible with jitter, but overall not impacting for a great amount the thermal noise level. With more surface budget, this impact could even be lower, but in this frame, the fact that it is sufficient not to impact the total budget is enough for design purposes.

6.11 Conclusion and Prototype Fabrication

Once all the performances are verified and eventually restored if necessary, this step concludes the design phase and CTSDM4FD8 is ready to be fabricated.

Among all, this core step in design proved that all the safety margin discussed all along the thesis become useful when implementing the system electrically. Non idealities introduced by real devices impact performance. For example, the complete transistor-level simulation shown in Sec. 6.8 with thermal noise reached a Dynamic Range of 100.28dBAw, while when the FIR-DAC block was still a behavioral model, this value was 103.67dB$_{\text{Aw}}$. It was a good practice to design the latter to be inline with a 3dB safety margin for implementation, which has been lost afterwards. A similar effect happened due to parasitic capacitance on the FIR-DAC taps delay, seen in Sec. 6.10, where the DR considering only quantization noise is 112.65dB$_{\text{Aw}}$ while once considering parasitics, it falls to 107.28dB$_{\text{Aw}}$. Once again, the 10-15dB of safety margin commented in Ch. 2 proved to be a good practice, otherwise, the risk would have been to see the noise budget disrupted, losing the dominance of thermal noise.

A more general comment can be made about the fact, that there exist a great number of sources of degradation and some of them can be very difficult to anticipate. For example, among all those reported in this chapter, possible performance degradation while synthesizing modulator coefficients (Sec. 6.2) and technology spread impact on RC-Product (Sec. 6.6) were forecast and anticipated with dedicated design techniques. Once validation simulation were performed, these two aspect were perfectly mastered and no further major actions were needed about them. Instead, the input resistance flicker noise issue (Sec. 6.5.2), the switches timing (Sec. 6.7) and the parasitic capacitance on FIR-DAC taps (Sec. 6.10) were unexpected and have been studied and fixed after being discovered. In this case, a time budget had to be assigned to these issues to resolve. The task of a designer is then to anticipate issues as much as possible, thanks to knowledge gained by his own experience and by constant and active sharing with other designers.

There exist, however, some more backups a designer can use as a last safety procedure before fabricating a testchip. Some devices can be designed as to be partly excluded, for instance, if there is a concern about a capacitance value, the device can be cut in more parts, summing to the desired value, with wires at least partly using M4 metal: a process called FIB allow to create or cut M4 wires locally, excluding or adding capacitance. Another procedure can be adding *spare* components, such as inverters or flip-flops: during fabrication, for a fraction of samples, the process is interrupted before adding metals. This allows to get back to the layout phase and *redraw* all metal connections. The spare components can be connected and used if necessary. This procedure is called Metalfix. Both these procedures represent a cost in any case, so, the devices are prepared to perform them just in case, as another safety level, but with the intention of using them only if necessary.

Fabrication initiated in august 2020 and ended in January 2021. After packaging, the circuit was received in February 2021, ready for testing. All details about testing will be carried out in the next and last chapter.

Chapter 7

Results and Conclusion

This chapter concludes the coverage of CTSDM4FD8 project, research and development. Here, the final step of this work is presented and commented: it consists of the prototype performance and its placement with respect to the state of the art.

The only other content preliminary to this performance display is the testbench used for measurements. The testing board, instrumentation and environment will first be described, in order to contextualize how the results are produced.

Then, a summary of what have been done and what can be improved or explored, will conclude this thesis.

7.1 Testbench

The Testchip fabricated for CTSDM4FD8 has been designed to be pin-to-pin compatible with CENTO. Not only this allowed to use former CENTO testboards with perfect compatibility, but it also helped to implement an interesting check system: there exist VREFP/M input/output pins which allow to verify the actual level of these nodes and, eventually, force these value from external sources.

A photo of the board fitted with voltage and current references, signals for programming via I2C,input differential signal and output probe of the audio analyzer is shown in Fig. 7.1, while a photo of the entire bench with all the equipment (listed in Appendix D) used is shown instead in Fig.7.2.

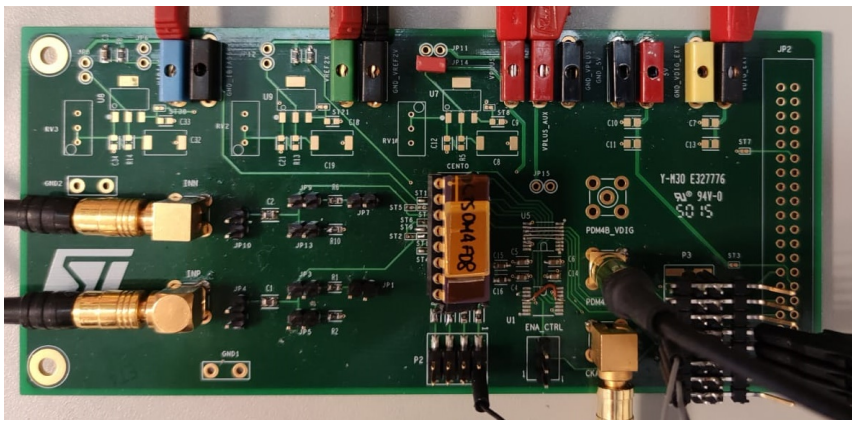

Figure 7.1: CTSDM4FD8 Test Board.

Programming of the testchip registers is performed via a Labview[1] interfaced I2C communication protocol, shown in Fig. 7.3 (top). Registers and their meaning are included in the figure.

[1] Ni.com - Labview 2016 version 16.0f2

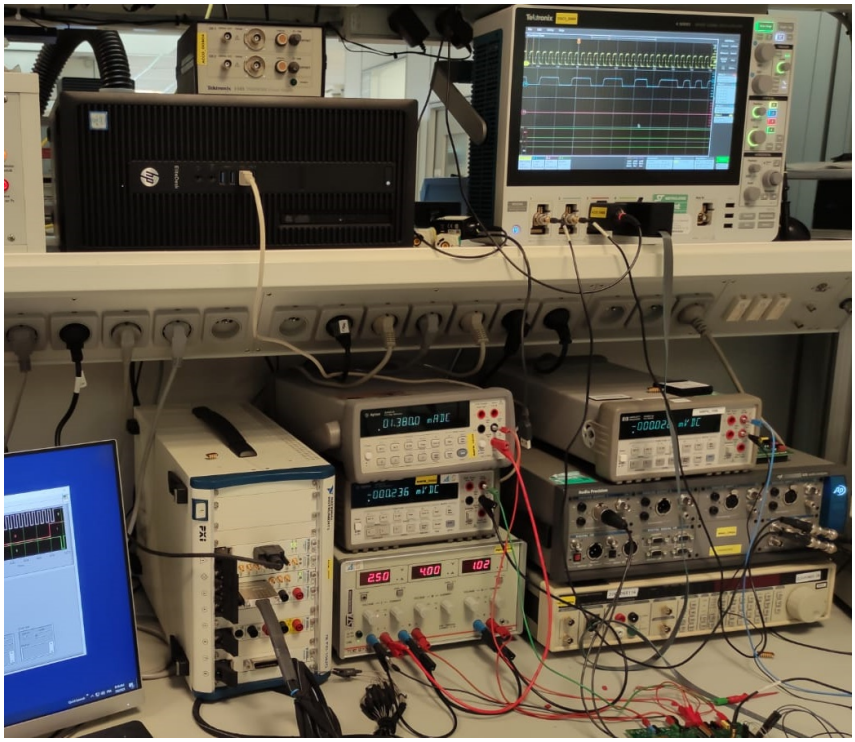

Figure 7.2: CTSDM4FD8 Testing Environment

Finally, measurements are managed by Audio Precision APx500 series dedicated interface[2] shown in Fig. 7.3 and for which all the settings are explained in the following Sec. 7.2.

7.2 Measurements

The Audio Precision APx500 series dedicated interface software is a support created by Audio Precision to interface their own APx500 series audio analyzers. It features several audio-oriented functions and settings, which in our case have been set up in order to obtain the following scenario. A differential sinusoidal signal is provided and FFT on the PDM output is performed. Output power is reported in dBFS where the Full-Scale has been of course set up to 2Vpeak, Differential (1.414VRMS, Differential) that is, 1Vpeak Single-Ended ("channel", 0.707VRMS Single-Ended). The FFT is performed on the decimated[3] output PDM. The band available to be selected by the Audio Precision APx500 instrument is 24kHz, there exist no option for 20kHz so calculations on this band will be carried on in a custom manner after data extraction (see further in this paragraph). Since the sampling frequency for this band is 48kHz, the decimation factor is 64x. The FFTs are therefore calculated on 480 points.

During measurements, some very important signs of degradation and malfunction have been encountered and could neither be resolved, nor could a cause be attributed with the time that was available.

First of all, the current bias of 1μA to be provided, determines a 10% loss on VREF swing. The current bias to be provided must be as high as 1.30μA in order to have the 2V VREF swing as designed. This setting is the one which is actually used all along the measurements, and this is the only parameter in the bench that is not inline with the design[4]. Notice that

[2]Software by Audio Precision Inc. V4.1.1.54.94537

[3]Decimation is synthesized inside Audio Precision APx500 instrument.

[4]For example, both trimming of RC-Product and First Amplifier Offset have been tested and found to be coherent with design.

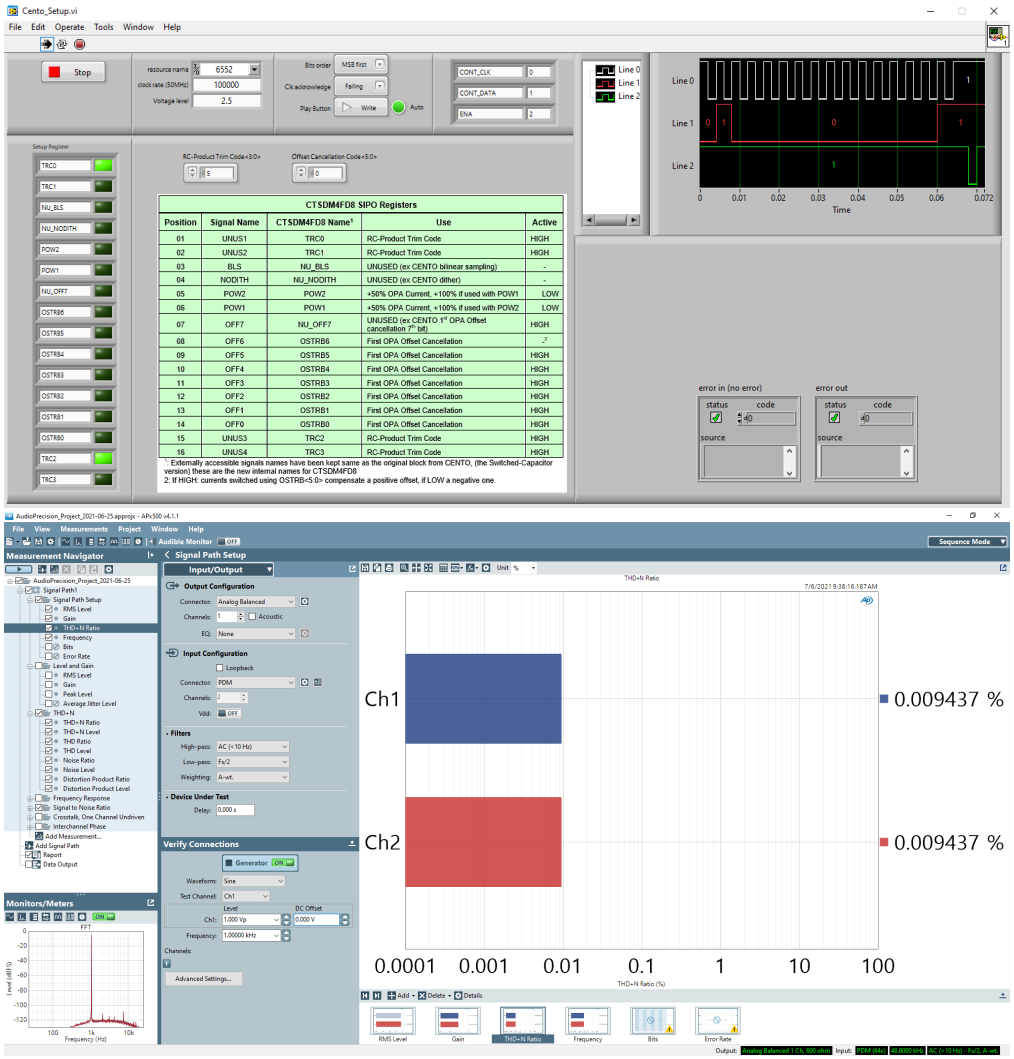

Figure 7.3: CTSDM4FD8 user interfaces for measurement: register setup interface using Labview (top) and measurement interface using Audio Precision dedicated software (bottom).

the IBIAS parameter regulates the current budgets present in all branches regarding both the reference block and the four amplifiers.

About performance, two kind of feedbacks were combined for analysis. The first is the signal processing analysis: for example, observing spectra calculated on the decimated output PDM and controlling input/output levels and waveforms in chronographs. The second was auditory: the input sinusoidal tone as well as some music have been *listened* with headphones through CTSDM4FD8.

In both cases, a great loss of performance could be noticed to occur randomly in time. This can be clearly heard in auditory analysis when the input power level is low. Specifically, there are pops and clicks (see transient example in Fig. 7.4) that become more frequent and audible the lower the power level is, while also noise can clearly be heard to raise in power irregularly in time.

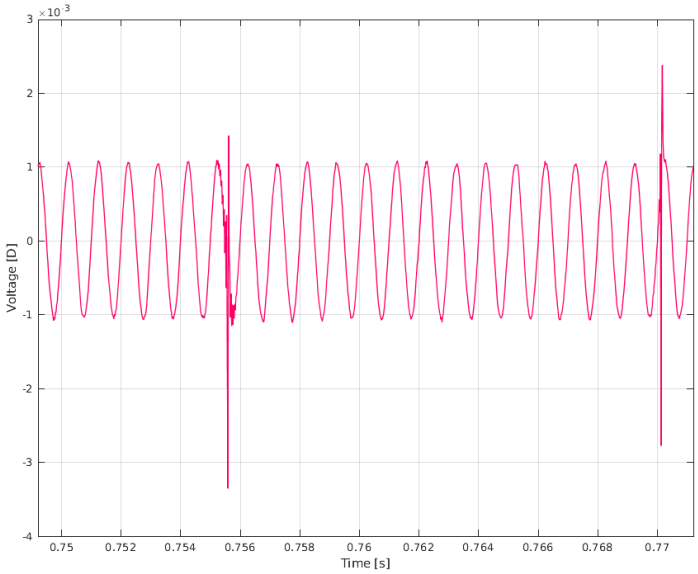

Figure 7.4: Extract of the decimated output of CTSDM4FD8 (filtered) showing abrupt behavior of the modulator. After investigation, there seem not to exist a regular pattern in this source of degradation. Calculations shown about these measurements, like FFT, are made on windows that are selected such as abrupt signals, as well as periods with higher noise power, are not included.

A New Measurement Strategy

Further insight on the origin of these two problems will be carried on in the future, but for a matter of time, results will not be included in this thesis. Instead, in order to show meaningful results with the material at our disposal at the moment, after having documented the two defective behaviors, calculations have been carried out as follows.

A 240000 points measurement of the decimated output of CTSDM4FD8 is performed.

This corresponds to 500 windows of 10 periods of the input signal sinus or 5 seconds of measurement. This time interval is sufficient to capture several transitions between "high" and "low" noise, based on hearing experience and realtime[5] spectra visualization. Data retrieved this way is then processed with a script, which finds an optimal 10-periods window from the performance point of view. Clearly, this window does not include pops and clicks either. The results of doing this are the following.

In Fig. 7.5, two representative spectra having input signal power at -60dBFS and -3dBFS, are shown. Their SNDR is respectively 32.93dBAw and 85.31dBFS, versus the reference simulation (see also Ch. 6, Sec. 6.8 and following) showing 43.67dBAw and 96.44dBAw respectively. The dynamic range is then 92.93dBAw versus 103.67dBAw (100.28dBAw for the complete simulation).

The full Dynamic Range plot is also provided, obtained by a set of aforementioned measurements performed at different input levels: it is shown in Fig. 7.6. It can be seen that the downshift due to degradation is coherent all along the DR.

[5]By realtime, it is meant that the setup combination of number of points and averages are such as having the spectrum updated often enough to distinguish the "high" and "low" noise regions: two very different shapes can be visualized alternatively.

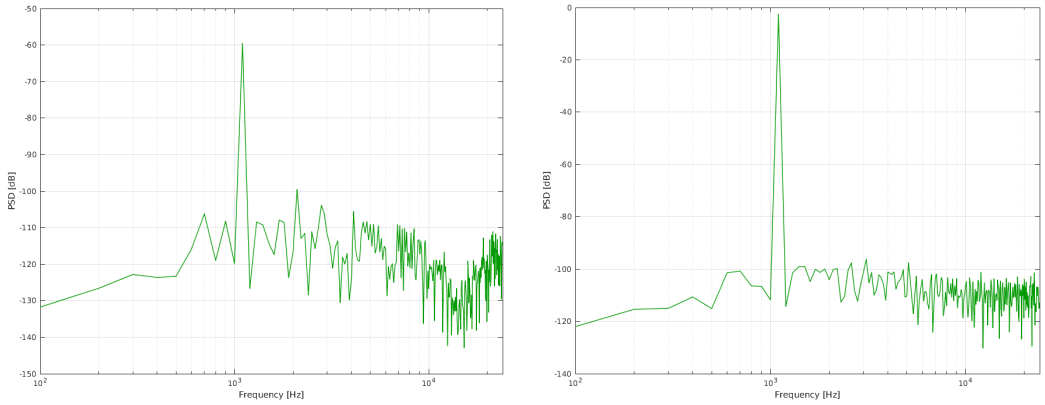

Figure 7.5: CTSDM4FD8 measured A-Weighted spectra for -60dBFS (left) and -3dBFS (right) input power level. The sudden transition between "high" and "low" thermal noise forced the measurement to be on very short windows. Keeping a 100Hz spectral resolution like in simulations was found to be a good compromise between visualization and possibility of finding an optimal window in a dataset.

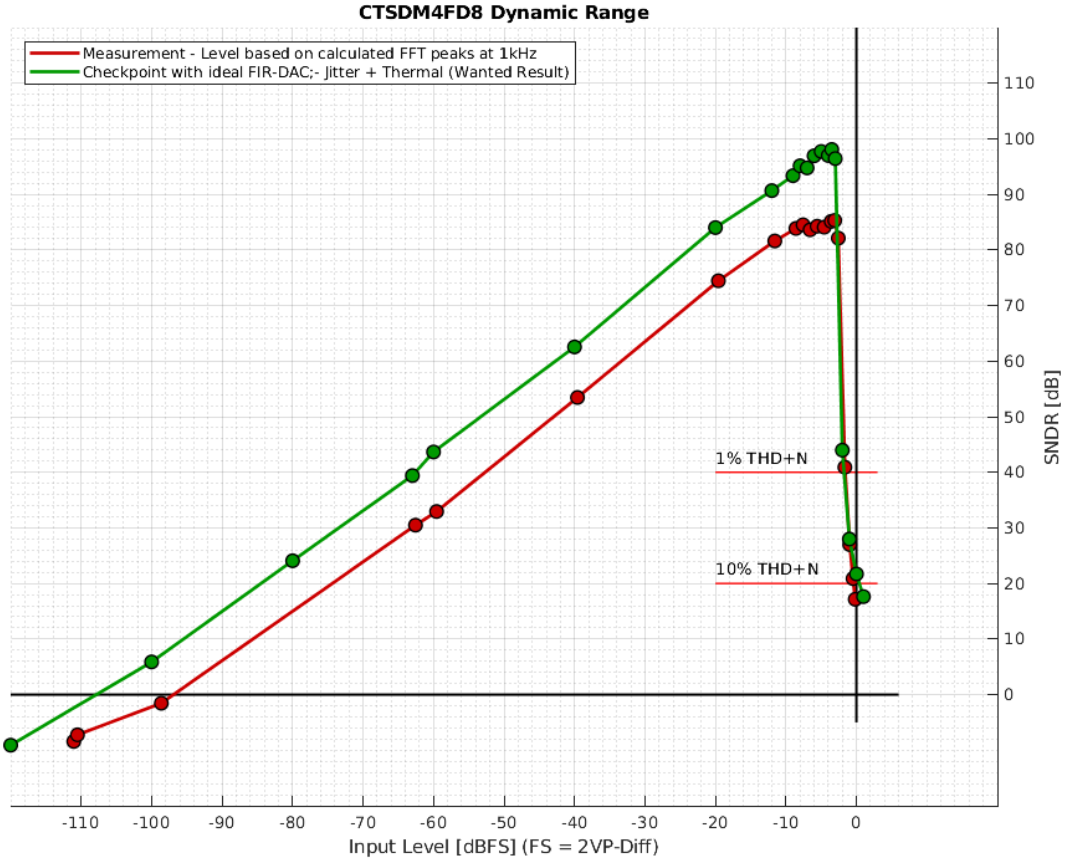

Figure 7.6: CTSDM4FD8 Dynamic Range with all standard configuration except for IB-IAS = 1μA. Results are coherent, but 7dB lower than the objective.

Measurement Parameters and Performance

The modulator testchip is equipped with VREFP and VREFM I/O pins and the reason of their presence is twofold. The first reason is that the reference voltage can be monitored: this helped to verify that, as for a previous remark, in standard biasing, VREF was not

correctly polarized. The second is that, thanks to the design of CTSDM4FD8 reference block, the reference voltages VREFP/M can be both provided internally or imposed from the external. While the two external voltage values are imposed, the internal is bypassed whether or not the block is enabled.

This feature was fundamental to eliminate the correlation between IBIAS and VREF: any value of IBIAS could be tested without preventing VREF to be correctly polarized. To resume the situation: there are now 4 parameters that can be used to explore the encountered issues, that are VPLUS, VREF, IBIAS and the Trimcode. Audio and graphical verification was then made for different scenarios and an interesting result was found for VPLUS = 4V, VREF = 2V, IBIAS = 1μA and 0101 (standard) Trimcode, these are shown in Fig. 7.7.

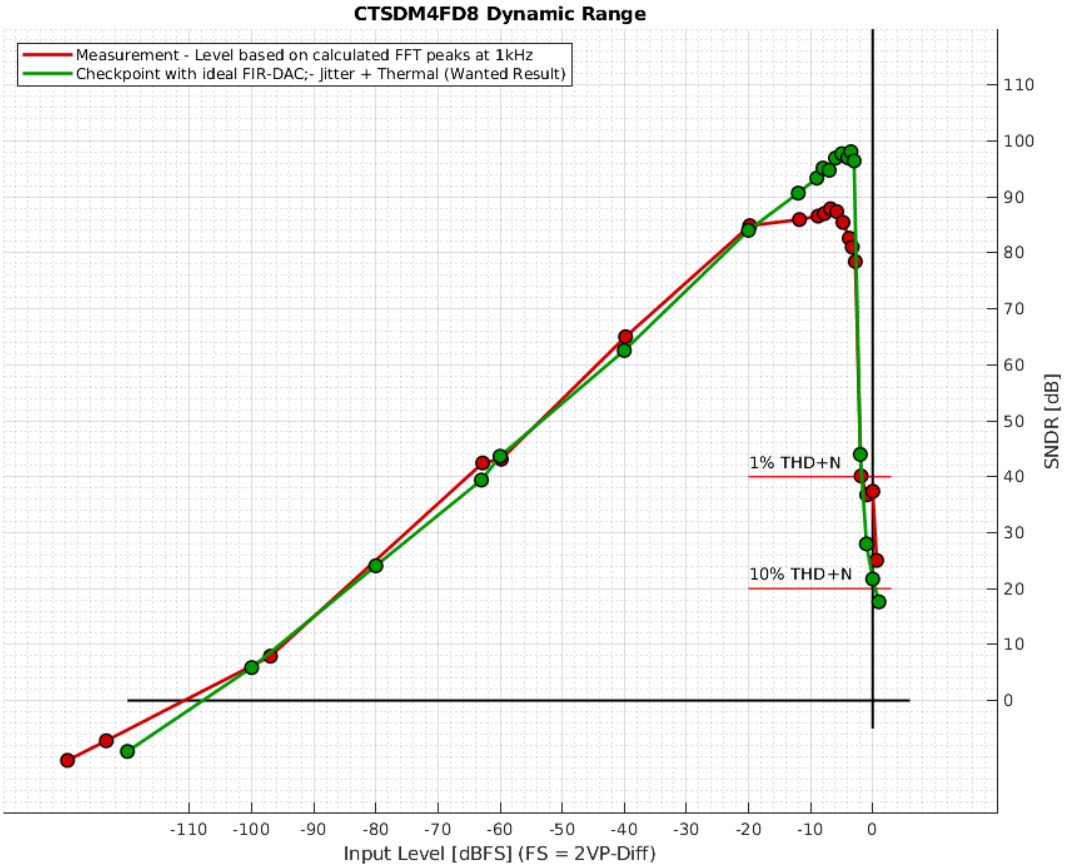

Figure 7.7: CTSDM4FD8 Dynamic Range with VPLUS = 4V, VREF = 2V, IBIAS = 1μA and 0101 (standard) Trimcode.

In this scenario, the SNDR=43.46 at -60dBFS, which means that a DR=103.46dB is found, inline with audio specifications, but, in addition to the clearly visible distortion at high input level, the occasional loss of performance under the form of increased noise and abrupt behavior are still an issue. The interesting fact about the latter two aspects is, that they could be found to be occurring less often in this configuration. In particular, reporting a trend from different scenarios that are not here mentioned specifically, increased noise happens to become less frequent with higher VPLUS and lower IBIAS, while abrupt behavior occurs less often with higher VPLUS and higher IBIAS. Notice that the higher VPLUS is an overall benefit while IBIAS reveals a trade off between the two.

As stated earlier, further inspection will be carried on on this circuit, but unfortunately, these are all the results that could have been obtained during the time dedicated to this thesis. The two major issues have to be resolved and may be related to delays caused by parasitic capacitance that was not mastered. For example, a critical point during PLS simulations were the signals delay during the comparator choice lock and all transmission

to Switches through FIR and the re-sampling logic blocks. For this reason, two of the ten 3ns *delays* in chain were designed in layout as to be easily metal-fixed if needed: the delay between comparator sampling and decision lock can become 3ns or 6ns shorter. The next steps are therefore to verify if the metal-fix is necessary and eventually perform it in order to compensate eventual unexpected parasitic capacitance on critical nodes, then, to repeat all the measurements.

7.3 Comparison with the State of the Art

To present the performances of our CTSDM, all the modulators that were proposed in the State of the Art (Ch. 2, Sec. 2.6), are now shown again in this concluding chapter for comparison. These candidates are modulators that were designed for audio application, having a DR superior to $100dB$ and being similar in performance to our target. CENTO, the switched capacitor starting point for this project, has been also included in order to show the improvement in power consumption. The candidates and their description can be found in Tab. 7.1.

The Figure of Merit (FOM) used in this comparison is again the one known as Schreier FOM and is calculated basing on the DR as follows:

$$FOM_S = DR + 10log_{10}\left(\frac{f_S}{2 \cdot OSR \cdot P}\right) = DR + 10log_{10}\left(\frac{BW}{P}\right) \tag{7.1}$$

Since, as it was seen in Sec. 7.2, measurements on the testchip are still not reflecting the correct operation of CTSDM4FD8, the following comments are made considering the results obtained in simulations.

The DR value, in the case of our CTSDM, has been extrapolated as the SNR at -60dBFS (that is 2mVPeak, Differential) adding 60dB, as it was explained in Ch 2, Sec. 2.3.2. Also the results obtained with the VPLUS = 4V configuration discussed in Sec. 7.2 are shown and for the "Simulation" case, data is about results from simulating CTSDM4FD8 with both jitter and thermal noise (the DR at the last checkpoint before PLS simulations[6]).

This modulator is of course not among the best, but it is still in the range of the state of the art. Furthermore, it should also be considered that there is no trace in literature of anyone having an intrinsic stability method implemented with high order modulators (see upcoming section). This feature, as it has been discussed in Ch. 4, Sec. 4.4, costs in term of power consumption, making it one of the reasons why this modulator has a lower FOM with respect to others. For stability purposes (see following section), the architecture has been chosen to be a Cascade of Integrators-Feedback (CIFB). The coefficients in this architecture are quite strong, instead of those in feed-forward architectures (CIFF), which are weak. Such an architecture may work even with a single feedback path towards the first stage, its coefficient being worth just around 0.1. This means lesser swing is necessary on "state nodes" overall and a relaxed current to be drawn on from amplifiers and reference, showing a remarkable power consumption advantage with respect of our architecture.

We also chose to clock at 3.072MHz, whereas many works clock at about double the frequency. In the FOM, decimation filter coming after any sigma delta modulator is not taken into account with its power consumption, neither is the clock tree in its entirety. This work, from a wider point of view, is part of a road-map to evaluate the possible introduction of continuous time sigma delta audio ADC[7] in STMicroelectronics portfolio. The target is low power consumption so the remaining parts of the chain should be taken into account. We preferred to keep the sampling frequency of the circuit lower: the targeted $100dB$ of DR is attained and the decimator filter and the clock tree will be less power consuming. This is also the reason why a fourth stage is needed, instead of the most widely spread three-stage architectures: the SNR is recovered this way from the fact of having a single bit and a lower

[6] It is worth to remind that since thermal noise simulations were not possible to be performed with post layout, the latter has been verified with respect to performance against quantization noise of the checkpoint previous to PLS.

[7] Or more in general low bandwidth applications continuous time sigma delta ADC.

Ref.	Tech Node [nm]	Supply [V]	SNDR [dB]	DR [dB]	BW [kHz]	Power [uW]	FOM (S) [dB]
[14]	350	5	105	114	20	68000	168.69
[15]	350	3.3	106	106	20	18000	166.45
[16]	180	0.7	95	100	25	870	174.58
[17]	40	2.5	90	102	24	500	178.81
[18]	180	5	99.5	101.3	20	1100	173.9
[19]	65	1.2	94.1	98.2	24	68	183.6
[20]	28	1.5	96	103	24	3000	172
[21]	180	1.8	106.4	108.5	20	618	183.6
[22]	160	1.8	106.5	109.8	20	440	186.4
[23]	65	1.2	101	103.5	24	134	186
[24]	160	1.6	91.3	103.1	20	390	180.2
[13]	180	1.8	98.2	103	24	280	182.3
CENTO	180	2.4	101	101	20	3000	169.24
This Work	180	2.5		92.9	20	2700	164.55
VPLUS = 4V*	180	4		103.4	20	13240	168.20
Simulation**	180	2.5		100.3	20	1005	173.23

Ref.	Year	Notes
[14]	2003	DT Fifth Order Multibit 17 Levels
[15]	2005	Hybrid CT/SC
[16]	2009	DT Multibit 18 Levels Second Order Chopper Stabilized
[17]	2011	Hybrid CT/SC Second Order 17 Level (5 Level Int.) DAC
[18]	2012	DT Multibit 15 Levels Third Order Spectral Shaped
[19]	2018	CT 1.5-bit Negative-R Assisted
[20]	2020	CT 7-bit up/down FIR DAC Chopper Stabilized
[21]	2020	CT Zoom
[22]	2020	DT Zoom
[23]	2020	CT Chopped Negative-R Tri-Level FIR-DAC
[24]	2016	CT Multibit 17 Levels
[13]	2013	CT Single-Bit Third Order FIR-DAC 12 Taps
CENTO	2016	DT Single-Bit Fourth Order FIR-DAC 4-Taps
This Work	2021	CT Single-Bit Fourth Order FIR-DAC 8 Taps

Table 7.1: State of The Art for Sigma-Delta Audio Converters plus their Notes and Architectures. By SNDR, $SNDR_{MAX}$ is meant. FoM(S) is calculated wherever it was not explicitly written in the corresponding publication.
*: Measurement taken with VPLUS = 4V, VREF = 2V, IBIAS = 1.30μA and 0101 (standard) Trimcode.
**: CTSDM4FD8 performance found in a .NOISETRAN simulation, jitter included. The circuit simulation is the last checkpoint version before PLS, as in Ch. 6, Sec. 6.8.

OSR. This last stage is the more relaxed but still represent about the 10% of the power consumption budget.

All of these choices made us have a higher power consumption than some other works, the same applying on DR, which both impact the FOM. This work is oriented towards the concept of industrial mass production, realisation constraints and robustness to process variation, temperature and corners can easily become a limiting factor on pure performance.

Comparison with "Industrial" State of the Art

The candidates selected from the industrial products present on the market in Ch. 2, Sec. 2.3 are as well proposed again in Tab. 7.2. Once again, this comparison is separated from modulators which are the result of pure research because of the different objectives and framework.

As already commented in Ch. 2, Sec. 2.3, industrial modulators tend to have a lower FOM, which makes CTSDM4FD8 among the best while considering this parameter.

Ref.	Price* [$]	Supply [V]	SNDR [dB]	DR [dB]	BW [kHz]	Power/Channel [uW]	FOM (S) ** [dB]
[30]	6.65	5	-	101	24	90000/2	158.27
[31]	5.95	2	107.3	115	27.7	19700/1	176.48
[32]	0.987	5	99	99	24	8600/1	163.46
[33]	2.74	3.3	106	107	24	11300/2	173.28
CENTO	-	2.4	101	101	20	3000/1	169.24
This Work	-	2.5		92.9	20	2700/1	164.55
VPLUS = 4V	-	4		103.4	20	13240/1	168.20
Simulation	-	2.5		100.3	20	1005/1	173.23

Ref.	Year	Notes
[30]	2008	Cirrus Logic - SC 5th Order Multi-Bit
[31]	2019	Analog Devices - Mostly Sensor-Oriented and for audio testing
[32]	2011	Texas Instruments - Single-Ended, Automotive Qualified
[33]	2019	Texas Instruments (Burr-Brown) - Quad Ch. Analog/8-Ch. Digital
CENTO	2016	DT Single-Bit Fourth Order FIR-DAC 4-Taps
This Work	2021	CT Single-Bit Fourth Order FIR-DAC 8 Taps

Table 7.2: "Industrial" State of The Art for Sigma-Delta Audio Converters. While multiple setups are available for these products, in the table only one is reported. All values are TYPical.
*: for a placed order of 1kU on Mouser Electronics online store, data updated to Q1 2021.
**: FOM is not reported in industrial applications and datasheet, in this table it is calculated.

7.4 Conclusion and Perspectives

Under the point of view of the target of the project, it is sure that it has been achieved: we have implemented a modulator reaching $100dB$ of DR gaining almost a factor of three in power consumption with respect to the previous switched capacitor version which was candidate to the task.

The experience of an industrial thesis is complete and fulfilling. Every aspect of the analog designer job is present, with a complete flow from circuit demand to measurements on the fabricated silicon solution.

The whole project started on the desire of optimizing the power consumption of an audio ADC for highly portable devices. It has been proposed to explore the possibility of converting a DT version of a recent prototype of a modulator existing in ST Portfolio to CT. This strategy has been confirmed by literature, as power consumption can always potentially be lower in a CT version than a DT of the *same* modulator. Another great literature acknowledgement at this step was about the downsides and issues a CT version could have. Jitter noise and coefficient drift, to make the most important examples, always have to be compensated in CTSDM with dedicated techniques implemented adding circuit parts that are (or potentially are) power consuming. Therefore, the strategy at this step has been to verify if these countermeasures for jitter and RC-Product spread would have costed as low power consumption as to represent an overall motivation to proceed with a CT version. Literature helped in forecast and a preliminary high level part. It was the case and the design phase could start. Once the 100dB performance had been secured simulating the whole modulator at a transistor level, the layout phase allowed to obtain a candidate modulator for fabrication. Another phase of simulations allowed to adjust the layout in order to keep the performances confirmed during the design step. The prototype could then be fabricated in HCMOS9A technology and, once ready and packaged, measured in laboratory to check performance.

The results obtained during this work allowed to publish a paper with the title "Quantitative Jitter Simulations and FIR-DAC sizing for Single-Bit Continuous Time Sigma Delta Modulators" to LASCAS2021 conference [83]. The paper presents the importance of accuracy of jitter model while simulating CTSDM, especially in our case, where the reference is quartzless and expected to have poor performance. After presentation to LASCAS2021, this paper has been chosen among the best of the conference and invited to be extended in order to be submitted to the Special Issue (SI) of TCAS-I journal. An extended version of the paper has been therefore edited and submitted to TCAS-I with the title of "The Importance of Quantitative Jitter Simulations while Sizing a Jitter Reduction Technique for Continuous Time Sigma Delta Modulators".

Under the point of view of the industrial flow, the points missing are the following measurements under stress (temperature, prolonged use...) and "maturity" certifications (see Ch. 2, Sec. 2.3), as well as eventual interaction with customers asking for additional features and/or support.

Nevertheless, the level of completeness of this experience is undeniable: all the steps constituting the design flow have been faced extensively with a great level of accuracy, every issue encountered has been addressed as well as performance has been always restored after experiencing a degradation.

Indeed, there are also many aspects that could have been analysed with a higher level of detail. The greatest of all is the stabilization method: this method is unexplored and, during this work, many other results and possible paths has been analysed. The time constraint forced to discard these arguments to be documented in this thesis, in favor of those which had a more clear backup.

There are also many facts acknowledged *a posteriori* that would have meant a different course of action, for example, if the methods of compensation of ELD was mastered earlier, a finer optimization of the coefficients would have been made. Instead, the coefficient choice remained rigidly similar to CENTO, mainly due to stability constraints which were as well mastered too late during the 3 years. This was due to the necessary deadlines: reviewing architecture while the layout started, for example, would surely meant a too important delay on fabrication of the prototype. With deadlines respected and less time dedicated to some kind of optimizations, the thesis could be completed with real results on silicon.

Finally, there are the two major issues encountered during measurements which sources are still to be found. At the time this manuscript was completed, a series of subsequent bench setups, modulator parameters and measurement strategies was deployed and constantly evolving, in order to complete the project and achieve a functional modulator on silicon. The situation was becoming more and more clear, but the results of this procedure will unfortunately be produced later with respect of the completion of this document.

Overall, I think that this work analysed many interesting aspects about mastering continuous-time sigma-delta architectures, kept several of them eligible subjects for further optimization studies and opened to some others for which a deeper exploration can start in the future.

Appendix

Appendix A

Compensating and Correcting Effects in the Loop

In SDM, compensating and correcting are two different concepts, because there exist an internal loop filter exists, with its own internal states (voltages).

During this work, this argument has been mentioned multiple times and hereby, each of those occurrence will be explained in the context of compensation and correction, inside and outside the internal loop filter of an SDM.

The first argument was in Ch. 4, Sec. 4.6.3, while integrating the thermal noise in the separate cases of using resistors or sampling capacitors. The comment is that the A-Weighted filter is not used, since it would filter all the alias from the band of interest to the oversampling frequency, underestimating the inband folded noise. Folded noise affects the internal loop filter, therefore, its effect is acting at this stage of the circuit and conditioning the internal state evolution. The A-Weighted filter is performed by human ear, which filters the output of the circuit, already affected by alias in-band folding effects. In fact, a similar comment can be recalled from Ch. 1, Sec. 1.2.2, where it has been pointed out that A-Weighted filter can be used because the *listener* is a human ear: if it was a device, such as it is the case for audio tasks including a post processing step, the filter should be flat (the human ear would *hear later* in the chain). To conclude this case, the loop filter is sensible to signals that are not A-Weighted.

Another case, mentioned in Ch. 5 is about saturating the internal stages. A saturation is an information loss. In the Local Loop Controlled Instability method (Sec 5.4.4) it is explained how there exist a compensation in the loop and a correction a posteriori. The compensation helps a saturating stage to get back to a not-saturated region, independently from the other stages. However, the actual data this stage should be providing, is not available to the rest of the loop filter, which will then evolve its internal states in a different way. The correction can be accounted for a posteriori, but the difference triggered from this point onward in the loop filter cannot. The correction is just partially covering the consequences of a stage saturation.

The last case encountered in Ch. 6, Sec. 6.4, is basically about the same mechanics. Considering an offset introduced in the fist stage of the internal loop filter, it can be surely corrected a posteriori with a digital correction, but it is not likely to be correcting all the shape of the NTF. The information telling the presence of an offset circulates in the loop filter and influence the evolution of the internal states of the modulator, thus the output PDM. This is why it has been decided to compensate the offset directly at it source: the first integrator input pair mismatch.

Appendix B

Stability

There are a few more comments worth to mention about the stability method presented in this thesis, as it was referenced referenced in Ch. 5, Sec. 5.8.4.

A first important remark is about the setup of "Simulation 1: Stability Condition Meeting Research", there are important aspect to be considered. At the very beginning of the transient simulation, a *delta* signal is used to put the modulator in jeopardy, as the conditions meeting the criterion are voluntarily not met because VR starting value is too low with respect to VS in our case, then it increases in order to find the stability condition. There are a few parameters that have been experienced to influence this simulation and that have to be kept under control. It has been decided in this appendix not to show any and every case transient in images, instead, just some examples shown in Fig. B.1 have been chosen, while all the parameters that could be experienced to influence the value of M are reported and are the following:

- the power injected by the delta. If it is too high, it can happen that the modulator is kept stable at the beginning with the first and very low value of VS. If it is too low, a signal-dependent nature can manifest.
- the delay between the delta and the VR ramp can
- the slope of VR increasing: it should not be too steep or the system stability is perturbed by the dynamic behavior of VR.
- small signal simulations should be performed, since M can be influenced by the signal-dependent nature of the modulator. High input level and any other signal is covered in the integrating "Simulation 2".

These arguments prove the importance of the setup of the stimulus and initial transient of this simulation.

In order to integrate the main discussion about "Simulation 2: Recovery Capability Test", in Fig. B.2 and Fig. B.3 two different modulator stimuli are proposed. The first substitutes the DC stimulus at +10·FS during the (I) phase with the modification of the input sinusoidal signal, bringing it suddenly to have its amplitude equal to 10·FS. The second uses a positive sawtooth signal and, in the same way, during the (I) phase the voltage swing of this signal becomes 10·FS. In both cases, the situation before and after can be perfectly superimposed (superimposition not shown), meaning that the ill signal of the phase (I) does not prevent the modulator to operate in a stable way, no matter the kind of signal.

Many other combination of cases and modulator have been tested in this empirical study, which results have been chosen not to be shown, but which are worth to mention. An accurate and exhaustive analysis should be made on a modulator using this set of two simulations. Especially Simulation 2, proved that often it is not just a matter of finding stability or instability in a configuration, but several contouring and otherwise uncontrolled situations may happen:

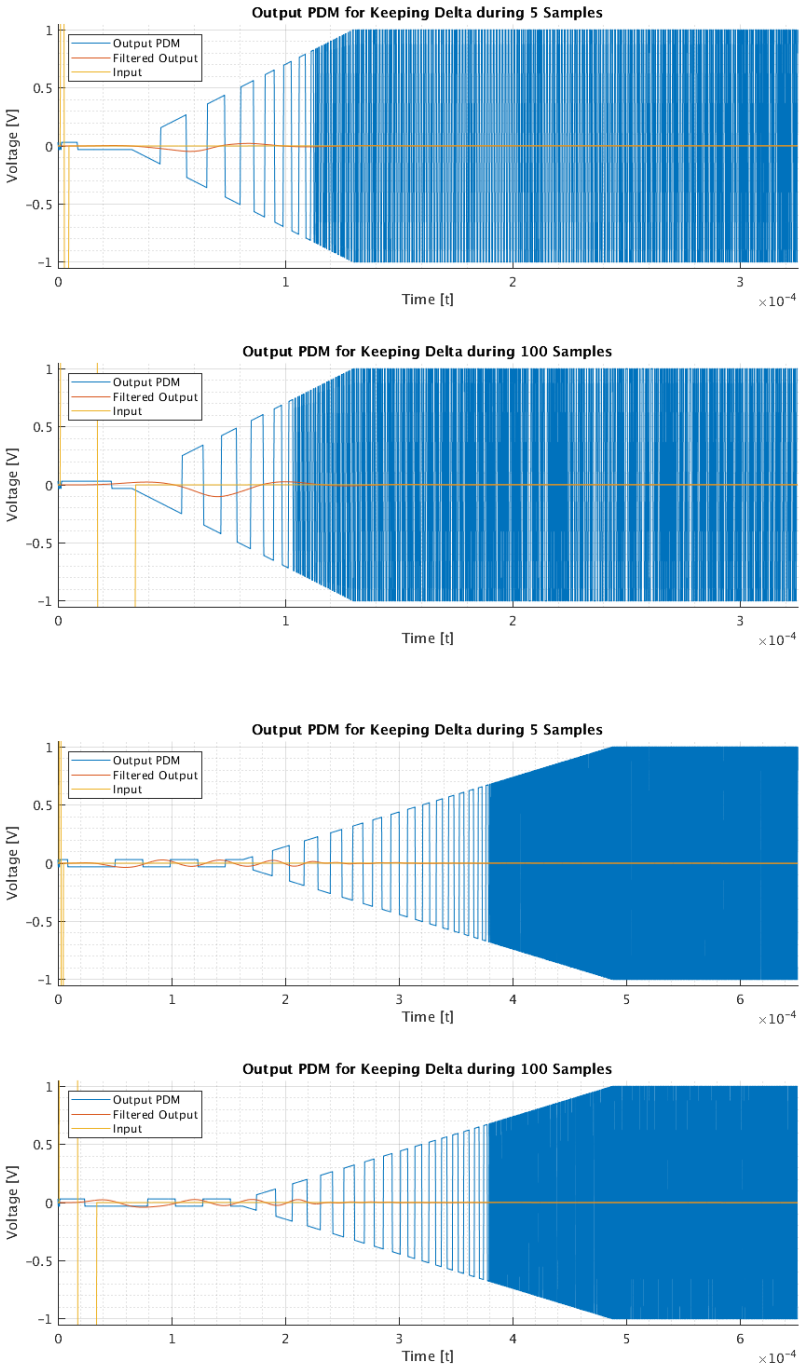

Figure B.1: Simulation showing the importance of input delta power, V_R slope and increasing delay. The first two examples on top have a delta which injects a different amount of power, causing M to change. The second two in the bottom are the same, but with a longer delay and a slower slope while increasing V_R, in this case, M is coherent, even if the power injected by the input delta is different. Notice that the time axis are not aligned between the top two and the bottom two and that therefore the bottom case represent a V_R taking even longer to increase.

- stability after some samples: already discussed in the main document, it may happen that M is not found, yet the modulator is actually stable with just a few more samples necessary to complete the transient.
- the latter can take a lot of time, it is a good practice to consider stable just those modulators which transient is compatible with the application. For example, it has been commented in Ch. 5, Sec. 5.3.3, that in audio applications, a disturb can be heard if it is lasts longer than 50μs ($\simeq$76.8 samples).
- a modulator declared stable (in general but even having found an M with Simulation 1 of our proposed method) can be put in jeopardy with a particular stimulus.
- input signal can determine a stable/unstable simulation

expecially for the latter it is worth to mention that it has been experienced, while performing a whole Dynamic Range analysis with a set of "Simulation 2", that the -5dBFS simulation shown a perfectly stable modulator after stimulus, while any other point in the DR was unstable and unreadable, after stimulus. This is why an exhaustive analysis is mandatory, stimulating the modulator with the most *dangerous* signals, for example, CTSDM4FD8 has been stimulated with a stimulus with a frequency matching the pattern.

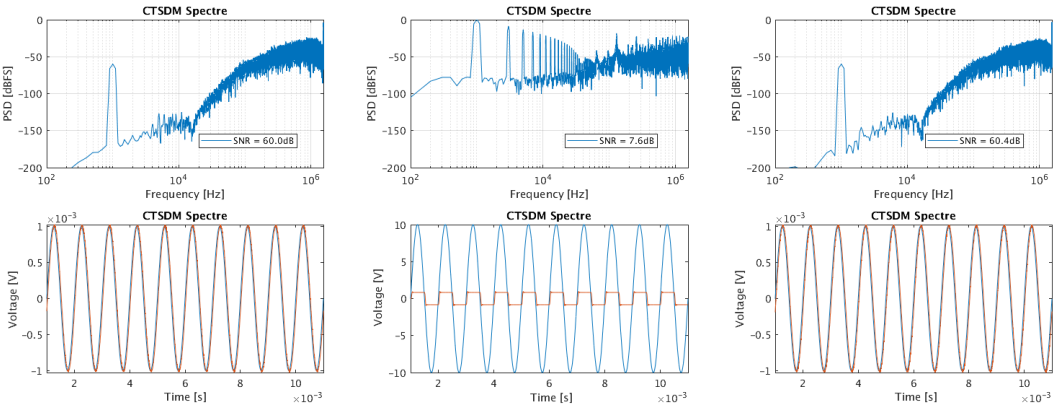

Figure B.2: "Simulation 2" with a 10·FS sinus as (I) period stimulus.

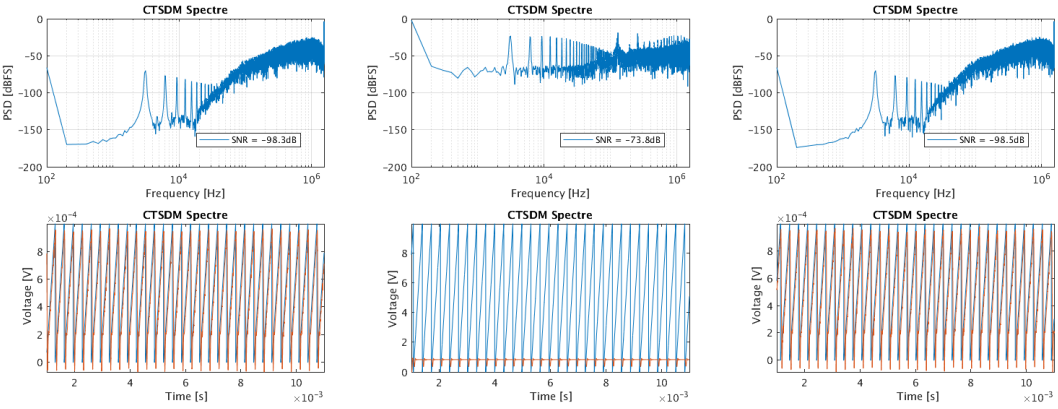

Figure B.3: Simulation 2 using a Sawtooth signal. Power changes to 10·FS during (I) period.

Appendix C

OPA Performance

The details of the design of the four amplifiers building each of the loop filter integrators have not been a main subject of discussion in this thesis. This is because the focus has been chosen to be strictly kept on Sigma-Delta related features. However, as it has been reported in the main part of this manuscript, a great work has been carried out by the master student Massimo Morabito, thanks to whom I could totally concentrate on those Sigma-Delta related features . More details about the performance reached by his efforts are given in the table present in Fig. C.1, completing the general discussion about how real amplifiers affect SDM performance.

OPA	Scenario	CC*	Gain** [dB]	UGBW** [kHz]	PM	GM** [dB]	IRN_{rms_aw}	Distortion	SR
OPA1	Typical	100µA	56.91/68.04/86.43	3.02/10.74/90.57	90°	58.21/39.68/21.01	2.54 $\frac{\mu V}{\sqrt{Hz}}$	105.96 dB	3.68 $\frac{V}{\mu s}$
	τ_{MAX}		57.63/68.89/87.44	2.14/7.58/15.97	90°	60.36/41.12/22.11	2.16 $\frac{\mu V}{\sqrt{Hz}}$	101.84 dB	3.28 $\frac{V}{\mu s}$
	τ_{min}		55.49/66.52/84.80	4.53/6.42/13.11	90°	55.47/39.00/20.46	3.09 $\frac{\mu V}{\sqrt{Hz}}$	96.23 dB	3.68 $\frac{V}{\mu s}$
OPA2	Typical	48µA	90.23/86.71	117.98/78.65	90°	59.67/46.31	3.20 $\frac{\mu V}{\sqrt{Hz}}$	97.76 dB	8.10 $\frac{V}{\mu s}$
	τ_{MAX}		90.13/86.61	37.07/24.71	90°	52.42/67.41	2.61 $\frac{\mu V}{\sqrt{Hz}}$	96.37 dB	7.24 $\frac{V}{\mu s}$
	τ_{min}		71.57/68.05	361.11/240.85	90°	30.31/69.58	4.44 $\frac{\mu V}{\sqrt{Hz}}$	75.12 dB	8.10 $\frac{V}{\mu s}$
OPA3	Typical	38µA	80.21/75.36/69.25	220.7/126.1/62.4	90°	24.37/30.81/39.60	11.86 $\frac{\mu V}{\sqrt{Hz}}$	89.69 dB	32.91 $\frac{V}{\mu s}$
	τ_{MAX}		82.98/78.12/72.02	214.3/122.4/60.6	90°	30.17/35.92/41.03	9.97 $\frac{\mu V}{\sqrt{Hz}}$	97.64 dB	20.81 $\frac{V}{\mu s}$
	τ_{min}		75.86/70.01/63.90	660.1/376.4/186.2	90°	16.86/22.18/29.42	15.14 $\frac{\mu V}{\sqrt{Hz}}$	81.32 dB	32.91 $\frac{V}{\mu s}$
OPA4	Typical	38µA	85.61/83.71/77.59	194.1/156.0/77.03	90°	58.40/29.76/52.44	11.86 $\frac{\mu V}{\sqrt{Hz}}$	101.34 dB	27.34 $\frac{V}{\mu s}$
	τ_{MAX}		86.32/84.43/78.30	61.81/49.67/24.54	90°	58.88/37.25/52.54	9.97 $\frac{\mu V}{\sqrt{Hz}}$	100.79 dB	18.17 $\frac{V}{\mu s}$
	τ_{min}		82.08/80.18/74.05	406.3/573.2/227.1	90°	57.94/21.53/53.58	15.14 $\frac{\mu V}{\sqrt{Hz}}$	101.23 dB	27.34 $\frac{V}{\mu s}$

Figure C.1: Summary of performance of the four OPA building the loop filter.

Appendix D

Timetable and Notes

<table>
<tr><th rowspan="2">Year</th><th rowspan="2">Year N</th><th rowspan="2">Month</th><th colspan="2">Activity</th></tr>
<tr><th>Theoretical</th><th>Practical</th></tr>
<tr><td rowspan="9">2018</td><td rowspan="20">Year 1</td><td>May</td><td rowspan="3">Research in Literature for
similar problems/solutions proposed.
Backup the necessity of
new circuit development.</td><td rowspan="2">MATLAB
Setup of ADC behavioral model and
results validation</td></tr>
<tr><td>Jun</td></tr>
<tr><td>Jul</td><td rowspan="8">VERILOG-A
Electrical Single Ended Implementation
Jitter Model Development
Architecture Choice
OTA Non-Idealities (Model limits)
RC-Spread</td></tr>
<tr><td>Aug</td><td rowspan="3">Evaluation of Constraints and Specifications,
choice of architecture (Order, Quantizer...)</td></tr>
<tr><td>Sep</td></tr>
<tr><td>Oct</td></tr>
<tr><td>Nov</td></tr>
<tr><td>Dec</td><td>Architecture final definition</td></tr>
<tr><td rowspan="2">2019</td><td>Jan</td><td>Stability with Delay Introduction</td></tr>
<tr><td>Feb</td><td rowspan="2">Paper for PRIME2019
Editing and submission</td><td rowspan="5">TRANSISTOR LEVEL (And Verilog-A)
Fully-Differential Implementation
(Quantizer and Delays still ideal/Verilog-A)
Thermal Noise
Offset, limit cycles and Dither</td></tr>
<tr><td>Mar</td></tr>
<tr><td>Apr</td><td>Feedback PRIME2019: Rejected</td></tr>
<tr><td rowspan="9">2019</td><td rowspan="9">Year 2</td><td>May</td><td rowspan="2">Definition of Low Power OPA Subject
(To be proposed to Internship Student)</td></tr>
<tr><td>Jun</td></tr>
<tr><td>Jul</td><td rowspan="6">Internship - Master Student Thesis
Subject: Four Low Power Operational
Amplifiers for a Continuous-Time
Sigma-Delta Modulator Audio Converter</td><td rowspan="3">TRANSISTOR LEVEL (Prototype Phase)
Full-MOS Implementation
Jitter
Worst Case
Statistical/Montecarlo
Stage Student OPAs in SDM (January)</td></tr>
<tr><td>Aug</td></tr>
<tr><td>Sep</td></tr>
<tr><td>Oct</td></tr>
<tr><td>Nov</td></tr>
<tr><td>Dec</td></tr>
<tr><td rowspan="11">2020</td><td rowspan="11">Year 3</td><td>Jan</td><td rowspan="2"></td></tr>
<tr><td>Feb</td><td rowspan="4">LAYOUT</td></tr>
<tr><td>Mar</td><td rowspan="3">Second version of paper Edited
Submitted to ICECS2020</td></tr>
<tr><td>Apr</td></tr>
<tr><td>May</td></tr>
<tr><td>Jun</td><td></td><td rowspan="2">PLS Simulations</td></tr>
<tr><td>Jul</td><td rowspan="2">Thesis Organisation</td></tr>
<tr><td>Aug</td><td>MPW Deadline</td></tr>
<tr><td>Sep</td><td>Paper Rejected: resubmitted to LASCAS2021</td><td rowspan="3">Prototype fabrication period.</td></tr>
<tr><td>Oct</td><td rowspan="3">Intrinsic Stability of a
Fourth Order CIFB SDM</td></tr>
<tr><td>Nov</td></tr>
<tr><td>Dec</td></tr>
<tr><td rowspan="3">2021</td><td>Jan</td><td>Thesis Editing</td></tr>
<tr><td>Feb</td><td>LASCAS2021, SI selection for TCAS-I*</td><td>Prototype Packaging</td></tr>
<tr><td>Mar</td><td rowspan="2">Thesis Editing</td><td rowspan="2">Prototype Received, testchip
measurement organization and setup</td></tr>
<tr><td>2021</td><td>3+</td><td>Apr</td></tr>
<tr><td></td><td></td><td>May
Jun</td><td>Thesis Editing</td><td>Measurements</td></tr>
</table>

Table D.1: PhD 3-Years Timetable.

* : The paper was selected for the Special Issue (SI) of LASCAS2021 in TCAS-I within a selection of the best papers of this conference. February 2021 has been mostly dedicated to edit an extended version of the previously presented conference paper.

Instruments used for Measurements

Instrument	Description
Agilent 34401A Multimeter	2x, one used as VPLUS generator, the other used as Multimeter
Toellner TOE 8733	Multiple-output power supply used for Reference and Current Bias
Hewlett Packard 34401A Multimeter	Used to eventually force Reference Voltage
National Instruments PXI-1042Q	Used for I2C communication protocol
Audio Precision - 525 audio analyzer	Input provider and Output analyzer for audio

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