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Sorbonne Université

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Présentée par

Doaa Mahmoud

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Le jury est composé de :

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by

Doaa Mahmoud

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List of Abbreviations & Symbols & Constants

List of Abbreviations

CT **C**ontinuous **T**ime

BP **B**and **P**ass

Q **Q**uality factor

SNR **S**ignal to **N**oise **R**atio

SNR$_Q$ **S**ignal to **Q**uantization **N**oise **R**atio

OSR **O**ver **S**ampling **R**atio

DAC **D**igital to **A**nalog **C**onverter

FD-SOI **F**ully **D**epleted **S**ilicon **O**n **I**nsulator

LHP **L**eft **H**alf **P**lane

PM **P**hase **M**argin

SCL **S**ource **C**oupled **L**ogic

FOM **F**igure **O**f **M**erit

UTBB **U**ltra **T**hin **B**ody and **B**uried Oxide

DWA **D**ata **W**eighted **A**veraging

CIFF **C**ascaded of **I**ntegrator **F**eed-**F**orward

LVT **L**ow **T**hreshold **V**oltage

IOT **I**nternet **O**f **T**hings

LPTV **L**inear **P**eriodically **T**ime **V**arying

STF **S**ignal **T**ransfer **F**unction

NTF **N**oise **T**ransfer **F**unction

List of Symbols

$\Sigma\Delta$ Sigma Delta

$g_{1,\ 2}$ Feedback coefficients of 2-op-amp resonator $\Sigma\Delta$ modulator before scaling

$a_{1\ :\ 5}$ Coefficients for DACs of 2-op-amp resonator $\Sigma\Delta$ modulator before scaling

$b_{1\ :\ 6}$ Coefficients for DACs of 1-op-amp resonator $\Sigma\Delta$ modulator

$w_{01\ ,\ 02}$ Two resonance frequencies centered at the bandwidth of 1-op-amp resonator $\Sigma\Delta$ modulator

A Integrator gain of the 2-op-amp resonator

R Integrator resistor of the 2-op-amp resonator

C Integrator capacitor of the 2-op-amp resonator

R_F Feedback resistor of the 2-op-amp resonator

T_s Sampling period

A_0 DC-gain of op-amp

f_p The 1st pole of op-amp

f_0 Centre frequency of the resonator

f_s Sampling frequency

R_{in} Input resistor of the 1-op-amp resonator

$R_{1,2}$ Feedback resistors of the 1-op-amp resonator

$C_{1,2}$ Feedback capacitors of the 1-op-amp resonator

R_p Highpass filter resistor of the 1-op-amp resonator

C_p Highpass filter capacitor of the 1-op-amp resonator

$g^*_{1,\ 2}$ Feedback coefficients of 2-op-amp resonator $\Sigma\Delta$ modulator after scaling

$a^*_{1\,:\,5}$ Coefficients for DACs of 2-op-amp resonator $\Sigma\Delta$ modulator after scaling

X_t The input of $\Sigma\Delta$ modulator before scaling

Y_n The output of $\Sigma\Delta$ modulator

$X_t{}^*$ The input of $\Sigma\Delta$ modulator after scaling

I_{scale} A parameter to scale all feedback coefficients, $a_{1\,:\,5}$, in the 2-op-amp resonator $\Sigma\Delta$ modulator

t_d The loop delay of $\Sigma\Delta$ modulator

U_i The equivalent noise source at the input of each integrator in 2-op-amp resonator $\Sigma\Delta$ modulator

$H_i(s)$ The transfer function, from the equivalent input noise source, $U_i(s)$, to the modulator output, $Y(s)$

$\Sigma\Delta_{BW}$ Bandwidth of each CT BP $\Sigma\Delta$ modulator

$\overline{V_{n,\Sigma\Delta}}^2$ Input-referred in-band noise power of 2-op-amp resonator $\Sigma\Delta$ modulator

$\overline{V_{n,R}}^2$ The noise power of integrator resistor of the 2-op-amp resonator

$\overline{V_{n,R_F}}^2$ The noise power of feedback resistor of the 2-op-amp resonator

$SNR_{error}(\%)$ the signal to noise ratio error

$\overline{V_{n,1^{st}\ integrator}}^2$ The input-referred in-band noise power of the 1st integrator in 2-op-amp resonator $\Sigma\Delta$ modulator

$\overline{V_{n,3^{rd}\ integrator}}^2$ The input-referred in-band noise power of the 3rd integrator in 2-op-amp resonator $\Sigma\Delta$ modulator

G_{m1} The transconductance of the 1st stage in the op-amp

G_{m2} The transconductance of the 2nd stage in the op-amp

G^*_{m1} The transconductance of the feedforward stage in the op-amp

A_{dc1} The DC-gain of the 1st stage in the op-amp

A_{dc2} The DC-gain of the 2nd stage in the op-amp

A^*_{dc1} The DC-gain of the feedforward stage in the op-amp

ω_{p1} The pole of the 1st stage in the op-amp

ω_{p2} The pole of the 2nd stage in the op-amp

$r_{o1}C_1$ The product of the total resistance and the total capacitance

seen at the 1st stage in the op-amp

$R_L C_L$ The product of the total resistance and the total capacitance seen at the 2nd stage in the op-amp

W_f The width per finger of each transistor

L_f The length per finger of each transistor

$N_{fingers}$ The number of fingers of each transistor

I_b The dc current needed for biasing circuits

$BB_{1,\ 2}$ The free body bias voltages in the op-amp

R_{cm} The resistor for the common-mode feedback circuits in the op-amp

V_{TH_n} The threshold voltage of NMOS transistor

V_{TH_p} The threshold voltage of PMOS transistor

f_T Unity gain frequency of the op-amp

$f_{T_{n,p}}$ Unity current gain frequency of the NMOS/PMOS flipped-well transistor

$BB_{Pre-Amp,\ Latches-Inverter}$ The free body bias voltages of the pre-amp and latch/inverter

R_{cm_1} The resistor for the common-mode feedback circuits in the pre-amp and latch/inverter

$I_{out+,-}$ The output currents of the current steering DAC circuit

BB_{DACs} The free body bias voltage of the current steering DAC circuits

$f_{r_{1,\ 2}}$ The resonance frequency of the 1st resonator and the 2nd resonator in 4th-order loop filter, which it is composed of two 2-op-amp resonator connected in series

List of Constants

k_B The Boltzmann constant $1.3811 \cdot 10^{-23}$

T The temperature 300K

μ 10^{-6}

n 10^{-9}

Abstract

We target to design a continuous-time band-pass $\Sigma\Delta$ modulator at 400 MHz for different receiver architectures. The 1st receiver architecture is from mm-wave-to-digital signal for 5G applications, where $\Sigma\Delta$ modulator samples moderate IF signal (@400 MHz) and enables a single-phase mm-wave passive local oscillator and moves I/Q mixing into the digital domain [Lu21]. The 2nd receiver architecture can digitize the RF signal directly without down-converting to low-frequency [Sayed20a]. Then it can be utilized for applications in the vicinity of 400 MHz, namely Advanced Research and Global Observation Satellite (ARGOS), Medical Implant Communication Service (MICS), and so on. We focus on the active RC resonators for a lower chip area than LC tank resonators. We introduce a new comparison between the two-op-amp resonator CT BP $\Sigma\Delta$ modulator and the one-op-amp resonator CT BP $\Sigma\Delta$ modulator. We study the sensitivity of the quality factor and the signal to noise ratio to the DC-gain op-amps in two-op-amp resonator $\Sigma\Delta$ modulator. It also shows how, in one-op-amp resonator $\Sigma\Delta$ modulator, the quality factor and the signal to noise ratio, are very sensitive to any variations in the capacitors values for limited DC-gain op-amps. We establish an approximate mathematical model of the thermal-noise behaviour for two-op-amp resonator CT BP $\Sigma\Delta$ modulator. This model matches the circuit simulator results with a good accuracy (error $\leq$ 2.5 %). Furthermore, we demonstrate that a high quality factor (>100) of the two-op-amp resonators can be achieved by selecting the proper value of the integrator gain at a moderate DC-gain op-amp (35 dB). Both $\Sigma\Delta$ modulators are designed using flipped-well devices on fully depleted silicon on insulator (FDSOI-28nm) technology.

Chapter 1

Introduction

1.1 Context and Motivation

Software defined radio (SDR) receiver is a promising technique for future receivers which provides a variety of protocols and be utilized in many applications. For example, in cognitive radio, the receiver is configured depending on the current usage of the channels to efficiently make use of the limited bandwidth. Nowadays SDR is difficult to achieve due to the difficulties of implementation and the large power consumption, but scaling of technology, thanks to fully depleted silicon on insulator (FDSOI) technology, plays a leading role in solving some of these challenges. An SDR receiver digitizes the RF signal without down-converting to low-frequency or base-band which omits many RF and analog blocks. Filtering, channel selection and mixing are done in the digital domain without the effect of thermal noise, non linearity and mismatch. Digital processing is easily upgradable by the software as shown in Fig. 1.1. In this work, we propose an SDR receiver based on a bandpass $\Sigma\Delta$ modulator (RF-ADC) which is an oversampling ADC and its resolution is improved by increasing the sampling-rate.

The most essential element for RF-ADC is the loop filter, there are two main configurations, an LC tank resonator and an active RC resonator. The LC tank resonator can be tuned at higher operating frequencies $\geq$ 433 MHz as the design examples of [Beilleau09], [Ashry11a], [Ashry11b], [Shibata12], [Ashry13], [Ashry15], [Belfort17] and [Sayed20a].

In this work, we focus on the active RC resonators for a lower chip area compared to the LC tank resonators. We target applications in the vicinity of 400 MHz, namely Advanced Research and Global Observation Satellite (ARGOS), Medical Implant Communication Service (MICS), Automobile Keyless system and Industrial, Scientific and Medical (ISM).

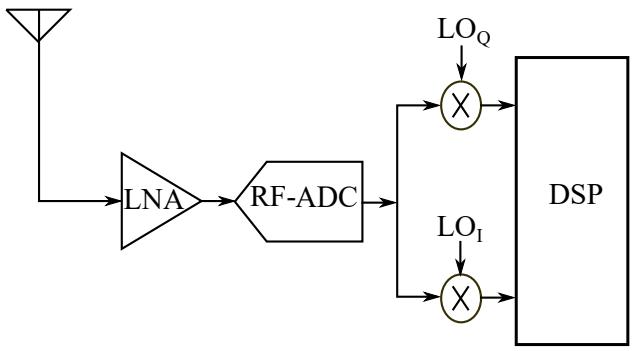

Fig. 1.1: A software defined radio (SDR) receiver.

1.2 Contribution

In this work, we compare between the two-op-amp resonator CT BP $\Sigma\Delta$ modulator and the one-op-amp resonator CT BP $\Sigma\Delta$ modulator. We study the sensitivity of both the quality factor Q and the signal to noise ratio (SNR) to the DC-gain A_0 of op-amps in CT BP $\Sigma\Delta$ modulator based on two-op-amp resonators. It also shows how, in CT BP $\Sigma\Delta$ modulator based on one-op-amp resonators, the quality factor Q and the signal to noise ratio (SNR), are very sensitive to any variations in the capacitors values for a limited DC-gain A_0 of the op-amp. We establish an approximate mathematical model of the thermal noise behaviour for CT BP $\Sigma\Delta$ modulator based on two-op-amp resonators. This model matches the circuit simulator results with a good accuracy (error $\leq$ 2.5 %). It can then avoid lengthy transient circuit simulations. Furthermore, we demonstrate that a high quality factor Q (>100) of the two-op-amp resonators can be achieved by selecting the proper value of the integrator gain, A. This high Q is achieved with a moderate DC-gain for the op-amp, $A_0 = 35\ dB$. Both 4th-order CT BP $\Sigma\Delta$ modulators, with one-op-amp resonators and two-op-amp res-

onators, are designed using Low V_{TH} "flipped-well" devices on fully depleted silicon on insulator (FDSOI) technology. Body biasing in FD-SOI provides a wide tuning range that is used to compensate the process, voltage and temperature (PVT) variations.

1.3 Short description of the manuscript structure (each chapter)

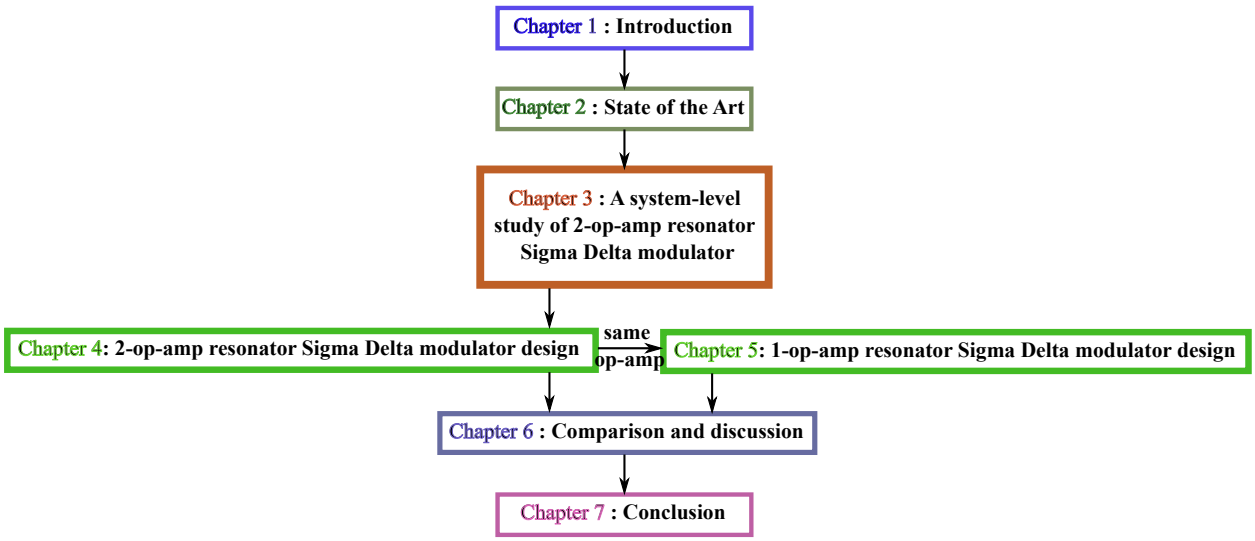

Fig. 1.2: A flowchart describes the flow of thesis manuscript.

Fig. 1.2 shows the flowchart which describes the flow of thesis manuscript. Thesis manuscript consists of seven chapters and two appendices which listed as following:

1. **Introduction:**

   In section 1.1, we first discuss the context and the motivation. We present the contribution, in section 1.2. A short description of the manuscript structure is introduced, in section 1.3.

2. **State of the Art:**

   In this chapter, we present the state of the art.

   First, in section 2.2, we discuss the basic concepts about $\Sigma\Delta$ modulators such as oversampling ADC, continuous-time $\Sigma\Delta$ modulator and bandpass $\Sigma\Delta$ modulator. Second,

we review the previous designs of BP CT $\Sigma\Delta$ modulators designs based on both of two-op-amp resonators, in section 2.3, and those based on one-op-amp resonators, in section 2.4. Third, in section 2.5, we discuss the fully depleted silicon on insulator FD-SOI technology particularly the flipped-well devices which are used in our $\Sigma\Delta$ modulators designs and its body biasing feature. Also, we show some design examples which were implemented on this technology. We also present the devices used in the design of both CT BP $\Sigma\Delta$ modulators. At the end, in section 2.6, we present the previous analyses of the thermal-noise in CT $\Sigma\Delta$ modulators.

3. **A system-level study of "4th-order CT BP two-op-amp resonator $\Sigma\Delta$ modulator":**

   In this chapter, we present a system-level study of 4th-order CT BP $\Sigma\Delta$ two-op-amp resonator modulator.

   First in section 3.2, we present the scaling method of the coefficients for the modulator. Second in section 3.3, we show the approximate linear model of the 4th-order CT BP $\Sigma\Delta$ modulator. Third in section 3.4, we compute the input-referred thermal-noise power of the integrators. We also study the influence of integrator resistor "R" and integrator gain "A" on the input-referred thermal-noise power of the modulator, in section 3.5. Also, we show the op-amps DC-gain "A_0" effect on both the quality factor "Q" and the resonance frequency "f_0" of the 2-op-amp resonator along with the SNR of the modulator, in section 3.6. The integrators gain A influence on the quality factor of the 2-op-amp resonator is presented using the mathematical model and compared with the transistor-level simulation results, in section 3.7.

4. **Two-op-amp resonator CT BP $\Sigma\Delta$ Modulator design:**

   In this chapter, we present the complete design of a two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator.

   First in section 4.2, we discuss the system-level of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Second in section 4.3, we discuss the transistor-level design of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Third in section 4.4, we discuss the

layout of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. At the end, we show the post-layout simulation results and we compare them to the state of the art, in section 4.5.

5. **One-op-amp resonator CT BP $\Sigma\Delta$ Modulator design:**

   In this chapter, we present the complete design of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator.

   First in section 5.2, the op-amps DC-gain "A_0" effect on both the quality factor "Q" and the resonance frequency "f_0" of the 1-op-amp resonator, along with the SNR of the 1-op-amp resonator CT BP $\Sigma\Delta$ modulator is introduced. Second in section 5.3, we discuss the system-level of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Third in section 5.4, we present the transistor-level design of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Then in section 5.5, we present the layout of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Finally, we compare the post-layout simulation results to the state of art, in section 5.6.

6. **Comparison and discussion:**

   In this chapter, we compare the two-op-amp resonator CT BP $\Sigma\Delta$ modulator to the one-op-amp resonator CT BP $\Sigma\Delta$ modulator.

   In section 6.2, we first discuss the quality factor "Q" of each resonator. Second in section 6.3, we show the signal to noise ratio "SNR" for both $\Sigma\Delta$ modulators. Third in section 6.4, the post-layout simulation results of the "worst-case" process corners of both $\Sigma\Delta$ modulators are introduced. Finally, we discuss the dynamic range and input third order intercept point (IIP3) for each $\Sigma\Delta$ modulator, in section 6.5.

7. **Conclusion**:

   We present our conclusions.

8. **Appendices**:

   a) Process corners procedure on "28nm-FDSOI" technology.

   b) The MATLAB code gets the transfer function of the gain for a two-op-amp resonator at limited DC-gain A_0 and infinite pole of the op-amps.

   c) The MATLAB code obtains the transfer function of the gain for the one-op-amp resonator at limited DC-gain A_0 and infinite pole of the op-amps.

d) The MATLAB code of the noise analysis of the 4th-order continuous-time band-pass $\Sigma\Delta$ modulator based on two-op-amp resonators.

e) The MATLAB code of the mathematical model for the two-op-amp resonator using two-stage feed-forward op-amp.

Chapter 2

State of the Art

2.1 Introduction

In this chapter, we present the state of the art.
First, in section 2.2, we discuss the basic concepts about $\Sigma\Delta$ modulators such as oversampling ADC, continuous-time $\Sigma\Delta$ modulator and bandpass $\Sigma\Delta$ modulator. Second, we review the previous designs of BP CT $\Sigma\Delta$ modulators designs based on both of two-op-amp resonators, in section 2.3, and those based on one-op-amp resonators, in section 2.4. Third, in section 2.5, we discuss the fully depleted silicon on insulator FD-SOI technology particularly the flipped-well devices which are used in our $\Sigma\Delta$ modulators designs and its body biasing feature. Also, we show some design examples which were implemented on this technology. We also present the devices used in the design of both CT BP $\Sigma\Delta$ modulators. At the end, in section 2.6, we present the previous analyses of the thermal-noise in CT $\Sigma\Delta$ modulators.

2.2 Basic concepts about $\Sigma\Delta$ modulators

Oversampling ADCs convert analog inputs to digital signals based on high sampling rates. Any complex processing units need processing digital signals but every real signal exists in the analog domain (continuous-time/continuous-amplitude). The quality of analog to digital conversion is very important in order not to lose the original information during the

conversion, and it is mostly related with the resolution of the ADC. Due to the digitization process, quantization noise is added to the original signal. This quantization noise usually behaves like white noise. The quantization noise decreases the quality of the original signal by decreasing the signal-to-noise ratio (SNR). It is known that the fundamental SNR in dB, when one sample has 2^N equally-spaced possible levels, can be:

$$SNR = 6.02 \cdot N + 1.76 \ [dB] \tag{2.1}$$

Where N is the number of bits for ADC, and F_s is the sampling frequency. Nyquist-rate ADCs convert signals with frequencies up to Nyquist-rate $F_s/2$, they are difficult to have both high speed and high resolution due to analog component imperfections [Schreier05], [Schreier96]. For example, the mismatch between the passive components such as capacitors in SAR ADCs causes harmonics and distorts the signal. As CMOS technology scales, it gets more difficult to have good matching between components and the maximum resolution is becoming saturated [Le05]. Instead, an oversampling ADC improves resolution by increasing the sampling rate, F_s, instead of increasing the number of sampled levels, N.

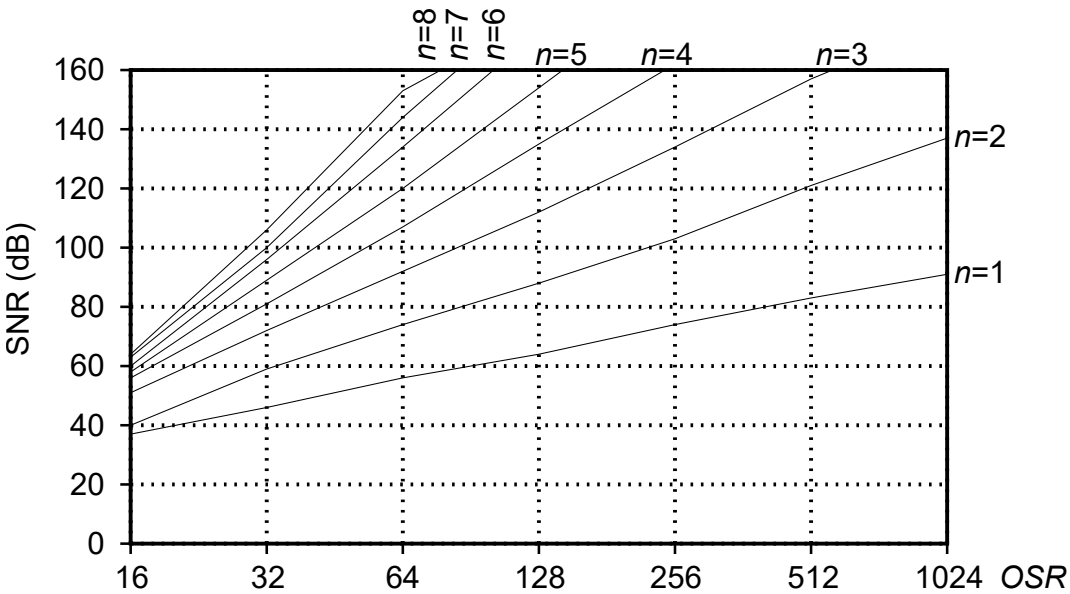

Fig. 2.1: SNR Limits for Lowpass $\Sigma\Delta$ Modulators versus oversampling ratio (OSR) and loop-filter's order (n) [R. Schreier].

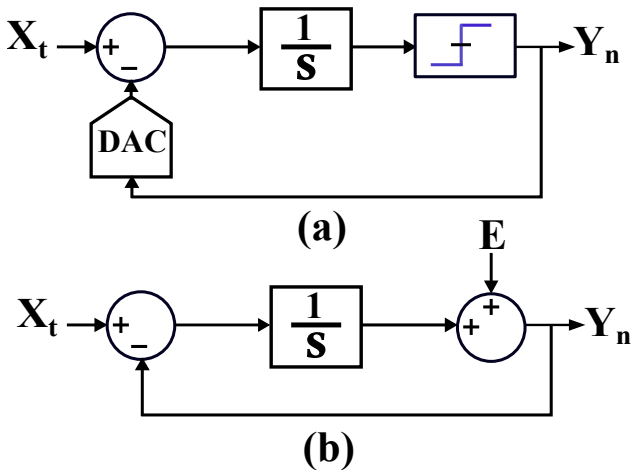

Fig. 2.2: 1st-order continuous-time Low-pass $\Sigma\Delta$ modulator 1-bit (a), with its linear model (b).

A $\Sigma\Delta$ modulator is considered as an oversampling ADC. As shown in Fig 2.1, The signal to noise ratio (SNR) of Low-pass $\Sigma\Delta$ Modulators is increasing by using a higher oversampling ratio (OSR) or designing a higher order (n) of loop-filter.

Its basic configuration is a feedback loop with an integrator, a local low resolution quantizer (1-bit) and feedback digital-to-analog converter (DAC) as shown in Fig 2.2 in (a) with its approximate linear model (b). The transfer function from the input X_t to the output Y_n is called signal transfer function (STF), and the transfer function from the quantization noise E to the output Y_n is noise transfer function (NTF).

$$STF = \frac{Y_n}{X_t} = \frac{1}{s+1}, \qquad NTF = \frac{Y_n}{E} = \frac{s}{s+1} \tag{2.2}$$

From equation 2.2, the feedback loop generates a notch at DC in the noise transfer function (NTF) and shapes the quantization noise, decreasing the in-band noise floor level as in Fig 2.3. The STF is not affected by this noise shaping as STF and NTF are different since the summing nodes are different. STF can be flat in-band. A high SNR can be achieved by considering the signal and the noise only in a specific frequency range where the noise floor level is shaped.

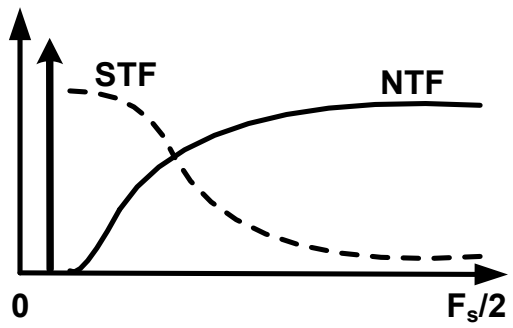

Fig. 2.3: Signal Transfer Function (STF) and Noise Transfer Function (NTF) of Fig 2.2 [Chae13a].

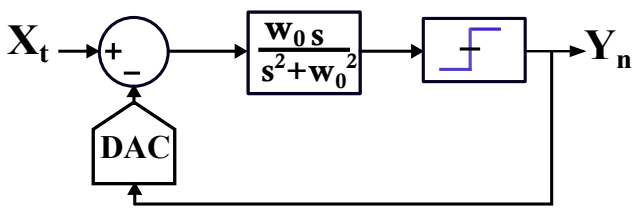

Fig. 2.4: 2nd-order continuous-time band-pass $\Sigma\Delta$ modulator 1-bit.

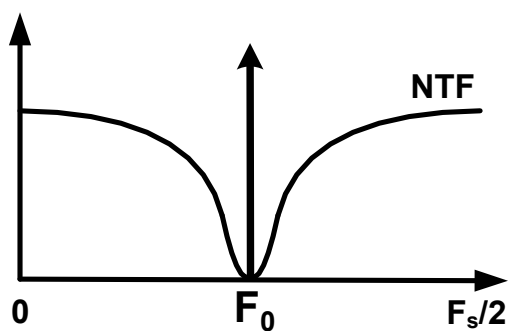

Fig. 2.5: Noise Transfer Function (NTF) of 2nd-order continuous-time band-pass $\Sigma\Delta$ modulator of Fig 2.4 [Chae13a].

Low-pass $\Sigma\Delta$ modulators have notches around DC in the noise transfer function (NTF), so the signal band is located at low frequency as shown before in Fig 2.3. In Fig. 2.4, by using a band-pass filter in the loop-filter centred at F_0, it modifies both of the signal transfer function (STF) and noise transfer function (NTF), which leads to have a notch in the noise

transfer function (NTF) at a mid or high frequency region. This means that the noise shaping lowers the noise floor level at RF or IF as shown in Fig 2.5. Consequently, the signal band can be at RF or IF, and it can digitize the signal directly without down-converting. In the following section, we discuss two different active RC resonators which are commonly utilized in CT BP $\Sigma\Delta$ modulators.

2.3 CT BP $\Sigma\Delta$ Modulators based on two-op-amp resonators

There are two main types of active RC resonators which are widely used in CT BP $\Sigma\Delta$ modulators. In this section, we discuss the first type called the two-op-amp resonator as shown in Fig. 2.6 . The two-op-amp resonator composes of two integrators, the 2nd integrator output connects to the op-amp input of the 1st integrator through the feedback resistor, R_F. Each integrator has an integrating capacitor C and an integrating resistor R.

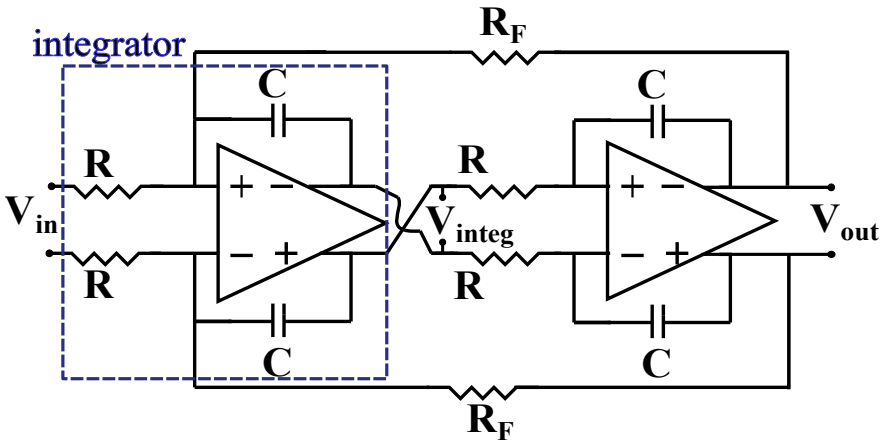

Fig. 2.6: Two-op-amp resonator circuit.

In [Shibata12], a 6th-order low-pass/band-pass $\Sigma\Delta$ modulator operates in a wide tunable range from DC to 1 GHz. According to the band-pass part, it can achieve a bandwidth of 100 MHz−75 MHz at center frequency f_0 equals to 450 MHz−1 GHz with the peak signal to noise ratio (SNR) of 72 dB−63 dB at a sampling frequency of 4 GHz while consuming 550 mW. The design is implemented by a re-configurable LC tank and 4th-order active-RC loop

filter using 2-op-amp resonators (this design style is called hybrid LC/active-RC structure). A feedback-architecture is used to avoid the out of band peaks in the signal transfer function (STF), despite having a lower power efficiency than a feedforward-architecture [Schreier05]. That is why we used the feedback-architecture in our designs for both types of CT BP $\Sigma\Delta$ modulators. The loop filter is tuned to have the resonance frequencies distributed within the band of interest. Normally, the 1st resonator for any order loop filter has the stringent requirements. The proposed solution by [Shibata12] is using an external (off-chip) inductor for a great linearity and power efficiency containing a high quality factor. The specifications of the used op-amps, to achieve a good linearity, in the active-RC loop filter, are 40 dB of gain at 1.5 GHz and the effective gain-bandwidth of 150 GHz and 15 GHz unity-gain frequency f_T with a phase margin 65°. To satisfy these requirements, a 7th-order (multi-stage) multi-path feedforward amplifier is designed, consuming 112.5 mW, at a 1-V supply voltage. It is the reason for the very high power consumption of this design (550 mW). This type of op-amp also used in [Leung01], [Thandri03], [Shibata12], [Gebreyohannes19], [Gebreyohannes20] are conditionally stable, they become unstable if the signal swing is sufficiently large. Nevertheless, multi-stage multi-path feed-forward op-amp designs are commonly employed in most of prior design examples for 2-op-amp resonator LP CT $\Sigma\Delta$ modulators in [Mitteregger06] and 2-op-amp resonator BP CT $\Sigma\Delta$ modulators in [Lu10], [Shibata12], [Yang16] and [Yang18]. Consequently, we had to explore the quality factor vulnerability to the op-amp DC-gain A_0 for the two-op-amp resonators as discussed later in chapter 3. Also, the influence of the op-amp DC-gain A_0 on the maximum SNR of the 4th-order CT BP $\Sigma\Delta$ modulator is studied. After, we show that by determining the value of integrator gain A, it leads to improve the quality factor Q and the linearity of $\Sigma\Delta$ modulator, using a moderate DC-gain op-amp $A_0 = 35\ dB$ implemented by only a two-stage stable op-amp.

2.4 CT BP $\Sigma\Delta$ Modulators based on one-op-amp resonators

In this section, we discuss the second type of the resonators called the one-op-amp resonator as shown in Fig. 2.7. [Chae13b] proposed this power-efficient resonator with a single amplifier as a loop-filter. The motivation for introducing this resonator is to overcome the disadvantages of the traditional LC and two-op-amp resonators: 1) the LC resonator consumes a huge area. 2) the two-op-amp resonator consumes a lot of power and contributes to thermal noise of the modulator as mentioned in section 2.3. The use of only one op-amp can reduce the noise contribution to the loop and it should also decrease the power consumption for a given noise requirement.

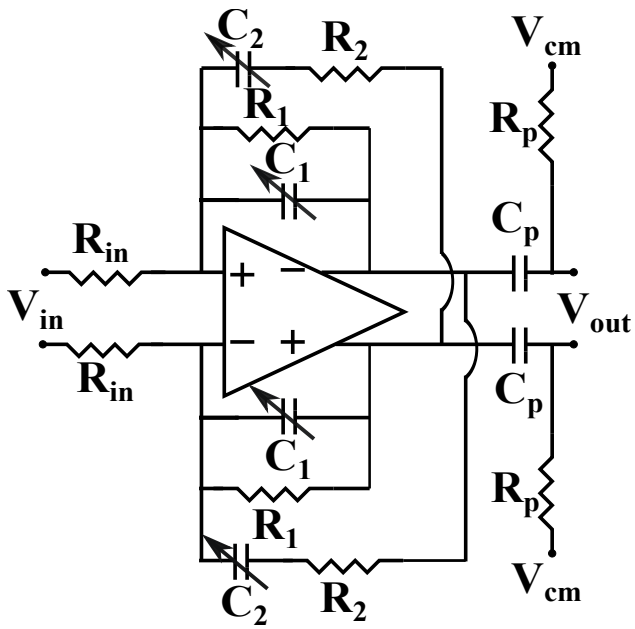

Fig. 2.7: One-op-amp resonator circuit.

In [Chae13b], a 4th-order CT BP $\Sigma\Delta$ modulator, based on this resonator, was designed with a 24 MHz bandwidth at a center frequency $f_0 = 200\ MHz$ and a sampling frequency $f_s = 800\ MHz$. This $\Sigma\Delta$ modulator achieves signal to noise ratio (SNR) of 58 dB, 60 dB dynamic range, with a total power consumption of 12 mW. As shown in Fig. 2.7, a positive

feedback connection, through the resistor R_2 and the capacitor C_2, is applied to realize a high quality factor resonator with a single amplifier, inspired from the design of voltage-controlled oscillators of [Liu99]. Its transfer function can be derived using an ideal op-amp, as following:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{R_1}{R_{in}} \cdot s \cdot \frac{1}{R_1 C_1}}{s^2 + s\ \{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} - \frac{1}{R_2 C_1}\} + s^0\ \{\frac{1}{R_1 R_2 C_1 C_2}\}} \tag{2.3}$$

To have an infinite quality factor, the term of s in the denominator, must be eliminated. The proposed condition is at $C_2 = 2\ C_1$ and $R_1 = 2\ R_2$.

The drawback mentioned by [Chae13b], is the bad linearity compared to the two-op-amp resonator due to using the positive feedback connection. He suggested to utilize this resonator in a modulator with a feedforward architecture since the feedforward architecture reduces the required swing from the op-amps where the non-linearity occurs. Actually we faced this problem in our design, discussed in chapter 5, as we use the feedback architecture that is applied on both types of $\Sigma\Delta$ modulators to realize a fair comparison.

From Eq 2.3, the quality factor of the resonator is determined by the capacitors whose values give the coefficient of s in the denominator of Eq 2.3. In [Chae13b], 4-bit capacitor banks are then used to fine-tune the quality factor, moreover this resonator needs a high DC-gain op-amp, $A_0 = 73\ dB$, to achieve a high quality factor.

The op-amp design, used in this resonator, has four cascading stages to provide a high overall gain and also achieve a sufficient voltage headroom of more than half the supply voltage ($V_{DD} = 1.25\ V$). The overall specifications of the op-amp are 73 dB DC-gain and 65° phase margin. The gain at 200 MHz is 30 dB, and the total power consumption is 2 mW.

In [Chae16], a 6th-order modulator using the one-op-amp resonator, with a single feedforward path from the output of the 1st resonator to the input of the 3rd resonator, is presented that shows a measured signal to noise ratio of 69 dB over a 25 MHz bandwidth around a center frequency $f_0 = 200MHz$, while consuming around 35 mW. This $\Sigma\Delta$ modulator uses also a 4-stage op-amp design, to provide more than 50 dB gain at 200 MHz. The op-amp

for the first resonator, has a 3 dB bandwidth of 450 MHz and DC-gain of 57 dB. The phase margin is approximately 50°. A separate high supply voltage of 1.7 V is used for the last stage of the op-amp to achieve a large voltage swing, while the other stages operate at a 1.2 V supply voltage. The power consumption of the first resonator is 7.5 mW, while the other two resonators consume a total of 9 mW.

While at [Jang18], the proposed digital beamformer utilizes 16 element of 4th-order continuous-time band-pass $\Sigma\Delta$ modulator based on power-/area-efficient 1-op-amp resonators. Each digitizes an intermediate frequency of 1 GHz at sampling frequency $f_s = 4\ GHz$ for a 100 MHz bandwidth with a signal to noise ratio (SNR) of 48 dB using 15.25 mW power consumption. The overall 16-element array achieves a SNR of 58.5 dB which corresponds to a 10.5 dB improvement from the array. For compensating the process, voltage and temperature (PVT) variations, the center frequency f_0 of the resonator is tuned with 3-bit trimming capacitor banks for the capacitors $C_{1,\ 2}$. A 3-stage cascaded op-amp is used to provide DC-gain of 71 dB and a 13.22 GHz unity gain frequency f_T with a power consumption of 5.4 mW.

According to the presented prior works of the feedforward CT BP $\Sigma\Delta$ modulators architectures using the one-op-amp resonator [Chae13b], [Chae16], [Jang18] and [Bell19], it seems clear that the one-op-amp resonator needs a high DC-gain op-amp implemented by several cascading low DC-gain single stages to provide a sufficient voltage headroom. While we propose our one-op-amp resonator CT BP $\Sigma\Delta$ modulator design using a moderate DC-gain of op-amps $A_0 = 35\ dB$ that is implemented by only two-stage op-amps, in chapter 5.

Besides, most of the mentioned analyses about this filter are studied based on the ideal behaviour of the op-amp. Therefore, we present a detailed study of the quality factor's sensitivity to the RC network capacitors values at a limited op-amp DC-gain for the one-op-amp resonators, in chapter 5.

In [Kim19], the authors propose a multi-mode CT BP $\Sigma\Delta$ modulator employing the one-op-amp resonator, presented in Fig. 2.7, with an additional positive resistor-feedback. This additional connection achieves a high quality factor even if the op-amp has a low gain-bandwidth. But, the op-amps have still a high DC-gain, where the op-amps DC-gain $A_0 \geqslant 44\ dB$. Also, the op-amps have a minimum gain-bandwidth of 1.22 GHz. The center

frequencies of this multi-mode CT BP $\Sigma\Delta$ modulator can be at 2 MHz, 5 MHz or 20 MHz at a narrow signal bandwidth of 200 kHz.

The transfer function of the one-op-amp resonator, presented in Fig. 2.7, is introduced in [Kim19] at limited DC-gain of the op-amps A_0. In spite of that, it showed that the quality factor of 100 requires a DC-gain of op-amp $A_0 \geqslant 50\ dB$. In our study, we have shown that it is possible to achieve high quality factors at limited DC-gain for the op-amps $A_0 = 35\ dB$. In chapter 5, we achieved similar results by using both of coarse-trimming and very fine-trimming of the capacitors $C_{1,\ 2}$ through varactors.

2.5 Fully depleted silicon on insulator FD-SOI technology

2.5.1 Flipped-Well devices and its body biasing feature

The design implementations of our CT BP $\Sigma\Delta$ modulators are designed in a 28 nm fully depleted silicon on insulator (FD-SOI) technology using low threshold voltage devices, called "flipped-well" devices as shown in Fig.2.8. In order to obtain the lower threshold voltage $V_{TH_{n,p}}$, the NMOS transistors lay on N-Well body, while the PMOS transistors lay on P-Well body [Cathelin17]. This technology is also called ultra thin body and buried oxide (UTBB) FD-SOI as the active device has the ultra-thin conduction film which is put on the top of the insulation layer of buried oxide (BOX). Thanks to this thin silicon film, the channel is fully depleted. No pocket implants are needed for the source and drain which enhances the analog/RF transistor's behavior. Fig.2.8 shows that the device has a front gate like the regular one (in bulk technology) and the second one comes from the body connection. In this technology, more than 10 % of the process steps and seven masks are saved, resulting in an overall manufacturing process cost saving of 10 % [Jacquet14].

The body factor of these devices is approximately 85 mV/V, while the body factor in bulk technologies is limited to 25 mV/V [Cathelin17]. In bulk technologies, the possible variation of the threshold voltage is only a few tens of m-Volts. In FDSOI, the threshold voltage $V_{TH_{n,p}}$ modulation through body biasing is limited because there are parasitic diodes between N-well to P-well/P-substrate. These are Zener-type diodes, with an opening voltage around

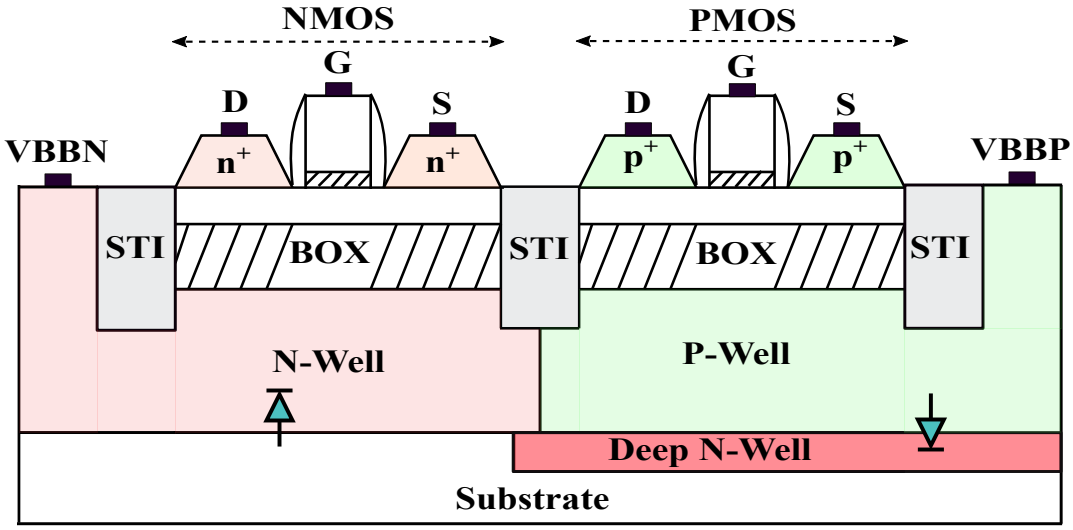

Fig. 2.8: A flipped-well CMOS Device; STI: Shallow Trench Isolation, BOX: Buried Oxide, VBBP/VBBN: Voltage Body Biasing of PMOS/NMOS transistor.

modulus of 3 V. Therefore, we can bias the body connection with a voltage range from -3 V to 3 V. There is no concern of the latch-up problem that usually happens at regular bulk technologies because the buried oxide (BOX) layer isolates totally the fully depleted channel of each NMOS/PMOS transistor from its N/P-wells, respectively. Fig. 2.9 shows the threshold voltage of the NMOS/PMOS flipped-well transistors $V_{TH_{n,p}}$ against Body Bias in range from -3 V to 3 V at $V_{DD} = 1.5\ V$. It shows that the threshold voltage $V_{TH_{n,p}}$ can vary in a range from -0.2 V to 0.76 V. We simulate this figure using the width per finger W_f equals to 1 µm, the length per finger L_f equals to 100 nm and the number of fingers $N_{fingers}$ equals to 1.0.

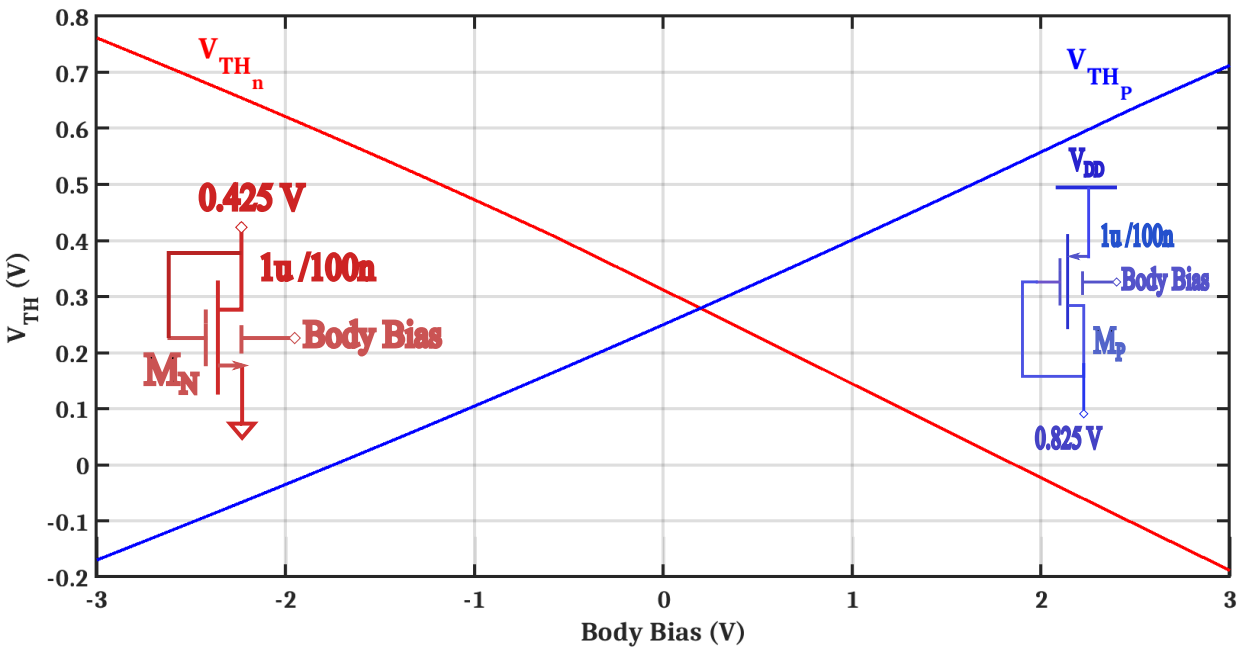

Fig. 2.9: The threshold voltage of the NMOS/PMOS flipped-well transistor $V_{TH_{n,p}}$ against Body Bias in range from -3 V to 3 V at $V_{DD} = 1.5\ V$.

This technology provides a higher G_m for a given current, combined with the lower parasitic capacitances, with respect to the equivalent bulk node. It permits the designer to realize higher bandwidths for a given current or even constant bandwidth with lower power consumption.

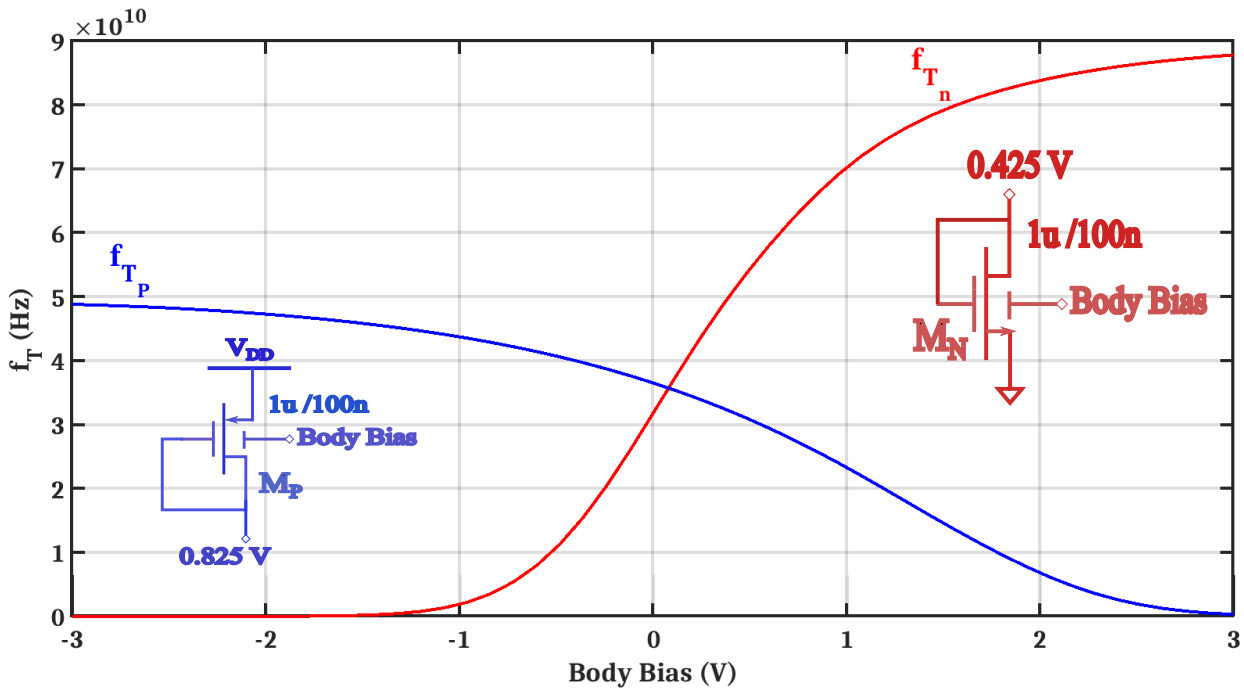

Fig. 2.10: The unity current gain frequency of the NMOS/PMOS flipped-well transistor $f_{T_{n,p}}$ against Body Bias in range from -3 V to 3 V at $V_{DD} = 1.5\ V$.

Fig. 2.10 shows the unity current gain frequency of the NMOS/PMOS flipped-well transistors $f_{T_{n,p}}$ against Body Bias in range from -3 V to 3 V at $V_{DD} = 1.5\ V$. It shows that the unity current gain frequency $f_{T_{n,p}}$ can significantly change and reach 90 GHz. We simulate this figure using the width per finger W_f equals to 1 µm, the length per finger L_f equals to 100 nm and number of fingers $N_{fingers}$ equals to 1.0.

2.5.2 Analog/RF design examples

Reducing the $V_{TH_{n,p}}$ through the body biasing is shown by the design of CMOS switches, in [Kumar17]. In Fig. 2.11, the small flat behavior of the CMOS switch resistance using the body biasing produces a small switch with a compact layout as well as a low parasitic capacitance. This design example can be utilized in the high-performance data converters and other switched-capacitor circuits.

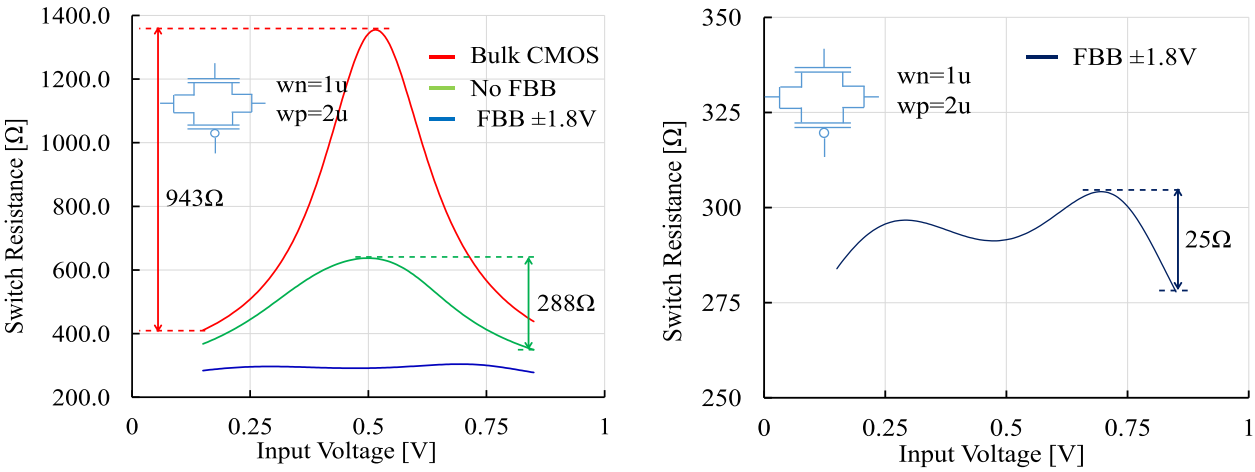

Fig. 2.11: Switch resistance variation across whole input voltage range [Kumar17].

In [Mas17], the analog compensation of the bandwidth mismatch, by tuning the body bias of a bootstrap circuit of Fig. 2.12, improves the spurious-free dynamic range (SFDR) from 44.73 dB to 85.9 dB at 2 GHz sine-wave input using the sampling frequency, $f_s = 4\ GHz$, as presented in Fig. 2.13.

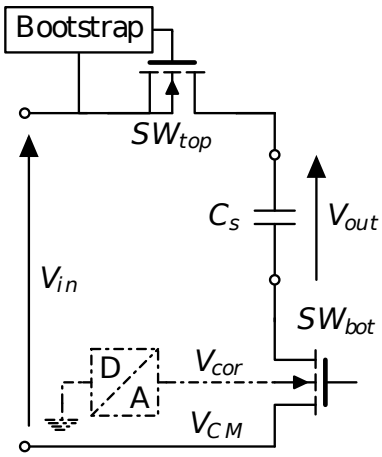

Fig. 2.12: Proposed Bandwidth Correction [Mas17].

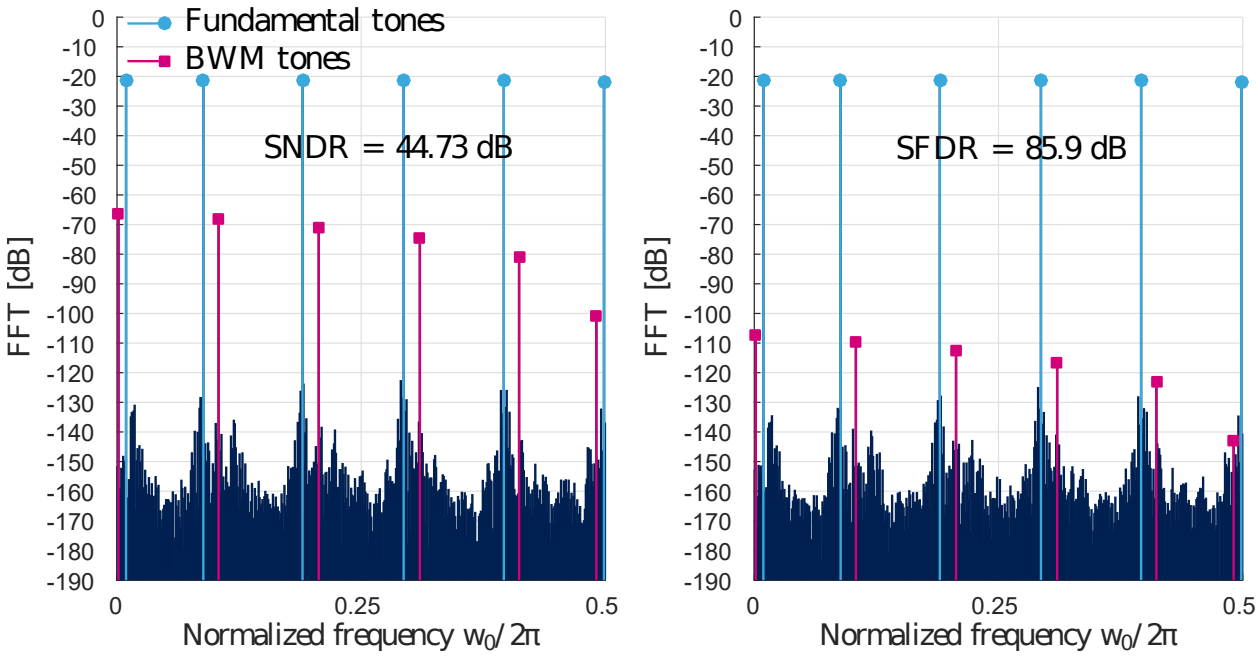

Fig. 2.13: Output spectrum with a multitone input before and after a 6-b DAC correction [Mas17].

A new technique consists of generating and making available on chip body-bias voltages variable over time, process, voltage, and temperature (PVT) variations. We can decrease system-level PVT variations by continuously tuning the threshold voltage $V_{TH_{n,p}}$ as in the design examples of [Lechevallier15], [Fanori15], [Danilovic16], [Sourikopoulos16] and [Streel17].

The technology enables flexible and energy efficient silicon on chip solutions for multiple types of applications in the field of internet of things (IoT) and 5G [Zimmer16].

2.5.3 The selective devices used in the design of both CT BP $\Sigma\Delta$ Modulators

The flipped-well transistors with low threshold voltage flavour (LVT), using $V_{DD} = 1.5\ V$ and minimum transistor length $L_{min} = 100\ nm$, are selected for both CT BP $\Sigma\Delta$ Modulators designs because our RF operation frequency is below 10 GHz [Cathelin17]. Using forward body bias tuning for decreasing the threshold voltage $V_{TH_{n,p}}$, we achieve a good output swing

with an optimized power consumption for the operational amplifiers as discussed in chapter 4 at section 4.3.2.

The used resistors in our designs are the poly high precision non silicided resistor that has the maximum sheet resistance value (Ω/sq) with a maximum absolute resistor error that can reach 15.8 %.

We used both of the MOM capacitor and the varactor in the capacitors implementations of both two types of resonators as discussed in chapter 4 at section 4.3.1 and in chapter 5 at section 5.4.1. We avoid using the P-Well/N-Well capacitors as they aren't accurate with the possible process corners of capacitance C_{MIN} and C_{MAX}. The used model of the MOM capacitor has a minimum value of capacitance $\approx 6\ fF$.

2.6 Thermal-noise analysis in CT $\Sigma\Delta$ Modulators

The signal to noise ratio (SNR) and in-band thermal noise of CT $\Sigma\Delta$ modulators based on active-RC resonators are important design parameters.

Most of the prior thermal-noise analyses of CT $\Sigma\Delta$ modulators are related to low-pass CT $\Sigma\Delta$ modulators. The thermal-noise behaviour of BP CT $\Sigma\Delta$ modulators are not discussed and studied in-details before.

The study of [Lamarre06] computes the integrator's capacitor from the requirements of overall signal to noise ratio (SNR) of the modulator. The used topology consists of a 5th-order loop filter, a 4-bit ADC, a DAC with data weighted averaging (DWA) compensation and an additional feedback coefficient to compensate the loop delay [Benabes97]. The 5th-order loop filter is composed of an integrator in-series with two 2-op-amp resonators. The $\Sigma\Delta$ coefficients are first scaled using the algorithm of [Beilleau03] in order to limit the integrators output below the saturation level. For stability consideration, it is suitable to have a rather small output swing [Philips04]. The analytical expression of the transfer functions based on the 5th-order linearized feedback CT LP $\Sigma\Delta$ modulator, from the input noise source of each integrator to the modulator output, are derived in-band and referred to the input of $\Sigma\Delta$ modulator. It shows that when the integrator is nearer to the quantizer, its noise is stronger

attenuated by the loop. The noise of the first integrator is not shaped by the converter, so it is dominant on the overall noise. The 2nd and the 3rd integrator noise can be moved out of the $\Sigma\Delta$ bandwidth when the over sampling ratio (OSR) is doubled or maximizing a little-bit the gain of integrator.

In [Pavan14], the suggested technique was demonstrated on the normalized third order cascaded-of-integrator feed-forward (CIFF) CT lowpass $\Sigma\Delta$ modulator where both the sampling rate and the input resistance of the modulator are 1 Hz and 1 Ω, respectively. It utilizes in particular both the two-stage Miller compensated op-amps and the switched capacitor feedback DACs.

The technique describing the thermal-noise behaviour of [Pavan14] considered a linear periodically time varying (LPTV) system. The output sequence of interest $v_{out}[n]$ is obtained by sampling the output $v_{out}(t)$ in number of points N with a period time $T_s = 1/f_s$ and a timing offset t_o.

Both of the signal transfer function (STF), the noise transfer function (NTF) and the normalized noise spectral density from the various noise sources of each integrator with the summing amplifier are computed with this technique and well-matched with the results of the periodic steady state analysis simulation. It proves that the first integrator's noise, that includes the input resistor and feedback DAC, contributes most of noise in the signal band.

This technique [Pavan14] can't be a generic one because it is based on the two-stage Miller compensated op-amps topology and only switched-cap feedback DACs. In our proposed approximate thermal-noise study presented in chapter 3, we neglect the thermal-noise contributed by both of the op-amps and the feedback DACs to be a generic analysis and valid for any circuit-level design of CT BP $\Sigma\Delta$ modulator using two-op-amp resonators. Our method can be applied on a different system-level architecture or with a different order of $\Sigma\Delta$ modulator.

Besides, normalizing the analysis [Pavan14] doesn't take into consideration any limitations of the signal swing allowable by the op-amps implementing the integrators. Although, we proved that scaling the integrators by an integrator gain A has a great influence on the in-band thermal-noise at the input of CT BP $\Sigma\Delta$ modulator based on two-op-amp resonators.

The technique of [Pavan14] was verified against the macro-model implementation using only the periodic steady state analysis in a circuit simulator such as PSS, PNOISE. Normally, we trust in the noise transient analysis for measuring the performance of $\Sigma\Delta$ modulators, consequently we had to validate our approximate thermal-noise study with the macro-model implementation using the lengthy noise transient analysis simulation of a circuit simulator. The discussions on previous thermal-noise analyses are related to low-pass CT $\Sigma\Delta$ modulators. Later in the chapter 3, we present in-details an approximate study of the thermal noise behaviour for the 4th-order CT BP $\Sigma\Delta$ modulator based on two-op-amp resonators. We take into consideration the effect of both integrator resistor R and integrator gain A. This study helps the designer to select the proper values for both of them at a given SNR. Our approximate thermal-noise analysis agrees with the noise transient analysis simulation of the macro-model implementation with a small error ≤ 2.5 %.

2.7 Conclusion

In this chapter, we discuss the basic concepts about $\Sigma\Delta$ modulators such as oversampling ADC, continuous-time $\Sigma\Delta$ modulator and bandpass $\Sigma\Delta$ modulator. Then, we showed the previous designs of BP CT $\Sigma\Delta$ modulators based on both of the two-op-amp resonators and the one-op-amp resonators. After that, we introduced the fully depleted silicon on insulator FD-SOI technology. We focused on explaining the characteristics of the low threshold voltage "flipped-well" devices as they are employed in our $\Sigma\Delta$ modulators designs. The type of devices used in our designs "transistors, resistors and capacitors" are presented. At the end, we discussed the previous work on thermal-noise analyses for CT $\Sigma\Delta$ modulators which were dedicated to low-pass $\Sigma\Delta$ modulators only.

Chapter 3

A system-level study of "4th-order CT BP two-op-amp resonator $\Sigma\Delta$ modulator"

3.1 Introduction

In this chapter, we present a system-level study of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator.

First in section 3.2, we present the scaling method of the coefficients for the modulator. Second in section 3.3, we show the approximate linear model of the 4th-order CT BP $\Sigma\Delta$ modulator. Third in section 3.4, we compute the input-referred thermal-noise power of the integrators. In addition to, the influence of integrator resistor "R" and integrator gain "A" on the input-referred thermal-noise power of the modulator is analysed, in section 3.5. Also, we show the op-amps DC-gain "A_0" effect on both the quality factor "Q" and the resonance frequency "f_0" of the 2-op-amp resonator along with the SNR of the modulator, in section 3.6. At the end, the integrators gain A influence on the quality factor of the 2-op-amp resonator is presented using the mathematical model and compared with the transistor-level implementation simulation results, in section 3.7.

3.2 The scaling method of the coefficients for the modulator

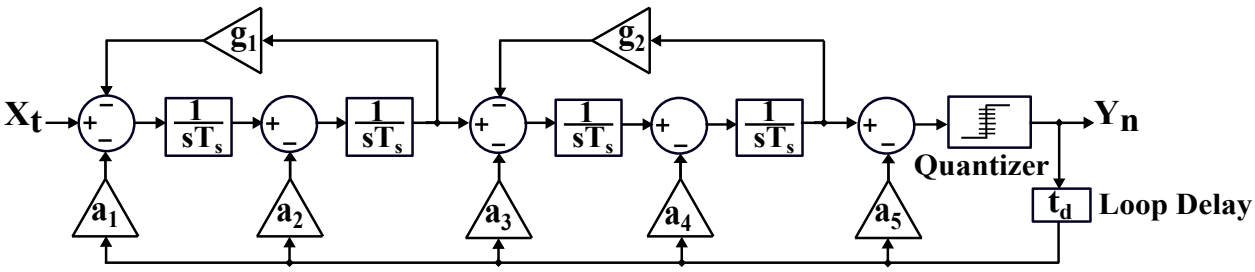

Fig. 3.1: A 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using a two-op-amp resonator before-scaling.

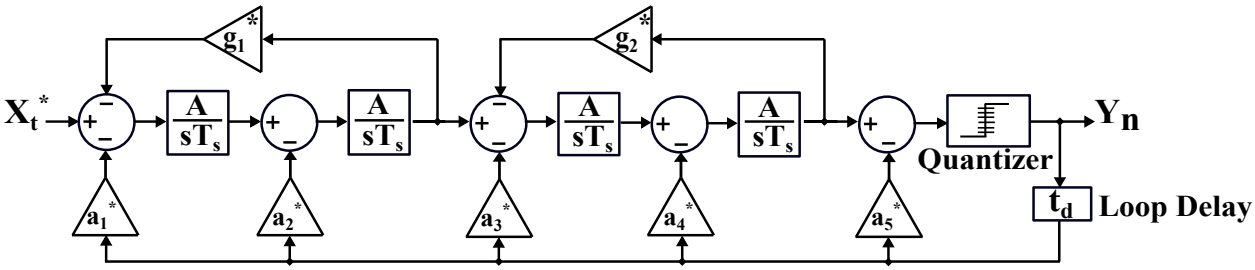

Fig. 3.2: A 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using a two-op-amp resonator after-scaling.

The continuous-time band-pass $\Sigma\Delta$ modulators, designed using [Aboushady04], have feedback coefficients and unity-gain integrators, which do not consider any circuit limitations. Fig. 3.1 shows the block diagram of a 4th-order BP CT $\Sigma\Delta$ modulator using two-op-amp resonators before scaling both of the feedback coefficients and the gain of integrators.

The feedback coefficients and the gain of integrators should be scaled to guarantee that the integrators outputs are bounded by the limited signal swing of the op-amps implementing the integrators [Beilleau03]. The integrators output swing cannot be predicted at the system-level but can be estimated by simulations from the transistor-level implementation of the $\Sigma\Delta$ modulator.

The gain of integrators are minimized from 1.0 to A, where $A < 1$. As well as, the feedback

coefficients are scaled from the original values a_1, a_2, a_3, a_4, a_5, g_1 and g_2 to the scaled values $a_1{}^*$, $a_2{}^*$, $a_3{}^*$, $a_4{}^*$, $a_5{}^*$, $g_1{}^*$ and $g_2{}^*$ as shown in Fig. 3.2. The input signal should also be converted from X_t to $X_t{}^*$ to have the same signal to quantization noise ratio (SNR_Q) as measured before scaling.

The scaled values of $a_1{}^*$, $a_2{}^*$, $a_3{}^*$, $a_4{}^*$, $a_5{}^*$, $g_1{}^*$, $g_2{}^*$ and $X_t{}^*$, as functions of the original values a_1, a_2, a_3, a_4, a_5, g_1, g_2 and X_t, respectively, are introduced in Table 3.1, where I_{scale} is a dimensionless parameter to scale all the feedback coefficients so that they can be realizable in the transistor-level implementation.

To validate our proposed scaling technique, as shown in Fig. 3.3, we present the output spectrum of the ideal model for two 4th-order CT BP $\Sigma\Delta$ modulators simulated by MATLAB. The 1st CT BP $\Sigma\Delta$ modulator is based on the non-scaled model, illustrated in Fig. 3.1 (blue), and the 2nd CT BP $\Sigma\Delta$ modulator is based on the scaled model, illustrated in Fig. 3.2 (red).

Both $\Sigma\Delta$ modulators are centered at $f_0 = 400$ MHz, they have a sampling frequency $f_s = 4\ f_0$ and a loop-delay $t_d = 1.5\ T_s$. These MATLAB simulations measure the maximum signal to quantization ratio (SNR_Q) of 70.1 dB for the 1st non-scaled CT BP $\Sigma\Delta$ modulator, and a 69.4 dB for the 2nd scaled CT BP $\Sigma\Delta$ modulator, both for an OSR of 64. In this example, the values of A, I_{scale} are equal to 0.75, 0.002, respectively.

Table 3.1: the scaled feedback coefficients and input signal for 4th-order CT BP $\Sigma\Delta$ modulator of Fig.3.2, at $A = 0.75$ and $I_{scale} = 0.002$.

after scaling	before scaling
${X_t}^* = (X_t \cdot I_{scale})/a_1$	X_t = - 6.8 dB
${a_1}^* = I_{scale}$	$a_1 = 0.584$
${a_2}^* = (a_2 \cdot I_{scale} \cdot A)/a_1$	$a_2 = 0.0$
${a_3}^* = (\mathrm{a}_3 \cdot I_{scale} \cdot A^2)/a_1$	a_3 = - 0.1453
${a_4}^* = (a_4 \cdot I_{scale} \cdot A^3)/a_1$	a_4 = - 0.86
${a_5}^* = (a_5 \cdot I_{scale} \cdot A^4)/a_1$	a_5 = - 0.3714
${g_1}^* = g_1/A^2$	$g_1 = (1.56)^2$
${g_2}^* = g_2/\mathrm{A}^2$	$g_2 = (1.585)^2$

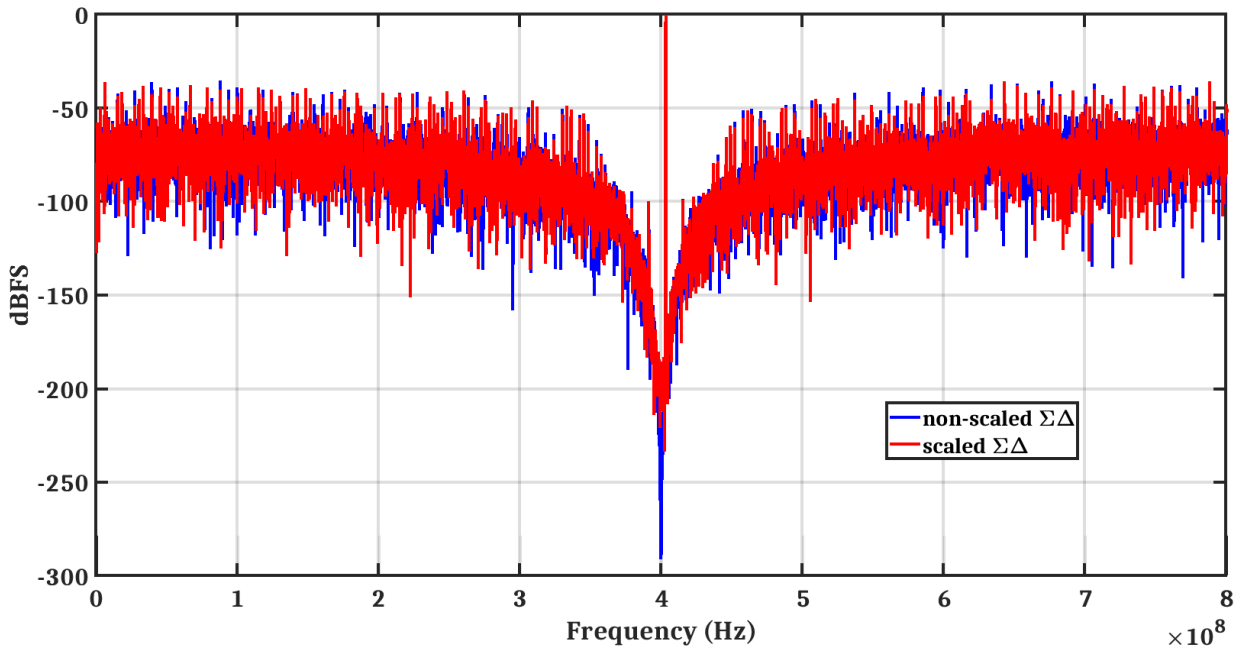

Fig. 3.3: The output spectrum of the ideal model for two 4th-order continuous-time bandpass $\Sigma\Delta$ modulator: the non-scaled in Fig. 3.1 (in blue), the scaled in Fig. 3.2 (in red), simulated by MATLAB.

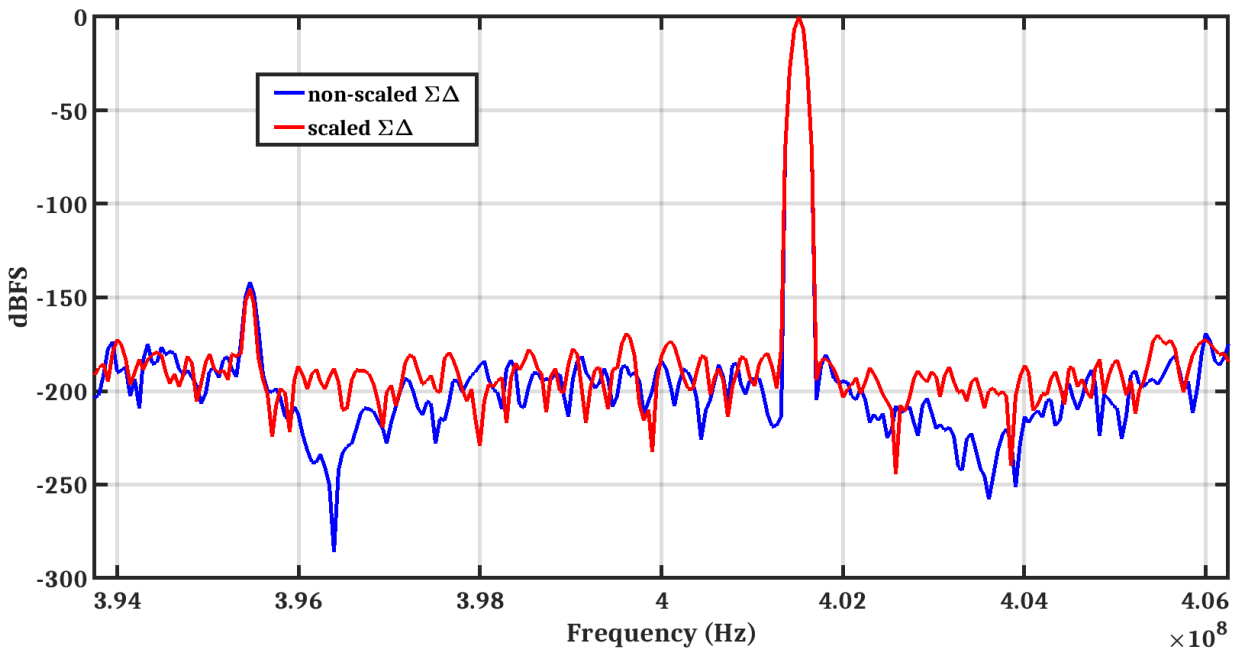

Fig. 3.4: The output spectrum of the ideal model for two 4th-order continuous-time bandpass $\Sigma\Delta$ modulator: the non-scaled in Fig. 3.1 (in blue), the scaled in Fig. 3.2 (in red), simulated by MATLAB, in the bandwidth of $\Sigma\Delta$ modulator, from 393.75 MHz to 406.25 MHz.

In Fig. 3.4, we show the output spectrum of the ideal model for two 4th-order CT BP $\Sigma\Delta$ modulators simulated by MATLAB, in the bandwidth of $\Sigma\Delta$ modulator. Where the bandwidth of $\Sigma\Delta$ modulator is from f_0 - $\frac{BW_{\Sigma\Delta}}{2}$ to f_0 + $\frac{BW_{\Sigma\Delta}}{2}$ where $BW_{\Sigma\Delta}$ equals to $\frac{f_s}{2 * OSR}$, f_s = 1.6 GHz and OSR = 64. Therefore, the bandwidth of $\Sigma\Delta$ becomes in the range from 393.75 MHz to 406.25 MHz.

3.3 Approximate linear model of CT BP $\Sigma\Delta$ modulator

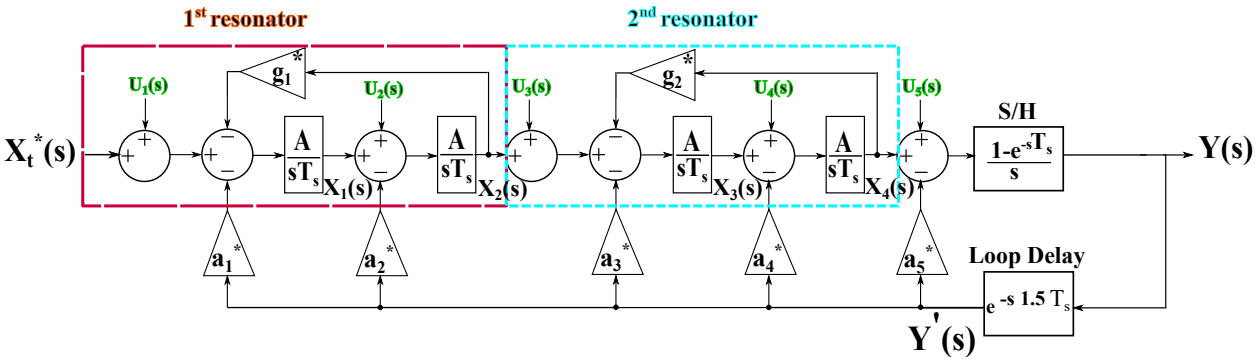

Fig. 3.5: Approximate linear model of a 4th-order continuous-time bandpass $\Sigma\Delta$ modulator including integrators noise sources.

Fig. 3.5 shows the approximate linear model of the 4th-order continuous-time band-pass $\Sigma\Delta$ modulator. where the U_i is the equivalent noise source at the input of each integration stage. The noise contributed by the quantizer is ignored, because it has a neglected influence on the overall $\Sigma\Delta$ modulator input noise compared to the thermal noise of integration stages as later shown. In addition to, removing the quantizer leads to linearize the model of 4th-order continuous-time band-pass $\Sigma\Delta$ modulator. The equations representing the approximate linear model of CT BP $\Sigma\Delta$ modulator of Fig. 3.5 can be written as:

$$X_1(s) = \frac{A}{sT_s}\{\{X_t{}^*(s) + U_1(s)\} - Y^{'}(s) \cdot a_1{}^* - X_2(s) \cdot g_1{}^*\} \tag{3.1}$$

$$X_2(s) = \frac{A}{sT_s}\{\{X_1(s) + U_2(s)\} - Y^{'}(s) \cdot a_2{}^*\} \tag{3.2}$$

$$X_3(s) = \frac{A}{sT_s}\{\{X_2(s) + U_3(s)\} - Y^{'}(s) \cdot a_3{}^* - X_4(s) \cdot g_2{}^*\} \tag{3.3}$$

$$X_4(s) = \frac{A}{sT_s}\{\{X_3(s) + U_4(s)\} - Y^{'}(s) \cdot a_4{}^*\} \tag{3.4}$$

$$Y^{'}(s) = e^{(-1.5\ \cdot\ sT_s)} \cdot Y(s) \tag{3.5}$$

$$Y(s) = \frac{1 - e^{-sT_s}}{s}\{\{X_4(s) + U_5(s)\} - Y^{'}(s) \cdot a_5{}^*\} \tag{3.6}$$

From these equations, the transfer function, $H_1(s)$, from the modulator input, ${X_t}^*(s)$, to the modulator output, $Y(s)$, is written as following:

$$H_1(s) = \frac{Y(s)}{{X_t}^*(s)} \tag{3.7}$$

While the transfer function, $H_i(s)$, from the equivalent noise source, $U_i(s)$, to the modulator output, $Y(s)$, can be derived as following:

$$H_i(s) = \frac{Y(s)}{U_i(s)} \tag{3.8}$$

Then, the transfer functions, $H_{i1}(s)$, are computed when the transfer functions of $H_i(s)$ are referred to the modulator input, ${X_t}^*(s)$, written as following:

$$H_{i1}(s) = \frac{H_i(s)}{H_1(s)} \tag{3.9}$$

$$H_{11}(s) = \frac{H_1(s)}{H_1(s)} = 1 \tag{3.10}$$

$$H_{21}(s) = \frac{H_2(s)}{H_1(s)} \tag{3.11}$$

$$H_{31}(s) = \frac{H_3(s)}{H_1(s)} \tag{3.12}$$

$$H_{41}(s) = \frac{H_4(s)}{H_1(s)} \tag{3.13}$$

$$H_{51}(s) = \frac{H_5(s)}{H_1(s)} \tag{3.14}$$

In Fig. 3.6, the magnitude of the transfer functions, $H_{11}(s)$, $H_{21}(s)$, $H_{31}(s)$, $H_{41}(s)$ and $H_{51}(s)$, are computed at $f_0 = 400$ MHz, a sampling frequency, $f_s = 4\ f_0$ and a loop-delay, $t_d = 1.5\ T_s$ at $OSR = 64$. These transfer functions are plotted versus the frequency, from 0 to ($f_s/2 = 800$ MHz). The values of A, I_{scale} are equal to 0.75, $60 \cdot 10^{-6}$, respectively, the same values as exploited later in the transistor-level implementation. The values of the feedback coefficients in the approximate linear model of Fig.3.5 are shown in table 3.2.

Fig. 3.7 presents these transfer functions (of Fig. 3.6) versus the frequency, in the bandwidth of $\Sigma\Delta$ from 393.75 MHz to 406.25 MHz.

Table 3.2: The values of the feedback coefficients in the approximate linear model of CT BP $\Sigma\Delta$ modulator in Fig. 3.5, at $A = 0.75$ and $I_{scale} = 60 \cdot 10^{-6}$.

after scaling
${a_1}^* = 60 \cdot 10^{-6}$
${a_2}^* = 0$
${a_3}^* = -9 \cdot 10^{-6}$
${a_4}^* = -38 \cdot 10^{-6}$
${a_5}^* = -12 \cdot 10^{-6}$
${g_1}^* = (2.08)^2$
${g_2}^* = (2.113)^2$

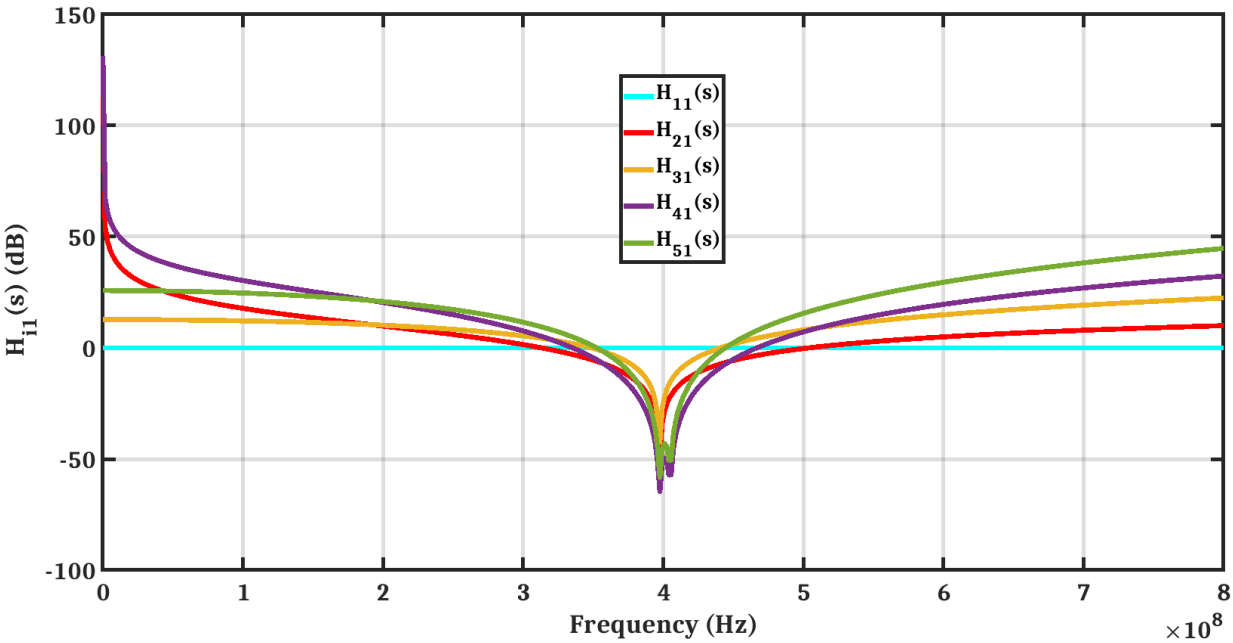

Fig. 3.6: the magnitude of the transfer functions, $H_{11}(s)$, $H_{21}(s)$, $H_{31}(s)$, $H_{41}(s)$ and $H_{51}(s)$, are plotted versus the frequency, from 0 to ($f_s/2 = 800$ MHz).

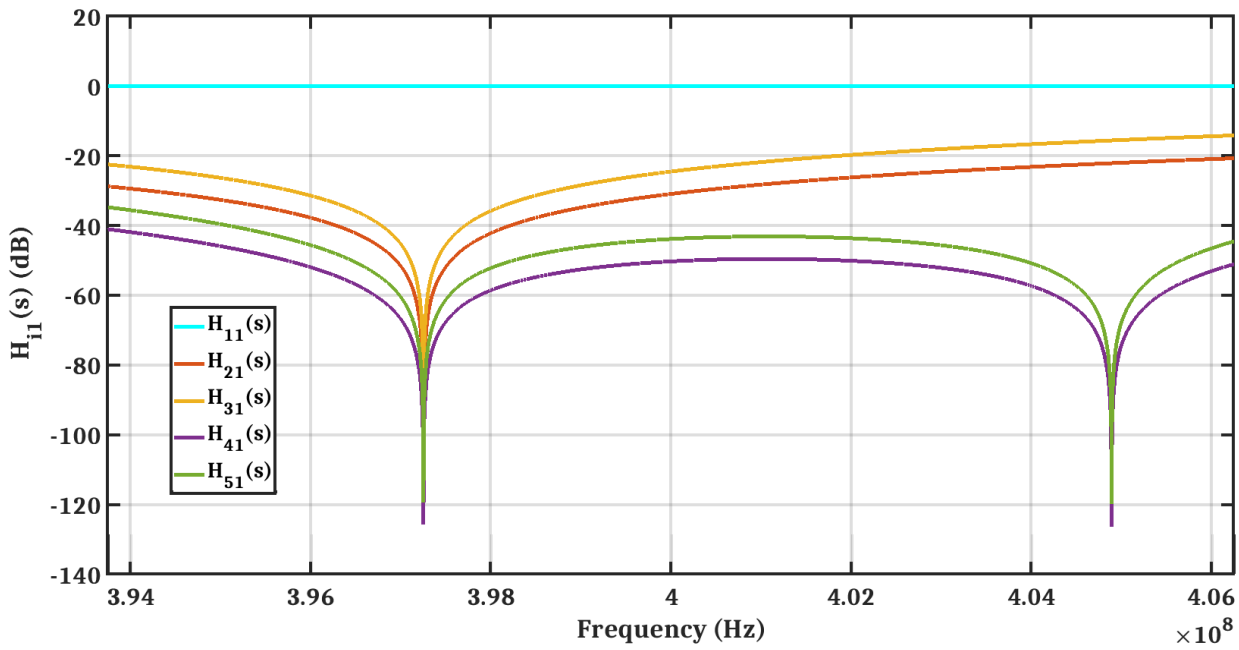

Fig. 3.7: the magnitude of the transfer functions, $H_{11}(s)$, $H_{21}(s)$, $H_{31}(s)$, $H_{41}(s)$ and $H_{51}(s)$, are plotted versus the frequency, in the bandwidth of $\Sigma\Delta$ from 393.75 MHz to 406.25 MHz.

The input-referred in-band noise power of the modulator, $\overline{V_{n,\Sigma\Delta}}^2$, is calculated as it follows:

$$\overline{V_{n,\Sigma\Delta}}^2 = \sum_{i=1}^{5} \int_{f_0 - \frac{BW_{\Sigma\Delta}}{2}}^{f_0 + \frac{BW_{\Sigma\Delta}}{2}} \overline{U_i(s)}^2 \cdot \mid H_{i1}(s)^2 \mid \, df \tag{3.15}$$

where,

$$BW_{\Sigma\Delta} = \frac{f_s}{2 \ * \ OSR} \tag{3.16}$$

It is obvious that the input noise source $U_1(s)$ is not shaped, as well as it contributes the most in the input-referred in-band noise power of the modulator, $\overline{V_{n,\Sigma\Delta}}^2$. It shows clearly that the input noise source $U_3(s)$ is highly affected on the input-referred in-band noise power of the modulator, $\overline{V_{n,\Sigma\Delta}}^2$, more than input noise sources $U_{2,\ 4,\ 5}(s)$

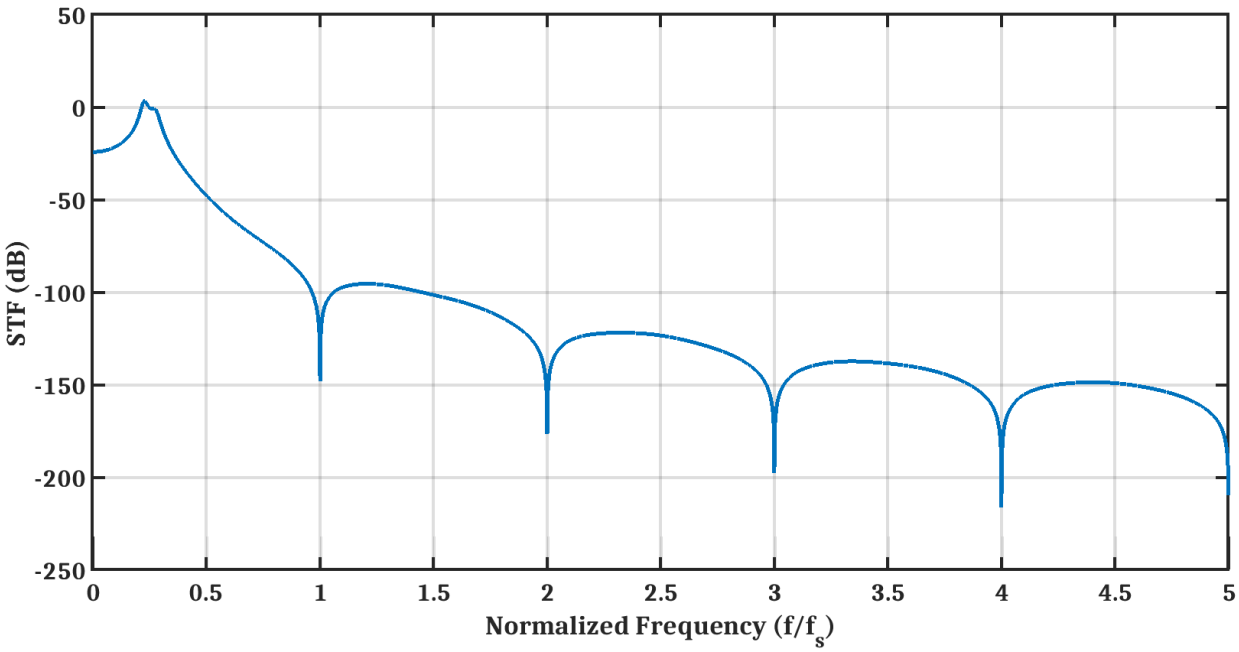

Fig. 3.8: the magnitude of the signal transfer function (STF), $H_1(s)$, is plotted versus the normalized frequency (f/f_s), at integrator gain A = 0.75.

Fig 3.8 shows the magnitude of the signal transfer function (STF), $H_1(s)$, is plotted versus the normalized frequency (f/f_s), at integrator gain A = 0.75. It has both an inherent selectivity filter and an inherent anti-aliasing filter, which leads to be more robust against out-of-band blockers.

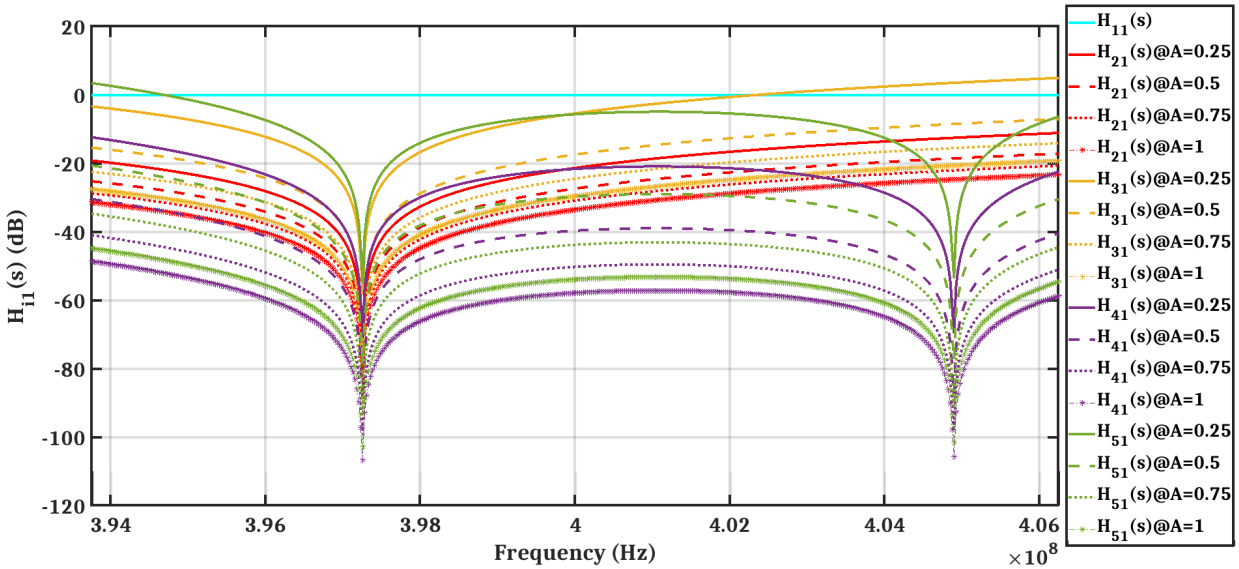

Fig. 3.9: the magnitude of the transfer functions, $H_{11}(s)$, $H_{21}(s)$, $H_{31}(s)$, $H_{41}(s)$ and $H_{51}(s)$, are plotted versus the frequency, in the bandwidth of $\Sigma\Delta$ from 393.75 MHz to 406.25 MHz, at integrator gain A = 0.25, 0.5, 0.75, 1.

Fig. 3.9 presents the transfer functions (of Fig. 3.6) versus the frequency, in the bandwidth of $\Sigma\Delta$ from 393.75 MHz to 406.25 MHz, at integrator gain A = 0.25, 0.5, 0.75, 1.
Fig 3.9 proves that the input noise sources $U_{2,\ 3,\ 4,\ 5}(s)$ contribute less on the input-referred in-band noise power of the modulator, $\overline{V_{n,\Sigma\Delta}}^2$, when integrator gain A is increasing.

3.4 The thermal-noise computation of integration stages in CT BP $\Sigma\Delta$ modulator

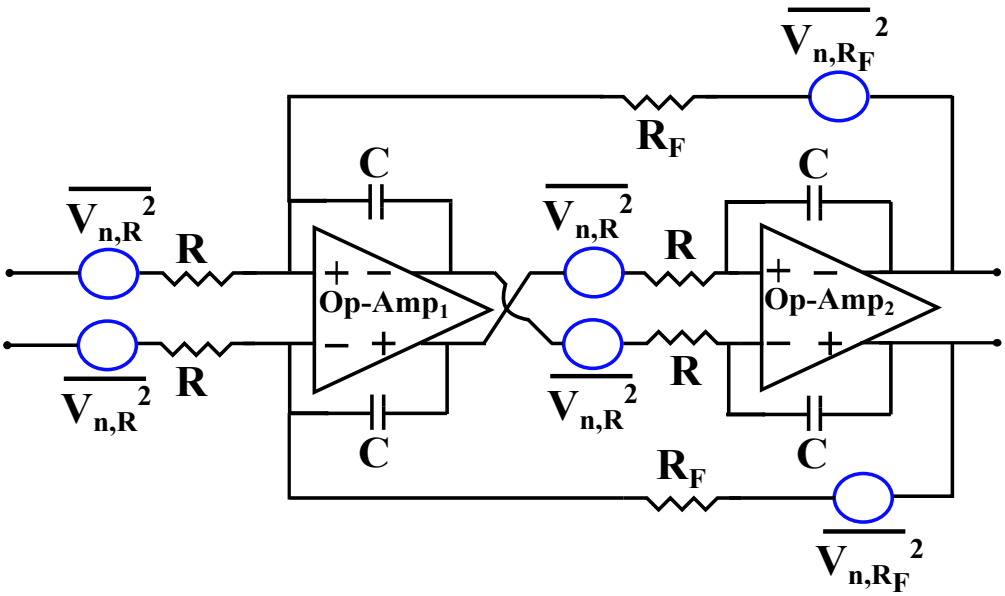

Fig. 3.10: Two-op-amp resonator circuit with the resistor thermal-noise sources.

Each resonator in Fig. 3.5, will be realized using a two-op-amp resonator with the resistor thermal-noise sources as shown in Fig. 3.10.

The thermal noise of the op-amps implementing the integration stages and the noise sources due to the current steering DACs feedback sources are neglected for simplicity.

We can deduce the equations of the noise power at the input of each integration stage, $\overline{U_1(s)}^2$, $\overline{U_2(s)}^2$, $\overline{U_3(s)}^2$, $\overline{U_4(s)}^2$, and $\overline{U_5(s)}^2$ in a relation of R and R_F, they are expressed by:

$$\overline{U_{1,\,3}(s)}^2 \;=\; 2\cdot\overline{V_{n,R}}^2 + 2\cdot\overline{V_{n,R_F}}^2\cdot\{\frac{R}{R_F}\}^2, \quad R_F \;=\; R\;\cdot\;\frac{1}{g_{1,2}{}^*} \tag{3.17}$$

$$\overline{U_{2,\,4,\,5}(s)}^2 \;=\; 2\cdot\overline{V_{n,R}}^2 \tag{3.18}$$

where,

$$\overline{V_{n,R}}^2 \;=\; 4\cdot k_B T\cdot R \quad , \quad \overline{V_{n,R_F}}^2 \;=\; 4\cdot k_B T\cdot R_F \tag{3.19}$$

k_B is the Boltzmann constant and T is the temperature.

The total thermal-noise power resulting from all integration stages in-band, $\overline{V_{n,\Sigma\Delta}}^2$, is computed referred to the $\Sigma\Delta$ modulator input, $X_t{}^*(s)$. It can be written as:

$$\begin{aligned}\overline{V_{n,\Sigma\Delta}}^2 = & \{ 8 \cdot k_B T \cdot R \cdot (1 + \frac{R}{R_F})\} \cdot \Sigma\Delta_{BW} \\ & + \{ 8 \cdot k_B T \cdot R \} \cdot \int_{f_0 - \frac{\Sigma\Delta_{BW}}{2}}^{f_0 + \frac{\Sigma\Delta_{BW}}{2}} \mid H_{21}(s)^2 \mid df \\ & + \{ 8 \cdot k_B T \cdot R \cdot (1 + \frac{R}{R_F})\} \cdot \int_{f_0 - \frac{\Sigma\Delta_{BW}}{2}}^{f_0 + \frac{\Sigma\Delta_{BW}}{2}} \mid H_{31}(s)^2 \mid df \\ & + \{ 8 \cdot k_B T \cdot R \} \cdot \int_{f_0 - \frac{\Sigma\Delta_{BW}}{2}}^{f_0 + \frac{\Sigma\Delta_{BW}}{2}} \mid H_{41}(s)^2 \mid df \\ & + \{ 8 \cdot k_B T \cdot R \} \cdot \int_{f_0 - \frac{\Sigma\Delta_{BW}}{2}}^{f_0 + \frac{\Sigma\Delta_{BW}}{2}} \mid H_{51}(s)^2 \mid df\end{aligned} \tag{3.20}$$

In order to verify Eq. 3.20, we implement a 4th-order continuous-time bandpass $\Sigma\Delta$ modulator presented in Fig. 3.2 using the macro-models. Fig. 3.11 shows, the signal to noise ratio (SNR) versus R computed using Eq. 3.20, the SNR versus R of the macro-model implementation of $\Sigma\Delta$ modulator simulated by a circuit simulator using a noise transient analysis (simulation results) with/without the thermal noise. The values of the feedback coefficients are presented before in table 3.2. The values of A, I_{scale} are equal to 0.75, $60 \cdot 10^{-6}$, respectively, the same values as exploited later in the transistor-level implementation.

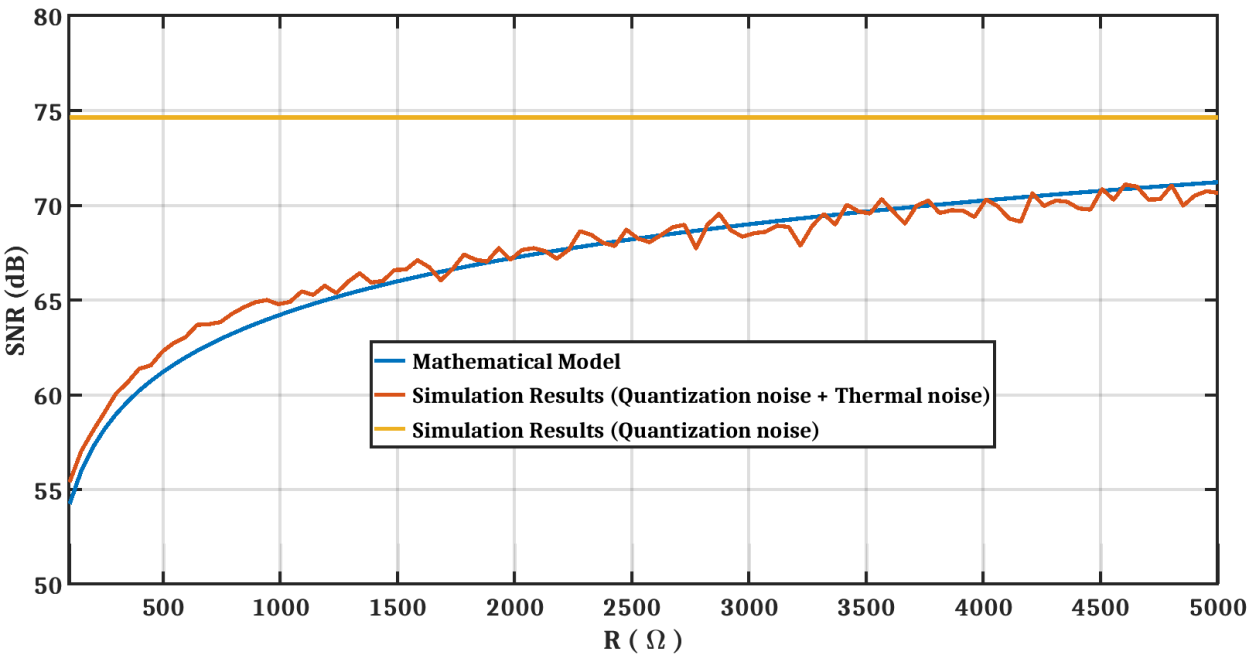

Fig. 3.11: The maximum SNR versus R, computed by Eq. 3.20 and the results with the quantization noise and (with/without) the thermal noise of a 4th-order continuous-time bandpass $\Sigma\Delta$ modulator in Fig. 3.2 using the macro-models simulated by a circuit simulator, taken into account Eq. 3.21.

Fig. 3.11 is measured at the amplitude of $\Sigma\Delta$ modulator input, $\{X_t{}^*(s)\}_{Amp}$, that is given by:

$$\{X_t{}^*(s)\}_{Amp} \;=\; (X_t \cdot I_{scale} \cdot R)/a_1 \;. \tag{3.21}$$

Fig. 3.12 shows the error of SNR, computed from Fig. 3.11, then SNR_{error} is expressed by.

$$SNR_{error}(\%) \;=\; 100\cdot \mid \frac{SNR_{\;Simulation\;\;Results} \;-\; SNR_{\;Eq.\;3.20}}{SNR_{\;Simulation\;\;Results}} \mid \tag{3.22}$$

Where $SNR_{\;Simulation\;\;Results}$ is measured with both of the quantization noise and the thermal noise of a 4th-order continuous-time bandpass $\Sigma\Delta$ modulator in Fig. 3.2 using the macro-models simulated by a circuit simulator.

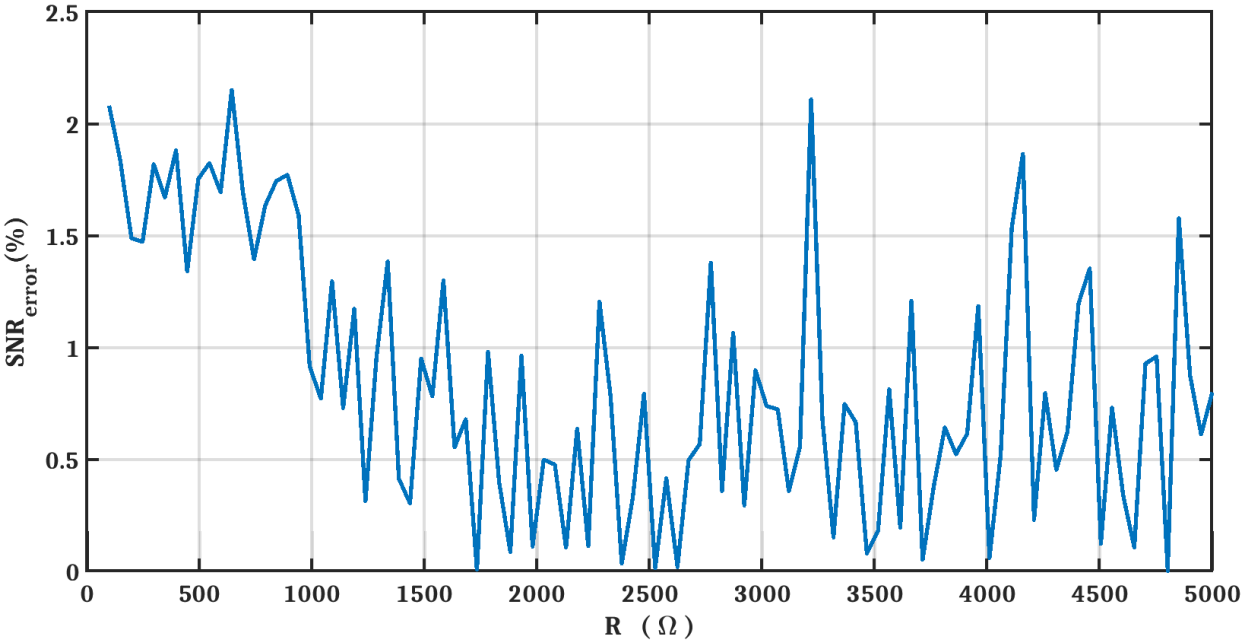

Fig. 3.12: The SNR_{error} versus R, computed by Eq. 3.22.

As illustrated in Fig. 3.11 and Fig. 3.12, Eq. 3.20 matches the noise transient analysis simulation results (simulation results with the quantization noise and the thermal noise) at an error ≤ 2.5 %. Furthermore, the noise transient analysis simulation presented in Fig. 3.11 lasts for two days, while the one simulated by Eq. 3.20 lasts for only four minutes.

In Fig. 3.11, the average of SNR simulated by transient analysis (simulation results with the quantization noise only) is ≈ 74.6 dB. It proves that the SNR is degraded due to the resistor thermal noise contributed by the integration stages and it is a little bit affected by the quantization noise, that validated and justified our assumption of ignoring the quantization noise.

3.5 The influence of integrator resistor "*R*" and integrator gain "*A*" on the total input-referred in-band thermal-noise power of CT BP $\Sigma\Delta$ modulator

We calculate the input-referred in-band thermal-noise power of the 1st integrator, using Eq. 3.23. Also, we compute the input-referred in-band thermal-noise power of the 3rd integrator, using Eq. 3.24.

$$\overline{V_{n,1^{st}\ integrator}}^2 = \{\ 8 \cdot k_B T \cdot R\ \cdot (\ 1\ +\ \frac{R}{R_F})\} \cdot\ \Sigma\Delta_{BW} \tag{3.23}$$

$$\overline{V_{n,3^{rd}\ integrator}}^2 = \{\ 8 \cdot k_B T \cdot R\ \cdot (\ 1\ +\ \frac{R}{R_F})\} \cdot \int_{f_0\ -\ \frac{\Sigma\Delta_{BW}}{2}}^{f_0\ +\ \frac{\Sigma\Delta_{BW}}{2}} \mid H_{31}(s)^2 \mid df \tag{3.24}$$

Fig. 3.13 shows the contribution in a percentage ratio of both the noise power of the 1st integrator using Eq. 3.23 and the noise power of the 3rd integrator using Eq. 3.24, in the overall input-referred in-band thermal-noise power, $\overline{V_{n,\Sigma\Delta}}^2$, that calculated by Eq. 3.20.
The values of the feedback coefficients in the approximate linear model of Fig. 3.5, for computing both the noise power of the 1st integrator, $\overline{V_{n,1^{st}\ integrator}}^2$, and the noise power of the 3rd integrator, $\overline{V_{n,3^{rd}\ integrator}}^2$, are shown in table 3.3.
Fig. 3.13 shows that the noise power of the 1st integrator dominates to the total in-band input-referred thermal-noise power, $\overline{V_{n,\Sigma\Delta}}^2$ at $A = 0.5$, 0.75, 1.
However, at $A = 0.25$, both of the noise power of the 1st integrator and the 3rd integrator are the significant. These observations are valid at any value of the integrator resistor, R.

Table 3.3: The values of the feedback coefficients in the approximate linear model of Fig. 3.5, for computing both the noise power of the 1st integrator, $\overline{V_{n,1^{st}\ integrator}}^2$, and the noise power of the 3rd integrator, $\overline{V_{n,3^{rd}\ integrator}}^2$, at $I_{scale} = 60 \cdot 10^{-6}$.

after scaling	before scaling
${a_1}^* = I_{scale}$	$a_1 = 0.584$
${a_2}^* = (a_2 \cdot I_{scale} \cdot A)/a_1$	$a_2 = 0.0$
${a_3}^* = (\mathrm{a}_3 \cdot I_{scale} \cdot A^2)/a_1$	$a_3 = -\ 0.1453$
${a_4}^* = (a_4 \cdot I_{scale} \cdot A^3)/a_1$	$a_4 = -\ 0.86$
${a_5}^* = (a_5 \cdot I_{scale} \cdot A^4)/a_1$	$a_5 = -\ 0.3714$
${g_1}^* = g_1/A^2$	$g_1 = (1.56)^2$
${g_2}^* = g_2/\mathrm{A}^2$	$g_2 = (1.585)^2$

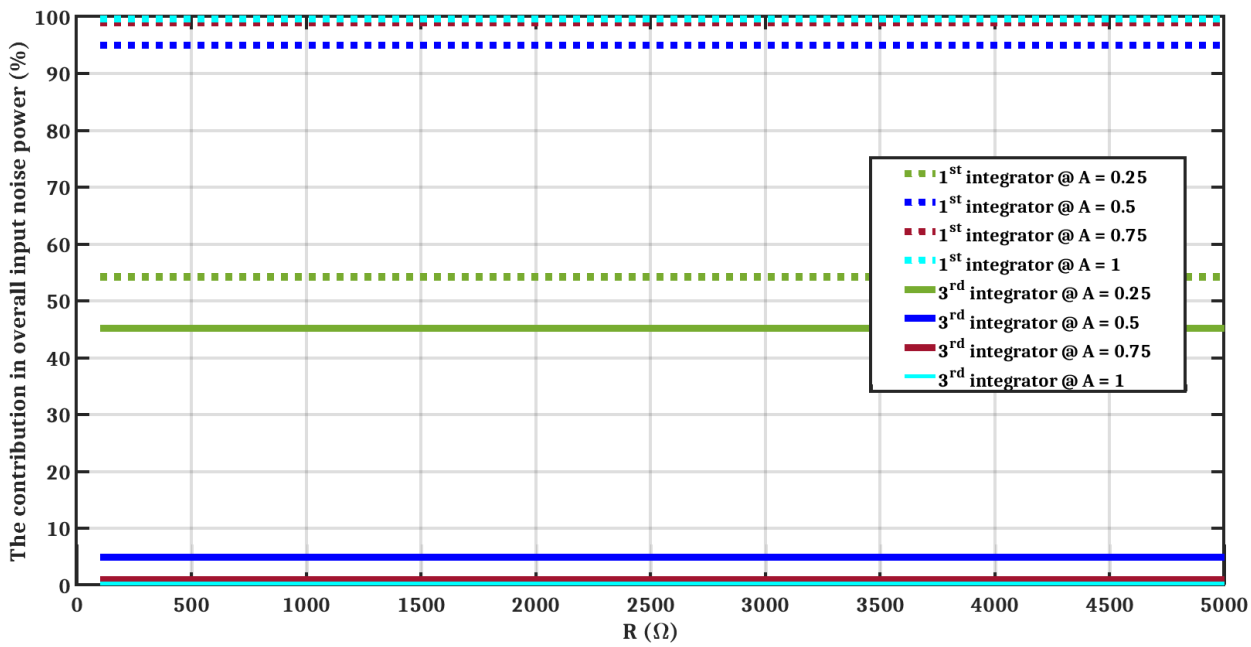

Fig. 3.13: the contribution in a percentage ratio of both the noise power of the 1st integrator using Eq. 3.23 and the noise power of 3rd integrator using Eq. 3.24, in the overall input-referred in-band thermal-noise power, $\overline{V_{n,\Sigma\Delta}}^2$, versus the integrator resistor, R, at integrator gain, A = 0.25, 0.5, 0.75, 1.

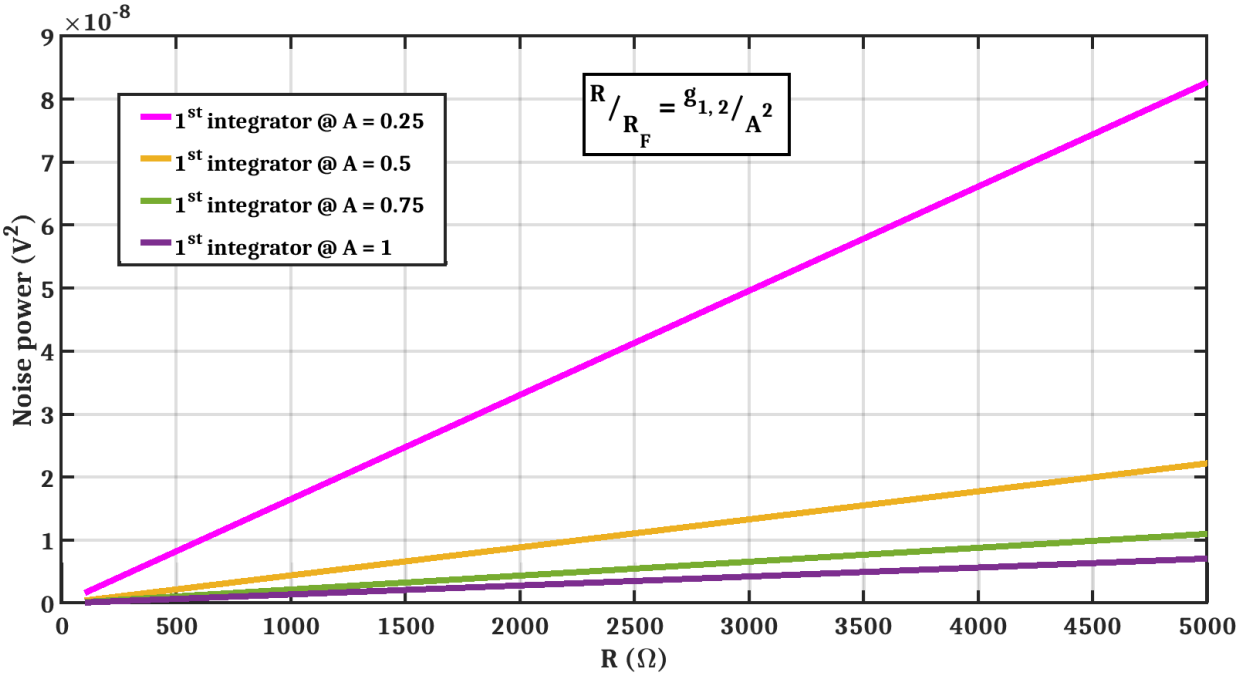

Fig. 3.14: The noise power of the 1st integrator versus the integrator resistor R at A = 0.25, 0.5, 0.75, 1, computed by Eq. 3.23.

Using Eq. 3.23, Fig. 3.14 demonstrates how the noise power of the 1st integrator change versus both of integrator resistor R in range of 100 Ω to 5000 Ω and the gain of integrator $A = 0.25, 0.5, 0.75, 1$.

It shows that the noise power of the 1st integrator decreases inversely with the gain of integrator, A, because the thermal noise from the resistor R_F decreases. And, it increases proportional with integrator resistor R.

Because we aim to achieve a SNR greater than 60 dB as well as the integrator gain A should be lower than 1, so we select the integrator gain $A = 0.75$. As well as we choose the integrator resistor R in a range of from 500 Ω to 1000 Ω to take into consideration moderate values of the integrator capacitor C which limits the unity gain frequency of op-amps, f_T. Besides, the designed op-amps as discussed later at this range of the integrator resistor R,

can provide the required swing.

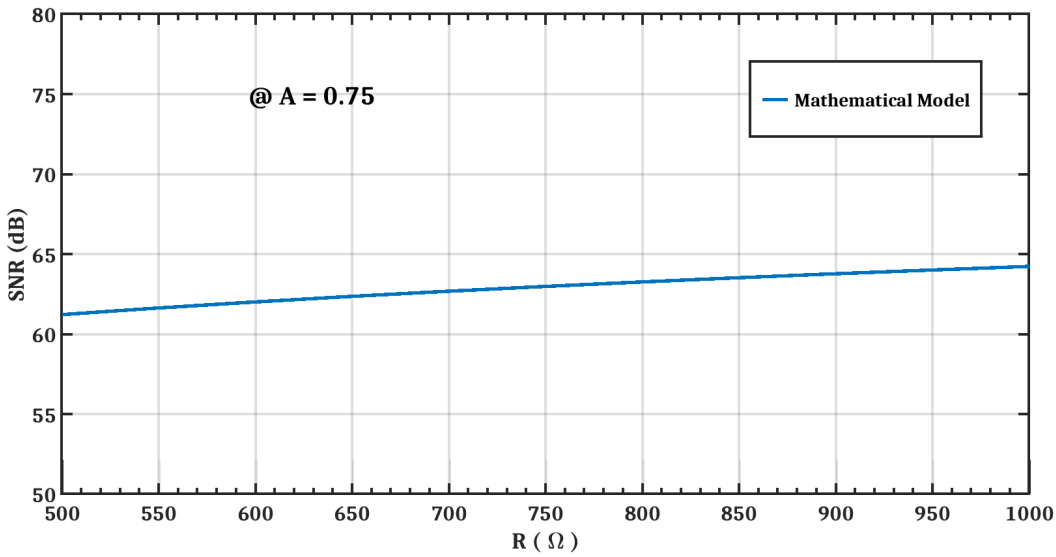

Fig. 3.15: The maximum SNR, computed by Eq. 3.20 taken from Fig. 3.11, versus integrator resistor R in a range of from 500 Ω to 1000 Ω at integrator gain $A = 0.75$.

Consequently at Fig. 3.15, we show the signal to noise ratio (SNR) versus integrator resistor R in a range of from 500 Ω to 1000 Ω at integrator gain $A = 0.75$, computed using Eq. 3.20. The values of the feedback coefficients are presented before in table 3.2. It is measured at the amplitude of $\Sigma\Delta$ modulator input, $\{X_t{}^*(s)\}_{Amp}$, that is given by Eq. 3.21.

3.6 The op-amps DC-gain "A_0"

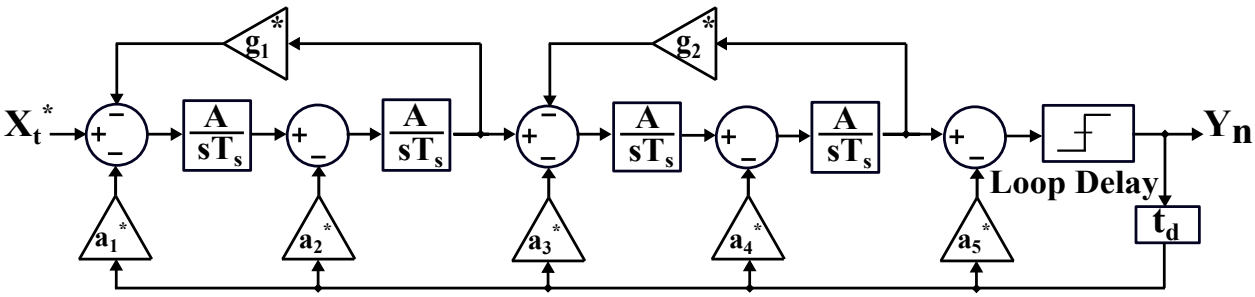

Fig. 3.16: A 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using a two-op-amp resonator.

Fig. 3.16 shows the block diagram of a 4th-order CT BP $\Sigma\Delta$ modulator using two-op-amp resonators. Each resonator is composed of two integrators with a feedback coefficient, $g_i{}^*$. Where i equals to 1, 2. The integrator gain is equal to $\frac{A}{T_s}$, where T_s is the sampling period and A is a factor used to adjust the op-amp output swing. The circuit realization of this resonator is shown in Fig. 3.17. Assuming a finite DC gain, A_0, and an infinite 1st pole, f_p, for the op-amp, the transfer function of the two-op-amp resonator at $A_0 \gg 1$, can be written as:

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{\frac{1}{(RC)^2}\cdot\frac{1}{1+\frac{2}{A_0}}}{s^2 + s.\frac{(R+2.R_F)}{(RC).R_F.(A_0+2)} + \frac{1}{R.C^2.R_F}\cdot\frac{1}{1+\frac{2}{A_0}}} \tag{3.25}$$

where, R, is the integrating resistor, C, the integrating capacitor and R_F the feedback resistor of the resonator.

By comparing the denominator of Eq. 3.25 to the denominator of a general resonator $s^2 + \frac{\omega_0}{Q}s + \omega_0^2$, we can show that the resonator quality factor, Q, is directly proportional to the op-amp finite DC-gain, A_0, while the centre frequency, f_0, is weakly affected by any variation in A_0.

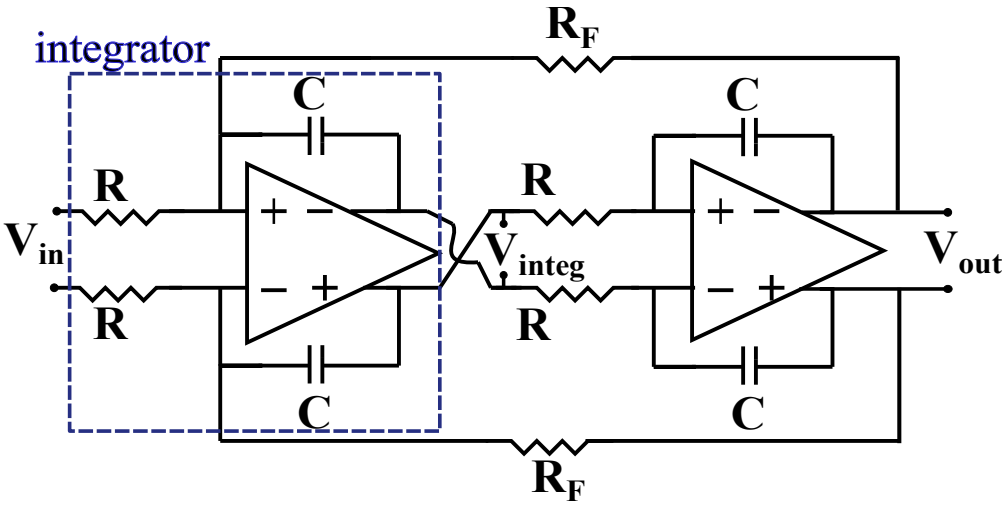

Fig. 3.17: The two-op-amp resonator circuit.

Similarly, assuming a finite DC gain, A_0, and an infinite 1st pole, f_p, for the op-amp, the transfer function of the integrator can be written as:

$$\frac{V_{integ}(s)}{V_{in}(s)} = \frac{1}{\frac{1}{A_0} + s.RC.(\frac{1}{A_0} + 1)} \tag{3.26}$$

Assuming $A_0 \gg 1$, Eq. 3.26 can be approximated to:

$$\frac{V_{integ}(s)}{V_{in}(s)} = \frac{1}{s.RC} \tag{3.27}$$

In order to design an integrator with a transfer function equal to $\frac{A}{sT_s}$, and for a sampling frequency, $f_s = \frac{1}{T_s}$, then the integrator RC product should be:

$$RC = \frac{1}{A.f_s} \tag{3.28}$$

From Eq. 3.25 and assuming that the resonator centre frequency, $f_0 = \frac{f_s}{4}$, we can then deduce the following relation for the feedback resistor of the resonator:

$$R_F = \frac{R}{g_{1,\ 2}{}^*} \cdot \frac{1}{(1 + \frac{2}{A_0})}, \qquad g_{1,2}{}^* = \frac{g_{1,\ 2}}{A^2} \tag{3.29}$$

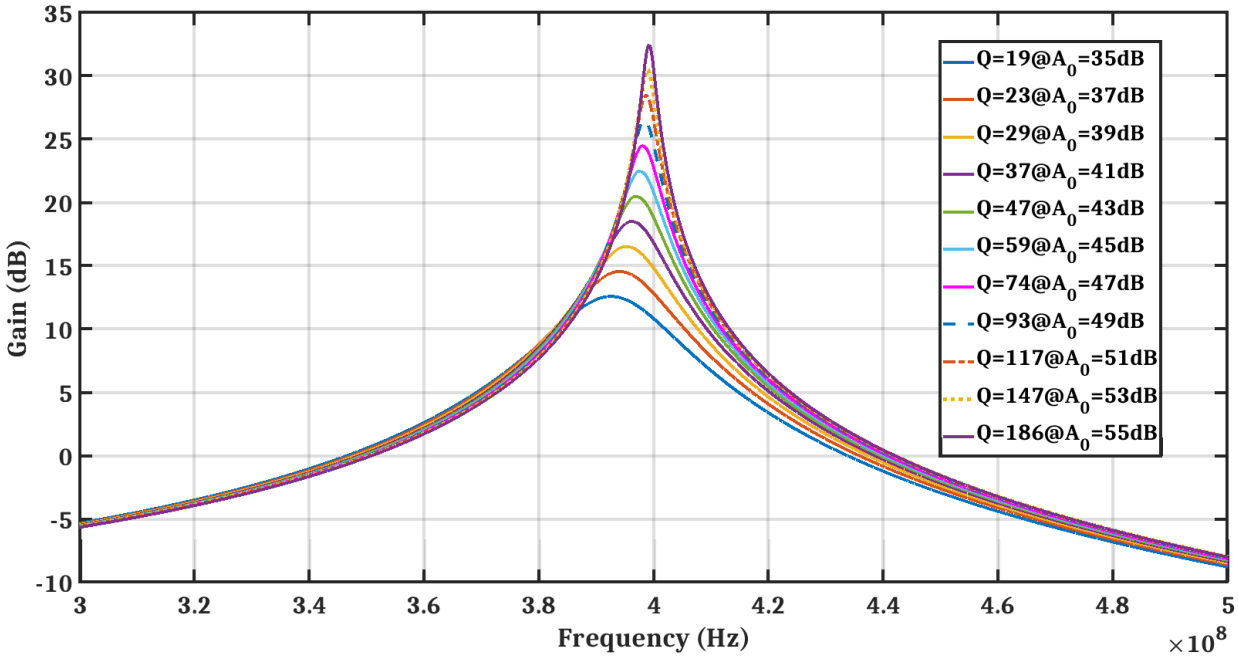

Fig. 3.18: The gain of a two-op-amp resonator (Eq.3.25) centered at $f_0 \approx 400$ MHz with op-amp DC gain, A_0, varying from 35 dB to 55 dB at a step of 2dB, at an infinite 1st pole, f_p.

At $f_0 = 400$ MHz, we selected the integrator gain $A = 0.75$ and the integrator resistor $R = 677\ \Omega$ from Fig. 3.15. Let's study the effect of limited DC gain opamps A_0 on the quality factor of the two-op-amp resonator and the maximum SNR of the two-op-amp resonator CT BP $\Sigma\Delta$ modulator. We can use Eq. 3.28 and Eq. 3.29 to calculate the values of the resonator's feedback resistors and capacitors: $R_F \approx 154\ \Omega$ and $C = 1231$ fF. Fig. 3.18 plots this resonator transfer function, using Eq. 3.25, for an op-amp DC gain, A_0, varying from 35 dB to 55 dB.

It can be seen from this figure, that when we increase A_0 from 35 dB to 55 dB, the quality factor, Q, is increasing from 19 to 186 and the centre frequency, f_0, varies from 390.3 MHz to 396.8 MHz.

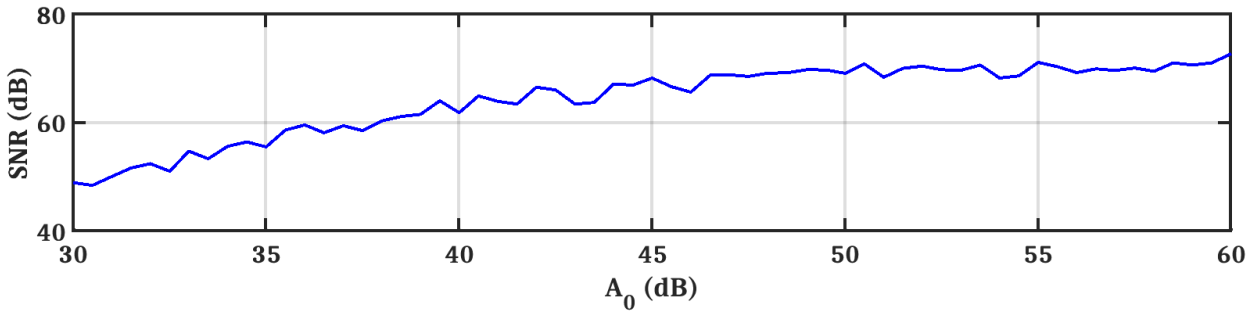

Fig. 3.19: The maximum SNR versus op-amp DC-gain, A_0, for a 4th-order two-op-amp resonator CT BP $\Sigma\Delta$ modulator mentioned in Fig. 3.16.

In Fig. 3.19, we show the effect of the op-amp DC gain on the maximum SNR of a 4th order CT BP $\Sigma\Delta$ modulator based on two-op-amp resonators.
These matlab simulations measure the SNR for an OSR of 64 and are based on the model of the feedback architecture, illustrated in Fig. 3.16, where each integrator is modeled using Eq. 3.26.
From this Figure, we can see that the maximum SNR is achieved for $A_0 \geq 48$ dB and we can achieve an SNR higher than 60 dB for $A_0 \geq 37$ dB.
In this chapter, we propose to use moderate DC-gain of op-amps $A_0 = 35\ dB$, which is implemented by only two-stage feed-forward op-amps explained later at section 4.3.2.

3.7 The integrators gain A

3.7.1 The mathematical model for the operational amplifier

Before we discuss the influence of the integrator gain A on the two-op-amp resonator performance, we should present first the operational amplifier circuit using our proposed mathematical model.

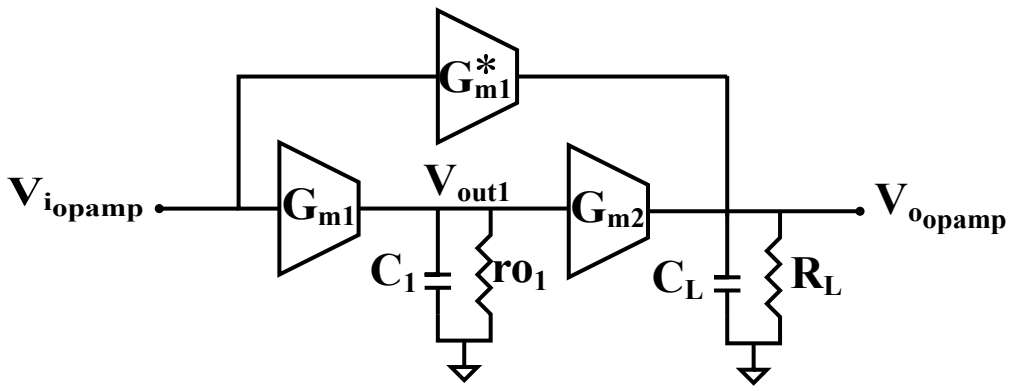

Fig. 3.20: The topology of the 2-stage feed-forward op-amp.

The topology of exploited op-amps is a 2-stage feed-forward op-amp as presented in Fig. 3.20. The transfer function of this op-amp can be expressed by the following relation:

$$H_{opamp}(s) = \frac{s.(\frac{A^*_{dc1}}{w_{p1}}) + (A^*_{dc1} + A_{dc1}.A_{dc2})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{pc}})} \tag{3.30}$$

where $\omega_{p1} = \frac{1}{ro_1 C_1}$, $\omega_{p2} = \frac{1}{R_L C_L}$, $\omega_{pc} \ggg \omega_{p1}$.

A_{dc1}, A_{dc2} and A^*_{dc1} are the DC-gains of the stages G_{m1}, G_{m2} and G^*_{m1}, respectively. $r_{o1}C_1$ and $R_L C_L$ are the product of the total resistance and the total capacitance seen at the output of each stage of the op-amp. We assumed that there is a non dominant pole $\omega_{pc} = 35\ \omega_{p1}$, which it is chosen to approach the op-amp transistor-level implementation results. G^*_{m1} is the feed-forward transconductance which adds a one left half plane (LHP) zero to 2-pole system for compensating the negative phase shift from poles, hence achieving a good phase margin. The relations of A_{dc1}, A_{dc2}, $A_{dc1}{}^*$ are represented as following:

$$A_{dc1} = G_{m1} \cdot ro_1 \quad A_{dc2} = G_{m2} \cdot R_L \quad A_{dc1}{}^* = G^*_{m1} \cdot R_L \tag{3.31}$$

3.7.2 The mathematical model for the two-op-amp resonator

The two-op-amp resonator as shown in Fig. 3.21 composes of two integrators, the 2nd integrator output connects to the op-amp input of the 1st integrator through the feedback resistor, R_F. This kind of resonator demands multi-stage op-amps with high DC-gains to obtain a high quality factor as discussed in chapter 2 at section 2.3 and also at section 3.6.

We propose a new technique where we select the integrator gain, A, with the appropriate value of the integrator resistor, R, to boost the quality factor, using moderate DC-gain implemented with only two-stage op-amps. This technique is discussed by the mathematical model and its MATLAB results are compared with the simulation results using the transistor-level implementation.

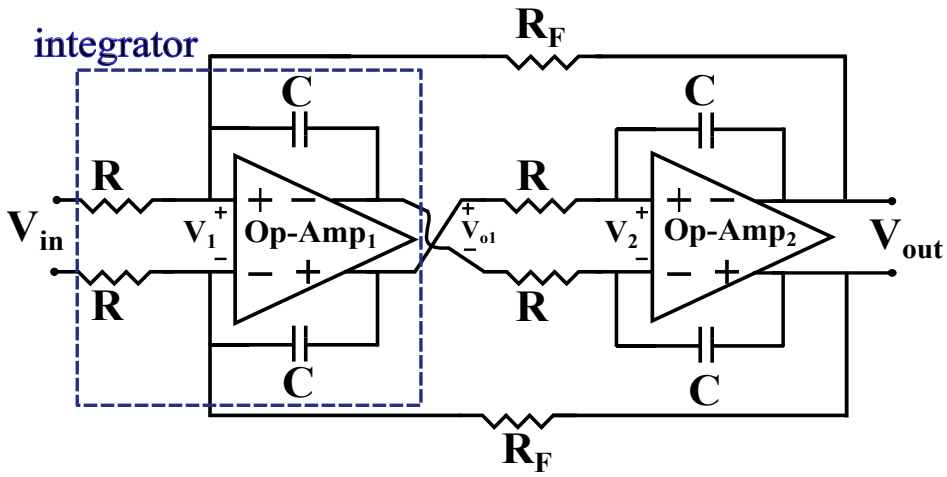

Fig. 3.21: Two-op-amp resonator circuit.

The mathematical model for the two-op-amp resonator:

We characterize the two-op-amp resonator circuit in Fig. 3.21 with the following equations:

$$\frac{\{V_{in}(s) - V_1(s)\}}{R} = \{V_1(s) + V_{o1}(s)\} \cdot s \cdot C + \frac{\{V_1(s) + V_{out}(s)\}}{R_F} \tag{3.32}$$

$$\frac{\{V_{o1}(s) - V_2(s)\}}{R} = \{V_2(s) + V_{out}(s)\} \cdot s \cdot C \tag{3.33}$$

$$V_{o1}(s) = V_1(s) \cdot H_{Op-Amp_1}(s) \tag{3.34}$$

$$V_{out}(s) = V_2(s) \cdot H_{Op-Amp_2}(s) \tag{3.35}$$

Each op-amp is only a 2-stage feed-forward op-amp explained before in section 3.7.1. At two different loads, the transfer functions of the same op-amp should be:

$$H_{Op-Amp_1}(s) = \frac{s.(\frac{\{A^*_{dc1}\}_1}{w_{p1}}) + (\{A^*_{dc1}\}_1 + A_{dc1}.\{A_{dc2}\}_1)}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\{\omega_{p2}\}_1})(1 + \frac{s}{\omega_{pc}})} \tag{3.36}$$

$$H_{Op-Amp_2}(s) = \frac{s.(\frac{\{A^*_{dc1}\}_2}{w_{p1}}) + (\{A^*_{dc1}\}_2 + A_{dc1}.\{A_{dc2}\}_2)}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\{\omega_{p2}\}_2})(1+\frac{s}{\omega_{pc}})} \tag{3.37}$$

The DC-gain of the 1st stage for the $Op-Amp_{1,\ 2}$ is A_{dc1}. The DC-gains of the 2nd stage for the $Op-Amp_{1,\ 2}$ are $\{A_{dc2}\}_{1,\ 2}$, respectively. As well as, the DC-gains of the feed-forward stage for the $Op-Amp_{1,\ 2}$ are $\{A^*_{dc1}\}_{1,\ 2}$, respectively. While, the 1st pole for the $Op-Amp_{1,\ 2}$ is ω_{p1}. The 2nd poles for the $Op-Amp_{1,\ 2}$ are $\{\omega_{p2}\}_{1,\ 2}$, respectively. The non-dominant pole $\omega_{pc} = 35\ \omega_{p1}$ for both $Op-Amp_{1,\ 2}$.

The relations of A_{dc1}, $\{A_{dc2}\}_1$, $\{A_{dc2}\}_2$, $\{A^*_{dc1}\}_1$ and $\{A^*_{dc1}\}_2$ are represented as following:

$$A_{dc1} = G_{m1} \cdot ro_1 \tag{3.38}$$

$$\{A_{dc2}\}_1 = G_{m2} \cdot R_{L1} \tag{3.39}$$

$$\{A_{dc2}\}_2 = G_{m2} \cdot R_{L2} \tag{3.40}$$

$$\{A^*_{dc1}\}_1 = G^*_{m1} \cdot R_{L1} \tag{3.41}$$

$$\{A^*_{dc1}\}_2 = G^*_{m1} \cdot R_{L2} \tag{3.42}$$

$$R_{L1} = \{\frac{ro_2 \cdot R}{ro_2 + R}\} \tag{3.43}$$

$$R_{L2} = \{\frac{ro_2 \cdot R_F}{ro_2 + R_F}\} \tag{3.44}$$

The transconductance of the 1st stage for the $Op-Amp_{1,\ 2}$ is G_{m1}, while the transconductance of the 2nd stage for the $Op-Amp_{1,\ 2}$ is G_{m2}, the transconductance of the feed-forward stage for the $Op-Amp_{1,\ 2}$ is G^*_{m1}. The output resistance of the 1st stage for the $Op-Amp_{1,\ 2}$ is ro_1, while the output resistance of the 2nd stage for the $Op-Amp_{1,\ 2}$ and the feed-forward stage for the $Op-Amp_{1,\ 2}$ is common, ro_2. The load resistance of the 2nd stage along with the feed-forward stage for the $Op-Amp_{1,\ 2}$ are R_{L1} and R_{L2}, respectively.

The relations of ω_{p1}, $\{\omega_{p2}\}_1$ and $\{\omega_{p2}\}_2$, can be deduced as following:

$$\omega_{p1} = \frac{1}{ro_1 \cdot C_1} \tag{3.45}$$

$$\{\omega_{p2}\}_1 = \frac{1}{R_{L1} \cdot C_{L1}} \tag{3.46}$$

$$\{\omega_{p2}\}_2 = \frac{1}{R_{L2} \cdot C_{L2}} \tag{3.47}$$

$$C_{L1},\ C_{L2} = C_2\ +\ C \tag{3.48}$$

The output parasitic capacitance of the 1st stage for the $Op-Amp_{1,\ 2}$ is C_1, while the output parasitic capacitance of the 2nd stage for the $Op - Amp_{1,\ 2}$ and the feed-forward stage for the $Op - Amp_{1,\ 2}$ is common, C_2. The load capacitance of the 2nd stage along with the feed-forward stage for the $Op - Amp_{1,\ 2}$ are C_{L1} and C_{L2}, respectively.

Based on the ideal transfer function of the integrator, from Fig 3.16, the initial value of integrator capacitor C and the feedback resistor R_F can be:

$$C = \frac{1}{A\ \cdot\ f_s\ \cdot\ R} \qquad R_F\ \approx\ R \cdot \{\frac{A}{\frac{\pi}{2}}\}^2 \tag{3.49}$$

where the sampling frequency, the integrator resistor, and the integrator gain are f_s, R, and A, respectively.

To finalize the proposed mathematical model, the values of the transconductance G_{m1}, G_{m2} and G^*_{m1}, and the values of the output resistance ro_1 and ro_2, as well as the values of the parasitic capacitance C_1 and C_2, are shown in table 3.4, extracted from the transistor-level implementation op-amps explained in section 4.3.2.

The two-op-amp resonator circuit is a complex transfer function, based on the previous equations [Eq. 3.32 : Eq. 3.49]. The denominator's order becomes higher than 2, so we can't express the denominator as the one of the traditional resonator $s^2 + \frac{\omega_0}{Q}s + \omega_0^2$. Therefore we can't have an explicit or a closed form equation for the quality factor Q and the center frequency f_0. We assume the transfer function of this two-op-amp resonator circuit for simplicity, where its simplified topology presented in Fig. 3.22, as following:

$$H_{2-op-amp\ resonator}(s)\ =\ \frac{H_{integ_1}(s)\ \cdot\ H_{integ_2}(s)}{1\ +\ {g_1}^*\ \cdot\ H_{integ_1}(s)\ \cdot\ H_{integ_2}(s)} \tag{3.50}$$

where

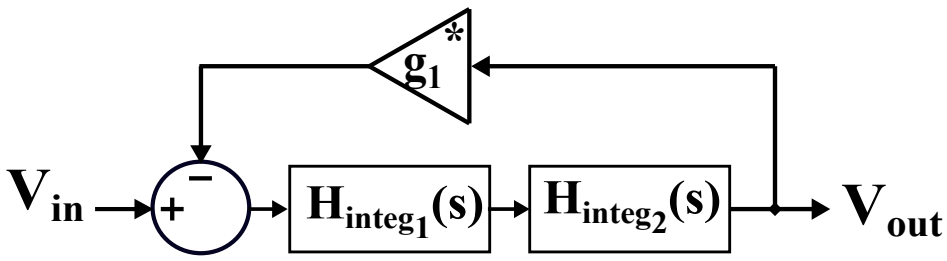

Fig. 3.22: A simplified two-op-amp resonator topology.

$$H_{integ_1}(s) = \frac{1}{\frac{1}{H_{Op-Amp_1}(s)} + s.RC.(\frac{1}{H_{Op-Amp_1}(s)} + 1)} \tag{3.51}$$

$$H_{integ_2}(s) = \frac{1}{\frac{1}{H_{Op-Amp_2}(s)} + s.RC.(\frac{1}{H_{Op-Amp_2}(s)} + 1)} \tag{3.52}$$

Transfer function of the 1st integrator is H_{integ_1}, while transfer function of the 2nd integrator is H_{integ_2} in the simplified two-op-amp resonator topology presented in Fig. 3.22.

Table 3.4: The op-amps specifications used in the mathematical models.

G_{m1}	22.2 mS
G_{m2}	10.3 mS
G^*_{m1}	80.82 mS
ro_1	922 Ω
ro_2	279 Ω
C_1	143 fF
C_2	525 fF

3.7.3 The comparison of the mathematical model and the transistor-level implementation for the two-op-amp resonator and the operational amplifier

To study the effect of the integrator gain A on the quality factor Q of the 2-op-amp resonator, we use the graphical method to measure it as we mentioned that we can't have a closed form equation for the quality factor Q.

For example, in Fig. 3.23, we plot the two-op-amp resonator gain using: mathematical model solved by equations [3.50, 3.51, 3.52] simulated by MATLAB using the op-amps specifications presented in table 3.4, at the integrator resistor $R = 677\ \Omega$, integrator gain $A = 0.75$ and the sampling frequency $f_s = 1.6\ GHz$. We measured both of the bandwidth (BW) and the center frequency f_0 as presented, then the quality factor Q equals to $\frac{f_0}{BW}$. Here, the quality factor Q and the center frequency f_0 are 81.5 and 380 MHz, respectively.

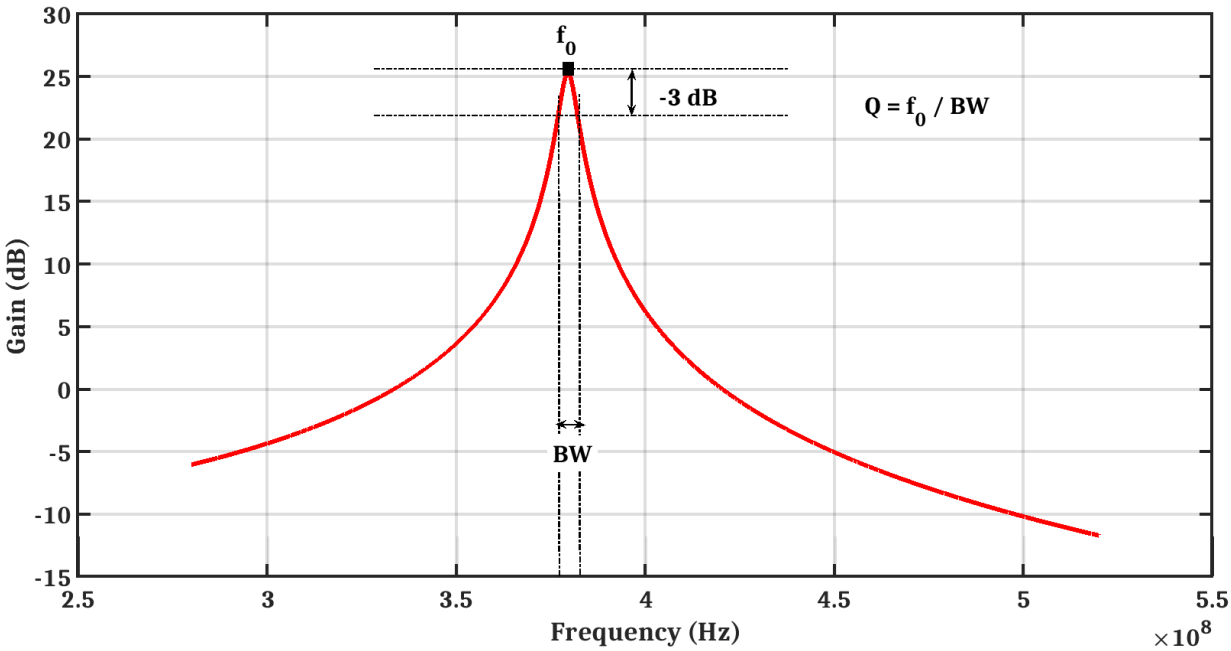

Fig. 3.23: The two-op-amp resonator gain using: mathematical model of equations [3.50, 3.51, 3.52] and simulated by MATLAB using the op-amps specifications presented in table 3.4, at the integrator resistor $R = 677\ \Omega$, integrator gain $A = 0.75$ and the sampling frequency $f_s = 1.6\ GHz$.

As mentioned in Fig. 3.15, we selected the integrator resistor $R = 677\ \Omega$ and integrator gain $A = 0.75$ to have SNR greater than 60 dB in the two-op-amp resonator CT BP $\Sigma\Delta$ modulator discussed in section 3.5. Also, at this value of integrator gain A, we should validate that we can achieve a high quality factor Q of two-op-amp resonator.

In Fig. 3.24, we compare the quality factor Q of the mathematical model of the two-op-amp resonator represented by the equations [3.50, 3.51, 3.52] and simulated by MATLAB using the op-amps specifications presented in table 3.4, and the quality factor Q of the transistor-level design of the two-op-amp resonator simulated by a circuit simulator at the integrator resistor $R = 677\ \Omega$ and the sampling frequency $f_s = 1.6\ GHz$.

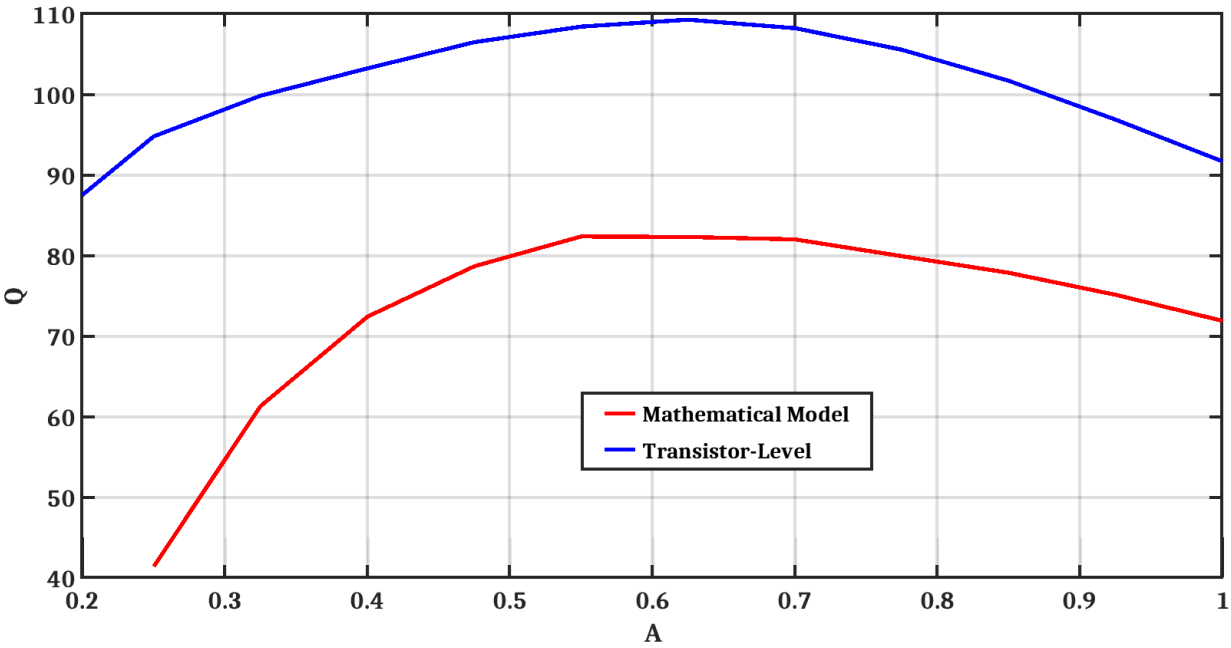

Fig. 3.24: The quality factor Q of the two-op-amp resonator using: mathematical model of equations [3.50, 3.51, 3.52] and simulated by MATLAB using the op-amps specifications presented in table 3.4, and the transistor-level design simulated by a circuit simulator at the integrator resistor $R = 677\ \Omega$ and the sampling frequency $f_s = 1.6\ GHz$.

Fig. 3.24 shows that the gain of the integrators A has a great influence on the quality factor of the two-op-amp resonator circuit using both the mathematical model and the transistor-level implementation. So that, we can select the proper value of the integrator gain A where we have the highest quality factor Q, using moderate DC-gain of the op-amps as presented before.

Fig. 3.25 presents the gain of the operational amplifier using both the mathematical model solved by equation 3.36 simulated by MATLAB using the op-amps specifications presented in table 3.4 and the transistor-level design simulated by a circuit simulator, both at integrator gain $A = 0.75$, integrator resistor $R = 677\ \Omega$ and the sampling frequency $f_s = 1.6\ GHz$. The specifications of both operational amplifiers are presented in table 3.5.

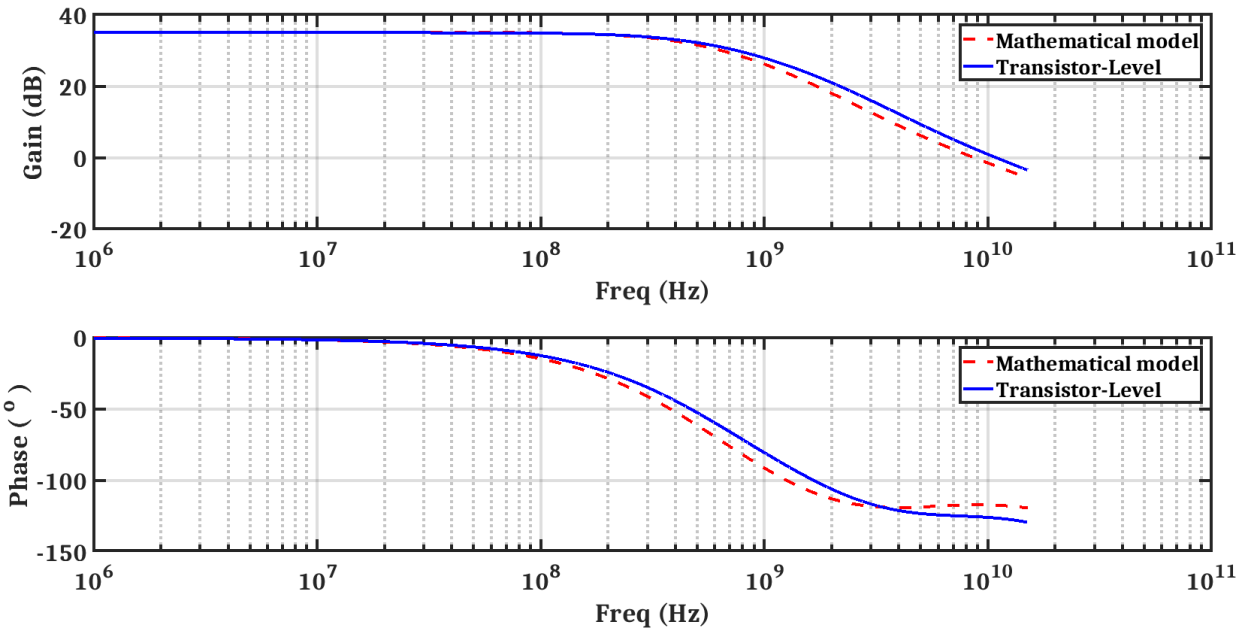

Fig. 3.25: The gain and phase of the operational amplifier using: mathematical model solved by equation 3.36 simulated by MATLAB using the op-amps specifications presented in table 3.4, and the transistor-level design simulated by a circuit simulator, both op-amps are loaded by R_{L1} and C_{L1}.

Table 3.5: The op-amps specifications using the mathematical model and the transistor-level design from Fig. 3.25.

	DC-gain	Unity gain Frequency (f_T)	Phase Margin (PM)
Mathematical model	35.2 dB	8.7 GHz	63°
Transistor-Level	35 dB	10.4 GHz	54°

Fig. 3.26 presents the gain of the operational amplifier using both the mathematical model solved by equation 3.37 simulated by MATLAB using the op-amps specifications presented in table 3.4 and the transistor-level design simulated by a circuit simulator, both at integrator gain $A = 0.75$, integrator resistor $R = 677\ \Omega$ and the sampling frequency $f_s = 1.6\ GHz$. The specifications of both operational amplifiers are presented in table 3.6.

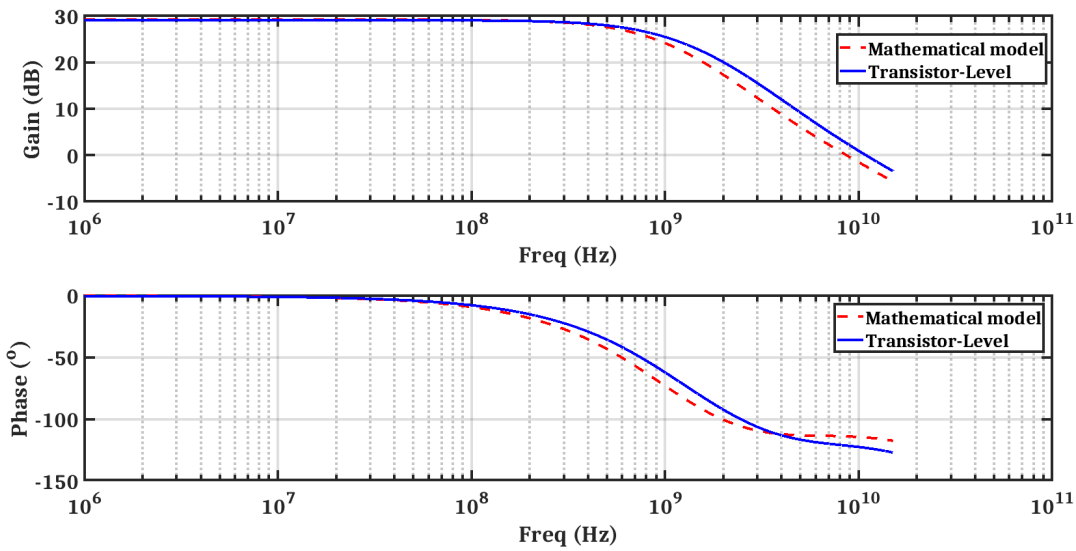

Fig. 3.26: The gain and phase of the operational amplifier using: mathematical model solved by equation 3.37 simulated by MATLAB using the op-amps specifications presented in table 3.4, and the transistor-level design simulated by a circuit simulator, both op-amps are loaded by R_{L2} and C_{L2}.

Table 3.6: The op-amps specifications using the mathematical model and the transistor-level design from Fig. 3.26.

	DC-gain	Unity gain Frequency (f_T)	Phase Margin (PM)
Mathematical model	29.4 dB	8.7 GHz	66°
Transistor-Level	29.2 dB	11 GHz	57.2^o

3.8 Conclusion

We introduced first a new approximate study of the thermal noise behaviour for the 4th-order CT BP $\Sigma\Delta$ modulator based on two-op-amp resonators. The influence of both integrator resistor R and integrator gain A is considered, where this study allows the designer to select the convenient values for both of them at the required SNR. The suggested technique is well matched with the noise transient analysis simulation of the macro-model implementation with a small error ≤ 2.5 %. The noise contributed by the quantizer isn't considered as it is a little-bit affected on the input-referred noise of $\Sigma\Delta$ modulator that was validated before by the macro-model noise transient analysis simulation results.

Based on this proposed noise study, we selected the values of the integrator resistor $R = 677\ \Omega$ and the integrator gain $A = 0.75$ to achieve a SNR greater than 60 dB. Then, we studied the effect of limited DC-gain op-amps A_0 on the quality factor of the two-op-amp resonator and the maximum SNR of the two-op-amp resonator CT BP $\Sigma\Delta$ modulator. So that, we proposed to use moderate DC-gain op-amps $A_0 = 35\ dB$. At the end, we suggested a new technique to select the proper value of the integrator gain A to boost the quality factor of the two-op-amp resonator using moderate DC-gain op-amps $A_0 = 35\ dB$. That was proved by the mathematical models and they were compared with the simulation results of the transistor-level designs.

Chapter 4

Two-op-amp resonator CT BP $\Sigma\Delta$ Modulator design

4.1 Introduction

In this chapter, we present the complete design of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator.

First in section 4.2, we discuss the system-level of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Second in section 4.3, we discuss the transistor-level implementation design of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Third in section 4.4, we discuss the layout implementation design of two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. At the end, we show the post-layout results compared to the state of the art, in section 4.5.

4.2 The system level

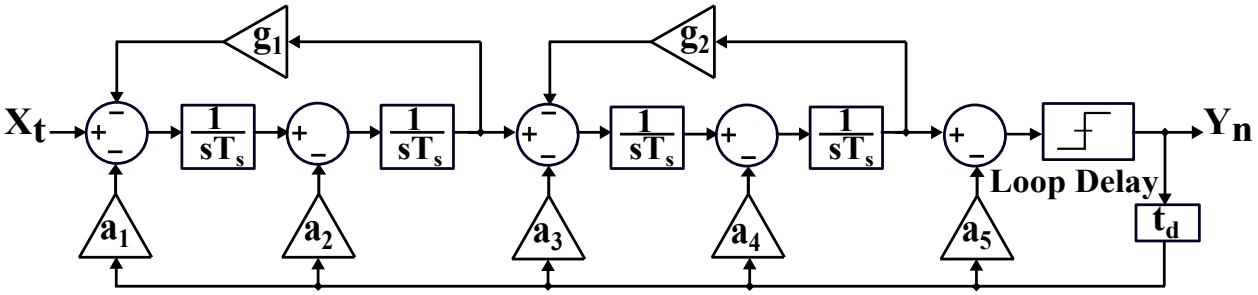

Fig. 4.1: A 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using a two-op-amp resonator, taken from Schreier toolbox (before scaling).

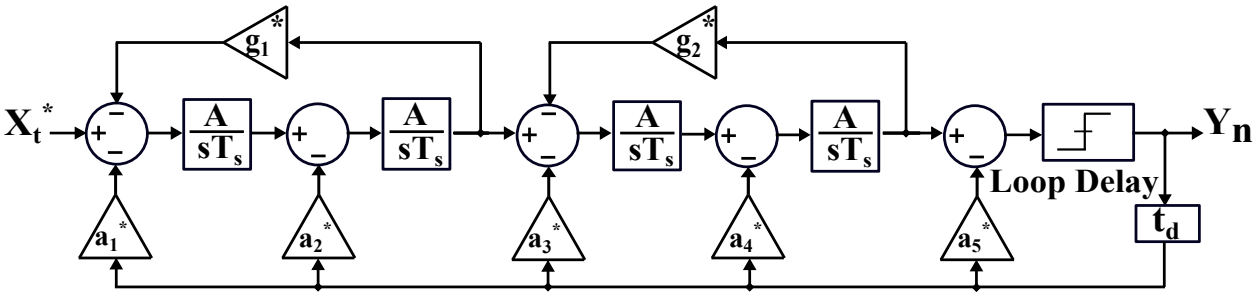

Fig. 4.2: A 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using a two-op-amp resonator, which used in the transistor-level implementation (after scaling).

Fig. 4.1 presents the block diagram of a 4th-order CT BP $\Sigma\Delta$ modulator using a two-op-amp resonator, taken from Schreier toolbox (before scaling). Its coefficients are calculated as following: 1) using the synthesis function in Schreier toolbox to design a bandpass NTF centered at quarter the sampling frequency with optimized SNR at OSR = 64, we get the discrete time loop gain transfer function. 2) By applying the pulse invariant transformation, the z-domain model of the continuous-time loop is found [Aboushady02]. With some simple manipulation, we calculate the continuous-time coefficients by matrix division.While, Fig. 4.2 shows a 4th-order CT BP $\Sigma\Delta$ modulator using a two-op-amp resonator, which used in the transistor-level implementation, after using the scaling method that discussed before

Table 4.1: The values of the feedback coefficients presented in Fig. 4.1 and Fig. 4.2, at $A = 0.75$, $t_d = 1.5\ T_s$ and $I_{scale} = 60\ \cdot\ 10^{-6}$.

after scaling	before scaling
${a_1}^* = 60.5\ \cdot\ 10^{-6}$	$a_1 = 0.584$
${a_2}^* = 0.0$	$a_2 = 0.0$
${a_3}^* = -\ 11.25\ \cdot\ 10^{-6}$	$a_3 = -\ 0.1453$
${a_4}^* = -\ 39\ \cdot\ 10^{-6}$	$a_4 = -\ 0.86$
${a_5}^* = -\ 11.25\ \cdot\ 10^{-6}$	$a_5 = -\ 0.3714$
${g_1}^* = (2.08)^2$	$g_1 = (1.56)^2$
${g_2}^* = (2.113)^2$	$g_2 = (1.585)^2$
${X_t}^* = -23.6$ dB	$X_t = -6.8$ dB

in chapter 3 at section 3.2. Table 4.1 demonstrates the values of the feedback coefficients presented in Fig. 4.1 and Fig. 4.2.

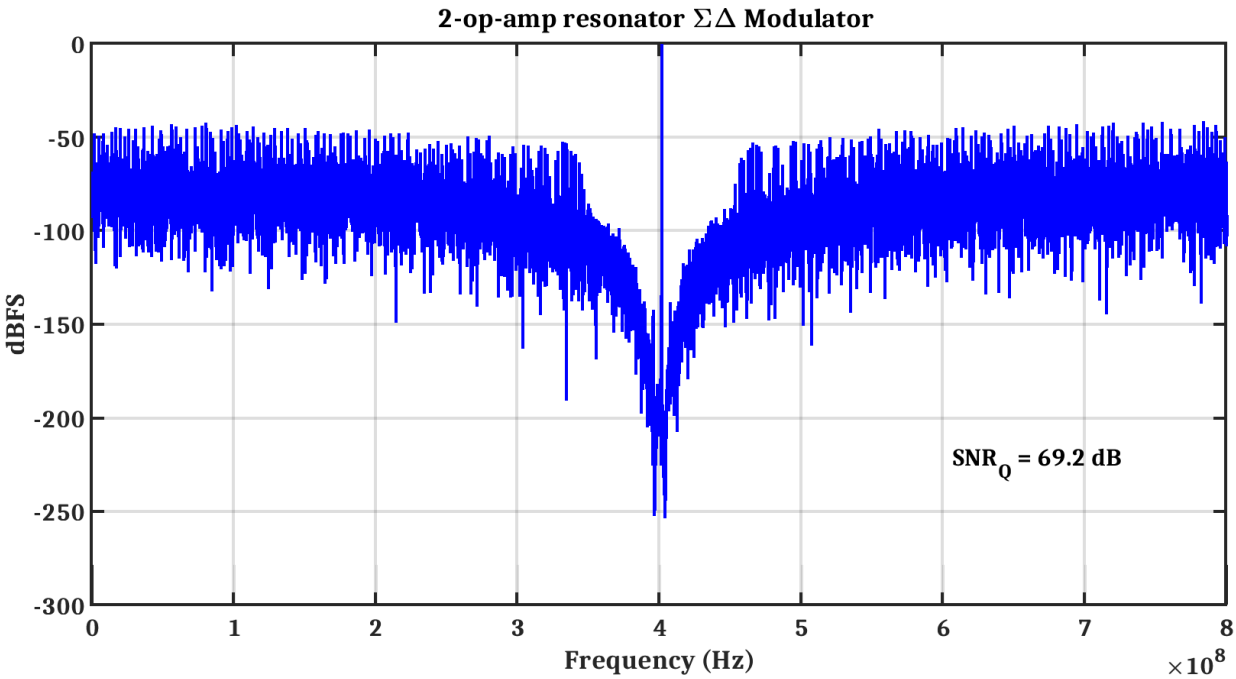

Fig. 4.3: The output spectrum of an ideal model for 4th-order continuous-time bandpass $\Sigma\Delta$ modulator by MATLAB of Fig. 4.1

In Fig. 4.3, we present the output spectrum of an ideal model for 4th-order CT BP $\Sigma\Delta$ modulator simulated by MATLAB of Fig. 4.1. These MATLAB simulations measure the maximum signal to quantization ratio (SNR_Q) of 69.2 dB.

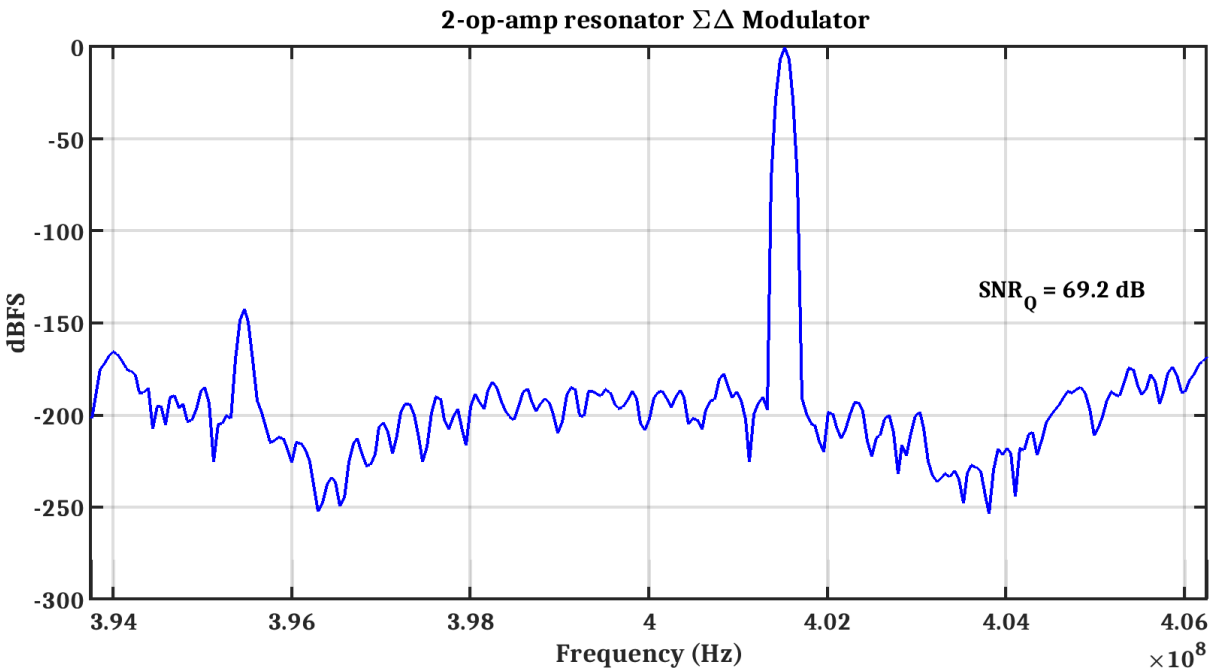

Fig. 4.4: The output spectrum of an ideal model for 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using two-op-amp resonators, simulated by MATLAB of Fig. 4.3, in the bandwidth of $\Sigma\Delta$ modulator, from 393.75 MHz to 406.25 MHz.

In Fig. 4.4, we present the output spectrum of an ideal model for 4th-order CT BP $\Sigma\Delta$ modulator using two-op-amp resonators, simulated by MATLAB of Fig. 4.3, in the bandwidth of $\Sigma\Delta$ modulator, from 393.75 MHz to 406.25 MHz.

4.3 The transistor-level implementation design

Fig. 4.5 shows the circuit-level implementation of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator design based on 2-op-amp resonators that was presented before in Fig. 4.2.

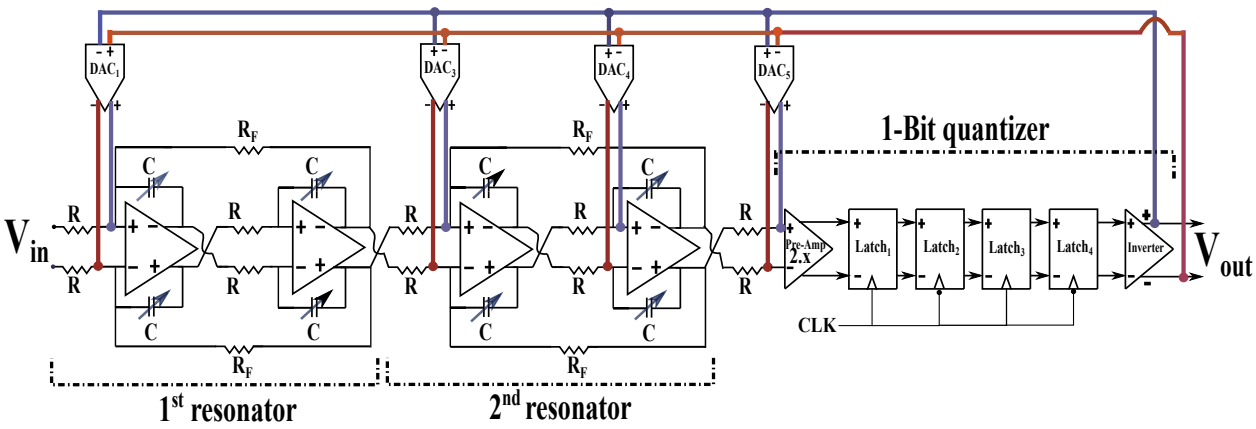

Fig. 4.5: The circuit-level implementation of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator based on 2-op-amp resonators.

In Fig. 4.5, two 2-op-amp resonators are connected in series through resistors and capacitors in order for the 2nd op-amp output of the 1st resonator to directly drive the input of the 2nd resonator. Four feed-back paths through current steering DACs connect the 1-Bit quantizer output to the input node of each op-amp starting from the 1st op-amp to the 3rd op-amp, the 4th op-amp and the input node of the 1-Bit quantizer, respectively. The main blocks are the two-op-amp resonator, the operational amplifier, 1-Bit quantizer and the current steering DACs with its biasing circuit. All blocks are designed on 28 nm FD-SOI technology using Low V_{TH} devices, that are also called "flipped-well" devices.

4.3.1 Two-op-amp resonator

The two-op-amp resonator is composed of two integrators with a feedback resistor, R_F, as presented in Fig. 4.5. The values of the integrator resistor R and the integrator gain A are equal to 677 Ω and 0.75, respectively, which are calculated from chapter 3, Fig. 3.15. Also, at this value of integrator gain $A = 0.75$, we showed that a high quality factor can be achieved in chapter 3 in section 3.7.2.

The feedback resistor , R_F, can be deduced from the following relation:

$$R_F = R.(\frac{A^2}{g_{1,2}}).\frac{1}{(1+\frac{2}{A_0})}, \qquad g_{1,2} \;=\; (\frac{\pi}{2})^2 \tag{4.1}$$

where the DC-gain, A_0 of the exploited op-amps, is around 35 dB. The capacitor, C, is implemented by a fixed cap, equal to 560 fF, in parallel with a trimming capacitor that is composed of two 4-Bit capacitors arrays with a $6fF$ and $50fF$ unit cap as presented in Fig. 4.6. The implementation of the transmission gate [Kumar17], used in the capacitor arrays of Fig. 4.6, is shown in Fig. 4.7. The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of PMOS/NMOS transistor in the transistor-level implementation of the transmission gate shown in Fig. 4.7 are presented in Table 4.2.

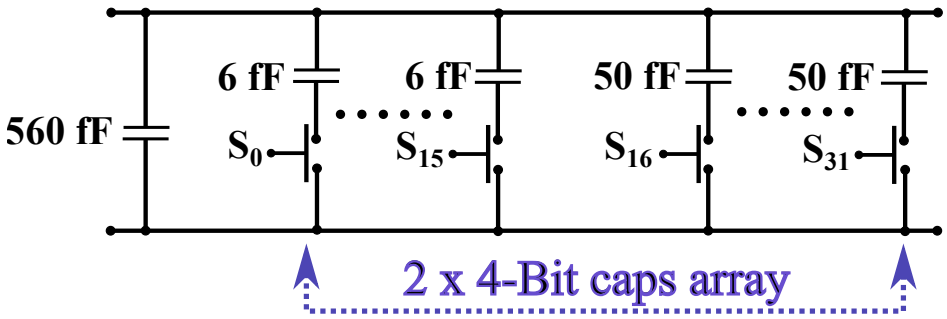

Fig. 4.6: The implementation of the capacitor C for the two-op-amp resonators presented in Fig. 4.5.

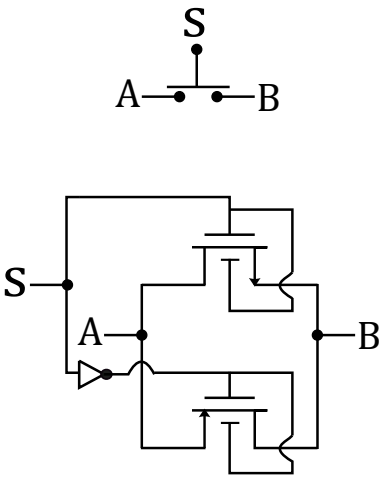

Fig. 4.7: The implementation of the transmission gate used in the capacitor arrays of Fig. 4.6, at $V_{DD} = 1.5$ V.

Table 4.2: The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of PMOS/NMOS transistor in the transistor-level implementation of the transmission gate shown in Fig. 4.7

.

M_i	W_f	L_f	$N_{fingers}$
$M_{NMOS,PMOS}$	1 μm	100 nm	10

For the RC network used in the transistor-level implementation of the op-amps presented at section 4.3.2 in case of the two-op-amp resonator, the values of resistors and capacitors R, R_F and C are equal to 677 Ω, 154 Ω and 1106 fF, respectively. In Fig. 4.8, the op-amp achieves a DC-gain $A_0 = 35$ dB, a unity-gain frequency, $f_T = 10.8$ GHz, and a phase margin, $PM = 54°$, when loaded with this RC network.

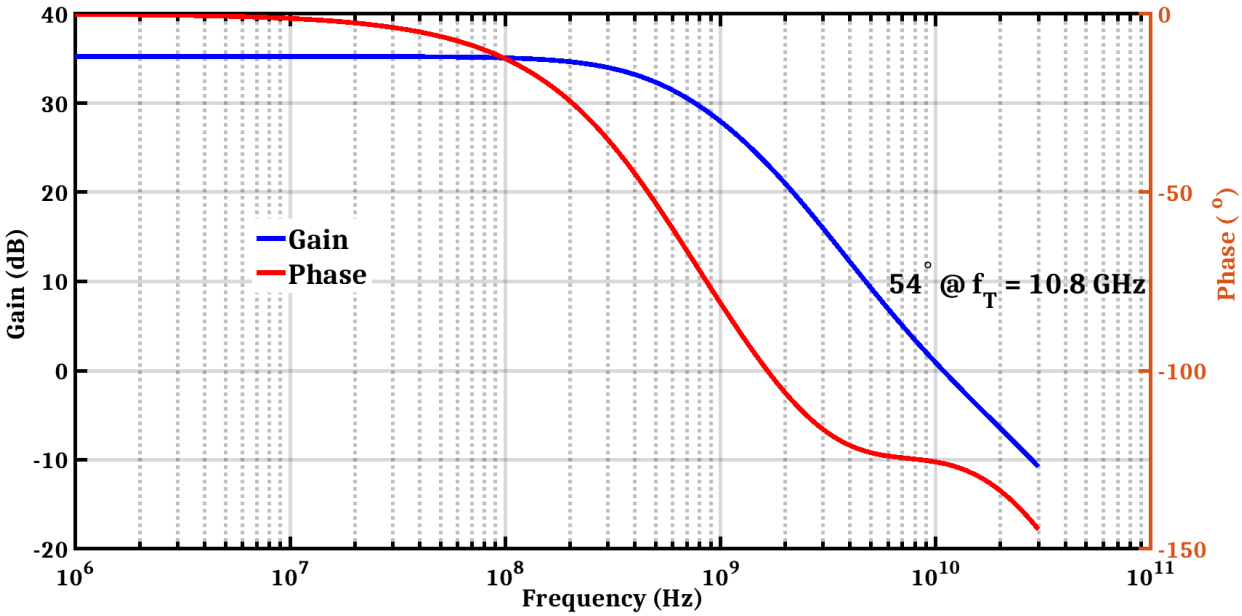

Fig. 4.8: Frequency response of the transistor level 2-stage feed forward op-amp, presented at section 4.3.2, loaded with the RC network of two-op-amp resonator.

Fig. 4.9 presents the transistor-level gain of a single 2-op-amp resonator, using fine tuning through a 4-Bit caps array of 6fF unit cap. It is shown that when we fine-tune the gain of a

single 2-op-amp resonator using fine tuning through a 4-Bit caps array of 6fF unit cap, the absolute change of the center frequency $\mid \Delta f_0 \mid$ is around 2 MHz, while the absolute change of the quality factor $\mid \Delta Q \mid$ is around 30.

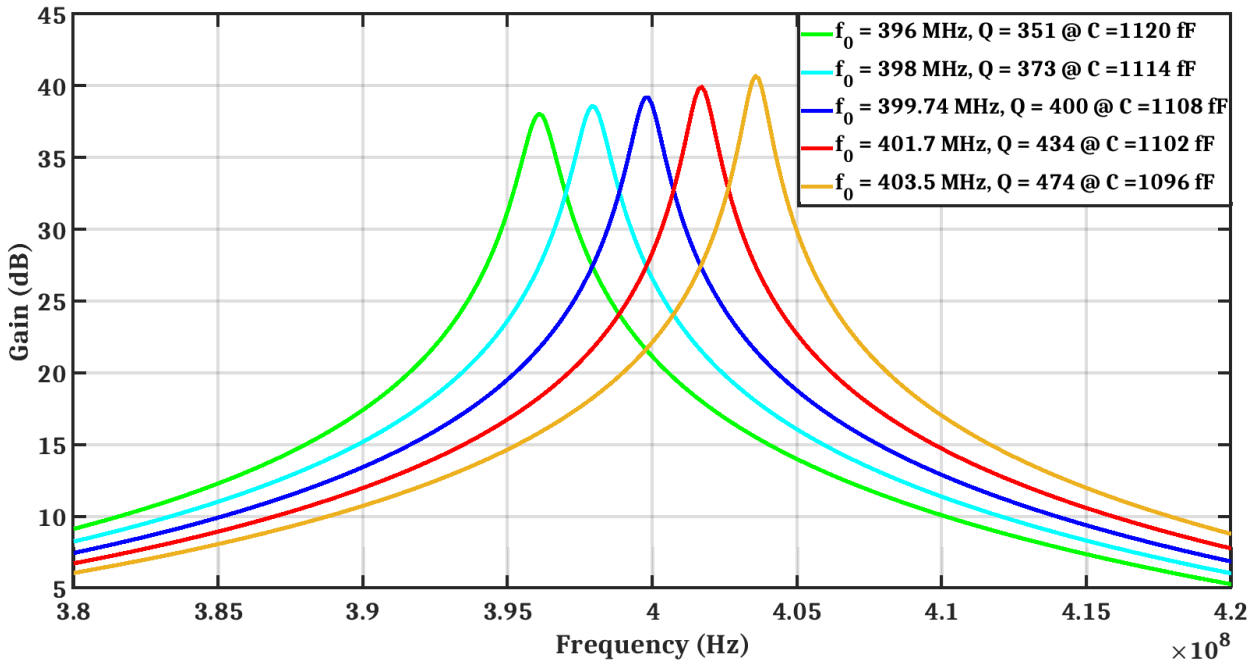

Fig. 4.9: The transistor-level gain of a single 2-op-amp resonator, using fine tuning through a 4-Bit caps array of 6fF unit cap.

Fig. 4.10 presents the transistor-level gain of a single 2-op-amp resonator, using coarse tuning through a 4-Bit caps array of 50fF unit cap. It is shown that when we coarse-tune the gain of a single 2-op-amp resonator using coarse tuning through a 4-Bit caps array of 50fF unit cap, the absolute change of the center frequency $\mid \Delta f_0 \mid$ is around 16 MHz, while the absolute change of the quality factor $\mid \Delta Q \mid$ is huge.

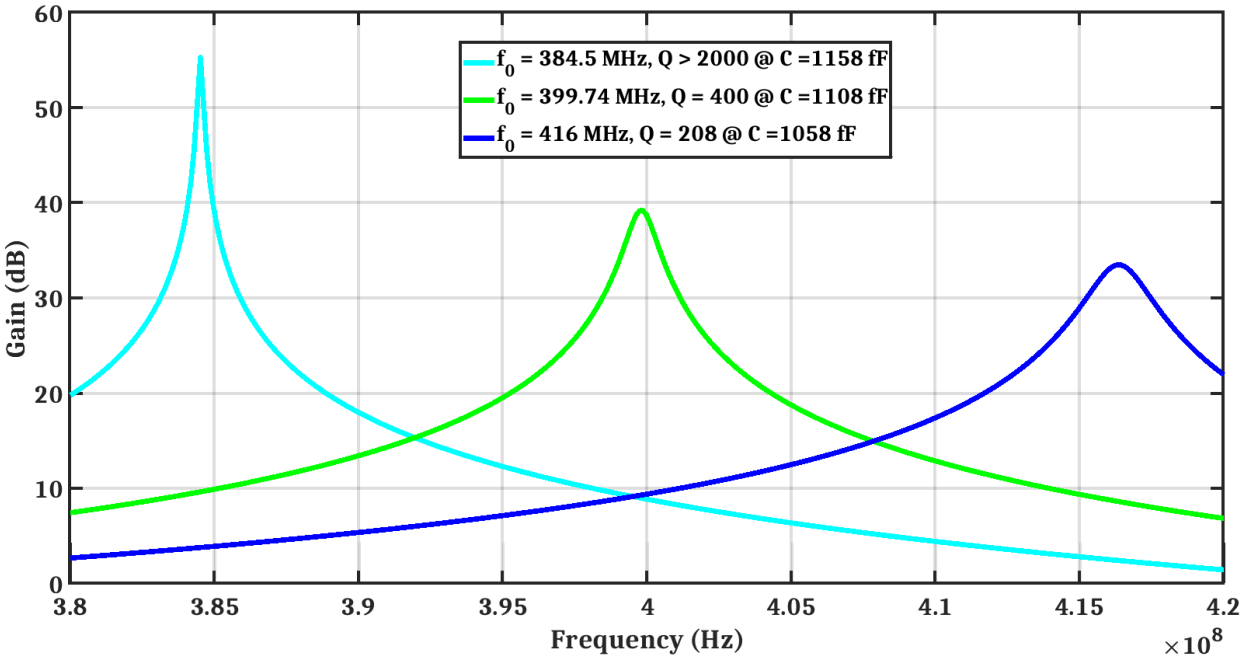

Fig. 4.10: The transistor-level gain of a single 2-op-amp resonator, using coarse tuning through a 4-Bit caps array of 50fF unit cap.

Fig. 4.11 presents the transistor-level simulation results of the 4th-order loop filter gain centered at $f_0 = 400$ MHz, composed of two 2-op-amp resonators connected in-series. It has two resonance frequencies $f_{01,\ 02} = 397.2\ MHz,\ 405.4\ MHz$, where f_{01} is the resonance frequency of the 1st resonator and f_{02} is the resonance frequency of the 2nd resonator. The quality factor of the 1st resonator Q_1 is 650 and the quality factor of the 2nd resonator Q_2 is 193.

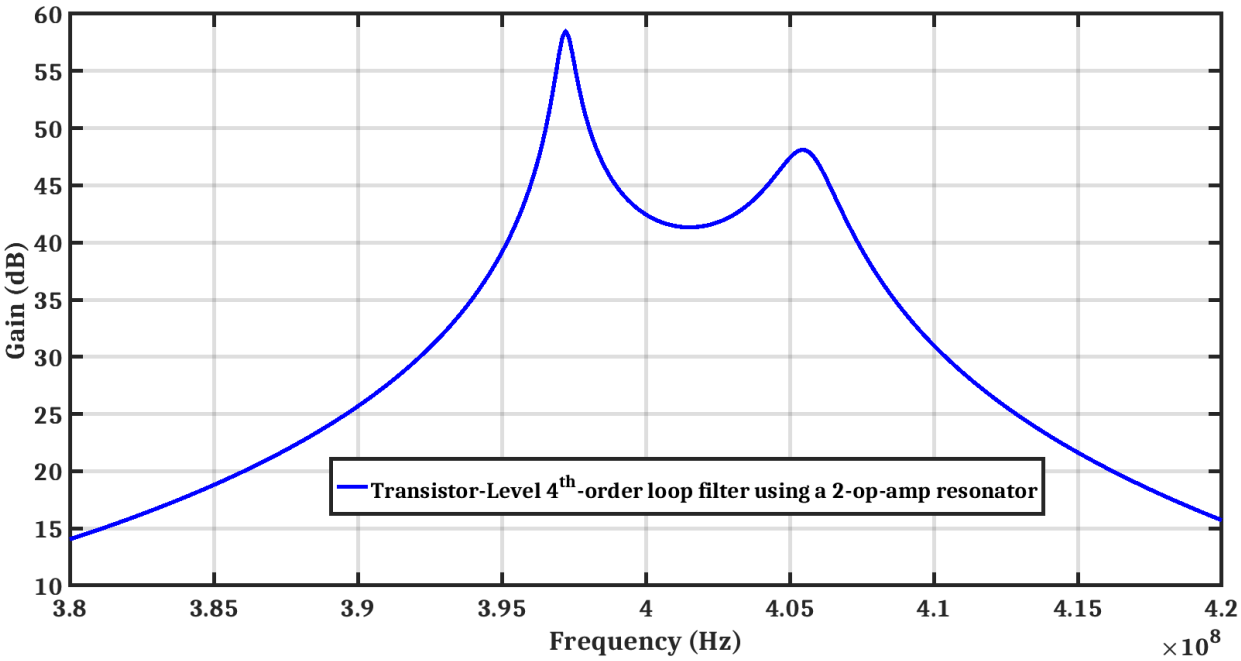

Fig. 4.11: The transistor-level gain of the 4th-order loop filter using a two-op-amp resonator, two 2-op-amp resonators connected in-series, centered at $f_0 = 400\ MHz$ with two resonance frequencies $f_{01,\ 02} = 397.2\ MHz,\ 405.4\ MHz$ and $Q_{1,2} = 650,\ 193$.

4.3.2 The transistor-level implementation for the operational amplifier:

The transistor-level implementation of the exploited op-amps is shown in Fig. 4.12. The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of each transistor in the transistor-level implementation of 2-stage feed-forward op-amp shown in Fig. 4.12 are presented in Table 4.3, where the values of both I_b, $BB_{1,\ 2}$ and R_{cm} are equal to 50 μA, 0 V and 3.5 $K\Omega$, respectively.

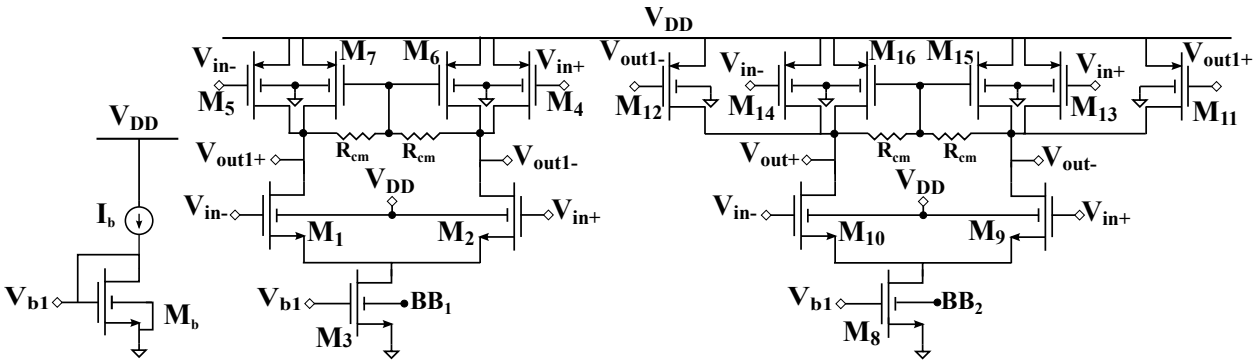

Fig. 4.12: Transistor-level implementation of the 2-stage feed-forward op-amp, at V_{DD} = 1.5 V.

Table 4.3: The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of each transistor in the transistor-level implementation of 2-stage feed-forward op-amp in Fig. 4.12

.

M_i	W_f	L_f	$N_{fingers}$
M_b	5 μm	100 nm	1
$M_{1,\ 2}$	4 μm	100 nm	22
M_3	5 μm	100 nm	30
$M_{4,\ 5}$	1 μm	100 nm	22
$M_{6,\ 7}$	1 μm	100 nm	14
M_8	5 μm	100 nm	106
$M_{9,\ 10}$	6 μm	100 nm	50
$M_{11,\ 12}$	2.4 μm	100 nm	24
$M_{13,\ 14}$	2.4 μm	100 nm	26
$M_{15,\ 16}$	2.4 μm	100 nm	10

The G_{m1} and G^*_{m1} are implemented through the current reusing. G_{m1} is approximately equal to the sum of $g_{m_{MN_{1,\ 2}}}$ and $g_{m_{MP_{4,\ 5}}}$. The G^*_{m1} is the sum of $g_{m_{MN_{9,\ 10}}}$ and $g_{m_{MP_{13,\ 14}}}$. For G_{m2}, it is designed through $MP_{11,\ 12}$.

Resistive common-mode feedback circuits are used in transistors $MP_{6,\ 7,\ 15,\ 16}$.

To minimize the input-referred thermal noise, the 1st stage, G_{m1}, consumes 3.7 mW. The complete op-amp consumes 18.75 mW, at $V_{DD} = 1.5$ V.
In order to reduce the parasitic capacitances of the input NMOS transistors, $MN_{1,\ 2,\ 9,\ 10}$, we reduce the threshold voltage, V_{TH_n}, of these transistors by connecting their body-bias to the supply voltage, while the body-bias of the input PMOS transistors, $MP_{4,\ 5,\ 13,\ 14}$, are connected to the ground for reducing the threshold voltage, V_{TH_p}.
For NMOS transistors, $MN_{3,\ 8}$, their body bias are free because the threshold voltage should be trimmed to adjust the currents during both of the post-layout and the process corners simulations [Lechevallier15], [Danilovic16], [Streel17]. Each body bias voltage, BB_1 or BB_2, is supplied from a 7-Bit Digital to Analog Converter (DAC) with 0/1.5V supply rails.

4.3.3 1-Bit quantizer

The 1-Bit quantizer block is composed of two of the pre-amplifier followed by four Source-Coupled-Logic (SCL) latches ($Latch_1$, $Latch_2$, $Latch_3$ and $Latch_4$) having inverted clock signals, which facilitates an excess loop delay of 1.5 T_s [Sayed20b].
The transistor-level implementation of both the pre-amplifier and the SCL latch are presented in Fig. 4.13 and Fig. 4.14. The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of each transistor in the transistor-level implementation of the pre-amplifier and the SCL latch are presented in Table 4.4, where the values of both $BB_{Pre-Amp,\ Latches-Inverter}$ and R_{cm_1} are equal to 0 V and 2 $K\Omega$, respectively.

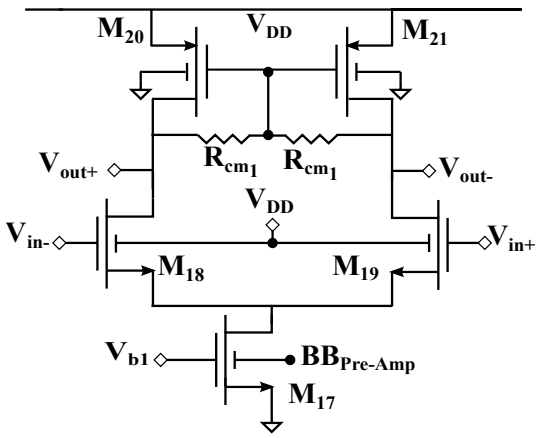

Fig. 4.13: The transistor-level implementation of the pre-amplifier/Inverter, at V_{DD} = 1.5 V.

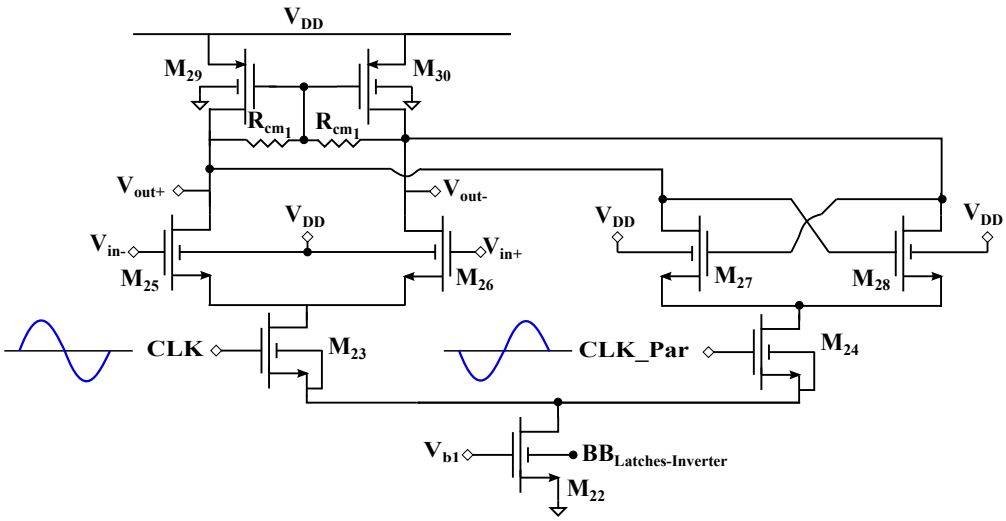

Fig. 4.14: The transistor-level implementation of Source-Coupled-Logic (SCL) latch, at V_{DD} = 1.5 V.

Table 4.4: The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of each transistor in the transistor-level implementation of the pre-amplifier and the SCL latch

.

M_i	W_f	L_f	$N_{fingers}$
M_{17}	2.5 μm	100 nm	30
$M_{18,\ 19}$	1.8 μm	100 nm	22
$M_{20,\ 21}$	1.5 μm	100 nm	10
M_{22}	2.5 μm	100 nm	15
$M_{23,\ 24}$	0.6 μm	100 nm	4
$M_{25,\ 26}$	0.6 μm	100 nm	36
$M_{27,\ 28}$	0.6 μm	100 nm	4
$M_{29,\ 30}$	0.3 μm	100 nm	24

The last block is the inverter to decouple the fourth latch, $Latch_4$, from the current steering DACs. The transistor-level implementation of the inverter is the same as the pre-amplifier but it consumes roughly half of the power of the pre-amplifier.

The complete 1-Bit quantizer consumes 6.24 mW, at $V_{DD} = 1.5$ V.

All the blocks implementing 1-Bit quantizer have the same active load of diode-connected PMOS transistors combined with resistive common-mode feedback circuit, R_{cm_1}. This kind of load gives the flexibility to set the DC-gain and bandwidth based on the resistor, R_{cm_1}, without changing the output common mode. The body bias of the current source NMOS transistors $M_{17,\ 22}$ are free, $BB_{Pre-Amp,\ Latches-Inverter}$, are supplied from a 7-Bit DAC with 0/1.5V supply rails. We see that it is of major importance to trim the currents of the NMOS transistors $M_{17,\ 22}$ during both of the post-layout and the process corners simulations.

4.3.4 Current steering DACs with its biasing circuit

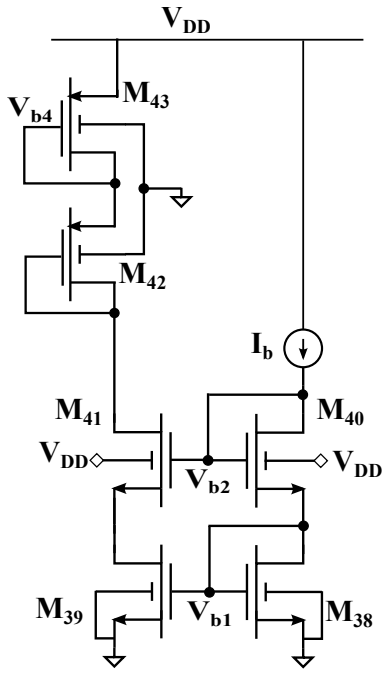

Fig. 4.15: The biasing circuit for current steering DACs, at V_{DD} = 1.5 V.

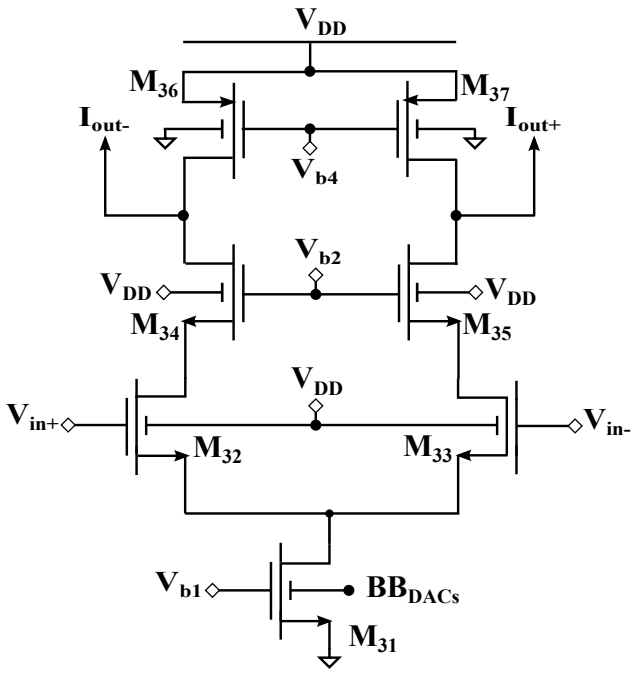

Fig. 4.16: The current steering DAC, at V_{DD} = 1.5 V.

Fig. 4.15 and Fig. 4.16 present the transistor-level implementation of a current-steering DAC along with its biasing circuit.

It enables a high-speed operation of input switches through NMOS transistors M_{32} and M_{33}, due to the body bias connection to the supply voltage for decreasing the threshold-voltage along with its parasitic capacitance.

The cascode NMOS transistors M_{34} and M_{35} are utilized for a high output impedance. They decouple the differential input of 1-Bit quantizer from the differential analog output current, $I_{out+,-}$.

The body connection of the PMOS current source transistors M_{36} and M_{37} is biased to the ground to have a low parasitic capacitance loading at the output nodes $I_{out+,-}$ which is

connected to the virtual ground of each op-amp.
The voltage headroom available for the PMOS transistors current source $M_{36,\ 37}$ together with the cascode NMOS transistors $M_{34,\ 35}$ and the current source NMOS transistor M_{31} is large enough around 1.4 V.
The body bias of the current source transistor M_{31} is free, BB_{DACs}, is supplied from a 7-Bit DAC with 0/1.5V supply rails.
The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of each transistor in the transistor-level implementation of the current-steering DAC (DAC_1), along with its biasing circuit in table 4.5.
The $NMOS$ transistor current source M_{31} of (DAC_1) has 121 μA. While the area of each transistor in the transistor-level implementation of the current steering DACs, ($DAC_{3,\ 4,\ 5}$), are designed so that its $NMOS$ transistors current sources have 22.5 μA, 78 μA and 22.5 μA, respectively.

Table 4.5: The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of each transistor in the transistor-level implementation of the current-steering DAC (DAC_1), along with its biasing circuit
.

M_i	W_f	L_f	$N_{fingers}$
M_{31}	1 μm	100 nm	8
$M_{32,\ 33}$	0.5 μm	100 nm	3
$M_{34,\ 35}$	1 μm	100 nm	7
$M_{36,\ 37}$	2.5 μm	100 nm	7
$M_{38,\ 39}$	1 μm	100 nm	4
$M_{40,\ 41}$	1 μm	100 nm	4
M_{42}	2.5 μm	100 nm	10
M_{43}	2.5 μm	100 nm	6

The real delay loop of the transistor-level CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators in Fig. 4.17, which equals approximately 1.6 T_s.

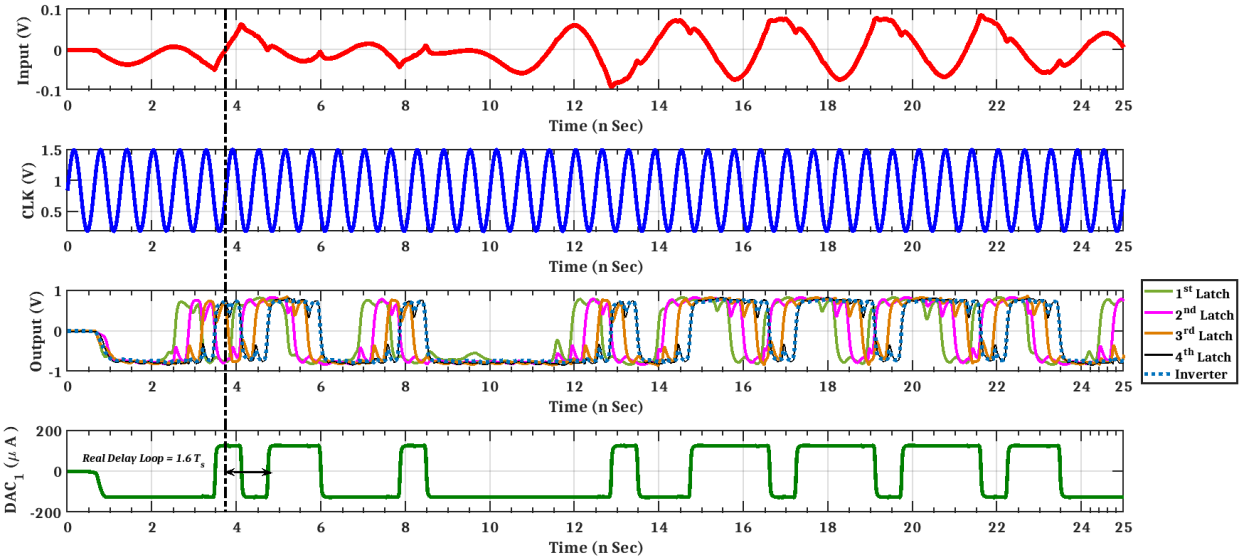

Fig. 4.17: The real delay loop of the transistor-level CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators.

Fig. 4.18 presents the output spectrum of a single-tone transistor-level simulation results of the CT BP $\Sigma\Delta$ Modulator using 2-op-amp resonators centered at $f_0 = 400$ MHz, it is shown before in Fig. 4.5. Using a single-tone sine-wave input, with amplitude equal to 66 mV, the signal to noise ratio (SNR) is 55 dB. Compared to the SNR calculated from our noise study at chapter 3, we lost only 6.8 dB due to the transistor-level implementation of each block in CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators.

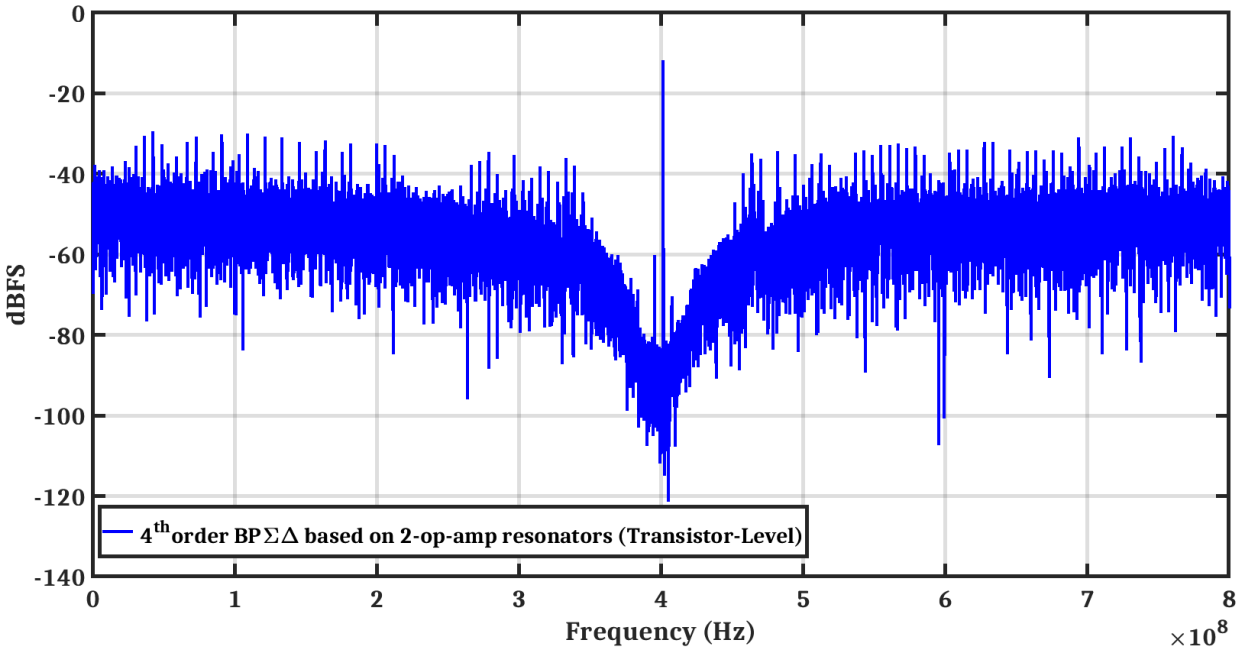

Fig. 4.18: Output spectrum of a single-tone transistor-level of the 4th-order CT BP $\Sigma\Delta$ modulator using a two-op-amp resonator, centered at $f_0 = 400$ MHz.

Fig. 4.19 shows also the output spectrum of a single-tone transistor-level simulation results of the CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators, shown before at Fig. 4.18, in the range of the bandwidth of $\Sigma\Delta$ from f_0 - $\frac{BW_{\Sigma\Delta}}{2}$ to $f_0 + \frac{BW_{\Sigma\Delta}}{2}$ where $BW_{\Sigma\Delta}$ equals to $\frac{f_s}{2 * OSR}$, $f_s = 1.6$ GHz and OSR = 64.

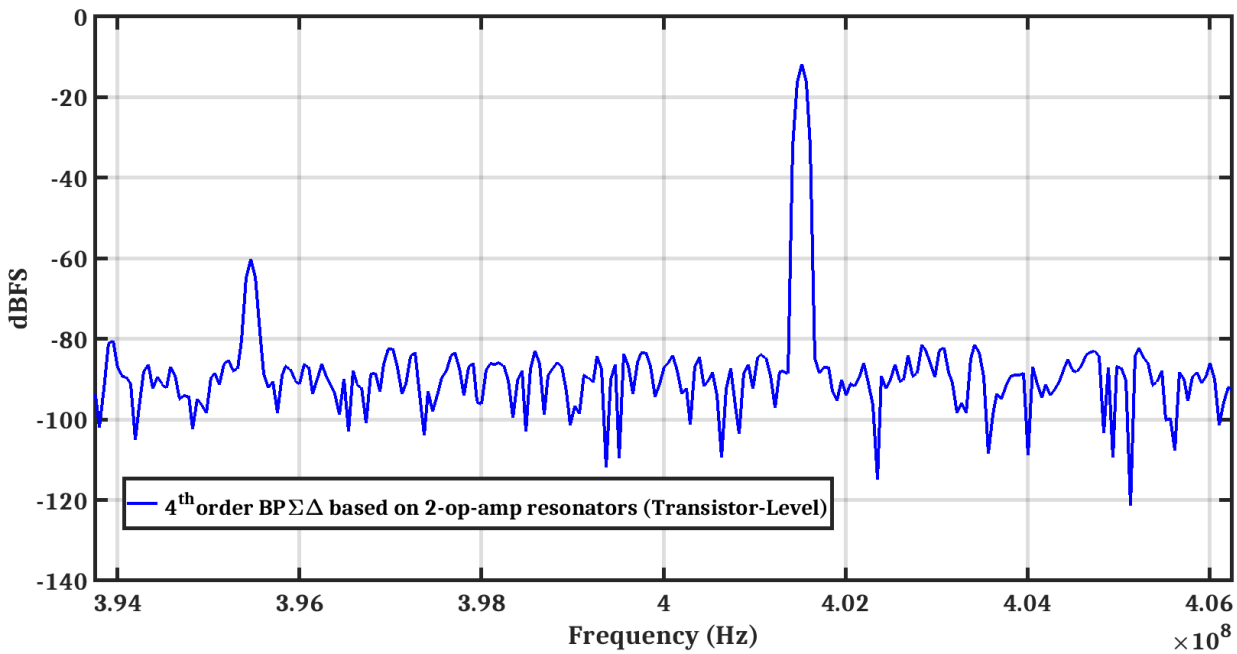

Fig. 4.19: Output spectrum of a single-tone transistor-level of the 4th-order CT BP $\Sigma\Delta$ modulator using a two-op-amp resonator, centered at $f_0 = 400$ MHz, in the range of the bandwidth of $\Sigma\Delta$, from 393.75 MHz to 406.25 MHz.

4.4 The layout-implementation design

The layout-implementation of all main blocks such as the operational amplifier, the 2-op-amp resonator, 1-Bit quantizer and the current steering DACs with its biasing circuit, are presented below:

4.4.1 The operational amplifier

The layout-implementation of the op-amps is shown in Fig. 4.20, where its transistor-level implementation was explained in-details at section 4.3.2.

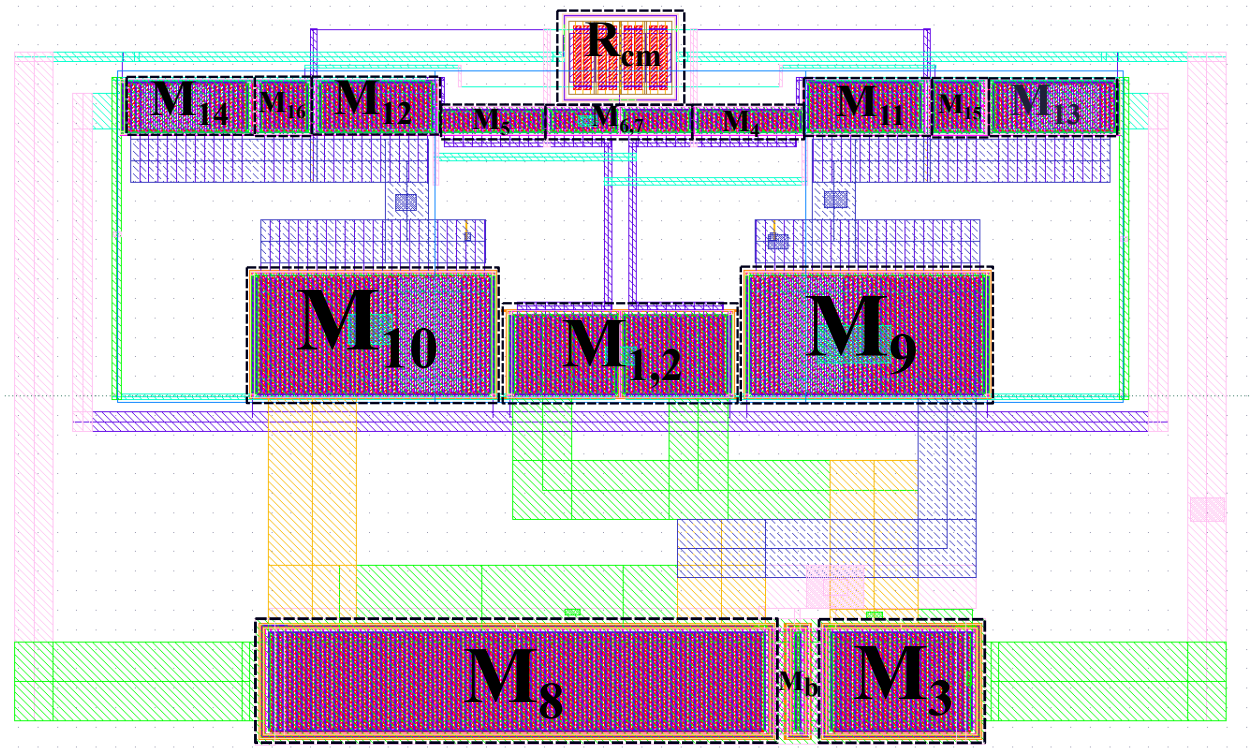

Fig. 4.20: The layout-implementation of the 2-stage feed-forward op-amp.

4.4.2 Two-op-amp resonator

Fig. 4.21 shows the layout-implementation of the integrator for the 2-op-amp resonator where its transistor-level implementation was explained in-details in section. 4.3.1.

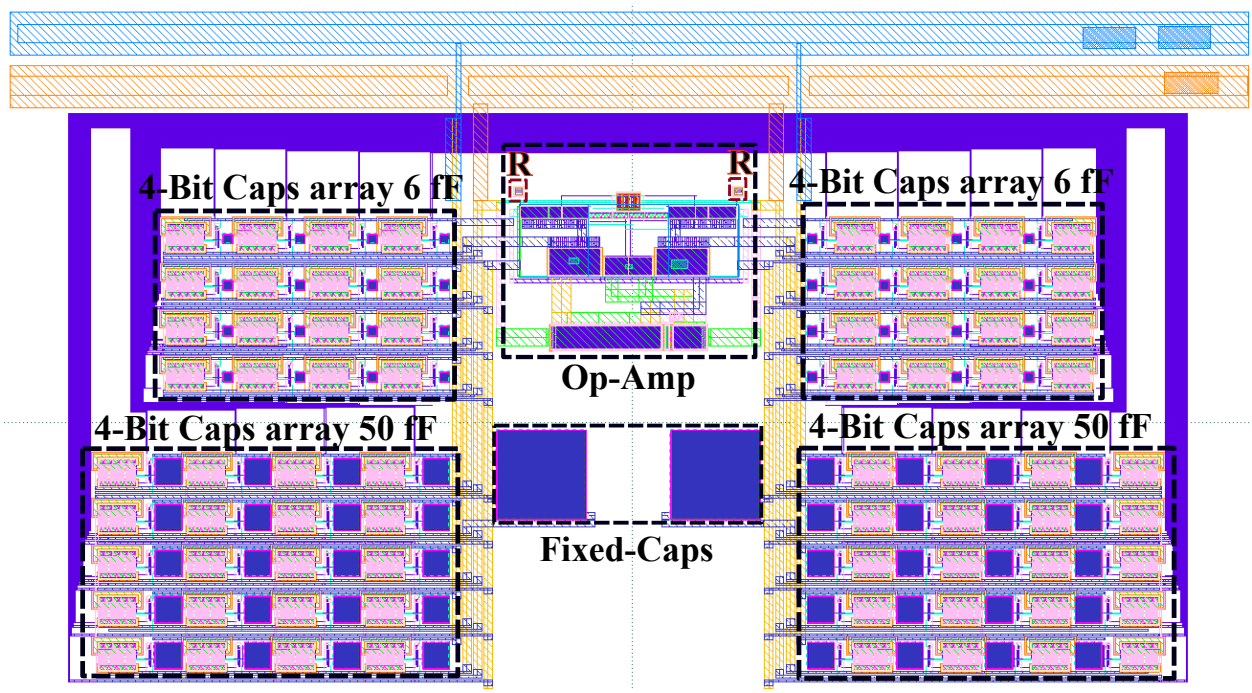

Fig. 4.21: The layout-implementation of the integrator for the two-op-amp resonator.

The area of the PMOS/NMOS transistor, in the transistor-level implementation of the transmission gate shown in Fig. 4.7, was resized to decrease its parasitic-resistance during the post-layout simulations. The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of the PMOS/NMOS transistor in the layout-implementation of the transmission gate are presented in Table 4.6.

Table 4.6: The width per finger, W_f, the length per finger, L_f, and the number of fingers, $N_{fingers}$, of the PMOS/NMOS transistor in the layout-implementation of the transmission gate shown in Fig. 4.7

.

M_i	W_f	L_f	$N_{fingers}$
$M_{NMOS,PMOS}$	1 μm	100 nm	36

Fig. 4.22 presents the post-layout simulation results of the 4th-order loop filter gain centered at $f_0 = 400$ MHz, composed of two 2-op-amp resonators connected in-series. It has two resonance frequencies $f_{01,\ 02} = 394.5\ MHz,\ 405.3\ MHz$, where f_{01} is the resonance frequency of the 1st resonator and f_{02} is the resonance frequency of the 2nd resonator, while the quality factor of the 1st resonator Q_1 is 65.4 and the quality factor of the 2nd resonator Q_2 is 77.2.

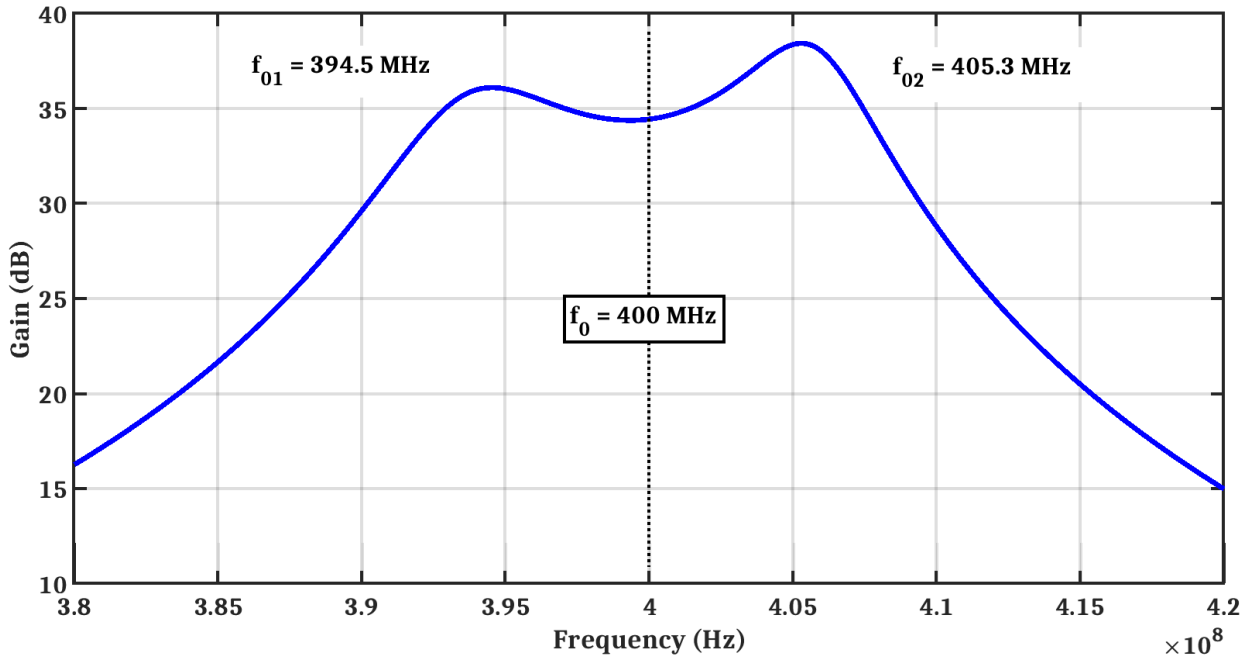

Fig. 4.22: Simulation of the post-layout gain of the 4th-order loop filter using a two-op-amp resonator, two 2-op-amp resonators connected in-series, centered at $f_0 = 400\ MHz$ with two resonance frequencies $f_{01,\ 02} = 394.5\ MHz,\ 405.3\ MHz$ and $Q_{1,2} = 65.4,\ 77.2$.

At post-layout simulations, the quality factory of 2-op-amp resonators $Q_{1,\ 2}$ are decreased, compared to the transistor-level results demonstrated in Fig. 4.11, since additional resistance and additional capacitance are extracted and have an effect on the gain of integrators, mentioned in Eq. 3.28, which leads to decrease the quality factor Q .

4.4.3 1-Bit quantizer

The layout-implementation of the 1-Bit quantizer is shown in Fig. 4.23, where its transistor-level implementation was explained in-details in section 4.3.3.

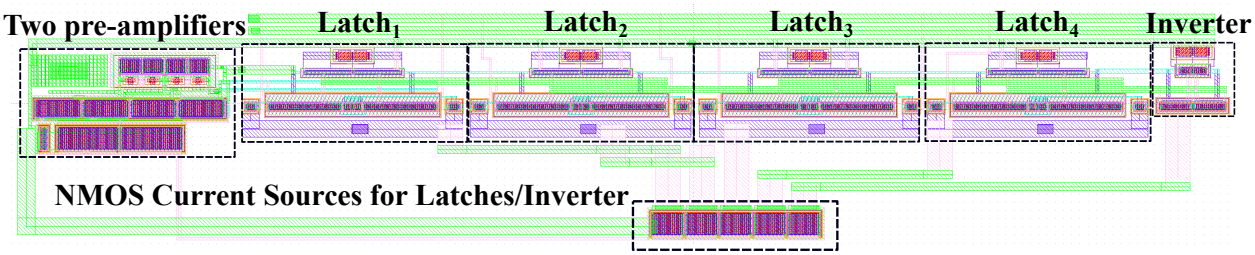

Fig. 4.23: The layout-implementation of the 1-Bit quantizer.

4.4.4 Current steering DACs with its biasing circuit

The layout-implementation of the current steering DACs along with its biasing circuit are shown in Fig. 4.24. where the transistor-level implementation was explained in-details in section 4.3.4.

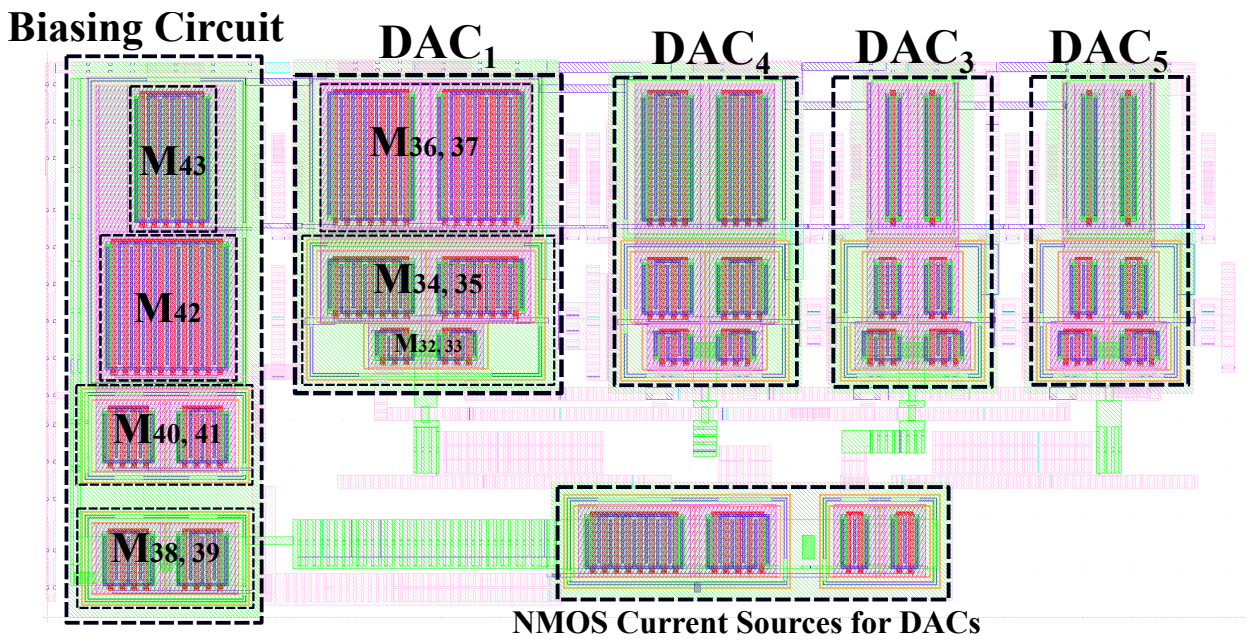

Fig. 4.24: The layout-implementation of the current steering DACs along with its biasing circuit for CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators.

Fig. 4.25 shows the floor-planning of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator design based on 2-op-amp resonators where its circuit-level implementation was presented before in Fig. 4.5. The four integrators are identical. Unfortunately, this floor-planning wasn't verified by Design Rule Checking (DRC), Layout Versus Schematic (LVS) and Parasitic Extraction (PEX) simulations.

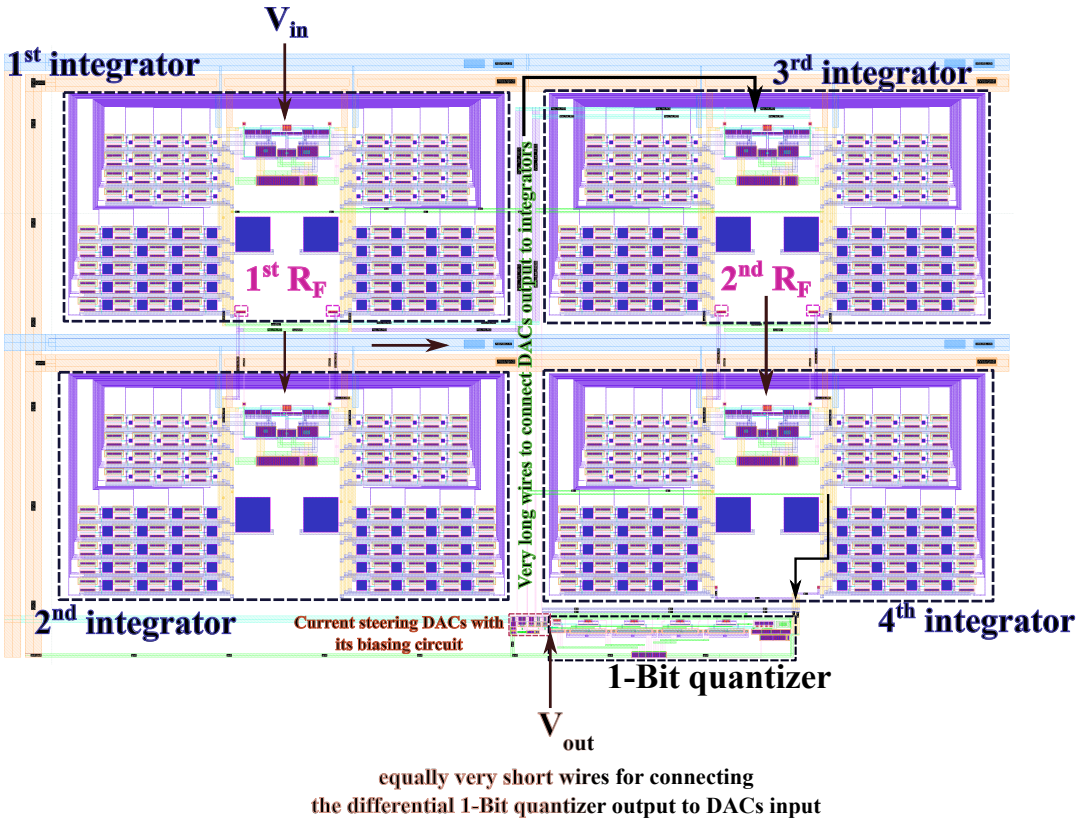

Fig. 4.25: The floor-planning of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator based on 2-op-amp resonators.

Figure 4.26 presents the output spectrum of a single-tone post-layout simulation results of the CT BP $\Sigma\Delta$ Modulator using 2-op-amp resonators centered at $f_0 = 400$ MHz, using a single-tone sine-wave input, with amplitude equal to 66 mV. The signal to noise ratio (SNR) is 53 dB. This SNR is only 2 dB less than the SNR of the transistor-level implementation as shown before in Fig. 4.18.

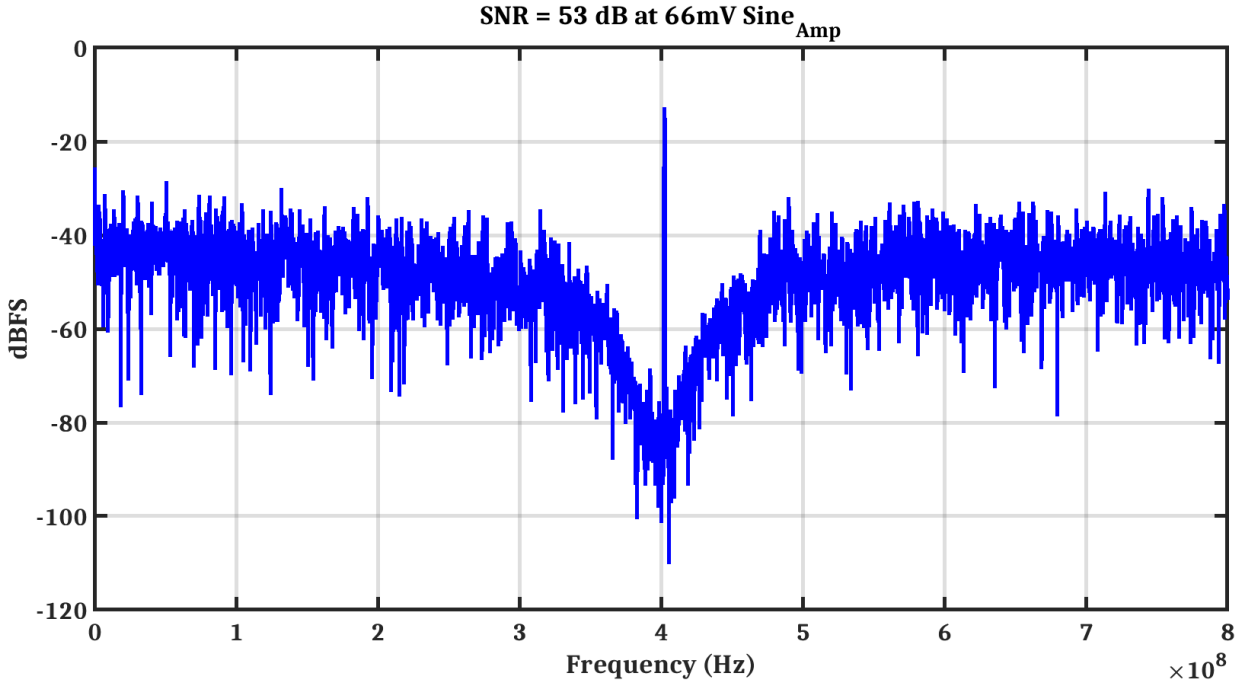

Fig. 4.26: Output spectrum of a single-tone post-layout simulation of the 4th-order CT BP $\Sigma\Delta$ modulator using a two-op-amp resonator, centered at $f_0 = 400$ MHz.

Fig. 4.27 shows also the output spectrum of a single-tone post-layout results of CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators, shown before at Fig. 4.26, in the range of the bandwidth of $\Sigma\Delta$ from f_0 - $\frac{BW_{\Sigma\Delta}}{2}$ to f_0 + $\frac{BW_{\Sigma\Delta}}{2}$ where $BW_{\Sigma\Delta}$ equals to $\frac{f_s}{2 * OSR}$, f_s = 1.6 GHz, OSR = 64. Table 4.7 presents the quality factors $Q_{1,\ 2}$, the resonance frequencies $f_{01,\ 02}$ and the SNR of 2-op-amp resonator $\Sigma\Delta$ at both of the transistor-level/post-layout simulation results.

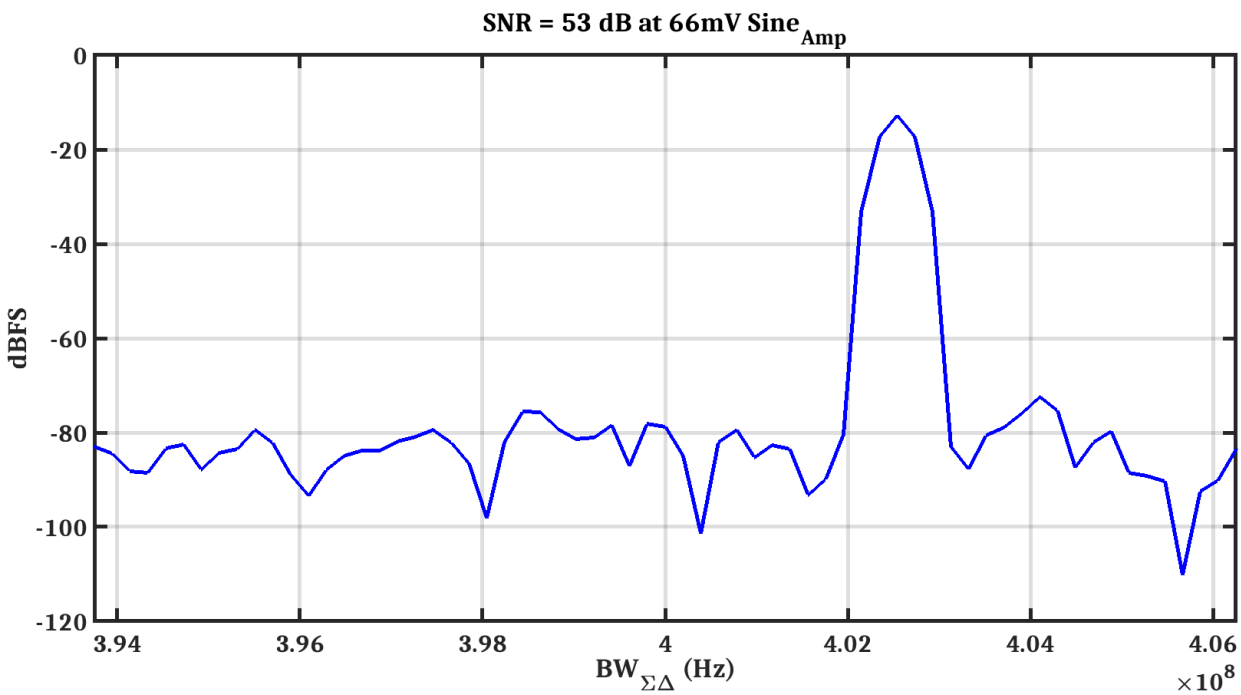

Fig. 4.27: Output spectrum of a single-tone post-layout simulation of the 4th-order CT BP $\Sigma\Delta$ modulator using a two-op-amp resonator, centered at $f_0 = 400$ MHz, in the range of the bandwidth of $\Sigma\Delta$, from 393.75 MHz to 406.25 MHz.

Table 4.7: The quality factors $Q_{1,\ 2}$, the resonance frequencies $f_{01,\ 02}$ and the SNR of 2-op-amp resonator $\Sigma\Delta$: at transistor-level/post-layout simulation results

	The resonators-performance	SNR of $\Sigma\Delta$
Transistor-Level	$Q_{1,2} = 650,\ 193$ $-f_{01,\ 02} = 397.2\ MHz,\ 405.4\ MHz$	55 dB
Post-Layout	$Q_{1,2} = 65.4,\ 77.2$ $-f_{01,\ 02} = 394.5\ MHz,\ 405.3\ MHz$	53 dB

4.5 The post-layout results compared to the state of the art

The performance of the post-layout two-op-amp resonator $\Sigma\Delta$ modulator is summarized in Table 4.8 and compared with the state of the art at the typical corner. Our 2-op-amp resonator $\Sigma\Delta$ modulator design consumes lower power consumption than the state of the

art at a moderate centre frequency $f_0 = 400$ MHz. Our $\Sigma\Delta$ modulator input third order intercept point (IIP3) is the highest. Besides, it has the smallest chip area. We utilized unconditionally stable op-amps with only two stages of DC-gain $A_0 = 35\ dB$, while the state of the art uses conditionally stable op-amps with minimum three stages and a minimum DC-gain $A_0 = 49\ dB$. But our design's figure of merit (FOM) is less than the state of the art since we use only 1-bit quantizer.

Table 4.8: Performance comparison with the state of the art.

		[Shibata12]		[Lu10]		[Yang18]		**This Work**
BP $\Sigma\Delta$	Order − Architecture	6th−Feedback		6th−Feedback		6th−Feedback/Feedforward		4th−**Feedback**
	Center frequency, f_0 (M Hz)	450	1000	200		250		**400**
	Sampling frequency, f_s (M Hz)	4000		800		1000		**1600**
	quantizer	4−bit		2−bit		4−bit		**1−bit**
	Power (mW)	550		160		156.3		**81.1**
	BW (MHz)	100	75	10	20	25		**12.5**
	SNR (dB)	72	63	68.4	62.3	76.1		**53**
	FOM {Eq. 4.2} [Ali10] [dB]	154.6	144.3	146.4	143.3	158.1		**135**
	IIP3 (dBm)/2-tone spacing (MHz)	+8 / 20		x		x		**+21.5 / 3**
	Area (mm^2)	5.5		2.5		x		**0.22**
Op-amp	no. of stages	7		3		4	5	**2**
	DC-gain (dB)	49		59		69	75	**35**
	Gain @ f_0 (dB)	40		40		54.4	62.5	**30**
	f_T (GHz)	15		8		7.21	6.14	**10.4**
	Stability	Conditionally stable		Conditionally stable		Conditionally stable		**Unconditionally stable**
	Power (mW) @ V_{DD}	112 @ 1 V		6.7 @ 1.8 V		19.6 @ 1.2 V	32.4 @ 1.2 V	**18.75 @ 1.5 V**
	Technology	CMOS 65nm		CMOS 180nm		CMOS 65nm		**FDSOI-28nm**
Major Drawback		Off-chip inductor		Off-chip calibration		Transistor-level simulation Results		**Post-layout simulation results**

$$FOM\ (\ dB\ )\ =\ SNR\ (\ dB\ )\ +\ 10\log_{10}(\frac{BW}{Power}) \tag{4.2}$$

4.6 Conclusion

The transistor-level implementation of the two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator was designed using Low V_{TH} devices, that are also called "flipped-well" devices, on fully depleted silicon on insulator (FDSOI) technology. We achieved $SNR = 55\ dB$, which is only 6.8 dB less than the one calculated by our proposed thermal-noise study. At the post-layout simulation results, the quality factors of 2-op-amp resonators are decreased, compared to the transistor-level implementation simulation results, since additional resistance and additional capacitance are extracted and have an effect on the gain of integrators. The post-layout SNR is 53 dB which is only 2 dB less than the SNR of the transistor-level implementation. Let us study the complete in-detailed design of 1-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator, in next chapter, to accomplish the comparison of both two types of CT BP $\Sigma\Delta$ modulators as we proposed.

Chapter 5

One-op-amp resonator CT BP $\Sigma\Delta$ Modulator design

5.1 Introduction

In this chapter, we present the complete design of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator.

First in section 5.2, the op-amps DC-gain "A_0" effect on both the quality factor "Q" and the resonance frequency "f_0" of the 1-op-amp resonator, along with the SNR of the 1-op-amp resonator CT BP $\Sigma\Delta$ modulator is introduced. Second in section 5.3, we discuss the system-level of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Third in section 5.4, we present the transistor-level implementation design of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Then in section 5.5, we present the layout implementation design of the one-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator. Finally, we compare the post-layout results to the state of art, in section 5.6.

5.2 The effect of op-amps DC-gain "A_0"

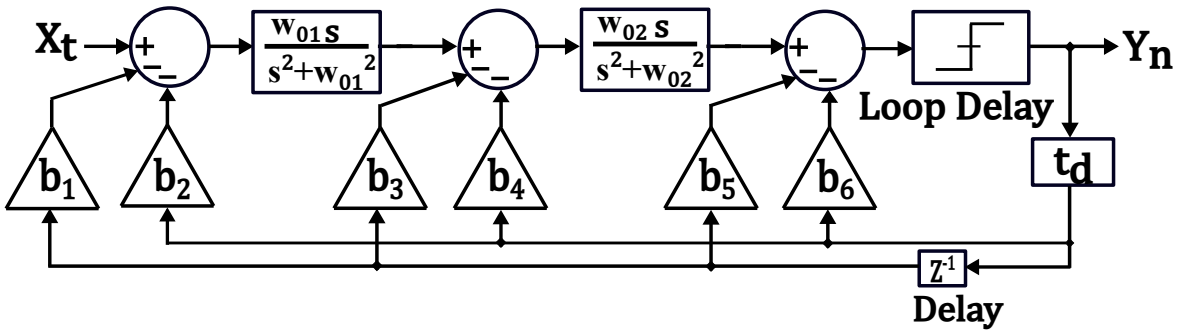

Fig. 5.1: A 4th-order CT BP $\Sigma\Delta$ modulator using a one-op-amp resonator.

Fig. 5.1 shows the block diagram of a 4th-order CT BP $\Sigma\Delta$ modulator using a one-op-amp resonator. The circuit realization of the one-op-amp resonator circuit is shown in Fig. 5.2. As for the case of the two-op-amp resonator, we assume a finite DC gain, A_0, and an infinite 1st pole, f_p, for the op-amp.

Taking $\frac{1}{R_pC_p}=\frac{1}{R_1C_1}=\frac{1}{R_2C_2}$, to be a function of the tuneable capacitors values, $C_{1,2}$, the one-op-amp resonator transfer function can be written at $A_0 \gg 1$ as follows:

$$
\begin{aligned}
\frac{V_{out}(s)}{V_{in}(s)} &= \frac{N}{D}, where \\
N &= \frac{R_1}{R_{in}}.s.\frac{1}{R_1C_1}, and \\
D &= s^2 \\
&\quad +s\Big\{(1+\frac{1}{A_0}).\frac{1}{R_1C_1}+(1+\frac{1}{A_0}).\frac{1}{R_2C_2} \\
&\quad +(-1+\frac{1}{A_0}).\frac{1}{R_2C_1}+\frac{1}{R_{in}C_1A_0})\Big\} \\
&\quad +s^0\Big\{\frac{1}{R_2C_1C_2}(\frac{1}{R_1}+\frac{1}{R_{in}A_0})\Big\}
\end{aligned}
\tag{5.1}
$$

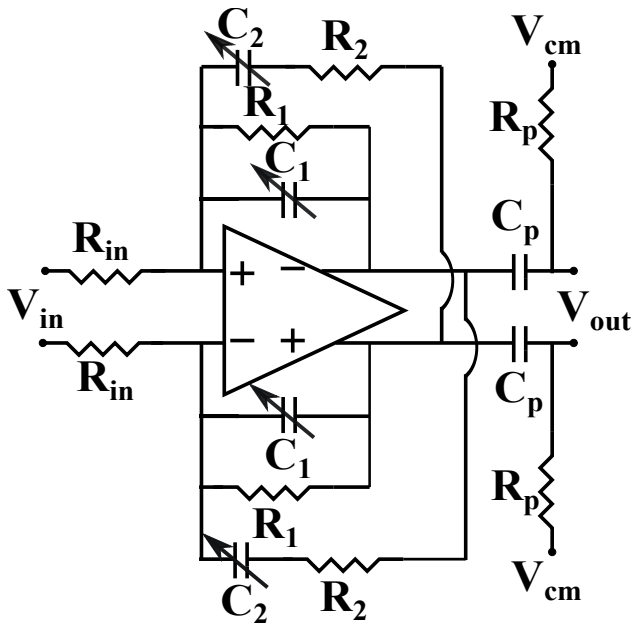

Fig. 5.2: The one-op-amp resonator circuit.

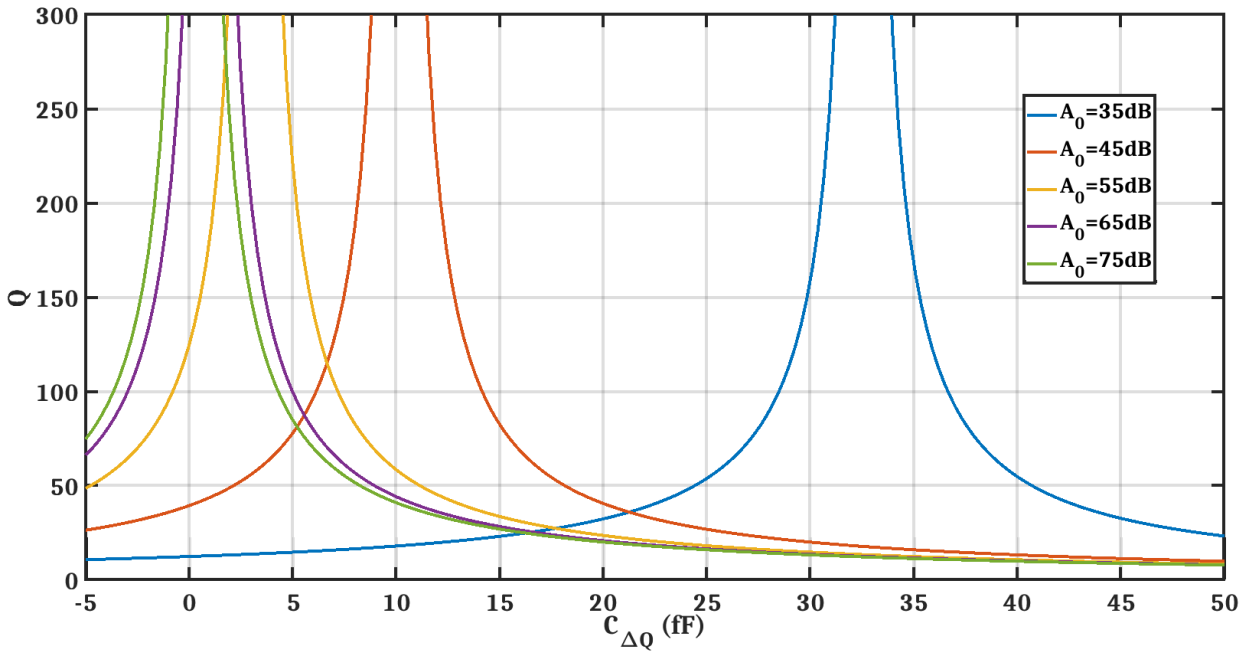

Fig. 5.3: The quality factor Q versus C_{Δ_Q} for different values of the op-amp DC-gain, A_0, from 35 dB to 75 dB at a step of 10 dB.

In the ideal case presented in [Jang18], by taking C_2=$2C_1$ and R_2=$\frac{1}{2}R_1$, the coefficient of s^1 in the denominator of Eq. 5.1 is null and an infinite quality factor is achieved. In these conditions, the centre frequency, is determined by the coefficient of s^0 and is given by $\omega_0 = \frac{1}{R_1C_1} = \frac{1}{R_2C_2}$.

In a non-ideal case, where we have a finite DC-gain for the op-amp, the conditions to nullify s^1 in the denominator of Eq. 5.1 and to obtain an infinite quality factor are changed and we need to modify the capacitors C_1 and C_2 in the following manner:

$$C_1 = \frac{1}{2\pi f_0 R_1} - C_{\Delta_Q}, \quad C_2 = \frac{1}{2\pi f_0 R_2} + 2\ .\ C_{\Delta_Q} \tag{5.2}$$

where $-C_{\Delta_Q}$ and $2\ .\ C_{\Delta_Q}$ are additional terms added to the capacitors C_1 and C_2 respectively to take into account the effect of the finite DC-gain of the op-amp A_0.

Using Eq. 5.1 and Eq. 5.2, it is possible to calculate the value of C_{Δ_Q} that nullifies the

coefficient of s^1 in the denominator of Eq. 5.1 and hence achieve the maximum quality factor for the one-op-amp resonator.

Fig. 5.3 shows that it is possible to calculate C_{Δ_Q} that achieves the maximum quality factor, Q, for different values of the op-amp DC-gain, A_0. This Figure also shows that for a very high op-amp DC-gain, $A_0 \geq 75$ dB, the value of C_{Δ_Q} is close to zero. This explains, the very high op-amp DC gain used in previous implementations of Bandpass $\Sigma\Delta$ ADCs based on one-op-amp resonator [Jang18].

In this work, we propose to use a moderate op-amp DC-gain. From Fig. 5.3, for $A_0 = 35$ dB, we need to add a C_{Δ_Q} of 32.5 fF in order to achieve an infinite quality factor. In Fig. 5.4, we study the sensitivity of the resonator's quality factor with respect to any variation in C_{Δ_Q}. These results are obtained using $A_0 = 35$ dB, the resistors values $R_{in} = 1000\ \Omega$, $R_1 = 500\ \Omega$, $R_2 = 250\ \Omega$, $R_p = 1591\ \Omega$, the capacitors values $C_p = 100$ fF to slightly load on the op-amp, $C_1 = 795.8$ fF, $C_2 = 1591.5$ fF and C_{Δ_Q} in a range of between 25 fF to 41 fF.

Notice from Fig. 5.4, that high quality factors, ≥ 100, can be achieved for values of C_{Δ_Q} in a range of between 29 fF to 35 fF, despite the moderate value of the op-amp DC gain. It is also worth noting that there is very little variation in the value of the centre frequency.

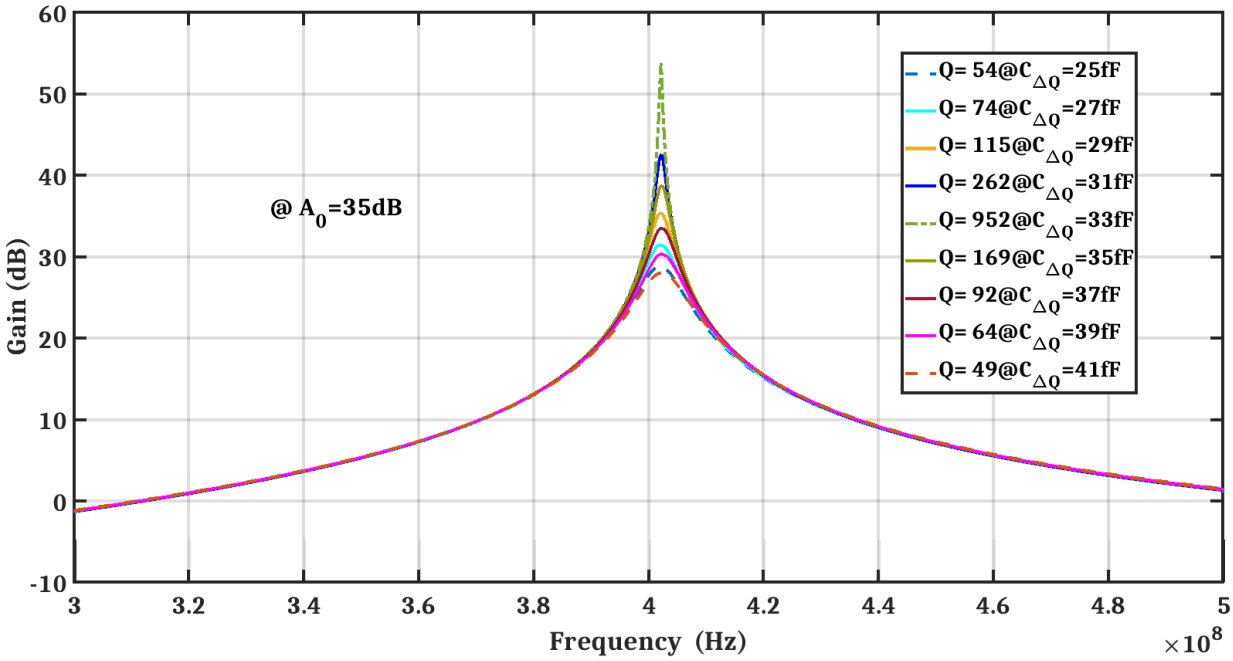

Fig. 5.4: The gain of one-op-amp resonator (Eq. 5.1) centered at $f_0 \approx 400$MHz with op-amp DC gain, $A_o = 35dB$, with an infinite 1st pole, f_p, and the capacitor, C_{Δ_Q}, varying from 25fF to 41fF at a step of 2fF.

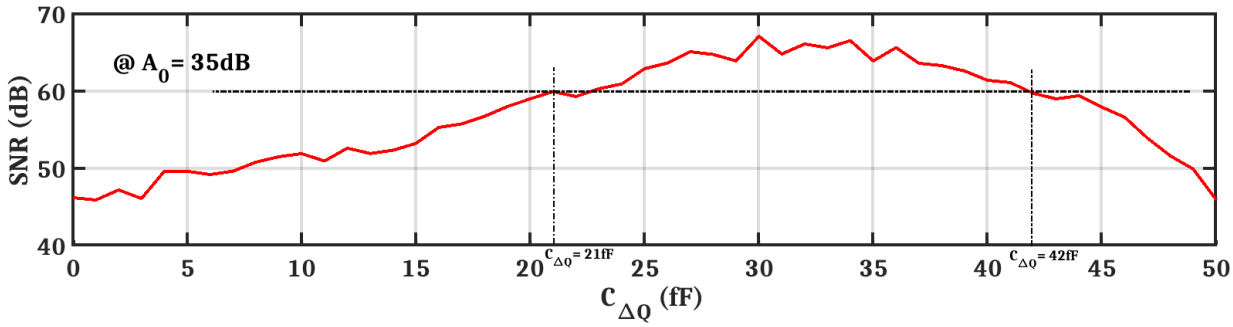

Fig. 5.5: The maximum SNR versus the value of C_{Δ_Q} for a 4th-order one-opamp resonator BP $\Sigma\Delta$ modulator presented in Fig. 5.1.

In Fig. 5.5, we show the effect of any deviation from the optimal value of C_{Δ_Q} on the maximum SNR of a 4th order BP $\Sigma\Delta$ modulator based on one-op-amp resonators. These

matlab simulations measure the SNR for an OSR of 64 and are based on the model of the feedback architecture, illustrated in Fig. 5.1, where each resonator is modeled using Eq. 5.1 and Eq. 5.2. From this Figure, we can see that the maximum SNR is achieved for C_{Δ_Q} in a range of between 30 fF to 35 fF and that we can achieve an SNR higher than 60 dB when C_{Δ_Q} is in a range of between 21 fF to 42 fF. That is why we have to design a fine-trimming circuit implementing the capacitors values $C_{1,\ 2}$ discussed later at section 5.4.1.
As newly discussed in this section, the quality factor sensitivity to the RC network capacitors at limited op-amp DC-gain A_0 has been analyzed for the one-op-amp resonator. Besides, the influence of the RC network capacitors at limited op-amp DC-gain A_0 on the maximum SNR of a 4th-order CT BP $\Sigma\Delta$ modulator based on one-op-amp resonators has been well discussed.

5.3 The system level

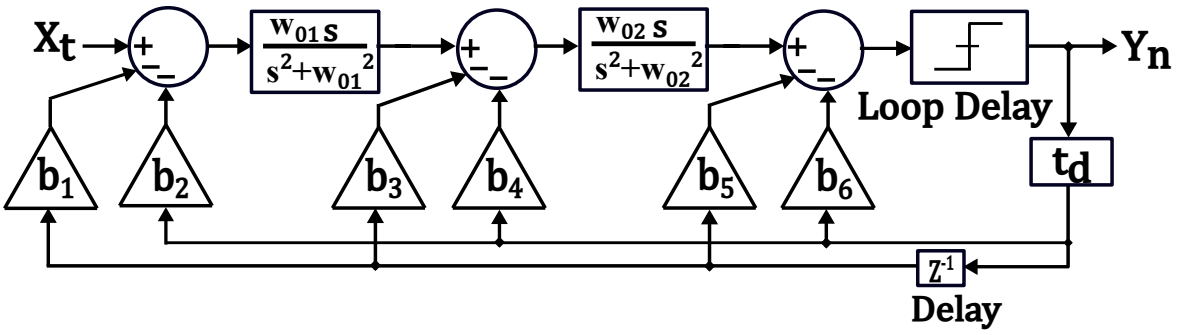

Fig. 5.6: A 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using one-op-amp resonators, taken from Schreier toolbox.

Fig. 5.6 presents the block diagram of the 4th-order CT BP $\Sigma\Delta$ modulator using one-op-amp resonators, taken from Schreier toolbox. Table 5.1 demonstrates the values of the feedback coefficients presented in Fig. 5.6 and its values where used in the transistor-level

Table 5.1: The values of the feedback coefficients presented in Fig. 5.6 (before scaling) and its values where used in the transistor-level implementation (after scaling) using $b_{1,\ 3,\ 5} = 0.0$ at $t_d = 1.5\ T_s$ and $w_{01,\ 02} = 2\ \pi\ (f_s/4)$.

after scaling	before scaling
$b_2{}^* = -\ 43\ \cdot\ 10^{-6}$	$b_2 = -\ 0.0967$
$b_4{}^* = -\ 76\ \cdot\ 10^{-6}$	$b_4 = -\ 0.5479$
$b_6{}^* = -\ 15.5\ \cdot\ 10^{-6}$	$b_6 = -\ 0.3165$
$X_t{}^* = -29$ dB	$X_t = -26.4$ dB

implementation design after we applied the same scaling technique discussed in chapter 3 at section 3.2.

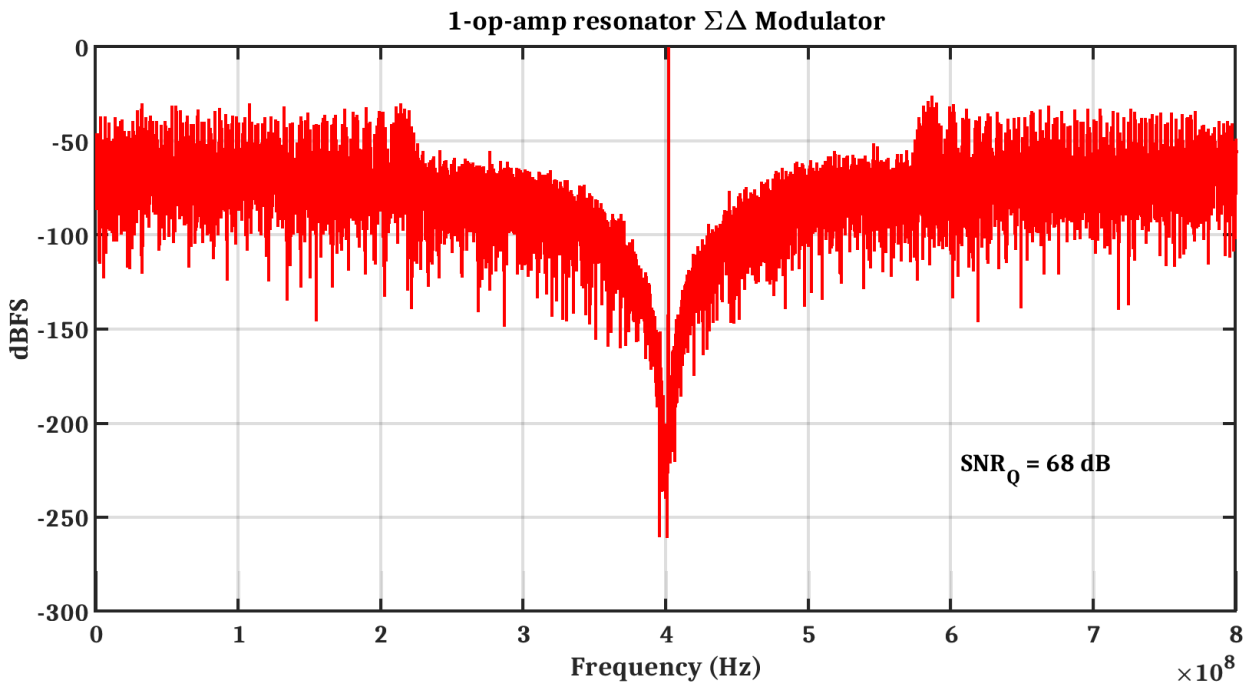

Fig. 5.7: The output spectrum of an ideal model for 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using one-op-amp resonators of Fig. 5.6, simulated by MATLAB.

In Fig. 5.7, we present the output spectrum of an ideal model for 4th-order CT BP $\Sigma\Delta$ modulator using one-op-amp resonators, simulated by MATLAB of Fig. 5.6. These MATLAB simulations measure the maximum signal to quantization ratio (SNR_Q) of 68 dB.

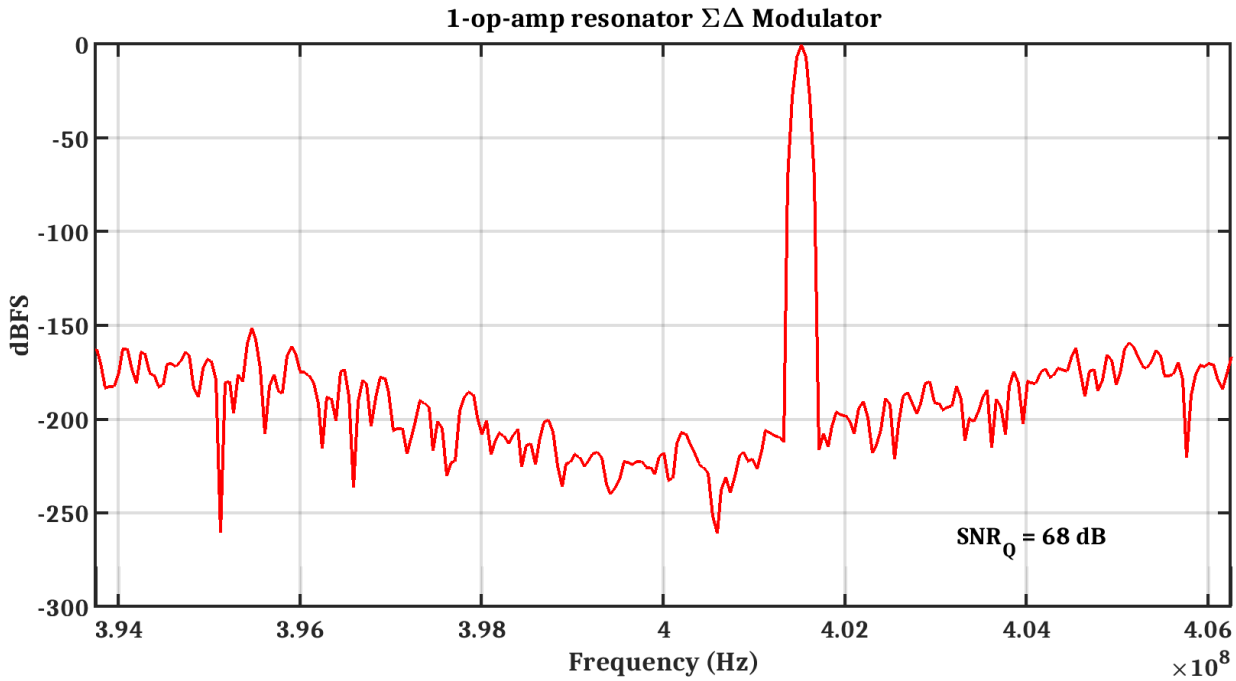

Fig. 5.8: The output spectrum of an ideal model for 4th-order continuous-time bandpass $\Sigma\Delta$ modulator using one-op-amp resonators, simulated by MATLAB of Fig. 5.6, in the bandwidth of $\Sigma\Delta$ modulator, from 393.75 MHz to 406.25 MHz.

In Fig. 5.8, we present the output spectrum of an ideal model for 4th-order CT BP $\Sigma\Delta$ modulator using one-op-amp resonators, simulated by MATLAB of Fig. 5.6, in the bandwidth of $\Sigma\Delta$ modulator, from 393.75 MHz to 406.25 MHz.

5.4 The transistor-level implementation design

Fig. 5.9 shows the circuit-level implementation of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator design based on 1-op-amp resonators.

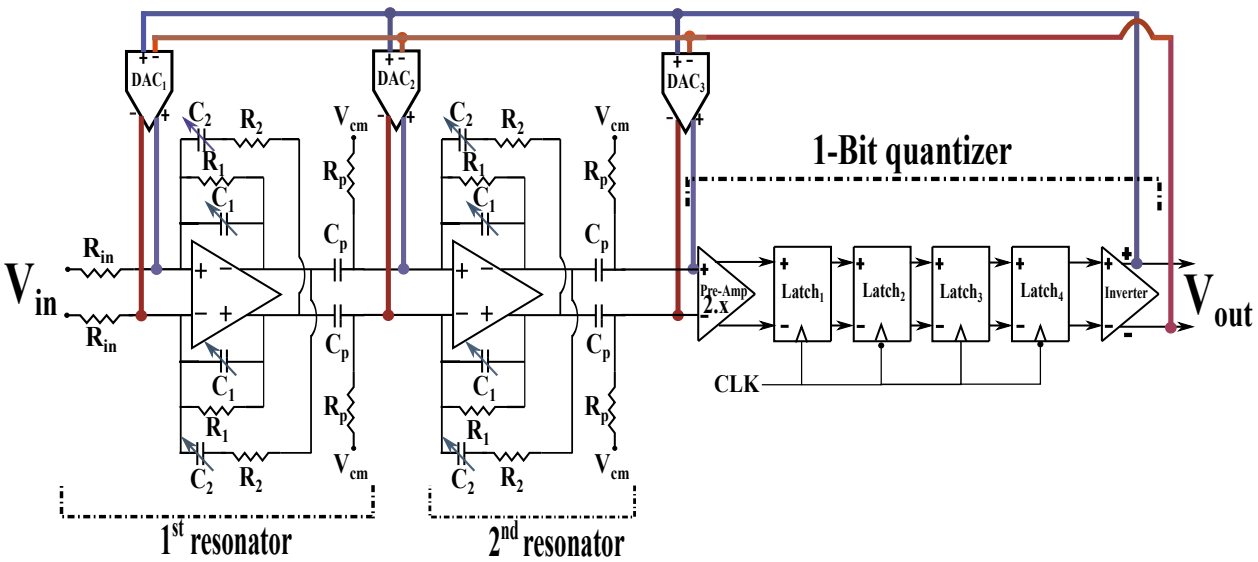

Fig. 5.9: The circuit-level implementation of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator based on 1-op-amp resonators.

In Fig. 5.9, two 1-op-amp resonators are connected in series through resistors and capacitors in order for the op-amp output of the 1st resonator to directly drive the input of the 2nd resonator through the capacitor C_p. Three feedback paths through current steering DACs connect the 1-Bit quantizer output to the input node of each op-amp starting from the 1st op-amp to the 2nd op-amp and the input node of the 1-Bit quantizer, respectively. The main blocks are the one-op-amp resonator, 1-Bit quantizer and the current steering DACs. All blocks are designed also on 28 nm FD-SOI technology using Low V_{TH} devices, that are also called "flipped-well" devices.

5.4.1 One-op-amp resonator

The circuit realization of the one-op-amp resonator is presented in Fig. 5.9. The values of resistors and capacitors are $R_{in} = 1000\ \Omega$, $R_1 = 500\ \Omega$, $R_2 = 250\ \Omega$, $R_p = 1591\ \Omega$ and $C_p = 100$ fF, mentioned in chapter 5 at section. 5.2.

Using the transistor-level implementation of the op-amps with finite DC gain, A_0, and a

finite bandwidth, we need to modify the capacitors C_1 and C_2 in the following manner:

$$C_1 = \frac{1}{2\pi f_0 R_1} - C_{\Delta_Q} + C_{\Delta_{f_0}}, \quad C_2 = \frac{1}{2\pi f_0 R_2} + 2.C_{\Delta_Q} + C_{\Delta_{f_0}} \tag{5.3}$$

where $-C_{\Delta_Q}$, $2C_{\Delta_Q}$ and $C_{\Delta_{f_0}}$ are additional terms added to the capacitors C_1 and C_2 respectively to accomplish a high quality factor at a certain value of the centre frequency f_0. As shown in Fig. 5.10 and Fig. 5.11, the capacitors $C_{1,\ 2}$ are implemented by fixed caps that equal to 473 fF and 1633 fF, respectively. Each of the fixed caps of $C_{1,\ 2}$ is in parallel with a trimming capacitor that is composed of two variable-capacitor (varactor) in parallel. The 1st varactor has a capacitance range from $107fF$ to $310fF$. While the 2nd varactor has a capacitance range from $16.7fF$ to $38.3fF$. Each varactor operates by a DC voltage, $V_{DC_{1a,\ 1b,\ 2a,\ 2b}}$, supplied from a 7-Bit Digital to Analog Converter (DAC) with -1.8V/1.8V supply voltage rails.

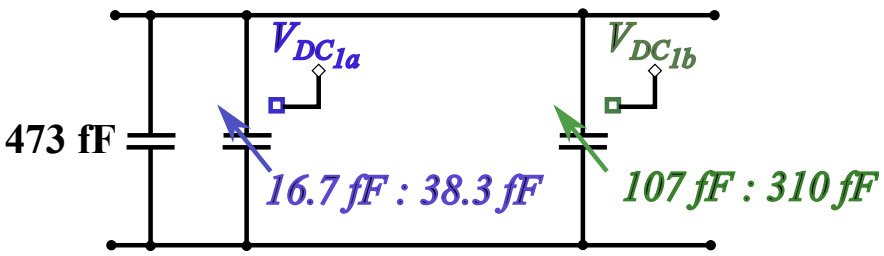

Fig. 5.10: The capacitor C_1 for the 1-op-amp resonators presented in Fig. 5.9

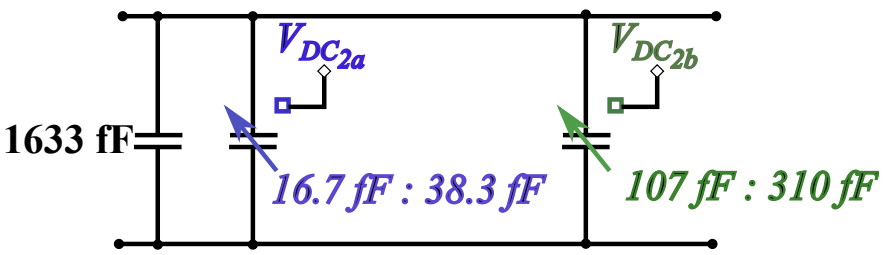

Fig. 5.11: The capacitor C_2 for the 1-op-amp resonators presented in Fig. 5.9

The transistor-level implementation of the op-amps for 1-op-amp resonators is the same design as the one for the 2-op-amp resonators mentioned in-details in chapter 4 at section 4.3.2.

For the RC network using the transistor-level implementation of the op-amps in case of the one-op-amp resonator, the resistors values are $R_{in} = 1000\ \Omega$, $R_1 = 500\ \Omega$, $R_2 = 250\ \Omega$, $R_p = 1591\ \Omega$, mentioned in chapter 5 at section. 5.2.

Taking into account the op-amp poles, the capacitors values are $C_1 = 645$ fF, $C_2 = 1662$ fF and $C_p = 100$ fF.

In Fig. 5.12, the op-amp achieves a DC-gain $A_0 = 34.4$ dB, a unity-gain frequency, $f_T = 15.2$ GHz, and a phase margin, $PM = 51°$, when loaded with this RC network.

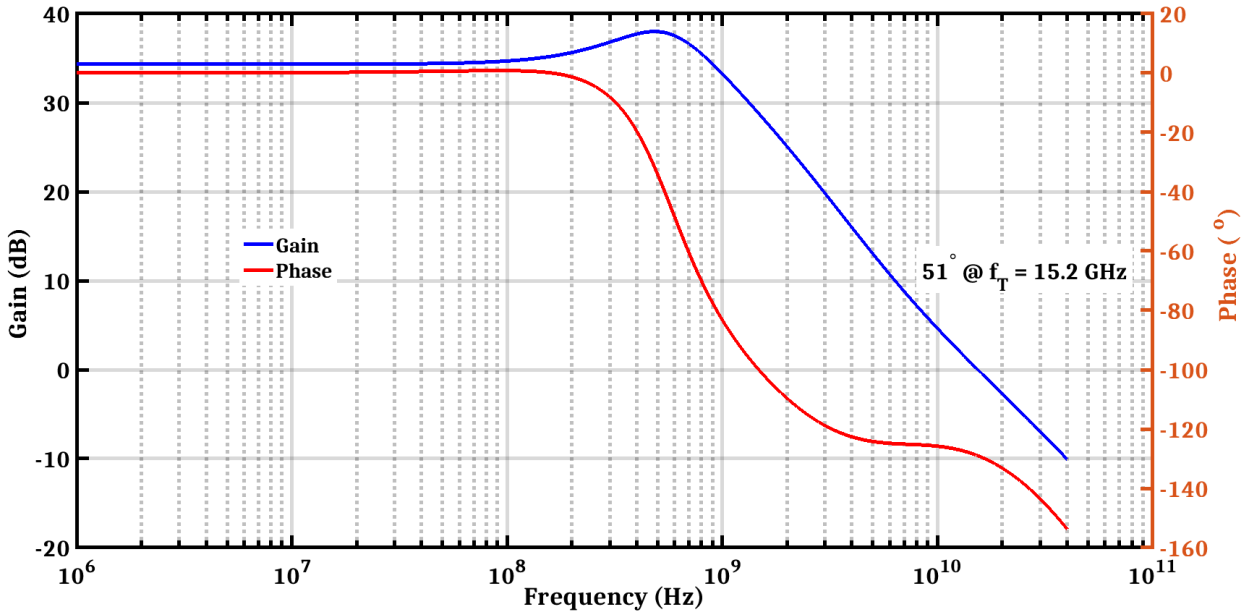

Fig. 5.12: Frequency response of the transistor level 2-stage feed forward op-amp, explained in-details in chapter 4 at section 4.3.2, loaded with the RC network of the one-op-amp resonator.

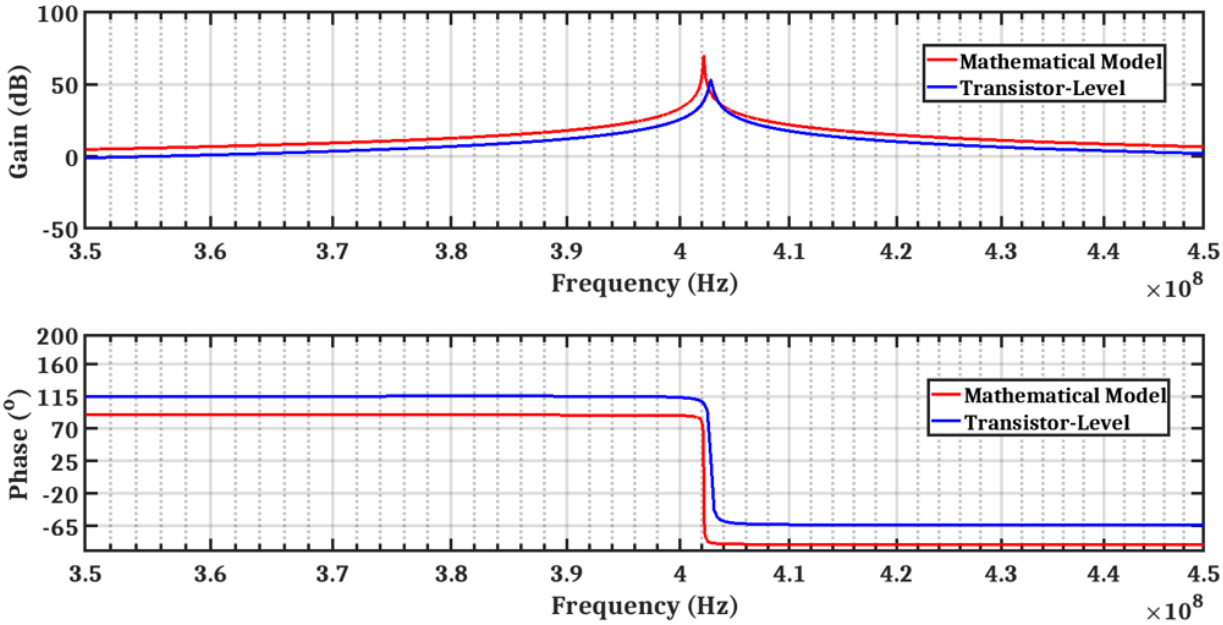

Fig. 5.13: The gain/phase of a single one-op-amp resonator, using the mathematical model of Eq. 5.1 at $C_{\Delta_Q} = 32.5\ fF$ and the transistor-level simulation results.

Fig. 5.13 presents the gain/phase of a single one-op-amp resonator, using the mathematical model of Eq. 5.1 at $C_{\Delta_Q} = 32.5\ fF$ and the transistor-level simulation results. We find a difference of phase which equals to 25°.

Fig. 5.14 presents the transistor-level simulation results of the 4th-order loop filter gain centered at $f_0 \approx 400$ MHz, composed of two 1-op-amp resonators connected in-series. The quality factor of the 1st resonator Q_1 is $> 10^3$ and the quality factor of the 2nd resonator Q_2 is $> 10^3$.

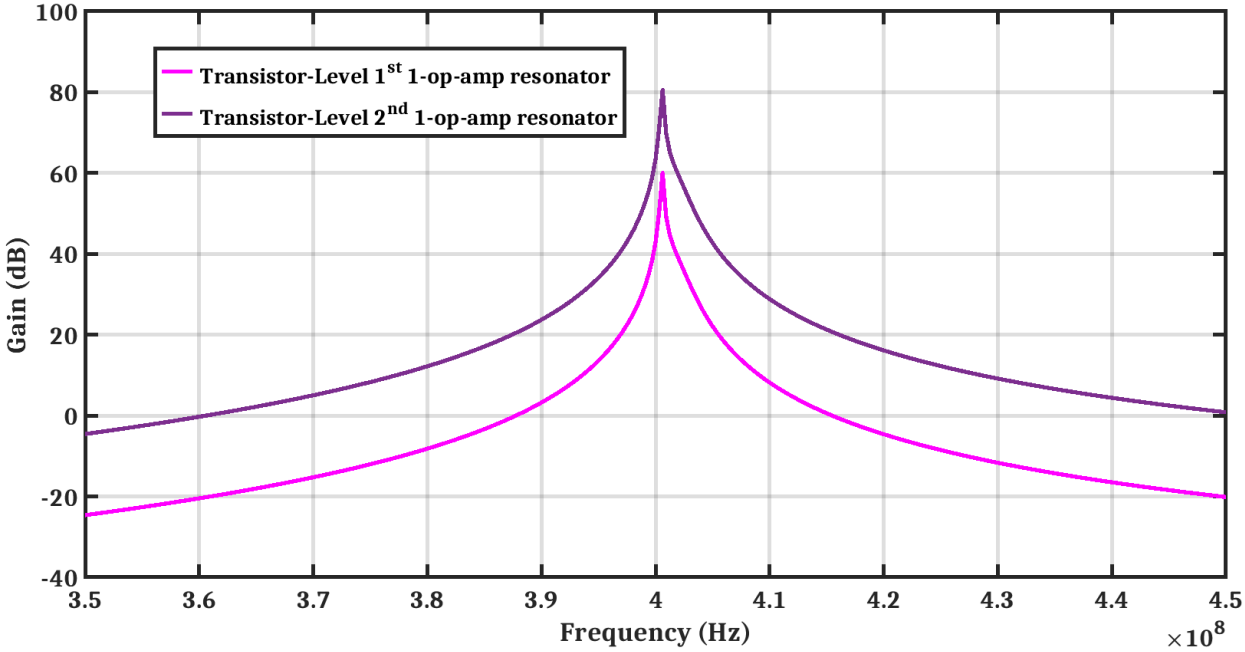

Fig. 5.14: The transistor-level gain of the 4th-order loop filter using a one-op-amp resonator, two 1-op-amp resonators connected in-series, centered at $f_0 \approx 400\ MHz$ and $Q_{1,2} > 10^3$.

5.4.2 1-Bit quantizer

In Fig. 5.9, the 1-Bit quantizer block is composed of two pre-amplifiers followed by four Source-Coupled-Logic (SCL) latches ($Latch_1$, $Latch_2$, $Latch_3$ and $Latch_4$) having inverted clock signals, which facilitates an excess loop delay of 1.5 T_s [Sayed20b].
The transistor-level implementation of the pre-amplifier, SCL latches and the inverter are the same topologies as for CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators in section 4.3.3.

5.4.3 Current steering DACs

The transistor-level implementation of the current steering DAC is the same topology as the one for CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators in section 4.3.4, but the area of each transistor in the transistor-level implementation of the current steering DACs, ($DAC_{1,\ 2,\ 3}$), are designed so that its $NMOS$ transistors current sources have 86 μA, 152 μA and 31 μA,

respectively.

Fig. 5.15 presents the output spectrum of a single-tone transistor-level simulation results of the CT BP $\Sigma\Delta$ modulator using 1-op-amp resonators centered at $f_0 = 400$ MHz, shown before in Fig. 5.9, using a single-tone sine-wave input, with amplitude equal to 35.4 mV. The SNR is 41 dB. It is lower than the SNR of the transistor-level implementation of two-op-amp resonator CT BP $\Sigma\Delta$ modulator, in Fig. 4.18. It happened due to the low linearity of 1-op-amp resonators that comes from the positive feedback connection through the resistor R_2 and the capacitor C_2.

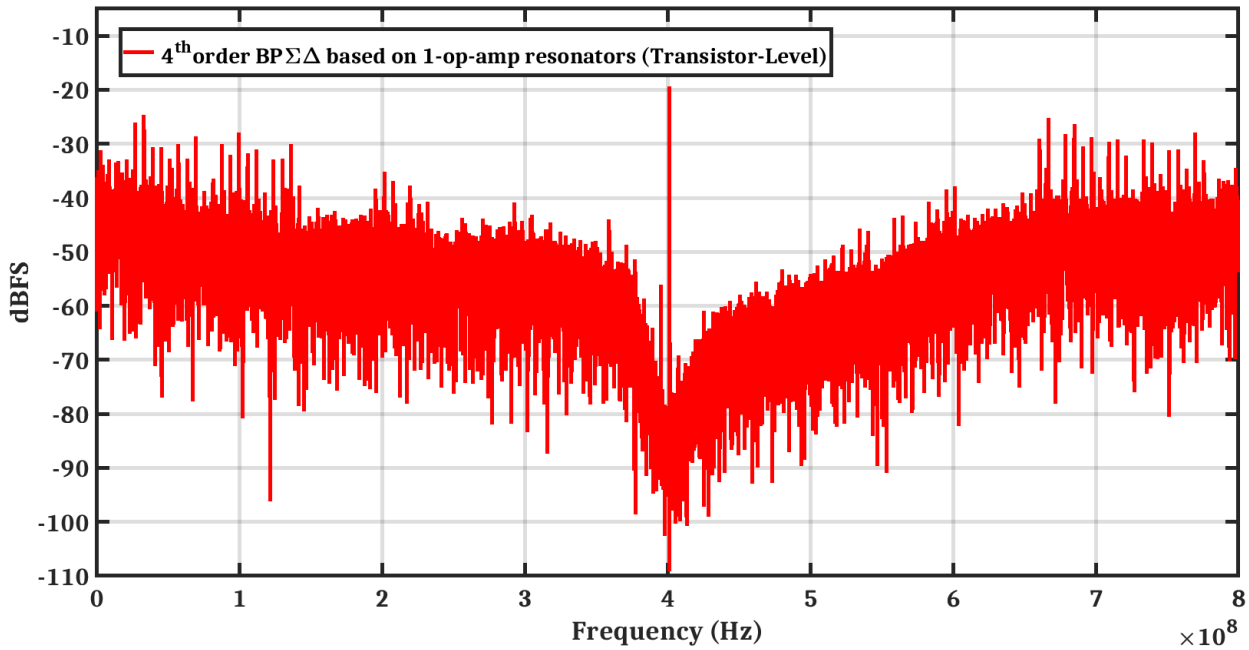

Fig. 5.15: Output spectrum of a single-tone transistor-level simulation results of the 4th-order CT BP $\Sigma\Delta$ modulator using a one-op-amp resonator, centered at $f_0 = 400$ MHz.

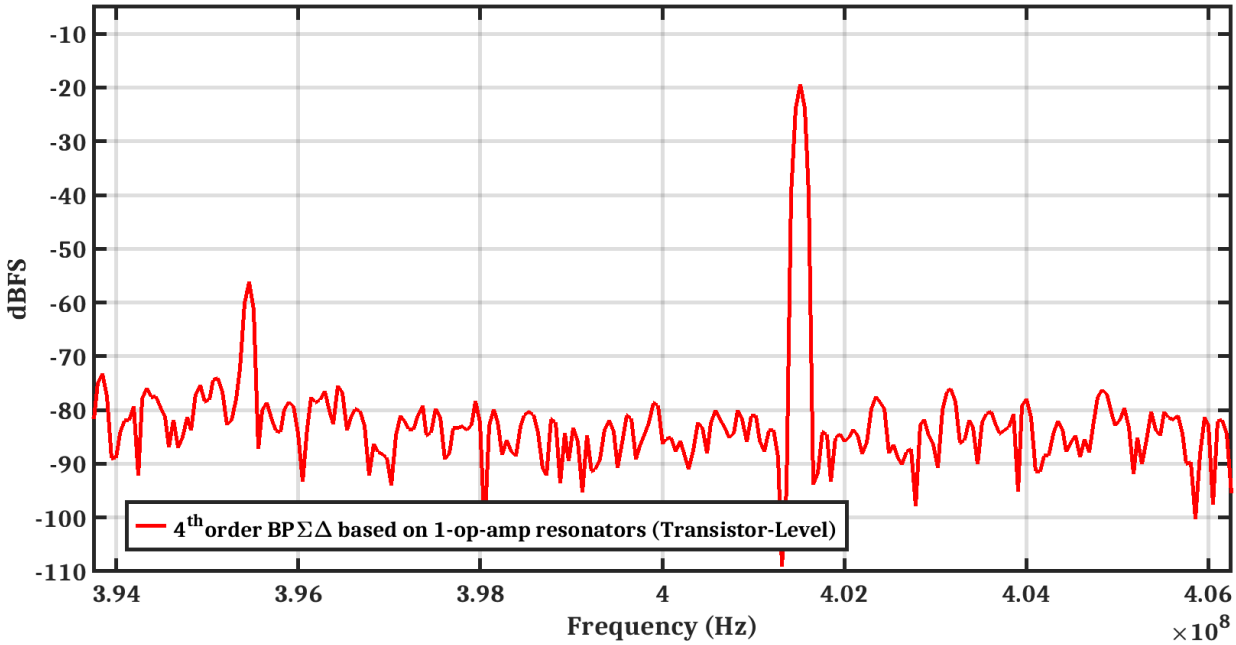

Fig. 5.16: Output spectrum of a single-tone transistor-level simulation results of the 4th-order CT BP $\Sigma\Delta$ modulator using a one-op-amp resonator, centered at f_0 = 400 MHz, in the range of the bandwidth of $\Sigma\Delta$, from 393.75 MHz to 406.25 MHz.

Fig. 5.16 shows also the output spectrum of a single-tone transistor-level simulation results of the 4th-order CT BP $\Sigma\Delta$ modulator using 1-op-amp resonators, shown before at Fig. 5.15, in the range of the bandwidth of $\Sigma\Delta$ from f_0 - $\frac{BW_{\Sigma\Delta}}{2}$ to $f_0 + \frac{BW_{\Sigma\Delta}}{2}$ where $BW_{\Sigma\Delta}$ equals to $\frac{f_s}{2 * OSR}$, f_s = 1.6 GHz, OSR = 64.

5.5 The layout implementation design

The layout-implementation of all main blocks such as the 1-op-amp resonator, the 1-Bit quantizer and the current steering DACs with its biasing circuit, are presented below:

5.5.1 One-op-amp resonator

Fig. 5.17 shows the layout-implementation of the 1-op-amp resonator where its transistor-level implementation was explained in-details in section. 5.4.1.

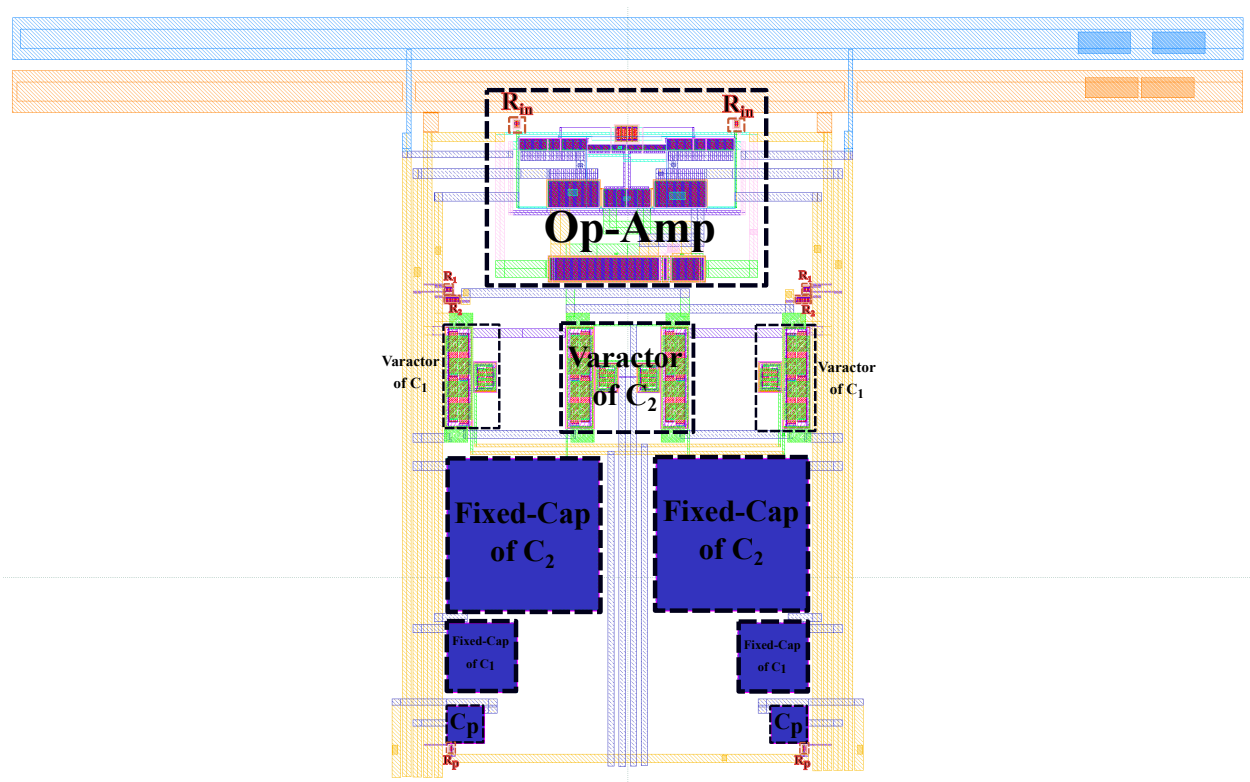

Fig. 5.17: The layout-implementation of the one-op-amp resonator.

Each of the fixed caps of $C_{1,\ 2}$, in Fig. 5.18 and Fig. 5.19, were modified to give us the suitable capacitance range during the post-layout simulation.

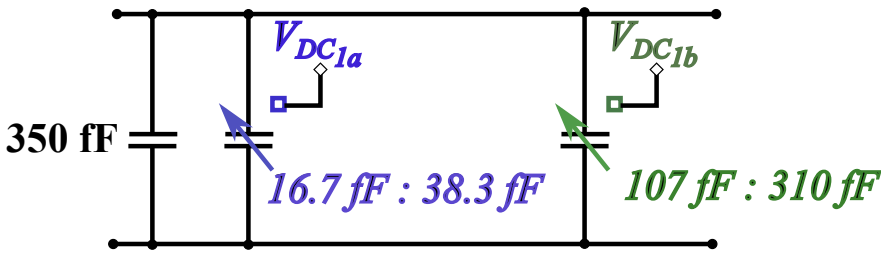

Fig. 5.18: The capacitor C_1 for the layout-implementation of the 1-op-amp resonators

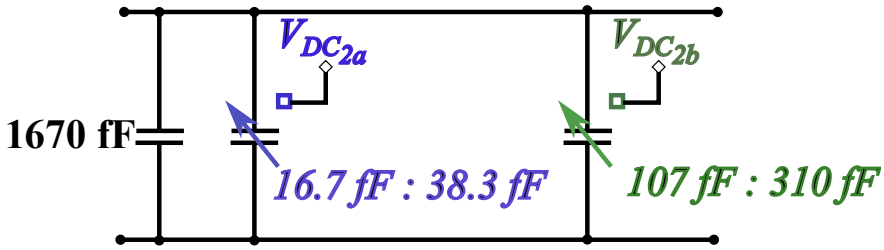

Fig. 5.19: The capacitor C_2 for the layout-implementation of the 1-op-amp resonators

Fig. 5.20 presents the post-layout simulation results of the 4th-order loop filter gain centered at $f_0 \approx 400$ MHz, it is composed of two 1-op-amp resonators connected in-series. The quality factor of the 1st resonator Q_1 is > 500 and the quality factor of the 2nd resonator Q_2 is > 500.

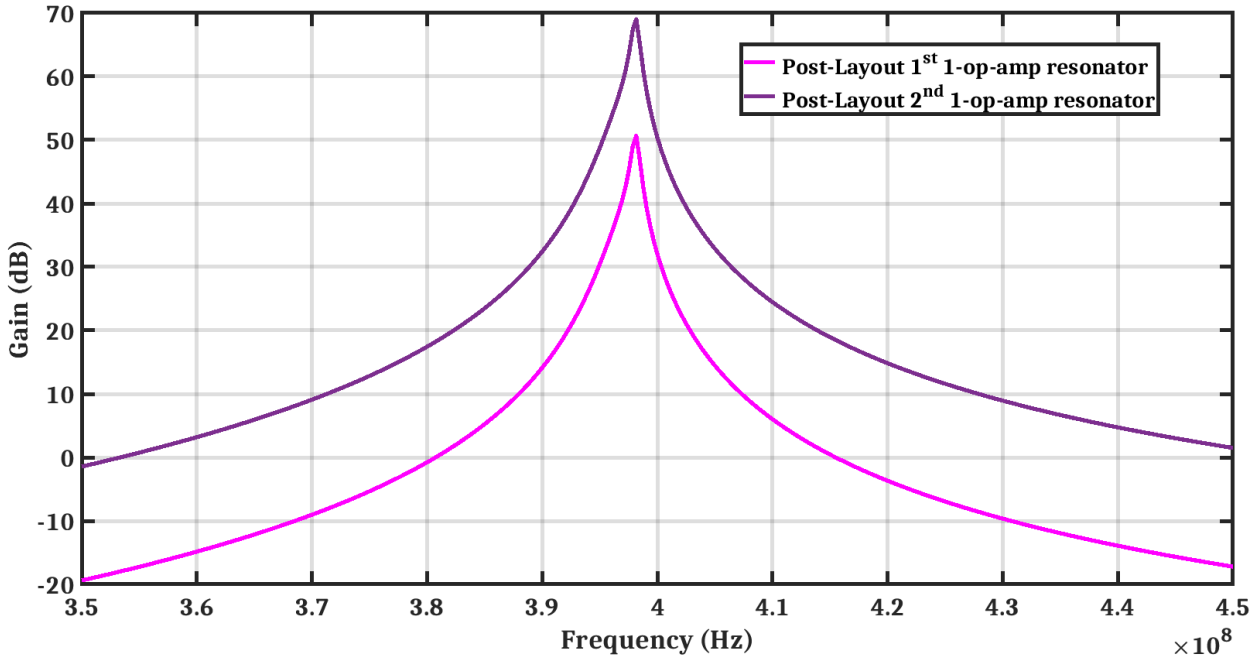

Fig. 5.20: The post-layout simulation results of the 4th-order loop filter gain using a one-op-amp resonator, two 1-op-amp resonators connected in-series, centered at $f_0 \approx 400\ MHz$ and $Q_{1,2} > 500$.

We can accomplish high quality factors for 1-op-amp resonators $Q_{1,\ 2}$, at post-layout simulations, by trimming the capacitors $C_{1,\ 2}$ through the varactors as shown in Fig. 5.18 and Fig. 5.19. Where each varactor operates by a DC voltage, $V_{DC_{1a,\ 1b,\ 2a,\ 2b}}$, supplied from a 7-Bit Digital to Analog Converter with -1.8V/1.8V supply voltage rails. That matches completely our conclusion at Section 5.2.

5.5.2 1-Bit quantizer

The layout-implementation of the 1-Bit quantizer is the same layout as the one for CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators in section 4.4.3.

5.5.3 Current steering DACs with its biasing circuit

The layout-implementation of the current steering DACs along with its biasing circuit are shown in Fig. 5.21, where the transistor-level implementation was explained in-details in section 5.4.3.

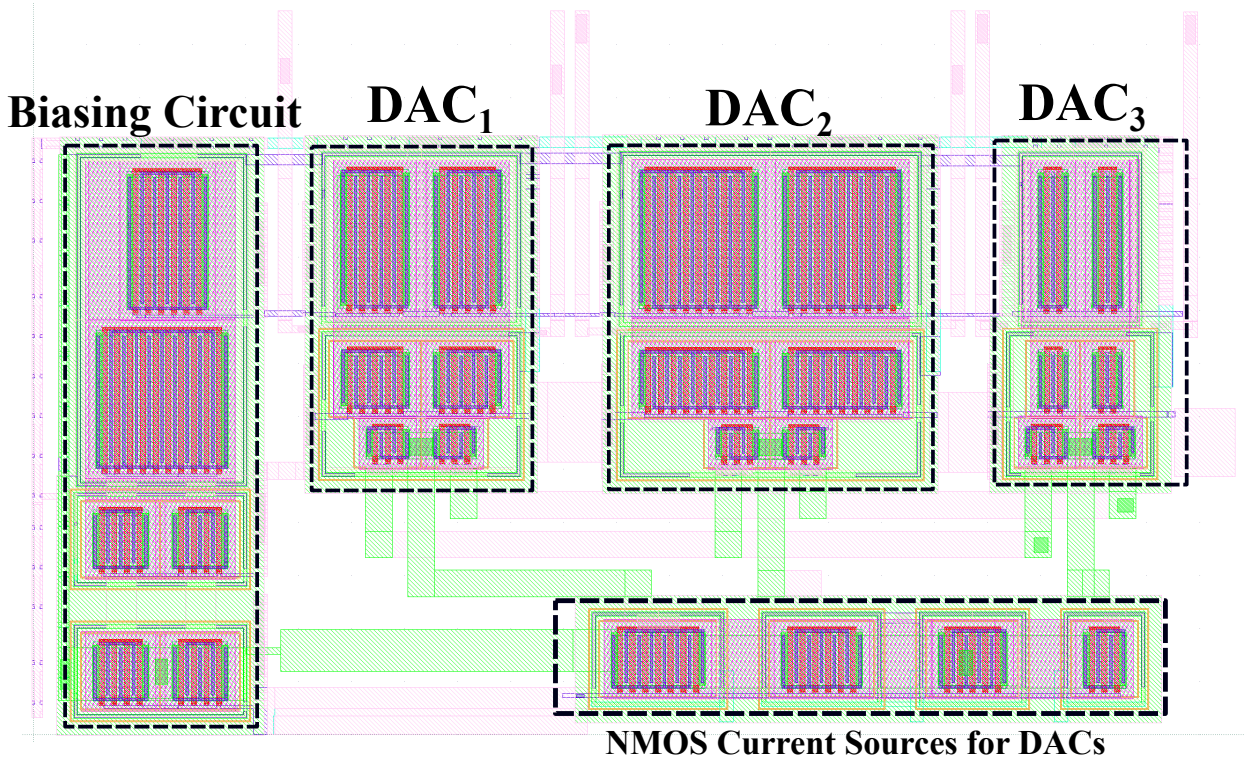

Fig. 5.21: The layout-implementation of the current steering DACs along with its biasing circuit for CT BP $\Sigma\Delta$ modulator using 1-op-amp resonators.

Fig. 5.22 shows the floor-planning of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator design based on 1-op-amp resonators where its circuit-level implementation was presented before in Fig. 5.9. Unfortunately, this floor-planning wasn't verified by Design Rule Checking (DRC), Layout Versus Schematic (LVS) and Parasitic Extraction (PEX) simulations.

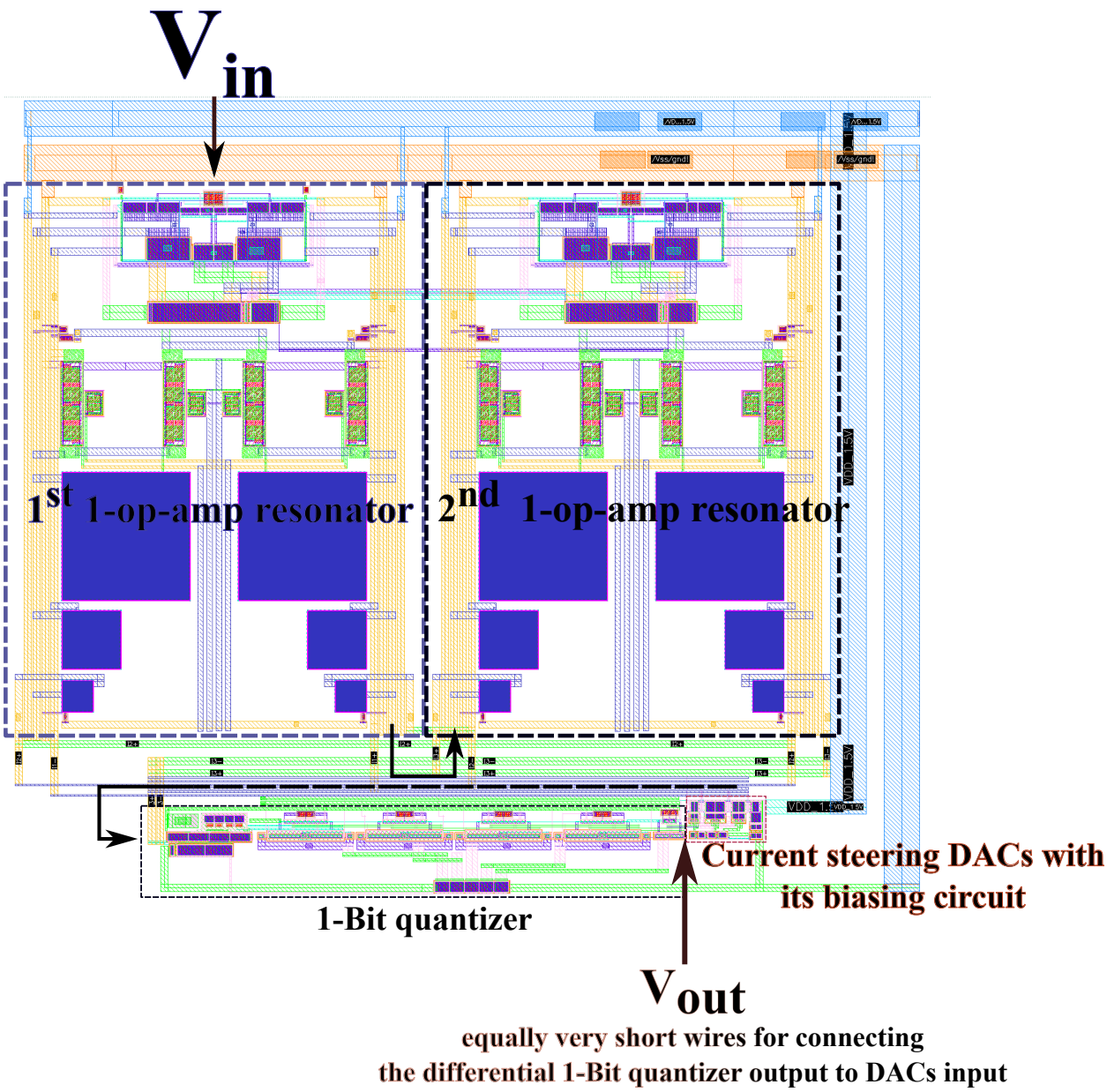

Fig. 5.22: The floor-planning of the 4th-order continuous-time bandpass $\Sigma\Delta$ modulator based on 1-op-amp resonators.

Fig. 5.23 presents the output spectrum of a single-tone post-layout simulation results of the CT BP $\Sigma\Delta$ modulator using 1-op-amp resonators centered at $f_0 = 400$ MHz. Using a single-tone sine-wave input, with amplitude equal to 35.4 mV, the signal to noise ratio (SNR)

is 38.4 dB. This SNR is only 2.6 dB less than the SNR of the transistor-level implementation as shown before in Fig. 5.15.

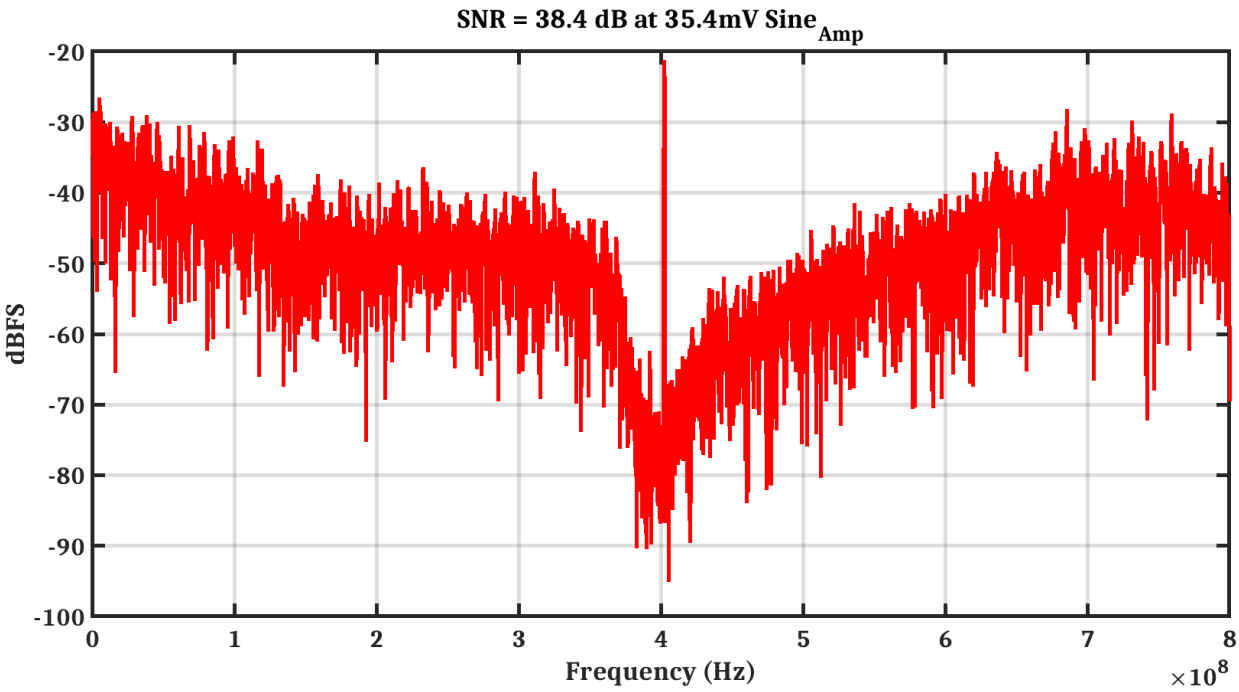

Fig. 5.23: Output spectrum of a single-tone post-layout simulation results of the 4th-order CT BP $\Sigma\Delta$ modulator using a one-op-amp resonator, centered at $f_0 = 400$ MHz.

Fig. 5.24 shows also the output spectrum of a single-tone post-layout simulation results of the 4th-order CT BP $\Sigma\Delta$ modulator using 1-op-amp resonators, shown before at Fig. 5.23, in the range of the bandwidth of $\Sigma\Delta$ from f_0 - $\frac{BW_{\Sigma\Delta}}{2}$ to $f_0 + \frac{BW_{\Sigma\Delta}}{2}$ where $BW_{\Sigma\Delta}$ equals to $\frac{f_s}{2 * OSR}$, $f_s = 1.6$ GHz and OSR = 64. Table 5.2 presents the quality factors $Q_{1,\ 2}$ and the SNR of 1-op-amp resonator $\Sigma\Delta$ at both of the transistor-level/post-layout simulation results.

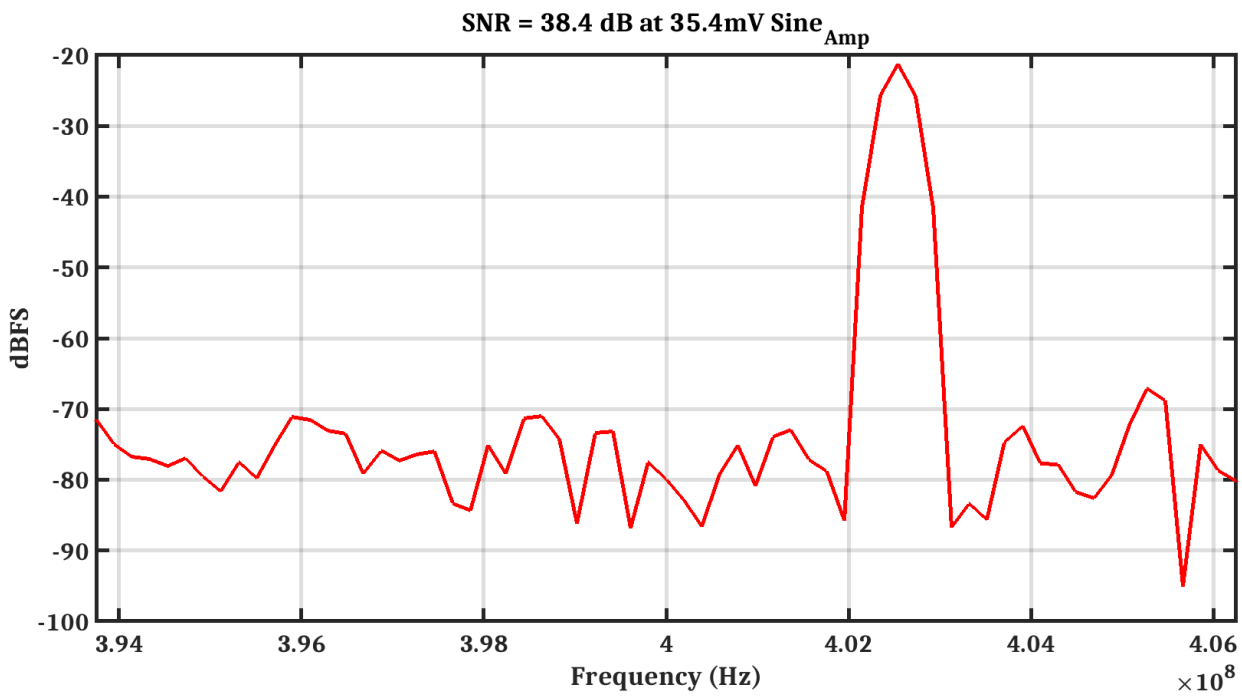

Fig. 5.24: Output spectrum of a single-tone post-layout simulation results of the 4th-order CT BP $\Sigma\Delta$ modulator using a one-op-amp resonator, centered at f_0 = 400 MHz, in the range of the bandwidth of $\Sigma\Delta$, from 393.75 MHz to 406.25 MHz.

Table 5.2: The quality factors $Q_{1,\ 2}$ and the SNR of 1-op-amp resonator $\Sigma\Delta$: at transistor-level/post-layout simulation results

	The resonators-performance	SNR of $\Sigma\Delta$
Transistor-Level	$Q_{1,2} > 1000$ at $f_0 \approx 400\ MHz$	41 dB
Post-Layout	$Q_{1,2} > 500$ at $f_0 \approx 400\ MHz$	38.4 dB

5.6 The post-layout results compared to the state of the art

The performance of the post-layout 1-op-amp resonator $\Sigma\Delta$ modulator is summarized in Table 5.3 and compared with the state of the art at the typical corner.

From Table 5.3, we see that we could design 1-op-amp resonators at moderate DC-gain

op-amps, $A_0 = 34.4\ dB$, using fine-tuning capacitors while the minimum DC-gain op-amps of the state of the art is 44 dB. Our chip area is considered to be competitive with the state of the art. Unfortunately, our design's figure of merit (FOM) is less than the state of the art because we use this kind of resonator in a feedback architecture $\Sigma\Delta$ to introduce a fair comparison with 2-op-amp resonator $\Sigma\Delta$ modulator, while the state of the art uses feedforward architecture $\Sigma\Delta$ which reduces the swing where the non-linearity occurs.

Table 5.3: Performance comparison with the state of the art.

		[Chae13b]	[Chae16]	[Jang18]	[Kim19]			**This Work**
BP $\Sigma\Delta$	Order − Architecture	4th−Feedforward	6th−Feedforward	4th−Feedforward	$4^{th}/6^{th}$−Feedforward			4th−**Feedback**
	Center frequency, f_0 (M Hz)	200	200	1000	2	5	20	**400**
	Sampling frequency, f_s (M Hz)	800	800	4000	8	20	80	**1600**
	quantizer	3-Bit	4-Bit	5-Level	4-Bit			**1-Bit**
	Power (mW)	12	36	15.25	25.8	18.8	14.7	**44.1**
	BW (MHz)	24	25	100	0.2			**12.5**
	SNR (dB)	58	69	48	69	70	70	**38.4**
	FOM {Eq. 4.2} [Ali10] [dB]	151	157.4	146.2	138	140	141.5	**123**
	IIP3 (dBm)/2-tone spacing (MHz)	x	x	-3/-	x			**+5.4/3**
	Area (mm^2)	0.2	0.25	0.0113	0.845			**0.057**
Op-amp	no. of stages	4	4	3	2			**2**
	DC-gain (dB)	73	57	71	$\geqslant 44$			**34.4**
	Gain @ f_0 (dB)	30	$>$ 50	?	40			**38**
	f_T (GHz)	3	?	13.22	$\geqslant 1.22$			**15.2**
	Stability	Unconditionally stable	?	?	Unconditionally stable			**Unconditionally stable**
	Power (mW) @ V_{DD}	2 @ 1.25 V	7.5 @ 1.2 V/1.7 V	5.4 @ 1.2 V	? @ 1.8 V			**18.75@ 1.5 V**
	Technology	CMOS 65nm	CMOS 65nm	CMOS 40nm	CMOS 180nm			**FDSOI-28nm**

5.7 Conclusion

The quality factor sensitivity to the RC network capacitors values at a limited op-amp DC-gain $A_0 = 35\ dB$ has been analyzed for the one-op-amp resonator. Besides, the influence of

the RC network capacitors values at limited op-amp DC-gain $A_0 = 35\ dB$ on the maximum SNR of a 4th-order CT BP $\Sigma\Delta$ modulator has been discussed. To achieve high quality factors for the one-op-amp resonators as soon as a SNR higher than 60 dB for CT BP $\Sigma\Delta$ modulator, the capacitors values $C_{1,\ 2}$ of its RC network should be trimmed using a very fine calibration circuit.

The SNR of the transistor-level implementation for the one-op-amp resonator CT BP $\Sigma\Delta$ modulator is 14 dB lower than the SNR of the transistor-level implementation for the two-op-amp resonator CT BP $\Sigma\Delta$ modulator. It is due to the bad linearity of one-op-amp resonators which comes from the positive feedback connection through the resistor R_2 and the capacitor C_2. At the post-layout simulation results, we can accomplish high quality factors for one-op-amp resonators by trimming the capacitors $C_{1,\ 2}$ through varactors. The SNR of the post-layout simulation results is 38.4 dB, it is only 2.6 dB less than the SNR of the transistor-level implementation simulation results.

Chapter 6

Comparison and discussion

6.1 Introduction

In this chapter, we compare the two-op-amp resonator CT BP $\Sigma\Delta$ modulator to the one-op-amp resonator CT BP $\Sigma\Delta$ modulator.
This comparison includes many design objective:
In section 6.2, we first discuss the quality factor "Q" of each resonator. Second in section 6.3, we show the signal to noise ratio "SNR" for both $\Sigma\Delta$ modulators. Third in section 6.4, the post-layout simulation results of the "worst-case" process corners of both $\Sigma\Delta$ modulators are introduced. Finally, it discusses the dynamic range of the transistor-level implementation simulation results for each $\Sigma\Delta$ modulator, in section 6.5.

6.2 The quality factor "Q":

- **Two-op-amp resonators:**

  Based on the 2nd-order mathematical model for the two-op-amp resonator considering a finite DC-gain A_0 and infinite 1st pole f_p for the op-amps, we reach the conclusion that the quality factor Q increases proportionally to the op-amp DC-gain A_0 as presented in Fig. 3.18.

  While, based on the high-order mathematical model for the two-op-amp resonator con-

sidering a finite DC-gain A_0 and finite poles/zeros for the op-amps, we found that there is an optimal value for quality factor Q which depends on the integrator gain A as shown in Fig. 3.24.

At the transistor-level implementation of the 4th-order loop filter presented at Fig. 4.11, the quality factor of the 1st resonator Q_1 was high equal to 650 and the quality factor of the 2nd resonator Q_2 was 193. While at the post-layout implementation of the 4th-order loop filter presented at Fig. 4.22, the quality factors $Q_{1,\ 2}$ were decreased to 65.4 and 77.2, since additional resistance and additional capacitance were extracted and have an effect on the gain of integrators of Eq. 3.28 that led to decrease the quality factor Q.

- **One-op-amp resonators:**

  In chapter 5 at section 5.2, the quality factor sensitivity to the RC network capacitors $C_{1,\ 2}$ at moderate DC-gain op-amps $A_0 = 35\ dB$ has been studied. We showed that a very-fine calibration circuit should be designed for implementing the capacitors $C_{1,\ 2}$, while it isn't required at a very high DC-gain op-amp $A_0 \geq 75\ dB$. At the transistor-level implementation of the 4th-order loop filter presented at section 5.4, the quality factors $Q_{1,\ 2}$were very high > 1000. Also, at the post-layout simulations presented at section 5.5, the quality factors $Q_{1,\ 2}$ were also high > 500. These high quality factors were achieved when we trimmed the capacitors $C_{1,\ 2}$ through varactors which operates by a DC voltage supplied from a 7-Bit Digital to Analog Converter with -1.8V/1.8V supply voltage rails.

6.3 The Signal to Noise Ratio "SNR":

- **Two-op-amp resonator CT BP $\Sigma\Delta$ modulator:**

  In chapter 3, the proposed noise study allowed us to select the convenient values for the integrator resistor R and the integrator gain A to achieve a SNR greater than 60 dB. Based on these values, we demonstrated that the moderate DC-gain op-amps $A_0 = 35\ dB$ is enough for our target, in chapter 3 at section 3.6. At the transistor-level implementation of the $\Sigma\Delta$ modulator presented in chapter 4 at section 4.3, the SNR was 55 dB. Compared to the SNR calculated from the noise study, we lost only 6.8 dB due to using the transistor-

level implementation, while at the post-layout implementation presented at section 4.4, the SNR equals 53 dB.

- **One-op-amp resonator CT BP $\Sigma\Delta$ modulator:**
  In chapter 5, the SNR sensitivity to the RC network capacitors $C_{1,\ 2}$ at moderate DC-gain op-amps $A_0 = 35\ dB$ has been discussed. We showed that a very-fine calibration circuit is needed for implementing the capacitors $C_{1,\ 2}$ to achieve a SNR greater than 60 dB. At the transistor-level implementation of the $\Sigma\Delta$ modulator presented at section 5.4, the SNR was 41 dB. It was 14 dB less than the SNR of the transistor-level implementation for the 2-op-amp resonator $\Sigma\Delta$ modulator, due to the linearity of one-op-amp resonator is inferior to two-op-amp resonator with the negative feedback connection which improves the linearity. While at the post-layout implementation presented at section 5.5, the SNR equals 38.4 dB.

6.4 The post-layout results at the "worst-case" process corners:

At the two worst-case process corners, the 1st process corner is measured at $V_{DD} = 1.4\ V$ and the temperature, $T = 125^o$. Moreover, it operates at the pre-defined corner for the speed performance of the NMOS transistors and the PMOS transistors, respectively, "$Slow - Slow$" and the maximum allowable value of the resistors R_{max}. While the 2nd process corner is measured at $V_{DD} = 1.6\ V$ and the temperature, $T = -40^o$. It operates at the pre-defined corner for the speed performance of the NMOS transistors and the PMOS transistors, respectively, "$Fast - Fast$" and the minimum allowable value of the resistors R_{min}.

- **Two-op-amp resonator CT BP $\Sigma\Delta$ modulator:**
  From Table 6.1, $\Sigma\Delta$ modulator has the Figure of Merit (FoM) = 123.2 at center frequency, $f_0 = 400MHz$, at the 1st process corner. While it has a FoM = 122 at center frequency $f_0 = 400MHz$, at the 2nd process corner.

- **One-op-amp resonator CT BP $\Sigma\Delta$ modulator:**

  From Table 6.1, $\Sigma\Delta$ modulator has a FoM = 98.4 at center frequency $f_0 = 390.6\ MHz$ measured at the 1st process corner. While at the 2nd process corner, it has a FoM = 120.4 at center frequency $f_0 = 407.8\ MHz$.

  In addition to, 1-op-amp resonator $\Sigma\Delta$ modulator consumes approximately half the power consumption of 2-op-amp resonator $\Sigma\Delta$ modulator, and its chip area is almost 26 % of the chip area of 2-op-amp resonator $\Sigma\Delta$ modulator.

Table 6.1: Post-layout simulation results using the typical model and the **worst-case** process corners (the 1st corner, the 2nd corner).

Resonator	**2-op-amp**			**1-op-amp**		
Process-Corner	Typical	1st corner	2nd corner	Typical	1st corner	2nd corner
Temperature [^{o}]	27	125	−40	27	125	−40
V_{DD} [V]	1.5	1.4	1.6	1.5	1.4	1.6
Resistance	$R_{typical}$	R_{max}	R_{min}	$R_{typical}$	R_{max}	R_{min}
NMOS-PMOS	$Typical - Typical$	$Slow - Slow$	$Fast - Fast$	$Typical - Typical$	$Slow - Slow$	$Fast - Fast$
f_s [M Hz]	**1600**			**1600**	**1562**	**1631**
f_0 [M Hz]	**400**			**400**	**390.6**	**407.8**
BW [M Hz]	**12.5**			**12.5**	**12.2**	**12.74**
SNR [dB]	**53**	**41**	**40.3**	**38.4**	**14.2**	**37**
$Power$ [m W]	**81.1**	**75**	**87.1**	**44.1**	**46.2**	**58.3**
FOM {Eq. 4.2} [Ali10] [dB]	**135**	**123.2**	**122**	**123**	**98.4**	**120.4**
$area$ [mm^2]	**0.22**			**0.057**		

6.5 The Dynamic range and input third order intercept point (IIP3):

Fig. 6.1 presents the dynamic range of the transistor-level implementation for each $\Sigma\Delta$ modulator. It shows that the dynamic range of 2-op-amp resonator CT BP $\Sigma\Delta$ modulator, $DR_{2-op-amp}$, is 10 dBm higher than the dynamic range of 1-op-amp resonator CT BP $\Sigma\Delta$ modulator, $DR_{1-op-amp}$.

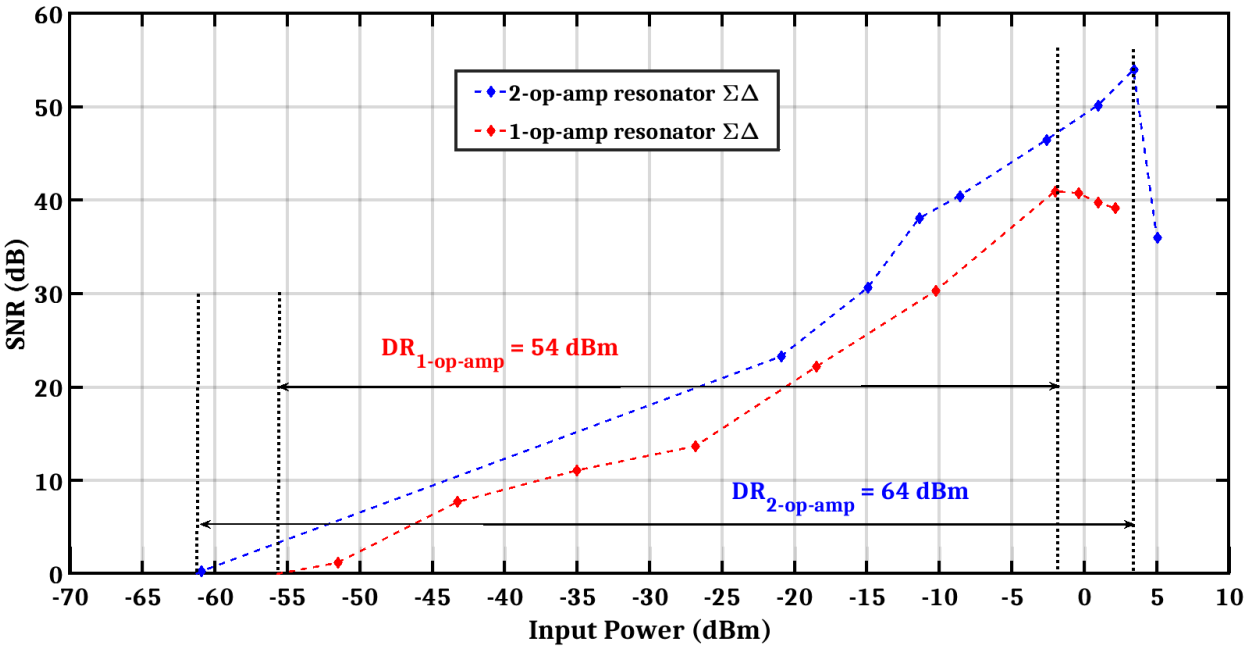

Fig. 6.1: Dynamic range of 4th-order CT BP $\Sigma\Delta$ modulator using both two-op-amp resonator and one-op-amp resonator against the input power in dBm.

Fig. 6.2 and Fig. 6.3 present the input third order intercept point (IIP3) of the transistor-level implementation for each $\Sigma\Delta$ modulator. It shows that IIP3 of 2-op-amp resonator CT BP $\Sigma\Delta$ modulator is 16.1 dBm higher than IIP3 of 1-op-amp resonator CT BP $\Sigma\Delta$ modulator.

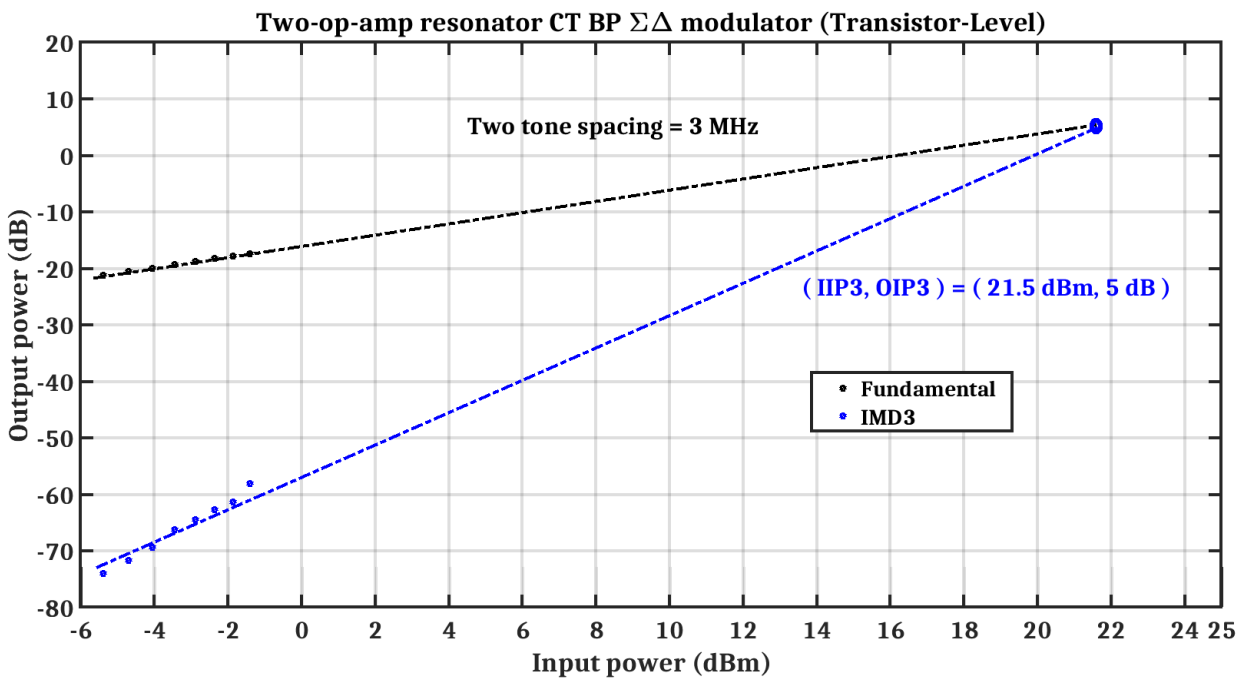

Fig. 6.2: IIP3 of the transistor-level 4th-order CT BP $\Sigma\Delta$ modulator using two-op-amp resonators.

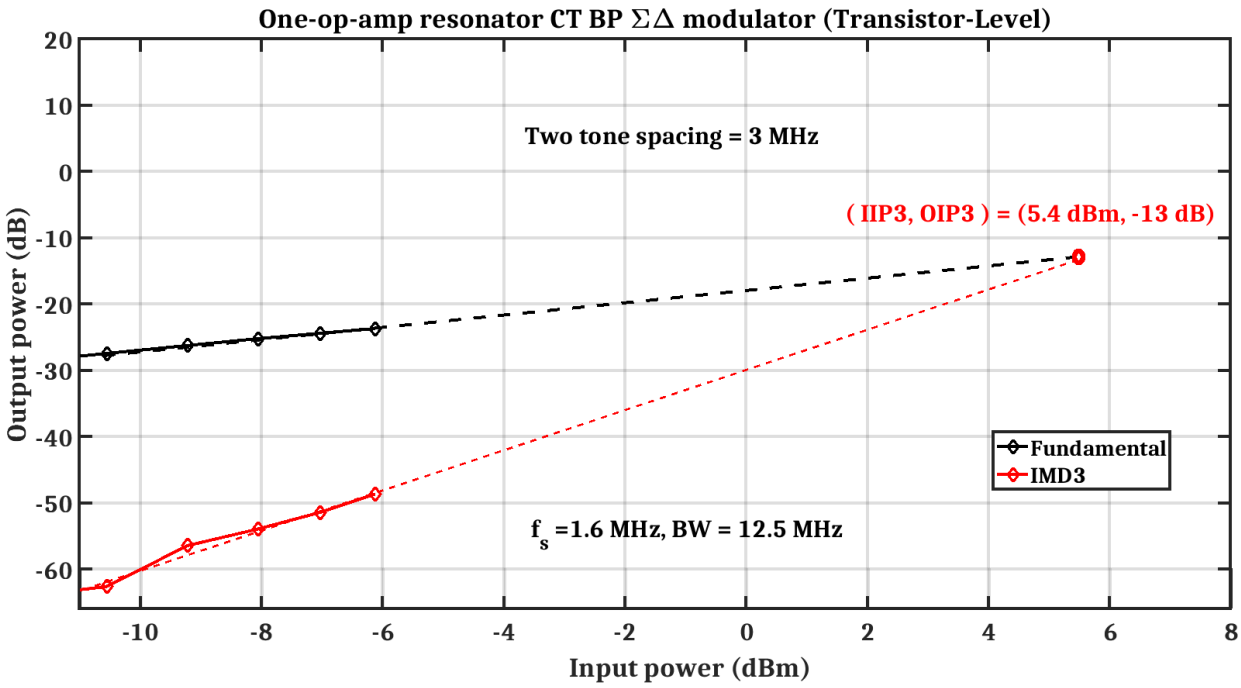

Fig. 6.3: IIP3 of the transistor-level 4th-order CT BP $\Sigma\Delta$ modulator using one-op-amp resonators.

6.6 Conclusion

A comparison between the two-op-amp resonator CT BP $\Sigma\Delta$ modulator and the one-op-amp resonator CT BP $\Sigma\Delta$ modulator was presented. It considered many design objectives such as the quality factor "Q" of each resonator, the signal to noise ratio "SNR", the post-layout simulation results of the "worst-case" process corners and the dynamic range with the input third order intercept point (IIP3) of the transistor-level implementation for each $\Sigma\Delta$ modulator. As presented in table 6.1, the 2-op-amp resonator $\Sigma\Delta$ modulator achieves higher SNR than the 1-op-amp resonator $\Sigma\Delta$ modulator at the typical corner and also it is robust for process, voltage and temperature (PVT) variations at "worst-case" process corners. As shown from Fig. 6.1, when we use the same op-amp, 2-op-amp resonator $\Sigma\Delta$ modulator achieves higher dynamic range than 1-op-amp resonator $\Sigma\Delta$ modulator. In Fig. 6.2 and

Fig. 6.3, when we use the same op-amp, 2-op-amp resonator $\Sigma\Delta$ modulator achieves higher IIP3 than 1-op-amp resonator $\Sigma\Delta$ modulator.

Chapter 7

Conclusion and Future work

- In this work, we have presented a mathematical model for the thermal noise contribution of each integrator in a 4th-order CT BP $\Sigma\Delta$ modulator based on two-op-amp resonators. The influence of integrator resistor R and integrator gain A is considered. This study allows the designer to select the convenient values for both of them for a required SNR. The suggested study is well matched with the noise transient analysis simulations with a small error ≤ 2.5 % .

- At finite DC-gain A_0 and infinite 1st pole f_p for the op-amps used for the two-op-amp resonators, we conclude that the quality factor Q and the maximum SNR of $\Sigma\Delta$ modulator increase proportionally with the op-amp DC-gain A_0.
  We propose then to select the proper value of the integrator gain A with the suitable value of the integrator resistor R to boost the quality factor of the two-op-amp resonator using moderate DC-gain op-amps $A_0 = 35\ dB$. This technique was presented by the mathematical models and compared with the simulation results of the transistor-level implementations.

- The transistor-level implementation of the two-op-amp resonator 4th-order CT BP $\Sigma\Delta$ modulator was designed using Low V_{TH} devices, that are also called "flipped-well" devices, on fully depleted silicon on insulator (FDSOI) technology as presented in chapter 4.

We achieved $SNR = 55\ dB$, which is only 6.8 dB less than the one calculated by our proposed thermal-noise study. At the post-layout simulation results, the quality factors of 2-op-amp resonators are decreased, compared to the transistor-level simulation results, since additional resistance and additional capacitance are extracted and have an effect on the gain of integrators. The SNR of the post-layout simulation results is 53 dB which is only 2 dB less than the SNR of the transistor-level implementation simulation results.

- The quality factor sensitivity to the RC network capacitors values at a limited op-amp DC-gain $A_0 = 35\ dB$ has been analyzed for the one-op-amp resonators in chapter 5. Besides, the influence of the RC network capacitors values at limited op-amp DC-gain $A_0 = 35\ dB$ on the maximum SNR of a 4th-order CT BP $\Sigma\Delta$ modulator has been discussed. To achieve high quality factors for the one-op-amp resonators as soon as for SNR higher than 60 dB, the capacitors values $C_{1,\ 2}$ of its RC network should be trimmed using a very fine-calibration circuit.
  The SNR of the transistor-level implementation for the one-op-amp resonator CT BP $\Sigma\Delta$ modulator is 14 dB lower than the SNR of the transistor-level implementation for the two-op-amp resonator CT BP $\Sigma\Delta$ modulator. At the post-layout simulation results, we can accomplish high quality factors for one-op-amp resonators by trimming the capacitors $C_{1,\ 2}$ through varactors. The SNR of the post-layout simulation results is 38.4 dB which is only 2.6 dB less than the SNR of the transistor-level implementation simulation results.

- A comparison between the two-op-amp resonator CT BP $\Sigma\Delta$ modulator and the one-op-amp resonator CT BP $\Sigma\Delta$ modulator was discussed in chapter 6. It considered many design parameters such as the quality factor "Q" of each resonator, the signal to noise ratio "SNR" and the post-layout simulation results of the "worst-case" process corners. Also, it discussed the dynamic range of the transistor-level implementation simulation results for each $\Sigma\Delta$ modulator.

In the future, we would like to study the thermal-noise behavior of 4th–order CT BP 1-op-amp resonator $\Sigma\Delta$ modulator and compare it with the thermal-noise study of 4th–order CT BP 2-op-amp resonator $\Sigma\Delta$ modulator. Then, the limited output swing of op-amps can be analyzed using 2-op-amp resonator and 1-op-amp resonator within $\Sigma\Delta$ modulators performance. Besides, a high DC-gain op-amp with a lower power consumption will be designed for 1-op-amp resonator and compare its $\Sigma\Delta$ modulator performance with our current results.

Appendix A

Process Corners procedure on "FDSOI-28nm" technology

The Fully Depleted Silicon on Insulator "**FDSOI**" technology enables a wide-tuning for the body bias. The body factor is approximately 85 mV/V, where body voltage can vary from -3 V to 3 V [Cathelin17]. We can decrease system-level process, voltage, and temperature (PVT) variations by continuously tuning the threshold voltage $V_{TH_{n,p}}$ as found in the design examples of [Lechevallier15], [Danilovic16], [Streel17]. In our available design kit, there are two extreme cases "R_{max}" and "R_{min}" for the passive device of resistor. As well as, there are four pre-defined corners "PDC" for the speed performance of the NMOS/PMOS transistors, respectively. They are "$Fast - Fast$", "$Fast - Slow$", "$Slow - Fast$", "$Slow - Slow$". We assume that the temperature can vary in the range from -40° to 125° and the supply voltage in the range from 1.4 V to 1.6 V. Therefore, we compose " $2\ X\ 2\ X\ 2\ X\ 4 = 32$ " possible process corners combinations from table A.1. First, we calculate the error of each free body

Table A.1: The process, voltage, and temperature (PVT) boundaries

$V_{DD_{1,\ 2}}$	**1.4 V**		**1.6 V**	
$T_{1,\ 2}$	**-40°**		**125°**	
Resistor	$\mathbf{R}_{max}$		$\mathbf{R}_{min}$	
The pre-defined corner	$Fast - Fast$ **(FF)**	$Fast - Slow$ **(FS)**	$Slow - Fast$ **(SF)**	$Slow - Slow$ **(SS)**

bias voltage such as BB_1, BB_2, BB_{DACs}, $BB_{Pre-Amp}$ and $BB_{Latches-Inverter}$ as discussed in-details at section 4.3 in chapter 4 at each process corner of 32 possibilities compared to the typical corner as expressed by Eq. A.1, Eq. A.2.

$$BB_{error}(\%) \;=\; 100 \;\cdot\; \frac{BB_{\;Typical\;Corner} \;-\; BB_{\;Process\;Corner}}{BB_{\;Typical\;Corner}} \tag{A.1}$$

where,

$$BB \;=\; BB_{\;1,\;2,\;DACs,\;Pre-Amp,\;Latches-Inverter} \tag{A.2}$$

The body bias voltage $BB_{\;Typical\;Corner}$ and $BB_{\;Process\;Corner}$ are trimmed during the post-layout simulations to achieve the same DC currents values of all NMOS transistors current sources as designed at the transistor-level implementations in the typical corner and each process corner of 32 possibilities, respectively. Table A.2 demonstrates the values of BB_{error} that was measured at each process corner of 32 possibilities compared to the typical corner for all blocks in $\Sigma\Delta$ modulator. The process corners have the max BB_{error} that are in a blue/red font color. We selected the 1st worst-case process corner, V_{DD_1} T_2 (SS) R_{max}, in a red font color since it has the maximum negative BB_{error} compared to the others in black font color. The process corner, V_{DD_1} T_2 (SS) R_{min}, has the same value of the BB_{error} as the process corner, V_{DD_1} T_2 (SS) R_{max}, so we can select only one of those. The process corners, V_{DD_2} T_1 (FF) R_{min}, V_{DD_2} T_1 (FF) R_{max}, V_{DD_2} T_1 (FS) R_{min} and V_{DD_2} T_1 (FS) R_{max}, have maximum positive BB_{error} compared to the others in black font color. We selected the 2nd worst-case process corner, V_{DD_2} T_1 (FF) R_{min}, in a red font color. Now, we can test the post-layout of both 2-op-amp resonator $\Sigma\Delta$ modulator and 1-op-amp resonator $\Sigma\Delta$ modulator at the selected two worst-case process corners. It is better to select the worst-case process corners from 32 possibilities, since one simulation lasts for more than 2 days so that it is not possible to simulate 32 runs because of memory-crash problems.

Table A.2: The $BB_{error}(\%)$ measured at each process corner compared to the typical corner for all blocks in $\Sigma\Delta$ modulator

	$\mathbf{BB}_{error}(\%)$				
The process corner	BB $_1$	BB $_2$	BB $_{Pre-Amp}$	BB $_{Latches-Inverter}$	BB $_{DACs}$
V_{DD_1} T_1 (FF) R_{min}	+22 %	+27 %	+25 %	+5 %	+14 %
V_{DD_1} T_1 (FF) R_{max}	+22 %	+27 %	+25 %	+5 %	+14 %
V_{DD_1} T_1 (FS) R_{min}	+11 %	+27 %	+25 %	+5 %	+14 %
V_{DD_1} T_1 (FS) R_{max}	+11 %	+27 %	+25 %	+5 %	+14 %
V_{DD_1} T_2 (FF) R_{min}	-33 %	-27 %	0 %	-19 %	-86 %
V_{DD_1} T_2 (FF) R_{max}	-33 %	-27 %	0 %	-19 %	-86 %
V_{DD_1} T_2 (FS) R_{min}	-44 %	-27 %	0 %	-19 %	-114 %
V_{DD_1} T_2 (FS) R_{max}	-44 %	-27 %	0 %	-19 %	-114 %
V_{DD_2} T_1 (FF) R_{min}	**+33 %**	**+33 %**	**+50 %**	**+29 %**	**+14 %**
V_{DD_2} T_1 (FF) R_{max}	**+33 %**	**+33 %**	**+50 %**	**+29 %**	**+14 %**
V_{DD_2} T_1 (FS) R_{min}	**+22 %**	**+33 %**	**+50 %**	**+33 %**	**+29 %**
V_{DD_2} T_1 (FS) R_{max}	**+22 %**	**+33 %**	**+50 %**	**+33 %**	**+29 %**
V_{DD_2} T_2 (FF) R_{min}	-25 %	-12 %	+33 %	0 %	-36 %
V_{DD_2} T_2 (FF) R_{max}	-25 %	-12 %	+33 %	0 %	-36 %
V_{DD_2} T_2 (FS) R_{min}	-25 %	-12 %	+33 %	0 %	-36 %
V_{DD_2} T_2 (FS) R_{max}	-25 %	-12 %	+33 %	0 %	-36 %
V_{DD_1} T_1 (SF) R_{min}	0 %	+13 %	0 %	0 %	+14 %
V_{DD_1} T_1 (SF) R_{max}	0 %	+13 %	0 %	0 %	+14 %
V_{DD_1} T_1 (SS) R_{min}	0 %	+13 %	0 %	-43 %	+14 %
V_{DD_1} T_1 (SS) R_{max}	0 %	+13 %	0 %	-43 %	+14 %
V_{DD_1} T_2 (SF) R_{min}	-67 %	-47 %	-50 %	-29 %	-100 %
V_{DD_1} T_2 (SF) R_{max}	-67 %	-47 %	-50 %	-29 %	-100 %
V_{DD_1} T_2 (SS) R_{min}	**-67 %**	**-47 %**	**-50 %**	**-43 %**	**-143 %**
V_{DD_1} T_2 (SS) R_{max}	**-67 %**	**-47 %**	**-50 %**	**-43 %**	**-143 %**
V_{DD_2} T_1 (SF) R_{min}	+11 %	+20 %	+50 %	+19 %	+14 %
V_{DD_2} T_1 (SF) R_{max}	+11 %	+20 %	+50 %	+19 %	+14 %
V_{DD_2} T_1 (SS) R_{min}	+11 %	+20 %	+25 %	+19 %	+14 %
V_{DD_2} T_1 (SS) R_{max}	+11 %	+20 %	+25 %	+19 %	+14 %
V_{DD_2} T_2 (SF) R_{min}	-56 %	-40 %	-25 %	0 %	-57 %
V_{DD_2} T_2 (SF) R_{max}	-56 %	-40 %	-25 %	0 %	-57 %
V_{DD_2} T_2 (SS) R_{min}	-56 %	-33 %	-25 %	0 %	-57 %
V_{DD_2} T_2 (SS) R_{max}	-56 %	-33 %	-25 %	0 %	-57 %

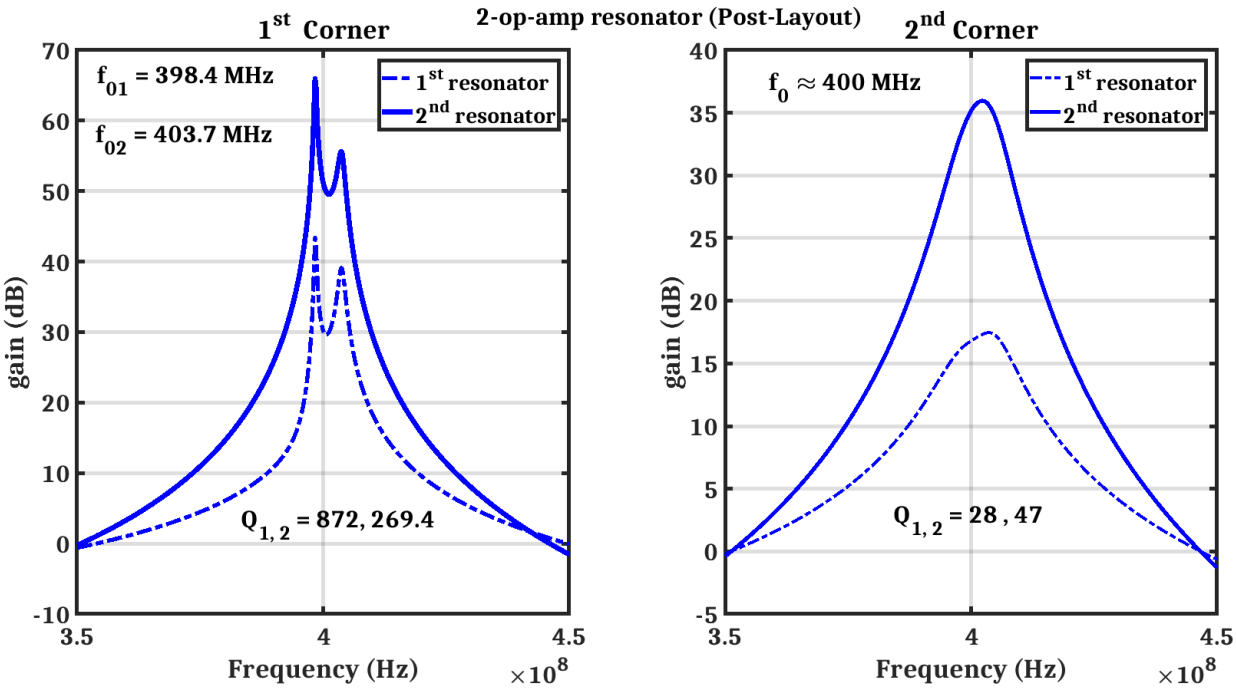

Fig. A.1: Simulations of the post-layout gain of the 4th-order loop filter using two-op-amp resonator, two 2-op-amp resonators connected in-series, at the two worst-case process corners.

Fig. A.1 presents the post-layout simulation results of the 4th-order loop filter gain, composed of two 2-op-amp resonators connected in-series, at the two worst-case process corners. At 1st worst-case process corner, it has two resonance frequencies $f_{01,\ 02} = 398.4\ MHz, 403.7\ MHz$, where f_{01} is the resonance frequency of the 1st resonator and f_{02} is the resonance frequency of the 2nd resonator, while the quality factor of the 1st resonator Q_1 is 872 and the quality factor of the 2nd resonator Q_2 is 269.4. At 2nd worst-case process corner, the quality factor of the 1st resonator Q_1 is 28 and the quality factor of the 2nd resonator Q_2 is 47, centered at $f_0 \approx 400$ MHz.

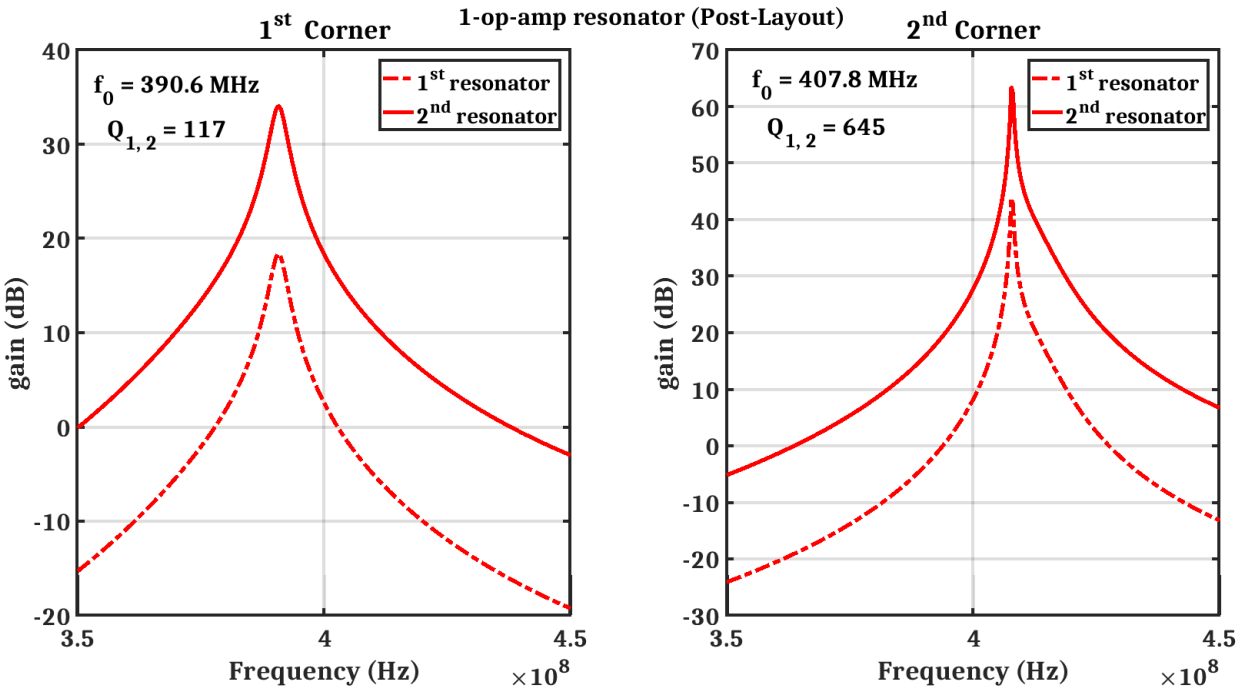

Fig. A.2: Simulations of the post-layout gain of the 4th-order loop filter using one-op-amp resonator, two 1-op-amp resonators connected in-series, at the two worst-case process corners.

Fig. A.2 presents the post-layout simulation results of the 4th-order loop filter gain, composed of two one-op-amp resonators connected in-series, at the two worst-case process corners. At 1st worst-case process corner, the quality factor of the 1st resonator Q_1 is 117 and the quality factor of the 2nd resonator Q_2 is 117, centered at $f_0 = 390.6$ MHz, using $V_{DC_{1a,\ 1b,\ 2a,\ 2b}} = 1.8$ V, 1.8 V, -1.8 V , 0.9 V. At 2nd worst-case process corner, the quality factor of the 1st resonator Q_1 is 645 and the quality factor of the 2nd resonator Q_2 is 645, centered at $f_0 = 407.8$ MHz, using $V_{DC_{1a,\ 1b,\ 2a,\ 2b}} = 1.8$ V, -1.8 V, -1.8 V , -0.9 V.

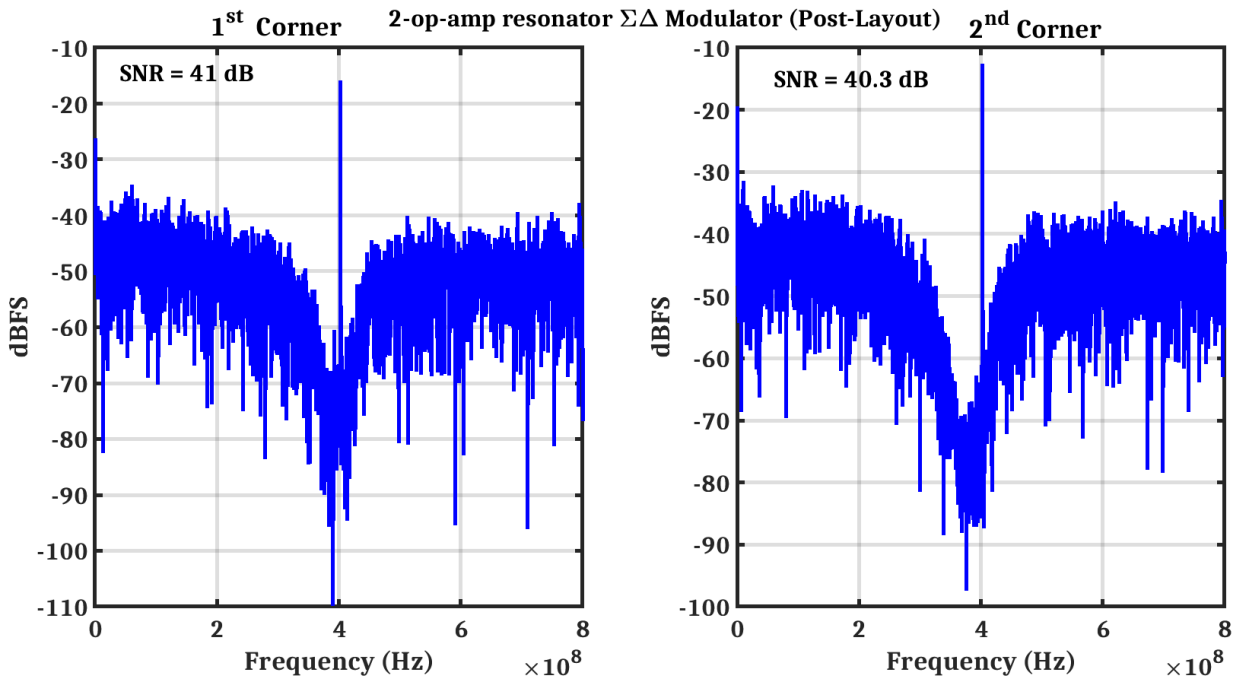

Fig. A.3: Output spectrum of a single-tone post-layout simulation of the 4th-order CT BP $\Sigma\Delta$ modulator using a two-op-amp resonator, centered at $f_0 = 400$ MHz, at the two worst-case process corners.

Fig. A.3 presents the output spectrum of a single-tone post-layout simulation results of the CT BP $\Sigma\Delta$ modulator using 2-op-amp resonators centered at $f_0 = 400$ MHz, using a single-tone sine-wave input, with amplitude equal to 66 mV, at the two worst-case process corners. The signal to noise ratio (SNR) is 41 dB at 1st worst-case process corner due to a high delay loop compared to the typical corner, while it is 40.3 dB at 2nd worst-case process corner due to lower quality factors compared to the typical corner.

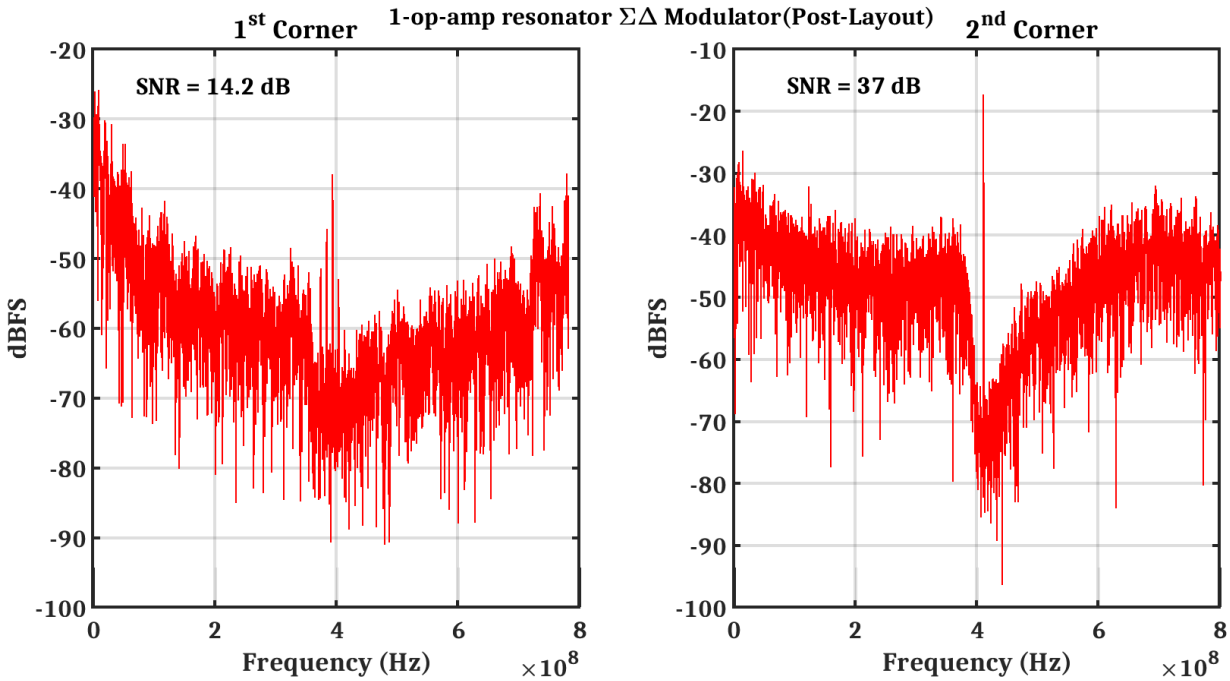

Fig. A.4: Output spectrum of a single-tone post-layout simulation results of the 4th-order CT BP $\Sigma\Delta$ modulator using a one-op-amp resonator, at the two worst-case process corners.

Fig. A.4 presents the output spectrum of a single-tone post-layout simulation results of the CT BP $\Sigma\Delta$ modulator using 1-op-amp resonators, using a single-tone sine-wave input with amplitude equal to 35.4 mV. The signal to noise ratio (SNR) is 14.2 dB centered at $f_0 = 390.6$ MHz due to a high delay loop compared to the typical corner, at 1st worst-case process corner, while it is 37 dB centered at $f_0 = 407.8$ MHz, at 2nd worst-case process corner.

Appendix B

MATLAB codes

B.1 The transfer function of the gain for the two-op-amp resonator at limited DC-gain and infinite pole of op-amps

As presented below, this MATLAB code computes the transfer function of the gain for a two-op-amp resonator at limited DC-gain, A_0, and an infinite 1st pole, f_p, for the op-amps. It calculates the accurate gain of 2-op-amp resonator using symbolic equations solved by **solve MATLAB function**, as well as, the approximate gain of 2-op-amp resonator at DC-gain, $A_0 \gg 1$.

Both transfer functions are well-matched. The quality factor Q and the center frequency f_0 are also calculated using the accurate and the approximate ways and discussed in the code. The values of the integrator resistor R, the integrator gain A, DC-gain of op-amps A_0 are 677 Ω , 0.75 and 35 dB, respectively, at $f_s = 1.6$ GHz in our design.

```
clear
clc
close all
%%
syms A0 s V_in V_1 V_2 V_o1 V_out C R RF
%%
```

```
Op_Amp_TF = A0;
%%
eqn1_accurate = (-1*(V_in-V_1)/R) + ((V_1+V_o1)*s*C) + ((V_1+V_out
    )/RF) == 0;
%%
eqn2_accurate  =(-1*(V_o1-V_2)/R) + ((V_2+V_out)*s*C) == 0;
%%
eqn3_accurate  = (-1*(V_o1)) + ((V_1)* Op_Amp_TF) ==0;
%%
eqn4_accurate  = (-1*(V_out)) + ((V_2)* Op_Amp_TF) ==0;
%%
eqns_accurate  = [eqn1_accurate eqn2_accurate eqn3_accurate
    eqn4_accurate];
S_accurate = solve(eqns_accurate,[V_in V_1 V_2 V_o1]);
%%
Num = (1/(R*C))^2 * (1/(1+(2/A0)));
%%
Denum_1 = (R+2*RF)/((C*R*RF) *(A0+2) );
%%
Denum_2 = (1/(RF*R*C^2)) * (1/(1+(2/A0)));
%%
T_F_Approx = Num/(s^2 +s *Denum_1 +Denum_2);
%% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
R_Array=linspace(677,677,1);
%%
fs=1.6e9;
A0=10^(35/20);
gc1  =1.57;
%%
```

```
A_Array = linspace(0.75,0.75,1);
%%
%%
figure;
for Count1=1:length(R_Array)
%%
%%
R =R_Array(1,Count1);
%%
for Count2=1:length(A_Array)
%%
A=A_Array(1,Count2);
%%
C= 1/(A*R*fs);
% %%
RF=R*(A*A)/(gc1*gc1);
%%
f= linspace(0.7*(fs/4),1.3*(fs/4),10000);
%%
w=2*pi*f;
%%
s=1i*w;
%%
filter_res_accurate =20*log10(abs(1./(subs(simplify(S_accurate.
    V_in/V_out)))));
%%
filter_res_approx = 20*log10(abs(subs(T_F_Approx)));
%%
filter_res_number_accurate= double(filter_res_accurate);
```

```
%%
[filter_res_number_MAX_accurate,
    filter_res_number_MAX_index_accurate]=max(
    filter_res_number_accurate);
%%
Count4=0;
%%
for Count3 = 1:length(filter_res_number_accurate)
    if filter_res_number_accurate(Count3) > (
        filter_res_number_MAX_accurate -3)
        f_3dB_accurate = f(Count3);
      break;
    end
end
%%
BW_accurate = 2*(f(filter_res_number_MAX_index_accurate)-
    f_3dB_accurate);
%%
Resonance_Frequency_accurate(Count1,Count2)=f(
    filter_res_number_MAX_index_accurate);
%%
Quality_Factor_accurate(Count1,Count2) = f(
    filter_res_number_MAX_index_accurate)/(BW_accurate);
%%
plot(f,filter_res_accurate);
%%
hold on;
plot(f,filter_res_approx);
%%
```

```
%%
Quality_Factor_approx(Count1,Count2) =((A0+2)*((R*RF)^0.5))/(R+2*
    RF);
%%
f_o_approx(Count1,Count2) = (1/(2*pi*(R*RF)^0.5*C)) * (1/(1+(2/A0)
    )^0.5);
%%
end
end
%%
```

B.2 The transfer function of the gain for the one-op-amp resonator at limited DC-gain and infinite pole of op-amps

As showed below, this MATLAB code computes the transfer function of the gain for a one-op-amp resonator at limited DC-gain, A_0, and an infinite 1st pole, f_p, for the op-amps. It calculates the accurate gain of 1-op-amp resonator using symbolic equations solved by **solve MATLAB function**, as well as, the approximate gain of 1-op-amp resonator at DC-gain, $A_0 \gg 1$. Besides, the condition of $\frac{1}{R_pC_p}=\frac{1}{R_1C_1}=\frac{1}{R_2C_2}$ is assumed to be a function of the tuneable capacitors values, $C_{1,2}$.

The quality factor Q and the center frequency f_0 are also calculated using the accurate and the approximate ways and discussed in the code, they are matched with at an small error $\leq$ 4.1%.

The values, which exploited in this code, are the DC-gain of op-amps, $A_0 = 35$ dB, the resistors values $R_{in} = 1000\ \Omega$, $R_1 = 500\ \Omega$, $R_2 = 250\ \Omega$, $R_p = 1591\ \Omega$, the capacitor value $C_p = 100$ fF at $f_0 = 400$ MHz in our design.

```
clear
clc
```

```
close all
%%
syms A0 s V_in V_1 Rin V_o1 C1 R1 C2 R2 V_out Cp Rp
%%
%% Op_Amp_TF = Adc/(1+(s/w_p));
Op_Amp_TF = A0;
%%
eqn1_accurate = (-1*(V_in-V_1)/Rin) + ((V_1+V_o1)*(s*C1+1/R1)) + ((V_1-V_o1)*(s*C2/(s*C2*R2+1))) == 0;
%%
eqn2_accurate = -1*(V_o1) + V_1*Op_Amp_TF== 0;
%%
eqn3_accurate = -1*(V_out) + (V_o1)*(s*Cp*Rp/(s*Cp*Rp+1)) ==0;
%%
eqns_accurate = [eqn1_accurate eqn2_accurate eqn3_accurate];
S_accurate = solve(eqns_accurate,[V_in V_1 V_o1]);
%%
TF_accurate = simplify(1/(S_accurate.V_in/V_out));
%%
Num = (1/(C1*R1)) ;
% %%
Denum_1 = (1+(1/A0))*(1/(C1*R1)) + (-1+(1/A0))*(1/(C1*R2)) + (1+(1/A0))*(1/(C2*R2)) + (1/(A0*C1*Rin));
% %%
Denum_2 = (1/(C1*R1*C2*R2)) + (1/(C1*C2*R2*Rin*A0));
% %%
T_F_Approx = ((R1/Rin)*Num*s)/(s^2 +s *Denum_1 + Denum_2);
%% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Rin = 1000;
```

```
%%
R1 = Rin/2;
%%
R2 = R1/2;
%%
f_0=400e6;
%%
w_0=2*pi*f_0;
%%
Cp =100e-15;
%%
Rp = 1591;
%%
A0 = 10^(35/20);
%% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
C_deltaf_0 = linspace(0,0,1);
C_deltaQ = linspace(25e-15,41e-15,9);
%%
figure;
%%
for Count1 =1:length(C_deltaf_0)
    for Count2 =1:length(C_deltaQ)
%% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
C1 = (1/(w_0*R1)) - C_deltaQ(Count2) -C_deltaf_0;
C2 = (1/(w_0*R2)) + 2* C_deltaQ(Count2) -C_deltaf_0;
%%
%%
```

```
f= linspace(0.7*f_0,1.3*f_0,10000);
%%
w=2*pi*f;
%%
s=1i*w;
%%
filter_res_accurate =20*log10(abs(subs(TF_accurate)));
%%
filter_res_approx = 20*log10(abs(subs(T_F_Approx)));
%%
filter_res_accurate_numbers = double(filter_res_accurate);
[filter_res_number_MAX_accurate,
    filter_res_number_MAX_index_accurate]=max(
    filter_res_accurate_numbers);
for Count3 = 1:length(filter_res_accurate_numbers)
    if filter_res_accurate_numbers(Count3) > (
        filter_res_number_MAX_accurate -3)
        f_3dB_accurate = f(Count3);
      break;
    end
end
BW_accurate = 2*(f(filter_res_number_MAX_index_accurate)-
    f_3dB_accurate);
%%
Resonance_Frequency_accurate(Count1,Count2)=f(
    filter_res_number_MAX_index_accurate);
%%
Quality_Factor_accurate(Count1,Count2) = f(
    filter_res_number_MAX_index_accurate)/(BW_accurate);
```

```
%%
filter_res_approx_numbers = double(filter_res_approx);
[filter_res_number_MAX_approx,filter_res_number_MAX_index_approx]=
    max(filter_res_approx_numbers);
for Count4 = 1:length(filter_res_approx_numbers)
    if filter_res_approx_numbers(Count4) > (
        filter_res_number_MAX_approx -3)
        f_3dB_approx = f(Count4);
      break;
    end
end
BW_approx = 2*(f(filter_res_number_MAX_index_approx)-f_3dB_approx)
    ;
%%
Resonance_Frequency_approx(Count1,Count2)=f(
    filter_res_number_MAX_index_approx);
%%
Quality_Factor_approx(Count1,Count2) = f(
    filter_res_number_MAX_index_approx)/(BW_approx);
%%
error_Q(Count1,Count2)= 100 * abs(Quality_Factor_accurate(Count1,
    Count2) - Quality_Factor_approx(Count1,Count2)) /(
    Quality_Factor_accurate(Count1,Count2));

error_f_0(Count1,Count2)= 100 * abs(Resonance_Frequency_accurate(
    Count1,Count2) - Resonance_Frequency_approx(Count1,Count2)) /(
    Resonance_Frequency_accurate(Count1,Count2));
%%
plot(f,filter_res_accurate,'-r','LineWidth',2);
```

```
%%
hold on;
%%
plot(f,filter_res_approx,'-b','LineWidth',2);
%%
    end
end
```

B.3 Noise analysis of the 4th-order continuous-time band-pass $\Sigma\Delta$ modulator based on two-op-amp resonators

As below, the code discusses the integrated resistors thermal noise calculated over the bandwidth of band-pass $\Sigma\Delta$ modulator from $393.75MHz$ to $406.25MHz$. It is computed at $f_0 = 400$ MHz, a sampling frequency, $f_s = 4\ f_0$ and a loop-delay, $t_d = 1.5\ T_s$ at $OSR = 64$. The values of A, I_{scale} are equal to 0.75, 60μ, respectively.

```
%%
clear
clc
close all
%%
syms X1 A s Ts fs Xt_star Y_par a1_star X2 g1_star a2_star X3
    a3_star X4 g2_star a4_star Y a5_star f
%%
Integ_TF = (A*fs)/(1i *2*pi*f);
%%
Y_par = exp(-1.5 * Ts * (1i *2*pi*f)) * Y;
%%
```

```
eqn1 = -X1 + Integ_TF*(Xt_star - Y_par * a1_star -X2 * g1_star)
    ==0;
%%
eqn2 = -X2 + Integ_TF*(X1 - Y_par * a2_star)==0;
%%
eqn3 = -X3 + Integ_TF*(X2 - Y_par * a3_star -X4 * g2_star)==0;
%%
eqn4 = -X4 + Integ_TF*(X3 - Y_par * a4_star)==0;
%%
eqn5 = -Y + ((X4 - Y_par * a5_star) *  ((1 - exp(-1 * (1i *2*pi*f)
    * Ts))/ (1i *2*pi*f))) == 0  ;
%%
eqns = [eqn1 eqn2 eqn3 eqn4 eqn5];
S = solve(eqns,[X1 X2 X3 X4 Xt_star]);
%%
%% cofficients of DACs and feedback%%
%%
%%
a1 = 0.58402;
a2 = 0;
a3 = -1*0.145335;
a4= -1*0.860153 ;
a5 = -1*0.37142;
g1 = (1.56)^2;
g2 = (1.59)^2;
% Xt = 10^(-6.72/20);
%%
Iscale = 60e-6;
%%
```

```
A = 0.75;
%%

%%
a1_star = Iscale;
a2_star = (a2/a1) * Iscale * A;
a3_star = (a3/a1) * Iscale * A^2;
a4_star = (a4/a1) * Iscale * A^3;
a5_star = (a5/a1) * Iscale * A^4;
%%
g1_star = g1/(A^2);
g2_star = g2/(A^2);
%%
%Xt_star = (Xt * Iscale)/a1;
%%
%%
Y_X1_subs=1/(subs ((simplify ((S.X1)/Y))));
Y_X2_subs=1/(subs ((simplify ((S.X2)/Y))));
Y_X3_subs=1/(subs ((simplify ((S.X3)/Y))));
Y_X4_subs=1/(subs ((simplify ((S.X4)/Y))));
Y_Xt_star_subs=1/(subs ((simplify ((S.Xt_star)/Y))));
%%
OSR=64;
fs = 1.6e9;
Ts =1/fs;
BW=(fs/(2*OSR));
BW1 = (fs/4) - (BW/2);
BW2 = (fs/4) + (BW/2);
%%
```

```
%%
%% plotting
%% f=linspace(1,4*fs,8000);
f=linspace(BW1,BW2,500);
%%
%%f=linspace(1000,4*fs,500);
%% %%
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
H1I = 20*log10((abs((subs(Y_X1_subs./Y_Xt_star_subs)))));
H2I = 20*log10((abs((subs(Y_X2_subs./Y_Xt_star_subs)))));
H3I = 20*log10((abs((subs(Y_X3_subs./Y_Xt_star_subs)))));
H4I = 20*log10((abs((subs(Y_X4_subs./Y_Xt_star_subs)))));
%%
figure;
plot (f,(20*log10(abs(subs(Y_Xt_star_subs)))));
figure;
H0I=zeros(1,length(f));
hold on;
plot (f,H0I);
%%
plot (f,H1I);
%%
hold on;
plot (f,H2I);
%%
hold on;
plot (f,H3I);
```

```
%%
hold on;
plot (f,H4I);
% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
H1I_square = abs((subs(Y_X1_subs/Y_Xt_star_subs)).^2);
H2I_square = abs((subs(Y_X2_subs/Y_Xt_star_subs)).^2);
H3I_square = abs((subs(Y_X3_subs/Y_Xt_star_subs)).^2);
H4I_square = abs((subs(Y_X4_subs/Y_Xt_star_subs)).^2);
%%
H1I_model = double(trapz(f,H1I_square));
H2I_model = double(trapz(f,H2I_square));
H3I_model = double(trapz(f,H3I_square));
H4I_model = double(trapz(f,H4I_square));
%%
R = linspace(100,5000,100);
Input_Signal = R.*(1.06/a1).*Iscale;
Input_power = 0.5*(Input_Signal.^2);
%%
for i=1:1:length(R)
KT=1.3811e-23 *(27+273);
%%
noise_of_resistor_R= 2*4*KT*R(i);
%%
RF1= R(i)/g1_star;
noise_RF1_to_input= ((R(i)/RF1)^2)*2*4*KT*RF1;
%%
RF2= R(i)/g2_star;
```

```
noise_RF2_to_input=((R(i)/RF2)^2)*2*4*KT*RF2;
%%
Int_1_noise(i)=(noise_of_resistor_R+noise_RF1_to_input)*BW;
%%
Int_2_noise(i)=noise_of_resistor_R*H1I_model;
%%
Int_3_noise(i)=(noise_of_resistor_R+noise_RF2_to_input)*H2I_model;
%%
Int_4_noise(i)=(noise_of_resistor_R)*H3I_model;
%%
Int_5_noise(i)=(noise_of_resistor_R)*H4I_model;
%%
noise_all(i) = Int_1_noise(i)+ Int_2_noise(i) + Int_3_noise(i)+
    Int_4_noise(i)+Int_5_noise(i);
%%
SNR_model(i)=10*log10(Input_power(i)./noise_all(i));
%%
%%
end
figure;
plot(R,SNR_model);
```

B.4 The mathematical model for the two-op-amp resonator using two-stage feed-forward op-amp

As presented below, this MATLAB code computes the transfer function of the gain for a two-op-amp resonator using two-stage feed-forward op-amps. It computes also both of the quality factor Q and the resonance frequency f_0.

```
clear
clc
close all
%%
syms  s V_in V_1 R V_o1 C w f V_out RF V_2 Adc1_star_1 Adc1_star_2
    Adc1 Adc2_1 Adc2_2 wp1 wp2_1 wp2_2 wpc
%%
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

eqn1 = (-1*(V_in-V_1)/R) + ((V_1+V_o1)*s*C) + ((V_1+V_out)/RF)==
    0;
%%
%%
eqn2 =(-1*(V_o1-V_2)/R) + ((V_2+V_out)*s*C)  == 0;
%%
%%
%%
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

 Op_Amp_TF_1st = (((s * Adc1_star_1)/wp1) + Adc1_star_1 + Adc1 *
     Adc2_1)/((1+ (s/wp1)) * (1+ (s/wp2_1)) * (1+ (s/wpc)));
%%
Op_Amp_TF_2nd = (((s * Adc1_star_2)/wp1) + Adc1_star_2 + Adc1 *
    Adc2_2)/((1+ (s/wp1)) * (1+ (s/wp2_2)) * (1+ (s/wpc)));
%%

%%
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
eqn3 = (-1*(V_o1)) + ((V_1)* Op_Amp_TF_1st) ==0;
%
eqn4 = (-1*(V_out)) + ((V_2)* Op_Amp_TF_2nd) ==0;
%
%
eqns = [eqn1 eqn2 eqn3 eqn4];
S = solve(eqns,[V_in V_1 V_2 V_o1]);
%
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
R_Array=677;
%
fs=4*400*1e6;
%
gc1 =1.57;
%
A_Array = linspace(0.1,1,13); %
% A_Array = 0.75; %
% A_Array = 1;
%
for Count1=1:length(R_Array)
%
figure;
%
R =R_Array(1,Count1);
%
for Count2=1:length(A_Array)

%
```

```
A=A_Array(1,Count2);
%%
C= (1/(A*R*fs)) ;
%%
RF=R*(A*A)/(gc1*gc1);
%%
gm1 =22.2e-3;
ro1= 922;
%%
Adc1 = gm1*ro1;
%%
gm2 = 10.3e-3;
ro2= 279;
%%
Adc2_1 = gm2 * (ro2*R)/(ro2+R);
Adc2_2 = gm2 * (ro2*RF)/(ro2+RF);
%%
gm1_star = 80.82e-3;
%%
Adc1_star_1 = gm1_star * (ro2*R)/(ro2+R);
Adc1_star_2 = gm1_star * (ro2*RF)/(ro2+RF);
%%
Cpar1=143e-15;
wp1 = 1/(ro1 * Cpar1);
%%
Cpar2 = 525e-15;
%%
wp2_1 = 1/(((ro2*R)/(ro2+R)) * (Cpar2+C));
wp2_2 = 1/(((ro2*RF)/(ro2+RF)) * (Cpar2+C));
```

```
%%
%%
wpc = 35*wp1;
%%
f= linspace(0.7*(fs/4),1.3*(fs/4),10000);
%%
%%
w=2*pi*f;
%%
s=1i*w;
%%
filter_res=20*log10(abs(1./(subs(simplify(S.V_in/V_out)))));
%%
filter_res_number= double(filter_res);
%%
[filter_res_number_MAX,filter_res_number_MAX_index]=max(
    filter_res_number);
%%
filter_res_number_MAX_3dB=filter_res_number_MAX -3;
%%
for Count3 = 1:length(filter_res_number)
    if filter_res_number(1,Count3) > filter_res_number_MAX_3dB
      f_3dB = f(Count3);
      break;
    end
end
%%
BW= 2*(f(filter_res_number_MAX_index)-f_3dB);
%%
```

```
Resonance_Frequency(Count1,Count2)=f(filter_res_number_MAX_index);
Quality_Factor(Count1,Count2) = f(filter_res_number_MAX_index)/(BW
    );
%%
plot(f,filter_res ,'r','LineWidth',3);
%%
hold on;
%%
% Gain_resontor_transistor_Level=csvread('Gain_reson_TL_2_Oct.
    matlab',1,0);
% plot(Gain_resontor_transistor_Level(:,1),
    Gain_resontor_transistor_Level(:,2),'b--','LineWidth',3);
% %%
Two_op_amp_resonator(Count2, :) = filter_res_number;
end
%%
figure;
%%
subplot(1,2,1);
plot (A_Array,Quality_Factor,'r','LineWidth',3);
end
%%
% Q_transistor_level=csvread('Q_transistor_Level.matlab',1,0);
% %%
% subplot(1,2,2);
% plot(Q_transistor_level(:,1),Q_transistor_level(:,2),'b','
    LineWidth',2);
```

List of Publications

1. Doaa Mahmoud, Michel Vasilevski, Marco Adel, Alhassan said, Marie-Minerve Louerat and Hassan Aboushady, "Two-Op-Amp Resonators Versus One-Op-Amp Resonators in Continuous-Time Bandpass $\Sigma\Delta$ Modulators", will be submitted to IEEE Transactions on Circuits and Systems II.

2. Doaa Mahmoud, Michel Vasilevski, Marco Adel, Alhassan said, Marie-Minerve Louerat and Hassan Aboushady, "A Noise Study for Continuous-Time Bandpass $\Sigma\Delta$ Modulator based on two-op-amp resonators", will be submitted to IEEE Transactions on Circuits and Systems I.

References

Aboushady02. Hassan Aboushady and Marie-Minerve Louërat. Systematic approach for discrete-time to continuous-time transformation of sigma-delta modulators. In IEEE International Symposium on Circuits and Systems, number 4, pages IV–229. IEEE; 1999, 2002.

Aboushady04. Hassan Aboushady and M-M Louerat. Loop delay compensation in bandpass continuous-time/spl sigma//spl delta/modulators without additional feedback coefficients. In 2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No. 04CH37512), volume 1, pages I–1124. IEEE, 2004.

Ali10. Ahmed MA Ali, Andrew Morgan, Christopher Dillon, Greg Patterson, Scott Puckett, Paritosh Bhoraskar, Huseyin Dinc, Mike Hensley, Scott Bardsley, David Lattimore, et al. A 16-bit 250-ms/s if sampling pipelined adc with background calibration. IEEE Journal of Solid-State Circuits, 45(12):2602–2612, 2010.

Ashry11a. Ahmed Ashry and Hassan Aboushady. A 3.6 gs/s, 15mw, 50db sndr, 28mhz bandwidth rf δ σ adc with a fom of 1pj/bit in 130nm cmos. In 2011 IEEE Custom Integrated Circuits Conference (CICC), pages 1–4. IEEE, 2011.

Ashry11b. Ahmed Ashry and Hassan Aboushady. A 4 th order subsampled rf δ adc centered at 2.4 ghz with a sine-shaped feedback dac. In 2011 Proceedings of the ESSCIRC (ESSCIRC), pages 263–266. IEEE, 2011.

Ashry13. Ahmed Ashry and Hassan Aboushady. A 4th order 3.6 gs/s rf/spl sigma//spl delta/adc with a fom of 1 pj/bit. IEEE Transactions on Circuits and Systems I: Regular Papers, 60(10):2606–2617, 2013.

Ashry15. Ahmed Ashry, Diomadson Belfort, and Hassan Aboushady. Phase noise effect on sine-shaped feedback dacs used in continuous-time \ *sigma* \ *delta* adcs. IEEE Transactions on Circuits and Systems I: Regular Papers, 62(3):717–724, 2015.

Beilleau03. N. Beilleau, H. Aboushady, and M.M. Louerat. Systematic approach for scaling coefficients of discrete-time and continuous-time sigma-delta modulators. In 2003 46th Midwest Symposium on Circuits and Systems, volume 1, pages 233–236 Vol. 1, 2003.

Beilleau09. Nicolas Beilleau, Hassan Aboushady, Franck Montaudon, and Andreia Cathelin. A 1.3 v 26mw 3.2 gs/s undersampled lc bandpass σ δ adc for a sdr ism-band receiver in 130nm cmos. In 2009 IEEE Radio Frequency Integrated Circuits Symposium, pages 383–386. IEEE, 2009.

Belfort17. Diomadson R Belfort, Sebastian YC Catunda, and Hassan Aboushady. 4th order capacitively-coupled lc-based σ δ modulator. Microelectronics Journal, 62:99–107, 2017.

Bell19. John Bell and Michael P Flynn. A simultaneous multiband continuous-time δ σ adc with 90-mhz aggregate bandwidth in 40-nm cmos. In ESSCIRC 2019-IEEE 45th European Solid State Circuits Conference (ESSCIRC), pages 1–4. IEEE, 2019.

Benabes97. Philippe Benabes, Mansour Keramat, and Richard Kielbasa. A methodology for designing continuous-time sigma-delta modulators. In Proceedings European Design and Test Conference. ED & TC 97, pages 46–50. IEEE, 1997.

Cathelin17. A. Cathelin. Fully depleted silicon on insulator devices CMOS: The 28-nm node is the perfect technology for analog, RF, mmW, and mixed-signal system-on-chip integration. IEEE Solid-State Circuits Magazine, 9(4):18–26, 2017.

Chae13a. Hyungil Chae. Low Power Continuous-time Bandpass Delta-Sigma Modulators. PhD thesis, 2013.

Chae13b. Hyungil Chae, Jaehun Jeong, Gabriele Manganaro, and Michael P Flynn. A 12 mw low power continuous-time bandpass δ σ modulator with 58 db sndr and 24 mhz bandwidth at 200 mhz if. IEEE Journal of Solid-State Circuits, 49(2):405–415, 2013.

Chae16. Hyungil Chae and Michael P Flynn. A 69 db sndr, 25 mhz bw, 800 ms/s continuous-time bandpass *sigma delta* modulator using a duty-cycle-controlled dac for low power and reconfigurability. IEEE Journal of Solid-State Circuits, 51(3):649–659, 2016.

Danilovic16. Dajana Danilovic, Vladimir Milovanovic, Andreia Cathelin, Andrei Vladimirescu, and Borivoje Nikolic. Low-power inductorless rf receiver front-end with iip2 calibration through body bias control in 28nm utbb fdsoi. In 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pages 87–90. IEEE, 2016.

Fanori15. Luca Fanori, Ahmed Mahmoud, Thomas Mattsson, Peter Caputa, Sami Rämö, and Pietro Andreani. A 2.8-to-5.8 ghz harmonic vco in a 28 nm utbb fd-soi cmos process. In 2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pages 195–198. IEEE, 2015.

Gebreyohannes19. Fikre Tsigabu Gebreyohannes, Marie-Minerve Louërat, and Hassan Aboushady. Design of a 4th-order feed-forward-compensated operational amplifier for multi-ghz sampling frequency continuous-time bandpass sigma-delta modulators. In 2019 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1–5. IEEE, 2019.

Gebreyohannes20. Fikre Tsigabu Gebreyohannes, Jacky Porte, Marie-Minerve Louërat, and Hassan Aboushady. A g m/i d methodology based data-driven search algorithm for the design of multistage multipath feed-forward-compensated amplifiers targeting high speed continuous-time σ δ-modulators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 39(12):4311–4324, 2020.

Jacquet14. David Jacquet, Frederic Hasbani, Philippe Flatresse, Robin Wilson, Franck Arnaud, Giorgio Cesana, Thierry Di Gilio, Christophe Lecocq, Tanmoy Roy, Amit Chhabra, et al. A 3 ghz dual core processor arm cortex tm-a9 in 28 nm utbb fd-soi cmos with ultra-wide voltage range and energy efficiency optimization. IEEE Journal of Solid-State Circuits, 49(4):812–826, 2014.

Jang18. S. Jang, J. Jeong, R. Lu, and M. Flynn. A 16-element 4-beam 1 GHz IF 100 MHz bandwidth interleaved bit stream digital beamformer in 40 nm CMOS. IEEE Journal of Solid-State Circuits, 53(5):1302–1312, 2018.

Kim19. Susie Kim, Cyuyeol Rhee, and Suhwan Kim. A Wide Dynamic Range Multi-Mode Band-Pass Continuous-Time Delta-Sigma Modulator Employing Single-Opamp Resonator with Positive Resistor-Feedback. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019.

Kumar17. Ashish Kumar, Chandrajit Debnath, Pratap Narayan Singh, Vivek Bhatia, Shivani Chaudhary, Vigyan Jain, Stephane Le Tual, and Rakesh Malik. A 0.065-mm 2 19.8-mw single-channel calibration-free 12-b 600-ms/s adc in 28-nm utbb fd-soi using fbb. IEEE Journal of Solid-State Circuits, 52(7):1927–1939, 2017.

Lamarre06. Laurent de Lamarre, Marie-Minerve Louërat, and Andreas Kaiser. Optimizing resistances and capacitances of a continuous-time sigma delta adc. In 2006 13th IEEE International Conference on Electronics, Circuits and Systems, pages 419–422. IEEE, 2006.

Le05. Bin Le, Thomas W Rondeau, Jeffrey H Reed, and Charles W Bostian. Analog-to-digital converters. IEEE Signal Processing Magazine, 22(6):69–77, 2005.

Lechevallier15. Joeri Lechevallier, Remko Struiksma, Hani Sherry, Andreia Cathelin, Eric Klumperink, and Bram Nauta. 5.5 a forward-body-bias tuned 450mhz gm-c 3 rd-order low-pass filter in 28nm utbb fd-soi with¿ 1dbvp iip3 over a 0.7-to-1v supply. In 2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers, pages 1–3. IEEE, 2015.

Leung01. Ka Nang Leung and Philip KT Mok. Analysis of multistage amplifier-frequency compensation. IEEE transactions on circuits and systems I: fundamental theory and applications, 48(9):1041–1056, 2001.

Liu99. Ting-Ping Liu. A 6.5 ghz monolithic cmos voltage-controlled oscillator. In 1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition (Cat. No. 99CH36278), pages 404–405. IEEE, 1999.

Lu10. Cho-Ying Lu, Jose Fabian Silva-Rivas, Praveena Kode, Jose Silva-Martinez, and Sebastian Hoyos. A sixth-order 200 mhz if bandpass sigma-delta modulator with over 68 db sndr in 10 mhz bandwidth. IEEE Journal of Solid-State Circuits, 45(6):1122–1136, 2010.

Lu21. Rundao Lu, Christine Weston, Daniel Weyer, Fred Buhler, Daniel Lambalot, and Michael P Flynn. A 16-element fully integrated 28-ghz digital rx beamforming receiver. IEEE Journal of Solid-State Circuits, 56(5):1374–1386, 2021.

Mas17. Alexandre Mas, Eric Andre, Caroline Lelandais-Perrault, Filipe Vinci dos Santos, and Philippe Benabes. Analog bandwidth mismatch compensation for time-interleaved adcs using fd-soi tech-

nology. In 2017 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1–4. IEEE, 2017.

Mitteregger06. Gerhard Mitteregger, Christian Ebner, S Mechnig, Thomas Blon, Christophe Holuigue, E Romani, A Melodia, and V Melini. A 14b 20mw 640mhz cmos ct/spl delta//spl sigma/adc with 20mhz signal bandwidth and 12b enob. In 2006 IEEE International Solid State Circuits Conference-Digest of Technical Papers, pages 131–140. IEEE, 2006.

Pavan14. Shanthi Pavan and Radha S Rajan. Simplified analysis and simulation of the stf, ntf, and noise in continuous-time \ *delta* \ *sigma* modulators. IEEE Transactions on circuits and systems II: Express briefs, 61(9):681–685, 2014.

Philips04. Kathleen Philips, Peter ACM Nuijten, Raf LJ Roovers, Arthur HM Van Roermund, Fernando Muñoz Chavero, Macarena Tejero Pallarés, and Antonio Torralba. A continuous-time/spl sigma//spl delta/adc with increased immunity to interferers. IEEE Journal of Solid-State Circuits, 39(12):2170–2178, 2004.

R. Schreier. Analog Devices R. Schreier. Oversampling delta-sigma data converters the one-page story.

Sayed20a. A. Sayed, T. Badran, M.-M. Louerat, and H. Aboushady. A 1.5-to-3.0GHz Tunable RF Sigma-Delta ADC with a Fixed Set of Coefficients and a Programmable Loop Delay. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020.

Sayed20b. Alhassan Sayed, Tamer Badran, Marie-Minerve Louërat, and Hassan Aboushady. A 1.5-to-3.0 ghz tunable rf sigma-delta adc with a fixed set of coefficients and a programmable loop delay. IEEE Transactions on Circuits and Systems II: Express Briefs, 67(9):1559–1563, 2020.

Schreier96. Richard Schreier and Boming Zhang. Delta-sigma modulators employing continuous-time circuitry. IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 43(4):324–332, 1996.

Schreier05. Richard Schreier, Gabor C Temes, et al. Understanding delta-sigma data converters, volume 74. IEEE press Piscataway, NJ, 2005.

Shibata12. H. Shibata, R. Schreier, W. Yang, A. Shaikh, D. Paterson, T. C. Caldwell, D. Alldred, and P. W. Lai. A DC-to-1 GHz Tunable RF Delta-Sigma ADC Achieving DR=74 dB and BW=150 MHz at fo =450 MHz Using 550 mW. IEEE Journal of Solid-State Circuits, 47(12):2888–2897, Dec 2012.

Sourikopoulos16. Ilias Sourikopoulos, Antoine Frappé, Andreia Cathelin, Laurent Clavier, and Andreas Kaiser. A digital delay line with coarse/fine tuning through gate/body biasing in 28nm fdsoi. In ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, pages 145–148. IEEE, 2016.

Streel17. Guerric de Streel, François Stas, Thibaut Gurne, François Durant, Charlotte Frenkel, Andreia Cathelin, and David Bol. Sleeptalker: A ulv 802.15. 4a ir-uwb transmitter soc in 28-nm fdsoi achieving 14 pj/b at 27 mb/s with channel selection based on adaptive fbb and digitally programmable pulse shaping. IEEE Journal of Solid-State Circuits, 52(4):1163–1177, 2017.

Thandri03. B. Thandri and J. Silva-Martinez. A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors. IEEE Journal of Solid-State Circuits, 38(2):237–243, 2003.

Yang16. Xi Yang and Hae-Seung Lee. Design of a 4th-order multi-stage feedforward operational amplifier for continuous-time bandpass delta sigma modulators. In 2016 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1058–1061. IEEE, 2016.

Yang18. X. Yang and H.-S. Lee. Design of a 6 th-order Continuous-time Bandpass Delta-Sigma Modulator with 250 MHz IF, 25 MHz Bandwidth, and over 75 dB SNDR. In 2018 IEEE International Symposium on Circuits and Systems (ISCAS), pages 1–5. IEEE, 2018.

Zimmer16. Brian Zimmer, Yunsup Lee, Alberto Puggelli, Jaehwa Kwak, Ruzica Jevtić, Ben Keller, Steven Bailey, Milovan Blagojević, Pi-Feng Chiu, Hanh-Phuc Le, et al. A risc-v vector processor with simultaneous-switching switched-capacitor dc–dc converters in 28 nm fdsoi. IEEE Journal of Solid-State Circuits, 51(4):930–942, 2016.