Characterization of degradation mechanisms and electrical reliability study on GaN-on-Si power transistors

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Caractérisation des mécanismes de dégradation au sein de transistors de puissance à base de GaN sur Si, et étude de leur fiabilité électrique

Characterization of degradation mechanisms and electrical reliability study on GaN-on-Si power transistors

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« God made the bulk; surfaces were invented by the devil » – Wolfgang Pauli

Résumé

Au cours des 30 dernières années, la consommation mondiale d'électricité a plus que doublé (115%) en passant de $10 \cdot 10^3$TWh en 1990 à $23 \cdot 10^3$TWh en 2019. Cette augmentation a engendré la mise en place de réseaux électriques de plus en plus complexes, denses, et interconnectés. En général, l'électricité produite est transportée depuis les centrales électriques vers les zones de consommation sous forme d'un courant alternatif (AC) ayant une fréquence fixe (50Hz en Europe), au travers d'un réseau électrique haute tension réparti sur l'ensemble du territoire. Une fois que cette énergie électrique arrive à proximité des lieux de consommation, sa tension est abaissé (220V en Europe) par le biais de transformateurs, avant d'être définitivement délivrée aux consommateurs afin d'alimenter une large gamme d'applications électriques. Cependant, de nombreuses applications sont alimentées à d'autres gammes de fréquence et de tension que celles fournies par le réseau électrique conventionnel. Par conséquent, il est nécessaire de convertir ces signaux électriques. Le rôle de l'industrie de l'électronique de puissance est de proposer des solutions pour assurer cette conversion électrique, et c'est dans ce cadre que les dispositifs à base de silicium ont été principalement utilisés jusqu'au début des années 2000. Avec l'émergence de nouvelles technologies telles que les véhicules électriques, les chargeurs ultra-rapides, ou encore la croissance des énergies renouvelables, les technologies à base de silicium montrent leurs limites en termes d'efficacité énergétique et de fréquence d'opération. L'industrie de l'électronique de puissance ainsi que les instituts de recherche ont alors commencé à développer des dispositifs de puissance basés sur des semi-conducteurs à grand gap, tels que le carbure de silicium (SiC) ou encore le nitrure de gallium (GaN). Ces matériaux offrent des caractéristiques physiques plus intéressantes que le silicium, notamment en termes de mobilité électronique, de conductivité thermique, ou encore de champ de claquage. Leurs propriétés physiques permettent d'augmenter la puissance des convertisseurs ainsi que leur rendement grâce à des pertes en conduction et en commutation plus faibles. Ces matériaux à grand gap répondent ainsi aux nouvelles exigences du marché.

Avec des applications en radiofréquence (RF) et en optoélectronique, le GaN a également un avenir prometteur dans le domaine des composants de puissance. En effet, ce matériau est un sérieux concurrent du silicium, notamment pour les applications à haute fréquence de fonctionnement (> 2 MHz) et à des tensions modérées (< 900 V). Actuellement, le GaN est utilisé dans les transistors et les diodes de puissance, et devrait avoir de meilleures performances que les dispositifs à base SiC ou de Si. Cela est rendu possible grâce à l'utilisation d'un gaz d'électrons bidimensionnel (2DEG) qui apparait naturellement à l'interface AlGaN/GaN. Il présente une mobilité ($\sim 2000\,\mathrm{cm^2 \cdot V^{-1} \cdot s^{-1}}$) ainsi qu'une vitesse de saturation ($\sim 2{,}5 \cdot 10^7\,\mathrm{cm \cdot s^{-1}}$) des électrons particulièrement élevées. Les applications utilisant des tensions inférieures à 900V occupent une part importante du marché de l'électronique de puissance ($\sim 70\%$) et le GaN est

un matériau particulièrement adapté pour cette gamme de tension.

Bien que le GaN présente des propriétés intéressantes, le développement de dispositifs de puissance à base de ce matériau est soumis à plusieurs défis technologiques, notamment si l'on souhaite rendre la fabrication des dispositifs compatible avec l'industrie CMOS. Le choix du substrat sur lequel est épitaxié le GaN fait partie de ces défis. En effet, cela implique une ingénierie complexe en termes de gestion des contraintes cristallines entre les substrats étrangers (Si ou SiC) et la couche de GaN sur lesquels elle repose. De plus, les architectures de diodes ou de transistors développées constituent également un autre défi majeur dans la mesure où ces dispositifs doivent être conçus pour supporter des tensions et des courants élevés tout en étant énergétiquement efficaces (faible dissipation de puissance en opération). Enfin, la stabilité électrique de ces dispositifs pendant leur fonctionnement est également l'un des défis les plus critiques. En effet, de nos jours, les instabilités électriques des transistors à base d'AlGaN/GaN restent la préoccupation majeure des industries, car elles réduisent la durée de vie des composants et leurs performances électriques empêchant ainsi leur production industrielle.

Les dispositifs à base de GaN sont soumis à plusieurs mécanismes de dégradation dus à différents types de défauts dans la structure qui agissent comme des pièges à électron. Au cours des dernières années, des efforts considérables ont été déployés pour traiter le phénomène de "Current collapse" qui peut aussi bien être observé dans les diodes que dans les transistors de puissance à base de GaN. Il se caractérise par une réduction du courant de sortie après l'application d'une haute tension. La dégradation par injection de porteurs chauds (ou dégradation HCI pour Hot Carrier Injection) est un autre mécanisme rapporté dans les transistors à base de GaN. Cette dégradation se manifeste principalement lors de la commutation de l'état bloqué à l'état passant du dispositif, lorsque le canal est faiblement conducteur et que la tension de drain est élevée conduisant ainsi à une puissance dissipée élevée. Le mécanisme associé à cette dégradation est due à des porteurs ayant acquis une grande quantité d'énergie dans le canal, induisant ainsi des phénomènes de ionisation par impact et donc des dommages importants au sein du dispositif. Lorsqu'une couche diélectrique est intégrée dans l'architecture du transistor de grille, le mécanisme de Time-Dependent Dielectric Breakdown (TDDB) peut également être observé. Il consiste en un claquage de l'oxyde de grille après l'application d'une tension de grille relativement élevée (environ 80% de la tension de claquage du diélectrique) pendant un certain temps. Enfin, l'un des problèmes de fiabilité les plus importants des transistors à base de GaN est l'instabilité de la tension de seuil V_{TH}, également connue sous le nom de Bias Temperature Instability (BTI). Cette dégradation est principalement due au piégeage de porteurs du canal conducteur vers des défauts préexistants dans l'oxyde de grille. Cela entraîne une modification électrostatique locale à l'interface de l'oxyde de grille, et donc des instabilités de V_{TH}. Plusieurs études ont rapporté que le phénomène de piégeage de charges peut affecter de manière significative les performances du dispositif et réduire sa durée de vie.

Actuellement, le CEA-LETI (Commissariat à l'Énergie Atomique et aux Énergies Alternatives - Laboratoire des Technologies de l'Information et de l'Électronique) développe sa propre ligne de production de GaN sur Si, de la plaquette de silicium au module de puissance final. Dans ce contexte, les dispositifs développés au CEA-LETI, qui présentent une architecture disruptive basée sur une grille MOS (Metal-Oxide-Semiconductor), ont démontré d'excellentes performances statiques et dynamiques. Cependant, ces mêmes transistors de puissance sont également soumis à de la dégradation BTI. Les travaux présentés dans ce manuscrit visent à étudier ce phénomène à l'aide de techniques proposées dans la littérature mais aussi de caractérisations

électriques innovantes. Le but de cette thèse est donc de parvenir à une meilleure compréhension des mécanismes physiques sous-jacents qui conduisent à de la dégradation BTI, et de pouvoir ensuite proposer des moyens de les réduire ou de les éliminer. La compréhension des instabilités de tension de seuil a donc conduit aux interrogations suivantes,

- Quelle est la nature des pièges impliquant la dégradation des BTI ?
- Où se trouvent-ils dans la structure du transistor ?
- Par quel mécanisme physique sous-jacent agissent-ils ?
- Comment modéliser les instabilités de tension de seuil ?
- Quelle est l'influence de la longueur de grille sur la dégradation BTI ?

Ces différents aspects sont abordés dans les quatre chapitres qui composent ce manuscrit.

Le chapitre 1 décrit le contexte général dans lequel s'inscrit l'industrie de l'électronique de puissance ainsi que les défis technologique associés au développement de nouvelles applications à base de GaN. Le positionnement des technologies à base de GaN sur le marché de l'électronique de puissance est également présenté. Dans une seconde partie, nous présentons les propriétés du GaN ainsi que les avantages qu'il offre par rapport à ses concurrents (Si et SiC) en termes de caractéristiques physiques intrinsèques lorsqu'il est intégré dans un dispositif de puissance. Les propriétés du gaz électronique bidimensionnel 2DEG à l'interface AlGaN/GaN sont également présentées. Dans un troisième temps, les différents défis technologiques liés à l'épitaxie du GaN sur des substrats étrangers tels que les substrats de Si, de SiC, ou de saphir sont également discutés. Nous soulignons également le fait que l'obtention de dispositifs de puissance compétitifs à base de GaN constitue un défi majeur. En outre, différentes architectures de diodes et de transistors proposées dans la littérature pour exploiter les propriétés intéressantes du 2DEG sont également décrites. Leurs principes de fonctionnement ainsi que leurs avantages et inconvénients sont également discutés. Enfin, les différents mécanismes de dégradation auxquels sont soumis les composants à base de GaN sont également décrits. Les problématiques liées aux instabilités de V_{TH} (BTI) sont développées de manière plus exhaustive, ainsi que les différentes méthodes de mesure permettant de les caractériser.

Le chapitre 2 est consacré à l'identification des pièges associés à la dégradation BTI au sein des transistors développés dans le CEA-LETI, et est composé de trois parties. La première donne un aperçu de la littérature sur la dégradation BTI rapportée sur deux architectures différentes de transistors à base de GaN. Les mesures expérimentales d'instabilités de V_{TH} obtenues sous tension de grille positive et négative sont décrites, ainsi que les mécanismes physiques sous-jacents. La deuxième partie concerne l'étude des instabilités de V_{TH} obtenues sous tensions de stress de grille négatives (aussi appelé dégradation nBTI pour negative Bias Temperature Instability). Les résultats expérimentaux ont montré que les variations de V_{TH} révèlent deux constantes de temps, espacées par des phases stables. Une étude approfondie de ce comportement est présentée dans cette même partie, et révèle l'influence des pièges situés dans l'épitaxie. Les pièges identifiés sont en fait des atomes de carbone situés en site azote dans la maille cristalline du GaN (C_N), et sont très abondants dans la couche de GaN dopé au carbone (GaN:C) utilisé pour augmenter la tenu en tension du transistor. Enfin, la troisième partie est consacrée à une étude approfondie de l'influence de la tension de stress de grille positive sur les instabilités de V_{TH}

(également appelé dégradation pBTI pour positive Bias Temperature Instability). Les mesures effectuées à différente températures et tensions de stress de grille ont conduit à des conclusions ont permis de mieux comprendre l'origine de la dégradation pBTI. En effet, ces résultats ont mis en évidence la présence de deux populations de pièges agissant par le biais de mécanismes différents sur les instabilités de V_{TH}. L'un d'entre eux est lié à des pièges C_N dans le GaN:C, tandis que l'autre est associé à une bande de défauts dans Al_2O_3, située au-dessus de la bande de conduction du GaN. Lorsqu'une tension de stress de grille inférieure à $1,5$V est appliquée, une ionisation des pièges C_N neutres ("0" $\rightarrow$ "1") se produit conduisant ainsi à une augmentation brutale de V_{TH} de l'ordre de $0,2$V. En revanche, lorsqu'une tension de stress de grille supérieure à $1,5$V est appliquée, un mécanisme de piégeage d'électrons dans les défauts préexistants de Al_2O_3 est activé, ce qui conduit à une augmentation continue de V_{TH} avec le temps de stress.

Le chapitre 3 concerne la modélisation des instabilités de tension de seuil obtenues sous tension de stress de grille positive (pBTI), et se compose de cinq parties. La première présente le modèle Shockley-Read-Hall (SRH) qui permet d'illustrer les processus de capture et d'émission de charges au sein des pièges. Cependant, la principale limite de ce modèle est que l'influence de la température sur le processus de piégeage est très faible alors qu'en réalité, les instabilités de V_{TH} sont très dépendantes de la température. Le modèle SRH étant inadéquat pour décrire le comportement de la dégradation BTI en fonction de la température, le modèle NRMP (Non-Radiative Multi-Phonon) est alors présenté dans la deuxième partie. Il peut être considéré comme une amélioration du modèle SRH prenant en compte la dépendance en température des pièges. Bien que le modèle NRMP soit capable de reproduire qualitativement les instabilités de V_{TH}, il reste tout de même imprécis, probablement à cause des nombreuses approximations physiques sur lesquelles il est basé. Etant donné que le modèle NRMP présente certaines limites pour modéliser la dégradation BTI, le modèle CET (Capture Emission Time) est alors exploré dans la troisième partie du chapitre. Bien que ce modèle soit basé sur un réseau RC n'étant pas pleinement représentatif de la réalité physique, il demeure bien adapté pour décrire et même prédire quantitativement les instabilités de V_{TH}. En revanche, nous verrons qu'il est assez contraignant d'ajuster ce modèle, basé sur une extraction de carte CET. C'est précisément pour cette raison que la quatrième partie propose une méthode innovante développée au cours de cette thèse pour extraire automatiquement les cartes CET. Enfin, la cinquième et dernière partie concerne la modélisation des instabilités de tension de seuil à différentes températures, ainsi que l'analyse approfondie des résultats.

Enfin, le chapitre 4 est dédié à l'influence des propriétés géométriques de la grille sur les instabilités de V_{TH} obtenues sous tension de stress de grille positive (pBTI). Ce chapitre est composé de deux parties. La première présente une étude sur les décalages des caractéristiques $I_D(V_G)$ et $C(V_G)$ obtenus sous diverses valeurs de tensions de stress de grille positives. Nous présentons notamment un dispositif expérimental innovant développé au cours de cette thèse qui permet de mesurer simultanément la dérive des deux caractéristiques au cours d'un même stress de grille. Sur la base des résultats expérimentaux obtenus et de simulations TCAD complémentaires, il est possible de déduire où se situe les pièges à l'interface de l'oxyde de grille. Le décalage de la caractéristique $I_D(V_G)$ a été attribué au piégeage des charges aux coins de la grille, tandis que la dérive de caractéristique $C(V_G)$ a été associé au piégeage ayant lieu au en fond de grille. La deuxième partie traite de l'influence de la longueur de grille L_G sur la dégradation pBTI. Il a été observé que la dégradation pBTI diminue lorsque L_G diminue à une tension de stress de grille fixe. Cela est due à une augmentation de la tension de seuil initiale à mesure que L_G

diminue, impliquant ainsi une réduction du champ électrique dans l'oxyde de grille et donc une dynamique de piégeage d'électrons moins importante au cours du stress de grille. D'autres simulations TCAD ont été effectuées pour mieux comprendre la relation entre la longueur L_G et la tension de seuil initiale.

Bien que les conclusions tirées au cours de cette thèse aient permis d'avoir une meilleure compréhension de l'origine des instabilités de tension de seuil, celle-ci peut encore être améliorée. En effet, dans le chapitre 2, nous avons mis en évidence la présence d'une bande de défauts dans l'Al_2O_3 située sous la bande de valence du GaN dans le cadre de l'étude nBTI. Cependant, cette bande de défauts n'a pas été caractérisée car sa signature électrique apparaît après des temps de stress de grille très longs ($> 10^3$ s) et à haute température. Pour la caractériser, des mesures BTI pourraient alors être réalisées sous rayonnement Ultra-Violet (> 3.4 eV), générant ainsi des trous libres dans le GaN, venant se piéger plus rapidement dans l'Al_2O_3. Des extractions de cartes CET sous tension de stress de grille négative (comme réalisé dans le chapitre 3) pourraient également permettre de déduire l'énergie liée à cette bande de défauts Al_2O_3 afin d'identifier la nature des pièges qui la composent. Pour aller plus loin, une étude de l'influence de la longueur de grille sur les transitoires nBTI pourrait également être menée. En effet, à l'heure actuelle, il n'existe pas d'explication cohérente pour décrire ce comportement particulier. Par ailleurs, bien que les simulations TCAD aient permis de mieux comprendre les mécanismes physiques à l'origine de la dégradation BTI, il est encore difficile de reproduire quantitativement cette dernière. Il est donc nécessaire de développer davantage la compréhension physique du dispositif afin de consolider les modèles mis en œuvre dans les simulations TCAD. Enfin, toutes les études menées dans cette thèse ont été réalisées en fixant la tension de drain à 0V lors de l'application d'une tension de stress de grille négative, alors que les transistors testés sont conçus pour supporter des tensions de drain élevées de plusieurs centaines de volts. Même si les études ont amélioré notre compréhension de la dégradation BTI, le comportement de la dérive de V_{TH} pendant l'application d'une tension de drain élevée doit être étudié, et reste un domaine de recherche nécessaire avant la commercialisation des transistors développés au CEA-LETI.

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List of abbreviations and symbols

Abbreviation

2DEG	2-Dimensional Electron Gas
AC	Alternating Current
ALD	Atomic Layer Deposition
BB	Back-Barrier
BTI	Bias Temperature Instability
CAVET	Current Aperture Vertical Electron Transistors
CEA	French Alternative Energies & Atomic Energy Commission
CET	Capture Emission Time
CMOS	Complementary Metal-Oxide-Semiconductor
D-mode	Depletion-mode
DC	Direct Current
DIBL	Drain-Induced Barrier Lowering
DLTS	Deep Level Transient Spectroscopy
E-field	Electric field
E-mode	Enhanced-mode
FET	Field-Effect Transistor
FP	Field Plate
GaN:C	Carbon-doped GaN
GaN:UID	UnIntentionally Doped GaN
GIT	Gate Injection Transistor
HCI	Hot Carrier Injection
HEMT	High-Electron-Mobility Transistor
HK	High-κ layer
HSE	Heyd-Scuseria-Ernzerhof
ICP-RIE	Inductively Coupled Plasma - Reactive Ion Etching
IGBT	Insulated Gate Bipolar Transistor
IL	Inter-Layer
IPM	Intelligent Power Module
LDA	Local-Density Approximation
LETI	Information Technologies & Electronics Laboratory
MIS	Metal-Insulator-Semiconductor
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal-Oxide-Semiconductor
MOSc	Metal-Oxide-Semiconductor-Channel
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSM	Measurement-Stress-Measurement
N-Off	Normally-Off

N-On	Normally-On
NBTI	Negative BTI
NRMP	Non-Radiative Multi-Phonon
OG-FET	Oxide GaN interlayer FET
OTF	On-The-Fly
PBTI	Positive BTI
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
RF	Radio-Frequency
RTCVD	Rapid Thermal Chemical Vapor Deposition
RTN	Random Telegraph Noise
SCE	Short Channel Effect
SEM	Scanning Electron Microscope
SNR	Signal to Noise Ratio
SRH	Shockley-Read-Hall
TAT	Trap Assisted Tunneling
TCAD	Technology Computer-Aided Design
TDDB	Time-Dependent Dielectric Breakdown
TDDS	Time-Dependent Defect Spectroscopy
TEM	Transmission Electron Microscopy
ToF-SIMS	Time-of-Flight Secondary Ion Mass Spectrometry
TRRG	Through Recessed and Regrowth Gate
UV	Ultra-Violet
WGFMU	Waveform Generator Fast Measurement Unit
WKB	Wentzel–Kramers–Brillouin
XPS	X-Ray Photo-electron Spectroscopy

Symbol

ΔV_{THC}	Shift of $C(V_G)$ characteristic
ΔV_{THI}	Shift of $I_D(V_G)$ characteristic
ΔV_{TH}	Threshold voltage shift
$\hbar$	Reduced Planck constant
$\overrightarrow{E_{pz}}$	Piezoelectric electric field
$\overrightarrow{E_{sp}}$	Spontaneous electric field
$\overrightarrow{E}$	Electric-field
$\overrightarrow{F}$	Parent vector
$\overrightarrow{O}$	Offspring vector
$\overrightarrow{P_{pz}^{AlGaN}}$	Piezoelectric polarization in AlGaN
$\overrightarrow{P_{pz}^{GaN}}$	Piezoelectric polarization in GaN
$\overrightarrow{P_{pz}}$	Piezoelectric polarization
$\overrightarrow{P_{sp}^{AlGaN}}$	Spontaneous polarization in AlGaN
$\overrightarrow{P_{sp}^{AlGaN}}$	Spontaneous polarization in GaN
$\overrightarrow{P_{sp}}$	Spontaneous polarization
$\overrightarrow{P}$	Polarization
$\overrightarrow{U_i}$	Eigenvector
Φ_b	Energy barrier
Ψ_s	Surface potential
Θ_R	Etching angle

α_f	Weibull distribution intercept
α_V	Varshni coefficient
β_D	Debye coefficient
β_f	Weibull distribution slope
β_i	Ideality factor
χ	Mole fraction
ϵ_R	Relaxation energy
$\epsilon_{Al_2O_3}$	Al_2O_3 dielectric permittivity
ϵ_{GaN}	GaN permittivity
ϵ_j	Strain field parameter
ϵ_{ox}	Dielectric constant of an oxide layer
ϵ_r	Relative permittivity
ϵ_{00}	Vacuum permittivity
λ_i	Eigenvalue
λ_w	Wavelength
μ_n	Electron mobility
$\mu_{n,p}$	Electron or hole mobility
ω	Pulsation
ρ	Resistivity
σ_p	Hole capture cross section
σ_P	Polarization charge
σ_s	Charge capture cross section
σ_{AlGaN}	AlGaN charge polarization
σ_{fixed}	Net positive charge plane
σ_{GaN}	GaN charge polarization
σ_{pz}^{AlGaN}	Effective surface charge induced by $\overrightarrow{P_{pz}^{AlGaN}}$
σ_{sp}^{AlGaN}	Effective surface charge induced by spontaneous $\overrightarrow{P_{sp}^{AlGaN}}$
σ_{sp}^{GaN}	Effective surface charge induced by $\overrightarrow{P_{sp}^{GaN}}$
τ_1	First time constant of nBTI stress transient
τ_2	Second time constant of nBTI stress transient
τ_r	Time constant on BTI recovery transient
τ_s	Time constant on stress transient
τ_c	Capture time constants
τ_e	Emission time constants
τ	Time constant
a_0	Lateral lattice constant of Wurtzite cell
a_x	a_0 with constraint
B_V	Breakdown voltage
b_w	Bowing parameter
BFoM	Baliga's figure of merit
c_{ps}	Trap capture rate
c_0	Height of the wurtzite unit cell
c_x	c_0 with constraint
C_{ij}	GaN elastic constant
C_{max}	Maximum of $C(V_G)$ characteristic
C_{min}	Minimum of $C(V_G)$ characteristic
C_{SW}	Switch capacitance
C	Capacitance
D_{ot}	Defect density
DF	Duty-factor
e_{ps}	Trap emission rate
E_Γ	Gap energy

E_C	Energy level of conduction band minimum
E_F	Fermi level
E_r	Relaxation energy level
E_t	Trap state level
E_V	Energy level of valence band maximum
E_a	Activation energy
E_{cost}	Error value
E_{crit}	Maximum electric field at the onset of avalanche breakdown
e_{ij}	Piezoelectric constant
e	Elementary charge of an electron
f_c	Cutoff frequency
f_t	Filling rate
f	Frequency
g_d	Degeneracy factor
g_m	Transconductance
$g_p(\tau)$	Probability density
$g_{m,max}$	Maximum transconductance
G	Bivariate gaussian
g	Normalized trap density
h	Planck constant
I_D	Drain current
I_S	Source current
$I_{D,On}$	Drain current at On-state
$I_{D,0}$	Initial drain current
I_{Dis}	Displacement current
I_{Leak}	Gate leakage current
I_{n0}	Nominal current
JFoM	Johnson's figure of merit
k_B	Boltzmann constant
k_T	Thermal conductivity
L_G	Gate length
L_{GD}	Gate to drain distance
L_{GS}	Gate to source distance
m_h	Hole effective mass
m_t	Hole tunneling mass
m	Radius of the gate corner
$N^0_{Acceptor}$	Neutral acceptor states
N^0_{Donor}	Neutral donor states
N_A	Acceptor concentration
N_D	Donor concentration
n_s	Charge density in 2DEG
N_t	Trap density
N_V	Effective valence band density of states
n_v	Volume charge density
N_{fixed}	Fixed charge density
$N_{n,p}$	Free carrier density
N_{pop}	Vector number
n	Free electron density
p_a	Probability of a trap being at state A
p_b	Probability of a trap being at state B
p_c	Probability of a trap being at state C
p_s	Hole concentration in the channel
p	Free hole density
Q_{fixed}	Fixed charge surface
Q_{SC}	Charge in the semiconductor

q	Elementary charge
R_D	Recess depth
R_s	Sheet resistance
R_{On}	On-resistance
R	Resistance
SS	Sub-threshold slope
S	Huang-Rhys factor
$t_{Al_2O_3}$	Al_2O_3 gate oxide thickness
t_0	Initial delay
t_{2DEG}	2DEG thickness
t_{AlGaN}	AlGaN thickness
$t_{extract}$	Time to extract V_{TH}
t_{ox}	Oxide thickness
T_P	Time associated with a period
t_{relax}	Recovery time
$t_{response}$	Trap response time
$t_{s,max}$	Maximum stress time
$t_{s,min}$	Minimum stress time
t_{stress}	Stress time
t_s	Thickness related to R_s
T_{tunnel}	Tunnel transparency
TTF	Time-to-Failure
T	Temperature
t	Time
u_0	Distance of Ga-N bond
U	Voltage acrross a capacitor
V_D	Drain voltage
v_d	Charge velocity
V_G	Gate voltage
V_{FB}	Flat band potential
$V_{GStress}$	Gate voltage stress
V_H	Nomalized gate voltage
V_{On}	Turn-on voltage
V_{ov}	Overdrive voltage
V_{ox}	Potential within an oxide layer
v_{sat}	Charge saturation velocity
$V_{TH,0}$	Initial threshold voltage
V_{TH}	Threshold voltage
v_{th}	Thermal velocity
W_G	Gate width
x_t	Trap position
$Y(V_G)$	Maserjian function
Y_{exp}	Experimental value
Y_{model}	Calculated value
C_{Ga}	Carbon in Ga site of GaN lattice
C_N	Carbon in N site of GaN lattice
N_{Ga}	Ga site occupation by N in GaN lattice
N_i	Interstitial position of N in GaN lattice
t_{BD}	Device breakdown time
V_{Ga}	Ga vacancy in GaN lattice
V_N	Nitrogen vacancy in GaN lattice

Contents

General introduction

Worldwide electricity consumption has more than doubled in the last 30 years, resulting in increasingly complex and interconnected electricity networks. Generally, electricity is transported from power plants to consuming areas in Alternating Current (AC) form via a high-voltage network spanned throughout the country. However, many electrical applications are supplied by direct current (DC) or alternating current (AC) at other frequency and voltage ranges than those provided by the conventional electrical network. Therefore, electrical conversion is necessary for many applications. The role of the power electronics industry is to propose solutions to ensure this electrical conversion. For this purpose, silicon-based devices were mainly used in power electronics. However, with the emergence of new technologies such as electric vehicles, ultra-fast chargers, or the growth of renewable energies, silicon-based technologies are demonstrating their limits in terms of efficiency. As a result, the power electronics industry as well as research institutes began to develop power devices based on wide band gap semiconductors, such as silicon carbide (SiC) or gallium nitride (GaN). Such materials offer physical characteristics (electron mobility, thermal conductivity, breakdown electric-field) better than those of silicon. Their physical properties enable to increase the converters power as well as their efficiency thanks to lower conduction and switching losses. These wide band gap materials thus address the new market requirements.

Besides its applications in radio-frequency (RF) and optoelectronics, GaN also has a promising future in power technologies. Indeed, this material is a serious challenger for silicon in the power device market, especially for applications with high operating frequencies and moderate voltages. Currently, GaN is used in power transistors and diodes, and is expected to have better performances than SiC and Si-based devices. This is possible due to the natural formation of a two-dimensional electron gas 2DEG at the AlGaN/GaN interface, which has a particularly high conductivity. Applications using voltages below 650V occupy an important part of the power device market (mainly related to the domestic voltage of 230V in Europe), and GaN is a material particularly suited to medium voltage and power sources. However, although GaN has interesting properties, the development of GaN-based power devices is subjected to several technological challenges, especially if we intend to make the fabrication of GaN-based devices compatible with the CMOS (Complementary Metal-Oxide-Semiconductor) . The substrate choice on which GaN is grown is one of those challenges. Indeed, this implies a complex engineering around the constraints management between the epitaxial GaN layer and the foreign substrates (Si or SiC) on which it is grown. Moreover, the diode or transistor architectures developed are also another major challenge, in the way that these devices must be designed to sustain high voltages and transmit high currents while limiting leakage currents and Joule effect losses. Finally, the electrical stability of theses device during operation is one of the most

critical challenges.

Indeed, nowadays the electrical instabilities of AlGaN/GaN based transistors remain the major concern since they reduce the devices lifetime and prevent their commercialization. GaN-based devices are subject to several degradation mechanisms due to different types of defects within the structure, which act as carrier traps. In recent years, considerable efforts have been made to address the "Current collapse" phenomena, which can be observed on power diodes or GaN-based transistors. It is characterized by an output current reduction after a high voltage application during a certain time period. Hot Carrier Injection (HCI) degradation is another type of degradation reported in GaN-based transistors. It mainly appears by switching from the Off to the On-state, when the channel is weakly conductive and the drain voltage is high, leading to a high dissipated power. The mechanism associated with this degradation consists in a trapping of the carriers having acquired a high energy amount in the channel, resulting in important damage within the device. When a dielectric layer is integrated in the gate transistor architecture, Time-Dependent Dielectric Breakdown (TDDB) mechanism can also be observed. It consists in the gate oxide breakdown after the application of a relatively low gate voltage during a certain time. Finally, one of the most important reliability issues in GaN-based transistors are the threshold voltage V_{TH} instabilities which is also known as Bias Temperature Instability (BTI) . This degradation is mainly due to carriers trapping from the conductive channel towards pre-existing defects in the gate oxide, resulting in local electrostatic modification at the gate oxide interface, and thus V_{TH} instabilities. Several studies reported that the charge trapping phenomenon can significantly affect the device performance and reduce its lifetime.

Currently, CEA-LETI (French Alternative Energies & Atomic Energy Commission - Information Technologies & Electronics Laboratory) is developing its own GaN-on-Si production line, from the silicon wafer to the final power module. In this context, the devices developed at CEA-LETI, featuring a disruptive architecture based on a MOS (Metal-Oxide-Semiconductor) gate, have demonstrated excellent static and dynamic performances. However, power transistors developed at CEA-LETI are also subjected to BTI degradation. Consequently, the works presented in this manuscript aim to study this phenomenon with techniques proposed in the literature but also with innovative electrical characterizations. The purpose is to achieve a better understanding of the underlying physical mechanisms that lead to BTI degradation, and then to be able to propose ways to reduce or eliminate them. The understanding of threshold voltage instabilities has raised the following questions,

- What is the nature of the traps involving BTI degradation?
- Where are they within the transistor structure?
- By which underlying physical mechanism do they act?
- How to model threshold voltage instabilities?
- What is the influence of the gate architecture layout on BTI degradation?

These different aspects will be discussed through the four chapters that compose this manuscript.

A general context in which the power electronics industry is evolving as well as challenges concerning new applications will be provided in chapter 1. It will also present the GaN-based technologies positioning in the power electronics market. In a second part, we will present the GaN

material, as well as the benefits it offers compared to its competitors in terms of intrinsic physical characteristics when it is integrated in a power device. Properties of the Two-Dimensional Electron Gas 2DEG at the AlGaN/GaN interface will also be presented. In a third step, the different technological challenges related to the GaN epitaxy on foreign substrates such as silicon or SiC substrates will also be discussed. We will also highlight the fact that it is a major challenge to obtain competitive GaN-based power devices. Furthermore, different diode and transistor architectures proposed in the literature to exploit the interesting 2DEG properties will be also described. Their operating principles as well as their advantages and inconveniences will also be discussed. Naturally, the issues associated with V_{TH} instabilities will be further developed, as well as the different measurement methods enabling to characterize them.

Chapter 2 is dedicated to traps identification associated to BTI degradation on transistors developed in CEA-LETI, and is composed of three sections. The first one will provide a literature overview on BTI degradation reported on two different GaN-based transistor architectures. Experimental threshold voltage instabilities obtained under positive and negative gate voltage will be described, as well as the associated underlying physical mechanisms. The second part will concern the V_{TH} instabilities study obtained under negative gate voltage. Experimental results showed that threshold voltage variations revealed two time constants, spaced by stable phases. An in-depth study of this curious V_{TH} behavior will be presented in this section, and will reveal the influence of traps located in the epitaxy. Finally, the third section will be dedicated to an in-depth study about the positive gate voltage stress influence on V_{TH} instabilities. Measurements performed at several temperatures and under different positive gate voltage stresses have led to interesting conclusions that have improved our understanding of pBTI degradation. Indeed, these results highlighted the presence of two traps populations acting through different mechanisms on the V_{TH} instabilities.

Chapter 3 concerns the modeling of threshold voltage instabilities obtained under positive gate stress, and is made up of five parts. The first one will introduce the Shockley-Read-Hall (SRH) model which enables the modeling of charges capture and emission processes within the traps. However, the main limitation of this model is that the influence of temperature on the trapping process is very low, while the V_{TH} instabilities are very temperature dependent. Since the SRH model is inadequate to describe the BTI degradation behavior as a function of temperature, the NRMP (Non-Radiative Multi-Phonon) model will be then presented in the second part. It can be considered as an improvement of the SRH model taking into account the traps temperature activation. Although it is able to reproduce qualitatively the experimental V_{TH} instabilities, we will see that the NRMP model remains inaccurate, probably due to several physical approximations on which it is based. Since the NRMP model has some limitations for BTI degradation modeling, the CET (Capture Emission Time) map is then explored and will be described in the third part of the chapter. Although the model is based on an RC network which is probably far from the physical reality, it appears to be very suited for describing and even predicting quantitatively the V_{TH} instabilities. On the other hand, we will see that it is also quite constraining to adjust the model which is based on a CET map extraction. It is precisely for this reason that the fourth section proposes an innovative method developed during this thesis to automatically extract the CET maps. Finally, the fifth and last section concerns the modeling of threshold voltage instabilities at different temperatures, and where a thorough analyze of the results will be exhibited.

Finally, chapter 4 is dedicated to the influence of the gate layout on the threshold voltage instabilities obtained under forward gate voltage stress, and is composed of two parts. The first one will present a study on the difference between the shifts of the $I_D(V_G)$ and $C(V_G)$ characteristics obtained under various gate stress voltages. We will present an innovative experimental setup developed during this thesis to simultaneously measure the differences between both characteristics. Based on the experimental results and complementary TCAD simulations, it has been possible to know where the trap density is located at the gate oxide interface. Indeed the $I_D(V_G)$ characteristic shift was attributed to charge trapping at the gate corners, while the $C(V_G)$ drift is related to the gate bottom. The second part will discuss the gate length influence on the BTI degradation obtained under positive gate stress. Indeed, it has been observed that the BTI degradation decreases as the gate length L_G decreases under constant stress due to an increase in the initial threshold voltage with length. It implies a variation of the electric field in the gate oxide which influences the threshold voltage shift. Further TCAD simulations have been carried out to better understand the relationship between the L_G and the initial threshold voltage.

Finally, all the points addressed in these four chapters will be discussed in a general conclusion, where perspectives to further understand the V_{TH} instabilities origin will also be presented.

1 General context

In a first time, a general description of the GaN-based technologies position in the power electronics market is given. The physical properties of AlGaN/GaN hetero-structure are thoroughly described in the 2nd section, as well as their compatibility with power applications. In the 3rd section, the various GaN-based transistor and diode architectures are described in detail. Finally, the reliability issues commonly encountered in these GaN-based devices, as well as their related underlying mechanisms, are discussed in the 4th section.

Contents

1.1 Context

Since 1990, the global electricity consumption has increased from 10 to 23 thousands TWh in 2019, corresponding to an increase of 115%, as shown in Figure 1.1 [1]. In 2019, the total electricity consumption in France reached 538TWh. The majority of this energy was supplied by the nuclear industry (71%), with a fleet of 19 nuclear power plants spread throughout the country. The remaining 30% was supplied by hydroelectric installations (11%), by renewable energies (11%) and finally by fossil energies (8%) [2].

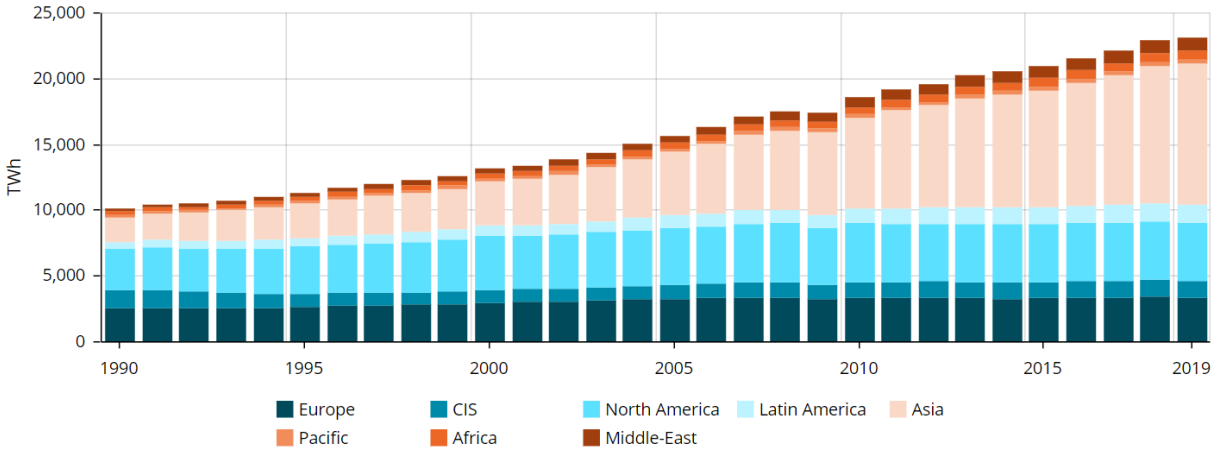

Figure 1.1. Global electricity consumption as a function of time from 1990 to 2019, split by region [1].

All the electricity produced by the power plants must then be brought to the consumption regions. It is therefore transported in the form of an Alternative Current (AC) through a high voltage network spread over the whole territory. The high voltage is then lowered by transformers close to the consumption places in order to limit the power losses by Joule heating during the transport. However, many electrical applications are supplied by Direct Current (DC), or AC at others voltage and frequency ranges than those provided by classical electrical network. Therefore, the electrical conversion provided by the conventional distribution network into a suitable form enabling the use of an electrical application is necessary. Conversely, the conversion of the direct current (produced by photovoltaic power plant for example) towards AC must be also possible in order to be transmitted to the classical electrical network. Consequently, electrical signal conversion is necessary for many applications. The role of power electronic industry is to propose solutions to ensure this electrical conversion. In a more exhaustive way, power electronic designates the circuits and power devices operating in variable frequencies and power ranges.

With the development of renewable energies, new demands such as ultra-fast chargers, wireless charging and the development of electric vehicles, the power device market is increasing considerably. It is expected to reach a value of 35 billion dollars in 2022, notably with a strong growth in demand for power integrated circuits, as shown in Figure 1.2-left. Within this market, low-voltage power devices calibrated to operate below 900V represent the most important sector in 2017, as it can be noticed in Figure 1.2-right.

To perform the various functions of electrical energy conversion, power circuits are mainly com-

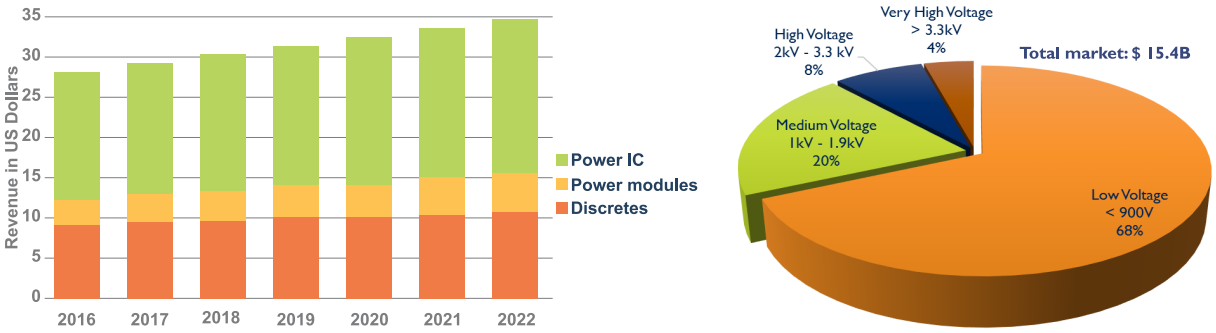

Figure 1.2. Left - Market size for power devices from 2016 to 2022 [3]. **Right -** Market size for power devices in power electronics, for different voltage rating, in 2017 [4].

posed of power transistors and diodes. For example, Figure 1.3 illustrates a simplified diagram circuit of three-phases inverter that enables a conversion from DC to AC signal. It provides a three-phase alternative current from a DC signal supplied by a solar cell in this case.

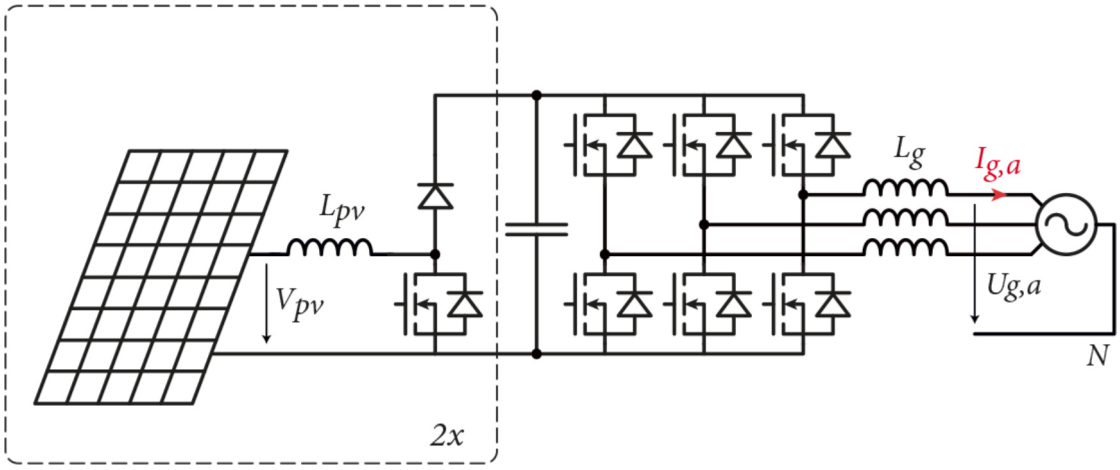

Figure 1.3. Simplified electrical schematic of a three-phase inverter that provides a three-phase alternative current from a DC signal supplied solar cell [5].

Unfortunately, the non-ideality of power devices results in power losses that decrease the power conversion efficiency. There are three types of losses during the operation, related to conduction, leakage currents, and switching events. Although it depends on the device switching frequency, conduction and switching losses are generally the highest, while the one associated with leakage current being lower [6]. The main challenge in power electronics is therefore to develop power transistors and diodes with the highest possible efficiency in order to minimize energy losses.

Until the early 2000s, silicon-based devices were mainly used in power electronics. The different available transistor architectures enabled the use of many applications operating at various powers and frequencies (Figure 1.4) [6]. Among these transistors, the Si-based power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is preferred for high operating frequencies, from 10kHz to several hundreds of kHz, and with low power. On the other hand, the IGBT (Insulated Gate Bipolar Transistor) is preferred for high power and high voltage applications, as shown in Figure 1.4. However, silicon-based technologies have limitations with

the emergence of new demands in terms of operating frequency, power and efficiency. Indeed, the silicon intrinsic properties are incompatible for certain applications in terms of breakdown voltage, On-state resistance, and thermal conductivity. As a result, research as well as power electronics industry started to develop power devices based on wide band gap semiconductors, such as gallium nitride (GaN).

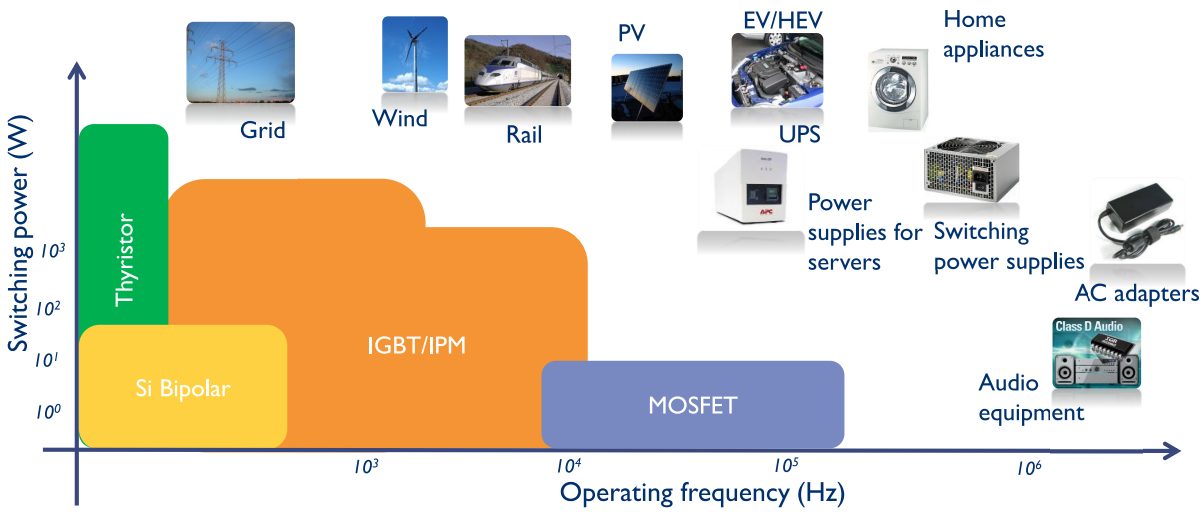

Figure 1.4. Silicon Power device technology positioning in 2018 [4].

With applications in optoelectronics and radio-frequency (RF), GaN is also promising in power technologies. Indeed, this material is a serious competitor to Si in the power device market, especially for applications with high operating frequencies and moderate voltages. Nowadays, GaN is used in power transistors and diodes, and is expected to have better performances than the Si-based devices. It is also a direct competitor to an another wide band gap material which is silicon carbide (SiC). SiC and GaN are both expected to be used for applications with high operating frequencies and medium powers, as illustrated in Figure 1.5.

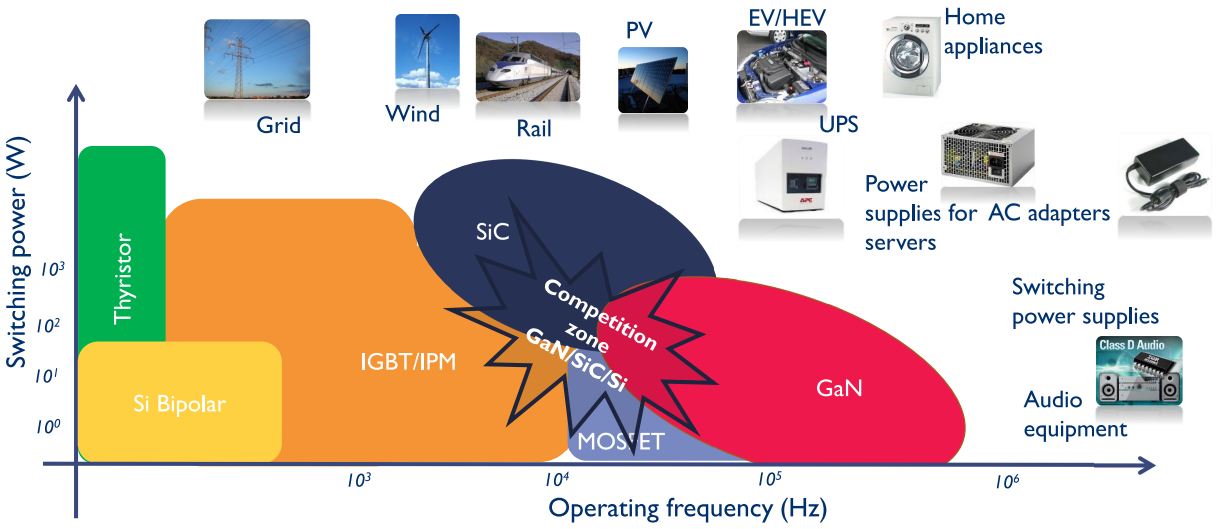

Figure 1.5. Positioning of GaN-based device technologies in the power device market (2018). IPM means Intelligent Power Module here [4].

Regarding high voltage applications, GaN is mainly positioned in the sub-900V market around 650V and 230V, which represents 68% of the global power device market (Figure 1.2). The GaN market is growing quickly with many companies that are investing in GaN-based technologies, as shown in Figure 1.6.

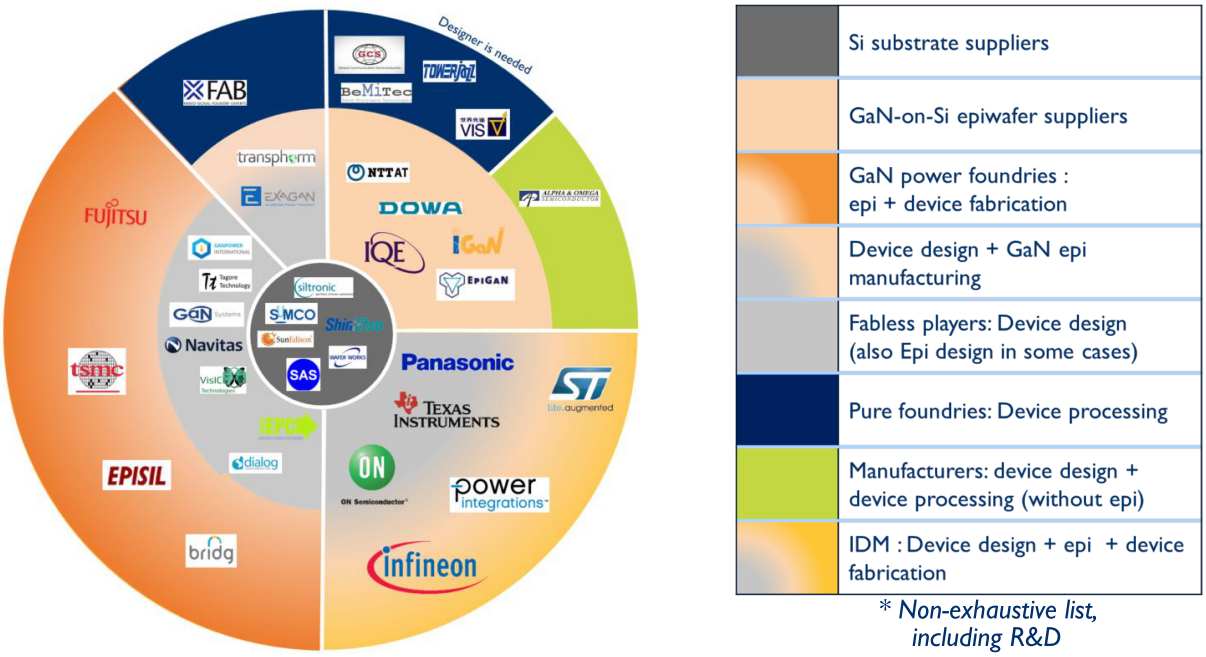

Figure 1.6. Companies involved in GaN-based devices development [7].

As reported in Figure 1.7, the projected market for GaN devices is estimated to be worth around 650 million dollars in 2025 [8].

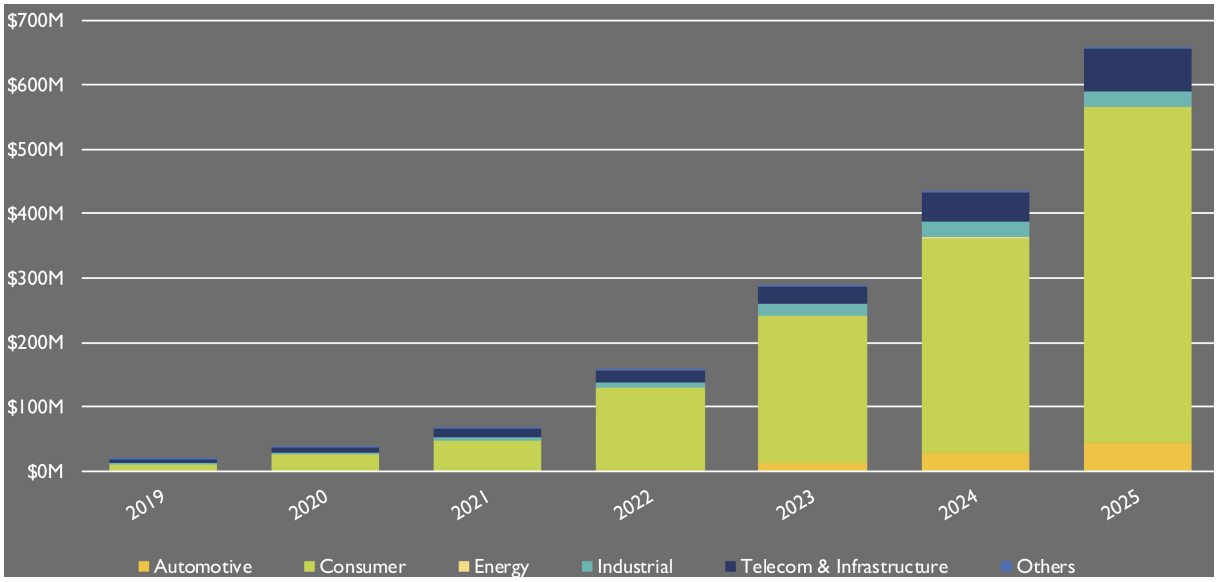

Figure 1.7. Annual forecast of power GaN device market evolution from 2019 to 2025 [8].

In the following section, the properties of gallium nitride will be described in details. The different power devices developed with this material as well as the reliability concerns encountered in these technologies will then be presented.

1.2 AlGaN/GaN hetero-structure

1.2.1 Crystalline properties of AlGaN and GaN materials

1.2.1.1 Lattice parameters

As a member of the III-nitrides (III-N) semiconductors family, GaN is a material that can be found in three different crystalline structures. Among them, there is the face-centered cubic structure that can be only formed at high pressures, and which has been widely investigated in fundamental research in material physics [9], [10]. GaN can be also found in the cubic zinc blende structure where the six face-centers and eight corners are Ga atoms while N atoms are in the $1/4$ place, with a lattice constant of 4.5Å [11]–[13]. Finally, GaN can take the hexagonal wurtzite structure which is the most commonly used in industry due to its thermodynamically stable form [11], [13]–[15]. Indeed, the ionic property of the Ga-N bond gives rise to a great stability of the structure implied by the strong electronegativity of the nitrogen (N) [16], [17]. In this manuscript, we refer to this last structure, the most widespread for the production of GaN-based devices dedicated to energy conversion, radio-frequency, or display applications. As illustrated in Figure 1.8, the ideal wurtzite crystal structure is composed of a succession of hexagonal sub-lattice layers, where one is occupied by a gallium element and the other one by nitrogen.

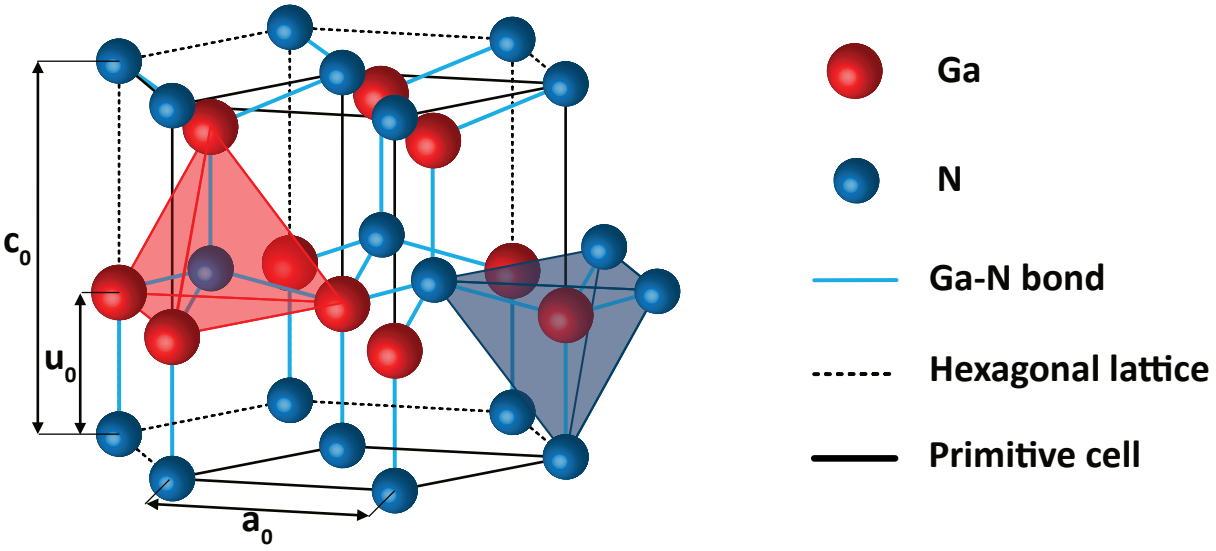

Figure 1.8. Representation of the ideal wurtzite crystal structure which is composed of a succession of hexagonal sub-lattice layers, where one is occupied by a Ga element and the other one by N. This crystalline configuration is defined by the lattice parameters a_0, c_0 and u_0, and gives rise to regular tetrahedrons where each atom is linked to four neighboring atoms.

The distance between each Ga and N sub-lattice layer along the axis $[0001]$ corresponds to $5/8$ of the elementary lattice. Due to its hexagonal form, an ideal wurtzite structure is defined by three parameters a_0, c_0 and u_0. The first one (a_0) corresponds to the length of the wurtzite hexagonal base , c_0 to the height of the unit cell corresponding to the distance between two atoms having the same nature, and u_0 to the distance of Ga-N bond . The relationship between these three parameters is described in the following expressions,

$$\frac{c_0}{a_0} = \sqrt{\frac{8}{3}} = 1.663 \tag{1.1}$$

$$u_0 = \frac{3}{8} = 0.375 \tag{1.2}$$

These latter expressions result in regular tetrahedrons where each atom is linked to four neighboring atoms. Three of these four atoms are in the same crystallographic plane perpendicular to the c-axis as shown in Figure 1.8 [16]. We will see in the section 1.2.2.1 that these tetrahedrons give rise to a spontaneous polarization of the GaN material.

Ga sites of the GaN lattice can be replaced by other metals such as aluminum (Al) or indium (In), resulting in two other well-known III-N materials which are indium nitride (InN) and aluminum nitride (AlN). A part of Ga sites can be also replaced by Al or In, giving ternary alloys as InGaN or AlGaN. Lattice constants (a_0, c_0 and u_0) of these alloys can be estimated using Vegard's law which is an empirical relation based on the mole fraction between two constituents, at a fixed temperature T [11], [15], [18], [19]. In the case of GaN-based ternary alloys, Vegard's law is described by the following expression,

$$y_0(z_\chi Ga_{1-\chi}N) = \chi \cdot y_0(zN) + (1-\chi) \cdot y_0(GaN) \tag{1.3}$$

Where, χ is the mole fraction,
y_0 is the lattice parameter (a_0 or c_0) of the concerned crystal,
and z is the metal (Al or In)

Note that this latter expression is also valid when Ga is replaced by another element, such as In or Al in order to obtain the lattice parameters of InAlN for example [17], [20]–[22]. The values of lattice parameters a_0, c_0 and u_0 of the three principal III-N materials (GaN, AlN, InN) are reported in Table 1.1. It can be noticed that GaN parameters $(c_0/a_0)_{GaN} = 1.626$ and $u_0 = 0.376$ are close to the ideal situation ($c_0/a_0 = 1.663$ and $u_{GaN} = 0.375$), whereas AlN shows more significant deviations with $(c_0/a_0)_{AlN} = 1.601$ and $u_{AlN} = 0.380$. This mismatch is correlated with the difference between the electronegativities of both atoms, and then to the polarization value within the material (cf. section 1.2.2.1) [23], [24].

	GaN	**AlN**	**InN**
a_0 [Å]	3.189	3.112	3.545
c_0 [Å]	5.185	4.982	5.703
u_0 [Å]	0.376	0.380	0.377

Table 1.1. Values of lattice parameters a_0, c_0 and u_0 of the most famous III-N materials: GaN, AlN, InN [25], [26].

1.2.1.2 Band structure

The knowledge of a band structure parameters is essential in the frame of any device development. It is an energy band representation of the density of electronic states in a material. In

the case of a semiconductor, one of the main important parameter in this representation is the energy value between valence band maximum (E_V) and the conduction band minimum (E_C) , which is also called "gap energy" E_Γ . It represents the energy required for an electron to pass from the valence band to the conduction band, around the center of the Brillouin zone Γ (Figure 1.9-left) [27]. The gap is direct in the case of GaN material, meaning that both E_C and E_V and are located at Γ. Figure 1.9-right shows a schematic representation of GaN band structure around Γ. It can be noticed that the valence band is degenerated in three different levels due to the influence of both anisotropic crystal field and spin–orbit interactions. The energy caused by the crystal field and is labeled as CH (Crystal-field split-off Hole), while HH (Heavy-Hole) and LH (Light-Hole) bands are implied by the spin–orbit interactions [11], [28]–[30]. At room temperature, GaN has a gap energy of $E_\Gamma = 3.4$ eV. The energy level separation at the symmetry point A (E_A) is between 4.7 and 5.5eV, while it is between 4.5 and 5.3eV at the points M and L ($E_{M,L}$) [11], [31], [32].

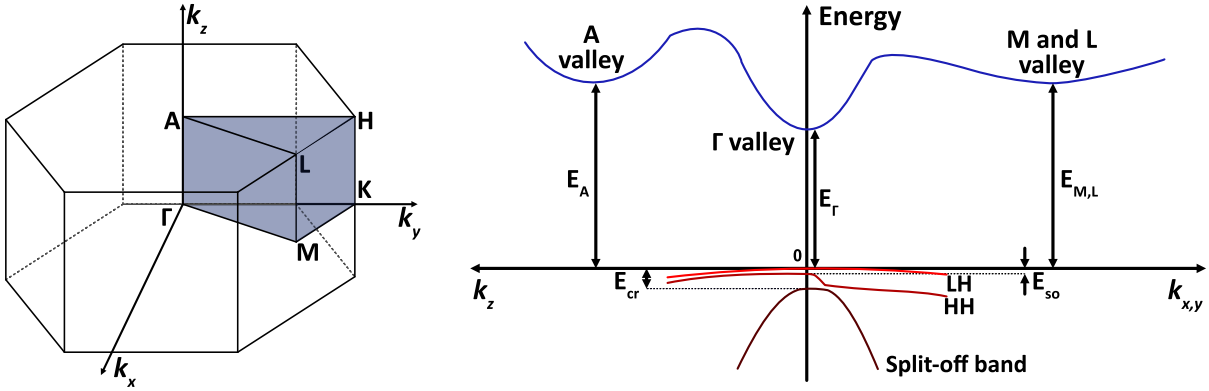

Figure 1.9. Left - Illustration of Brillouin zone of the Wurtzite hexagonal structure centered on Γ. **Right -** Schematic representation of GaN band structure around Γ where it can be noticed that the valence band is degenerated in three different levels due to the influence of both anisotropic crystal field and spin–orbit interactions [11].

The direct band gap energy of III-N material varies from 0.77eV for InN to 6.28eV for AlN at 300K [33]. It gives the possibility to form alloys enabling to modulate the band gap by adjusting the composition of the alloy. The gap energy determination of ternary alloys is commonly given by the following expression [19], [34]–[36].

$$E_\Gamma^{A_\chi B_{1-\chi} N} = \chi \cdot E_\Gamma^{AN} + (1-\chi) \cdot E_\Gamma^{BN} - b_w^{ABN} \cdot \chi \cdot (1-\chi) \tag{1.4}$$

Where, χ is the mole fraction,
A and B are two materials belonging to the III columns of Mendeleev table,
and b_w is the "bowing" non-linearity term which represents the deviation from the linear law and which is experimentally extracted. For InGaN, InAlN and AlGaN, the bowing parameter is estimated to 1.32eV [37], 5.36eV [38] and 1.0eV [22], [35], respectively.

The latter expression (1.4) is illustrated in Figure 1.10 where the gap energy is plotted as a function of lattice parameter a_0 for InGaN, InAlN and AlGaN. As showed previously in equation 1.3, the lattice parameters of III-N alloys directly depend on the mole fraction χ. This Figure also depicts that the gap energy of III-N alloys allows to cover a wide range of the electromagnetic spectrum, with wavelengths λ_w ranging from infrared (2μm) to deep Ultra-Violet

(200nm), which is very interesting for optoelectronic applications. However, some compositions remains limited due to the crystalline stress management [17], [39].

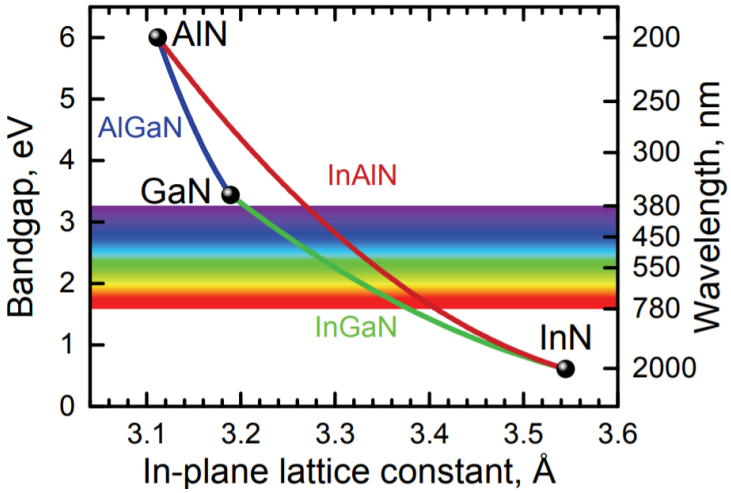

Figure 1.10. Band gap energy in left y axis, as a function of the lattice parameter a_0 of InGaN, InAlN and AlGaN alloys. The right y-axis shows the wide range of the electromagnetic spectrum, with wavelengths λ_w ranging from infrared (2µm) to deep UV (200nm) [39].

Temperature can also influence the GaN gap energy value [40]. Indeed, due to the temperature-dependent lattice expansion and electron-lattice interaction [41], [42], the band gap energy gap decreases slightly when the temperature increases. This has been experimentally evaluated by luminescence experiments [43] and absorption [44] in GaN and AlN materials. The gap energy behavior with temperature can be easily modeled by the empirical Varshni law which is given by the following expression [36]:

$$E_\Gamma(T) = E_\Gamma(T = 0K) - \frac{\alpha_V \cdot T^2}{\beta_D + T} \tag{1.5}$$

Where, T is the temperature,
α_V is the Varshni coefficient ,
and β_D is the Debye coefficient .

These latter parameters are given for GaN and AlN in Table 1.2.

	GaN	**AlN**
$E_\Gamma(T = 0K)$ [eV]	3.507	6.23
α_V [meV.K^{-1}]	0.909	1.999
β_D [K]	830	1429

Table 1.2. Values of gap energy at T = 0 K, Varshni α_V and Debye β_D coefficients for GaN and AlN [25].

1.2.2 Polarizations in GaN materials

1.2.2.1 Spontaneous polarization

Wurtzite crystalline form of gallium nitride has also the property to have an intrinsic polarization. Indeed, N is known to have a very strong electronegativity, meaning that N tends to attract the electrons within the Ga-N bonds leading to a barycenter displacement of electrical charges towards N sites. This effect causes a spontaneous polarization $\overrightarrow{P}$ resulting from the sum of the polarization vectors related to each Ga-N bonds within a single tetrahedron constituting the hexagonal lattice (Figure 1.8) such as,

$$\overrightarrow{P} = \sum_{i=1}^{N=4} \overrightarrow{P_i} \tag{1.6}$$

Consequently, a tetrahedron in the wurtzite crystal can be considered as a dipole with a polarization vector which is oriented along the c_0 direction, as shown in Figure 1.11-left. From a global point of view, the finite aspect of the GaN crystal automatically implies the presence of hetero-surfaces which act as electrical charge planes perpendicular to the [0001] direction. These latter induce a spontaneous polarization $\overrightarrow{P_{sp}}$ in the [0001] direction, and then an electric field $\overrightarrow{E_{sp}}$ within the crystal, as shown in Figure 1.11-right [14], [20], [24], [45].

GaN material have a spontaneous polarization $||\overrightarrow{P_{sp}}|| = 0.029\ \mathrm{C}\cdot\mathrm{m}^{-2}$, however the direction of this latter depends on the two distinct polarities that GaN can have, and which are called Ga-Face and N-Face. The crystal will be Ga-face if a gallium atom occupies the top layer position in the [0001] axis for each bi-layer, or N-face if the nitrogen atom occupies this position. The polarity is reversed between these two cases, pointing to [000-1] direction in Ga-face configuration and to [0001] direction in N-face configuration. The N polarity means that the base of tetrahedron is on the bottom, and the associated polarization is oriented along the [000-1] direction, as shown in Figure 1.11. Conversely, Ga polarity means that the base on the tetrahedron is on the top and the related polarization is oriented along the [0001] direction. Therefore, these crystal orientation considerations are of great importance as they determine the orientation of the polarization within the crystal. In the rest of this manuscript, the Ga-Face polarity will be always considered [14], [20], [24], [45].

The value of the spontaneous polarization of ternary alloys cannot be extrapolated through a linear law. Non-linear laws integrating a "bowing" parameter to the expression of the spontaneous polarization have been presented in [20]. This term represents the deformation contribution and the effects of the internal stress within the alloy. It depends on the lattice parameter u_0 in the c_0 direction [24]. The spontaneous polarization can thus be written from the known values for GaN, AlN and InN by the following empirical relations (which is also illustrated in Figure 1.12),

$$\overrightarrow{P_{sp}^{ABN}}(\chi) = \overrightarrow{P_{sp}^{AN}}\cdot\chi + \overrightarrow{P_{sp}^{ABN}}\cdot(1-\chi) + b_w\cdot(1-\chi)\cdot\chi \tag{1.7}$$

Where, χ is mole fraction ,
A and B are two materials belonging to the III columns of Mendeleev table,
and b_w is the "bowing" non-linearity term.

From the latter equation, the spontaneous polarization as a function the stoichiometry χ in AlGaN is described by the equation (1.8) [14], [20] and is illustrated in Figure 1.12,

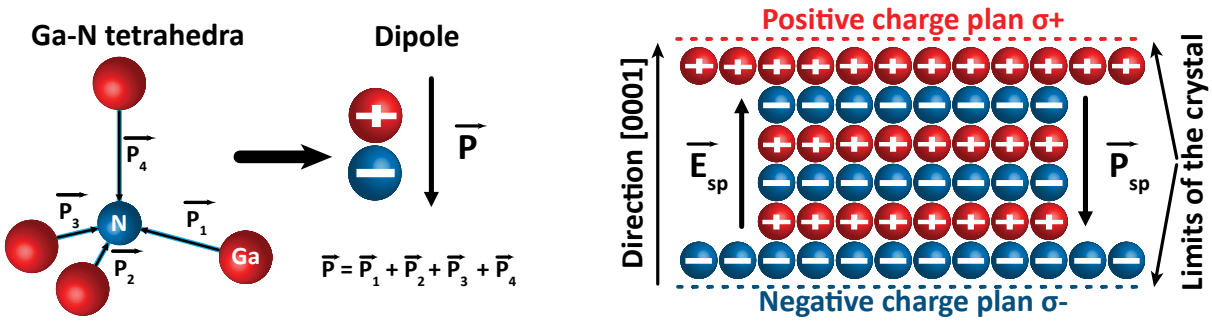

Figure 1.11. Left - Representation of the different polarizations within a single tetrahedron constituting the hexagonal Wurtzite lattice shown in Figure 1.8, and resulting into a global polarization within the tetrahedron $\overrightarrow{P}$. **Right -** Role of the dipole in the wurtzite crystal, where the finite aspect of the crystal automatically implies the presence of hetero-surfaces, inducing a spontaneous polarization $\overrightarrow{P_{sp}}$ in the direction [0001] within the crystal.

$$||\overrightarrow{P_{sp}^{AlGaN}}(\chi)|| = -0.090\cdot\chi - 0.034\cdot(1-\chi) + 0.0021\cdot\chi\cdot(1-\chi) \ [\mathrm{C\cdot m^{-2}}] \tag{1.8}$$

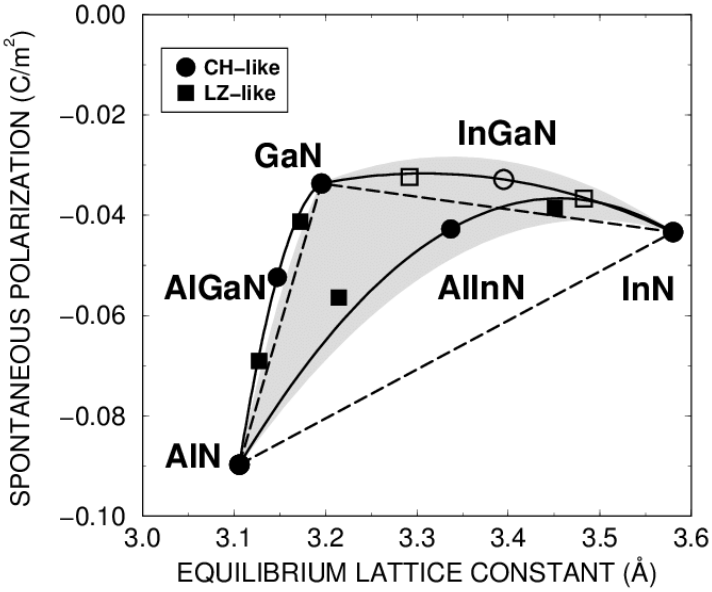

Figure 1.12. Spontaneous polarization as a function of lattice constant a_0 for AlGaN, InGaN and AlInN ternary alloys [46].

1.2.2.2 Piezoelectric polarization

When a strain is applied on GaN, a piezoelectric polarization $\overrightarrow{P_{pz}}$ within the crystal appears leading to an internal electric field $\overrightarrow{E_{pz}}$. Depending on the type of stress, compression or tension, this piezoelectric polarization will be added or subtracted from the spontaneous polarization $\overrightarrow{P_{sp}}$ already present. Indeed, the stress modifies the lattice constant and thus the c_0/a_0 ratio. $\overrightarrow{P_{pz}}$

can be defined in the Cartesian system as a function of the strain field parameters ϵ_j and the piezoelectric constants e_{ij} such as,

$$\overrightarrow{P_{pz}} = \sum_{i,j} e_{ij} \cdot \overrightarrow{\epsilon_j} \tag{1.9}$$

By considering the crystal symmetry, this latter equation 1.9 can be simplified such as,

$$||\overrightarrow{P_{pz}}|| = e_{33} \cdot \epsilon_3 - 2 \cdot \epsilon_1 \cdot e_{13} \tag{1.10}$$

Where e_{33} and e_{13} are piezoelectric constants,
and $\epsilon_3 = {}^{c_x - c_0}/_{c_0}$ and $\epsilon_1 = {}^{a_x - a_0}/_{a_0}$ which are both the deformations along vertical and transversal directions, respectively.

The lattice parameters without constraint are defined by a_0 and c_0, and by a_x and c_x with constraint. By taking into account the relationship between ϵ_3 and ϵ_1 that depend on C_{13} and C_{33}, which are GaN elastic constants, such as $\epsilon_3 = {}^{C_{13}}/_{C_{33}} \cdot \epsilon_1$, the piezoelectric polarization can be expressed via the following relation.

$$||\overrightarrow{P_{pz}}|| = 2 \cdot \frac{a_x - a_0}{a_0} \cdot (e_{31} - \frac{e_{33} \cdot C_{13}}{C_{33}}) \tag{1.11}$$

Since the term $e_{31} - {}^{e_{33} \cdot C_{13}}/_{C_{33}}$ is always negative, the direction of the piezoelectric polarization depends on the sign of $a_x - a_0$. This means that if $a_x - a_0 > 0$, the lattice will be in tensile strain leading to a negative direction of the piezoelectric polarization along [0001] direction. Conversely, if $a_x - a_0 < 0$, the lattice will be compressively strained, implying a positive direction of $\overrightarrow{P_{pz}}$ along [0001] direction. Consequently, for a same crystalline polarization (Ga-Face or N-Face), the piezoelectric polarization can be added or subtracted to the spontaneous polarization $\overrightarrow{P_{ps}}$, depending on the strain within the crystal (Figure 1.13).

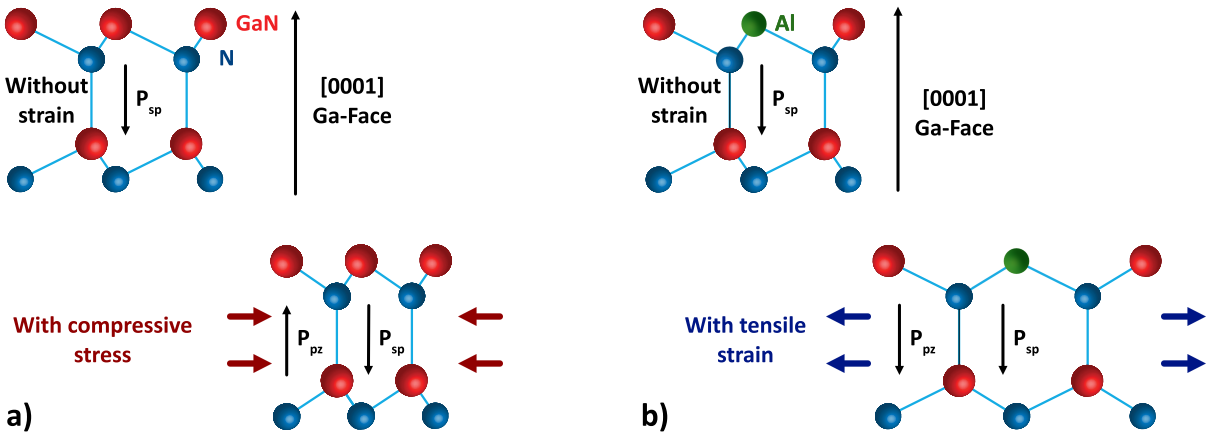

Figure 1.13. Influence of compressive stress for GaN (**a**) and tensile stress for AlGaN (**b**) as well as the associated directions of the polarization vectors $\overrightarrow{P_{pz}}$ and $\overrightarrow{P_{sp}}$ [47].

In the case of a Ga-Face polarity, a compressive strain within the GaN crystal leads to a spontaneous and piezoelectric polarization which have opposite directions (Figure 1.13-a). In contrast, when the lattice is submitted to a tensile strain, both spontaneous and piezoelectric polarizations will have the same directions as can be shown for AlGaN in Figure 1.13-b. The resulting polarization from the superposition of $\overrightarrow{P_{ps}}$ and $\overrightarrow{P_{pz}}$ will give rise to polarization charges at the interface

between GaN and AlGaN. It is this phenomenon that enables the creation of a two-dimensional gas of electrons (2DEG) at the AlGaN/GaN interface. The following equation gives the $\overrightarrow{P_{pz}}$ value in an AlGaN layer deposited on a relaxed binary layer (GaN) as a function of the molar fraction χ [14], [20], [24], [45],

$$||\overrightarrow{P_{pz}^{AlGaN}}(\chi)|| = -0.0525 \cdot \chi - 0.0282 \cdot (1-\chi) \cdot \chi \, [\mathrm{C \cdot m^{-2}}] \tag{1.12}$$

1.2.3 AlGaN/GaN hetero-structure properties

1.2.3.1 2D-Electron Gas formation in AlGaN/GaN hetero-structure

AlGaN/GaN hetero-structure gives rise to a bi-dimensional gas of electrons (2DEG) at the hetero-junction interface. By ensuring that the polarization vectors $\overrightarrow{P_{sp}}$ and $\overrightarrow{P_{pz}}$ have the same direction in AlGaN layer as shown in Figure 1.14-left, the effective surface charge related to the polarization will be the highest such as,

$$\overrightarrow{P^{AlGaN}}(\chi) = \overrightarrow{P_{sp}^{AlGaN}}(\chi) + \overrightarrow{P_{pz}^{AlGaN}}(\chi) \tag{1.13}$$

By the application of Maxwell's law giving the polarization charge σ_P via the gradient of the polarization $\overrightarrow{P}$ ($\sigma_P = \nabla \overrightarrow{P}$), the following relation is obtained,

$$\Rightarrow \sigma_{\mathrm{AlGaN}}(\chi) = \sigma_{\mathrm{sp}}^{\mathrm{AlGaN}}(\chi) + \sigma_{\mathrm{pz}}^{\mathrm{AlGaN}}(\chi) \tag{1.14}$$

with $\sigma_{\mathrm{sp}}^{\mathrm{AlGaN}}$ and $\sigma_{\mathrm{pz}}^{\mathrm{AlGaN}}$, the absolute value of effective surface charge which induces by the spontaneous and piezoelectric polarization respectively,
and σ_{AlGaN}, the absolute value of total surface charge in AlGaN. By doing the same operation for the GaN layer and considering $\overrightarrow{P_{pz}^{GaN}}$ as negligible, the GaN charge polarization σ_{GaN} is equal to $\sigma_{\mathrm{sp}}^{\mathrm{GaN}}$.

Since the effective surface charges do not have the same values in both materials due to a negligible piezoelectric polarization in GaN compared to AlGaN, this leads to the apparition of a net positive charge plane σ_{fixed} at the interface of AlGaN/GaN hetero-structure such as,

$$\sigma_{\mathrm{fixed}}(\chi) = \sigma_{\mathrm{AlGaN}}(\chi) - \sigma_{\mathrm{GaN}} \tag{1.15}$$

Considering that $\sigma_{\mathrm{AlGaN}} > \sigma_{\mathrm{GaN}}$, the positive charge plane is compensated by the presence of a 2D electron gas (2DEG) localized at the hetero-structure interface at thermodynamic equilibrium, and more precisely in the GaN side due to the lower E_C energy level as shown in Figure 1.14-right. Note that the charge density within the 2DEG depends on the molar fraction χ in AlGaN, due to the strong influence of this parameter on $\overrightarrow{P_{pz}^{AlGaN}}$ and then on $\sigma_{\mathrm{fixed}}(\chi)$ [20], [45].

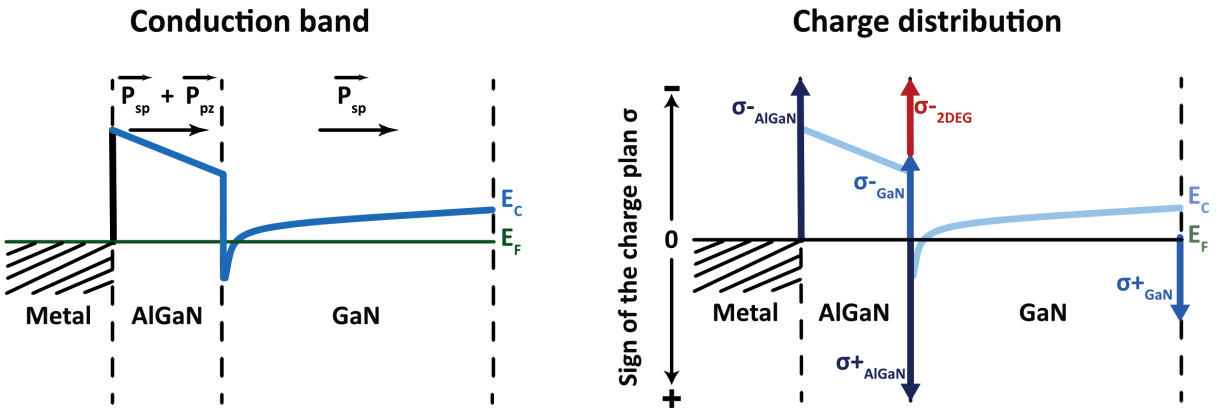

Figure 1.14. Left - Illustration of the polarization direction. **Right -** Charge distribution representation of AlGaN/GaN conduction band structure at thermodynamic equilibrium [48].

1.2.3.2 2D-Electron Gas properties in AlGaN/GaN

The 2DEG has the properties to be very conductive due to its high charge density n_s which is around $10^{13}cm^{-2}$. It can be estimated at $10^{19}cm^{-3}$ by considering a 2DEG thickness t_{2DEG} of 10nm [14], [20], [45]. The surface charge density n_s can be calculated using the following equation,

$$n_s(\chi) = \frac{\sigma_{fixed}(\chi)}{e} - \frac{\epsilon_{00}\cdot\epsilon_r}{t_{AlGaN}}\cdot(e\cdot\Phi_b + E_F(\chi) - \Delta E_C(\chi)) \tag{1.16}$$

Where e is the constant electron charge ($-1.609\cdot10^{-19}C$),
t_{AlGaN} is the AlGaN thickness,
χ is the mole fraction,
Φ_b is the energy barrier at the metal/AlGaN interface,
$E_F(\chi)$ the Fermi level from the GaN conduction band,
$\Delta E_C(\chi)$ the conduction band offset at the AlGaN/GaN interface,
and ϵ_{00} and ϵ_r the dielectric permittivity of classical vacuum ($8.854\cdot10^{-12}F\cdot m^{-1}$) and in AlGaN respectively.

In this latter equation 1.16, it can be noticed that one of the main parameter that influences n_s is the Al concentration. According to Ambacher *et al.* [14], [20], [45], it is mainly determined by $\sigma_{fixed}(\chi)/e$ which is strongly dependent on χ. Indeed, as previously mentioned, $\sigma_{fixed}(\chi)$ is directly influenced by the piezoelectric polarization in AlGaN (via $\sigma_{pz}^{AlGaN}(\chi)$ in equation 1.14) which depends on χ according equation 1.12. For an AlGaN barrier thickness of 20nm that is not relaxed, Ambacher's calculations indicate a charge concentration of $1\cdot10^{13}cm^{-2}$ and $1.6\cdot10^{13}cm^{-2}$ for an Al concentration of $\chi = 0.2$ and 0.3 respectively, which is consistent with the typical values obtained experimentally in our devices [14]. Figure 1.15 illustrates the equation 1.16 by showing the electron density as a function of alloy concentration for various AlGaN barrier thicknesses.
Due to the absence of doping atoms to create the 2DEG (or eventually a significant distance of the doping atoms from which the 2DEG electrons are derived [51]–[53]) combined with the charge confinement in the potential at AlGaN/GaN interface, the 2DEG has the property to reach a high electron mobility μ_n which is between 1000 and $2000cm^2\cdot V^{-1}\cdot s^{-1}$ at 300K [54]–[56], as depicted in Figure 1.16.

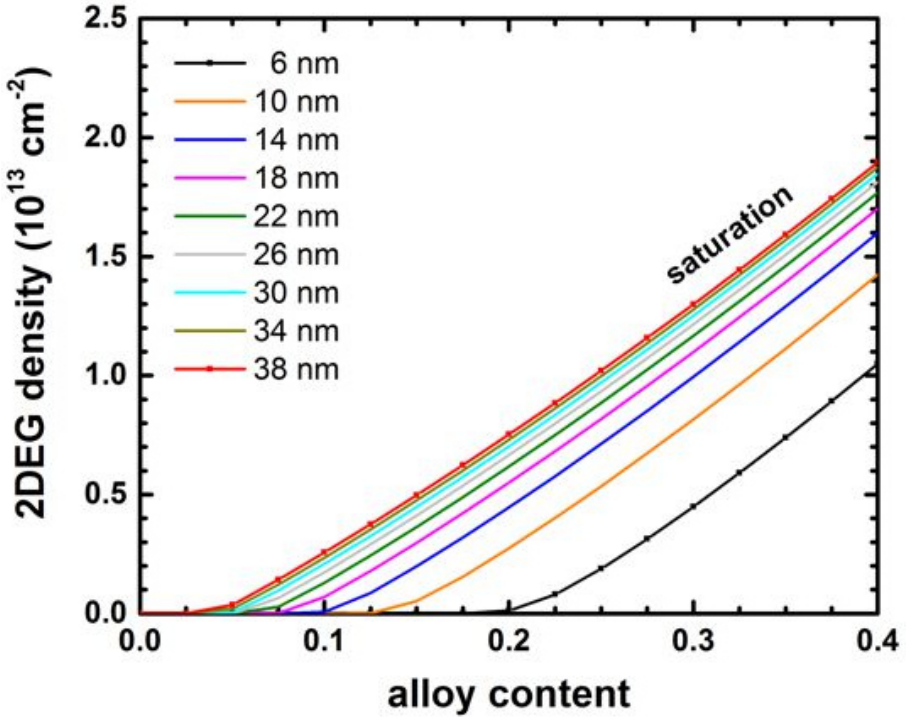

Figure 1.15. Electron density within the 2DEG as a function of alloy concentration for various AlGaN thicknesses [49], [50].

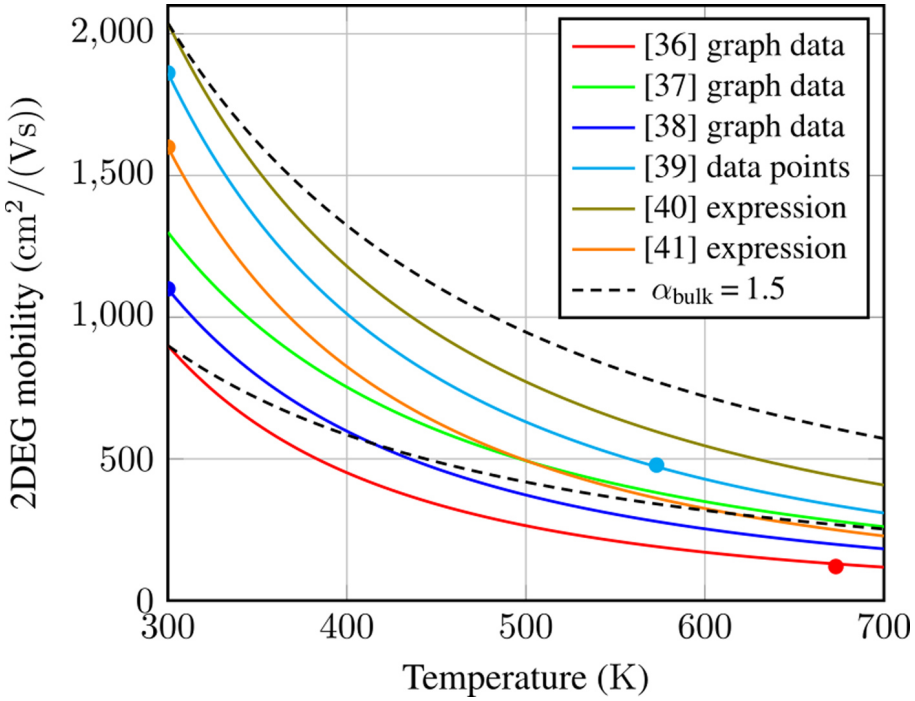

Figure 1.16. Mobility of 2DEG as a function of temperature T from 300 to 700K [54].

By combining the volume charge density n_v with the electron mobility μ_n, the resistivity ρ (conventionally expressed in $[\Omega \cdot cm]$) can be easily obtained using the following equation,

$$\rho = \frac{1}{e \cdot n_v \cdot \mu_n} \tag{1.17}$$

In the frame of AlGaN/GaN HEMT, the notion of "sheet resistance" is usually used, and refers to the resistance R_s of a material which has a rectangular form with a fixed thickness t_s , such as $R_s = \rho \cdot t_s$. This latter parameter is usually extracted by applying the well-known van der Pauw method [57], and it is commonly expressed in $[\Omega/\square]$. It enables us to get a value of R_s which is independent of the geometry of the sample (considering that $t_s = t_{2DEG}$), and thus presents the advantage of being comparable to other values of R_s. In our laboratory, the typical value of the 2DEG sheet resistance is obtained around $380\Omega/\square$ for an Al proportion χ of 0.22.

Another property of the 2DEG is its high saturation velocity corresponding to the maximum velocity that the carriers can reach. When a low electric field $\overrightarrow{E}$ is applied on any conductive semiconductor, the drift velocity of the charges v_d is linearly dependent on $\overrightarrow{E}$, such as $v_d = \mu_n \cdot \overrightarrow{E}$ where μ_n is the electron mobility . However, this linear regime is valid for a certain range of electric field. Indeed, at high electric field, a saturation of the charge velocity can be observed, which is also called saturation of velocity v_{sat} . As mentioned previously, the electron saturation velocity in GaN is relatively high, reaching theoretical values from $2.1 \cdot 10^5 m \cdot s^{-1}$ to $3.3 \cdot 10^5 m \cdot s^{-1}$ at 300K. However, it is important to note that these values can vary with the residual donor doping in GaN as well as with the temperature [58]. As well as the charge density and the mobility, the saturation velocity is a key parameter in power applications, since it strongly contributes to the maximum current that can be obtained in a power device. It is also a very important parameter in radio-frequency applications because it also determines the cutoff frequency f_c, as depicted in the following expression giving the relationship between v_d and f_c (L_G is the gate length of the transistor),

$$f_c = \frac{v_{sat}}{2 \cdot \pi \cdot L_G} \tag{1.18}$$

The cutoff frequency is a limit where the energy flowing through the transistor begins to be attenuated or reflected. It needs to be increased in order to enable high frequency applications. Recently, a maximum value of 400GHz has been obtained with a gate length of 20nm [59].

1.2.3.3 GaN advantages for power applications

1.2.3.3.1 Figures of merit

In power electronics, the device development is globally driven by four parameters which are the nominal current I_{n0} , the On-resistance R_{On} , the breakdown voltage B_V and the switch capacitance C_{SW} . I_{n0} and B_V have to be the highest as possible to maximize the output power and sustain high voltage, while C_{SW} and R_{On} have to be the lowest as possible in order to minimize the energy dissipation. The optimization and determination of these parameters are necessarily based on the semiconductor properties used to develop the device. Since semiconductors and more generally all materials have different properties, it is not easy to do a fair comparison between them. To do so, a figure of merit is generally used. Indeed, it enables quantifying the important electrical properties of the material in the context of a specific device application, through a numerical expression. In the literature, Johnson's figure of merit and Balliga's figure

of merit are generally used for power semiconductors, and will be presented in the following sub-sections.

Baliga's figure of merit

Baliga's figure of merit is one of the most appropriate for power device applications. As mentioned previously, the On-resistance R_{On} should be the lowest as possible in order to limit the power dissipation, and the breakdown voltage B_V has to be the highest as possible. Baliga's figure of merit combine these parameters by giving the power density that a given semiconductor can theoretically withstand [6], [60]. The following expression enables to calculate this figure of merit BFoM in $[W \cdot m^{-2}]$,

$$BFoM = \epsilon_{00} \cdot \epsilon_r \cdot \mu_{n,p} \cdot E_{crit}^3 \tag{1.19}$$

Where $\mu_{n,p}$ is the electron or hole mobility,
and E_{crit} is the maximum electric field at the onset of avalanche breakdown, which also called critical electric field. Note that for a given material, the higher the BFoM the lower the resistance and therefore the lower the energy losses for a given technology. BFoM usually appears in the relation between the On-resistance R_{On} and the breakdown voltage square B_V^2 such as,

$$R_{On} = \frac{4 \cdot B_V^2}{\epsilon_{00} \cdot \epsilon_r \cdot \mu_{n,p} \cdot E_{crit}^3} = \frac{4 \cdot B_V^2}{BFoM} \tag{1.20}$$

This latter relation is illustrated in Figure 1.17, where the BFoM is plotted for different semiconductors. It can be noticed that other materials such has Ga_2O_3, diamond, AlN, or C-BN (Cubic-Boron Nitride) have a better figure of Baliga compared to gallium nitride. However, the p-doping in these ultra-wide band gap semiconductors is not controlled. In the case of diamond, one of the main issue is the absence of shallow acceptor and donor species, as well as the lack for now of consistent physical models specific to diamond-based devices [61], [62].

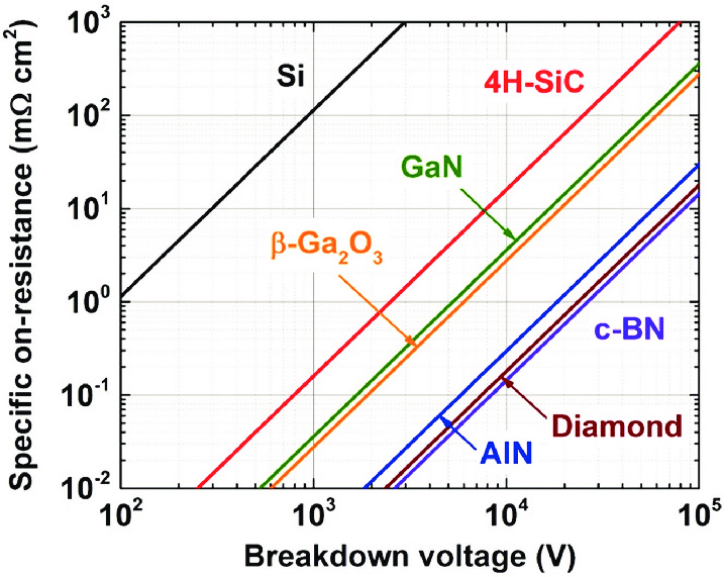

Figure 1.17. Baliga figure-of-merit (BFOM) for various semiconductors, where On-resistance versus breakdown voltage is plotted in log-log scale. The lower right region represents higher BFOM, and hence the higher performance [61].

Johnson's figure of merit

Johnson's figure of merit is one of the most appropriate for radio-frequency (RF) power transistors. With applications in sensing and communications, and wavelength range from the microwave to millimeter, RF power transistors are necessary in electronic systems. In general, good efficiency combined with high output power is expected from these transistors. The high output power enables to improve the signal/noise ratio. Transistor efficiency is often defined as the ratio between the output radiated power and the input electrical power. Non-radiated power is lost through Joule heating and contributes to the system overheating. Therefore, the main challenges in high frequency applications are to simultaneously minimize the carrier transit time (to increase f_c), maximize the electron density (to increase the output power) and reduce the access resistances (to increase the efficiency). The basic trade-off therefore mainly depends on the breakdown voltage B_V and the cutoff frequency f_c. These parameters are taken into account in the Johnson figure of merit JFoM [63] such as,

$$JFoM = B_V \cdot f_c \tag{1.21}$$

In the case of a uniform electric field in the channel, the breakdown voltage can be expressed as a function of the critical electric field, such as $B_V = E_{crit} \cdot L_G$. By combining this latter expression with equation 1.18,

$$\Rightarrow JFoM = E_{crit} \cdot L_G \cdot f_c = \frac{E_{crit} \cdot v_{sat}}{2 \cdot \pi} \tag{1.22}$$

Johnson's figure of merit is illustrated in Figure 1.18, where the breakdown voltage is plotted as a function cut off frequency for different type of semiconductors. As BFoM, the higher JFoM the better the trade-off between the breakdown voltage B_V and the cutoff frequency f_c, corresponding to the upper right region in Figure 1.18 [64].

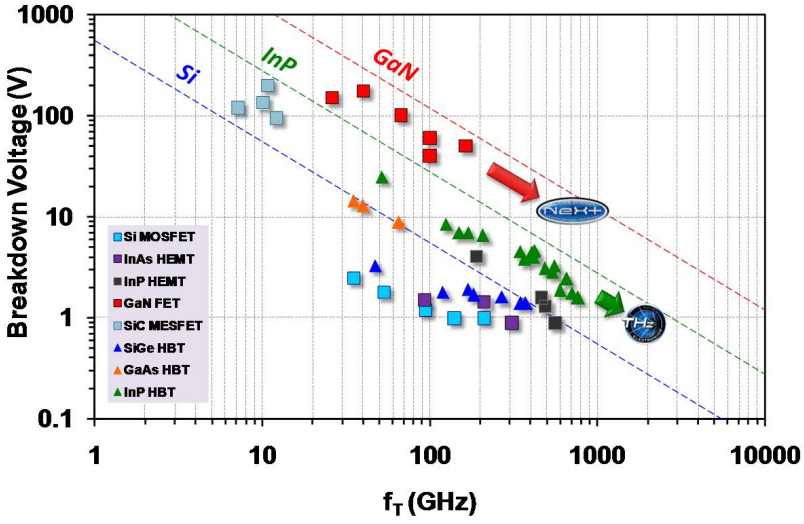

Figure 1.18. Johnson figure of merit (JFoM) for various semiconductors, where breakdown voltage as function of cutoff frequency is plotted in log-log scale. The upper-right region represents higher JFoM, and hence the higher performance [64].

1.2.3.3.2 Comparison between GaN and other semiconductor materials

As shown in figures 1.17 and 1.18, GaN depicts physical properties especially adapted to power electronics industry. The particular interest of GaN can be better understood by comparing its properties with other common semiconductors. The direct competitors to GaN are Si and SiC. To compare the physical characteristics of GaN to Si and SiC, we generally use a star diagram giving the value of five main parameters for each material which are E_Γ, B_V, v_{sat}, μ_n and thermal conductivity k_T .

Figure 1.19 shows the star diagram enabling to do comparison between GaN, Si and 4H-SiC. It can be noticed that GaN has very interesting properties compared to Si and 4H-SiC, notably for high frequency and high current applications. Indeed, the mobility in the 2DEG can reach $2000 cm^2 \cdot V^{-1} \cdot s^{-1}$ which is at least 33% higher than the mobility found in Si ($1350 cm^2 \cdot V^{-1} \cdot s^{-1}$) and 4H-SiC ($1190 cm^2 \cdot V^{-1} \cdot s^{-1}$). GaN saturation velocity ($2.5 \cdot 10^7 cm \cdot s^{-1}$) is also higher than v_d found in Si ($1 \cdot 10^7 cm \cdot s^{-1}$) and SiC ($2.0 \cdot 10^7 cm \cdot s^{-1}$). Moreover, GaN is also very interesting for high voltage applications with a critical electric field E_{crit} of $3.8 MV.cm^{-1}$ which is much higher than the E_{crit} found in Si ($0.3 MV.cm^{-1}$) and 4H-SiC ($2 MV.cm^{-1}$). A high gap energy is also very important for high voltage applications, because it limits the unwanted impact ionization phenomena. The latter is related to an electron generation from the valence band to the conduction band under a high electric field application. As shown in Figure 1.19, the gap energy of GaN (3.44eV) is higher than the 4H-SiC (3.26eV) and Si (1.1eV). Although GaN properties are globally higher than Si and SiC, the latter is also very well positioned, especially with a thermal conductivity that is much higher than GaN, and which makes it suitable for high power and high temperature applications [65].

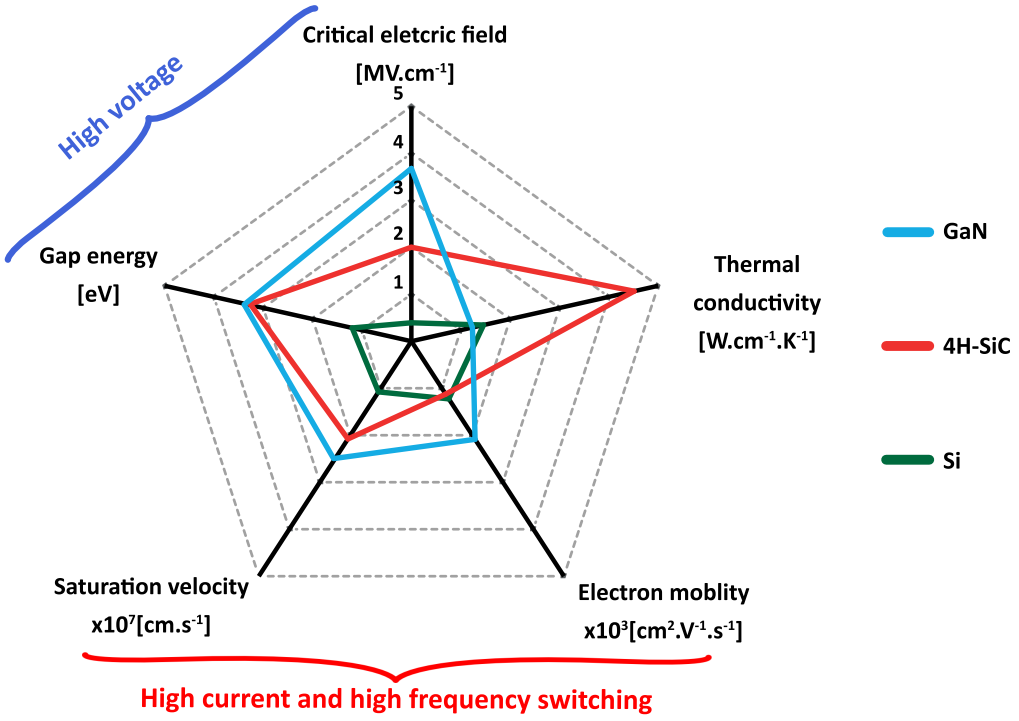

Figure 1.19. Star diagram enabling the comparison between GaN, SiC and Si properties in the frame of power electronic applications [65].

Fundamental properties of wide-bandgap semiconductors commonly used in power electronics are listed together in Table 1.3.

	Si	**GaAs**	**GaN**	**3C-SiC**	**4H-SiC**	**6H-SiC**
E_Γ [eV]	1.1	1.4	3.44	2.2	3.26	3.0
ϵ_r [–]	11.8	13.1	9.5	9.6	10	9.7
μ_n [$cm^2 \cdot V^{-1} \cdot s^{-1}$]	1350	8500 (b)	1000 (a) 2000 (b)	650	950 (a) 1190 (c)	420 (a) 84 (c)
E_{crit} [$MV \cdot cm^{-1}$]	0.3	0.4	3.8	1.2 (d)	2.0	2.4
v_{sat} [10^7 $cm \cdot s^{-1}$]	1.0	1.2	2.5	2.0	2.0	2.0
k_T [$W \cdot cm^{-1} \cdot K^{-1}$]	1.5	0.44	1.3	4.5	4.5	4.5
BFoM [$TW \cdot cm^{-2}$]	0.38	6.31	923.11	9.55	84.29	49.87
JFoM [$THz \cdot V$]	0.48	0.76	15.12	3.82	6.37	7.64

Table 1.3. Comparison between fundamental properties of several semiconductor materials commonly used in power electronics. Both figures of merit, BFoM and JFoM show a large advantage for GaN properties. (a) Mobility along a-axis. (b) Mobility in 2DEG (c) Mobility along c-axis. (d) Estimated value [66].

1.3 GaN-based devices for power applications

1.3.1 Common epitaxial structures

1.3.1.1 Substrate choice

In the power electronics industry, GaN epitaxy is mostly carried out on foreign substrates such as Si, SiC and sapphire (Al_2O_3) [67] due to the high cost and the low availability of native substrates. However, foreign substrates introduce mechanical stresses and dislocations due to the mismatch in lattice constants and thermal expansion coefficients between different materials, as shown in Table 1.4. Induced dislocations and defects can deteriorate the devices performance by acting as electron traps [68]. The material with the most advantageous properties is the SiC substrate. Indeed, the lattice mismatch with GaN is relatively low (3.1%) and the linear thermal expansion coefficients are relatively close, with $4.4 \cdot 10^{-6} K^{-1}$ and $5.6 \cdot 10^{-6} K^{-1}$ for SiC and GaN respectively. Furthermore, the high thermal conductivity of the SiC substrate allows an efficient heat dissipation which is very interesting in the frame of power devices development. Nevertheless, SiC wafers remain very expensive compared to silicon.

Although there is a higher lattice constant mismatch (-17%) and thermal expansion coefficient $2.6 \cdot 10^{-6} K^{-1}$ between Si (111) and GaN, the lower cost, the compatibility with existing fabrication processes, and the wide range of available size, make silicon a very interesting substrate for mass production of GaN devices [69]. Moreover, epitaxial engineering and strain management techniques have been developed to obtain dislocations density comparable with those found on SiC (10^8), and prevent cracks and dislocations formation. That is why the silicon wafer is chosen to develop GaN-on-Si E-mode MOSc-HEMT in CEA-LETI .

Regarding sapphire substrate, similar problems to silicon can be found due to the mechanical strain and crack formation [70], however it can be attractive for high-frequency applications due to its higher resistivity compared to Si wafers.

	Sapphire	**SiC**	**Si (111)**	**GaN**
Lattice mismatch [%]	16	3.1	-17	0
Thermal expansion $[\times 10^{-6} \cdot K^{-1}]$	7.5	4.4	2.6	5.6
Thermal conductivity $[W \cdot cm^{-1} \cdot K^{-1}]$	0.25	4.9	1.6	2.3
Dislocation density $[cm^{-2}]$	10^8	10^8	10^8	$10^4 - 10^8$
Cost	Cheap	Expensive	Cheap	Very expensive

Table 1.4. Key parameters of the main substrates used for GaN epitaxy [48], [69], [71], [72].

1.3.1.2 AlN nucleation layer

For reasons of growth rate, GaN layers are commonly deposited by MOCVD (Metal Organic Chemical Vapor Deposition) in the power device industry. As mentioned earlier, the main drawbacks of growing GaN on a silicon substrate are the difference in thermal expansion coefficients as well as the crystal lattice mismatch between both materials, which leads to dislocations and

defects. Since GaN is grown at a temperature around 1000°C, wafer bowing effects (wafer curvature) can appear [69] during growth and cooling, inducing cracking of the GaN film [73], [74]. These problems imply the necessity to use a nucleation layer between silicon and GaN. Watanabe et. al. [75] demonstrated for the first time that the growth of an AlN-based nucleation layer of $100-200$nm-thick on Si substrate, improves the final quality of the GaN film. Nowadays, this AlN-based nucleation layer around 300nm-thick is systematically integrated in epitaxial structures made on Si substrates. AlN has a smaller lattice constant compared to GaN, leading to a compression strain of GaN enabling to avoid crack formation. However, accurate growth conditions of AlN are required because it directly influences the wafer curvature as well as the GaN defects density, such as inverted pyramids defects (Figure 1.20). These latter defects are known to cause premature breakdown in power devices [76].

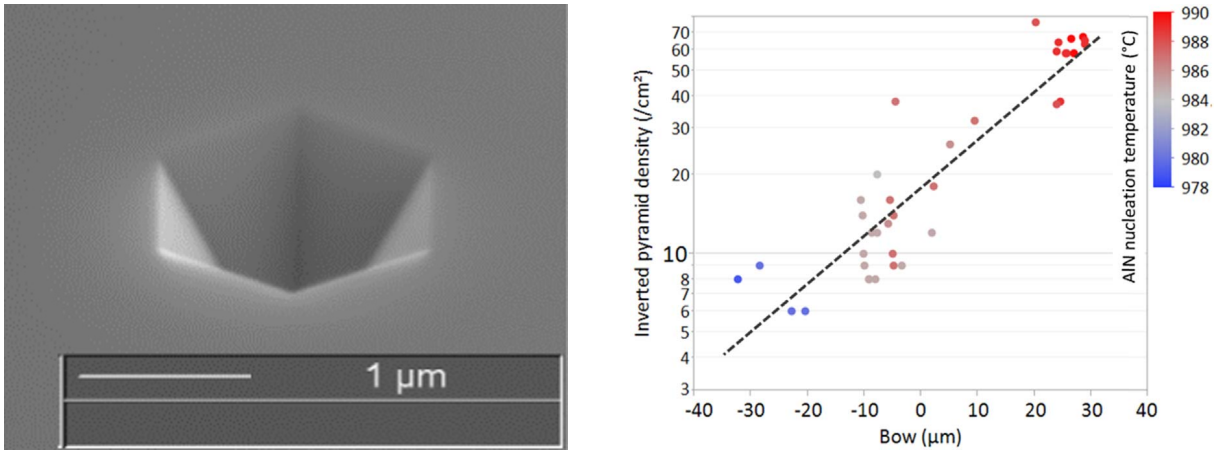

Figure 1.20. Left - Inverted pyramid defect obtained by Scanning Electron Microscope (SEM). **Right -** Average inverted pyramid density over a full wafer as a function of wafer bow for different AlN nucleation temperatures [76].

1.3.1.3 Transition layers

To reduce the wafer curvature induced by GaN deposition, the epitaxial layer stack is grown such as the final layer is under compression at the growth temperature. This compression is compensated by tensile force implied by cooling, resulting in negligible wafer curvature. Various stress management procedures have been developed to achieve this negligible wafer bow. One consists in including compositional gradation from AlN to GaN (Figure 1.21-a) [77], while the other one is based on deposition of AlN intermediate layers between thicker GaN layer [78], [79] (Figure 1.21-b). Another approach consists on the insertion of an AlN-GaN or AlGaN/GaN superlattice [80]–[82] (Figure 1.21-c), while the last one is based on several AlGaN layers where the Al concentration is reduced gradually (Figure 1.21-d) [83]. These different techniques require accurate process control to minimize the final wafer curvature. The latest in situ control systems allow the monitoring of the wafer curvature throughout the epitaxial growth process [48], [73], [84].

1.3.1.4 Unintentionally doped GaN

GaN epitaxy is carried out using a trimethylgallium (TMGa) metal precursor brought into the reactor via a neutral gas (H_2 or N_2) which reacts with ammonia NH_3 to form GaN on the

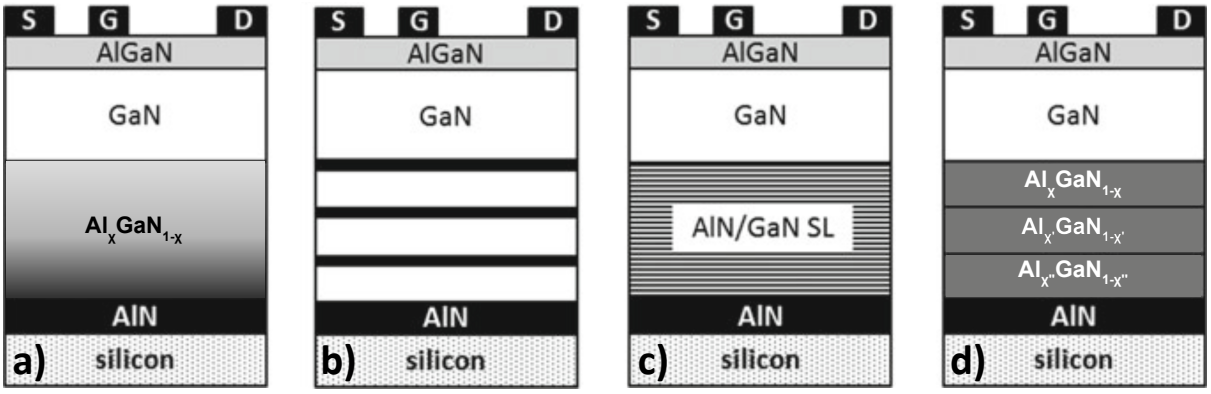

Figure 1.21. Schematics of transistors with different base layers for strain management on Si substrates. **a-** Graded AlGaN layer. **b-** AlN interlayers. **c-** AlN/GaN superlattice (SL). **d-** Step-graded. $Al_{\chi}Ga_{1-\chi}N$ layers where $\chi < \chi' < \chi''$ [48].

substrate surface [85], [86]. Due to different reasons, mainly related to the GaN deposition on foreign substrates and issues associated with GaN mechanical stress during and after epitaxy, the intrinsic defect density in GaN (Table 1.4) is much higher compared to silicon. In addition, the type of observed defects as well as their densities are directly influenced by the nature of the substrate used, growth technology and processing. Due to these different reasons, the undoped GaN-bulk is usually considered as an unintentionally doped GaN (GaN:UID) which generally appears to be a lightly doped n-type semiconductor [48]. Defect types can be classified into three different categories [87], [88]:

- **Native defects** can be found in bulk GaN due to crystallographic imperfections, such as gallium (V_{Ga}) or nitrogen (V_N) vacancies or N_{Ga} and Ga_N antisites. Atoms present in the space between the crystal sites called interstitials defects (N_i and Ga_i) can be also found.
- **Extended defects** such as dislocation which can be induced by mechanical stress, mismatch in the lattice constants between two different materials, or surface imperfections on the substrate. Other types of extended defects can be formed by impurities which tend to form complexes with native defects.
- **Impurities** can be intentionally incorporated into the lattice structure as doping such as iron (Fe), magnesium (Mg), carbon (C), or Si. However, they can also be unintentionally through a potential pollution in the epitaxy reactor or during processing. In fact, hydrogen (H) or oxygen (O) can be incorporated between two process steps during an air-break. Methyl structures of precursor gases used for GaN growth can also be a source of C or hydrogen (H).

These different defects type can create unwanted energy levels within the bandgap (cf. section 1.4.1.1).

1.3.1.5 Carbon doping in GaN

Carbon-doped GaN (GaN:C) is generally used to increase the intrinsic resistivity as well as the lateral and vertical breakdown voltage of the epitaxial structure. Indeed, the carbon concentration is correlated with the increase of the breakdown voltage as well as the decrease of the leakage currents [89]–[91] (Figure 1.22). The higher the carbon concentration the better the voltage withstanding of the device, and breakdown voltages up to 800V can be reached.

Carbon can be introduced into GaN without an external source. Indeed, carbon is present in TMG (trimethylgallium) and TMA (trimethylaluminum), commonly used for GaN and AlGaN growth as precursors [85], [92]. By using the appropriate growth conditions mainly defined by temperature, pressure and growth rate, it is possible to introduce C concentrations greater than 10^{19} with these precursors. External C-sources can be also used to introduce carbon such as CBr_4 [93].

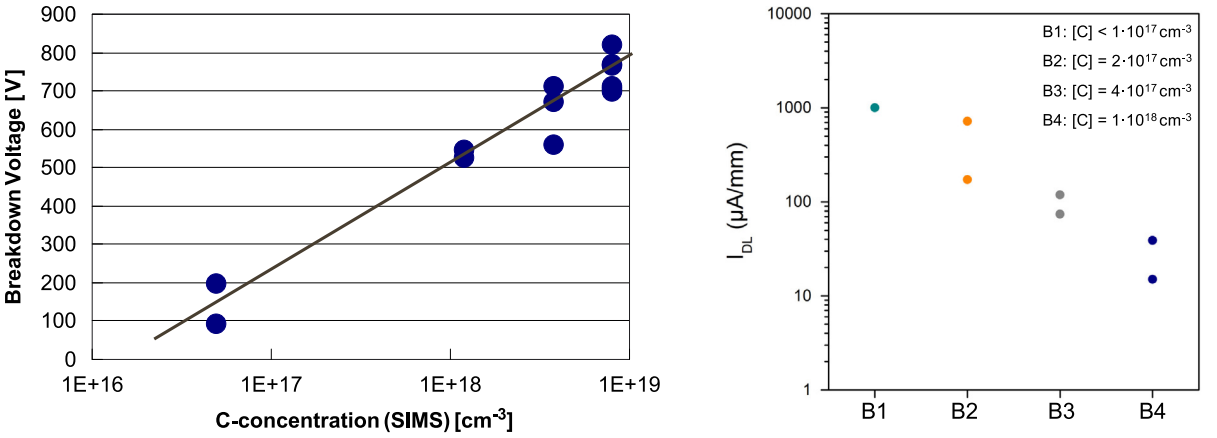

Figure 1.22. Left - Evolution of breakdown voltage as a function of carbon concentration in an approximately 0.7µm thick GaN:C layer [91]. **Right -** Leakage current of a HEMT (V_D = 50 V and V_G = 7 V) as a function of carbon concentration in GaN:C [90].

When carbon is incorporated in GaN in under Ga-rich growth conditions, C-species moves to the nitrogen position and introduces a C_N deep acceptor level at $0.8 - 0.9$eV from the Valence band [87], [94]–[96]. By introducing a sufficient carbon concentration, the GaN:C Fermi level is aligned with this deep acceptor. Hence, the number of free carriers in GaN is limited, resulting in a very resistive GaN layer with p-type doping [90], [91]. Nevertheless, compensation of C_N acceptors by C_{Ga} shallow donors ($\approx E_C - 0.2$ eV) [97] is predicted to occur, notably when the GaN:C is grown under N-rich conditions [98]–[100]. Uren *et al.* reported simulations of the free holes density evolution in the GaN:C layer as a function of the C_{Ga} concentrations, for different C_N concentration considered as deep acceptors, are shown in Figure 1.23 [101]. Although the calculated free holes concentration is modulated by the ratio between C_{Ga} acceptors and C_N donors, it can be noted that it remains relatively low with a maximum value of $10^8 cm^{-3}$. Carbon is therefore necessary to obtain a resistive epitaxial structure and thus increase the breakdown voltage. Nevertheless, carbon is also considered as one of the main contributors to the degradation of the dynamic performance and reliability of GaN-based devices [102]–[104], as it will be demonstrated in this manuscript.

1.3.1.6 Doping in GaN

Although the incorporation of C-species in GaN leads to a p-type layer, carbon is considered as a deep acceptors with a related energy level at $0.8 - 0.9$eV from the valence band maximum E_V. Nowadays, the best candidate enables to obtained shallow acceptor combined with high ionization level is magnesium (Mg) [105]. The activation energy E_a of Mg in GaN is between 110 and 170meV above E_V, which is relatively high for a shallow acceptor [106]. Indeed, it leads to a partial ionization of Mg sites and thus limits the maximum concentration of free holes that can be reached in an Mg doped layer, as illustrated in Figure 1.24. The free hole density p in the

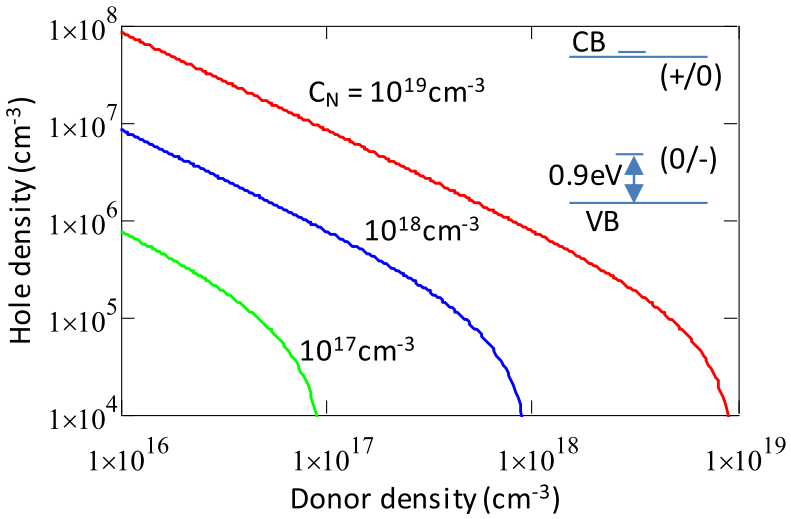

Figure 1.23. Simulations of the free holes density evolution in the GaN:C layer as a function of the C_{Ga} concentration for different C_N concentration [101].

frame of Boltzmann approximation, and the ionized acceptor concentration N_A^- are determined using the formulas given in equations 1.23 and 1.24 respectively. The hole concentration in the bulk p_0 at equilibrium state is obtained when Fermi level energy E_F satisfies the requirement of charge neutrality given by $p + N_D^+ = n + N_A^-$ [27], [107].

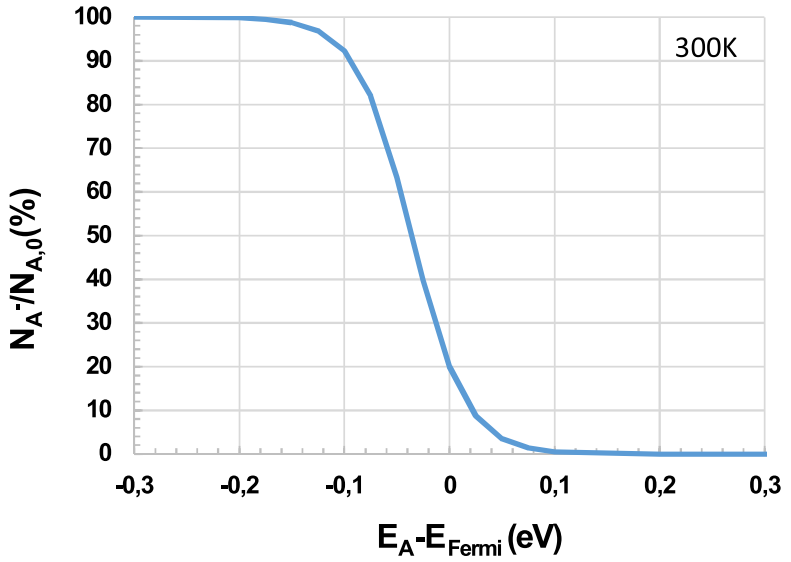

Figure 1.24. Fermi-Dirac distribution giving the fraction of ionized Mg-dopant as a function of the Fermi level energy at room temperature and for an activation energy of $E_a = 170$ meV [106].

$$p = N_V \cdot \exp\left(-\frac{E_F - E_V}{k_B \cdot T}\right) \tag{1.23}$$

$$N_A^- = N_A \cdot \left[1 + g_d \cdot \exp\left(\frac{E_{a,Mg} - E_F}{k_B \cdot T}\right)\right]^{-1} \tag{1.24}$$

Where N_D^+, is the ionized donor concentration ,
n, is the free electron density ,
N_A, is the acceptor concentration ,
g_d, is the degeneracy factor ,
k_B, is the Boltzmann constant,
and N_V is the effective valence band density of states .

To perform intentional n-type doping of GaN, silicon is usually incorporated. It is added via disilane Si_2H_6 in vapor phase into the crystal lattice during epitaxy [108]. The GaN n-type doping has no particular constraints, however it is not widely used in power devices due to GaN intrinsic doping property to be unintentionally n-type.

1.3.1.7 Passivation layer

A passivation layer is commonly deposited on the AlGaN layer to avoid surface states that induce electrical characteristics degradation. The interface between both materials must be as perfect as possible to minimize the surface states density [109]. AlN [110], SiN [102], [111], and GaN "cap" [111], [112] are the three materials mainly used to create this passivation layer. In-situ SiN, grown by MOCVD [111] or by Plasma-Enhanced Chemical Vapor Deposition (PECVD) [113] over a few nanometers, allows to obtain an amorphous and neutral material. SiN enables to passivate the nitrogen dangling bonds on the AlGaN surface in order to avoid surface states that may induce electrical dispersion, as shown in Figure 1.25-left [102], [113]. This material is compatible with CMOS fabrication process, and enables to obtain very good quality interface by limiting impurities. The use of GaN "caps" lead to the creation of an additional polarization charge at the passivation/AlGaN interface [114], thus inducing an even higher layer resistance, as shown in Figure 1.25-right [111]. However, AlN obtained by PECVD shown to be an effective passivation material, including a wider bandgap (6.2eV), better thermal conductivity, and smaller lattice mismatch with AlGaN (-2.4%) compared to SiN [110], [115].

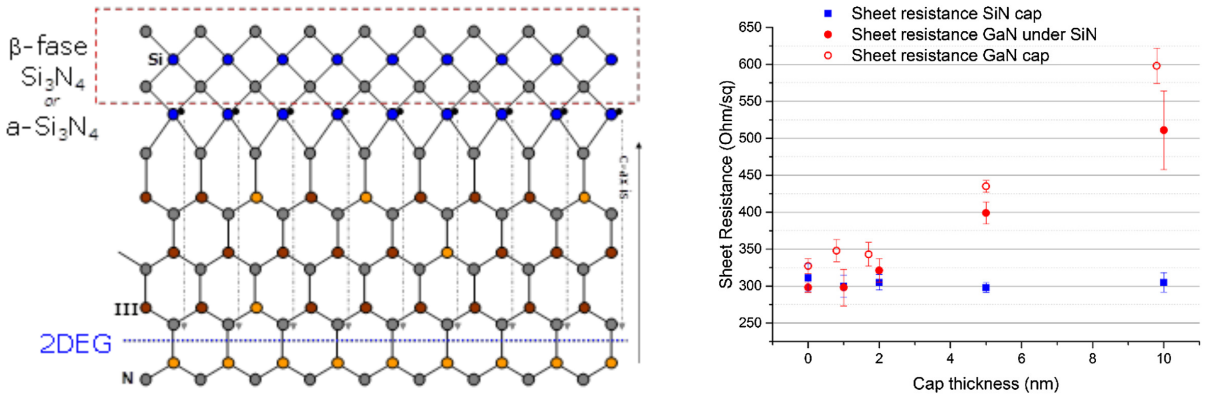

Figure 1.25. Left - Schematic representation of the N dangling bonds passivation at the SiN/AlGaN interface [102]. **Right -** Sheet resistance as a function of cap thickness, for GaN "caps", SiN "caps", and a combination of both caps, all on AlGaN barrier layers [111].

1.3.2 GaN-based diodes

1.3.2.1 Lateral Schottky diode

In this section, we will see that AlGaN/GaN hetero-junction enables to develop Schottky diodes dedicated for multi-MHz moderate power applications (< 2 kW). Since the conduction is ensured by majority carriers, the reverse recovery time is negligible and the diode can be used for high-power low-loss switching circuits [116]. Lateral Schottky Barrier Diode (SBD) is based on the AlGaN/GaN hetero-junction, in order to use the 2DEG as a highly conductive channel during On-state. Although the SBD developed in CEA-LETI is a 650V-rated technology [117], it can be adapted for applications requiring even higher voltages.

The SBD principle is presented in Figure 1.26. The 2DEG performs a lateral junction between two contacts, anode and cathode. The difference between both contacts is based on their electrical properties, where the cathode is an ohmic contact while the anode is a rectifier contact. This latter is usually obtained through a partial or fully recessed AlGaN/GaN hetero-junction followed by the metal deposition based on titanium nitride (TiN). The full recess of AlGaN/GaN hetero-junction, compared to the partial recess enables to get a higher current and a lower turn-on voltage V_{On} [117], [118]. Note that the cathode is also obtained via a full recess of the AlGaN/GaN interface followed by metal deposition based on Ti and Al.

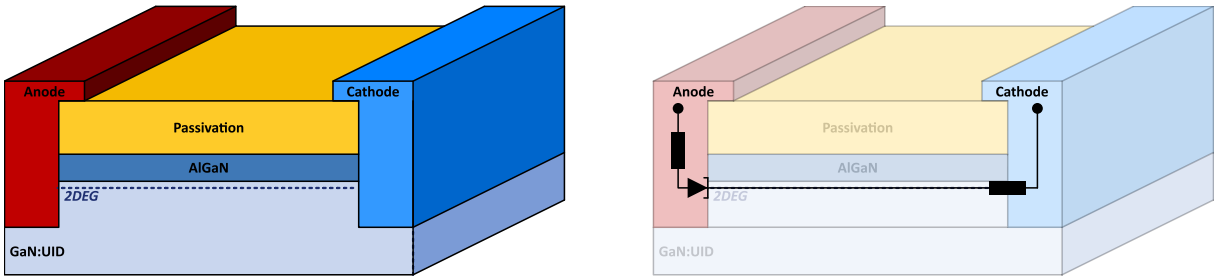

Figure 1.26. Left - Principle of GaN-based Schottky barrier diode where both contacts are represented after a full recess of the AlGaN/GaN hetero-junction. **Right -** The rectifier contact is located at the anode side, while the ohmic contact is situated at the cathode side [119].

An optimized architecture of an AlGaN/GaN Schottky barrier diode, shown in Figure 1.27a, recently demonstrated very interesting performances which are at the state of the art of GaN-based lateral diodes, and suitable for mass production [117]. Indeed, this diode depicts a current density of $100\text{mA}\cdot\text{mm}^{-1}$ at a forward bias of 1.6V and a turn-on voltage $V_{On} = 0.6$ V. Moreover, a reverse current density lower than 1µA recorded at 650V and 150°C is also reported, showing excellent performance in both forward and reverse modes. This performance were mainly achieved thanks to the full recess of the 2DEG, the fine tuning of the SiN passivation layer thickness deposited on the AlGaN barrier, and the integration of field plates (FP) which are a metal caps above the passivation layers that are connected to the anode contact [117]. The importance as well as the principle of FP will be thoroughly explained in section 1.3.5.4.

1.3.2.2 Vertical GaN-based diode

Due to the emergence of good quality and affordable GaN substrates, the development of vertical GaN devices has been boosted since 2013 [120]. These diodes are based either on a

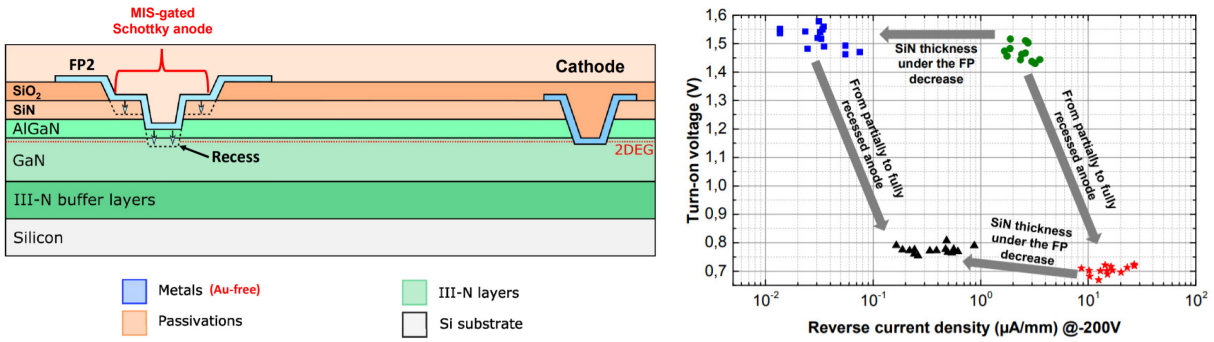

Figure 1.27. Left - Illustration of the AlGaN/GaN Schottky barrier diode developed at CEA-LETI. **Right -** Influence of the field plates, the full recess and the passivation layer thickness deposited on the AlGaN barrier on V_{On} plotted as a function of leakage current [117].

vertical PN junction (Figure 1.28-left) or Schottky barrier (Figure 1.28-right), and have the advantage to achieve high breakdown voltages and higher integration densities compared to lateral Schottky diodes. They are fabricated on GaN substrates with high N++ doping where N-type homoepitaxial layers are grown by MOCVD. The doping as well as the thicknesses of these epitaxial layers are defined according to the desired breakdown voltage [121]–[123]. The Schottky diodes are made through a palladium (Pd) or nickel (Ni) deposition on the GaN epitaxial layer. PN junction diodes are fabricated by in-situ growth of a P+ GaN epitaxial layer on the N-type GaN epitaxial drift region, followed by metal deposition for electrical contact [120], [124]. Recent work reported the development of high voltage vertical GaN p–n diodes that can sustain a breakdown voltage higher than 3.9kV and provide a current density higher than $1.4\text{kA}\cdot\text{cm}^{-2}$ with a low On-resistance R_{On} ($< 0.9\,\text{m}\Omega\cdot\text{cm}^2$) [125]. Concerning the vertical Schottky diode configuration, recent results showed that very high breakdown voltages (around 800V) and On-state currents up to 50A were achieved, with an area of $3\text{x}3\text{mm}^2$ [126].

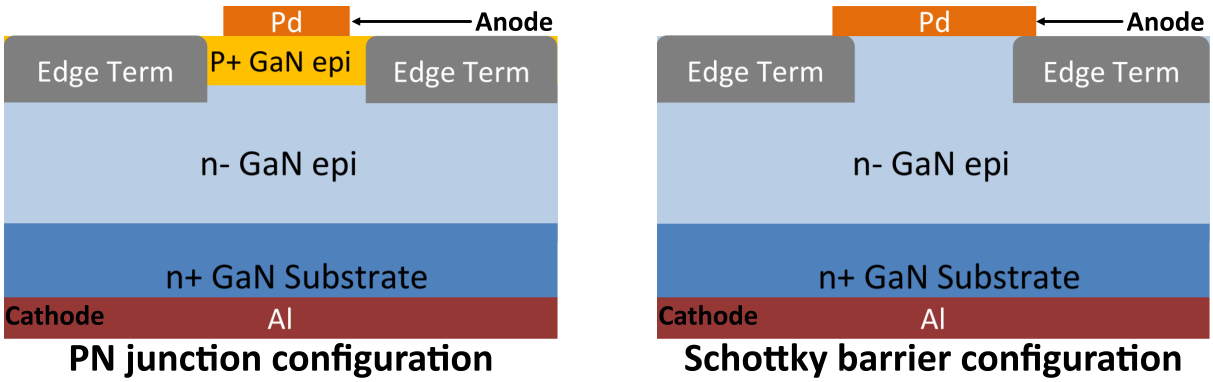

Figure 1.28. Left - Representation of the GaN-based vertical PN junction diode configuration. **Right -** Illustration of the GaN-based vertical Schottky barrier diode configuration [120].

1.3.3 Normally-On architectures

1.3.3.1 Schottky gate HEMT

The first High Electron Mobility Transistor (HEMT) based on AlGaN/GaN hetero-junction was reported in 1993, and consisted of a lateral device architecture based on a Schottky gate HEMT.

Epitaxial layers were deposited on a base-plane sapphire substrate by MOCVD and consisted of a 0.6µm thick n-GaN deposition on an AlN film, prior to the growth of a 100nm thick AlGaN barrier with an Al content of 14%. Both source and drain ohmic contacts were obtained via a full AlGaN barrier recess followed by a metallic deposition based of Ti and Au layers respectively. The gate was made by direct metallic deposition based on a TiW alloy on the AlGaN layer, forming a Schottky contact [127].

Figure 1.29 gives a representation of a typical AlGaN/GaN-based Schottky gate HEMT. At On-sate, the connection between source and drain is ensured by the low resistivity 2DEG (Figure 1.29-left). Off-sate is obtained by applying a negative gate voltage V_G which is lower than the threshold voltage V_{TH} ($V_G < V_{TH}$). It induces an electron depletion (or space charge) around the gate region and prevent the connection between the source an drain ensured by the 2DEG (Figure 1.29-right). This GaN-based Depletion-mode (D-mode) HEMT architecture was of great interest in the frame of high-frequency power applications, especially in the late 90s and early 2000s [128], [129].

In the 90s, good electrical performances of high frequency-switch power transistors were reported, with cutoff frequencies in the GHz range (35GHz in [128]) and output powers higher than $1W \cdot mm^{-1}$ [129]. However, all these devices showed a large drain current dispersion, due to charge trapping in the buffer and on the top AlGaN surface. Optimization of the substrate nucleation layers and deposition of silicon nitride (SiN) passivation layers on AlGaN [113], [130], [131] partially solved this issue. Moreover, the integration of field plates also helped to reduce this dispersion by reducing the electric field between the gate and the drain during high voltage operation (cf. section 1.3.5.4) [132], [133].
Even though this architecture is promising for RF applications and electrical performances were improved, Schottky contacts for the transistor gate have some intrinsic drawbacks. One of the main issue is the increase of the gate leakage current, especially during the Off-state when a high reverse bias is applied [134], [135]. This specific issue led to the development of the MIS-HEMT (Metal-Insulator-Semiconductor-HEMT) architecture as we will see in next section 1.3.3.2.

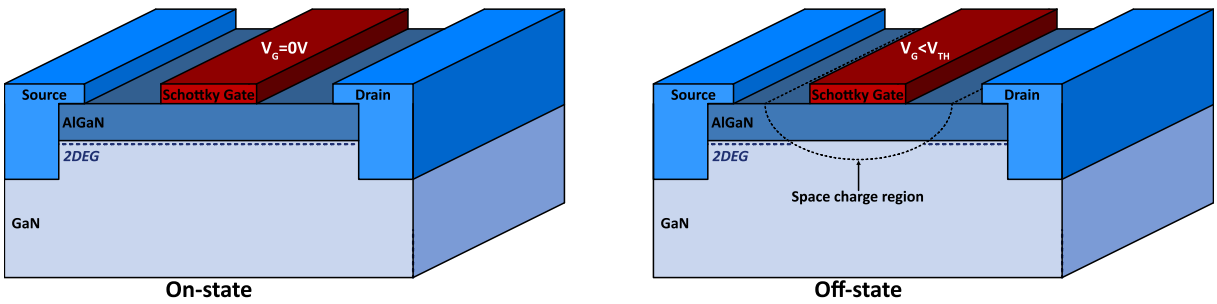

Figure 1.29. Schematic of a typical AlGaN/GaN-based Schottky gate HEMT, where the principle of this normally-On transistor is to switch from On-state (**left**) to Off-state (**right**) via the application of a negative gate voltage V_G, inferior to the threshold voltage V_{TH}.

1.3.3.2 MIS-HEMT architecture

The first MIS-HEMT was demonstrated by Khan in 2003. An illustration of the typical GaN-based MIS-HEMT is presented in Figure 1.30 [136]. A passivation layer on the top of AlGaN barrier is embedded providing a defined interface condition. The gate dielectric is typically a separated layer deposited underneath the gate, but can also be the same as the passivation layer in principle [137]. Although it has been argued that the recess of the passivation layer prior to the gate dielectric deposition may degrade the dielectric/AlGaN interface, remote-plasma and wet etching have shown a negligible influence on this interface quality due to the inertness of the (0001) AlGaN surface [137]–[140].

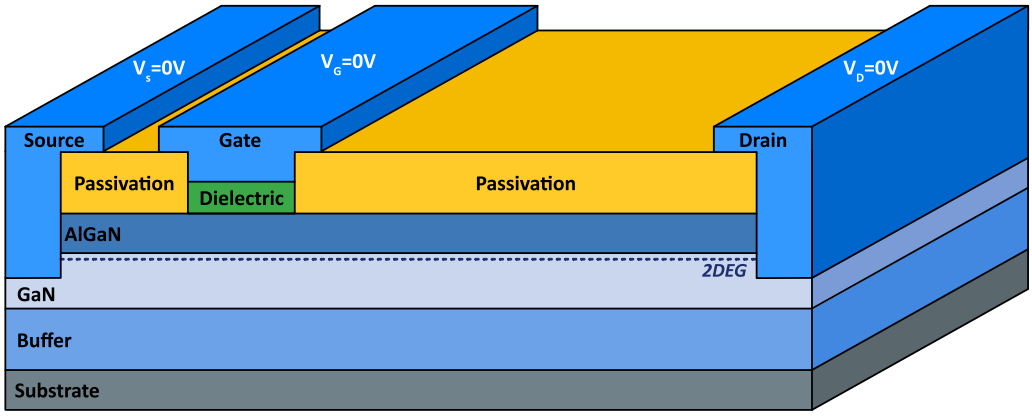

Figure 1.30. Schematic of a typical MIS-HEMT structure with a dielectric layer is integrated between the AlGaN barrier and the gate contact in order to reduce the gate leakage current.

Although the MIS gate architecture depicts a significant reduction of leakage current compared to a Schottky gate ($4-6$ orders of magnitude lower with a SiO_2 layer as gate dielectric [136]), this additional insulator layer underneath the gate introduces an new issue. Indeed, threshold voltage (V_{TH}) instabilities occur through an electron trapping within the defects at the dielectric/AlGaN interface (Figure 1.31), especially under forward bias conditions. A Coulombian repulsion between the trapped charges at dielectric/AlGaN interface and the electrons within the channel leads to a V_{TH} shift. Note that the trapped electrons also induce a local electrostatic modification which influences the V_{TH} as well. This effect is well known and called Bias Temperature Instability (BTI). Figure 1.31-left shows a band structure representation of the MIS gate stack indicating the different possible defects at the dielectric/AlGaN region. In the other hand, Figure 1.31-right exhibits a circuit model indicating the influence of the interface charge on the potential distribution across the gate stack, and then on the V_{TH} [137], [141]–[144].

1.3.4 Normally-Off architectures

As shown previously, the AlGaN/GaN hetero-junction enables the natural apparition of the 2DEG at the interface of both materials without any positive polarization. Consequently, without any specific process on the 2DEG, a negative voltage must be applied to the gate in order to switch towards the Off-state, meaning that AlGaN/GaN-based transistors are naturally Depletion-mode (D-mode or "Normally-On") transistors. For safety and reliability reasons, normally-Off transistors are preferred in power electronics industry. In case of a gate driver

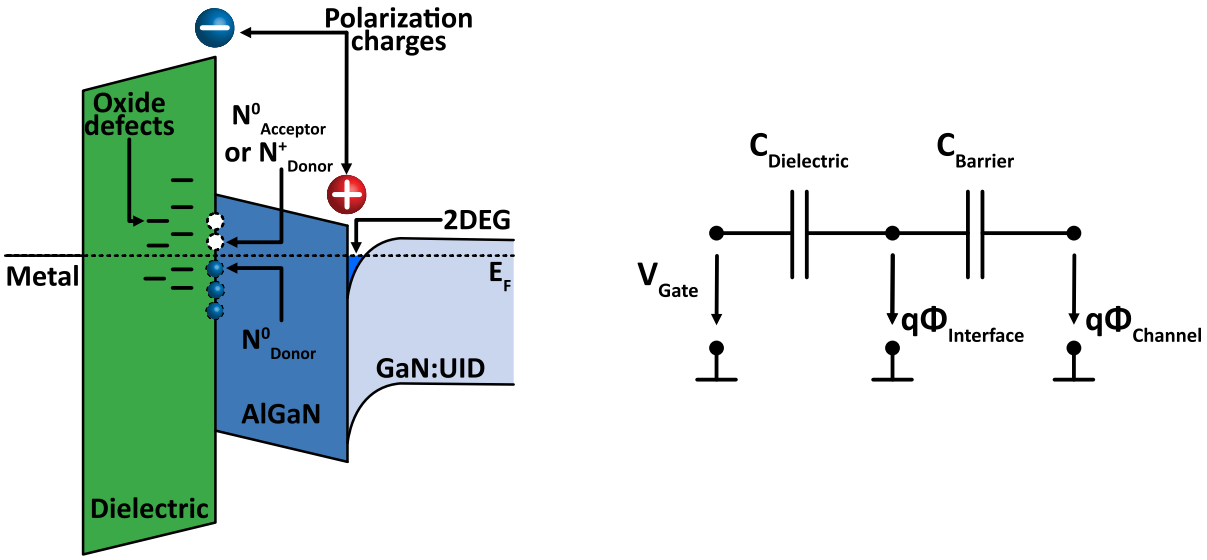

Figure 1.31. Left - Band structure schematic of the MIS gate stack indicating the different possible defects at the dielectric/AlGaN region such as positive donor states N^0_{Donor}, neutral acceptor states $N^0_{Acceptor}$, neutral donor states N^0_{Donor} and near-interface oxide defects. **Right -** Circuit model indicating the influence of the interface charge $q \cdot \Phi_{Interface}$ on the potential distribution across the MIS gate stack [137].

failure, the normally-off transistors ensure a natural cutoff of the drain current at a gate voltage set to 0V, which is not case for the normally-on and can be potentially dangerous due to the high output power. In addition, the gate drivers commonly used only allow the application of gate positive voltages, although it exists more complex gate drivers that enable to apply negative voltages. Consequently, new transistor architectures have been developed to reach the Enhancement-mode (E-mode or "Normally-Off") transistors.

The main difference between the different transistors proposed in the literature lies mainly in the gate architecture. The lateral architecture between the different concepts of transistors are very similar. In general, HEMTs are not symmetrical transistors, with a gate closer to the source due to the high voltage applied to the drain. The higher gate-to-drain distance the higher the lateral breakdown voltage, while the vertical breakdown voltage depends on the composition and thickness of the epitaxy. Contrary to a classical MOSFET for low power application, the gate does not occupy the whole width between the drain and source since the channel is already formed without any voltage applied on the whole external part of the gate.

This section introduces the most common transistors architectures having a normally-Off behavior, with their individual advantages and drawbacks.

1.3.4.1 AlGaN/GaN HEMT with a fluorine based gate

One of the concepts to get an enhancement-mode HEMT is to integrate a natural depletion zone underneath the gate dielectric of a MIS-HEMT through a fluorine (F^-) implant in the AlGaN barrier. It thus leads to a 2DEG that is present in the access regions at both source and drain sides, while it is depleted underneath the gate at the equilibrium state, as shown in Figure 1.32 [145]–[147]. The On-state is achieved by applying a positive gate voltage, resulting in the depletion region removal and the accumulation of carriers at the AlGaN/GaN interface that es-

tablishes the connection between the source and the drain. A partial recess of the AlGaN barrier doped with fluorine also showed a reliability improvement and a V_{TH} increase [148], [149].

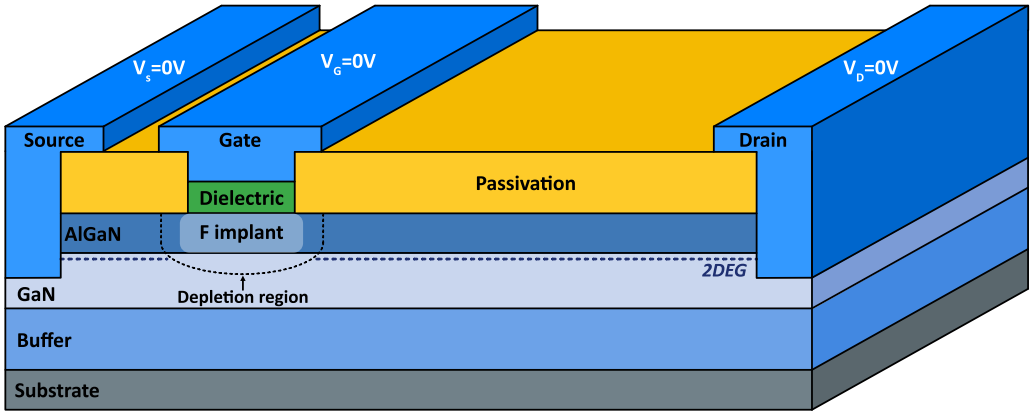

Figure 1.32. Schematic of a fluorine implanted E-mode MIS-HEMT structure at equilibrium state, where a fluorine implant is integrated in the AlGaN in order to create a depletion region underneath the AlGaN barrier and then modify the normally-On MIS-HEMT towards a normally-Off behavior.

Fluorine (F) has seven valence electrons (outer orbital in the electron shell diagram). By capturing an eighth electron, F^- has a negative charge and becomes chemically inert with a valence band completely filled, as shown in Figure 1.33 [147]. Among all the chemical elements, F atom has the highest electronegativity.

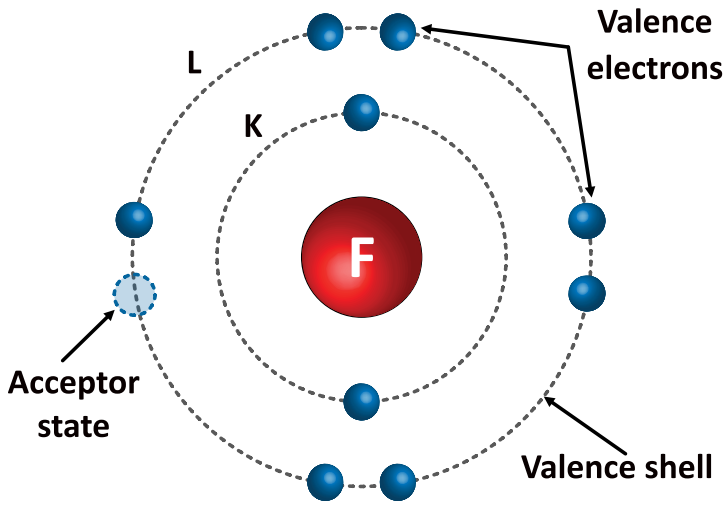

Figure 1.33. Representation of fluorine electronic structure [147].

In fluorine based gate HEMTs, ionic implantation is commonly used to effectively incorporate negatively charged F^- ions into the AlGaN barrier. Experimental results as well as molecular simulations demonstrated that the preferable and most stable position of fluorine atoms is in the interstitial position [147]. Due to their strong electronegativity property, they act as fixed negative charges in AlGaN or GaN lattice and compensate the net positive polarization charge at the AlGaN/GaN interface leading to the depletion of the 2DEG underneath the AlGaN barrier. This automatically leads to a positive threshold voltage value that can be robustly controlled by

the F implantation time [150]. Figure 1.34 gives a comparison between the conduction band profile with and without F implant in the AlGaN barrier.

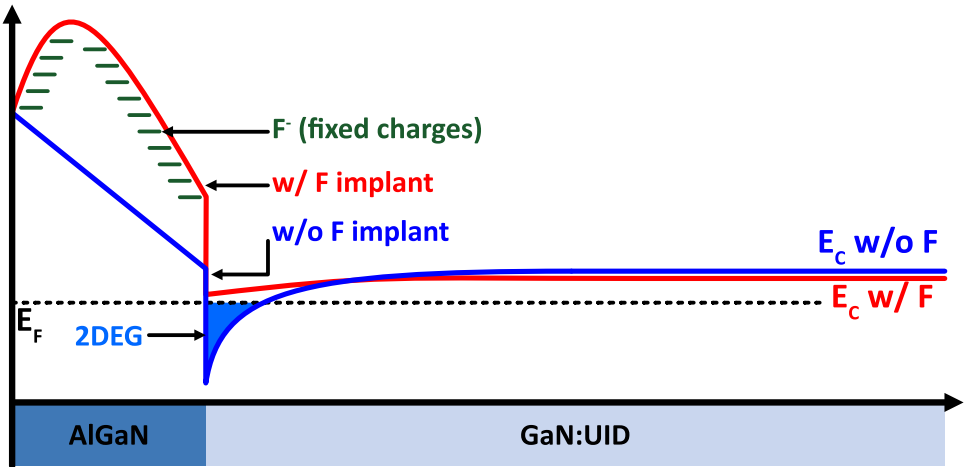

Figure 1.34. Conduction band profile of the AlGaN/GaN hetero-structure without (blue) and with fluorine implanted in AlGaN (red). An increase of the conduction band, and thus a rise of the threshold voltage towards positive values can be noticed when F^- is incorporated [147].

This fluorine-based gate has several advantages, including the fact that it gives relatively high threshold voltage values, from 0.6V to up to 3V according to the literature [147], [151], [152]. Moreover, the integration of a single process step on the gate enables to obtain a normally-Off behavior from a D-mode MIS-HEMT. It also helps the reduction of both reverse and forward gate leakage currents [145]. Finally, it also has the advantage to keep the high conductivity property of the 2DEG. Although the mobility in the channel can potentially be altered by an electron scattering phenomenon induced by the fluorine presence, it is difficult to evaluate the F^- ions influence on electron scattering. Indeed, it is possible that this mobility decrease is due to a crystal degradation of the channel induced by the implantation. A transconductance g_m degradation of 10% has been reported comparing a conventional D-mode MIS-HEMT and a fluorine-based gate HEMT, with a g_m peak from $182 mS \cdot mm^{-1}$ to $167 mS \cdot mm^{-1}$ respectively [145]. An another study reported no degradation after annealing, with a g_m peak of $151 mS \cdot mm^{-1}$ for the D-mode HEMT and $148 mS \cdot mm^{-1}$ for the E-mode HEMT [146].

However, and as the majority of E-mode transistors, the fluorine based-gate also depicts threshold voltage (V_{TH}) instabilities phenomena due to charge trapping at the interface between dielectric and the F-doped AlGaN interface, as shown in Figure 1.31 [153].

1.3.4.2 Cascode HEMT configuration

The cascode HEMT structure is a way to obtain a normally-off behavior without specific process to remove the 2DEG under the gate. It consists in obtaining, from a normally-On GaN-based HEMT, a normally-off behavior by connecting in series a low voltage silicon Si MOSFET with D-mode GaN-based HEMT. The gate voltage V_G of the HEMT is the same as the drain voltage V_D of the nMOS as shown in Figure 1.35 [48], [114], [154], [155].

The principle of the cascode GaN HEMT is quite simple. To switch the HEMT to On-state, a low positive gate voltage ($> V_{TH}$) is applied on the nMOS to switch it to On-state, leaving both

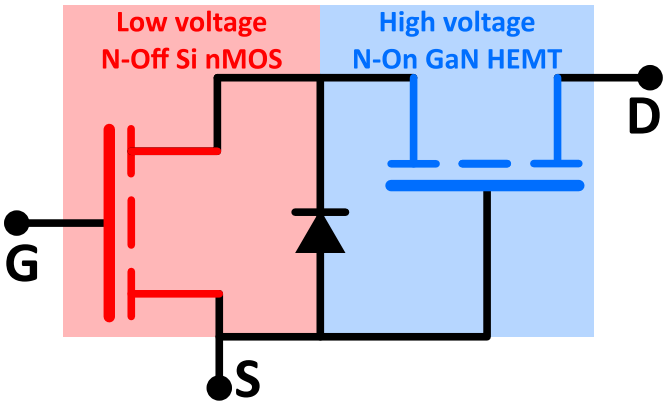

Figure 1.35. Schematic of the cascode structure where a normally-On GaN-based HEMT is connected in series to a N-Off low voltage nMOS [48], [114], [154], [155].

transistors in On-state. The total channel resistance is equal to the sum of channel resistances of both transistors. To switch the HEMT to Off-state, the silicon nMOS is turned off first. As the drain voltage increases, the GaN-HEMT will switch automatically towards Off-state when the gate voltage drops below the GaN-HEMT threshold voltage. Indeed, since the HEMT gate is connected to the source, a depletion region around the gate appears by applying a positive drain voltage. If V_D is sufficiently high, this space charge region under the gate will also deplete the 2DEG. This leads to a cutoff of the electrical connection between source and drain contacts ensured by 2DEG. Consequently, controlling the state of low voltage Si nMOS enables to drive the state of the high voltage D-mode GaN-based HEMT, and makes the cascode GaN-HEMT structure compatible with commercial drivers [48], [155].

The cascode GaN-HEMT configuration has several advantages. First, it gives rise to a positive and stable threshold voltage ($V_{TH} > 0$ V) thanks to the silicon nMOS [155], [156]. For example, Transphorm GaN device demonstrated a V_{TH} of $+2.1$V and maximum gate voltage swing of ± 18V [48]. These performances are achieved without deteriorating the advantageous properties provided by gallium nitride, such as the ability to apply a high electric field during the Off-state as well as the high conductivity of 2DEG at On-state. Consequently, it enables to get an excellent switching rate and power efficiency performances [114], [154], [157], and does not requires a specific process on 2DEG which can potentially degrade the device reliability. Moreover, the ability to use standard commercial Si nMOS drivers is probably one of the biggest benefits of the cascode configuration. Finally, this transistors show excellent results in terms of reliability, to such an extent that "the reliability of GaN is indistinguishable from the reliability of silicon" [48]. Figure 1.36-left shows the failure times versus high-voltage stress at during Off-state, while Figure 1.36-right exhibits the failure time extracted at high-temperature during On-state. A mean lifetime above $1 \cdot 10^7$ hours (≈ 1142 years) at 650V and 150°C was determined for a cascode HEMT developed by Transphorm [48].

The cascode configuration also has drawbacks. Indeed, the series connection of the two devices leads to a complex packaging, and introduces parasitic inductances that can affect the switching performances [159]. In addition, the presence of a silicon-based device limits the high temperature operations to some extent [155]. Another issue concerns the reverse recovery time when switching from On-state to Off-state, which results in a reverse conduction due to the recombination time of minority carriers in the silicon MOSFET [160]. Finally, it is also important

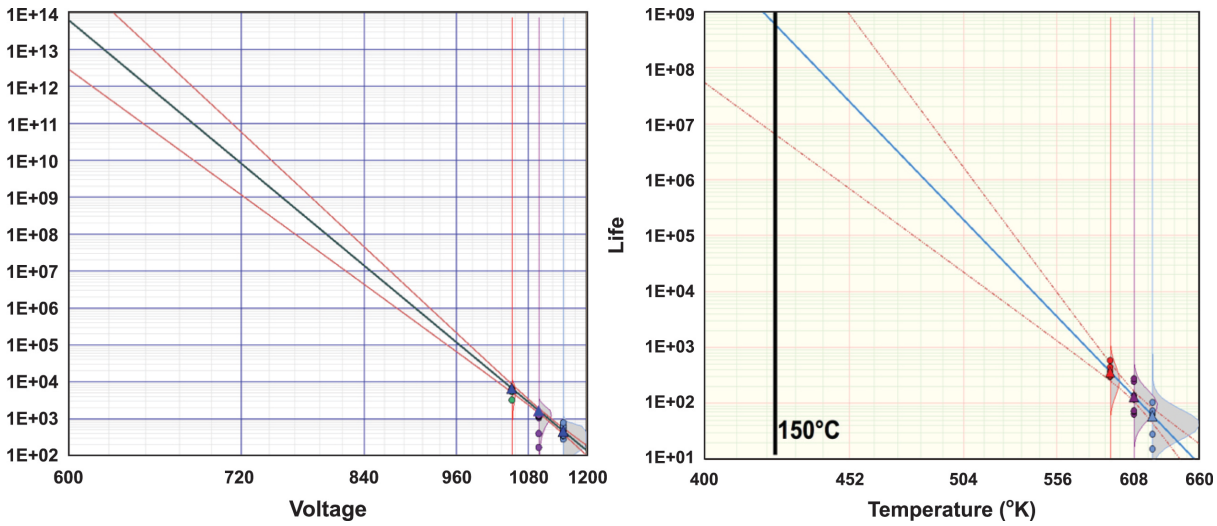

Figure 1.36. Left - Failure times versus high-voltage stress during Off-state at 82°C (expected use conditions). **Right -** failure time as a function of temperature at On-state. The drain voltage is set at 10V [48], [158].

to note that the cascode configuration works well when the D-mode GaN-based HEMT has a relatively high On-state resistance R_{On} compared to the Si nMOS which is typically designed to sustain 30V [155], [161]. When the on-resistance of the GaN HEMT decreases, which is the case when targeted breakdown voltage is lowered, the influence of the Si nMOS becomes significant. As an example, a silicon nMOS will only increase the R_{On} of an engineered 600V cascode HEMT by 3%. Figure 1.37 illustrates very well this effect by showing the contribution of nMOS on the R_{On} as a function of rated voltage. It can be noticed that the cascode configuration starts to become interesting for applications above 200V [155], [161].

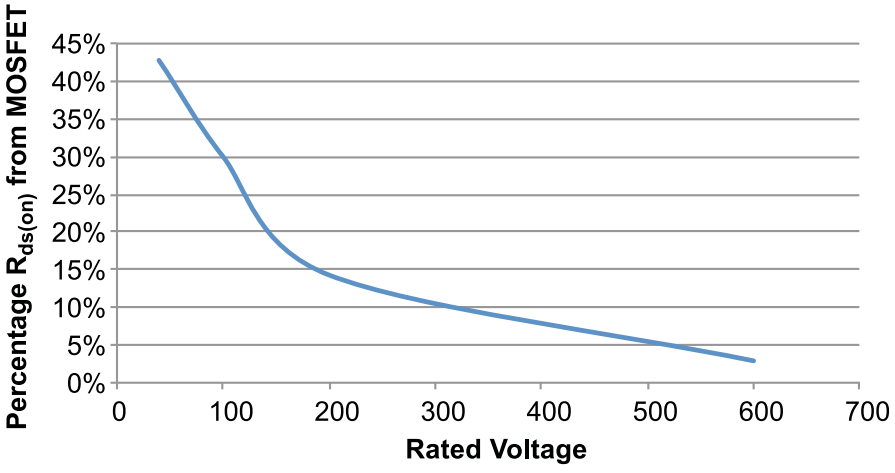

Figure 1.37. Resistance contribution of Si nMOS on the total R_{On} as a function of rated voltage in cascode configuration [161].

To overcome these latter issues, the design of the cascode configuration in a monolithic integration has been developed [159], [162]. It consists in making the same integration as a "normally-On" high voltage GaN HEMT and a "normally-Off" low voltage GaN HEMT. For example, by connecting an E-mode fluorine-based gate described in section 1.3.4.1 with a D-

mode MIS-HEMT. Both GaN transistors are directly connected via the metallization levels, as shown in Figure 1.38 [159], [163]. The monolithic cascode cancels several problems mentioned above, including the reduction of parasitic inductances and enables a switching rate increase by eliminating the reverse recovery time. It also demonstrated a reduction in turn-On and turn-Off energy losses of 21% and 35%, respectively in comparison to a discrete GaN E-mode transistor under 200V hard switching conditions. Finally a positive V_{TH} of 2V has been obtained on this monolithic architecture [159], [163]. Note that this solution is also compatible with the MOSc-HEMT architecture (cf. 1.3.5).

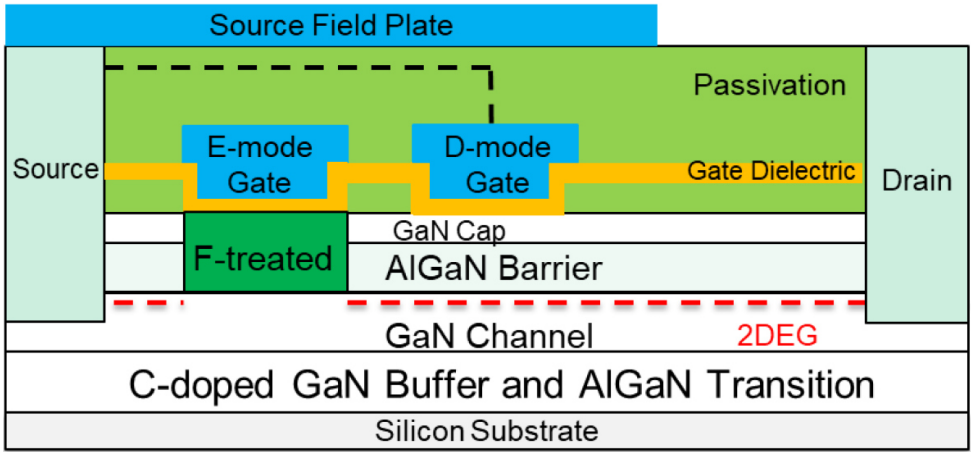

Figure 1.38. Example of a monolithic integration of a cascode HEMT where a low voltage E-mode GaN-HEMT and a high voltage D-mode GaN HEMT enable to overcome some disadvantages of the cascode using silicon nMOS [159], [163].

Several companies decided to develop cascode HEMT technology, which enables to avoid the issues associated with the critical process steps required to get an E-mode HEMT and reliability problems related to the gate (Exagan, EPC, Transphorm [164], Infineon [165], or Fujitsu [166]). However, they are also pursuing the development of normally-Off GaN HEMT solutions in parallel.

1.3.4.3 Gate Injection Transistor (GIT) or pGaN-gate HEMT architecture

Another concept to obtain an E-mode transistor is called Gate Injection Transistors or pGAN-gate HEMT. Compared to Cascode, pGaN gate architecture has an advantageous cost, a simpler packaging and can fully exploit the 2DEG properties in power applications. This solution has been chosen by companies such as Panasonic, ON Semiconductor, EPC, or Infineon. Figure 1.39 illustrates the typical E-mode pGaN-Gate HEMT structure at equilibrium state. A p-type layer is deposited above the AlGaN barrier in order to create a 2DEG depletion underneath the gate, and thus a cutoff of the electrical connection between source and drain. Historically, this architecture was first proposed by Uemoto *et al.* [155], [167], which exhibited a breakdown voltage of 800V and a V_{TH} of 1.0V.

The role of the p-type layer is to raise the conduction band at the AlGaN/GaN interface in order to deplete the 2DEG channel at a gate voltage set to 0V. Figure 1.40-a shows that the conduction band value at the interface depends on the Al concentration in the AlGaN barrier which enables to modulate the charge polarization at the AlGaN/GaN interface. Consequently,

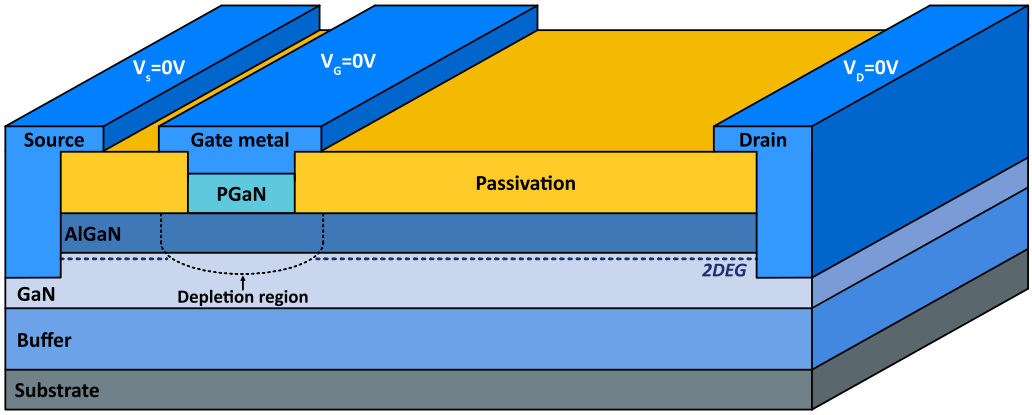

Figure 1.39. Schematic of a E-mode pGaN-Gate HEMT structure at equilibrium state, where a p-type layer is deposited above the AlGaN barrier in order to create a depletion of the 2DEG and then obtain normally-Off behavior.

Al concentration underneath the gate needs to be low ($\chi = 0.12$) while it is preferred to be high in the access region ($\chi = 0.26$). It will be seen later that this can play an interesting role in the pGaN-gate HEMT developed by Panasonic. The pGaN layer proximity with the channel also tends to increase the V_{TH} as shown in Figure 1.40-b. The p-type layer is a magnesium-doped GaN layer, and the magnesium concentration adjustment enables the modulation of the conduction band level, and thus the tuning of the threshold voltage value as depicted in Figure 1.40-c.

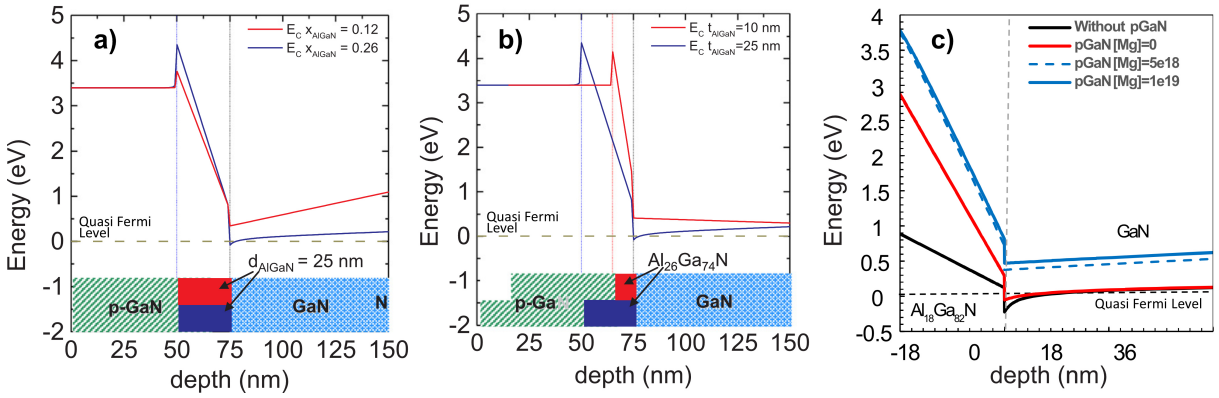

Figure 1.40. Simulated conduction band profile of a p-GaN/AlGaN/GaN stack for (**a**) two different values of Al molar fraction, (**b**) two different values of the AlGaN thickness [168], [169] and (**c**) three different Mg concentration in the p-GaN layer [106]

As shown in Table 1.5, the V_{TH} is also related to the choice of the gate metal. The influence of the metal gate work-function on the electrical behavior of p-GaN gate HEMTs was demonstrated in several studies [170]–[174]. Moreover, TCAD simulations predicted that a Schottky metal gate on p-GaN should give a higher V_{TH} and lower gate -leakage current compared to an ohmic gate contact [172], [173]. Indeed, as reported by Meneghini *et al.* [174], a WSiN-based Schottky gate metal instead of a Ni/Au-based ohmic contact deposited on p-GaN layer enables to reduce the gate leakage current by about four orders of magnitude at On-state and raises the transistor gate voltage swing.

Gate metal structure	PGaN thickness [nm]	P-doping concentration [cm^{-3}]	V_{TH} [V]	Refs.
Mo (100nm) / Ni (20nm)	80	$3 \cdot 10^{19}$	1.08	[175]
Mo / Ti / Au	60	$1 - 2 \cdot 10^{18}$	1.9	[172]
Ni	100	$1 \cdot 10^{19}$	1.23	[171], [176]
Ni / Au	60	$1 - 2 \cdot 10^{18}$	1.8	[172]
Ni (20nm) / Au (300nm)	50	$3 \cdot 10^{18}$	0.48	[177]
Ni (25nm) / Au (120nm)	60	$3 \cdot 10^{19}$	1.7-2.1	[178]
Pd (50nm) / Au (150nm)	70	Not given	1.0	[179]
Ti (50nm) / Au (150nm)	70	Not given	1.2	[179]
Ti / Au	60	$1 - 2 \cdot 10^{18}$	1.7	[172]
Ti (30nm) / Al (170nm)	50	$3 \cdot 10^{19}$	1.5	[173]
TiN	70	$1 \cdot 10^{20}$	1.6	[180]
TiN	Not given	Not given	2.1	[181]
W	100	$1 \cdot 10^{19}$	3.0	[171], [176]

Table 1.5. Literature data synthesis giving the V_{TH} of E-mode pGaN-gate HEMTs for different gate stacks [155].

Good results are shown by the use of a TiN gate, due to its processing compatibility and its chemical and thermal stability [172], [173], [180]–[182]. As reported by Posthuma *et al.* [181], a threshold voltage up to 2.1V can be obtained by the use of a TiN gate metal combined with an optimized Mg activation in the p-GaN layer.

Another solution to control the V_{TH} consists in a partial recess of the AlGaN barrier layer below the gate electrode prior to an epitaxy of the pGaN layer followed by the gate metal deposition [183], as shown in Figure 1.41-a. This approach requires an accurate control of the AlGaN etching technology, and the damages induced by the dry etching process lead to V_{TH} instabilities. In order to address these issues, a new gate recess process technology which is called "Through Recessed and Regrowth Gate" (TRRG) technology has been proposed by Panasonic [183]. It consists in carrying out a complete recess of AlGaN barrier followed by a regrowth of a new AlGaN layer. This technique shows a lower V_{TH} variability by controlling the thickness of the redeposited AlGaN, as illustrated in Figure 1.41-b. The difference of both technologies in terms of V_{TH} variability can be seen in Figure 1.41-c, where a reduction of the standard deviation from 229mV to 63mV can be noticed. Moreover, the desired threshold voltage can be chosen precisely from 1 to 2.3V in [183], by controlling the thickness and composition of the redeposited AlGaN as well as the pGaN doping level [184].

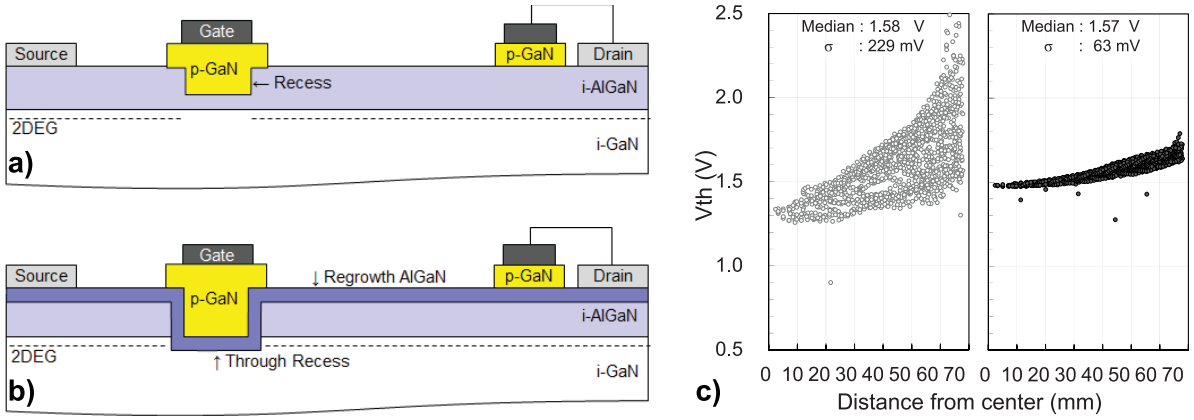

Figure 1.41. aiutg - Illustration of conventional HD-GIT with partial AlGaN recess. **b -** Representation of the a GIT integrating the TRRG technology based on a complete recess of AlGaN barrier followed by a regrowth of a new AlGaN layer. **c -** V_{TH} radius dispersion plot of conventional (left) and TRRG HD-GIT (right) [183], [184].

The pGaN-gate HEMT also exhibits the advantageous electrical property to possess two operation modes. In the first one, the device operates as a Field-Effect Transistor (FET) for low gate voltages. In the second operation mode, a conductivity increase occurs at higher gate voltages due to hole injection towards the AlGaN/GaN interface from the p-GaN layer [167], [185]. The holes injected into the channel lead to an equal amount of electrons in the 2DEG because of the charge neutrality. Due to their higher mobility, the electrons contribute to the drain current while the holes tend to remain around the gate region. This supply of holes from the grid allows an electron density modulation within the channel and enables to obtain high drain currents. That is why pGaN-gate HEMT is also called Gate Injection Transistor (GIT). However, note that not all pGaN HEMTs are GITs because some architecture work with a Schottky contact and are therefore different in operation. Figure 1.42 illustrates these different conduction regimes. At $V_G = 0$ V, the 2DEG channel is depleted under the gate due to the pGaN gate (Fig-

ure 1.42-a). For gate voltages lower than the forward built-in voltage V_F of the p-i-n junction ($V_{TH} < V_G < V_F$), the channel is formed and a drain current appears like for a conventional HEMT (1.42-b). At gate voltages higher than V_F, the injection of holes localized around the gate enables to increase the drain current (Figure 1.42-c). In fact, a second conductance peak can be noticed in Figure 1.42-d, and enables to achieve a current density up to $250 A \cdot mm^{-1}$.

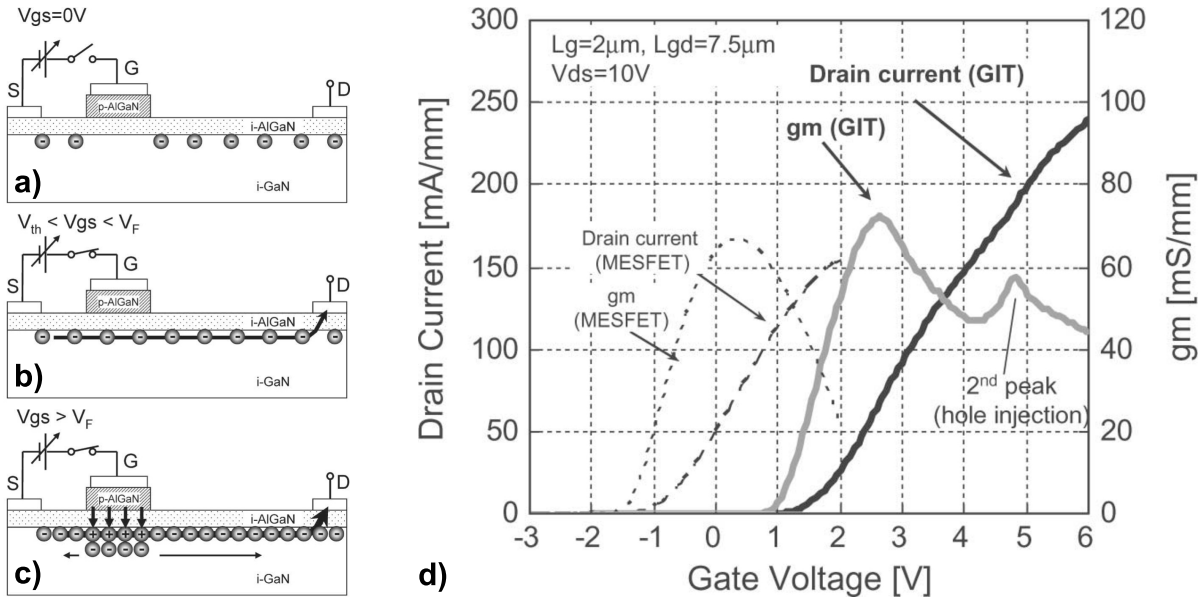

Figure 1.42. Illustration of the channel resistivity modulation of a GIT transistor at $V_G = 0$ V **(a)**, $V_{TH} < V_G < V_F$ **(b)** and $V_F < V_G$ **(c)**. $I_D(V_G)$ characteristic with the associated transconductance **(d)**. The holes injection is visible around $V_G = 4.75$ V through a second transconductance peak [167].

One limitation of this technology is the voltage range applicable on the gate. In fact, the pGaN layer on the AlGaN/GaN forms a p-i-n junction. At a gate voltage set to 0V, the diode formed is reverse biased. For a gate voltage higher than the threshold voltage, a strong electric field starts to be established in the pGaN layer. It can lead to gate breakdown caused by the creation of the percolation path in the p-GaN layer close to the metal [186].

1.3.4.4 Vertical transistor architecture

Since 2008, interest in GaN-based vertical architectures for power applications has grown steadily, with an exponential increase in published studies on the subject lately. Several vertical architectures have been proposed, such as the Current Aperture Vertical Electron Transistors (CAVET) [187]–[192], the junction FETs [124], [193], the trench Metal – Oxide – Semiconductor Field Effect Transistors (trench MOSFETs) [194], [195], the fin power FETs [196]–[200], the GaN nanowire transistors [201], as well as the Oxide GaN interlayer FETs (OG-FETs) [202]–[207] . Among all these different structures, Panasonic presented a normally-Off vertical GaN-based power transistor with very interesting performances in terms of reliability and electrical characteristics [192].

Figure 1.43-right gives an illustration of the vertical GaN process, where a n-doped GaN layer is directly grown on a bulk GaN substrate. Then, a p-GaN well layer is deposited followed

by a carbon-doped insulating GaN (GaN:C) in order to avoid a punch-through current. An undoped GaN layer (GaN:UID) followed by an AlGaN barrier is deposited in order to form the 2DEG. An epitaxial re-growth of p-GaN gate/AlGaN/GaN layers is carried out after a recess until the n-GaN drift layer, in order to form a pGaN-gate and creates a drain current aperture. Source ohmic electrodes are embedded on the surface while the drain ohmic contact is integrated on the backside of the GaN substrate. Note that the source is connected to the 2DEG as well as pGaN and GaN:C layers in the epitaxial structure. Although GaN:C is usually buried in other transistor architectures, it can be noted that this is not the case here. At equilibrium state ($V_G = 0$ V), the 2DEG is depleted by the pGaN layer as a classical pGaN gate. During on state ($V_G > V_{TH} > 0$ V), the 2DEG appearing at AlGaN/GaN interface act as a source of electrons which flow towards the drain through the n-doped GaN layer.

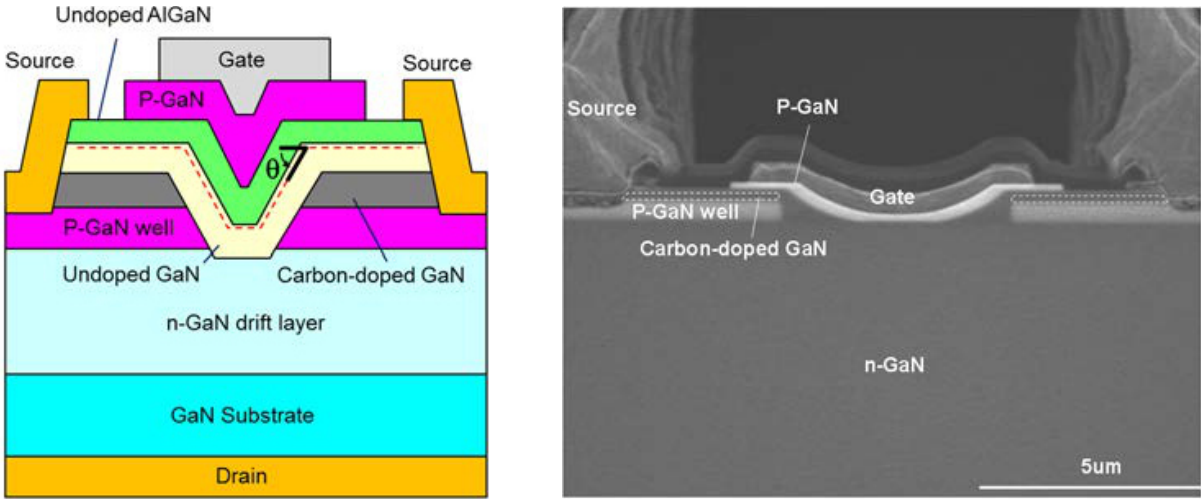

Figure 1.43. Left - Schematic cross section of a vertical GaN transistor embedding a pGaN gate **Right -** Cross-sectional TEM image of the vertical GaN transistor with regrown p-GaN/AlGaN/GaN triple layers [192].

As mentioned previously, this structure demonstrates very interesting performances in terms of reliability and electrical characteristics. In fact, it has been reported a low On-state resistance ($1.0 m\Omega \cdot cm^2$) and a high Off-state breakdown voltage (1.7kV). Moreover, the triple layers regrown over the n-doped drift layer results in a high threshold voltage of 2.5V. The drain leakage current during the off-state and threshold voltage demonstrated a very stable behavior over 300hours, as well as a fast switching at 400V/15A in the order of 40ns [192].

1.3.5 Enhanced-mode MOS-Channel HEMT architecture

The Metal-Oxide-Semiconductor-Channel-HEMT (MOSc-HEMT) is another approach to build an E-mode HEMT. Contrary to the GIT, the AlGaN/GaN hetero-junction is completely removed by etching the AlGaN barrier, and sometimes also a part of the GaN underneath [149], [208]–[210]. The gate dielectric is then deposited between the GaN and the gate metal in order to get a MOS gate, while the 2DEG is unaffected in the access regions. During the Off-state, the full recessed MOS gate cuts the electrical connection between the drain and the source which are directly connected to the 2DEG. At On-state ($V_G > 0$ V) a conductive electron channel appears along the Al_2O_3/GaN interface and ensures the connection between the drain and the source

through the 2DEG. The global cross-sectional view of the MOSc-HEMT developed at CEA-LETI and presented in Figure 1.44 is designed to sustain 650V and provides a drain current of 30A.

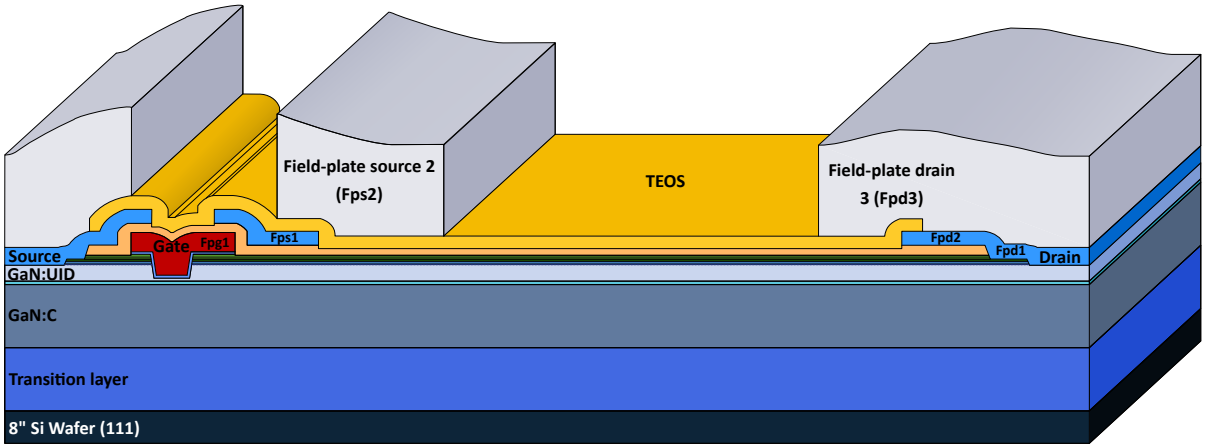

Figure 1.44. Cross-sectional view of the GaN-on-Si E-mode MOSc-HEMT after the front-end process developed in CEA-LETI.

In order to deliver a high current from a compact device, an interdigitated design was chosen with a gate width that can reach several tens of millimeters, as shown in Figure 1.45. The gate length L_G is generally between 0.25 and 2µm and the gate to drain distance L_{GD} is higher than gate to source distance L_{GS} . This unbalanced distance, as well as the field-plates presence is used to increase the breakdown voltage between the gate and drain. Note that this dissymmetric architecture is also used in other lateral GaN-based device architecture.

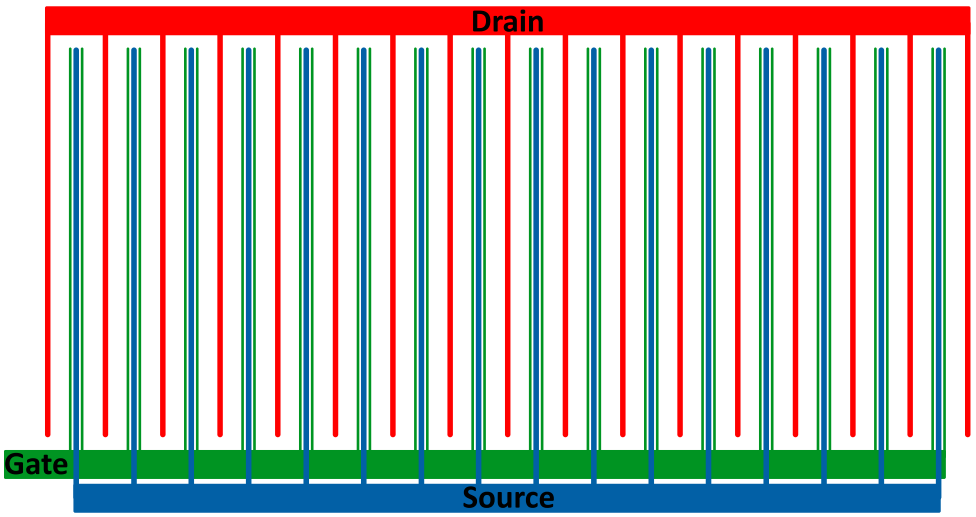

Figure 1.45. Inter-digited schematic of the GaN-on-Si E-mode MOSc-HEMT seen from top.

In the following subsections, the ohmic contacts, the gate stack as well as the epitaxial structure will be thoroughly described. The field-plates influence on the electrical performances of the devices will be also explained.

1.3.5.1 Epitaxy structure of the MOSc-HEMT

The epitaxial structure of the GaN-on-Si E-mode HEMT developed in CEA-LETI is illustrated in Figure 1.46. It is grown by MOCVD on a 1mm thick 200mm p-type (111) silicon substrate ($\approx$ 10 $\Omega \cdot$cm). A thick transition layer ($>$ 1 µm) is deposited on a thin 200nm-thick AlN nucleation layer. These layers are followed by the deposition of a thick ($>$ 1 µm) carbon-doped GaN layer (GaN:C) to ensure a vertical electrical insulation as well as a high breakdown voltage. Then, a back-barrier (BB) layer used to adjust the threshold voltage V_{TH} is grown, followed by an unintentionally doped GaN layer (GaN:UID) to form the channel. Consequently, a 24nm AlGaN barrier with 25% Al content is grown to form the 2DEG at the AlGaN/GaN heterostructure. Finally, a 10nm thick in-situ SiN layer is used to passivate the AlGaN surface.

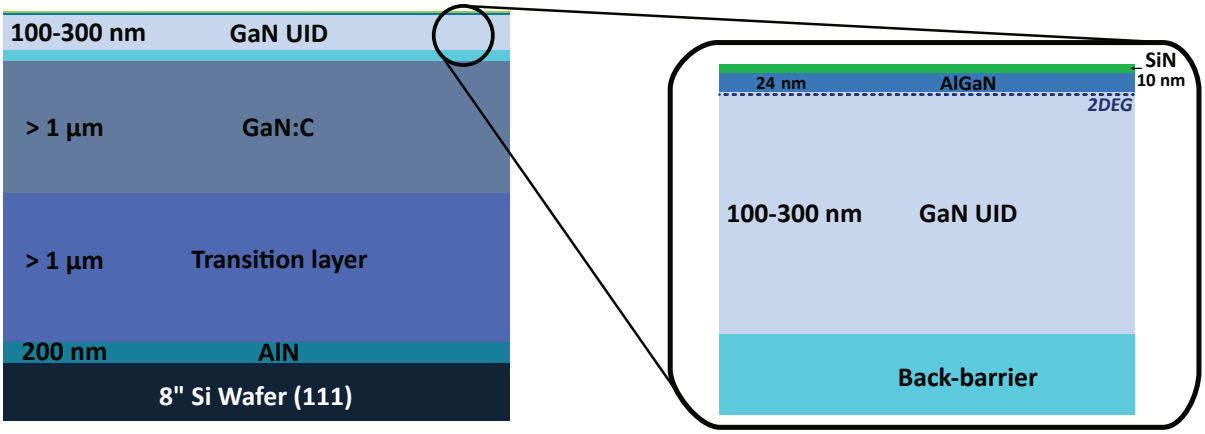

Figure 1.46. Illustration of the epitaxial structure of the GaN-on-Si E-mode HEMT developed in CEA-LETI.

1.3.5.2 MOS gate embedded in the MOSc-HEMT

As mentioned previously, one of the solutions to obtain a Normally-Off (N-Off) behavior is to remove the 2DEG, and integrate a MOS-gate. In a first time the passivation layers as well as the encapsulation dielectric are removed. Thereby, the Inductively Coupled Plasma - Reactive Ion Etching (ICP-RIE) technique is used to remove the AlGaN barrier and a part of the GaN:UID layer, in order to reach a fixed recess depth R_D from the AlGaN surface. Then, a 30nm-thick Al_2O_3 layer is deposited by Atomic Layer Deposition (ALD) on the cavity as a gate oxide, followed by the deposition of the gate metal. Figure 1.47-left shows a representation of the fully recessed gate integrated in the MOSc-HEMT. Transmission Electron Microscopy (TEM) image cross section in Figure 1.47-right exhibits the recess profile of the gate, where R_D is the recess depth, Θ_R the etching angle and m the curvature radius of the gate corner . Note that these latter parameters can vary with etching process as well as the gate length, and influence the electrical parameters such as V_{TH} and channel resistance.

1.3.5.3 Description of the source and drain ohmic contacts

The drain and source contacts consists of a ohmic connection between both contacts and the 2DEG. According to the literature, it is preferable to process these after the gate process. The

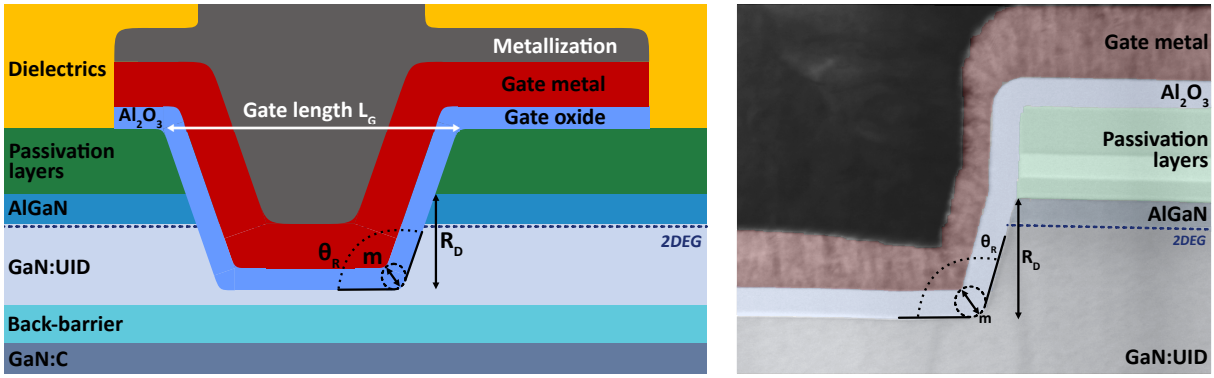

Figure 1.47. Left - Schematic of the GaN-on-Si E-mode MOSc-HEMT. **Right -** TEM cross section illustrating the recess depth. R_D is the recess depth, Θ_R the etching angle and m the curvature radius of the gate corner.

advantage of making the gate first is to allow a better alignment of the source and drain ohmic contacts with the gate via a self-alignment effect on the gate. It is also preferable to obtain a gate closer to the source which is impossible when the gate is embedded after the ohmic contacts due to design rules. This L_{GS} reduction enables to decrease the access resistances between the gate and the source [211]. One of the constraints to make the gate before the source and drain first is the thermal budget allowed by the gate. Generally, the annealing of ohmic contacts is carried out at temperatures above 800°C [82], [117], [212], while the thermal budget allowed for the gate is below 600°C. This constraint implies the process development enabling to obtain ohmic contacts with low contact resistances at such low annealing temperatures. It is for that reason that Ti/Al alloy is used in the integration of ohmic contacts. Indeed, these materials lead to a minimum contact resistance at a temperature of 550°C. Figure 1.48 illustrates a schematic of the ohmic contact.

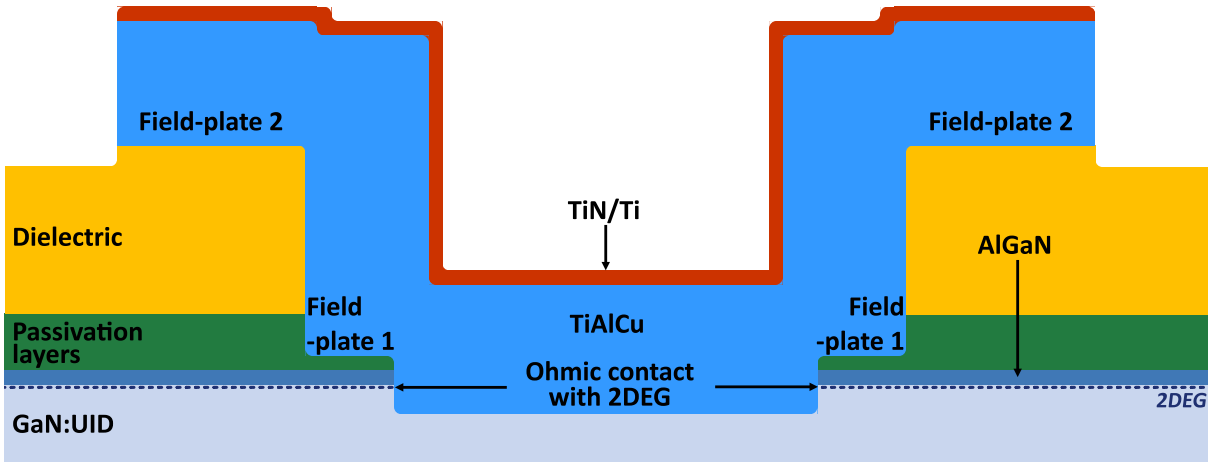

Figure 1.48. Illustration of the ohmic contacts embedded after the gate process, and used as source and drain.

The source and drain process can be separated into two main steps of etching. The first one is a combination between dry and wet etching techniques in order to remove the dielectrics and a part of the passivation layers. This first etching enables to create the first layer of field plate, which will be present at both sides of the gate. A second dry etching of 60nm $\pm$ 5nm, with

a smaller recess depth than the previous one, is then carried out by (ICP-RIE) in the recessed cavity. AlGaN/GaN hetero-structure is then recessed, in order to connect the 2DEG with the 220nm-thick TiAlCu alloy deposited by Physical Vapor Deposition (PVD) , after the second etching process. TiAlCu layer is deposited in both recessed cavities with an overlap, in order to obtain a second layer of field plate at both sides of the ohmic contact. In order to protect the TiAlCu layer against oxidation, a passivation layer of 25nm composed of Ti/TiN is finally integrated.

1.3.5.4 The role of field plates

The effect of the field plate can be explained by the very simple structure of a D-mode transistor shown in Figure 1.49-top, where the drain and the source are connected to the 2DEG [213]. As it can be noticed, a field plate is nothing more than a metallic cap connected to the source, the gate or the drain contact. It enables to increase the breakdown voltage by homogenizing the charge density in the 2DEG via a capacitive effect. The simulation depicted in Figure 1.49-bottom shows a configuration where the gate voltage is at -2.8V while the drain voltage is at 123V. This corresponds to a potential difference of 125.8V over a distance of 6.1µm leading to a high electric field between the gate and the drain.

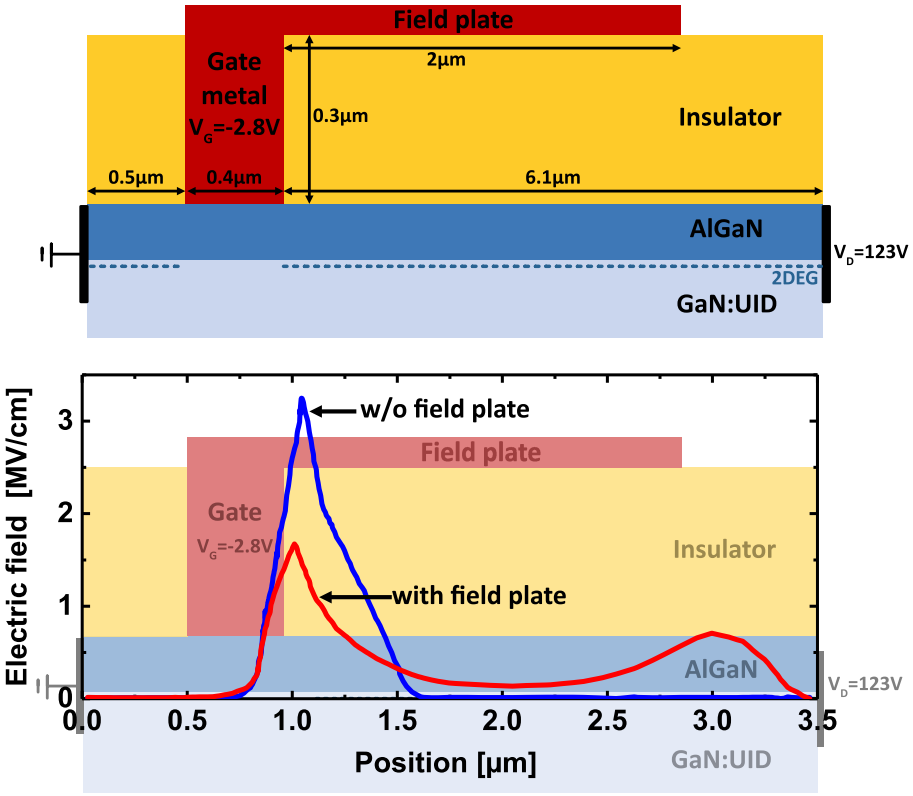

Figure 1.49. Schematic of a contact connected to the 2DEG combined with a field plate above passivation layer [213].

It can be noticed that when the field-plate is not integrated in the structure, there is a high peak of electric field at drain side of the gate due to the strong variation of charge density in the region. However, a significant decrease of the electric field peak at the drain side of the gate can

be noticed when the field-plate is embedded, due to a better charge density repartition within the 2DEG. Note that a second peak of electric field at the end of the field-plate can be observed, which also could contribute to the reduction of the lateral breakdown voltage. To overcome this issue, a second field plate layer connected to the source (as FPS1 in Figure 1.44) can be embedded above the first one in order to reduce this second peak of electric field [213].

1.4 Reliability Issues in GaN based HEMT transistors

Nowadays, the electrical stability of AlGaN/GaN based HEMTs remains the main issue that prevents their mass adoption. A large majority of the observed degradation phenomena are associated with charge trapping and are detrimental for the dynamic electrical response of the devices [214]–[217]. During regular device operation, these different degradation mechanisms overlap. In this section we will describe the different types of traps found in GaN, before describing the different degradation mechanisms including V_{TH} instabilities. This last degradation phenomenon will be described in a more exhaustive way in the third and last part.

1.4.1 Defects in AlGaN/GaN

1.4.1.1 Bulk defects

A large variety of traps in bulk GaN and AlGaN were reported in literature. These latter were mainly identified using ab initio calculations, as well as physico-chemical and electrical characterization. Despite the important efforts engaged to attribute defect levels within the GaN bandgap to specific defects, some results are often unrelevant due to systematic errors introduced by the experimental method or to the measurement uncertainties. Rossetto *et al.* reported an excellent overview of the different energy levels in GaN bandgap attributed to the most common defects found in GaN bulk, which is given in Figure 1.50 [88].

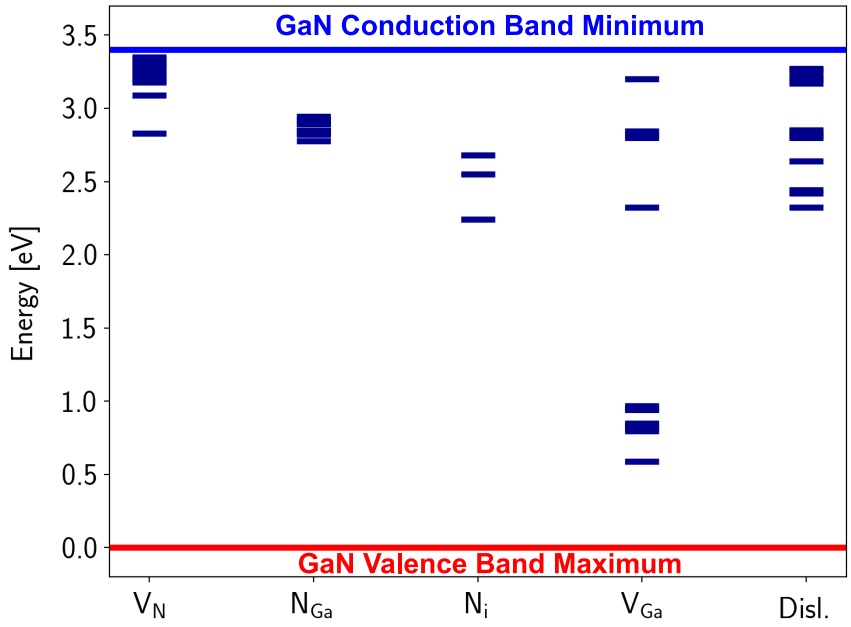

Figure 1.50. Energy levels formed by intrinsic defects in GaN bulk, such as V_{Ga}, N_i, V_N, N_{Ga} and dislocations. The blue and red lines give the E_C and E_V positions of GaN, respectively [88], [150].

One of the most common defects found in GaN bulk is Nitrogen vacancies (V_N) which are known to behave as shallow donors, with energy levels between $0.089 - 0.26$eV below the GaN conduction band energy E_C. Although they typically occur as point defects, they can also

behave as extended defects with energy levels between 0.19 and 0.25eV below E_C [218]–[221], which is probably due to a connection with dislocations [88]. Two additional levels at 0.35eV [222] and 0.613eV [223] are probably related to V_N complexes. Even tough that Honda *et al.* [224] reported that the energy level of $E_C - 0.24$ eV may be related to complexes between nitrogen and gallium vacancies, several comparisons with further studies reported that this latter energy level is ascribed to V_N [88].

Regarding occupation of Ga sites by nitrogen (N_{Ga}) , several studies using Deep Level Transient Spectroscopy (DLTS) measurements reported an energy level between 0.5 and 0.664eV below E_C, which behaves as a deep hole acceptor [224]–[227]. Similar energy levels have been reported via first-principles calculations and shows that N_{Ga} implies significant distortions of the GaN lattice, resulting in a high formation energy. Consequently, electrical influence of N_{Ga} can be considered as negligible in GaN [87], [228], [229].

Experimental measurements mainly based on DLTS demonstrated that nitrogen in interstitial position within GaN lattice N_i is attributed to energy levels between 0.76, and 1.2eV below E_C [222], [230], [231]. Furthers abinitio calculations showed that N_i defect points are related to two energy levels around 1eV from E_C, corresponding to $E_V + 2.34$ eV $(+/0)$ and $E_V + 2.52$ eV $(0/-)$. It means that N_i defects are positively charged when the Fermi level is in the lower part of the band gap, and become negatively charged at higher Fermi levels [87]. These simulation results, are also consistent with an experimental study based on electron paramagnetic resonance [232].

Gallium vacancies V_{Ga} are also commonly reported defects in GaN, however there is no consensus in literature regarding the trap level related to V_{Ga}. Honda *et al.* reported that the energy level of 0.24eV below E_C is either related to nitrogen or gallium vacancies [224]. As previously mentioned, this energy level is ascribed to V_N. Moreover, V_{Ga} has also been related to an energy level of 2.85eV below E_C, corresponding to $E_V + 0.55$ eV [233]. Other results reported energy levels around 0.6eV [234] or 1.118eV [234], [235] relatively to E_C. According to Rossetto *et al.* [88] these energy levels may be associated with V_{Ga} complex or dislocations in GaN. Finally, it has also been reported that a complex related to V_{Ga} leads to energy levels between 2.4 and 2.7eV below E_C [236]–[242]. Regarding abinitio calculations, it is important to remind that in the 90s, a low V_{Ga} formation energy around 1.3eV under Ga-rich conditions [243] has been reported using LDA (Local-Density Approximation) calculations [244]. These results suggested that Ga vacancies would be relatively abundant within GaN bulk. However, very recent simulations based on HSE (Heyd-Scuseria-Ernzerhof) calculation [245] reported a higher formation energy about 4.5eV in 2017. This high value suggests that V_{Ga} are "highly unlikely to occur in as-grown GaN, even if the chemical potentials would shift away from the extreme Ga-rich limit" [87]. Nevertheless, the same study also mentioned that complexes can form between unintentional donor impurities such as H or O and V_{Ga}, leading to the reduction of the formation energy and likely V_{Ga}-related complexes.

Finally, due to the extended nature and to the formation of complexes, dislocations are known to imply a broad range of energy levels in near to E_C, as shown in Figure 1.50. However, the energy levels reported in the literature are generally unclear about the origin of the defects, in the way that the levels may be related to intrinsic defects arranged along dislocations, such as V_N.

1.4.1.2 Defects levels induced by impurities

Rossetto *et al.* [88] have also reported a very interesting overview of the different energy levels induced by common impurities found in GaN, which is illustrated in Figure 1.51.

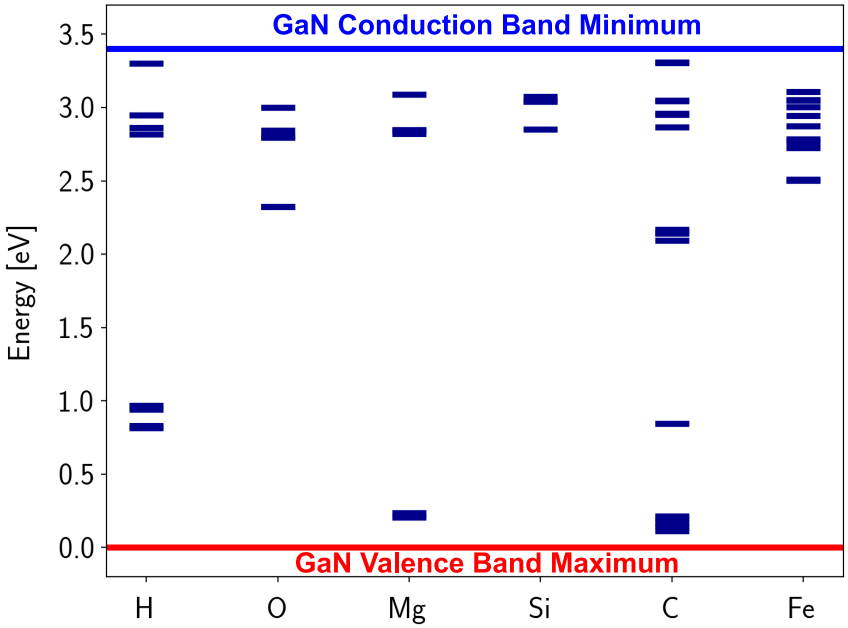

Figure 1.51. Energy levels induced by common impurities species. The blue and red lines give the E_C and E_V positions of GaN, respectively [88], [150].

Hydrogen can be found in complexes involving other defects such as Mg or V_{Ga}. Indeed, an energy level around 0.6eV relatively to E_C have been ascribed to Mg-H complexes [246]. Regarding V_{Ga}-H complexes, energy levels of 2.48eV [237] and 2.62eV [238] comparatively to E_C has been reported. In addition, other deep-donor energy levels at 0.14eV [86], 0.49eV [86], and 0.578eV [247] have been tentatively attributed to either carbon or hydrogen impurities.
Altough that silicon is commonly used as shallow donor dopant, it also gives rise to other energy levels between 0.37 and 0.59eV below E_C [248], [249].
Oxygen is known to behave as a donor 0.44eV [250] when in nitrogen site of GaN lattice O_N. However, several energy levels related either to V_{Ga}-O complexes or dislocations have been reported, with energy levels around 0.6eV and 1.118eV below E_C [234].

As mentioned in section 1.3.1.5, carbon (C) is often used in GaN to increase the breakdown voltage as well as the critical electric field E_c. Due to the amphoteric nature of carbon in GaN, it is relatively tough to clearly determine its electrical influence in GaN. Carbon in N sites of GaN lattice (C_N) is widely ascribe to an energy level located at $0.8-0.9$eV above the valence band ($E_V + 0.9$ eV), according to electrical studies as well as hybrid functional calculations [87], [94]–[96], [103], [229]. Although other studies also reported that C_N trap is related to energy levels from 0.09 to 0.18eV above E_V [98], [100], [241], these energy levels are not supported by ab initio calculations, and are closer to Mg energy level related to p-doping. Carbon in gallium substitutional position C_{Ga} , is tentatively related to a shallow donor level at 0.4eV below E_C [224]. Finally, energy levels ascribed to carbon in interstitial positions C_i are in the range from 1.28eV to 1.35eV [238]–[241].

1.4.2 Degradation mechanisms in AlGaN/GaN based HEMT

1.4.2.1 Current collapse

Since the late 90s, many studies have shown a degradation of $I_D(V_G)$ and $I_D(V_D)$ characteristics of GaN-based devices after applying a voltage stress to the gate or to the drain, as shown in Figure 1.52 [216], [251]. This degradation is mainly described by a transient drain current $I_{D,On}$ reduction as well as a threshold voltage V_{TH} shift, especially after a switch from the Off-state. Note that in the case of power devices, the drain voltage is generally higher during the Off-State (blocking state) than in the On-state. This degradation phenomenon is commonly called "current collapse", and was first observed on transistors dedicated for RF applications, where relatively low drain voltages ($\sim$ 10 V) are applied during Off-state compared to power devices [109], [252]–[255]. Since GaN-based devices are mostly interesting for their promising properties regarding the high output power they are able to provide, a strong drain current reduction combined with dispersion over the operation time is a strong reliability issue. That is why "current collapse" degradation has been the subject of many studies and research to understand its origin and then reduce and eliminate it.

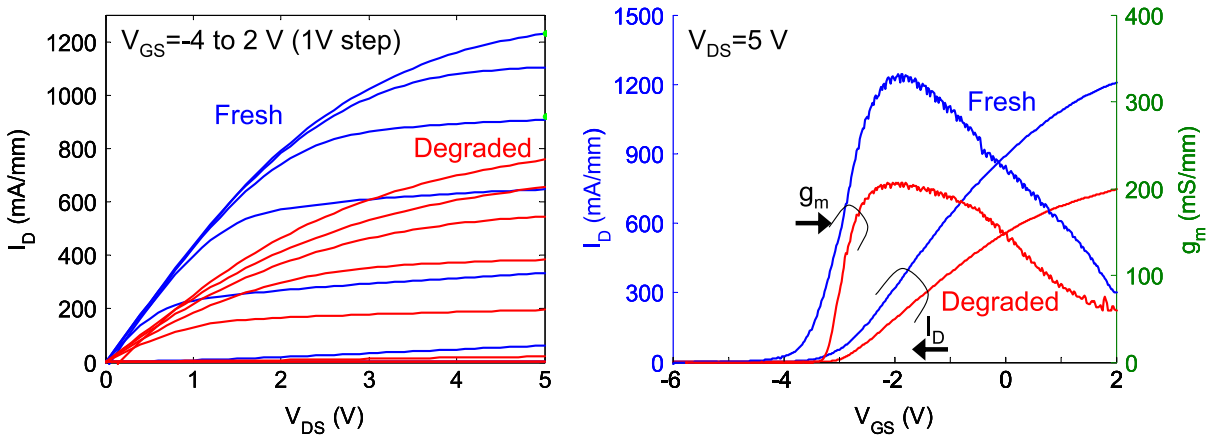

Figure 1.52. $I_D(V_D)$ (**left**) and $I_D(V_G)$ (**right**) characteristics measured on a typical GaN-based D-mode MIS-HEMT before and after a voltage stress. This latter consists in the application of a gate bias staircase from -10V to -50V, with a step of 1V during 1 minute each. The "current collapse" degradation can be observed in both characteristics [216].

Current collapse degradation in the GaN-based devices was first attributed chronologically to surface trapping. Indeed, due to the absence of passivation layer on AlGaN top surface, the electrons between the gate and the drain tended to charge the surface states at AlGaN top surface and induce a virtual gate effect. This leads to a resistance channel increase during the On-state, as shown in Figure 1.53 [109]. Numerous studies have shown that the integration of a passivation layer deposited on the AlGaN surface strongly reduces the current collapse effect, induced by charging at the AlGaN top surface [109], [131], [256], [257]. As explained in section 1.3.1.7, the passivation layer prevents the appearance of dangling bonds at the AlGaN top surface, which may act as electron traps in the region between the gate and the drain. This passivation improved of the resistance during the On-state (R_{On}), rather than a decrease

of the V_{TH} instabilities. The use of SiN or AlN as a passivation layer demonstrated a reduction of the current collapse phenomenon in both cases [110]. This degradation can be further improved by using specific surface treatments with nitrogen before the passivation layer deposition [258]. Nevertheless, despite the improvement of passivation layers, this "current collapse" phenomenon continues to be observed in the literature [259].

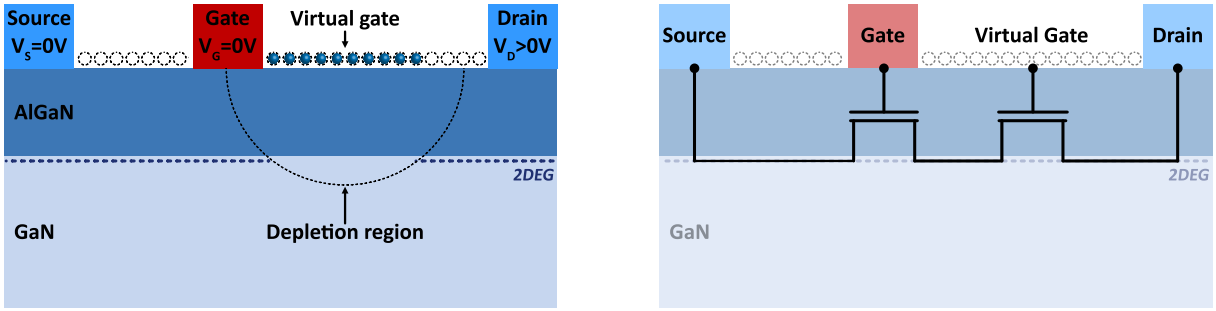

Figure 1.53. Left - Illustration of the virtual gate effect. A 2DEG depletion appears due to the surface states modification between the gate and the drain. **Right -** It is possible to simulate the virtual gate by adding an extra gate in series [109].

Optimization of the field-plates architecture also improves the amplitude of the charge trapping at the AlGaN/passivation interface as well as within passivation. Indeed, as mentioned in section 1.3.5.4, the role of the field plates is to homogenize the 2DEG electric field which strongly depends on their designs. As shown in Figure 1.49, the main purpose of field plates is to attenuate electric field peaks near the gate and drain and thus avoid premature breakdowns. However, it has been observed that field plates also reduce the current collapse phenomenon related to the top layers of the devices [260]. Therefore, field-plates have the double function of increasing the devices breakdown voltage [261], [262], and contributing to the reduction of the "current collapse" degradation [263]. Since the passivation layers and their interfaces are not perfect, the electric field distribution between the drain and the gate influences the charge trapping within the passivations and at their interfaces. Some devices with a good passivation and an optimized field-plates architecture have therefore shown much lower post-stress degradations than before. However, this current collapse degradation still remains, especially at high drain voltage (650V) and high temperature (150°C).

Another contribution to the "current collapse" takes place in deep layers of the epitaxy. The influence of these epitaxy-related traps on the current collapse degradation rises as the voltage and temperature increase [259]. Several studies carried out on epitaxy-related trapping tend to point out that the C_N deep acceptor, presented in section 1.3.1.5, as one of the root cause of the current collapse [101], [102], [264]–[269]. C_N trap leads to high R_{On} degradation associated with very long trapping and detrapping time constants. Nevertheless, there is no exact description about the trapping process that is unanimously accepted in the literature. Uren *et al.* [101] proposed that carbon-doped GaN (GaN:C) as well as transition layers can be considered as a dielectric with C_N deep acceptor traps and partially compensated by donors (C_{Ga}). The modification of C_N charge states influences the buffer that can become more or less negatively charged and partly deplete the 2DEG via a back-gating effect.

There are different solutions to prevent the current collapse degradation induced by the C_N traps. For example, Uren *et al.* [101] proposed to introduce "leakage" paths within the GaN:UID that

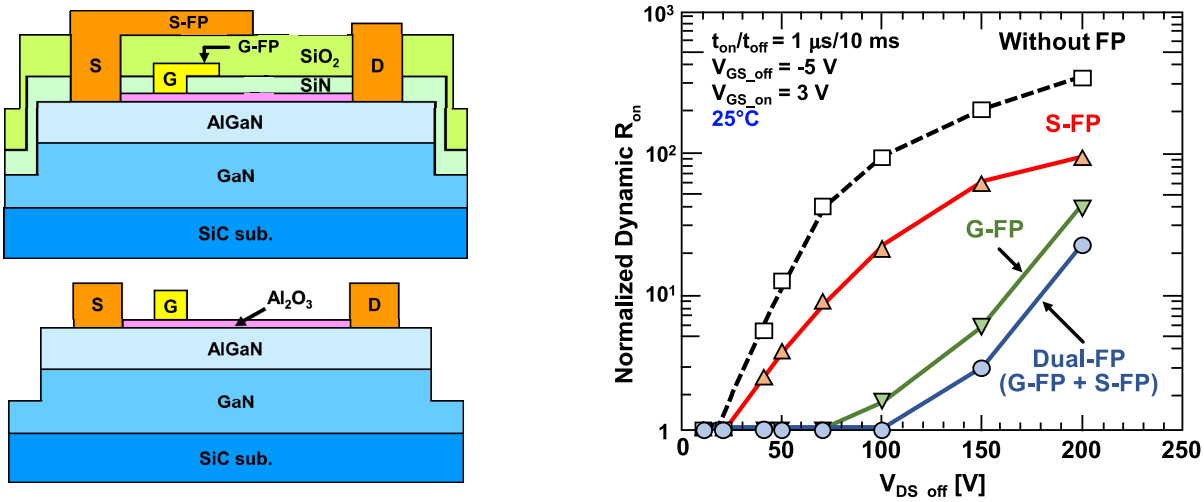

Figure 1.54. Left - Illustration of typical GaN-based D-mode MIS-HEMT with (top) and without (bottom) source and drain field-plates, S-FP and G-FP respectively. **Right -** Influence of S-FP and G-FP on current collapse degradation [263].

connect the 2DEG and the GaN:C, enabling the C_N acceptors to return to a neutral or positive charge states more quickly. This allows to avoid a C_N negative charging and do not imply a 2DEG depletion via a back-gating effect. A simulation of the buffer potential with a fixed carbon trap concentration just after (1µs) a high voltage stress is shown in Figure 1.55. Four scenarios including the introduction of these "leaky" paths are evaluated. It can be noticed that these latter prevent the remnant negative potential in the buffer.

Although these latter simulations tend to show current collapse degradation reduction, controlling the GaN:UID conductivity during growth is not straightforward, and reproducible methods have not been proposed so far in the literature. The validity of Uren's model have been experimentally demonstrated by Meneghini *et al.* for the first time, using proton irradiation in order to control the current leakage within the GaN:UID layer. The conductivity modification of GaN:UID enables to significantly reduce the dominant trapping process in the GaN:C buffer. Indeed, it prevents a massive negative charge trapping in GaN:C, and moves towards a configuration where the accumulation of positive charges is prominent. As shown in Figure 1.56, the use of proton irradiation enables to achieve a complete suppression of current collapse degradation at high drain voltage and at high temperature [270], [271].

Another solution to reduce the current collapse has been proposed by Panasonic [183], [184]. It consists in avoiding this degradation phenomenon by injecting holes in the epitaxy via the drain, which prevents the creation of a negative potential in the epitaxy. For this purpose the drain is connected to a p-type source as shown in Figure 1.41.

In any case, the use of carbon in the epitaxy used to ensure good performances in terms of breakdown voltage and leakage current, should be associated with a development solution preventing the occurrence of the current collapse phenomena. It is also important to note that the current collapse related to the buffer remains quite dependent on the epitaxy used in terms of carbon concentration, layer thickness, dislocation density, as well as growth conditions.

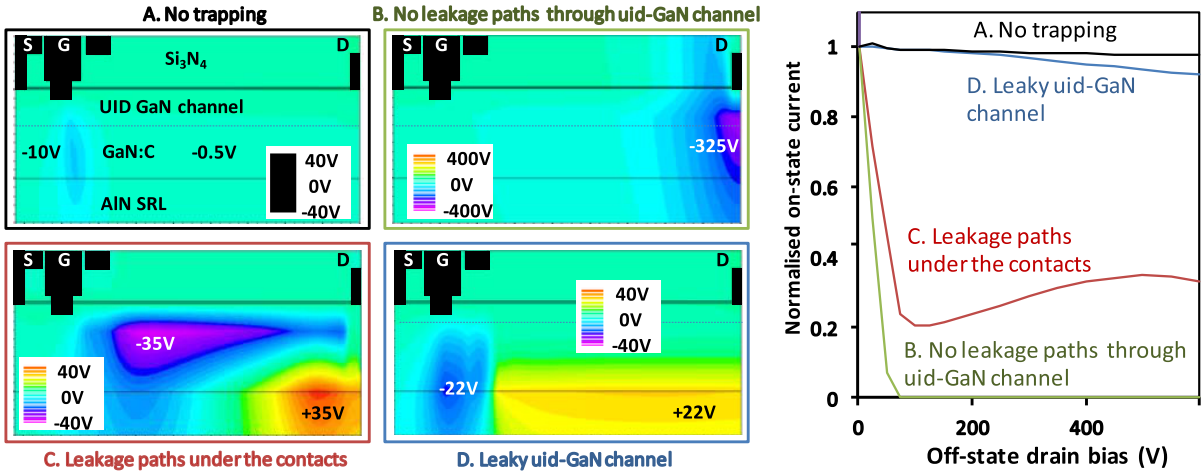

Figure 1.55. Left - Simulated electrical potential distribution of a HEMT, 1µs just after a high voltage drain stress in the Off-state. The four distributions correspond to the following situations: **A.** No traps in the epitaxy. **B.** A deep acceptor concentration of $10^{19}cm^{-3}$ at 0.9eV above E_V with no "leaky" path in GaN:UID. **C.** Same traps as B configuration but with detrapping paths under the contacts. **D.** Same traps as B and C configuration but with a leaky GaN:UID channel. **Right -** Drain current obtained 1µs after the end of high voltage drain stress, in four configurations shown at left [101].

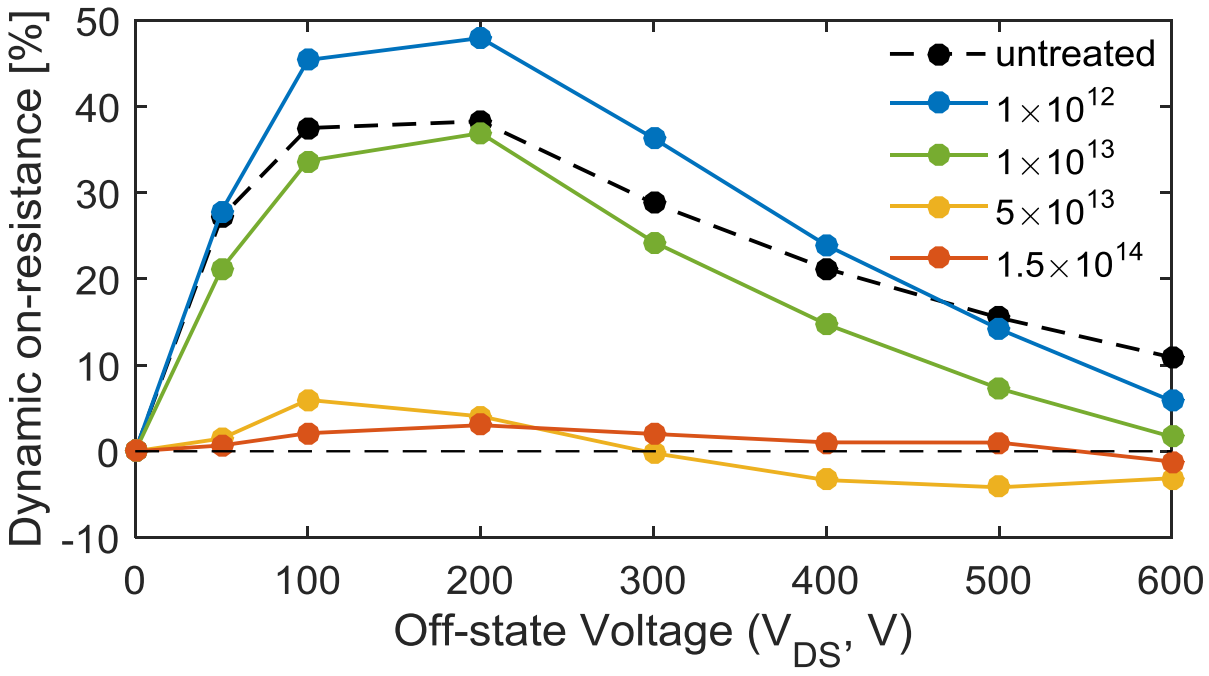

Figure 1.56. R_{On} difference obtained before and after the application of an Off-state drain voltage at 150°C for different proton irradiation [270], [271].

1.4.2.2 Hot carrier injection

Hot Carrier Injection (HCI) degradation is another type of degradation reported in GaN-based HEMTs. It especially appears during the switching from Off to On-state, when the channel is weakly conductive and the drain voltage is high. This condition is generally called "semi-on" state, and is considered as critical due to high power dissipation. Indeed, carriers having acquired a very high amount of energy (hot carriers) within the GaN channel are accelerated towards the drain leading to impact ionization phenomena. It consists in the electron transits from the valence band to the conduction band as a result of an electron channel collision with an atom. Consequently, carriers reach such an energy level that they are able to move without control within the device. They are then captured in pre-existing defects that can be found in the GaN:C, the AlGaN barrier or at the gate region, and create permanent damage [214], [215], [272]–[274]. Del Alamo and al. proposed another degradation mechanism that can potentially create permanent damage at high electric fields, and which is called reverse piezzo-electric effect. It is related to the piezoelectric properties of GaN and AlGaN materials, which can store a mechanical stress when they are exposed to high electric fields, leading to the potential formation of cracks and the creation of electrically active defects [216].

A recent study based on the electro-luminescence experiment correlated HCI to the increase of gate currents. It provides an experimental evidence demonstrating the presence of hot electrons in the channel as well as impact ionization phenomena in GaN-based HEMTs [275]. Another study proposed by Bisi *et al.* [214] also demonstrated that HCI degradation mechanisms affect the R_{On} and amplifies the V_{TH} instabilities. Moreover, Hua *et al.* reported that energetic holes trapping in the case of MIS-HEMT architecture, results in a negative V_{TH} shift associated with a decrease of the gate dielectric breakdown voltage [273]. One of the only solutions proposed to limit the injection of energetic holes in the gate was to integrate a GaO_XN_{1-X} crystalline layer at the interface between the gate oxide and the GaN. This layer creates a hole potential barrier as shown in Figure 1.57 [276], [277].

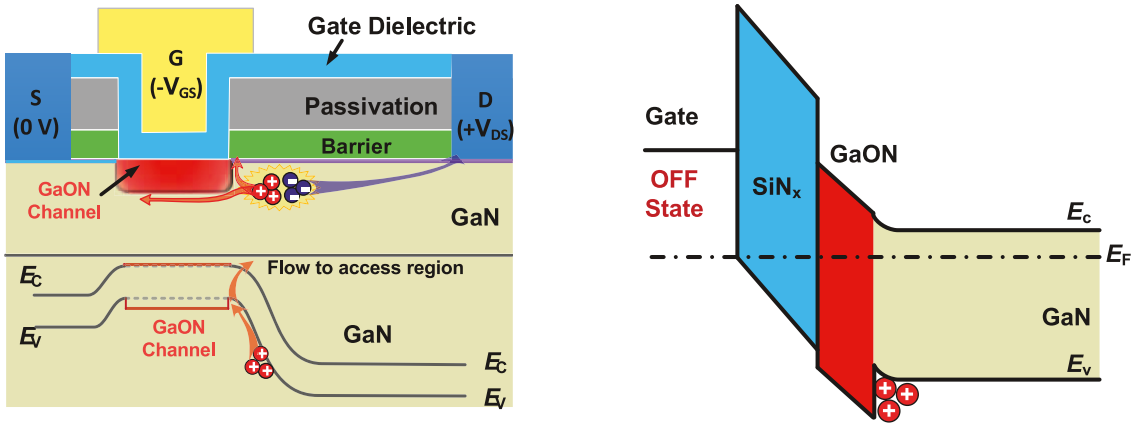

Figure 1.57. Left - Hybrid cross-section and schematic band-diagram along the channel showing the possible energetic holes current in the structure. **Right -** Schematic band-diagram of MIS-FET gate stack at off-state. Holes are not able to be trapped within the gate dielectric due the potential barrier induced by GaN layer [276].

1.4.2.3 Temperature Dependent Dielectric Breakdown

As opposite to immediate gate dielectric breakdown which is caused by a strong electric field, Time-Dependent Dielectric Breakdown (TDDB) is a failure mechanism observed for the first time in MOSFETs. It consists in the gate oxide breakdown as a result of long-time application of a relatively high electric field [278], [279].

Many studies at high electric field and high temperature were carried out to understand this dielectric breakdown as a function of time, notably in Si CMOS technologies [280], [281]. It has been observed that the device breakdown time t_{BD} follows a particular distribution known as the Weibull distribution [282], [283], and which is described by the following formulas,

$$\ln(-\ln(1-F)) = \beta_f \cdot \ln(t) - \ln(\alpha_f) \tag{1.25}$$

Where α_f and β_f are respectively the intercept and the slope of the distribution, and F is the cumulative distribution function given by,

$$F = 1 - \exp\left(-\left(\frac{t}{\alpha_f}\right)^{\beta_f}\right) \tag{1.26}$$

In the literature, two possible types of TDDB failures have been identified which are called "extrinsic" and "intrinsic" failure [284]. This latter degradation is characterized by a steeper slope at longer stress times in the Weibull distributions. It is caused by defects generation due to the electrical-field within the gate oxide. Extrinsic failure appears as a set of failures with a very broad distribution in time before intrinsic breakdown. Extrinsic breakdown is caused by imperfections induced by the process such as roughness, impurities, structural weakness and many other extrinsic defects type. It can be eliminated by processing technique improvement [285]. Figure 1.58-left exhibits a t_{BD} distribution obtained on SiC Power MOSFETs where both extrinsic and intrinsic failures are identified [286].
Finally, the well-known percolation model proposed by R. Degraeve *et al.* enables to capture the statistics of TDDB distribution [287]. In this model, defects are randomly generated within the gate oxide during the electric field application. If the defects overlap occurs sufficiently, a conduction path may be formed, leading to the dielectric breakdown. Indeed, as defects continue to be generated by the electric field, a bridge will be created across the entire oxide thickness from the channel to the gate. At the moment when this bridge is created, the instantaneous power dissipated can be enough to destroy the oxide layer and trigger breakdown.

In the past decade, there have been preliminary works on TDDB in GaN MIS-HEMT systems which were mainly conducted to confirm the trend already observed in Si CMOS [288]–[291]. Indeed, the Weibull breakdown statistics of t_{BD} as well as the breakdown time reduction with the gate electric field increase [102], [288] has been also observed in GaN HEMT. However, these studies also enable to evaluate the dielectric quality in order prevent TDDB degradation in AlGaN/GaN-based HEMT [180], [292], [293]. Figure 1.58-right gives a TEM picture under the gate where the possible percolation paths are illustrated in a fully recessed gate E-mode MIS-FETs.

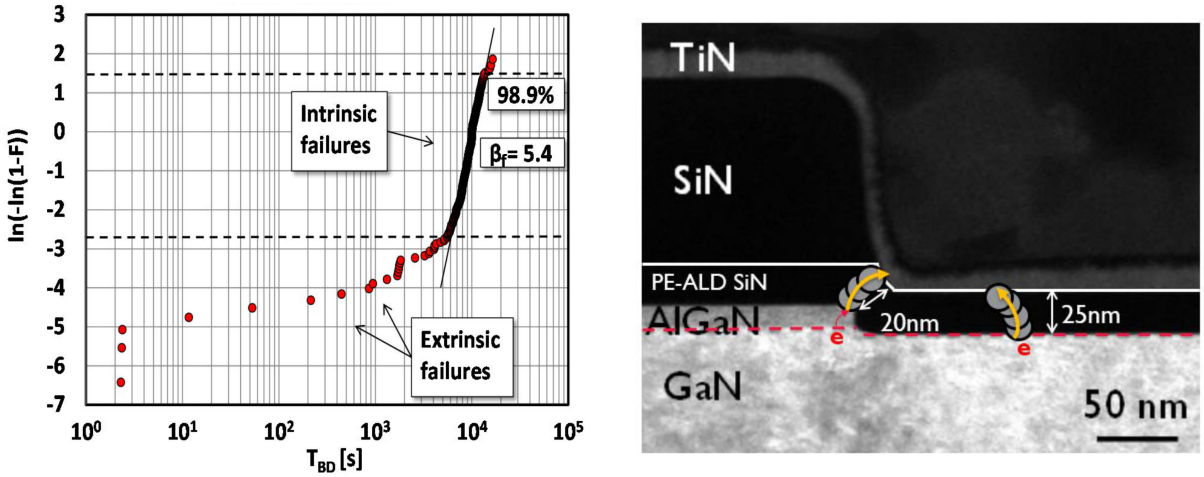

Figure 1.58. Left - Breakdown time distribution obtained on SiC Power MOSFETs where both TDDB extrinsic and intrinsic failures are identified [286]. **Right -** TEM picture under the gate where the possible percolation paths are illustrated in a fully recessed gate E-mode MIS-FETs [294].

1.4.3 Bias Temperature Instabilities

1.4.3.1 BTI principle

Bias Temperature Instability is a degradation phenomenon mainly related to a shift of threshold voltage V_{TH}. It can be also ascribed to instabilities of maximum transconductance ($g_{m,max}$) and sub-threshold slope (SS) . It mainly depends on the gate voltage value V_G, the time of applied gate voltage, as well as the temperature T. This degradation can be observed by carrying out a first $I_D(V_G)$ measurement as a reference, then applying a fixed gate voltage stress $V_{GStress}$ during a time of stress at a fixed temperature, and finally carrying out a new measurement $I_D(V_G)$. Note that the bulk as well as the drain are both set to 0V during the stress (Figure 1.59-left). As illustrated in Figure 1.59-right, a shift occurs between both $I_D(V_G)$ characteristics, resulting in a threshold voltage shift ΔV_{TH}. Note that the ΔV_{TH} shift induced during the gate voltage stress is reversible, and can be totally or partially recovered once the gate is grounded (relaxation) [295]–[298].

There are two different types of BTI degradation mechanisms. One is related to the ΔV_{TH} instabilities resulting from the application of a positive gate voltage stress ($V_{GStress} > 0$ V), and called pBTI. The other one is ascribed to the ΔV_{TH} shifts obtained via the application of negative gate voltage stress ($V_{GStress} < 0$ V), and called nBTI (for negative BTI). Historically, the pBTI was a degradation attributed to nMOS transistors, while the nBTI was ascribed to pMOS transistors. In both cases, BTI degradation is due to the carrier trapping from the conductive channel into the pre-existing defects within the gate oxide, thus leading to a local electrostatic modification at the gate oxide interface. Repulsive interactions between the charges trapped in the gate oxide and the carrier within the channel occurs. In order to compensate this electrostatic modification, a higher gate voltage $|V_G|$ has to be applied to obtain the same charge concentration in the channel, which automatically leads to a V_{TH} modification. It is important to note that the trapped charges are not permanently trapped, which gives the reversible property to BTI degradation. Indeed, when the gate is grounded or floating, the BTI degradation tends to disappear over the time due to charge detrapping, leading to a $|\Delta V_{TH}|$ shift reduction.

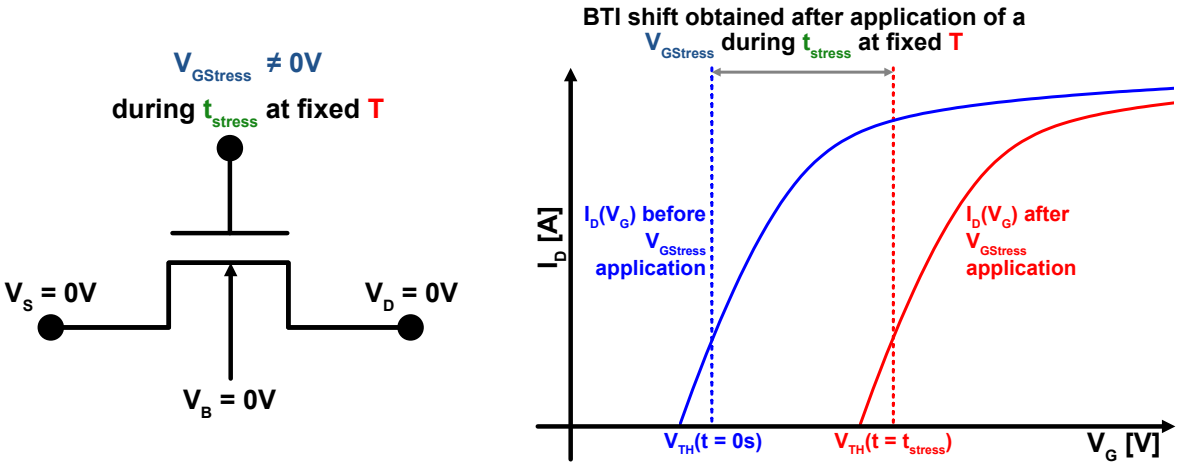

Figure 1.59. Left - Schematic of the transistor configuration during a gate voltage stress. **Right -** Illustration of the ΔV_{TH} shift obtained after the application a constant gate voltage stress $V_{GStress}$ during a certain time of stress t_{stress} at a fixed temperature T.

Indeed, these latter parameters directly influence the charge trapping dynamic. If the temperature rises, the charge trapping and detrapping phenomena are amplified due to the increase of thermal excitation of carriers. Similarly, if the electric field is increased, the charge trapping and detrapping rate is also amplified due to the higher activation of trap states in the gate oxide.

In the case a of classical normally-Off nMOS transistors, a positive gate voltage ($V_G > V_{TH} > 0$ V) must be applied to switch to On-state via an electron channel that connects the source and the drain. During On-state, the electrons within the channel are attracted at the gate oxide interface due to the positive potential applied in the gate metal. If pre-existing acceptor-defects exists in the gate oxide, the electron will be captured by these latter and imply a local electrostatic modification, as shown in the top-schematic of Figure 1.60-left. Repulsive interactions are induced between trapped electrons and the n-channel which prevent or degrade the channel formation at a fixed V_G (bottom-schematic of Figure 1.60-left). A higher gate voltage V_G has to be applied to obtain the same electron concentration in the n-channel, leading to a V_{TH} increase also called pBTI degradation (Figure 1.60-right).

Conversely to nMOS transistors, a negative gate voltage ($V_G < V_{TH} < 0$ V) needs to be applied to switch to On-state in the case of a classical normally-off pMOS transistor, leading to a holes channel apparition connecting the source and the drain contacts. In inversion mode, holes within the p-channel are concentrated at the gate oxide interface due to the negative potential of the gate metal. If there are pre-existing donor-defects in the gate oxide, the holes will be captured by these latter inducing a local electrostatic modification, as shown in the top-schematic of Figure 1.61-left. Subsequently, Coulombic interactions occur between trapped holes and p-channel, preventing the channel formation at constant V_G (bottom-schematic of Figure 1.61-left). Then, a higher gate voltage V_G needs to be applied to obtain the same hole concentration in the p-channel, leading to a V_{TH} reduction which is commonly called nBTI degradation, as illustrated in Figure 1.61-right).

Although BTI is a reversible degradation, it is one of the most critical reliability issues nowadays. This phenomenon appears when a MIS or MOS gate is integrated in a transistor, and can be found in memory, CMOS as well as in power technologies notably. In GaN-based devices,

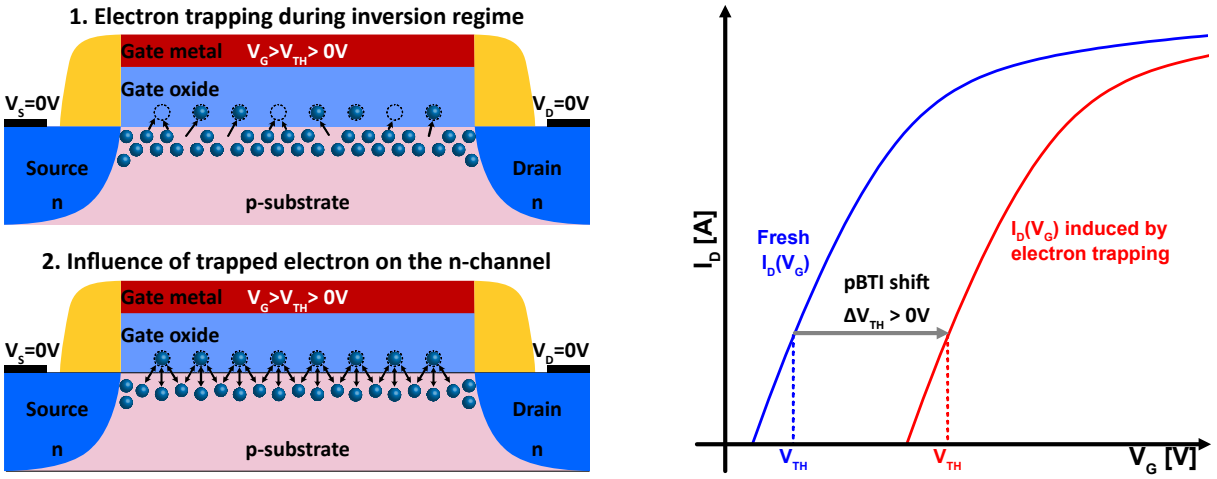

Figure 1.60. Left - 1. Schematic of the electron trapping from the n-channel towards pre-exiting acceptor defects within the gate oxide, during the inversion regime of a classical nMOS transistor **2.** Illustration of the Coulombic interactions between the trapped electrons and the electron channel. **Right -** Illustration of the positive ΔV_{TH} shift or pBTI shift induced by the trapped electron in the gate oxide.

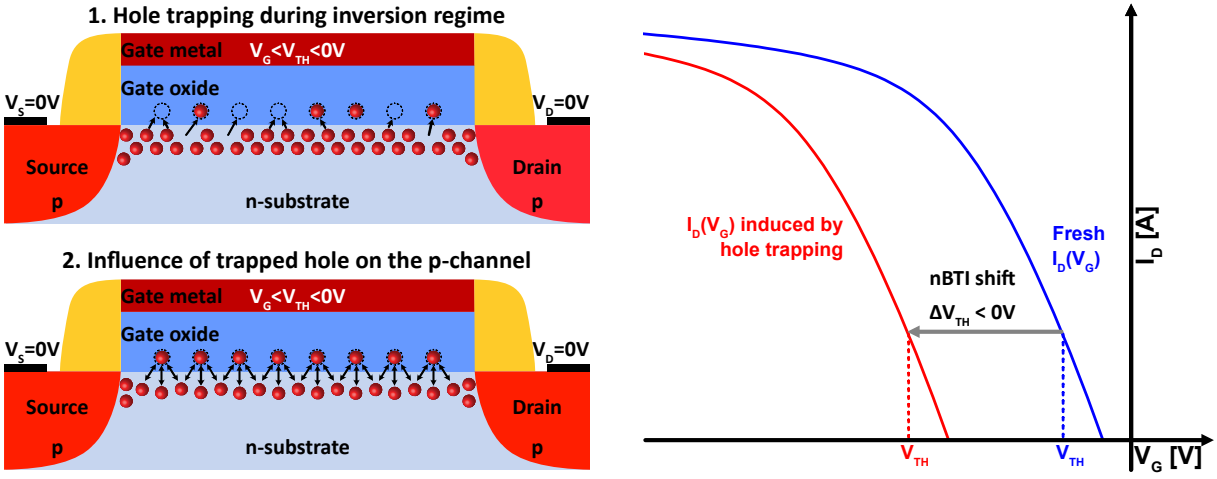

Figure 1.61. Left - 1. Schematic of the hole trapping from the p-channel towards pre-exiting donor-defects within the gate oxide during the inversion regime of a classical pMOS transistor **2.** Illustration of the repulsive interactions between the trapped holes and the p-channel. **Right -** Illustration of the negative ΔV_{TH} shift or nBTI shift induced by the trapped hole in the gate oxide.

V_{TH} instabilities are known to be one of the most critical issues. Several studies reporting BTI shift indicates that charge trapping phenomena may significantly affect device performances. Indeed, threshold voltage instabilities have been demonstrated under both positive [141], [144] and negative gate voltage stresses [207], [299]–[301], in MIS [137] and MOS-gate HEMT architecture [302] as well as in p-GaN gate HEMT configuration [303], [304]. The frame of this work lies in a better understanding of the underlying physical mechanisms leading to BTI degradations in GaN-based transistors GaN-on-Si E-mode MOSc-HEMT developed in CEA-LETI.

1.4.3.2 Experimental measurement technique

There are different ways to measure V_{TH} drift [297], [305]. In this section, the main BTI measurement methods will be discussed. We will focus on the compatibility of these different methods with BTI measurements in GaN-on-Si E-mode MOS-HEMTs.

1.4.3.2.1 Hysteresis measurement

The easiest way to measure V_{TH} drift is to perform several successive $I_D(V_G)$ or $C(V_G)$ characteristics, as shown in Figure 1.62-left. The resulting hysteresis is then directly proportional to the trapped charges density within the gate oxide [306], [307]. However, this measurement method has several drawbacks to characterize the traps electrical response. Indeed, the hysteresis depends on the sweep rate, the bias range (Figure 1.62-right) and the sweep direction [308].

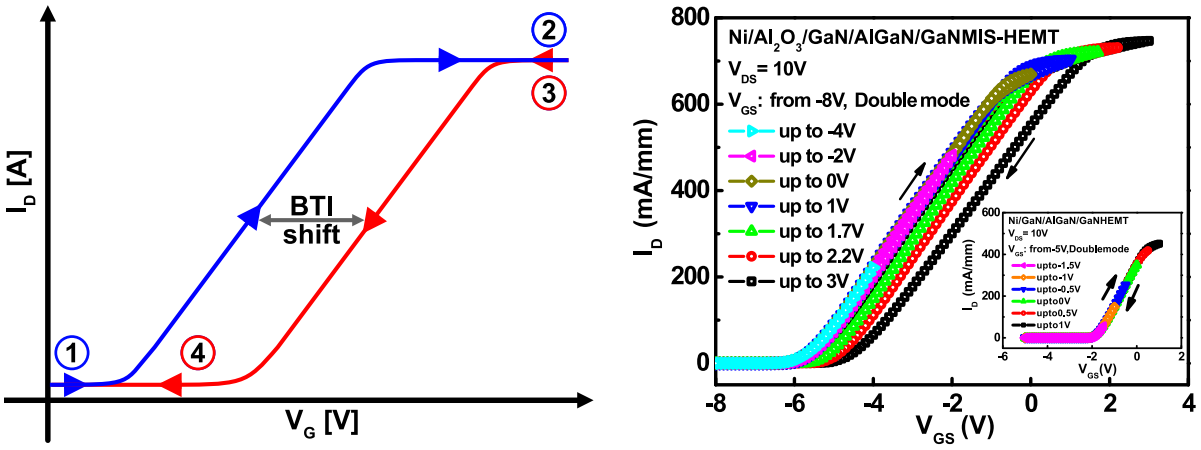

Figure 1.62. Left - Schematic of a way to measure BTI shift using hysteresis method, where the drain current is recorded during the forward V_G sweep (blue) directly followed by a backward V_G sweep (red). **Right -** Experimental $I_D(V_G)$ hysteresis measurements obtained by applying different V_G range on a GaN-on-Si MIS-HEMT. An influence of V_G range on hysteresis can be noticed [309].

In the case of BTI measurements in GaN-based devices, the wide range of capture and emission time constants and the large defect density require to be characterized using very short time measurement, much lower than milliseconds. It is therefore very complex to characterize a certain defects range when the minimum sweep time of standard parameter analyzers is generally limited to milliseconds. Indeed, traps which have a capture and emission constants time lower than the sweep rate would lead to a dispersion of the $I_D(V_G)$ or $C(V_G)$ characteristics, which

can easily be the source of results misinterpretations [143]. It is the reason why the obtained results using this method must be used with caution for the traps characterization.

1.4.3.2.2 On-the-fly method

The On-The-Fly (OTF) measurement enables the continuous ΔV_{TH} monitoring under a fixed gate voltage stress without any measurement delay [310], [311]. This BTI measurement technique consists in I_D degradation monitoring (at fixed V_D) over the time during the application of $V_{GStress}$, thereby avoiding any relaxation. Considering the device is operating in linear regime, the threshold voltage V_{TH} shift can be deduced from the drain current I_D obtained at a fixed $V_{GStress}$ after a certain time of stress, using the following expression.

$$\Delta V_{TH} \approx \frac{I_D - I_{D,0}}{I_{D,0}} \cdot (V_{GStress} - V_{TH,0}) \tag{1.27}$$

Where $V_{TH,0}$ is the initial threshold voltage measured at $t_{stress} = 0$ s, and $I_{D,0}$ is the corresponding drain current obtained at $V_{GStress}$. This latter OTF method (OTF1) has been improved in OTF2, which takes into account the mobility variation via the transconductance g_m measurements during the gate voltage stress. The g_m shift is deduced using a small-signal modulation of the gate voltage stress [312]. Afterwards, a better integration of mobility variations during the stress was proposed in OTF3 method [313], [314].

Even though the OTF method allows a continuous ΔV_{TH} monitoring without any measurement delay, there is always an intrinsic delay t_0 before the first measurement. Indeed, $I_{D,0}$ initial measurement takes $1 - 100$ms with a typical analyzer (B1500 or HP4156), during which some ΔV_{TH} degradation occur under $V_{GStress}$ application [315]. Figure 1.63-left shows that all OTF methods suffer from the t_0 delay which is inherent to the first measurement point and strongly distorts the data [314]. OTF methods limitations are also depicted in Figure 1.63-right showing a significant simulating error due to the mobility variations. Note that the theoretical accuracy in the case of OTF2 method is complex to set up in practice, because the extracted ΔV_{TH} is extremely sensitive to unavoidable measurement errors in the estimation of g_m [314], [316].

1.4.3.2.3 Measurement-Stress-Measurement technique

The Measurement-Stress-Measurement (MSM) technique is considered as the the most accurate BTI measurement [314], and is described in Figure 1.64 [141], [143], [317]. During the stress phase, a gate voltage stress is applied causing the charging of the trap states within the gate oxide. As previously mentioned, the degradation type (nBTI or pBTI) is conditioned by the sign of the applied gate voltage. Note that the source, drain as well as the bulk potentials are fixed to the ground. In order to control the V_{TH} degradation during the stress phase, measurements of $I_D(V_G)$ are performed during a very short time, and are considered not to influence the traps state [143]. Fast $I_D(V_G)$ measurements are performed by applying a voltage sweep (or staircase) on the gate in less than 10μs, while the drain current I_D is recorded via the application of a low fixed drain bias V_D. After the stress phase, recovery starts to monitor trapped charges relaxation. The difference between stress and recovery lies in the $V_{GStress}$ which is different than 0V during the stress phase, and set to the ground during the recovery phase. In the same

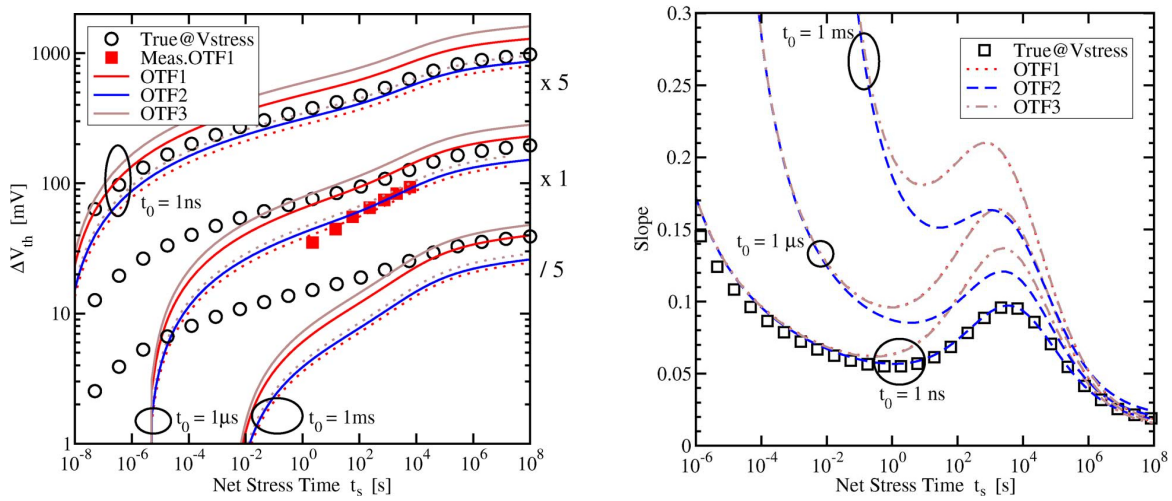

Figure 1.63. Left - Influence of the initial delay t_0 on the results obtained by the three OTF measurements methods. **Right -** Influence of the different OTF measurement methods on the observed slope. OTF1 and OTF3 methods exhibits an important error due to the mobility modification [314].

way as the stress phase, the ΔV_{TH} shift is also monitored during the recovery phase.

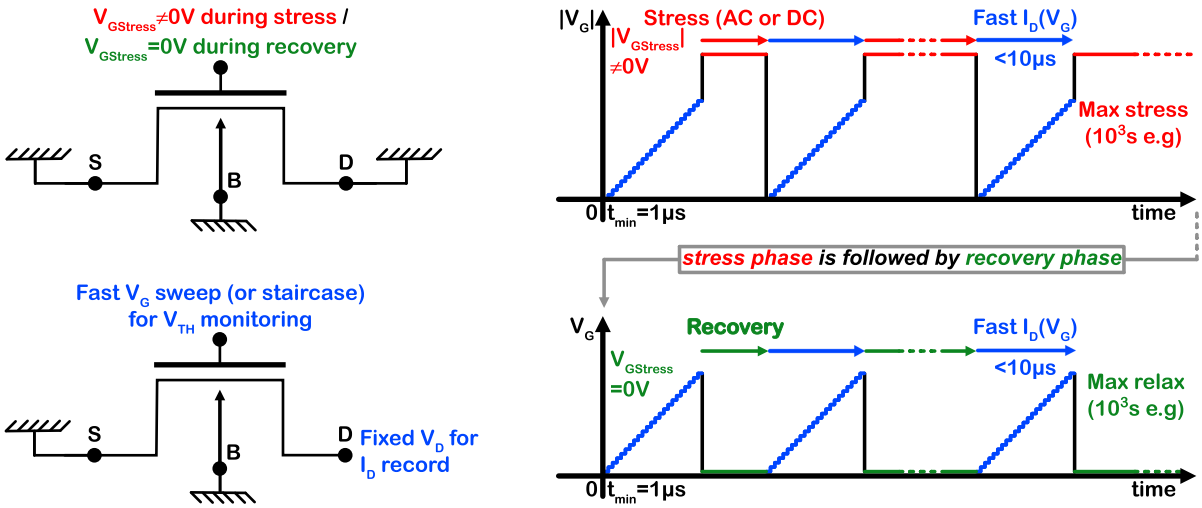

Figure 1.64. Left - Transistor configuration during stress and recovery phases (top), as well as during fast $I_D(V_G)$ measurements for V_{TH} monitoring (bottom). **Right -** Illustration of the chronograph applied on the gate during stress (top) and recovery (bottom) phases.

Using a pulsed experimental setup on the gate and drain thus allows trap characterization down to a few microseconds. Therefore, this method allows scanning a wide range of the capture and emission time constants. However, there are some fundamental drawbacks by using the MSM technique. One of them is that we assume that fast $I_D(V_G)$ measurement does not alter the device. In the case of a E-mode HEMT integrated a MIS or MOS gate, this assumption is probably true for a gate voltage range between 0V and a positive V_{TH}. For a gate voltage above V_{TH}, charge injection at the gate oxide interface occurs. For V_G below 0V, a depletion zone appears within the buffer layers and can lead potentially to additional unwanted trapping or detrapping phenomena under the gate [137].

Moreover, this measurement technique could lead to an underestimation of the real V_{TH} drift. Indeed, during the stress phases, the device is subject to a gate voltage stress where charge trapping can occur leading to a threshold voltage modification. However, the induced ΔV_{TH} remains undetected as it cannot be monitored during the gate voltage stress application. After a certain time t_{stress} , the gate stress stops and the transistor starts to recover. The trapped charges may already be emitted before the first moment at which it is possible to detect the threshold voltage, corresponding to $t_{response}$ in Figure 1.65-left.
An illustration of V_{TH} drift during stress and recovery phases after two stress times $t_{stress1}$ and $t_{stress2}$, such as $t_{stress2} >> t_{stress1}$, is given in Figure 1.65-right. After each stress, the V_{TH} measurement is possible at $t_{extract}$. By assuming that $t_{extract} > t_{response}$, an unavoidable error should appear between the real and the measured drift. In order to graphically compare them, the measurement points obtained at $t_{extract}$ were plotted as a function of the stress times $t_{stress1}$ and $t_{stress2}$, showing a difference between the real and the measured ΔV_{TH}. In this example, the error was chosen arbitrarily. Indeed, this error cannot be estimated experimentally, leaving an unknown number of undetected defects outside the measurement window [137].

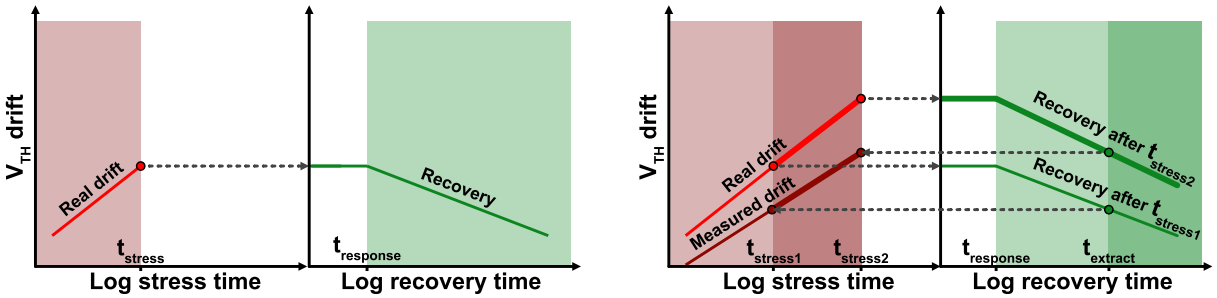

Figure 1.65. Left - Schematic representation of the recovery occurring just after a gate voltage. **Right -** Illustration of the error that may be induced between the real and measured ΔV_{TH}, due to the delay of V_{TH} measurement just after the stress [137].

Finally, those fundamental drawbacks are significantly amplified when the effect of temperature is considered. Note that temperature-accelerated tests are often performed in order to extract lifetime estimations [142], [318]. Figure 1.66 shows the influence of elevated temperature on BTI transients. By assuming that the charge trapping is thermally activated, the threshold voltage drift is higher at high temperature compared to a V_{TH} drift extracted at lower temperature (blue). After a certain stress time, charge emission towards the semiconductor starts to appear. As the temperature is still elevated, the detrapping process is also thermally activated, resulting in a faster charge emission, which results in a steeper ΔV_{TH} slope during recovery. Considering that $t_{extract}$ does not vary with temperature, the underestimation of real ΔV_{TH} is amplified due to the thermal activation of trapping and detrapping processes. Although the example given in Figure 1.66, still describes a realistic scenario that must be considered [137].

1.4.3.3 Single defects characterization in small gates

Although that the following measurement techniques, similar to BTI degradation, have not been used for this work, they give an interesting overview of a single defect behavior. They experimentally demonstrate that the isolated gate oxide defects can be compared to a quantum well

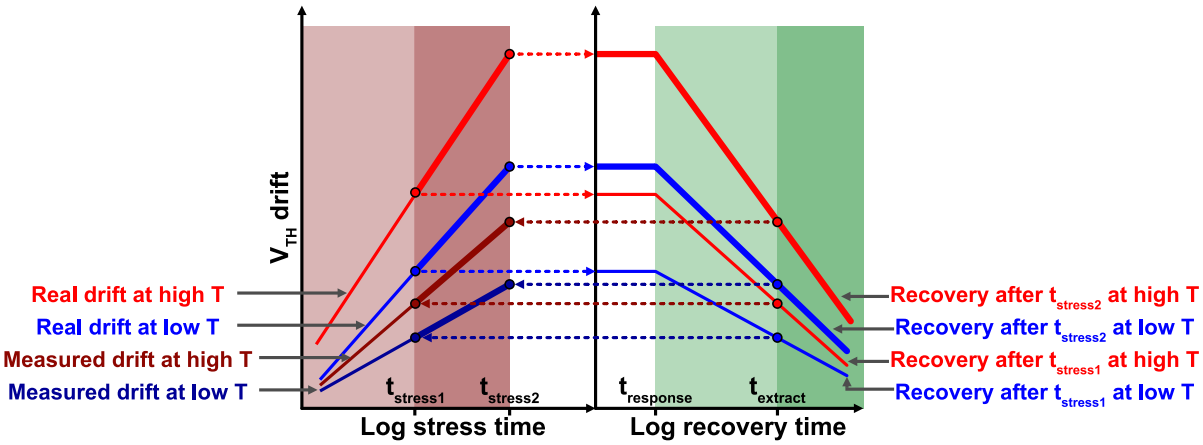

Figure 1.66. Illustration of the likely amplification of the difference between the real and measured ΔV_{TH} at high temperature, induced by the thermal activation of charge trapping and detrapping [137].

with one or several energy states. The charges in the channel can be found at these unwanted energies levels (trapping), with a probability to go back in channel (detrapping) [150], [298].

1.4.3.3.1 Random Telegraph Noise

In the case of large area devices, BTI measurements result in the response of a large set of defects at the same time. Therefore, it is very difficult to isolate the electrostatic impact of a single gate oxide defects. In contrast, the continuous reduction of the device size enables to isolate the charge trapping and detrapping events of a single defect. This phenomenon was first observed as Random Telegraph Noise in the 1980s [319]–[321], and the signal measurement consists in the application of different gate voltages in the linear regime of the device, while continuously recording the resulting drain current. The resulting drain current fluctuations can be described by step functions, where each step corresponds to the different state level occupancy of a unique gate oxide defect. If desired, these drain current fluctuations can be correlated with the V_{TH} shifts.

Since the first RTN observations in the 80s, different types of complex RTN signals have been reported and attributed to a single defect with several state levels. These complex transients are also called "anomalous RTN" signals, and consists in regular RTN signals with two or three levels interrupted by inactive phases. In literature, these latter transients have been described by a defect model including three energy levels among which one is metastable [321]. Later, this three-states model became the basis of Non-Radiative Multi-Phonon (NRMP) models with metastable states, thus enabling to describe BTI degradation [322], [323]. Another phenomenon called "temporary RTN" has been also identified, where the signal does not reappear again in contrast to anomalous RTN [323]. Figure 1.67 gives an example of two state defect configurations providing simulated anomalous and temporary RTN signals.

There are several obstacles to carrying out RTN measurements on GaN/AlGaN hetero-structures. Indeed, the fabrication processes usually do not allow to produce devices down to the required size. In the case of MIS-HEMT, the presence of the AlGaN barrier layer additionally reduces the expected drain current fluctuations of the individual defects, which deteriorates the signal

to noise ratio (SNR) , and then the RTN measurements. In addition, the gate voltage range allowing to obtain a drain current also induces the activation a large number of gate oxide defects implying BTI drift phenomenon, and thus a deteriorated RTN signal. However, the possibility to carry out RTN measurements at very low temperature on GaN-based devices can be considered. Indeed, a low temperature condition would lead to a SNR increase due to the reduction of the thermal noise level, and would also imply a reduction of active defects. The idea of this RTN experiment at low temperature, can be compared to RTN measurements in Si technologies where high temperatures and voltages are used to generate more defect responses [150], [323].

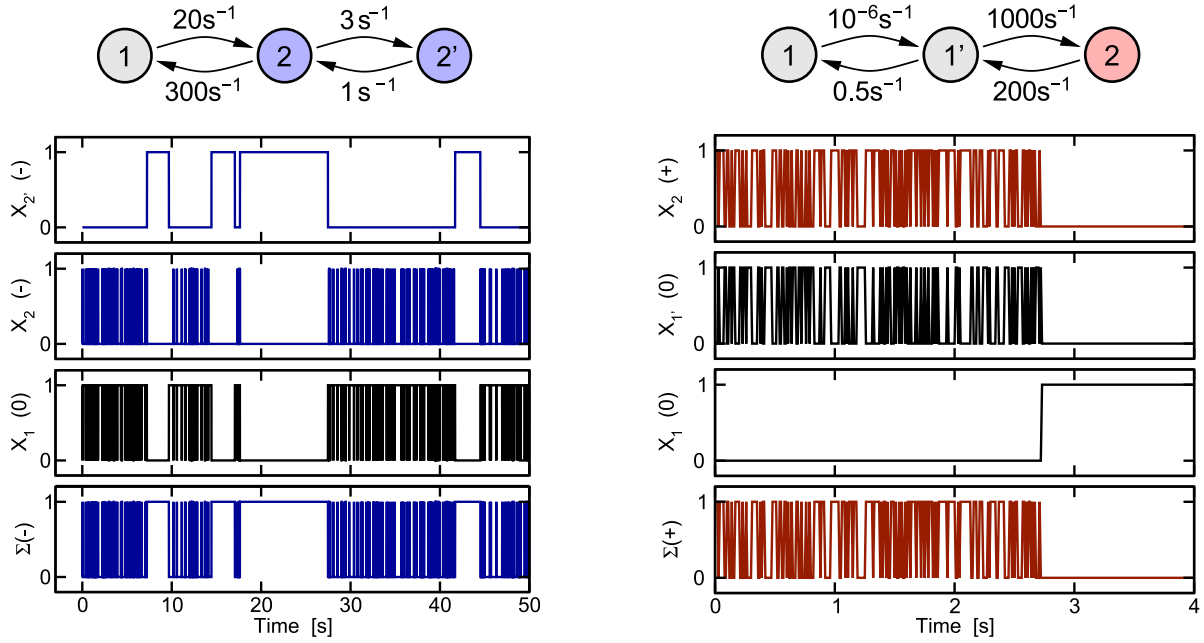

Figure 1.67. Simulated RTN signal of defects producing anomalous RTN (**left**) and temporary RTN (**right**), which are both represented with a three-state defect including one metastable state, as shown in schematics at the top. Both configurations differ in their charge states which can either be neutral (grey), positive (red), or negative (blue). Traces X_i and $X_{i'}$ exhibit the occupancies of each state i (such as $i = 1$ or 2 here), as well as their resulting RTN signal (bottom row) which is the sum of all traces [323].

1.4.3.3.2 Time Dependent Defect Spectroscopy

Time-dependent defect spectroscopy (TDDS) was derived from DLTS measurement principle, itself extended to single defects in 1988 [324]. TDDS measurements are very similar to the MSM BTI measurement, since the V_{TH} shift recording occurs during both stress and recovery phases. The difference between both measurements lies in the gate oxide traps density, and hence in the obtained ΔV_{TH} transient. Indeed, the BTI measurements are described by continuous V_{TH} transients due to the large number of activated traps within the gate oxide. Conversely, in the frame of TDDS measurements, the traps are so few that discrete V_{TH} shifts are observed and are ascribed to the traps state modifications. V_{TH} step heights enable to characterize the trap by extracting their capture and emission time constants (τ_c and τ_e) as well as their activation

energies (E_a).

To do this, a large number of measurements are carried out on a single transistor in order to obtain statistical measurements. The ΔV_{TH} step heights measured during the stress or recovery phases are plotted as a function of the corresponding time constant, as shown in Figure 1.68-left. In the upper graph, two relaxation measurements have been carried out on the same device, after two stress phases. In the lower Figure, the values of the ΔV_{TH} step heights are plotted as a function of their emission times, giving a "spectral map". These measurements show the stochastic aspect of the trap time constants. Indeed, although the V_{TH} offset value caused by a single trap is unique, the emission time is random. In order to obtain the characteristic constants time, it is therefore mandatory to repeat these trapping and detrapping operations several times on the same device, in order to establish reliable measurements.

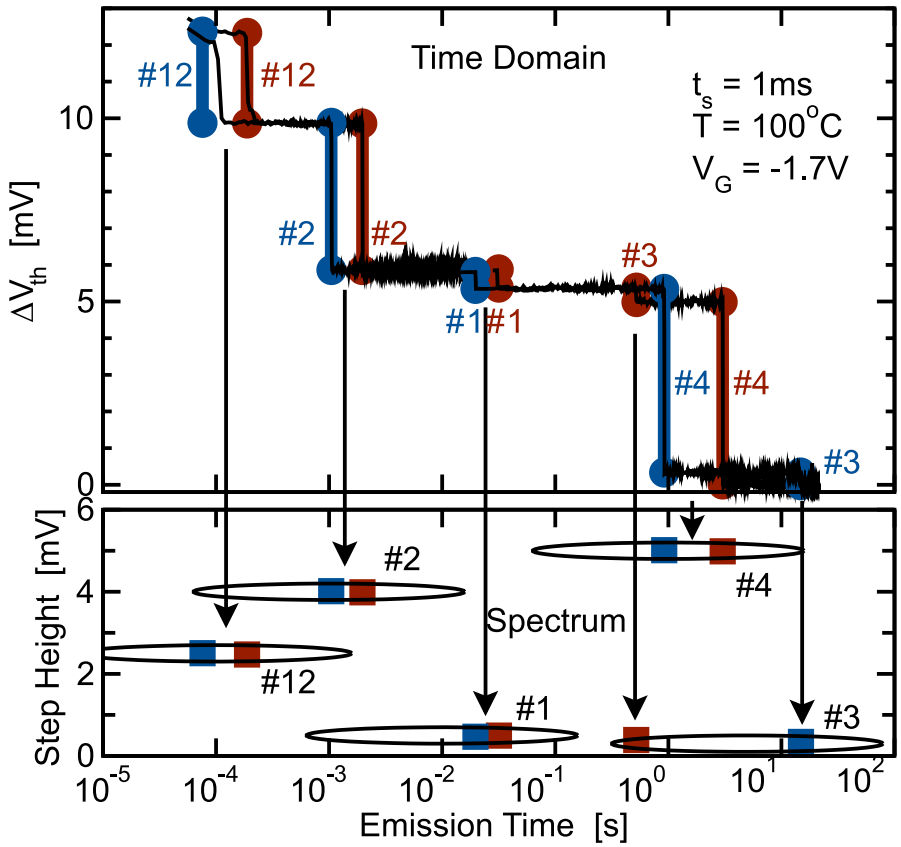

Figure 1.68. Two ΔV_{TH} recovery transients measured on the same device with the same stress conditions (**top**). Plot of the step-heights as a function of the corresponding emission times (**bottom**) [325], [326].

Two experimental spectral maps extracted at two different temperatures (100°C and 150°C) are shown in Figure 1.69-left (and middle), resulting from the one hundred ΔV_{TH} stress and recovery transients. The same trap population can be found on both maps. However, their corresponding emission time constants decrease with temperature as shown in Figure 1.69-right, demonstrating the thermal activation of the traps behavior. These temperature-dependent measurements also enable to extract the activation energies of each trap populations in order to identify their nature.

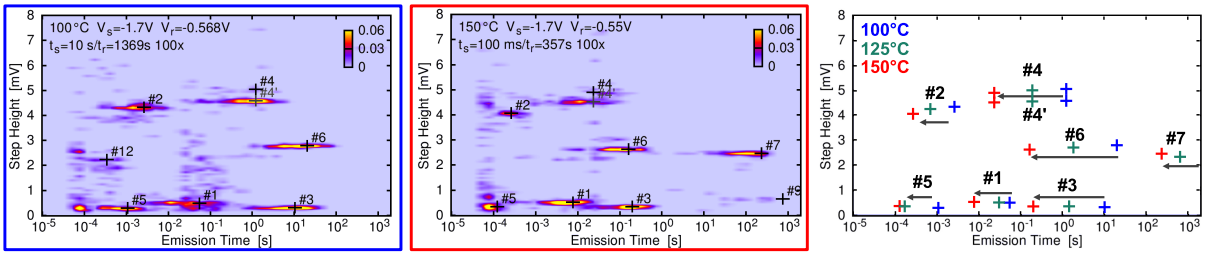

Figure 1.69. Experimental spectral maps extracted at two different temperatures, 100°C (**left**) and 150°C (**middle**), respectively 1.69. Trap population position as a function of temperature is plotted in the right graph, showing the trap dependency on temperature [325], [326].

Conclusion

In this chapter, we have shown the important growth of the power electronics market due to the development for greener energy conversion. Si-based technologies, which are mainly used in power electronics nowadays, have limitations with the emergence of these new demands in terms of operating frequency, power and efficiency. Indeed, the silicon intrinsic properties are incompatible for certain applications in terms of breakdown voltage, On-state resistance, and thermal conductivity. In order to address these new demands, the power electronics industry started to develop power devices based on wide band gap semiconductors, such as gallium nitride (GaN).

The GaN properties have been thoroughly presented in the second section. It has been shown how this material is extremely interesting for medium power and high frequency applications. Its wide band gap gives rise to a high breakdown voltage, which is very interesting for high voltage applications. Moreover, the intrinsic positive polarization charge at AlGaN/GaN interface gives rise to a bi-dimensional electron gas (2DEG) with a very high charge density, a high mobility and a high saturation velocity favorable for high current applications as well as the development of high frequency switching technologies. The combination of these properties adapted to high voltage and high current applications, makes GaN a very suitable material for the development of power applications.

Due to the high cost and the low availability of native GaN substrates, GaN-based devices are mostly fabricated on foreign substrates such as Si, SiC or sapphire which lead to mechanical stress and high dislocation densities. These latter lead to reliability issues and complicate the devices development, slowing down their commercialization. Several GaN-based device architectures can be found in literature for power diodes and transistors. Regarding diodes, lateral and vertical architectures have been proposed. Lateral Schottky Barrier diode is based on AlGaN/GaN hetero-junction, and use the 2DEG as a highly conductive channel during On-state. The optimized SBD architecture developed in CEA-LETI, recently demonstrated very interesting performances which are at the state of the art of GaN-based lateral diodes, and suitable for mass production. More recently, the vertical diode architecture demonstrates the possibility to achieve higher breakdown voltages and higher integration densities compared to lateral Schottky diodes. However, they need to be integrated on native GaN substrates, which makes them more expensive. Concerning HEMT architecture, several architectures have been proposed in the case of the E-mode, while the MIS-HEMT configuration remains the most suitable architecture for the D-mode. The cascode technology, the vertical HEMT, the pGaN gate HEMT, the flurorine-based gate HEMT as well as the MOS Channel HEMT each have their own technological challenges to address the medium power market.

Nowadays, reliability issues of AlGaN/GaN-based HEMTs is a major concern for mass market production. Indeed, several types of instability have been reported in these devices, such as Current Collapse, TDDB, or BTI. These issues are explained by several physical underlying mechanisms. However, they are often associated with the presence of defects within the device structure. It is also the case in BTI degradation. This latter phenomenon is one of the most critical reliability issues nowadays, as it degrades electrical performances and device lifetime through V_{TH} instabilities occurring during device operation. This appears when a MIS or MOS gate is integrated in a transistor, and can be found in memory, CMOS as well as in power technologies notably. In GaN-based devices, V_{TH} instabilities are known to be one of the biggest

reliability issues.

The aim of this work is to provide a better understanding of the underlying physical mechanisms leading to BTI degradations in the GaN-on-Si E-mode MOSc-HEMT developed in CEA-LETI. In the following chapter, we will demonstrate the influence of traps within the gate oxide as well as the epitaxial structure on V_{TH} instabilities, by applying both negative and positive gate voltage stress.

2

Identification of traps involved in BTI degradation

This chapter is dedicated to traps identification involved in both nBTI and pBTI degradations. At first, a BTI literature overview is provided on studies carried out on MOSc-HEMT and MIS-HEMT architecture. The second part is dedicated to nBTI where the stress transients present two strong ΔV_{TH} decreases revealing two time constants. An in-depth investigation of this peculiar behavior is presented in this section. Finally, the third section presents a thorough analysis of the pBTI transients. Temperature dependent measurements at various positive gate voltage stress reveal interesting conclusions which improved our understanding on pBTI degradation.

Contents

2.1 BTI literature overview on GaN-based transistors

One of the main challenges of GaN-based HEMT is the threshold voltage V_{TH} stability during operation, which is now a major concern to increase the device operation lifetime. This reliability issue concerns D-mode [137], [144], [327], [328] as well as E-mode transistors. Indeed, several negative and positive BTI studies on E-mode MIS gate HEMT [276], [329], pGaN gate HEMT [330], [331], or MOSc-HEMT [300], [302], [332], [333] architectures reported V_{TH} instabilities, and demonstrated degradation of the dynamic performance of transistors during operation. Therefore, it is crucial to improve the understanding of the physical mechanisms involved in negative and positive BTI degradation in GaN-based HEMT. As mentioned in section 1.3.3.2, BTI degradation is a major concern in MIS-HEMT architectures, consequently the physical mechanisms involved in BTI degradation on this transistor are probably the most studied and understood among the different GaN-based architectures [137], [144], [327], [328]. Conversely, few studies have been reported on V_{TH} instabilities in GaN-based MOS-HEMT architecture [300], [302], [329], [332], [333]. Since this thesis is dedicated to BTI degradation study on a GaN-on-Si E-mode MOSc-HEMT architecture, and that V_{TH} instabilities have been thoroughly studied in MIS-HEMT architecture, a literature overview of nBTI and pBTI degradations reported on both technologies is provided in this section.

2.1.1 Negative Bias Temperature Instability degradation

2.1.1.1 MIS-HEMT achitecture

As mentioned in section 1.4.3.1, BTI degradation is related to electrons trapping in preexisting gate oxide defects. This induces a local electrostatic modification at gate oxide interface, and then a V_{TH} variation. The sign of V_{TH} drift lies in trapped charge type. Considering that the 2DEG forms the channel of a MIS-HEMT architecture, this latter is more subject to pBTI degradation. However, Matteo Meneghini *et al.* reported nBTI degradation on MIS-HEMT architecture [299] whose paper will be presented in the following section. Note that this paper is one of the few studies addressing nBTI degradation on the MIS-HEMT architecture.

2.1.1.1.1 Device structure and experimental setup

The study reported by Matteo Meneghini *et al.* was carried out on a D-mode HEMT integrating a MIS gate, and which has been fabricated on an 8" Si substrate as illustrated in Figure 2.1. The epitaxial structure is composed of a 200nm-thick AlN nucleation layer, followed by a 2.3µm-thick AlGaN buffer layer and 150nm-thick GaN channel. Thereafter, a 15nm-thick AlGaN barrier is deposited, followed by a GaN cap and a SiN passivation layer using RTCVD (Rapid Thermal Chemical Vapor Deposition). The gate is made of a 3.7nm-thick AlGaN barrier layer and 15nm-thick SiN gate dielectric. Regarding the device layout, the gate width is $W_G = 0.1$ mm while the length is $L_G = 0.6$ µm. Finally, the spacing between the gate to drain and gate to source is 0.75µm [299] .

Concerning the experimental setup, the negative V_{TH} shift is induced by applying a gate voltage stress $V_{GStress} = -10$ V during $5 \cdot 10^3$s. During the stress phase, $I_D(V_G)$ measurements are periodically performed, enabling the evaluation of the V_{TH} variation during the stress, as shown in Figure 1.64. Just after the stress phase, the recovery phase is immediately ($\sim 50 - 500$ ms)

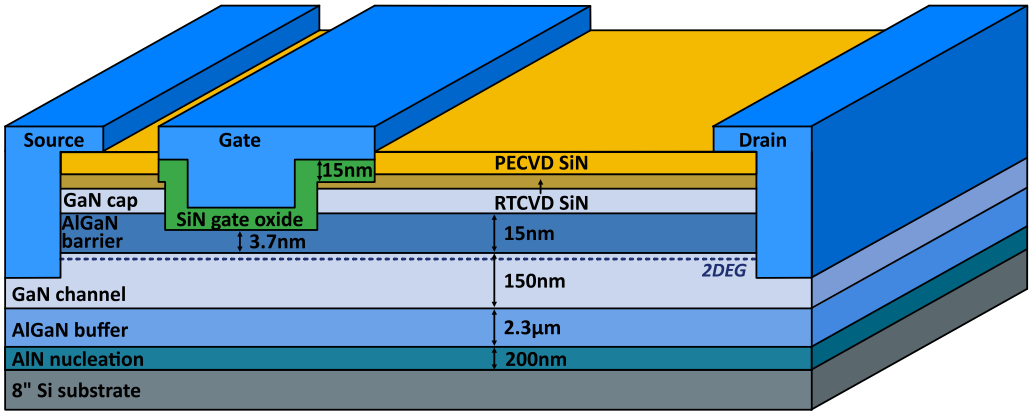

Figure 2.1. Representation of the tested transistor used for nBTI study [299], [306].

recorded. It consists in fixing the gate voltage stress at 0V, and still monitoring the V_{TH} drift during $5 \cdot 10^3$s (Figure 1.64). Note that the drain voltage is set to 0.5V during $I_D(V_G)$ measurements, while it is grounded when the constant gate voltage is applied. $I_D(V_G)$ records dedicated are carried out in the range $-6\ V < V_G < 0\ V$, with a duration measurement between $50 - 500$ms.

2.1.1.1.2 Experimental nBTI results

$I_D(V_G)$ characteristics measured at different times of a negative $V_{GStress}$ of -10V during $5 \cdot 10^3$s and at a temperature of 90°C, are presented in Figure 2.2-left. A negative shift of the $I_D(V_G)$ characteristics without significant sub-threshold slope degradation is shown. $I_D(V_G)$ characteristics measured during the recovery phase are presented in Figure 2.2-right. It can be observed that when the device is grounded, the threshold voltage exhibits a slow and partial recovery after the relaxation phase.

Stress and recovery nBTI transients extracted from results presented in Figure 2.2, are depicted in Figure 2.3. It shows that the stress nBTI transient starts to decrease monotonously after a 10s stress, and reaches a ΔV_{TH} drift of 3.2V after a stress time of $5 \cdot 10^3$s. This behavior can be described by a broad range of time constants corresponding to an energy states continuum related to a defect band probably located at SiN/AlGaN interface here. On the other hand and as mentioned previously, nBTI recovery transient rises slowly without reaching a full recovery, but a ΔV_{TH} value of 1.12V. Since the ΔV_{TH} increases monotonously and do not reach a plateau through the recovery phase, it is difficult to attribute the ΔV_{TH} drift to a permanent degradation here.

A temperature dependent analysis has been also carried out as shown in Figure 2.4-left. It presents stress and recovery nBTI transients obtained by applying a negative gate stress at various temperatures from 30°C to 150°C. At 30 and 60°C, it can be noticed that the nBTI degradation starts after 100s of stress and reaches a $|\Delta V_{TH}|$ value of 0.5V and 1.5V after $5 \cdot 10^3$s of stress, respectively. A $|\Delta V_{TH}|$ plateau is also observed on nBTI recovery transients, suggesting a permanent degradation at low temperature. At high temperature, Figure 2.4-left depicts that nBTI degradation is significantly activated with temperatures, and can reach a $|\Delta V_{TH}|$ of 4V after a gate stress of $5 \cdot 10^3$s at 150°C. It can be also observed that at high temperature, $|\Delta V_{TH}|$

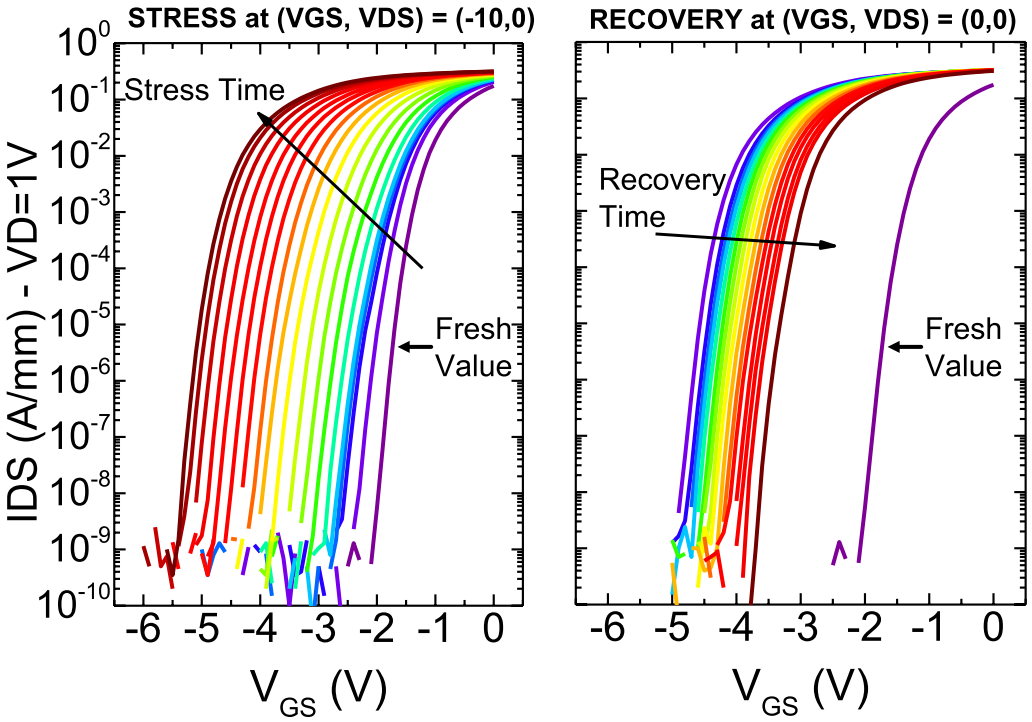

Figure 2.2. **Left -** $I_D(V_G)$ characteristics measured during the stress phase where $V_{GStress} = -10$ V during $5 \cdot 10^3$s at T = 90 °C. **Left -** $I_D(V_G)$ characteristics measured during the recovery phase where the $V_{GStress} = 0$ V during $5 \cdot 10^3$s at T = 90 °C [299], [306].

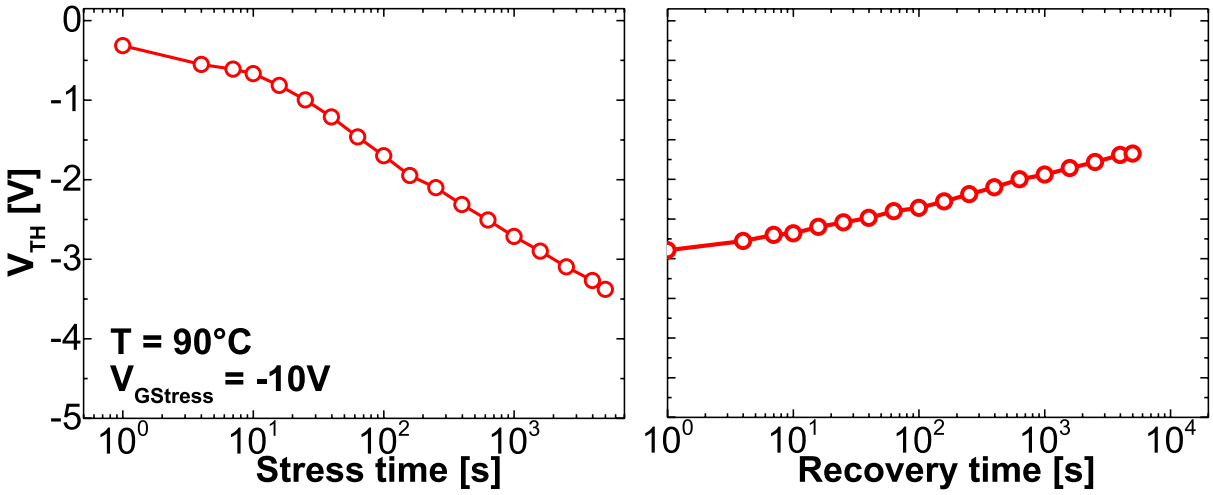

Figure 2.3. Stress and recovery nBTI transients obtained by applying a negative gate stress of $V_{GStress} = -10$ V during $5 \cdot 10^3$s and at a temperature of T = 90 °C [299], [306].

increases during the recovery phase, which is not the case when temperatures are below 60°C.

It has been found that the V_{TH} drift during stress follows a stretched exponential proportional to $\exp(-t_{stress}/\tau)^{\beta_i}$, where β_i is an ideality factor. The coefficient β_i quantifies the stretch of the exponential function with respect to the ideal behavior, defined by $\beta_i = 1$. Moreover, as the V_{TH} drift shift is found to be partly recoverable at temperatures above 90°C, the latter is reproduced by a model having a logarithmic dependence with recovery time It is shown in Figure 2.4-left, that these models reproduce relatively well the stress and recovery nBTI transient obtained at a temperature of 90°C. The time constants τ extracted from the model reproducing the stress nBTI transients at different temperatures are then reported in an Arrhenius plot, as shown in Figure 2.4-right. The extracted activation energy is about 0.37eV.

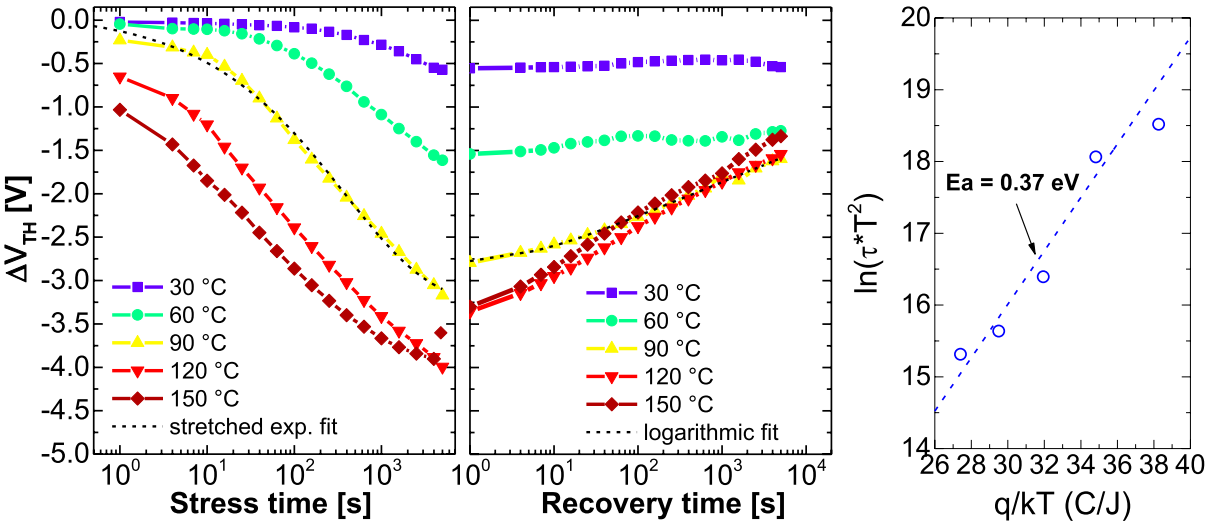

Figure 2.4. Left - Stress and recovery nBTI transients obtained by applying a $V_{GStress}$ of -10V during $5 \cdot 10^3$s and at temperatures from 30 to 150°C. **Right -** Arrhenius plot of the time constant τ related to the process inducing a negative V_{TH} shift during stress. An activation energy of 0.37eV is extracted here [299], [306].

2.1.1.1.3 Results interpretation

Based on the experimental results presented previously, the negative V_{TH} shift is schematically illustrated in Figure 2.5. According to M. Meneghini *et al.*, the V_{TH} drift could be due to trap states within the SiN bulk, at the SiN/AlGaN interface, in the AlGaN barrier, or at the AlGaN/GaN interface. They consider that the low gate voltage stress values used to obtained previous results are not sufficient to activate trap states located in the epitaxial structure. Moreover, AlGaN/GaN interface is not supposed to significantly contribute to V_{TH} drift. Consequently, it is supposed that nBTI is due to a defect distribution at the SiN/AlGaN interface and/or in the SiN layer. Considering these assumptions, at equilibrium state the traps within the defects band are negatively charged if they are below the Fermi level while they are neutral when they are located above, as illustrated in Figure 2.5-left. When a negative gate voltage stress is applied, these trap states are depleted either via tunneling conduction through the 3.7nm AlGaN barrier or via trap-assisted conduction such as Hopping, Poole-Frenkel or Trap Assisted Tunneling (TAT) mechanisms for example (Figure 2.5-center). According to M. Meneghini *et al.*, the

barrier-limited conduction and the broad energy level distribution leads to stretched exponential kinetics rather than in a purely exponential behavior. The charge state modification of traps results in a net positive charge, leading to a threshold voltage shift towards negative values. During the recovery phase, the defects drop below the Fermi level, and are subject to trap electrons. However, this trapping process is slow because the electrons are supplied by the channel and/or the metal (Figure 2.5-right). Hence, they must reach the trap states by defect-assisted conduction through the AlGaN barrier or the SiN dielectric, respectively. The recovery process is self-limited due to the repulsive influence of electrons that have already reached the traps. The electron trapping during the recovery also limits the available state amount. These are the reasons why the recovery is explained by a logarithmic dependence according to M. Meneghini *et al.* [299], [306].

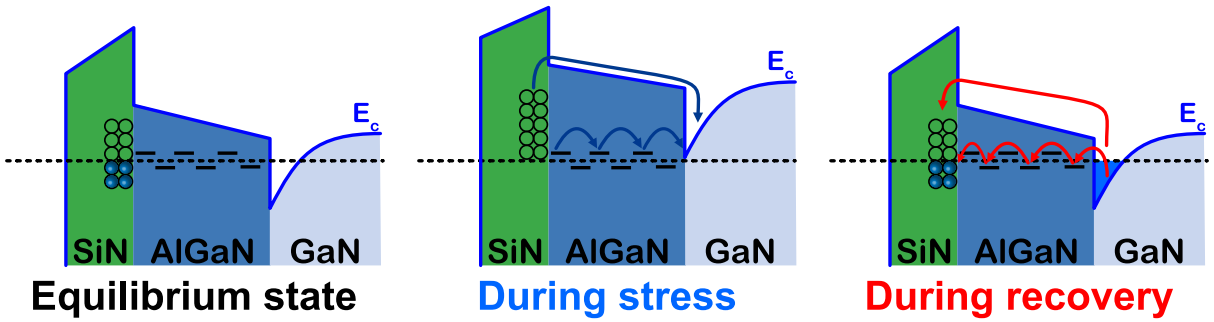

Figure 2.5. Left - Illustration of the gate stack band diagram at equilibrium state, where the defects are negatively charged if they are below the Fermi level while they are neutral when they are located above. **Center -** Conduction band representation of the gate stack showing the defects depletion during the negative gate voltage stress inducing a negative ΔV_{TH}. **Right -** Band diagram schematic exhibiting the trapping during the recovery, thus leading to a positive ΔV_{TH} [299], [306].

2.1.1.2 Fully recessed MOS gate HEMT architecture

Before studying nBTI degradation on E-mode GaN-on-Si MOSc-HEMT architecture during this thesis, A. Guo and J. A. del Alamo were the first to have investigated this topic [300], [302].

2.1.1.2.1 Device structure and experimental setup

A. Guo and J. A. del Alamo worked on the HEMT illustrated in Figure 2.6-left, where the AlGaN/GaN is fully recessed in order to embed the MOS gate. The gate oxide layers are then deposited in the etched cavity, and consists in 40nm-thick bi-layer composed of SiO_2/Al_2O_3 where Al_2O_3 is next to the GaN channel. Note that both oxide layers are relatively thick here. Regarding the design, the gate is 100µm wide while the gate length is 1µm. Electrical device properties are provided in Figure 2.6-left by showing the $I_D(V_G)$ and transconductance characteristics measured on a pristine device at $V_D = 0.1$ V in the linear regime. The V_{TH} is at 0.34V here, while the sub-threshold swing SS and the maximum trans-conductance $g_{m,max}$ are at 148mV/decade and 0.91mS/mm, respectively [302].

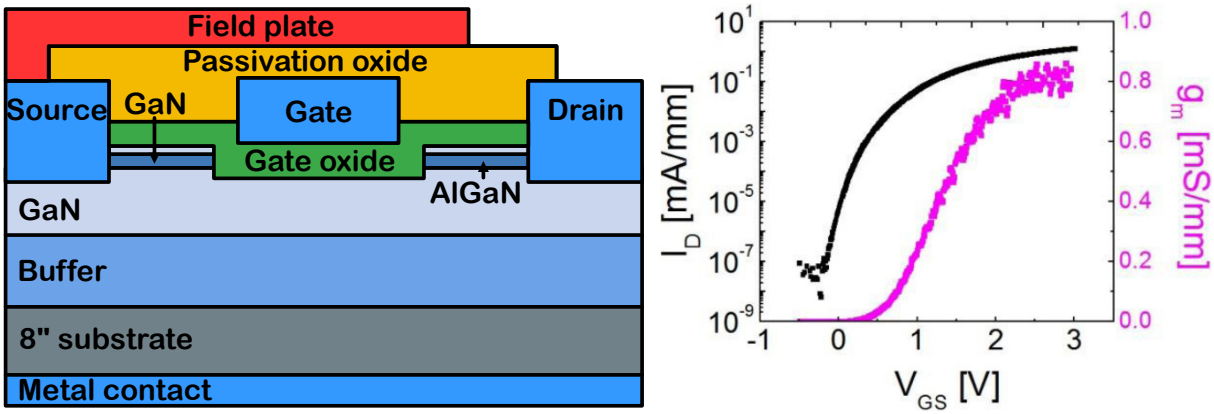

Figure 2.6. Left - GaN-on-Si MOS-HEMT representation used for nBTI study, where the gate oxide is composed of a SiO_2/Al_2O_3 bi-layer. The gate is 100µm wide while the gate length is 1µm. **Right -** $I_D(V_G)$ and transconductance characteristics measured on a pristine device at $V_D = 0.1$ V. The V_{TH} is at 0.34V, while SS and $g_{m,max}$ are at 148mV/decade and 0.91mS/mm, respectively [302].

The experimental setup is similar to the one presented in section 2.1.1.1.2, and consists in a stress phase and a recovery phase. During the stress phase, the device is subject to a constant DC gate voltage stress ($V_{GStress} \neq 0$ V), while the drain, the source, and the substrate are grounded. The constant gate stress is periodically interrupted to perform $I_D(V_G)$ measurements to monitor the ΔV_{TH}. Note that each $I_D(V_G)$ record is about $1-2$s long, i.e the constant gate stress is then interrupted during this measurement period. Just after the stress phase, the recovery phase is triggered and consists in setting $V_{GStress}$ to the ground, and monitor the V_{TH} drift. In this study both stress and recovery phases are 10^3s long [302].

2.1.1.2.2 Experimental nBTI results

Stress and recovery nBTI transients obtained by applying different negative gate voltage stress from -1 to -5V at room temperature, are presented in Figure 2.7. It exhibits that nBTI degradation starts to occur around 10s independently from the gate voltage value. However, the $|V_{TH}|$ drift dynamic rises as $|V_{GStress}|$ increases. It can be also noticed that when a $V_{GStress}$ of -4 and -5V are applied a ΔV_{TH} saturation appeared from 10^2s to 10^3s of stress. At $V_{GStress} = -5$ V, an increase of ΔV_{TH} after the saturation can be observed. According to A. Guo and J. A. del Alamo, this behavior is related to a second degradation regime leading to a ΔV_{TH} turnaround for long stress times, and which is attributed to GaN substrate trapping [300]. This latter will be developed in section 2.1.1.2.3. Regarding recovery phase, nBTI transients increase monotonously and reached a total recovery after more than $1 \cdot 10^3$s of relaxation. As mentioned in the previous section, this behavior can be described by a broad range of time constants corresponding to an energy state continuum related to a defect band, probably located in Al_2O_3, close to the gate oxide interface [302].

Temperature dependent analysis at a fixed $V_{GStress}$ of -2V has been also carried out as depicted in Figure 2.8. It presents stress and recovery nBTI transients obtained at temperatures from $-40°$C to 40°C. It can be noticed that ΔV_{TH} transients exhibit a strong dependence with temperature during stress phase, while this dependence is weaker during recovery phase. An

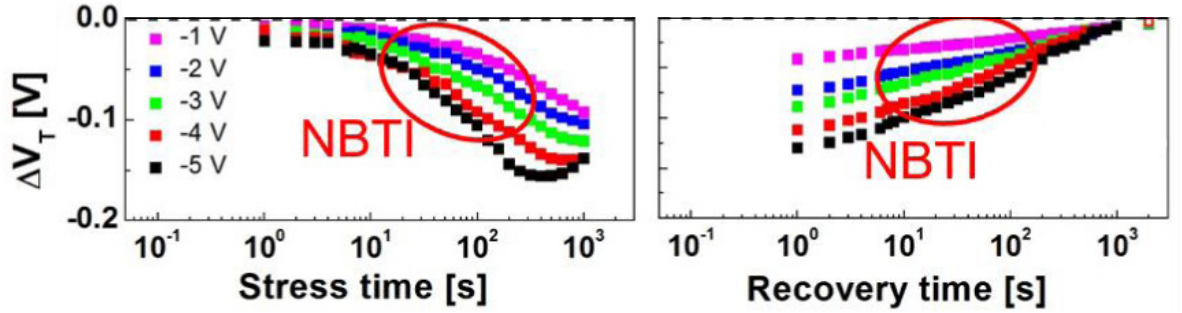

Figure 2.7. Stress and recovery nBTI transients obtained by applying different gate voltage stresses from -1 to -5V during 10^3s at room temperature [302].

Arrhenius analysis was also carried out using these latter results as shown in Figure 2.9. Stress times reported in these plots correspond to the time when ΔV_{TH} reach a value of -0.018V. The activation energy related to nBTI degradation is $E_a = 0.37$ eV showing a strong temperature dependence. Although that both gate stacks are not comparable, it can be noticed that this activation energy is surprisingly identical to the one found in the study of Meneghini *et al.* on MIS-HEMT architecture (Figure 2.4).

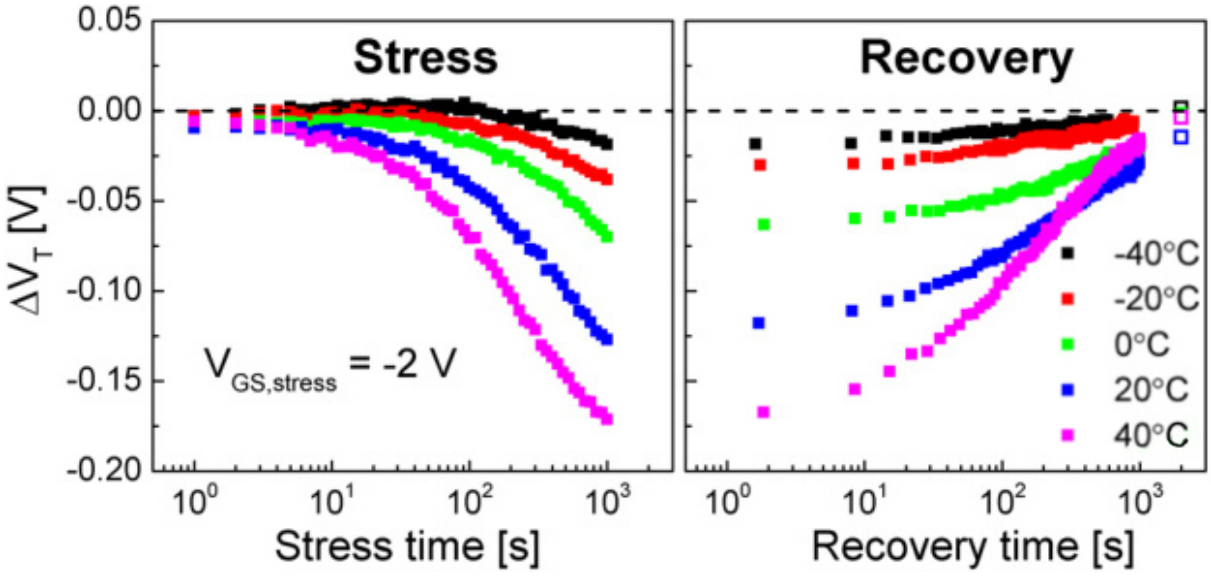

Figure 2.8. Stress and recovery nBTI transients obtained at temperatures from -40 to 40°C at $V_{GStress} = -2$ V [302].

Arrhenius analysis on recovery nBTI transients was also carried out, by extracting the recovery time needed for a 50% ΔV_{TH} recovery. An activation energy of $E_a \approx 0.056$ eV is extracted exhibiting a weak temperature dependence of ΔV_{TH} recovery, compared to stress phase.

2.1.1.2.3 Results interpretation

According to A. Guo and J. A. del Alamo, all these previous observations suggest a distribution of preexisting oxide traps in Al_2O_3, close to gate oxide interface. At equilibrium state, this

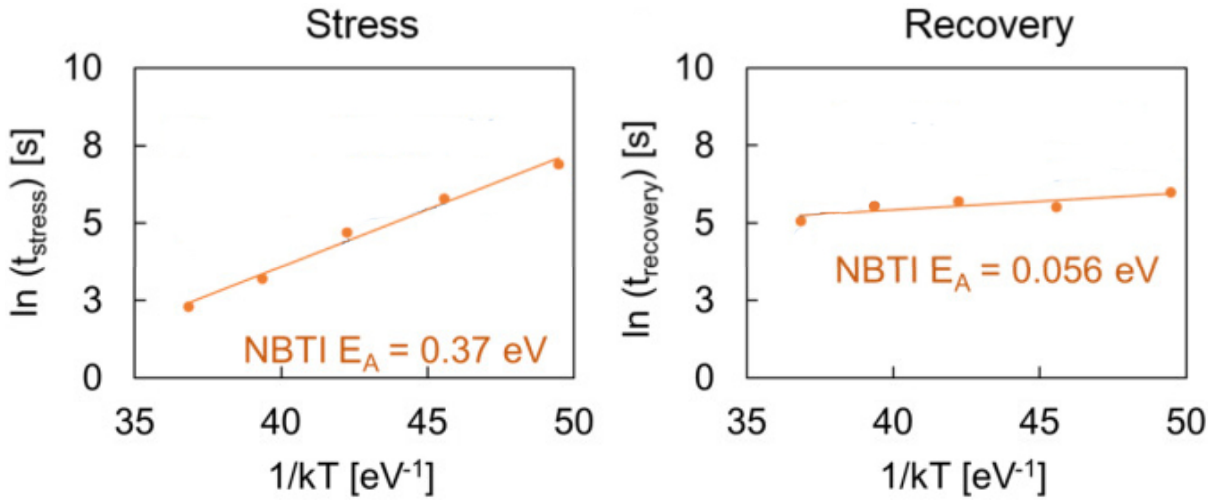

Figure 2.9. Arrhenius plot of stress and recovery nBTI transients obtained by applying a negative gate voltage stress of −2V [302].

defect band spans from below the Fermi level to above the GaN conduction band minimum, as illustrated in 2.10-left. If the traps are above the Fermi level, they are neutral while they are negatively charged whether they are located below. During negative gate voltage stress, trapped electrons are depleted and must overcome an energy barrier before they can be released into the GaN conduction band, resulting in an observed higher apparent activation energy (Figure 2.10-center), as well as a V_{TH} decrease. During recovery, trap states below the Fermi level are available within the oxide defect band. Hence channel electrons tunnel into them, which is also consistent with the low apparent activation energy (Figure 2.10-right). It automatically leads to a V_{TH} increase.

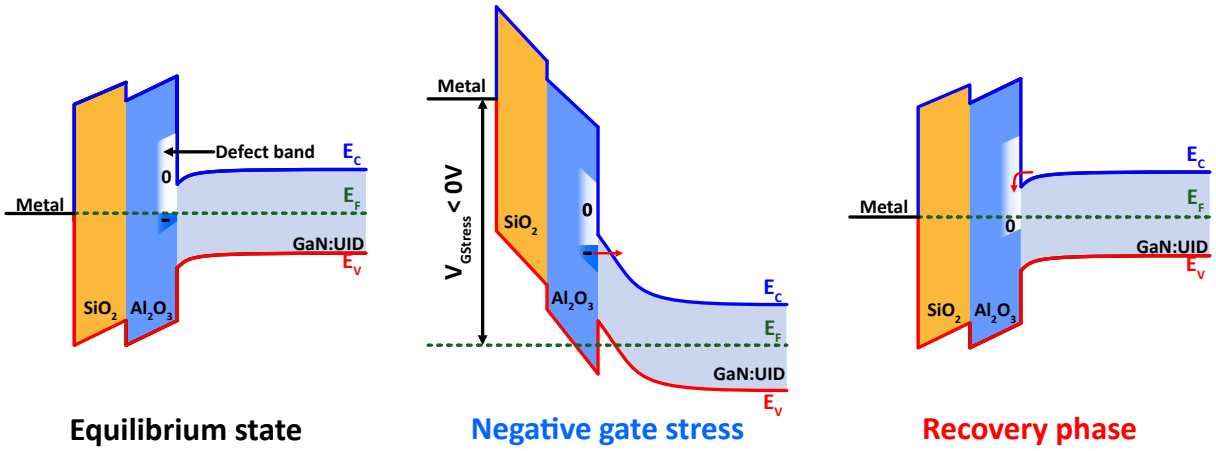

Figure 2.10. Left - At equilibrium state, the traps within the Al_2O_3 defects band are neutral if they are above the Fermi level while they are negatively charge when they are located below. **Center -** When a negative $V_{GStress}$ is applied, the trapped electrons are depleted and must overcome an energy barrier before they can be released into the GaN conduction band. It results in a V_{TH} decrease. **Right -** During recovery, the available trap states in the oxide defect band become occupied by the channel electrons that tunnel into them, leading to a V_{TH} increase [302].

When a negative gate voltage stress of −5V at 25°C is applied, a ΔV_{TH} increase around 10^3s of

stress is observed (Figure 2.7). According to A. Guo et J. A. del Alamo, this behavior is related to a second degradation regime leading to a ΔV_{TH} turnaround for long time of stress, attributed in to GaN substrate trapping. Indeed, an electron trapping in the GaN channel is suggested under reverse electric field where the electrons tunnel from the valence band to trap states in the GaN channel, in a process sometimes referred to as Zener trapping (Figure 2.11-a). According to this hypothesis, the high electron trapping lifts the bands in the GaN channel resulting in a V_{TH} increase (Figure 2.11-b). The threshold voltage instabilities are related to the gate corners here because is it assumed that the threshold voltage is determined by the gate corners potential in this study. After stress removal, electron detrapping takes place through thermal processes (Figure 2.11-c). According to A. Guo and J. A. del Alamo, this trapping process may be related to deep carbon traps with energy levels at 2.85eV from the GaN conduction band edge [300]. In the next section, we will see that this latter hypothesis is strongly relevant.

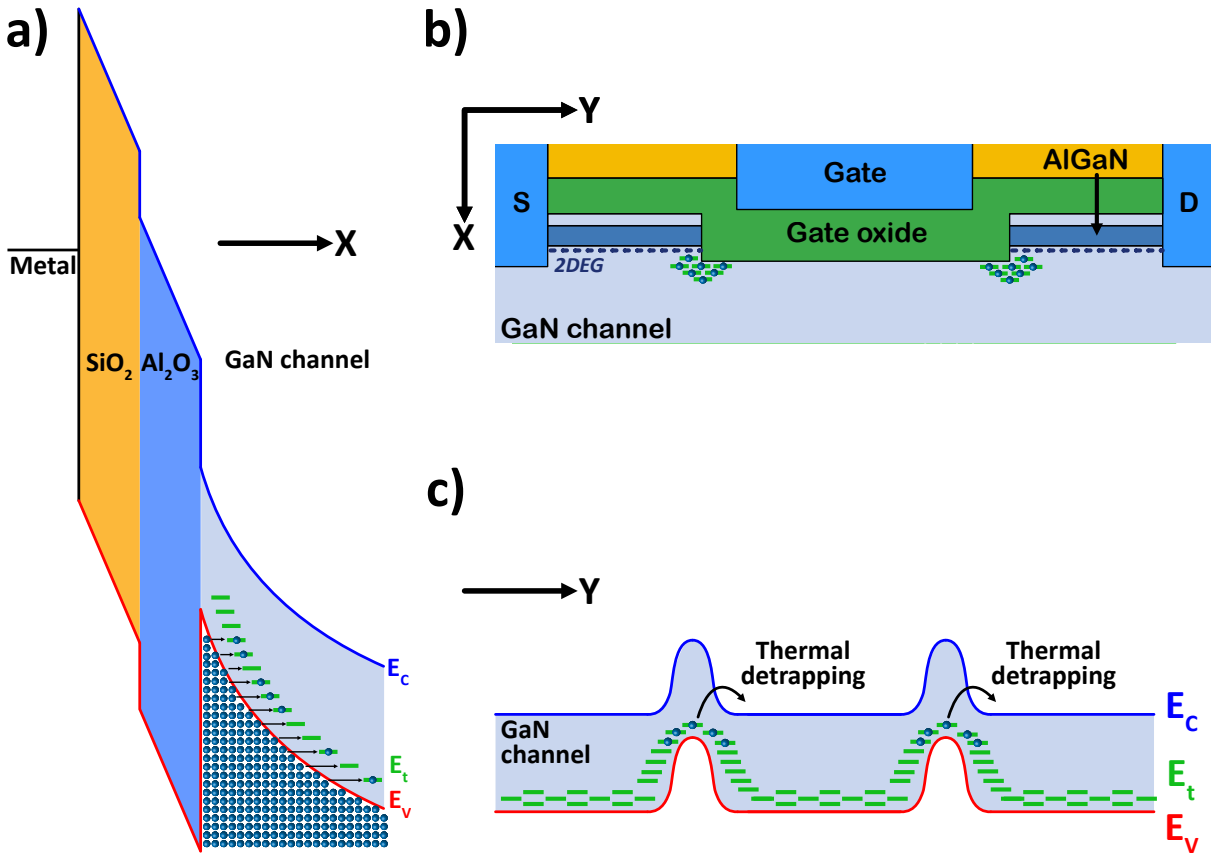

Figure 2.11. a - Illustration of the Zener trapping mechanism. Electrons from the valence band E_V transit towards trap states E_t in GaN under high electric field in the GaN channel, caused by a reverse gate stress. **b -** Electrons are trapped within the GaN channel near the gate corners. **c -** The high electron trapping raises the GaN conduction band energy at gate oxide interface, thus shifting threshold voltage towards positive values. During the recovery, electron detrapping occurs through thermal processes [300], [302].

2.1.2 Positive Bias Temperature Instability degradation

2.1.2.1 MIS-HEMT achitecture

Since the gate is dedicated to be submitted to a positive gate voltage during device operation, V_{TH} instabilities under positive gate stress have been studied more extensively than under negative gate stress in MIS-HEMT architectures. P. Lagger *et al.* have studied the physical mechanisms that explain the pBTI degradation in MIS-HEMT architectures. Indeed, they first presented a systematic approach to characterize the pBTI and understand underlying physical mechanisms behind this effect [144]. They then studied the dynamics of V_{TH} drifts at very short times by improving their experimental setup [143]. P. Lagger *et al.* also studied the influence of the gate dielectric nature on V_{TH} instabilities [327]. The complex dynamics of pBTI degradation was also studied at various gate voltage stresses, involving several types (Figure 1.31) of trap in the structure [141]. Finally, temperature influence was studied to investigate the trapping dynamics involved in pBTI degradation [142]. All these studies were reported by C. Ostermaier *et al.* in 2018, who reviewed the pBTI degradation in MIS-HEMT architectures [137]. In this section, a brief overview of V_{TH} instabilities reported at different gate voltages will be presented [144], providing a general understanding of pBTI degradation in MIS-HEMT architecture.

2.1.2.1.1 Device structure and experimental setup

The tested device was fabricated on 4"GaN-on-SiC substrates, where the 2DEG is created using a 25nm-thick $Al_{0.25}Ga_{0.75}N$ barrier directly grown on a GaN:UID channel. A 3nm-thick GaN cap is then grown on the AlGaN layer before the gate dielectric deposition. It corresponds to a 20nm-thick Al_2O_3 layer, deposited by ALD with an additional annealing at 650°C. Concerning the gate transistor layout, the gate length is 2µm while the gate width is 200µm. A representation of the gate stack is provided in Figure 2.12-left, with the corresponding band diagram in Figure 2.12-right.

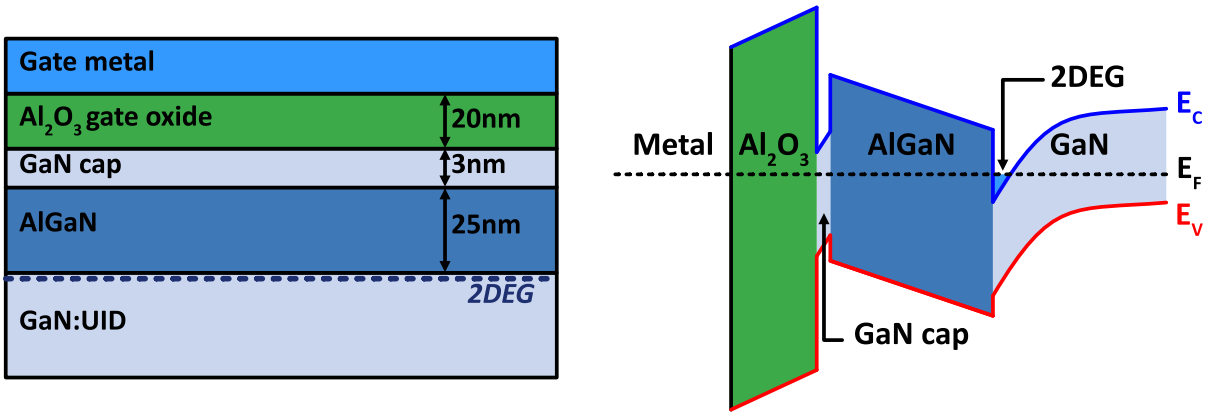

Figure 2.12. Left - Gate stack schematic of the tested MIS gate HEMT. **Right -** Band diagram illustration of the gate stack [144].

All measurements were performed on a Keithley SCS 4200, used to apply the chronogram illustrated in Figure 2.13-left. ΔV_{TH} monitoring is performed at a single polarization point ($V_{g,meas}$, $V_{d,meas}$) located in the linear region of the $I_D(V_G)$ characteristic, where the drain current I_D

degradation and V_{TH} shift can be correlated (Figure 2.13-right). This measurement technique also called "On the Fly" method and has been presented in section 1.4.3.2.2. V_{TH} drifts are then monitored during the stress ($V_{GStress} \neq 0$ V) and recovery ($V_{GStress} = 0$ V) phases. Note that there is a delay of about 20ms between the end of stress and the V_{TH} record, during which a recovery already occurs but cannot be measured. During stress phase, a positive $V_{GStress}$ is applied, while the drain and source are grounded. During recovery, all contacts are grounded. In both phases, the V_{TH} is periodically recorded (Figure 2.13-left).

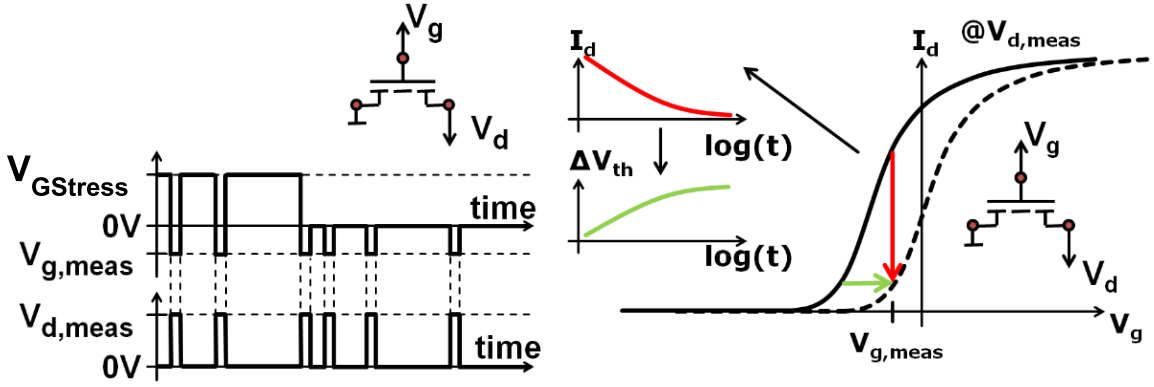

Figure 2.13. Left - Chronogram illustration applied to monitor V_{TH} drift during the stress and recovery phases. **Right -** Representation of the correlation between I_D degradation and ΔV_{TH}. The polarization point ($V_{g,meas}$; $V_{d,meas} = 5$ V) is in the linear region of $I_D(V_G)$ characteristic [144].

2.1.2.1.2 Experimental pBTI results

Stress and recovery pBTI transients obtained at different gate voltage stresses from 1 to 6V at room temperature, are presented in Figure 2.14. All stress and recovery transients depict a quasi-linear behavior on the semi-logarithmic scale indicating that the involved defects are uniformly distributed.
It can be observed that the trapping dynamic increases as $V_{GStress}$ rises during the stress phase. Conversely, the recovery dynamic also increases as the gate voltage stress increases. According to P. Lagger *et al.*, this linear behavior indicates a high concentration of traps. Finally, after 10^6s of relaxation, a nearly full recovery can be noticed after a gate voltage of 6V during 10^2s, at room temperature, indicating an absence of permanent degradation [144].

Electric field influence on the dynamic of the traps is highlighted on the data presented in Figure 2.15. These results were obtained via an experiment composed of different stress phases, where the gate voltage differs between each phase. A gate voltage stress of 3V is initially applied for 10s, during which the V_{TH} drift is monitored (green triangles). Immediately after this first stress phase, the gate voltage is increased to 4V for another 10s causing a higher V_{TH} drift (red diamonds). Directly afterwards, the gate voltage switches back to 3V for 10^3s (green circles). The BTI transient obtained from this latter transient depicts a partial recovery occurred via the electrons emission from defects that are active at 4V, but not at 3V. The fact that the ΔV_{TH} increases further for t_{stress} above 10^2s, after a ΔV_{TH} decrease before 10^2s, shows that there are still more defects with longer capture time that can be activated at $V_{GStress} = 3$ V. It is supposed

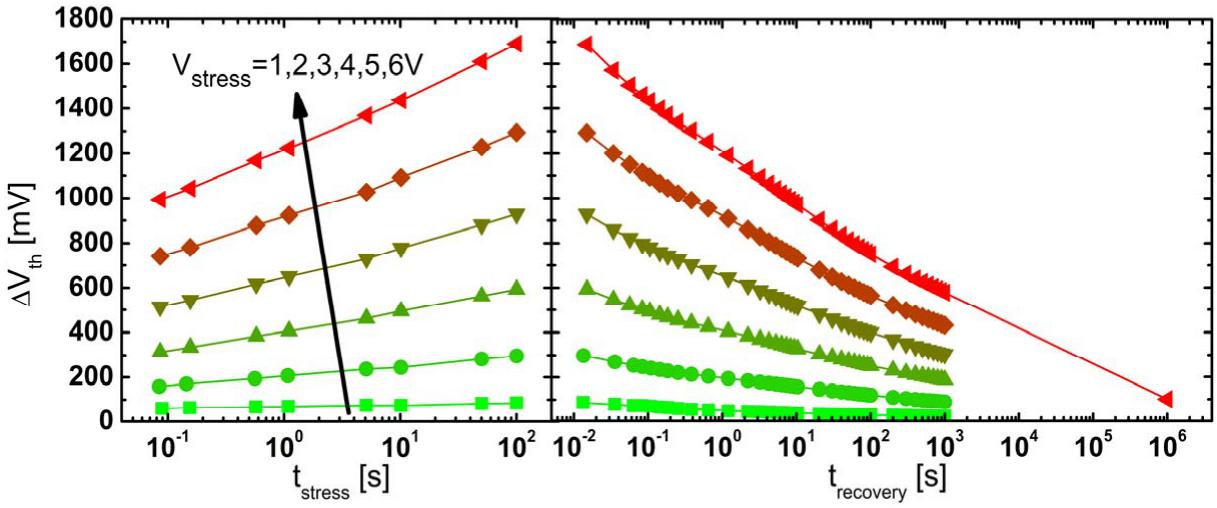

Figure 2.14. Stress and recovery pBTI transients for different gate voltage stress from 1V to 6V, at room temperature [144].

by the authors that the gate stress at 4V has accelerated electron capture into some defects by increasing the electric field. In any case, this experiment shows that a part of the trapped activated at high $V_{GStress}$ are not necessarily involved in BTI degradation obtained at a lower $V_{GStress}$ [137], [144].

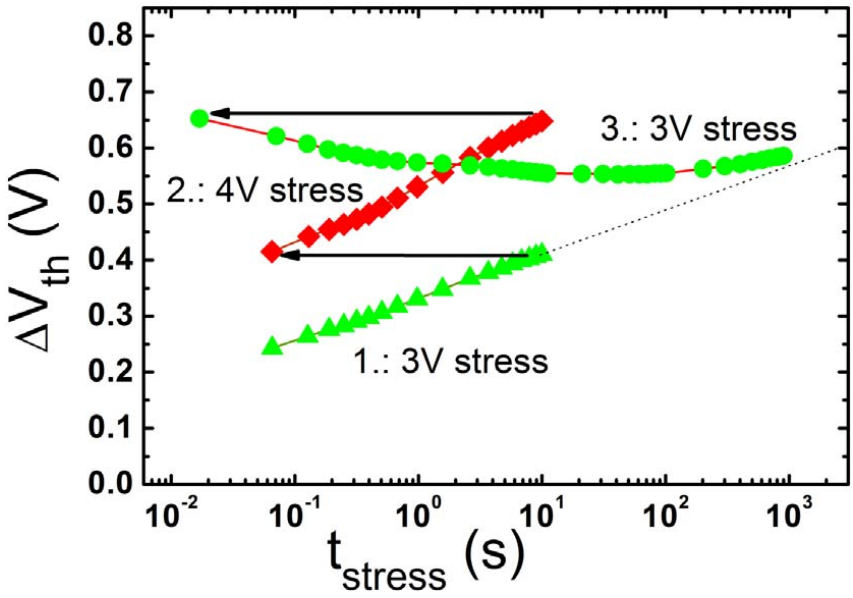

Figure 2.15. Experiment results showing the influence of the electric field on the traps dynamic. A pBTI degradation is initially obtained by applying a gate voltage stress of 3V for 10s (green triangles). Immediately after, the gate is then re-stressed at 3V for 10^3s (green circles), after an intermediate sequence of stress at 4V for 10s (red diamonds), showing parallel electron emission and capture [137], [144].

2.1.2.1.3 Results interpretation

As Meneghini *et al.* in [299], P. Lagger *et al* explain the pBTI degradation via a defect band between the Al_2O_3/GaN interface [144]. This is also consistent with the fact that V_{TH} drift is not associated with sub-threshold swing degradation, due to remote trapping at the dielectric/GaN interface spatially distant from the active channel (2DEG).

At equilibrium state, all traps within the defect band do not have the same charge state. Those being below the Fermi level are filled by an electron, while the defects above this reference energy level are empty, as illustrated in Figure 2.16-left. When a positive gate voltage stress is applied, a part of empty defects drops below the Fermi level and become energetically advantageous for the 2DEG electrons, i.e energy level related to the traps states is lower than energy level related to electron channel. Consequently, channel electrons move towards these new available states via a leakage path through the barrier, represented by a dashed line in Figure 2.16-center, and result in a V_{TH} decrease. During recovery, the defect band returns to its initial position, and the traps that were filled during stress are located thus above the Fermi level. Hence, the available states within the channel are energetically advantageous for electrons trapped above Fermi level. Consequently, they move towards the electron channel via the leakage path within the AlGaN barrier, as shown in Figure 2.16-right [144], leading to a V_{TH} decrease.

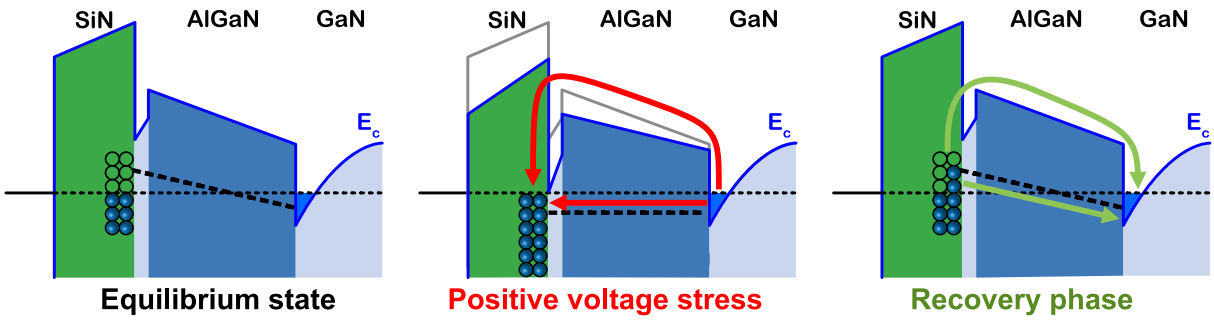

Figure 2.16. Left - At equilibrium state, the traps states within the defects band at Al_2O_3/GaN interface are neutral if they are above the Fermi level while they are negatively charged if they are positioned below. **Center -** When a positive $V_{GStress}$ is applied, the channel electrons move towards the available states within the defect band via a leakage path in the barrier which is represented by a dashed line here. Hence, it results to V_{TH} increase. **Right -** During recovery, trapped electrons within the defects states above the Fermi level are depleted, and move towards the channel that is energetically advantageous, resulting to a V_{TH} decrease [144].

2.1.2.2 Fully recessed MOS gate HEMT architecture

Nowadays, the literature suffers from a severe lack of pBTI degradation studies on transistors integrating a fully recessed MOS gate HEMT. We can quote the study of Tian-Li Wu *et. al* who were interested in the influence of the gate dielectric nature on pBTI degradation [329]. We can also cite the study of W. Vandendaele *et. al* who compared the pBTI degradation induced by an AC gate voltage stress to that induced by a DC $V_{GStress}$ [332]. Finally, A. Guo and J. A. del Alamo sought to explain both nBTI and pBTI degradation through a single physical model, whose study will be presented in this section [302]. In their study, the tested transistor as well as

the experiment are exactly the same as what is presented in section 2.1.1.2.1 about nBTI study on fully recessed gate MOS-HEMT architecture.

2.1.2.2.1 Experimental pBTI results

Stress and recovery pBTI transients obtained under different positive gate voltage stresses from 1 to 5V at room temperature, are shown in Figure 2.17.

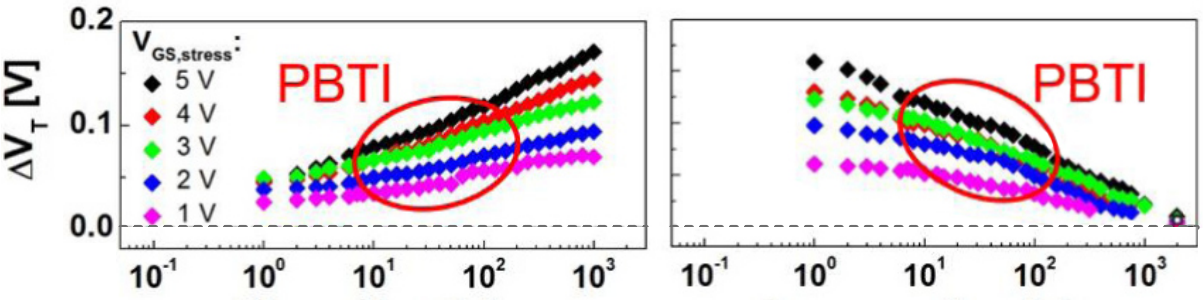

Figure 2.17. Stress and recovery pBTI transients recorded under different positive gate voltage stress from 1 to 5V at 25°C [302].

During the stress phase, it can be noted that pBTI degradation increases with the gate voltage, by following a linear dynamic in semi-log scale. This linear behavior can be also observed during recovery phase, and indicates a high amount of traps involved in pBTI degradation. As also observed by P. Lagger *et al.* the recovery dynamic increases with $V_{GStress}$, by achieving a full recovery after more than 10^3s of relaxation. It thus indicates that there is no permanent BTI degradation here.

A correlation between nBTI and pBTI degradation was also pointed out in this study through the results presented in Figure 2.18.

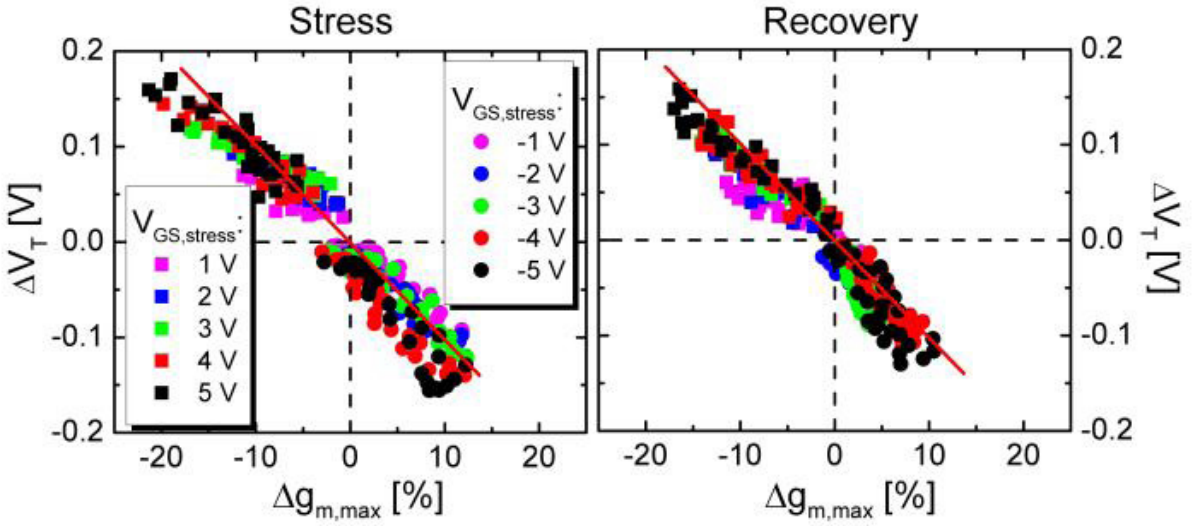

Figure 2.18. ΔV_{TH} as a function of $g_{m,max}$ during the stress and recovery phases for $V_{GStress}$ from -5 to 5V at room temperature indicates a strong correlation between these parameters. It also suggests that nBTI and pBTI degradation are the consequence of a common reversible mechanism under moderate gate voltage [302].

It shows ΔV_{TH} as a function of $\Delta g_{m,max}$ during the stress and recovery phases for $V_{GStress}$ from -5 to 5V at room temperature. A close correlation between the two parameters via a linear relationship and with an almost constant slope, can be observed. According to A. Guo and J. A. del Alamo, this symmetric continuum strongly indicates that nBTI and pBTI are the result of a common reversible mechanism under moderate gate voltage.

The temperature influence on pBTI degradation obtained under positive gate voltage stress was also studied here. Figure 2.19 shows the ΔV_{TH} transients under a gate stress of 2V for different temperatures. It can be noted that there seems to be a fast trapping phenomenon for very short stress times, but as the experimental setup is limited to studies beyond 1s, it is difficult to confirm this. It can also be observed that ΔV_{TH} increases more rapidly during stress as temperature increases, and ΔV_{TH} recovery is also accelerated with temperature, particularly at T $= 20\,^{\circ}$C and 40°C.

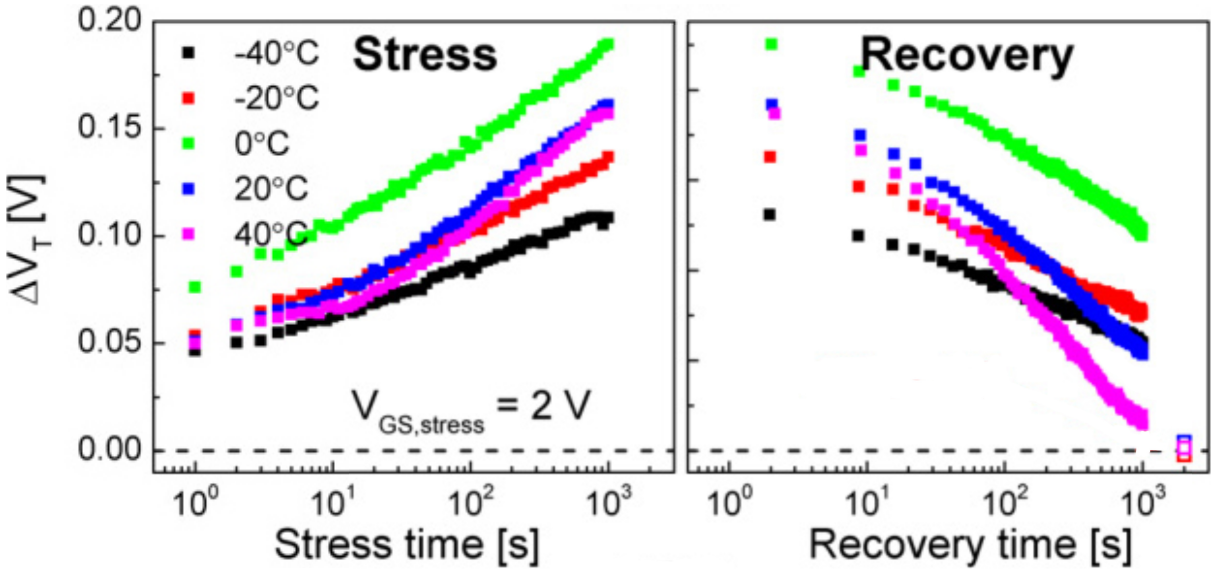

Figure 2.19. Stress and recovery pBTI transients obtained temperatures from -40 to 40°C at $V_{GStress} = -2$ V [302].

By using the results presented in Figure 2.19, an Arrhenius analysis was carried out (Figure 2.20). Stress times reported in these plots correspond to the time when pBTI shifts reach a value of 0.6V. The activation energy related to nBTI degration is at 0.37eV showing a strong temperature dependence. Arrhenius analysis on recovery nBTI transients was also performed, by extracting the recovery times needed for a 50% ΔV_{TH} recovery. It can be noticed in Figure 2.20, that pBTI stress times show a significant dispersion for both stress and recovery phases, indicating that the extracted activation energy is likely to be subjected to an important error. As shown in Figure 2.20, the activation energies are around $E_a \approx 0.1$ eV for both phases, exhibiting a weak temperature dependence of ΔV_{TH} recovery. In chapter 4, we will see that a similar activation energy value is also obtained in the case of our device. Although the extracted activation energies values in pBTI degradation are not comparable to those obtained in nBTI degradation, it can be noticed that the reported points are relatively close in the Arrhenius plots of Figure 2.20. Based on the dispersion obtained for pBTI degradation, the question of whether the activation energies are actually the same in the case of nBTI and pBTI degradation is legitimate.

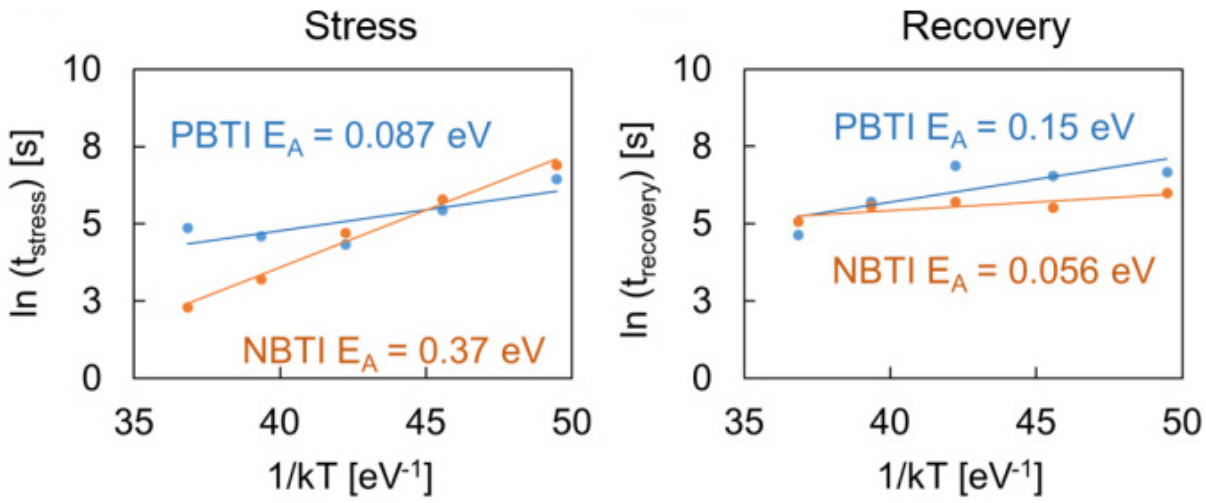

Figure 2.20. Arrhenius plot of nBTI and pBTI transients obtained by applying a gate voltage stress of −2V and 2V respectively, for stress and recovery phases [302].

2.1.2.2.2 Results interpretation

According to A. Guo and J. A. del Alamo, both nBTI and pBTI degradation can be explained by a distribution of preexisting Al_2O_3 gate oxide traps. At equilibrium state, Al_2O_3 defect band is distributed from below the Fermi level to above the GaN conduction band minimum, as illustrated in Figure 2.10-left and 2.21-left. The traps are filled if they are below the Fermi level while they are neutral if they are located above. During the positive gate voltage stress, trapped electrons are attracted by the neutral traps that are dropped below the Fermi level (Figure 2.21-center), leading to a positive V_{TH} shift. During recovery, the same acceptor states go back above the Fermi Level. Hence, trapped electrons within these related traps move towards GaN conduction band which is energetically advantageous during recovery (Figure 2.21-right). It thus results in a relaxation towards the equilibrium.

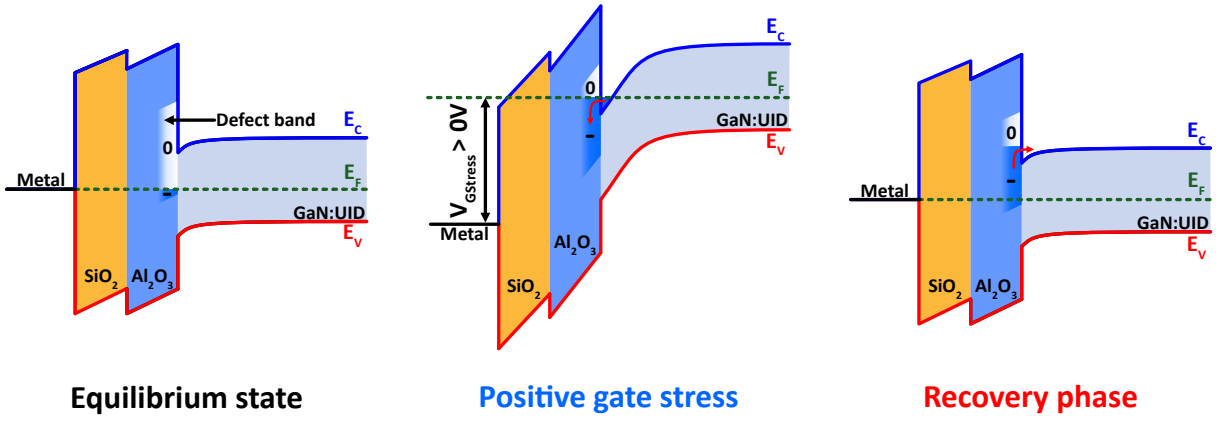

Figure 2.21. Left - At equilibrium state, the traps within the Al_2O_3 defects band are filled if they are below the Fermi level and are negatively charged when they are located above. **Center -** When a positive $V_{GStress}$ is applied, the electrons channel are attracted by the new available states below the Fermi level, leading to electron injection within the gate oxide defects, and hence to a positive V_{TH} drift. **Right -** During recovery, the trapped electrons move towards GaN conduction band, and induce a negative V_{TH} shift [302].

2.2 Investigation of nBTI degradation

In this section, the influence of a negative gate stress on the V_{TH} threshold voltage instabilities is studied in the case of the E-mode GaN-on-Si MOSc-HEMT developed at CEA-LETI. Temperature-dependent nBTI transients revealed the influence of traps located in the epitaxy, which was confirmed by complementary ToF-SIMS analyses and TCAD simulations. The traps nature was identified as carbon species in the nitrogen sites of the GaN lattice (C_N), located in the GaN:C layer. All these aspects will be developed in the following sections.

2.2.1 Device description and experimental setup

A representation of the fully recessed MOS gate for 8" GaN-on-Si MOSc-HEMTs developed in CEA-LETI is also presented in Figure 2.22-left. The reference epitaxial structure embeds a transition layer followed by a carbon doped GaN (GaN:C), both thicker than 1µm. A back-barrier (BB) layer is used to adjust the V_{TH}. Afterwards, an unintentionally doped GaN layer is grown on the top of the back-barrier (BB) to form the conductive channel. An AlGaN barrier is then deposited afterward in order to create the 2D Electron Gas (2DEG) at AlGaN/GaN:UID interface. Regarding the layout, all the tested transistors are either 100 or 200µm wide (W_G) while L_{GD} and L_{GS} are constant.

Fast nBTI technique principle under DC negative gate voltage stress is illustrated in Figure 2.22-right and is similar to the one used in Figure 1.64. A negative gate voltage stress $V_{GStress}$ of -5V is applied between 1µs and 100s. During this period, fast $I_D(V_G)$ ramps (< 10 µs) are periodically applied using an Agilent B1500 with Waveform Generator Fast Measurement Units (WGFMU) to monitor the ΔV_{TH} during the stress phase while minimizing the unwanted recovery during measurements. Note that the drain voltage is set to 0V during gate stress, while it is fixed at 100mV during fast $I_D(V_G)$ measurements. Finally, the threshold voltage is always extracted at a fixed current level of $I_D = I_0 \cdot W_G/L_G$ where $I_0 = 20 \cdot 10^{-9}$ A.

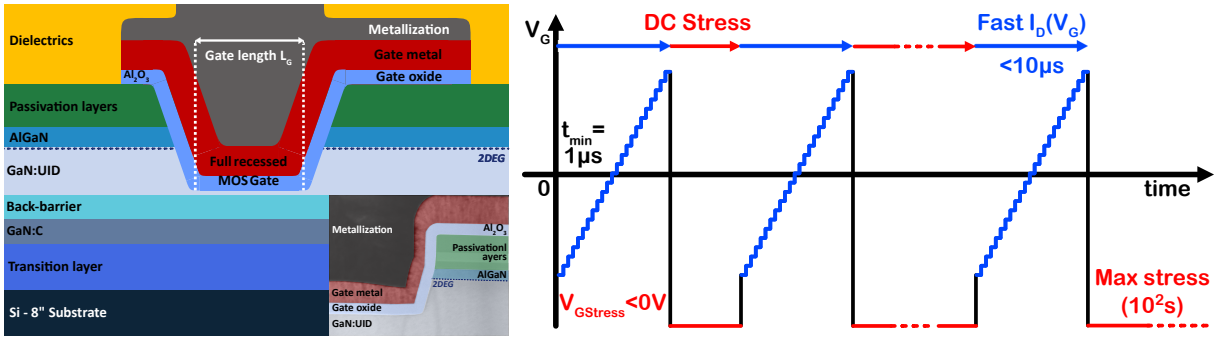

Figure 2.22. Left - Schematic of the GaN-on-Si E-mode MOSc-HEMT. TEM cross section exhibits the full recess profile of the gate corner. The gate length L_G is set to 1µm here. **Right -** Illustration of the chronogram used for the ultra-fast nBTI technique under DC gate voltage stress.

2.2.2 Typical BTI measurements

Median curves of typical nBTI transient behavior for four different L_G are shown in Figure 2.23, where the devices are subject to a negative gate stress of -5V during 10^3s. These measurements were performed at room temperature on 21 devices to get statistical measurements. It can be noticed that at the beginning of the gate stress, ΔV_{TH} is very stable until 1s. From 1s to 10s of stress, ΔV_{TH} suddenly decreases revealing a first time constant τ_1, which increases as L_G increases. Then, the ΔV_{TH} reaches a plateau whose level increases as L_G decreases. After more than 10^2s of stress, ΔV_{TH} decreases abruptly and seems to exhibit a second time constant τ_2 at longer stress time. These behaviors, described by strong ΔV_{TH} decrease separated by stable ΔV_{TH} phases, have never been observed and studied before. In this section, these time constants will be explored in detail through temperature dependent measurements.

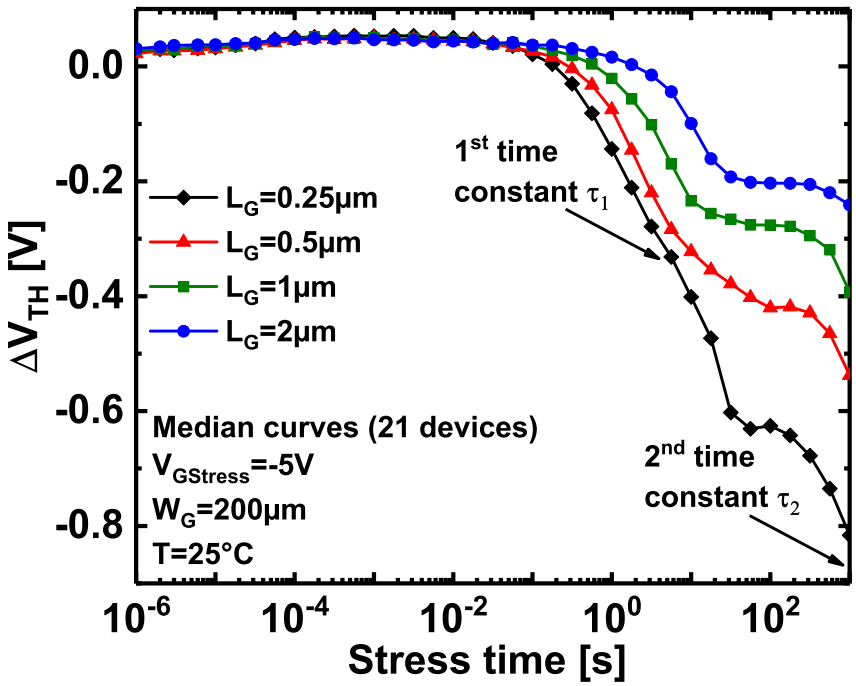

Figure 2.23. Median curves of typical nBTI transients obtained by applying a gate voltage stress of -5V. They have been measured at room temperature on 21 devices for $L_G = 0.25$, 0.5, 1 and 2 µm (W_G of 200µm).

2.2.3 Hole influence within the devices at room temperature

2.2.3.1 Device description

In the literature, the V_{TH} decrease under negative gate stress phenomenon is well known in particular with regards to the pMOS transistor [296]–[298], [334]. As explained in section 1.4.3.1, when the pMOS is at On-state, a negative gate voltage ($|V_G| > |V_{TH}|$) is applied, consequently the accumulated charges are holes. If there are some defects in the gate oxide, the holes can be trapped depending on the oxide traps position as well as their energy level relative to the hole channel. This trapping process also depends on the temperature, as well as on the gate voltage, i.e the electric field within the gate oxide. Once the trapping process occurs, a repulsive force is set up between trapped holes and the carriers in the channel leading to a V_{TH} shift. The

hypothesis that nBTI transients might be induced by hole trapping in the Al_2O_3 gate oxide has to be verified. In order to know if free holes are responsible for nBTI degradation, $C(V_G)$ measurement are performed on the reference substrate and on an intentionally p-type doped epitaxy which are presented in Figure 2.24.

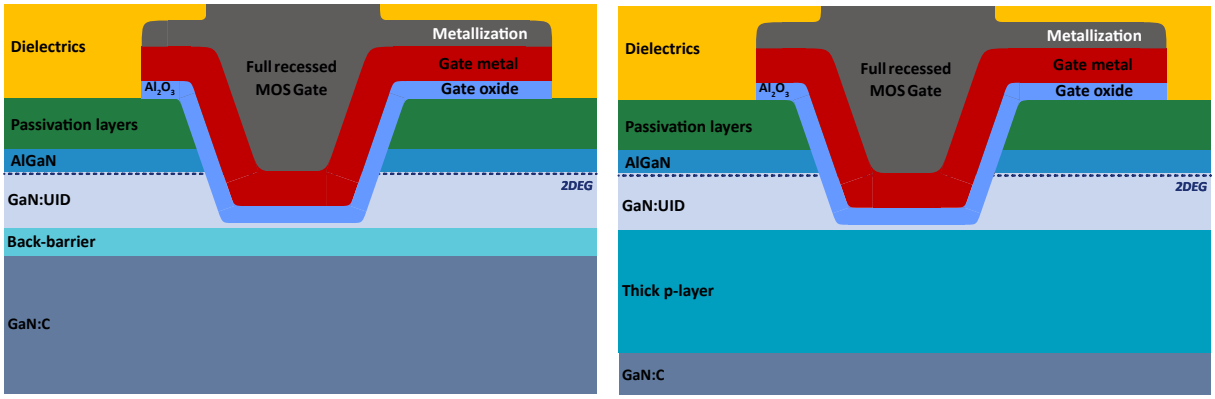

Figure 2.24. Right - Device representation of the reference epitaxial structure **Left -** Illustration of the device where an intentionally p-type doped epitaxy is embedded.

2.2.3.2 Holes detection via $C(V_G)$ characteristics

$C(V_G)$ measurements performed on both structures (Figure 2.24) are exhibited in Figure 2.25-left. They were performed at room temperature, at a frequency of 1kHz, and on three devices to ensure measurements repeatability. We can notice that the capacitance is not the same at negative gate voltage. Indeed, the capacitance on thick p-layer structure is around $50\text{nF}\cdot\text{cm}^{-2}$ at -6V, and tends to increase as the gate voltage decreases. On the other hand, the capacitance is negligible on the reference structure for negative gate voltage and does not vary with V_G. When a p-thick layer is embedded, a free hole accumulation under the gate appears and then increases the capacitance which is not the case on the reference structure due to free hole absence. By using the following relations, it is possible to deduce the free carrier density $N_{n,p}$ using the $C(V_G)$ characteristics [335].

$$N_{n,p}(V_G) = \frac{1}{q\cdot\epsilon_{00}\cdot\epsilon_{GaN}\cdot Y(V_G)} \tag{2.1}$$

Where $Y(V_G)$ is the Maserjian function which is expressed by the following equation,

$$Y(V_G) = \frac{1}{C(V_G)^3}\cdot\frac{dC(V_G)}{dV_G} \tag{2.2}$$

As shown in Figure 2.25-right, the free holes density p is about $5\cdot10^{17}\text{cm}^{-3}$ in the case of a thick p-layer structure at $V_G = -7$ V.

2.2.3.3 Hole influence on nBTI transient behavior

Both structures presented in Figure 2.24-left have been subject to nBTI tests. A gate voltage stress $V_{GStress}$ of -5V during 10^3s has been applied, at room temperature and for $L_G = 1$ µm.

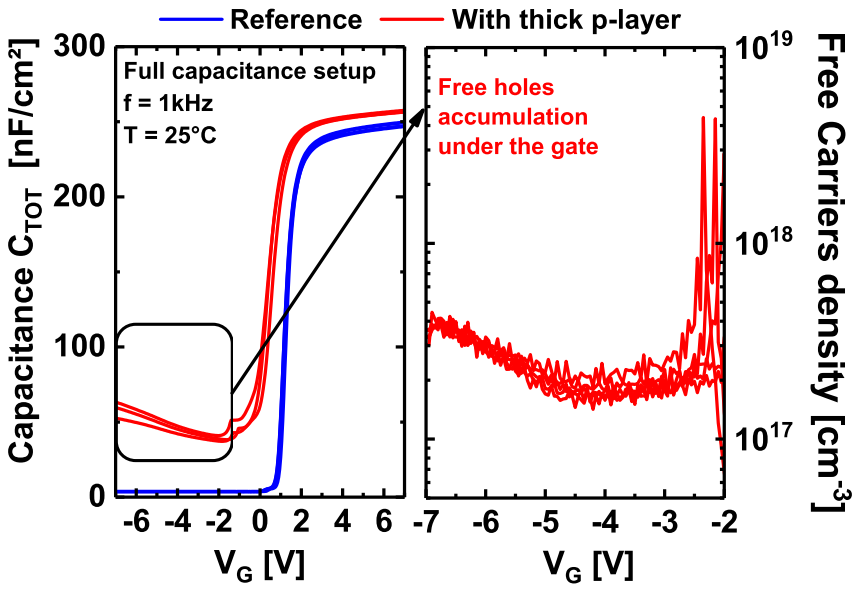

Figure 2.25. Right - $C(V_G)$ measurements performed at room temperature and at a frequency 1kHz on the reference and the thick p-layer structure. **Left -** Free carrier density as a function of the gate voltage during the hole accumulation regime on thick p-layer structure deduced from the Maserjian function.

Figure 2.26 exhibits a median curves comparison between nBTI transients obtained on both structures. A monotonous ΔV_{TH} decrease can be observed for the p-type thick layer structure, which is related to nBTI degradation behavior reported in literature [298], [334]. On the other hand, the nBTI behavior obtained on the reference structure is completely different in the way that strong ΔV_{TH} decreases occur but are separated by ΔV_{TH} plateaus. These observations suggest that the nBTI transient behavior obtained on the reference epitaxy (Figure 2.22-left and 2.23-left) is not due to free hole injection in the gate oxide.

2.2.4 Temperature dependent analysis

2.2.4.1 NBTI transient as a function of temperature

In order to characterize the trap populations involved in the nBTI transients presented in Figure 2.23, a temperature-dependent analysis has been carried out. The aim of this analysis is to extract an activation energy E_a through time constants τ_1 and τ_2 analysis, in order to identify the nature of the related trap populations. NBTI measurements are performed under negative gate stress of -5V during 10^3s from 25°C to 225°C. Figure 2.27 shows the resulting nBTI transients for a gate length of 0.25 and 2µm. It can be noticed that both time constants τ_1 and τ_2 decrease when the temperature increases, showing that trapping process is significantly activated by the temperature.

2.2.4.2 Arrhenius analysis of τ_1 and τ_2

The time constant τ_1 is extracted by taking the minimum position of the nBTI transient derivative ($\partial\Delta V_{TH}/\partial\log(t)$) at each temperature. ΔV_{TH} transients were fitted with a moderate order

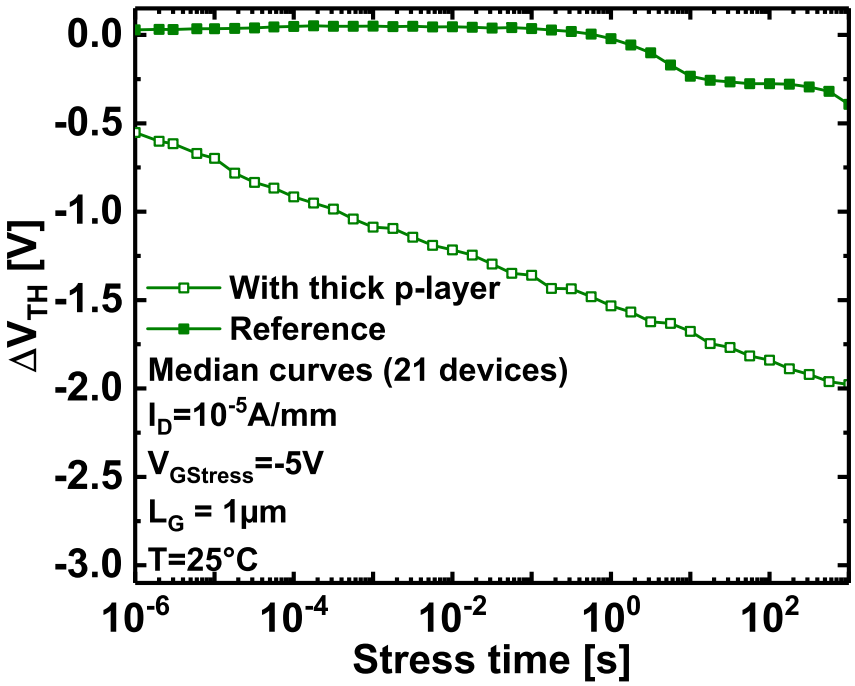

Figure 2.26. NBTI transient performed at a $V_{GStress} = -5$ V at 25°C, on the reference epitaxial structure and the structure including the thick p-layer. The gate width is 100µm, and the gate length is $L_G = 1$ µm here.

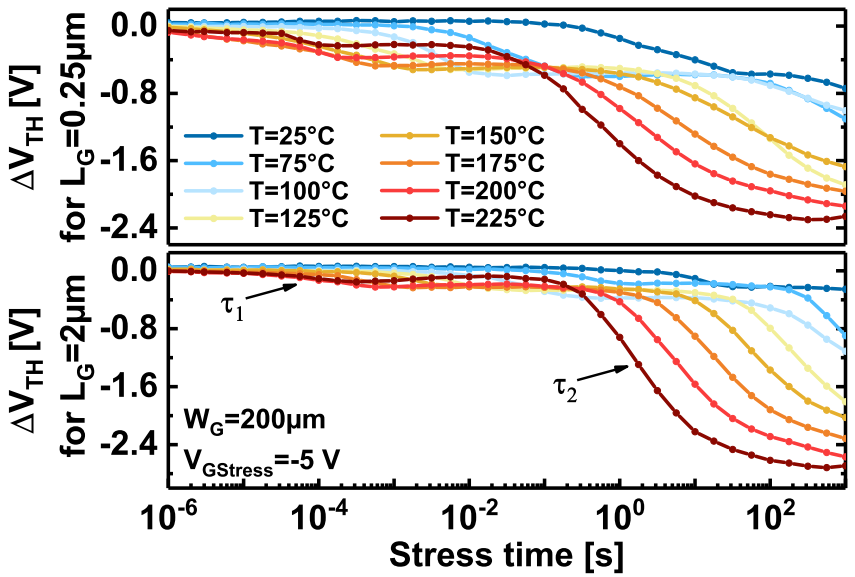

Figure 2.27. NBTI transients obtained at $V_{GStress} = -5$ V and different temperatures T, from 25°C to 225°C, and for $L_G = 0.25$ and 2 µm.

polynomial function (between 5 and 7), in order not to derive the possible noise from the experimental results and thus increase the error. Figure 2.28-left shows the derivative curves of the nBTI transients at various temperature for two different L_G. The minima positions of these derivative curves correspond to τ_1 at each temperature. Once extracted, time constants τ_1 are then reported as a function of $q/k_B \cdot T$ in an Arrhenius plot, as shown in Figure 2.28-right. It is worth noticing that the activation energy $E_a \approx 0.8$ eV for the four different gate lengths. Therefore, the first time constant is then related to the same trap population whatever the gate length.

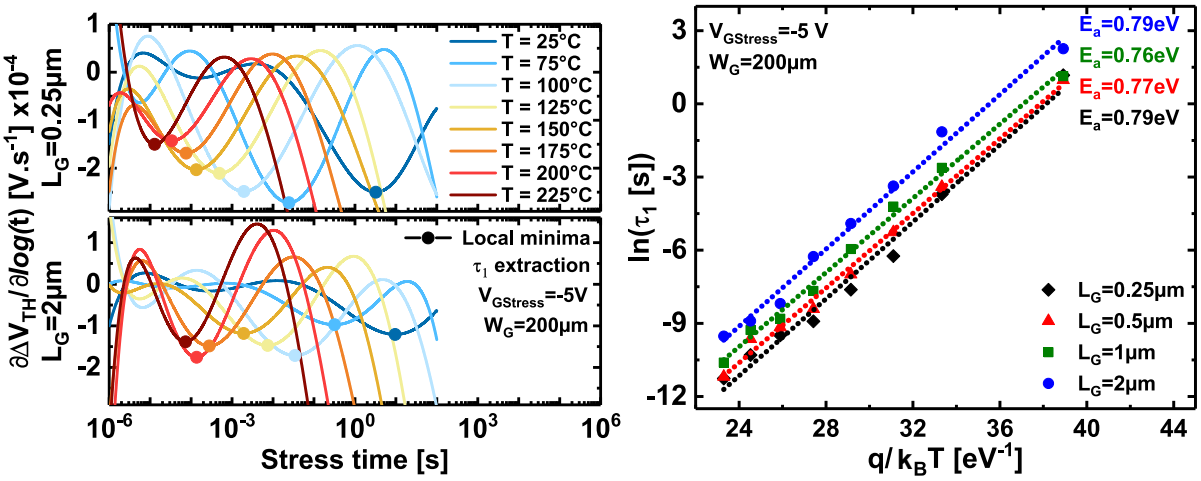

Figure 2.28. Left - First time constant τ_1 extraction corresponding to the local minima of nBTI transient derivative at each temperature, for $L_G = 0.25$ and 2 µm. **Right -** Arrhenius plot of the first time constant τ_1. The same activation energy $E_a \approx 0.8$ eV is found for all gate lengths.

Figure 2.29-left shows the derivative curves of the nBTI transients at each temperature for $L_G = 0.5$ and 2 µm. Minima positions of these derivative curves correspond to τ_2. The second time cannot be extracted at all temperatures, because it appears after longer stress durations, especially at low temperature ($T < 100$ °C). As first time constant, τ_2 is also reported as a function of $q/k_B \cdot T$ in an Arrhenius plot, shown in Figure 2.29-right. The extracted activation energy of τ_2 is also around 0.8eV for the four different gate lengths. Therefore, the first and the second time constants are then related to the same trap population for all gate lengths. According to the literature, this energy is very often related to C traps in N sites in GaN (C_N) [87], [94]–[96], [229]. The same activation for two different time constants can be explained by the position of the trap populations. Indeed, recent studies indicated that C_N traps could be located at two different positions under the gate. The latter observation suggests that two C trap populations are involved in nBTI degradation [101], [267], [336], [337].

2.2.5 Trap population localization via ToF-SIMS measurement

In order to locate these two C_N trap populations that are involved in nBTI degradation, Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) measurements were carried out from the top of the gate oxide to the GaN bulk. This destructive measurement consists, first, in scanning a low energy Cs ion beam (between 250keV and 2keV) to separate the surface atoms from the bulk. Subsequently, a second high energy beam (between 15keV and 30keV) based on Bi_3 scans the surface to ionize the different particles on the sample surface, as shown in Figure 2.30-left.

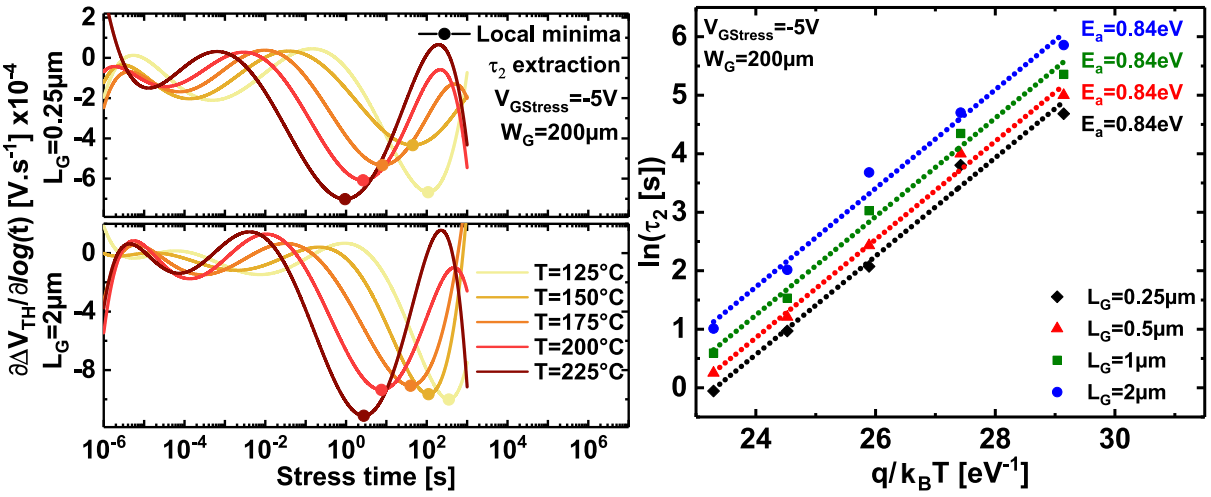

Figure 2.29. Left - Second time constant τ_2 extraction corresponding to the local minima of nBTI transient derivative at each temperature, for $L_G = 0.25$ and 2 µm. **Right -** Arrhenius plot of the second time constant τ_2. The same activation energy $E_a \approx 0.8$ eV is found for all gate lengths.

Note that the Bi_3 beam is only dedicated to the analysis, which implies that the associated dose is relatively low (one Bi_3 atom for 10^3 surface atoms), while the dose related to the cesium beam (one Cs atom for one surface atom) is used to abrade the surface. Finally, the ionized particles are brought towards a detector thanks to an electric field applied between the detector and the sample. The time of flight for the surface particles to reach the detector depends on their mass. Consequently, it is possible to know the chemical nature of the particles that composed the sample by measuring their time of flight.

The lateral resolution of the Tof-SIMS measurement is about one hundred nanometers, which is unlikely to provide reliable information. However, the vertical resolution can reach one nanometer, which is very interesting to study the presence of the carbon population below the gate oxide. In order to increase the Tof-SIMS measurement resolution, the abraded area must be as wide as possible. Consequently, this measurement was performed on a structure dedicated to Van der Pauw measurements where the gate stack is the same as the gate transistor, but with an area of $200 \times 200\mu m^2$. The measurement resolution can also be degraded if the layers above the region of interest are higher than 1µm. In our case, the 4µm thickness of the passivation and metallization layers above the Al_2O_3 gate oxide was removed via a wet etching, where hydrofluoric acid (10%) was used during 30min.

ToF-SIMS analysis results are presented in Figure 2.30-right. By tracking the presence of C atoms and CN molecules, we can observe the presence of two carbon populations. The first one is located at the Al_2O_3/GaN interface and the second one related to the GaN:C layer. The carbon presence at the Al_2O_3/GaN interface could originate from the TMA precursor used to deposit the Al_2O_3 by Atomic Layer Deposition, since TMA is a carbon-based molecule ($Al_2C_6H_{18}$). After subsequent thermal treatments, carbon can diffuse into N-vacancies previously induced by dry etching to create the recessed cavity [338]. This carbon presence could be also explained using resin mask during the dry etching of the gate cavity. Indeed, during ICP etching, ion beams can potentially abrade the resin, and favor the incorporation of carbon within the gate cavity.

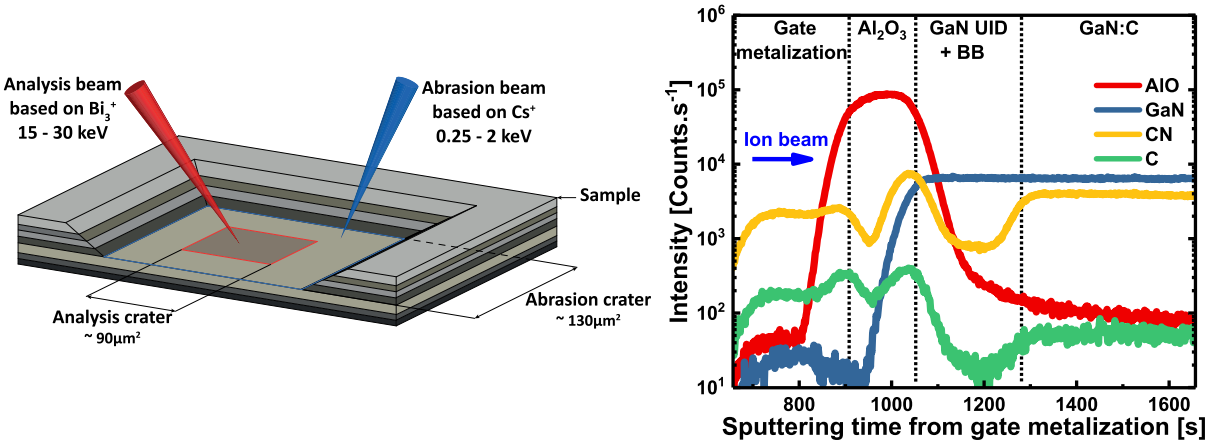

Figure 2.30. Left - Illustration of ToF-SIMS measurements principle. **Right -** Results of ToF-SIMS analysis showing two carbon populations. One located at Al_2O_3/GaN interface, and the second one located in the GaN:C layer which is intentionally embedded.

2.2.6 V_{TH} reduction mechanism studied with TCAD simulation

2.2.6.1 Experiment principle

To summarize, the $C(V_G)$ measurements in Figure 2.25 showed that the nBTI degradation in Figure 2.23 is probably not due to the holes trapping in the Al_2O_3 gate oxide, at least at 25°C. From the temperature dependent analysis, two C_N trap populations are located at different positions in the GaN bulk. ToF-SIMS analysis indicates that the C_N trap populations are localized in the GaN:C layer and at Al_2O_3/GaN interface. Since the V_{TH} reduction under negative gate voltage stress is associated with holes injection mechanism in the literature, and we have already demonstrated that this mechanism cannot be valid due to the absence of holes in the structure at 25°C, how can these two populations of C_N traps lead to a V_{TH} reduction?

In order to understand the physical mechanism that induces this V_{TH} reduction, TCAD simulations were performed on a structure composed of GaN:C ($10^{19}cm^{-3}$), GaN:UID and Al_2O_3 gate oxide layers, as illustrated in Figure 2.31. A 2DEG is simulated at AlGaN interface and is connected to the source and drain on both sides of the gate. The structure does not embed a back-barrier layer for simplicity. In the simulation, the C-doping is declared as a trap acceptor with an energy level at 0.8eV above the GaN valence band, according to the literature. Note that the trapping and detrapping process have been simulated using Shockley-Read-Hall model. Transient simulations have been performed on gate stack presented in Figure 2.31. The aim of this simulation is to compare the ionized C_N distribution at $V_G = 0$ V, obtained before and 1µs after a gate voltage stress of -5V during 10^3s, as illustrated in Figure 2.32. Note that during this simulation, the source, drain and substrate are connected to ground.

2.2.6.2 Simulation results

Concentration distributions of the ionized C_N traps before and 1µs after a negative gate stress of 10^3s at $V_{GStress} = -5$ V are shown in Figure 2.33. Comparing these distributions, a charge

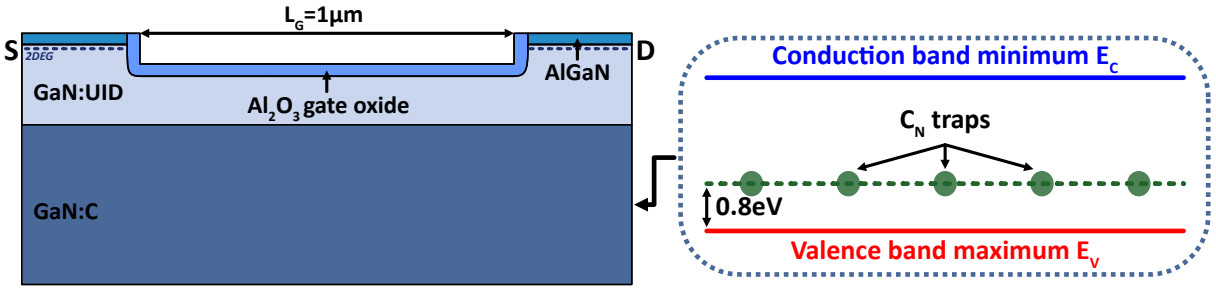

Figure 2.31. Left - Illustration of the structure simulated by TCAD. The stack is composed of a GaN:C (10^{19}cm^{-3}), a GaN:UID and an Al_2O_3 gate oxide layer. **Right -** The carbon in GaN:C layer has been declared as an acceptor trap at 0.8eV from the valence band, and the trapping and detrapping processes have been simulated using Shockley-Read-Hall model.

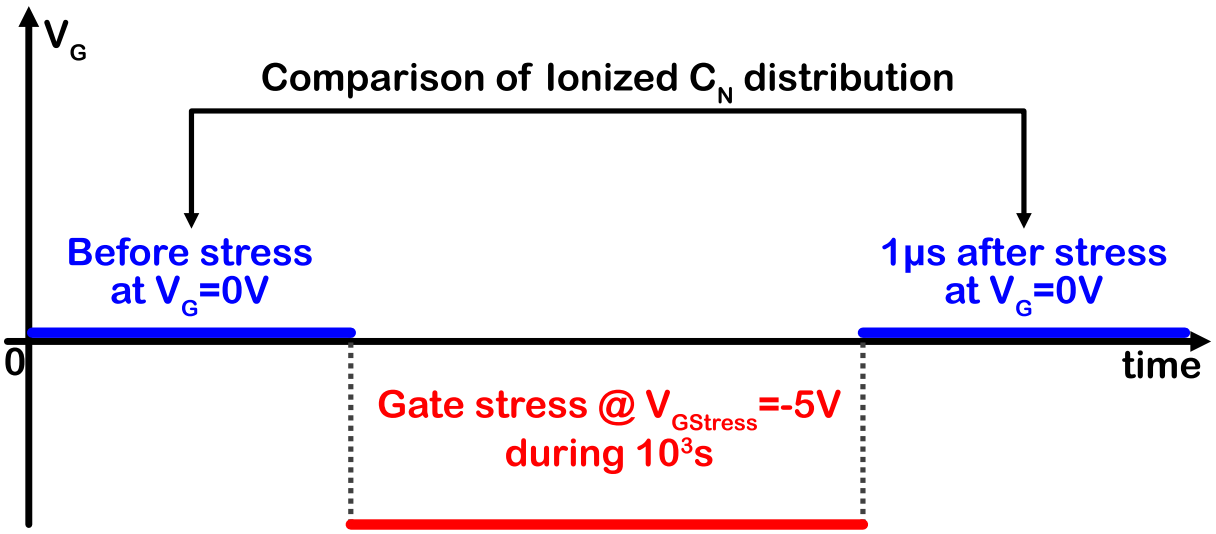

Figure 2.32. Principle of the transient simulations performed on gate stack presented of Figure 2.31. Ionized C_N distribution at $V_G = 0$ V, obtained before and 1µs after a gate voltage stress of -5V during 10^3s, are compared. Note that the source, drain and substrate are connected to the ground.

state modification of C_N sites after the gate stress can be noticed. Indeed, C_N traps are known to act as deep acceptors. At the equilibrium state, a part of them is ionized, i.e they are negatively charged ($-$), as shown in Figure 2.33-top. When a negative gate stress is applied, these ionized C_N traps release an electron which gives them the property of being neutrals. This mechanism can be also assimilated as a free hole trapping from the GaN valence band towards C_N sites. Consequently, C_N traps become neutral 2.33-bottom.

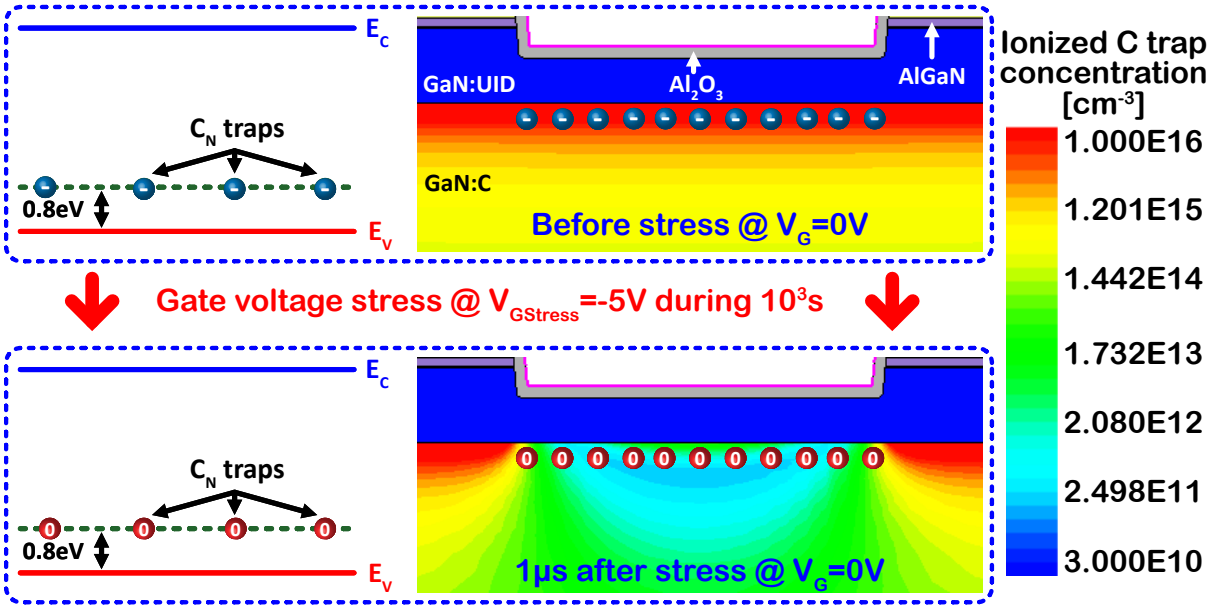

Figure 2.33. TCAD simulations showing concentration distribution of ionized C_N sites in GaN:C layer at $V_G = 0$ V. **Top -** Distribution obtained before the gate voltage stress of -5V during 10^3s. **Bottom -** C_N distribution 1µs after the gate stress.

The electrical consequences of the C_N sites charge state modification induced by a negative gate stress are relatively important. Indeed, by plotting the conduction band profiles E_C at $V_G = 0$ V, before and 1µs after the same gate stress, it can be noticed that they are quite different as shown in Figure 2.34.

Before the gate stress, a part of C_N sites is ionized ($-$), leading to a general increase of E_C value in the structure. After the negative gate stress, these become neutrals ($- \rightarrow 0$). This charge state modification implies the annihilation of the p-type doping-like effect induced by C_N sites and thus a global conduction band decrease within the whole structure. Since the conduction band value at the gate oxide interface gives an image of the threshold voltage, a general E_C collapse leads to a V_{TH} reduction [101]. Although that these TCAD simulations are not calibrated, these results are consistent with the experimental nBTI transients and explain the C_N trap influence on V_{TH} reduction.

Dynamic effects can be simulated as shown in Figures 2.34 and 2.35, where the E_C value behavior at 1nm under the middle of the gate is plotted as a function of time, after a gate voltage stress of -5V during 10^2s. It can be noticed that a stabilization occurs around 10s towards the initial value of E_C, corresponding to the moment when the C_N sites are ionized, i.e. modification of their charge state. Consequently, a positive ΔV_{TH} shift occurs by changing the charge state of C_N sites. These TCAD simulations thus demonstrates that V_{TH} decrease is possible without

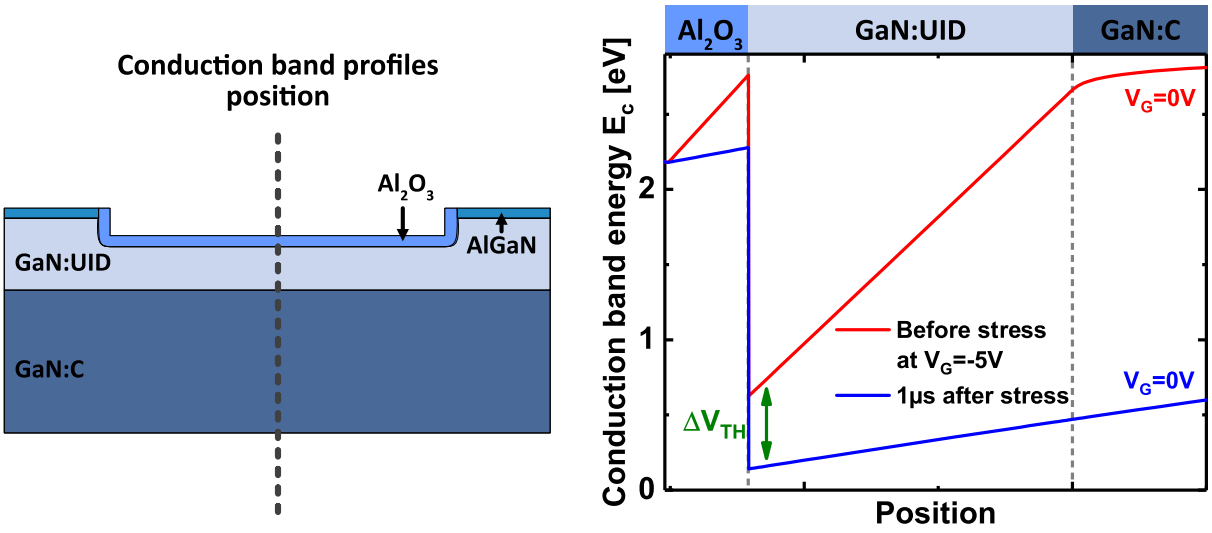

Figure 2.34. TCAD simulations of the conduction band energy profile of the MOS structure at $V_G = 0$ V before and 1µs after a stress at $V_{GStress} = -5$ V during 10^3s.

holes injection in the gate oxide by modifying C_N traps charge state.

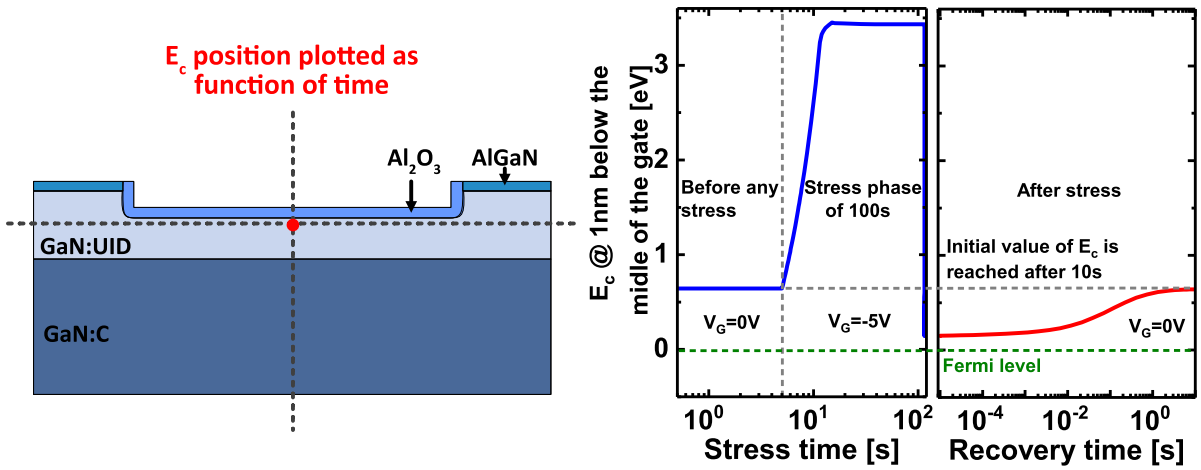

Figure 2.35. Conduction band energy value at 1nm below the middle of the gate before, during and after a stress of $V_{Gstress} = -5$ V during 10^2s. The gate is grounded before and after the stress.

2.2.7 Overall understating of nBTI degradation

2.2.7.1 Trap population related to τ_1

In section 2.2.5, ToF-SIMS analysis indicates that C_N trap populations are located in the GaN:C layer and at the Al_2O_3/GaN interface. According to the thermal analysis, two populations of C_N traps are located at different positions in the GaN bulk. Considering that, the question is to know which population corresponds to the time constants τ_1 and τ_2. For this purpose, nBTI measurements have been performed on a structure where the epitaxial GaN:C has been voluntarily moved away from the Al_2O_3/GaN interface as shown in Figure 2.36-left. It is considered

that with a GaN:UID thickness of more than 1µm between the Al_2O_3/GaN interface and the GaN:C layer, the C_N traps have no influence on the V_{TH} shift. The nBTI measurement was performed at $V_{GStress} = -4$ V during 10^3s and at T = 200 °C, for two gate lengths $L_G = 0.5$ µm and 1µm. Measurements results are presented in Figure 2.36-right.

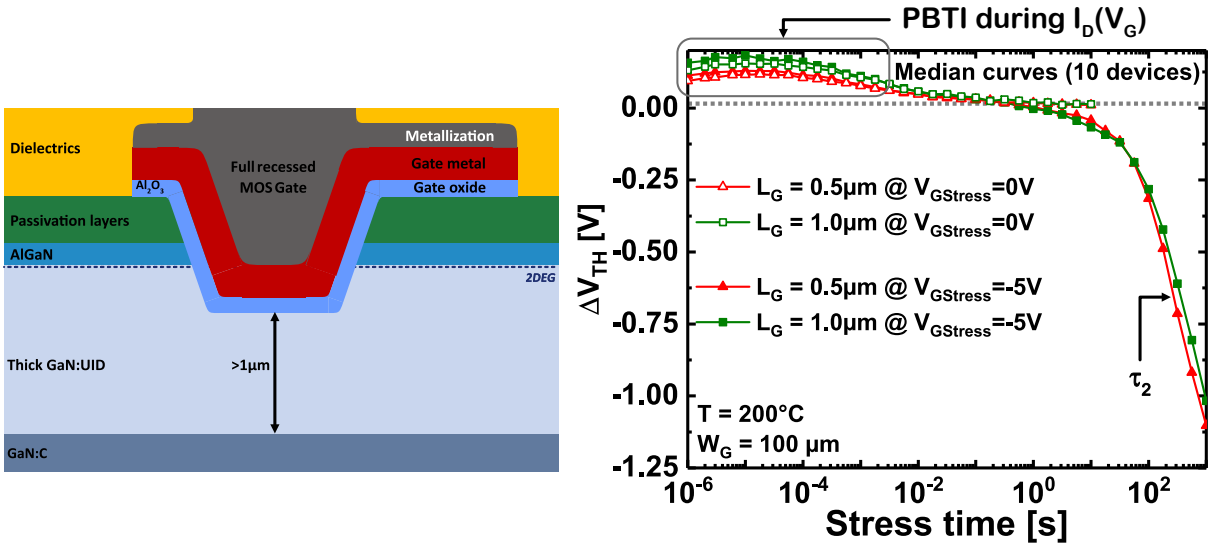

Figure 2.36. Left - Structure schematic where the epitaxial GaN:C has been moved away from the Al_2O_3/GaN interface. **Right -** NBTI transients performed on structure presented on the left at $V_{GStress} = -5$ V during 10^3s and at a temperature of 200°C, for two gate lengths $L_G = 0.5$ and 1 µm. Another BTI transients obtained at $V_{GStress} = 0$ V have been plotted to demonstrate that the bump at low time constants is related to an artifact measurement.

At very low stress times, a slight ΔV_{TH} increase followed by a decrease around $5 \cdot 10^{-3}$s can be can noticed, and could be associated with τ_1. In fact, this ΔV_{TH} bump is associated with a measurement artifact related to the fast $I_D(V_G)$ measurements dedicated to extract V_{TH}. Indeed, since there are four $I_D(V_G)$ measurements per time decade, this can lead to a slight pBTI degradation in the small time decades, i.e. between 10^{-5} and 10^{-6}s for example. At longer times (from 10^{-4} to 10^{-3}s) a recovery of this slight pBTI degradation occurs since the time between $I_D(V_G)$ measurements is higher than at low stress times. This measurement artifact can be observed by plotting the BTI transients obtained under a gate voltage stress of 0V, as shown in Figure 2.36. It can be observed that before 10^{-1}s, both BTI transients obtained at $V_{GStress} = 0$ V and −4V are identical revealing that the ΔV_{TH} bump at low time constants is associated with an artifact measurement and not with τ_1.

After 10s of stress, it can be noticed that a strong decrease of V_{TH} regarding the nBTI transients obtained under a $V_{GStress}$ of −4V. The $|\Delta V_{TH}|$ decrease magnitude above 1V is comparable to the strong variation of the BTI shift related to τ_2 in Figure 2.27. It can be also noticed that this strong variation related to τ_2 occurs later when the GaN:C is moved away from the gate. However, no ΔV_{TH} decrease related to τ_1 is observed on these nBTI transients. Therefore, it can be deduced that τ_1 is related to the GaN:C layer. In the following section, the influence of the carbon population at Al_2O_3/GaN interface on nBTI transients will be studied.

2.2.7.2 Trap population related to τ_2

2.2.7.2.1 Hard mask integration

As already discussed in section 2.2.5, the carbon presence at the Al_2O_3/GaN interface could originate from the precursor used to deposit the Al_2O_3 (TMA) as well as the photo-resist mask used during the gate recess. Indeed, during ICP etching, ion beams can abrade the resin on the surrounding of the gate cavity, and favor the incorporation of carbon on the GaN etched surface. This latter assumption was confirmed since a huge amount of carbon species has been found at GaN surface just after the recess via X-Ray Photo-electron Spectroscopy (XPS) measurements (not show here). In order to find out whether this trap population has an influence on the nBTI degradation, a SiN hard mask is used instead of a photoresist mask during gate recess. Consequently, the SiN hard mask should reduce the carbon concentration found at Al_2O_3/GaN interface. A decrease of nBTI degradation related to τ_2 is expected in the case where it is induced by C_N traps at gate oxide interface. A comparison between nBTI transients performed on devices fabricated using a photoresist mask and a hard mask are presented in Figure 2.37. Both of these transients are obtained by applying a $V_{GStress}$ of -4V at 200°C. It can be noted that there is no significant difference between the two nBTI transients. Assuming that the carbon population at the Al_2O_3/GaN interface was effectively removed, it can thus be suggested that it does not influence the degradation of nBTI. Therefore, the hypothesis stating that the τ_2 related nBTI degradation is induced by the C_N trap population at the Al_2O_3/GaN interface is not valid.

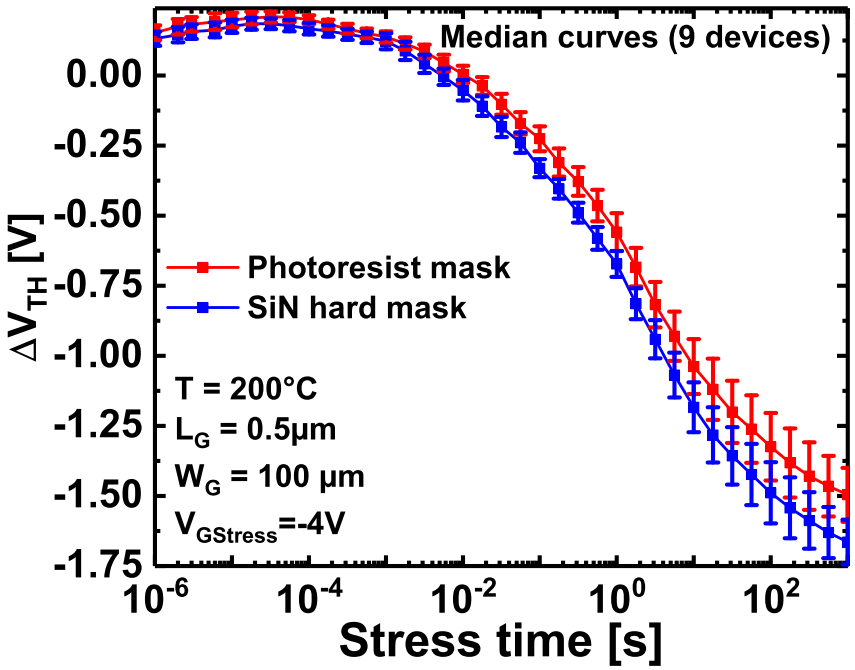

Figure 2.37. Comparison between nBTI transients performed on devices fabricated using a photoresist mask and a hard mask. These measurements have been obtained by setting $V_{GStress}$ at -4V during 10^3s at a temperature of 200°C. These median curves have been obtained by testing 9 devices where $L_G = 0.5$ µm and $W_G = 100$ µm.

2.2.7.2.2 NBTI at different gate voltage stress

In order to have a better understanding of the nBTI degradation origin related to the τ_2 time constant, another nBTI measurements were performed at different $V_{GStress}$. Figure 2.38 shows median curves of stress and recovery transients obtained at 200°C, where $L_G = 0.5$ µm and $W_G = 8$ mm. These median curves are the result of nBTI measurements performed on 10 devices. Recovery nBTI transients have been obtained by setting $V_{GStress}$ to 0V just after the stress phase. The ΔV_{TH} is then monitored during this recovery phase by performing fast $I_D(V_G)$ measurements.

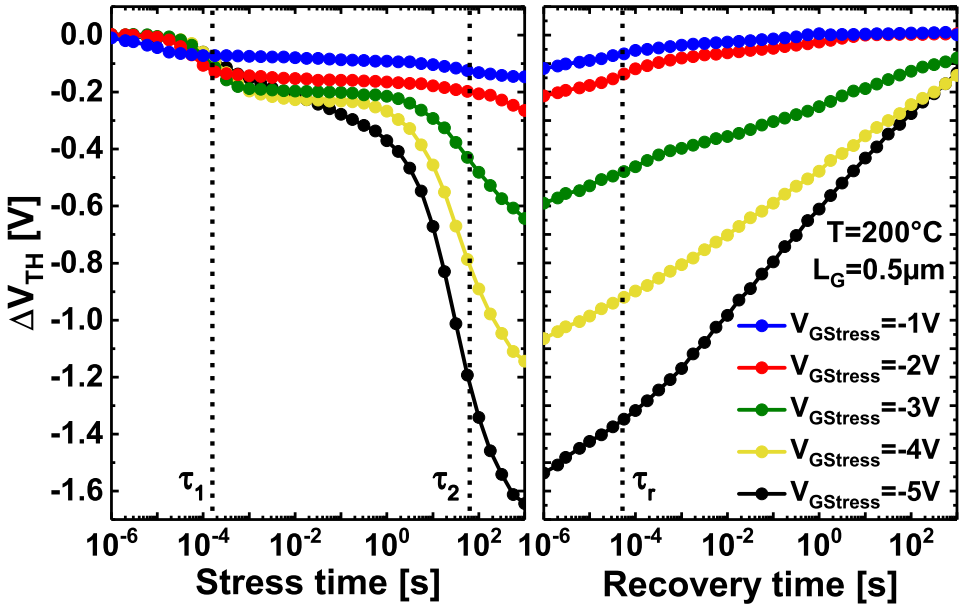

Figure 2.38. Stress and recovery nBTI transients obtained at different $V_{GStress}$ from -1V to -4V at a temperature of 200°C.

It can be noticed that the $V_{GStress}$ amplitude has a negligible influence on the time constant τ_1 which is around $2 \cdot 10^{-4}$ here. As shown in section 2.2.7.1, the presence of this time constant is related to the presence of GaN:C layer in the epitaxy. Indeed, a deionization of C_N sites located at 0.8eV from E_V occurs during a negative gate voltage stress, induces a conduction band collapse within the structure and thus a decrease of V_{TH}, as demonstrated in Figure 2.33, 2.34, and 2.35. The C_N sites deionization can also be assimilated as free holes trapping from the GaN:C valence band towards the C_N sites. A recovery can also be noticed on the whole relaxation transients, where there is a slight ΔV_{TH} acceleration around $5 \cdot 10^{-5}$, noted τ_r here.

Contrary to τ_1, it can be noted that the amplitude of $V_{GStress}$ has an important effect on the nBTI degradation related to τ_2. Indeed, the nBTI degradation related to τ_2 increases as $|V_{GStress}|$ increases. It is also important to note that this observation is only valid for gate voltage stresses lower than -2V, where a negligible nBTI degradation related to τ_2 is observed. This nBTI degradation behavior is the sign of a charge injection in the defects of gate oxide. Indeed, the underlying mechanism related to the charge trapping in the gate oxide is known to increase with the gate stress voltage, and appears only if the gate stress voltage is high enough. Therefore, a free hole trapping mechanism in a defect band in Al_2O_3 located below the GaN valence band can be considered in the case of long time nBTI degradation linked to τ_2. This assumption is

also supported by the monotonous increase of recovery transients. As it will be shown in chapter 3, this behavior can be described by a broad range of time constants τ related to a continuum of defect states usually found in amorphous material, i.e an Al_2O_3 defects band.

2.2.7.3 Results interpretation

2.2.7.3.1 Observations related to τ_1

A synthesis of the main observations related to τ_1 are given below:

- In section 2.2.4.2, temperature dependent analysis showed that the activation energy of τ_1 is around $0.8-0.9$eV. According to the literature, this energy is very often related to C traps in N sites in GaN (C_N) [87], [94]–[96], [229].
- In section 2.2.5, Tof-SIMS analysis depicted two potential carbon trap populations. One at Al_2O_3/GaN interface and the second within the GaN:C layer.
- By moving the GaN:C layer away from the gate oxide interface, nBTI transients presented in Figure 2.36 depict that the V_{TH} shift related to τ_1 disappears. Consequently, it can be deduced that τ_1 corresponds to the charge state modification of the GaN:C layer.
- TCAD simulations demonstrated (Figure 2.33, 2.34, and 2.35) that a deionization of C_N sites can occur during a negative gate voltage stress. It induces a conduction band collapse within the structure and thus a V_{TH} decrease.

2.2.7.3.2 Observations related to τ_2

The following points gives a summary of the main observations associated with τ_2:

- As τ_1, results presented Figure 2.29 shown that the activation energy of τ_2 is also around $0.8-0.9$eV.
- In section 2.2.7.2.1, hard mask integration shown that the carbon population at Al_2O_3/GaN interface has no influence on nBTI degradation related to τ_1 and τ_2.
- NBTI transients presented in Figure 2.36 depicted that the V_{TH} shift related to τ_2 occur later when the GaN:C is moved away from the gate. Consequently, τ_2 is also related to the GaN:C layer.
- Stress and recovery nBTI transients presented in Figure 2.38, and obtained by applying different $V_{GStress}$ tend to show that V_{TH} shift related to τ_2 is associated to free holes trapping in Al_2O_3 gate oxide. Consequently, the presence of a defect band in Al_2O_3 located below the GaN valence band can be considered.

2.2.7.3.3 Results interpretation

Considering the observations presented in sections 2.2.7.3.1 and 2.2.7.3.2, the following assumption is formulated. This latter can be described in five points defined below, and are also illustrated in Figure 2.39:

1. **At the beginning of the negative gate stress**
   For a sake of simplicity, a structure integrating an Al_2O_3 gate oxide and a GaN:C layers, both separated by a GaN:UID layer is considered. At equilibrium state, it is considered that the GaN:UID layer is naturally n-doped, while the GaN:C layer is considered as a p-doped layer since the C_N sites are deep acceptors. Therefore, the GaN:C/GaN:UID interface acts as a PN junction, and the GaN:C layer can be related to a free hole reservoir. At the onset of a negative gate stress, a space charge region from the gate to the bulk is opened. Since GaN:UID is very resistive, part of the space charge region also located in a part of GaN:C. The free holes both located in the GaN:C and the space charge region are naturally attracted to the gate. On the other hand, they cannot reach the interface since the PN junction at the GaN:C/GaN:UID interface acts as a potential barrier for them. Therefore, free holes are accumulated at the GaN:C/GaN:UID interface at the beginning of the negative gate stress.

2. **C_N trap deionization at τ_1**
   After a certain time of stress, $|\Delta V_{TH}|$ suddenly decreases revealing the first time constant τ_1. It corresponds to C_N sites deionization located at 0.8eV from E_V, which can can be also assimilated as a free hole trapping from the GaN:C valence band towards the C_N sites. This charge state modification of C_N sites imply the p-doped effect annihilation of GaN:C and induces a conduction band collapse within the structure, and thus a decrease of V_{TH}. Since the GaN:C p-doped effect is annihilated, the PN junction at GaN:C/GaN:UID interface is also suppressed. Consequently, there is no more free holes potential barrier at GaN:C/GaN:UID interface.

3. **Free hole current towards Al_2O_3/GaN interface**
   Once the PN junction at GaN:C/GaN:UID interface is removed, there is no more free holes potential barrier at GaN:C/GaN:UID interface. The free holes from the GaN:C are then able to move towards the Al_2O_3/GaN interface since they are attracted by the negative potential applied on the gate. Consequently, a hole accumulation occurs at Al_2O_3/GaN interface. It is worth noticing that the time τ related to this hole accumulation depends on the distance between the GaN:C and the gate oxide interface, such as $\tau = R \cdot C$. It thus explains why τ_2 occurs later when the GaN:C is moved away from the gate in Figure 2.36-right.

4. **Hole injection in Al_2O_3 defects band**
   As we consider the presence of a defects band in Al_2O_3 located below the GaN:UID valence band, the free holes accumulated in Al_2O_3/GaN are then captured by them. It then induces a local electrostatic modification leading to a $|\Delta V_{TH}|$ decrease revealing the second time constant τ_2. This underlying physical mechanism only occurs if the PN junction is suppressed at GaN:C/GaN:UID interface. Since this suppression only depends on the C_N sites which have an activation energy of $0.8-0.9$eV, the charge injection mechanism appearing at τ_2 also has an activation energy of $0.8-0.9$eV. In other words, once the C_N deionization mechanism related to τ_1 happens, it triggers the hole injection phenomenon related to τ_2.

5. **Overdrive voltage decrease within Al_2O_3**
   Once the hole injection related to τ_2 is triggered, the ΔV_{TH} start to decrease. However, this trapping mechanism depends on the electric field within the gate oxide that is proportional on the overdrive voltage $V_{ov} = V_{GStress} - V_{TH}$. If this latter value is not high

enough, the hole trapping dynamics will saturate. Since the V_{TH} decreases at a fixed negative $V_{GStress}$, the overdrive voltage automatically decreases as well as the electric field within the oxide. Therefore, the hole injection ends up saturating which explains the ΔV_{TH} plateau observed after τ_2.

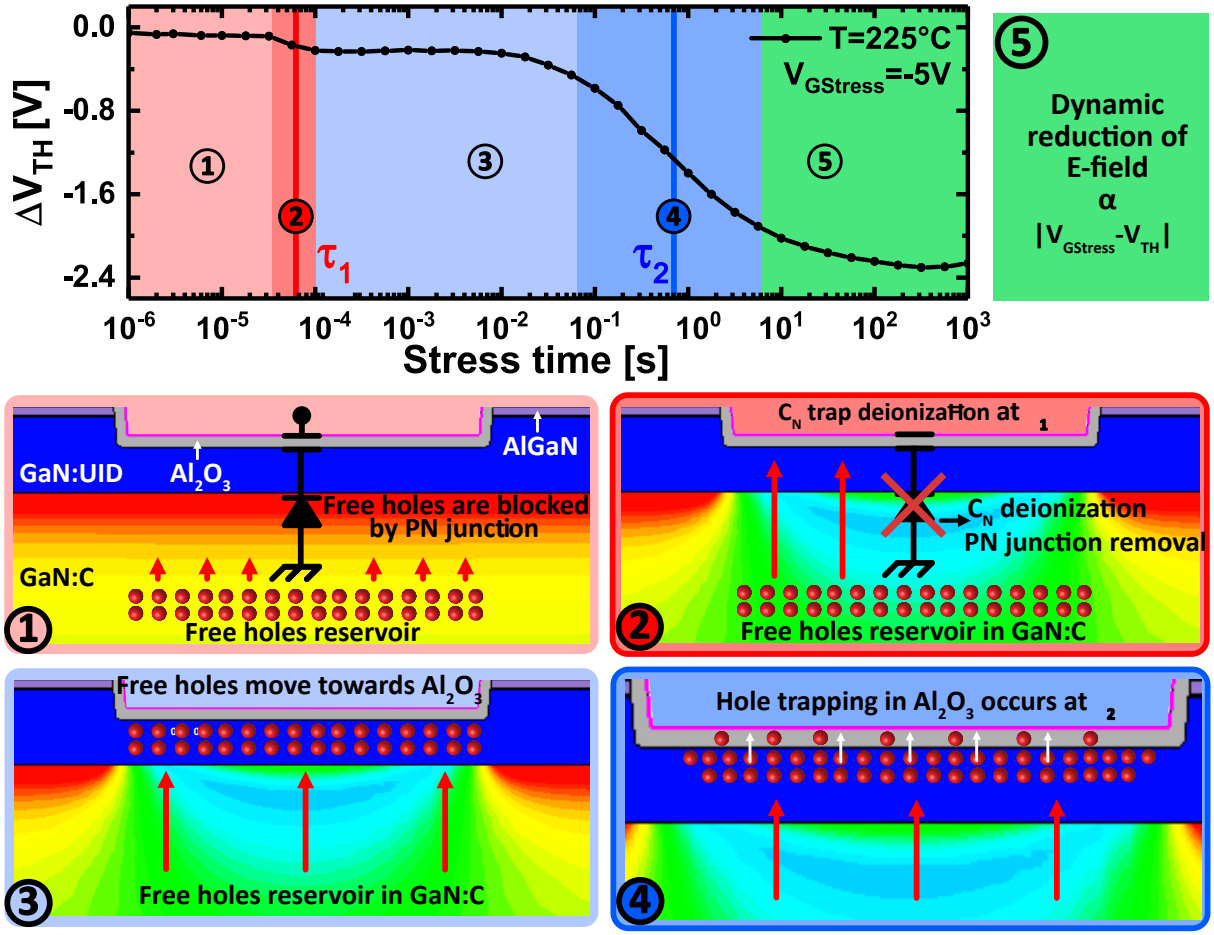

Figure 2.39. Illustration of the assumption explaining the nBTI degradation behavior. **1 -** GaN:C/GaN:UID interface acts as a PN junction, and the GaN:C layer can be related to a free hole reservoir. The free holes are naturally attracted to the gate due to its negative potential. However, they cannot reach the gate oxide interface since the PN junction at the GaN:C/GaN:UID interface acts as a potential barrier. **2 -** C_N sites deionization located at 0.8eV from E_V at τ_1. This charge state modification of C_N sites induces a p-doped effect annihilation of GaN:C and thus leads to a V_{TH} decrease. Since the GaN:C p-doped effect is annihilated, the PN junction at GaN:C/GaN:UID interface is also suppressed. **3 -** Once the PN junction at GaN:C/GaN:UID interface is removed, there is no more free hole potential barrier at GaN:C/GaN:UID interface. Consequently, a hole accumulation occurs at Al_2O_3/GaN interface since they are attracted by the gate. **4-** Hole trapping occurs within a defects band in Al_2O_3 located below the GaN:UID valence band at τ_2. Since the PN junction suppression only depends on the C_N charge state modification which has an activation energy of $0.8-0.9$eV, the charge injection mechanism appearing at τ_2 also has an activation energy of $0.8-0.9$eV. **5 -** Since V_{TH} decreases at a fixed negative $V_{GStress}$, the overdrive voltage automatically decreases as well as the electric field within the gate oxide. The holes injection finally saturates, which explains the ΔV_{TH} plateau observed after τ_2.

2.3 BTI degradation under positive gate voltage stress

In this section, the influence of the positive gate stress on the V_{TH} instabilities is studied in the case of a GaN-on-Si MOSc-HEMT developed at CEA-LETI. To do so, an analysis of pBTI transients performed at several temperatures reveals two traps populations which are C_N acceptors within the GaN:C layer, and defects in the gate oxide Al_2O_3. By studying the V_{TH} instabilities under several positive gate voltage stresses ($V_{GStress}$), we also noticed the possibility to isolate the involved underlying mechanisms in pBTI degradation. We also demonstrated that both trap populations lead to V_{TH} instabilities via different underlying mechanisms through TCAD simulations. At $V_{GStress}$ lower than 1.5V, the V_{TH} drifts are attributed to the ionization of the C_N traps localized at $0.8-0.9$eV above the valence band (E_V). For higher $V_{GStress}$, electron trapping also occurs in Al_2O_3 defects leading to a stronger ΔV_{TH} drift. These different aspects will be developed in the following sections.

2.3.1 Device description and experimental setup

In this study, the tested transistor architecture is similar to the previous section. An architecture representation of the GaN-on-Si MOSc-HEMTs developed in CEA-LETI is also given in Figure 2.40-left. Regarding the transistor design, all the tested devices are 8mm wide (W_G) while L_{GS} and L_{GD} are constant. The gate length is fixed to 1µm. The principle of the MSM pBTI technique under AC or DC stress is illustrated in Figure 2.40-right and is similar to the one used in Figure 1.64. A positive gate voltage stress $V_{GStress}$ is applied between 1µs and 10^3s at a constant temperature. During this stress phase, fast V_G ramps ($<$ 10 µs) are applied using a Keysight B1530 in order to monitor the V_{TH} drift while minimizing the unwanted recovery. Once the stress phase is finished, it is immediately ($<$ 10 µs) followed by the recovery phase, where the gate voltage stress is set to $V_{GStress} = 0$ V and the ΔV_{TH} recovery is measured using the same fast V_G ramps ($<$ 10 µs) from 10^{-6}s to 10^3s. Note that the drain voltage is set to 0V when $V_{GStress}$ is applied, while it is fixed at 100mV during fast $I_D(V_G)$ measurements. The threshold voltage is always extracted at a fixed current level of $I_D = I_0 \cdot W_G/L_G$ where $I_0 = 20 \cdot 10^{-9}$ A.

2.3.2 Study of pBTI degradation at different $V_{GStress}$

Stress and recovery pBTI transients obtained at room temperature for different $V_{GStress}$ from 0.25 to 5V are presented in Figure 2.41-left.

During the stress phase, a strong pBTI acceleration around 10s is visible for all $V_{GStress}$, revealing the time constant τ_s . When a $V_{GStress} \leq 1.5$ V is applied, the pBTI shift is negligible before τ_s. However, an abrupt positive V_{TH} variation can be observed at τ_s, followed by a stabilization, which gives rise to a ΔV_{TH} plateau. It can be also noticed that the plateau amplitude increases with $V_{GStress}$. On the other hand, when a high gate voltage stress ($V_{GStress} > 1.5$ V) is applied, the pBTI shift rises monotonously before and after the time constant τ_s with a strong ΔV_{TH} acceleration at τ_s. Moreover, an increase of the trapping dynamic as $V_{GStress}$ rises is also depicted. These strong V_{TH} variations related to τ_s are also shown on the $I_D(V_G)$ characteristics drift performed during a gate voltage stress of 1.5V and 5V in Figure 2.41-right.

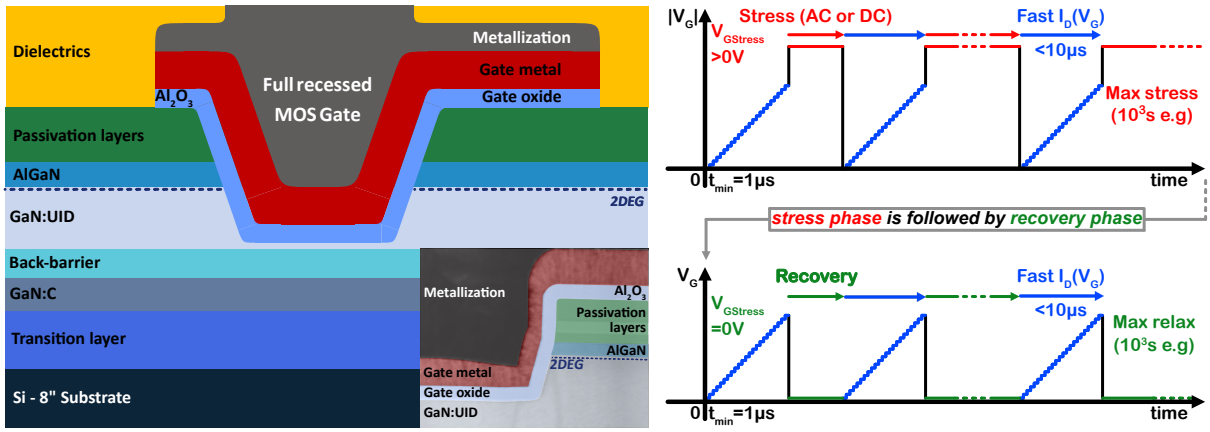

Figure 2.40. Left - Representation of the 8" GaN-on-Si E-mode MOSc-HEMT. The tested transistors are 8mm wide while the gate length L_G is 1µm. **Right -** PBTI measurement principle where ultra-fast V_{TH} measurements (< 10 µs) are performed during the stress (top) and recovery (bottom) phases in order to minimize the unwanted recovery. The stress phase ($V_{GStress} > 0$ V) is immediately followed by the recovery phase ($V_{GStress} = 0$ V).

During the recovery phase (Figure 2.41-left), an abrupt ΔV_{TH} reduction occurs at around 2s for all $V_{GStress}$ revealing a time constant τ_r. When a gate voltage stress below 1.5V is applied, it can be observed that ΔV_{TH} is very stable at the beginning of the recovery. Thereafter, it suddenly decreases at τ_r before becoming negligible. On the other hand, when a $V_{GStress} > 1.5$ V is applied, pBTI recovery transients start to decrease monotonously at low relaxation time ($\sim 10^{-4} - 10^{-3}$ s) and continue after τ_r. Moreover, a stronger ΔV_{TH} reduction at τ_r can be also noticed. Finally, it can be observed that the relaxation dynamic is more important after τ_r, and will be investigated in section 2.3.5.

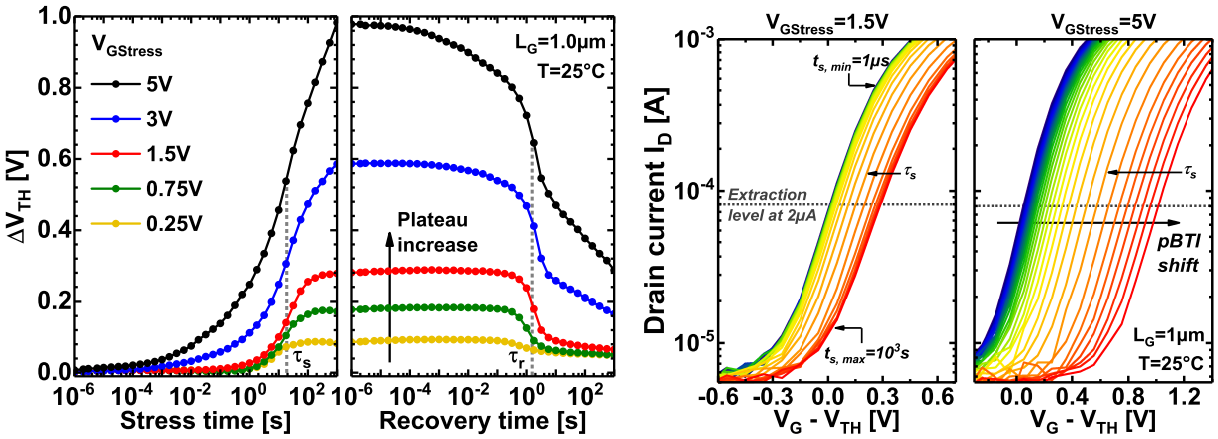

Figure 2.41. Left - Median curves of pBTI stress (left) and recovery (right) transients obtained at 25°C, and for $V_{GStress}$ from 0.25 to 5V. These measurements have been performed on 9 devices. **Right -** $I_D(V_G)$ characteristics carried out by applying a $V_{GStress}$ of 1.5V (left) and 5V (right) at 25°C. Four ultra-fast $I_D(V_G)$ measurements are performed per decade of stress time, with a minimum of $t_{s,min} = 10^{-6}$ s and $t_{s,max} = 10^3$ s, respectively.

As time constants τ_s and τ_r are both related to significant ΔV_{TH} variations and have the same order of magnitude, it is likely that they are associated with the same trap population. In order

to confirm this, and to get a better understanding of pBTI transient behavior, temperature dependent analysis will be presented in the next section.

2.3.3 Temperature dependent analysis

2.3.3.1 PBTI transients at different $V_{GStress}$

PBTI stress and recovery transients recorded at various temperatures from 25 to 175°C and at $V_{GStress} = 1.5$ and 3 V are presented in Figure 2.42.

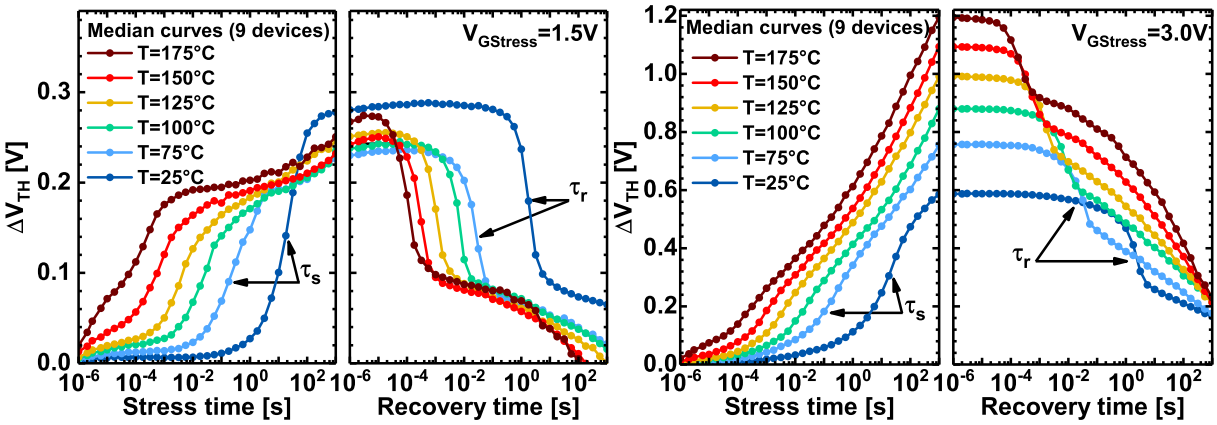

Figure 2.42. Median curves of pBTI stress and recovery (right) transients obtained at different temperatures from 25°C to 175°C. $V_{GStress} = 1.5$ V (left) and 3.0 V (right).

The pBTI transients obtained at low gate voltage stress ($V_{GStress} = 1.5$ V) in Figure 2.42-left show that τ_s and τ_r are strongly dependent on the temperature. Moreover, it can be noticed that at each temperature both time constants have the same order of magnitude, suggesting that they have the same activation energy. It is also clear that both time constants are related to the same ΔV_{TH} amplitude. These similarities indicate that τ_s and τ_r are probably correlated, suggesting that they are related to the same trap population.

On the other hand, stress and recovery pBTI transients obtained at a specific gate voltage stress of 3V (Figure 2.42-left) clearly show two different temperature dependencies. These observations suggest the presence of two different trap populations. One of these trap populations is related to time constants τ_s and τ_r, both of which strongly decrease with increasing temperature. As previously mentioned (Figure 2.41 and Figure 2.42-left), this first trap population is also visible when $V_{GStress} \leq 1.5$ V, leading to a strong and punctual ΔV_{TH} drift, followed by a stabilization. The pBTI signature of the second trap population only appears when the gate voltage stress is above $V_{GStress} > 1.5$ V (Figure 2.41). In Figure 2.42-right, the pBTI signature of this trap population is mainly observed after τ_s and τ_r during the stress and recovery phase, respectively. Although the temperature dependence of the second trap population is lower than the first one, it can be observed that the trapping rate increases with temperature. The monotonous pBTI drift associated with the second trap population is the image of a broad distribution of time constants related to an energy distributed trap population. In literature and as mentioned in section 1.4.3.1, this behavior is often explained by electron trapping into Al_2O_3 gate oxide

defects induced by forward gate stress [141], [302], [327], [329], [333], [339]–[342].

2.3.3.2 Arrhenius analysis of τ_s and τ_r

In order to investigate the relationship between τ_s and τ_r, and thereafter demonstrate if they are related to the same trap population, an Arrhenius analysis is performed. Both time constants are extracted using the same method exhibited in section 2.2.4.2. In a first time, the derivatives of stress and recovery pBTI transients $\partial\Delta V_{TH}/\partial\log(t)$ are plotted. The derivatives of stress and recovery pBTI transients for $V_{GStress} = 1.5$ V and 3 V are depicted in Figure 2.43-left and 2.43-right, respectively. The two resulting time constants τ_s and τ_r corresponding to extrema positions of the derivative curves were extracted at each temperature. This procedure has been applied for four different $V_{GStress}$ from 0.25V to 3V.

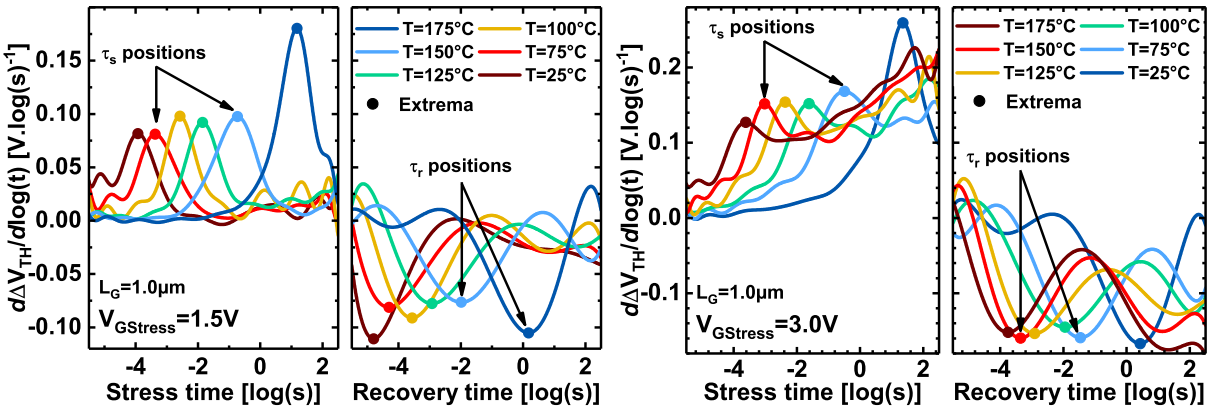

Figure 2.43. Extraction of time constants τ_s and τ_r corresponding to the local extremum of pBTI transient derivative curves at each temperature T, and for $V_{GStress} = 1.5$ V (left) and 3.0 V (right).

Figure 2.44 presents these Arrhenius plots where τ_s and τ_r are reported for different gate voltage stresses. It is worth noticing that the activation energy E_a of both time constants is around $0.8 - 0.9$eV for all $V_{GStress}$. As mentioned previously, several studies notably on current collapse phenomena demonstrated that this energy value is related to C traps in N sites of GaN lattice (C_N) acting as a deep acceptor around 0.8eV above valence band E_V [94], [95], [101], [104], [271], [343], [344]. In addition that τ_s and τ_r are related to the same trap population, these results also highlight that a C_N trap population is involved in pBTI degradation.

In the previous section, we have concluded that the two time constants τ_1 and τ_2 on nBTI transients are associated with C_N within the GaN:C layer. It can be noticed that τ_1 seems to have strong similarities with τ_s and τ_r. Indeed, in addition to have the same activation energy, these time constants have the same order of magnitude at a fixed temperature. Moreover, they are all associated with a strong ΔV_{TH} variation. Finally, it can be noted that the ΔV_{TH} amplitude associated with these three time constants have the same order of magnitude, i.e around $0.2 - 0.3$V. Therefore, we make the assumption that the time constants τ_s and τ_r are also associated with C_N traps located in the GaN:C.

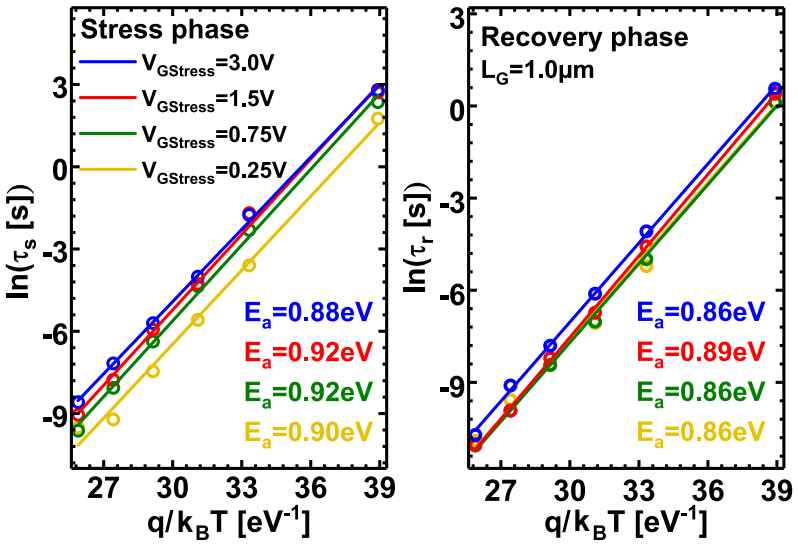

Figure 2.44. Arrhenius plots of time constants τ_s (left) and τ_r (right). Same activation energy $E_a \approx 0.8-0.9$ eV is found for both time constants and at different $V_{GStress}$. This activation energy value is related to C_N traps [94]–[96].

2.3.4 Physical underlying mechanism study through TCAD simulations

In this section, we will try to explain how these C_N traps can cause V_{TH} instabilities when a positive gate voltage stress is applied. Thereafter, we will also try to simulate the influence of the trapped electrons within the Al_2O_3 gate oxide defects on the V_{TH} instabilities.

2.3.4.1 Physical underlying mechanism of C_N traps

2.3.4.1.1 Experiment principle

In order to understand how C_N traps in the GaN:C layer can induce an increase in V_{TH} under a positive gate voltage stress, TCAD simulations similar to those presented in section 2.2.6.1 are performed. The simulated structure is exhibited in Figure 2.45 and is close to the one presented in Figure 2.31. It is composed of a GaN:C layer ($[C] = 5 \cdot 10^{18}$ cm^{-3}), a GaN:UID and Al_2O_3 gate oxide layers. This structure does not integrate a back-barrier layer for simplicity. In the simulation, the C-doping within the GaN:C layer is declared as a trap acceptor with an energy level at 0.8eV above the valence band, according to the literature. Note that the trapping and detrapping process have been simulated using Shockley-Read-Hall model.

Transient simulations are then performed on the structure presented in Figure 2.45. The simulation purpose is to compare the ionized C_N distribution at $V_G = 0$ V, obtained before and 1µs after positive gate voltage stress of 1.5V during 10^3s, as illustrated in Figure 2.46.

2.3.4.1.2 Simulation results

Concentration distributions of the ionized C_N trap in GaN:C layer before and 1µs after a positive gate stress of 10^3s at $V_G = 1.5$ V are depicted in Figure 2.47. By comparing these distributions, an increase of ionized C_N sites $(-)$ leading to a negative charge build up can be noticed after

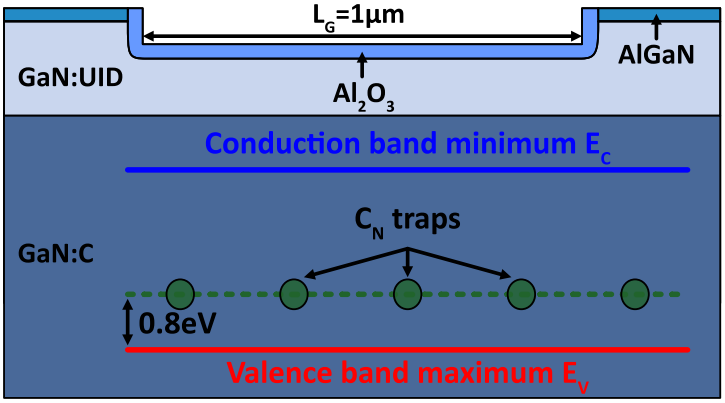

Figure 2.45. Structure representation simulated by TCAD. It is composed of GaN:C ($5 \cdot 10^{18} cm^{-3}$), GaN:UID and Al_2O_3 gate oxide layers.

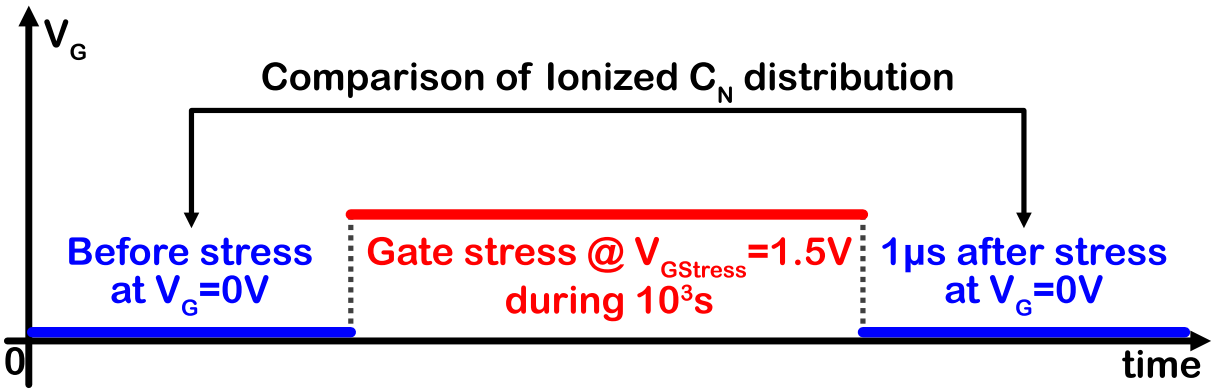

Figure 2.46. Transient simulations principle performed on the gate stack presented of Figure 2.31. Ionized C_N distributions at $V_G = 0$ V, obtained before and 1µs after gate voltage stress of 1.5V during 10^3s, are compared.

the application of stress. At the equilibrium state only a portion of all C_N traps is ionized, suggesting that the other part of C_N traps are neutral. When a positive gate stress is applied, the electron in GaN:C valence band are attracted by the gate, while the free holes within the GaN:C layer move away. Consequently, the neutral C_N traps are more likely to capture an electron which gives them the property of being ionized.

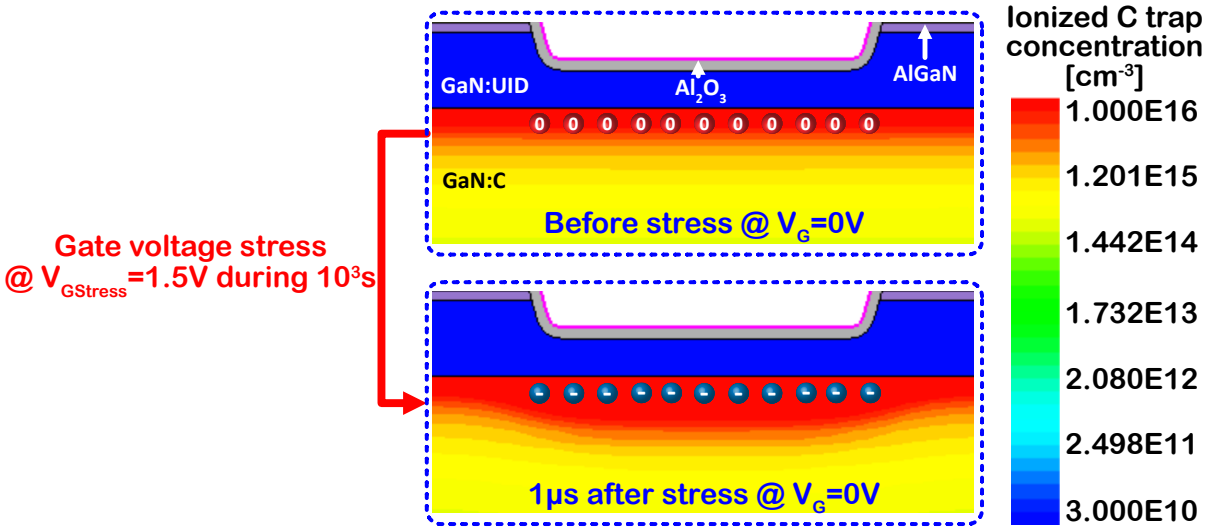

Figure 2.47. Transient simulations principle performed on the gate stack presented of Figure 2.31. Ionized C_N distribution at $V_G = 0$ V, obtained before and 1µs after gate voltage stress of 1.5V during 10^3s, are compared.

The electrical consequences of the C_N charge modification induced by a positive gate voltage stress are significant. Indeed, Figure 2.48 represents the profiles of the conduction band minimum (E_C) before and 1µs after the application of a forward gate stress, corresponding to the two distributions exhibited in Figure 2.47. An E_C increase at the Al_2O_3 gate oxide interface can be observed after positive stress, revealing a V_{TH} increase [101], [343]. This effect can be explained by the charge state modification of C_N sites during the stress implying a p-type doping-like effect. It then induces an important increase of GaN:C conduction band as well as an increase of the conduction band within the whole structure (Figure 2.48-left). It can be also observed (Figure 2.48-right), that the C_N trap ionization is coupled to an electric field increase within the gate oxide layer, indicated by the steeper slope of Al_2O_3 conduction band profile.

The C_N ionization, as well as the electric field increase in Al_2O_3, is not permanent and is maintained by the positive gate stress [104]. During the recovery, the system returns to the initial state as illustrated in TCAD simulations presented Figure 2.49. It shows the behavior of the E_C value under the middle of the gate oxide interface as a function of time, before, during and after a gate stress of 1.5V during 10^3s. It can be noticed that the initial E_C value is reached around 10^2s after stress, corresponding to the discharge time of the C_N sites to reach the initial equilibrium state. The C_N traps discharge is also coupled to an electric field reduction in the gate oxide. In section 2.3.5, we will see that this electric field reduction can be experimentally observed.

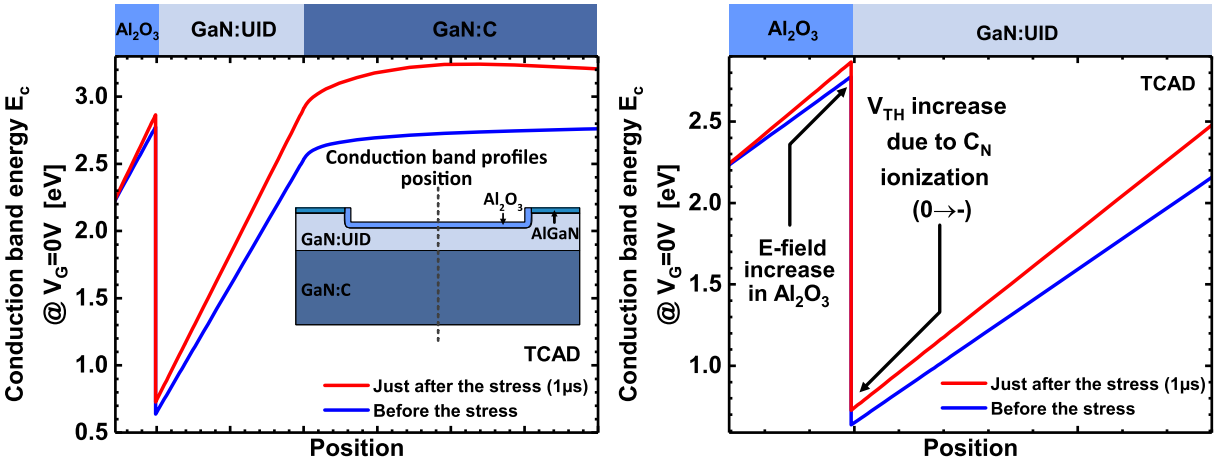

Figure 2.48. Left - Conduction band minimum (E_C) profile of the whole simulated structure before and 1µs after the application of a forward gate stress. A global conduction band increase can be noticed after the gate stress. **Right -** Same graph as presented at left, but by zooming on the gate oxide interface.

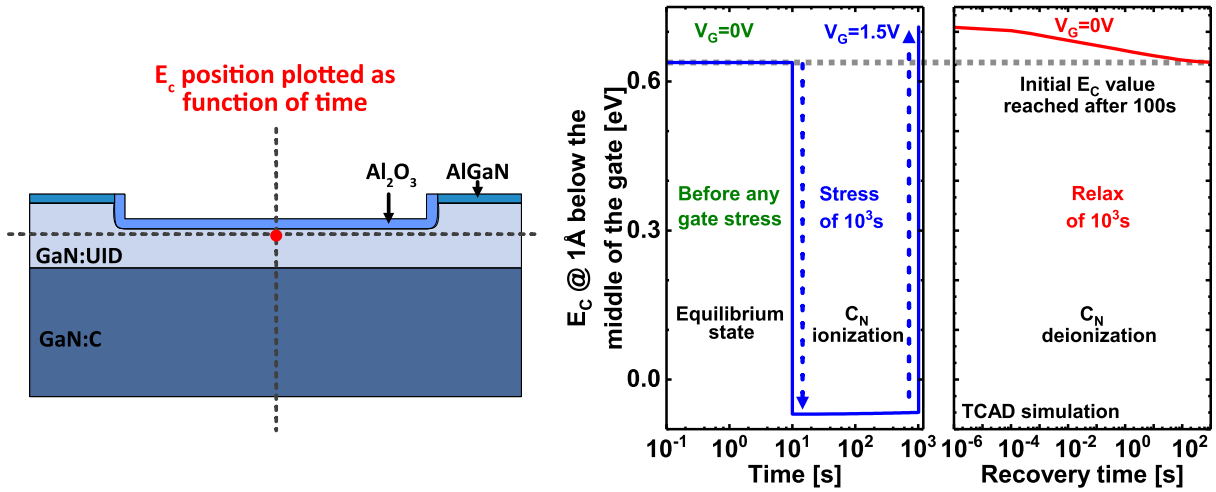

Figure 2.49. Conduction band energy value (E_C) calculated at 1Å below the middle of the gate before, during and after a stress of 10^3s at $V_{GStress} = 1.5$ V. The gate is grounded before and after the stress. A V_{TH} increase can be noticed just after the gate stress, compared to the initial V_{TH} value. This later is reached after 10s of recovery.

2.3.4.2 Physical underlying mechanism related to charge trapping in Al_2O_3

In this section, the electron trapping mechanism in Al_2O_3 defects for $V_{GStress} > 1.5$ V is simulated. To simplify, the trapped electrons are simulated using a negative and fixed charge surface Q_{fixed} at the Al_2O_3/GaN interface, as illustrated in Figure 2.50-left. The charge density N_{fixed} is set to $5 \cdot 10^{11} cm^{-2}$ such as $Q_{fixed} = q \cdot N_{fixed}$. The aim of this simulation is to observe the effect of this fixed charge surface on the threshold voltage. Simulated $I_D(V_G)$ characteristics in Figure 2.50-right highlight that the fixed charge surface induces a positive V_{TH} shift .

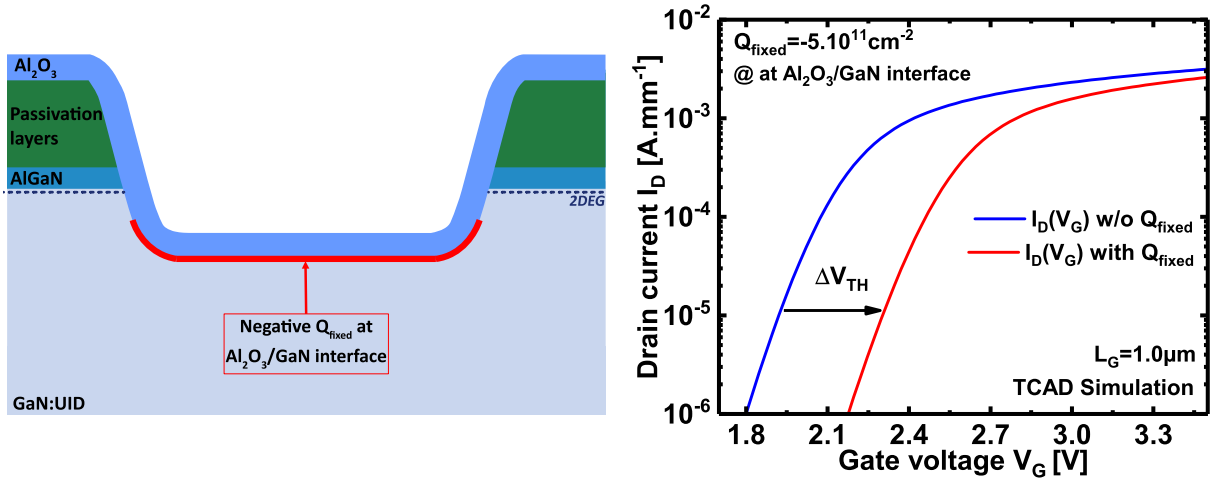

Figure 2.50. Left - TCAD simulation principle where trapped electrons in Al_2O_3 defects are simulated by a fixed negative charge Q_{fixed} at the Al_2O_3/GaN interface. **Right -** Simulated $I_D(V_G)$ characteristics showing that Q_{fixed} induces a positive V_{TH} shift.

2.3.5 Coupling between trapping mechanisms

In previous sections, it has been shown that pBTI degradation is driven by two effects: 1) C_N traps located in GaN:C layer, and 2) Al_2O_3 defects close to the gate oxide interface. According to TCAD simulations, both trap populations act through different underlying mechanisms. Indeed, a gate voltage stress below 1.5V is sufficient to activate the ionization of neutral C_N traps ($0 \rightarrow -$) leading to an increase of the conduction band energy at the Al_2O_3 gate oxide interface. On the other hand, an electron injection in Al_2O_3 traps is allowed energetically when a $V_{GStress} > 1.5$ V is applied. In this section, we will investigate whether the two degradation mechanisms are coupled, i.e. whether one of the two mechanisms influences the other.

Experimental pBTI recovery transient performed after a gate voltage stress of 5V during 10^3s at room temperature is shown in Figure 2.51. It can be observed that the electron detrapping accelerated after τ_r. This effect can be explained by the electric field reduction in the Al_2O_3 gate oxide induced by the C_N trap discharge ($- \rightarrow 0$), as illustrated in Figure 2.48 and 2.52.

Indeed, this reduction of electric field implies that the trapped electrons are less likely to remain in the oxide, thus leading to an increase of the charge detrapping probability from the Al_2O_3 traps. Conversely, when a positive gate stress is applied, the C_N traps in the GaN:C become ionized. As demonstrated in section 2.3.4.1.2, this ionization of C_N traps induces a global increase of the conduction band within the structure, implying a V_{TH} increase as well as an electric field

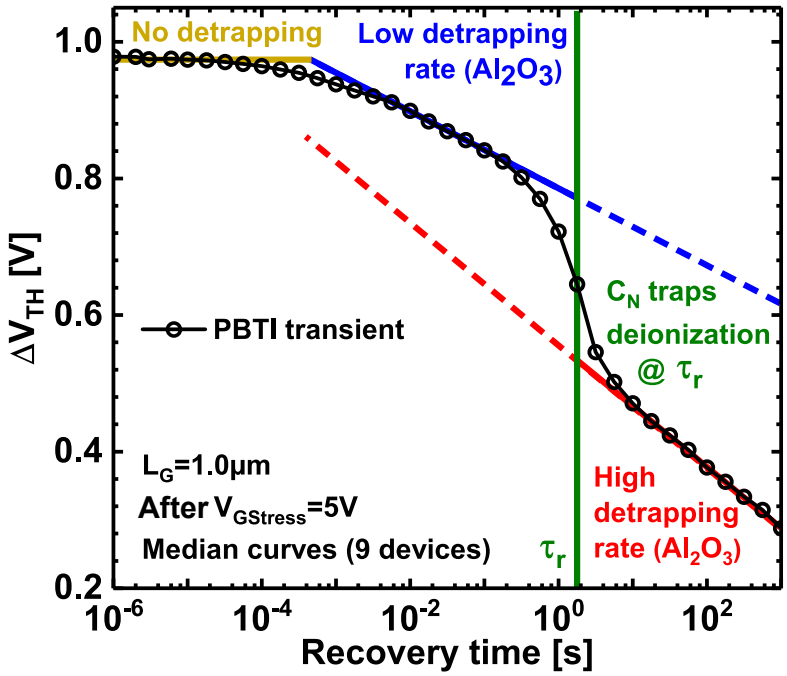

Figure 2.51. Experimental pBTI recovery transient performed at 25°C after $V_{GStress} = 5$ V. An acceleration of charge detrapping dynamics from Al_2O_3 defects can be noticed just after the C_N traps deionization. Charge state modification of C_N traps induces an electric field decrease in the Al_2O_3 gate oxide, leading to an increase of the charge detrapping probability of trapped electrons in Al_2O_3 defects.

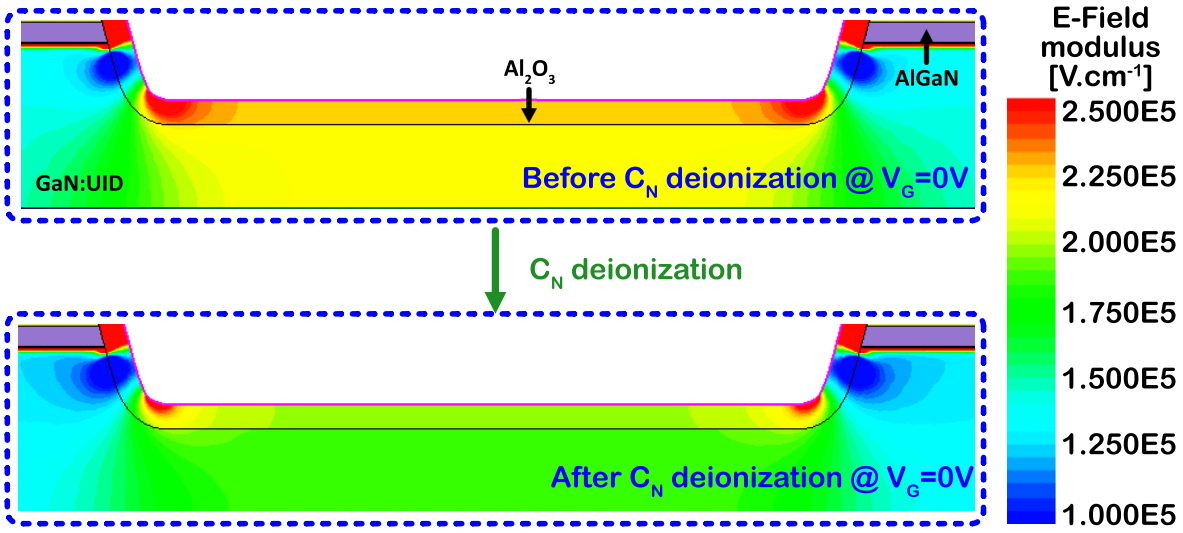

Figure 2.52. electric field distributions in the gate region obtained by TCAD simulations at a gate voltage of 0V. It illustrates the electric field reduction within Al_2O_3 gate oxide induced by the C_N traps discharge ($- \rightarrow 0$).

rise in the Al_2O_3 gate oxide layer. Consequently, the channel electrons are more likely to be trapped in the oxide defects, and C_N traps ionization should enhance the trapping rate during stress phase.

2.3.6 Overall understanding of pBTI degradation

Considering the main results of previous sections, pBTI degradation is due to the presence of C_N and Al_2O_3 trap populations. Both trap populations act via different underlying mechanisms and at different gate voltage stresses. Indeed, a low $V_{GStress}$ (< 1.5 V) is enough to activate the ionization of C_N traps that are initially neutral ($0 \rightarrow -$), leading to an increase of the conduction band energy at the gate interface. When a $V_{GStress} > 1.5$ V, electrons are injected in Al_2O_3 traps. Figures 2.53, 2.54 and 2.55 illustrate the charge states of Al_2O_3 defects band and C_N traps within the GaN:C layer after 10^3s of stress at different $V_{GStress}$. At the equilibrium state (Case 1), a part of C_N traps in the GaN lattice is already ionized ($-$) in order to be consistent with nBTI study presented in previous section 2.2.7.3.3, while the other part is neutral (0). On the other hand, Al_2O_3 trap states are fully neutral when $V_{GStress}$ is set to 0V.

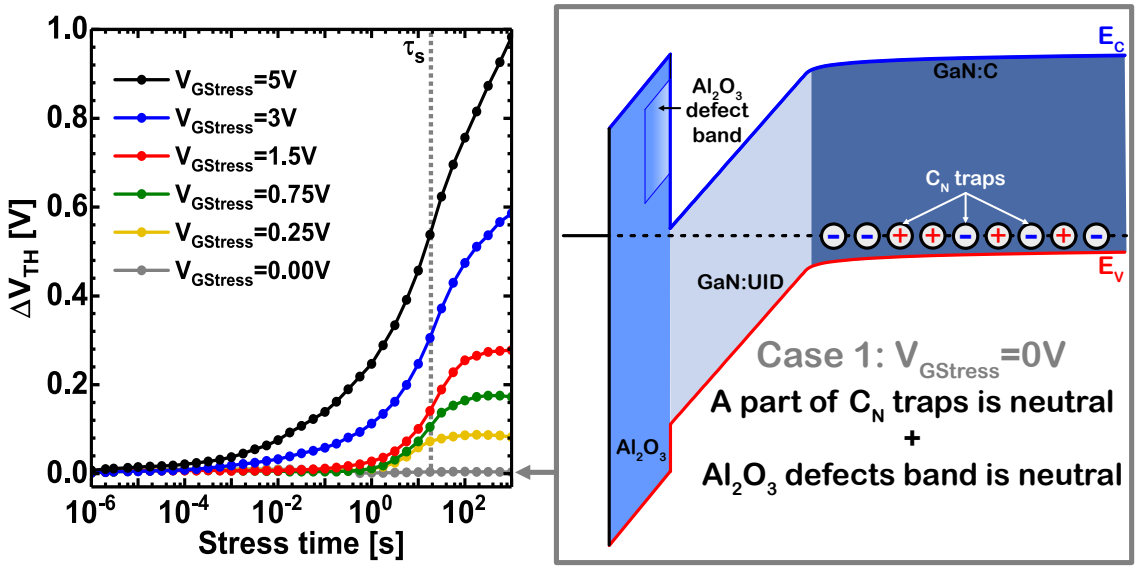

Figure 2.53. At the equilibrium state (Case 1), a part of C_N traps is already ionized ($-$) while the other part is neutral (0). The Al_2O_3 traps states at $V_{GStress} = 0$ V are fully neutral.

When $V_{GStress} \leq 1.5$ V is applied (Case 2), the electrons in GaN:C valence band are attracted by the gate, while the free holes within the GaN:C layer move away. Consequently, the neutral C_N traps are more susceptible to capture an electron which gives them the property of being ionized. This C_N site ionization thus leads to an increase of the GaN:C conduction band then inducing an E_C increase at Al_2O_3/GaN interface, and hence a V_{TH} increase. In this case, the E-field is too low to observe charge trapping in Al_2O_3 defects, which remain neutral.In Case 3, the pBTI shift obtained at high $V_{GStress}$ is the result of a combination between C_N ionization and charges injection in Al_2O_3 defects. Indeed, in this condition the electric field is enough to trigger an electron injection mechanism in the Al_2O_3 defects band, leading to a monotonous pBTI increase.

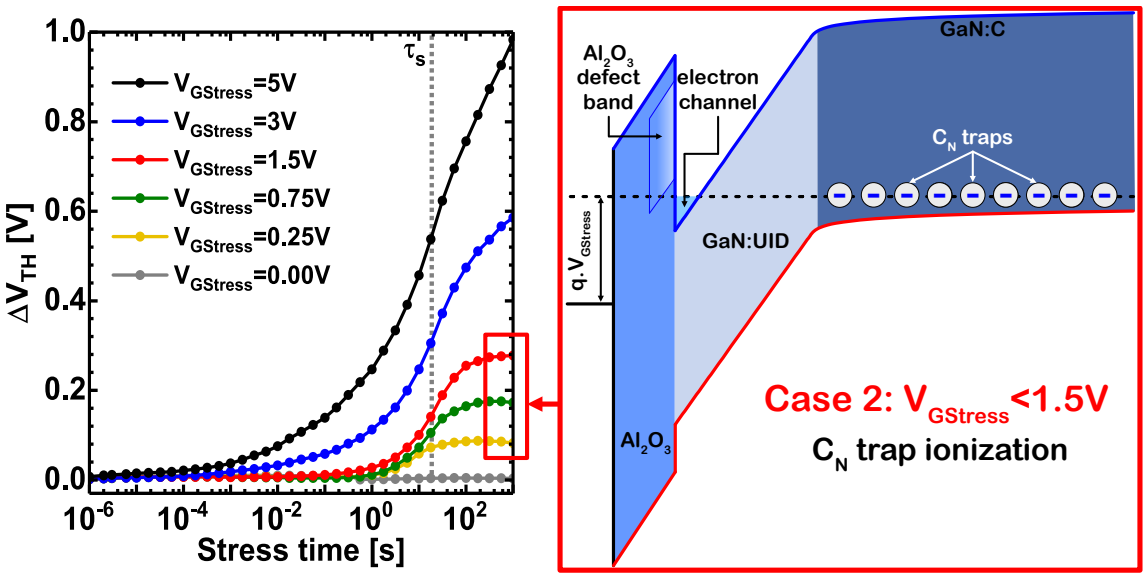

Figure 2.54. At $V_{GStress} < 1.5$ V (Case 2), the global conduction band increase within the substructure is due to C_N traps ionization, leading to a positive V_{TH} shift. However, the gate oxide electric field is too low to observe a charge trapping in Al_2O_3.

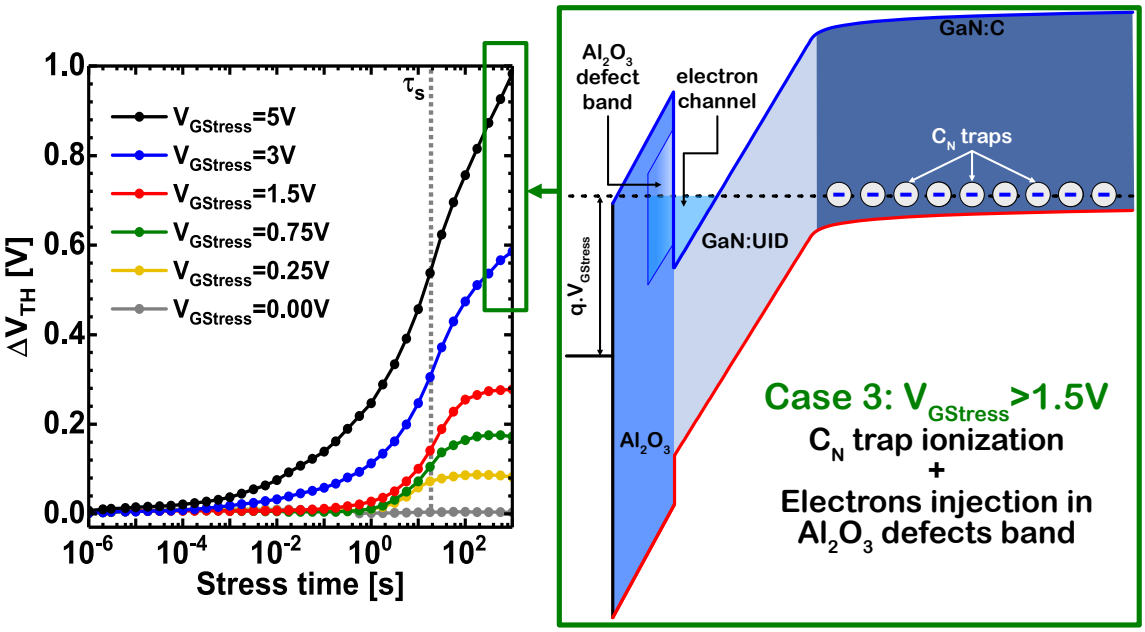

Figure 2.55. At $V_{GStress} > 1.5$ V (Case 3), the electric field is enough to obtain a monotonous positive V_{TH} drift induced by combination between C_N ionization and charge injection in Al_2O_3 defects. In other words, the alignment between the Al_2O_3 defect band and the channel leads to an electron trapping of the within the gate oxide.

Conclusion

In this chapter, an overview of the BTI degradation literature was first presented for two GaN-based transistor architectures, which are the MIS gate HEMT and the MOSc-HEMT. First, we have seen that nBTI degradation can occur on these two architectures. Regarding the MIS-HEMT architecture, Meneghini *et al.* explained this degradation by the presence of a defect band at the AlGaN/dielectric interface located around the Fermi level. When a negative gate voltage stress is applied, a part of the negatively charged traps move above the Fermi level and release an electron that transits towards the conduction band of GaN. It then induces a negative charge decrease at the AlGaN/dielectric interface leading to a V_{TH} decrease. Regarding the nBTI degradation on the MOSc-HEMT architecture, A. Guo and J. A. del Alamo also explained the V_{TH} negative drift by introducing a defect band around the Fermi level that is located at the Al_2O_3/GaN interface. In the same way as in the explanation given by Meneghini *et al.*, when the gate is subject to a negative voltage stress, a part of the initially charged traps rises above the Fermi level and releases electrons which go towards the conduction band of GaN. It then induces a V_{TH} decrease due to the negative charge decrease at the Al_2O_3/GaN interface. A. Guo and J. A. del Alamo also demonstrated that this mechanism does not induce permanent degradation and is perfectly recoverable. In a second step, we have seen that the pBTI degradation had also been studied on these two architectures. P. Lagger *et al.* have thoroughly studied this subject on the MIS-HEMT architectures. They also explained the pBTI degradation by defects present at the GaN/dielectric interface. When a positive gate voltage stress is applied, a part of the uncharged traps goes below the Fermi level and captures electrons from the channel that have transited through the barrier, which induces a V_{TH} increase. During the recovery phase, these same trapped electrons go back to the 2DEG without creating any permanent degradation. A. Guo and J. A. del Alamo also studied the pBTI degradation on MOSc-HEMT architecture, and according to them the Al_2O_3 defect band that induces nBTI degradation is also at the origin of the pBTI degradation. When the gate is subjected to a positive stress voltage, the electrons in the channel are trapped by the Al_2O_3 defects. This induces a V_{TH} rise which is fully recoverable during relaxation.

In a second time, an in-depth study on nBTI degradation was presented. The nBTI stress transients presented two time constants spaced by stable ΔV_{TH}. Temperature-dependent analysis indicated that the activation energy of τ_1 and τ_2 is about $0.8-0.9$eV, which is related to C_N traps in GaN substrate. A ToF-SIMS analysis revealed two populations of carbon traps. One at the Al_2O_3/GaN interface and the second one within the GaN:C layer. By moving the GaN:C layer away from the gate oxide interface, the nBTI transients showed that the V_{TH} shift related to τ_1 disappeared. Therefore, it was deduced that τ_1 is related to the GaN:C layer. Moreover, the V_{TH} shift related to τ_2 occurs later when the GaN:C is moved away from the gate. Therefore, the GaN:C layer impacts τ_2. It can also be noted that the hard mask integration showed that the carbon population at the Al_2O_3/GaN interface coming partly from the photoresist mask has no influence on the nBTI degradation related to τ_1 and τ_2. Finally, the nBTI stress and recovery transients obtained by applying different $V_{GStress}$ tend to show that the V_{TH} shift related to τ_2 is associated with the trapping of holes in the gate oxide Al_2O_3. Therefore, the presence of a defect band in the Al_2O_3 located under the valence band of GaN has been considered. Considering these different aspects, the following hypothesis has been formulated. At equilibrium state, the GaN:C layer can be assimilated to a free hole reservoir, where free holes that are naturally attracted towards the gate due to negative potential. However, holes cannot reach the gate oxide interface due to the PN junction at the GaN:C/GaN:UID interface that acts as a potential

barrier. When C_N sites deionization occurs, it induces an annihilation of the p-doping effect of GaN:C and thus leads to a ΔV_{TH} decrease related to τ_1. The PN junction at GaN:C/GaN:UID interface is also suppressed, allowing the free holes within from GaN:C layer to accumulate at the gate interface. This then induces free holes trapping in the gate oxide, which causes a second ΔV_{TH} drop corresponding to τ_2. It also induces an overdrive voltage decrease, proportional to the electric field within the gate oxide, which also slows the hole injection mechanism, until a ΔV_{TH} saturation is reached.

In the third part of the chapter, the positive gate voltage stress influence on the V_{TH} instabilities has been investigated. PBTI measurements at several temperatures and at various positive gate voltage stresses showed that the degradation of pBTI is induced by two trap populations. One of the two has been identified as the C_N traps located in GaN:C, while the second one is related to a defect band in the Al_2O_3, located above the GaN conduction band. These two populations induce a V_{TH} drift via different underlying mechanisms that are not activated at same gate stress voltage ranges. Indeed, a gate voltage stress lower than 1.5V is enough to activate the ionization of the neutral traps C_N ($0 \rightarrow -$) which leads to an increase of the GaN conduction band level at the Al_2O_3/GaN interface. It leads then to an abrupt V_{TH} variation. On the other hand, the electron injection mechanism in the Al_2O_3 traps is triggered at gate voltage stresses above 1.5V, and results to a monotonous V_{TH} increase with stress time. Finally, a coupling between the two trapping mechanisms has also been reported. Indeed, the charge state modification of the C_N sites induces a variation of the gate oxide electric field. This has the effect of varying the electron trapping rate in the Al_2O_3 defects.

3

Modeling of BTI transients

This chapter is dedicated to pBTI degradation modeling. In a first time, the Shockley-Read-Hall (SRH) model is explored. Since this latter model is inadequate for temperature-dependent pBTI degradation, the Non-Radiative Multi-Phonon (NRMP) model is explored. The NRMP model is then thoroughly described in the 2^{nd} section, as well as its ability to reproduce experimental BTI degradations. Since the NRMP model has some limitations for BTI modeling, the Capture Emission Time (CET) model is then explored and described in the 3^{rd} section. The 4^{th} section proposed an innovative method developed in this thesis to extract automatically CET maps. Finally, the results concerning pBTI modeling using the CET map model are presented in the 5^{th} section.

Contents

3.1 Shockley-Read-Hall model

In a first step, we will focus on a model where capture and emission are governed by the SRH (Shockley-Read-Hall) model. The model presented here is in A. Subirats's thesis [298] and has been adapted from the model proposed by X. Garros *et al.* [345] initially used in the frame of PBTI degradation. It deals with hole trapping (nBTI) in gate oxide.

3.1.1 Principle

Originally, the SRH model considers defects in the channel of a semiconductor [346]. It is assumed here that the defects are in the gate oxide and that their filling or emptying is performed by a tunneling transition of the holes present in the channel. In this model, it is also considered that when a trap captures a hole, it relaxes to get a more stable energy level. Thus, the trap energy level is noted E_t^i and its relaxation energy level E_r^i . Figure 3.1 illustrates the capture and emission mechanisms of holes from the channel to the oxide traps.

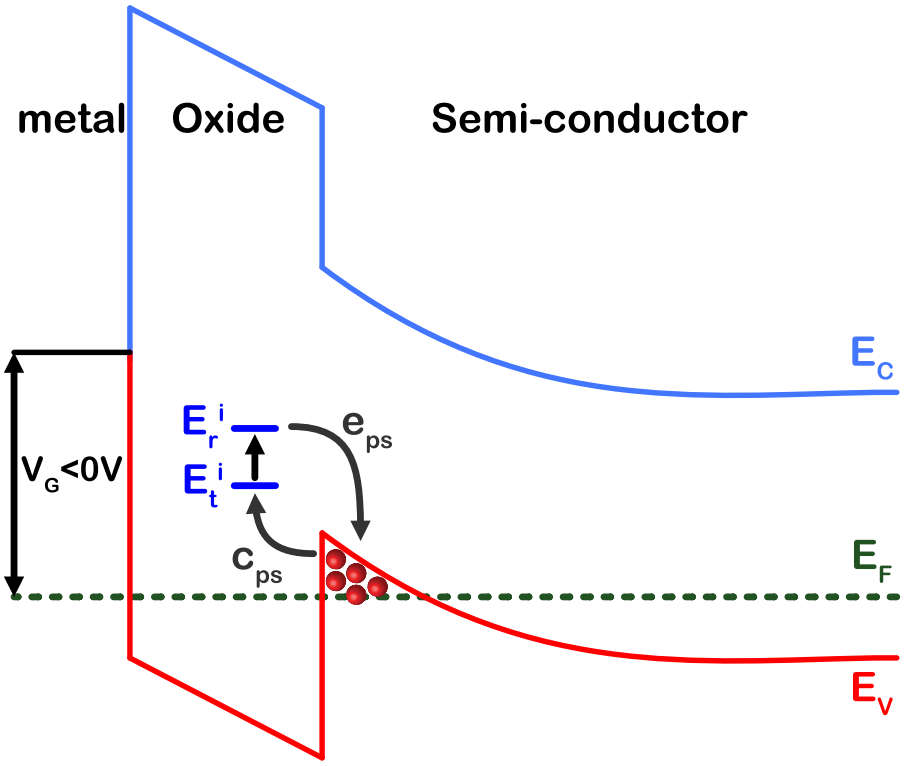

Figure 3.1. Holes capture by a trap located in the oxide during a negative gate voltage stress. A hole emission can also occur during equilibrium state (after negative stress).

In this model, the filling and emptying of the N traps within the oxide is governed by $N+1$ coupled differential equations. First, there are N differential equations governing the filling rate f_t of the N different oxide traps i such as,

$$\frac{\partial f_t^i}{\partial t} = c_{ps}(V_G,\, E_t^i,\, f_t)\cdot(1-f_t^i) - e_{ps}(V_G,\, E_r^i,\, f_t)\cdot f_t^i \tag{3.1}$$

With c_{ps} and e_{ps}, the capture and emission rates of the traps, respectively.

In addition to these latter N equations, it is necessary to consider a last equation which describes the electrostatics within the structure. It takes into account the modification of the electric field in the gate oxide layer induced by the filling and emptying of the various traps during stress and relaxation. This latter equation is given just below,

$$V_G = V_{FB} + \Delta V_{TH}(t) + \Psi_s(V_G) + V_{ox}(V_G,\, f_t, i) \tag{3.2}$$

With V_{FB} the flat band potential,
Ψ_s the surface potential,
and V_{ox} the potential within the gate oxide layer which is expressed by the following equation,

$$V_{ox}(V_G, f_t, i) = -\frac{Q_{SC}(V_G, f_t)\cdot(t_{ox} - x_t^i)}{\epsilon_{ox}} + q\sum_{k=1}^{i}\frac{N_t^k \cdot f_t^k \cdot (x_t^i - x_t^k)}{\epsilon_{ox}} \tag{3.3}$$

Where, Q_{SC} is the charge in the semiconductor,
x_t, the position of trap i,
N_t, the trap density,
t_{ox} is the gate oxide thickness,
and finally, ϵ_{ox} the oxide dielectric constant.
In equation 3.3, the first term represents the potential within the oxide without charge in the layer, while the second term represents the barrier shape modification due the charge trapping in the oxide.

Once f_t^i is obtained, the variation of the threshold voltage ΔV_{TH} with time is given by,

$$\Delta V_{TH}(t) = q\sum_{i=1}^{N}\frac{N_t^i \cdot f_t^i \cdot (t_{ox} - x_t^i)}{\epsilon_{ox}} \tag{3.4}$$

The remaining step to be able to use the model is to determine the characteristic time constants of the traps.

3.1.2 SRH model related time constant

The time constants that allow to calculate the filling of the traps are given by a simple tunnel model such as,

$$\frac{1}{\tau_c^i} = c_{ps} = v_{th}\cdot\sigma_p\cdot p_s(V_G)\cdot T(E_t^i, V_G) \tag{3.5}$$

$$\frac{1}{\tau_e^i} = e_{ps} = v_{th}\cdot\sigma_p\cdot p_s(V_G)\cdot T(E_t^i, V_G)\cdot\exp\left(\frac{E_t^i - E_r^i - E_F}{k_B\cdot T}\right) \tag{3.6}$$

With σ_p the hole capture cross section,
T_{tunnel} the tunnel transparency ,
E_F the Fermi level,
v_{th} the thermal velocity ,
and p_s the hole concentration in the channel at the gate oxide interface.

SRH model enables to obtain the capture and emission time constants of traps. However, the model is found to be independent of temperature. Indeed, c_{ps} and e_{ps} depend very little on temperature. However, it has been clearly shown, experimentally, that capture and emission process is related to an underlying-mechanism dependent on the temperature. This is why, it is preferable to consider another model to determine the capture and emission time constants of the traps.

3.2 Non-Radiative Multi-Phonon model

The Non-Radiative Multi-Phonon (NRMP) model initially proposed by B. K. Ridley [347] is currently one of the most accepted models to describe V_{TH} drifts. Tibor Grasser's work on the NRMP model has greatly contributed to the improvement of this model [297]. This model describes charges trapped in discrete energy states. Some derivatives of this model can take into account the effect of these charged traps on their local environment. Note that the process of charge exchange with a charge reservoir (2DEG) always induces a local electrostatic modification around the defect site, towards the new thermodynamic equilibrium [348]. The first applications of the NMP theory were related to the modeling of deep levels in semiconductors [349]. Modeling of V_{TH} drift transients with NMP transitions to oxide defects was first performed by T.L. Tewksbury *et al.* [350]. Nowadays, several derivatives of NRMP models can be found in literature [150]. In this section, we present the NRMP model proposed by Tibor Grasser in the frame of hole trapping modeling (nBTI) [323]. It can also be found in Subirats's thesis [298].

3.2.1 3-states NRMP model - Markov chains resolution

In this model, the oxide traps can be found in three distinct states (A, B and C):

- **State A** is related to the charge reservoir (channel), corresponding to the energy level E_{A0}. When the device is subjected to an electrical stress, the energy level E_{A0} increases which enables the charge transition to the two other states.
- **State C** corresponds to the stable oxide trap state. If this state is filled, the traps are charged. The trap energy level E_{C0} is arbitrary set to the energy reference, leading to get $E_{C0} = 0$.
- **State B** is ascribed to a meta-stable state, corresponding to a temporary state between stable states A and C. In this state, the charge can transit to state C via a lattice relaxation or go back to state A. The justification of the existence of this meta-stable state is due to the "switching" traps explaining the anomalous RTN signals [351].

As illustrated in Figure 3.2-left, the energies E_{A0}, E_{B0}, E_{C0} represent the energy levels of the traps in different states. The energies ϵ_{AB}, ϵ_{BA}, ϵ_{BC} and ϵ_{CB} correspond to the transition energies between the different states A, B and C.
The transitions between the different states can be described by Markov chains given in Figure 3.2-right during stress and relaxation phases. A Markov process is a stochastic process where the information useful for predicting the future event is entirely contained in the present state of the process and is independent of previous states [352].

In the stress configuration, the probability of a transition from state C to state B is almost zero [323]. In the same way, during the recovery, the probability for a charge to transit from state A to state B is also considered as negligible. The parameters a, b, c and d correspond to the transition rates of states A, B, C and B from states B, A, B and C respectively (Figure 3.2-right). In the case of a simple system with two states A and B, the time constants of emission and capture would be given by $\tau_e = a^{-1}$ and $\tau_c = b^{-1}$, respectively.

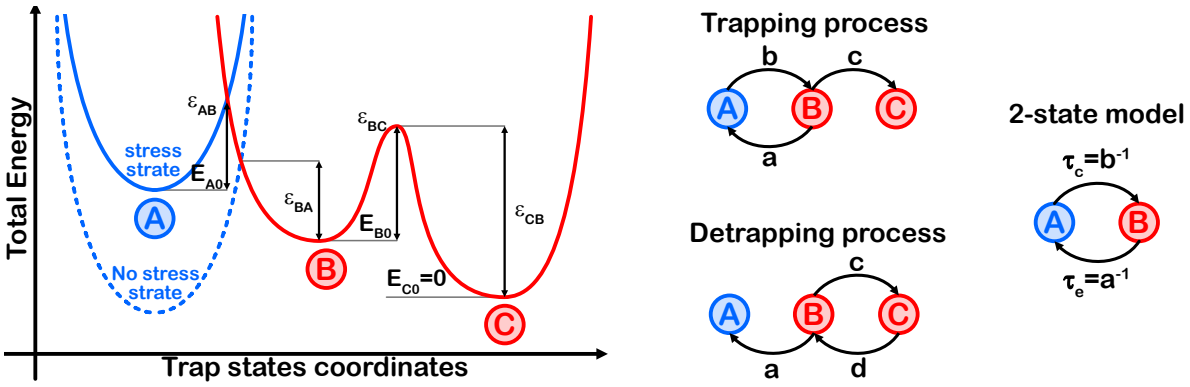

Figure 3.2. Left - Diagram showing the three states that a charge can occupy and the non-radiative transitions assisted by phonon between the different states. **Right -** Markov chain of a three-state system in the case trapping and detrapping process (left). In the case of a system with two states A and B, the time constants of emission τ_e and capture τ_c would be given by a^{-1} and b^{-1}, respectively (right).

It is possible to solve the latter Markov chains in order to obtain expressions of the capture and emission time constants. In the case of stress configuration (trapping process in Figure 3.2-right), the probabilities p_a, p_b and p_c of a trap being at states A, B and C, respectively, are expressed using differential equations such as,

$$\begin{cases} \dfrac{\partial p_a}{\partial t} = -b \cdot p_a + a \cdot p_b \\ \dfrac{\partial p_b}{\partial t} = b \cdot p_a - (a+c) \cdot p_b \\ \dfrac{\partial p_c}{\partial t} = c \cdot p_b \end{cases} \tag{3.7}$$

System 3.7 can be expressed in matrix form such as,

$$X' = M \cdot X \tag{3.8}$$

Where,

$$X' = \begin{pmatrix} p'_a \\ p'_b \\ p'_c \end{pmatrix}, \quad M = \begin{pmatrix} -b & a & 0 \\ b & -(a+c) & 0 \\ 0 & c & 0 \end{pmatrix}, \quad X = \begin{pmatrix} p_a \\ p_b \\ p_c \end{pmatrix} \tag{3.9}$$

After calculating the determinant such as $|M - \lambda \cdot I| = 0$, the eigenvalues λ_i are obtained, and are expressed as follows,

$$\begin{cases} \lambda_0 = 0 \\ \lambda_1 = \dfrac{-s + \sqrt{s^2 - 4 \cdot b \cdot c}}{2} \\ \lambda_2 = \dfrac{-s - \sqrt{s^2 - 4 \cdot b \cdot c}}{2} \end{cases} \tag{3.10}$$

Where $s = a + b + c$.

Consequently, the general solution of the equations system 3.7 can be written as follows,

$$\overrightarrow{X}(t) = \alpha_0 \cdot \exp(\lambda_0 \cdot t) \cdot \overrightarrow{U_0} + \alpha_1 \cdot \exp(\lambda_1 \cdot t) \cdot \overrightarrow{U_1} + \alpha_2 \cdot \exp(\lambda_2 \cdot t) \cdot \overrightarrow{U_2} \tag{3.11}$$

Where $\overrightarrow{U_i}$ are the associated eigenvectors of matrix M, and α_i are constant values to be determined. Using the eigenvalues, the eigenvectors are thus deduced,

$$\overrightarrow{U_0} = \begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix}, \quad \overrightarrow{U_1} = \begin{pmatrix} -\frac{\lambda_1}{c} - 1 \\ \frac{\lambda_1}{c} \\ 1 \end{pmatrix}, \quad \overrightarrow{U_2} = \begin{pmatrix} -\frac{\lambda_2}{c} - 1 \\ \frac{\lambda_2}{c} \\ 1 \end{pmatrix}$$

$$\Rightarrow \overrightarrow{U_0} = \begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix}, \quad \Rightarrow \overrightarrow{U_1} = \begin{pmatrix} \frac{s - 2\cdot c - \sqrt{s^2 - 4\cdot b\cdot c}}{2\cdot c} \\ \frac{-s + \sqrt{s^2 - 4\cdot b\cdot c}}{2\cdot c} \\ 1 \end{pmatrix}, \quad \Rightarrow \overrightarrow{U_2} = \begin{pmatrix} \frac{s - 2\cdot c + \sqrt{s^2 - 4\cdot b\cdot c}}{2\cdot c} \\ \frac{-s - \sqrt{s^2 - 4\cdot b\cdot c}}{2\cdot c} \\ 1 \end{pmatrix}$$

At the beginning of the trapping process, the traps are considered as empty contrary to the charge reservoir. Considering that the boundary conditions are set to $p_a = 1$, $p_b = 0$ and $p_c = 0$ at the initial state ($t = 0$). Injecting these conditions in equation 3.11 it is possible to deduce the constant values α_i such as,

$$\begin{cases} \alpha_0 = 1 \\ \alpha_1 = \dfrac{\lambda_2}{\lambda_1 - \lambda_2} \\ \alpha_2 = \dfrac{-\lambda_1}{\lambda_1 - \lambda_2} \end{cases} \tag{3.12}$$

Consequently, the general solution is expressed by,

$$\overrightarrow{X}(t) = \overrightarrow{U_0} + \frac{\lambda_2}{\lambda_1 - \lambda_2} \cdot \exp(\lambda_1 \cdot t) \cdot \overrightarrow{U_1} - \frac{\lambda_1}{\lambda_1 - \lambda_2} \cdot \exp(\lambda_2 \cdot t) \cdot \overrightarrow{U_2} \tag{3.13}$$

Finally, projecting the general solution 3.13 on the z-axis, the capture probability p_c is obtained (3.14). Note that the latter gives the probability of the oxide traps to be filled, it is thus the only one that is interesting among p_i. Indeed, p_a is related to the state of the charge reservoir while p_b is associated with a temporary meta-stable state between p_a and p_c.

$$p_c(t) = 1 - \frac{1}{\tau_{\lambda 2} - \tau_{\lambda 1}} \cdot \left(\tau_{\lambda 2} \cdot \exp\left(\frac{-t}{\tau_{\lambda 2}}\right) - \tau_{\lambda 1} \cdot \exp\left(\frac{-t}{\tau_{\lambda 1}}\right) \right) \tag{3.14}$$

where $\tau_{\lambda 1} = -\lambda_1^{-1}$ and $\tau_{\lambda 2} = -\lambda_2^{-1}$.

The probability density $g_p(\tau)$ that the charges transit from state A to state C in this 3-state model is given by:

$$g_p(\tau) = \frac{dp_c(\tau)}{d\tau} \tag{3.15}$$

$$\Rightarrow g_p(\tau) = \left(\exp\left(-\frac{\tau}{\tau_{\lambda 2}}\right) - \exp\left(-\frac{\tau}{\tau_{\lambda 1}}\right)\right) \cdot (\tau_{\lambda 2} - \tau_{\lambda 1})^{-1} \tag{3.16}$$

The average capture constant τ_c is given by the probability density expectation of $g_p(\tau)$ such as,

$$\tau_c = \int_0^{\infty} \tau \cdot g_p(\tau) \cdot d\tau \tag{3.17}$$

$$\Rightarrow \tau_c = \frac{1}{\tau_{\lambda 2} - \tau_{\lambda 1}} \cdot \int_0^{\infty} \left(\tau_{\lambda 2} \cdot \exp\left(\frac{-\tau}{\tau_{\lambda 2}}\right) - \tau_{\lambda 1} \cdot \exp\left(\frac{-\tau}{\tau_{\lambda 1}}\right)\right) \cdot d\tau \tag{3.18}$$

$$\Rightarrow \tau_c = \frac{\tau_{\lambda 2}^2 - \tau_{\lambda 1}^2}{\tau_{\lambda 2} - \tau_{\lambda 1}} = \tau_{\lambda 2} + \tau_{\lambda 1} \tag{3.19}$$

Writing the average capture time τ_c of the oxide traps as a function of acceptance rates (a, b and c), the following expression is obtained,

$$\Rightarrow \tau_c = \frac{a + b + c}{b \cdot c} = \frac{s}{b \cdot c} \tag{3.20}$$

In the same way, the average emission time τ_e of oxide traps during detrapping process can be also calculated by performing the same procedure. The expression of τ_e is given as follows,

$$\Rightarrow \tau_e = \frac{a + d + c}{a \cdot d} \tag{3.21}$$

The expressions of the capture and emission time constants associated to the traps in the 3-state NRMP model are thus obtained. In the next section, the expression of the time constants of an isolated trap will be calculated.

3.2.2 Time constant calculation

In this section, the two average time constants (τ_c and τ_e) of a single trap will be calculated. The acceptance rates a, b, c and d (Figure 3.2) are given by the following system in the frame of Boltzmann statistic,

$$\begin{cases} a = \sigma_s \cdot v_{th} \cdot p \cdot \exp\left(\frac{-q \cdot \epsilon_{BA}}{k_B \cdot T}\right) & \\ b = \sigma_s \cdot v_{th} \cdot p \cdot \exp\left(\frac{-q \cdot \epsilon_{AB}}{k_B \cdot T}\right) & \\ c = \frac{1}{\tau_{c,min}} & \text{In stress configuration (High Bias Path [323])} \\ d = \frac{1}{\tau_{e,min}} & \text{In recovery configuration (High Bias Path [323])} \end{cases} \tag{3.22}$$

With σ_s, the efficient charge capture section,
v_{th}, the thermal velocity of charges,

p_s, the free hole concentration,
And finally, the time constants $\tau_{c,min}$ and $\tau_{e,min}$ correspond to the thermal transitions that bound the global time constants.

Consequently, combining 3.22 with the expressions of τ_c (3.20) and τ_e (3.21), the latter can be expressed as follows,

$$\tau_c = \tau_{c,min} \cdot \left(1 + \frac{a}{b}\right) + \frac{1}{b} \tag{3.23}$$

$$\tau_e = \tau_{e,min} \cdot \left(1 + \frac{c}{a}\right) + \frac{1}{a} \tag{3.24}$$

The different rates (a, b and c) can be expressed in terms of the physical parameters of the model. Thus, after calculations, the different terms ($1/b$ and a/b) used in the expression of capture time constant τ_c (3.24) can be expressed as follows [323]:

$$\frac{1}{b} = \frac{\tau_0 \cdot N_V}{p_s} \cdot \exp\left(-\frac{R_\omega}{1+R_\omega} \cdot \frac{||\overrightarrow{E}|| \cdot x_t}{V_{TH}}\right) \cdot \exp\left(\frac{q \cdot \epsilon_R}{k_B \cdot T \cdot (1+R_\omega)^2} - \frac{q \cdot R_\omega \cdot (\Delta E_{A0} - \epsilon_{BC})}{k_B \cdot T \cdot (1+R_\omega)}\right) \tag{3.25}$$

$$\frac{a}{b} = \frac{N_V}{p_s} \cdot \exp\left(-\frac{||\overrightarrow{E}|| \cdot x_t}{V_{TH}}\right) \cdot \exp\left(-\frac{q \cdot (\Delta E_{A0} - \epsilon_{BC})}{k_B \cdot T}\right) \tag{3.26}$$

The expression of parameters c/a and $1/a$ used in the emission time constant τ_e are given below:

$$\frac{1}{a} = \tau_0 \cdot \exp\left(\frac{1}{1+R_\omega} \cdot \frac{||\overrightarrow{E}|| \cdot x_t}{V_{TH}}\right) \cdot \exp\left(\frac{q \cdot \epsilon_R}{k_B \cdot T \cdot (1+R_\omega)^2} + \frac{q \cdot (\Delta E_{A0} - \epsilon_{BC})}{k_B \cdot T \cdot (1+R_\omega)}\right) \tag{3.27}$$

$$\frac{c}{a} = \frac{1}{a \cdot \tau_{e,min}} \cdot \exp\left(\frac{q \cdot \epsilon_{BC}}{k_B \cdot T}\right) \tag{3.28}$$

Where $N_V = 2 \cdot \left(2 \cdot \pi \cdot m_h \cdot k_B \cdot T \cdot h^{-2}\right)^{3/2}$ is the effective valence band density,
m_h, is the hole effective mass ,
h, is the Planck constant such as $h = 2 \cdot pi \cdot \hbar$,
$\tau_0 = (N_V \cdot v_{th} \cdot \sigma_s \cdot \exp(-x_t/x_0))^{-1}$, is the time constant related to temperature-dependent auxiliary quantities which are independent to the electric field,
x_t, is the trap position in the 1D-structure,
$x_0 = \hbar \cdot (2 \cdot \sqrt{2 \cdot m_t \cdot \Phi_b})^{-1}$, is a constant obtained via the Taylor expansion of the tunneling coefficient in the WKB (Wentzel–Kramers–Brillouin) approximation. The parameter m_t is the hole tunneling mass within the potential barrier height Φ_b.
The parameter R_ω is a pulsation ratio such as $R_\omega = \omega_A/\omega_B$, where ω_i is the pulsation of defect i at minimum energy E_i.
The relaxation energy ϵ_R can be expressed by Huang-Rhys factor S such as $\epsilon_R = S \cdot \hbar \cdot \omega$. Huang-Rhys factor determines the number of phonons required to excite the harmonic oscillator in state i to reach the equilibrium position at state j.
The energy difference between the charge reservoir state E_{A0} and the trap state E_{C0} is given by $\Delta E_{A0} = E_{A0} - E_V$.

And finally, $\overrightarrow{E}$ is the electric field within the 1D-structure.

These expressions enable to evaluate the average time constants of capture and emission of the traps distributed in the oxide layer. The filling rate f_t calculation of each trap i over stress or recovery time is thus possible by solving the same differential equation (3.1) used in SRH model,

$$\frac{\partial f_t^i}{\partial t} = \frac{1}{\tau_c} \cdot (1 - f_t^i) - \frac{1}{\tau_e} \cdot f_t^i \tag{3.29}$$

Consequently, using this latter equation, it is possible to calculate the charge state (fill or empty)

of the traps over time. However, it should be noted that this model requires a large number of parameters to physically determine both time constants τ_c and τ_e of the traps. Among these parameters, a certain number of parameters are impossible to determine experimentally. In reality, they become "fitting" parameters and do not really have a physical meaning according to A. Subirats's thesis [298]. The values of the parameters used to run the model are those given by Tibor Grasser in [323].

3.2.3 NRMP simulation - Examples

3.2.3.1 Simulation of an AC gate voltage stress

In this section, simulation results of the NRMP model from Subirats' thesis [298] are presented, where a modeling of the nBTI experimental results obtained on a classical silicon pMOS is considered. Note that the gate stack is composed of an inter-layer (IL) between a high-κ layer (HK) and the silicon. The first simulation result presents the increase of the BTI degradation during an AC negative gate voltage stress of -2V, at a frequency $f = 100$ kHz. ΔV_{TH} results calculated by simulations at the end of various stress time decades are reported in Figure 3.3. It shows the behavior of the simulated ΔV_{TH} transients during the last period of the AC gate voltage stress. The initial ΔV_{TH} at the beginning of the last period is determined by the AC stress previously applied [298].

During each period of AC gate voltage stress, the simulations exhibit a ΔV_{TH} degradation increase during the first half period, corresponding to the time when the voltage stress is applied. This latter is directly followed by a ΔV_{TH} decrease during the second half period, related to moment where $V_{GStress}$ is set to 0V. It can be also noticed that there is a global ΔV_{TH} increase with the number of periods, although the traps have capture time constants much higher than the half stress periods applied during the AC stress. Indeed, τ_c is 2s for a trap located in the middle of the oxide layer at an energy level $E_t - 0.6$eV. These results are consistent with experimental behavior, and qualitatively reproduce the cumulative property of BTI degradation which is rather well explained by the CET map model in section 3.3 [298].

3.2.3.2 NRMP simulations at different $V_{GStress}$

In this section, the traps behavior is simulated by applying a gate voltage stress pattern composed of four different voltage levels of 10s, from -2V to -1.4V, as shown at the top of

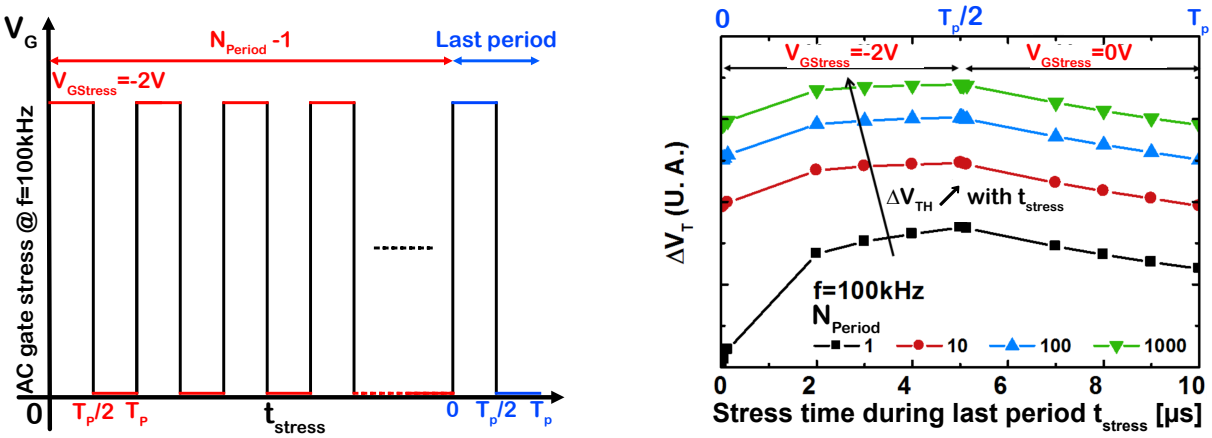

Figure 3.3. Right - Chronogram illustrating the gate voltage stress pattern applied to obtain the simulation results. **Left -** Simulation of the nBTI degradation obtained during the first period of AC stress (Black), the tenth period (Red), the hundredth period (Blue) and the thousandth period (Green) [298].

Figure 3.4. The band diagram for the first stress level ($V_{GStress} = -2$ V) and the last stress level ($V_{GStress} = -1.4$ V) are at the bottom of Figure 3.4-left and right, respectively. Finally, the nBTI degradation simulations obtained with the NRMP model are presented in Figure 3.4-center. It can be observed that the model is able to reproduce the experimentally observed behavior, such as the recovery after the first 10s of stress at $V_{GStress} = -2$ V for example. Indeed, depending on their energy level, some traps with an energy $E_t - E_V = 0.85$ eV capture a hole during the first 10s of stress and re-emit it during the successive changes of gate voltages stress from -2.0V to -1.4V [298], [334].

For example, considering the traps with energy $E_t = -0.85$ eV, the Figure 3.5 shows the filling rate of these traps during the first three phases of the pattern according to their position in the oxide. The Figure depicts that during the first 10s of stress at $V_{GStress} = -2$ V a part of the traps is filled, notably the ones farthest from the interface. During the following stress phases, the traps closest to the interface will tend to discharge with the decrease of the gate stress voltage. These results confirm that the NRMP model enables to describe the recorded nBTI degradation. They also show that the filling of the traps is governed by the Fermi level, and enable to explain the experimental results of nBTI degradation [298], [334].

3.2.4 Limitations

These previous sections have shown that the NRMP model is exclusively based on trapping, itself governed by the Fermi level. It allows to explain qualitatively the experimental results of nBTI degradation obtained on our transistors. However, the objective of the model is to be able to explain perfectly the nBTI degradation obtained experimentally. In particular, the set of nBTI transients measured during a stress and recovery phase. More concretely, the NRMP model must be able to reproduce the measured nBTI stress and relaxation kinetics. In order to test the model, nBTI DC stress measurements at $V_{GStress} = -2$ V for 10^3s followed by a 10^3s relaxation at $V_{GStress} = -1.8$ V were performed in [298]. This experiment can be seen as a two-step pattern, (comparable to the experiment presented in Figure 3.4), during which the

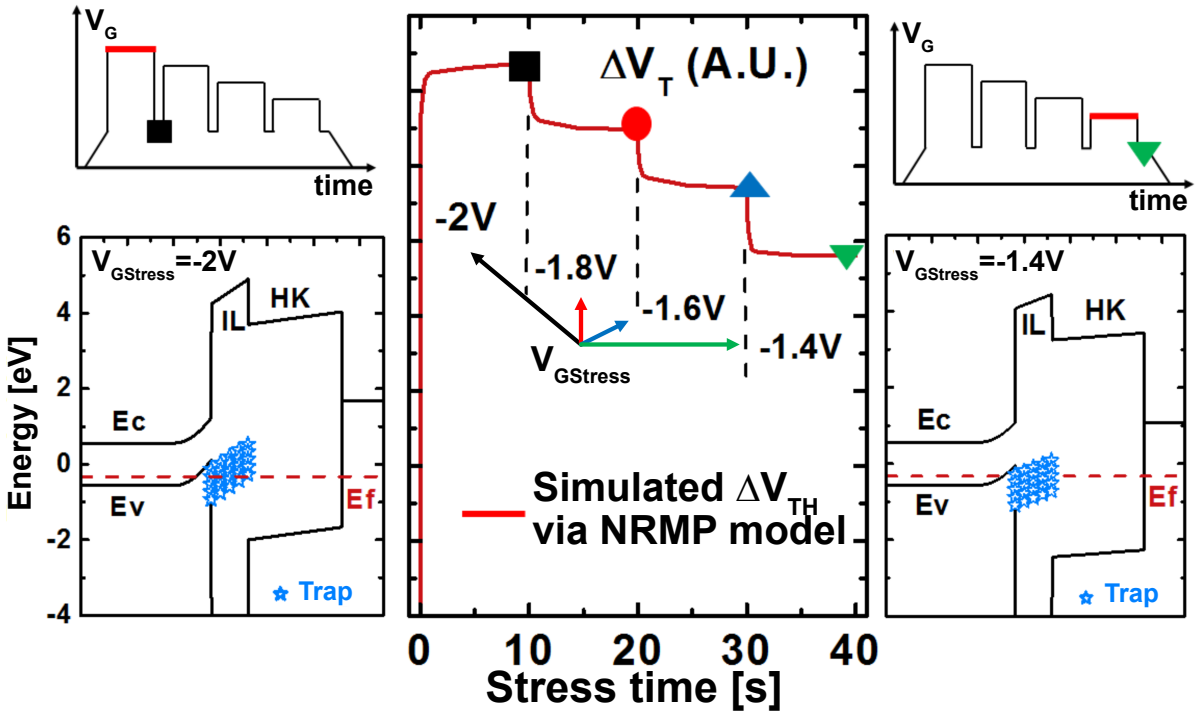

Figure 3.4. Left - The energy band diagrams for the first 10s of the pattern, corresponding to a DC $V_{GStress}$ of -2V. **Center -** Simulation of nBTI degradation during the application of the 4-stage gate voltage stress pattern using the NRMP model. **Right -** The energy band diagram at the end of the pattern, corresponding to a DC $V_{GStress}$ of -1.4V [298], [334].

V_{TH} drift is measured. These measurements give the stress and relaxation transients, and are presented in Figure 3.6. Keeping the same simulation parameters as those used in the previous section (3.2.3.2), simulations using the NRMP model were calculated, which are also reported in Figure 3.6.

It can be noticed that it is possible to reproduce the global degradation behavior (increasing or decreasing). Indeed, the ΔV_{TH} decrease during the relaxation phase can be reproduced by the model despite the high gate voltage applied ($V_{GStress} = -1.8$ V). However, the dynamics obtained from the model do not fit with the experiment. Although the degradation levels after stress as well as after relaxation are relatively well predicted by the model, the trapping and detrapping kinetics predicted by the model do not reproduce the nBTI transient dynamics obtained experimentally [298].

According to A. Subirats in [298], this poor evaluation of the stress and relaxation kinetics comes from the too many parameters required to run the model, and in particular to calculate the capture and emission time constants of the traps. As a result, this model seems inadequate to describe more complex phenomena, such as nBTI transients obtained via an arbitrary gate voltage stress for example [298], [334], [353]. For this reason, the NRMP model was not chosen to reproduce the BTI degradation obtained on GaN-based HEMTs. In the following section, we will focus on another model where the trap time constants are considered as an input parameter of the model rather than the result of a physical model with too many parameters. Although this latter model less describes the physical reality and underlying mechanisms of BTI degradation, we will see that it is very useful to model and predict V_{TH} instabilities [298].

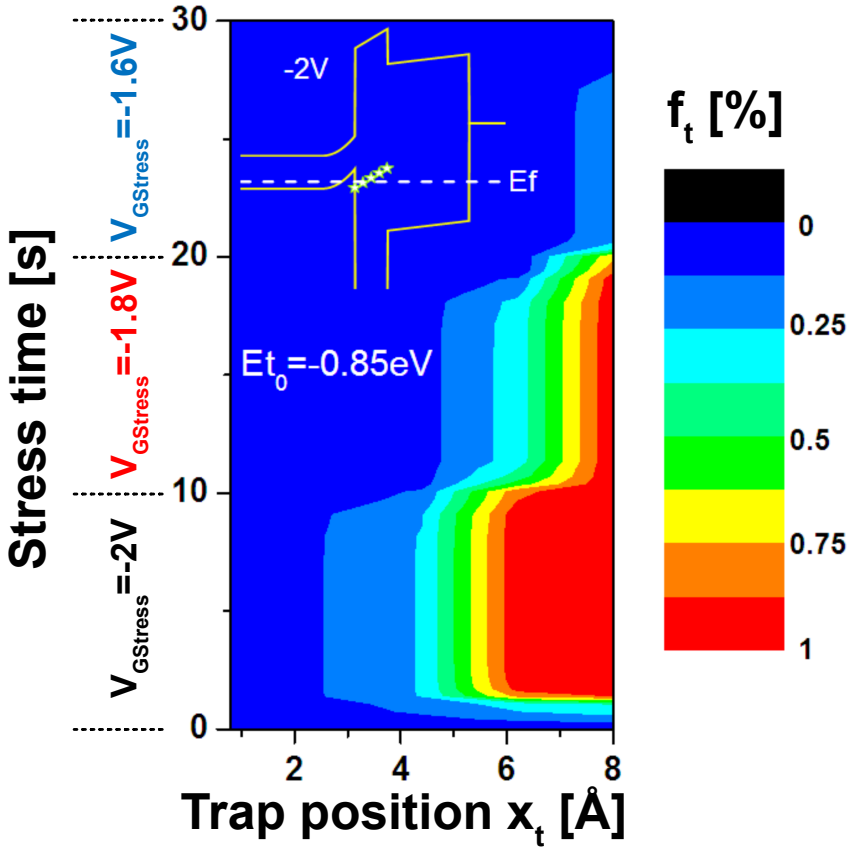

Figure 3.5. NRMP simulation of the filling rate of the energy traps $E_t = -0.85$ eV during the first three phases of the 4-stage pattern ($V_{GStress} = -2$, -1.8 and -1.6 V). It can be noticed that a high $|V_{GStress}|$ favor to fill the traps away from the gate oxide interface [298], [334].

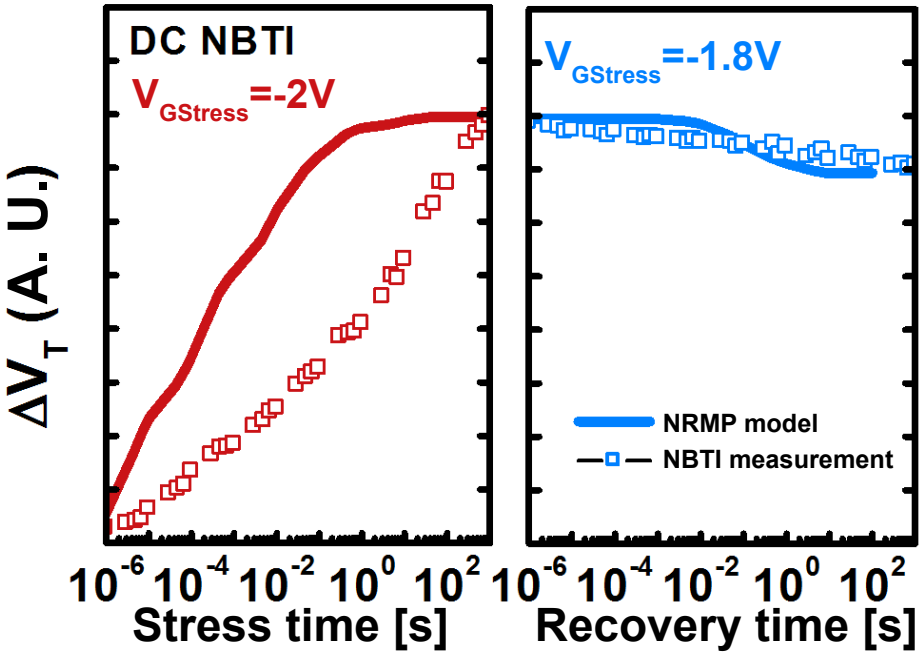

Figure 3.6. Comparison between experimental results and NRMP model. **Left -** NBTI stress transients obtained by applying a $V_{GStress}$ of -2V during 10^{-3}s. Right - NBTI recovery transients obtained by applying a $V_{GStress}$ of -1.8V during 10^{-3}s [298], [334].

3.3 Capture Emission Time map model

In the previous section, we have seen that a trap model was able to explain the stress and relaxation phases of nBTI AC stress. The NRMP model established by Tibor Grasser is able to explain qualitatively the experimental results. However, A. Subirats's thesis [298] showed that the large number of parameters required to run the model led to a poor evaluation of the time constants. For this reason, another way was considered to model the BTI degradation on the GaN-based devices. In the following, we will consider the Capture Emission Time map model where the time constants are not physically determined, but are consider as input parameters of an RC model, first proposed by Hans Reisinger in 2010 [354] and then updated in 2011 [355].

3.3.1 RC model principle

In the previous sections, we have seen that the SRH and NRMP models use the same differential equation (3.1 and 3.29) to calculate the filling of a trap such as,

$$\frac{\partial f_t}{\partial t} = \frac{1 - f_t}{\tau_c} - \frac{f_t}{\tau_e} \tag{3.30}$$

The difference between those latter models (SRH, NRMP and CET map model) relies in the time constant determination. In the case of CET map model the constant time τ_c and τ_e of a single trap are given by an RC circuit. This electric circuit, illustrated in Figure 3.7-left, model a single trap where the charge and discharge of the capacitor C can be compared to the charge and discharge of a single trap. Both time constants are independently defined by the resistance R_c and R_e, such as $\tau_c = R_c \cdot C$ and $\tau_e = R_e \cdot C$. The differential equation governing the voltage acrross the capacitor U is given by the following equation.

$$\frac{\partial U}{\partial t} = \frac{1 - U}{\tau_c} - \frac{U}{\tau_e} \tag{3.31}$$

It can be noticed that the latter equation 3.31 is similar to the one solved by the NRMP and SRH models (3.1 and 3.29) to calculate the filling of a single trap. By analogy, the RC model principle developed by Hans Reisinger [355] is to consider each trap present in the gate oxide of the transistors as an individual RC electric circuit.

In this RC model, all the traps are considered in a network of RC circuits where each RC sub-circuit represents a single trap, as shown in Figure 3.7-right. In this RC network, all combinations of time constant couple (τ_c, τ_e) exist, but each pair is unique. The emission and capture time constants of each trap are set as input parameters of the model, and U (i.e the trap filling rate) of the different traps is calculated via equation 3.31. The influence of each trap on the V_{TH} is represented by the capacitance. As the transistors studied have a large surface area, it is considered that all traps have the same impact on the V_{TH}, i.e. the same capacitance [354].

Considering the circuit given in Figure 3.7-right, the filling probability of each trap can be calculated via an analytical formula which will be demonstrated. In this model, filling probability of a trap is represented by the voltage across the capacitor U. When a normalized gate voltage stress V_H is applied, the filling probability of a trap over the stress time t_{stress} is given by solving the following differential equation,

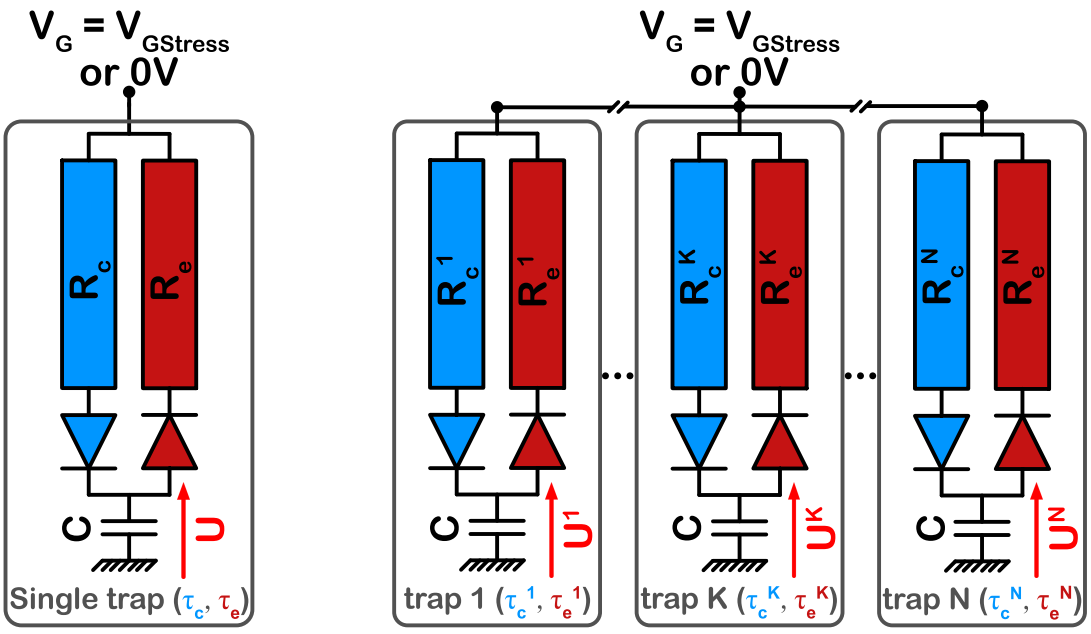

Figure 3.7. Left - Equivalent RC circuit modeling a unique trap. **Right -** Representation of the RC circuit network. Each trap k has a capture and emission time constants determined by the resistances R_c^k and R_e^k, respectively. All the couple τ_c and τ_e are present in this network, but each couple is unique. [298], [354].

$$V_H = R_c \cdot C \cdot \frac{dU}{dt} + U \tag{3.32}$$

$$\Rightarrow U(t_{stress}) = U(t_{stress} = 0s) \cdot \exp\left(1 - \frac{-t_{stress}}{\tau_c}\right) \tag{3.33}$$

In the same way, the detrapping probability over the recovery time t_{relax} is given by solving the following differential equation,

$$0 = R_e \cdot C \cdot \frac{dU}{dt} + U \tag{3.34}$$

$$\Rightarrow U(t_{relax}) = U(t_{relax} = 0s) \cdot \exp\left(\frac{-t_{relax}}{\tau_e}\right) \tag{3.35}$$

Equations 3.33 and 3.35 enable to calculate the charge and discharge probability of the traps during a DC gate voltage stress, respectively. However, we will see in the following section that it is possible to find an analytical formula to calculate the charge state of the traps during both AC and DC gate stress.

3.3.2 Trap state determination when applying either an AC or DC gate stress

In this section, the analytical expression enabling the charge state determination of the traps during an AC gate voltage stress is demonstrated [298]. Figure 3.8 shows the two equivalent

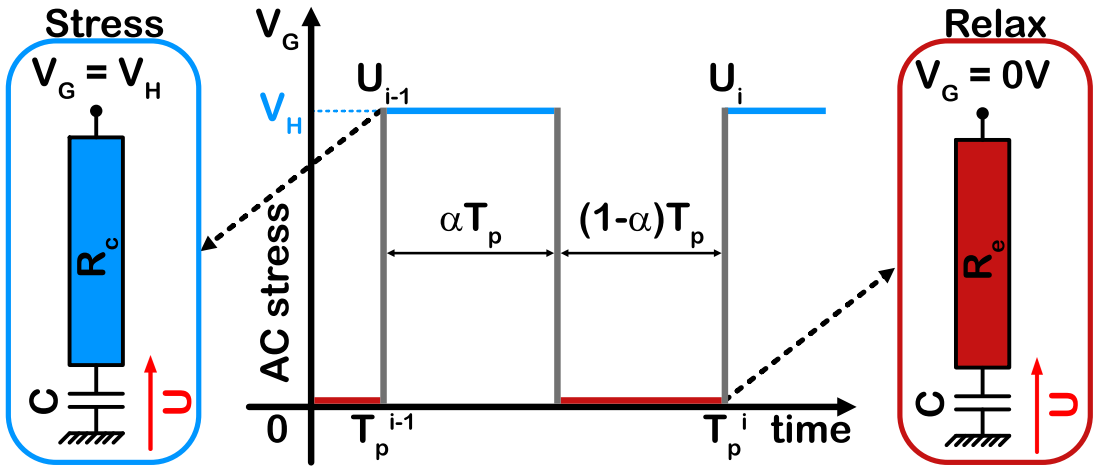

Figure 3.8. Equivalent circuits in the stress and recovery phases found during a single period T_p of AC gate voltage stress. When $V_G = V_H$, the traps are subjected to a trapping process described by the equivalent circuit on the left. However, when $V_G = 0$ V the traps are subjected to a detrapping process corresponding to the equivalent circuit on the right.

circuits during the two phases of an AC stress period.

Before calculating the charge state of the traps during an AC gate stress, the formalism is defined such as,

$$\begin{cases} U_i(t), \text{The voltage across the capacitor during the current period } [T_p^{i-1}, T_p^i] \\ U_{i-1}(T_p^{i-1}) = U_{i-1}, \text{The voltage across the capacitor at the end of the period } i-1 \end{cases}$$

By using the solutions of the differential equations 3.33 and 3.35, it is possible to calculate the voltage across the capacitor U after a certain number of periods, and thus to obtain the charge state of a single trap. Considering the period i of an AC gate stress, i.e. in the interval $[T_p^{i-1}, T_p^i]$, the voltage across the capacitor $U_i(t)$ at the end of the first stress phase ($\alpha \cdot T_p$) is given by,

$$U_i(t) = (U_{i-1} - V_H) \cdot \exp\left(\frac{-t}{\tau_c}\right) + V_H \tag{3.36}$$

In the same way, during the relaxation phase following the stress phase in the same period $[T_p^{i-1}, T_p^i]$,

$$U_i(t) = U_i(\alpha \cdot T_p) \cdot \exp\left(-\frac{t - \alpha \cdot T_p}{\tau_e}\right) \tag{3.37}$$

Considering that the AC stress periods finished with a relaxation phase, it is possible to determine the charge state of the trap at the end of the period. To do this, the new expression of equation 3.36 for $t = \alpha \cdot T_p$ (i.e. at the end of the half period) must be determined in a first time,

$$U_i(\alpha \cdot T_p) = (U_{i-1} - V_H) \cdot \exp\left(\frac{-\alpha \cdot T_p}{\tau_c}\right) + V_H \tag{3.38}$$

Afterwards, the new expression of equation 3.37 for $t = T_p^i$ (i.e. at the end of the period i) need to be determined,

$$U_i(T_p^i) = U_i(\alpha \cdot T_p) \cdot \exp\left(-\frac{(1-\alpha)\cdot T_p}{\tau_e}\right) \tag{3.39}$$

Injecting equation 3.38 in 3.39, the following expression is thus obtained,

$$\begin{aligned} U_i = \; & U_{i-1} \cdot \exp\left(-T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right) + \\ & V_H \cdot \exp\left(-\frac{(1-\alpha)\cdot T_p}{\tau_e}\right) \cdot \left(1 - \exp\left(-\frac{\alpha \cdot T_p}{\tau_c}\right)\right) \end{aligned} \tag{3.40}$$

Thus, we have the voltage across the capacitance U_i during the period i of AC stress as a function of the charge capacitance U_{i-1} during the previous period. Using a recurrence relation, it is possible to find the relationship between the trap charge after N stress periods, U_N, and the initial trap charge state U_0. After calculation we find:

$$\begin{aligned} U_N = \; & U_0 \cdot \exp\left(-N \cdot T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right) + \\ & V_H \cdot \exp\left(-\frac{(1-\alpha)\cdot T_p}{\tau_e}\right) \cdot \left(1 - \exp\left(-\frac{\alpha \cdot T_p}{\tau_c}\right)\right) \cdot \\ & \left[1 - \exp\left(-N \cdot T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right)\right] \cdot \left[1 - \exp\left(-T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right)\right]^{-1} \end{aligned} \tag{3.41}$$

Considering that the traps are initially in a completely empty state ($U_0 = 0$), the equation giving the trap charge over time is given below. Since the following equation is only valid for AC stresses ending with a relaxation phase, the trap charge state is noted as $U_{N,\,Low}$,

$$\begin{aligned} U_{N,\,Low} = \; & V_H \cdot \left[1 - \exp\left(-N \cdot T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right)\right] \cdot \\ & \left[\exp\left(-\frac{(1-\alpha)\cdot T_p}{\tau_e}\right) - \exp\left(-T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right)\right] \cdot \\ & \left[1 - \exp\left(-T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right)\right]^{-1} \end{aligned} \tag{3.42}$$

However, it is simple to obtain the equation of the charge trap state, $U_{N,\,High}$, in the case of an AC gate voltage stress ending with a stress phase. By injecting equation 3.38 in 3.39, and following the same mathematical path, the expression of the trap charge state, $U_{N,\,High}$, is given by the following equation.

$$\begin{aligned} U_{N,\,High} = \; & V_H \cdot \left[1 - \exp\left(-N \cdot T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right)\right] \cdot \\ & \left[1 - \exp\left(-\frac{\alpha \cdot T_p}{\tau_c}\right)\right] \cdot \left[1 - \exp\left(-T_p \cdot \left(\frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e}\right)\right)\right]^{-1} \end{aligned} \tag{3.43}$$

Formulas 3.42 and 3.43 can therefore be used to calculate the traps filling rate for any time constant couple. In our study, all the AC gate stresses performed end with a relaxation phase. Hence, equation 3.42 is used exclusively for this work. The latter (3.42) also enables to obtain the trap charge state in the case of a DC gate stress by setting α to 1. Note that α parameter

is comparable to the duty-factor annotated DF. The latter parameter is commonly expressed in percent, while α is usually expressed between 0 and 1. However, both parameters correspond to the ratio between the time where $V_G = V_H$ and the time where $V_G = 0$ V during a single AC gate voltage stress period.

3.3.3 V_{TH} drift calculation

3.3.3.1 Filling map principle

In the previous section, the possibility to calculate the normalized trap charge state U_N after a gate stress ($V_G = V_H$) has been demonstrated. The charge state (0 or 1) of each trap modeled by the RC circuits of the network (Figure 3.7-right) can be illustrated by a "Filling map". This latter is illustrated in Figure 3.9 and is composed of three dimensions. The x-axis and y-axis correspond to the capture time τ_c and the emission time τ_e, respectively. The third dimension corresponds to the filling state of each trap having the coordinates (τ_c, τ_e). The filling map of Figure 3.9 has been simulated for an AC gate stress of $t_{stress} = 10^3$ s for a frequency of 1kHz and a duty factor DF of 50%. Note that the specific form of this filling map is defined by the latter parameters and needs to be simulated for each stress/recovery pattern. Indeed, the red area corresponds to filled traps ("1") while the blue area is ascribed to empty traps ("0").

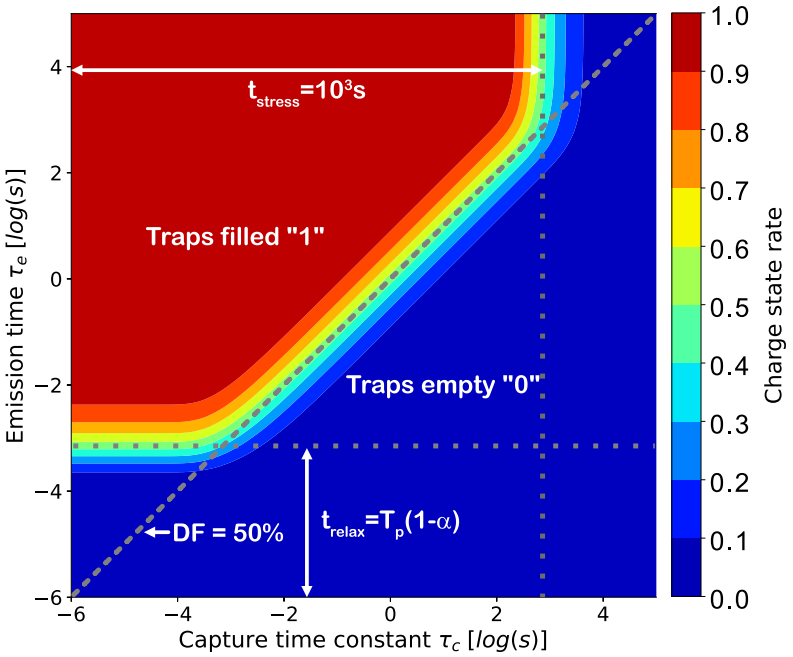

Figure 3.9. Filling map illustrating the filling state of the traps after an AC gate stress of 10^3s, at a frequency of 1kHz and a duty factor of 50%, i.e $\alpha = 0.5$.

At the beginning of a DC gate stress, all the traps are considered as empty (”0”), and hence the filling map is fully blue as shown in Figure 3.10-right. After the application of a DC stress during a fixed stress time t_{stress}, all the traps having a capture time constants τ_c below t_{stress} are subjected to be filled (”0” $\rightarrow$ ”1”), as represented in 3.10-center. Conversely, after a certain recovery time t_{relax}, all the filled traps (”1”) having a capture time constants τ_e below t_{stress} are

subjected to remain empty (”1” → ”0”), as depicted in 3.10-right.

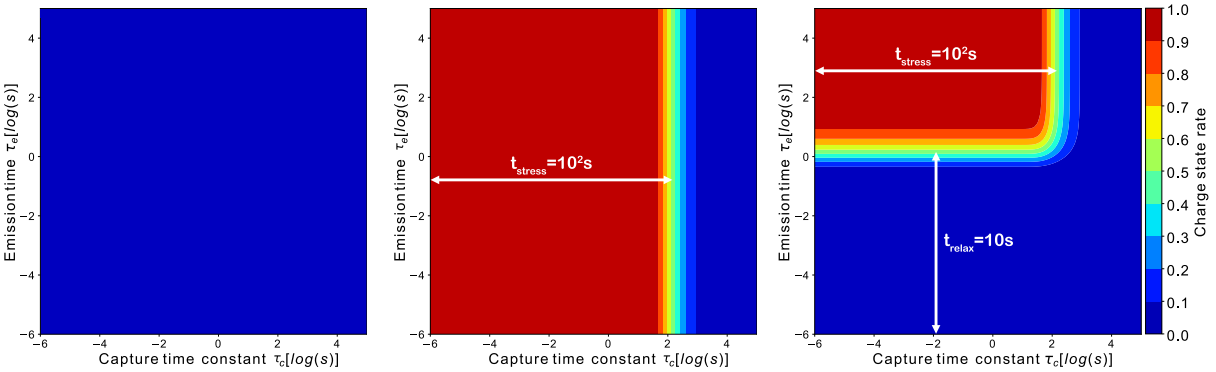

Figure 3.10. Left - Filling map without stress. **Middle -** Filling map obtained after a DC stress of 10^2s. **Right -** Filling map related to a recovery of 1s, applied just after a DC stress of 10^2s.

When an AC gate voltage stress is applied for a certain time t_{stress}, the resulting filling map is characterized by a diagonal front separating filled traps (”1”) from empty traps (”0”). The occurrence of this diagonal front is due to the fact that each AC stress period is composed of a stress and recovery phase. When the duty factor is set to 50%, this front is described by the equation $\tau_c = \tau_e$, as shown in Figure 3.11-center. If the duty factor is lower than DF = 50 %, this front shifts to the top of the filling map (3.11-left). Conversely, if the duty factor is higher than 50%, this front shifts to the bottom of the filling map (Figure 3.11-right). In both cases, the shift amplitude depends on the duty factor value. An AC gate stress can also be characterized by a relaxation of traps having a low τ_e, in the case of AC gate stress ending with a relaxation phase. This recovery is due to the relaxation phase during the last period of AC stress, corresponding to a relaxation time $t_{relax} = T_p \cdot (1 - \alpha)$.

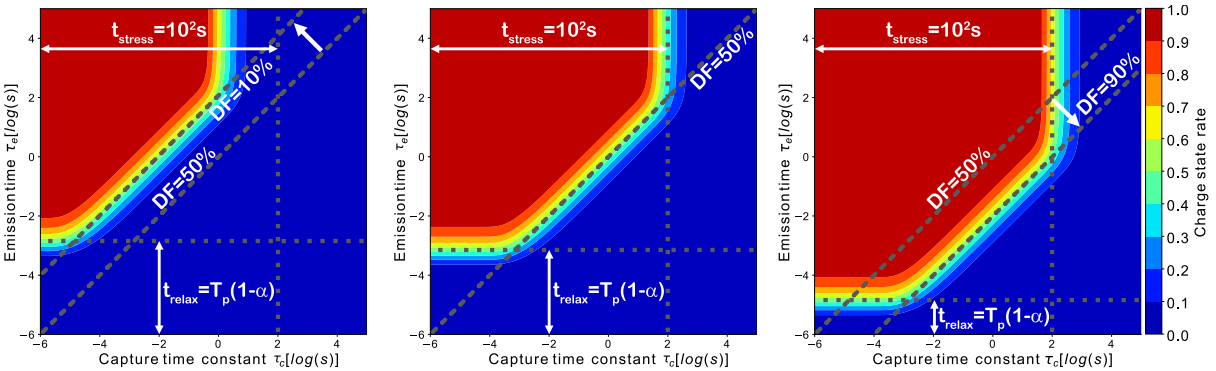

Figure 3.11. Filling maps obtained for an AC gate stress of 10^2s, at a frequency of 1kHz, and for different duty factor. **Left -** DF = 10 %. **Middle -** DF = 50 %. **Right -** DF = 90 %.

3.3.3.2 Capture Emission time map principle

At this level, the RC model developed so far enables to calculate the filling rate of the traps. However, in order to simulate the V_{TH} drift, it is necessary to define the trap density for each couple (τ_c, τ_e). It is for this precise purpose that the Capture Emission Time (CET) map is

used. The CET map is defined in 3 dimensions and has exactly the same size as the filling map. As the filling map, the x-axis and y-axis correspond to the capture time τ_c and the emission time τ_e, respectively. The third dimension corresponds to the normalized trap density $g(\tau_c, \tau_e)$. Although the filling map is obtained in a purely theoretical way (via formulas 3.42 or 3.43), the CET map is extracted via the BTI experimental measurements. Indeed, the CET map is obtained by fitting the theoretical ΔV_{TH} transients with the experimental stress and recovery BTI shifts obtained at different stress times t_{stress}. Once extracted, the CET map must be able to reproduce experimental stress and recovery BTI transients obtained via the application of an AC or DC gate stress, at a fixed $V_{GStress}$ and a fixed temperature T. Note that contrary to the filling map that must be simulated at each t_{stress} (or t_{relax}), the CET map is independent from these latter parameters as well as on the gate stress signal (AC or DC). However, a CET map is valid at one temperature T and one $V_{GStress}$.

Figure 3.12, gives an example of a CET map extracted via the application of $V_{GStress}$ of 4V at room temperature. The normalized trap density $g(\tau_c, \tau_e)$ gives an image of each trap influence on BTI shift. The higher the $g(\tau_c, \tau_e)$ of a single trap characterized by a (τ_c, τ_e) couple, the higher its influence on BTI shift. Conversely, if $g(\tau_c, \tau_e)$ related to a single specific trap is negligible, the BTI shift attributed to that trap will also be negligible even if its trap is filled. As shown in Figure 3.12 and as commonly found in literature [298], [332], [355], the trap density distribution $g(\tau_c, \tau_e)$ is usually composed of combined bivariate Gaussians. Their parameters such as their positions, their standard deviations, or their angles are adjusted until the correct normalized trap density distribution is obtained, i.e the resulting ΔV_{TH} shift reproduces the experimental BTI transients.

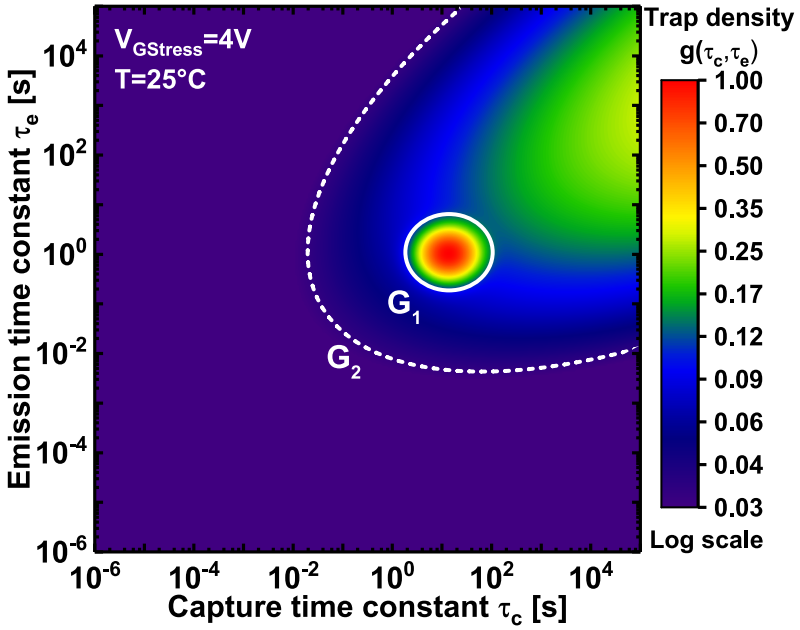

Figure 3.12. Example of a CET extracted for $V_{GStress} = 4$ V and $T = 25$ °C. The normalized trap density distribution is obtained by combining two bivariate gaussians G_1 and G_2.

3.3.3.3 V_{TH} drift determination

To summarize, when a stress signal is applied to the RC circuit network, it is possible to calculate the charge state of all the RC circuits assimilated to traps via 3.42 and 3.43. All the charge states are then reported in a filling map which is valid for a unique stress time t_{stress} (or t_{relax}), as well as a specific gate stress signal (DC or AC). On the other hand, the CET map enables to assign a normalized trap density $g(\tau_c, \tau_e)$ to each couple (τ_c, τ_e). Unlike the filling map, the CET Map is deduced from the measured BTI transients. Once determined, it is valid at a fixed temperature T and a fixed gate voltage stress $V_{GStress}$. The convolution between the filling map and the Capture Emission Time (CET) map, enable to deduce a V_{TH} shift, using the following formula.

$$\Delta V_{TH} = K \cdot \sum_{k=1}^{N} g(\tau_c^k, \tau_e^k) \cdot U^k(t) \tag{3.44}$$

Where K, is a constant specific to the technology used,
t, is the stress or recovery time,
and N is the number of traps considered in the CET map.

According to equation 3.44, a unique trap k contributes to the BTI shift at a given stress time when it is charged ($U^k = 1$), and when its trap density $g(\tau_c^k, \tau_e^k)$ is significant (> 0). If $g(\tau_c^k, \tau_e^k)$ or U^k is negligible, the trap k will not contribute to the BTI shift, even if the other parameter is high. The latter equation 3.44 is illustrated in Figure 3.13, by showing that the ΔV_{TH} is the result of a convolution between the filling map and the Capture Emission Time (CET) map. In this example, the integral of the region defined by the red continuous line in Figure 3.13-right corresponds to the resulting ΔV_{TH}. Indeed, as mentioned previously this red zone is the only one where the traps are charged ("1"), and where the trap density is significant.

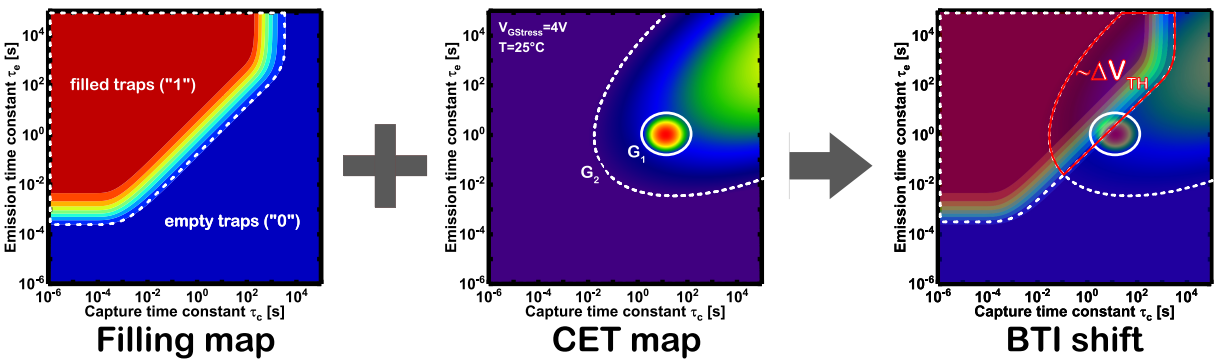

Figure 3.13. Illustration of equation 3.44, showing that the ΔV_{TH} is the result of a convolution between the filling map and the CET map. In the right figure, the zone defined by the red continuous line is the only one where the traps are charged ("1"), and where the trap density is significant. The integral of this region thus corresponds to the BTI shift value in this example.

3.3.3.4 From CET map to simulated BTI transients

3.3.3.4.1 During stress phase

Figure 3.14 illustrates how the stress BTI transients are obtained from a CET map. In this example, DC gate stresses of $V_{GStress} = 4$ V at 25°C during three different stress time ($t_{stress} = 1$ s, 10^2 s and 10^3 s) are considered. The three cases are represented by a superposition of the corresponding filling (varying with t_{stress}) with the CET map (independent from t_{stress}). In each case, a specific region (defined by the blue, green and red continuous line for $t_{stress} = 1$ s, 10^2 s and 10^3 s, respectively) is determined such as the traps are charged ("1"), and where the traps density $g(\tau_c, \tau_e)$ is significant. According to formula 3.44, the integral of these regions corresponds to the resulting ΔV_{TH}. Indeed, it can be noticed that these region surfaces increase with t_{stress}, as well as the resulting BTI shift values.

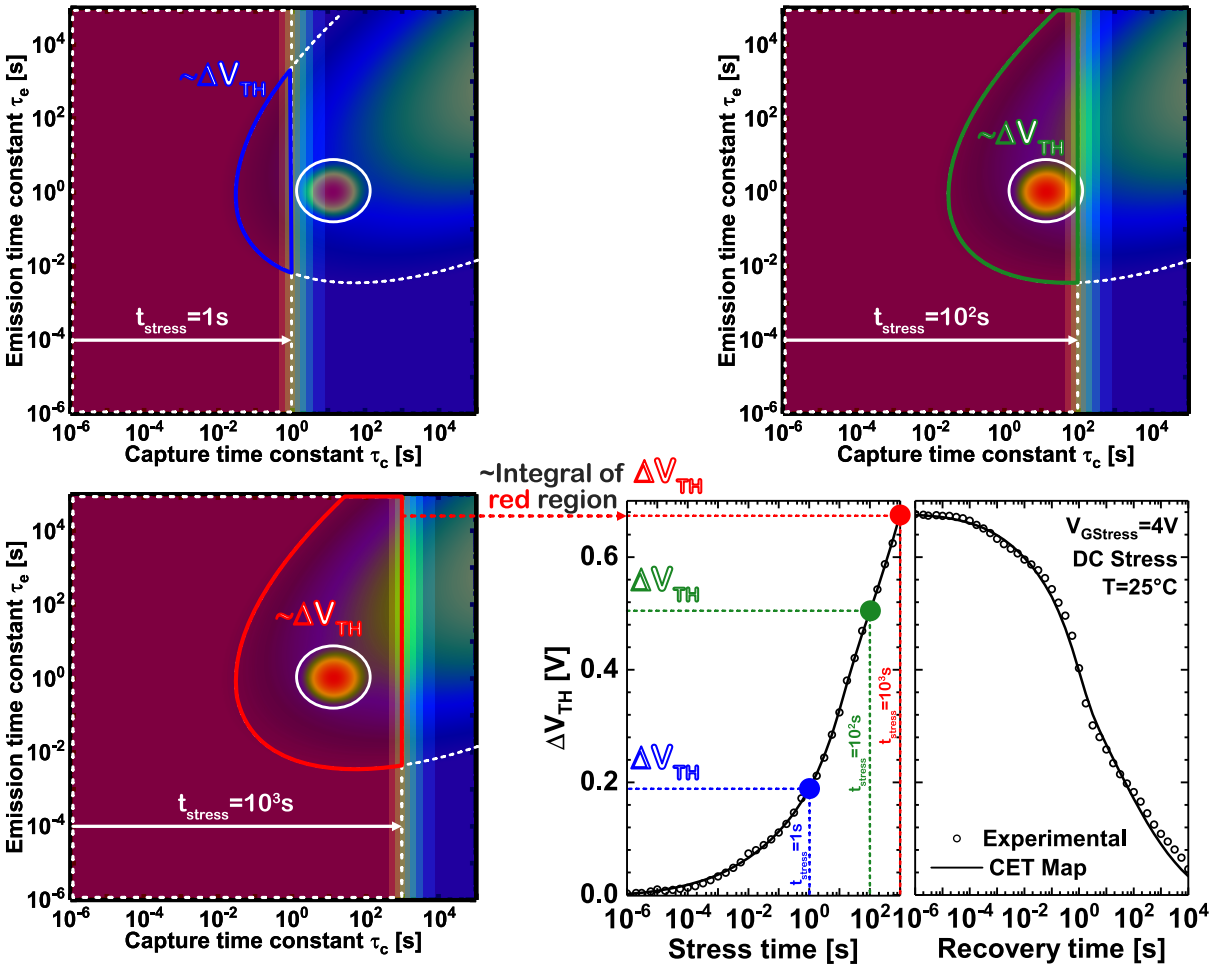

Figure 3.14. Top - Illustration of the convolution between the filling and the CET map for $t_{stress} = 1$ s (left) and 10^2 s (right). **Bottom -** Representation of the convolution between the filling and the CET map for $t_{stress} = 10^3$ s (left). Comparison between pBTI transients and ΔV_{TH} calculated from the CET map model during the stress and recovery phases at room temperature and $V_{GStress} = 4$ V (right). The resulting ΔV_{TH} obtained from the three other plots are reported. These values correspond to the integral of the regions (defined by the blue, green and red continuous line for $t_{stress} = 1$ s, 10^2 s and 10^3 s, respectively) where the traps are charged, and where the traps density is significant.

3.3.3.4.2 During recovery phase

Figure 3.15 illustrates how the recovery BTI transients are obtained from a CET map. In this example, three different recovery times (t_{relax} = 1 s, 10^2 s and 10^3 s) are considered after DC gate stresses of $V_{GStress}$ = 4 V at 25°C during 10^3s. In the same way as the stress phase, these three cases are represented by a superposition of the corresponding filling map (varying with t_{stress}) on the CET map (independent from t_{stress}). When the DC stress is applied for a duration of 10^3s, the filling map indicates that traps with a τ_c lower than 10^3s are charged in a first time. Afterwards, when a recovery is applied just after t_{stress} during a certain time t_{relax}, the initially charged traps having a τ_e less than t_{relax} become discharged. In each cases, a specific region (defined by the blue, green and red continuous line for t_{relax} = 1 s, 10^2 s and 10^3 s, respectively) is determined such as the traps are charged ("1"), and where the traps density $g(\tau_c, \tau_e)$ are significant. The integral of these regions corresponds to the ΔV_{TH} value in each case. It can be noticed that these region surfaces decrease with t_{relax}, as well as the resulting BTI shift values.

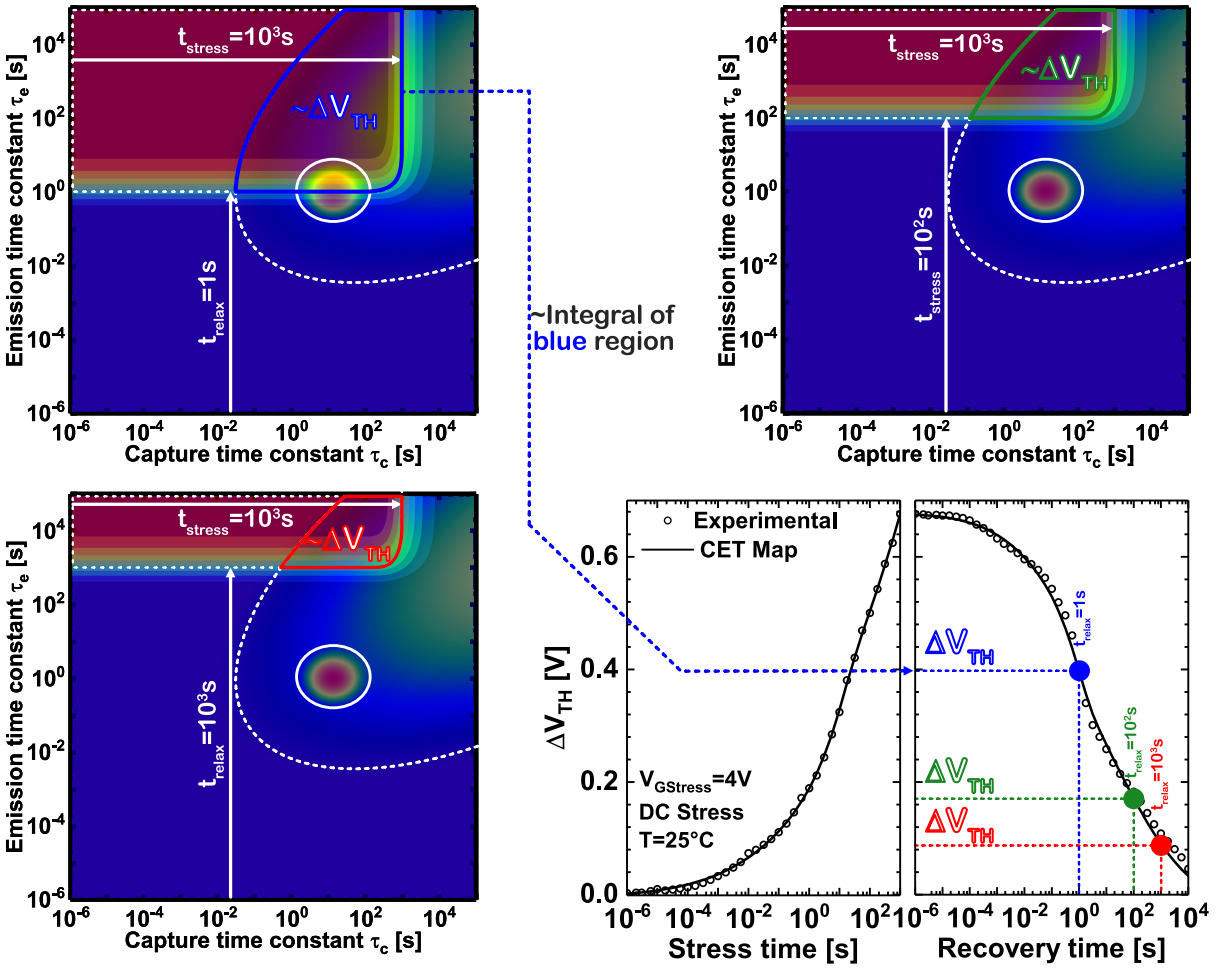

Figure 3.15. **Top -** Illustration of the convolution between the filling and the CET map for t_{relax} = 1 s and 10^2 s after a DC stress during 10^3s. **Bottom -** Same representation for t_{relax} = 10^3 s (left). Comparison between pBTI transients and ΔV_{TH} calculated from the CET map model during the stress and recovery phases (right). The resulting ΔV_{TH} obtained from the three other plots are reported on this latter plot. These values correspond to the integral of the regions where the traps are charged, and where the density of traps is significant.

3.3.4 Limitations

As we mentioned before, the CET map is valid at a fixed temperature T, and a gate stress voltage $V_{GStress}$. On the other hand, it remains unchanged with respect to the stress or recovery time. It also remains unchanged when applying a DC or AC gate stress. Indeed, the frequency f, the Duty Factor DF, and the time of application of the gate stress signal are fully taken into account by the Filling map, and therefore fully deduced mathematically (via equations 3.42 and 3.43). The interest of this CET map model is that it is possible to model and also to predict experimental BTI transients, for any type of stress signal applied at $V_{GStress}$ and fixed T.

One of the main problems of the model is the CET map extraction. Nowadays, no automatic CET map extraction method has been reported in the literature. The method initially proposed by Hans Reisinger to extract the map was based on BTI DC measurements stopped at several stress times followed by long relaxation measurements to perform a map scan [354]. This method is rarely efficient and gives rise to very poorly resolved CET maps due to a too large granularity. The CET maps proposed in the literature are all extracted by a manual retro-fit of the experimental BTI transients, i.e. a basic CET map is chosen from the BTI DC measurements and refined to describe the experimental results. Beyond the fact that it is tedious, this way of proceeding is also very time consuming. In addition, the accuracy of the CET map can also be questioned when it is extracted manually because the resulting map is judged to be acceptable in a subjective way. In the next section, an innovative method that enables to extract automatically a CET map will be proposed.

Another limitation is the uniqueness of the CET MAP. In theory, there is only one CET map able to describe experimental BTI transients in a certain validity range. However, this has never been demonstrated in the literature, i.e even if an extracted CET map describes all the experimental results, it is possible that another map will do so. Hence, it is difficult to be sure if an extracted CET map is the only one, and thus if the physical interpretation of the extracted map is valid.

Another critical point concerns the impossibility for a CET map to predict the degradation beyond its bounds. As stated before, the CET map is extracted from the experimental measurements. Therefore it is normally bounded by the time decades explored in the measurements. In our case, the CET map is bounded between $1\mu s$ which is our minimum resolution, and $10^4 s$ which is the maximum time used to determine it. Therefore, it is impossible to use our CET map to predict the BTI degradation outside its bounds.

Finally, it is also important to note that a CET map is valid at a fixed $V_{GStress}$, i.e. at a constant electric field in the gate. The problem with that point is that the V_{TH} shift inevitably induces a decrease of the overdrive voltage with the stress time, and thus an electric field decrease within the gate oxide. Therefore, the trapping probability decreases with the stress time. This trapping rate decrease can potentially be interpreted as a decrease in the trap density within the CET map (for high τ_c), which is only a decrease in the electric field in the oxide in reality.

Although the CET map model has limitations, it remains very interesting for modeling, predicting, and explaining the underlying physical mechanisms of BTI degradation. The next two sections will therefore focus on the automatic method of extracting the CET maps, as well as the associated results.

3.4 CET map extraction

In this section, a method to automatically extract a CET map using a genetic algorithm is proposed. It enables an unconstrained use of the CET map model, and thus the possibility to model, predict and study V_{TH} instabilities in a systematic way.

3.4.1 Genetic Algorithm - Notions and principle

3.4.1.1 General principle

The genetic algorithm is based on Charles Darwin's theory of evolution, and is used to solve mathematical problems without analytical solutions. It is used to find the best numerical solution of equations having a large number of unknown parameters. Figure 3.16 illustrates Darwin's theory. An initial population (monkeys here) is placed in an environment (the earth) in which it must adapt. Each individual in the population is assigned to a unique DNA molecule, with varying similarity degrees between congeners. For simplicity, we consider here that DNAs are simple chains of nucleotides (T, C, G and A). Over time, all of these DNAs will cross over each other, mutate, be evaluated by their environment, and those that adapt the best will be selected. The more this procedure is iterated, the more the population will contain DNA sequences that are adapted to the environment in which they are found [356].

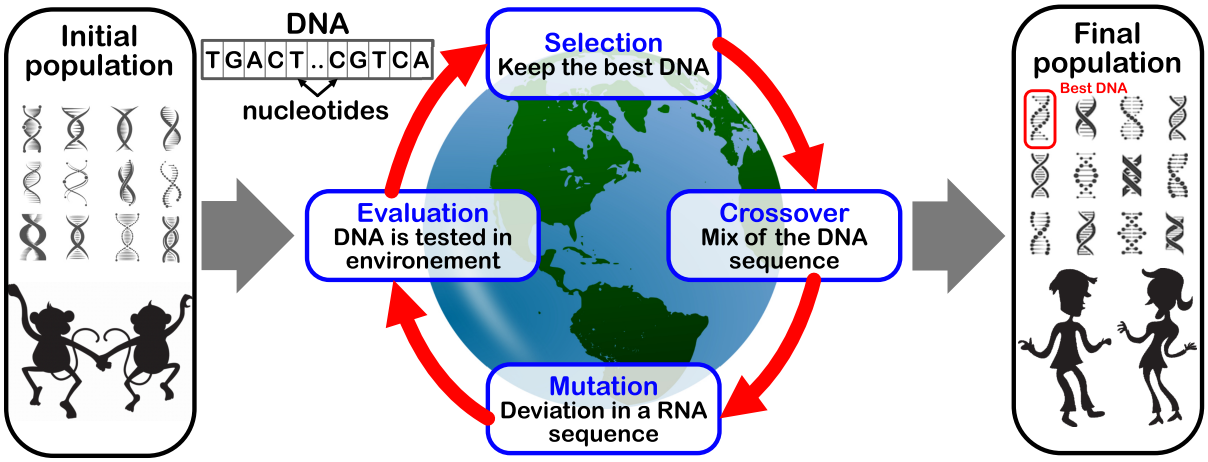

Figure 3.16. Simplified illustration of Charles Darwin's theory of evolution.

The principle of the genetic algorithm is to use the philosophy of Charles Darwin's theory. To do so, DNA made up of nucleotides, will be replaced by a vector composed of normalized fitting parameters to solve the equation, as shown in Figure 3.17.

The genetic algorithm follows exactly the procedures cited in Darwin's theory, as shown in Figure 3.18. The initial population consists of vectors containing normalized unknown parameters, randomly defined. These vectors will then be crossed between themselves via the "Crossover" function in order to give offspring vectors, which have a probability to mutate, via the "Mutation" function. The offspring vectors obtained after the application of the "Crossover" and "Mutation" functions are then evaluated. It consists in calculating the error E_{cost} between the experiment and the model through the "Evaluation" function. The offspring vectors having the

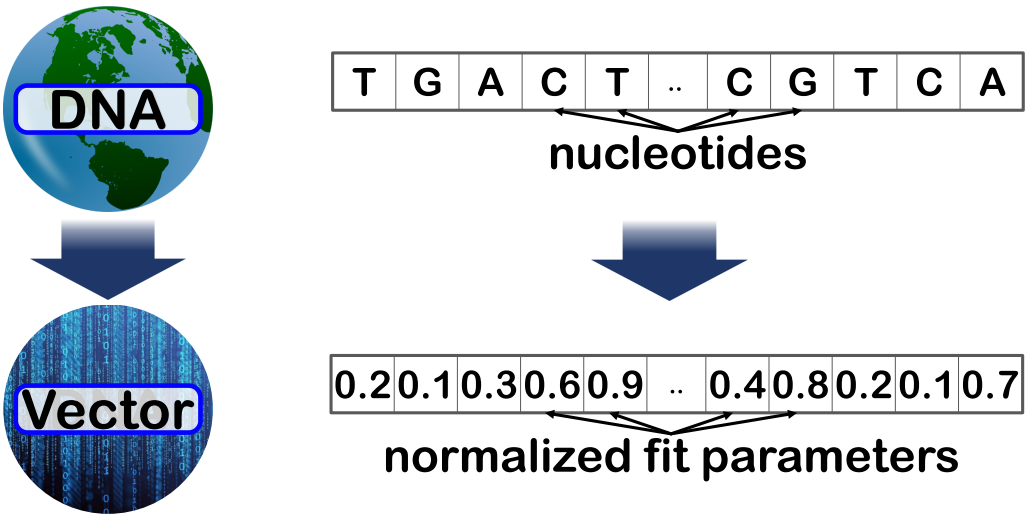

Figure 3.17. The DNA composed of nucleotides, is replaced by a vector composed of normalized fit parameters, between 0 and 1 here.

smallest error will then be selected to be subjected once again to the "Crossover", "Mutation" and "Evaluation" functions. The more the iterations, the smaller the error between the model and the experimental results [356].

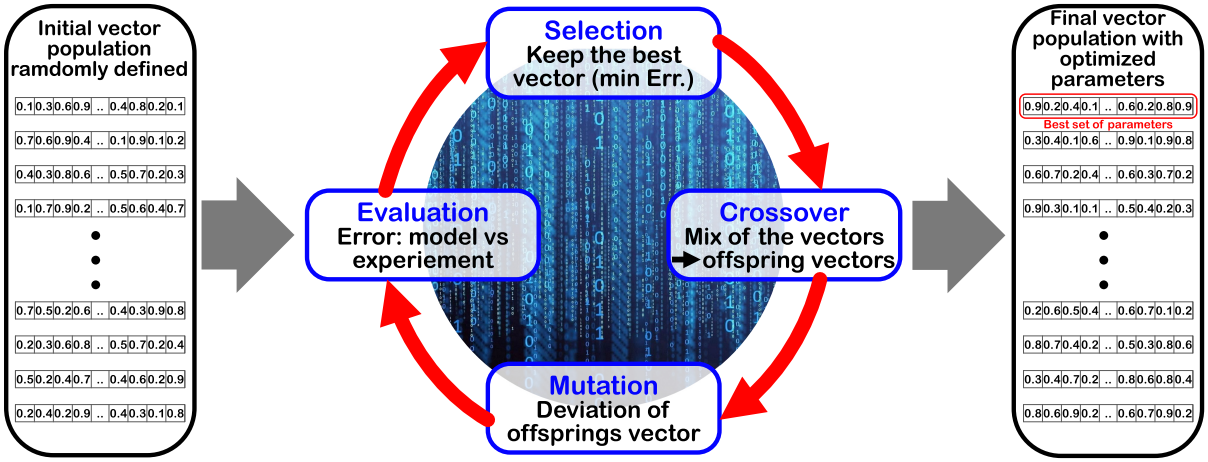

Figure 3.18. Schematic diagram of the genetic algorithm.

3.4.1.1.1 "Crossover" function

The "Crossover" function takes two parent vectors as input ($\overrightarrow{F_1}$ and $\overrightarrow{F_2}$) and returns two offspring vectors ($\overrightarrow{O_1}$ and $\overrightarrow{O_2}$) via a linear combination depending on a repartition vector α (Figure 3.19-left), such as,

$$\begin{cases} \overrightarrow{O_1} = \alpha \cdot \overrightarrow{F_1} + (1-\alpha) \cdot \overrightarrow{F_2} \\ \overrightarrow{O_2} = \alpha \cdot \overrightarrow{F_2} + (1-\alpha) \cdot \overrightarrow{F_1} \end{cases} \tag{3.45}$$

Note that α is defined randomly with elements contained between 0 and 1. Figure 3.19-right shows the associated error as a function of all the values that the fit parameters A can take. The

latter parameter is the first element of the vector in the example below. The points $F_1(A)$ and $F_2(A)$ correspond to A values belonging to the parent vectors $\overrightarrow{F_1}$ and $\overrightarrow{F_2}$, respectively. In the same way, the points $O_1(A)$ and $O_2(A)$ correspond to A values of the offspring vectors $\overrightarrow{O_1}$ and $\overrightarrow{O_2}$, respectively. As mentioned earlier, the points $O_1(A)$ and $O_2(A)$ are deduced from $F_1(A)$ and $F_2(A)$ through $\alpha(A)$, the first parameter of the vector α [356].

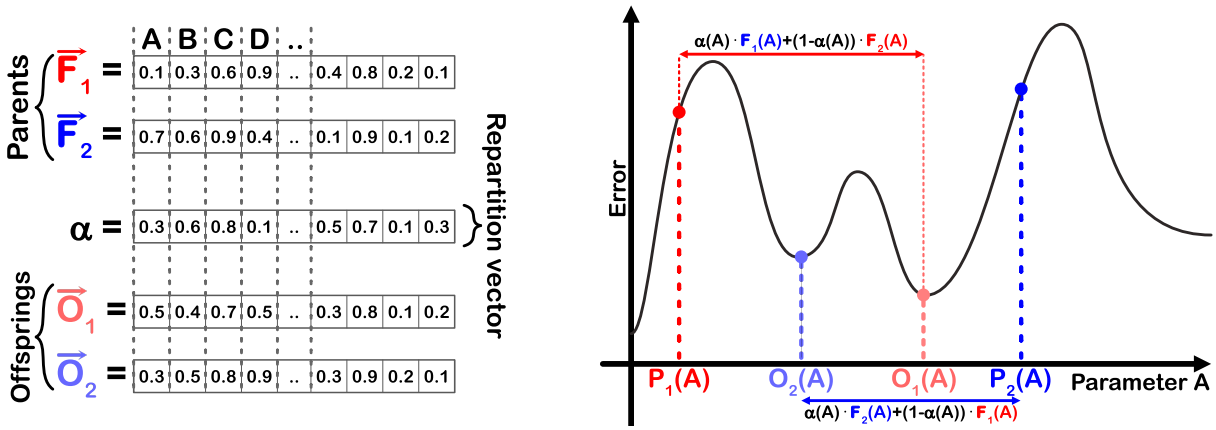

Figure 3.19. Left - Example of different vectors involved in "Crossover" function. **Right -** Plot illustration giving the associated error as a function of all the values that can take the fit parameter A, and positioning of $F_1(A)$, $F_2(A)$, $O_1(A)$ and $O_2(A)$ on this graph.

3.4.1.1.2 "Mutation" function

The "Mutation" function takes a vector as input and returns a new vector with the same dimension. It consists in modifying one or several values of the input vector. The probability that a vector element may be modified (mutated) is relatively low in general, between 1 and 15%. If an element is chosen to be mutated, the new replacement value is selected with a probability that follows a normal distribution centered on the initial value, as shown in Figure 3.20. The "Mutation" function enables to explore the solution space in order to avoid local minima [356].

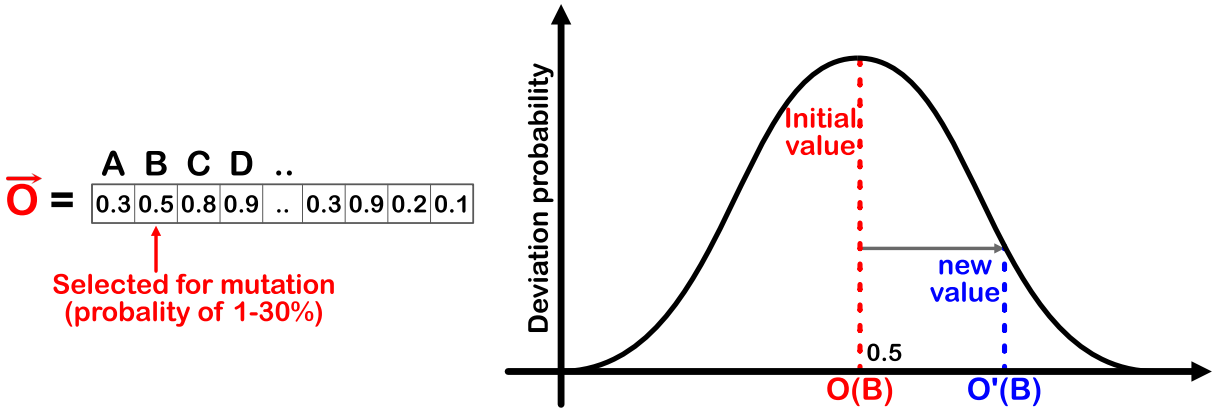

Figure 3.20. Illustration of the "Mutation" function

3.4.1.1.3 "Evaluation" function

The "Evaluation" function, also called "cost" function, takes a fit parameters vector as input and returns the associated error after comparing the model and the experiment. It first denormalizes each element of the vector before being injected into the model. Results obtained with the model are then compared to the experimental results. The method used to calculate the error E_{cost} is the least squares method, based on the following formula,

$$E_{cost} = \sum_{i=1}^{N} (Y^{i}_{exp} - Y^{i}_{model})^2 \tag{3.46}$$

Where N, is the number of points contained in the curves to be compared,
Y^{i}_{exp}, the experimental value having the index i,
Y^{i}_{model}, the calculated value with index i.

3.4.1.1.4 "Selection" function

Finally, the "selection" function takes a set of vectors composed of fit parameters, containing N_{pop} vectors. In a first time, the function ranks the input vector as a function of their associated errors E_{cost}, and afterwards selects the best N_{pop} vectors. The vectors with the best ranking are those with the lowest error in the set N_{pop}.

3.4.1.2 Global procedure of genetic algorithm

The following points describe each step of the genetic algorithm procedure illustrated in Figure 3.21 [356].

1. **Initial or parent population**
   The procedure starts with an initial population of vectors gathering all the fit parameters. It is considered that this population is composed of N_{pop} vectors randomly defined at the beginning of the procedure.

2. **Offspring population**
   The "Crossover" function (section 3.4.1.1.1) is then applied $N_{pop}/2$ times. Each time, two parent vectors ($\overrightarrow{F_1}$ and $\overrightarrow{F_2}$) are randomly picked from the initial population, resulting in two descendant vectors ($\overrightarrow{O_1}$ and $\overrightarrow{O_2}$) as illustrated in Figure 3.12. The set of offspring vectors obtained through the "Crossover" function are then subjected to the "Mutation" function (section 3.4.1.1.2). At the end of this procedure, a set of N_{pop} offspring vectors is then obtained.

3. **Evaluation**
   The initial (or parent) population and the resulting (descendant) population are then combined. A population composed of $2 \cdot N_{pop}$ vectors is then obtained. Each vector of this latter population is then evaluated using the "Evaluation" function (section 3.4.1.1.3), and an error value E_{cost} is assigned to each vector.

4. **Selection**
   As mentioned in section 3.4.1.1.4, a ranking of the set of $2 \cdot N_{pop}$ vectors is then performed, considering that the best vector is the one with the lowest error. The best N_{pop} vectors are then kept among the set of $2 \cdot N_{pop}$ vectors ranked according to their associated errors. A final population composed of N_{pop} vector is then formed.

5. **Iteration of the procedure**
   If the error associated with the best vector of the selected population is deemed acceptable, the fit parameters are considered as found and the procedure is stopped. If this error can still be reduced, the final (selected) population becomes a new parent population on which the whole previous procedure will be applied. The more this procedure is iterated, the more the error decreases, and the more accurate the fit parameters are.

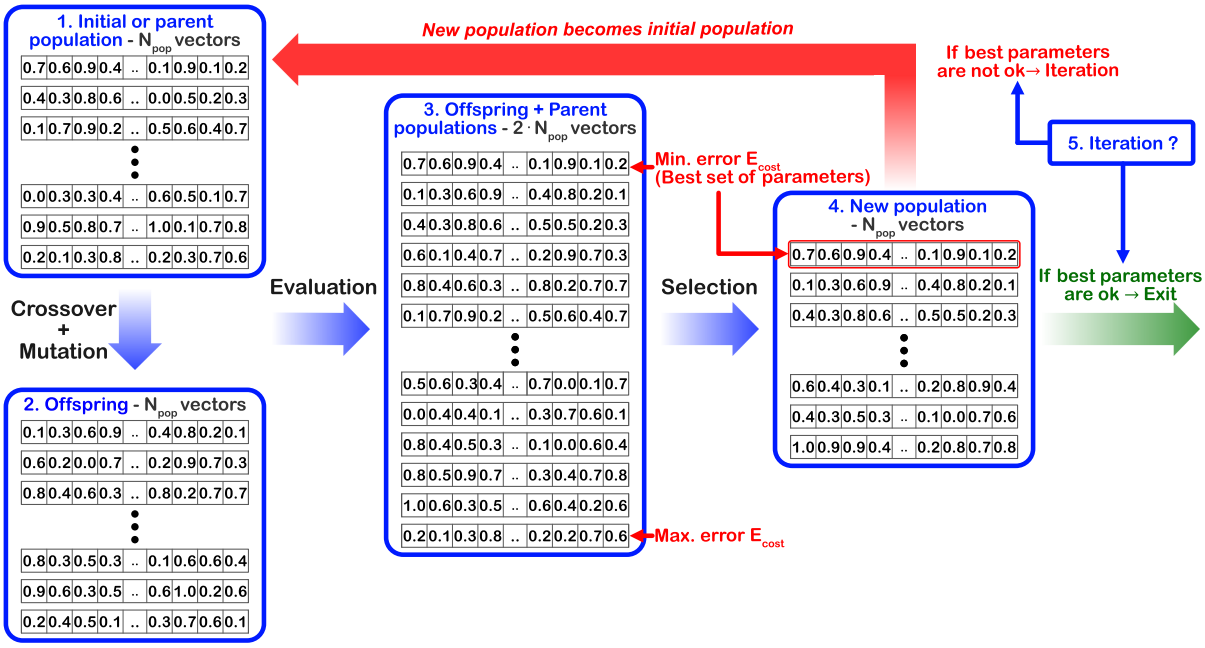

Figure 3.21. Illustration of the global procedure of the genetic algorithm.

3.4.1.3 Importance of the population size N_{pop}

In order to avoid local minima, it is necessary to explore the whole solution space. This is possible by taking a high enough vector number N_{pop} in the parent or initial population, in order to cover the whole solution space (Figure 3.22).

On the other hand, the use of a high value of N_{pop} requires to use a significant number of times the "Crossover", "Mutation", and "Evaluation" iterations (proportional to N_{pop}), which is time consuming (Table 3.1).

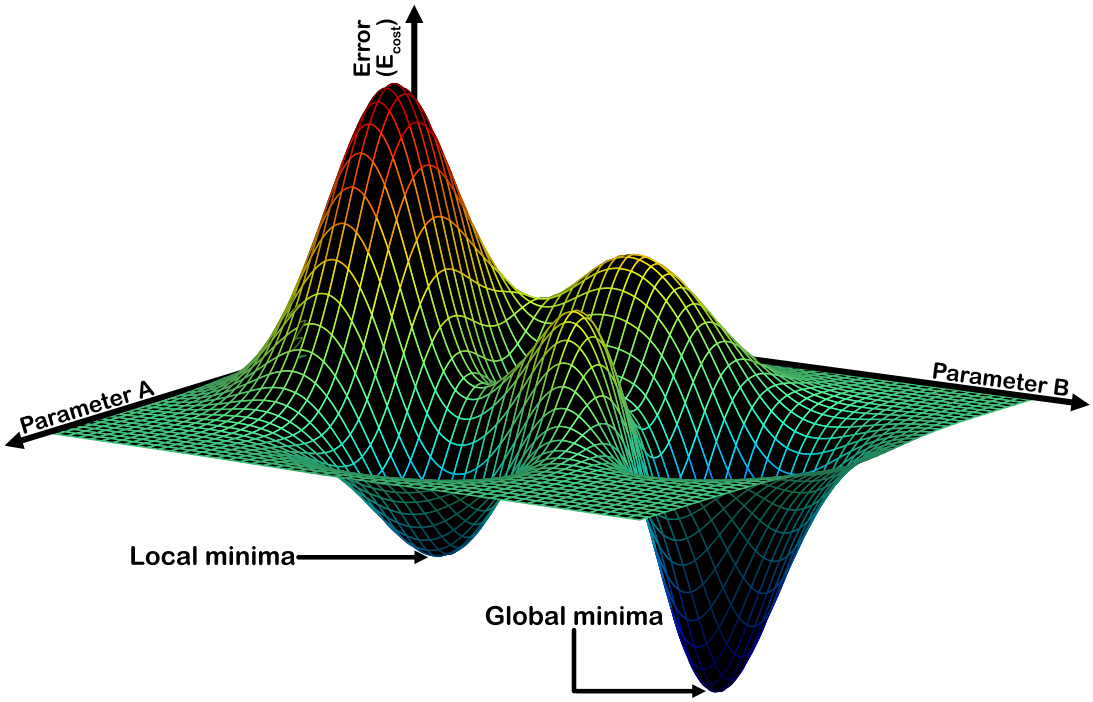

Figure 3.22. Example of a 3D solution giving the associated error E_{cost} as a function of parameter A and B. It illustrates a local minimum and the global minimum. If there are N fit parameters, the solution space will be of dimension $N+1$.

N_{pop} value	Computing time	May the solution be related to a local minimum?
Low	Low	Yes
High	High	No

Table 3.1. Influence of N_{pop} value on computing time and possible convergence to local minima.

3.4.2 Genetic Algorithm adapted to CET map extraction

3.4.2.1 CET map construction

In our approach we choose to use Gaussian distributions for CET Map extraction, as shown in Figure 3.23-left. Note that another distribution functions can be used, and does not modify the proposed method. The difficulty consists in placing the bivariate Gaussians on the map, i.e. determining the value of the 6 different parameters defining each of them. Among these parameters, there are the Gaussian center coordinates which are defined by μ_x and μ_y as well as the standard deviations defined by σ_x, and σ_y. There are also the amplitude and lateral orientation of the Gaussian defined by A and Θ respectively as illustrated in Figure 3.23-right. The bivariate gaussian equation $G(x,y)$ is given below,

$$G(x,y) = A \cdot \exp(C_x + C_y) \tag{3.47}$$

Where,

$$C_x = -\frac{1}{2} \cdot \left(\frac{(x-\mu_x)\cdot\cos(\theta) - (y-\mu_y)\cdot\sin(\theta)}{\sigma_x} \right)^2$$
$$C_y = -\frac{1}{2} \cdot \left(\frac{(x-\mu_x)\cdot\sin(\theta) + (y-\mu_y)\cdot\cos(\theta)}{\sigma_y} \right)^2$$

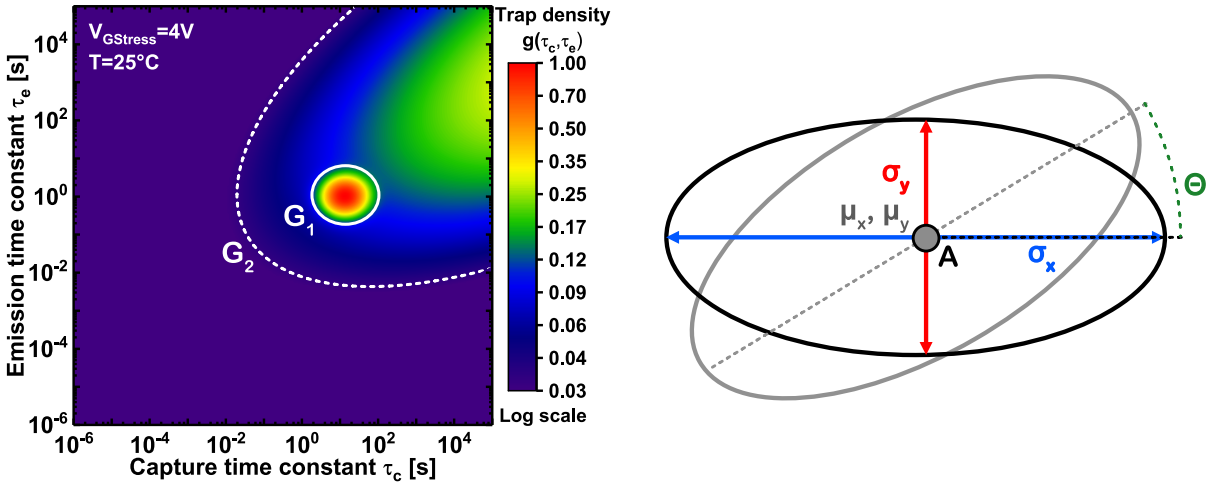

Figure 3.23. Left - Example of CET map, built from two gaussians G_1 and G_2. **Right -** Schematic showing the 6 parameters on which a bivariate gaussian depends.

Therefore, the number of parameters defining N_{param} is proportional to a factor 6 and depends on the number of Gaussians $N_{Gaussian}$, which need to be integrated in the CET map.

$$N_{param} = 6 \cdot N_{Gaussian} \tag{3.48}$$

N_{param} defines the dimension of the vectors that will be used in the genetic algorithm. The role of this latter is then to place a certain number of Gaussians $N_{Gaussian}$ previously defined on the CET map.

3.4.2.2 CET map discretization

Once the Gaussians are placed on the CET map, the associated ΔV_{TH} instabilities must be calculated from it. The CET map is then discretized as shown in Figure 3.24, where each discrete point is associated with a single trap ascribed to a couple (τ_c, τ_e), and corresponding to one of the sub-circuits of the RC network in Figure 3.7. The discretization is performed using a resolution R_p defined in point number per time decade. The finer the resolution, the higher the accuracy of the CET map. Although it depends on the studied devices, a CET map is considered significant when the resolution is sufficiently high, i.e. around 10 points per time decade approximately. On the other hand, such a high resolution requires a relatively high computational time to deduce the associated ΔV_{TH} transients.

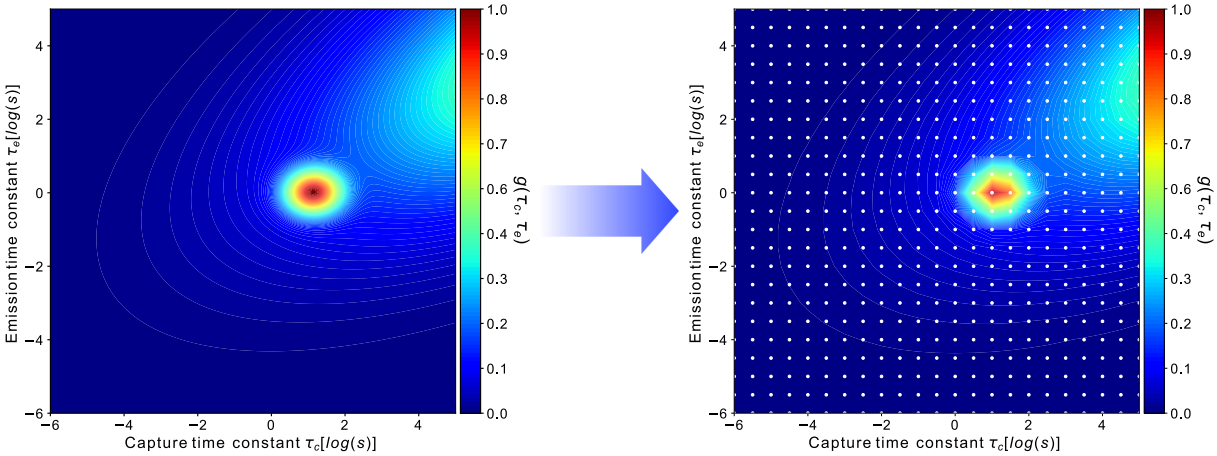

Figure 3.24. Illustration of the discretization of the left CET map. The discretized CET map (right) has a resolution of 3 points per decades, in this example.

3.4.2.3 Genetic Algorithm limitations when it is applied to CET map extraction

There are three main constraints that limit the application of the genetic algorithm to the automatic extraction of CET maps. The first one is to avoid local minimum, and thus to choose a high enough value of N_{pop} to explore the whole solution space, which implies a significant computation time (Table 3.2).

N_{pop} value	Computing time	May the solution be related to a local minimum?
Low (<100)	Low	Yes
High ($\sim$ 500-1500)	High	No

Table 3.2. Influence of N_{pop} value on computing time and the possible convergence to a local minima.

The second constraint consists in obtaining a significant CET map, i.e. a high resolution in the order of 10 points per time decade, which also implies computation time (Table 3.3).

Mesh resolution R_p	Computing time	Is the CET map significant?
Low ($\sim$ 2 points per decades)	Low	No
High ($\sim$ 10 points per decades)	High	Yes

Table 3.3. Influence of mesh resolution R_p on computing time and on the relevance of the resulting CET map.

Finally, the third constraint is intrinsic to the genetic algorithm itself, meaning that the more iterations there will be ("Crossover", "Mutation", "Evaluation", "Selection"...), the more the algorithm will converge towards precise fit parameters, which will also imply an increase in computation time (Table 3.4).

Iterations	Computing time	Error E_{cost} value
Low (10)	Low	high
High (10^5)	High	Low

Table 3.4. Influence of iteration number on computing time and the resulting error between the model and the experiment.

As it is necessary to find the global minimum of the solution space, to obtain an accurate and significant CET map, it is therefore necessary to find a solution to reduce the computation time while respecting the latter conditions (corresponding to green cells in Table 3.2, 3.3 and 3.4).

3.4.2.4 Procedure to overcome extraction limitations

This section consists in a presentation of the procedure enabling to get a reasonable computation time, while extracting an accurate and significant CET map which is the image of the global minimum of the solution space. This procedure consists in running the genetic algorithm several times, by progressively increasing the resolution and lowering N_{pop} between each run. The following points describe each step of the procedure as shown in Figure 3.25.

1. **Initialization**
   Before launching the procedure, an initialization of N_{pop}, the resolution R_p and the maximum number of iterations is necessary. The latter parameter defines a maximum number of iterations that needs to be reached to get an acceptable E_{cost} error. At the beginning of the procedure, we try to find the global minimum in a rather coarse way. To do so, a relatively high N_{pop} is defined to explore the whole solution space quite finely. N_{pop} value depends on parameter number and therefore Gaussian number, $N_{Gaussian}$, as well as the size of the solution space. A rather high value of maximum iterations is also defined at initialization, in order to be sure to converge toward the global minimum solution. In order to have a reasonable computation time, the high N_{pop} value and the high number of iterations are compensated by a low resolution with $R_p = 1-4$ points per time decade. Note that the resolution is the parameter that has the most influence on the computation

time. The number of Gaussian distributions chosen, and thus the fit parameter number N_{param} is defined by the user. N_{param} remains fixed throughout the whole procedure. As a reminder, N_{param} defines the number of fit parameters, and thus the dimension of the vectors that will be processed in the genetic algorithm.

2. **Genetic algorithm**
   The genetic algorithm described in section 3.4.1.2 takes the different parameters defined in the initialization as input value. It will therefore start by creating an initial population of vectors each containing N_{param} fit parameters which are normalized and randomly generated. The initial population contain N_{pop} vectors. Finally, the algorithm will iterate the "Crossover", "Mutation", "Evaluation" and "Selection" procedures, until it reaches the maximum value of iterations. Once this latter value is reached, the error is considered as the best one and cannot decrease significantly.

3. **Resulting optimized fit parameters**
   Once the genetic algorithm has reached the maximum number of iterations, it returns the vector containing the best fit parameters for the defined resolution R_p. Since the resolution is relatively low, the resulting vector parameters do not fully reflect the global minimum of the solution space, but they can be considered as very close to the global minimum.

4. **Construction of a new parent population**
   Now that the position of the global minimum is coarsely found, the goal is to refine this position, at higher resolutions. A new parent population will then be built around the vector previously returned by the genetic algorithm and containing the best fit parameters (reference vector). The vectors are defined randomly with a probability that follows a normal distribution centered on the reference vector.

5. **Resolution increase**
   As a reminder the goal of the procedure is to obtain a CET map with a high resolution. Once the global minimum has been coarsely found, the resolution R_p can be increased from $+1$ to $+6$ points per time decade.

6. **Decrease of the maximum iterations number**
   In order to reduce the computation time which has necessarily increased with the increase of $_p$, it is possible to reduce the maximum number of iterations. Indeed, since the vectors constituting the new parent population are already close to the global minimum, the algorithm will converge to the global solution with fewer iterations than at the beginning of the procedure.

7. **N_{pop} decrease**
   Since the use of a high N_{pop} enables to explore the whole solution space in order to find the global minimum in a coarse way, it is no longer necessary to explore the whole solution space in a fine way. Indeed, it is enough to explore only the area associated with the global minimum, i.e. the area defined by the reference vector. Thus, it is also possible

to reduce N_{pop} in order to save computation time. To do so, N_{pop} is divided by a factor ranging from 2 to 10. This has the effect to compensate the increase of calculation time induced by the resolution increase.

8. Iteration

The rest of the procedure consists in injecting the new parent population as an input of the genetic algorithm, which will once again return fit parameters at a higher resolution. A new parent population will then be constructed based on the new reference vector. The latter will be injected once again in the genetic algorithm, with an increase in resolution and a decrease in the maximum number of iterations as well as N_{pop}. Once the resolution is significant, and the associated error is acceptable, it is possible to exit the loop including the last 6 procedure steps.

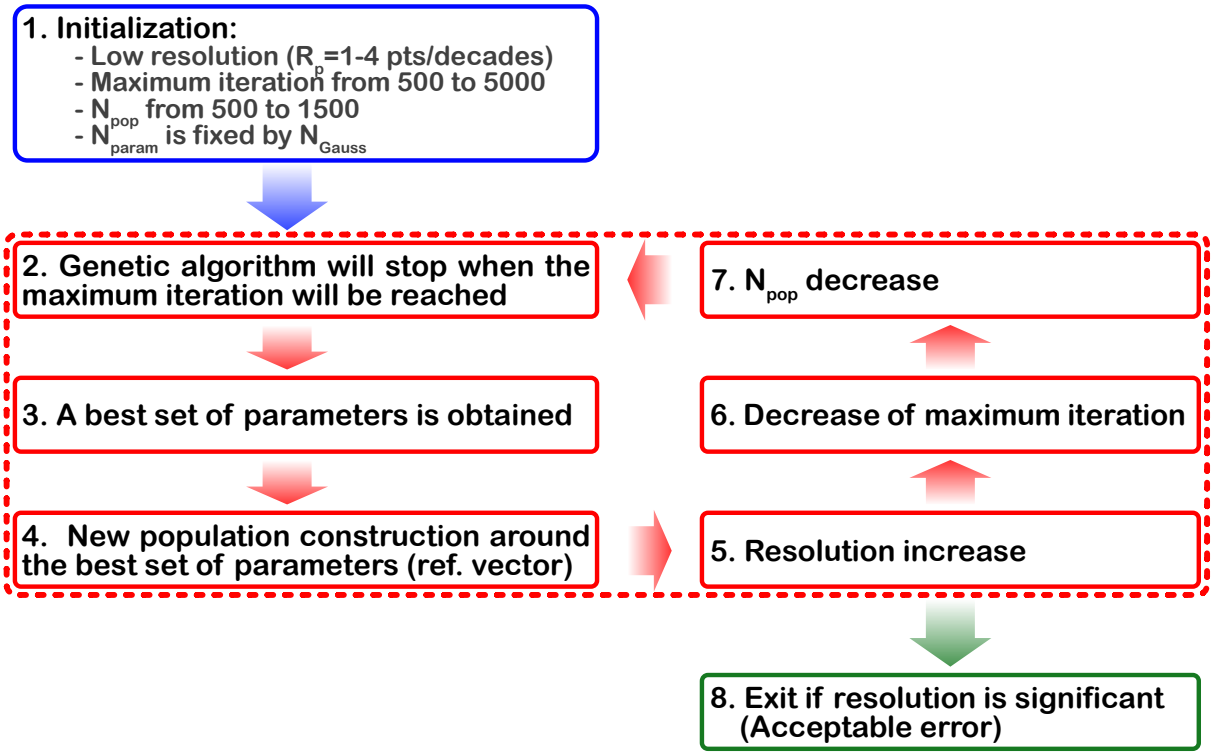

Figure 3.25. Illustration of the procedure enabling to get a reasonable computation time, while extracting an accurate and significant CET map which is the image of the global minimum of the solution space. The diagram shows how the 8 steps previously described are structured.

3.5 PBTI modeling using CET map model

In this section, Capture Emission Time (CET) map approach is applied to go further in the understanding of the pBTI degradation kinetics obtained in our gate stack. As previously mentioned, this model enables the modeling as well as the prediction of BTI transients obtained under a wide range of AC and DC gate stress conditions. All the experimental results presented in this section concern the pBTI degradation on transistors presented in section 2.3. The whole CET map presented in this section has been extracted using the method illustrated in Figure 3.25. As described in chapter 2, ΔV_{TH} is monitored through ultra-fast V_G ramp ($<$ 10 µs) during stress and recovery phases in order to minimize the unwanted recovery during the $I_D(V_G)$ measurements. Note that V_{DS} is fixed at 100mV during fast $I_D(V_G)$ measurements, while it is set to 0V during stress phase. Finally, the tested transistors are 8mm wide with a gate length (L_G) of 1µm, while L_{GD} and L_{GS} are constant. The V_{TH} is extracted at fixed drain current level such as $I_D = I_0 \cdot W_G/L_G$, where $I_0 = 20 \cdot 10^{-9}$ A.

3.5.1 DC PBTI modeling at room temperature

In the previous chapter, we demonstrate that pBTI degradation is influenced by a C_N deep acceptor and Al_2O_3 (oxide) trap populations. The latter is located at the gate oxide interface while the C_N trap population is ascribed to the burried GaN:C layer. Both of these trap influence pBTI degradation via different underlying mechanisms. Indeed, a low gate voltage stress ($V_{GStress} < 1.5$ V) is sufficient to activate the neutral C_N trap ionization ($0 \rightarrow -$) leading to the increase of the conduction band energy at the Al_2O_3 gate oxide interface, and then a V_{TH} increase. As a reminder, C_N trap ionization is related to strong ΔV_{TH} variations occurring during stress and recovery phases respectively at the time constants τ_s and τ_r, respectively. On the other hand, an electron injection in Al_2O_3 traps is activated at high gate voltage stress $V_{GStress} > 1.5$ V. This underlying mechanism is ascribed to a continuous V_{TH} shift.

Figure 3.26-left shows the CET map extracted for a $V_{GStress} = 4$ V at 25°C giving the C_N and Al_2O_3 trap population densities via two bivariate Gaussians. This CET map is composed of a peaked Gaussian G_1 and a broad Gaussian G_2, where the former trap density distribution (G_1) is centered around a capture τ_c and emission τ_e time constants of 2 and 10s, respectively, and with an important trap density $g(\tau_c, \tau_e)$. Characteristic parameters of both G_1 and G_2 Gaussians have been determined by fitting the ΔV_{TH} pBTI degradation. The latter shows the pBTI stress and recovery transients obtained under a DC gate voltage stress of 4V at room temperature, for different maximum stress times $t_{s,max}$ from 10^{-5}s to 10^{3}s. These pBTI transients allow to get the behavior of a wide range of emission time constants, which is necessary for CET map extraction. It can be noticed on the same figure, that the experimental DC pBTI degradations are accurately reproduced by the V_{TH} transients calculated from the CET map for a wide range of maximum stress times $t_{s,max}$. The strong V_{TH} variations occurring at τ_s and τ_r, and which has been ascribed to C_N traps in chapter 2, are also accurately modeled.

3.5.2 AC PBTI modeling at room temperature

As mentioned previously, the CET map model also predicts the BTI experimental results obtained at a fixed gate voltage stress as well as a fixed temperature. Once the CET map is

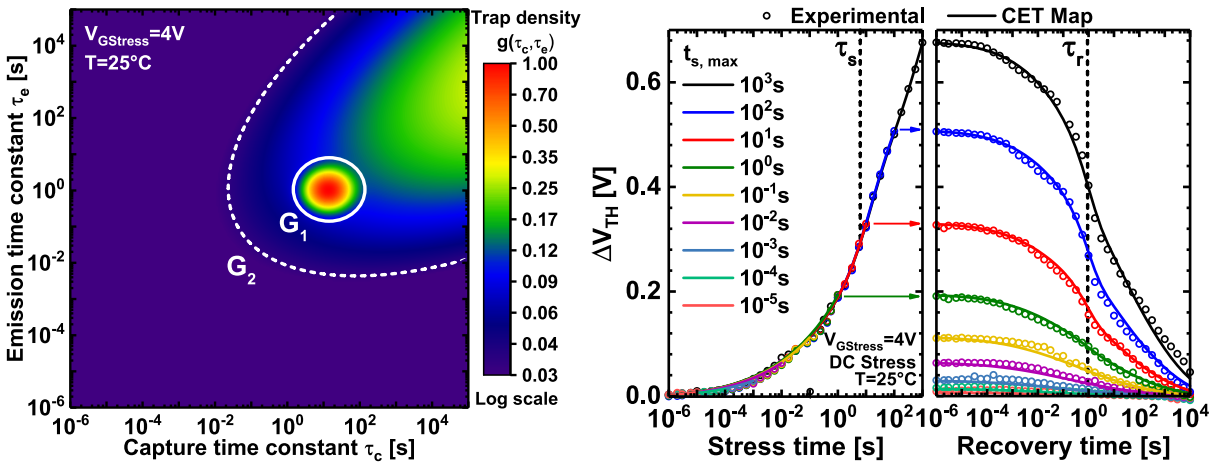

Figure 3.26. Left - CET Map giving the trap density $g(\tau_c, \tau_e)$ obtained at $V_{GStress} = 4$ V and at room temperature. It depicts two trap populations, described by a peaked Gaussian G_1 centered at $\tau_c = 10$ s and $\tau_e = 2$ s, and a broad bivariate Gaussian distribution G_2. **Right -** Comparison between pBTI transients and ΔV_{TH} calculated from CET map, during the stress and recovery phases, and for different maximum stress times $t_{s,max}$. PBTI transients have been performed at room temperature and applying a DC stress of $V_{GStress} = 4$ V.

extracted by fitting the calculated ΔV_{TH} shifts with the DC pBTI stress and recovery transients obtained at different $t_{s,max}$ (Figure 3.26-right), it can be used to predict the pBTI degradation obtained under an AC or a random gate voltage stress pattern [298], [334], [353]. Figure 3.27-right depicts a comparison between ΔV_{TH} shift transients calculated from CET map of Figure 3.26-left, and experimental AC pBTI stress and recovery transients obtained under various duty factors (DF) at a frequency f of 1kHz and a $V_{GStress}$ of 4V. As already mentioned in section 3.3.2, the duty factor is the ratio between the time where $V_{GStress} > 0$ V (On-state) and the time where $V_{GStress} = 0$ V (Off-state), during a single AC gate voltage stress period. The calculated ΔV_{TH} transients accurately predict the experimental pBTI transients, thus confirming the consistency of the CET map, and therefore the characteristics of G_1 and G_2 trap density distributions. The results presented in Figure 3.27-right are obtained from the data shown in Figure 3.27-left. It exhibits the ΔV_{TH} shifts after three AC maximum stress times $t_{s,max} = 1$, 10 and 100 s as a function of the duty factor DF from 0.1 to 99.9%. Note that these three S-curves are normalized by the pBTI degradation obtained after 100s of DC stress at $V_{GStress}$ of 4V at room temperature. It can be noticed that the CET map model also reproduces the experimental S-curves quite accurately, in particular at low DF thus confirming the consistency of the lower part of the CET map, i.e at capture time constant τ_c below 100µs.

3.5.3 PBTI modeling as a function of temperature

3.5.3.1 PBTI modeling at high temperature

In the same way as CET map in Figure 3.26-left dedicated to model BTI shift at room temperature, a CET map at high temperature has also been extracted. Figure 3.28-left exhibits the trap density $g(\tau_c, \tau_e)$ via trap populations G_1 and G_2, for a gate voltage stress of 4V at 150°C. A shift of G_1 distribution towards very short time constants, compared to the CET map extracted at 25°C (Figure 3.26-left), can be noticed. Moreover, an extension of G_2 distribution towards

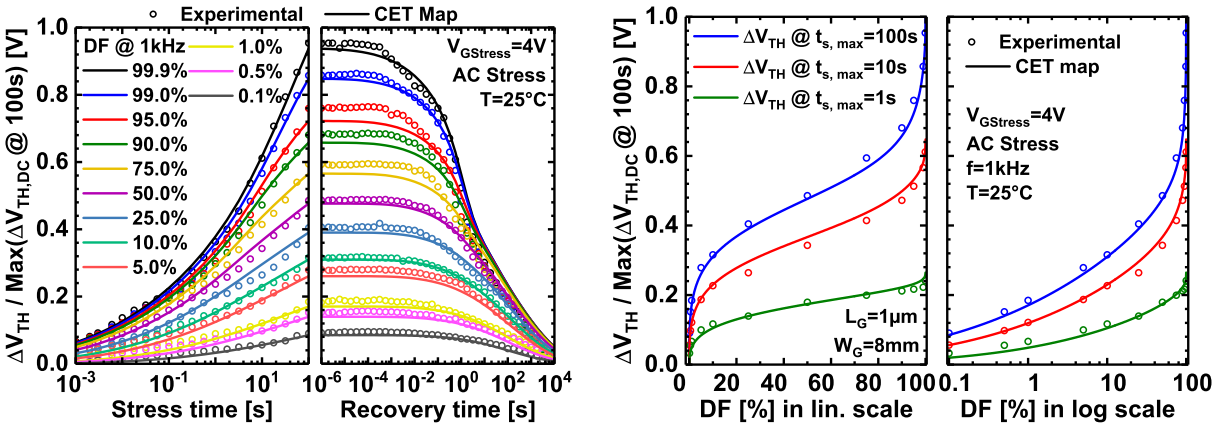

Figure 3.27. Left - Comparison between normalized experimental pBTI and modeled transients from CET map of 3.26-Right. Stress and recovery experimental pBTI transient are obtained via the application of an AC gate voltage stress of 4V at room temperature, and for various duty factors DF. The AC stress frequency f is set to 1kHz. **Right -** Comparison between normalized experimental pBTI and modeled ΔV_{TH} variation as a function of the duty factor, obtained under $V_{GStress} = 4$ V at 25°C for 3 different maximum stress times $t_{s,max} = 1$, 10 and 100 s.

short time constants can be also observed, revealing a wider spectrum of trap state continuity at high temperature. Figure 3.28-right shows that experimental pBTI transients are fitted with accuracy, during the stress and recovery phases, thus providing a validation of the CET map. These latter transients have been obtained via the application of a DC gate voltage stress of 4V and at 150°C for different $t_{s,max}$.

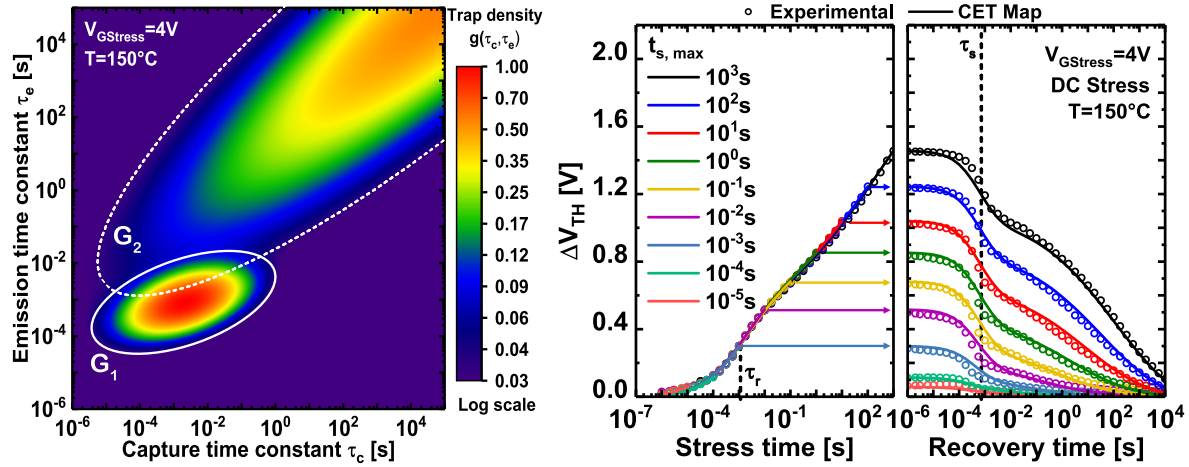

Figure 3.28. Left - Traps density distribution $g(\tau_c, \tau_e)$ for $V_{GStress} = 4$ V at 150°C showing the broad trap distribution G_2 and the peaked distribution G_1 centered around $\tau_c \approx 1$ ms and $\tau_e \approx 2$ ms. **Right -** Comparison between pBTI transients and ΔV_{TH} calculated from CET map presented in left graph, during the stress and recovery phases, for different maximum stress times, $t_{s,max}$. PBTI transients have been performed by applying a DC stress of $V_{GStress} = 4$ V at 150°C.

3.5.3.2 PBTI modeling at different temperatures

CET maps have been extracted at various temperature T from 25 to 150°C at $V_{GStress} = 4$ V, using the method proposed in Figure 3.25. All these CET maps are illustrated in Figure 3.29-left. It gives the positions of G_1 and G_2 trap density distributions at each temperature, via ellipses corresponding to the Gaussian contours at $2 \cdot \sigma$. Each CET map presented was extracted by fitting the DC pBTI stress and recovery transients obtained after different maximum stress times $t_{s,max}$. It is observed that both G_1 and G_2 trap distributions have different kinetics with temperature. Indeed, G_1 peaked trap density distribution has an exponential dependency on temperature, and moves towards very short capture and emission time constants as the temperature rises.

Although all $2 \cdot \sigma$ ellipses related to G_2 are approximately located at the same position in Figure 3.29-left, it does not mean that G_2 is not temperature dependent. Indeed, the $2 \cdot \sigma$ ellipses are also defined by the Gaussian amplitude A, which increases with temperature in our case. An amplitude augmentation combined with an extension towards short time constants of G_2 distribution can be observed on the CET map extracted from pBTI transients obtained at 150°C in Figure 3.28-left. The latter CET map reveals a wider spectrum of trap state continuum related to G_2 compared to the CET map of Figure 3.26-left.

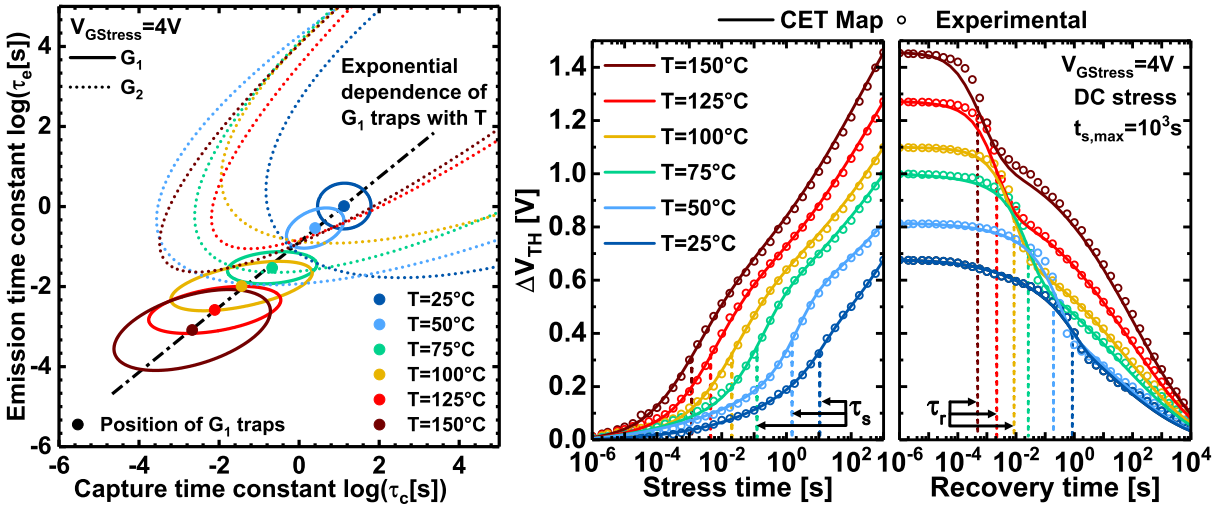

Figure 3.29. Left - CET maps giving the positions of both trap density distributions G_1 and G_2 at various temperatures, through ellipses corresponding to the Gaussians contours at $2 \cdot \sigma$. **Right -** Comparison between experimental pBTI transients and ΔV_{TH} calculated from CET maps of left graph, during the stress and recovery phases, and at different temperatures from 25 to 150°C. These transients have been obtained applying a DC gate voltage stress of 4V during 10^3s.

The different CET maps presented in Figure 3.29-left enable the modeling of the experimental DC pBTI stress and recovery transients at different temperatures from 25 to 150°C, as exhibited in Figure 3.29-right. The strong ΔV_{TH} variations at τ_s and τ_r associated to the presence of C_N traps in GaN:C layer can be clearly observed at a $V_{GStress}$ of 4V. Moreover, the second trapping regime related to charge injection in Al_2O_3 defects and which have a lower temperature dependence can be also observed in the same figure.

Even though only the pBTI transients performed for maximum stress times of 10^3s are de-

picted in Figure 3.29-right, each CET map shown in Figure 3.29-left is able to accurately model the experimental pBTI transients obtained for all the maximum stress times, $t_{s,max}$, presented in Figure 3.26-right and 3.28-right. A Comparison between stress and recovery experimental pBTI transients and ΔV_{TH} deduced from CET maps of Figure 3.29-left are presented in Figure 3.30 for $t_{s,max} = 10$ s and 100 s. As depicted in Figure 3.29-right, the latter transients have been obtained by applying a DC gate voltage stress of 4V during 10^3s. It can be noticed that the contribution of strong ΔV_{TH} variation at τ_s and τ_r in stress and recovery transient decrease as $t_{s,max}$ decrease. This can be explained by a charge state saturation of the C_N trap population over stress time, resulting in a ΔV_{TH} plateau if $V_{GStress} < 1.5$ V. The continuous pBTI increase with stress time in Figure 3.29-right is explained by electron trapping in alumina gate oxide occurring at high gate voltage stress (> 1.5 V).

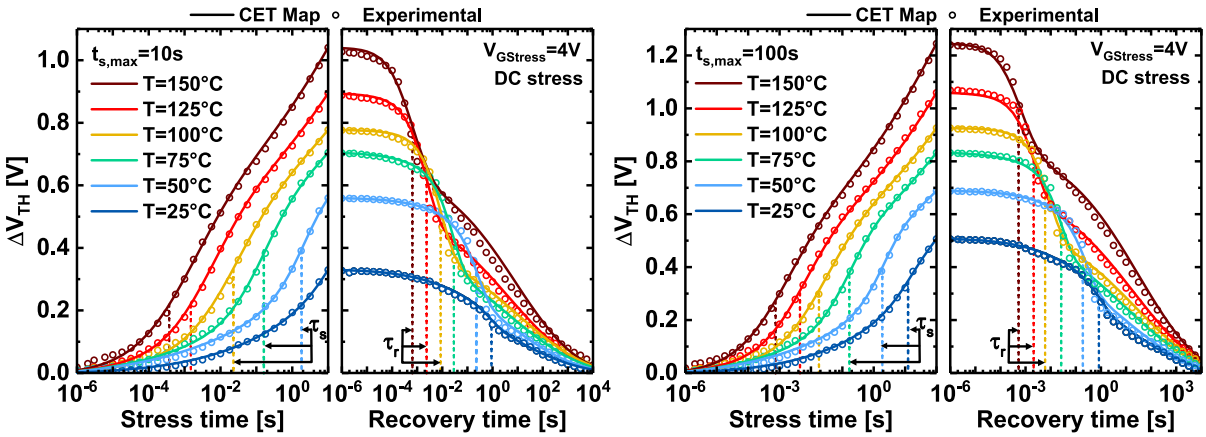

Figure 3.30. Comparison between experimental pBTI transients and ΔV_{TH} deduced from CET maps of Figure 3.29-left, during the stress and recovery phases, at different temperatures from 25 to 150°C. These latter transients have been obtained by applying a DC gate voltage stress of 4V. **Left -** Maximum stress time $t_{s,max}$ of 10s. **Right -** Maximum stress time of 100s.

In the next section, an Arrhenius analysis of the temperature dependent CET maps presented in Figure 3.29 is carried out to go further. It will enable to determine rigorously the nature of G_1 and G_2 trap density distributions.

3.5.3.3 Arrhenius analysis of the CET map

The temperature dependence of the time constants τ_c or τ_e (τ) of an individual traps follows an Arrhenius law such as,

$$\tau = \tau_0 \cdot \exp\left(\frac{q \cdot E_a}{k_B \cdot T}\right) \tag{3.49}$$

Where τ_0 is the elastic tunneling exchange time between the traps and the substrate carriers [357]. The latter parameter can be extracted using the following equation [358], [359], which links a time constant τ_{T1} obtained at a temperature T_1 to its equivalent time constant τ_{T2} obtained at a second temperature T_2 such as,

$$\tau_{T2} = \tau_0 \cdot \left(\frac{\tau_{T1}}{\tau_0}\right)^{T_1/T_2} \tag{3.50}$$

By solving equation 3.50, a τ_0 of 10^{-13}s has been obtained. Once τ_0 is obtained, it is possible to convert the CET maps presented in Figure 3.29-left into activation E_a maps for each temperature, giving the possibility to deduce the activation energy of different trap populations. The activation energy of G_1 and G_2 trap density distributions as a function of the temperature is presented in Figure 3.31-left.

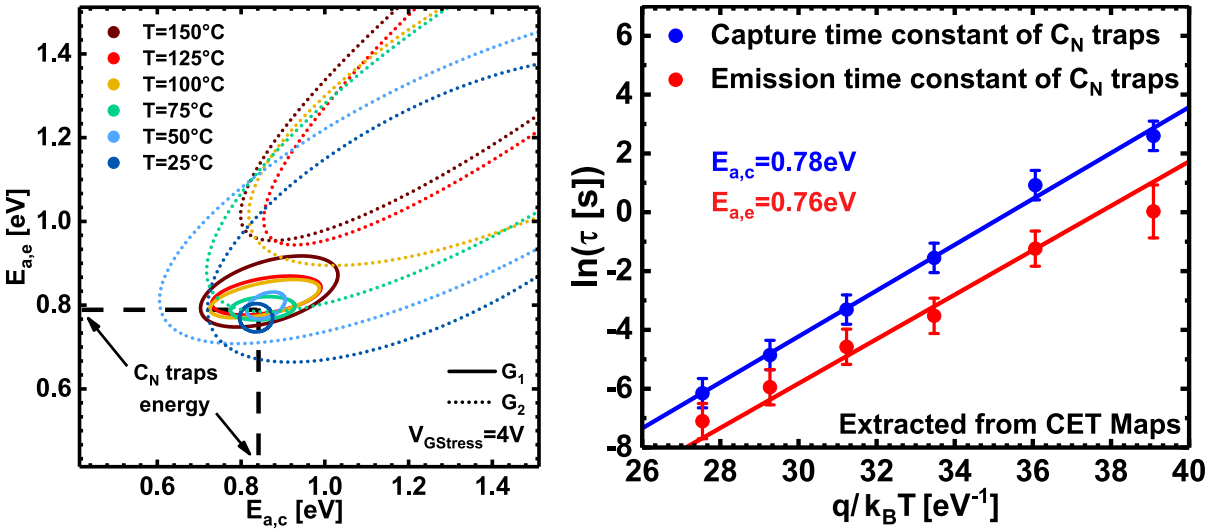

Figure 3.31. Left - Activation energy map deduced from Figure 3.29-left, for different temperatures T with $\tau_0 = 10^{-13}$ s. The activation energy of G_1 distribution is around $0.8-0.9$eV for all temperatures, while the activation energy of G_2 i between 0.7 and 1.5eV. **Right -** Arrhenius plot where the coordinates of G_1 centers extracted from the CET maps of 3.29-left are reported for each temperature. The extracted activation energies $E_{a,c}$ and $E_{a,e}$, corresponding to capture and emission time constants respectively are both around 0.8eV, confirming that C_N traps are involved in pBTI degradation.

It can be pointed out that the G_1 peaked Gaussian is located around $0.8-0.9$eV, which is consistent with the activation energy ascribed to C_N traps. In addition, the same activation of $E_{a,e} \approx E_{a,c} \approx 0.8$ eV is extracted by reporting the coordinates of G_1 centers (τ_c, τ_e) in an Arrhenius plot as shown in Figure 3.31-right. It thus confirms that G_1 is related to the C_N trap population. The latter results are also consistent with the activation energy extracted in the previous chapter, and confirms that a C_N trap population is involved in pBTI degradation. Figure 3.31-left also highlights that the second G_2 trap density distribution is ascribed to a defect band having an approximate energy range between 0.7 and 1.5eV for the different temperatures. This broad distribution of activation energies describes a trap state continuum associated to an Al_2O_3 defects band which should be located above the GaN conduction band. Indeed, during the recovery the trapped charges move towards the conduction band energy in order to minimize their energy, meaning that the trap energy of Al_2O_3 defects is certainly above the GaN conduction band, as illustrated in Figure 3.32-left. Finally, it is also interesting to note that this activation energy range ($0.7-1.5$eV) is consistent with the energy range of Al_2O_3 defects band reported by T.-L. Wu *et al.* using a different method [329]. In this study, an energy of $E_t = 1.15$ eV above the GaN conduction band with an energy spread σ_t of 0.42eV has been reported in [329], corresponding to an energy range of $0.73-1.57$eV. The defect density D_{ot} distribution within the Al_2O_3 defect band is expressed by the following expression, which is also illustrated in Figure 3.32-right.

$$D_{ot}(E,x) = \frac{D_{ot,0}}{\sigma_t \cdot \sqrt{2 \cdot \pi}} \cdot \exp\left(-\frac{E - E_t(x)}{2 \cdot \sigma_t^2}\right) \tag{3.51}$$

Where E is the energy within the Al_2O_3 bandgap,
x is the spatial position within the dielectric layer,
and $D_{ot,0}$ is a constant.

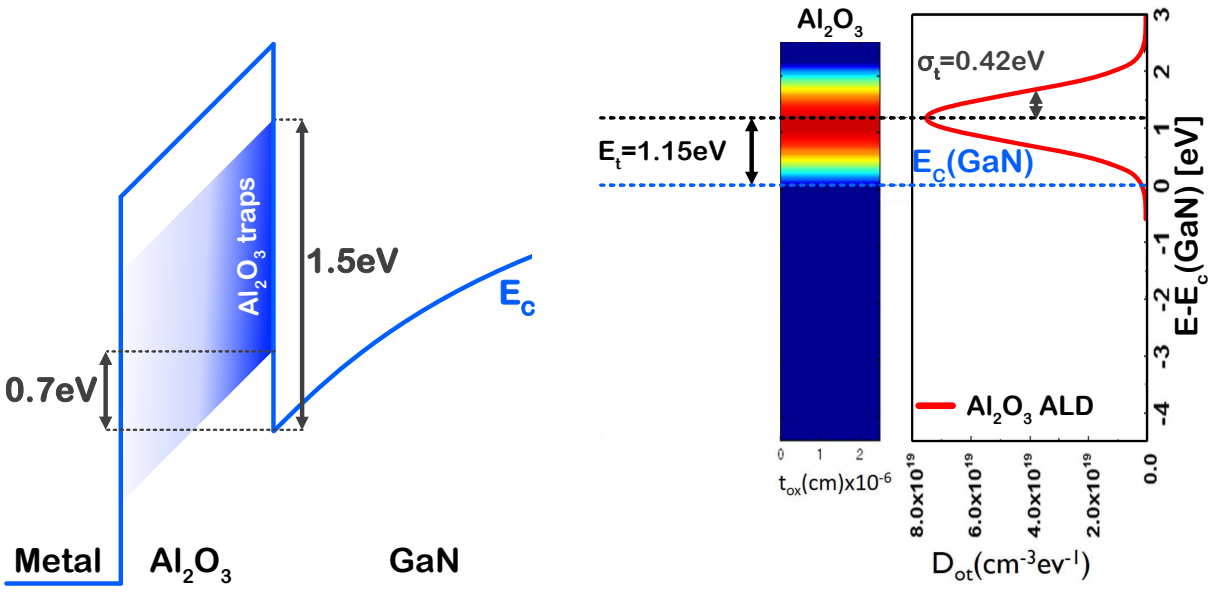

Figure 3.32. Left - Illustration of the Al_2O_3 defect band having an energy range between 0.7 and 1.5eV according to E_a maps in Figure 3.31-left. **Right -** An energy of $E_t = 1.15$ eV above the GaN conduction band with an energy spread σ_t of 0.42eV has been reported in [329], corresponding to an energy range of $0.73 - 1.57$eV. These results confirm the consistency of the energy range values of Al_2O_3 defect band extracted from 3.31-left.

3.5.3.4 Nature of Al_2O_3 defect band

Since the energy range related to the defective band Al_2O_3 has been determined and appears to be relevant by comparing our result with the study of T.-L. Wu *et al. et al.* [329], we sought to define the nature of this trap state continuum. To do so, a comparison of the Al_2O_3 defect band energy with the trap state level resulting from ab initio calculations has been carried out. In 2013, Minseok Choi *et al.* reported two studies on the energy levels that could theoretically be found in Al_2O_3 bulk [360], [361]. The first study was about the energy levels related to native point defects and dangling bond DB in Al_2O_3. Figure 3.33-left shows these results in a band diagram for α-Al_2O_3 and κ-Al_2O_3 which are two phases of Al_2O_3 [362]. However, note that α-Al_2O_3 is the most stable one. Superposing the energy range Al_2O_3 defect band of $0.7 - 1.5$eV on these theoretical results, the energy level related to an alumina defect bond Al_{DB} seems to be responsible for the defect band in the case of α-Al_2O_3. In the case of κ-Al_2O_3, the energy level related to Al atoms in oxygen sites Al_O seems to be at the origin of the defect band [360]. However this assumption has to be verified by further experimental studies. In his second paper, M. Choi studied the influence of traps levels of carbon in nitrogen impurities [361]. As illustrated in Figure 3.33-right, by comparing the energy range of the Al_2O_3 defect band around $0.7 - 1.5$eV with these theoretical results, the energy level related to C traps in Al sites C_{Al}

seems to be responsible for the defect band in the case of α-Al_2O_3 here [361]. Since Al_2O_3 is deposited using a Trimethylaluminum precursor (TMA) which is a molecule composed of carbon elements ($Al_2C_6H_{12}$), the fact that carbon impurities are involved in pBTI degradation is relevant, and has to be considered. In addition, M. Uenuma *et al.* recently demonstrated that TMA using as precursor leads to pBTI degradation as shown in Figure 3.34 [363].

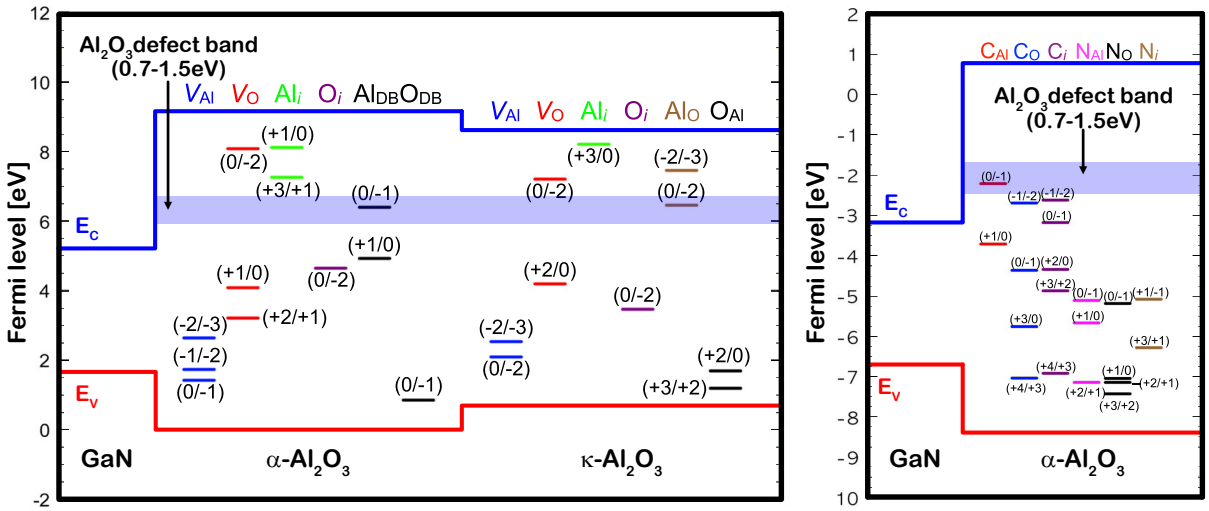

Figure 3.33. Left - Band alignment between α-Al_2O_3, κ-Al_2O_3 and GaN. The energy reference corresponds to the valence band minimum of α-Al_2O_3. The position of thermodynamic transition levels for native point defects and dangling bonds (Al_{DB} and O_{DB}) in α-Al_2O_3 is shown with respect to GaN band edges [360]. **Right -** Band alignment between semiconductor GaN and Al_2O_3. The positions of charge-state transition levels for C and N impurities in Al_2O_3 are shown within the oxide band gaps and relative to the GaN band edges. The zero corresponds to the vacuum level with the GaN band-edge positions [361].

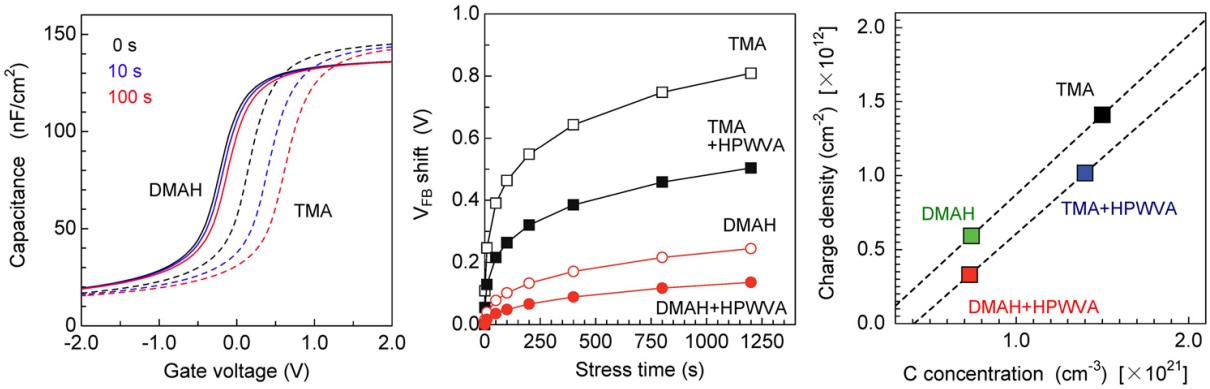

Figure 3.34. Left - $C(V_G)$ characteristics obtained by applying a gate voltage of 5V during 10 and 100s, for two samples having a gate oxide layer Al_2O_3 obtained differently. One being obtained with the TMA precursor (dotted line) and the other with the dimethyl aluminum hydride (DMAH: $Al(CH_3)_2H$) precursor (solid line). **Middle -** $C(V_G)$ shift as a function of stress-time evolution by varying the precursor used to obtained Al_2O_3. A gate stress voltage of 5.0V is applied here. **Right -** Charge trap density as a function of carbon concentration for different Al_2O_3 precursor. Charge trap density has been deduced using the $C(V_G)$ shift after a gate stress voltage of 7V during 1200s [363].

Conclusion

In this chapter we first presented the SRH model that considers defects in the channel allowing to obtain the capture and emission time constants of traps. Although it has been clearly shown experimentally that capture and emission processes are related to an underlying-mechanism dependent on the temperature, the SRH model is more or less independent of temperature. It is the reason why the NRMP model has been explored.

In a second time, the NRMP model proposed by Tibor Grasser in the frame of hole trapping modeling has been presented. It has been demonstrated that the Markov chains resolution in the frame of a three-state model enables to deduce analytical expressions of emission time constants. However, the NRMP model requires a large number of parameters to physically determine these time constants. Among these parameters, a certain number of parameters are impossible to determine experimentally and become "fitting" parameters. By injecting the time constants in the SRH equation, the possibility to calculate the charge state (filled or empty) of the traps over time has been demonstrated, enabling to reproduce the global degradation behavior. However it has been shown that the trapping and detrapping kinetics predicted by the model do not reproduce the nBTI transient dynamics obtained experimentally, although the degradation behavior after stress and relaxation are relatively well predicted by the model. According to A. Subirats, this poor evaluation comes from the numerous parameters required to run the model, and in particular to simulate the capture and emission time constants of the traps. For this reason, the NRMP model was not chosen to reproduce the BTI degradation obtained on GaN-based HEMTs.

A Capture Emission Time (CET) map approach has been used for a better understanding of the pBTI degradation kinetics obtained in our device. Although this last model is farther from the physical reality of the underlying mechanisms of BTI degradation, it is very useful to model and predict V_{TH} instabilities. It is based on an RC parallel network where each subcircuit model a trap with a unique capture and emission time constant couple. The charge state (0 or 1) of each trap modeled by the RC circuits of the network can be illustrated by a "Filling map", while the trap density is defined by a CET map. Unlike the filling map, the CET Map is deduced from the experimentally measured BTI transients. The convolution of both gives a BTI shift. Beyond enabling the study of trap populations density, the CET map approach allows to model and predict the DC and AC pBTI transients. Moreover, the analysis of temperature-dependent CET maps enables the deduction of the activation energy of both trap population densities. One of them has an activation energy of $0.8-0.9$eV and is related to a C_N traps population related to buried GaN:C layer. In the other hand, the other one is associated with an energy range between 0.7 and 1.5eV ascribed to an Al_2O_3 defects band above the GaN conduction band energy.

An energy of $E_t = 1.15$ eV above the GaN conduction band with an energy spread σ_t of 0.42eV has also been reported in [329], corresponding to an energy range of $0.73-1.57$eV. These results thus confirm the consistency of the energy range values of Al_2O_3 defect band extracted from our E_a map. Comparing this energy range with abinitio calculations, we found that the energy level related to Al_{DB} traps seems to be responsible for the defect band in the case of α-Al_2O_3. In the case of κ-Al_2O_3, the energy level related to Al atoms in oxygen sites Al_O seems to be at the origin of the defect band. The energy level related C traps in Al sites C_{Al} can be also responsible to the defect band in the case of α-Al_2O_3 [361]. These results are also consistent with the carbon presence in the TMA precursor used to deposit alumina. Finally, M.

Uenuma *et al.* recently demonstrated that using TMA as an Al_2O_3 precursor leads to a pBTI degradation amplification [363]. In any case further studies need to be carried out to know if these assumptions are valid.

4

Gate layout influence on BTI degradation

This chapter is ascribed to the influence of the gate layout on the pBTI degradation. The difference between $I_D(V_G)$ and $C(V_G)$ pBTI drift is first presented and constitutes one of the two parts of the chapter. An innovative experimental setup developed for this study enables fast and simultaneous $I_D(V_G)$ and $C(V_G)$ measurements. We demonstrated that it is possible to know where the charge trapping occurs at the gate-oxide interface, based on the experimental results and complementary TCAD simulations. In the second part, the gate length influence on pBTI degradation is discussed. It was observed that the pBTI degradation is enhanced when the gate length L_G increases at fixed gate stress voltage due to a V_{TH} roll-up behavior. Additional TCAD simulations were performed to improve our understanding of the relationship between gate length and initial threshold voltage. Results showed that this V_{TH} roll-up behavior is implied by the back-barrier presence within the epitaxial structure.

Contents

4.1 Difference between $I_D(V_G)$ and $C(V_G)$ pBTI shifts

In this section, the difference between $I_D(V_G)$ and $C(V_G)$ pBTI shifts under various gate voltage stresses and temperatures are investigated. An innovative experimental setup using ultra-fast and simultaneous $I_D(V_G)$ and $C(V_G)$ measurements enables to record the V_{TH} drift through two metrics, ΔV_{THI} and ΔV_{THC}. A difference between ΔV_{THI} and ΔV_{THC} has been observed on experimental pBTI results. Further TCAD simulations support that $I_D(V_G)$ shift (ΔV_{THI}) is ascribed to charge injection in Al_2O_3 gate oxide defects at the gate corner regions while $C(V_G)$ shift (ΔV_{THC}) is mainly related to the gate bottom. It is due to the presence of the back-barrier layer in the epitaxial structure. The latter results allow to deduce that the Al_2O_3 defect density is more important at the gate corners than at the gate bottom. All these different aspects will be developed in the following sections.

4.1.1 Device Specification

4.1.1.1 Description of the tested transistor structure

In this study, the tested transistors are similar to those presented in chapter 2. As a reminder, the epitaxial structure includes a thick transition layer for stress management, followed by a thick (> 1 µm) C-doped GaN layer to provide high vertical and lateral breakdown voltage as well as electrical insulation. Next, a back-barrier layer is deposited to adjust the threshold voltage, followed by an unintentionally doped GaN layer (GaN:UID) used as a conductive channel. An AlGaN barrier epitaxy is then performed on GaN to create the 2DEG, followed by the growth of a SiN passivation layer. Afterwards, ICP RIE etching is used to strip off the top passivation layers, the AlGaN barrier and part of the GaN:UID layer in order to create the MOS gate. Subsequently, a 30nm-thick Al_2O_3 gate oxide layer is deposited by ALD in the recessed cavity, prior to the deposition of the gate metal. A representation of the GaN-on-Si MOSc-HEMTs architecture is provided in Figure 4.1. Regarding the transistor design, all tested transistors have a gate length of 0.5µm, while the gate width W_G is 8mm. The source to gate distance L_{GS} and source to drain distance L_{GD} are both constant.

4.1.1.2 Electrical properties of the pristine device

During the switch toward On-state, electrons accumulate at the gate oxide interface to form a conductive channel connecting the drain and the source via the 2DEG. This charge accumulation is not homogeneous along the entire gate oxide interface as shown in Figure 4.2-left, whose results are provided by TCAD simulations. It displays the conduction band energy distribution E_C in GaN at $V_G = 0$ V, showing that E_C is higher at the gate corners than at the gate bottom. Such effect is due to the back-barrier presence which lead to the stretching of the electric field iso-lines under the gate, and thus to a local conduction band increase at the gate corners. A direct image of the local V_{TH} value along the Al_2O_3 gate oxide interface is given by the conduction band energy. Consequently, the threshold voltage of $I_D(V_G)$ characteristic (V_{THI}) is controlled by the gate corners, while the threshold voltage of $C(V_G)$ characteristic (V_{THC}) is controlled by the gate bottom. Such effects automatically lead to a mismatch between $I_D(V_G)$ and $C(V_G)$ characteristics, such that V_{THI} is higher than V_{THC}. Indeed, for a specific range of applied gate voltage such as $V_{THC} < V_G < V_{THI}$, carriers can be accumulated at the gate bottom while they cannot move to the drain due to the higher value of the conduction band energy at

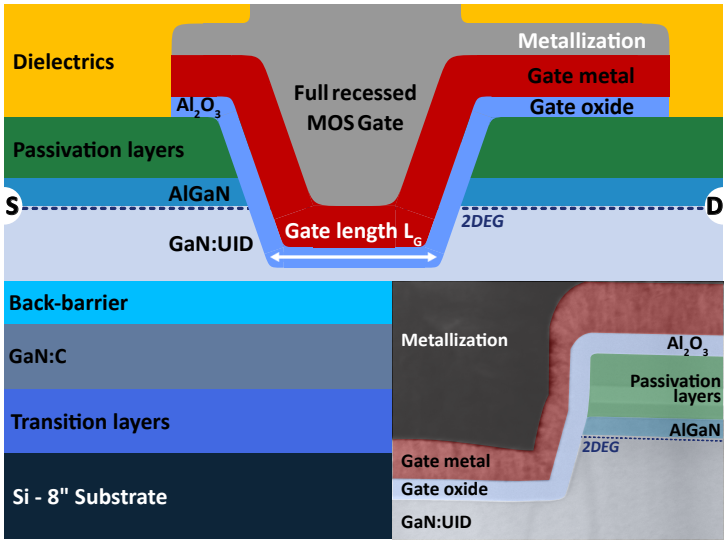

Figure 4.1. Illustration of the fully recessed GaN-on-Si E-mode MOSc-HEMT, and the various layers that are integrated within the GaN-based epitaxial structure. The TEM cross-section depicts the fully recessed MOS gate profile at the right corner.

the gate corners than at the bottom of the gate. The conduction band energy at the gate corners act as a potential barrier for electrons located at the gate bottom. It thus results in a significant capacitance value but a negligible drain current.

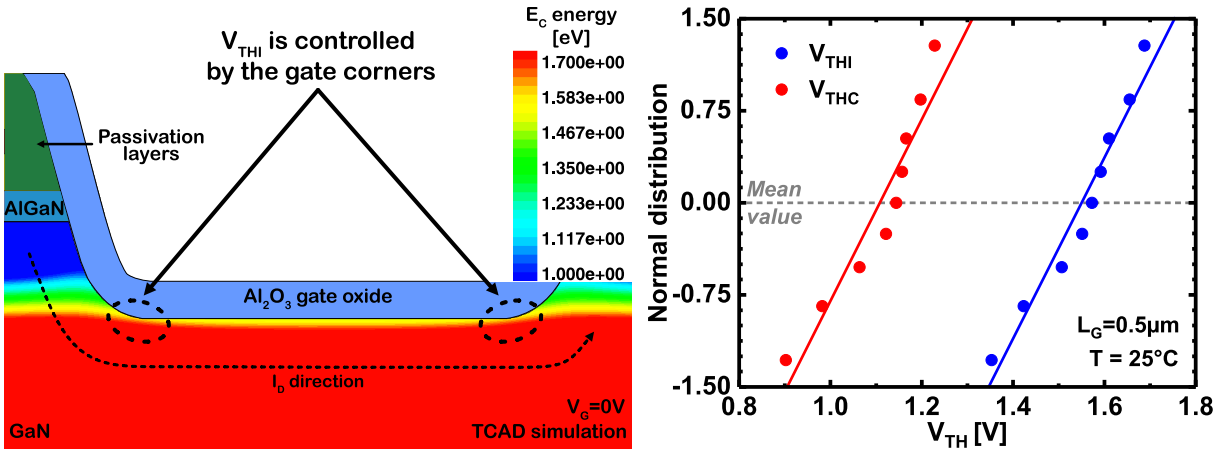

Figure 4.2. Left - TCAD simulations providing the GaN conduction band energy E_C distribution at $V_G = 0$ V for $L_G = 0.5$ µm. It can be observed that the $I_D(V_G)$ threshold voltage V_{THI} is driven by the gate corners, while V_{THC} is controlled by the gate bottom due to the presence of a back-barrier layer. **Right -** Normal distribution of V_{THI} and V_{THC}, with an average value around of 1.55V and 1.1V, respectively. These results confirm the consistency of the conduction band energy distribution illustrated on the left.

The simulation consistency presented in Figure 4.2-left is confirmed by experimental measurements of V_{THI} and V_{THC} presented in 4.2-right. It shows that both V_{THI} and V_{THC} parameters follow a normal distribution, with a similar standard deviation. It is also worth noticing that V_{THI} average value is around 1.55V, which is higher than V_{THC} mean value which is about 1.1V. Note that V_{THI} was extracted at a fixed drain current of $I_D = I_0 \cdot (L_G/W_G)$,

where I_0 is fixed to 20nA. On the other hand, V_{THC} is extracted at a fixed capacitance of $C = (C_{max} + C_{min})/2$. In this study, these values will always be extracted in this way.

4.1.2 Experimental setup

4.1.2.1 Experimental setup description

The procedure of the pBTI stress-measurement (MSM) technique under DC or AC gate voltage stress is schematically displayed in Figure 4.3-left and is similar to the one used in section 2.3 of chapter 2. A fixed and positive gate voltage stress is applied for a stress time ranging from 10^{-6}s to 10^{3}s at a constant temperature T. During the stress phase, fast gate voltage ramps (< 10 µs) are applied using a Keysight B1530 with a Wave Generator / Fast Measurement Unit (WGFMU) to monitor V_{TH} drift in order to minimize unwanted recovery. Upon the end of the stress phase, the latter is followed immediately (< 10 µs) by the recovery phase, where the gate voltage stress is set to the ground during 10^{3}s and the V_{TH} recovery is measured using the same fast V_G ramps. Note that the drain voltage V_D is set to 0V during the stress and recovery phases while it is fixed to 50mV during the fast gate voltage ramps.

In this study, an innovative experimental setup allowing to simultaneously measure the $I_D(V_G)$ and $C(V_G)$ characteristics at very short times (< 10 µs) has been implemented. Figure 4.3-right illustrates the experimental setup principle which consists in connecting a WGFMU to the gate (WGFMU 1) and a second one to the drain (WGFMU 2) of the tested transistor, while the source is grounded. During a fast gate voltage ramp applied by WGFMU 1, the gate current I_G as well as the drain current I_D are both recorded using WGFMU 1 and WGFMU 2 respectively, while the drain voltage V_D is fixed at 50mV via WGFMU 2.

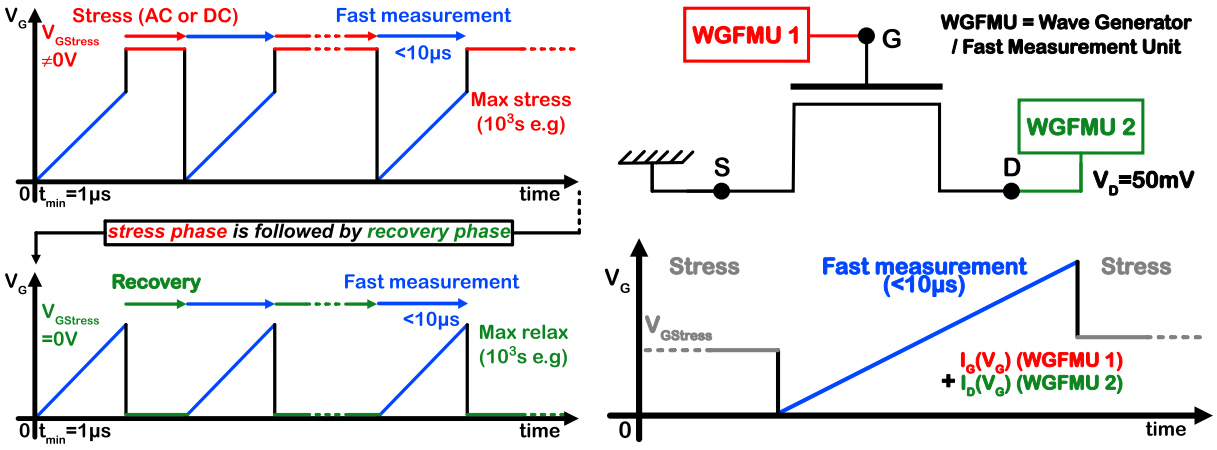

Figure 4.3. Left - BTI measurement principle using ultra-fast V_{TH} (< 10 µs) measurements to minimize unwanted recovery, during the stress (top) and recovery (bottom) phases. The stress phase ($V_{GStress} \neq 0$ V) is immediately followed by the recovery phase ($V_{GStress} = 0$ V). **Right -** Representation of the experimental setup. During the fast gate voltage ramp applied by WGFMU 1, the drain voltage is fixed at 50mV using WGFMU 2 (top). At the same time, the displacement current I_G as well as drain current I_D are recorded by WGFMU 1 and WGFMU 2, respectively (bottom). A $C(V_G)$ characteristic is then deduced from $I_G(V_G)$ measurement using formula 4.1.

The gate current I_G consists in the sum of a leakage current I_{Leak} and a displacement current I_{Dis}. By isolating I_{Dis}, it is possible to deduce a $C(V_G)$ characteristic using the following expression,

$$I_{Dis} = C \cdot \frac{dV_G}{dt} \tag{4.1}$$

As described in formula 4.1, it can be noted that the faster the V_G ramp (dV_G/dt), the higher the order of magnitude of the displacement current. This is very interesting to improve the I_{Dis} signal quality when it is noisy and not suitable for the resolution of the WGFMU measurement.

It is possible to deduce the leakage current and to subtract it from I_G in order to isolate I_{Dis}. Indeed, by connecting a third WGFMU3 to the source and measuring the source current I_S, the leakage current I_{Leak} can be obtained such as $I_{Leak} = |I_D| - |I_S|$. In our case, the gate oxide thickness Al_2O_3 is relatively high and then the leakage current can be considered negligible since $I_{Leak} \sim 10^{-13}$ A compared to the order of magnitude of the displacement current $I_{Dis} \sim 10^{-6}$ A, which permits to consider that I_G is equivalent to the displacement current.

4.1.2.2 Experimental setup evaluation

It is worth noticing that a high drain voltage can affect the $C(V_G)$ characteristic integrity. Indeed, when a drain voltage is applied, the potential difference V_{GD} is different from V_{GS}. As a result, distortions are induced on the $C(V_G)$ characteristics. Figure 4.4 exhibits the $C(V_G)$ curves obtained when applying different drain voltages from 0V (reference) to $V_D = 200$ mV.

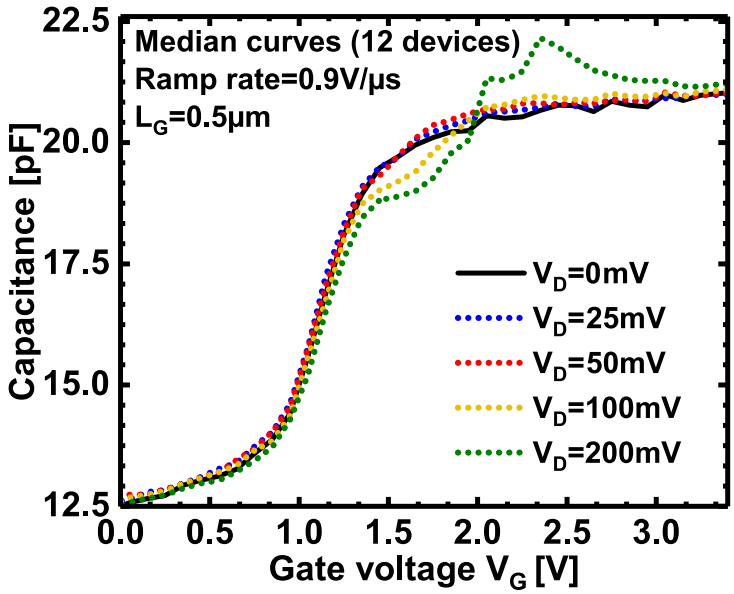

Figure 4.4. $C(V_G)$ characteristics measured at various drain voltages V_D, and deduced from the displacement current $I_{Dis}(V_G)$ obtained via the application of a fast gate voltage ramp (< 10 µs). It can be observed that the influence of a drain voltage below 100mV is negligible on $C(V_G)$ characteristics. Hence, it enables the $I_D(V_G)$ measurement simultaneously.

It can be clearly observed that when drain voltage is higher than 100mV, a distortion of the $C(V_G)$ curves occurs compared to the reference characteristic ($V_D = 0$ V). However, the influence of drain voltage below 100mV is negligible on $C(V_G)$ characteristics, which enables to

measure the drain current during the same fast V_G ramp. Therefore, Figure 4.4 demonstrates that it is technically possible to simultaneously monitor the pBTI $I_D(V_G)$ and $C(V_G)$ shifts (ΔV_{THI} and ΔV_{THC} respectively) during the same gate voltage stress. Figure 4.5-left displays the $I_D(V_G)$ characteristics measured during $V_{GStress} = 5$ V for 10^3s at room temperature, and Figure 4.5-right, the $C(V_G)$ characteristics measured simultaneously. V_{THC} is being controlled by the gate bottom while V_{THI} by the gate corners, ΔV_{THI} and ΔV_{THC} should behave differently during gate stress. It can already be noticed in Figure 4.5 that ΔV_{THI} is slightly higher than ΔV_{THC}. This difference between both metrics will be extensively studied in the following sections.

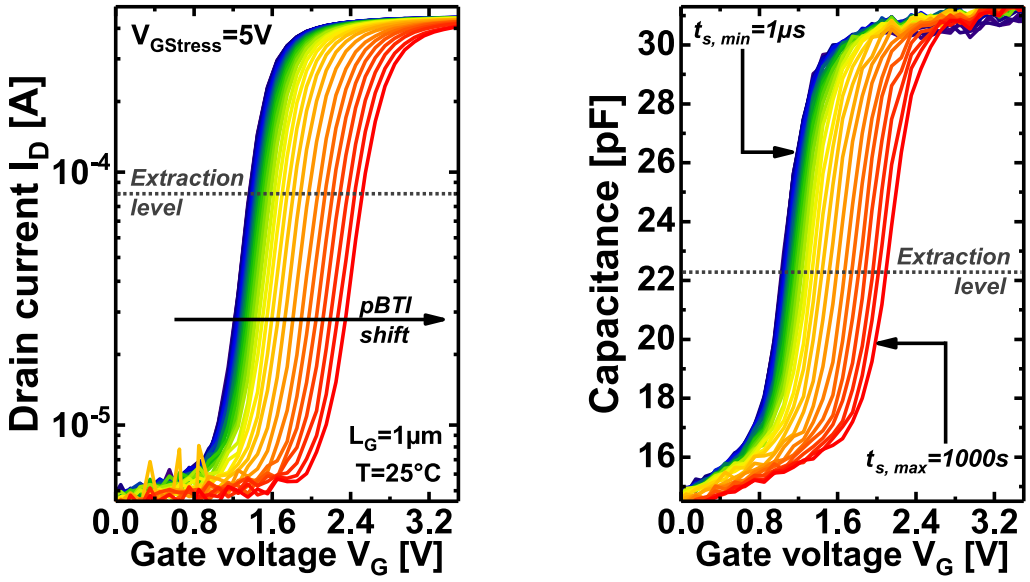

Figure 4.5. $I_D(V_G)$ characteristics (left) and $C(V_G)$ characteristics (right) measured simultaneously during a gate voltage stress of 5V for 10^3s and at 25°C. V_{DS} is fixed at 50mV during each fast V_G ramps. These plots demonstrate the possibility to monitor simultaneously the $I_D(V_G)$ and $C(V_G)$ pBTI shifts during a gate voltage stress.

4.1.3 PBTI experimental results

4.1.3.1 Analysis of the difference between ΔV_{THI} and ΔV_{THC}

$I_D(V_G)$ and $C(V_G)$ drift (ΔV_{THI} and ΔV_{THC}) obtained at gate stress voltages ranging from 1 to 5V and at room temperature are shown in Figure 4.6. We can notice that they have a very similar behavior to the transients shown in section 2.3. Indeed, during the stress phase, a significant acceleration of the pBTI drift can be observed around 10s on whole stress transients, revealing the time constant τ_s. When the gate voltage stress is lower than 2V, the pBTI shift is negligible before τ_s and suddenly increases at τ_s, followed by a ΔV_{THI} and ΔV_{THC} transient saturation . On the other hand, when a high $V_{GStress}$ is applied (> 2 V), the pBTI shift increases monotonously before and after τ_s. This rising corresponds to a strong acceleration at τ_s as well as an increase of trapping dynamics as $V_{GStress}$ increases. A difference between ΔV_{THI} and ΔV_{THC} that rises significantly with $V_{GStress}$ and stress time can be also noted. During the recovery phase, an abrupt decrease of pBTI drifts is observed at about 1s on all transients, independently on $V_{GStress}$, thus revealing a second time constant τ_r. When a gate voltage stress

below 2V is applied, both ΔV_{THI} and ΔV_{THC} are stable at the beginning of recovery until they abruptly decrease at τ_r towards a negligible value. When $V_{GStress}$ is higher than 2V, pBTI drift begins to decrease monotonously at low relaxation times ($\sim 10^{-4} - 10^{-3}$ s) and continues after τ_r, with a sharp decrease of ΔV_{TH} at τ_r. It can also be observed that the difference between ΔV_{THI} and ΔV_{THC} decreases monotonously with increasing recovery time.

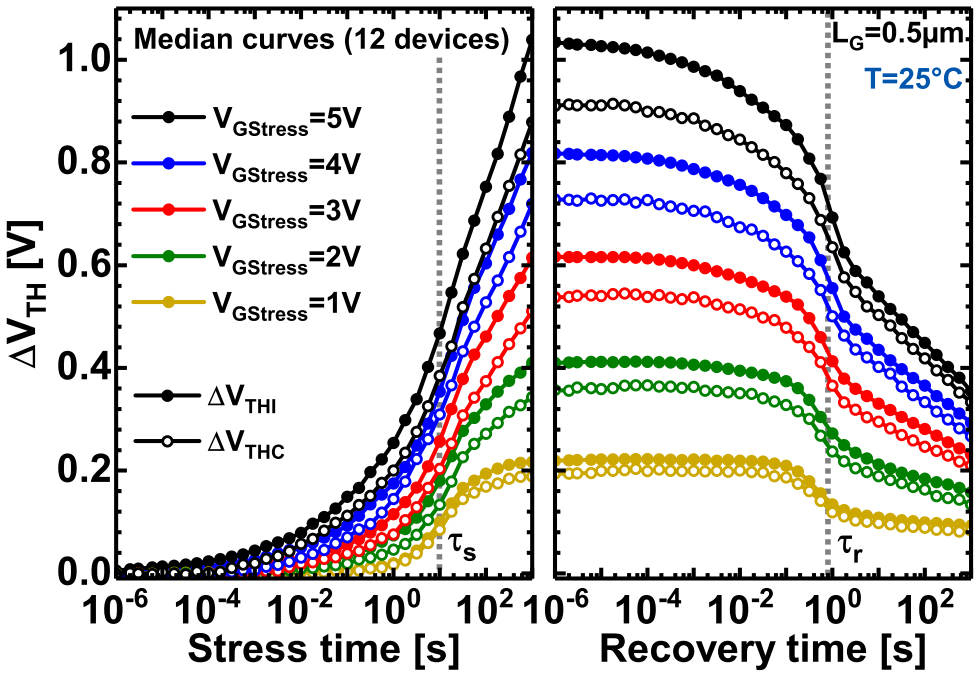

Figure 4.6. Stress and recovery pBTI transients obtained under various gate stress during 10^3s at 150°C. It can be also noted that both time constants τ_s and τ_r are strongly activated with T by being at 10^{-3}s and $2 \cdot 10^{-3}$s, respectively. After 10^{-4}s of gate stress, a difference between ΔV_{THI} and ΔV_{THC} can be noticed, notably for $V_{GStress}$ above 2V. At low $V_{GStress}$, this difference can be considered as negligible.

PBTI stress and recovery transients obtained at a temperature of 150°C for different $V_{GStress}$ are presented in Figure 4.7. Firstly, a strong reduction of both time constants τ_s and τ_r can be observed. Indeed, their values are around 10^{-3}s and $2 \cdot 10^{-4}$s at 150°C, while they were respectively about 10 and 0.1s at room temperature. Moreover, a more significant degradation can be observed at high temperature, especially when a $V_{GStress}$ higher than 2V is applied. At low gate voltage, a pBTI stabilization after τ_s during the stress phase and an abrupt pBTI recovery at τ_r during relaxation phase can also be observed at 150°C. Finally, a difference between ΔV_{THI} and ΔV_{THC} can also be noticed at high temperature, especially when the gate voltage stress is higher than 2V. However, when a low $V_{GStress}$ is applied (< 2 V), this difference becomes negligible.

Although the applied gate voltages stress is not exactly the same, the stress and recovery pBTI transients behavior presented in Figures 4.5 and 4.6 are strongly similar to the one presented in section 2.3 of chapter 2. In the latter, the pBTI strong variation was associated with the time constants τ_s and τ_r. They were explained by the C_N trap ionization within the GaN:C layer, which can be activated at very low positive gate voltage stresses (< 1.5 V). At high $V_{GStress}$, an electron injection mechanism into the gate oxide defects occurred. Consequently, the pBTI degradation is the result of a combination of both mechanisms. In the next section, the presence

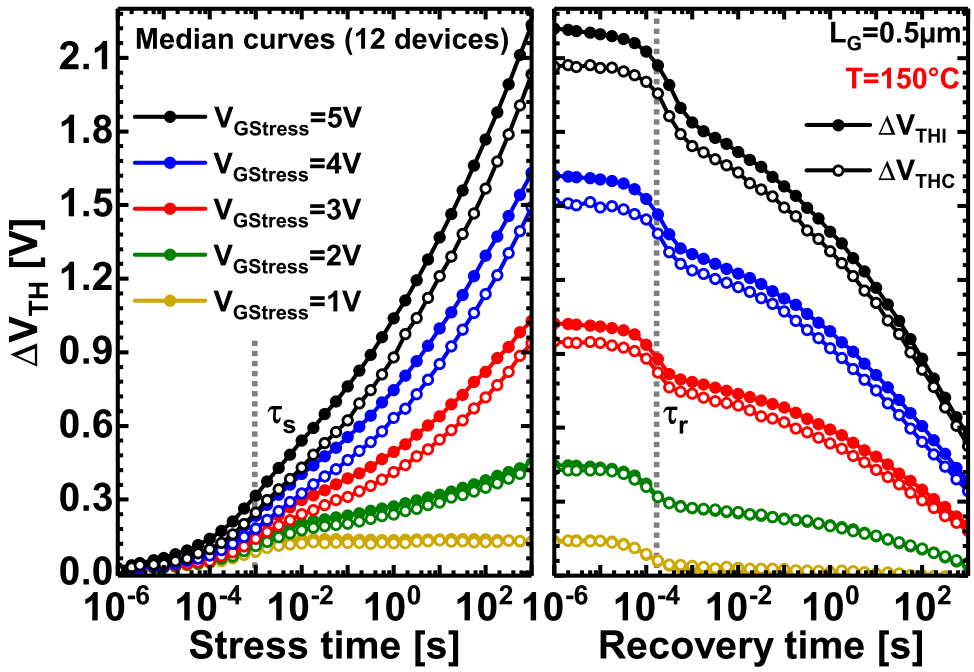

Figure 4.7. ΔV_{THI} and ΔV_{THC} transients obtained at 25°C for various $V_{GStress}$ from 1 to 5V. After 10s of gate stress, a difference between ΔV_{THI} and ΔV_{THC} can be observed, as well as a strong pBTI drift variation at time constants τ_s and τ_r.

of these trap populations will be verified via temperature dependent measurements and Arrhenius analysis.

4.1.3.2 Trap population identification involved in pBTI

Stress and Recovery pBTI transients performed at different temperatures from 25°C to 175°C and at a gate voltage stress of 1V are presented in Figure 4.8. The ΔV_{THI} and ΔV_{THC} transients are shown in Figures 4.8-left and 4.8-right, respectively. We can note that these latter are very similar since they all show the time constants τ_s and τ_r. As observed in the previous section, we can remark that the time constants τ_s and τ_r are both related to a strong and punctual ΔV_{TH} variation followed by a stabilization. Furthermore, they are both strongly activated with temperature. According to these observations, it is likely that they are both related to the same trap population, which would activate at low $V_{GStress}$.

Same pBTI transients under $V_{GStress} = 2$ V are shown in Figure 4.9. There are clearly two temperature dependencies depicted in pBTI transients, thus suggesting that two distinct trap populations are involved in the ΔV_{TH} degradation at this gate voltage stress. The first one is attributed to the time constants τ_s and τ_r, which are both associated with a punctual ΔV_{TH} shift and a strong temperature dependency, such that they decrease with increasing temperature. The signature of the second trap population is mainly visible after τ_s and τ_r during the stress and recovery phase, respectively. It is depicted by a lower temperature dependency and trapping rate, which rises as temperature increases. The monotonous variation of ΔV_{TH} related to the second trap population can be modeled by a broad distribution of time constants, as shown by the capture emission time map presented in section 3.5 of chapter 3. As explained in section 2.3 of chapter 2, this behavior is commonly explained by charge trapping in the Al_2O_3 gate oxide

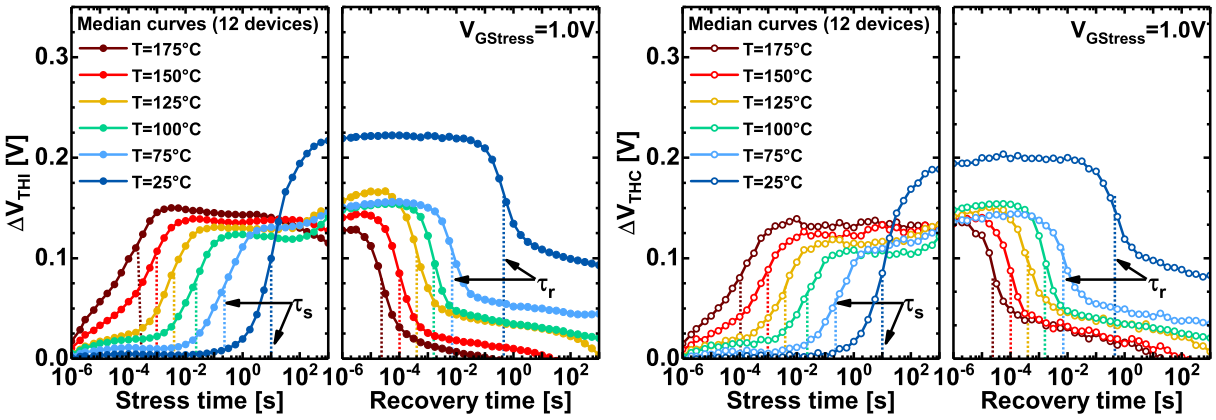

Figure 4.8. PBTI stress and recovery transients, obtained after 10^3s at different temperatures and at a fixed gate voltage stress of 1V. It can be noticed that the time constants τ_s and τ_r are related to strong and punctual ΔV_{TH} variation followed by a stabilization. They are also strongly activated with temperature. **Left -** PBTI shift extracted from $I_D(V_G)$ characteristics. **Right -** Threshold voltage drift of $C(V_G)$ characteristics.

defects, induced by a positive gate voltage stress [141], [302], [327], [329], [333], [339]–[342].

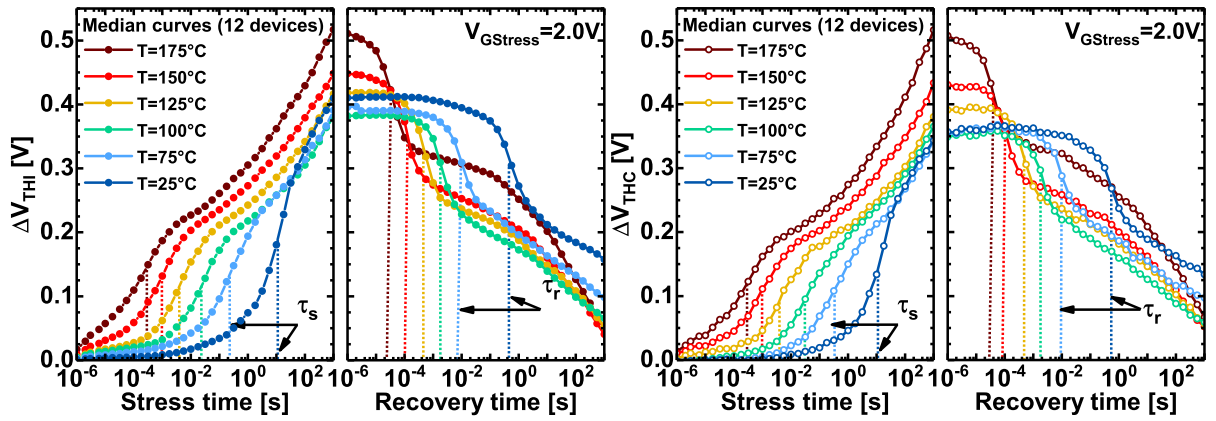

Figure 4.9. PBTI stress and recovery transients, obtained after 10^3s at a fixed gate voltage stress of 2V for different temperatures. It can be noticed that there are two temperature dependencies, thus suggesting that two different trap populations are involved in pBTI degradation at this specific gate voltage stress. **Left -** Threshold voltage drift of $I_D(V_G)$ characteristics. **Right -** PBTI drifts of $C(V_G)$ characteristics.

An Arrhenius analysis of τ_s and τ_r was performed to identify the nature of the associated trap populations. In the same way as the previous chapters, the stress and recovery pBTI transients extracted from $I_D(V_G)$ characteristics were fitted by a moderate order polynomial function (between 5 and 7) from which was derived $\partial\Delta V_{THI}/\partial\log(t)$ to extract both τ_s and τ_r. Thereafter, extrema positions of the derivative curves that are respectively correlated with τ_s and τ_r were extracted at each temperature, and for different gate voltage stresses from 0.5 to 4V. By plotting the two time constants as a function of $q/k_B \cdot T$ in the Arrhenius plots shown in Figure 4.10, an activation energy E_a around $0.8-0.9$eV is extracted for both time constants and for all gate voltage stress. As mentioned several times in the three previous chapters, this activation energy has been reported many times in literature [94], [95], [101], [104], [271], [343], [344]. It is

generally attributed to C traps in the N sites of the GaN lattice (C_N) that act as deep acceptors around $0.8-0.9$eV above the GaN valence band E_C. This new set of data is perfectly consistent with the results presented in section 2.3. It thus confirms that a population of C_N traps is involved in the pBTI degradation as demonstrated in chapter 2 and 3.

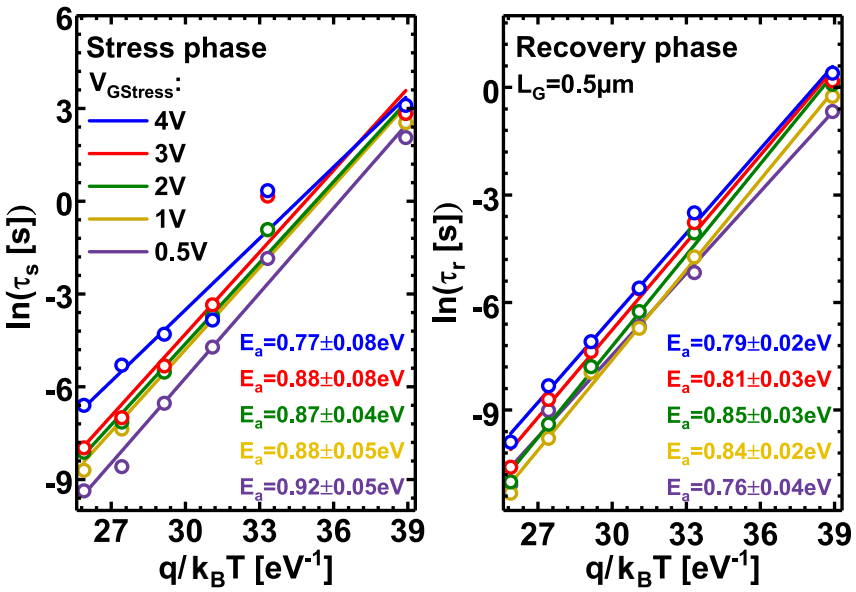

Figure 4.10. Arrhenius plots of time constants τ_s (left) and τ_r (right) for different gate voltage stress from 0.5 to 4V. An activation energy $E_a \approx 0.8-0.9$ eV is extracted for different $V_{GStress}$ and for both time constants. This activation energy value is related to C in the N sites of the GaN lattice, acting as deep acceptors around $0.8-0.9$eV above the GaN valence band. These results highlight that a population of C_N traps is implicated in pBTI degradation, and support that τ_s and τ_r are related to the same trap population.

Results provided in this section thus support the conclusions presented in section 2.3. As a reminder, the transient simulations (obtained by TCAD) presented in section 2.3, demonstrated that a part of C_N traps located in GaN:C layer are neutral. The latter traps can be ionized ($0 \rightarrow -$) at a positive gate voltage stress below 1.5V. It then implies a conduction band energy rise at the gate oxide interface (Al_2O_3/GaN), and thus a V_{TH} increase. During the recovery phase, the C_N traps go back to their initial neutral state, which leads to a conduction band energy decrease at Al_2O_3/GaN interface and thus a reduction of V_{TH}. It was also shown that the trapping regime depends on the applied $V_{GStress}$ due to the influence of two different trap populations. One is attributed to C-trap acceptors (C_N) located in the GaN:C layer, while the other is related to a defect band in the gate oxide Al_2O_3, close to interface with GaN. Both trap populations are involved in the V_{TH} instabilities via two different underlying mechanisms. A gate voltage stress below 1.5V is sufficient to activate ionization of the neutral C_N traps ($0 \rightarrow -$) and leads to an increase in the conduction band energy at the Al_2O_3 gate oxide interface, whereas electron injection into the Al_2O_3 traps is activated at a high $V_{GStress}$ (> 1.5 V).

4.1.3.3 Underlying mechanism ascribed to the difference between ΔV_{THI} and ΔV_{THC}

The ΔV_{THI} and ΔV_{THC} drifts obtained after a 10^3s stress versus $V_{GStress}$ value for different temperatures from 25 to 175°C is presented in Figure 4.11. It shows that there is a difference

between ΔV_{THI} and ΔV_{THC} at all temperatures, such as V_{THC} is lower than ΔV_{THI}. Furthermore, the discrepancy between ΔV_{THI} and ΔV_{THC} rises as the gate voltage stress increases and becomes significant when the $V_{GStress}$ is above 1.5V. Given the above results, the shift between ΔV_{THI} and ΔV_{THC} is hence mainly related to charge trapping within the Al_2O_3 defects.

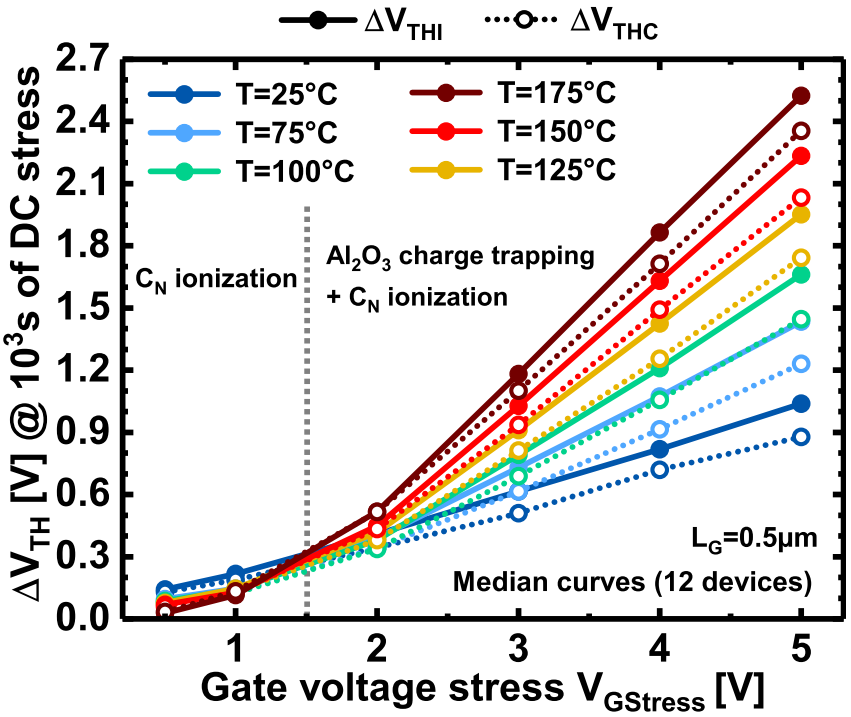

Figure 4.11. ΔV_{THI} and ΔV_{THC} shifts obtained after 10^3s as a function of gate voltage stress at different temperatures T. A discrepancy between ΔV_{THI} and ΔV_{THC} mostly appears for $V_{GStress}$ above 1.5V can be observed, and shows that it is most likely ascribed to charge trapping in Al_2O_3 defects band.

4.1.4 Results interpretation through TCAD simulations

4.1.4.1 TCAD simulation principle

As mentioned at the beginning of this section via Figure 4.2, the threshold voltage of $I_D(V_G)$ characteristic is driven by the gate corners while V_{THC} is mainly controlled by the gate bottom due the presence of back-barrier within the epitaxial structure. Furthermore, the results presented in Figure 4.11 exhibits that the discrepancy between ΔV_{THI} and ΔV_{THC} is mainly related to electron trapping in Al_2O_3 defects band. Based on these aspects, the TCAD simulation principle depicted in this section is to highlight the influence of localization of electron trapping on the $I_D(V_G)$ and $C(V_G)$ characteristic drifts. For the sake of consistency, the trapped electrons are simulated using a negative and fixed surface charge Q_{fixed} at the Al_2O_3/GaN interface, with a charge density N_{fixed} of $5 \cdot 10^{11} cm^{-2}$ such as $Q_{fixed} = q \cdot N_{fixed}$. The fixed surface charge Q_{fixed} has been placed either at the gate corners, at the gate bottom, or at the gate sidewalls as illustrated in Figure 4.12. A threshold voltage shift around 0.3V is expected according to the following expression, where $t_{Al_2O_3}$ and $\epsilon_{Al_2O_3}$ are the Al_2O_3 gate oxide thickness and relative dielectric permittivity respectively,

$$\Delta V_{TH} = q \cdot N_{fixed} \cdot \frac{t_{Al_2O_3}}{\epsilon_{00} \cdot \epsilon_{Al_2O_3}} \tag{4.2}$$

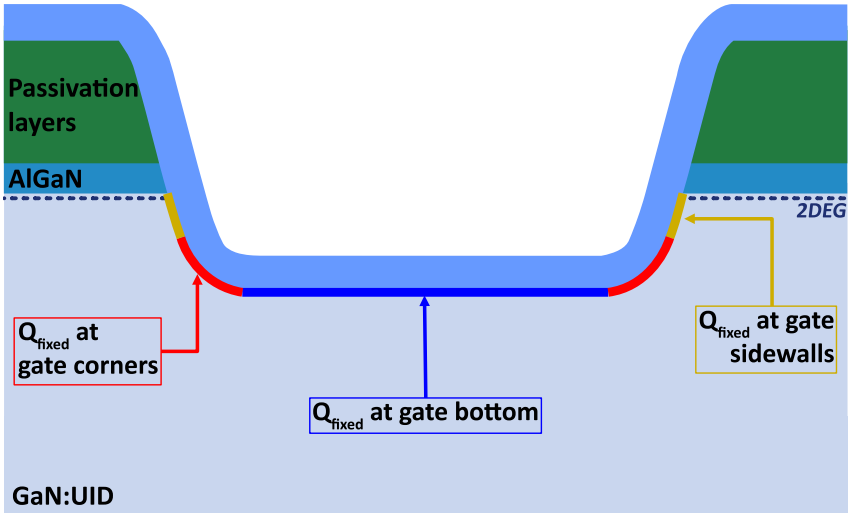

Figure 4.12. Illustration of TCAD simulation principle where trapped electrons within Al_2O_3 defects band are simulated using a fixed and negative surface charge Q_{fixed} along the Al_2O_3/GaN interface. Q_{fixed} has been placed at different gate regions (corner, bottom and sidewalls) in order to distinguish the charge position influence on $I_D(V_G)$ and $C(V_G)$ characteristics shifts.

4.1.4.2 TCAD simulation results

$I_D(V_G)$ and $C(V_G)$ characteristics calculated through TCAD simulations as a function of Q_{fixed} positions are depicted in Figure 4.13. At first sight, it can be observed that when Q_{fixed} is located at the gate sidewalls, the influence on both $I_D(V_G)$ and $C(V_G)$ characteristics is negligible compared to the reference characteristics, where no fixed surface charges at the Al_2O_3 gate oxide interface have been defined. However, a $C(V_G)$ shift can be noted when Q_{fixed} is defined at the gate bottom, while the $I_D(V_G)$ drift is negligible compared to the reference characteristics. Conversely, when the position of the fixed surface charge Q_{fixed} is at the gate corners, an $I_D(V_G)$ shift can be observed whereas it is negligible regarding the $C(V_G)$ characteristics. Consequently, the $I_D(V_G)$ instabilities are related to trapped carriers at the gate corners while the $C(V_G)$ shifts are associated with trapped electrons at the gate bottom. Such an effect is due to the presence of the back-barrier layer, which then induces that V_{THI} is controlled by the gate corners while V_{THC} is mainly driven by the gate bottom, as depicted in Figure 4.2. These observations are also consistent for different gate lengths as exhibited in Figure 4.14. It also shows that is possible to separate the charge trapping contribution of the gate bottom from the gate corners. It can be also observed that V_{THI} as well as V_{THC} increases as the gate length decreases, also called V_{TH} roll-up. As it will be extensively developed in the next section (4.2), this effect is also due to the back-barrier presence that influences the pBTI degradation.

4.1.4.3 Result interpretation

Considering that the gate oxide thickness is the same at the gate regions (bottom, corners, and sidewalls) and that V_{THC} is lower than V_{THI}, the overdrive voltage (which is proportional to

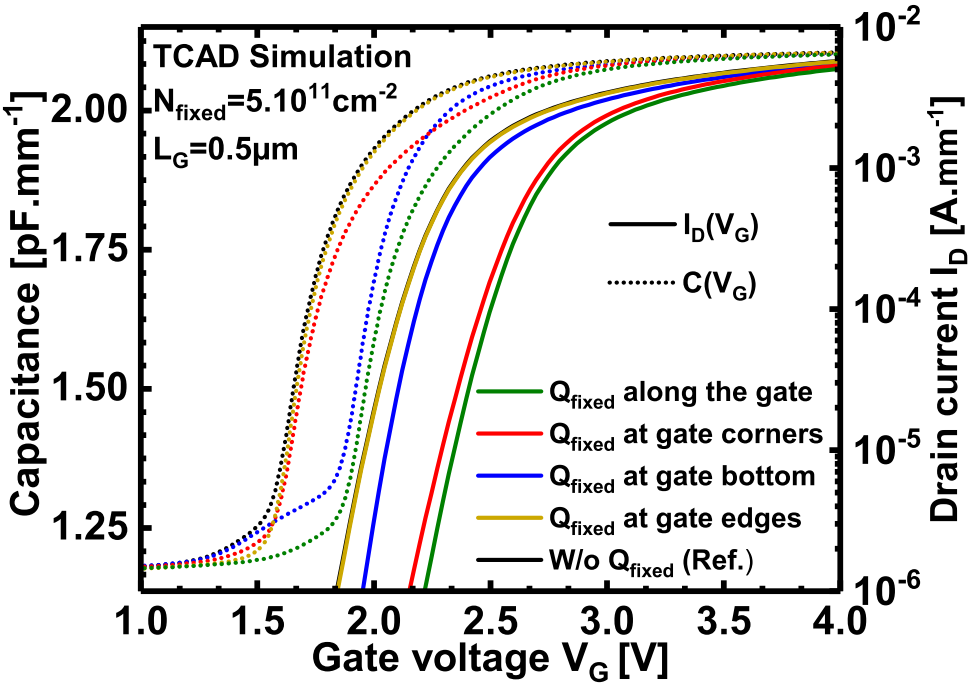

Figure 4.13. TCAD simulation results providing $I_D(V_G)$ and $C(V_G)$ characteristics obtained for different Q_{fixed} positions for a gate length of 0.5µm. A $C(V_G)$ shift can be observed while the $I_D(V_G)$ drift is negligible, when Q_{fixed} is at the gate bottom. Conversely, when Q_{fixed} is at the gate corners, an $I_D(V_G)$ shift can be noted while there is not any $C(V_G)$ drift. Consequently, the $I_D(V_G)$ shift is mostly related to fixed charges at the gate corners while the $C(V_G)$ drift is associated to trapped carriers at the gate bottom.

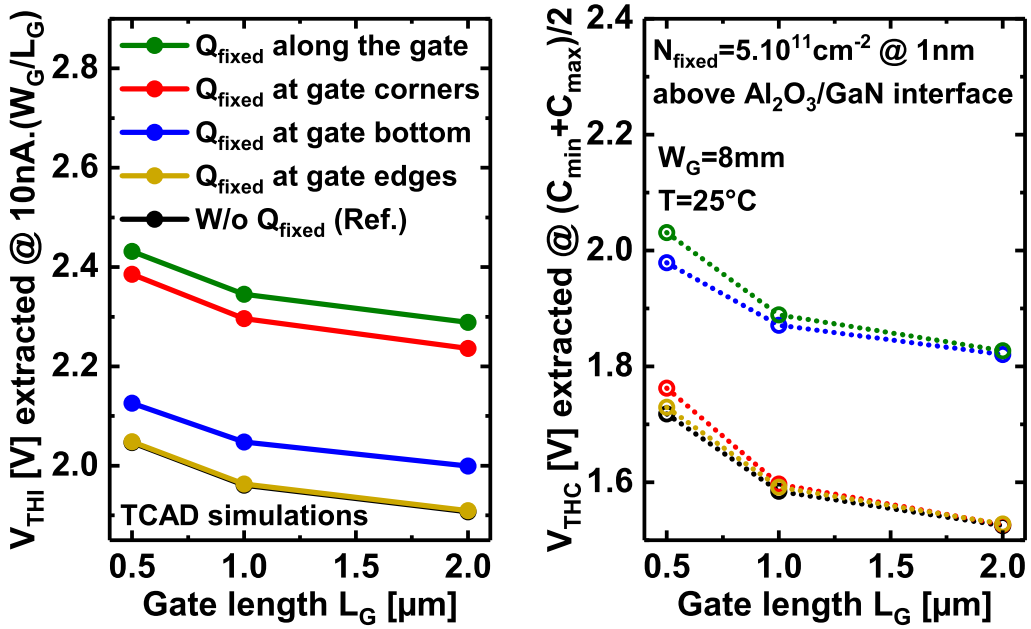

Figure 4.14. Influence of fixed surface charge position on V_{THI} (left) and V_{THC} (right) for different gate lengths simulated by TCAD. In the same way as experimental results, V_{THI} is extracted at $I_D = 10nA \cdot W_G/L_G$ while V_{THC} is extracted at $C = (C_{min} + C_{max})/2$. These results demonstrate that the observations presented in Figure 4.13 are also consistent for different gate lengths.

the gate electric field) during the gate stress should be lower at the gate corners than at the gate bottom when a fixed and positive gate voltage stress is applied such as,

$$|V_{GStress} - V_{THC}| > |V_{GStress} - V_{THI}| \tag{4.3}$$

Furthermore, we demonstrated that BTI degradation is induced by carrier injection into Al_2O_3 gate oxide defects. This underlying trapping mechanism strongly depends on the applied electric field within the gate oxide. Consequently, a higher pBTI degradation should be observed on ΔV_{THC} rather than on ΔV_{THI} for a fixed trap density of Al_2O_3 defects along the gate oxide, according to the simulations presented in Figures 4.13 and 4.14. This assumption is also consistent with the electric field distribution provided by TCAD simulations at a gate voltage of 5V, as depicted in 4.15.

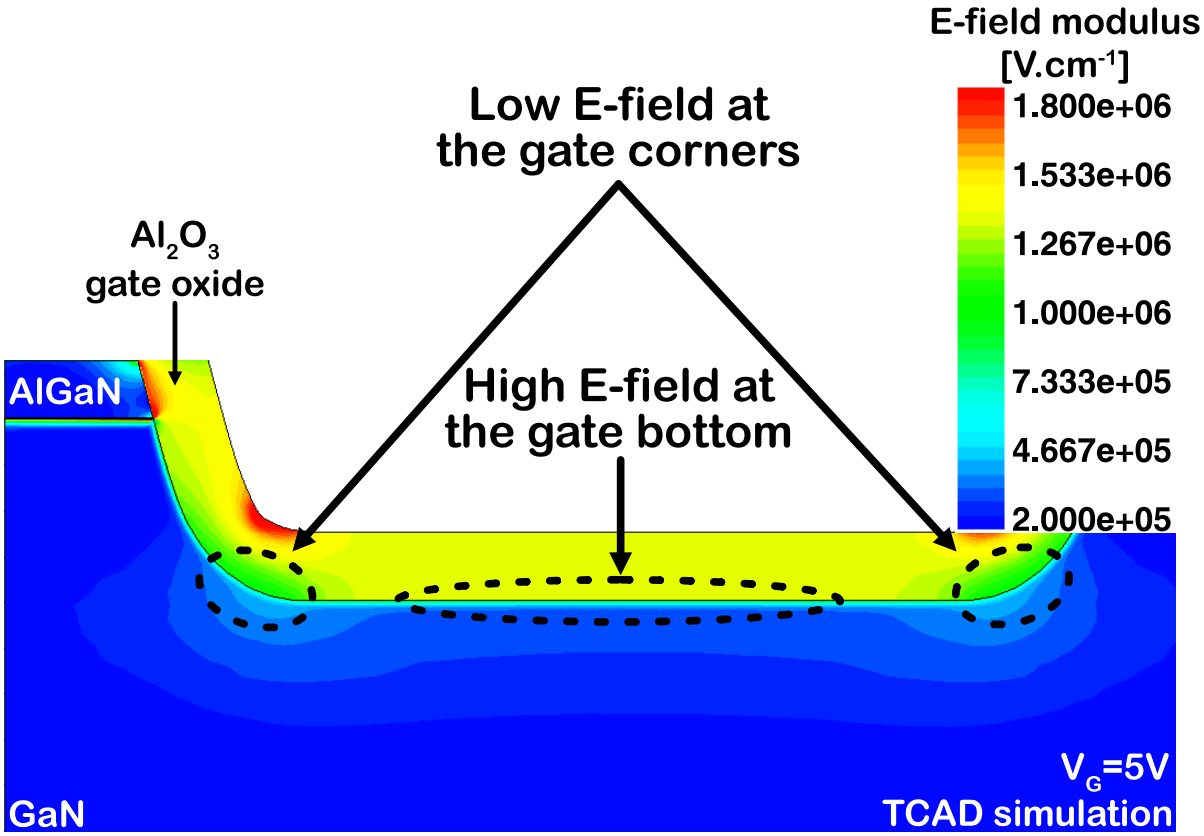

Figure 4.15. TCAD simulations depicting the electric field distribution around the gate region at a gate voltage of 5V and a gate length of 0.5µm. It can be observed that the electric field is higher at the gate bottom than at the gate corners, along the Al_2O_3 gate oxide interface. As a result, the pBTI degradation is expected to be higher at the gate bottom than at the gate corners, which should exhibit a higher ΔV_{THC} than ΔV_{THI} for a fixed trap density of Al_2O_3 defects along the gate oxide.

Indeed, a lower electric field at the gate corners compared to the gate bottom along the gate oxide interface can be noticed. Therefore, the pBTI degradation should be superior at the gate bottom than at the gate corners. It should result in a ΔV_{THC} higher to ΔV_{THI} for a fixed trap density of Al_2O_3 defects along the gate oxide interface. However, the experimental pBTI transients exhibited in Figures 4.6, 4.7 and 4.11 depict that $I_D(V_G)$ shifts are higher than $C(V_G)$ drifts. The only explanation for this behavior difference between the TCAD simulations and the

experimental results is to conclude that the trap density is more important at the gate corners than at the gate bottom, as illustrated in Figure 4.16.

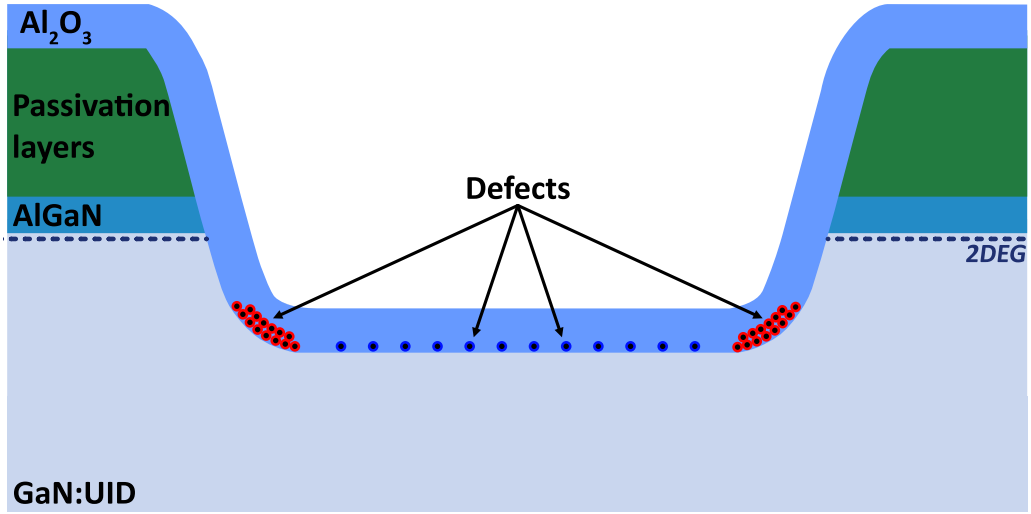

Figure 4.16. Illustrations showing a higher trap density at gate corners compared to the gate bottom, leading to a ΔV_{THI} higher than ΔV_{THC}.

4.2 Gate length influence on pBTI degradation

In this part, the influence of the gate length L_G on the pBTI degradation is investigated. Indeed, it has been observed that the pBTI degradation decreases when the gate length decreases under constant $V_{GStress}$. It is due to an increase of the initial threshold voltage with L_G reduction (V_{TH} roll-up). Studying the gate voltage acceleration factors, we pointed out that this behavior is essentially due to an electric field modification within the gate oxide layer. Indeed, the overdrive voltage expressed by $|V_{GStress} - V_{TH}|$, and proportional to the gate oxide electric field, tends to decrease as V_{TH} increases with L_G reduction. It thus leads to a pBTI shift reduction when shortening the gate length. Specific variation of V_{TH} as a function of L_G was also reproduced by the TCAD simulations, indicating that shortening the gate length can improve the device performance in terms of PBI degradation. These simulations showed that this V_{TH} roll-up behavior is induced by the back-barrier presence in the epitaxial structure. All these results will be extensively described in this section.

4.2.1 Device specification and experimental setup

4.2.1.1 Device description

The tested transistors are close to the one described in the previous chapters. Epitaxial growth has been performed by MOCVD on 8" p-type Si substrates. A transition layer followed by a carbon-doped GaN (GaN:C) layer is used within the epitaxial structure, both with a thickness above 1µm. Subsequently, a back-barrier layer used to tune the V_{TH} is grown, followed by an unintentionally doped GaN layer (GaN:UID) used to form the channel. An AlGaN barrier is then grown to create the 2DEG (2-D Electron Gas) at the interface with the GaN. Then, a 10nm in-situ SiN is deposited to passivate the AlGaN surface. Thereafter, ICP RIE etching has been carried out to remove the AlGaN barrier in order to reach a fixed recess depth R_D from the AlGaN surface. A 30nm Al_2O_3 gate oxide is deposited on the recessed well as a gate insulator. In this section, the gate profile is described by the recess depth R_D, the etch angle Θ_R, and the curvature radius m of the gate corner. The latter parameters are described in the fully recessed gate representation provided in Figure 4.17. Finally, all tested transistors have a width of 200µm while both L_{GD} and L_{GS} distances are fixed.

4.2.1.2 Experimental setup

Contrary to the experimental setup presented in previous study (section 4.1), only $I_D(V_G)$ drift under positive gate voltage stress is monitored in this study. The experimental setup can be compared to the one used in section 2.3. An illustration of the Measurement-Stress-Measurement (MSM) pBTI technique under DC stress is illustrated in Figure 4.18. Experimental pBTI measurements can be separated in two phases which are the stress and the recovery phases. The stress phase is dedicated to observe the charge trapping dynamics by applying a positive $V_{GStress}$, and is immediately followed by the recovery phase where the gate voltage stress is set to 0V in order to observe the electron detrapping dynamics. In this study, the stress phase is generally 10s long, while the recovery is 10^2s long. All fast $I_D(V_G)$ characteristics (< 10 µs) are performed periodically during both phases using a Keysight B1500 with ultra-fast WGFMU (B1530). $I_D(V_G)$ records need to be as fast as possible to avoid a recovery during the measurement. Note that V_{DS} is grounded during the stress while is is fixed at 100mV during fast

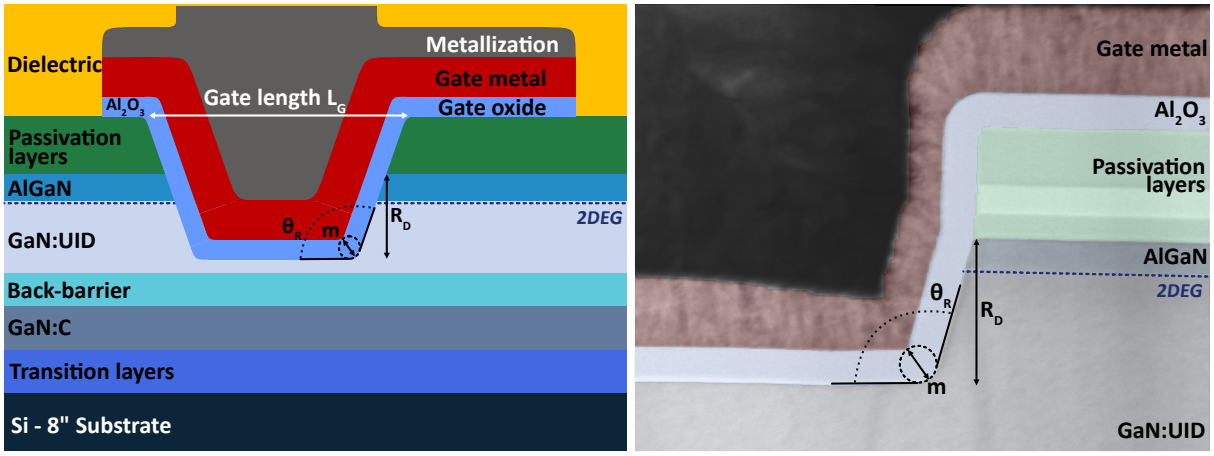

Figure 4.17. Both pictures describe the recess depth R_D, etching angle Θ_R and curvature radius m of the gate corner. **Left -** Representation of the tested GaN-on-Si E-mode MOSc-HEMT. **Right -** TEM cross section of the gate right side.

$I_D(V_G)$ measurements. V_{TH} extraction from fast $I_D(V_G)$ measurements is extracted at constant drain current of $I_D = I_0 \cdot (W_G/L_G)$ where $I_0 = 10$ nA.

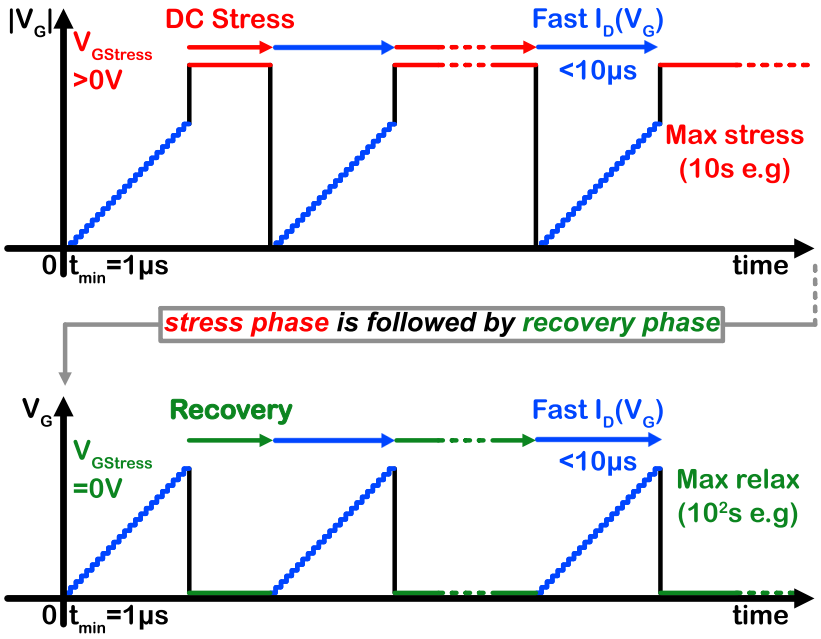

Figure 4.18. Representation of pBTI measurement principle where ultra-fast $I_D(V_G)$ records (< 10 µs) during the stress (top) and recovery (bottom) phases in order to minimize the unwanted recovery. The recovery phase ($V_{GStress} = 0$ V) starts immediately at the end of stress phase ($V_{GStress} > 0$ V).

4.2.2 Gate length influence on experimental pBTI transient

Threshold distributions of pristine devices extracted at room temperature for three different gate lengths, from 0.5µm to 2µm, are presented in Figure 4.19-left. First of all, it can be noticed

that these distributions follow a normal law with a V_{TH} average above 0.5V for the three gate lengths. Moreover, it is also interesting to note that V_{TH} is dependent on the gate length, such as it increases as L_G decreases. Such a behavior of threshold voltage as a function of L_G is well known in CMOS technologies, and is commonly called "V_{TH} roll-up". Threshold voltage extracted after a gate voltage stress of 7V during 10s at room temperature are depicted in Figure 4.19-right. V_{TH} distributions follow a normal distribution, which is consistent with a large gate area. Indeed, in CMOS technology, the gate area is too small to have many defects, which implies that the ΔV_{TH} distribution after a gate stress does not follow a normal distribution [298]. Furthermore, it is worth noticing that the distributions are inverted compared to those presented in Figure 4.19-left, indicating that the pBTI shift increases as the gate length rises.

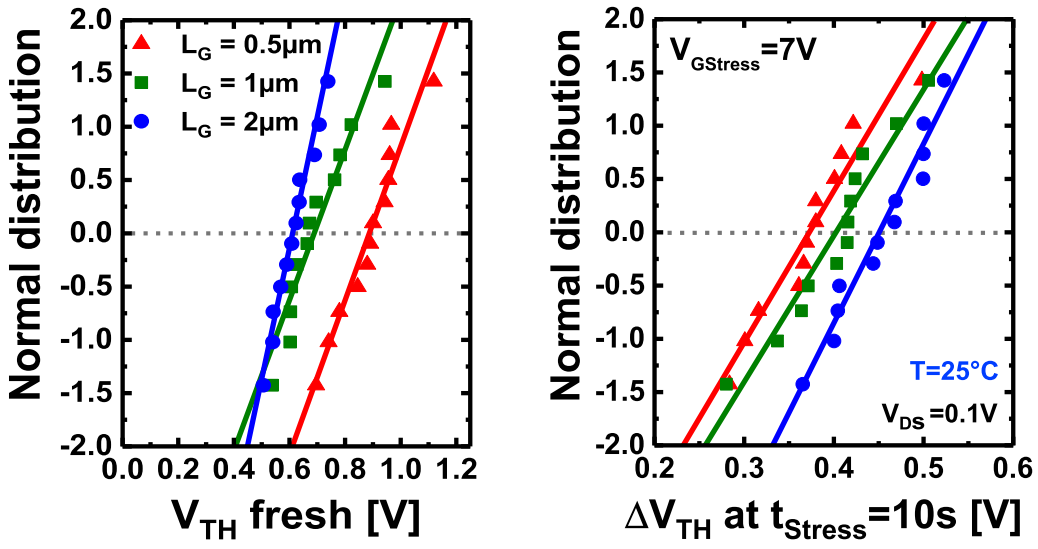

Figure 4.19. Left - Initial V_{TH} distribution extracted at a constant current, $I_D = I_0 \cdot (W_G/L_G)$ where $I_0 = 10 \cdot 10^{-9}$ A. Experimental data are fitted with normal law (lines) demonstrating a positive V_{TH} (N-Off behavior) for the three gate lengths at 25°C. **Right -** ΔV_{TH} distributions extracted after at $t_{Stress} = 10$ s under $V_{GStress} = 7$ V for the three L_G at room temperature. Experimental data is fitted with normal law (lines) which is consistent with large gate area. The pBTI shift increases as the gate length rises.

Median curves of pBTI stress and recovery transients for the three different gate lengths are presented in Figure 4.20. During the stress phase, a gate voltage stress of 7V was applied for 10s at room temperature just before the recovery phase which lasted 100s. These results are comparable to those observed in chapter 2, where a strong acceleration of pBTI degradation after $1-10$s has been observed. This acceleration is most likely a signature of the C_N traps within the GaN:C layer, which is combined with the V_{TH} instabilities induced by the electron injection into the Al_2O_3 defect band. As mentioned in the previous section, the carriers trapping in the gate oxide defects is predominant at such high gate stress voltage ($V_{GStress} = 7$ V) and screens the ΔV_{TH} variation induced by C_N sites. However, during the recovery phase, it can be observed that there is a strong ΔV_{TH} variation at around 1s which is due to C_N trap deionization. Although the stress transients show a similar shape for all L_G during the stress and recovery phases, we can notice an influence of gate lengths on the pBTI degradation. Indeed, a ΔV_{TH} increase can be noted as the gate length increases.

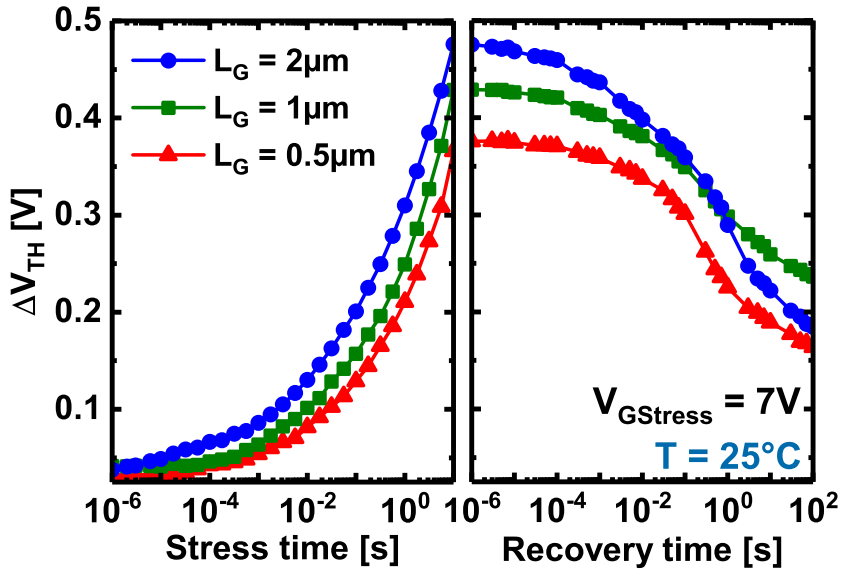

Figure 4.20. Stress and recovery pBTI transients as a function of the gate length L_G. These results have been obtained under a $V_{GStress}$ of 7V at room temperature. Similar dynamics are observed during stress and recovery phases. However, a slight increase of ΔV_{TH} shift can be noticed when L_G increases.

Same stress and recovery pBTI transients obtained at 150°C are depicted in Figure 4.21, where a stronger degradation is visible at the end of the stress phase. Similar dynamics are observed during stress and recovery phases for all gate lengths. The degradation acceleration occurs at a shorter time ($\sim$ 10 ms) than at room temperature, due to the increase of charge trapping rate with temperature. It is also interesting to note that the pBTI reduction dynamics increase as the gate length increases at 150°C, which is not observed at room temperature.

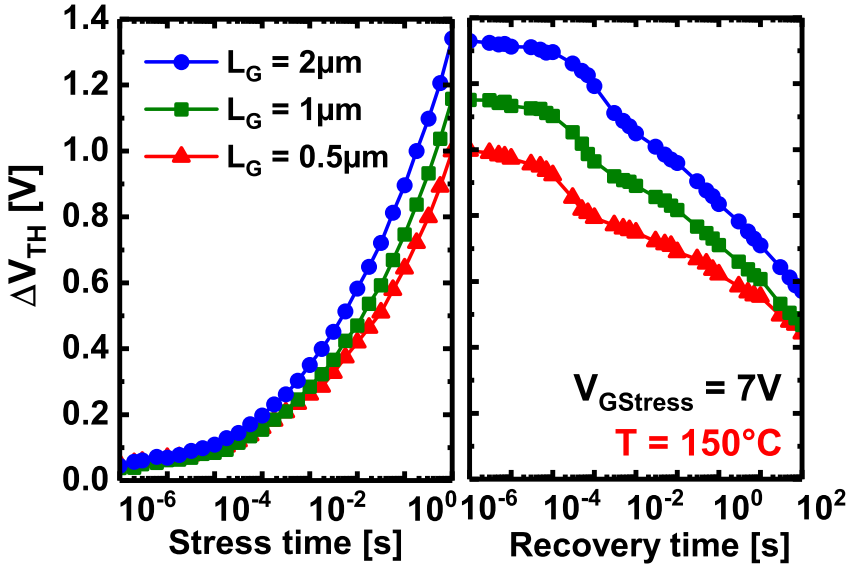

Figure 4.21. Stress and recovery pBTI transients as a function of the gate length L_G. These results have been obtained under a $V_{GStress}$ of 7V at 150°C. Comparing with the results at 25°C, a strong amplification of ΔV_{TH} shift as L_G increases can be observed.

Analyzing the recovery transients at 25°C and 150°C presented in Figures 4.20 and 4.21, it is possible to extract the time constants related to the strong ΔV_{TH} variation observed on the relaxation transients. To do so, we fitted the experimental relaxation transients with a moderate order polynomial function which have been derived, such as $(\partial \Delta V_{TH})/(\partial \log(t_{relax}))$. Figure 4.22 displays an example of these derivative fitted curves for each gate length at room temperature (Figure 4.22-left) and 150°C (Figure 4.22-right). It is interesting to note that the peak positions, corresponding to the time constant related to the sharp pBTI decrease, all have the same order of magnitude independently of the gate length. Moreover, it also depicts that there is a strong temperature activation of this time constant. Indeed, at 150°C it is located around $5 \cdot 10^{-4}$s while it is around 5s at 25°C. This strong temperature activation as well as the values associated with these time constants indicate that they are most certainly related to the C_N trap deionization located in the GaN:C, as demonstrated in previous section. Consequently, these results demonstrate that the population of traps involved in pBTI degradation are rather equivalent for all gate lengths.

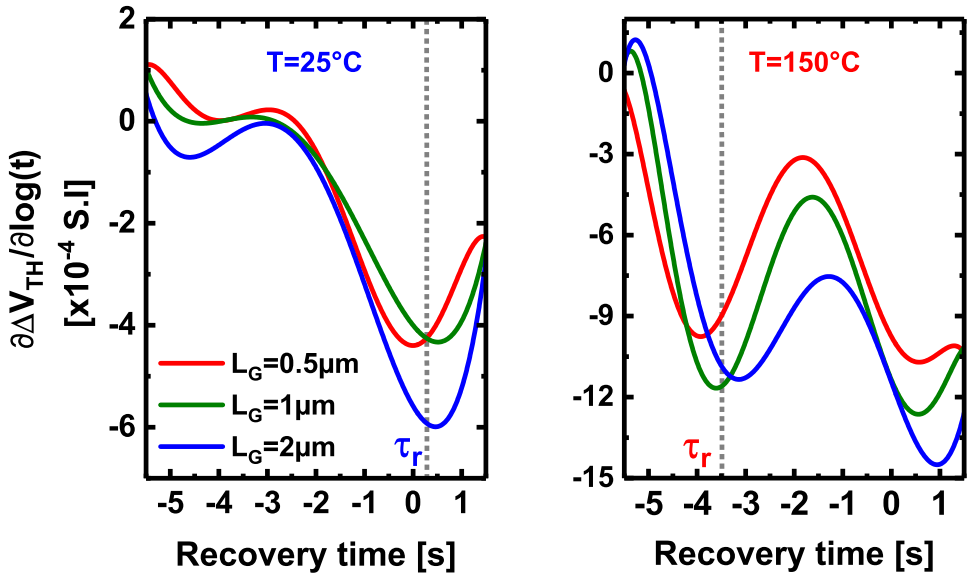

Figure 4.22. Derivatives curves of polynomial equation fitted to pBTI shift transients. These curves enable to extract a recovery time constant τ_r related to strong pBTI decrease, and corresponds to the pic positions. **Left -** Derivatives curves related to the pBTI transients obtained at 25°C **Right** Results obtained at 150°C.

The correlation between the threshold voltage of pristine devices and the pBTI shift obtained after 10s of stress at $V_{GStress} = 7$ V is presented in Figure 4.23 for temperature of 25 and 150°C. It can be noticed that a trend appears between pBTI shift with the variation of the fresh V_{TH} value as a function of L_G. Indeed, the lower the fresh V_{TH}, the higher the pBTI shift. This trend can be explained by an overdrive gate voltage ($V_{OV} = V_{GStress} - V_{TH}$) reduction as the gate length decrease, due to the higher initial V_{TH}. Therefore, a smaller pBTI is induced at a given $V_{GStress}$ since the electric field within the Al_2O_3 gate oxide is proportional to the overdrive voltage. At 150°C, the pBTI variation with L_G is higher after 10s since the electron trapping rate is higher. A difference of 40% in pBTI between 0.5µm and 2µm gate lengths can be noticed at high temperature. Hence, the use of a short gate length can guarantee a higher initial V_{TH}, as well as a reduced pBTI under real device operation.

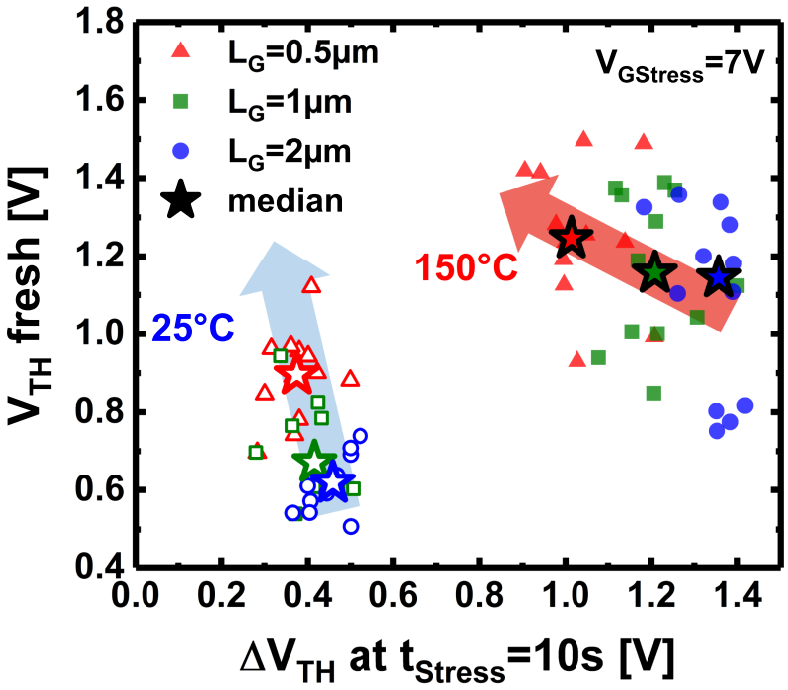

Figure 4.23. Initial V_{TH} versus pBTI shift at $t_{Stress} = 10$ s for T = 25 °C and 150 °C.

4.2.3 TCAD simulations

4.2.3.1 Gate topology influence on the electric field distribution within the gate oxide

To further understand the influence of electric fields within the gate oxide on parameters such as initial V_{TH} and pBTI degradation, TCAD simulations were performed. Figure 4.24 shows the electric field distribution in the Al_2O_3 gate oxide at a gate voltage of 7V.

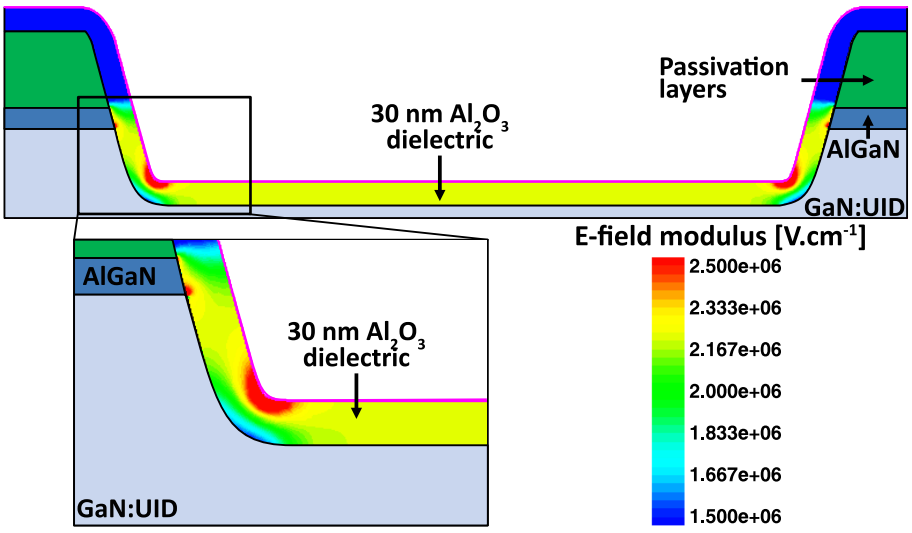

Figure 4.24. TCAD simulation of electric field modulus distribution in the gate dielectric at $V_G = 7$ V on 30nm Al_2O_3 gate oxide including the first gate field plate. A non-uniform distribution of the electric field modulus at the gate corners can be noticed. Conversely, the electric field distribution at the gate bottom is uniform. The gate length is 1µm here.

It reveals a non-uniform distribution of the electric field modulus at the gate corners, in contrast to the gate bottom where the electric field distribution is uniform. This peculiar electric field distribution is due to the two-dimensional architecture of the gate. In the previous section, we demonstrated that the pBTI degradation is more important at the gate corners than at the gate bottom. These discrepancies in electric field distribution between the gate corners and the gate bottom induce different local pBTI degradation in these regions. It is therefore important to understand how the electric field is distributed in the gate oxide as a function of the gate geometry parameters, in order to better explain the pBTI drift behavior.

The influence of the curvature radius m can affect significantly the initial V_{TH} as well as the electric field distribution on the gate corners. Figure 4.25 shows the electric field distribution in the gate corner dielectric for different curvature radius ranging from m = 0.02 to 0.09 A.U. It can be observed that the electric field tends to decrease at the Al_2O_3/GaN interface as the curvature radius decreases. If the gate corner is sufficiently smoothed, the electric field should be uniform and match with the value of the gate bottom. It is also important to note that these electric field distributions are valid at a fixed gate recces angle Θ_r and fixed recess depth R_D, and can be also influenced by the latter parameters. Since the electric field distribution is modified by the gate topology, the latter is particularly likely to influence the pBTI under a fixed $V_{GStress}$. Note that the gate topology significantly depends on the different process steps such as the etch technique used, the post etching cleaning as well as the dielectric deposition uniformity. Consequently, these aspects can influence the pBTI degradation.

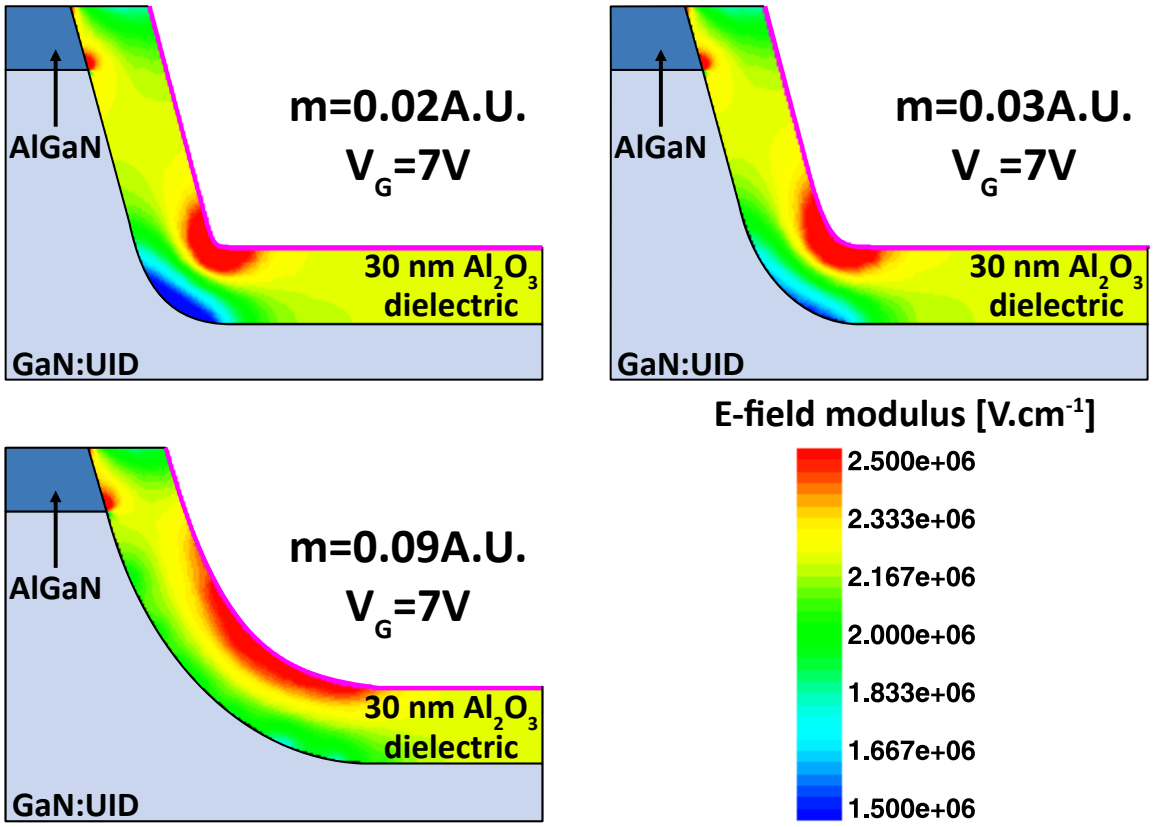

Figure 4.25. Electric-field distribution simulated by TCAD at $V_G = 7$ V as a function of the radius curvatures, from m = 0.02 to 0.09 A.U. It can be noticed that the electric field tends to decrease at the Al_2O_3/GaN interface as the curvature radius decreases.

Beyond influencing the electric field distribution within the Al_2O_3 gate oxide, the curvature radius also tends to modify the initial V_{TH}. Indeed, Figure 4.26 illustrates this effect where the variation of the initial V_{TH} has been plotted as a function of the drain voltage V_D. Although the curvature radius influence on V_{TH} decreases as the drain voltage increases, it is shown that its effect remains significant. It also exhibits that the smaller the radius of curvature, the higher the V_{TH} variation with the drain voltage.

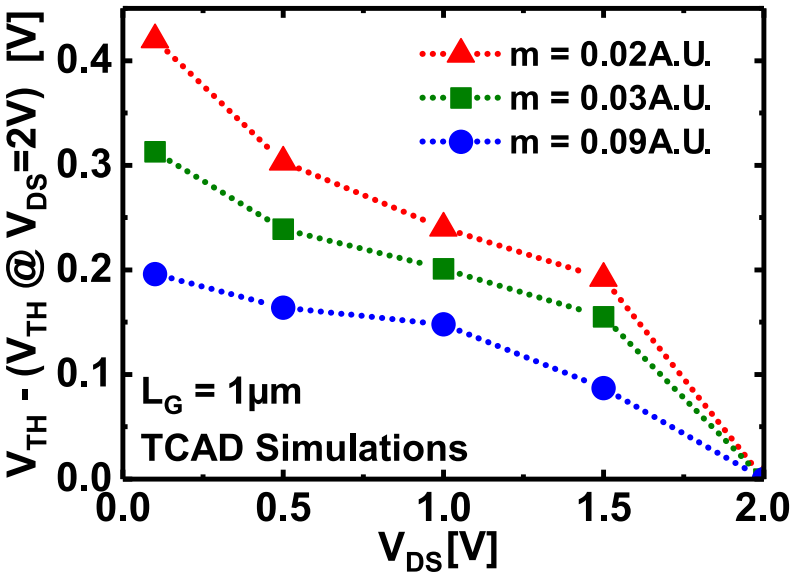

Figure 4.26. TCAD simulation where the variation of the initial V_{TH} is plotted versus V_D.

4.2.3.2 Epitaxial structure influence on V_{TH} behavior with gate length

In CMOS technologies, the decrease of the gate length induces the well-known Short Channel Effect (SCE). It leads to a series of issues, including gate depletion, Drain-Induced Barrier Lowering (DIBL), carriers velocity saturation, increased reverse leakage current, reduced mobility, Hot Carrier Injection effects and other similar drawbacks. Among these, the gate length influence on the threshold voltage reduction must also be noted, which is also called V_{TH} roll-off. Source and drain PN junctions contribute to depletion charges in the channel region. The depletion charge in the channel region is then balanced by the charges in the source and drain regions rather than by the charges on the gate. Therefore, a lower gate charge is required to achieve inversion, i.e. V_{TH} decreases as L_G is reduced. Since the source and drain regions in HEMTs are spatially distant from the gate region, the V_{TH} roll-off should not occur. However, Figure 4.27 shows an experimental V_{TH} roll-up at $V_{DS} = 100$ mV.

In order to improve our understanding of the threshold voltage dependence with the gate length, TCAD simulations have been carried out. Figure 4.28 presents the conduction band energy E_C distribution under the gate without any polarization. These results enable to better understand how the threshold voltage is defined. Indeed, the conduction band energy value along the gate interface gives a direct image of the local V_{TH} value. As observed in the previous section (Figure 4.2), this distribution reveals that the local E_C value is higher at the gate corners than at the gate bottom. Since the conduction band energy at the gate corners act as the highest potential barrier along the channel for electrons moving toward the drain, the threshold voltage

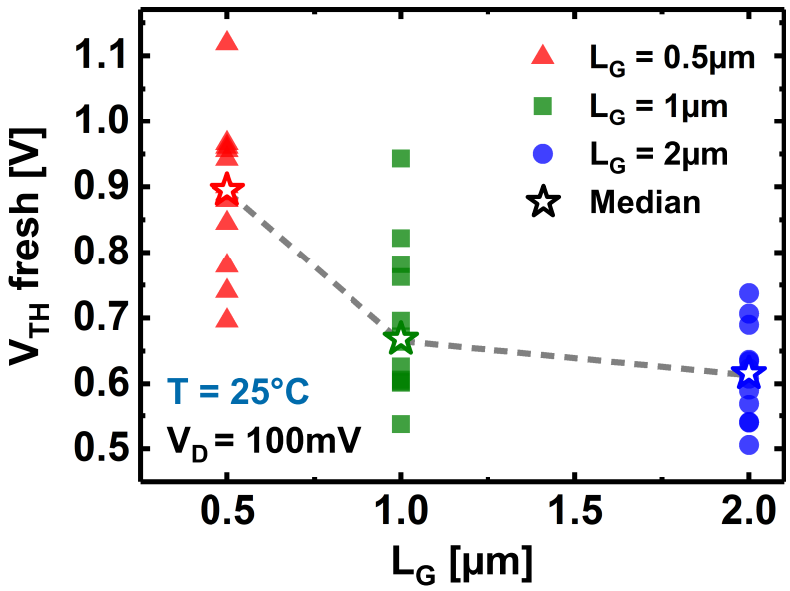

Figure 4.27. Experimental V_{TH} roll-up at $V_D = 0.1$ V. V_{TH} fresh values come from Figure 4.19-left.

of $I_D(V_G)$ characteristic is thus controlled by the gate corners. This effect is due to the presence of the back-barrier layer leading to the stretching of the electric field iso-lines under the gate and thus to a local increase of conduction band energy at the gate corners.

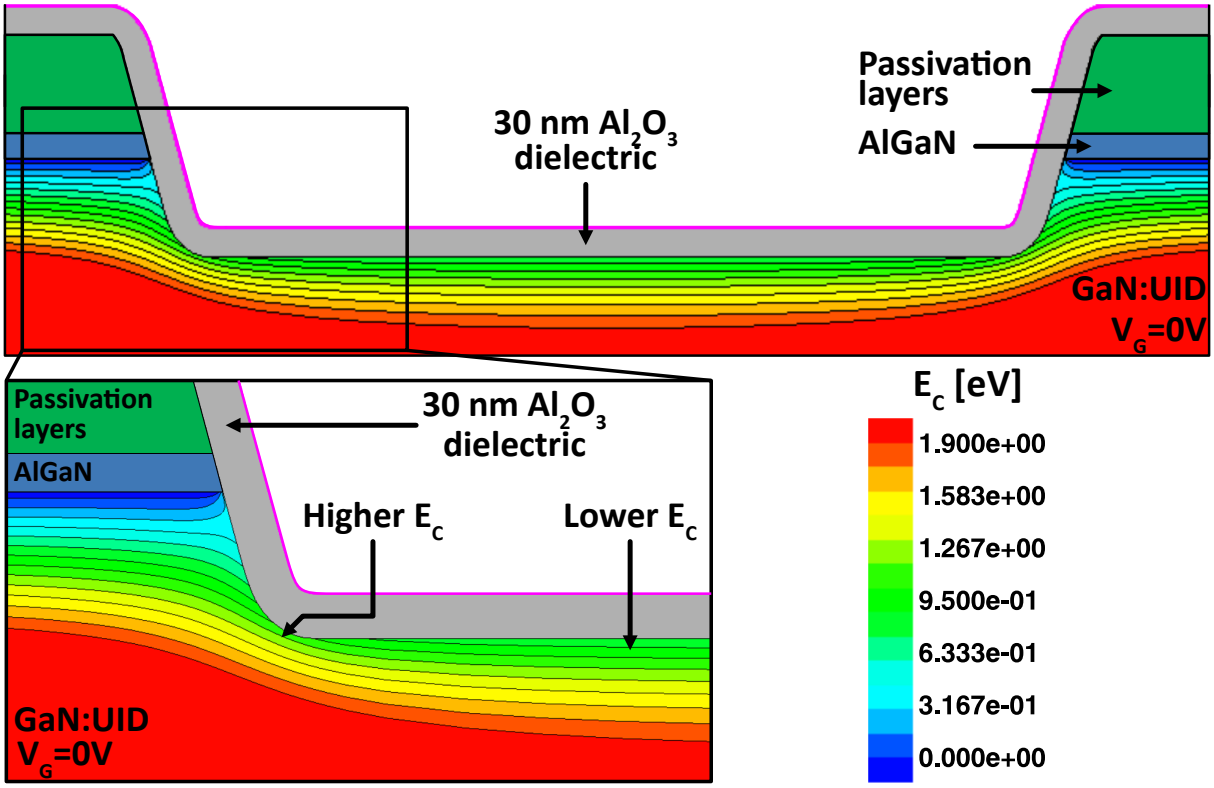

Figure 4.28. Conduction band energy distribution just below the gate without any polarization when a back-barrier is embedded. It can be noticed that E_C is higher at the gate corners than at the gate bottom. The gate length is 1µm while the curvature radius is 0.03A.U.

Influence of the gate length on the conduction band energy at gate oxide interface is depicted in Figure 4.29. It shows the variation of the GaN conduction band profile along Al_2O_3/GaN interface as a function of the gate length from 0.25µm to 2µm. It can be observed that the conduction band increases as the gate length decreases. This behavior occurs at the gate corners as well as at the gate bottom. This conduction band behavior with the gate length automatically leads to V_{TH} reduction when the gate length decreases, as shown in Figure 4.30.

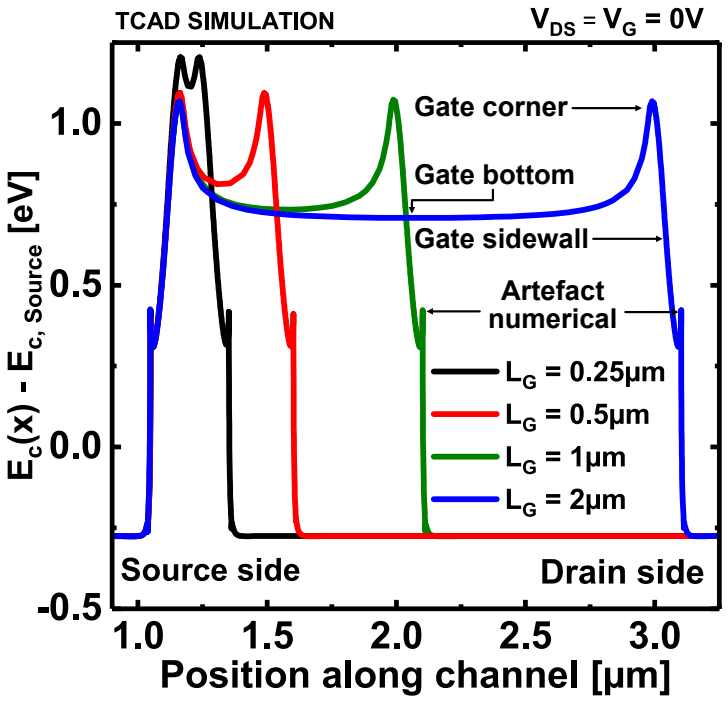

Figure 4.29. GaN conduction band profile along Al_2O_3/GaN interface as a function of the gate length from 0.25µm to 2µm. It can be noticed that the conduction band increases as the gate length decreases.

4.2.3.3 V_{TH} behavior without back-barrier

As previously pointed out, this peculiar variation in $V_{TH}(L_G)$ shows that shortening the gate length improves the device performances by reducing pBTI degradation. However, it is very important to note that this only occurs if a back-barrier is present into the epitaxial structure. Indeed, it leads to a confinement of the electric field iso-lines at the gate corners and then implies an increase of the conduction band in the same gate region. If there is no back-barrier, this behavior should not appear and the maximum value of the conduction band energy would be located at gate bottom according to the TCAD simulations. Consequently, the threshold voltage would be controlled by the gate bottom. Figure 4.31 shows the GaN conduction band energy distribution around the gate region with a gate voltage of $-1V$. It can be noticed E_C is higher at the gate bottom than at the gate corners, due to the absence of back-barrier. Note that, when a back-barrier is not integrated, the device has a Normally-On behavior at a gate voltage of 0V. This is the reason why a slight polarization is applied.

Figure 4.32 illustrates the gate length influence on the conduction band energy at gate oxide interface when the back-barrier is not integrated. It shows the variation of the GaN conduction

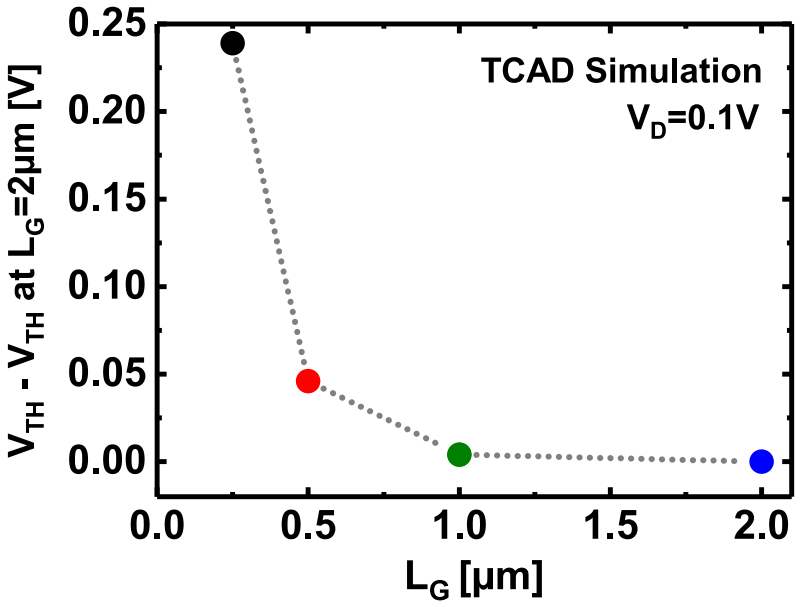

Figure 4.30. TCAD simulation showing the threshold voltage variation as a function to the gate length at $V_D = 0.1$ V. It depicts that the V_{TH} roll-up behavior, experimentally observed in Figure 4.27, can be reproduced by integrating a back-barrier layer in the simulations.

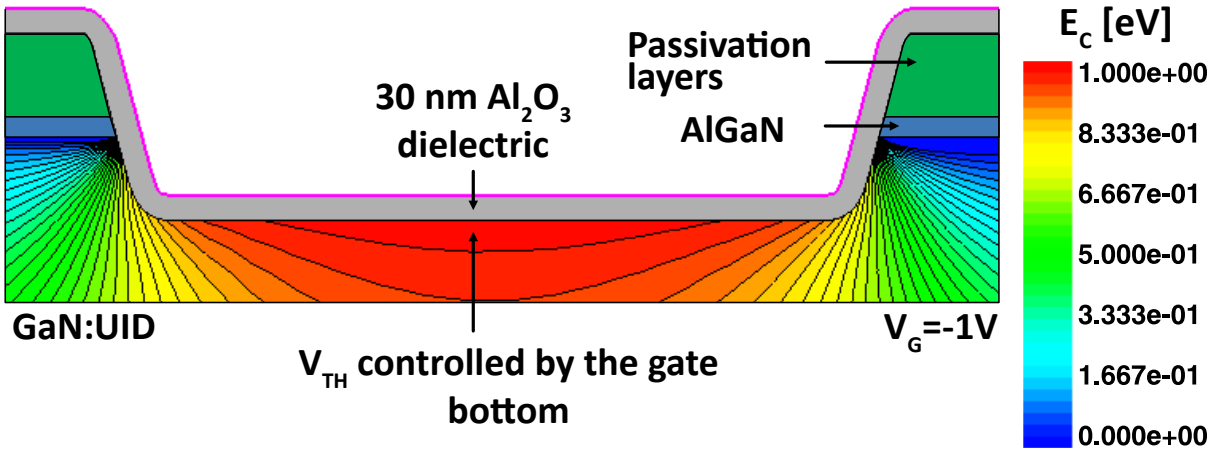

Figure 4.31. Conduction band energy distribution around the gate region with a slight polarization of $V_G = -1$ V. If the gate voltage is set to 0V, the device is naturally at the On-state when a back-barrier is not integrated. This polarization is applied to highlight the fact that the E_C is higher at the gate bottom than at the gate corners, due to the absence of back-barrier. It shows that the threshold voltage is controlled by the gate bottom. The gate length is 1µm while the curvature radius is 0.03A.U. here.

band profile along Al_2O_3/GaN interface as a function of the gate length from 0.25µm to 2µm. It can be observed that the conduction band decreases as the gate length decreases. This behavior occurs at the gate bottom as well as at the gate corners.

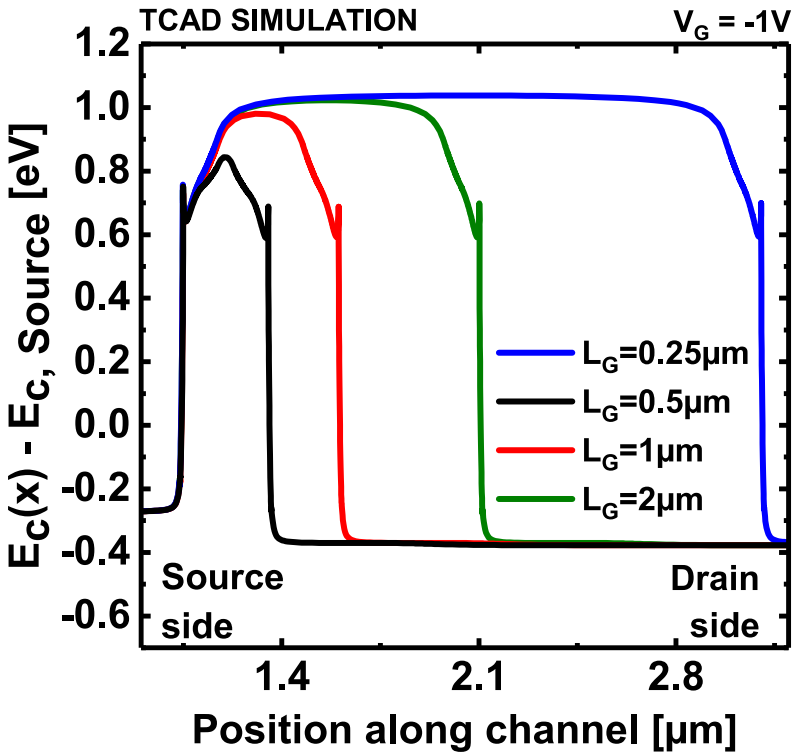

Figure 4.32. GaN conduction band profile along Al_2O_3/GaN interface as a function of the gate length from 0.25µm to 2µm when the back-barrier is not integrated. It can be noticed that the conduction band decreases as the gate length decreases.

Such a conduction band behavior with the gate length automatically leads to V_{TH} reduction when the gate length decreases, as exhibited in Figure 4.33. In the configuration where there is no back-barrier, the pBTI reduction with gate length reduction is not valid because the overdrive voltage will increase as well as the pBTI degradation. Indeed, the difference between V_{TH} and $V_{GStress}$ should increase as the gate length decreases, leading to a higher electric field with the gate oxide, and then a higher electron trapping rate.

4.2.4 Acceleration factor as a function of gate length

4.2.4.1 Arrhenius analysis

PBTI acceleration factors have been evaluated in order to provide a better understanding of the V_{TH} drift phenomena. The activation energy (E_a) related to pBTI shift obtained after 10s of gate voltage stress at 7V has been extracted in a first time. A statistical approach was used to carry out a reliable E_a extraction, at five different temperatures from 50°C to 150°C. It can be observed in Figure 4.34 that similar apparent activation energy values have been found for the different gate dimensions, which is around 130meV. Although this value is much too low and does not represent the physical activation energies of the capture and emission trapping processes [137], [142], the pBTI degradation follows the same temperature dependence

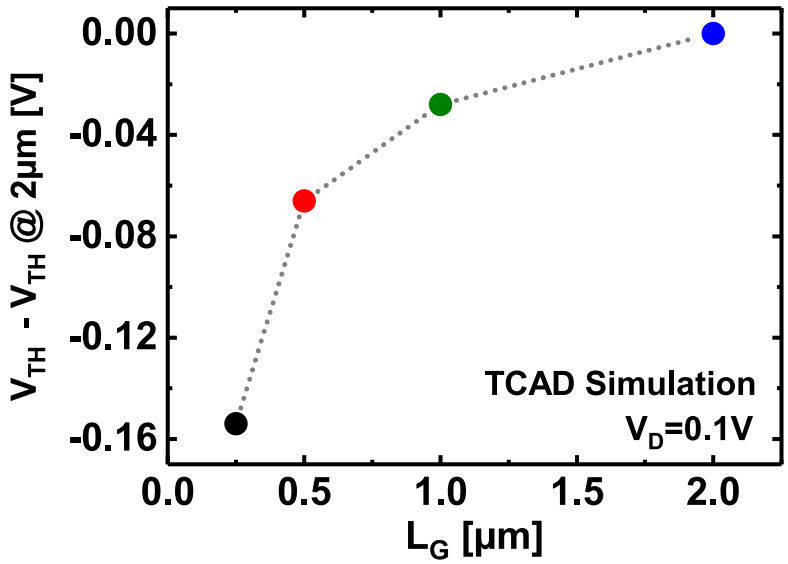

Figure 4.33. TCAD simulation presenting the threshold voltage variation as a function of the gate length at $V_D = 0.1$ V. It shows a V_{TH} roll-off when the back-barrier layer is removed.

independently of the gate length. Consequently, it indicates that the same underlying physical mechanism occurs for all three gate lengths.

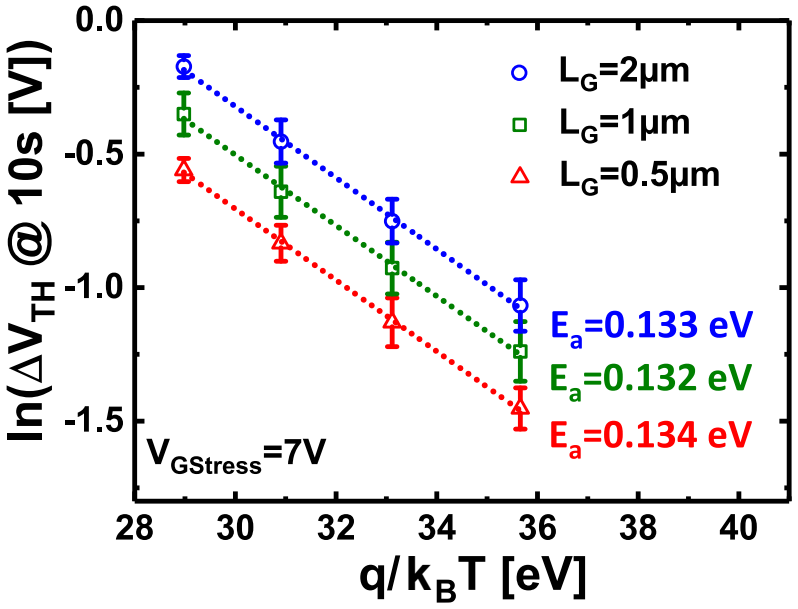

Figure 4.34. Arrhenius plot of the pBTI degradation after 10s of gate voltage stress at 7V. The same activation energy $E_a \approx 130$ meV is extracted for the three gate lengths. Since the temperature dependency is exactly observed for all three gate lengths, it thus indicates that the same underlying physical mechanism occur independently on L_G.

4.2.4.2 Extraction of the gate voltage acceleration factors

The gate voltage acceleration factor α has been also extracted for the three different gate lengths. It has been evaluated at room temperature under different gate stress voltage conditions from

5V to 9V using the following equation,

$$\Delta V_{TH} = C_R \cdot V_{GStress}^{\alpha} \cdot \exp\left(\frac{q \cdot E_a}{k_B \cdot T}\right) \cdot \ln\left(1 + \frac{\tau_c \cdot t_S}{\tau_e \cdot t_R}\right) \quad (4.4)$$

Where C_R is a constant,
τ_c and τ_e are the capture and emission average time constants of the oxide trap respectively, and t_S and t_R the stress and relaxation times used in the measurement, respectively.

It is interesting to note that the longer the gate length, the more important the α factor, increasing from 4.6 for $L_G = 0.5$ µm to 5.3 for 2µm, as depicted in Figure 4.35.

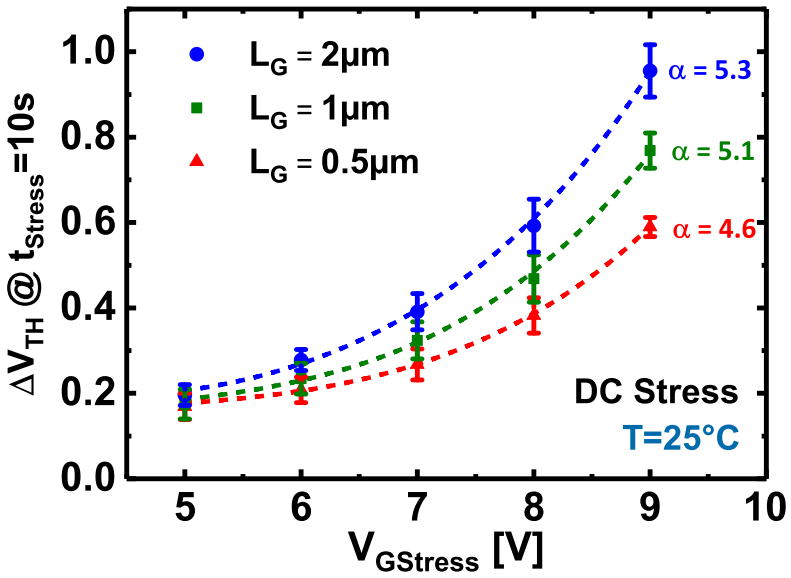

Figure 4.35. ΔV_{TH} drift after 10s of stress as function of $V_{GStress}$ at 25°C for the three different gate lengths. It can be observed that the gate voltage acceleration factor depends on the gate length, due to the overdrive voltage modification induced by the V_{TH} roll-up. The electron trapping in Al_2O_3 gate oxide defects is thus enhanced for longer gate lengths.

Such an effect confirms that pBTI shift depends on the applied electric field within Al_2O_3 gate oxide layer that is proportional to the overdrive voltage. Since the $V_{GStress}$ is fixed, the overdrive gate voltage during stress only depends on the initial V_{TH} that varies with the gate length. Indeed, the threshold voltage decreases as the gate length increases, leading to a V_{OV} increase for $L_G = 2$ µm. As the electric field is higher in the gate oxide where $L_G = 2$ µm compared to $L_G = 0.5$ µm, the electron trapping in the Al_2O_3 gate oxide defects is worst for longer gate lengths. Consequently, it results in a higher extracted α for longer L_G.

4.2.4.3 Time-to-Failure

As mentioned before, the modification of the gate length influences the charge trapping in the gate oxide and tends to decrease the pBTI for short gate length. Indeed, the V_{TH} roll-up implies a V_{OV} reduction with the L_G decrease and thus a decrease of the electric field in the gate dielectrics. This V_{OV} effect automatically reduces the pBTI degradation which automatically influences the transistor lifetime. Figure 4.36 shows the Time-to-Failure (TTF) as a function of

$V_{GStress}$ by considering a pBTI drift criteria of 0.15V. These results demonstrate that adopting a shorter gate length can result in more stable device operation in the frame of pBTI degradation. A short gate length also allows for a larger initial threshold voltage which is important in the context of a normally-off transistor.

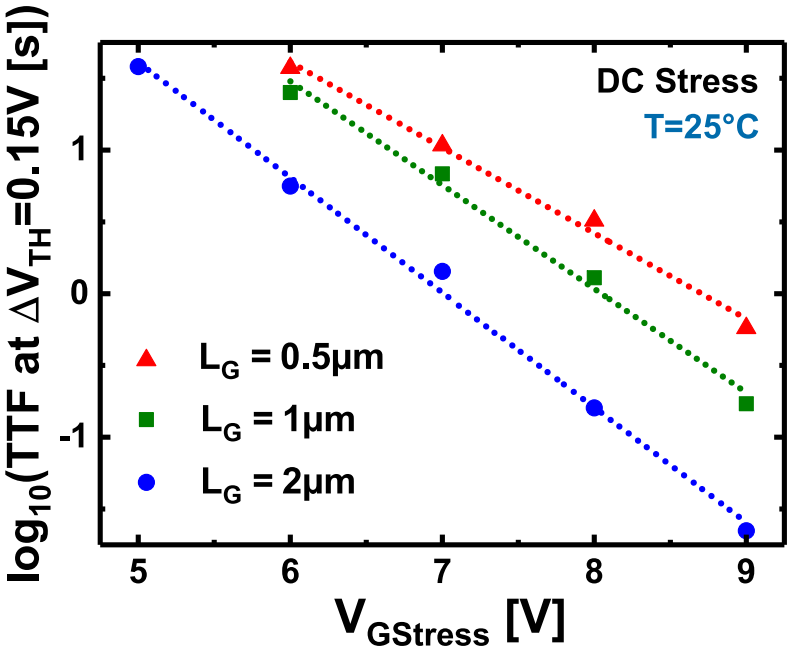

Figure 4.36. Time-to-failure extraction at $\Delta V_{TH} = 0.15$ V as a function of gate voltage stress varying from 5V to 9V at room temperature. It demonstrates that shortening the gate helps to increase the transistor lifetime considerably, especially at high $V_{GStress}$.

Conclusion

To conclude this chapter, a study explaining the pBTI shift difference between $I_D(V_G)$ and $C(V_G)$ characteristics under forward gate stress has been presented in a first time. In the framework of this study, an innovative experimental setup has been developed. It enables to perform ultra-fast and simultaneous measurements of $I_D(V_G)$ and $C(V_G)$ characteristics, measuring the drain current I_D and the gate displacement current I_{Dis} during the same fast V_G ramp. These measurements were thus performed using MSM technique, allowing to record the threshold voltage drift of $I_D(V_G)$ and $C(V_G)$ characteristics through two metrics, ΔV_{THI} and ΔV_{THC} respectively. Stress and recovery pBTI transients obtained via this innovative experimental setup revealed a difference between ΔV_{THI} and ΔV_{THC}. Performing measurements at different gate voltage stress and various temperatures the pBTI transients behavior was found to be similar to that observed in section 2.3. Indeed, the involvement in the pBTI degradation of both trap populations located within GaN:C and Al_2O_3 layers was again verified through Arrhenius analysis. It was also observed that the difference between ΔV_{THI} and ΔV_{THC} after a stress of 10^3s increases with $V_{GStress}$. Moreover, this difference is significant from a gate stress voltage higher than 1.5V. As mentioned in chapter 3, this gate voltage value is the minimum required to activate the electron injection mechanism in the Al_2O_3 defect band. When a positive gate voltage stress lower than 1.5V is applied, the threshold voltage shift is only caused by the ionization of C_N traps in GaN:C layer. Therefore the difference between ΔV_{THI} and ΔV_{THC} was attributed to charge trapping in Al_2O_3 defect band. TCAD simulations were used to model the electrons trapped in the gate oxide by negative surface charge at the gate oxide interface which was placed at different positions (gate corners, gate bottom, or gate sidewalls). The aim of these simulations was to highlight the influence of the trapped electron position at gate oxide interface on the $I_D(V_G)$ and $C(V_G)$ characteristic drift. Simulation results showed that the $I_D(V_G)$ drift (ΔV_{THI}) is attributed to the charge injection into the Al_2O_3 gate oxide defects at the gate corners, while the $C(V_G)$ shift (ΔV_{THC}) is mainly related to charge trapping at the gate bottom. It is due to the presence of the back-barrier layer in the epitaxy which leads to a V_{THI} controlled by the gate corners while V_{THC} is driven by the gate bottom. Previous results allowed to deduce that the Al_2O_3 defects density is more important at the gate corners than at the gate bottom.

In a second step, a study of the gate length influence on the pBTI degradation is presented. It is observed that the pBTI degradation decreases when the gate length reduces under a constant $V_{GStress}$. Although this effect is visible at room temperature, it is even more visible at high temperature where a difference of about 40% has been observed between $L_G = 0.5$ µm and $L_G = 2$ µm. In order to better understand this effect, an energy of about 130meV was extracted for all gate lengths. As a result, it demonstrated that the pBTI degradation follows the same temperature dependence regardless of the gate length. Therefore, it shows that the same underlying physical mechanisms occur for all three gate lengths. Such an effect can be explained by the overdrive gate voltage which is proportional to the applied electric field within the Al_2O_3 gate oxide layer. The overdrive gate voltage only depends on the initial V_{TH} which varies with the gate length, since the gate voltage is fixed. Indeed, experimental measurements revealed a threshold voltage reduction as the gate length increases (V_{TH} roll-up), which leads to an increase in the overdrive voltage for high gate lengths. Since the electric field is higher in the gate oxide when $L_G = 2$ µm compared to $L_G = 0.5$ µm, the electron trapping in the Al_2O_3 gate oxide defects is then increased for longer gate lengths. TCAD simulations have revealed the significant impact of the back-barrier layer on the conduction band distribution of GaN under the gate and thus on the initial threshold voltage. The gate voltage acceleration factor α has

also been extracted for the three different gate lengths. An increase of α with the gate length was observed. It confirms that the electric field in the gate oxide tends to increase with the gate length, implying a higher electron trapping in the gate defects, and thus a higher pBTI degradation. A lifetime decrease has thus been observed as the gate length increases, indicating that shortening the gate length can improve the device performance in terms of pBTI degradation.

General conclusion and perspectives

To conclude, BTI degradation includes all threshold voltage instabilities that mainly occur when a DC or AC gate voltage stress is applied. It is due to the trapping of the channel carriers in the pre-existing defects in the gate oxide, which causes a local electrostatic modification at the gate oxide interface, and hence a V_{TH} drift. Nowadays BTI degradation is one of the most critical issues in GaN-based transistors as it significantly alters the device performances and reduces their lifetime. During this Ph.D thesis, we focused on improving our understanding on BTI degradation observed in GaN-on-Si MOSc-HEMT developed at CEA-LETI. It has led to the development of innovative electrical characterization techniques dedicated to the assessment of threshold voltage instabilities. The results enabled trap identification and allowed to define their localization within the device structure. Furthermore, we investigated the underlying physical mechanisms related to the degradation using TCAD simulations and numerical models. Finally, we have proposed options to reduce this degradation based on the analysis. Although this study is based on GaN-on-Si MOSc-HEMT developed at CEA-LETI, a significant part of the results and assumptions can be extended to other HEMT architectures. The different aspects have been exhaustively detailed in the four chapters contained in this manuscript.

Chapter 1 gave a general description of the context in which the power electronics industry is evolving as well as challenges concerning new applications such as electrical vehicles, power converters, or ultra-fast charging. It also presents the GaN-based technology positioning on the market, as well as a description of the physical characteristics of GaN material. The advantages it offers over its competitors in terms of intrinsic physical characteristics when it is embedded in a power device are also discussed in the second part of this chapter. The third part mentioned the different technological challenges associated with the GaN epitaxy on foreign substrates such as Si or SiC substrates. In addition, a description of the different diode and transistor architectures proposed in the literature to exploit the interesting properties of 2DEG was presented. Indeed, their operating principles as well as their advantages and drawbacks have also been described. Finally, BTI degradations have been described, as well as the different associated measurement methodologies.

Chapter 2 was dedicated to trap identification associated with BTI degradation on the transistors developed at CEA-LETI. An overview of the literature on BTI degradation of GaN-based transistors was presented in a first time. Experimental results showed that the threshold voltage variations exhibit two time constants, separated by stable phases. A thorough study of this V_{TH} behavior has been carried out, and revealed the C_N trap influence located in GaN:C. We also demonstrated that GaN:C acts as a free hole reservoir, which are able to be trapped in the gate oxide after a certain time of negative gate stress. Finally, the third part of this chapter was related to an in-depth study of the pBTI degradation obtained under different positive gate volt-

age. Measurement results pointed out the presence of two trap populations acting upon different mechanisms on the pBTI degradation. One of them has been found to be related to C_N deep acceptor traps in GaN:C, while the other is associated with a Al_2O_3 defect band, located above the GaN conduction band. A gate voltage stress lower than 1.5V is enough to trigger the ionization of the neutral C_N traps ("0" $\rightarrow$ "1") leading to an increase of the GaN conduction band level at the Al_2O_3/GaN interface. It then causes a strong pBTI drift. Moreover, the electron injection mechanism in Al_2O_3 traps is activated at gate voltage stresses higher than 1.5V, which leads to a monotonous rise of V_{TH} with the stress time.

Chapter 3 is about pBTI degradation modeling. The Shockley-Read-Hall (SRH) model is presented in the first part and proposes to model the charge capture and emission processes within the traps. However, the temperature influence on the trapping process is not properly addressed and presents a limitation. Indeed, the pBTI transients obtained experimentally are highly temperature dependent. The NRMP (Non-Radiative Multi-Phonon) model was then presented in the second part. It can be considered as an improvement of the SRH model taking into account the traps temperature activation. Although it is able to reproduce qualitatively the experimentally obtained pBTI transients, we concluded that the NRMP model remains inaccurate in some cases, probably due to physical approximations. In the third part of the chapter, the Capture Emission Time map model is described, enabling to describe and even predict quantitatively the pBTI transients, even though it is based on a RC network that is probably far from the physical reality. On the other hand, we found that it is quite difficult to extract the CET maps. It is precisely for this reason that an innovative method allowing the automatic CET maps extraction is presented in the fourth section. Finally, results about the threshold voltage instability modeling at different temperatures have been presented and thoroughly analyzed in the fifth and last section.

Finally, chapter 4 deals with the influence of the fully recessed gate geometry properties on the pBTI degradation. The difference between $I_D(V_G)$ and $C(V_G)$ pBTI shifts obtained under various gate voltage stresses is first presented, and constitutes one of the two parts of the chapter. An innovative experimental setup developed during this Ph.D thesis to simultaneously measure $I_D(V_G)$ and $C(V_G)$ characteristics is initially presented. We demonstrated that it was possible to know where the charge trapping occurs at the gate-oxide interface, based on the experimental results and complementary TCAD simulations. Indeed, the $C(V_G)$ characteristic drift was associated with the gate bottom, while the $I_D(V_G)$ characteristic shift was assigned to charge trapping at the gate corners. The gate length influence on pBTI degradation is discussed in the second part. It was observed that the pBTI degradation is reduced when the gate length L_G is shortened at fixed gate stress due to an increase of the initial threshold voltage. Indeed, these results are due to an electric-field modification within the gate oxide which influences the threshold voltage shift. Additional TCAD simulations were carried out to improve our understanding of the relationship between gate length and initial threshold voltage. They showed that the V_{TH} roll-up behavior is induced by the back-barrier presence in the epitaxial structure.

Although the conclusions drawn throughout this thesis have provided a better vision of threshold voltage instabilities, it can still be improved. Indeed, in chapter 2, we pointed out the presence of an Al_2O_3 defect band located below the GaN valence band in the framework of the nBTI study. However, this defect band defect band has not been characterized since it appears after very long gate stress times ($> 10^3$ s) at high temperatures. To characterize it, nBTI measurements under Ultra-Violet radiation (> 3.4 eV) could then be performed. This should enable a free hole

generation in GaN, and lead to a quicker hole trapping within this Al_2O_3 defect band. It would then be possible to characterize it more easily. CET map extractions at negative gate voltage stress should enable to deduce the energy related to this Al_2O_3 defect band, as carried out in chapter 3. To go further, a study on the gate length influence dependence on nBTI transients might also be conducted. Indeed, at this time, there is no consistent explanation to describe this particular behavior, and a study on this topic should improve our understanding of nBTI degradation. Moreover, although the TCAD simulations have provided a better understanding of the physical mechanisms underlying BTI degradation, it is still difficult to quantitatively reproduce the latter. It is necessary to further develop the physical understanding of the device in order to consolidate the models implemented in the TCAD simulations. Finally, all the studies carried out in this thesis were performed by setting the drain voltage at 0V during the application of a negative gate voltage stress, while the tested transistors are designed to sustain high drain voltages of several hundred volts. Even tough the studies improved our comprehension of BTI degradation, V_{TH} drift behavior during high drain voltages stress need to be investigated, and remains a necessary research area before the commercialization of GaN-on-Si E-mode MOSc-HEMT developed at CEA-LETI.

List of publications

Conference article

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Patent

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Caractérisation des mécanismes de dégradation au sein de transistors de puissance à base de GaN sur Si, et étude de leur fiabilité électrique

Characterization of degradation mechanisms and electrical reliability study on GaN-on-Si power transistors

Résumé

L'avènement des véhicules électriques et des batteries de stockage d'énergie ont conduit à une croissance très importante du marché des composants de moyenne puissance. Les futures générations de composants devront supporter des tensions de l'ordre de 650V et devront fonctionner à des hautes fréquences (>1MHz). Les composants à base de GaN sur silicium sont vus à l'heure actuelle comme les meilleurs candidats pour atteindre ces spécifications. Actuellement, le CEA-LETI développe sa propre filière GaN sur Si, en partant du wafer de silicium jusqu'au module de puissance final. Ces composants possèdent une architecture disruptive basé sur une grille de type MOS et ont démontré d'excellentes performances statiques et dynamiques. Les dégradations temporelles sous stress en tension ainsi que les mécanismes de défaillances des composants sont en revanche mal connus. Le but de cette thèse vise à étudier les instabilités de tension de seuil V_{TH} des transistors à base GaN sur silicium à travers des techniques de caractérisation électriques avancées initialement dédiés aux technologies CMOS. Une partie des travaux menés ont portés sur l'identification des défauts à l'origine des dérives de V_{TH}, ainsi que sur la compréhension des mécanismes physique sous-jacent impliquant ces variabilités. Une attention particulière à également été apportée à la modélisation physique des phénomènes observés. Enfin, l'influence de l'architecture de grille sur les variations de V_{TH} été étudié notamment par le bias d'un dispositif expérimentale innovant. Bien que ces travaux ont contribué au développement des transistors à base GaN sur Si développés au CEA-LETI, la compréhension autour des instabilités de V_{TH} reste encore à améliorer.

Mots-clés : Fiabilité électrique, Caractérisation électrique, HEMT, GaN sur Si, Instabilités de V_{TH}, pBTI, nBTI.

Abstract

Electric vehicles and energy storage batteries have led to a very significant growth in the market for medium power devices. Future generations of devices will need to support voltages in the range of 650V and operate at high frequencies (>1MHz). GaN-on-Si devices are currently considered as the best candidates to meet these specifications. CEA-LETI is developing its own GaN-on-Si production line, from the silicon wafer to the final power module. In this context, the devices developed at Leti and featuring a disruptive architecture based on a MOS gate, have demonstrated excellent static and dynamic performances. However, the temporal degradation under stress as well as the failure mechanisms of the devices need to be further understood. The purpose of this thesis is to study the threshold voltage V_{TH} instabilities of GaN-based transistors on silicon through advanced electrical characterization techniques initially dedicated to CMOS technologies. A part of the research work focused on the defects identification at the origin of V_{TH} drifts, as well as on the understanding of the underlying physical mechanisms involved in these instabilities. Moreover, a particular attention has been paid to the physical modeling of the observed phenomena. Finally, the influence of the gate architecture on the V_{TH} variations has also been investigated through the implementation of an innovative experimental setup. Although this work has contributed to the development of GaN-on-Si transistors at CEA-LETI, the V_{TH} instabilities understanding still remains to be improved.

Keywords : Electrical reliability, Electrical characterization, HEMT, GaN-on-Si, V_{TH} instabilities, pBTI, nBTI