A Temperature-Aware Framework for Analog Design Using a gm/ID Approach

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université PARIS-SACLAY

A Temperature-Aware Framework for Analog Design Using a g_m/I_D Approach

Une méthodologie de conception des circuits analogiques consciente de la température basée sur g_m/I_D

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DOCTORAL SCHOOL
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Titre: Une méthodologie de conception des circuits analogiques consciente de la température basée sur g_m/I_D

Mots clés: Electronique Analogique, g_m/I_D, Effets de Température, Physique des semiconducteurs

Résumé: La quatrième révolution industrielle et l'arrivée de l'Internet des Objets introduisent de nouveaux défis pour la conception de circuits fiables. Dans les nouveaux véhicules, les circuits doivent pouvoir fonctionner de manière fiable dans une plage de température étendue. Les caractéristiques des transistors sont connues pour être fortement dépendantes de la température. Pour minimiser ces effets de dérive thermique, l'utilisation de points de polarisation ZTC (Zero Temperature Coefficients) a déjà été proposée. Cependant, cette approche ZTC considère l'influence d'un seul transistor sur le comportement en température des différentes spécifications du circuit et ne permet pas une approche plus générale et méthodologique.

D'autre part, les techniques de conception tels que la g_m/I_D permettent une approche méthodologique pour la conception analogique, sans possibilité d'analyse en température. Ce travail propose une extension de la méthodologie g_m/I_D en introduisant le concept de paramètres g_m/I_D normalisés en température. Ce paramètres permetent au concepteur de prendre en compte les effets de la température à un stade très précoce de la conception de la plupart des circuits analogiques, permettant ainsi une méthodologie unifiée pour la conception sensible à la température. Ces résultats sont validés à partir de données de simulation et de mesures de -40 $°C$ à 200 $°C$ avec la technologie XT018 de X-FAB. Trois exemples de conception différents sont également présentés dans cette thèse: circuit de référence de tension (Bandgap), Amplificateur à Transconductance (OTA), et oscillateur contrôlé par tension (VCO). Ces circuits présentent une meilleure performance en température comparable aux spécifications de l'état de l'art.

Title: A Temperature-Aware Framework for Analog Design Using a g_m/I_D Approach

Keywords: Analog Design, g_m/I_D, Temperature Effects, Semiconductor Physics

Abstract: The fourth industrial revolution and the Internet of things introduce new challenges to reliable circuit design. In this context, new transports circuits must be able to reliably work at an extensive temperature range. Transistor characteristics have been known to be highly temperature-dependent. Zero Temperature Coefficients (ZTC) bias points have already been proposed to minimize transistor's temperature drift effects. However, this ZTC approach considers the influence of a single transistor on the different circuit specifications' temperature behavior. Moreover, it does not allow and does not allow a more general and methodological approach.

On the other hand, design frameworks such as the g_m/I_D allow a methodological approach for analog design, with no possibility of temperature analysis. This work proposes an extension of the g_m/I_D methodology by introducing the concept of temperature normalized g_m/I_D parameters. This concept allows the designer to take temperature effects in a very early design stage in most analog circuits, allowing a unified methodology for temperature-aware design. Those results are validated from simulation and measurement data from -40 $°C$ to 200 $°C$ on the XT018 technology node of X-FAB. Three different design examples are also presented in this thesis, being: a Band Gap voltage reference, an operational transconductance amplifier (OTA), and a voltage-controlled oscillator (VCO). Those circuits present a better presenting a better temperature performance comparable to the state-of-the-art specifications.

Contents

List of Symbols

Acronyms

BJT Bipolar Junction Transistor

BSIM Berkley Short-channel IGFET Model

CAD Computer Aided Design

CLM Channel Length Modulation

CTAT Complementary to Absolute Temperature

DIBL Drain Induced Barrier Lowering

GaN Gallium Nitrite

GCA Gradual Channel Approximation

IoT Internet of Things

MOSFET Metal Oxide Silicon Field Effect Transistor

MTS Mean Temperature Sensitivity

NTC Negative Temperature Coefficient

PTAT Proportional to Absolute Temperature

RF Radio Frequency

SCCT Self-Cascode Composite Transistor

SiC Silicon Carbide

SOI Silicon Over Insulator

SRAM Static Random Access Memory

UICM Unified Current Control Model

ZTC Zero Temperature Coefficient

Physics Constants

k_b	Boltzman Constant	$8.617333262 \cdot 10^{-5}. eV/K$
q	Elementary Charge	$1.60217662 \cdot 10^{-19}. C$
ε_0	Vacum Permitivity	$8.85418782 \cdot 10^{-14}. F/cm$

Transistor Parameters

g_m/g_{ds}	Transistor Self-Gain	$1/V$
g_m/I_D	Drain Current to Drain to Gate Transconductance ratio	$1/V$
α_{th}	Treshold Voltage Linear Temperature Coefficient	V/K
β_μ	Carriers Mobility Temperature Coefficient	
χ_{si}	Semiconductor Vacum Energy	V
η	Non-Ideality Factor	
μ_n	Electrons Mobility	cm^2/Vs
μ_p	Holes Mobility	cm^2/Vs
μ_{eff}	Effective Mobility of Carriers at the Inversion Layer	cm^2/Vs
ϕ_m	Metal Workfunction Voltage	V
ϕ_T	Thermal Voltage	V
ψ	Electric Potential	V
ψ_B	Bulk Electric Potential	eV
ψ_p	Pintch-off Electric Potential	V
ψ_s	Electric Potential at Semiconductor Surface	V
ψ_{sa}	Surface Potential Approximation at Depletion and Accumulation	V
$\sigma(L)$	DIBL Coefficient	V/V

Θ_D	Debye Temperature	K
ε_{si}	Silicon Permitivity	F/cm
ξ	- Electric Field	V/cm
C_p	Specific Heat Capacity at Constant Pressure	$J \cdot Kg^{-1} \cdot K^{-1}$
C_{ds}	Drain to Source Capacitance	F
C_{gb}	Gate to Bulk Capacitance	F
C_{gd}	Gate to Drain Capacitance	F
C_{gg}	Total Gate Capacitance	F
C_{gs}	Gate to Source Capacitance	F
C_{ox}	Capacitance Density from Oxide	F/cm^2
C_{si}	Silicon Capacitance	F
E_A	Ionization Energy for the Acceptor	eV
E_C	Conduction Band Energy	eV
E_D	Ionization Energy for the Acceptor	eV
E_F	Fermi Level Energy	eV
E_i	Intrinsic Fermi Level Energy	eV
E_V	Valence Band Energy	eV
E_G	Semiconductor Band Gap	eV
E_{sat}	Minimum Electric Field for Mobility Saturation	
$F(\psi)$	Kingston Function	
g_m	Drain to Gate Transconductance	S
G_p	Equivalent Parallel Conductance	S
G_{comp}	Compensation Conductance	S
$G_{d_{ZTC}}$	Normalized Drain g_m/I_D parameter Zero Temperature Coefficient Bias point	

$G_{g_{ZTC}}$	Normalized Gate g_m/I_D parameter Zero Temperature Coefficient Bias point	
$g_{m_{ZTC}}$	Gate Transconductance Zero Temperature Coefficient Bias Point	
I_B	Bulk Current	A
I_D	Drain Current	A
i_f	Normalized Forward Current	
i_r	Normalized Reverse Current	
$I_{DS_{ZTC}}$	Drain to Source Current ZTC Bias Point	
I_{DS}	Drain to Source Current	A
J_n	Electrons Current Density	A/cm
J_p	Holes Current Density	A/cm
L_{eq}	Equivalent Inductance	H
n	Electrons Concentration	cm^{-3}
N_A	Acceptor Doping Concentration	cm^{-3}
N_A^-	Ionized Acceptor Doping Concentration	cm^{-3}
N_C	Effective Density of States at the Conduction Band	cm^{-3}
N_D	Donnors Doping Concentration	cm^{-3}
N_D^+	Ionized Donnors Doping Concentration	cm^{-3}
n_i	Intrinsic Carriers Concentration	cm^{-3}
n_q	Equivalent Non-Ideality Factor	
N_V	Effective Density of States at the Valence Band	cm^{-3}
p	Holes Concentration	cm^{-3}
q_b	Normalized Bulk Charge	
Q_d	Inversion Charge at the Drain	C
Q_i	Invertion Charge	C

q_i	Normalized Inversion Charge	
Q_s	Inversion Charge at the Source	C
$Q_s(\psi_s)$	Surface Charge as a Function of the Surface Potential	C
q_{id}	Normalized Inversion Charge at Drain	
q_{im}	Normalized Inversion Charge at Channel Midle Point	
q_{is}	Normalized Inversion Charge at Source	
R_s	Equivalent Series Resistance	Ω
$S_x^{y(x)}$	Sensitivity of y in relation to x	
$T_{C_{eqq}}$	Equivalent Temperature Coefficient	
V_p	Pintch-off Voltage	V
V_{ch}	Quasi-Fermi Level at the Channel	eV
$V_{D_{sat}}$	Minimum Drain Source for Mobility Saturation	V
V_{DS}	Drain to Source Voltage	V
V_{FB}	Flatband Voltage	V
V_{GB}	Gate to Bulk Voltage	V
V_{SB}	Source to Bulk Voltage	V
V_{th}	Transistor Threshold Voltage	V
Z_{in}	Input Impedance	Ω
Z_{out}	Output Impedance	Ω
L	Drawing Channel Length	μm
W	Drawing Channel Width	μm

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Chapter 1

The need of Temperature-Aware Circuits

According to Professor Jeremy Rifkin, all significant economic changes in history originate from a paradigm change over three leading technologies: communication, transport, and energy [11]. In the first industrial revolution, the steam printing press and the telegraph joined with charcoal, and railroads allowed the beginning of modern urban society and industry. Some decades after, telephone and radio communications powered by a centralized electricity system, mostly based on fossil fuels and cars, allowed urban and industrial growth to the present state.

In the last few years, the most significant advancement in communication is that the internet is now arriving in transport and energy through the Internet of Things (IoT) framework. The exponential advances in circuits, processing power, and the internet deeply affected our relationship with technology and reshaped our society. Those innovations, promoted in the latest decades, now arrive at objects with Big Data, allowing better performance in data analytics and the Internet of Things (IoT), shortening the time to acquire information, and allowing real-time control and analysis of processes [1].

As with the previous industrial revolutions, Industry 4.0 starts to deeply affect our way to design, manufacture and consume new products. In his book entitled Entropy [11], Professor Rifkin discusses the productivity paradox present in our society. Even though technology and education standards have known and massive growth, producing better performance machines and workers, productivity has been declining in the last 20 years. This paradox is later discussed in his book and explained by introducing thermodynamical inspired modeling of economics, showing that the major efficiency losses in the production phases are due to our inability to control our processes closely.

The Industry 4.0, the productivity paradox is solved using the IoT framework, where connected machines and sensors are used to gain better knowledge and have

better decisions through the process. In this context, it becomes critical to access real-time, accurate, and reliable information to monitor and control any process included in the IoT framework.

To achieve this goal, circuits and sensors must work reliably, have low production costs and environmentally sustainable materials. According to the Boston Consulting Group [2], the fast spread of IoT is mainly limited by production and maintenance costs. Circuit reliability is a complex task and should be considered through the whole design and manufacturing process. Since IoT circuits need to be placed inside machines, vehicles, and portable devices, they can be submitted to extreme and harsh environments.

1.1 Circuits Reliability in Harsh Environments

With the increasing demand for sensors to monitor performance, the readout circuits must reliably work under the different environmental conditions they are surrounded by. Those external perturbations must not deteriorate their ability to provide fast and accurate measurements. Temperature, pressure, and radiation impacts on circuit reliability have to been studied since the early stages of electronics development [12].

Much work has been done to model, characterize and minimize different physical phenomena that reduce circuit reliability [13]–[15]. In IoT and smart vehicle applications, temperature considerations are arguably one of the main challenges for reliable circuit design [16]. Today, electric vehicles represent new investments in sensors and integrated circuits that, between 2017 and 2019, accounted for 1.3 billion dollars worldwide, with projections of growth in the next coming years [17]. The usual approach for small temperature sensitivity circuits, relies on wide bandgap semiconductor materials such as GaN [18] or SiC [19]. Even though those materials present intrinsically smaller performance degradation over temperature [18], [19], they come with a higher production cost, not enabling the integration of digital circuits on-chip, an essential feature of smart sensing.

Even though temperature effects are widely understood and present in the simulation transistor models, one needs to have a deep physical understanding of their origins and consequences on circuits to incorporate and minimize those effects. Based on the physical characterizations of the problem, some works have been done that create simple design rules that are easier to be followed and taken into account in the early design stages. In [13] a pareto approach to optimization is developed to account for component statistical variability. In [14] a design methodology to overcome aging effects and transistor variability in Radio Frequency circuits (RF) is proposed. In [15] a tool that allows the evaluation and adjustment of tracks dimensions to overcome electromigration effects is proposed.

However, when considering temperature effects, no general methodology was proposed in the literature before this work.

1.2 Context of Temperature Considerations in Circuits

The search for temperature-aware circuits started even before the popularization of integrated circuits. In 1956, Lin presented one of the first papers concerning temperature considerations in circuits [20]. In this work, Lin and Barcor present and analytical and experimental results showing a technique for stable saturation current of germanium over temperature.

Widlar, inspired by [20] and the advance of circuits integration, proposes first a paper that takes advantage of the thermal coupling provided by integration to propose some of the basic building blocks of modern analog integrated electronics [21]. Some years after Widlar publishes "New Developments in IC Voltage Regulators" [22], in this work, the working principles of arguably the circuit where temperature studies were more explored in the research are presented, the bandgap reference.

The voltage reference proposed by Widlar laid the foundations for a research problem that continues to be explored 50 years after his proposition [23]. The working principle of the bandgap reference is to combine two voltages having similar temperature behaviors in magnitude but with opposite signals arriving at a voltage with a zero temperature coefficient (ZTC). His name comes from using the semiconductor bandgap temperature dependency to create a negative temperature coefficient (NTC) voltage.

The same principle of joining two opposite temperature coefficient effects has been explored in low temperature sensitivity circuits. In [24] the opposite temperature coefficients from the threshold voltage and mobility coefficient of MOSFET transistors were used to propose ZTC bias points for the drain current and the maximum operating frequency of an SRAM circuit. The drain current ZTC bias ($I_{DS_{ZTC}}$) has been used for temperature-aware designs since their first appearance in literature. As an example, Fonseca et al. [25] used the same temperature models and techniques employed by [24] to propose a temperature-aware analysis of a latched comparator. Toledo et al. explored another ZTC bias point in [26], the gate transconductance ZTC point, based on the UICM model and explored this point to design a 34 ppm/$^{\circ}C$ single-ended Gm closed-loop resistor.

In circuits in which in some transistors eighter the drain bias current (I_{DS}), or the gate transconductance (g_m) are key for this circuit parameter, the known ZTC can be used to reduce temperature dependency. However, this is not necessarily the case for all circuits, and no general framework exists for obtaining

the desired temperature behavior. Besides, the existence of both ZTC points depends hugely on the transistor's mobility temperature behavior that has gained increasing complexity in more recent nanometric scale transistors [27].

On the other hand, with the advances in transistor miniaturization, short-channel effects have become an important consideration in analog design. These second-order effects increase design challenges and make simple transistor models no longer effective. Incorporating short-channel effects into hand-calculation models leads to impractical equations to solve, making those models lose their purpose. On the other hand, since this effect has gained importance, oversimplified models lose their accuracy. Therefore, new design techniques have been developed to aid analog circuit development providing a good compromise between simplicity and accuracy.

One of the techniques that stands out in analog circuit design is the g_m/I_D methodology [28]. Proposed by Silveira *et al.* [28] is a powerful transconductance to drain current method to help designers size up transistors quickly. The so-called "g_m/I_D design" was initially developed to calculate parameters such as small-signal gain and bandwidth, later extended to distortion analysis [29], age-dependent degradation effects [30], and short channel effects [31], but not temperature effects.

1.3 Contributions

This work proposes a temperature analysis using the g_m/I_D methodology. Introducing the concept of temperature normalized g_m/I_D parameters. This analysis allows the designer to account for temperature effects on circuits from an early design step using sensitivity analysis and the normalized g_m/I_D parameters ZTC bias points.

The presented ZTC bias points have no significant influence on mobility temperature dependency and are still compatible with the g_m/I_D methodology. The methodology is then applied to standard cells in analog design. The final designs present temperature awareness with little or nil performance constraints. This thesis resumes the present the obtained results in the following publications:

1.3.1 Journal Papers

- **Martins, J. R. R. O.**, Mostafa, A., Juillard, J., Hamani, R., De Oliveira Alves, F., & Maris Ferreira, P. (2021). A Temperature-Aware Framework on gm/ID-Based Methodology Using 180 nm SOI From 40 °C to 200 °C. IEEE Open Journal of Circuits and Systems, 2, 311322. https://doi.org/10.1109/OJCAS.2021.3067377

- **Martins, J. R. R. O.**, De Oliveira Alves, F., & Maris Ferreira, P. (2021). A General g_m/I_D Temperature-Aware Design Methodology Using 180 nm CMOS up to 250 °C. 2021 Journal of Integrated Circuits and Systems (Submitted)

1.3.2 International Conferences

- **Martins, J. R. R. O.**, De Oliveira Alves, F., & Maris Ferreira, P. (2021). A 237 ppm / °C L-Band Active Inductance Based Voltage Controlled Oscillator in SOI 0.18 μm. 2021 34th Symposium on Integrated Circuits and Systems Design (SBCCI), 1115.https://doi.org/10.1109/SBCCI53441.2021.9529990

- Ferreira, P. M., **Martins, J. R. R. O**., Mostafa, A., & Juillard, J. (2019). Process-Voltage-Temperature Analysis of a CMOS-MEMS Readout Architecture. 2019 Symposium on Design, Test, Integration Packaging of MEMS and MOEMS (DTIP), 14. https://doi.org/10.1109/DTIP.2019.8752699

- Mostafa, A., Juillard, J.,**Martins, J. R. R. O.**, & Maris Ferreira, P. (2019, May). An Adaptative Ratio-Metric Analog-To-Digital Interface For Weakly-Coupled Resonant Sensors Based On Mutually Injection-Locked Oscillators. Proc. IEEE Design, Test, Integration & Packaging of MEMS/MOEMS. https://hal.archives-ouvertes.fr/hal-02290315

- **Martins, J. R. R. O.**, Avignon-Meseldzija, E., & Maris Ferreira, P. (2019, August). Temperature-Aware gm/ID-based Methodology for Active Inductor Design. Workshop on Circuits and System Design. https://hal.archives-ouvertes.fr/hal-02268794

1.3.3 National Colloquium

- **Martins, J. R. R. O.**, & Maris Ferreira, P. (2019, June). Méthodologie de Conception Conscient des Variations en Température: Circuits de Lecture pour les Environnements Sous Contraintes. Journées Nationales Du Réseau Doctoral En Micro-Nanoélectronique (JNRDM). https://hal.archives-ouvertes.fr/hal-02294927

- **Martins, J. R. R. O.**, & Maris Ferreira, P. (2019, June). Méthodologie de Conception Conscient des Variations en Température: Circuits de Lecture pour les Environnements Sous Contraintes. GdRSoC2 `https://hal.archives-ouvertes.fr/hal-02294927`

1.3.4 Open Source Journals and Libraries

- **Martins, J. R. R. O.**, De Oliveira Alves, F. & Ferreira, P. (2021). MOSLab.jl [Julia]. https://github.com/Rapos0/MOSLab.jl, DOI:10.5281/zenodo.5589821 (Original work published 2021)

- **Martins, J. R. R. O.**, De Oliveira Alves, F.& Ferreira, P. (2021). IC Layout Render [Python]. https://github.com/DrPiBlacksmith/icLayoutRender DOI: 10.5281/zenodo.5618268 (Original work published 2021)

Chapter 2

Transistor Temperature Effects

The first theoretical and experimental papers from Bardeen, Shockley and Brattain already pointed out the temperature as an important parameter on semiconductors [32], [33]. In those papers, performances at different temperatures were usually presented to highlight the temperature effects. However, with the increasing complexity in circuit design, minimization of temperature effects were reserved for critical areas, such as voltage references and precision circuits, wherein less important blocks temperature were controlled externally by using either heat sinks or forced ventilation.

With the increase of electronics portability and miniaturization, external temperature control are no longer an option since it requires an important space in the IoT imprint and is exigent in power consumption. Moreover, in applications such as autonomous vehicles, temperature heavily fluctuates, for example, due to mechanical losses in nearby devices, making temperature changes in electronics inevitable.

To understand how temperature changes affect transistor performances and how those effects are integrated into simulation models. This chapter reviews the different temperature effects on transistors. First, by making a brief introduction into semiconductor physics, evaluating how temperature affects the different material properties, then using these principles analyze how modern transistor models incorporate temperature effects and explore how these physical phenomena can be used in the designer's favor to achieve temperature-awareness in some cases. All the concepts on this chapter are extensively reviewed on the developed open source MOSLab package [34]

Those results are compared when possible to measurement data from X-FAB XT018 technology, a leading technology on the automotive industry. The XT018 allows the design of mixed signal circuits with simulation models validated from -40 °C to 175 °C. This manuscript presents also measurement data up to 200 °C never seen before on the literature for this technology.

2.1 Semiconductor Temperature Effects

Semiconductors are crystalline materials[1], that even though they behave like insulators at very low temperatures, can conduct somewhat at temperatures close to the ambient temperature [35].

Classifying materials conductivity into insulators, semiconductors, and conductors can be done using a measurable quantity: the bandgap. The bandgap is defined as the minimum energy necessary to make an electron on the valence band (bounded to the crystal lattice) go to the conduction band. The periodicity of the crystal lattice can explain the origin of the bandgap, that due to phonons interactions [2] and thermal expansion, will change with temperature.

2.1.1 Band Gap Temperature dependency

The determination of the bandgap temperature dependency from a theoretical point of view, incorporating both effects, without fitting parameters was only proposed recently in literature [36]:

$$\begin{cases} E_G(T) &= \left\{ E_G(T_0) - [E_G(T_0) - E_G(T_1)] \left(\frac{\int_{T_0}^{T} C_p(T)dT}{\int_{T_0}^{T_1} C_p(T)dT} \right) \right\} \frac{\left(1+\int_0^{T_0} \alpha(T)dT\right)^3}{\left(1+\int_0^{T} C_p(T)dT\right)^3} \\ C_p(T) &= \frac{9Nk_B}{M} \left(\frac{T}{\Theta_D}\right)^3 \int_0^{\frac{\Theta_D}{T}} \frac{x^4 e^x}{(e^x-1)^2} dx \end{cases}, \tag{2.1}$$

where N is the Avogadro number; Θ_D the Debye temperature; C_p the specific heat capacity at constant pressure; M the molar mass and α the temperature-dependent linear expansion coefficient of the semiconductor. Even though (2.1) fits pretty well with data, it involves a computational-intensive process to calculate, and it is not feasible for circuit simulations.

Previous to the physical modeling proposed on [36] some semi-empirical bandgap temperature dependencies were highlighted. The first model proposed by [37] comes from the asymptotic temperature behavior of the bandgap that has a quadratic behavior at low temperatures and a linear behavior when the temperature is closer to Θ_D.

$$E_G(T) = E_G(T_0) - \frac{\alpha T^2}{T+\beta} \tag{2.2}$$

Equation (2.2) is still widely used in compact modeling [6] but not universally, as an example, in [38] a second-order polynomial gives the temperature behavior of the bandgap. Figure 2.1 shows the comparison between [37] used also in

[1] Materials in which atoms are arranged periodically

[2] Thermal vibration waves propagating through the coupled charge carriers

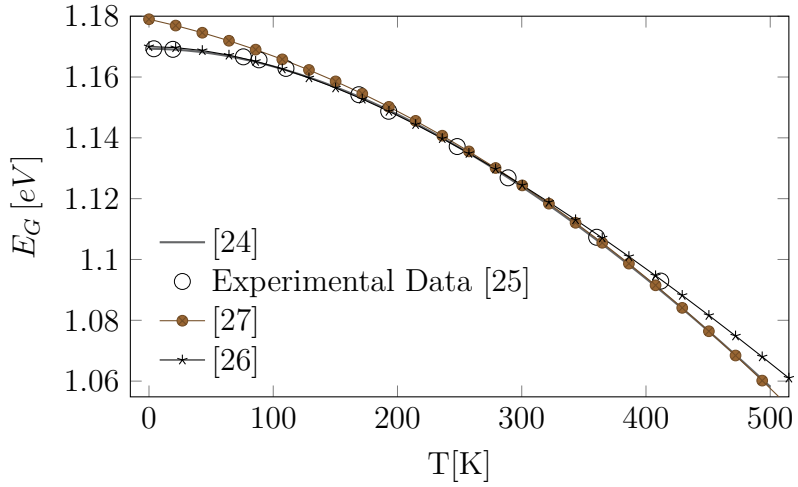


Figure 2.1: Bandgap temperature model comparison to experimental data from [36].

[6],[36], and [38] models and experimental data extracted from [37]. The calculation of Varnishni's model implemented in Julia using an adaptive Gauss-Kronrod integration method took 10 times longer to calculate than the simpler Gen Model [34].

2.1.2 Carriers Concentration

When considering a classical approach to the electrons and holes behavior, the Gibbs measure predicts that the probability per unit time that energy as large as E_g at one atomic site is proportional to [see Appendix A]

$$p\left(E = E_g\right) \propto e^{-\frac{-E_g}{k_b\ T}}, \tag{2.3}$$

where T is the temperature, and k_b is the Boltzmann's constant. At a given temperature, those holes and electrons pairs will be generated and recombined with the probability (2.3). The probability of this recombination depends on the generation of an electron and a hole and therefore is proportional to the product of both carriers' generation probability [35]. Since in equilibrium, the generation and recombination rates must equal the electron density (n) and hole density (p) product (usually denoted n_i^2) must be proportional to (2.3). Besides, in equilibrium, in the absence of external electric field n must be equal to p and therefore to n_i also called the intrinsic carriers concentration.

A more careful quantum treatment that takes into account the Pauli exclusion principle predicts a probability distribution other than Boltzmann's, the Fermi

distribution. However for energy bigger than $3k_bT$ the Boltzmann approximation is considered a good approximation [see Appendix B]. Figure 2.2 shows the calculation of the intrinsic carriers concentration using the Fermi-Dirac distribution. As it can be seen the n_i temperature dependency is almost exponential at temperatures close to the ambient temperature.

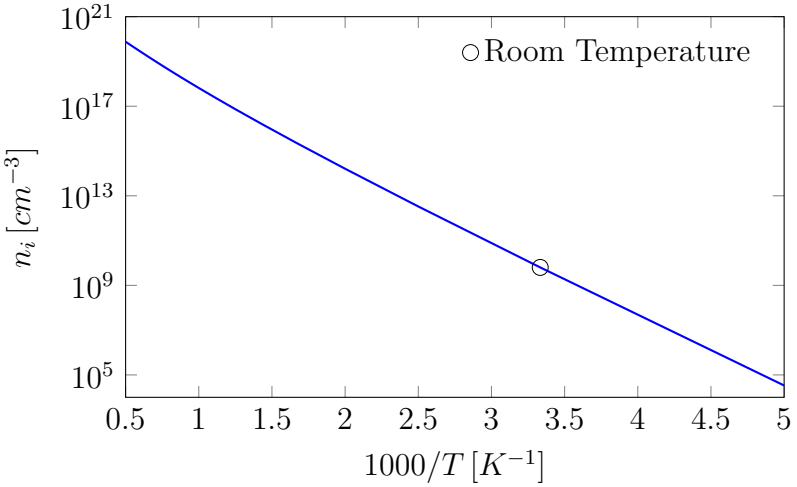


Figure 2.2: Intrinsic carrier concentration relation with inverse temperature using Fermi-Dirac distribution.

2.1.3 The Fermi Level

Since the number of electrons at the conduction band and holes are equal in equilibrium, the middle of the bandgap can be seen as the energy level, in which there is an equal probability of having an electron or a hole. This energy level is named the Fermi level (E_F), or chemical potential can also be seen as the mean semiconductor energy. By introducing the E_F, the electrons and holes concentrations can be expressed by:

$$n\left(T\right) = N_C\left(T\right) e^{-\frac{E_C - E_F}{k_b T}}, \tag{2.4}$$

$$p\left(T\right) = N_V\left(T\right) e^{\frac{E_V - E_F}{k_b T}}, \tag{2.5}$$

where N_C and N_V are the effective density of states at the conduction and the valence band with an exponential temperature relation; E_C and E_V are the minimum conduction band energy and the maximum valence band energy. Using the

definitions of n and p using the Boltzmann distribution, the intrinsic Fermi level (E_i) can be calculated

$$E_i = \frac{E_C + E_V}{2} + \frac{k_B T}{2} \ln\left(\frac{N_V}{N_C}\right). \tag{2.6}$$

Equation (2.6) shows that as explained before, the intrinsic Fermi level is very close to the middle of the bandgap $^{(E_C+E_V)}/_2$ and that would be the case if $N_C = N_V$. However the difference on the effective mass of electrons and holes makes the intrinsic Fermi level slightly below the middle of the bandgap.

2.1.4 Doping

The semiconductor conductivity is directly related to the number of free carriers. So far, the only two ways that extra free carriers can be added are either by thermal energy or an external electron source. However, there is still a major tool that can be used to control the number of free carriers on Silicon: doping. Doping consists of substituting silicon atoms (that possess four electrons on the valence shell) with other atoms having three or 5 electrons on the valence shell.

For Silicon technology, the usual dopants used are Boron and Phosphorus. The addition of those elements will add one extra electron (donor) or vacant electron (acceptor) per dopant atom. The number of extra free electrons or free holes is directly proportional to acceptors density N_A or donors density N_D. The addition of electrons and holes will change the position of the Fermi-Level, that can be interpreted as the electrons mean energy level, the addition of electron donors will fill higher energy levels and increase the Fermi-Level when compared to the intrinsic level (E_i) while the addition of acceptors will decrease the Fermi level.

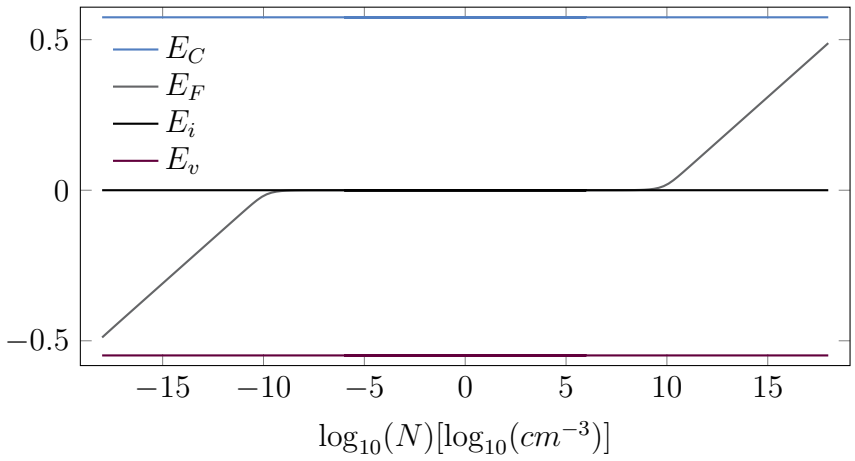


Figure 2.3: Fermi-level position due to doping concentration, negative values are for P-doped silicon and positive for N-doped Silicon.

Figure 2.3 illustrates the Fermi level shift for different doping levels, where negative part of the x-axis is P-doping and the positive N-doping at 300 K. It is noticeable that for doping concentrations smaller than n_i approximately $10^{-10}\ cm^{-3}$ at 300 K the Fermi-Level shift is negligible.

The insertion of dopants disturb the crystalline structure and add intermediate levels of energy, usually, inside the Band Gap at the doping atom locus. When doping is added, depending on the impurity level and temperature, not all dopants will necessarily present a free carrier (ionized). The ionized concentration for donors and acceptors is given by [39]

$$N_D^+ = \frac{N_D}{1 + g_D e^{\frac{E_F - E_D}{k_B T}}} \tag{2.7}$$

$$N_A^- = \frac{N_A}{1 + g_A e^{\frac{E_A - E_F}{k_B T}}} \tag{2.8}$$

where g_A and g_D are the ground state degeneracy factor for acceptors and donors; and E_A and E_D the ionization energy for the acceptor and donor. Those effects are only at very low temperatures, since for higher temperatures the thermal energy is sufficient to ionize the dopants. However, for a given doping concentration at a high enough temperature, since n_i presents a positive temperature coefficient, the intrinsic concentration will be higher than the dopping concentration. Those effects are illustrated on Fig. 2.4 for a N doped Silicon with doping concentration of $10^{-15}\ cm^{-3}$.

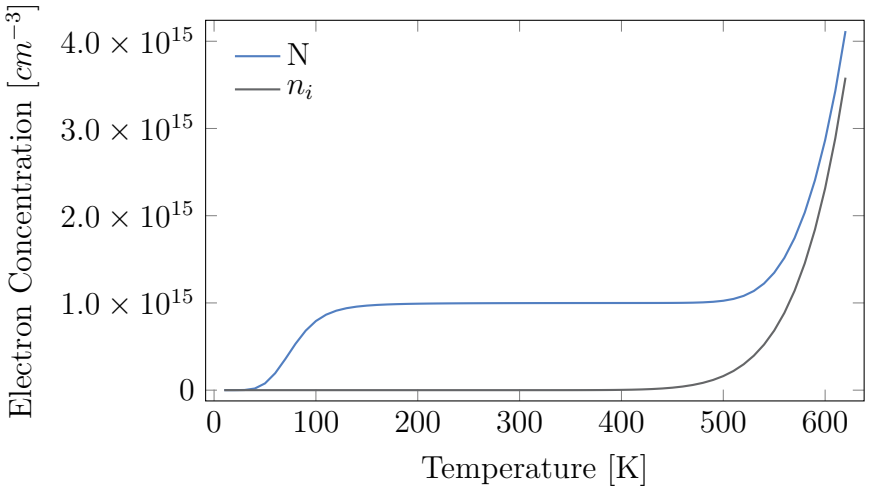


Figure 2.4: Electrons concentration for a N doped Silicon with doping concentrations of $10^{-15}\ cm^{-3}$ and $E_a = 0.044\ eV$.

2.2 MOSFET

An illustration of a bulk MOSFET structure is presented in Fig. 2.5; it is formed by two minority charges reservoirs (drain and source) implanted on a bulk semiconductor. Between the two reservoirs, an oxide is added to form a capacitor that allows charge control, as shown in Fig. 2.5.

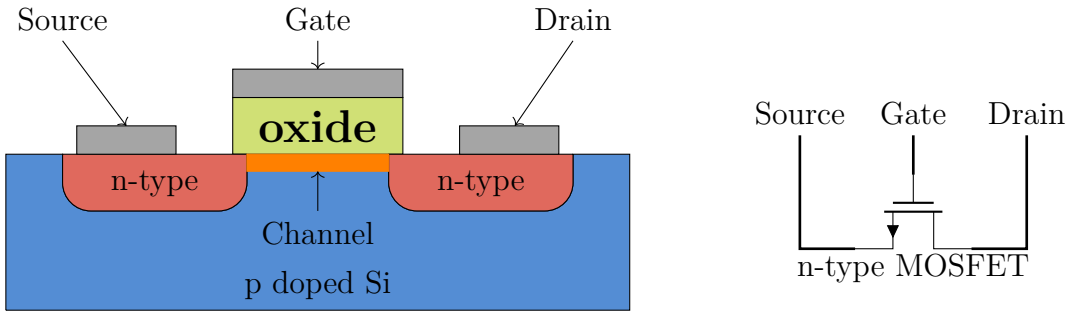


Figure 2.5: MOSFET structure and electrical symbol.

The gate contact forms a capacitor between the metallic contact and silicon surface that allows the repulsion or attraction of minority carriers. When a voltage difference is applied between the drain and source, a carrier's concentration gradient and an electric field create a current between drain and source. The MOSFET behavior can be divided into two distinct but related analyses: MOSFET electrostatics and transport phenomena that will be the subject of the next two subsections.

2.3 The MOS Electrostatics

In the middle of the channel, the MOSFET consists of a simple two-terminal device composed from a sandwich of a contact material (historically metal, but nowadays highly doped polysilicon), a thin oxide layer, and a semiconductor slab as shown in Fig. 2.6. In equilibrium, the Fermi-Levels must align since they represent the mean system potential energy. Considering a metal with the same Fermi-Level as a P-doped semiconductor, the band structure will be as illustrated Fig. 2.6.

The total structure capacitance is given by the series of the linear C_{ox} capacitor given by ε_{ox}/t_{ox}, where ε_{ox} is the oxide material permittivity and t_{ox} the oxide thickness. The silicon capacitance C_s is dependent on the silicon surface potential ψ_s and can be obtained by solving the Poisson equation on silicon. For a P-dopped silicon with complete ionization of dopants and assuming Boltzmann statistics, the Poisson equation can be written as

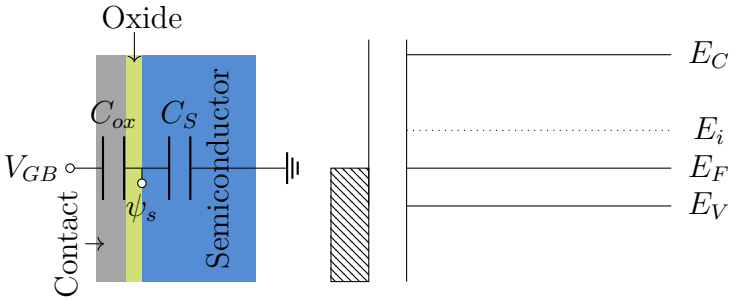


Figure 2.6: Physical structure and Band Diagram on the y axis of a MOS Structure.

$$\frac{\partial^2\psi}{\partial y^2} = -\frac{q}{\varepsilon_{Si}}\left[N_C \cdot e^{-\frac{Ec-Ef-q\psi(y)}{k_B \cdot T}} + N_V \cdot e^{-\frac{Ef-Ev+q\psi(y)}{k_B \cdot T}} - N_A\right], \tag{2.9}$$

$$\xi(\psi) = -\frac{\partial\psi(y)}{\partial y} = \pm\sqrt{\frac{2k_B T N_A}{\varepsilon_{Si}}}F(\psi) \tag{2.10}$$

where $\psi(y)$ is the electrical potential across the semiconductor; ξ is the electric field and $F(\psi)$ is called the Kingston function since was first proposed by Kington *et al.* [40], another proposition with a complete treatment using Fermi-Dirac Statistics, non-complete dopants ionization and minority carriers inclusion can be found in [41]. The surface charge $Q_s(\psi_s)$ can be calculated as $Q_s(\psi_s) = -\varepsilon_{si}\xi(\psi_s)$.

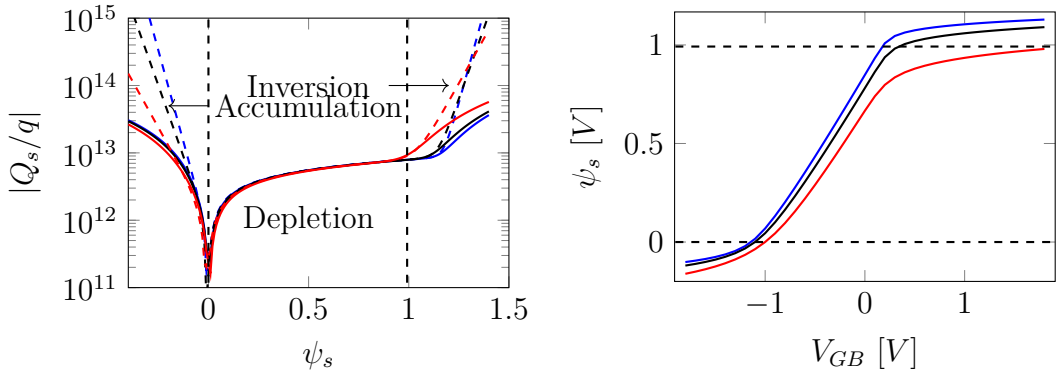


Figure 2.7: Surface Charge of a P-type Silicon with the assumptions of [29] (dashed) and [30] (solid) (a) and the surface potential (b) for an with P-type dopant concentration of $5 \cdot 10^{18}\ cm^{-3}$ considering a Boron doping with $E_a = 0.044\ eV$ at three different temperatures: $-40\ ^\circ C$ (blue), $27\ ^\circ C$ (black) and $175\ ^\circ C$ (red).

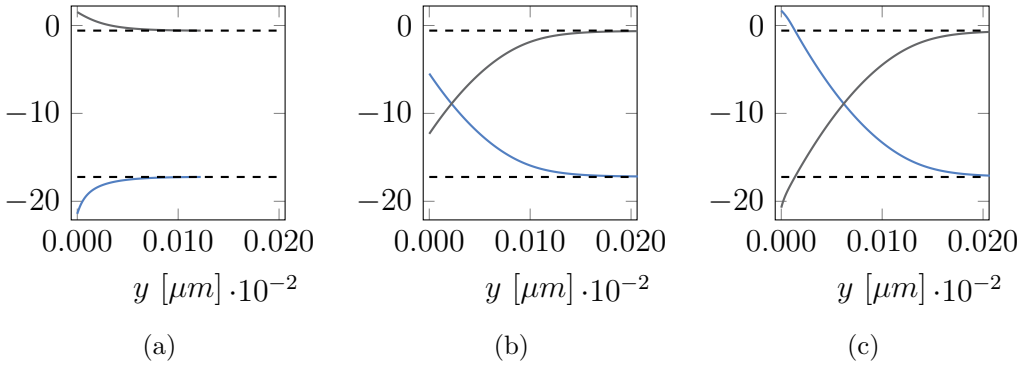


Figure 2.8: Electrons ($\log_{10}(n(y)/N_A)$ blue) and holes ($\log_{10}(p(y)/N_A)$ grey) concentration on the bulk of a PMOS at three different biasing conditions respetivelly accumulation (a),depletion (b) and inversion (c).

The surface charge relation with the surface potential (ψ_s) by using the definitions of [40] and [41] are here illustrated on Fig. 2.7 for a P-type Silicon with doppant concentration of $5 \cdot 10^{18}\ cm^{-3}$ considering a Boron doping with $E_a = 0.044\ eV$ at three different temperatures: $-40\ ^\circ C$, $27\ ^\circ C$ and $175\ ^\circ C$

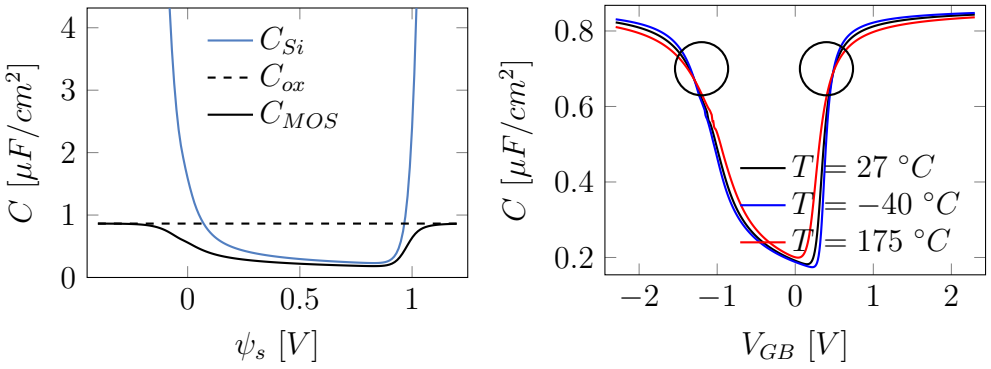
The graph present three different regions with different behaviours, first for $\psi_s < 0$ the majority carriers are attracted to the Silicon-Oxide interface creating an accumulation of majority carriers. For $0 < \psi_s < 2\left(E_F - E_i\right)/q$, the minority carriers are attracted to the interface and recombinate with minority carriers creating an depletion region on the semiconductor. For $\psi_s > 2\left(E_F - E_i\right)/q$ the band-bending is such a layer of minority carriers form on the interface "inverting" the majority carriers on the region. This can be better visualized with a plot of electrons and holes concentrations on the Silicon for ψ_s at those three different regions illustrated on Fig. 2.8.

All the present electric information from the MOS structure is given as a function of ψ_s, however the variation of ψ_s is actually given by the voltage between the gate and the bulk (V_{GB}), by the Kirchhoff voltage law:

$$V_{GB} = V_{FB} + \psi_s - \frac{Q_s\left(\psi_s\right)}{C_{ox}} \tag{2.11}$$

$$V_{FB} = \phi_m - \chi_{Si} - E_{C_{Si}} - E_{F_{Si}} \tag{2.12}$$

where, V_{FB} is the flatband voltage that accounts for the difference on the metal and semiconductor work function; ϕ_m the metal work-function; χ_{Si} the semiconductor vacuum energy; $E_{C_{Si}}$ e $E_{F_{Si}}$ the semiconductor conduction and Fermi levels; and C_{ox} the oxide capacitance per unit area given by $\varepsilon_{ox}/t_o x$. Solving the (2.11) for ψ_s cannot be done analytically but an numeric solution for ψ_s is shown on Fig.



(a) (b)

Figure 2.9: Analytical expressions for total gate capacitance and the silicon and C_{ox} capacitance.

2.9 for an P-type MOS with Boron doping with concentration of $5 \cdot 10^{18}\ cm^{-3}$ considering a Boron doping with $E_a = 0.044\ eV$ at three different temperatures: $-40\ °C$, $27\ °C$ and $175\ °C$ and $\phi_m = 4.1\ eV$

Notice that on the structure two parallel capacitances are present, one from the metal to silicon surface (C_{ox})and another due to the depletion/inversion region created (C_{si}) in such a way that the total capacitance is given by $\left(C_{ox}^{-1} + C_{si}^{-1}\right)^{-1}$. The Silicon capacitance can be obtained by differentiating the silicon charge $Q_s\left(\psi_s\right)$ in respect to the surface potential $\left(dQ_s\left(\psi_s\right)/d\psi_s\right)$. The total gate capacitance and the silicon and C_{ox} capacitances are presented on Fig. 2.9.

Notice that at deep accumulation and inversion the total capacitance is almost equal to C_{ox}. Physically, in accumulation and inversion, the carrier concentration is high making the semiconductor behave like a metal at surface. Besides, the two highlighted bias points present a capacitance value that are temperature independent, those bias points will be explored in the proposal of this thesis

2.3.1 Carriers Transport on MOSFETs

As explained before, when a potential difference is applied between the drain and source, the mobile charges on the channel will flow due to a concentration gradient (diffusion) and the generated electric field (drift). The drift-diffusion model encapsulates this behavior as [see more details in Appendix.C]:

$$J_n = q\mu_n \left(n(x)\xi(x) + \phi_T \frac{dn}{dx} \right) \tag{2.13}$$

$$J_p = q\mu_p \left(p(x)\xi(x) + \phi_T \frac{dp}{dx} \right) \tag{2.14}$$

where J_n and J_p are the current density for electrons and holes; μ_n and μ_p the electrons and holes mobility; and ξ the electric field on the x direction. The mobility parameter characterizes how fast a carrier can move when pulled by an electric field. When passing through the channel, carriers will be deflected by the lattice, in bulk Silicon, there are 3 major scattering mechanisms: Coulomb Scattering, Phonon Scattering and Surface Roughtnes Scattering.

At low temperatures and low electric fields, carriers will be scattered by the coulombic potential of the lattice. When temperature is higher, the lattice vibrations increase and phonon (mechanical vibrations quanta) scattering becomes more frequent. At higher electric fields, another scattering takes place, in this condition most carriers will be present at the rough silicon-oxide interface, and surface roughness scattering will be more present. Besides at high enough electric fields scattering events will become much more frequent and an increased electric field mobility will not increase carriers velocity and the mobility will be saturated.

To model those effects, Caughey and Thomas [42] proposed a local doping an temperature low-field mobility tuned from 77K to 450K as

$$\mu_{n0} = \mu_1 \left(\frac{T}{T_0} \right)^{\alpha} + \frac{\mu_2 \cdot \left(\frac{T}{T_0} \right)^{\beta} - \mu_1 \left(\frac{T}{T_0} \right)^{\alpha}}{1 + \left(\frac{T}{T_0} \right)^{\gamma} \cdot \left(\frac{N}{N_{crit}} \right)^{\delta}}, \tag{2.15}$$

with mobility saturation defined by

$$\mu = \frac{1}{\left(1 + \left(\frac{\mu_0 \xi}{V_{sat}} \right)^{\beta} \right)^{\frac{1}{\beta}}}, \tag{2.16}$$

$$V_{sat} = \frac{v_\alpha}{1 + v_\theta \cdot e^{\frac{T}{T_0}}}. \tag{2.17}$$

The parameters used for the silicon are given by [42] are shown on Tab. 2.1 The local mobility behaviour with doping, temperature, and bias are illustrated in Fig. 2.10, the calculations where done with the Caughey Thomas Mobility mobilty model. In Fig. 2.10(a) one can see that the increase of dopants will make scattering events increase therefore decreasing mobility, on the Fig. 2.10(c) the increase of the potential will increase the electric field and the scattering events, however, at a given temperature, the scattering will be more frequent and mobility will saturate.

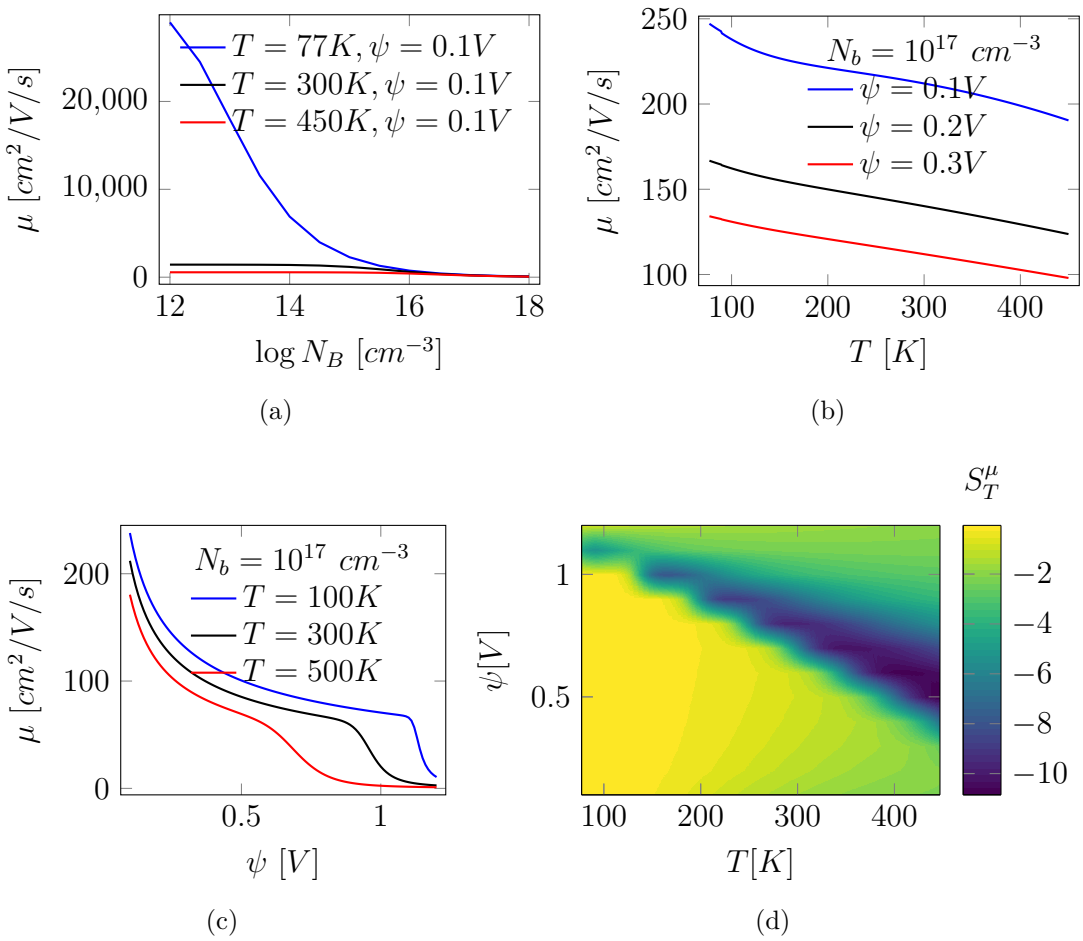


Figure 2.10: Caughey Thomas Mobility mobilty model behavior over temperature, doping concentration and electric potential.

Table 2.1: Default Caughey Thomas Mobility model default parameters used in ATLAS.

	N_{MOS}	P_{MOS}
μ_1	55.24 $cm^2/V/s$	49.7 $cm^2/V/s$
μ_2	1429.23cmˆ2/V/s	479.37cmˆ2/V/S
α	0.0	0.0
β	-2.3	-2.3
γ	-3.8	-3.7
δ	0.73	0.7
N_{crit}	1.072 10^{17} cm^{-3}	1.606 10^{17} cm^{-3}

Figure 2.10(d) shows the temperature sensitivity of the mobility for different doping concentrations and electric potentials. The S_T^{μ} represents the exponential temperature coefficient of the mobility (β in the expression $\mu = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{\beta}$) as it can be seen the mobility exponential temperature coefficient varies widely for different electric potential and consequently different biases.

The use of the drift-diffusion model was able to accurately predict devices behaviors up to 100 nm. However, for small nodes the assumptions made are no longer justifiable. Thus, it is an actual field of research the modeling of mobility for more modern nodes.

In this section, a brief introduction to semiconductor physics focuses on MOSFETs and temperature effects was presented. However, the physics and calculation involved can not be easily handed at circuit level with a considerable amount of transistors. Next chapter will propose an analysis of the major modeling paradigms presented on hand-analysis models and simulation models for MOSFETs used in the industry

2.3.2 MOSFET Models

Similarly presented in the MOS example, the MOSFET presents three operation modes, accumulation, depletion, and inversion. The theory previously developed for the MOS structure can be directly extended to MOSFET by considering the channel potential due to the lateral electric field from source to drain. By considering the source referenced MOSFET ($V_S = 0$ V), due to an external V_{DS} voltage applied, as for the MOS, the energy term on the carriers concentration will include a new potential called the channel potential V_{ch}, such that

$$\begin{cases} V_{ch}\,(x=0) & V_{SB} \\ V_{ch}\,(x=L) & V_{SB}+V_{DS} \end{cases} \tag{2.18}$$

Similar to the MOS structure, the different potentials can be calculated through the Poisson equation; generally, the MOSFET is a 3D structure. Since the external potentials are applied evenly (except for very small transistor widths), we can treat the problem as a 2D structure. Further, by assuming that the gate to bulk electric field variation is greater than the variation on the source to drain direction, we have:

$$\xi_x \ll \xi_y \therefore \frac{\partial^2 \psi}{\partial x^2} \ll \frac{\partial^2 \psi}{\partial y^2} \tag{2.19}$$

Equation (2.19) is usually referred to as the gradual channel approximation (GCA) that allows for solving the MOSFET much like a MOS structure unconsidering the coupling between V_{ch} and ψ and to obtain Q_s making all previously derive equations for the MOS the same by replacing $\psi(y) \rightarrow \psi(y) - V_{ch}(y)$. By taking this approximation, the drain to source current can be obtained by:

$$I_{DS} = \int_{V_{SB}}^{V_{DS}} \mu \cdot W \cdot Q_i(V_{GB}, V_{ch}) \cdot dV_{ch} \tag{2.20}$$

where the μ is the silicon mobility, Q_i the inversion charge per unit area, by using the previously derived charge to potential relation, the equation can be further developed as:

$$I_{DS} = -q\mu_{eff}\frac{W}{L}\int_{V_{SB}}^{V_{DS}}\left[\int_{\psi_B}^{\psi_s}\frac{p(\psi, V_{ch}) - n(\psi, V_{ch})}{\xi(\psi, V_{ch})}d\psi\right]dV_{ch} \tag{2.21}$$

where μ_{eff} is the average channel mobility. Equation (2.21) is known as the Pao-Sah double integral formula and is considered as the reference to transistor models. The equation is usually presented with no holes concentration dependency ($p(\psi, V_{ch})$ since minority carriers concentration is usually way smaller than minority carriers, therefore for a P doped Bulk MOSFET (NMOS) the hole concentration can be neglected and for a N doped MOSFET (PMOS) the electron concentration $n(\psi, V_{ch})/\xi(\psi, V_{ch}) \approx 0$.

Figure 2.11 shows the Pao-Sah Model for a NMOS with acceptors concentration of $5 \cdot 10^{17} cm^{-3}$, oxide thickness of 4 nm and Alluminium gate contact. The integral was approximated using a hcubature with an maximum absolute error estimated at 10^{-19}. Even though the (2.21) is very powerful, the integral must be done numerically, having a computational cost not affordable for computer-aided design (CAD) tools, where possibly millions of transistors must be simulated at for other thousands of time steps. For this matter, some approximations were developed for different transistor compact models. Those approximations and their influence on temperature-related effects will be further investigated in the next sections.

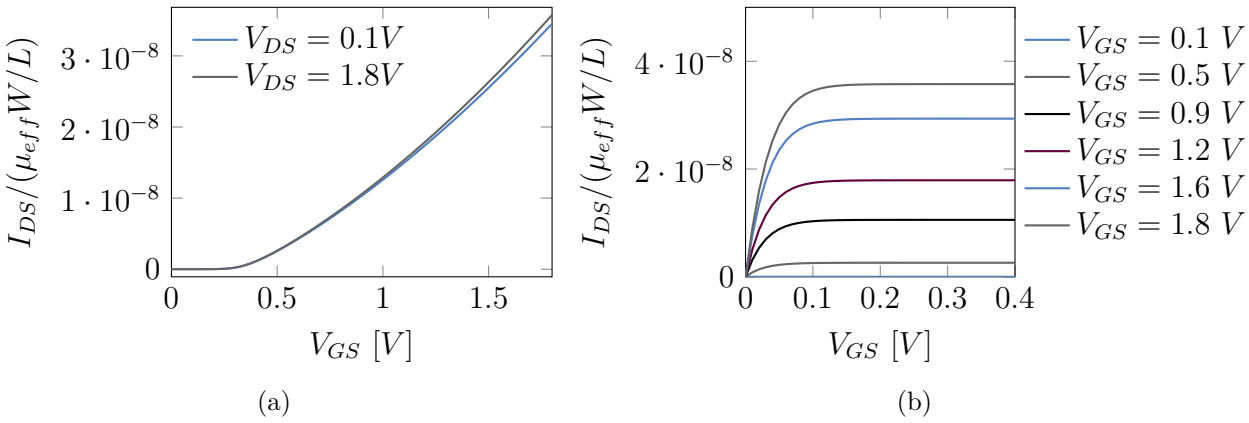


Figure 2.11: Pao-Sah Current model numerical calculations

But first to obtain a complete current model the effective mobility μ_{eff} must be investigated.

2.3.3 The Effective Silicon Mobility

For MOSFET simulations some specific mobility models were developed, where the mobility is only carried for the inversion layer and Matthiesen's rule approximation is usually taken [43] [44]. For an more accurate mobility modelling Monte-Carlo or quantum transport simulations must be carried out [45] [46].

Usual effective mobility temperature dependency modelling considers an exponential temperature dependency. This model is valid under the assumption that one of Si's significant scattering events is predominant. The primary approach to combine different scattering effects is Matthiessen's rule:

$$\frac{1}{\mu_{eff}} = \sum_i \frac{1}{\mu_i}, \tag{2.22}$$

where μ_{eff} is the total effective mobility and μ_i the contribution of each scattering event. However, as pointed out in [45] [see more on Appendix D], Matthiesen's rule is only valid using the Time Relaxation Approximation, assuming Boltzmann statistics, and, more importantly, if the characteristic scattering exponents are the same for the different scattering mechanisms. Although (2.22) is widely used on compact models, from a theoretical point of view the assumptions taken are hardly valid. Typical process design kit, transistor models combine surface phonon scattering and surface roughness using Matthiesen's rule expressed as :

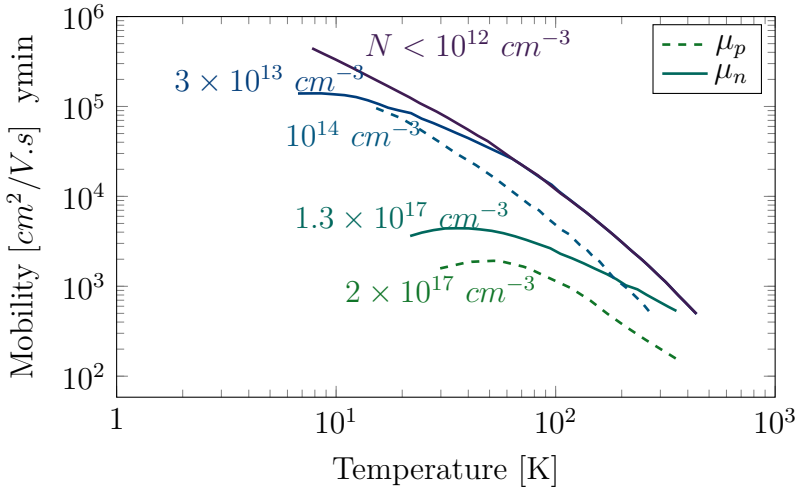


Figure 2.12: Effective Mobility Temperature dependency extracted from measurement data, for holes (μ_p) and electrons (μ_n) for different doping concentrations extracted from [39].

$$\mu_{eff} = \frac{\mu_0}{1 + \left[\left(\theta_{ph} \cdot E_{eff}\right)^{\nu/3} + \left(\theta_{sr} \cdot E_{eff}\right)^{k \cdot \nu} \right]^{1/\nu}} \cdot \left(\frac{T}{T_0}\right)^{-\beta_\mu}, \tag{2.23}$$

where E_{eff} is the effective electric field; θ_{ph}, θ_{sr} are empirical parameters related to phonon scattering and surface roughness; μ_0 is the carrier mobility limited by ionized impurity scattering and acoustic phonon scattering; ν is an empirical parameter that accounts for a statistical averaging of the relaxation times [47]; β_μ is the strong inversion temperature coefficient [6]. This claim can hold either in a short temperature range or at a specific inversion level where a scattering mechanism is dominant.

2.3.4 The Charge Sheet Approximation

One of the first attempts to further simplify the double integral Pao-Sah model was proposed by J.R Brews [48]. Since at inversion the surface potential raises slowly with a gate voltage increase, as discussed in the MOS structure section, and the inversion layer thickness is always smaller than the depletion width, the inner integral on (2.21) varies greatly with a small ψ_s increase. Mathematically this assumption can be expressed as:

$$Q_i = Q_s - Q_d = -C_{ox}\left(V_{GS} - V_{FB} - \psi_s\right) + \sqrt{2\epsilon_{si} N_A \psi_s} \tag{2.24}$$

This simplification, along with the same assumptions made on [40] , allow to solve V_{ch} as a function of ψ_s as:

$$V_{ch} = \psi_s - \phi_T \ln\left\{\frac{N_A}{n_i^2}\left[C_{ox}^2\left(V_{GS} - V_{FB} - \psi_s\right)^2 - \frac{\psi_s}{\phi_T}\right]\right\} \tag{2.25}$$

Allowing to rewrite the double integral as a single one with a change of variable. However, this substitution leads to another single integral with no analytical solution:

$$I_{DS} = \mu\frac{W}{L}\int_{\psi,s,s}^{\psi_{s,d}}\left[C_{ox}\left(V_{GS} - V_{FB} - \psi_s\right) - \sqrt{2\varepsilon_{si}qN_A\psi_s}\right. \tag{2.26}$$

$$\left. + 2\phi_T\frac{C_{ox}^2\left(V_{GS} - V_{FB} - \psi_s\right) + \varepsilon_{si}qN_A}{C_{ox}\left(V_{GS} - V_{FB} - \psi_s\right) - \sqrt{2\varepsilon_{si}qN_A\psi_s}}\right] d\psi_s \tag{2.27}$$

This issue is tackled by Brews by introducing a new approximation, since the second term in (2.27) is multiplied by ϕ_T and therefore is much smaller than the first term it can be neglected, leading to:

$$I_{DS} = \mu\frac{W}{L}\left\{C_{ox}\left(V_{GS} - V_{FB} + \phi_T\right)\psi_s - \frac{1}{2}C_{ox}\psi_s^2 - \frac{2}{3}\sqrt{2\varepsilon_{si}qN_A}\psi_s^{3/2} + \phi_T\sqrt{2\varepsilon_{si}qN_A\psi_s}\right\}\Bigg|_{\psi_{s,s}}^{\psi_{s,d}} \tag{2.28}$$

The Brews Charge sheet approximation presents an analytical approximation for the Pao-Sah model. However, the surface potential at the source and drain sides still need to be calculated numerically. Many solutions for the calculation appeared in literature; however, using such a model is not possible for hand calculations. For this matter, a piece-wise approach was developed to simplify the hand analysis of transistor circuits.

Regional Approximations of the Charge Sheet Model

On the onset inversion, however far from current saturation, the surface potential can be approximated by $\psi_s \approx 2(E_i - E_F) + V_{ch}(y)$ as shown in fig 2.13 for a NMOS transistor with $N_A = 5 \cdot 10^{17}\ cm^{-3}$ and $t_{ox} = 4\ nm$

By using this approximation $\psi_{s,s} = 2\phi_B = 2(E_i - E_F)$ and $\psi_{s,d} = 2\phi_B + V_{DS}$, and the MOSFET current can be expressed as:

$$I_{DS} = \mu_{eff}C_{ox}\frac{W}{L}\left\{\left(V_{GS} - V_{FB} - 2\phi_B - \frac{V_{DS}}{2}\right)V_{DS} - \right. \tag{2.29}$$

$$\left.\frac{2\sqrt{2\varepsilon_{si}qN_A}}{3C_{ox}}\left[\left(2\phi_B + V_{DS}\right)^{3/2} - \left(2\phi_B\right)^{3/2}\right]\right\} \tag{2.30}$$

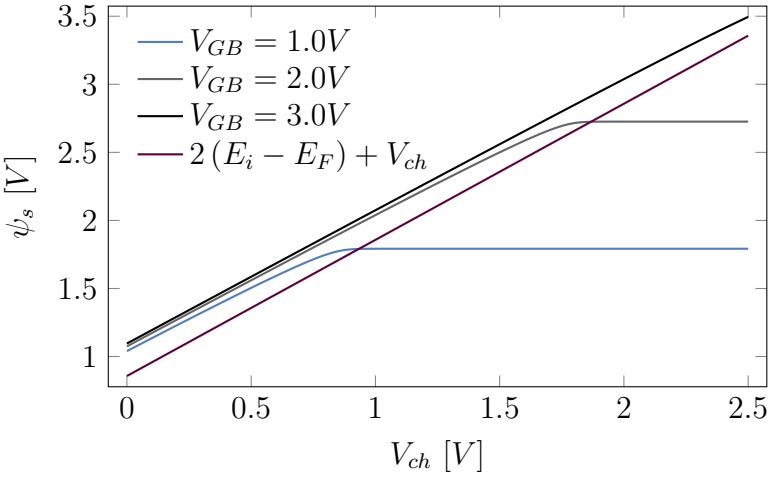


Figure 2.13: Brews approximation for the the surface potential as a function of V_{ch} and V_{GB}.

In the $\psi_s$linear region the current can be approximated by the first order McLaurent expansion of (2.30) of V_{DS}:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS}, \tag{2.31}$$

$$V_{th} = V_{FB} + 2\phi_B + \frac{\sqrt{4\varepsilon_{si} q N_A \phi_B}}{C_{ox}}, \tag{2.32}$$

where V_{th} is the threshold voltage. Physically the threshold voltage can be defined as the gate to bulk voltage in which $\psi_s = 2\phi_B$ and that the bulk depletion charge is equal to the total silicon charge. For higher V_{DS} ($V_{DS} > V_{th}$) the second order terms on (2.30) become important, however as seen in Fig. 2.13 for higher V_{ch} is pinned to $2\phi_B$ that corresponds to $V_{DS} = V_{GS} - V_{th}$ making the saturated current:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{2L} (V_{GS} - V_{th})^2 \tag{2.33}$$

2.3.5 V_{th} Temperature effects

The threshold voltage is a key parameter for large transistors. When considering the series expansions of the Brews models, the only two parameters that have a temperature dependency are the effective mobility μ_{eff} and the threshold voltage. Differently from the mobility, the threshold voltage comes from an electrostatic formulation, and therefore an analytical temperature coefficient can be obtained.

From (2.32) the only two parameters that have temperature dependency are the flat band voltage and the bulk poteintial voltage ϕ_b.

V_{FB} Temperature Variation

The flat band is defined as $V_{FB} = \phi_m - \chi_{Si} - E_{C_{Si}} - E_{F_{Si}}$ in this definition the metal work-function and semiconductor vacuum energy posses very little temperature dependency [49]. For the silicon Conduction Band and Fermi-level difference, temperature dependency will be a function of the body dopping N_B. By assuming Boltzmann-Statistics:

$$E_C - E_F = \phi_T \ln\left(\frac{N_C}{n_0}\right) \tag{2.34}$$

where n_0 is the equilibrium electron concentration and N_C is the effective density of states at the conduction band. Figure 2.14 shows the temperature derivative of V_{FB} in mV/K for different doping profiles and temperatures using Fermi distribution and non-ionized acceptors with $E_a = 0.044eV$. Modern transistors present high bulk dopping and therefore very little V_{FB} temperature dependency.

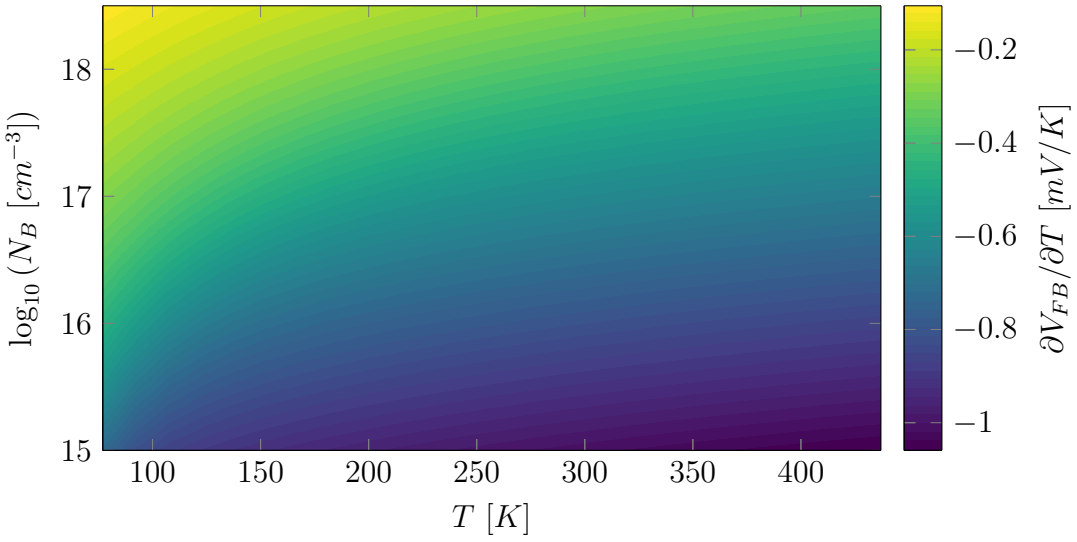


Figure 2.14: V_{FB} temperature coefficient of in mV/K for different doping profiles and temperatures using Fermi distribution and non-ionized acceptors with $E_a = 0.044eV$ and aluminum gate contact.

For an NMOS transistor, the equilibrium electron concentration can be approximated by $n_0 \approx n_i^2/N_A$, while for an PMOS $n_0 \approx N_D$ by using this approximation the flatband voltage temperature dependency can be expressed by:

$$\frac{\partial V_{FB}}{\partial T} = \begin{cases} \frac{1}{2}\frac{k_B}{n_i(T)q}\left(2\ln\left(\frac{N_v(T_0)TN_A}{T_0(ni(T))^2}\sqrt{\frac{T}{T_0}}\right)ni\,(T) + 3\,ni\,(T) - 4\left(\frac{\mathrm{d}}{\mathrm{d}T}n_i\,(T)\right)T\right) & \text{NMOS} \\ \frac{1}{2}\frac{k_B}{q}\left(2\ln\left(\frac{N_V(T_0)T}{T_0N_D}\sqrt{\frac{T}{T_0}}\right)+3\right) & \text{PMOS} \end{cases} \tag{2.35}$$

ϕ_B Temperature Dependency

The flat band is defined as $\phi_B = E_i - E_f$, by considering that E_i is at the middle of the bandgap and assuming Boltzmann statistics:

$$\phi_B = \phi_T \ln\left(\frac{N_A}{n_i}\right) \tag{2.36}$$

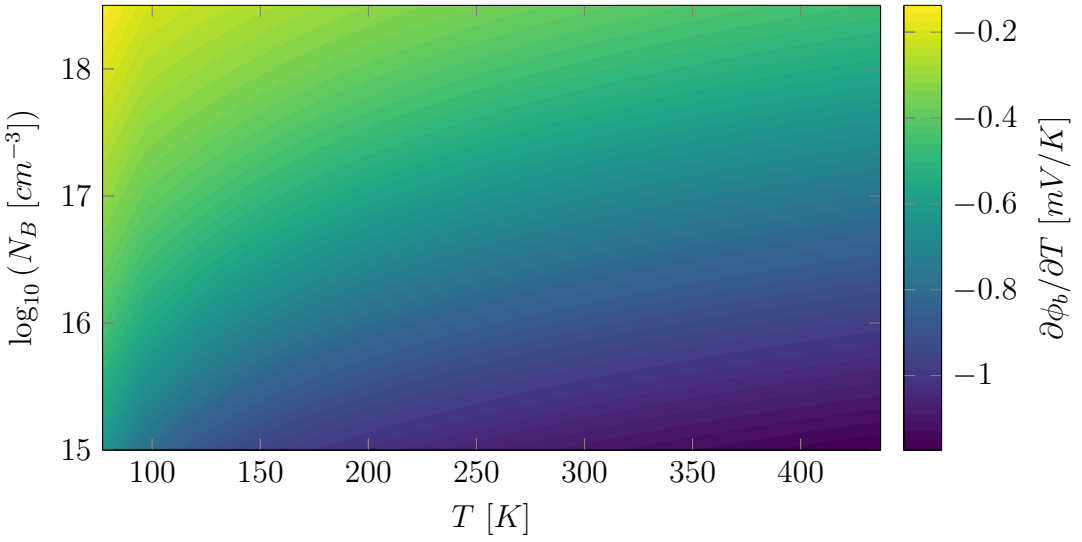
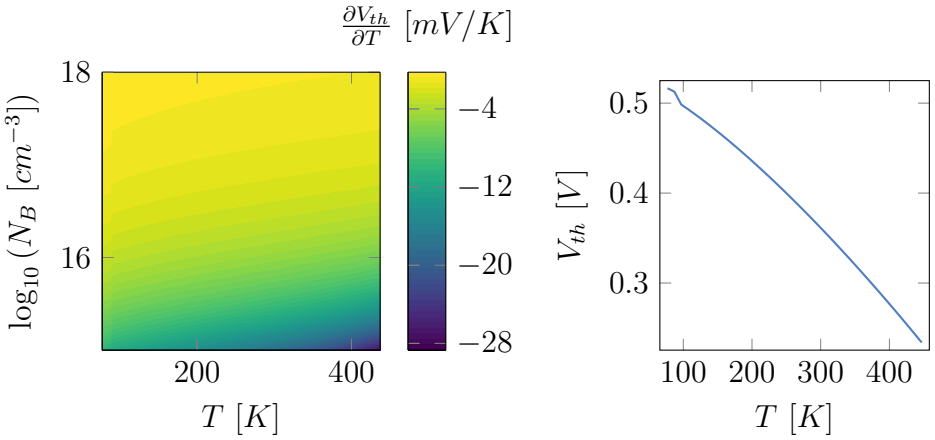


Figure 2.15: Bulk potential temperature coefficient at different temperatures and doping concentrations.

Figure 2.15 shows the temperature coefficient for the bulk potential over different doping concentrations and temperatures; it is noticeable that the bulk potential possesses an opposite temperature relation to the flat band voltage. Those two temperature relations recombine to compose the threshold voltage temperature dependency. However, for the threshold voltage temperature dependency, the oxide thickness plays also a role in the γ factor by using Dennard's scaling rule and using a base transistor with $(N_B = 5 \cdot 10^{17} cm^{-3}, t_{ox} = 4\ nm)$

Figure 2.16 shows the V_{th} temperature coefficient in mV/K and a plot of V_{th} for a $N_B = 5 \cdot 10^{18} cm^{-3}, t_{ox} = 4\ nm$ transistor using Fermi-Distribution. It



(a) (b)

Figure 2.16: Threshold voltage temperature coefficient at different temperatures and doping concentrations, and threshold voltage temperature behavior for a $N_B = 5 \cdot 10^{18} cm^{-3}, t_{ox} = 4\ nm$ transistor.

is noticeable that V_{th} presents almost linear behavior with temperature with a negative temperature coefficient for a very large temperature range. The threshold voltage temperature coefficient is usually represented by α_{th}, and the $V_{th}(T)$ is given by

$$V_{th}(T) = V_{th_0} - \alpha_{th} \cdot T. \tag{2.37}$$

2.3.6 Current ZTC Point

While considering the threshold voltage and mobility temperature dependency, Giralt *et al.* proposed the first analytical bias condition for achieving a temperature stable I_{DS} current. Those bias points in which a given transistor parameter does not change with temperature this point is commonly referred as the zero temperature coefficient (ZTC) bias point.

The analytical condition of the ZTC condition was studied in a long transistors using the quadratic model in [50]:

$$V_{GS} - V_{th} = \frac{V_{th} + \phi_B}{2} \left[\frac{1}{T} - \frac{\partial n_i}{\partial T} \frac{1}{n_i \cdot \ln\left(\frac{N_D}{n_i}\right)} \right] - \frac{\partial \mu_{eff}}{\partial T} \frac{1}{2 \cdot \mu_{eff}} \tag{2.38}$$

This ZTC point have even been used to achieve temperature-aware designs in analog and digital electronics [24], [25]. Figure 2.17 illustrates de $I_{D_{ZTC}}$ found

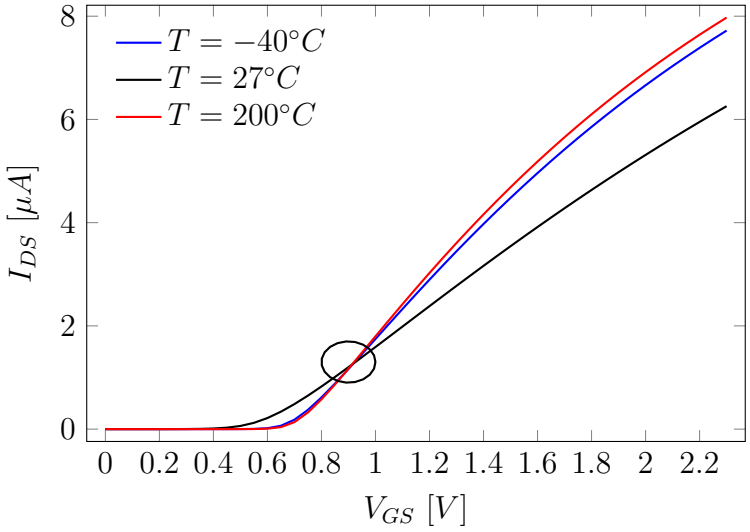


Figure 2.17: Drain do source current of a PMOS transistor calculated numerically at different temperatures using Pao-Sah model.

using the Pao-Sah model with CVT mobility model, $5 \cdot 10^{16} cm^{-3}$ P-type bulk doping, 4 nm oxide thickness and Aluminium Gate. The same ZTC is found on the measurement data for a transistor with similar parameters here illustrated on Fig. 2.18.

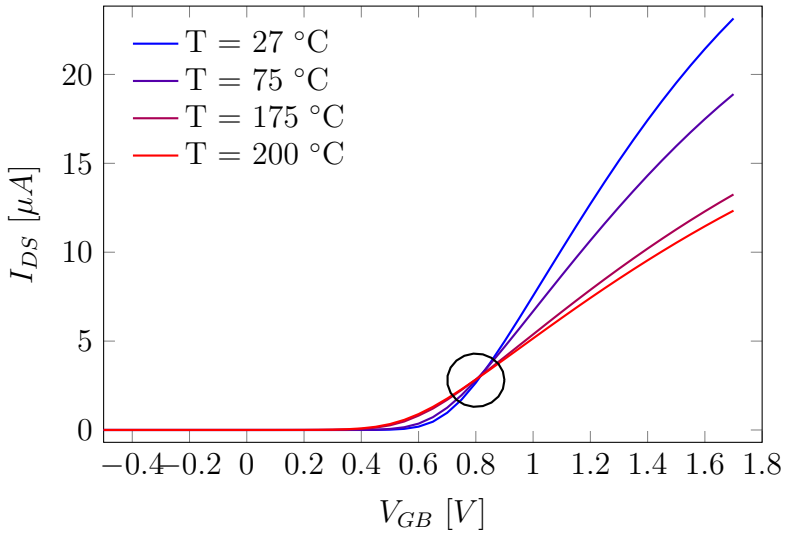


Figure 2.18: Measured Drain do source current of a PMOS transistor at different temperatures.

2.3.7 Small Channel Effects in Analog Design

In the previous sections, a transistor model was developed base on some assumptions e.g the electric field on the longitudinal (Drain to Source) is small, that the channel is sufficiently long such as "edge" effects could be neglected and so an one-dimensional analysis could be done.

In real devices, specially more recent technological nodes, those assumptions break down and some important effects appear that had not been previously described. Some of effects have a deep impact on the analog design and must be considered in a temperature-aware framework. Following subsections will consider this effects an comment on their temperature drift effects.

Velocity Saturation

When transistor lengths gets smaller the longitudinal electric field gets bigger for the same V_{DS} applied, with the increased electric field mobility saturates, virtually creating a depletion area and reducing the effective transport length.

Figure 2.19 shows the longitudinal electric field of two NMOS with bulk dopping of $5.7 \cdot 10^{17}\ cm^{-3}$, a source/drain dopping of $6 \cdot 10^{1}6\ cm^{-3}$ with an Aluminium gate and a gate oxide of 4 nm at two different gate lengths ($0.54\ \mu m, 2.0\ \mu m$) with an lattice temperature of 300 Kat a 0.9 nm distance from the silicon-oxide interface The small transistor presents an longitudinal electric field up to 7 orders of magnitude higher than the long transistor.

The simulation is done numerically using a finite volume method with 5151 grid points, no recombination and generation phenomena with Shaffered-Gummel flux using the developed MOSLab package [34]. The mobility considering electric field is usually modeled by

$$\mu = \frac{\mu_0}{\left(1 + \left(\frac{\xi_x \cdot \mu_0}{V_{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \tag{2.39}$$

where V_{sat} is a temperature dependent parameter that represents the saturated velocity and β a fitting parameter that goes from 1 to 3, and are usually close to 1 for holes and close to 2 for electrons. The V_{sat} temperature and doping dependency is given by Swarts [51]

$$V_{sat}\,(T) = \frac{\alpha}{1 + \theta \cdot e^{\frac{T}{T_0}}} \tag{2.40}$$

The usual parameters for α, θ at $T_0 = 600K$ are $2.4 \cdot 10^7\ cm/s$ and 0.8 respectively. Figure 2.20 shows the temperature behavior of the saturation velocity and the saturated mobility. The mobility temperature behavior is taken as

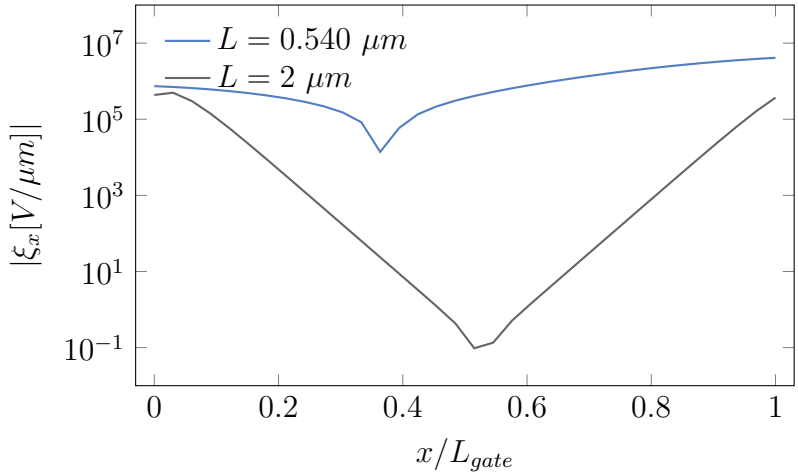


Figure 2.19: Longitudinal electric field calculated numerically [43] using a finite volume method whit 5151 grid points, no recombination and generation phenomena with Shaffered-Gummel flux, of two NMOS with bulk dopping of $5.7{\cdot}10^{17}\ cm^{-3}$, a source/drain dopping of $6 \cdot 10^16\ cm^{-3}$ with an Alluminum gate and a gate oxide of 4 nm at two different gate lengths ($0.54\ \mu m, 2.0\ \mu m$) with an lattice temperature of 300 Kat a 0.9 nm distance from the silicon-oxide interface.

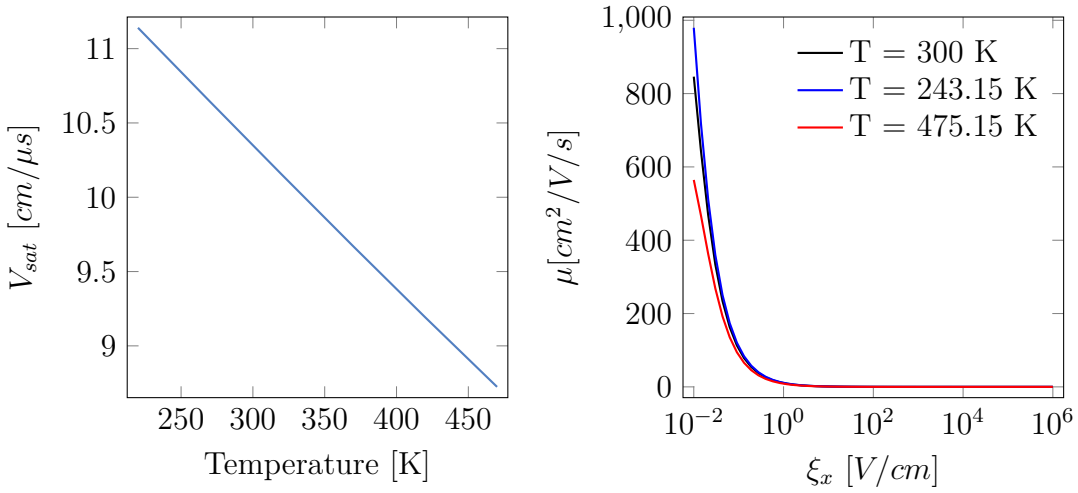


Figure 2.20: Temperature behavior of the saturation velocity and the saturated mobility given by the Swarts Model.

$\mu(T) = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{-1.5}$ (predominant Surface Roughness Scattering mobility behavior) with a low-field mobility at room temperature of 1470 $cm^2/V/s$. The saturated velocity temperature behavior have an approximate linear behavior, over a large

temperature range, however when considering the mobility model temperature has small effect on the saturated mobility value.

Channel Length Modulation (CLM)

When the drain to source voltage exceeds V_{Dsat} (V_{DS} voltage in which the current starts to become saturated), the pinch-off region starts to grow towards the source, making the effective channel length smaller with the increase of V_{DS}. Classically the CLM effect for long channel effects is incorporated in the quadratic saturated current function by:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{2L} \left(V_{GS} - V_{th}\right)^2 \left(1 + \lambda V_{DS}\right) \tag{2.41}$$

$$\lambda = \frac{\Delta L}{L} \tag{2.42}$$

The modeling of CLM of long channel MOSFETs inherits from the Early effect on the bipolar transistor that have approximately the same effects on the collector current as the MOSFET CLM effect. The relative channel length shortening is related to the Early voltage by $\lambda = \frac{1}{V_{Early}}$.

In short channel transistors, the current saturation may occur in a smaller voltage then the classical $V_{Dsat} = V_{GS} - V_{th}$ due to the velocity saturation. Besides, the short channel V_{Dsat} is dependent on the longitudinal electric field and not on V_{GS}. Thus, the MOSFET saturation current increases linearly with V_{GS} rather than quadratically as in the long transistor.

$$I_{DS_{sat}} = \mu_{eff} C_{ox} \frac{W}{L} \left\{ \left(V_{GS} - V_{th} - \frac{V_{Dsat}}{2} \right) V_{Dsat} \right\} \tag{2.43}$$

Figure 2.21 shows the measured current characteristics of a $220 \times 180\ nm^2$ NMOS transistor and its comparison with the quadratic model. For high V_{DS}, the quadratic model predicts saturation current proportional to V_{GS}^2. When comparing to measurement data from small transistors it over estimates the real saturation current, that occurs earlier V_{GS} bias. Besides, the quadratic model without CLM predicts a constant I_{DS} current, independent of V_{DS} where in the measurement data I_{DS} increases slowly with V_{DS}.

Drain Induced Barrier Lowering (DIBL)

As seen before the carriers current density can be expressed in terms of the spatial variation of V_{ch} (the quasi-Fermi-Level). When considering a long NMOS transistor the electrons have to overcome a barrier created between source and bulk

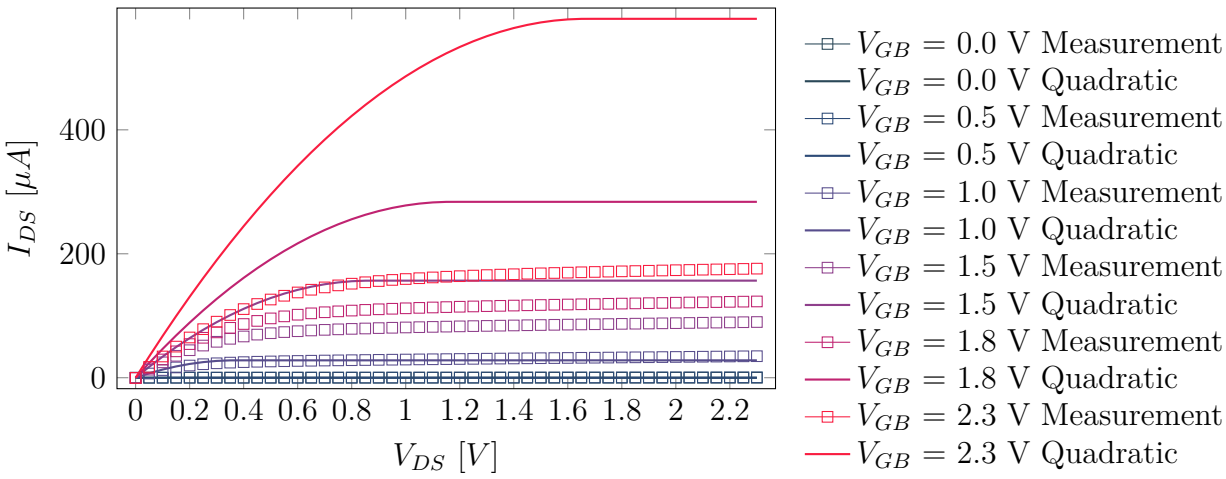


Figure 2.21: Comparison between the quadratic model drain current and measurement data of a NMOS transistor.

$(E_{F_B} - E_{F_S})$ to then conduct to the drain. However, when the channel gets smaller the lowering of the drain potential affects the source side of the channel potential, lowering the source to bulk barrier when compared to the long channel case.

Figure 2.22 shows the conduction band difference in relation to the source E_C at the same depth and condition as in Fig. 2.19. In the long channel transistor the conduction band presents constant values at the middle of the source $(-1.0 < x/(L_{gate}) < 0.0)$; gate $(0.0 < x/(L_{gate}) < 1.0)$; and drain $(1.0 < x/(L_{gate}) < 2.0)$ allowing to separate the source-bulk interaction and the bulk-drain one. However, the on the short channel transistor this separation can no longer be considered and the maximum E_C value is not reached in the bulk.

In threshold based models, the incorporation of the DIBL effect is done by making V_{th} a function of the source to drain voltage and the channel length. The usual approach comes from empirical formulas to describe the effect [52]:

$$V_{TH}\left(V_{DS}, L\right) = V_{th}(0, L) - \sigma\left(L\right) \tag{2.44}$$

$$\sigma\left(L\right) = \frac{\left(\beta_4 + \beta_5 \cdot V_{SB}\right)}{L^{\beta_6}} \tag{2.45}$$

where σ is the DIBL coefficient; V_{SB} the source to bulk voltage; and β_4,β_5,β_6 are fitting parameters

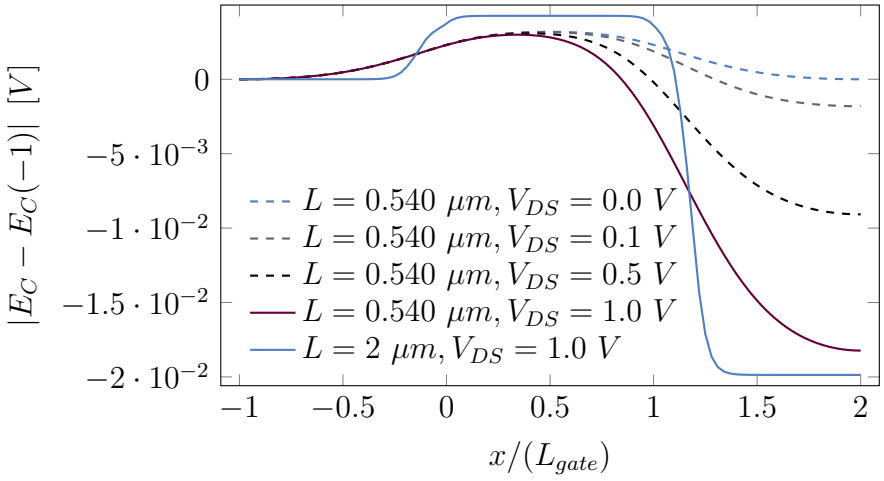


Figure 2.22: Electric potential from source to drain calculated numerically using a finite volume method with 5151 grid points, no recombination and generation phenomena with Shaffered-Gummel flux, of two NMOS with bulk dopping of $5.7 \cdot 10^{17}\ cm^{-3}$, a source/drain dopping of $6 \cdot 10^{1}6\ cm^{-3}$ with an Alluminum gate and a gate oxide of 4 nm at two different gate lenghts ($0.54\ \mu m, 2.0\ \mu m$) with an lattice temperature of 300 Kat a 0.9 nm distance from the silicon-oxide interface.

2.4 Transistor Compact Models

The small-channel effects make the transistors compact model more complicated and do not allow. Modern transistor compact models for simulation have hundreds of parameters to account for various effects, such as temperature variation, small geometries effects, and stress effects. Besides, incorporating such effects must be donne carefully to avoid model discontinuities that may lead to erroneous simulation results [53].

For this matter most modern transistor compact models take another approach to compact transistor modeling in small nodes. In this section the two main approaches will be discussed (Symmetric Linearisation and Charge Linearization) and the main simulation and hand-analysis models will be developed.

2.4.1 Symmetric Linearization Models

Symmetric Linearisation models rely on a numerical fast algorithm to calculate the surface potential at the drain and bulk sides. By defining q_b as the normalized bulk charge to the oxide capacitance per unit area (C_{ox}) and q_i the C_{ox} normalized inversion charge, by charge neutrality:

$$q_i = -(V_{GB} - V_{FB} - \psi_s) - q_b \tag{2.46}$$

By defining since deep in the bulk no inversion charge is present q_b can be taken as the approximated depletion charge:

$$q_b = -\text{sign}\left(\psi_s\right)\gamma\sqrt{\psi_s - \phi_T\left[1 - e^{-\frac{\psi_s}{\phi_T}}\right]} \approx -\gamma\sqrt{\psi_s - \phi_T}; \psi_s > 3\phi_T \tag{2.47}$$

The main approximation taken by symmetric linearizations models is that the normalized channel inversion charge can be expressed as a function of the inversion charge at the point in which the surface potential is equal to the mean of the ψ_s at the source and the drain. By using this assumption, on the charge sheet model, the drain to source current can be obtained by [See more on Appendix E]

$$I_{DS} = \mu_{eff}\frac{W}{L}C_{ox}\left(-q_{im} + \alpha\phi_T\right)\left(\psi_{sD} - \psi_{sS}\right), \tag{2.48}$$

where ψ_{sD} and ψ_{sS} are the surface potential at the drain and source sides; α the linearization factor; and q_{im} the inversion charge at the mean surface potential. To calculate the drain current the surface potentials on the source and drain needs to be calculated, to solve this problem symmetric linearisation compact models such as the PSP model proposes an fast but accurate algorithm to solve the surface potential equation.

The algorithm presented on [54] is the first non-iterative solution for ψ_s that presents an maximum absolute on the order of nano Volts for the surface potential when considering only majority carriers contributions, Boltzmann distribution and complete ionization. Figure 2.23 shows the comparison of the PSP surface potential calculation with numerical results using Fermi-Dirac distribution, including minority carriers contributions and incomplete ionization with an reduced ionization energy of 0.044 eV for a transistor with Boron dopping concentration of $5 \cdot 10^{17}$ cm^{-3} and oxide thickness of 4 nm. At low temperatures the incomplete ionization reduces the surface potential since the effective doping is smaller than the impurities concentration, when the bias has an higher absolute value the Boltzmann approximation is less accurate and the surface potential is smaller than the numerical results. The maximum absolute error of the PSP approximation for different impurity concentrations and temperatures with an oxide thickness of 4 nm is here shown on the Fig. 2.23 an present an error in the order of mV.

Figure 2.24 shows the complete PSP model for various biasing and temperatures for the same NMOS transistor as illustrated in Fig. 2.23. Notice that the same I_{DS} ZTC point presented on the Pao-Sah model is also presented on the PSP model.

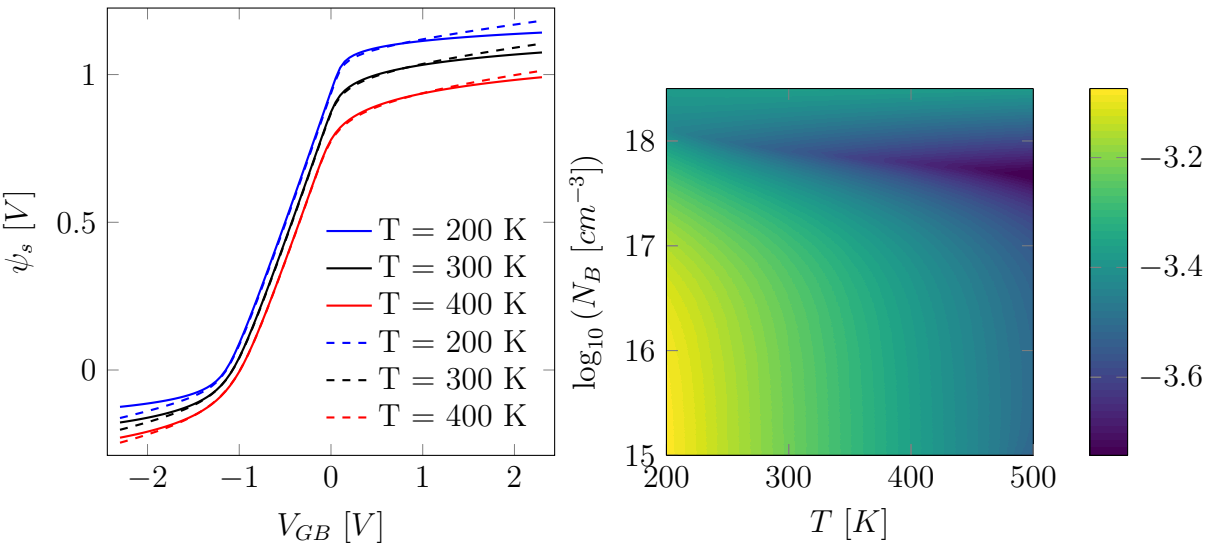


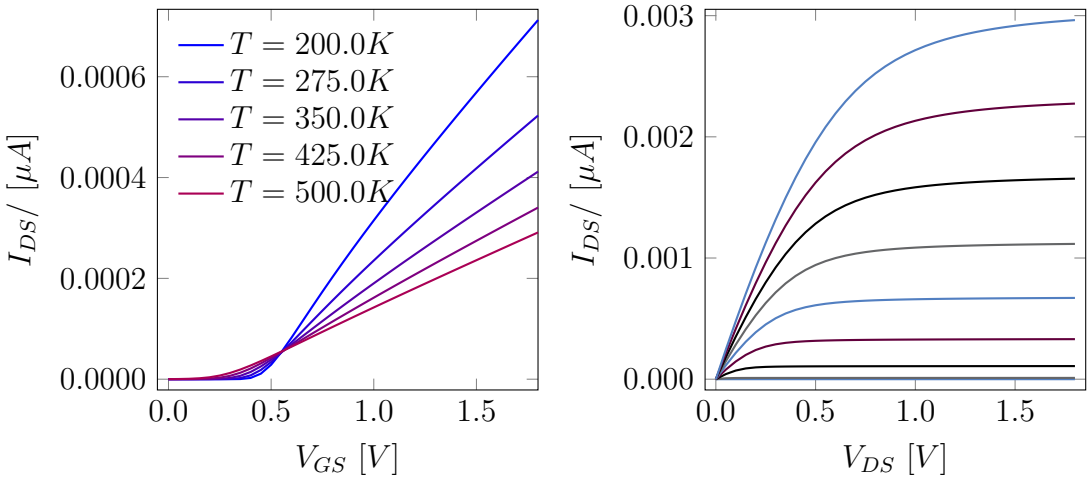
Figure 2.23: Comparison between PSP approximation for the surface potential (solid) and numerical results considering Fermi-Dirac distribution (dashed) and maximum absolute error on the approximation for different temperatures and doping levels.

Temperature Effects

Figure 2.23 highlights two main temperature effects on the $\psi_s \times V_{GB}$ characteristics, an horizontal shift and a surface potential reduction with the temperature increase. The horizontal shift is a consequence of the flat-band voltage temperature drift that was addressed on Chap. 2. However, in new CMOS nodes the gate contact is done using highly doped polycrystalline silicon (Poly). The replacement of the gate contact material affects the temperature behaviour of V_{FB}, Fig. 2.25 shows the V_{FB} temperature coefficient for the same MOS structure as in Fig. 2.23 with a Aluminum contact, and with a Poly Contact. The Poly contact MOS structure presents a lower temperature coefficient in this case 4.5 to 3.2 times smaller than the metal contact.

In order to evaluate the temperature behaviour of the surface potential and the current, the concept of the temperature sensitivity needs to be introduced. The temperature sensitivity of a parameter $y(T)$, defined as $S_T^{y(T)}$ is defined as the percentual change of the $y(T)$ when T is changed by 1.0 or mathematically:

$$S_T^{y(T)} = \lim_{\Delta T \to 0} \frac{\frac{y(T+\Delta T)-y(T)}{y(T)}}{\frac{\Delta T}{T}} = \frac{T}{y\,(T)} \frac{\partial y\,(T)}{\partial T} \tag{2.49}$$



(a) (b)

Figure 2.24: $I_D \times V_{GB}$ Characteristics of long channel MOSFET calculated using the PSP model.

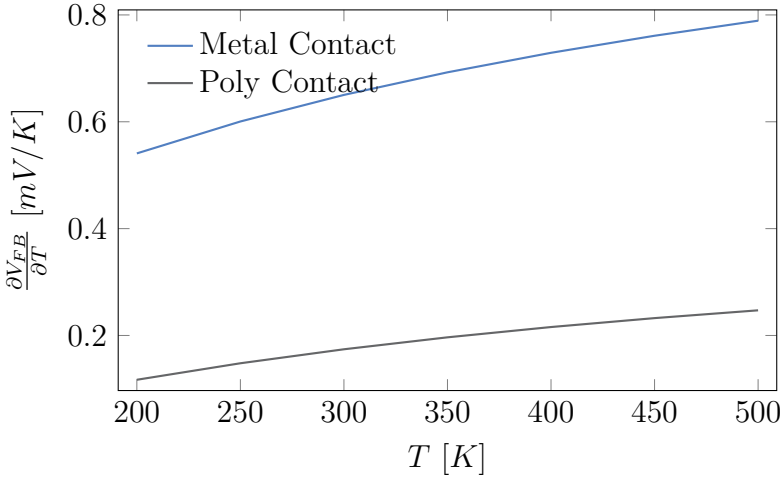


Figure 2.25: Comparison of flat-band temperature coefficient theoretical calculations when using a metal gate contact and Poly gate contact.

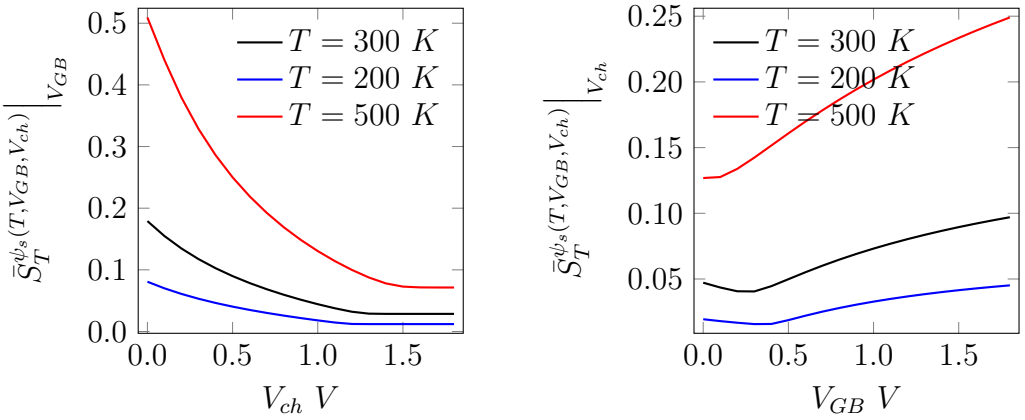


Figure 2.26: Mean Temperature Sensitivity of the surface potential by averaging on the V_{GB} voltage and the V_{ch} voltage.

And the mean temperature sensitivity of $y(T,p)$ over $p \in [p_0, p_1]$ defined as:

$$\bar{S}_T^{y(T,p)}\Big|_p = \frac{1}{p_1 - p_0} \int_{p_0}^{p_1} \left| S_T^{y(T,p)} \right| dp \tag{2.50}$$

Since temperature sensitivities defined as in (2.49) and (2.50) are dimensionless quantities the temperature sensitivity of parameters having different units can be compared. The mean temperature sensitivity of the ψ_s PSP calculation of ψ_s in relation to V_{GB} and V_{ch} from 0 to 1.8 V are here shown in Fig. 2.26

The mean sensitivities are here shown for a transistor with body doping density of $5 \cdot 10^{17}\ cm^{-3}$ an oxide thickness of 4 nm and a Poly gate. The derivatives for ψ_s to temperature are calculated using automatic differentiation and the integral using Gaussian adaptive Gauss-Kronrod quadrature [55]. It is visible that the ψ_s sensitivity presents a minimum for a V_{GB} smaller than 0.5 V and around 0.4 V at 300 K and for higher V_{ch} the temperature sensitivity is smaller.

The same analysis can be done on the drain current considering a three terminal MOSFET (Bulk and source connected) and averaging by V_{GB} and V_{DS}. The mean temperature sensitivity of I_{DS} on the PSP model for the same transistor as in Fig. 2.26 is here shown on Fig. 2.27.

As discussed before the mobility temperature behavior is complex and influenced by many parameters, such as the channel charge concentration, longitudinal and transverse electric fields and temperature and becomes a difficult task to designers to consider all those parameters for the transistors on the circuit. For this matter, one may define a normalized drain current as $I_{D0} = I_{DS}/(\mu_{eff} \cdot W/L)$. By using this definition the mean temperature sensitivity can then be calculated:

Figure 2.28 shows the mean temperature sensitivity(MTS) of I_{D0}, it is notice-

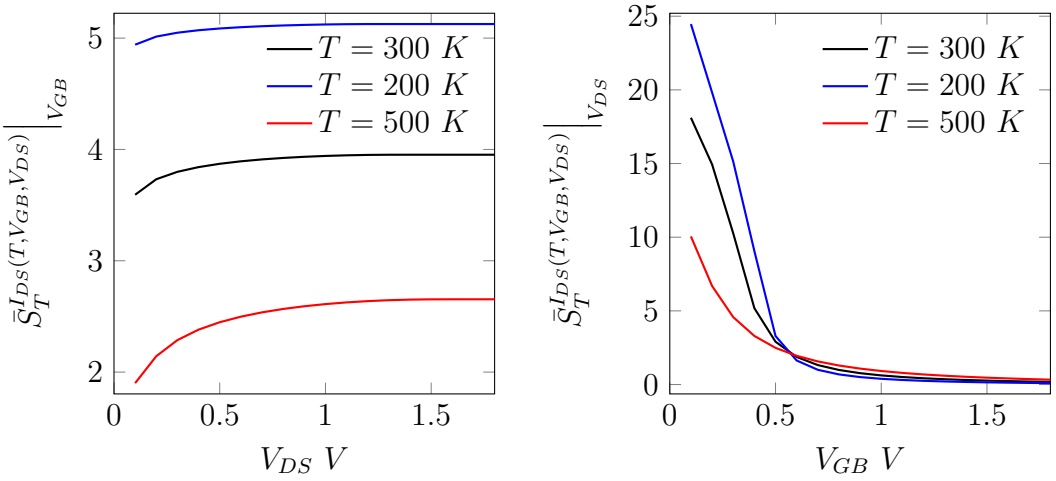


Figure 2.27: Drain to source current mean temperature sensitivities by averaging on the V_{GB} voltage and the V_{DS} voltage.

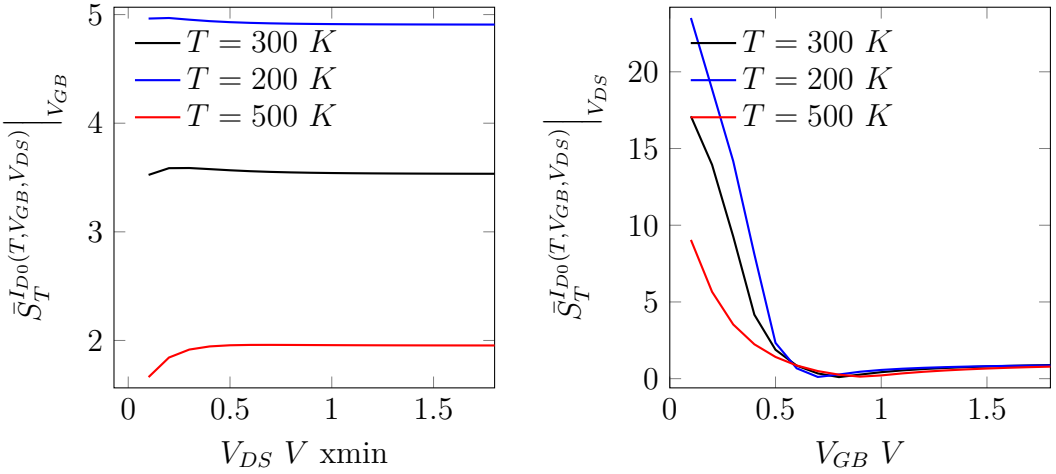


Figure 2.28: Mean Temperature Sensitivity of the drain current when considering (first row) and not considering mobility temperature dependency by averaging on the V_{GB} voltage and the V_{DS} voltage.

able that both MTS from I_{DS} and I_{D0} possesses the same overall behavior. At higher V_{DS} the MTS in relation to V_{GB} present an almost constant value, the MTS in relation to V_{DS} presents a decreasing behaviour with a constant value under temperature (ZTC point) for $V_{GB} \approx 0.55\ V$. This similarity can be explained by the averaging of the mobility temperature effects under the bias conditions.

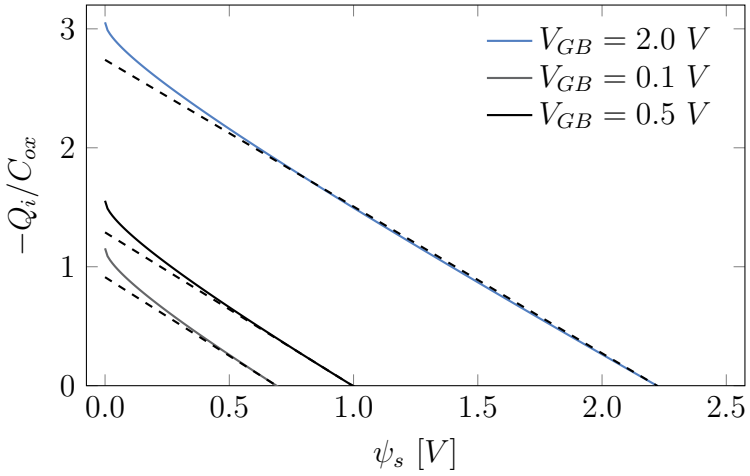


Figure 2.29: Theoretical inversion charge given by (2.52) (solid lines) charge linearization approximation (dashed lines) for different gate to bulk voltages.

2.4.2 Inversion Charge Linearization Based Models

The charge sheet modeling approach uses an implicit variable $\psi_s(V_G, V_S, V_D)$ to define transistor properties continuously. However, using ψ_s to calculate the inversion charge needed for the Pao-Sah formulation does not represent any helpful concept for the design, where more global properties such as charges, currents, transcapacitances, and transconductances are key.

The Brews charge approximation (2.24) can be rewritten in terms of the ψ_s as:

$$V_{GB} - V_{FB} = \psi_s + \gamma\sqrt{\psi_s} - \frac{Q_i}{C_{ox}} \tag{2.51}$$

$$Q_i = -\gamma C_{ox}\sqrt{\phi_T}\left[\sqrt{\frac{\psi_s}{\phi_T} + e^{\frac{\psi_s - 2\phi_B - V_{ch}}{\phi_T}}} - \sqrt{\frac{\psi_s}{\phi_T}}\right] \tag{2.52}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \tag{2.53}$$

The inversion charge variation is almost linear when the gate to bulk voltage is kept constant, as shown in Fig. 2.29 for a 15 nm oxide thickness, $5 \cdot 10^{16}\ cm^{-3}$ acceptor concentration at 300 K.

By defining the pinch-off surface potential as the surface potential at wich $Q_i = 0$, one may find:

$$\psi_p = V_{GB} - V_{FB} - \gamma^2\left(\sqrt{\frac{V_{GB} - V_{FB}}{\gamma^2} + \frac{1}{4}} - \frac{1}{2}\right) \tag{2.54}$$

The inversion charge can then be defined by the secant between $(0,\psi_p)$ and another arbitrary surface potential (Q_{i0},ψ_{s0}) as:

$$\frac{Q_i}{C_{ox}} = n_q\left(\psi_s - \psi_p\right) \tag{2.55}$$

$$n_q = \left(1 + \frac{\gamma}{\sqrt{\psi_{s0}} + \sqrt{\psi_p}}\right) \tag{2.56}$$

By using this linearized inversion charge expression, one may find another V_{ch} expression as:

$$\frac{V_{ch}}{\phi_T} = \ln\left[\frac{-Q_i}{\gamma C_{ox}\sqrt{\phi_T}}\left(\frac{-Q_i}{\gamma C_{ox}\sqrt{\phi_T}} + 2\sqrt{\frac{Q_i}{n_q C_{ox}\phi_T} + \frac{\psi_p}{\phi_T}}\right)\right] - \frac{Q_i}{n_q C_{ox}\phi_T} - \frac{\psi_p - \psi_{s0}}{\phi_T} \tag{2.57}$$

Using this $V_{ch}\left(\psi_s\right)$ relation into the Pao-Sah model, the drain to source current can then be expressed as:

$$i = \frac{I_{DS}}{I_0} = \left(q_s^2 - q_s\right) - \left(q_d^2 - q_d\right) \tag{2.58}$$

$$q_i = \frac{Q_i}{Q_0} \tag{2.59}$$

where I_0 and Q_0 are the specific current and charges per unit surface [56] given by:

$$I_0 = 2n_q\mu_{eff}C_{ox}\phi_T^2\frac{W}{L} \tag{2.60}$$

$$Q_0 = -2n_q C_{ox}\phi_T \tag{2.61}$$

By defining normalized potentials as $v = V/\phi_T$; normalized body factor $G = \gamma/\sqrt{\phi_T}$; normalized pincth off surface potential $\phi_p = \psi_p/\phi_t$; and normalized bulk potential $\varphi_B = \phi_B/\phi_T$ the charge to bias relation can be expressed as:

$$\ln\left(q_i\right) + \ln\left[\frac{2n_q}{G}\left(q_i\frac{2n_q}{G} + 2\sqrt{\phi_p - 2q_i}\right)\right] + 2q_i = \phi_p - 2\varphi_B - v_{ch} \tag{2.62}$$

Equation (2.4.2) present two asymptotic behaviors, when $q_i \ll 1$ (weak inversion) the normalized inversion charge can be obtained by

$$q_i \approx \frac{G}{4n_q\sqrt{\phi_p}} e^{\phi_p - 2\varphi_B - v_{ch}} \tag{2.63}$$

In contrast, when $q_i \gg 1$ (strong inversion) the normalized inversion charge presents a linear relation to ϕ_p:

$$q_i \approx \frac{\phi_p - 2\varphi_B - v_{ch}}{2} \tag{2.64}$$

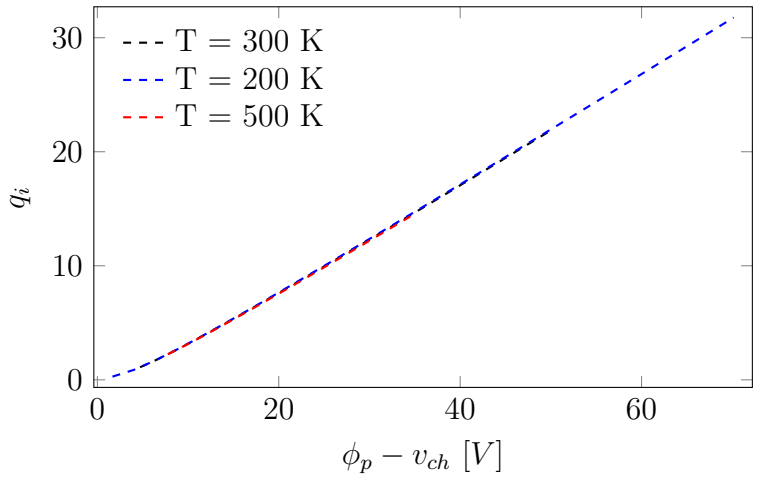


Figure 2.30: Normalized Inversion Charge over three different temperatures given as function of the normalized pitch off surface potential and normalized channel potential difference.

Figure 2.30 shows the relation between the normalized charge and the normalized pintch-off and channel voltage for three different temperatures. Notice that when considering the normalized variables the temperature variation of the inversion charge is negligible.

Solutions to Charge Linearization Models

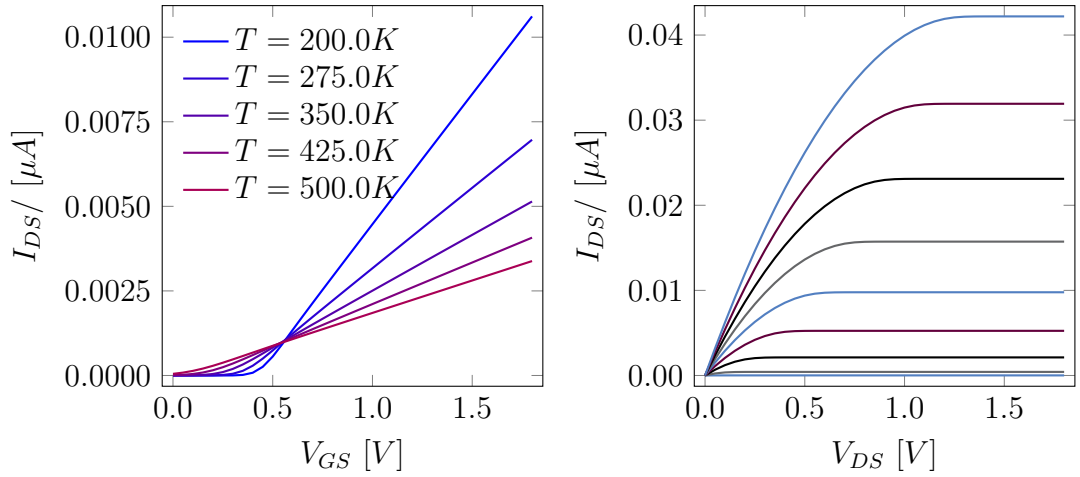
The charge linearization models have gained popularity in the latest years due to its simplicity and performance in compact models [56] [7] [6]. One of the first attempts to solve analytically the normalized charge given the transistor bias is donne by the EKV model. The EKV model relies on an interpolation function that covers both assymptotic behaviours of the linearized inversion charge previouslly discussed [57]. The EKV model approximates (2.4.2) the q_i to V_p characteristics by:

$$q_i^2 - q_i \approx \ln^2\left(1 + e^{\frac{\phi_p - 2\varphi_B - v_{ch}}{2}}\right) \tag{2.65}$$

Allowing the drain current to be written as:

$$I_{DS} = 2n_q\phi_T^2\mu_{eff}C_{OX}\frac{W}{L}\left[\ln^2\left(1 + e^{\frac{V_p - V_S}{2\phi_T}}\right) - \ln^2\left(1 + e^{\frac{V_p - V_D}{2\phi_T}}\right)\right] \tag{2.66}$$

where the V_p is the called pintch-off voltage given by $\psi_p - 2\phi_B$. Notice that when compared with the PSP current model equation the EKV equation presents a much more direct relation between transistor bias and the current allowing its use to hand-designed circuits.



(a) (b)

Figure 2.31: The EKV approximation for the charge linearisation model for a large transistor considering multiple bias points and temperatures.

As for the PSP model the current the I_{DS} characteristics for the EKV model are here shown on Fig. 2.31. The EKV strong inversion model of the pinch-off voltage needs to approach $V_{GB} - V_{Th}$ in order to be compatible with the quadratic model.

Figure 2.32 shows the $V_p \times V_{GB}$ relation on the EKV model and the $V_{GB} - V_{th}$ approximation given in dashed lines, both approximations agree close to the $V_p \approx 0$ however deviate on others bias points since the slope of V_p is actually smaller than 1. This problem can be solved by dividing $V_{GS} - V_{th}$ by n_q resulting in an very good approximation for V_p as shown in the dotted lines especially in low temperatures.

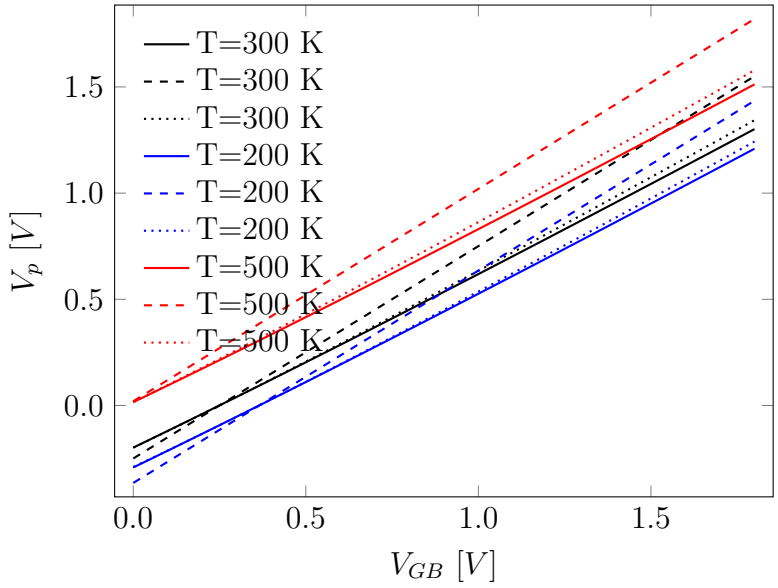


Figure 2.32: Pitch-Off voltage approximation, overdrive voltage (dashed), indroduction of n_q (doted) and numerical calculation (solid) at multiple temperatures.

2.4.3 The UICM model

Another approach to the charge linearisation model is given by [58]. The Unified Current Charge Model (UICM) introduces a new normalization constant to the inversion charges on the channel and a novel interpretation to the V_p model in such a way that the V_p to q_i relation can be expressed analytically.

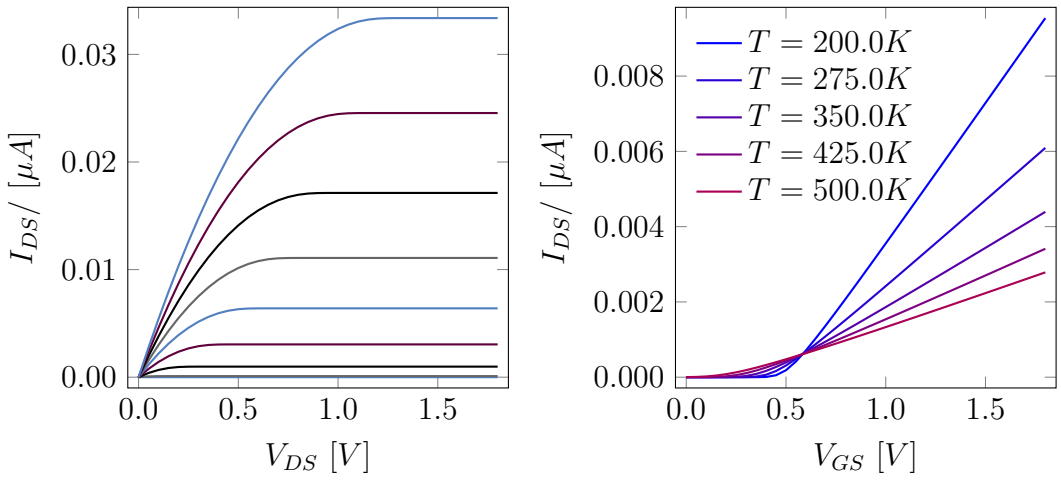
The charge linearisation from the UICM model derivation starts very close to the PSP charge sheet representation, by defining the inversion charge in differential form as:

$$dQ_i = (C_{ox} + C_b)\, d\psi_s = nC_{ox} d\psi s \tag{2.67}$$

where C_b is the depletion capacitance and n is given by $1 + \frac{C_b}{C_{ox}}$. By this definition the transistor I_{DS} can be written as:

$$I_D = \int_0^L \frac{-\mu_{eff} W}{nC_{ox}} (Q_I - \phi_T n C_{ox}) \frac{dQ_I}{dx} dx = \mu_{eff} C_{ox} n \frac{\phi_T^2}{2} \frac{W}{L} \left[\left(q_{is}^2 - 2q_{is}\right) - \left(q_{id}^2 - 2q_{id}\right) \right] \tag{2.68}$$

where q_{is} and q_{id} are the inversion charges at source and drain normalized by $-nC_{ox}\phi_T$. Notice that the I_{DS} current can be divided into a forward current i_f (controlled by q_{is}) and a reverse current i_r (controlled by q_{id}). Those current components can be written as:



(a) (b)

Figure 2.33: The ACM approximation for the charge linearisation model for a large transistor considering multiple bias points and temperatures.

$$i_{r(f)} = \left(q_{is(d)} + 1\right)^2 - 1 \tag{2.69}$$

By defining the pintch-off voltage as the gate voltage in which the normalized inversion charge is equal to 1 the following relation between $q_{is(d)}$ and the pintch-off voltage:

$$\frac{V_p - V_{S(D)}}{\phi_T} = q_{is(d)} - 1 + \ln\left(q_{is(d)}\right) = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{2.70}$$

This relation can be analytically solved by introducing the WLambert function defined as $W_0(x)e^{W_0(x)} = x$. Even though an analytical solution is achievable the calculation of the WLambert function cannot be donne accurately by series expansions and need some more computer intensive method such as newton iterations. A solution to the calculation of the W_0 function with only one newton iteration with acceptable precision for circuit simulations is proposed in [59]. The V_p expression for the depletion and inversion region can be approximated in a similar matter as did for the EKV model.

The current characteristics of a long channel UICM transistor are here shown for different bias conditions and temperatures in Fig. 2.33. In contrast to the EKV model the UICM does not relly on an interpolation function, however posseses an increased computational cost. The precision of the shown models approximations will be latter discussed and compared in this chapter.

2.4.4 The BSIM 6 Model

The Berkeley Short-channel IGFET Model (BSIM) model is one of the first developed model for small channel transistors and is considered, as the PSP model, one of the industry standard models. Up to the version 4v7 the BSIM model was a V_{th} based model. With some known minor limitations, the BSIM4 is still widely used in the industry. It has been extensively reviewed and presents curve-fitting techniques from measurements, keeping it essential in the development of MOSFET devices in the industry. As known, BSIM4 has separate equations to describe the drift and the diff regimes resulting in less smoothness in current derivative and discontinuities in the transition region between sub threshold and moderate inversion of the $I_{DS} \times V_{GS}$ curve [60]. Its complexity makes it challenging to be used in a designer-friendly framework by the extensive list of parameters and equations, however makes it a very useful validation and simulation model.

In order to mitigate these problems, beginning from the version 5 the BSIM model changed their modeling paradigm to a charge linearization model [53]. The BSIM derivation follows closely to the EKV model, however instead of using an interpolation function, it proposes a fast algorithms for calculating V_p and the normalized inversion charges with no approximations taken. Besides, the complete BSIM6 model includes many second-order and small channel effects [6].

Figure 3.17 shows the two proposed temperature normalized g_m/I_D parameters (G_g, G_d) for two different channel lengths, extracted using (3.28) and the previous extracted values. At first glance, it is noticeable that a ZTC point occurs in the DIBL dominated portion of G_d in small channel sizes. This ZTC point indicates that contrary to the usual analog design rule of thumbs of using a L bigger than L_{min} in order to minimize second-order effects when considering a temperature-aware design, a smaller L can be preferable

Figure 2.34 illustrates the current characteristics of a long channel BSIM6 transistor at different biases and temperatures. The temperature modeling of the BSIM6 model presents more than 50 parameters and accounts for temperature coefficients variations with scaling. However, contrary to the PSP model that inherited the MOS11 mobility model that includes Coulomb Scattering, the BSIM6 mobility model (same as the BSIM4) does not account for it [6]. The absence of Coulomb Scattering at mobility may lead to problems at very low temperatures and biases.

2.5 The g_m/I_D methodology

As seen before the transistor compact models can be extremely complicated, in the last chapter only an introduction to the basic formulation of the compact models

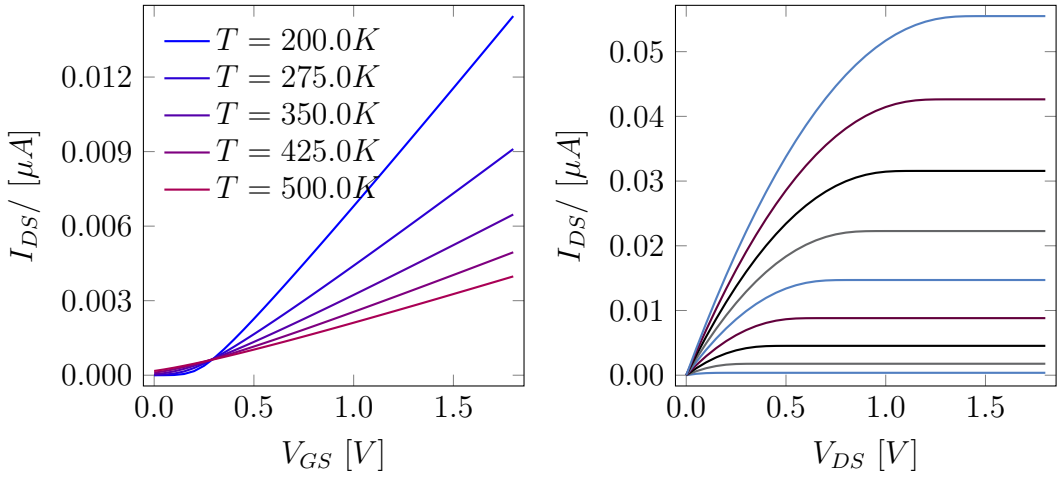


Figure 2.34: The BSIM6 approximation for the charge linearisation model for a large transistor considering multiple bias points and temperatures.

is given. In reality simulation models can have hundreds of parameters and can no longer be used to hand design circuits. For this matter Silveira *et al.* [28] proposed the g_m/I_D method, the basis for g_m/I_D comes from the fact that transistors connected in parallel behave as a stand-alone transistor with an equivalent width which is the sum of all the devices widths. The only hypothesis behind this principle is that devices are biased at the same V_{GB}. Thus, parallel transistors have the same g_m/I_D characteristic as the equivalent stand-alone transistor. This methodology have been employed and extended to handle noise analysis [61], small geometry effects [31], parameters extraction [62] and in the next chapter temperature.

One of the main advantages of the g_m/I_D methodology is its weak dependency on transistor sizing in general. The parameters employed by the technique are usually a ratio of parameters that are both proportional to the transistor aspect ratio W/L. Figure 2.35 shows the extracted g_m/I_D $\left(\frac{\partial \ln(I_{DS})}{\partial V_{GB}}\right)$ from 3 measured transistors of different sizes. Apart from noise the three characteristics follows the same overall shape and possesses similar parameters.

The g_m/I_D parameter can also be seen as a "transistor amplification efficiency", since most amplifier gains will be proportional the gate transconductance g_m and the power consumption is proportional to the sum of I_{DS} for the different branches connected to the power line. Once the g_m/I_D parameters are extracted (either by measurement data or CAD simulations) the methodology allows to size transistors appropriately only relying on the extracted design space. For analog electronics, the g_m/I_D represents a very powerful and versatile. However, as seen before

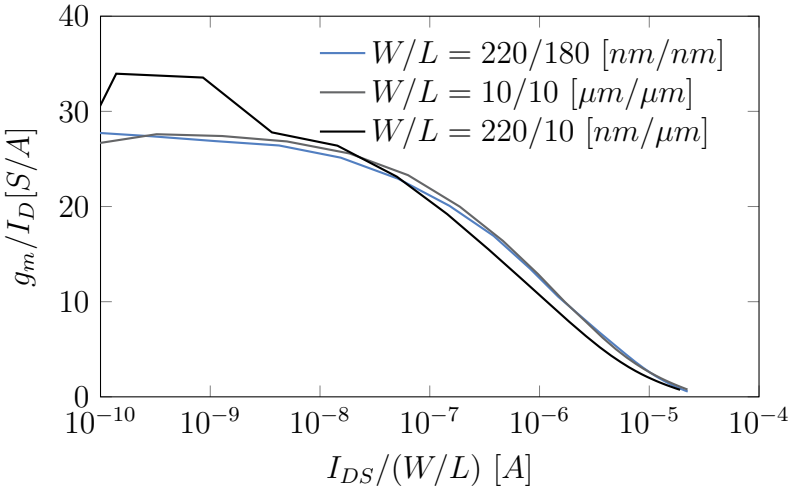


Figure 2.35: g_m/I_D calculated from measurement data for different transistor dimensions.

many of those models rely on approximations, that were never before studied over temperature variations on the g_m/I_D characteristics.

g_m/I_D Temperature Modeling on Compact Models

The g_m/I_D characteristics have an important temperature variation as depicted in Fig. 2.35. However, it has the advantage of having very little mobility dependency, except of Coulomb Scattering, that occurs in very low temperatures, the mobility is not much affected by V_{GB}. Figure 2.36 shows the g_m/I_D characteristics of a long and wide ($10\mu m/10\mu m$) transistor for 5 different temperatures). The illustrated g_m/I_D characteristics present a negative temperature coefficient, the same can be seen on the mean sensitivity plot in which for the entire biasing condition ($0 < V_{GB} < 1.8V$) the sensitivity is negative. In weak inversion, the sensitivity is high but the transistor amplifying efficiency is high, where in strong inversion the opposite is true. Those plots tends to indicate that a moderate inversion biased transistor present a good trade-off between g_m/I_D and temperature awareness.

2.5.1 Pao-Sah and Brews g_m/I_D description

Even though the Pao-Sah model has no direct application in analog design it is still considered a reference model to long channel effects, by taking the single integral formulation (2.20) and using the effective mobility definition, and considering that the inversion charge an L^2 function the g_m/I_D can be expressed as:

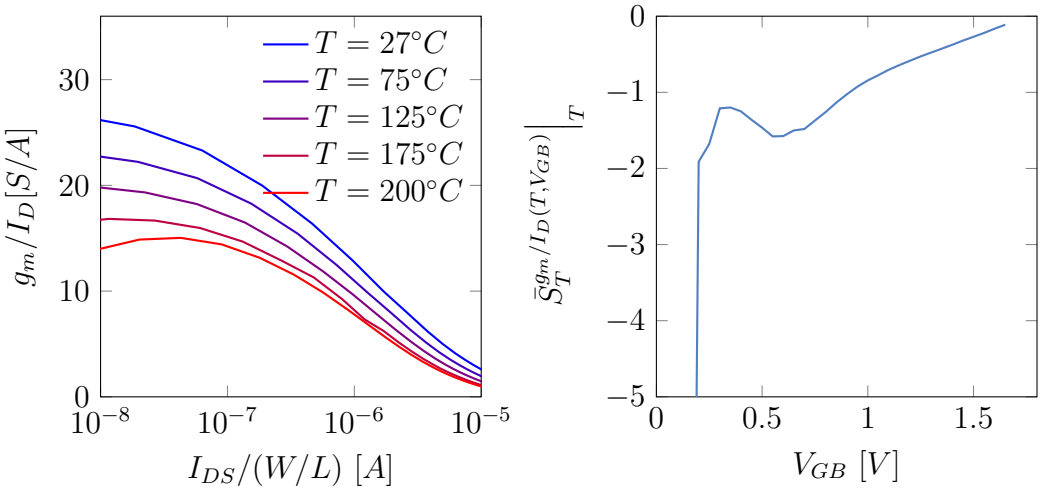


Figure 2.36: g_m/I_D calculated from measurement data for different transistor temperatures.

$$\frac{g_m}{I_D} = \frac{\partial \ln(\mu_{eff} W)}{\partial V_{GB}} + \int_{V_{SB}}^{V_{DS}} \frac{\partial Q_i(V_{GB}, V_{ch})}{\partial V_{GB}} \cdot dV_{ch} = \int_{V_{SB}}^{V_{GB}} \frac{\partial Q_i(V_{GB}, V_{ch})}{\partial V_{GB}} \cdot dV_{ch} \tag{2.71}$$

which can be seen as a channel averaged capacitance, this definition comes with the hypothesis that the log of the effective mobility has nil or negligible V_{GB} dependency. This hypothesis can be verified in Fig. 2.37 where the g_m/I_D characteristics of a transistor possessing the same process parameters as the measured transistor obtained by a third order central difference method considering the CVN mobility model (dashed lines) and constant mobility (solid lines). The relative error is also shown in Fig. 2.37, for low gate bias ($V_{GB} < 1.0V$) the error is no bigger than 10%. For higher V_{GB} the error grows, however, high gate bias is not desirable for analog circuits since the g_m gain at this condition comes with a large power consumption.

By using the regional brews model the g_m/I_D asymptotes can be obtained as:

$$\frac{g_m}{I_D} = \begin{cases} \frac{1}{\eta \phi_t} & V_{GS} \to 0 \\ \frac{1}{2(V_{GS} - V_{th})} & V_{GS} \to \infty \end{cases} \tag{2.72}$$

where η is the non ideality factor in weak inversion. The asymptotic curves (in dashed black lines) are here shown in Fig. 2.38 and, even though, shows a poor approximation which highlights the advantage of the g_m/I_D method in the moderate inversion region. Such region could never been modeled by the traditionally used quadratic model.

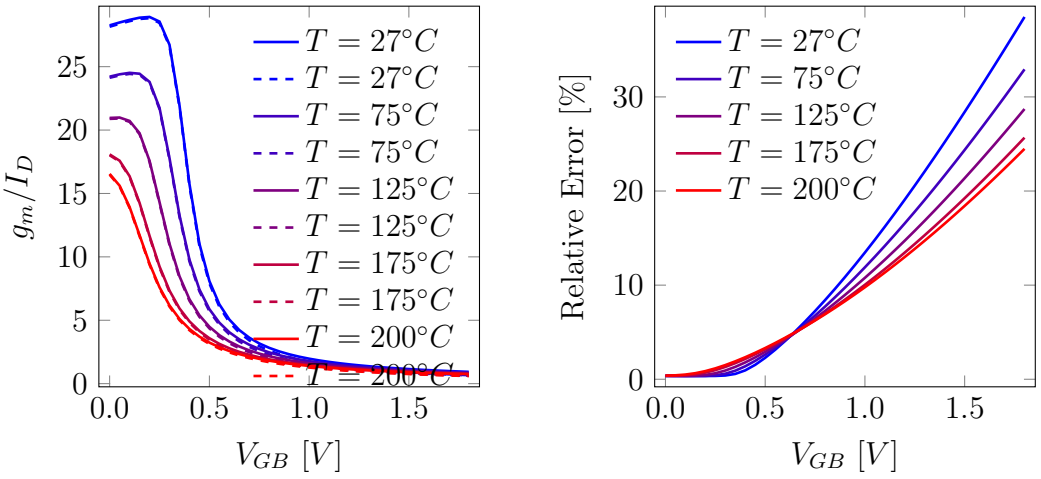


Figure 2.37: g_m/I_D characteristics obtained by a third order central difference method when considering the CVN mobility model (dashed lines) and constant mobility (solid lines) and their relative error.

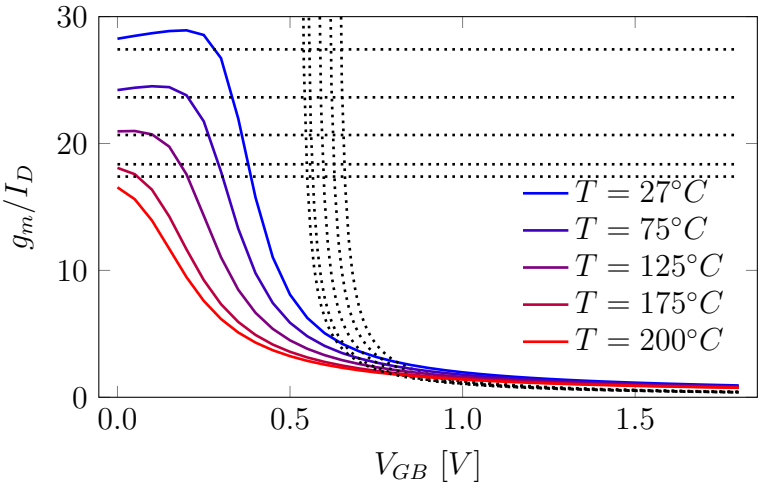


Figure 2.38: g_m/I_D characteristics obtained by a third order central difference method when considering the CVN mobility model (solid lines) and Brew's model assymptotes (dashed lines).

Chapter 3

A Temperature-Aware design Methodology

As analog circuit increases in complexity and miniaturization, even the simplest transistor current models become an overwhelming design challenge. The whole design process becomes a big non-linear coupled, often transcendental, system of equations attached to constraints such as system performance (noise, linearity, gain, speed), power consumption, and in this work scope, the temperature-awareness. Literature has already presented some design methodologies to overcome this challenge. As discussed in the last chapter, the g_m/I_D is a promising analog design methodology that was successfully extended before for distortion analysis [29], age-dependent degradation effects [30], and short channel effects [31]. Even though powerful, the g_m/I_D was never before used to address temperature effects in analog design.

This chapter proposes an extension to the g_m/I_D methodology that allows the designer to account for temperature effects on an early design stage. First, an g_m/I_D parameters versus temperature effects analysis through the UICM model is developed. With the proposed analysis, the modified g_m/I_D parameters are introduced to facilitate a temperature-aware design task. These modified g_m/I_D parameters, here called temperature normalized g_m/I_D parameters, are then explored to find ZTC points. Analytical approximations for the temperature sensitivity are proposed. All models and temperature sensitivities are compared to BSIM 4v6 simulations and measurement data for a 0.18 μm SOI technology from X-FAB XT018 node through a temperature ranging from -40 $°C$ to 200 $°C$.

3.1 Zero Temperature Coefficients (ZTC) Point

Most temperature-aware circuit designs rely on ZTC bias conditions, i.e., points where the value of a given parameter remains almost independent of temperature. The known ZTC bias conditions are based on the threshold voltage and mobility temperature dependency [4], [52]. For this reason, they are dependent on the temperature modeling of those quantities, which are not necessarily accurate in the circuit working conditions [63]. Before our work [9], here developed, there were two known ZTC bias points, the I_{DS} ZTC that where already discussed in Sec. 2.3.6, and more recently the g_m ZTC proposed by Toledo *el al.* [4].

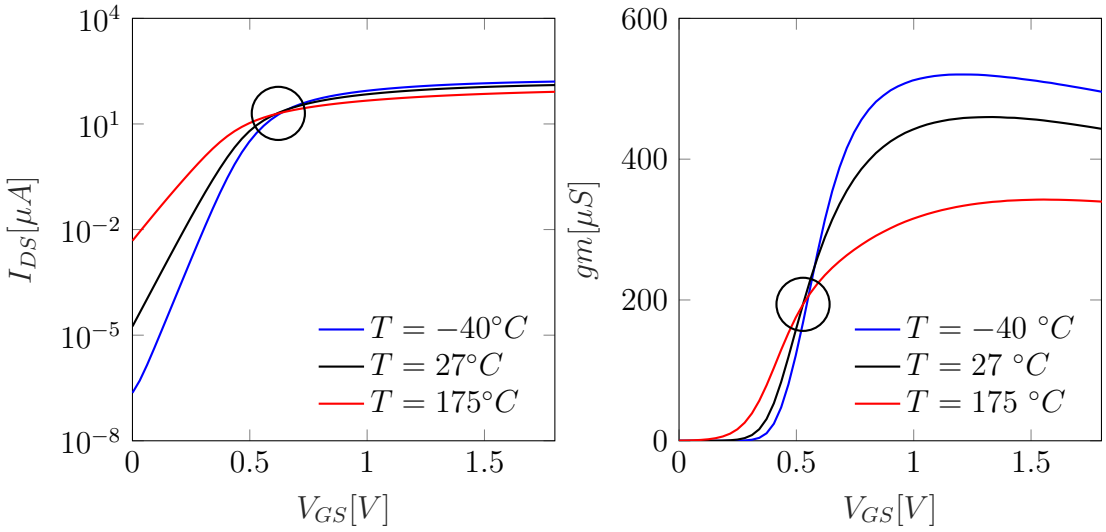


Figure 3.1: Electric Simulation of (a) $I_D \times V_{GS}$, $V_{DS} = 1.8$ V, (b) $g_m \times V_{GS}$, $V_{DS} = 1.8$ V for a $10 \times 0.22\,\mu m^2$ low V_{th} NMOS transistors of XT018. One may observe in Fig. 3.1(a) and Fig. 3.1(b) present a ZTC bias point around 0.6 V and 0.5 V, respectively. Both figures are taken at -40 °C (blue), 27 °C (black), and 175 °C (red), which lies on the temperature range in which the process design kit is validated.

Both $I_{DS_{ZTC}}$ and $g_{m_{ZTC}}$ are illustrated in Fig. 6.1 from electric simulation for a $10 \times 0.22\,\mu m^2$ low V_{th} NMOS transistors of XT018. Sub-figures (a) and (b) present a ZTC bias point around 0.6 V and 0.5 V, respectively. Both figures are taken at -40 °C (blue), 27 °C (black), and 175 °C (red), which lies on the temperature range in which the process design kit is validated trough measurements.

3.1.1 The g_m ZTC Bias

The gate transconductance is, as the V_{th}, a key parameter for analog design. The gate transconductance ZTC ($g_{m_{ZTC}}$) was proposed by Toledo *et al.* in[4]. The bias point condition for the $g_{m_{ZTC}}$ using the UICM model, considering a transistor in strong inversion $i_f \gg i_r$, and it can be expressed as

$$g_m = \frac{2I_S}{n\phi_t}\left(\sqrt{1+i_f}-1\right), \tag{3.1}$$

considering a mobility exponential temperature dependency with coefficient $\beta\mu$ and a linear V_{th} temperature dependency with a temperature coefficient of α_{vth}. The temperature derivative of the gate transconductance can be expressed by [4]

$$\begin{aligned}\frac{\partial g_m}{\partial T} &= \beta_\mu\left(\sqrt{1+i_f}-1\right)-2 \\ &\quad -\frac{\sqrt{1+i_f}+1}{\sqrt{1+i_f}}\left(\frac{|\alpha_{vth}|\,q}{\alpha k_b}+2-\ln\left(\sqrt{1+i_f}-1\right)\right).\end{aligned} \tag{3.2}$$

Notice that by disregarding the β_μ and α_{vth} temperature dependency, for a fixed i_f, the g_m temperature coefficient does not depend on temperature. A solution to (3.2) can be found numerically. Figure 3.2 shows the inversion coefficient $\left(I_{DS}/\mu_{eff}\eta C_{OX}\frac{\phi_t^2}{2}\frac{W}{L}\right)$ at 300 K.

The ZTC point was calculated using a bisection algorithm on the difference of $V_{GB} \times g_m$ characteristics at 290 K and 310 K for a transistor having dopping and oxide thickness considering Denard's scaling rules from 90 nm to 1 μm, the inversion coefficient was calculated at 300 K.

According to [5] the inversion coefficient is an indicator of the transistor operating mode, for $i_c < 1.0$ indicates weak inversion, $1.0 < i_c < 100$ moderate inversion $i_c > 100$ strong inversion, when considering Dennard's scaling [64] the $g_{m_{ZTC}}$ can be found in any inversion level (WI, MI or SI) and $i_{C_{g_m ZTC}}$ gets smaller with technology scaling.

The $g_{m_{ZTC}}$ is not only a function of V_{GB} as shown on Fig. 6.1 but also a function of V_{DS}. Figure 3.3 was obtained in the same manner as on Fig. 3.2, it illustrates the impact of V_{DS} and β_μ at the overdrive voltage to V_{th} ratio, this ratio grows as transistor length gets smaller and β_μ gets higher. For large V_{DS}, the ratio reaches a plateau that for a $L = 180\ nm, \beta_\mu = -1.0$ corresponds to a $1.2 \cdot V_{DS}$ variation when compared to the V_{GB} taken at $V_{DS} = 0\,(i_f = i_r)$.

Besides, as it can be seen in Fig. 3.3, the V_{GB} needed for $g_{m_{ZTC}}$ can vary largely with the transistors V_{DS} which can be a function of temperature when transistor drain and source are not connected to stable voltage sources.

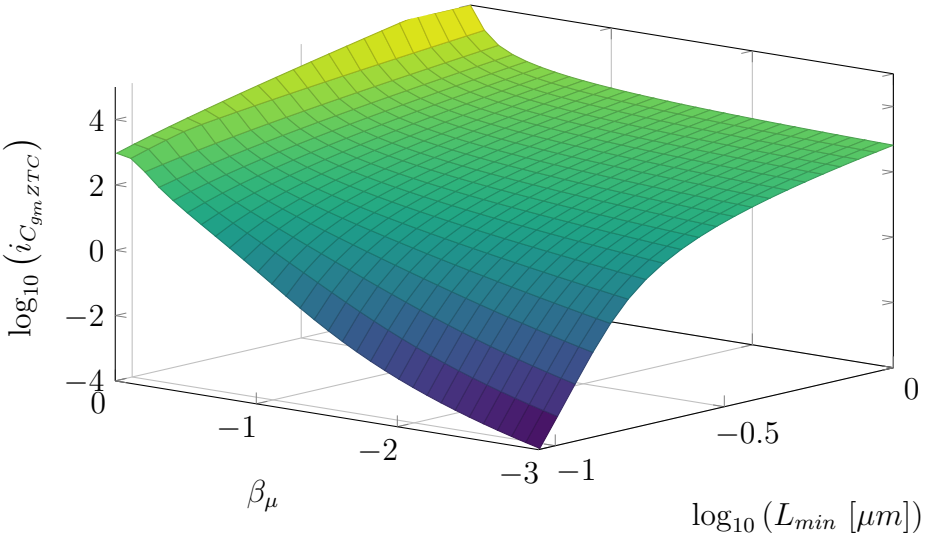


Figure 3.2: Inversion Coefficient of the $g_{m_{ZTC}}$ calculated numerically using the UICM model for different β_μ as a function of L_{min} using Denard's scalling rule. [64]

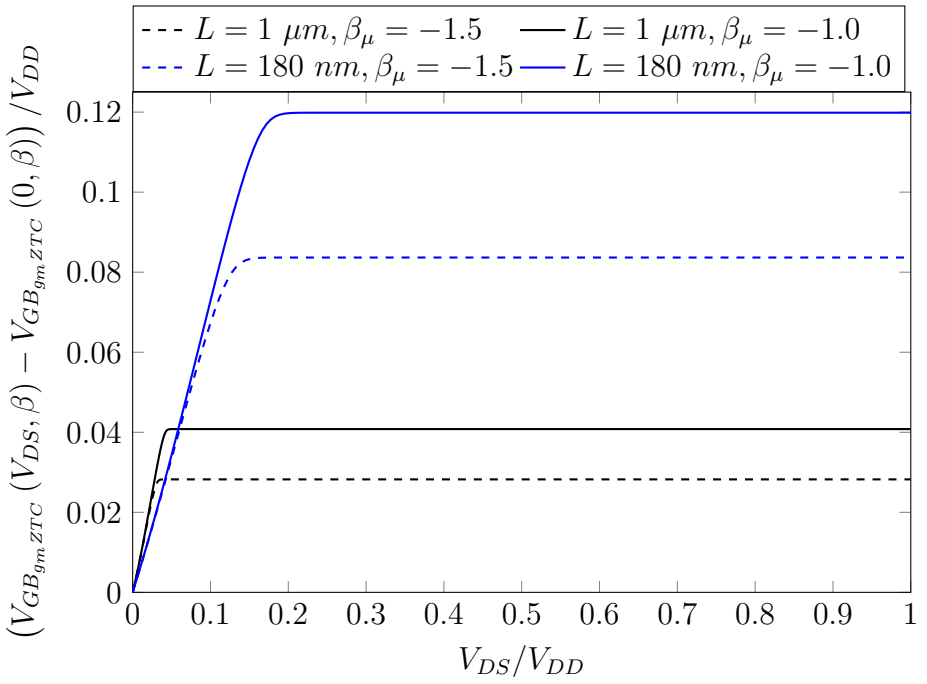


Figure 3.3: Overdrive voltage to threshold voltage ratio at $g_{m_{ZTC}}$ for two different transistors sizes at 300 K and two different mobility temperature exponent.

Even though those ZTC points exist, their bias condition relies on mobility temperature dependency, which depends on several scattering effects including ballistic ones in new technologies [45]. For this reason, modeling the temperature dependency is a challenging task. Besides, Fig. 6.1(a) and 3.1(b) highlight a required V_{GS} close to V_{th} for XT018 technology and, therefore, the transistor should be in moderate inversion region. In opposition to the strong and weak inversion, the moderate inversion does not present a straightforward current model [52]. Furthermore, some critical parameters for analog and digital design, i.e., g_{DS}, are already proven to do not have a ZTC point, as pointed out in [25].

This thesis proposes a common framework for temperature-aware design, one may approach using a design methodology such as g_m/I_D, the development of such framework will be detailed on the next section.

3.2 Temperature analysis of g_m/I_D Parameters

The g_m/I_D methodology introduces width-independent parameters allowing the designer to choose the transistor W to accommodate other circuit prerequisites such as power consumption, occupied active surface, and operation region.

Some work has been done when analyzing the temperature effects when considering different g_m/I_D values. However, no ZTC point was exploited, nor were analytical expressions for the different g_m/I_D temperature behaviors discussed. In [65] Eggermont *et. al.*, discusses some $_m/I_D$ guidelines for high-temperature applications when designing a single-stage operation transconductance amplifier (OTA). The paper proposes four different designs achieving an estimated temperature coefficient from 2917 ppm/$^\circ C$, to 4674.16 ppm/$^\circ C$, for the gain and from 2686.32 ppm/$^\circ C$ to 3719.43 ppm/$^\circ C$ for the transition frequency at a measured circuit. In [66], the same considerations taken in [65] are now stated for gate-all-around transistors at the same circuit achieving 327 ppm/$^\circ C$ for the gain and 2303 ppm/$^\circ C$ for the gain bandwidth. Even though some g_m/I_D guidelines for temperature considerations were explored before, those discussions never made possible a systematic approach when considering temperature awareness.

The main parameters analyzed in this thesis are the gate transconductance ratio (g_m/I_D) and the transistor self-gain (g_m/g_{ds}). The mathematical model to analyse those parameters will be based on the UICM model, introduced by Galup *et al.* [7]. The UICM is a charge-based model that accounts for accurate, straightforward g_m/I_D parameters expressions, even quasi-ballistic nanometer-sized transistors [8]. The validation is done using the factory temperature validated BSIM model from -40 $^\circ C$ to 175 $^\circ C$ and novel measurement data from 27 $^\circ C$ to 200 $^\circ C$.

3.2.1 Gate Transconductance Ratio

The g_m/I_D parameter for a long-channel transistor, neglecting specific current gate voltage dependency, is defined in the UICM model as:

$$\frac{g_m}{I_D} = \frac{2}{\eta(V_G) \cdot \phi_T \left(q_{is}(V_G, V_S) + q_{id}(V_G, V_D) + 2\right)}; \tag{3.3}$$

where ϕ_T is the thermal voltage; q_{is}, q_{id} are the inversion charge on the source side and the drain side normalized by the inversion charge at pinch-off.

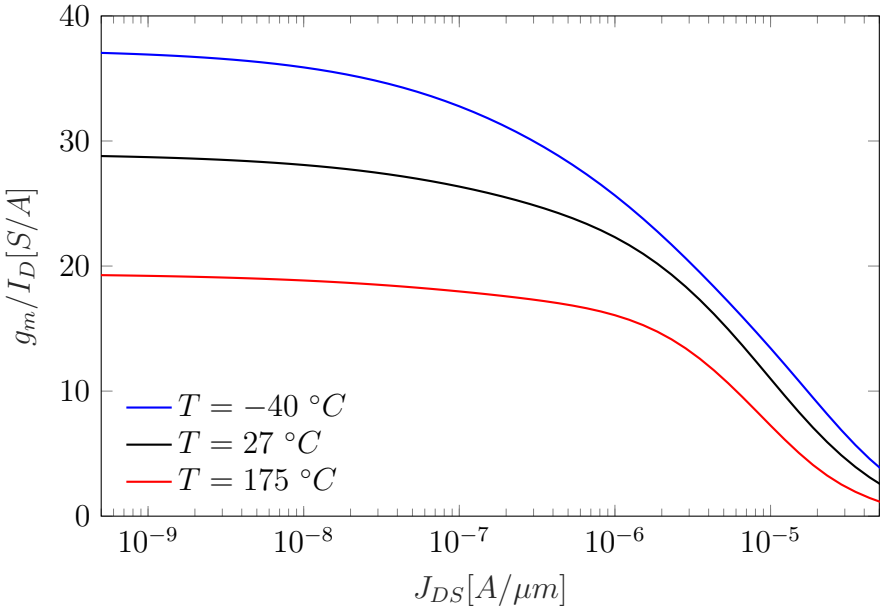


Figure 3.4: Electric Simulation of $g_m/I_D \times V_{GS}$, $V_{DS} = 0.1$ V, low V_{th} NMOS transistors of XT018 taken at -40 °C (blue), 27 °C (black), and 175 °C (red), which lies on the temperature range in which the process design kit is validated.

Figure 3.4 illustrates the g_m/I_D parameter obtained from electric simulation using XT018 process design kit for a $10 \times 0.22\mu m^2$ low V_{th} NMOS transistor for three different temperatures, one may notice the absence of ZTC bias. From a design point of view, it is helpful to analyze the bias dependency of the given parameter, through (3.3). There the only term that is not bias dependent is ϕ_T. In order to consider a temperature-aware bias selection using g_m/I_D, one may define the temperature normalized gate transconductance ratio (G_g) as:

$$G_g = \phi_T \cdot \frac{g_m}{I_D}. \tag{3.4}$$

The sensitivity is defined in [67] as the normalized variation $S_x^{y(x)} = \frac{\frac{\Delta y}{y}}{\frac{\Delta x}{x}} \approx \frac{x}{y(x)} \cdot \frac{dy(x)}{dx}$. The temperature normalized gate transconductance G_g is a function of η, q_{IS} and q_{ID}, and can be expressed as:

$$S_T^{G_g} = -\left[S_T^{\eta} + \left(q_{is} \cdot S^{q_{is}} + q_{id} \cdot S^{q_{id}}\right) \cdot \frac{G_g \cdot \eta}{2}\right]. \tag{3.5}$$

As reported in [8], the weak inversion slope factor η is sufficient to represent the g_m/I_D characteristics even in quasi-ballistic transistors; therefore, one may define η by neglecting the inversion charge as:

$$\eta = \left(\frac{\partial \psi_{sa}}{\partial V_{GB}}\right)^{-1} = 1 + \frac{\gamma}{2 \cdot \sqrt{\psi_{sa}}}, \tag{3.6}$$

$$\psi_{sa} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB} - V_{FB}(T)}\right)^2, \tag{3.7}$$

by definition, the η sensitivity can be calculated as:

$$S_T^{\eta} = \frac{T}{2} \frac{\partial V_{FB}/\partial T}{\psi_{sa}^2 \left(2 \cdot \sqrt{\psi_{sa}} + \gamma\right)}, \tag{3.8}$$

the flat-band voltage temperature behavior depends on the materials used for the transistor gate contact and bulk. In the node sizes addressed in this thesis, the gate contacts are highly doped poly-Silicon over a SOI substrate. The poly-Silicon is considered doped enough, so its Fermi level is pinned to the conduction band. By considering a low enough doping on the substrate and Boltzmann statistics, one may write:

$$\frac{\partial V_{FB}}{\partial T} = \frac{1}{T}\left(\frac{E_G(T=0)}{2 \cdot q} - \phi_F\right). \tag{3.9}$$

For Silicon, the extrapolated bandgap at 0 K ($E_G(T=0)/q$) is 1.12 eV. For normal doping levels, the Fermi level is not very apart from the middle gap ($E_G(T=0)/2 \cdot q$) making the flat-band voltage (V_{FB}) temperature derivative very low and, by consequence S_T^{η} negligible.

Some approximations were made for the development of the η sensitivity. Figure 3.5 evaluates the relative error of those approximations when calculating the Fermi Level. The gray area's top represents the limit where Boltzmann statistics and incomplete dopant ionization give a relative error smaller than 1%. The bottom border of the gray area is caused by neglecting minority carriers on the Fermi level calculation. Since the usual doping of Silicon starts to rise with scaling,

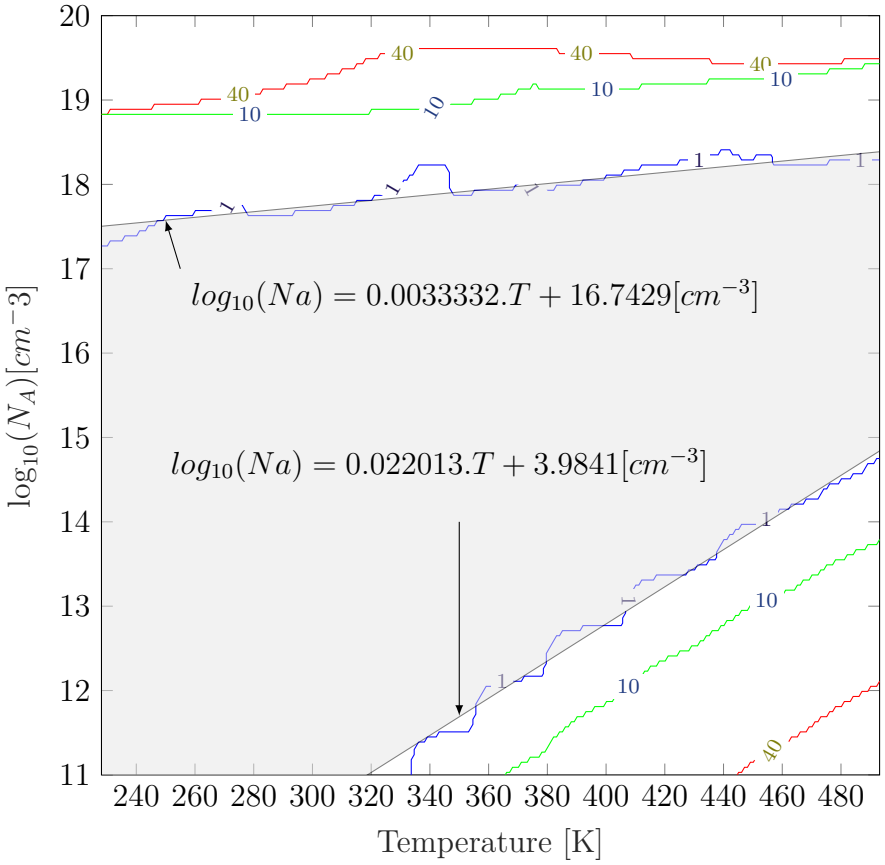


Figure 3.5: Relative error of approximation of Boltzmann statistics, neglecting minority carriers, and complete dopant ionization on the calculation of the Fermi level.

some factors to account for Fermi-Dirac statistics and incomplete ionization may be added for smaller technologies.

The normalized inversion charges (q_{is}, q_{id}) sensitivity can be obtained from the so-called universal MOSFET characteristics of the UICM model

$$\frac{V_p - V_{S(D)}}{\phi_T} = q_{is(d)} - 1 + \ln\left(q_{is(d)}\right), \tag{3.10}$$

by taking the temperature sensitivity of both sides of (3.10) one may find

$$S_T^{q_{is(d)}} = -\frac{V_p \cdot \left(S_T^{V_p} - 1\right) + V_{S(D)} \cdot \left(S_T^{V_{S(D)}} - 1\right)}{\phi_T \cdot \left(q_{is(d)} + 1\right)}. \tag{3.11}$$

It is essential to point out that unlike the ZTC bias pointed out in Sec. 3.1.1, the bias voltages are considered temperature-dependent. The importance of considering the temperature dependency of the bias voltages is that even though on the test benches often used for to extract the ZTC points, the bias point is constant, in a more complex circuitry, transistor nodes not connected to voltage sources can suffer from bias drift with temperature. For an extended temperature range, the use of Silicon over Insulator (SOI) is essential to minimize bulk leakage currents. Considering a MOSFET with source and bulk connected $V_S = 0$ and that in moderate inversion ($1 < q_{is(d)} < 100$) $q_{is} \approx q_{id} = \bar{q}$ one may find

$$S_T^{G_g} = \frac{\bar{q} \cdot \left(V_p \left(S_T^{V_p} - 1\right)\right)}{\phi_T \left(1 + \bar{q}\right)^2}. \tag{3.12}$$

Since q_{id}, q_{is}, G_g, η, and ϕ_T are always greater than 0, one may find that the ZTC condition is $V_p \left(S_T^{V_p} - 1\right) = V_x$, by taking the usual approximation of $V_p \approx {}^{(V_{GB}-V_{th})}/_{\eta}$ and the threshold voltage temperature dependency from (2.37). One may find that the nil condition of (3.12) being

$$V_p|_{S_T^{G_g}=0} = \frac{\alpha_{th} \cdot T}{\eta} \tag{3.13}$$

At the vicinity of the ZTC point, $V_p \approx 0$; $q_{is} \approx q_{id} \approx 1$ [7] the sensitivity can be approximated as:

$$S_T^{G_g} \approx \left(\frac{T \cdot \alpha_{th}}{V_p \cdot \eta} - 1\right) \frac{V_p}{4 \cdot \phi_T}, \tag{3.14}$$

by replacing (3.13) in (3.10) ones may find that $\bar{q}$ is independent of V_D and equal to a temperature invariant constant (ν):

$$G_g|_{ZTC} = \frac{1}{2 \cdot \eta \cdot \nu} \tag{3.15}$$

Since for modern node sizes, α_{th} tends to get smaller due to the channel doping increase [52], as illustrated on Fig. 3.6, and η lies between 1 and 3, the right-hand side of (3.13), is very close to zero and a weak temperature function.

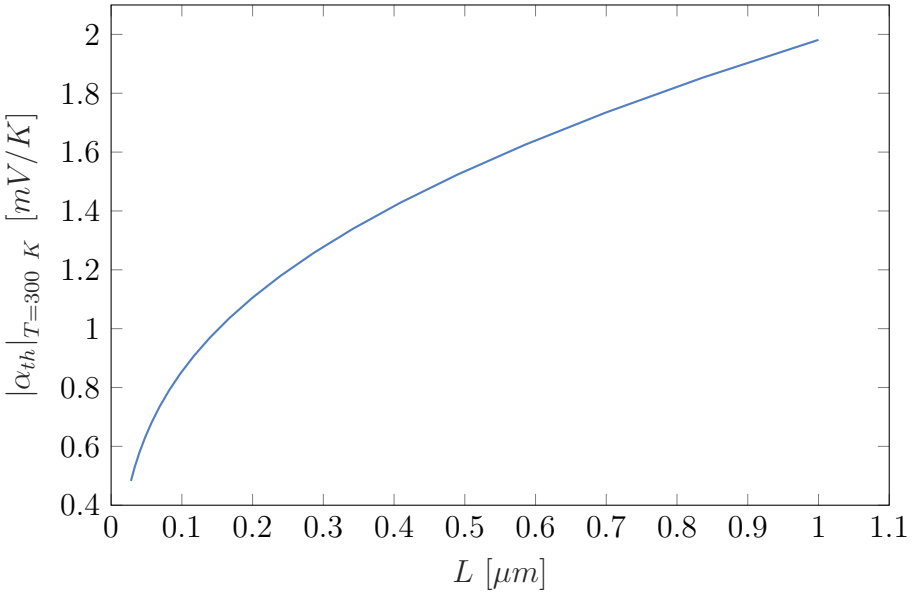


Figure 3.6: α_{th} calculated at 300 K considering Dennard's scalling rule for different transistor sizes.

Figure 3.7 shows the sensitivity of the G_g parameter for a $10 \times 10\,\mu m^2$ low V_{th} transistor obtained from BSIM simulations using the factory validated PDK from -40 $°C$ to 175 $°C$. It is important to point out that in our simulations, the same ZTC point was found in small length transistors, which is expected since g_m/I_D is known to have little channel length dependency [8].

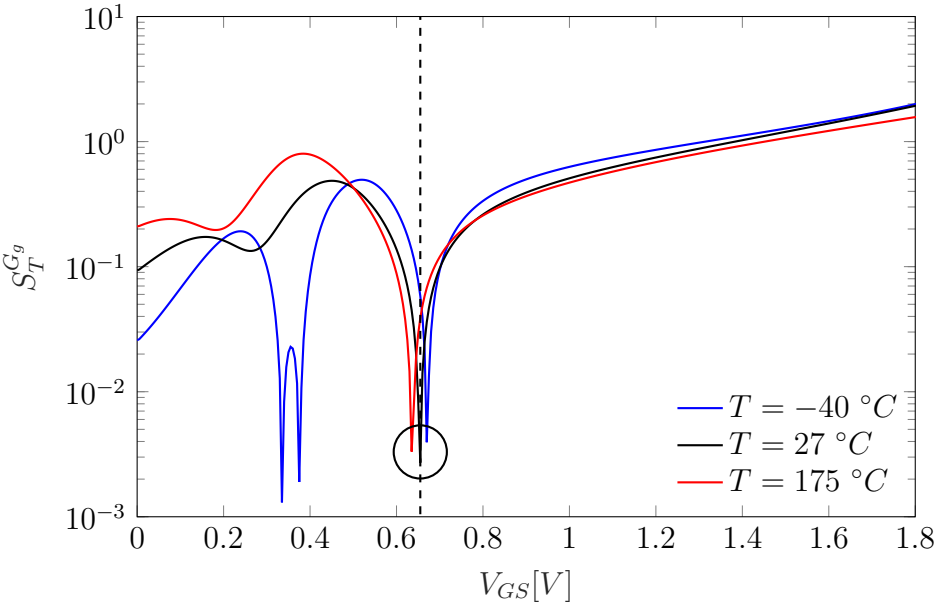


Figure 3.7: The G_g for a Low VT NMOS transistor $10\,\mu m \times 10\,\mu m$ on different temperatures on the valid simulation range.

To extend the temperature range, factory measurements were made and are here presented on Fig.3.8. The same ZTC bias point can be seen in measurement data obtained from the same transistor up to 200 $°C$. Figure 3.8 shows the G_g parameter extracted from measurement data at 27, 75 , 125, 175, 200 $°C$ of a long and a short channel Low V_{th} NMOS transistor with the estimated $V_{GS_{ZTC}}$. The gate transconductance was obtained using Euler's method. Threshold voltage was obtained at the different temperatures by the linear extrapolated method with the correction proposed in [68] following the threshold definition. The extracted V_{th} at different temperatures was later fitted using least squares to obtain α_{th} and V_{th0} estimation. The η parameter was obtained from the linear interpolation of the log current in weak inversion.

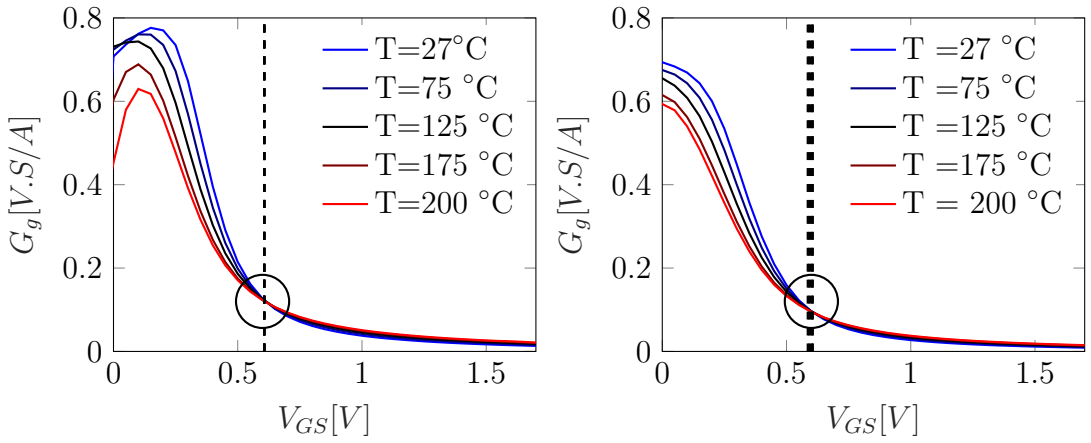


Figure 3.8: The G_g parameter extracted from measurement data from a Low VT NMOS transistor at 27, 75, 125, 175, 200$°C$ (from blue to red) with dimensions (a) $10 \times 10\ \mu m^2$ and (b) $10 \times 0.18\ \mu m^2$ with $V_s = 0$ and $V_D = 0.1\ V$.

3.2.2 Parasitic Source/Drain Diodes

On the MOSFET structure two parasitic diodes are present at the source to gate and drain to gate NP junctions. At high temperatures, the reverse-biased parasitic diodes at the S/D nodes could drain a large current (in the order of magnitudes of a few nA) to the Bulk as shown in Fig. 3.9.

Figure 3.9 shows the I_B to V_{DS} relation from a measured silicon over oxide (SOI) NMOS with $W/L = 220\ nm/180\ nm$. The usage of a SOI technology already limits this current by dramatically decreasing the conductance at the leak

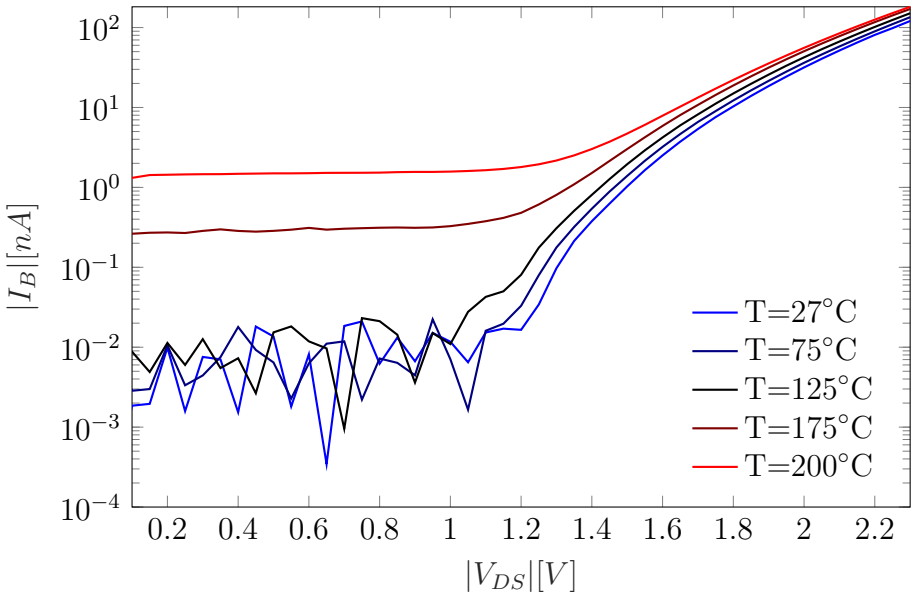


Figure 3.9: NMOS low VT transistor bulk current at $V_{GS} = 0.5$ V.

current path while limiting Joule heating evacuation when compared with bulk technology.

In low power applications those currents may have an impact on the total drain to source current. To investigate the source/drain diodes effects on the g_m/I_D characteristics considering a simple model of the diode current dependent only on the V_{DB} voltage [56], the drain to source current and, by consequence the, g_m/I_D can be written as:

$$I_D = I_{DS}\left(V_{GB}, V_{DB}, V_{SB}\right) - I_B\left(V_{DB}\right), \tag{3.16}$$

$$\frac{g_m}{I_D} = \frac{\partial \ln\left(I_D\right)}{\partial V_{GB}} = \frac{g_m}{I_{DS} - I_B}. \tag{3.17}$$

One may use (3.17) to calculate the relative error on the g_m/I_D characteristics as:

$$R = \frac{\Delta g_m/I_D}{g_m/I_{DS}} = \frac{1}{\frac{I_{DS}}{I_{BD}} - 1} \approx \frac{I_B}{I_{DS}} \tag{3.18}$$

that for big values of $\frac{I_B}{I_{DS}}$, R can be approximated to I_B/I_{DS}. To evaluate the consequences on the G_g temperature sensitivity one may write:

$$g_m/I_D = \frac{g_m/I_{D_0}}{1+R}, \tag{3.19}$$

where g_m/I_{D_0} is the g_m/I_D parameter without the diodes leakage current. By taking the sensitivity operator on both sides one may find

$$S_T^{g_m/I_D} = S_T^{g_m/I_{D_0}} - \left(\frac{S_T^R}{R+1}\right). \tag{3.20}$$

By taking the G_g definition and considering the an exponential temperature relation on the diode current [69] with a temperature coefficient β_{DB} one may get:

$$S_T^{G_g} = S_T^{G_{g_0}} - \left(\frac{\beta_{DB}}{T} - S_T^{I_{DS}}\right)\frac{R}{R+1} = S_T^{G_{g_0}} + \Delta S, \tag{3.21}$$

where G_{g_0} is the G_g parameter without considering the leakage current. It can be seen on the right column of Fig. 3.9 the leakage current under moderate inversion in a small ratio transistor ($220 \times 180\ nm^2$) presents in this technology the worst case scenario of $R = 0.1\%$. Consequently ΔS is also small making $S_T^{G_g} \approx S_T^{G_{g0}}$. In weak and moderate inversion the G_d and G_g presents a linear relation, since the sensitivity operator is invariant to scaling, it is expected that the leakage current have also little effect on the ZTC point.

3.2.3 Self Gain

Another critical parameter on the g_m/I_D methodology is the self-gain (g_m/g_{DS}). This parameter's modeling needs to be handled with little more attention since the self-gain is very sensitive to short channel effects compared to the g_m/I_D parameter. According to [70], the significant short channel effects controlling the drain to source transconductance are velocity saturation, drain induced barrier lowering (DIBL), and channel length modulation (CLM). Those effects will be first evaluated, and then a g_m/g_{DS} expression will be presented for temperature behavior evaluation.

Drain Induced Barrier Lowering

The DIBL is a 2D effect that includes the variation of carriers barrier on the source to drain axis caused by the V_D variation. In a long channel MOSFET, the threshold voltage can be extrapolated from the classical MOS capacitor 1D analysis, since most of the channel has similar behavior. However, this approximation does not hold in short channels since the transverse field and drain/source junctions can no longer be neglected. In the short channel case, the V_D increase causes a reduction of the PN barrier between source and gate, usually modeled as a linear relationship between the threshold voltage and V_D[52].

$$V_{th}\left(V_{DS}\right) = V_{th}\left(0\right) - \sigma \cdot V_D. \tag{3.22}$$

Since the definition of DIBL naturally depends on the transistor length, many works have proposed different $\sigma(L)$ relations. However, most experiments show a power relation with L [52]. One may express this relation in general as:

$$\sigma(L) = \frac{(\sigma_0 + \sigma_1 \cdot V_{SB})}{\pi t_{ox} L^m}. \tag{3.23}$$

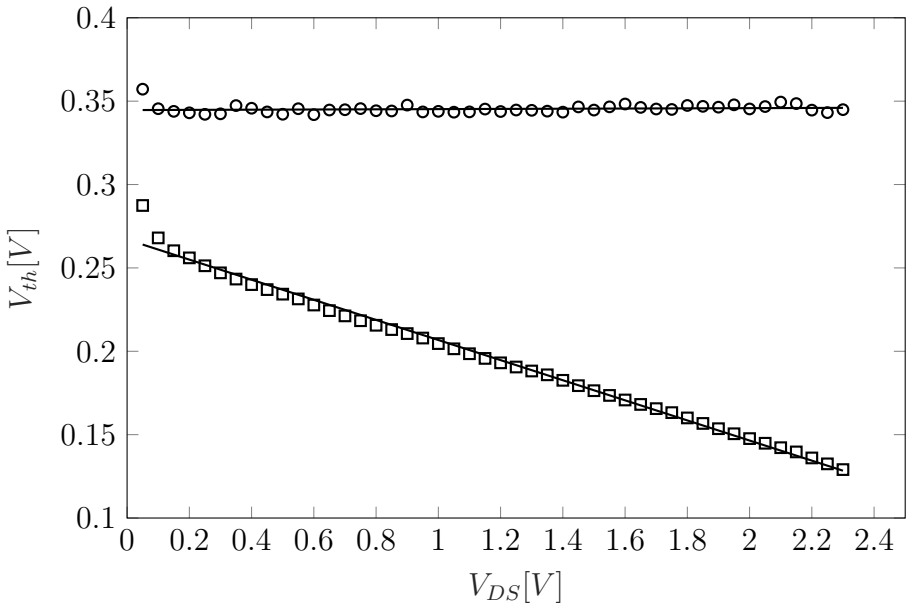


Figure 3.10: Estimated DIBL from measurement data for a Low VT NMOS transistor with $L = 0.18\mu m$ (squares), $L = 10\mu m$ (circles), and the fitted data (solid lines).

Figure 3.10 shows the DIBL effect from measurement data. V_{th} was extracted using the method explained in [71]. Even though the work [72] points out a linear increase of σ with temperature, as illustrated in Fig. 3.11, the 99.7% confidence bars of the extracted σ value exceeds the presented temperature variation, and therefore was considered negligible. Since the available measurement data only contains two different channel lengths, the σ parameter was extracted from Spectre simulations from the foundry PDK. Even though BSIM 4v6 (suitable for the node size) models $\sigma(L)$ having an exponential relation, [52] points out that the model shown in (3.23) fits better with experimental results. For this reason the latest BSIM version uses (3.23) model [6]. Figure 3.12 shows the comparison of both models presenting overall similar behavior.

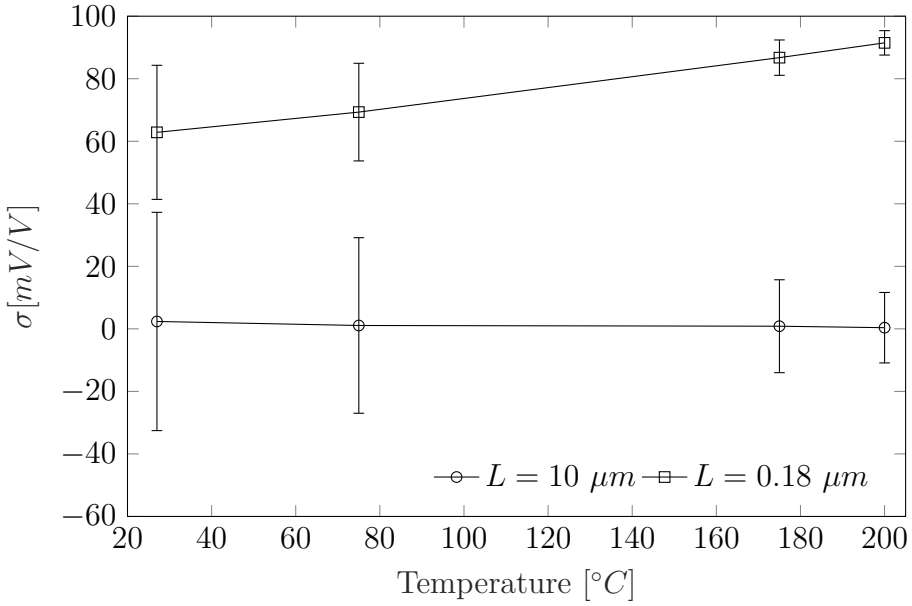


Figure 3.11: Estimated DIBL from measurement data for a Low VT NMOS transistor with $L = 0.18\mu m$ (squares), $L = 10\mu m$ (circles) and the fitted data (solid lines).

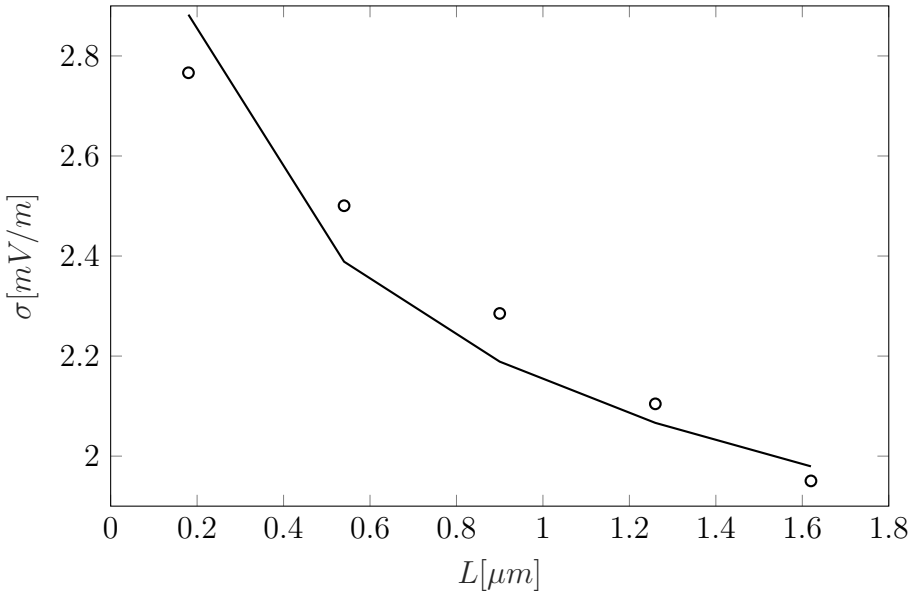


Figure 3.12: Estimated σ parameter for different channel lengths estimated from BSIM 4v6 (circles), and fitted data.

Velocity Saturation

With the decrease of channel length, the electric fields hugely increase, giving carriers more energy and increasing the probability of scattering events [45]. This increase of scattering events, limits the maximum electric field on the channel to a value E_{sat}. This saturation makes the transition between the linear and saturated regimes occurs earlier than the classical limit $V_{D_{sat}} = V_{GS} - V_{th}$. In [70], the $V_{D_{sat}}$ is considered constant ($\approx L \cdot E_{sat}$) because the channel length is smaller than 200 nm, which is not the case for all transistors on the working technology. Jepers *et al* [73] define $V_{D_{sat}}$ as $2/g_m$ that, in contrast to [70] is highly dependent of V_{GS}, a proposition considering both effects in $V_{D_{sat}}$ is given in [74] as:

$$V_{D_{sat}} = 2/g_m \| L \cdot E_{sat}. \tag{3.24}$$

To validate (3.24), $V_{D_{sat}}$ was extracted using [75], the E_{sat} value was calculated from the measured g_m/I_D for $L = 10\mu m$ and then reused for $L = 0.18\ \mu m$. The obtained $V_{D_{sat}}$ can be shown in Fig. 3.13. The obtained $E_{sat} = 1.396 \cdot 10^4\ V/cm$ value is in accordance with literature values.

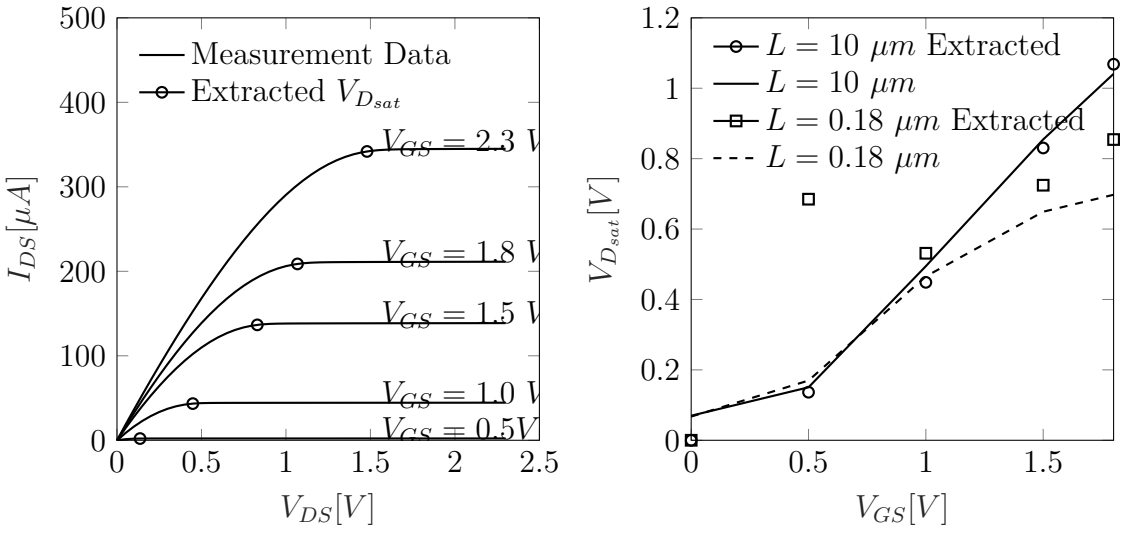


Figure 3.13: $V_{D_{sat}}$ Extraction, in (a) the extracted $V_{D_{sat}}$ is highlighted with circles at different V_{GS}, (b) shows the extracted model based on (3.24) for $L = 10\mu m$ (circles) and $L = 0.18\mu m$.

Channel Length Modulation

When the drain to source voltage exceeds $V_{D_{sat}}$, the pinch-off region starts to grow towards the source, making the effective channel length smaller with the increase of V_{DS}. In [70] the CLM effect is modeled as:

$$F_{CLM}\left(V_{DS}\right) = \left(1 + \frac{V_{DS} - V_{D_{sat}}}{V_0}\right)^{\frac{1}{\alpha}}, \tag{3.25}$$

the α coefficient is a length-dependent coefficient responsible for the CLM strength and V_0 a constant model parameter. It is important to point out that, even though no temperature studies were made concerning the α and V_0 parameters, they showed no temperature dependency on our experiments. Figure 3.14 shows the results from the extraction of CLM parameters using [70] for different channel lengths and temperatures, α and V_0 were kept constant trough different temperatures while E_{sat} modelled with a surface roughness scattering predominant model [52]. The obtained values where $V_0 = 0.433$ V and the α parameter modelled in [76] as

$$\alpha = \alpha_0 + \alpha_1 \cdot L + \alpha_2 \cdot L^2. \tag{3.26}$$

It is important to point out that the temperature variation observed in Fig. 3.14(a) is due to E_{sat} variation following the dependency of the limiting scattering effect. Contrary to mobility temperature dependency, the scattering mechanism is known and unique (surface roughness scattering on Silicon). Since only one scattering mechanism is responsible for the field saturation, the exponential temperature behavior can be taken with no approximation. Figure 3.14(b) validates (3.26) by showing the extracted value of α and the polynomial relation with the channel length.

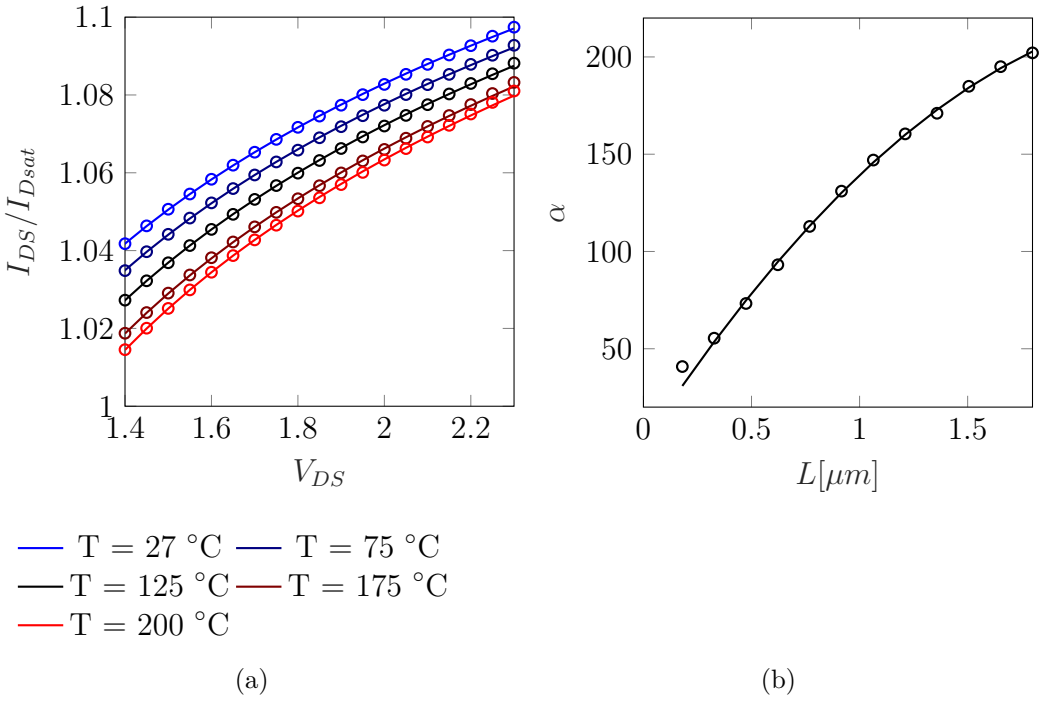


Figure 3.14: CLM parameters extraction, (a) for $L = 0.18\mu m$ for temperatures 27, 75, 125, 175, 200 $°C$ (from blue to red) and α obtained from L_{min} to $10 \cdot L_{min}$. Circles represent extracted data from simulations, and lines the proposed models.

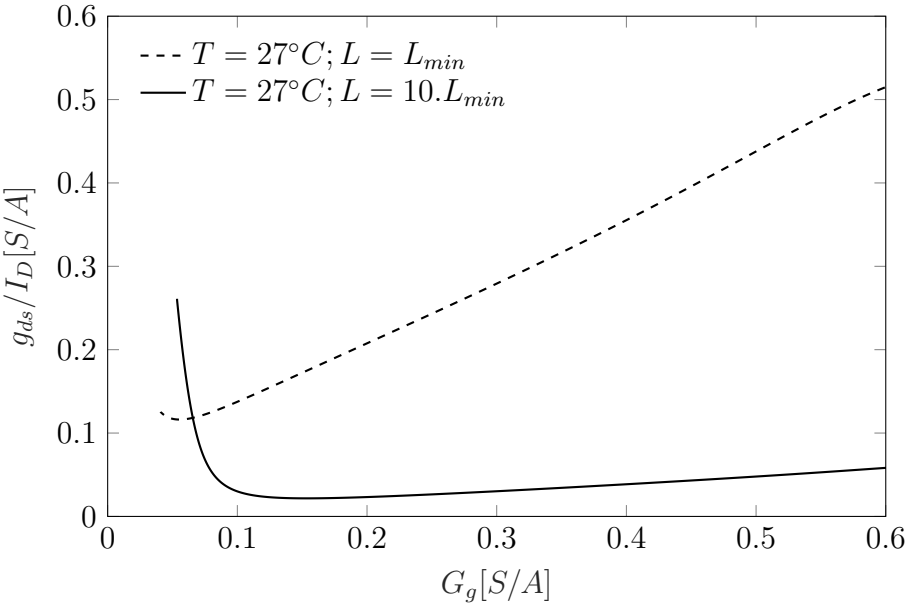


Figure 3.15: $g_{ds}/I_D \times G_g$ plot obtained from BSIM model for different L and $V_{DS} = 0.6$V.

The g_m/g_{ds} Model

The latest subsections explained the principal effects that affect the self-gain, with those effects modeled and extracted based on [73] definition, one may write g_m/g_{ds} as a function of the temperature normalized gate transconductance ration G_g:

$$\frac{g_m}{g_{ds}} = \frac{g_m}{I_D} \cdot \left(\frac{g_{ds}}{I_D}\right)^{-1} \tag{3.27}$$

$$\frac{g_{ds}}{I_D} = \sigma \cdot \frac{G_g}{\phi_T}. + \frac{1}{\alpha \cdot \left(V_0 + V_{DS} - \left(\frac{2\phi_T}{G_g}\| L \cdot E_{sat}\right)\right)}. \tag{3.28}$$

Figure 3.15 shows the $g_{ds}/I_D \times G_g$ plot for one transistor with two different channel lengths. The decreasing part of the curve is dominated by CLM, represented by the second term in (3.28). The increasing portion is the DIBL dominated $g_{ds}/I_d\,(G_g)$ relation. Figure 3.16 shows the temperature variation of the g_{ds}/I_D parameter using $4{\cdot}L_{min}$, a very common rule of thumb length sizing for analog design, $V_{DS} = 0.6V$ at different temperatures -40 $°C$, 27 $°C$ and 175 $°C$. Even though the different curves cross in an area close to $G_g = 0.1$ the difference on the bias of those crossing points are very different and therefore unusable for large temperature variations. For low-power devices, weak and moderate inversion bias is

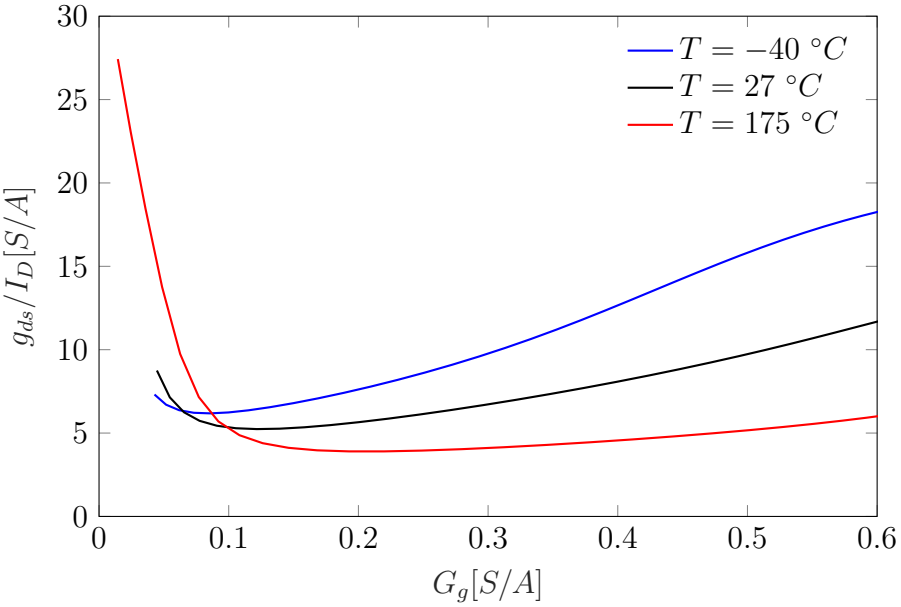


Figure 3.16: $g_{ds}/I_D \times G_g$ plot obtained from BSIM model for different L and $V_{DS} = 0.6$V.

preferable, the transistor's bias point will rather lie on the DIBL dominated region. As in the g_m/I_D characteristics, a factor $1/\phi_t$ is present on this region. Thus, one may define a temperature normalized quantity (G_d) for the g_{ds}/I_D similarly to what was done for g_m/I_D as

$$G_d = \frac{g_{ds}}{I_D}\phi_T. \tag{3.29}$$

Since most of the analog expressions for circuits are written in terms of g_m/I_D and g_m/g_{ds}, it is essential to highlight the expression of the latter as a function of the temperature normalized g_m/I_D parameters. Figure 3.17 shows the relation of both temperature normalized parameters for different channel lengths.

$$\frac{g_m}{g_{ds}} = \frac{\frac{g_m}{I_D}}{\frac{g_{ds}}{I_D}} = \frac{G_g}{G_d}. \tag{3.30}$$

Figure 3.17 shows the two proposed temperature normalized g_m/I_D parameters (G_g, G_d) for two different channel lengths, extracted using (3.28) and the previous extracted values. At first glance, it is noticeable that a ZTC point occurs in the DIBL dominated portion of G_d in small channel sizes. This ZTC point indicates that contrary to the usual analog design rule of thumbs of using a L bigger than L_{min} in order to minimize second-order effects when considering a temperature-aware design, a smaller L can be preferable

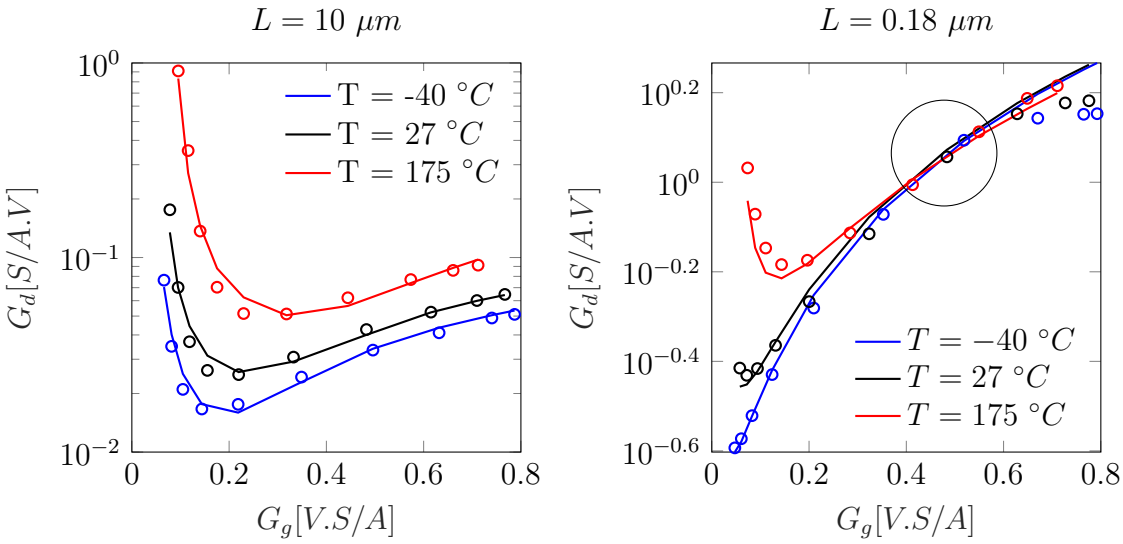


Figure 3.17: Proposed temperature normalized parameters extracted from for (a) $L = 10\ \mu m$ and (b) $L = 0.18\ \mu m$ for temperatures -40, 27 and 175 $°C$ (from blue to red) obtained from simulated data.

Temperature Analysis

In order to evaluate the G_d temperature sensitivity, one may write (3.28) as a function of G_g, for this matter, G_d will be divided into two parts, responsible for DIBL and CLM effects:

$$\begin{cases} G_d^{DIBL} & = \sigma \cdot G_g \\ G_d^{CLM} & = \frac{\phi_T \left(G_g \, LE_{sat} + 2\,\phi_T\right)}{\alpha \left(V_0 + V_{DS}\right)\left(G_g \, LE_{sat} + 2\,\phi_T\right) - 2\,\phi_T \, LE_{sat}} \end{cases} \tag{3.31}$$

By separating G_d on those factors, the total sensitivity can be written as:

$$S_T^{G_d} = \frac{G_d^{DIBL} \cdot S_T^{G_d^{DIBL}} + G_d^{CLM} \cdot S_T^{G_d^{CLM}}}{G_d}, \tag{3.32}$$

Furthermore, ZTC bias occurs in the DIBL dominated part of G_d, i.e. G_d^{CLM} close to $\phi_T/\alpha\left(V_0 + V_{DS}\right)$. The sensitivity of G_d^{DIBL} is approximately the same as G_g due to the weak temperature dependency of the multiplicative factor. One may suppose that the ZTC points occur when:

$$\sigma \cdot G_g \cdot S_T^{G_g} = -\frac{\phi_T}{\alpha\left(V_0 + V_{DS}\right)}, \tag{3.33}$$

using the approximations developed for the ZTC vicinity of G_g

$$\left(V_p|_{S_T^{G_g}=0} - V_p\right) = -\frac{8\eta\phi_T^2}{\alpha \cdot \left(V_0 + V_{DS}\right)\sigma}. \tag{3.34}$$

Figure 3.17(b) shows the G_d sensitivity, as described by (3.34). The linear relation with G_g makes the overall shape pretty similar. However, minimum point position is now dependent on V_{DS}, L, and V_p in opposition to the $S_T^{G_g}$ that mainly depended on V_p. It is important to point out that (3.34) implies that there is a maximum channel length that the ZTC occurs. This relation depends on the dependency of σ and α to L better developed as:

$$\phi_T^2 \cdot C_1 \cdot L^m = -C_2 \cdot \Delta V_p \cdot \alpha\left(L\right)\left(V_0 + V_{DS}\right), \tag{3.35}$$

where $C_1 = 8 \cdot \eta \cdot \pi \cdot t_{ox}$, $C_2 = \sigma_0 + \sigma_1 \cdot V_{SB}$, and ΔV_p the left-hand side of (3.34). Since L^m is a monotonic function and α a quadratic polynomial, if (3.34) occurs, then it must cross twice defining a region where the ZTC condition is fulfilled.

Figure 3.18 shows the pinch-off voltage at $G_{d_{ZTC}}$ obtained from BSIM 4v6 simulations. The lines lie inside the limit defined in (3.35). The short channel ZTC point comes in contrast with usual analog design practices that maximize L to increase linearity performance, with the trade-off of decreasing speed performance.

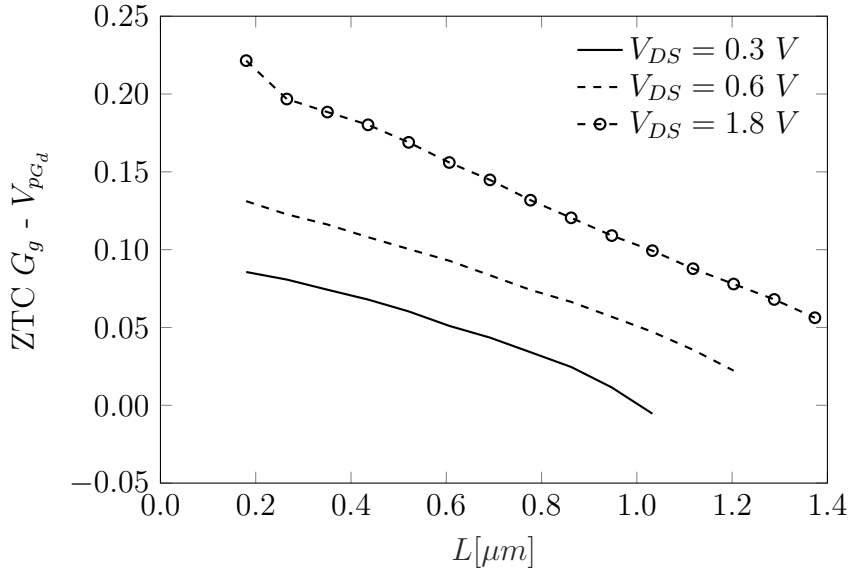


Figure 3.18: Extracted pinch-off voltage at $G_{d_{ZTC}}$ for different V_{DS} and channel lengths.

Another way of seeing this deduction is given that when L gets bigger, the DIBL effect gets smaller and CLM dominates on (3.31); $S_T^{G_d}$ approaches to $S_T^{G_d^{CLM}}$, which has no ZTC bias point. Both sensitivities for long and small channels are illustrated in Fig. 3.19.

3.3 Temperature Analysis of MOSFET Capacitances

When considering the frequency behavior of an analog circuit, the intrinsic transistor capacitances also need to be handled. Those capacitive coefficients are usually represented as three different capacitors connected between a three-terminal MOSFET (C_{gd}, C_{gs}, C_{ds}) [52] as shown on Fig. 3.20.

Figure 3.20 shows the calculated capacitances using the UICM model for a transistor with $N_B = 5 \cdot 10^{17}\ cm^{-3}$, $t_{ox} = 4\ nm$, Poly gate at 300 K for a $V_{DS} = 0.1V$. The C_{gd} and C_{gs} represent the capacitance at the created depleted region between drain/source and the bulk, and the C_{ds} capacitor is the equivalent capacitance between drain and source being able to achieve negative values due to the positive feedback created by the transistor transconductance.

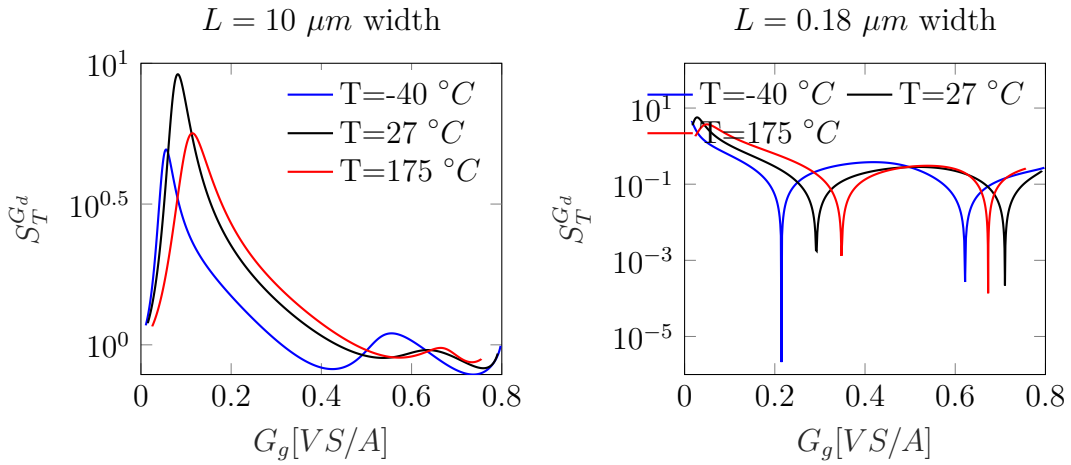


Figure 3.19: Extracted sensitivities for long channel ($L = 10\mu m$) (a) and short channel ($L = 0.18\,\mu m$) (b) at -40°C (Blue); 27°C (Black); 175°C (Red).

The UICM model defines the different MOSFET capacitances as [77]:

$$C_{gb} = \frac{\eta - 1}{\eta}\left(C_{ox}WL - C_{gs} - C_{gd}\right), \tag{3.36}$$

$$C_{gs} = \frac{2}{3}WLC_{ox}\frac{1+2\alpha}{(1+\alpha)^2}\frac{q_{IS}}{q_{IS}+1}, \tag{3.37}$$

$$C_{gd} = \frac{2}{3}WLC_{ox}\frac{\alpha^2+2\alpha}{(1+\alpha)^2}\frac{q_{ID}}{q_{ID}+1}, \tag{3.38}$$

$$C_{ds} = -\frac{4}{15}nC_{ox}WL\frac{1+3\alpha+\alpha^2}{(1+\alpha)^3}\frac{q_{is}}{1+q_{is}}, \tag{3.39}$$

$$C_{gg} = C_{gs} + C_{gd} + C_{gb}, \tag{3.40}$$

$$\alpha = \frac{q_{ID}+1}{q_{IS}+1}. \tag{3.41}$$

The C_{ab} is the capacitance between a and b terminals (source, drain, gate); α an indicator of the linearity degree of the profile of the inversion charge along the channel; and C_{gg} the total gate capacitance related to the MOS structure capacitance.

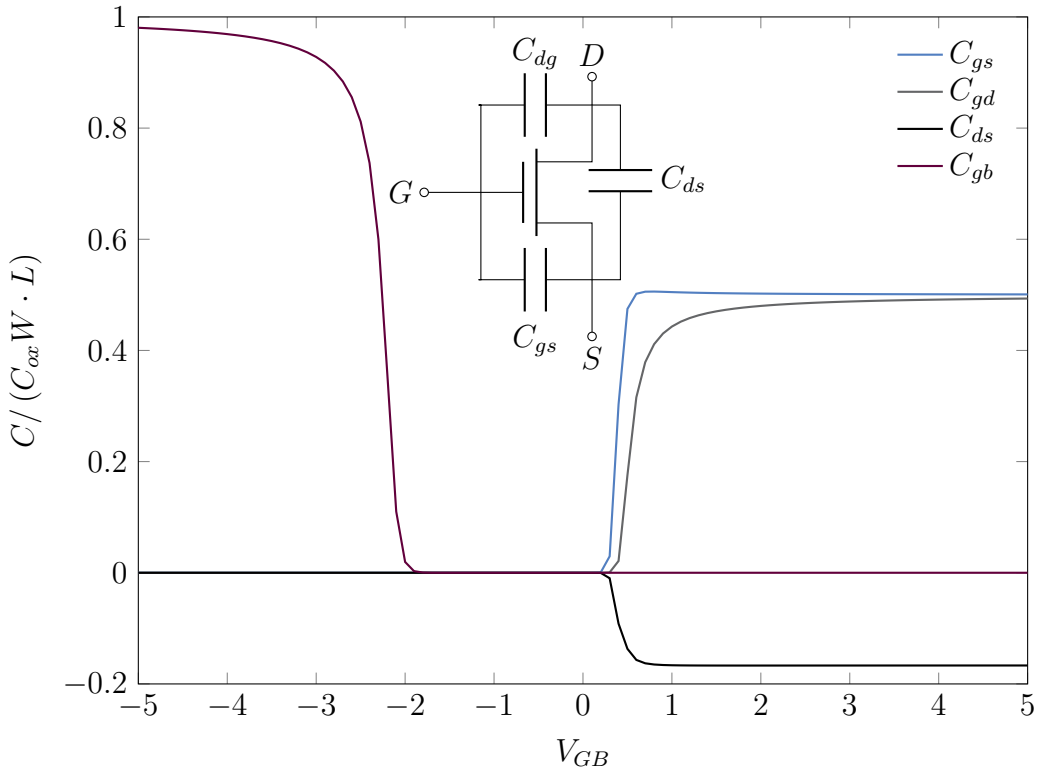


Figure 3.20: MOSFET capacitances on a three terminal transistor (a) and numerical calculations of them using the UICM model.

3.3.1 Varicap Temperature Analysis

One of the uses of the MOSFET capacitors is the Varicap, by connecting the drain, source and bulk at the same potential one can obtain a voltage controlled capacitance of value C_{gg}.

Figure 3.21 shows measurement data of a $100\mu m \times 100\mu m$ NMOS varicap capacitance at $27°C$, 75 $°C$, 125 $°C$ and 200 $°C$. As discussed for the MOS structure the capacitance has two distinct ZTC points in accumulation and moderate inversion. In most applications, transistors are biased in depletion and inversion regimes, since at those biasing condition the channel conductance decrease allowing the drain to source current. For this reason, most design-by-hand models usually consecrate more attention to those regimes to the detriment of the accumulation region [77]. For these reasons, hand analysis models can present less accurate results in accumulation. However, for RF application varicaps must be biased in accumulation since in this region the channel charge does not depend on recombination of carriers and therefore the capacitance does not suffer from

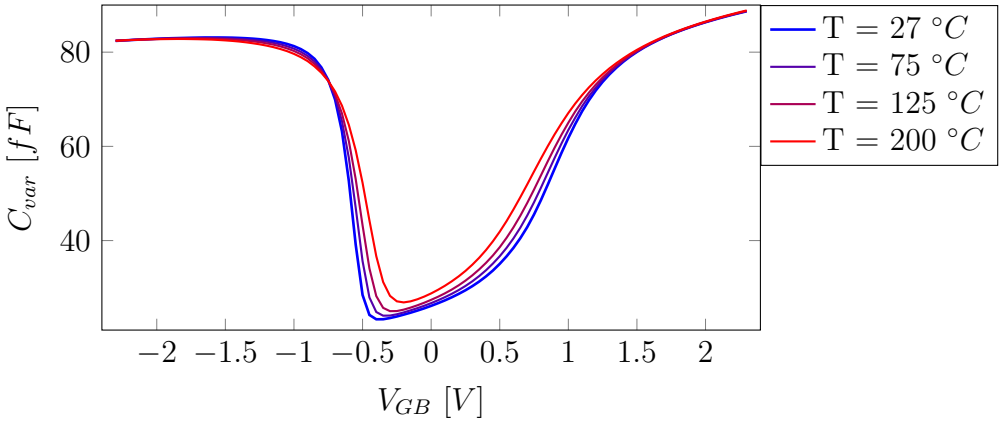


Figure 3.21: Measurement Data of a $100\mu m \times 100\mu m$ NMOS varicap capacitance at 27°C, 75 °C, 125 °C and 200 °C.

non-quasi-static effects.

Depletion and Inversion Analysis

Since at a varicap drain and source are connected $q_{is} = q_{id} = q_0$ by analyzing (3.40) and using the same hypothesis as [9] for the sub-threshold slope η and the validity of Boltzmann distribution at the working conditions, one may find that the temperature sensitivity of C_{var} as:

$$S_T^{C_{var}} = -q_0 \frac{V_p \cdot \left(S_T^{V_p} - 1\right)}{\phi_T \cdot (q_0 + 1)^2} \tag{3.42}$$

where V_p can be approximated by $(V_{GB} - V_{th})/\eta$. The presented analysis shows a similar temperature behavior between $S_T^{C_{var}}$ and $S_T^{G_g}$ (temperature normalized g_m/I_D parameter) [9], presenting a ZTC point at (3.43). Figure 3.22 illustrates this similarity by presenting $S_T^{C_{Var}}$ in Fig. 3.22(a) and $S_T^{G_g}$ in Fig. 3.22(b) for two dies of the same PMOS standard V_{th} transistor at temperatures from 27 °C to 200 °C. Both results are obtained from measurement data. Voltage derivatives are obtained by Euler differentiation and temperature gradients from a third order polynomial fitting.

$$V_p|_{S_T^{G_g}=0} = \frac{\alpha_{th} \cdot T}{\eta} \tag{3.43}$$

Since at negative V_{GB} drain current present a negative temperature coefficient, for lower temperatures, the current magnitude is comparable to the equipment

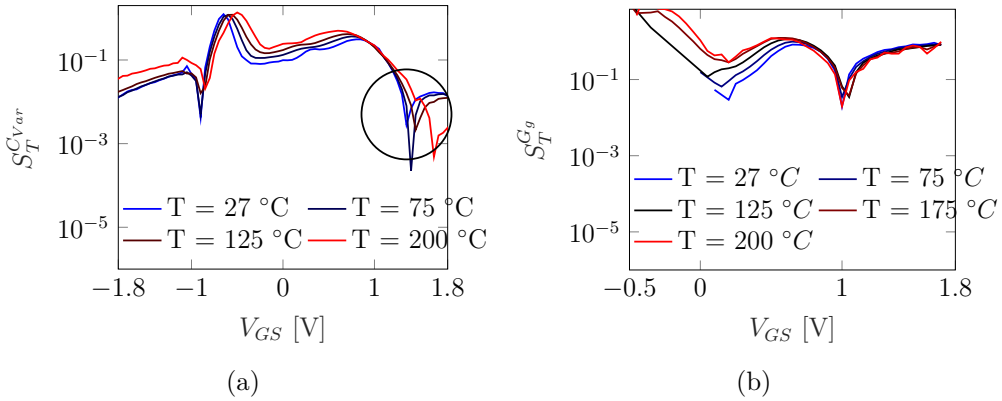


Figure 3.22: Extracted sensitivity from measurement data for C_{var} (a) and G_g (b).

noise floor and it was excluded from the plot in Fig 3.22(b). A standard V_{th} transistor is used since, for high-frequency oscillator, the varicap must be biased in accumulation to avoid capacitance-frequency modulation due to quasi-non-static effects. Figure 3.22 reinforces the discussed relation proposed parameter G_g and the total gate capacitance C_{gg} showing the same overall behavior for both parameters at $V_{GS} > 0$. The presented analysis can be extended for other transistor sizes, at least for a first-order model, since the sensitivity operator is unchanged over scaling, and transistor capacitances are known to scale linearly with gate area. This property makes the sensibility a suitable tool for evaluating transistor capacitance's temperature performance degradation due to scaling.

Accumulation Mode Analysis

Figure 3.22(a) highlights a second ZTC point that happens close to the accumulation region ($V_{GS} < V_{FB}$), in this region the pinch-off voltage approximation $V_p \approx (V_{GS} - V_{th})/\eta$ does not hold anymore. In order to further investigate this ZTC point, one may take the deep-accumulation approximation given by:

$$Q_b \approx -C_{ox}\gamma\phi_t e^{\frac{\psi_s}{2\phi_t}}, \tag{3.44}$$

$$C_b = \frac{\partial Q_b}{\partial \psi_s} = -\frac{Qb}{2}, \tag{3.45}$$

where Q_b is the bulk charge; C_b the bulk capacitance; C_{ox} the oxide capacitance; ϕ_t the thermal voltage; γ the bulk-effect parameter; and ψ_s the surface potential. By using this approximation, one may calculate the surface potential in relation to the $V_{GB_0} = V_{GB} - V_{FB}$ as:

$$\psi_s = 2\phi_t W_0\left(\frac{\gamma}{2}e^{\frac{V_{GB_0}}{2\phi_t}}\right) + V_{GB_0}, \tag{3.46}$$

where W_0 is the principal branch from the Lambert-W function. The total capacitance C_{Var} is given by the series association between C_b and C_{ox}. A sufficient condition for the ZTC point at deep-accumulation can be obtained by

$$\frac{\partial C_b}{\partial T} = 0. \tag{3.47}$$

Using the surface potential model and considering a linear flat-band voltage temperature dependency with a temperature coefficient α_{fb} one may find the ZTC condition for C_{var} in accumulation as:

$$V_{GB} = \alpha_{fb}T + V_{fb} - (2\ln(\gamma) + 1)\,\phi_t, \tag{3.48}$$

$$\alpha_{fb} = \frac{1}{T}\left(\frac{E_G\,(T=0)}{2\cdot q} - \phi_F\right). \tag{3.49}$$

For Silicon, the extrapolated bandgap at absolute zero ($E_G\,(T = 0\ K)\,/q$) is 1.12 eV, for usual doping levels, the bulk Fermi level ϕ_F is not very apart from the middle gap ($E_G\,(T = 0\ K)\,/2\cdot q$) making the flat-band voltage (V_{FB}) temperature derivative very low and therefore the accumulation ZTC point very close to V_{FB} and mostly dependent of the substrate doping.

3.3.2 C_{gs} Temperature analysis

As highlighted in Fig. 3.20 in usual bias conditions (depletion and inversion) the MOSFET largest capacitance is the C_{gs}. This capacitor have an important influence at the transistor speed and its temperature sensitivity needs to be calculated. By taking the temperature sensitivity from C_{gs} [see details in (3.37)] one may find:

$$\begin{aligned} S_T^{C_{gs}} =& 2\alpha S_T^{\alpha}\left(\frac{1}{1+2\alpha} + \frac{1}{1+\alpha}\right) + \\ & S_T^{q_{IS}}\left(1 - \frac{q_{IS}}{q_{IS}+1}\right) \end{aligned} \tag{3.50}$$

$$S_T^{\alpha} = \frac{q_{ID}S_T^{q_{ID}}}{q_{ID}+1} - \frac{q_{IS}S_T^{q_{IS}}}{q_{IS}+1} \tag{3.51}$$

The α parameter can be interpreted as the linearity degree from the inversion charge density along the channel whereas it varies from $\alpha \approxeq 1$ in weak inversion and $\alpha \to 0$ in strong inversion. This asymptotic behavior of α entails a more

important impact of the overall temperature sensitivity in weak and moderate inversion. Figure 3.23(a) and 3.23(b) show the S_T^{α} for $V_D = 1V$ and $V_D = 0.6V$, it is noticeable that the ZTC point at V_{GB} close to V_{th} indicating a moderate inversion ZTC point. In moderate inversion the source and drain normalized charges have almost the same value making α close to unity, and nulling (4.29). At this condition of $\alpha \approx 1$ and $q_{is} \approx q_{id}$, one may find that the ZTC condition is given by:

$$S_T^{C_{gs}} \approx \frac{V_p \cdot \left(S_T^{V_p} - 1\right)}{\phi_t \left(q_{is} + 1\right)^2}. \tag{3.52}$$

The same behavior discussed on Sec. 3.3.1 for the total gate capacitance is found for C_{gs}. The C_{gs} sensitivity is shown in Fig. 3.22(a), the presence of the same ZTC points indicate a very close relationship between the G_g parameter and the MOSFET capacitors, making it a good starting point to bias transistors in which the capacitance interfere in the quantity of interest at this ZTC point.

3.4 Conclusion

In this chapter, a novel concept of temperature normalized g_m/I_D parameters was proposed to allow a temperature-aware g_m/I_D. The proposed parameters (G_g, G_d) can be used in a g_m/I_D framework on a design-by-experiments, analytical, or mixed design flow. Besides, the MOSFET capacitances temperature behavior and ZTC points where discussed. The temperature sensitivity of the capacitances, and the moderate inversion ZTC point present close relation to the proposed temperature normalized g_m/I_D. This results allows an analysis of temperature effects on circuit parameters in an early design stage using the g_m/I_D methodology. This thesis proposal was validated on simulation and measurement data for a 0.18 μm SOI technology in a temperature range from -40 $^{\circ}C$ to 200 $^{\circ}C$.

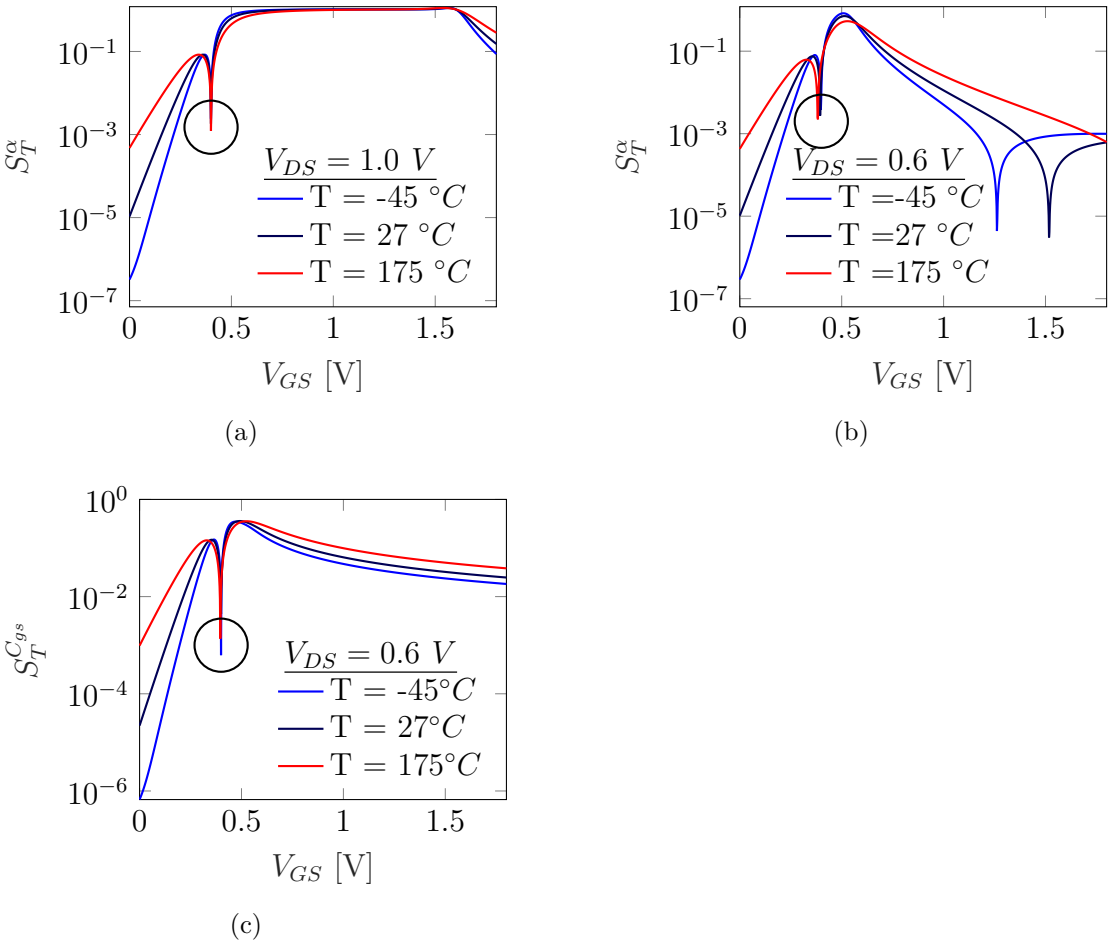


Figure 3.23: Extracted sensitivity from UICM model for transistors presenting the same physical parameters as low V_{th} transistor for (a) α at $V_D = 1$ V, (b) α at $V_D = 0.6$ V and (c) C_{gs} at $V_D = 0.6$ V.

Chapter 4

A Temperature-Aware Methodology Applications: A Study Case

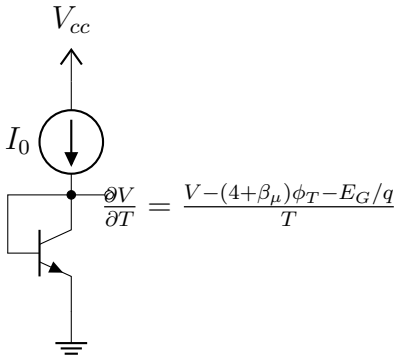
In the last chapters, the proposal for achieving a temperature-aware design methodology was reviewed and developed. This chapter will explore some examples on how the temperature normalized g_m/I_D parameters can be used to achieve low temperature sensitivity circuits. The shown examples are common analog circuits in most electronics designs and demonstrate how the temperature analysis can be easily incorporated in a traditional g_m/I_D workflow. For each circuit presented, a comparison with the traditional g_m/I_D approach is presented to highlight the trade-offs of the proposed technique.

4.1 Bandgap Voltage Reference

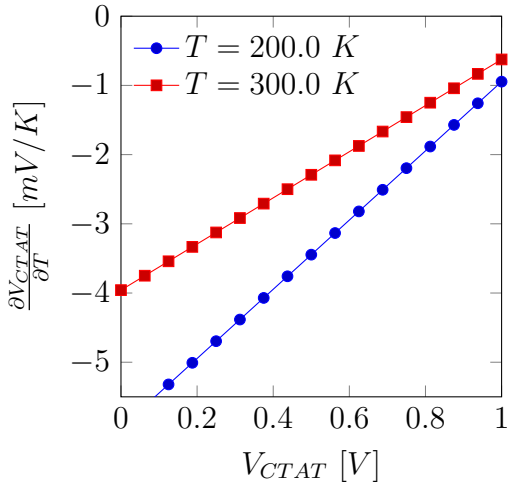
The presented temperature normalized g_m/I_D technique on the last chapter, as the traditional g_m/I_D methodology, allows the design of circuits meeting reliable performance such as gain, distortion, noise, etc. However, to achieve such performance a constant bias over temperature must be first achieved. When discussing temperature-aware design, argubly the most known circuit that achieve a temperature independent parameter is the Bandgap voltage reference.

As seen on Chap. 2, the semiconductor bandgap present a complementary to absolute temperature behavior (CTAT). When biasing diode-connected bipolar junction transistor (BJT) with an constant current source, the collector voltage will present a temperature coefficient proportional to the material bandgap [78]

Similarlly to the CTAT voltage, an proportional to absolute temperature (PTAT) can be obtained in a similar matter as presented on Fig. 4.1. The base of the



(a)



(b)

Figure 4.1: Traditional CTAT Voltage Generation and the theoretical temperature coefficient at different temperatures for $\beta_\mu = -1.5$.

bandgap voltage reference is to linearly combine a CTAT voltage with a PTAT voltage such as the two temperature coefficients are compensated presenting an output voltage equal to $V_{BG} = \frac{E_G}{q} + (4 + \beta_\mu)\,\phi_T$ [78].

In modern MOS technologies, even though Bi-CMOS technologies exists, the BJT is usually replaced by a MOS transistor biassed in weak inversion, that present similar electrical and thermal behavior. Besides, the "traditional" bandgap voltage reference present a voltage that is thigh to values close to the bandgap energy of the semiconductor. New topologies solves those problems and allow not only a reference voltage insensitive to temperature but also power-supply variations [79]. One alternative to generate the PTAT and CTAT voltages in modern MOS technology is the self-cascode composite transistor (SCCT). Figures 4.2(a) and 4.2(b) illustrates respectively the NMOS and PMOS SCCT implementations.

The SCCT have many application in analog circuits, is as an equivalent resistor of length $(L_1 \cdot (m+1))$ occupying less area than a transistor of this length. By assuming that both transistors are in weak inversion and $V_{DS} > 3\phi_t$, the node V_o can be expressed by:

$$\begin{cases} V_o = \eta\phi_t \ln\left(\frac{I_{DS1}\cdot m}{I_{DS2}}\right) & \text{NMOS} \\ V_o = V_{GS2} - \eta\phi_t \ln\left(\frac{I_{DS2}\cdot m}{I_{DS1}}\right) & \text{PMOS} \end{cases} \tag{4.1}$$

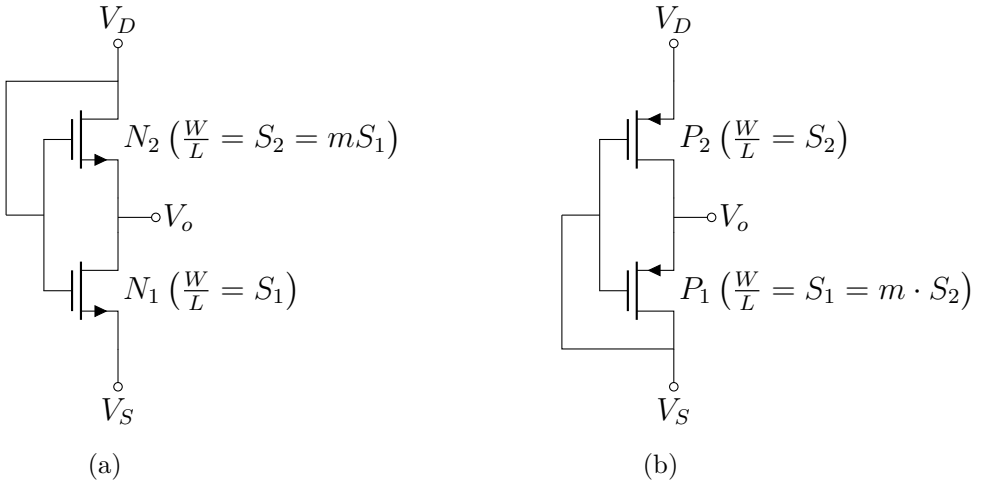


Figure 4.2: Self-Cascode Composite Transistor in NMOS (a) and PMOS (b) versions.

4.1.1 Temperature Analysis

In weak inversion, the drain to source current can be expressed as $I_{DS} = \eta\phi_t g_m$. By replacing I_{DS} in (4.1) and dividing the numerator and denominator by I_{DS}/ϕ_t the V_o can be expressed as a function of the temperature normalized g_m/I_D parameters as:

$$\begin{cases} V_o = \eta\phi_t \ln\left(\frac{G_{g_1}\cdot m}{G_{g_2}}\right) & \text{NMOS} \\ V_o = V_{GS2} - \eta\phi_t \ln\left(\frac{G_{g_2}\cdot m}{G_{g_1}}\right) & \text{PMOS} \end{cases} \tag{4.2}$$

Once the substitution is done the temperature sensitivity of V_o can be obtained as:

$$\begin{cases} S_T^{V_0} = 1 + \left(S_T^{G_{g_1}} - S_T^{G_{g_2}}\right)\frac{G_{g_2}}{G_{g_1}\cdot m} & \text{NMOS} \\ S_T^{V_o} = \frac{V_{GS_2}\left[1+\left(S_T^{G_{g_2}} - S_T^{G_{g_1}}\right)\frac{G_{g_1}}{G_{g_2}\cdot m} + S_T^{V_{GS_2}}\right] - V_{GS_2}\cdot S_T^{V_{GS_2}}}{V_o} & \text{PMOS} \end{cases} \tag{4.3}$$

By biasing the NMOS circuit in $G_{g_{ZTC}}$ the temperature sensitivity of V_o becomes 1 indicating a linear temperature behavior, by imposing $S_T^{V_o} = 1$ at the $G_{g_{ZTC}}$ vicinity on the PMOS circuit, one may find the condition in which V_o presents a linear temperature behavior as:

$$V_{p1} = V_{p_2} - \phi_T \frac{4mG_{g_2}\left(S_T^{V_{GS_2}} - 1\right)(V_o - V_{gs_2})}{G_1 V_{GS_2}} \approx V_{p_2} \tag{4.4}$$

where V_{p1} and V_{p2} are the pinch-off voltages from transistors P_1 and P_2. Equation (4.4) indicate that for maximum temperature linearity at the vicinity of G_{gZTC} the PMOS SCCT: $V_o \approx \frac{V_D - V_S}{2}$. For XT018 technology, the g_m/I_D value at 27 $°C$ in which G_{gZTC} occurs is around $g_m/I_D \approx 6$, by imposing the maximum linearity for temperature dependency $\left(S_T^{V_o} = 1\right)$ on both CTAT and PTAT one get the following results:

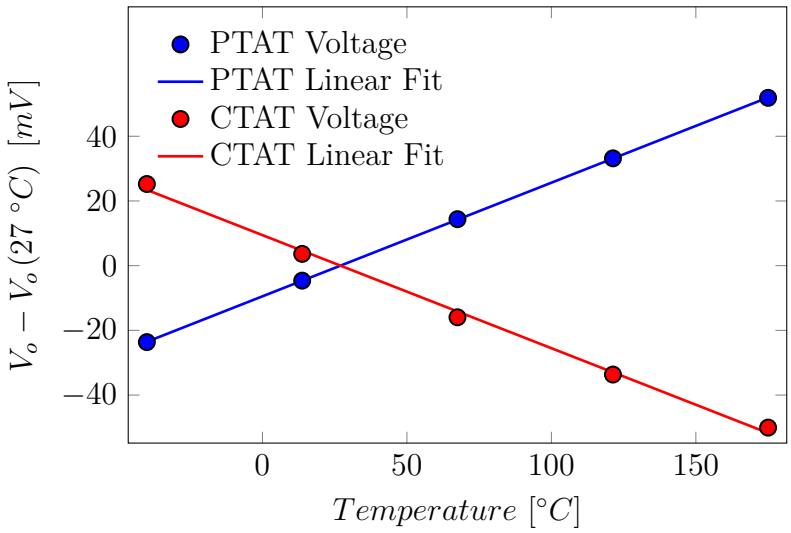


Figure 4.3: PTAT and CTAT voltages when designed for maximum linearity.

Once the two voltages are generated one possibility to add the them is by using a voltage to current converter as illustrated on Fig. 4.4. The operational amplifier assure that voltage on the resistor R to be equal to V_{ref}, and therefore making the I_{DS} on transistors M_1 proportional to the reference voltages. Since the current to voltage conversion factor is given by the resistance value a P_+ non-salicided poly silicon resistor, was chosen, presenting a temperature coefficient of $-0.04\ [10^-3/K]$.

Figure 4.5 shows the simulation results for the generated PTAT and CTAT currents. The V-I converter MOSFET was sized to be in $I_{DS_{ZTC}}$ with an drain current at 27 $°C$ equal to the bias current of the CTAT and PTAT SCCT. Since the resistors does not only present a slight non linear (spectre models allows for quadratic temperature dependency) the linearity was slightly . In order to compare the linearity both voltages and currents where fitted to a second-order polynomial, the quadratic terms of the fitted polynomials are here presented on Tab. 4.1.

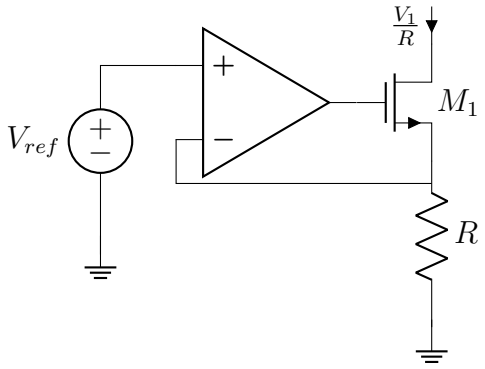


Figure 4.4: Voltage to Current Converter.

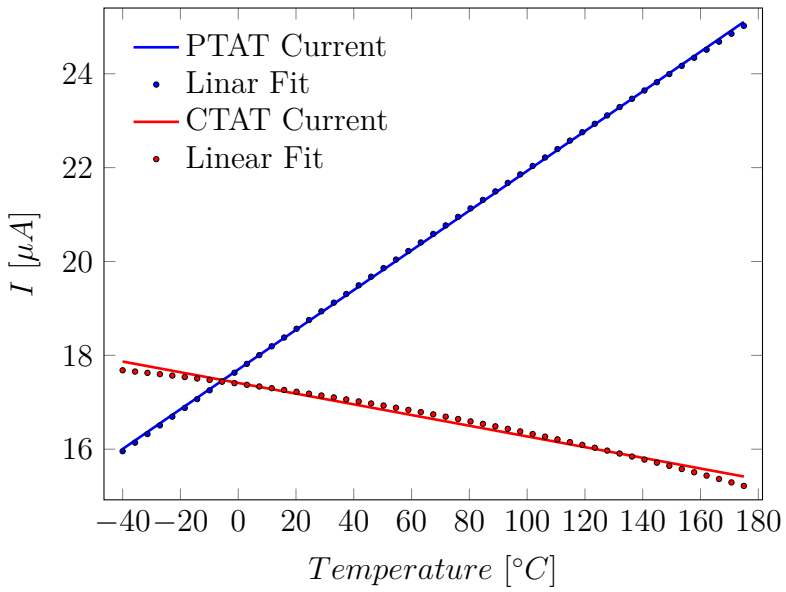


Figure 4.5: PTAT and CTAT Currents after the voltage to current converters.

Table 4.1: Linearity Comparison Between Current and Voltage Generators.

	PTAT	CTAT
Voltage	$0.055{\cdot}10^{-3}\ K^{-1}$	$0.778{\cdot}10^{-3}\ K^{-1}$
Current	$3.158{\cdot}10^{-3}\ K^{-1}$	$-0.200{\cdot}10^{-3}\ K^{-1}$

4.1.2 Results

Both currents can be added using simple current mirrors that are sized with W/L ratio proportional to the inverse of the temperature coefficient. The result current is than injected in the same low temperature coefficient resistor, the complete circuit schematic is shown in Fig. 4.6.

Temperature-awareness is often estimated by the temperature coefficient (TC). However, the usual definition considers 27 $°C$ as a reference temperature. Since the goal of the method is to allow a wide temperature working range, in contrast to a circuit working on ambient temperature, another approach is taken in this work. To this end, one may define a modified TC figure of merit as:

$$T_{C_{eqq}}(A_v) = \frac{\max(A_v) - \min(A_v)}{A_v\,(\text{mean}(T))\,(T_{max} - T_{min})} \tag{4.5}$$

Using the metric in (4.5) , the output voltage present a 18.23 $ppm/°C$ TC from -40 $°C$ to 175 $°C$.

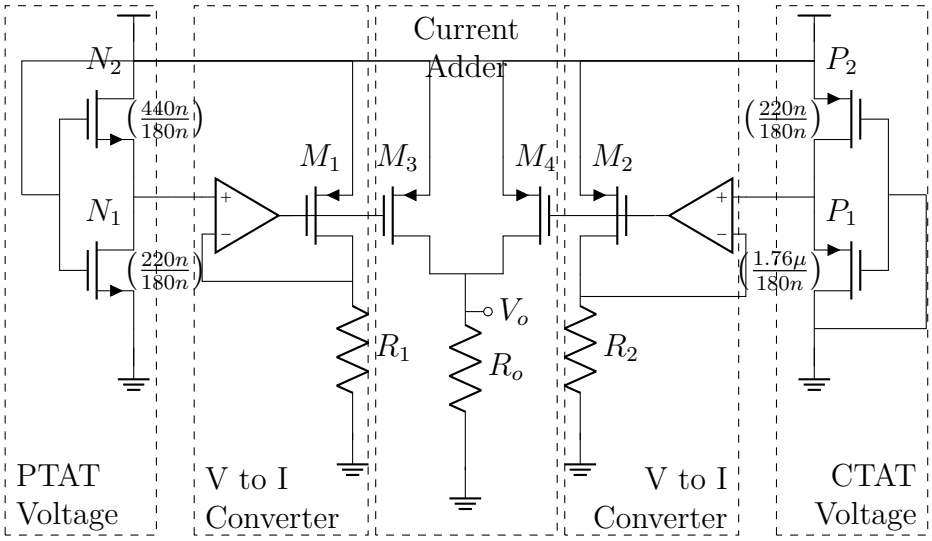


Figure 4.6: Proposed bandgap circuit.

The obtained power supply rejection ratio is 28.91 dB as show in Fig. 4.8.

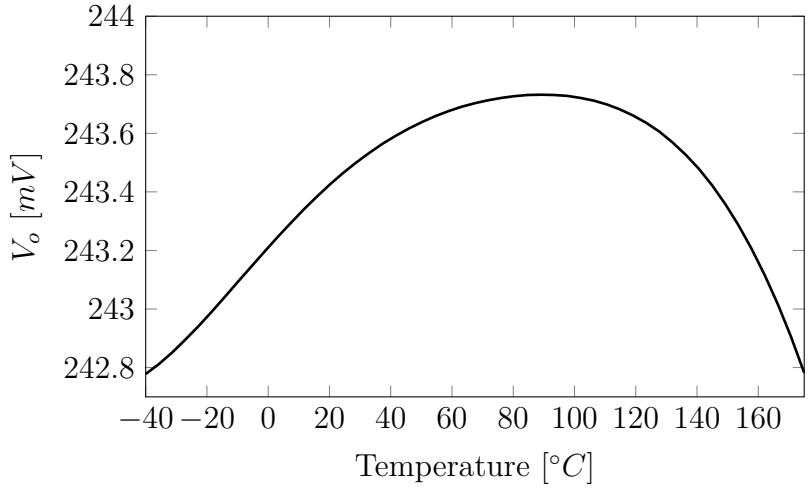


Figure 4.7: Simulated bandgap reference voltage from -40 °C to 175 °C.

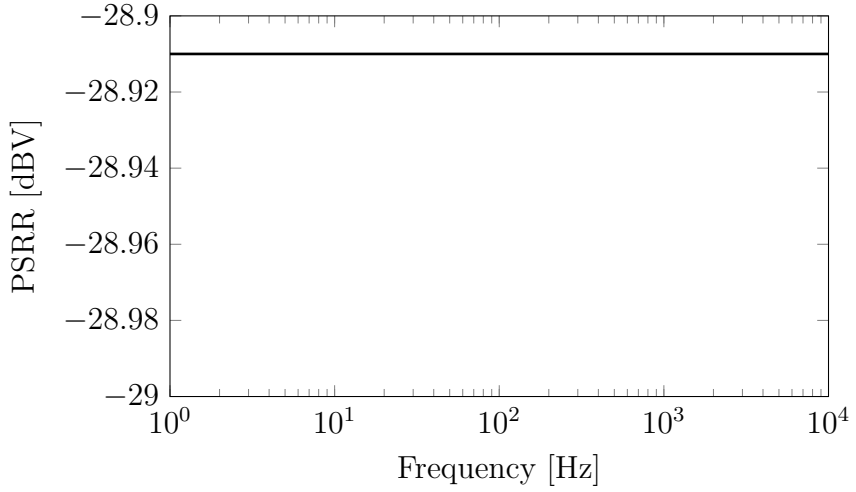


Figure 4.8: Simulated Power Supply Rejection Ratio.

Bandgap performance is now tested over process variations. Figure 4.10 shows the output voltage for the worst and typical transistor and resistor corners considering a 3σ variation.

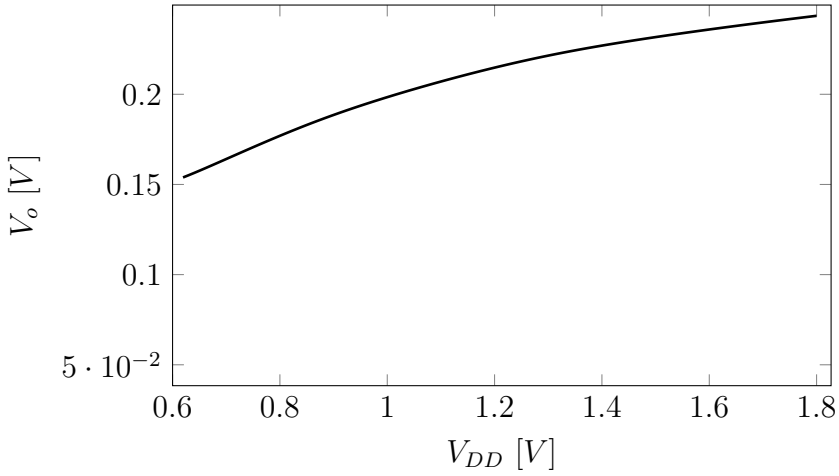


Figure 4.9: Output Voltage Dependency to power supply voltage.

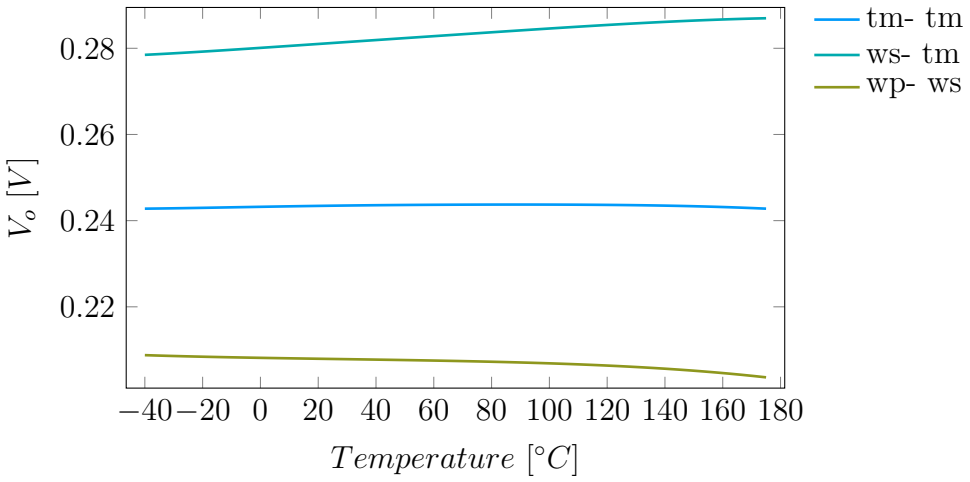


Figure 4.10: Corner Simulation over temperature for the output voltage, first corner corresponds to the transistors corner and second to the resistors.

4.1.3 Conclusions

A simple bandgap voltage reference was designed and analyzed using the temperature normalized g_m/I_D parameters. The PTAT and CTAT circuit sides analytical temperature behavior close to the $G_{g_{ZTC}}$ where developed and could be optimized for maximum linearity. The developed circuit present an temperature coefficient of 18.23 $ppm/°C$ at typical corner in a temperature range from -40 $°C$ to 175 $°C$.

4.2 Differential Amplifier

Often used in design methodology studies as a testing circuit, the PMOS differential pair OTA with active load [28][61] is illustrated in Fig. 4.11. The circuit is composed of a PMOS differential pair with transistors M_{2A} and M_{2B}, an NMOS active load, and a current mirror biasing circuit (transistors M_{3A} and M_{2B}). The differential voltage gain is obtained by:

$$|A_v| = \frac{g_{m_2}}{g_{ds_1} + g_{ds_2}} \tag{4.6}$$

4.2.1 Voltage Gain Temperature Analysis

By multiplying (4.6) numerator and denominator by ϕ_t the differential voltage gain as a function of the temperature normalized g_m/I_D and its temperature sensitivity can be obtained by:

$$|A_v| = \frac{G_{g2}}{G_{d1} + G_{d2}}, \tag{4.7}$$

$$S_T^{A_v} = S_T^{G_{g2}} - \frac{S_T^{Gd1} \cdot G_{d1} + S_T^{Gd2} \cdot G_{d2}}{G_{d1} + G_{d2}}. \tag{4.8}$$

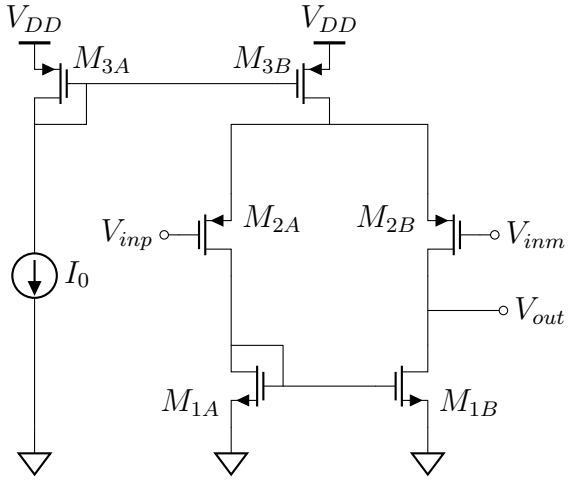


Figure 4.11: PMOS differential pair with active load.

Imposing $M_{2A,B}$ and $M_{1A,B}$ to be at the vicinity of G_{gZTC} developed in (3.15), (4.8) simplifies to

$$S_T^{A_v} = \frac{1}{4} \frac{(TV_{th2}\,\alpha_{th} - V_{p2})\,\sigma_2\,(-\sigma_1\,\eta_2 + \eta_1)}{\phi_T\,(\sigma_2\eta_1 + \sigma_1\eta_2)}. \tag{4.9}$$

To reach $A_{v_{ZTC}}$, one must have either $V_{p2} = V_{p_{ZTC}}(\eta_2 - 1) = 0.08$ V or make $\sigma_1 = \frac{\eta_1}{\eta_2} = 1.0123$. Since it is not possible in XT018 technology to have such a big σ_1 DIBL coefficient, $M_{2A,B}$ is biased at $V_p = 0.08$ V. In order to compensate the (3.15) temperature dependency, the current-source temperature coefficient was chosen such as the temperature coefficient of $V_{D_{M2,A}}$ being $\frac{\alpha_{th}}{\eta}$. The transistors biasing were chosen to be at $I_{DS_{ZTC}}$ point, and sizing was therefore calculated.

4.2.2 Amplifier Gain-Bandwidth Product

When considering a differential amplifier, another key parameter is the gain-bandwidth product (GBW). For the circuit illustrated on Fig. 5.11 the GBW is given by:

$$\text{GBW} = \left[\frac{g_m}{I_D}\right]_2 \cdot \frac{I_{D_2}}{2\pi C_L} \tag{4.10}$$

where C_L is the capacitance seen at the output node where taken with a value of 100 fF and zero temperature coefficient. The capacitance choice is made based on an average transistor input capacitance from the technology.

Since to minimize the temperature effects on the amplifier open-loop gain transistors M_{2_A} and M_{2_B} are biased at the vicinity of $G_{g_{ZTC}}$ the temperature sensitivity of $(g_m/I_D)_2$ can be obtained by considering the G_g definition

$$\frac{g_m}{I_D} = \frac{G_g}{\phi_T} \tag{4.11}$$

By calculating the temperature sensitivity of (4.11) leads to

$$S_T^{\frac{g_m}{I_D}} = S_T^{G_g} - 1 \tag{4.12}$$

That at G_g ZTC, becomes $S_T^{\frac{g_m}{I_D}} = -1$. Using the sensitivity operator property

$$f(x) = A \cdot x^k \rightarrow S_x^{f(x)} = k, \tag{4.13}$$

The g_m/I_D temperature behaviour at $G_{g_{ZTC}}$ is

$$\left.\frac{g_m}{I_D}(T)\right|_{G_{g_{ZTC}}} = \frac{A}{T} \tag{4.14}$$

Since the circuit is symmetric the $I_{D_2} = I_{bias}/2$. Therefore the GBW temperature behavior can be estimated by

$$\text{GBW}(T) = \frac{(g_m/I_D)_2|_{T_0} \cdot T_0}{T} \cdot \frac{I_{bias}(T_0) + \text{TC}(T - T_0)}{4\pi C_L} \tag{4.15}$$

Figure 4.12 illustrates the simulated GBW temperature behavior given by (4.15), notice that the presented results follow a $1/T$ behavior as predicted by (4.15).

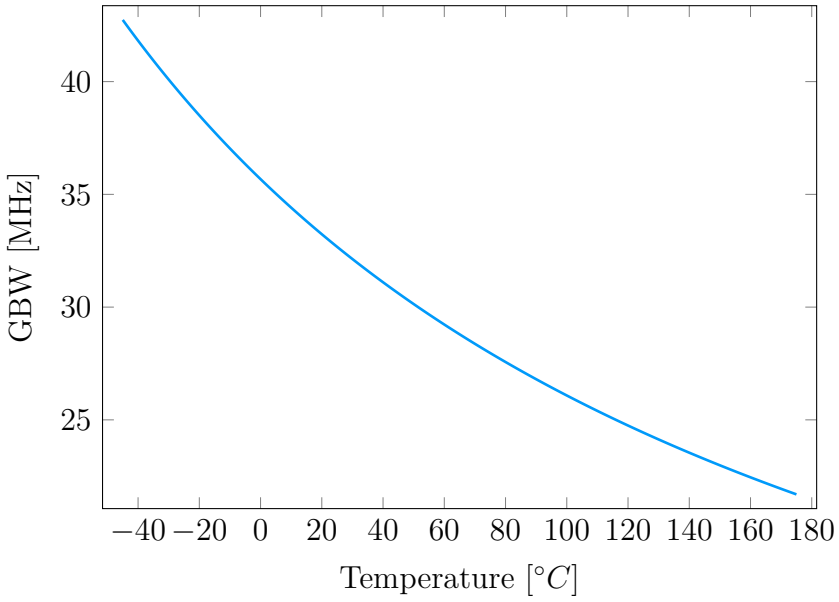


Figure 4.12: GBW from the proposed amplifier, as estimated by (4.15) and simulated at spectre(To Do) from -45 $°C$ to 175 $°C$

Since the bias current temperature coefficient is very small compared with the g_m/I_D temperature variation, by taking $T_0 = 0.5\,(T_{max} + T_{min})$ the temperature coefficient of GBW can be estimated by:

$$\mathrm{TC_{GBW}} = \frac{(g_m/I_D)_2|_{T_0} \cdot I_{bias}\,(T_0)}{4\pi C_L} \cdot \frac{T_{max}^2 - T_{min}^2}{2 \cdot T_{max} \cdot T_{min}} = 3321 \text{ ppm}/°C \tag{4.16}$$

4.2.3 Comparison to Strong Inversion Solution

The obtained voltage gain is illustrated in Fig. 4.13 at the typical corner and the worst corner boundary defined by WZ and WO corners. It is essential to point out that the temperature coefficient of the bias current is negative, the temperature-aware solution does not come with a power consumption (9.2 μW at 27 $°C$) increase. This is an essential feature for novel, temperature-aware, low-power IoT circuits.

To compare the novel technique with the strong inversion, "traditional", one may take the methodology given in [73] for the same topology. All transistors'

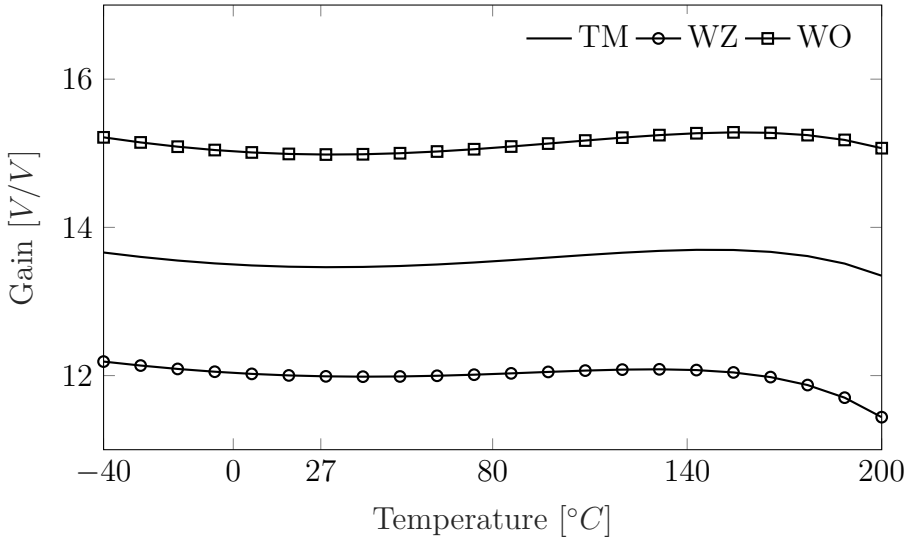


Figure 4.13: Gain variation over temperature in different corners of the amplifier design with the novel methodology.

lengths were made $3 \cdot L_{min}$ for linearity improvement. The g_m/I_D of the active load, the differential pair, and the current mirrors were chosen to be 4 to decrease g_{ds}/I_D, and therefore increase gain, while keeping V_{Dsat} small enough for $M_{1,2,3}$ being saturated. The electrical simulations result from the classically designed circuit can be seen in Fig. 4.14. Using (4.5) the obtained value of $T_{C_{eqq}}$ of 2364.46 ppm/°C for the strong inversion solution, compared with on typical corner for the proposed circuit that has a $T_{C_{eqq}}$ of 107.33 ppm/°C the proposition roughly a 22 times smaller $T_{C_{eqq}}$.

4.2.4 Results

The different sizing and performance figures of the two designs are summarized in Tab. 4.2 and also compared to [65] results. The temperature-awareness still present even under process variations, Fig. 4.13 illustrates the gain variation over temperature at the typical and the two worst $T_{C_{eqq}}$ corners. Since the mean gain depends on g_{mPMOS}/g_{dsNMOS} parameter, it is expected that the WZ and WO corners present a higher variation on the mean gain. However, this variation on the mean gain does not affect the small temperature sensitivity of A_v over corner simulations, presenting 260 ppm/°C and 82.42 ppm/°C WZ and WO corners respectively.

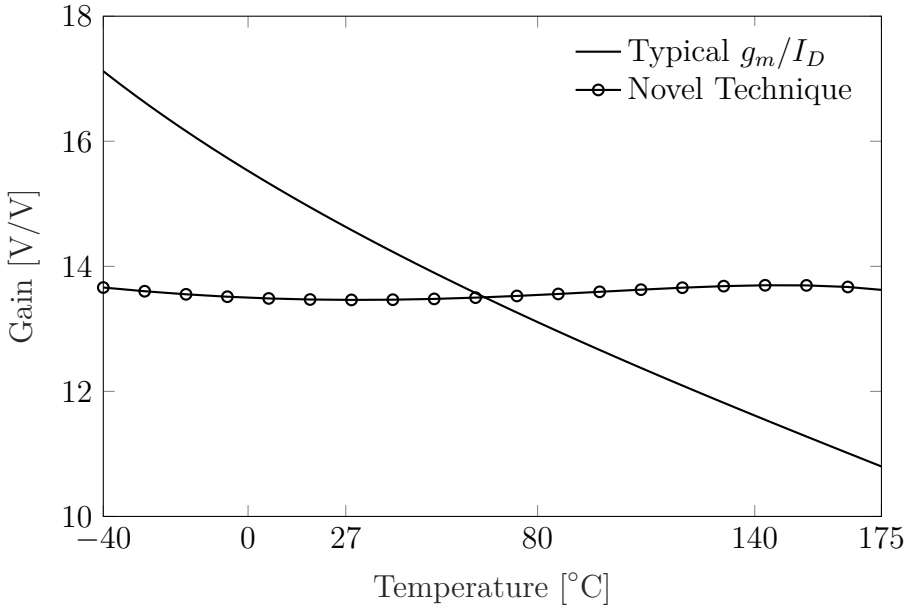


Figure 4.14: Comparison with gain over temperature using typical strong inversion and the proposed in TT corner.

Table 4.2: Circuit Dimensions and Parameters

	Novel Technique	SI	[65] Micropower	[65] High Gain	[65] HF 3 μm	[65] HF 2 μm
$^{W}/_{L}\vert_{M1,A,B}$	1.8/0.18	1.5/0.54	30/3	300/6	600/3	400/2
$^{W}/_{L}\vert_{M2,A,B}$	0.45/0.18	4.5/0.54	33/3	150/6	300/3	60/2
$^{W}/_{L}\vert_{M3,A,B}$	0.36/0.18	4.5/0.54	-	-	-	-
Bias TC $[nA/°C]$	-19.5	0	0	0	0	0
Pss [W]	9.2 μ	240 μ	3.6 μ	100 μ	29 m	12 m
Gain TC [ppm/$°C$]	107.33	2159	2917	3151	4069	4674
Ft TC [ppm/$°C$]	3321	-	3719	3719	2132	2686.32
V_{DD} $[V]$	1.8	1.8	1.2	2.0	4	4

4.2.5 Temperature Sensitivity in Closed-Loop Operation

Differential pairs with active load, and its variations, are usually used as a the core component for the design of operational amplifiers or operational transconductance amplifiers. They are often used in closed loop systems that are inherently less sensible to parameters variations, with the expanse of increased power consumption.

This sensitivity reduction can be shown by taking a classical closed-loop transfer function and calculating the closed-loop transfer function sensitivity ($H(s)$), one may find:

$$H(s,T) = \frac{A(s,T)}{1 + A(s,T) \cdot B(s,T)}, \tag{4.17}$$

$$S_T^{H(s,T)} = -\left(\frac{S_T^{A(s,T)}}{A(s,T) \cdot B(s,T) + 1} \right), \tag{4.18}$$

since the feedback is usually a capacitive or resistive network, with very little or nil temperature dependency; their temperature dependency was neglected. Equation (4.18) shows that closed-loop sensitivity is expected to be reduced by the sensitivity transfer function $\left((A(s,T) \cdot B(s,T) + 1)^{-1} < 1 \right)$. Since the loop-gain ($B(s)$) is chosen to fit the required closed-loop gain, one may find that in order to minimize the temperature sensitivity a high-gain amplifier ($A(s)$) is needed. To achieve high-gain amplifiers, techniques such as gain-boosting and multistage amplifiers are mandatory. This design choice intrinsically increases power consumption, which could be prohibitive in new low-power IoT devices.

In order to quantify this trade-off, one may take as an example a multistage (N stages) design using as a basic cell the non-optimized amplifier presented in the paper with a temperature sensitivity of 2364.46 ppm/ $^\circ C$ with a open loop gain of 16 V/V at 27 $^\circ C$ and a 240 μW power consumption illustrated in Fig.4.15. The total gain for N-stages is thus estimated in (4.19). The multistage amplifier gain sensitivity to temperature is then obtained according to (4.20).

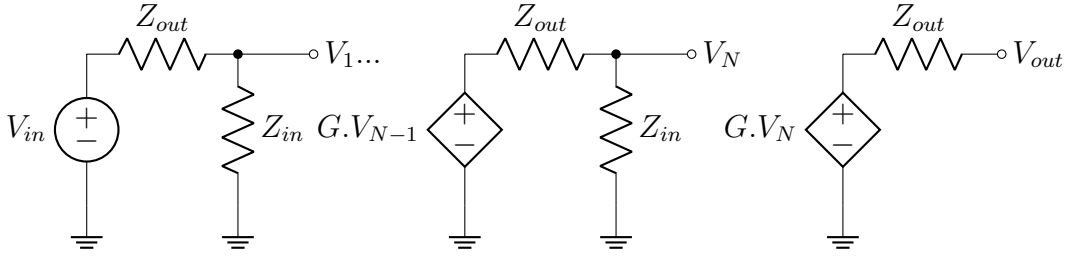


Figure 4.15: Multiple Stage Amplifier Model.

$$A(s,T) = \frac{V_{out}(s,T)}{V_{in}(s,T)} = G(s,T)^N \cdot \left(\frac{Z_{in}(s,T)}{Z_{in}(s,T) + Z_{out}(s,T)} \right)^N < 16^N \tag{4.19}$$

$$S_T^{A(s,T)} = N \cdot S_T^{G(s,T)} + N \cdot S_T^{\frac{Z_{in}(s,T)}{Z_{in}(s,T)+Z_{out}(s,T)}} > N \cdot 2364.46 \text{ppm/}^\circ\text{C} \tag{4.20}$$

Assuming this multistage amplifier example, one may choose a closed-loop gain of 10 V/V,thus the closed-loop sensitivity is given by

$$S_T^{H(s,T)} = \frac{N \cdot 2364.46 + N \cdot \left(S_T^{\frac{Z_{in}(s,T)}{Z_{in}(s,T)+Z_{out}(s,T)}} \right)}{1 + \frac{16^N}{10}} \tag{4.21}$$

To obtain a sensitivity comparable to the typical corner, one may calculate that the needed number of stages is 3 resulting in power consumption of roughly 750 μW. Besides, some applications such as analog front-ends [80] demand a open-loop configuration and may deeply suffer from temperature effects.

4.2.6 Conclusion

An PMOS differential pair with active load was presented using the temperature normalized g_m/I_D parameters, having an equivalent temperature coefficient of 107.3ppm/K for its gain performance having a 22 times improvement to the traditional g_m/I_D methodology. The novel temperature stabilization methodology is shown to hold even with process variability. This is the first demonstration of a temperature-independent gain for an extended temperature range suitable for smart vehicles to the best of our knowledge.

4.3 Active Inductance VCO

Oscillators are often classified into five main categories (RC, Ring, LC, Crystal, and MEMS). In [81], a survey indicates that LC-based oscillators present an overall better performance for L-band applications. Lu *et al.* presented a very wide tuning range LC-based oscillator with an active inductance and low noise performance [10]. Figure 4.16 illustrates the VCO under analysis, composed by an active inductor (L_{active}), a MOS capacitor (C_{var}), and a negative impedance (G_{comp}).

The active inductance L_{active}, controlled by V_{ctrl1}, allows a very wide tuning range. However, it can present a large temperature variation [82]. The tunable MOS varicap C_{var} is controlled by V_{ctrl2}. The G_{comp} works as a negative resistance to nil the real part of the LC impedance and enforce oscillation. The LC tank resonance frequency gives the oscillation frequency:

$$F_{osc} = \frac{1}{2 \cdot \pi \sqrt{L_{eq} \cdot C_{var}}}. \tag{4.22}$$

To evaluate the oscillation frequency temperature sensitivity, one may use the sensitivity operator defined in [9], so

$$S_T^{F_{osc}} = S_T^{L_{eq}} + S_T^{C_{var}}. \tag{4.23}$$

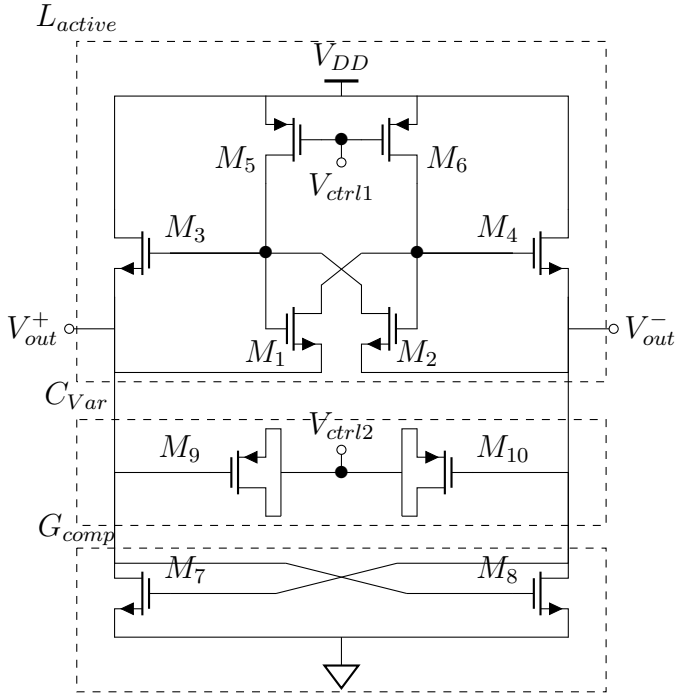


Figure 4.16: Active Inductor Based VCO.

It is clear from (4.23) that in order to have a zero temperature coefficient (ZTC) oscillation frequency the relation between $S_T^{L_{eq}}$ and $S_T^{C_{var}}$ must be:

$$S_T^{F_{osc}} = 0 \Longleftrightarrow S_T^{L_{eq}} = -S_T^{C_{var}}. \tag{4.24}$$

To further investigate the total temperature sensitivity in this oscillator, one may first study the different temperature behavior of C_{var} and L_{active}. For these matter sub-section 3.3.1 and 4.3.1 details the temperature analysis of the varicap and the active inductance respectively.

4.3.1 Active Inductance Temperature Analysis

Active inductances usually do not present an inductive behavior over all biasing, frequency, and temperature. This, at first glance, may seem like a disadvantage when compared to passive inductors. However, passive inductor integration tends to occupy a large silicon area and does not present the reconfigurability, being a major disadvantage for VCO's. The differential active inductance presented on Fig. 4.16 can be represented as a equivalent impedance of a parallel association of a inductor (L_{eq}) with a series resistor (R_s) and a conductance (G_p), where L_{eq},R_s and G_p are given by:

$$L_{eq} = \frac{2(C_{gs1} + C_{gs3})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})} \tag{4.25}$$

$$R_s = \frac{2(g_{ds5} - g_{m1})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})} \tag{4.26}$$

$$G_p = \frac{g_{ds5}}{2} \tag{4.27}$$

As highlighted in (4.25), the equivalent inductance value is given by **1)** transistor capacitance's (C_{gs_1} and C_{gs_3}) and **2)** transistor small-signal parameters. The temperature behavior of small-signal parameters can be evaluated by the technique proposed in this manuscript on Chap. 3. Besides, the temperature sensitivity of the C_{gs} capacitor can be calculated as introduced on Subsec. 3.3.2. By taking the temperature sensitivity from (3.37), one may find:

$$\begin{aligned} S_T^{C_{gs}} =& 2\alpha S_T^{\alpha}\left(\frac{1}{1+2\alpha} + \frac{1}{1+\alpha}\right) + \\ & S_T^{q_{IS}}\left(1 - \frac{q_{IS}}{q_{IS}+1}\right) \end{aligned} \tag{4.28}$$

$$S_T^{\alpha} = \frac{q_{ID} S_T^{q_{ID}}}{q_{ID}+1} - \frac{q_{IS} S_T^{q_{IS}}}{q_{IS}+1} \tag{4.29}$$

The α parameter can be interpreted as the linearity degree from the inversion charge density along the channel whereas it varies from $\alpha \cong 1$ in weak inversion and $\alpha \to 0$ in strong inversion. This asymptotic behavior of α entails a more important impact of the overall temperature sensitivity in weak and moderate inversion. Fig. 3.23(a) and 3.23(b) show the S_T^{α} for $V_D = 1V$ and $V_D = 0.6V$; it is noticeable that the ZTC point at V_{GB} close to V_{th} indicating a moderate inversion ZTC point. In moderate inversion, the source and drain normalized charges have almost the same value close making α close to unity, and nulling (4.29). At this condition of $\alpha \approx 1$ and $q_{is} \approx q_{id}$, one may find that the ZTC condition is given by:

$$S_T^{C_{gs}} \approx \frac{V_p \cdot \left(S_T^{V_p} - 1\right)}{\phi_t \left(q_{is}+1\right)^2}. \tag{4.30}$$

The C_{gs} sensitivity is shown in Fig. 3.23(c). The presence of the same ZTC points indicate a very close relationship between the G_g parameter and the MOSFET capacitors, making it a good starting point to bias transistors in which the capacitance interfere in the quantity of interest (in this case, the equivalent inductance) at this ZTC point.

Biasing transistors M_3 and M_1 ($g_m/I_{D_3} = 7.25$, $g_m/I_{D_1} = 7.15$ at $27°C$) at G_g ZTC, one may find that the equivalent inductance temperature sensitivity reduces to:

$$L_{eq} = \frac{(C_{gs1} + C_{gs3})/{I_D}^2}{(g_{ds}/I_D)_5(2(g_m/I_D)_1 + r(g_m/I_D)_3 - (g_{ds}/I_D)_5)}, \tag{4.31}$$

$$S_T^{L_{eq}}(G_{d_5}) = S_T^{C_{tot}(G_{g1},G_{g3})} - \left(S_T^{G_{d_5}} + \frac{S_T^{G_{g_1}} G_{g_1} - S_T^{G_{g_5}} G_{g_5}}{G_{g_1} - G_{g_5}}\right) + 2 - 2S_T^{J_{ds}}, \tag{4.32}$$

where I_D is the drain current of transistors M_1 and M_3; r the ratio between I_{D_5} and I_{D_3}. Even though most low temperature sensitivity circuits rely on the ZTC biasing of all its components, a VCO requires a bias changing for frequency selection. For this matter, one may bias M_1 and M_3 on G_g ZTC making (5.25)

$$S_T^{L_{eq}}(G_{d_5}) = -\left(S_T^{G_{d_5}} - \frac{S_T^{G_{g_5}} G_{g_5}}{G_{g_{ZTC}} - G_{g_5}}\right) + 2 - 2S_T^{J_{ds}}. \tag{4.33}$$

Since at $G_{g_{ZTC}}$, $S_T^{q_{is}} \approx 0, S_T^{q_{id}} \approx 0$ the J_{DS} temperature sensitivity can be expressed as:

$$J_{DS} = n\frac{\phi_T^2}{2 \cdot L} C_{ox}\mu \left[(q_{is} - 1)^2 - (q_{id} - 1)^2\right], \tag{4.34}$$

$$S_T^{J_{DS}} = 2 + S_T^{\mu}. \tag{4.35}$$

Considering μ with an exponential temperature dependency $\mu(T) = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{-\beta_\mu}$, $S_T^{\mu} = -\beta_\mu$, therefore

$$S_T^{L_{eq}}(G_{d_5}) = -\left(S_T^{G_{d_5}} - \frac{S_T^{G_{g_5}} G_{g_5}}{G_{g_{ZTC}} - G_{g_5}}\right) + 2\beta_\mu - 2. \tag{4.36}$$

Considering G_{d_5} at the proximity of ZTC, where $S_T^{G_{d5}} \approx 0, S_T^{G_{d5}} \approx 0$, (4.36) becomes constant and equal to $2\beta_\mu - 2$. At the vicinity of $G_{g5_{ZTC}}$ transistor M_5 is biased at moderate inversion, therefore CLM effects are negligible and the relation between G_{g_5} and G_{d_5} is linear. By considering equations (4.14) and (4.15) that

gives the approximate G_g and $S_T^{G_g}$ values at the ZTC proximity (4.36) can be approximated by

$$S_T^{L_{eq}}(G_{d_5}) \approx -\left(\left(\frac{T \cdot \alpha_{th}}{V_{p_5} \cdot \eta} - 1\right) \frac{V_{p_5}}{4 \cdot \phi_T} \left(\sigma - \frac{\sigma^2}{(1-\sigma)}\right)\right) + 2\beta_\mu - 2, \tag{4.37}$$

$$\approx \frac{\sigma\,(1-2\sigma)}{4\phi_T\,(1-\sigma)} V_p - \frac{q\alpha\sigma\,(1-2\sigma)}{4\eta k_B\,(1-\sigma)} + 2\beta_\mu - 2 + \mathcal{O}\left(V_p^6\right). \tag{4.38}$$

Equation (4.38) shows an linear relation between $S_T^{L_{eq}}(G_{d_5})$ and V_p that in this technology present a small linear coefficient. Therefore, for some range of V_{ctrl1} the equivalent inductance temperature sensibility can be considered as almost constant.

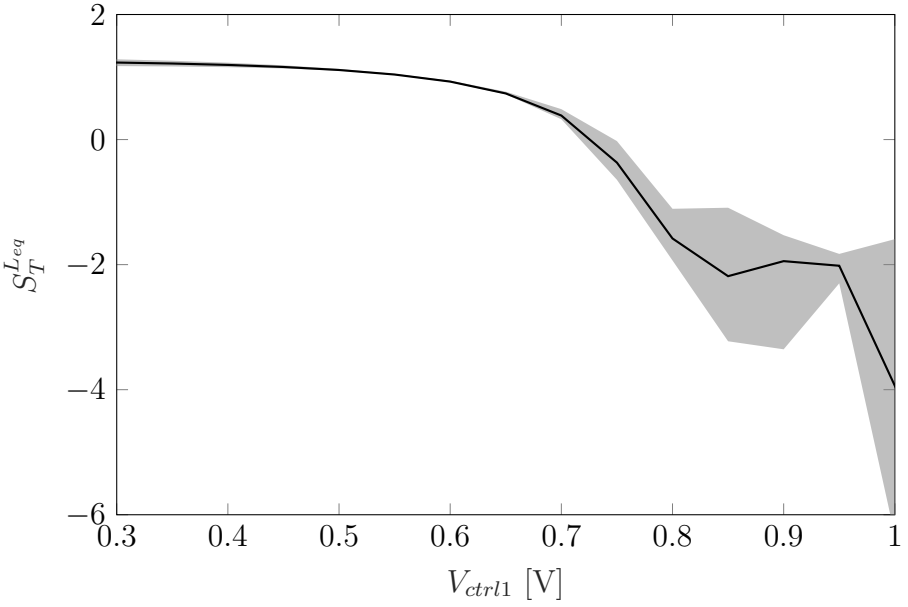


Figure 4.17: Active Inductance equivalent inductance range (gray) and mean(solid) at different control voltages and temperature from -40 $°C$ to 200 $°C$.

Figure 4.17 illustrates the equivalent inductance sensitivity range from temperatures ranging from -40 $°C$ to 175 $°C$. This figure shows a ZTC point of the average temperature sensitivity at $V_{ctrl1} \geq 0.7$ V. However by biasing M_5 in ZTC, the VCO loses its frequency control characteristics. Figure 4.17 shows also an almost constant temperature sensitivity around 1.3 in the region from V_{ctrl1} between 0.3 and 0.6 V. This constant temperature sensitivity can be compensated by the C_{var} temperature sensitivity using (4.24) to achieve a frequency ZTC point and still allow for VCO control.

4.4 Results

To achieve F_{osc} ZTC while maintaining tuning range, the active inductance was biased with G_g ZTC for transistors M_1 and M_3, and the MOS varicap was biased with a V_{ctrl2} of 1.3 V, making the V_{BG} equal 0.4 V when the source voltage is $V_{DD}/2$ and temperature sensitivity is -1.3. The maximum real part of the equivalent impedance seen from the parallel of C_{var} and L_{active} is shown on the Fig. 4.18, post-layout simulation results achieving a maximum value of 600 Ω.

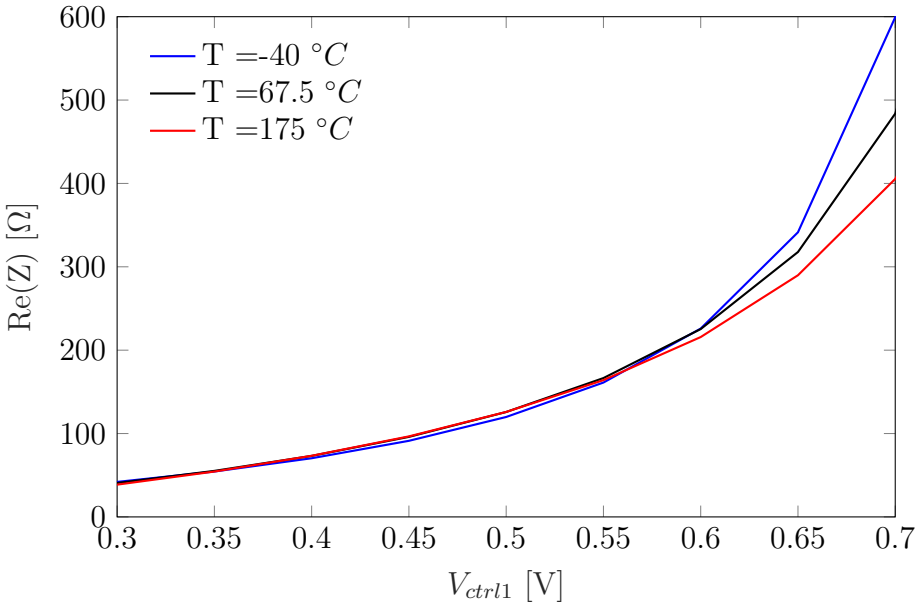


Figure 4.18: PSL Real Part from active inductance impedance for V_{ctrl1} at the tuning range and different temperatures.

The G_{comp} network was designed to have a negative resistance bigger than 600 Ω ($g_m/I_{D_7} = 5.95$ at $27°C$) and the M_{10}, M_9 ($W \times L = 200\mu m \times 300nm$) sizes were adjusted for L-Band range. Fig. 4.19 presents the oscillation frequency and the temperature variation of the circuit. The presented frequencies are designed for a 10% head-up in order to account for the latter parasitic capacitors on the layout. The final circuit layout was generated by the tool IC Layout Render[83] and is presented in Fig. 4.20 having an area of 163.5 x 190 μm^2.

In order to compare the temperature-aware design with the proposition in [10], Fig. 4.21 shows the temperature coefficient of the circuit from [10] called "Traditional"($g_m/I_{D_1} = 9.9$, $g_m/I_{D_3} = 9.8$, $g_m/I_{D_7} = 7.8$ at $27°C$) and the results presented in this work.

The presented work shows an overall zero temperature coefficient, with a tem-

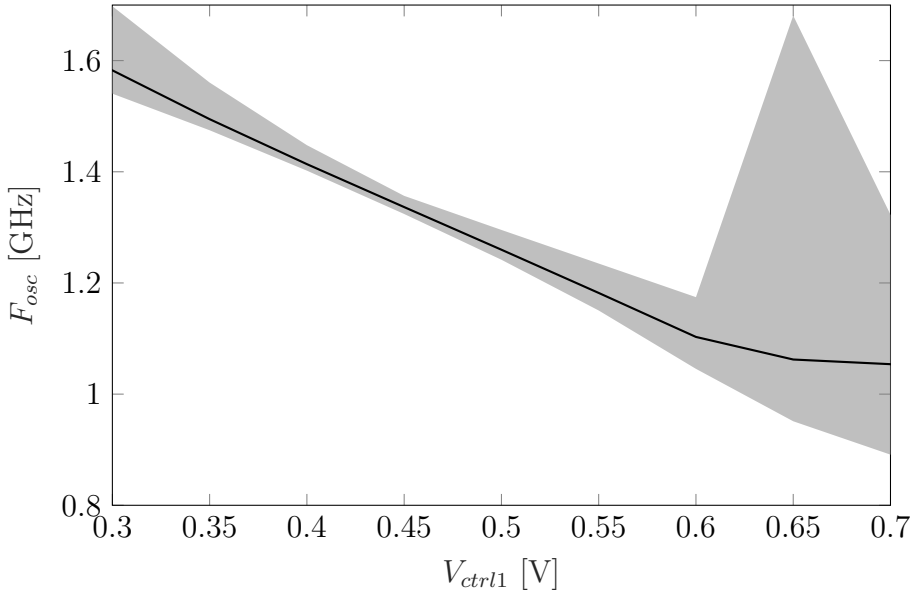


Figure 4.19: PSL Oscillation frequency range (gray) and mean(solid) at different control voltages and temperature from -40 $°C$ to 175 $°C$.

perature coefficient reduction between 2.62 to 9.84 times better than the more traditional design and a mean temperature coefficient of 237.8 ppm/$°C$. For impedance matching two common-source output buffers with 50 Ω drain P+ non-salicided poly resistors presenting its 40 ppm/$°C$ resistance temperature coefficient, see details in Fig. 4.20. Power supply planes were made to decrease line resistance and increase bypass capacitance. All trace widths were constructed to minimize electromigration effects. It is important to point out that the traditional circuit does meet the oscillation condition for some V_{ctrl2} values at low-temperature and low V_{ctrl1} or high-temperature and high V_{ctrl1}.

To evaluate the process and mismatch variations and their consequences on the circuit temperature behavior, a 41 points Monte-Carlo simulation was made for 9 V_{ctrl1} points and 11 temperature points, in a total of 4059 simulations. Since this works goal is to acount for reliability all results will be presented on the worst-case Monte Carlo points. The mean 3σ variation over temperature and the maximum frequency temperature variation is shown in Fig. 4.22.

The Monte-Carlo results show a temperature variation smaller than the mean 3σ variation indicating that the temperature awareness is kept even with process and mismatch variations. The final VCO present a worst case phase-noise of -60 dBc/Hz at a 100 kHz frequency offset, a worst case power consumption varying from 70 mW to 54 mW and a negative temperature coefficient.The oscillator figure of merit is given by:

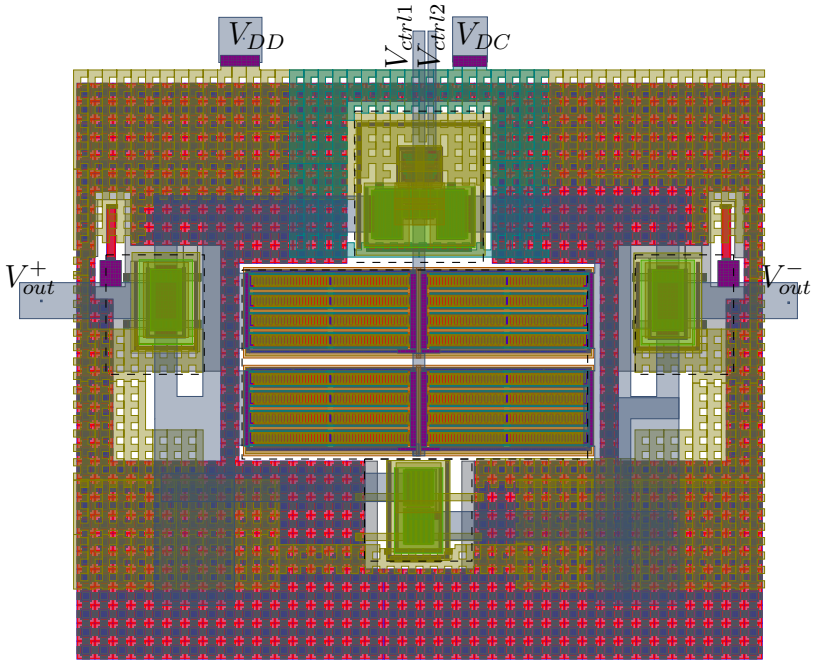


Figure 4.20: Temperature-Aware VCO Layout presenting an area of 163.5 x 190 μm^2.

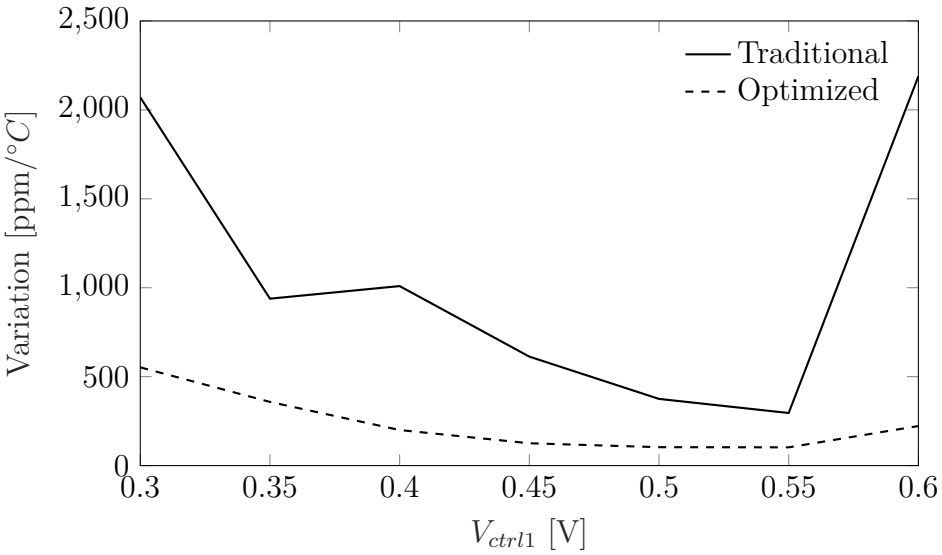


Figure 4.21: Frequency Temperature coefficient comparison between [10] and this work.

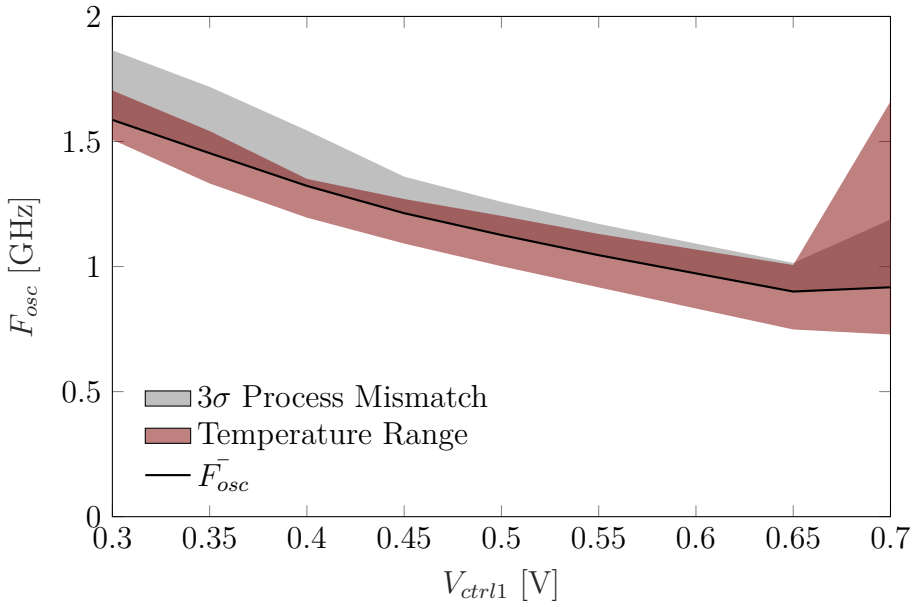


Figure 4.22: Monte Carlo Results for the oscillation Frequency of the proposed VCO.

$$\text{FOM} = \left| L(\Delta f) + 20\log\left(\frac{\Delta f}{f_0}\right) + 10\log\left(\frac{P}{1mW}\right)\right|, \tag{4.39}$$

where $L(\Delta f)$ is the phase noise with a frequency offset of Δf; f_0 is the oscillation frequency; and P the power consumption. The circuit presents a mean FOM over temperature and control voltage of 131 dB. Since the phase noise varies largely with temperature the mean FOM over temperature present a worst case value taken at 27 $°C$ of 146 dB. The typical FOM values are compatible with the state of art.

4.4.1 Conclusion

A low-temperature coefficient VCO suitable for L-band from -45 $°C$ to 175 $°C$ temperature range was proposed. The proposed circuit presents a mean FOM of 131 dB/Hz over the entire temperature range and a mean temperature coefficient of 237.8 ppm/$°C$. A circuit design was presented using a g_m/I_D methodology and can be adapted to other frequency ranges by sizing the circuit's varicap. This is the first demonstration of a temperature-independent oscillation frequency for an extended temperature range suitable for harsh environments applications to the best of our knowledge.

4.5 Conclusion

In this chapter three different temperature-aware circuits were designed using the temperature normalized g_m/I_D parameters. The circuits were chosen to explore the hole frequency helm, starting with a DC bias (Bandgap Voltage Reference), going to a quasi-static operation (The in-band gain of an amplifier), and finally high-frequency (Oscillator Output Frequency). All the circuits presented better or comparable results with state-of-the-art and built in a common framework. This result shows the first encouraging results that explore the flexibility of the temperature normalized g_m/I_D method in designing temperature-aware circuits.

Chapter 5

Conclusion and Perspectives

5.1 Work Conclusions

The IoT platform is changing our relationship with the objects and the world around us. In this search for a more connected Things, some challenges surge to assure the reliability of the different circuits in the harsh environments. Literature has already done some work to model, characterize and minimize different physical phenomena that reduce circuit reliability [13]–[15].

However, when considering the temperature effects on circuits, even though different techniques are presented for different circuits[3], [4], [79], [84]–[86], no general framework for treating the temperature effects has never been done before. This work presents a framework that allows evaluating and minimizing temperature effects on circuits at a very early design point.

The presented technique, called the temperature normalized g_m/I_D, can be included in the more general g_m/I_D allowing the analysis of temperature drift effects and other important parameters as distortion, short channel effects, noise. The proposed technique is here used in three very different use cases for different circuits (Band-Gap Bias Circuit, Differential Amplifier, Oscillator), indicating the flexibility of the technique at different use cases. The proposed technique considers some important short channel effects to analog electronics and is validated on 0.18 μm from -40 $°C$ to 175 $°C$ by simulation and from 27 $°C$ to 200 $°C$ by measurements data on different transistor sizes.

5.2 Research Perspectives

5.2.1 Multi-Objective Optimization

Even though the presented technique allows the analysis and minimization of temperature effects on circuits, temperature is not the only parameter designers are concerned with. In some circuits, some serious trade-off between key circuit parameters and temperature awareness may occur.

The g_m/I_D methodology has already made his proof as an optimization tool in specific parameters. Some examples are amplifier noise, output distortion, and now temperature effects. However, never a strategy for optimizing the different parameters on a circuit, even though ambitious, the g_m/I_D the methodology seems to be a good starting point for this goal. This perspective is starting to be explored on the extension of the SBCCI paper on the Journal of Integrated Circuits and Systems

5.2.2 System Level Optimization

The proposed methodology made his proofs in the circuit level building blocks, achieving low temperature sensitivity of certain parameters. However, considering a more complex system where multiple blocs have connected, the optimization of each block may not be the optimum for the whole system.

The examples showed in the thesis, and the literature takes a bottom-up approach in which once the circuit parameters are defined, the optimization of some transistors bias point will achieve the desired optimum. However, in more complex systems, the circuit interconnects are not necessarily temperature independent. The example shown on SubSec. 4.2.5 talks briefly about the input/output impedance problem that can deteriorate circuits temperature-awareness.

More studies must be conducted to evaluate or extend the presented methodology into a system-level/ top-bottom approach, allowing the technique to tackle bigger and more complex circuits and systems.

5.2.3 Technology Shrink

All results on this thesis are presented using XFAB's XT018 SOI technology. The choice of this technology was motivated by it being a standard in high-end automotive applications, allowing for electronics to operate near-combustion engine compartments or electric engine housings with a temperature range from -40 $°C$

up to 175 $^{\circ}C$ [87], low-power digital applications in communications, consumers, and industrial markets [25].

However, other foundries propose MOS SOI technologies at different temperature ranges and other transistor technologies such as FinFET, Floating Gates transistors, Gate-All-Around transistors that have their applications in newer and modern nodes. Even though the physics behind those new technologies can deviate from the one presented on SubSec. 2.3.2 the g_m/I_D characteristics has been proved to be universal among them [88]–[90]. This universality of the g_m/I_D characteristics may indicate a good starting point for the possibility of using the temperature normalized g_m/I_D technique on these new technologies.

Chapter 6

Résumé Étendu en Français

Larrivé de lindustrie 4.0 et des objets connectés engendre de nombreux défis pour la conception des circuits. L'avancée la plus significative en matière de communication est qu'internet arrive désormais dans les transports et dans l'énergie dans le cadre de l'Internet des objets (IoT). Les progrès exponentiels des circuits, de la puissance du traitement des données et de l'internet ont profondément affecté notre relation avec la technologie et ont remodelé notre société. Ces innovations, promues au cours des dernières décennies, arrivent maintenant aux objets avec le Big Data, permettant de meilleures performances dans l'analyse des données et IoT, réduisant le temps d'acquisition des informations, et permettant le contrôle et l'analyse en temps réel des processus [1].

Pour atteindre cet objectif, les circuits et les capteurs doivent fonctionner de manière fiable, avoir de faibles coûts de production et d'utiliser des matériaux durables sur le plan environnemental. Selon le Boston Consulting Group [2], la propagation rapide de l'IoT est principalement limitée par les coûts de production et de maintenance. La fiabilité des circuits est une tâche complexe et doit être prise en compte tout au long du processus de conception et de fabrication. Les circuits IoT devant être placés à l'intérieur de machines, de véhicules et d'appareils portables, ils peuvent être soumis à des environnements sous contraintes.

La littérature a présenté des solutions de conception pour traiter les circuits sensibles à la température dans divers technologies [3], [4]. Bien que les articles récents aient présenté une sensibilité à la température très faible, les méthodes présentées dépendent principalement du point de polarisation à coefficient de température nulle (ZTC) d'un transistor unique ou de circuits de contrôle supplémentaires. Ce choix de conception augmente intrinsèquement la consommation et le coût de production, ce qui pourrait être prohibitif dans les nouveaux dispositifs IoT à faible puissance. Avec le besoin croissant de conceptions des circuits insensibles à la température, il est indispensable de disposer d'un cadre commun pour les concevoir.

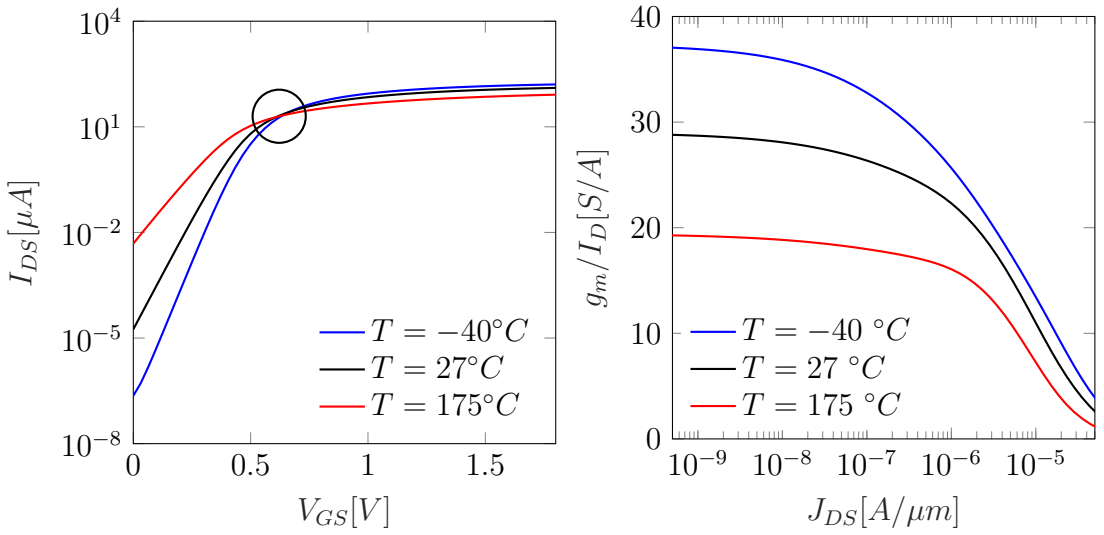
Ce travail propose une analyse de la température en utilisant la méthodologie g_m/I_D, en introduisant le concept de paramètres g_m/I_D normalisés en température. Les points de polarisation ZTC présentés n'ont pas d'influence significative sur la dépendance en température de la mobilité et sont toujours compatibles avec la méthodologie g_m/I_D. Le développement analytique est effectué à l'aide du modèle UICM [5], validé par des simulations sur BSIM v4.6 [6], après leur validation en usine de -40 °C à 175 °C, et par des données de mesure pour des températures plus élevées, jusqu'à 200°C. En outre, un cadre global de la méthodologie tenant compte de la température et un exemple de conception sont présentés.

6.1 Contexte

Avec les progrès de la miniaturisation des transistors, les effets de canal court gagnent en importance. L'incorporation des effets de ces effets dans les modèles de calcul manuel conduit à des équations peu pratiques à résoudre, ce qui fait perdre à ces modèles leur utilité. D'autre part, depuis que cet effet a pris de l'importance, les modèles trop simplifiés perdent de leur précision. Par conséquent, de nouvelles techniques de conception ont été développées pour aider au développement de circuits analogiques offrant un bon compromis entre complexité et précision.

La méthodologie g_m/I_D introduit des paramètres indépendants de la largeur du transistor permettant au concepteur de choisir le W en fonction d'autres prérequis du circuit tels que la consommation d'énergie, la surface active occupée et la région de fonctionnement. Les principaux paramètres analysés dans cet article sont le rapport de transconductance de grille (g_m/I_D) et le gain propre du transistor (g_m/g_{ds}). Le modèle mathématique pour analyser ces paramètres sera basé sur le modèle UICM, introduit par Galup *et al.* [7], un modèle basé sur l'état de charge qui rend compte d'expressions précises mais simples des paramètres g_m/I_D, même pour les transistors quasi-balistiques de taille nanométrique [8].

En contraste avec des paramètres de conception traditionnelle (I_{DS},g_m) les paramètres de la méthodologie g_m/I_D ne présente pas un ZTC comme illustré sur la Fig. 6.1 . Cette absence de ZTC représente a priori un désavantage pour la conception des circuits consciente de la température.



(a) (b)

Figure 6.1: Simulation électrique (a) $I_D \times V_{GS}$, $V_{DS} = 1.8$ V, (b) $g_m \times V_{GS}$, $V_{DS} = 1.8$ V and (c) g_m/I_D , $V_{DS} = 1.8$ V for a $10 \times 0.22\,\mu m^2$ low V_{th} d'un transistor NMOS. Sub-figures (a) et (b) présentent un ZT C, lorsque (c) ne le présente pas.

6.2 Proposition

Malgré ce désavantage, ce travail propose d'adapter cette méthodologie à l'aide des paramètres dit normalisés en température G_g et G_d.

$$G_g = \phi_t \cdot \frac{g_m}{I_D} \tag{6.1}$$

$$G_d = \phi_t \cdot \frac{g_{ds}}{I_D} \tag{6.2}$$

Les paramètres g_m/I_D normalisés sont illustrés ici sur la Fig. 6.2. Il est notable que ces paramètres modifiés présentent des ZTC. Leur utilisation, les conditions analytiques des existences de ZTC et le comportement en température à proximité du ZTC sont décrits sur [9].

6.3 Résultats

Dans cette thèse la technique des paramétrés g_m/I_D normalisé est appliqué a trois circuits: **I)** Une référence de tension bandgap **II)** Un Pair différentielle PMOS avec charge actif **III)** Un Oscillateur contrôlé par tension en bande L. Les choix des

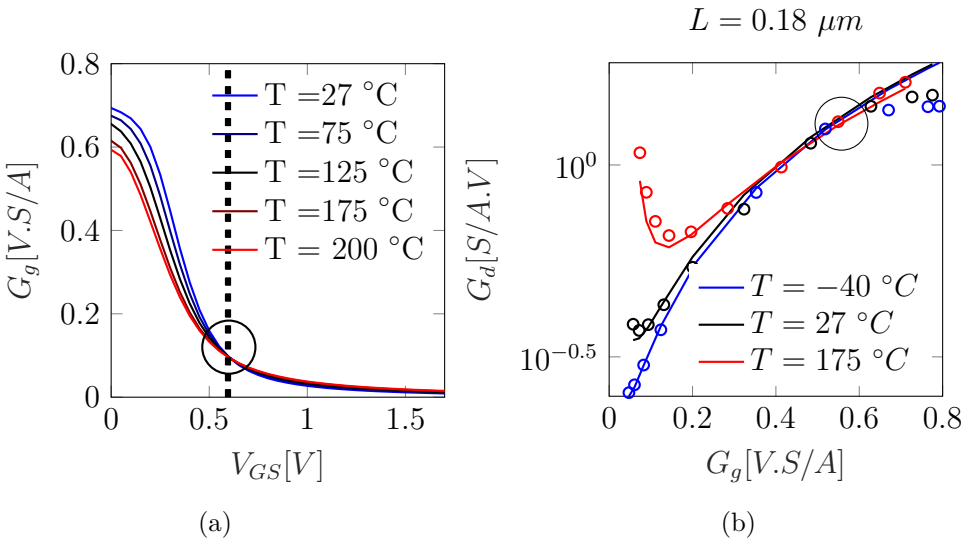


Figure 6.2: Caractéristiques des paramètres proposés pour un transistor low-VT avec 180 nm de longueur de canal (a) G_g (b) G_d

circuits a été fait pour couvrir les trois différents régimes en fréquence: polarisation, régime quasi-statique et radio fréquence.

Une méthode differente d'optimization a été employé pour chaque circuit. Sur le bandgap les références PTAT (Proportionall to Absolute Temperature) et CTAT (Complementary to Absolute Temperature) on été optimisée pour avoir une réponse la plus linéaire possible. L'amplificateur à été optimisée de façon que les transconductances des différents transistors s'annulent mutuellement en température afin d'avoir un gain stable en température. L'Oscillateur contrôlé par tension (VCO) a été optimisé de façon que l'inductance active présente une sensibilité constante sur une plage de polarisation et que peux être annulé avec une sensibilité de même valeur et différent signé d'un varicap.

Le bandgap a présenté un comportement en température compatible avec l'état de l'art comme illustré sur la Fig. 6.3. La variation de la tension de référence est de 18.23 ppm/$°C$, avec un PSRR de 28.91 dB.

L'amplificateur présente une performance en température approximativement 22 fois supérieur quand comparé a la methode classique de conception de tel circuit. Figure 6.4 illustre le gain des amplificateurs quand conçu par la méthodologie traditionnelle et la méthodologie proposé par cette thèse.

Cette performance en température est maintenu même si les variations de process sont prises en compte comme illustré sur la Fig. 6.5 ou le deux corners avec les pires performances en température sont affichés. A notre connaissance ceci

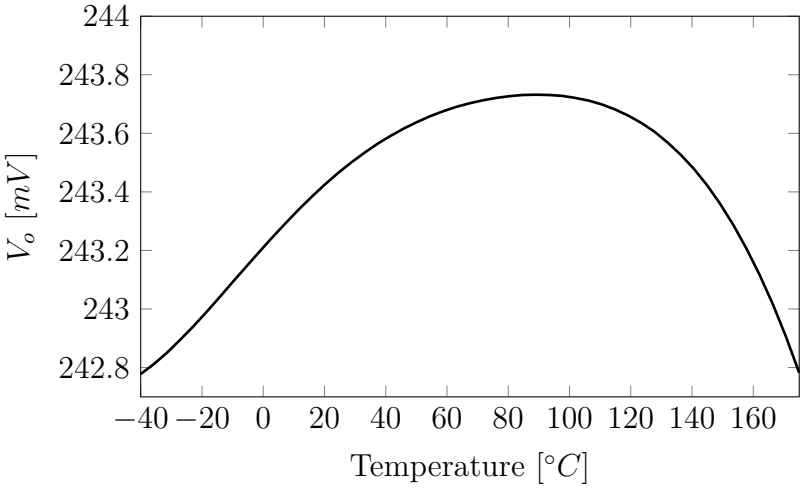


Figure 6.3: Tension de reference du bandgap proposé de -40 $°C$ à 175 $°C$.

est la premier démonstration d'un gain de tension d'un amplificateur invariant en température.

Quand comparé au design initiale proposé par [10] le VCO présente une performance en température entre 2.6 et 9.8 fois meilleur en température pour les différents polarisations. Ces résultats ici illustrés par la Fig. 6.6 sont en notre connaissance le premier VCO en boucle ouverte conçu avec une technologie de Silicium,pour addresser des défits de température élèvé (200 °C) jamais publié.

Une simulation Monte-Carlo du layout de ce circuit illustré à Fig. 6.7 est présenté sur la Fig. 6.8. Le layout occupe une surface de 163.5 x 190 μm^2 et est composé du VCO avec sortie différentielle et deux buffers avec une impédance de sortie de 50 Ω. Les résultats Monte-Carlo montre que la variation de fréquence avec la température est plus petite ou comparable à la variation de process et missmatch.

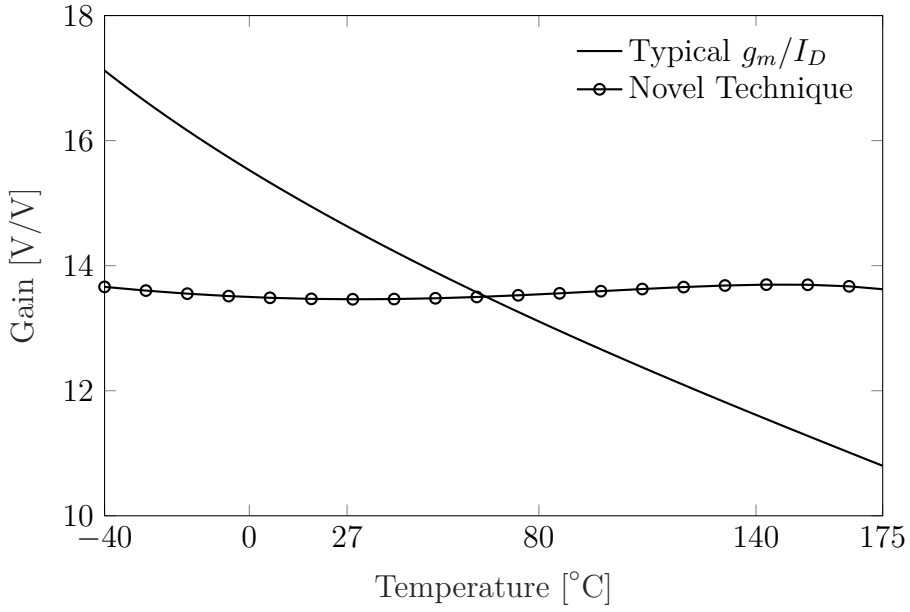


Figure 6.4: Comparaison entre le gain d'un amplificateur conçu avec g_m/I_D traditionnelle et la proposition

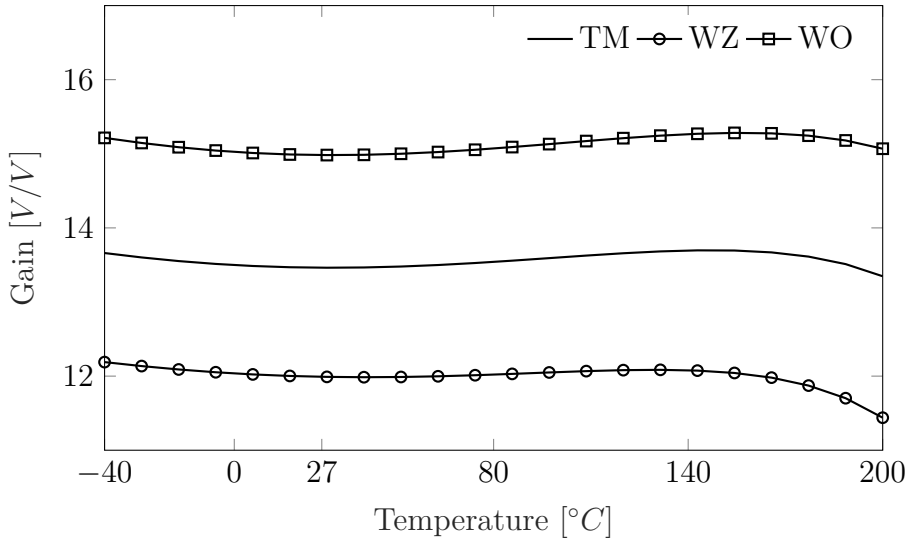


Figure 6.5: Variation du gain de l'amplificateur proposé à différentes températures.

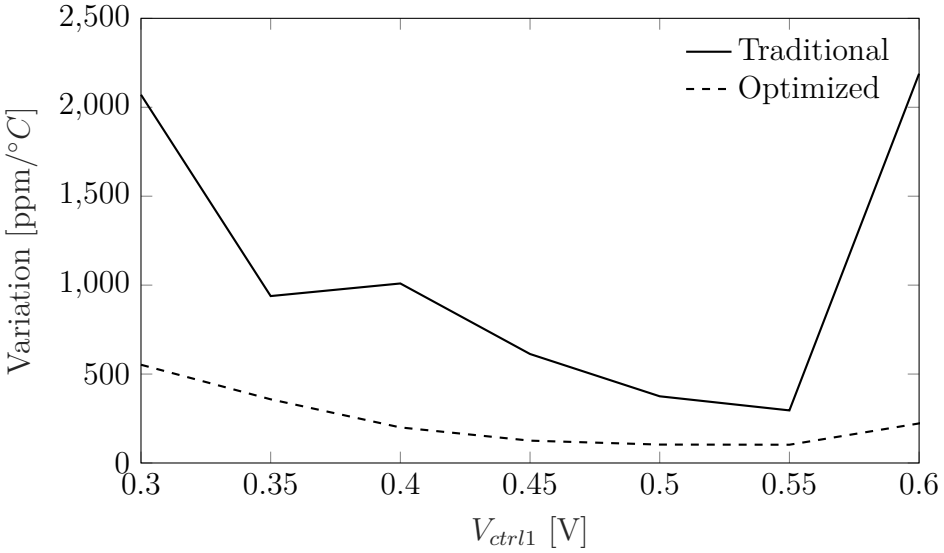


Figure 6.6: Variation du gain de l'amplificateur proposé à différentes températures.

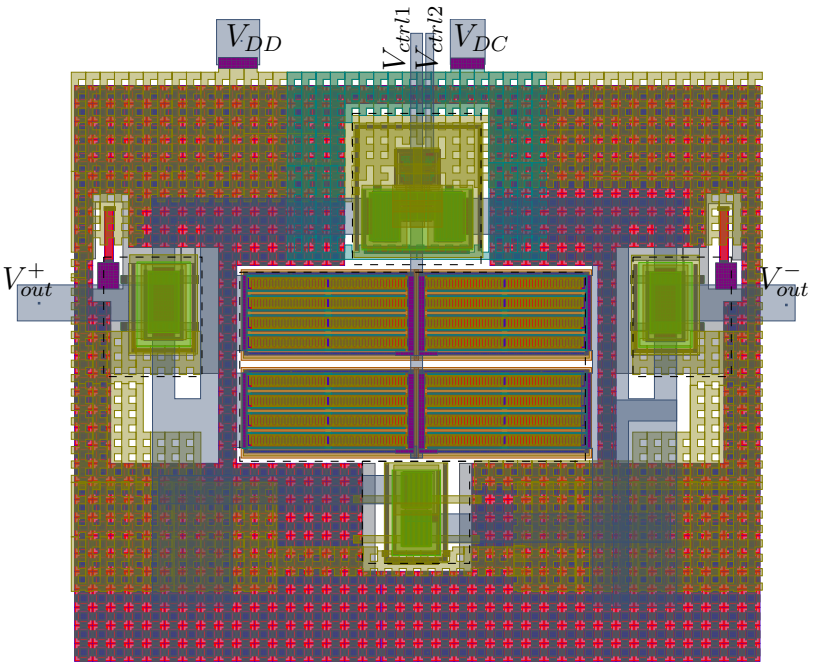


Figure 6.7: Layout du VCO proposé avec une surface de 163.5 x 190 μm^2.

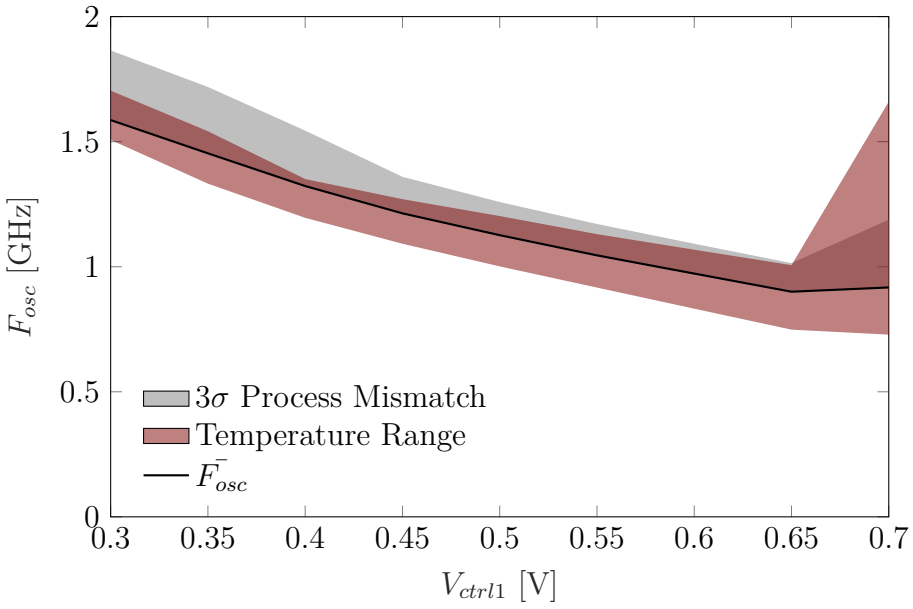


Figure 6.8: Résultats Monte Carlo de la fréquence généré par l'oscillateur proposé.

6.4 Conclusion

Avec l'arrivée des Objets Connectés et les besoins de l'industrie 4.0, la prise en compte de la température est essentielle. Avant cela aucune méthodologie ne présentait un cadre commun pour une conception des circuits consciente de la température. Dans ce travail une adaptation de la méthodologie g_m/I_D est proposée pour la prise de conscience des effets de température dans les étapes préliminaires de conception. Les paramètres ainsi que les points de ZTC sont testés par simulation et validés par des résultats des mesures. Avec cela trois circuits illustrent l'utilisation de la méthodologie mise en ouvre dans ce travail. Ces trois circuits présentent des performances similaires à la méthodologie traditionnelle avec une réduction considérable sur les effets de température sur un paramètre choisi.

Appendices

Appendix A

Crystal Structures Statistics

The presence of atoms will introduce a periodic potential well due to Coulomb and other interactions. Fig. A.1 represents in blue the Coulomb potential for Silicon atoms with lattice constant 5.4 $\mathring{A}$. This potential can be firstly approximated by rectangular wells. In this structure, the nuclei interaction will be represented by a simple localized rectangular potential of width b, height V_0 and spacing a_0, this toy model is called the Kronig-Penney model, and the potential $V(x)$ is here represented in black on Fig. A.1.

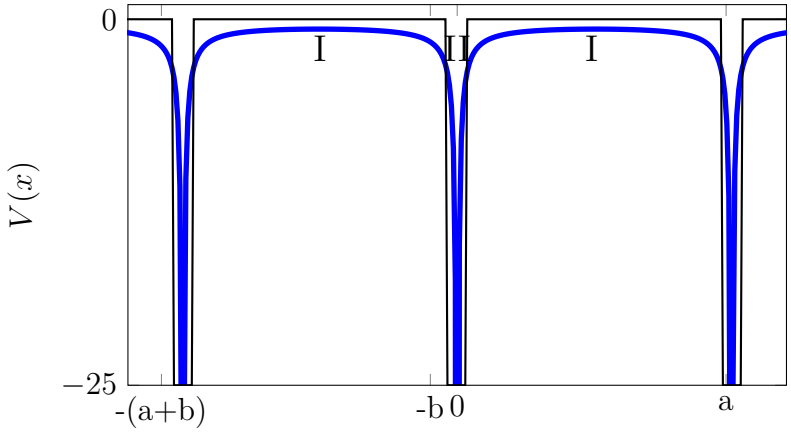


Figure A.1: The Kronig-Penney model potential energy approximation

In a quantum framework, particles and their states are represented by a wave function, $\psi(x)$, entirely representing the particle in their environments. In this periodic configuration, it is expected that the wave function presents a periodic configuration in the form $\psi(x) = u(x)e^{ikx}$; where $u(x)$ is a periodic function with period a_0; k the wave number; and i the imaginary unit. This assumption can be more formally derived and is called the Bloch-Theorem. By solving the Schrodinger

equation in the two different regions (I, II) of the potential illustrated in Fig. A.1, one may get:

$$\begin{cases} u(x) = \left(A\cos\left(\beta x\right) + B\sin\left(\beta x\right)\right)e^{-ikx} & \text{On Region I} \\ u(x) = \left(C\cosh\left(\alpha x\right) + D\sin\left(\alpha x\right)\right)e^{-ikx} & \text{On Region II} \\ \alpha = \frac{\sqrt{2m(V_0-E)}}{\hbar} \\ \beta = \frac{\sqrt{2mE}}{\hbar} \end{cases} \tag{A.1}$$

where m is the electron rest mass; E the electron energy; and $\hbar$ the reduced plank constant. By imposing the continuity of the wave-function on the region's boundaries and its periodicity due to Blochs theorem, one may get:

$$\cos\left(ka\right) = \frac{\alpha\left(E\right)^2 - \beta\left(E\right)^2}{2\alpha\left(E\right)\beta\left(E\right)}\sinh\left(\alpha\left(E\right)b\right)\sin\left(\beta\left(a-b\right)\right) \tag{A.2}$$

$$+\cosh\left(\alpha\left(E\right)b\right)\cos\left(\beta\left(E\right)\left(a-b\right)\right) \tag{A.3}$$

The left-hand side of equation (A.3) is limited to the interval $[-1, 1]$ however, as can be seen in Fig. A.2 the right-hand side assume values outside this range, in this prohibited (highlighted in gray) the equation presents no solutions and therefore it is not possible to have electrons with energy in the forbidden gap

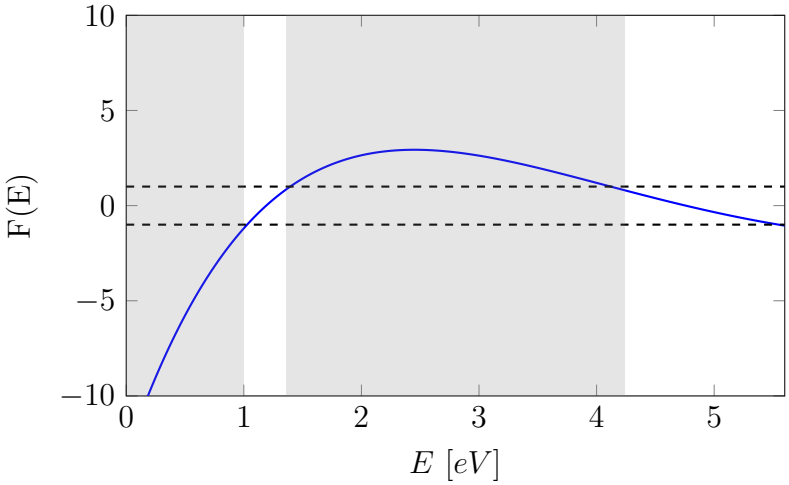


Figure A.2: Right hand side of Kronig-Penney model solution

The usual representation of this effect in materials is through the use of an E-K diagram shown in Fig. A.3. The x-axis is proportional to wave-number k, related

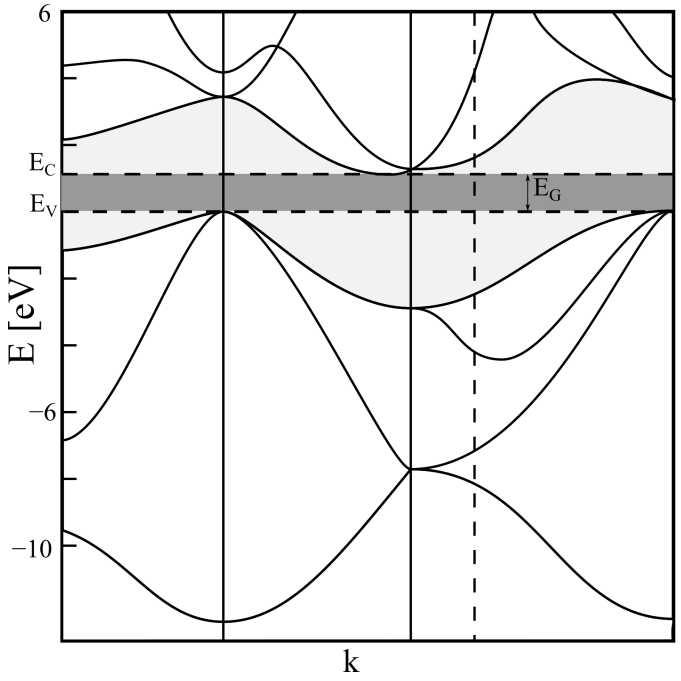


Figure A.3: Silicon Energy, wave vector relation on intrinsic silicon

to the particle moment, and the y-axis the corresponding allowed energies. It is noticeable that at low velocities, the $K \times E$ relation is almost quadratic, as shown on the dashed blue line. Besides, there is a gap of allowable energies, usually called *Energy Band Gap* and represented by E_G. In the E-K diagram the energies are usually represented in an interval of $\frac{2\pi}{a}$ since it is periodic.

For real crystalline structures, the calculations are much more involved and can only be determined numerically, but the overall features are the same, as can be seen in Fig. A.3 that shows the E-K diagram for Silicon. The Energy band diagrams are frequently simplified when studying semiconductor devices.

The study of the physical properties of solid-state materials began in the early years of the 20th century. Solid-state materials are composed of arranged atoms that, in their simplest form, produce a periodic grouping known as a crystal [91]. The interaction between those atoms are intematly related to the macro-properties of the cristal. However, The study of many interacting bodies through Newtonian or quantum physics does not present any closed-form analytical solution for systems with more than a few dozen particles and was an open problem for more than three bodies until very recently in science [92]

Most semiconductor materials used in microelectronics present crystalline structures. For low-cost electronics, Si is the most suitable material due to the already acquired manufacturing process maturity. For this reason, silicon material will be

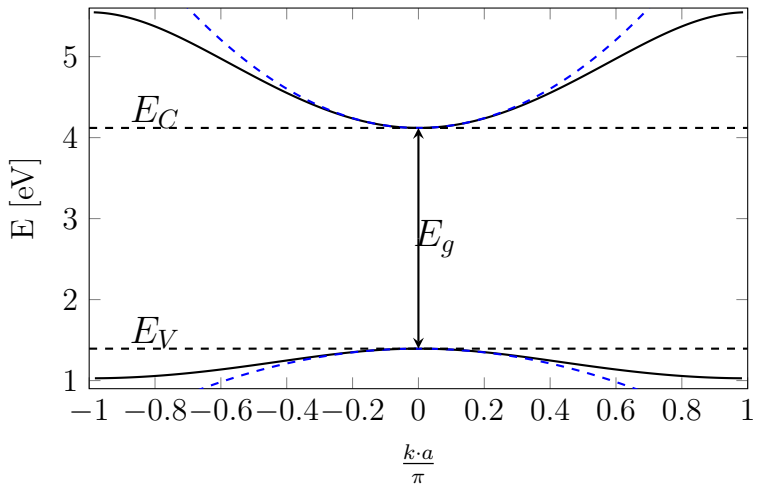


Figure A.4: Test

the focus of this chapter. Fig. A.5 presents a 2D representation of a Silicon crystalline sheet. The nucleus is there presented in blue, and the electrons in red. The scale presented on A.5 is exaggerated for illustration purposes, in reality considering a nuclei radii (r_0) of 1.3 fm the nucleus of Silicon present a radius of 3.9 fm while the mean distance from two Silicon nucleus on the crystal is of $5.4 \cdot 10^5$ fm.

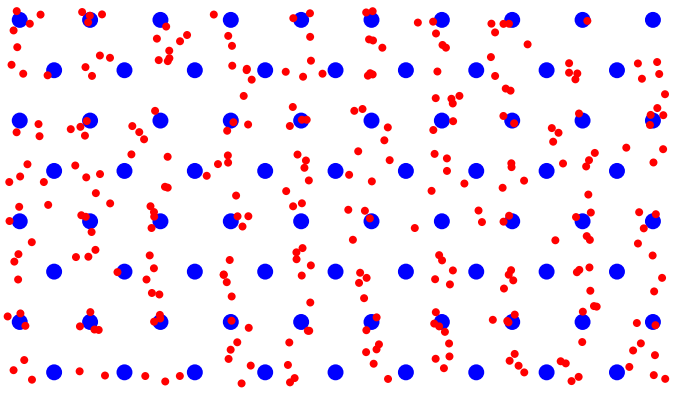


Figure A.5: Representation of a crystal lattice

In the 18th century, Boltzmann and Maxwell proposed a different approach to the many-body interaction problem in gasses. The proposed solution took a probabilistic approach to the problem and started a new branch of physics nowadays entitled statistical mechanics. Since the Maxwell-Boltzmann Theories represent the basis of the studies of crystalline structures and highlight many important concepts in semiconductor physics and temperature, the next subsection will the

devoted to it.

A.1 Classical Statistical Mechanics

As discussed in the previous subsection, the distance between nuclei on a silicon slab is five orders of magnitude bigger than those nuclei. As a first approximation, one may say that the nuclei are dispersed in the slab in a gas of electrons. To study the gas behavior, one may start with a simple two-dimensional gas in a box. Considering that the gas particles possess the same mean energy, one may subdivide the system into N subsystems. Let E be the total energy of the system. One may divide the interval $[0, E]$ into M bins. Let n_i be the number of subsystems that possess energy in the E_i bin.

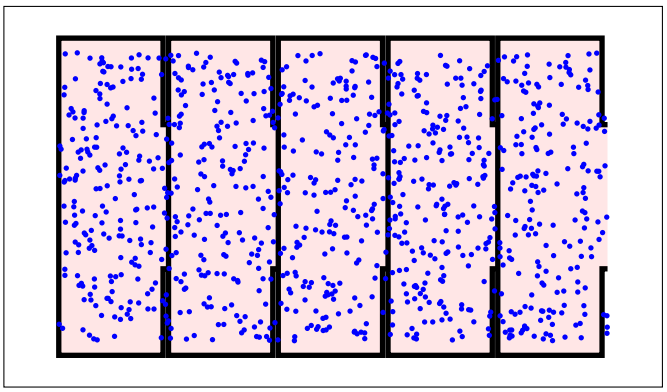


Figure A.6: System Subdivisions

According to the second law of thermodynamics, energy distribution will be such as the entropy is maximized, in other terms, such as the number of possible arrangements C of the occupation numbers n_i over the N subsystems is maximized, where C is given by:

$$C = \frac{N!}{\prod_i n_i!} \tag{A.4}$$

By letting N and M big (subdividing many times the system and the energy levels), one may take Stirling's approximation for factorials, leading to:

$$C \approx \frac{N^N \cdot e^{-N}}{(\prod_i n_i^{n_i}) \cdot e^{-(n_1+n_2+\ldots)}} \tag{A.5}$$

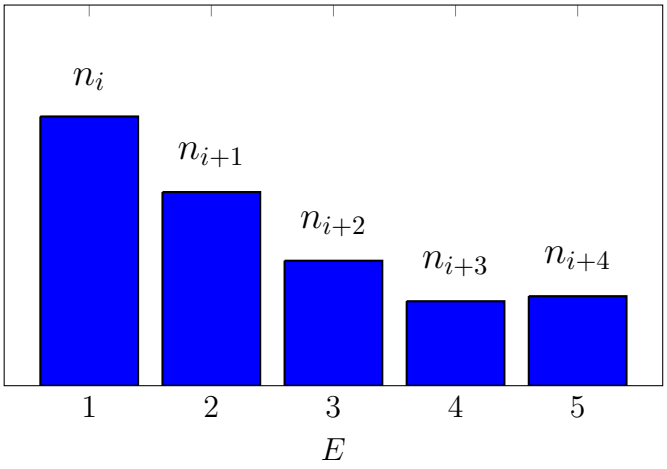


Figure A.7: Energy binning histogram

Since the sum of the occupation numbers must be equal to the total number of subsystems, the exponential part of the numerator and denominator can be canceled out. Since the logarithm function is monotone, maximizing C is the same as maximizing

$$\log(C) = N\log(N) - \sum_i n_i \cdot \log(n_i) \tag{A.6}$$

By letting p_i be the probability of having a subsystem with energy on the E_i bin, such as $n_i = N \cdot p_i$ (A.6) reduces to

$$\log(C) = -N \sum_i p_i \log\left(p_i\right). \tag{A.7}$$

One may notice that (A.7) is the actual Boltzmonic definition of entropy. However, this maximization problem is constrained by the fact that probabilities have to sum up to 1.0 and that, as stated before, all subsystems possess the same average energy $\bar{E}$. The maximization procedure can be done by the use of Lagrange-Multipliers leading to:

$$\begin{cases} p_i & = \operatorname{argmax} \log(C) \\ \sum_i p_i & = 1 \\ \sum_i p_i \cdot E_i & = \bar{E} \end{cases} \tag{A.8}$$

$$p_i = \frac{1}{Z(\beta)} \cdot e^{-\beta \cdot E_i}, \tag{A.9}$$

$$Z(\beta) = \sum_i e^{-\beta \cdot E_i}, \tag{A.10}$$

where $Z(\beta)$ and β comes from the Lagrange-Multipliers from the constraints. The model taken considers that the energy states and probabilities are discrete. However, from a classical point of view, energy can assume any real positive value. To get the continuous definition of the probability density function, one may take the limit as $M \to \infty$ and $N \to \infty$ turning (A.9) into:

$$\begin{cases} p(E)dE &= n_0(\beta) \cdot e^{-\beta(E-\mu)} \\ n_0(\beta) &= \frac{1}{e^{\beta\mu} \int_0^\infty e^{-\beta\epsilon} d\epsilon} \end{cases}. \tag{A.11}$$

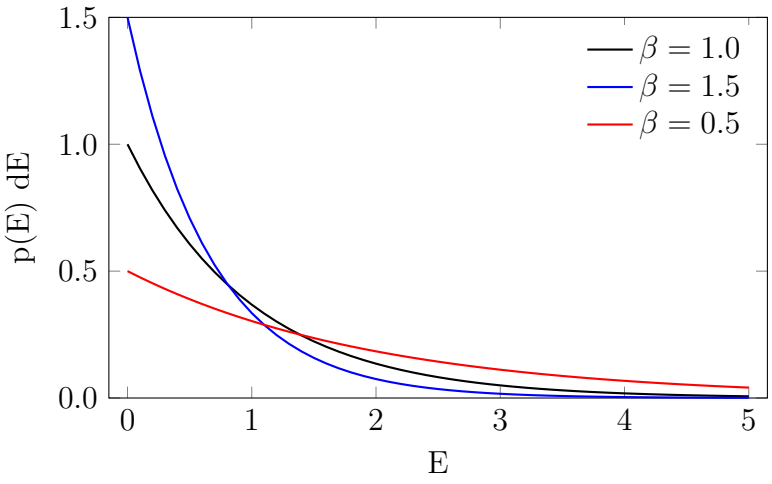


Figure A.8: The Boltzmann Distribution

The $n_0(\beta)$ is a scaling term that for a given β makes the integral of $p(E)dE$ be equal to 1.0; the μ term is added by convenience to represent an energy reference, and effects do not affect the distribution shape. However, as seen in Fig. A.8, the β parameter greatly impacts the distribution.

$$\bar{E} = \int_0^\infty E \cdot p(E)dE = \frac{1}{\beta} \propto T \Rightarrow \beta = \frac{1}{k_B \cdot T}, \tag{A.12}$$

where k_B is the Boltzmann constant, the proportionality constant to temperature and energy. This crude model shows a first approximation for energy distribution on semiconductors viewing them as electron gas. As seen in this model, the temperature plays a major role, but this model does not account for the atoms' nucleus periodicity, to have a more accurate model, one needs to advance one century on the history of science and get into the quantum description of particles.

Appendix B

Fermi Distribution

Electrons cannot assume continuous values of energies inside the crystal lattice. Electrons obey the Pauli exclusion principle that states that two or more electrons on the same system cannot occupy the same state. Two new concepts need to be introduced to mitigate the presented problems: the density of states that accounts for multiple states with the same energy and the Fermi-Dirac distribution function that makes corrections for the Boltzmann distribution.

B.1 Fermi Level

The Pauli exclusion principle states that two or more electrons on the same system cannot occupy the same state. Each state corresponds to a set $< \vec{p}, \vec{k}, s >$, where $\vec{p}$ is the particle position, $\vec{k}$ the wake vector and s the spin. Therefore the given energy levels must be either filled by one electron or unoccupied. As seen before imposing entropy maximization, the probability of having N electron on a given energy state is proportional to $e^{-\frac{E(N)}{kT}}$ by imposing that a state can only have either one or zero electrons, one may find:

$$P\left(N=0\right)+P\left(N=1\right)=\frac{1}{Z}\left[e^{-\frac{E(0)}{k_BT}}+e^{-\frac{E(1)}{k_BT}}\right]=1\Rightarrow Z=e^{-\frac{E(0)}{k_BT}}+e^{-\frac{E(1)}{k_BT}} \quad \text{(B.1)}$$

Therefore, the probability of occupation of a state considering the Pauli exclusion principle is:

$$P\left(N=1\right)=F\left(E,T\right)=\frac{e^{-\frac{E}{k_BT}}}{e^{-\frac{E_0}{k_BT}}+e^{-\frac{E}{k_BT}}}=\frac{1}{1+e^{\frac{E-E_0}{k_BT}}} \quad \text{(B.2)}$$

The result of (B.2) is known as the Fermi-Dirac distribution and represents the probability of occupation of a given energy level by Fermions (particles that follow

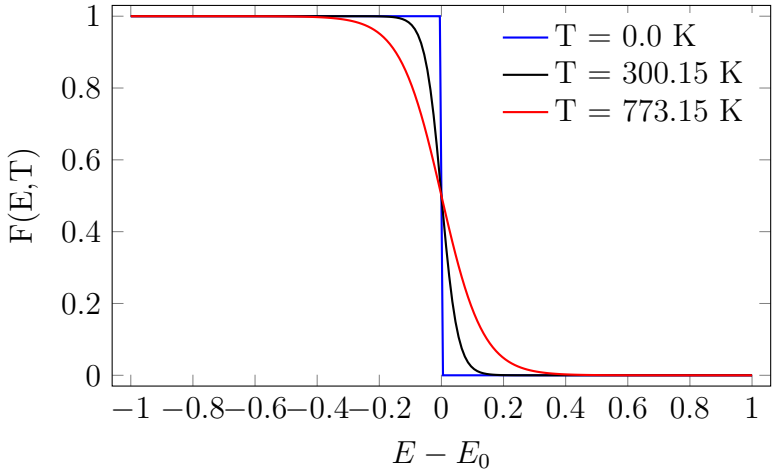


Figure B.1: Fermi-Dirac distribution function at different temperatures

the Pauli exclusion principle). At 0 K electrons, as shown on Fig. B.1, the Fermi-Dirac distribution approaches a step function. At this temperature, electrons do not present any kinetic energy and will only be held the potential energy of atoms. By applying the principle of least action, the atom's potential energy will define a supremum limit at 0 K in which the Energy level will be occupied. This maximum occupied energy at 0 K on a semiconductor material is called the *Fermi Level* (E_f) or the *Chemical Potential* (μ_E) and is constant trough-out the system. This energy will separate the band structure into two regions; if electrons possess energy below E_F, it will be held by the atom's potential. Otherwise, it may "escape" the potential well and be "free" to conduct.

In Semiconductor materials, the Fermi Level lies in the middle of the band gap and will separate the possible energy levels into a valence band and a conduction band. With the increase of temperature, the deviation from E_f is contained. This small deviation implies that electrons will usually be either on the top of the valence band or when they gain enough kinetic energy at the bottom of the conduction band, leaving a hole behind it. In [93] Shockley *et al.* showed that the treatment of holes as positive mobile particles immensely decrease semiconductors calculations, since they represent the absence of electrons their energy partition function is given by $(1 - F(E,T).)$

Given the density and the occupation probability of states, the calculation of the number of free carriers can be calculated as follows:

$$n(T) = \int_{E_C}^{\infty} g(E,T)F(E,T)dE = \int_{E_C}^{\infty} M_C \frac{\sqrt{2}}{\pi^2} \frac{m_{de}^{3/2}(E - E_C)}{\hbar^3} \frac{1}{1 + e^{\frac{E-E_F}{k_B T}}} dE \tag{B.3}$$

$$= N_C \frac{2}{\sqrt{\pi}} \mathcal{F}_{1/2}\left(\frac{E_F - E_C}{k_B T}\right) \tag{B.4}$$

$$N_C = 2\left[\frac{m_e^* k_B T}{2\pi\hbar}\right]^{\frac{3}{2}} \tag{B.5}$$

where N_C is the effective density of states on the conduction band. The integral presented on (B.5) does not present a closed analytical solution. It is called the Fermi-Dirac integral of order 1/2 $\left(\mathcal{F}_{1/2}\right)$

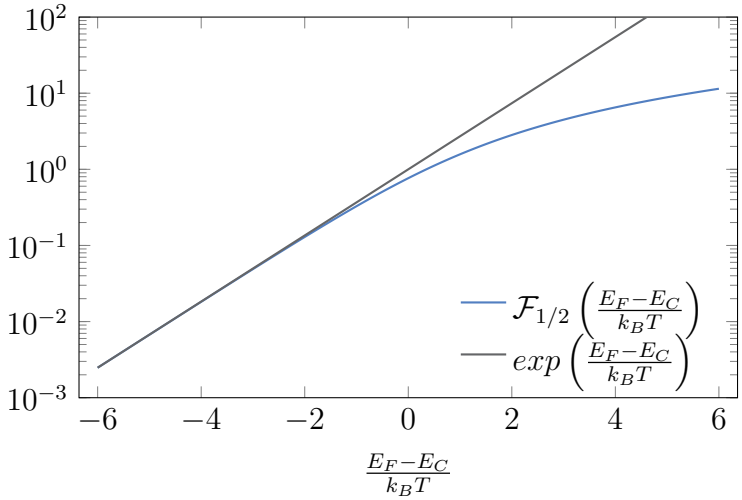


Figure B.2: Comparison Between Fermi-Dirac integral and Boltzmann approximation

However, for high temperatures or low enough energies, the Fermi-Dirac integral can be approximated by an exponential similar to the Boltzmann-Maxwell distribution. Physically, it means that the carriers' kinetic energy is much greater than the lattice potential barrier, making the carriers behavior closer to the electron gas problem. A similar calculus can be done to investigate the holes concentration expressed as:

$$p(T) = N_V \frac{2}{\sqrt{\pi}} \mathcal{F}_{1/2} \left(\frac{E_V - E_F}{k_B T} \right) \tag{B.6}$$

$$N_V = 2 \left[\frac{m_p^* k_B T}{2\pi\hbar} \right]^{\frac{3}{2}} \tag{B.7}$$

In a semiconductor in equilibrium the number of mobile carriers (electrons in the conduction band and holes in the valence band) must be the same. Considering the Boltzmann approximation one may solve for the Fermi level E_F:

$$E_F = \frac{E_C + E_V}{2} + \frac{k_B T}{2} \ln \left(\frac{N_V}{N_C} \right) \tag{B.8}$$

Since for Silicon the ratio between the effective density of states on the conduction and valence band is very close to one, Si intrinsic Fermi level is very close to the middle of the band gap, independently of temperature. In temperatures other than 0 K the thermal energy can be high enough to transfer their energy and give rise to a electron-hole pair. The probability per unit time that the created pair has energy bigger than the semiconductors E_G is proportional to the the product $n \cdot p = n_i^2$ shown bellow on Fig. B.3.

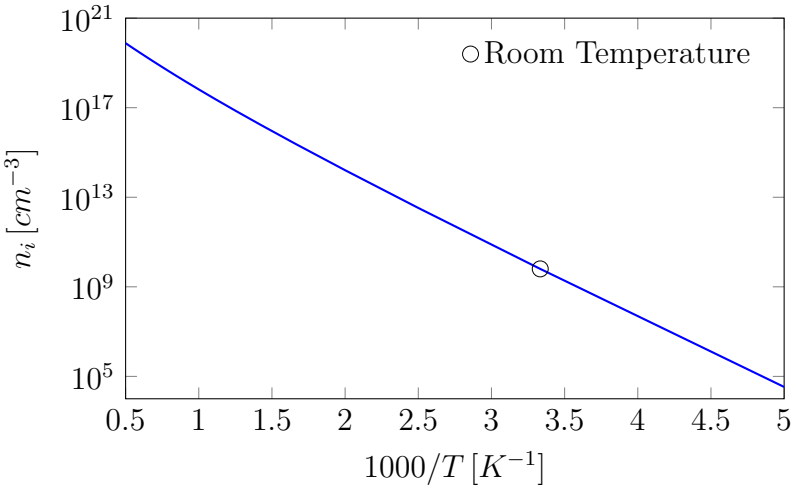


Figure B.3: Intrinsic carrier concentration relation with inverse temperature using Fermi-Dirac distribution

For a semiconductor in equilibrium, the number of holes and electrons must be the same ($n = p$) and therefore equal to n_i. By using Boltzmann approximation, the intrinsic carrier concentration can be written as:

$$n_i(T) = \sqrt{N_C(T)\,N_V(T)}e^{\left(-\frac{E_G}{2k_BT}\right)} \tag{B.9}$$

The advantage of (B.9) in relation to (B.5) and (B.7) is the absence of the Fermi Level dependency. The Validity of the approximation can be estimated by the relative error of the np product using the Boltzmann Approximation and the Fermi-Dirac distribution shown in Fig. B.2

Appendix C

Drift-Diffusion Equation

In the last analysis where formulated to understand the behavior of semiconductors at equilibrium. However, when a bias voltage is applied on a silicon slab an electric field will be generated making carriers displace. Considering that the dynamical behavior of particles can be described by an state composed by position and crystal momentum, one may write the time evolution equations as:

$$\frac{d\vec{p}}{dt} \rightarrow \frac{d\left(\hbar\vec{k}\right)}{dt} = -q\vec{\xi} = -\nabla_r E_C\left(\vec{r}\right) \tag{C.1}$$

$$\hbar\vec{k}\left(t\right) = \hbar\vec{k}\left(0\right) + \int_0^t -q\vec{\xi}(\tau)d\tau \tag{C.2}$$

$$\vec{\nu}\left(t\right) = \frac{1}{\hbar}\nabla_k E\left[\vec{k}\left(t\right)\right] \tag{C.3}$$

$$\vec{r}\left(t\right) = r\left(0\right) + \int_0^t \vec{\nu}\left(\tau\right)d\tau \tag{C.4}$$

where ξ is the electric field; ν the group velocity and the $E\left[k\right]$ corresponds to the dispersion relation given on the $E \times k$ diagram from the semiconductor. By appling the time evolution equations on a given initial carrier state, the result is a state-space trajectory $T(r,p)$ from the carrier. Since the carrier energy occupation probability $(f(x,p,t))$ does not change on this trajectory, the following can be written:

$$f(x,p,t) = f(x - \nu dt, p - F_e dt, t - dt). \tag{C.5}$$

By subtracting both sides and dividing by dt, the result shows that the total derivative of f in relation to time is equal to zero.

$$\frac{df}{dt} = \frac{\partial f}{\partial t} + \frac{\partial f}{\partial x}\frac{dx}{dt} + \frac{\partial f}{\partial p}\frac{dp}{dt} = \frac{\partial f}{\partial t} + \frac{\partial f}{\partial x}\nu + \frac{\partial f}{\partial p}F = 0 \tag{C.6}$$

However, an external process such an recombination of an electron following an trajectory $T(r,p)$ may recombine with a hole or a scattering event may occur changing the total time derivative of f, making (C.6):

$$\frac{\partial f}{\partial t} + \frac{\partial f}{\partial x}\nu + \frac{\partial f}{\partial p}F = C\left[f\right] + S \tag{C.7}$$

where $C[f]$ accounts for scattering events and S for any possible source or sink of carriers. Equation (C.7) is known as the Boltzmann Transport equation. Even though the semi-classical approach was take to derive the equation, the scattering operator C must be handled in a quantum framework. It is important to highlight that for semiconductors some approximations where taken, the definition of the momentum and position of a given particle is limited by Heisenberg uncertainty principle, the carrier to carrier correlations where ignored (mean-field approximation) and the temperature was considered homogenous over the system.

C.1 Scattering and the Relaxation Time Approximation

The scattering effects alter the distribution function $f(x,p,t)$ from either a in-scattering process, where carriers at $p\prime$ get scattered to p, or an out-scattering process both controlled by a transition rate S. The net difference of change on f will be given by:

$$C\left[f\right] = \sum_{p\prime} f\left(p\prime\right)\left[1 - f(p)\right] S\left(p\prime, p\right) - \sum_{p\prime} f\left(p\right)\left[1 - f(p\prime)\right] S\left(p, p\prime\right) \tag{C.8}$$

Since for non degenerate semiconductors the probability of non occupancy of a state $(1 - f(p))$ is very close to 1 (C.8) can be further simplified to:

$$C\left[f\right] = \sum_{p\prime} f\left(p\prime\right) S\left(p\prime, p\right) - \sum_{p\prime} f\left(p\right) S\left(p, p\prime\right) \tag{C.9}$$

The used distribution is no longer the equilibrium distribution $(f_0(E))$ for this reason one may describe the non equilibrium function as a disturbance from the equilibrium $f(x,p,t) = f_0 + \delta f$, making (C.9):

$$C\left[f\right] = C\left[f_0\right] + C\left[\delta f\right] \tag{C.10}$$

Notably in equilibrium there are no scattering events and therefore $C[f_0] = 0$, now considering that the non-equilibrium function approaches exponentially f_0 once the disturbance has finished one may write the collision operator as:

$$C[f] \approx -\frac{f - f_0}{\tau(x, p, t)} \tag{C.11}$$

This form of the Boltzmann transport equation is called the Boltzmann Transport equation under relaxation time approximation (RLA). Considering an uniform n-type infinite semiconductor in steady-state with a small electric field applied. Since at steady state $\frac{\partial f}{\partial t} = 0$, in addition the electric field being small one may expect that the RLA holds. Assuming $\tau(x, p, t)$ is constant and equal to τ_0, (C.7) becomes:

$$\frac{(-q)\,\xi}{m^*}\frac{\partial f}{\partial \nu} + \nu\frac{\partial f}{\partial x} = -\frac{f_0 - f}{\tau_0} \tag{C.12}$$

where m^* is the effective mass. A general definition of current is given by:

$$J(x) = q\int \nu f(\nu, x) d\nu \tag{C.13}$$

by multiplying (C.12) by ν and integrating both sides:

$$J(x) = -q\frac{q\tau_0}{m^*}\xi\int \nu\frac{\partial f}{\partial \nu}d\nu + q\tau_0\frac{d}{dx}\int \nu^2 f d\nu \tag{C.14}$$

it can be shown that:

$$\int \nu\frac{\partial f}{\partial \nu}d\nu = -n(x) \tag{C.15}$$

$$\frac{d}{dx}\int \nu^2 f d\nu = n(x)\left\langle \nu^2 \right\rangle \tag{C.16}$$

$$J(x) = q\frac{q\tau_0}{m^*}\xi n(x) + q\tau_0\frac{d}{dx}n(x)\left\langle \nu^2 \right\rangle \tag{C.17}$$

The term $\frac{q\tau_0}{m^*}$ is usually referred as the low field mobility μ; the term $\langle \nu^2 \rangle$ is the average squared velocity that at equilibrium corresponds to $\frac{k_B T}{m^*}$. By making those substitutions one may arrive at the known drift-diffusion equations:

$$J_n = qn(x)\mu_n\xi(x) + qD_n\frac{dn}{dx} \tag{C.18}$$

$$J_p = qp(x)\mu_p\xi(x) - qD_p\frac{dp}{dx} \tag{C.19}$$

Appendix D

Effective Mobility and Matthiessen's Rule

Using the Caughey Thomas may with the Pao-Sah model one can calculate the effective mobility numerically as:

$$\mu_{eff} = \frac{q\frac{W}{L}\int_{V_{SB}}^{V_{DS}}\left[\int_{\psi_B}^{\psi_s}\mu(\psi,Vch)\frac{n(\psi,V_{ch})}{\xi(\psi,V_{ch})}d\psi\right]dV_{ch}}{q\frac{W}{L}\int_{V_{SB}}^{V_{DS}}\left[\int_{\psi_B}^{\psi_s}\frac{n(\psi,V_{ch})}{\xi(\psi,V_{ch})}d\psi\right]dV_{ch}} \tag{D.1}$$

The results for the low field mobility for different doping concentrations is shown in Fig. D.1. At low temperatures mobility rises with temperature increase since mobility dominated by coulomb scattering present a positive temperature coefficient, however when temperature increases phonon and surface roughness scattering starts to be more frequent and mobility tents to decrease with temperature increase.

When considering the temperature the modeling is more complicated, since it behavior will hugely depend on bias and lattice temperature. Usually the mobility temperature behavior is expressed as having an exponential temperature behavior with an limit exponent at high bias (predominant surface roughness scattering) of ≈ -1.5. However as the contour plot of 2.10 shows the $S_T^\mu = \frac{T}{\mu(T)} \cdot \frac{\partial\mu(T)}{\partial T}$, by considering a temperature behaviour of $\mu(T) = \mu_0 \cdot \left(\frac{T}{T_0}\right)^{-\beta} \Longrightarrow S_T^\mu = \beta$. Figure 2.10 shows that the usual assumption of $\beta \approx -1.5$ is true for high biasses and temperatures close to 300 K however this does not hold true for all temperature and especially for lower biasses.

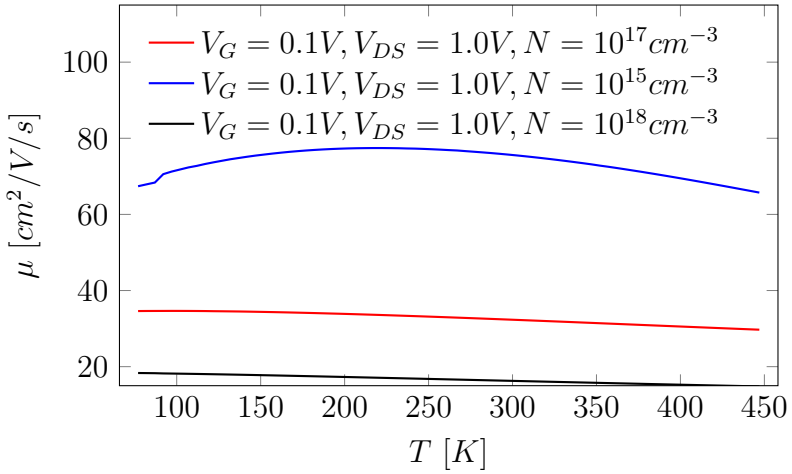


Figure D.1: Numerical calculations of the effective mobility over temperature at different doping concentrations

D.1 Mobility with Multiple Scattering Mechanisms

On Silicon the mobility is affected not only by one scattering mechanisms but multiple ones. Notably Coulomb Scattering, Phonon Scattering and Surface Roughen Scattering. This scattering mechanisms relaxation times have a power law dependency with momentum. To investigate how multiple scattering mechanisms affects the silicon low-field mobility lets consider the collision operator with two independent terms as:

$$C\left[f\right] = -\frac{\delta f}{\tau_1(p)} - \frac{\delta f}{\tau_2(p)} = -\frac{\delta f}{\tau_{eff}(p)} \tag{D.2}$$

$$\tau_i = \tau_{0i}\left(\frac{p^2}{2m^* k_B T}\right)^{s_i} \tag{D.3}$$

where

$$\tau_{eff}(p) = \left(\frac{1}{\tau_1(p)} + \frac{1}{\tau_2(p)}\right)^{-1} = \frac{\tau_{01}\tau_{02}\left(p^2/2m^*k_BT\right)^{s_1+s_2}}{\tau_{01}\left(p^2/2m^*k_BT\right)^{s_1} + \tau_{02}\left(p^2/2m^*k_BT\right)^{s_2}} \tag{D.4}$$

when $s_1 = s_2$ the effective relaxation time is exactly the impedance parallel of the individual relaxation times:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} \tag{D.5}$$

which is known as Matthiessen 's rule and states that the mobility may be deduced from the mobility due to each mechanism acting alone. Matthiessen's rule is often used to estimate mobility when multiple scattering mechanisms are present, but it must be stressed that Matthiessen's rule applies only when $s_1 = s_2$. Because independent scattering mechanisms rarely have the same energy dependence, the use of Matthiessen's rule is rarely justified in practice.

Appendix E

Symmetric Linearization Models

Symmetric Linearisation models rely on a numerical fast algorithm to calculate the surface potential at the drain and bulk sides. By defining q_b as the normalize bulk charge to the oxide capacitance per unit area (C_{ox}) and q_i the C_{ox} normalized inversion charge, by charge neutrality:

$$q_i = -(V_{GB} - V_{FB} - \psi_s) - q_b \tag{E.1}$$

By defining since deep in the bulk no inversion charge is present q_b can be taken as the approximated depletion charge:

$$q_b = -\text{sign}\left(\psi_s\right)\gamma\sqrt{\psi_s - \phi_T\left[1 - e^{-\frac{\psi_s}{\phi_T}}\right]} \approx -\gamma\sqrt{\psi_s - \phi_T}; \psi_s > 3\phi_T \tag{E.2}$$

By introducing the helper functions and variables:

$$u = \frac{\psi_s}{\phi_T} \tag{E.3}$$

$$P(u) = e^{-u} - u - 1 \tag{E.4}$$

$$D(u) = \Delta\left(V_{ch}\right)\left[e^{u} - u - 1 - \chi(u)\right] \tag{E.5}$$

$$\Delta\left(V_{ch}\right) = e^{-\frac{2\phi_B + V_{ch}}{\phi_T}} \tag{E.6}$$

$$G = \frac{\gamma}{\sqrt{\phi_T}} \tag{E.7}$$

where, $\chi(u)$ is an smoothing function to avoid numerical issues when $u \to 0$. using the defined functions the KVL at the MOSCAP and normalized charges can be written as:

$$\left(\frac{V_{GB} - V_{FB}}{\phi_T} - u\right)^2 = G^2 \left[P(u) + D(u)\right] \tag{E.8}$$

$$q_b = -\phi_T G \sqrt{P} \tag{E.9}$$

$$q_i = -\frac{\phi_T G D\left(u\right)}{\sqrt{P\left(u\right) + D\left(u\right)} + \sqrt{P\left(u\right)}} \tag{E.10}$$

The main approximation taken by symmetric linearizations models is that the normalized channel inversion charge can be expressed as a function of the inversion charge at the point in which the surface potential is equal to the mean of the ψ_s at the source and the drain. By using this assumption, on the charge sheer model, the drain to source current can be obtained by

$$q_i = q_{im} + \alpha \cdot s \tag{E.11}$$

$$\alpha = \left(\frac{dq_i}{d\psi_s}\right)_{\psi_s = \psi_m} = \frac{1 + G\left(1 - e^{-u_m}\right)}{2\sqrt{P\left(u_m\right)}} \tag{E.12}$$

$$s = \psi_s - \psi_m \tag{E.13}$$

By implying this approximation the Charge-Sheet current model can be expressed as:

$$I_{DS} = \int_0^L -\mu W C_{ox} \left(q_{im} + \alpha \cdot s - \alpha\phi_T\right) \frac{ds}{dy} \cdot dy = \mu_{eff} \frac{W}{L} C_{ox} \left(-q_{im} + \alpha\phi_T\right) \left(\psi_{sD} - \psi_{sS}\right) \tag{E.14}$$

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