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Development of low noise setup "on" and "off" wafer up to 325 GHz for the performance evaluation of silicon technology

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UNIVERSITÉ DE LILLE
ECOLE DOCTORALE SPI
DOCTEUR EN ÉLECTRONIQUE, MICROÉLECTRONIQUE, NANOÉLECTRONIQUE ET MICRO-ONDES

Development of low noise setup "on" and "off" wafer up to 325 GHz for the performance evaluation of silicon technology

Mise au point de banc de mesure de bruit "on" et "off" wafer jusqu'a 325 GHz pour l'évaluation de performances de technologies silicium

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Haitham GHANEM

A thesis submitted in fulfillment of the requirements for the degree of Doctor of Philosophy

THz Photonics Group
Institut d'électronique de microélectronique et de nanotechnologie (IEMN)

Décembre 2nd, 2020

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General Introduction

Development of low noise setup "on" and "off" wafer up to 325 GHz for the performance evaluation of silicon technology

A recent study made by “eMarketer” , which is a subscription-based market research company that provides insights and trends related to digital marketing, media, and commerce, showed that in 2020, around 2.96 billion people use the internet and social. This value is expected to increase to over 3 billion people by 2021 [1]. This demanded an increase in the capacities of the transmission channels and the design of communication systems with high data rates [2]. To cope with the market, one can design systems with large bandwidth, and a high signal to noise ratio (SNR), which means that the power delivered to the systems must be maximized, and greater than the noise power or losses in the system. For this purpose high frequency bands (> 30 GHz) are of great interest.

Nowadays, as device technology is rapidly improving, interest in the higher frequency band grows (frequencies above 110 GHz). Wireless communication systems migrate to higher frequencies, millimeter-wave radars and passive sensors find new solid-state implementations that promise improved performance, electronic components are fabricated to have high cut-off frequencies where entirely new applications in the mm-wave and Tera-hertz bands become feasible. Fig.1 shows some of the available features and components associated to each frequency band on the RF frequency spectrum [3].

Furthermore, as the maturity and development of this fabrication process of the wireless systems is rapid , circuit or system designer is faced with a new and unique set of challenges and constraints to deal with in order to use this portion of the spectrum successfully. In particular, the advantages of component integration become increasingly important [4, 5]. In order to overcome these challenges and constrains a deep understanding of the RF systems is required. To accomplish this, characterization of electronic systems is performed through S-parameter measurements, power measurements and **RF noise measurements.**

Here lies the interest of this thesis, where we discuss the characterization of noise in RF systems and devices. The first chapter states some basic definitions of terms and concepts that are used in noise characterization. It also presents the state of the art in the field of noise measurements and the available devices used such as noise sources. In the second chapter, we discuss the assembling of an off wafer test bench to perform noise characterization up to 260 GHz. We also characterize a newly developed integrated noise source based on silicon technology, and the extraction of the ENR of this noise source. Then the noise source and the assembled noise receiver were used to perform noise measurements of active devices up to 260 GHz.

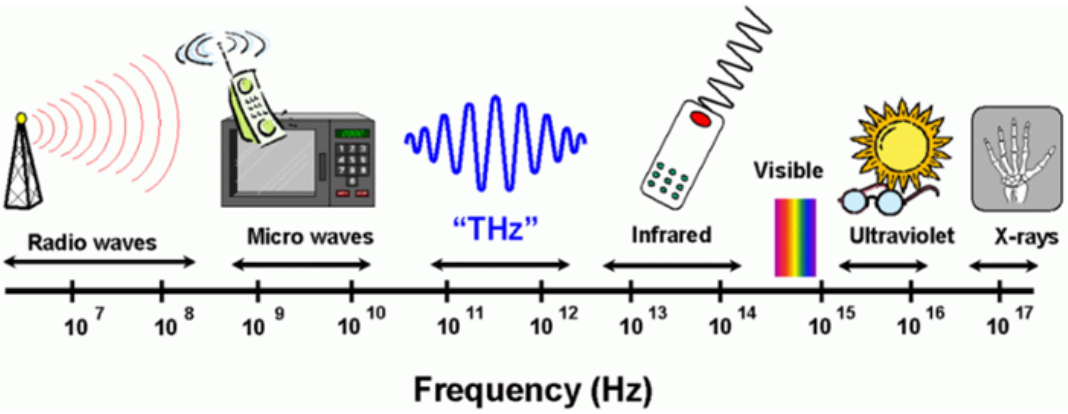

FIG. 1: Available features and applications associated to RF frequency bands [3].

Moreover, we develop the electrical model of the integrated noise source up to 325 GHz, and extend the ENR measurements up to 325 GHz using a newly assembled noise receiver structure. In the third chapter the study of an optical noise source is also performed, where we use a UTC-PD as a noise source to perform noise measurements up to 325 GHz after extracting the ENR value, the results are then compared to the integrated silicon based noise source. Also the UTC-PD is used as a two tone generator to extract the intermodulation points of active devices around 300 GHz. In the fourth chapter, we discuss the design and fabrication of a low noise amplifier using BiCMOS technology from STmicroelectronics. The LNA will be used in the noise characterization test bench in front of the noise source, after that the noise figure is extracted using the assembled noise measurement set-up.

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Chapter 1

Noise In Components and Systems In The Millimetre-Wave and Sub-Terahertz Frequencies

1.1 Applications In mm-W and Sub-terahertz Frequencies

Nowadays applications such as the Internet of Things (IoT) and high data rate wireless communication systems and other high frequency applications are becoming unavoidable. The development in the microelectronics industry allows the emergence of these electronic applications for the mass market by increasing the performance of the latest-generation transistors. The millimeter-wave (mm-W) frequency band is defined when working between 30 and 300 GHz (which corresponds to a wavelength (λ) included between 1 and 10 mm), while tera hertz range covers signals with frequencies between 100 GHz and 10 THz (which corresponds to a wavelength (λ) included between 3mm and 30 um). As mentioned earlier several applications in this frequency range in the field of telecommunications, imaging and medical domain are attracting more attention [6, 7].

1.1.1 Imaging

Imaging and detection systems based on Terahertz and sub-terahertz frequencies has long gained an interest in several fields such as radio astronomy and security screening. The capability that THz frequency offers, is a good penetration through obscurant (such as clothing) with good spatial resolution. An application example is illustrated in Fig.1.1, where a passive terahertz imaging system is used to scan an object inside the envelope held by the man presented in the image[8].

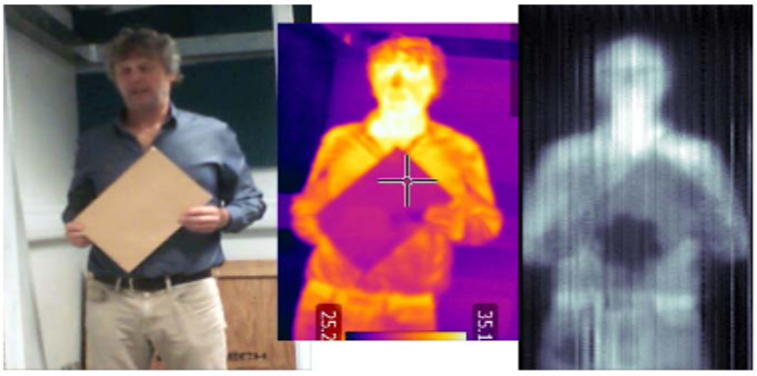


FIG. 1.1: Passive THz imaging system [8].

1.1.2 Telecommunication

Today's overloaded networks, and the evolution of social media applications and 4k streaming increase the demand for high data rate communication systems and large bandwidth spectrum in order to cope with the increasing market. For 5G technology for example, several attempts where launched to develop the circuits dedicated to cope with the 5G connectivity. Such circuits and systems should provide a breakthrough in terms of speed and power efficiency. Fig. 1.2 shows a 5G connection scenario where several items are connected to a base station, where it will be able to manage many customers by wireless link such as smart phones, drones or connected cars that will evolve within reach, using a mm-wave point-to-point bit-rate 100 Gbit.s-1 link, wireless or optical fiber [6, 9].

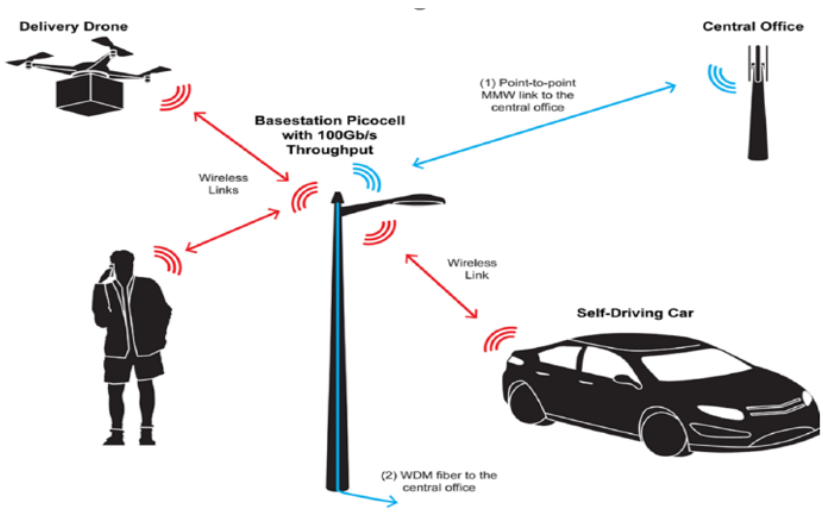


FIG. 1.2: 5G connection scenario where several items are connected to a base station [6].

Moreover, emerging applications for vehicle radars are also operating in high frequency range. Radar sensors, operating at 77 GHz for long range and 122 GHz

for short range, would allow accurate speed or distance evaluation, thus reducing the risk of collision [10].

1.1.3 Industry Quality Control

Companies take advantage of THz systems in applications concerning quality and process control, as they are used to work in a contact free environment and in very high speed measurements. These applications are important especially if it involves rapidly moving samples, for example, items on a fast conveyor belt need to be screened with high resolution. Fig. 1.3 shows an example using THz system in quality control application, where folded boxes are being scanned while moving at speed more than 20 m/s.

FIG. 1.3: 1D-scan of folded cardboard boxes with and without a package slip. This graph shows the transmitted terahertz intensity while the boxes moved at a velocity of 21 m/s [11].

We mention these applications among many other examples (Telecommunication, radar applications, imaging applications...) to highlight the fact that a huge market and several applications are now feasible if working with mm-W and sub-THz spectrum. The design of such complex systems is based on accurate and reliable electrical models of active devices like MOS and bipolar transistors.

These models are extracted and validated through high frequency (HF) measurement, including small signal, large signal and noise characterization. Furthermore, in high frequency applications the noise level becomes of major importance to ensure good performance of integrated devices. Throughout this thesis we will be focusing of the study of the "Noise" parameter and the methods with which we can extract and characterize such parameter. In addition, we will present the study of noise sources and the design of an experimental test bench to perform the noise measurements of electronic devices in high frequency range [11].

1.2 Technology Advancements and Electronic Components

Technology advancement to address the market's growing demand for the fabrication of advanced electronics systems will require simultaneous advances in materials science and technology in order to meet the performance demands of new electronic components. In this section we introduce the basic components used in building RF circuits and the state of the art properties of transistor technology.

1.2.1 Transistors

Transistors are the building blocks of any modern integrated electronic circuits, and the use of a transistor is inevitable when designing complex RF systems. The continuous improvement of the silicon CMOS and bipolar technology made it possible to fabricate advanced transistor circuits with higher cut-off frequencies ft/fmax, which made it possible to fabricate advanced and improved systems in high frequency range. This was possible by reducing the size and gate length of transistor. Fig. 1.4 shows the cut-off frequency ft, the maximum oscillating frequency Fmax and the gate length parameter of CMOS technology devices advances in recent years [12].

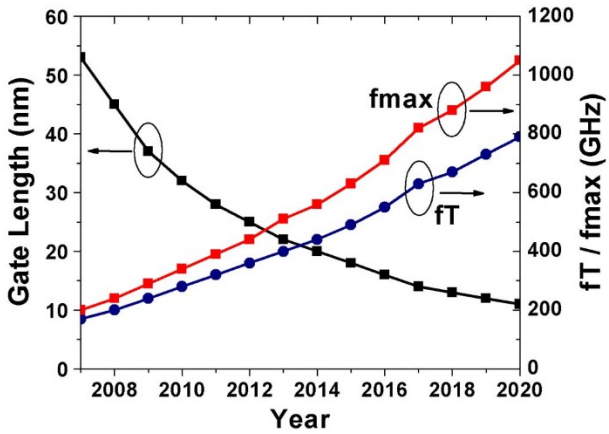


FIG. 1.4: Ft/fmax dynamics and the gate length parameter of CMOS technology devices advances in recent years [12].

While CMOS technology is very useful for fabricating simple, low power logic gates, bipolar transistors provide higher speed and gain which is important for high frequency analog application. BiCMOS technology combines high-performance bipolar transistors and CMOS technology on a single chip, and are powerful components for building high performance RF blocks such as amplifier [13].

Table 1.1 presents the features of the SiGe Bipolar and BiCMOS technology for some industrial manufacturers.

III-V MMIC semiconductor technologies (primarily GaAs and InP HEMT) are also suited for the RF front ends of mm-W systems such as power amplifiers and low

TABLE 1.1: Features of The SiGe Bipolar and BiCMOS Technology For Some Industrial Manufacturers.

Company	technology	Ft/fmax (GHz)
Freescale	HiP6MW	200/280
	HiP6MW2	260/350
IBM	BiCMOS8HP	210/270
	BiCMOS8XP	260/320
	BiCMOS9HP	300/350
Infineon	B7HF200	190/250
	B11HFC	240/380
Tower Jazz	SBC18H3	240/270
	SBC18H4	275/350
STmicroelectronics	BiCMOS9MW	220/280
	BiCMOS055	320/370

noise amplifiers, as well as enabling oscillators with excellent phase noise characteristics. The cut-off frequency ft, the maximum oscillating frequency Fmax of several technologies are shown in Fig. 1.5 [14]. All these technologies and advancements in the transistor fabrication made it possible to design high performance systems and components to be used in the mm-W and terahertz frequencies.

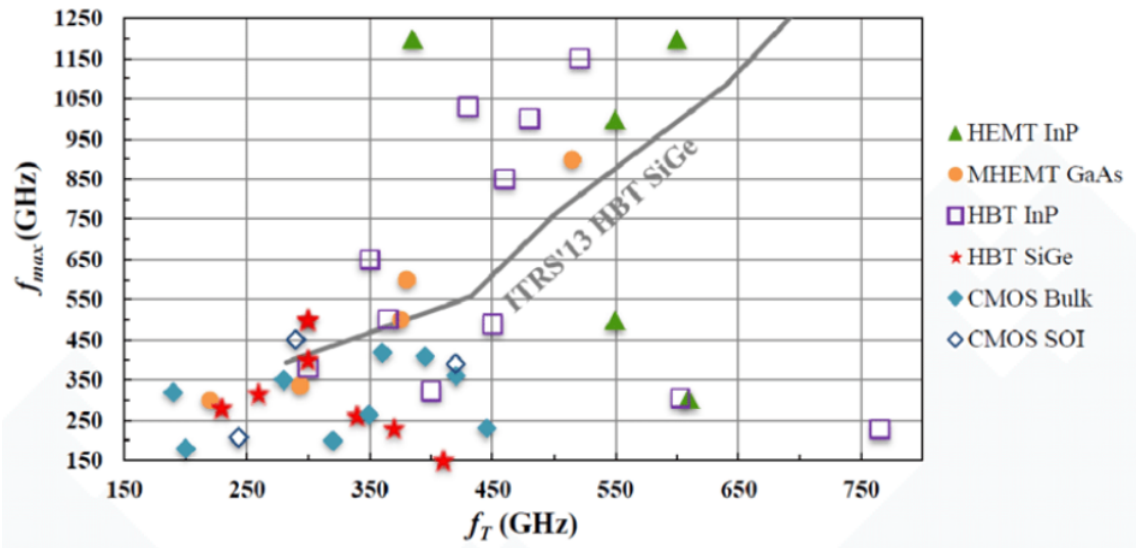


FIG. 1.5: The cut-off frequency ft, the maximum oscillating frequency Fmax of several technologies.

1.2.2 Active Circuits and Components For mm-W and Sub-terahertz Range

With this development in the transistor technology, and the emerging millimetre wave applications, the interest and attention for circuit integration is very high [15].

This comes with the goal of cost reduction and fast production. Many approaches are done to integrate active circuits such as power amplifiers, low noise amplifiers, power detectors and many others, using MOS or Bipolar transistors. All these active circuits have gained a lot of attentions especially in the domain of wireless communications that has undergone an unprecedented evolution, moving rapidly through a series of generations [16]. Fig. 1.6 illustrates a simple example of a system (Receiver chain) with several active circuits.

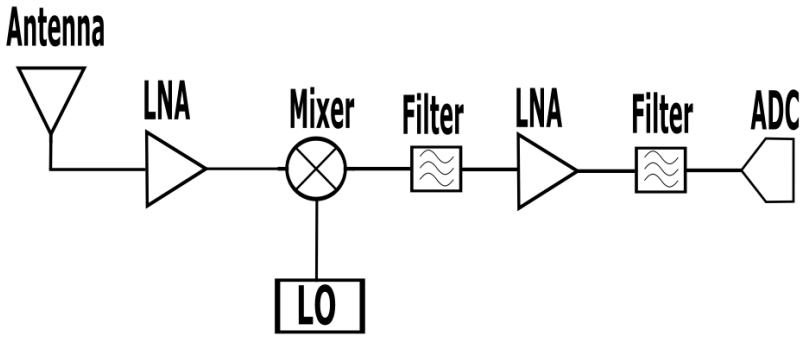


FIG. 1.6: Block diagram of a Receiver chain with several active circuits.

In the following receiver architecture for example, the low-noise amplifier (LNA) constitutes one of the essential components. The five fundamental parameters of the LNA are: gain and bandwidth, noise figure, linearity, impedance matching and power consumption [17]. For optimal performance the LNA design must consider minimising its noise figure, providing a high gain with sufficient linearity, and establishing compatibility to other transceiver blocks in other words to be matched to previous or following stages. The additional constraint of low power consumption is imposed in portable systems. Further analysis of the LNA will be considered in chapter 4.

Dealing with RF signal transmission, in order to measure the power level of this radio signal is using a detector. Among the several types of detector, one important parameter is the Noise-equivalent power (NEP), which determine the noise floor for which the minimum signal power can be detected by the detector.

Another important block in the receiver will be the mixer where it is used to down convert or up convert the signal from one frequency band to another. In passive down converters for example, to insure minimum signal losses of the converted signal, the mixer should have a low noise figure or conversion loss.

The design of such complex systems requires accurate and reliable electrical models of these active devices. These linear and non-linear models are extracted and validated through high frequency (HF) measurements performed when the device operates under small or large signal conditions. In all devices mentioned above we notice that the noise level plays an important role to insure the performance of the system and to see the signal degradation throughout the system. For this purpose we should also consider noise characterization.

1.3 Noise In Millimetre Frequency Bands

The term "Noise" is normally used to express the unwanted fluctuations that may disturb the information propagation within the signal, or reduce the quality of its contents [18]. Concerning electronic systems, this noise can be internal from within the system components, or external from the surrounding environment. Noise power can be a result of random processes such as the flow of charges or holes in an electron tube or solid-state device, propagation through the ionosphere or other ionized gas, or, most basic of all, the thermal vibrations in any component at a temperature above absolute zero [19]. Such motions may be due to any of several mechanisms, leading to various types of noise such as thermal noise, shot noise or flicker noise. In order to retrieve the information within a signal, the noise should be eliminated or reduced.

Types of Noise

The noise source of an electronic circuit can originate from the noise sources in a transistor. For that, noise in transistors and active circuits have been of interest throughout the literature for many years, and in this section we will specify briefly the types of noise that can originate within these devices [20]. Basically, there are 4 types of noise sources that we can define:

- **Thermal noise:** It is one of the main noise sources in the RF and electronic circuits. This mechanism occurs in all resistors or any device having a resistive impedance. It is generated as a result of the vibration of the charge carriers (electrons) within an electrical conductor, which vibrates due to temperature. The higher the temperature, the higher the vibrations and hence the thermal noise level. In a transistor, thermal noise can originate from the extrinsic base resistor. '

  Thermal noise cannot be cancelled, its effect can only be reduced through a decrease of the temperature of operation of the component, or by reducing the value of the resistors in the circuit. Moreover, thermal noise is one of the main limiting factors when designing an electronic device. For example it limits the sensitivity of RF receivers because it sets a noise floor below which signals cannot be detected.

- **Shot noise:** Shot noise is due to the discrete nature of the charges carried by electrons or holes, since current consists of a vast number of discrete charges, and is not a totally analogue phenomenon. In devices such as transistors for example, shot noise is due to the fact that the output current is not smooth and continuous but is the sum of numerous small pulses caused by the passage within the device of discrete electronic charges. Unlike thermal noise, shot noise is dependent upon the current flowing and not on the operating temperature of the system. Shot noise is particularly noticeable in semiconductor devices, such as tunnel junctions, Schottky barrier diodes, PN junctions and on the base current and the collector current of transistors. Also shot noise can

limit the performance of active electronics circuits and thus should be taken into account when designing RF circuits such as amplifiers and detectors [21].

- **Flicker noise:** This is low frequency noise for which the noise power is inversely proportional to the frequency, thus it is also known as 1/f noise. In transistors for example it is proportional to emitter current and junction temperature [22]. Several theories went to explain the origin of the flicker noise, among these are: the McWhorter number fluctuation theory and the Hooge mobility fluctuation theory. The McWhorter theory, working with germanium, proposed that flicker noise is primarily a surface effect. On the contrary the Hooge theory propose that 1/f noise is not a surface effect but rather a bulk phenomenon [23].
- **Avalanche noise:** Which is normally generated in diode junctions when biased in reverse near the avalanche region. Avalanche noise is later described in section 1.5.1.

1.4 Fundamentals of Noise Measurements

When studying the noise performance of the devices or systems we have to deal with some main parameters, and well-known terms and formulas used to perform such measurements. In this section we go back to some basic definitions such as Noise Figure, Noise temperature, Signal to noise ratio and other noise parameters, which are useful and important to understand when dealing with noise characterization. We also define fundamental equations explaining the relations between these terms.

1.4.1 Noise Power and Noise Temperature

An important aspect to begin with is to define the power of the Noise generated within the electronic components (noise Power). For a simple case we will consider a resistor at a physical temperature T (in Kelvin) Fig. 1.7. There will be a random movement of the electrons within the resistor with a kinetic energy that is proportional to the temperature. This random motion produce small random voltage fluctuations at the resistor terminals, which is considered a source of noise. This in fact is the Thermal noise we defined in the previous section. This voltage has a zero average value but a nonzero root mean square (rms) value and can be expressed as in (1.1):

$$V_n = \sqrt{\frac{4hfBR}{e^{\frac{hf}{kT}} - 1}} \tag{1.1}$$

Where:

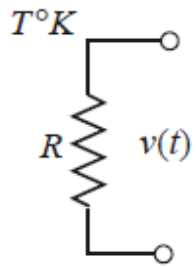


FIG. 1.7: A resistor at a physical temperature T.

h= 6.626×10^{-34} J s is Boltzmann constant

k= 1.38×10^{-23} J K^{-1} is Planck's constant

T is the temperature in Kelvin

B is the bandwidth of the system in Hz

f is the centre frequency of the bandwidth in Hz

R is the resistance in Ω

In cases where hf < < KT (at mm-w frequency range for example), using the Taylor series expansion for the exponential term:

$$e^{\frac{hf}{KT}} - 1 \approx \frac{hf}{KT} \tag{1.2}$$

Then the term in equation (1.1) can be reduced to the term seen in (1.3):

$$V_n = \sqrt{4kTBR} \tag{1.3}$$

Now to see the generated noise power from this noise source, we can replace the noise resistor in Fig. 1.7 by a noiseless resistor in series with a generator with a voltage given by equation (1.3). The maximum power transfer from the noisy resistor to a noiseless load resistor with the same resistance R (a matched load) in a bandwidth B is given in (1.4):

$$P_n = \frac{{V_n}^2}{2R} = kTB \tag{1.4}$$

This result gives the available noise power transferred from the noisy resistor at temperature T. This noise power is independent of frequency; the power spectral density of this noise source is constant with frequency, and is an example of a white noise source.

In addition, noise temperature is one way of expressing the level of available noise power introduced by a component or source. Now suppose we have an arbitrary noise source that delivers a noise power N_0 to a load of impedance R. This noise source can be replaced by a noisy resistor at an equivalent temperature T_e, where T_e is an equivalent temperature selected so that the same noise power is delivered to the load as from the original noise source. This equivalent temperature can be expressed as in (1.5) [24] :

$$T_e = \frac{N_0}{kB} \tag{1.5}$$

Throughout the literature, many labels are given to describe the noise temperature of a two-port system, such as available, equivalent or effective noise temperature. Usually all the derived noise temperature equations are **available** noise temperature. In this thesis we should note that when using noise temperature it is defined as the **equivalent** or **available** values. Whereas **effective** noise temperatures means the delivered noise temperature where the source is not necessary matched to the input of the network [25].

1.4.2 Noise Figure

Another parameter that is considered to characterize a two-port is the Noise Figure. The Noise Figure indicates the degradation of the signal to noise ratio between the input and the output of a system. Therefore, we should first define the signal to noise ratio, which is the ratio of the desired signal available power both at the input and output of the system (S_i/S_o) to the unwanted available noise power (N_i/N_o) at the input and the output of the system. Then the noise figure can be expressed as in 1.6:

$$F = \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}} \tag{1.6}$$

Fig. 1.8 shows a noise power N_i and a signal power S_i being fed into a noisy network with a gain G, a bandwidth B and an equivalent temperature T_e. The input power at the networks input port is the sum of the input signal power and the input noise power (1.7).

$$P_i = S_i + N_i \tag{1.7}$$

Similarly, the output power of the network is the sum of the output signal power

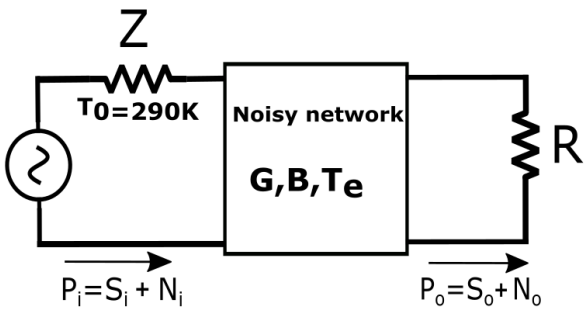


FIG. 1.8: Input and output signal and noise powers of a noisy two-port network.

and the output noise power (1.8).

$$P_o = S_o + N_o \tag{1.8}$$

Where the output signal power is the input power of the input signal multiplied by the gain of the network (1.9).

$$S_o = GS_i \tag{1.9}$$

On the other hand, the output noise power is the input noise power multiplied by the gain of the network plus an extra noise power added by the noisy network itself (1.10).

$$N_o = GN_i + N_{\text{added}} \tag{1.10}$$

In the example shown in Fig. 1.8 the input noise power is that of the resistor (R) at temperature T_o, $N_i = kBT_o$.
Then the output noise power can be written as N_o, according to T_e, the equivalent noise temperature brought back at the input of the network.T_e expresses the equivalent noise temperature of a virtual impedance Z located at the input of the network that produces the same noise power as of the noisy network. In other words it models the noise power generated by the noisy network. The noise figure writes (1.11):

$$F = \frac{\frac{S_i}{N_i}}{\frac{S_o}{N_o}} = \frac{S_i N_o}{S_o N_i} = \frac{kBG(T_o + T_e)}{GkBT_o} = 1 + \frac{T_e}{T_o} \tag{1.11}$$

So the equivalent noise temperature of the network can be related to the noise figure (1.12):

$$T_e = (F - 1)T_o \tag{1.12}$$

We should note that this definition of the noise figure applies in case of a source impedance Z (see Fig. 1.8) whose temperature is equal to T_0=290K. If the reflection

coefficient of the source at the input is changed, this will affect the value of F and thus T_e.

1.4.3 The Y-Method

Ideally, to determine the equivalent noise temperature of a two-port device, one must measure its output noise power when the input of the component is connected to a matched load at 0 k. This is of course impossible since we cannot obtain a 0 k source, then another method should be carried out to determine the equivalent temperature and this is called the Y-method [24]. It is carried out by measuring the output noise power of the component (if we suppose that the output powers are measured using a noiseless noise receiver, whose noise was accounted using the calibrated standard noise source) corresponding to a calibrated standard noise source at two different temperatures. To illustrate this method, consider the simple example in Fig. 1.9. Let

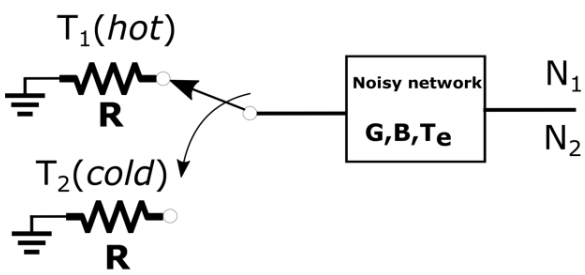


FIG. 1.9: Output noise powers measured at the output of a component corresponding to a matched noise source at two different temperatures.

T_1 be the hot temperature of the source and T_2 is the cold temperature of the source ($T_1 > T_2$). N_1 and N_2 are the corresponding noise powers measured at the output of the network. Referring to the previous definition of noise power we can write:

$$N_1 = kGBT_1 + kGBT_e \tag{1.13}$$

$$N_2 = kGBT_2 + kGBT_e \tag{1.14}$$

Where G is the available gain of the network, B is the bandwidth and T_e is the equivalent noise temperature. The available power at the output of the network is the input available noise power multiplied by G in addition to the available noise power added by the network itself. Using the Y-method we define the Y-factor as the ratio between the two noise powers measured at the output of the network 1.15.

$$Y = \frac{N_1}{N_2} = \frac{T_1 + T_e}{T_2 + T_e} \tag{1.15}$$

So the equivalent noise temperature can be deduced as in 1.16 :

$$T_e = \frac{T_1 + Y.T_2}{Y - 1} \tag{1.16}$$

1.4.4 FRIIS Formula For Noise

Electronic systems usually consists of several components. Thus the signal travels through a number of components, each with a different signal to noise ratio. The total noise figure of the system can be determined knowing the noise figure at each stage. The following example shows the calculation of the total noise figure of a two-stage system each with its own noise characteristics Fig. 1.10. The input available

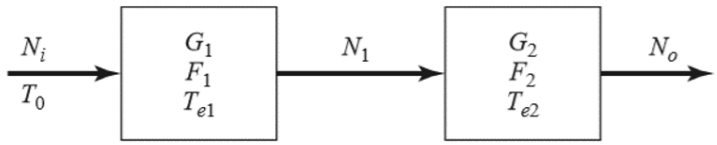


FIG. 1.10: Multi stage system of noisy networks.

noise N_i comes from a input load held at a temperature T_0, the first stage is a network with gain G_1, equivalent noise temperature T_{e1} and an noise figure F_1. Similarly the second stage is a network having a gain G_2, equivalent noise temperature T_{e2} and a noise figure F_2. The noise power (N_1) at the output of the first stage can be written as in 1.17:

$$N_1 = N_i.G_1 + N_{\text{added by stage 1}} = kBT_oG_1 + kBT_{e1}G_1 = kBG_1(T_0 + T_{e1}) \tag{1.17}$$

Similarly the noise power N_o at the output of the second stage (system output) can be expressed as in 1.18:

$$N_0 = N_1.G_2 + N_{\text{added by stage 2}} = kBG_1G_2(T_0 + T_{e1}) + kBT_{e2}G_2 \tag{1.18}$$

Which gives:

$$N_0 = kBG_1G_2(T_0 + T_{e1} + \frac{T_{e2}}{G_1}) \tag{1.19}$$

So for the cascade system we have:

$$N_0 = kBG_1G_2(T_0 + T_{\text{cascade}}) \tag{1.20}$$

where $T_{\text{cascade}} = T_{\text{e1}} + \frac{T_{\text{e2}}}{G_1}$

Using 1.12 we convert the noise temperatures to noise figure:

$$T_{\text{cascade}} = T_{\text{e1}} + \frac{T_{\text{e2}}}{G_1} = (F_1 - 1)T_0 + \frac{(F_2 - 1)T_0}{G_1} \tag{1.21}$$

1.21 can be written as:

$$T_{\text{cascade}} = (F_{\text{cascade}} - 1)T_0 \tag{1.22}$$

where

$$F_{\text{cascade}} = F_1 + \frac{(F_2 - 1)}{G_1} \tag{1.23}$$

It can be deduced that for any system of (n) cascade stages, the overall noise figure and the overall equivalent temperature is given by:

$$F_{\text{cascade}} = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} ... \tag{1.24}$$

$$T_{\text{cascade}} = T_{\text{e1}} + \frac{T_{\text{e2}}}{G_1} + \frac{T_{\text{e3}}}{G_1 G_2} ... \tag{1.25}$$

1.4.5 Excess Noise Ratio (ENR)

Usually noise sources are characterized and measured for their performance by the Excess Noise Ratio (ENR), which is the noise level above the noise floor. The ENR is a ratio in dB between two noise temperatures of a noise source, taken for two states of power measured from the noise source. It is then calculated using the Y-method explained earlier.

$$ENR(dB) = 10 \log \frac{T_H - T_C}{T_0} \tag{1.26}$$

Where T_0 is the standard noise temperature (in K). T_C and T_H are the equivalent noise temperatures of the noise source. Usually we turn the noise source between ON and OFF states in order to get the two different noise temperatures. To simplify, we consider in (1.26) that T_C corresponds to the room temperature, considered to be

equal to T_0. Thus (1.26) can be simplified to (1.27):

$$ENR(dB) = 10\log(\frac{T_H}{T_0} - 1) \tag{1.27}$$

Moreover, the ENR value can be linked to the noise figure. To derive this relation we should recall the term "Y-factor", which is defined as the ratio between two measured noise powers each related to a noise temperature (1.28). Consider the scenario shown in Fig. 1.11. The two noise powers P_{hot} and P_{cold} measured at the output of a network of gain G, correspond to the two equivalent noise temperatures T_H and T_0 respectively.

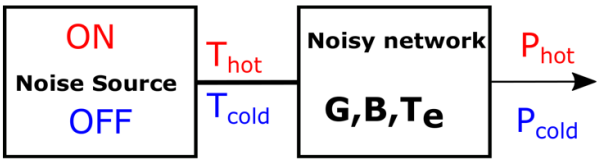


FIG. 1.11: Noise power measured for two noise temperatures.

$$Y = \frac{P_{hot}}{P_{cold}} \tag{1.28}$$

Using 1.4 we can write $P_{hot} = kT_{hot}BG + N_{added}$ and $P_{cold} = kT_0BG + N_{added}$

Then

$$Y = \frac{kT_{hot}BG + N_{added}}{kT_0BG + N_{added}} \tag{1.29}$$

Using 1.27 we can write:

$$Y = \frac{k(ENR + 1)T_0BG + N_{added}}{kT_0BG + N_{added}} \tag{1.30}$$

$$Y = 1 + \frac{kBGT_0ENR}{kT_0BG + N_{added}} \tag{1.31}$$

Substituting in 1.11 the Y factor can be written as shown in 1.32:

$$Y = 1 + \frac{ENR}{F} \tag{1.32}$$

Then we see the relation relating the Excess noise ratio to the noise figure directly as:

$$ENR = F(Y - 1) \tag{1.33}$$

The method will be further discussed in following sections, when characterizing the noise source and doing the extraction of the noise figure.

1.5 Basic Blocks In a Noise Test Bench

One of the main limitations when designing a noise measurement test bench on high frequencies is the availability of the noise source. Also, as we will see in later chapters, the noise power produced from a noise source decreases as frequency increases, making it more difficult to detect this noise signal. Thus we need a sensitive noise receiver with adequate noise figure and sensitivity to perform noise measurement at frequencies in the millimetre range or sub tera-hertz range. In the following section, we will present the basic blocks and concepts used in a noise receiver to perform noise measurements in the millimetre wave range. Also we will define briefly the noise sources that can be used to generate the noise power and the state of the art of the studied noise sources using various technologies used for noise generation at the frequency of interest.

1.5.1 Diode Noise Sources

In previous section we described the type of noise sources that can be present in electronic devices such as thermal, shot and flicker noise. We also said that such noise sources can be present in semiconductor junctions such as p-n or Schottky junctions Fig. 1.12. Over the years diodes have been used as noise sources when

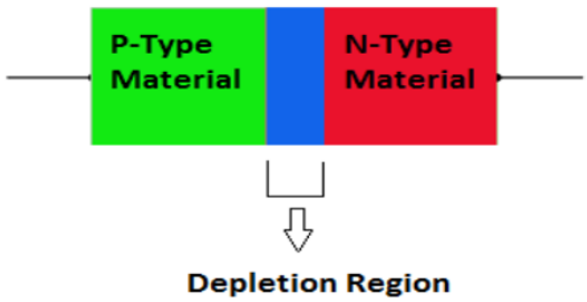


FIG. 1.12: P-N junction diode structure.

they are reverse-biased to avalanche breakdown. The produced noise at the voltage breakdown is another type of noise source called avalanche noise. Fig. 1.13 represent the $I - V$ characteristic of a diode.
Under forward bias conditions the I-V behaviour of the diode (junction) is presented in the right side in Fig. 1.13. While in the reverse biasing conditions (when the current is flowing from the cathode to the anode side) the I-V characteristics are presented in the left side in Fig. 1.13.

For our case, to use the diode as a noise source, we are concerned with the second case where the diode is reverse biased. Under low voltage conditions the diode will not allow any current to pass through the junction, ideally the reverse current is zero [26]. Though in reality we notice a small current seen on the graph which corresponds to a leakage current, which is the result of drifting of charge carriers from the junction region to terminal region. This drift is caused by the electric field generated by depletion region. If the reversed applied voltage continue to increase, we will reach a limit where the junction is broken and the current passing through the junction will increase rapidly (infinite current). This is shown on Fig. 1.13 where V_{BD} is called the breakdown voltage and it sets the limit of the biasing allowed in reverse before the junction is destroyed. The noise generated during this mechanism is the avalanche noise [27]. In semiconductors avalanche breakdown occurs when

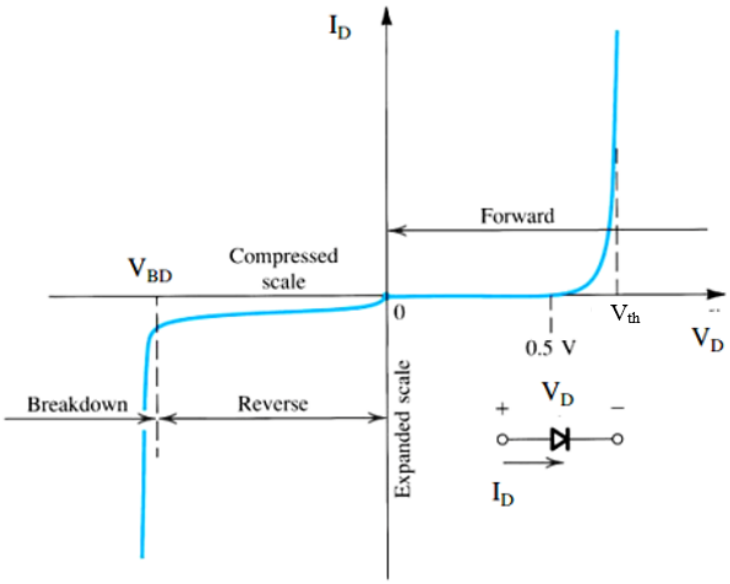


FIG. 1.13: I-V curve of a diode showing the avalanche break down.

carriers in the junctions gain energies in a high electrical field and then they collide with the crystal lattice. If the energy gained during these collisions is high enough, carriers can collide with other charge creating another carriers (electron hole pair). This way the revised biased current can be multiplied. This process is random and the noise source is associated with this avalanche carrier generation. The intensity of the avalanche noise is usually much larger than any other noise component. This process can happen in PN junctions and Schottky diodes. Silicon based Schottky diodes and GaAs Schottky diodes are commonly used as RF noise sources in the millimetre wave range [21, 28]

1.5.2 Optical Noise Source

Uni travelling carrier photodiode (UTC-PD) are also used as noise sources to carry out reliable characterizations in the millimeter wave (mm-W) and sub-terahertz frequency range [29]. The mechanism of noise generation in photodiodes is different from what was described in solid state diodes (p-n and schottky junctions). The electrical noise is basically generated by converting the broadband optical noise into electrical noise using the UTC-PD. The set-up is shown in Fig. 1.14 and consists of an Er-doped fiber amplifier(EDFA) with no input and a UTC-PD. The origin of the

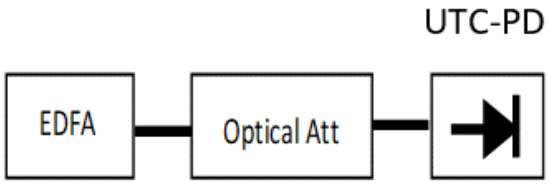


FIG. 1.14: Optical noise generation.

optical noise is the amplified spontaneous emission (ASE) noise from an Er-doped fiber amplifier (EDFA). The noise power is determined by the responsivity of the PD and intensity of the input optical noise. To control the generated noise level we use an optical attenuator to control the optical noise level [30].

The following table 1.2 presents the state of the art of noise sources used for noise generation and the ENR associated to use source. Several technologies are used such as silicon diodes (p-n junctions, Schottky junctions and CMOS diodes), diodes in the bulk of transistors, GaAs based diodes and photodiodes.

TABLE 1.2: State Of The Art Of Noise Sources and The Associated ENR.

Technology	Device	Frequency (GHz)	ENR (dB)	Silicon integration	Ref
Packaged	Waveguide	75-110	14	NO	[31]
III-V GaAs	Schottky diode	170-220	10	NO	[28]
UTC-PD	Photodiode	285-325	10-30	NO	[29]
90-nm CMOS	CMOS diode	0-24	20-25	YES	[32]
55-nm BiCMOS	Schottky diode	130-325	5-20	YES	[33, 34]

1.5.3 Minimum Detectable Signal (MDS)

The Minimum detectable signal (MDS) is the minimum input power required at the input port of a receiver (RCV) in order to provide a relevant output. We can also define it as the minimum power requested at the input of a receiver to ensure a particular signal to noise ratio at the output.

Recall from section (1.3.1 and 1.3.2) the relation between the noise temperature and noise figure in a system. To show the relation between the MDS and input power required at the input of a receiver, suppose we have the system shown in Fig. 1.15. The

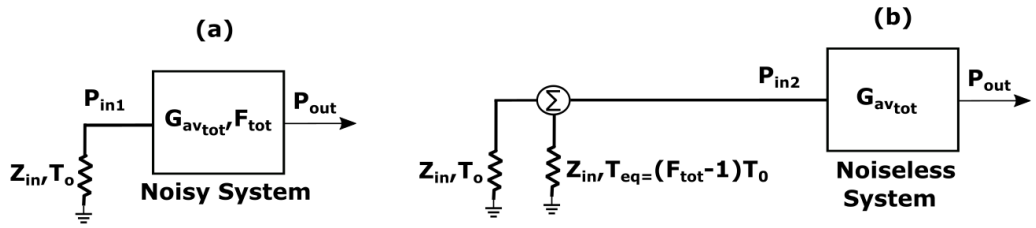


FIG. 1.15: Input and output power of a noisy system.

noisy network in Fig. 1.15.a has a noise figure F_{tot} and gain $G_{av_{tot}}$, and is connected to a noise source at temperature T_0. The output power can be expressed as follows[6]:

$$P_{out} = P_{in} G_{av_{tot}} + P_{\text{Noise added}} \tag{1.34}$$

This can also be expressed as the system shown in Fig. 1.15.b, as a noiseless network having a gain $G_{av_{tot}}$ and connected to the same noise source at temperature T_0 and another source at the equivalent noise temperature T_{eq}.
Then the output power can be expressed as follows:

$$P_{out} = P_{in2} G = kT_{tot} GB \tag{1.35}$$

$$P_{out} = k(T_{eq} + T_0)GB \tag{1.36}$$

Substituting $T_{eq} = (F-1)T_0$, we have:

$$P_{out} = kGFT_0B \tag{1.37}$$

The same methodology can be used to calculate the input power at a receiver port. Consider the diagram shown in Fig. 1.16: Using the same procedure, we can see that the input power at the receiver side can be expressed as:

$$P_{\text{in RCV}} = kF_{\text{RCV}}T_0B = P_{\text{MDS}} \tag{1.38}$$

Referring to Fig. 1.17,to ensure the MDS conditions we should have:

$$P_{out} \geq P_{\text{MDS}} \tag{1.39}$$

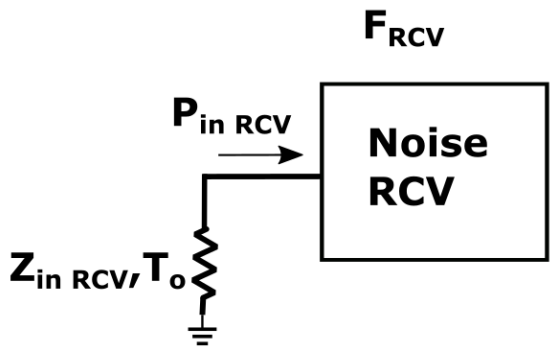


FIG. 1.16: MDS power of a receiver.

$$kGT_0F\Delta f \geq kF_{\text{RCV}}T_0B \tag{1.40}$$

$$GF \geq F_{\text{RCV}} \tag{1.41}$$

If we convert to dB values, we have the total power at the input of the receiver, which should be greater than the noise figure of the receiver plus a 3 dB margin.

$$G(dB) + NF(dB) \geq F_{\text{RCV}}(dB) + 3dB \tag{1.42}$$

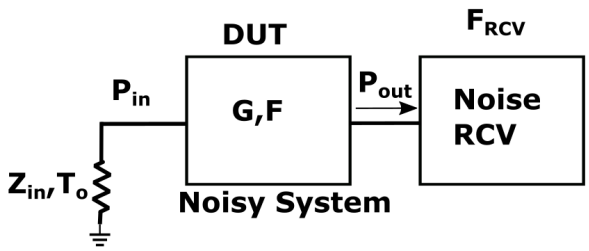


FIG. 1.17: MDS Power Condition.

1.5.4 Low Noise Amplifier (LNA) in Noise Source

For the noise measurement test bench, we are dealing with small signals with low power level. At RF frequencies, the NF of the component increases and so does the signal losses. In order to ensure the MDS conditions explained previously (Fig.

1.17), we need to increase the gain on the source side [35]. Thus, we need to use an amplifier in front of the source in order to increase the signal level, keeping in mind not to increase the losses by much. For that, a low noise amplifier is usually used. The test bench will be as shown in Fig. 1.18: Using high performance transistors,

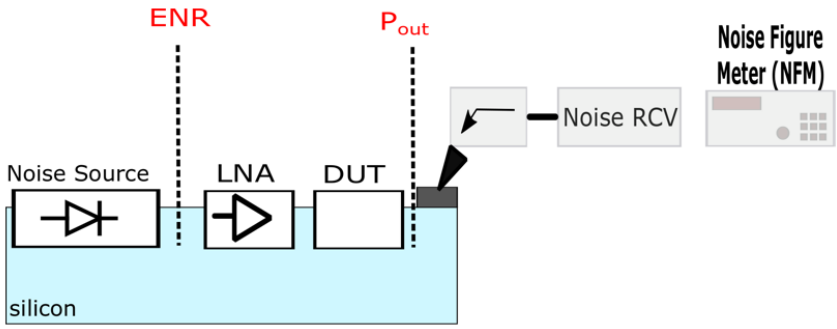


FIG. 1.18: Test Bench Setup to Perform Noise Measurements.

many LNA circuits have been designed and used in small signal and large signal systems. HEMT III-V based technology is used to fabricate LNA with high gain and low noise figure at the device operating frequency. However, these technologies cannot be integrated within silicon chips. Advances have been made with LNA design using CMOS and BiCMOS technologies, to be used in the RF frequency range. In the noise test bench set-up, it is preferred for the LNA to be placed close to the noise source in order to decrease the losses due to connections and probes. For that, it is interesting for this work if the LNA is integrated on silicon close to the noise source circuit. The design of such amplifier will be further discussed in a later chapter.

1.5.5 Frequency Conversion

In the signal path of a receiver, we will use the down conversion phenomena to translate the RF signal to the intended base band frequency range for analysis. Generally, we use mixers in order to perform this frequency translation, by multiplying two signals. Mixers usually have three different ports as shown in Fig. 1.19 [23]. In the case of down conversion an RF input signal is applied to the input of the mixer. The assumed RF signal can be of the form:

$$RF(t) = V_{\mathrm{RF}}.\cos(2\pi.f_{\mathrm{RF}}t) \tag{1.43}$$

The mixer will then modulate this signal by another local oscillator signal (LO) having the form:

$$LO(t) = V_{\mathrm{LO}}.\cos(2\pi.f_{\mathrm{LO}}t) \tag{1.44}$$

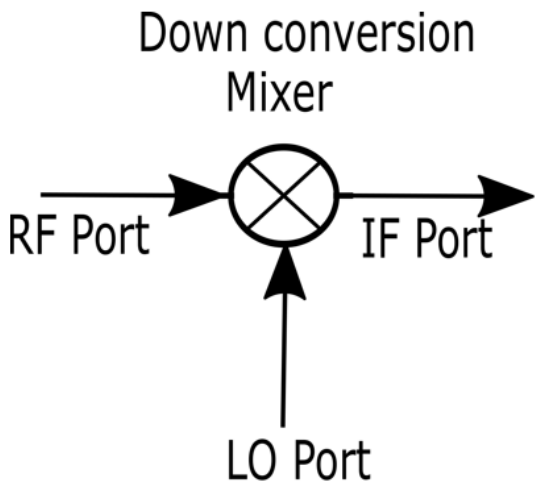


FIG. 1.19: Frequency down converter.

Then the IF output of the mixer will be:

$$IF(t) = V_{\mathrm{LO}}.V_{\mathrm{RF}} \cos(2\pi.f_{\mathrm{RF}}t).\cos(2\pi.f_{\mathrm{LO}}t) \tag{1.45}$$

$$IF(t) = \frac{V_{\mathrm{LO}}V_{\mathrm{RF}}}{2}[\cos((2\pi)(f_{\mathrm{RF}} - f_{\mathrm{LO}})t) + \cos((2\pi)(f_{\mathrm{RF}} + f_{\mathrm{LO}})t)] \tag{1.46}$$

Then it is seen that the IF output signal of the mixer consists of the sum and difference of the two input signals (RF and LO)(Fig. 1.20).

$$f_{\mathrm{IF}} = f_{\mathrm{RF}} \pm f_{\mathrm{LO}} \tag{1.47}$$

So far we have considered CW signals, both for the RF and LO signals. In the context

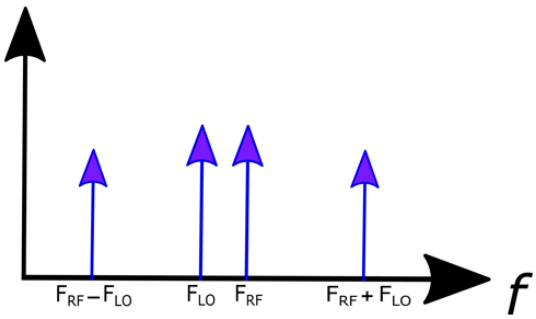


FIG. 1.20: Output signal of a down converter and its image.

of this thesis,the RF signal is a broadband noise corresponding to the frequency band of interest. The noise power at the output of the system is measured and analysed

using a noise figure meter or a power meter operating at much lower frequencies. Down converters are then needed to transfer the noise signal from the RF frequency band of the noise to the frequency of the measuring instrument, using a reference LO signal.
There are several types of down converters that can be used for frequency transfer such as sub-harmonic mixers (SHM), even harmonic mixers (EHM) and fundamental mixers (FM). Throughout this work we will only use the sub-harmonic mixers (SHM) when assembling a noise receiver, although other types are also possible.

When choosing a mixer to use in the measurement set-up, one should consider several characteristics.

- *Conversion loss:* This accounts for the resistive losses in the mixer and the losses in the frequency conversion process from RF to IF ports. It is defined as the ratio of available RF input power to the available IF output power in dB.

$$L = 10 \log \frac{\textit{available RF input power}}{\textit{available IF output power}} \tag{1.48}$$

  The mixer should be matched at the three ports (RF, LO, IF) due to the fact that several frequencies and their harmonics are involved. Minimum conversion loss is required to minimize the losses in the RF power converted.

- *Noise Figure:* In mixers noise is generated from the diodes or transistors in the structure. The noise figure of a mixer depends on whether its input is a single-sideband signal or a double sideband signal. This is because the mixer will down-convert noise at both sideband frequencies (since these have the same IF), but the power of a SSB signal is one-half that of a DSB signal [24].

- *Port Isolation:* In ideal cases the LO and RF ports would be decoupled, but internal impedance mismatches and limitations of coupler performance often result in some LO power being coupled out of the RF port.

Some state of the art found in literature are presented in Table. 1.3.

TABLE 1.3: Frequency Converters Specifications.

Type	**Frequency (GHz)**	**Loss (dB)**	**NF (dB)**	**P_{LO} (dBm)**	**Technology**	**Ref**
Active	148-158	4.5	-	2	CMOS 45nm	[36]
Active	113-127	12	33.5	9	CMOS 65nm	[37]
Pasive	130-185	12/13	-	2.8	CMOS 45nm	[36]
Pasive	130-170	20.5	18.3	2.9	CMOS 65nm	[38]
Active	154-165	20	8	3	CMOS 65nm	[39]

1.6 Conclusion

In the first chapter, we introduced the concept of electronic noise and the motivation for performing noise measurements in the millimeter and sub-terahertz frequency range. This is due to the advances made in the micro and Nano technology, and the ever-increasing cut off frequency and enhanced performance of transistor devices, where several applications in this frequency band are now possible. We presented some of the fundamental definitions of noise and noise measurements, where these concepts and equations will be used throughout the thesis. Also we talked about the types of noise sources that can originate in semiconductors such as thermal noise, shot noise, flicker noise and avalanche noise. Moreover, we introduced some of the basic blocks used in noise measurements test bench set-up (for the noise source and the noise receiver). Furthermore, noise generation using diode noise sources was introduced (p-n and schottky junctions) CMOS diodes, and photodiodes. This concept of noise generation will be more detailed throughout the manuscript as we use these devices in the studied test bench required for noise measurements. A state of the art of the technology and some important devices was also presented to give a better view of the development of device applications in the mm-W and sub-terahertz frequency range.

1.7 Thesis Objectives

The aim of this work is to develop a test bench set up to perform noise characterization of wave-guide and integrated devices in the millimetre frequency range. We start by continuing an ongoing work for assembling an OFF wafer receiver and performing noise figure measurements of waveguide devices up to 260 GHz frequency range using a newly developed integrated silicon based noise source. The integrated noise source is also characterized and the ENR value is extracted up to this frequency (260 GHz).

The following step was to extend the frequency range of the measurements to higher frequencies by characterizing a new assembled receiver dedicated to perform the measurements above 260 GHz (up to 325 GHz). The ENR value of the integrated diode noise source is then measured up to 325 GHz using the new assembled receiver structure. Furthermore a comparison between the silicon based integrated noise sources with an optical noise source (uni-travelling photodiode) is performed. Beyond this proof of concept to use the developed integrated noise source to perform the extraction of the noise figure of electronic devices, the electrical noise model of the source is developed to better understand the functionality and to enhance the performance of the device. To validate the noise measurements up to 325 GHz, noise measurements were done on wave-guide devices up to this frequency.

Also an integrated low noise amplifier was designed using BiCMOS 55 nm technology from STMicroelectronics. The device is then characterized up to 260 GHz, and the noise figure is extracted using the developed noise set-up. This device will

be then used next to the integrated noise source as part of the noise test bench, towards designing a fully integrated noise test bench. [40]

Chapter 2

Noise Measurements Test Bench Up to 325 GHz

In the first chapter, the motivation of designing a noise measurement test bench to extract the noise performance of silicon devices was expressed, which define the aim of this thesis. In addition, some general definitions related to electrical noise were stated. In this chapter we address the design and assembly of noise characterization test bench, which consists of performing noise measurements on active and passive devices using both commercially available external elements and on wafer integrated elements. First we recall the available bench set-up used to cover noise measurements on the D-band frequency range (110-170 GHz) .

The block diagram of the characterization bench dedicated to perform noise measurements in D-Band is available at IEMN and is shown in Fig. 2.1.

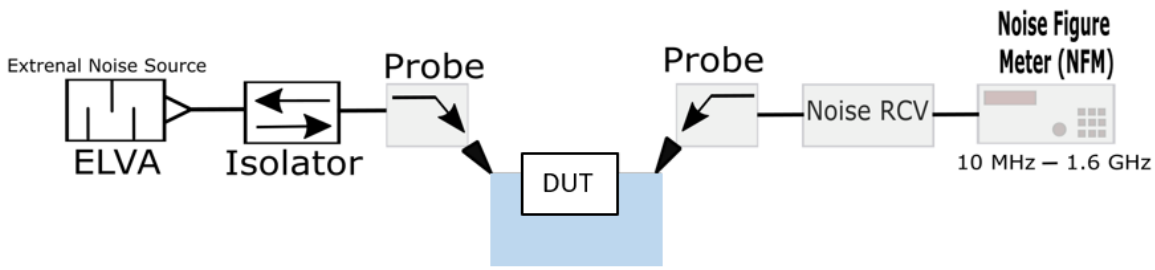


FIG. 2.1: Bench setup dedicated for noise measurements on D-band.

It consists of an external solid-state noise source (ELVA) with an ENR value up to 16 dB (Fig. 2.2). GSG probes are used to connect the measuring external instruments to the access pads of the device under test fabricated on silicon.The noise receiver is then used to capture the RF noise signal at the output of the device where the NFM is used to measure the noise power. The noise measurements beyond this frequency is limited by the commercial availability of a noise source and the sensitivity of the noise receiver. Moreover, using and external noise source induce many losses due to

the connection losses between the source and the DUT [6].

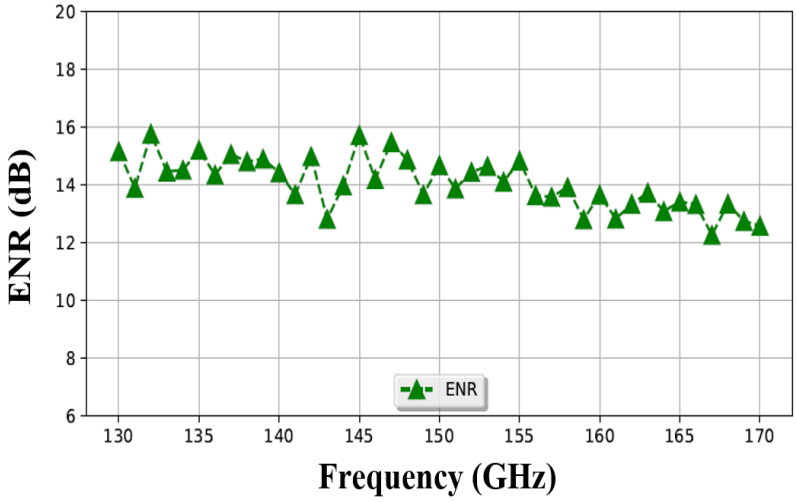


FIG. 2.2: ENR value of the external solid state noise source (ELVA)[6].

In this chapter, we extend the frequency range of the noise measurements, where a noise measurement set-up was assembled and used to extract the noise figure of an active device. The experiment set-up is carried out as follows:

- A noise receiver structure used to capture the RF noise power is assembled and characterized up to 325 GHz.
- Analysis and characterization of a silicon based integrated noise source used to generate the RF noise signal are performed.
- Noise figure of a device is extracted using the assembled system, by placing it between the source and the receiver.

2.1 Noise Receiver Structure

The noise receiver is an important block in the noise measurement test bench. To perform noise measurements in the millimetre wave range, the noise signal produced from the noise source has to be in the RF frequency range. To measure and analyse the noise signal we use a noise figure meter (NFM), in our case we use the NFM (**HP 8970B** from keysight). This NFM operated in the frequency range 10 MHz to 1.6 GHz. Then the noise receiver, placed before the NFM, is used to down convert this RF noise signal from the RF frequency range to an IF frequency, before feeding the noise figure meter (NFM), that is used as a power meter to measure the noise power. The block diagram of the noise receiver is shown in Fig. 2.3.

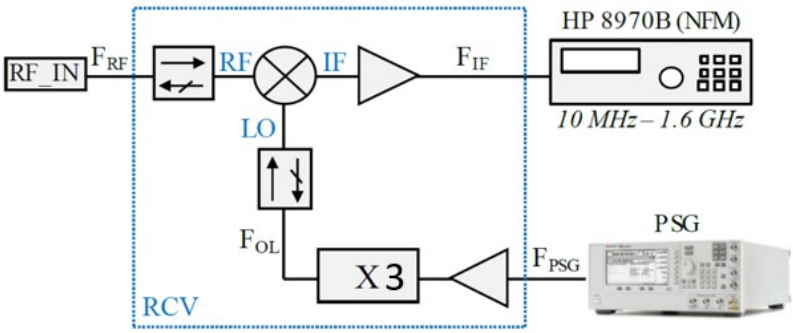


FIG. 2.3: Block diagram of a noise receiver.

The receiver consists of a mixer with an RF frequency signal as input, LO drive signal and an IF signal at the output. The RF input of the mixer is connected to the previous stage using an isolator, this is important to minimize the reflected signals from flowing back to the circuit, therefore enhancing the matching between the mixer and the previous stage. The LO drive signal is generated using a signal generator (PSG) followed by a frequency tripler to increase the frequency of the generated signal to match the required RF signal. A wave guide isolator is also used to increase the matching and minimize the reflection at the LO input. The IF output signal is followed by a low noise amplifier to compensate for the losses of the mixer and increase the level of the generated signal. To perform noise measurements at a wide frequency range (170-325 GHz) several receiver structures were used, each dedicated to a certain frequency range. Power measurements were also carried out prior to the noise power measurements in order to determine the power characteristics of the receiver such as the conversion loss, the maximum input power allowed and the optimum LO drive power [33].

2.1.1 Noise Receiver In The 170-260 GHz Frequency Range

The receiver structure used for noise measurements in the frequency band 170-260 GHz was assembled using: a sub harmonic mixer (SHM) from VDI (WR4.3SHM) with flange size WR 4.3 for the RF signal port and WR 8.6 for the LO port (LO frequency range 85-130 corresponding to RF/2 frequency). The LO required input power to drive this mixer should be between 2 and 4mW (3-6 dBm), the value suggested from the data sheet of the component. A performance signal generator (PSG) (Keysight E8257D) was used to generate the pumping power, with a frequency range 28.3-43.3 GHz. To increase the frequency range of the PSG to the required LO frequency range, a tripler (VDI product:WR8.0X3) was used with 90-140 GHz frequency range (Flange WR8.0), and a required input power of 40-240mW (16-23 dBm). To achieve this required power at the input of the tripler a broadband power amplifier was used in front of the PSG. The broadband amplifier (RF-LAMBDA product:

RAMP00M50GA) has a gain of 31-38 dB. At the IF port the signal is amplified using a LNA (MC2 technologies product:LNA1p52GHz).The noise receiver is assembled and presented in Fig. 2.4.

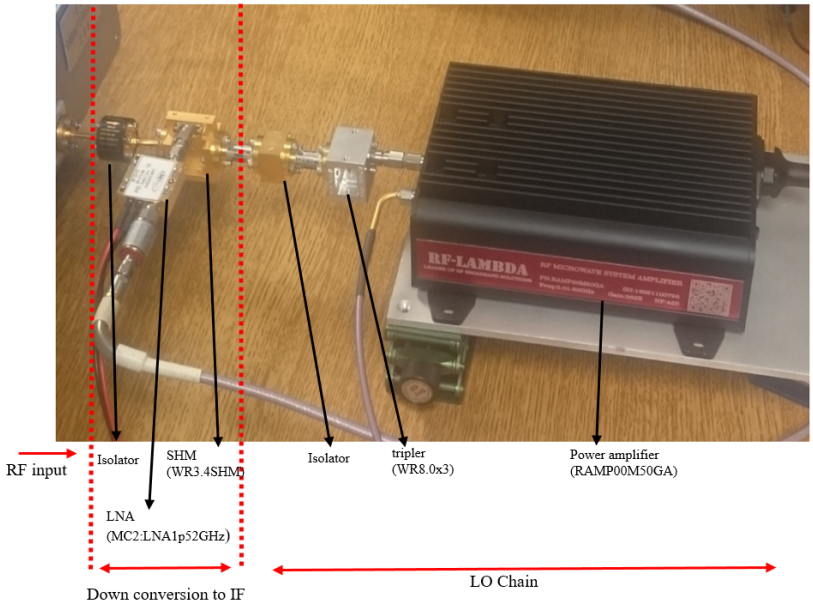


FIG. 2.4: Noise receiver in the 170-260 GHz frequency range.

To evaluate the input power (supplied by the PSG) required to pump the mixer (3-6 dBm according to the data sheet) the Lo chain of the noise receiver had to be characterized. To perform this measurement the set-up shown in Fig. 2.5 was assembled.

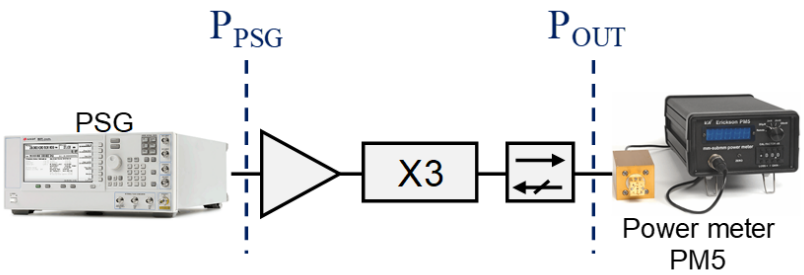


FIG. 2.5: LO chain of the noise receiver.

The PM5 power meter used in Fig. 2.5 is a calibrated calorimeter-style power meter. it offers power measurement ranges from 1 μW up to 200 mW. The sensor head has a WR10 input. The power meter PM5 (VDI-Erickson Power Meters PM5B) was used to measure the output power from the LO chain corresponding to the PSG power supplied at the input for each frequency point. Then the suitable power from the PSG yielding to an output power (at the PM5 port) in the correct range to pump

the mixer was noted, keeping in mind not to exceed the maximum input power allowed at the input of the amplifier (to make sure we do not damage the amplifier). The maximum input power allowed at the input of the amplifier is first measured by connecting the input of the amplifier to the signal generator (PSG) and the output power is read on a power meter where we measure the 1 dB compression point of the power amplifier. Fig. 2.6 shows the maximum input power allowed at the input of the power amplifier (P_{MAX}) and the input power provided by the PSG (P_{PSG}) in order to achieve the suitable power required to pump the mixer.

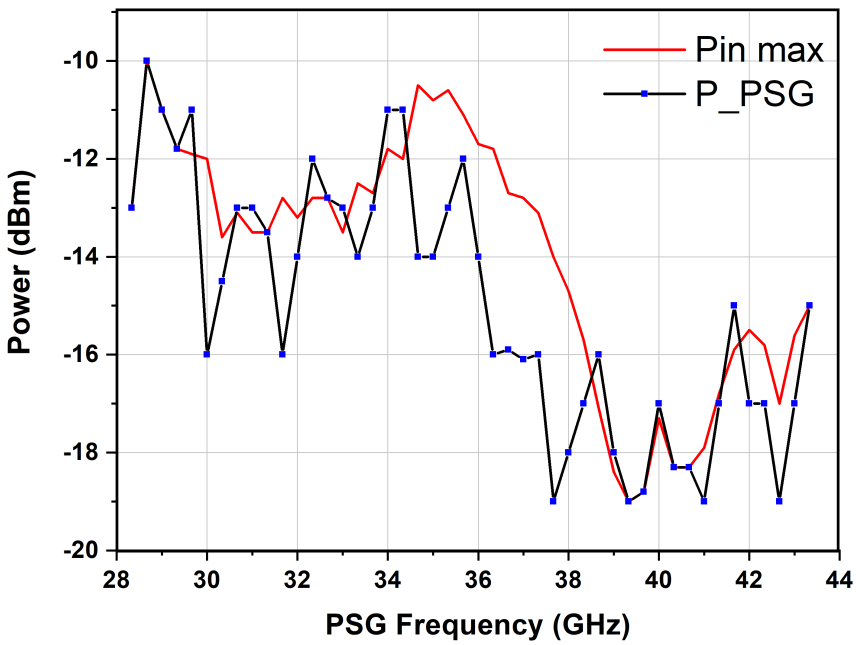


FIG. 2.6: Maximum input power allowed at the input of the LO chain and the power provided by the PSG to drive the mixer versus PSG frequency.

During the power measurements we note that at some frequency points it is not possible to achieve the required LO output power to drive the mixer without exceeding the maximum power allowed at the input of the power amplifier (i.e when P-PSG is greater than Pin max in Fig. 2.6). This is due to the frequency response of the mixer at these specific points. For the security of the amplifier these points are not used.

The second step was to extract the noise figure of the receiver, which is done using cryogenical method or else known as the hot/cold measurements. Fig. 2.7 shows the experiment mounted to perform the extraction of the noise figure of the receiver. As discussed in section 1.4.1, hot/cold measurements are done by introducing two different temperatures at the input of the device under test (in this case the noise receiver), then we measure the two powers (calibrated relative powers in dB) at the output corresponding to each temperature. The Y method is used to extract the noise figure. Therefore we are interested in the power variation between the two states.

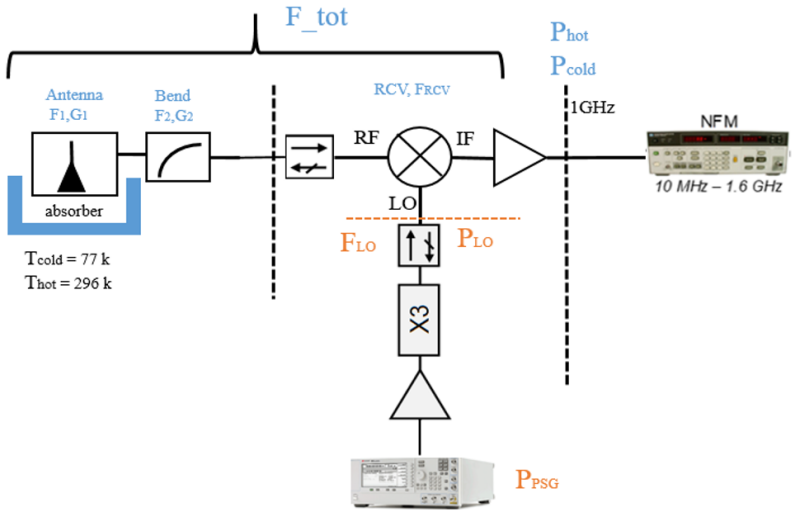


FIG. 2.7: Hot/cold experiment setup for receiver noise figure extraction.

First the equivalent noise temperature T_{tot} and the noise figure (F_{tot}) for all the elements between the noise source (antenna input) and the noise figure meter (Fig. 2.7) are extracted using the Y method.

$$T_{\text{tot}} = \frac{T_{\text{hot}} - Y.T_{\text{cold}}}{Y - 1} \tag{2.1}$$

$$F_{\text{tot}} = 1 + \frac{T_{\text{tot}}}{T_0} \tag{2.2}$$

The Y factor is calculated as the ratio between the two measurements Y= $\frac{P_{\text{hot}}}{P_{\text{cold}}}$.

The antenna is placed close to a liquid nitrogen solution used to obtain a 77 K radiator, where this is considered as the cold noise temperature (T_{cold}) and the hot noise temperature (T_{hot}) is taken at 294 K (corresponding to room temperature at 21 °C). Power measurements P_{hot} and P_{cold} are done at these two different temperatures using the noise receiver (Fig. 2.7). In this set-up the noise figure (F_1) and the loss (G_1) of the antenna are noted to be 0.25 dB, and the noise figure (F_2) and the loss (G_2) of the bend are noted to be 1 dB. Note that the measurements are all done at a room temperature of 21 °.

After the equivalent noise figure F_{tot} is calculated, and knowing the noise figure and the loss of each passive device between the source and the NFM, we use FRIIS formula to extract the noise figure of the receiver F_{RCV}(2.3,2.4).

$$F_{\text{tot}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_{\text{RCV}} - 1}{G_1 G_2} \tag{2.3}$$

$$F_{\mathrm{RCV}} = (F_{\mathrm{tot}} - F_1 - \frac{F_2 - 1}{G_1}).G_1 G_2 + 1 \tag{2.4}$$

The extracted noise figure of the receiver in the frequency range 170-260 GHz is shown in Fig. 2.8.

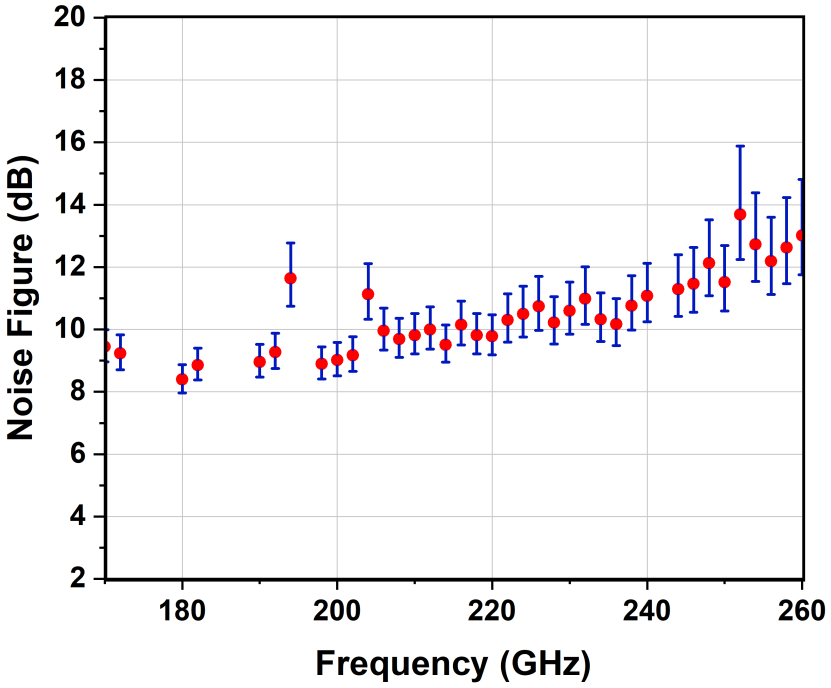


FIG. 2.8: Receiver noise figure extracted using Hot/Cold measurement.

The error bars were calculated taking into account the uncertainty in the power measurements from the NFM (taken to be 0.5 dB from the NFM manual), where the best and worst case scenario of the NF calculation is extracted as the error bar value.
Fig. 2.8 shows a noise figure of 10 dB up to 240 GHz, and it increases slightly to 13 dB at 260 GHz [33].

2.1.2 Noise Receiver In The 260-325 GHz Frequency Range

Similar to the previous receiver structure, a noise receiver for the frequency range 260-325 GHz (for the RF signal range) was assembled using: a sub harmonic mixer (SHM) from VDI (VDI Model:WR3.4SHM) with flange size WR3.4 for the RF signal port (range 220-330 GHz) and size WR6.8 for the LO port (LO frequency range 110-165 corresponding to RF/2 frequency). The typical LO input power required to drive this mixer is in the range 2-4mW (3-6 dBm), this value is suggested from the data

sheet of the component (this value is optimized as discussed after). A PSG (Keysight E8257D) was used to generate the pumping power, with a frequency range 36.6 - 55 GHz. To increase the frequency range of the PSG to the required LO frequency range, a tripler (VDI product:WR6.5x3) was used with 110-170 GHz frequency range (Flange WR6.5), and a required input power 40-180mW (16-22.5 dBm). To achieve this required power at the input of the tripler a power amplifier was used in front of the PSG. The power amplifier (Quin-Star product:MN QPI-U02132-HS01 https://quinstar.com, with frequency range 40-60 GHz) has a typical gain of 35 dB and a P1dB about 19 dBm[34]. The assembled noise receiver is presented in Fig. 2.9.

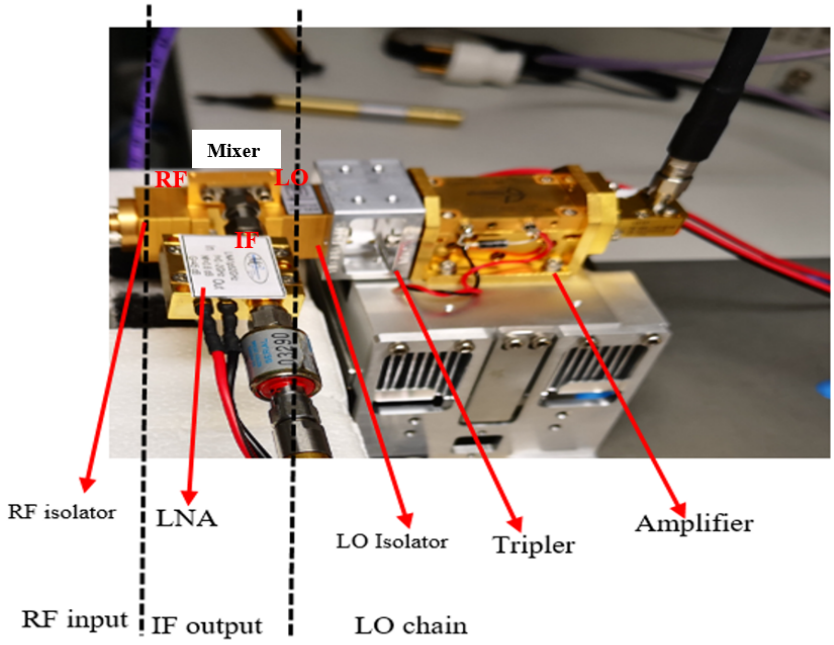


FIG. 2.9: Noise receiver structure for the 260-325 GHz frequency range.

To calculate the input power (supplied by the PSG) needed to pump the mixer at the required power a similar setup as in 2.5 is carried out .

The PM5 power meter was used to measure the output power from the LO chain corresponding to the PSG power supplied at the input for each frequency point. Then the suitable power from the PSG yielding to an output power (at the PM5 port) in the correct range to pump the mixer was noted, keeping in mind not to exceed the maximum input power allowed at the input of the LO chain power amplifier. The following graph shows the input power from the PSG power needed at the input in order to drive the mixer. The maximum input power allowed at the input of the amplifier is first measured by connecting the input of the amplifier to the signal generator (PSG) and the output power is read on a power meter where we measure the 1 dB compression point of the power amplifier. Fig. 2.10 shows the maximum input power allowed at the input of the power amplifier (P_{MAX}) and the optimum

input power provided by the PSG (P_{PSG}) provided by the PSG in order to achieve the necessary power needed to pump the mixer. The LO power detected at the output of the chain , and is fed into the mixer, is shown in 2.11 .

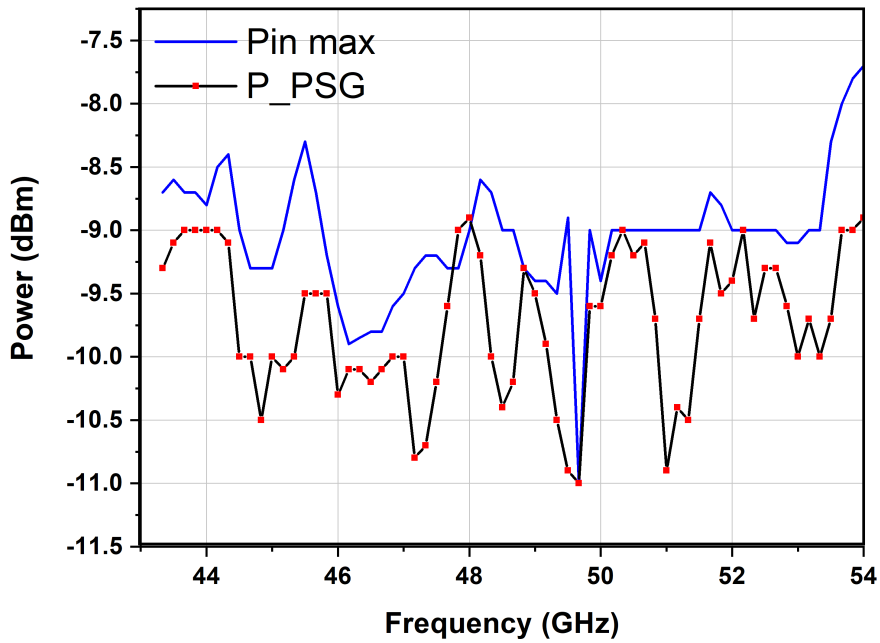


FIG. 2.10: Maximum input power allowed at the input of the LO chain and the power provided by the PSG to drive the mixer versus PSG frequency.

The following step was to extract the noise figure of the receiver , which is done using cryogenical method or hot/cold measurements (see section 1.4.1). The same experiment as in Fig. 2.7 is mounted, where the room temperature at the time of measurements for this structure was 22 °, and the antenna is placed close to a liquid nitrogen solution used to obtain a temperature of 77 K , where this is considered as the cold noise temperature (T_{cold}) and the hot noise temperature (T_{hot}) is taken at 296 K (room temperature at the time of measurements). Power measurements P_{hot} and P_{cold} are done at these two different temperatures using the noise receiver (Fig. 2.9). The block diagram of Fig. 2.7 is illustrated in Fig. 2.12 .

Equations (2.1 to 2.4) were used to extract the noise figure of the receiver, the extracted noise figure in the frequency range 260-325 GHz is shown in Fig. 2.13. The receiver has a noise figure value around 9 dB up to 310 GHz, this value increases to around 13 dB at 325 GHz. The error bars were calculated taking into account the uncertainty in the power measurements from the NFM (taken to be 0.5 dB from the NFM manual), where the best and worst case scenario of the NF calculation is extracted as the error bar value [34]. Note that one point (at 297 GHz in Fig. 2.13) is left out, since at this point the power supplied from the PSG is not sufficient to drive the

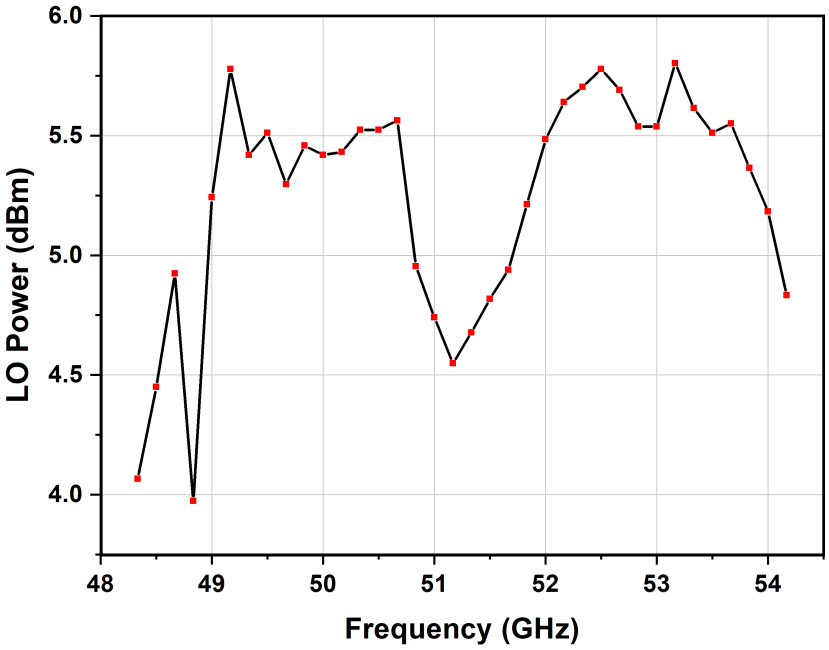


FIG. 2.11: LO power used to drive the mixer.

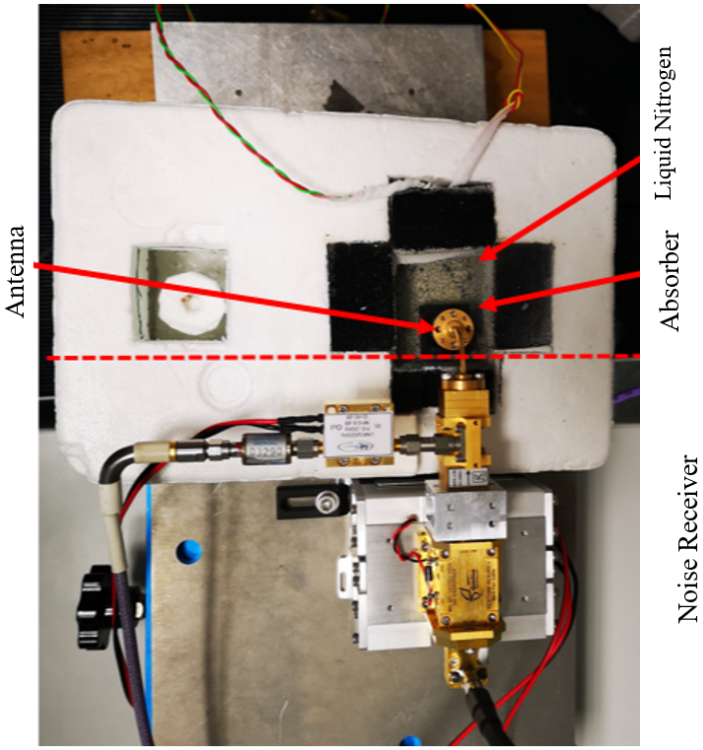


FIG. 2.12: Receiver noise figure extraction using HOT/COLD measurements.

mixer without exceeding the max input power allowed at the input of the amplifier.

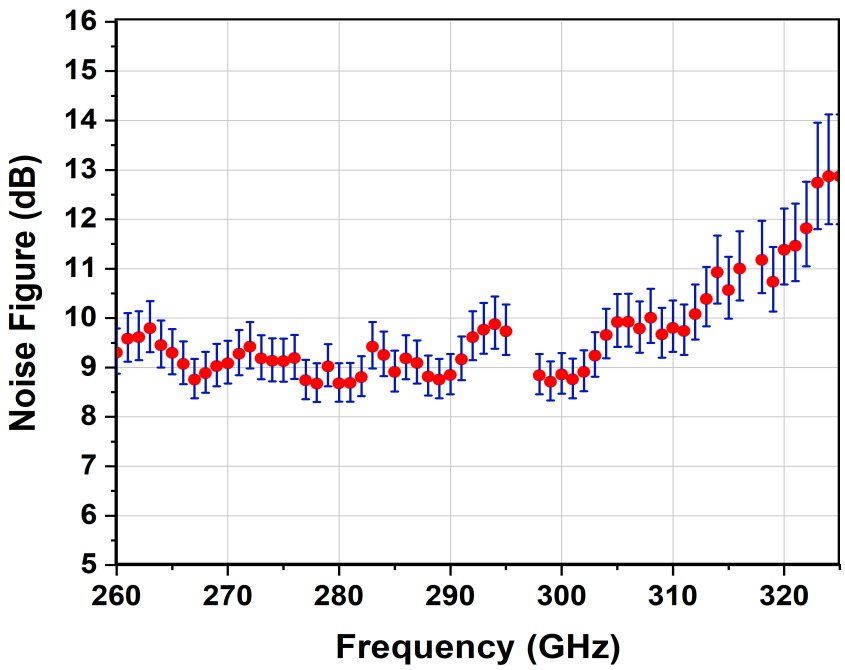


FIG. 2.13: Receiver extracted noise figure.

It should be noted that for the characterization of both the receiver structures, the power measurements were automated. A matlab code was developed to control the PSG (in order to supply the power to the mixer after knowing the optimal power needed), the current source (used to bias the integrated diode noise source) and then for each frequency point the code will read the detected power from the NFM and save it in an information file to be analysed. This gave us the advantage of performing the measurements fast, therefore preventing the liquid nitrogen solution to evaporate (decreasing the error of temperature variation of the nitrogen solution), thus increasing the accuracy of the Hot/Cold measurements.

Fig. 2.14 summarizes the extracted noise figure of all the receiver structures available at IEMN for noise measurements in the frequency range 130-325 GHz.

2.2 Integrated Noise Source ENR Extraction (170-260 GHz)

As mentioned in the previous sections, noise sources are usually characterized for the Excess Noise Ratio (ENR), which is defined as the noise level above the thermal noise floor. Usually, depending of the integration type, the ENR is calibrated with any commercial noise source, now available up to 220 GHz with ENR level of 12 dB

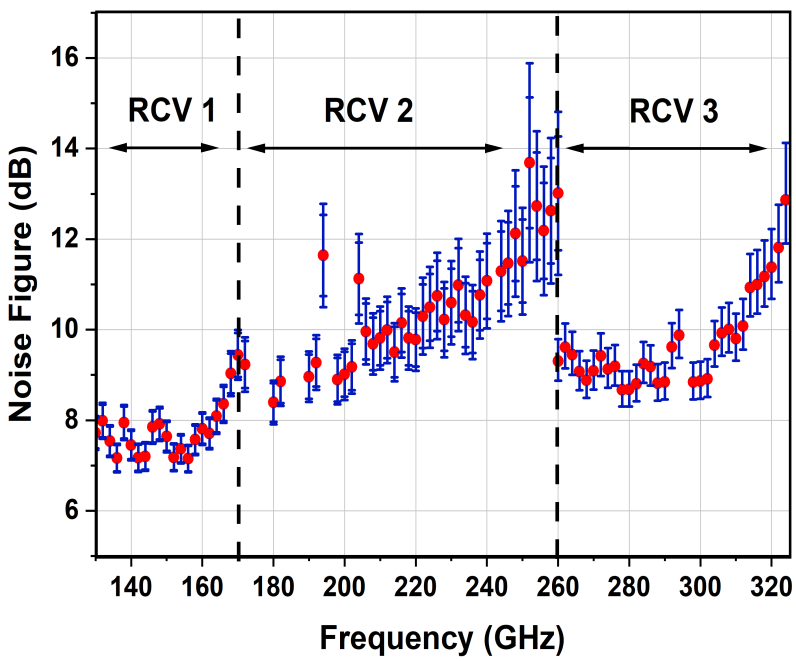


FIG. 2.14: Extracted noise figure for all receiver structures available.

[31] . The noise source used in this experiment was developed using BiCMOS 55nm technology from STMicroelectronics, as part of this work [34] , for that we should extract experimentally the ENR value.

A cross-section of the diode is shown in Fig. 2.15. The junction is a Schottky contact. This Schottky contact is formed by silicidation (Co-Si) of exposed silicon (P-type) surface between the two shallow trench isolation (STI) regions. The high doped N type silicon region (Nsinker and N+) allows a low-resistance link to the cathode from the silicide contact on the silicon surface. The STI prevents electrical shorts between cathode and anode contacts, and a deep trench isolation provides perimeter isolation from the substrate and between the devices. A P-type ground guard ring (P+ plug) is surrounding the device in order to delimitate the substrate area. M1 is the first metal layer which present the access to the active part. The contacts (cathode and anode contacts) are accessed on the third metallization layer M3. For the noise source structure, the Schottky diode on the anode is shunted to ground and its cathode connected to a RF-pad (1 port configuration) as shown in Fig. 2.16.

To extract the ENR value of the noise source the setup shown in 2.17 was mounted. The global setup is also shown in Fig. 2.18.

In this test configuration, the diode was biased through the bias tee of the RF probe by a positive current (so the diode is reverse biased near the avalanche region)

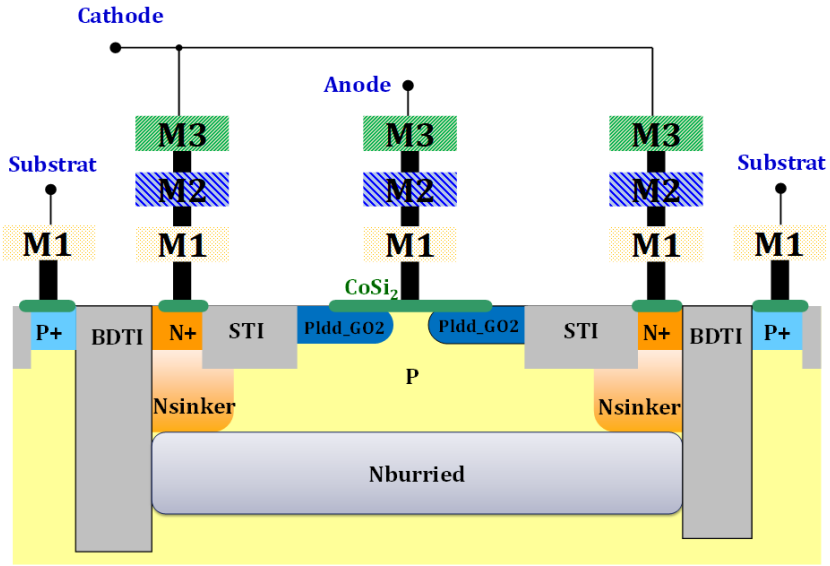


FIG. 2.15: Cross section Layout of the integrated diode noise source.

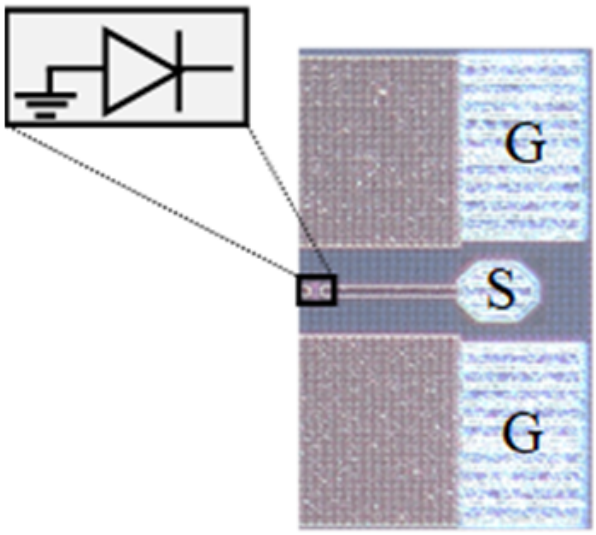


FIG. 2.16: Diode noise source (1 Port) layout [41].

for the ON state and un-biased for the OFF state (Fig. 2.19). The available noise temperature at the on-wafer reference plane A ($T_{HOT}^{A,av}$) may be obtained with the calibrated noise receiver characterized previously. In our case, the diode is unmatched at the output. Thus, the available power cannot be directly measured (Recall section 1.4.5). Therefore, a mismatch factor (M) defined by (2.5) shall be used to perform the necessary correction and take into account the mismatched impedance from the noise source (Γ_{NS} the reflection coefficient at the noise source output), where (Γ_{OUT}^{probe}) is the output reflection coefficient of the RF probe, (Γ_{IN}^{RCV}) is the input reflection coefficient of the noise receiver. The noise power can be expressed by (2.6). To reduce the transformations between noise power and noise temperature, we will combine

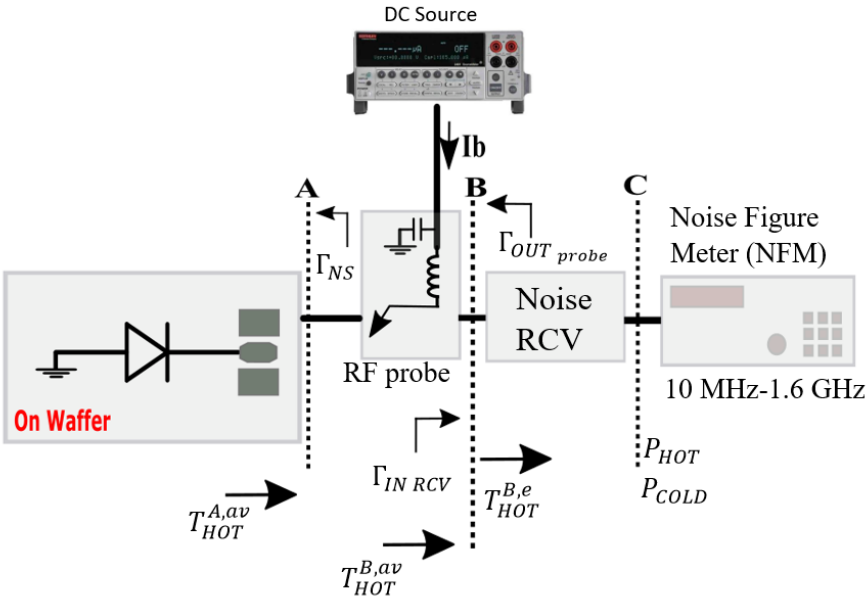


FIG. 2.17: Setup for ENR extraction of the integrated diode noise source [33].

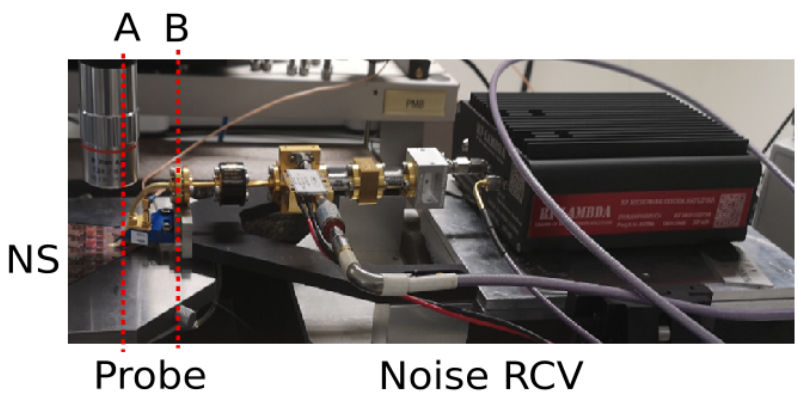


FIG. 2.18: Mounted test bench for ENR extraction of the integrated diode noise source [33].

the mismatch factor and gain with the noise temperature calculation.

$$M = \frac{1 - \left|\Gamma_{\text{OUT}}^{\text{probe}} . \Gamma_{\text{IN}}^{\text{RCV}}\right|^2}{(1 - \left|\Gamma_{\text{OUT}}^{\text{probe}}\right|^2).(1 - \left|\Gamma_{\text{IN}}^{\text{RCV}}\right|^2)} \tag{2.5}$$

$$P = K.T_{\text{noise}}\Delta f \tag{2.6}$$

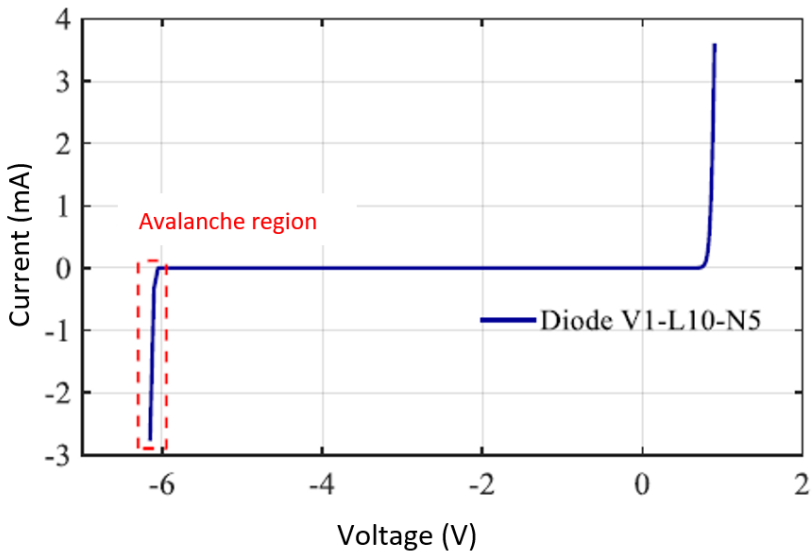


FIG. 2.19: Diode operated as a noise source when biased near the avalanche region.

The ENR was extracted using the Y-factor method. The Y-factor was determined as the ratio of the power measurement in the two states, P_{hot} corresponding to the ON state, when the diode is reverse biased near its avalanche regime and P_{cold} corresponding to the OFF state when the diode is un-biased.

Since we cannot directly extract the equivalent noise temperature due to the mismatched noise source, the effective hot noise temperature (delivered noise temperature) ($T_{HOT}^{B,e}$) is first determined in the wave guide plane B by (2.7) and the Y-factor measurement.

$$T_{HOT}^{B,e} = T_{RCV}.(Y-1) + Y\frac{T_{COLD}}{M} \tag{2.7}$$

Then, the available hot noise temperature ($T_{HOT}^{B,av}$) is determined by the use of the mismatch factor at plane B using (2.8).

$$T_{HOT}^{B,av} = T_{HOT}^{B,e}.M \tag{2.8}$$

Then, we should calculate the hot noise temperature at plane A (the output plane of the integrated noise source). Knowing the available gain of the probe (from the data sheet provided from the supplier), the hot noise temperature at plane A can be written as in (2.9).

$$T_{HOT}^{A,av} = \frac{T_{HOT}^{B,av} - T_A(1 - G_{probe}^{av})}{G_{probe}^{av}} \tag{2.9}$$

Where G_{probe}^{av} is the available gain of the probe defined by (2.10). The calculation

of the mismatch factor and the available gain are calculated using the S-parameters measurements of the probe, the reflection coefficient of the diode noise source ($\Gamma_{\mathrm{NS(i)}}$), which is measured for the various bias current conditions and the reflection coefficient of the noise receiver $\Gamma_{\mathrm{IN}}^{\mathrm{RCV}}$.

$$G_{\mathrm{probe}}^{\mathrm{av}} = \left|S_{21}^{\mathrm{probe}}\right|^2 . \frac{1 - \left|\Gamma_{\mathrm{NS(i)}}\right|^2}{\left|1 - S_{11}^{\mathrm{probe}}\Gamma_{\mathrm{NS(i)}}\right|^2 .(1 - \left|\Gamma_{\mathrm{OUT}}^{\mathrm{probe}}\right|^2)} \tag{2.10}$$

Finally, the available excess noise ratio in at plane A ($\mathrm{ENR_{A,av}}$) can be determined by (2.11).

$$ENR_{\mathrm{A,av}} = \frac{T_{\mathrm{HOT}}^{\mathrm{A,av}} - T_{\mathrm{COLD}}}{T_0} \tag{2.11}$$

The extracted $\mathrm{ENR_{A,av}}$ of the diode noise source, measured for several biasing current, versus frequency is shown in Fig. 2.20. The graph is plotted in the range 130-260 GHz to show the full continuity of the ENR value in a wide frequency range, where the ENR extracted in the frequency range 130-170 GHz was carried out using the same methodology with a different noise receiver structure [33]. We notice that the level of ENR varies according to the reversed biasing current of the diode source. The diode features a varying ENR value up to 20 dB. Note that the ENR value constantly decreases according to all bias currents. This ENR shape is related to the diode noise model. In Fig. 2.21 the measured ENR value is plotted versus the biasing current at specific frequency points. We notice that the ENR value will decrease as the current decreases. Thus using the noise source at low current levels will not generate the sufficient power to be used to characterize devices of the next stage, also making the output noise power not detectable [33, 34].

2.3 Integrated Noise Source ENR Extraction (260-325 GHz)

Now we tend to expand the frequency range and extract the ENR value of the integrated diode noise source up to 325 GHz, in order to study the performance of the noise source up to this frequency. To extract the ENR we followed the same methodology as in section (2.2),using the receiver structure dedicated to the required frequency band (2.1.2). The extracted ENR of a noise source of the same structure size and biased at 6 and 7 mA respectively in the frequency range (130-325 GHz) is shown in Fig. 2.22. We show the full frequency band so that we can have a clear image og the ENR curve behaviour on a wide frequency band range.

We notice that the noise source achieved an ENR value of 20 dB up to 170 GHz, and then the curve starts to decrease. The curve flattens out above 220 GHz and we

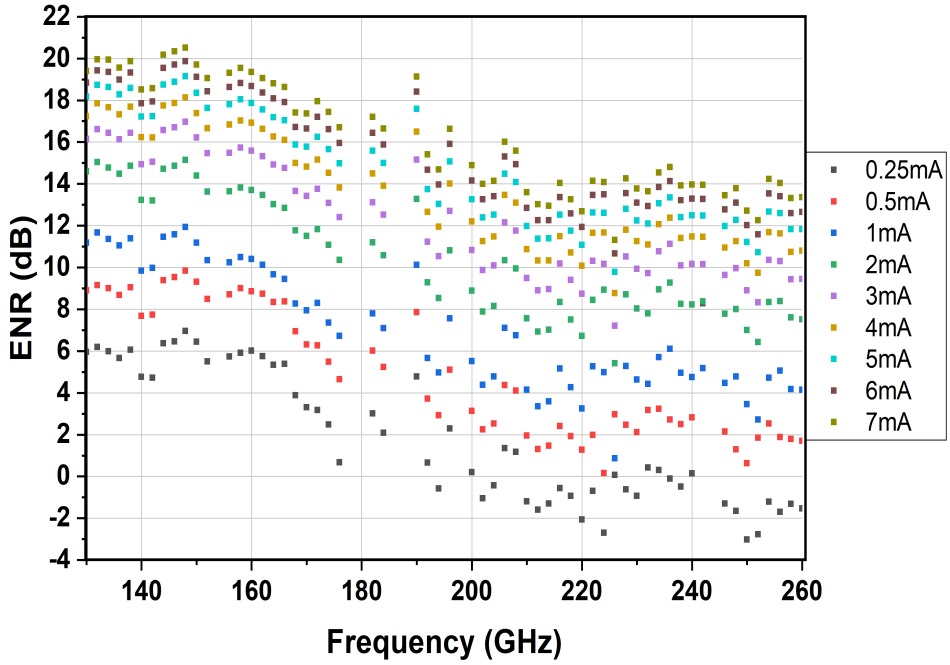


FIG. 2.20: Extracted ENR of the integrated noise source up to 260 GHz.

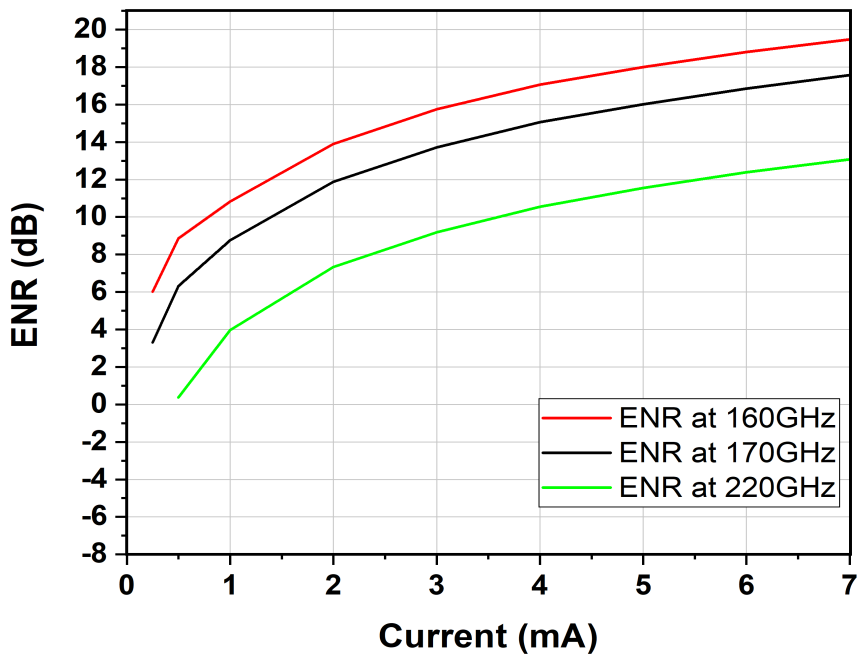


FIG. 2.21: Extracted ENR of the integrated noise source versus biasing currents for three frequency points.

can no longer notice the slope. To better understand the behaviour of this source, and to determine the physical response of the ENR curve versus frequency we need to better understand the model of the device [34].

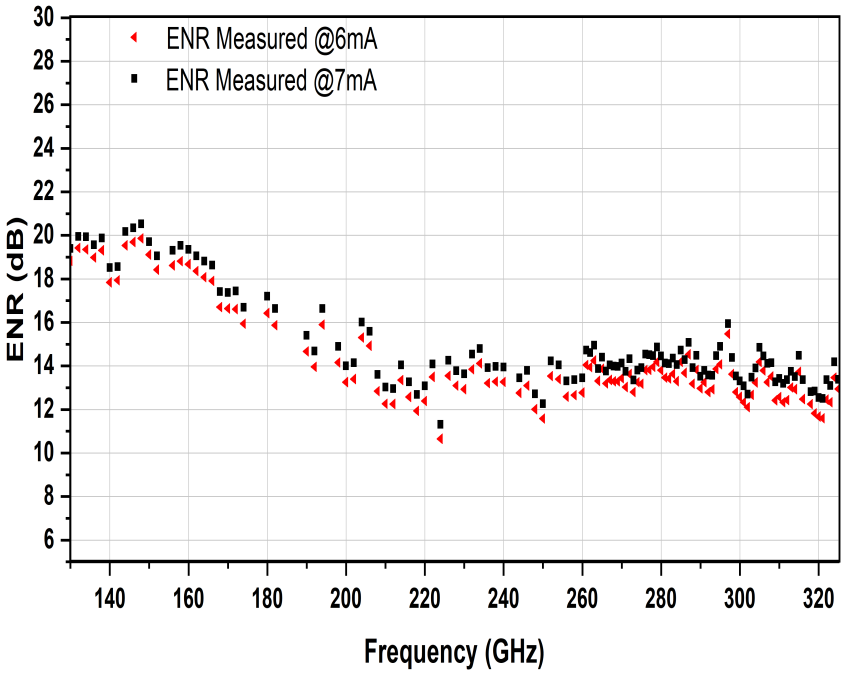


FIG. 2.22: Extracted ENR of the integrated noise source up to 325 GHz.

For the measurements of P_{hot} and P_{cold} used in the extraction of the ENR value described in the above sections (2.2 and 2.3), we used the developed matlab code as previous so that the measurements were automated.

2.4 Integrated Noise Source Electrical Model and ENR Study up to 325 GHz

Till now, the integrated diode noise source was characterized for its ENR value. Beyond this initial proof of concept of a silicon based noise source, the technological developments need deeper analysis and design guidelines to be conducted. In this context, the electrical model of this noise source was developed, and the ENR value was extracted from this model and used as a simulated value to be compared to the measurements, to support the results of the previous experiment performed in sections (2.2 and 2.3) and extract silicon process design guidelines towards the use of these devices in millimetre-wave noise generation.

Following the procedure in [40], the diode equivalent electrical circuit, including an intrinsic noise current-source associated with the avalanche zone i_a, is shown in Fig. 2.23.
In this electrical circuit, C_{sub} and R_{sub} are the capacitance and resistance of the substrate respectively. R_s is the contact resistance, C_p represents the parasitic capacitance. The intrinsic diode impedance is represented by Z_i , where R_j is the junction resistance and Z_d is the sum of the impedance of the drift region and that of the avalanche region, where the drift region can be expressed by a drift resistance R_d and a parallel capacitance C_d . In this model C_d is not included in the schematic due to the fact that its value is considered negligible compared to that of the intrinsic structure (extracted to be in the range of atto farad). The avalanche region Z_a is described by a resonant circuit C_a and L_a [42]. From S-parameters measurements of the device and by de-embedding the effect of the extrinsic part (open-short de-embedding [43]), we first extract the impedance of the internal structure Z_s . Where Z_s is expressed as in (2.12).

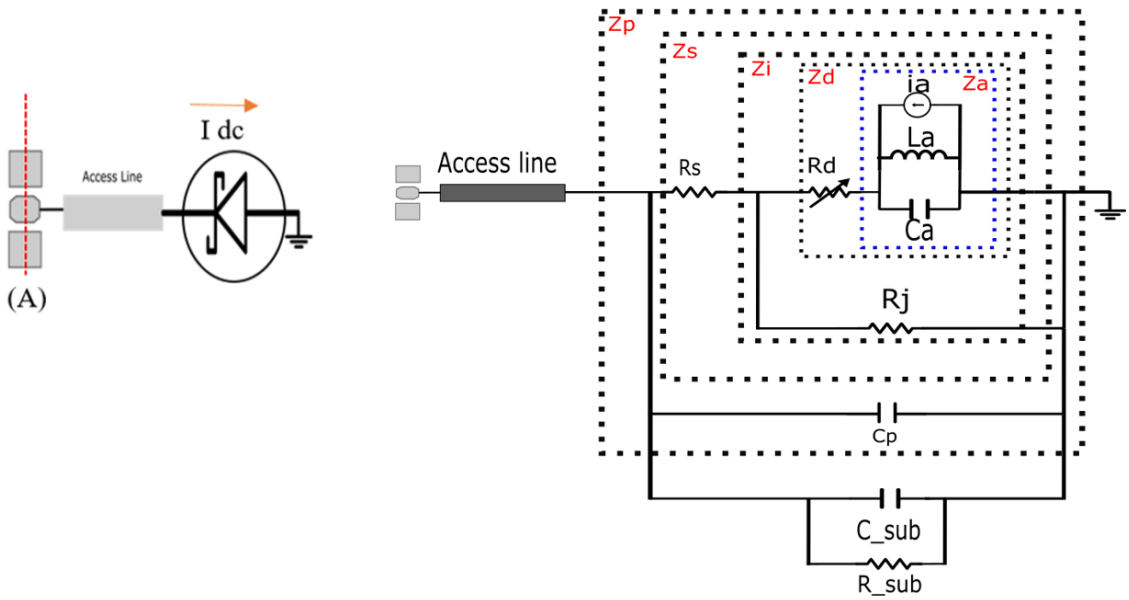


FIG. 2.23: Noise source electrical model.

$$Z_s = Z_i + R_s \tag{2.12}$$

R_s is bias independent and can be extracted from the slope of the I-V curve ($Slope_{\text{I-V}}$) when the diode is forward biased above the threshold voltage ($R_s = \frac{1}{Slope_{\text{I-V}}}$) . Then the intrinsic diode impedance Z_i can be extracted using (2.12). Knowing this value, we can relate it to the intrinsic parameters of the diode (2.13).

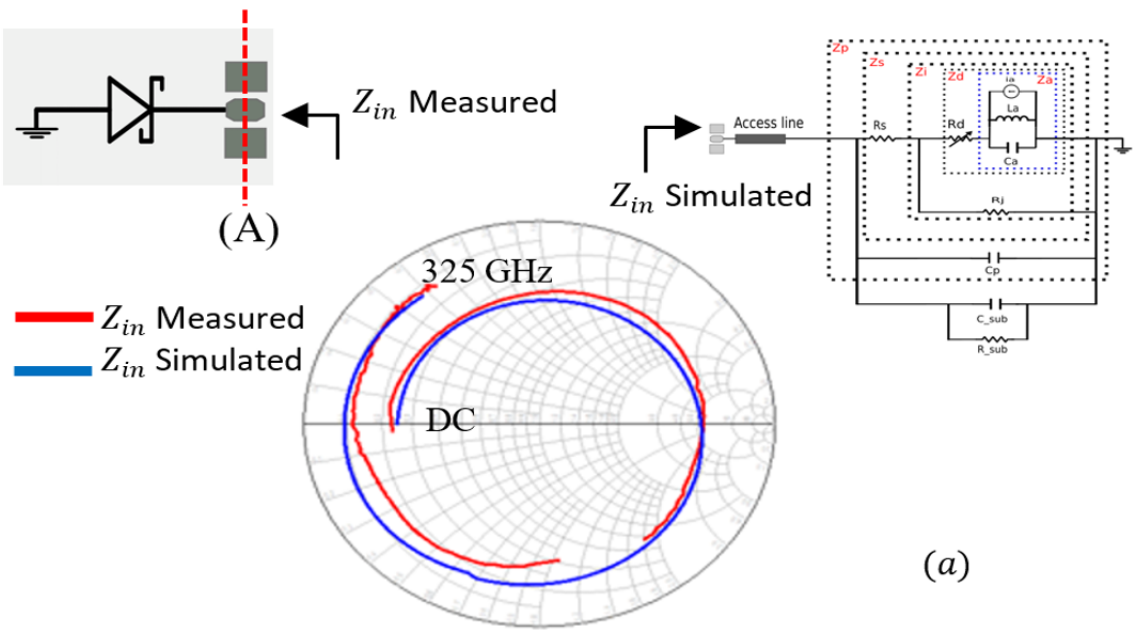
$$Z_i = (\frac{1}{R_j} + \frac{1}{Z_d})^{-1} \tag{2.13}$$

As stated, Z_d can be expressed as the sum of the drift zone resistance and the avalanche zone impedance (2.14).

$$Z_d = R_d + Z_a \tag{2.14}$$

Due to the LC circuit of the avalanche region, a resonance in the imaginary part of the Z_i curve at a frequency where ($\omega = \omega_a$) the angular frequency of the avalanche region is observed. At this resonance frequency $|\frac{1}{Z_d}|$ is assumed negligible, then R_j is calculated as the real part of Z_i. Whereas at lower frequencies $|\frac{1}{R_j}|$is considered negligible and the real part of Z_i is assumed to be that of the drift region R_d.Knowing the resonant frequency and the curve of the imaginary part of Z_i, we can extract the impedance of the avalanche region (C_a and L_a).

The diode electrical model was simulated using ADS Keysight © and the value of the model parameters are extracted (using the equations 2.12 to 2.14). This model will be studied for several structure sizes and biasing conditions of the noise source. To validate the extraction methodology, the input impedance of this simulated electrical model is compared to the impedance extracted from the S-parameters (S11 of the 1 port structure used as a noise source configuration), the results are shown (Fig. 2.24.a) in the range DC - 325 GHz. Between the frequency range 110-140 GHz we can measure the diode S11 parameter using the available measuring equipment in the lab, therefore we only show the simulated model. Note that in the high frequency range, we should take into account the capacitance and the resistance of the substrate. To show the importance of such parameters, (Fig. 2.24.b) shows the input impedance of the electrical model neglecting the capacitance and the resistance of the substrate, as we see the curve does not fit with the measurements.



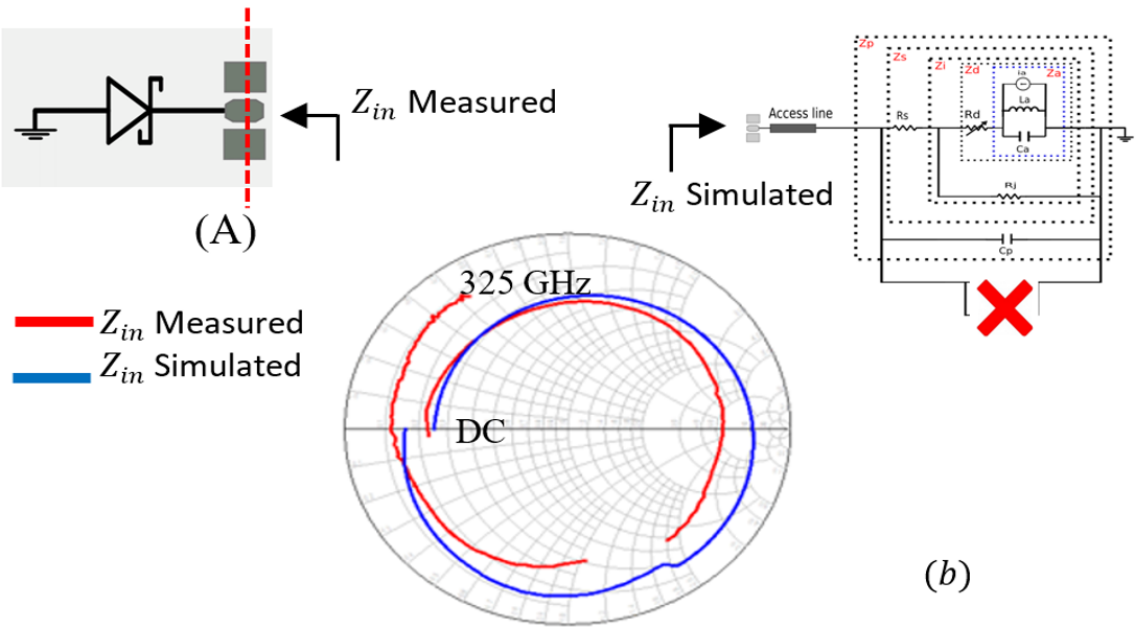


FIG. 2.24: Comparison between the input impedance of the noise source extracted from the measurements and that simulated from the electrical model.

The structure size used in Fig. 2.24 was 6.8 µm^2 , and it was biased at 7mA (reverse biasing).

Note that to cover the whole bandwidth, the S parameters were measured using several probes each associated to a certain bandwidth (DC-110 GHz, 140-220 GHz, 220-320 GHz), this can introduce a small shift on the curve of the measured impedance at the transition from one frequency band to another. Also, the difference in the real part of the impedance which is present between the model and the measured curve (Fig. 2.24.a), is due to some variations and uncertainties in the measurement files(such as the probe position or change in the calibration files) which lead to inaccurate model of the access line impedance and the pads over the total bandwidth (DC-325 GHz).

Fig. 2.25 presents the comparison between the internal diode structure Z_s extracted from S-parameters measurements after de-embedding (open-short to eliminate the effect of access lines and pads) and the one extracted from the model. The area of this sample is 3.4 µm^2 and the diode was biased at 6mA (we selected a different sample size to show the validity of the model for several structure sizes). A good agreement between the simulated and the extracted value of the impedance can be observed, which validated the electrical model and the extracting methodology of the parameters of the diode noise source up to 325 GHz.

The I-V curve showing the avalanche region of the diode structure of 3 different sizes is shown in Fig. 2.26.

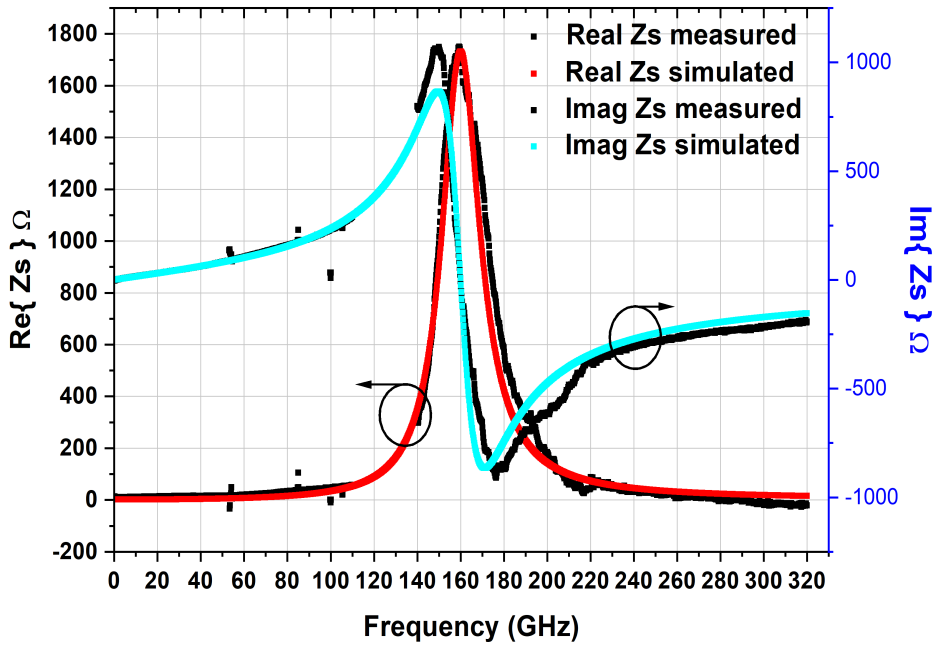


FIG. 2.25: Comparison between the internal diode structure Z_s extracted from S-parameters measurements and that extracted from the model.

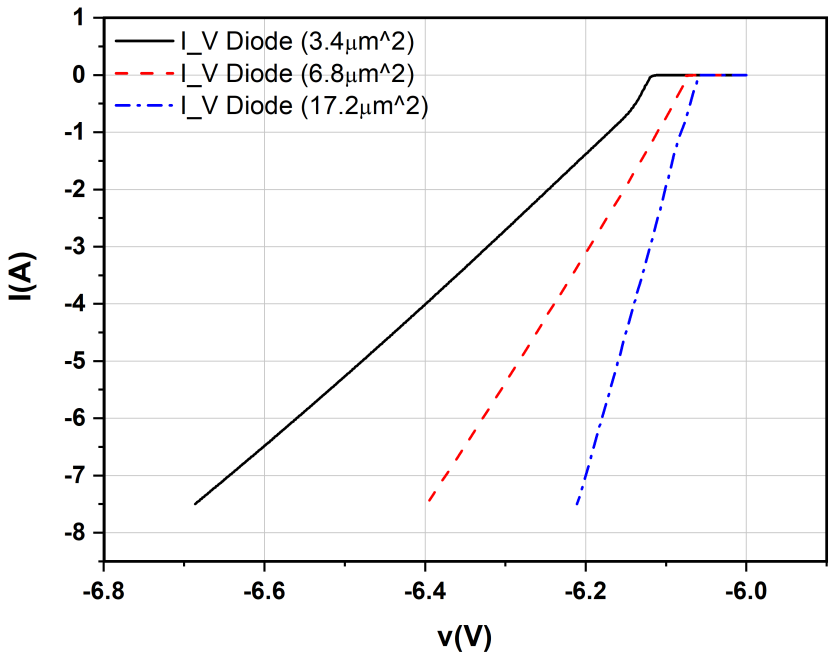


FIG. 2.26: I-V characteristics of 3 diode structures.

The model parameters can vary with the structure size, for example the avalanche capacitance C_a.

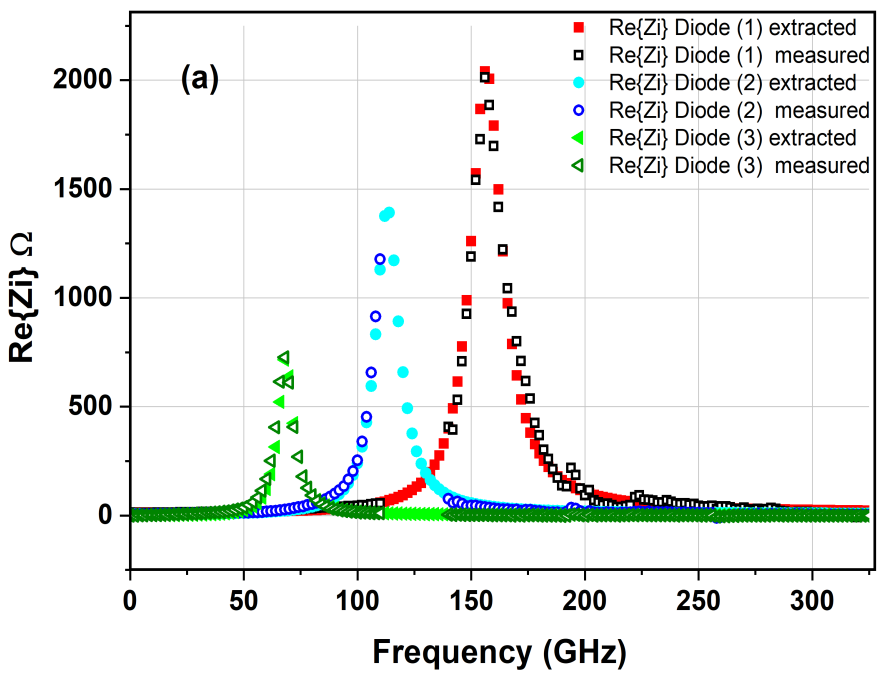
$$C_a = \frac{\epsilon A}{l_a} \tag{2.15}$$

Where A is the effective area of the structure, l_a is the length of the avalanche region, (ϵ) is the permittivity of the material. Also the case for the avalanche inductance L_a, as it will vary inversely with the DC biasing current, which in turn will affect the resonant frequency of the diode.

$$L_a = \frac{\tau_a}{2I_0\bar{\alpha}'} \tag{2.16}$$

τ_a is the transit time and $(\bar{\alpha}')$ is the derivative of the average ionization coefficient with respect to the electric field [42].

Fig. 2.27.a and Fig. 2.27.b show the real and imaginary part of the intrinsic impedance Z_i for three different sizes of the diode noise source, while fixing the biasing current at 6mA. Diode 1 with the smallest area (3.4 µm^2), diode 2 of area (6.8 µm^2) and diode 3 of area (17.2 µm^2).
A good agreement is noticed between the measurements and the simulation of the intrinsic impedance. As can be seen, a smaller diode area will result in a higher resonant frequency as expected, so the size of the diode structure is an important parameter to consider when choosing the noise source for mmW and sub-terahertz applications.



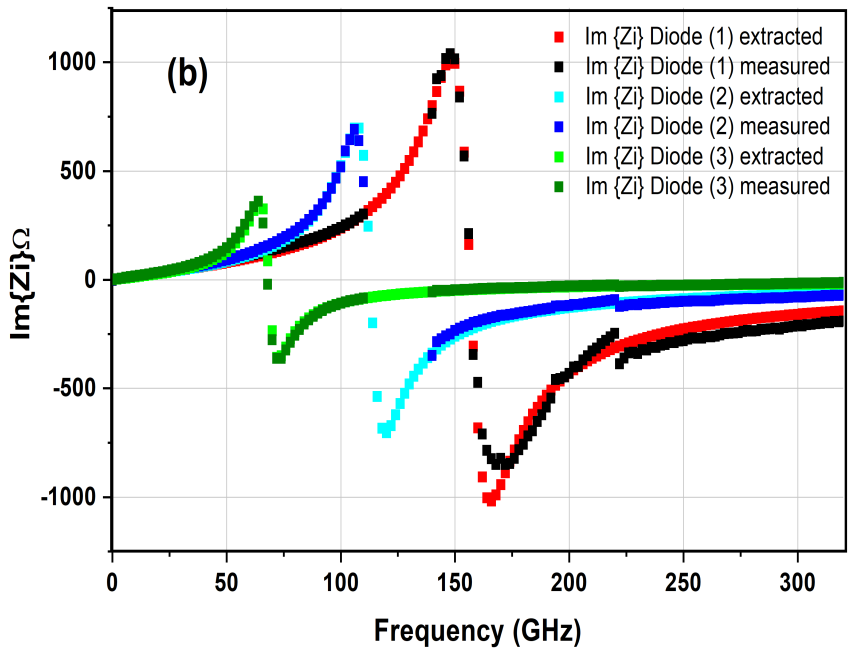


FIG. 2.27: Real and imaginary part of the intrinsic impedance Z_i for three different sizes of the diode noise source, while fixing the biasing current at 6mA.

Also (Fig. 2.28) shows the imaginary part of the impedance Z_i of a diode structure of a fixed area 6.8 µm^2 biased with several biasing currents. As we notice, decreasing the biasing current also decreases the resonance frequency, since the avalanche current density will decrease referring to 2.17 in the next section, also the change in the resonant frequency is related to the value of the avalanche inductance as seen in 2.16. Tables 2.1 and Tables 2.2 summarizes the variation in the noise source parameters for different sizes and biasing currents [34].

2.5 Extraction of ENR From The Noise Source Electric Model

In the following study, we propose to use the developed model to extract the ENR of the noise source towards design guidelines for technological developments. We consider that the avalanche noise current is dominant over thermal noise sources, and is the only source of noise in the structure (the flicker noise (1/f noise) is neglected at high frequencies since it decreases with frequency; also usually, it is more dominant in the forward biasing conditions [44–46]. It is therefore important to calculate the avalanche current spectral density [42, 47]. Relation (2.17) is usually used to describe the avalanche current spectral density, we consider that this relation holds for

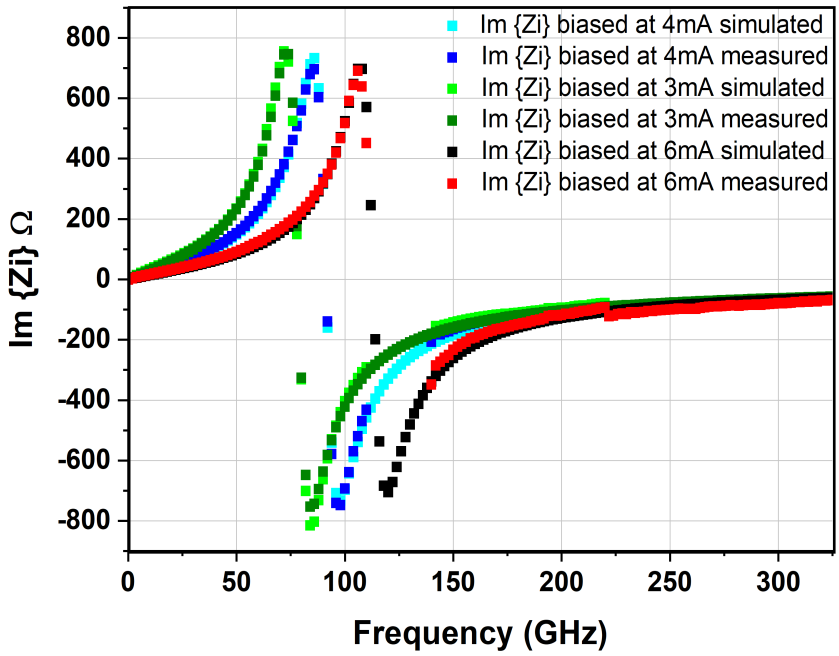


FIG. 2.28: I-V characteristics of 3 diode structures.

the structure represented in this study (the Schottky diode structure).

$$\langle i_{\mathrm{a}}^2 \rangle = \frac{2qI_0\Delta f}{\omega^2\tau_{\mathrm{x}}^2} \tag{2.17}$$

Where q is the electron charge, I_0 is the DC bias current and τ_x is the average time between two ionizations. Note that the value τ_x is considered as a fitting factor and has been adjusted accordingly.

Using the model (Fig. 2.23), we can relate $\langle i_{\mathrm{a}}^2 \rangle$ to the total noise current density.

$$\langle i_{\mathrm{t}}^2 \rangle = \langle i_{\mathrm{a}}^2 \rangle . \left| \frac{Z_a}{Z_d} \frac{Z_i}{Z_s} \frac{Z_p}{Z_{\text{access line}}} \right|^2 \tag{2.18}$$

Then the noise temperature of the diode while in ON state can be calculated as in (2.19).

$$T_h = \frac{\langle i_{\mathrm{t}}^2 \rangle}{4kR_e(Y_d)\Delta f} \tag{2.19}$$

Y_d is the measured admittance of the diode and k is the Boltzmann constant.

TABLE 2.1: Electrical Model Parameters (Reverse Biased at 7 mA) For Several Diode Sizes.

Parameter	Diode 1	Diode 2	Diode 3
Size (μm^2)	3.4	6.8	17.2
L_a (nH)	0.196	0.19	0.17
C_a (fF)	4.5	9	27
C_{sub} (fF)	8	12	20
R_{sub} (Ω)	1000	1000	2000
R_s (Ω)	12.3	6.3	5
R_j (Ω)	1920	1400	697
R_d (Ω)	13	6.3	2
τ_x (ps)	1.1	0.7	0.7

TABLE 2.2: Electrical Model Parameters (Current Dependant) For Several Currents.

Current (In reverse)	7mA	6mA	3mA
L_a (nH)	0.196	0.229	0.456
R_j (Ω)	1920	2053	2230

The ENR value can thus be deduced as follows:

$$ENR = \frac{T_h - T_0}{T_0} \tag{2.20}$$

T_0 being the standard noise temperature (290 K), close to the room temperature.
To verify this assumption (to use 2.17 for a schottky junction) we follow the procedure explaned in [32], where we proceed in three steps:
First, we used the relation in (2.17) to describe the current spectral density $\langle i_a^2 \rangle$. Then this equation is used to calculate the ENR value extracted from the model (2.17 to 2.20).
Following this calculation, the extracted ENR value from the model is compared to the ENR measured (2.30, 2.31) using the test bench represented in Fig. 2.17.
We then use the measured hot noise temperature value (T_{hot} extracted from the measured ENR value), and follow the procedure used in [32] to recalculate the value of the current spectral density $\langle i_a^2 \rangle$. The procedure is shown in the following equation.

$$T_{\text{hot,meas}} = \frac{|h_{21}|^2}{4.K.\left|Y_{\text{eq}}\right|^2}.\langle i_a^2 \rangle \tag{2.21}$$

Where $T_{\text{hot,meas}}$ is the hot noise temperature taken from the measured ENR value, Y_{eq} is the equivalent admittance of the structure and h_{21} is the short-circuit current

gain expressed as $\frac{y_{21}}{y_{11}}$.
Fig. 2.29 shows the comparison between the value extracted using the measured parameters and that calculated using (2.17). The extracted values stand within the same range for this diode structure (of size 3.4 μm^2 , biased at 6mA) over a 40 GHz frequency band. As a result (2.17) was justified to be used.

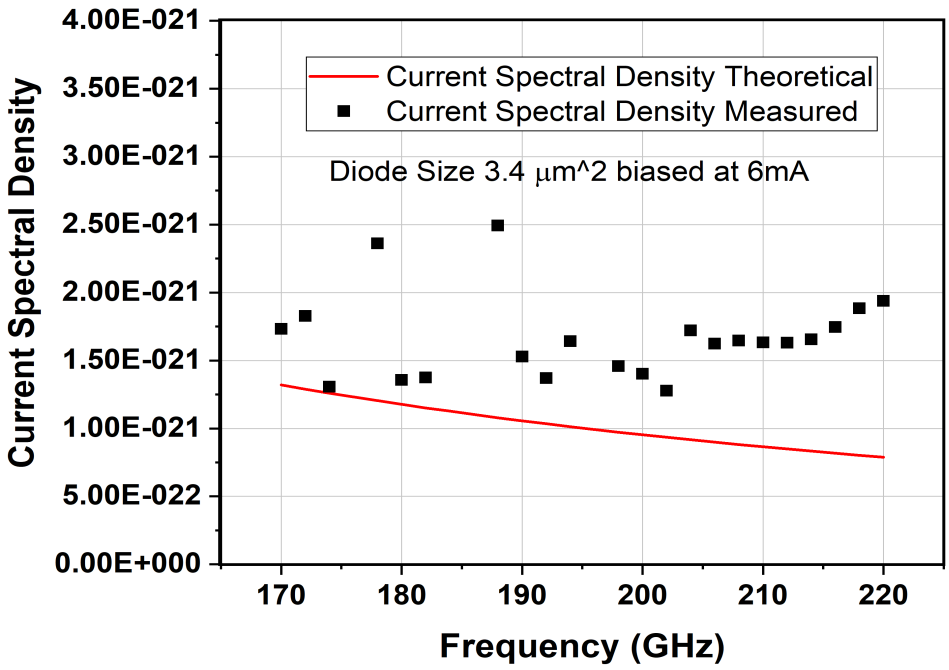


FIG. 2.29: Theoretical current spectral density calculated using (2.17) in comparison with that extracted from measured values.

Fig. 2.30 and Fig. 2.31 show the ENR value extracted from the model (2.17 to 2.20) in comparison with the ENR value extracted by the measurements done up to 220 GHz (Fig. 2.20). In Fig. 2.30, and for the clarity of the presented graph, one sample of the measured ENR curve is plotted, where the diode structure was biased at 7 mA and the structure size is 3.4 μm^2.

We should note that some points are not available for the curve of measured data (red curve), due to limitations of the noise receiver at these frequency points.

From (2.17 and 2.18), we notice that the change in the diode impedance or current density will affect the value of the ENR produced, which explains the variation of the ENR curve with the biasing current presented in Fig. 2.20. This is also validated in Fig. 2.31, where the extracted ENR value from the electrical model of a single size diode structure (3.4 μm^2) biased at two different D.C. currents is plotted. Also, the extracted ENR value is compared to the measured value in the frequency range up to 220 GHz.

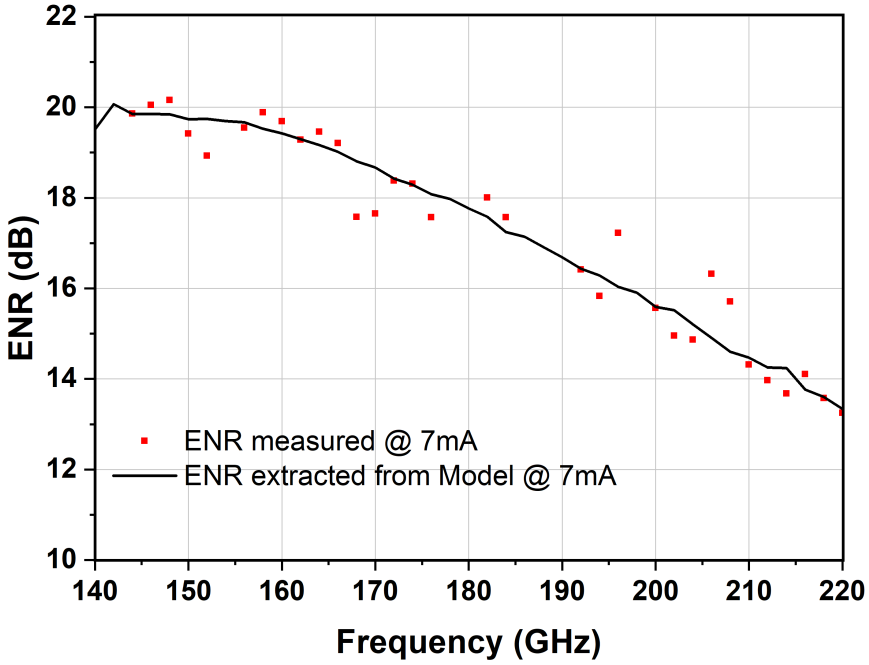


FIG. 2.30: Simulated and measured ENR curve of the diode of size 3.44 µm^2 biased at 7mA.

In all the ENR extractions the value of τ_x is considered a fitting factor and is adjusted accordantly (τ_x value varies between 0.7 and 1.02 ps, with an average value taken around 1 ps). As the biasing current increases the ENR level increases as well. We chose to go up to a maximum of 7mA biasing current to be coherent to the experiment done in 2.2, and to have a valid comparison between the measured value and the model.
TABLE 2.3 shows the maximum biasing current possible for each diode size. This maximum value of the biasing current has been noted by measuring several diode structures, where the DC biasing current was increased slowly until the diode sample is burned.

TABLE 2.3: Maximum Current/Current Densities VS Diode Size.

Size (µm^2)	3.4	6.8	17.2
Current (mA)	14	25	50
Current Density(mA/µm^2)	4.06	3.63	2.9

In our study, the ENR value of the noise source is calculated at the input plane of the on-wafer diode structure (Fig. 2.17). Here we should mention that the extrinsic part (the combined effect of the pad impedance, the access lines and the parasitic impedances) have an effect on the slope of the ENR curve. That being said, we can

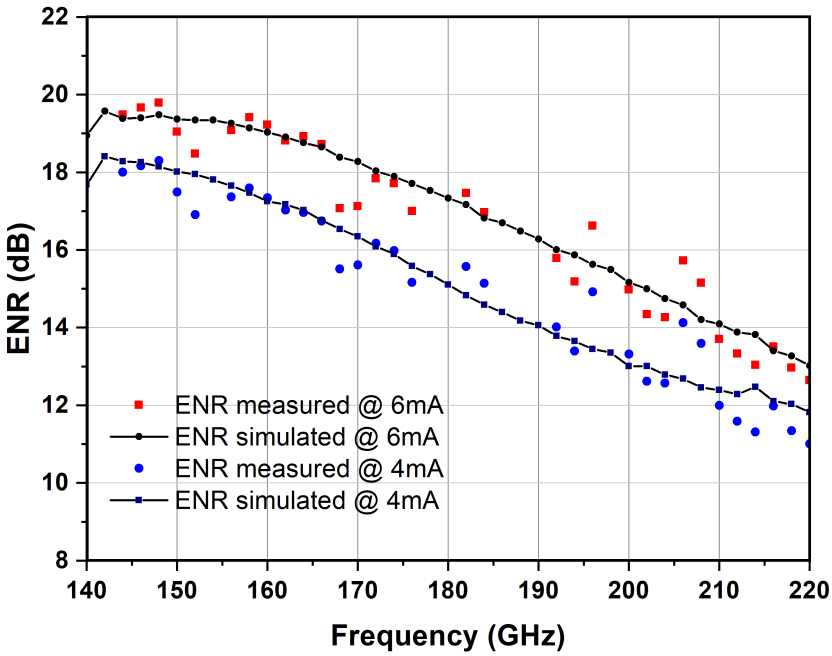


FIG. 2.31: Simulated and measured ENR curve of the diode of size 3.44 µm^2 biased at 4 and 6mA.

notice that in (2.18) the dominant factor is $\left(\left|\frac{Z_a}{Z_d}\frac{Z_i}{Z_s}\frac{Z_p}{Z_{\text{access line}}}\right|^2\right)$.
So, the noise temperature is affected by the admittances of the extrinsic part of the structure ($\frac{1}{Y_d}$) and the factor presented in (2.18) (Fig. 2.17). The inverse of the real part of the intrinsic admittance (Y_i) for 2 diodes of different sizes is shown in Fig. 2.32 and compared to the inverse of the real part of the admittance measured at the input plane of the wafer.

Looking on the surface effect for a constant biasing current on the ENR curve, Fig. 2.33 shows the effect of using several sizes of the noise source structure, where the ENR curve was measured at the input plane of the wafer (Fig. 2.17) for 3 different diode sizes all biased at 7 mA.

This study can give us an insight of the noise source performance, as well as the size and current parameters that will affect the ENR level, especially when we consider the use of the diode as a noise source integrated with a silicon device at wafer-level [34].

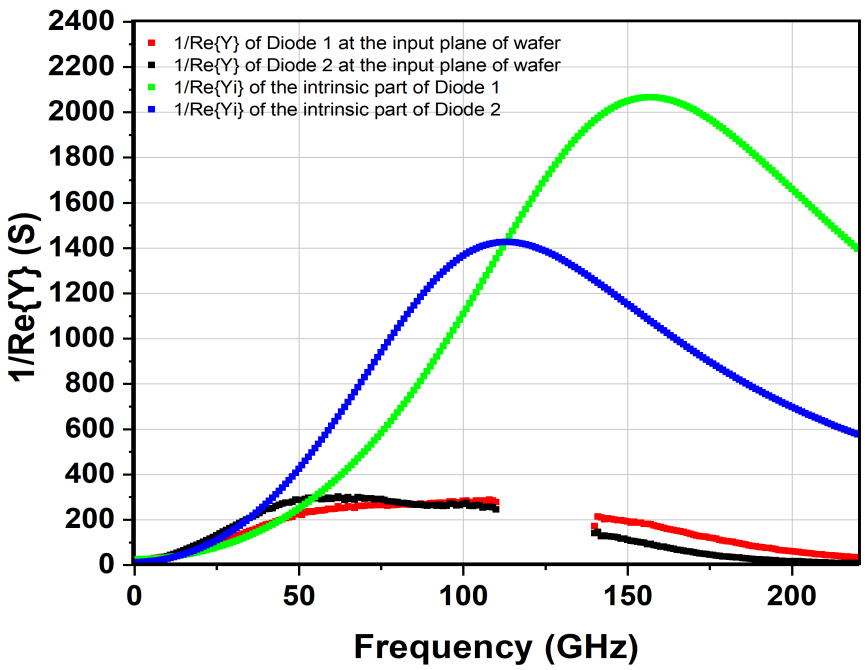


FIG. 2.32: Inverse of the real part of the intrinsic admittance for 2 diodes measured at the input plane of the wafer and at the intrinsic part of the structure.

2.6 Extension Of The Noise Measurements Up To 325 GHz

In section 2.3, the ENR value was measured up to 325 GHz and the ENR curve continued with a flat slope after 220 GHz (Fig. 2.22). The ENR value extracted from the model showed a very good agreement with the measured value up to 220 GHz (Fig. 2.30 and 2.31). Thus we can now extrapolate the diode impedances, parameters, and ENR value for higher frequencies (up to 325 GHz). Here we should note that smaller size diodes will handle lower biasing current levels, at which lower ENR levels are produced. This induces a usual trade-off between the diode size used and the ENR value achieved.

Due to the model response of the noise source (2.17), the ENR value should follow a decreasing slope as frequency increases.Therefore further study was done on the ENR measurements at frequencies above 220 GHz, and we noticed that at higher frequencies, the output power produced by the source is below the MDS level of the noise receiver (1.5.3), moreover the value of the Y-factor decreases (the difference between P_{hot} and P_{cold}) as frequency increases to approach unity at high frequencies (near 325 GHz). This leads to inaccurate power measurements and thus a false representation of the measured ENR value.To overcome this issue and better detect the output power of the noise source a modified setup is proposed and assembled (Fig. 2.34).

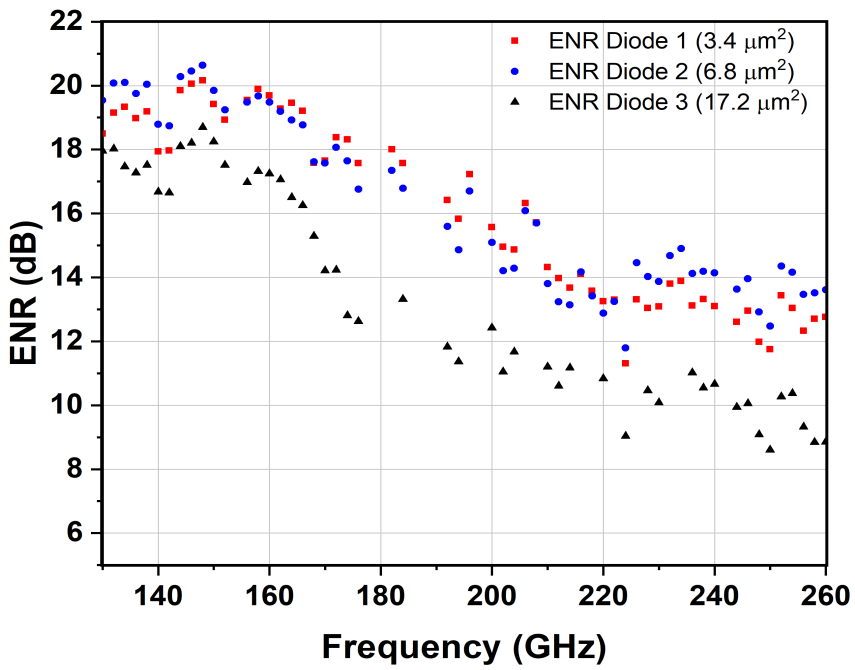


FIG. 2.33: ENR curve measured at the input plane of the wafer of 3 different diode sizes biased at 7mA.

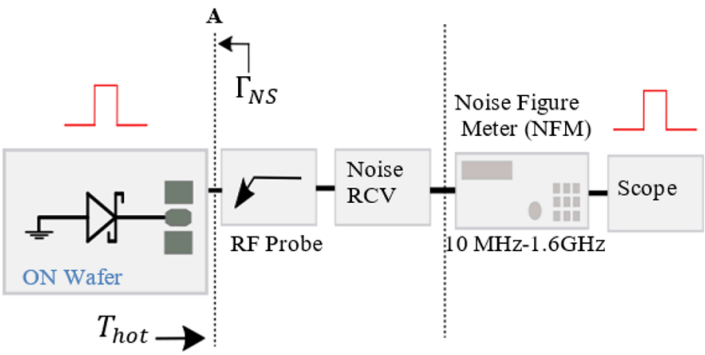


FIG. 2.34: Pulsed noise measurement setup to extract low ENR levels up to 325 GHz.

In the previous set-up, the biasing of the diode with a DC current and the powers P_{hot} and P_{cold} are measured in continuous wave (CW) corresponding to the ON and OFF states of the diode. In NFM instruments, the power level is usually measured using a diode rectifier after a mixer. When measuring the ON and OFF states, the diode output is a D.C. voltage and thus difficult to average to reduce the noise floor. In order to further increase the sensitivity, the noise source was biased with a pulsed CW current source to produce a pulsed signal at NFM diode output, with an amplitude linearly dependent to the incoming power (ON or OFF states).Then, the peak

to peak voltage at the diode output (NFM detector) was measured in time domain using an oscilloscope (corresponding to the input pulsed current signal), with an averaging enabling to reduce the temporal noise while keeping peak to peak voltage. The detected output peak-to-peak voltage has the same shape (slope) of the expected ENR curve extracted from the model.

To validate the measurement method, we applied this technique to re-measure the ENR curve shapes at lower frequencies, around 200 GHz. Both methods lead to the same results (the same slope of the measured curve was obtained using the CW biasing and the pulsed CW biasing) and knowing the absolute noise power at 200 GHz (frequency for which the slope is correct, see Fig. 2.35), we were able to extract the corrected ENR curves beyond the MDS limitation.

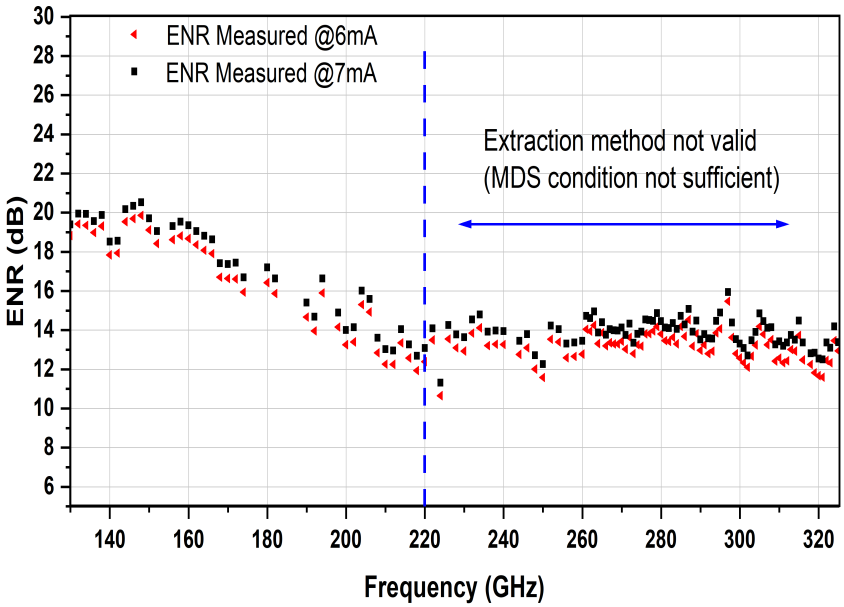


FIG. 2.35: Measured ENR value of the noise source in the frequency range 130-325 GHz. Above 220 GHz the extraction method is not valid since the MDS conditions are not sufficient.

Fig. 2.36 shows the measurements of ENR curve of the diode noise source (area=6.8 µm^2) with a biasing current of 7 mA, compared to the ENR extracted from the model extended up to 325 GHz. A good fitting is noticed through all the measured frequency range. Using this new method (Pulsed biasing) we can overcome the measurement limitations, moreover we can now measure low noise power levels. This bench set-up is available now at IEMN and used to perform noise measurements up to this frequency range. We should also note that instead of the NFM we can use a diode detector to sense the output voltage levels (we only used the diode detector inside the NFM to detect the voltage pulses)[34].

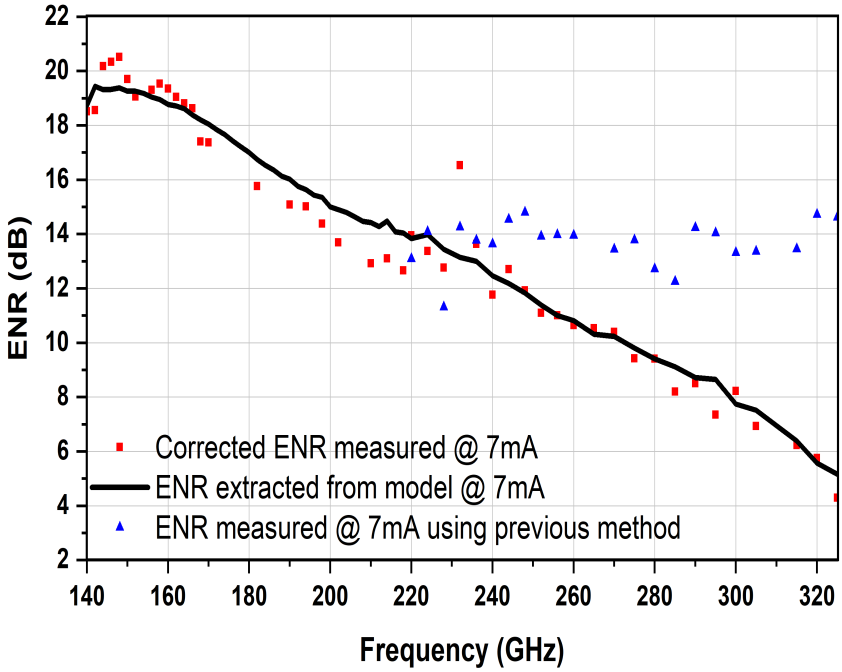


FIG. 2.36: Measured ENR value of the noise source (area=6.8 µm^2) at 7 mA in the frequency range 130-325 GHz using the pulsed setup, compared to the ENR extracted from the model. In blue is the ENR curve extracted using the previous method (CW bias).

2.7 NF Extraction Of Active Devices Using Integrated Noise Source

We presented an integrated noise source based on a Schottky diode structure. This source have been characterized up to 325 GHz frequency range using an assembled noise receiver. In order to validate the use of the developed noise test bench (noise receiver and the integrated source above), a packaged amplifier was chosen to perform the noise characterization in the frequency range 220 GHz to 260 GHz. Fig. 2.37 shows the set-up used in order to perform the noise characterization of the packaged amplifier.

For waveguide noise characterization, the amplifier is placed between the RF probe waveguide flange and the input of the noise RCV. Based on the block diagram set-up presented in 2.37, the noise source has been used in waveguide flange at plan B, through the RF probe. The diode is contacted by the RF probe and reverse-biased through the bias tee of the RF probe in its avalanche regime. The assembled experiment is presented in Fig. 2.38.
The amplifier stand alone has a poor matching, so the amplifier is connected with variable attenuators at the input and output planes, to improve the matching to the other stages, even if that will increase the total noise figure of the device (Fig. 2.38) [33] .

The attenuation value was chosen by varying the position of the knob of the attenuator. Several configurations could be set regarding the attenuator values at the input and output of the amplifier. 2.4 shows the attenuation value for each configuration. Knowing the available hot noise temperature on plane B extracted earlier (2.9),

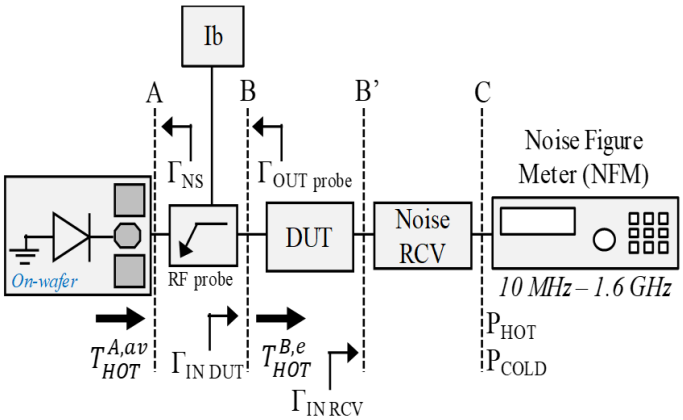


FIG. 2.37: Block diagram set-up to perform noise characterization of a packaged amplifier up to 260 GHz.

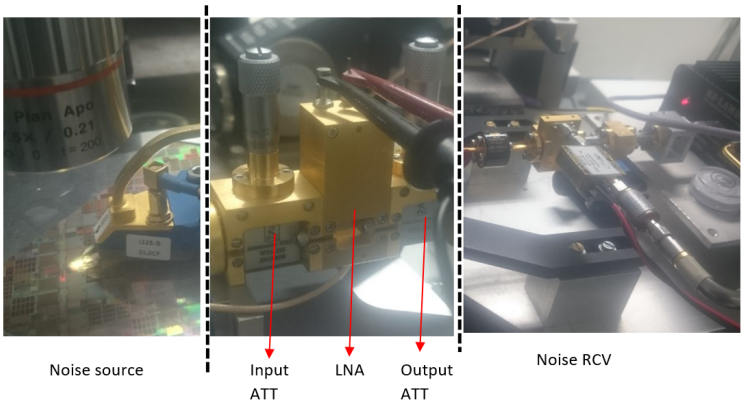


FIG. 2.38: Test bench set-up to perform noise characterization of a packaged amplifier up to 260 GHz.

the equivalent noise temperature between plane B and C could be extracted using the Y-factor method. Using the same methodology as (2.1 to 2.4), the noise temperature T_{tot} and the noise figure F_{tot} were then extracted. Then, the extraction of the noise factor of the packaged amplifier was deducted using FRIIS formula (2.22). The gain of the amplifier was extracted by performing off wafer power measurements.

$$F_{\text{Amplifier}} = F_{\text{tot}} - \frac{F_{\text{RCV}} - 1}{G_{\text{Amplifier}}} \tag{2.22}$$

TABLE 2.4: Attenuation Value At The Input and Output Ports Of The Packaged Amplifier.

Configuration	Input attenuator value (dB)	Output Attenuator value (dB)
1	7.9	9.5
2	0.8	9.5
3	0.8	0.5

The measurements and extractions were performed for variable bias current condition of the diode noise source, between 0.25 mA and 7 mA, as shown in Fig. 2.39. For biasing currents below 2 mA the extracted noise figure shifts from the extracted values done between 2 mA and 7 mA, this is due to the insufficient noise power supplied by the noise source to the amplifier. This can be seen in Fig. 2.20 where the ENR value for low biasing currents is very small in this frequency range, and it is further attenuated after the probe.

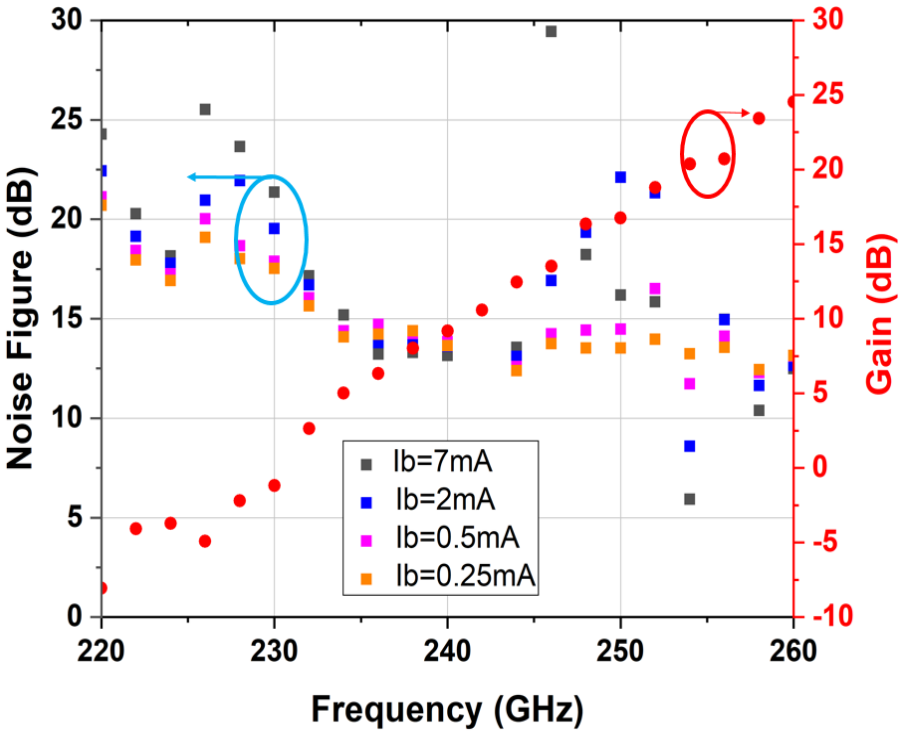


FIG. 2.39: Extracted noise figure of packaged amplifier using assembled test bench.

The extracted gain (deduced from noise measurements shown in Fig. 2.39) is close to the measured S21 parameter, for the configuration 3.

2.8 Conclusion

In this chapter we illustrated the concept of noise measurements in millimetre wave and sub-terahertz frequency range. We indicated the assembly of noise measurements test bench set-up. The set-up consists of an integrated noise source, a noise receiver and an active device (packaged amplifier) was connected in between and the noise figure was extracted.

The noise source is a Schottky diode fabricated on silicon substrate using BiCMOS 55 nm technology from STMicroelectronics. The noise source was characterized in the frequency range 130-325 GHz where the ENR value was extracted using the assembled noise receiver. Moreover the small signal electrical model of this noise source was developed and validated with the measurements (Impedance and ENR value) in the frequency range 130-325 GHz . A very good agreement was established which validated the extraction methodology.

The noise receiver consists of a down converter (mixer) used to transfer the RF noise signal from the source to a base band signal to be fed into the NFM where the noise power is measured. Two receiver structures where used to cover the full frequency band. The receiver noise figure was extracted using Hot/Cold measurements. Then the structure is used to perform noise measurements (ENR extraction of the noise source and NF extraction of active device) up to 325 GHz. Moreover using the pulsed extraction method we can now detect low power levels making it possible to overcome the MDS receiver limitations.

Finally to validate the set-up,we connect an active device (Packaged amplifier) between the noise source and the noise receiver and the noise figure is extracted.
This set-up is now available at IEMN and we can perform noise measurements over a wide band up to 325 GHz. The results are very promising, since we now have a noise source working at frequencies beyond 220 GHz so it is possible to perform noise measurements up to sub terahertz frequencies (overcoming commercial noise sources frequency limitations), and it is integrated on silicon so it can be placed on chip next to other devices. This decrease the connection losses between the source and the device under test which provide more accurate results. Furthermore, using the assembled receiver we can perform the noise measurements of devices over a wide band up to 325 GHz, which is not trivial using available commercial equipment.

Chapter 3

Noise and Power Measurements of Active Devices in the mmW and Sub-Terahertz Frequency Range

3.1 Optical Source For Noise and Power Measurements

Terahertz defines electromagnetic waves and radiation which lies between 0.1 THz (λ = 3 mm) and 10 THz (λ = 30 μm). Several applications in the field of radio astronomy, high-resolution spectroscopy and remote sensing areas use terahertz technology [48–50], due to the fact that this range of frequencies accommodates unique physical phenomena with interesting characteristic features. Terahertz wavelengths are longer than infrared and optical radiation, so scattering is comparatively small. Moreover, the terahertz wavelength is sufficiently short to achieve a sub-millimetre lateral resolution [51]. Terahertz imaging sensors for example bridge the gap between microwave radar and infra-red camera [52].

Despite the exceptional potential, the THz region is commonly known as the THz-gap due to the lack of tunable, high power and room temperature sources and detectors. A way to generate THz signals is by using a photodiode (PD) where it plays the role of converting the optical signal generated using lasers, into an electrical signal. In particular a unitraveling-carrier photodiode (UTC-PD) is a type of photo-diodes that uses only electrons as the active carriers [53]. The active part of the UTC-PD consists of a p-type doped InGaAs light absorption layer and an undoped (or a lightly n-type doped) InP carrier-collection layer Fig. 3.1.a. In the UTC-PD, the photo-generated minority electrons in the neutral absorption layer diffuse into the depleted collection layer and then drift to the cathode layer. On the other hand, because the absorption layer is P-doped, photo-generated majority holes respond very fast within the dielectric relaxation time by their collective motion. Therefore, the photoresponse of a UTC-PD is determined only by the electron transport. This is an essential difference from the conventional pin-PD (Fig. 3.1.b), in which both electrons and holes contribute to the device response and the low-velocity hole-transport

determines the total performance.

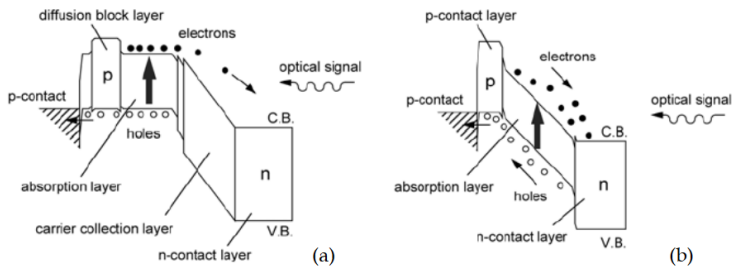


FIG. 3.1: Band diagram of a UTC-PD (a) and a pin-PD (b).[54]

In this section we will focus on the use of a uni-traveling-carrier photodiode (UTC-PD) in the mounted test bench to perform measurements on active devices in the millimeter wave and sub-terahertz frequency range. The UTC-PD will be used as a noise source in one configuration to perform noise measurements of the device under test (DUT), and also as a source to perform power measurements of the DUT, when connected in a different configuration [53].

3.2 Noise Measurements Using UTC-PD As Noise Source

3.2.1 ENR Extraction Of A UTC-PD

UTC-PDs are usually used as noise sources to carry out reliable characterizations in the millimeter wave (mmW) and sub-terahertz frequency range [29]. Unlike the silicon based noise source , the noise signal is generated by converted an optical based noise signal to an electrical domain using the UTC-PD. The optical noise signal determines the power level and shape of the generated noise, thus by simply controlling the optical noise,we can control and predict the power level, occupied frequency band, and the spectral density of the generated noise (Fig. 3.2) [30]. Using it as a

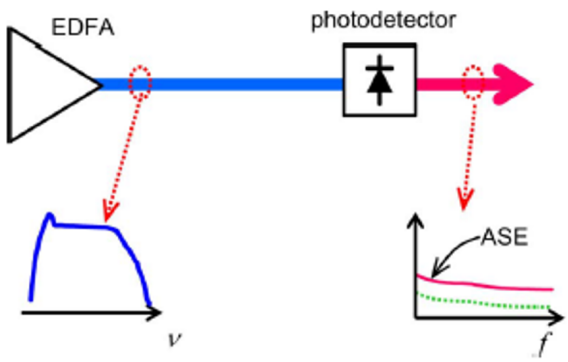


FIG. 3.2: Bench setup to extract the ENR of the UTC-PD.[54]

noise source, the UTC-PD should first be characterized for its ENR value, which is the noise level above the thermal noise floor. The set-up for the ENR extraction of the photodiode is shown in Fig. 3.3. The UTC-PD (provided from NTT electronics,

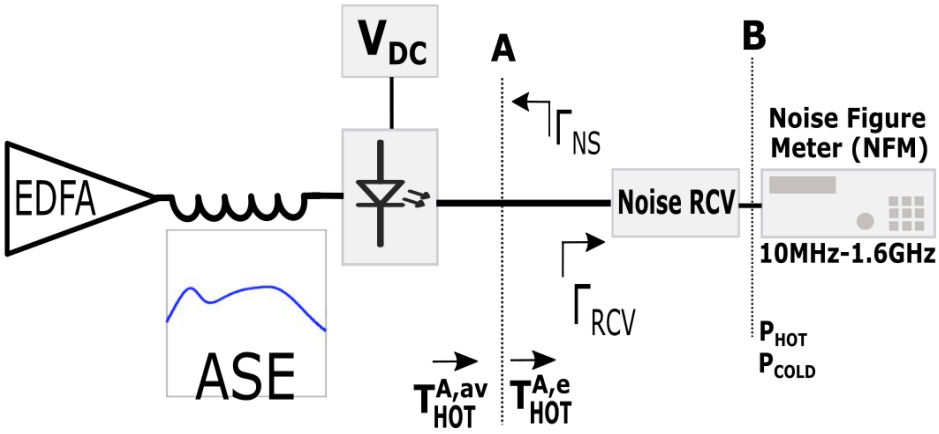


FIG. 3.3: Bench setup to extract the ENR of the UTC-PD.[54]

IOD-PMJ-13001) has a waveguide output port flung WR3.4 and is connected directly to the input of the noise receiver. It is biased with a D.C. source providing 1V, and at the input it is connected via a fibre to an Er-doped fibre amplifier (EDFA). The origin of the optical noise is the amplified spontaneous emission (ASE) noise from the (EDFA). The noise power is determined by the responsivity of the PD (0.2 A/W) and intensity of the input optical noise. To control the generated noise level we use an optical attenuator to control the optical power level [55].

The ENR values produced by this noise source (UTC-PD) for different current levels (varying the input optical power) have been extracted. Fig. 3.4 shows the mounted test bench for the ENR extraction of the UTC PD in the frequency range 260-325 GHz. As in the case of the integrated diode noise source, the Y method is used to extract the ENR of the UTC-PD using the same noise receiver mounted in section 2.1.2.

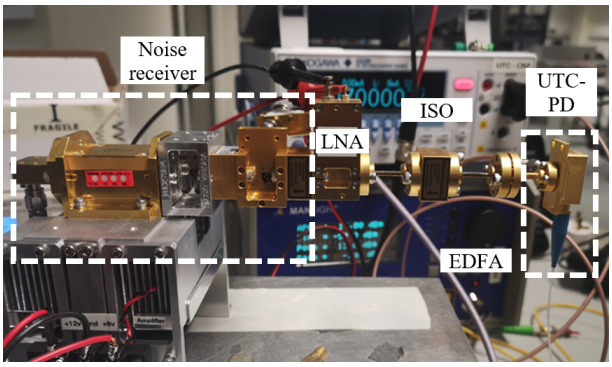


FIG. 3.4: Measurement setup for the UTC-PD ENR measurement.

Knowing the noise figure of the receiver (F_{RCV}) from section 2.1.2 (Fig. 2.13) we can relate it to the equivalent noise temperature at the input of the receiver 3.1.

$$T_{RCV} = \frac{F_{RCV} - 1}{T_0} \tag{3.1}$$

In order to account for the mismatch between the output flange of the UTC-PD and the input of the receiver, we will introduce a mismatch factor between the two stages, which will be used to correct for this mismatch (3.2). Γ_{RCV} (the receiver input reflection coefficient) and Γ_{NS} (the noise source output reflection coefficient) in Fig. 3.3 can be calculated from the S-parameter measurements of the isolator (first stage of the noise receiver) and the noise source (UTC-PD) respectively.

$$M = \frac{1 - |\Gamma_{RCV}.\Gamma_{NS}|^2}{(1 - |\Gamma_{RCV}|^2).(1 - |\Gamma_{NS}|^2)} \tag{3.2}$$

To extract the ENR of the UTC-PD, the output noise power of the source is measured for two states P_{ON} and P_{OFF} , when the source is switched ON and OFF, respectively [56]. The Y-factor was determined as the ratio of these power measurements.

$$Y = \frac{P_{ON}}{P_{OFF}} \tag{3.3}$$

First, the effective hot noise temperature ($T_{HOT}^{A,e}$) is determined in the waveguide plane A (using 3.4) and the Y-factor measurement.

$$T_{HOT}^{A,e} = T_{RCV}.(Y - 1) + Y\frac{T_{cold}}{M} \tag{3.4}$$

Then the available hot noise temperature is determined by multiplying with the mismatch factor M (3.5).

$$T_{HOT}^{A,av} = T_{HOT}^{A,e}.M \tag{3.5}$$

Finally, the available excess noise ratio at plane A can be determined as in 3.6 [33].

$$ENR_{A,av} = \frac{T_{HOT}^{A,av} - T_{cold}}{T_0} \tag{3.6}$$

The extracted ENR for the UTC-PD in the frequency range 260-325 GHz is shown in Fig. 3.5 for several values of photo-current (controlling the optical power). As expected, the ENR value produced increase as we increase the optical power [56], and the obtained ENR value is proportional to I^2.

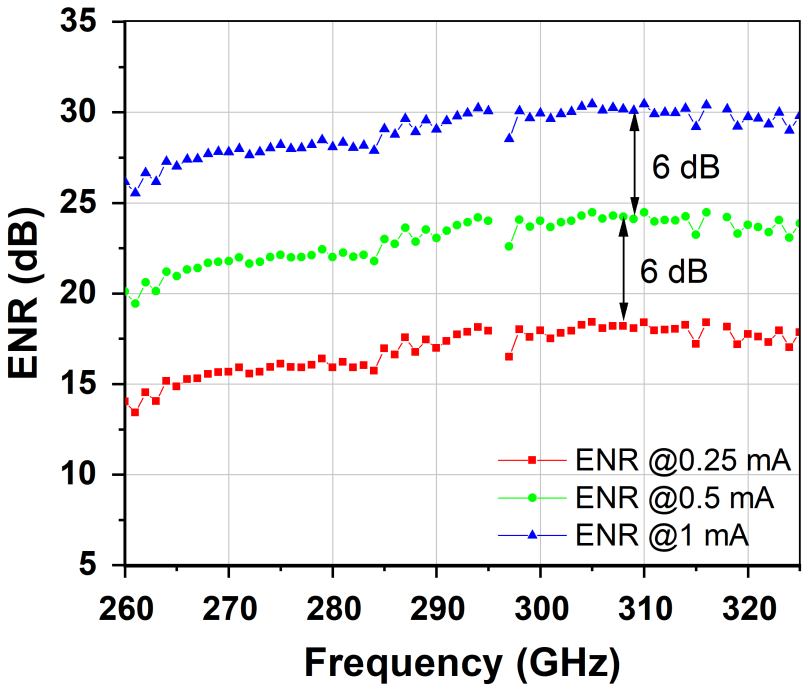


FIG. 3.5: Extracted ENR of the UTC-PD for several biasing currents.

3.2.2 Noise Figure Extraction Of LNA Using UTC-PD

To validate the use of the UTC-PD as a noise source, it has been used in the assembled noise measurement test bench to extract the NF of a packaged LNA. The WR3.4 wave guide module presented in this section is a three stage LNA based on a high performance metamorphic HEMT technology, integrated in a wave guide module. First, a small-signal wave guide measurement using a vector network analyzer (VNA) calibrated in TRM (Thru, Reflect, Match) and using source port < -35 dBm was used. The S-parameters measurements of the LNA are shown in Fig. 3.6

Referring to section 2.7 the LNA (the DUT) has been placed between the output flange of an isolator connected to the output of the noise source (to prevent reflected signals flowing back to the NS output) and the input of the noise receiver (RCV). The available power at the photomixer output can be varied between -60 dBm and -10 dBm with control on the optical injected power. Fig. 3.7 and 3.8 show the block diagram and bench top set-up used to extract the noise figure of the LNA.

Knowing the ENR of the noise source (3.6), the available hot noise temperature at the source output (T_{hot}) is deduced. Using the Y-Method, and knowing the loss of the isolator (G_{ISO}), the total noise temperature (T_{tot}) and the total noise figure (F_{tot}) between planes A and C using (3.7, 3.8) is calculated [33].

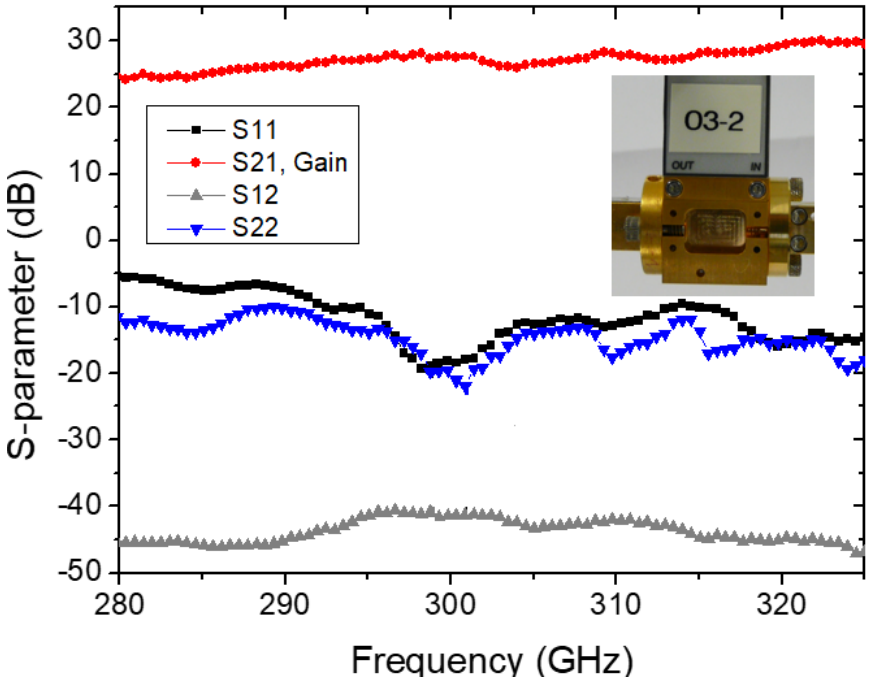


FIG. 3.6: Measured S-parameters of the LNA.

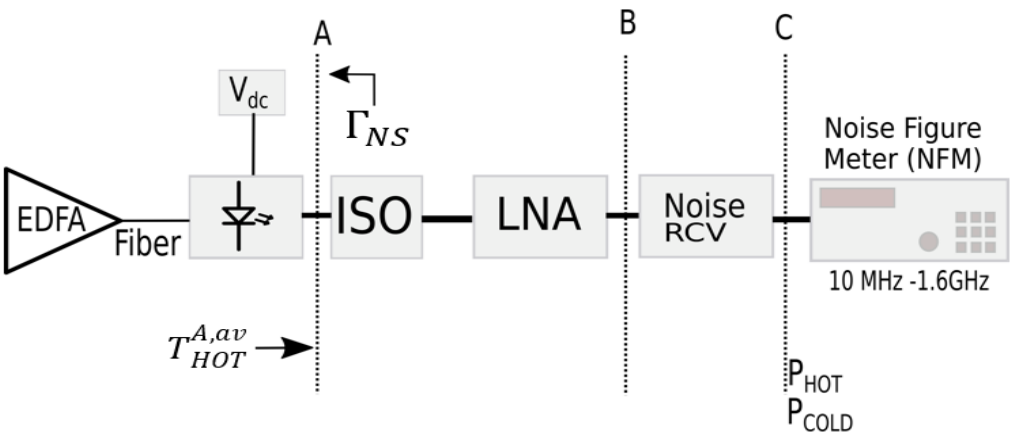


FIG. 3.7: Block diagram of the setup used to extract the NF of the LNA.

$$T_{\text{tot}} = \frac{T_{\text{HOT}}^{\text{A,av}} - Y.T_{\text{cold}}}{Y - 1} \tag{3.7}$$

$$F_{\text{tot}} = 1 + \frac{T_{\text{tot}}}{T_0} \tag{3.8}$$

Then, the extraction of the NF of the packaged amplifier was deducted using FRIIS

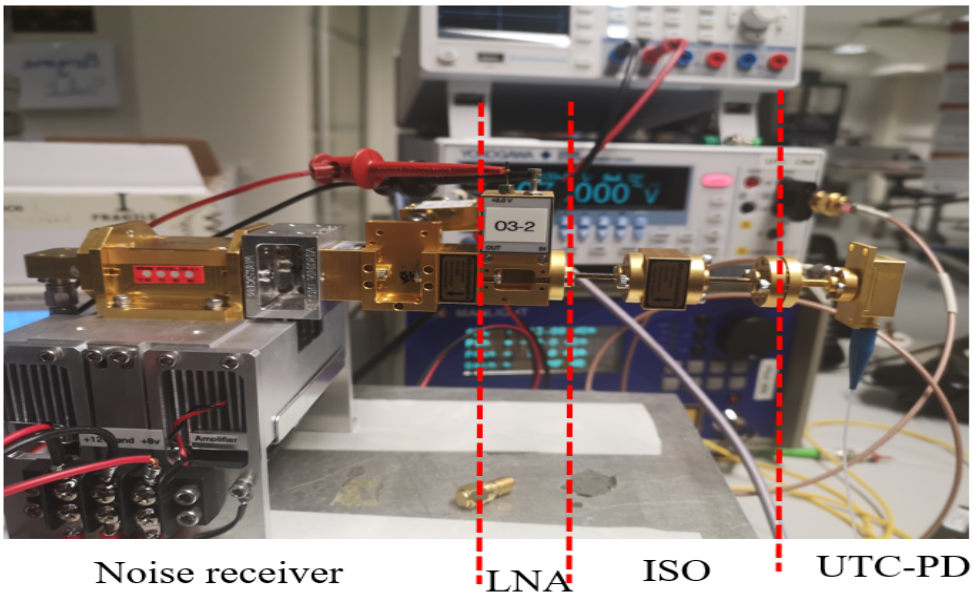


FIG. 3.8: Bench top set-up for the extraction of the LNA NF.

formula (3.9), knowing the amplifier gain (3.10) and the noise figure of the receiver [33].

$$F_{\text{Amplifier}} = (F_{\text{tot}} - F_{\text{ISO}} - \frac{F_{\text{RCV}} - 1}{G_{\text{ISO}}.G_{\text{Amplifier}}}).G_{\text{Amplifier}} + 1 \tag{3.9}$$

$$G_{\text{Amplifier}} = \frac{P_{\text{plane B}}}{P_{\text{plane A}}} \tag{3.10}$$

The gain is simply deduced by measuring the input and output power at the input and the output of the amplifier respectively. The injected power at the LNA input is the power measured at the output of the UTC-PD when connected directly to the receiver and read on the NFM as in Fig. 3.3, which is possible since the power produced is beyond the MDS conditions of the receiver. The output power is measured at the output of the amplifer with the set-up shown in Fig. 3.7. The extracted noise figure of the LNA and the measured gain are shown in Fig. 3.9.

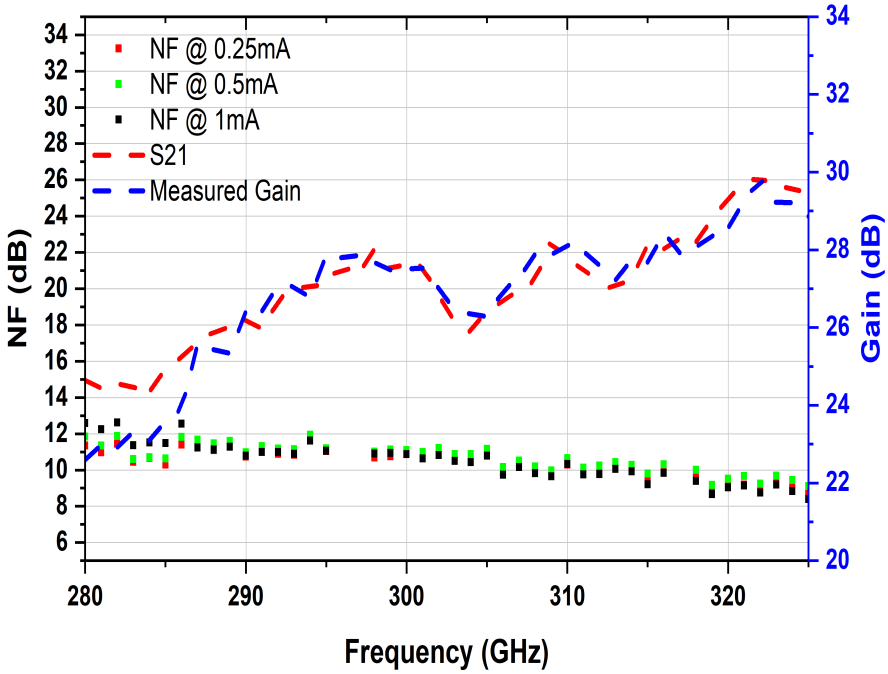


FIG. 3.9: Extracted noise figure and measured gain of the LNA.

3.3 UTC-PD Application In Power Measurements

After the demonstration of the use of a UTC-PD as a noise source, we will use it in another configuration to perform power measurements on active devices in the millimeter wave and sub-terahertz frequency range. Furthermore, the advancement in the industries of micro and nano technologies, enabled high performance transistors and associated circuits, in the context of large operational bandwidth required for high data rate communications at 300 GHz using the recent IEEE 802.15.3d standard for 100 Gbps wireless connectivity [57]. This in turn increased the demand on high performance amplifiers for application in high-speed transceivers, high-resolution radars, and instrumentations, where amplifiers (LNA or PA) present one of the main components of the RF front-end receiver [58, 59]. To obtain high system specifications, the amplifier design has to achieve a good trade-off between noise figure, gain, linearity, and power consumption. An important parameter to investigate when designing an amplifier is the third order inter-modulation point (IP3), closely related to the device linearity and dynamic range. To perform large signal and power measurements at high frequency, a signal power source working at the mentioned frequency range is required.

Usually, the non-linearity of an RF amplifier is described by IP3 or, equivalently, by the 1 dB compression point [60]. The 1 dB compression point (P1dB) is the output power level at which the gain decreases by 1 dB from its constant value, and the third

order intercept point (IP3) is the intersection of the straight lines that fit to the first and the third order intermodulation products versus the RF input power [61]. Due to non-linear effects present in an amplifier, higher order intermodulation products appear in the output spectrum when two or more tones are presented at the input of the amplifier [61, 62]. The frequencies at which intermodulation distortions (IMD) are generated can be the sum or difference of various IMD products (made of second order, third order, fourth order and so on). Among the intermodulation products of different orders, the third order product is the most disturbing one because its frequency is the nearest to the fundamental product.

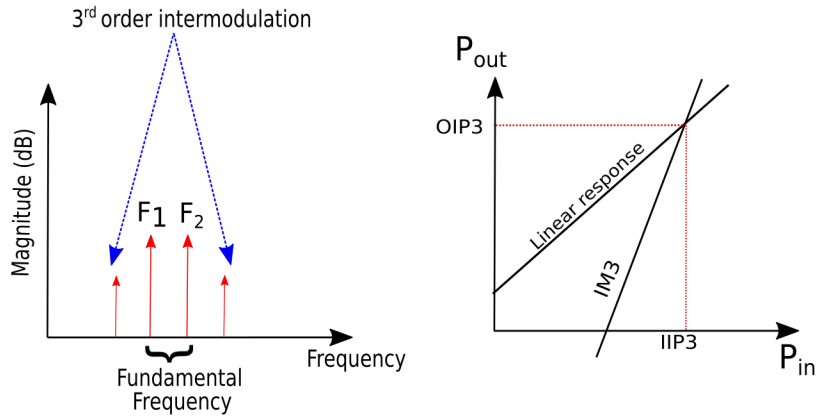


FIG. 3.10: Traditional definition of the IP3 [63].

The definition of the IP3 contains an assumption that the slope of the third order products versus the RF input power is three times that of the first order products. Traditional definition of the IP3 is shown in Fig. 3.10. At high frequencies (above 200 GHz), the third-order intercept point (IP3) characterization remains a challenge; indeed, it is complicated and costly because two separate tones closely spaced in frequency have to be generated, then applied to the device under test (DUT, usually an amplifier), allowing the fundamental and third-order distortion terms power to be measured [64].

In this study we present a new method to extract the IP3 parameter of active devices (a packaged Low noise amplifier and a power amplifier on wafer) using an optically-driven millimeter/sub-millimeter source, namely a uni-travelling carrier photodiode (UTC-PD), as the signal generator. We take advantage of the photo-mixing phenomena to generate two optical signals in the terahertz (THz) frequency range, and use the UTC-PD to convert these optical signals into electrical signals which will then be used to measure the IP3 at the output of the DUT. The advantage is that we are able to use only one wave guide device (UTC-PD) to generate the two signals (two tones) instead of two signal generators; moreover, it provides flexibility to perform the measurements at millimeter wave (mmW) frequencies (near 300 GHz) [64].

First we introduce the concept of terahertz photomixing, as the phenomenon of

combining two independent signals from two tunable laser sources set at different frequencies, generating a signal at the difference frequency in the desired terahertz region through a heterodyne process [65, 66]. The basic block diagram of the photo-mixing operation is shown in Fig. 3.11.

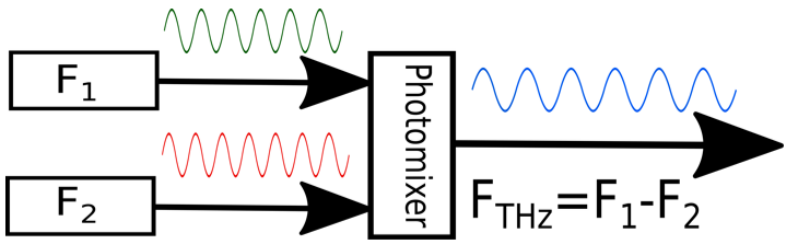


FIG. 3.11: Basic block diagram of a THz photo-mixer.

First, let us recall that two laser sources are required to generate a single THz signal. Bearing in mind that for the extraction of the IP3 parameter, two signals have to be injected at the input of the DUT, thus two THz signals through photo-mixing are required. For that, three laser sources generating three signals at frequencies f_A , f_B and f_C , respectively, are used. The outcome are two THz signals centred at two different frequencies $F_1 = f_A - f_B$ and $F_2 = f_C - f_A$. We will demonstrate the IP3 extraction method using the UTC-PD for an integrated PA MMIC and a packaged waveguide LNA device.

3.3.1 Integrated PA IP3 Extraction

The first set-up is assembled to extract the third-order intercept point (IP3) of a 300 GHz medium power amplifier MMIC based on III-V technology in an on-wafer measurement set-up [67]. Fig. 3.12 shows the chip photograph of the broadband power amplifier MMIC, which serves as a DUT for this measurement set-up.

Fig. 3.12 shows the block diagram of a five gain stages common source configuration, where stage one is a single cell, stage two and three contain two parallel transistors and the last two stages are designed with four transistors in parallel. The gate widths were chosen in a way to avoid compression in the first stages. The measured S-parameters are shown in Fig. 3.13 with a small signal gain of more than 15dB in the frequency range of 279 to 313 GHz which corresponds to a bandwidth of 34 GHz. The maximum gain of 18dB is located at 303GHz. The bias condition of the small signal measurement was $V_d = 1V$ and $V_g = 0.1V$. For this bias point the total current draw by the power amplifier is $I_d = 143mA$ which results in a current density of each transistor of $I_d = 377mA.mm^{-1}$. The magnitudes of the measured input and output reflection parameter for the operation bandwidth are below - 6 dB and - 4 dB, respectively.

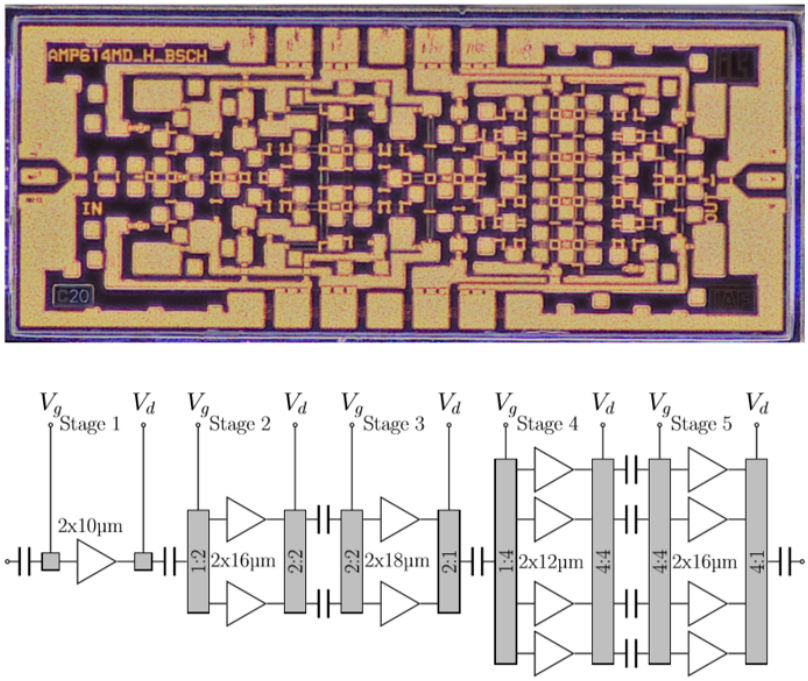


FIG. 3.12: Chip photograph and block diagram of the five-stage broadband power amplifier. Chip size is 1.75mm x 0.75mm.

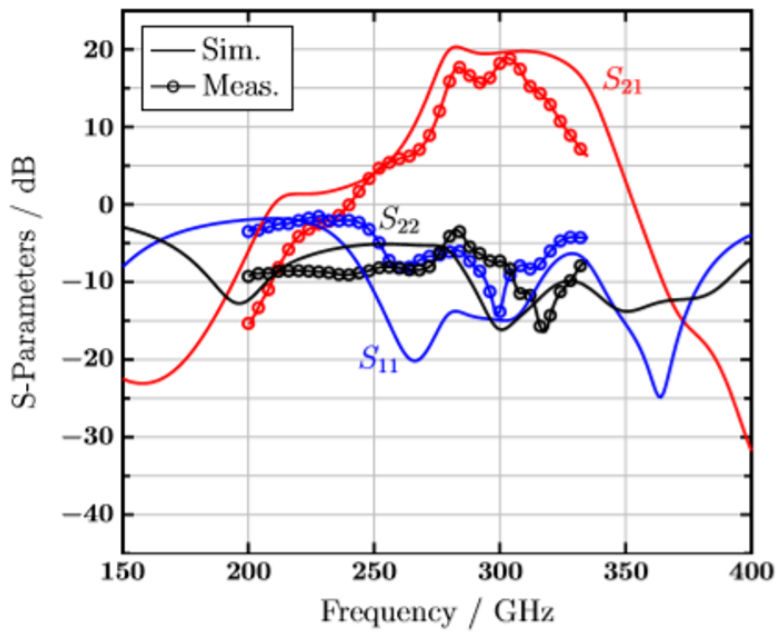


FIG. 3.13: Measured and simulated S-parameters of the five-stage broadband power amplifier.

For this setup, in order to perform the measurements near the 300 GHz frequency range, the three laser sources are set to generate three optical signals at frequencies $f_A = 194THz$, $f_B = 193.701THz$ and $f_C = 194.301THz$, producing two

signals at frequencies $F_1 = 301GHz$ and $F_2 = 299GHz$ respectively, separated by Δf=2 GHz. Using optical combining techniques, the three optical tones are simultaneously injected at the input of the uni-travelling photodiode (UTC-PD). As a result, the signal at the photodiode output is composed of two RF tones, at frequencies F_1 and F_2 , respectively. The set-up is described in Fig. 3.14.

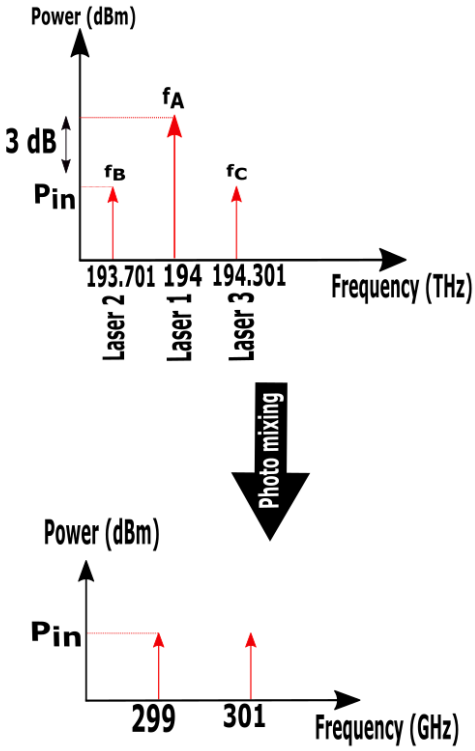


FIG. 3.14: Concept of two-tone generation using UTC-PD.

UTC-PD photo-mixers have been able to produce signals close to mW levels at 300 GHz [68], enabling to drive state-of-the art LNAs or MPAs up to the compression regions. The power of the two beat signals at F1 and F2 can be swept with the control of the photocurrent in the UTC-PD. Taking into account the noise figure of the receiver (harmonic mixer), a dynamic range of approximately 50 dB is obtained [64].

Now, that the two RF signals are generated at the output of the UTC-PD, it operates as a signal source to extract the IP3 parameters of the PA. First the UTC-PD is connected to a power meter in order to measure the absolute output power of the source (contribution for the two tones). Then the UTC-PD is connected to the receiver in order to calibrate the signal power read at the spectrum analyser (ROHDE AND SCHWARZ FSU Spectrum Analyzer 20 Hz-67 GHz), so that the down converter losses are determined. The set-up is shown in Fig. 3.15.

For IP3 extraction the PA is then connected (wafer-level) between the output of the source (UTC-PD) and the input of the receiver; the latter is a mixer used to down-convert the MPA output signal from RF frequencies to baseband frequencies and

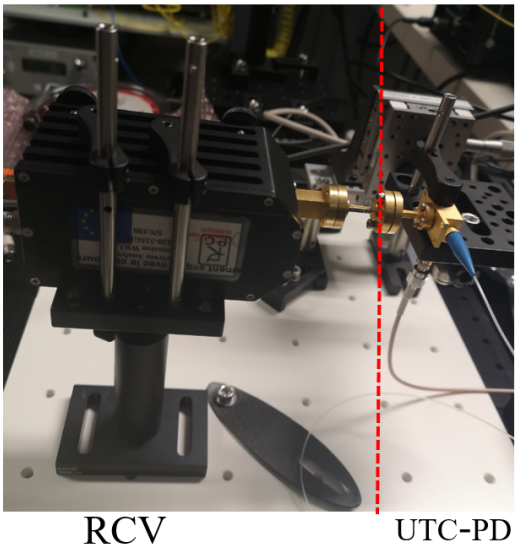


FIG. 3.15: UTC-PD connected to the WR3.4 receiver to calibrate the signal power read at the spectrum analyser.

spectrum analysis. The mixer output signal is then applied to a spectrum analyser. The block diagram of the set-up is shown in Fig. 3.16. To access the MPA on chip,

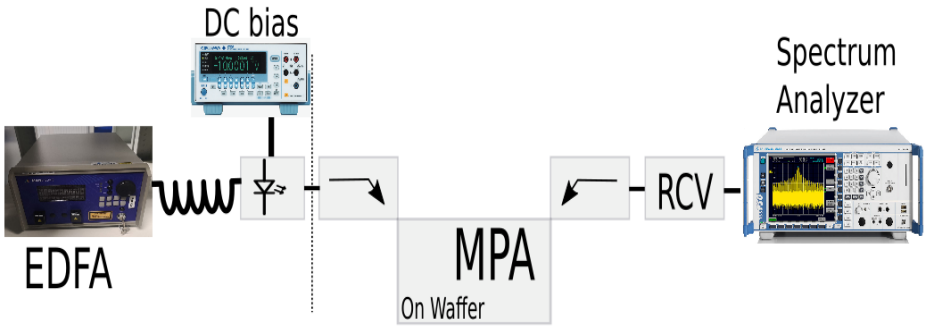


FIG. 3.16: Block diagram of the setup for IP3 extraction of an on-wafer LNA using the UTC-PD.

the wave guide (WG) output port of the UTC-PD is connected to the input of WG structure of two bends which are then in turn connected to the input flange of an RF probe. On the other hand,the output of the MPA is accessed through an RF probe which is connected at the output to the input flange of a two bends structure. The WG output port of the bend is connected to the input of the receiver through an attenuator. The attenuator is placed to insure the output power from the MPA does not saturate the receiver (Harmonic Mixer). The connection is presented in Fig. 3.17.

The optical tones are monitored throughout the measurements to insure an equal

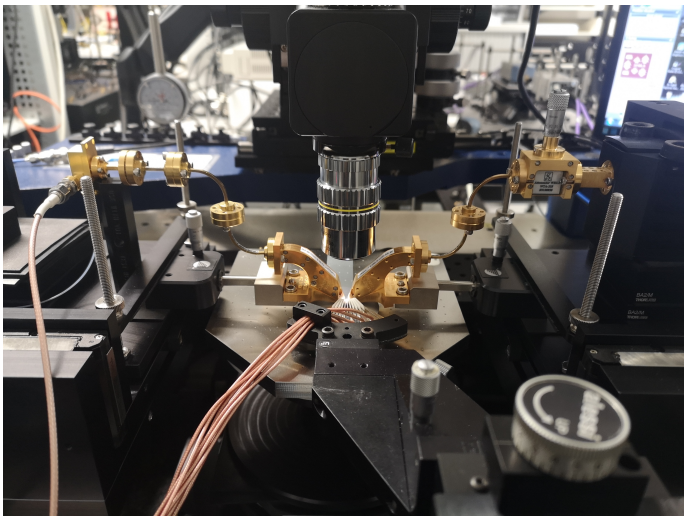


FIG. 3.17: Experiment set-up for the IP3 extraction of an integrated MPA using a UTC-PD.

power level of the two RF signals at the input of the MPA. The input power incident on the MPA (at the output of the photodiode), is adjusted by changing the biasing current of the UTC-PD. For each input power provided by the UTC-PD, the output power at the spectrum analyser is measured. For low input powers only two peaks are observed at the output, corresponding to the two fundamental tones that have been introduced at the input of the LNA located at frequencies F_1 and F_2 respectively.As the input power is increased, two other tones located at frequencies $(2F_1 - F_2)$ and $(2F_2 - F_1)$ become noticeable; these additional peaks represent the IP3 signals at the output of the amplifier(Fig. 3.18). In Fig. 3.19, the output power

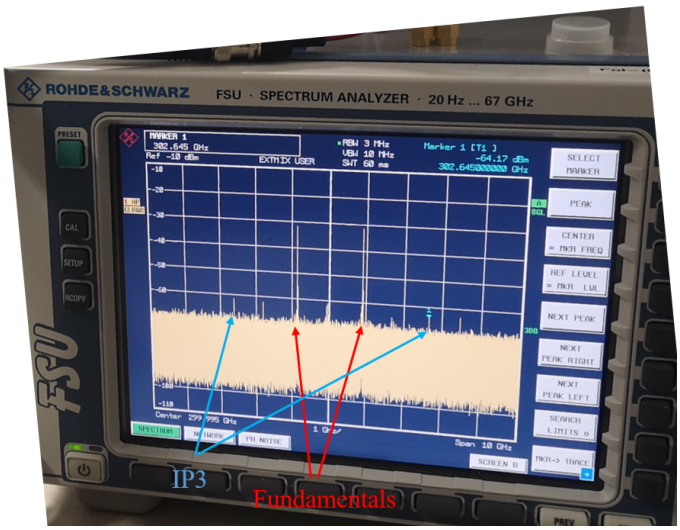


FIG. 3.18: Spectrum Analyzer measuring the peaks of the fundamental and IP3 frequencies.

of the two fundamental tones and the IP3 parameters are plotted versus the input

power from the source.It is noted that the slope of the IP3 curve increases three times faster than that of the output signal, as predicted by the theory. The measured IP3 is obtained through extrapolation of the linear portion of the first and third-order intermodulation products. The MPA used as a DUT achieves an input-related IIP3 of $-0.5dBm$ and an output related OIP3 of $13.7dBm$ [64].

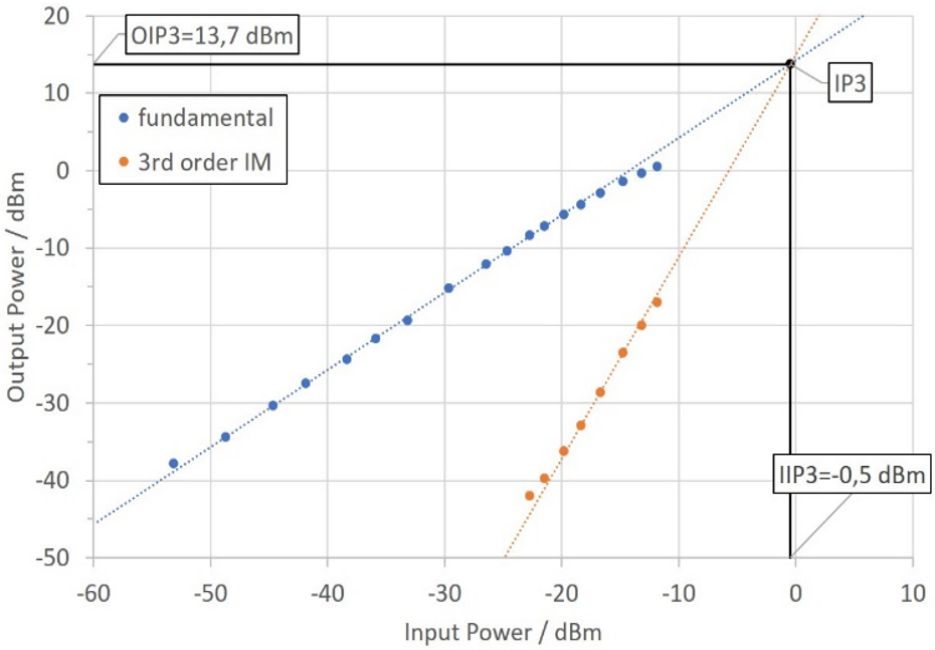


FIG. 3.19: Output power signal and IP3 plotted for various input powers.

3.3.2 IP3 Extraction Of A Waveguide-Packaged LNA

The packaged LNA used in this section is that represented in Fig. 3.6. Looking on the matching of the device, the best performance is achieved around 300 GHz, where the LNA achieves 27 dB gain. Accordingly, we choose this frequency range for the intermodulation measurements Fig. 3.20. As stated in section 3.3, the concept of photomixing will be used for the extraction of the intermodulation response of the LNA. Therefore, two signals must be injected at the input of the LNA, thus we need to generate two THz signals using photo-mixing process. For this measurement, three laser sources are used to generate the three signals at optical frequencies $f_A = 194\ THz$, $f_B = 193.701\ THz$ and $f_C = 194.301\ THz$ respectively. Similar to the previous measurement, the photomixer output in that case is two mm-wave/THz signals centred at two different frequencies. Here we chose $F_1 = f_A - f_B$ and $F_2 = f_C - f_A$ ($F_1 = 299\ GHz$ and $F_2 = 301\ GHz$ separated by $\Delta f = 2\ GHz$). The block diagram is shown in Fig. 3.21. Thanks to the photomixing process, the two-tones are generated within 1 single device, thus injection in the LNA is very simple. The same concept can be also applied with a multiple frequency signal.

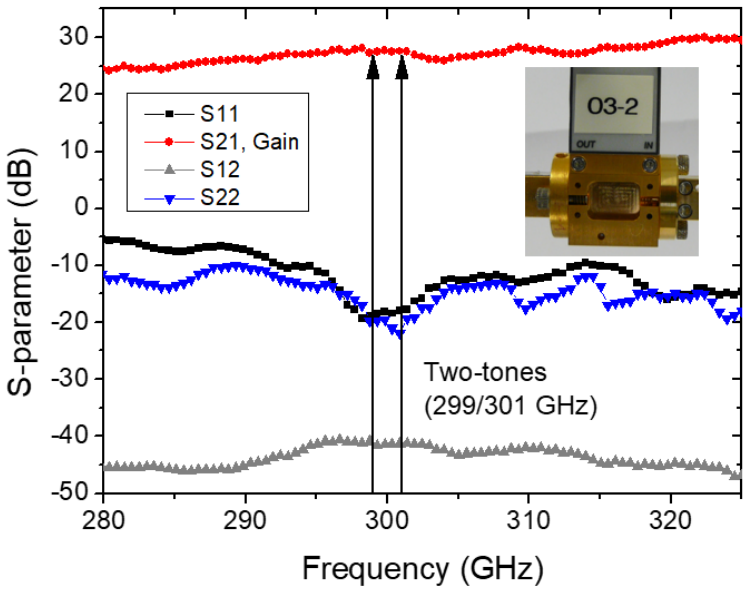


FIG. 3.20: Packaged LNA S-parameters. The arrows shows the chosen frequencies to perform IP3 measurements.

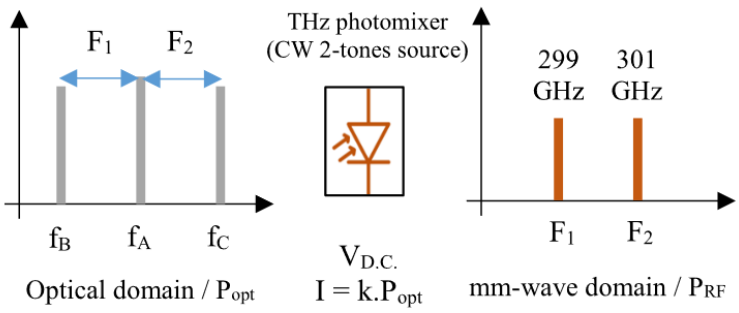


FIG. 3.21: Laser setup for IP3 extraction for LNA IP3 extraction.

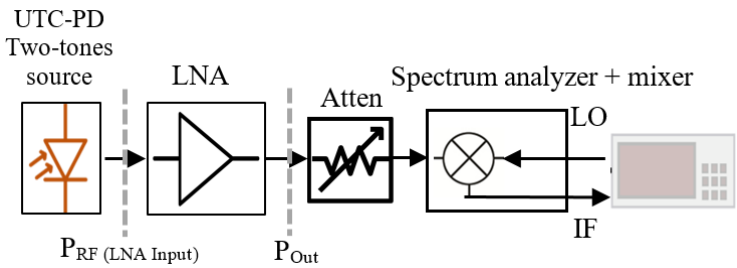


FIG. 3.22: Measurement setup of intermodulation terms of the LNA.

To evaluate the intermodulation response of the LNA, the LNA is placed between the THz photomixer and the input of the receiver as in Fig. 3.22, and the attenuator (WR3.4) is used to avoid any saturation of the measurement equipment. During measurement, the power calibrations were done using a PM5 power-meter

[69]. The optical tones are adjusted to get equal power on the two RF signals at the input of the LNA. The input power incident on the LNA (PRF), is varied by changing the Popt. At LNA output, a mixer is used to measure the power of the tones. For low input powers we only observe the two fundamental tones (F_1 and F_2). Increasing the power at the input, give rise to two other tones located at frequencies ($2F_1 - F_2$) and ($2F_2 - F_1$). These additional peaks represent the IP3 signals of the amplifier. Furthermore, as the input power increases additional peaks representing the fifth order terms are visible (IP5) at frequencies ($3F_1 - 2F_2$) and ($3F_2 - 2F_1$). The power measured at the output of the LNA versus the input power is shown in Fig. 3.23. Γ_{RCV} and Γ_{NS} in Fig. 3.3 can be calculated from the S-parameter measurements of the isolator (first stage of the noise receiver) and the noise source (UTC-PD) respectively.

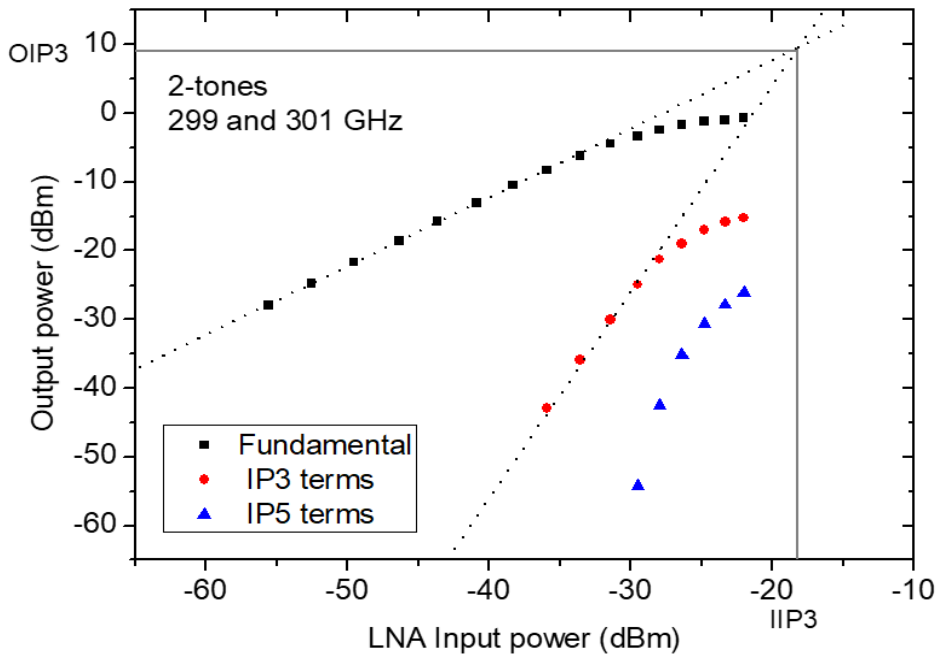


FIG. 3.23: Measurement of the intermodulation of the LNA. IIP3 is measured to be -18 dBm, and OIP3 = 9 dBm. The slope of the IP5 curve is about 1:5, however the slope determination is limited by the noise floor of the receiver.

The IP3 and IP5 curves were clearly detected. The slope of the IP3 curve found was 1:3 as expected and IIP3/OIP3 found were -18/+9 dBm, respectively. Here, the limitation of the dynamic range is only limited by the spectrum analyzer mixer, making the points below -55 dBm not measurable. The receiver used has 24 dB conversion losses, thus using GaAs sub-harmonic mixers less conversion losses, the dynamic range can be increased [70].

In order to increase the accuracy and efficiency of the set-up, the measurements were automated using a software running on Labview instrument control program, used to inject the optical signals from the laser sources and reading the output power on the spectrum analyser.

3.4 Conclusion

In this chapter a new technique was developed to evaluate the intermodulation and the noise figure of amplifiers (LNA packaged in a wave-guide module and an on wafer power amplifier) around 300 GHz, using a single mm-wave/THz source (UTC-PD). To the best of our knowledge, this is the first realization of combined power and noise measurement with the same source and first intermodulation measurement at 300 GHz. The concept is easily scalable with frequency and is an appealing approach for testing mm-wave/THz active devices, as UTC photo diodes can be used at far higher frequencies. The set-up is done taking advantage of the photo mixing phenomenon, where it is possible to generate two THz/mmW at the output of a single source (photo diode), by injection several optical signals at the input. The measurement set-up is shown in Fig. 3.24. Moreover the UTC-PD was also used in another configuration as a noise source, and was used to extract the noise figure of the packaged LNA module in the frequency range up to 325 GHz.

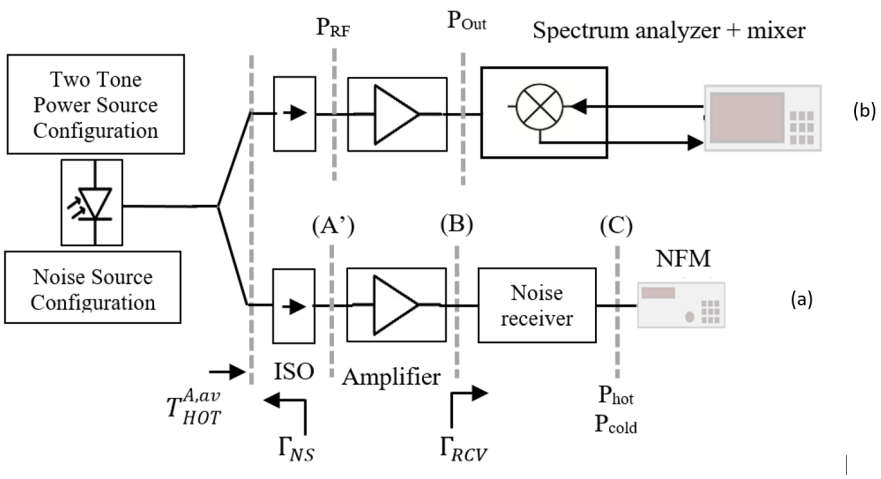


FIG. 3.24: (a) Measurement of the ENR of the THz photonics source. (b) Measurement of the NF of the amplifier block

Chapter 4

Design, Characterization and Application of LNA Using BiCMOS 55 nm Technology

4.1 Low Noise Amplifiers Basic Topologies

As mentioned earlier, the high performance of transistors allowed the fabrication of systems and devices with large operational bandwidth for high data rate communications. This in particular is of advantage for wireless communication systems, radar and imaging systems. Moreover, in communication systems, a low noise amplifier (LNA) constitutes one of the main component of the RF front-end receiver [70]. The main function of a Low Noise Amplifier is to minimize the noise contribution while amplifying the small signal with a reasonable gain [71]. Depending on the systems and the application in which it is used, the LNA can be designed according to various topologies and structures. Table 4.1 shows a brief summary of the basic LNA topologies in CMOS technology that are considered during the amplifier design [72].

TABLE 4.1: Overview Of Basic LNA Topologies.

Common-Source Stage with:	**Common-Gate Stage with:**	**Broadband Topologies:**
Inductive load	Inductive load	Noise Cancelling LNAs
Resistive feedback	feedback	Reactance Cancelling LNAs
Cascode with inductive load inductive degeneration	Cascode inductive load	

Common-source (CS) and common-gate (CG) topologies are two widely used configurations in LNA circuits. CS LNA has high gain and good noise performance while CG configuration leads to low power, robust against parasitic and stable circuit [73] but have low noise performance. Cascode LNA promises high power gain, good noise performance, low power consumption and high reverse isolation [73–

75]. Therefore, cascode stage configurations have widely been used in mm-wave frequencies [76], but unfortunately the noise and gain performance of cascode stage degrades at higher frequencies. This is due to substrate parasitic admittance at the drain-source common node that increases as frequency increases [73]. Table 4.2 shows a comparison between several LNA topologies in CMOS and HBT transistor amplifiers.

TABLE 4.2: CMOS and HBT Transistor Amplifiers Topologies.

- BiCMOS Transistor Amplifier

	CE	**CB**	**CC**
Current Gain	High	Low	High
Voltage Gain	High	High	Low
Power Gain	High	Medium	High
Z_{in}	Medium	Low	High
Z_{out}	Medium	High	Low

- MOSFET Transistor Amplifier

	CS	**CG**	**CD**
Voltage Gain	High	High	Low
Power Gain	High	Medium	High
Z_{in}	Medium	Low	High
Z_{out}	Medium	High	Low

LNA configurations are designed using silicon technologies (CMOS, BiCMOS..)[77] as well as III-V processes. At frequencies beyond 220 GHz, several LNA designs have been reported in literature. III-V based LNA devices with 29 dB gain and 6 dB noise figure (NF) have been developed up to 320 GHz [58, 78–82]. Moreover, LNA based on Silicon technologies such as SiGe and RF CMOS technologies are also designed with gain reported up to 12dB at 245 GHz [83, 84], and 32.6 dB gain at 144.5 GHz respectively [85]. At such high frequencies, the performance of InP devices outperform that established by SiGe and RF CMOS technologies in terms of noise figure, gain, cut-off frequencies and power added efficiency [71]. Table 4.3 shows a comparison of the LNA structures reported in literature using different technology processes.

4.2 LNA Circuit Design

As mentioned in section 1.5.4 the LNA can be used in the noise test bench chain after the noise source in order to increase the noise signal level, before being injected into

TABLE 4.3: Overview Of Basic LNA Topologies.

Frequency (GHz)	Gain (dB)	Noise Figure (dB)	Process	Ref
160	15	8.25	BiCMOS 55nm	[6]
252-330	26-29	6.5	35nm InAlAs/InGaAs	[58]
190	20-24	9.2-9.8	130nm SiGe	[86]
190	16.9	9.4	0.13 μm SiGe	[87]
183	17.2	9.4	0.13 μm SiGe	[88]
233	22.5	12.5	0.13 μm SiGe	[89]
185-255	14-28	-	250 nm InP HBT	[90]
152-192	7.5-10.5	-	100 nm GaN HEMT	[91]

the DUT input for the noise parameters extraction. The aim is to integrate the device on silicon to be compatible with silicon based in-situ noise measurement test bench, thus in this chapter we discuss the design of a low noise amplifier based on BiCMOS 55nm technology from STMicroelectronics. A previous work done in [6] described a LNA design using the same technology on D-Band (gain peak at around 150 GHz). As this thesis targets noise and power measurements at higher frequencies, thus the LNA was design to operate in G and J band (>200 GHz). The design is based on HBT transistors (based on BiCMOS 55nm technology from ST microelectronics) connected in CE-CB cascode multi stage topology.

The B55 nm technology is a shrink down from the 65 nm BiCMOS technology (10 % shrink). This technology is targeted because it offers the possibility of processing digital and analog signals [92, 93]. In addition, HBT transistors in this technology have transition and maximum oscillation frequencies of 320 GHz and 370 GHz, respectively [41, 94]. Derived from 55 nm CMOS technology and incorporating a SiGe Bipolar transistor, the 55 nm BiCMOS technology has 8 levels of copper metals and a last level of aluminium, as illustrated in Fig 3.22. The Back-End Of Line (BEOL) is formed from the stack of metals connected together by vias, which allows the connection between the components produced in the active area such as the transistors and the metallization level M8. The eighth metallization level (M8) is thicker than the others, allows a lower line resistance, thus it is at this level that the design of the RF micro-strip lines and the RF inductors are carried out.

4.2.1 Two Stage Design

Fig 4.2 shows the design of a two stage cascode configuration LNA. In the following design, the transmission lines TL_1 and TL_2 are chosen such that the LNA structure is matched to the previous stage at the input (in this case 50 ohm of the probe) in the desired frequency range, in order to achieve the highest gain with a minimal noise figure. The series capacitors (C_1, C_5, C_9) are used as a DC blocks to insure that the DC bias from the biasing networks of the transistors does not flow through the

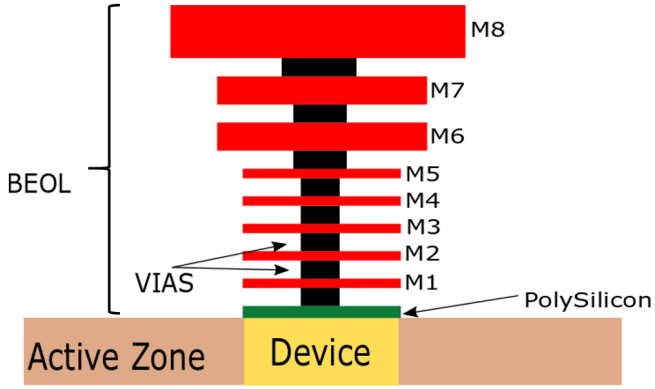


FIG. 4.1: B55 nm BEOL and metallization levels.

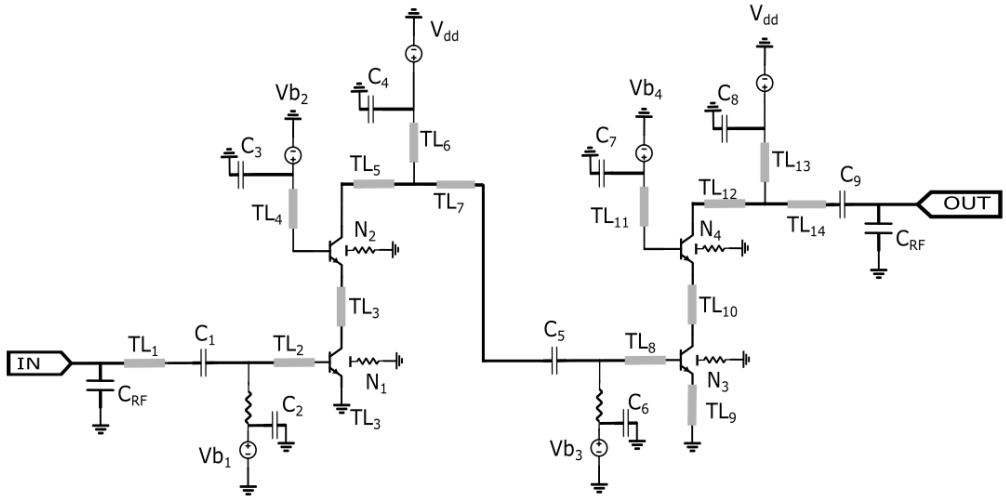


FIG. 4.2: Two Stage LNA Design.

RF path. When simulating and designing the LNA, HiCUM level 2 model of the HBT transistor was chosen, with enabling the NQS (Non-Quasi static) option. The biasing of the base of the transistors (N_1 and N_3) is applied in a presence of a 9K ohm resistor (Rhiorpo type). Capacitors (C_2,C_3,C_6,C_7) in the biasing networks are added to act as RF short. This method (Cascode configuration) is used to compensate for the so-called Miller effect, and the transmission lines in the structure were adjusted and designed to find a compromise between high gain, low noise factor and stability, in order to preserve the complete circuit from an unstable state.

The operational frequency of the LNA structure is set by the size of the transistors. Smaller transistor size can operate at higher frequencies but will achieve a lower gain, while large transistors will increase the gain but decrease the frequencies on which the LNA will operate. Thus the transistor size chosen in the LNA design varies to reach a considerable gain in the required frequency band, usually smaller transistors are chosen for the first transistors (N_1, N_3) on the stage, while the cascade transistors (N_2, N_4) are chosen of bigger size to boost the gain value. A two stage

cascode structure was designed using this methodology. Furthermore, to reduce the connection parasitic capacitance between the access nodes of the transistor (C_{finger}), the staircase connection is used in the design. This will increase the efficiency and performance of the transistors (Fig 4.3).

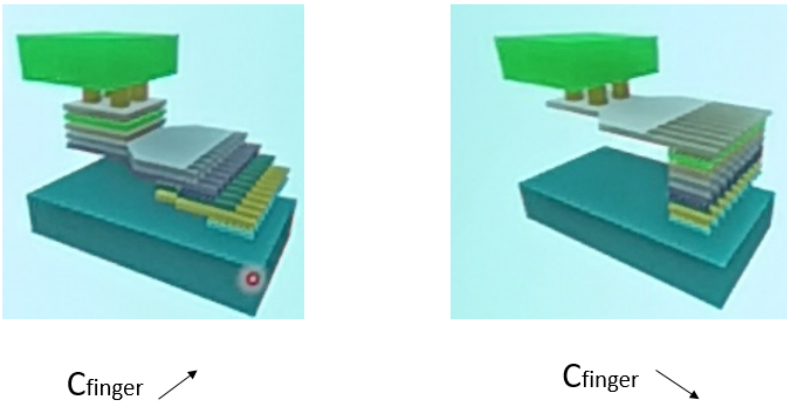


FIG. 4.3: Staircase connection on the transistor access.

LNA Circuit Simulation

The LNA design is simulated using a cadence virtuoso simulator with the associated design KIT (DK) provided by STMicroelectronics. The schematic of the LNA is shown in Fig. 4.2.

The design consists of four transistors (two stage cascode design). The C_{RF} capacitors at the input and output ports of the LNA have been added to simulate the capacitance of the RF pads (in order to take the RF pad effect in the simulation). The capacitor value of the RF pads with pitch length of 50 μm is estimated to be 3fF [95, 96] (Fig. 4.4). The pads are designed to be used with probes of both 100 and 50 μm pitch.

Resistors (Rhiorpo type) of value 4K ohm where added on the bulk of the transistors to adjust the performance of the transistors so that the frequency band is further increased (Fig. 4.5). These resistors provided in the DK by STMicroelectronics for the BiCMOS 55 nm technology are used in the design layout when working in RF frequencies. The model accounts for effects of geometry, temperature, noise, mismatch and bias non-linearity.

This is compared in simulation for two structures of a biased single HBT transistor (Fig. 4.6). In Fig. 4.6, an example circuit using a single HBT is simulated in cadence, and the imaginary part of Z_{21} is plotted in both cases, where the bulk is grounded and while the bulk is connected to a resistor. It is noticed that the circuit will resonate at higher frequency when connected to a resistor. Similarly is the case

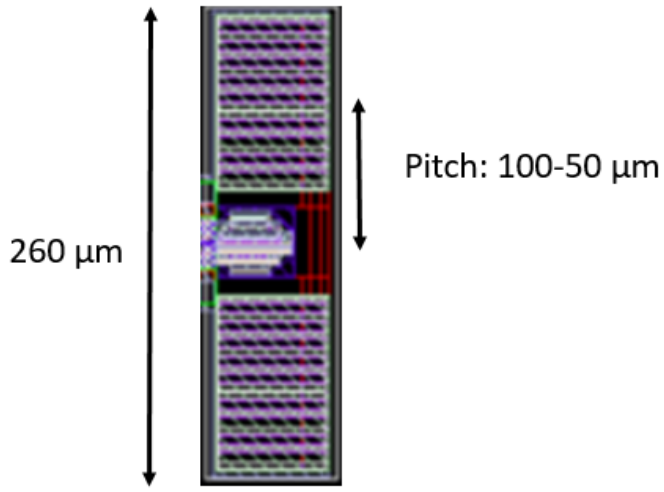


FIG. 4.4: RF Pads, compatible with pitches 50/100 μm.

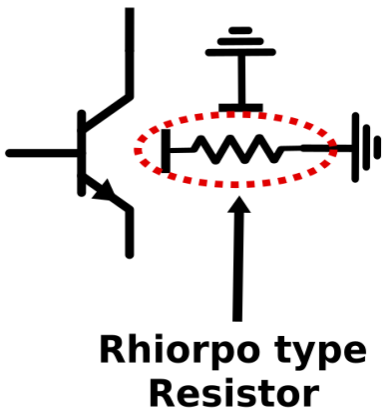


FIG. 4.5: Bulk of the HBT connected to a resistor.

of the LNA design, we noticed in simulation that the gain curve is shifted to higher frequencies when connecting all the transistor bulks to a resistor.

In this design, the transistor N_1 through N_4 have an emitter width of (W=0.2 μm) and emitter lengths (L=2.5, 4.5, 3.25, 4.5 μm) respectively. The length and the characteristic impedances of transmission lines used in the design are shown in table 4.4. The first transistor of each stage (N_1 and N_3) is biased with (Vb_1=Vb_3= 0.88 V). While the transistors (N_2 and N_4) are biased at the base with Vb_2=Vb_4=2.5 V. Both stages are biased with a voltage V_{dd}= 3.25 V at the collector of transistors (N_2 and N_4).

S-Parameter simulation was carried out in cadence virtuoso simulator and the results are shown in Fig. 4.7. The layout of the design is showed in Fig. 4.8 .

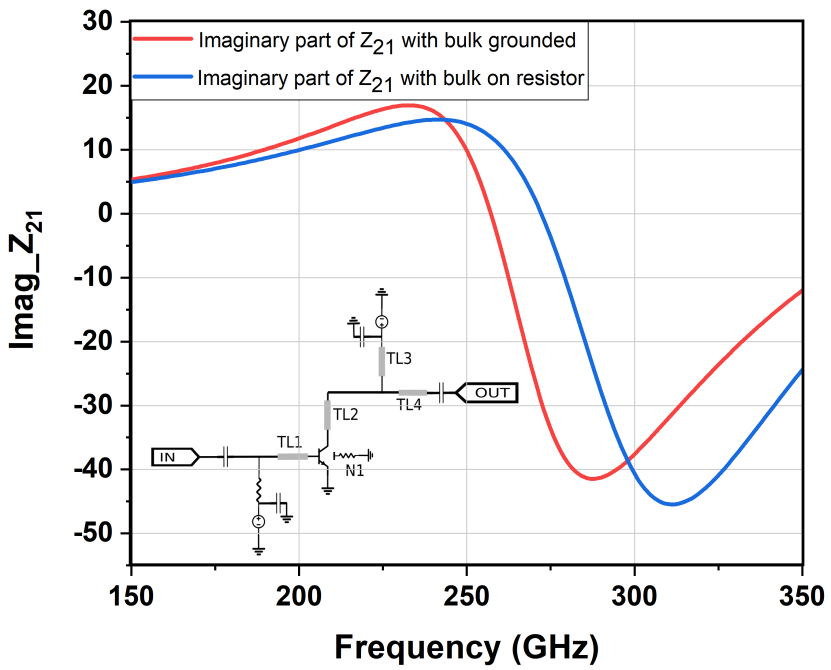


FIG. 4.6: Comparison that shows the effect of adding a resistor at the bulk of the HBT transistor.

TABLE 4.4: Transmission line Parameters.

Line	TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7	TL_8	TL_9	TL_{10}	TL_{11}	TL_{12}	TL_{13}	TL_{14}
Length μm	46	61	54	42	44	50	31	31	47	57	42	40	67	210
Z_c Ω	66	56.4	61.8	67.3	81.5	44.6	44.6	81.5	81.5	61.8	54.7	59.7	44.6	44.6

Measurements and Analysis

The LNA design was fabricated by STMicroelectronics. Although, the method of connecting a resistor to the bulk of the transistor, was carried out in the design of the LNA structure (simulation), we later learned that was not the case in fabrication. In the simulation each device (transistor, resistors...) is considered as a local device, and thus there is no problem connecting a resistor (4k Rhiorpo type) to the bulk of the transistor, so that the potential on the bulk is not grounded. In fabrication, the bulk is treated as global, that means all the bulks of all the devices on the design are connected to the same potential. That should be taken into consideration when designing the LNA structure (which was not the case in this design for this first feedback). That is, in layout, if we connect the bulk of the transistor to a resistor as in Fig. 4.2, the other bulks can not be grounded since in the actual layout the bulk will take the same potential. This may affect the results obtained in the measurement.

To test the LNA structure, first small signal measurements (S-parameters) are

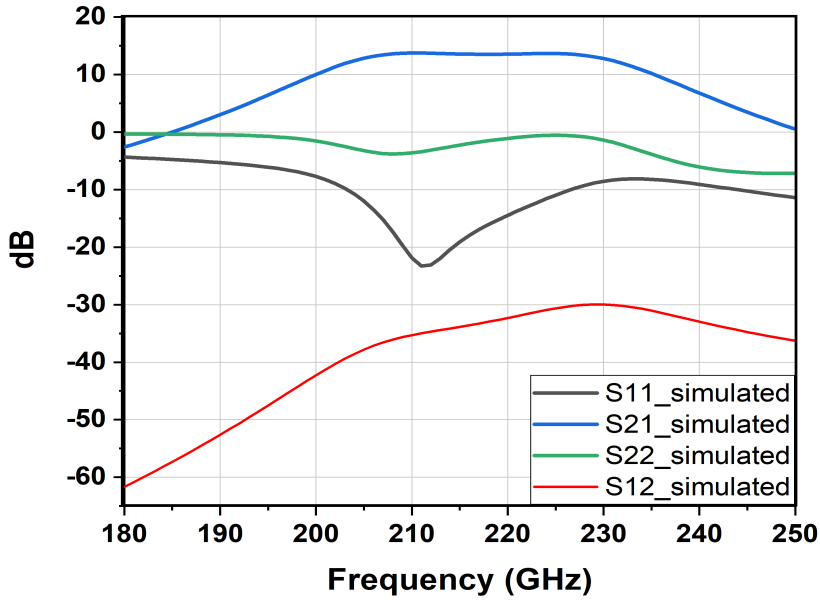


FIG. 4.7: Cadence Simulation of 2 Stages LNA design.

performed, using a vector network analyzer (VNA)(from Rodhe and Schwarz) calibrated with TRM (Thru, Reflect,Match) method. Infinity RF probes (i220-S for measurements up to 220 GHz and i325-S for measurements up to 325 GHz) are used to connect the LNA pads to the waveguide input of the extender. A precision I-V analyzer (E5270B from Keysight technologies) with 8 slot precision measurement mainframe was used for biasing the LNA. The LNA is then biased through a DC probe, with the biasing pins decoupled to the ground pins with capacitors (120 pF) to avoid D.C. coupling and thus prevent the oscillation of the LNA which can affect the gain at RF frequencies. The measurement set-up is shown in Fig. 4.9.

During the measurements the LNA bias was varied slightly to achieve the optimum output gain (S_{21}). The measured S-parameters are shown in Fig. 4.10. These results are obtained for the following biasing conditions (N_1 is biased with $1.07V$, N_2 with $2.4V$, N_3 with $1.05V$ and N_4 with $2.05V$).

It is clear that the measurements are not in agreement with the simulations, and the LNA did not work as intended. This might be due to several reasons, therefore further measurements were done to eliminate possible factors that might have affected the measured results.

In the design shown in Fig. 4.2, the biasing network of the cascode transistors (N_2 and N_4) is designed without a series resistor (unlike the CS transistors N_1 and N_3), to increase the gain (Fig. 4.11).

It is suspected that the change in the impedance (impedance **"Z"** seen at the

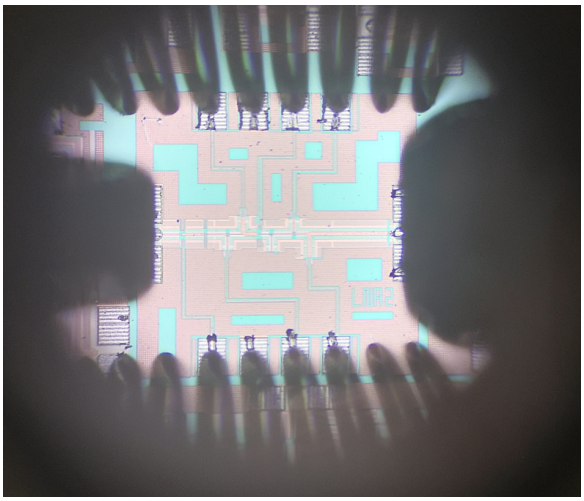


FIG. 4.8: Layout of a two stage LNA design in cascade configuration, and the view of RF probes and D.C. needles.

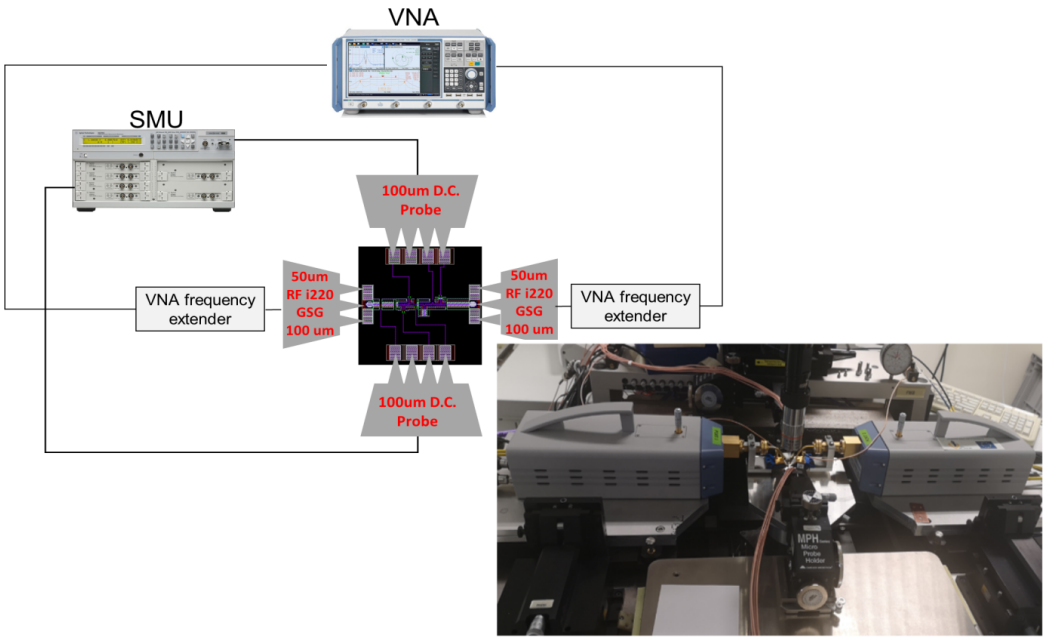


FIG. 4.9: Bench set-up for small signal measurements for the integrated 2 Stage LNA.

base of the transistor) at low frequency might affect the operation of the LNA and thus the measured gain. To verify this, the S_{21} of the LNA is measured using a voltage source to bias the base of the transistors in the LNA structure. The base current (ib) is then measured for each transistor. Then the biasing is done using a current source with the corresponding (ib) value for each transistor (Fig. 4.12). The measured S_{21} parameter was the same for both cases, which mean that the low frequency impedance of the biasing network is not affecting the gain measurements if the transistor is biased by the same base current (ib) at the transistor base.

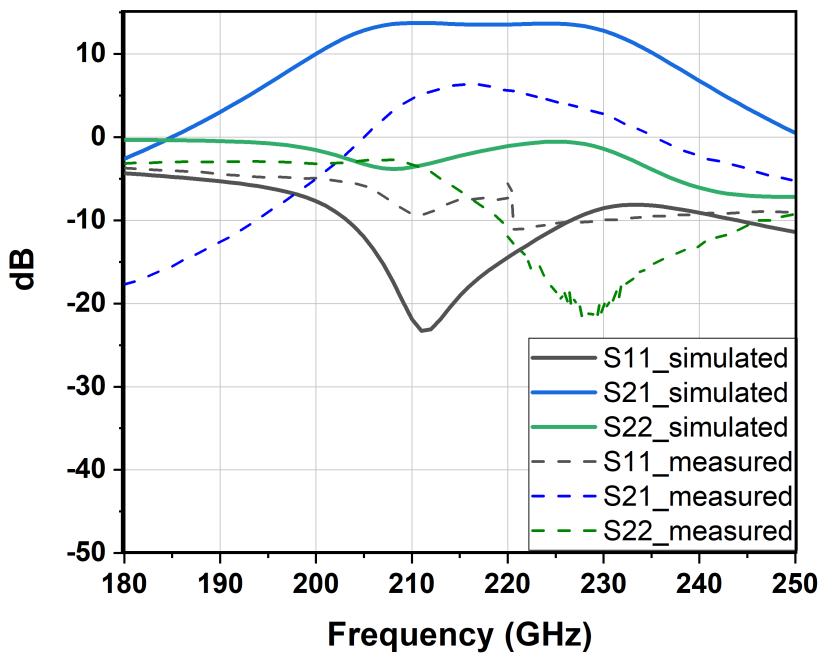


FIG. 4.10: Measured S-parameters of the 2 stage LNA compared to the simulated values.

A second measurement was carried out to test if the LNA is oscillating, since the lack of stability might also affect the gain [97]. The measurement set-up is presented in Fig. 4.13. An input CW signal is injected from the VNA at the input of RF probe 1, and the output signal is observed at the spectrum analyzer. If a single peak signal is observed, centered at the operating frequency set by the VNA then we can say that the LNA is not oscillating, else some harmonics will be seen near the fundamental frequency. After performing this test, a single tone centered at the operating frequency is observed, which concludes that the overall LNA circuit is not oscillating, thus this is not what is affecting the gain. The output signal and the experiment set-up is shown in Fig. 4.14.

To verify the obtained S_{21} parameter measurements, and have a better idea of the LNA saturation point, power measurements were also performed on the LNA sample. For the input power generation, two lasers are used to generate a single tone signal in the mmW frequency range using two optical beams through photomixing. Then a UTC-PD is used to convert this optical signal into an electrical signal to be used at the input of the LNA. Similar method was used in Chapter 3. The block diagram of the setup is shown in Fig. 4.15.

The power measurements are automated using a Labview software, where the input power signal is generated through photomixing and swept in frequency in order to generate an input signal for the desired frequency range. Then the power at

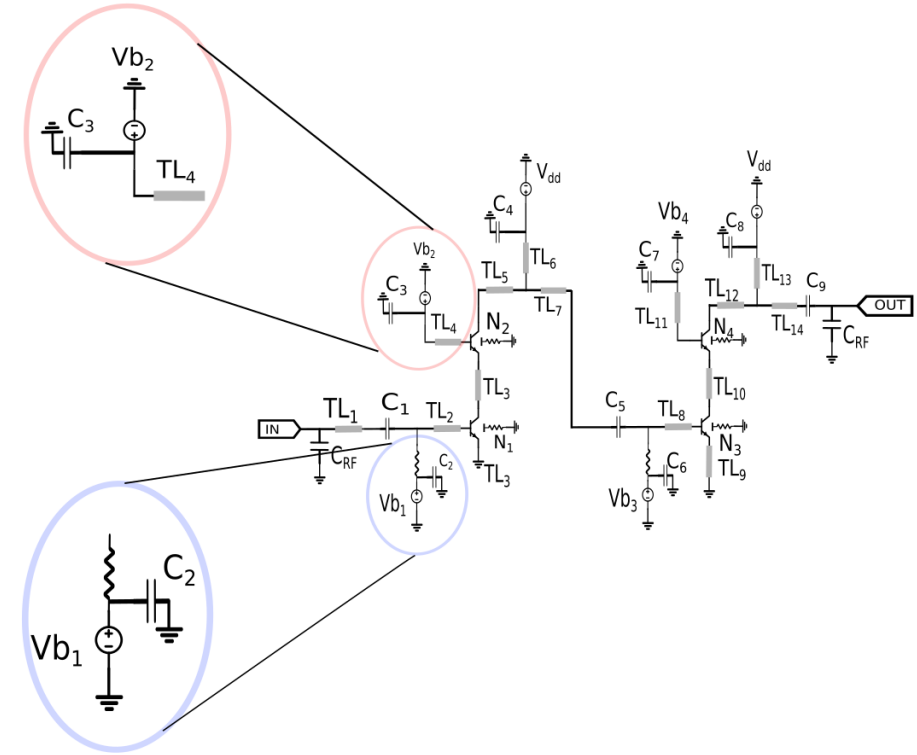


FIG. 4.11: Biasing network of the LNA cascade stages. The first transistor is biased in the presence of a series 9K ohm resistor, while the cascode stage is biased without a resistor to increase the gain of the overall structure.

the output (plane D, at the reference plane of the PM5 power meter) is measured for each frequency point. First, we place a THRU structure (as DUT in Fig. 4.15) and the output power (P_{THRU}) is measured on the PM5, this is taken as the reference power level. Then the LNA is placed as DUT and the output power (P_{LNA}) is measured again, for the same input power (photodiode biased at 0.5mA). The gain (G) of the amplifier is the difference of the two measured powers (4.1).

$$G_{\text{Amplifier}} = P_{\text{LNA}} - P_{\text{THRU}} \tag{4.1}$$

Note that the losses of the passive devices between planes A and B are about 4 dB, the RF probes used to access the DUT are infinity-probes; note that due to the unavailability of symmetric RF probes during this measurement, at the input of the DUT a WR5 range probe was used while at the output a WR3 range probe is used, since the LNA is operated between the two frequency bands, this can have a slight effect on the impedance presented at the DUT planes, but the gain measured (power measured at the output of the LNA - Power measured at the output of a THRU) is relative to the same set up configuration. The curve is then compared to the extracted S_{21} parameters measured with the VNA. The gain showed a peak value around 6 dB

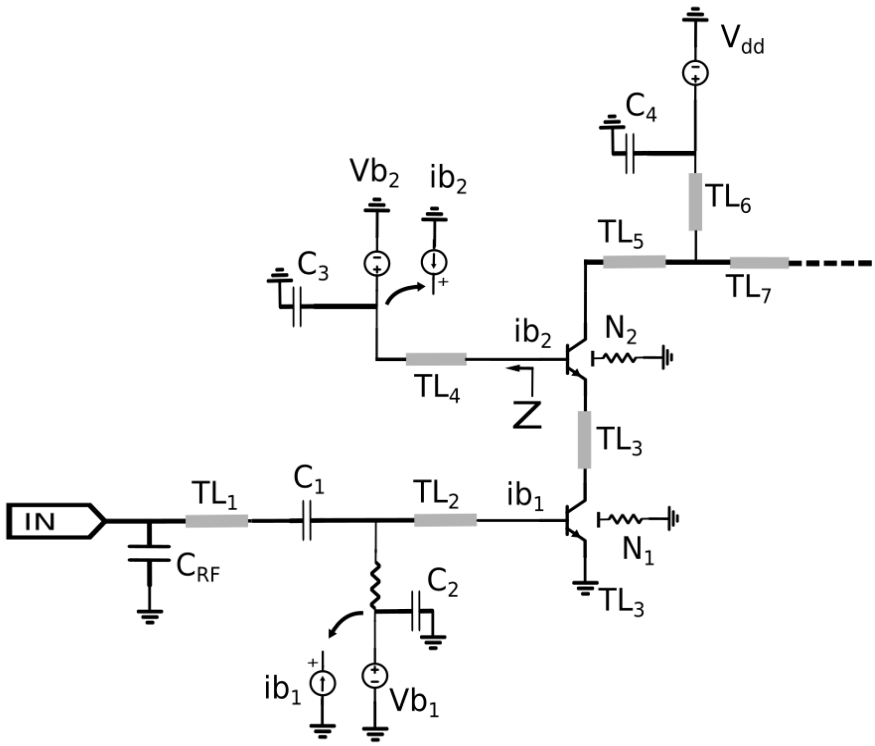


FIG. 4.12: HBT transistors of the LNA are biased once by a voltage source or a current source.

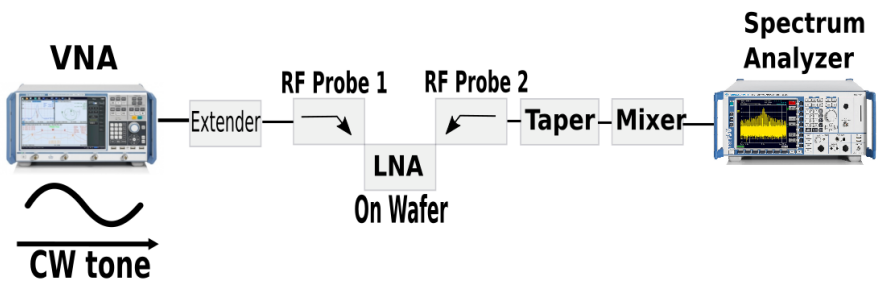


FIG. 4.13: Measurement setup for testing the LNA oscillation.

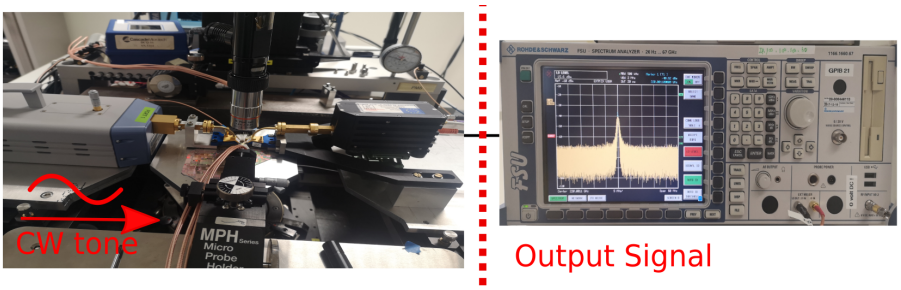


FIG. 4.14: Experiment setup for testing the LNA oscillation.

at 215 GHz. The two curves are shown in Fig. 4.16, and are in agreement which validates the gain measurements. The experiment setup is shown in Fig. 4.17.

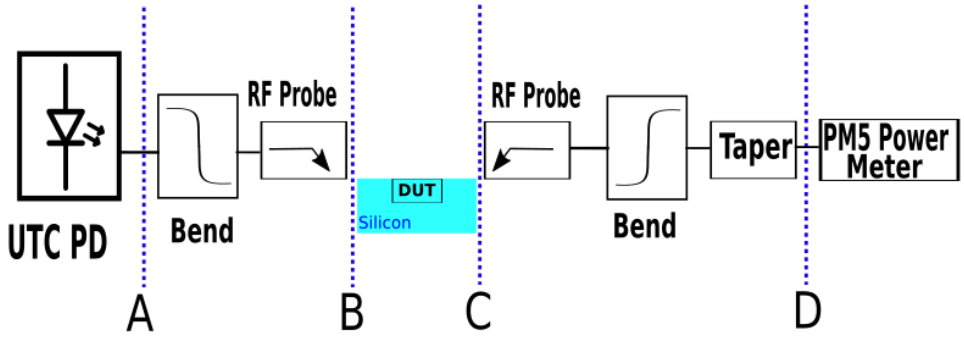


FIG. 4.15: LNA power measurements block diagram.

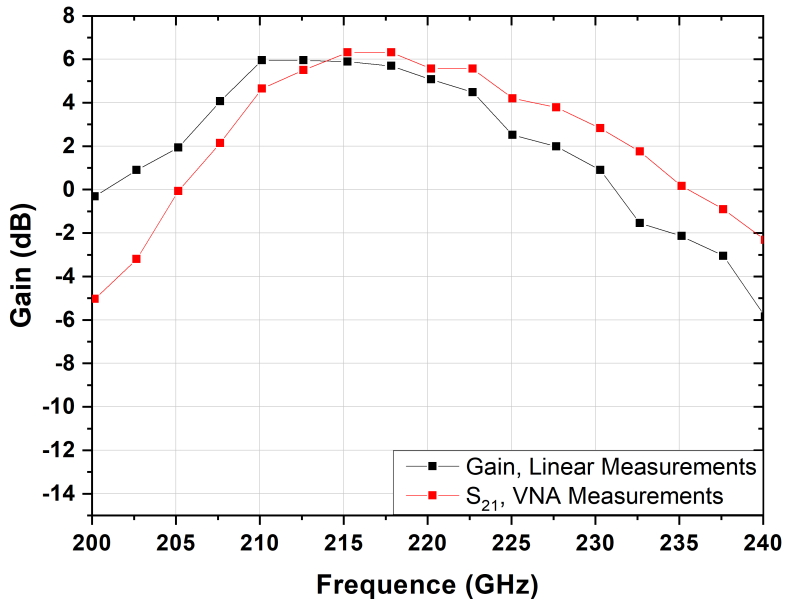


FIG. 4.16: LNA Gain extracted from linear power measurements and S-parameters measurements.

To determine the linearity of the LNA and extract the saturation power, the output power is measured versus several input power values. To insure the saturation power of the device is reached, we add an amplifier at the input of the integrated LNA (a WR4-MPA packaged in a waveguide module). The block diagram of the setup is shown in Fig. 4.18. The input power is varied by adjusting the D.C. biasing of the UTC-PD, for each input power the output power is measured at the plane of the PM5 (plane D). The measured power and the power simulated in cadence for the designed schematic are shown in Fig. 4.19, where the LNA seems linear up to -8 dBm of input power (the UTC-PD is biased at 1.7 mA), with an output saturation power of -6 dBm. Notice that, for the simulated curve, the biasing used for the HBT transistors in the LNA structure is that of the design shown in Fig. 4.7. Since the gain in the simulated circuit is higher (the intended gain is around 11dB in cadence), the

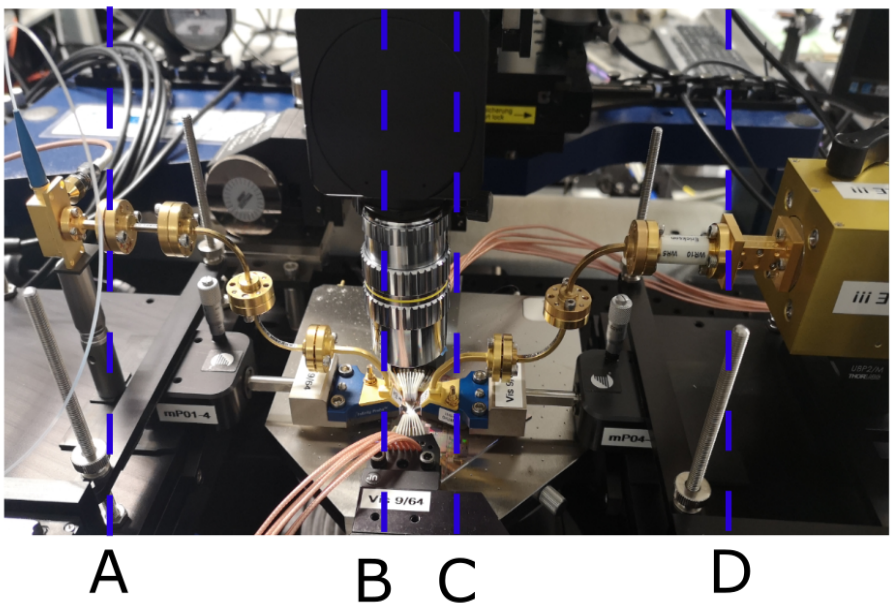


FIG. 4.17: LNA power measurements experiment setup.

output power curve is shifted from that of the measured one as expected.

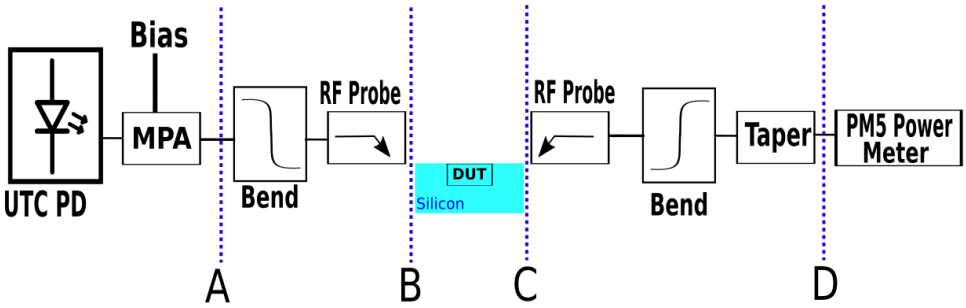


FIG. 4.18: LNA saturation power extraction setup.

The set-up in Fig. 4.18 is then used to measure the gain of the LNA for several input power values. The input power is varied by controlling the optical power of the UTC-PD. First the output power is measured at the output plane D of the THRU structure for the several input power values, then the LNA is connected as DUT and the output power is measured at the PM5 reference plane D. The gain is extracted as a function of the input power, and the results are shown in Fig. 4.20. The UTC-PD is then biased at 1.7 mA (input power at which the LNA saturates) and the saturation power P_{SAT} is measured in the required frequency band, with a 4 dB correction performed to account for the passive devices between plane C and D (probe, bend and tapper). The power versus frequency performance of the LNA is shown in Fig. 4.21.

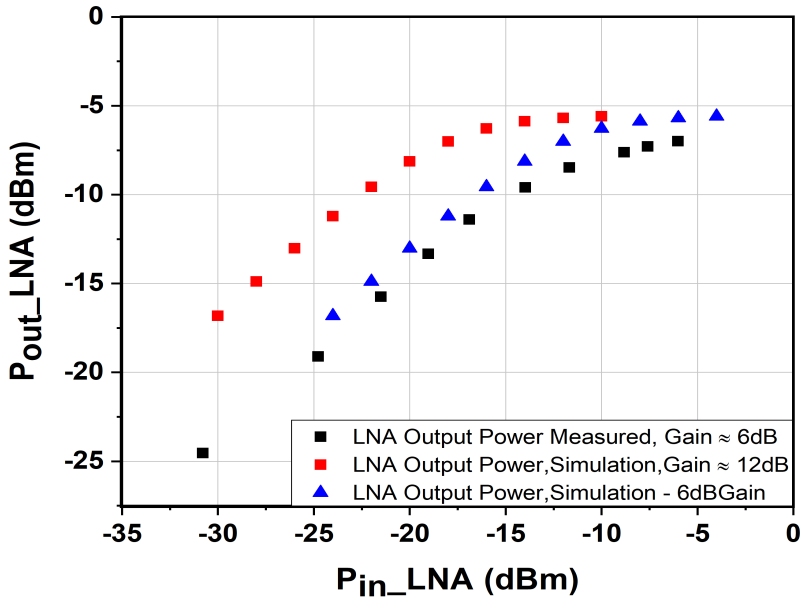


FIG. 4.19: LNA output power versus various input power.

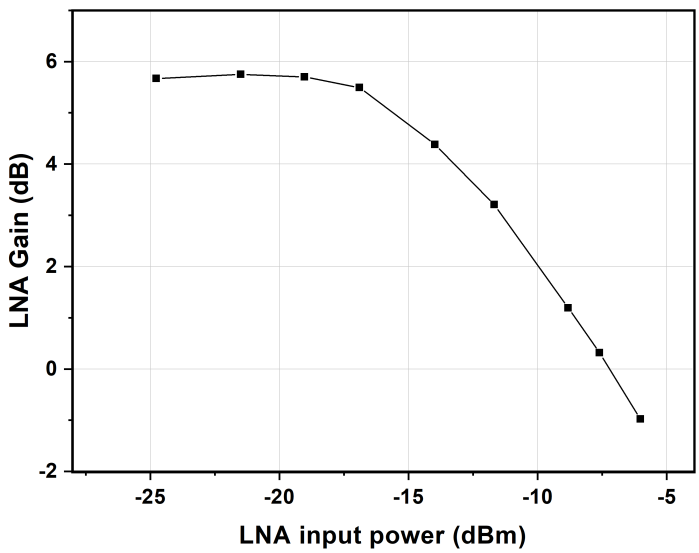


FIG. 4.20: LNA Gain versus input power.

The LNA was characterized by performing VNA measurements, also by measuring the saturation power and power response, but there are other aspects to consider such as phase and group delay response. To get a better idea of the LNA performance and to validate that it can be used as a part of a datacom system application, the LNA is used within a transmitter-receiver chain. The optical signal is modulated

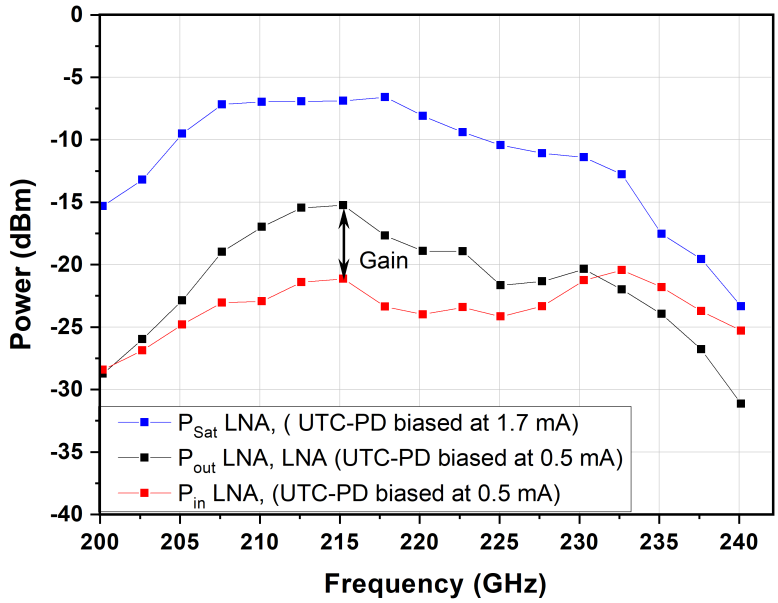


FIG. 4.21: LNA power versus frequency performance.

(AM modulation) before injected into the UTC-PD. Thus the UTC-PD output a modulated RF signal, and acts like a modulated signal source. This signal is then passed through a DUT, where it is detected at the output by a Schottky diode envelope detector [98, 99]. First the signal is passed through a THRU structure (THRU is taken as the DUT), and the output signal is measured. This is taken as the reference signal. Two signals of data rate 5Gbit/sec and 9Gbit/sec are used respectively. The eye diagrams of the signals detected at the output of the THRU structure, at a frequency of 211.6 GHz, are shown in Fig. 4.22.

Notice that for the signal transmitter at the higher data rate 9Gbit/sec, the eye diagram is more distorted compared to the 5Gbit/sec, this is due to the bandwidth limitation at the detector side. Increasing the data rate means more power is needed for the transmission signal. Therefore, the LNA is added at the receiver input to increase the output signal power (received signal at the detector input) and hence increasing the receiver sensitivity. The eye diagrams of the 5Gbit/sec and 9Gbit/sec signals detected at the output of the LNA , at a frequency of 211.6 GHz, are shown in Fig. 4.23. The detected signal is distorted, thus the opening of the eye diagram is not ideal due to the bandwidth limitation of the LNA (Fig. 4.16 the gain is not flat). The experiment set-up is presented in Fig. 4.24.

The modulated signals are detected at the output and the bit error rate (BER) is measured for various input signal power. For higher data rate more power is needed, thus using an LNA will increase the margin of data rate transmitter for the available input signal power. The BER versus input power for the two transmitted signals

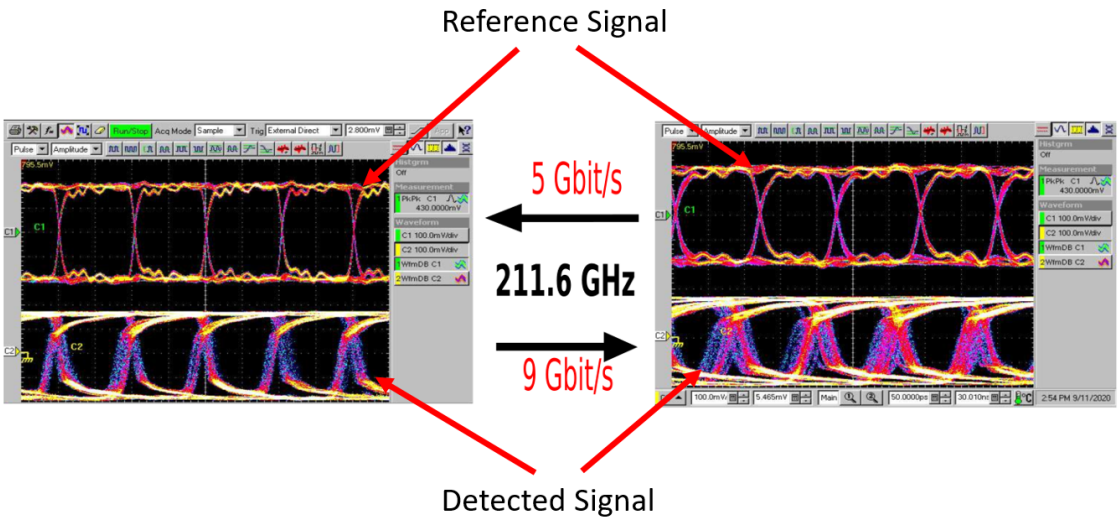


FIG. 4.22: Eye diagram of the modulated signal detected at the output of the THRU for 5Gbit/sec and 9Gbit/sec respectively .

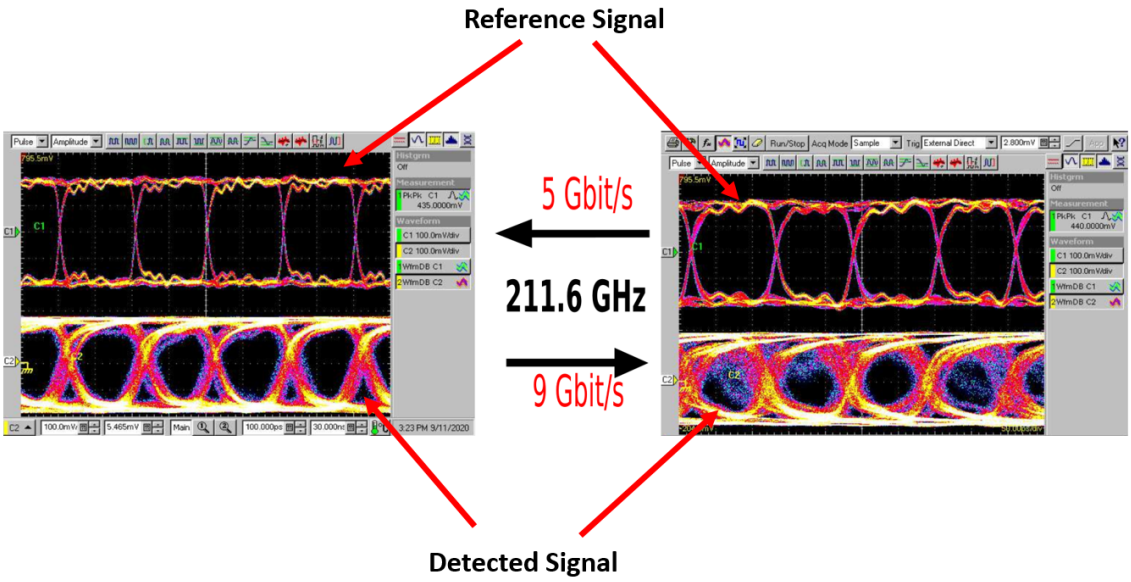


FIG. 4.23: Eye diagram of the modulated signal detected at the output of the LNA for 5Gbit/sec and 9Gbit/sec respectively .

(5Gbit/sec and 9Gbit/sec) is shown in Fig. 4.25. Notice that for the 5Gbit/sec signal, the BER curve is shifted after using the LNA (by a margin equivalent to the LNA gain). As for the 9Gbit/sec signal, as we increased the data rate more bandwidth is needed, and the detected signal was too distorted due to the fact that the LNA gain is not flat (Fig. 4.16) and thus the bandwidth needed to detect a clear signal is limited.

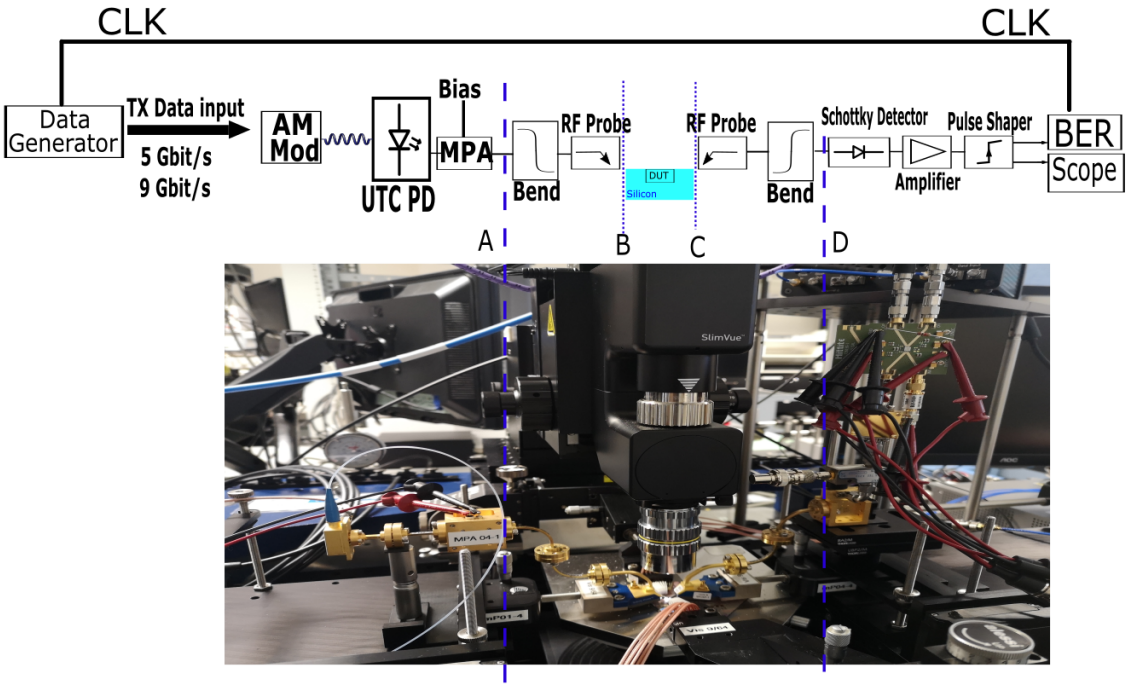


FIG. 4.24: Setup representaion of datacom chain to detect AM modulated signals at 5Gbit/sec and 9Gbit/sec.

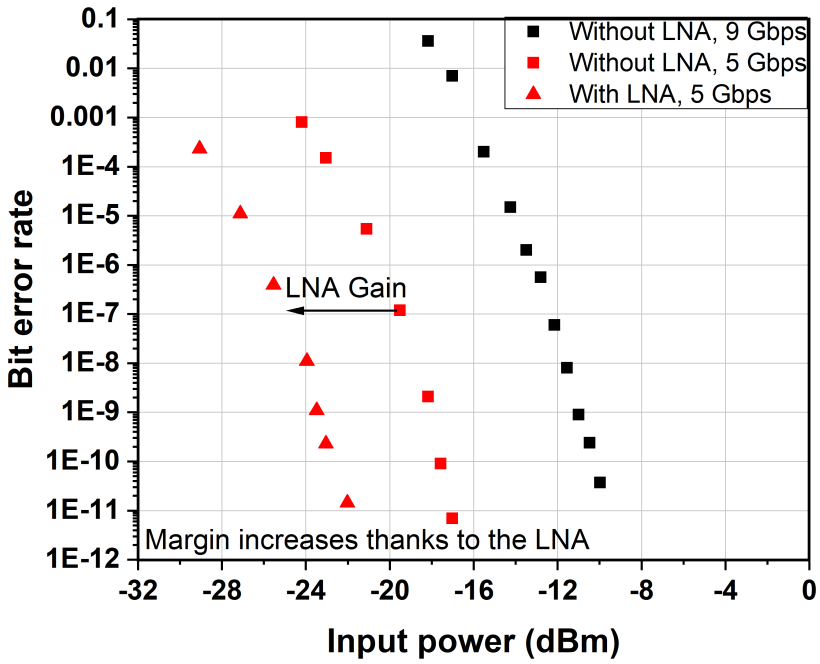


FIG. 4.25: BER curves versus input power with and without the use of LNA.

4.2.2 Conclusion

A two stage cascode LNA was designed and measured up to 240 GHz, using HBT transistors based on BiCMOS 55 nm technology from ST microelectronics. The LNA circuit was simulated in cadence virtuoso, and a gain of 13 dB was obtained up to 230 GHz with a bandwidth around 25 GHz. VNA measurements of the LNA did not agree with the simulation, where a 6 dB gain was obtained around 220 GHz and the LNA did not work as intended. Several tests were performed to eliminate the problem.

- **Power measurements:** A UTC-PD is used as a signal generator at the input of the LNA and the output signal is detected using a PM5 power meter. The gain is then extracted and compared to that of the VNA measurements. Moreover, the saturation power curve is extracted.
- **Oscillation measurements:** The LNA was tested to verify it is not oscillating. A CW tone was injected at the input of the LNA, and the output signal is observed using a spectrum analyzer, and no oscillation is detected since a peak centered at the required frequency was obtained. Furthermore, the LNA was used in a data communication chain, where a modulated signal is injected at the input, at the output a schottky diode detector is used to detect the signal. The BER curve was extracted versus the input power. The BER curve was compared in two cases, with and without the use of the LNA. The fact that the signal could be retreated also show that the LNA have no oscillations.
- **Biasing test:** The base of the HBT used in the LNA design was biased both using a current source and an voltage source. The biasing of the HBT seems to be stable and we retrieved the same gain in both cases.

Several other reasons might affect the performance on the design level. T-structures, in Fig. 4.2 for example, the transmission lines TL_5,TL_6,TL_7 form a T-shape but in the design the dimensions of the transmission line does allow direct connections to form this T-shape. Therefore, a T-shape structure had to be designed (to represent this connection) using the metal layers. This structure might not have the same performance as connecting the transmission lines in the schematic, which may cause a change in the impedance of the stubs and affect the LNA performance. This is verified in the simulation where if we change the dimensions of the transmission lines the performance maybe affected and oscillation may accrue. As perspective to improve the performance of the LNA and achieve the desired gain, future designs will be made to test the passive structures in the circuit (T-structures as a standalone element), also to test the separate stages of the LNA and the HBT structure as a single element. Also in future designs the bulk of the transistors will be grounded to avoid the conflict between simulation and fabrication. Moreover, a three-stage LNA structure is designed in attempt to increase the gain, future measurements will be done as perspective to this work.

Chapter 5

Thesis Summary

This thesis targeted the development of a noise characterization test bench, to perform noise measurements at frequencies up to 325 GHz. To perform noise measurements, it is essential to have a noise source to generate the noise signal. Commercial noise source availability remains a challenge for frequencies above 200 GHz. For this purpose, an integrated silicon based noise source (Schottky diode structure) was developed using BiCMOS 55 nm technology from STMicroelectronics.

The developed noise source was used to perform wide band in-situ noise measurements up to 325 GHz. In order to capture the noise signal, a new noise receiver was assembled. The receiver is basically a down converter which down converts the noise signal generated by the noise source, from the RF range to an IF frequency band, where the noise power is measured using a Noise Figure Meter (NFM). To cover the full frequency band (130-325 GHz), several receiver structures where used each dedicated to a part of the frequency band. To extract the noise figure (NF) of the receiver, cryogenical HOT/COLD method was used, where two temperatures are introduced at the input of the receiver structure (T_{HOT} and T_{COLD}) and the output noise power corresponding to each temperature is measured. Using the Y-method and FRIIS formula, the NF of the receiver is then exacted.

After extracting the noise figure of the assembled receiver structure, the receiver was used to characterize the noise source. Noise sources are characterized by their excess noise ratio (ENR) value, which is the noise level above the thermal noise floor. To extract the ENR value, the output of the noise source is connected to the input of the receiver, and the output noise power is measured for two states, when the noise source is turned ON (we measure P_{HOT}) and OFF (we measure P_{COLD}) respectively. Then the Y-method is used to extract the ENR of the noise source. The integrated diode noise source showed and ENR of 20 dB at 130 GHz, and the ENR value was extracted up to 325 GHz.

To validate the noise measurements, this test bench was used to extract the NF of active devices, where the device under test (DUT) is placed between the noise source and the noise receiver. The noise power at the output of the receiver is measured using the NFM. Then the Y-method and FRISS formula are used to extract the NF of

the DUT. Using this test bench the NF of a LNA was extracted up to 260 GHz.
The steps for the characterization of the noise measurement test bench are listed below, and the block diagram is shown in Fig. 5.1.

- **Step 1:** Assemble the noise receiver, perform power characterization and extract the NF using cryogenic HOT/COLD measurements.
- **Step 2:** Connect the noise source output to receiver input and extract ENR of the noise source using Y-method.
- **Step 3:** Knowing the ENR of the noise source and the NF of the receiver, a DUT is placed between the output of the noise source and the input of the noise receiver, and the NF of the DUT is extracted using Y-method and FRIIS formula.

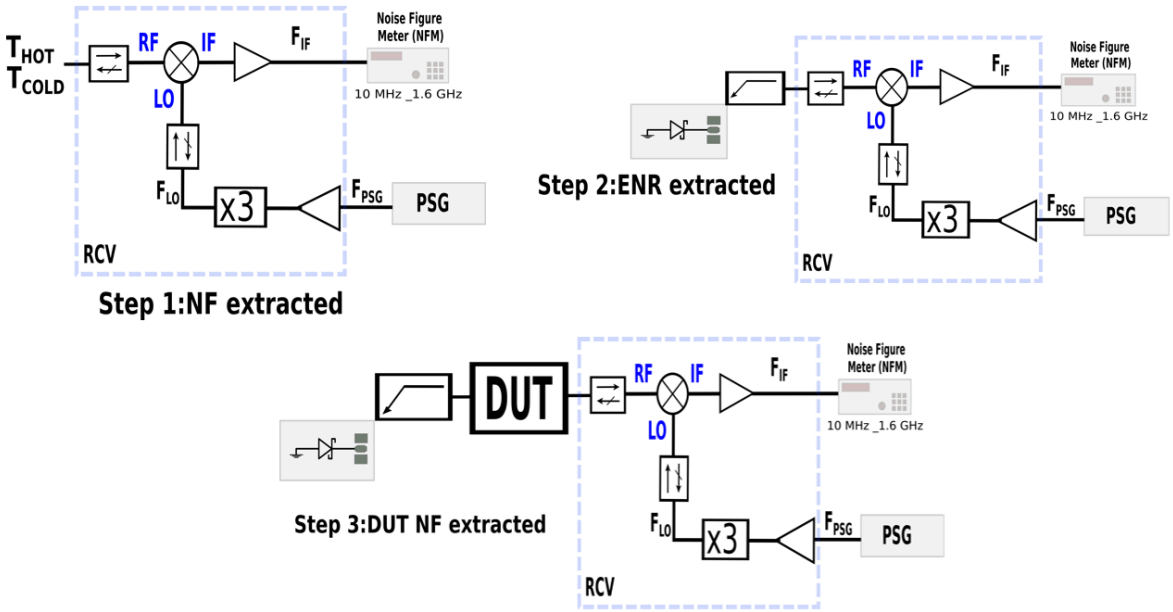


FIG. 5.1: Noise test bench characterization up to 325 GHz.

Beyond this initial proof of concept of using the developed silicon based noise source to perform noise measurements in the frequency range 130-325 GHz, the technological developments needs deeper analysis and design guidelines to be conducted. Therefore, the electrical model of this noise source was developed, and the ENR value was extracted from this model and compared to the measured value, to support the results of the performed experiment. Moreover, the model is developed for several biasing current and structure sizes (section 2.4). The electrical model was developed in the frequency range D.C. to 325 GHz. To validate the electrical model the input impedance of the structure simulated using ADC simulator is compared to the measured input impedance (deduced from S11 parameter), the results are shown in Fig 5.2. A good agreement is noticed between the two curves (simulated and

measured impedance), which validates the methodology and the extraction of the electrical model.

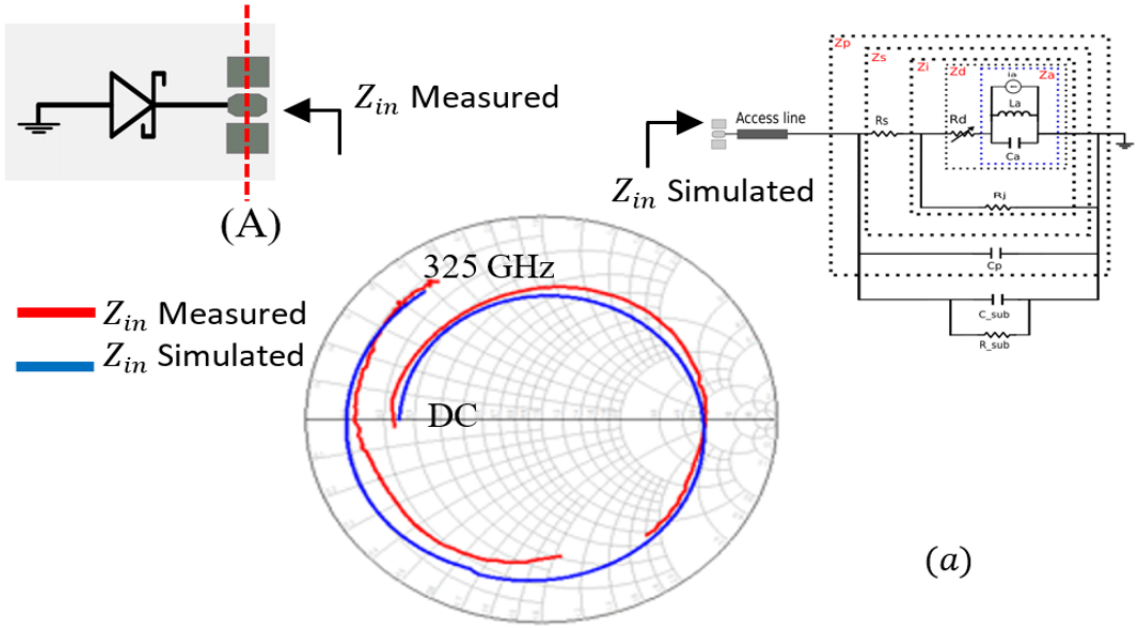


FIG. 5.2: Comparison between the input impedance of the noise source extracted from the measurements and that simulated from the electrical model.

After the development and characterization of the integrated silicon based noise source, a uni-traveling-carrier photo diode (UTC-PD), used as a noise source along with the assembled noise receiver, was characterized and used to perform broadband noise measurements up to 325 GHz. The UTC-PD is packaged in a wave guide module. First the ENR value of this UTC-PD is extracting using the same methodology as for the integrated noise source, where the noise source is connected to the noise receiver and noise power is measured for two stated when the photo diode is in On and OFF respectively. The ENR is then calculated using the Y-method, for several biasing levels (Fig. 3.5). As UTC-PDs are usually used to perform reliable noise measurements in the mmW and sub-THz frequencies, the ENR was compared to that of the integrated diode noise source . The UTC-PD is then used to extract the NF and gain of a packaged LNA in the frequency band 260-325 GHz (Fig. 3.9).

Furthermore, a new technique was developed to use the same device (UTC-PD) in another configuration as a single source to evaluate the intermodulation points of active devices around 300 GHz. Taking advantage of the photo-mixing phenomena to generate two optical signals in the terahertz (THz) frequency range, the UTC-PD was used to convert these optical signals into electrical signals which will then be used to measure the IP3 at the output of the DUT. The advantage is that we are able to use only one wave guide device (UTC-PD) to generate the two signals (two tones) instead of two signal generators; moreover, it provides flexibility to perform

the measurements at millimetre wave (mmW) frequencies (near 300 GHz)(section 3.3). This method was applied to extract the IP3 of an integrated power amplifier (on wafer measurements), and to extract the IP3 and IP5 of the packaged LNA (Off wafer measurements). To the best of our knowledge this is the first realization of using the same source to perform both noise and power measurements around 300 GHz frequency. The experiment block diagram is shown in Fig. 5.3.

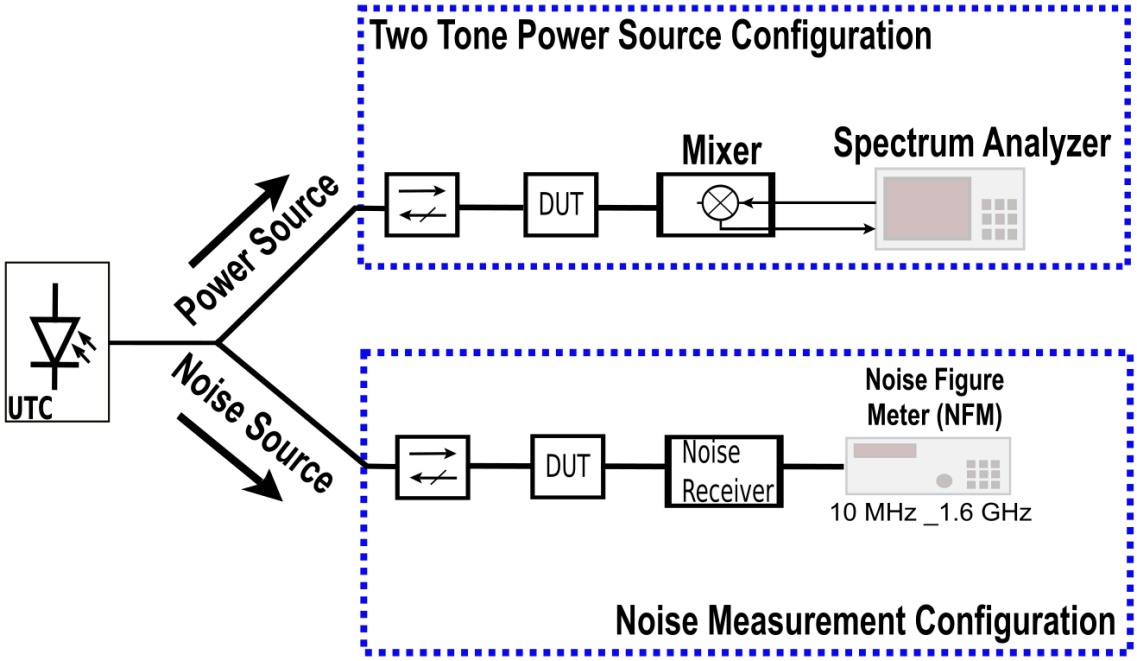


FIG. 5.3: Noise and power measurements using the same UTC-PD source.

A noise test bench is mounted and used to perform noise measurements up to 325 GHz. Both a UTC-PD packaged in a waveguide module and an integrated silicon based diode noise source were used to generate the noise power for the noise measurements, as we saw in chapters 2 and 3. As noticed in Fig. 2.36, the ENR value degrades at higher frequencies, which can make it difficult the maintain the MDS conditions needed at the input of the noise receiver (section 1.5.3). For this purpose, the noise source is usually followed by a LNA in order to amplify the source signal. A LNA structure was designed to be integrated after the noise source (on the same chip) in order to amplify the noise signal, and also to be used as a DUT to perform in-situ noise measurements (above 200 GHz) and extract the NF. The LNA structure was designed using BiCMOS 55 nm technology from STMicroelectronis. Although the LNA did not work as intended, several perspectives are planed in order to develop and design a functional device.

Conclusion and Perspectives

To cope with the increasing demand in the capacity of transmission channels and high communication data rates, systems with large bandwidth, and a high signal to noise ratio (SNR) are required. Therefore high frequency bands are of great interest. The rapid development in device technology made it possible for electronic components to be fabricated with high cut-off frequencies where entirely new applications in the millimeter-wave and Tera-hertz bands become feasible, where wireless communication systems migrate to higher frequencies, improved performances of millimeter-wave radars and sensors is achieved in new implementations. In order to overcome the challenges and constraints when using this portion of the spectrum, a deep understanding of the RF systems is required, which is accomplish by the characterization of electronic systems and devices through S-parameter measurements, power measurements and RF noise measurements.

In this thesis, we discussed the characterization of noise in RF systems and devices at mmW and sub-terahertz frequency bands. One of the main challenges at high frequencies (above 200 GHz) is the equipment availability especially noise sources, used to perform noise measurements. Therefore, a silicon based noise source (a schottky diode structure) was developed using BiCMOS 55 nm technology from ST microelectronics. As a proof of concept, the integrated noise source was used in [33] to perform noise measurements up to 260 GHz. In Chapter 2, the noise source characterization was extended and ENR value was extracted up to 325 GHz. The diode achieved a 20 dB ENR value around 130 GHz, but it decreased to about 4 dB at 325 GHz. In order to detect this low noise power level (which falls below the MDS conditions of the receiver) a pulsed biasing measurement method was used. Using this method, low ENR levels of the noise source can be detected, but the output noise power is not sufficient to perform noise measurements (up to 325 GHz). Therefore, to better understand the diode structure, the electrical small signal model of this noise source was extracted from D.C up to 325 GHz. The model showed a good agreement with measurements over this wide bandwidth. To our knowledge, the validation of the electrical model extraction and characterization of the silicon based noise source up to 325 GHZ (ENR extraction), is new. Future work can be continued, in attempt to develop the noise source (using the developed model) in order to achieve higher ENR values at higher frequencies.

As explained in Chapter 3, UTC-PDs are also used as noise sources to carry

out reliable characterizations in the millimeter wave (mmW) and sub-terahertz frequency range. The ENR value of a UTC-PD (packaged in a waveguide module) was extracted up to 325 GHz, and the UTC-PD was used to perform noise measurements up to this frequency. Moreover, the same device was used in another configuration to perform power measurements around 300 GHz. The UTC-PD was used as a two-tone signal generator to extract the IP3 and IP5 of active devices (integrated MPA and packaged LNA), which is simpler and less costly than using two separate signal generators with frequency multipliers. To our knowledge, this is the first time a single source (the UTC-PD) is used to perform both noise and power measurements (state of the art IP3 extraction around 300 GHz).

Chapter 4 describes the design and characterization of a LNA structure based on HBT transistors using BiCMOS 55 nm technology from ST microelectronics. Integrated noise measurements have been done up to 170 GHz in [6]. The aim is to use this LNA in front of the integrated noise source in order to amplify the noise power, also it can be used as a DUT to perform in-situ noise measurements using the test bench developed in Chapter 2 above 200 GHz. The LNA consists of a two stage cascode structure. S-parameters simulation is done using candence virtuso and the LNA achieved S21 of 13 dB around 220 GHz, then VNA measurements were carried out to measure the S-parameters. The measured S21 parameter of the LNA was about 6 dB at 220 GHz, which does not agree with the simulation. However, despite the gain reduction, several characterization tests were done such as saturation power and oscillation measurements. Moreover, a data-communication experiment was performed at 216 GHz, were the results were successful and highlight the potentiality of using active silicon based stages above 200 GHz. As perspective to this work, analysis and new designs will be fabricated and measured in order to improve the LNA gain, and implement the device in an integrated noise test bench to perform in-situ noise measurements in the mmW frequency range.

As perspective to this work, and after establishing a functioning LNA structure, the device will be used at the input of a detector diode to be used as part of a low power measurement set-up. Moreover, the LNA will be also used in an integrated noise measurement set-up to extract the 4 noise parameters of HBT structures above 200 GHz, which to our knowledge is not yet established. The LNA will be integrated between the output of the integrated noise source and the input of a tuner.

As for the future perspective, the idea is to establish a fully integrated noise test bench to perform in-situ noise measurements at such high frequencies, where all the developed blocks will be integrated within a smart probe module. The probe will contain the integrated noise source, the LNA and a tuner.

List Of Puplications

- **Puplications in International Journals:**

  H.Ghanem et al. "Modeling and Analysis of a Broadband Schottky Diode Noise Source up to 325 GHz based on 55-nm SiGe BiCMOS Technology". In: *IEEE Transactions on Microwave Theory and Techniques 68.6* (2020), pp. 2268 –2277.

  H.Ghanem et al. "300-GHz Intermodulation/Noise Characterization Enabled by a Single THz Photonics Source". In:*IEEE Microwave andWireless Components Letters (MWCL)* (2020), pp. 1–4.

  J.C.Goncalves H.Ghanem et al. "Millimeter-Wave Noise Source Development on SiGe BiCMOS 55 nm Technology for Applications up to 260 GHz". In:*IEEE Transactions on Microwave Theory and Techniques 67.9* (2019).

- **International Communication:**

  H.Ghanem et al. "Silicon Based Diode Noise Source Scaling For Noise Measurement Up To 325 GHz". In: *44th International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)* (2019).

  H.Ghanem et al. "Non-linear analysis of a Broadband Power Amplifier at 300 GHz". In: *European Microwave Conference (EuMC)* (2020) *(Accepted to be puplished)*.

- **National Communication:**

  H.Ghanem et al. "Modélisation d'une Source de Bruit à Diode Schottky en Technologie SiGe BiCMOS 55 nm en Bandes Millimétriques (<300 GHz)". In: *21^{éme} édition des Journées Nationales Microondes (JNM)* (2019).

  H.Ghanem et al. "Schottky Diode Noise Source Modelingand CharacterizationBased on BiCMOS 55 nm Technology". In: *Journées Nationales du Réseau Doctoral en Micro-nanoélectronique (JNRDM)* (2019).

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Development of low noise setup "on" and "off" wafer up to 325 GHz for the performance evaluation of silicon technology

Abstract: Device technology is rapidly improving, making it possible to fabricate electronic components with high cut-off frequencies where entirely new applications in the millimetre-wave and Terahertz band become feasible . This rapid development raise a set of challenges to deal with in order to use this portion of the spectrum successfully. In particular, the advantages of component integration become increasingly important. In order to overcome these challenges a deep understanding of the RF systems is required. To accomplish this, characterization of electronic systems is performed through S-parameter measurements, power measurements and RF noise measurements, which remains a challenge at frequencies above 200 GHz. This thesis addresses the development of a noise set-up to perform noise measurements "off" and "on" wafer to evaluate the noise performance of active devices. A noise receiver is assembled and characterized which enabled noise measurements up to 325 GHz. Moreover, a silicon based noise source developed in the frame work of this project was characterized and the electrical model was developed up to 325 GHz. Furthermore, an optical based source was also studied and used to perform noise and power measurement in the same frequency range. Finally, a LNA was designed and characterized to be used in the developed bench set-up.

Résumé: La technologie des appareils s'améliore rapidement, ce qui permet de fabriquer des composants électroniques avec des fréquences de coupure élevées où des applications entièrement nouvelles dans la bande des ondes millimétriques et Térahertz deviennent réalisables. Ce développement rapide soulève un ensemble de défis à relever pour pouvoir utiliser avec succès cette partie du spectre. En particulier, les avantages de l'intégration de composants deviennent de plus en plus importants. Afin de surmonter ces défis, une compréhension approfondie des systèmes RF est nécessaire. Pour ce faire, la caractérisation des systèmes électroniques est effectuée par des mesures de paramètres S, des mesures de puissance et des mesures de bruit RF, ce qui reste un défi aux fréquences supérieures à 200 GHz. Cette thèse porte sur le développement de différentes techniques expérimentales permettant des mesures de bruit «off» et «on» wafer pour évaluer les performances de bruit des dispositifs actifs. Un récepteur de bruit est tout d'abord assemblé et caractérisé; ce dernier a permis des mesures de bruit jusqu'à 325 GHz. Par ailleurs, une source de bruit à base de silicium développée dans le cadre de ce projet a été caractérisée et le modèle électrique a été validé jusqu'à 325 GHz. De plus, une source optique a également été étudiée et utilisée pour effectuer des mesures de bruit et de puissance dans la même gamme de fréquences. Enfin, un LNA a été conçu et caractérisé pour être utilisé dans la configuration du banc développée.