Theoretical and experimental evaluation of the Integrated gate-commutated thyristor (IGCT) as a switch for Modular Multi Level Converters (MMC)

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Theoretical and experimental evaluation of the Integrated gate-commutated thyristor (IGCT) as a switch for Modular Multi Level Converters (MMC)

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Abstract

This manuscript investigates the potential of Integrated Gate-Commutated Thyristors (IGCT) for Modular Multi-Level Converters (MMC). After a theoretical analysis of the advantages of IGCTs regarding losses, we investigate their switching operation experimentally. In particular, we focus on di/dt limiting inductance and RCD-clamp reduction/suppression using plastic module silicon (Si) fast recovery diodes and silicon carbide (SiC) diodes in an MMC submodule. This study aims to explore improvements for the MMC, focusing on using different semiconductors in the MMC submodule.

This Ph.D. manuscript contains:

- An analysis of existing HVDC MMC Submodules and their technologies.
- A review on the IGCT: semiconductor structure, types and features.
- An assessment of the interest of the IGCT in HVDC MMC Submodules and losses comparison with IGBTs, using MMC-specific figures-of-merit created in this thesis.
- An assessment of the works on limiting di/dt inductor size reduction.
- A double pulse test design with specific structure imitating an MMC submodule.
- A review and an analysis of the PiN diode failure modes.
- Double pulse tests with fast recovery diode in plastic module with successful attempts to reduce and suppress the limiting di/dt inductor (up to 2400V/1800A and 2000V/2400A).
- The packaging of High-Voltage (10kV) High-Current (50A) SiC PiN diode dies (1cm^2), test with IGCT in the same setup, with successful attempts to reduce and suppress the limiting di/dt inductor (up to 2400V/100A and 2000V/150A), and analysis of the specificities of the SiC diode in that setup.

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Résumé

Ce manuscrit étudie le potentiel des thyristors de type IGCT pour les convertisseurs multi-niveaux modulaires (MMC). Après une analyse théorique des avantages des IGCTs au regard de leurs niveaux de pertes, nous étudions leur fonctionnement en commutation de manière expérimentale. En particulier, nous nous concentrons sur la réduction/suppression de l'inductance de limitation di/dt pour IGCTs et du clamp RCD en utilisant des diodes rapides en silicium (Si) et des diodes en carbure de silicium (SiC) dans les sous-modules MMC. Cette étude vise à explorer les pistes d'amélioration pour le MMC, en se concentrant sur l'utilisation de différents semi-conducteurs dans le sous-module MMC.

Ce manuscrit de thèse de doctorat contient :

- Une analyse des sous-modules de MMC HVDC existants.
- Une revue de l'IGCT : structure du semi-conducteur, types et caractéristiques.
- Une évaluation de l'intérêt des IGCTs dans les sous-modules MMC HVDC et comparaison des pertes avec les IGBT, en utilisant des facteurs de mérite spécifiques aux MMC créés dans cette thèse.
- Une évaluation des travaux sur la réduction de la taille des inductances limitant le di/dt.
- Un design de banc d'essais test à double pulse avec une structure spécifique imitant un sous-module MMC.
- Une revue et une analyse des modes de défaillance des diodes PiN.
- Des tests en double pulse avec diode à récupération rapide dans un module plastique pour tenter de réduire et supprimer l'inductance limitant le di/dt.
- Packaging de puces de diodes SiC PiN à haute tension et courant élevé, test avec IGCT dans le même montage,pour tenter de réduire et supprimer l'inductance limite di/dt, et analyser les spécificités de la diode SiC dans ce montage.

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Chapter 1

Review of MMC-submodule technology

In this chapter, the MMC submodule technology will be assessed. In a first section, the MMC and its design will be presented before going into the details of the submodules themselves (components and design rules) in a second section, and concluding with a review of the existing submodule realisations (industrial and litterature submodules) in a third section.

The goal of this chapter is to expose the submodule design rules and their typical features and values.

1.1 Introduction to the Modular Multilevel Converter Topology and its Submodule

1.1.1 Voltage Source Converters

The Modular Multilevel Converter (MMC) is a Voltage Source Converter (VSC) developed and used for Medium or High Voltage Direct Current (MVDC or HVDC) applications. This is a reversible, AC/DC Converter. A simple type of VSC is the two-level converter and its understanding helps to identify the advantages of the Modular Multilevel Converter.

1.1.1.1 The two-level converter

The two-level converter is presented in fig. 1.1a, and the corresponding waveforms on the AC side are given in fig. 1.1b. Because only 2 levels of voltage can be applied on each terminal of the AC side, the AC/DC conversion relies on high-frequency switching, with for example the Pulse Width Modulation method – using a sinusoidal reference signal, and the filtering of high-frequencies. This strategy has its main drawbacks: high switching frequency implies large switching losses, and requires filtering to remove the high frequency harmonics. Because the power semiconductor devices have a limited voltage ratings – up to 10kV, it is necessary to connect many of them in series (as illustrated in figure 1.1a) to sustain the MVDC or HVDC

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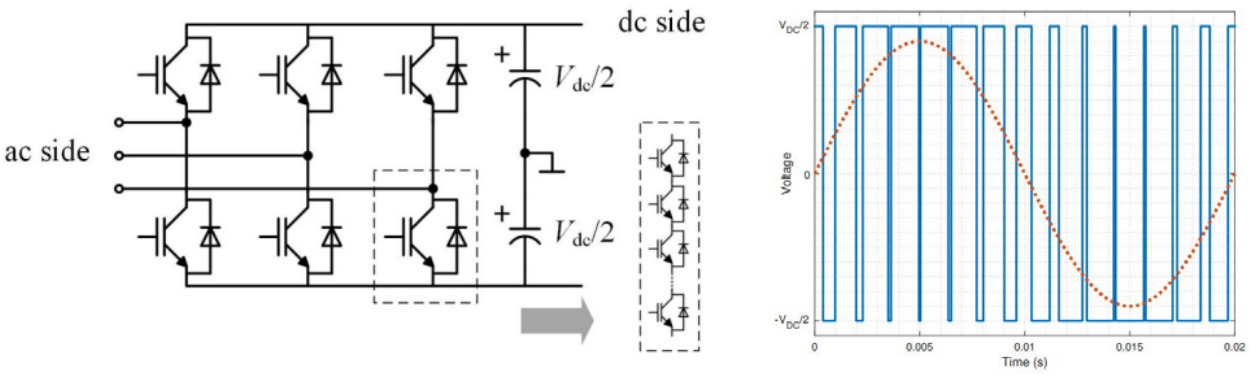

(a) Circuit Diagram [105], each arm is composed of series-connected switches.

(b) Typical voltage waveform of a 2-level converter [50]

Figure 1.1: Circuit diagram and typical voltage waveform of a 2-level converter.

DC voltage – from tens of kVs to hundreds of kV. Such connection is complex to ensure balanced voltage distribution as well as simultaneous switching of all the semiconductor components.

1.1.1.2 The Modular Multilevel Converter

The Modular Multilevel Converter (fig. 1.2a) is based on submodules, its elementary unit. Formed by power semiconductors (switches and diodes) and a capacitor, a submodule can be seen as a small voltage source, that can be inserted or not (depending on the switching sequence and the current sign along the submodules). This structure permits to function as a rectifier or an inverter. The number of submodules can be high – up to hundreds, allowing a good sinusoidal waveform to be generated (see figure 1.2b), even without filtering. The quality of the signal is measured with the total harmonic distortion (THD). The MMC topology is also easily scalable: for a given submodule, different MMCs can be built (a 100 kV MMC and a 400 kV MMC can be built with the same submodule). The way the converter works, the switching frequency of each individual submodule is lower than the one for a two-level converter, and so switching losses are lower as well. The switching frequency of a submodule is generally between 100Hz and 300Hz. It has also a good failure management, a larger number of submodules than the minimum number needed is used inside an MMC to have redundancy in the converter. When a submodule fails, it is bypassed and this permits the converter to continue working.

Operation and main parameters Submodules are inserted or removed from the circuit to obtain the desired voltage waveform, the capacitor acting like a voltage source. While inserted, capacitors either charge or discharge, depending on the sign of the current. The control of the MMC is aiming to generate the desired voltage waveform but is also aiming to control the state of charge of the capacitors. The typical submodule selection process is divided into two parts: first the number of submodules that have to be inserted to generate the voltage is calculated, and then a balancing control algorithm (BCA) selects which submodule will be inserted or removed – depending on the capacitor voltage level and the voltage limits that are set. This algorithm is very important because it influences the losses of the whole converter, the voltage ripple of the capacitors, the quality of the signal... Typically, this kind of algorithm ranks the

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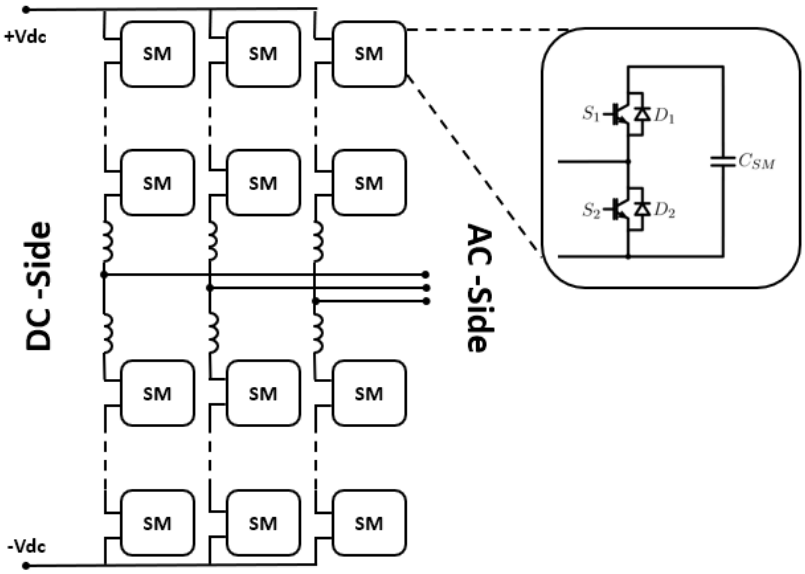
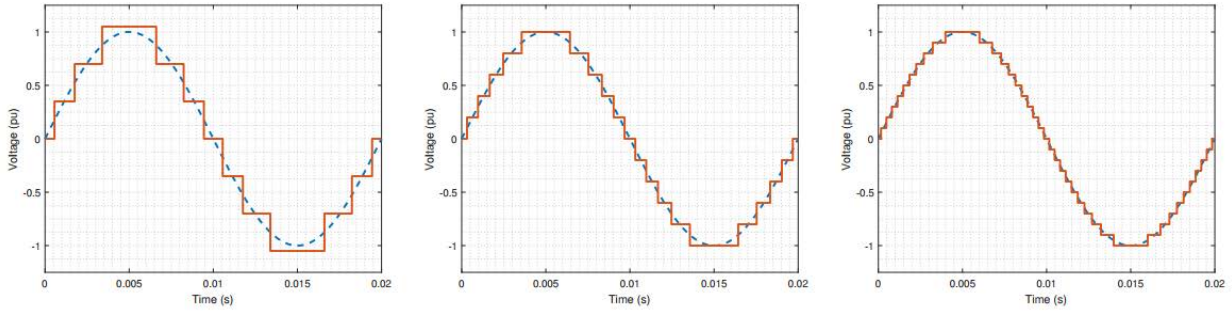


(a) Circuit Diagram of the modular multilevel converter and if one of its submodules (SM)



(b) Typical voltage waveform of an MMC with different number of submodule per arm [50], from the left to the right, larger number of submodules.

Figure 1.2: Circuit Diagram and typical voltage waveform of an MMC

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submodules according to the voltage levels of their capacitor, and depending on the voltage level and the current direction, it chooses which capacitor has to be inserted or removed. Allowing a large voltage swing in the capacitors lowers the losses in the submodule (because the switching is less frequent). But for the same capacitor, a higher voltage ripple will accelerate its ageing. This would force the submodule manufacturer to oversize the capacitor, leading to extra cost and extra volume.

The MMC is converting power from DC to AC (or the opposite). Its operation depends on the voltages on the AC and DC sides, and the transmitted powers. It must also create or absorb reactive power. The operation point can be defined as a combination of the modulation factor (see equation (1.2)) – the ratio between AC and DC-voltage, the power factor on the AC-side, and the transmitted active power.

In the hypotheses of a sinusoidal signal, the voltage across an arm is:

$$V_{arm}(t) = \frac{V_{dc}}{2} - V_{ac}.cos(\omega t + \phi) \tag{1.1}$$

$$= \frac{V_{dc}}{2} - \frac{V_{dc}}{2}.m.cos(\omega t + \phi) \tag{1.2}$$

With m, the modulation factor defined as $\frac{2V_{ac}}{V_{dc}}$, with V_{ac} the amplitude of the AC-voltage, V_{dc} the DC-voltage, ω the pulsation, ϕ the power factor.

Examples of MMCs implementations for HVDC A list of HVDC projects based on MMCs can be found in Table 1.1. This list describes the different ratings (voltages, power) as well as the submodule topologies (see 1.1.2.2), the applications (GC stands for Grid Connection, OWF for offshore wind farm) and the manufacturers. This table is based on manufacturer documentation [1, 4, 32, 99], publications and presentations listing the projects [70, 53, 38]. It is, of course, non-exhaustive.

1.1.2 The MMC Submodule

1.1.2.1 Structure of an MMC Submodule

The different parts of a typical submodule, their role and characteristics are described below [24] (each of theses parts is then described in details in section 1.2). The table 1.2 and the figure 1.3 offer a quick overview of those parts.

- The **power module** houses the power switches with their anti-parallel diodes. This power module is the main source of losses in the MMC and one of the most expensive parts. The most used switch for HVDC MMCs is the silicon (Si) IGBT, due to a combination of its high voltage and high current ratings and its ease of control. Silicon carbide (SiC) MOSFETs are used in low current MMC (such as MVDC MMCs). IGCT, a component

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Table 1.1: Table listing existing HVDC Projects based on MMCs, based on [4, 99, 32, 10]

Project - date	DC (kV)	AC (kV)	Power (MW)	Topology	Application	Manufacturer
TransBay Cable - 2010	±200	115/230	400	HB	GC	Siemens
ULTRANET - 2020	±380	400	2000	FB	GC	Siemens
SylWin1 - 2015	±320	155/300/380	864	HB	OWS	Siemens
INELFE - 2015	±320	400	2×1000	HB	GC	Siemens
Caithness Moray - 2018	±320	230/400	1200	-	GC	ABB
Skagerrak 4 - 2014	500	400	700	-	GC	ABB
DolWin 1 - 2015	±320	155/380	800	-	OWS	ABB
DolWin 2 - 2017	±320	155/380	900	-	OWS	ABB
DolWin 3 - 2018	±320	380	900	-	OWS	GE
SydVästlänken (South-West Link) - 2016	±300	400	2×600	-	GC	GE
Nan'ao Three-terminals - 2013	±160	110	T1:200 T2:100 T3:50	T1: HB	GC	T1:RXPE T2:XiDian T3:NanRui
Zhoushan Five-terminals - 2014	±200	T1-2:220 T3-4-5:110	T1:400 T2:300 T3-4-5:100	-	GC	-

of the thyristor family, is being studied as a good alternative of the IGBT in HVDC MMC due to its lower losses and will be investigated in details in this thesis memoir. The different semiconductor switches are further developed in section 1.2.1.

- The **capacitor** behaves in the MMC like a voltage source. All high power MMC sub-modules reported use of MPPF (Metallized PolyPropylene Film) capacitors because of their self-healing property, stability and cost. In [45], the energy storage requirements are calculated for a 4.5MVA MMC at 21kJ/MVA. The same calculation was done in [75], with a 20 MVA MMC and a 600 MVA MMC, and a value of 39kJ/MVA was found. As it can be guessed, these values depend on the MMC specifications, on the control etc. In [105], commercialised MPPF capacitors have been listed and studied. For the MMC ratings of [45, 75], the capacitor energy density would be around 350 J/L according to [105]. It would mean a capacitor volume of 60L/MVA or 111.4L/MVA, that is a total capacitor volume of 270L for the 4.5MVA MMC [45] and 66.8m^3 for the 600MVA MMC of [75]. This represents one of the main source of volume of the converter. The review of capacitor technologies and dimensioning techniques are developed in section 1.2.2.

- The **busbar** is the electrical connexion between the elements of the submodule. It is subject to dielectric, thermal and mechanical stresses. It is further developed in section 1.2.3.

- The **control electronics** manage the interface with the main controller (fibre optic link) of the MMC converter: they receive switching orders for the IGBTs, and send status

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Table 1.2: Table presenting an overview of the different parts of a submodule in an MMC.

Part	**Role**	**General Design Rules and Principles**
Power Module	Inserts or removes the capacitor	Generate low losses, Able to withstand voltage, current, frequency constraints
Capacitor	Voltage Source/ Energy Storage	Energy requirement, RMS Current, Voltage
Busbars	Electrical Connexion	Low stray inductance, low stray capacitance, low resistance
Protection Circuits and Bypass Components	Protect the SM or the MMC	Short-Circuit, overvoltages, and other defined failure scenarii
Auxiliary Circuits	Acquire measures, Control the SM, Power Supply	High reliability (regarding EMC), Isolation
Cooling System	Cools mainly the semiconductors	Cooling power and insulation requirements
Mechanical Structure	Holds the SM parts together, permit valve assembly	Applied efforts, insulation requirements, possible to assemble

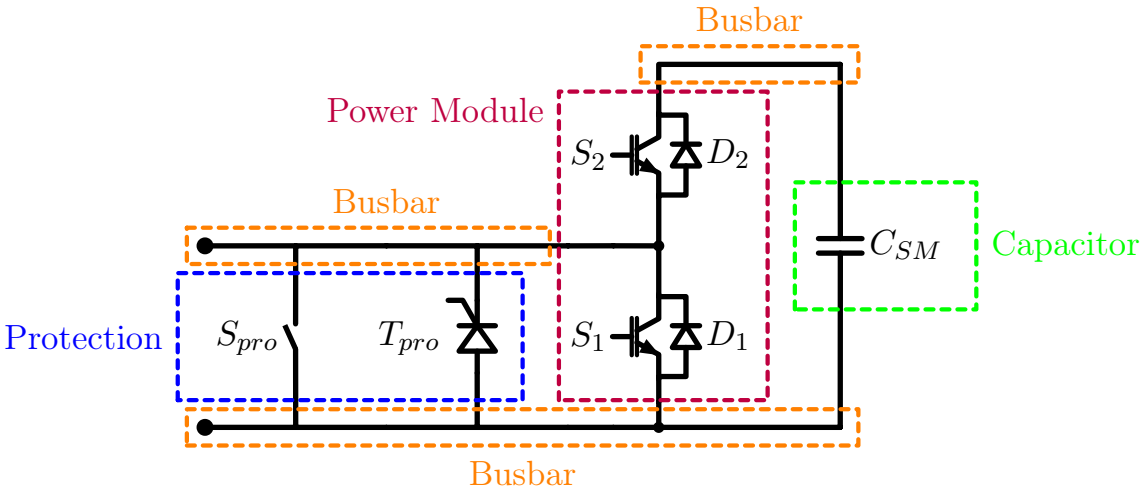

Figure 1.3: Typical Half-Bridge submodule structure.

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feedback, as well as measurements of the capacitor voltage and of the submodule current. It also drives the protection circuits and bypass systems. This control system requires a low voltage power supply (with an external or internal power source). It is often a complex printed circuit board, with an important number of electronic components. This element is essential and is working in a harsh electromagnetic environment. Auxiliary circuits are developed in section 1.2.4.

- **Bypass components** are necessary for mainly two reasons: a permanent and a temporary bypass. The permanent bypass is activated in case of fault in a submodule. It can be done by a mechanical switch or a switch in short-circuit – a fail-to-short system. A temporary bypass can be needed either to protect the diodes from overcurrents or to help a mechanical switch, often too slow for the bypassing operation. Other protection circuits can be found and they vary from one submodule to another. Bypass components and other protection circuits are developed in section 1.2.5.

- A **cooling system** is designed to evacuate the losses, mostly from the power semiconductors, the main source of losses. This is done with liquid (often deionised water) or air cooling, with forced or natural convection. More details are given in section 1.2.6.

- The **mechanical structure** is holding together the different parts of the submodule. It must take into account the weight, but also that the submodule can be easily assembled, that different parts have different voltages and must be isolated from one another (insulation function, see section 1.1.5).

1.1.2.2 Submodule Topologies

Many submodule circuits topologies have been introduced in the scientific literature. At the time this thesis is written, only two of them (the so-called "half-bridge" and "full-bridge") actually appear to be produced industrially for HVDC. They are presented in the next section. The remaining topologies may offer specific advantages, but their development is much less advanced.

Half-Bridge (HB) The half-bridge structure (displayed in figure 1.4a) is the most common topology for MMC submodules. Its simplicity – only 2 switches – makes it easy to study, and limits the cost of the semiconductors. This topology has been intensively investigated [107, 56, 28, 16]. MMC converters based on Half-Bridge submodules have been designed and built by companies such as General Electric, Siemens, ABB, Mitsubishi, or Hyosung [12].

The Half-Bridge is the reference topology for losses as current flows through only one semiconductor switch at any given time, resulting in low conduction losses. An example of losses breakdown for half-bridge submodules (as well as for other topologies introduced below) can be found in figure 1.5.

The main problem with that topology is that it is unable to block a “pole to pole” DC short-circuit. Such short-circuit condition is described in the section about overstress situations (1.1.4). It implies that the MMC must be equipped with an AC or DC circuit breaker and that the anti-parallel diode of the switches must sustain large surge currents, or be assisted by a bypass thyristor.

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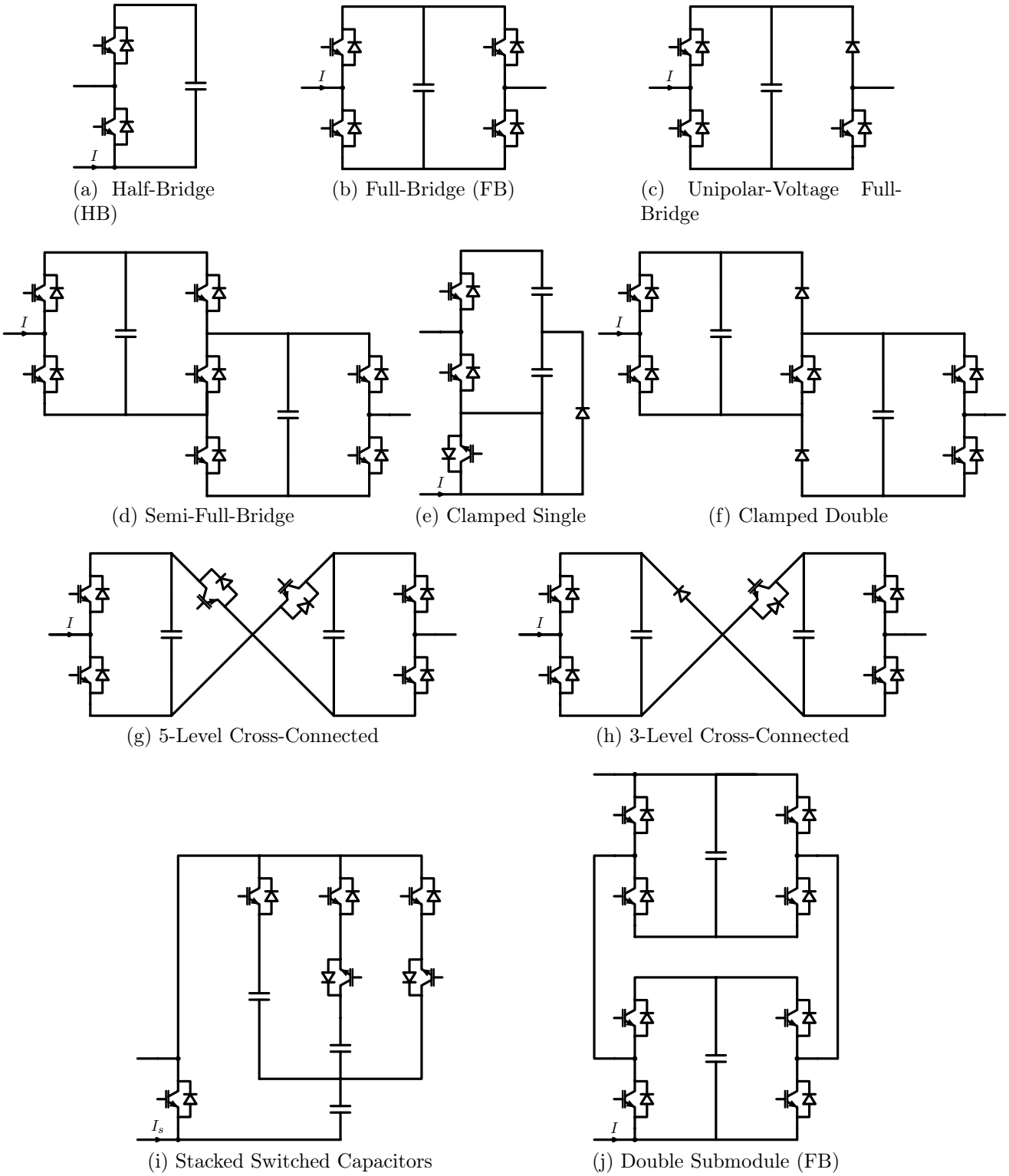

(a) Half-Bridge (HB)

(b) Full-Bridge (FB)

(c) Unipolar-Voltage Full-Bridge

(d) Semi-Full-Bridge

(e) Clamped Single

(f) Clamped Double

(g) 5-Level Cross-Connected

(h) 3-Level Cross-Connected

(i) Stacked Switched Capacitors

(j) Double Submodule (FB)

Figure 1.4: Submodule topologies, see the corresponding table 1.3.

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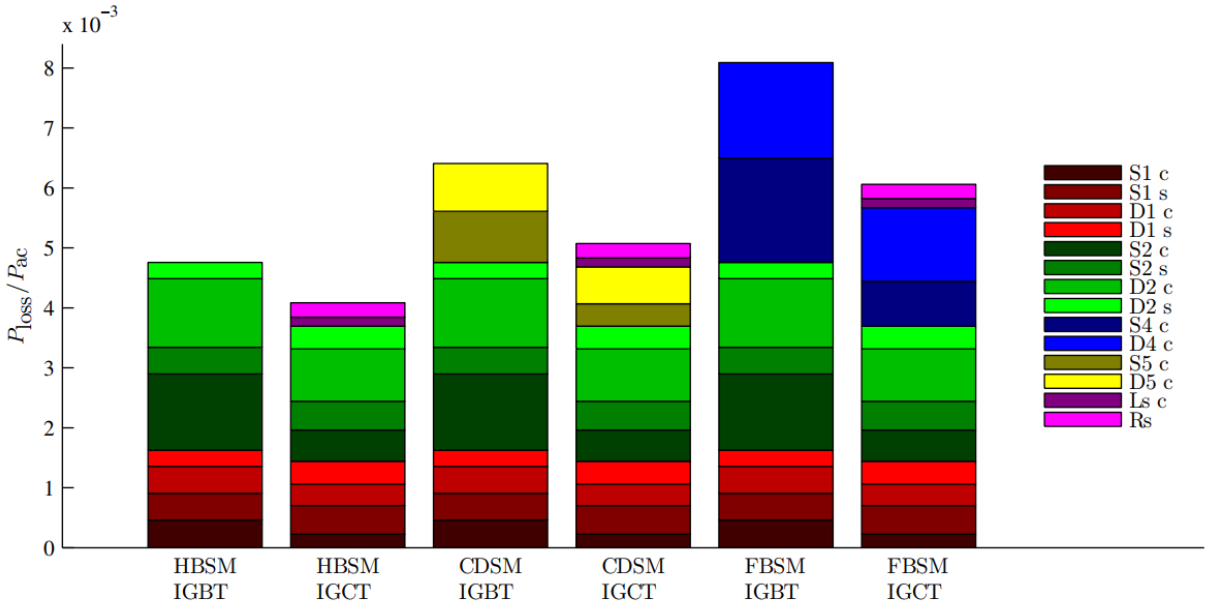

Figure 1.5: Example of losses breakdown for HB, FB and Double clamped submodule topologies using IGBT or IGCT switches, extracted from [76]

Another limitation of this topology is its lack of flexibility. Indeed, the modulation factor of the MMC cannot exceed 1, and in practice it is mostly used around 0.8 [68].

Full-Bridge (FB) The full-bridge topology (also called H-bridge, displayed in figure 1.4b) is composed of 4 switches. This makes this topology more expensive, more complex in terms of control. It also has more conduction losses (Fig. 1.5) [76, 68], as current has to flow through two switches connected in series at any given time. The two main advantages of this topology are: its capability of handling a DC-side short circuit (because the capacitors of the submodules are on the path of the short-circuit current), and a modulation factor higher than 1 (because negative voltage can be inserted).

To mitigate the drawbacks of the full bridge topology, a mixed MMC (i.e. including some FB submodules and some HB submodules) can be found in the literature. In [58], it is found that to handle the DC-side short-circuit, around 80 % FB submodules are needed, so 20 % of the submodules can have a HB topology. However, this kind of combination will not be investigated further in this thesis, because we will focus on the conception of one submodule – HB, FB or other topology – and not on the entire converter.

Other topologies and Comparison A summary of the different topologies which can be found in the literature is presented in table 1.3 and figure 1.4. These submodule topologies are only listed here for reference, and will not be discussed further. Only the HB and FB topologies appear to have been used in full-scale demonstrations.

As written in [69, 98], the half-bridge submodule is the topology with the lowest losses and the lowest cost – if we only take the price of the power semiconductors into account. In addition, most other topologies have only been described in publications using computer simulation or

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Table 1.3: Comparison of the different submodule topologies, the circuits are displayed in Fig. 1.4

SM Topology	Advantages	Drawbacks
Half-Bridge [69, 68, 98]	Simple, low losses, well-known and studied, few semiconductors	Lack of flexibility, no negative voltage possible, $k \leq 1$, DC-short not controllable
Full-Bridge [69, 68, 98]	Negative voltage possible, possibility of $k > 1$, DC-short controllable	Lots of semiconductors, high losses
Unipolar-Voltage FB [98]	DC-short controllable	No negative voltage, higher losses than HB (conduction only)
Semi-Full-Bridge [44, 69, 98]	Reducing Capacitance a lot (by reducing the ripple), $k > 1$ possible, two switches rated half of the other ones	losses and perturbation due to current going from one capacitor to another
Clamped Single [98]	DC-short controllable, some device with lower blocking voltage	Higher losses than HB
Clamped Double [98, 69]	DC-short controllable, Reduced arm inductance	Slightly higher losses than HB, complex mechanical design, $k \leq 1$
Five-Level Cross-Connected [69, 98]	Only 25 percent of the submodules to be efficient (rest : HB), negative voltage, DC-short controllable	2 different submodule topologies required in the converter
Three-Level Cross-Connected [98]	Similar to 5-level	Similar to 5-level
Stacked Switched Capacitors [106]	Reducing the ripple and then the capacitors size, control same as HB	HB with added switches, more losses
Double Submodule (FB) [98]	Same as for FB, plus reduced capacitance	Same as FB, may be difficult to assemble

small-scale demonstrators. Meanwhile, the half-bridge topology is already implemented in real industrial applications. Full-bridge submodules may also be of interest, but in the current study (which focuses on the submodule design) they would only add costs to a demonstrator, without actually resulting in fundamental changes in the design procedure. As a consequence, in this thesis, we will focus on the Half-Bridge submodule topology.

1.1.3 MMC Definitions, Design, and existing MMCs

1.1.3.1 Some MMC Definitions

The MMC is divided into three **legs** and each leg is divided into two **arms** (six arms in total), as it can be seen in figure 1.6. The term **valve** is used to describe an association in series of parts of a converter (in a thyristor valve this is a series-connection of thyristor, in an MMC submodules in series). In thyristor-based converters, it corresponds to an entire thyristors

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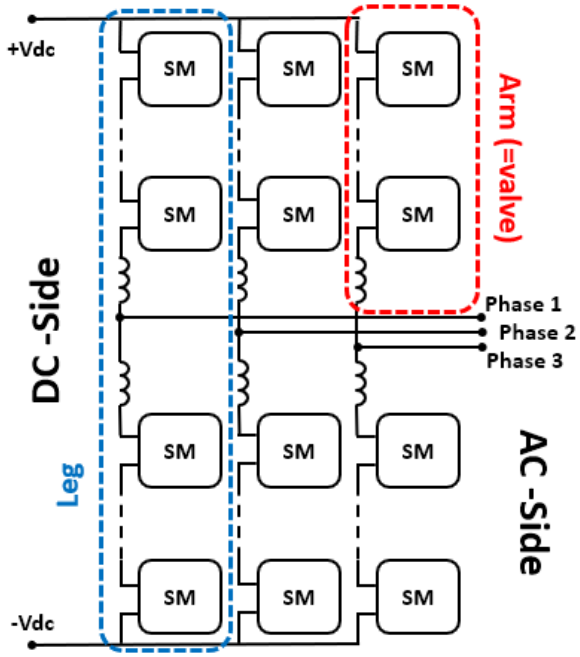

Figure 1.6: Definitions of arm, leg and valve in an MMC.

association conduction or blocking at the same time. In MMCs, it corresponds to an arm. The valve term is useful for technical issues covered in all types of converters (such as insulation coordination, in section 1.1.5).

1.1.3.2 Considerations for the design of an MMC

An MMC must match a defined set of specifications. The first type of specifications is imposed by the project (voltage, current, power levels) and its physical location (volume, footprint); the second type of specifications is imposed by the network and its transmission system operators (TSO).

Specifications imposed by the project and its location One type of constraints is due to the location of the converter inside the electrical grid. This can impose the active power, the AC and DC voltages and therefore the current. Paralleling of converters can be achieved to reach the wanted current and power. But the AC voltage can be adapted with a transformer between the MMC and the AC-grid. Another type of constraint is due to the physical location of the converter. If the converter is located in the ocean or the sea, the weight and volume of the converter are critical.

Specifications imposed by the network When designing an MMC converter, some constraints are imposed by the local electrical network characteristics, its local TSO and its rules. For example, the European Union gives rules for voltage and reactive power ratings (allowed and imposed variations) [113].The voltage ratings are described in the article 18 and annex III of [113] and the reactive power capability is described in the article 20 and annex IV of the

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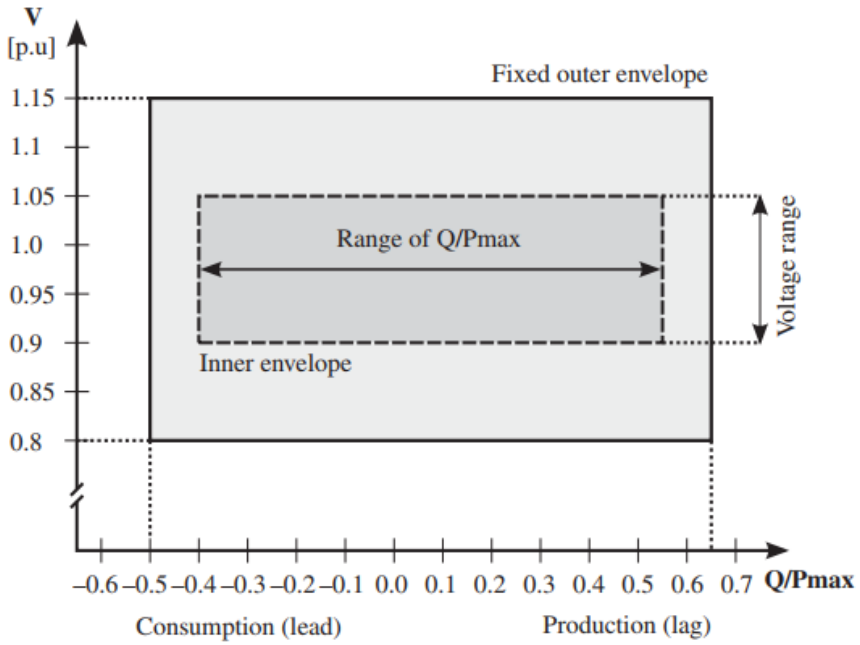

Figure 1.7: Requirements on reactive support proposed by ENTSO-E, extracted from [98]

same regulation document. The pole-to-pole voltage can vary from 0.85 to 1.15 p.u. . But it depends on the region of Europe and some operating points (mainly voltages between 1.118 and 1.15 p.u.) have to be held for a limited amount of time only.

The reactive power capability is defined with a profile: a V-Q/Pmax profile with P the active power and Q the reactive power. An example of such a profile is given in figure 1.7, defined by the ENTSO-E (standing for European Network of Transmission System Operators). The regulation document of the European Union gives the outer envelope and the local TSO can draw any wanted profile inside of the outer envelope, not just rectangular shapes. Values for the inner region is available in the regulation document in the annex IV.

The frequency ranges are also defined in [113], and each range is associated to a time during which the converter still has to work. The converter has to work for an unlimited time between 49 and 51 Hz. The other ranges have to be specified by each TSO.

Global design parameters for the MMC Then an optimisation has to be done, mainly driven by global cost of the project, taking into account the efficiency and the overall cost of the station. If the submodule has to be designed from scratch, a submodule voltage is chosen. But most often, the submodule is chosen among available submodules in the market or the MMC building company. The inductance and the transformer have to be designed as well. The dimensioning process of the submodule is described in section 1.2.

The safety margin on the number of submodule is driven by the scheduled maintenance frequency (every 2 years typically), and seems to be around 5 to 10 % extra-modules for redundancy.

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1.1.4 Overstress and Dimensioning Situations

1.1.4.1 Identified Cases of Overstress

There are plenty of overstress cases. They correspond to external or internal issues. It can be overvoltages, overcurrents, bad commutation of the switches, destruction of a part of the submodule (capacitor, switch...). The main problems that must be considered at design stage (as they affect the dimensioning of the submodule) are identified as the short-circuits, mainly on the DC-side, and the cosmic rays (which dictate the semiconductor switches operating voltage).

1.1.4.2 Overcurrents

The different overcurrent cases that impact the MMC are developed in [131]. They are due either to short-circuits in the submodule with the erroneous firing of an IGBT for example, or to short-circuits outside of the submodule (AC-side short-circuit, DC-side short-circuit, short-circuit inside an MMC arm).

Internal short-circuits Two types of internal short-circuits are listed in [131]. The first is one IGBT going from off-state to short-circuit (Hard-Switch Fault) due to erroneous firing or due to the failure into short-circuit of the other IGBT. The other one is the IGBT going from on-state to short-circuit due to the break down of the IGBT or the erroneous firing of the other IGBT. This last one is called Fault under load (FUL) in [131]. Such internal short circuit causes the charged capacitance to be short-circuited by closing both IGBTs. [131] finds that this kind of fault causes fault current levels rising by 5kA to 20kA in a few µs – depending on the short-circuit situation inside the SM – for a 2.2 kV charged capacitor (value of capacitance none disclosed).

DC-side Short-Circuits Two types of DC-side short-circuits exist: the pole-to-ground short circuit and the pole-to-pole short-circuit. As their names indicate, the pole-to-ground is a short-circuit between one of the DC side terminal and the ground and the pole-to-pole between the two terminals of the DC side of the converter. A pole on the DC side is the negative or positive voltage terminal (-Vdc or +Vdc in figure 1.6).

According to [98], the most severe possible short-circuit for the components of the submodule is the DC-side short-circuit. It is hard to provide a probability or frequency of fault for these short-circuits, because they are specific to the converter, the cables and the grid around the converter. But the risk is high enough for the semiconductors in the submodules to consider installing a protection system. When the pole-to-pole fault occurs, the voltage on the DC side drops below the voltage on the AC side, allowing current to flow through the antiparallel diodes of the semiconductor switches in a HB submodule. Three main strategies exist to interrupt the short-circuit current [134]: having an AC-side breaker, having a DC-side breaker or having a topology able to withstand the short-circuit (i.e. a topology in which submodules can block current in both directions, such as a full-bridge). For topologies with uni-directional current control (such as the half-bridge), a bypass thyristor can be connected in parallel with the

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diodes, and triggered during the short-circuit. Such system allows to temporarily sustain the surge current (before the circuit breakers open), without using very large diodes which would increase switching losses due to their large recovery charge.

When a DC-side short-circuit happens, for a topology with uni-directional current control and an AC-side or DC-side breaker, three different stages occur [29]. The first one is the discharge of the capacitors until the MMC is blocked (all switches open). The second one is the AC-side current becoming the source of the short-circuit current. The third starts once the AC or DC breaker has been triggered. In [98], it is said that there is an additional phase, during which the cable discharges (between the first and the second one). This can lead to really high surge current in the arm (from 8 kA to 21 kA for a nominal current of 1 or 2 kA). This current flows through the antiparallel diodes after the MMC is blocked. The stress is evaluated over the duration of the event (I^2t is the evaluated variable in that case). The duration of the short-circuit current (phase 1 and 2) is then very important: the longer it takes to trigger protection systems and breakers, the higher the fault current is going to be. [134] concludes that the AC-breaker strategy is the readiest technology but it is also the strategy which results in the highest fault current and the largest fault duration. A test method can be found in [132]. Also according to [134], the best solution to clear a DC-side short-circuit is a DC circuit breaker, because it has a really short response time (DC-breakers, for example from ABB, operate in 5 ms [29, 134]). Furthermore, clearing the short circuit only involves opening the DC breaker, and there is no need to block all IGBTs in the converter [134].

To detect them, a simple method would be to use a predefined threshold current like described in [98, 132]. When that threshold current is overcome, the order to open all switches and to close the protective thyristors is sent.

AC-side short-circuit Here will be considered the fault of one AC-side phase-to-ground short-circuit, between the secondary side of the converter transformer and the converter. [98] describes that in such case, the shorted phase descreases to zero and the other two healthy phases see their voltage increasing to $\sqrt{3}$ times their nominal voltage. This is considered with a star/delta transformer (delta on the converter side). This kind of short-circuits is dealt with by having sufficient insulation for this overvoltage and by having surge arresters in the converter. A very important point is that with an MMC, unlike a 2-levels VSC, there is no grounded middle point on the DC-side, and therefore, there is no path for current surges (like the ones observed in DC-side short-circuit). So during that kind of failure event, the semiconductors in the submodules are not stressed, even with Half-Bridge submodules.

1.1.4.3 Overvoltages

Overvoltages types that can be encountered in MMC converters, are listed in IEC-60071. The most common types are the switching impulse and the lightning impulse. The first one is a slow-front transient overvoltage, while the second one is a fast-front overvoltage. These standard overvoltage waveshapes are defined in IEC 60071 and these are illustrated in Fig. 1.8. Their time parameters are described in Tab. 1.4, in which you can find the values of standard tests (standard value) and their typical values. T_p or T_1 are the time values when the overvoltage is at its maximum while T_2 is the value when the voltage has decreased back to half the overvoltage.

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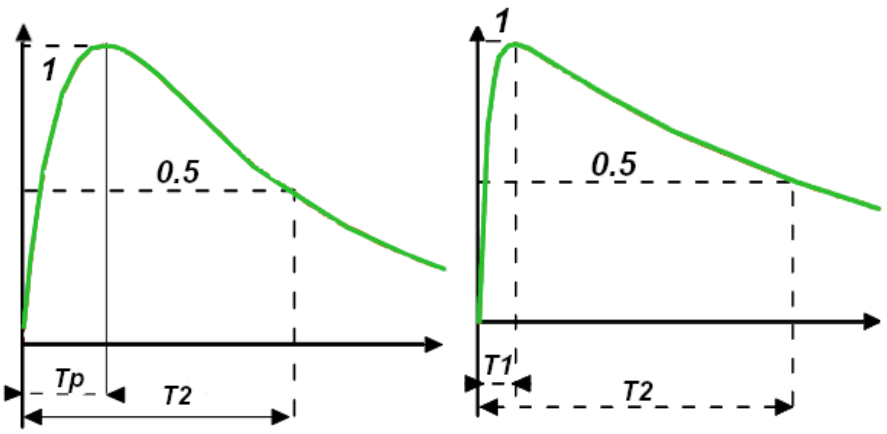

(a) Slow front Overvoltage (Switching) (b) Fast-Front Overvoltage (Lightning)

Figure 1.8: Standard overvoltage waveforms, normalized scale: 1.0 is the maximum overvoltage, and 0.5 is half of the overvoltage. Source: IEC60071-1.

Table 1.4: Waveform parameters of overvoltages, extracted from IEC 60071-1.

Time	T_p or T_1		T_2	
	Standard	Typical	Standard	Typical
Switching Impulse (Slow-Front)	250µs	20µs$<T_p<$500µs	2500µs	$T_2<$20ms
Lightning Impulse (Fast-Front)	1.2µs	0.1µs$<T_1<$20µs	50µs	$T_2<$300µs

Switching impulses can be a consequence of a breaker opening, a capacitive switching, a load rejection, a phase to earth fault or a filter energisation. Lightning impulses can be created with direct lightning strikes or back flashovers.

These overvoltages define the insulation co-ordination of the converter: insulation material, insulation level, distances between parts, protection systems. Surge arresters are generally added inside the circuit of the MMC to protect the MMC from overvoltages. [98]

1.1.4.4 Cosmic Rays

The cosmic rays have a big impact on the lifetime of the semiconductors and are therefore important to understand and to model. The cosmic rays – high-energy particles – interact in the atmosphere and generate neutrons. If they reach the drift region of a blocked semiconductor, these neutrons cause bursts of charge which cause a conductive filament to appear, resulting in the possible destruction of the device. The mechanism of the cosmic rays failure in semiconductors can be seen in figure 1.9 [136].

Each supplier of semiconductor gives formulas to estimate a mean expected FIT (Failures in Time, corresponding to the number of failures in one bilion device-hours operation). ABB's formula [3] depends on temperature, altitude and operation voltage. Its coefficients depend on

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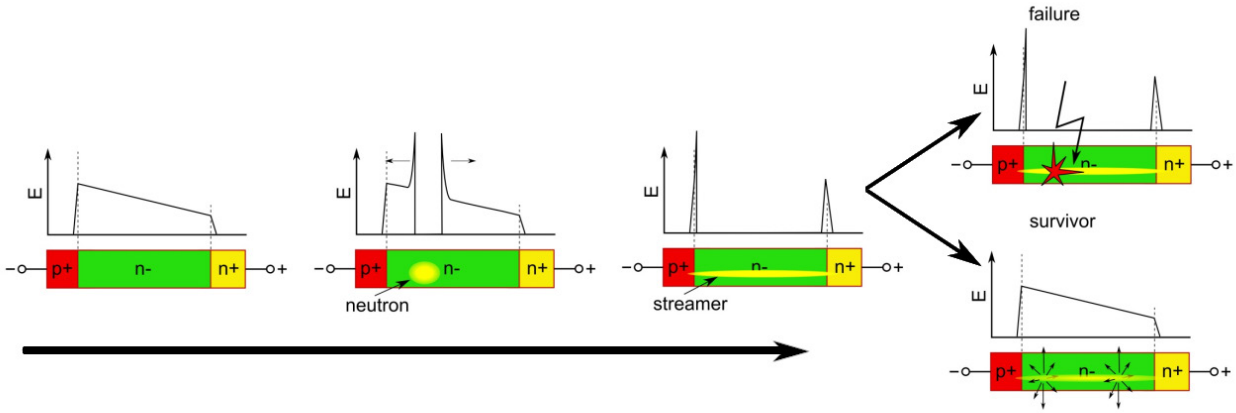

Figure 1.9: Mechanism of cosmic rays failure in a semiconductor adapted from [96], using a PiN diode for example.

the chip model. The formula from Semikron [96] is different but the dependencies are the same. An example of a failure rate function of operation voltage can be found in figure 1.10. It can be seen that the operation voltage has a dramatic impact on the failure rate, as increasing from 2550 to 3350 V results in a 1000-fold increase in failure rate.

In [98], it is said that typical target value for semiconductors is 100 FIT. It is confirmed by [41], where operation voltage is calculated to have a maximum failure rate of 100 FIT. Typically, the blocking voltage of the selected switch is usually noticeably higher than its intended operating nominal voltage (100 to 120 % higher, typically [69]), so that the FIT-rate of the semiconductor does not exceed 100.

1.1.5 Insulation Co-ordination

1.1.5.1 Definitions

Insulation co-ordination Insulation co-ordination can be defined in a simple way as in [40]: "Insulation co-ordination is the selection of the insulation strength." Or it can be defined in a more complex way like in the international IEC standards (60071-1, 61800-5-1) : the insulation co-ordination is the "selection of the dielectric strength of equipment in relation to the operating voltages and overvoltages which can appear on the system for which the equipment is intended and taking into account the service environment and the characteristics of the available preventing and protective devices".

Clearance and creepage distances Two distances are keys to the electrical insulation: the creepage and the clearance distances, defined in the UL 840 standard and the IEC 61800-5-1. The creepage distance is the shortest distance between two conductors at different potentials along the surface of an insulation material. The clearance distance is the shortest distance

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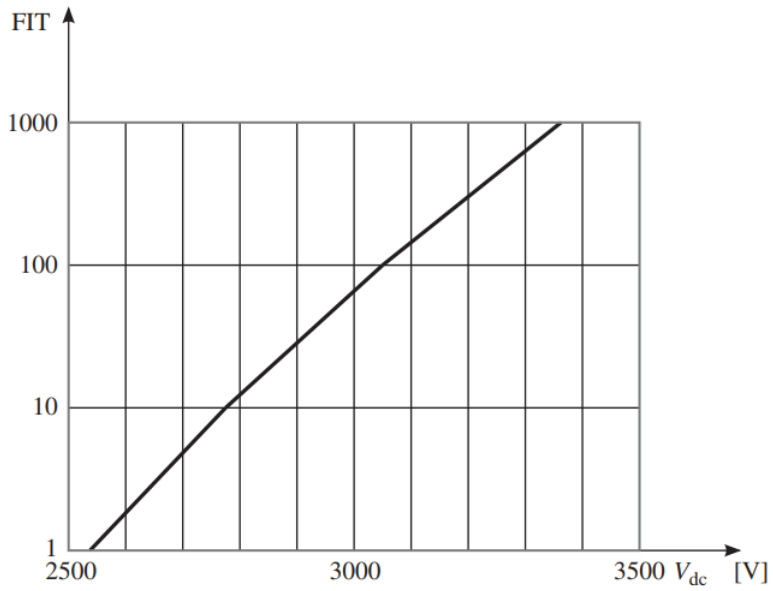

Figure 1.10: Example of the failure rate depending on the operation voltage of a 4kA/4,5kV IGCT. This figure is extracted from [98] but adapted from [101]. Temperature and altitude are not provided.

between two conductors at different potentials. These distances are illustrated in figure 1.11.

Pollution Degree The values of creepage distances depend on the pollution degree, describing the environment in which the system evolves. The pollution degrees, as defined in IEC 61800-5-1, are displayed in table 1.5. They basically describe how the environment could create conductive path with solid pollution, like dust, or liquid, like water.

Comparative Tracking Index and Insulating Material Groups The Comparative Tracking Index (CTI) is a charateristic of insulating material describing how easily an electrical breakdown can happen on the surface of the material (and not inside it). The method to measure the CTI is described in 6.2 of IEC 60112. The higher the CTI, the higher is the insulation. Insulating materials are classified into 4 groups depending on the value of the CTI: group I (CTI $\geq$ 600), group II (600 >CTI $\geq$ 400), group IIIa (400 >CTI $\geq$ 175), group IIIb (175 >CTI $\geq$ 100).

1.1.5.2 Insulation co-ordination in the MMC case, an example

In [19], four zones are defined for the insulation co-ordination of a low-power MMC: the submodule, the zone between the submodules inside a branch (leg or arm), the zone between the branch and the surrounding cabinet, the zone around the low voltage circuits (control boards and auxiliary circuits). But the MMC built in this publication is a MV MMC, so its overall size remains quite small (cabinet dimensions are 1970 mm x 800 mm x 800 mm). These zones are illustrated in figure 1.12.

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Table 1.5: Pollution degrees definition, according to IEC 61800-5-1

Pollution degree	Description
1	No pollution or only dry, non-conductive pollution occurs. The pollution has no influence.
2	Normally, only non-conductive pollution occurs. Occasionally, however, a temporary conductivity caused by condensation is to be expected,when the PDS is out of operation.
3	Conductive pollution or dry non-conductive pollution occurs, which becomes conductive due to condensation, which is to be expected.
4	The pollution generates persistent conductivity caused, for example by conductive dust or rain or snow.

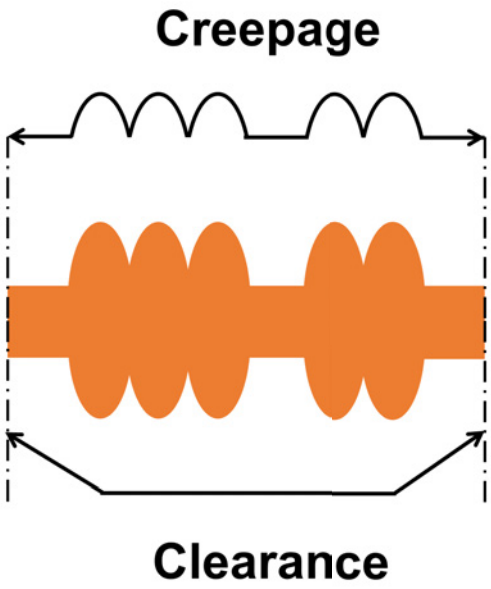

Figure 1.11: Creepage and Clearance distances, across an illustrative fictional object.

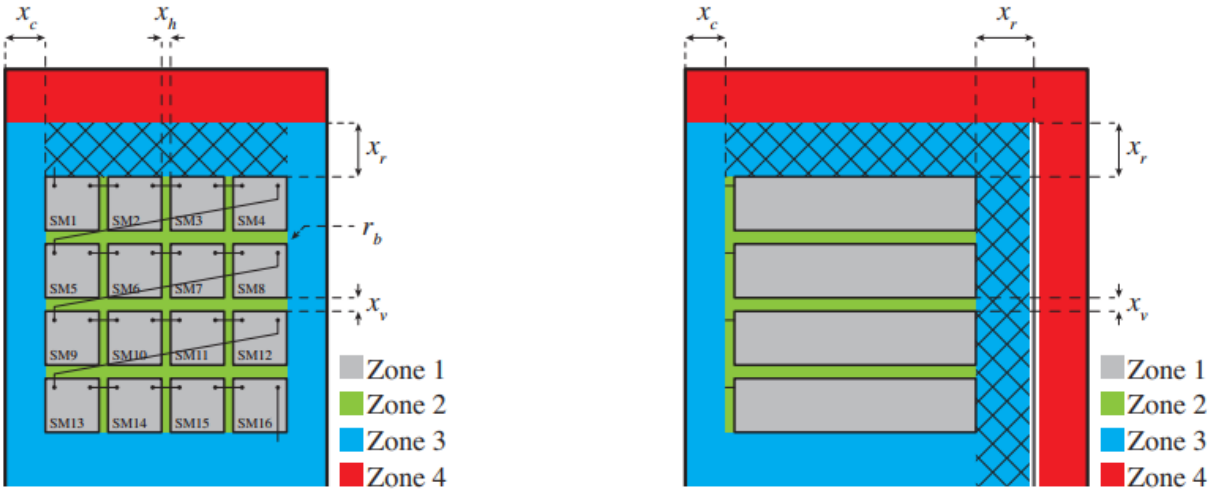

Figure 1.12: Insulation co-ordination analysis: areas defined in [19]

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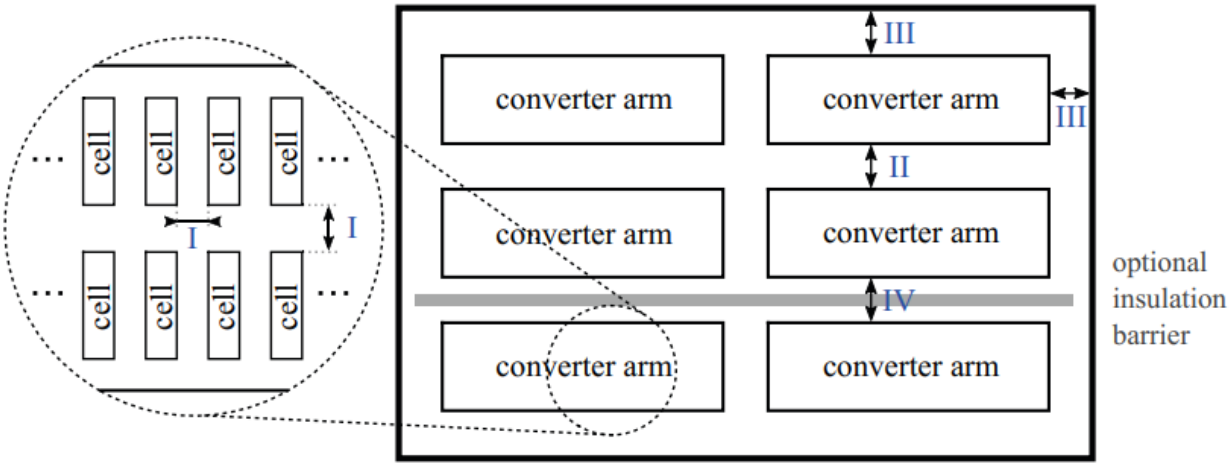

Figure 1.13: Insulation co-ordination analysis: distances defined in [48]. The distance IV is the same as III, but in the case of solid insulation between two arms.

For HV applications, the MMC can be much larger. In [132], the valve is typically 15 m x 12 m x 5 m. In [48], HV MMC are studied, and three different distances are determined: the distance between the submodules (cells), the one between the converter arms, and the one between the walls and the floor. These distances are illustrated in figure 1.13.

1.1.5.3 Insulation of the submodule, between submodules and modules

The submodules are in great majority insulated by air. In [19], the submodule is enclosed in a metallic box to provide shielding from the electrical field. This enclosure is not connected to the ground but to the negative terminal of the submodule . The same way, submodules are separated from each other either with air and mechanical supports (HV or MV) or directly with a cabinet (MV).

1.1.5.4 Insulation around the valve and between the valves

Mainly, the solution to ensure insulation between the valve and the building is, like before, to use air. The valves can be attached to the roof (like in figure 1.14b) or mounted on a mechanical support (like in figure 1.14a). In figure 1.14, corona shields can also be seen. These are the rings all around the valve to protect the valve from corona effect. Corona shields are in general, made of conductive material, with edges as smooth as possible, to shape the electrical field and reduce corona effect possibility. In [123], corona shields designs are tested, the different designs are diplayed in figure 1.15. In this article the critical value for the electric field is 2kV/mm. A higher value of electric field would potentially lead to corona effect.

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(a) Nanao RXPE MMC [10]

(b) ABB MMC (source : ABB)

Figure 1.14: Typical Built MMCs

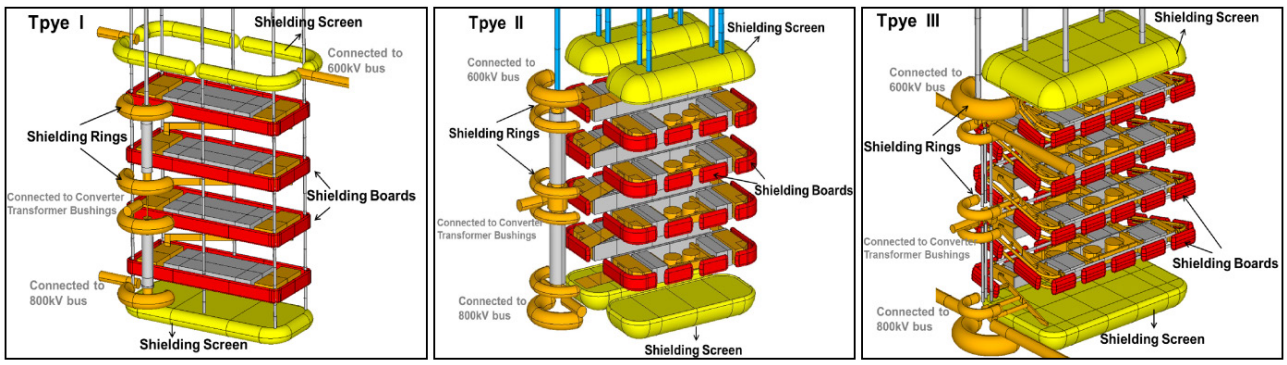

Figure 1.15: Example of corona shields designs in [123].

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Table 1.6: Some clearance distances for working voltages corresponding to typical voltages that can encountered in HVDC MMC Submodules (Source: IEC 61800-5-1).

Working Voltage (V)	Clearance Distance (mm)
1 000	1.5
2 300	5.5
4 500	14
23 000	90
50 000	220

1.1.5.5 The insulation of auxiliary circuits

The insulation between the high voltage (switches, capacitor) and low voltage (sensors, gate-driver) circuits is essential to avoid shorting, arcing and EMC problems. To avoid shorting and arcing, the creepage and clearance distances have to be respected. But to counter EMC problems, shielding and functional isolation are needed to ensure that the signals will not be sensitive to the perturbations. To ensure functional isolation, many isolation techniques exist: inductive coupling (transformer), optical coupling (opto-coupler, fiber optics), capacitive coupling or a monolithic coupling (level shifter) [41]. For MMC submodules, the commonly found solution for information transmission is fiber optics because it has a very high galvanic isolation (isolating different parts of the circuit without direct current flow) and EMI immunity, it can be used on long distances and it is compatible with high power and voltage.

On the other hand, the power supply of the gate drivers for the semiconductor switches is an issue that cannot be solved this way. Because of the high voltage level of all the elements of the submodules close to the poles, the mechanical structure and the other elements of the submodule are connected to the negative terminal voltage of the submodule, like a local ground (see section 1.1.5.3). The control signals can be centralised in a global controller, because as said before it is done with fiber optics, and the control board of the submodule can be connected at the negative terminal of the submodule. But for the power supply, where the needed power is between 10W (typical for IGBTs) to more than 100W (typical for IGCTs), it is difficult to reach a sufficient galvanic isolation. Therefore, an auxiliary power supply using the capacitor of the submodule as the source of energy is most often developed (like in section 1.3.5.3).

1.1.5.6 Typical Values for Clearance and Creepage Distances

Some values of clearance and creepage distances corresponding to typical values of working voltage for HVDC MMC Submodules are displayed in the tables 1.6 and 1.7.

1.2 Components of a Submodule

After the review on the MMC technology and its design characteristics in the previous section, the following section will focus on the submodule itself. This section describes the various components which can be found in an MMC submodule, investigating their functions and possible technology variants.

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Table 1.7: Some creepage distances for working voltages corresponding to typical voltages that can encountered in HVDC MMC Submodules (Source: IEC 61800-5-1).

Working Voltage (V)	**Creepage Distance (mm)**			
	Pol. level 1	Pol. level 2		
	All insulating material groups	Group I	Group II	Groups IIIa & IIIb
1 000	3.2	5	7.1	10
2 500	10	12.5	18	25
5 000	20	25	36	50
25 000	100	125	180	250

1.2.1 Power Switches and Diodes

1.2.1.1 Semiconductor Materials

Two major semiconductor materials are available to produce power switches with voltage rating exceeding 1200 V: silicon (Si) and silicon carbide (SiC). Si devices represent the vast majority of the market (15 G$ vs. 300 M$ in 2017) because their technology is more mature (the first SiC transistors were only introduced 10 years ago). Silicon carbide has superior properties: lower intrinsic carrier concentration, higher electric breakdown field, higher thermal conductivity, a larger saturated electron drift velocity, and a wider energy bandgap. This results in a thinner (up to ten times thinner), more doped, drift region, and so this lowers the on-state resistance. [8, 11, 26]

1.2.1.2 Semiconductor Switches Types

For HVDC MMC applications, the required type of switch is a high-voltage one, able to operate efficiently at frequencies around 250 Hz. For other applications, like motor MMC, higher frequencies are needed. Although any voltage rating can be considered for the switches, components with a higher voltage rating are preferred as they allow to build an MMC converter with fewer submodules. The main types of semiconductor switches that are available on the market are the following:

- The thyristors:
  - SCR (Silicon Controlled Rectifier)
  - GTO (Gate Turn-Off thyristor)
  - IGCT (Integrated Gate-Commutated Thyristor)
- The transistors:
  - MOSFET (Metal Oxide Semiconductor Field Effect Transistor)
  - IGBT (Insulated Gate Bipolar Transistor)

These components are presented in more details below. The semiconductor devices that are not or no longer on the market such as the SiC BJT (Bipolar Junction Transistor) or the ETO (Emitter Turn Off thyristor) are not developed here.

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Thyristor The thyristor (also called SCR) is a device with four layers of alternating p-type and n-type layers and with three terminals (anode, cathode and gate). It is used in power converters as a switch that is turned on when the gate receives a current impulse. It stops conducting when the current through the thyristor becomes lower than the holding current. Therefore, its turn-off is not controllable. This turn-off behaviour makes it difficult to use in a converter where the current does not naturally change sign during the switching period. Furthermore, this kind of switch needs a snubber circuit to avoid large di/dt at turn-on and large dv/dt at turn-off [93]. Thyristors are used in some HVDC converters thanks to their high voltage and current ratings (up to 8 kV and 5.6 kA), or because some of them can be triggered using light, ensuring good insulation with the control circuit [67].

Gate Turn-Off Thyristor The GTO (Gate Turn-Off) thyristor was introduced in 1980 [67]. It offers a controlled turn-off capability by applying a negative voltage to the gate. To efficiently remove the charges from the semiconductor, the GTO has finely divided cathodes and gates to form an interdigitated gate-cathode junction. It can be seen as a large number of thyristors in parallel with common anodes but individual gates and cathodes. This fine interdigitated structure permits a relatively homogeneous turn-off process across the surface of the device. But even with a fine structure, the charge removal is not totally homogeneous. And the larger the device, the more difficult it is to achieve a homogeneous operation of all fingers. This is the weak point of the GTO thyristor, because inhomogeneities in the turn-off process result in excessive current densities in some localized areas of the device, possibly causing failures.

Integrated Gate-Commutated Thyristor The GCT is an evolution of the GTO. Two improvements are the base of the GCT: a low-inductive housing-design allowing a quick, more homogeneous turn-off without filamentation, and a "transparent emitter buffer layer".

The buffer-layer and transparent emitter technologies consist in a weakly doped n-layer located between the n-base and the p-emitter. Thanks to this buffer, the electric field distribution in the semiconductor has a trapezoidal shape, allowing a much smaller silicon layer for the same blocking voltage. This results in reductions in on-state voltage and turn-off energies.

The low-inductive structure of the GCT (below 2 nH for the entire control loop of a GCT versus 50 nH for the GTO housing alone [5]), allows to rapidly redirect all the anode current from the cathode to the gate at turn-off. This prevents filamentation [5] and reduces turn-off times (the entire turn-off process takes around 10 µs for GCTs compared to around 100 µs for GTOs). Another consequence is a much better immunity to dV/dt, removing the need for a turn-off snubber.

Because of the need for a control loop with a very low inductance, GCTs are often proposed with an attached gate control unit. The IGCT is a GCT combined with its gate-drive circuit.

MOSFET The MOSFET is an unipolar device. This makes it switch faster than bipolar devices, hence allowing a higher switching frequency and/or to reduce switching losses. It is a voltage driven device and this characteristic makes the gate driver simpler and smaller. No snubber is required.

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The need for high voltage excludes switches like the silicon MOSFET as it is interesting only up to 600 V according to [26] and 100 or 200 V according to [8], due to its specific on-resistance that grows really quickly with the blocking voltage. Using silicon carbide instead of silicon reduces the specific on-resistance by three orders of magnitudes (according to [9] for 5-kV MOSFET). An interesting characteristic of the MOSFET is its really low switching losses (lower than the IGBT that is presented below). Nowadays, The SiC MOSFET is used in MMCs but only for small current converters or/and high frequency MMCs – like in ship electrical systems, due to the low current ratings available today. This rating makes it unsuitable for HVDC MMCs, where the nominal current is at least 1kA, without putting a lot of them in parallel.

IGBT The IGBT is a voltage-driven semiconductor developed in the early 1980s using a combination of a MOSFET and a N-P-N transistor structure [8]. Its relatively low losses and its ability to operate at high frequencies (several kilohertz) make it widely used in many fields, for applications with blocking voltage higher than 200 V [9]. It requires a simple gate unit with a low power consumption. Compared to the GCT or other thyristors, which are made on a whole semiconductor wafer, IGBT modules are formed by paralleling a number of smaller semiconductor chips, making it scalable to different power ratings.

IEGT This transistor has a the same structure as the IGBT but it has bigger trenches than IGBTs. This transistor permits to have a higher collector-emitter voltage (at blocking state) and a low saturation voltage, according to [111]. Toshiba is the most famous manufacturer of IEGTs. Press-pack is also available.

1.2.1.3 Semiconductor switches packaging types

Two types of packaging exist for semiconductor switches: press-pack and plastic module. The choice of press pack (PP) rather than plastic module (PM) is explained through the listing of the drawbacks of PM and PP in [16]. Mainly, the PP is expected to have a longer lifetime (because of the elimination of solder layer and bonding wires), a higher i^2t capability, a potential short-circuit failure mode and an explosion-proof package. But press-pack components imply the implementation of a pressing system, making its use not as flexible as plastic module package.

1.2.1.4 Current/Voltage ratings of the switches available on the market

As mentioned above, it is difficult to find references which provide an up-to-date comparison of the capabilities of different switch technologies. For example, most of the data on thyristor-based switches date from the 90s, a time where the IGBT technology was not as advanced as it is today.

To give a better overview of the performance of the various switch technologies, the graph in figure 1.16 presents the maximum ratings of devices currently available from major manufacturers, as a function of their current and voltage ratings. Only IGBTs, IEGTs and IGCTs are considered, as they can be turned on or off. Furthermore they are available in current and voltage levels which are compatible with an HVDC converter and have been used in real

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implementation of submodules. Note that this does not constitute a full comparison of the performance of the switches, as it does not present the losses in conduction nor in switching. A more in-depth comparison is presented in sections 2.3, 2.4 and 2.5.

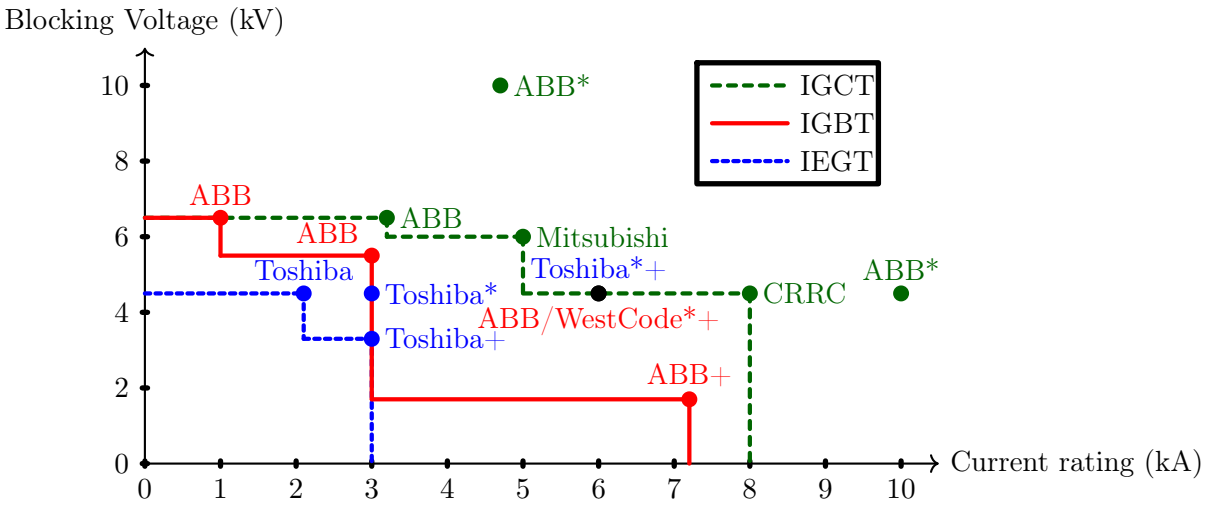

Figure 1.16: Ratings of semiconductors (IGBTs, IEGTs and IGCTs), with the blocking voltage and the current calculated in the section: $I_{dc-igbt}$ for IEGTs and IGBTs and $I_{eq-igct}$ for the IGCTs. '+' means 'not found in catalog but in literature', '*' means 'prototype'. The black dot corresponds to at the same time an IEGT from Toshiba and an IGBT from ABB/WestCode. Sources: ABB, Mitsubishi, CRRC, Dynex, Toshiba online catalogs (2019) and [31, 18, 83]

1.2.1.5 Switches selection

The switches are chosen for a given submodule according to two main constraints: their operating area – operating voltage and current, as well as transient surges – and failure rate due to cosmic rays. Other factors are taken into account such as: max. operating temperature, switching frequency range, losses, price. But the main parameters – voltage rating and current capability – are selected with the study of the SOA (Safe Operation Area) and the failure rate.

Safe Operation Area The Safe Operation Area represents the voltage and current domain in which power switch can safely operate in. According to [98], the main mechanisms limiting the safe operation area are avalanche breakdown and overheating, but filamentation, latch-up, and dynamic avalanche are also important. The SOA is specificied for a level of stray inductance and junction temperature T_j (temperature of the semiconductor chip).

Once the typical values of voltage and current are defined for the submodule, the power switch must withstand standard operation and stay in its safe operation area. If not, the power switch is not selected. A SOA of a fictitious IGBT is drawn in figure 1.17.

Switching Frequency For higher frequencies SiC switches (MOSFET mainly) are preferable. However, HVDC MMCs tend to require low switching frequencies (between 100Hz and 300Hz), for which Si is suitable.

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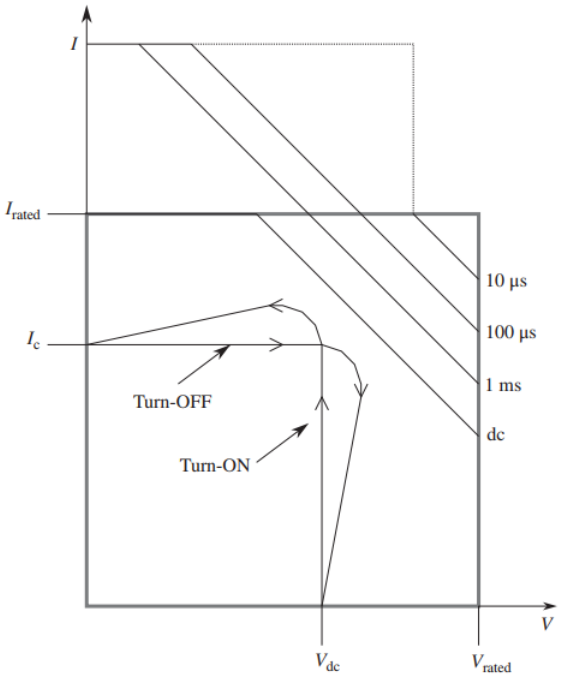

Figure 1.17: SOA of a fictitious IGBT [98], showing the focus of turn-on and turn-off switches.

1.2.1.6 Diodes selection

For the diode selection, similar constraints are taken into account: the SOA, the nominal voltage and current, the switching frequency and losses. For the SOA, T_j, di/dt, current, voltage and stray inductance can be specified. The two main types of diodes in semiconductor devices (PiN and Schottky) will be explained in details in chapter 4.

1.2.2 Capacitors

1.2.2.1 Capacitor technologies

As presented in section 1.1, an MMC submodule is basically comprised of a capacitor bank and some power switches. In an HVDC submodule, the capacitor is typically rated a several millifarad, and 2 kV or more. As a consequence, it stores large amounts of energy (several kilojoules) and has a large volume.

A comparison between the different technologies of capacitors is presented in [105]. The three main technologies of capacitors are: electrolytic capacitors, ceramic capacitors and film capacitors. The technology massively adopted in HVDC MMC SMs are film capacitors [28, 105, 98, 50]. A qualitative comparison of those different technologies in DC-link applications is done in [122]. This qualitative approach is still valid in MMC application and is diplayed in figure 1.18. The energy storage density for each technology has been assessed in [80] and is presented in figure 1.19. It shows that ceramic and film capacitors have close energy density (around 200J/L) while electrolytic capacitors have higher energy density. In [105], MMPF capacitors have been listed and their energy density is around 300 to 350 J/L for a voltage rating higher

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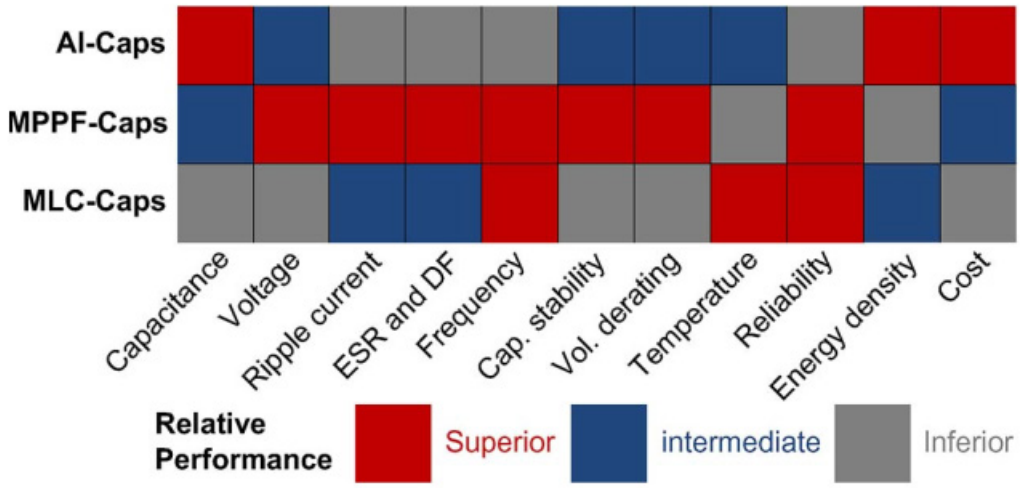

Figure 1.18: Qualitative approach for comparison of capacitor technologies (Al-caps=electrolytic, MPPF=metalized film, MLC=ceramic), extracted from [122].

than 1000V.

Despite their better energy density electrolytic capacitors present problems that make them unsuitable for MMC SM. The first one is that their maximum nominal voltage is only around 500 V, so to reach high voltages series connection is needed [105, 109]. The second one is their reliablity. In [81], the reliability of eletrolytic capacitors and film capacitors is compared in an MMC application. It concluded that the reliability of film capacitors is better. The third one is the ripple current capability. In [122], it is said that film have better ripple current capabilities per capacitance, as shown qualitatively in figure 1.20. [105] has found with its listing of film capacitors that film capacitors have a capability from 100 A/mF to 400 A/mF, while [109] gives a value of 20 A/mF for electrolytic capacitors. These problems make the electrolytic capacitor unsuitable for HVDC MMC submodules.

For ceramic capacitors, the capacitance ratings are not high enough for HVDC MMC Submodule (below the mF for [104]), mainly due to the difficulty of firing large ceramics [84]. The failure-mode of the ceramic capacitors is also problematic with the absence of self-healing [122] causing short-circuit to be the dominant failure mode [122, 84].

1.2.2.2 Self-healing

Self-healing is a really interesting property of metalized film capacitors. In case of failure of the dielectric, the metallic layer is vaporized due to high temperature and to its really low thickness (a few nanometres). This implies that even if the dielectric cannot isolate anymore, the fault area does no longer conduct because the metal has vanished. It is also called clearing instead of self-healing and is illustrated with the figure 1.21.

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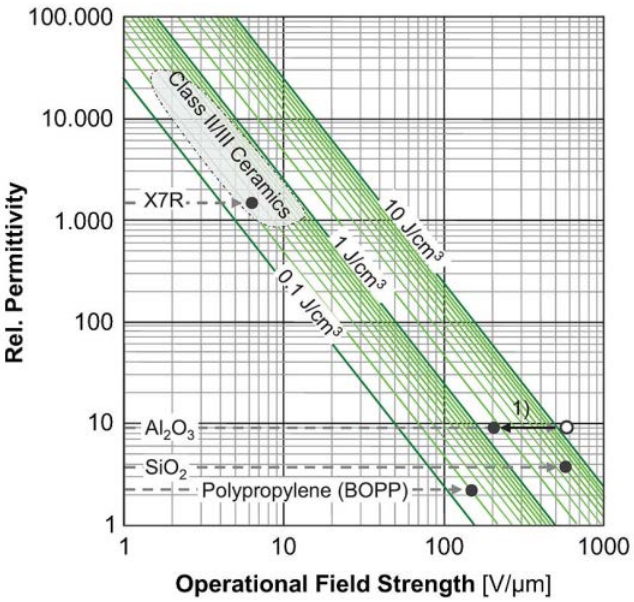

Figure 1.19: Energy density of different capacitors technologies (Al_2O_3=electrolytic, SiO_2=silicon, BOPP=film, X7R=ceramic), extracted from [80].

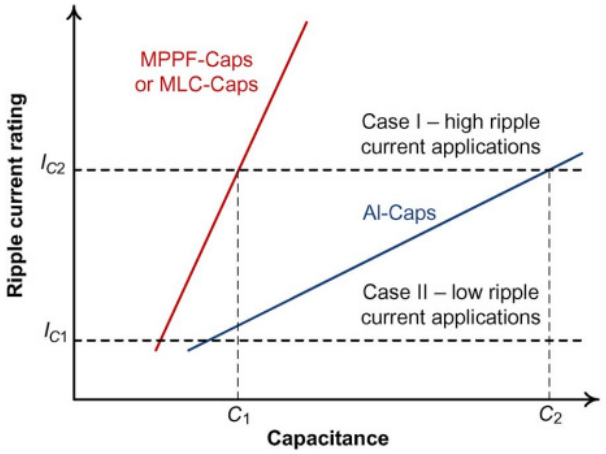

Figure 1.20: Qualitative comparison of current capabilities between electrolytic capacitors (Al-Caps) and the other technologies (MPPF and MLC-Caps) – extracted from [122].

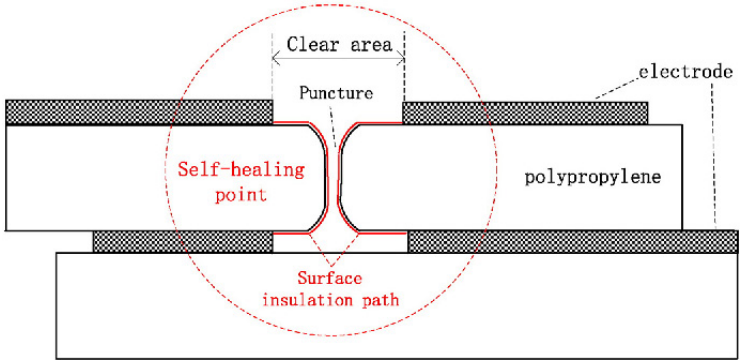

Figure 1.21: Mechanism of Self-healing [55]

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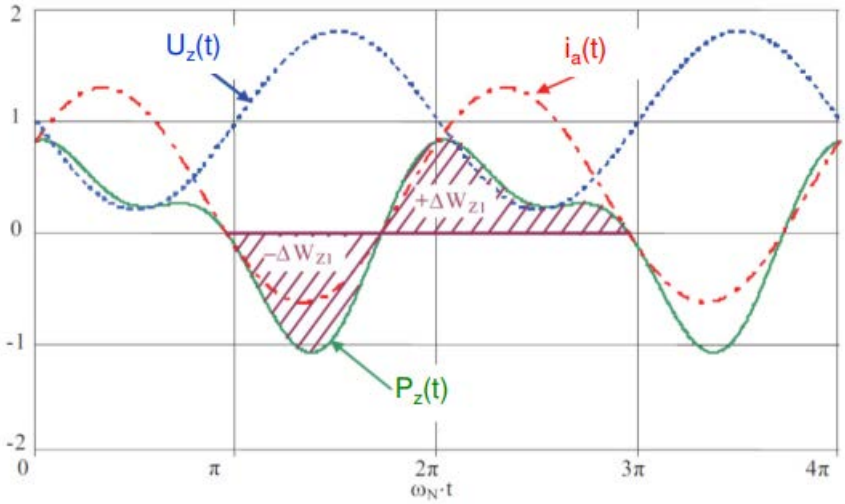

Figure 1.22: Arm Current, Arm Voltage and Energy Deviation [69]

1.2.2.3 Capacitor dimensioning methods

This subsection summarises the different methods for the MMC submodule capacitor dimensioning. It will focus on this issue: for a given MMC, what is the capacitance value.

One of the most used design techniques is based on the peak-to-peak energy deviation of the capacitor, between the minimum energy and the maximum energy stored in the submodule capacitor during normal operation. The corresponding voltage ripple across the capacitor is then basically determining the capacitance, because minimum and maximum energies correspond to minimum and maximum voltages of the capacitor, respectively.

In [28, 69], the dimensioning is based on the following assumptions: idealized, sinusoidal arm voltages and currents, half-bridge submodules, no circulating current, no energy transfer between the phases – a phase being a leg of the MMC. The energy deviation is calculated by integrating power between two zeros of current (equation 1.3). The waveforms of the arm current, arm voltage and arm power exchange can be found in figure 1.22.

$$\Delta W_{SM} = \frac{2.P_s}{3.k.n.\omega}.\Big(1 - \big(\frac{k.cos(\phi)}{2}\big)^2\Big)^{\frac{3}{2}} \tag{1.3}$$

ΔW_{SM} is the energy deviation in the capacitor of a submodule, P_s is the apparent power, k is the voltage modulation index, $cos(\phi)$ is the power factor, n the number of submodules and ω is the fundamental frequency of the AC side.

The submodule capacitance value then depends on the allowed the voltage ripple (modelled as $U_{Cmin} = U_{Cnom}.(1-\epsilon)$ and $U_{Cmax} = U_{Cnom}.(1+\epsilon)$) is:

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$$W_C = \frac{1}{2}.C_{SM}.U_{Cnom}^2 = \frac{1}{4.\epsilon}.\Delta W_{SM} \tag{1.4}$$

With W_C the energy stored in the capacitor. Thus the obtained capacitance value is:

$$C_{SM} = \frac{\Delta W_{SM}}{2.\epsilon.U_{Cnom}^2} = \frac{P_s}{3.k.n.\omega.\epsilon.U_{Cnom}^2}.\Big(1 - \big(\frac{k.cos(\phi)}{2}\big)^2\Big)^{\frac{3}{2}} \tag{1.5}$$

In [75], the dimensioning technique is based on exchanged deviation too. The hypotheses of the model are the following: voltage and current waveforms are assumed to be ideal, i.e. the voltage waveform does not have a staircase shape (normally due to the limited number of submodules in an MMC, like in figure 1.2b); the energy stored in the various inductors of these converters is neglected; all the cell capacitors in a stack – also called arm – present the same voltage; the stacks of cells are analysed under the load convention.

Then the deviation of energy is calculated as above and the same equation is obtained:

$$C_{SM} = \frac{\Delta W_{SM}}{2.\epsilon.U_{Cnom}^2} \tag{1.6}$$

In this study one parameter is added compared to the precedent method: the AC voltage is allowed to vary between 90% and 110% of its nominal value (±10%). This makes the equations much more complex, and makes it impossible to have an analytical solution. So the energy deviation is obtained by numerical resolution and the result can be seen in figure 1.23.

The highest energy deviation for an MMC arm happens when the AC grid voltage is at 90% of its nominal value, and transmits reactive power only. So the capacitor in that case has a minimum value of:

$$C_{SM} \geq \frac{1.22|S|}{3\omega U_{Cnom} V_{DC} \epsilon} \tag{1.7}$$

For 50 Hz and 10% of voltage ripple, the minimum energy is 39kJ/MVA for the whole converter.

In a precedent article [74] of the same author, the AC voltage was considered to remain at its nominal value and the resulting miniminum capacitance value was found to be:

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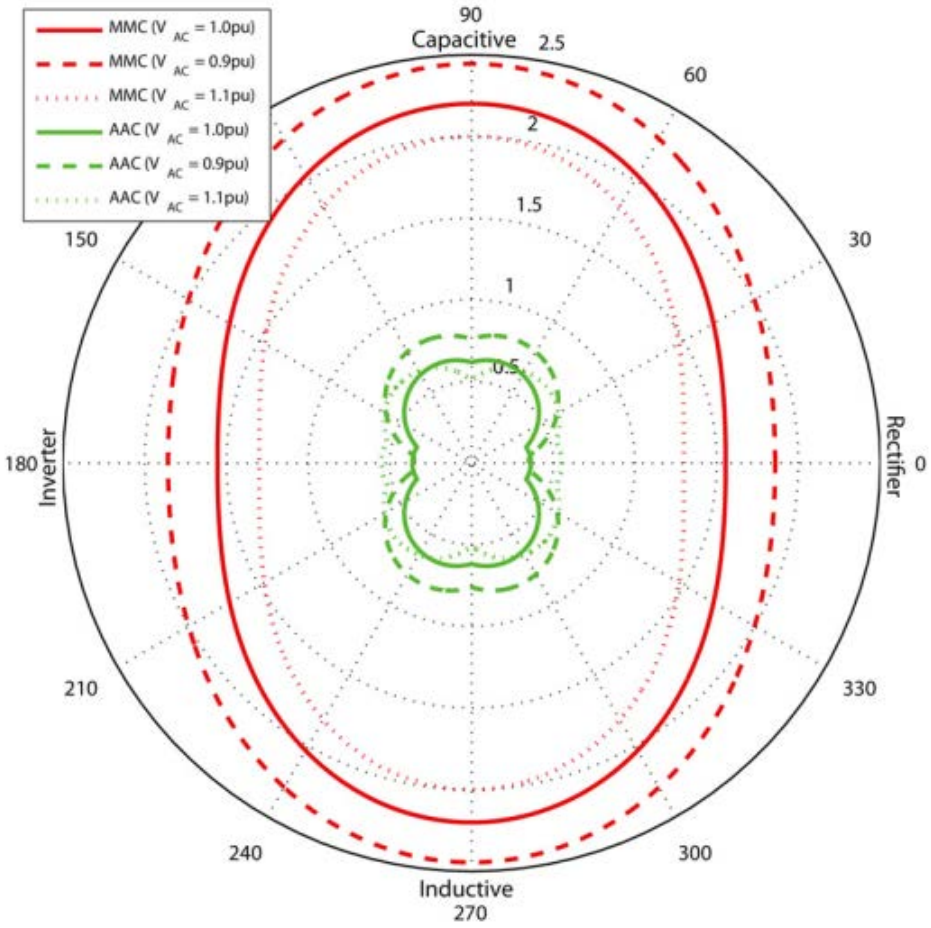

Figure 1.23: Normalised peak-to-peak energy deviation for the MMC (dark red), depending on power factor. The light green curves are for AAC converter(not studied in the thesis). [75] Normalised energy deviation is defined this way: $\Delta W_{SM-norm} = \frac{\Delta W_{SM}.3\omega}{|S|}$. $\Delta W_{SM-norm} = \Delta W_{SM}.3\omega/|S|$

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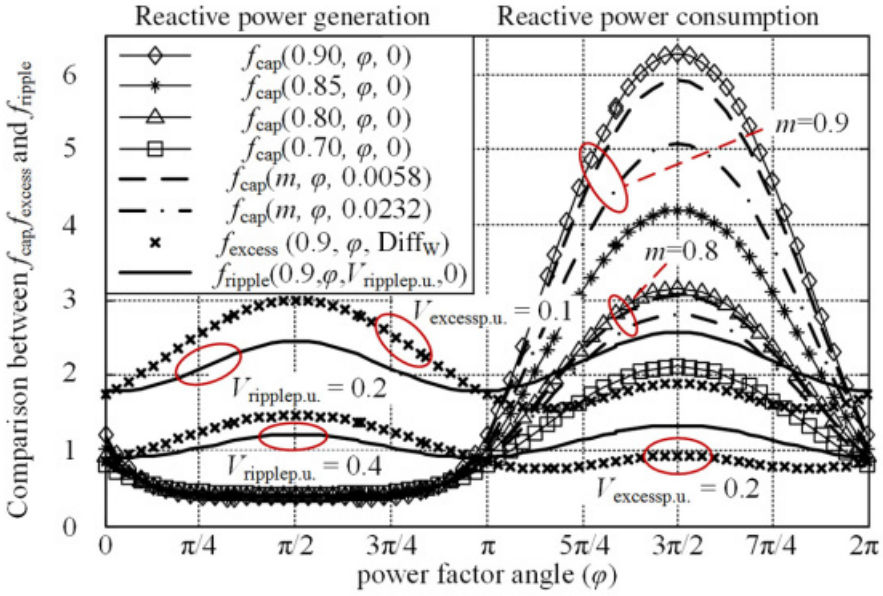

Figure 1.24: Comparison between f_{ripple}, f_{cap} and f_{excess} with different parameters for capacitor selection [107]

$$C_{SM} \geq \frac{1|S|}{3\omega U_{Cnom} V_{DC} \epsilon} \tag{1.8}$$

This proves the importance of taking into account the variation of voltage that often occurs on AC grids. Indeed, a 10% change can result in a required capacitance value being 22% higher (on the behalf of this method and model).

In [108], an even more sophisticated dimensioning method is developed. On top of the voltage ripple of the capacitor, it also takes into account: the maximum allowed capacitor voltage, the capability to synthezise the required arm voltage at any time to ensure the conversion between AC and DC sides, and the current ripple capability. Nondimensionalised functions are developed for each one of these criteria (f_{excess} for the maximum voltage, f_{ripple} for the ripple voltage, f_{cap} for the capability to synthezise the arm voltage). Those functions depend on the operating point of the MMC (modulation factor, power factor).

The calculations in [108] will not be developed here. What is important to understand is that each function is evaluated at different operating points, and by comparing them, a minimal capacitance value is determined. The three functions f_{ripple}, f_{cap} and f_{excess} are evaluated for some values of parameters in figure 1.24.

The Balancing Control Algorithm influence (BCA) In all the dimensioning methods in this section, the capacitors of all submodules in an MMC were considered at the same voltage (balanced situation). But in real operation, this is not the case. In [57], the influence of the unbalancing voltages has been studied. The main result is that the unbalanced voltages make the voltage extremes more important, as if the voltage ripple was more important. In this

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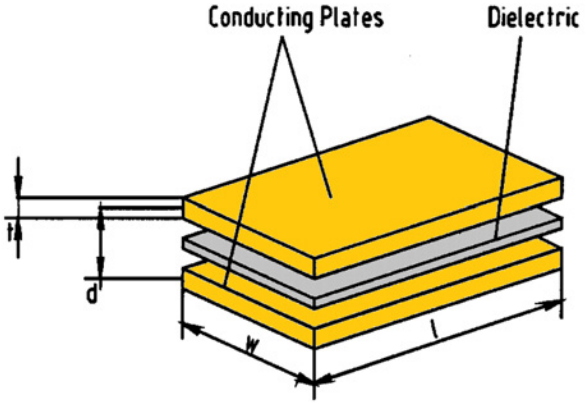

Figure 1.25: Exploded view of a busbar [89]

publication, it has been found that the switching frequency of the submodules, representative of the switching losses, is inversely proportional to the submodule capacitor voltage unbalance. This means that, as described in this section, the obtained capacitance values with the dimensioning methods are **minimum capacitance values**: the BCA has to be taken into account for the final value selection.

1.2.3 Interconnections

The connections inside a submodule are done with bus-bars, to connect the capacitor, the semiconductor switches, the protection systems and to provide terminals for the submodule. They are made out of copper plates, and sometimes a dielectric layer in-between (forming in that case a so-called "laminated busbar"). The use of laminated busbar is not general and is often found for high-voltage high-frequency submodules (like in [125] with high voltage, 6kV, SiC submodule). A diagram of such a busbar is available in figure 1.25.

1.2.3.1 Stray Inductance and EMC

The distance between the two planes creates a loop and causes a non-negligible stray inductance to appear. This inductance might be responsible for overvoltages and oscillations at turn-on and turn-off of the semiconductor switches. This could disturb the operation of sensitive elements (because of electro-magnetic coupling), or even cause the destruction of components (due to excessive overvoltages). The stray inductance is divided into two types: internal inductance L_i (due to flux linkages inside the conductors) and external inductance L_e (due to the space around the two conducting plates). A formula for the stray inductance, taken from [89], valid under certain hypotheses ($d << 2t$ and $d << t + w$ for the calculation of L_e, ref to fig 1.25), is the following equation 1.11. The expression of L_i is valid only at low frequencies (this threshold is linked to the skin effect), L_e is frequency independent.

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$$L_{stray} = L_i + L_e \tag{1.9}$$

$$L_i = \frac{\mu_0 \mu_r}{8\pi} l \tag{1.10}$$

$$L_e = \frac{2\mu_0 \mu_r l}{\pi} \ln(1 + \frac{t}{t+w}) \tag{1.11}$$

For more complex cases, or for geometries which do not meet the hypotheses, numerical modelling is required with software tools such as Ansys Q3D Extractor. In [128], a typical value of total stray inductance in a 2.5kV MMC submodule is given: between 70 and 120 nH. In [16], where a submodule is designed values between 160nH and 200nH are mentioned. In the datasheets of the semiconductors are mentioned typical expected stray inductances in a commutation cell (300nH for the IGCT 5SHY 42L6500 from ABB, 150nH for the diode 5SLD 1200J450350 from ABB). Basically, values from between 100nH and 300nH can be expected.

1.2.3.2 Mechanical Constraints

Mechanical constraints are due to Lorentz force which arises from the circulation of current in the busbar and from the magnetic field it creates. They are mainly dependent on the current levels and the space between the conductors. The formula of the applied force on the busbars can be found in [21], but it is quite complex. A simpler, but probably less accurate formula can be found in [110]. It can be used to analyze the dependencies of the phenomenon. This equation is given in (1.12), and the shape of the conductor can be selected from the abacus in figure 1.26. This figure is used to define k (a corrective factor corresponding to the influence of the shape of the conductor). I_1, I_2 are the currents in the two conductors, l is the length of the conductor, and F is the force applied. A quick calculation of the effort applied to the busbar with the following parameters (currents both equal to 1 kA, k = 1, d = 50 mm, l = 1m) gives a total strenght on the busbars of 4N. If the busbars were closer and only 5 mm away, it would be 40N. Those sets of parameters would correspond to normal operation of a submodule (current at 1kA). If the current is as high as it can get during overcurrent events (like DC pole-to-pole short circuit), around 25kA, this strenght would be 625 times higher.

$$\frac{F}{l} = \frac{\mu_0}{2\pi} I_1 I_2 \frac{k}{d} \tag{1.12}$$

Exemple with a real submodule busbar in [16] In [16], a submodule design is presented. One of the specific features of this submodule is the use of a thyristor as permanent bypass, being achieved by the eventual failure of the thyristor as a short-circuit. In the simulations, a current of 246 kA goes through the thyristor and therefore the busbar. This current result in a maximal stress of 190 MPa and a busbar deformation of 0.35mm (obtained by simulation). A suitable busbar design permits to keep electrical contacts between the parts in case of maximum current.

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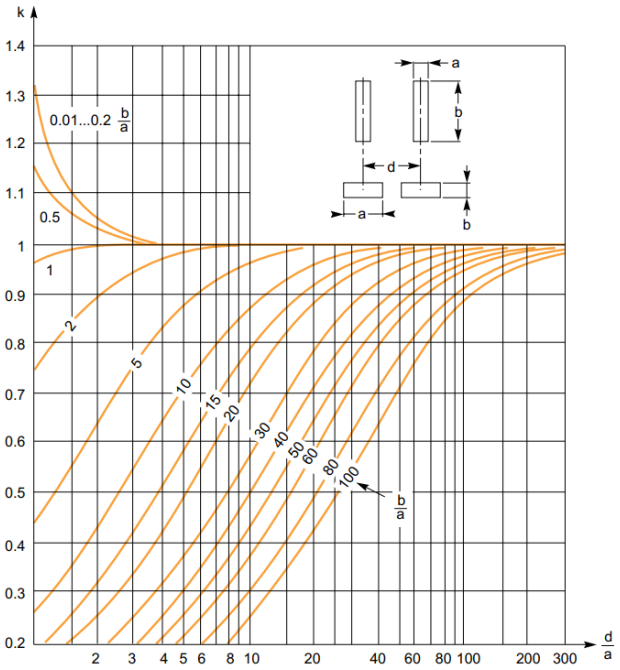

Figure 1.26: Variation of k as a function of ratios b/a and d/a (Dwight's chart), extracted from [110], but originally from [23]

1.2.3.3 Losses

The losses are quite simple to calculate for the rectangular model of the bus bar. For low frequencies, the resistance is the following (with w the width, l the length, and t the thickness of the busbar):

$$R = \rho \frac{2l}{wt} \tag{1.13}$$

In case of high frequency operation, if the skin depth is such as $t > 2\delta$, the resistance changes: (reminder: $\delta = \sqrt{\frac{2\rho}{\omega\mu}}$)

$$R = \rho \frac{4l}{w\delta} \tag{1.14}$$

1.2.3.4 Dielectric Insulation

The dielectric insulation between the two plates can be realised with a solid insulator. The main parameter is the distance between the two plates. Polyimide (Kapton) and epoxy are commonly used like in [73] or [89], but for higher voltages (6kV in [133]) GPO3 and PET can be found. The minimum thickness of the insulation is determined by the ratio of maximum admitted

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voltage over dielectric strength of the material. Temperature variations have to be taken into account when evaluating the dielectric strength. Partial discharge events can also happen, due to inhomogeneities (like air bubbles). In [133], the determined insulation thickness is 5mm of GPO3, with two PET films, between the negative and positive poles with 6kV difference, to take into account the partial discharge events by having a more homogeneous electric field distribution in the insulating material.

1.2.3.5 Conclusion on Dimensioning Aspects

To design a busbar three main aspects must be considered: the stray inductance, the dielectric insulation, the mechanical constraints. To minimize the stray inductance, the space between the conducting plates must be reduced. But that distance can not be reduced too much due to the necessity of a sufficient air gap for air insulated busbars, and a sufficient dielectric insulation thickness in the case of laminated busbars. This distance has to be bigger than the distance for nominal voltage, due to overvoltages (maximum considered voltage can be the breakdown voltage of the main semiconductors). The mechanical constraints have to be calculated not at nominal current but at maximum current, corresponding to the short-circuit current.

Air insulation case The dielectric insulation is not the general case, air insulation is often found in HVDC converters and MMCs from the valve level to the submodule level and their busbars. Such a design needs a lot of space because it has to respect creepage and clearance voltage between parts and busbars having different potentials (see section 1.1.5).

1.2.4 Auxiliary Circuits

1.2.4.1 Gate-Driver

The gate-driver is the circuit that applies the desired voltage and current to the gate of a power switch to turn it on or off. It is basically the interface between the control signals and the power switches. These circuits are very different depending on what the semiconductor switch is. IGBTs and the MOSFETs are voltage-driven switches with voltage varying from -15V to 20V approximately, while the GTO and the GCT are current-driven with current pulses that can reach a few kA.

As it contains low-level electronics and is in direct contact with the power switches, the gate-driver is particularly sensitive to electro-magnetic interferences (EMI). In high voltage applications, fibers optics are used to communicate with the central controller of the MMC, thus providing an insulation barrier and preventing the transmission of EMI. The issue of EMI becomes even stronger with faster switches; an example of gate driver design for SiC MOSFET can be found in [126]. To ensure good operation despite the electro-magnetic noise generated by the power semiconductors, the whole submodule has to be designed to reduce parasitic inductance and capacitance. In [43], the gate driver structure is using low inductance paths to divert common mode current from sensitive parts of the gate driver.

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The gate driver circuit may also include protection functions to ensure fast reaction in case of unexpected behaviour. In [56], the gate-driver has: a “miller clamping” to prevent spurious turn-on of a SiC MOSFET; a de-sat protection with soft turn-off in case of over-current; an under-voltage lock-out (UVLO) feature, to ensure that the power semiconductors are safely turned off in case the gate driver power is lost; a submodule capacitor voltage monitoring; a PWM signal check, to ignore possible erroneous firing signals; an optical fiber malfunction protection; an EMI shielding. Sensors may be required for some of these protection functions. They are developed in the next part.

1.2.4.2 Sensors

Mainly three types of sensors are found: temperature (for the power switches, junction temperature), voltage (capacitor voltage, power switch voltage) and current sensors. This section lists the different sensors or the measurement method for each type.

Temperature Sensor Direct temperature measurement can be achieved with infrared cameras, thermocouples (based on thermoelectric effect), resistance thermometers (resistors with a varying resistance depending on temperature) and fiber optic thermometers. Temperature measurements with these sensors can be invasive and complex, so they are not implanted in MMCs. Two other methods exist. The first one is based on the use of "Temperature Sensitive Electrical Parameters" (TSEPs) of the power semiconductor devices, like the on-state resistance, the threshold voltage, the collector-emitter voltage. These parameters are temperature dependent and are measured by using voltage or current sensors. The drawback of that method is that each temperature sensitivity is specific to one semiconductor and its package. The other method is based on observers, like the equivalent thermal network [88]: by measuring the temperature somewhere else, like the cooling liquid temperature, it is possible to calculate the junction temperature of a semiconductor.

Current Sensor Here are the main types of sensor that are used for current measurement: current transformers, Rogowski coils, shunts (resistors) and Hall effect sensors (often used in their closed loop version).

The shunts are basically resistors, using the Ohm’s law. Using resistors implies additional losses, and may require temperature compensation. Resistors offer no galvanic insulation which makes them more complex to use on floating potentials [88]. They can measure DC as well as AC currents.

The current transformers rely on the induction phenomenon and because of that can not measure direct current, but they provide a galvanic insulation. They are used for measuring rapid current peaks like in [126, 124] to monitor high di/dt transients. The current transformers can be "conventional" ones with a magnetic core, iron-free transformers and Néel effect magnetic core transformers [85]. A common problem with most transformers is the material saturation, when the measured current exceeds the capability of the transformer.

Rogowski coils are air coils wound around the measured current conductor, combined with an integrator to recreate the current waveform. Rogowski coils are iron-free: this allows the

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device to work at high frequencies (30 MHz for a commercial product such as PEM CWT HF) and to overcome the saturation problems of conventional transformers. But no DC measurement can be achieved with the Rogowski coils (for the PEM probe above, the minimum frequency is 0.1 Hz).

The last type of sensor is the Hall effect sensor. The Hall effect is the occurence of a voltage across a material with high electron mobility (like gallium arsenide GaAs, indium antimonide InSb or indium arsenide InAs), transverse to an applied current and to a magnetic field. To measure the current with a Hall sensor, a magnetic core encircles the cable to measure and a Hall sensor is inserted in a gap of the magnetic core. It is based on the magnetic field measurement and permits to measure a direct current [88, 85]. This combination of current transformer and Hall sensor is widely found in power electronics. It can measure DC and AC currents.

Voltage Sensor Voltage measurement can be done in many ways. An example is a Hall effect-based circuit: a resistor is connected across the voltage difference which has to be measured, causing a current to appear. This current is then measured with a Hall effect sensor with a transformer, which indirectly gives the value of the measured voltage.

Generally, the method is to lower the voltage to measure directly (with a voltage divider for example) or indirectly (using a resistor to transform the voltage into current), while providing an insulation (capacitive barrier, piezoelectric transformer, magnetic transformer, optocoupler) [85]. The use of an amplifier can be found like for the Petercem company to lower the voltage to make it measurable [87]. For low voltage submodule, a simple resistive voltage divider can be used like in [114].

1.2.4.3 Power Supply of Auxiliary Circuits

The auxiliary circuits have to be powered. One solution is to provide a central power supply that is connected to each submodule. But for HVDC MMCs, this is challenging as high voltage insulation must be provided between each submodule.

Another solution to power the auxiliary circuits is to draw the needed power locally using the submodule capacitor as the power source. A large voltage conversion ratio is then required (capacitors are usually charged at several kilovolts, while the auxiliary required voltages are in the range of 10-20 V). It is therefore not possible to use linear voltage regulators or a resistive voltage divider, as they would have a conversion efficiency in the order of 1 %. Therefore, switching based power supplies have to be used.

The EPFL has developed a simple power supply based on a fly-back converter and a switch [114], for a submodule with a rated voltage of 625 V. In [43], this solution is provided: based on a voltage divider structure with switches and resistors, it can be compared to a half-bridge submodule for its switching part. This active circuit, which can be seen in fig. 1.27, also contains a start-up circuit. This power supply is designed for submodules (or power electronics building blocks PEBB) using 10 kV SiC devices. The complexity of this kind of circuit grows with the nominal voltage of the capacitor: supplying the same low power needed for the auxiliary circuits from a higher voltage is challenging. In [125], a two-switch flyback converter has been

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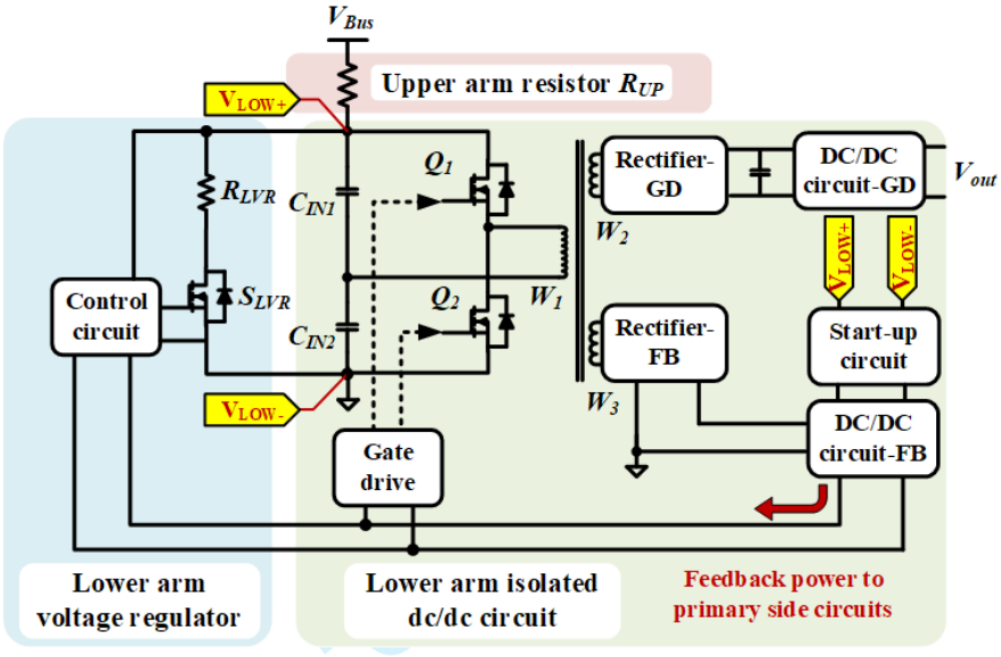

Figure 1.27: Auxiliary power supply structure of [43]

chosen for a PEBB with 1.7 kV SiC MOSFETs. In [124], a resonant circuit with rectifiers has been designed for a submodule with 10 kV SiC MOSFETs.

Besides the large voltage conversion ratio, another challenge of these power supplies is to ensure they will start as soon as the voltage in the capacitor is high enough. This require self starting oscillators. In [33], a flyback solution has been developed with series-connected SiC JFETs for a 2 kV source. These devices are normally-on, which makes it easier for the converter to start. The input voltage can be higher but the number of series-connected JFETs has to increase.

1.2.5 Protections Systems

The devices for protection have different roles: to protect the submodule or its components (over-currents or over-voltages), to bypass the submodule in case of fault, to discharge the capacitor when the submodule is shut down. As different technical solutions can be implemented for this, this section is organized around the different functions rather than around the different components. It should be noted that little information is available in the literature on these functions, which tend to be only implemented in industrial products, not in the demonstrators used in academia.

1.2.5.1 Protecting the diodes in case of DC short-circuit

In case of a DC-side short-circuit with HB submodules, the DC voltage falls below the voltage on the AC side of the MMC, so an un-controlled current can flow through the low-side diodes of the submodules from the AC side to the DC side. This means that a very large surge current

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goes through the lower diodes.

To protect this diode, a temporary bypass thyristor is often used, like in the submodule of AlstomGrid [98], in [30], or in the submodule of Siemens [98]. A thyristor is used because is has a large current withstand capability and because a device with natural turn-off behavior is acceptable (the interruption of the fault current being taken care of by, for example, a DC breaker). This thyristor must have the same blocking voltage as the other power switches. The figures 1.37 and 1.38, presented with their corresponding submodules in the next section 1.3, display such thyristors.

Another solution is implemented, for example, by ABB: no thyristor is required because their diodes withstand the surge current of a DC-side short-circuit until the AC breaker opens [98]. It is the same for [16], the diodes are able to withstand the surge current. This may be because of the packaging technology (diodes from ABB and [16] are press-pack or stakpak diodes), and/or because they have a larger current ratings (in which case they would cause larger recovery losses in normal operation).

1.2.5.2 Bypassing the Submodule

Being able to bypass the submodule if it is faulty is essential. For that, two solutions have been found in the literature. The first one is the vacuum mechanical switch (used in the submodule of AlstomGrid [98], in [30], in the submodule of Siemens as well [98]). Its blocking voltage has to be the same as the power switches and it has to withstand the nominal current and the surge current. Because this bypass is needed in case of failure of the submodule, the activation of the switch must require only a small amount of energy that can be stored nearby, such as compressed air or pyrotechnical triggering.

The other solution is the use of a thyristor with a short-circuit failure mode like in [16] (as shown in figure 1.28). A shoot-through is intentionally triggered, forcing the capacitor to discharge rapidly through the thyristor, causing the failure of the thyristor, which becomes a short-circuit. Because the thyristor is connected in the other direction compared to the diodes, this thyristor can not be used as a protection for diode in case of DC short-circuit.

1.2.5.3 Protecting the submodule from overvoltages

In [114], two anti-parallel transil diodes are connected to the submodule terminals to avoid any overvoltage. Rated at 900 V, they turn into breakdown mode in case of overvoltage.

1.2.5.4 Summary of Protection Systems

Table 1.8 summarizes the various protection systems described in this section

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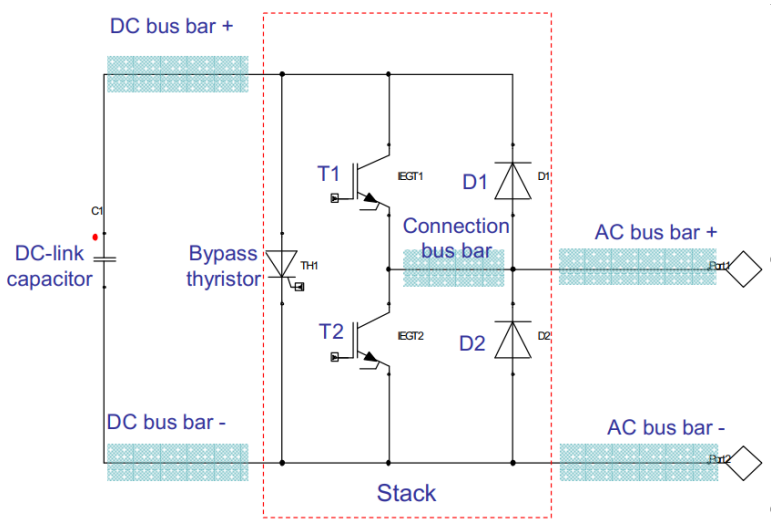

Figure 1.28: Connections of the submodule of [16]

Table 1.8: Summary of submodule protection components

Component	Description	Aim	Seen in
Bypass Thyristor (terminals of the submodule)	Thyristor connected in the same direction compared to the diodes	Helping the diode to support the surge current in case of DC-side short-circuit (temporary bypass)	AlstomGrid submodule [98], [30], Siemens submodule [98]
Bypass Thyristor (capacitor)	Thyristor connected in parallel with the capacitor, to trigger a shoot-through and turn the thyristor into permanent short-circuit	Bypassing the submodule (in case of fault)	[16]
Mechanical Switch	A vacuum switch, possibly with pyrotechnic triggering	Bypassing the submodule (in case of fault)	AlstomGrid submodule [98], [30], Siemens submodule [98]
Transil Over-Voltage Diodes	Two antiparallel diodes connected to the SM terminals	Over-Voltage protection, by turning into breakdown mode	EPFL submodule [114]

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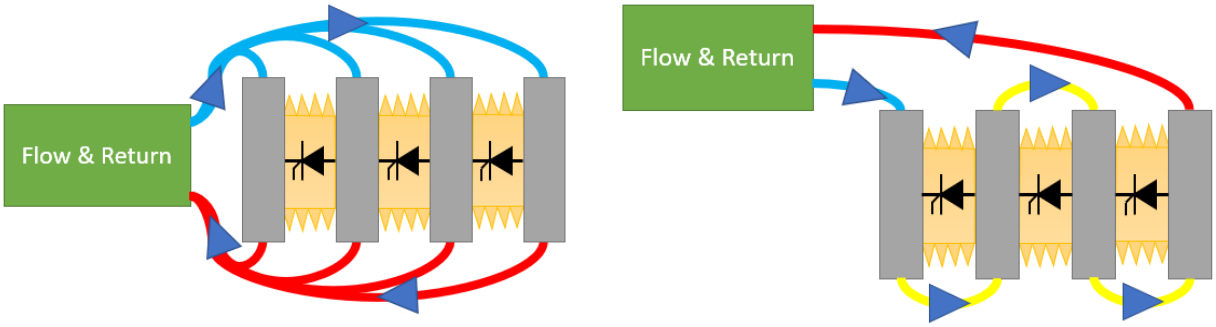

(a) Parallel Cooling System (b) Series connected Cooling System

Figure 1.29: Cooling System Structures, with the example of three thyristors in series.

1.2.6 Cooling

1.2.6.1 Cooling Principles in High Voltage Valves

In HVDC, the cooling systems follow the same rules and principles whether they are thyristor valves or MMCs. Two main cooling techniques are available: direct exchange with the surrounding air, or using a liquid coolant (dezionised water or another coolant like a phase-changing fluid in [28] or [79]) to move heat further before it is released in the environment.

Regarding direct air cooling, depending on the available space and the level of losses, it can be forced convection or a combination of forced and natural convections (forced convection at the submodule level, natural convection at the MMC scale, like in [56]). No example of natural air cooling has been found for an HVDC MMC.

Regarding liquid cooling, two structures are possible: series and parallel, as it can be seen in figure 1.29. The choice between the two solutions depends on the design of the heatsinks located at the power switches: their flow rate and their pressure losses. As it is said in [98], extensive studies are required to design adequate cooling system capacities for the converter.

In HVDC converters, dezionised water cooling is commonly found [60]. The water is dezionised for the following reasons: to avoid corrosion, and to avoid leakage currents through the coolant which may interfere with the normal operation of the converter [47]. Some ethylene glycol is added to the water to prevent freezing. The heatsink is made of metal, so it is a good heat conductor. In some cases, it is also used as an electrical conductor between two components (switches, diodes...). The pipes going from one heatsink to another are made of insulating material such as PEX. The cooling circuit is then connected to external heat exchangers.

Passive cooling systems exist and would avoid reliability problems due to the active parts (pumps for example). Such system is described in [79]. It consists in a thermosiphon working with a dielectric fluid which undergoes a phase change. But this kind of passive system is unsuitable for HVDC converters due to the high converter losses and volume, therefore high active cooling power is needed.

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Table 1.9: Table with examples of loss studies and submodule cooling designs

Project or Publication	Average losses of 1 SM (kW)	Operation Temp. Max (°C)	Allowed Temp. Max (°C)	Cooling Method
[28]	5.5	81.6	125	passive, phase changing (unknown liquid)
[30]	2.536	-	-	forced cooling water
[56]	-	133.2	175	forced air (SM scale) and natural air convection (MMC scale)
[61]	5.6	102	150	-
[16]	2.042	81	-	forced water, heatsink described

1.2.6.2 Cooling systems and losses of submodules in literature

Table 1.9 gives examples of cooling designs for power losses of one submodule. Its aim is to reflect the order of magnitude of power losses and junction temperature in a submodule.

1.3 Review of Existing Submodules

This section is a review of what has been found in the literature on MMCs and submodules, the companies and the laboratories working on MMCs. This list is not exhaustive, but describes designs and teams working on this subject, with corresponding publications. For the following submodules (ABB, Siemens, GE Grid), no public information has been found on the exact values of current, voltage ratings and capacitance.

1.3.1 Alstom Grid / GE Grid

The information about the Alstom Grid (now GE Grid) in the thesis is mostly extracted from [98]. A picture of a GE Submodule is displayed in figure 1.30.

This submodule is based on plastic module IGBTs (no press-pack). It is equipped with two bypass systems. The permanent bypass switch is mechanical. It has to withstand the nominal valve current (1kA) and the surge current. The bypass thyristor protects the diodes in case of a DC side short-circuit. It is triggered in case of overcurrent [98].

1.3.2 Fraunhofer Institute IISB

This information is extracted from [12]. The Fraunhofer Institute has developed a submodule based on a horizontal design. This means that rather than mounting the control electronics and the power switches on a small side of the capacitor – like most of the submodules – these are mounted on the large side of the capacitor. This has a major impact on the organisation of

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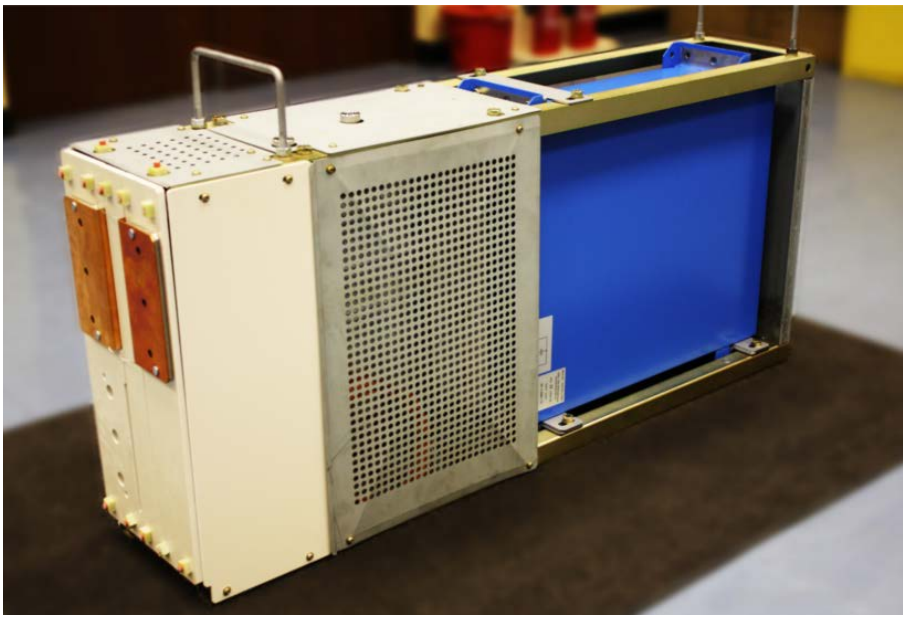
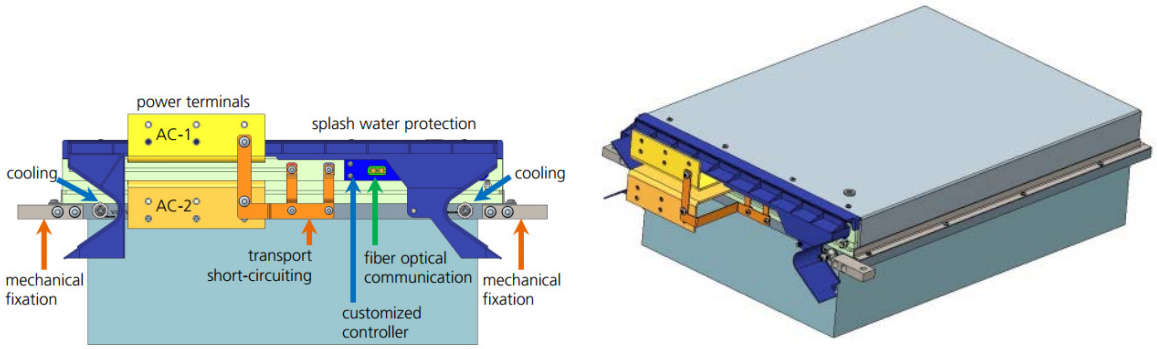


Figure 1.30: Alstom Grid/GE Grid Submodule [50]



(a) Side View (b) Side/Top View

Figure 1.31: Submodule of the Fraunhofer Institute [12]

the structure and the cooling surface is more important. The submodule can be seen in figure 1.31. The capacitor is the part below and the power electronics and control parts are on top. For comparison, a typical submodule with a vertical oriented design can be seen in figure 1.32.

With the information available so far, it is not clear, however, how electrical insulation is ensured between submodules: [12] describes a rack-mount assembly which is optimized for rapid submodule replacement, but does not appear to contain insulating sections.

1.3.3 Siemens

The Siemens submodule is described in [98], which corresponds to fig.1.32b. A bypass thyristor is located between the metal plates in the front. This thyristor is housed in a press-pack package (the white, grooved part). It is used as a protection for the anti-parallel diodes of the IGBTs in case of a dc-side short-circuit (to handle the short-circuit current).

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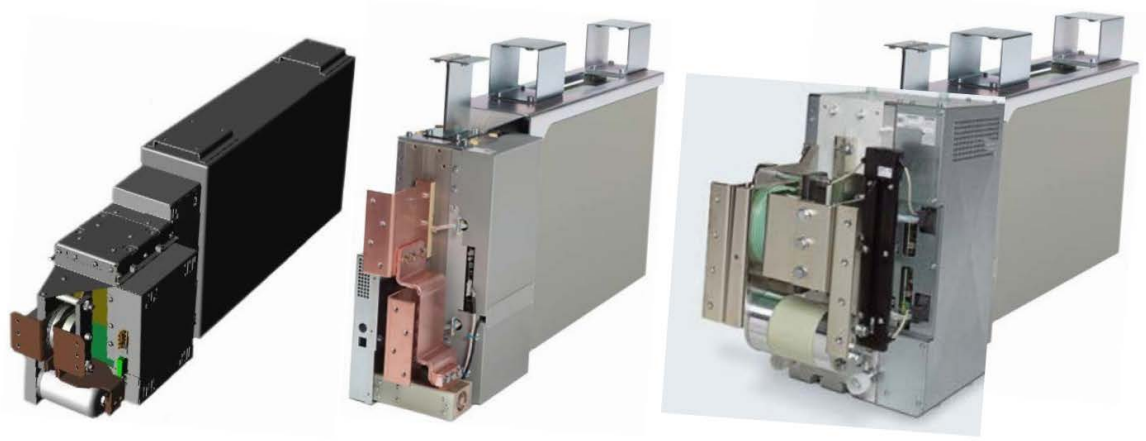
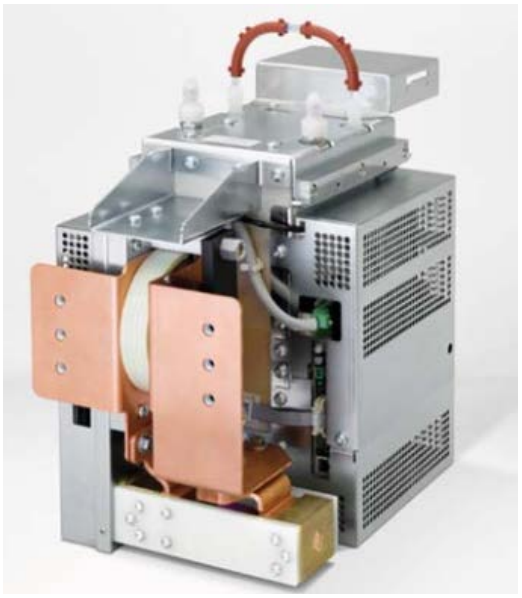


(a) Siemens submodules variants from [12], Half-Bridge and Full-Bridge



(b) Siemens submodules from [98]

Figure 1.32: Submodules from Siemens, without the capacitor

The white block at the bottom/front contains the vacuum switch, which is used the same way as in the case of the submodule from Alstom Grid (see section 1.3.1), to bypass the submodule in case of fault. On the top of the submodule, fittings for the cooling circuit (de-ionized water) are visible. On the right, perforated metal sheets constitute the housing for the communication, control and IGBT gate driver electronics of the submodule. Their ratings are not described in the found documents. This submodule exists in Half-Bridge and Full-Bridge variants.

1.3.4 ABB

In the ABB design presented here, the half-bridge submodules use switches consisting of eight series-connected press-pack IGBTs each (Fig. 1.33). Cooling blocks are inserted between each IGBT press-pack, and use de-ionized water to cool them. This water goes through the white plastic pipes. This series connection allows to increase the voltage rating of the submodule, hence reducing the overall number of submodules in an MMC converter, and therefore simpli-

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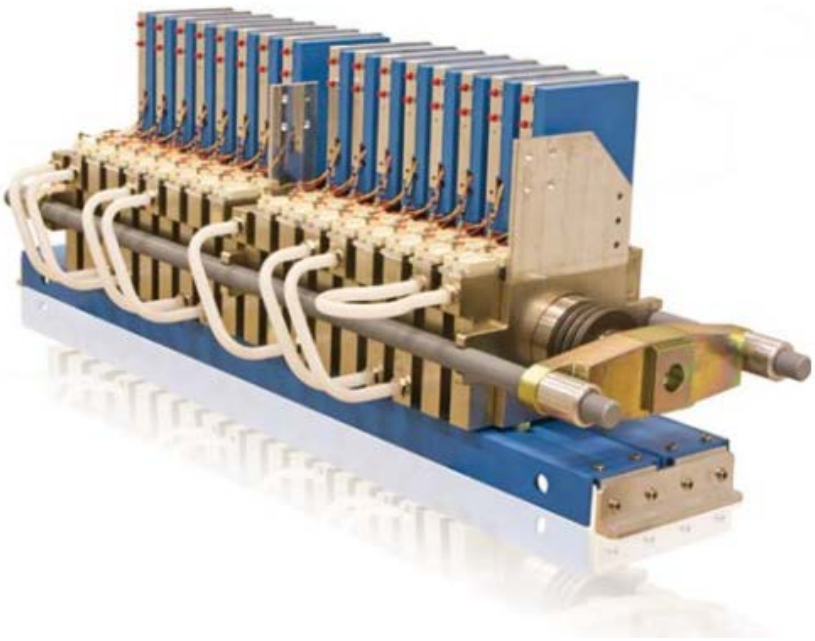

Figure 1.33: The switching part of ABB's MMC submodule [98]

fying the general control system. Press-pack IGBT modules seem to be necessary with this cascaded structure, because they offer a fail-to-short behaviour, and therefore do not require bypass switches. On the contrary, bypassing the entire submodule when a single IGBT module fails would result in disconnecting 7 perfectly good ones (and loosing a large blocking voltage capability). According to [98], the diodes of the submodules are designed to handle a DC short-circuit until the circuit breaker of the MMC cuts off power.

According to [98], this structure makes the local control (i.e. at the gate drive level) more difficult. ABB has developed its own gate drive that is able to ensure static and dynamic voltage sharing among all IGBTs in the stack. Mechanically, the whole stack is held together with plastic rods, allowing a precise mechanical pressure and constraint to be applied on the stack. This is important for electrical and thermal conduction.

A double submodule structure is used here according to [98], the double submodule can be seen in figure 1.34. Rounded tubes form corona rings, to prevent arcing with the environment; the capacitors can be seen in the back of the photograph. As for the Siemens submodule, the ratings of the ABB submodule are not described.

1.3.5 Submodule designs from scientific literature

The submodules described below are only presented in the scientific literature, so it is sometimes difficult to evaluate their industrial maturity. Some of them may be used industrially, while other were clearly developed in the course of academic reseach projects. Although it is related to an industrial installation, the first submodule below (Nan'ao MMC) is described in this section because all the sources that were found referring to it are scientific papers.

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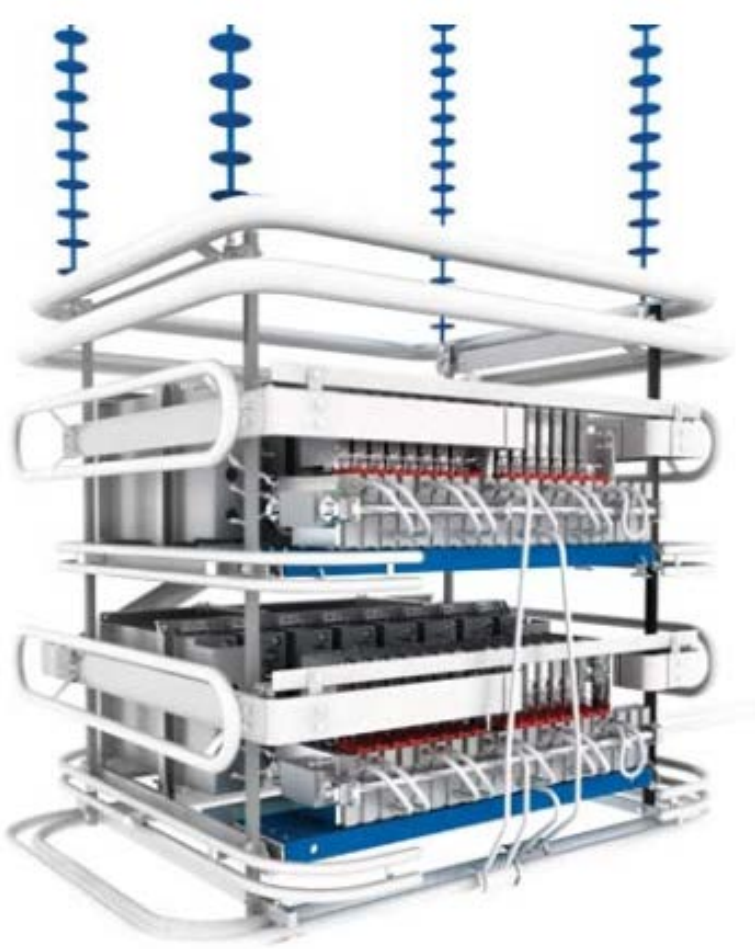

Figure 1.34: ABB's MMC double submodule [98]

1.3.5.1 Press-Pack Based Submodule - Nan'ao MMCs (RXPE and Queen's University Belfast)

The Nan'ao station is a multiterminal HVDC and one of the MMC is based on Press-Pack IGBT (PPI). This MMC is a ± 160 kV/200 MW station.

The publication [16] explains the design of the submodule of this station. The choice of PPI (Press Pack IGBT) rather than PMI (Plastic Module IGBT) is explained through the listing of the drawbacks of PMI and PPI. (see section 1.2.1.3) The diodes have an i^2t capability large enough to withstand the DC short-circuit current (the protection circuit diagram of the converter – in particular the presence of a circuit breaker – is not addressed in the publication). The submodule has a patented feature: a protection thyristor connected in parallel with the capacitor. When fired, this thyristor creates a short circuit across the capacitor, causing the thyristor to melt and form a permanent short-circuit. Therefore, unlike in 1.3.1, no mechanical switch is required to ensure the continuity of the current flow in case of submodule failure. This solution reacts faster than a mechanical switch. This is irreversible, as the thyristor is destroyed in the process. The PPI implies that diodes and IGBTs are in different packs. They are connected through heatsinks and busbars. The submodule (without the control electronics) can be seen in figure 1.35.

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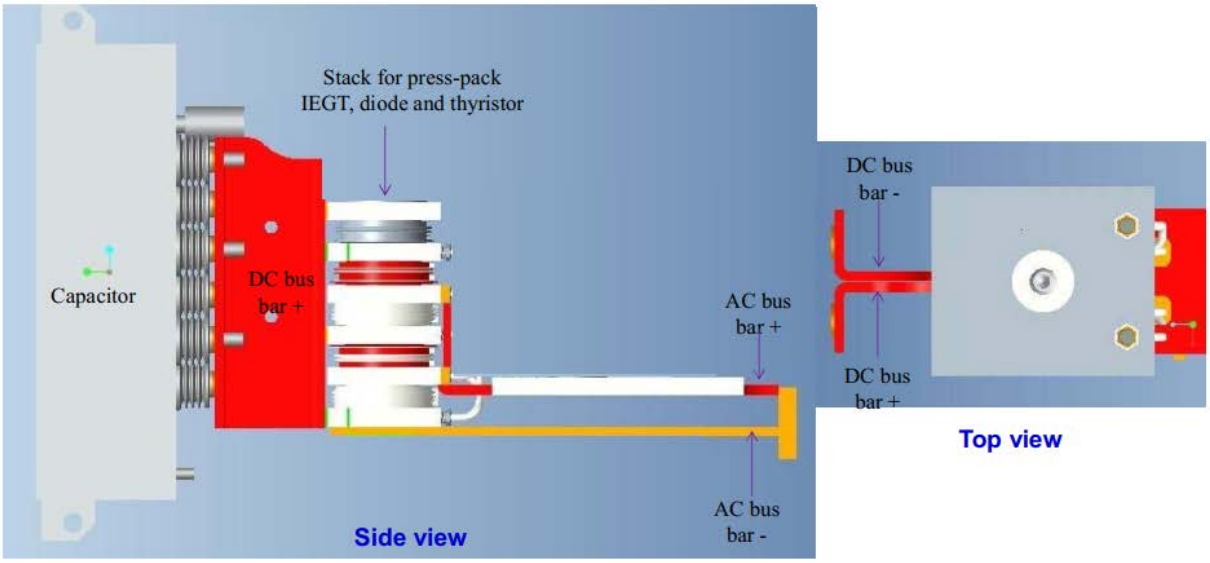

Figure 1.35: MMC submodule of Nan'ao station [16]

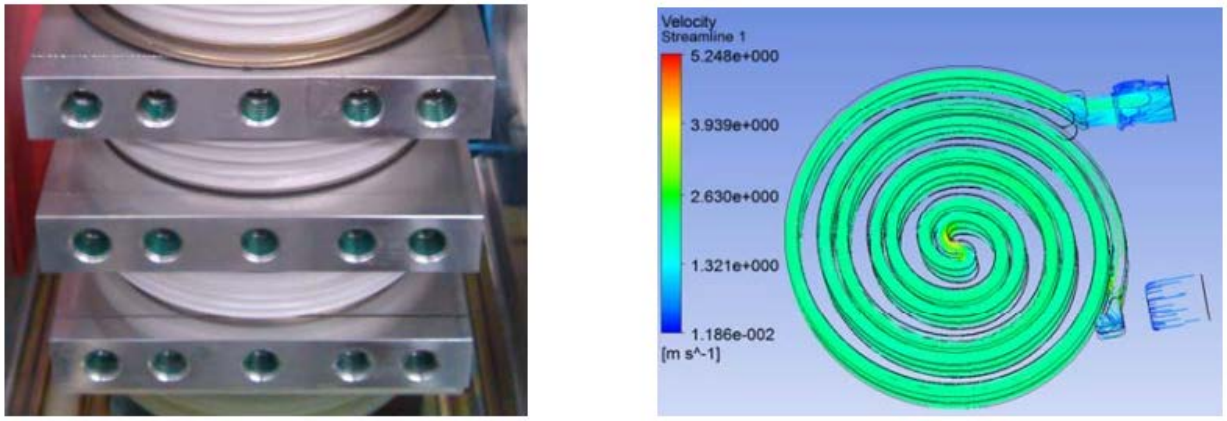

Figure 1.36: Nan'ao submodule heatsink [16], with its computer model on the right side

Table 1.10: Description of the Nan'ao Submodule

Characteristic	Description
Electronic Module	Press-Pack IGBTs and diodes
Bypass Switch	SCFM Thyristor only
Heatsink	see figure 1.36
Switching Frequency	200 Hz
Capacitance	5 mF
Average Voltage Cell	2.5 kV
Stray Inductance	164.4 nH (FEM), 202 nH (IGBT turn-off sim), 100 nH (test)
Switches	IEGT S6X06B(ANSD,Q) for simulation (4.5 kV/1.5 kA)

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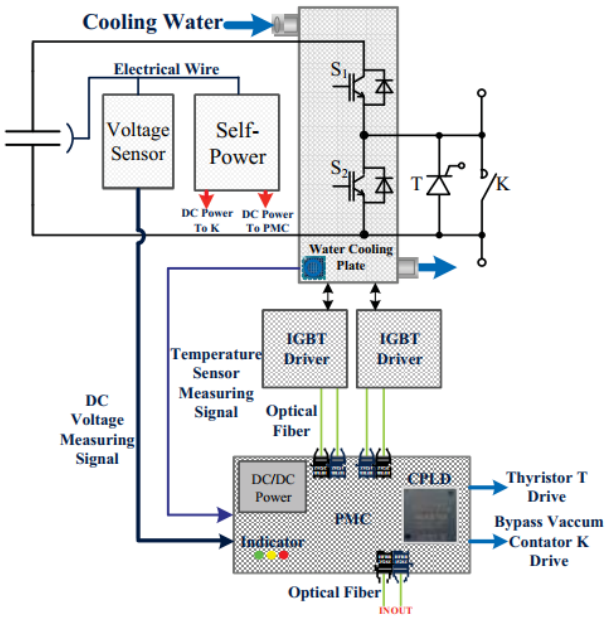

Figure 1.37: Submodule structure of [30]

The thermal management system uses the heatsinks depicted in figure 1.36. An original structure, with double-spiral cooling channels makes the coolant temperature uniform over the surface of the cold plate. The greenish holes on the photograph are used for mechanical support and electrical connections.

The characteristics of the different parts of the submodule are described in table 1.10.

Table 1.11: Description of the submodule from [30]

Characteristic	Description
Electronic Module	IGBTs 3.3 kV HB (FZ1500R33HL3 from Infineon)
Bypass Thyristor	Yes
Bypass Switch	Vacuum switch
Cooling system	Forced water with 4L/min, cooling plate
Operating Frequency	50 Hz
Switching Frequency	400 Hz
Capacitance	8.5 mF
DC Voltage	1.7 kV
Current	910 A (peak)
Sensors	Voltage, Temperature
Other features	Self-power from capacitor, fibre optics

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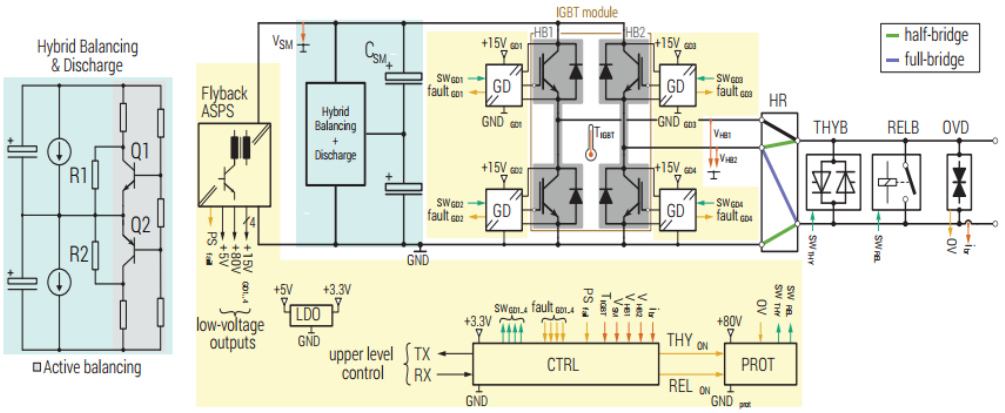

Figure 1.38: circuit diagram of the EPFL Low Voltage Submodule [114], the yellow part corresponds to the Control PCB part and the blue one to the power PCB part.

1.3.5.2 Submodule of the Xi'an Jiaotong University - China Xian XD Power Systems

In [30], a half-bridge submodule is designed. Its structure is the following: 2 IGBTs with a 3.3 kV blocking voltage and their anti-parallel diodes, a vacuum switch, a bypass thyristor. The submodule is water-cooled, the control uses fiber optics. It includes sensors for voltage and temperature measurements (used technologies not mentioned). A self-power block provides energy to the controller and to the vacuum switch from the capacitor of the submodule (structure not explained either). Figure 1.37 shows the structure of the submodule. Table 1.11 shows the specifications.

In this publication, the series-connection of two IGBTs is also studied but not tested in a real submodule. The voltage balancing between the two IGBTs uses an RCD clamp.

1.3.5.3 EPFL MMC Submodule

The Power Electronics Laboratory from École Polytechnique de Lausanne (EPFL) is working on MV MMC with 625 V submodules, based on 1200V IGBTs [114]. They developed a really interesting structure for their submodules. Their capacitors are, unlike many capacitors in the literature, electrolytic capacitors. It is possible because of the low voltage rating of their submodule. But even so, two 450 V capacitors must be connected in series to reach the desired voltage. The power module is based on IGBTs rated at 1200 V and 50 A. To reach either 50A or 100A in the MMC, their submodules can be reconfigured from FB to HB with IGBTs in parallel. Some other interesting features are developed due to their submodule structure: a hybrid balancing circuit – mix between a passive (resistors) and an active solution (switches) – to balance the capacitor voltages, an auxiliary submodule power supply using a flyback converter supplied from the SM's capacitors. Their simple power supply circuit is possible due to the relatively small voltage ratio between the capacitor's voltage and the voltage of the drivers and other devices. Their gate drivers use optocouplers. The circuit of their submodule is shown in figure 1.38.

Antiparallel thyristors offer a temporary bypass and a bi-stable relay is providing the perma-

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nent one (in case of fault of the submodule). In case an overvoltage occurs across the terminals of the submodule, transil over-voltage diodes become conductive (breakdown voltage of 900 V).

Table 1.12: Description of the EPFL submodule [114]

Characteristic	Description
Electronic Module	IGBTs 1.2 kV, 50 A, HB or FB
Bypass Thyristor	2 anti-parallel connected
Bypass Switch	Bistable Relay
Cooling system	Forced air ($45\,m^3\,h^{-1}$)
Operating Frequency	50 Hz
Switching Frequency	250 Hz
Capacitor	1.5 mF and 450 V each 2.25 mF and 900 V in total Hybrid balancing circuit
DC Voltage	625 V (rating) 900 V (max)
Current	50 A or 100 A (IGBT ratings)
Sensors	Temperature: NTC thermistance Current: Hall-effect sensor Voltage: resistive voltage dividers
Auxiliary Power Supply	From capacitor, with flyback converter
Gate driver	Optocouplers

Their work on MMCs is not limited to the conception of the submodule. They studied the electrothermal design of an MMC arm in [22], the galvanic isolation of an MMC in [20] and the insulation co-ordination for an MMC prototype in [19]. To sum it up, the submodule is cooled with forced air, and is located inside a metalic enclosure (aluminium), inside a drawer made of melamine/paper-based laminate (CTI of 600) to reduce creepage distance, inside a cabinet containing the 32 submodules of an MMC leg.

1.4 Conclusion of this review and research axes

In this chapter, the submodule and the MMC technologies have been assessed.The typical features, values, and design rules have been discussed using a consistent and complete bibliography. This thesis aims to improve the submodule itself, not the MMC control method or the design of whole MMCs. Therefore it has been decided to focus on semiconductor technology implementation improvement. With some semiconductors, it seems possible to remove some protection devices (with press-pack switches and diodes, for example), reducing the complexity of the submodule. The overall efficiency of the MMC, mainly related to semiconductor losses, could also be increased. The use of high voltage semiconductors would reduce the total number of submodules in the MMC. It has been decided to focus on the implementation of IGCTs in HVDC MMC submodules, as it will be explained in the next chapter.

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Chapter 2

IGCT in MMC Submodule – State of the Art, comparison with IGBTs and losses study

In this chapter, the interest of IGCTs as a switch in MMC submodules will be assessed, as well as its related disadvantages, the turn-on snubber in particular. In the two first sections the IGCT technology will be described, with a first section explaining the evolution from the thyristor to the GTO and then to the IGCT, and a second section, where the different types of GCTs will be discussed.

In the three following sections, the IGCT is compared to the IGBT in the HVDC MMC case. First, in the third section, a literature review on the comparison of the two switches in HVDC MMCs is carried out, including losses studies and a qualitative comparison. Then, in the fourth section, a specific comparison using original losses figures-of-merit created in this thesis is conducted. Finally, in the fifth section, a losses study is realized to confirm the interest of the IGCT compared to the IGBT and the interest of the newly developed figures-of-merit.

This chapter is concluded by the scientific locks and possible investigations related to the implementation of the IGCT in HVDC MMCs.

2.1 Thyristors semiconductor structures – evolution from SCR to GCT

This section is a deepening of the section 1.2.1 on thyristors, going into the semiconductor structure evolution from the SCR to the GCT.

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2.1.1 Thyristor (SCR)

A thyristor SCR is a P+N-PN+ semiconductor arrangement, which structure is displayed in figure 2.1a and symbol in figure 2.1c. The gate is on the P layer, the cathode on the N+ layer and the anode on the P+ layer. This combination of 3 junctions permits a reverse and a forward blocking capability. The thyristor is a switch turned-on with a current impulse in the gate. It turns itself off when the current through it extinguishes, but as long as current flows through it, it cannot be turned off. According to [67], it was described as early as 1956 and reached the market in the 1960s.

Turn-on The turn-on current pulse has the effect to overflow the P layer (orange in figure 2.1a) with electrons, and consequently this P part behaves like a N- layer: the thyristor becomes a PiN diode (which functioning is developed further in section 4.1). The SCR turn-on behaviour can also be explained by modeling it as the combination of two transistors PNP and NPN [5, 67] as displayed in figure 2.1b. A gate current impulse flows in the base of the NPN transistor, the NPN transistor starts to conduct, triggering the conduction of the PNP transistor. At that point even if I_G disappears, I_{C1} is maintaining the conductive state of the NPN transistor.

Turn-off From the transistor equivalent model can be understood how the SCR is turned-off: the current I_A stops, there is no more I_{B2} current flowing in the NPN transistor and it starts blocking.

Forward-blocking Forward blocking (V_{ak}>0) in the thyristor happens when no current impulse or a low current impulse take place: at that point, J2 is reversed-biased and the blocking voltage depends on the current impulse. As said in the previous paragraphs, the gate has the effect to transform the P layer into an equivalent N- layer. The bigger the current impulse is, the more this P layer is behaving like a N- layer, and the less the junction J2 can withstand voltage. With no current impulse, forward-blocking and reverse-blocking capabilities are similar.

Reverse-blocking Reverse blocking (V_{ak}<0) in the thyristor provokes J1 and J3 to be reversed-biased. But due to much lower N doping of junction J1 compared to the other doping levels (P+ of J1, P and N+ of J3), J1 is blocking most of the applied voltage with the electric field penetrating in the N- region.

2.1.2 GTO

According to [67], the GTO was first introduced in the 1980's. A few changes on the thyristor presented above permitted to allow turn-off capability. To design the GTO structure able to turn-off current, the turn-off gain $\beta = I_{a-max}/-I_g$ is defined (I_{a-max} the maximum anode current, I_g the negative current pulse needed to turn-off the thyristor). β has to be as big as possible (smallest I_g for biggest I_{a-max}) to make possible the design of the turn-off circuitry.

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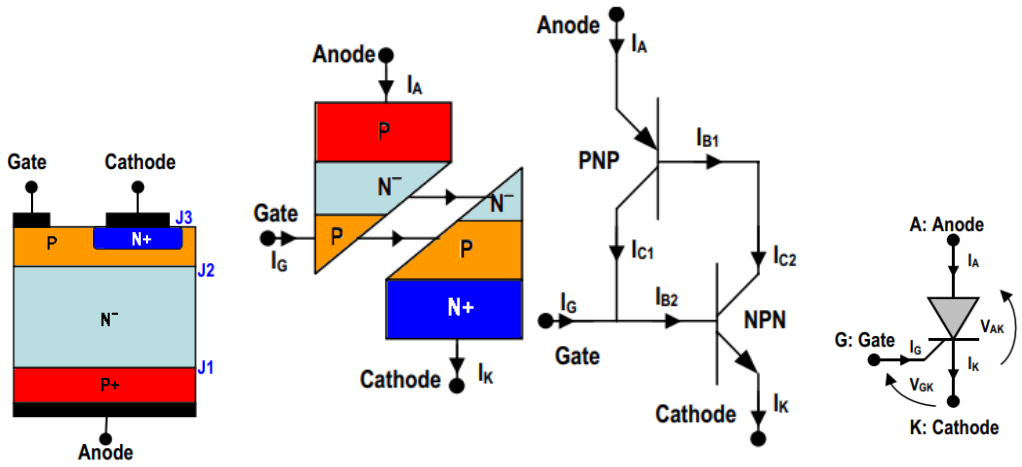

(a) Cross section. (b) Equivalent transistor schematic. (c) Thyristor symbol.

Figure 2.1: Thyristor semiconductor structure, symbol and equivalent transistors model. [5]

Using the transistor model of the thyristor, a high β can be attained with a high current gain of the NPN transistor and low current gain of the PNP transistor. A typical value of β is between 3 to 5. The turn-off current still being high (1000A for a β=3 and 3000A GTO), homogeneous turn-off across the GTO is necessary. This is achieved by implementing an interdigitated gate-cathode junction, with small cathode fingers, like displayed in figure 2.2b. A typical width of 100 to 300µm is mentioned in [67]. Increasing the doping of the P base (to a certain extent to avoid lowering too much the breakdown voltage of J3) and using N+ anode shorts (like displayed in figure 2.2a) are also improving the turn-off capability of the GTO [5, 8, 67]. However, the use of the anode shorts suppresses the reverse-blocking capability of the device.

But even with these upgrades, the turn-off takes a certain time: the NPN transistor part (like in figure 2.1b) blocks quickly but the anode still has current flowing through it after the NPN blocking. This current is called 'tail current' and takes more than 10µs to interrupts itself, leading to high turn-off losses. The GTO is sensitive to high dv/dt: a too high dv/dt value during turn-off before the current is totally interrupted would retrigger the GTO. The GTO is protected with a **turn-off** snubber (not the same as the turn-on snubber explained in section 2.3.3 and object of the study in the thesis) which main element is a capacitor to limit the dv/dt.

2.1.3 GCT

To avoid the problems due to the GTO turn-off, a fast turn-off is necessary, leading to the GCT and its hard-driven turn-off principle [35, 102]. The turn-off gain is 1 for a GCT ($|I_g| = |I_a|$), and to achieve this value the gate circuitry has to display very low inductance and resistance [67, 5]. These low values are attained by: a change in the housing of the GCT (lower inductance), paralleling MOSFETs and capacitors responsible for the current impulses in the gate drive circuit (lower inductance and resistance), using a PCB instead of a cable (lower inductance and resistance). The difference between the GTO and the GCT driver circuitry is illustrated in figure 2.4b. **The IGCT is the association of the GCT (the semiconductor and its**

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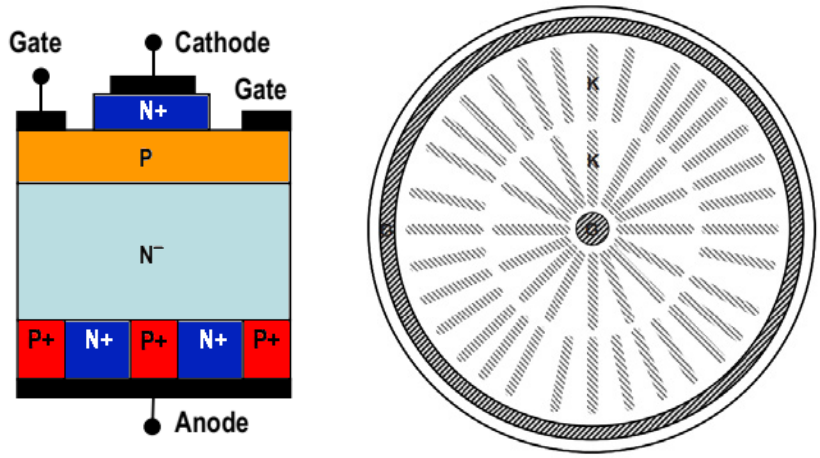

(a) Cross section with anode shorts. Adapted from [5].

(b) Interdigitated structure. [8]

Figure 2.2: GTO structure, illustrating anode shorts and interdigitated fingers.

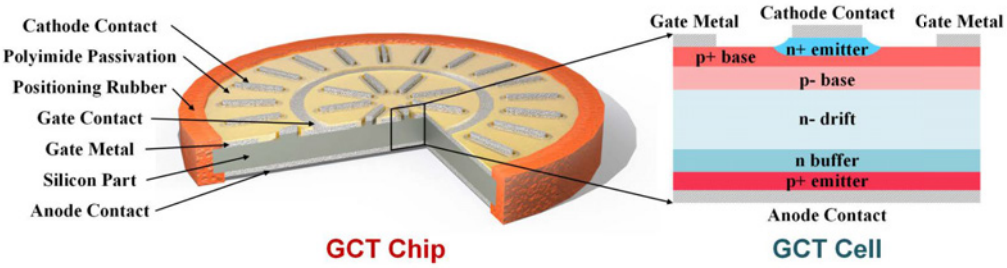

Figure 2.3: GCT wafer structure and associated semiconductor structure. [62]

housing) and the gate drive circuit, as shown in figure 2.4a.

The first trace of the hard-driven turn-off principle dates from 1996 [35]. With this turn-off process, there is no need for anode shorts like in most GTOs and therefore a N buffer layer can be used, these two being incompatible [102]. The use of the N buffer layer leads to lower drift thickness, producing lower conducting and switching losses and facilitating the integration of a diode on the same wafer. Like for the anode shorts, the N buffer layer does not permit a reverse-blocking capability of the device. There is also no need for dv/dt limiting turn-off snubber anymore. But if the IGCT is accompanied by a freewheeling diode, like in an MMC submodule, a turn-on snubber is needed, to protect the diode from high destructive di/dt. Indeed, without any external limiting element, the turn-on speed of the IGCT is not limited and cannot be controlled as in the case of the IGBT. This conclusion is also valid for a GTO. The turn-on snubber is composed of a di/dt limiting inductance, and an RCD clamp to reduce the overvoltage due to this added inductor. The turn-on snubber is discussed in more details in section 2.3.3.

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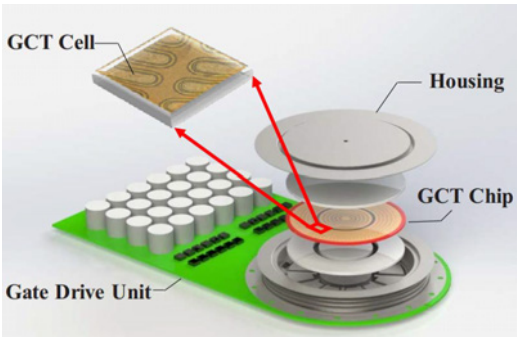
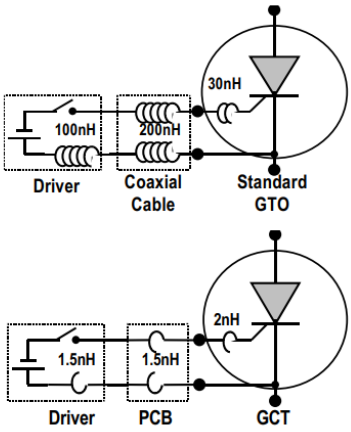
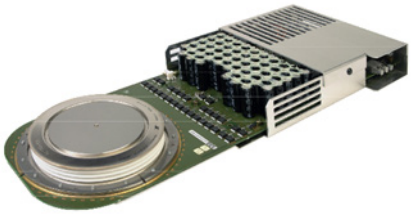


(a) IGCT structure (GCT + gate driver). [63]



(b) Difference between GTO and GCT drivers. [5]

Figure 2.4: IGCT structure with exploded housing view structure and difference on inductance gate driver loop with GTO.



(a) IGCT from ABB.

(b) IGCT from CRRC.

(c) IGCT from Mitsubishi.

Figure 2.5: IGCTs from different manufacturers, with their gate-drive circuits based on electrolytic capacitors. Sources: ABB, CRRC, Mitsubishi.

2.1.3.1 Commercially available GCTs and IGCTs

GCTs and IGCTs are produced and sold by at least 4 companies ABB, CRRC, Tianjin Century Electronics Co (TCEC) and Mitsubishi. The mostly found model is a 91-94mm wafer asymmetric IGCT (asymmetric IGCT is presented in 2.2.1.1). But some are just GCT (FGC6000AX-120DS from Mitsubishi), some are reverse-conducting (reverse-conducting IGCT is presented in 2.2.1.2), some are smaller (GCU15DB-130 from Mitsubishi), some are bigger (CAE 8000-45 from CRRC). The ratings can vary from 4.5 kV to 6.5 kV for the voltage, and from 400 A to 8000 A for the current. IGCTs from different companies can be seen in figure 2.5.

2.1.3.2 Typical Waveforms

Typical waveforms of the IGCT can be seen on 2.6.

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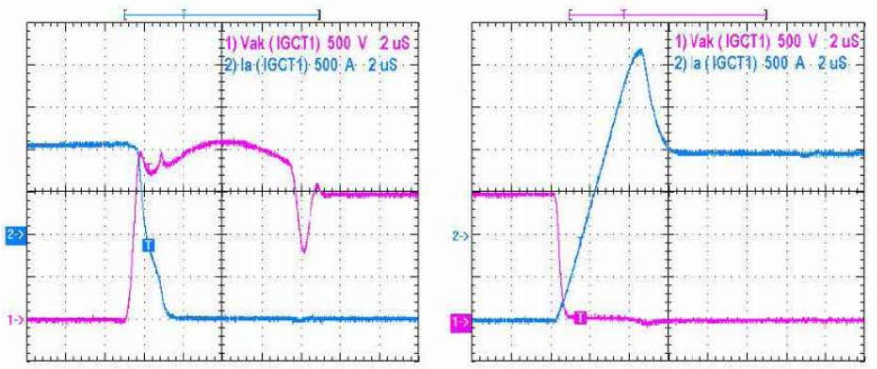

Figure 2.6: Waveforms of a 3.3kV IGCT at 2kA [5]: turn-off (left), turn-on (right).

2.2 The IGCT – types and functioning

2.2.1 GCTs Types

GCTs exist in different versions. Three types are commercialized: the asymmetric one (the main type that can be found), the reverse conducting and the reverse blocking one. Others can be found in the literature such as the Bi-mode IGCT (BGCT) but they are not currently available.

2.2.1.1 Asymmetric GCT

The asymmetric device cross-section and its top view can be found in Fig. 2.7. It is called asymmetric because it does not withstand voltage in both directions, due to its asymmetric profile (N buffer layer and P doping profile), unlike the symmetric IGCT presented in 2.2.1.4. Asymmetric IGCTs can differ from one to another on these points: their wafer size and their top layout (position of the gate contact and cathode segments placement). Most of the asymmetric IGCTs commercially found use 91 mm wafers with the gate contact region as displayed in 2.7b and a constant segment width. Recent work from ABB in [130] focuses on 94mm wafers with the gate contact region on the outer region of the wafer, and variable segment widths (standard segment width is 250µm). It seems this very recent work gave birth to the 5SHY 65L4521 and 5SHY 65L4522 models in the ABB catalog. There is also a trade-off between turn-off losses and conduction losses, as it is illustrated in figure 2.8. Some bigger asymmetric IGCTs can be found in the CRRC catalog (model CAE 8000-45, with a GCT diameter of 130mm, compared to 85mm for the CAC 4000-45), leading to an even greater current (8kA for the CAE 8000-45 compared to 4kA for the CAC 4000-45).

2.2.1.2 Reverse-Conducting GCT

A first trace of the reverse conducting (RC) GCT can be found in [51, 59] in 1997. The RC-GCT includes an anti-parallel diode on the same wafer as it can be seen in Fig. 2.9. New RC-IGCT

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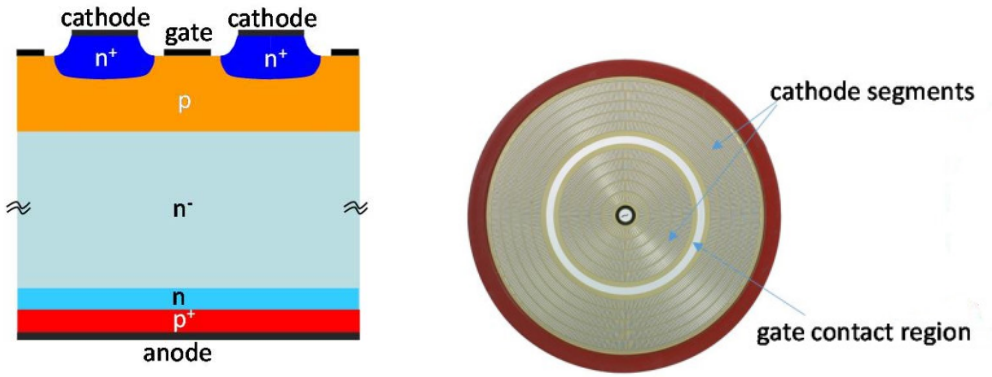

(a) Cross section of the GCT (b) Top-view

Figure 2.7: Asymetric GCT device: cross-section and top view of a 91 mm wafer [118]

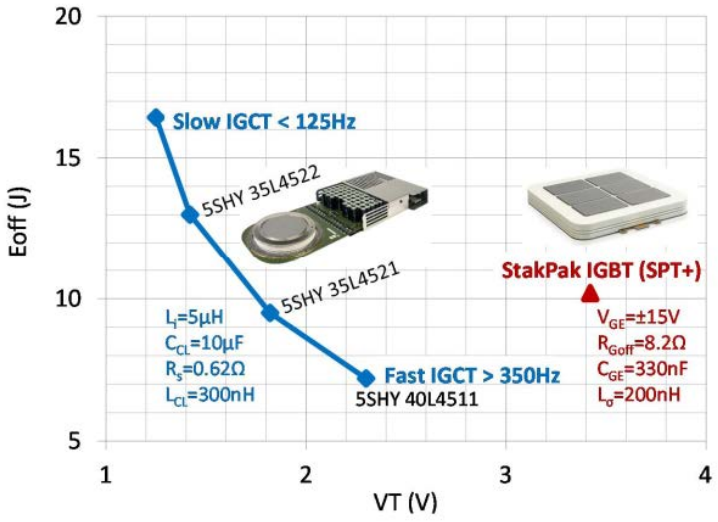

Figure 2.8: A technology curve comparison [118]

are being developed, on 94 mm wafers like in [120] or 150 mm wafers like in [129]. They have been proved to work at 4.7kA/5.3kV and 9.5kA/2.8kV respectively. The advantage compared to the asymmetric IGCT is that there is only one housing for GCT and diode parts (two for asymmetric IGCT + diode) reducing the pressing clamp size and the commutation cell size. But it leads to a reduced GCT-area, and therefore a reduced current level capability.

2.2.1.3 Bi-mode GCT

This type of GCT is similar to the RC-GCT in principle. Indeed, the wafer of the BGCT is a combination of a GCT with an antiparallel diode. The difference, as it can be seen in figure 2.10 is that the diode is interdigigated with the GCT. It is as if plenty of GCT and antiparallel diode segments-associations were put in parallel, while the RC-IGCT has a one monolithic diode. The advantages of the BGCT compared to the similar RC-IGCT are: a better current capability for the same area, a better heat repartition, a softer reverse recovery and a lower leakage current. [117, 118, 116] Not available commercially at the time of the writing of this thesis.

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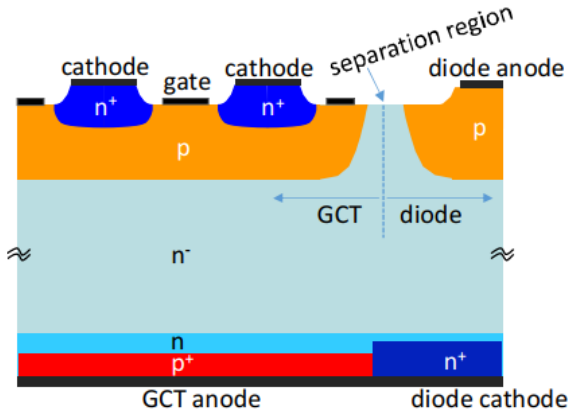
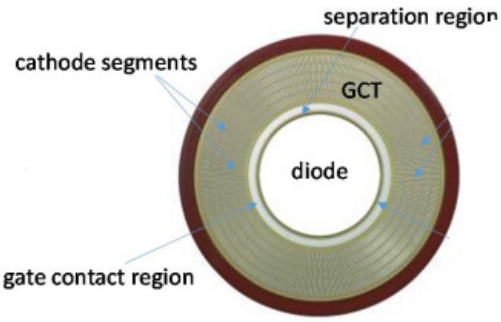
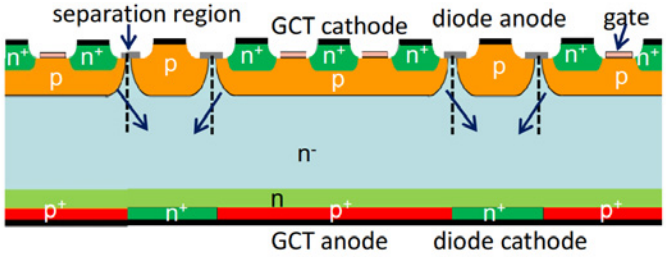


(a) Cross section of the RC-GCT [100]

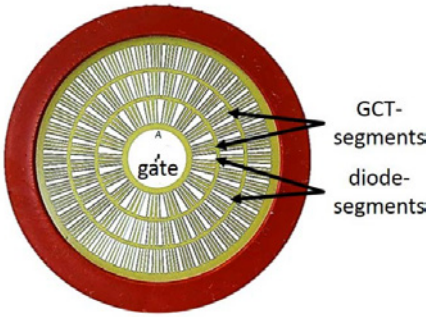


(b) Top-view [118]

Figure 2.9: RC-IGCT device: cross-section and top view of a 91 mm wafer [118]



(a) Cross section of the BGCT [116]



(b) Top-view of the BGCT [118]

Figure 2.10: The bi-mode GCT: cross-section and top view of a 38 mm wafer [118, 116]

2.2.1.4 Reverse-Blocking/Symmetric GCT

This type of IGCT was developed more than 20 years ago [127, 46] and is sold only by Mitsubishi at the time of the thesis. Such configuration can be obtained by connecting an asymmetric IGCT in series with a diode [118], which could explain the low quantity of manufacturers. Such an IGCT would be useful for Current Source Converters [127] or circuit breakers. [115] The reverse blocking characteristic is obtained by removing the N layer buffer (implying more losses by conduction and switching) and modifying the P doping profile in the GCT compared to asymmetric GCT. The symmetric device cross-section can be seen in Fig. 2.11. The top-view of the RB-IGCT is the same as the top view of the asymmetric IGCT (see Fig. 2.7b).

2.2.1.5 The future of IGCTs

Although the market size of IGBTs is much larger than that of IGCTs (5 G$ vs. 10–15 M$ in 2019 (Sources: Allied Market Research, Reuters), the IGCT is still evolving in many ways. Larger GCTs (6' wafer diameters) have been demonstrated to reach higher current by ABB (up to 9.5kA max turn-off current at 125°C) [129] and CRRC (up to 8kA max turn-off current at 125°C) [17], the latter being already in the manufacturer's catalog. Higher voltage ratings are

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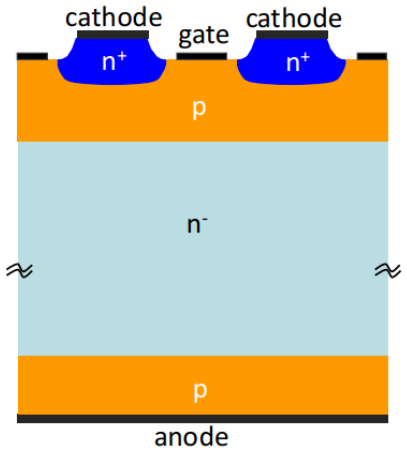

Figure 2.11: Cross section of the RB-IGCT [118]

also reached with a 10 kV RC-IGCT in [120] (ABB). Other current and future improvements of the IGCTs are developed in [118]: improved thermal performance and reduced conduction losses (getting closer to 1 V in the on state like in [92, 62]) for the current developments; bi-mode GCT (BGCT); reduced turn-off losses for the future developments. Those trends are summarized on the figure 2.12. In [119], a change of the structure from a trench gate structure to a planar gate structure is studied and might be found more often in the future because, according to [119], it would make the manufacturing easier.

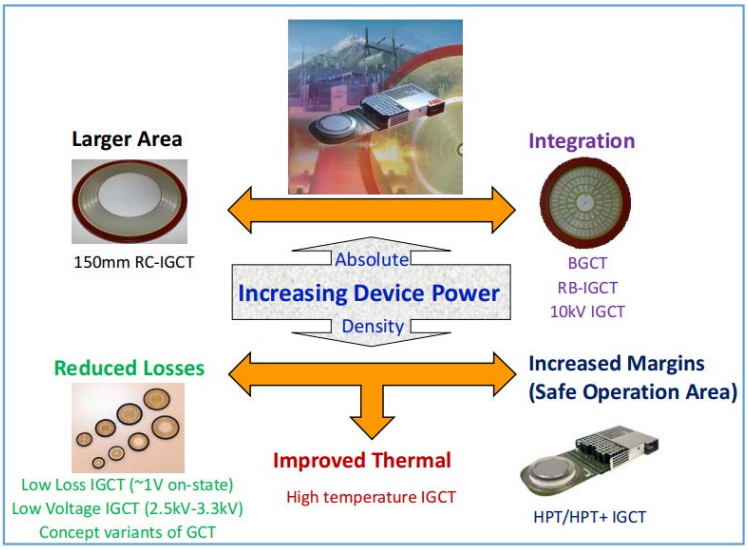

Figure 2.12: Trends for improvements of GCTs and IGCTs according to ABB [118].

Although it is often difficult to estimate the maturity level of a research prototype and the corresponding time to market, it must be noticed that most publications on the topic are based on experimental results at high current/voltage ratings. Furthermore, the current IGCTs are the results of several iterations. For example, ABB introduced their "High Power Technology" (HPT/HPT$^+$) platform in 2010 to improve avalanche robustness, turn-off current capability, and extend the junction temperature range [118].

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2.2.2 Gate Drive Circuit functions and parts

The GCT is a current-driven switch. The gate drive circuit of the IGCT is then very different from the one of the IGBT and is described in this section.

Because of the need for a control loop with a very low inductance, as said in sections 1.2.1 and 2.1.3, GCTs are often proposed with an attached gate control unit. The IGCT is a GCT combined with its gate-drive circuit. IGCTs from different companies can be seen in figure 2.5. The gate-drive circuit has three functions [35]: to ensure turn-on, turn-off but also to keep the GCT in the on-state (with a few amperes, up to 15 A). An illustration of the main functions of the gate-drive circuit of the GCT can be seen in figure 2.13. The power supply of the gate-drive circuit is, according to [52], usually provided by a DC/DC converter. Some additional features can be added, such as short-circuit detection. Among other components, the gate-drive circuit comprises a large capacitor bank (in a range of 40mF [52], to 150mF [17], for electrolytic capacitors) and low voltage MOSFETs permitting the charge removal at turn-off. Designed to reach the lowest possible stray inductance, the driver board of a 6-inch device was found to reach inductances as low as 0.4 nH (classic gate circuit) or even 0.04 nH (optimized gate circuit), to be compared with $\approx$ 1 nH of stray inductance due to the GCT housing itself according to [17]. The resistance of the gate circuit is between 0.2 and 0.5 mΩ according to [17] as well. Such low values are required to sustain the high $\frac{dI_G}{dt}$ and I_G values during turn-off (in [34] 6kA and 12kA/µs values are displayed during turn-off). The maximum current going through the gate corresponds to the maximum controllable turn-off current of the GCT. The turn-on gate current is lower: according to [78], this value is around 200 A (duration of 5 µs). Finally, the gate driver unit of an IGCT typically consumes a power of 20–100 W (depending on the IGCT part number and switching frequency), about one order of magnitude higher than the gate driver of an IGBT with comparable ratings. The possible improvements of IGCT gate drive units are discussed in section 2.6.2.

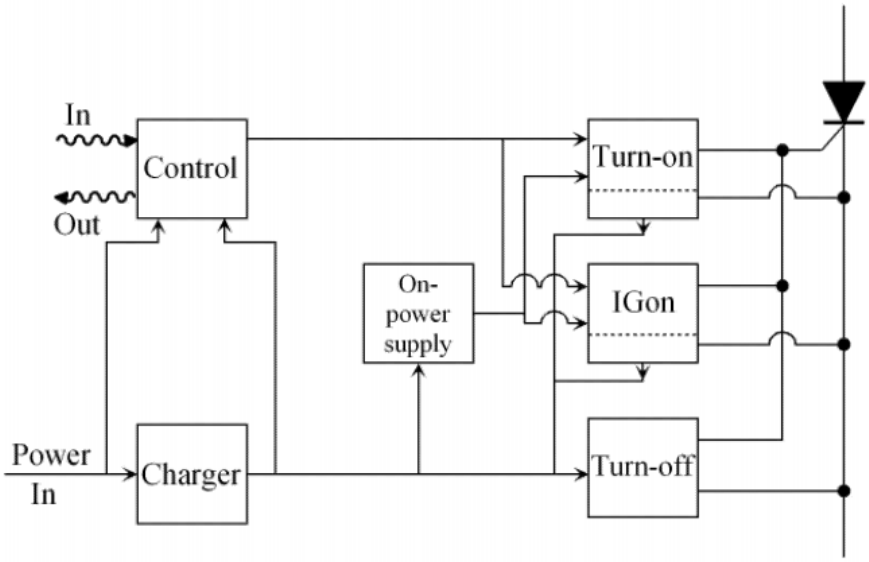

Figure 2.13: Gate-drive circuit main functions [34]

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2.3 Comparison of IGCTs and IGBTs in MMCs – a literature review

In this section, we compare IGBTs and IGCTs in the case of an MMC application, based on the literature. Only IGBTs packaged in Press-Packs (PP) are considered, as they are expected to offer a short-circuit failure mode – which is desirable in HVDC converters, see subsection 1.2.1 – just as the IGCTs.

2.3.1 General considerations and features to compare

The ratings of some commercially available IGCTs and press-pack IGBTs are displayed in Tab. 2.1. Note that it is difficult to perform a fair comparison, as IGBTs and IGCT current ratings differ sensibly. For the IGBTs, the current is defined in the datasheets as the "DC Current". The "peak current" is also given and is often the double of the "DC Current". For the the GCTs, three currents are given: the "maximum controllable turn-off current", the "maximum RMS on-state current" and the "maximum average on-state current".

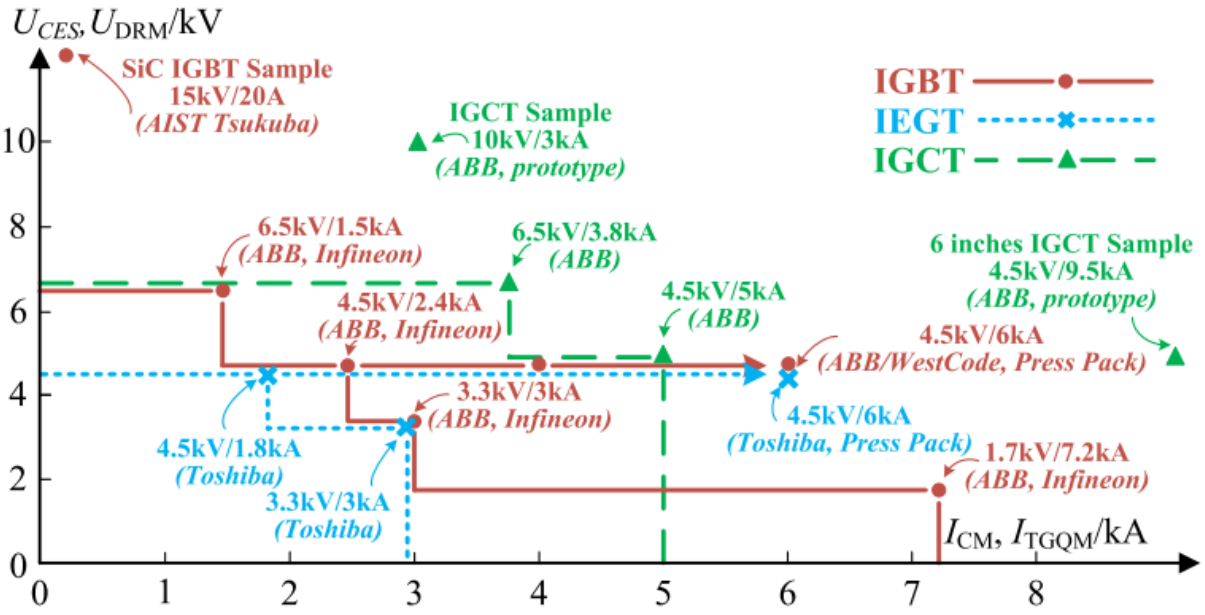

Figure 2.14: Maximum ratings of semiconductors in 2017 according to [18]. Note that some noticeable devices are missing, such as a 6 kV, 6 kA GCT from Mitsubishi.

In the literature, the Fig. 2.14 – or similar – can be found: it displays the maximum ratings of different semiconductors devices (either currently available on the market or described in other publications). We can see that the IGCT offers the highest ratings when compared to IGBTs or IEGTs. However, this graph suffers from one major weakness: it uses the "maximum controllable turn-off current" for the IGCTs, and it might not be the proper figure to use in the case of an MMC. To provide a better comparison between IGBTs and IGCTs, a new current metric is introduced in section 2.4.1.3. Using this new metric, and including a few devices which have been introduced since, an updated version of figure 2.14 is in proposed in figure 1.16.

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Table 2.1: Ratings of 2 press-pack IGBTs and 2 IGCTs

Type (company)	**IGCT (ABB)**	**IGCT (CRRC)**	**IGBT PP (ABB)**	**IGBT PP (Dynex)**
Model	5SHY 35L4520	CAC 4000-45	5SNA 2000K450300	DPI2100P45A5200
Blocking Voltage	4.5 kV	4.5 kV	4.5 kV	4.5 kV
Max. turn-off current	4 kA	4 kA	-	-
Av. on-state current	1.7 kA	1.7 kA	-	-
DC current	-	-	2 kA	2.1 kA
Turn-on energy				
@ 2.8 kV, 125 °C	1.5 J (4 kA)	1.5 J (4 kA)	11 J (2 kA)	11 J (2.1 kA)
	-	-	5.5 J (1 kA)	5 J (1 kA)
	-	-	-	10.5 J (2 kA)
Turn-off energy				
@ 2.8 kV , 125 °C	19.5 J (4 kA)	23 J (4 kA)	10.5 J (2 kA)	11 J (2.1 kA)
	5 J (1 kA)	6 J (1 kA)	5.5 J (1 kA)	4.5 J (1 kA)
	10 J (2 kA)	12 J (2 kA)	10.5 J (2 kA)	10.5 J (2 kA)
On-state Voltage				
@ 2.8 kV, 125 °C	1.5 V (1 kA)	1.7 V (1 kA)	2.4 V (1 kA)	1.9 V (1 kA)
	1.8 V (2 kA)	2.1 V (2 kA)	3.4 V (2 kA)	2.8 V (2 kA)

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Table 2.2: Loss studies results comparing IGCTs and IGBTs in HVDC MMCs.

Publication	Total losses IGBT (%)	Total losses IGCT (%)	Inverter or rectifier	Losses reduction (%)
[76]	0.48	0.41	Average rectifier and inverter	14.6
[36]	0.64 (StakPak)	0.44	Rectifier	31
[36]	0.32 (StakPak)	0.27	Inverter	15.6
[138]	0.76 (PressPack)	0.74	Rectifier	2.6
[138]	0.83 (PressPack)	0.64	Inverter	22.9

Table 2.3: Ratings of the MMCs considered in the investigations of converter losses in the literature.

Publication	Power rating (MVA)	Cell volt. (kV)	DC Volt. (kV)	Nbr of SMs per arm	Arm Cur. (kA)
[76]	1100	-	±320	286	1.7
[36]	100 to 500	2.5	±160	64	
[138]	600	2.2	±320	145	

The cost of a press-pack IGBT is estimated to be twice as much of that of an IGCT according to [137], mentioning the simple processing and high yield of the IGCT. In [54], a cost comparison analysis is also carried out and finds out that, according to the article model, the IGCT has a lower capital cost per MW, a slightly higher life-cycle cost, and a better reliability than press-pack IGBT (the Stakpak from ABB was considered in this publication).

The IGCTs exhibit the following apparent advantages: lower losses, lower cost, higher ratings than the IGBTs. It has also a short-circuit failure mode, very appreciable in HVDC MMCs. Theses advantages will be discussed all along this section.

IGCTs also exhibit drawbacks, which may explain that the device was excluded from the first generation of HVDC MMC submodules. As this device does not offer any way to control the current transients during switching, they need to be equipped with a turn-on snubber circuit (discussed in chap. 2.3.3). Also, it requires a complex gate unit, due to the large capacitor bank, low inductance and high-current capability required to control the device. The snubber adds losses, complexity, volume and cost to the submodule. On the contrary, the low switching frequency capability of IGCTs is not a problem in the case of MMCs, which operate at low frequency (70 to 300 Hz), regardless of the technology of their switches.

2.3.2 Losses studies in literature

Several studies [138, 36, 76] focus on comparing IGCTs with other semiconductors devices in the case of MMC submodules. [36, 76] use average model, while [138] uses a model to reproduce the dynamic of the submodules – modelling each submodule with realistic waveforms. All of them take into account the losses generated by the snubber. The results of these papers are summarized in Tab. 2.2, and the ratings of the corresponding MMCs are listed in Tab. 2.3. As a result, among all the semiconductors ([138] considers four different types, [36] compares 2 IGBTs with an IGCT) the IGCT solution is always the one with the lowest losses. Also, it can

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be seen that the losses are very much dependent on the operation point, the MMC ratings, the control method (influence on switching frequency and therefore on switching losses) and other parameters of the model.

Some detailed results of the loss calculations in [138] can be seen in figure 2.15. Among the semiconductors (IEGT module and press-pack, IGBT module and press-pack), the IGCT has the lowest losses. The snubber only adds a small contribution to the losses. Comparable results for [36] can be seen in figure 2.16 and for [76] in figure 2.17. In all cases, the MMCs using IGCTs are found to have the best efficiency.

The IGCT displays lower losses in these studies due its comparable switching energies and lower on-state voltage compared to the IGBT, as it will also be discussed in sections 2.4 and 2.5. In [36, 138], the press-pack IGBTs display lower losses, but it could be because the semiconductor structures inside (doping, thicknesses...) are different rather than the package type has an impact on the losses.

2.3.3 A focus on the turn-on snubber and the associated literature

2.3.3.1 Why is a turn-on snubber needed

While the switching speed of an IGBT can be controlled through the current supplied by its gate driver, the IGCT offers no such control feature. Once initiated, the IGCT turn-on is a self-sustained process, with a positive feedback which makes it very fast. Although such fast turn-on is desirable to reduce switching losses, it may cause an excessive burden on the semiconductor switches and in particular on the opposite diode (in a Half-Bridge configuration). As a consequence, a turn-on snubber is recommended to limit the turn-on speed to a value usually lower than $1\,\mathrm{kA\,\mu s^{-1}}$. In sections 2.3.3.2 and 2.3.3.3, we study the consequences of an excessive turn-on speed on the diode and IGCT respectively.

2.3.3.2 di/dt limitations due to the freewheeling diode during diode turn-off

For ABB and for most of the papers about IGCTs [5, 15, 27, 36, 37, 77, 100, 120], the reason why a di/dt snubber is needed is to ensure the diodes D_1 and D_2 (Fig. 2.18) remain in their SOA while they are turning-off. If no snubber (corresponding to components L_I, D_{CL}, C_{CL} and R_S in Fig. 2.18b) is installed, the di/dt at turn-on for the IGCT is only limited by the stray inductance of the power loop (L_S in Fig. 2.18b). In [128], it is shown that without snubber, the value of di/dt can then reach up to $20\,\mathrm{kA\,\mu s^{-1}}$.

Very fast diode turn-off transients cause a large negative recovery current to flow through the diode. Because of thermal effects, large recovery currents are not uniformly distributed over the diode surface, making it possible for current filamentation to occur. This causes the diode to fail, and may even yield to explosion of the package, as shown in figure 2.19 [128]. The maximum acceptable turn-off speed is a characteristic value for a given diode. For example, while $20\,\mathrm{kA\,\mu s^{-1}}$ is way too high a value, many diodes can withstand $1\,\mathrm{kA\,\mu s^{-1}}$, and some can achieve up to $5.2\,\mathrm{kA\,\mu s^{-1}}$, like in [128, 137] (for example the ABB diode 5SDF 28L4521).

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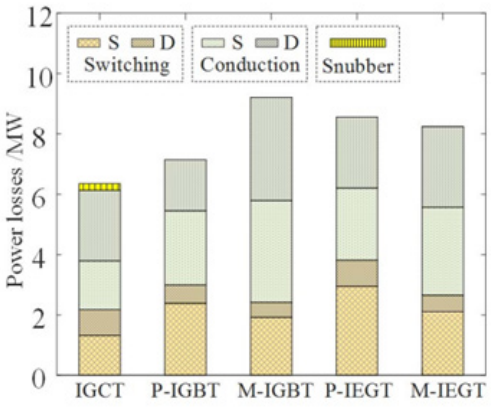
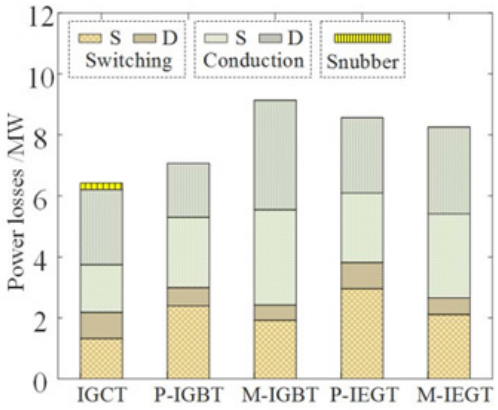
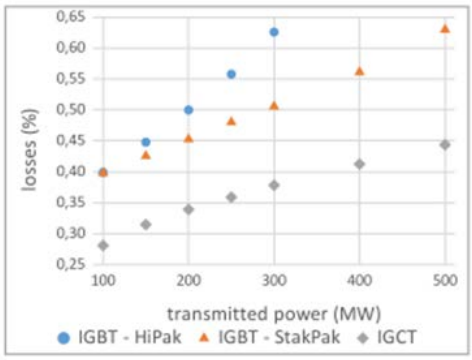


(a) Inverter situation losses

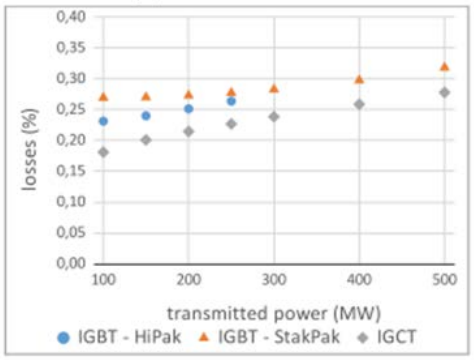


(b) Rectifier situation losses

Figure 2.15: Losses estimation for the semiconductor switches of the 600 MVA converter in Tab. 2.3, as a function of the switch technology [138]. M: plastic module. P: press-pack.



(a) Inverter situation losses



(b) Rectifier situation losses

Figure 2.16: Losses estimation for the semiconductor switches of the 500 MVA converter in Tab. 2.3, as a function of the switch technology [36].

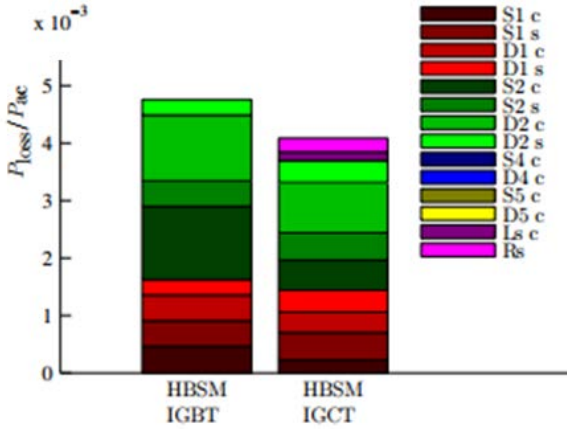


Figure 2.17: Losses estimation for the semiconductor switches of the 1100 MVA converter in Tab. 2.3, as a function of the switch technology [76]

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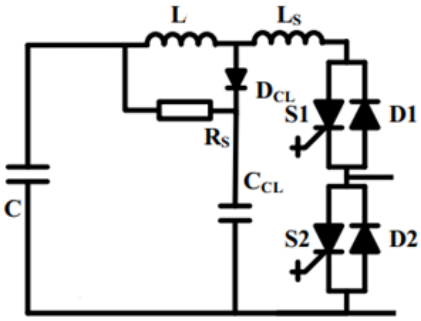
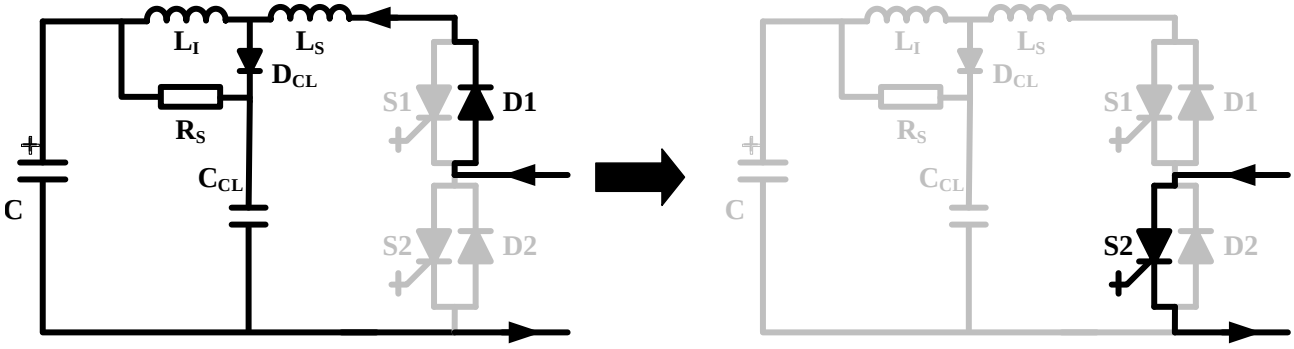


(a) IGCT-based submodule with snubber circuit.



(b) Switching sequence: before lower IGCT turn-on, current is flowing through the upper diode; after it flows through the lower IGCT, forcing the upper diode to turn-off.

Figure 2.18: IGCT based submodule and associated switching sequence illustrating the role of the snubber circuit. [128].

2.3.3.3 di/dt limitations due to the GCT during GCT turn-on

Even though most of the papers focus on the diode di/dt limit, some papers address the intrinsic limits of the IGCT at turn-on. The di/dt limit of the IGCT is due to the physics of its turn-on process (therefore of the semiconductor part, i.e. the GCT), which is as follows: a current is injected through the gate to turn the gate-cathode junction on. As a consequence the GCT starts to conduct current through a small area around the gate. This conduction area grows at a finite speed, by $0.1\,\mathrm{mm\,\mu s^{-1}}$ according to [137]. This statement about the growing rate was only found in one paper for the GCT, it corresponds to the same speed as other thyristors according to [67] (0.05mm/µs to 0.1mm/µs) or [8] (0.05mm/µs). If the di/dt is too high, only a small area around the gate circuit will conduct a lot of current, resulting in area dissipating a very high power density and in a very localized heating. This presents a risk of thermal runaway which would destroy the device [137]. Despite the very fast turn-on capability of the IGCT, the limited rate of growth of its conducting area during the current rising phase is therefore imposing a limit on the di/dt that it can handle. In other words, nothing in the IGCT (GCT part or gate drive circuit) itself is limiting the rise of the current during the turn-on process, but the rise of the current has to be limited to avoid the destruction of the GCT.

The di/dt limit value for the IGCT, described in the previous paragraph, depends on the gate current delivered by the gate driver (I_G, $\frac{dI_G}{dt}$). According to [2], a large gate current I_G ensures that all IGCT cathode segments are turned on simultaneously. This leads to an

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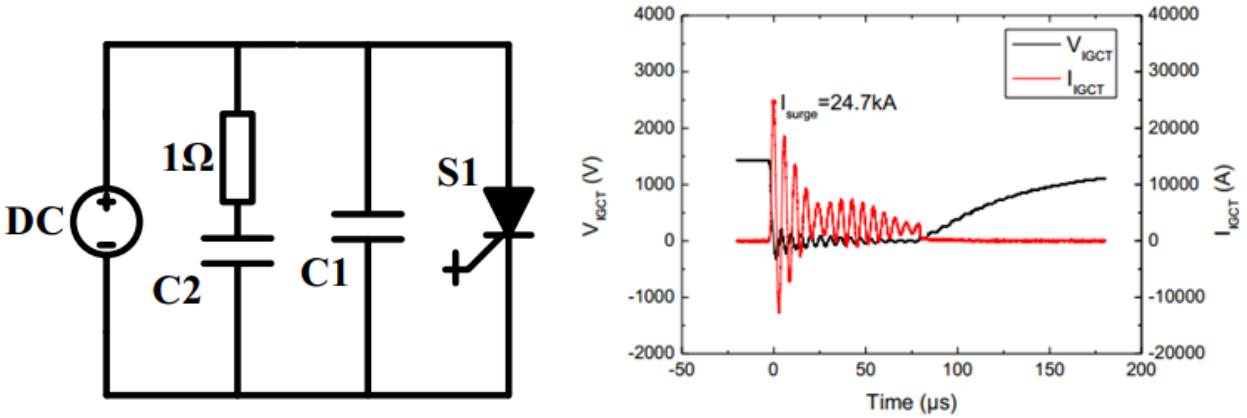
Figure 2.19: Diode exploded due to too high di/dt [128]

uniform conduction and avoids localized and concentrated conduction areas. Thus, an IGCT can be tuned to support higher di/dt values at turn-on. The only paper that has been found which explores the IGCT's intrinsic di/dt limits [128], demonstrates that an IGCT can handle up to $19.3\,\mathrm{kA\,\mu s^{-1}}$ without failure. And even though the test presents problems like its non-representative waveforms (oscillatory current rather than hard switching operation), this shows that IGCTs have intrinsically high di/dt capability. The test circuit and the resulting waveform for $19.3\,\mathrm{kA\,\mu s^{-1}}$ can be found in figure 2.20. The di/dt limit value is quoted in the datasheets at around $1\,\mathrm{kA\,\mu s^{-1}}$ [2, 137, 128], but do not state whether this limit is actually that of the recommended diode or of the IGCT. Also this value (way smaller than $19.3\,\mathrm{kA\,\mu s^{-1}}$) may takes into account the reliability of the IGCT: at higher di/dt the operation lifetime may be reduced, due to repeated localized non-destructive hotspots during commutations. But the impact of di/dt on the IGCT lifetime is hard to compute without precise semiconductor simulations.

In a nutshell, the IGCT has a di/dt limit at turn-on, but this limit seems much further away than the di/dt limit of the diode at its turn-off (corresponding to the IGCT turn-on), with the current diodes and IGCTs available on the market.



(a) Test circuit: single-pulse

(b) Obtained result

Figure 2.20: di/dt test for IGCT [128]

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2.3.3.4 Snubber design

To limit the di/dt at turn-on, an inductor is connected in series with the IGCT. It is simply calculated with the maximum voltage of the submodule and the di/dt limit, as follows.

$$L_{snubber} = \frac{V_{SM}}{\frac{di}{dt}_{max}} \tag{2.1}$$

But the IGCT snubber is not limited to a single inductor. A capacitor is connected to the inductor through a diode to absorb the energy stored in the inductor when the IGCT turns-off. A resistor is then used to dissipate that energy before the next switching cycle. This classic turn-on snubber circuit can be seen in figure 2.18a. The selection of suitable capacitor and resistor is developed in [135]. The stored energy in the snubber is the energy in the inductor with the current at turn-off ($\frac{1}{2}LI^2$). As it can be seen in Tab. 2.4, this energy can range from 0.64 J (L=0.3 µH and I=2 kA) to 20 J (L=10 µH and I=2 kA). A simple analysis on the size of the snubber elements is carried out in the next subsection. The large spread in the inductance values (from 0.32 µH to 11.5 µH) means that the inductor can be anything from a small copper plate (see figure 2.21) to a big and bulky winding.

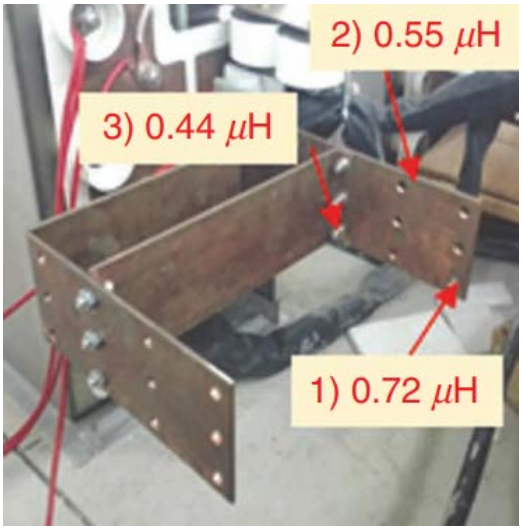

Figure 2.21: Inductor optimisation in [137]

2.3.3.5 Literature review on IGCT snubbers

Table 2.4 displays a decent number of studies that deal with the turn-on snubber matter but also all the studies modelling or testing IGCTs with a freewheeling diode. The ratings of the devices used in those studies (snubbers devices and IGCTs) are displayed to give an overview on typical values that can be encountered.

The estimated volume due to the snubber in the table is calculated being the sum of $V(L_{snubber})$ (calculated with eq. 2.2, valid for cylindrical inductors) and $V(C_{snubber})$ (calculated with eq. 2.3), N/l is the number of turns per length unit. For the calculations in table 2.4, N/l= 100 turns/m, μ_r=1 (air inductor). The inductor would be reduced using magnetic core

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but the aim of this subsection is to give a volume estimation, not to achieve the minimal volume optimisation. In eq. 2.3) D_{E-capa} is the energy density of the capacitor, it has been chosen for calculation to be 50J/L (corresponding to the snubber capacitor used in experimental setup of the thesis, see chapter 3).

$$V(L_{snubber}) = \frac{L_{snubber}}{\mu_0.\mu_r.(\frac{N}{l})^2} \tag{2.2}$$

$$V(C_{snubber}) = \frac{C.U^2}{2.D_{E-capa}} \tag{2.3}$$

As it is analysed in chapter 3, these values do not correspond to the real volume occupied by the snubber in the submodule because it does not take into account the physical arrangement, clearance/creepage distances or potential cooling (like [137], where an air core inductor with water cooling is displayed). It does not take into account the snubber diode or the snubber resistor either, which can require cooling themselves. Such a precise analysis, taking all these factors into account, would require a complex model. But what these volume calculations do illustrate, is a tendency on space occupation and that an optimised snubber can lead to a volume reduction: from 1.8L to 0.3L for 4.5kV IGCT in the table 2.4 (6 times smaller). Because this calculated volume underestimates largely the volume, it can be estimated that for 6.5kV IGCT, the snubber volume represents at least 3.4L (see table 2.4).

2.3.4 Conclusions and limits on this literature review

The IGBT and IGCT both display qualities regarding their use in HVDC MMCs submodules. The IGCT seems, according to studies, to produce lower losses, but these losses are calculated for a specific MMC, a specific control method and a specific device (the studies almost only consider one type of IGCT and one type of press-pack IGBT). An attempt to compare efficiently IGCTs and IGBTs in the HVDC MMC case in a non-specific and general approach, will be carried out in the next section.

On the other hand, the IGCT is intrinsically a very fast semiconductor device. At turn-on, this switching speed exceeds the capability of the diodes currently available (and, to some extent, the capability of the IGCT itself). As a consequence, a turn-on snubber circuit is used in all the circuits we could find.

However, fast diodes that can sustain much faster current transients than usually considered ones exist ($>5\,\mathrm{kA\,\mu s^{-1}}$ instead of $<1\,\mathrm{kA\,\mu s^{-1}}$, as is usually considered). This means that the turn-on snubber can be reduced substantially. In particular, its main element (the inductor) may have inductance values as low as 320 nH, at which point it is comparable to the stray inductance of the interconnects in an MMC submodule.

The turn-on snubber will be one of the focus points of this thesis work, and its reduction and removal will be discussed and tested experimentally in the chapters 3, 4 and 5.

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Table 2.4: Analysis of publications dealing with IGCT snubbers as a main or a secondary topic. (est.) stands for estimation (based on the ratings of the device and the snubber inductance). FWD: Freewheeling diode, RR: Reverse Recovery.

Ref.	IGCT Volt. Rating (kV)	di/dt value (kA μs^{-1})	Snubber/clamp inductor presence reason according to Ref.	Snubber Induct. (µH)	Snubber Res. (Ω)	Snubber Cap. (uF)	Snubber Vol. (L)	Pub. date
[2]	4.5	0.2 to 1	- FWD Diode RR mainly - For really high di/dt also possible hot spots and destruction of IGCT					2016
[5]	3.3	0.2 to 1	FWD Diode RR	1.5	0.75	6	0.4	2005
[15]	4.5	0.75	FWD Diode RR					2001
[27]	4.5	0.2 to 1	FWD Diode RR	5	0.65	10	1.2	2008
[36]	4.5	1.2	FWD Diode RR	2.5	0.3	20	1.8	2019
[37]	4.5	1.2	FWD Diode RR	2.5	0.3	20	1.8	2019
[77]	6.5	1 to 2 (est.)	FWD Diode RR	1.8 to 3	0.35	20	3.4	2018
[100]	5.5	0.51	FWD Diode RR	6.5	0.77	7.6	1.3	2012
[101]	4.5		- FWD Diode RR - Surge withstand of semiconductors?					2000
[120]	10	0.5 (est.)	FWD Diode RR	10	1.25	4	2.2	2019
[128]	4.5	optimal: 5.2	- FWD Diode RR - For really high di/dt, hot spots and destruction of IGCT	optimal: 0.32	0.2	10	0.8	2018
[135]	4.5	0.2 (est.)		11.5	2	2	1.1	2014
[137]	4.5	optimal: 5.3	- FWD Diode RR - For really high di/dt, hot spots and destruction of IGCT	optimal: 0.44	0.2	4	0.3	2019
[138]	4.5	3 (est.)		0.6	0.76	3.8	0.3	2019
[139]	4.5	3 (est.)		0.6	2	4	0.4	2020
[65]	4.5	3 (est.)		0.6	0.4	6	0.5	2020
[129]	4.5	2		1 to 2				2014

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2.4 Developing a comparison between IGCTs and IGBTs through the creation of Figures-of-Merit and a current metric

2.4.1 Current Metric for comparison of current ratings

2.4.1.1 Impossibility to compare current ratings of IGBTs and IGCTs

As described in section 2.4.1.3, many values are quoted in the datasheet of a semiconductor switch regarding the on-state current it can manage. These current values and those introduced in this section are described in table 2.5. For the IGCT, none of them can directly and simply be linked to the MMC operation, unlike for the IGBT (for which the dc-current rating on the IGBT datasheet, $I_{dc-igbt}$, corresponds to the maximum current going through the semiconductor during MMC operation, $I_{max-semi}$). As a consequence, the suitability of an IGCT for a given MMC cannot be assessed directly, and no direct comparison can be done between IGBTs and IGCTs.

2.4.1.2 Creation of the current metric

Thus, a new current metric ($I_{eq-IGCT}$) has to be defined to compare efficiently IGCTs and IGBTs current capabilities. This new current metric should correspond to a generic MMC case (it is not specific to one MMC implementation in particular) and has of course to be based on data available in the IGCT datasheet. The goal is to build a current metric comparable to the dc-current quoted in IGBT datasheets $I_{dc-igbt}$, considering the actual current waveforms in an MMC.

The worst case for the IGCT – i.e. when the IGCT is subjected to the maximum possible current – is when the submodule is inserted for an entire ac period. Considering the asymmetric operation of the MMC (because arm currents have DC and AC components), one of the IGCTs will be subjected to stronger current than the other. These IGCTs currents have their waveforms drawn in figure 2.22, assuming the current of the ac output of the MMC is perfectly sinusoidal. It can be seen that this waveform is close to a 50 Hz half-sine. The adopted approach is to calculate the average current of that waveform in the general case and link it to the maximum current value of the same waveform, i.e. finding a relation between $I_{av-semi}$ and $I_{max-semi}$. By establishing this connection between $I_{av-semi}$ and $I_{max-semi}$, and based on $I_{av-IGCT}$ we can introduce $I_{eq-igct}$, which is the equivalent for the IGCT of the dc current for an IGBT ($I_{dc-igbt}$, quoted in the device datasheet). The waveforms of the MMC are described in eqs. (2.4a) and (2.4b), with i_a, the current on the ac-side, I_{arm} the current through the considered arm and I_d the current on the dc-side. Here, it will be considered that the arm current is the one described in equation 2.4b, but the same reasoning can be used with any arm and any power factor.

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Table 2.5: Description of the current-related variables mentioned in the section.

Current	**Switch**	**Origin**	**Description**	**Symbol**
dc-current	IGBT	Datasheet	Max. dc-current that the IGBT can conduct	$I_{dc-igbt}$
Peak Current	IGBT	Datasheet	Max. peak (1ms) current that the IGBT can switch	$I_{pk-igbt}$
Max. average on-state current	IGCT	Datasheet	Based on half-sine, no real practical meaning according to [2]	$I_{av-igct}$
Max. RMS on-state current	IGCT	Datasheet	Based on half-sine, no real practical meaning according to [2]	$I_{rms-igct}$
Max. controllable turn-off current	IGCT	Datasheet	Max. anode current that can be turned-off	$I_{mto-igct}$
Switching Current	Both	Datasheet	Current value condition for the switching energy value given in the datahseet	I_{swi}
Max. av. current MMC	Both	This section	Av. current going through the switches (worst case)	$I_{av-semi}$
Max. instantaneous current MMC	Both	This section	Max. instantaneous current seen by the switches	$I_{max-semi}$
Equivalent current IGCT	IGCT	This section	Built with the datasheet currents, equivalent of $I_{dc-igbt}$ for the IGCT	$I_{eq-igct}$

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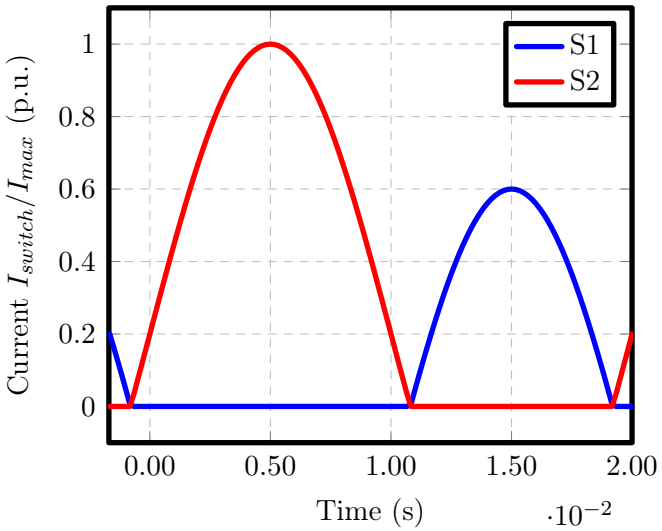

Figure 2.22: Currents in the power switches, if the submodule is kept inserted (worst case). S1 and S2 defined in figure 1.3.

$$i_a = I_a \times sin(\omega t) \tag{2.4a}$$

$$I_{arm}(t) = \frac{I_d}{3} + \frac{I_a}{2} \sin \omega t \tag{2.4b}$$

An MMC can be described with the following design-related ratios (eqs. (2.5a) and (2.5b)), k being the ratio between the ac and dc currents, and m being the ratio between the ac and dc voltages. The relation between these ratios and the power (2.5c), results from the hypothesis that the powers from each side (ac and dc) are equal. Typical values for m are around 0.8 ± 0.1 and for $\cos(\phi)$ (power factor) around 0.85 ± 0.1. So the typical value of k is 3 ± 0.8.

$$k = \frac{3I_a}{2I_d} \tag{2.5a}$$

$$m = \frac{2U_a}{U_d} \tag{2.5b}$$

$$k * m * \cos(\phi) = 2 \tag{2.5c}$$

The calculation of the average current through the IGCT in the worst case is described in eqs.(2.6a) to (2.6d), with the integration of the positive component of the arm current, corresponding to the current in the most loaded IGCT. The values t_1 and t_2 correspond to the times when $I_{arm}(t) = 0$, therefore their expression in eq. 2.6a is obtained using eq. 2.4b. The average current of the IGCT is obtained in eq. (2.6d).

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$$t_1 = \frac{\arcsin\left(-\frac{1}{k}\right)}{\omega}; t_2 = \frac{\pi - \arcsin\left(-\frac{1}{k}\right)}{\omega} \tag{2.6a}$$

$$I_{av-semi} = \frac{1}{T}\int_{t_1}^{t_2} I_{arm}(t)dt = \frac{1}{T}\int_{t_1}^{t_2}[\frac{I_d}{3} + \frac{I_a}{2}\sin\omega t]dt \tag{2.6b}$$

$$I_a = \frac{2k}{3}I_d \tag{2.6c}$$

$$I_{av-semi} = \frac{I_d}{6\pi} * (\pi - 2\arcsin\left(-\frac{1}{k}\right)) + \frac{kI_d}{3\pi}[\cos\left(\arcsin\left(-\frac{1}{k}\right)\right)] \tag{2.6d}$$

This expression of $I_{av-semi}$ can be simplified using a linear regression, shown in eq. (2.7a). This regression is done on a limited range of values of k, between 2 (minimum of k in half-bridge based MMCs according to eq. 2.5c) and 10 (10 is high for an HVDC MMC). Therefore, this range of values of k covers a vast majority of HVDC MMCs. The regression gives a coefficient of determination (R^2) value of 0.99992.

$$I_{av-semi} = I_d * [\alpha * k + \beta] \quad ; \quad \alpha = 0.103398 \quad ; \quad \beta = 0.19019 \tag{2.7a}$$

$I_{max-semi}$ is obtained from equation (2.4b) and equation (2.5a) by replacing the sinus by its maximal value, i.e. 1. The function f is then introduced in equation 2.8b, as the ratio between $I_{max-semi}$ and $I_{av-semi}$.

$$I_{max-semi} = I_d * (\frac{1+k}{3}) \tag{2.8a}$$

$$f(k) = \frac{I_{max-semi}}{I_{av-semi}} = \frac{1+k}{3 \times (\alpha \times k + \beta)} \tag{2.8b}$$

An equivalent current $I_{eq-IGCT}$, that can be directly compared to the $I_{dc-igbt}$ of an IGBT, is defined in equation 2.9. $I_{eq-IGCT}$ is equal to the minimum of $I_{mto-IGCT}$ (maximum current at turn-off) and $I_{av-IGCT} \times f(k)$ to ensure it does not exceed the current that can safely be interrupted, in a normal operation. In this section, only the normal operation is taken into account, not the behaviour in case of fault.

$$I_{eq-IGCT} = \min(I_{mto-IGCT}, I_{av-IGCT} \times f(k)) \tag{2.9}$$

f is a function that is increasing with k. Here, we consider the case in which $k = 2$, i.e. $f(k) = 2.5116$, to stay in the most general case. In this case, for many IGCTs, $I_{av-IGCT} \times f(k)$ has a higher value than $I_{mto-igct}$.

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2.4.1.3 Comparison of the current metric for the IGCT with the IGBT current ratings

Two things can be concluded from that result. First, $I_{mto-igct}$ can be most of the times compared to $I_{dc-igbt}$ (even though it needs to be checked afterwards with this method). Then, most available IGCTs have very high $I_{mto-igct}$ (3 to 8 kA), which means they can handle much larger currents than available IGBTs ($I_{dc-igbt}$ = 1 to 3 kA for >3.3 kV IGBTs) in an MMC application. This is illustrated in Fig. 1.16 where $I_{dc-igbt}$ and $I_{eq-IGCT}$ are plotted. Finally, $I_{mto-igct}$ is a limit of the IGCT related to the gate circuit (how much current the gate can divert to open the IGCT) and $I_{av-IGCT} \times f(k)$ is a thermal related limit of the semiconductor. If $I_{eq-IGCT}$ is equal to $I_{mto-igct}$, the limit is not related to the semiconductor itself: the semiconductor could withstand more current.

2.4.2 Figures-of-merit to compare losses

After we established a consistent current rating for IGBT and IGCTs in the previous section, we can now compare the merits of different switches. These Figures of Merit (FOMs) are related to the conduction and switching losses.

2.4.2.1 Conduction Losses Figure-of Merit

For the conduction losses, a FOM that can be used is the on-state voltage. We consider in this section the on-state voltage model as described in eq (2.10a) for the following reasons: it is very accurate for IGCTs over their entire SOA and acceptable for IGBTs, even though an exponential fit would be more accurate for these devices. As this on-state voltage is dependent on the current flowing through the component, we consider the MMC waveforms to calculate an average on-state voltage value. It is equal to the on-state voltage for the average current, as it is demonstrated in eqs (2.10a) to (2.10b). Thus, this approach only uses values that are available in the datasheets, which makes it interesting at the early stages of design, for the pre-selection of devices.

$$V_{on}(I) = V_0 + R.I \tag{2.10a}$$

$$\text{average}(V_{on}) = V_0 + R.average(I) = V_{on}(I_{av-semi}) \tag{2.10b}$$

The average on-state voltage is then normalised with respect to the blocking voltage of the switch (considered with a de-rating to reach a reliability of 100 Failure-In-Time – FIT – defined in particular in [3]), to allow for the comparison between semiconductors with different voltage ratings. In an MMC, submodules are connected in series to reach HVDC levels, so devices with any voltage rating can be used in theory, and the number of submodules is adjusted accordingly. The final figure of merit is then:

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$$FM_{cond-loss}(IGCT) = \frac{V_{on}(I_{av-igct})}{V_{block-100FIT}} \tag{2.11a}$$

$$FM_{cond-loss}(IGBT) = \frac{V_{on}(\frac{I_{dc-igbt}}{2.5116})}{V_{block-100FIT}} \tag{2.11b}$$

2.4.2.2 Switching Losses Figure-of Merit

For the switching losses, turn-on and turn-off energies are used to compare semiconductors. In datasheets, the losses figures are always quoted at maximum rated current (I_{swi}), which differs from one semiconductor to another and may differ from the actual current in the application. The IGBT and IGCT switching losses can be approximated by a linear function depending on the current. For the IGBT this is only true up to the dc-current rating, but this is sufficient in the case of the MMC. To compare the switching losses, the chosen figure of merit is the following:

$$FM_{swi-loss} = \frac{E_{datasheet}}{V_{block-100FIT} \times I_{swi}} \tag{2.12}$$

2.5 Losses simulation to validate the Figures-of-Merit

2.5.1 Model

As it can be seen in the literature (see Tab. 2.2), IGCTs are always found to cause lower losses than IGBTs. However, the estimated amount actually varies noticeably from one publication to another because it depends on many factors: MMC ratings, control methods, operating points, not all of which are disclosed in the corresponding publications. As a consequence, it is difficult to rely on published results to validate our FOMs. That is why a simple MMC model has been developed, focusing on the individual behaviour of each submodule (capacitor and semiconductors). This model is used to validate the FOM approach.

The model is written as a Matlab script. The modelling assumptions are as follows: perfect sinusoidal current in the arm and perfect sinusoidal voltage across the arm for the current and voltage AC-components; arm inductor, line resistors and energy exchange between arms are not modelled; only one arm is considered.

2.5.1.1 Control and Balancing Control Algorithm

The model calculates the switching instants of the semiconductors switches with the nearest level modulation control method [86] and the capacitor voltage balancing with the reduced switching algorithm [112] (a balancing capacitor algorithm based on a voltage tolerance band). Other controls based on the Pulse Width Modulation (phase-shift PWM, level-shift PWM or other derivative) are developed in the literature and presented in [105, 28, 50]. Although

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Table 2.6: Conducting and switching devices depending on the current direction and insertion state.

	I>0		**I<0**	
State	1	0	1	0
Conducting device ($E_{loss-cond}$)	D2	S1	S2	D1
State-change	$1 \rightarrow 0$	$0 \rightarrow 1$	$1 \rightarrow 0$	$0 \rightarrow 1$
Turning-on device ($E_{loss-on-swi}$)	S1	D2	D1	S2
Turning-off device ($E_{loss-off-swi}$)	D2	S1	S2	D1

simple, this model produces realistic waveforms for the operating voltage and current of each submodule, which allows for a more accurate estimation of the losses than average arm models. The whole control is described on the scheme in figure 2.23. In 2.23, nbr corresponds to the total number of inserted submodules needed to reach the aimed voltage, while Δnbr is the number of submodules that has to be inserted (if Δnbr positive) or removed (if Δnbr negative). Δnbr takes into account the submodules that are removed or inserted due to exceeded voltage limits.

2.5.1.2 Calculation of losses and voltage variation of capacitors

Switching Losses The switching losses are calculated according to the current sign (I positive or negative in figure 1.3), and the change of insertion state. The switching devices depending on these conditions are given in the table 2.6. These switching losses are all calculated according to eq. (2.13), with $E_{swi-datasheet}$ being the energy rated on the datasheet (whether it is turn-on or turn-off). The assumption here is that the switching energy is proportional to the current through the device and to the voltage across the device during the switching.

$$E_{loss-swi}(V_{SM}(t), I_{arm}(t)) = \frac{E_{swi-datasheet}}{V_{block-100FIT} \times I_{swi}} \times V_{SM}(t) \times |I_{arm}(t)| \tag{2.13}$$

Conduction Losses The conduction losses are calculated according to the current sign (I positive or negative in figure 1.3), and the insertion state. The conducting device depending on these conditions is given in the table 2.6. Then the conduction losses are calculated according to eq. (2.14).

$$E_{loss-cond}(I_{arm}(t)) = (V_0.|I_{arm}(t)| + R.I_{arm}(t)^2) * \Delta t \tag{2.14}$$

Voltage variation of the capacitor The submodule capacitor voltage variation is described by the following equation 2.15. SM_{status} is a boolean equal to 1 if the submodule is inserted and 0 if not.

$$V_{SMi}(t+\Delta t) = V_{SMi}(t) - \sqrt{\frac{2}{C_{SM}}(E_{loss-cond}(t) + E_{loss-swi}(t))} - SM_{status}(t) * \frac{I_{arm}(t).\Delta t}{C_{SM}} \tag{2.15}$$

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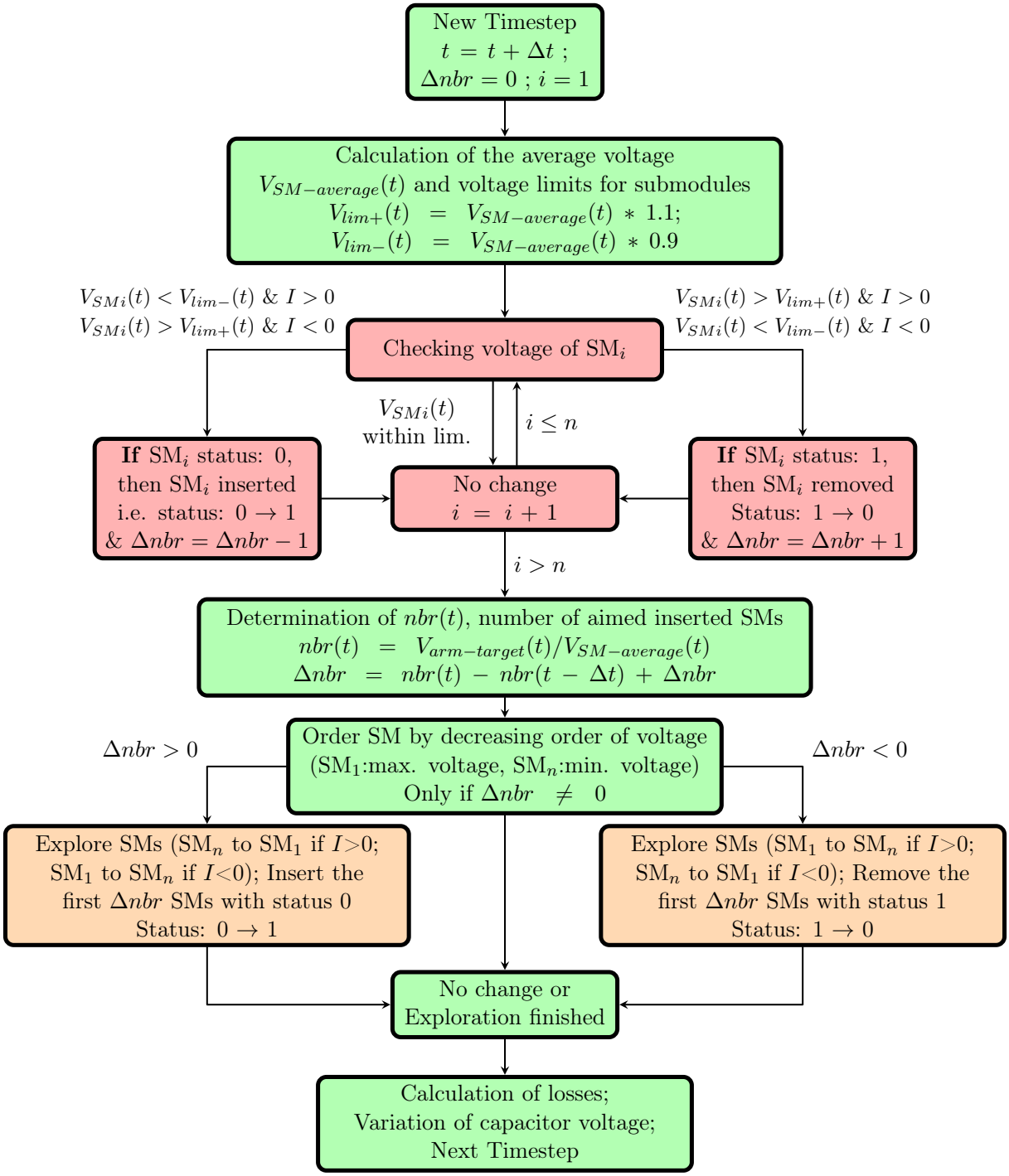

Figure 2.23: Scheme explaining the control Algorithm for the simulation. This control is valid for I charging the capacitor (I positive in the sign convention for capacitors).

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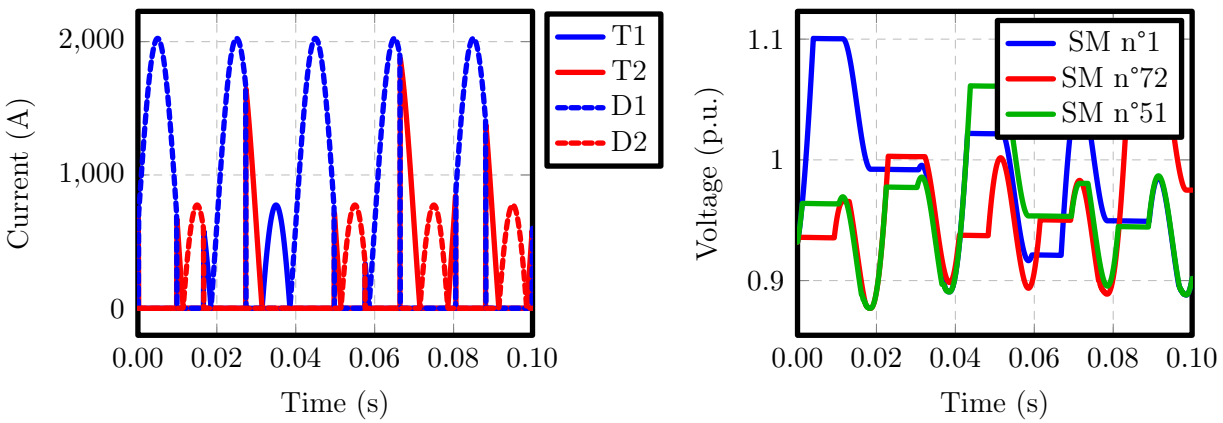
Snubber related losses Because this losses study is aiming to validate the figures-of-merit, and that the figures-of-merit do not take into account any snubber related losses or behaviour, it has been decided not to compute the snubber losses. A method could have been considering for every IGCT a snubber inductor value of $L_{snu} = U_{rating-igct}/(di/dt)$, with di/dt=1kA/µs, and then snubber losses of $1/2.L_{snu}.I_{arm}$ at each IGCT turn-on. For indication, the snubber losses have been found to be lower than 10% of the whole submodule losses for [36, 76], and around 2.5% for [138].

2.5.1.3 Obtained waveforms

Examples of current and voltage waveforms for the upper arm, and the capacitor voltages for some (randomly chosen) submodules are displayed in figure 2.24. The waveforms in figure 2.24b show that, as it is the case in actual MMCs, the different submodules have different switching instants, different voltages at a given time, and they respect the set voltage ripple (10% in that case) around the average value of the capacitors voltages. The waveforms in figure 2.24a show that the semiconductor conduction losses are calculated with realistic current waveforms. This model has been used to simulate MMC operation over different lengths of time (up to 100 AC-periods), and it was found that simulating operation over 5 AC-periods was sufficient to get consistent results (which takes a few minutes).



(a) Currents in the semiconductor switches for the SM n°72

(b) Capacitor Voltages

Figure 2.24: Waveforms of the arm and some submodules, after simulation of the same MMC as [138]. (p.u. means per unit and is the instantaneous voltage of the submodule divided by the rated voltage of the submodule)

2.5.2 Results

Simulations were realised considering the following MMC: 1 GVA, 400 submodules per arm, a mean submodule voltage of 1600 V, a dc voltage of 640 kV (pole to pole). The considered devices are: IGCTs (5SHY 35L4521) and associated diodes (5SDF 20L4520), or press-pack IGBTs (5SNA 2000K450300) which include their own diodes. Using the model, losses of 5.2 MW (0.52% of the transferred power) in the case of the IGCT and 6.72 MW (0.672%) in the case of the IGBT have been obtained. This corresponds to a loss reduction of 23.6% for

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the IGCT case compared to the IGBT case, which is consistent with the results presented in Tab. 2.2.

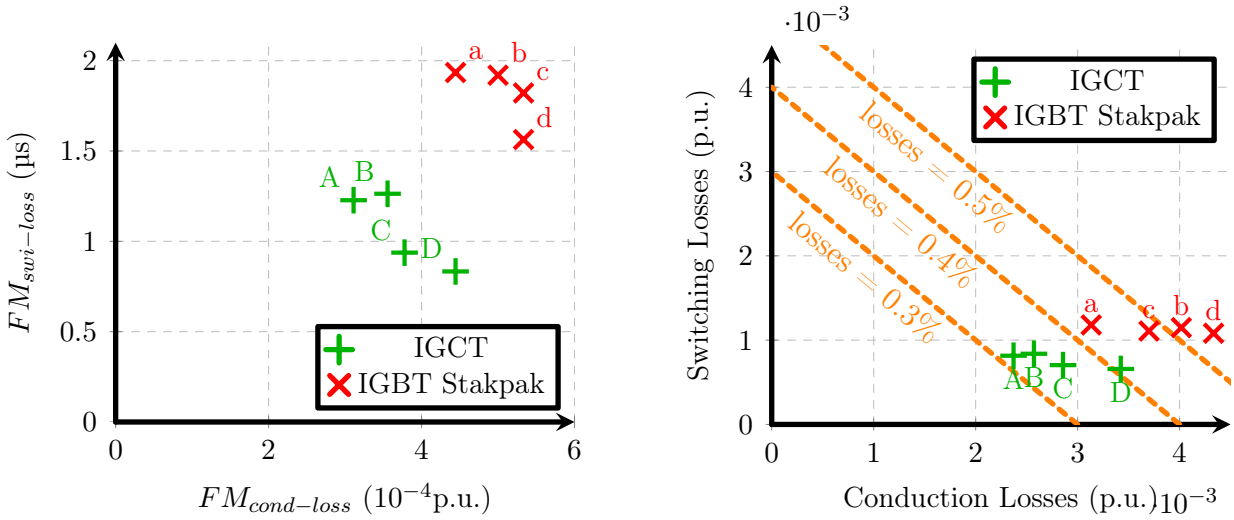

Figure 2.25: (a) Figures of merit applied to ABB online catalog for 4.5kV IGCTs and Stakpak IGBTs in 2019; (b) corresponding Switching and conduction losses for the same 4.5 kV ABB IGCTs and Stakpak IGBTs, simulated for the same MMC as [138] (inverter case), with iso-loss curves drawn in orange.

2.5.3 Conclusion on the Figures-of-Merit

The figures of merit for the ABB IGCTs and Stakpak IGBTs for different voltage ratings are displayed in Fig. 2.25a. They are in good agreement with the corresponding switching and conduction losses calculated using the MMC model (for 4.5 kV devices only, Fig. 2.25b). Both approaches confirm the superiority of IGCTs over IGBTs regarding losses in general. Fig. 2.25a provides a comparison which is independent from the actual characteristics of the target MMC, while Fig. 2.25b is specific to one particular MMC. This demonstrates the interest of these figures of merit: they provide a quick, general and efficient way to compare devices even before modelling and simulating a specific MMC.

As expected, the IGCT has lower conduction losses on average, although in some cases, with the worst IGCT and the best IGBT in terms of conduction losses, the IGBT is better. This appears both using the figure of merit (see Fig. 2.25a) and the simulated conduction losses (see figure 2.25b). It can be explained by the use of average on-state voltage in the figure of merit – calculated as the on-state voltage at the average current of each semiconductor – and by the use of the same MMC for the simulations – the current of this MMC is the same for all the semiconductors. This implies an under-use of the IGCTs, whose on-state voltage grows slowly with the current. Indeed, as it can be seen in figure 2.26, the on-state voltage of an IGCT grows slower than the on-state voltage of an IGBT. In fact, the IGCT is more suitable for MMCs with higher current ratings. But it has to be kept in mind that figure 2.26 is a particular case of one IGCT and one IGBT.

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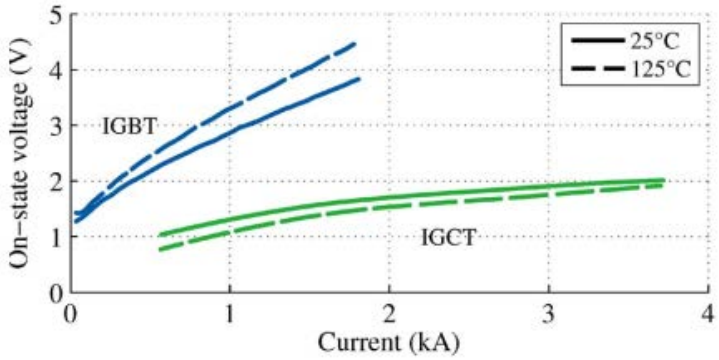

Figure 2.26: On-state voltage of one IGCT and one IGBT [31]

Furthermore, the IGCT is often described as having more switching losses than the IGBT: with the figures of merit (and confirmed by the simulation), it can be seen that any considered IGCT actually has lower switching losses than any IGBT. The turn-on losses are actually very small for the IGCT. Regarding conduction losses, the biggest difference (the best IGCT and the worst IGBT in terms of conduction losses) is 0.2% while the biggest switching losses difference is 0.055%. This is due to the low switching frequency of the devices in the case of HVDC MMCs.

2.6 Possible investigations on the IGCT for MMC applications

The literature review presented in the previous chapters indicate that the IGCT is a very high performance switch, which should improve conversion efficiency in HVDC MMCs. However, this device has drawbacks, which deserve further investigation to determine whether they can be overcome or dealt with.

2.6.1 Snubberless IGCTs

As presented in the previous chapter, a turn-on snubber is needed because even if the IGCT can handle higher di/dt values than those quoted in the datasheets, the diode may not be able to withstand them. The authors of [128, 137] consider that an optimal value is $5.3\,\mathrm{kA\,\mu s^{-1}}$, which corresponds to the maximum di/dt acceptable for some diodes (e.g. ABB diode 5SDF 28L4521).

But even if the snubber cannot be suppressed, it can be reduced, thanks to these higher di/dt values, as [128] has shown. To limit di/dt at $1.1\,\mathrm{kA\,\mu s^{-1}}$ at a DC bus voltage of $\approx$2 kV, the inductance of the snubber must be 1.95 µH. With a di/dt of $5.2\,\mathrm{kA\,\mu s^{-1}}$, the inductance is reduced to 0.32 µH. Not only this results in a smaller snubber inductor, but the energy stored in the inductor is also reduced: at 2 kA, this corresponds to 3.9 J and 0.64 J respectively. As this energy is transferred from the inductor to the capacitance and then dissipated by the resistance of the snubber, reducing the inductor also results in down-sizing the other elements

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of the snubber.

Furthermore, a snubber inductor of 320 nH is comparable to the stray inductance encountered in standard IGCT circuits (L_S in the circuit diagram in Fig.2.18b). This means that the IGCT may be able to withstand the overvoltage created by this smaller inductor at turn-off, so the energy may be dissipated in the IGCT itself. This would allow to remove the capacitor, the resistor and the diode of the snubber. This dramatic simplification of the power circuit would have important consequences on the cost and volume of an MMC submodule. This hypothesis is explored experimentally in the chapter 4.

2.6.2 Improving the gate driver

As it can be seen in Fig. 2.5, the gate driver unit of an IGCT is larger than the GCT itself. In the IGCTs of ABB or CRRC, the gate-drive unit comprises many electroytic capacitors. The lifetime of these capacitors is temperature sensitive, which is an important reliability issue. Due to that sensitivity, their ambient temperature is limited to 50°C, while the maximum junction temperature of the GCT is 125°C (values from 5SHY 35L4520 IGCT from ABB). The difference between these temperatures require to position the capacitors away from the GCT, which in turn puts a lower limit on the stray inductance (corresponding to the minimal distance from the GCT) of the control loop.

In 2005, using other types of capacitors for the gate circuit was considered, but was not found to be interesting (due to cost and available space [34]). According to [52], changing the type of capacitors is possible due to recent improvements in multilayer ceramics capacitors (such as X7R), which now offer both a high capacitance density and a low equivalent series inductance (ESL). As a consequence fewer capacitors are needed. In [52], a total capacitance of 470 µF is required when using ceramic capacitors while electrolytic capacitors require 44.7 mF, because of their much higher ESL. Furthermore, as ceramic capacitors can sustain the junction temperature of the GCT, the authors of [52] were able to integrate them (along with the MOSFET switches) in the GCT case, resulting in the dramatic size reduction shown in figure 2.27. Integrating the gate driver in the GCT package also allows to achieve a lower inductance of the gate circuit, resulting in a higher turn off current capability of the IGCT.

Even without considering integration of the gate driver (which requires the development of special housing and reduces the cooling paths for the GCT), a recent study (2019) has demonstrated the advantages of using a combination of electrolytic and ceramic capacitors inside the gate-drive unit [17] (lower stray inductance, lower stray resistance, lower volume). Furthermore, as shown in the previous chapter, modifying the gate driver may be necessary to allow for faster turn-on capability of the IGCT.

As said in section 2.2.2, the gate driver of the IGCT has high power requirements (up to more than 100W). This calls for the development of specific power supply units to draw power from the main capacitor in an MMC submodule.

Despite being a subject of interest, this optimisation of the gate driver unit is not addressed in this thesis.

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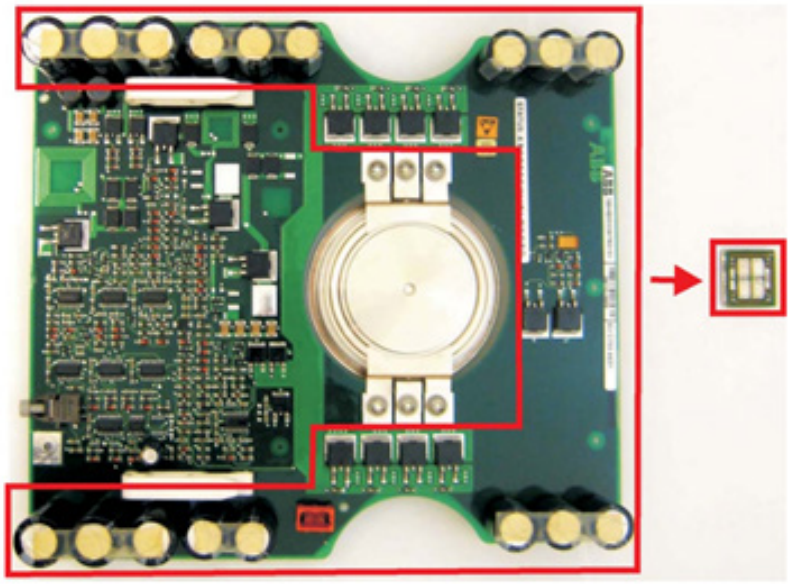

Figure 2.27: Gate-drive circuits in [52]. Encircled in red: on the left the circuit based on electrolytic capacitors and on the right the circuit based on ceramic capacitors.

2.6.3 Other research topics

Many more questions should be addressed to fully explore the potential of IGCTs in MMC converters. For example:

- Depending on the results of the "snuberless" study, is a hybrid submodule (i.e using one IGBT and one IGCT, and possibly two different diodes) required? Is it desirable (for cost reduction/performance improvement)?
- What are the limits regarding series/parallel association of IGCTs? Series association may be attractive to form submodules with higher voltage ratings; parallel association may be a simple solution to increase current ratings. There are, however, few published studies of such associations.
- Is the fail-to-short behavior sufficient to ensure continuous operation of an MMC over long periods (between two scheduled maintenances), or is a mechanical switch still needed?

2.7 Conclusion on the use of IGCT in MMC submodules and perspectives

In this chapter, the interest of the IGCT has been assessed in HVDC MMC submodules. First, the technology of the IGCT, its specific features (hard-driven principle, housing, gate drive circuit, buffer layer) and the evolution from the SCR thyristor have been presented, as well as the different types of GCTs (Asymmetric, Reverse-Conducting, Reverse-Blocking, Bi-mode).

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Then the IGCT has been compared with the IGBT in the HVDC MMC case. The IGCT displays lower losses than the IGBT mainly because of its lower on-state voltage, as it has been found in the literature and in this chapter. The creation of original losses figures-of-merit in this thesis, validated by losses simulation results, has permitted a more general approach, compared to the specific approach of losses studies (one converter, one control method and often one device).

But the IGCT also has a negative impact on the freewheeling diode due to its switching speed at turn-on. This speed, if not controlled by a turn-on snubber leads to potential destruction of the diode by a too high di/dt, but the GCT part of the IGCT seems to withstand way higher di/dt.

Other possible investigation leads have been found and explained in this chapter. But in the following chapters, the reduction and potential removal of the IGCT snubber will be studied experimentally, the test bench being designed in chapter 3, the IGCT being tested with very fast (up to 13kA/µs) silicon diodes in chapter 4 and with silicon carbide diodes (with an original packaging, created in this thesis) in chapter 5.

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Chapter 3

Double Pulse Test of IGCT with fast recovery diodes – a test bench Design

3.1 Experiment objective, functioning of the double pulse test setup

3.1.1 Experiment objective

The goal of this study is to determine if the snubber can be removed in IGCT-based MMC submodules (or at least downsized) if fast enough freewheeling diodes are used. As a reminder, the turn-on snubber is composed by a snubber inductor (limiting the di/dt) and an RCD-clamp (limiting the overvoltage produced by the snubber inductor). Removing the snubber would mean that the limit on di/dt during reverse recovery is not exceeded with only the stray inductance of the circuit to limit it and without any RCD clamp. For a 300nH stray inductance at 3kV bus voltage for example, a diode withstanding at least 10kA/µs is needed.

3.1.2 Double pulse test setup description

To analyse and test the snubber reduction and suppression, the commutations of the IGCT have to be studied, especially the turn-on phase. A commonly used switching test circuit is the "double-pulse test" to determine the dynamic characteristics of semiconductor devices (switching energy, behaviour at switching) and the integration of devices together (study of a commutation cell behaviour and its parasitic elements). As described in a simplified way in figure 3.1, the double pulse circuit consists in a capacitor serving as voltage source, an inductor, a switch and a freewheeling diode. It then works like illustrated in figure 3.2 with the switching events and phases described below.

A - Phase A: Before t_0, the capacitor C is charged, up to a predefined voltage (1000V in Fig. 3.2), calculated to reach the desired pulse voltage during turn-off or turn-on (980V for the first turn-off and the turn-on in Fig. 3.2).

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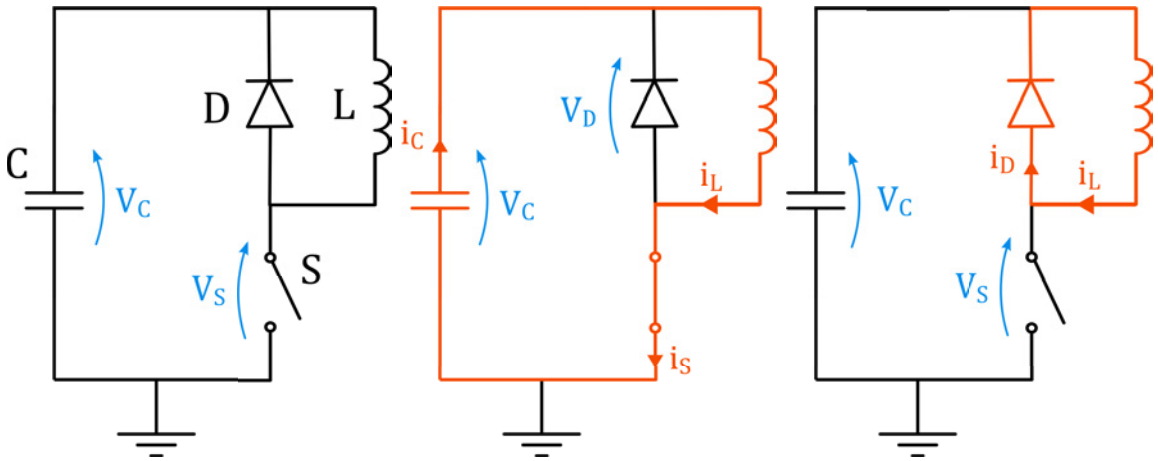

(a) Phase A. (b) Phase B and D. (c) Phase C and E.

Figure 3.1: Simplified circuit of double pulse test, at different phases during the test.

0 - At t_0, the switch is closed.

B - Phase B: Between t_0 and t_1, the inductor is charging up to a current determined by $u = L.di/dt$ due to energy exchange with the capacitor. Therefore the voltage of the capacitor decreases during that phase.

1 - At t_1, the switch is opened. This is the first turn-off of the switch and the first commutation event at non-zero current and non-zero voltage.

C - Phase C: Between t_1 and t_2, the freewheeling mode is going on: the diode conducts and the inductor is slowly discharging in the diode. This duration is aimed to be the shortest possible to have the lowest current drop between t_1 and t_2.

2 - At t_2, the switch is closed again. This is the only turn-on event at at non-zero current and non-zero voltage. This is the moment when the diode reverse recovery happens.

D - Phase D: Between t_2 and t_3, the current is increasing and the voltage is decreasing again the exact same way as during phase B.

3 - At t_3, the switch is opened again. This is the second turn-off event.

E - Phase E: After t_3, the circuit is in a freewheeling mode, until the discharge of the inductor is complete.

3.1.3 Presentation of the circuit of the test setup

The whole test setup circuit is displayed in figure 3.3. Each part will be explained in terms of role and design in the rest of the chapter. In a nutshell, compared to figure 3.1, source, safety elements and snubber are added. The test setup main objectives and features are as follows:

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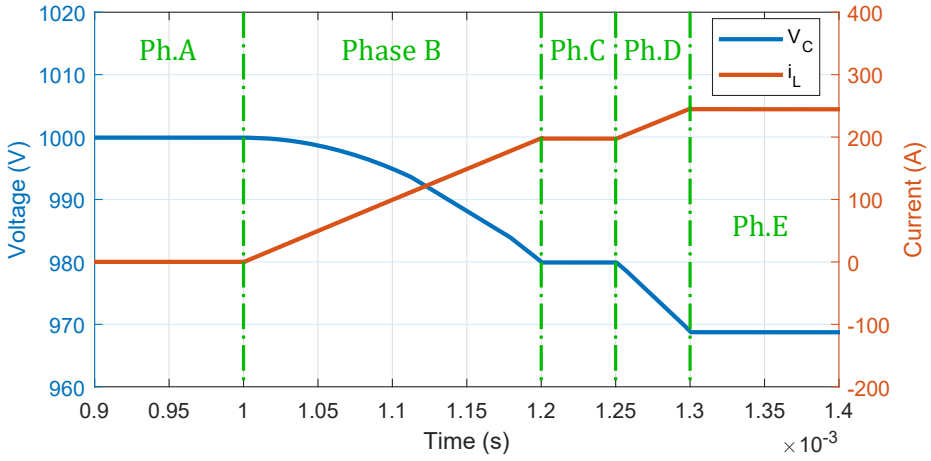
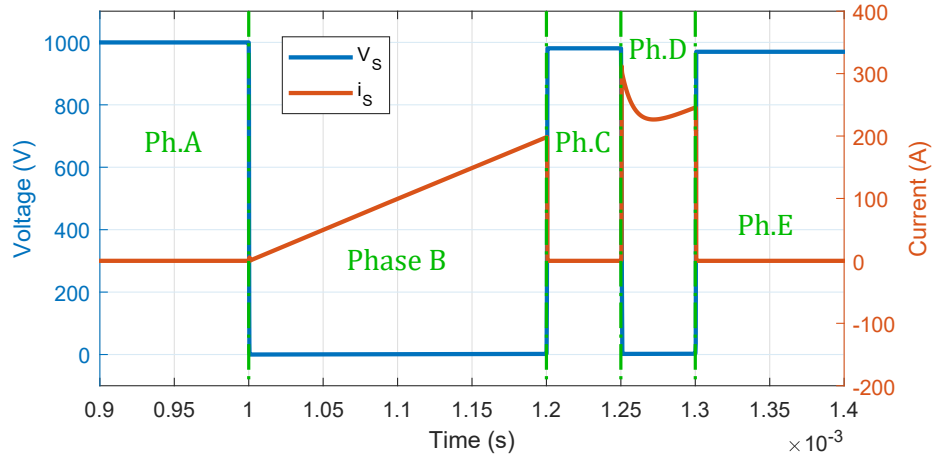
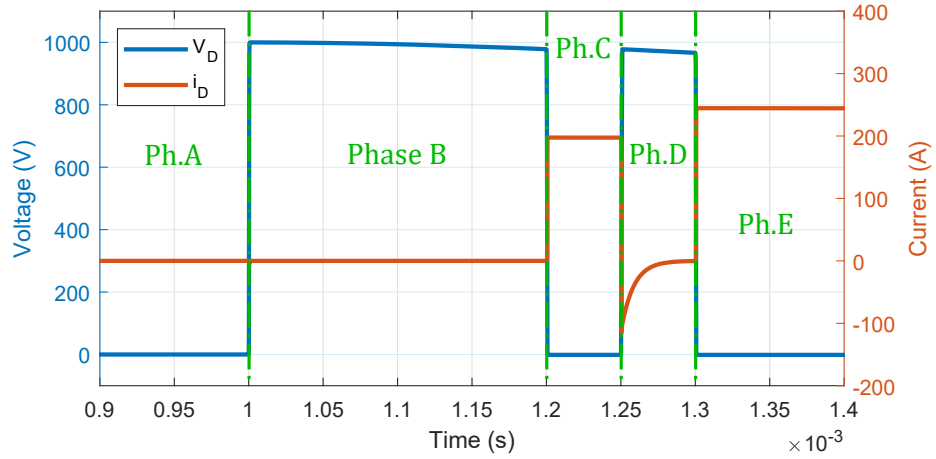


(a) Waveforms of bus voltage and inductor charge current



(b) Waveforms of switch voltage and current



(c) Waveforms of diode voltage and current

Figure 3.2: Typical Waveforms of double pulse, obtained with simulation on LTSpice. Here, $t_0 = 1ms$, $t_1 = 1.2ms$, $t_2 = 1.25ms$, $t_3 = 1.3ms$.

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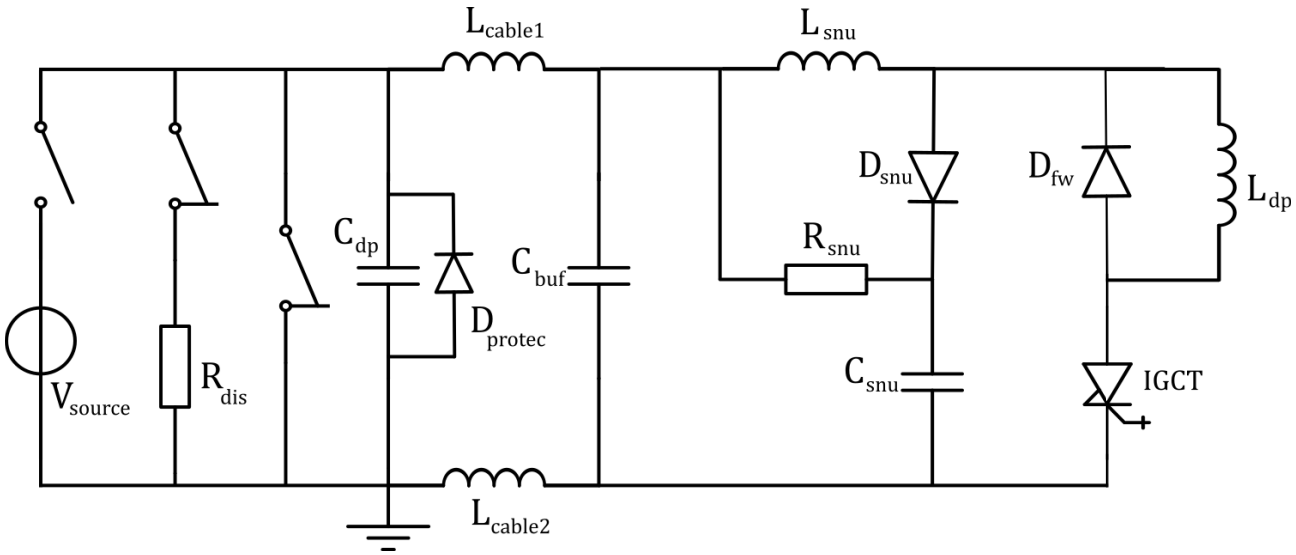

Figure 3.3: Complete experimental circuit.

- The experimental setup has to imitate the structure of an HVDC MMC Half-Bridge submodule, so that the commutation cell designed here has a similar behaviour as a submodule and tests conclusions can be extrapolated to the case of a real HVDC MMC submodule. Busbars inside this submodule part of the setup need to be sized for typical nominal currents of HVDC MMC submodules for the same reason.
- The capacitance and inductance (C and L in figure 3.1)) should be big enough to allow a range of measurements corresponding to typical HVDC MMC submodule voltage and current.
- The snubber must be representative (size, capacitance, inductance and resistance levels) in respect to section 2.3.3.
- The snubber inductance value can be adjusted easily, either with different inductors or a modular system, permitting a wide range of snubber inductance values.
- Dedicated elements protect the components, and other dedicated ensure the operator safety.

The platform that served for the tests in SuperGrid Institute is the HCSW – High Current SWitching, shown empty without equipment in figure 3.4.

3.2 Design of the test circuit part imitating the structure of an MMC submodule and component selection

In this section, the design of the submodule as part of the test setup is presented. The design of this part is articulated around the choice of the semiconductors (diode + IGCT), presented in the first subsection. To imitate the submodule structure, an essential feature of the setup is its physical assembly: the parts are arranged to allow the future assembly of a full HB submodule.

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Figure 3.4: HCSW Platform in SuperGrid Institute.

Spots for one more IGCT and one more freewheeling diode are available, as it can be seen in figure 3.5a. The varistors are being used as protections for the double pulse test but are not designed to stay in a final submodule design, leaving a free space for another freewheeling diode. This physical assembly permits to have stray inductances similar to HVDC MMC submodules ones. The circuit schematic of this part of the setup is displayed in figure 3.6.

The snubber relative to the selected semiconductors is designed in a second subsection, with the inductor part first, followed by the RCD clamp. Then in a third subsection, the buffer capacitor C_{buf} is selected to imitate a submodule capacitor. Finally, the connections of the different parts through typical submodule busbars are designed in the fifth subsection.

From the designed submodule, an experimental plan emerges, presented in the sixth and last subsection.

3.2.1 Choice of semiconductors – IGCT, freewheeling and snubber diode.

The three semiconductors to select are the IGCT and the two diodes (the freewheeling diode and the snubber diode). They are displayed in the 3D rendering in figure 3.5a and in the circuit schematic in figure respectively named 3.6 IGCT, D_{fw} and D_{snu}.

The IGCT In section 2.3, the ratings of IGCTs have been discussed. Some representative references are displayed in table 3.2. Here it has been decided to focus on 6kV-6.5kV IGCTs because they allow higher voltage operation, a general trend in MMCs, and because they would allow to test 4.5 and 6.5kV diodes. The IGCTs of Mitsubishi have been eliminated because of their lower current rating (max. 1.5kA) and because they were symmetrical IGCTs (no specific interest for the MMC). The asymmetrical GCT from Mitsubishi has not been selected either to avoid the heavy task to design a drive circuit. There is only one reference of 6kV-6.5kV both in CRRC and ABB catalog (a 6kV IGCT CAC3000-60 for CRRC, a 6.5kV IGCT 5SHY42L6500 for ABB). The ABB device was selected, driven by cost reason. This IGCT is rated at 3.8kA

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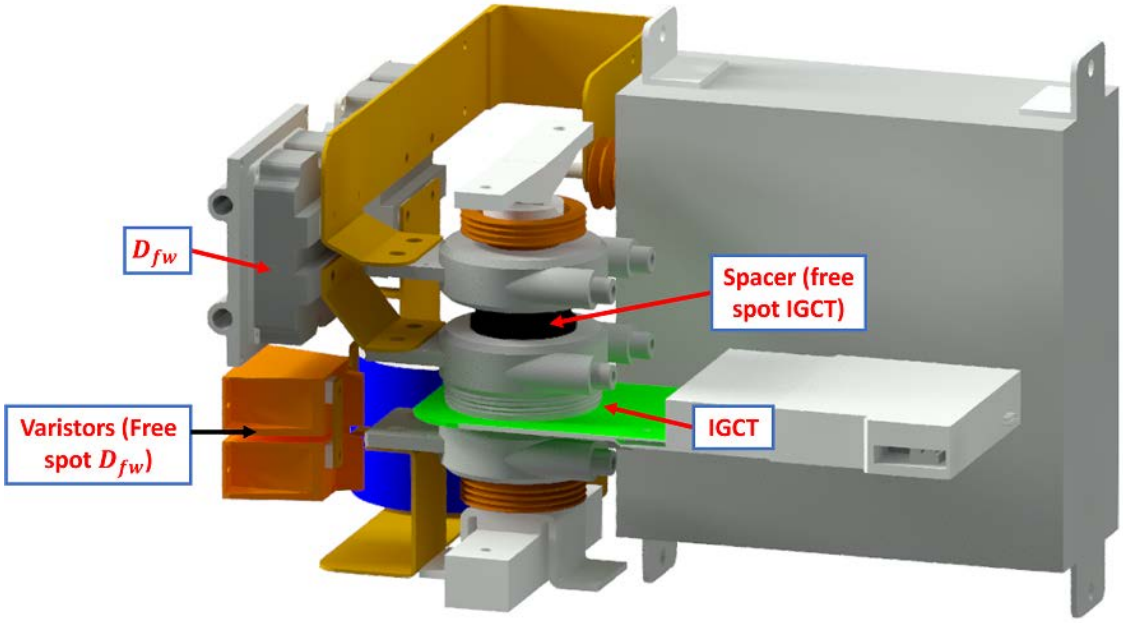
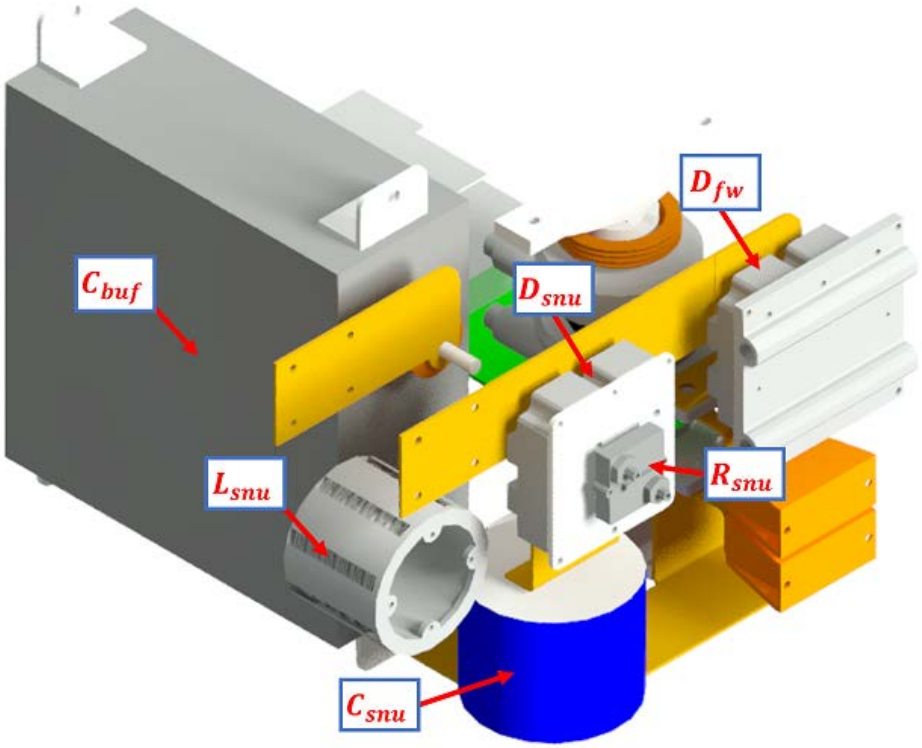


(a) Side view, displaying the IGCT and the freewheeling diode, with the busbar as the snubber inductor.



(b) Top corner view, displaying the snubber, with the cable inductor as the snubber inductor.

Figure 3.5: 3D renderings of the submodule part of the setup. Note that for clarity, the mechanical frame holding the parts together, as well as screws, bolts and cables are not rendered here.

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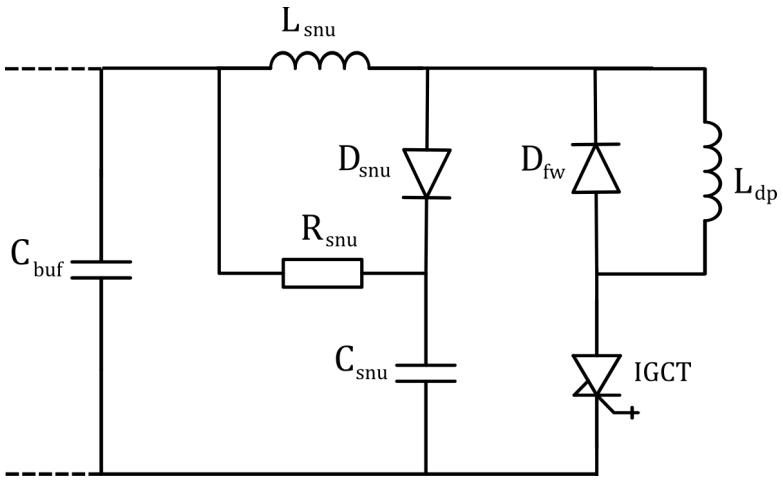

Figure 3.6: MMC submodule part of the double pulse test setup.

Table 3.1: Some IGCTs available in the market. The red one is the one selected. TBD: "to be determined" on the datasheet. RC-IGCTs have not been considered, due to the low di/dt capability of their diode.

Model	***Type***	***Voltage Rating***	***Max. controllable turn-off current***	***Average Current***
CAC 4000-45 (CRRC)	IGCT	4.5kV	4000A	1700A
CAC 8000-45 (CRRC)	IGCT	4.5kV	8000A	TBD
CAC 3000-60 (CRRC)	IGCT	6kV	3000A	1300A
5SHY 35L4522 (ABB)	IGCT	4.5kV	4000A	1700A
5SHY 65L4521 (ABB)	IGCT	4.5kV	6500A	2660A
5SHY 50L5500 (ABB)	IGCT	5.5kV	3600A	1290A
5SHY 42L6500 (ABB)	IGCT	6.5kV	3800A	1290A
FGC6000AX-120DS (Mitsubishi)	GCT	6kV	-	2000A
GCU08CB-130 (Mitsubishi)	S-IGCT (Symmetrical)	6kV	1500A	500A

(regarding $I_{mto-igct}$, see table 2.5).

Pressing system and heatsinks The 5SHY42L6500 IGCT has to be pressed at 40kN to function correctly. The designed pressing system is displayed in figure 3.7. This pressing system has two available locations for IGCTs to imitate a real submodule structure.

This space could be used in the future for a study with an entire submodule structure (2 IGCTs + 2 D_{fw}) or for a double pulse with a press-pack diode (as a freewheeling diode). An important detail is that electrical conduction and cooling are both provided by the heatsinks. This means that the cooling system (pipes and liquid) has to be non conductive.

Freewheeling diode To select the freewheeling diode, the main criteria was its maximum allowed di/dt during the diode turn-off, undifferently from the package – either plastic or press-pack. Some diodes are listed in the table 3.2. After a complete search and listing, we selected the 5SLD0600J650100 and 5SLD1200J450300 references. On top of having the highest possible di/dt, plastic packages combined with IGCTs have not been found in the literature, and that

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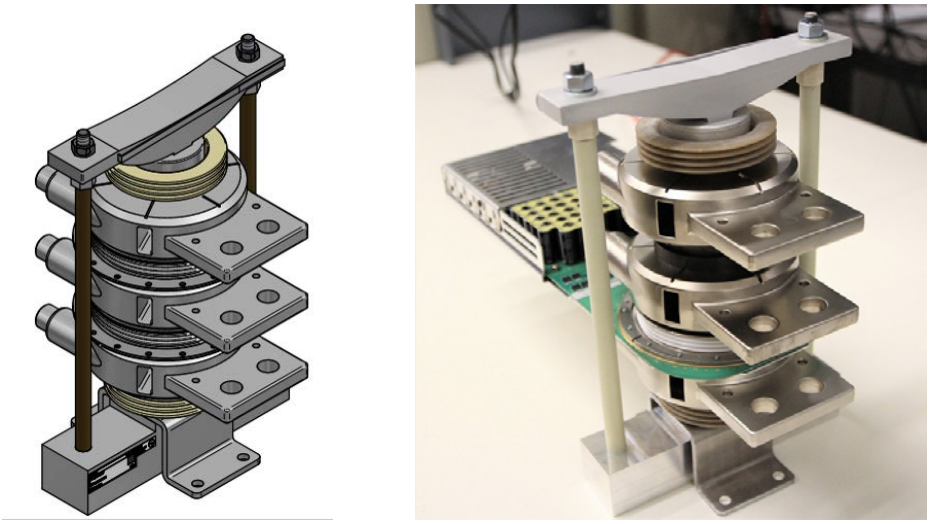

(a) Design of the system on a CAD Software

(b) Real implementation, with one IGCT and one spacer.

Figure 3.7: Pressing system for 40kN. Designed by 5SComponents and Astrol companies.

Table 3.2: Some diodes available in the market. The red ones are the ones selected.

Diode Model	***Voltage Rating***	***Current Rating***	***Maximum*** di/dt ***at reverse recovery***	***Package***
5SLD 0600J650100 (ABB)	6.5kV	2×600A	2×4kA/µs	Plastic
5SLD 1200J450300 (ABB)	4.5kV	2×1200A	2×6.5kA/µs	Plastic
5SDF 20L4521 (ABB)	4.5kV	2070A	5kA/µs	Press-pack
5SDF 20L4520 (ABB)	4.5kV	1970A	1.2kA/µs	Press-pack
RM600DG-130S (Mitsubishi)	6.5kV	2×600A	2×3kA/µs	Plastic
RM1200DG-90F (Mitsubishi)	4.5kV	2×1200A	2×6kA/µs	Plastic
FD3000AU-120DA (Mitsubishi)	6kV	3000A	2kA/µs	Press-pack

could lead to an original contribution. The pack will be used fully: the two diodes in the pack will be put in parallel to increase the overall current rating and to have the highest possible di/dt.

Snubber diode For simplicity, the diode used as snubber diode will be one 5SLD0600J650100 from ABB (same reference as one of the freewheeling diodes). This diode handles the same voltage as the selected IGCT, handles the current that can go through it during its operation – checked with simulation. It's not uncommon to have the same diode used for both freewheeling and snubber.

3.2.2 Snubber inductor design

The whole snubber in the circuit schematic is displayed in figure 3.8 and in the 3D rendered system in figure 3.5b. The snubber will be designed in two steps: first the snubber inductor in this subsection, and then, in the next subsection, the RCD clamp. As a reminder, the role of this inductor is to slow the switching current at IGCT turn-on so that the di/dt does not

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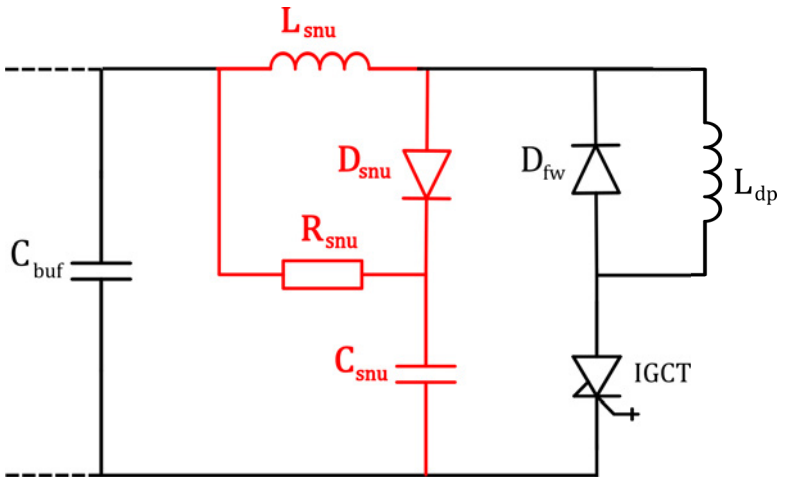

Figure 3.8: Test setup with snubber circuit highlighted.

Table 3.3: Important points for the study in term of di/dt.

Points	***di/dt Value***	***Voltage***	***Corresponding inductance***
Indicated di/dt on IGCT datasheet (2×diode 6.5kV)	1kA/µs	3.6kV	3.6µH
Maximum di/dt (2×diode 6.5kV)	8kA/µs	3.6kV	450nH
Indicated di/dt on IGCT Datahseet (2×diode 4.5kV)	1kA/µs	2.8kV	2.8µH
Maximum di/dt (2×diode 4.5kV)	13kA/µs	2.8kV	215nH

exceed the capability of the diode. The RCD clamp role is to absorb the overvoltage created by the snubber inductor. This link of causality justifies the two-steps design process.

3.2.2.1 Inductance value

The inductance range values are calculated by using the equation $u = L.di/dt$, with u being the nominal voltage of the bus during IGCT turn-on (2.8kV for the 4.5kV diode and 3.6kV for the 6.5kV diode). The important points are described in table 3.3. These characteristic points define the typical maximum acceptable value for a normal diode on the hand (1kA/µs) and on the other hand the maximum acceptable value of these fast diodes (8kA/µs and 13kA/µs). These points also indicate what the order of magnitude of the stray inductance should be to work snubberless, as close as possible to highest di/dt (215nH for the 4.5kV diode and 450nH for 6.5kV diode). This will guide the design of the snubber inductor presented in the next paragraph, and of the busbar in section 3.2.6.

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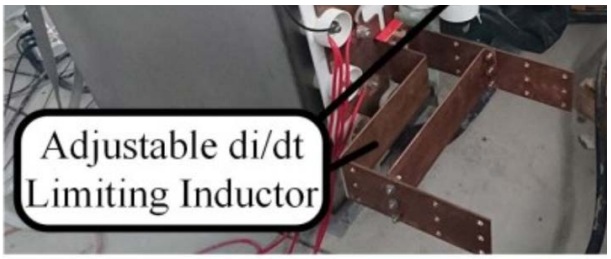
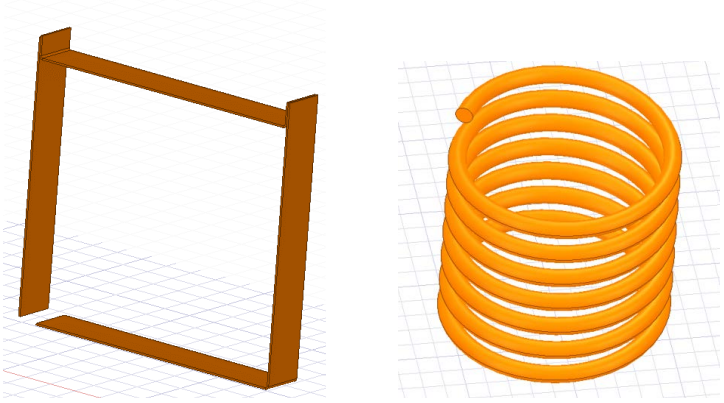


Figure 3.9: Adjustable busbar inductor. Extracted from [128].



(a) Square-shaped busbar inductor.

(b) Cable inductance.

Figure 3.10: Different types of inductors shapes that have been imagined during this thesis.

3.2.2.2 Technical Realisation

In [128], the authors are using an inductance which value can be changed by changing the position of a copper bar, like it can be seen in figure 3.9. This solution with a movable median bar was investigated in this Ph.D. study and is shown in figure 3.10a.

The width of the busbar is dictated by the current rating of the commutation cell, the same way the busbars are designed (see 3.2.6), and this width is fixed to 75mm. With some calculations using Q3D from the Ansys EMSuite, for a 1m times 1m square shape, the inductance is 2.5µH, less than the desired 3.6µH top value. Furthermore, the whole inductor built that way would be too big for the test setup, and would need a complex mechanical structure.

The other solution would be a typical cable inductor with a cable rolled around a cylinder, as shown in figure 3.10b. The diameter of the cable is critical: the minimum bending radius of a cable is considered 10 times the diameter of the cable. In order to minimize the diameter of the inductor, the solution is to use a cable with a decent copper quantity (8.37 mm^2 for a low resistance value) but almost no insulation (600V), to reduce to the minimum the diameter of the cable, and provide the insulation by spacing the turns to respect clearance distance value (14mm for 4.5kV according to IEC 61800-5-1). This solution permits to have a sufficiently low inductor diameter, and therefore more values of inductances within the aimed range of this study. This cable copper section is lower than the copper section of the square shape in the previous paragraph. Indeed, the choice of the cable is the result of a comprise between low resistance (higher copper section) and low diameter of the inductor (lower cable diameter).

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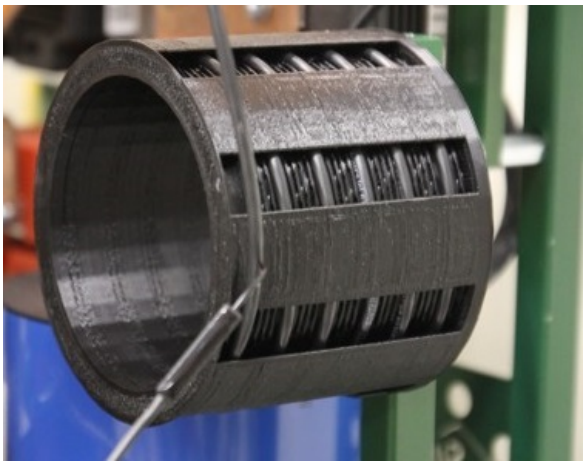

Figure 3.11: Final design of the 3D-printed snubber inductors.

Table 3.4: Real inductances values, measured with an impedance-meter; with simulated inductance values, for 100kHz frequency, 12cm diameter cylinder, an 8.37mm^2 cable, 15mm between turns, exact number of turns.

Inductor nbr/ designation	*Apparent nbr of turns*	*Inductance (µH) @10kHz*	*Ind. (µH) @100kHz*	*Simulated Ind. (µH) @100kHz*
Inductor n° 1	2	0.825	0.80	0.637
Inductor n° 2	3	1.39	1.34	1.156
Inductor n° 3	4	2.05	1.97	1.759
Inductor n° 4	5	3.1	2.9	2.395
Inductor n° 5	6	3.55	3.42	3.161

The table 3.4 shows the values that could be obtained with this solution in the last column, according to Q3D simulations.

The realisation of this inductor cylinder is shown in figure 3.11, and was realised with 3D printing, using PLA as printing material. 3D printing is used here because it permits to produce unique pieces for a low overall cost. This shape permits inserting the cable easily, holds the cable without impregnation, allows scalability by adding turns. The values obtained with the real inductors are displayed in the table 3.4. The difference between the real inductors and the simulated values can be explained by the fact that the simulated inductor excludes the cable length to connect the inductors to the busbars, which can be estimated around 10cm long each side. The estimation of a 10cm long cable corresponding to 100nH corroborates this hypothesis for most inductors. For the inductor n°4 (5 apparent turns), the difference between simulated and measured values can be explained because half a turn was accidentally added during the process. The average of the simulated values of 5 and 6 turns gives a value of 2.78µH, which would support this hypothesis.

3.2.2.3 Movable busbar solution for low inductances

For inductances values smaller than 800nH, 1-turn inductors were not considered. Instead, a busbar with different clamping positions, to have different current loop sizes, is the adopted solution for low inductance, in a similar manner as in figure 3.9. These 4 positions of the

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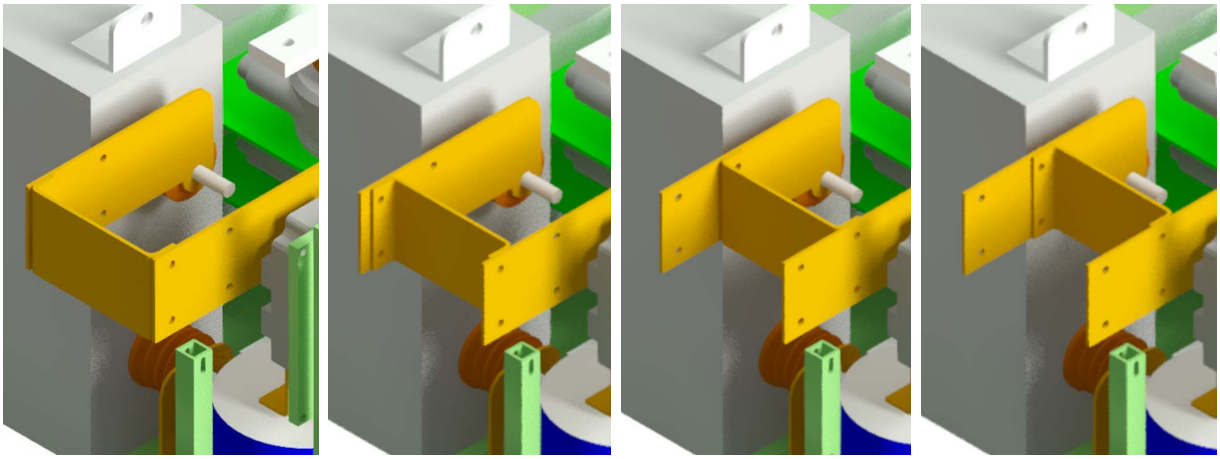

(a) Position 1. (b) Position 2. (c) Position 3. (d) Position 4.

Figure 3.12: Complementary solution for snubber inductance. Screws have not been rendered. 4 positions are possible here, leading to 4 different snubber inductance values.

busbar are displayed in figure 3.12. The overall busbar arrangement will be described later in this chapter when busbar design will be discussed (see 3.2.6).

3.2.3 Snubber capacitor and resistor

The snubber capacitor and resistor role is to limit the overvoltage due to the presence of the snubber inductor. Different methods exist in the literature [5, 135, 27, 100] for their selection, all based on the optimisation between two main parameters:

- The duration between pulses, defining the discharge duration for the snubber inductor. Here the value is imposed at 40µs by the IGCT datasheet. The IGCT should not be turned on or off before the snubber inductor is discharged and the snubber capacitor is back to its normal value, to ensure normal operation of the submodule. [2, 135] Filure to meet this criterion could lead to non negligible voltage increase and if the snubber diode is still conducting, high di/dt turn-off for the snubber diode (potentially destructive) [27].
- The tolerated overvoltage across the IGCT at turn-off due to the snubber inductor, in the presence of R_{snu} and C_{snu}. Here it has been decided to limit the overvoltage at **1kV at 3.5kA and 2.8kV, and 1kV at 2.4kA and 3.6kV**.

In a nutshell, selecting R_{snu} and C_{snu} for a rapid discharge of the snubber circuit would lead to a high overvoltage across the IGCT, and selecting them to lower the overvoltage across the IGCT would lead to a slow discharge of the snubber circuit.

On top of that list, these following parameters have to be added during the final component selection: the power and current ratings of the resistor and the voltage rating of the capacitor.

The selection of both R_{snu} and C_{snu} has been done through iterative simulation, testing different values of R_{snu} and C_{snu}, starting from values found in literature (see table 2.4). The

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simulations were performed with the 'LTSpice' circuit simulation tool using simple components models: the IGCT is a voltage controlled switch (like in [2]), the diodes are modelled with a simple diode model (without reverse recovery). As an example of typical values, on the datasheet of the selected IGCT, the value of the capacitance is 20µF and the value of the resistor is 0.35Ω.

In figure 3.13 is displayed the influence of the snubber capacitor size on the overvoltage. Figure 3.14 shows the influence of the snubber resistor value. These results have been obtained with the worst case scenarii: the maximum current (at the corresponding diode, and therefore voltage, 3.6kV and 2.4kA, 2.8kV and 3.8kA) going through the biggest snubber inductor (3.4µH).

Regarding the capacitor size influence, with a bigger capacitor the overvoltage across the IGCT is reduced. But there is a compromise to make between overvoltage across the IGCT and the size of the capacitor. If we consider the energy density of the capacitors to be constant with the same technology and similar voltage ratings, then a 10µF/6kV capacitor would be twice the size of a 5µF/6kV capacitor which would be 5 times the size of a 1µF/6kV capacitor, for a few hundreds of volts difference regarding the overvoltage between each configuration. That is why it is important to set a clear level of tolerated overvoltage.

Regarding the resistor size influence, two conclusions can be drawn. With a lower resistance value (0.1Ω in figure 3.14), the overvoltage due to the discharge of the snubber inductor is reduced. But in that case, the snubber inductor cannot be completely discharged after 40µs, which would be source of failure. With a high resistance value (1Ω on the displayed simulations), the overvoltage can exceed the imposed limit. There is here an optimum to find for the resistor value as well.

After simulations and analysis, it has been decided to stand by a 5µF/6kV capacitor (a E51.S11-502R20, from UPE, with a volume of 1.7L) and 0.5mΩ/800W resistor. 5µF and 0.5 Ω are values that are within the typical values of a snubber capacitor and resistor in the literature (see table 2.4).

A last point about the figures 3.13 and 3.14 is that the sudden drop of voltage on the IGCT voltage waveform is due to the unrealistic behaviour of the ideal components used for the simulation.

3.2.4 Analysis of the snubber volume

In this setup, the maximum volume of the snubber inductor is 1L (3.4µH inductor with dimensions RxH: 58mm x 96mm), and the volume of the capacitor is 1.7L, which is coherent with the model and the results in subsection 2.3.3.5. But as said in the same subsection, these theoretical volumes do not correspond to the real volume occupied by the snubber because it does not take into account physical assembly, clearance/creepage distances and the snubber diode. The real volume for this test setup is closer to 15L (calculated with AutoCad). It should be noted that the volume of the snubber has not been optimised in this study. What can be concluded though is that volume estimation of the snubber by estimating only the volume of its elements is underestimating largely the real volume occupied by the snubber.

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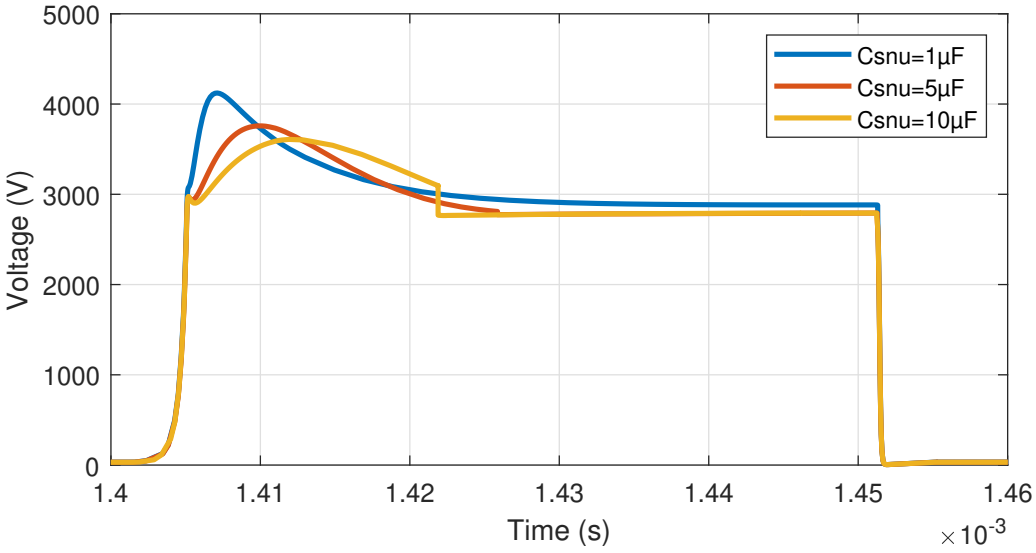
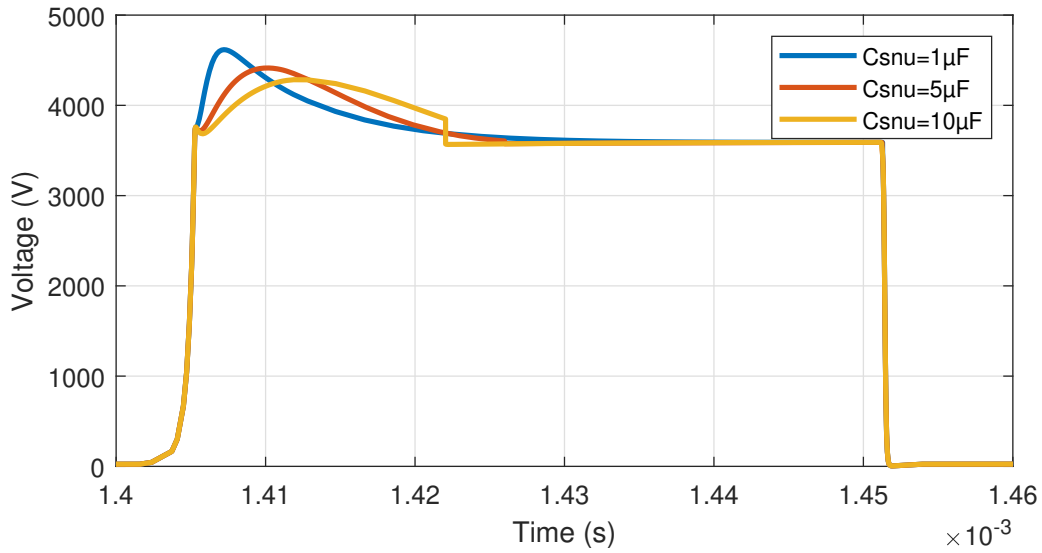


(a) Waveforms for a 2.8kV, 3.5kA pulse



(b) Waveforms for a 3.6kV, 2.4kA pulse

Figure 3.13: Voltage across the IGCT waveforms at turn-off of the IGCT, depending on the snubber capacitor size, with a snubber resistor of 0.5mΩ, no stray inductance, and the biggest snubber inductor (3.4µH). Obtained with simulation.

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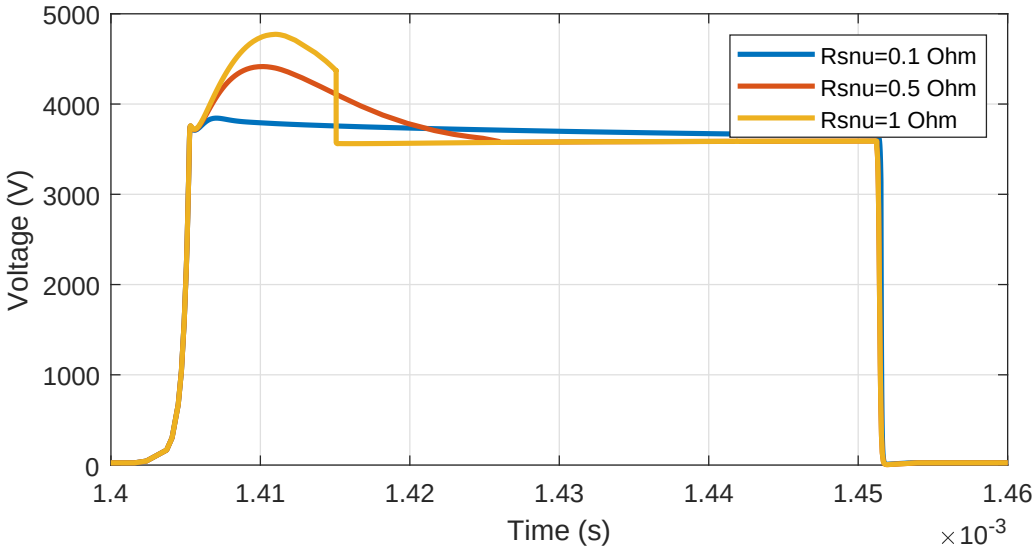
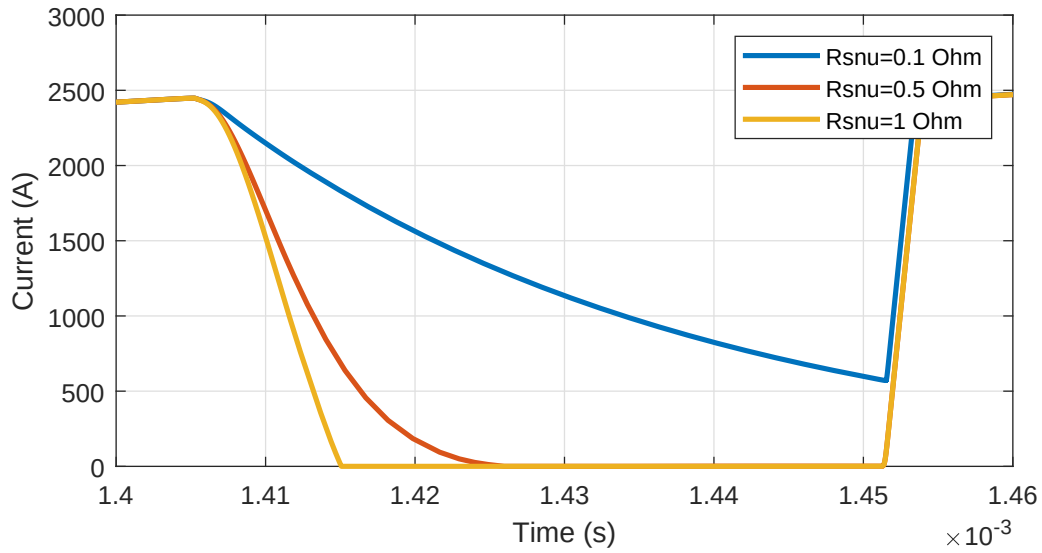


(a) Voltage across the IGCT waveforms for a 3.6kV, 2.4kA pulse.



(b) Current through the snubber inductor, waveforms for a 3.6kV, 2.4kA pulse.

Figure 3.14: Waveforms at turn-off of the IGCT, depending on the snubber resistor size, with a snubber capacitor of 5µF, no stray inductance, and the biggest snubber inductor (3.4µH). Obtained with simulation.

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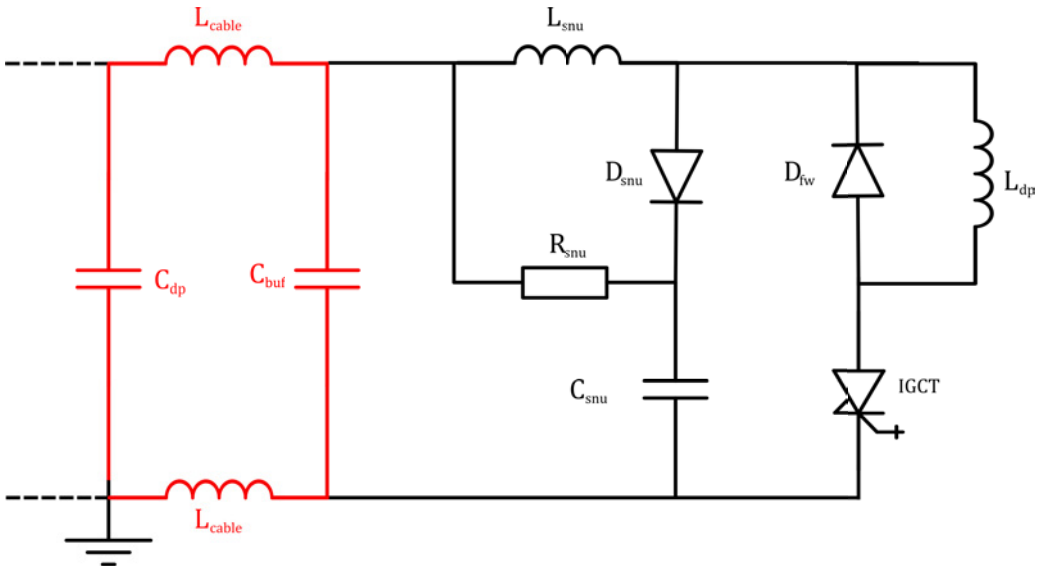

Figure 3.15: Buffer Capacitor, Capacitor bank and inductances created by the cables.

3.2.5 Buffer capacitor

The role of the buffer capacitor is to imitate the capacitor of a typical submodule (bulky film capacitor, close to the semiconductors devices) to limit the stray inductance to a typical submodule stray inductance. In the test platform HCSW the capacitor bank in place is far from the circuit (around 2m away, creating approximately 2×2µH of stray inductance by connecting it). For a 4µH inductance created by the cables between the commutation cell and the capacitor bank, the maximum di/dt at the turn-on of the IGCT would be less than 1kA/µs for voltage values under 4kV, which is far from the speed that is aimed at the turn-on of the IGCT (8kA/µs at 3.6kV and 13kA/µs at 2.8kV). To imitate the structure of a submodule and the behaviour of a typical submodule capacitor, a film capacitor C_{buf} has been added next to the switching cell (an AVX Trafim capacitor, see 3.20) rated at 3.8kV and 0.8mF, with two connectors. It is a lower capacitance value compared to typical submodules (see section 1.3) but is still representative, and is sufficient for double pulse tests. A capacitor bank C_{dp}, presented in section 3.3.1 will be used to increase the double pulse energy and reach all the desired values during the tests.

The buffer capacitance value C_{buf} has been assessed for its efficiency as a buffer and its behaviour compared to typical submodule capacitors (a few mF) with simulation, as it can be seen in figure 3.16. On the blue and orange waveforms (corresponding respectively to the values of 1µF and 50µF), the buffer capacitor is unable to remove or attenuate the oscillations and overvoltage due to the cable inductance. But the yellow and purple waveforms (corresponding respectively to the values of 800µF and 5mF) are very similar, and do not show the same oscillations or overvoltages. The voltage levels (at $t = 1.42ms$ for example) of the yellow and purple curves are slightly different: it is due to the fact that the bigger the whole capacitance of the circuit is $(C_{buf} + C_{dp})$, the lower the voltage drop after charge will be (as discussed in a following section 3.3.1).

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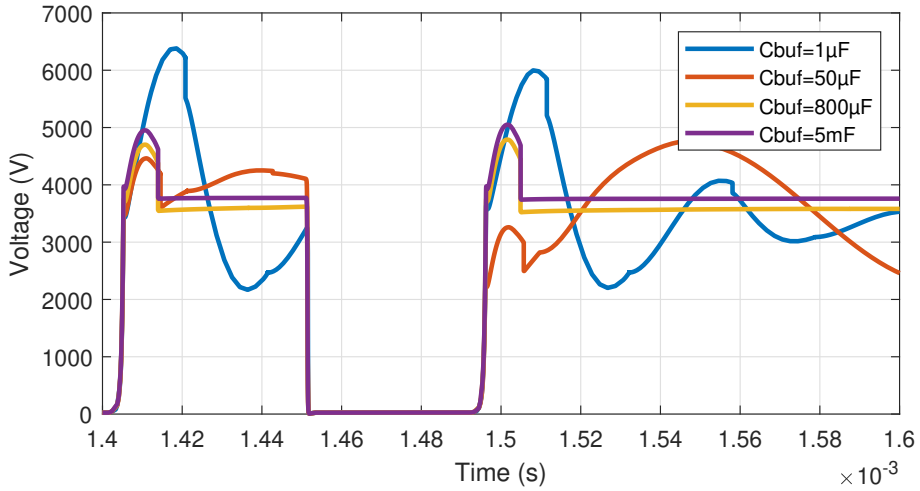

Figure 3.16: Simulation of the voltage across the IGCT, depending on capacitor buffer size, for a 3.6kV, 2.4kA pulse. The snubber values are: $L_{snu} = 3.4\mu H; R_{snu} = 0.5\Omega; C_{snu} = 5\mu F; C_{dp} = 1mF; L_{dp} = 0.8mH$.

3.2.6 Busbar design

The busbars are designed according to three factors: the rated current, the stray inductance of the overall circuit and the physical arrangement of the different components. Concerning the section of the copper, it has been based on ampacities/size of copper busbar tables given by the Copper Development Association. With the rating of 1.2kA of the 6.5kV diode, the size for the busbar for a temperature elevation of 65°C, 3.2mm x 76.2mm will be sufficient for this current rating.

Drawing the busbars is complex because they need to connect every component of the circuit with the smallest loop inductance. To do so, every geometry has to be taken into account, with mechanical support. The clearance distances have to be respected (here 14mm for 4.5kV working voltage, see table 1.6), and the frame has to be grounded. The final design of the busbars, after different steps and versions, is displayed in figure 3.17.

The different stray inductances of the busbars have been calculated with Ansys Q3D software. The results are displayed in figure 3.18. To complete these values, table 3.5 shows the values of the self-inductances of the components themselves (given by the components datasheets). Therefore, the whole commutation loop ($IGCT - D_{fw} - L_{snu} - C_{buf}$) reaches a total stray inductance value of approximately 450nH – approximative because this value depends on the frequency in particular. This value of 450nH corresponds to the value in table 3.3, for the maximum di/dt of the 6.5kV diode. This means that it seems possible to realise tests without failure due to high di/dt and without added snubber inductance.

Table 3.5: Values of self-inductances.

	C_{buf}	R_{snu}	D_{snu}/D_{fw}	C_{snu}
Inductance value (nH)	69	80	18	15

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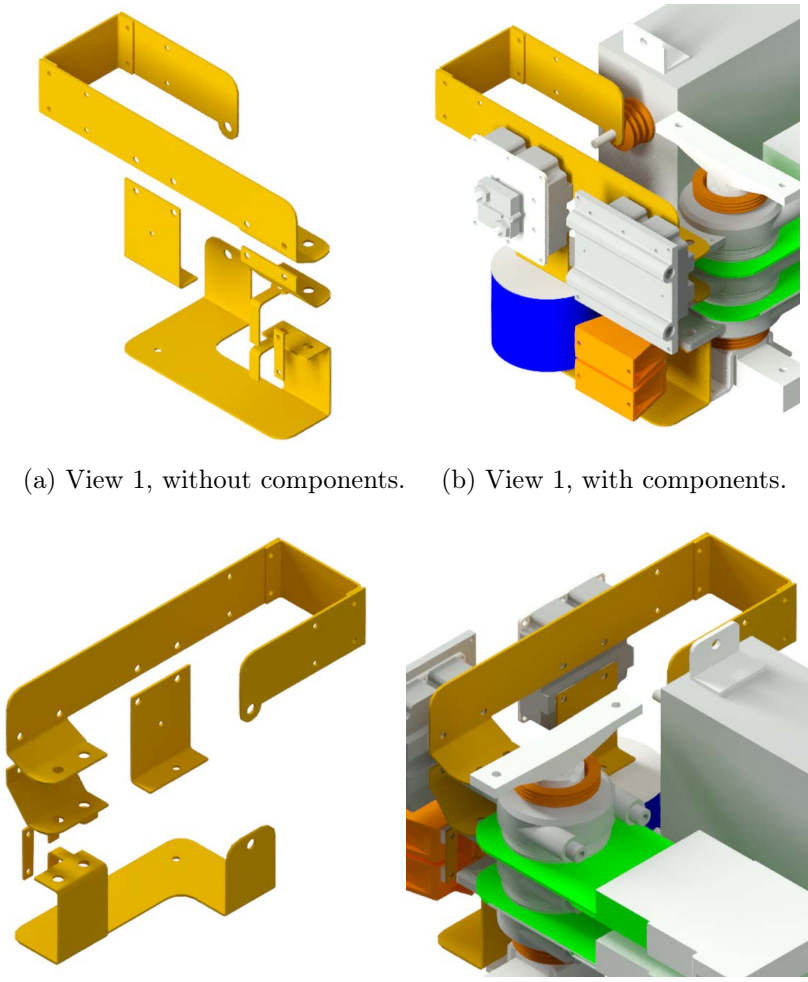

(a) View 1, without components. (b) View 1, with components.

(c) View 2, without components. (d) View 2, with components.

Figure 3.17: Busbar final design, different views, with and without components. The frame holding the whole setup is not displayed here for clarity purpose.

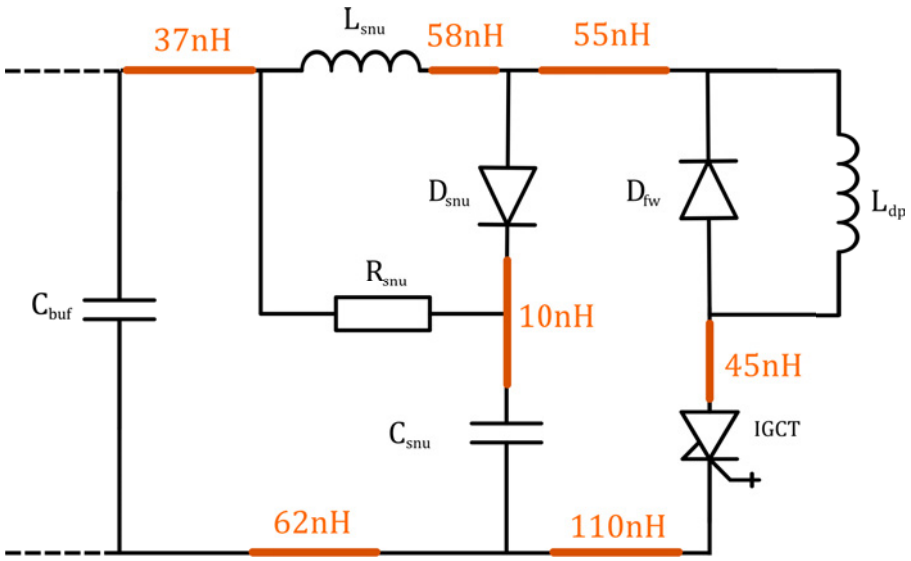

Figure 3.18: Stray inductance due to the busbars in the test circuit. Calculated with Q3D.

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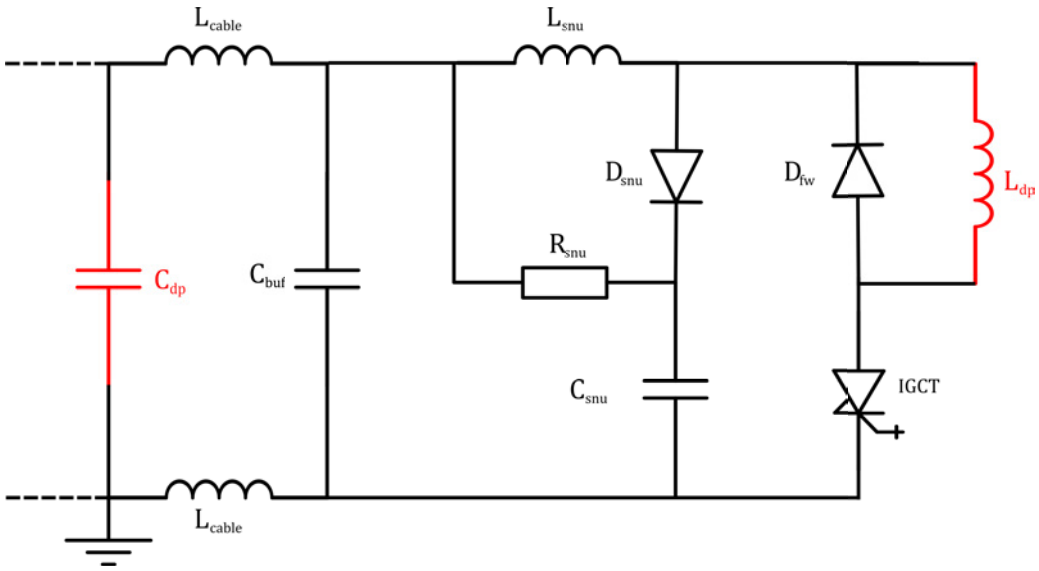

Figure 3.19: Capacitor bank and Charge inductor in the circuit.

3.3 Implementation of the rest of the test circuit

In this section, most of the elements of the circuit, not being part of the submodule structure (like the capacitor bank and the charge inductor) or the protection systems are presented.

3.3.1 Capacitor bank and Charge Inductor

Considering the different elements of the circuit, presented in the last section 3.2 the desired extreme values for the measures during the experiment are:

- Max. current: 2400A. Min. current: 100A.
- Max. voltage: 2800V for the 4.5kV diode, 3600V for the 6.5kV diode. Min. voltage: 800V.

These values define the size of the added capacitor bank and the charge inductor, as shown in figure 3.19. These elements are normally designed at the same time (as an overall optimisation). But in this thesis work, these setup parts being chosen among the elements available in SuperGrid Institute, the capacitor bank has been maximized (to reach all desired values of current and voltage) and the charge inductor has been verified to fulfill the criteria described later in this subsection.

Capacitor bank The capacitor bank capacitance value is supposed to be big enough to feed the energy of the inductor (to reach the aimed current) and limit the voltage drop during the inductor charge to reach the aimed voltage at t_1. The capacitor bank voltage rating has to be bigger than the maximum aimed voltage value for the tests (here 3.6kV). Considering the available components, we decided to use two capacitors of 2.5kV, 2.27mF in series, resulting

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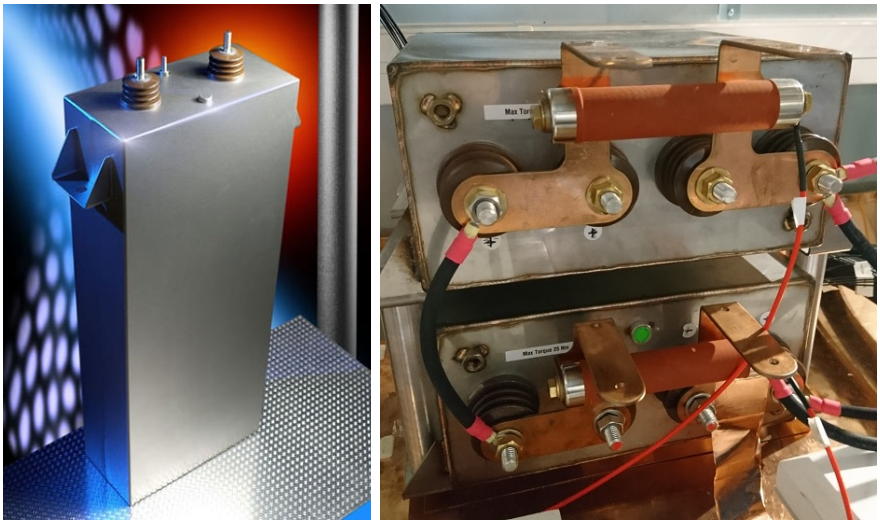

(a) Type of capacitor used. TRAFIM Series. (Source: AVX)

(b) Implementation on the circuit.

Figure 3.20: Capacitor bank.

in a capacitor bank of 5kV, 1.135mF, adding to the buffer capacitor of 0.8mF. The voltage balancing between the two capacitors is acquired with two resistors of 2.1MΩ, serving as well as slow discharge resistors.

Charge Inductor Qualitatively, the inductor inductance value is an optimum between current growth during charge (phase B and D, see figure 3.2), current drop during freewheeling phase C, voltage drop during phases B and D, and energy to evacuate during phase E. The bigger the inductance value is, the bigger the voltage drop during phase B and D, and the bigger the energy to evacuate by the diode during phase E. But if the inductance value is too small, then the current will grow too fast during phase D.

Quantitatively, these parameters are evaluated with: the minimum duration between two pulses (the IGCT gate unit requires 40µs between successive switching events), the maximum ratings of the different components, the ranges of the aimed current and voltage values, and the energy to evacuate in the diode which can be derived from the I^2t that the freewheeling diode can withstand. All these criteria are described in the table 3.6. All of them do not have to be fulfilled at the same time: different inductor values can be used depending on the test points. For example, a lower inductance value can be used for high voltage pulses to avoid too big of a voltage drop or a bigger inductance can be used for high current pulse to avoid exceeding the IGCT current limit at the second turn-off event (at t_3).

Table 3.6 was built with the extreme values aimed for this experiment, presented at the beginning of this subsection, and the selected diodes I^2t (displayed on their datasheets).

On top of the criteria described in table 3.6, the resistance value of the whole inductor as well as the mechanical strength – because of the possible 4kA pulses – are important here. In SuperGrid Institute, an inductor is already in place, able to withstand mechanically 4kA pulses, with different possible values by connecting on mid-connectors (391µH, 782µH, 1.45mH, 2.74mH). This inductor is limited to 50mΩ, and fulfills all criteria identified in the table 3.6,

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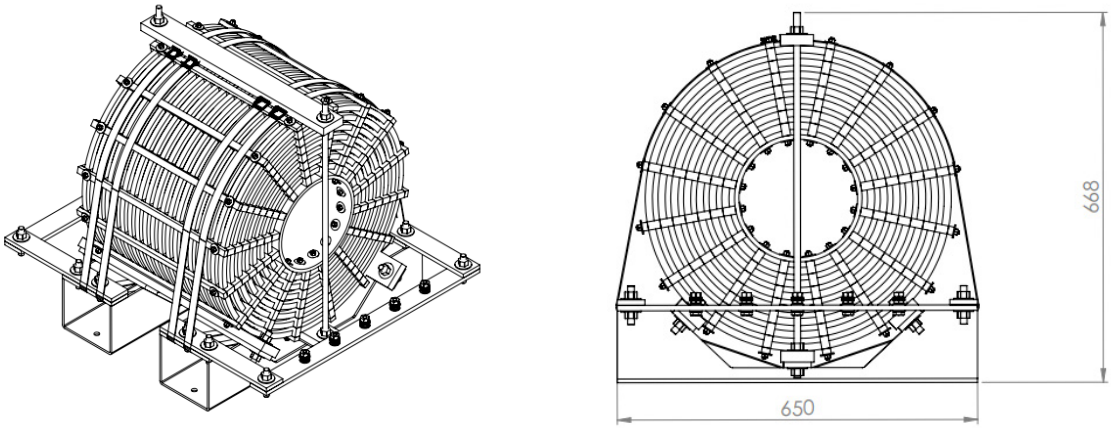
Table 3.6: Set of criteria for the choice of the inductance value of the charge inductor.

Criteria	***Values for the test setup***	***Main influencing circuit parameters***	***Top or Bottom limit for L***
Allowed drop in voltage during phase B	4kV to 2.8kV to reach 2.4kA (4.5kV diode) 4.5kV to 3.6kV to reach 2.4kA (6.5kV diode)	C_{dp} and L_{dp} sizes R of the whole circuit	Top
Minimum current value at the end of phase B	100A after 40µs	L_{dp} size	Bottom
Allowed drop in current during phase C	50A in 40µs	R_{on} of the diode L_{dp} size	Bottom
Allowed drop in voltage during phase D	–	C_{dp} and L_{dp} sizes	Top
Allowed increase in current during phase D	100A in 40µs	L_{dp} size	Bottom
Energy to evacuate during phase E	6000A on 10ms (half-sine)	R_{on} of the diode L_{dp} size	Top



(a) Inductor for double pulse, view 1.

(b) Inductor for double pulse, view 2.

Figure 3.21: Charge inductor for double pulse in SuperGrid Institute platform. Lenghts are in mm.

by changing its value depending on the desired pulses.

3.3.2 Temperature control System

The role of the temperature control system is to allow the tests at different temperatures. Indeed, in real HVDC MMCs, semiconductor devices heat up, so testing the semiconductor devices at different temperatures is crucial. Because the semiconductor devices datasheets display values up to 125°C, the whole temperature control system has to be designed to reach 125°C. Its also has to ensure electrical insulation between parts, especially since the heatsinks of the IGCT also provide electric connections. The designed cooling system is using a Julabo A40 as a thermostat, EPDM Rubber pipes and HL60 cooling liquid. The EPDM rubber is compatible with silicon oils (like the HL 60 cooling liquid) and is an electrical insulator (more than 20kV/mm dielectric strenght). The selected pipes can withstand 164°C and 6bars. The HL60 cooling liquid is also insulating (resistivity of $4.10^{14}\Omega.cm$) and works in the temperature range from -60°C to 250°C.

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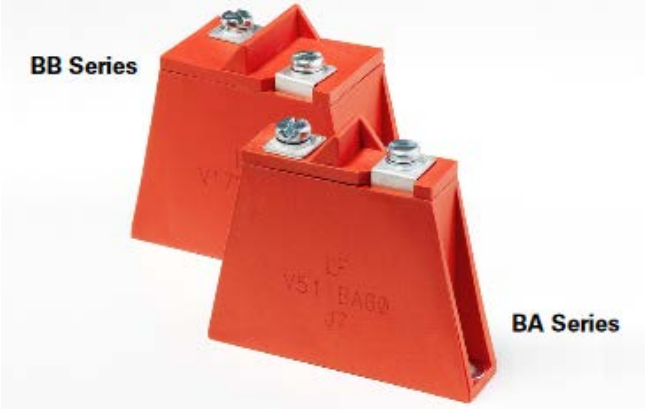

Figure 3.22: MOVs used for IGCT overvoltage protection. (Source: LittleFuse)

3.3.3 Protection elements

Varistor for overvoltage protection A voltage surge could occur when the IGCT opens while the diode is in open-circuit failure mode and the charge inductor L_{dp} has a non null current going through. Because of the continuation of current through the inductor, this provokes a high voltage surge across the IGCT, which could lead to its destruction. To protect the IGCT from this voltage surge, Metal-Oxide Varistors have been selected from the LittleFuse catalog. Two varistors V112BB60 in series are connected parallel to the IGCT. The obtained equivalent MOV is conducting 2kA at 6kV and 2mA at 3.7kV. This type of varistor is displayed in figure 3.22.

Safety Freewheeling diode for IGCT protection If the diode fails into open circuit failure mode and the IGCT into short circuit failure mode, then the charge inductor and bank capacitor would form an oscillating circuit which could damage the IGCT by imposing a negative voltage across the IGCT. To protect the circuit from this scenario, a safety freewheeling diode has been installed parallel to the capacitor bank (D_{protec} in figure 3.3). The safety freewheeling diode has to be able to withstand the surge current, which is determined by calculating the I^2t that goes through the diode in the worst possible case: the charge inductor with maximum energy, so at its maximum current (for the calculation here 4kA). The selected diode is the LS412660 from Powerex, two of them are connected in series to reach the voltage of 5.2kV. Its I^2t is 1.81 MA^2s and is greater than the calculated maximum of I^2t in case of failure (0.52 MA^2s).

Protective screen As shown in figure 2.19, extracted from [128] where diodes are tested at di/dt higher than their limits, a strong explosion can happen. To protect equipment from such an explosion, a protection has been designed: a 10mm thick polycarbonate screen.

HV Relays To ensure the user safety of the setup, high-voltage relays controlled by voltage source have been installed. (from the E12 type in Ross Engineering catalog) A normally open relay is connecting the source to the capacitor bank. Two normally closed relays are connecting the capacitor bank to a rapid discharge resistor, to ensure a proper discharge of the capacitor bank, and to the ground, to ensure a proper grounding of the whole setup. These relays can

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Figure 3.23: High-Voltage Relay used in the circuit. (Source: Ross Engineering)

be seen drawn in the circuit in figure 3.3. A picture of this kind of relays is displayed in figure 3.23.

3.4 Finalised setup and conclusion on the test setup

In this chapter, the process of designing the test setup for the experiments that will be run in this thesis has been presented. One of the main achieved goals of this test setup is to imitate the structure of an HVDC MMC submodule to allow extrapolation of the results of this study to real HVDC MMC submodules. This part of the setup has been presented in the second section, with the choice of the semiconductor devices, the design of a realistic snubber, realistic busbars and the use of a representative capacitor. The other parts of the setup have been presented in the third section. The main limit of the setup is that it is not possible to modify the value of the stray inductance imposed by the mechanical structure, which could have been interesting.

Overall, this test setup will permit to study efficiently the reduction and potential suppression of the snubber. Views of the finalised experimental setup can be seen in figure 3.24.

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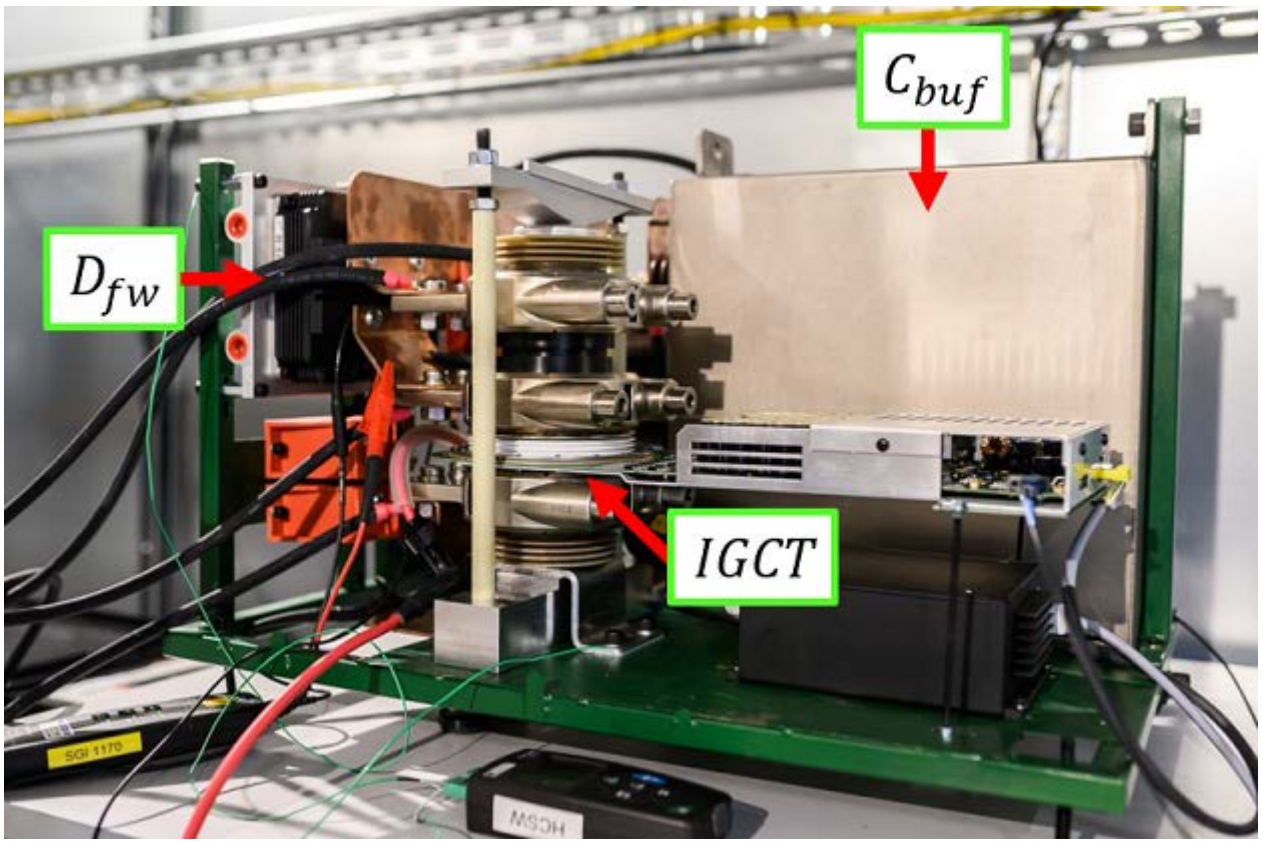
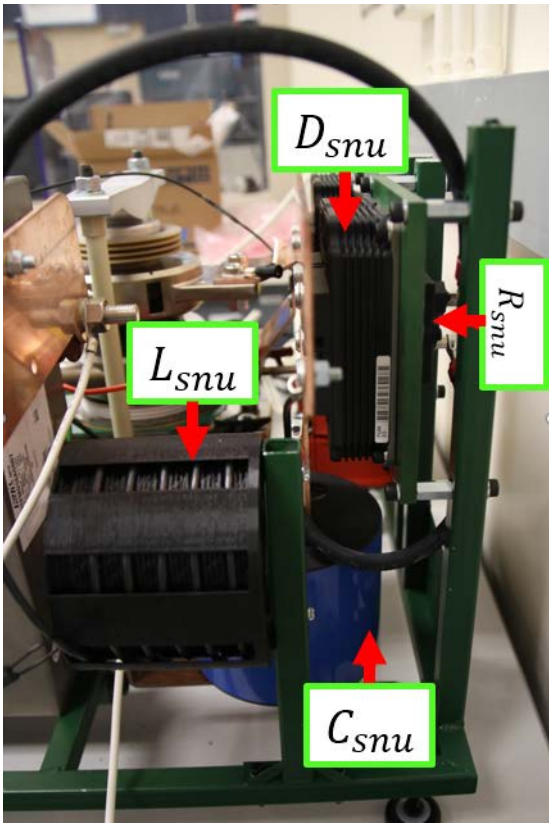


(a) Left View. Picture taken in SuperGrid Institute.



(b) Right View. Picture taken in CPES.

Figure 3.24: Views of the finalised setup with annotated main components.

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Chapter 4

Commutation of an IGCT with fast Silicon diodes

The precedent chapter focused on the design of the test setup for the study of an IGCT coupled with different Silicon diodes with fast recoveries. This chapter will now logically focus on the results of this study. But because the comprehension of the study and its conclusions rely on the understanding of the reverse recovery event, this chapter will be organized as follows:

- a first section consisting of a comprehensive explanation of the phenomenon of reverse recovery through a literature review. The diode reverse recovery being the limiting phenomenon for a potential IGCT based submodule without turn-on snubber, as discussed in chapter 2, it is essential to understand the reverse recovery thoroughly. As a reminder, a high di/dt provokes the destruction of the diode. Therefore a turn-on snubber composed of an inductor and an RCD clamp is installed in the submodule to limit the di/dt level.

- A second section consisting in analysing the obtained waveforms and the results of the experiment with the silicon diodes and its comparison with the literature studied in the first section.

4.1 Literature review on reverse recovery and its destructive modes

The goal of this section is to understand the behaviour of PiN diodes during reverse recovery and the parameters influencing recovery such as operational and design parameters.

It first starts with some useful definitions, then describes the reverse recovery phenomenon – what happens in the semiconductor, what types of recoveries exist and what influences the reverse recovery. Then, a focus on snappy recovery and its origin and destructive modes will be presented. The dynamic avalanche, a potential destructive mode for the diode during reverse recovery will be addressed later. This section will finish with the typical trade-offs which are encountered during the design of silicon PiN diodes.

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4.1.1 Useful definitions

These definitions below are simplified for the ease of the reader and are displayed here as an introduction to concepts used in this chapter. For more detailed explanations, you can refer to the books of Lutz [67] or Baliga [8].

Unipolar and Bipolar semiconductor devices An unipolar semiconductor device uses only one type of carriers to ensure conductive mode, such as the Schottky diode, using only electrons. A bipolar semiconductor device uses both types of carriers during on-state and relies on the injection of minority carriers, such as the PiN diodes relying on holes injection. These minority carriers have to be removed during the turn-off, provoking a reverse recovery in diodes, described in section 4.1.3.

Lifetime and Recombination The lifetime of a carrier (hole or electron) is the average time it takes for a carrier to recombine (with a hole for an electron and vice versa). Often considered as the minority carrier recombination time, it is composed of three main mechanisms [67]: radiative band-to-band recombination, Auger recombination, and recombination via a deep-energy level. The last mechanism is the main mechanism in semiconductors. Recombination centers (also called traps) are impurities in the semiconductor such as gold, widely used for that purpose, where the recombination is facilitated. By controlling the concentration of impurities, the lifetime of carriers is controlled and therefore the properties of the semiconductor, such as on-state resistance or switching losses, are controlled: the longer the lifetime, the lower the conduction losses and the higher the switching losses.

Mobility Mobility is defined in a material as the average speed of a carrier (hole or electron) when subjected to an electric field. It depends obviously on the scattering that encounters a carrier such as vibrating lattice atoms or impurity ions [67]. The mobilities of electrons and holes inside the semiconductors are different. The mobility, along with the doping concentration, defines the conductivity of the material.

Impact ionization and avalanche Impact ionization is the process during which a highly energetic carrier creates one more free carrier in the semiconductor by giving some of its energy to a carrier in the valence band. The energy of the first carrier is big enough to create a new free carrier while still being a free carrier itself. This happens especially at high voltage where carriers have higher energy. Impact ionization is the cause of avalanche at high voltage: exceeding a certain voltage leads to a snowball effect with more carriers with high energy creating more carriers by impact ionization. All these created carriers form the avalanche current going the opposite direction to the normal current direction. This current, combined to the voltage applied at the same time, can lead to overheating and destruction of the semiconductor.

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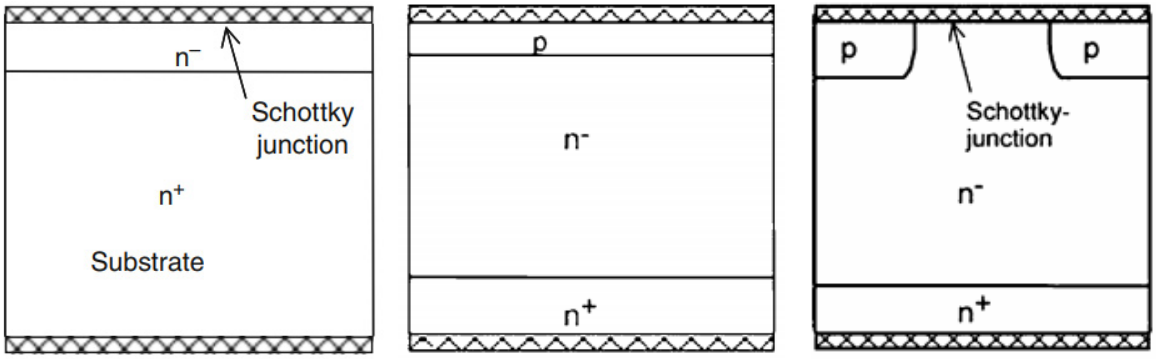

(a) Schottky diode. (b) Pin Diode. (c) MPS Diode.

Figure 4.1: Structures of power semiconductor diodes. Figures extracted from [67]

Table 4.1: Comparison of Schottky and PiN silicon diodes.

	Schottky Diode	Pin Diode
Junction type	Metal-N	P-N
Conduction Type	Unipolar (electrons)	Bipolar
Typical Voltage rating (for Silicon)	up to a 200V	up to 6.5kV
Voltage drop (V)	Lower	Higher
Drift region resistance	Higher	Lower

4.1.2 Types of diodes in Power Electronics

Two main types of diodes are found in power electronics: the Schottky diode and the PiN diode. Each one of them are based on a junction: metal-semiconductor junction for Schottky diodes, P-N junction for PiN diodes. Their typical structures are displayed in figure 4.1. Table 4.1 summarises the comparison between the two types of diodes. Some other structures can be found which often are derived from Schottky and PiN diodes, such as the MPS diode for "Merged Pn-Schottky" diode, a mix between the two structures.

With silicon as the semiconductor material, Schottky diodes are often rated at less than 200V or 100V [8, 67], due to their on-state voltage drop, too high compared to PiN diodes at higher voltages. For higher ratings, silicon PiN diodes are used in converters. In HVDC MMCs, where voltages requirements are between 1.7kV and 10kV, only silicon PiN diodes are found.

To give some perspectives, the on-state voltage calculation of a Schottky diode with a blocking voltage of 1000V, a current density of $100A/cm^2$, and a barrier height of 0.7eV, would be 18.75V. For the same current density, same blocking voltage and a lifetime of 1µs, a PiN diode would have an on-state voltage of 0.8V [8].

But for wide-band gap semiconductor material, such as silicon carbide, Schottky diodes are found at voltage ratings such as 1.7kV or 3.3kV, due to the much lower drift resistance. For indication, in [8], a figure of an approximately 2000 smaller specific on-state resistance is given for the SiC Schottky diode compared the Si one (for the same breakdown voltage). But silicon carbide PiN diodes can also be found like in [6], at a rating of 10kV, at a prototype stage.

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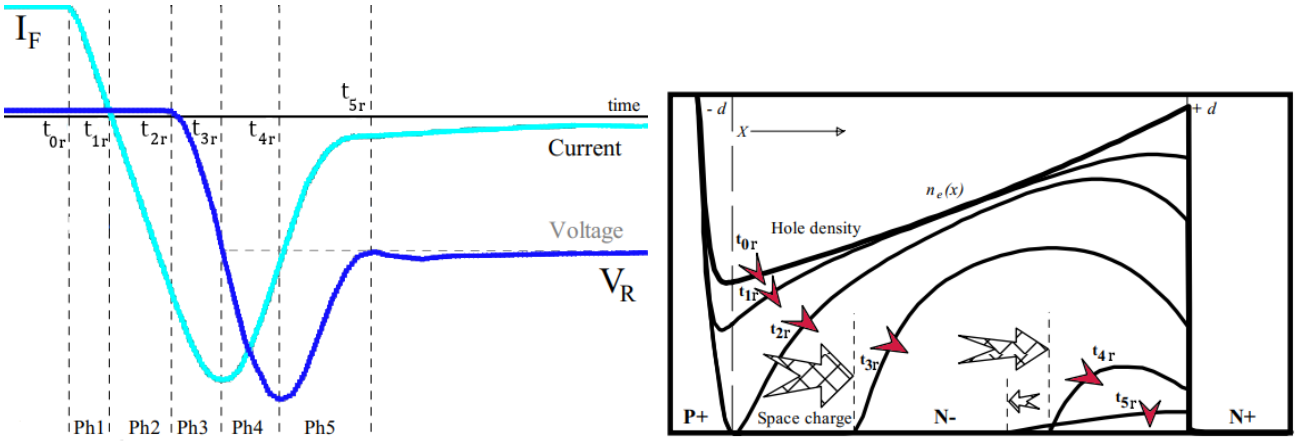

(a) Waveforms.

(b) Excess carriers (holes) dynamic.

Figure 4.2: Phases and instants in Reverse Recovery, adapted from [90].

In the end, silicon PiN diodes are mostly found in power electronics converters with high voltage and high current ratings. These diodes, as seen in this section, are bipolar devices and therefore are subject to reverse recovery, a phenomenon that will be described in the next section.

4.1.3 Reverse Recovery

4.1.3.1 Typical waveform and charges dynamics

Because the PiN diodes are bipolar devices, minority carriers participate to the on-state of the diode, but these need to be removed during the transition between on-state and off-state. This charge removal creates a transitory negative current called reverse recovery. A typical reverse recovery waveform is displayed figure 4.2. [90] describes reverse recovery in 5 phases:

A Commutating phase (Ph1): the current decreases until I_{dio}=0.

B Storage phase (Ph2): the current keeps decreasing until the di/dt starts decreasing. The voltage has not started to increase.

C Voltage build-up phase (Ph3): The voltage starts to increase until it reaches V_R and $I_{dio} = I_{rr}$.

D Inductive phase (Ph4): this phase is called that way because it stops at $V_{dio} = V_{max}$ and corresponds to the effect of the stray inductance of the circuit.

E Recovery phase (Ph5): the rest of the reverse recovery.

A first inductive phase (phase 1 + phase 2) takes place when there are excessive minority carriers everywhere in the drift region. During that phase, no space charge can form and the voltage across the device is still equal to on-state voltage as long as there are minority carriers

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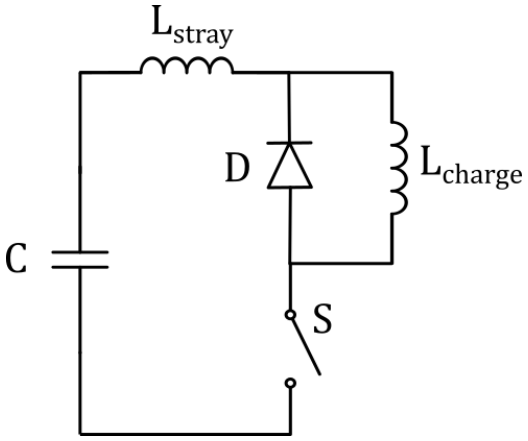

Figure 4.3: Simple explanatory circuit schematic for reverse recovery.

in excess. The stray inductance of the circuit (L_{stray} in figure 4.3) supports the whole voltage and dictates the rate of current drop, the di/dt. ($\frac{di}{dt} = \frac{U}{L}$)

At t_{2r}, the excess of charges at P+N- junction disappear, the depletion region starts to grow and block voltage at a rate of dv/dt until it reaches V_R at t_{3r}. When the diode reaches for the first time the value of V_R, the inductance of the circuit does not support any voltage. Therefore at t_{3r}, when $V_{dio} = V_R$, $di/dt = 0$ and $I_{dio} = I_{rr}$.

The charges removal keeps on going at a slower rate after, di/dt becomes positive and corresponds to the inductance voltage changing sign, creating an overvoltage on the diode, with the maximum at t_{4r}. Between t_{2r} and t_{4r}, during phases 3 and 4, capacitive effects take place: [90] models them with two different capacitors, C_j the junction capacitance based on the depletion layer charge and the displacement current, and the C_D the drift capacitance based on drift current.

The last part of the recovery is the decrease of the current through the diode to zero.

4.1.3.2 Parameters used to described the reverse recovery

Several key parameters can be used to describe a recovery event: the forward current I_F before diode turn-off, the voltage at the end of diode turn-off V_F, the current slope when the current starts to be negative $di/dt(I = 0A)$, the reverse current peak I_{rr}. The time at which the current reaches 0 for the first time will be called t_{1r} in this thesis.

The parameters above do not need any calculation or standardisation, unlike the recovery duration T_{rr}, the recovery charge Q_{rr} and the recovery energy losses E_{rr}. Indeed these last parameters are related to one question: when is the reverse recovery considered over? On that point the JEDEC – Joint Electron Device Engineering Council – has standardized this matter in the section 5.6.9 of the standard covering Silicon Rectifier Diodes (reference JESD282B.01 [49]). For reverse recovery related calculations, the end of the reverse recovery is obtained by using the values I_{rr} and 25% of I_{rr}, determining a linear interpolation and obtaining the time for when this linear interpolation crosses the time-axis, like it is displayed in figure 4.4. Here, the obtained time is called t_{5r}. The reverse recovery, when the current is negative, is cut into

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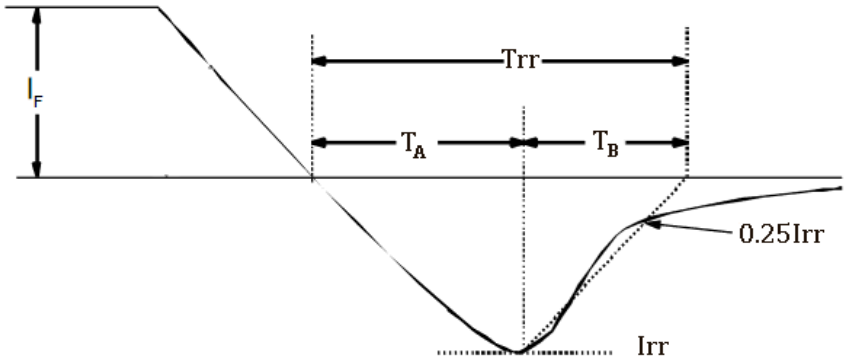

Figure 4.4: JEDEC standard definition for reverse recovery time. [49]

Table 4.2: Parameters describing Reverse Recovery (RR).

Parameter	Description
V_R	Reverse Voltage
I_F	Forward Current
$di/dt(I = 0A)$	Decreasing current rate at 0A
I_{rr}	RR peak current
T_{rr}	RR duration, defined in Jedec 282B.01
Q_{rr}	RR charge, $Q_{rr} = \int_{t_{1r}}^{t_{5r}} I_{dio}.dt$
E_{rr}	RR Energy, $E_{rr} = \int_{t_{1r}}^{t_{5r}} V_{dio}.I_{dio}.dt$
T_A	First part of RR, between $I = 0$ and I_{rr}
T_B	Second part of RR, $T_B = T_{rr} - T_A$

two parts: the first between t_{1r} and t_{3r}, that we are going to call the part A of the reverse recovery; and the second between t_{3r} and t_{5r}, that we are going to call the part B (see figure 4.4). On the table 4.2, a summary of these parameters describing reverse recovery are displayed.

4.1.3.3 Types of reverse recovery

The end-tail of the reverse-recovery transient defines the type of the reverse recovery. The reverse recovery is called "soft" when the di/dt of the B part is within a certain range (compared to the $di/dt(I = 0A)$) and slowly decreasing until the current in the diode reaches zero. On the contrary, a snappy recovery is a recovery where a brutal return to zero current happens, at a high di/dt, with sometimes a discontinuous d^2i/dt^2. Snappy recoveries examples are displayed in figure 4.5.

An intermediate is described in [90], called an oscillatory recovery, when the tail of the recovery is oscillating around zero current without a discontinuous d^2i/dt^2.

To differentiate the different types of reverse recovery, the different Jedec norms [49] have defined two softness-factors. The first one (equation 4.1) is obsolete because it considers the reverse recovery in figure 4.5a to be snappy and the reverse recovery in figure 4.5b not to be

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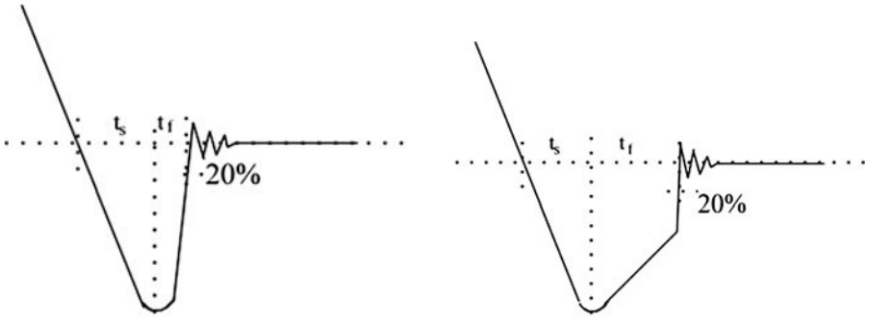

(a) Whole recovery B-part snappy. (b) Late snap-off.

Figure 4.5: Two types of snappy recovery. Figures extracted from [67]

snappy.

$$s_{RRSF-old} = \frac{T_A}{T_B} \tag{4.1}$$

$$s_{RRSF} = |\frac{\frac{di}{dt}i=0}{(\frac{di}{dt})_{B-max}}| \tag{4.2}$$

The softness-factor defined in the equation 4.2 considers the recoveries with a whole B-part being abrupt as well as a late snap-off to be considered snappy, like on both waveforms from figure 4.5. The problem with that softness-factor is that it does not differentiate these two types of snappy recovery. The question is: are these types of recoveries the same? This will be answered by the results developed in the chapter 5 and the theory developed in the following section 4.1.4.

An important point is that a soft-recovery diode (often designated as soft diodes for short) does not mean a slow diode: some fast diodes present soft recovery. A fast diode is a diode that withstand high di/dt(0A) levels during turn-off. The definition of a soft diode relies on the comparison of max. di/dt during the B-part of the recovery and the $di/dt(0A)$, not on the absolute value of one of these di/dt levels.

4.1.3.4 Operational parameters influence on reverse recovery

Here is a quick explanation of the main effects of operational (can also be called external) parameters (which are explained in [67] and studied thoroughly in [97]): higher temperature, higher forward current, higher di/dt or higher voltage tend to increase E_{rr}, I_{rr} and Q_{rr}. A higher temperature or higher forward current will tend to increase T_{rr} unlike a higher di/dt, which will have the opposite effect. A higher stray inductance will lead to a higher voltage peak at t_{4r}. Publications trying to provide the exact impact of increasing the voltage, while keeping a constant di/dt, have not been found, but according to [67] a higher voltage tends to worsen the reverse recovery.

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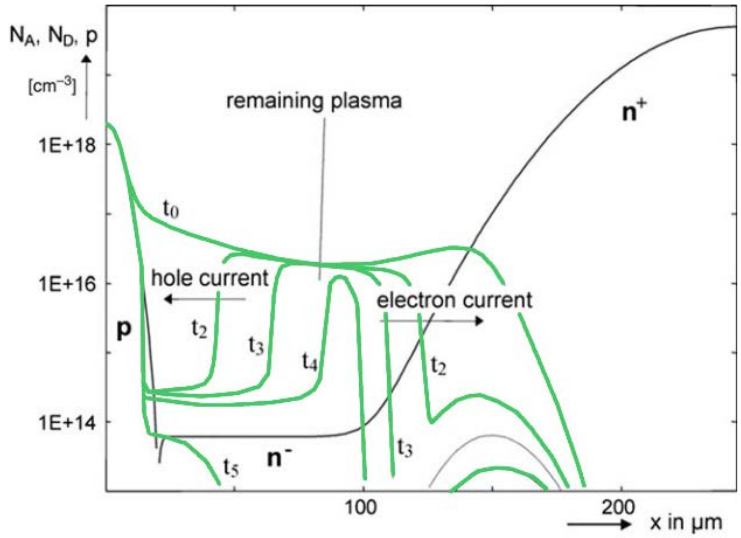

Figure 4.6: Snap-off plasma dynamics. From [67], colorized.

4.1.4 A focus on snappy recovery

4.1.4.1 Origin of the phenomenon

If the conditions explained in the next section 4.1.4.2 are met – not necessarily all of them – the diode displays snap-off behaviour at the end of the recovery: in the N- region, depletion starts from both sides (unlike in figure 4.2b) and the two plasma fronts end up meeting (see figure 4.6), concluding the plasma removal [67]. The plasma removal being the reverse recovery current source, the end of its removal while a consequent current is still present, provokes a steep current return to 0, leading to a snappy behaviour and overvoltages. This high current slope creates an overvoltage with the stray inductance of the circuit, through the equation $u = L_{stray}.di/dt$ [91].

4.1.4.2 Parameters influencing snap-off phenomenon

Diode design (internal parameters) In [90] different doping profiles are simulated to identify the diode design parameters that have an impact on diode snapiness. The first of them is the doping level at the P+ part of the diode: when the doping level in the P+ region is higher, there is more chance to have a diode with snappy behaviour. It is explained by the fact that if the P+ region is more doped, there will be more charges around the P+N- junction. The increased number of charges on that side will take more time to be removed and this extra time will lead to more charges removed on the N+ side, compared to a lower P+ doping level situation. If too many charges are removed on the N+ side, the reverse recovery will present double-sided penetration of the depletion region, leading to a snap-off.

The same reasoning can be applied to the N+ doping level: when the N+ doping level is higher, more charges are injected on that side and the double sided penetration phenomenon is reduced. Regarding the base, a thinner layer makes the diode snappier and a lower N- doping level makes the diode snappier too. This is due to a higher penetration of the depletion region

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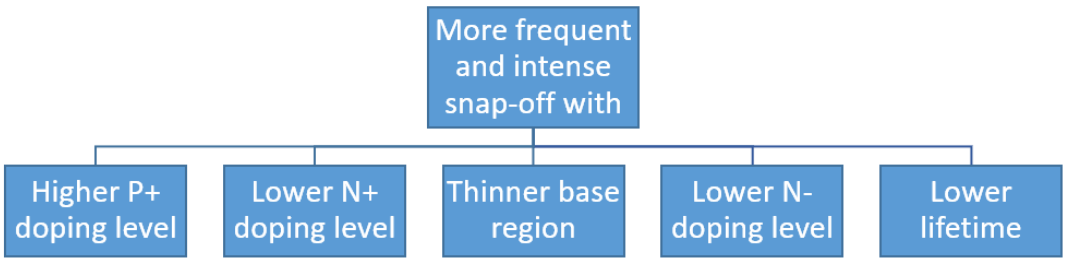

Figure 4.7: Diode design parameters influence on snap-off behaviour.

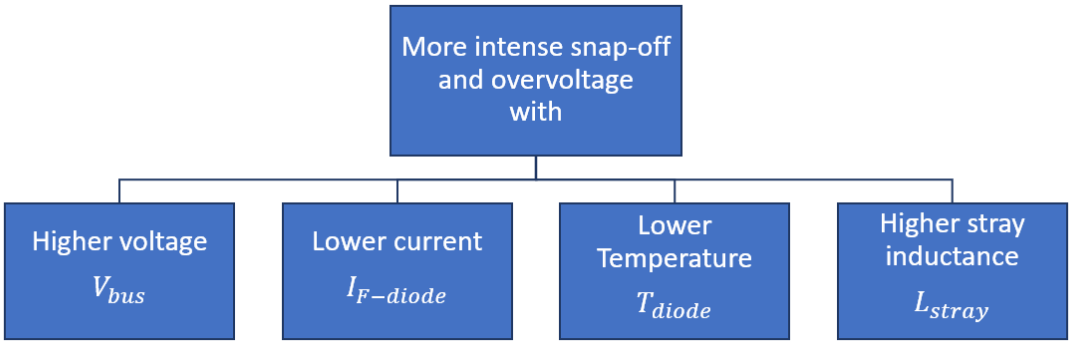

Figure 4.8: Operational parameters influence on snap-off behaviour.

in these cases. The carrier lifetime plays a key role in the snapiness of the diode as well: when the lifetime is lower, the charges tend to disappear near the ends and move towards the middle, leading to snap-off. The impact of the diode design on the snap-off as described in [90] is summarised in figure 4.7.

In [13, 14], lifetime zoning is studied and the result is that a non-uniform carrier lifetime is preferable to reduce snap-off with a lifetime reduced on the P+ side and increased on the N+ side. This is done to stimulate charge removal on the P+ side in priority.

Operational parameters (external parameters) The influence of operational parameters (that can also be called external) is widely studied in [72, 90, 97]. These results can be summarised with figure 4.8. Lower current means fewer minority carriers and a smaller plasma. Higher voltage level leads to a more intense snap-off. Higher temperature means more stored charges for the same current and voltage, and therefore lower snap-off. An increase in stray inductance augments the overvoltage during the commutation, leading to the same effect as a higher voltage level: more frequent and intense snap-off.

Even diodes designed for soft recovery can present snap-off behaviour under certain conditions and in particular with specific operational parameters (current, voltage, temperature and stray inductance), as it has been presented in [97, 64] for example.

In [64] is exposed that on-state duration also plays a role in snappy recovery: if the diode has

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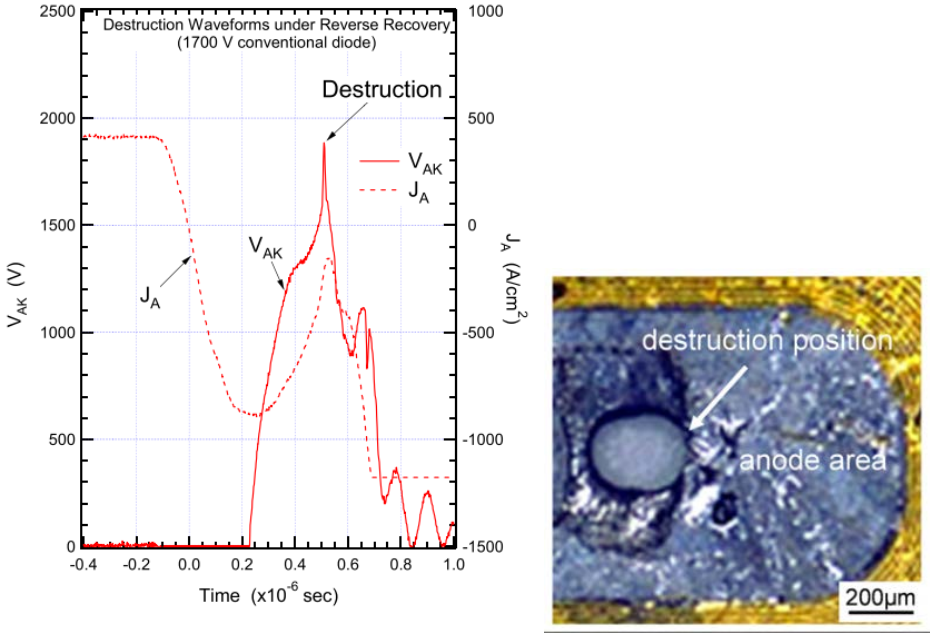

(a) Waveforms.

(b) Die anode view.

Figure 4.9: Snap-off destructive event on a 1.7kV diode, extracted from [82]. Bus voltage V_{CC} = 1200 V, current density J_F = 400 A/cm2 (×2.0 nominal current), current density slope dJ_F/dt = 5080 A/cm²/µs, L_S = 2µH, 398 K.

not been conducting current for long enough, and therefore the minority carriers distribution is not ideal, the diode can show snappy recovery behaviour, even if this diode is identified and sold as being a soft one.

4.1.4.3 Destruction by overvoltage due to snap-off

The snap-off at the end of the recovery can be destructive. [90] describes that if the voltage during snap-off goes over a certain limit, the snap-off is destructive, without explaining how to calculate this limit. [13, 14] describe that snap-off can lead to destructive electric field, although it does not detail. The goal of this section is to try to go further and explain the chronology of the events happening in the semiconductor during the failure due to snap-off. An example of snap-off related failure is displayed in figure 4.9.

[67, 82, 90] permit together to draw that chronology. As explained in 4.1.4.1, [90] explains that during snap-off, the depletion layers penetrates the drift region (N-) from both sides (P+ and N+). This double penetration causes an electric field to develop in the N-N+ region, which does not happen during normal soft-recovery operation. The plasma fronts meet, the current reaches 0 very quickly, an overvoltage occurs. At that moment, the electric field is an Egawa-type field [25] – or also called hammock-shaped field in [82], with a high electric field on the N-N+ interface. The difference between a trapezoidal field and an Egawa-type field is displayed in figure 4.10. Destruction of the diode then happens by avalanche breakdown, localized in a hot spot/filament, leading to overheating, and eventually exceeding the melting point of silicon. It seems that, according to [82], the filament builds up in the center of the active region, as it can be seen in figure 4.9b. The chronology of the snap-off failure is summarised in figure 4.11.

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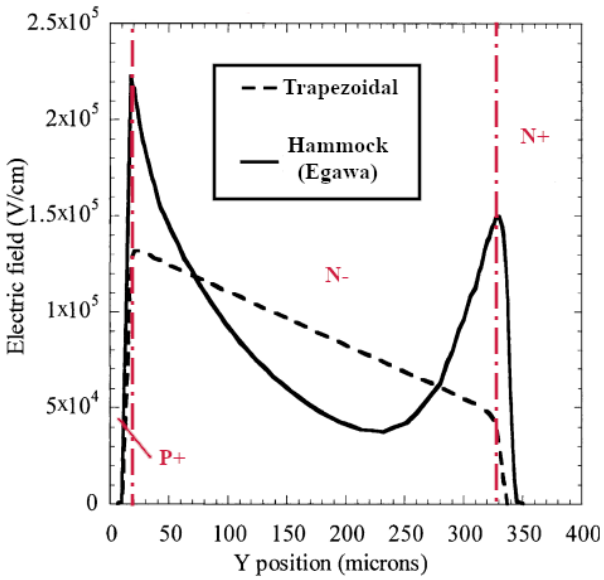

Figure 4.10: Difference between an Egawa-type field (or hammock-shaped) and a trapezoidal field. Adapted from [66].

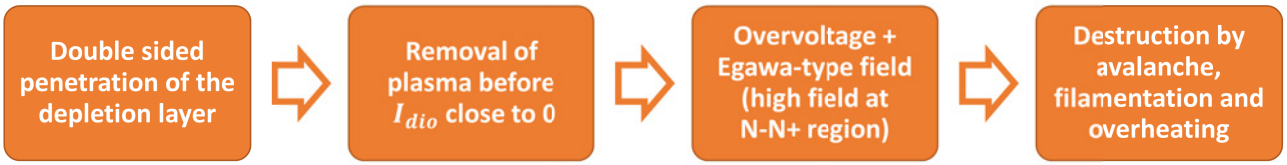

Figure 4.11: Chronology of the diode failure due to snap-off.

4.1.5 Dynamic avalanche

An another phenomenon in the diode can lead to failure during reverse recovery: the dynamic avalanche of 3rd degree. The dynamic avalanche is when, during reverse recovery, avalanche takes place below the breakdown voltage, due to the presence of charges in the drift region. Dynamic avalanche will be presented in this section.

4.1.5.1 The phenomenon and its different degrees

During reverse recovery, when the space charge region grows, a hole current is going through the space charge region at the saturation drift velocity. These moving charges add to the background doping and an effective doping can be considered [66, 67, 90] instead of the background doping during reverse recovery. The hole density is depending on current density: the higher the current density, the higher the hole density in the space region, and therefore the higher the effective doping. This means that for high reverse recovery current, the dynamic avalanche voltage threshold is low.

[66] gives the example of reverse current density levels at which starts dynamic avalanche for a 1.7kV diode and a 3.3kV diode. This phenomenon starts at 60A/cm^2 for the 1.7kV diode,

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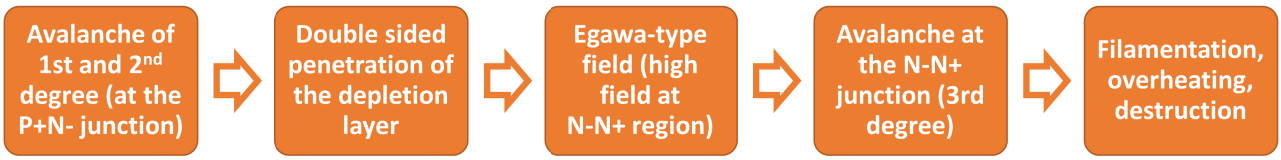

Figure 4.12: Chronology of the diode failure due to high di/dt.

and 30A/cm² for the 3.3kV diode. But for examples of significant drops in the withstanding voltage, at 200A/cm², the dynamic avalanche starts at 1000V for the 1.7kV diode and 1100V for the 3.3kV diode. These levels of reverse current densities can happen during reverse recovery for high di/dt.

Dynamic avalanche can be divided into three different degrees [66, 67]:

- 1st degree: beginning of dynamic avalanche and impact ionization at the P+N- junction.
- 2nd degree: a filament is forming at the P+N- junction.
- 3rd degree: an Egawa-type electric field forms, filament is forming at the N-N+ junction and the diode ends up being destroyed by overheating.

During 2nd degree avalanche, couteracting events make the step between 2nd and 3rd degrees significant [66, 67]: the temperature rise due to the filament will increase locally the avalanche voltage, the current density of the filament quickly removes the excess charges in the local region, and the current density of the filament is limited because an increase of current leads to a decrease of voltage (negative differential resistance). These phenomenons explain also why filaments are often moving during an avalanche.

4.1.5.2 A typical destruction by dynamic avalanche – 3rd degree dynamic avalanche

Third degree avalanche happens at even higher reverse current density. For these levels of current, the charge dynamics change and an Egawa-type field builds up in the diode with a high electrical field at the N-N+ junction while there is still the filament and dynamic avalanche at the P+N- junction. Figure 4.12 sums up the failure mode chronology for dynamic avalanche.

In [39], the third degree avalanche is simulated and the current densities and electric fields from this publication are displayed in figure 4.13. The filament during 2nd degree avalanche is localized between the active region and the termination region due to natural current crowding as illustrated in figure 4.14, simply explained because the anode metal contact area is smaller than cathode metal contact area.

An example of a destruction by dynamic avalanche is displayed in figure 4.15. In figure 4.15a, it can be seen that the voltage across the diode never reaches the breakdown voltage of the diode (1.7kV) but because the reverse current density is very high (due to high di/dt and

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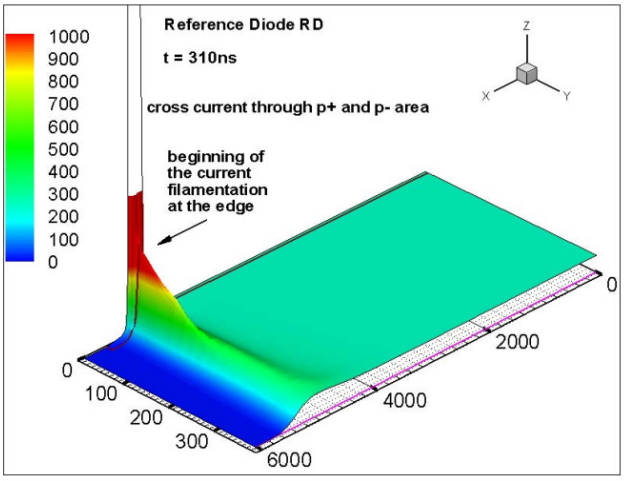
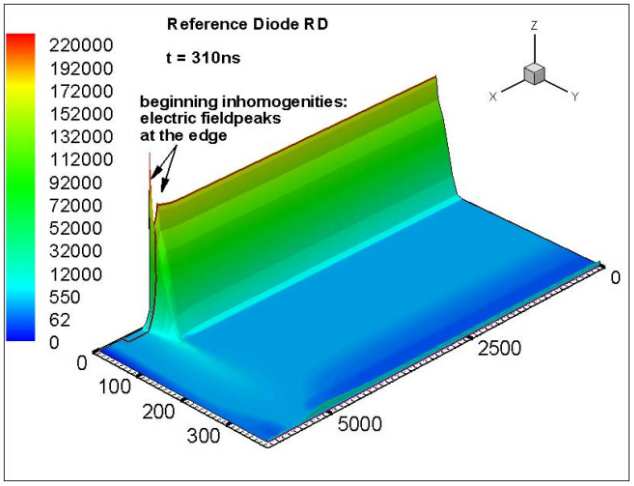
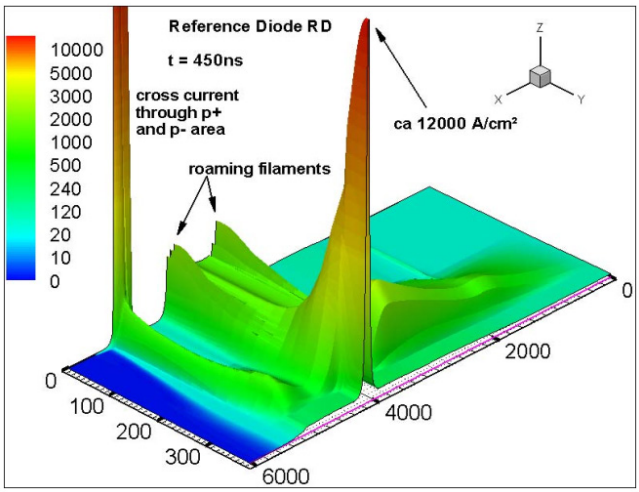


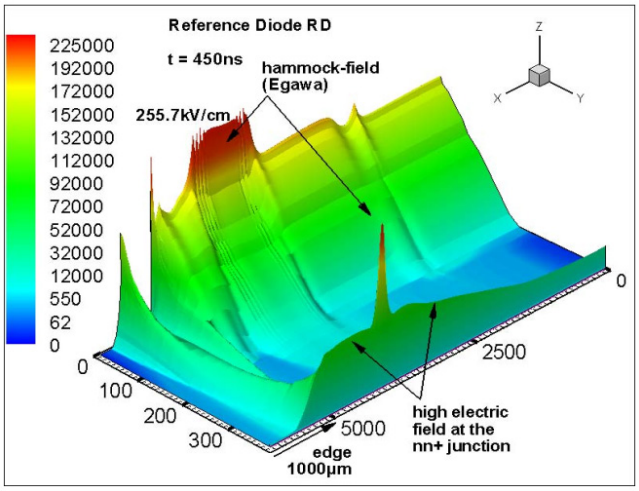
(a) Current density during 2nd degree.



(b) Electric field during 2nd degree.



(c) Current density during 3rd degree.



(d) Electric field during 3rd degree.

Figure 4.13: Current densities and electric field before and during 3rd degree avalanche. Extracted from [39].

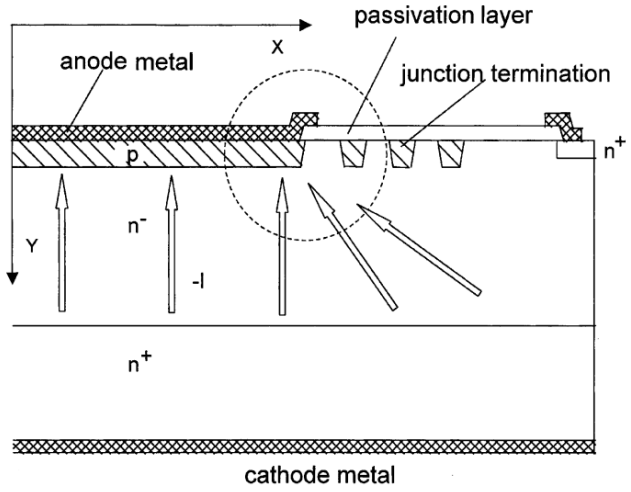


Figure 4.14: Current crowding phenomenon illustration. Extracted from [66].

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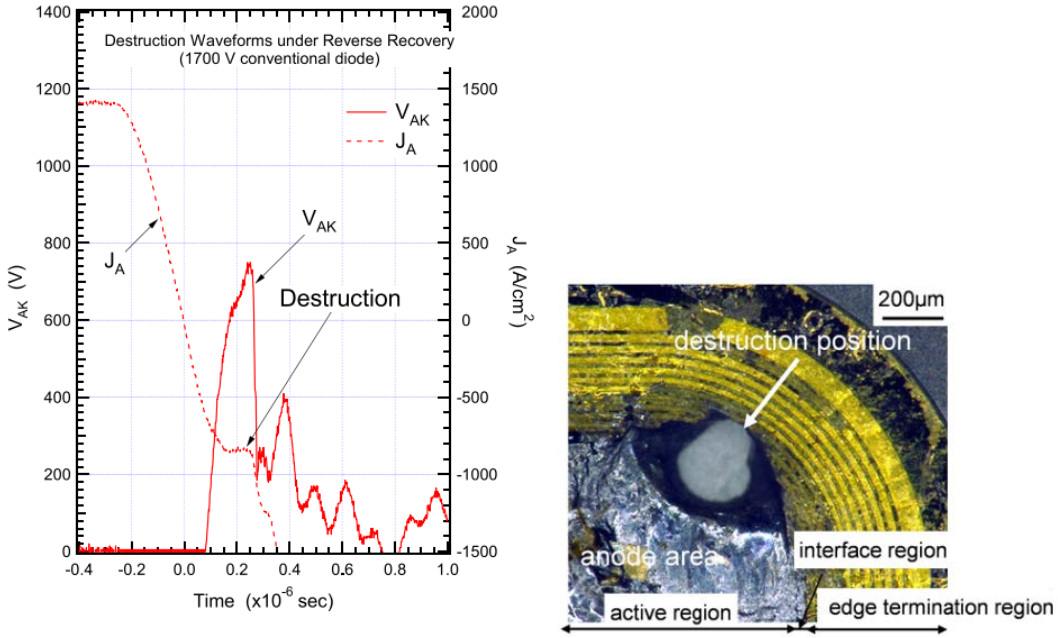

(a) Waveforms. (b) Die anode view.

Figure 4.15: Over-SOA destructive event on 1.7kV a diode, extracted from [82]. Bus voltage $V_{CC} = 1000$ V, current density $J_F = 1400$ A/cm2 ($\times 7.0$ nominal current), current density slope $dJ_F/dt = 7380$ A/cm²µs, $L_S = 2$µH, 398 K.

I_F), 3rd degree avalanche occurs and destroys the diode. It can be seen in figure 4.15b that the diode is destroyed at the interface between the termination and active regions, confirming the hypothesis in the last paragraph.

4.1.6 Conclusion on destructive modes during reverse recovery

The two failures modes described in 4.1.4.3 and 4.1.5.2 are the failures modes that have been found in literature related to reverse recovery. Their comprehension is based on the local phenomenon in the semiconductor (plasma and electric field). They display common points but also crucial differences which explain that their causes are different, i.e. why these phenomena happen for different conditions.

Common points: Both failure modes are ending with a filament due to a destructive avalanche. This deadly filament is caused by an Egawa-type field distribution: the electric field at the N-N+ interface is higher than normal operation. [42] gives an indication on destructive field levels at the interfaces P+N- and N-N+: 350kV/cm for the P+N- (anode) and 100kV/cm for the N-N+ (cathode). The assumption of the destructive electric field at the N-N+ junction of 100kV/cm is also given in [67].

Differences: The first step of the destructive event is different in snap-off destruction and dynamic avalanche destruction: snap-off can be triggered at low di/dt and destructive dynamic avalanche can happen without a particular overvoltage. The other difference is that during

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Table 4.3: Summarised and simplified design trade-offs for PiN diodes.

	P+ doping level	**N+ doping level**	**N- doping level**	**Base Width**	**Lifetime**
Higher blocking voltage when:	-	-	Lower	Larger	
Lower conduction losses when:	Higher	Higher	Higher	Thinner	Higher
Lower switching losses when:	Lower	Lower	-	Thinner	Lower
Less snap-off when:	Lower	Higher	Higher	Larger	Higher on N+ side than P+

dynamic avalanche of 3rd degree a filament is already present before the occurrence of an Egawa-type field, whereas in the snap-off destructive event, the filament only appears after the Egawa-type field distribution takes place.

4.1.7 Design trade-offs on PiN Silicon Diodes

The design of PiN diodes concerning snap-off is only one among many design constraints. The main four characteristics to focus on when designing a diode are: the blocking voltage, the conduction losses, the switching losses and the reverse recovery softness. In table 4.3, the main trade-offs can be found with the following parameters: doping levels in the three regions, the base width and the carrier lifetime. Some direct opposition can be seen (between conduction and switching losses, on doping levels and lifetime for example), and more complex interactions (like between the blocking voltage and the snapiness for example). It can be concluded that: 1) the diode design is a complex trade-off between which characteristic to optimize, 2) the diode design has to be optimized for the final application. To complete the last point, it is better to have a diode with excellent switching characteristics and poor conduction ones in a high frequency converter (and opposite in a low frequency converter) than a medium diode in both characteristics.

4.2 Experiment on IGCT and quick Silicon diode commutation at high di/dt

This section presents the results of the experiment designed in the previous chapter. A summary of the conclusions on the different aspects of the experiment is provided in the last section 4.2.8 to give the reader a complete view in the last part.

This section is organized as follows: first a reminder of the experimental plan, then an overview of the typical waveforms that have been observed, before presenting failure events and results.

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4.2.1 Summary of the experimental plan

Experiment description summary: The experiment is a double pulse, described in chapter 3, to test a commutation cell (IGCT + diode) similar to a submodule (in both ratings, structure and typical values). The capacitance providing the energy for the double pulse is composed of: 2 capacitors in series (equivalent 1.135mF and 5kV) far from the setup and 1 capacitor in parallel to first two, close to the setup (800µF and 3.8kV), giving an equivalent 1.935mF capacitor. The charge inductor has different configurations: 491µH, 782µH, 1.45mH, 2.74mH, and different values will be used all along the tests. The delay between commutations has been chosen to be 40µs (phase C and D in figure 3.2) first, and changed to 200µs after the failure events (described in section 4.2.4). The IGCT used in this experiment is the 6.5kV IGCT described in section 3.2.1.

Goal of the experiment: The identified issue related to the use of IGCTs in MMC submodules in chapter 2, is the presence of the turn-on snubber, slowing down the di/dt to protect the freewheeling diode. Is it possible to remove the snubber using the fastest silicon diodes on the market? If not, by how much the snubber inductance can be reduced? Because the IGCT was never used in SuperGrid Institute or the Ampere Lab, a side goal is to gain experience on this switch.

Different configurations:

- Diodes packs (see section 3.2.1):
  - a 6.5kV PM (plastic-module) diode pack comprised of two diodes sub-packages in parallel inside (total nominal current 2×600A, limit of 4kA/µs per sub-package).
  - a 4.5kV PM diode pack comprised of two diodes sub-packages in parallel inside (total nominal current 2×1200A, limit of 6.5kA/µs per sub-package).
- Snubber inductance (see section 3.2.2):
  - 5 cable inductances (0.8µH, 1.34µH, 1.97µH, 2.9µH, 3.42µH), see subsection.
  - 4 busbar positions, see subsection 3.12.

It should be noted that the press-pack diode that is recommended to use as a freewheeling diode with an IGCT – a 4.5kV PP (press-pack) diode (nominal current 2000A, limit of 1kA/µs) – has been used to check if a diode designed for IGCTs displays snap-off (see subsection 4.2.3.3). In this chapter the 4.5kV PM diode will be called 4.5kV diode.

Different points: The measures have been done for the following points, when it was possible:

- Temperature: ambient, 60°C, 90°C, 120°C for the heatsinks temperature.
- Voltage: 800V, 1100V, 1400V, 1700V, 2000V, 2400V, 2800V, 3300V*, 3600V*. (* = only for the 6.5kV diode)

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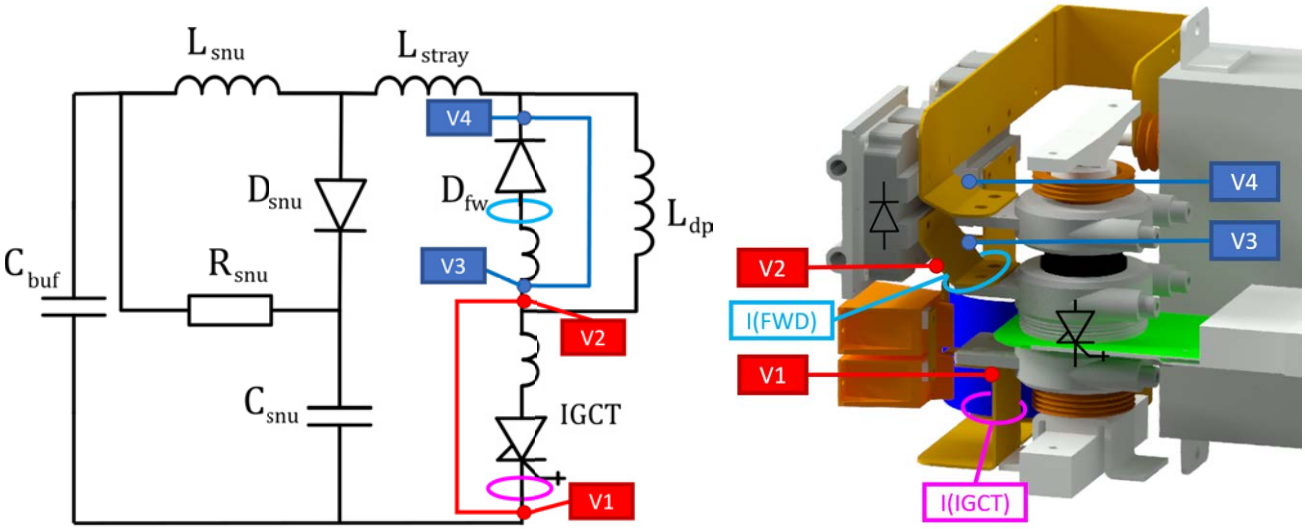

(a) Circuit diagram, SM part.

(b) 3D rendering.

Figure 4.16: Positions of the voltage and current probes in the circuit, precised with a circuit diagram and a 3D rendering of the experiment. V2-V1=V(IGCT); V4-V3=V(FWD).

- Current: 100A, 300A, 600A, 900A, 1200A, 1800A, 2400A.

Due to undesirable phenomenon (like snap-off or dynamic avalanche), not all the measures have been done. Especially, for the 6.5kV diode, some measurements have been abandoned after the diode failure, as explained in section 4.2.4.2.

4.2.2 Overview of typical waveforms

Because the focus of this study is the IGCT turn-on impact on the reverse recovery of the diode, and possibly its destruction, it is important to understand the typical waveforms of this commutation. The position of the probes and a reminder of the circuit diagram of the submodule part of the setup are displayed in figure 4.16. The turn-on waveforms that are displayed and analysed during this chapter and the next one corresponds to t_2 in section 3.1.2. On the other hand, the turn-off waveforms that are displayed and analysed during this chapter and the next one corresponds to t_1 in section 3.1.2.

4.2.2.1 Typical turn-on waveform with no snap-off event

In both sub-figures of figure 4.17, typical pulse waveforms can be found, including the snubber inductor voltage waveform. The typical chronology, described using sub-figure 4.17a for timestamps, is as follows:

A The IGCT receives the turn-on command and its voltage (V_{IGCT}) starts decreasing ($t = 41.2\mu s$). The current through the diode starts to transfer to the IGCT. The voltage across the snubber inductor increases. This first phase stops when the IGCT voltage

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has finished its first decrease and is stable at a low voltage (t =42µs), and the snubber inductor voltage has also finished its increase to a portion of the voltage pulse (that ratio can be approximated by $L_{snu}/(L_{snu} + L_{stray})$, see figure 4.16a).

B Then the current still transfers from the diode to the IGCT at a constant rate, and the snubber inductor voltage is stable. This second phase stops when the diode starts to block voltage ($t = 44$µs; see section 4.1.3 for reverse recovery phases explanation).

C The diode di/dt starts to increase (but is still negative, $t = 44$µs), the voltage across the diode increases and the snubber inductor voltage decreases. Then the reverse recovery current reaches its minimum (I_{rr}), the current through the IGCT reaches its maximum and di/dt=0 at $t = 44.8$µs.

D From $t = 44.8$µs to $t = 45.2$µs, the di/dt through the diode is now positive and is still increasing. This phase is over when the voltage across the diode reaches a first maximum, which corresponds to the overvoltage due to the stray inductance.

E Starting from $t = 45.2$µs, a slow recovery takes place: the di/dt through the diode slowly decreases until the recovery is over ($t = 50$µs)

F The last phase is the slow discharge of the snubber inductor, which is the cause of the last bump of the diode voltage waveform.

4.2.2.2 Typical turn-on waveform with snap-off event

In both sub-figures of figure 4.18 are displayed typical waveforms with snap-off, one with the 6.5kV diode (figure 4.18a) and the other with the 4.5kV diode (figure 4.18b). The snap-off event will be studied further in section 4.2.3, but it can already be noted that the overvoltages observed on both pulses are far from negligible (2.5kV for the 6.5kV diode pulse and 1.5kV for the 4.5kV diode pulse).

4.2.2.3 Typical turn-off waveform

Typical waveforms at IGCT turn-off are displayed in figure 4.19. What can be observed on the IGCT waveforms is that the current through the IGCT is first decreasing quickly and then at a way slower rate. These two phenomena are due to the semiconductor itself. The shape of the IGCT voltage waveform, with the local minima (0.6-0.7µs after the maximum voltage of the IGCT) is explained by the presence of the snubber in the circuit. The diode negative peak is due to the forward recovery of the diode. This phenomenon happens during the diode transient between blocking and conducting when the base region temporarily has a higher resistance than conducting steady-state mode [8].

During turn-off with snubber, the simple chronology, described using sub-figure 4.19b for timestamps, is the following:

A The IGCT receives the turn-off command, its voltage (V_{IGCT}) starts increasing (t = 83.7µs) and the voltage across the diode starts to decrease, until it reaches 0 at $t = 84.2$µs.

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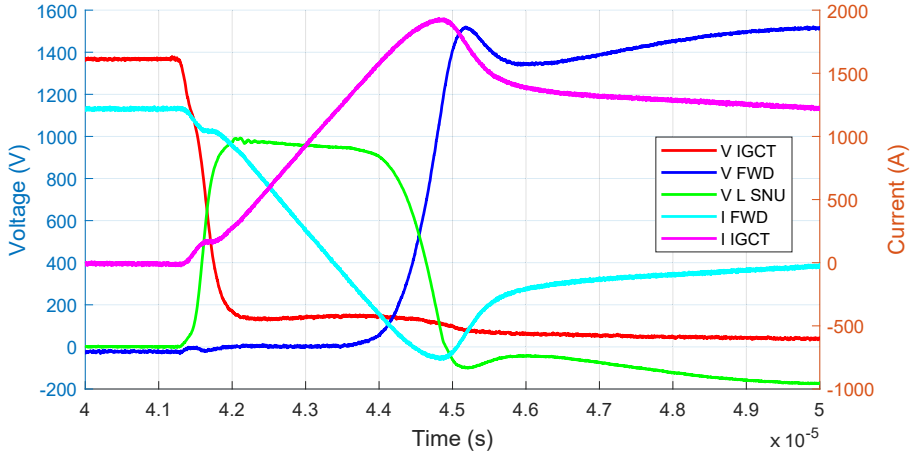
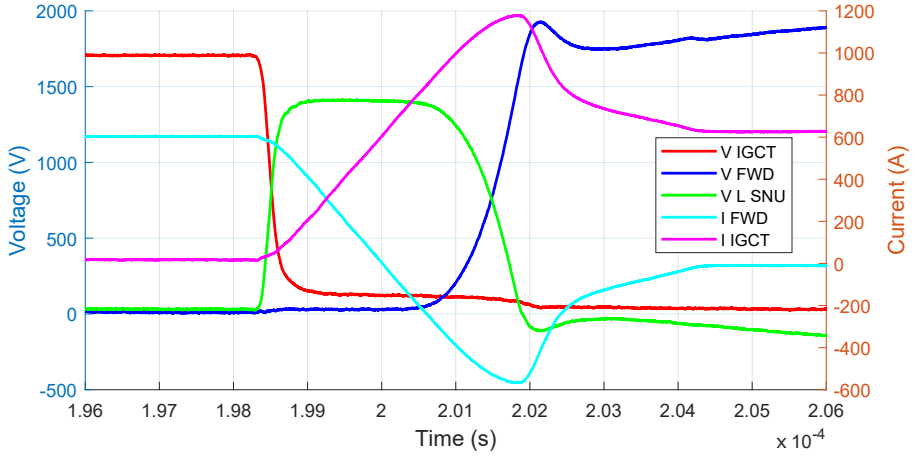


(a) 6.5kV diode, 1400V, 1200A, 1.34µH snubber inductor, 90°C.



(b) 4.5kV diode, 1700V, 600A, 3.4µH snubber inductor, 120°C.

Figure 4.17: Typical waveforms at IGCT turn-on, without snap-off event, with snubber inductor voltage waveform (V L SNU).

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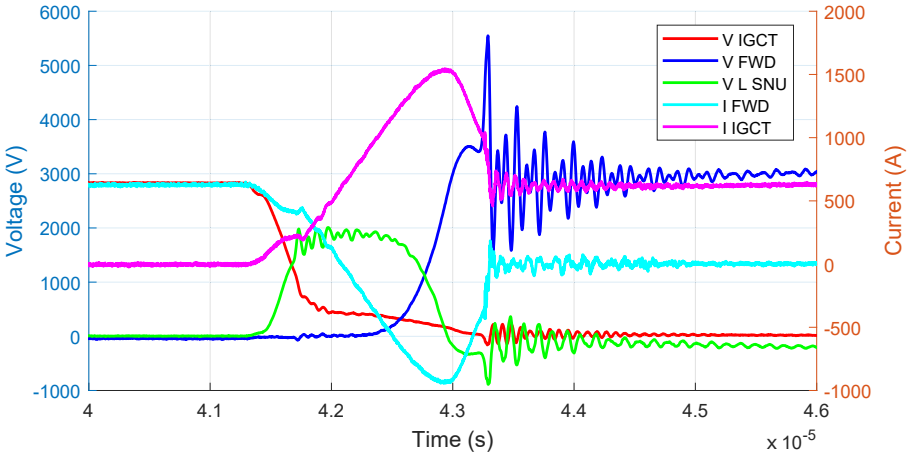
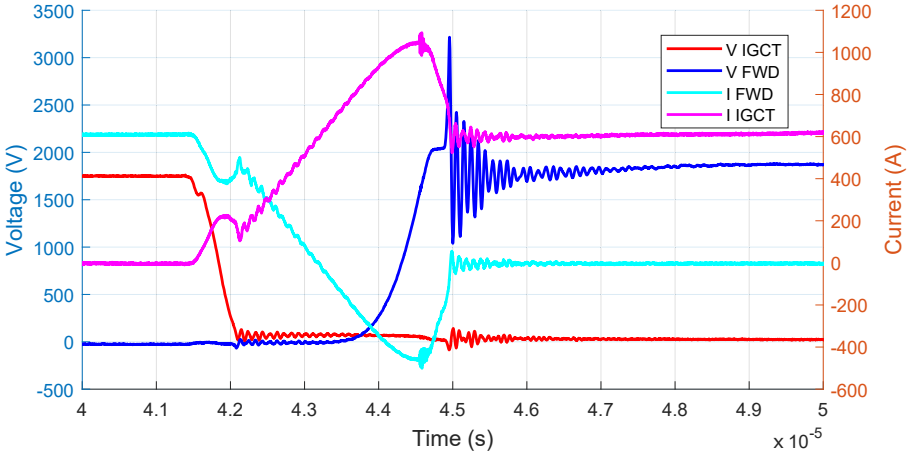


(a) 6.5kV diode, 2800V, 600A, 2.9µH snubber inductor, ambient temperature, with snubber inductor voltage waveform (V L SNU).



(b) 4.5kV diode, 1700V, 600A, 2.9µH snubber inductor, ambient temperature.

Figure 4.18: Typical waveforms at IGCT turn-on, with snap-off event.

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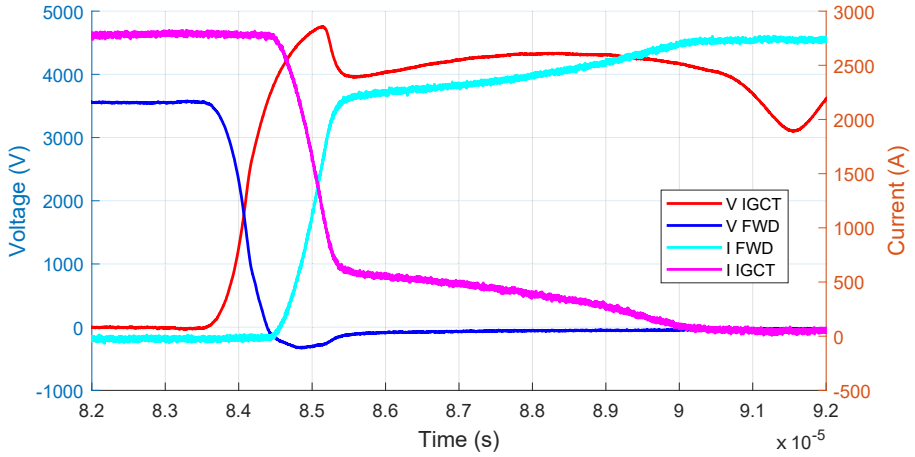
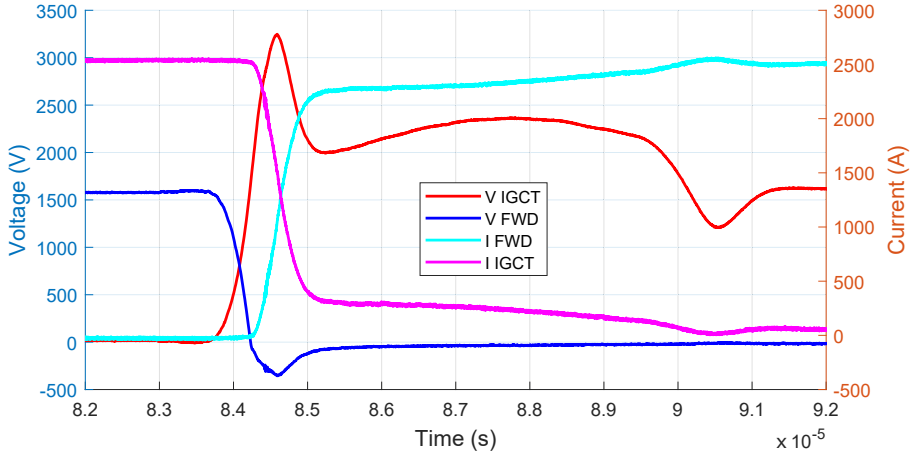


(a) 6.5kV diode, 3600V, 2700A, 0.8µH snubber inductor, ambient temperature.



(b) 4.5kV diode, 1700V, 2500A, 0.8µH snubber inductor, ambient temperature.

Figure 4.19: Typical waveforms at IGCT turn-off.

B The current through the diode begins its increase starting that moment ($t = 84.2$µs), and the current through the IGCT starts to decrease. The forward recovery described previously takes place between $t = 84.2$µs and $t = 85$µs and the IGCT voltage reaches its peak in the middle of that phase.

C At $t = 85$µs, the di/dt of the diode and the IGCT slows down and keeps a low value until the commutation stops, when the IGCT does not conduct any more current, after $t = 92$µs. The voltage bump during that period on the IGCT waveform is due to the snubber.

4.2.2.4 Focus on snubber waveforms at IGCT turn-on

Typical waveforms for the snubber part of the circuit are displayed in figure 4.20. It can be observed that the snubber diode experiences at the same time non-neglictable reverse recovery and snap-off, leading to the current bumps at the beginning of the commutation on the current waveforms of the freewheeling diode and the IGCT, and oscillations on most of the waveforms. The snubber diode is always experiencing very low forward currents (a few tens of

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amps maximum), increasing the possibility of snap-off (see figure 4.8). The snappy recovery of the snubber diode has been studied in [140]. In our case, the choice of the snubber diode has not been optimized in the test bench (the same diode as the freewheeling diode has been chosen for practical reasons) and these perturbations could have been avoided by choosing a more suitable diode. They could also be avoided by increasing the delay between turn-off and turn-on (here 40µs) to have a fully discharged snubber inductance.

During turn-on, the simple chronology of the snubber waveforms, is the following:

A The snubber inductor blocks most of the voltage between the IGCT turn-on command and the start of the voltage blocking of the diode, near the end of the reverse recovery. During that phase (between t =42µs and t = 44.2µs), the current slope of the circuit follows the equation $di/dt = U_{L-SNU}/L_{snu}$.

B After t =45.2µs, the diode blocks entirely the voltage, and the RCD-clamp plays its role of discharging the snubber inductor, up until t =60µs.

4.2.3 Operational parameters influence on the snap-off phenomenon

During the experimental campaign, snap-off was found to occur more often than initially expected. As a consequence, this phenomenon will be the focus of attention.

A crucial point in the upcoming subsections is to detect when a snap-off event happens. Different boolean criteria could be used: the sudden return of the current to zero (high di/dt at the end of the recovery, or zero reached within a certain time), the overvoltage analysis (frequency analysis or number of peaks), or a change in the di/dt slope. In this thesis, it has been decided to identify the snap-off with the sudden return to zero criterion, by detecting a high level of di/dt.

4.2.3.1 Current, Voltage and temperature

"Heatmaps" analysing the snap-off overvoltage are shown in figure 4.21 as a function of I_F, V_{bus} and the temperature. The scale of these heatmaps is between 500 and 1000V of overvoltage to emphasize the limit when snap-off can be considered significant. It can be analysed that, in accordance with the theory (see section 4.1.4), snap-off is more important at low current, high voltage and low temperature. What it can be concluded too, is that this diode, in that particular configuration (with an IGCT and with this stray inductance) seems unsuitable for MMC submodules. Indeed, this 4.5kV diode suffers from too significant overvoltages (greater than 1000V) starting 1700V (compared to 2800V, nominal voltage), at a current as high as 600A (1/4 of the current rating and typical current that is encountered during normal MMC operation). Similar tendency is observable with the 6.5kV diode. Even if the MMC operational temperature is around 80-90°C, the start of the MMC would pose a critical problem. These diodes would be usable in an MMC if snap-off is reduced, and a study on the stray inductance influence on snap-off is conducted in the next subsection.

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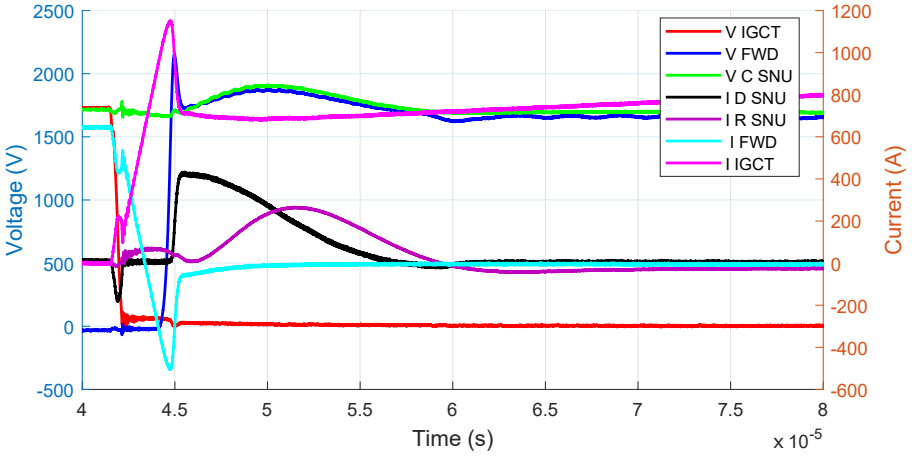
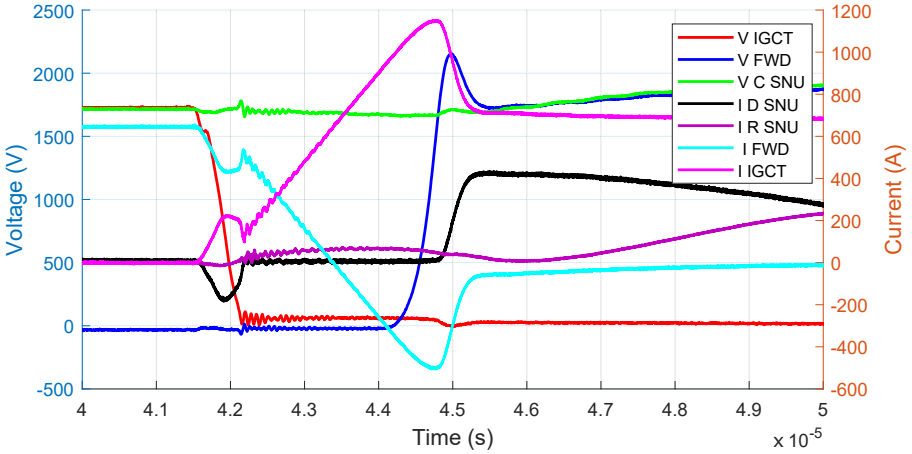
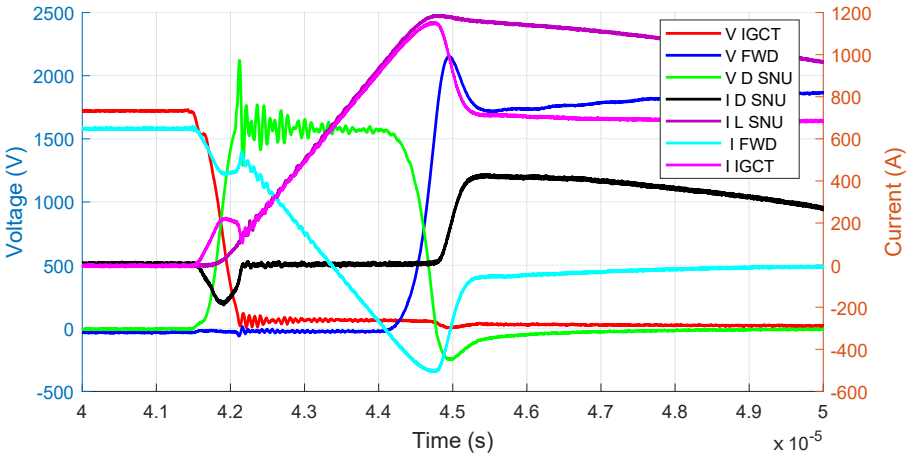


(a) With snubber capacitor voltage (V C SNU), snubber diode current (I D SNU), snubber resistor current (I R SNU) waveforms, time scale: t=40µs to t=80µs.



(b) With snubber capacitor voltage (V C SNU), snubber diode current (I D SNU), snubber resistor current (I R SNU) waveforms, time scale: t=40µs to t=50µs.



(c) With snubber diode voltage (V D SNU), snubber diode current (I D SNU), snubber inductor current (I L SNU) waveforms, time scale: t=40µs to t=50µs.

Figure 4.20: 1700V, 600A pulse, ambient temperature, 3.4µH snubber inductor, including snubber circuit parts waveforms.

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These levels of overvoltages have limited the current/voltage range of the possible pulses to avoid potential destruction by snap-off, as happened in section 4.2.4.1. For a specific snubber inductance and specific temperature, the tests were limited to pulses with snap-off overvoltages lower than 1kV outside of this particular study, in this subsection.

4.2.3.2 Clamped and unclamped/stray inductance influence, with snubber

In the literature, diode snappiness is studied as a function of stray inductance. Here, the inductance in the circuit is comprised of two elements: a "clamped" inductor (that of the snubber circuit, with its associated dissipative circuit, L_{snu} in figure 4.16a) and the stray inductance of the interconnects (busbars, packages... L_{stray} in figure 4.16a).

Therefore, a legitimate question is: it is known that stray inductance has an effect on snappiness of the diode, but does clamped inductance has one? To answer that question, the experiment has been simply modified. The lower busbar, shown in figure 4.22 has been replaced by a cable. Three situations have been studied:

A 1.3µH clamped inductor + busbar. L_{snu}=1.3µH; L_{stray}=$L_{stray-bb}$.

B 0.8µH clamped inductor + cable. L_{snu}=0.8µH; L_{stray}=$L_{stray-cab}$.

C 0.8µH clamped inductor + busbar. L_{snu}=0.8µH; L_{stray}=$L_{stray-bb}$.

The 50cm long cable was estimated adding around 500nH. This value makes the whole inductance of the loop, the one slowing down the IGCT turn-on, similar. The results of tests with the setup in these configurations are shown in figure 4.23. The selected diode for these measures is the 6.5 kV diode.

From the results displayed in figure 4.23a, it can be seen that for the two first situations (situations n°1 and n°2 described above), the total loop inductance (unclamped + clamped, $L_{snu} + L_{stray}$) is similar. Indeed, for similar V_{bus} values, di/dt at 0A is almost the same. The entire inductive loop is estimated at around 1.8µH. On the other hand, situation n°3 has an estimated total loop inductance of 1.3µH. This is coherent compared to situation n°1, where the clamped inductances are 500nH different and the stray inductances are the same ($L_{stray-bb}$). This makes the estimated added stray inductance of 500nH in situation n°2 coherent too by comparing the total loop inductances in situations n°2 and 3 (difference 500nH), while the clamped inductor is the same (L_{snu}=800nH).

But despite having the same total loop inductance, the overvoltage due to the snap-off between situations n°1 and n°2 for the same di/dt at snap event is very different, as it can be seen in figure 4.23b. For a given di/dt at snap-event, the situation with a bigger stray inductance is worse: the overvoltage is bigger. While for the same stray inductance and different clamped inductors (situations n°1 and n°3), the overvoltage due to the snap-off is very similar.

The equivalent obtained stray inductances are 300-350nH for $L_{stray-bb}$ and 700nH for $L_{stray-cab}$, calculated with $L = \Delta U/(di/dt)$. The difference between the two stray inductances is 350-400nH, which is coherent with the added stray inductance by the 50cm long cable (with an estimated 500nH inductance).

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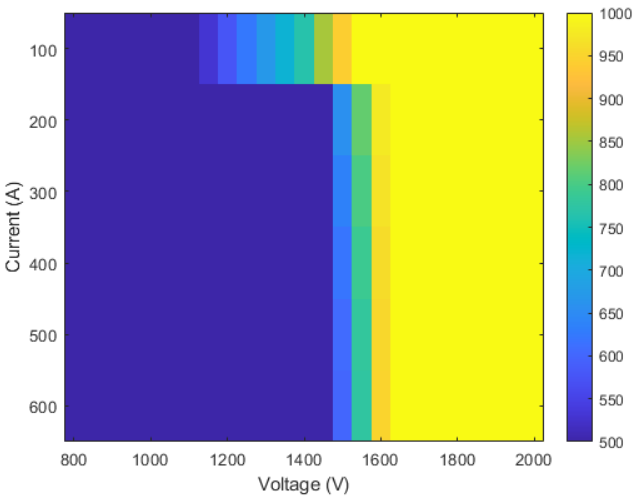
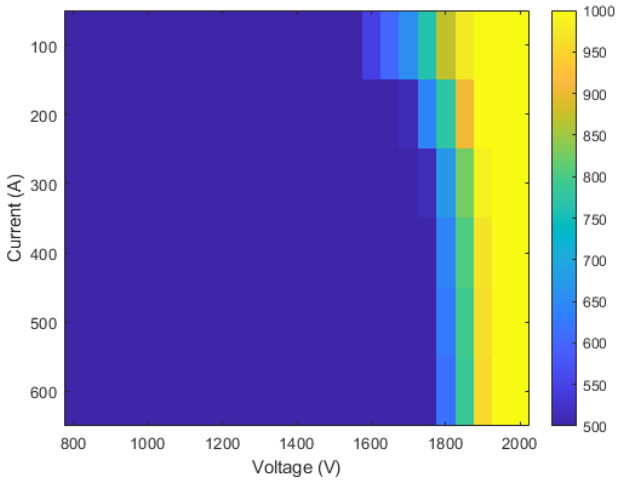
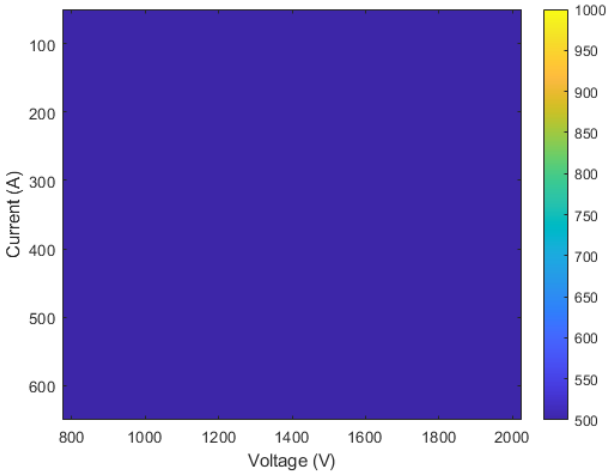


(a) Ambient temp. (25°C).



(b) 60°C.



(c) 120°C.

Figure 4.21: Heatmaps illustrating the influence of voltage, current and temperature on snap-off event. diode used here: 4.5kV diode. L_{snu}=3.4µH.

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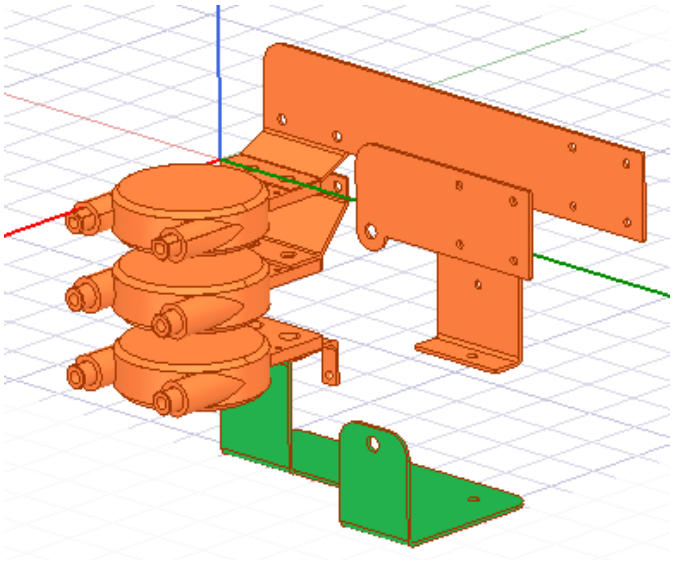
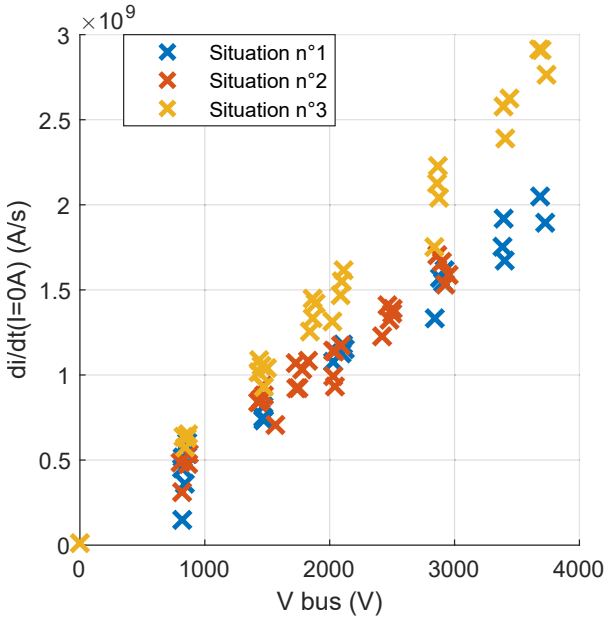
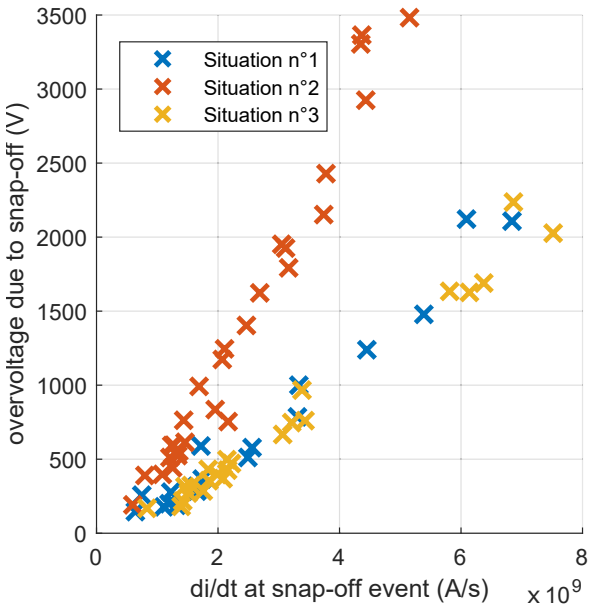


Figure 4.22: Busbar replaced by a cable in the clamped/unclamped inductance study on diode snap-off.



(a) di/dt at 0A function of V_{bus}



(b) Overvoltage due to snap-off function of di/dt at snap-off.

Figure 4.23: Results of the study clamped/unclamped inductance influence on snap-off overvoltage. Currents from 100A to 2400A are displayed.

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These results show that the snubber inductor value has little if no effect on snap-off. But the stray inductance has at least a much more significant impact on snap-off overvoltage. It is preferable to reduce it as much as possible by connecting the snubber RCD clamp as close as possible to the IGCT and diode.

4.2.3.3 Snap-off of the recommended diode with IGCT

A few pulses have been done installing the diode 5SDF 20L4520 (ABB, see table 3.2) instead of the spacer and removing the PM diode D_{fw} (see figure 3.5a). This diode has been recommended for the use of IGCTs. The pulses were performed from 800V to 2000V and from 300A to 1800A, at 25°C and 80°C. The goal is to verify if snap-off behaviour is present with this diode at these levels of voltage/current (which is the case for the PM 4.5kV in the subsection 4.2.3.1). The result is that it does not present any snap-off (even a low intensity snap-off) at these levels, at any temperature. This points that the PM 4.5kV and 6.5kV diodes might not be adapted to work with IGCT, in this configuration (with its associated snubber and stray inductance).

4.2.4 Destructive events

Two destructive events occurred during the tests. One was directly related to the snap-off event, the other to a dynamic avalanche because of a too high di/dt, I_F, and V_{max} combined. In this section, we focus on these destructive events, with waveforms and close-up photographs.

4.2.4.1 Snap-off related destruction

This destructive event took place with the 4.5kV diode. Figure 4.24 shows the waveforms and the destroyed dies. A snap-off event took place and a maximum voltage over 4.5kV (see figure 4.24a and 4.24b) has led to destructive filaments in 3 dies next to each other (see figure 4.24c). The di/dt during snap-off reaches 12kA/µs, which gives an equivalent stray inductance of 280nH, considering an overvoltage of 3.4kV, which is coherent with the order of magnitude of the estimated stray inductance of the circuit (450nH). The difference between the two values could be explained by potential saturation of the overvoltage. Indeed voltage exceeded the breakdown voltage, which might modify the rule $u = L.di/dt$. It should be noted, though, that no typical avalanche saturation of voltage is observed. A simpler explanation would be measurements inaccuracies or simulated stray inductance values being off at this level of frequency.

The current was low compared to the current rating (600A among the two parallel diodes, a fourth of the nominal current rating being 2×1200A), and the temperature of the diode was the ambient temperature. These factors, as described in section 4.1.4.2, makes the snap-off more intense in terms of overvoltage. The di/dt at I_F=0 is lower than the limit: 1.7kA/µs for the two diodes in parallel, which is lower than the limit of only one diode (6kA/µs per diode).

The dies that have exploded were part of the diode side with the highest inductance path. The fact they failed can be related to a local lower current and therefore a higher local overvoltage due to the snap-off (or a higher electric field at the N-N+ junction), or to a local higher overvoltage due to the higher inductance path. It could also be a combination of both.

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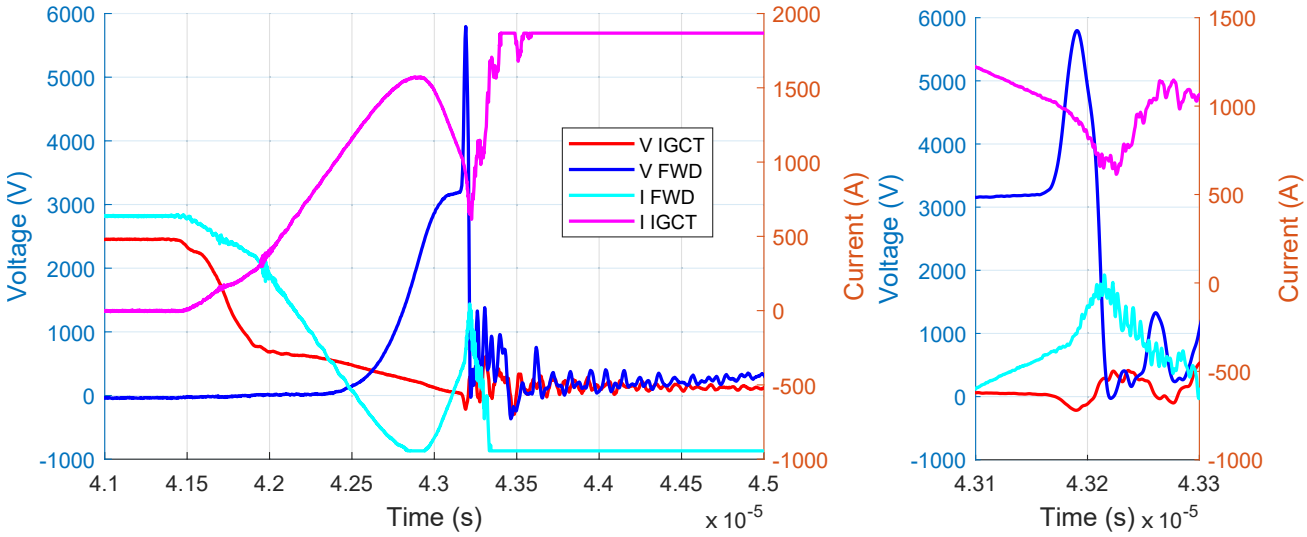
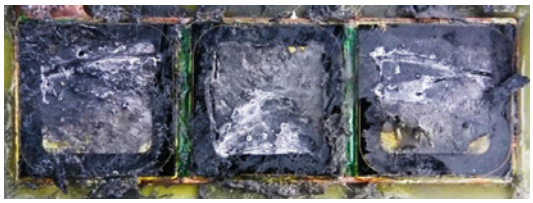


(a) Waveforms of failure event due to snap-off.

(b) Zoom on snap-off.



(c) Dies.

Figure 4.24: Failure event due to snap-off. 2400V, 600A, di/dt of 1.7kA/µs, 25°C. used diode for the pulse: the 4.5kV.

Because the filaments seemed that they have moved during the failure (they form lines rather than spots), it is difficult to relate the position of the most impacted areas to a specific phenomenon, unlike in [82] and section 4.1.4.3.

As said in subsection 4.2.3.1, pulses leading to more than 1kV overvoltage due to snap-off have been avoided after this failure event.

4.2.4.2 Dynamic avalanche related destruction

This second failure event, that can be found in figure 4.25, happened with the 6.5kV diode. The di/dt, while not being higher than the maximum (4.5kA/µs for the two diodes in parallel compared to the limit of 2×4kA/µs), was still high, and combined with twice the nominal current (2400A), a high stray inductance (approx. 450nH compared to 280nH for the SOA test conditions in the datasheet) and a decent voltage level (3300V), it apparently lead to a dynamic avalanche failure. Unlike the last subsection, the voltage did not go higher than the breakdown voltage 6.5kV (see figure 4.25a), which emphasises the dynamic avalanche hypothesis.

The dies that visibly failed were close to each other and on the least inductance path. They might have experienced a higher di/dt and I_F which would have lead to a higher dynamic avalanche phenomenon. It can be seen in figure 4.25b, like in the previous subsection, that the filaments have moved during the failure. They seemed to have followed the bonding wires

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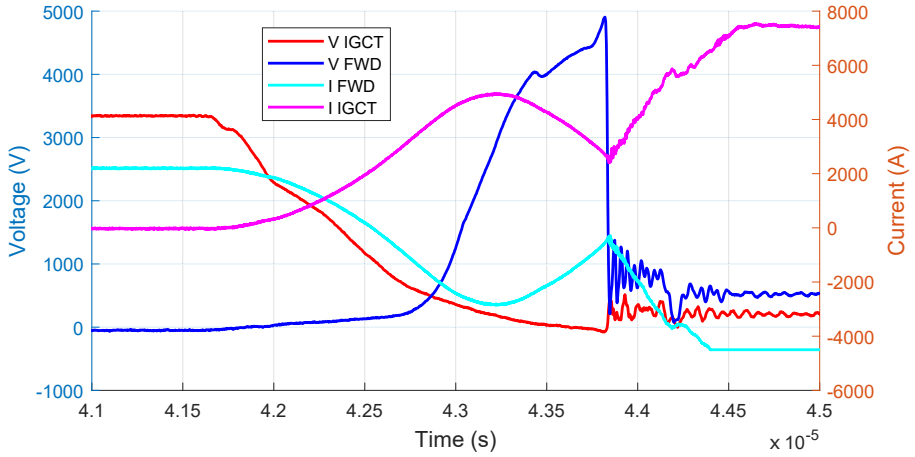
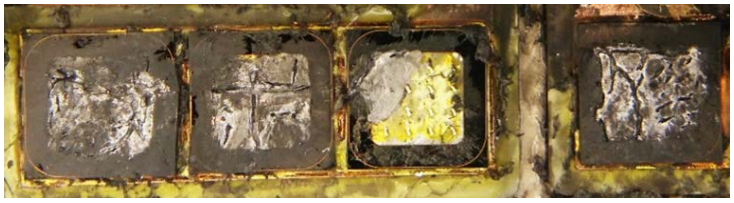


(a) Waveforms of failure event due to overlimit pulse.



(b) Dies.

Figure 4.25: Failure event due to over-limit pulse. 3300V, 2200A, di/dt of 4.5kA/µs, 25°C. used diode for the pulse: the 6.5kV.

positions, which appears to be logical. Indeed, there is a current crowding around the wire bondings, which is an important factor on where the dynamic avalanche starts in the P+N- junction (see section 4.1.5.2). It also seems that there has been damage at the peripherical protection but it is complicated to determine at which step of the failure the peripherical protection were destroyed. The theory says that it could be at the beginning of the failure, but there is no decisive evidence on where exactly the filaments started.

This failure pointed out that the 6.5kV diode might not be a suitable candidate for snubberless operation. To prevent any risk, this diode has not been tested in a snubberless configuration (no snubber inductor and no RCD clamp), unlike the 4.5kV diode (see subsection 4.2.6).

4.2.5 Operational parameters influence on the reverse recovery

With the entire set of experimental points, it is possible to study the influence of operational parameters on reverse recovery characteristics. These two following subsections will focus on the effects of the temperature and of the snubber inductor value. Each measure point in the figures in this section are obtained after the analysis of the pulses with Matlab scripts. The measures scripts follow the JEDEC standard for the measures of the reverse recovery.

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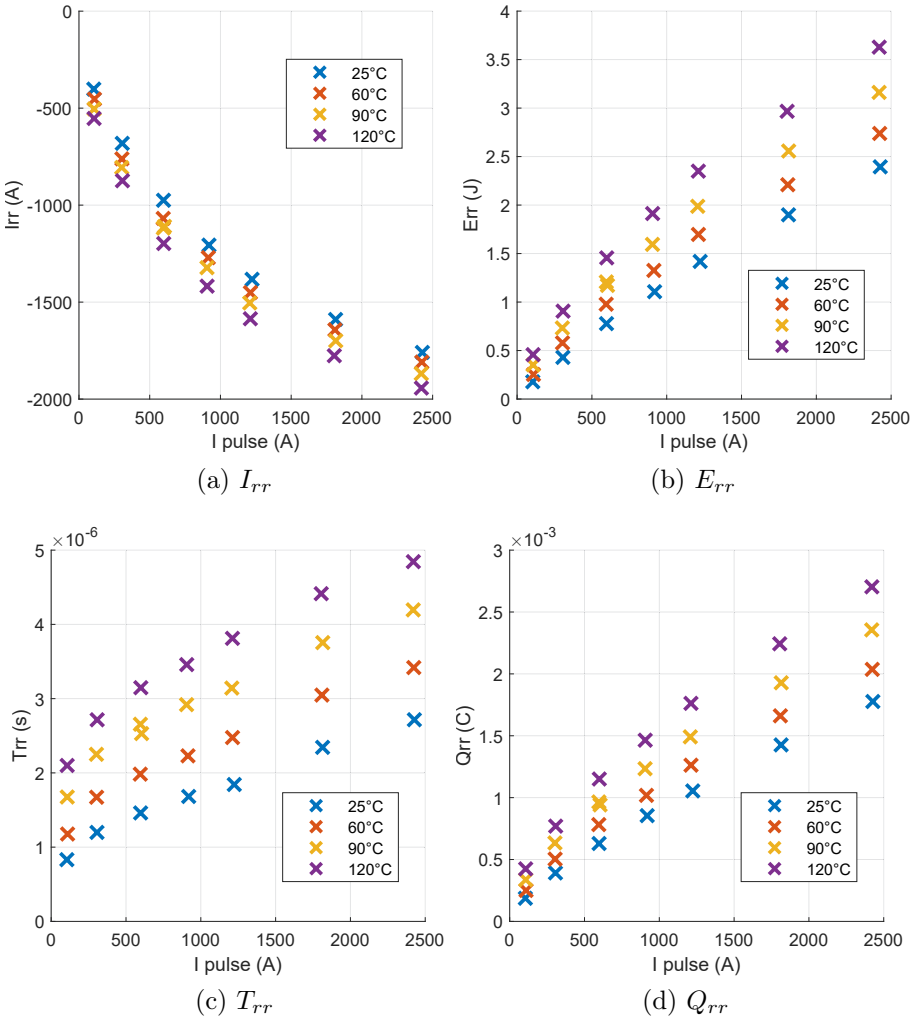

(a) I_{rr} (b) E_{rr}

(c) T_{rr} (d) Q_{rr}

Figure 4.26: Reverse recovery parameters for the 4.5kV diode, V_{bus}=1700V, snubber inductor: busbar position 4 (100nH est.). Temperature variation with values: 25°C, 60°C, 90°C, 120°C.

4.2.5.1 Temperature effect

The values of the various reverse recovery parameters for the 4.5kV diode operating at different temperatures are displayed in figure 4.26. It can be seen that increasing the temperature increases the absolute value of I_{rr}, E_{rr}, T_{rr} and Q_{rr}. This is the expected behaviour: a higher temperature leads to a higher quantity of charges, as described in subsection 4.1.3.4. For 1.7kV, 2.4kA and a very low snubber inductance (busbar position 4 around 100nH), the values of the reverse recovery are:

- For I_{rr}, 1940A at 120°C and 1760A at 25°C (180A difference).
- For E_{rr}, 3.6J at 120°C and 2.4J at 25°C (1.2J difference).
- For T_{rr}, 4.8µs at 120°C and 2.7µs at 25°C (2.1µs difference).
- For Q_{rr}, 2.7mC at 120°C and 1.8mC at 25°C (0.9mC difference).

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4.2.5.2 Snubber inductor value influence

The values of the same parameters, still for the 4.5kV diode but this considering different snubber inductors are displayed in figure 4.27. Points for position 4 at 2100A and 2400A have not been done, to ensure safe operation. It can be seen that reducing the snubber inductance value increases the speed of the commutation (lower T_{rr}) but with a slightly higher Q_{rr}. It also leads to a higher absolute value of I_{rr} and E_{rr}. This is the impact (of lowering the snubber inductance) on reverse recovery which was expected, because it leads to a higher di/dt during commutation. For 2.4kV, 1.8kA and 120°C, the values of the reverse recovery are:

- For I_{rr}, 2350A for Pos.4 and 950A for 3.4µH (1400A difference).
- For E_{rr}, 4.8J for Pos.4 and 2.8J for 3.4µH (2J difference).
- For T_{rr}, 2.8µs for Pos.4 and 3.7µs for 3.4µH (-0.9µs difference).
- For Q_{rr}, 2.6mC for Pos.4 and 2mC for 3.4µH (0.6mC difference).

4.2.6 Operation without RCD clamp

Operation with the lowest snubber inductance value (busbar position 4 around 100nH) was possible with the 4.5kV diode, but not with the 6.5kV, that exploded with the busbar in position 1. The step after has been to remove the capacitor, resistor and diode, and test in the same conditions, with the busbar at position 4. As presumed, overvoltage is higher in the case of removal of the RCD clamp, because removing the RCD increased the unclamped inductance. The resulting overvoltages are displayed in figure 4.28 at 120°C. Pulses were done, and measure points were obtained for lower temperatures (25°C, 60°C, and 90°C) but on smaller voltage/current ranges due to snap-off limitations.

Waveforms of IGCT turn-on in the two different cases (with or without RCD) are displayed in figure 4.29 for 2400V and 1800A and in figure 4.30 for 2400V and 200A. Waveforms of IGCT turn-off in the two different cases (with or without RCD) are displayed in figure 4.31. It can be seen like previously that overvoltage is higher at turn-on (but also turn-off) for the case without RCD clamp, but also that snap-off is more intense for the case without RCD. This can be explained by the fact that the unclamped stray inductance has been augmented by removing the RCD clamp. On the turn-off waveforms, it can be seen that the local minimum around t=3.5µs is effectively due to the RCD part of the snubber, like presentend in 4.2.2.2.

The maximum reached di/dt at 0A in this configuration is 3.15kA/µs, which is far from the limit of the 4.5kV diode (2×6.5kA/µs), indicating that a further decrease of the inductance without threatening the diode is possible. It should be noted that the maximum di/dt does not correspond to L_{stray}/V_{bus} (L_{stray} for that specific pulse, V_{bus}=2400V), which gives 5.3kA/µs. This can be explained by the fact that the inductance of the circuit does not support 2400V when I_{FWD}=0, because the IGCT still supports 750V. This phenomenon (the voltage across the IGCT not dropping is even more present with the SiC diode) is presented in section 5.3.3

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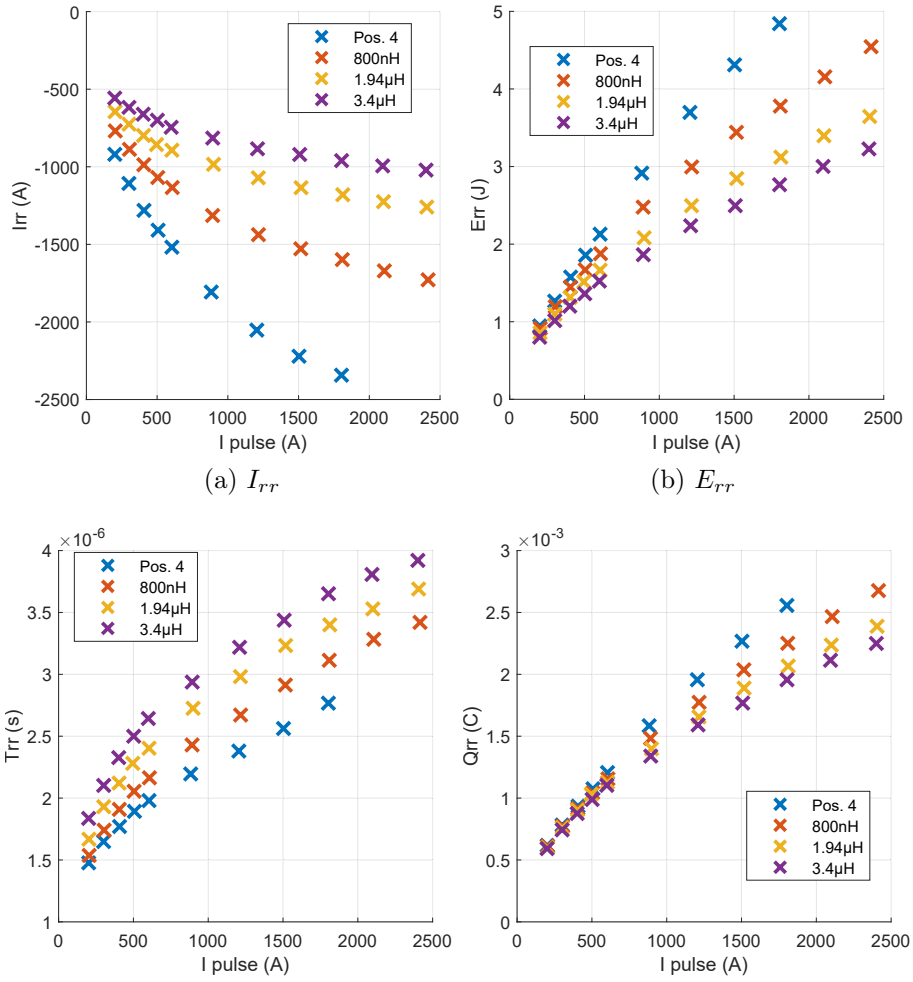

(a) I_{rr} (b) E_{rr}

(c) T_{rr} (d) Q_{rr}

Figure 4.27: Reverse recovery parameters for the 4.5kV diode, V_{bus}=2400V, temperature: 120°C. Snubber inductance variation with values: 3.4µH, 1.9µH, 0.8µH, and busbar position 4 (estimated 100nH).

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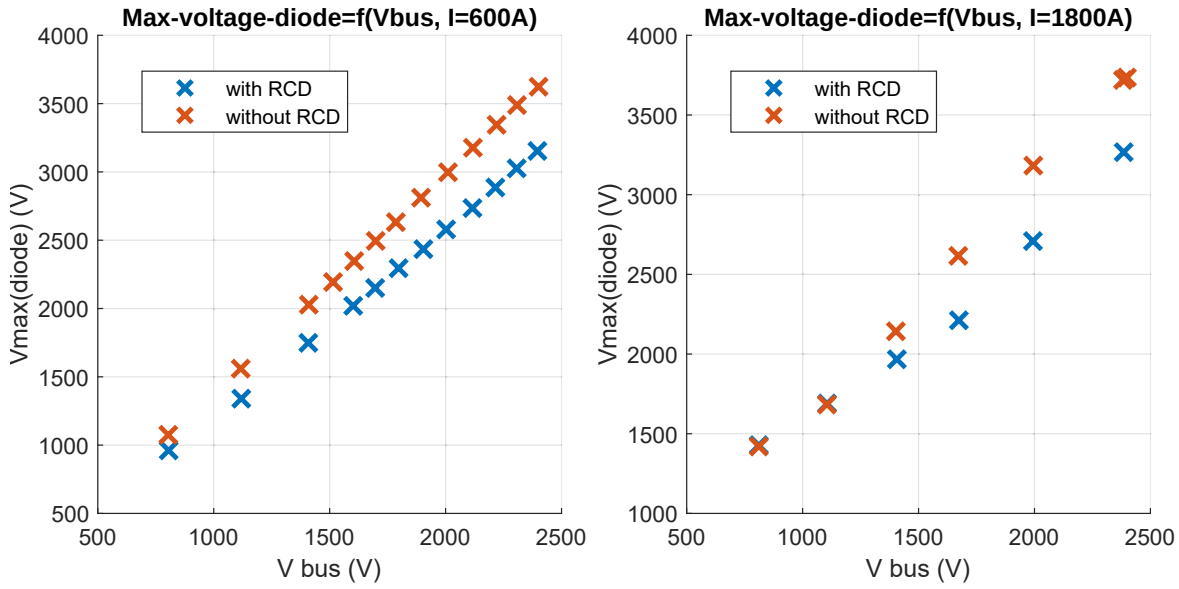

(a) Case I=600A. (b) Case I=1800A.

Figure 4.28: Comparison of overvoltages in the case with RCD (blue) and without RCD (orange), V = 2400V, temperature = 120°C.

4.2.7 Snubber reduction impact on losses

In this subsection, the impact of reducing and removing the snubber on the losses is studied. The total losses during turn-on are displayed in figure 4.32a, for 120°C, the 4.5kV diode and 2000V. This total losses is the sum of the reverse recovery losses, the snubber energy and the IGCT turn-on losses. The snubber losses has been calculated as $E_{snu} = 1/2.L.I^2_{pulse}$. The turn-on losses of the IGCT are calculated between 90% and 10% of the voltage pulse.

The losses are highly reduced when the snubber is reduced. The snubberless configuration in green, compared to the position 4 with RCD clamp in purple, exhibits more losses, but it is still less losses than the 0.8µH snubber inductor configuration.

The distribution of the losses among the different parts is displayed in figure 4.32b. The IGCT turn-on losses are coherent with the values of the datasheet (2J at 4000V and 3800A) and therefore they represent the smallest contribution to the losses. At higher current, the snubber becomes an increasingly important contribution of the losses, which would explain why the total losses diminish when the snubber inductance is reduced.

4.2.8 Conclusion on the experiment with fast silicon diodes

As a reminder, the experiment aims to study the reduction and removal of the snubber. An unexpected behaviour of the diode is the late snap-off, leading to destructive overvoltages. The conclusions drawn in this experimental section are grouped and summarised here.

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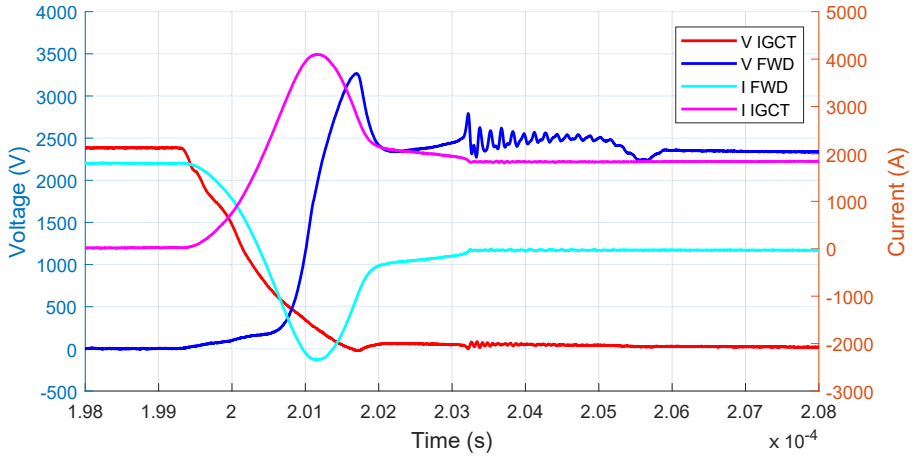
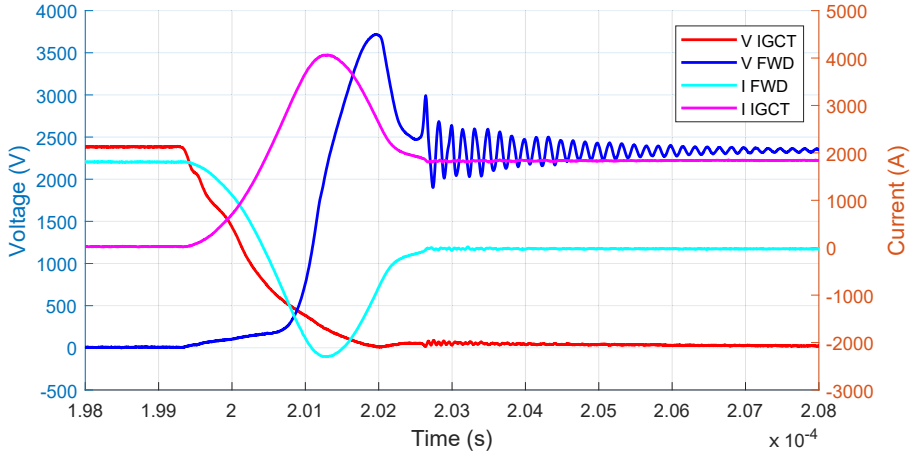


(a) With RCD.



(b) Without RCD.

Figure 4.29: Waveforms of the case with and without RCD clamp. 2400V, 1800A, 120°C, 4.5kV diode, busbar position n°4.

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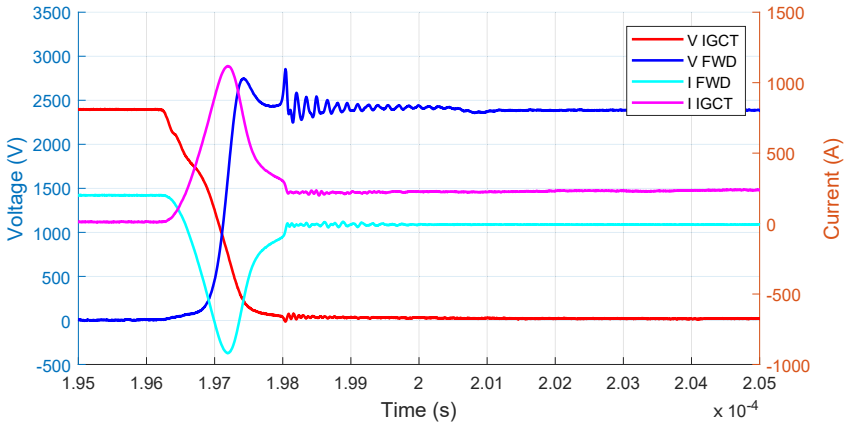
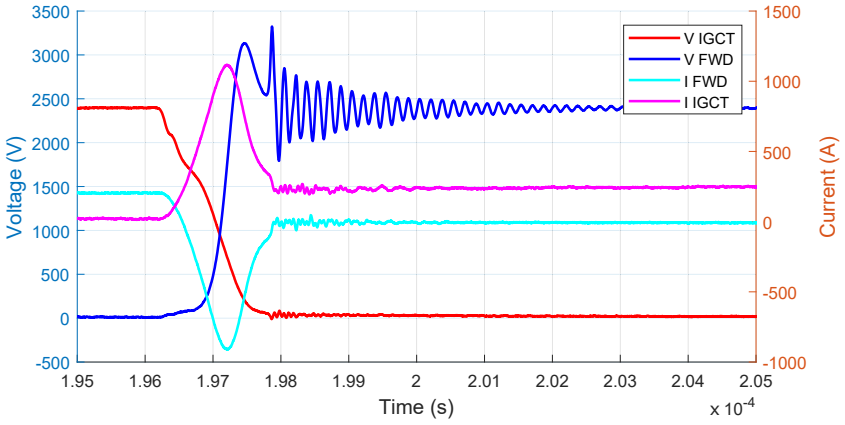


(a) With RCD.



(b) Without RCD.

Figure 4.30: Waveforms of the case with and without RCD clamp. 2400V, 200A, 120°C, 4.5kV diode, busbar position n°4.

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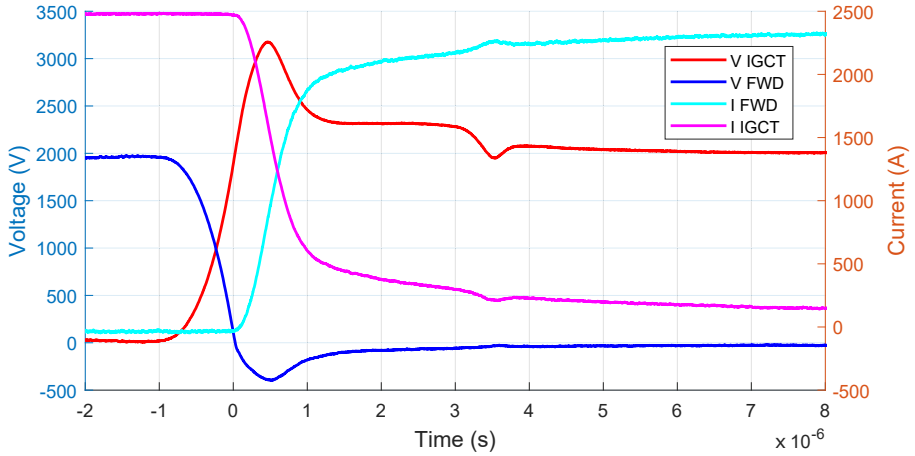
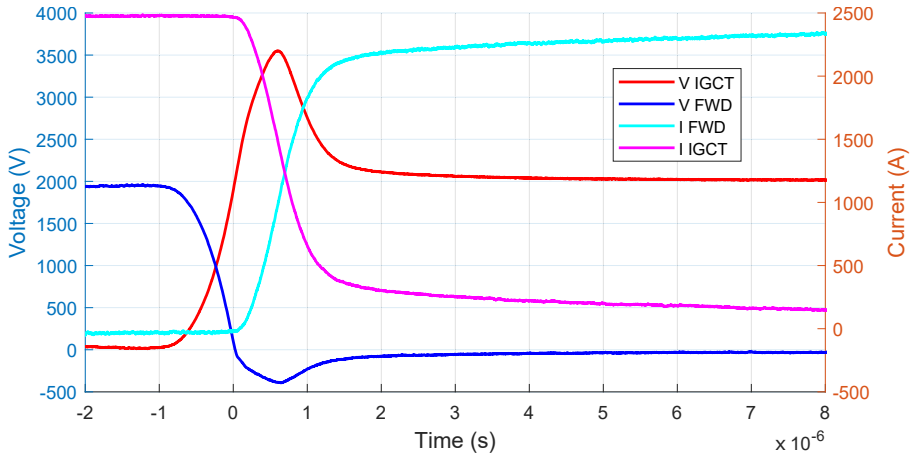
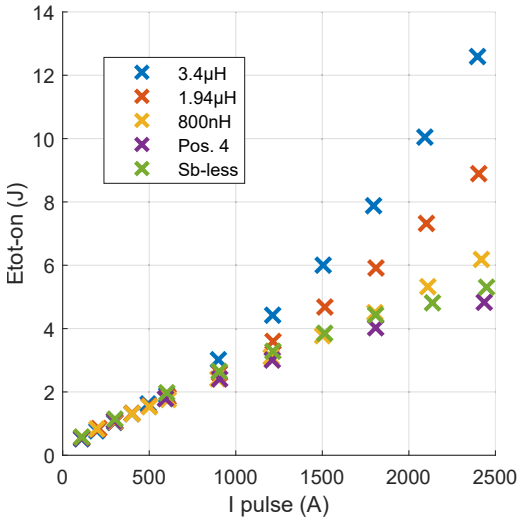


(a) With RCD.

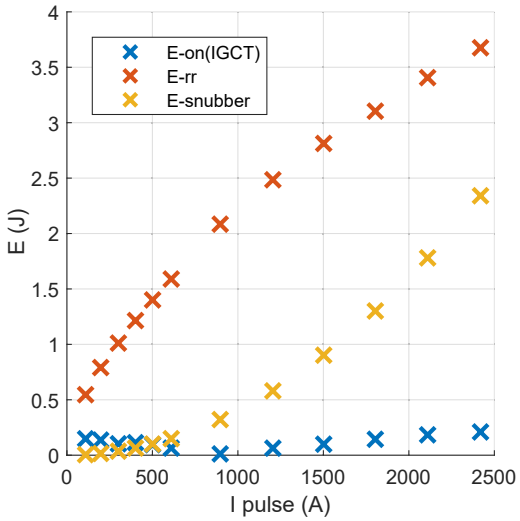


(b) Without RCD.

Figure 4.31: Waveforms of turn-off of the case with and without RCD clamp. 2000V, 2400A, 120°C, 4.5kV diode, busbar position n°4.



(a) Total Losses for 2000V; 120°C.



(b) Distribution of the losses (in J), for 2000V; L_{snu}=800nH; 120°C.

Figure 4.32: Losses at turn-on: total losses depending on snubber configuration (left) and distribution of the losses among the different parts (reverse recovery, IGCT turn-on, snubber).

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4.2.8.1 Effect of stray inductance on the commutation

To understand fully the conclusions listed in this section, it is important to understand the role of the stray inductance in the circuit on the following aspects. It has:

- A clearly identified impact on snap-off overvoltage values.
- A clearly identified impact on overvoltage without snap-off.
- A potential impact on snap-off occurrence.

Reducing the stray inductance would lead to lower overvoltages (for snap-off and non-snap-off events), could lead to snap-off happening on lower range and potentially using the diode at lower temperature (hypothetical). But the stray inductance, in a snubberless configuration is limited and cannot be lower than 215nH for the 4.5kV diode (see table 3.3).

4.2.8.2 Snap-off event in soft-recovery diodes

As a reminder, these diodes are considered fast because they display high di/dt capability. Still they are considered soft because their reverse recovery has a soft behaviour, as described in section 4.1.3.

This experiment has confirmed the literature results on diode snap-off: the operational parameters influence on snap-off levels (temperature, voltage, current and stray inductance), the failure potential of this phenomenon, and the fact that soft-recovery diodes can present a snappy behaviour. What should be studied further is the transition between soft and snappy behaviour due to stray inductance: at what level of stray inductance the snap-off disappears or at least is negligible at typical current, voltage and temperature levels?

The press-pack freewheeling diode recommended for the IGCT as the freewheeling does not display any snap-off at the same levels of current and voltage, as shown in subsection 4.2.3.3.

4.2.8.3 Diode selection process

The 4.5kV diode has shown the possibility to be operate snubberless. The 6.5kV diode has not been tested snubberless, to avoid a failure like in section 4.2.4.2, that was due to a high forward current and high di/dt at 0A. For the two diodes however, the stray inductance in our circuit was higher than the ones considered in their datasheets (450nH instead of 150nH for the 4.5kV diode and 280nH for the 6.5kV diode). This difference in stray inductance could explain the snap-off phenomenon appearing more often than expected (as a reminder these diodes are sold as soft-recovery diodes). It seems likely that at a closer stray inductance and/or without being used with an IGCT, they do not experience snap-off, because they are used in other configurations, in particular with IGBTs. That has been the major problem of using diodes designed to operate with IGBTs.

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It can be clearly concluded that these PM fast diodes cannot be used in this configuration with an IGCT in an MMC: for typical MMC voltage and current levels, at ambient temperature, these diodes experience destructive snap-off phenomenons (see subsection 4.2.3.1, with figure 4.21). The snubberless IGCT-based submodule should be equipped only with diodes not experiencing this kind of constraint: either the same diodes with a different configuration and lower stray inductance, or fast diodes not experiencing destructive events (snap-off or dynamic avalanche at high di/dt). Both of these hypothesis have to be confirmed with experience. For the second hypothesis, SiC PiN diodes will be tested in this setup in the next chapter.

4.2.8.4 Reducing the snubber size

It has been possible to reduce the snubber inductance to the lowest possible value of the experimental setup for the 4.5kV diode (position 4 of the busbar, around 100nH). But the 6.5kV diode failed at the busbar position 1, meaning that it might have been too risky to reduce the snubber inductance further, even if the failure resulted from a combination of factors (voltage, current, di/dt, stray inductance) rather than simply the di/dt or the snubber inductance value.

The results of this study confirmed the possibility of reducing the snubber inductor, compared to typical designs using 6.5kV IGCTs (see table 2.4), and which can lead to a reduction of the snubber capacitor and therefore of total volume, cost and losses. The snubber inductor was reduced to a few hundreds of nH for the 4.5kV diode, and worked efficiently at 2.4kV and 1.8kA at a temperature of 90°C and 120°C (for 25°C and 60°C: 1.7kV 2.4kA). But it has to be noted that reducing the snubber inductance leads to higher losses in the diode during the reverse recovery.

4.2.8.5 Removing the snubber

Removing entirely the snubber has been done and tests were completed up to 2.4kV and 1.8kA at 120°C and 90°C, and 1.7kV and 600A at 25°C with the 4.5kV diode. Removing the RCD clamp increased the unclamped stray inductance, leading to higher overvoltages and switching losses, but also to more intense snap-off events. To be conclusive, removing the snubber entirely needs to be done with the minimum possible inductance. This can be accomplished either by reducing the busbars length , or even further but adding one or two more diodes in parallel (the di/dt limit of the obtained diode would be higher) and stray inductance can be reduced even further. As pointed out in table 3.3, the needed inductance to reach a di/dt value of 13kA/µs (diode limit) is 215nH. A realistic stray inductance reduction objective can be 250nH of total stray inductance.

For the 6.5kV diode, it seems rather unlikely to remove the snubber completely. On top of having a lower di/dt rate than the 4.5kV, the failure event happened at a lower voltage level than the diode voltage rating (3300V rather than 3600V). It seems to point out that there is no margin to reduce the stray inductance. A lower stray inductance will lead to a lower overvoltage but to a higher di/dt, which the 6.5kV diode might not be able to withstand.

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4.2.8.6 Losses and volume reduction

With this study, it has been proved that a volume reduction (by reducing the snubber inductance, or removing the entire snubber) is possible. It has also been proved that reducing the snubber leads to lower levels of losses (see subsection 4.2.7). Also, even if removing the RCD clamp increases the losses by a little (compared to the situation with the busbar position and an RCD clamp), it still represents a lower level of losses than a configuration with a cable inductor and an RCD clamp.

4.2.8.7 The limits of this study

The results presented in this chapter, while proving the main goal of this thesis (to remove entirely the snubber), has its limits:

- One type of diode was selected: fast soft diodes in a plastic module, designed to work with IGBTs. A semiconductor simulation study could identify adjustable parameters to make the snubberless operation more efficient (less snap-off).
- Understand, model and study the voltage drop of the IGCT.
- The stray inductance has been proved to be too big, at least way bigger than the diode datasheets indications (for the SOA). A further reduction of the stray inductance could be possible in the future with the space left by snubber been fully removed with the 4.5kV diode. This reduction could lead to lower snap-off and lower overvoltage for clampless/snubberless operation.
- The possibility of having a reduced snubber inductance has been shown, but no optimisation of the whole snubber, with different values of R, C and different diodes, has been studied to assess the gain in volume.
- Reliability of the IGCT at high di/dt has to be studied to conclude fully on the interest of the clampless/snubberless submodule.

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Chapter 5

IGCT Switching with SiC PiN diodes at high di/dt

As shown in the previous chapter, snubberless operation of IGCTs is limited by the performance of Si diodes during their recovery (snap-off, dynamic avalanche...). In this chapter, we investigate the use of SiC diode to overcome this limitation.

The SiC diode dies which were used are presented in the first section. A specific packaging, designed specifically for this work is detailed in the second section. The packaged SiC diodes were tested in the test setup with the IGCT. Results are displayed and discussed in the third and last section.

5.1 SiC PiN diodes

5.1.1 Difference with Silicon PiN diodes

In subsection 1.2.1, the interest of silicon carbide (SiC) compared to silicon (Si) has been discussed. In this chapter and this thesis work in general, the interest of silicon carbide is to offer very good reverse recovery characteristics, such as lower losses, lower stored charge, and faster reverse recovery. This is explained by the fact that silicon carbide has a wider energy band gap leading to a thinner base region (for the same blocking voltage) and therefore a lower quantity of stored charge.

If we model simply the forward voltage by the equation $V_F = V_0 + R_{on}.I_F$ (with V_0 the forward voltage drop at low current, R_{on} the on-state resistance, and I_F the current through the diode), then the wider band gap has the effect of increasing the forward voltage drop at low current V_0. On-state resistance R_{on} on the other hand is lower (for the same surface and breakdown voltage), due to the thinner base region.

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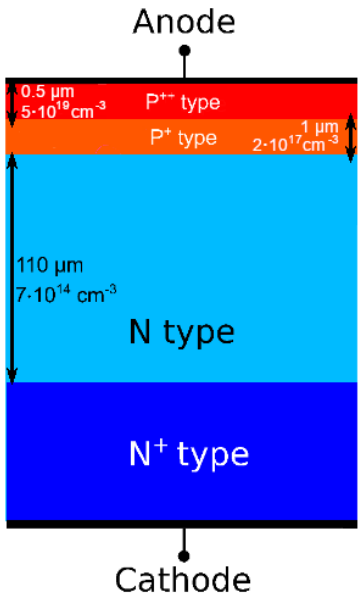

Figure 5.1: Structure of the PiN diode used in this work (thicknesses and dopings). Adapted from [6].

5.1.2 Description of the SiC diode dies

The diodes dies used here were designed during previous projects in SuperGrid Institute and Ampère Lab. This section presents the results of these studies [6, 7].

5.1.2.1 Semiconductor structure and voltage characteristics

The diodes dies were designed to withstand 10kV (breakdown voltage) and conduct 50A (nominal forward current) for the 10mmx10mm size die (outside dimensions). A 4 inches wafer from CREE has been selected and the different layers (with their associated doping and thicknesses) of the diode are displayed in figure 5.1. The total thickness of the diode is 500µm.

The theoretical breakdown voltage limit of this structure is 13.2kV [6] (using infinite plane-parallel junction model). But due to imperfect process, the obtained breakdown voltages will be lower and different from one die to another, with some diode breakdown voltages higher than 11kV and other lower than 5kV, and some even around a few tens of volts. An unsawn wafer is displayed in figure 5.2a and the associated voltage map is displayed in 5.2b. Even if during the previous projects, the diodes not reaching 5kV were considered faulty, in this work, diodes dies with breakdown voltage starting at 2kV are being used. Their voltage distribution is given in figure 5.3.

5.1.2.2 Other characteristics

In [6], typical static and dynamic characteristics values are given such as the voltage at 10A and 50A; the on-state resistance; the junction capacitance at 60V and 3kV. These paramaters values can be seen in table 5.1. Given the on-state resistance of 23.3mΩ, and the active area of

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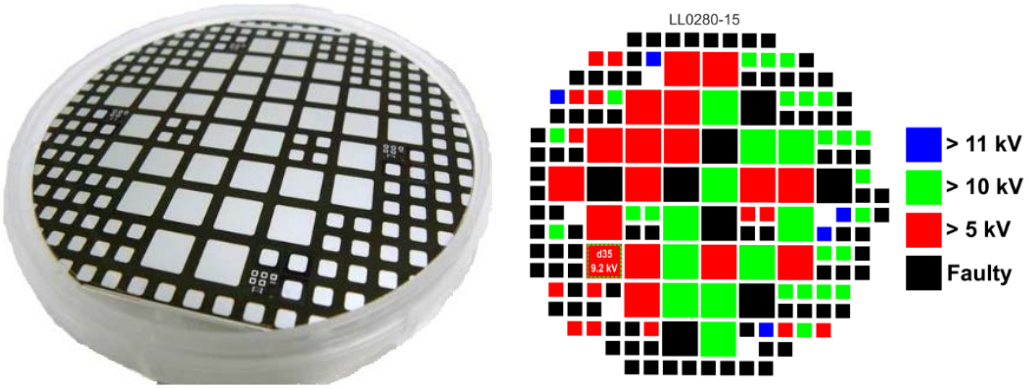

(a) Wafer with diodes, before being cut. (b) Diode Voltage distribution.

Figure 5.2: One of the wafer of the SiC PiN diodes designed at SuperGrid Institute and their associated breakdown voltage map [6]. In [6], a diode with a lower breakdown voltage than 5kV is considered faulty.

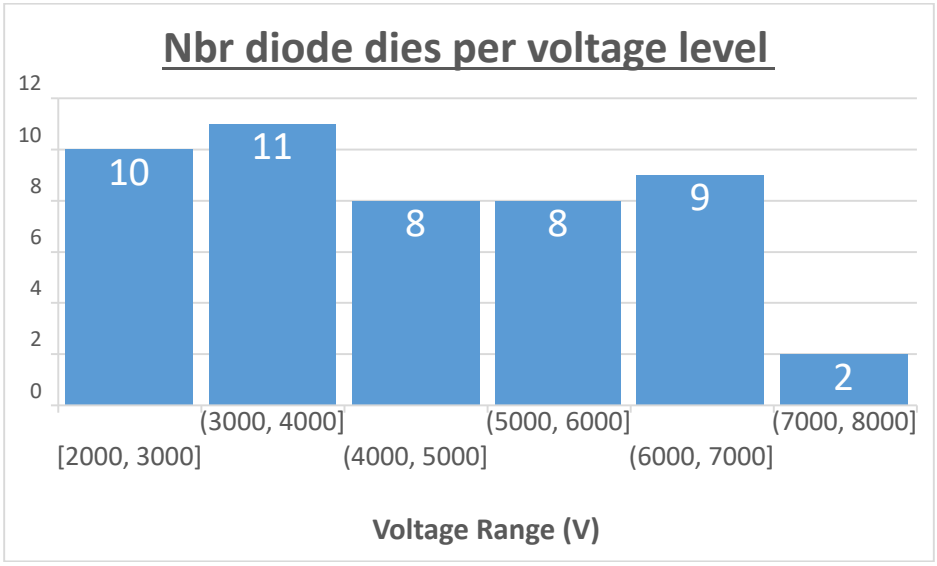

Figure 5.3: Voltage distribution of diodes dies used here.

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59mm², it corresponds to a resistivity of 13.8mΩ.cm², lower than the theoretical limit of SiC unipolar devices.

Table 5.1: Diode Die Typical Parameters Values [6]

Diode Die Parameter	V_F**(50 A)**	V_F**(80 A)**	R_{on}	C_j**(60 V)**	C_j**(3 kV)**
Typical Value	4.98 V	5.68 V	23.3 mΩ	594 pF	82.2 pF

5.2 Packaging of the SiC dies

Because only bare dies diodes were available, and because we had to accommodate the existing test set-up, a custom package was designed.

Before considering the design itself, the overall concept of the package has to be explained. Some important features are listed below:

- Due to the small quantity of diode dies, the large spread in their voltage ratings and a limited confidence in the packaging operation, **the package will be divided into sub-packages** with a limited number of dies to increase yield.
- Due to the poor condition of the top face of the diode dies, a **local pressing system** on the dies using spring contact probes is selected rather than classic bonding wires.
- Substrates from a previous project [95, 94] are used, because they have proved voltage withstand capability across the ceramic layer. Given the substrate size, there are **4 dies per sub-package**.

5.2.1 Constraints to be considered

5.2.1.1 Ratings and related constraints

Voltage rating The voltage of the dies, as described in section 5.1.2, is maximum 13kV theoretically, but the maximum voltage measured among the available dies that will be used is 8kV. 8kV will be considered for the clearance and creepage distances. IEC 61800-5-1 gives the value of 25mm for clearance distance. The pollution degree is considered to be I (scientific experiment in a laboratory), giving a creepage distance value of 32mm independently of its insulating material group (defined by the CTI of the material). Silicone encapsulation will be used to provide insulation inside the package. The dielectric insulating silicone should have a rating of at least 10kV/mm considering that the edge termination region is 1mm wide. The silicone encapsulation is detailed in section 5.2.3.5. The plastic casing of the package needs to have high dielectric strength (chosen arbitrarily, at least 10kV/cm).

Current rating The nominal current of the dies is 50A. This value will be used to determine conducting parts sizes (busbars, spring contact probes, conductive layers in the PCB). Because

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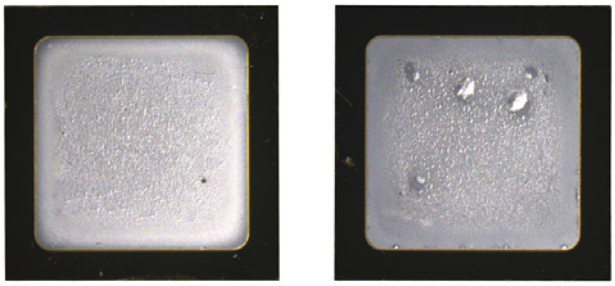
these diodes will be tested in a double pulse setup, the nominal current capability requirements are not critical from a thermal point of view.

Temperature constraints The maximum temperature considered for the tests is 120°C. This value has an impact on the plastic package choice (plastic glass transition temperature is critical) and the insulating silicone. The base plate and the glue attaching the substrate have to be as heat-conductive as possible. A metal is preferable for the base plate. However because of the double-pulse test configuration, which dissipates little power on average, thermal resistance of the package was not considered as critical as voltage withstand.

5.2.1.2 Die related constraints

Die attach The bottom material of the die (cathode) is silver. Silver sintering is a die-attach process which allows good position control of the die and had previously been used in Ampere Lab (like in [71] seems therefore the most adequate process to attach the dies on the copper substrate. The silver sintering has been realised in this work with Ag-paste mAgic PE338 (ASP338-38 F150) from Heraeus.

Top contact Photographs of the top face of some dies is displayed in figure 5.4. The surface is irregular and presents bumps. Because of this, wire bonding has not been selected to avoid any risk of tearing up the top metalization. This lead to the development a local pressing solution on the top of the dies, that will be developed in subsection 5.2.2.5.



(a) Diode a. (b) Diode b.

Figure 5.4: Typical top face (anode) of the diode dies.

5.2.1.3 Mechanical and physical constraints

Adaptation to the current experiment setup To be tested in the test setup presented in chapter 3, the SiC diode package must be mechanically compatible with the ABB diode package. It must respect the mounting holes positions for the base plates, and the busbars holes positions for the bubsbars.

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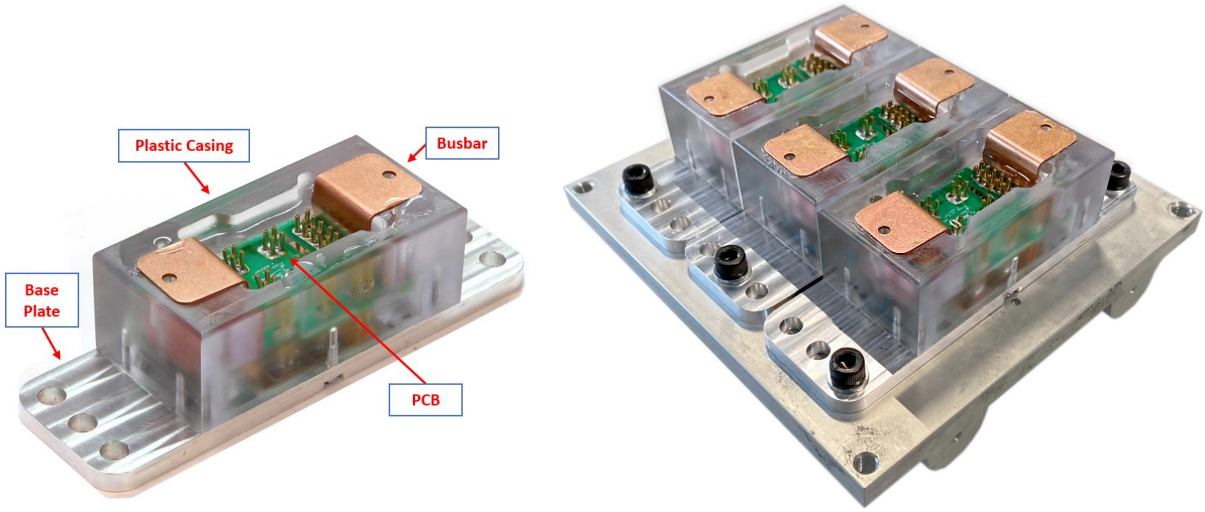
Efforts in the package As said previously, a local pressing system on the dies using spring contact probes is selected. Due to the spring efforts, a special focus has been given to the distribution of the efforts in the package to avoid gaps between the base plate and the casing (to ensure good silicone encapsulation) and to ensure good electrical contacts.

5.2.2 Package design

5.2.2.1 Overview of the final design

The final design is displayed in figure 5.5. The diode is divided into 3 sub-packages, put in parallel, as shown in figure 5.5b. One sub-package is displayed in figure 5.5a, with its main parts.



(a) One sub-package.

(b) Three parallel sub-packages, on the heatsink used with the PM diode.

Figure 5.5: Final Design of the diode package.

A simplified sectional view of the sub-package can be found in figure 5.6. This schematic only displays one diode die (out of four) and one contact spring probe per side (instead of 4 per die on the anode side, 16 total and 14 on the cathode side). The different parts are detailed below.

5.2.2.2 Substrate

The substrate has been taken from a previous project in SuperGrid Institute and Ampère Lab [95, 94] because it was in stock and proved its 10kV voltage withstanding capability. The ceramic layer is made of aluminium nitride (AlN) with a 635µm thickness, the top and bottom layers are copper layers of 300µm thickness and the braze alloy used to attach the copper on the aluminium nitride is a mix of titanium, copper and silver (TiCuSil). The subtrate dimensions are displayed in figure 5.7.

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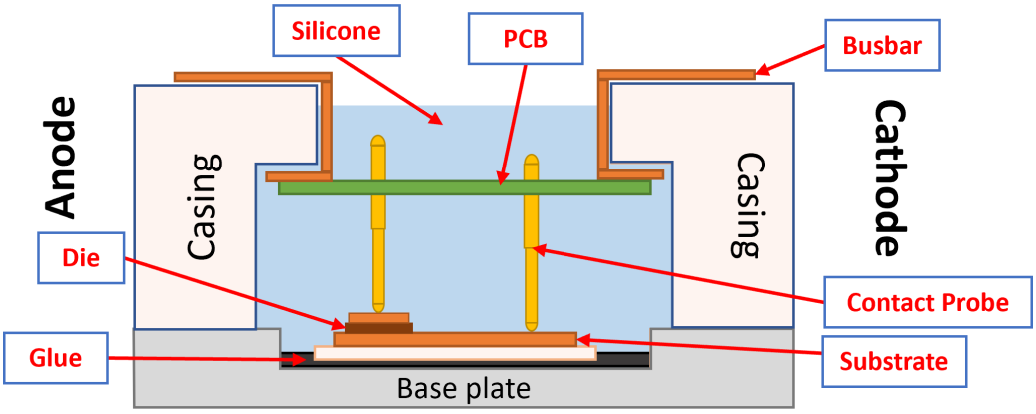

Figure 5.6: Sub-package, sectional view, simplified schematic.

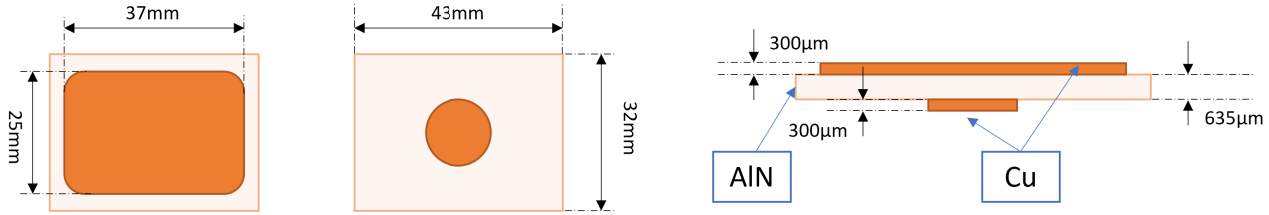

Figure 5.7: Dimensions and materials of the substrate.

5.2.2.3 Base plate

The base plate (see figure 5.8a) is built in Aluminium (6061-T6 type), manufactured with CNC. The **central cavity** hosts the substrate that is inserted. **Side cavities** serve as retention pools to absorb any excessive glue. Three types of holes exist on the base plate (see figure 5.8b): **Hole A** is an alignment hole (diameter of 3H9), **Hole B** is a mounting hole to pass and hold the screws coming inside the casing (6 screws tightening casing and base plate together), **Hole C** is a mounting hole to pass and hold the 2 screws tightening the base plate to the heatsink designed for the ABB diode. There are 6 C holes to allow each base plate to be tightened at any position (left, middle or right position) in the three parallel sub-package configuration, as it can be seen in figure 5.5b.

5.2.2.4 Casing

The 3D model of the casing is displayed in figure 5.9.

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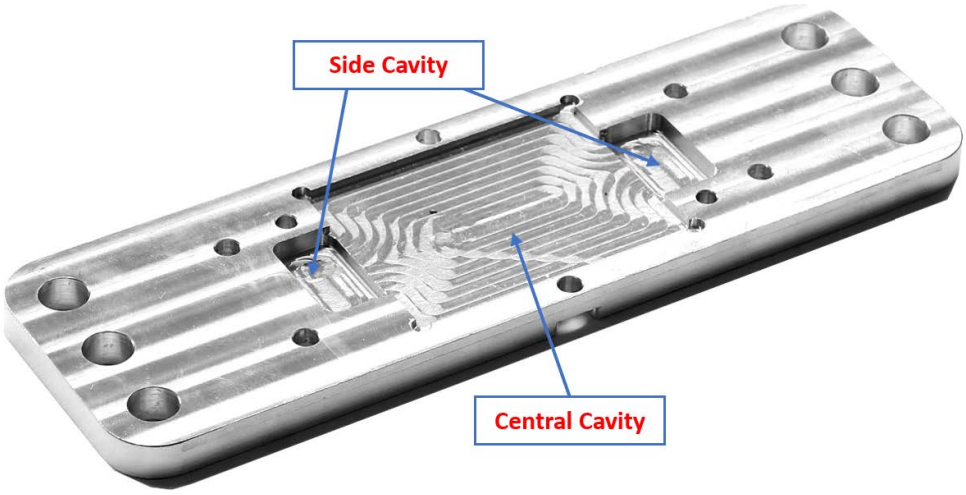
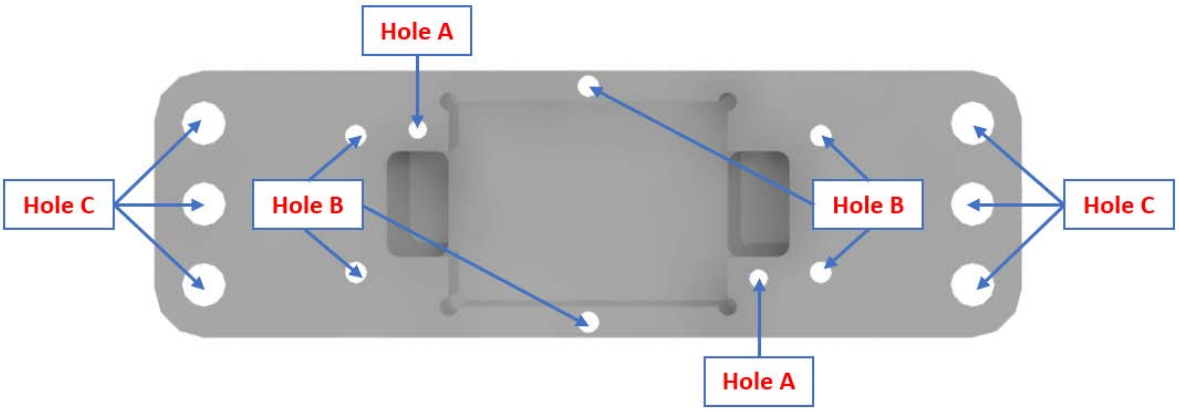


(a) Base plate picture.



(b) Rendered base plate, top view.

Figure 5.8: Base plate.

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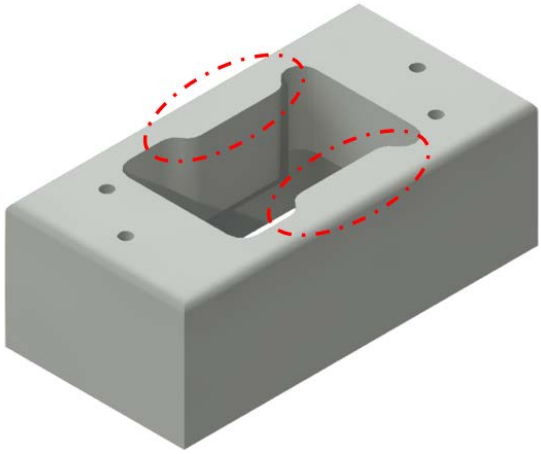
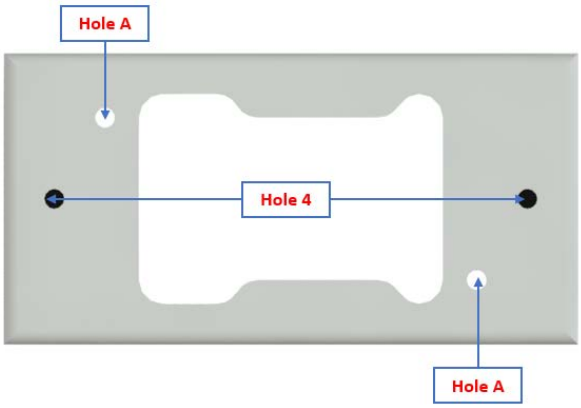
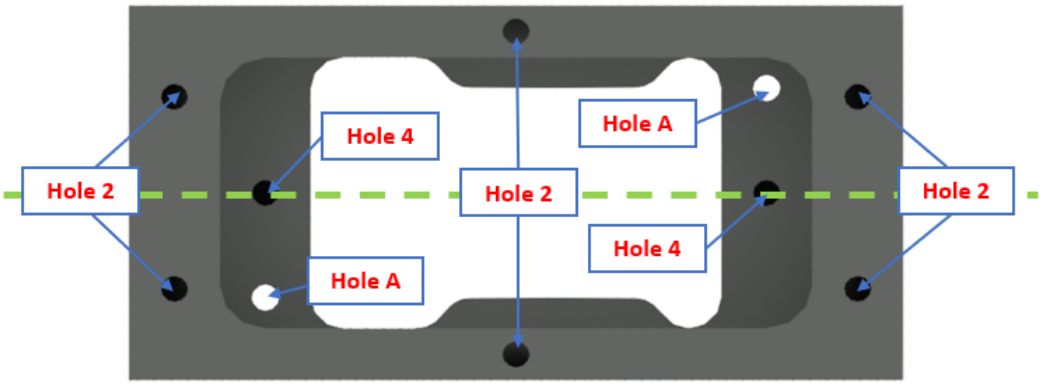


(a) Diagonal view.



(b) Top view.

(c) Cross-section, following the green line in fig. 5.9d .



(d) Bottom view.

Figure 5.9: Plastic casing design, 3D rendering.

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Material choice: In [94], potential casing materials are compared. In this thesis work, it has been decided to use Polycarbonate (PC). PC has been selected due to its high glass transition temperature (140°C), its dielectric strength (at least 15kV/mm), and its hardness (to have strong threads in the casing).

Design: On top of the consideration of creepage and clearance distances, the assembly and stress distribution has been taken into account. It has been chosen to have six threads for the attachment with the base plate (**Holes 2**, complementary of the **Holes B** in the base plate), with holes near the center to ensure a good effort distribution. As for many parts of the package, an alignment hole is present (**Hole A**, with the same diameter as for the base plate). The **Holes 4** receive the screws for the busbars connections on top of the casing and for the busbar/PCB connection on the bottom.

To ensure a homogeneous distribution of the efforts in the package and to avoid PCB bending (the PCB is presented in section 5.2.2.5), a middle reinforcement, circled in red in figure 5.9a has been added to the design.

5.2.2.5 Busbars, printed circuit board and pressing system

Pressing system and die top contact As shown in section 5.2.1.2, the top face of the diode die is irregular and it has been chosen to avoid wire bonding. Therefore, a local pressing system has been designed, and is displayed in figure 5.10. For 1 die, it uses 4 spring contact probes soldered together on a copper plate that is in contact with the diode die. The copper plate is small enough (6mm×6mm) to avoid any contact with the peripherical protection of the die.

While the contact pins have a small nominal current (3A), it was considered here that they could be used at much higher value: as explained above, their tip is soldered on a large copper plate, improving current distribution, the double pulse test conditions correspond to a high peak current but a small average one. Finally, tests with a curve tracer showed that the springs were strong enough to maintain contact up to 500A.

(a) Four local pressing systems. (b) Schematic.

Figure 5.10: Local pressing system design.

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Printed Circuit Board The local pressing systems are soldered to a Printed Circuit Board that can be seen in figure 5.11. As described previsouly, the contact on the anode side (top face) of the die is realised with the local pressing systems. For the cathode side (bottom face), the current is transported in the copper of the substrate and comes in the PCB through the 14 spring contact probes on the right of the PCB in figure 5.11. Holes on the corner of the PCB are made for the alignment rods to pass through, like for the casing and the base plate, and ensure that the copper plates of the pressing systems are in the middle of the diode die top face.

(a) Top view. (b) Bottom view.

Figure 5.11: Printed Circuit Board for one sub-package.

Busbars 1mm thick copper busbars are used to transport the current from the PCB to the rest of the circuit. One type, that can be seen in figure 5.12a is located inside the sub-package. The other type of busbars (figure 5.12b) is located outside the sub-package connects sub-packages together and mimics the terminals of the ABB diode. Because the PM diode has two connectors, the choice has been made to connect two sub-packages in parallel for one connector and the third diode with the other connector. The lenghts of the connectors have been calculated to ensure equal current sharing between the three sub-packages in parallel.

5.2.3 Packaging process

5.2.3.1 Substrate preparation

As described in section 5.2.2.2, the substrate that is used in this package has 300µm thick copper layers on both top and bottom sides. Only the top face will be used to sinter the diodes and the bottom face will be put in contact with the base plate. To prevent damage to the substrate during the pressure-assisted sintering, the copper patter is removed from the bottom side.

The process steps are illustrated in figure 5.13, with the initial state of the bottom face in figure 5.13a. To remove the copper from the bottom face, ferric chloride ($FeCl_3$) is sprinkled on the substrate during 5 minutes. To protect the top face copper of the substrate, blue Dry

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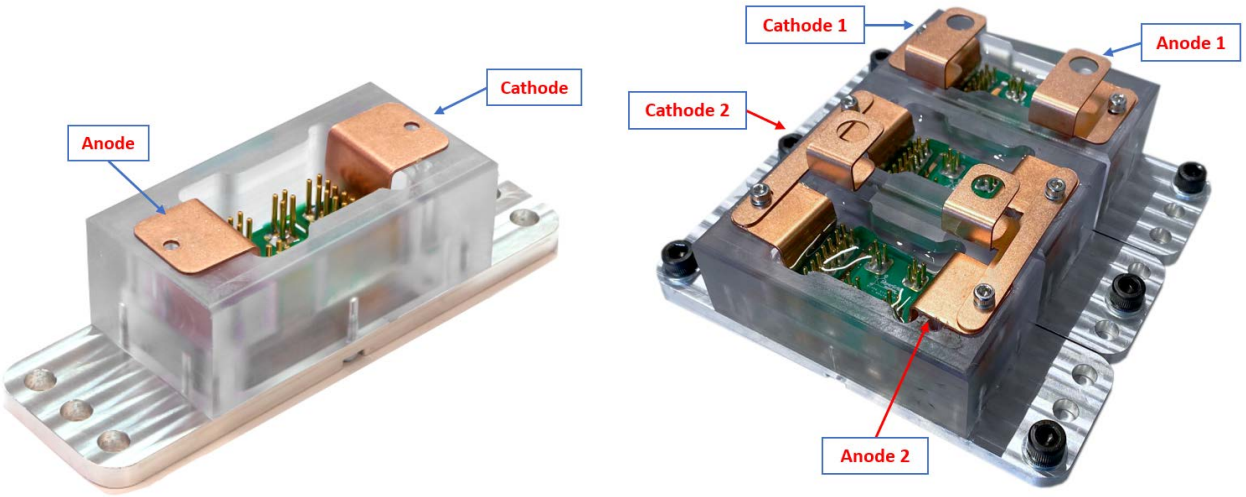
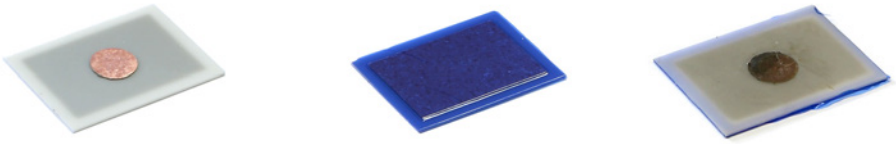


(a) Sub-package view. (b) Full-package (3 diodes).

Figure 5.12: Busbars in the package, with location of anodes and cathodes.

Film Photoresist (DFP) is covering the top face, as it can be seen in figure 5.13b. The result of this removal can be seen in figure 5.13c. The copper has been removed but the thin (a few µm) braze alloy layer remains. This is considered acceptable for the next steps.



(a) Bottom face, before. (b) Top face, with DFP. (c) Bottom face, after.

Figure 5.13: Steps of substrate preparation, before sintering, copper removal from bottom face.

5.2.3.2 Silver Sintering

The steps of the sintering process are displayed in figure 5.14.

Deoxidation of the substrate: A small step before using the Ag-paste is the deoxidation of the top copper surface, to ensure a good adhesion between the silver paste and the copper. This is realized using hydrochloric acid (HCl) vapor, rinsed with deionised water.

Application and drying the Ag-paste step: After deoxidation of the substrate, the Ag-Paste is applied using a stencil in a similar manner as in figure 5.15b for the die placement. The square holes in the stencil have sides 100µm smaller than the diode die side. The substrate is then placed in an oven (Jipelec JetFirst) for drying the paste (140°C, 20min, in N2 atmosphere).

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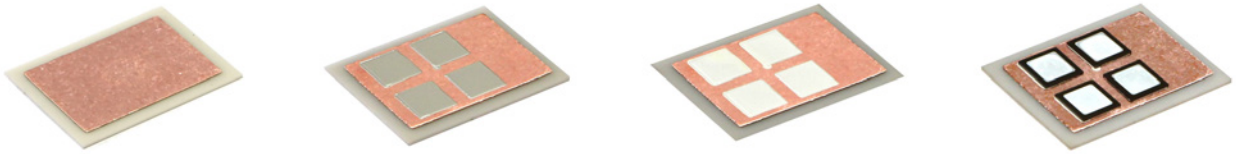
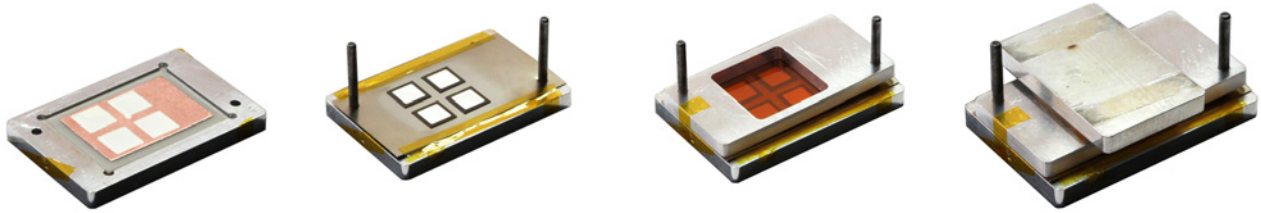


(a) After Desoxidation. (b) After Ag-Paste Application. (c) After Drying. (d) After Sintering.

Figure 5.14: Steps of dies sintering, from bare copper to sintered dies, top layer.

Sintering: The pressuring assembly to sinter the diodes dies on the substrate is displayed in figure 5.14. It uses an aluminium piston and polyimide sheet to provide a buffer function and distribute the pressure. The pressing system installed in the oven is limited to about 1.4kN (7 bars with a 50mm diameter oven piston). Considering the pressure us evenly distributed on the 4 $1cm^2$ dies, this corresponds to a pressure of 2.5MPa, lower than the value recommended by the paste manufacturer (10 to 30MPa). To compensate for this low pressure, a high temperature (280°C) and a longer duration (10 min instead of 3-5 min) are applied.

The substrate is placed in the cavity of the holder (figure 5.15a), then a stencil is positioned precisely thanks to the alignment rods (figure 5.15b). The square holes in the stencil have sides 200µm larger than the diode die side. 4 dies are placed and then the rest of the pressuring assembly (polyimide sheet + guide + piston, figures 5.15c and 5.15d). The whole is then installed in the JetFirst oven and the sintering process is carried out (10min, 280°C, 2.5MPa, in N2 atmosphere). The result can be seen in figure 5.14d.



(a) Subtrate in Cavity. (b) Die placement. (c) Polyimide sheet and guide. (d) Final, with piston.

Figure 5.15: Steps of pressure device assembly for sintering.

5.2.3.3 Die preparation

In the first sintering attempts, it was found that no satisfying attach could be obtained using the dies directly out of their container (maximal shear strength of 1.6MPa only). After some investigations (SEM, X-ray fluorescence, Raman microscopy), an hypothesis was made that this poor adhesion could be due to some organic pollution layer.

In [103], plasma cleaning of the bottom face of the die, before Ag-based sintering is recommended, to remove pollution. In [121], different plasma recipes are studied. It has been concluded for this thesis that O_2 and Ar plasmas would be used to ensure the removal of any

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pollution layer. The retained plasma recipe is 2min 30sec of O_2 plasma followed by 2min 30sec of Ar plasma, both with a 1000sccm inflow, 300W power and 100mTorr pressure. The final plasma cleaning process has been established due to the following reasons:

- The use of O_2 plasma only, or a mix Ar/O_2 resulted in the oxidation of the silver.
- It has been prefered to use both types of plasmas to ensure an extensive cleaning.
- Ar plasma is used after O_2 to remove the oxidation created by the O_2 plasma.

Attach test The attach of the dies have been tested. It resulted in a passed shear test at 180kgf ($18N/mm^2$) without any destruction or detachment. It confirms the good attach of the dies on the substrate with the Ag-based sintering and the need to clean the diode dies with plasma before sintering.

5.2.3.4 Assembly

Substrate gluing in the base plate The substrate is glued with Duralco 133, a thermally conductive glue, with 1g of glue. The glue is cured for 4h at 121°C with pressing weights to ensure the surface of the substrate is flush with the baseplate.

Soldering The pressing local systems are soldered together (contact probes + copper plates). Then the PCB is soldered with the spring contact probes. To ensure the optimal spring travel and therefore the best current conduction, a guide is used during soldering, holding the pins and copper plates at the correct distance.

Mechanical assembly Using alignment rods in Holes A, the sub-package is assembled with the PCB and the busbars screwed on Holes 4, the casing with the base plate screwed with Holes B and 2.

5.2.3.5 Silicone encapsulation

The silicone encapsulation takes place after the whole package (PCB + busbar + base plate with substrate and dies + casing) is assembled. The silicone used here is SilGel 612 from Wacker. It has a voltage withstand capability of more than 23kV/mm. Once the package is ready for encapsulation, the two components of the SilGel 612 are mixed in a 1:1 ratio and degassed during 15min under vacuum in the mixing vessel. The silicone is then poured in the package and degassed again in a vacuum enclosure. After 30 more minutes of vacuum treatment, the whole assembly is put in an oven at 100°C during 15min.

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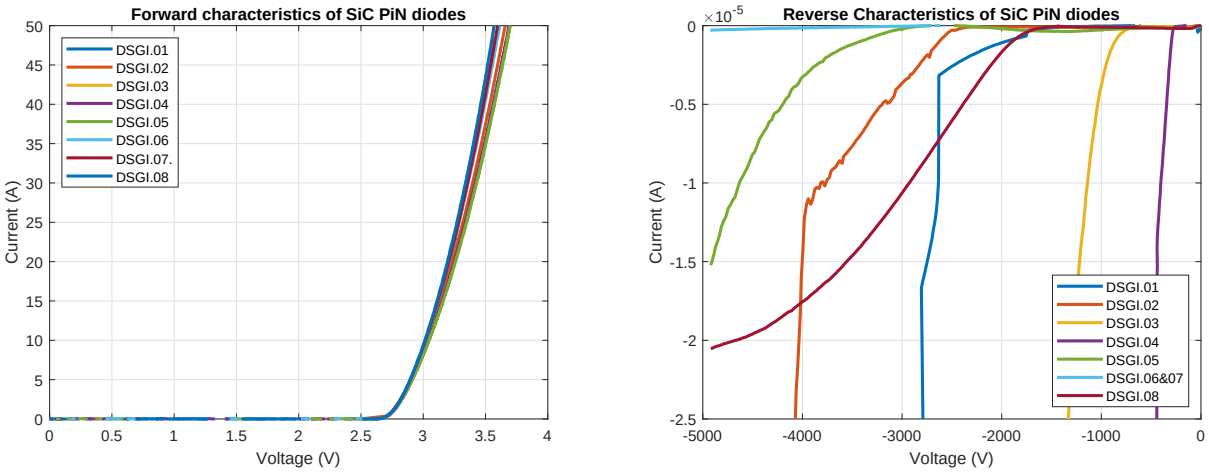
5.2.4 Characterisation of the obtained diodes sub-packages

8 sub-packages have been obtained out of the process described in this section. They are numbered from 01 to 08, ordered by creation date.

Forward characteristics The forward characteristics of each diode sub-package are displayed in figure 5.16a. Typical values for the forward characteristics can be found in table 5.2. The voltage drop of 2.7V corresponds to the value in [6], as much as 6.5mΩ for 4 diode dies correspond to the 24mΩ for 1 diode die from [6]. The difference on on-state resistance can be explained by a slightly more resistive package in this thesis. It should be noted that the diode sub-package n°04 has been tested with 1kA 400µs pulses, without noticeable damage.

Table 5.2: Diode Sub-package Typical Parameters Values.

Diode Sub-package Parameter	V_0	$R_{on}(50A)$	$R_{on}(200A)$
Typical Value	2.7 V	12.8 mΩ	6.5 mΩ



(a) Forward characteristic.

(b) Reverse characteristic.

Figure 5.16: Forward characteristics of the 8 obtained sub-packages.

Reverse characteristics The reverse characteristic of each diode sub-package is displayed in figure 5.16b. The values of reverse blocking voltage for each diode sub-package can be found in table 5.3. What can be analysed from the values is that 1µA cannot be the reference current for determining the breakdown voltage: the diode n°08 has a reverse voltage of 1.8kV at 1µA but more than 5kV at 25µA.

Table 5.3: Diode Sub-package Reverse Voltage Values. Obtained with Keysight B1506a, with a voltage source limited to 5kV.

Diode Sub-package (n°)	01	02	03	04	05	06	07	08
$V_r(1\mu A)$ (V)	1950	2620	862	296	3420	>5kV	>5kV	1882
$V_r(10\mu A)$ (V)	2630	3752	1137	402	4625	>5kV	>5kV	2031
$V_r(25\mu A)$ (V)	2806	4072	1332	443	>5kV	>5kV	>5kV	>5kV

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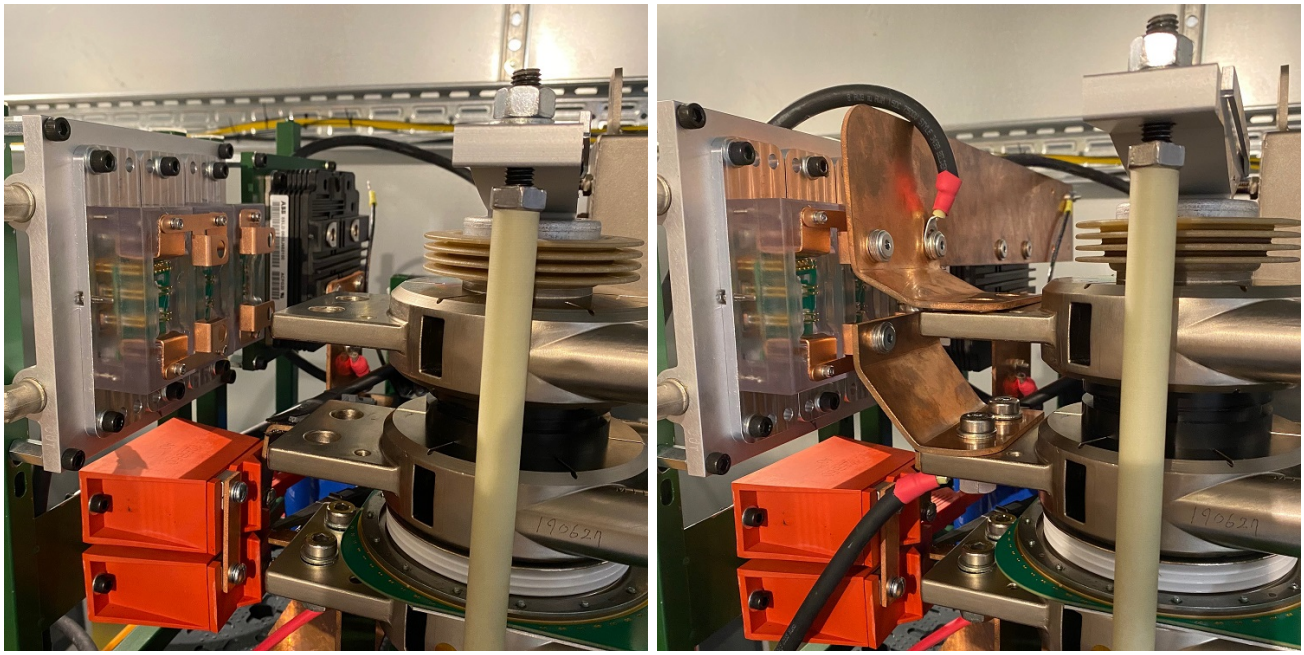

(a) Without main busbars. (b) With main busbars.

Figure 5.17: Integration of the SiC full-package (3 diodes) on the IGCT double pulse test setup.

5.2.5 Conclusion on the packaging of the SiC diodes

An original packaging has been designed to respect the features and constraints of the SiC PiN diode dies used here, but also the constraints of the test setup. This led to the fabrication of operational sub-packages that can be put in parallel to reach theoretically a nominal current of 600A and a breakdown voltage higher than 5kV.

These SiC diode sub-packages will be used in the double pulse test setup together with the silicon IGCT, to explore the possibility of snubberless operation.

The full-package configuration integrated in the test setup presented in the last two chapters can be seen in figure 5.17.

5.3 Double pulse with IGCT

5.3.1 Current surge test

To evaluate the maximum current that a sub-package can withstand during this amount of time, a "surge" test was performed, during which peak current would be increased until the sub-package failed.

Only the diode sub-package n°01 has been tested in the following configuration: 2.8mH for the double pulse inductor, around 600V during turn-on, with a 3.4µH snubber inductor, only one sub-package (no paralleling), room temperature. The double-pulse waveforms of these tests

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were recorded on 1ms, which is way lower than the estimated duration of the whole double pulse (120ms, obtained with LTSpice simulation).

Result and waveforms The diode withstood pulse up to 510A at turn-on but failed during the freewheeling phase with 550A. With 550A, the energy dissipated in the diode sub-package is 424J (calculated as $E = 1/2.L_{dp}.I^2$). The scope of the recorded waveform was limited to what is displayed in figure 5.18b. Therefore an LTSpice simulation was run to obtain the equivalent I^2t of the diode. It uses a diode model of 6mΩ on-state resistance and a voltage drop of 2.7V, an inductance value of 2.8mH and a 50mΩ ESR (value from the datasheet of the inductor), and the obtained I^2t value is 6.8kA^2s.

The waveforms of the pulse without failure (490A at turn-on, 525A during freewheeling period) and the failure pulse (510A at turn-on, 550A during freewheeling period) are displayed in figure 5.18a and in figure 5.18b respectively. What can be analysed from these waveforms is that the pulses seem both normal. Therefore the failure event happened during the freewheeling period, not recorded on the oscilloscope.

Failure analysis The failed sub-package is displayed in figure 5.19. It can be seen that burnt silicone is present, leading to a hypothesis of arcing during the failure, between the cathode (positive voltage of the bus) and the base plate (ground). But it does not mean that this is the reason why the diode failed: the arcing could be due to the diode failure, and not the diode failure being due to the arcing. The diode could have, while conducting current, failed. This would have interrupted the current through the charge inductor, leading to a large overvoltage and arcing.

To know more about the failure, the sub-package n°01 has been disassembled. Arcing traces have been found (as it can be seen in figure 5.20) with arcing traces on the base plate (figure 5.20a) and on the casing (figures 5.20b and 5.20c). The arcing path on both of the casing and the baseplate indicates that the arc started outside of the casing.

After the baseplate and the casing, the dies and their corresponding copper plates have been observed under microscope. On the die, a localised bump can be seen (in figures 5.21a and 5.21b). A corresponding grey trace is present on the corresponding copper plate (in figure 5.21c). This seems to indicate a hot spot and a current concentration area on the die. It can be due to preexisting bumps on the top of the die (like in figure 5.4b), silicone getting between the plate and the die, irregular surface or misalignment of the copper plate, or a combination of those factors.

It can be concluded in that subsection that the package, despite being effective at nominal current and nominal I^2t, presents defaults that make it potentially unsuitable for high current surge (starting at twice the nominal current, for an estimated 6.8kA^2s I^2t). For comparison, the current pulse test in the curve tracer was at a 1000A peak pulse (5 times the nominal current) but during 400µs (estimated I^2t: 400A^2s).

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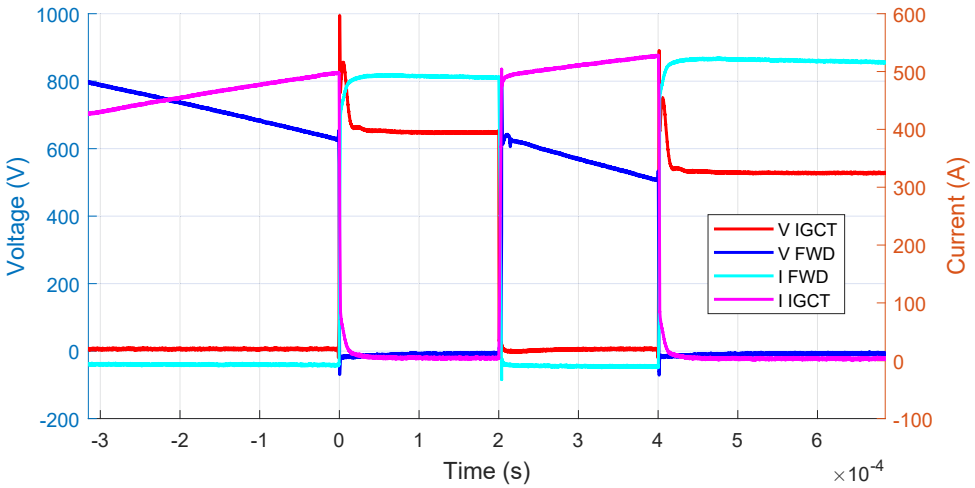
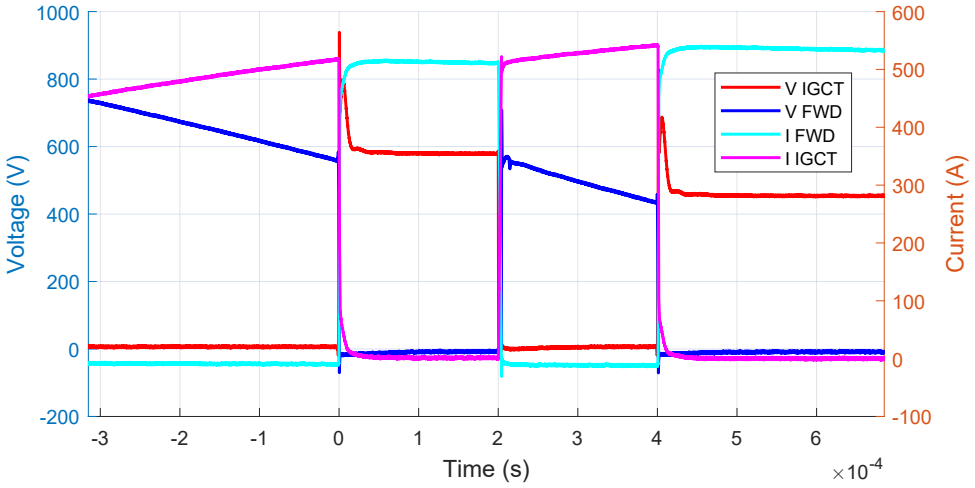


(a) Non-failing pulse.



(b) Failing pulse.

Figure 5.18: Waveforms for current surge test of the SiC PiN diode. Ambient temperature, snubber inductor 3.4µH. Total estimated duration of the double pulse: 120ms.

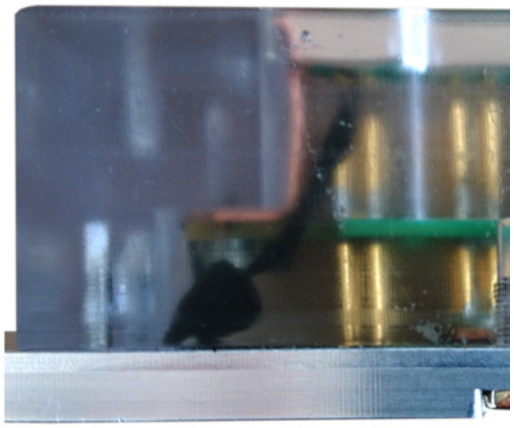


Figure 5.19: Failed package, cropped view on the burnt silicone.

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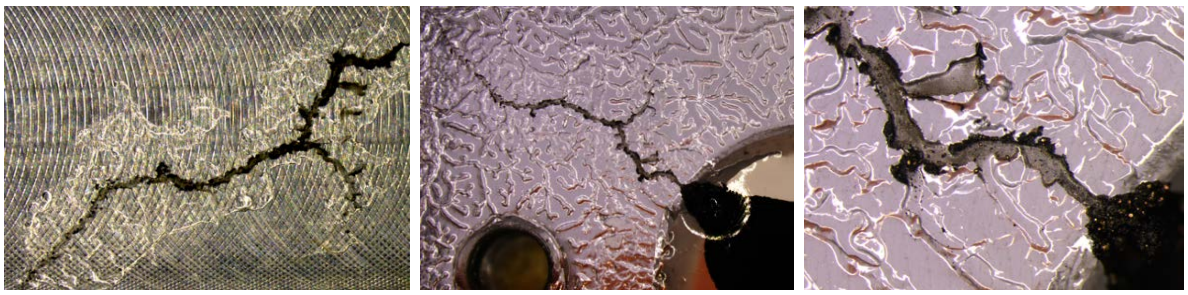
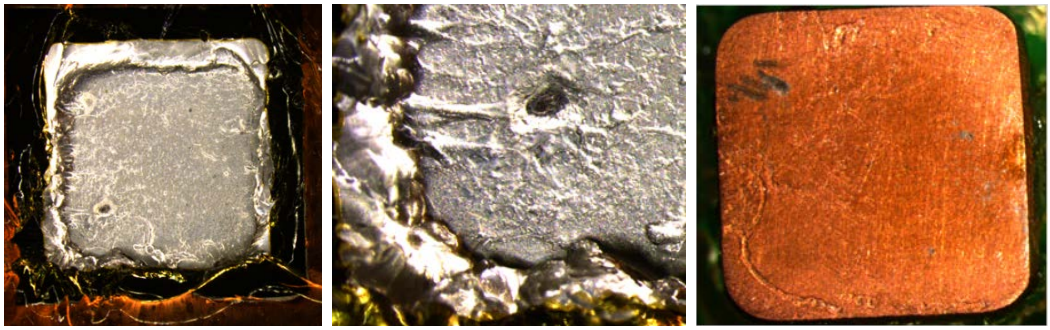


(a) Baseplate. (b) Casing. (c) Casing (zoomed).

Figure 5.20: Arcing trace on the baseplate and the casing, with visible burnt silicone.



(a) Die top view. (b) Die top view (zoomed). (c) Copper plate.

Figure 5.21: Sub-package n°01, one die and its associated copper plate after failure.

5.3.2 Double pulses with snubber

A careful approach has been preferred during the experiments whose results are described in this subsection due to the limited number of available high voltage sub-packages. This has led to pulses limited to 1400V/300A in the 3 diodes in parallel and 2400V/100A (and 2000V/150A) in the 2 diodes in parallel configuration. These limits were not due to any failure at these levels, and pulses at higher current and voltage are planned to be done shortly after this thesis.

The measuring probe locations are the same as in chapter 4 (see figure 4.16).

5.3.2.1 Typical IGCT turn-on waveforms

Typical turn-on waveforms with the silicon carbide diodes can be found in figure 5.22. The differences with the waveforms acquired with the silicon diode (see subsection 4.2.2.1), are the occurring of voltage oscillations on the diode, that do not seem exactly like snap-off. Furthermore the second part of the recovery (the B-part, as defined in subsection 4.1.3) is steep and not soft. It should also be noted that the test voltage and current levels were not pushed beyond 1400V/300A for the three diodes configuration and 2400V/150A for the two diodes configuration. The reason is a cautious approach to collect a maximum quantity of data, without breaking any sub-package. In the future, more tests will be realised with higher current and voltage levels.

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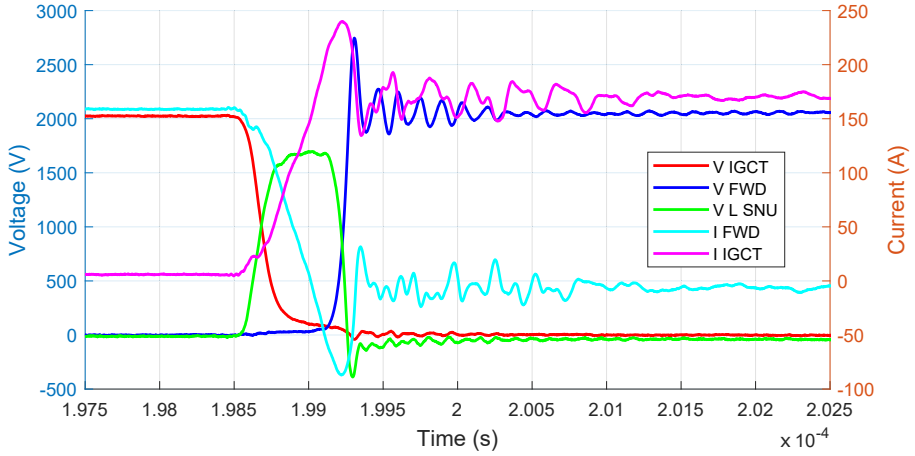
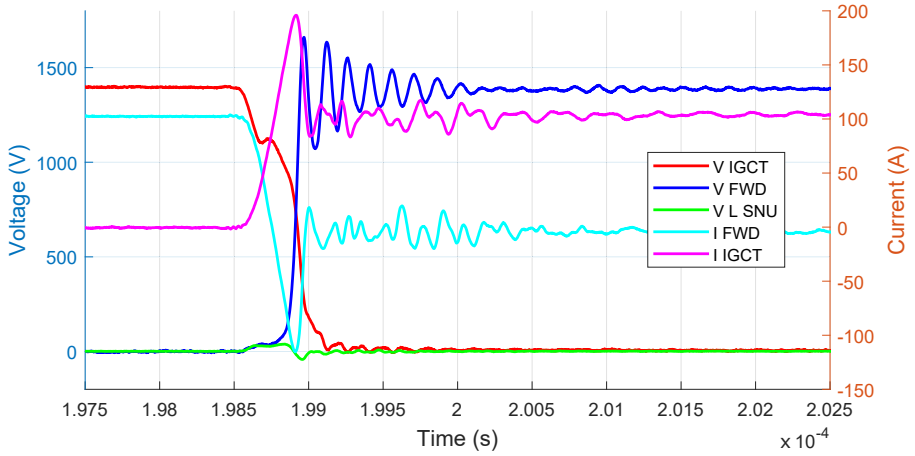


(a) 2000V, 150A, 3.4µH snubber inductor, ambient temperature.



(b) 1400V, 100A, snubber inductor: busbar position n°4, ambient temperature.

Figure 5.22: Typical waveforms at IGCT turn-on, with a two sub-packages configuration (sub-packages n°05 and n°08).

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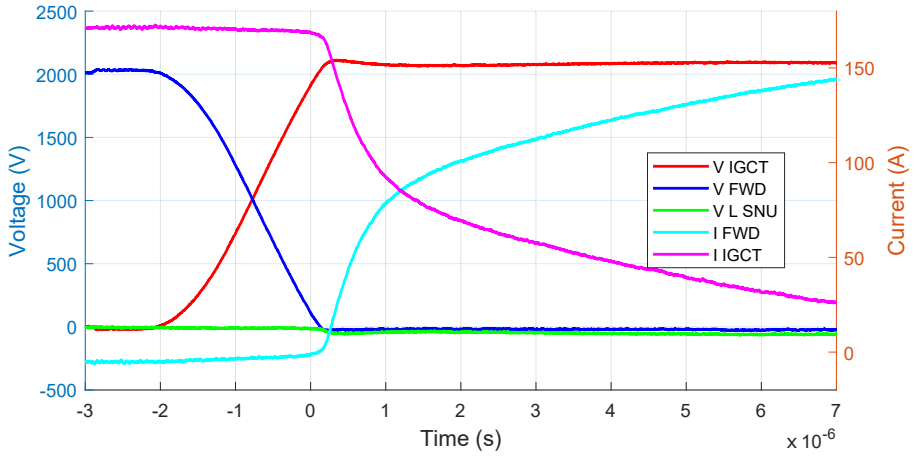
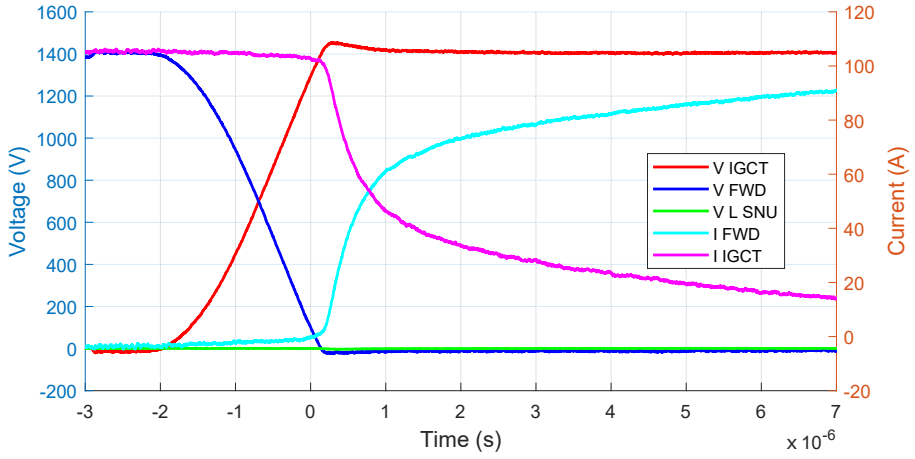


(a) 2000V, 150A, 3.4µH snubber inductor, ambient temperature.



(b) 1400V, 100A, snubber inductor: busbar position n°4, ambient temperature.

Figure 5.23: Typical waveforms at IGCT turn-off, with a two sub-packages configuration (sub-packages n°05 and n°08).

5.3.2.2 Typical turn-off waveform

Typical turn-off waveforms with the silicon carbide diodes can be found in figure 5.23. The difference with the silicon diode, explained and displayed in subsection 4.2.2.3, is that no forward recovery can be observed in the SiC diode case, unlike in the Si diode case.

5.3.2.3 Comparison with Si diode

In order to confirm that silicon carbide diodes have lower I_{rr}, E_{rr}, Q_{rr} and T_{rr} compared to silicon diodes (see subsections 1.2.1 and 5.1.1), a comparison is developed here. The comparison of the reverse recovery parameters is displayed in figure 5.24, with an on-state current of 300A, a snubber inductor value of 800nH and a temperature of 120°C. On top of the values of I_{rr}, E_{rr}, Q_{rr} and T_{rr} being lower for the SiC diode than the Si diode (which validates the theory), the increase of E_{rr} and I_{rr} with the voltage is slower for the SiC diode than the Si diode. The reverse recovery parameters comparison is similar at 25°C. It should be pointed out that the switching losses are way smaller for the SiC diode: at 1400V, 300A, 120°C and 800nH snubber

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Table 5.4: Forward voltage drop comparison between the different diodes used in this memoir.

	V_F ***(SiC diode)***	V_F ***(4.5kV diode)***	V_F ***(6.5kV diode)***
At low current	2.7V (1A)	1.5V (100A)	1.5V (50A)
At nominal current	4.75V (200A)	3.25V (1200A)	3.25V (600A)

inductance, the SiC diode displays 54.5mJ switching losses while the 4.5kV diode displays 752mJ (more than 13 times lower).

For conduction losses, a quick comparison of the different values of forward voltage drop is available in table 5.4, for one sub-package of each diode model. The SiC diode displays more conduction losses, as it could be expected for a SiC PiN diode (see subsection 5.1.1). This is a drawback that could question the use of these SiC diodes in MMCs. It should be noted though that, these diodes were designed for a 10kV breakdown voltage. The same design for a 5kV breakdown voltage would have a lower on-state resistance and therefore lower forward voltage drop for the same current.

5.3.2.4 Influence of operational parameters

In this subsection the effects of the operational parameters on the reverse recovery (voltage, current, temperature and snubber inductor) are studied. It aims to check if the SiC diode behaves in accordance with the theory developed in section 4.1.

Voltage and Current The reverse recovery parameters depending on voltage and current at 120°C and with a 800nH snubber inductors are displayed in figure 5.25. As presented in sections 4.1 and 4.2), higher voltage causes higher I_{rr}, E_{rr} and Q_{rr}, and lower T_{rr}, while higher current causes higher I_{rr}, E_{rr}, Q_{rr} and T_{rr}. The maximal values for I_{rr}, E_{rr}, Q_{rr} and T_{rr} are 240A, 60mJ, 0.54µs and 68µC respectively, with a 800nH snubber inductor at 120°C.

Temperature The reverse recovery parameters depending on temperature and current at 1400V and with a 800nH snubber inductors are displayed in figure 5.26. As expected a higher temperature causes higher I_{rr}, E_{rr}, Q_{rr} and T_{rr}. The small difference between values at 60°C and 90°C is observed for all snubber inductor values, and no explanation has been found.

Snubber inductance The same parameters, this time depending on snubber inductor value and current for 1400V and 120°C are displayed in figure 5.27. As expected a higher snubber inductor value causes higher T_{rr} and lower I_{rr}, E_{rr}, Q_{rr}.

Overvoltage As it can be seen in figure 5.22, there is a noticeable overvoltage across the diode during its turn-off. In figure 5.28 are displayed different parameters that could influence the overvoltage across the diode which help determining if the behaviour of the diode recovery is a snap-off behaviour or not, like described in section 4.1.4. From figure 5.28a it can be analysed that the overvoltage is not correlated with the current (no or low increase of overvoltage with

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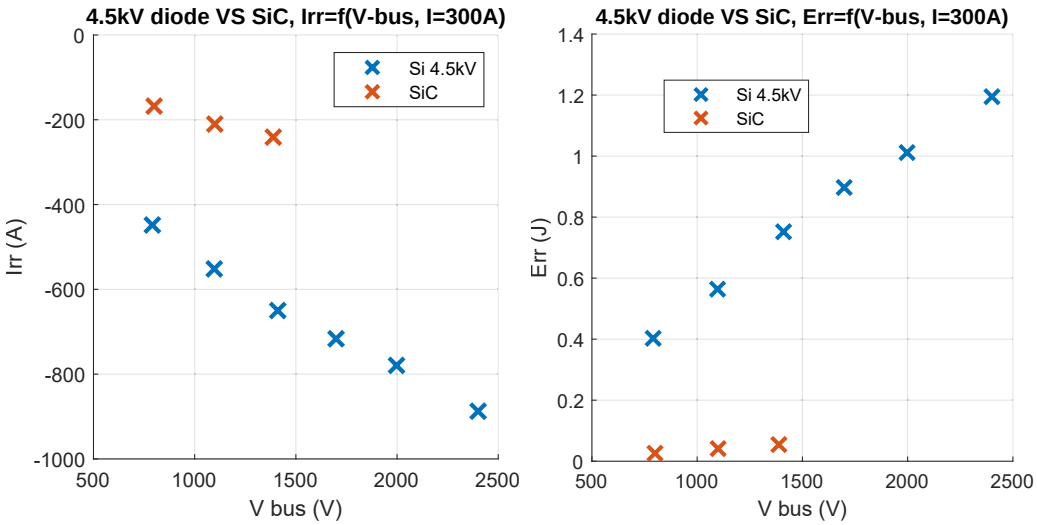

(a) I_{rr} (b) E_{rr}

(c) T_{rr} (d) Q_{rr}

Figure 5.24: Reverse recovery parameters comparison between the 4.5kV diode ABB diode and the SiC diode (configuration 3 sub-packages), I_{pulse}=300A, snubber inductor: 800nH, temperature: 120°C.

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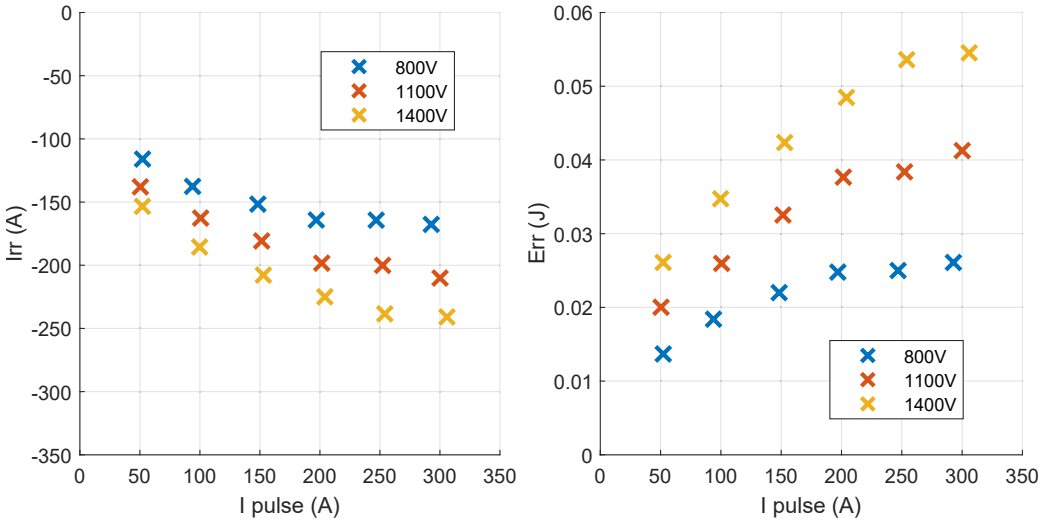
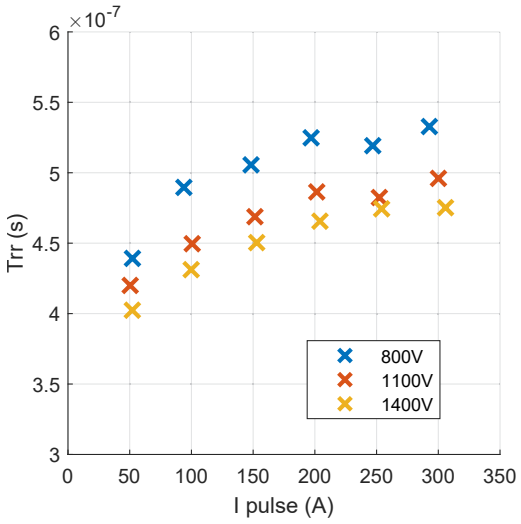
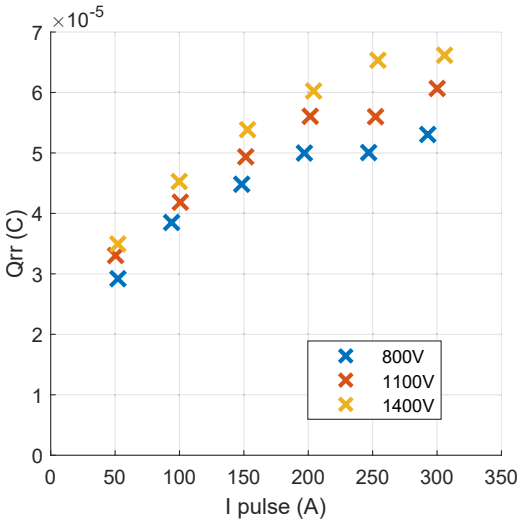


(a) I_{rr}

(b) E_{rr}



(c) T_{rr}



(d) Q_{rr}

Figure 5.25: Reverse recovery parameters with the SiC diode (configuration 3 sub-packages), V_{bus}=800V, 1100V, 1400V, snubber inductor: 800nH, temperature: 120°C.

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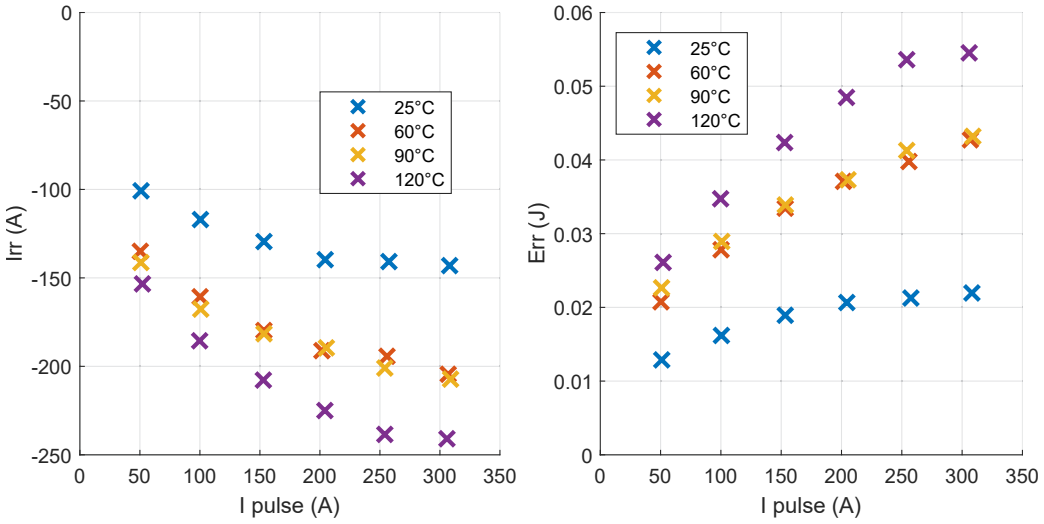
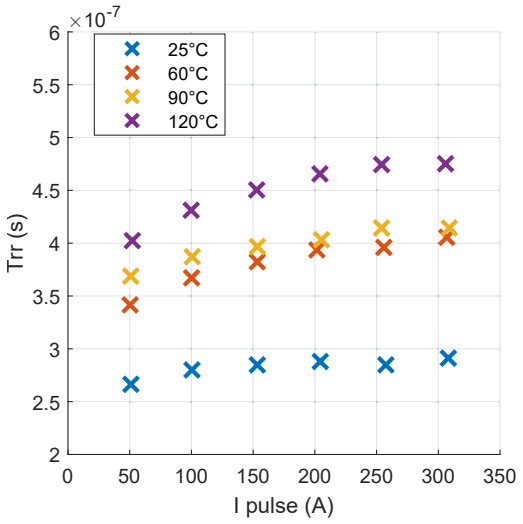
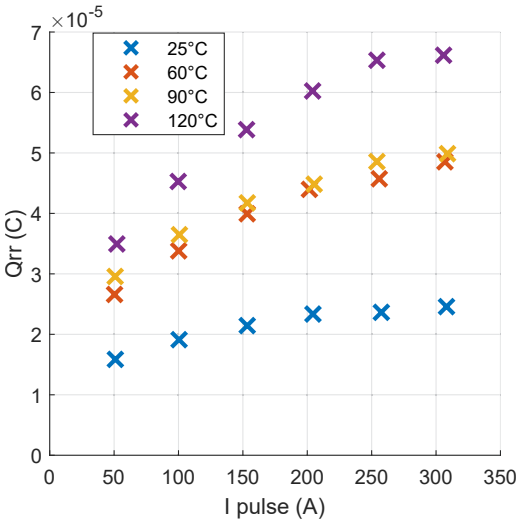


(a) I_{rr}

(b) E_{rr}



(c) T_{rr}



(d) Q_{rr}

Figure 5.26: Reverse recovery parameters for the SiC diode (3 diodes in //), V_{bus}=1400V, snubber inductor: 800nH. Temperature variation with values: 25°C, 60°C, 90°C, 120°C.

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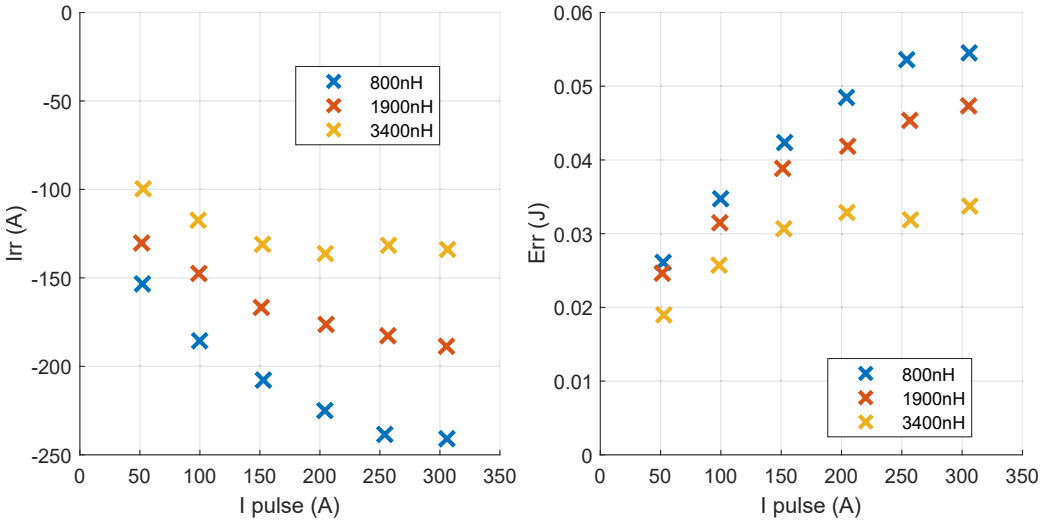
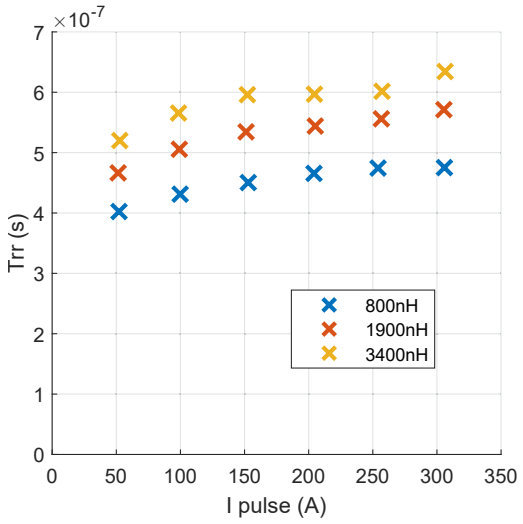
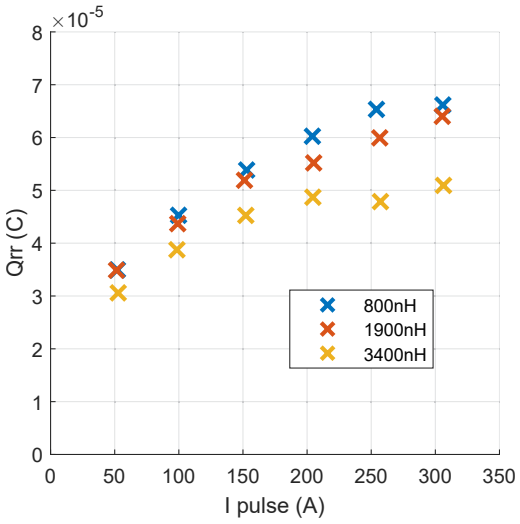


(a) I_{rr}

(b) E_{rr}



(c) T_{rr}



(d) Q_{rr}

Figure 5.27: Reverse recovery parameters for the SiC diode (3 diodes in //), V_{bus}=1400V, temperature: 120°C. Snubber inductance variation with values: 800nH, 1.94µH, 3.4µH.

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the increase of current), but highly correlated with the voltage (around 750V of overvoltage for 800V pulses and 1100V of overvoltage for 1400V pulses, in a three parallel sub-package configuration). From figure 5.28b it can be analysed that an increase in temperature leads to an increase in overvoltage and in figure 5.28c it can be seen that a decrease in snubber inductor value leads to an increase in overvoltage.

These combined influences of operational parameters on the diode overvoltage, show that the reverse recovery of the SiC diode does not display a snap-off behaviour as defined in section 4.1.4. For a snap-off behaviour, a lower current would lead to a higher overvoltage (not the case here), a higher temperature would lead to lower overvoltage (not the case here) and snubber inductor value has no effect on the overvoltage level (not the case here). Therefore it shows that **high di/dt during the second part of the recovery like with this SiC diode, called snappy in [67], is not necessarily the same as a snap-off behaviour, described in chapter 4**.

The hypothesis retained in this thesis about the diode overvoltage is that the overvoltage is due to internal dynamics inside the diode, with capacitive effects that seem to dominate here. The internal behaviour could explain the linear relation between the di/dt during the A-part and the di/dt during the B-part of the reverse recovery, as shown in figure 5.28d. It shows a narrowing behaviour of the reverse recovery: when the di/dt of the A-part increases, the di/dt of the B-part increases too. This hypothesis could be developed and analysed after this thesis with semiconductor simulations.

As expected, the overvoltage has a linear relation with the di/dt of the B-part, as it can be seen in figure 5.28e.

5.3.2.5 A Focus on diode overvoltage at high di/dt

Snubberless operation will be described further in section 5.3.3. This subsection here will focus on high di/dt behaviour of the combination of IGCT and SiC diode. There is indeed a specific behaviour that was not present with the silicon diode. It can be seen in figure 5.29a, unlike in figure 5.22a for example, that the first diode overvoltage spike is lower than the second overvoltage spike (see 4.16 for circuit diagram and probes locations). Normally, the first diode overvoltage spike is the highest during the IGCT turn-on and it corresponds to the maximum di/dt of the B-part of the reverse recovery (see subsection 4.1.3). The hypothesis here is that the IGCT takes up a part of the overvoltage because it has not reached a low voltage level. It can be seen in figure 5.29b, where the sum of the diode and IGCT voltages has been plotted. The sum of the voltages displays the expected overvoltage behaviour, with a first spike higher than the second one. This phenomenon, where the diode starts blocking voltage before the IGCT is fully on, is due to the quick reverse recovery duration of the silicon carbide diode (0.25µs) which is in the same range as the voltage drop duration of the IGCT turn-on.

In figure 5.30a, it can be seen that the linear relation between diode overvoltage and V_{bus} exists for high snubber inductor values (in blue, 3.4µH) but disappears for low snubber inductor values (yellow, busbar position 4, 100nH estimated). But when the sum of the voltages is considered, like in figure 5.30b, this linear relation can be found.

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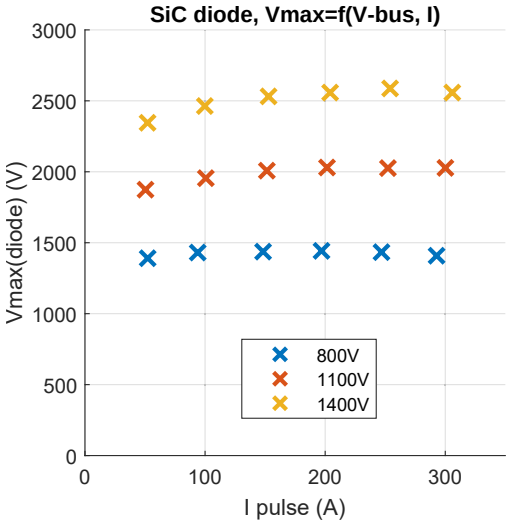
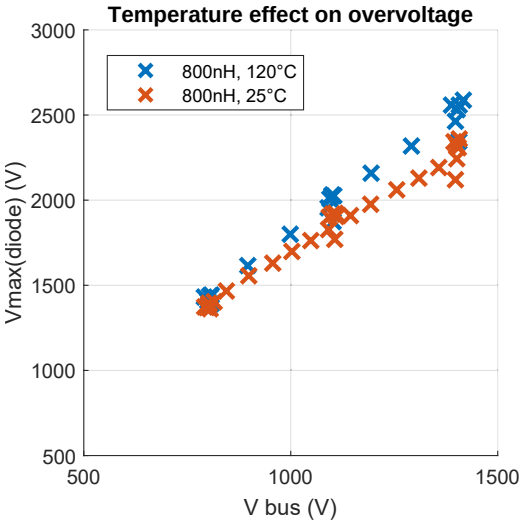
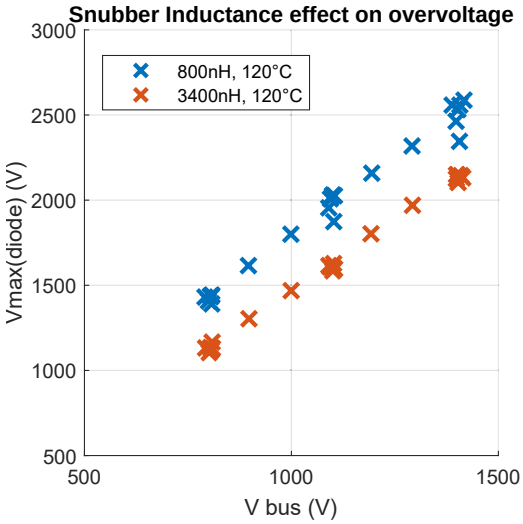


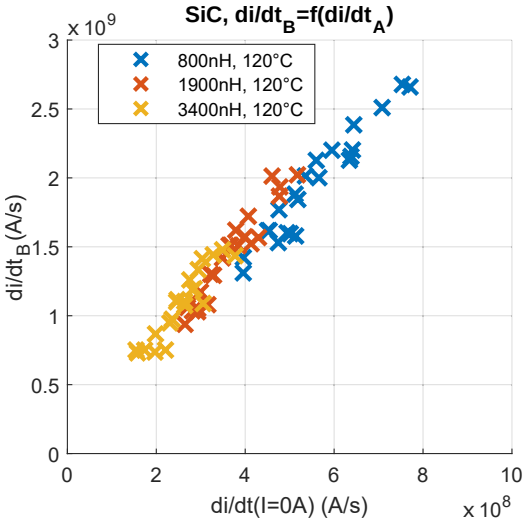
(a) V_{bus} and I_{pulse} (120°C, 800nH).



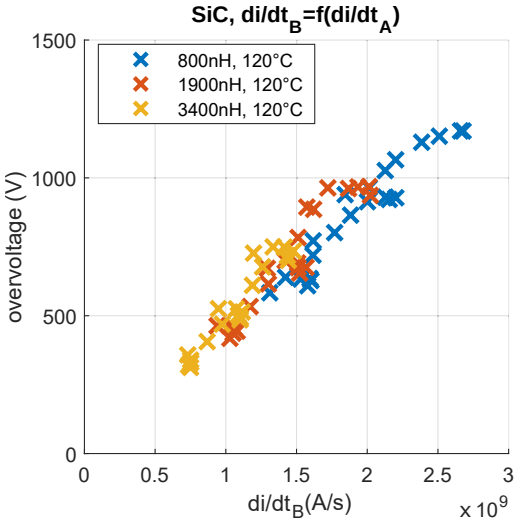
(b) Temperature.



(c) Snubber inductor Value.



(d) di/dt_B function of di/dt_A.



(e) Overvoltage function of di/dt_A.

Figure 5.28: Diode maximum voltage analysis for the SiC diode (3 diodes in //), examining the effect of voltage, current, temperature, snubber inductor value and di/dt at 0A.

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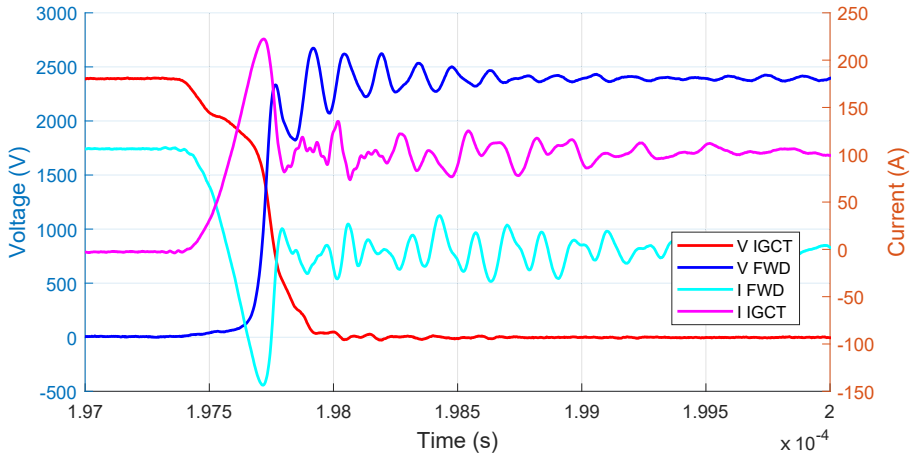
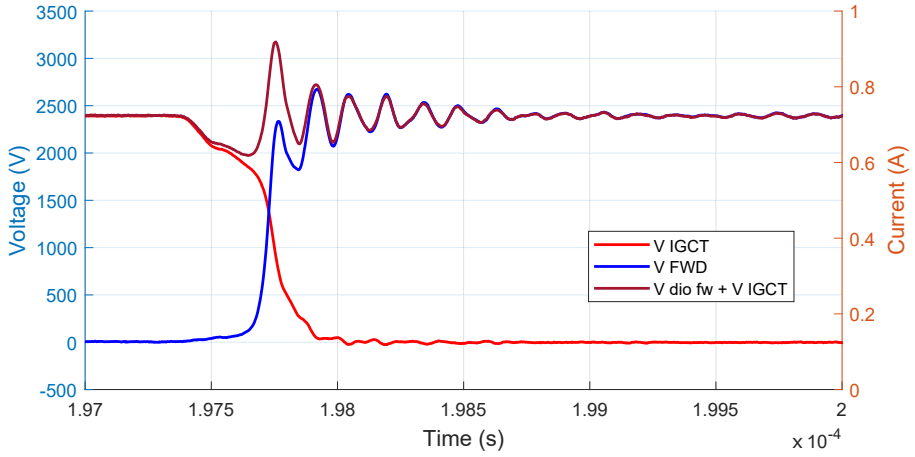
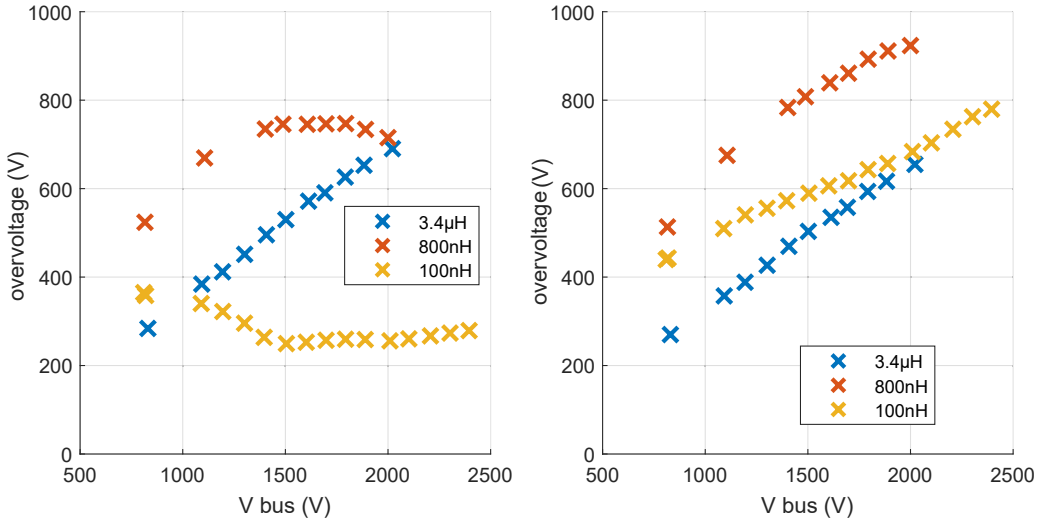


(a) 2400V, 100A, busbar position 4, ambient temperature.



(b) 2400V, 100A, busbar position 4, ambient temperature, with voltage sum.

Figure 5.29: Waveforms at IGCT turn-on at high di/dt, 2400V, 100A, with a two sub-packages configuration (sub-packages n°05 and n°08).



(a) Diode only.

(b) Diode + IGCT.

Figure 5.30: Overvoltage depending on V_{bus}, for the diode only (left) and the voltage sum (IGCT + diode) waveform. SiC diode configuration: 2 in //, RCD clamp present. Current of 100A, ambient temperature.

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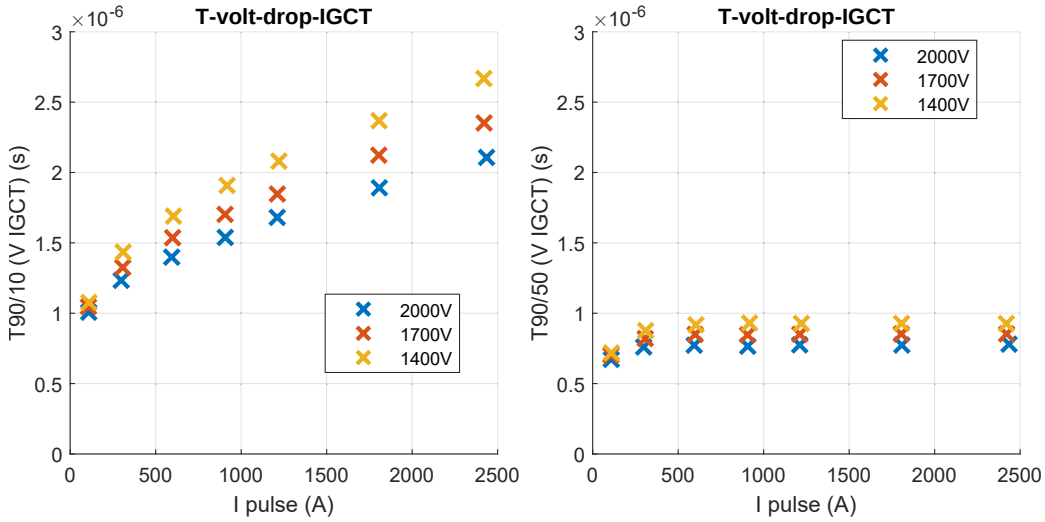

(a) 90% to 10% drop.

(b) 90% to 50% drop.

Figure 5.31: Voltage-drop duration across the IGCT depending on on-state current, with the 4.5kV ABB diode, at 120°C and a snubber inductor of 100nH (busbar position 4 and RCD clamp present).

Voltage-drop of IGCT during turn-on The behaviour described previously (**the diode being fast enough to start blocking voltage before the IGCT stops blocking voltage, limiting the overvoltage across the diode at high di/dt**) can be found up to 150A and 2400V (because tests were not pursued at higher voltage/current). The following interrogation is on the continuation of the phenomenon at higher current. This can be partially answered by analysing the voltage-drop duration of the IGCT with the silicon diode used in chapter 4, at high current. Figures 5.31a and 5.31b present the voltage-drop across the IGCT duration between 90%-10% of the bus voltage and between 90%-50% of the bus voltage respectively, for the 4.5kV silicon diode of chapter 4, at 120°C with a snubber inductance value of 800nH.

In figure 5.31a, it can be seen that this duration increases with the current, but this is not the case in figure 5.31b. This can be explained by the position of the voltage probes a little bit distant from the IGCT (on the busbars, on the side on the heatsink as it can be seen in figure 4.16), displaying an inductive effect. From these two figures it can be concluded that, even if the voltage falling time across the IGCT increases with the current, the time it takes to halve the voltage across the IGCT remains stable.

In conclusion, because the voltage falls rapidly (<1µs) in the first stage of the IGCT turn-on regardless of the current level, the same voltage-sharing between IGCT and SiC diodes can be expected. This would mean that the reduction of overvoltage across the SiC diode should happen for any current level.

5.3.3 Without snubber and RCD clamp

Snubberless operation had been successful in a two sub-packages diodes in a parallel configuration up to 2400V/100A and 2000V/150A. Waveforms of snubberless configuration are available in figure 5.33 and correspond to the same level of current (100A), voltage (2400V), temperature

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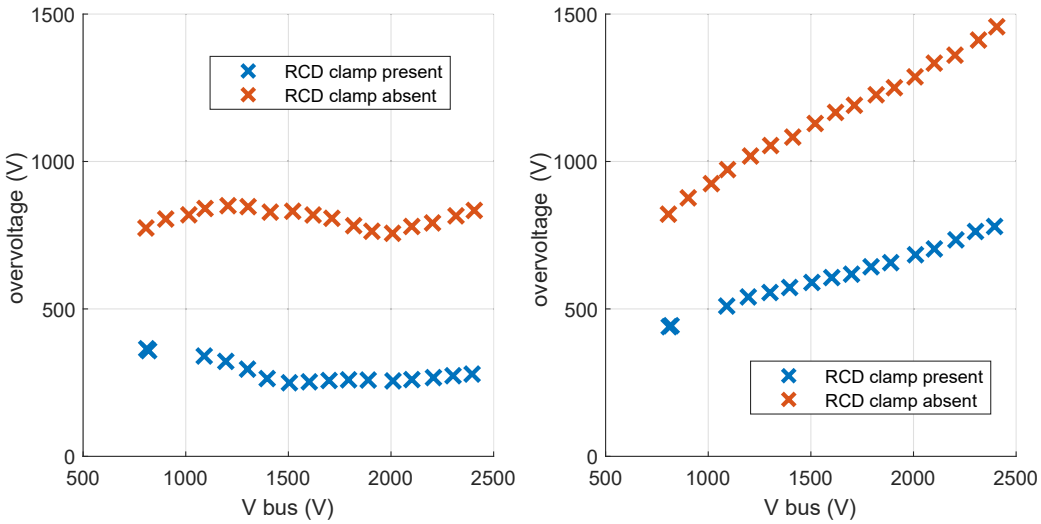

(a) Diode only.

(b) Diode + IGCT.

Figure 5.32: Overvoltage depending on V_{bus}, for the diode only (left) and the voltage sum (IGCT + diode) waveform. Each color corresponds to a setup: blue (RCD clamp present), orange (RCD clamp absent). SiC diode configuration: 2 in //. Current of 100A, ambient temperature, snubber inductance: 100nH.

(25°C) and busbar position (n°4) as in figure 5.29. Figure 5.32a shows the overvoltage across the diode and figure 5.32b shows the overvoltage on the sum of the IGCT and diode voltages, with the inductor busbar being in position n°4. First, as in section 4.2.6, the overvoltage across the diode increases in a clampless configuration compared to a configuration with an RCD clamp. From all these figures, it can also be analysed that in a snubberless configuration, the first peak reduction phenomenon still appears: it can be seen on the pulse waveforms (see figure 5.33b), but also by the difference of overvoltage between figure 5.32a and 5.32b (for the orange points). In the end, the overvoltage across the diode never surpassed 1kV.

It has been determined in section 5.3.2.4 that the reverse recovery of the SiC diode does not display any snap-off. Therefore, the phenomenon seems only due to the standard mechanism of stray inductance provoking this overvoltage. Indeed, unclamping the stray inductance by removing the RCD-part increased the stray inductance. The same conclusion on overvoltage as in section 4.2.6 applies here: it seems that the overvoltage could be diminished by reducing the stray inductance.

The operation of this diode in an MMC snubberless configuration appears to be possible. Unlike the silicon diode, whose snap-off behaviour puts it at risk for a wide range of current and voltage levels (and in particular at high voltage and low current levels), the SiC diode can operate safely up to decent voltage levels. If the overvoltage across the diode is still limited at higher current and voltage, and if the stray inductance is reduced, pulses up to 4kV with overvoltage lower than 1kV are imaginable, with currents levels up to 600A (nominal current). 600A would represent a low level for MMC operation (where a current level of 1kA can be expected) but would be demonstrative. Rather than projections, only more pulses at higher current and voltage would permit to assess completely this configuration and this diode for normal MMC operation.

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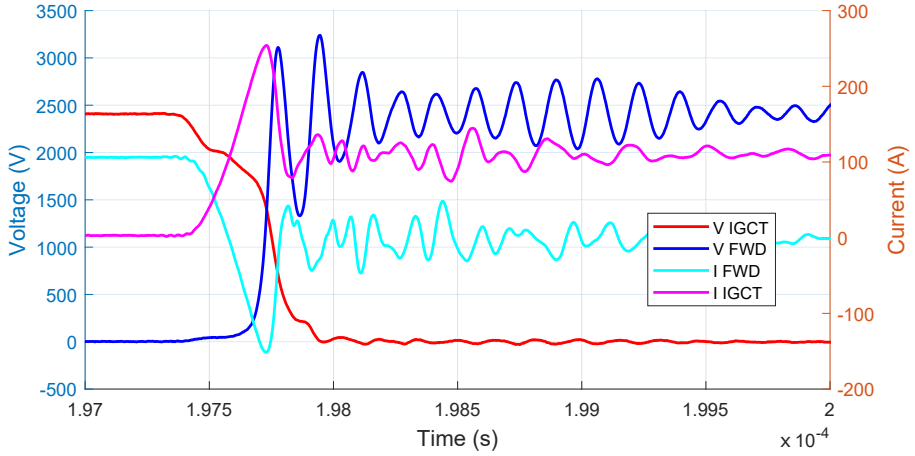
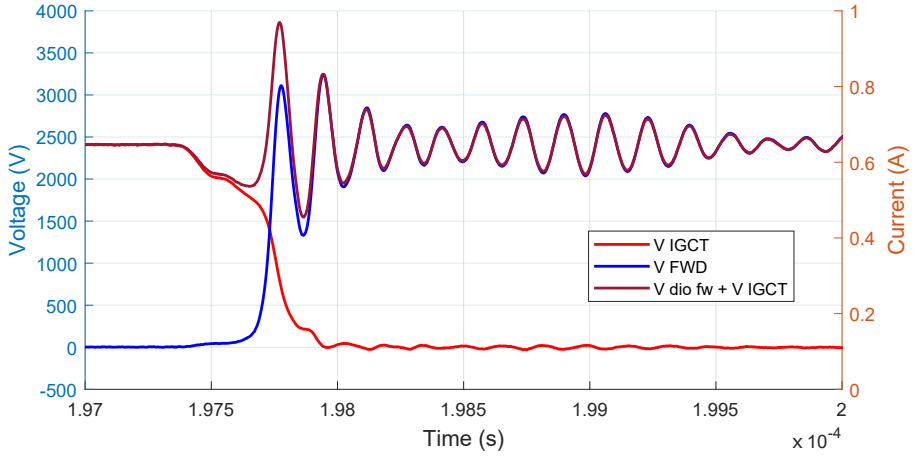


(a) 2400V, 100A, busbar position 4, ambient temperature.



(b) 2400V, 100A, busbar position 4, ambient temperature, with voltage sum.

Figure 5.33: Waveforms at IGCT turn-on at high di/dt, in a snubberless configuration, 2400V, 100A, with a two sub-packages configuration (sub-packages n°05 and n°08).

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5.4 Conclusion on the packaging and the use of HV SiC diodes with IGCTs

In this chapter, an original and specific packaging has been designed, with the aim to test SiC PiN diodes at high voltage (more than 5kV for some sub-packages) and high current levels (200A per sub-package). These diode sub-packages have been successfully tested in the test setup designed in chapter 3 and used in chapter 4, displaying excellent reverse recovery parameters but significant overvoltages.

Indeed, the SiC diode has shown a better switching behaviour than the silicon diode: less switching losses (54.5mJ compared to 752mJ at 1400V, 300A, 120°C and with the 800nH snubber inductor), lower reverse recovery duration (0.48µs compared to 3.5µ for the same levels). The overvoltage of the silicon carbide diode is high but it could be reduced by decreasing the stray inductance of the circuit, as discussed in section 5.3.3. This is even more important considering that no failure linked to a too fast reverse recovery has been identified yet, and therefore higher di/dt values have to be explored, with lower stray inductance and higher voltage levels. As shown in section 5.3.1 the current level that can be reached safely will be limited, with an indicated value of 2.5 times the nominal current (the nominal current being 200A for a sub-package). As a reminder, a careful approach and a lack of time led to reduced range of voltage and current test values, but no contraindication for higher levels of current and voltage (up to nominal ratings at least) has been found.

An important conclusion must also be drawn from the results of this chapter: a quick second part of reverse recovery (B-part), like in this chapter, despite being called snappy in the literature, is not the same as a snap-off behaviour, like in chapter 4.

With sufficiently high di/dt values, a specific phenomenon appears with the SiC diode: the SiC diode, being very fast (in the range of 0.25-0.5µs), starts blocking voltage before the IGCT is fully on. This has limited the overvoltage across the diode as discussed in section 5.3.2.5.

Snubberless operation has been successful (no failure) at 2000V/150A and 2400V/100A in a two-diodes parallel configuration. As discussed in section 5.3.3, no limiting phenomenon (like snap-off for the Si diode) has been identified. Therefore, safe operation up to nominal ratings (4000V, 600A) can be envisaged, which would be coherent with normal ratings of MMC. In the future, much higher voltage and current levels, with lower stray inductance have to be tested in this setup to conclude fully on snubberless/clampless operation of the IGCT in an HVDC MMC submodule with a SiC diode. Also SiC Schottky diodes, not displaying reverse recovery, could be used in series to reach a sufficient voltage, with the IGCT at high di/dt.

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General Conclusion

This manuscript summarizes our investigations on the use of the IGCT for the MMC HVDC application case. A review on the technology of the MMC submodule has been proposed in chapter 1. It has shown that although the installed HVDC MMCs currently use IGBTs, a possible evolution was to use IGCTs for both reducing losses and simplifying the submodule architecture.

In chapter 2, we focused on this device. The interest of the IGCT has been verified by comparing IGCTs and IGBTs, using literature, simulation, and newly created figures-of-merit. These figures-of-merits offer a way to generalize the comparison of devices (regardless of their type, IGBTs or IGCTs) in the MMC case. This is different from the losses studies reported in the literature, where only one control method, one converter, one losses model, and one device per type are usually investigated. These figures of merit offer a very simple way to compare devices using only parameters available in their datasheet, so that the best device can be selected in a straightforward manner.

The IGCT has proven to display lower losses in the HVDC MMC case, which is consistent with the findings reported in the literature. Interestingly, these devices offer both lower conduction and switching losses compared to IGBTs. In addition, its robustness and its press-pack case open the possibility (not investigated experimentally in this study) to operate without additional fail-safe mechanisms (crow-bar thyristor and/or vacuum switch). However, one limiting aspect that has been identified is the need for a turn-on snubber.

Indeed, in the submodule structure, a diode is associated with the IGCT. The switching speed of the IGCT is very fast and cannot be controlled through its gate. Without any limiting circuit (the turn-on snubber) the associated diode would endure very high di/dt (several kA/µs up to tens of kA/µs) when turning-off, a condition it cannot sustain. Therefore a turn-on snubber is used, comprised of an inductor which slows down the current transient, and an RCD (resistor-capacitor-diode) clamp absorbing the energy stored in the snubber inductor. Although it is an auxiliary circuit used only during switching, the snubber ends up being bulky and costly, especially considering high voltage IGCTs (6.5kV voltage rating, 4kV nominal DC bus voltage) associated with slow diodes (1kA/µs during commutation). It adds losses, volume, cost and complexity of the submodule (with potential reliability concerns because more components are used in the submodule).

As a result of this, we decided to verify if it was possible to reduce or even to remove this snubber by using faster diodes. This has been conducted experimentally. A specific double pulse test setup has been designed and built, integrating as many constraints of a full-size MMC submodule (dimensions of the busbars, cooling system, etc.), to help visualise what such

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a submodule would be. To specifically study the snubber reduction, different snubber inductors have been manufactured (from 800nH to 3.4µH). For lower values, the busbars form a adjustable inductor with a movable middle piece, reaching a value as low as 150nH (resulting in a total stray inductance of 450nH).

6.5kV/3.8kA IGCTs (press-pack) and silicon diodes in a plastic-module (models: 4.5kV/2 × 1200A and 2 × 6.5kA/µs ; 6.5kV/2 × 600A and 2 × 4kA/µs) have been investigated first, and compared to a more standard, press-pack diode designed to operate together with IGCTs. The first part of the double-pulse tests, described in chapter 4, has shown two limitings phenomena associated with the recovery of the silicon diodes. The first one is the dynamic avalanche that happens at high di/dt at the end of the recovery, at a lower voltage than the rated breakdown voltage of the diode. During reverse recovery, dynamic avalanche happens because of stored charges in the diode while voltage is rising. The second limiting phenomenon is the snap-off. It is a brisk stop in the current at the end of the recovery. This strong di/dt at the end of the recovery has been measured at values as high as 10 to 15kA/µs and has led to overvoltages up to several kilo-volts across the diode. Both of these phenomena can be severe, as they have led to destructions in the experimental setup.

In particular, snap off has been found to occur over a large part of the I/V domain of operation for the fast diodes, especially at room temperature. While snap-off is not a destructive mechanism in itself, the overvoltages it generates can exceed the capability of the diodes, resulting in their failure. As a result, the experimental I/V domain has been limited to ensure the overvoltages would remain lower than the breakdown voltage of the diodes.

Despite these phenomena, it has been possible to test the 4.5kV PM diode in a snubberless configuration (no inductor, no RCD) up to 2400V/1800A at 120°C. Nevertheless, significant snap-off happens at levels of current and voltage that can be encountered during MMC normal operation (1700V/600A at ambient temperature, for the 4.5kV diode). Even if further improvement to the test setup may help reducing the severity of the snap-off phenomenon (by reducing the stray inductance of the structure, currently 450nH), it will probably still remain a strong limiting factor, especially for the low current values.

To overcome the limits of the silicon diodes, it has been chosen to test the IGCT with some silicon carbide (SiC) diodes. In chapter 5, SiC PiN diode dies have been packaged and tested with the IGCT. A specific packaging has been designed for work, considering specific constraints associated with these dies and the test setup. The approach was to build so-called "sub-packages" to improve manufacturing yield and mimic the footprint of the Si diodes. 8 sub-package containing 4 dies each have been built in-house. They can reach up to 200A in nominal current (600A for a complete assembly of 3 sub-packages, with a large surge current capability), and half of them can withstand more than 5kV. During the tests, the SiC diode displayed excellent reverse recovery characteristics. For example, their switching losses (54.5mJ) are much lower than those of the Si diodes (752mJ for the 4.5kV diode at 1400V, 300A, 120°C, and 800nH snubber inductance). They also exhibit much shorter reverse recovery duration (0.48µs compared to 3.5µ for the same levels).

The SiC diode has been tested successfully with the IGCT in a snubberless configuration up to 2400V/100A and 2000V/150A in a 2-parallel sub-packages configuration. So far, the tests have been limited to low current and voltage values compared to the nominal values of the diodes because of the limited number of sub-packages. No limiting phenomenon has been

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identified during the tests, and therefore tests at higher voltage and current will be realised in the near future. Because the SiC diodes are much faster, it has been shown that they start turning off earlier, resulting in an effect of voltage sharing between the IGCT and the diode. As a result, despite the occurrence of a high di/dt, the overvoltage across the diode remains limited. This, together with the absence of snap-off phenomenon can potentially allow snuberless operation.

In conclusion, this study confirms the potential of IGCTs in the case of HVDC MMCs, as a replacement for IGBTs. Moreover, snuberless operation seems possible, providing SiC diodes are used instead of Si diodes. Indeed, fast Si diodes exhibit a snap-off phenomenon which strongly limits the operating range of the switches. On the other hand, SiC diodes display excellent reverse recovery characteristics and are natural candidates for IGCT based MMC submodule without turn-on snubber.

Nevertheless, some more investigations are needed to definitely conclude on the snubberless operation. In particular, the following should be studied:

- First, test the current SiC diodes at higher current and voltage, to ensure they can operate over the entire I/V domain in a snubberless configuration. In our case, PiN diodes have been used because they were available, but "Schottky" diodes, which offer even better switching behaviour (and are available up to 6.5kV or can be connected in series) may be tested too.
- The current test setup has a relatively high stray inductance (450nH), which limited some of the investigations. A better design should help reduce this stray inductance so as to reduce switching losses and evaluate whether snuberless operation remains possible.
- So far, switching speed has been limited by the diodes only, which is why we have focused on them in this study. As faster switching events are allowed by SiC diodes in a snuberless configuration, it is important to ensure no excessive burden is transferred to the IGCTs. Although double pulse tests revealed no issue, a more thorough reliability study seems necessary to ensure IGCTs can operate over a long time under di/dt. This may be conducted by semiconductor simulation and/or testing.
- Finally, we only performed experimental tests on the diodes. A better understanding of their limitations would require a more extensive analysis, probably based on semiconductor physics simulation, so as to identify their theoretical limits.

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Arthur Boutry

Résumé en Français de la Thèse 'Theoretical and experimental evaluation of the Integrated gatecommutated thyristor (IGCT) as a switch for Modular Multi Level Converters (MMC)'

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Chapitre I : Revue de la technologie des MMCs et des sous-modules

I.1 Le convertisseur modulaire multiniveaux (MMC)

Dans ce chapitre, la technologie du sous-module MMC est évaluée. Le convertisseur modulaire multiniveaux (MMC) est un convertisseur de type source de tension (VSC) développé et utilisé pour les applications de courant continu à moyenne ou haute tension (MVDC ou HVDC). Il s'agit d'un convertisseur AC/DC réversible. Un type simple de VSC est le convertisseur à deux niveaux. Sa compréhension permet d'identifier les avantages du convertisseur multiniveaux modulaire.

Le convertisseur à deux niveaux est présenté à la figure I.1 (schéma électrique et formes d'ondes). Étant donné que seuls deux niveaux de tension peuvent être appliqués à chaque borne du côté AC, la conversion AC/DC repose sur l'utilisation d'interrupteurs à haute fréquence. La conversion AC/DC repose sur des méthodes de contrôle comme la méthode de modulation de largeur d'impulsion - en utilisant un signal de référence sinusoïdal, et le filtrage des hautes fréquences. Cette stratégie présente des inconvénients majeurs : une fréquence de commutation élevée implique de grandes pertes en commutation et nécessite un filtrage pour éliminer les harmoniques de haute fréquence. Parce que les composants semi-conducteurs de puissance ont une tension nominale limitée - jusqu'à 10kV, il est nécessaire d'en connecter un grand nombre en série pour soutenir la tension MVDC ou HVDC. Cette connexion est complexe (afin d'assurer une tension équilibrée entre les interrupteurs), tout comme la commutation simultanée de tous les interrupteurs.

Le convertisseur modulaire multiniveaux (fig. I.2a) est basé sur des sous-modules, son unité élémentaire. Formé de semi-conducteurs de puissance (interrupteurs et diodes) et d'un condensateur, un sous-module peut être considéré comme une petite source de tension, qui peut être insérée ou non (selon l'état d'insertion du sous-module et le signe du courant traversant le bras du MMC). Cette structure permet de fonctionner comme un redresseur ou un onduleur. Le nombre de sous-modules peut être élevé - jusqu'à des centaines de sous-modules, ce qui permet de générer une bonne forme d'onde sinusoïdale (voir figure I.2b), même sans filtrage. La topologie MMC est également facilement modulable : pour un sous-module donné, différents MMC peuvent être construits (un MMC 100 kV et un MMC 400 kV peuvent être construits avec le même sous-module). De par le fonctionnement du convertisseur, la fréquence de commutation de chaque sous-module individuel est bien inférieure à celle d'un convertisseur à deux niveaux, et les pertes de commutation sont donc également plus faibles. La fréquence de commutation

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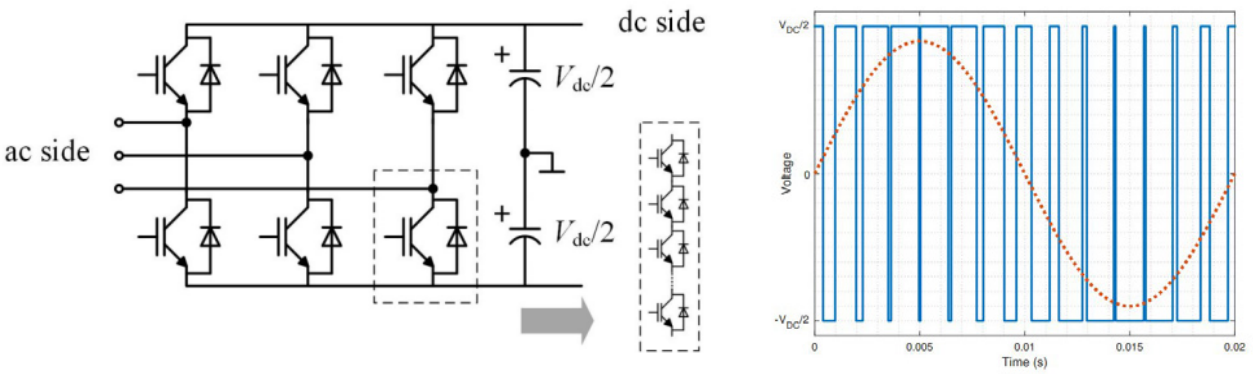

(a) Schéma électrique [13].

(b) Formes d'ondes de tension typiques d'un convertisseur 2-niveaux [8].

Figure I.1: Schéma électrique et formes d'onde en tension typiques d'un convertisseur 2-niveaux.

d'un sous-module est généralement comprise entre 100 et 300 Hz.

I.2 Le sous-module et ses composants

Les différentes parties d'un sous-module typique, leur rôle et leurs caractéristiques sont décrits ci-dessous. Le tableau I.1 et la figure I.3 offrent un aperçu rapide de ces parties. Le module de puissance, qui est le point central de cette thèse, abrite les interrupteurs de puissance avec leurs diodes antiparallèles. Ce module de puissance est la principale source de pertes dans le MMC et l'une des pièces les plus coûteuses. L'interrupteur le plus utilisé pour les MMC HVDC est l'IGBT en silicium (Si), en raison de la combinaison de sa tenue en haute tension et de son courant nominal élevé, ainsi que de la facilité de son contrôle. Les MOSFET en carbure de silicium (SiC) sont utilisés dans les MMC à faible courant (tels que les MMC MVDC). L'IGCT, un thyristor, est étudié comme une bonne alternative à l'IGBT dans les MMC HVDC en raison de ses faibles pertes et sera étudié en détail dans ce mémoire de thèse.

I.3 Interrupteurs de puissance utlisés dans les sous-modules

Ici sont présentés rapidement les deux principaux interrupteurs étudiés dans cette thèse et utilisés dans les MMC: l'IGCT et l'IGBT.

Thyristor de type IGCT ('Integrated Gate-Commutated Thyristor')

L'IGCT est une évolution du GTO ('Gate Turn-Off Thyristor'), un thyristor pouvant se contrôler à la fermeture et à l'ouverture avec des impulsions de courant. Deux améliorations sont à la base de l'IGCT : une conception de boîtier à faible inductance parasite permettant une commutation rapide et plus homogène sans filamentation, et une "couche tampon" dans la structure semi-conductrice entre les zones P+ et N-, à dopage N moyen. Grâce à cette couche

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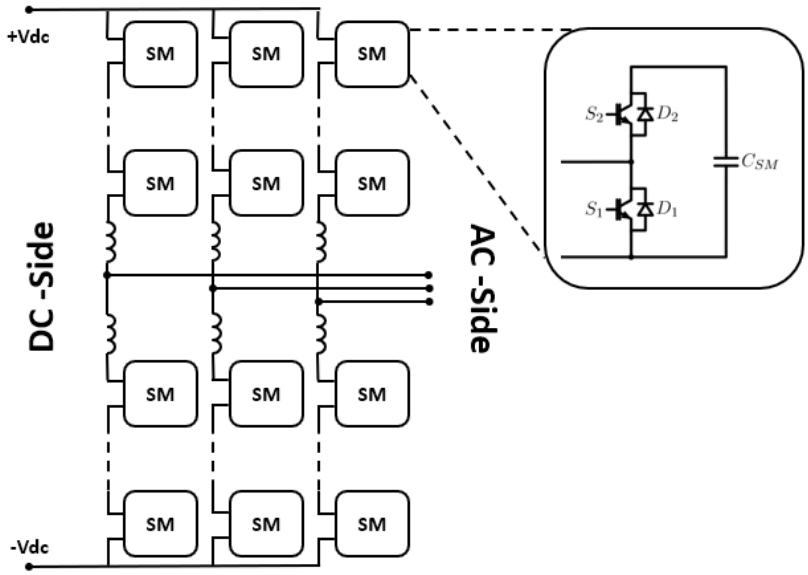
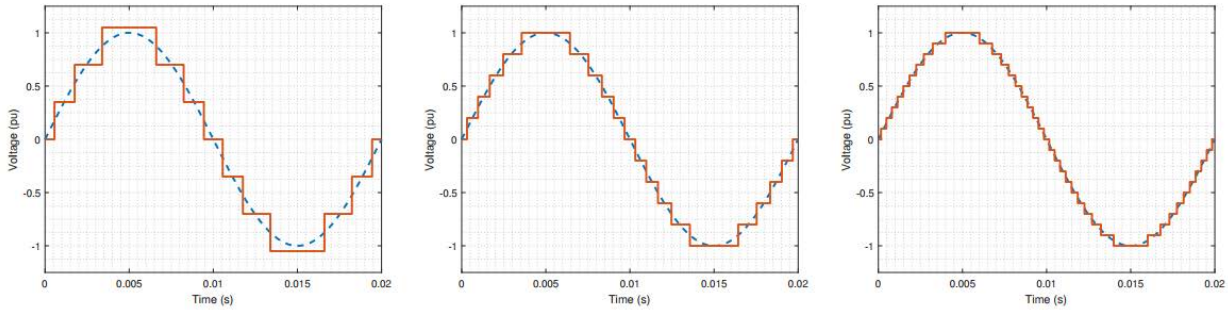


(a) Schéma électrique du convertisseur modulaire multi-niveaux et un de ses sous-modules (SM)



(b) Formes d'ondes de tension typiques d'un MMC avec un nombre différents de sous-modules [8], de gauche à droite, le nombre de sous-modules grandit.

Figure I.2: Schéma électrique et formes d'onde en tension typiques d'un MMC.

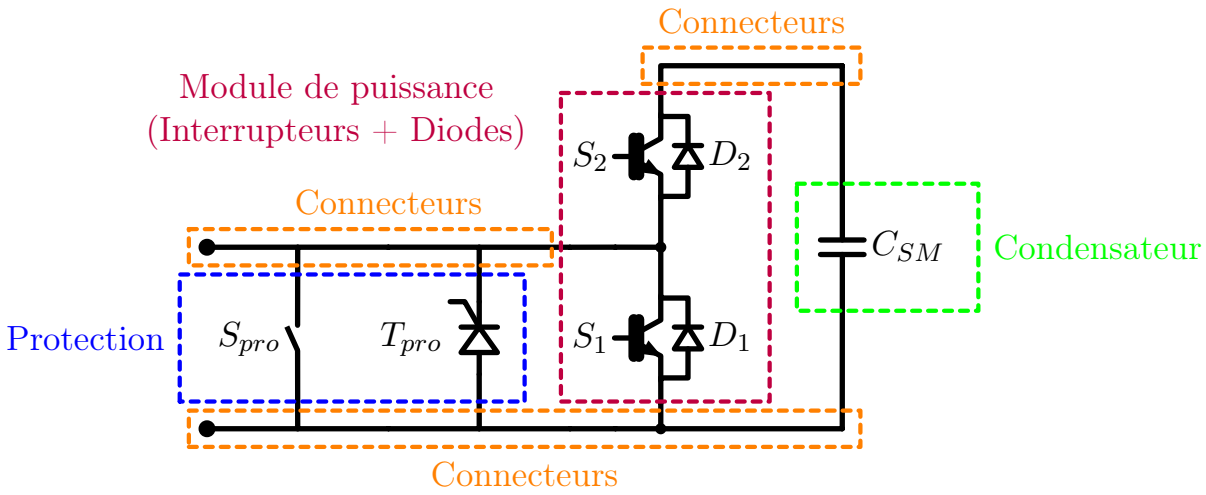


Figure I.3: Structure typique d'un sous-module Demi-Pont (HB, pour 'Half-Bridge'). Les connecteurs sont généralement des barres de cuivre ('busbars').

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Table I.1: Tableau présentant un aperçu des différentes parties d'un sous-module (SM) dans un MMC.

Élément	**Rôle**	**Conception: Règles et Principes**
Module de puissance	Insérer or retirer le condensateur	Générer de faibles pertes, tenue en tension, courant, et fréquence
Condensateur	Source de tension / Source d'énergie	Dimensionnement en énergie, courant, tension
Connecteurs	Connexion électrique	Faible inductance parasite, faible capacité parasite, faible résistance
Circuits de protection	Protéger le SM ou le MMC	Courts-circuits, surtensions, et autres scénarios de défaillance
Circuits auxiliaires	Acquérir des mesures, Contrôler le SM, Alimentation	Haute fiabilité (concernant la CEM), Isolation
Système de refroidissement	Refroidit les semi-conducteurs	Puissance de refroidissement, isolation électrique
Structure mécanique	Maintenir les pièces ensemble, permet l'assemblage	Efforts appliqués, besoins en isolation, assemblage possible

tampon, la distribution du champ électrique dans le semi-conducteur a une forme trapézoïdale, ce qui permet d'utiliser une couche de silicium beaucoup plus petite pour la même tension de blocage. Il en résulte une réduction de la tension à l'état passant et des énergies dissipées à la commutation. Une autre conséquence est une bien meilleure immunité aux dV/dt, éliminant le besoin d'un 'snubber' à l'ouverture, utilisé pour les GTO. Dans le cas où une diode de roue libre est associée à l'IGCT, un 'snubber' pour la fermeture est nécessaire. Ce 'snubber' est consistitué d'une inductance, d'un condensateur, d'une diode et d'une résistance.

Transistor de type IGBT ('Insulated Gate Bipolar Transistor')

L'IGBT est un interrupteur semi-conducteur commandé en tension, développé au début des années 1980 en combinant la structure d'un MOSFET et d'un transistor N-P-N. Ses pertes relativement faibles et sa capacité à fonctionner à des fréquences élevées (plusieurs kilohertz) font qu'il est largement utilisé dans de nombreuses applications. Par rapport au GCT ou à d'autres thyristors, qui sont fabriqués sur une tranche entière de semi-conducteur, les modules IGBT sont formés par la mise en parallèle d'un certain nombre de puces semi-conductrices plus petites, ce qui permet de les adapter à différentes puissances, et d'avoir de nombreux modules différents avec les mêmes puces unitaires.

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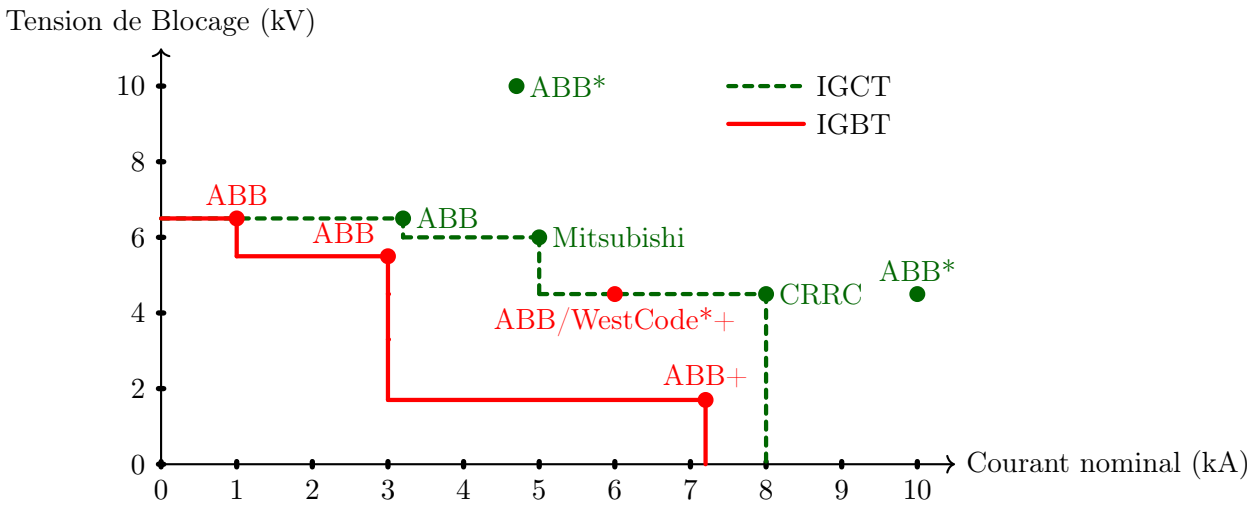
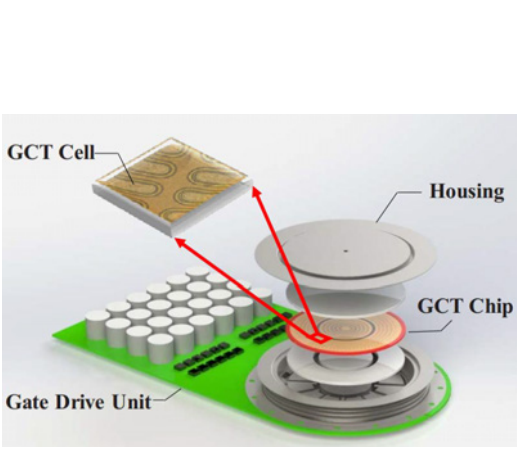
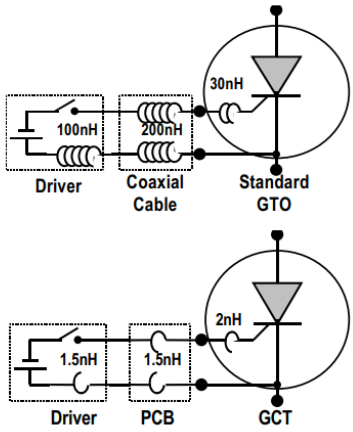


Figure I.4: Valeurs nominales des interrupteurs semi-conducteurs (IGBTs et IGCTs), avec leur tension de blocage et leur courant nominal. Sources : Catalogues en ligne d'ABB, Mitsubishi, CRRC, Dynex, Toshiba (2019).



(a) Structure de l'IGCT (GCT + circuit de grille). [9]



(b) Différence entre circuits de grille du GTO et de l'IGCT. [1]

Figure I.5: Structure de l'IGCT avec une vue éclatée et la différence des circuits de grille avec le GTO.

(a) ABB. (b) CRRC. (c) Mitsubishi.

Figure I.6: IGCTs de différents fabricants. Sources: ABB, CRRC, Mitsubishi.

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Chapitre II : IGCT dans un sous-module MMC - Comparaison avec les IGBTs, nécessité du 'snubber' et étude de pertes.

II.1 Études de pertes de la littérature

Plusieurs études se concentrent sur la comparaison des IGCTs avec des IGBTs dans le cas des sous-modules MMC. Les résultats de ces articles sont résumés dans le Tab. II.1. Il en résulte que parmi tous les semi-conducteurs la solution IGCT est toujours celle qui présente les pertes les plus faibles. On peut également constater que les pertes dépendent fortement du point de fonctionnement, des valeurs nominales des MMC, de la méthode de contrôle (influence sur la fréquence de commutation et donc sur les pertes de commutation) et d'autres paramètres du modèle. Le 'snubber' n'ajoute qu'une faible contribution aux pertes. L'IGCT présente des pertes inférieures dans ces études en raison de ses énergies de commutation comparables (à tension/courant équivalent) et de sa tension à l'état passant inférieure à celle de l'IGBT.

Table II.1: Etudes de pertes venant de la litérature, comparant des IGCTs et des IGBTs dans des MMCs HVDC.

Publication	Pertes totales IGBT (%)	Pertes totales IGCT (%)	Onduleur ou redresseur	Réduction des pertes (%)
[10]	0.48	0.41	Moyenne redresseur et onduleur	14.6
[5]	0.64 (StakPak)	0.44	Redresseur	31
[5]	0.32 (StakPak)	0.27	Onduleur	15.6
[17]	0.76 (PressPack)	0.74	Redresseur	2.6
[17]	0.83 (PressPack)	0.64	Onduleur	22.9

II.2 Nécessité du 'snubber'

Alors que la vitesse de commutation d'un IGBT peut être contrôlée par le courant fourni par son circuit de grille, l'IGCT n'offre pas cette possibilité de contrôle. Une fois initiée, la fermeture de l'IGCT est un processus auto-entretenu, avec une rétroaction positive qui la rend très rapide. Bien qu'une fermeture aussi rapide soit souhaitable pour réduire les pertes de

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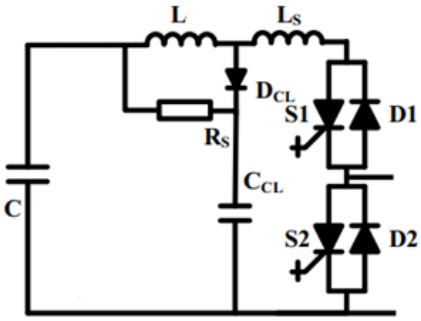
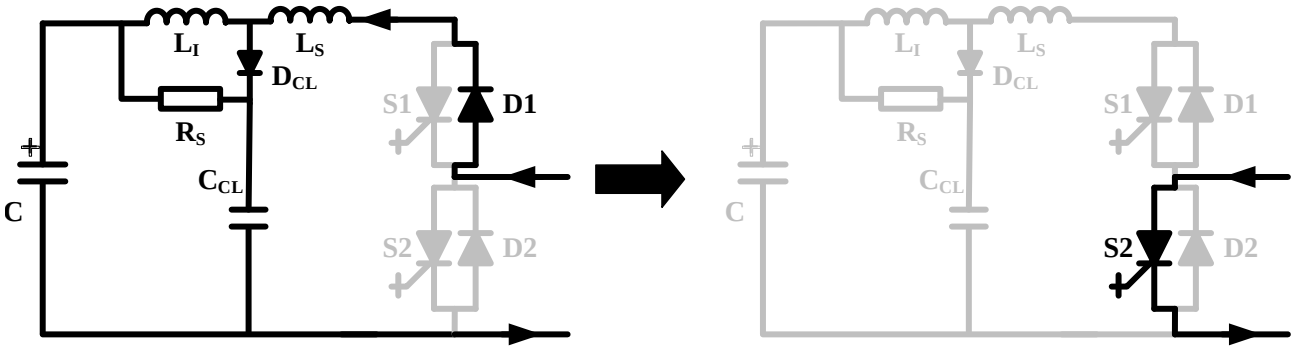


(a) Sous-module MMC avec des IGCTs et un circuit de 'snubber'.



(b) Séquence de commutation: Avant la fermeture de l'IGCT du bas, le courant passe oar la diode du haut; après, le courant par l'IGCT du bas, forçant la diode du haut à s'ouvrir.

Figure II.1: Sous-module MMC avec des IGCTs et un circuit de 'snubber' et sa séquence de commutation illustrant le rôle du circuit de 'snubber'. [15].

commutation, elle peut entraîner une contrainte excessive sur la diode de roue libre opposée (dans une configuration HB). Par conséquent, il est recommandé d'utiliser un 'snubber' d'aide à la fermeture pour limiter la vitesse de fermeture à une valeur généralement inférieure à 1 kA/µs.

Pour ABB et pour la plupart des articles sur les IGCT [1, 3, 4, 5, 6, 11, 12, 14], la raison pour laquelle un 'snubber' di/dt est nécessaire est de s'assurer que les diodes D1 et D2 (Fig. II.1) restent dans leur domaine d'utilisation lorsqu'elles s'éteignent. Si aucun 'snubber' (correspondant aux composants L_I, D_{CL}, C_{CL} et R_S dans la Fig. II.1) n'est installé, le di/dt à la fermeture pour l'IGCT est seulement limité par l'inductance parasite de la boucle de puissance (LS dans la Fig. II.1a). Dans [15], il est montré que sans 'snubber', la valeur de di/dt peut alors atteindre jusqu'à 20 kA/µs. Les transitoires très rapides d'ouverture de la diode provoquent le passage d'un important courant de recouvrement négatif à travers la diode. En raison des effets thermiques, les grands courants de recouvrement ne sont pas répartis uniformément sur la surface de la diode, ce qui rend possible l'apparition d'un filament de courant. Cela entraîne une défaillance de la diode, voire l'explosion du boîtier, comme le montre la figure II.2 [15]. La vitesse de coupure maximale acceptable est une valeur caractéristique d'une diode donnée. Par exemple, alors que 20 kA/µs est une valeur beaucoup trop élevée, de nombreuses diodes peuvent supporter 1 kA/µs, et certaines peuvent atteindre jusqu'à 5.2 kA/µs, comme dans [15, 16] (par exemple la diode ABB 5SDF 28L4521).

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Figure II.2: Diode explosée à cause d'un trop fort di/dt [15].

II.3 Comparaison via des figures de mérite originales et une simulation de pertes

La création de figures de mérite de pertes originales dans cette thèse, validées par des résultats de simulation de pertes, a permis une approche plus générale, comparée à l'approche spécifique des études de pertes (un convertisseur, une méthode de contrôle et souvent un seul modèle de composant par type de composant). La figure de mérite $FM_{swi-loss}$ est liée aux pertes en commutation et la figure de mérite $FM_{cond-loss}$ est liée aux pertes en conduction.

Les figures de mérite utilisées sur les IGCTs et des IGBTs Stakpak d'ABB pour différentes tensions nominales sont présentées à la figure II.3a. Ils sont en bon accord avec les pertes de commutation et de conduction correspondantes calculées à l'aide du modèle MMC développé dans cette thèse, représentées sur la figure II.3b. Les deux approches (figures de mérite et étude de pertes) confirment la supériorité des IGCT sur les IGBT en ce qui concerne les pertes en général. Ceci démontre aussi l'intérêt de ces de ces figures de mérite : elles offrent un moyen rapide, général et efficace de comparer des composants avant même de modéliser et de simuler une MMC spécifique. de modéliser et de simuler une MMC spécifique.

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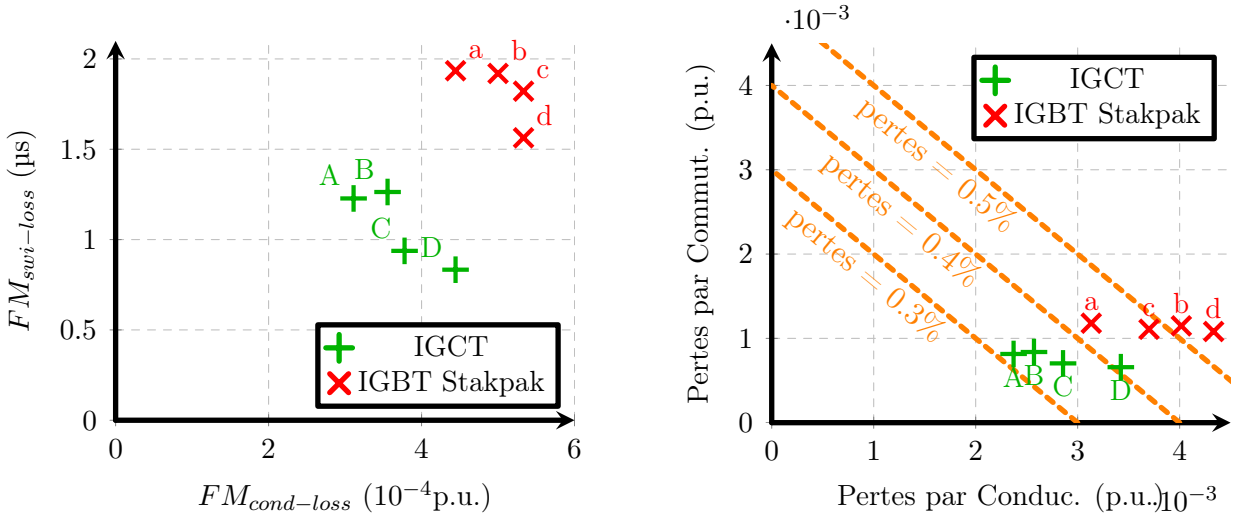

Figure II.3: (a) Figures de mérite appliquées au catalogue d'ABB pour les IGCTs et les IGBTs Stakpak de 4,5kV en 2019; (b) Pertes en conduction et commutation pour les mêmes composants, avec les courbes iso-pertes en orange.

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Chapitre III : conception d'un circuit de test de Double Impulsion combinant IGCT et diode à recouvrement rapide

III.1 Circuit de test utilisé et contrainte principale

Comme présenté dans le chapitre précédent, un 'snubber' à la fermeture (de l'IGCT) est nécessaire car même si l'IGCT peut gérer des valeurs de di/dt plus élevées que celles citées dans les fiches techniques, la diode peut ne pas être capable de les supporter. Les auteurs de [15, 16] considèrent qu'une valeur optimale est de 5.3 kA/µs, ce qui correspond à la valeur maximale de di/dt acceptable pour certaines diodes (par exemple la diode ABB 5SDF 28L4521).

Le but de cette étude est de déterminer si le 'snubber' peut être supprimé dans les sous-modules MMC à base d'IGCT (ou du moins réduit) si des diodes de roue libre suffisamment rapides sont utilisées. Pour rappel, le 'snubber' à l'allumage est composé d'une inductance de 'snubber' (limitant le di/dt) et d'un circuit (appelé 'clamp') RCD (limitant la surtension produite par l'inductance de 'snubber'). En retirant le 'snubber', la limite en di/dt lors du recouvrement inverse serait limitée seulement par l'inductance parasite du circuit. Pour une inductance parasite de 300nH et à une tension de bus de 3kV par exemple, une diode supportant au moins 10kA/µs est nécessaire.

Pour analyser et tester la réduction et la suppression du 'snubber', il faut étudier les commutations de l'IGCT, en particulier sa phase de fermeture. Un circuit d'essai de commutation couramment utilisé est le "test à double impulsion" ('double pulse' en anglais) pour déterminer les caractéristiques dynamiques des composants semi-conducteurs (énergie de commutation, comportement à la commutation) et l'intégration des composants (étude du comportement d'une cellule de commutation et de ses éléments parasites). Ce test à double impulsion sera utilisé pour cette thèse. Le circuit complet de ce test est donné en figure III.1.

Le dispositif expérimental doit imiter la structure d'un sous-module MMC HVDC en demi-pont ('Half-Bridge' en anglais), de sorte que la cellule de commutation conçue ici ait un comportement similaire à celui d'un sous-module et que les conclusions des essais puissent être extrapolées au cas d'un véritable sous-module MMC HVDC. **Ceci est la contrainte principale fixée lors de la conception de ce banc d'essais.** Les plaques de cuivres servant à connecter les éléments de la partie sous-module doivent être dimensionnées pour les courants nominaux typiques des sous-modules MMC HVDC pour la même raison. Le concept finalisé de

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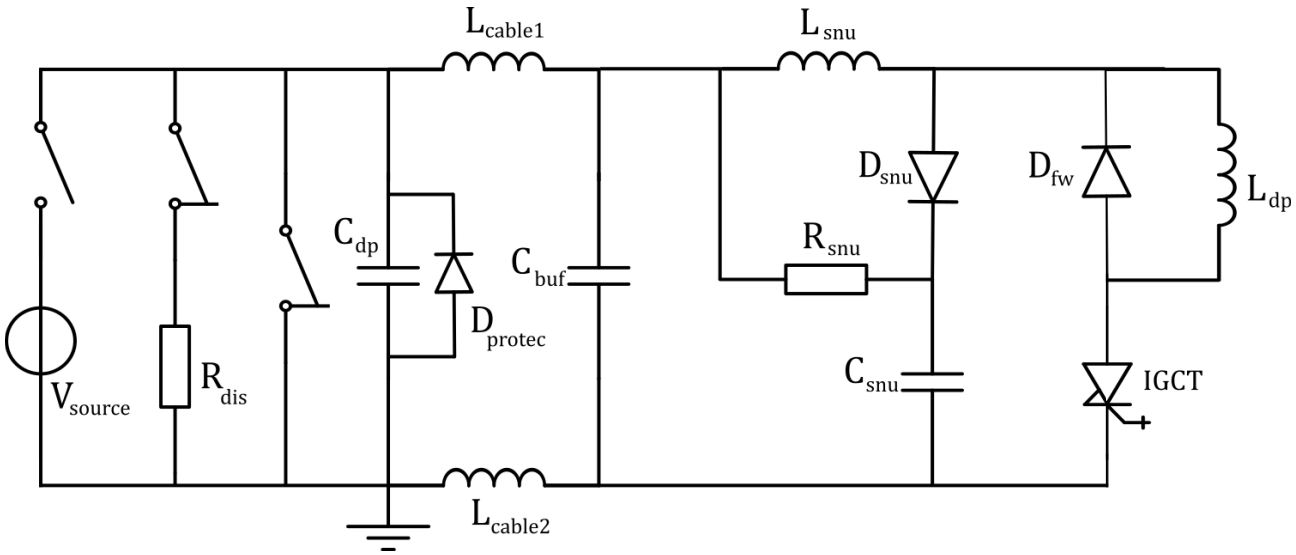

Figure III.1: Circuit de test complet.

cette partie sous-module, qui s'étend dans le circuit figure III.1 de C_{buf} (inclus) à L_{dp} (exclus) est visible en figure III.2.

III.2 Choix et conception des éléments principaux

Les éléments qui sont présentés dans ce résumé sont l'IGCT, la diode de roue libre et le concept développé pour l'inductance de 'snubber'.

IGCT Ici, il a été décidé de se concentrer sur les IGCT 6kV-6.5kV car ils permettent un fonctionnement à plus haute tension, une tendance générale dans les MMC, et parce qu'ils permettraient de tester les diodes 4.5 et 6.5kV. L'IGCT sélectionné est le modèle 5SHY 42L6500 d'ABB. Il tient une tension de 6.5kV (tension de blocage) et peut interrompre un courant de 3.8kA (équivalent à 1.29kA de courant moyen).

Diodes de roue libre Pour sélectionner la diode de roue libre, le critère principal était son di/dt maximal autorisée pendant le recouvrement de la diode. Après une recherche complète, nous avons sélectionné les références 5SLD0600J650100 (6,5kV de tension de blocage, 2 ×600A de courant et 2 ×4kA/µs en di/dt autorisé) et 5SLD1200J450300 d'ABB (4,5kV de tension de blocage, 2 ×1200A de courant et 2 ×6,5kA/µs en di/dt autorisé).

Inductance de 'snubber' Les valeurs de la plage d'inductance sont calculées à l'aide de l'équation $u = L.di/dt$, u étant la tension nominale du bus (2,8kV pour la diode de 4,5kV et 3,6kV pour la diode de 6,5kV). Les points importants sont décrits dans le tableau III.1. Ces points caractéristiques définissent d'une part la valeur maximale typique acceptable pour une diode 'normale' (1kA/µs) et d'autre part la valeur maximale acceptable de ces diodes rapides (8kA/µs et 13kA/µs). Ces points indiquent également quel doit être l'ordre de grandeur de

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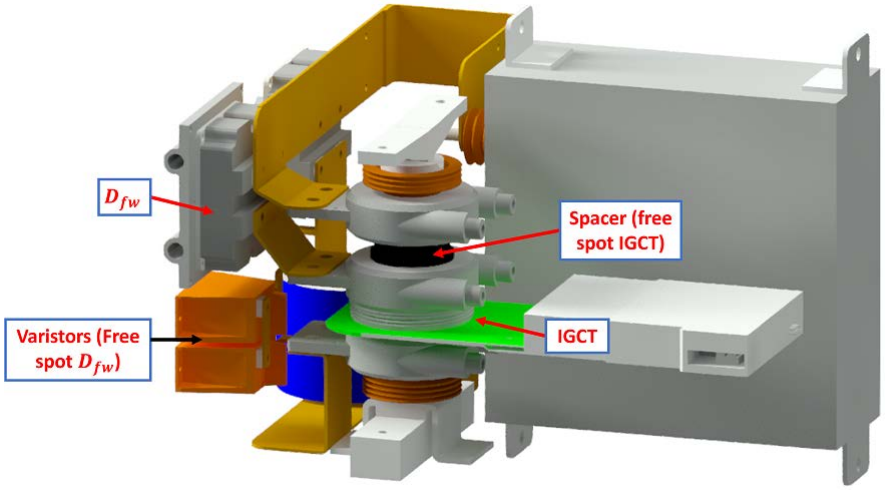
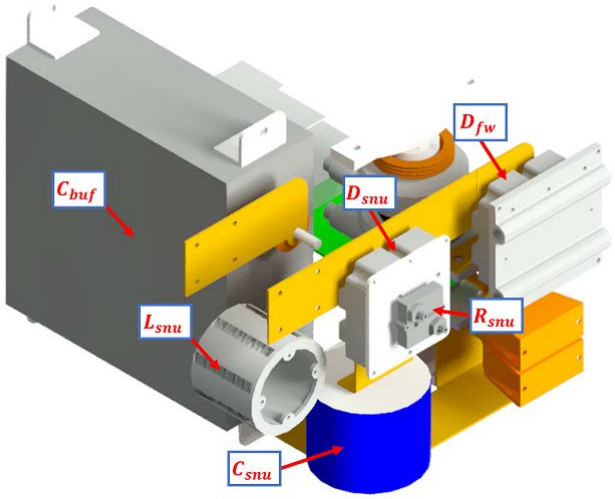


(a) Vue de côté, montrant la cellule de commutation (IGCT + diode).



(b) Vue de dessus montrant le 'snubber'.

Figure III.2: Rendus 3D de la partie sous-module du banc d'essais. Pour la clarté de la lecture, les câbles, le support mécanique et la visserie ne sont pas modélisés.

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Table III.1: Points importants de l'étude en termes de di/dt.

Points	***Valeur de di/dt***	***Tension***	***Inductance correspondante***
di/dt indiqué sur la fiche technique (2×diode 6.5kV)	1kA/µs	3.6kV	3.6µH
di/dt maximal (2×diode 6.5kV)	8kA/µs	3.6kV	450nH
di/dt indiqué sur la fiche technique (2×diode 4.5kV)	1kA/µs	2.8kV	2.8µH
di/dt maximal (2×diode 4.5kV)	13kA/µs	2.8kV	215nH

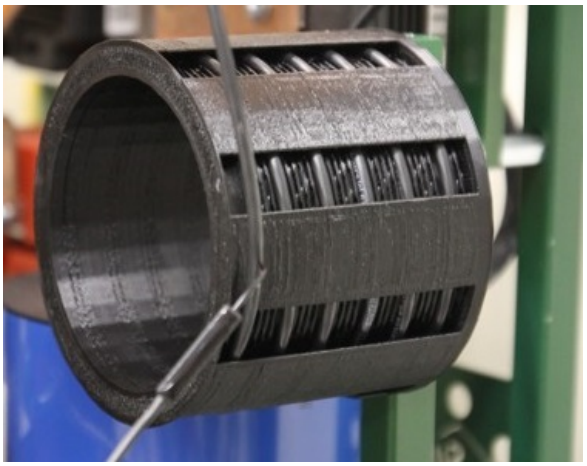

Figure III.3: Concept final de l'inductance imprimée en 3D.

l'inductance parasite pour fonctionner sans 'snubber', au plus près du di/dt maximal (215nH pour la diode 4,5kV et 450nH pour la diode 6,5kV).

La solution retenue pour le concept de l'inductance est celui d'un câble enroulé autour d'un cylindre, comme le montre la figure III.3. La réalisation de ce cylindre a été faite par impression 3D, en utilisant le PLA comme matériau d'impression. L'impression 3D est utilisée ici car elle permet de produire des pièces uniques pour un coût global faible. Les valeurs obtenues des inductances sont présentées dans le tableau III.1. La différence entre les inductances réelles et les valeurs simulées peut s'expliquer par le fait que l'inductance simulée ne tient pas compte de la longueur de câble pour connecter les inductances aux plaques de cuivre, qui peut être estimée à environ 10 cm de long de chaque côté. Pour les valeurs d'inductances inférieures à 800nH, les inductances à 1 tour n'ont pas été envisagées. Au lieu de cela, un jeu de barres avec différentes positions de serrage, pour avoir différentes tailles de boucles de courant, est la solution adoptée pour les faibles inductances.

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Table III.2: Valeurs des inductances obtenues après fabrication; comparées aux valeurs obtenues par simulation, pour 100kHz, un cylindre de diam. 12cm, a câble de surface conductrice 8.37mm^2, et 15mm d'inter-tours.

Inductance n°	*Nbr de tours apparents*	*Inductance (µH) @10kHz*	*Ind. (µH) @100kHz*	*Ind. simulée (µH) @100kHz*
Inductance n° 1	2	0.825	0.80	0.637
Inductance n° 2	3	1.39	1.34	1.156
Inductance n° 3	4	2.05	1.97	1.759
Inductance n° 4	5	3.1	2.9	2.395
Inductance n° 5	6	3.55	3.42	3.161

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Chapitre IV : Commutation d'un IGCT avec des diodes Silicium rapides

Les diodes PiN étant des composants bipolaires, les porteurs minoritaires participent à l'état passant de la diode, mais ils doivent être évacués pendant la transition entre l'état passant et l'état bloquant. Cette évacuation des charges crée un courant négatif transitoire appelé recouvrement inverse. La figure IV.1 présente une forme d'onde typique de recouvrement inverse. Ce phénomène est limitant dans l'utilisation des diodes, notamment en cas de forts di/dt (pouvant mener à une destruction provoquée par une avalanche dynamique) ou en cas de dynamique de charges particulières (appelée 'snap-off' en anglais) créant des surtensions potentiellement destructrices.

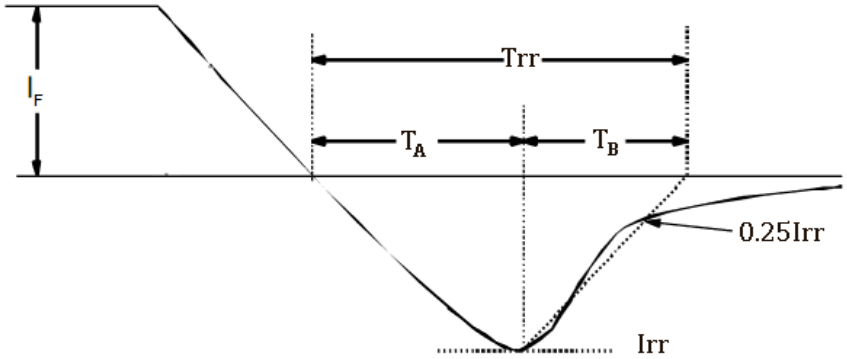

Figure IV.1: Formes d'ondes de recouvrement inverse dans une diode utilisée dans le JEDEC. [7]

IV.1 Formes d'onde typiques

Afin de mieux comprendre les formes d'onde présentées dans le reste de ce résumé, le circuit et le rendu 3D de notre banc d'essais avec les positions des capteurs est montré en figure IV.2. Des formes d'ondes typique d'une commutation (lors de la fermeture de l'IGCT) est montré en figure IV.3.

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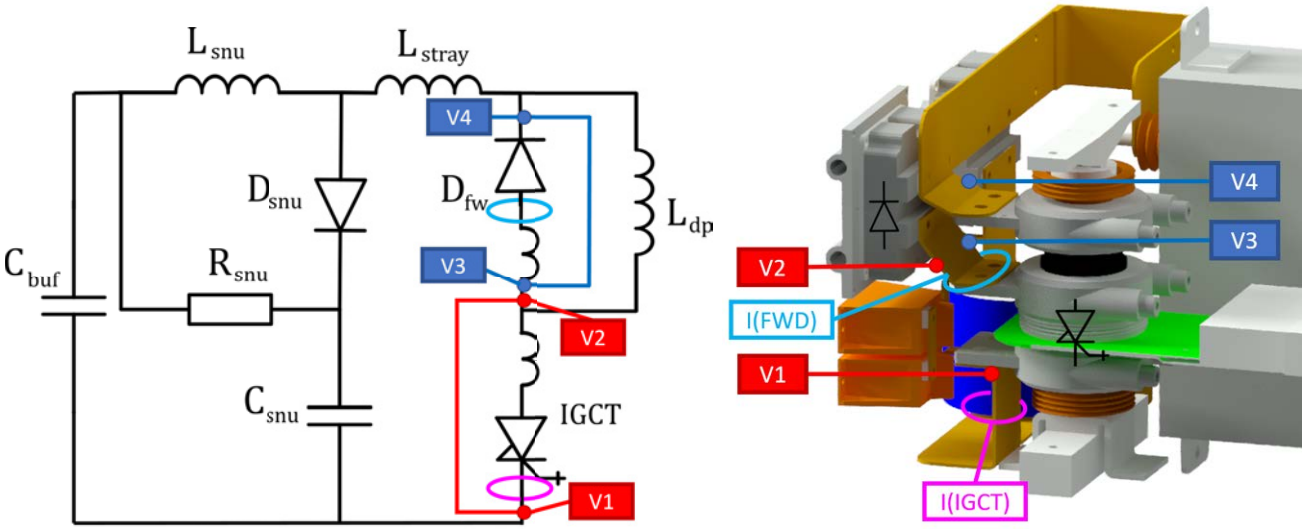

(a) Schéma électrique, partie SM. (b) Rendu 3D.

Figure IV.2: Positions des sondes de courant et de tension dans le circuit, précisées avec un schéma du circuit et un rendu 3D. V2-V1=V(IGCT); V4-V3=V(FWD).

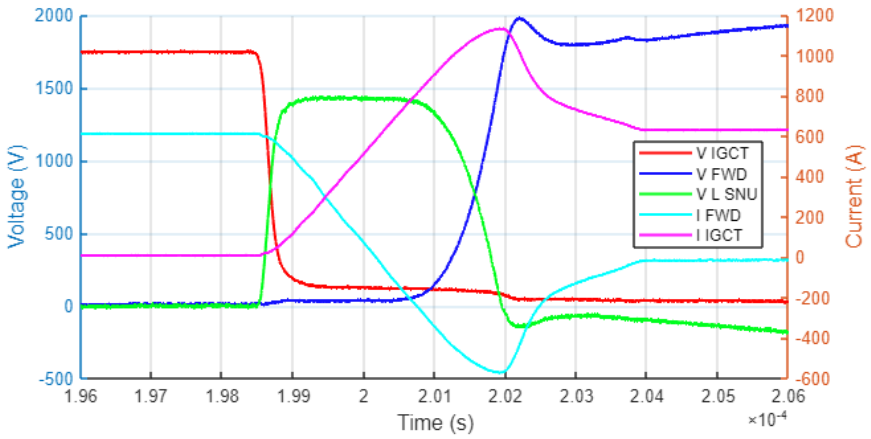

Figure IV.3: Formes d'ondes typique d'une commutation (lors de la fermeture de l'IGCT), sans événement de type 'snap-off'. La forme d'onde de tension aux bornes de l'inductance est V L SNU. Impulsion pour la diode 4,5kV, 1700V, 600A, inductance de 'snubber' de 3,4µH, 120°C.

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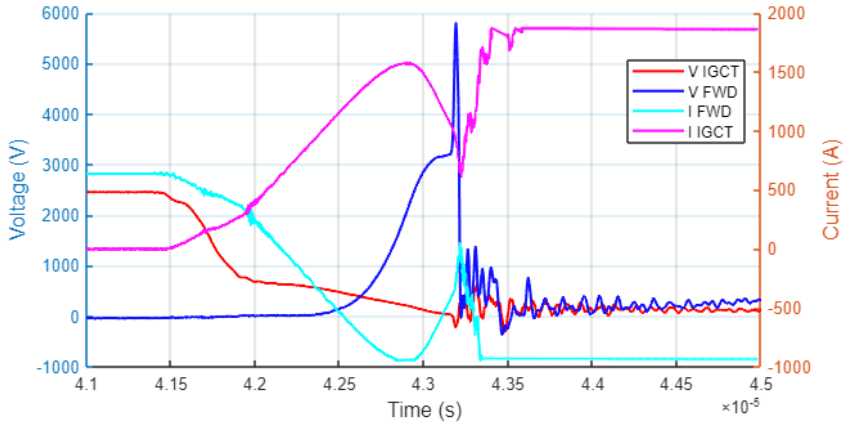
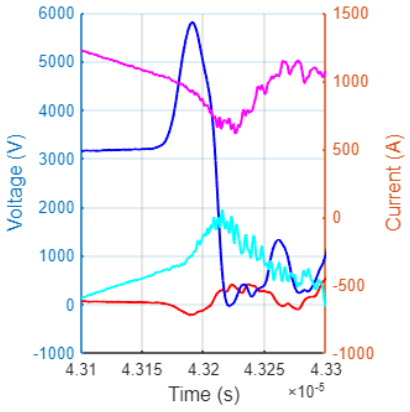
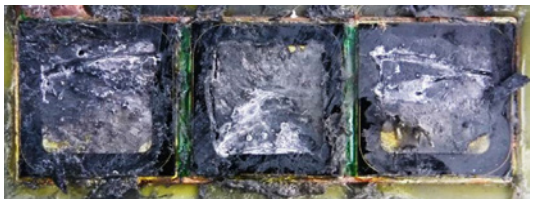


(a) Formes d'ondes de la défaillance 'snap-off'.



(b) Zoom sur le moment du 'snap-off'.



(c) Puces.

Figure IV.4: Évènement de défaillance à cause d'un événement de 'snap-off'. 2400V, 600A, di/dt : 1.7kA/µs, 25°C. Diode : 4,5kV.

IV.2 Évènements destructifs dans notre banc d'essai

Surtension provoquée par un 'snap-off' Cet événement destructeur a eu lieu avec la diode de 4,5kV. La figure IV.4 montre les formes d'onde et les puces détruites. Un événement de snap-off a eu lieu et une tension maximale de plus de 4.5kV (voir figure IV.4a et IV.4b) a conduit à la formation de filaments destructeurs dans 3 puces côte à côte (voir figure IV.4c). Le di/dt pendant le snap-off atteint 12kA/µs, ce qui donne une inductance parasite équivalente de 280nH, en considérant une surtension de 3.4kV, ce qui est cohérent avec l'ordre de grandeur de l'inductance parasite estimée du circuit (450nH). Le 'snap-off' a été étudié dans cette thèse et sur notre banc de tests. Il survient à faible courant, faible température, tension élevée et inductance de fuite élevée. Dans notre circuit avec la diode 4,5kV, il survient à des niveaux de courants/tensions rendant l'utilisation de notre sous-module dans un MMC réel impossible. Sur la figure IV.5, on voit qu'à température ambiante la diode ne peut commuter au dessus de 1700V sans subir une violente surtension de plus de 1kV.

Avalanche dynamique en raison de fort di/dt Ce deuxième événement de défaillance, que l'on retrouve sur la figure IV.6, s'est produit avec la diode de 6,5kV. Le di/dt, bien que n'étant pas supérieur au maximum (4,5kA/µs pour les deux diodes en parallèle par rapport à la limite de 2×4kA/µs), est tout de même élevé, et combiné avec un courant au double du courant nominal (2400A), une inductance parasite élevée (environ 450nH par rapport à 280nH pour les conditions de test dans la fiche technique de la diode) et un niveau de tension assez élevé (3300V), il a apparemment conduit à une défaillance par avalanche dynamique. Contrairement

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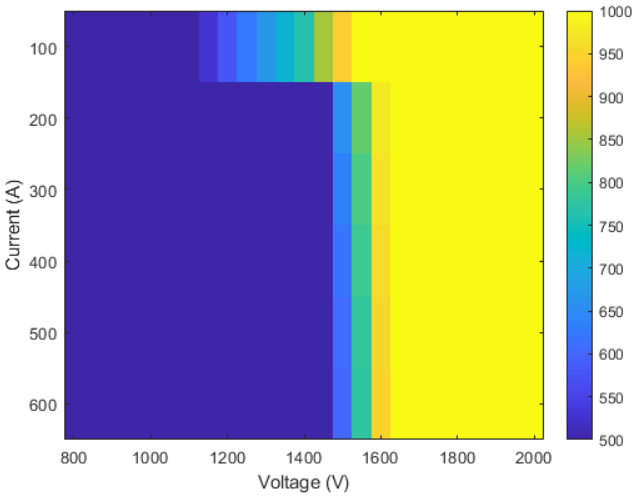
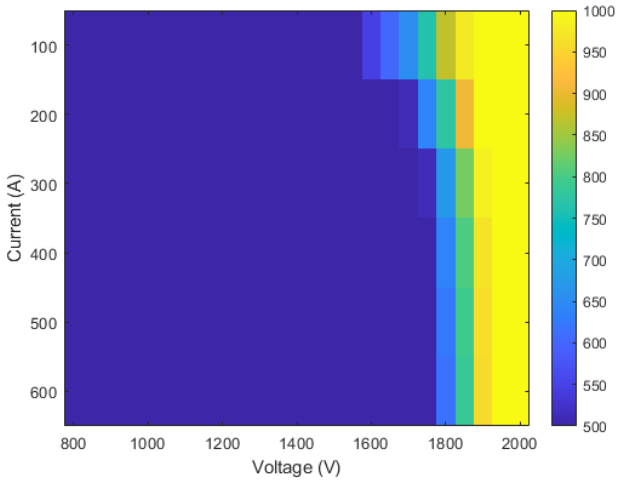
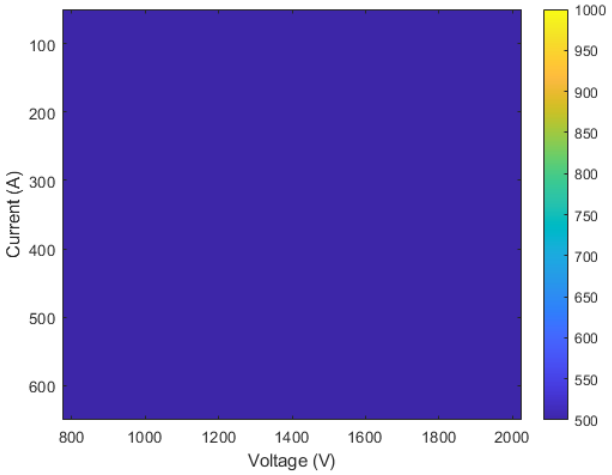


(a) Temp. Amb. (25°C).



(b) 60°C.



(c) 120°C.

Figure IV.5: Cartographies illustrant l'influence de la tension, du courant et de la température sur l'occurrence du 'snap-off'. Diode : 4.5kV. L_{snu}=3.4µH.

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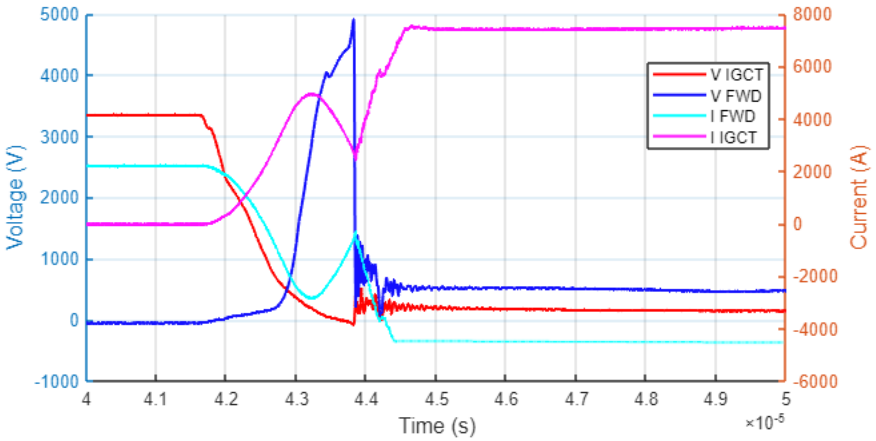
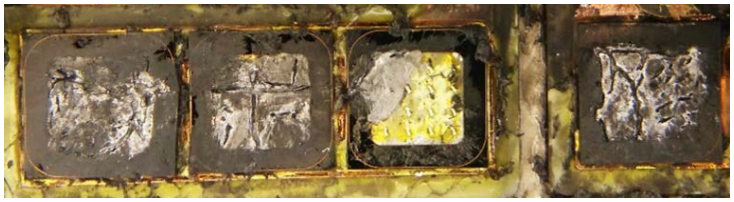


(a) Formes d'ondes de la défaillance 'hors-limites'.



(b) Puces.

Figure IV.6: Evénement de défaillance à cause d'un événement de type 'hors-limites' (avalanche dynamique de 3ème degré). 3300V, 2200A, di/dt of 4.5kA/µs, 25°C. Diode : 6,5kV.

au précédent paragraphe, la tension n'a pas dépassé la tension de claquage de 6,5kV (voir figure IV.6a), ce qui appuie l'hypothèse de l'avalanche dynamique.

IV.3 Fonctionnement sans 'RCD-clamp'

Le fonctionnement avec la plus petite valeur d'inductance du 'snubber' (autour de 100nH) a été possible avec la diode 4,5kV, mais pas avec la diode 6,5kV. L'étape suivante a été de retirer le condensateur, la résistance et la diode, et de tester dans les mêmes conditions, avec la même inductance de 'snubber'. Comme prévu, la surtension est plus élevée dans le cas du retrait du 'RCD-clamp', parce que le retrait de ce 'clamp' a augmenté de fait l'inductance de fuite. Les surtensions résultantes sont affichées sur la figure IV.7 à 120°C. Le fonctionnement sans 'clamp' a été testé jusqu'à 2400V, 1800A à 120°C, sans aucune défaillance.

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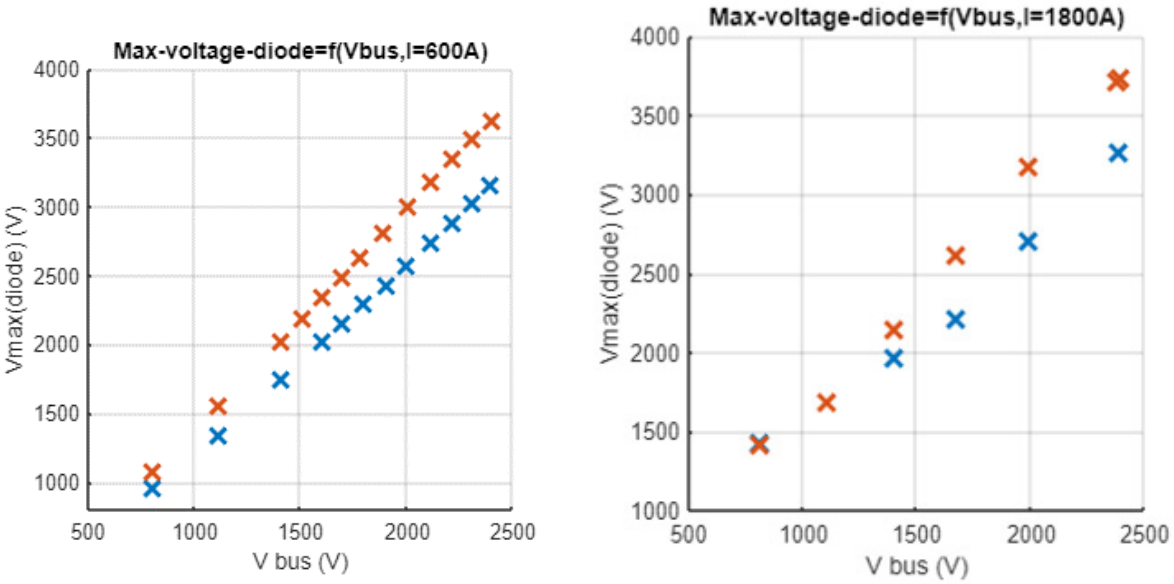

(a) Cas I=600A.

(b) Cas I=1800A.

Figure IV.7: Comparaison des surtensions dans le cas avec 'clamp RCD' (bleu) et sans (orange), V = 2400V, température = 120°C.

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Chapitre V : Commutation d'un IGCT avec des diodes en Carbure de Silicium à fort di/dt

IV.1 Diodes en carbure de silicium

Dans ce chapitre et dans ce travail de thèse en général, l'intérêt du carbure de silicium est d'offrir de très bonnes caractéristiques de recouvrement inverse, telles que des pertes plus faibles, une charge stockée plus faible et un recouvrement inverse plus rapide. Ceci s'explique par le fait que le carbure de silicium possède une bande interdite plus large conduisant à une région de base plus fine (pour une même tension de blocage) et donc une quantité de charge stockée plus faible. Les diodes utilisées ici ont été conçues lors de projets précédents à SuperGrid Institute et au laboratoire Ampère.

Les puces de diodes ont été conçues pour résister à 10kV (tension de claquage, mais elles ne tiennent pas toutes cette tension) et conduire 50A (courant direct nominal) pour une puce de taille 10mmx10mm (dimensions extérieures).

IV.2 Le concept du packaging créé dans cette thèse

En raison de la faible quantité de puces de diodes, de l'écart important entre leurs tensions d'avalanche et d'une confiance limitée dans l'opération de conditionnement, le boîtier sera divisé en sous-paquets avec un nombre limité de diodes pour augmenter le rendement 4 par sous-paquet. Pour être testé dans le montage de test présenté au chapitre III, le boîtier de diodes SiC doit être mécaniquement compatible avec le boîtier de diodes ABB. Il doit respecter les positions des trous de montage pour les semelles de boitier, et les positions des trous des plaques de cuivre.

Le matériau de la face arrière des puces (cathode) est de l'argent. Le frittage d'argent, utilisé dans cette thèse, est un procédé de fixation des puces qui permet un bon contrôle du processus (notamment la position) et avait déjà été utilisé dans le laboratoire Ampère.

La surface supérieure elle, est irrégulière et présente des bosses (comme cela peut se voir en figure IV.1). Pour cette raison, la connexion électrique de la face supérieure par la soudure de

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fils fins ('wire bonding' en anglais) n'a pas été retenu pour éviter tout risque de déchirure de la métallisation supérieure. Ceci a conduit au développement d'une solution de pressage local sur le dessus des puces.

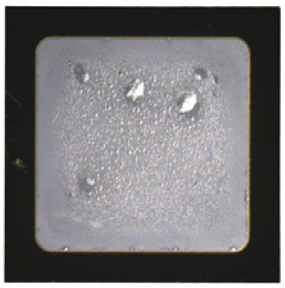

Figure IV.1: Face supérieure typique des puces (anode) des diodes utilisées.

La conception finale est représentée sur la figure IV.2. La diode est divisée en 3 sous-ensembles, mis en parallèle, comme indiqué sur la figure IV.2b. Un sous-ensemble est représenté sur la figure IV.2c, avec ses principaux composants.

IV.3 Caractéristiques des packs obtenus et résultats en double impulsion

Les caractéristiques directes de chaque sous-paquet de diodes sont présentées sur la figure IV.3a. La chute de tension de 2,7V correspond à la valeur de [2], autant que 6,5mΩ pour 4 diodes correspondent aux 24mΩ pour 1 diode de [2]. La différence sur la résistance d'état peut être expliquée par un boîtier légèrement plus résistif dans cette thèse. Il faut noter que le sous-paquet de diodes n°04 a été testé avec des impulsions de 1kA 400µs, sans dommage notable.

La caractéristique inverse de chaque sous-paquet de diodes est représentée sur la figure IV.3b. Ce que l'on peut analyser à partir des valeurs est que 1µA ne peut pas être le courant de référence pour déterminer la tension de claquage : la diode n°08 a une tension inverse de 1.8kV à 1µA mais plus de 5kV à 25µA.

Un packaging original a été conçu pour respecter les caractéristiques et les contraintes des puces de diodes SiC PiN utilisées ici, mais aussi les contraintes du montage de test. Ceci a conduit à la fabrication de sous-packages opérationnels qui peuvent être mis en parallèle pour atteindre théoriquement un courant nominal de 600A et une tension de claquage supérieure à 5kV.

Ces sous-ensembles de diodes SiC seront utilisés dans le montage d'essai à double impulsion avec l'IGCT en silicium, afin d'explorer la possibilité d'un fonctionnement sans 'snubber'.

Afin de confirmer que les diodes en carbure de silicium ont des Irr, Err, Qrr et Trr inférieurs à ceux des diodes en silicium, une comparaison est développée ici. La comparaison des paramètres de recouvrement inverse est illustrée à la figure IV.4, avec un courant à l'état passant de 300 A, une valeur d'inductance de 'snubber' de 800nH et une température de 120°C. En plus des valeurs de Irr, E rr, Qrr et Trr qui sont plus faibles pour la diode SiC que pour la diode Si (ce

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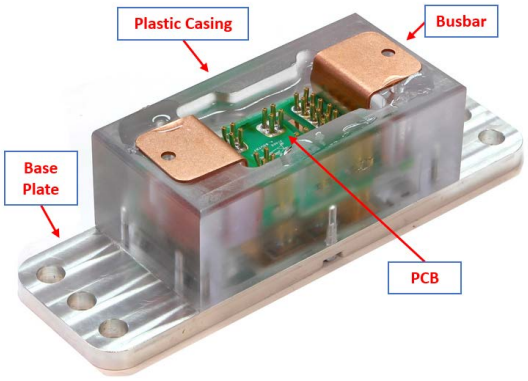
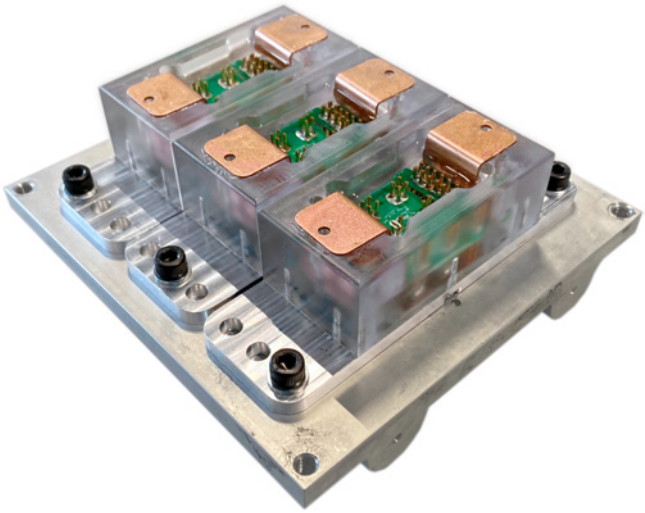
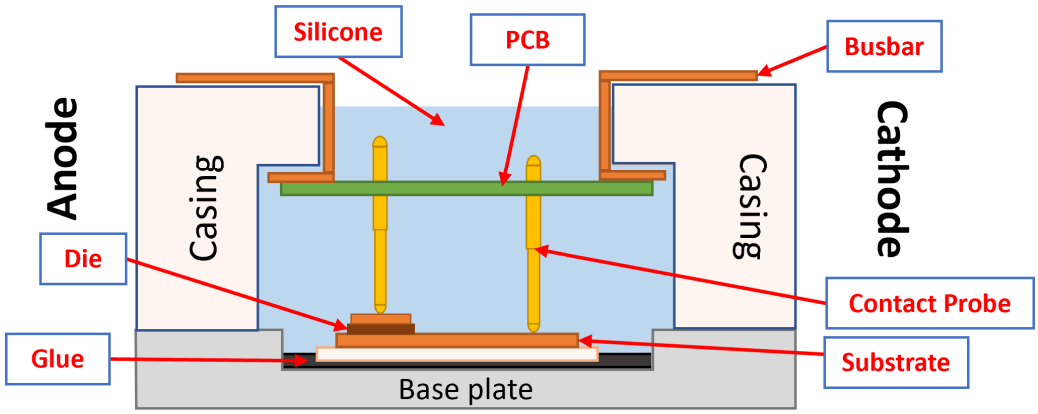


(a) Un sous-paquet.



(b) Trois sous-paquets en parallèle, montés sur le radiateur de la diode ABB.



(c) Sous-paquet, vue en coupe, schéma simplifié.

Figure IV.2: Concept Final de la diode.

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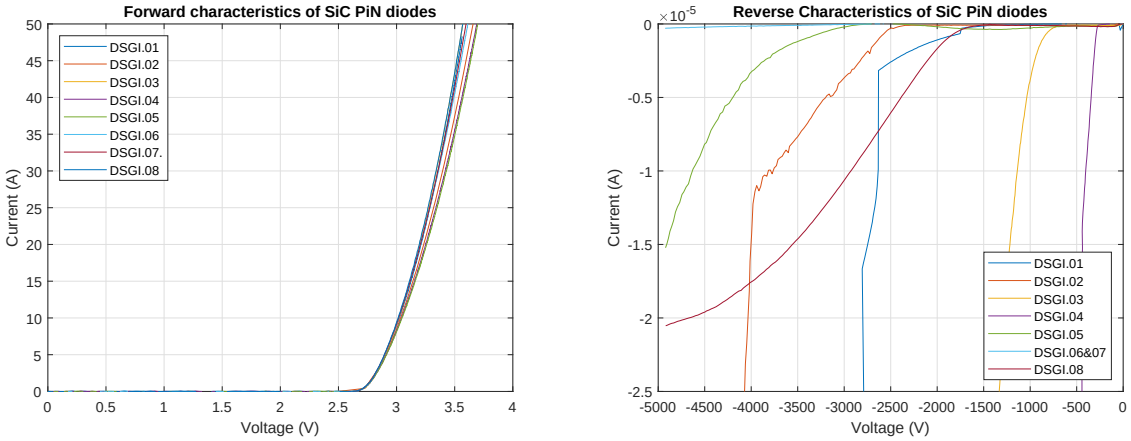

(a) Caractéristiques en conduction.

(b) Caractéristiques en blocage.

Figure IV.3: Caractéristiques des 8 sous-paquets fabriqués.

qui valide la théorie), l'augmentation de Err et Irr avec la tension est plus lente pour la diode SiC que pour la diode Si.

La diode SiC a montré un meilleur comportement de commutation que la diode silicium : moins de pertes de commutation (54.5mJ comparé à 752mJ à 1400V, 300A, 120°C et avec l'inductance 'snubber' de 800nH), durée de recouvrement inverse plus faible (0.48µs comparé à 3.5µ pour les mêmes niveaux). Ceci est d'autant plus important qu'aucune défaillance liée à une recouvrement inverse trop rapide n'a encore été identifiée, et que des valeurs de di/dt plus élevées doivent donc être explorées, avec une inductance parasite plus faible et des niveaux de tension plus élevés.

Avec des valeurs di/dt suffisamment élevées, un phénomène spécifique apparaît avec la diode SiC : la diode SiC, étant très rapide (dans la gamme de 0,25-0,5µs), commence à bloquer la tension avant que l'IGCT ne soit complètement hors tension. Cela a limité la surtension aux bornes de la diode. Le fonctionnement sans 'snubber' a été réussi (aucune défaillance) à 2000V/150A et 2400V/100A dans une configuration parallèle à deux diodes. Aucun phénomène de limitation (comme le claquage pour la diode Si) n'a été identifié. Par conséquent, un fonctionnement sûr jusqu'aux valeurs nominales (4000V, 600A) peut être envisagé, ce qui serait cohérent avec les valeurs normales de la MMC.

À l'avenir, des niveaux de tension et de courant beaucoup plus élevés, avec une inductance parasite plus faible, devront être testés dans cette configuration afin de conclure pleinement sur le fonctionnement sans 'snubber' de l'IGCT dans un sous-module MMC HVDC avec une diode SiC.

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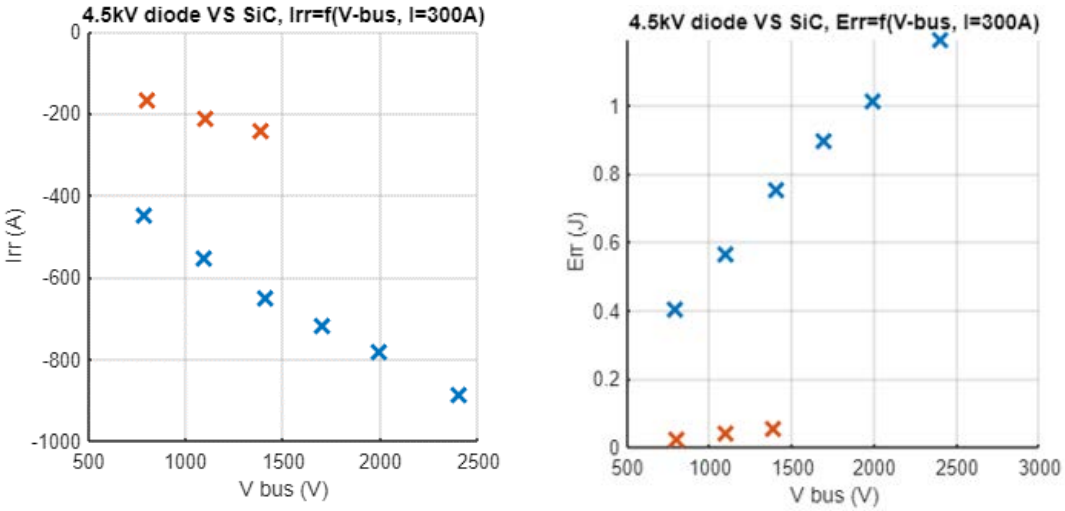
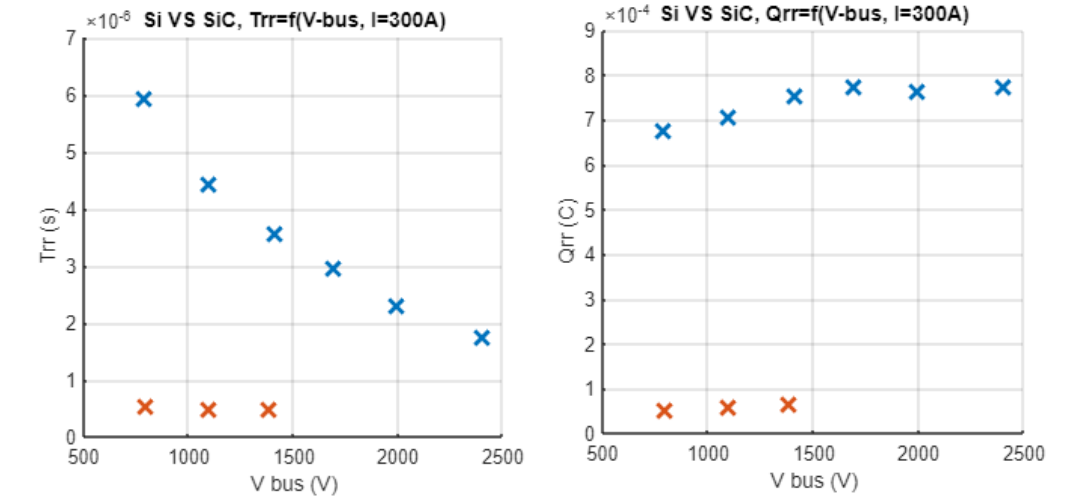


(a) I_{rr} (b) E_{rr}



(c) T_{rr} (d) Q_{rr}

Figure IV.4: Recouvrement inverse : comparaison des mesures des paramètre entre la diode 4,5kV ABB et la diode SiC (configuration 3 sous-paquets), I_{pulse}=300A, inductance 'snubber' : 800nH, température: 120°C.

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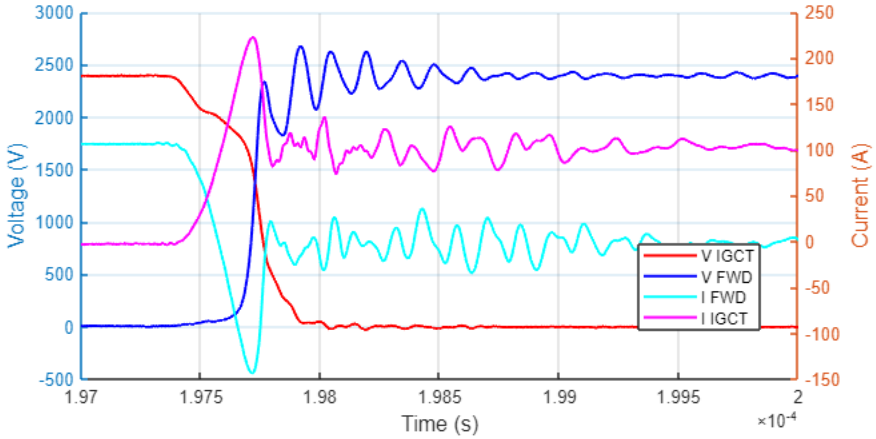
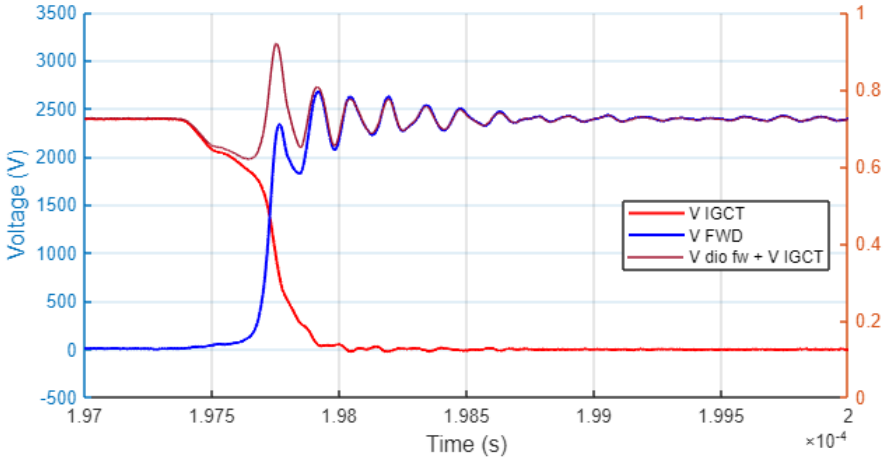


(a) 2400V, 100A, inductance 'snubber' 100nH, température ambiante.



(b) 2400V, 100A, inductance 'snubber' 100nH, température ambiante, avec la somme des tensions.

Figure IV.5: Formes d'ondes de l'IGCT à la fermeture, à fort di/dt, 2400V, 100A, avec une configuration 2-sous-paquets en parallèle.

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FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : BOUTRY DATE de SOUTENANCE : 16/12/2021

Prénoms : Arthur, Jules, Marco

TITRE : Theoretical and experimental evaluation of the Integrated gate-commutated thyristor (IGCT) as a switch for Modular Multi Level Converters (MMC)

NATURE : Doctorat Numéro d'ordre : 2021LYSEI095

Ecole doctorale : Electronique, Electrotechnique et Automatique

Spécialité : Génie Electrique

RESUME :

EN: A study on Integrated gate-commutated thyristors (IGCT) di/dt limiting inductance and RCD-clamp reduction/suppression using plastic module silicon (Si) fast recovery diodes and silicon carbide (SiC) diodes, in Modular Multilevel Converters (MMC). This PhD manuscript contains:
- Analysis of existing HVDC MMC Submodules.
- Assessment of the interest of the IGCT in HVDC MMC Submodules and losses comparison with IGBTs, using MMC-specific figures-of-merit created in this thesis.
- Double pulse test with fast recovery diode in plastic module to attempt to reduce and suppress the limiting di/dt inductor.
- Packaging of High-Voltage High-Current SiC PiN diode dies, test with IGCT in the same setup to attempt to reduce and suppress the limiting di/dt inductor and analyze the specificities of the SiC diode in this setup.

FR : Une étude sur la réduction/suppression de l'inductance de limitation di/dt pour IGCTs et du clamp RCD en utilisant des diodes rapides en silicium (Si) et des diodes en carbure de silicium (SiC) dans les convertisseurs multiniveaux modulaires (MMC). Ce manuscrit de thèse contient :
- Analyse des sous-modules de MMC HVDC existants.
- Évaluation de l'intérêt des IGCTs dans les sous-modules MMC HVDC et comparaison des pertes avec les IGBT, en utilisant des facteurs de mérite spécifiques aux MMC créés dans cette thèse.
- Test de double pulse avec diode à récupération rapide dans un module plastique pour tenter de réduire et supprimer l'inductance limitant le di/dt.
- Packaging de puces de diodes SiC PiN à haute tension et courant élevé, test avec IGCT dans le même montage, pour tenter de réduire et supprimer l'inductance limite di/dt, et analyser les spécificités de la diode SiC dans ce montage.

MOTS-CLÉS : électronique de puissance, HVDC, MMC, IGCT, diode, sous-module, silicium, carbure de silicium, semiconducteur

Laboratoire (s) de recherche : Laboratoire Ampère, CNRS UMR 5005

Directeur de thèse : Cyril Buttay

Président de jury : Philippe Ladoux

Composition du jury :

Ladoux, Philippe, Professeur des Universités	Univ. Toulouse	Examinateur, Président
Dieckerhoff, Sibylle, Professor	TU Berlin	Rapporteure
Dujic, Drazen, Associate Professor	EPFL	Rapporteur
Batut, Nathalie, Maitre de conférences, HDR	Univ. Tours	Examinatrice
Buttay, Cyril, Directeur de recherches	INSA de Lyon	Directeur de thèse
Vagnon, Eric, Maitre de conférences, HDR	Centrale Lyon	Co-directeur
Lefebvre, Bruno, Docteur	SuperGrid Institute	Invité
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Vemulapati, Umamaheswara, Docteur	Hitachi	Invité

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