



Etude et conception d'un pilote de diode laser à cavité verticale générant des pulses inférieurs à 1ns, ayant un haut rendement énergétique et fonctionnant à faible tension

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sous la direction du Professeur Ian O'CONNOR

Study and Design of a Low-Voltage and Power-Efficient Sub-ns Pulse CMOS VCSEL Driver for SPAD-based Direct Time-of-Flight Ranging in Consumer Mobile Electronics.

École Doctorale "Électronique Électrotechnique Automatique"

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*À ma famille,
Isabelle, Denis, Matthieu, Pauline et Simon*

Abstract

Direct time-of-flight (TOF) laser rangefinding is a remote sensing technology which has recently been a growing focus in a wide range of applications. This technique makes it possible to determine the distance to an unknown target from the measurement of the round-trip transit time of a light pulse. A direct TOF sensor is usually implemented by a photodetector based on single-photon avalanche diodes (SPAD) as well as by a near-infrared semiconductor laser. In such a system, the importance of the laser driving electronics cannot be overstated. As a matter of fact, the distance measurement accuracy is a direct function of the transmitted laser pulse width. Thus, a sub- ns laser driver enabling fast rising and falling edges is a key demand. Furthermore, the shortening of the pulse duration improves resolution as it permits to detect multiple echoes when several targets lie in the field of view of the sensor. On the other hand, the energy of the light pulse set the detection range of the sensor. Therefore, shortening the pulse width calls for increasing the laser power so that the detection range remains constant.

The present thesis is carried out with STMicroelectronics. The aim is to develop a fully integrated vertical-cavity surface-emitting laser diode driver for direct TOF rangefinding in consumer embedded electronics. The key focus is to demonstrate the feasibility of sub- ns pulse operation at high repetition frequency, up to several hundreds of megahertz. Furthermore, the electrical specifications involve conflicting and challenging requirements, such as the enhancement of the current capability up to $200mA$ (*i.e.* increase in laser pulse power) while lowering the supply voltage, down to $2.5V$. Last but not least, in the context of consumer mobile devices, there is always a need to aim towards a power- and area-efficient solution.

The key innovation of this thesis is the development of a novel laser diode driver topology. The circuit incorporates a capacitive voltage boost structure so as to overcome the low-voltage constraint. In addition, slow turn-off transient phenomena associated with laser diodes, such as optical tailing, could limit the performances of direct TOF sensors. Accordingly, the proposed driver architecture adds a carrier sweep-out circuit feature in order to mitigate such unwanted phenomena. The circuit has been fabricated in a $40nm$ complementary metal-oxide-semiconductor (CMOS) technology node by STMicro-

electronics.

The manuscript reviews the state-of-the-art of laser diode driver architectures dedicated to TOF applications. This review highlights the pros and cons of each topology in regards to the framework of the thesis. A feasibility study is presented to further compare these architectures. The design of the silicon chip, *i.e.* transistor-level sizing and physical layout, is the central part of the thesis. Then, the manuscript provides a set of measurement to assess the performances as well as the limitations of the fabricated driver circuit. The silicon experimental characterization is mainly based on laser pulse measurements by means of a high-speed photodetector and an integrating sphere. A laser pulse of $311ps$ with a driving current pulse up to $200.8mA$ have been demonstrated at a supply voltage of $2.5V$ and a repetition frequency of $250MHz$. The main performance-limiting factor is the parasitic inductance which is always a major issue in high-speed electronics. The achievements of this thesis represent an important step forward towards future product development by STMicroelectronics.

Résumé

La détection laser par temps de vol (TOF) direct est une technologie qui représente un enjeu majeur dans un nombre croissant d'applications. Cette technique permet de déterminer la distance d'une cible inconnue à partir de la mesure du temps de vol d'une impulsion laser. De manière générale, un capteur TOF direct est réalisé par un photodétecteur utilisant des photodiodes à avalanche mono-photonique ainsi que par un laser à semi-conducteur. Dans ces capteurs, le circuit de pilotage du laser est d'une importance cruciale. En effet, la précision de mesure est directement fonction de la largeur d'impulsion laser transmise. Ainsi, le circuit pilote doit idéalement être capable de générer des impulsions inférieures à la nanoseconde avec des fronts montant et descendant les plus rapides possible. De plus, le raccourcissement de l'impulsion permet d'améliorer la résolution du capteur en autorisant la détection de plusieurs échos lorsque diverses cibles sont localisées dans son champ de vision. D'autre part, l'énergie de l'impulsion transmise définit la portée du dispositif TOF. Par conséquent, la diminution de la largeur d'impulsion impose d'augmenter la puissance optique afin de conserver la portée.

La présente thèse a été effectuée en partenariat avec l'entreprise STMicroelectronics. Le but est de développer un circuit intégré pilote de diode laser à cavité verticale pour la détection laser TOF dans l'électronique embarquée grand public. L'objectif clé est de démontrer la faisabilité d'impulsion laser inférieure à la nanoseconde à une fréquence de répétition de l'ordre de plusieurs centaines de megahertz. De plus, la spécification électrique comporte des exigences ambitieuses et antagonistes. Notamment, l'augmentation de la capacité en courant de pilotage à $200mA$ (*i.e.* accroissement de la puissance optique des impulsions) ainsi que la réduction de la tension d'alimentation du circuit à $2.5V$. Enfin, dans le contexte des appareils mobiles grand public, il y a toujours un besoin de concevoir une solution efficace en puissance et compact.

L'innovation majeure de ce travail est le développement d'une nouvelle topologie de circuit pilote de diode laser. Le circuit proposé est composé d'une structure à pompe de charge afin de satisfaire la contrainte sur la tension d'alimentation. De plus, les phénomènes de coupure lente associés aux diodes laser ont été identifiés comme des facteurs limitants potentiels pour les performances des capteurs TOF directs. En conséquence, l'architecture développée

inclue une fonction spécifique permettant de prévenir de tels effets via une extraction rapide des charges stockées dans la diode laser. Le circuit a été fabriqué avec la technologie CMOS $40nm$ de STMicroelectronics.

Le présent manuscrit examine l'état de l'art des circuits pilotes de diode laser dédiés à la détection TOF. Cette revue met en évidence les avantages et inconvénients de chaque topologie par rapport au cadre de la thèse. Une étude de faisabilité est également présentée pour confronter, en détail, ces différentes architectures. La conception du circuit sur silicium, *i.e.* le dimensionnement au niveau transistor et l'implémentation physique, représente le cœur de la thèse. Par la suite, le manuscrit détaille l'ensemble des mesures réalisées pour évaluer les performances et les limitations du circuit de test fabriqué. Cette caractérisation est principalement fondée sur la mesure d'impulsion laser au moyen d'un photodétecteur rapide et d'une sphère d'intégration. Le résultat fondamental de la thèse est la démonstration d'un courant de pilotage pic de $200.8mA$, correspondant à une impulsion laser de $311ps$, à une tension d'alimentation de $2.5V$ et une fréquence de répétition de $250MHz$. L'inductance parasite, qui représente toujours un problème majeur pour l'électronique rapide, a été identifiée comme étant le principal facteur limitant des performances du circuit. En résumé, les résultats de cette thèse représentent un pas en avant significatif pour les développements futurs de STMicroelectronics.

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Synthèse

Cette section propose une synthèse étendue en français du contenu du manuscrit.

This section presents an extended summary of the manuscript content in French.

Introduction générale

Le principe temps de vol ("TOF : time-of-flight") direct est une technologie de détection qui représente un enjeu majeur dans un nombre croissant d'applications. Cette technique permet de déterminer la distance d'une cible inconnue à partir de la mesure du temps de vol d'une impulsion de lumière. Comme montré en Figure 1, les principales composantes d'un capteur de distance TOF direct sont un émetteur et un détecteur. Le fonctionnement est le suivant. Une impulsion de lumière est émise en direction de la cible d'intérêt. Par la suite, une portion des photons réfléchis sont capturés par le détecteur et le temps de détection est comparé à un temps de référence dérivé de l'impulsion émise. Ainsi, la distance de la cible peut être calculée à partir de la mesure du temps de vol des photons τ et de la célérité de la lumière c ($\sim 3 \times 10^8 m.s^{-1}$),

$$d = \frac{c}{2}\tau \quad (1)$$

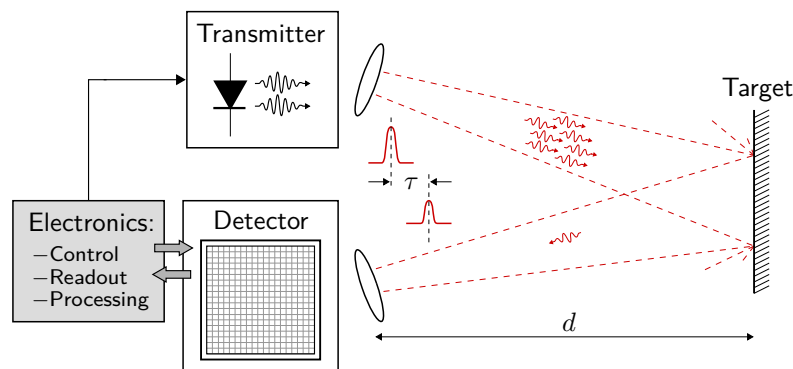


Figure 1 – Schéma fonctionnel d'un capteur TOF direct.

La précision de mesure des capteurs TOF direct dépend directement de la résolution temporelle de l'électronique. Afin d'atteindre une précision spatiale centimétrique, une résolution temporelle de $66ps$ ou une bande passante de $15GHz$ est nécessaire. Étant donné cette exigence, le détecteur est typiquement réalisé à partir de photodiodes à avalanche mono-photoniques ("SPAD : single-photon avalanche diode"). Ces dernières sont des photodiodes à avalanche polarisées en mode Geiger, c'est-à-dire au delà de la tension d'avalanche. De cette manière, elles sont capables de détecter un simple photon avec une résolution temporelle de l'ordre de la centaine de picosecondes.

D'autre part, les caractéristiques de l'impulsion de lumière émise jouent un rôle majeur pour les performances du système:

- La diminution de la largeur d'impulsion permet d'améliorer la précision ainsi que la résolution de la mesure de distance. Idéalement, l'impulsion présente une durée de $100ps$ pour atteindre une précision centimétrique pour une unique mesure.

- L’augmentation de l’énergie d’impulsion étend la portée du dispositif. Autrement dit, réduire la largeur d’impulsion implique d’augmenter la puissance pic de cette dernière afin de maintenir la portée constante.

La forme d’onde idéale correspond donc à un pulse de haute énergie présentant des fronts montant et descendant les plus rapides possible. L’émetteur est ainsi généralement réalisé par un laser à semiconducteur, ou diode laser, émettant dans l’infrarouge proche. Les diodes laser présentent un certain nombre de propriétés avantageuses telles que, une haute bande passante, un faible coût, une largeur spectrale étroite ou encore une faible divergence du faisceau d’émission. En termes simples, une diode laser est une jonction $p - n$ qui émet des photons cohérents lorsqu’elle est pompée par un courant électrique. Aujourd’hui, elles constituent la principale source utilisée pour la détection TOF. Dans le système, la diode laser doit être connectée à un circuit pilote dont la fonction est de générer les impulsions de courant de pilotage.

En raison du fait que les caractéristiques de l’impulsions laser dépendent directement de l’impulsion de courant de pilotage correspondante, le circuit pilote joue un rôle clé au sein du capteur. En effet, il doit être capable de produire les impulsions de courant les plus courtes possible. Afin d’avancer vers ce défi, le but de la présente thèse est d’étudier les circuits pilotes de diode laser pour la génération de pulses inférieurs à la nanoseconde. Ce travail a été effectué au sein de l’entreprise STMicroelectronics. Le but précis est de développer un circuit intégré pilote de diode laser à cavité verticale pour la détection TOF dans l’électronique embarquée grand public. La spécification électrique du circuit est présentée dans le Tableau 1. L’objectif clé est de démontrer la faisabilité d’impulsion laser inférieure à la nanoseconde à une fréquence de répétition de l’ordre de plusieurs centaines de mégahertz. De plus, la spécification électrique comporte des exigences ambitieuses et antagonistes. Notamment, l’augmentation de la capacité en courant de pilotage à $200mA$ (*i.e.* accroissement de la puissance optique des impulsions) ainsi que la réduction de la tension d’alimentation du circuit à $2.5V$. Enfin, dans le contexte des appareils mobiles grand public, il y a toujours un besoin de concevoir une solution efficace en puissance et compact. Ici, une efficacité énergétique de 47% est visée.

Specification	Min.	Typ.	Max.	Unit
Tension d’alimentation	—	2.5	—	V
Courant de pilotage pic	—	200	—	mA
Largeur d’impulsion de courant	250	500	—	ps
Fréquence de répétition	—	200	—	MHz
Efficacité énergétique	47	—	—	%

Table 1 – Spécification électrique du pilote de diode laser.

L'organisation du manuscrit est la suivante :

Le Chapitre 2 passe en revue l'état de l'art des circuits pilotes de diode laser dédiés aux applications TOF. L'objectif est de grouper les topologies existantes et de discuter les avantages et les inconvénients de chaque solution.

Le Chapitre 3 couvre plusieurs considérations de pré-conception. Celles-ci incluent un aperçu de la technologie CMOS $40nm$ ainsi qu'une présentation de la diodes laser et de l'environnement matériel. Ensuite, une étude de faisabilité est réalisée sur la base de ces considérations, le but final étant de proposer une topologie de pilote de diode laser pour satisfaire la spécification électrique.

Le Chapitre 4 est dédié à la conception du circuit pilote intégré avec une focalisation sur le dimensionnement au niveau transistor et la mise en œuvre physique des composants. Le circuit a été fabriqué avec le nœud technologique $40nm$ de STMicroelectronics.

Le Chapitre 5 présente la caractérisation expérimentale et les résultats de mesure de la puce de test fabriquée. Les facteurs limitants des performances sont mis en évidence et des améliorations futures concernant la conception et la caractérisation sont proposées.

Le Chapitre 6 résume les principales contributions de la thèse avec les perspectives. La principale réalisation est le développement d'une architecture innovante de pilote de diode laser compatible avec un fonctionnement basse tension, jusqu'à $2.5V$, et capable de générer des impulsions de courant inférieures à $1ns$ jusqu'à $200mA$. En bref, ce travail représente une étape importante vers le développement de futurs produits par STMicroelectronics.

État de l'art

L'objectif de ce chapitre est d'identifier et de présenter les topologies existantes de circuit pilote de diode laser, en se concentrant exclusivement sur les recherches publiées consacrées aux applications TOF. Chaque topologie est successivement détaillée en termes de caractéristiques clés. Enfin, les avantages et les inconvénients de chaque solution sont soulignés au regard du cadre de la thèse, c'est-à-dire l'électronique mobile grand public. Les topologies ont été divisées en trois catégories principales en fonction des caractéristiques de l'impulsion de pilotage :

- Le pilote de diode laser résonnant à décharge capacitive.
- Le pilote de diode laser mode courant.
- Le pilote de diode laser mode tension.

Les métriques importantes pour l'étude de la littérature sont : la tension d'alimentation, la capacité en courant (courant pic) I_{peak} , la largeur d'impulsion de courant t_{pw} ainsi que la fréquence de répétition f_{sw} . De plus, la

puissance consommée P_{draw} ainsi que l'efficacité énergétique η_{elec} sont discutées dans la mesure du possible.

Le circuit pilote résonnant à décharge capacitive

La topologie résonnante basée sur la décharge capacitive est largement rapportée dans la littérature. L'architecture la plus simple ainsi que le diagramme temporel sont représentés en Figure 2. Le fonctionnement du circuit consiste en des phases répétées de charge et de décharge d'un condensateur de stockage d'énergie C . Plus précisément, le condensateur est d'abord chargé à la tension d'alimentation V_{in} (à travers R_{in}) tandis que la diode laser est éteinte. Par la suite, l'interrupteur M_{sw} est mis en marche pour que le condensateur puisse se décharger complètement à travers la diode laser, générant ainsi un pulse laser. Finalement, M_{sw} est désactivé, ce qui permet au condensateur de se recharger pour le prochain pulse. Étant donné qu'une inductance parasite L_s existe toujours dans le chemin de décharge, la forme de l'impulsion de courant est définie par une réponse RLC série. Par conséquent, la stratégie principale lors de la conception d'une telle structure résonnante consiste à fixer les parties RLC du circuit afin d'obtenir les caractéristiques de pulse souhaitées.

Dans cette topologie, il y a un compromis intrinsèque entre le courant pic et la largeur d'impulsion de courant pour le dimensionnement de la capacité C . En effet, afin de minimiser la largeur d'impulsion, C doit être la plus faible possible. Néanmoins, cela implique en retour une tension d'alimentation élevée afin d'augmenter le courant de pilotage. Ainsi, les topologies résonnantes utilisent souvent une tension d'alimentation de l'ordre de la dizaine de volt. Elles sont donc peu adaptées pour générer des pulses courts en fonctionnement basse tension.

En résumé, les caractéristiques principales de la topologie résonnante sont :

- L'inductance parasite dans le chemin de courant joue un rôle dans le fonctionnement du circuit, c'est-à-dire mise en forme de l'impulsion de courant. Néanmoins, elle doit être minimisée afin d'obtenir des performances maximales.
- Étant donné que la forme d'impulsion est prédéfinie par le réseau RLC, la largeur d'impulsion de déclenchement de l'interrupteur peut être nettement plus longue que l'impulsion laser requise.
- L'énergie du pulse laser est bien contrôlée via la tension d'entrée, éliminant ainsi l'emballement thermique. Cependant, la forme d'impulsion est fixe par conception, ce qui limite la polyvalence du circuit.
- La fréquence de répétition maximale des impulsions est limitée par le temps de recharge du condensateur, ce qui signifie qu'une charge incomplète finirait par entraîner une baisse du courant de pilotage. En effet,

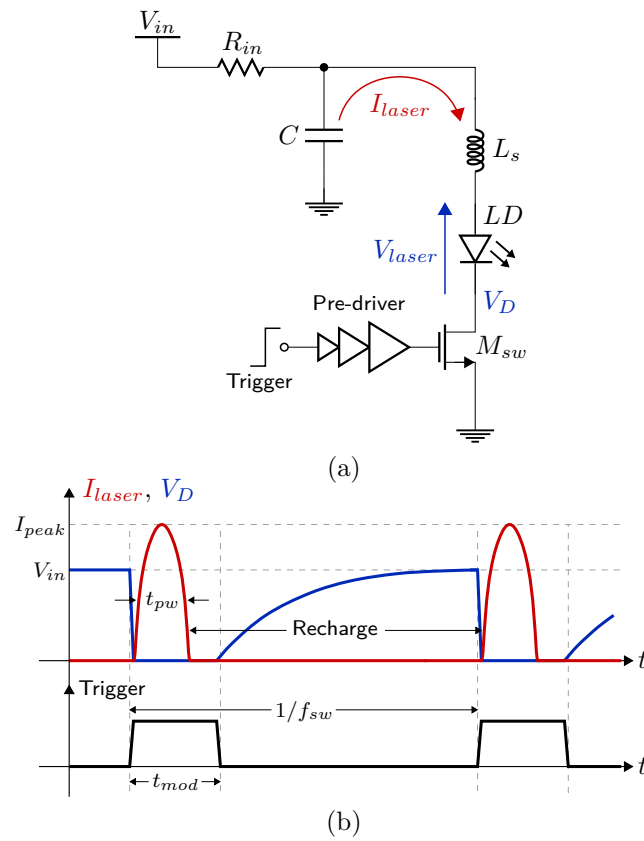


Figure 2 – Topologie résonnante à décharge capacitive : (a) architecture du circuit, (b) diagramme temporel.

les fréquences maximales rapportées ne dépassent pas la dizaine de mégahertz.

- La consommation électrique moyenne depuis la tension d'entrée est directement proportionnelle à la capacité de décharge ($CV_{in}^2 f_{sw}$). Cependant, l'efficacité énergétique ne peut pas être discutée en raison du manque de données dans la littérature publiée. Toutefois, en raison de la tension d'alimentation élevée, il est attendu que l'efficacité soit fortement limitée.

Le circuit pilote mode courant

Le circuit pilote mode courant consiste à piloter la diode laser à travers une source de courant. Cette source peut être implémentée en configuration parallèle ou en configuration série.

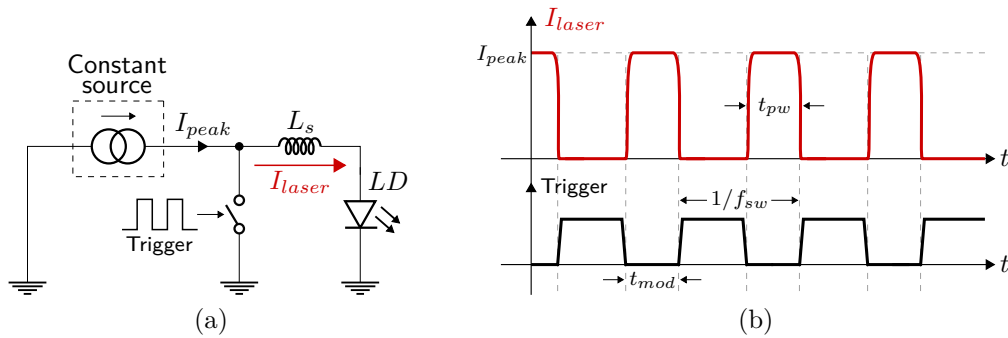


Figure 3 – Topologie mode courant parallèle : (a) architecture du circuit, (b) diagramme temporel.

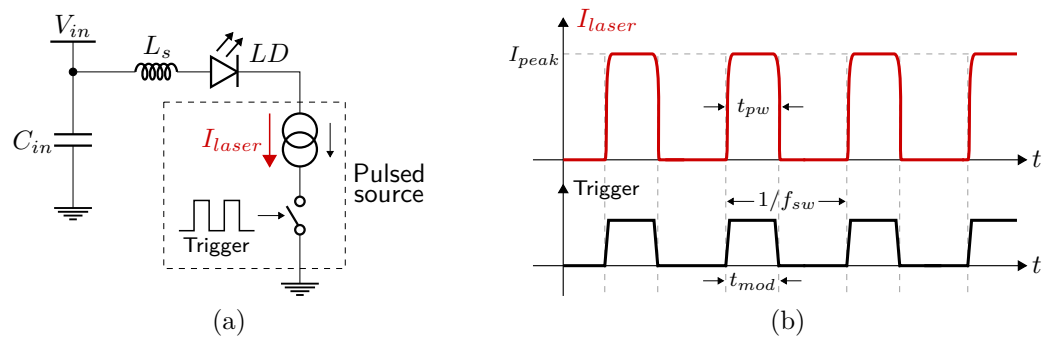


Figure 4 – Topologie mode courant série : (a) architecture du circuit, (b) diagramme temporel.

Dans la configuration parallèle (Figure 3), une source de courant constante fournit le courant pic I_{peak} à la diode laser. Un interrupteur parallèle permet alors de diriger le courant à travers la diode laser ou vers la masse. Typiquement, la source est réalisée par un redresseur demi-pont et une inductance.

L'inductance procure une forte impédance à la source de courant, ce qui permet en retour au circuit de fonctionner à basse tension. De plus, le courant pic peut être bien contrôlé par le redresseur demi-pont à condition que le circuit incorpore un schéma de détection de courant précis et une boucle de rétroaction. Cependant, il est nécessaire que l'inductance soit suffisamment grande pour assurer un courant constant. Dans le cadre d'une solution intégrée, cela nécessite un composant externe qui doit être monté à proximité de la puce, augmentant ainsi la taille et la complexité du système. De plus, sachant que toutes structures inductives présentent une résistance série équivalente, la source de courant constante peut induire des pertes ohmiques importantes qui sont préjudiciables au rendement énergétique du circuit.

Dans la configuration série (Figure 4), la diode laser est pilotée à travers une source de courant pulsée. Cette dernière est généralement implémentée par un transistor fonctionnant en régime saturé, c'est-à-dire en source de courant contrôlée en tension. Le courant pic est donc bien contrôlé au moyen du transistor en saturation. Par conséquent, la forme de l'impulsion laser est entièrement configurable en termes de puissance pic et de durée. Enfin, il n'y a pas de facteur limitant la fréquence de répétition des impulsions. Cependant, il est nécessaire d'assurer une marge de tension suffisante pour le bon fonctionnement de l'étage de source de courant. En conséquence, une tension d'entrée minimale, qui peut être approximée en additionnant la tension directe de la diode laser ciblée et la tension de saturation requise, est nécessaire. Ainsi, un pilote mode courant en configuration série ne semble pas approprié pour un fonctionnement à basse tension. De même, les pertes par conduction aux bornes d'un transistor en saturation vont limiter le rendement énergétique du circuit. Enfin, l'inductance parasite est un facteur de restriction prédominant pour les performances transitoires. Cela nécessite d'optimiser les interconnexions physiques entre la diode laser et le circuit pilote. Une autre solution consiste à augmenter la tension d'entrée de manière à obtenir le temps de montée souhaité. Néanmoins, cela réduirait davantage l'efficacité énergétique en raison des pertes par conduction. En outre, il est important de garder à l'esprit que la tension nominale finie des transistors limite l'augmentation de la tension d'entrée.

Le circuit pilote mode tension

La structure mode tension (Figure 5) consiste à connecter la diode laser en série avec une source de tension V_{in} et un interrupteur M_{sw} . Cette topologie est presque similaire à un pilote résonnant à décharge capacitive, la principale différence étant la valeur relative des composants. Les avantages de la topologie mode tension comprennent le potentiel pour un fonctionnement à basse tension. Par rapport à un pilote mode courant série, l'étage de sortie ne comprend qu'un dispositif de commutation. Ainsi, la tension directe de la diode

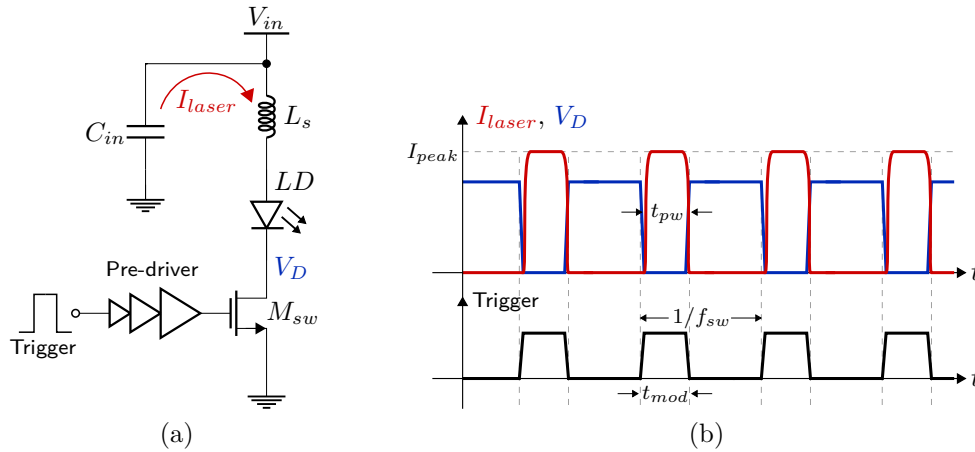


Figure 5 – Topologie mode tension : (a) architecture du circuit, (b) diagramme temporel.

laser n'est pas limitée par la marge de tension de saturation. Dans le même ordre d'idée, l'efficacité énergétique devrait être plus élevée car il n'y a pas de pertes par conduction à travers une source de courant. De plus, contrairement à un pilote résonnant à décharge capacitive, la fréquence de répétition des impulsions n'est pas limitée. Il est cependant admis que la tension directe des diodes laser dépend dans une large mesure de la température. De manière générale, la tension de la diode a tendance à chuter avec l'échauffement de l'appareil. La conséquence directe est une augmentation du courant de pilotage, formant ainsi une rétroaction positive. Dans un pilote résonnant à décharge capacitive, l'emballement thermique est intrinsèquement atténué en raison de l'énergie fixe de l'impulsion définie par le condensateur de stockage, tandis que dans un pilote mode courant, l'énergie d'impulsion est régulée via une source de courant contrôlée. Pour les structures mode tension, le contrôle du courant de pilotage apparaît comme une tâche difficile, nécessitant à la fois un schéma de détection de courant et un contrôle sur la tension d'alimentation. Cela se traduira donc éventuellement par une augmentation de la taille et de la complexité du circuit. Enfin et surtout, de la même manière que pour un circuit mode courant série, les performances transitoires d'un pilote mode tension sont fortement limitées par l'inductance parasite. Ainsi, l'assemblage du circuit doit être optimisé avec un câblage soigné de la diode laser.

Étude de pré-conception et de faisabilité

Ce chapitre couvre plusieurs considérations préalables à la conception. Celles-ci comprennent une présentation de la technologie CMOS 40nm ainsi qu'un aperçu détaillé de la diode laser utilisée et du circuit véhicule. L'objectif final est de réaliser une étude de faisabilité afin de proposer une architecture de circuit pilote adaptée pour répondre aux spécifications électriques.

La technologie CMOS 40nm

La technologie CMOS 40nm est dédiée aux applications à faible consommation d'énergie, telles que le mobile et le sans fil. Grâce à l'option SPAD du processus de fabrication, c'est la technologie actuelle de choix pour développer des produits TOF direct chez STMicroelectronics. Le procédé utilise un substrat de silicium dopé p . L'empilement métallique est composé de sept couches (M1-M7Z), les deux couches supérieures étant plus épaisses pour garantir la distribution de la puissance.

Le nœud technologique 40nm supporte les composants passifs standards, c'est-à-dire les résistances, les condensateurs et les inductances. Une résistance peut être réalisée par des régions actives $n+$ ou $p+$, par des caissons dopés n ou p ou encore par des couches de polysilicium ou de métal. De la même manière, plusieurs structures de condensateurs sont disponibles : métal-oxyde-semiconducteur (MOS), métal-oxyde-métal (MOM) ainsi que métal-isolant-métal (MIM). Enfin, une inductance peut être fabriquée à partir de la pile métallique. De manière générale, plusieurs couches métalliques doivent être utilisées afin de réduire la résistance série du composant et donc d'obtenir un facteur de qualité raisonnable.

Les dispositifs de commutation (actif) dans la technologie 40nm sont les MOSFETs classiques à canal n (NMOS) ou canal p (PMOS). Ceux-ci sont disponibles à différentes valeurs de tension nominale en fonction de l'épaisseur de l'oxyde de grille et de la longueur du canal.

La technologie de diode laser

La diode laser employée dans le cadre du projet doctoral est un réseau de sept VCSELs connectés en parallèle sur la même puce. Tous les VCSELs ont une électrode de cathode commune. L'utilisation de plusieurs VCSELs sur une puce n'affecte pas les caractéristiques du laser, ce qui signifie que les performances sont principalement définies par le laser individuel. Essentiellement, le courant et la puissance d'un réseau s'adaptent simplement au nombre d'émetteur connectés en parallèle tandis que la tension reste inchangée.

Le VCSEL a été fourni par un fabricant externe. Ce dispositif a été spécifiquement choisi car il était déjà utilisé pour le développement de produits au sein de STMicroelectronics. Ce laser est d'abord spécifié pour un courant de pilotage de 120mA. Ainsi, l'objectif de conception est d'étendre le courant à 200mA avec des impulsions de courant inférieures à 1ns.

Afin de concevoir le circuit de pilotage, nous avons construit un modèle électrique du VCSEL. Sachant que seule les données de mesure statique $I - V$ étaient disponibles, le modèle a été développé à partir d'un ajustement de courbe basé sur l'équation de diode de Shockley. Le processus d'ajustement de courbe a été effectué avec Matlab *optimisation toolbox*. Le schéma équivalent

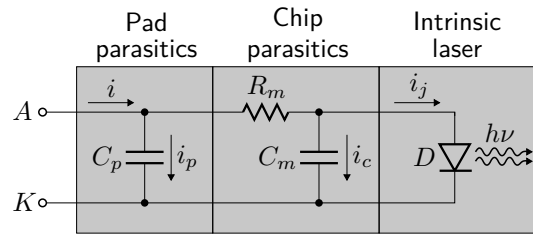


Figure 6 – Modèle électrique du VCSEL.

du VCSEL est présentée en Figure 6. La résistance R_m est la résistance série et représente avec la diode D la caractéristique statique de la diode laser. D'autre part, les capacités C_p et C_m sont les parasites associés respectivement au plot de contact et à la jonction. Il convient de garder à l'esprit que ce modèle présente des limitations importantes. Premièrement, il ne capture pas le comportement intrinsèque du VCSEL régi par les équations de balance. Par conséquent, le modèle permet seulement de simuler le courant de pilotage circulant à travers le VCSEL, mais ne fournit pas l'impulsion laser correspondante. De plus, la dépendance thermique des paramètres du modèle n'est pas prise en compte. En règle générale, la tension directe du VCSEL aura tendance à diminuer avec l'augmentation de la température. Ainsi, le modèle n'est pertinent qu'autour de la température ambiante, c'est-à-dire la température à laquelle les mesures $I - V$ ont été effectuées.

Le circuit véhicule

Afin de bénéficier d'un environnement matériel complet et fonctionnel, le circuit véhicule STVC a été réutilisé comme base pour la conception. Une vue d'ensemble de l'assemblage est fournie en Figure 7. Le STVC est un capteur de télémétrie tout-en-un conçu par STMicroelectronics. Il incorpore un circuit intégré silicium monté sur un substrat avec la puce VCSEL et des condensateurs céramiques multi-couches (MLCC). L'ensemble de l'assemblage est logé dans un module compact avec des optiques de couplage.

Dans le but de prendre en compte l'environnement matériel pour la conception. Un modèle électrique équivalent a été construit pour les interconnexions physiques entre le circuit pilote et le VCSEL ainsi que pour le réseau de distribution de puissance. Cette étape vise à avoir un environnement de simulation complet afin de correctement dimensionner le circuit et évaluer ses performances. Le modèle de l'environnement matériel a été mis en œuvre en utilisant des formules théoriques pour le calcul des inductances, capacités et résistances. Le résultat clé de cette démarche est que l'inductance et la résistance globales dans le chemin du VCSEL sont respectivement égales à $1.95nH$ et $248m\Omega$.

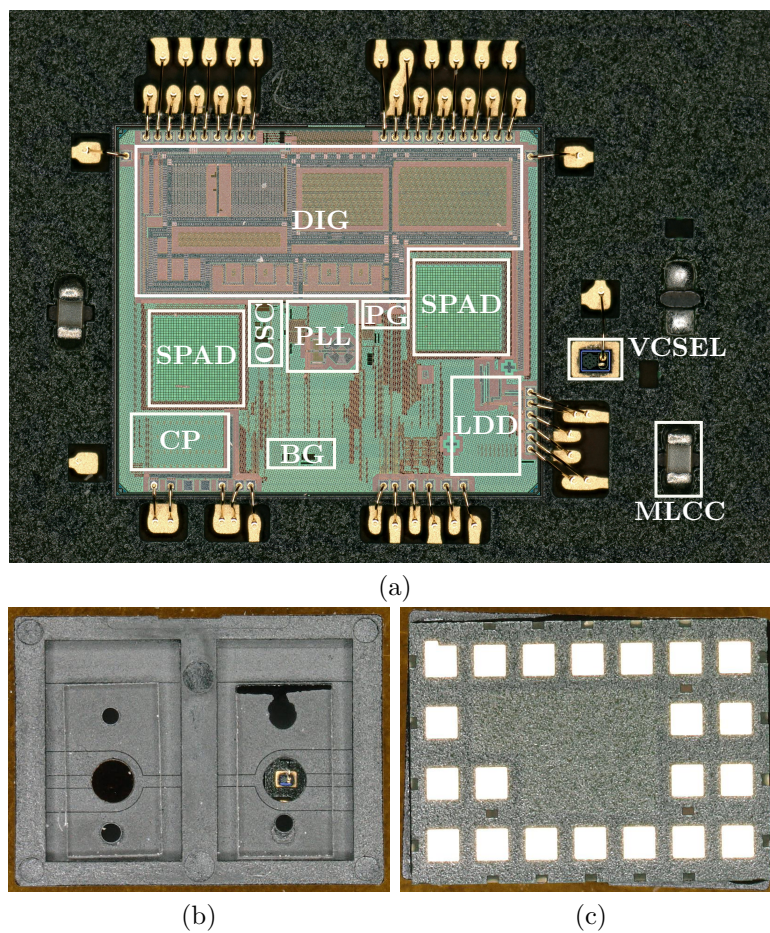


Figure 7 – Circuit véhicule : (a) puce en silicium, (b) Vue du dessus du module, (c) Vue du dessous du module.

Étude de faisabilité

Les architectures de pilote de diode laser sont évaluées par simulation avec la technologie CMOS 40nm de STMicroelectronics et le modèle électrique du VCSEL. Les conditions de fonctionnement de la simulation sont alignées sur les spécifications techniques. Les valeurs des parasites ont été choisies pour être cohérentes avec celles calculées sur le circuit véhicule.

Dans la topologie résonnante à décharge capacitive, la forme de l'impulsion laser est fixe pour une conception donnée. En conséquence, une telle structure est inadéquate lorsque la configuration de la largeur d'impulsion est requise. La faisabilité peut être rapidement évaluée. Pour une largeur d'impulsion de courant inférieure à 1ns, un condensateur de stockage de 114pF est nécessaire. Cela implique une tension d'alimentation minimum de 4V afin d'atteindre le courant spécifié de 200mA. Ainsi, un circuit résonnant à décharge capacitive apparaît comme une solution complexe compte tenu du niveau de tension d'alimentation requis.

Dans le pilote mode courant parallèle, une inductance est nécessaire pour construire la source de courant constante. Ceci n'est pas compatible avec le facteur de forme du circuit véhicule et nécessiterait une refonte complète du substrat. De la même manière, intégrer l'inductance sur silicium conduirait à une consommation de surface trop importante.

Le pilote mode courant série est limitée par la marge de tension de saturation. En effet, afin de satisfaire la condition de saturation en régime permanent pour un courant de 200mA, une tension d'alimentation du pilote d'au moins 4V est requise.

Le pilote mode tension est intrinsèquement supérieur en termes de capacité en courant et d'efficacité énergétique par rapport au circuit mode courant série. La tension d'alimentation requise pour atteindre un courant pic de 200 mA est estimée 3.57V.

Il est clairement prouvé que, quelle que soit l'architecture du circuit, l'objectif de conception basse tension (2.5V) n'est pas réalisable sans un circuit intermédiaire permettant une élévation de tension. Afin de se conformer à l'exigence entièrement intégrée, l'élévation de tension serait réalisée par un convertisseur DC-DC à capacité commutée. Le principal inconvénient de cette solution est que les convertisseurs capacitifs sont limités en termes d'efficacité et conduisent à une consommation importante de la surface du silicium (basée sur l'implémentation précédente du pilote de diode laser par STMicroelectronics). Ainsi, il a été choisi de se diriger vers une mise en œuvre différente pour surmonter la contrainte de basse tension.

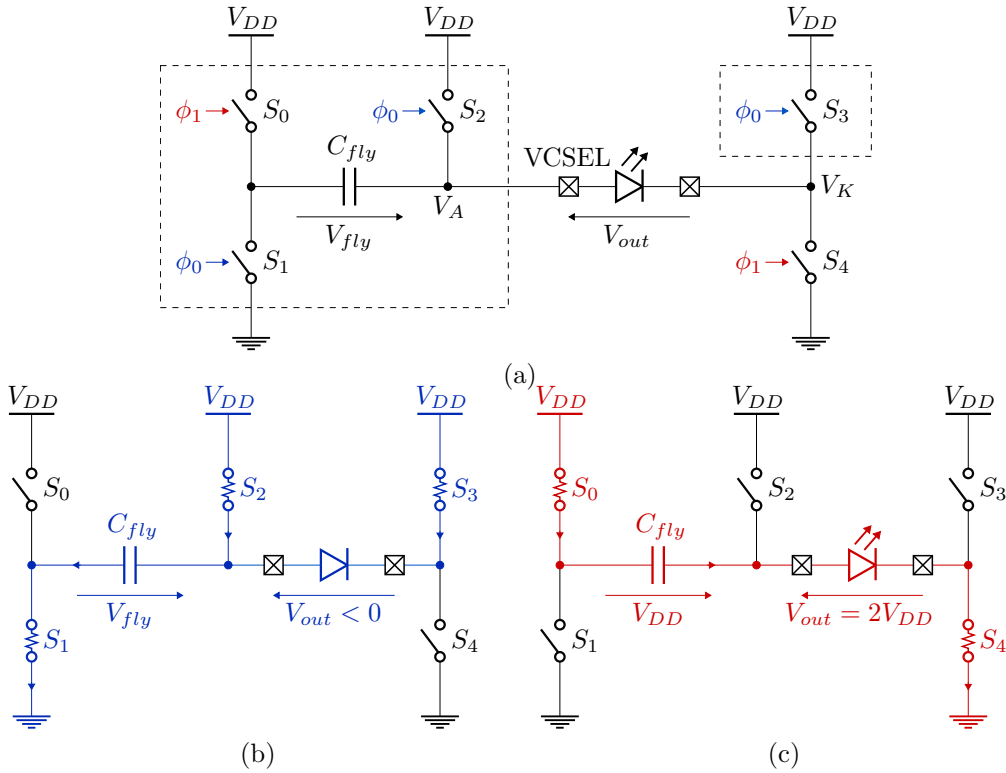


Figure 8 – Architecture proposée : (a) assemblage des interrupteurs, (b) phase de charge ϕ_0 , (c) phase de décharge ϕ_1 .

Architecture proposée

Cette section présente en détails les principales caractéristiques de l'architecture de pilote de diode laser proposée. Une structure de circuit basée sur un transfert de charge capacitif entre une capacité de pilotage C_{fly} et la diode laser a été choisie. L'architecture $S_0 - S_4$ est représentée en Figure 8. Il est important de noter que le but de C_{fly} n'est pas de se décharger complètement à travers le laser comme c'est le cas pour un pilote résonnant à décharge capacitive. De cette manière, l'architecture proposée peut être considérée comme une topologie mode tension modifiée basée sur une décharge capacitive.

Le diagramme temporel correspondant est illustré en Figure 9.

Les spécificités de l'architecture sont:

- Une élévation de tension capacitive pour augmenter le courant de pilotage tout en garantissant un fonctionnement à basse tension.
- Un schéma d'extraction des porteurs de charge pour prévenir les transitoires lents à la coupure de la diode laser et ainsi améliorer le fonctionnement à impulsions courtes.

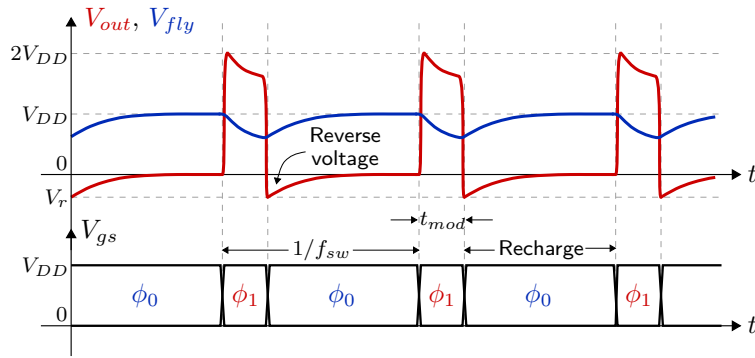


Figure 9 – Diagramme temporel de l'architecture proposée.

Élévation de tension capacitive

Le principe de l'augmentation de tension capacitive est reproduit à partir d'un brevet de STMicroelectronics. Dans les termes les plus simples, il reproduit le principe d'élévation de tension exploité par un convertisseur capacitif. La principale différence est que l'objectif n'est pas d'obtenir un niveau de tension de sortie régulé.

L'opération est la suivante. Dans la première phase de fonctionnement ϕ_0 , C_{fly} est chargée à V_{DD} à travers S_1 et S_2 . Dans la deuxième phase ϕ_2 , un chemin de décharge est créé pour la capacité à travers la diode laser. Plus précisément, la plaque inférieure de C_{fly} est poussée à V_{DD} par S_0 . En conséquence, le nœud d'anode V_A de la diode laser peut monter jusqu'à $2V_{DD}$ en raison de la continuité de tension à travers un condensateur. Simultanément, le nœud de cathode V_K est poussé à la masse. En conséquence, une impulsion de tension doublée est appliquée à la charge du circuit. Étant donné que le courant pilote s'établit en fonction de la tension de charge V_{out} , un tel principe d'augmentation de tension permet d'augmenter la capacité en courant du circuit.

Le capacité de pilotage C_{fly} est le composant clé de la structure du circuit car elle détermine l'énergie de l'impulsion de courant de pilotage. Évidemment, étant donné que le condensateur stocke une charge finie, la largeur d'impulsion de courant est intrinsèquement limitée. Par conséquent, une telle architecture de circuit est destinée à un fonctionnement à impulsions courtes. De plus, pour permettre une solution totalement intégrée et éviter d'ajouter plus d'inductance parasite dans le trajet du courant, le condensateur doit être implémenté sur silicium.

Extraction de charge

Sur la base des caractérisations précédentes de pilote de diode laser par STMicroelectronics, une traînée optique dans le transitoire de désactivation de l'impulsion laser a déjà été observée. Un tel phénomène se traduit par

une augmentation substantielle du temps de descente apparent de l'impulsion laser et constitue par conséquent un scénario indésirable pour la détection TOF direct. Par conséquent, l'un des objectifs de la thèse était d'étudier ces problèmes.

Au-dessous du courant de seuil d'émission laser, la réponse de désactivation des VCSELs peut être limitée par la diffusion de porteurs et les phénomènes de brûlage de trous spatiaux. La dynamique sous-seuil des VCSELs est régie par la durée de vie spontanée des porteurs de charge, qui est de l'ordre de la nanoseconde. Ce lent processus de recombinaison est susceptible d'empêcher le laser de s'éteindre rapidement, sous la forme d'une traînée optique dans l'impulsion laser. Dans le même ordre d'idée, le brûlage de trous spatiaux, dû à la redistribution spatiale des porteurs de charge, peut entraîner des pulsations secondaires plusieurs centaines de picoseconde après le front descendant de l'impulsion laser.

Ces phénomènes sont principalement liés au stockage des porteurs de charge. Ils peuvent ainsi être supprimés via une fonction de circuit permettant une extraction rapide des charges présentes dans la diode laser. Par conséquent, la topologie de pilote proposée incorpore l'interrupteur S_3 connecté entre V_K et V_{DD} . Le but de S_3 est de pousser V_K à V_{DD} au moment de l'extinction de la diode laser. En raison de la décharge partielle de la capacité de pilotage, une légère tension négative est appliquée aux bornes de la charge. La tension de charge V_{out} est maintenue dans la plage négative pendant le temps d'arrêt du VCSEL. Par la suite, une fois que C_{fly} est complètement chargée, la tension de charge est nulle.

Conception du circuit intégré

Ce chapitre détaille le flot de conception de la topologie de pilote de diode laser proposée dans le chapitre précédent. Le circuit est fabriqué à l'aide de la technologie CMOS 40nm de STMicroelectronics. Dans un premier temps, une vue complète du système est fournie. Ensuite, le dimensionnement au niveau transistor de chaque sous-bloc est présenté. De plus, les considérations concernant la disposition physique des composants sont également soulignées tout au long du chapitre. Enfin, une vérification post-implantation est effectuée pour évaluer les performances du circuit avant mesures.

Vue globale

Le pilote de VCSEL a été implémenté dans le circuit véhicule STVC. Une vue d'ensemble du système avec les principaux blocs de construction est représentée sur la Figure 10. Le générateur d'impulsion ("pulse generator")

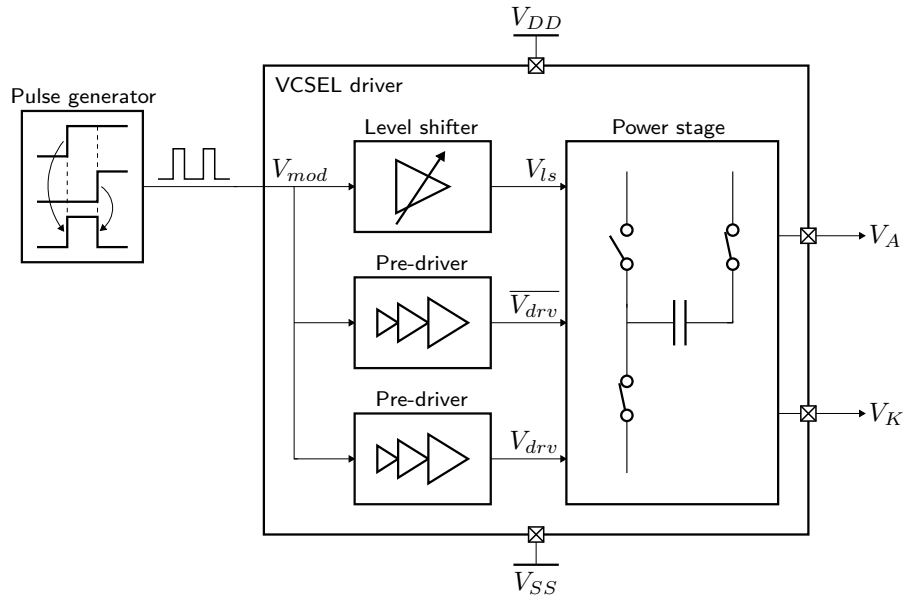


Figure 10 – Vue d'ensemble du système.

est réutilisé pour fournir le signal de modulation V_{mod} de la diode laser. La fréquence et la largeur d'impulsion de V_{mod} sont respectivement notées f_{sw} et t_{mod} .

Les principaux blocs de construction du circuit qui sont conçus tout au long de ce chapitre sont :

- L'étage de puissance.
- Un circuit de changement de niveau de tension ("level-shifter").
- Les circuits pré-pilotes.

L'architecture au niveau transistor de l'étage de puissance est représentée sur la Figure 11a. Nous avons implémenté l'assemblage des commutateurs (décrit dans le chapitre précédent) à partir de transistors PMOS et NMOS de la technologie CMOS 40nm. Notez que le nœud de commutation de la plaque inférieure de C_{gly} a été exploité pour piloter la grille du NMOS M_4 . De cette façon, il n'était pas nécessaire d'ajouter un troisième circuit pré-pilote pour M_4 , économisant ainsi de la surface de silicium. De plus, le commutateur M_2 a été réalisé par une paire de MOSFET partageant un potentiel de bulk flottant.

La séquence de synchronisation proposée des signaux de pilotage est illustrée dans la Figure 11b. Le circuit de changement de niveau génère un signal V_{ls} [$V_{DD} - 3.6V$] qui assure l'activation complète de NMOS M_2 . Le niveau de tension de 3.6V correspond à la tension nominale des MOSFET 3.3V dans le nœud technologique 40nm. Les pré-pilotes augmentent la force du signal V_{mod} avant de le transmettre à l'étage de puissance, ce qui donne les signaux V_{drv} et $\overline{V_{drv}}$ [$0 - V_{DD}$]. Chaque sous-bloc est alimenté par les broches d'alimentation

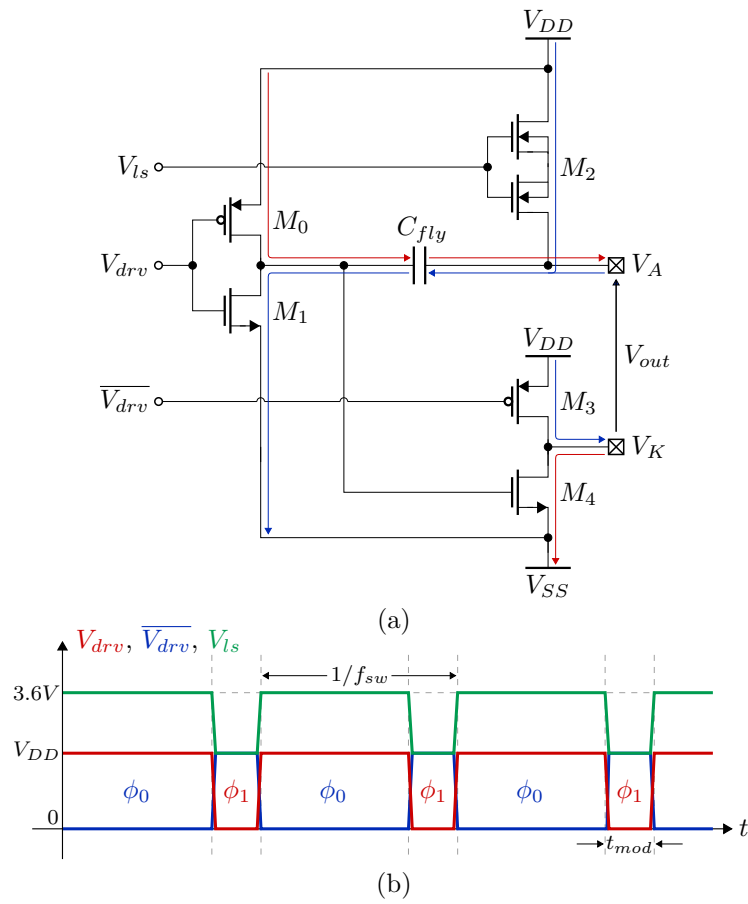


Figure 11 – Implémentation de l'étage de puissance : (a) architecture niveau transistor, (b) diagramme temporel.

et de masse dédiées du pilote, c'est-à-dire V_{DD} et V_{SS} .

Détails de conception

La capacité C_{fly} est l'élément clé du circuit et elle a donc été dimensionnée en premier. Pour cela, le courant pic et la largeur d'impulsion de courant ont été extraits pour des valeurs croissantes de C_{fly} . Les résultats de simulation (obtenus en opération typique) ont montré que la dérivée du courant pic tend rapidement vers zéro à mesure que la capacité augmente. À partir d'une valeur de $200pF$, un incrément de $10mA$ du courant pic nécessite au moins une augmentation de 50% de C_{fly} , quelle que soit la résistance de canal des MOSFETs. Étant donné qu'une surface de silicium limitée est allouée au pilote, la consommation de surface importante des structures de condensateur sur puce doit être prise en compte. Par conséquent, la valeur cible du condensateur a été choisie autour de $200pF$, comme compromis entre le courant pic et la surface de silicium. En outre, il permet une durée d'impulsion de courant jusqu'à $2ns$, ce qui convient par rapport à la spécification.

Afin d'implémenter C_{fly} , la technologie CMOS $40nm$ propose plusieurs structures : MOS, MOM et MIM. Pour la réalisation, il est indispensable que la densité capacitive soit la plus élevée possible. De plus, les capacités parasites doivent être minimales afin de ne pas détériorer les performances du circuit pilote. Finalement, la capacité doit être indépendante de la tension étant donné que C_{fly} fonctionne en cycles répétés de charge et décharge. En conclusion, les dispositifs MOS ont été considérés comme inadéquats pour la mise en œuvre de C_{fly} . En effet, puisqu'une électrode est le silicium, il y a une grande capacité parasite. Ensuite, le condensateur MOM a été exclu en raison de sa densité limitée. En conséquence, le dispositif MIM est apparu comme le meilleur compromis possible entre densité capacitive et parasites malgré sa variation plus élevée au regard du processus de fabrication.

Du point de vue de la disposition physique, nous avons conçu la capacité MIM C_{fly} à partir de 36 cellules unitaires parallèles disposées en carré. La capacité typique obtenue est de $178pF$, ce qui est proche des $200pF$ ciblés. De plus, la stratégie de disposition est de garder l'espace sous l'électrode inférieure vide afin de minimiser les couplages parasites vers le substrat. La capacité résultante entre la plaque inférieure et le substrat a été extraite par simulation post-implantation à environ $940fF$.

Par la suite, le dimensionnement de la largeur de canal des MOSFETs de puissance formant les chemin de courant de charge et de décharge de C_{fly} (M_0 , M_1 , M_2 et M_4) a été mené. Ces transistors fonctionnent tous dans la région triode.

En termes de mise en œuvre, les MOSFETs pilotant la plaque inférieure de C_{fly} , c'est-à-dire le PMOS M_0 et le NMOS M_1 , ont été réalisés par des MOSFETs $2.5V$. Étant donné que les tensions à leurs bornes commutent

entre V_{SS} et V_{DD} , ils peuvent être dimensionnés avec la longueur de canal minimale ($0.27\mu m$). Le MOSFET M_2 est connecté à la plaque supérieure du condensateur volant. Puisque ce potentiel devrait augmenter jusqu'à $2V_{DD}$, le NMOS inférieur a été réalisé par un MOSFET 3.3V. D'autre part, le NMOS supérieur connecté entre V_{DD} et le nœud flottant de bulk a été dimensionné avec la longueur de canal minimale. Enfin, le drain de NMOS M_4 est connecté au nœud de commutation V_K . Comme ce dernier est sujet au dépassement de tension (dû à l'inductance parasite), ce MOSFET a été implémenté par un dispositif 3.3V afin de garantir la fiabilité du circuit.

Dans la phase ϕ_0 , C_{fly} est chargée à travers la résistance de canal de M_1 et M_2 . Sachant qu'une charge incomplète de C_{fly} conduirait à terme à une baisse du courant de pilotage, le temps de recharge du condensateur est le principal facteur limitant la fréquence de répétition des impulsions. Ainsi, des MOSFETs larges avec une faible résistance de canal doivent être employés de manière à minimiser la constante de temps de charge RC de C_{fly} . Dans la phase ϕ_1 , C_{fly} se décharge à travers la charge et la résistance de canal de M_0 et M_4 . Étant donné que toute chute de tension résistive dans le chemin de décharge a tendance à limiter le courant pic, M_0 et M_4 devraient être aussi larges que possible. Néanmoins, comme le pilote vise une fréquence de répétition des impulsions élevée, jusqu'à plusieurs centaines de mégahertz, les pertes dynamiques dues à la commutation des capacités de grille ne peuvent être ignorées lors du dimensionnement des MOSFETs. Par conséquent, un dimensionnement optimal nécessite une analyse de compromis entre la capacité en courant, la fréquence de répétition et l'efficacité énergétique du circuit pilote.

A la suite d'une simulation, on peut voir que l'efficacité énergétique atteint un maximum entre $2000\mu m$ et $3000\mu m$. En revanche, le courant pic augmente continuellement avec l'augmentation de la largeur, mais avec une dérivée décroissante (en raison du fait que la résistance du canal varie avec l'inverse de la largeur). Ces courbes mettent clairement en évidence le compromis entre la capacité en courant et les pertes de puissance.

Une valeur de $800\mu m$ a été choisie pour M_2 car elle permet à C_{fly} de se charger jusqu'à 95% de la tension d'alimentation. D'autre part, M_0 et M_4 ont été dimensionnés avec une largeur de $1800\mu m$ comme un compromis entre efficacité, courant pic et surface.

Concernant le dimensionnement de la largeur du canal de M_3 , la résistance du canal doit être aussi faible que possible. En d'autres termes, M_3 doit agir comme une résistance à faible impédance afin de garantir un transitoire d'arrêt laser rapide. Ainsi, le PMOS M_3 a été implémenté en tant que MOSFET 3.3V (longueur de canal de $0.44\mu m$) avec une largeur de canal de $480\mu m$. Cette valeur spécifique a été choisie sur la base de préoccupations de disposition physique afin de prendre en compte les contraintes de surface et de routage.

Les dimensions des MOSFETs de puissance sont récapitulées dans le Tableau

Transistor	Largeur (μm)	Longueur (μm)	Resistance (Ω)
PMOS M_0	1800	0.27	2
NMOS M_1	600	0.27	2
NMOS M_2	800	0.27 + 0.55	8
PMOS M_3	480	0.44	10
NMOS M_4	1800	0.55	3

Table 2 – Dimensions des MOSFETs de puissance.

2.

Dans les circuits CMOS, la commande de grandes charges capacitives est généralement effectuée par des buffers. Ceux-ci sont réalisés par une chaîne d'inverseurs pour lesquels la largeur du canal des MOSFETs est augmentée vers la charge d'un facteur constant. De cette manière, la capacité de pilotage peut être progressivement incrémentée des blocs logiques à l'étage de puissance.

Les buffers pré-pilotes ont été réalisés à partir de MOSFET 2.5V. Ceux-ci sont plus adaptés pour piloter des impulsions inférieures à la nanoseconde par rapport aux dispositifs 3.3V en raison de leur capacité de grille inférieure. La cellule standard 2.5V disponible dans le kit de conception technologique a été utilisée comme base pour la conception. Le rapport de largeur entre les transistors PMOS et NMOS est 1.3, qui est fixé par la technologie.

Le facteur de taille entre chaque étage a été sélectionné par simulation. Ce dernier a été fixé à 3 car il conduit à une propagation satisfaisante d'une impulsion de 250ps

Afin de générer le signal de pilotage V_{ls} , un pilote d'horloge avec une tension de sortie pompée a été utilisé.

Considérations physiques

Les considérations physiques s'appliquent principalement aux MOSFETs formant l'étage de puissance du pilote, c'est-à-dire ceux assurant la conduction de courant élevé.

Étant donné que chaque composant est couplé au substrat, la disposition physique a été effectuée de manière à minimiser le bruit de commutation. En effet, ce bruit électrique peut être à l'origine d'un phénomène de verrouillage ("latch-up") et ainsi conduire à une défaillance du circuit. Pour prévenir ces problèmes, l'approche courante pour protéger un circuit bruyant ou sensible au bruit est de l'entourer avec des implants $p+$ ou $n+$, également appelés anneaux de garde. De cette manière, un chemin à faible impédance vers la masse ou une source de tension de référence est créé pour des injections de charges parasites. De plus, comme les anneaux de garde maintiennent idéalement le substrat et les différents caissons à un potentiel fixe, il s'agit d'une stratégie

efficace pour prévenir les problèmes de verrouillage. De plus, les MOSFETs formant l'étage de puissance du pilote ont été conçus comme des structures inter-digitées. La grille est ainsi divisée en plusieurs doigts parallèles avec une disposition alternée des contacts de source et de drain. Cette stratégie permet aux transistors larges de présenter un rapport hauteur/largeur raisonnable, facilitant ainsi leur placement ainsi que leur interconnexion au niveau de la puce. En plus, étant donné que deux doigts parallèles successifs partagent des contacts de drain ou de source communs, les dispositifs multi-doigts sont plutôt des structures compacts.

La pile métallique de la technologie CMOS 40nm de STMicroelectronics présente sept couches (M1-M7Z). Rappelons que les deux couches supérieures (M6Z et M7Z) sont plus épaisses et sont dédiées à la distribution d'énergie. De plus, les couches métalliques voisines sont interconnectées à l'aide de vias (de CO à VIA6Z). Typiquement, les couches métalliques présentent une résistance série parasite et une capacité parallèle. Ces parasites peuvent avoir un impact néfaste sur les performances globales du circuit. D'une part, la résistance métallique dans le chemin de puissance induit une chute de tension qui diminue la capacité en courant du circuit. D'autre part, le couplage capacitif entre des pistes métalliques adjacentes augmente les pertes par commutation, réduisant ainsi le rendement énergétique. Enfin, la capacité parasite augmente également le retard de propagation des signaux, affectant ainsi leur synchronisation. En conséquence, plusieurs couches métalliques parallèles et de nombreux vias ont été utilisés pour former le chemin de puissance. De cette manière, la résistance du métal peut être minimisée. En même temps, l'utilisation de plusieurs couches limite la densité de courant, atténuant ainsi l'électromigration des métaux. De plus, les parasites ont été réduits en appliquant les règles d'espacement minimales afin de maintenir la longueur des chemins métalliques aussi courte que possible.

Implémentation physique

La vue de l'implémentation physique du circuit pilote de VCSEL est présentée en Figure 12. La majeure partie de la surface est occupée par la capacité C_{fly} . Les sous-circuits assurant la génération des signaux de pilotage, c'est-à-dire les pré-pilotes et le circuit de changement de niveau, ont été placés en haut du circuit. Les signaux de pilotage sont envoyés à l'étage de puissance à l'aide de pistes métalliques M6Z. Enfin, les MOSFETs de puissance ont été connectés aux plots de contact via de grandes routes métalliques M7Z.

Étant donné que des courants transitoires rapides sont tirés de l'alimentation, un condensateur de découplage sur puce est obligatoire par conception. Son rôle est d'atténuer les fluctuations de la tension d'alimentation dues aux chutes Ri et $L\frac{di}{dt}$ à travers le réseau de distribution d'énergie. Le condensateur doit être suffisamment grand pour que V_{DD} et V_{SS} fluctuent à l'unisson. En termes

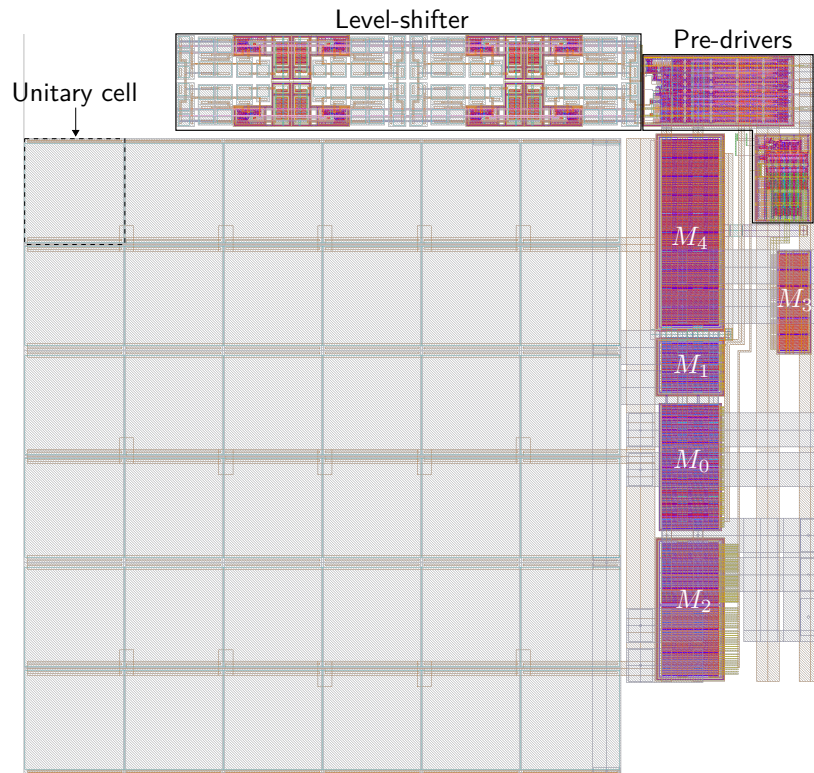


Figure 12 – Implementation physique du circuit pilote.

de mise en œuvre, un transistor NMOS configuré en condensateur convient à des fins de découplage. Comme il fonctionne en inversion forte, une densité capacitive élevée peut être obtenue. Ainsi, la capacité de découplage sur puce est construite à partir de condensateurs NMOS à oxyde épais. Afin d'augmenter encore la densité, un condensateur MIM a été empilé et connecté en parallèle des dispositifs NMOS. La capacité de la cellule unitaire est d'environ $8pF$. Afin d'obtenir la plus grande capacité possible, cette cellule a été distribuée afin de remplir la zone restante disponible dans la puce. Au final, un condensateur de découplage d'environ $1nF$ a été intégré.

Validation post-implantation

Le circuit pilote de VCSEL conçu a été simulé avec les circuits adjacents de l'environnement matériel du STVC. Il s'agit notamment du générateur d'impulsion, de l'unité de sécurité laser et des plots de contact métalliques. Afin de prendre en compte les parasites du routage métallique, une extraction post-implantation de l'étage de puissance du circuit a été réalisée. De cette manière, les résistances et capacités parasites peuvent être incorporées dans la simulation.

Les résultats de simulation ont montré que le circuit était fonctionnel dans l'environnement matériel. Premièrement, les signaux de commande sont

t_{mod}/f_{sw}	1ns/100MHz	500ps/250MHz	250ps/250MHz
I_{peak} (mA)	222.6	207.5	193.3
t_{pw} (ps)	972	468	230
t_r (ps)	188	188	189
t_f (ps)	94	92	95
$\frac{\Delta I_{laser}}{\Delta t}$ (mA.ps ⁻¹)	0.94	0.88	0.81
P_{draw} (mW)	111.7	140	78.6
η_{elec} (%)	55	48.7	35.5

Table 3 – Résultats de simulation post-implantation.

raisonnablement synchronisés lorsqu'ils sont envoyés à l'étage de puissance. La tension d'ondulation associée à V_{DD} est inférieure à $100mV$, ce qui signifie qu'un condensateur de découplage suffisant a été intégré. En outre, la forme d'onde de tension de la capacité de pilotage est cohérente avec le fonctionnement prédit du circuit, c'est-à-dire des cycles de charge et de décharge répétés. En raison de la structure d'élévation de tension capacitive, la forme d'onde de la tension de charge représente une impulsion rapide avec un temps de montée de $50ps$ et une magnitude d'environ $2V_{DD}$. Ensuite, la tension est maintenue dans la plage négative pendant le temps d'arrêt du VCSEL, ce qui est l'impact attendu de la fonction d'extraction de charge de la diode laser. La forme d'onde de l'impulsion de courant présente un pic à $210mA$ et une durée de $468ps$, atteignant ainsi l'objectif de conception. Le temps de montée du courant simulé est d'environ $190ps$. Ce dernier est principalement fixé par l'inductance parasite dans le trajet du courant à travers le VCSEL.

Une vue d'ensemble des résultats de simulation post-implantation est présentée dans le Tableau 3.

Caractérisation expérimentale

Ce chapitre présente la banc expérimentale et les résultats de mesure de la topologie de pilote VCSEL proposée et fabriquée dans la technologie CMOS $40nm$ de STMicroelectronics. Le but ici est d'évaluer le fonctionnement, les performances ainsi que les limites du circuit conçu. Le processus expérimental a été divisé en deux parties. Dans un premier temps, un banc de mesure électrique a été mis en place, dont le but était de caractériser l'impulsion de courant de pilotage à travers une charge résistive. Étant donné qu'il n'y a pas d'exigence spécifique de sécurité laser associée à cette expérience, le banc électrique a permis de vérifier rapidement le bon fonctionnement du pilote. Par la suite, un banc de mesure optique a été mis en place afin d'évaluer les caractéristiques de l'impulsion laser.

Afin d'effectuer les tests, la puce fabriquée a été montée sur une carte (PCB) de caractérisation dédiée. Étant donné que le signal de modulation de la diode laser est généré sur la puce, une carte microcontrôleur STM32 a été connectée au PCB de caractérisation via un bus de communication I^2C . De cette façon, la largeur d'impulsion de modulation t_{mod} (125ps de pas temporel) et la fréquence f_{sw} peuvent être configurées via un script Python. Enfin, la puce a été alimentée via une alimentation externe pour permettre de mesurer le courant moyen consommé par le circuit pilote. Cela a permis de caractériser la consommation et le rendement du circuit.

La puce de test a été évaluée expérimentalement avec une plage de tension semblable à celle d'un produit, entre 1.8V et 2.8V. Également, toutes les mesures ont été effectuées à température ambiante.

Le défi crucial lié à la caractérisation expérimentale consiste à capturer avec précision la propagation transitoire des impulsions inférieures à la nanoseconde. Afin de garantir la fiabilité des mesures dans le domaine temporel, l'équipement de test doit présenter une bande passante supérieure à la bande passante $-3dB$ du signal d'intérêt. Par conséquent, les instruments de mesure ont été sélectionnés en fonction de ces contraintes de bande passante et de précision.

Tout au long de ce chapitre, les performances extraites ont été comparées, dans la mesure du possible, à la simulation post-implantation ("PLS : post-layout simulation").

Vérification électrique

Dans le cadre des mesures électrique, une sonde de tension différentielle Tektronix P7720 (bande passante de 20GHz) a été utilisée pour mesurer la tension aux bornes de la résistance de charge. Le P7720 présente une résistance d'entrée DC de 100k Ω , garantissant ainsi une faible charge de sonde. Afin de visualiser la forme d'onde électrique, la sonde a été connectée à un oscilloscope Tektronix DSA71254C (bande passante de 12.5GHz).

A partir de la forme d'onde électrique, le courant pic généré par le circuit pilote a pu être extrapolé. De la même manière, l'efficacité énergétique est calculée à partir de la puissance aux bornes de la résistance et du courant consommé par le circuit.

Les tests électriques ont démontré que la puce fabriquée est globalement fonctionnelle. Il n'y a pas de défaillance critique résultant de la structure d'élévation de tension capacitive, ce qui signifie que le pilote est capable de produire une tension de charge supérieure à la tension d'alimentation. De plus, les formes d'onde mesurées sont cohérentes avec le principe d'extraction de charge de la diode laser. Cependant, il existe des écarts majeurs entre les mesures et les résultats PLS, comme récapitulé dans le Tableau 4. En un mot, les données mesurées mettent en évidence une diminution significative de la capacité en courant du circuit ainsi que des performances transitoires.

L'hypothèse la plus probable de telles disparités est les parasites du circuit apportés par la plate-forme de test (boîtier, PCB et résistance de charge). En conséquence, la banc de test électrique a été considéré comme inadéquate pour mesurer les performances du circuit en fonctionnement à impulsions inférieures à la nanoseconde.

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	172.5	222.6	-22.5%
P_{draw} (mW)	67.5	111.7	-39.5%
η_{elec} (%)	53.3	55	-3%
t_{pw} (ps)	975	972	+0.3%
t_r (ps)	306	188	+62%
t_f (ps)	322	94	+242%

Table 4 – Résumé des résultats de la caractérisation électrique.

Les perspectives de test incluent évidemment l'extraction des parasites de la plate-forme de test afin de comparer et de corrélérer rigoureusement les résultats de mesure et de simulation. Finalement, des mesures de qualité nécessiteraient un PCB de caractérisation conçu de manière optimale.

Vérification optique

La caractérisation optique a été effectuée en deux étapes :

- Mesure de la forme de l'impulsion laser avec un photodétecteur rapide (bande passante $> 1GHz$) pour capturer les caractéristiques temporelles de l'impulsion laser transmise (largeur d'impulsion, temps de montée et temps de descente).
- Mesure de la puissance laser avec une sphère d'intégration afin d'estimer la capacité en courant et l'efficacité énergétique du circuit pilote.

Notez que toutes ces mesures ont été effectuées dans un boîtier de sécurité laser.

Afin de capturer la forme de l'impulsion laser, le module a été couplé à un photodétecteur Thorlabs DET08CL. Ce dernier est essentiellement une photodiode $p-n$ qui fonctionne par absorption de photons et génère un flux de courant proportionnel à la puissance optique incidente. Le DET08CL est conçu pour fonctionner en mode photoconducteur (par opposition au mode photovoltaïque), ce qui signifie que la photodiode est polarisée en inverse. Le DET08CL est basé sur un alliage d'arséniure d'indium et de gallium (InGaAs) et présente une responsivité d'environ $0.6A/W$ à $940nm$. Le photodétecteur a été connecté à un oscilloscope Tektronix DPO72304DX (bande passante

de $23GHz$) via un câble coaxial d'impédance 50Ω avec des connecteurs sub-miniature A (SMA). Enfin, l'oscilloscope a été configuré avec une résistance de terminaison de 50Ω afin de garantir l'adaptation d'impédance.

La mesure de la puissance laser a été réalisée avec une sphère d'intégration Newport 919-SL-5.3-CAL2 couplée à un détecteur à base de silicium. La sphère d'intégration est un appareil creux avec un revêtement interne diffusant la lumière. De cette manière, il permet la collecte et l'intégration spatiale de la lumière incidente. Dans la sphère, le rayonnement passe par de multiples réflexions et tend à être uniformément réparti sur la surface interne de la sphère. Après un certain temps, le détecteur recevra une irradiance uniforme, permettant ainsi de mesurer la puissance optique moyenne. En assumant que la forme d'onde des impulsions laser est une onde carrée idéale, cette mesure rend possible l'extrapolation simple du courant pic de pilotage. De la même manière, la mesure du courant consommé permet de calculer l'efficacité énergétique du circuit pilote. Cela nécessite également de faire intervenir les paramètres du VCSEL. Ici, les paramètres typiques ont été utilisés. Il est important de garder à l'esprit que l'incertitude des résultats de cette mesure réside dans le fait que le calcul est basé sur une onde carrée idéale (ce qui n'est pas le cas en pratique) et que la dépendance en température des paramètres du VCSEL n'est pas prise en compte. Ainsi, les données doivent être considérées et discutées avec du recul.

L'ensemble des résultats de mesure de la caractérisation optique est rassemblé dans le Tableau 5.

De manière générale, la puce fabriquée présente des performances satisfaisantes. Pour une tension d'alimentation typique de $2.5V$, le circuit est capable de générer des impulsions laser inférieures à la nanoseconde avec des fronts transitoires rapides, de l'ordre de $100ps$. Le pic de courant de pilotage correspondant a été calculé à $200mA$. En conséquence, la spécification typique concernant la capacité en courant est respectée. Cependant, le fonctionnement du circuit en impulsions inférieures à $500ps$ est limité. En effet, on peut observer d'importantes disparités au niveau du courant pic entre les résultats de mesure et de simulation, jusqu'à 38.8% . Ceux-ci sont probablement dus aux parasites du circuit résultant de l'interconnexion du VCSEL qui ont été calculés de manière optimiste pour la conception du circuit. Ainsi, les améliorations futures devraient être orientées vers l'optimisation de l'interconnexion physique entre la puce pilote et le VCSEL. Concernant la consommation électrique, il existe un bon accord entre la mesure et la simulation. Pourtant, les chiffres d'efficacité énergétique calculés ne correspondent pas aux valeurs simulées. De plus, la valeur ciblée de 47% n'est pas respectée lorsque la largeur d'impulsion est inférieure à $1ns$.

Il existe donc plusieurs axes d'amélioration pour le banc expérimentale optique. Avant tout, des mesures complémentaires doivent être effectuées afin de caractériser les paramètres du VCSEL en fonction de la température. Cela devrait permettre d'améliorer la précision de calcul des données de courant pic

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	197.6	222.6	-11.2%
P_{draw} (mW)	97.5	111.7	-12.7%
η_{elec} (%)	47.5	55	-13.6%
t_{opt} (ps)	824	—	—

(a) Settings: $V_{DD} = 2.5V$, $t_{mod} = 1ns$ and $f_{sw} = 100MHz$.

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	200.8	207.6	-3.2%
P_{draw} (mW)	132.5	140	-5.3%
η_{elec} (%)	33.5	48.7	-31.2%
t_{opt} (ps)	311	—	—

(b) Settings: $V_{DD} = 2.5V$, $t_{mod} = 500ps$ and $f_{sw} = 250MHz$.

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	118.3	193.3	-38.8%
P_{draw} (mW)	77.5	78.6	-1.3%
η_{elec} (%)	15.8	35.5	-55.4%
t_{opt} (ps)	191	—	—

(c) Settings: $V_{DD} = 2.5V$, $t_{mod} = 250ps$ and $f_{sw} = 250MHz$.

Table 5 – Résumé des résultats de la caractérisation optique.

et d'efficacité énergétique. Ensuite, en ce qui concerne les mesures de forme d'impulsion laser, la mise en place d'un banc de test avec un photodétecteur couplé à une fibre optique (Newport 1544-A) a été proposée. Dernier point mais non le moindre, le pilote doit être testé dans le cadre du système temps de vol, c'est-à-dire avec le détecteur basé sur des photodiodes à avalanche mono-photoniques.

Conclusion générale

L'objectif de la présente thèse était de développer un pilote de diode laser pour la télémétrie temps de vol direct dans les appareils portables grand public. Comme pour tout développement de circuit, le projet s'est déroulé de la faisabilité à la caractérisation expérimentale en passant par l'étape de conception et de dimensionnement. L'objectif de ce dernier chapitre est de passer en revue les principales réalisations de la thèse.

Avant de passer en revue les contributions de cette thèse, il est important de rappeler les principales spécifications électriques de la cible de conception. L'objectif principal était de démontrer la faisabilité d'impulsions

laser inférieures à la nanoseconde avec une haute fréquence de répétition, jusqu'à plusieurs centaines de mégahertz. De plus, les principales exigences antagonistes sont l'augmentation de la capacité en courant jusqu'à $200mA$ et l'abaissement de la tension d'alimentation à $2.5V$. Enfin, une efficacité énergétique de 47% a été ciblée.

La première étape a été de définir une classification des topologies de pilote de diode laser dédiées aux applications TOF. Les architectures existantes ont été regroupées en trois catégories:

- Le pilote de diode laser à décharge capacitive résonnant.
- Le pilote de diode laser mode courant.
- Le pilote de diode laser mode tension.

Celles-ci ont été évaluées en ce qui concerne la demande en tension d'alimentation, la vitesse transitoire et l'efficacité énergétique. Suite à une étude de faisabilité, la topologie mode tension a été mise en évidence comme le meilleur compromis possible entre la capacité en courant et l'efficacité énergétique tout en étant conforme avec un fonctionnement basse tension. Ainsi, il a été choisi de s'orienter vers une structure mode tension modifiée pour répondre aux spécifications techniques.

Le fonctionnement du circuit proposé est basé sur des cycles répétés de charge et de décharge d'un condensateur de pilotage C_{fly} , combiné à une structure d'élévation de tension. La tension de charge est ainsi augmentée, augmentant ainsi la capacité en courant du pilote. Une telle conception permet de surmonter la contrainte à $2.5V$ sur la tension d'alimentation. De plus, une fonction d'extraction de charge a été suggérée pour supprimer toute traînée optique ou pulsation secondaire dans le transitoire de désactivation de l'impulsion laser, ce qui est essentiel pour la détection TOF direct. Cette fonctionnalité est fournie par un transistor connecté entre la tension d'alimentation et le nœud de cathode du VCSEL. Simplement dit, ce transistor permet de forcer une tension inverse aux bornes de la charge pendant le temps d'arrêt du VCSEL.

Le circuit a été entièrement implémenté sur puce dans la technologie CMOS $40nm$ de STMicroelectronics. Les principaux blocs de construction qui ont été conçus sont l'étage de puissance, composé des MOSFETs de puissance et de la capacité de pilotage C_{fly} , ainsi que les circuits de génération des signaux de pilotage. La capacité de pilotage a été réalisée avec une structure MIM de $178pF$. Le dimensionnement de la largeur de canal des MOSFETs de puissance a été effectué selon une analyse de compromis entre la capacité en courant, l'efficacité énergétique, la fréquence de répétition et la surface de silicium. De plus, un condensateur de découplage sur puce de $1nF$ a été connecté entre les broches d'alimentation et de masse du circuit.

Le fonctionnement, les performances et les limites du pilote ont été évalués par des mesures électriques et optiques. Il a été montré que la topologie

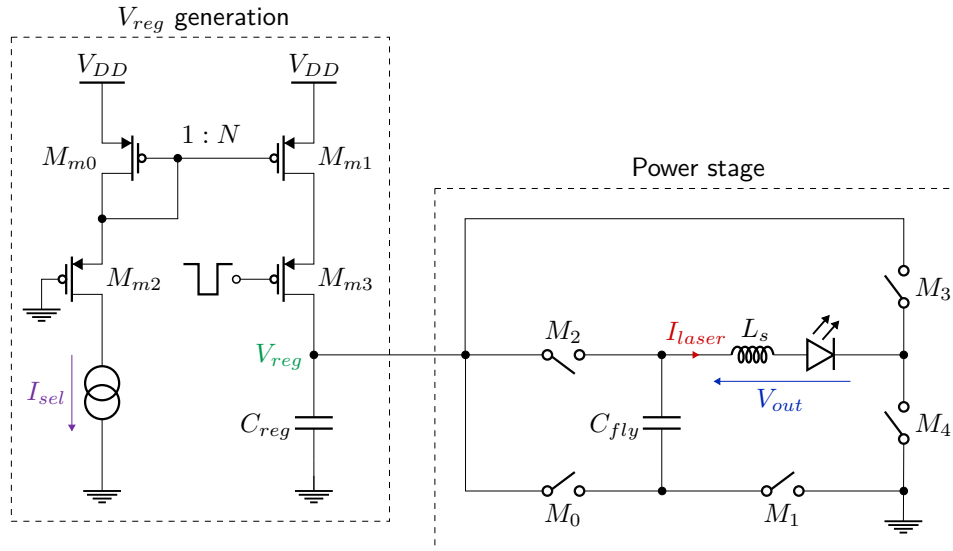


Figure 13 – Proposition de stratégie de contrôle de courant de pilotage.

proposée présente des performances supérieures par rapport aux précédents développements de pilote réalisés par STMicroelectronics. En effet, le pilote est capable de générer un courant de pilotage de $200.8mA$ tout en fonctionnant à une tension d'alimentation de $2.5V$ et à une fréquence de répétition de $250MHz$. Cela correspond à la mesure d'une impulsion laser de $311ps$ avec des temps de montée et de descente de l'ordre de $100ps$. Cependant, seule une efficacité énergétique de 33.5% a été mesurée dans ces conditions de fonctionnement. De plus, la capacité en courant du circuit est limitée en fonctionnement à impulsions inférieures à $500ps$, probablement en raison de l'inductance parasite. Cela souligne que les futures améliorations de conception devraient être orientées vers l'optimisation des interconnexions physiques entre le pilote et le VCSEL.

En bref, les réalisations de cette thèse représentent un pas en avant important en ce qui concerne l'état de l'art actuel ainsi que pour le développement des futurs produits de STMicroelectronics.

La perspective principale de ce travail est la proposition d'un schéma de contrôle et de régulation du courant de pilotage. En effet, l'emballement thermique dû à la dépendance en température de la tension directe de la diode laser est une préoccupation clé pour la conception du circuit pilote. Afin d'éviter un tel phénomène, une stratégie de contrôle du courant a été proposée pour les futurs travaux de conception. La structure est illustrée en Figure 13. À partir de la caractérisation expérimentale de la puce de test, il a été montré que le pic de courant de pilotage varie linéairement avec la tension d'alimentation. De plus, la tension d'alimentation n'a pas d'impact significatif sur la durée de l'impulsion laser. Ainsi, la stratégie de contrôle que nous avons proposée consiste à générer un nœud de tension dynamique V_{reg} pour alimenter l'étage

de puissance du pilote. Le circuit est basé sur une structure miroir de courant simple composée des PMOS M_{m0} et M_{m1} (rapport N). Ceux-ci fonctionnent en régime de saturation. De plus, le PMOS M_{m3} est synchronisé avec M_2 et M_1 . Lorsque ces derniers sont activés, un chemin de charge pour C_{reg} et C_{fly} est créé. Notez que C_{reg} agit comme une capacité de découplage pour le nœud V_{reg} . Lorsque M_0 et M_4 sont activés, C_{reg} et C_{fly} sont connectés en série et se déchargent à travers la diode laser. De cette manière, le nœud V_{reg} s'ajuste dynamiquement en fonction de la quantité de charges fournie par le miroir de courant (définie par le courant I_{sel}) et pulsée à travers la diode laser. Cette stratégie permet de définir le courant moyen $\overline{I_{laser}}$ traversant la charge,

$$\overline{I_{laser}} = \frac{1}{2} N I_{sel} (1 - \alpha) \quad (2)$$

où α est le cycle d'activité de l'étage de puissance.

La stratégie de commande de courant proposée devrait ainsi permettre d'ajuster le courant de pilotage à travers la diode laser. De la même manière, elle doit permettre de compenser dynamiquement les variations de tension directe induites par la température. Cependant, le circuit doit être correctement validé avec une future puce de test.

1 General introduction

Nowadays, environment sensing is becoming a key ingredient in a wide range of applications such as self-driving cars, consumer electronics, robotics or machine control. Broadly speaking, contactless distance measurement techniques either employ microwaves, ultrasounds or light waves [1, 8–10]. Yet, due to the shorter wavelength, only light waves provide the required angular resolution when it comes to sensing at a human scale [1, 8, 9]. As a matter of fact, only objects with a feature size larger than the wavelength can be easily resolved [11]. Light-based distance measurement can be further grouped into three main principles: triangulation, interferometry and time-of-flight.

The crucial parameters associated with distance measuring systems are the detection range (reach) and the distance resolution or precision. Figure 1.1 synthesizes the performances of each light-based range measurement technique.

In a triangulation-based setup, the position of an unknown visual point within a triangle is determined via a known triangulation basis and the related side angles pointing to the unknown point [1, 8, 12]. This principle can be implemented by means of a structured light projector (active triangulation) or with passive off-the-shelf cameras (stereoscopic vision) [8, 13]. The major drawback is that the distance accuracy is limited by the length of the triangulation basis, which eventually restricts the miniaturization of the measurement setup [12]. In addition, triangulation is commonly associated with high computational power, in particular for stereoscopic vision where the so-called correspondence problem is to be solved [10, 13].

Interferometry is based on the phenomenon of interference of light waves. There exist a wide variety of measurement setups, such as multi-wavelength interferometry, holographic interferometry, speckle interferometry or white-light interferometry [1]. Simply put, a coherent wavefront is split into a wavefront travelling towards an unknown point and a reference wavefront. The reflected wavefronts are superimposed again onto a photodetector so as to generate an interference pattern [1]. In this way, small differences in the optical paths can be detected from the analysis of the interferogram. This principle allows for a very high resolution, down to the nanometer range. Yet, the detection range is restrained by the coherence length of the light source, meaning that interferometry is mainly applicable up to a few centimeters [1, 8]. What is more,

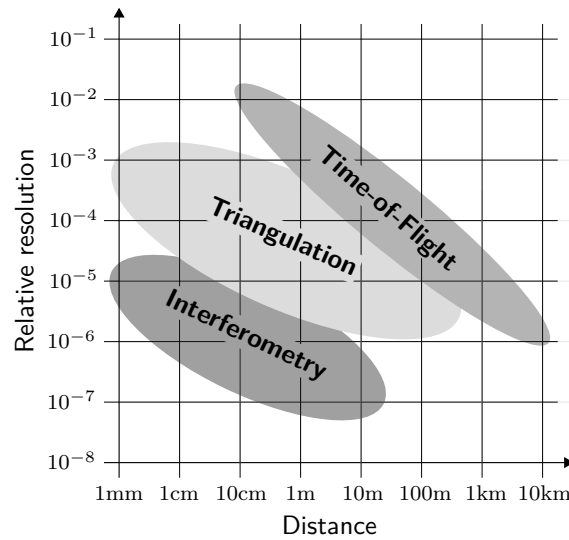


Figure 1.1 – Relative resolution of light-based range measurement techniques [1].

interferometric measurement setups require a bulky and precise mechanical instrumentation [1].

The distance to an unknown target can easily be determined by measuring the time-of-flight (TOF) of a light signal sent by a measuring setup and reflected back by the target [1]. Typically, TOF sensors are based on either direct or indirect measurement methods. With direct TOF, the distance is directly extracted from the round-trip transit time of a light pulse by means of an accurate stopwatch. With indirect TOF, the distance is indirectly extrapolated from the measurement of the phase shift between the transmitted and reflected light signal. Such a technology permits distance measurement up to several kilometers with centimetric accuracy. Moreover, it has recently become feasible in a compact measurement setup due to the miniaturization and progress of the semiconductor technology [8]. As of now, direct TOF rangefinders are more and more an essential component in mobile electronics, supporting a wide range of key functionalities such as proximity sensing (presence detection), camera focus assist in low-light or low-contrast scenes, gesture recognition and so forth [14]. Additionally, forecasts show that the TOF sensor's market is expected to grow from 2.8 billion US dollars in 2020 to 6.9 billion US dollars by 2025 [15]. This growth being mainly driven by the increasing demand of sensing capacities in automotive vehicles and consumer electronic devices.

The primary aim of this introduction is to provide a brief overview of direct TOF rangefinding as well as associated challenges. On the other hand, indirect TOF is not part of the scope of the present thesis and will not be further discussed.

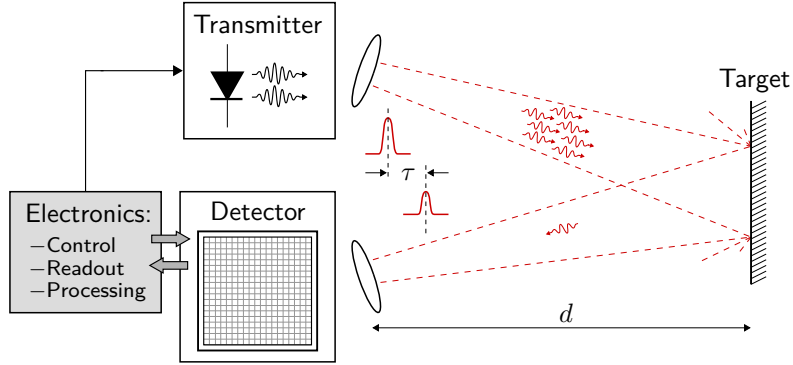


Figure 1.2 – Schematic diagram of a direct time-of-flight rangefinder.

1.1 Direct time-of-flight rangefinding

The schematic diagram of a direct TOF system is represented in Figure 1.2. It is similar to a microwave radar, except that it employs an electromagnetic radiation in the near-infrared spectral range [8, 16]. The basic operation is as follows. A light pulse is transmitted towards a visible target. Then, a portion of the reflected photons are captured by the detector (array of photodetectors) and compared to a reference time derived from the transmitted pulse. In this way, the distance to the target can be calculated from the measured pulse's round-trip transit time τ and the known velocity of light c ($\sim 3 \times 10^8 m.s^{-1}$),

$$d = \frac{c}{2}\tau \quad (1.1)$$

The measurement accuracy of such a system is limited by the timing resolution of the electronics [1, 12].

$$\delta d = \frac{c}{2}\delta\tau \quad (1.2)$$

So as to ensure a centimetric distance precision δd , a timing resolution $\delta\tau$ of $66ps$ or a bandwidth of at least $15GHz$ is required. Given that such a bandwidth seems impractical with current CMOS electronics, the ranging process usually consists in correlating a large number of repetitive pulses [11, 17, 18]. This approach allows for achieving a better precision, but eventually leads to an increase in measurement and computation time [11, 19].

1.1.1 Detector

In order to precisely detect the arrival time of reflected photons, a very fast detector and front-end electronics are required. Single-photon avalanche diodes (SPAD) fulfill the requirement for high-speed. These photodetectors have recently been feasible in standard CMOS technology and have been so

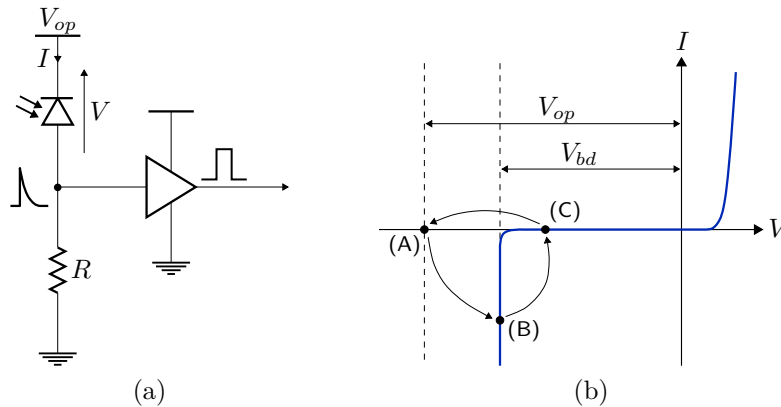


Figure 1.3 – Functioning principle of SPADs in a passive quenching circuit: (a) quenching circuit structure, (b) $I - V$ characteristics with operating cycle.

far widely employed in TOF applications [20–26].

A SPAD is basically a $p - n$ junction biased in the so-called Geiger-mode, *i.e.* beyond the breakdown voltage V_{bd} [27, 28]. Owing to the significant electric field existing in the depletion region, the drift velocity and kinetic energy of charge carriers is such that a single photon-generated electron-hole pair can trigger a self-sustaining avalanche through the process of impact ionization [17, 27]. Hence, SPADs are able to detect down to single-photon events with a timing accuracy in the order of one hundred of picoseconds, which is particularly suitable in direct TOF rangefinding [17, 29, 30]. Yet, given that the theoretical current gain is infinite, a SPAD must be coupled to a specific circuitry allowing to quench the avalanche current. The structure of a classical passive quenching circuit is depicted in Figure 1.3a. The SPAD is simply connected in series with a resistance R [17]. The operation cycle on the diode $I - V$ curve is represented in Figure 1.3b. Initially, the device is precharged to V_{op} in Geiger-mode (A). The absorption of a photon of sufficient energy (1.1eV for silicon) leads to a rapid current inrush which is converted into a digital-like voltage by a pulse shaping circuitry (B). At the same time, the voltage drop across the quenching resistor builds up, thus reducing the reverse voltage of the junction below the breakdown voltage (C). At this point, the avalanche current is quenched and the SPAD recharges towards the initial biasing point [29].

1.1.2 Transmitter

In direct TOF rangefinding as in radar, the characteristics of the transmitted light pulse are crucial [9, 11, 19, 24, 31, 32].

It is widely accepted that distance accuracy and resolution depend to a large extent on the light pulse width. This is because in the basic form of the single-photon detection, the position of the detected photon within the pulse envelope is not priori known [24]. Thus, a wide pulse would inevitably lead

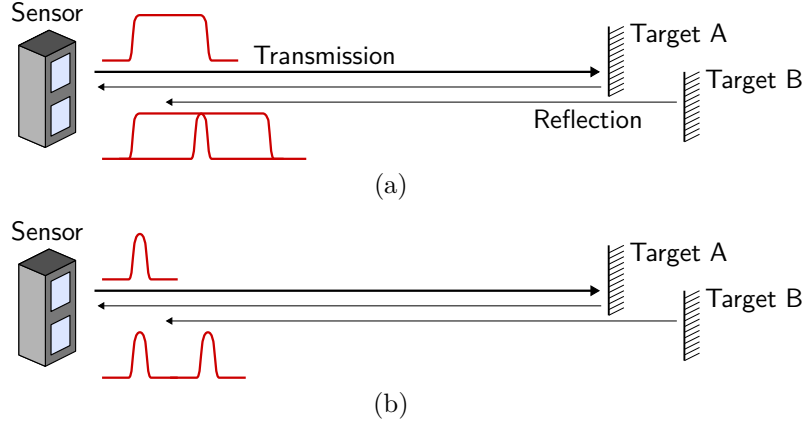


Figure 1.4 – Impact of transmitted light pulse width on distance resolution in direct TOF rangefinding: (a) wide pulse width, (b) narrow pulse width.

to an inherent measurement uncertainty. Then, let us regard the case when multiple targets lie in the sensor's field of view (see Figure 1.4). On one hand, a wide pulse results in an overlapping of the echo pulses. As a consequence, it is impossible to resolve closely spaced targets. On the other hand, a narrow pulse permits to properly discriminate multiple echoes, thus allowing to detect fine details in the sensor's field of view [11, 19]. In a nutshell, the sensor cannot resolve a distance much shorter than the space length l_{pw} of the light pulse,

$$l_{pw} = ct_{pw} \quad (1.3)$$

where t_{pw} is the pulse width and c is the speed of light. Hence, a centimetric single-shot accuracy requires a pulse width on the order of $100ps$ [11]. As the design of high-speed driving electronics is challenging, such a narrow pulse width is complex to realize in practice. Again, this calls for averaging of repetitive single measurements, which in turn results in a longer processing time [11, 19, 24]. Thus, it must be kept in mind that the shortening of the light pulse width is a key focus in direct TOF rangefinding as it enables a substantial improvement of the ranging performances, *i.e.* accuracy, resolution and processing time.

Another important aspect regarding the transmitter is the light pulse energy. When a light signal strikes a target, any detected echo is only a small portion of the incident signal. Referring to Appendix A, the number of photon detection correlated to the transmitter increases linearly with pulse energy but is likewise inversely proportional to the square of the distance. Given that the detector is also sensitive to ambient photons, the pulse energy determines the maximum detection range of the sensor. As a consequence, there is clear evidence that shortening the light pulse width calls for an increase in peak power so as to guarantee sufficient signal-to-ambient ratio for distance measurement.

All these considerations point that the optimum pulse waveform represents

a high-energy impulse with the fastest possible rising and falling edges [32]. This necessarily imposes to employ a light source with a high modulation bandwidth. Among existing light-emitting devices, directly modulated semiconductor lasers, generally referred to as laser diodes, provide attractive benefits, such as low cost, small size, high bandwidth, narrow spectral width, low divergence [11, 33]. Simply put, a semiconductor laser is a form of $p-n$ junction diode which generates coherent photons when pumped with electrical current. Laser diodes, either edge-emitting or vertical-cavity surface-emitting devices, are currently the dominant light source technology for TOF sensing [16]. The laser must be coupled to an electrical pulsed driver circuit, whose basic function is to generate a driving current pulse and provide control over pulse width and amplitude.

Typically, the emission wavelength range exploited in consumer electronics applications is the $830nm$ to $950nm$ spectral region [7]. More specifically, one can distinguish two wavelengths of interest, $850nm$ and $940nm$. The accuracy of a TOF measuring setup does not fundamentally depends on the wavelength of the transmitted light, yet the latter can impact the overall performance. The choice of wavelength is a matter of trade-off between three factors:

- **Detector responsivity:** the responsivity of silicon-based detectors tends to drop rapidly in the near-infrared spectral region [34]. As a result, the $850nm$ wavelength will provide a better signal-to-ambient ratio.
- **Physiology:** the human eye is still sensitive to infrared radiation at $850nm$. This appears as an important factor in consumer electronics as the user will still see a red glow. On the contrary, the $940nm$ wavelength is completely imperceptible to the human eye.
- **Sunlight:** the spectral irradiance received from the Sun at the Earth's surface (see Figure 1.5) can be approximated by a blackbody spectrum. The curve shows that sunlight experiences an absorption peak around $940nm$, notably due to water molecules within the Earth's atmosphere [35]. In outdoor applications, the $940nm$ wavelength will lead to a better ambient light immunity of the system.

1.2 Thesis design target

This general introduction emphasizes the importance of the laser driving electronics in direct TOF rangefinding. The driver should enable the generation of the shortest possible light pulse for optimum ranging performances. So as to advance towards this challenging requirement, the present thesis intends to investigate on laser diode driver circuits for sub- ns pulse operation in consumer mobile electronics.

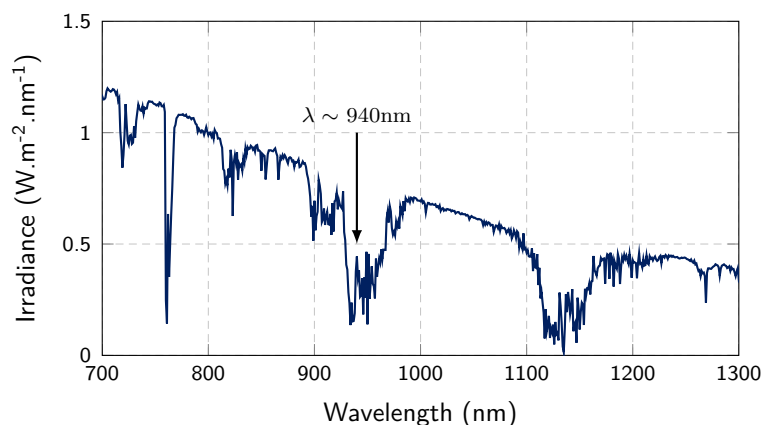


Figure 1.5 – Solar spectral irradiance at the Earth’s surface [2].



Figure 1.6 – Pictures of the VL53L0X developed by STMicroelectronics.

This project is carried out as part of the research and development pole of STMicroelectronics. The Franco-Italian semiconductor manufacturer was the first company to market a miniature silicon-based TOF rangefinder jointly incorporating a SPAD detector array as well as a semiconductor laser. An example of such a device is the VL53L0X module ($4.4\text{mm} \times 2.4\text{mm} \times 1.0\text{mm}$) which exhibits a ranging capability up to 2m for single-point sensing (see Figure 1.6).

The goal of the project is to design a fully integrated vertical-cavity surface-emitting laser (VCSEL) driver for enhancing the performances of current TOF products developed by STMicroelectronics.

The main electrical specifications of the design target are listed in Table 1.1. The focus of the thesis is to demonstrate sub- ns driving current pulses with an amplitude of 200mA as well as promote low-voltage operation, *i.e.* down to 2.5V . In comparison with latter driver development by STMicroelectronics, the aim is to increase the driver’s current capability, that is transmitted power, while decreasing the supply voltage of the circuit. Last but not least, there is a need for TOF technology providers to optimize the power efficiency of sensors,

which is an ever-present concern in consumer embedded electronics. Here, an efficiency of at least 47% is targeted.

The circuit is to be designed in a $40nm$ CMOS technology as it is the current technology node for the fabrication of the SPAD photodetector in STMicroelectronics.

Specification	Min.	Typ.	Max.	Unit
Supply voltage	—	2.5	—	V
Driving current peak	—	200	—	mA
Driving current pulse width	250	500	—	ps
Pulse repetition frequency	—	200	—	MHz
Power efficiency	47	—	—	%

Table 1.1 – Electrical specifications of the laser diode driver.

1.3 Manuscript content

The organization of the manuscript is as follows.

[Chapter 2](#) reviews the state-of-the-art of laser diode driver circuits dedicated to time-of-flight applications. The goal is to group existing topologies and discuss pros and cons.

[Chapter 3](#) covers several pre-design considerations. These include an overview of the $40nm$ CMOS technology as well a presentation of the laser diode technology and hardware environment. Afterwards, a feasibility study is carried out on the basis of these considerations, with the final aim being to propose a laser diode driver topology for meeting the design target.

[Chapter 4](#) is dedicated to integrated driver circuit design with a focus on transistor-level sizing and physical implementation. The circuit has been fabricated using the $40nm$ technology node by STMicroelectronics.

[Chapter 5](#) presents the experimental setup and measurement results of the fabricated test chip. Performance-limiting factors are highlighted and future improvements regarding design and experimental setup are proposed.

[Chapter 6](#) summarizes the key contributions of the thesis together with perspectives. The main achievement is the development of an innovative laser diode driver architecture compliant with low-voltage functioning, down to $2.5V$, and capable of generating sub- ns current pulses up to $200mA$. In short, this work represents an important step forward towards future product development by STMicroelectronics.

2 State-of-the-art

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The aim of this chapter is to identify and present the existing topologies of laser diode driver, focusing exclusively on published researches dedicated to time-of-flight (TOF) applications. Each topology is successively detailed in terms of circuit functioning and implementation. The relevant performance metrics are discussed based on either experimental measurement data or post-layout simulation results. Additionally, the pros and cons of each solution are pointed out in regards to the framework of the thesis, that is consumer mobile devices. In the end, a performance review of the literature in the form of landscapes is outlined.

2.1 Framework of the review

Pulsed laser diode drivers have been widely developped in the field of optical data communication [36–41]. Generally speaking, topologies in use rely on a differential current-steering circuit structure, with D and $\bar{D}$ being complementary data signals (see Figure 2.1). That way, the current I_m flows either in the right or in the left transistor, thus modulating the laser diode between I_b and $I_b + I_m$. A constant current source which must remain active at all times is therefore required to supply the modulation current I_m . Such a differential circuitry is adequate for enabling the transmission of digital signals with a modulation current of a few milliamps. However, using a similar approach when a higher driving current is required would result in an excessive current consumption and power dissipation through the tail current source I_m . These architectures are therefore not discussed in the literature review.

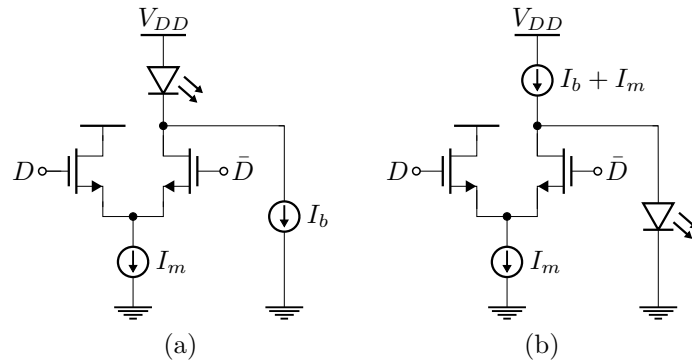


Figure 2.1 – Current-mode laser diode drivers for optical datacom: (a) common-anode, (b) common-cathode.

The study of the literature dedicated to TOF applications has highlighted several metrics of interest to assess the performances of laser diode driver circuits. Referring to Table 2.1, these are the input voltage, the laser diode driving current pulse peak and duration, the laser diode optical power and pulse width and the pulse repetition frequency. Moreover, the transient performance, *i.e.* current pulse's rise and fall times, as well as the circuit area are also stated when available.

Most of the published research falls within the scope of long-range sensing applications, such as automotive light detection and ranging (LiDAR). In this field, the power consumption does not appear as an important figure and is often eluded. Thus, electrical efficiency which is a key performance criteria in consumer embedded electronics could not be rigorously discussed. Still, the aim was to evaluate, to the extent possible, the efficiency for each circuit topology. The latter can be simply computed from,

$$\eta_{elec} = \frac{P_{laser}}{P_{draw}} = \frac{P_{laser}}{P_{laser} + P_{loss}} \quad (2.1)$$

where P_{laser} is the useful electrical power through the laser diode and P_{loss} is the driver circuit's power losses, either switching losses (*e.g.*, a transistor switching on and off) or conduction losses (*e.g.*, a transistor conducting current).

2.2 Laser diode driver topologies

This section presents the existing laser diode driver topologies in terms of operation, implementation and performances. The architectures have been divided into three main categories depending on the driving pulse's features:

- The resonant capacitive discharge laser diode driver.
- The current-mode laser diode driver.

Name	Symbol	Unit
Input voltage	V_{in}/V_{DD}	V
Peak current	I_{peak}	A
Current pulse width	t_{pw}	ns
Current pulse rise time	t_r	ns
Current pulse fall time	t_f	ns
Optical output power	P_{opt}	W
Optical pulse width	t_{opt}	ns
Pulse repetition frequency	f_{sw}	MHz
Power consumption	P_{draw}	mW
Power efficiency	η_{elec}	%

Table 2.1 – Metrics of interest for the state-of-the-art review.

- The voltage-mode laser diode driver.

Throughout this section, the notion of parasitic or stray inductance is regularly raised. Inductance is an unavoidable ingredient of any electronic devices, arising from packaging, interconnects (*e.g.*, metal traces or bond wires) and so forth [42]. The voltage drop V_L across an inductance L_s is directly proportional to the time rate of change of the current I_L flowing through it,

$$V_L = L_s \frac{dI_L}{dt} \quad (2.2)$$

Since this voltage drop opposes a change in current, parasitic inductance represents a critical point in high-speed driving electronics.

2.2.1 The resonant capacitive discharge driver

The resonant topology based on capacitive discharge is widely reported in literature [11, 23, 25, 43–48]. In the simplest terms, the circuit's behavior consists in repeated charging and discharging phases of an energy storage capacitor. More specifically, the capacitor is first charged to a predefined input voltage while the laser diode is off. A switch is then turned on so that the capacitor can fully discharge through the laser diode, thus generating a light pulse. Eventually, the switch is turned back off, which lets the capacitor recharge for the next pulse. Given that stray inductance always exist in the capacitive discharge path, the driving current pulse shape is set by a series RLC response. Hence, the main strategy when designing such a resonant structure consists in setting the circuit's RLC parts in order to get the desired pulse features.

2.2.1.1 Driver circuit topology

There exist two distinct capacitive discharge resonant circuit structures. Both of which are represented in Figure 2.2 together with the corresponding timing sequence. Note that L_s depicts the parasitic inductance.

In the first setup shown in Figure 2.2a, the capacitor C is charged to V_{in} through R_b and D . When transistor M_{sw} is turned on, the node V_X is pushed to $-V_{in}$ due to the voltage continuity across the capacitor. As a result, the laser diode is forward biased, thus discharging the capacitor [23, 25, 43–45].

A damping resistor R_d is often added in the current path to optimally set the damping factor of the RLC response. This way, significant current oscillations which could lead to secondary light pulsations or laser diode damage can be avoided [23, 25, 44, 45].

An alternative resonant driving structure is shown in Figure 2.2b [11, 47, 48]. Here, the capacitor C is charged through resistor R_{in} and its top plate is connected to the anode pin of the laser diode. In the same way as described above, the discharge is triggered by the turn-on of transistor M_{sw} .

Regardless of component layout, the current pulse shape is controlled by the resonant network composed of C and L_s , as well as by the total ohmic resistance R_s in the current loop through the laser diode. The latter accounts primarily for the on-state resistance of the switch M_{sw} . Also, it should be noted that any damping resistor will add up to R_s .

In the underdamped RLC response, the pulse shape can be described by a half-cycle of a sine wave of period $t_{res} = 2\pi\sqrt{L_s C}$ [11, 47]. Under the assumption that the laser diode has a fixed forward voltage drop V_{laser} , the current pulse peak and width can be approximated from,

$$I_{peak} \approx \frac{V_{in} - V_{laser}}{R_s + \sqrt{\frac{L_s}{C}}} \quad (2.3)$$

$$t_{pw} \approx \frac{t_{res}}{3} = \frac{2}{3}\pi\sqrt{L_s C} \quad (2.4)$$

One can see that there exists a trade-off between peak current and pulse width when setting the value of C . In addition, parasitic inductance have a significant impact on the design, limiting both the driving current capability and the shortening of the pulse duration. From expressions (2.3) and (2.4), it is possible to solve for V_{in} ,

$$V_{in} = \left(\frac{2\pi L_s}{3t_{pw}} + R_s \right) I_{peak} + V_{laser} \quad (2.5)$$

There is clear evidence that for a fixed current pulse shape, the necessary input voltage increases linearly with the value of L_s [47, 48]. For these reasons, minimizing stray inductance is a key focus to improve circuit performances and allow at the same time for a lowering of the input voltage [11, 25, 43, 44, 47, 48].

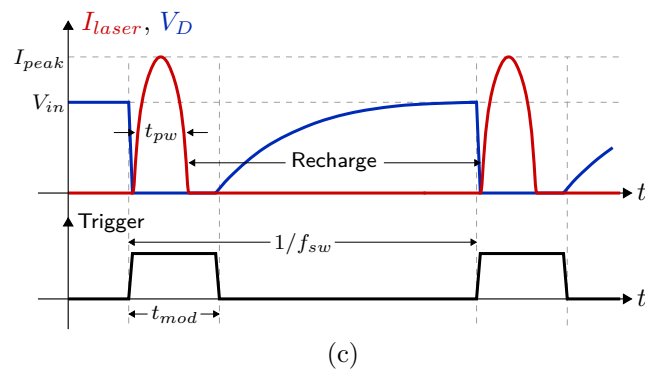
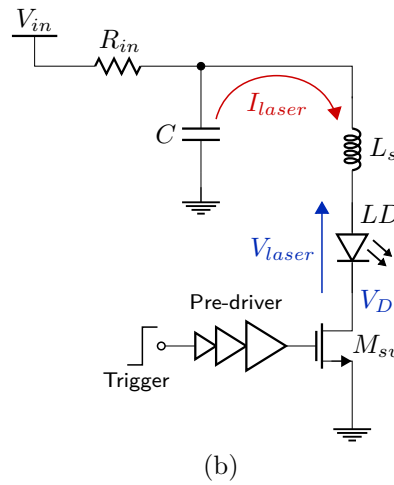
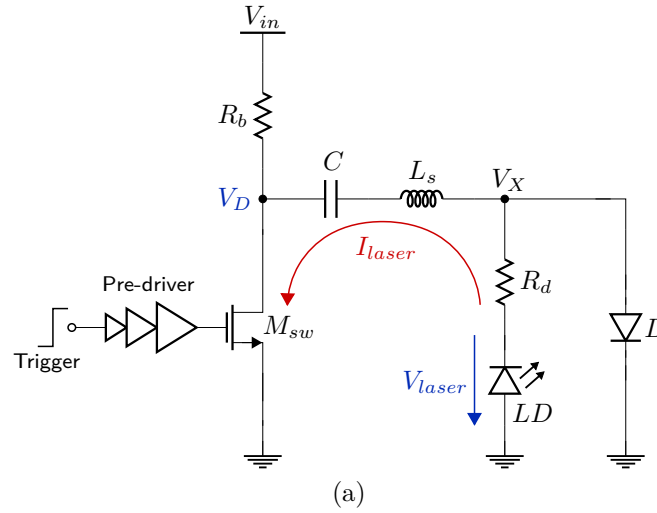


Figure 2.2 – Capacitive discharge resonant laser diode driver topology: (a) (b) circuit architectures, (c) timing sequence.

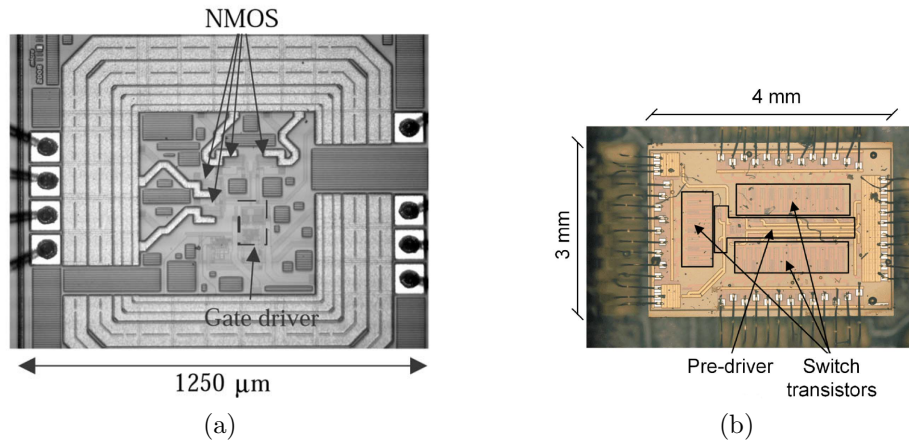


Figure 2.3 – Joint integration of MOSFET and gate driver: (a) 0.35μm CMOS and (b) 0.35μm high voltage CMOS.

2.2.1.2 Driver switch features

Given that the storage capacitor must be relatively small in order to get a narrow laser pulse, the capacitive discharge resonant circuit usually calls for a large input voltage. Typical values for long-range sensing applications range up to several tens of volts in order to achieve ampere-scale current pulses with the required slope $\frac{di}{dt}$ [47]. Consequently, choosing the proper device for implementing the switch M_{sw} appears as a crucial design step. As a matter of fact, it must withstand both high voltage and current as well as enable fast switching [47].

Former implementations have mostly relied on silicon (Si) power MOSFETs. In [45], the resonant circuit is built using a Fairchild FDMC86244 MOSFET with an Intersil EL7158 gate driver. The major drawback to discrete MOSFETs is that they exhibit a large gate capacitance which tends to increase their switching time [11, 47, 49]. Furthermore, it is accepted that the packaging technology is a major preoccupation regarding parasitics [50]. Due to their vertical structure, large MOSFETs necessitate external packaging which adds significant stray inductance in the current path of both the laser diode and the pre-driver [47, 49].

A possible alternative shown in Figure 2.3 consists in placing the pre-driver and the MOSFET on-chip [25, 43, 44]. In this way, the gate capacitance is substantially reduced as compared to discrete devices [43].

More recently, field-effect transistors (FET) based on gallium nitride (GaN) have been employed to overcome the known limitations of Si MOSFETs [11, 47, 48]. GaN devices show far less gate capacitance and resistance as compared to their silicon-based counterparts of comparable voltage and current ratings. In addition to their faster turn-on, GaN FETs are lateral devices which enable

the use of chip-scale packaging [11, 47, 48]. Together with the small die size, this contributes to considerably reduce the parasitic inductance, thus improving circuit performances.

Apart from the use of Si MOSFETs or GaN FETs, it is worth noting that bipolar junction transistors (BJT) have also been used within the capacitive discharge resonant driver [46]. Since the BJT is operated in the avalanche breakdown regime a very high voltage is required to trigger the device. Also, the pulse repetition frequency is limited due to thermal constraints.

2.2.1.3 Summary

A partial performance overview of the capacitive discharge resonant driver based on recently published researches is presented in Table 2.2. On the face of it, reported implementations are quite disparate with a driving current peak ranging from 1A to 64A. Still, it is clear that a relatively small storage capacitance is usually employed, between a few tens and a few hundreds of picofarads, in order to get a current pulse width in the order of the nanosecond. As already explained, due to the intrinsic trade-off between pulse duration and peak current, a small capacitance eventually translates into a requirement for a high supply voltage for reaching an ampere-scale driving current. What is more, the capacitor have only been realized so far by means of discrete devices. Yet, knowing that capacitor structures are available in any CMOS process, such a topology could be implemented as a fully integrated solution.

It is worth noting that sub- ns laser pulses have been demonstrated so far by using a custom laser diode based on the enhanced gain-switching operation [25, 45]. This specific laser can achieve single isolated pulse ($t_{opt} \approx 100ps$) when pumped with a current pulse having a duration of approximately $1ns$ [51].

In conclusion, some fundamental characteristics of the resonant topology are pointed out below:

- The parasitic inductance in the current path plays a part in the circuit functioning, *i.e.* current pulse shaping [11, 47]. Nevertheless, it must be kept as small as possible in order to achieve maximum performance.
- As the pulse shape is preset by the RLC network, the trigger pulse width of switch M_{sw} can be significantly longer than the required laser pulse duration. This point is convenient for pre-driver design since only the rising edge must be carefully looked at.
- The laser pulse energy is well controlled via the input voltage, thus eliminating thermal runaway [11]. Still, the pulse shape is fixed for a given design, which prevents the feasibility of diverse pulse sequence.
- The maximum pulse repetition frequency is limited by the recharge time of the capacitor, meaning that an incomplete charge would eventually

lead to a drop in driving current. Indeed, reported repetition rates do not exceed the megahertz range.

- The average power consumption from the input voltage follows a $CV_{in}^2 f_{sw}$ dependence [25, 44]. However, power efficiency cannot be discussed due to the lack of data in the published literature.

Reference	[43]	[44]	[23]	[45]	[25]	[46]	[47]	[48]
Year	2009	2013	2013	2014	2016	2018	2018	2019
Implementation	$0.35\mu m$ CMOS	$0.35\mu m$ 50V CMOS	Discrete Si MOSFET	Discrete Si MOSFET	$0.35\mu m$ HV-CMOS	Discrete Si BJT	Discrete GaN FET	Discrete GaN FET
Laser diode	L904P030	PGAS1S03H	—	Custom	Custom	—	TPGAD1S09H	TPGAD1S09H
V_{in} (V)	5	50	140	120	50	140	75	75
C (nF)	0.22 – 0.68	0.120	0.320	0.047	0.033	—	1.1 (EPC2016C) 2.8 (EPC2001C)	1.1
f_{sw} (MHz)	0.01	1	0.3 – 0.6	> 0.1	1	0.01	10 [11]	10 [11]
I_{peak} (A)	~ 1	~ 4	~ 25	~ 6.5	~ 2	—	35 (EPC2016C) 64 (EPC2001C)	49
t_{pw} (ns)	~ 3	~ 2	~ 4	~ 1.1	~ 1	—	3.4 (EPC2016C) 5.6 (EPC2001C)	2.8
P_{opt} (W)	0.277 – 0.43	2.3	40	~ 10	2.7	50	—	—
t_{opt} (ns)	2.4 – 4.7	1.5	4	~ 0.125	~ 0.1	1.87	—	—
P_{draw} (mW)	—	~ 300 (1MHz)	—	—	175 (500kHz)	—	—	—

Table 2.2 – Partial state-of-the-art of the resonant laser diode driver performances.

2.2.2 The current-mode driver

The basic principle of current-mode driver topologies consists in driving the laser diode through a current source [3–5, 52–54]. These can be distinguished according to whether the current source is laid out in a shunt [52, 53] or a series design [3–5, 54]. The shunt architecture (see Figure 2.4) employs a constant current source which provides the necessary driving current to the laser diode. The current flow is either routed towards or away from the load depending on the state of a shunt switch. On the other hand, the series architecture (see Figure 2.5) consists in connecting the laser diode in series with a voltage source V_{in} and a pulsed current source. Note that C_{in} is the decoupling capacitor associated with V_{in} . Simply put, the current circulates through the load when the current source is enabled. In both configurations, the laser pulse duration is set by the trigger signal.

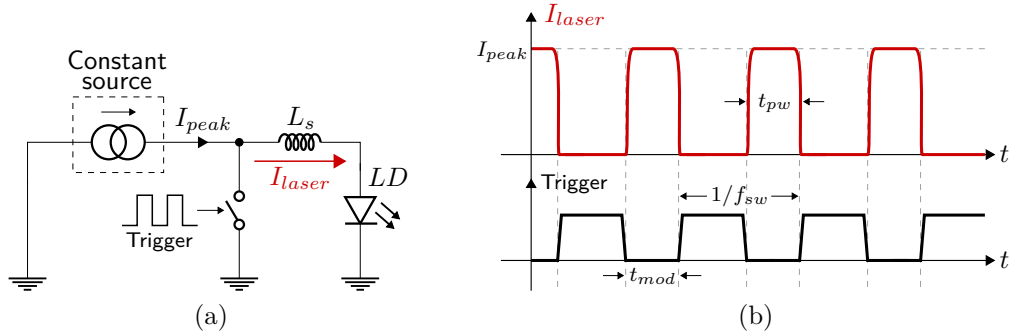


Figure 2.4 – Shunt current-mode topology: (a) circuit structure, (b) timing sequence.

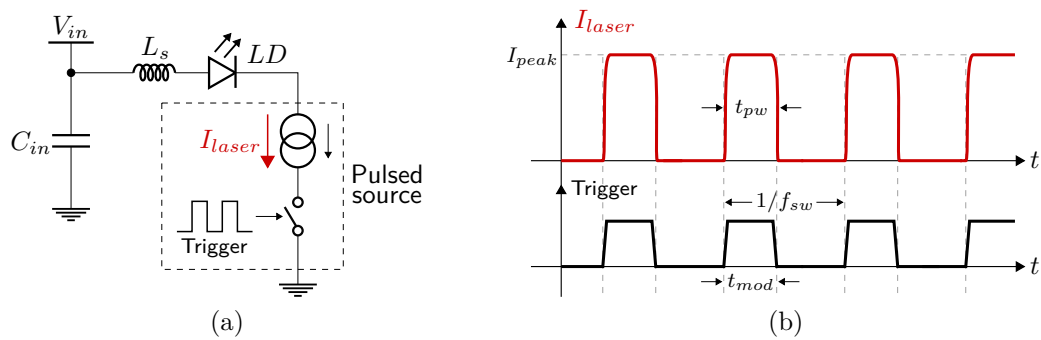


Figure 2.5 – Series current-mode topology: (a) circuit structure, (b) timing sequence.

This section covers all the reported implementations of the current-mode laser diode driver as part of time-of-flight applications.

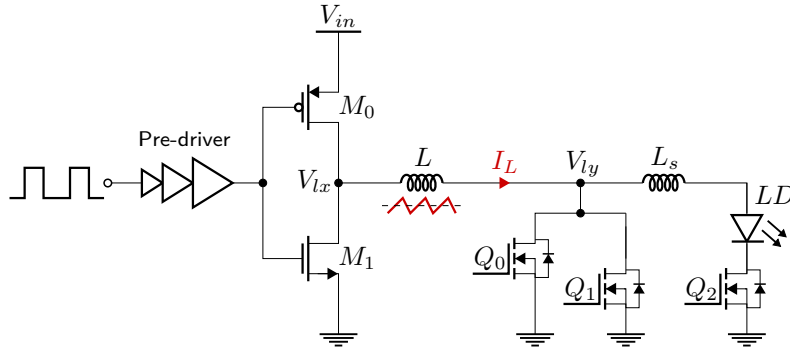


Figure 2.6 – Inductor-based shunt current-mode laser diode driver.

2.2.2.1 Inductor-based shunt structure

The current-mode driver described in [52] is based on a regulated constant current source and a network of both series and shunt power switches. As illustrated in Figure 2.6, the current source is realized by an inductor $L = 1\mu H$ as well as a half-bridge synchronous rectifier comprising a PMOS high-side switch M_0 and a NMOS low-side switch M_1 . On the other hand, the switches $Q_0 - Q_2$ act as a current steering circuit. Note that the switching period of the rectifier must be sufficiently lower than the width of the load current pulse so that the switches are not affected by the ripple current through the inductor.

The switches operate as follows. In the idle state, the switch Q_0 is on to maintain the continuity of the current through the inductor. The current flow is steered towards the laser diode when Q_2 and Q_0 are respectively on and off. Finally, the laser diode is switched off by simultaneously turning Q_2 off and Q_1 on.

The low-side switch Q_2 is specifically added to reduce the switch-off time of the laser diode. Once Q_2 is turned off, the loop parasitic inductance L_s induce a voltage overshooting at the drain or cathode node. As a result, a large negative voltage is applied across the load, thus leading to a rapid interruption of the current flow. The con of this approach is that the impact of Q_2 relies only on parasitic inductance. Obviously, its purpose becomes less visible with reduced parasitics. Moreover, the use of an additional switch can be detrimental for electrical efficiency due to switching losses, in particular when aiming for a high pulse repetition frequency.

In terms of implementation, switching devices have been fabricated within an integrated circuit. On one hand, the half-bridge rectifier has been realized by standard 5V CMOS devices. On the other hand, the switches $Q_0 - Q_2$ have been implemented by custom high-voltage 5V-gated laterally-diffused power MOSFETs (LDMOS). These provide voltage clamping through their inherent avalanche breakdown effect, thus guaranteeing the circuit's reliability against voltage spikes induced by parasitic inductance. Last, the $1\mu H$ inductor is

placed off-chip.

The post-layout simulation and experimental measurement results of the driver circuit are presented in Table 2.3 [52, 53]. The laser diode utilized for characterization is an Excelitas PGAS1S03H.

Parameter	Post-layout	Experimental
V_{in} (V)	5	5
f_{sw} (MHz)	20	20
I_{peak} (A)	5	5
t_{pw} (ns)	3.5	5
t_r (ns)	0.9	0.9
t_f (ns)	0.9	2.5
Area (mm ²)	2.56	2.56

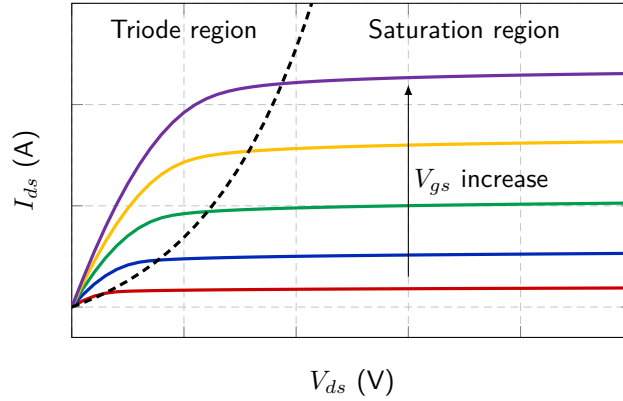
Table 2.3 – Post-layout simulation and experimental results of the inductor-based shunt current-mode driver.

There are several benefits to using such a magnetic-based shunt current-mode topology. The inductor provides a high-impedance characteristics to the current source. The driving current peak is well controlled through the half-bridge rectifier provided that the circuit incorporates an accurate current sensing scheme and feedback loop. In addition, given that the voltage swing at node V_{ly} is independent of V_{in} , the circuit can be operated from a relatively low supply voltage. Yet, as V_{ly} can potentially rise to a high value, it could be necessary to add area and power consuming protection devices, such as power cascode transistors or low-impedance fast clamping circuits. This would be especially true in advanced CMOS technology nodes for which the breakdown voltage of transistors is limited to a few volts.

Another downside is that the inductor must be sufficiently large in order to build up a constant current source. As demonstrated in expression (2.6), the current ripple ΔI_L through the inductor is inversely proportional to the inductance L and the switching frequency f_r of the half-bridge rectifier [55].

$$\Delta I_L = \frac{V_{ly}(V_{in} - V_{ly})}{Lf_r V_{in}} \quad (2.6)$$

As part of an integrated solution, this calls for an external component that must be mounted close to the driver chip, thus increasing system size and complexity. Also, knowing that any inductor structure exhibits an equivalent series resistance, the constant current source may induce large ohmic losses which is detrimental for the circuit's power efficiency.

Figure 2.7 – Output characteristics of a n -channel MOSFET.

2.2.2.2 Series structure

Broadly speaking, the series current-mode driver exploits the saturation regime of the MOS transistor, *i.e.* $V_{ds} > V_{gs} - V_{th}$, with V_{th} being the threshold voltage. Referring to the output characteristic $I_{ds} = f(V_{ds})$ shown in Figure 2.7, a transistor in saturation operates as a voltage-controlled constant current source.

2.2.2.2.1 Current source switch: The current-mode laser diode driver presented in [54] is based on capacitive discharge and employs the exact same circuit structure as the resonant topology depicted in Figure 2.2. The particularity is that transistor M_{sw} works as a current source switch. In opposition to the resonant driving scheme, the storage capacitor is also significantly larger ($\sim 18nF$) so that the steady-state current is kept constant throughout the whole pulse duration.

During the driving current transient, the voltage is essentially applied across the stray inductance, which determines the pulse's rise time. Thus, the input voltage is set depending on the amount of parasitics in the current path. Here, an input voltage of 70V is needed to generate a peak current of approximately 10A with rise and fall times of $\sim 2ns$. It should be noted that this voltage level is generated from a switched-capacitor DC-DC converter described in [56]. Furthermore, the laser pulse width can be configured from 10ns to 50ns owing to the large discharged capacitor.

The laser diode's forward voltage is only 2.5V at an operating current of 10A. As the stray inductance acts as a short circuit at steady-state, the drain-source voltage of M_{sw} captures a large portion of the available voltage. Eventually, this leads to large conduction losses across M_{sw} , therefore resulting in a poor electrical efficiency. Given that the overall power consumption of the driver at a duty cycle $\alpha = 0.1\%$ is 591mW, the corresponding electrical efficiency can be estimated from,

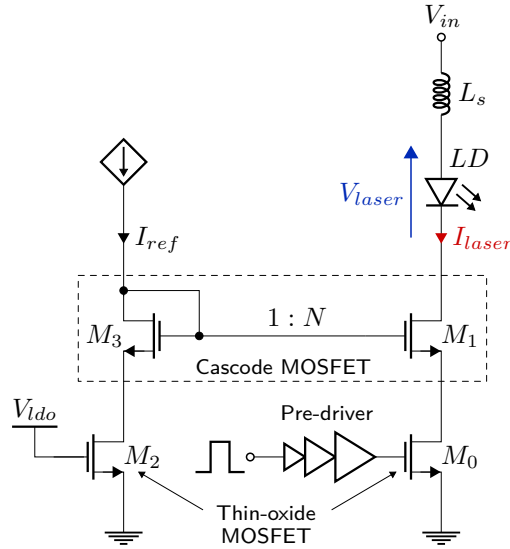


Figure 2.8 – Series cascode current-mode laser diode driver with current mirror structure [3].

$$\eta_{elec} \approx \frac{\alpha V_{laser} I_{peak}}{591mW} = \frac{0.001 \times 2.5V \times 10A}{591mW} = 4.2\% \quad (2.7)$$

Obviously, reducing parasitic inductance would permit to significantly lower the input voltage while maintaining similar transient performance.

2.2.2.2.2 Cascode current source In the simplest possible form, the output stage of a series cascode current-mode driver consists in a low-side switch together with a cascode NMOS transistor functioning in the saturation region [3–5].

In [3], a series cascode current-mode driver fabricated in a $0.18\mu m$ CMOS technology has been implemented. The key feature of the circuit is that it incorporates a combination of a coarse and a fine delay generator. In this way, the laser pulse duration can be configured from below $100ps$ to $5ns$ with a $1ps$ resolution.

As shown in Figure 2.8, the driver’s output stage comprises switch M_0 and cascode M_1 . The gate voltage of M_1 , and so the driving current peak, is controlled via a current mirror structure. It is worth noting that M_0 and M_2 have been realized by low-voltage thin-oxide NMOS. In this manner, M_1 also acts as a protection device for the low-side NMOS. The benefit of employing a low-voltage NMOS switch is the potential for faster gate signal transient. The voltage level, V_{ldo} associated with thin-oxide transistors is generated on-chip by a low-dropout linear regulator.

So that M_1 operates in the saturation region, a minimum drain-source voltage of $2V$ is required. On the other hand, the laser diodes utilized for

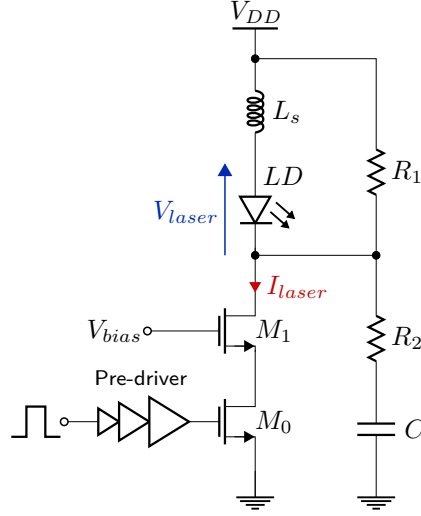


Figure 2.9 – Series cascode current-mode laser diode driver with pull-up resistor [4].

testing have a forward voltage in the range of $2V$ to $2.5V$. Since the input voltage V_{in} should not exceed $5.5V$ for guaranteeing safe operation of M_1 , a key concern is that the parasitic voltage drop through the laser diode current path must be minimized. This calls for an optimized wiring of the laser diode.

The fabricated chip has demonstrated a driving current peak of $500mA$ (measured through a resistive load) at a repetition frequency up to $200MHz$. The current pulse width can be programmed down to $464ps$ to isolate the gain-switching pulse of the laser diode. In this way, a $74ps$ laser pulse can be produced.

The power consumption of the driver is $105mW$ at $200MHz$. This figure does not take into account the current sunk from the input supply rail V_{in} . Still, it is possible to roughly estimate the electrical efficiency of the structure based on a duty cycle $\alpha = 10\%$ and an input voltage of $5V$,

$$\eta_{elec} \approx \frac{\alpha V_{laser} I_{peak}}{(\alpha V_{in} I_{peak}) + 105mW} = \frac{0.1 \times 2.5V \times 500mA}{(0.1 \times 5V \times 500mA) + 105mW} = 35.2\% \quad (2.8)$$

In [4], the driver's output stage is formed by a similar cascode structure (see Figure 2.9). The driving current peak being controlled through the gate voltage V_{bias} of cascode M_1 . In addition, a pull-up resistor R_1 is also incorporated between the positive supply rail and the cathode node. As a consequence, when M_0 is turned off, the capacitance of the laser diode are discharged in a time which depends on the pull-up strength. The switch-on of the laser diode is therefore delayed due to the charging time of the capacitance. During this time, the stray inductance L_s is expected to be charged, thus leading to a faster rising edge of the driving current pulse.

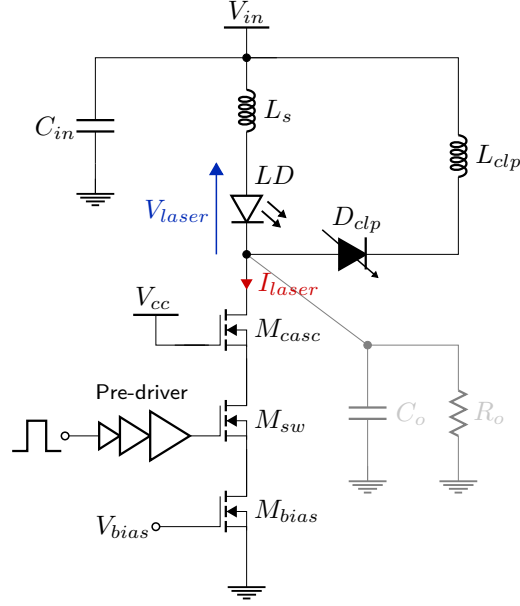


Figure 2.10 – Resonant series current-mode laser diode driver [5].

The driver has been fabricated in a $0.18\mu m$ CMOS technology and powered from a fixed $3.3V$ source. A laser pulse with a duration of $5ns$ and a peak power of $1.84W$ has been demonstrated. The corresponding driving current peak is approximately $2.2A$. These measurement results have been obtained at a $100MHz$ switching frequency, *i.e.* 50% duty cycle.

So far, there is no sizing approach proposed for the pull-up resistor. However, it should be sufficiently large in order to limit the short circuit current when M_0 is on. Also, the role of R_2 and C is not specified. Moreover, it is not clearly stated whether the passive components are implemented on-chip or by discrete devices. Still, the main issue with such a structure is that adding more capacitance, namely C , on the cathode node will tend to slow down the transient speed of the driving current pulse.

Last, given that the laser diode's forward voltage is approximately $2.5V$ at a bias current of $2.2A$, the power efficiency can be estimated from,

$$\eta_{elec} \approx \frac{V_{laser} I_{peak}}{V_{DD} I_{peak}} = \frac{2.5V \times 2.2A}{3.3V \times 2.2A} = 75.6\% \quad (2.9)$$

It is worth keeping in mind that this figure does not take into account the current drawn through the switching of transistor M_0 . The latter must be dimensioned with a large channel width in order to minimize ohmic losses. Hence, the effective efficiency of the driver is expected to be drastically lower.

The laser diode driver described in [5] also employs a cascode output stage. As depicted in Figure 2.10, it comprises transistors M_{casc} , M_{sw} and M_{bias} . The circuit can be seen as a parallel RLC network formed by the resistance R_o and capacitance C_o of the output stage as well as by the stray inductance L_s .

The key feature is that a supplementary cascode transistor is incorporated, namely M_{casc} . In this way, R_o is significantly increased and the RLC response is strained in strong underdamped regime. As a result, a large peak current with fast rising edge can be achieved due to the overshooting caused by the RLC resonance. The current pulse duration is set by the width of the gate signal of M_{sw} . Ideally, the switch is turned off immediately after the primary current spike, hence the denomination as a resonant series current-mode driver. Then, the clamp diode D_{clp} creates a secondary path for the ringing arising from the energy stored in the parasitic inductance. Hence, the clamping device protects the laser diode against potential damage due to overvoltage.

The major pro of this topology is that, due to the large resistance R_o , the value of the stray inductance does not significantly impact the damping ratio $\xi = \frac{1}{2R_o} \sqrt{\frac{L_s}{C_o}}$ of the RLC network. The current pulse peak and width can be approximated from,

$$I_{peak} \approx 2I_{bias} \quad (2.10)$$

$$t_{pw} \approx \pi \sqrt{L_s C_o} \quad (2.11)$$

where I_{bias} is the direct current level set via gate voltage V_{bias} . In the same way as for a capacitive discharge resonant driver, the pulse width can be further reduced by minimizing parasitics.

The driver has been realized in a 160nm BCD technology. A driving current pulse up to 18.55A with a duration of approximately 850ps has been demonstrated. Yet, an input voltage V_{in} of 54V is required to ensure sufficient headroom so that the cascode current source works properly. As the forward voltage of the laser diode is 10V, the efficiency can be calculated from,

$$\eta_{elec} \approx \frac{V_{laser} I_{peak}}{V_{in} I_{peak}} \frac{10V \times 18.55A}{54V \times 18.55A} = 18.5\% \quad (2.12)$$

Again, this number does not include the dynamic losses due to the switching of transistor M_{sw} .

2.2.2.2.3 Wrap-up: Table 2.4 presents a performance overview of current-mode series laser diode driver topologies. All reported implementations are based on an integrated solution (either partial or full).

The primary benefit of such a topology is that the driving current peak is well controlled by means of a transistor in saturation. Therefore, the laser pulse shape is fully configurable in terms of peak power and duration. Last but not least, there is no structural factor limiting the pulse repetition frequency, as it is the case in a capacitive discharge resonant driver.

However, ensuring sufficient voltage headroom for proper functioning of the current sourcing stage is a critical concern. As a result, a minimum input voltage, which can be approximated by summing the targeted laser diode's

Reference	[54]	[3]	[4]	[5]
Year	2009	2018	2018	2018
Process	0.35 μm 80V CMOS	0.18 μm CMOS	0.18 μm CMOS	160nm BCD
Laser diode	SPLPL85	—	VT2-850M-1W-BC-A	—
V_{in} (V)	70	3 – 5.5	3.3	54
f_{sw} (MHz)	0.02 – 0.1	200	100	40
I_{peak} (A)	~ 10	≤ 0.5	≤ 2.3	≤ 18.55
t_{pw} (ns)	10 – 50	≥ 0.464	5	~ 0.850
P_{opt} (W)	—	≤ 0.25	≤ 1.8	—
t_{opt} (ns)	—	0.074 – 5	5	—
P_{draw} (mW)	591	—	—	—
η_{elec} (%)	4.2	35.2	75.6	18.5

Table 2.4 – State-of-the-art of the series current-mode laser diode driver performances.

forward voltage and the required saturation voltage, is needed. Hence, a series current-mode driver does not appear as suitable when aiming for low-voltage operation. Similarly, conduction losses across a transistor in saturation will eventually limit the power efficiency of the circuit.

Finally, parasitic inductance is a predominant restricting factor for transient performance. This calls for optimizing the physical interconnects between the laser diode and the driver. Another solution is to increase the input voltage so that the desired rise time is obtained [54]. Still, this would further decrease power efficiency through conduction losses. Also, it is important to keep in mind that the finite voltage rating of transistors put a limit on the input voltage increase.

2.2.3 The voltage-mode driver

To the best of our knowledge, the implementation of a voltage-mode laser diode driver is reported only once in the literature [57]. Referring to Figure 2.11a, the voltage-mode structure consists in connecting the load in series with a voltage source V_{in} and a switch M_{sw} [11]. This topology is nearly similar to a capacitive discharge resonant driver, the main difference being the relative value of the components. Here, capacitor C_{in} is the decoupling capacitance associated with V_{in} . Then, the laser pulse duration is set by the gate signal of M_{sw} , which is similar as compared to current-mode drivers.

In [57], a DC-DC boost converter has been employed to generate an input

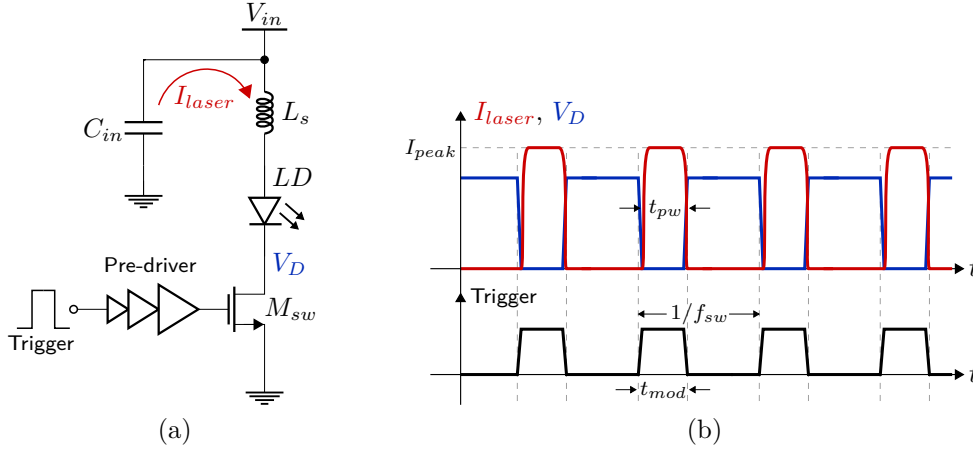


Figure 2.11 – Voltage-mode laser diode driver topology: (a) circuit architecture, (b) timing sequence.

voltage V_{in} of 10V. In addition, a correction circuit based on average current sensing regulates V_{in} so that the driving current peak is kept constant. The DC-DC converter, the control circuitry and the pre-driver have been jointly implemented on-chip and fabricated in a 55nm CMOS technology. The resulting die size is $1.96mm \times 1.85mm$. On the other hand, the switch has been realized by a discrete GaN FET, EPC2040, sustaining up to 15V continuous drain-source voltage.

The experimental measurement results of the prototype are summarized in Table 2.5. The driver is able to produce a driving current pulse up to 28A with a duration of 900ps and rise and fall times of 200ps. In terms of power efficiency, the available data do not permit to estimate the consumption of the circuit.

Parameter	Value
V_{in} (V)	10
f_{sw} (MHz)	200
I_{peak} (A)	28
t_{pw} (ns)	0.9
t_r (ns)	0.2
t_f (ns)	0.2
Area (mm ²)	3.626

Table 2.5 – Experimental results of the voltage-mode driver.

The advantages of the voltage-mode topology include the potential for low-voltage operation. In comparison with a series current-mode driver, the output stage only comprises a switching device. Thus, the laser diode's forward voltage

is not limited by saturation voltage headroom. In the same vein, the power efficiency is expected to be higher as there is no conduction losses across a constant current source. Furthermore, unlike a resonant capacitive discharge driver, the pulse repetition frequency is not limited.

It is accepted that the forward voltage of laser diodes depends to a large extent on temperature. Generally speaking, the diode voltage tends to drop with device heating. The direct consequence is a rise in driving current, thus forming a positive feedback, *i.e.* thermal runaway [11]. In a capacitive discharge driver, thermal runaway is inherently mitigated due to the fixed pulse energy defined by the storage capacitor whereas in a current-mode driver, the pulse energy is regulated through a controlled current source. For voltage-mode structures, controlling the driving current appears as a challenging task, requiring both a current sensing scheme and a control over V_{in} . This will eventually translate into an increase in the size and complexity of the circuit.

Last but not least, in the same manner as for a series current-mode circuit, a voltage-mode driver's transient performance is strongly limited by parasitic inductance. Thus, the assembly of the circuit must be optimized with careful wiring of the laser diode.

2.3 Performance landscapes

The aim of this section is to review and discuss all literature results previously pointed out throughout this chapter. To this end, parameters of interest are plotted versus each other so as to form several performance landscapes. Another goal herein is to highlight possible design trends and compromises.

Figure 2.12 presents the driving current peak plotted against the input voltage. Markers are distinguished depending on driver topology. The plot expressly highlights that increasing the current capability calls for a higher voltage level, regardless of circuit architecture. This emphasizes that the design target of the present thesis involves conflicting requirements. Additionally, recently published studies show that the current design trend for pushing forward the increase in driving current is supported by the GaN technology [47, 48, 57]. As already explained, the use of GaN-based switching devices contributes to reduce parasitic inductance, which in turn allows for a significant performance enhancement.

Another reading of that plot is that employing a capacitive discharge resonant driver leads to the need for a high supply voltage.

Figure 2.13 plots the pulse repetition frequency against the input voltage. One can clearly see that combining both low-voltage and fast switching operation has been completed so far by current-mode and voltage-mode structures. Moreover, the plot stresses the limitation of the resonant topology in terms of

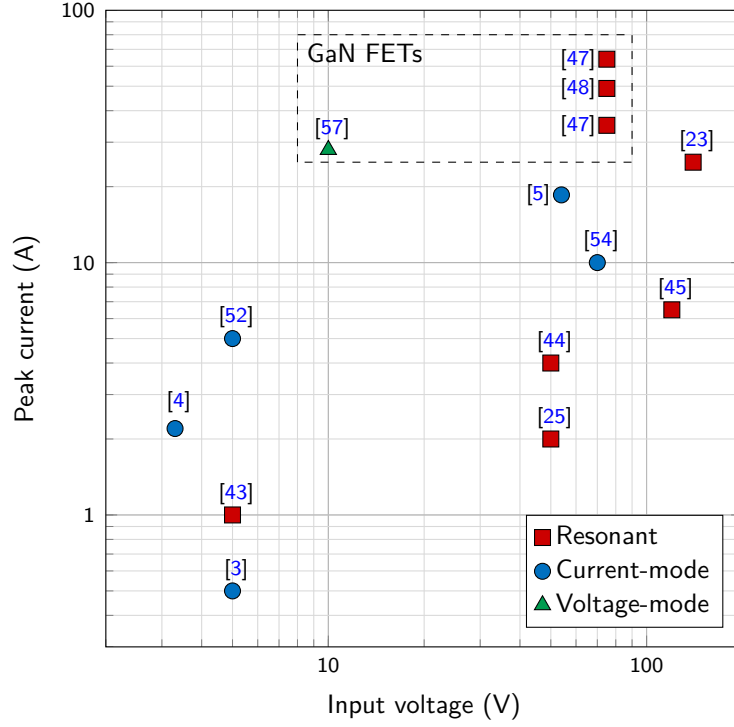


Figure 2.12 – Driving current peak versus input voltage.

switching speed, most notably due to the recharge time of the energy storage capacitor.

Figure 2.14 illustrates the driving current peak plotted against the pulse duration. Here, markers are divided according to input voltage range. On the face of it, there is no apparent trend on the plot. A possible reading is that the ability to generate short current pulses with a high magnitude is strongly dependent on circuit implementation, technology and layout, which in turn set the amount of parasitics in the current loop through the laser diode. This is clearly emphasized by the studies presented in [54] and [5] which are both based on a current-mode topology with an on-chip current sourcing stage. The key difference is the value of the parasitic loop inductance. In [5], the inductance is kept in the nanohenry range, thus allowing for much faster current transients as compared to [54] where the parasitic inductance equals $20nH$.

It is worth noting that the voltage-mode driver reported in [57] stands out with very good performances in terms of driving current pulse's features while operating at a reasonable input voltage of $10V$. This is because it combines the inherent low-voltage functioning of a voltage-mode structure with a GaN FET and an optimized laser diode mounting.

The plot also outlines the design trade-off between peak current and pulse width when choosing the value of the energy storage capacitor in capacitive discharge resonant topologies. In [25], a $33pF$ capacitor is chosen, thus result-

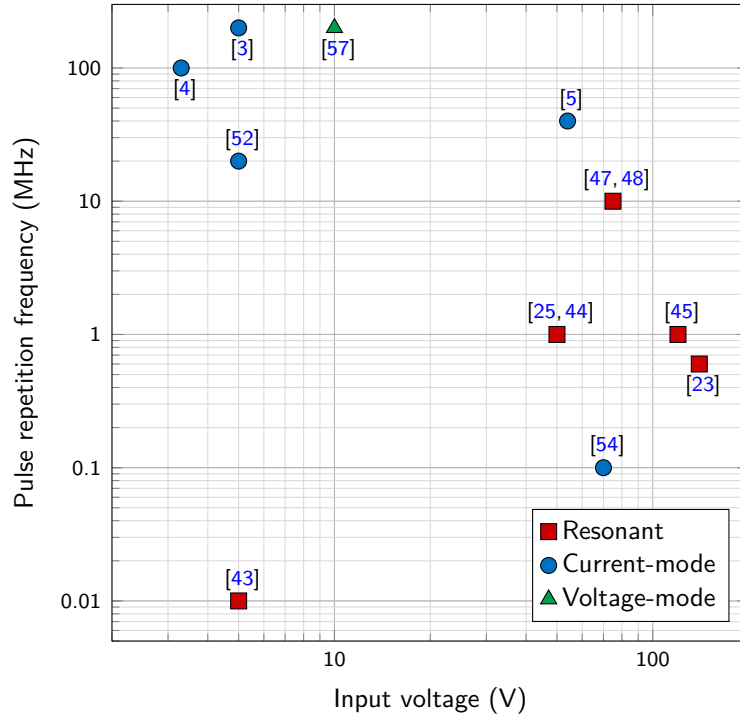


Figure 2.13 – Maximum pulse repetition frequency versus input voltage.

ing in a $2A$ driving current pulse with a duration of $1ns$. In contrast, in [47], the capacitor is set to $1.1nF$, which leads to a much higher current, up to $64A$, but also to a longer pulse width of $5.6ns$.

It is important to keep in mind that results are derived from different implementations, either discrete or fully integrated, employing various laser diode technologies and packaging. This means that, even though these landscapes provide an insight into the pros and cons of each topology, they are not fully relevant and rigorous. This is the aim of the upcoming chapter to further compare in a similar hardware environment the existing laser diode driver topologies and point out the associated design issues and trade-offs.

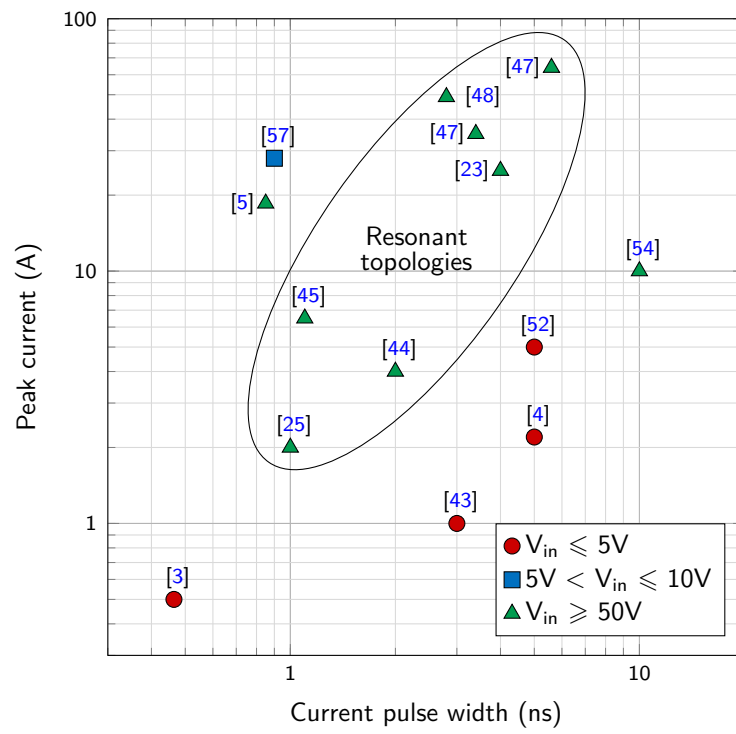


Figure 2.14 – Driving current peak versus pulse width, parametrized as a function of the input voltage range.

3 Pre-design and feasibility study

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This chapter covers several pre-design considerations. These include a presentation of the $40nm$ CMOS technology portfolio as well as a detailed overview of the laser diode technology and the vehicle hardware. The final objective is to carry out a feasibility study so as to propose a driver circuit architecture fitted for meeting the electrical specifications.

3.1 Technology overview

The $40nm$ bulk CMOS technology is dedicated to low-power applications, such as mobile and wireless. Thanks to the SPAD process option, it is the

current technology of choice for developing direct time-of-flight products in STMicroelectronics. The process uses a p -doped silicon substrate. The back-end metal stack is composed of seven layers (M1-M7Z), with the two upper layers being thicker for guaranteeing power distribution.

The key features of the process flow are listed below:

- Shallow trench isolation (STI) is a common approach for device isolation in CMOS technology. It consists in etching the surface of the wafer in order to form dielectric regions, called field regions, between the active silicon areas in which transistors lie [58].
- Retrograde vertical profile for well implantation to lower the sheet resistance of wells and enhance latch-up immunity.
- Triple-well technology which allows to electrically isolate a p -well from the substrate [59].
- Self-aligned silicide deposit to reduce the sheet resistance of polysilicon gates and active silicon regions [58, 60].
- Chemical mechanical polishing on STI, metals and vias for enhanced planarization prior to photolithography [58].
- Dual-Damascene technique for copper wiring [58].

3.1.1 Passive components

The 40nm technology node supports the standard passive components, *i.e.* resistor, capacitor and inductor.

A resistor can be realized by either $n+$ or $p+$ active regions, n -well or p -well and polysilicon or metal layers. In the same way, several capacitor structures are available: metal-oxide-semiconductor (MOS), metal-oxide-metal (MOM) as well as metal-insulator-metal (MIM). These are extensively described in the upcoming chapter. Last, an inductor can be fabricated from the back-end metal stack. Generally speaking, multiple metal layers are to be used in order to reduce the inductor's series resistance and therefore get a reasonable quality factor. Figure 3.1 shows the microphotograph of a $\sim 1.2nH$ inductor realized using the 40nm technology node. The surface occupied by the device is approximately $230\mu m \times 245\mu m$, which is quite area consuming.

3.1.2 Switching devices

Switching devices in the 40nm technology are classical n -channel and p -channel MOSFETs. These are available at different voltage ratings depending on gate oxide thickness and channel length.

The cross section of an n -channel MOSFET (NMOS) is shown in Figure 3.2a. The drain and source terminals of the transistor are realized by two $n+$ regions implanted in the substrate. The gate terminal is formed by polysilicon, which is grown over a thin layer of silicon dioxide, namely the gate oxide. Note



Figure 3.1 – Microphotograph of an inductor realized in 40nm CMOS technology.

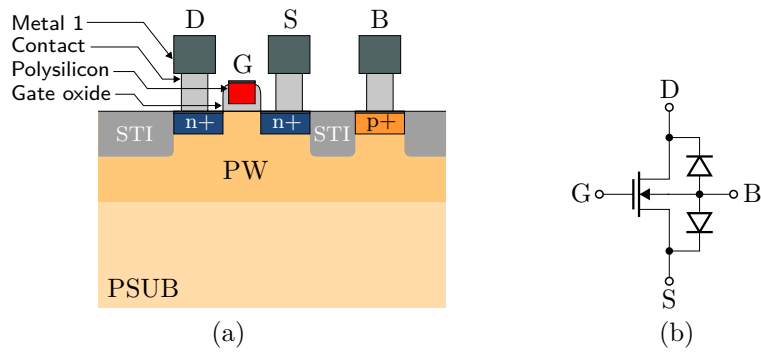


Figure 3.2 – n -channel MOSFET: (a) cross section, (b) equivalent circuit.

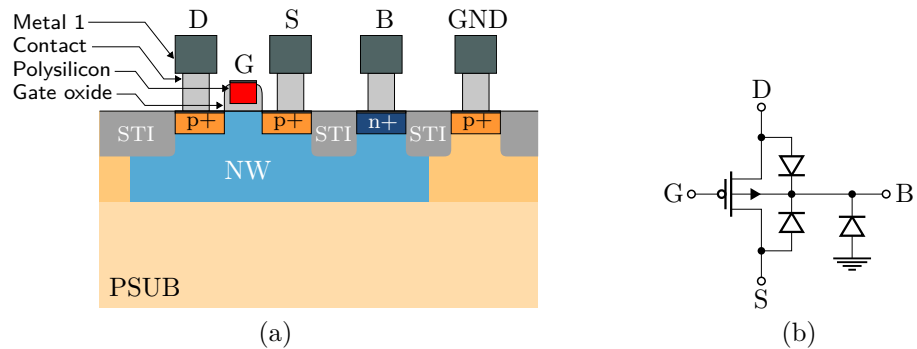


Figure 3.3 – p -channel MOSFET: (a) cross section, (b) equivalent circuit.

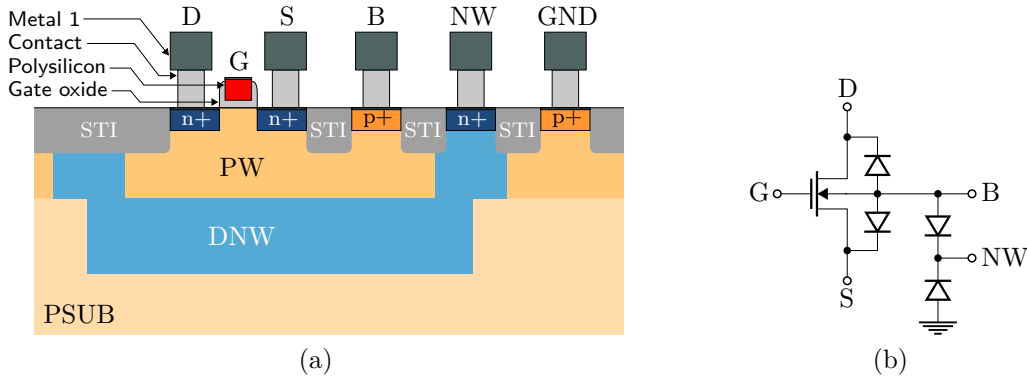


Figure 3.4 – Isolated n -channel MOSFET: (a) cross section, (b) equivalent circuit.

that the bulk and the substrate cannot be differentiated and are connected to the same potential. The equivalent electrical circuit of the transistor is depicted in Figure 3.2b. Two parasitic junctions exist between the bulk and the drain and source terminals. Given that the substrate is usually tied to the lowest potential available in the chip, the junctions are reverse-biased.

A p -channel MOSFET (PMOS) must be fabricated in a n -well (NW) acting as the bulk. The corresponding cross section is represented in Figure 3.3a. Two p^+ diffusions in the NW are placed on both sides of the polysilicon gate to form the drain and source terminals of the transistor. The bulk is connected through an n^+ implant in the NW. The equivalent electrical circuit of the transistor is depicted in Figure 3.3b. In addition to the junctions associated with the drain and source terminals, the n -well creates a junction between the bulk and the substrate. Accordingly, the bulk must be tied to a potential such that these junctions remain reverse-biased.

Furthermore, a triple-well process allows the implementation of an isolated n -channel MOSFET. The cross section is shown in Figure 3.4a. Unlike the structure of a regular NMOS, the p -well (PW) is electrically isolated from the substrate by a deep n -well (DNW). In this way, the bulk can be tied to a potential different than the one of the substrate. The equivalent circuit of the structure is depicted in Figure 3.4b. The implantation of a DNW creates two additional junctions associated with the bulk and the substrate. Typically, the DNW is connected to the highest potential available in the chip to ensure that the junctions are reverse-biased.

The n - and p -channel MOSFETs are available at different voltage ratings: thin-oxide 1.1V MOSFET, thick-oxide 2.5V MOSFETs and thick-oxide 3.3V MOSFET. The difference between 2.5V and 3.3V devices is essentially the minimum channel length which is extended from $0.27\mu\text{m}$ to $0.55\mu\text{m}$ and

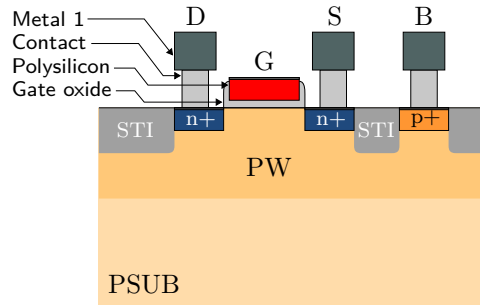


Figure 3.5 – Cross section of a 3.3V n -channel MOSFET.

$0.44\mu m$ for NMOS and PMOS, respectively. In this way, the safe operating area is increased up to 3.6V. Figure 3.5 illustrates the cross section of a 3.3V n -channel device.

3.2 Laser diode technology

The vertical-cavity surface-emitting laser (VCSEL) appears as the ideal light source in time-of-flight sensors due to their superior properties in comparison with conventional edge-emitting lasers (EEL). This is the aim of this section to cover the fundamental aspects of VCSELs. Key modelling points that are especially important for the design of the driving circuitry are outlined. Finally, a presentation of the VCSEL array in use and the available models is provided. Even though VCSELs can be designed to lase over a wide range of wavelengths, the focus is on VCSELs that emit within the $830nm$ to $950nm$ spectral region, *i.e.* compatible with the existing silicon-based detector technology [7]. For more details, an extensive description of the near-infrared VCSEL technology as well as basic knowledge on semiconductor laser diodes are available in [Appendix B](#).

3.2.1 What is a VCSEL?

The VCSEL is a rather recent type of semiconductor laser device, being commercially available since 1996 [61]. It shows attractive features for infrared sensing applications as compared to conventional Fabry-Pérot EELs, among which stand out:

- The narrow emission spectrum and low thermal shift of the lasing wavelength ($\sim 0.07nm/K$) which allow to combine the detector with narrow spectral filter, thus enhancing environmental light rejection [7, 33, 62, 63].
- The circularly-symmetric beam with low divergence making the integration of coupling optics straightforward [33, 62, 64].
- The scalability in two-dimensional arrays enabling adaptive power levels and speckle-free imaging [33, 62].

Table 3.1 summarizes the key characteristics of VCSELs compared with edge-emitters [7, 33, 62–68].

Name	EEL	VCSEL
Manufacturing cost	–	++
Reliability	–	+
Continuous-wave power	++	–
Wall-plug efficiency	++	+
Modulation bandwidth	+	++
Beam shape	–	++
Spectral width	+	++
Spectral thermal shift	–	++

Table 3.1 – Key features of VCSELs compared to EELs.

3.2.1.1 Device structure

VCSELs, like most semiconductor laser devices, incorporate a thin slab of intrinsic active material placed inside a $p-n$ junction. The latter is made from a combination of semiconductor materials having different band gap energies so as to create an heterostructure [64, 69]. The laser cavity is then formed by surrounding the heterostructure with two highly reflecting mirrors, referred to as Bragg reflectors, which provide optical feedback. In VCSELs, the light propagates perpendicularly to the wafer plane and is emitted from the upper surface. In addition, carrier confinement into the small volume of the active medium and index guiding are usually provided by selective oxidation [64, 67]. The basic structure of an oxide-confined VCSEL is represented in Figure 3.6 [64–67]. Typically, VCSELs emitting in the near-infrared spectral range are epitaxially grown on an n -doped gallium arsenide (GaAs) substrate [65].

3.2.1.2 Static characteristics

Figure 3.7 shows the common light-current-voltage ($L-I-V$) characteristics of a VCSEL under continuous-wave (CW) operation. Above the lasing threshold current I_{th} , the optical power P_{opt} is a linear function of the bias current I dictated by the slope efficiency $\eta = \frac{\Delta P_{opt}}{\Delta I}$. The $L-I$ curve can be described by,

$$P_{opt} = \eta(I - I_{th}) \quad (3.1)$$

Simultaneously, a voltage V with a diode-like behavior builds up across the device. Once the lasing turn-on potential V_{on} ($\sim 1.4 - 1.6V$) is reached, the

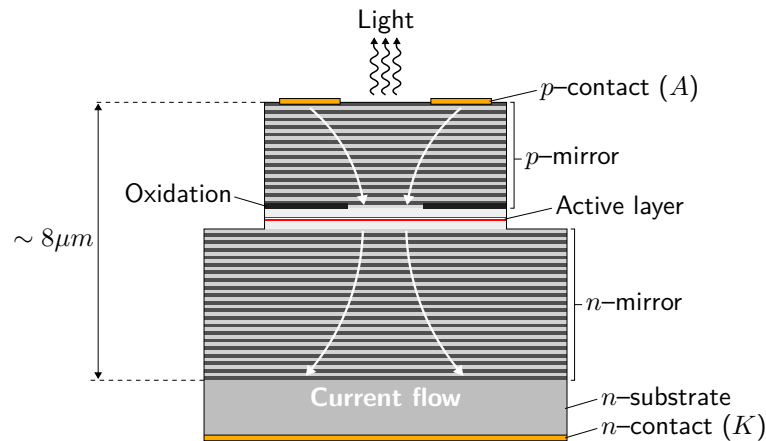
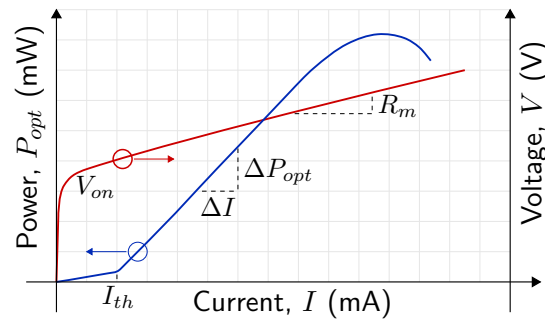


Figure 3.6 – Cross-sectional view of an oxide-confined VCSEL.


 Figure 3.7 – Typical $L - I - V$ static curve of a VCSEL.

voltage increases roughly linearly with bias current. The $I - V$ curve can be accurately modelled using the Shockley diode equation [70–72],

$$V = R_m I + n V_T \ln \left(1 + \frac{I}{I_s} \right) \quad (3.2)$$

where, R_m is the electrical series resistance, I_s is the reverse saturation current, n is an ideality factor and V_T is the thermal voltage, that is approximately 25.85mV at room temperature.

At a particular bias point, the CW power of VCSELs saturates and eventually begins to drop with a further increase in current. This so-called thermal roll-over is due to device self-heating and translates into a rapid rise of internal losses [62, 63, 73]. This phenomenon depends, to a large extent, on the operating regime, either CW or pulsed. It is accepted that driving the VCSEL with short pulses at low duty cycle ($\sim 10\%$) can substantially extend the linear range of the power curve [62, 63].

3.2.1.3 Dynamic response

The dynamic response of semiconductor lasers to a driving current step displays a turn-on delay followed by high-frequency (greater than a ten of

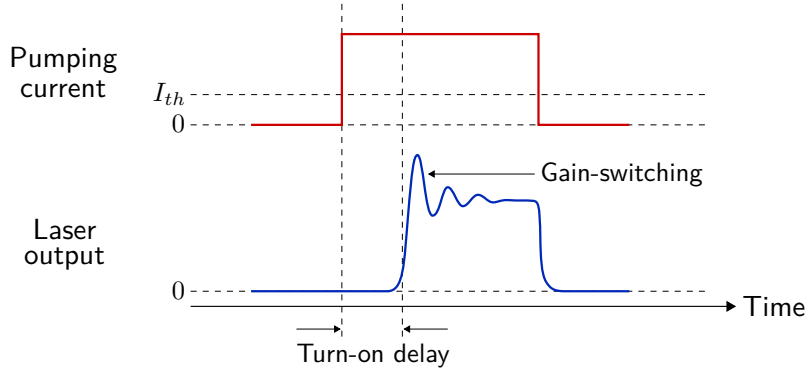


Figure 3.8 – Dynamic response of a directly modulated semiconductor laser.

gigahertz for VCSELs [65]) relaxation oscillations (see Figure 3.8) [74].

The turn-on delay results from the initial build up of the photon density up to the lasing threshold. Only when the optical gain is unity, the device starts to lase. This delay is related to the carrier lifetime, the lasing threshold current as well as the driving current. On the other hand, the gain-switching phenomenon occurs when the pumping current exceeds the laser threshold. Indeed, as the laser goes from spontaneous to stimulated emission, the carrier recombination lifetime is greatly reduced. In consequence, a large amount of carriers is rapidly depleted, thus resulting in a short flash of light. Then, relaxation oscillations occur until the electron and photon populations within the structure reach equilibrium.

These transient phenomena are often a major concern in datacom, in particular at high data rate. Therefore, the laser diode is pre-biased near the threshold current to reduce the turn-on delay and damp the oscillations. Yet, even below threshold, the laser still emits a small amount of incoherent photons through spontaneous recombination. In TOF ranging, spontaneous emission can impact the signal-to-noise ratio for distance measurement. Hence, it is preferable not to use a pre-biasing technique in the laser driving electronics. Furthermore, the turn-on delay does not appear as a critical issue. As a matter of fact, since the laser pulse's transit time is measured relatively to the transmitted pulse, the delay is taken into account in the measurement.

3.2.2 VCSEL modelling

3.2.2.1 Intrinsic laser dynamics

As for any laser diodes, the dynamics of VCSELs can be described using a set of phenomenological rate equations (3.3) [75]. These relate the evolution of the carrier and photon density within the active region.

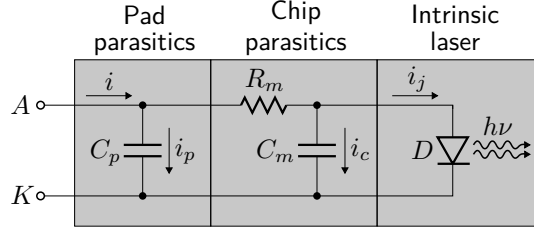


Figure 3.9 – Equivalent circuit model of a VCSEL.

$$\begin{aligned} \frac{dN}{dt} &= \frac{\eta_i I}{qV_{qw}} - \frac{N}{\tau_n} - v_g g S \\ \frac{dS}{dt} &= S \left(\Gamma v_g g - \frac{1}{\tau_s} \right) + \Gamma \beta_{sp} R_{sp} \end{aligned} \quad (3.3)$$

where:

- N is the carrier density in the active region and S is the photon density into the cavity.
- I is the bias current, η_i is the injection efficiency, q is the electron charge and V_{qw} is the volume of the active medium. Then, the term $\frac{\eta_i I}{qV_{qw}}$ is the rate of injected electrons per unit volume in the active region [75].
- τ_n is the carrier lifetime. The term $\frac{N}{\tau_n}$ represents the natural carrier decay process, which is primarily related to spontaneous and non-radiative recombinations [75].
- v_g is the group velocity and g is the gain per unit length. Hence, the term $v_g g S$ is the rate of photon-stimulated recombinations.
- τ_s is the photon lifetime into the cavity. The term $\frac{S}{\tau_s}$ depicts the photon decay process, which accounts for internal absorption and scattering losses as well as for the useful light transimission occuring at the front cavity mirror [75].
- Γ is the confinement factor. Generally speaking, the cavity volume (occupied by photons) is larger than the active medium volume (occupied by electrons). Then, the factor Γ represents the electron-photon overlap within the laser structure [75].
- β_{sp} is the spontaneous emission coupling factor and R_{sp} is the spontaneous recombination rate. The term $\Gamma \beta_{sp} R_{sp}$ is the spontaneous recombination rate coupled into the lasing mode.

3.2.2.2 Electrical circuit model

The VCSEL can be electrically modelled by a $p-n$ junction diode, designating the intrinsic laser wherein carriers and photons interact, together with the surrounding extrinsic parasitics. The common electrical circuit model is shown in Figure 3.9 [71, 72, 76–79]. The laser dynamics is a direct function of the pumping current i_j flowing through the junction.

The extrinsic parasitics can be directly superimposed on the device structure seen in Figure 3.6. These appear as a major concern when aiming for high-speed devices. Indeed, parasitics limit the bandwidth by shunting a portion of the terminal current away from the intrinsic laser, as highlighted by i_p and i_c .

The pad capacitance C_p represents the parasitic coupling between the p - and n -type metallizations. Its value depends on the pad layout as well as the material between the pads [76, 78].

The chip resistance R_m is the overall series resistance. It is mostly dominated by the resistance from the p - and n -doped mirrors [76]. As a matter of fact, Bragg reflectors are realized by multiple semiconductor layers with alternating high and low refractive index. Due to the short optical cavity of the VCSEL, 20 layer pairs are usually required so that the reflectivity can exceed 97% [67]. Consequently, the successive heterojunctions in the Bragg mirrors form a large potential barrier which results in a substantial voltage drop [62, 76]. In addition, R_m includes the resistance associated with the p - and n -type ohmic contacts as well as the sheet resistance through the n -type contact layer [76, 78].

The chip capacitance C_m primarily represents the junction capacitance of the active region wherein current flows. Under forward bias, it is mainly dominated by the diffusion capacitance induced by the accumulation of minority carriers in the heterostructure (electrons in the p -type region) [80, 81]. For oxide-confined VCSELs, C_m also accounts for the capacitance of the oxidized layer as well as for the junction capacitance associated with the intrinsic active layer underneath the oxide [76].

3.2.3 The VCSEL array

The laser diode employed as part of the doctoral project is an array of seven VCSELs connected in parallel on the same die. All having a common cathode electrode. The use of multiple VCSELs (commonly referred to as mesas) on one chip does not impact the laser features, meaning that the performance is primarily defined by the individual laser [63]. Essentially, current and power for an array simply scale with the number of parallel-connected mesas while the voltage remains unchanged.

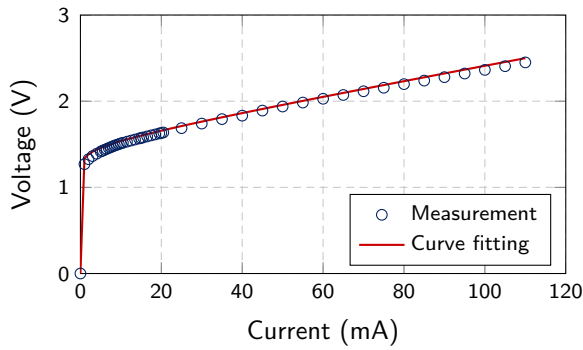
The VCSEL array was provided by an external manufacturer. This specific device has been chosen because it was already being used for product development within STMicroelectronics. This laser is formerly designed for a driving current of $120mA$. Then, the design target is to enable overdriving with sub- ns current pulses up to $200mA$.

The typical electro-optical characteristics of the VCSEL array are listed in Table 3.2.

Afterwards, this part presents the available models of the VCSEL array as well as their limitations.

Parameter	Value
Lasing wavelength (nm)	940
Threshold current (mA)	15
Slope efficiency (W/A)	~ 0.8
Lasing voltage (V)	~ 1.5
Beam divergence ($^\circ$)	~ 25

Table 3.2 – Characteristics of the VCSEL array.



(a)

Parameter	Value
R_m (Ω)	~ 8.3
n (-)	~ 2
I_s (fA)	~ 20

(b)

Figure 3.10 – Curve-fitted electrical model of the VCSEL array: (a) $I - V$ data curve-fitting with Shockley diode equation, (b) extracted value of the model's parameters.

3.2.3.1 Curve-fitted electrical model

In order to design the driving circuitry, we have built an electrical VCSEL model. Knowing that only $I - V$ measurement data were available, the model was developed from $I - V$ curve fitting based on the Shockley diode equation 3.2. The curve fitting process that have been performed with Matlab *optimization toolbox* is illustrated in Figure 3.10a. The extracted values of the series resistance R_m , the saturation current I_s and the ideality factor n are presented in Table 3.10b.

So as to form the VCSEL equivalent circuit as seen in Figure 3.9, I_s and n were incorporated into a SPICE diode model, serially connected with a resistance of value R_m . Finally, pad and chip capacitances were provided by the manufacturer to complete the model, $C_p = 300\text{fF}$ and $C_m = 1.05\text{pF}$.

Since $I - V$ data were measured up to 110mA , the forward voltage beyond this bias point is extrapolated assuming a strict linear behavior, $V = V_{on} + R_m I$. Accordingly, a voltage of 3.2V (*i.e.*, higher than the specified supply voltage) must be applied across the VCSEL so that the targeted 200mA current can be reached.

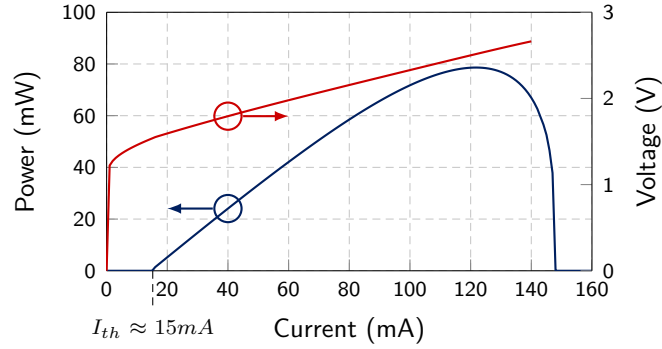


Figure 3.11 – Simulated CW $L - I - V$ curve of the VCSEL array at room temperature.

It is worth keeping in mind that the present model exhibits significant limitations. First, it does not capture the intrinsic VCSEL behavior governed by the rate equations. Therefore, the electrical model allows to monitor the driving current flowing through the VCSEL, but does not provide the corresponding laser pulse. Furthermore, the thermal dependance of the model parameters is not taken into account. Typically, the VCSEL's forward voltage will tend to decrease with increasing temperature. Thus, the model is only relevant around room temperature, that is the temperature at which $I - V$ measurements were performed.

3.2.3.2 Electro-optical model

At a later stage, an electro-optical VCSEL model was provided by the manufacturer. In such a model, the rate equations are translated into an equivalent sub-circuit as described in [70, 82].

The simulated static characteristics of the VCSEL array is represented in Figure 3.11. The power curve (in blue) clearly shows the thermal roll-over occuring at a bias current of approximately 120 mA . As expected, the voltage curve is in agreement with the curve-fitted model.

It is important to note that the electro-optical model has not been employed for circuit desing. As a matter of fact, it exhibits strong convergence issues which prevent proper simulation. Still, the model was exploited to validate some concepts which will be discussed later on.

3.3 Hardware environnement

The aim of this section is to give a thorough overview of the vehicle circuit shown in Figure 3.12. The emphasis is put on the modelling of the physical interconnect between the VCSEL and the driving electronics. Some considerations about power distribution are also presented.

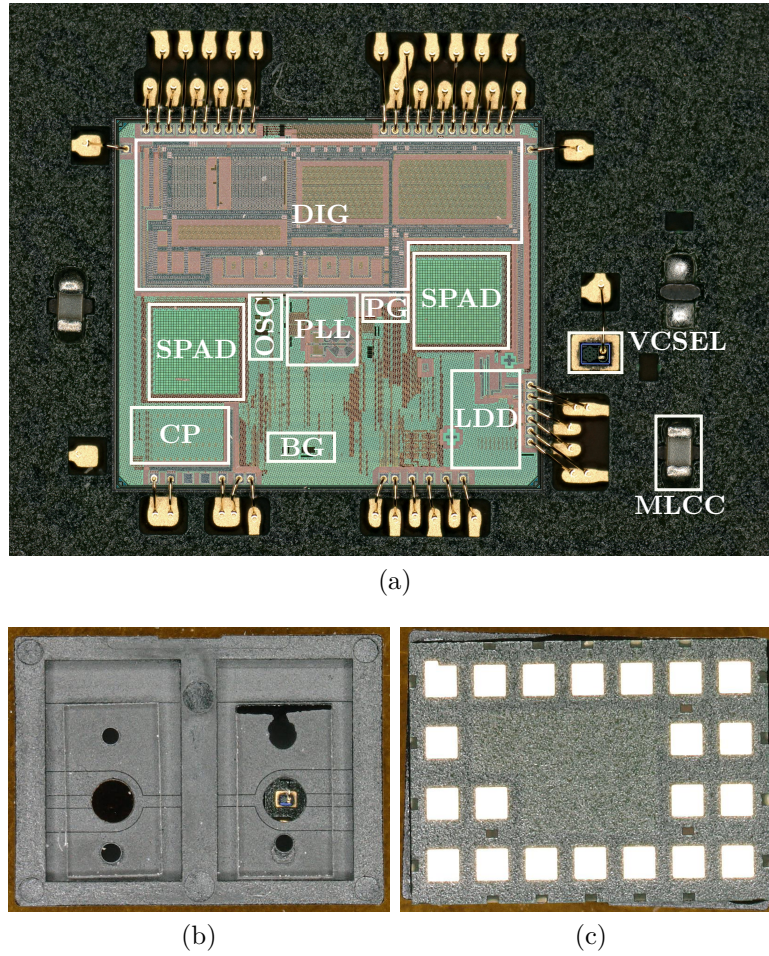


Figure 3.12 – Vehicle circuit: (a) microphotograph of the silicon die, (b) module's top view with optical apertures, (c) module's bottom view.

3.3.1 The vehicle circuit

So as to benefit from a complete and functional hardware environment, a STMicroelectronics' vehicle chip (STVC) has been re-used as a basis for carrying out the design. The STVC is an all-in-one time-of-flight ranging sensor designed by STMicroelectronics. It incorporates a silicon IC mounted onto a substrate together with the VCSEL bare die and multi-layer ceramic capacitors (MLCC). A microphotograph of the assembly is shown in Figure 3.12a. The size of the substrate is $5.84mm \times 4.24mm$ with a thickness of $300\mu m$. As illustrated in Figure 4.33b and 3.12c, the whole setup is housed in a compact land grid array (LGA) optical module with coupling optics.

The IC was designed and fabricated by STMicroelectronics using the $40nm$ CMOS technology. The die size is $3.33mm \times 2.89mm$.

The main building blocks are:

- A digital unit (DIG) which includes, among others, programmable registers for controlling the operation of the system.
- A bandgap circuit (BG) for generating the necessary reference voltages and currents.
- Two SPAD arrays, one for echo pulse detection and one positioned in the vicinity of the VCSEL in order to set the reference time for range measurement.
- A 40V switched capacitor DC-DC converter (CP) which generates the bias voltage of the SPADs for Geiger-mode operation.
- A laser diode driver (LDD) with dedicated laser safety circuitry.
- A pulse generator (PG) which internally generates the modulation signal of the laser.
- A phase-locked loop (PLL) and an oscillator (OSC), whose key functionality is to enable tunability of the signal modulating the laser.

Inside the chip, the area available for the VCSEL driver is approximately $820\mu m \times 420\mu m$. The circuit has a typical supply voltage range of $[2.5V, 3.6V]$ with dedicated power supply and ground pins, V_{DD} and V_{SS} . Also, it has one anode pin (V_A) and one cathode pin (V_K) for connecting the VCSEL.

The re-use of a previously designed chip allows for a "plug and play" approach. In this way, the purpose was to simply substitute the proposed laser diode driver circuit to the existing one, therefore eliminating time-consuming design work. This is particularly convenient when it comes to on-chip high-speed signal generation. Here, the vehicle hardware incorporates a phase-locked loop (PLL) which permits to set the features of the signal modulating the laser. The pulse width is configurable within the range $[125ps, 9ns]$ with a $125ps$ time stepping. Similarly, the pulse repetition frequency can be selected from the following values, $[62.5MHz, 120MHz, 170MHz, 250MHz]$.

3.3.2 VCSEL interconnect modelling

The physical interconnect between the driver chip and the VCSEL results in a complex electrical response [83]. Thus, a circuit model for the interconnect is critical to properly capture the transient propagation of signals with simulation. Especially, it is accepted that parasitic inductance can lead to a significant bandwidth limitation. Also, it may cause large voltage spikes during current transient, thus adversely affecting the circuit's reliability.

Within the STVC, the VCSEL die is attached on a dedicated metal pad from its back cathode contact using an electrically conductive glue. On the other hand, wire bonding is used to connect the upper anode contact. Then, two copper traces through the substrate as well as two gold bond wires are

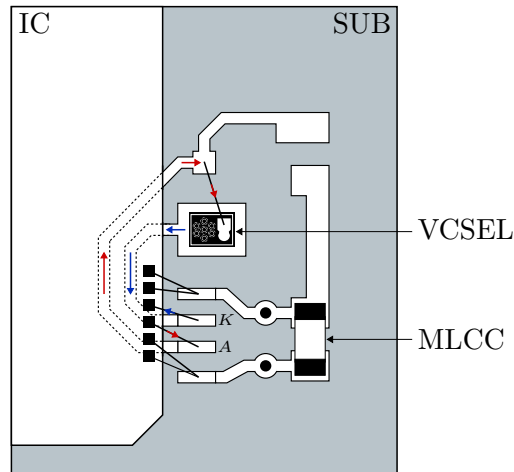


Figure 3.13 – Drawing of the on-substrate physical interconnects (not on scale).

added to close the current loop through the VCSEL. A schematic drawing of the interconnect is represented in Figure 3.13.

The modelling of the physical structure of interconnects is well described in literature. The aim of this part is to apply the theoretical formulas in [84] so as to estimate the parasitics of the different interconnect segments, *i.e.* bond wires and traces, from their geometry.

Individually, each of these segments can be seen as electrically short against the minimum wavelength in the bandwidth of interest. The wavelength λ is defined as the ratio between the velocity of propagation v and the frequency f of the waves traveling along the interconnect. Additionally, the maximum frequency f carried by the interconnect under transient excitation can be derived from rise time t_r [85].

$$\lambda_{min} = \frac{v}{f_{max}} \quad \text{with,} \quad f_{max} = \frac{0.35}{t_r} \quad (3.4)$$

On the basis of a realistic rise time of $50ps$, the minimum wavelength equals approximately $25mm$. Note that the velocity of wave propagation is taken to be about 60% of that of free space ($\sim 3 \times 10^8 m.s^{-1}$) [86]. As the physical dimension of the interconnect ($\sim mm$) is only a small portion of the wavelength, it is reasonable to build a lumped RLC network to model the interconnect [86, 87].

The self partial inductance for a round wire L_{bw} and a trace of rectangular cross section L_t can be calculated from,

$$\begin{aligned}
 L_{bw} &= \frac{\mu_0}{2\pi} l \left[\ln \left(\frac{2l}{r} \right) - 1 \right] \\
 L_t &= \frac{\mu_0}{2\pi} l \left[\ln \left(\frac{2l}{w+t} \right) + \frac{1}{2} \right]
 \end{aligned} \tag{3.5}$$

where l is the length, r is the wire radius and w and t are the trace width and thickness respectively. In addition, mutual inductance must be algebraically subtracted from self inductance in order to calculate the net partial inductance of each segment. The mutual partial inductance M between two parallel conductors is expressed from the spacing s as,

$$M = \frac{\mu_0}{2\pi} l \left[\ln \left(\frac{2l}{s} \right) - 1 \right] \tag{3.6}$$

Summing the net partial inductances associated with each segment allows to compute the overall loop inductance in the current path through the VCSEL [88]. It is important to keep in mind that these formulas are only valid for straight lines under the assumption that the cross-sectional dimensions are negligible compared with the length.

The parasitic resistance is theoretically calculated using $R = \rho \frac{l}{A}$, where ρ is the resistivity, l is the length and A is the section area. The value for bond wires and traces are respectively $R_{bw} = 76m\Omega/mm$ and $R_t = 12.6m\Omega/mm$.

Finally, the parasitic capacitance is derived from the parallel plate capacitor formula, $C = \frac{\epsilon A}{s}$, where ϵ is the permittivity of the dielectric, A is the area of the plates and s is the spacing between the plates.

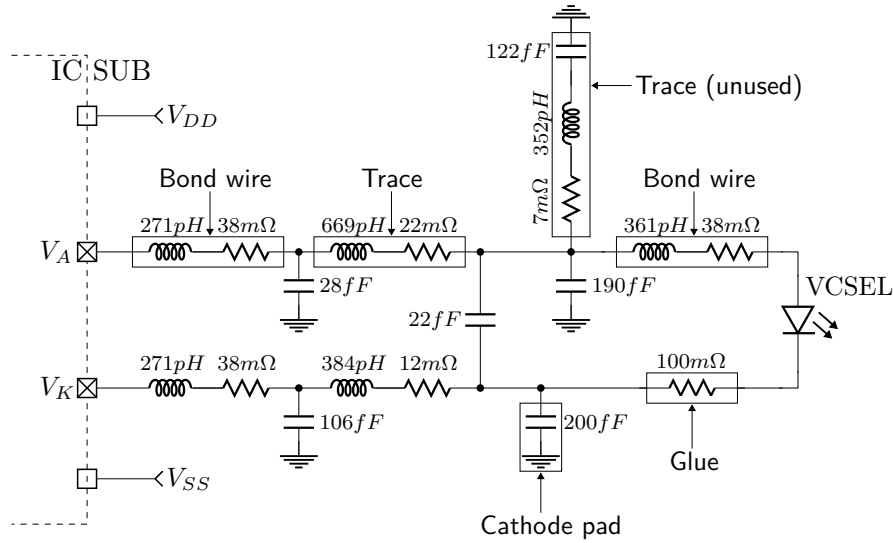


Figure 3.14 – Equivalent lumped-circuit model of the interconnect between the VCSEL and the driving electronics.

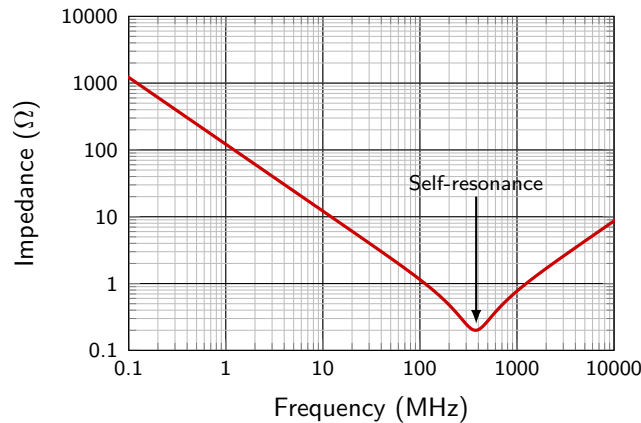


Figure 3.15 – Impedance versus frequency characteristic of the on-substrate MLCC.

The equivalent lumped-circuit model of the interconnect is shown in Figure 3.14. The resistivity of the conductive glue used for attaching the VCSEL die was also taken into account with resistance $R_{glue} = 100m\Omega$. The total parasitic loop inductance and resistance are respectively $L_s = 1.95nH$ and $R_s = 248m\Omega$. The resulting equivalent circuit can be directly incorporated into a SPICE-like simulation environment.

3.3.3 Power distribution

The physical interconnect between the external power supply and the driver's supply and ground pins can be essentially represented by an inductance in series with a resistance. In a switching circuit, detrimental voltage fluctuations can build up across the distribution line during fast current transients. As a consequence, a circuit model for the power distribution network (PDN) is mandatory for circuit simulation. To this end, formulas for inductance and resistance calculation have been applied in order to estimate the parasitic contributions of the interconnect associated with pins V_{DD} and V_{SS} . The PDN also comprises a 0402 MLCC, which is mounted onto the substrate for decoupling purpose. This capacitor has been re-used from the latter circuit version (Murata GRM022R61A152ME19). The capacitor value is $1.5nF$ with a self-resonant frequency around $400MHz$ (see the impedance curve in Figure 3.15).

The equivalent lumped-circuit model of the PDN is presented in Figure 3.16. Note that the external power supply was modelled by a constant voltage source together with a large capacitor.

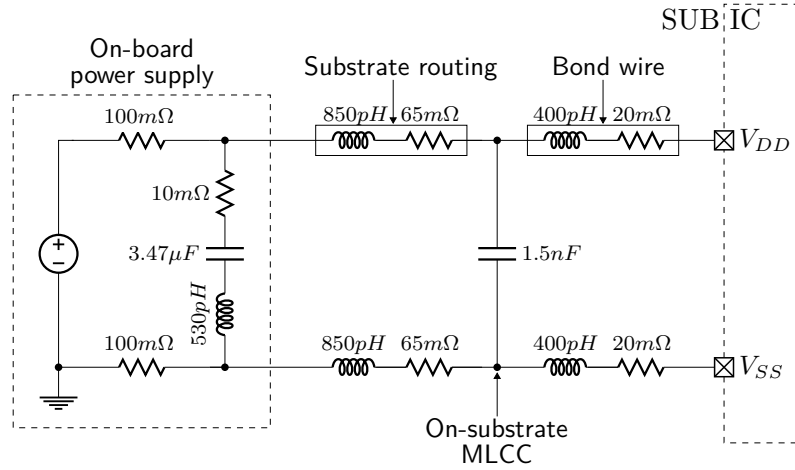


Figure 3.16 – Equivalent lumped-circuit model of the power distribution network.

3.4 Feasibility study

This section focuses on carrying out a feasibility analysis based on the different laser diode driver topologies highlighted in the preceding chapter. The final objective is to choose the most suitable circuit structure regarding design specifications.

3.4.1 Methodology

The relevant laser diode driver architectures are evaluated via circuit simulation using the CMOS 40nm technology by STMicroelectronics. Operating conditions for simulation are aligned with the technical specifications (listed in [Chapter 1](#)). The parasitics' values R_s and L_s were chosen to be consistent with those calculated from the vehicle hardware in [Part 3.3.2](#). Simulation conditions are summarized in [Table 3.3](#).

Name	Value	Unit
V_{DD}	2.5	V
f_{sw}	200	MHz
t_{mod}	1	ns
R_s	250	mΩ
L_s	2	nH

Table 3.3 – Simulation conditions for architecture evaluation.

The primary performance metrics to be looked at are transient speed, cur-

rent capability and power efficiency. Here, another goal is to get an understanding of the transient behavior of each architecture. Note that current control strategy, which is an important topic for the voltage-mode topology, is excluded from the scope of the study.

Two architectures are discussed in detail as part of the feasibility analysis:

- The voltage-mode topology employing a single low-side NMOS switch.
- The current-mode series topology employing a NMOS in saturation and a low-side NMOS switch.

Other architectures can be directly excluded from the study as they cannot meet the technical specifications:

- In the capacitive discharge resonant topology, the laser pulse shape is fixed for a given design. Accordingly, such a structure is inadequate when pulse width configurability is required. The feasibility can be quickly assessed from the analytical expressions of the driving current pulse peak and duration (see [Chapter 2](#)). For a sub- ns current pulse width ($t_{pw} \leq 1ns$), one can calculate the value required for the storage capacitor,

$$C \approx \frac{2.25}{\pi^2} \frac{t_{pw}^2}{L_s} \leq 114pF \quad (3.7)$$

Then, it is possible to estimate the necessary input voltage for $I_{peak} = 200mA$. Recall that the targeted VCSEL's forward voltage is $3.2V$.

$$V_{in} \approx I_{peak} \left(R_s + \sqrt{\frac{L_s}{C}} \right) + V_{laser} \geq 4V \quad (3.8)$$

Thus, a capacitive discharge resonant circuit appears as a complex solution given the specified supply voltage level.

- In the inductor-based shunt current-mode driver, an inductor device is required to build the constant current source. This is hardly compatible with the form factor of the STVC and would necessitate a complete redesign of the substrate. In the same way, placing the inductor on-chip would lead to an unmanageable silicon area overhead.

3.4.2 Evaluation

The simulation setup incorporates the previously developed circuit model of both the VCSEL and the power distribution network. Additionally, a $2nF$ capacitance is connected between pins V_{DD} and V_{SS} so as to mimic an on-chip decoupling capacitor. The MOSFETs are provided by the $40nm$ CMOS technology library. Their widths have been chosen arbitrarily, but still realistic in regards to former VCSEL driver developments by STMicroelectronics.

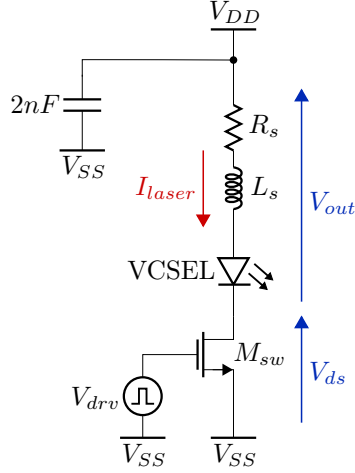


Figure 3.17 – Simulation circuit of the voltage-mode topology.

3.4.2.1 Voltage-mode topology

The simulation bench for the voltage-mode topology is presented in Figure 3.17. The MOSFET M_{sw} is driven on-off by a pulsed voltage source V_{drv} . It is realized by a thick-oxide 3.3V MOSFET, $W \times L = 1.2mm \times 0.55\mu m$.

The simulated electrical waveforms are shown in Figure 3.18. In order to clearly understand those waveforms, one must look into the equivalent network of the voltage-mode circuit during transition of M_{sw} .

In ON state (see Figure 3.19a), M_{sw} operates in the deep triode region, *i.e.* $V_{ds} \ll V_{gs} - V_{th}$, with V_{th} being the threshold voltage. Thus, it can be represented by the channel resistance $R_{on} = 1.8\Omega$ together with the drain-source junction capacitance $C_{ds} = 400fF$. Thereafter, each consecutive transient steps numbered ①, ② and ③ are described:

① The gate of M_{sw} is charged to V_{DD} , thus decreasing the channel resistance. As a consequence, capacitance C_{ds} rapidly discharges through R_{on} . At this point, M_{sw} is fully on.

② The charging of the VCSEL's capacitances, C_m and C_p , produces a current inrush. Once C_m is charged up to the lasing turn-on voltage ($V_{on} \approx 1.5V$), the current begins to flow through the junction diode D which models the VCSEL's active region.

③ Given that C_{ds} , C_m and C_p act as an open circuit, the voltage-mode structure behaves in the same manner as a first-order series RL network. Hence, the driving current builds up according to a $\frac{L_s}{R_{tot}}$ time constant, where $R_{tot} = R_s + R_m + R_{on} \sim 10.35\Omega$ is the overall ohmic resistance in the current path through the VCSEL [89]. Here, the simulated rise time is in the order of 280ps. At steady-state, the parasitic inductance is charged and acts as a short circuit. Thus, the peak current can be expressed as,

$$I_{peak} \approx \frac{V_{DD} - V_{on}}{R_{tot}} = \frac{2.5 - 1.5}{10.35} = 96mA \quad (3.9)$$

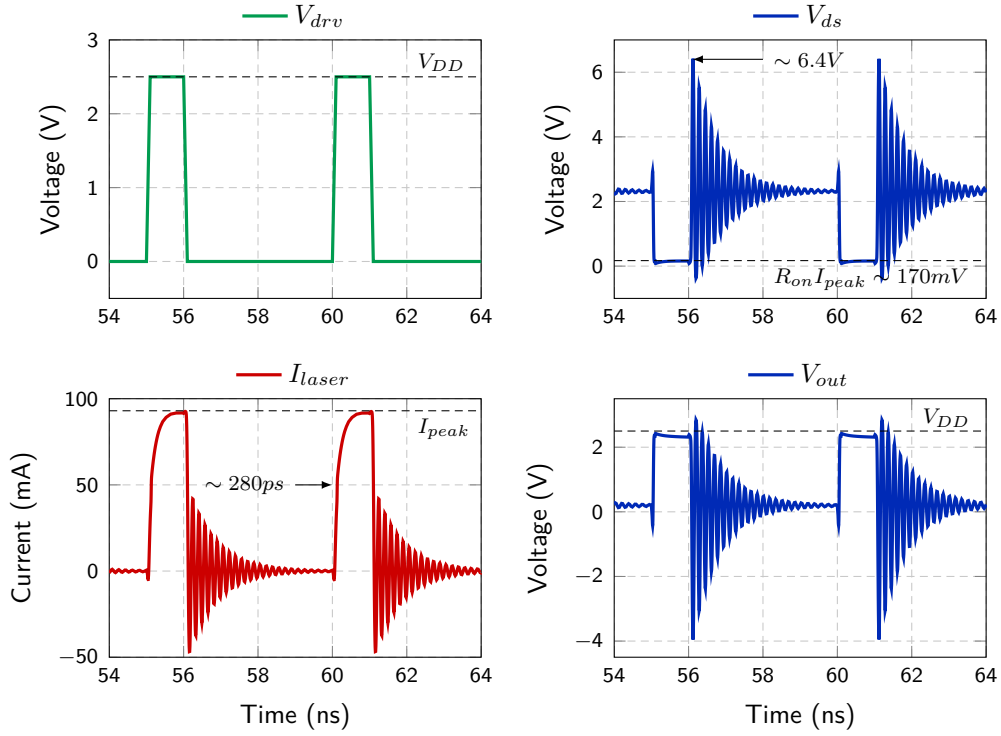


Figure 3.18 – Simulated waveforms of the voltage-mode topology.

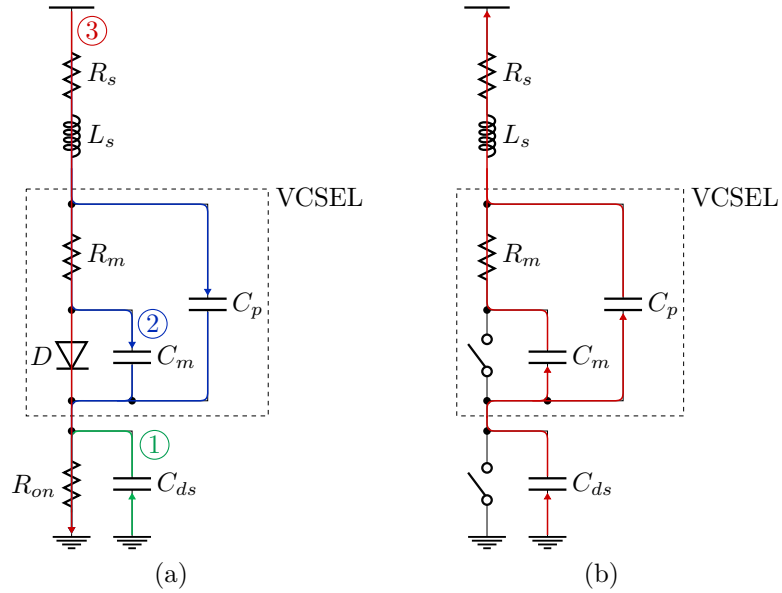


Figure 3.19 – Transient electrical equivalent circuit: (a) NMOS turn-on, (b) NMOS turn-off.

The drain-source voltage of M_{sw} is tied to $R_{on}I_{peak} \sim 170mV$. From a silicon design standpoint, a large NMOS with low channel resistance is to be used in order to maximize the driver's current capability.

In OFF state (see Figure 3.19b), M_{sw} and D are both off. As a result, the equivalent circuit is a series RLC network, which is being excited by the energy initially stored in the capacitance and inductance. Neglecting the VCSEL's pad capacitance, the overall resistance R_{res} and capacitance C_{res} involved in the resonance are calculated from,

$$\begin{aligned} R_{res} &\approx R_s + R_m = 8.55\Omega \\ C_{res} &\approx \frac{C_m C_{ds}}{C_m + C_{ds}} = 289fF \end{aligned} \quad (3.10)$$

The RLC network exhibits an underdamped response ($\xi = \frac{R_{res}}{2} \sqrt{\frac{C_{res}}{L_s}} < 1$), *i.e.* oscillatory and exponentially damped [90]. Simply put, the stored energy flows back and forth between L_s and C_{res} until it is completely dissipated through R_{res} . Due to the RLC resonance, voltage V_{ds} exhibits a significant voltage overshooting up to 6.4V. As a result of the large negative voltage applied across the load, the driving current rapidly decreases with a fall time below 100ps. Then, both V_{ds} and I_{laser} ring at the RLC resonant frequency f_{res} expressed as,

$$f_{res} \approx \frac{1}{2\pi\sqrt{L_s C_{res}}} \approx 6.6GHz \quad (3.11)$$

After the initial excitation, the ringing decays exponentially according to the damping factor $\frac{R_{res}}{2L_s}$.

Such a ringing is detrimental for the circuit's reliability. As a matter of fact, the ringing exceeds the safe operating area of NMOS M_{sw} . Thus, it would be necessary to add a dedicated protection circuitry. In addition, as the ringing current is greater than the VCSEL's threshold current, there is nothing to prevent the laser from turning back on.

3.4.2.2 Series current-mode topology

The test bench for the current-mode series topology is presented in Figure 3.20. The NMOS M_{sw} is a thin-oxide 1.1V MOSFET, $W \times L = 800\mu m \times 0.1\mu m$. The cascode MOSFET M_{casc} is sized to operate in the saturation region, $W \times L = 200\mu m \times 0.55\mu m$. The constant voltage source V_{bias} is set to 1.6V which is the maximum voltage for ensuring safe operation of M_{sw} , *i.e.* 1.1V for the drain-source voltage.

The simulated electrical waveforms and equivalent circuit are respectively shown in Figure 3.21 and Figure 3.22.

In ON state (see Figure 3.22a), the current-mode circuit behaves as a second-order parallel RLC network. As the gate of M_{sw} is charging to V_{DD} ,

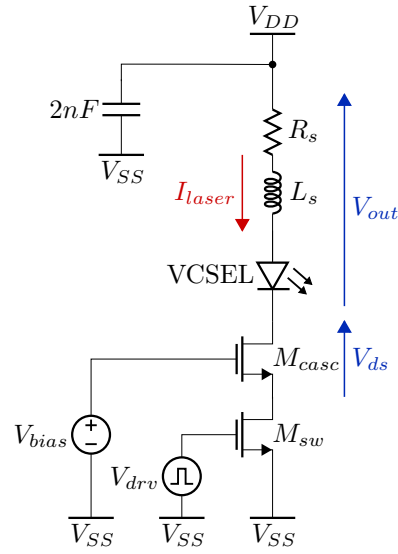


Figure 3.20 – Simulation circuit of the current-mode series topology.

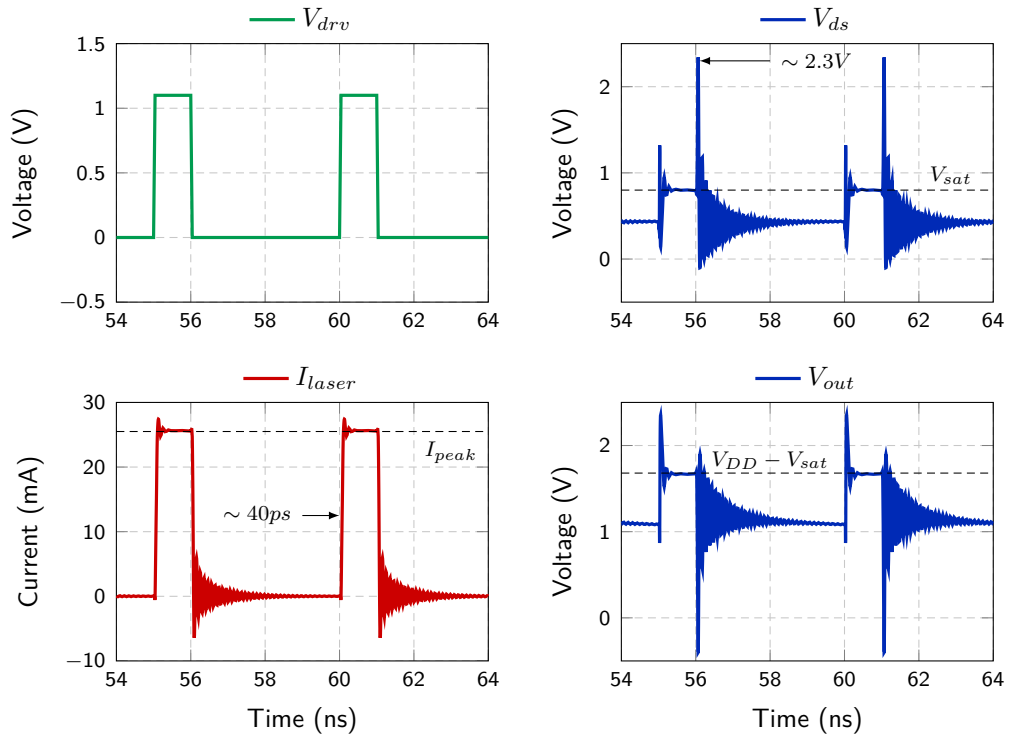


Figure 3.21 – Simulated waveforms of the series current-mode topology.

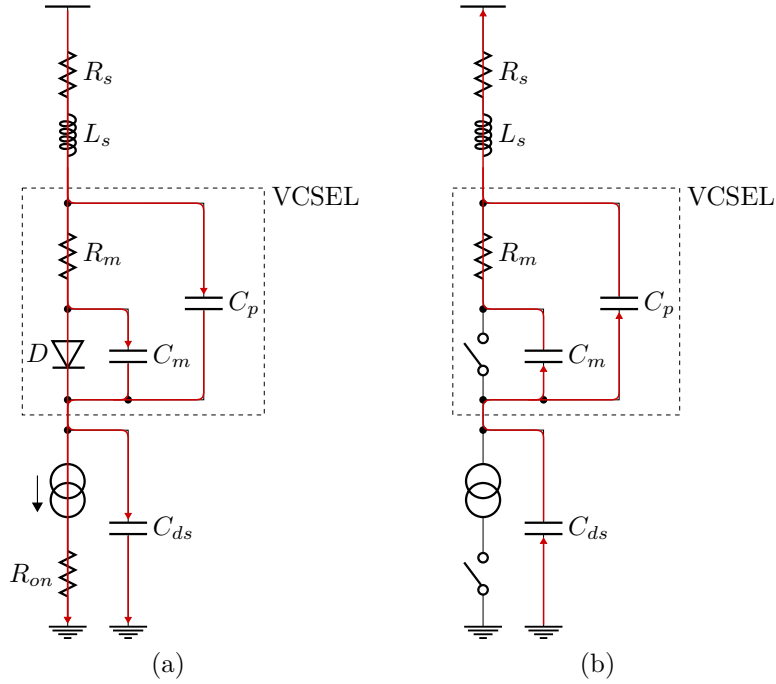


Figure 3.22 – Transient electrical equivalent circuit: (a) NMOS turn-on, (b) NMOS turn-off.

M_{casc} briefly functions in the triode region. As a consequence, the damping factor of the RLC response is set in the underdamped regime. This leads to a rapid increase of the driving current with a simulated rise time of approximately $40ps$. Eventually, M_{casc} starts to operate as a current source, thus providing a constant driving current determined by the saturation voltage V_{sat} . Here, the maximum current to satisfy the saturation condition is $25mA$.

In OFF state, the equivalent circuit is a series RLC network with an oscillatory response.

The operating regime of M_{casc} is of great importance. On one hand, the saturation regime ensures a fast rising edge of the current pulse. On the other hand, the saturation voltage headroom limits the current pulse peak (by restricting the VCSEL's forward voltage), in particular at low-voltage operation. At a fixed supply voltage, increasing current via an increase in channel width will eventually push M_{casc} towards the triode region. As outlined in Figure 3.23, the current-mode topology would behave as a voltage-mode structure.

3.4.3 Wrap-up

A figure of merit is proposed to quantify the overall performance of each topology. The figure gather together the key performance metrics, *i.e.* speed, current capability and power efficiency. It is expressed as,

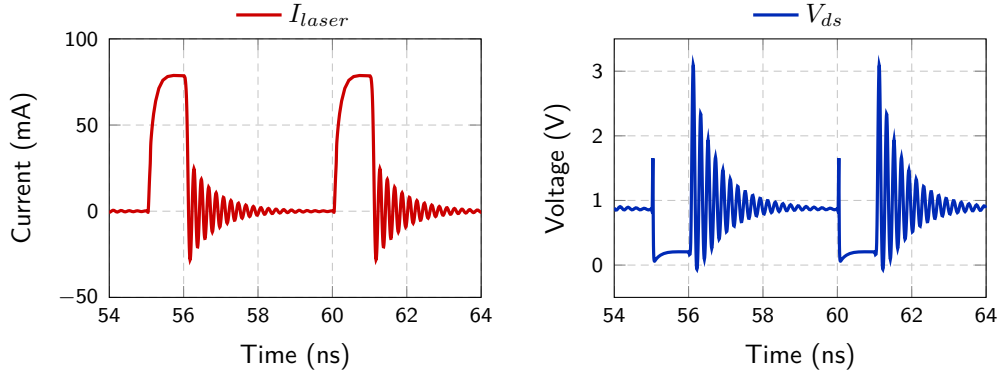


Figure 3.23 – Simulated waveforms of the current-mode topology with cascode operating in the triode region.

$$\alpha_{FOM} = \frac{\Delta I_{laser}}{\Delta t} \times I_{peak} \times \eta_{elec} [mA^2.ps^{-1}] \quad (3.12)$$

The term $\frac{\Delta I_{laser}}{\Delta t} [mA.ps^{-1}]$ is the slope of the driving current pulse's rising edge, $I_{peak} [mA]$ is the peak current and η_{elec} is the power efficiency.

Table 3.4 summarizes the performance metrics of the voltage-mode and series current-mode architectures extracted from circuit simulation.

Performance	$\frac{\Delta I_{laser}}{\Delta t} (mA.ps^{-1})$	$I_{peak} (mA)$	$\eta_{elec} (\%)$	$\alpha_{FOM} (mA^2.ps^{-1})$
Voltage-mode	0.250	92.8	74.1	17.1
Current-mode	0.420	25.7	61.5	7.1

Table 3.4 – Performance comparison between voltage-mode and current-mode laser diode driver topologies at low-voltage operation.

Although, the voltage-mode structure presents a better overall performance, choosing the adequate driver architecture is a matter of compromises. As a matter of fact, the current-mode circuit may enable for a faster rising transient, but at the expense of voltage headroom. Therefore, in a voltage-constrained design, it is difficult to combine both superior current capability and transient speed. With the VCSEL array in use, in order to satisfy the steady-state saturation condition for a peak current of $200mA$ ($V_{laser} = 3.2V$), the driver's supply voltage must equal at least,

$$V_{DD} \approx V_{sat} + V_{laser} = 4V \quad (3.13)$$

In contrast, the voltage-mode driver is inherently superior in terms of current capability and power efficiency. However, the transient speed is mainly

defined by the parasitic inductance through the laser diode current path. Based on an overall resistance of 10Ω in the driving path, the required supply voltage to reach a peak current of $200mA$ can be estimated from,

$$V_{DD} \approx I_{peak}R_{tot} + V_{on} = 3.57V \quad (3.14)$$

There is clear evidence that, regardless of circuit architecture, the low-voltage design target ($2.5V$) is not feasible without an intermediate circuitry allowing for a voltage step-up. So as to comply with the fully integrated requirement, voltage step-up would be realized by a switched-capacitor DC-DC converter. The main drawback to this solution is that capacitive converters are limited in terms of efficiency and lead to large silicon area overhead (based on previous laser diode driver implementation in STMicroelectronics). Thus, it was chosen to head towards a different implementation to overcome the low-voltage constraint.

3.5 Proposed architecture

This section presents in detail the key features of the proposed laser diode driver architecture. A circuit structure based on capacitive charge transfer between a flying capacitor C_{fly} and the laser diode was chosen. The switch assembly $S_0 - S_4$ is presented in Figure 3.24a. It is important to note that the purpose of the flying capacitor is not to fully discharge through the laser as it is for a capacitive discharge resonant driver. This way, the proposed architecture can be viewed as a modified voltage-mode topology based on capacitive discharge.

The specific features of the architecture are:

- A capacitive voltage boost for increasing the driving capability while guaranteeing low-voltage operation.
- A carrier sweep-out scheme to address typical laser diode slow turn-off transient, thus enhancing short-pulse operation.

The corresponding timing sequence is shown in Figure 3.25.

3.5.1 Capacitive voltage boost

The capacitive voltage boost principle is replicated from a STMicroelectronics patent [91]. In the simplest term, it reproduces the voltage step-up principle exploited in capacitive converter. The key difference is that the aim is not to get a regulated output voltage level.

The operation is as follows. In phase ϕ_0 , C_{fly} is charged to V_{DD} through S_1 and S_2 . In phase ϕ_1 , switches S_0 and S_4 are turned on to create a discharging path for the capacitor. Specifically, S_0 pushes the bottom plate of C_{fly} to V_{DD} .

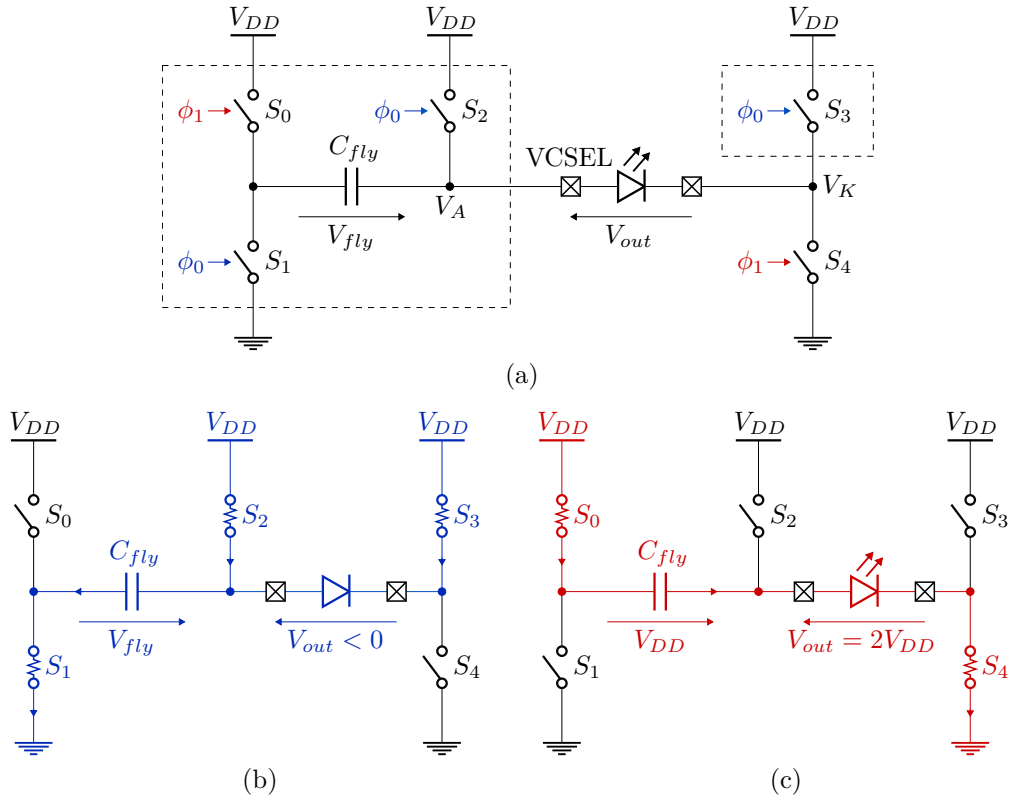


Figure 3.24 – Proposed modified voltage-mode laser diode driver based on capacitive discharge: (a) switch assembly, (b) charging phase ϕ_0 , (c) discharging phase ϕ_1 .

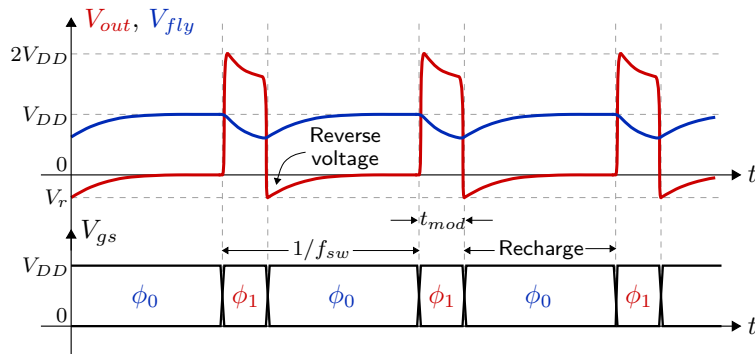


Figure 3.25 – Timing sequence of the proposed laser diode driver architecture.

As a result, node V_A can rise up to $2V_{DD}$ due to the voltage continuity across C_{fly} . Simultaneously, node V_K is pushed to ground by S_4 . As a consequence, a $2V_{DD}$ voltage pulse is applied across the load. Given that the driving current builds up according to the load voltage, such a voltage boost principle permits to increase the circuit's driving capability. The voltage pulse width is set by the driving signals of S_0 and S_4 .

The flying capacitor is the key component of the circuit structure as it determines the energy of the driving current pulse. Obviously, considering that the capacitor stores a finite charge, the current pulse width is inherently limited. Hence, such a circuit architecture is intended for short pulse operation (from sub- ns to ns pulse width). Furthermore, so as to allow for a fully integrated solution and prevent from adding more parasitic inductance in the current path, the capacitor must be implemented on-chip.

3.5.2 Carrier sweep-out

With latter VCSEL driver characterization in STMicroelectronics, optical tailing in the laser pulse's turn-off transient has already been observed. Such a phenomenon translates into a substantial increase in the apparent fall time of the laser pulse and is accordingly an unwanted scenario in direct time-of-flight rangefinding. Therefore, one of the objectives of the thesis was to investigate on this matter, and eventually propose a way for addressing it.

Below the lasing threshold current, the turn-off response of VCSELs can be limited by carrier diffusion and spatial hole burning phenomena [70, 92].

The sub-threshold dynamics of VCSELs is governed by the spontaneous carrier lifetime, which is in the order of the nanosecond [80]. This slow recombination process is likely to prevent the laser from rapidly turning off, in the form of a slow tail in the laser pulse [70].

In the same vein, spatial hole burning can result in secondary pulsations up to several hundreds of picoseconds after the laser pulse's falling edge [70, 92]. In oxide-confined VCSELs, the transverse or spatial optical mode is constrained in the center of the device. Due to the strong central stimulated recombination process, carriers in the center are depleted much faster as compared to those at the edges [80, 92]. As a consequence, a spatial hole is burned in the carrier density. When the driving current is modulated from an above-threshold value to a sub-threshold value, the hole is filled due to the spatial redistribution of carriers. At this point, the VCSEL can momentarily get back into lasing operation and therefore emit secondary light pulses [70, 92].

Such phenomena are primarily related to charge carrier storage. They may thereby be mitigated through any circuit function enabling fast carrier sweep-out. From a VCSEL modelling point of view, carrier accumulation is modelled

by capacitance C_m . Hence, the proposed driver topology incorporates a sweep-out switch, namely S_3 , which aims at rapidly discharging C_m . Such a scheme was already successfully demonstrated in a CMOS LED driver dedicated to data transmission [93].

The purpose of S_3 is to push the cathode node V_K to V_{DD} at the laser diode switch-off. Owing to the partial discharge of C_{fly} , a slight negative bias is applied across the load. The amplitude of the reverse voltage V_r can be expressed as,

$$V_{fly} = V_{DD} - \frac{Q_{laser}}{C_{fly}} \rightarrow V_r = -\frac{Q_{laser}}{C_{fly}} \quad (3.15)$$

where Q_{laser} is the amount of charge pulsed in the laser diode. Referring to Figure 3.25, the load voltage is kept in the negative range during the off time of the VCSEL. Once C_{fly} is fully charged, the load voltage is zero.

The carrier sweep-out principle was validated via simulation of the electro-optical VCSEL model. In Figure 3.26a, the VCSEL is driven by a pulsed current source from $0mA$ to $100mA$. One can see that the voltage V_{laser} exhibits a slow turn-off transient and remains non zero during the off time. This is due to the fact that the sub-threshold recombination rate of charge carriers is in the order of the nanosecond. In Figure 3.26b, the VCSEL is driven by a voltage source from $-50mV$ to $2.5V$. The sweep-out of the carrier superimposes an undershoot of a few tens of milliamps on the driving current pulse's falling edge.

The resulting laser pulse shapes are compared in Figure 3.27 with both linear and logarithmic scales. There is clear evidence that without carrier sweep-out, the laser takes a relatively long time to switch off. In contrast, turning off the VCSEL via a reverse voltage allows to remove the optical tail. The apparent fall time is decrease from $74ps$ to $40ps$, *i.e.* an improvement of 46% in transient speed. In addition, the laser pulse width is slightly shortened ($\sim 20ps$) due to the charging time of the VCSEL's capacitances C_p and C_m . Still, the rising transient speed remains unchanged as it is set by the gain-switching pulse.

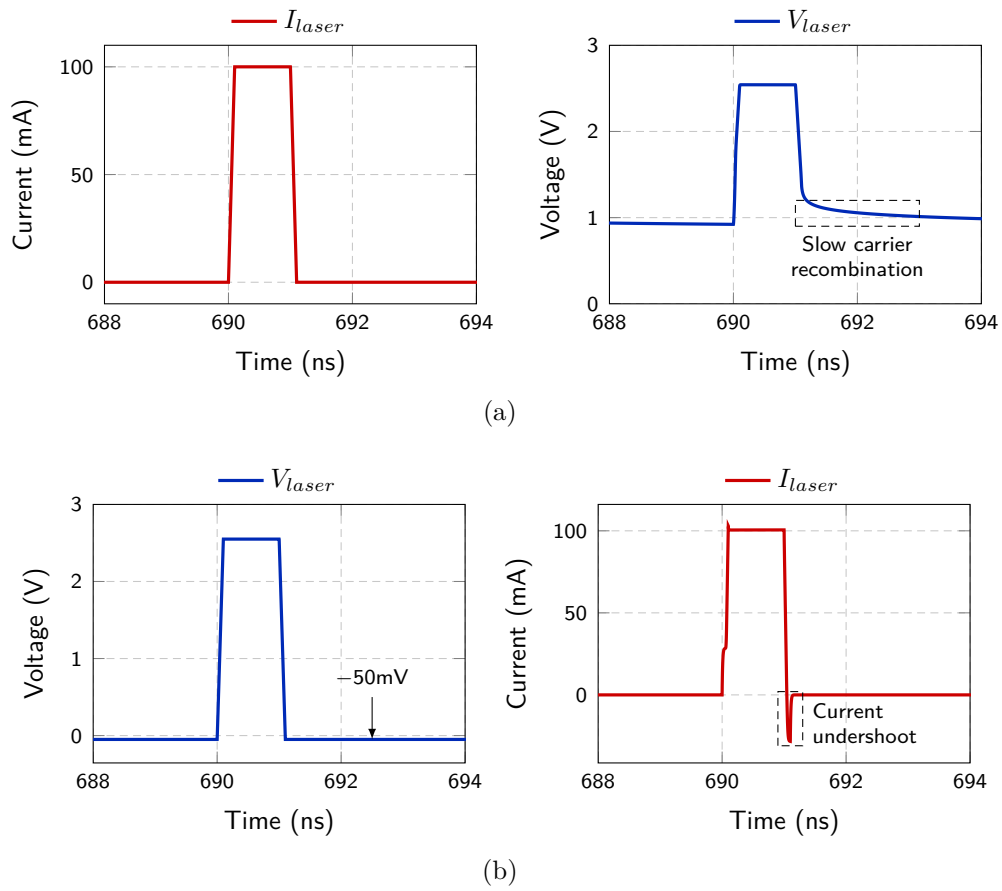


Figure 3.26 – Simulated electrical waveforms of the VCSEL: (a) driven by current (b) driven by voltage.

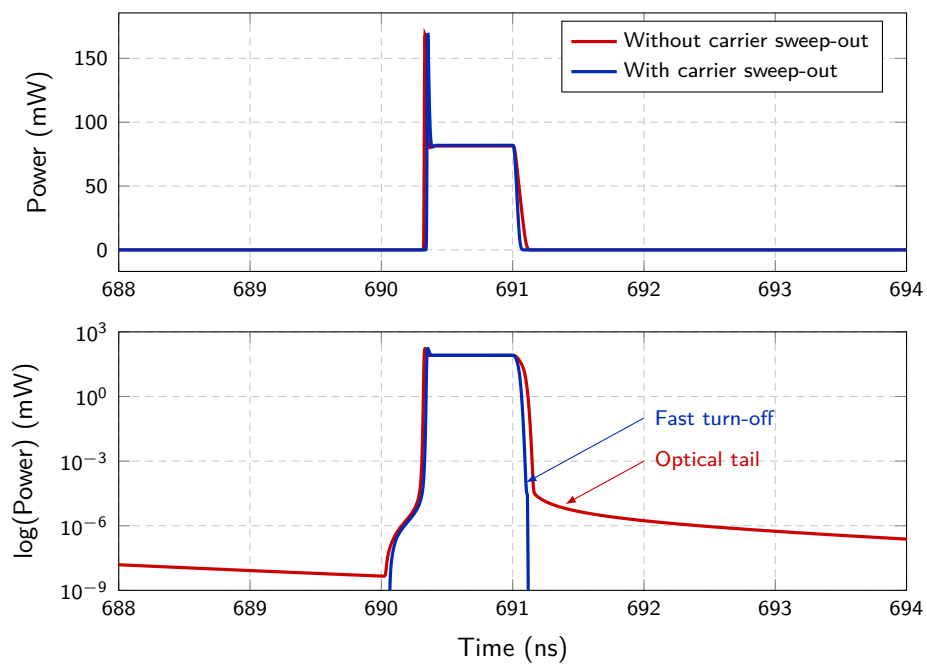


Figure 3.27 – Simulated optical waveforms of the VCSEL with and without carrier sweep-out.

4 Laser diode driver IC design

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This chapter details the design flow of the laser diode driver topology proposed in the preceding chapter. The circuit is fabricated using the CMOS 40nm technology by STMicroelectronics. As a first step, a comprehensive view of the system is provided. Afterwards, the transistor-level dimensioning of each sub-block is presented. What is more, considerations regarding physical component layout are also pointed out throughout the chapter. Finally, a post-layout verification is carried out to assess the performances of the circuit prior to measurement.

4.1 System-level view

The VCSEL driver has been implemented in the STVC vehicle circuit. An overall view of the system with the main building blocks is represented in Figure 4.1. As already mentioned, the pulse generator is re-used so as to provide

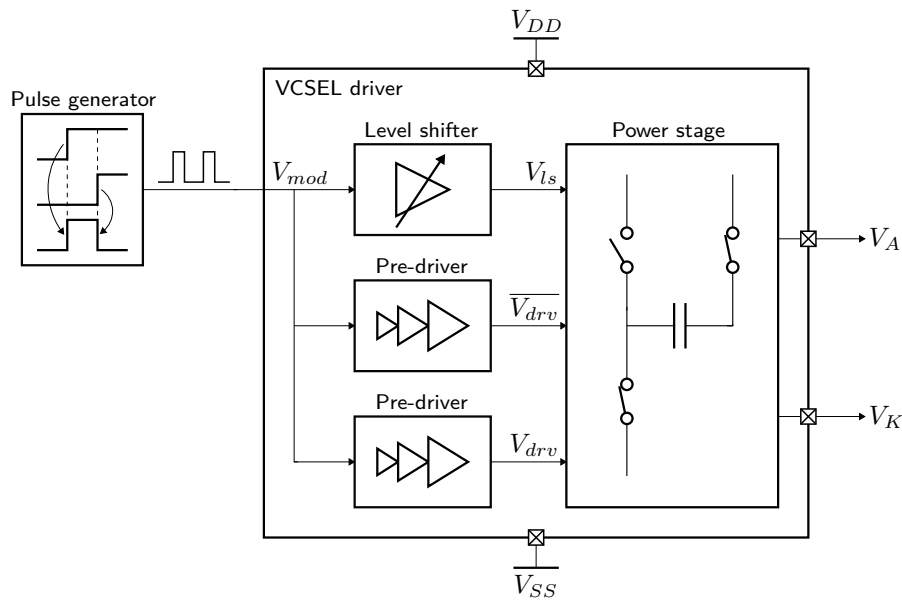


Figure 4.1 – System-level view with building blocks.

the modulation signal V_{mod} of the laser diode. The frequency and pulse width of V_{mod} are respectively denoted as f_{sw} and t_{mod} .

The circuit's main building blocks which are designed throughout this chapter are:

- The power stage.
- A level-shifter.
- The pre-drivers.

The transistor-level architecture of the power stage is shown in Figure 4.2a. We have implemented the switch assembly (described in the preceding chapter) from actual PMOS and NMOS devices from the 40nm technology portfolio. Note that the flying capacitor's bottom plate switching node has been exploited to drive the gate of NMOS M_4 . In this way, it was not necessary to add a third pre-driver circuit to drive M_4 , thus saving silicon area. In addition, switch M_2 has been realized in a back-to-back configuration. Basically, such a structure involves a pair of MOSFETs sharing a floating bulk potential [94]. The motivation for choosing this specific implementation is discussed later in Part 4.2.2.1.

The proposed timing sequence of driving signals is illustrated in Figure 4.2b. The level-shifter generates signal V_{ls} [$V_{DD} - 3.6V$] which ensures full turn-on of NMOS M_2 . The 3.6V voltage level being the safe voltage rating of 3.3V MOSFETs in the 40nm technology node. The pre-drivers increase the driving strength of signal V_{mod} before feeding it to the power stage, thus resulting in signals V_{drv} and $\overline{V_{drv}}$ [$0 - V_{DD}$]. Each sub-block is supplied from

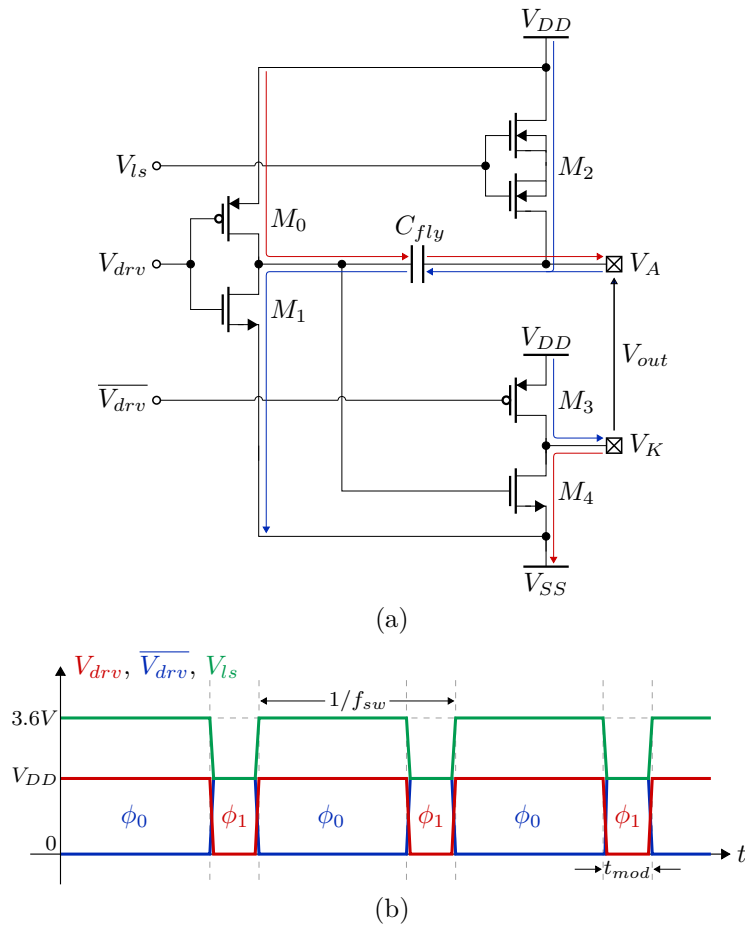


Figure 4.2 – Power stage implementation: (a) transistor-level architecture, (b) timing sequence.

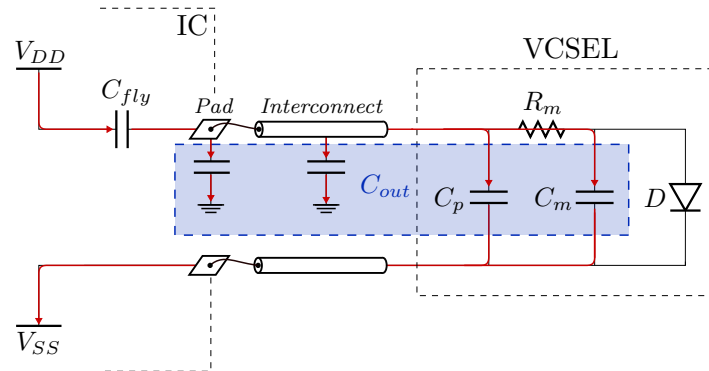


Figure 4.3 – Charge redistribution between the flying capacitor and the output capacitance.

the dedicated power supply and ground pins of the driver, *i.e.* V_{DD} and V_{SS} .

4.2 Cell design details

This section presents the sizing of the driver's components, starting with the flying capacitor. Given that the goal of the project was to develop a test chip (proof of concept), the variation of the process (corners) was not considered as an important matter. Additionally, the design was completed for a temperature of 55°C as it is an estimate of the operating temperature of the system within a consumer portable device.

4.2.1 On-chip flying capacitor

The role of the integrated flying capacitor C_{fly} is to partially discharge so that a current pulse is generated through the VCSEL. Its dimensioning was carried out using a dedicated simulation circuit.

4.2.1.1 Dimensioning

The primary approach to size the flying capacitor relies on the charge transfer principle. When MOSFETs M_0 and M_4 are turned on, there is a charge redistribution between C_{fly} and the driver's load capacitance C_{out} . The latter is mainly contributed by the VCSEL (pad and mesa capacitances, C_p and C_m), the anode bonding pad and the interconnect. C_{out} was estimated at approximately 3pF based on post-layout extraction of the bonding pad's parasitic capacitance.

As illustrated in Figure 4.3, C_{fly} and C_{out} form a capacitive voltage divider. The resulting voltage loss V_{drop} across the flying capacitor can be expressed as,

$$V_{drop} = V_{DD} \left(1 - \frac{C_{fly}}{C_{fly} + C_{out}} \right) \quad (4.1)$$

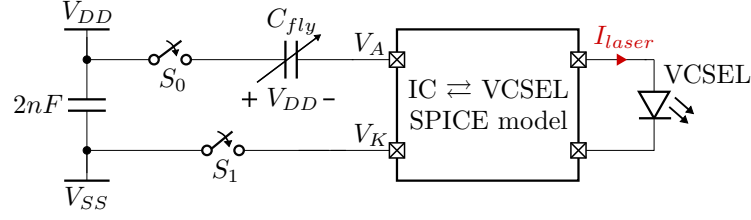
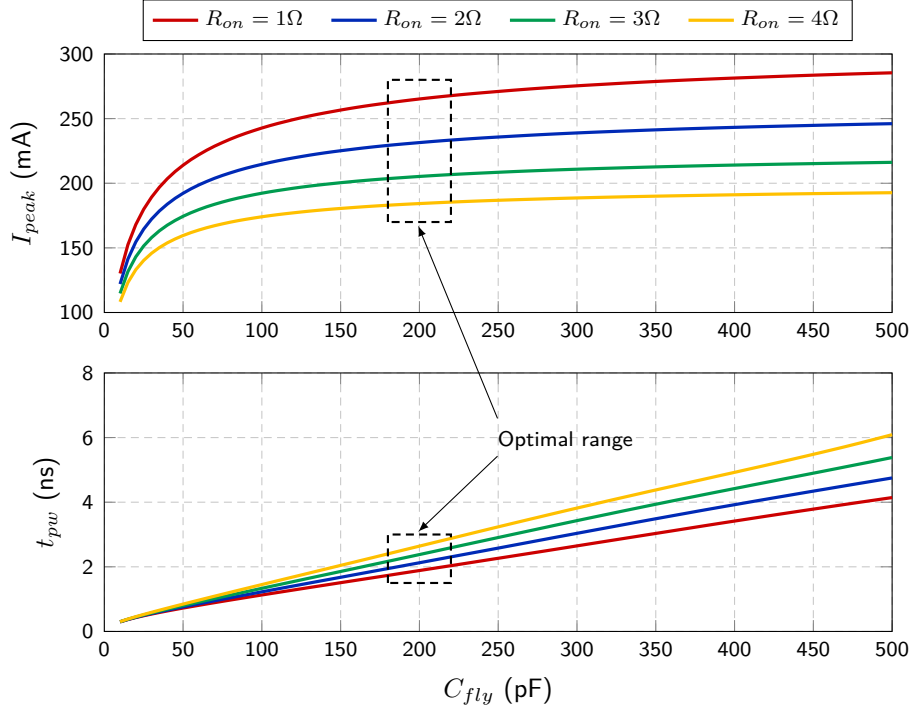


Figure 4.4 – Simulation circuit for the dimensioning of the flying capacitor.

Figure 4.5 – Laser driving current pulse peak and duration extracted from simulation ($V_{DD} = 2.5V$).

So as to limit the capacitive voltage drop, C_{fly} must be significantly larger than the load capacitance. From expression (4.1), one can calculate the minimum required capacitance for a given supply voltage. Here, C_{fly} should be at least $150pF$ to reduce the drop down to 2% of V_{DD} .

The simulation circuit for determining the value of C_{fly} is represented in Figure 4.4. It simply replicates the current path through the VCSEL. The initial voltage across the flying capacitor is set to V_{DD} to take into account the preceding charging phase. MOSFETs M_0 and M_4 are simulated using ideal devices, S_0 and S_1 . Their on-state resistance R_{on} was set within the range $[1\Omega, 2\Omega, 3\Omega, 4\Omega]$, which is realistic given the technology and the available area. Last, an arbitrary but sufficiently large value of on-chip decoupling capacitance ($\sim 2nF$) is incorporated.

The circuit is simulated for a fixed $2.5V$ supply voltage. The width t_{pw} and peak I_{peak} of the driving current pulse are extracted for a flying capacitance

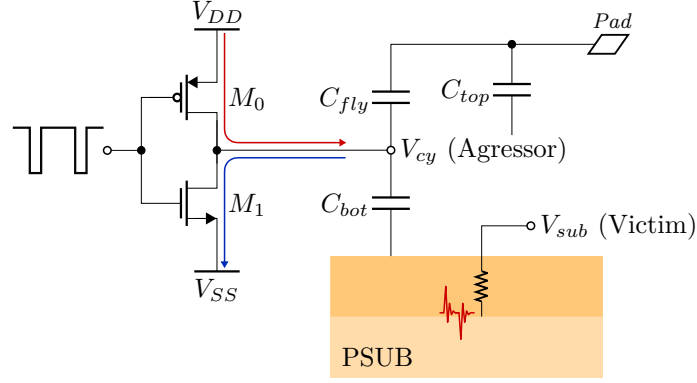


Figure 4.6 – Substrate noise injection due to bottom plate parasitic capacitive coupling.

sweep between $10pF$ and $500pF$.

Simulation results presented in Figure 4.5 show that the peak current's derivative tends rapidly towards zero as the capacitance increases. From a value of $200pF$, a $10mA$ increment in peak current requires at least a 50% increase in C_{fly} , regardless of the MOSFETs' channel resistance. Given that a limited silicon surface is allocated to the driver, the significant area cost of on-chip capacitor structures must be taken into account. Hence, the capacitor's value was chosen around $200pF$, as a compromise between the driving current peak and area. In addition, it permits a current pulse duration up to $2ns$, which is suitable in regards to the targeted sub- ns pulse width range.

4.2.1.2 Comparison of integrated capacitor structures

This part focuses on choosing the most adequate capacitor structure for realizing C_{fly} . To this end, a feature comparison of capacitors available in the CMOS $40nm$ technology portfolio is carried out.

Primarily, density appears as a key criteria since a capacitance of approximately $200pF$ must be integrated within a limited area. In addition, the inherent top and bottom plates parasitic capacitances, C_{top} and C_{bot} , must be examined. As a matter of fact, parasitic capacitances have a detrimental impact on the functioning of the proposed driver topology. First, C_{top} adds up to the circuit's load capacitance. As a result, the voltage divider loss is expected to increase with increasing C_{top} . Then, knowing that the circuit incorporates a capacitive voltage boost structure, the bottom plate parasitic capacitance is periodically charged and discharged. It can therefore cause a substantial drop in the circuit's power efficiency due to switching losses [95, 96]. The power losses P_{bot} due to the bottom plate capacitance can be expressed as,

$$P_{bot} = C_{bot} V_{DD}^2 f_{sw} \quad (4.2)$$

The parasitic capacitance could as well create unwanted coupling between

critical nodes. Specifically, since the substrate is a resistive material, substrate current injection via capacitive coupling can lead to local variations of the substrate potential V_{sub} (see Figure 4.6). Such voltage fluctuations may severely disturb sensitive neighboring circuits and induce latch-up issues [97]. Last, voltage coefficient, *i.e.* capacitance variation versus applied voltage, is an important feature as C_{fly} operates in repeating cycles of charge and partial discharge.

4.2.1.2.1 MOS capacitor: The intrinsic capacitor type available in CMOS technologies is the metal-oxide-semiconductor (MOS) capacitor. In the STMicroelectronics' 40nm node, two distinct MOS devices can be distinguished: poly/ p -well and poly/ n -well. MOS capacitors show a high density in accumulation operation. Yet, they are highly non-linear with applied voltage as shown in Figure 4.8.

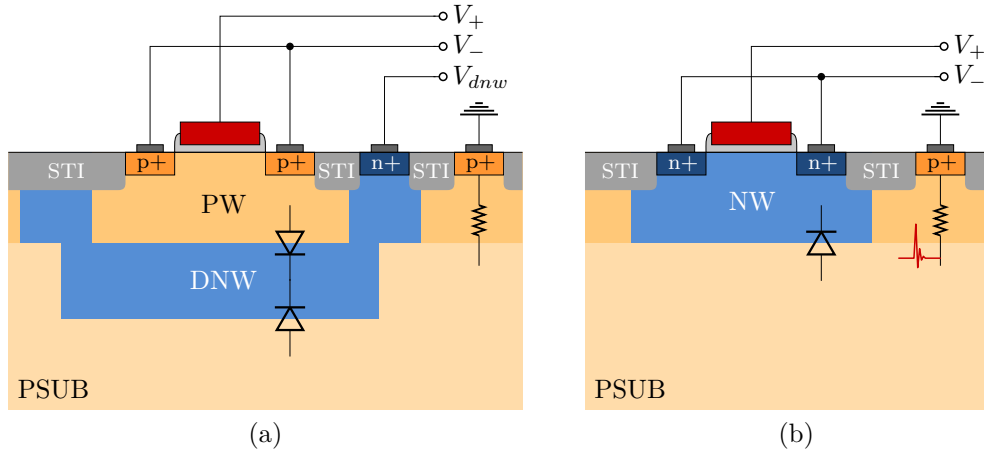


Figure 4.7 – Cross section of MOS capacitors: (a) poly/ p -well device, (b) poly/ n -well device.

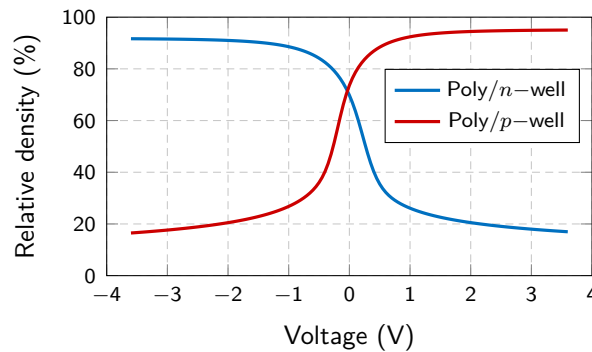


Figure 4.8 – Typical capacitance-voltage characteristics of MOS capacitors in the CMOS 40nm process: (a) poly/ p -well, (b) poly/ n -well.

The poly/ p -well structure illustrated in Figure 4.7a must to be isolated from the substrate (PSUB) by a deep n -well (DNW). One issue associated with this device is that the p -well (PW) must play the role of the capacitor's top electrode for accumulation mode. Accordingly, the DNW should be biased at a voltage of at least $V_{dnw} = 2V_{DD}$ so that the PW/DNW diode remains reverse-biased. This dedicated biasing voltage should be generated via an additional circuitry, which would in turn increase the circuit's complexity and area. Furthermore, the PW/DNW diode brings a high top plate parasitic capacitance, up to 9% of the effective capacitance.

In the poly/ n -well capacitor represented in Figure 4.7b, the gate and the n -well (NW) are the top and bottom plates, respectively. The main drawback of this structure is that it exhibits a significant bottom plate parasitic capacitance, up to 4% of the effective capacitance, due to the PSUB/NW junction.

4.2.1.2.2 MOM capacitor: The straightforward capacitor in a CMOS technology back-end metal stack is the metal-oxide-metal (MOM) capacitor. In the STMicroelectronics' CMOS 40nm technology, MOM capacitors are formed in the thin metal levels (M1-M5X) by multiple parallel fingers and dielectric inter-metal separators. The metal stripes from one metal layer to another are perpendicular as depicted in Figure 4.9. MOM devices can be densely distributed on-chip, thus resulting in low parasitic resistance and inductance. In addition, a major asset of MOM as compared to MOS capacitors is that the capacitance variation against voltage is negligible. However, they exhibit a poor density which depends on the number of metal layers employed as well as their thickness and spacing.

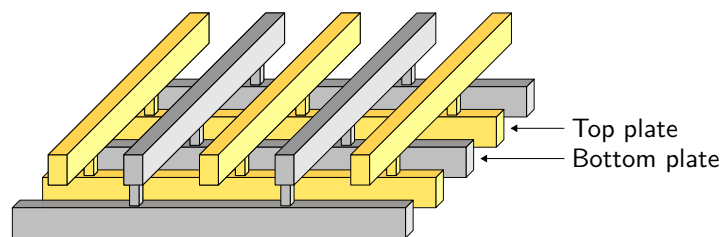


Figure 4.9 – MOM capacitor.

4.2.1.2.3 MIM capacitor: Another alternative to have integrated capacitors is the metal-insulator-metal (MIM) capacitor. It is a parallel plate capacitor with a thin dielectric spacing. In the 40nm node by STMicroelectronics, it is nested between the last non-thick metal layer (M5X) and the first thick metal layer (M6Z). The layout of a MIM structure is presented in Figure 4.10. MIM capacitors show a typical density which is significantly higher than MOM.

Additionally, the density value is independent of the applied voltage. The major pro of the MIM structure is that it can potentially allow for a low bottom plate parasitic capacitance provided that the space below the bottom electrode is kept empty. In such a case, the parasitic capacitance was estimated at 0.5% of the effective capacitance based on post-layout extraction. In contrast, any M5X metallization placed below the MIM capacitor's bottom plate can lead to a significant parasitic capacitance increase.

It must be kept in mind that MIM devices are not available by default in CMOS technologies. Their fabrication also requires additional masks and process steps, thus leading to an increase in the overall manufacturing cost [60].

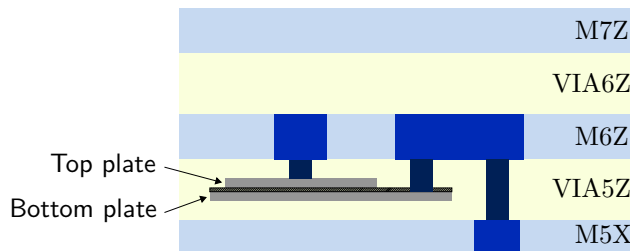


Figure 4.10 – MIM capacitor.

4.2.1.2.4 Wrap-up: In conclusion, MOS devices were considered as inadequate for implementing a flying capacitor. Since one electrode is the silicon, there is a large parasitic capacitance. Then, the MOM capacitor was excluded on the grounds of its limited density. As a result, the MIM device appeared as the best possible trade-off between capacitive density and parasitics despite its higher process sensitivity and cost.

4.2.1.3 Physical layout

We have designed a MIM flying capacitor whose physical layout is presented in Figure 4.11. It is divided into 36 parallel unitary cells arranged in a square shape. The typical capacitance obtained is $178pF$, which is close to the targeted $200pF$.

The top and bottom plates are both only connected to the rest of the circuit via the upper MZ6 metal layer (see Figure 4.10). For this purpose, M6Z metal tracks have been laid out. These are alternatively distributed along the capacitor structure in order to minimize the metal's sheet resistance. Note that the bottom plates of each MIM cell were merged together to reduce area overhead.

As already explained, the layout strategy is to keep the space below the bottom electrode empty in order to minimize parasitic substrate couplings. The resulting bottom plate capacitance to the substrate was extracted from post-layout simulation at approximately $940fF$. Furthermore, the top plate

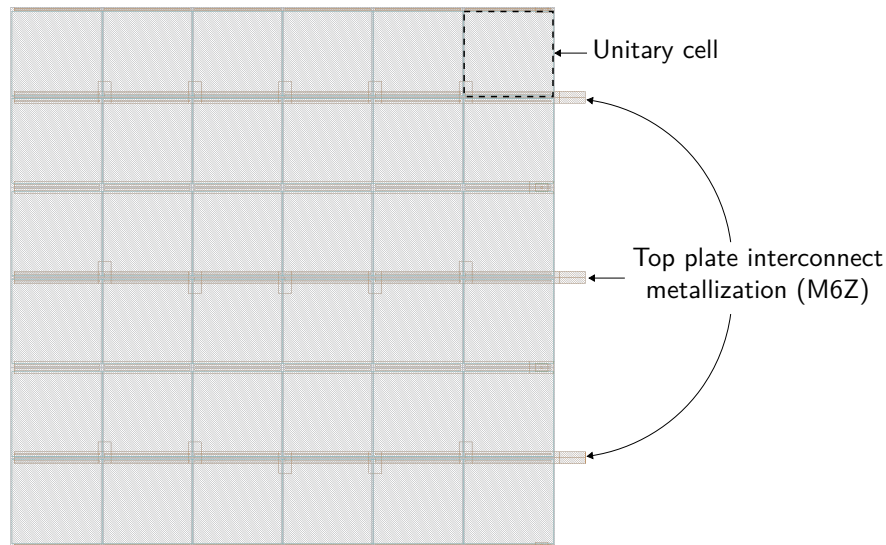


Figure 4.11 – Physical layout of the MIM flying capacitor.

capacitance mostly arises from the M6Z metallization that connects the top electrode. As a first approximation, this parasitic contribution was neglected.

4.2.2 MOSFET dimensioning

Firstly, this section provides the explanation for choosing a back-to-back configuration for MOSFET M_2 . Then, the dimensioning of the power MOSFETs and the pre-driver is carried out.

4.2.2.1 Why a back-to-back transistor?

In this part, physical design considerations for the MOSFET M_2 are reviewed. This switch is connected between V_{DD} and the flying capacitor's top plate. When on, it provides a current path for recharging C_{fly} . This topic was looked at because available MOSFET models in the design kit do not include vertical and lateral parasitic bipolar transistors. These bipolar transistors are inherent in any CMOS process and form the basis of latch-up parasitic structures [60, 98, 99]. Since latch-up is a potential root cause of IC failure, it was examined when implementing M_2 .

Initially, M_2 was realized by a single isolated NMOS device. Referring to Figure 4.12, an isolated NMOS is implanted in a PW isolated from the substrate by a DNW. The latter must be tied to V_{DD} as it is the highest available voltage level. In this way, the PSUB/DNW and PW/DNW junctions are properly reverse biased. Note that the bulk of M_2 (PW) is biased to V_{DD} to respect the drain-bulk voltage rating of the device when V_A is pushed to $2V_{DD}$.

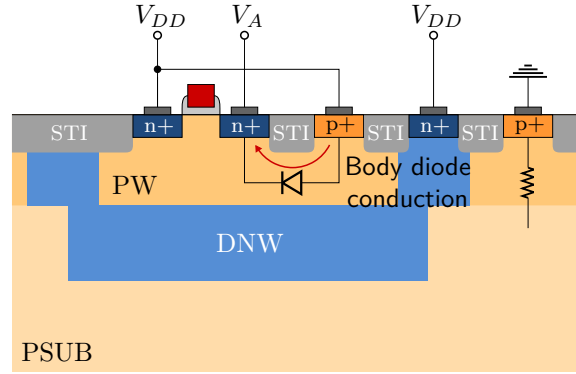


Figure 4.12 – Cross section of transistor M_2 realized by an isolated NMOS device.

However, this primary implementation did not comply with the laser safety circuit re-used from the STVC. The safety system is composed of several current-steering switches. Its function is to attest the integrity of the physical interconnect between the driver chip and the VCSEL die. In addition, it allows for the detection of any short-circuit condition. The problem associated with the isolated NMOS comes from the intrinsic body diode (PW/ $n+$) depicted in Figure 4.12. This diode is forward biased during the laser safety routine. As a result, a leakage current flows from the supply pin, thus leading to a failure of the safety circuit.

In order to ensure the compatibility of the proposed VCSEL driver topology with the STVC's hardware, the issue was first resolved by the addition of a high-side PMOS transistor. The drain potential of the PMOS being the bulk bias of transistor M_2 . As the PMOS is intentionally kept off during the laser safety routine, current injection from the body diode is eliminated. Nonetheless, such a workaround is a source of potential failure risk arising from the parasitic bipolar transistors.

Figure 4.13 shows the equivalent circuit with parasitic bipolar transistors, NPN Q_n (DNW/PW/ $n+$) and PNP Q_p (PW/DNW/PSUB), as well as parasitic substrate and DNW resistances, R_{sub} and R_{dnw} . Since the PMOS is always on when the driver is pulsing, it is simply depicted by a resistance.

Knowing that C_{fly} partially discharges throughout each driving current pulse, the base-emitter diode of Q_n is likely to be periodically forward biased. A current flow through Q_n can induce a voltage drop across R_{dnw} , which in turn may trigger Q_p . As a result, a direct current path could possibly be created between the supply pin V_{DD} and the substrate through the PMOS and Q_p . Pursuing this chain of events further, a current flow through Q_p should lead to a drop in the PMOS drain voltage (PW), thus tending to turn off the base-emitter diode of both Q_n and Q_p . Hence, the parasitic effect outlined herein does not seem to be self-sustaining as common latch-up.

Still, so as to prevent any potential risk (due to the lack of parasitic bipolar

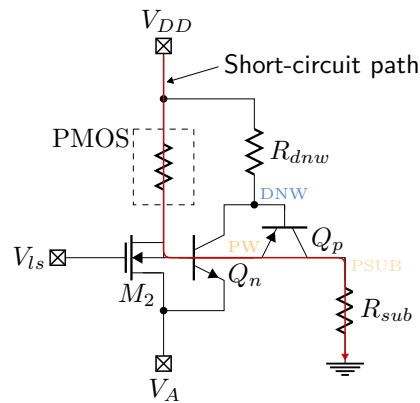


Figure 4.13 – Equivalent circuit with parasitics of transistor M_2 realized by an isolated NMOS device (PMOS always-on).

transistors modelling), a back-to-back configuration was employed [94]. It is realized by two NMOS transistors implanted in a shared well (see Figure 4.14a). These are both driven by the same signal V_{Is} . As a consequence, the bulk node (PW) is floating when the device is off, thus cutting out the continuity of the signal path between the supply and the substrate. In the same way, any base current in Q_n is interrupted. The equivalent parasitic circuit of the back-to-back MOSFET is presented in Figure 4.14b. It is worth noting that such a configuration does not avoid the conduction of the base-emitter diode of Q_n , the latter being caused by the partial discharge of C_{fly} . Yet, although Q_n is triggered, it operates in parallel with M_2 , meaning that its emitter current contributes to the charging of C_{fly} .

It is important to note that specific layout design rules have been used to mitigate latch-up issues. These are discussed later in the manuscript, in [Part 4.3](#).

4.2.2.2 Pre-driver

As mentioned in [Section 4.1](#), pre-drivers are required to drive the gate capacitance of the MOSFETs forming the driver's power stage.

In CMOS circuits, driving large capacitive loads is typically performed by tapered buffers [98, 100, 101]. These are realized by a chain of scaled inverters for which the MOSFET channel width is increased towards the load by a constant factor. In this way, the driving capability can be gradually incremented from the logic blocks to the power stage.

The design of tapered buffers has been extensively studied in the literature. Typical performance aspects are delay, power dissipation, physical area and circuit reliability [100]. Herein, the main design criteria is the propagation of sub-ns pulsed signals, down to 250ps.

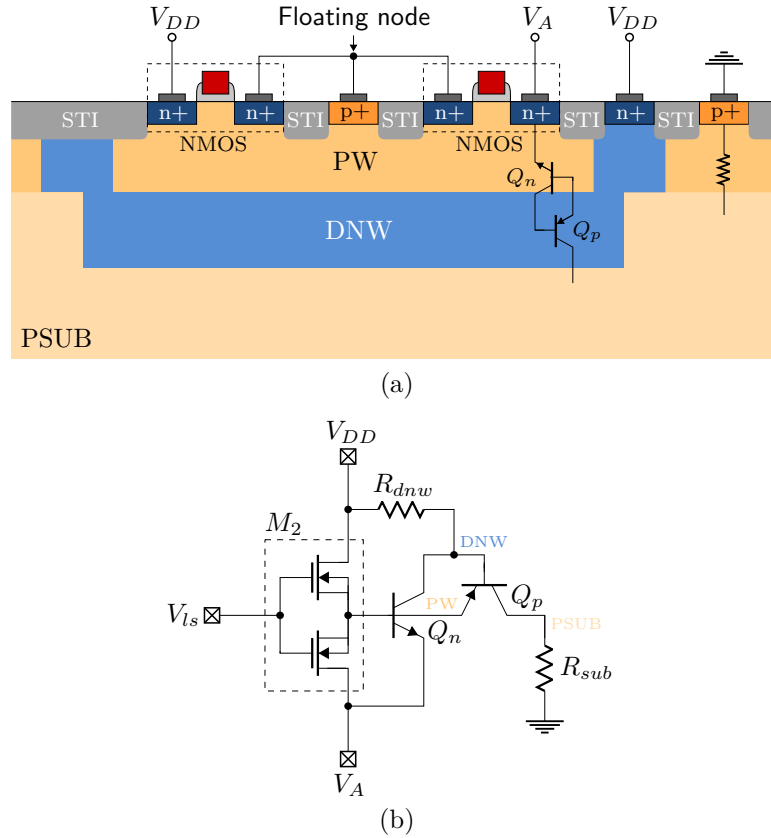


Figure 4.14 – Transistor M_{b2b} realized by an NMOS device in back-to-back setup: (a) cross section, (b) equivalent circuit with parasitics.

Device	Width (μm)	Length (μm)
2.5V NMOS	6.04	0.27
2.5V PMOS	7.88	0.27
3.3V NMOS	6.04	0.55
3.3V PMOS	7.88	0.44

Table 4.1 – Dimensions of MOSFETs for the 2.5V and 3.3V standard inverter cells.

The pre-drivers were realized from 2.5V MOSFETs. These are more suitable for driving sub-ns pulses as compared to 3.3V devices due to their lower gate capacitance. The 2.5V standard cell available in the technology design kit was used as a basis for the design. The MOSFETs' size are pointed out in Table 4.1. The width ratio between PMOS and NMOS transistors is $\beta = 1.3$, which is fixed by the technology. The dimensions for the 3.3V cell are also indicated for the sake of comparison.

The tapering factor γ of the pre-drivers was selected from simulation. As shown in Figure 4.15a, the simulation circuit is simply a realistic tapered buffer

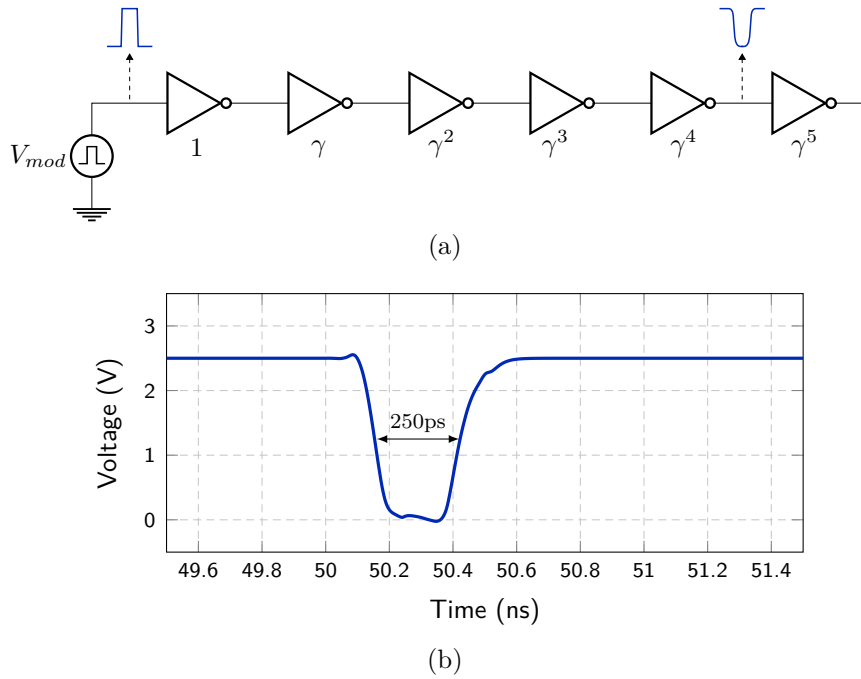


Figure 4.15 – Design of the pre-driver: (a) simulation circuit, (b) simulated output waveform of a pre-driver for a tapering factor of $\gamma = 3$ ($V_{DD} = 2.5V$, $t_{mod} = 250ps$).

composed of five inverter cells powered from a $2.5V$ voltage source. As a result of a simulation run, the factor was set to $\gamma = 3$ as it leads to a satisfactory propagation of a $250ps$ pulse (see Figure 4.15b). The simulated rise and fall times are approximately $100ps$.

It is important to note that tapered buffers can account for a substantial part of the total power consumption of the chip. This is especially true at high frequency functioning where switching losses cannot be neglected [101]. As a result, the final dimensioning of the gate drivers was simultaneously carried out with that of the power MOSFETs in order to optimize the circuit's power efficiency.

4.2.2.3 Power MOSFETs channel width sizing

The aim of this part is to set the width of the power MOSFETs forming the charging and discharging current paths of the flying capacitor (M_0 , M_1 , M_2 and M_4). These were all designed to operate in the triode region. Afterwards, the final sizing of the pre-drivers is carried out.

In terms of implementation, the MOSFETs driving the bottom plate of the flying capacitor, *i.e.* PMOS M_0 and NMOS M_1 , have been realized by $2.5V$ devices. Given that the voltages at their terminals switch between V_{SS}

and V_{DD} , they can be sized with the minimum channel length ($0.27\mu m$). The MOSFET M_2 is connected to the top plate of the flying capacitor. Since this potential is expected to rise up to $2V_{DD}$, the lower NMOS was realized by a 3.3V device. On the other hand, the upper NMOS connected between V_{DD} and the floating bulk node was sized with the minimum channel length. Last, the drain of NMOS M_4 is connected to the switching node V_K . As the latter is prone to voltage overshooting (due to parasitic inductance), these MOSFETs were implemented by 3.3V devices so as to guarantee the circuit's reliability.

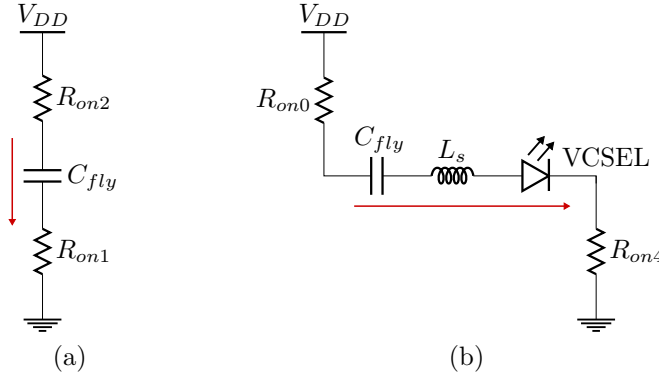


Figure 4.16 – Equivalent circuit of the power stage with the MOSFETs' channel resistance: (a) charging phase ϕ_0 , (b) discharging phase ϕ_1 .

The equivalent circuit of the power stage during each operating phase is illustrated in Figure 4.16. In phase ϕ_0 (see Figure 4.16a), the flying capacitor is charged through the channel resistance of M_1 and M_2 . Knowing that an incomplete charging of C_{fly} would eventually lead to a drop in driving current, the capacitor's recharge time is the main factor limiting the pulse repetition frequency of the driver. Thus, large MOSFETs with low channel resistance must be employed so as to minimize the RC charging time constant of C_{fly} . In phase ϕ_1 (see Figure 4.16b), C_{fly} discharges through the load and the channel resistance of M_0 and M_4 . Given that any resistive voltage drop in the discharge path tends to limit the driving current, M_0 and M_4 should be as large as possible. Nevertheless, since the driver aims for a high pulse repetition frequency, up to several hundreds of megahertz, dynamic losses due to gate capacitance switching cannot be ignored when dimensioning the MOSFETs. As a consequence, optimal sizing calls for a trade-off analysis between the driver's current capability, repetition frequency and power efficiency. The above explanation can be summarized with the basic equations of a transistor's channel resistance R_{on} and gate switching losses P_{sw} , which are antagonistic quantities as a function of the channel width W ,

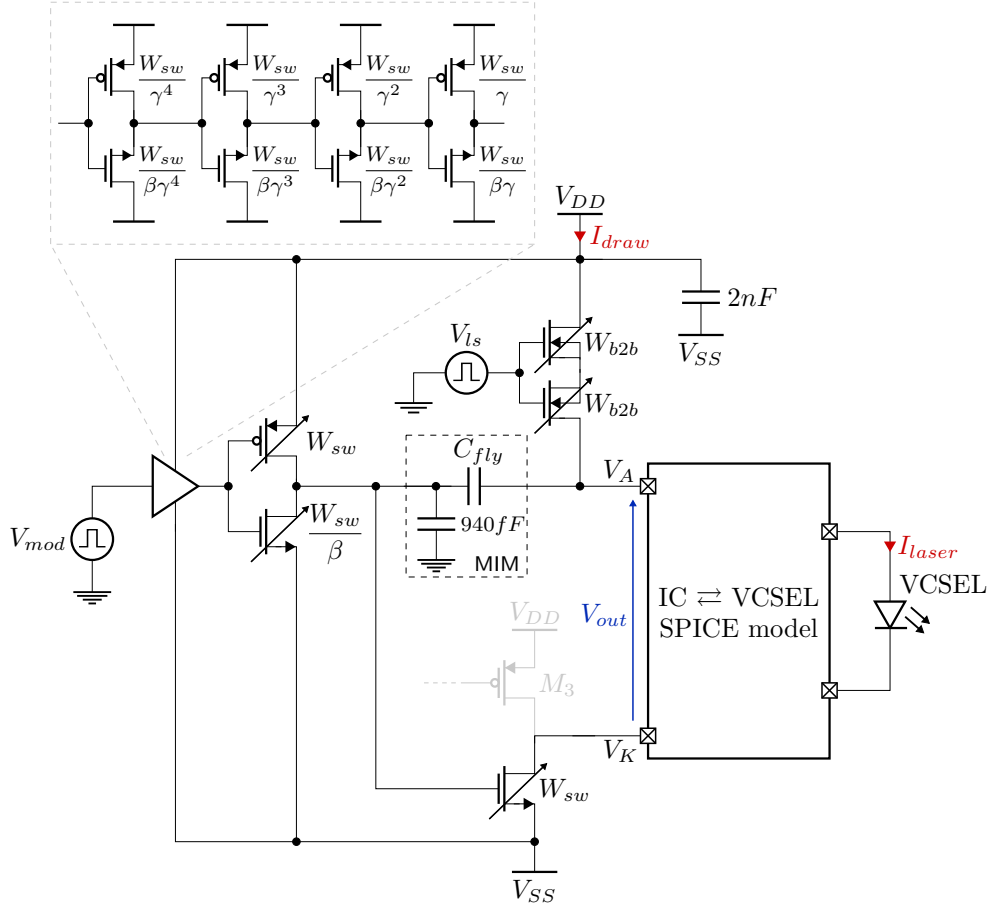


Figure 4.17 – Simulation circuit for dimensioning the power MOSFETs.

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \quad (4.3)$$

$$P_{sw} = W L C_{ox} V_{gs}^2 f_{sw}$$

where L is the channel length, μ is the charge carrier mobility, C_{ox} is the oxide capacitance, V_{gs} is the gate-source voltage and V_{th} is the threshold voltage [102].

The simulation circuit for the dimensioning is depicted in Figure 4.17. Two variable design parameters have been used: W_{b2b} and W_{sw} . W_{b2b} is the channel width of M_2 , whereas W_{sw} is the channel width of M_0 and M_4 . The pre-driver has been incorporated in the circuit in order to properly account for the switching losses. It is simulated with four inverter stages, all using W_{sw} as a parameter. Recall that $\beta = 1.3$ is the PMOS to NMOS width ratio and $\gamma = 3$ is the tapering factor computed in the preceding part. Two pulsed voltage sources are also added to mimic the control signals V_{mod} and V_{ls} .

The simulation is performed at a fixed 2.5V supply voltage. The pulse width and frequency of the control signals are respectively set to 500ps and

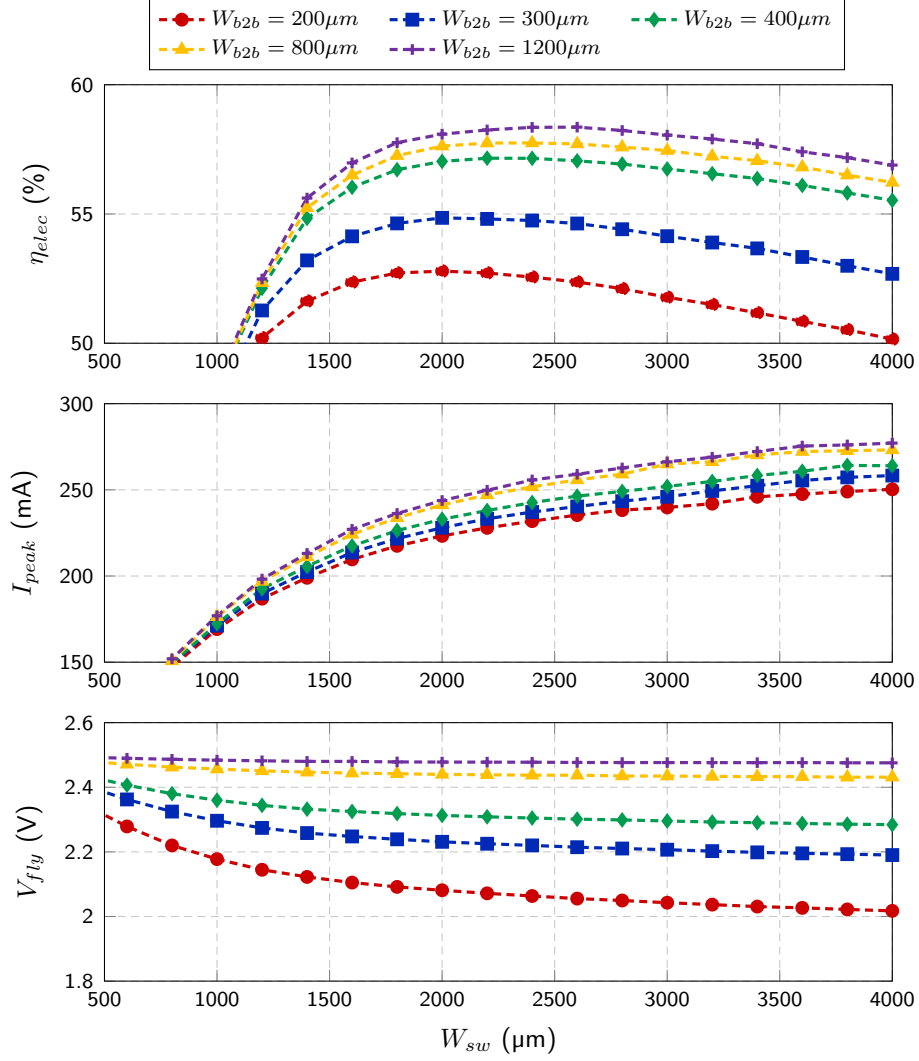


Figure 4.18 – Simulation results of the power MOSFETs sizing ($V_{DD} = 2.5V$, $t_{mod} = 500ps$, $f_{sw} = 200MHz$).

200MHz, *i.e.* typical operating conditions. The driving current peak I_{peak} , the power efficiency η_{elec} and the flying capacitor's charge voltage V_{fly} are extracted as a function of the MOSFETs' channel widths, W_{sw} and W_{b2b} . Simulation results are presented in Figure 4.18.

One can see that power efficiency reaches a maximum between $2000\mu m$ and $3000\mu m$. In contrast, the peak current increases continuously with increasing width, yet with a decreasing derivative (due to the fact that channel resistance varies with the inverse of the width). These curves clearly highlight the trade-off between driving capability and power losses.

A value of $800\mu m$ was chosen for W_{b2b} as it permits the flying capacitor to charge up to 95% of the supply voltage. A further size increase would result in a negligible gain in both driving current and efficiency. Additionally,

Device	Width (μm)	Length (μm)	Resistance (Ω)
PMOS M_0	1800	0.27	2
NMOS M_1	600	0.27	2
NMOS M_2	800	$0.27 + 0.55$	8
NMOS M_4	1800	0.55	3

Table 4.2 – Overview of the dimensions and channel resistances of power MOSFETs.

given that the driving signal V_{ls} is generated on-chip by a level-shifter circuit, increasing W_{b2b} also requires to build up the level shifter's driving strength, thus further augmenting silicon area overhead. On the other hand, M_0 and M_4 were dimensionned around $2000\mu\text{m}$ as a compromise between efficiency, peak current and area.

Table 4.2 presents the final dimensions of the power MOSFETs with the corresponding channel resistance. In the end, the width of M_1 was scaled down from $1384\mu\text{m}$ to $600\mu\text{m}$ in order to comply with the constraint of area. Note that values were rounded in order to ease layout.

On the basis of the power MOSFETs sizing, the pre-driver providing the driving signal V_{drv} can be dimensioned. The number of stage N_{stage} required is computed from,

$$N_{stage} = \frac{\ln\left(\frac{C_{power}}{C_{unit}}\right)}{\ln \gamma} = 4.79 \rightarrow 5 \text{ stages} \quad (4.4)$$

where $C_{power} = 4.45\text{pF}$ is the gate capacitance of M_0 and M_1 , $C_{unit} = 25\text{fF}$ is the gate capacitance of the standard inverter cell and γ is the pre-driver's tapering factor. These capacitances were extracted from simulation.

4.2.2.4 Sweep-out MOSFET channel width sizing

The sweep-out MOSFET M_3 plays a key role in the proposed laser diode driver topology, *i.e.* pulling the cathode node V_K to V_{DD} at the end of the driving current pulse. In this way, a negative voltage should be applied across the load, therefore ensuring fast laser switch-off. The main approach for dimensioning M_3 was to visualize the impact of the channel width on the transient behavior of node V_K .

Figure 4.19 depicts the simulated cathode voltage waveform as a function of the channel width of M_3 .

Without M_3 , node V_K is high-impedance and the circuit is roughly equivalent to a series RLC network. As for a classical voltage-mode topology, the

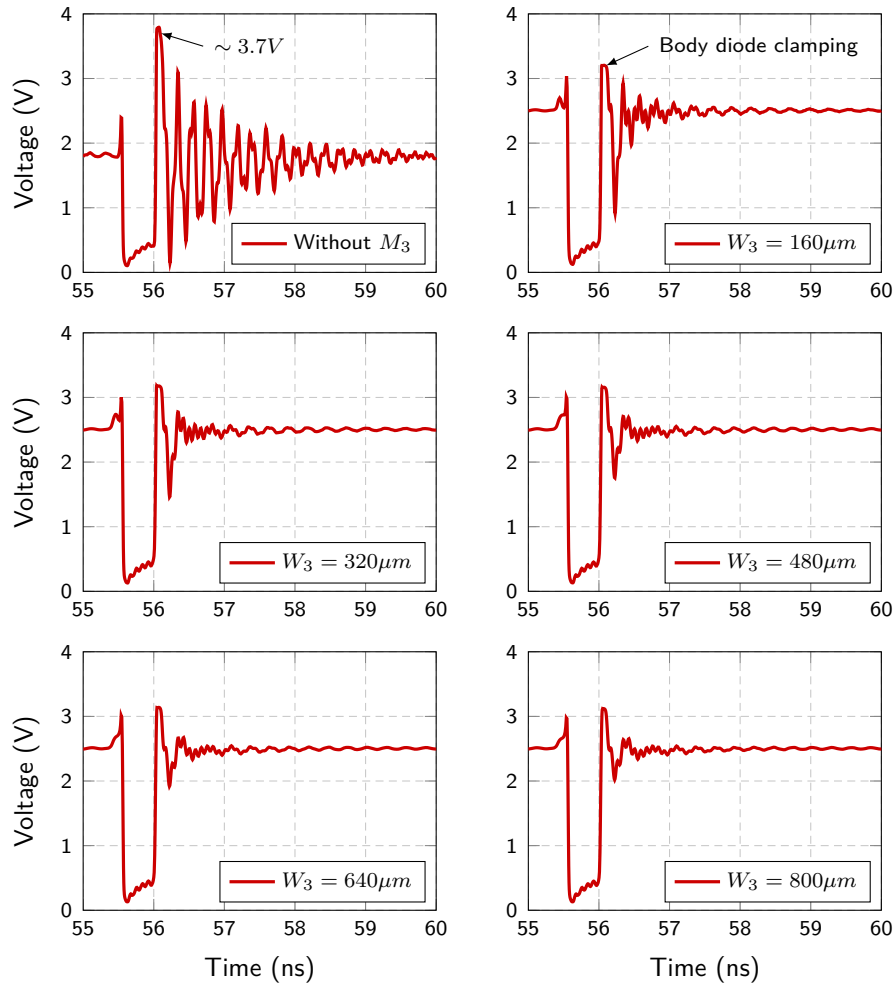
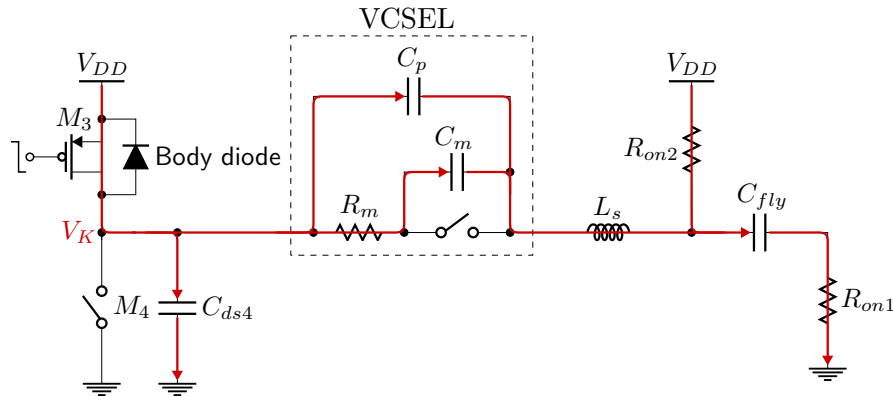


Figure 4.19 – Impact of the dimensioning of M_3 on the transient behavior of the cathode node ($V_{DD} = 2.5V$, $t_{mod} = 500ps$).


 Figure 4.20 – Equivalent circuit of the power stage with MOSFET M_3 .

drain-source capacitance C_{ds4} of M_4 rings together with the parasitic inductance and the VCSEL capacitances. This causes a significant voltage overshooting, up to 3.7V, at node V_K . The first spike remains below the breakdown voltage but still briefly exceeds the safe operating area of switch M_4 . In addition to detrimentally affect the reliability of the circuit, the subsequent ringing could also result in a succinct reignition of the VCSEL (due to the fact that the cathode voltage is such that a forward bias voltage could briefly build up across the laser diode).

Remaining in Figure 4.19, there is clear evidence that M_3 provides an enhanced control over parasitic ringing. As illustrated in Figure 4.20, M_3 pulls up the voltage across capacitance C_{ds4} that is involved in the RLC resonance. This leads to a rapid damping of the oscillations. Additionally, voltage clamping through the PMOS body diode ($p+/NW$) contributes to mitigate voltage overshooting. In consequence, the starting voltage spike is reduced from 3.7V down to $V_{DD} + V_t \sim 3.2V$, with $V_t \sim 0.7V$ being the threshold voltage of the diode. Yet, such a result depends largely on how well the body diode is modelled. In the 40nm technology design kit, available MOSFET models do not fully include the body diode. Thus, the effective voltage clamping seen on the cathode voltage waveform must be carefully looked at. Concerning channel width sizing, so as to rapidly eliminate parasitic ringing, the channel resistance of M_3 should as small as possible. In other word, M_3 should act as a low-impedance pull-up resistor in order to guarantee a fast laser turn-off transient.

In the end, PMOS M_3 has been implemented as a 3.3V MOSFET (channel length of $0.44\mu m$) with a channel width of $480\mu m$. This specific value has been chosen on the basis of physical layout concerns in order to take into account area and routing constraints.

In the same manner as for the power MOSFETs, M_3 is driven by the signal $\overline{V_{drv}}$ which is provided by a pre-driver with a tapering factor of $\gamma = 3$. So as to ensure proper synchronization of the driving signals, the latter has been

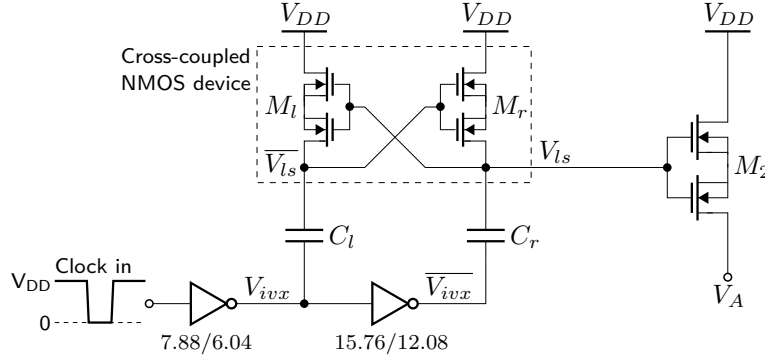


Figure 4.21 – Schematic of the charge-pump level-shifter for generating the driving signal V_{ls} .

dimensioned so that it exhibits the same propagation delay as the pre-driver associated with MOSFETs M_0 and M_1 .

4.2.3 Level shifter

In order to generate the driving signal V_{ls} , a clock driver with a pumped output voltage was employed [103]. The level shifter structure is depicted in Figure 4.21. The circuit operation is as follows: when the input node is low, node V_{ivx} is set to V_{DD} and NMOS M_r is turned on due to capacitive coupling through C_l . As a consequence, node V_{ls} is precharged to V_{DD} . When the input node goes high, node $\overline{V_{ivx}}$ is set to V_{DD} , thus pushing node V_{ls} above V_{DD} due to capacitive coupling through C_r . The resulting voltage is set according to the capacitive voltage divider principle. It can be approximated from,

$$V_{ls} = V_{DD} \left(1 + \frac{C_r}{C_r + C_{g2}} \right) \quad (4.5)$$

where C_{g2} is the gate capacitance of NMOS M_2 . The latter was extracted from simulation, $C_{g2} \approx 1.87pF$.

In terms of implementation, the inverter cells have been realized from 2.5V devices. Since the shifted nodes V_{ls} and $\overline{V_{ls}}$ are expected to exceed V_{DD} , 3.3V MOSFETs have been used to implement M_l and M_r . These were laid out following a back-to-back setup so as to avoid body diode conduction (see Part 4.2.2.1). Coupling capacitors C_l and C_r have been realized by MIM devices because of their high density and negligible variation versus voltage.

The dimensioning was carried out for a supply voltage of 2.5V. The circuit was sized so that V_{ls} and $\overline{V_{ls}}$ can be pushed to 3.6V. In this way, the gate voltage of M_2 can exceed $V_{DD} + V_{th}$, with V_{th} being the MOSFET's threshold voltage. The dimensions of the components are listed in Table 4.3.

Note that the left side of the cross-coupled NMOS device was sized smaller than the other side as it does not supply any power to the output of the circuit.

Device	Width (μm)	Length (μm)	Value (fF)
M_l	12	2×0.55	—
M_r	120	2×0.55	—
C_l	8×4	8×4	544
C_r	8×8	8×8	2176

Table 4.3 – Dimensions of the level shifter’s component.

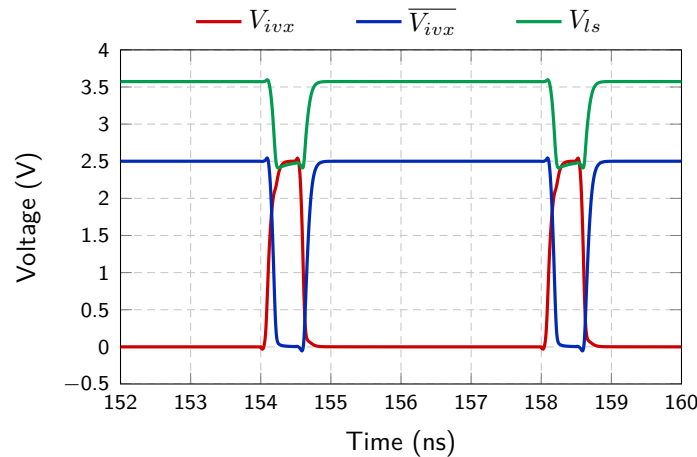


Figure 4.22 – Simulated waveforms of the charge-pump level-shifter ($V_{DD} = 2.5V$, $t_{mod} = 500ps$, $f_{sw} = 250MHz$).

The node $\overline{V_{vx}}$ being only used to drive M_r . The simulated waveforms of the level shifter are represented in Figure 4.22.

Last but not least, small inverters acting as a delay cell have been connected upstream of the level shifter. Their role is to match the propagation delay of the level-shifter with the one of the pre-drivers. In this way, it was ensured that the driving signals were synchronized when fed to the power stage.

It is important to keep in mind that a charge-pump level-shifter topology was chosen for the sake of simplicity. As the output voltage is sensitive to supply voltage and process variations, a more robust solution would be to use a regulated voltage level.

4.3 Cell physical layout considerations

This section covers critical layout concerns that were looked at during circuit design. These considerations apply mainly to the MOSFETs forming the driver’s power stage, that is large devices with high switched current.

4.3.1 Switching noise

Fast switching transients of large transistors operating at high frequency induce parasitic current injections which translate into an electrical noise. The latter is referred to as switching noise. For instance, capacitive coupling associated with reverse junctions in CMOS technologies is a substantial switching noise injection mechanism [97]. As mentioned in Part 4.2.1.2, this noise can degrade the performances of analog and digital adjacent circuits as well as cause latch-up chip failures. Accordingly, the circuit's physical layout has been carried out with the aim of minimizing its impact.

It is a common approach to shield any noisy circuit and noise sensitive circuit with $p+$ or $n+$ implants, also referred to as guard rings. In this manner, a low-impedance path to ground or a reference voltage source is created for parasitic charge injections [104]. Furthermore, as guard rings ideally hold the substrate and the different wells at a fixed potential, it is an effective layout strategy for mitigating latch-up issues [98].

The cross section and top views of the guard ring strategy for both NMOS and PMOS devices are respectively presented in Figure 4.23 and Figure 4.24.

Given that the driver is supplied from dedicated power supply and ground pins, each NMOS has its bulk (PW) connected at a different potential than the one of the substrate. Apart from back-to-back MOSFETs which have a floating bulk node, all NMOS have the bulk and source tied together to V_{SS} . The bulk polarization is ensured by a $p+$ diffusion (GR_0) surrounding the active NMOS region. The DNW which provides the isolation from the substrate must be connected to a high voltage via a low-impedance path. To this end, an $n+$ implant (GR_1) is added and tied to V_{DD} . As it is the highest voltage level in the circuit, parasitic junctions PW/DNW and PSUB/DNW are reverse-biased. The whole structure is enclosed inside a $p+$ implant (GR_2) connected to the substrate ground. In this way, the vertical PNP bipolar transistor (PW/DNW/PSUB) is kept off, thus preventing latch-up problems.

All PMOS have the bulk (NW) and source connected together to V_{DD} . The PMOS active region is surrounded by an $n+$ diffusion (GR_0) which ensures the polarization of the NW. The latter is shielded with a $p+$ implant (GR_1) tied to the substrate ground. Given that the NW is connected to V_{DD} , the PSUB/NW junction is properly reverse-biased and the parasitic PNP bipolar transistor ($p+$ /NW/PSUB) is off.

It is important to note that minimum width and spacing design rules must be applied when implementing the guard rings. As a consequence, the present layout strategy results in a substantial increase in silicon area overhead [98].

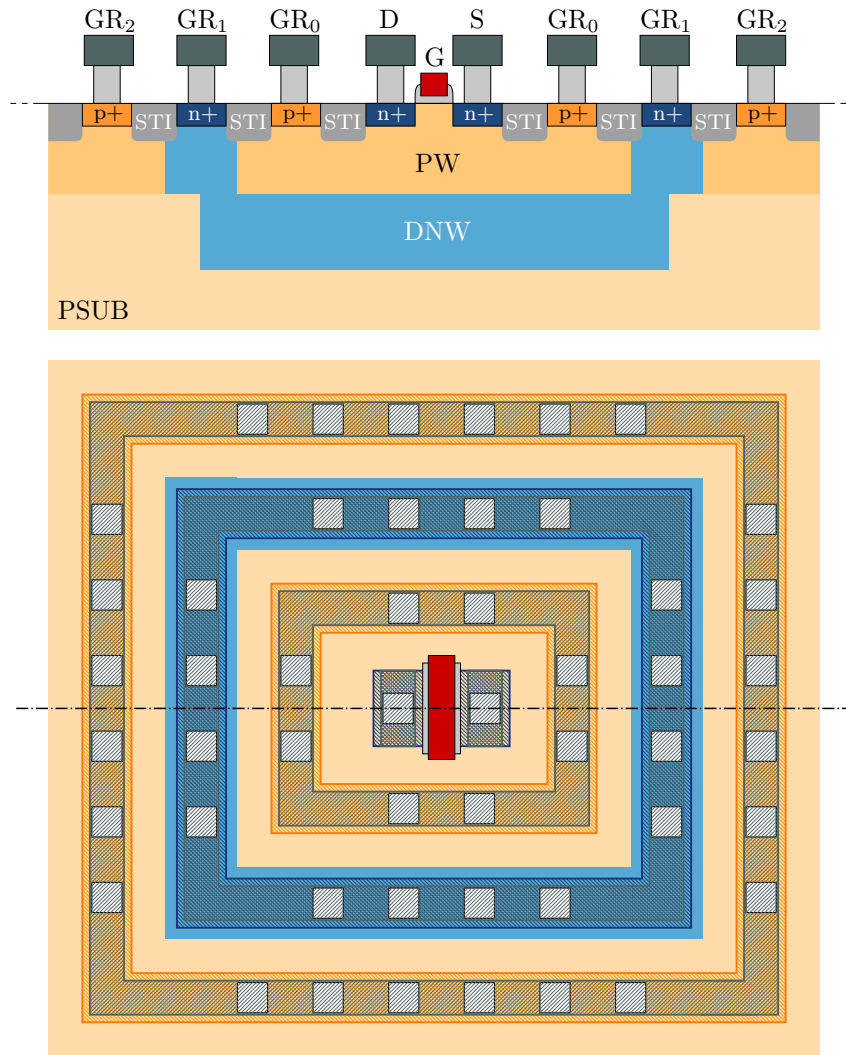


Figure 4.23 – Cross section and top views of the guard-ring layout for n -channel MOSFETs.

4.3.2 Metal routing parasitics

The MOSFETs forming the driver's power stage were laid out as multi-fingers structures. As shown in Figure 4.25, the gate is divided into multiple parallel stripes with an alternating arrangement of the source and drain contacts [42]. This strategy allows large devices to exhibit a reasonable aspect ratio, thus easing their placement as well as their interconnection at the chip level. Furthermore, given that two successive parallel fingers share common drain or source contacts, multi-fingers devices are rather area efficient structures.

In a CMOS chip, metal layers are used to connect together the circuit's components. The metal stack for the 40nm CMOS technology by STMicro-

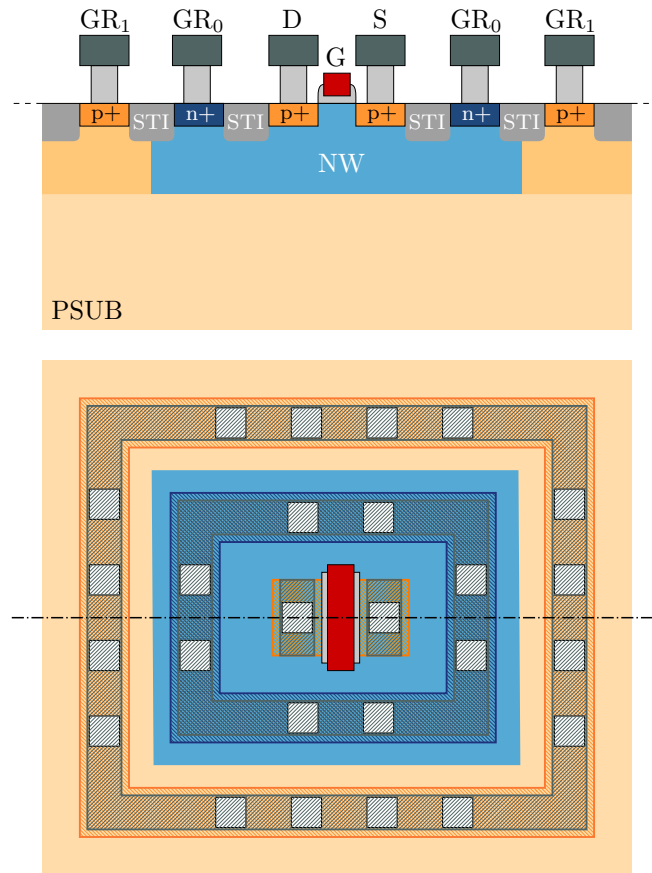


Figure 4.24 – Cross section and top views of the guard-ring layout for p -channel MOSFETs.

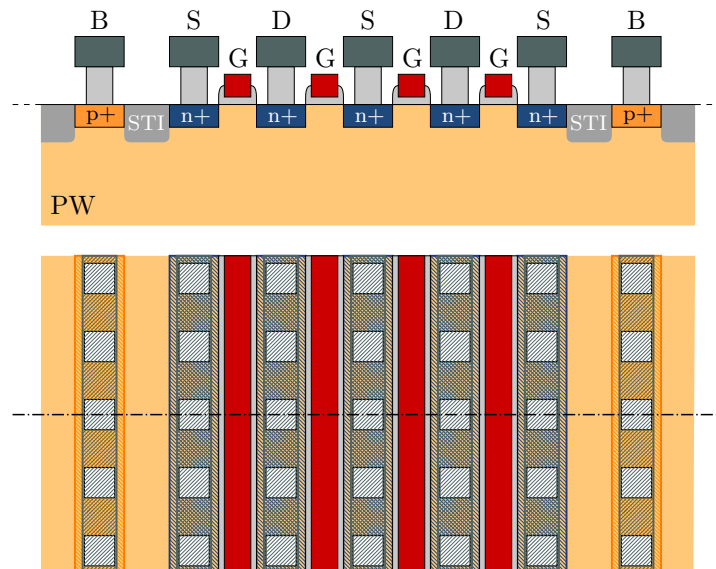


Figure 4.25 – Layout of a multi-fingers n -channel MOSFET.

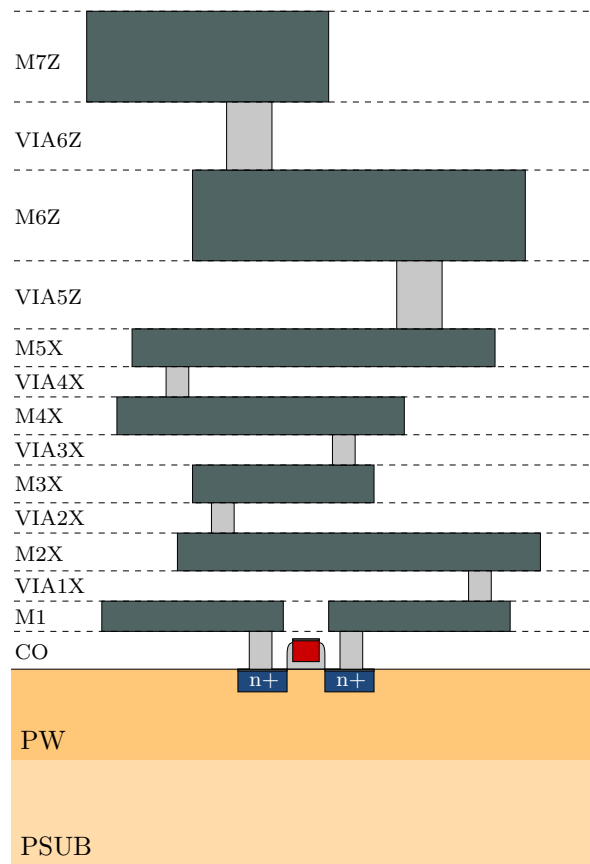


Figure 4.26 – Metal stack of the 40nm CMOS technology by STMicroelectronics.

electronics is depicted in Figure 4.26. Recall that the two upper layers (M6Z and M7Z) are thicker and are dedicated to power distribution. Additionally, neighboring metal layers are interconnected using vias (from CO to VIA6Z).

Typically, metal layers are associated with parasitic series resistance and parallel capacitance [105]. These may have a detrimental impact on the overall performance of the circuit. On one hand, metal resistance in the power path induces a voltage drop which lowers the driver's current capability. On the other hand, capacitive coupling between adjacent metal tracks increases switching losses, thus reducing power efficiency. Last but not least, parasitic capacitance also increases the propagation delay of the signals, thus affecting their synchronization.

As a consequence, multiple parallel metal layers and numerous vias have been used for routing the power path. In this way, metal resistance can be minimized. At the same time, the use of multiple layers restricts the current density, thus mitigating metal electromigration [105]. What is more, parasitics have been reduced by applying the minimum spacing rules in order to keep the length of the metal routes as short as possible.

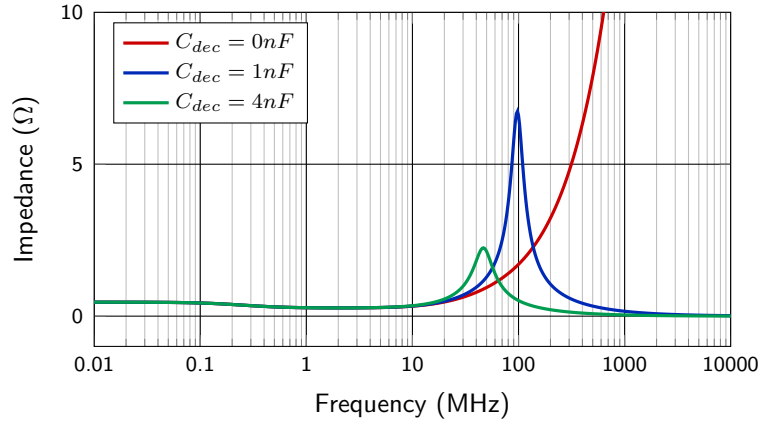


Figure 4.27 – Impedance versus frequency characteristics of the PDN as a function of the on-chip decoupling capacitance.

4.4 On-chip decoupling capacitor

Since fast transient currents are drawn from the power supply, an on-chip decoupling capacitor is mandatory by design. Its role is to attenuate supply voltage fluctuations due to Ri and $L\frac{di}{dt}$ drops through the power distribution interconnect. The capacitor must be sufficiently large so that V_{DD} and V_{SS} ring in unison [42].

Figure 4.27 represents the impedance characteristics of the power distribution network (PDN) with different on-chip decoupling capacitance C_{dec} .

Without on-chip decoupling, the PDN impedance tends towards infinite due to the parasitic inductance of the bond wires (red curve). In such a case, the circuit would not be functional. In order to minimize the PDN impedance and reject any resonance outside of the operating frequency range of the circuit, *i.e.* well below 100MHz , the capacitance should be as large as possible.

In terms of implementation, an NMOS transistor set up as a capacitor is suitable for decoupling purposes. As it operates in strong inversion, a high capacitive density can be achieved [60]. The physical layout of the unitary decoupling cell is presented in Figure 4.28. It is built from thick-oxide NMOS capacitors arranged in a square shape. These are implanted in a PW connected to V_{SS} and isolated from the substrate by a DNW tied to V_{DD} . In order to further increase density, a MIM capacitor was stacked over and connected in parallel to the NMOS devices. In terms of interconnect, M3 and M4 metal routes are added so as to form a dense metal grid in order to reduce parasitic resistance and improve decoupling effectiveness.

The capacitance of the unitary cell is approximately 8pF . So as to get as much capacitance as possible, this cell was distributed in order to fill the

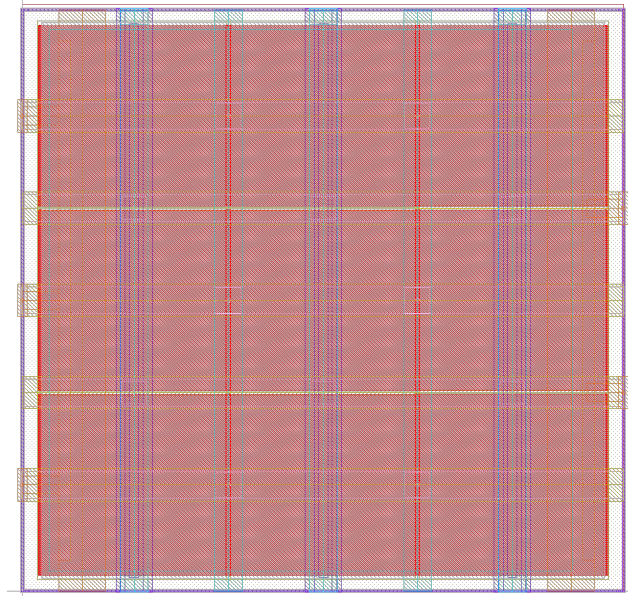


Figure 4.28 – Physical layout of the unitary decoupling capacitor cell.

remaining area available in the chip.

4.5 Layout view

4.5.1 VCSEL driver layout

The layout view of the VCSEL driver is presented in Figure 4.29. Most of the silicon area is occupied by the flying capacitor. Recall that the space below the MIM capacitor's bottom plate was kept empty in order to minimize substrate coupling.

The sub-circuits ensuring the generation of the driving signals, *i.e.* the pre-drivers and level shifter, have been placed at the top of the circuit. The driving signals are fed to the power stage using M6Z metal tracks. Last, the power MOSFET have been connected to the metal pads via large M7Z metal routes.

4.5.2 Chip-level layout

The floorplan of the full chip is illustrated in Figure 4.30. The driver circuit has been placed as close as possible to the metal pads with the aim of minimizing the length of the power route.

A specific pad has been used for the anode node V_A . As a matter of fact, the latter must sustain fast voltage variations up to $2V_{DD}$. In contrast, the other pads (V_{DD} , V_{SS} and V_K) were re-used from latter version of the vehicle circuit.

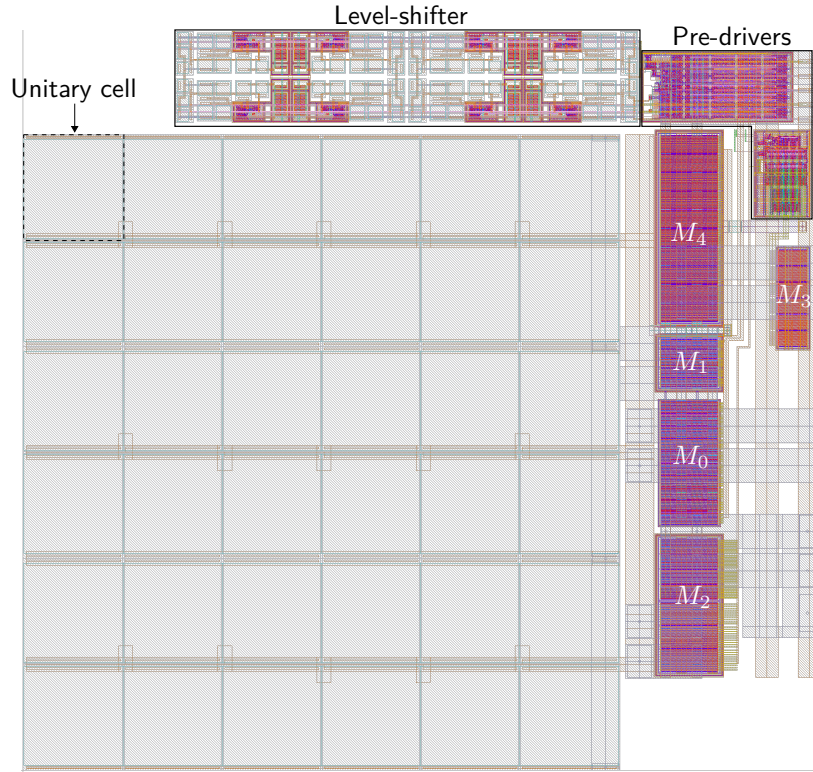


Figure 4.29 – Physical layout of the VCSEL driver.

The remaining area at the bottom right corner of the die was filled with unitary decoupling cells. In the end, a decoupling capacitor of approximately $1nF$ was integrated.

4.6 Post-layout verification

The designed VCSEL driver have been simulated together with the relevant adjacent circuits in the chip. These include the pulse generator, the laser safety unit and the metal pads. So as to take into account the metal routing parasitics, a post-layout extraction of the driver's power stage was performed. In this way, both parasitic resistances and capacitances can be incorporated in simulation.

The simulation is carried out at a fixed $2.5V$ supply voltage. The modulation pulse width and frequency were set to $500ps$ and $200MHz$, respectively. The simulated waveforms are presented in Figure 4.31.

Results show that the circuit is functional within the STVC hardware. First, the driving signals are reasonably synchronized when fed to the power stage. The ripple voltage associated with V_{DD} is less than $100mV$, meaning that a sufficient on-chip decoupling capacitor has been added. Furthermore, the flying capacitor voltage waveform is consistent with the predicted circuit

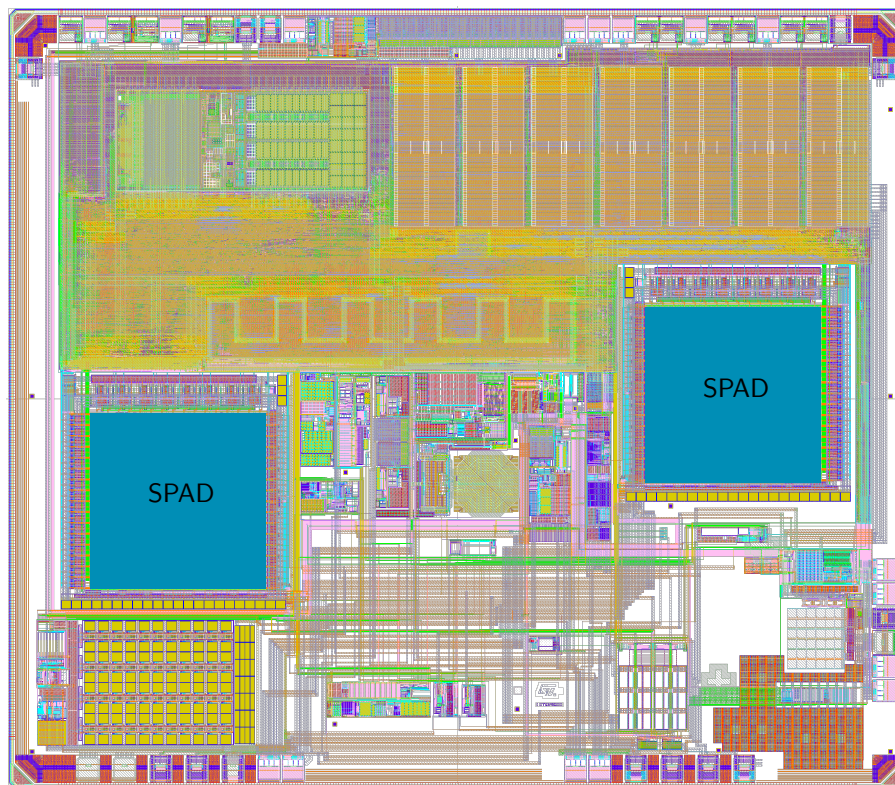


Figure 4.30 – Floorplan of the full chip with the VCSEL driver in the bottom right corner.

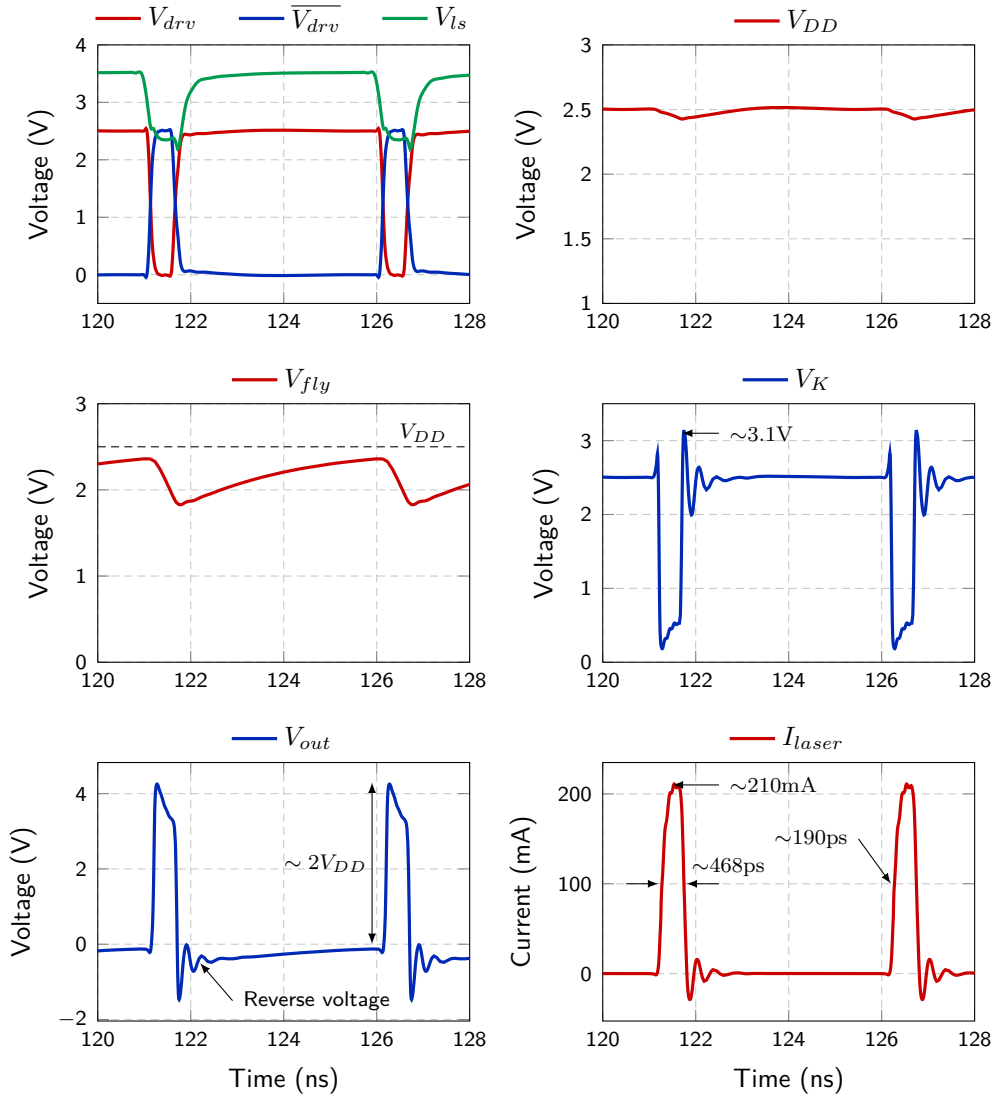


Figure 4.31 – Post-layout simulated waveforms of the VCSEL driver ($V_{DD} = 2.5V$, $t_{mod} = 500ps$, $f_{sw} = 200MHz$).

t_{mod}/f_{sw}	1ns/100MHz	500ps/250MHz	250ps/250MHz
I_{peak} (mA)	222.6	207.5	193.3
t_{pw} (ps)	972	468	230
t_r (ps)	188	188	189
t_f (ps)	94	92	95
$\frac{\Delta I_{laser}}{\Delta t}$ (mA.ps ⁻¹)	0.94	0.88	0.81
P_{draw} (mW)	111.7	140	78.6
η_{elec} (%)	55	48.7	35.5

Table 4.4 – Overview of the post-layout simulation results ($V_{DD} = 2.5V$).

operation, *i.e.* repeated charging and discharging cycles. Due to the capacitive voltage boost structure, the load voltage waveform represents a fast impulse with a rise time of $50ps$ and a magnitude of approximately $2V_{DD}$. Then, the voltage is kept in the negative range during the off time of the VCSEL, which is the expected impact of the carrier sweep-out circuit feature. The driving current pulse waveform exhibits a peak at $210mA$ and a duration of $468ps$, thus meeting the design target. The simulated current rise time is approximately $190ps$, which is primarily set by the amount of parasitic inductance in the current path through the VCSEL.

Table 4.4 summarizes the simulated performances of the VCSEL driver in different operating conditions. The corresponding current pulse waveforms are illustrated in Figure 4.32. With a $1ns$ pulse width, one can clearly notice the discharge of the flying capacitor. This stresses that the driving pulse duration is inherently limited with the proposed driver topology. Moreover, for a $1ns$ as well as for a $500ps$ pulse, both the $200mA$ current and 47% power efficiency specifications are duly respected. However, when setting the pulse width down to $250ps$, the driving current peak is limited to $193.3mA$ due to the fact that the pulse is terminated prior to full build up. This is primary the result of the parasitic inductance contributed by the physical interconnect of the VCSEL. For the same reason, the power efficiency drops to 35.5% and the 47% target is no longer met. Thus, optimizing the mounting and interconnection of the laser diode appears a key design focus for guaranteeing efficient sub- ns driving current pulse operation.

In a nutshell, encouraging simulation results have been demonstrated. These clearly prove the feasibility and satisfactory performances of the proposed VCSEL driver circuit architecture.

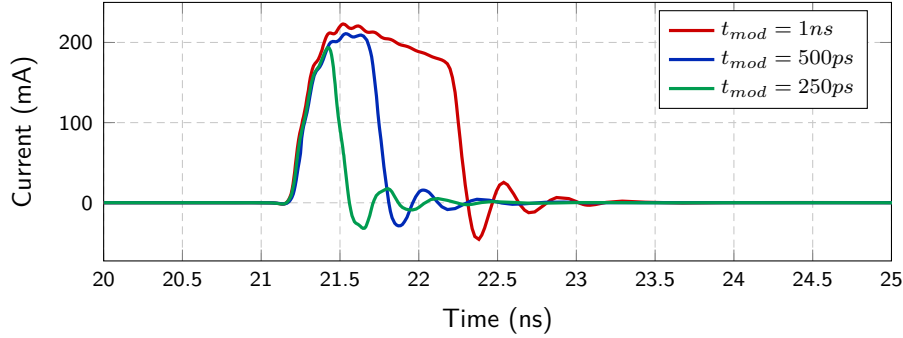
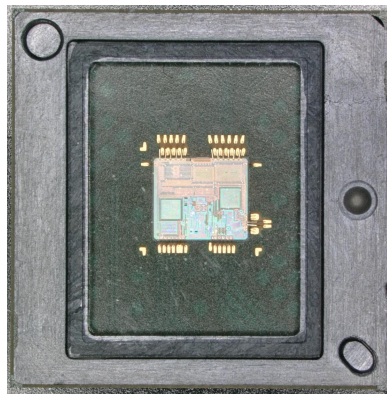


Figure 4.32 – Simulated driving current pulse waveform for different modulation pulse width ($V_{DD} = 2.5V$, $f_{sw} = 200MHz$).

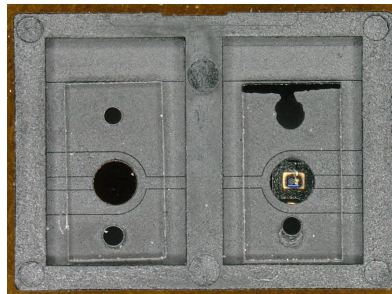
4.7 Conclusion

This chapter detailed the core of this thesis, *i.e.* the design of the integrated VCSEL driver. Due to planning constraints, the IC was fabricated in a three-dimensional (3D) 40nm CMOS process instead of a standard process. In order to comply with new process rules, the SPAD arrays within the chip had to be removed. This had a non-negligible impact on the testing procedure of the IC, which is the topic of the upcoming chapter.

Two distinct land grid array (LGA) test chips were fabricated, both serving different testing purposes (see Figure 4.33). With the LGA electrical package, the driver circuit is not loaded and can be connected to any component. This package was exploited for electrical characterization with a resistive load. On the other hand, the LGA optical module, incorporating the VCSEL array, was used for laser measurements.



(a)



(b)

Figure 4.33 – Fabricated test chip: (a) LGA electrical package, (b) LGA optical module.

5 Experimental characterization

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This chapter presents the experimental setup and measurement results of the proposed VCSEL driver topology fabricated in the STMicroelectronics' 40nm CMOS technology. The purpose herein is to assess the functioning, performances as well as the limitations of the designed driver. To this end, the test chip was first verified via electrical measurement prior to being tested in an optical test setup.

5.1 Experimental methodology

The experimental process was divided in two parts. First, an electrical measurement bench was set up, whose aim was to characterize the driving current pulse through a resistive load. Given that there are no specific laser safety requirements associated with this experiment, the electrical bench allowed to rapidly check the proper functioning of the driver. At a later stage, an optical measurement bench was set up in order to assess the characteristics of the laser pulse.

In order to perform testing, the fabricated chip (either LGA or module) was mounted onto a dedicated characterization printed circuit board (PCB).

The latter was re-used from previous product verification within STMicroelectronics. Since the modulation signal of the laser diode is generated on-chip, a STM32 microcontroller board was connected to the characterization PCB through an I²C communication bus. In this way, the modulation pulse width t_{mod} (125ps time stepping) and frequency f_{sw} can be configured via a Python script. The characterization PCB was designed to operate together with a power board. Yet, herein the chip was powered from an external power supply to allow monitoring of the average current drawn by the circuit. This permitted to characterize the driver's power consumption and efficiency.

Even though the goal of the thesis was to demonstrate a proof of concept at a supply voltage of 2.5V, the test chip was experimentally evaluated with a product-like voltage range, between 1.8V and 2.8V. However, due to the lack of availability of appropriate testing equipment, the driver was not characterized as a function of temperature. Thus, all measurements were performed at room temperature.

The crucial challenge related to the experimental setup lies in accurately capturing the transient propagation of sub-ns pulses. In order to guarantee the fidelity of time-domain measurements, the test equipment must exhibit a bandwidth greater than the -3dB bandwidth of the signal of interest. Therefore, measurement instruments were selected based on these bandwidth and accuracy constraints.

Throughout this chapter, extracted performances are compared, to the extent possible, to post-layout simulation (PLS). The key metrics that are looked at are summarized in Table 5.1, which recalls specifications and PLS results in typical operating conditions ($V_{DD} = 2.5V$, $t_{mod} = 500ps$, $f_{sw} = 250MHz$).

Name	Symbol	Target	PLS	Unit
Peak current	I_{peak}	200	207.5	mA
Power consumption	P_{draw}	—	140	mW
Power efficiency	η_{elec}	47	48.7	%
Current pulse width	t_{pw}	< 1	0.468	ns
Current pulse rise time	t_r	—	188	ps
Current pulse fall time	t_f	—	92	ps
Average optical power	$P_{opt,avg}$	—	—	mW
Laser pulse width	t_{opt}	< 1	—	ns

Table 5.1 – Metrics of interest for the experimental characterization.

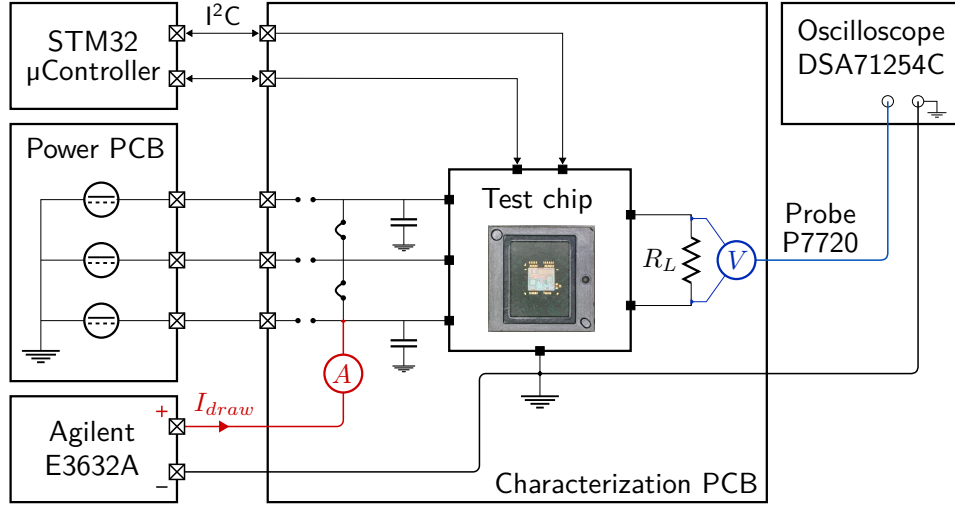


Figure 5.1 – Synoptic of the electrical measurement setup.

5.2 Electrical verification

5.2.1 Test setup

The synoptic of the electrical test setup is presented in Figure 5.1. The load consists in a surface-mounted 0805 resistor which acts as a current sensing device. The resistance R_L was chosen in accordance with the static $I - V$ curve of the VCSEL array,

$$R_L = \frac{V_{laser}}{I_{laser}} = \frac{3.2V}{200mA} = 16\Omega \quad (5.1)$$

A Tektronix P7720 differential voltage probe (20GHz bandwidth) was employed to measure the voltage V_L across the load resistor. The P7720 exhibits a 100kΩ DC input resistance, thus guaranteeing low probe loading, *i.e.* signal loss. As shown in Figure 5.2, the probe's flex tip was soldered to the terminals of the load resistor. Given that the connecting wires add parasitics, the actual bandwidth of the probe is eventually lower than the 20GHz specification. Hence, the wire length was kept as short as possible [106]. In order to visualize the electrical waveform, the probe was connected to a Tektronix DSA71254C oscilloscope (12.5GHz bandwidth, 50GS/s).

The three supply pins of the test chip were jointly connected to an Agilent E3632A power supply. In addition, the power supply, the chip and the oscilloscope were connected to a common ground potential.

The driving current peak can be directly derived from Ohm's law,

$$I_{peak} = \frac{V_{peak}}{R_L} \quad (5.2)$$

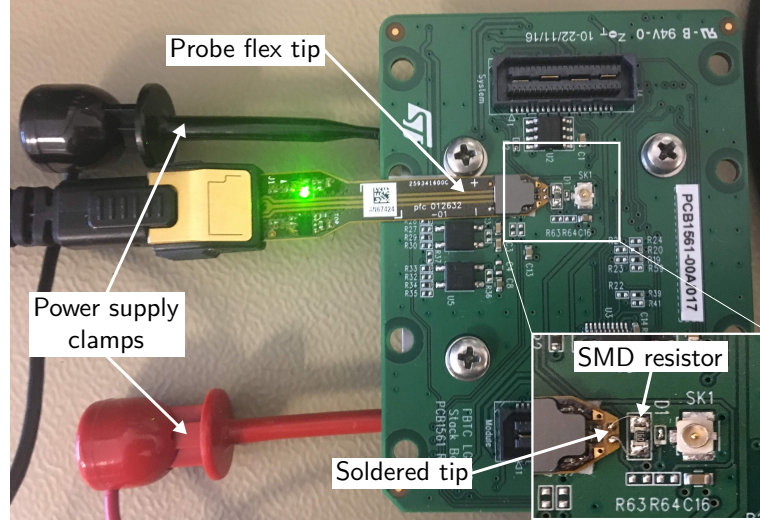


Figure 5.2 – Photograph of the PCB’s rear side with the differential voltage probe attached.

where V_{peak} is the peak voltage measured across the load resistor. Then, the power efficiency is expressed as,

$$\eta_{elec} = \frac{\overline{P_L}}{\overline{P_{draw}}} = \frac{\overline{P_L}}{V_{DD} \overline{I_{draw}}} \quad (5.3)$$

where:

- P_L is the power measured across the load resistor. It was computed from $\frac{V_L^2}{R_L}$ using the oscilloscope’s math functionality.
- V_{DD} and $\overline{I_{draw}}$ are respectively the supply voltage and the average current consumption visualized on the E3632A supply. Hence, P_{draw} is the average power consumption of the chip.

Note that in order to assess the effective consumption of the laser diode driver, the drawn current was firstly evaluated with the driver disabled. Then, this measured value was subtracted from the overall current consumption measured with the driver enabled.

5.2.2 Measurements

5.2.2.1 Behavioural assessment

So as to qualitatively check the behavior of the circuit, the electrical measurement was first carried out for above- ns pulse durations. In this way, the electrical waveform was measured for a $2ns$ and a $4ns$ pulse width with a $62.5MHz$ repetition frequency (smallest frequency setting of the test chip) and a $2.5V$ supply voltage. The measured voltage, image of the driving current pulse, is shown in Figure 5.3.

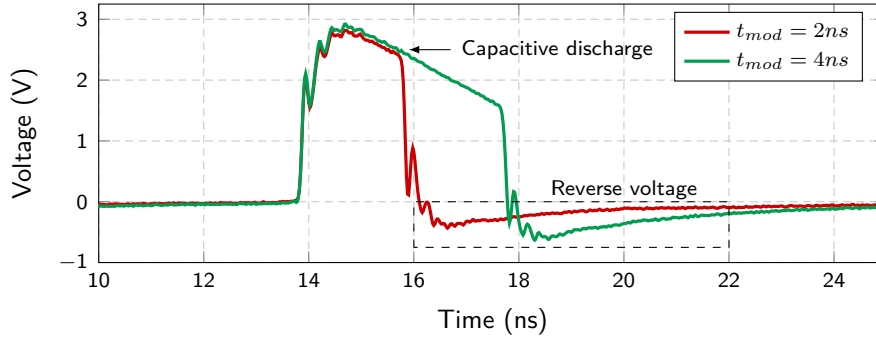


Figure 5.3 – Electrical waveform measurement for above- ns pulse width ($V_{DD} = 2.5V$, $f_{sw} = 62.5MHz$).

At first sight, the current pulse shape is consistent with the predicted circuit operation. As a matter of fact, the discharge of the flying capacitor is distinctly observed. During the off time, the voltage is slightly negative due to the carrier sweep-out and tends towards zero through the charging of the flying capacitor. Furthermore, one can see that the magnitude of the reverse voltage rises with increasing pulse width. This is a logical finding as the reverse voltage is proportional to the total charge pulsed through the load.

5.2.2.2 Sub-ns pulse measurement

First, the electrical waveform was characterized in the less constraining use case, that is for a $1ns$ pulse width and a $100MHz$ frequency (10% duty cycle). The supply voltage was fixed to $2.5V$. Figure 5.4 illustrates the measured voltage waveform. The driver is capable of generating an electrical pulse up to $2.76V$, *i.e.* $172.5mA$. The pulse duration is $975ps$ with $306ps$ and $322ps$ rise and fall times, respectively. However, although the global behavior is consistent, the measured values differ quite widely from those computed from PLS (with a VCSEL as load). Indeed, a 22.5% drop in peak current can be noticed. The rise and fall times are also substantially increased to 62% and 242%, respectively. Last but not least, a significant ringing can be observed in both the electrical pulse's rising and falling edges. Accordingly, the measured waveform was further compared to PLS. The circuit model of the load is presented in Figure 5.5a, where L_s and R_s depict the overall parasitic inductance and resistance, respectively. Note that the P7720 probe's circuit model is given in [106].

The waveform comparison is illustrated in Figure 5.5b. The dashed curve is computed based on parasitics' values consistent with those calculated in Chapter 3, *i.e.* $L_s = 2nH$ and $R_s = 250m\Omega$. In such a case, the current pulse rises up to $220mA$, which is similar to the previous PLS result of $222.6mA$. In order to match the measurement, L_s and R_s must be respectively increased up to $7nH$ and 4Ω . Even though the ringing is still not captured, the measured

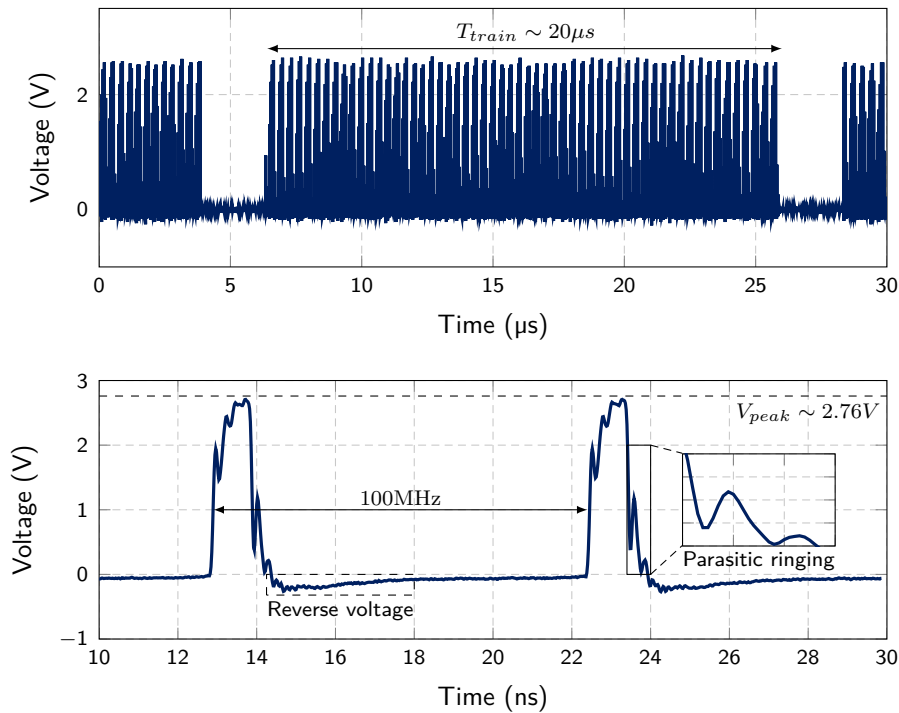


Figure 5.4 – Electrical waveform measurement ($V_{DD} = 2.5V$, $t_{mod} = 1ns$, $f_{sw} = 100MHz$).

waveform can be closely approximated. This highlights that the difference between PLS and measurement is probably due to the parasitics contributed by the test setup. As a matter of fact, the package leads, the PCB routing and the load resistor add circuit parasitics which can severely impact the load pulse, reducing both the available current and the transient speed.

Figure 5.6 presents the experimental characterization of the driver for a supply voltage sweep between 1.8V and 2.8V. The modulation pulse width and frequency are respectively set to 1ns and 100MHz. One can see that I_{peak} increases linearly with voltage, ranging from 110mA to 190mA. On the other hand, the temporal characteristics of the electrical pulse are relatively stable (less than 2.6% variation) within the voltage range. Similarly, the driver's power efficiency changes little with voltage and reaches a maximum of 53.3% at 2.5V. This is a particularly good result as the measured value is of the same order as the one extracted from PLS, *i.e.* 55%. The corresponding power consumption is 67.5mW.

At a 2.8V supply voltage, the circuit exhibits an erratic behavior with an abnormal increase in losses. At the same point, the driving current saturates. This issue was not investigated because it was not noticed with the optical measurement setup.

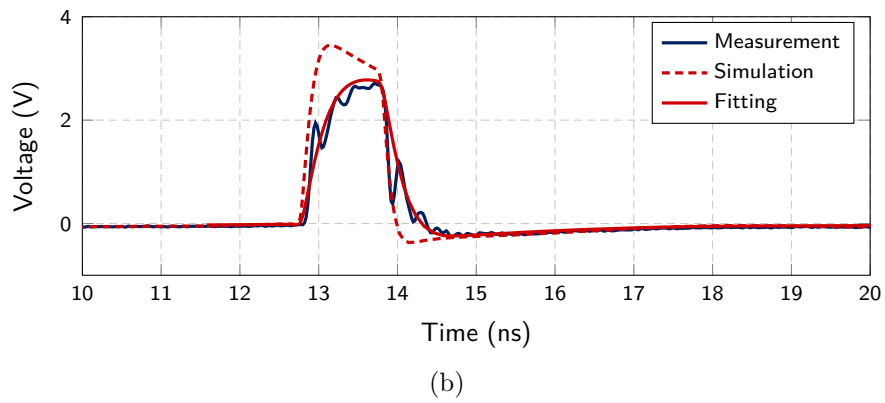
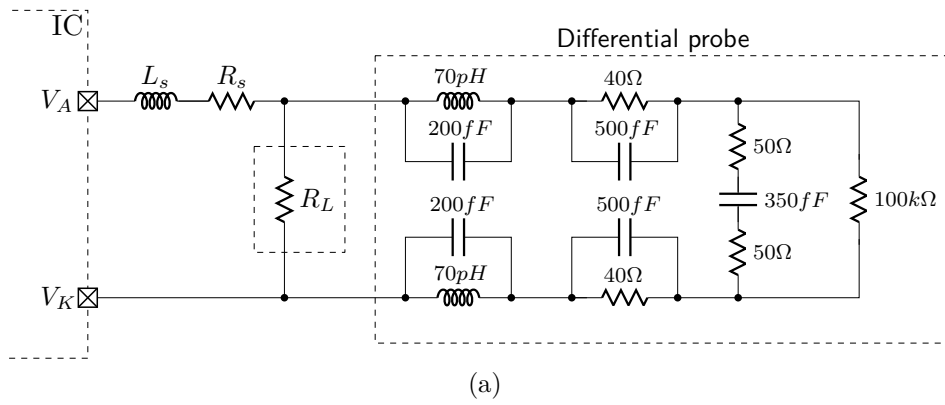


Figure 5.5 – Comparison between measurement and post-layout simulation: (a) equivalent circuit model of the load, (b) electrical waveform.

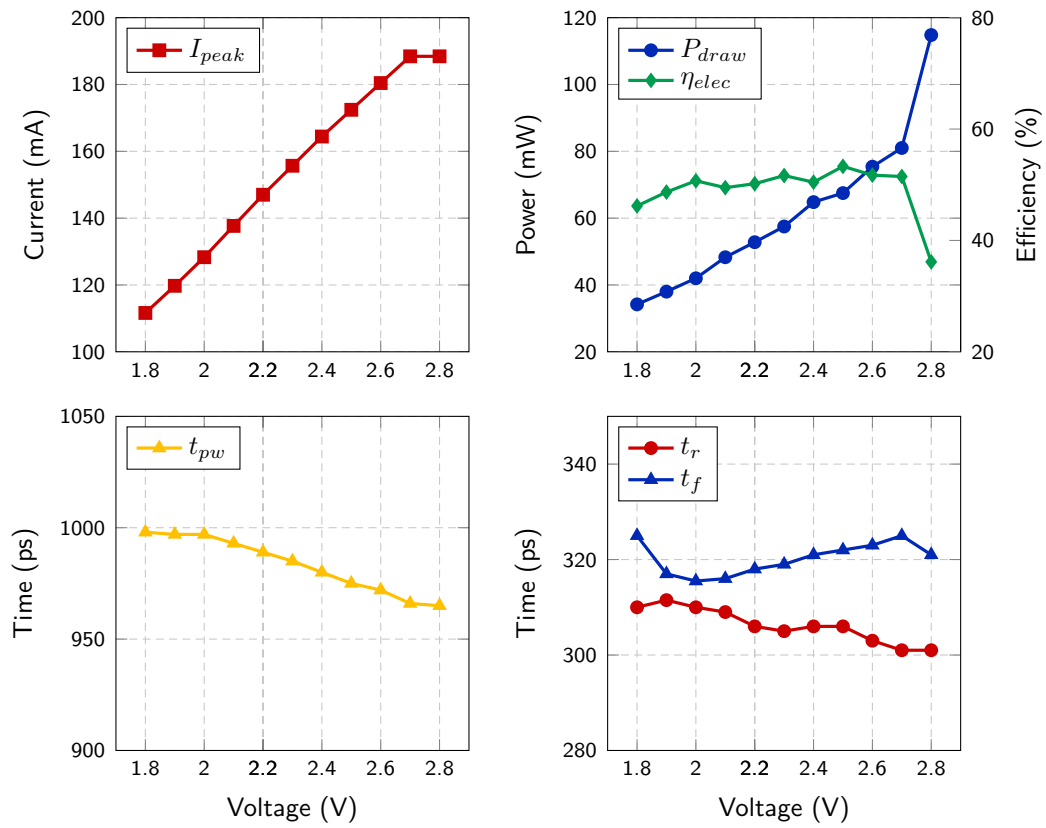


Figure 5.6 – Electrical characterization as a function of the supply voltage ($t_{mod} = 1ns$, $f_{sw} = 100MHz$).

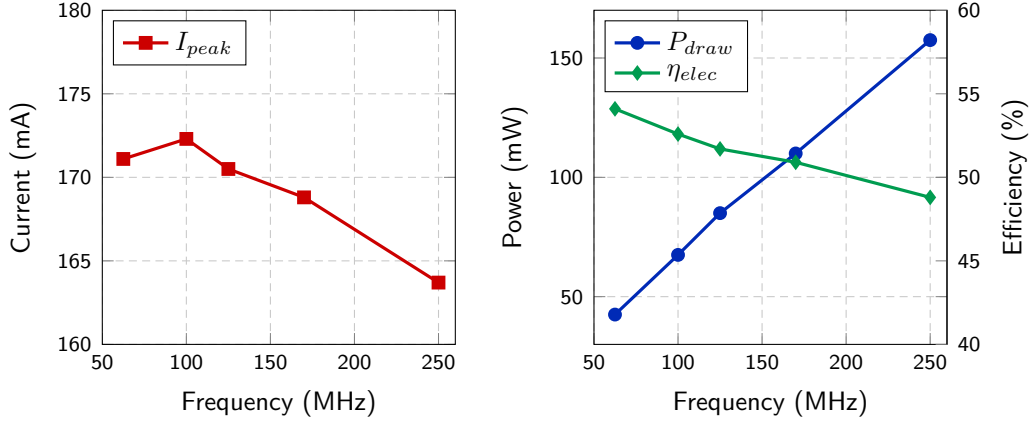


Figure 5.7 – Electrical characterization as a function of the pulse repetition frequency ($V_{DD} = 2.5V$, $t_{mod} = 1ns$).

Figure 5.7 illustrates the behavior of the driver versus the pulse repetition frequency. The latter was swept from $100MHz$ to $250MHz$ whereas the modulation pulse width was kept to $1ns$. The measured data show that the driving current tends to decrease with increasing frequency. This is most likely due to an incomplete charging of the flying capacitor with the augmentation of the duty cycle. In the same manner, the efficiency is slightly reduced because switching losses varies proportionally to frequency. Recall that the gate switching loss P_{sw} of a MOSFET can be expressed by,

$$P_{sw} = C_g V_{gs}^2 f_{sw} \quad (5.4)$$

with C_g being the gate capacitance and V_{gs} the gate-source voltage.

Afterwards, the circuit was characterized for a $500ps$ pulse width and a $250MHz$ frequency (12.5% duty cycle). Figure 5.8 shows the measured electrical waveform. The supply voltage is set to $2.5V$. On the face of it, the available current is substantially reduced as compared to the $1ns$ waveform, with a drop from $172.5mA$ to $148mA$. Here, the most probable hypothesis is that the pulse is terminated before building up. This means that what is being measured is an incomplete pulse due to parasitics in the load path. As illustrated in Figure 5.9, this trend clearly continues with a further decrease of the modulation pulse width. From $750ps$ to $250ps$, both the driving current peak and power efficiency considerably drop.

These observations emphasize that the electrical test setup was not adequate to assess the performances of the driver in sub- ns pulse operation. As a consequence, electrical measurements were not pursued further.

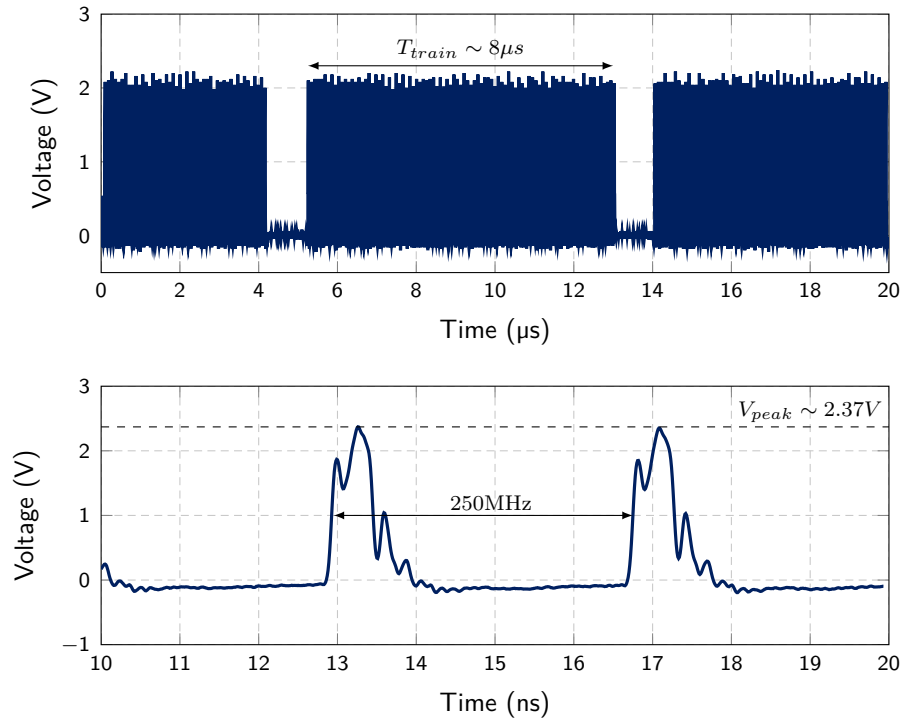


Figure 5.8 – Electrical waveform measurement ($V_{DD} = 2.5V$, $t_{mod} = 500ps$, $f_{sw} = 250MHz$).

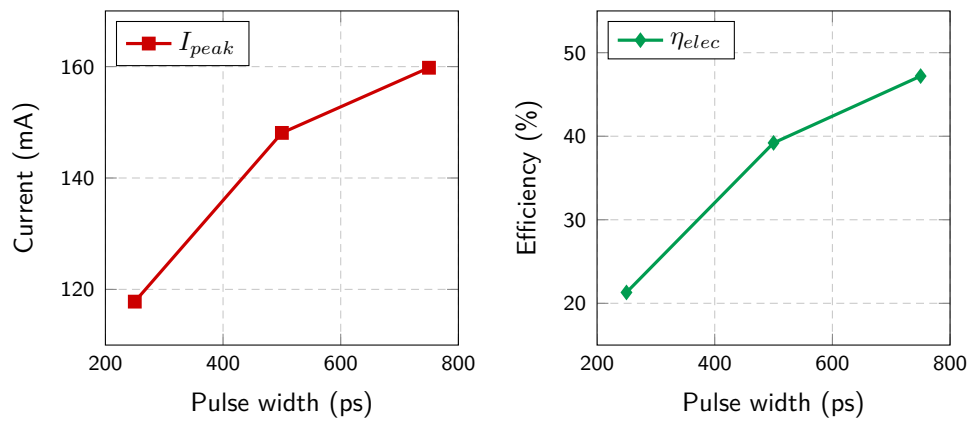


Figure 5.9 – Impact of pulse width on the driver's performances ($V_{DD} = 2.5V$, $f_{sw} = 250MHz$).

5.2.3 Summary

In conclusion, the electrical testing has demonstrated that the fabricated chip is globally functional. There is no critical failure arising from the capacitive voltage boost structure, meaning that the driver is able to produce a load voltage greater than the supply voltage. Furthermore, measured waveforms are consistent with the proposed carrier sweep-out scheme. However, there exist major discrepancies between measurement and PLS results, as recapitulated in Table 5.2. In a nutshell, measured data bring out a significant decrease of the driver's current capability and transient performances as compared to simulation. The most likely hypothesis for such disparities is the circuit parasitics contributed by the test platform (package, PCB and load resistor). As a result, the test setup was considered as inadequate for measuring the driver's performances in sub- ns pulse operation.

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	172.5	222.6	-22.5%
P_{draw} (mW)	67.5	111.7	-39.5%
η_{elec} (%)	53.3	55	-3%
t_{pw} (ps)	975	972	+0.3%
t_r (ps)	306	188	+62%
t_f (ps)	322	94	+242%

Table 5.2 – Summary of the electrical characterization ($V_{DD} = 2.5V$, $t_{mod} = 1ns$, $f_{sw} = 100MHz$).

Testing perspectives obviously include the extraction of the setup's circuit parasitics so as to rigorously compare and correlate measurement and simulation results. Moreover, it could permit to properly identify the root cause of the parasitic ringing seen in the electrical waveform. This has been partly examined by means of scattering parameters measurement, but not carried out due to time restriction. In the end, quality measurements would require an optimally designed characterization PCB.

5.3 Optical verification

The purpose of the optical verification was to test the proposed VCSEL driver in a product-like hardware environment, *i.e.* with the VCSEL array as load.

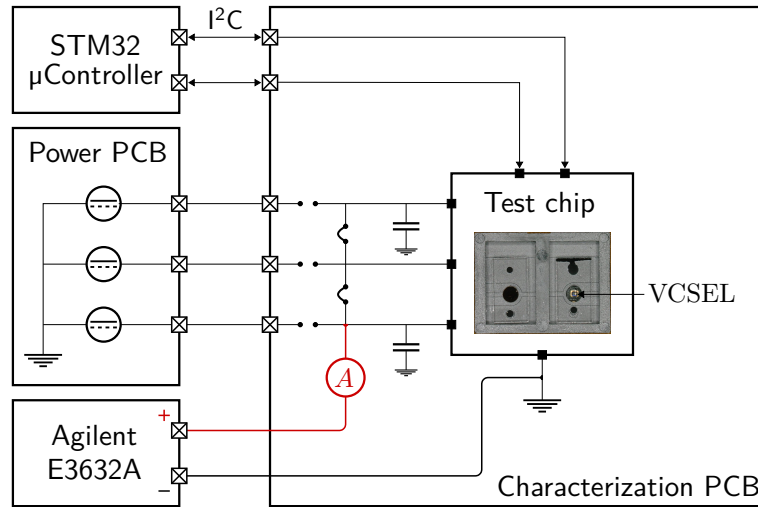


Figure 5.10 – Synoptic of the optical measurement platform.

5.3.1 Test platform

The synoptic of the optical measurement setup is presented in Figure 5.10. The optical module, incorporating the silicon chip and the VCSEL array, was mounted onto an LGA socket. As previously, the test chip was powered externally with an Agilent E3632A in order to monitor the current consumption.

Knowing that the chip does not provide the SPAD-based detector, alternate measurement instruments were used to characterize the circuit. Two different testing were carried out as part of the optical verification:

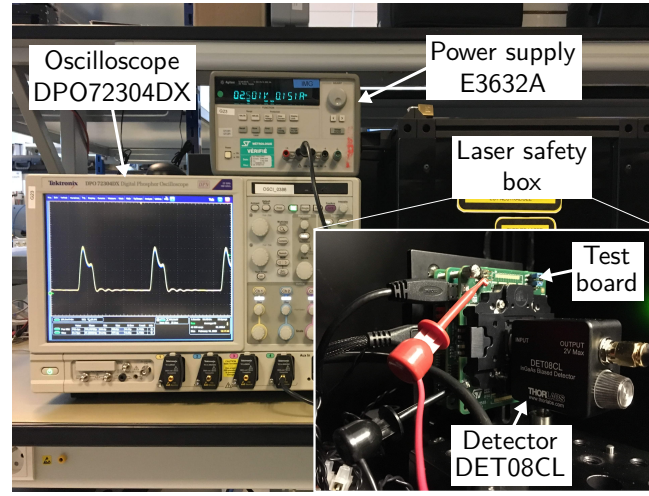
- Laser pulse shape measurement with a high-speed photodetector ($> 1GHz$ bandwidth) for capturing the temporal attributes of the transmitted laser pulse (pulse width, rise time and fall time).
- Laser power measurement with an integrating sphere in order to estimate the driver's current capability and power efficiency.

Note that all these measurements were performed in a laser-safe and dark enclosure.

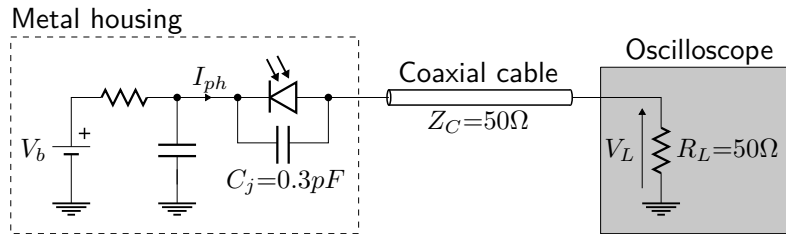
5.3.2 Pulse shape measurements

5.3.2.1 Experimental setup

A photograph of the test bench is presented in Figure 5.11a. So as to capture the laser pulse shape, the module was coupled to a Thorlabs DET08CL free-space photodetector. The latter is basically a $p - n$ photodiode which operates by absorption of photons and generates a current flow proportional to the incident optical power. The DET08CL is designed to function in the photoconductive mode (in opposition to the photovoltaic mode), meaning that the photodiode is reverse-biased. The key benefit of such a mode of operation



(a)



(b)

Figure 5.11 – Laser pulse shape measurement setup: (a) photograph of the test bench, (b) equivalent circuit of the receiver channel.

is that the width of the depletion region is increased. As a result, the parasitic junction capacitance is lowered, thus improving the detector's frequency response [107]. The DET08CL is based on indium gallium arsenide (InGaAs) alloy and exhibits a responsivity of approximately 0.6 A/W at 940 nm .

The photodetector was connected to a Tektronix DPO72304DX oscilloscope (23 GHz bandwidth, 100 GS/s) via a 50Ω coaxial cable with sub-miniature A (SMA) connectors. Generally speaking, SMA connectors operate properly up to 24 GHz [108]. Last but not least, the oscilloscope was set up with a 50Ω terminating resistance in order to guarantee impedance matching and prevent ringing.

It is worth noting that given the small beam divergence ($\sim 25^\circ$) of the VCSEL array, the setup is very sensitive to the optical alignment between the module and the detector. Accordingly, the mechanical support of the DET08CL was gradually adjusted until sufficient light detection. The alignment was then kept stable during the whole experiment. Even though some optical losses might be expected due to the manual coupling, the goal was only to capture the time features of the laser waveform.

The electrical equivalent circuit of the photodetector channel is shown in

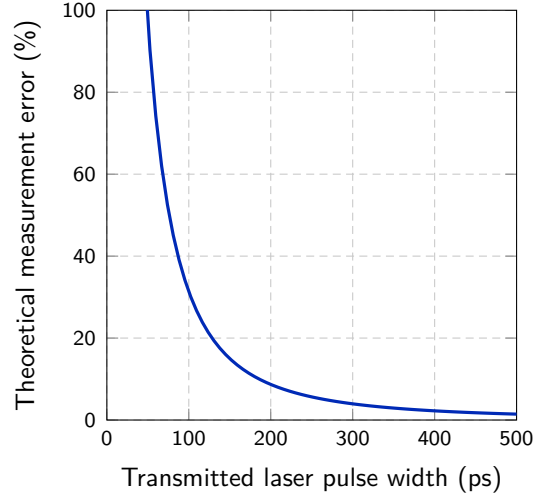


Figure 5.12 – Measurement error versus laser pulse width.

Figure 5.11b. The corresponding transfer function $\frac{V_L}{I_{ph}}$ can be expressed as,

$$\frac{V_L}{I_{ph}} = \frac{R_L}{1 + (Z_C + R_L)C_j s} \rightarrow \begin{cases} f_{det} = \frac{1}{2\pi(Z_C + R_L)C_j} \approx 5.3GHz \\ t_{det} = \frac{0.44}{f_{det}} \approx 83ps \end{cases} \quad (5.5)$$

The bandwidth f_{det} and impulse response width t_{det} of the detector are respectively calculated to $5.3GHz$ and $83ps$ [109].

The temporal characteristics of the laser pulse shape were directly measured using the oscilloscope's functionalities. It is important to keep in mind that the signal observed is the result of the convolution between the intrinsic laser pulse shape and the instruments' impulse response. Thus, the measured pulse width t_{opt} can be approximated by,

$$t_{opt} = \sqrt{t_{laser}^2 + t_{det}^2 + t_{scope}^2} \quad (5.6)$$

where t_{laser} is the transmitted laser pulse width and t_{scope} is the impulse response width of the oscilloscope [109]. Therefore, the test equipment leads to an unavoidable measurement error which is illustrated in Figure 5.12 as a function of t_{laser} .

5.3.2.2 Measurements

Figure 5.13 shows the laser waveform measured for a $1ns$ pulse width and a $100MHz$ frequency (10% duty cycle). The supply voltage was set to $2.5V$. The starting spike of the pulse clearly matches the gain-switching behavior of a

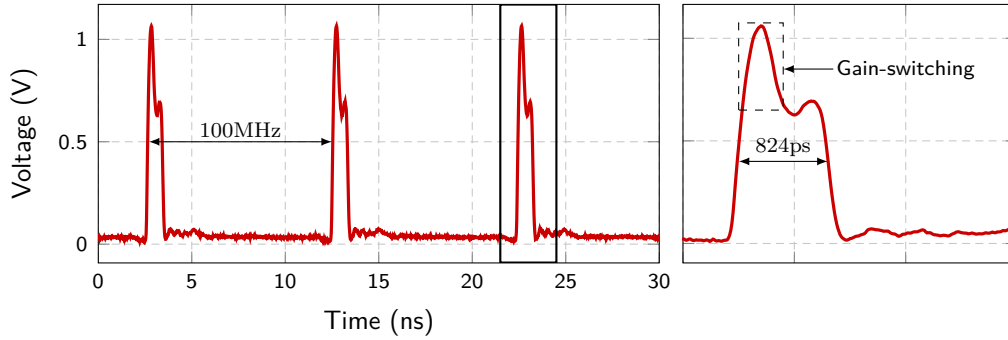


Figure 5.13 – Laser pulse shape measurement ($V_{DD} = 2.5V$, $t_{mod} = 1ns$, $f_{sw} = 100MHz$).

laser diode. Recall that gain-switching is an intrinsic relaxation phenomenon which occurs when the pumping current exceeds the laser threshold. The measured laser pulse duration is $824ps$. The time distortion between the set and measured pulse width is expected as any laser diode exhibits an inherent turn-on delay. Under the assumption of a $1ns$ driving current waveform, the turn-on delay is calculated at approximately $180ps$. Here, a particularly important result in comparison with the electrical characterization is that there is no parasitic ringing in the laser pulse's transient edges. Thus, relatively sharp edges are demonstrated, with measured rise and fall times of $165ps$ and $115ps$, respectively.

However, one can see that the measured waveform is non zero even in the absence of light excitation. This phenomenon was investigated in detail in order to reject the VCSEL or the driver as possible root causes. Given that it was also observed on a STMicroelectronics' reference product, the focus was put on the photodetector. Consequently, a second InGaAs free-space detector, the iChaus iC212 ($1GHz$ bandwidth), was employed to capture the laser pulse in the same experimental conditions. As shown in Figure 5.14, comparing the measured laser pulses clearly indicates that the light offset is primarily an artefact of the DET08CL.

The foremost hypothesis explaining such a phenomenon is the diffusion current in a $p - n$ photodiode. Referring to Figure 5.15, carriers generated within one diffusion length of the depletion region can potentially diffuse into the high-field region. Since the diffusion time of carriers may be greater than several microseconds, a slow tail can be produced in the photodetector's response [110, 111]. When pulsing at a high repetition rate, such a diffusion tail can eventually results in a constant offset in the signal coming out of the detector. Here, carrier diffusion does not seem to impact the laser pulse shape, meaning that the pulse's temporal characteristics could still be measured with acceptable accuracy. Therefore, the DET08CL was kept for pursuing measurements due to its higher bandwidth as compared to the iC212.

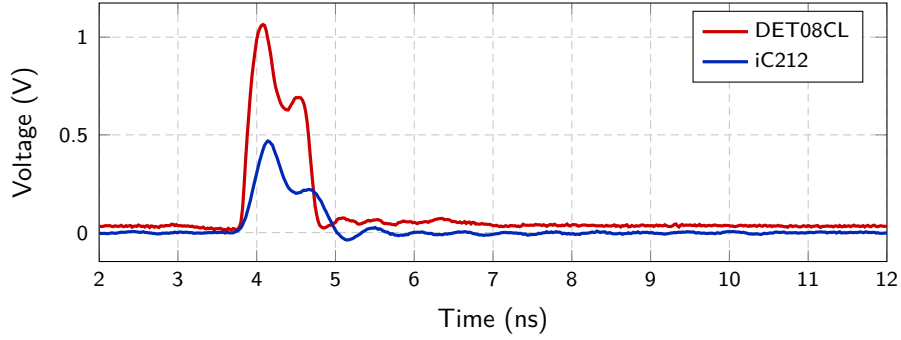


Figure 5.14 – Laser pulse waveforms captured with the DET08CL (red) and iC212 (blue) photodetectors.

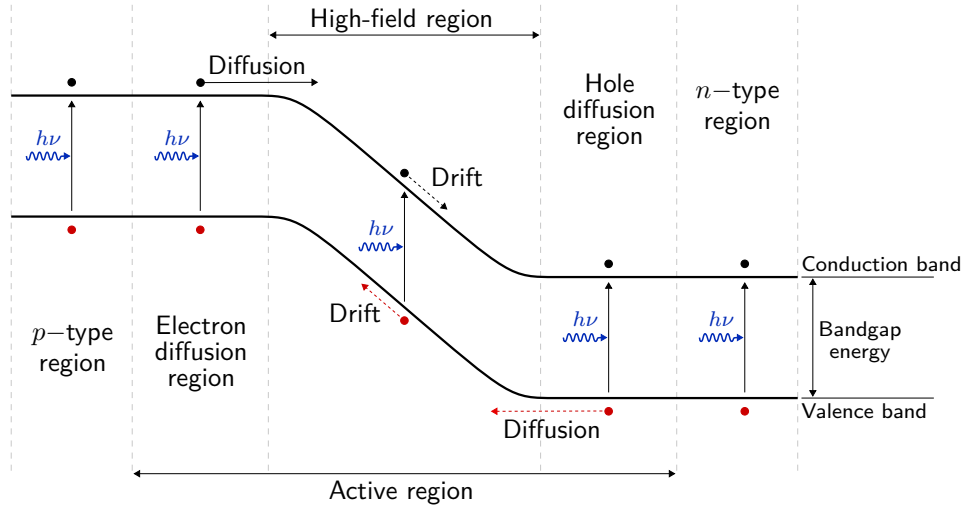


Figure 5.15 – Energy band diagram of a photoexcited $p-n$ photodiode.

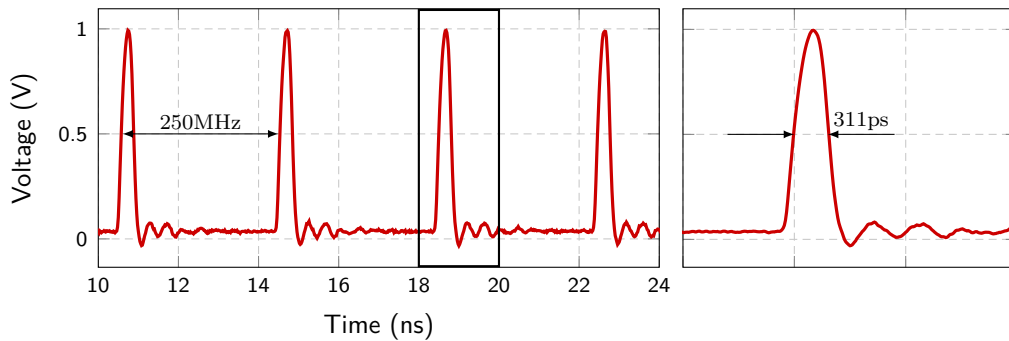


Figure 5.16 – Laser pulse shape measurement ($V_{DD} = 2.5V$, $t_{mod} = 500ps$, $f_{sw} = 250MHz$).

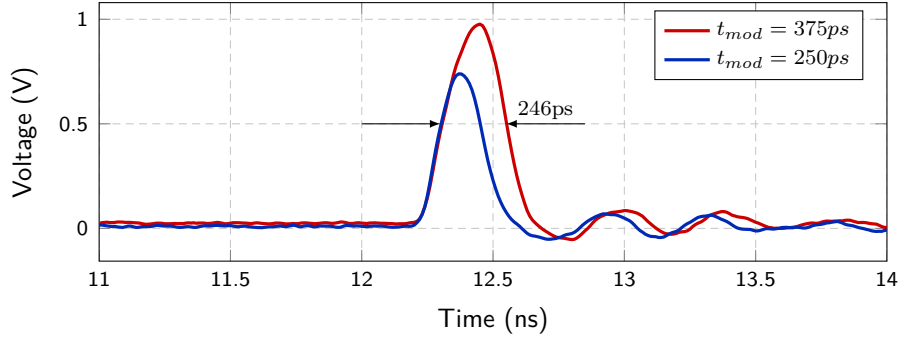


Figure 5.17 – Sub-500ps laser pulse shape measurement ($V_{DD} = 2.5V$, $f_{sw} = 250MHz$).

Figure 5.16 depicts the laser waveform measured for a modulation pulse width of 500ps, a frequency of 250MHz (12.5% duty cycle) and a supply voltage of 2.5V. In such a case, the laser pulse shape is mainly defined by the gain-switching spike with a measured pulse width of 311ps. This means that the laser driving current pulse is terminated directly after the first spike of the VCSEL's relaxation oscillation. Once again, a light offset is clearly seen in the pulse train. What is more, the ringing seen after the pulse's falling edge is probably due to the detector. Indeed, referring to the DET08CL's user manual, the detector can exhibit an after-pulse ringing up to 20% of the maximum [107]. The measured rise time is 163ps, which is similar to the 1ns waveform. In contrast, the measured fall time is slightly increased to 145ps because the laser pulse is terminated in the gain-switching overshoot.

The measured sub-500ps pulse operation of the driver is represented in Figure 5.17. Setting the pulse width to 375ps results in an approximately 246ps laser pulse. Below 375ps, a degradation of the signal coming out of the detector can be observed. Indeed, with a pulse width setting of 250ps, the measured laser pulse width is 191ps and the signal drop can be clearly noticed. This issue is discussed in the upcoming part which covers power measurements.

Figure 5.18 summarizes the laser pulse duration measurement as a function of the supply voltage. One can see that the pulse width is relatively constant within the voltage range.

As already explained, the measurement by means of a high-speed photodetector only permits to capture the timing characteristics of the laser pulse. Therefore, the focus of the upcoming part is the measurement of the related optical power.

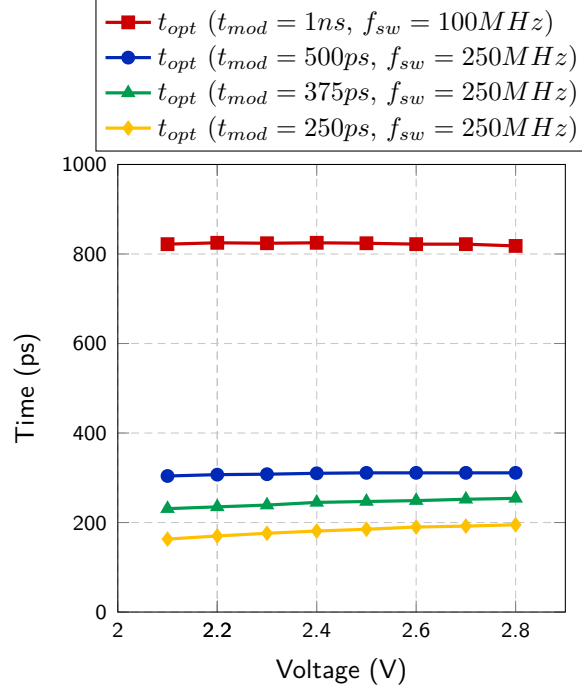


Figure 5.18 – Laser pulse width measurement in different use conditions.

5.3.3 Power measurements

5.3.3.1 Experimental setup

The measurement of the laser power was performed with a Newport 919-SL-5.3-CAL2 integrating sphere coupled to a silicon-based detector. A schematic drawing of the experimental setup is shown in Figure 5.19a. The integrating sphere is a hollow apparatus with a light scattering inner coating. In this way, it enables collection and spatial integration of the incident light. Within the sphere, the radiation goes through multiple reflections and tends to be uniformly distributed at the sphere's inner surface [112]. After a while, the detector will receive uniform irradiance, thus permitting to measure the average optical power.

Measuring the power $P_{opt,avg}$ lets us derive the driver's peak current and power efficiency. For this purpose, the laser waveform was assumed to be an ideal square wave with constant pulse energy. Referring to Figure 5.19b, the laser driving current peak can be expressed as,

$$I_{peak} = \frac{P_{opt,avg}}{\eta \times \alpha_{train} \times f_{sw} \times t_{opt}} + I_{th} \quad (5.7)$$

where α_{train} is the duty cycle of the laser pulse train and f_{sw} and t_{opt} are respectively the frequency and width of the laser waveform measured with the DET08CL detector. Note that α_{train} is a constant equal to 88.8% set

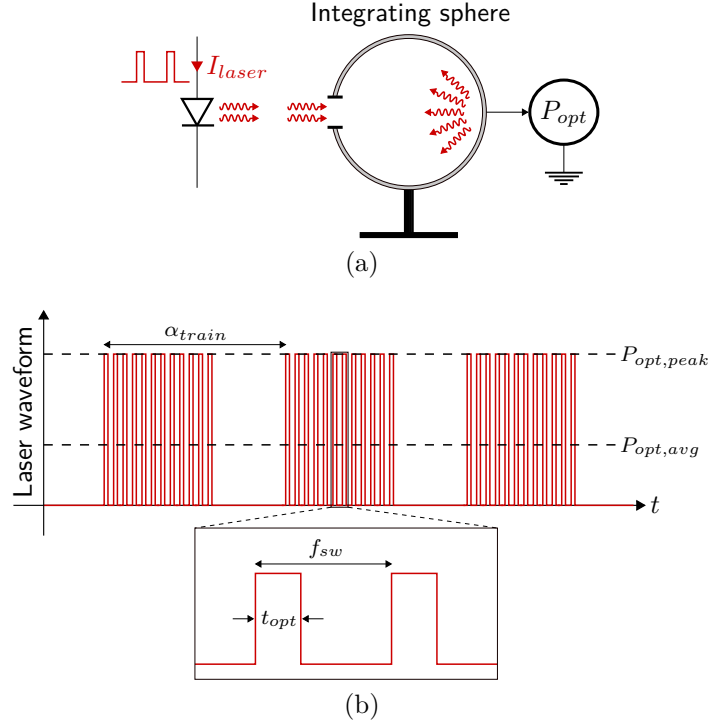


Figure 5.19 – Laser power measurement setup: (a) schematic drawing, (b) timing diagram with quantities of interest.

via the Python script. On the other hand, η and I_{th} are the VCSEL's slope efficiency and threshold current, respectively. It is important to keep in mind that both of these parameters are temperature-dependent. Yet, given that it was not possible to monitor the VCSEL's operating temperature, typical values were exploited, *i.e.* $\eta = 80\%$ and $I_{th} = 15mA$. As a consequence, a current capability of $200mA$ matches a $148mW$ peak optical power.

The power efficiency of the driver is calculated from the VCSEL's wall-plug efficiency WPE ,

$$\eta_{elec} = \frac{P_{opt,avg}}{WPE \times P_{draw}} \quad (5.8)$$

The wall-plug efficiency is expressed as the ratio between the optical power P_{opt} and the electrical power of the laser diode [65].

$$WPE = \frac{P_{opt}}{V_{laser} I_{laser}} = \frac{\eta(I_{laser} - I_{th})}{(R_m I_{laser} + V_{on}) I_{laser}} \quad (5.9)$$

Recall that $R_m \sim 8.3\Omega$ and $V_{on} \sim 1.5V$ are respectively the VCSEL's series resistance and lasing voltage curve-fitted at room temperature. The wall-plug efficiency curve extrapolated for the calculation of the driver's power efficiency is represented in Figure 5.20. Again, since this curve is computed for fixed values of η , I_{th} and R_m , the temperature dependence of the VCSEL was not

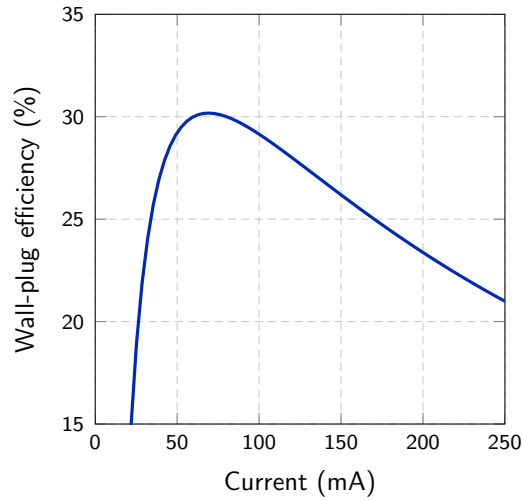


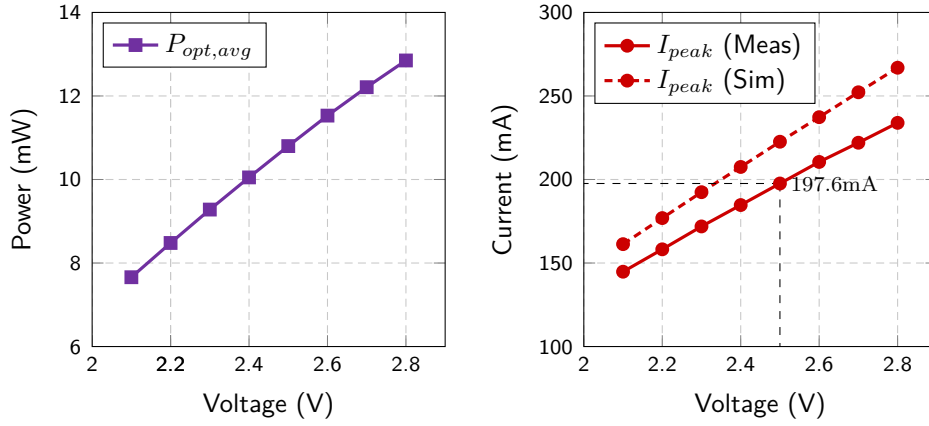
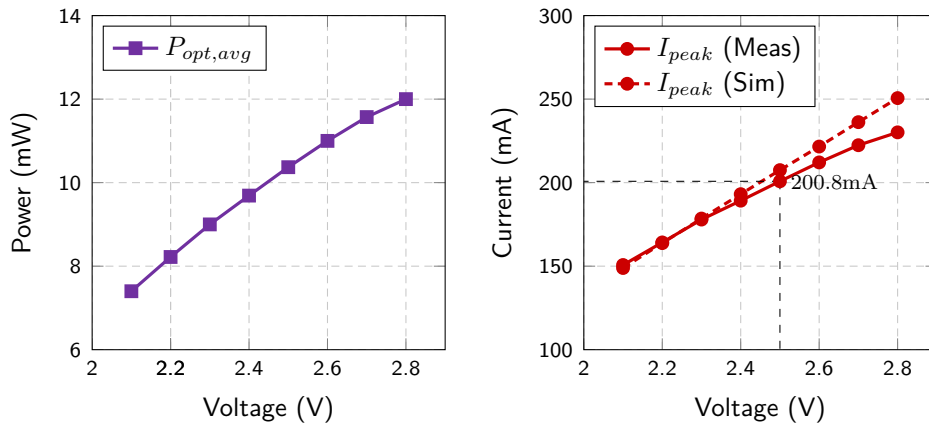
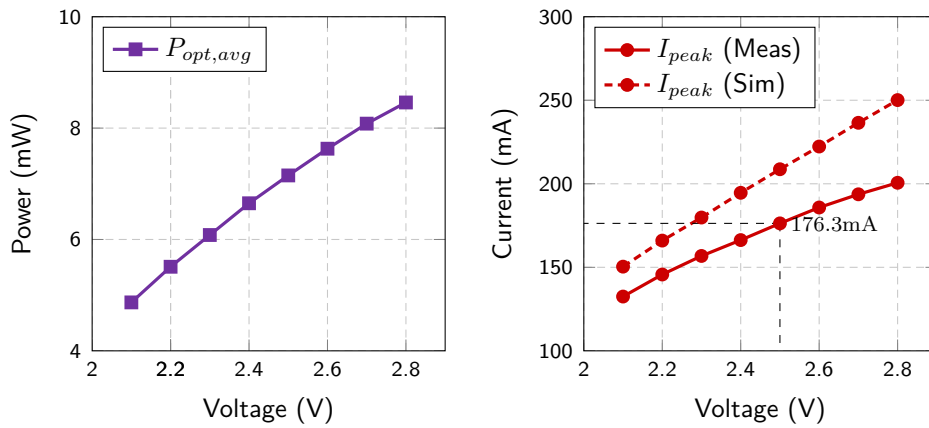
Figure 5.20 – Wall-plug efficiency of the VCSEL array calculated for $\eta = 80\%$ and $I_{th} = 15mA$.

taken into account (such as the non-linear thermal rollover phenomenon).

5.3.3.2 Measurements

Prior to presenting measurement data, it is important to recall that the uncertainty of the results lies in the fact that the calculation was based on an ideal square wave (which is not the case in practice) and that the VCSEL's temperature dependence was not captured. With a constant pumping current, both η and WPE will tend to decrease with increasing temperature. Thus, data must be regarded and discussed with care.

Figure 5.21 illustrates the measured average optical power together with the driving current peak calculation. Data are presented as a function of the supply voltage, from $2.1V$ to $2.8V$, and are compared to post-layout simulation. As observed during electrical characterization, the average optical power, and thus the driving current peak, increases almost linearly with voltage. For a pulse width greater than or equal to $500ps$, there is a relatively good agreement between measurement and simulation with a disparity less than 15% . In addition, a peak current of approximately $200mA$ is demonstrated at a voltage of $2.5V$, thus meeting the design target. However, below $500ps$, there is a significant discrepancy which tends to increase with decreasing pulse width. For a $375ps$ pulse width, achieving the $200mA$ targeted current calls for a supply voltage increment up to $2.8V$. A similar behavior was noticed with current pulse probing, meaning that this is not related to the VCSEL. The most likely explanation is that the peak current is limited because the driving current pulse is terminated prior to fully build up. Simulation results depict the same trend, but in a lesser degree. This means that parasitics' values


(a) Settings: $t_{mod} = 1ns$ and $f_{sw} = 100MHz$.

(b) Settings: $t_{mod} = 500ps$ and $f_{sw} = 250MHz$.

(c) Settings: $t_{mod} = 375ps$ and $f_{sw} = 250MHz$.

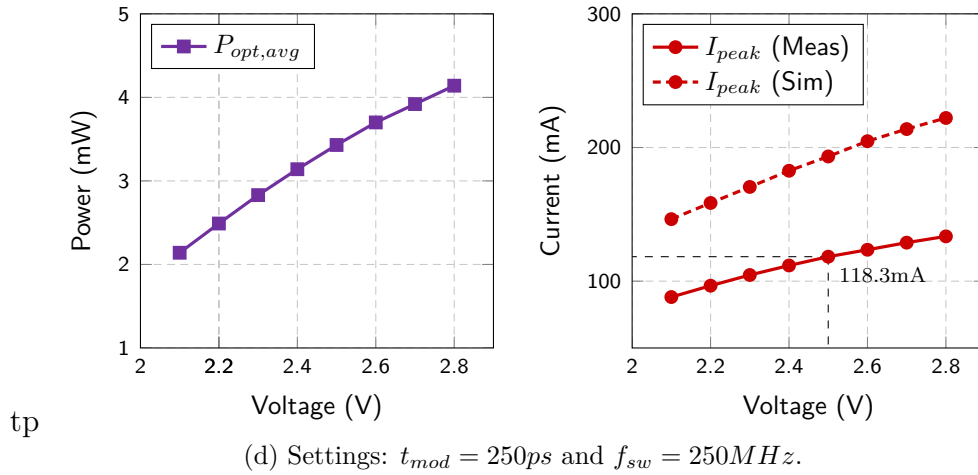


Figure 5.21 – Optical power measurement data and driving current peak calculation as a function of the supply voltage.

theoretically calculated in [Chapter 3](#) and exploited for circuit design represent an optimistic scenario. Furthermore, referring to [Figure 5.12](#), it should be noted that a supplementary measurement error is contributed when measuring sub- $500ps$ pulses due to the uncertainty on the laser pulse width t_{opt} . This error arises from the limited bandwidth of the pulse shape measurement setup.

[Figure 5.22](#) represents the impact of the pulse repetition frequency and duty cycle on the driving current peak. Measurement data highlight that the current decreases with increasing frequency, which is consistent with the behavior already observed with electrical testing. This significant drop is likely to result from an incomplete charging of the flying capacitor. What is more, a non-negligible calculation error might be contributed due to the VCSEL's self-heating. As a matter fact, the operating temperature of the VCSEL will tend to increase with increasing duty cycle. Hence, the value of the parameters employed for calculating the peak current might be substantially overestimated.

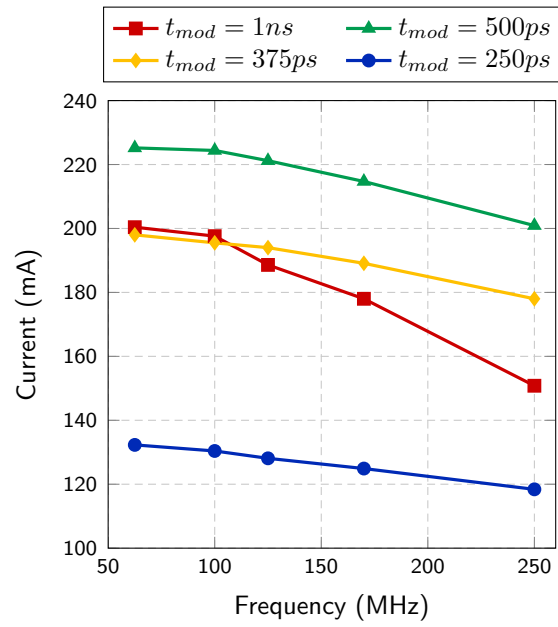
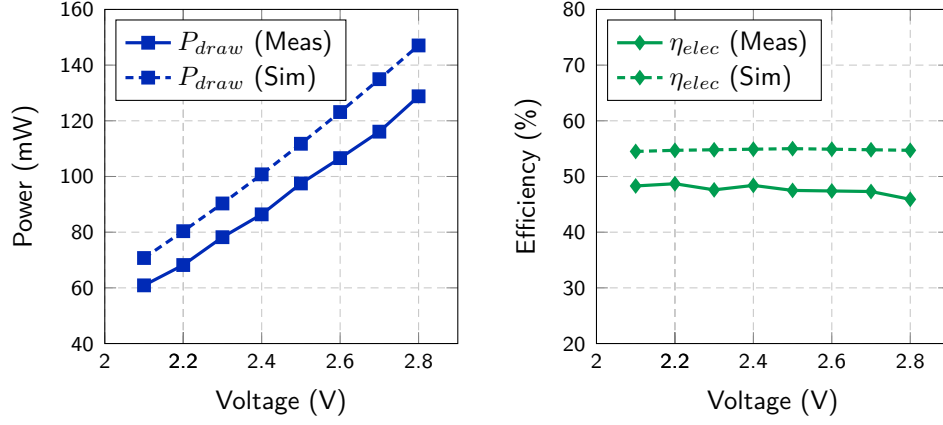
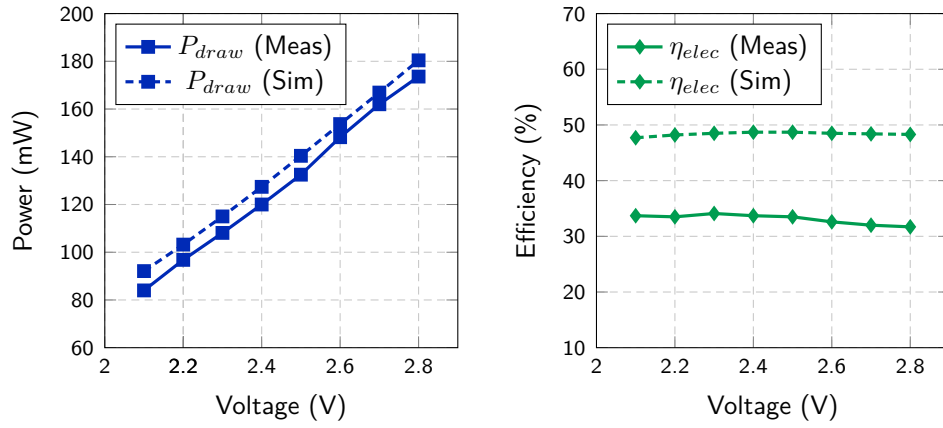
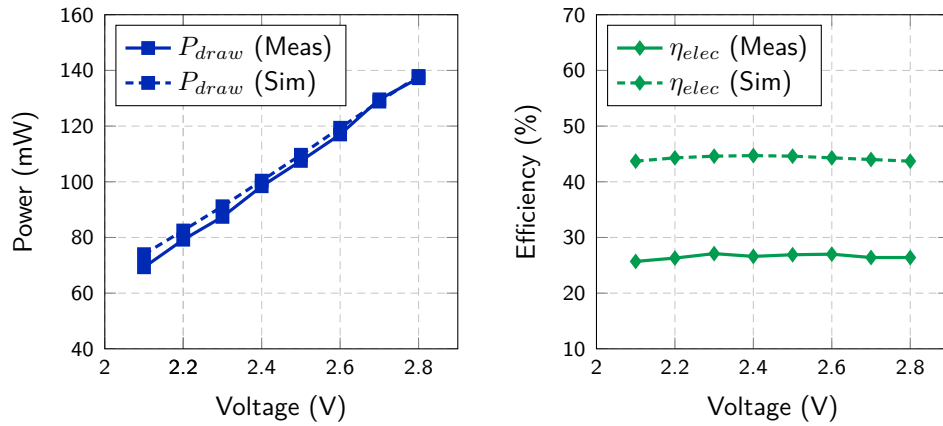
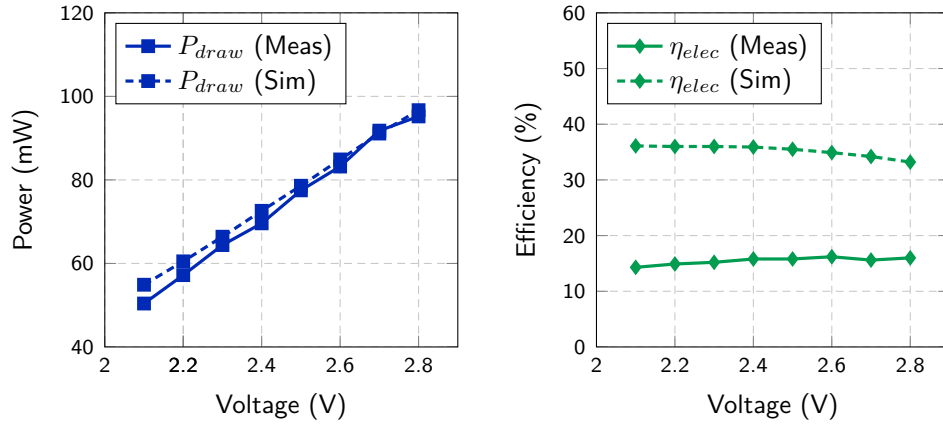


Figure 5.22 – Calculated driving current peak as a function of the pulse repetition frequency ($V_{DD} = 2.5V$).

The measured power consumption as well as the calculated efficiency of the driver are presented as a function of the supply voltage in Figure 5.23. Recall that efficiency data were computed at a given current based on the VCSEL's wall-plug efficiency curve depicted in Figure 5.20. On the face of it, the measured driver's power consumption corresponds quite favorably to simulation. However, there are large disparities regarding efficiency, in particular when decreasing pulse width. Additionally, the value computed for the first use conditions ($t_{mod} = 1ns$ and $f_{sw} = 100MHz$) is not aligned with the one measured via electrical characterization, *i.e.* 53.3%. A possible explanation is that power losses in the circuit are globally higher than expected. It must also be kept in mind that a calculation error is inherently introduced. Indeed, since the WPE was extrapolated with typical parameters, the self-heating of the VCSEL in pulse operation is not taken into account. As a result, the WPE figure could be overestimated, which in turn may lead to an underestimation of the driver's power efficiency.

Figure 5.24 represents the impact of the pulse repetition frequency and duty cycle on power efficiency. As expected, efficiency decreases roughly linearly with increasing switching frequency.

(a) Settings: $t_{mod} = 1ns$ and $f_{sw} = 100MHz$.(b) Settings: $t_{mod} = 500ps$ and $f_{sw} = 250MHz$.(c) Settings: $t_{mod} = 375ps$ and $f_{sw} = 250MHz$.



(d) Settings: $t_{mod} = 250ps$ and $f_{sw} = 250MHz$.

Figure 5.23 – Power consumption measurement and efficiency calculation as a function of the supply voltage.

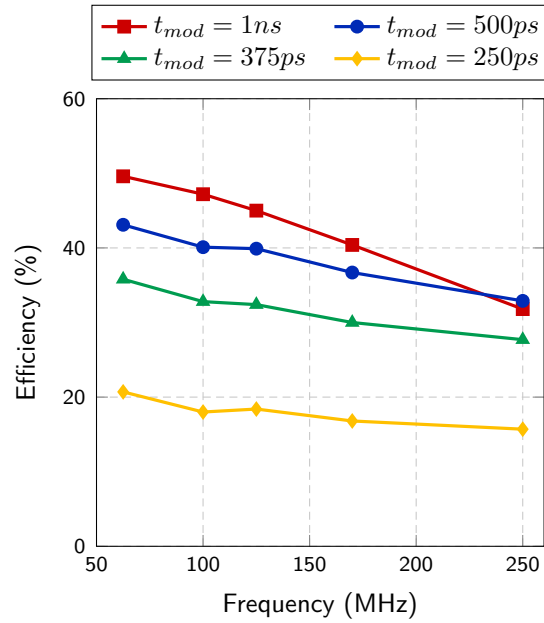


Figure 5.24 – Calculated power efficiency as a function of the pulse repetition frequency ($V_{DD} = 2.5V$).

5.3.4 Summary

Generally speaking, the fabricated chip demonstrates satisfactory performances. These are summarized in Table 5.3 for a typical 2.5V supply voltage. The circuit is capable of generating sub- ns laser pulses with fast transient edges, in the order of $100ps$. The corresponding driving current peak has been calculated at $200mA$. As a result, the typical specification regarding driving capability is met. However, the sub- $500ps$ pulse operation of the driver is limited. As a matter of fact, one can observe major peak current disparities between measurement and simulation results, up to 38.8%. These are probably due to circuit parasitics arising from the module interconnect which have been optimistically calculated for circuit design. Thus, future improvements should be directed towards optimizing the physical interconnect between the driver chip and the VCSEL. Concerning power consumption, there is a good agreement between measurement and simulation. Yet, calculated power efficiency figures do not match simulated values. Moreover, the 47% targeted value is not respected when reducing the modulation pulse width below $1ns$. Obviously, it should be kept in mind that the efficiency calculation is uncertain since it is based on extrapolated VCSEL data.

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	197.6	222.6	-11.2%
P_{draw} (mW)	97.5	111.7	-12.7%
η_{elec} (%)	47.5	55	-13.6%
t_{opt} (ps)	824	—	—

(a) Settings: $V_{DD} = 2.5V$, $t_{mod} = 1ns$ and $f_{sw} = 100MHz$.

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	200.8	207.6	-3.2%
P_{draw} (mW)	132.5	140	-5.3%
η_{elec} (%)	33.5	48.7	-31.2%
t_{opt} (ps)	311	—	—

(b) Settings: $V_{DD} = 2.5V$, $t_{mod} = 500ps$ and $f_{sw} = 250MHz$.

Parameter	Measurement	PLS	Variation
I_{peak} (mA)	118.3	193.3	-38.8%
P_{draw} (mW)	77.5	78.6	-1.3%
η_{elec} (%)	15.8	35.5	-55.4%
t_{opt} (ps)	191	—	—

(c) Settings: $V_{DD} = 2.5V$, $t_{mod} = 250ps$ and $f_{sw} = 250MHz$.

Table 5.3 – Summary of the optical characterization.

There are multiple axis for improvement of the optical experimental setup. Yet, these were not pursued due to the time restriction of the doctoral project.

First and foremost, additional measurements must be performed in order to characterize the VCSEL's parameters as a function of temperature. This should allow to improve the calculation accuracy of the peak current and power efficiency data. Then, regarding laser pulse shape measurements, the set up of a more complete and effective optical test bench should permit to remove the DET08CL's artefact. As a matter of fact, since the light offset in the laser waveform was assumed to arise from carrier generation outside of the detector's photosensitive area, a possible workaround is to couple the detector with a focusing lens. An alternative approach for cancelling the light offset, which was investigated at the end of the project, was to use a $12GHz$ optical fiber-coupled photodetector (Newport 1544-A). This solution could also ameliorate the setup's bandwidth. Another improvement would be to enable joint monitoring of the laser pulse shape as well as the corresponding driving electrical waveform.

Last but not least, the driver should be tested as part of a time-of-flight system, *i.e.* together with the SPAD-based detector. This would, among other, allow to assess the impact of the proposed carrier sweep-out scheme on distance measurement accuracy.

6 General conclusion

The objective of the present thesis was to develop a laser diode driver for direct time-of-flight rangefinding in consumer portable devices. As for any circuit development, the project was carried out from feasibility through to design and experimental characterization. The aim of this final chapter is to review the main achievements of the thesis as well as to highlight perspectives.

6.1 Summary of contributions

Prior to going through the contributions of this thesis, it is important to restate the main electrical specifications of the design target. The key focus was to demonstrate the feasibility of sub- ns laser pulse operation at high repetition frequency, up to several hundreds of megahertz. Moreover, the major challenging and antagonistic requirements are the increase of the driving current capability up to $200mA$ and the lowering of the supply voltage down to $2.5V$. Last, a power efficiency of 47% was targeted.

The first step was to set a classification of laser diode driver topologies dedicated to time-of-flight applications (see [Chapter 2](#)). The existing architectures have been grouped into three main categories:

- The resonant capacitive discharge (RCD) laser diode driver.
- The current-mode (CM) laser diode driver.
- The voltage-mode (VM) laser diode driver.

These have been evaluated in regards to supply voltage demand, transient speed and power efficiency. As a result of a feasibility study carried out in [Chapter 3](#), the voltage-mode topology has been highlighted as the best possible compromise between current capability and power efficiency while being compliant with low-voltage functioning. Thus, it was chosen to head towards a modified voltage-mode structure to meet the technical specifications.

The proposed laser diode driver circuit architecture is shown in [Figure 6.1](#), with V_{mod} (pulse width t_{mod} and frequency f_{sw}) being the modulation signal of the laser. The circuit's operation is based on repeated charging and discharging cycles of a flying capacitor C_{fly} , combined with a capacitive voltage boost

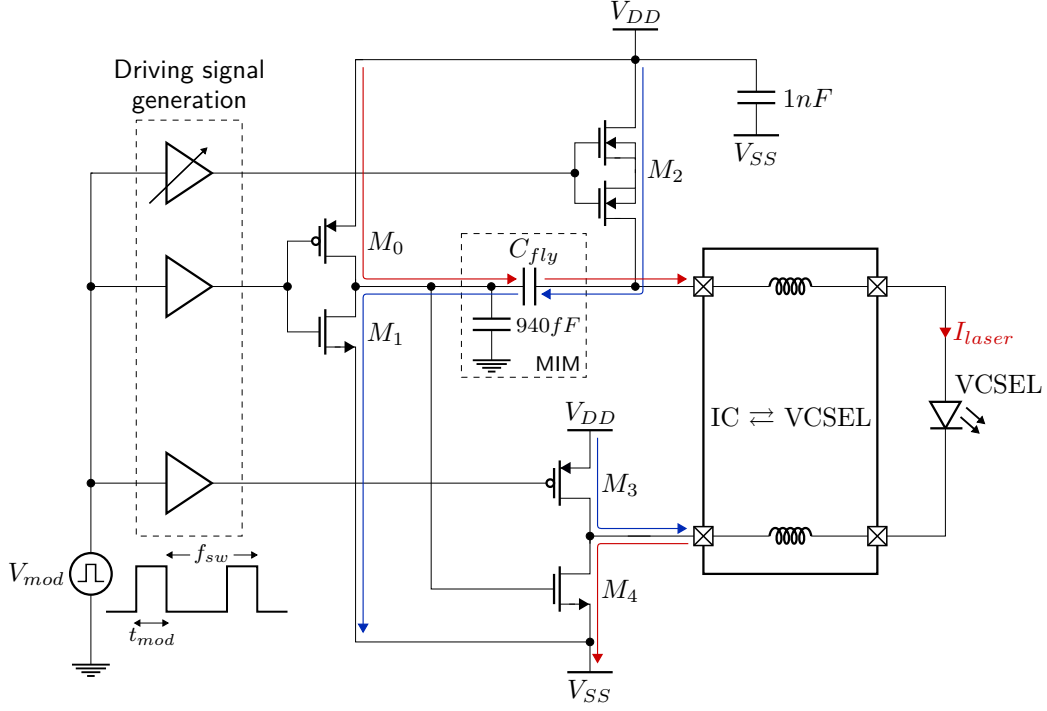


Figure 6.1 – Schematic diagram of the designed laser diode driver circuit.

structure. During a first operating phase, C_{fly} is charged to V_{DD} through NMOS M_2 and NMOS M_1 . Then, PMOS M_0 and NMOS M_4 are turned on so as to create a discharging path for C_{fly} through the laser diode. Given that PMOS M_0 pushes the bottom plate of C_{fly} to V_{DD} , the load voltage is boosted, thus increasing the driver's current capability. Such a design permits to overcome the 2.5V supply voltage constraint. Moreover, a carrier sweep-out circuit feature has been suggested to remove any optical tailing or secondary pulsations in the laser pulse's turn-off transient, which is critical for direct time-of-flight rangefinding. This feature is provided by PMOS M_3 connected between V_{DD} and the VCSEL's cathode node. Simply put, M_3 permits to force a reverse voltage across the load during the off time of the VCSEL.

The driver's design methodology is detailed in [Chapter 4](#). The circuit has been fully implemented on-chip in the 40nm CMOS technology within a previously developed TOF sensor of STMicroelectronics. The main building blocks that have been designed are the power stage, composed of the power MOSFETs and the flying capacitor, as well as the driving signals' generation circuits, *i.e.* the pre-drivers (chain of scaled inverters) and the level-shifter (see [Figure 6.1](#)). The flying capacitor has been realized with a 178pF MIM device due to its superior capacitive density and reduced bottom plate parasitic capacitance as compared to MOS or MOM capacitor structures. The dimensioning of the power MOSFETs' channel width (M_0 , M_1 , M_2 and M_4) has been performed according to a trade-off analysis between current capability, power efficiency,

repetition frequency and silicon area. On the other hand, PMOS M_3 must act as a low-impedance pull-up resistor and has been sized with the largest possible channel width. In addition, a $1nF$ on-chip decoupling capacitor has been connected between the power supply and ground pins of the circuit, V_{DD} and V_{SS} . The latter has been realized by MOS and MIM devices which have been arranged in a stacked structure.

The post-layout verification of the circuit has brought out satisfactory results with a $207.8mA$ driving current peak and a 48.7% power efficiency in the typical operating mode ($V_{DD} = 2.5V$, $t_{mod} = 500ps$, $f_{sw} = 250MHz$). Yet, some limitations have been highlighted when setting the pulse width down to $250ps$. These are most probably due to the parasitic inductance in the current path through the VCSEL.

The experimental characterization of the fabricated test chip is outlined in [Chapter 5](#). The functioning, performances and limitations of the driver have been assessed via electrical and optical measurements. It has been shown that the proposed topology demonstrates superior performances in comparison with former driver developement by STMicroelectronics. Indeed, the driver is capable of generating a driving current up to $200.8mA$ while being operated at a $2.5V$ supply voltage and a $250MHz$ repetition frequency. This corresponds to the measurement of a $311ps$ laser pulse with rise and fall times in the order of $100ps$. However, only a 33.5% power efficiency has been measured in these operating conditions (in contrast to the 48.7% computed from simulation). Furthermore, the circuit's current capability is limited in sub- $500ps$ pulse operation, most likely due to parasitic inductance. This points out that future design improvements should be directed towards optimizing the physical interconnect between the driver and the VCSEL.

Table [6.1](#) compares in details the performance of the proposed laser diode driver topology to the existing literature. This work demonstrates the feasibility of sub- ns laser pulse, down to $191ps$, at a repetition rate of $250MHz$, which is the highest frequency performance reported. Thanks to the capacitive voltage boost principle, the proposed driver architecture enables to apply a laser diode forward voltage above the supply voltage. As a result, this work demonstrates the lowest supply voltage reported, *i.e.* $2.5V$. Moreover, an efficiency of up to 47.5% is achieved, which is a good result in comparison with the literature. Finally, this work is consistent with the concept of technology scaling with an implementation in a $40nm$ CMOS process.

In short, the achievements of this thesis represent an important step forward in regards to the current state-of-the-art as well as for future product development by STMicroelectronics.

Ref.	V_{in} / V_{DD} (V)	I_{peak} (A)	t_{pw} (ns)	t_{opt} (ns)	η_{elec} (%)	f_{sw} (MHz)	Topology	Implementation
[43]	5	~ 1	~ 3	2.4 – 4.7	—	0.01	RCD	0.35 μm CMOS
[44]	50	~ 4	~ 2	1.5	—	—	RCD	0.35 μm 50V CMOS
[23]	140	~ 25	~ 4	4	—	0.3 – 0.6	RCD	Discrete Si MOSFET
[45]	120	~ 6.5	~ 1.1	~ 0.125	—	> 0.1	RCD	Discrete Si MOSFET
[25]	50	~ 2	~ 1	~ 0.1	—	1	RCD	0.35 μm HV-CMOS
[46]	140	—	—	1.87	—	0.01	RCD	Discrete Si BJT
[48]	75	49	2.8	—	—	10	RCD	Discrete GaN FET
[53]	5	5	5	—	—	20	Shunt CM	TS 0.18 μm 5V-gated
[57]	10	28	~ 0.9	—	—	200	VM	55nm CMOS
[54]	70	~ 10	10 – 50	—	4.2	0.02 – 0.1	Series CM	0.35 μm 80V CMOS
[5]	54	≤ 18.55	~ 0.850	—	18.5	40	Series CM	160nm BCD
[4]	3.3	≤ 2.3	5	5	75.6	100	Series CM	0.18 μm CMOS
[3]	3 – 5.5	≤ 0.5	≥ 0.464	0.074 – 5	35.2	200	Series CM	0.18 μm CMOS
This work	2.5	0.2	≤ 1	0.191 – 0.824	up to 47.5	250	VM	STMicroelectronics’ 40nm CMOS

Table 6.1 – Performance summary compared to the current state-of-the-art.

6.2 Perspectives

6.2.1 Test setup

First and foremost, the electrical test setup is not adequate for measuring the performances of the test chip. This is most likely due to circuit parasitics contributed by the test platform (package, PCB and load resistor). Thus, we have brought out two main perspectives regarding electrical characterization:

- Circuit parasitic extraction to rigorously compare and correlate measurement and simulation results. This topic has been partly examined by means of scattering parameters measurement.
- Design of an optimal electrical characterization PCB with minimum circuit parasitics.

Then, several axis for enhancement of the optical experimental setup have been underscored:

- Improvement of the accuracy of laser pulse shape measurements via an increase in the setup's bandwidth (equipment-related matter). This point has been partially looked at by means of a high-speed fiber-coupled photodetector, but further in-depth investigation is necessary.
- Characterization of the VCSEL as a function of temperature for accurate extrapolation of the driving current peak and power efficiency data.
- Test chip verification within a direct time-of-flight system, *i.e.* together with the SPAD-based detector. This would allow to rightly assess the proposed driver topology in the application context.
- Joint monitoring of the laser pulse shape as well as the corresponding driving electrical waveform.

6.2.2 Module design

Parasitics in the current path through the VCSEL are a major performance-limiting factor. Specifically in sub-500ps pulse operation, parasitic inductance seems to prevent the full build up of the laser driving current pulse. Thus, the optimization of the physical interconnect between the driver chip and the VCSEL die appears as a major axis for future improvement. This should be made possible through a redesign of the substrate on which the TOF integrated circuit and the VCSEL are mounted.

6.2.3 Laser diode modelling

So as to carry out the design of the proposed driver circuit, we have only used an electrical VCSEL model built from $I - V$ data curve fitting. The main drawback to such a model is that it does not capture the intrinsic dynamics

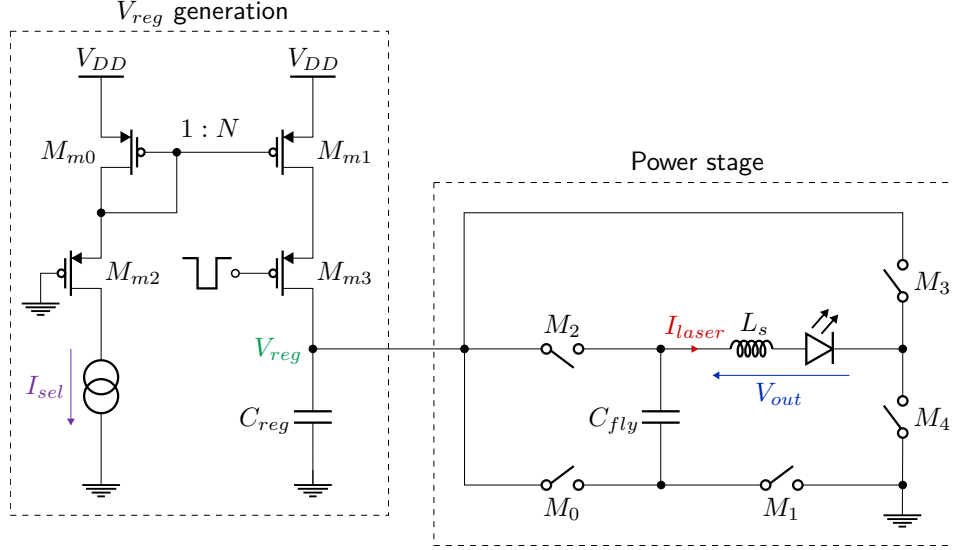


Figure 6.2 – Proposed current control strategy.

as well as the temperature dependence of the VCSEL. Accordingly, effective circuit design calls for a working electro-optical-thermal model.

6.2.4 Current control strategy

Thermal runaway due to the temperature dependence of the laser diode's forward voltage is a key concern for driver circuit design [11]. So as to prevent such a phenomenon, a current-controlling strategy has been proposed for future design work. The structure is illustrated in Figure 6.2. From the test chip's experimental characterization, it has been shown that the driving current peak varies linearly with supply voltage. Also, the supply voltage does not significantly impact the current and laser pulse duration. Thus, the control strategy we have suggested consists in generating a dynamic voltage node V_{reg} for supplying the driver's power stage. The circuit is based on a simple current mirror structure composed of PMOS M_{m0} and M_{m1} (ratio N). These function in the saturation region. Moreover, PMOS M_{m3} is synchronized with M_2 and M_1 . When on, a charging path for C_{reg} and C_{fly} is created. Note that C_{reg} acts as a decoupling capacitance for node V_{reg} . In opposition to C_{fly} , this capacitor could be implemented off-chip in order to save silicon area, but at the expense of adding off-chip physical interconnect. When M_0 and M_4 are on, C_{reg} and C_{fly} are connected in series and discharge through the laser diode. In this way, node V_{reg} dynamically adjusts according to the amount of charge provided by the current mirror (defined by current I_{sel}) and pulsed through the laser diode. This strategy allows to set the average current $\overline{I_{laser}}$ flowing through the load,

$$\overline{I_{laser}} = \frac{1}{2} N I_{sel} (1 - \alpha) \quad (6.1)$$

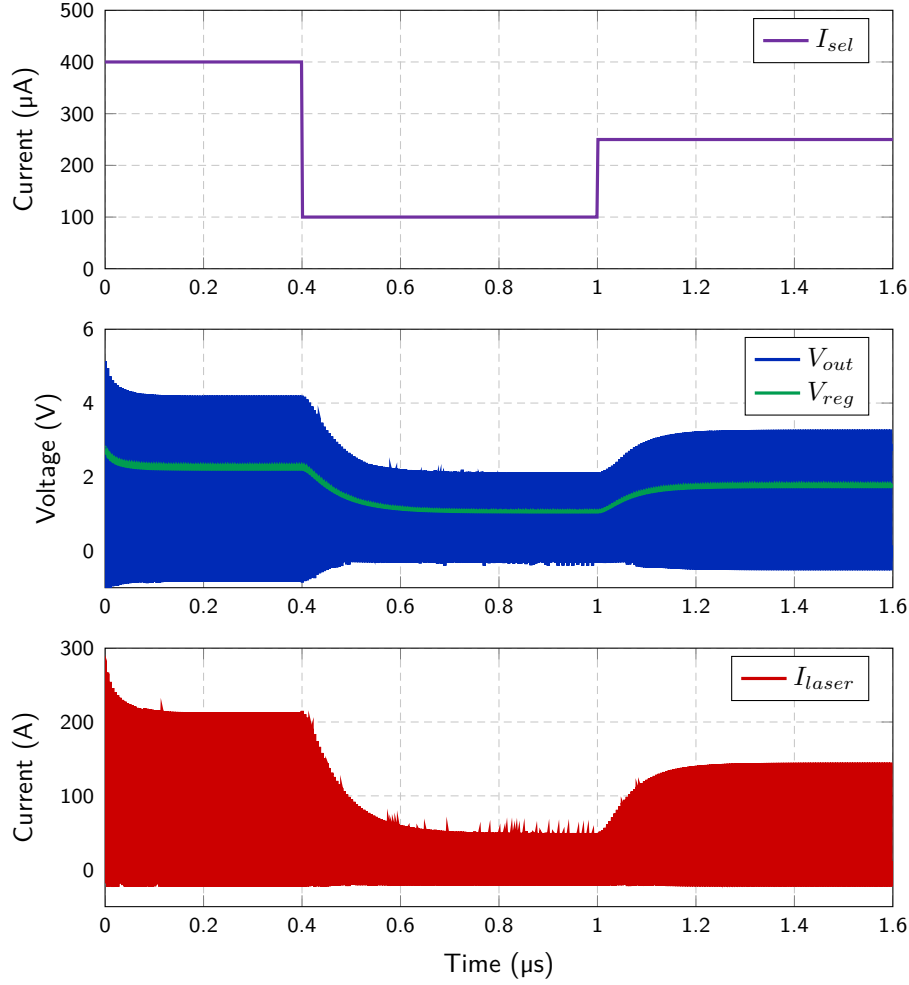


Figure 6.3 – Simulated waveforms of the current control strategy.

where α is the duty cycle of the power stage.

The full architecture has been validated with a simplified simulation circuit using ideal supply and control voltage sources. The supply voltage V_{DD} is fixed to $2.8V$. Additionally, C_{reg} , C_{fly} and N are set to $1nF$, $200pF$ and 100 , respectively. The simulated waveforms for a duty cycle of 10% ($t_{mod} = 500ps$ and $f_{sw} = 200MHz$) are represented with a $1.6\mu s$ time range in Figure 6.3.

One can see that the proposed current control strategy enables to adjust the driving current through the laser diode. In the same way, it should dynamically compensate for temperature-induced forward voltage variations. However, the circuit should be properly validated with a future test chip.

6.3 Dissemination

The work presented in this manuscript has been disseminated through various publications, as well as protected by several patent fillings. The dissemination is listed in the subsequent parts.

6.3.1 Patents

- Samuel Rigault and Nicolas Moeneclaey, "Control circuit for a laser diode," *United States Patent Application US20200106239A1*, 2020.
- Samuel Rigault, Xavier Branca and Nicolas Moeneclaey, "Laser diode driver circuits and methods of operating thereof," *on-going*.

6.3.2 Conferences

- Samuel Rigault, Nicolas Moeneclaey, Lioua Labrak and Ian O'Connor, "CMOS VCSEL driver dedicated for sub-nanosecond laser pulses generation in SPAD-based time-of-flight rangefinder," *2018 Conference on Design of Circuits and Integrated Systems (DCIS)*, 2018.
- Samuel Rigault, Nicolas Moeneclaey, Lioua Labrak and Ian O'Connor, "A Low-Voltage Sub-ns Pulse Integrated CMOS Laser Diode Driver for SPAD-based Time-of-Flight Ranging in Mobile Applications," *2019 32nd IEEE International System-on-Chip Conference (SOCC)*, 2019.

A Photon detection calculation for time-of-flight measurement

The setup of a time-of-flight measurement is presented in Figure A.1. The light source is a pulsed laser diode with a lasing wavelength λ_{laser} . A pulse of energy E_{laser} is transmitted towards an extended target of reflectivity ρ located at a distance d from the measuring setup. The reflected energy is captured by the SPAD-based detector, with A_{det} being the area of the detector's lens.

Assuming a homogeneous, isotropic and non-absorbing propagation medium (such as clear air), the energy E_{trg} incident on the target is simply,

$$E_{trg} = E_{laser} \quad (A.1)$$

The target is assumed to exhibit a diffusely reflecting surface with Lambertian reflectance. Then, the energy per solid angle $E_{trg,\Omega}$ reflected by the target is determined from the solid angle of the half-sphere. Recall that a unit solid angle in spherical coordinates is expressed as, $d^2\Omega = \sin\theta d\theta d\phi$, with θ being the reflection angle relative to the target surface's normal.

$$E_{trg,\Omega} = \frac{\rho E_{laser}}{\int_0^{2\pi} \int_0^{\frac{\pi}{2}} \cos\theta \sin\theta d\theta d\phi} = \frac{\rho E_{laser}}{\pi} \quad (A.2)$$

The reflected energy received by the detector can be expressed according to the solid angle Ω_{det} subtended by the detector's optics.

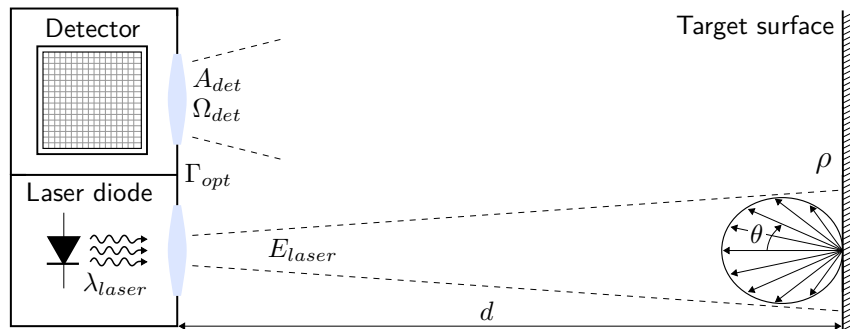


Figure A.1 – Time-of-flight measurement setup with quantities of interest.

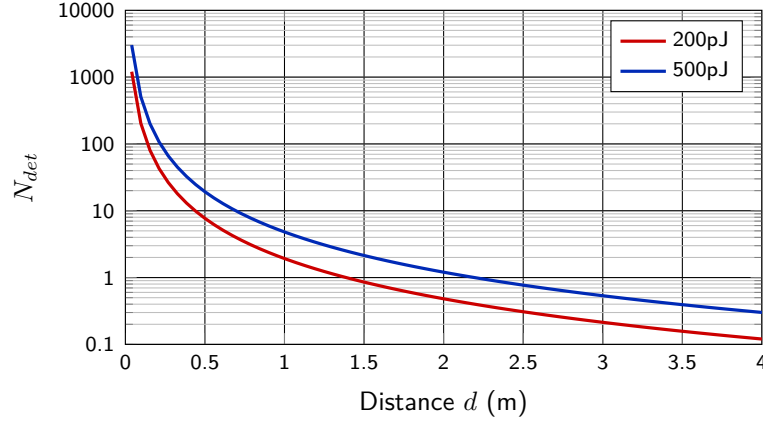


Figure A.2 – Number of photon detection versus distance with a 200pJ and a 500pJ laser pulse energy.

$$E_{det} = E_{trg,\Omega} \Omega_{det} = \frac{\rho E_{laser}}{\pi} \frac{A_{det}}{d^2} \quad (A.3)$$

Finally, the average number of photon detection per laser pulse is determined by multiplying E_{det} by the SPAD's photon detection efficiency η_{SPAD} and by dividing by the photon energy $E_{ph} = \frac{hc}{\lambda_{laser}}$. Here, $h = 6.626 \times 10^{-34} J.s$ is the Planck's constant and $c = 3 \times 10^8 m.s^{-1}$ is the speed of light. In addition, the efficiency of the optics is taken into account with coefficient Γ_{opt} .

$$N_{det} = \frac{\rho E_{laser} \Gamma_{opt} A_{det} \eta_{SPAD}}{\pi d^2 \frac{hc}{\lambda_{laser}}} \quad (A.4)$$

Table A.1 summarizes the parameters' value for an example case. The resulting photon detection curve as a function of distance is shown in Figure A.2.

Parameter	Value	Unit
λ_{laser}	940	nm
ρ	40	%
Γ_{opt}	80	%
A_{det}	1	mm ²
η_{SPAD}	2	%

Table A.1 – Physical parameters for example case.

B VCSEL fundamentals

The vertical-cavity surface-emitting laser (VCSEL) is a recent class of semiconductor laser diode that has the peculiarity of being monolithically fabricated. Since their first commercialization in 1996, VCSELs have emerged as the critical technology for high-density optical interconnects ranging from the chip-to-chip links in computer systems up to the local and wide area networks [65, 71]. Within this scope, the laser diode is on-off modulated, usually with a forward current of a few milliamps, to enable the transmission of digital signals. VCSELs are also widely used in various optical systems such as computer mice, displays, optical disks, laser printers and so on [65].

Now, VCSELs appear as a very suitable light source regarding the current demand for sensing capacities in a wide range of applications. As a matter of fact, the intrinsic single-longitudinal-mode operation, non-astigmatic and circular output beam, enhanced reliability and scalability in two-dimensional arrays are among the advantages of VCSELs that make them more superior to conventional light-emitting diodes (LED) and edge-emitting lasers (EEL) [6, 33, 62, 63, 113].

The typical lasing wavelengths for infrared illumination and sensing in the consumer market are between $830nm$ and $950nm$ [7]. In this way, illuminators are compatible with the existing mature detector technology based on silicon. VCSELs operating within the $830nm$ to $950nm$ spectral range are typically grown on gallium arsenide (GaAs). This appendix review the main properties and advantages of GaAs-based VCSELs.

B.1 Background

Laser diodes, like most lasers, consist in a optical gain medium within a resonant optical cavity. If the active medium is supplied with energy (electrical current for electrically pumped laser diodes), electrons and holes within the gain material recombine according to the well-known stimulated emission process and create coherent photons (light-matter interactions are underlined in Figure B.1) [69]. Laser diodes are typically engineered by incorporating an intrinsic direct bandgap semiconductor layer between a $n-$ and $p-$ doped cladding layers (see Figure B.2) [69]. This structure is often referred to as double-heterostructure since the cladding layers are usually processed using a

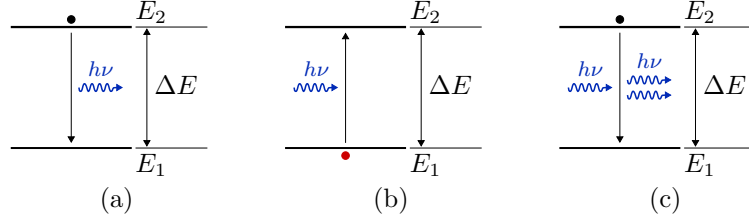


Figure B.1 – Light-matter interactions: (a) spontaneous emission, (b) absorption, (c) stimulated emission.

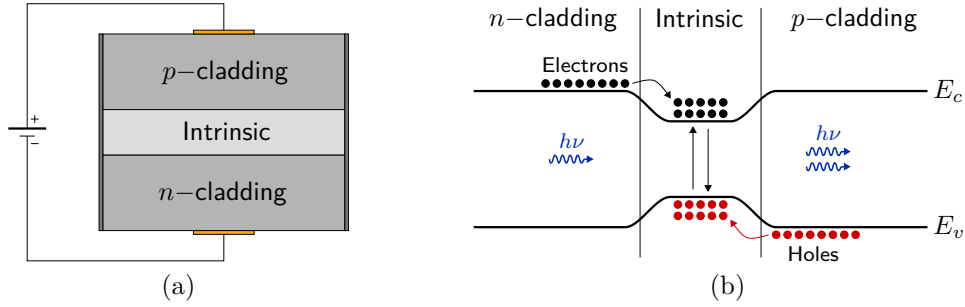


Figure B.2 – Principle of the double-heterostructure laser diode: (a) material structure, (b) energy diagram of the conduction and valence bands.

material with an energy gap higher than that of the intrinsic region. Thus, under forward bias, electrons and holes injected in the double-heterostructure from the n - and p -type metallizations accumulate in the intrinsic gain region. What is more, claddings act as a waveguide due to their lower refractive index. In other words, the double-heterostructure provides carrier and light confinement [69].

At a particular pumping current, referred to as the threshold current, stimulated emission within the resonant cavity dominates over spontaneous emission and lasing occurs. This condition is reached when the gain of the material exactly matches the losses experienced by light in one round-trip of the cavity. The threshold modal gain g_{th} can be expressed as,

$$g_{th} = \alpha_i + \alpha_m = \alpha_i + \frac{1}{2l_{cav}} \ln \left(\frac{1}{R_f R_r} \right) \quad (\text{B.1})$$

where α_i is the internal loss, α_m is the mirror loss, l_{cav} is the cavity length and R_f and R_r are the reflectivity of the front and rear mirrors, respectively.

Furthermore, lasing requires that the standing wave condition is verified, meaning that the resonant cavity supports a finite number of longitudinal modes. This resonance condition is checked when the cavity length is a multiple of half the wavelength, as defined by,

$$l_{cav} = m \frac{\lambda}{2n_{eff}} \quad (B.2)$$

where λ is the wavelength, n_{eff} is the effective refractive index and m is an integer called the mode order [69]. Then, the longitudinal mode spacing $\Delta\nu$ within the cavity is inversely proportionnal to the cavity length,

$$\Delta\nu = \frac{c}{2n_{eff}l_{cav}} \quad (B.3)$$

where c is the speed of light.

B.2 VCSELs versus EELs

In classical laser diodes, also referred to as edge-emitting lasers or stripe lasers, the optical cavity is formed in the plane of the semiconductor active layers, *i.e.* parallel to the wafer surface as shown in Figure B.3a [69]. Since the light is emitted from one facet of the semiconductor laser, the characteristics of the output beam depends directly on the active region's rectangular cross section. Thus, EELs suffer from a highly elliptical beam shape which makes the design and integration of coupling optics complex and expensive [64]. In terms of manufacturing, the cavity mirrors are fabricated either by cleaving or etching with a resulting 30% reflectivity due to the discontinuity in the refractive index at the semiconductor/air interface. Hence, the testing of the laser chip can only be carried out once several processing and packaging steps are completed [64]. Finally, stripe lasers display a long resonant cavity of several hundreds of micrometers and therefore lase inherently on multiple wavelengths (as defined by the standing wave condition), unless a particular structure is employed for the design of the cavity.

The VCSEL technology is significantly different from conventional laser diodes. In VCSELs, the light propagates perpendicularly to the vertically-grown epitaxial layers. The cavity length is simply the overall thickness of the active layers and is therefore much shorter ($\sim 1 \mu m$) as compared to edge emitters. Due to the short gain length, the active region and the laser heterostructure are sandwiched between two multi-layers distributed Bragg reflectors (DBR) which can achieve reflectivity greater than 99.5%. Those high-reflectivity mirrors are mandatory to confine photons in the active region and hence to achieve lasing as evidenced by equation (B.1).

VCSELs designed for emission in the 850nm to 980nm spectral range are generally manufactured with approximately 8μm of epitaxially-grown material. On the other hand, the active region is composed solely of multiple quantum wells with some 10nm thickness [67]. In recent VCSELs, current confinement and index guiding are typically ensured by oxide layers which are located close

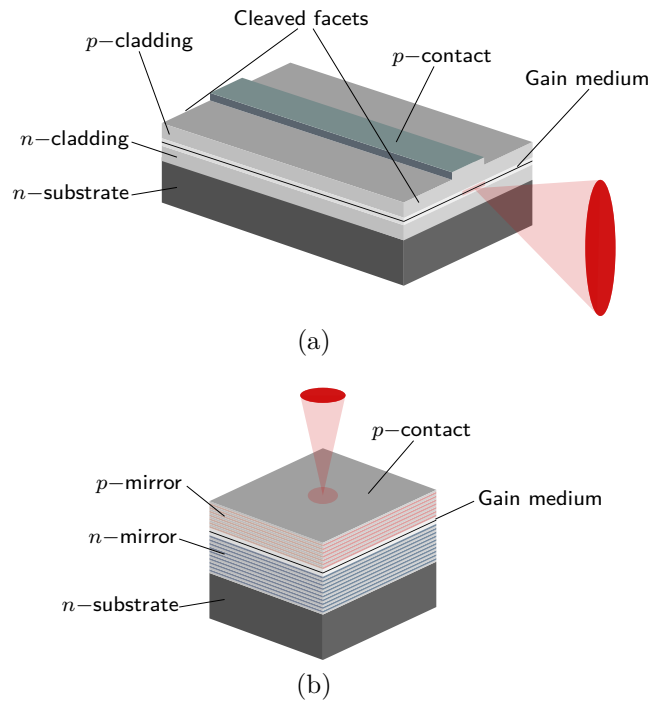


Figure B.3 – Schematic drawings of semiconductor lasers: (a) EEL, (b) VCSEL.

to the active region in order to lower lateral carrier diffusion effects [65–67]. Figure B.3b shows the typical cross-sectional view of a top-emitting VCSEL device. Since VCSELs exhibit a very short resonator length, the longitudinal mode spacing is sufficiently large to ensure single-longitudinal mode operation. However, given their large transverse dimensions, *i.e.* typically from $10\mu m$ to $20\mu m$, the cavity supports inherently multiple transverse or spatial modes.

The VCSEL’s geometry provides several key advantages over conventional semiconductor high-emitting devices. First, the surface-emitting design allows VCSELs to be entirely processed on wafer level. Equally, on-wafer testing can be performed at several steps throughout the manufacturing process, thereby providing a potential for low-cost fabrication at high yield [64]. Moreover, VCSELs have beneficial high-speed characteristics. As a matter of facts, given their small cavity volume, VCSELs’ typical threshold current value are in the sub-milliamp range. Also, their relaxation frequency is very high even at low current level, *i.e.* higher than $5\text{--}10GHz$. Therefore, given that the modulation bandwidth is directly proportional to the relaxation frequency, VCSELs can be modulated at high-speed with low power consumption [65, 66].

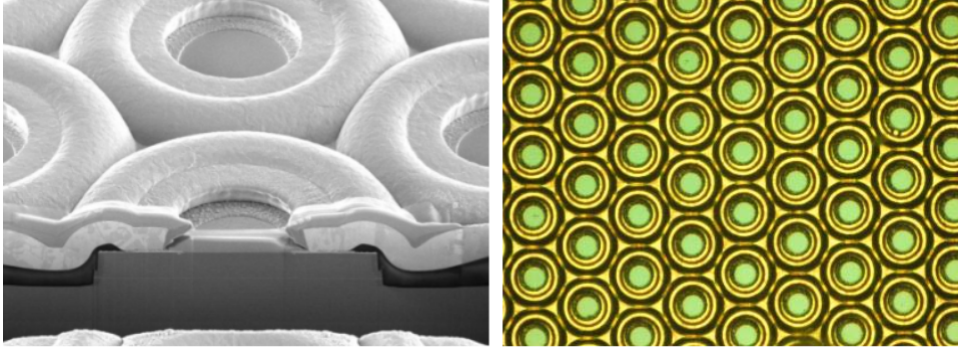


Figure B.4 – SEM and plan view of a VCSEL array [6].

B.3 VCSEL arrays for infrared illumination

Single VCSELs are limited in optical output power with a typical power range of $1mW$ to $30mW$ for active diameters between $4\mu m$ and $20\mu m$, respectively [6]. Further increase of the active diameter has already been investigated [114]. However, this approach is problematic since increasing the diameter results in a significant drop of the wall-plug or power conversion efficiency as well as a deterioration of the output beam quality. On the other hand, VCSELs are scalable in densely packed arrays comprising from tens to thousands individual lasers (often referred to as mesas) connected in parallel on a single chip. VCSEL arrays maintain the same laser performance as single devices and provide a scalable optical output power [33, 62, 63]. Thus, they are the ideal candidate to handle the high power requirements of infrared illumination applications. Figure B.4 represents the scanning electron microscope (SEM) and plan view of a VCSEL array [6]. It is worth noting that the individual mesas in an array are connected with each other by the same electrodes.

It is widely accepted that VCSEL arrays are an attractive light source for infrared illumination as compared to conventional LEDs or edge emitters. Since the emission of VCSELs is set by a λ -thick optical cavity, its spectral width is very narrow, typically $1 - 2nm$ wide [33, 62, 63]. Similarly, their emission wavelength is significantly stable over temperature with only a $0.065nm/K$ thermal shift [62, 63]. Thus, assuming an operating temperature range of $0 - 80^\circ C$, the wavelength will shift by only $5nm$ over this range. In LEDs or EELs, the wavelength's thermal shift is usually much larger, *i.e.* $0.3nm/K$ [7, 62]. In time-of-flight sensors, these advantageous emission properties enable to combine the detector with narrow band filters thus removing unwanted environmental lights and improving signal-to-noise ratio for range measurement [7, 62, 113]. Furthermore, given that VCSEL arrays are made up of multiple individual lasers, the far field pattern is the superposition of the far fields of the mesas. Because individual mesas emit incoherently and independently of each other,

the interference effect is low. Hence, VCSEL arrays provide speckle-free illumination, which is critical for various imaging applications [6, 33, 113]. In addition, due to their surface-emitting design, the emission beam is intrinsically circular with a small divergence angle which allow straightforward and efficient coupling with optics [33, 62, 67, 113]. Therefore, the beam divergence can be easily tailored according to the targeted application.

In terms of efficiency, individual VCSELs as well as VCSEL arrays exhibit a wall-plug efficiency that can be higher than 50% [65, 66]. In [33], a peak efficiency of 56.4% is reported for a VCSEL array operating at $976nm$. Therefore, the VCSEL technology is about to reach the same efficiency as EELs which is currently 70% [33].

Last but not least, VCSEL arrays reported in the litterature have shown advantageous switching characteristics with rise and fall time significantly lower than $1ns$ demonstrated. For instance, the high-power VCSEL presented in [7] achieved a rise and fall time of $180ps$ at a normal operating power of $5 - 10W$ when properly package with driver (see Figure B.5). In [113], a pulse duration of $85ps$ up to $100mW$ is achieved with a 25 mesas VCSEL array emitting at $850nm$.

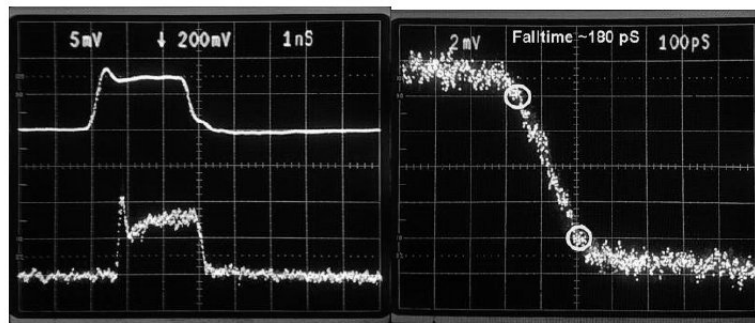


Figure B.5 – Example of VCSEL pulse [7].

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Direct time-of-flight (TOF) laser rangefinding is a remote sensing technology which has recently been a growing focus in a wide range of applications. This technique makes it possible to determine the distance to an unknown target from the measurement of the round-trip transit time of a light pulse. A direct TOF sensor is usually implemented by a photodetector based on single-photon avalanche diodes (SPAD) as well as by a near-infrared semiconductor laser. In such a system, the importance of the laser driving electronics cannot be overstated. Thus, the aim of the present thesis, carried out with STMicroelectronics, is to develop a fully integrated vertical-cavity surface-emitting laser diode driver for direct TOF rangefinding in consumer embedded electronics. The key focus is to demonstrate the feasibility of sub- ns pulse operation at high repetition frequency, up to several hundreds of megahertz. Last but not least, in the context of consumer mobile devices, there is always a need to aim towards a low-voltage and power- and area-efficient solution. The key innovation of this thesis is the development of a novel laser diode driver topology. The circuit incorporates a capacitive voltage boost structure so as to overcome the low-voltage constraint. In addition, slow turn-off transient phenomena associated with laser diodes, such as optical tailing, could limit the performances of direct TOF sensors. Accordingly, the proposed driver architecture adds a carrier sweep-out circuit feature in order to mitigate such unwanted phenomena. The circuit has been fabricated in a $40nm$ complementary metal-oxide-semiconductor (CMOS) technology node by STMicroelectronics. The main experimental result is the demonstration of a laser pulse of $311ps$ with a driving current peak up to $200.8mA$ at a supply voltage of $2.5V$ and a repetition frequency of $250MHz$. Simply put, the achievements of this thesis represent an important step forward towards future product development by STMicroelectronics.

La détection laser par temps de vol (TOF) direct est une technologie qui représente un enjeu majeur dans un nombre croissant d'applications. Cette technique permet de déterminer la distance d'une cible inconnue à partir de la mesure du temps de vol d'une impulsion laser. De manière générale, un capteur TOF direct est réalisé par un photodétecteur utilisant des photodiodes à avalanche mono-photonique ainsi que par un laser à semi-conducteur. Dans ces capteurs, le circuit de pilotage du laser est d'une importance cruciale. Le but de la présente thèse, effectuée en partenariat avec l'entreprise STMicroelectronics, est de développer un circuit intégré pilote de diode laser à cavité verticale pour la détection laser TOF dans l'électronique embarquée grand public. La spécification majeure est de démontrer la faisabilité d'impulsion laser inférieure à la nanoseconde à une fréquence de répétition de l'ordre de plusieurs centaines de megahertz. De plus, dans le contexte des appareils mobiles grand public, il y a toujours un besoin de concevoir une solution fonctionnant à basse tension, efficace en puissance et compact. L'innovation majeure de ce travail est le développement d'une nouvelle topologie de circuit pilote de diode laser. Le circuit proposé est composé d'une structure à pompe de charge afin de satisfaire la contrainte sur la tension d'alimentation. De plus, les phénomènes de coupure lente associés aux diodes laser ont été identifiés comme des facteurs limitants potentiels pour les performances des capteurs TOF directs. En conséquence, l'architecture développée inclue une fonction spécifique permettant de prévenir de tels effets via une extraction rapide des charges stockées dans la diode laser. Le circuit a été fabriqué avec la technologie CMOS $40nm$ de STMicroelectronics. Le résultat fondamental de la thèse est la démonstration d'un courant de pilotage pic de $200.8mA$, correspondant à une impulsion laser de $311ps$, à une tension d'alimentation de $2.5V$ et une fréquence de répétition de $250MHz$. En résumé, les résultats de cette thèse représentent un pas en avant significatif pour les développements futurs de STMicroelectronics.