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# THÈSE POUR OBTENIR LE GRADE DE DOCTEUR DE L'UNIVERSITÉ DE MONTPELLIER

En Systèmes Automatiques et Microélectroniques

École doctorale : Information, Structures et Système (I2S)

Unité de recherche : Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM)

## Étude des Effets Induits par la Radiation Spatial et Atmosphérique sur des Mémoires Électroniques

(Analysis of Space and Atmospheric Radiation-Induced Effects on Memory Devices)

Présentée par Lucas MATANA LUZA

Le 14 decembre 2021

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## Résumé

Le rayonnement est défini comme l'émission ou la transmission d'énergie sous forme d'ondes ou de particules, qui peuvent être ionisantes ou non ionisantes. L'interaction entre le rayonnement et la matière peut générer différentes réactions, qui peuvent varier en fonction des propriétés de la particule (type, énergie cinétique, masse et charge) et de la matière ciblée (semi-conducteurs dans le cadre de cette thèse). L'exposition de composants électroniques à des environnements avec une présence significative de rayonnement peut conduire à ce type d'interaction et, par conséquent, à une variété d'effets qui peuvent affecter considérablement la fiabilité des systèmes électroniques.

Lors de la conception de dispositifs et de systèmes électroniques, la prise en compte des effets des rayonnements est fondamentale pour les applications dans des environnements hostiles. Par exemple, dans les systèmes avioniques et spatiaux, ces effets sont largement étudiés pour garantir la haute fiabilité des composants et fournir les informations nécessaires pour les décisions de conception. Les préoccupations liées aux rayonnements ont commencé à être prises en compte au début de l'ère spatiale.

Les rayonnements ionisants peuvent induire des effets dans différents dispositifs, et plusieurs travaux ont montré que les mémoires électroniques sont l'une des principales causes d'erreur dans les systèmes. De plus, en raison de leur nature, les mémoires ont la capacité intrinsèque de stocker la trace des fautes induites par les rayonnements, comme le Single-Bit Upset (SBU), ce qui fait de ces dispositifs le meilleur candidat pour étudier les événements singuliers.

Le premier sujet introduit par la thèse est une étude sur les effets induits par les ions lourds sur une mémoire Flash de type NAND. Cette étude est basée sur plusieurs campagnes d'irradiation avec une large gamme d'énergies. Les résultats ont révélé différents mécanismes de défaillance, notamment des SBUs, des petits groupes d'erreurs, des fautes dans le registre et des fautes affectant une ou plusieurs colonnes de la mémoire. La section efficace a été calculée pour chaque type de faute, et leurs causes ont été discutées.

Ensuite, une étude sur les effets de la radiation neutronique (spectres thermiques et atmosphériques) sur une DRAM auto-rafraîchissante est présentée. Des méthodes de test statique et dynamique ont été utilisées pour définir la réponse du dispositif sous faisceau

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neutronique. Dans ce manuscrit, les résultats expérimentaux de deux campagnes de tests sont présentés, avec l'identification de différents modèles de faute, comme les SBUs, bits collés et blocs d'erreurs. Ces fautes ont été étudiées et caractérisées avec le calcul de la section efficace, du taux d'erreurs et l'étude des bitmaps. Une analyse du temps de rétention des cellules affectées a été réalisée, montrant une différence d'efficacité entre le mécanisme d'autorafraîchissement et une véritable opération de lecture. De plus, une corrélation du mécanisme de défaillance qui génère à la fois des SBUs et des bits collés est également proposée. Finalement, les effets de réparation du recuit à haute température ont été étudiés dans des tests post irradiation.

Après, ce manuscrit présente aussi une étude comparative sur les effets induits par les neutrons sur les SDRAM produites avec trois nœuds technologiques différents. Les résultats ont révélé la présence de SBUs et de bits collés dans les mémoires, montrant une sensibilité plus élevée pour la génération la plus ancienne et des résultats similaires pour les deux autres modèles étudiés.

Enfin, une procédure est présentée afin d'évaluer la fiabilité des applications basées sur réseau de neurones convolutifs (CNN). Dans cette optique, cette étude propose d'utiliser des modèles de défauts réalistes extraits des tests de rayonnement comme entrée pour un émulateur logiciel qui effectue l'injection de défauts dans le système informatique dans lequel le CNN est implémenté.

**Mots-clés:** Radiation, effets singuliers, DRAM, mémoire Flash, injection de fautes, réseaux de neurones

## Abstract

Radiation is defined as the emission or transmission of energy as waves or particles, which can be either ionizing or non-ionizing. The interaction between the radiation and the matter can generate different reactions, which may vary depending on the properties of the particle (type, kinetic energy, mass, and charge), and the target (semiconductors in this thesis scope). The exposition of electronics components to environments with a significant presence of radiation may lead to this kind of interaction and, consequently, to a variety of effects that can drastically affect the reliability of electronic systems.

When designing electronic devices and systems, considering radiation effects is fundamental for applications in harsh environments. For instance, in avionics and space systems, these effects are extensively studied to ensure the high reliability of the components and provide the needed insight for design decisions. The concerns related to radiation started to be noted at the beginning of the space era.

Ionizing radiation may induce effects in different types of devices, and many works have shown that memories are one of the highest contributors to soft errors in systems. Furthermore, due to their nature, memories have the intrinsic capability of storing radiation-induced fault tracks, e.g., Single-Bit Upsets (SBUs), making these devices the best candidate for studying soft errors.

The first topic introduced by the thesis is a study on the heavy-ion induced effects on a Single-Level Cell NAND Flash. This study is based on several irradiation test campaigns with a wide range of heavy-ions energies. The results revealed different failure mechanisms, including Single-Event Upsets, small clusters of errors, data register upsets, and a column-wise failure mode. Cross section was calculated for each of these failure modes, and their causes were discussed.

Then, a study on the effects of neutron irradiation (thermal and atmospheric-like spectra) on a self-refresh DRAM is presented. Static and dynamic test methods were used to define the response of the device under irradiation. In this manuscript, experimental results from two different test campaigns are presented, with the identification of SBUs, stuck bits, and block errors. These faults were investigated and characterized by event cross section, soft-error rates, and bitmaps evaluations. An analysis of the damaged cells' retention time was

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performed, showing a difference between the self-refresh mechanism and a read operation. Additionally, a correlation of the fault mechanism that generates both SBUs and stuck bits under neutron irradiation is also proposed. Furthermore, high-temperature annealing was studied in post-radiation tests.

Following, this thesis presents a comparative study on the neutron-induced effects on SDRAMs produced with three different technology nodes. The results revealed the occurrence of SBUs and stuck-bits in the memories, showing higher sensitivity for the oldest generation and similar results for the other two models.

Finally, a framework is presented to assess the reliability of Convolutional Neural Network (CNN) applications. In this light, this study proposes using realistic fault models retrieved from radiation tests as input for a software emulator that performs fault injection in the computing system in which the CNN is implemented.

**Keywords:** Radiation, single-event effects, DRAM, Flash memory, fault injection, neural networks

## Résumé Substantiel en Français

Le rayonnement est défini comme l'émission ou la transmission d'énergie sous forme d'ondes ou de particules, qui peuvent être ionisantes ou non ionisantes. L'interaction entre le rayonnement et la matière peut générer différentes réactions, qui peuvent varier en fonction des propriétés de la particule (type, énergie cinétique, masse et charge) et de la matière ciblée (semi-conducteurs dans le cadre de cette thèse). L'exposition de composants électroniques à des environnements avec une présence significative de rayonnement peut conduire à ce type d'interaction et, par conséquent, à une variété d'effets qui peuvent affecter considérablement la fiabilité des systèmes électroniques.

Le domaine des effets des rayonnements dans la recherche en électronique demande des investigations pour chaque nouveau composant et technologie. Lors de la conception de dispositifs et de systèmes électroniques, la prise en compte des effets des rayonnements est fondamentale pour les applications dans des environnements hostiles. Par exemple, dans les systèmes avioniques et spatiaux, ces effets sont largement étudiés pour garantir la haute fiabilité des composants et fournir les informations nécessaires pour les décisions de conception. Les préoccupations liées aux rayonnements ont commencé à être prises en compte au début de l'ère spatiale.

Les environnements radiatifs en naturels ou artificiels. Les milieux naturels comprennent l'espace et l'atmosphère. Les environnements artificiels sont, par exemple, les centrales nucléaires et les accélérateurs de particules. Chaque environnement est caractérisé par la présence de différents spectres de rayonnement.

L'aspect principal du rayonnement ionisant et de son interaction avec les dispositifs électroniques est le dépôt d'énergie dans le matériau. Les effets des rayonnements sont divisés en trois catégories principales : la dose ionisante totale (TID), les dommages par déplacement (DD) et les effets singuliers (SEE). Les SEE sont dus à une particule énergétique traversant le matériau semi-conducteur transférant son énergie par le biais d'interactions coulombiennes. Le passage de la particule ionisante crée des paires électrons-trous qui peuvent atteindre des endroits critiques du dispositif, entraînant différents types d'effets, par exemple, des bit flip dans la mémoire, des courants parasites, des transitoires de tension sur les nœuds du circuit. TID et DD sont des effets cumulatifs causés par l'accumulation de rayonnements



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ionisants entraînant une dégradation à long terme des paramètres du dispositif, par exemple une augmentation du courant de fuite et un décalage de la tension de seuil des transistors.

À mesure que les nœuds technologiques deviennent plus petits et les composants plus intégrés, le dépistage des effets induits par les rayonnements sur les composants devient encore plus important. Cette recherche joue un rôle crucial dans la compréhension de la fiabilité de chaque technologie, de ses mécanismes de défaillance et des techniques de durcissement qui peuvent être appliquées. Les effets des rayonnements peuvent différer lorsque l'on considère différents nœuds technologiques, par exemple, les SEEs par ionisation induits par les protons, ont une importance croissante pour les technologies les plus intégrées.

Comme mentionné plus haut, une seule particule ionisante passant à travers un dispositif semi-conducteur perd de l'énergie par les interactions coulombiennes et laisse une trace de paires électron-trou libres. L'excès créé de porteurs de charges mobiles atteignant les sites sensibles du dispositif peut conduire à des SEEs. Les parties les plus sensibles des composants électroniques sont généralement les jonctions p/n polarisées en inverse, car ces régions peuvent collecter efficacement les charges mobiles en raison de la présence d'un champ électrique élevé. Contrairement aux effets de dose, qui sont cumulatifs dans le temps, les SEEs sont des effets localisés dus à un impact d'une particule unique, provoquant un état transitoire pouvant conduire à des dommages temporels (*soft errors*) ou permanents (*hard errors*). Les erreurs temporelles sont celles qui peuvent être corrigées ou récupérées. Par exemple, une cellule de mémoire qui a perdu son information, une fois qu'elle sera réécrite, elle ne sera plus fautive. Les erreurs permanentes provoquent des dommages physiques irréversibles, par exemple, la rupture d'un diélectrique de grille. De plus, certaines fautes peuvent être classées comme temporelles ou permanents selon les effets qui les produisent. Par exemple, le *Single-Event Latch-up* peut provoquer une erreur permanent si la coupure d'alimentation n'est pas effectuée rapidement, ou simplement des effets transitoires.

Cette thèse est consacrée à l'étude des effets induits par les radiations, avec un focus particulier sur les SEEs dans les mémoires. L'utilisation de dispositifs commerciaux standards dans l'avionique, les missions spatiales ou les accélérateurs de particules nécessite une compréhension de leur comportement lorsqu'ils sont exposés à des environnements hostiles. Dans l'étude bibliographique, plusieurs travaux ont montré que les mémoires électroniques sont l'une des principales contributrices aux défaillances des systèmes. En raison de leur nature, les mémoires sont capables de stocker des erreurs induites par les rayonnements en forme de *Single-Bit Upset* (SBU) ou *Multiple-Cell Upset* (MCU), ce qui fait de ce dispositif le meilleur candidat pour étudier ce type de faute. Ensuite, en mettant l'accent sur les environnements spatial et avionique (atmosphérique), cette thèse présente les résultats d'une

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recherche de trois ans sur les effets de différentes sources de rayonnement sur plusieurs types de mémoires électroniques.

Le premier sujet introduit par la thèse est une étude sur les effets induits par les ions lourds sur une mémoire Flash de type NAND. La mémoire Flash est un type d'EEPROM (*Electrically Erasable Programmable Read-Only Memory*) basé sur une cellule à transistor unique à grille flottante (FG). Cette technologie a joué un rôle important sur le marché des mémoires non volatiles à semi-conducteurs, avec une tendance agressive à l'intégration. Dans la suite, la technologie à base la mémoire Flash et les effets induits par les rayonnements sont discutés. Une étude est présentée sur l'impact des ions lourds sur un dispositif de type Flash faisant partie de la mission MTCube (Memory Test CubeSat). Le projet MTCube a pour objectif principal de développer et tester en vol différentes mémoires commerciales et d'évaluer leur sensibilité à l'environnement spatial en comparant leur comportement dans l'espace avec des données de simulations et de test à l'aide de faisceaux de particules accélérées. L'étude de cette mémoire a conduit à l'identification de différents mécanismes de défaillance. Les plus simples entre eux sont les SBUs. Les bit-flips observés dans la mémoire Flash sont toujours produits par une transition de "0" à "1" logique, ce qui est attendu sur cette technologie puisqu'une grille flottante chargée est, par convention, normalement utilisée pour représenter le "0" logique. Une particule ionisante traversant une grille flottante chargée peut conduire à une décharge de la même, affectant la tension de seuil du transistor et affectant alors la lecture de la donnée stockées. L'apparition de petits groupes d'erreurs, définis comme MCUs, a été identifiée, montrant un comportement similaire aux SBUs. Cela peut se produire en raison du partage de charge (*charge sharing*) dans la ligne de bit ou même de particules secondaires générées avec des angles. Ces tests révèlent également l'apparition de lignes d'erreurs verticales affectant tous les blocs du plan mémoire appartenant à une même colonne. Enfin, des tests spécifiques ont été effectués sur les registres de données de la mémoire. Ces tests ont révélé des SBUs, ainsi que des reset intempestifs des registres.

Ensuite, une étude sur les effets de la radiation neutronique (spectres thermiques et atmosphériques) sur différentes mémoires DRAM a été réalisée. La technologie DRAM est apparue dans les années 70 et reste une technologie importante de nos jours, avec de nouvelles architectures apportant des caractéristiques de haute performance et haute densité. La cellule DRAM est constituée d'un transistor d'accès et d'un condensateur utilisé comme élément mémoire. La charge stockée dans le condensateur définit l'état logique de la cellule, étant utilisée pour représenter un bit avec une valeur "0" ou "1" logique. Une pSRAM a été utilisée comme cible des expériences. La pSRAM est basée sur un plan mémoire de cellule DRAM. Ce type de cellules nécessite des opérations de rafraîchissement périodiques, et dans la pSRAM, l'opération de rafraîchissement est effectuée par un circuit logique embarqué

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dans la puce, qui utilise l'opération de rafraîchissement en fonction de ses exigences de synchronisation et pendant que la mémoire n'est pas en cours de lecture ou d'écriture. Dans cette structure, puisque l'hôte n'a pas besoin de gérer d'opération de rafraîchissement, la mémoire se comporte comme un dispositif SRAM, qui est composé de cellules statiques qui ne nécessitent pas ce type de contrôle, d'où le nom pseudo SRAM (pSRAM). Dans cette étude, il est démontré qu'il existe une similitude entre le mécanisme de défaillance des SBUs et des bits collés. Les cellules présentant un SBU ou un bit collé ont été identifiées et étudiées dans des tests fonctionnels post-radiation où la capacité de rétention a été explorée. Les résultats de ces tests montrent que la dégradation de la rétention est déjà présente dans les cellules avec SBUs, mais elle est beaucoup plus prononcée dans les cellules qui présentent bit collé, c'est-à-dire que ces dernières sont tellement endommagées d'avoir une très faible capacité de rétention. Cependant, concernant le mécanisme physique de défaillance, l'interprétation la plus probable est un endommagement par déplacement qui affecte ou le transistor d'accès ou le condensateur de la cellule mémoire. Cette explication est aussi confirmée par le test de recuit thermique qui démontre une réduction des fautes permanentes et l'amélioration des propriétés de rétention des cellules affectées après exposition à des températures élevées. L'étude a également conduit à l'observation des fautes de type SEFI (*Single-Effect Functional Interruption*) sous la forme de blocs d'erreurs, avec, par exemple, une ligne verticale ou horizontale d'erreurs sur plusieurs adresses. Ces blocs d'erreurs peuvent constituer une menace réelle pour les applications critiques car la mise en œuvre de codes de correction d'erreurs ne sont pas en mesure de faire face à des erreurs de cette envergure.

Ensuite, une étude comparative sur trois nœuds technologiques différents (110 nm, 72 nm et 63 nm) est présentée pour le même dispositif SDRAM placé sous faisceau neutronique. La SDRAM est un type de DRAM dans laquelle les opérations sont effectuées en mode synchrone. Le mode synchrone fonctionne sur la base de signaux de contrôle qui doivent respecter les restrictions du temps d'accès de la mémoire. Les dispositifs SDRAM ont été soumis à un faisceau de neutron avec une spectre atmosphérique. Les résultats ont montré l'apparition de SBUs et de bits collés, comme pour la pSRAM. La comparaison entre les trois technologies a été faite sur la base des sections efficaces pour chaque type de faute, et elle a mis en évidence une sensibilité plus élevée pour la génération la plus ancienne (110 nm). Ceci montrant que les améliorations architecturales et matérielles face à la radiation dans ce cas sont prédominantes par rapport à une sensibilité plus élevée induite par une intégration plus poussée (72 nm et 63 nm). Il est important de souligner que les changements exacts dans la structure, la conception et les matériaux utilisés entre les modèles ne sont pas accessibles au public, pour cela, l'analyse reste dans une perspective de haut niveau.

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Les réseaux de neurones convolutifs (CNN) sont actuellement l'un des modèles prédictifs les plus utilisés en apprentissage automatique (*Machine Learning*). Des études récentes ont démontré que les défauts matériels induits par la radiation, y compris les rayonnements cosmiques, peuvent avoir un impact significatif sur l'inférence des CNNs conduisant à des prédictions erronées. Par conséquent, garantir la fiabilité des CNNs est crucial, en particulier, lorsqu'ils sont déployés dans des applications critiques, telles que la robotique, l'aéronautique et la conduite autonome. Dans cette thèse, un cas d'étude est présenté avec l'objectif d'évaluer l'impact des radiations sur la fiabilité des systèmes où des CNNs ont été implantés. A cette fin, l'étude se base sur des campagnes d'injection de fautes réalistes qui sont extraites dans des campagnes de test par irradiation. Dans ce contexte, les modèles de faute étudiés précédemment dans la mémoire pSRAM ont été utilisés, en particulier les fautes de type SBU, bit collé et bloc d'erreurs, en tenant compte de leur fréquence d'apparition calculée dans les expériences.

Dans cette étude, trois représentations de données ont été exploitées pour créer trois versions du même modèle CNN. Ces versions (*Float 32*, *Int 16* et *Int 8*) ont été implémentées dans un système embarqué utilisant la pSRAM étudiée auparavant. L'un des objectifs de cette étude était d'évaluer la fiabilité de différentes représentations des données, montrant, que la moins sensible est celle qui utilise une représentation de type *integer* sur 8 bits. Le deuxième objectif, comme mentionné avant, était d'explorer l'utilisation des modèles réalistes de fautes pour définir un émulateur capable d'injecter les fautes les plus proches de la réalité représentant un certain environnement et qui pourrait être généralisé pour d'autres types d'application.

En conclusion, l'évolution technologique, qui comporte une meilleure intégration des transistors et l'utilisation de nouveaux matériaux, nous amène à reconduire de nouvelles études pour comprendre l'impact des radiations sur les dispositifs électroniques. Les travaux présentés dans cette thèse contribuent à l'avancement de ces connaissances et évaluent l'impact des radiations non seulement au niveau des dispositifs mais également d'un point de vue des applications au niveau système. De plus, l'approche présentée dans le cas d'étude des réseaux de type CNNs apporte une méthodologie complète pour évaluer la fiabilité des systèmes par la méthode expérimentale et par simulation/émulation.



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# List of Author's Publications

This doctoral thesis is based in part on the following peer-reviewed publications, the number used in this reference list is self-contained and is not related to thesis main matter.

## Journals

- [JO-1] **L. Matana Luza**, A. Ruospo, D. Söderström, C. Cazzaniga, M. Kastriotou, E. Sanchez, A. Bosio and L. Dilillo, “Emulating the Effects of Radiation-Induced Soft-Errors for the Reliability Assessment of Neural Networks” in *IEEE Transactions on Emerging Topics in Computing*, Oct. 2021. DOI: 10.1109/TETC.2021.3116999. [Early access]. © 2021 IEEE

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- [JO-2] **L. Matana Luza**, D. Söderström, H. Puchner, R. G. Alía, M. Letiche, C. Cazzaniga, A. Bosio and L. Dilillo, “Neutron-Induced Effects on a Self-Refresh DRAM” in *Microelectronics Reliability*, vol. 128, pp. 114406, Nov. 2021, DOI: 10.1016/j.microrel.2021.114406.

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- [JO-3] A. Ruospo, **L. Matana Luza**, A. Bosio, L. Dilillo, R. Mariani, M. Traiola, and E. Sanchez, “A Survey on Artificial Neural Networks Reliability Assessment Methodologies,” in *ACM Computing Surveys*. [Under review].

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- [IE-1] A. Ruospo, **L. Matana Luza**, A. Bosio, M. Traiola, L. Dilillo and E. Sanchez, “Pros and Cons of Fault Injection Approaches for the Reliability Assessment of Deep Neural Networks” in *2021 IEEE 22nd Latin American Test Symposium (LATS)*, Oct. 2021, pp. 1-5, DOI: 10.1109/LATS53581.2021.9651807. © 2021 IEEE

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- [IE-6] **L. Matana Luza**, D. Söderström, G. Tsiligiannis, H. Puchner, C. Cazzaniga, E. Sanchez, A. Bosio, and L. Dilillo, "Investigating the Impact of Radiation-Induced Soft Errors on the Reliability of Approximate Computing Systems," in *2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Frascati, Italy, Oct. 2020, pp. 1-6, DOI: 10.1109/DFT50435.2020.9250865. © 2020 IEEE



## List of Author's Publications

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- [IE-7] **L. Matana Luza**, D. Söderström, H. Puchner, R. G. Alía, M. Letiche, A. Bosio, and L. Dilillo, "Effects of Thermal Neutron Irradiation on a Self-Refresh DRAM," in *2020 15th Design Technology of Integrated Systems in Nanoscale Era (DTIS)*, Marrakech, Morocco, Apr. 2020, pp. 1–6, DOI: 10.1109/DTIS48698.2020.9080918. © 2020 IEEE

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- [IE-8] D. A. Santos, **L. Matana Luza**, C. A. Zeferino, L. Dilillo, and D. R. Melo, "A Low-Cost Fault-Tolerant RISC-V Processor for Space Systems," in *2020 15th Design Technology of Integrated Systems in Nanoscale Era (DTIS)*, Marrakech, Morocco, Apr. 2020, pp.1–5, DOI: 10.1109/DTIS48698.2020.9081185. © 2020 IEEE

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- [IE-9] **L. Matana Luza**, A. Bosser, V. Gupta, A. Javanainen, A. Mohammadzadeh, and L. Dilillo, "Effects of Heavy Ion and Proton Irradiation on a SLC NAND Flash Memory," in *2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Noordwijk, Netherlands, Oct. 2019, pp. 1–6, DOI: 10.1109/DFT.2019.8875475. © 2019 IEEE

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- [IE-10] V. Gupta, A. Bosser, **L. Matana Luza**, D. Söderström, A. Javanainen, H. Kettunen, J. Praks, K. Voss, A. Virtanen, and L. Dilillo, "Vertical Line Fault Mechanism Induced by Heavy Ions in an SLC NAND Flash," in *2019 19th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Montpellier, France, Sept. 2019. [Accepted for publication].

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- [IE-11] D. Söderström, **L. Matana Luza**, A. Bosser, T. Gil, K. Voss, H. Kettunen, A. Javanainen, and L. Dilillo, “Stuck and Weakened SDRAM Cells due to Heavy-Ion Irradiation,” in *Data Workshop in 2019 19th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Montpellier, France, Sept. 2019. [Accepted for publication].

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- [IE-12] I. Fara, **L. M. Luza**, J. Boch, G. Furano, M. Ottavi, and L. Dilillo, “Design and Implementation of a Flexible Interface for TID Detector,” in *2019 IEEE 8th International Workshop on Advances in Sensors and Interfaces (IWASI)*, Otranto, Italy, Jun. 2019, pp. 158–162, DOI: 10.1109/IWASI.2019.8791299. © 2019 IEEE

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# Nomenclature

BE	Block Error
BL	Bit Line
BSPG	Borophosphosilicate Glass
CERN	European Organization for Nuclear Research ( <i>Conseil Européen pour la Recherche Nucléaire</i> )
CME	Coronal Mass Ejections
CMOS	Complementary Metal–Oxide–Semiconductor
CNN	Convolutional Neural Network
CONV	Convolutional Layers
COTS	Commercial Off-The-Shelf
CRC	Cyclic Redundancy Check
DD	Displacement Damage
DDR	Double Data Rate
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
E-SER	Execution Soft Error Rate
ECC	Error-Correction Code
EDAC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory

## Nomenclature

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ESA	European Space Agency
FC	Fully Connected
FG	Floating Gate
FI	Fault Injection
FIT	Failure In Time
FPGA	Field-Programmable Gate Array
FRAM	Ferroelectric Random-Access Memory
GANIL	Grand Accélérateur National d'Ions Lourds
GCR	Galactic Cosmic Ray
GPU	Graphics Processing Unit
GSI	Helmholtzzentrum für Schwerionenforschung
HDL	Hardware Description Language
ILL	Institute Laue Langevin
IP	Intellectual Property
ITER	International Thermonuclear Experimental Reactor
JEDEC	Joint Electron Device Engineering Council
JUICE	JUpiter ICy moons Explorer
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LOCOS	LOCal Oxidation of Silicon
LU	Logical Unit
MBU	Multiple-Bit Upset
MCU	Multiple-Cell Upset

MLC	Multiple-Level Cell
MOS	Metal–Oxide-Semiconductor
MRAM	Magnetoresistive Random-Access Memory
MTCube	Memory Test CubeSat
NaN	Not a Number
NVM	Non-Volatile Memory
ONO	Oxide-Nitride-Oxide
PAC-G	Platform for Advanced Characterisation
PB	Page Buffer
PCB	Printed Circuit Board
pSRAM	Pseudo-Static Random-Access Memory
RADEF	RADIation Effects Facility
RES	Radiation Effects Study
RTL	Register-Transfer Level
SAA	South Atlantic Anomaly
SBU	Single-Bit Upset
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SEEs	Single-Event Effects
SEFI	Single-Event Functional Interruption
SEL	Single-Event Latch-up
SEM	Soft Error Mitigation
SER	Soft Error Rate
SET	Single-Event Transient

## Nomenclature

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SEU	Single-Event Upset
SLC	Single-Level Cell
SoC	System-on-Chip
SOI	Silicon On Insulator
SRAM	Static Random-Access Memory
TC	Test Campaign
TID	Total Ionizing Dose
UNILAC	UNIversal Linear ACcelerator
VESPER	Very energetic Electron facility for Space Planetary Exploration missions in harsh Radiative environments
VL	Vertical Line
VRT	Variable Retention Time
WL	Word Line

# Chapter 1

## Introduction

The field of radiation effects in electronics research includes unknowns for every new device, technology node, and technical development. Furthermore, it is always relevant and necessary to study the impact of radiation effects in today's devices. When designing electronic devices, the consideration of radiation effects is fundamental for applications in harsh environments. For instance, in avionics and spatial systems, these effects are extensively studied to ensure the high reliability of the system components and provide the required insight for important design decisions. Most of the radiation-related issues started to be noted at the beginning of the space era, with, e.g., the critical errors caused by cosmic ions affecting space probes of the Pioneer programs (launched in 1972 and 1973) and the Voyager (launched in 1977) [3].

Notably, as the technology nodes get smaller and components more integrated [4], testing components for radiation-induced effects becomes a growing issue. This procedure plays a crucial role in understanding the weakness of each technology, its failures mechanisms, and the mitigation techniques that can be applied. Relevant radiation effects might differ when considering different node sizes as, for instance, Single-Event Effects (SEEs) by direct ionization from protons [5, 6], which is of increasing importance for smaller technology nodes.

Besides the fact the ionizing radiation may induce effects of different kinds of components, several works have shown that memories devices are one of the highest contributors of soft errors in systems, e.g., in [7–9]. Furthermore, due to its nature, memories are capable of storing radiation-induced errors, e.g., Single-Bit Upsets (SBUs), making this kind of device the best candidate for studying soft errors.



# 1.1 Radiation Environments

Radiation is defined as the emission or transmission of energy as waves or particles, which can be ionizing and non-ionizing. The interaction between the radiation and the matter can generate different reactions, which may vary depending on the properties of the particle (type, kinetic energy, mass, and charge), and the target (semiconductors in this thesis scope). The radiation particles can be classified according to their interaction with the materials, such as (i) *photons*, which interact with matter through photoelectric effects, Compton scattering, or pair production; (ii) *charged particles*, which interact with matter through several physical processes, such as nuclear interactions, and Coulombic interactions (ionization, excitation, Bremsstrahlung); (iii) *neutrons*, which interact with matter through elastic and inelastic interactions, neutron absorption, and fission reaction [10–12]. The exposition of electronics components to environments with a significant presence of radiation may lead to these kinds of interactions, and consequently to a variety of effects that can drastically affect the electronic system reliability [13].

The radiation environments can be divided into natural and artificial environments [13, 14]. The natural environments comprise the space and the terrestrial (or atmospheric) ones. The artificial environments are, e.g., nuclear power plants and particles accelerators. Each environment is characterized by the presence of different spectra of radiation [13]. More details about each environment are described in the following subsections.

## 1.1.1 Space Radiation

The space environment, more specific, the near-Earth space radiation environment, has different sources of radiation, which can be classified into three major groups: particles originating from the sun, the Galactic Cosmic Rays (GCRs), and the trapped particles in the Earth's radiation belts, also known as Van Allen Belt [14, 15]. The radiation space environment is a major concern for any space mission, and radiation-induced anomalies in spacecraft are regularly observed. Several missions faced the radiation-induced effects on their electronic systems, e.g., the early cited space probes from the Pioneer programs and the Voyager, and the loss of the “Superbird” satellite due to a radiation-induced upset and an operator error [3].

### 1.1.1.1 Solar Particles

The solar particles are provided from the solar wind, the solar flares, and the Coronal Mass Ejections (CMEs). The occurrence of solar particle events is influenced by the cyclic

solar activity, which typically has 7 years of high activity levels and 4 years of low activity levels [3, 13]. The solar wind flows a continuous stream of protons, electrons, and heavier particles at a velocity of approximately 300 to 900 km/s, with temperature ranging from  $10^4$  to  $10^6$  K, and a density of 1 to 30 particles/cm<sup>3</sup> [3].

If from one side we have the continuous solar wind, solar flares and CMEs are random events. The solar flare is a sudden burst of energy caused by an increase in the localized energy storage in the corona magnetic fields that exceed a critical instability threshold [3, 13, 16]. CMEs are large eruptions events originating from a shock wave followed by the emission of accelerated particles at speeds varying from 50 to 2,500 km/s [3, 13, 15]. These events release energetic protons, electrons, alpha particles, and heavy ions [3, 14, 15].

### 1.1.1.2 Galactic Cosmic Rays

In the literature, it is known that GCRs originate from outside of our solar system. However, their source and mechanism are still not fully understood [17]. According to [15], their composition is protons (87%), alpha particles (12%), and heavy ions (1%), with energies up to  $\sim 10^{11}$  GeV, and a flux of 1 to 10 cm<sup>-2</sup>s<sup>-1</sup>. The interface between the heliosphere and the interstellar medium filters most of these ions, and the remaining ones interact with the heliospheric magnetic field [18]. The GCRs spectrum and flux that is observed nearby the Earth have a substantial influence on the solar activity, with the already cited 11-year solar cycle, and also a 22-year cycle, 27-day, and the solar diurnal variation, as described in [19, 20].

### 1.1.1.3 Trapped Radiation

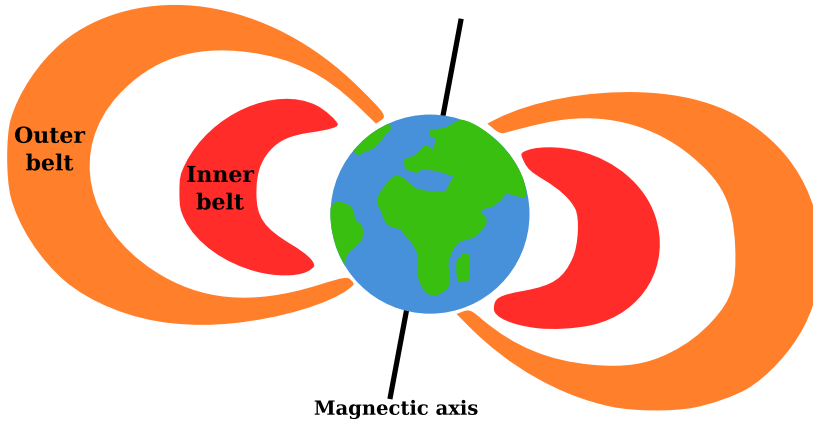
The Earth's magnetic field can deflect and trap particles coming mainly from the solar particles and GCRs. It then creates a cavity known as the magnetosphere, a dynamic structure that suffers the influence of the solar activity variations [15, 21]. The created trapped fields of radiation are known as Van Allen belts, named since its discovery was due to a Geiger counter proposed by J. A. Van Allen that was carried by the Explorer I (satellite developed by the Jet Propulsion Laboratory and launched on January 31, 1958). The counter abruptly saturated at a certain altitude, leading to this discovery [22, 23, 15].

The Van Allen belts are commonly described as two fields comprising an inner and an outer belt. Figure 1.1 [1] presents a simplified 2-D representation of its structure. The trapped particles in the belts are mainly composed of protons and electrons. However, alpha particles and heavy ions are also trapped but are normally negligible considering the spacecraft's shield systems since the ions with an energy that is high enough to penetrate these systems are very

## Introduction

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low [14]. The inner belt extends between  $1.2$  and  $2 R_E^1$ , and the outer belt extends to higher distances ( $\gtrsim 3 R_E$ ) [24]. Also, the region between the inner and outer belt is denominated “slot region” [14, 24].



**Figure 1.1** – A simplified 2-D representation of the Van Allen belts. Figure adapted from: [1].

More in details, the internal (or inner) belt is mainly composed by protons in a very stable flux of about  $10^4$  to  $10^5 \text{ cm}^{-2}\text{s}^{-1}$  and depending on the position, the energies may reach between a few MeV up to hundreds of MeV. And by electrons with also a very stable flux ( $\sim 10^9 \text{ cm}^{-2}\text{s}^{-1}$ ) and with energies of about 10 MeV, or even higher [15]. The proton belt has fluxes peak (for  $E > 30 \text{ MeV}$ ) at  $\sim 2,500 \text{ km}$  altitude at the equator. Also, the inner belt electrons fluxes peak (for  $E > 2 \text{ MeV}$ ) is at  $\sim 2,500 \text{ km}$  [14]. The external (or outer) belt is mainly composed by electrons with energies up to 7 MeV. The electron flux is much more variable, with fluxes peak (for  $E > 2 \text{ MeV}$ ) at  $\sim 20,000 \text{ km}$  [15].

An interesting observation from NASA’s Van Allen probes that are reported in [25] reveals an isolated third ring on the two rings Van Allen belts structure. It identified three radiation zones and two slot regions for electrons with energies  $\gtrsim 2 \text{ MeV}$ . This barrier persisted relatively stable in the geocentric radial range ( $3$  to  $\sim 3.5 R_E$ ) for more than 4 weeks, being after disrupted by an interplanetary shock wave passage [25, 24].

Taking into account the space missions targeting the Low Earth Orbit (LEO), a spacecraft will be exposed to trapped particles during two portions of the orbit: passing through the polar horns, and by the South Atlantic Anomaly (SAA) [15]. The polar horns consist of electrons below 1,000 km, and electrons and protons above this altitude that are encountered closer to the poles in both hemispheres. The SAA is a region centered in South America with a weak magnetic field. This magnetic field depression is caused by the  $11^\circ$  angle between the magnetic and geographic axes, causing an increase in the particle flux at lower

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<sup>1</sup>The Earth radius ( $R_E$ ) is around 6,371 km.

altitudes [3, 26]. As an example of the radiation impact on spacecraft passing through the SAA, the Hubble Space Telescope is turned off during the passage [26].

### 1.1.2 Atmospheric Radiation

The interaction between GCRs and solar particles (which, depending on angle and energy, may enter the Earth's atmosphere) with Earth's atmospheric particles through nuclear reactions result in a shower of several types of radiation [14, 27]. These secondary particles are mainly neutrons, protons, electrons, heavy ions, pions, and muons [14, 27, 28]. The maximum peak of ionization rate is at the Pfozter maximum (at  $\sim 18$  km), although, in the literature, it is pointed to variable altitude for this maximum [27, 29]. Then, the particle flux slowly drops off to sea level reaching approximately three orders of magnitude lower than the peak, which will have a dependency on the energy and the particle type [28].

The particles that reach the ground level are primarily neutrons, some protons, and few pions. The neutrons are the dominant source of soft errors in electronics at ground level [14, 30], and their effects on the context of this work are explored in Chapter 3 and Chapter 4. According to [31], the nominal integral neutron flux at ground level, New York, outdoors, for energies above 10 MeV is  $13 \text{ cm}^{-2}\text{h}^{-1}$ , and for thermal energies ( $< 400 \text{ meV}$ ), it is  $6.5 \text{ cm}^{-2}\text{h}^{-1}$ . The neutron flux increases with the altitude, being about 300 times greater at typical aircraft altitudes [32, 33]. For this reason, the neutron-induced effects, which are already significant at ground level, are a high concern, and effort is applied to understand its impact and increase the reliability of avionics systems [34].

### 1.1.3 Artificial Radiation Environments

The artificial radiation environments are generated in biomedical devices, nuclear power plants, particles accelerators, and other high-energy physics experiments [13]. Two interesting examples are the Large Hadron Collider (LHC) at the European Organization for Nuclear Research (*Conseil Européen pour la Recherche Nucléaire*) (CERN), where it is needed to carefully qualify the electronics units against radiation effects since controller systems will be affected by high radiation levels present in this environment [35]. The ionizing radiation is also present in the nuclear fission power plants, in which, e.g., in the ITER (International Thermonuclear Experimental Reactor) environment, where a large flux of neutrons, x-rays, and gamma rays impact electronics systems placed near the vessel and bio shield [13, 36].

## 1.2 Radiation Effects in Electronics

The main aspect of ionizing radiation and its interaction with electronic devices is the deposition of energy in the target material. The radiation effects are divided in three main categories: Total Ionizing Dose (TID), Displacement Damage (DD), and Single-Event Effects (SEEs) [13]. SEEs are due to an energetic particle passing through the semiconductor material transferring its energy through Coulombic interactions. The created ionized track of free electrons-holes can reach critical places on the device structure, leading to different kinds of effects, e.g., memories bit upsets, high current states, voltage transients on the circuit nodes [3, 13]. TID and DD are cumulative effects caused by the accumulation of ionizing radiation resulting in a long-term degradation of the device parameters, e.g., increase of the leakage current and shift of the transistor threshold voltage [13, 37].

### 1.2.1 Total Ionizing Dose

The TID effects on metal-oxide-semiconductor (MOS) transistors are known since the 60's [38, 37]. TID is the amount of energy deposited by the ionization processes per unit mass of material in the target material, which is measure in  $\text{rad}^2$  or  $\text{Gy}^3$ . The accumulation of the created electron-hole pairs produced by the ionizing radiation, when trapped on the oxide ( $\text{SiO}_2$ ) and interface ( $\text{Si}/\text{SiO}_2$ ) in MOS devices, can cause a significant change in the device characteristics [39].

The electron-hole pair's production depends on the electric field applied to the material during the radiation incidence. With the presence of an electric field, the electrons that have high mobility compared to the holes are dispersed away, and the holes are transported in direction to the oxide and interface regions. The electrons-holes pairs will recombine or be trapped in the oxide and interface regions. These trapped charges in the gate are capable of inducing a shift on the threshold voltage ( $\Delta V_{th}$ ), which can also increase the sub-threshold leakage current. Additionally, with the technology scaling, the gate oxide is becoming thinner, reducing the charge trapped. As a result, the thick lateral isolation and oxide spacers have become a major source of dose-related problems [13]. The channel mobility is also degraded, resulting from scattering from charges on the interface traps. In a more generic view, the variation on the device characteristics have a dependence on the mechanisms that will take place according to the device structure, materials, and working principle [10, 39–41].

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<sup>2</sup>1 rad correspond to the deposition of 100 ergs of energy in 1 gram of material.

<sup>3</sup>Gy (gray) is the international system of units (SI) equivalent of 100 rads.

### 1.2.2 Displacement Damage

The DD occurs by means of Coulombic interactions or nuclear reactions with the nuclei. This effect can be produced by impinging energetic radiation, such as neutrons, protons, heavy ions, electrons, and, indirectly, photons [13, 42]. The energy transferred during the radiation-matter interaction, when sufficiently high, can displace a nucleus from its lattice position, creating a lattice defect. These lattice defects are vacancies, the absence of an atom in its initial position, and interstitial, a displaced atom residing on a nonlattice position. A vacancy and an adjacent interstitial are known as the Frankel pair, and two adjacent vacancies are referred to as divacancy. Depending on the impinging particle mass and energy, the defects can be created either isolated or in clusters [42].

The DD effects in semiconductors are based on the energy levels introduced in the bandgap. The accumulation of this effect can lead to major impacts on the electrical and optical behavior of semiconductors. For example, in a high-level functionality view, these effects can be seen as an increase in the leakage current, lifetime decrease, and gain degradation on bipolar transistors. In general, DD effects are a significant concern for electronic devices and minority carriers, such as a bipolar transistor. For MOS transistors, it becomes to take an important place at very high particle fluences [42].

### 1.2.3 Single-Event Effects

A single ionizing particle passing through a semiconductor device loses energy through Coulombic interactions and leaves a track of free electron-hole pairs. The created excess of mobile charge carriers reaching sensitive sites of the device can lead to SEEs [3, 13]. The most sensitive parts are usually the reverse-biased p/n junctions since this region can efficiently collect chargers due to its high electric field [43].

Contrary to dose effects, which are cumulative over time, the SEEs are localized effects due to a single particle strike, causing a transient state on a device that may lead to recoverable (soft) or permanent (hard) damage. Soft errors are the ones that can be mitigated, e.g., a memory cell that has lost the information but, when rewritten, is able to store the new information. Hard errors cause irreversible physical damage, e.g., the rupture of a gate dielectric. Additionally, some errors can be classified as soft or hard, such as the Single-Event Latch-up (SEL), which can cause a hard error if a power supply cut is not performed quickly [3, 13]. Some of these events are detailed below.

### 1.2.3.1 Single-Event Upset

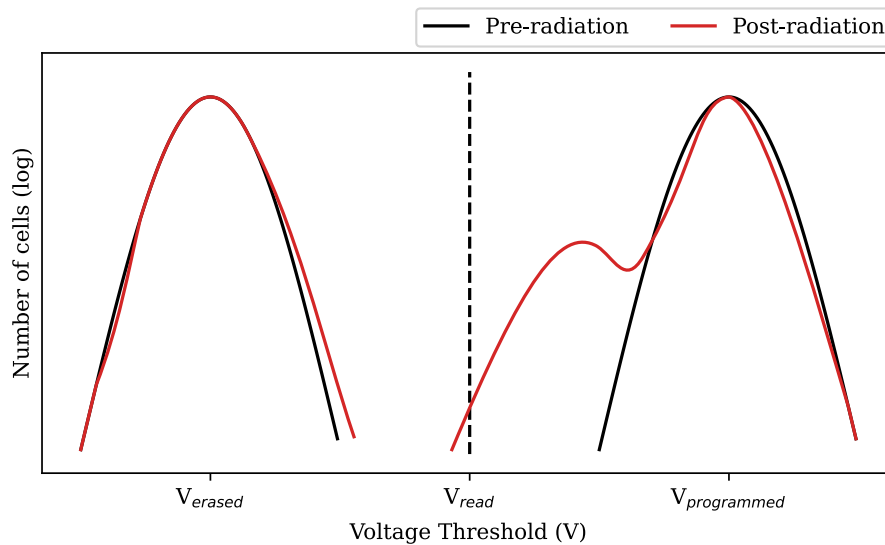
The Single-Event Upset (SEU) generally refers to the corruption of a stored memory element due to a particle strike. It can be the corruption of only one single bit in the memory array, defined as a Single-Bit Upset (SBU). The generation of bit-flips in two or more cells within the same memory word is defined as Multiple-Bit Upset (MBU), and when it is generically in the cell array, it is defined as Multiple-Cell Upset (MCU).

The mechanisms to generate an SEU have a strong dependency on memory technology. In a DRAM (Dynamic Random Access Memory), whose technology is based on a one-transistor one-capacitor cell structure, the memory information is defined by the charge stored in the capacitor. The SEU mainly occurs by a charge collection within the memory binary cell caused by a particle strike occurring in, or close to, the storage capacitor or the access transistor [43, 44]. The cell upsets occur through a charge collection by the bias junction of a cell-access transistor, increasing the charge on the storage capacitor, and by charge transfer due to a low-resistive path created by an ionizing particle, which moves electrons from a low-voltage node to a high-voltage node [45]. Also, upsets can be caused by a charge collection in the pre-charged bit line during a memory access, introducing an imbalance in the sensing signal during or before the sensing operation [43].

In Flash memories, the bit upset occurs with the introduction of a voltage threshold shift. The charges trapped in the floating gate transistors can be discharged due to the radiation interaction, which will reduce its voltage threshold. If this shift brings the threshold value to a value lower than the one to identify the correct logic value in the cell, it will then generate a fault [2]. Figure 1.2 presents an illustrative distribution of the cells voltage threshold in a Flash array before and after the radiation exposure. The mechanism that leads to these effects is not fully established. Some of them are described in [46].

### 1.2.3.2 Single-Event Transient

The free carriers path created by an ionizing particle strike may be collected by a sensitive node and cause an unexpected behavior. However, contrary to SEU, in this case, the Single-Event Transient (SET) is especially correlated to analog circuits and combinatorial logic in digital circuits. The created voltage/current transient can be propagated in the circuit, and, especially, it can be latched by a memory element resulting in a soft error. The transient should be high and long enough to be propagated in the circuit, being an issue in high-frequency circuits, since due to the fast clock, the probabilities to latch the transient is higher [13]. More related to analog circuits, it may generate, e.g., voltage pulses in the output of the operational amplifier.



**Figure 1.2** – Voltage threshold distribution of cells in a Flash memory pre- and post-radiation. The figure is an illustration based on results presented in [2].

### 1.2.3.3 Single-Event Functional Interruption

The Single-Event Functional Interruption (SEFI) is defined as a device lose of its functionality due a particle strike. This loss of functionality may be created by a change on a register that causes the device to enter in an undefined or unexpected state or any other change in critical locations of the device. For this reason, these kinds of effects, more than the others, are heavily dependent on the device design and technology [47].

### 1.2.3.4 Single-Event Latch-up

The SEL is produced by a parasitic bipolar structure in bulk<sup>4</sup> CMOS technology that is activated by an ionizing particle passage and subsequently the charge collection. The bipolar parasitic structure is a thyristor that is common in a CMOS circuit, such as a typical inverter, as shown in Figure 1.3, which presents a simplified device cross-sectional view of the structure. This parasitic structure is normally in a high-impedance state. However, the external excitation provided by the ionizing particle can force one of the transistors to enter in an on-state, creating a loop condition that leads to a high-current state on the semiconductor. The low-impedance path between the  $V_{DD}$  and  $V_{SS}$  is defined, resulting in a device malfunctioning [47, 48]. If a power cycle operation (turn off and on) is performed in the device, the latch-up effect is stopped, and the device returns to its normal operation. However, if the power cycle is not quick enough, permanent effects can be generated due

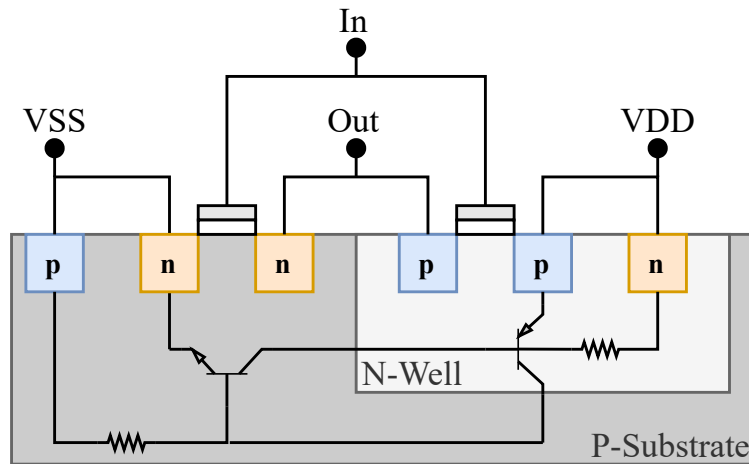
<sup>4</sup>Bulk refers to a chip that is built on a standard silicon wafer.



## Introduction

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to thermal runaway [49]. Additionally, the circuits can be protected against latch-up by employing different techniques, such as in [49]. Furthermore, the dielectric isolation of SOI circuits makes this technology immune to SEL, as described above, since it eliminates the parasitic thyristor [50]. However, as shown in [51], the *pnpn* path may be presented in some of the SOI processes (e.g., with the use of Local Oxidation of Silicon – LOCOS, as lateral dielectric), and SELs can occur.



**Figure 1.3** – A simplified device cross-sectional view of the parasitic *pnpn* structure of a typical CMOS inverter.

## 1.3 Thesis Outline

The rest of this thesis is structured as follows. Chapter 2 presents a study of the heavy-ions induced effects on a Single-Level Cell (SLC) NAND Flash. The Flash memory used in this study has been chosen to be part of the MTCube (Memory Test CubeSat) payload experiment [52]. Chapter 3 presents a study on the neutron-induced effects on a self-refresh DRAM targeting the thermal and the atmospheric-like spectra, in which an analysis on the radiation-induced degradation on the memory cells is performed. Also, high-temperature annealing is observed post-radiation test procedures. Chapter 4 presents a comparative study between three generations of the same Synchronous Dynamic Random Access Memory (SDRAM). The comparative study is based on the memory response under neutron irradiation, presenting the occurrence of SBUs and stuck-bits in the memory, showing a higher sensitivity in the oldest generation and a very similar (with some differences) result in the other two models. Chapter 5 presents an application case study, the radiation-induced effects on the reliability of neural networks, which extends the results proposed in Chapter 3. This

Chapter first presents the motivations and related works. Then, a proposed approach to assess the reliability of the Neural Networks application is proposed, followed by experimental results, which are the outcome of radiation test campaigns and the use of a software emulator. This latter allows injecting realistic fault models according to the outcomes of the actual experimental tests. Finally, Chapter 6 concludes the works presented in this dissertation.



## Chapter 2

# Study of Single-Event Upsets in a Single-Level Cell NAND Flash Memory

This Chapter presents contents based on the author's publications [IE-9] and [IE-10].

This Chapter introduces the results of radiation test campaigns with heavy ions on an SLC NAND Flash memory. This study was driven by the MTCube project [52], and its related results were also already presented in part in two thesis dissertations of the research group: Gupta [53], and Bosser [54]. The results revealed different failure mechanisms, including Single-Event Upsets, small clusters of errors, data register upsets, and a column-wise failure mode. Cross section was calculated for each of these failure modes, and their causes were discussed. Characterization of effects on the data registers embedded in the device is also performed. In relation with the outcomes presented in [53, 54], this Chapter represents an advancement of this study since it provides further results obtained from two supplementary irradiation test campaigns made with complementary heavy-ion species and energies. In this direction, the behavior analysis of the column-wise failures was extended, and cross sections were recalculated with also the addition of data coming from dynamic test mode. An overall discussion of the impact of the events is also introduced, presenting the ratio of event type for different test points and a raw error cross section, which provides a perspective from a user point of view.

### 2.1 Flash Memories

The Flash memory is a type of EEPROM (Electrically Erasable Programmable Read-Only Memory) based on a single Floating Gate (FG) transistor cell [55, 56]. This technology

has taken an important role in the semiconductor non-volatile memory market, with an aggressively scaling down trend [46]. Compared to other NVM (Non-Volatile Memory) technologies, Flash memory suffers from poor access latency (in the order of microseconds) and read/write speed, as well as low endurance due to gate oxide degradation during cell programming and erasure. However, since each memory cell is made up of only one transistor, Flash technology enables extremely high storage density and low cost-per-byte, which has made it the technology of choice for mass data storage also in the spatial context. As rest of the Chapter will introduce the basics of Flash memory technology and the radiation-induced effects on this device. Also, it will be present a study on the heavy-ion radiation impact on a Flash device that is part of the MTCube [52]. The MTCube has a primary objective to develop, test, and fly different commercial memories and assess their sensitivity to the space environment by comparing their behavior in space with accelerated radiation testing and simulations [52].

### 2.1.1 Cell Structure and Memory Architecture

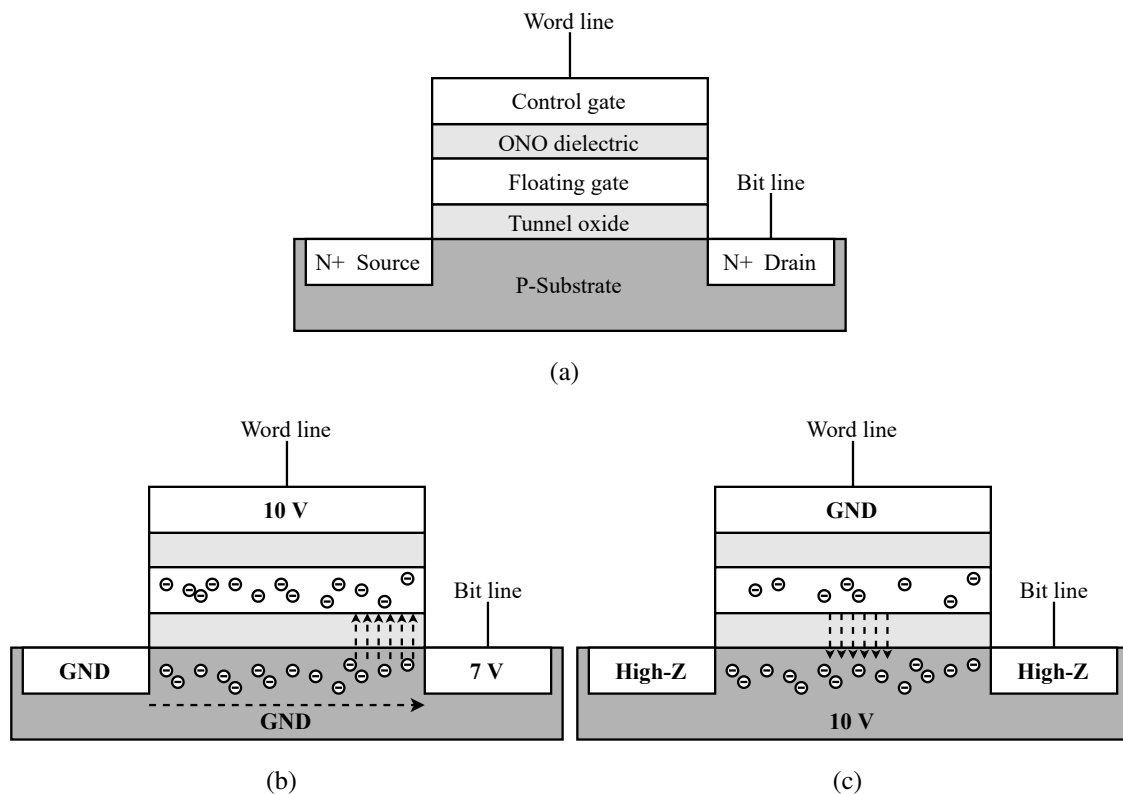
The Flash cell structure is depicted in Figure 2.1(a). The technology is based on the capacity of storing charges in the FG. The FG is made of polysilicon and is surrounded by two oxides. A control gate oxide, which usually an ONO (Oxide-Nitride-Oxide) stack, and a thin tunnel oxide. The dielectrics enable the non-volatility of the stored charge in the floating gate by acting as potential barriers, but at the same time, they enable the possibility of the electrical-induced charge and discharge of the FG [2, 53, 56].

The Flash memory has three types of operations: (i) program, (ii) erase, and (iii) read. The process for program and erase the memory cell consists of injection or removal of electrons in/from the FG by two main mechanisms:

1. **Channel hot electrons** is used to program the cell, and it injects electrons over the potential barrier of the tunnel oxide. By turning on the gate and the drain, a lateral field close to the drain terminal is created, and the electrons that flow through the channel gain enough energy to pass over the tunnel oxide and get trapped in the FG [2, 53, 56]. Figure 2.1(b) depicts this mechanism.
2. **Fowler-Nordheim tunneling** is used for both program and erase, and it is done by applying a strong electric field between the gate and the substrate. For programming, the control gate receives a high voltage while the substrate is kept at 0 V. As a result, the electrons are able to tunnel through the tunnel oxide and reach the FG. Conversely, erase the FG is performed by setting a high voltage in the substrate and 0 V in the

control gate, and then, the electrons can tunnel back to the substrate [2, 53, 56]. Figure 2.1(c) depicts the mechanism for the erase process.

Both mechanisms are able to change the amount of charge that is stored in the FG, and these variations in the charge affect the voltage threshold ( $V_{th}$ ) of the transistor. By convention, in SLCs Flash memories, when the FG is charged, i.e., electrons are trapped in the FG, it corresponds to the logic '0' and the transistor  $V_{th}$  increases. Furthermore, the opposite, i.e., when the FG is discharged, corresponds to the logic '1', and the transistor  $V_{th}$  is lowered [2, 53, 56]. The read operation is based on this idea, an intermediate voltage with a voltage level between the  $V_{th}$  for an erase and a programmed state is applied to the control gate, and the state of the cell is identified by measuring the drain current ( $I_{ds}$ ).

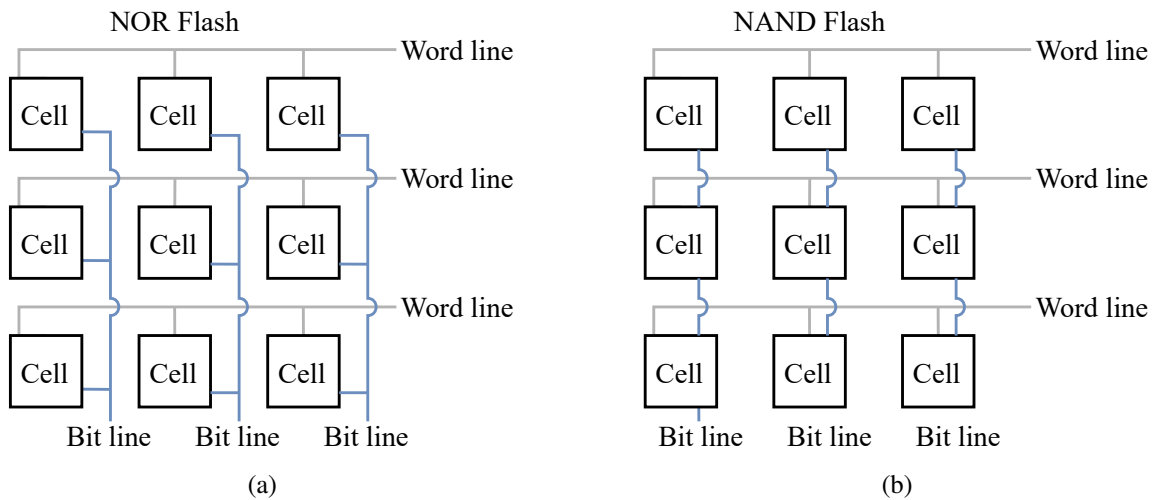


**Figure 2.1** – (a) Flash memory cell structure, (b) channel hot electrons program mechanism, and (c) Fowler-Nordheim tunneling erase mechanism.

Besides the cell structure, Flash memories have two main architectures: NOR and NAND. The NOR organization provides random access to words, which means that each memory cell is independently connected to word lines and bit lines, which provides a fast read operation at the cost of a small memory cell density, which makes this type of memory very suitable for read-mostly memories, e.g., for code storage. Conversely, the NAND architecture connects

## Study of Single-Event Upsets in a Single-Level Cell NAND Flash Memory

the memory cells in series, enabling a high memory cell density with a good serial access time. However, random access is inhibited by the architecture. The NAND organization is more suitable for data storage since the memory can achieve very high storage density [2, 53]. Figure 2.2 presents a simplified high-level view of both architectures.



**Figure 2.2** – A simplified high-level view of the architecture of NOR (a) and NAND (b) Flash memories.

## 2.2 Radiation Effects on Flash Memories

The FG technology and the peripheral circuitry used in the NAND Flash architecture are susceptible to radiation effects [57]. Besides, technology scaling to deep sub-micron levels has increased these memories' susceptibility to SEEs. Since Flash memory cells rely on electric fields and charge trapping, they are inherently sensitive to ionizing radiation: when a charged particle goes through a charged floating gate, it can induce its discharge, thus corrupting the stored information [2]. This failure mechanism, called SEU, is a major concern for space applications, where high radiative environments can lead to rapid accumulation of errors in Flash devices, beyond the mitigation capability of Error-Correction Codes (ECCs). Furthermore, the peripheral circuitry of Flash devices, which is used to access, read and write to the memory array, is manufactured by using CMOS technology, which is also sensitive to various SEEs [58].

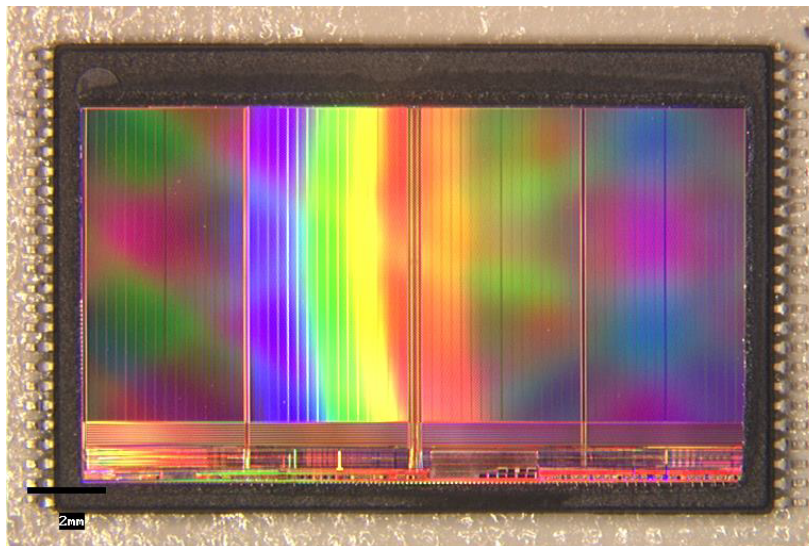
NAND Flash devices have been extensively tested using different sources of radiation, such as in [59] and [60]. Proton-induced effects and their sensitivity in SLC and MLC (Multiple-Level Cell) devices are approached in [61]. In [62] the authors compare the effects

of electron irradiation with results from  $^{60}\text{Co}$  TID measurements. The SEE dependence on heavy-ion fluence is investigated in [63]. Besides these ones, other studies have been published regarding failure mechanisms in the peripheral circuitry such as the charge pump [64], and the contribution of the Page Buffer (PB) and the duration of data storage in this buffer to the overall upset rate [65]. Finally, [66] presents three different types of permanent effects under heavy-ion irradiation in the same SLC NAND Flash memory as the present work; these failures are non-recoverable with a simple power cycle.

## 2.3 Experimental Setup

### 2.3.1 The Device Under Test

The memory tested in this study is the MT29F32G08ABAAA, a 32 Gib Asynchronous SLC NAND Flash memory manufactured by Micron Technology. The Device Under Test (DUT) nominal operating voltage is 3.3 V, and the memory consists in one Logical Unit (LU), which is divided into two planes of 2,048 blocks each. A block is composed of 128 pages, each page is divided into 8,192 columns, and each column stores one 8-bit word. All specimens were delidded via chemical means for the irradiation test campaigns and passed functional tests, ensuring that all the memories were fully operational before the irradiation. Figure 2.3 presents a top-down photograph of the delidded device.



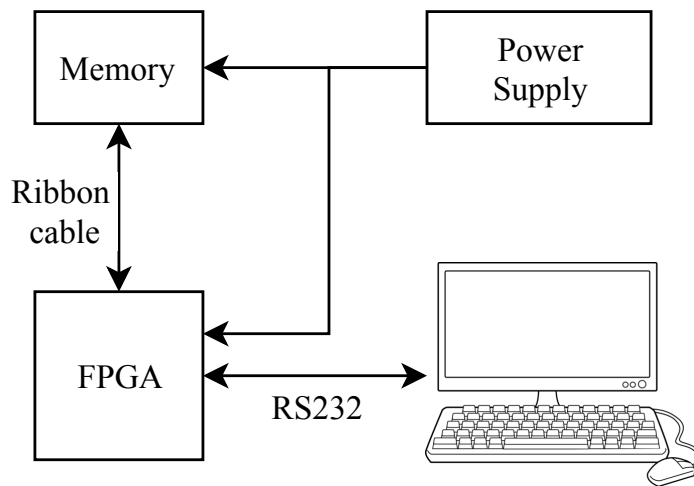
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**Figure 2.3** – Top-down photograph of the SLC NAND Flash.



### 2.3.2 Test Setup

The test setup is described in Figure 2.4, where the DUT is placed on a daughterboard that is connected to a motherboard featuring an FPGA-based controller. The controller system is connected to a host computer to provide the capability to send commands to perform different functions on the DUT (e.g., read and write operations), and to store the received log data with operation status and bit error data. The controller part was not exposed to radiation sources to ensure the reliability of the tests.



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**Figure 2.4** – Schematic of the experimental set-up for radiation testing of memories.

### 2.3.3 Test Modes

The memory devices were tested under four different modes: *unbiased static mode*, *biased static mode*, *dynamic mode* and *static data register mode*. The biased and unbiased static mode tests consist of a write operation using a known data pattern (i.e., solid ‘0’, solid ‘1’, and checkerboard patterns), followed by the irradiation of the device. Subsequently, the memory is read back, and corrupted bits are identified. For the unbiased test, the memory power supply is cut during irradiation. In dynamic read mode, the memory was written with a solid ‘0’ pattern, then irradiated while being read continuously. The *unbiased static mode*, *biased static mode* and *dynamic mode* target the memory controller and cells.

The static data register mode targets the memory data register. This test consists of writing one page of the memory with a checkerboard or a solid ‘1’ pattern. Then, instead of reading the memory, the sequence command was interrupted in order to keep the data stored

on the data registers. Subsequently, the memory was irradiated, and a reading operation was finally performed to check the data register.

Considering that the memory has a large capacity, the static tests considered 512 Mib (64 block) out of 32 Gib, and the dynamic was applied in 8 Mib (1 block). Several erase, write, and read operations were performed between test runs, before and after power cycles. This procedure was applied to ensure that the memory was error-free and fully functional before the next run.

### 2.3.4 Test Facilities

This study is based on several test campaigns (TC) with heavy ions. The first TC took place at GANIL (*Grand Accélérateur National d'Ions Lourds*) (Caen, France). The test was carried out using a xenon beam with an LET (Linear Energy Transfer) in silicon of 26.75 MeV.cm<sup>2</sup>/mg at the DUT surface at normal incidence. GANIL provided the values displayed in Table 2.1.

The second TC was carried out by using the broad beam of the RADiation Effects Facility (RADEF) at the University of Jyväskylä, Finland. Tests were performed on several specimens in vacuum, with LETs at the DUT surface ranging from 1.8 to 60.0 MeV.cm<sup>2</sup>/mg. On most test runs, the beam incidence was normal to the DUT, but sometimes the DUT was tilted to yield a higher effective LET:

$$LET_{\text{eff}} = \frac{LET}{\cos\theta} \quad (2.1)$$

The values given in Table 2.1 were calculated with the tool SRIM [67].

The third TC was carried out on a single specimen at GSI Helmholtzzentrum für Schwerionenforschung (GSI), using the UNILAC (UNIversal Linear ACcelerator) microbeam. Only one type of particle was used (calcium at 230.4 MeV at normal incidence), yielding a surface LET in silicon of 15.6 MeV.cm<sup>2</sup>/mg (calculated using SRIM). Areas of interest on the die were identified with the aid of a colinear microscope, then selectively irradiated.

In the GANIL and RADEF, the devices were irradiated and tested using test sockets. Due to the geometry of the GSI microbeam facility, test sockets could not be used, so the DUT was directly soldered on a PCB (Printed Circuit Board) during this TC. The specimen irradiated at GSI had previously been irradiated with a broad muon beam, accumulating a total ionizing dose of about 5.5 krad; nevertheless, the device was fully functional at the start of the GSI campaign.

Furthermore, in order to correlate the used radiation sources with the expected in a space mission, Figure 2.5 represents the LET spectrum of all particles encountered over one year around solar minimum on an orbit at a 600 km altitude and 98.7° inclination (this includes

**Table 2.1** – Facilities and beams used for heavy-ion irradiation.

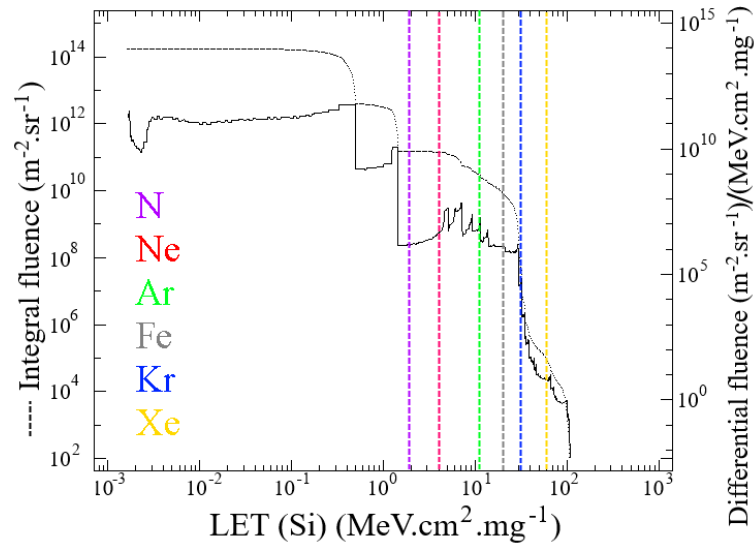
Facility	Ion	Energy (MeV)	Effective LET (@ DUT surface) (MeV.cm <sup>2</sup> /mg)	Range to Bragg peak in Si (μm)
GANIL	Xe	6005	26.75	700
	N	139	1.8 (0°) and 2.1 (30°)	202
	Ne	186	3.6 (0°) and 4.2 (30°)	146
	Ar	372	10.1 (0°) and 11.7 (30°)	118
	Fe	523	18.5 (0°) and 21.4 (30°)	97
	Kr	768	32.1 (0°)	94
	Xe	1217	60.0 (0°) and 69.3 (30°)	89
GSI	Ca	230.4	15.6	55

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solar energetic particles, trapped particles, and galactic cosmic rays) calculated using AP8, SAPHIRE, CREME96, and ISO-15390 models via SPENVIS [68]. This illustrates that the ions used in these experiments are representative of the most ionizing particles in the low Earth orbit radiation environment; while relatively rare, these particles are the most likely to induce errors in electronic devices.

## 2.4 Results and Discussion

The data that were acquired from the various test campaigns were post-processed and the following subsections describe the effects according to the test mode where the occurrences were identified. In Subsection 2.4.1, the effects under biased and unbiased static mode and also in dynamic mode are described. It was identified three different types of faults: isolated SBUs, cluster of word errors (multiple-cell upsets, or MCUs), and vertical lines (VLs) of word errors. Also, in Subsection 2.4.2 it is described the effects for the data register tests, where it was identified two different types of faults: SBUs and resets in the data register.



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**Figure 2.5** – LET in silicon of particles accumulated over one year around solar minimum on a 600 km orbit with  $98.7^\circ$  inclination and calculated using AP8, SAPHIRE, CREME96, and ISO-15390 models via SPENVIS. The dashed colored lines indicate the LETs of ions used at RADEF, for comparison.

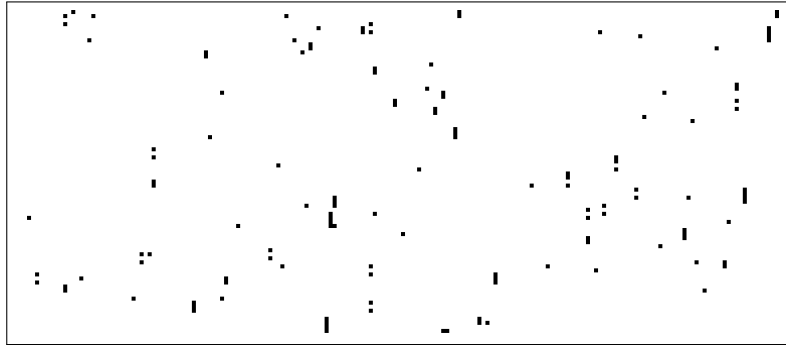
## 2.4.1 Static and Dynamic Mode

### 2.4.1.1 Single-bit Upsets and Small Clusters

The simplest observed failure mode consists of SBUs, which were detected with nitrogen (LET  $1.8 \text{ MeV.cm}^2/\text{mg}$ ) in only a few biased and unbiased static tests using a solid ‘0’ pattern and with neon and all heavier ions (LET 3.6 to  $60 \text{ MeV.cm}^2/\text{mg}$ ) in all tests (bias and unbiased static as well as dynamic test modes) using a solid ‘0’ pattern.

The small clusters (MCU clusters) occurred as single or double upsets in sequential pages of the same block and column, presetting the same data error pattern. The small clusters were observed with a maximum of 10 sequential, where the largest clusters were observed in xenon test data.

Figure 2.6 presents, among also SBUs, examples of the small clusters. Additionally, a detailed example is presented in Table 2.2, where after a test using a solid ‘0’ pattern, the readback and check operation identified four faulty bits with the same data pattern in the same block and column, varying the page address consecutively. This failure type started to appear at an LET of  $10.1 \text{ MeV.cm}^2/\text{mg}$ , but did not appear when using a neon beam at a  $30^\circ$  incidence angle (yielding an effective LET of  $4.2 \text{ MeV.cm}^2/\text{mg}$ ), suggesting that the threshold for the occurrence of MCU clusters is between 4.2 and  $10.1 \text{ MeV.cm}^2/\text{mg}$ .



**Figure 2.6** – Close-up on a bitmap generated after a static test with xenon using a solid '0' pattern, showing multiple MCU clusters. Each pixel represents one word; pixels are white if the data read was correct, and black if the word contained at least one upset. Words on the same row all belong to the same page, and words on the same column all belong to the same column. All these words belong to the same block.

**Table 2.2** – Example of a read back check operation identifying a cluster of word errors. Values are presented in hexadecimal.

Block	Page	Column	Data Read
26	60	0D63	02
26	61	0D63	02
26	62	0D63	02
26	63	0D63	02

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The NAND architecture enables a very high-density memory array, which in the case of the DUT, is composed of 32 Gib. In this light, as also proposed in [53, 54], a single particle can lead to this kind of fault. Charge sharing and secondary particles generated at angles can possibly create this pattern of errors. In this case, since only vertical shapes were observed, it would be necessary to consider insulating spacers to separate the columns. Both SBUs and small clusters were only observed when the faulty bit stored the logic '0'. Commonly, a charged floating gate is used to identify the logic '0'. The charges trapped on the floating gate play a role in the transistor voltage threshold (used to determine the stored data in the cell). The radiation can lead to a gradual discharge of the floating gate, creating a possible faulty cell. A discharged floating gate, used to represent the logic '1', will not be impacted by this process. These results were also found, e.g., in [59].

Additionally, it was also observed that some cells presented borderline behavior. This behavior was identified by fluctuations in the number of errors during sequential read operations performed after the irradiation runs. The radiation-induced shift in the transistor

voltage threshold can bring a cell to an intermediate value very close to the voltage level used to determine the logic value stored in the cell, which can lead to intermittent errors [53, 65].

The estimated cross section ( $\sigma$ ) is defined as

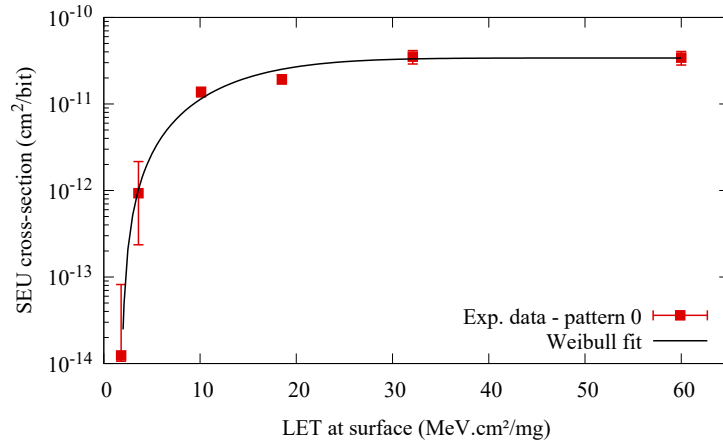
$$\sigma = \frac{N}{F \times M} \quad (2.2)$$

where  $N$  is the number of failing words or events,  $F$  is the beam fluence in particles/cm<sup>2</sup>, and  $M$  is the memory size [3]. The SEU cross section was fitted using the 4-parameter cumulative Weibull function

$$\sigma(LET) = \sigma_{SAT} \left( 1 - \exp \left[ - \left( \frac{LET - LET_{th}}{W} \right)^s \right] \right) \quad (2.3)$$

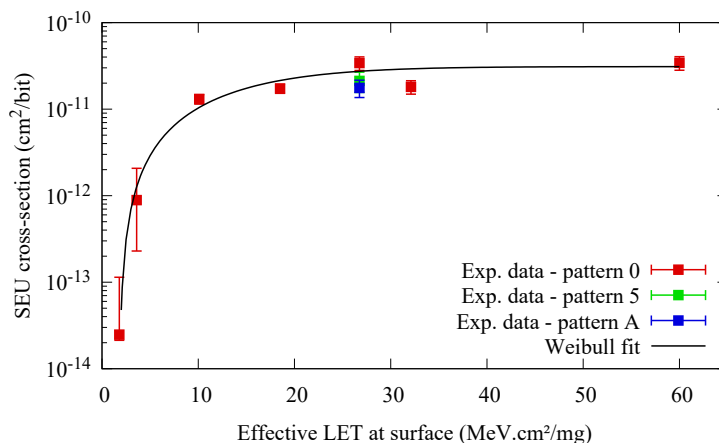
where  $\sigma_{SAT}$  is the saturation cross section,  $LET_{th}$  is the LET threshold,  $W$  and  $s$  are the width and shape parameters of the Weibull distribution [69, 70].

During unbiased static mode tests, SBUs and MCU clusters were identified in a pattern similar to that presented in Figure 2.6. The SEU cross section for SBUs and clusters is presented in Figure 2.7.



**Figure 2.7** – SEU cross section of SBUs and clusters in the memory array in unbiased mode calculated according to Equation 2.2. The error bars indicate the 95% confidence interval. The LET threshold was guessed at 1.8 MeV.cm<sup>2</sup>/mg in order to fit the data with a Weibull curve. The Weibull parameters used are:  $W = 14$ ,  $S = 1.7$ ,  $\sigma_{sat} = 3.4 \times 10^{-11}$  cm<sup>2</sup>/byte,  $LET_{th} = 1.8$  MeV.cm<sup>2</sup>/mg.

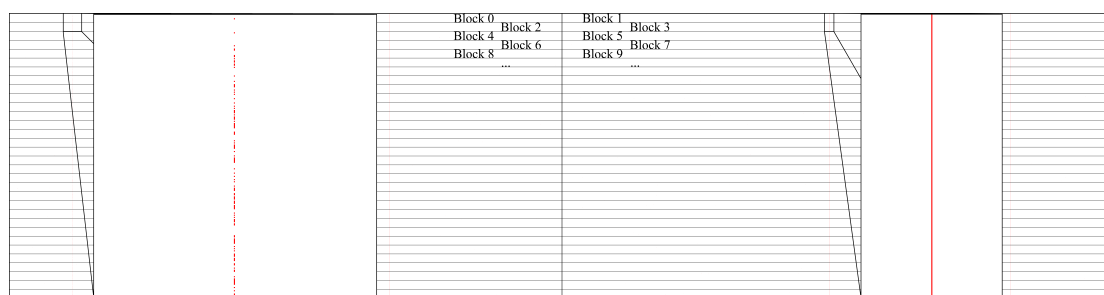
Also, in order to plot the biased static SEU cross section for the SBUs and the MCU clusters, the VLs were first filtered, and each isolated SBU or MCU cluster was treated as one SEU. The resulting cross section is depicted in Figure 2.8.



**Figure 2.8** – SEU cross section of SBUs and clusters in the memory array in biased mode calculated according to Eq. 2.2. The error bars indicate the 95% confidence interval. The LET threshold was guessed at 1.8 MeV.cm<sup>2</sup>/mg in order to fit the data with a Weibull curve. The Weibull parameters used are:  $W = 15$ ,  $S = 1.5$ ,  $\sigma_{sat} = 3.1 \times 10^{-11}$  cm<sup>2</sup>/byte,  $LET_{th} = 1.8$  MeV.cm<sup>2</sup>/mg.

### 2.4.1.2 Vertical Lines

From the acquired data, a failure mode creating vertical lines of errors was observed. Individual VLs occur within a single memory plane; they span all the blocks within the plane (meaning they affect either all the even blocks, or all the odd blocks), and affect only the words of a single column. Several VLs affecting different columns may occur at once during a test over one or both planes. VLs can be seen on the bitmap in Figure 2.9, computed using data from a static test with xenon at GANIL.



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**Figure 2.9** – Bitmap obtained after a static irradiation at GANIL, using xenon and a solid ‘0’ pattern. Each pixel represents one word; words appear as a red pixel if they suffered at least one bit upset and white otherwise. Black lines are overlaid on top of the image to indicate block limits; each block is made of 128 pages (lines) of 8,192 columns each. Zoom-ins are added to enhance the visibility of parts of an intermittent VL (left) and of a continuous VL (right). Both VLs span the whole height of the bitmap.

When considering test runs carried out with a broad beam, VLs did not occur in unbiased static mode. In static tests (with both solid '1' and '0' patterns) and dynamic tests, VLs did not occur at an effective LET of 4.2 MeV.cm<sup>2</sup>/mg (neon irradiation at 30°), but they did occur at an effective LET of at least 10.1 MeV.cm<sup>2</sup>/mg (argon irradiation at normal incidence). Hence, the LET threshold for the appearance of those VLs is somewhere between these two values.

Vertical lines may either be continuous (with all words of the column exhibiting bit errors) or discontinuous (with sparse word errors along the column). Within a VL, the affected words tend to share the same data pattern. To be more precise, most data bit positions have identical values across all the words of a given VL, although the value of one or two-bit positions may fluctuate randomly.

Unlike SEUs, VLs persist when attempts are made to overwrite the erroneous data. Furthermore, the set of columns presenting VLs and the error pattern of the interested words is affected by write and erase operations and power cycles.

However, erase operations alone, or power cycles alone are not sufficient to eliminate a VL. Indeed, in most cases, VLs persist after several erase operations or several power cycles and only disappear when the device is overwritten after both an erase operation and a power cycle were applied, regardless of the order. In a few rare instances, VLs were found to disappear spontaneously.

Table 2.3 illustrates the behaviour of vertical lines observed after a biased static irradiation at RADEF, using xenon at a normal incidence (LET 60 MeV.cm<sup>2</sup>/mg). This behavior is typical of observations made on other test runs.

As can be seen from Table 2.3, the device was written with a solid '0' data pattern, then irradiated with xenon, and read back (operation "W0, irrad, R0"). The memory plane #1 initially exhibited five VLs, at column positions 571, 1595, 3775, 4290, 6701. The error pattern was consistent within each VL (give or take one or two-bit positions), and differed from VL to VL. The device was then erased, and the data was read (first "E, R1" operation). Among the previously observed VLs, only those at positions 3775 and 6701 remained, but their error patterns were completely modified. The remaining VLs had seemingly vanished. Following that, the device was again written with a solid '0' pattern, and its data was read (first "W0, R0" operation). The original set of five VLs reappeared, each one with its original error pattern. Power supply to the device was then cycled, after which its data was read (first "Power Cycle, R0" operation). A slightly different set of VLs was now observed, at positions 571, 1595, 3775, 6338, 6701, and every word of each VL had all bits set to '1' (0xFF). Power supply to the device was cycled again, and its data read again (second "Power Cycle, R0" operation), with exactly the same results. Finally, the device was erased, its data



## Study of Single-Event Upsets in a Single-Level Cell NAND Flash Memory

**Table 2.3** – Hexadecimal data values in vertical lines observed on plane 1 during a static solid ‘0’ test. ‘-’ means correct data.

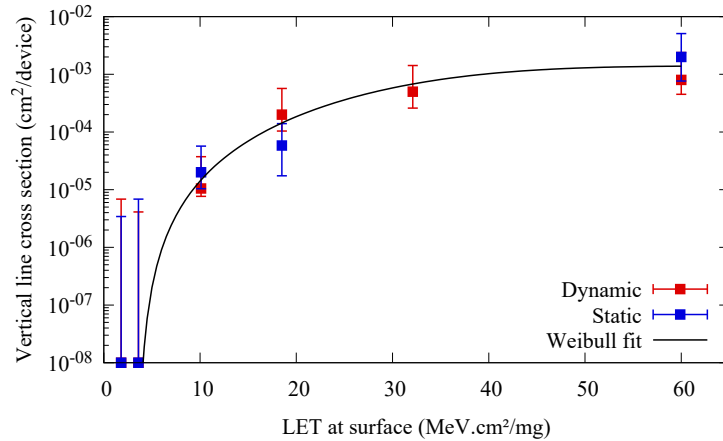
Operation	VL Column Address					
	571	1595	3775	4290	6338	6701
<b>W0, irradi, R0</b>	24/26	24/26/34	2	8B/9B	-	4/14/34
<b>E, R1</b>	-	-	E2/E3/E6/E7	-	-	7D
<b>W0, R0</b>	24/26	24/26/34	2	8B/9B	-	4/14/34
<b>Power Cycle, R0</b>	FF	FF	FF	-	FF	FF
<b>Power Cycle, R0</b>	FF	FF	FF	-	FF	FF
<b>E, R1</b>	-	-	-	-	-	-
<b>W0, R0</b>	-	-	-	-	-	-

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read (second “E, R1” operation), and all words at last contained the expected data (0xFF). The device was written with a solid ‘0’ pattern, and the data was read (second “W0, R0” operation). Only returned two isolated single-bit errors - these are believed to be due to actual cell damages.

The cross section for VL occurrence for the whole device as a function of effective ion LET is displayed on Figure 2.10; these were calculated using the data from the RADEF test campaign. The static and dynamic cross sections are reported separately. While static tests are carried out on memory blocks from both memory planes, dynamic tests are only carried out on one block; since each VL only affects one memory plane, the dynamic device cross section was extrapolated by doubling the cross section observed from the only memory plane which was used during the dynamic tests.

Once the VL failure mode was observed, it was set to identify its origin on the die by using the GSI microprobe facility. The DUT was subjected to a dynamic read test, in which a solid ‘0’ data pattern was first written, then read constantly under irradiation. Figure 2.11 exhibits

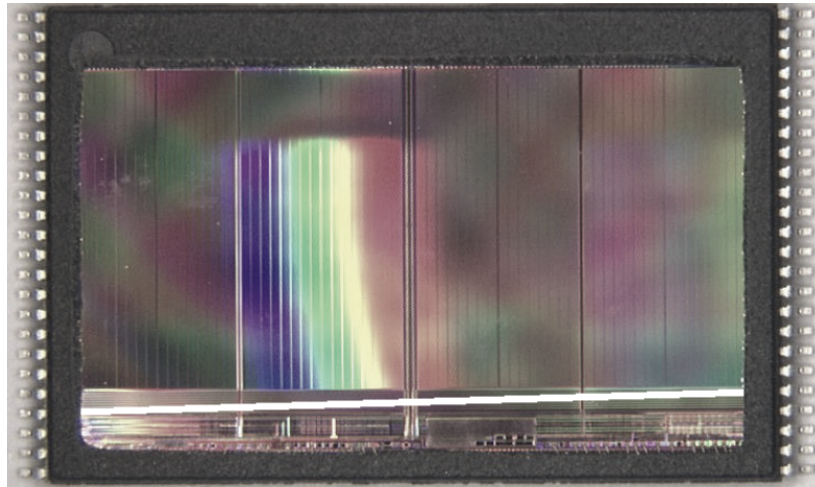


**Figure 2.10** – Device cross section for vertical lines as a function of effective LET. The dynamic cross section is extrapolated from a single memory plane to the whole device. The error bars indicate the 95% confidence interval. Below 10 MeV.cm<sup>2</sup>/mg, no VLs were detected, so the cross section was arbitrarily set to  $1.0 \times 10^{-8}$  cm<sup>2</sup> for these data points. The Weibull parameters used are:  $W = 33$ ,  $S = 2.8$ ,  $\sigma_{sat} = 1.40 \times 10^{-3}$  cm<sup>2</sup>/byte,  $LET_{th} = 3.6$  MeV.cm<sup>2</sup>/mg. Data taken from the RADEF test campaign.

a photograph of the DUT die; in two occasions, and only when irradiating the area identified by the frame, the DUT exhibited VL failure mode. This area was identified by Gerardin *et al.*, who studied the same device, to contain the page buffers and sense amplifiers [66].

From the results, as presented in [53, 54], one assumption of the failure mechanism would be a stuck bit in the data buffer. The target Flash memory uses a data buffer to perform a read operation. In this procedure, the contents of a page are loaded to the data buffer, and then the user can access the contents using the memory interface. A stuck bit on the data buffer could lead to the vertical shape of errors, which would be repetitive in each page and could generate the shape and extension of the VL. However, since the VLs appeared with fluctuations in the data pattern and an erase operation and a power cycle are necessary for the recovery, this assumption is not fully supported. Another possible mechanism would be a failure in the controlling system of the related column involved in the reading operation. The bit line may have its access inhibited by a micro-latch-up and charges trapped on the access transistor of the bit line [65]. This mechanism would explain the VL shapes since all the accesses to the related column will be affected. Additionally, the recovery options comprehend a power cycle that stops the micro-latch-up and an erase operation that restores the access transistor.

This failure mode has the potential to cause large-scale data corruption because it affects word columns across entire memory planes and cannot be resolved by simply overwriting erroneous data. The most straightforward mitigation strategy for the end-user is to cycle power the device and erase all blocks in the affected plane, which inevitably leads to data loss.



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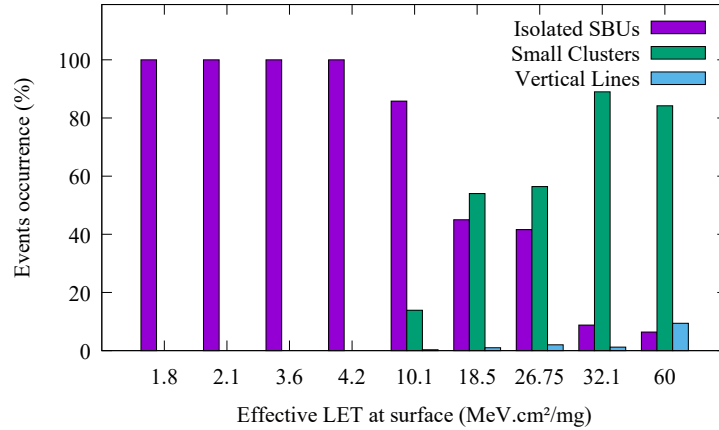
**Figure 2.11** – Top-down photograph of the specimen irradiated at GSI. The narrow, oblique white band represents the area where the beam was scanned when VLs were observed.

While this strategy is impractical for applications where the device cannot be erased, other applications in high-radiation environments which use Flash memories for temporary data storage could benefit from regularly “flushing” these devices (performing an erase and power cycle). For long-term data storage, the user may apply duplication of the data in separated topological areas of the memory array. This configuration is resource-consuming since it needs a double amount of memory space, but it may reduce to statistically insignificant the data loss since a concurrent error in two locations is statistically irrelevant. In order to refine this solution, it will be needed the introduction of detection codes, e.g., CRC (Cyclic Redundancy Check), to spot the corrupted data. Moreover, the data duplication may be restricted to only sensitive data to reduce the resource overhead. Targeting the micro-latch-up mechanism, technologies such as SOI, triple well, and guard ring can protect the system from SELs [50, 51], and consequently, avoid the occurrence of the vertical lines events.

### 2.4.1.3 Events Impact and Discussion

Complementing, Figure 2.12 presents a ratio between the occurrence of an event type by the total number of events in a determined LET using the data of the biased static mode. Only isolated SBUs occurred for LETs under  $4.2 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ . For higher LETs, the three different types of events appeared. Small clusters started to become more frequent than the isolated SBUs with the LET increase, showing that particles with a higher linear energy transfer are capable of upsetting more cells. In summary, it shows a predominance of isolated SBUs for lower LETs, on the contrary, small clusters are the predominant fault on higher

LETs, and there is an increase in the VLs with the increase of the LET. These outcomes may lead to a correlation between not just the number of events but its kind with the space environment.



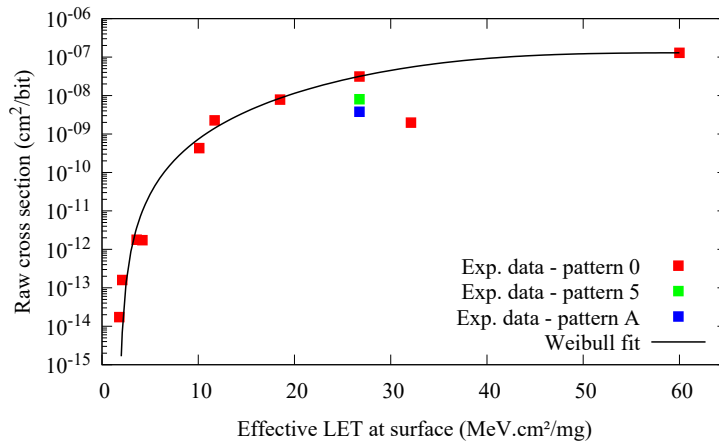
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**Figure 2.12** – Ratio of event type occurrence for different LETs in biased mode.

Furthermore, for an application point of view, it is interesting to evaluate the number of identified errors regardless of the event that caused them. Figure 2.13 presents the raw error cross section in biased static mode, counting each bit in error without performing any clustering (useful for computing the event cross section), in this case, the number of events  $N$  is equal to the number of upset bits. The cross section presented in Figure 2.13 show the same behavior for a LET up to 4.2 MeV. For LETs from 10.1 MeV upwards, since the events that imply a considerable quantity of errors (such as the VLs) start to occur, the raw error cross section results in a higher order of magnitude.

Isolated SBUs and clusters of errors (MCUs) were identified in the Flash cell array; some of the affected words exhibited a fluctuating data pattern in consecutive read operations, exposing recoverable threshold voltage shifts due to trapped charges [65]. Since the words affected by MCU clusters all belong to different pages, MCU and MBU events upset at most one 8-bit word per page, which itself should not be sufficient to overload an ECC implementation, that is highly recommended, and, according to the DUT datasheet, should be implemented with a minimum 8-bit ECC per 540 bytes of data. A danger of data corruption exists, however, if severe error pile-up occurs in the device.

Regarding to the vertical lines of errors. Schmidt *et al.* and Oldham *et al.* reported comparable *Vertical Errors* in a study of SEE occurrences in Micron NAND Flash [59, 71]. However, it has been assumed that, so far, no study reported any detail on this failure mode



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**Figure 2.13** – Raw error cross section calculated by dividing the number of bit errors by the fluence and the tested memory size (i.e., 512 Mib). The LET threshold was estimated at 1.8 MeV.cm<sup>2</sup>/mg in order to fit the data with a Weibull curve. The Weibull parameters used are:  $W = 36$ ,  $S = 3.5$ ,  $\sigma_{sat} = 1.3 \times 10^{-7}$  cm<sup>2</sup>/byte,  $LET_{th} = 1.8$  MeV.cm<sup>2</sup>/mg.

(dependence on data pattern, persistence, resilience to erase operations or power cycles, and origin of the fault within the device).

### 2.4.2 Static Data Register Test

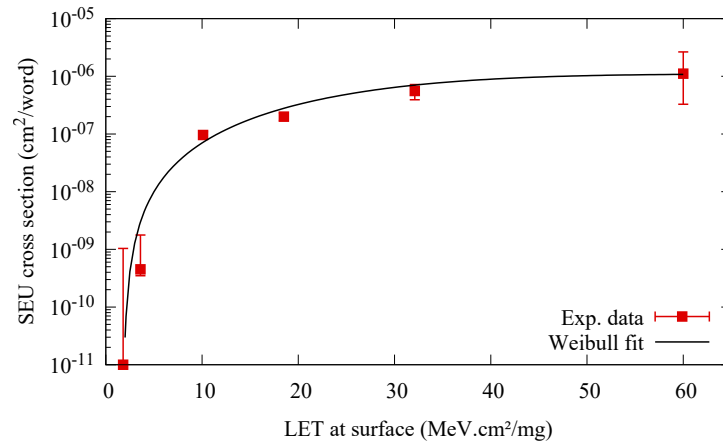
During this part of the study, a checkerboard or a solid pattern was written on one page of the memory. Then, instead of reading the memory, the sequence command was interrupted in order to keep the data stored on the data registers. Subsequently, the memory was irradiated, and a reading operation was finally performed to check the data register.

This test mode was carried out at effective LETs ranging from 1.8 up to 60 MeV.cm<sup>2</sup>/mg. The results presented two different types of faults. The first was sparse SBUs occurring randomly in the data register. The second was characterized by all words failing in the data registers (i.e., 8,192 words).

Concerning the first type of failure (sparse errors in the data register), most of the failing words presented only one bit in error with exceptions in:

- at 10.1 MeV.cm<sup>2</sup>/mg, one word had 2 bit flips.
- at 18.5 MeV.cm<sup>2</sup>/mg, seven words had 2 bit flips and one word had 5 bit flips.

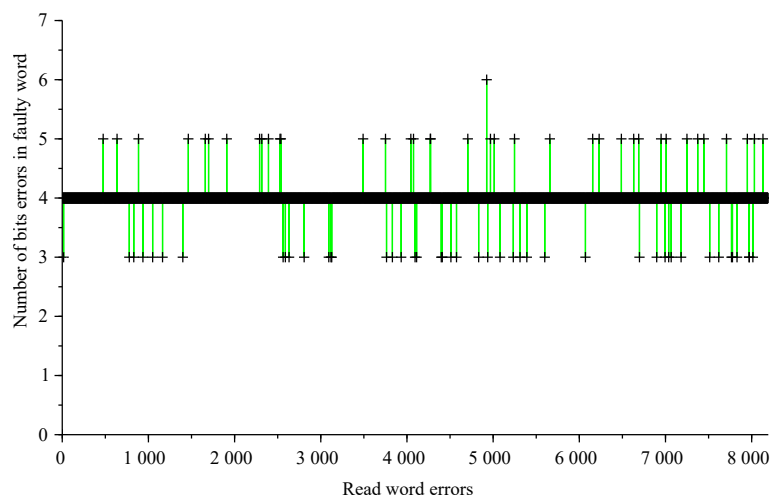
presents the cross section in the data register considering only the results of the first group, i.e., without an entirely failing data register. In this case, the word cross section was fitted with a Weibull curve, presenting a very similar result to the experiments shown in [65].



**Figure 2.14** – Word cross section of errors in the data register calculated according to Equation 2.2. The error bars indicate the 95% confidence interval. No events were recorded at an LET of 1.8 MeV.cm<sup>2</sup>/mg, so the cross section was arbitrarily plotted at  $1.10 \times 10^{-11}$  cm<sup>2</sup>/byte. The Weibull parameters used are:  $W = 30$ ,  $S = 2.1$ ,  $\sigma_{sat} = 1.10 \times 10^{-6}$  cm<sup>2</sup>/byte,  $LET_{th} = 1.8$  MeV.cm<sup>2</sup>/mg. Data taken from the RADEF test campaign.

In the previous research group works [53, 54], the presented results were limited to LETs of 1.8, 18.5, 32.1 and 60 MeV.cm<sup>2</sup>/mg, which led to the conclusion that the threshold effective LET for this fault was between 1.8 and 18.5 MeV.cm<sup>2</sup>/mg. Within this study, results for intermediate values (LETs of 3.6, 4.2, 10.1 and 60 MeV.cm<sup>2</sup>/mg) are introduced, and the threshold effective LET for this fault could be fined. When using a checkerboard pattern, most of the words (8 bits) had 4 bits upsets. Also, when using a solid ‘1’ pattern, most of the words had errors in their 8 bits. An example of this behavior is depicted in Figure 2.15, retrieved from a run using an LET of 18.5 MeV.cm<sup>2</sup>/mg. Since the memory provides a reset command that clears the data register contents, its control logic could be affected during the irradiation, leading to an unwanted reset that sets all bits of the data register to ‘0’ [53, 54].

Within the results in which an entirely faulty buffer was identified, some words appear with 3, 5, and 6-bit flips (instead of the expected 4-bit flips). In this case, once an unwanted reset occurs in the buffer, the fluence accumulated between the event moment and the end of the irradiation run may generate regular bit flips. The number of irregular data errors (additional bit flips) strongly depends on the moment the unwanted reset occurs. Clearly, the closer the event is to the end of the irradiation, the lower is the number of additional bit flips [53, 54].



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**Figure 2.15** – Number of data register bits falling in each failed word, in static mode, using a checkerboard pattern, at a surface LET of  $18.5 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ .

## Chapter 3

# Neutron-Induced Impact on a Pseudo-Static RAM

This Chapter presents contents based on the author's publications [JO-2] and [IE-7].

This Chapter presents a study on the effects of neutron irradiation (thermal and atmospheric-like spectra) on a self-refresh DRAM, also known as Pseudo-Static RAM (pSRAM), recently launched on the market (2020). Static and dynamic test methods were used to define the response of the device under irradiation. Experimental results from two different test campaigns are presented, with the identification of SBUs, stuck bits, and block errors in the memory. These faults were investigated and characterized by event cross section, soft-error rates, and bitmaps evaluations. An analysis of the damaged cells' retention time was performed, showing a difference between the self-refresh mechanism and a read operation. Additionally, a correlation of the fault mechanism that generates both SBUs and stuck bits under neutron irradiation is proposed, in line with the results under electron irradiation in [72]. Furthermore, high-temperature annealing was observed in post-radiation tests.

### 3.1 Dynamic Random Access Memory

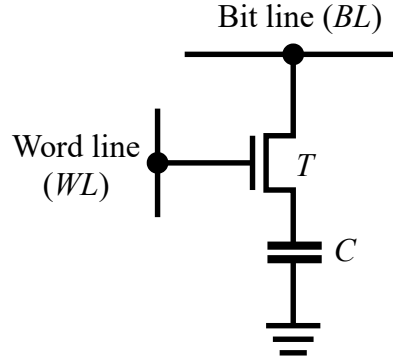
The DRAM technology has been well established since the 70s and remains an important technology nowadays with new designs bringing high-performance capabilities and its high usability in a wide range of applications [73, 74]. The DRAM cell consists of an access transistor and a capacitor used as a memory element. The charge stored in the capacitor defines the logic state of the cell, being used to represent a bit with a '0' or '1' value. Figure 3.1 presents a basic schematic of the 1T-1C structure. The gate of the access transistor



## Neutron-Induced Impact on a Pseudo-Static RAM

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( $T$ ) is connected to the word line ( $WL$ ). The transistors drain terminal is connected to the bit line ( $BL$ ), and the source terminal is connected to the storage capacitor ( $C$ ) [75, 76].



**Figure 3.1** – A simplified schematic of a one-transistor one-capacitor DRAM cell.

Both write and read operations are based on the activation of the  $WL$ , which enables the access transistor. For a write operation, a positive voltage is applied to the  $WL$ . Besides the transistor access activation, a high- or low-level voltage is applied to the  $BL$  during a specific time window enabling the change on the capacitor charge, which can swing from the low-level (data '0'), or high-level (data '1') [75, 76].

For the read operation, the  $BL$  is precharged. Then, once the access transistor is switched on, the stored charge of the capacitor flows to the bit line. A charge distribution takes place between the  $BL$  capacitance and the storage capacitance. This process generated a potential change on the  $BL$  that can be detected by a sense amplifier attached to this node, and then, respecting a charge-sharing time necessary to achieve enough voltage difference with respect to a reference value, the memory logic state can be identified. The read process is destructive, which means that the stored data is lost after the process, requiring a refresh procedure that is driven by feeding the  $BL$  with the sense amplifier output [75, 76].

An important aspect of DRAM is that the very small storage capacitor is not capable of storing its charge permanently, and it occurs due to multiple leakage current paths in the cell structure. This behavior requires a periodical refresh of the full memory array. The JEDEC (Joint Electron Device Engineering Council) specification defines a typical refresh time of 64 ms. However, considering the full memory array, only a very small portion of weak cells have a discharge time close to the typical limit. In any case, this small portion imposes a limit for the refresh period [75].

## 3.2 Pseudo-Static RAM

A pSRAM is based on an array of DRAMs cells that require periodic refresh operations in its memory contents. In DRAMs, the refresh operation is performed by the host, which should take care of applying such operations following timing requirements to maintain the data consistency. In a pSRAM device, the refresh control is performed by an on-chip logic, which will apply the refresh operation according to its timing requirements and while the memory is not actively being read or write. In this structure, since the host does not need to manage any refresh operation, the memory behaves as an SRAM (Static Random-Access Memory) device, which is composed of static cells that do not demand this kind of refresh controller [77, 78].

## 3.3 Neutron-Induced Effects on DRAMs

Neutron-induced soft errors on electronics have been a matter of study since the 70s [79]. The interaction of cosmic rays with the terrestrial atmosphere generates high-energy and thermal neutrons [80, 81]. Neutrons interact with matter and, through the processes of elastic and inelastic scattering and nuclear reactions, result in charged nuclear recoils [82, 83]. The created free charges of electron-hole pairs generated from the neutron events might subsequently lead to SEEs in the devices [83].

The reaction of thermal neutrons with boron-10 ( $^{10}\text{B}$ ) also generates byproducts (an alpha particle and a lithium-7 nucleus) that can cause SEUs [80, 81, 84, 85]. These effects were a concern for SRAMs and DRAMs fabricated with borophosphosilicate glass (BSPG) during the 90s. Nowadays, the BSPG is not present in these devices [81].

However, several works have been done on sub-micron devices showing that even without the BSPG layer in advanced Si technologies, there is a high probability of contamination during the fabrication process [86, 87]. The  $^{10}\text{B}$  may still be present as p-doping in the source/drain implementation [81, 88–90]. Furthermore,  $^{10}\text{B}$  originate from  $\text{B}_2\text{H}_6$  etcher gas used to improve the adhesion of tungsten in the trench contacts, causing high concentrations of  $^{10}\text{B}$  close to active regions of transistors [91, 92]. As a consequence of the scaling trend, a reduction of the  $^{10}\text{B}$  present in high-density devices is expected since also the contact size is reduced. At the same time, the shrinking of the technology node may also decrease the critical charge needed to induce SEUs [88]. Generally, the details of the internal architecture are not publicly available since they are proprietary. Thus radiation experiments represent an important method to evaluate the neutron sensitivity of modern devices. Often neglected, the impact of thermal neutrons should not be ignored [93–95]. As shown in [96], thermal

## Neutron-Induced Impact on a Pseudo-Static RAM

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neutrons contribute to the error rate in modern computing devices, such as the double-data-rate (DDR) DRAMs.

DRAM cells present a variable retention time (VRT) capability. This effect is intensified when the device is exposed to radiative environments, enhancing the cell leakage current and reducing its retention time. The cells with a reduced retention capability may appear as stuck bits that are known to be induced by the radiation [97–99]. This behavior was already reported in several studies on DRAM memories with different radiation sources, showing the intermittent behavior with a radiation-induced variation in the retention time of the memory cells [72, 100–102]. A relation between the bias condition and the occurrence of stuck bits is discussed in [103], as well as a temperature dependency [104].

Micro-dose and displacement damage is concluded as a cause of this effect in several works [97, 100]. In, e.g., [100, 104], the stuck bits were attributed to single-particle displacement damage effects (SPDDE), induced by single high-energy neutrons and protons. Also, in [101], the authors state that the neutron-induced number of VRT cells is similar to the observed in the same TID range on  $^{60}\text{Co}$  testing. However, the work also shows that the intermittent stuck bits can be caused by neutron-induced displacement damage.

### 3.4 Experimental Setup

#### 3.4.1 Device Under Test

The DUT is the S27KS0642GABHI020, a 64 Mib HyperRAM<sup>TM</sup> self-refresh DRAM (a.k.a, pSRAM) manufactured by Cypress Semiconductor. The DUT is a high-speed CMOS with a HyperBus<sup>TM</sup> interface, which uses the DDR to reach a data throughput up to 400 MBps with a maximum clock rate of 200 MHz. The memory is laid out on a 38 nm technology, and the cell array is composed of 8192 rows, and each row contains 512 word (16 bits) addresses. The self-refresh mechanism distributes single row refresh operations with an array refresh interval of 64 ms [105].

#### 3.4.2 Test Facilities

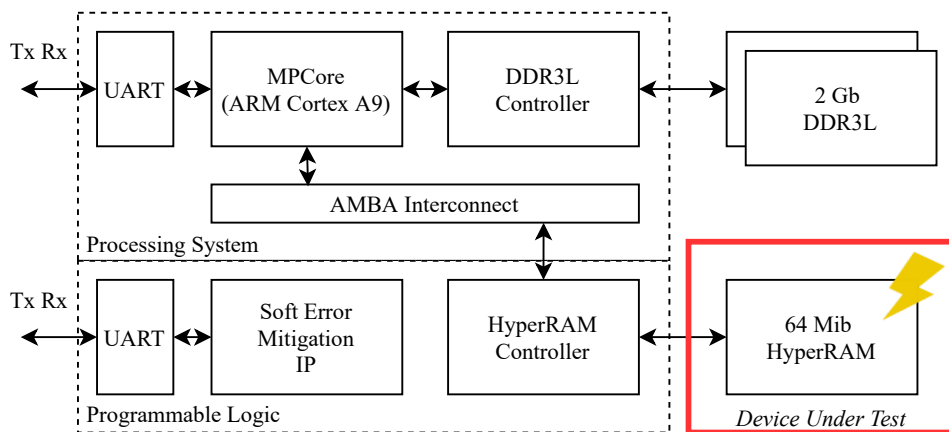
This study relies on two separate test campaigns. The first test campaign was carried out at the Platform for Advanced Characterisation (PAC-G) facility that is hosted by the Institute Laue Langevin (ILL) in Grenoble, France, using the D50 instrument. This instrument provides thermal neutrons moderated by liquid deuterium at 20 K, and the captured flux (i.e., the equivalent flux of 25 meV neutrons, which correspond to the room temperature

of 300 K) was  $10^9$  n/cm<sup>2</sup>/s, which is controlled by a <sup>3</sup>He-detector and periodical gold foil measurements [106].

The second test campaign [107] was carried out at the Rutherford Appleton Laboratories, UK. In the ChipIr beamline that provides an atmospheric-like neutron spectrum with a flux of about  $5 \times 10^6$  n/cm<sup>2</sup>/s for energies above 10 MeV, and also a thermal component for energies lower than 0.5 eV with a flux of  $4 \times 10^5$  n/cm<sup>2</sup>/s [32, 108]. The thermal neutron component is smaller than 10% [109, 96]. In comparative terms, the neutron flux in the beamline is approximately  $10^9$  times larger than the atmospheric neutron flux, which is 13 n/cm<sup>2</sup>/h ( $3.6 \times 10^{-3}$  n/cm<sup>2</sup>/s) at sea level [31].

### 3.4.3 Test Setup

The test setup is composed of a control board based on the Zynq-7000 SoC from Xilinx and a daughter board carrying the DUT. Figure 3.2 depicts the top-level diagram of the controller system with the DUT. The control system uses the System-on-Chip (SoC) ARM Cortex™-A9 processor to perform the test algorithms on the DUT through the HyperBus™ controller, which is an IP (Intellectual Property) provided by Cypress and implemented in the SoC's Programmable Logic, which manages the communication between the processor and the DUT.



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**Figure 3.2** – Top-level diagram of the test setup highlighting the Device Under Test.

## 3.5 Test Modes

In this study, static and dynamic memory tests were applied to the DUT to evaluate the memory response during irradiation. Dynamic tests constantly access the memory employ-

## Neutron-Induced Impact on a Pseudo-Static RAM

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ing read and write operations in order to emulate real applications and detect functional faults [110, 111]. For the static test, a write operation is performed with a known data pattern (e.g., solid ‘0’, solid ‘1’, and checkerboard patterns), then the memory is irradiated during a time interval. During irradiation, the memory then only performs data refresh, after which a readback operation is applied to identify the corrupted bits.

For dynamic tests, four different algorithms were used: March C-, Dynamic Stress, Dynamic Classic, and mMats+ [112, 113]. These algorithms were previously used on SRAM [114], FRAM (Ferroelectric Random-Access Memory) [115], MRAM (Magnetoresistive Random-Access Memory) [116], to evaluate the radiation impact on the devices. The algorithms are presented below in: (3.1) March C-, (3.2) Dynamic Stress, (3.3) Dynamic Classic, and (3.4) mMats+. The arrow indicates the addressing order (‘↑’ up or ‘↓’ down), ‘w’ (write), and ‘r’ (read) indicates the operation, and the following Boolean number indicates the data background. The algorithms are composed of elements indicated by the arrow, followed by the operations in parenthesis. In our work, the operations enclosed by the parenthesis are performed in sequence in each memory address. When the addressing order is “↑”, the operations are executed from the address 0 to  $N$ , and when is “↓”, the operations are executed from the address  $N$  down to 0, being  $N$  the highest memory address. Thus, e.g., the element “↑( $r0, w1$ )”, goes from the first address up to the last one, applying a read operation (where a solid ‘0’ data background is expected) followed by a write operation (using the solid ‘1’) in each address. A complete dynamic test algorithm is delimited by a bracket pair [117]. For the March C-, Dynamic Stress, and mMats+, the first element (up write operation) is performed only once to initialize the memory.

$$\begin{aligned}
 & \uparrow (w0); \\
 \{ & \uparrow (r0, w1); \uparrow (r1, w0); \downarrow (r0, w1); \downarrow (r1, w0); \\
 & \uparrow (r0); \}
 \end{aligned} \tag{3.1}$$

$$\begin{aligned}
 & \uparrow (w1); \\
 \{ & \uparrow (r1, w0, r0, r0, r0, r0); \\
 & \uparrow (r0, w1, r1, r1, r1, r1); \\
 & \uparrow (r1, w0, r0, r0, r0, r0); \\
 & \downarrow (r0, w1, r1, r1, r1, r1); \\
 & \downarrow (r1, w0, r0, r0, r0, r0); \\
 & \uparrow (r0, w1, r1, r1, r1, r1); \}
 \end{aligned} \tag{3.2}$$

$$\{\uparrow(w0); \uparrow(r0); \uparrow(w1); \downarrow(r1); \} \quad (3.3)$$

$$\begin{aligned} & \uparrow(w0); \\ & \{\uparrow(r0, w1); \uparrow(r1, w0); \} \end{aligned} \quad (3.4)$$

## 3.6 Results and Analysis

The analysis of the test outputs led to the identification of different types of faults. First, the results related to SBUs and stuck bits are detailed in this section, including retention capability analysis and high-temperature thermal annealing. Following this, a description and discussion of large events leading to clusters of errors defined in this work as block errors are presented. Finally, the overall event cross section and Soft Error Rate (SER) for the three different types of faults are given.

### 3.6.1 SBUs and Stuck Bits

The simplest observed fault consists of SBUs, appearing as a ‘0’ to ‘1’ and ‘1’ to ‘0’ transition. Analyzing the full test campaign data for each DUT, we classified as SBU errors in bits that appeared only once, having no further occurrence in the same location.

Stuck bits were observed in two different manners: permanent and temporary stuck bits. The fault is defined as a memory cell that has its retention time affected by a particle interaction resulting in a cell with a stuck value (‘0’ or ‘1’) independently of the written value. In this study, permanent stuck bits are the ones that, after the first appearance, return a faulty logic value for each of the following read accesses to the faulty address. In the case of temporary stuck bits, the error returns during a certain time window, with an intermittent behavior.

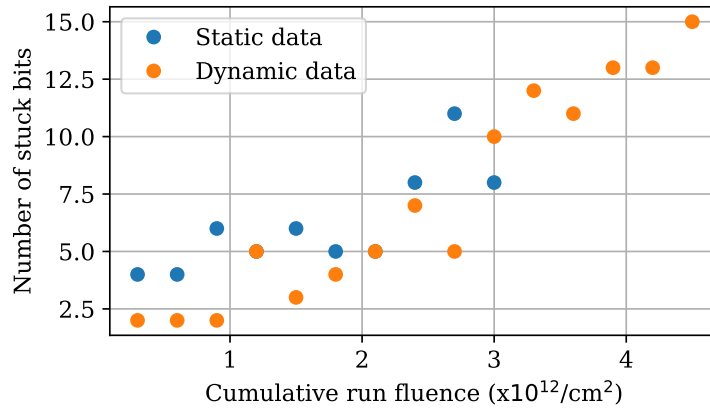
The experiments reveal that the stuck cell’s logic value could be either ‘0’ or ‘1’, showing that each logic value is represented by a charged or discharged capacitor depending on the memory region. The acquired results support this assumption, where for atmospheric-like neutrons, in which the amount of stuck-at and SBU faults were about two thousand events, 49% of the cells were stuck-at, or flipped, to ‘0’, and 51% to ‘1’.

The number of stuck bits as a function of cumulative run fluence is presented in Figure 3.3 for thermal neutron irradiation, and in Figure 3.4 for the atmospheric-like neutron beam.

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The points depicted in these figures represent the number of stuck bits (both permanent and temporary) during a test run. The data points were generated by first identifying all the occurrences of stuck bits, and then, in the graphs, the points depict the number of stuck bits addresses that were identified within each test run and are located at the total cumulative fluence on the DUT at the end of the runs. The results exhibit growth of stuck bits with the increase of the cumulative run fluence.

For thermal neutrons, no significant difference can be observed between static and dynamic test data. The atmospheric-like irradiation results presented more variations on the static test mode. These variations can be caused by the long exposure (long duration of the run). The arrow in the plot indicates a result related to a 9 hours irradiation run with a static test (memory in retention mode with just the self-refresh action during the whole run).



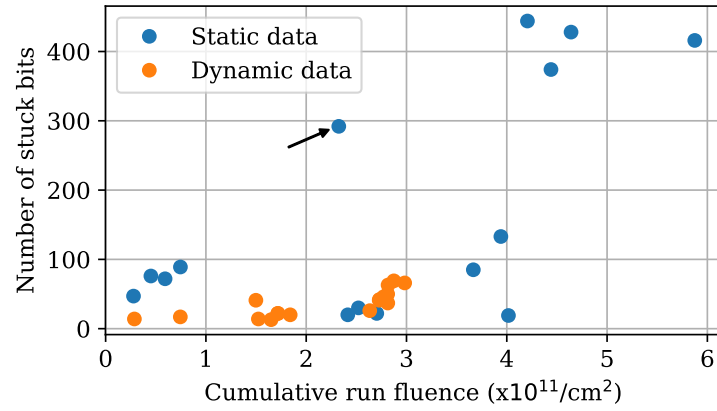
**Figure 3.3** – Number of stuck bits in the DUT as a function of cumulative run fluence during the thermal neutron irradiation.

Moreover, in Figure 3.5 and Figure 3.6, it is presented the bit cross section for each type of algorithm and test mode. For this purpose, first, we identified all the bit addresses where an SBU or a stuck bit was present. Then, according to each type of test (all the dynamic algorithms and the static mode), the bit cross section is defined as:

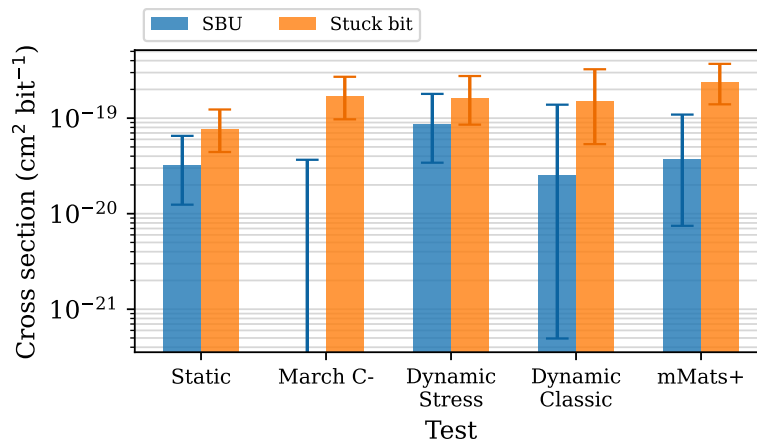
$$\sigma_{type(bit)} = \frac{\sum N_{type}}{\sum F_{type} \times M} \quad (3.5)$$

where  $\sum N_{type}$  is the sum of the number of bits that return an error (SBU and stuck are presented separately) within the test type,  $\sum F_{type}$  is the cumulative run fluence of each test type, and  $M$  is the memory size in bits.

During the exposure under thermal neutrons, with a flux of  $10^9$  n/cm<sup>2</sup>/s, the SBUs appear in dynamic and static test runs, with only a few events. In the second test campaign, with



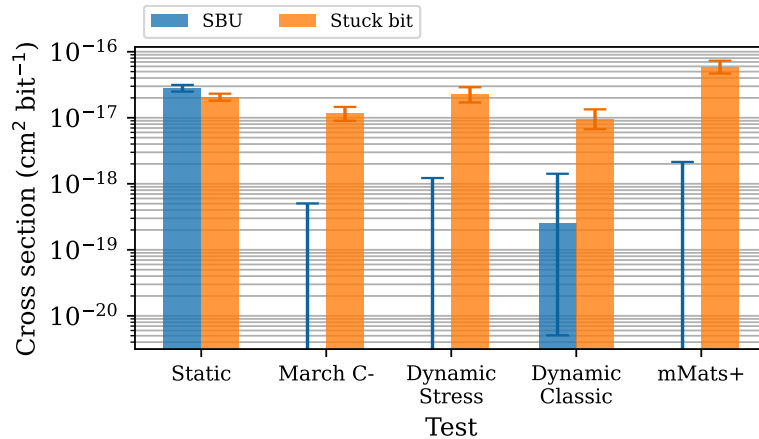
**Figure 3.4** – Number of stuck bits in the DUT as a function of cumulative run fluence during the atmospheric-like neutron irradiation.



**Figure 3.5** – Estimated bit cross section for each test type with 95% confidence interval using a fluence uncertainty of 10%. The results presented in this figure are related to thermal neutron irradiation.



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**Figure 3.6** – Estimated bit cross section for each test type with 95% confidence interval using a fluence uncertainty of 10%. The results presented in this figure are related to the atmospheric-like neutron irradiation.

an average flux of  $4 \times 10^6 \text{ n/cm}^2/\text{s}$  and an atmospheric-like neutron beam, the SBUs only appeared during the static mode, with over a thousand events, excluding a unique event during a Dynamic Classic. Even with a lower cumulative fluence, the amount of SBU occurrences was higher, about  $62\times$ , under the atmospheric-like neutron beam. However, the events were identified only during static mode tests. In the dynamic mode, the cells are continuously accessed for read or write actions, and both of them induce a refresh of the cells' content. In the static mode, the refresh is reduced only to the self-refresh mechanism of the memory. Thus, w.r.t. static mode, the charge stored in the cells is statistically lower (weaker cells), and, for this reason, the SBU occurrence is higher. Since SBUs were identified in dynamic test mode during the ILL test campaign but not in ChipIr, it is possible that the lower flux of the ChipIr beam may play a role in this different behavior. Furthermore, the occurrence of stuck bits is very similar within the four dynamic algorithms.

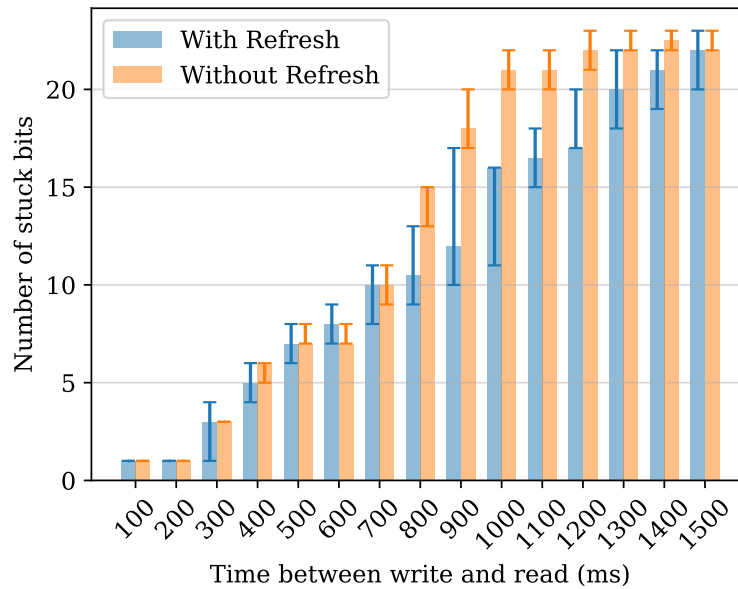
### 3.6.2 Cells' Retention Time

Temporary stuck bits present the same behavior as the permanent ones. The only difference is that, in the first case, the fault is not permanent and just occurs during consecutive write and read operations that were performed within the dynamic and static test modes. Temporary stuck bits also presented a different level of damage, i.e., different levels of degradation of the cell's retention capability. The duration of these temporary errors was different depending on the test run. During Dynamic Stress tests, all the cells that presented the stuck-at phenomenon did not return an error in the sequential five read back performed just after a write operation. However, the error appeared in the first read operation performed in the next element of

the algorithm. This behavior can be explained with an induced reduction (by the particle interaction) of the retention time of the storage capacitor of the cell [100].

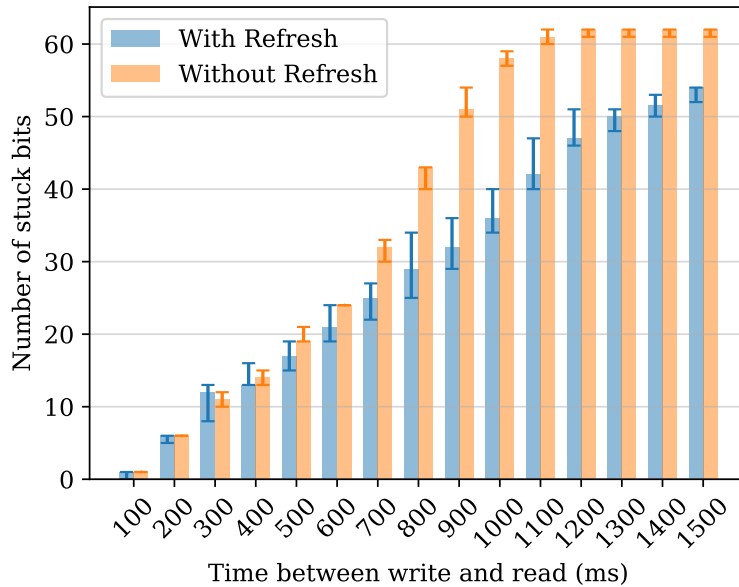
A post-radiation test was performed in both DUTs targeting the cells that present the stuck behavior to deeper analyze this effect. To identify the faulty cells, the entire memory was written with both solid ‘0’ and ‘1’ data patterns, and since they presented a different data retention time, the read operation was performed just after 60 seconds in order to elapse a significant amount of time to induce the stuck cells to lose their contents. Then, the retention test consisted of writing a ‘0’ (or ‘1’) in the faulty cells’ addresses, followed by a waiting time period (with different duration), and finally, a read-back operation was performed to check if the elapsed time between the write and read operations was enough to induce the fault. Since the memory self-refresh mechanism can be disabled, we considered the two different test scenarios with the self-refreshing enabled and not.

The acquired results from these tests are presented in Figure 3.7 and Figure 3.8, where the bars presents the number of bits that appeared as stuck relatively to the different elapsed time between the write and read operations for both scenarios. A variation due to borderline cells was identified, leading to a maximum and minimum amount of stuck cells for each value of elapsed time (giving the error bars). The write-wait-read operations were executed 10× for each value of waiting time and scenario.



**Figure 3.7** – Retention time on faulty cells in post thermal neutron irradiation tests in the DUT used during the thermal-neutron test campaign. Error bars present the maximum and minimum values. The bars’ height presents the mode value.

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**Figure 3.8** – Retention time on faulty cells in post thermal neutron irradiation tests in the DUT used during the atmospheric-like neutron test campaign. Error bars present the maximum and minimum values. The bars' height presents the mode value.

From both presented graphs, it is possible to spot that the refresh operation decreased the faulty cells' discharge rate, which is expected behavior. These results are in line with several works that relate the stuck fault with the refresh rate, as presented in [97] and [100], where the number of stuck bits decreases when the refresh rate increases. However, since the memory self-refresh mechanism distributes single row refresh operations, where the array should be fully refreshed in a maximal time interval of 64 ms [105], it is expected that if the time needed to discharge the bit cell is higher than the refresh interval, the self-refresh mechanism should be able to keep the capacitor with a charge above the threshold value used to identify the cells' logic data. The results presented in Figure 3.7 and Figure 3.8 show that the expected behavior is not achieved in those cells that presented radiation-induced errors since they have degraded retention capability.

A further analysis based on this behavior is also proposed. After identifying the stuck bits in the post-radiation DUTs, we performed two different procedures:

1. A write operation is performed in each bit that appears as stuck post-radiation; the self-refresh mechanism is kept enabled during 10 minutes; the bits are read.
2. A write operation is performed in each bit that appears as stuck post-radiation; the self-refresh mechanism is disabled; keep applying read operations in the bits with a time interval of 64 ms (the same of the self-refresh) during 10 minutes;

As a result, with the first procedure (1), the read operation returned the stuck bits failing. On the other hand, with the second procedure (2), no failing bits were returned when reading the memory, which means that the “refresh” achieved by an actual read operation was able to keep the bit cells with a charge above the failure threshold, while the normal refresh operation was not. Experimentally, we noticed that the self-refresh and the actual read (applied by the host) lead to different refresh efficiency. Since the internal device design and architecture are not available, our hypothesis of explanation is that the self-refresh circuitry accesses the memory for a period shorter than an actual write/read access. The larger access time allows a larger equivalent charge to be stored in the cell capacitor.

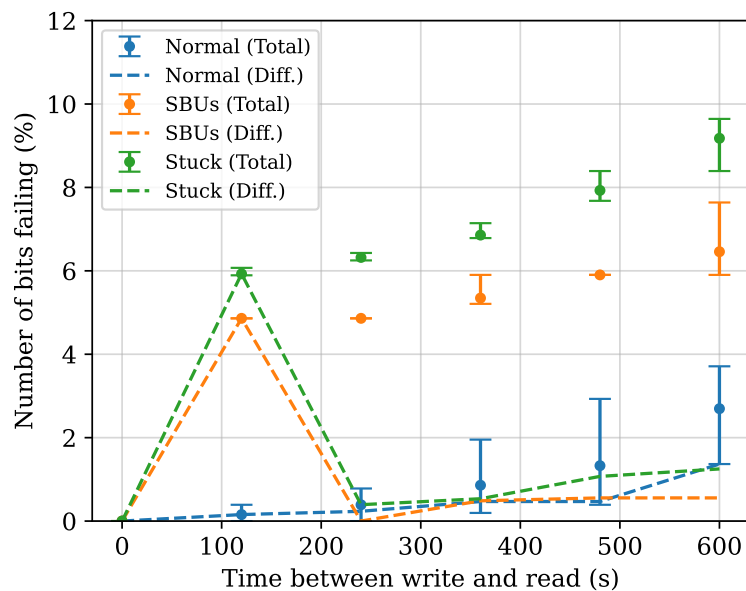
### 3.6.3 Fault Mechanism of the Stuck Bits and SBUs

Neutron irradiation may induce different levels of damage on a cell, which is presented by the appearance of permanent and temporary stuck bits. Further analysis of results exhibits a trend concerning the cells that experienced an SBU, which shows to be very similar to the stuck bit fault mechanism. In this case, the cells’ retention time has been measured by disabling the memory’s self-refresh mechanism and performing write and read operations with different time intervals. Note that in all observed cases, within a 16-bit word, only one failing bit at a time has been identified during the tests, and the adopted test procedure is similar to the one used to obtain the results presented in Figure 3.7 and Figure 3.8. However, in this case, the target word addresses are the ones that presented either an SBU or a stuck bit during the irradiation tests. As a control procedure, the same test has also been applied to random portions of the memory, with word addresses that did not present any fault during the radiation tests. Table 3.1 presents the number of addresses used for each case. Figure 3.9 presents the acquired results for the thermal neutron irradiation, and Figure 3.10 for the atmospheric-like neutron irradiation. The error bars represent the maximum and minimum value, and the dot represents the mean value. The dashed lines represent the increase in the number of bits failing from one measure to the next.

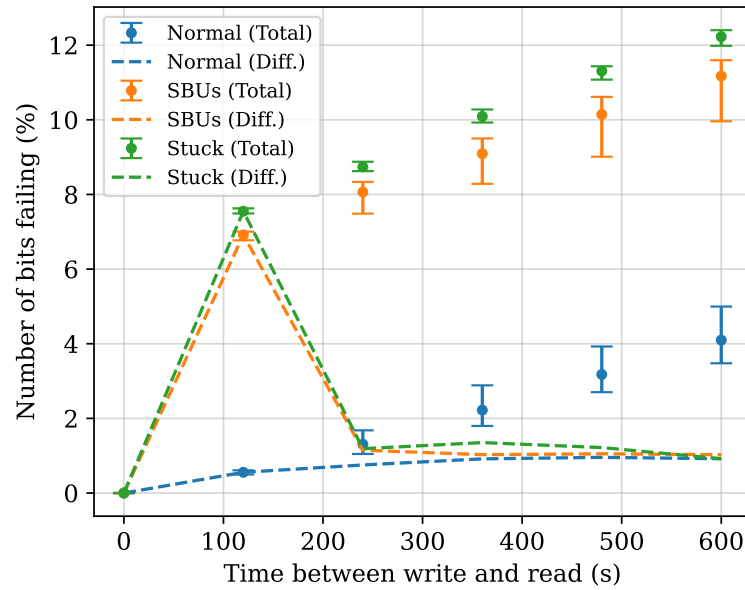
## Neutron-Induced Impact on a Pseudo-Static RAM

**Table 3.1** – The number of word addresses that presented an SBU or a stuck bit, and also the number of word addresses of the random portion. The numbers are presented according to the irradiation source.

Neutron beam	SBUs	Stuck bits	Normal
Thermal	18	35	32
Atmospheric	1127	821	1057



**Figure 3.9** – The percentage number of bits failing at a defined interval between the write and read operation with the self-refresh mechanism disabled. Error bars present the maximum and minimum values. The dot represents the mean value. The dashed lines represent the increase in the number of bits failing. Data acquired from post-radiation tests on the DUT used in the thermal neutron irradiation.



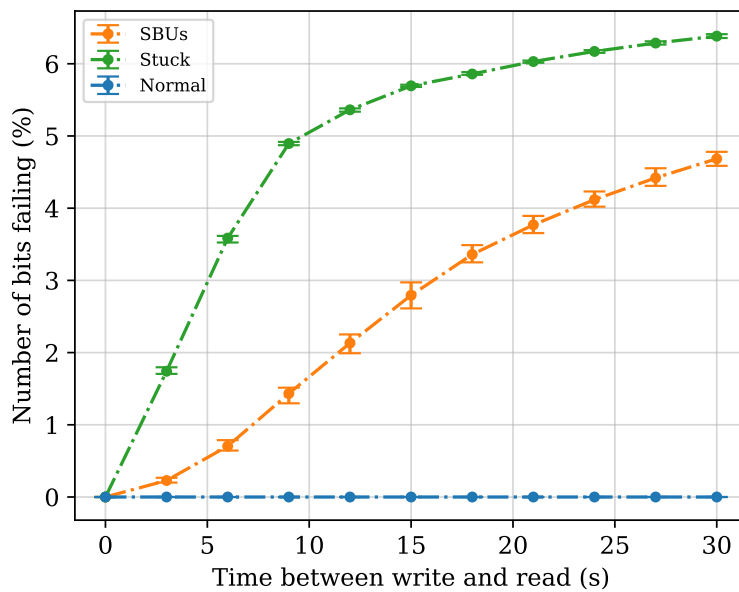
**Figure 3.10** – The percentage number of bits failing at a defined interval between the write and read operation with the self-refresh mechanism disabled. Error bars present the maximum and minimum values. The dot represents the mean value. The dashed lines represent the increase in the number of bits failing. Data acquired from post-radiation tests on the DUT used in the atmospheric-like neutron irradiation.

The populations that contain the damaged cells have their nominal retention time decreased, showing similar behavior for both SBUs and stuck bits. Also, the other cells (the remaining 15 bits) from the faulty addresses show normal behavior. These results suggest a similarity of fault mechanism between SBUs and stuck bits, despite the fact they lead to different fault models. The difference in terms of effect (fault model) is the different levels of damage in the cell due to the particle hit that is more severe in the case of a stuck bit. Thus, concerning the fault mechanism, the most probable interpretation is particle-induced displacement damage that leads to a variation (reduction) of the retention time of the affected cells (with a leakage current discharging the cells) [100, 101, 99]. The permanent degradation is observable when the refresh mechanism is disabled and a sequence of write-wait-read operations is acted. Intermittent bits show borderline behaviors between permanent stuck and normally working cells. Clearly, the more time elapses between the read and write accesses, the more small degradation in cells will be detected as faults.

In the case of SBUs, the degradation leads to a small reduction of the retention time of the cell. In order to spot the degradation of the cells concurrent to SBUs, we need to relax the refresh frequency or enlarge the time between two cell accesses when the self-refresh is disabled. This behavior is also confirmed in our experiments by the different efficiency of the self-refresh and actual read operation, as presented in the previous subsection

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(Subsection 3.6.1). In our tests, under atmospheric-like neutron irradiation, only a unique occurrence of SBU was detected in dynamic test mode, while several SBUs were observed in static test mode. In the first case, the dynamic test mode ensures frequent read and write accesses, while in static mode, the data refresh is made only by the self-refresh mechanism. The Figure 3.11 presents the percentage of bits failings when targeting the different addresses (SBUs, stuck bits, and “normal”) in post-radiation tests on the DUT used in the atmospheric-like neutron irradiation. Differently from Figure 3.9 and Figure 3.10, in Figure 3.11, the time interval between the write and read is shorter, enabling a finer visualisation of the degradation on the retention time of the target addresses.



**Figure 3.11** – The percentage number of bits failing at a defined interval between the write and read operation with the self-refresh mechanism disabled. Error bars present the maximum and minimum values. The dot represents the mean value. Data acquired from post-radiation tests on the DUT used in the atmospheric-like neutron irradiation.

In a general, for regular use, i.e., not in a harsh environment, the refresh mechanism is able to keep the charge of the cells at a level above the reference used to identify the stored logical value. In most of the cases, the cells display a large margin of retention that could be one or two order of magnitude higher than the minimum needed [118–120]. Considering this characteristic of DRAMs, higher refreshing frequency can be targeted only on a small lot of cells with lower retention capability. This aspect is already explored by several works targeting reducing the refresh operation overheads in power consumption, memory access latency, and memory throughput [118–122]. However, with the neutron-induced degradation of the cell’s retention capability, the trend goes in the opposite direction. In this case,

one approach to improve memory reliability would target increasing the efficiency of the refresh procedure, e.g., as explored above, the self-refresh mechanism could provide more extended memory access when refreshing, increasing the average stored charge (reducing the occurrence of faulty cells). This effect could also be achieved by applying memory scrubbing, which would be more effective at recharging the cell. However, these procedures may lead to a higher memory access latency and consequently reduce the memory throughput. Additionally, in [123, 124], the authors propose mechanisms that explore the VRT of the DRAM cells and could be adapted to handle the radiation-induced retention time degradation of the cells.

### 3.6.4 Thermal Annealing Tests

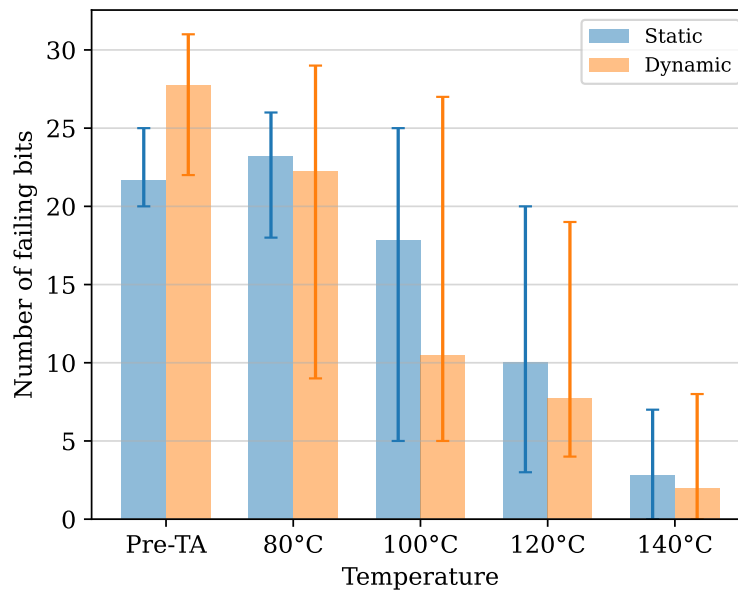
A temperature dependency is shown in several works treating the stuck phenomena in DRAMs. In running time, the increase in the temperature raises the leakage current, leading to the appearance of more stuck bits [101, 104, 100]. However, studies have shown that a high-temperature baking process can recover the memory cells' retention capability. In [98], the damage induced by X-ray irradiation was recovered by a thermal annealing process, which presented a reduction in the cells' retention time with the increase of the baking temperature. This behavior is also observed by [97], where the number of stuck bits decreased with the increase of the temperature annealing.

To analyze the thermal annealing effect on the damaged cells, the DUTs were baked during 8 hours at four different temperatures: 80°C, 100°C, 120°C, and 140°C. After each high-temperature exposure, we performed five runs of the static test with solid '0' and solid '1' data pattern with an interval of 60 seconds between the write and read operation, four sequences of the dynamic March C- algorithm (with ten dynamic cycles each sequence), and retention time tests were applied in the DUTs at room temperature.

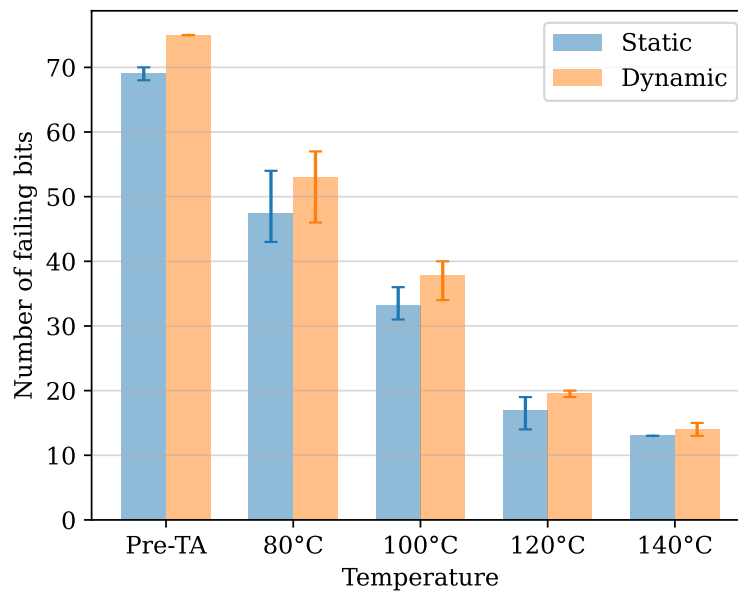
For the dynamic and static tests, the self-refresh mechanism was kept enabled. These two tests target inducing thermal annealing on the cells that appear as stuck on the DUT after the irradiation. The results are presented in Figure 3.12 and Figure 3.13 for thermal and atmospheric-like neutron irradiation, respectively. The acquired results are compared with tests performed before the thermal annealing tests. From now on, Pre-TA stands for pre thermal annealing.



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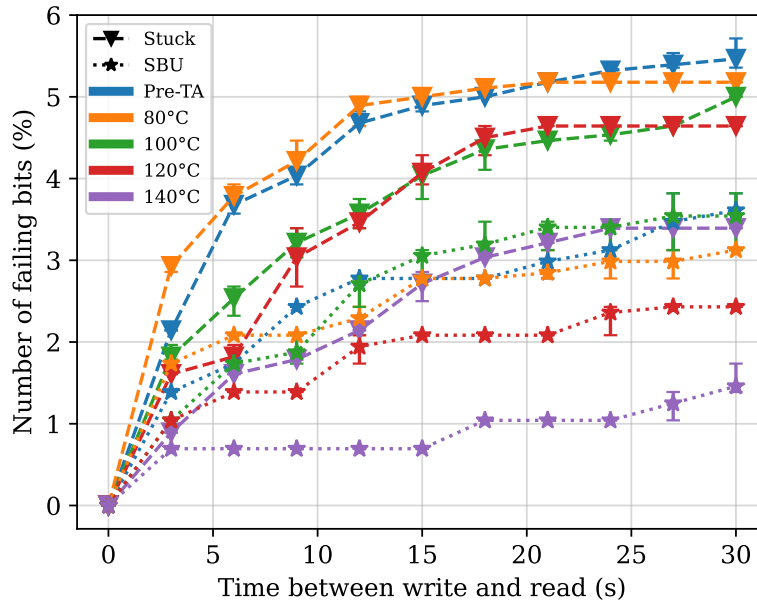


**Figure 3.12** – The number of bits failing for pre and post thermal annealing tests using static with solid ‘0’ and solid ‘1’ data pattern, and the dynamic March C- algorithm. Errors bars present the maximum and minimum values. Data was acquired from the post-irradiation thermal annealing test on the DUT used in the thermal neutron irradiation.

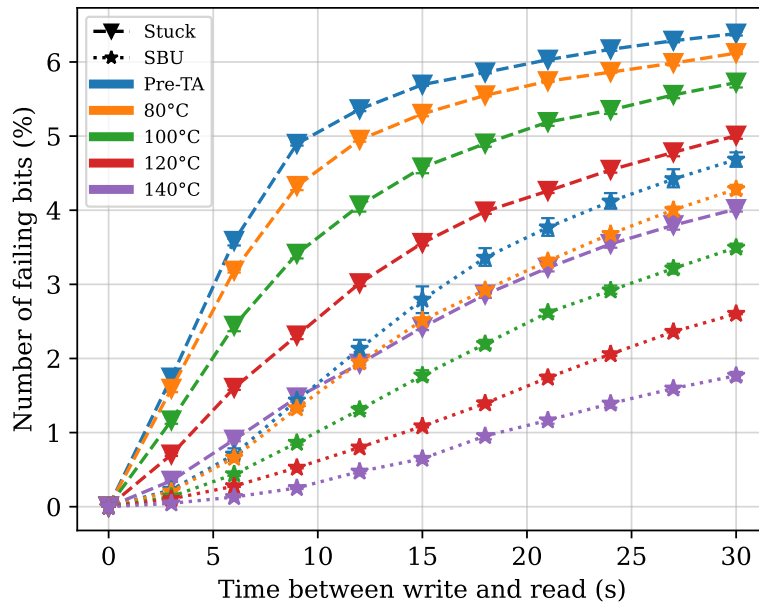


**Figure 3.13** – The number of bits failing for pre and post thermal annealing tests using static with solid ‘0’ and solid ‘1’ data pattern, and the dynamic March C- algorithm. Errors bars present the maximum and minimum values. Data was acquired from the post-irradiation thermal annealing test on the DUT used in the atmospheric-like neutron irradiation.

Further, an additional test for retention time was made in the addresses where a stuck bit or an SBU was identified during the irradiation tests. This test is similar to the one presented in the previous section. The addresses that contain a faulty cell passed through a sequence of write-wait-read operations while the self-refresh mechanism was disabled. This test identifies the cells' retention time. Figure 3.14 and Figure 3.15 depict a comparison between pre-annealing and post-annealing results for both DUTs. The figures show how the high-temperature annealing decreases the number of stuck bits present at all tested points and that the retention time of the cells recovers with the annealing. The displacement damage induced by the neutron irradiation is thus annealed and annealed more efficiently with higher temperatures.



**Figure 3.14** – The percentage number of bits failing in pre and post thermal annealing tests. Errors bars present the maximum and minimum values. Data was acquired from the post-radiation thermal annealing test on the DUT used in the thermal neutron irradiation.



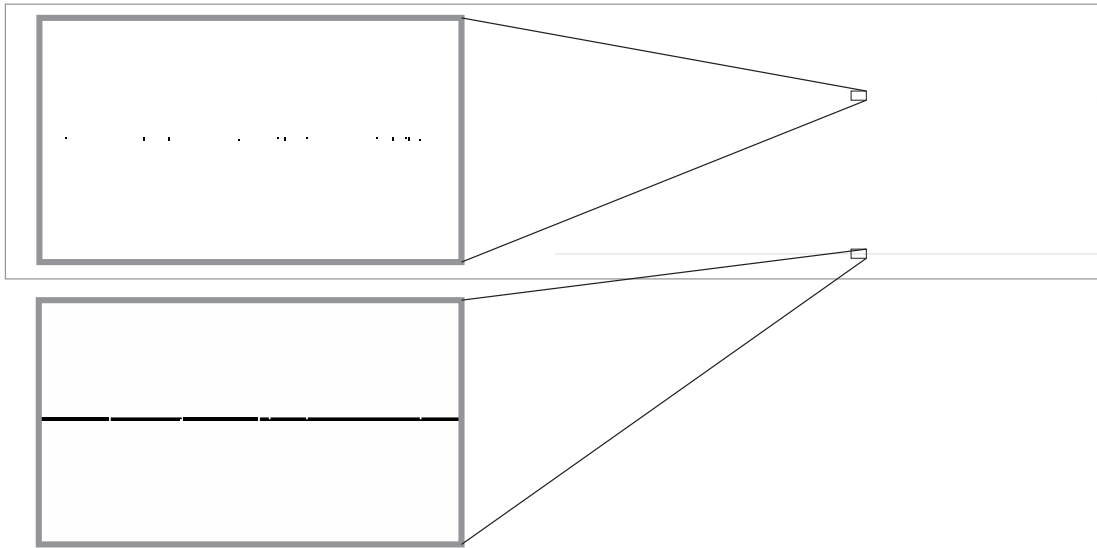
**Figure 3.15** – The percentage number of bits failing in pre and post thermal annealing tests. Errors bars present the maximum and minimum value. Data acquired from the post-radiation thermal annealing test on the DUT used in the atmospheric-like neutron irradiation.

### 3.6.5 Block Errors

Besides the described faults (SBUs and stuck bits), block errors with vertical and horizontal shapes were observed in the memory bitmaps. To evaluate these events, we generated logical bitmaps by dividing the memory array into two parts, using the left side for odd rows and the right side for the even ones. This procedure generated 16384 columns. In a bitmap, each pixel represents a bit cell.

An example of a horizontal block error can be seen in Figure 3.16, which is the resulted bitmap of a static test with a checkerboard pattern as a data background. In the figure, two square zones are zoomed in to increase visibility. These events are characterized by errors occurring in all the 512-word addresses of two consecutive even or odd rows, being most of the bits within a word with an error. An exception of this behavior is presented in the top left zoomed-in square of Figure 3.16, where within the same address range, the bitmap shows a horizontal strip of errors with most of the not-faulty bits, resulting in events with less than the expected 1024 words errors.

Block errors were also observed with a vertical shape, in which the same column is affected in subsequent even or odd rows. Figure 3.17 spot this block error identified during a Dynamic Stress test in a second cycle for the first “r1” operation of the fourth element of the



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**Figure 3.16** – Bitmap was obtained after a static test mode using a checkerboard “AAAAh” during a thermal neutron run. Each pixel represents a bit; bits that were identified with errors appear in black. The grey lines are used to limit the region. Zoom-ins are added to increase the visibility of the horizontal block events.

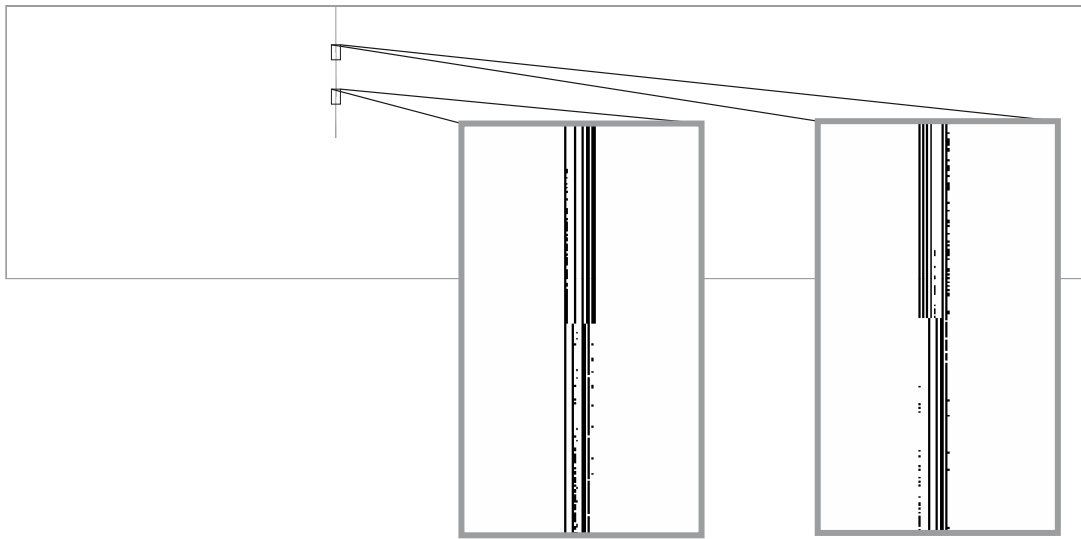
algorithm. It is interesting to highlight that in all vertical lines of errors, the addresses with errors span in the same range, returning a maximum of 2048 words with errors.

For both vertical and horizontal block errors, a write operation was able to restore the access to the cells without the need to carry out a power cycle. This error type is not due to a problem related to the affected cells but rather to the control logic. In particular, a temporary malfunction of the sense amplifier or register that serves that column may lead to this behavior.

An interesting way to see the impact of both faults (stuck-at and block errors) is using a timeline plot. Figure 3.18 presents a run of a mMats+ (Equation 3.4) test, where the dots represent a faulty word detected during a read element of the test. The faults detected during the  $\uparrow (r0, w1)$ -element are depicted in blue, and the ones detected during the  $\uparrow (r1, w0)$ -element are in orange. During this test run, stuck bits appear as permanent and temporary, which can be seen by the horizontal sequence of dots on the graph. Also, a block error spanning 2048 addresses can be identified by the two vertical sequences of dots.

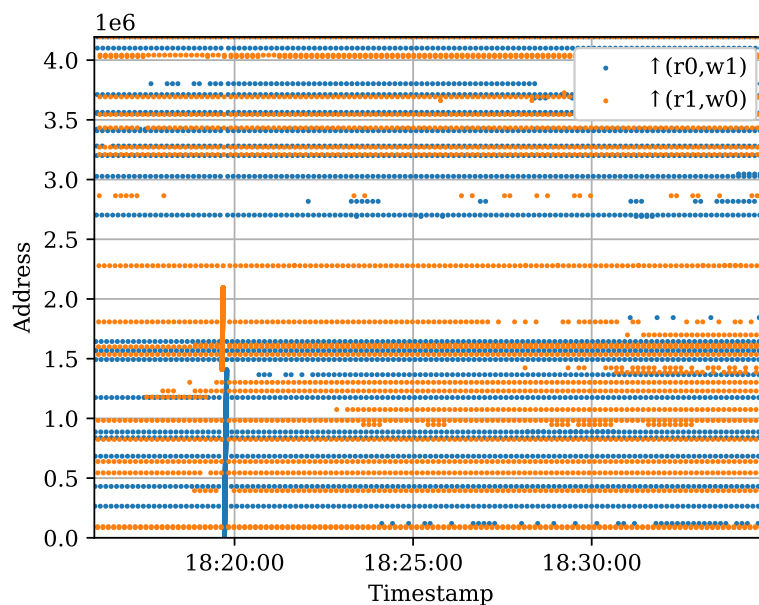
Two blocks of errors spanning a different range of addresses occurred during the thermal-neutron test campaign. The first event is depicted in Figure 3.19. The Bitmap presented in the figure was obtained during a Dynamic Stress test. The red arrows show the six error lines that were presented in the five “r1” operations performed in the last element of the Dynamic Stress algorithm. In this case, we identified twelve address ranges in three fixed columns in

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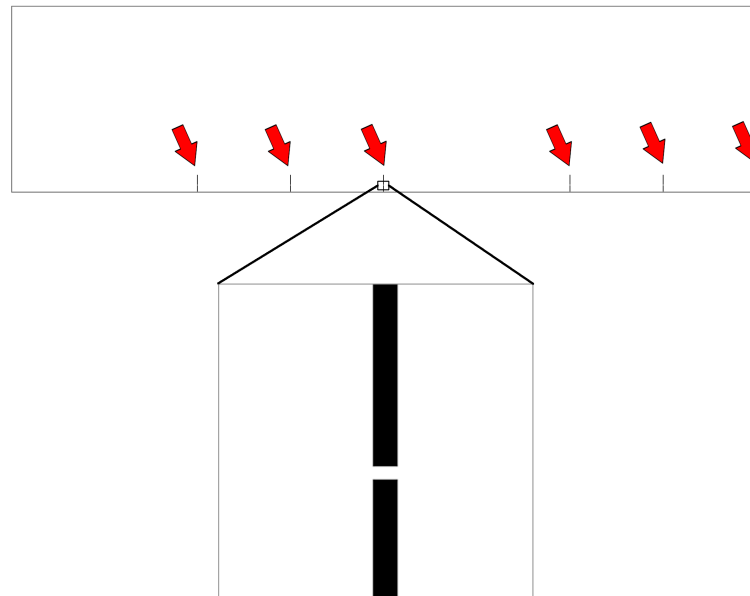
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**Figure 3.17** – Bitmap was obtained during a Dynamic Stress test during a thermal neutron run, occurring after the first ‘r1’ of the algorithm’s fourth line. Each pixel represents a bit; bits that were identified with errors appear in black. The grey lines are used to limit the region. Zoom-ins are added to increase the visibility of the vertical block events.



**Figure 3.18** – Errors during a mMats+ test run under the atmospheric-like neutron beam. The dots represent a faulty word detected during the different operations of the algorithm. Stuck bit appears as a horizontal sequence of dots; a block error appears as two vertical sequences of dots.

both even and odd rows. As the opposite of the first vertical event, all the addresses returned all bits with an error, and a power cycle was performed in the DUT.



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**Figure 3.19** – Bitmap was obtained during a Dynamic Stress test after the fifth ‘r0’ of the algorithm’s sixth line in the thermal-neutron test campaign. Each pixel represents a bit; bits that were identified with errors appear in black. The grey lines are used to limit the region. Zoom-ins are added to increase the visibility of the horizontal block events. Red arrows indicate the six vertical lines.

The second type of vertical line block error was observed during March C- test execution, with increasing addressing order, resulting in a sequence of more than 100 words with errors. The affected addresses were dependent on the execution order, resulting in a range from “000000h” to “00006Ah” for an increasing order (↑), and from “3FFFFFFh” down to “3FFF8Dh” for a decreasing order (↓). The effect persisted during several cycles of dynamic tests. However, after a dynamic execution, we performed a static write and read operation, and the block error was recovered after two static writes, returning its appearance during the next dynamic test. This event occurred during five runs using March C-, Dynamic Classic, mMats+, and with a sequence of static tests between the irradiation runs. It was recovered only through a power cycle.

Experimentally, a write operation in the memory addresses can recover the vertical and horizontal block errors. However, for the above specific cases (Figure 3.19, and the one mentioned in the previous paragraph), a power cycle was required to reestablish the memory functionality. It is possible that a micro latch-up occurring in the memory may have produced

## Neutron-Induced Impact on a Pseudo-Static RAM

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the malfunction since we did not spot any relevant increase in the memory current, which is typical of a large-scale latch-up.

Finally, the block error cross section is defined as

$$\sigma_{mode(device)} = \frac{\sum N_{mode}}{\sum F_{mode}} \quad (3.6)$$

where  $\sum N_{type}$  is the total number of occurrence of block errors for each test mode (static or dynamic), and  $\sum F_{mode}$  is the total cumulative fluence of each test mode. Table 3.2 and Table 3.3 present the values that were calculated using a 95% confidence interval and a fluence uncertainty of 10% for both scenarios (thermal and atmospheric-like neutrons).

**Table 3.2** – The estimated block error cross sections with 95% confidence intervals using a fluence uncertainty of 10%. The results presented in this table were identified under thermal neutron irradiation.

Test mode	$\sigma$	$\sigma$	
		Lower limit	Upper limit
Static	$1.81 \times 10^{-12} \text{cm}^2$	$6.52 \times 10^{-13} \text{cm}^2$	$3.96 \times 10^{-12} \text{cm}^2$
Dynamic	$1.77 \times 10^{-12} \text{cm}^2$	$7.51 \times 10^{-13} \text{cm}^2$	$3.51 \times 10^{-12} \text{cm}^2$

**Table 3.3** – The estimated block error cross sections with 95% confidence intervals using a fluence uncertainty of 10%. The results presented in this table was identified under atmospheric-like neutron irradiation.

Test mode	$\sigma$	$\sigma$	
		Lower limit	Upper limit
Static	$1.87 \times 10^{-11} \text{cm}^2$	$9.25 \times 10^{-12} \text{cm}^2$	$3.35 \times 10^{-11} \text{cm}^2$
Dynamic	$1.08 \times 10^{-10} \text{cm}^2$	$6.98 \times 10^{-11} \text{cm}^2$	$1.60 \times 10^{-10} \text{cm}^2$

### 3.6.6 Overall Event Cross Section and SER

To evaluate the overall events' cross sections of this memory, the fault types were divided into SBUs, stuck bits, and block errors. For these cases, we did not split the events occurring in dynamic and static modes.

The estimated event cross section ( $\sigma$ ) is defined in two different ways since the stuck bits and the SBUs are cell-related, the cross section takes into account the size of the memory, being the equation as

$$\sigma_{\text{bit}} = \frac{N}{F \times M} \quad (3.7)$$

where  $N$  is the number of events,  $F$  is the beam fluence in  $\text{n/cm}^2$ , and  $M$  is the number of bits [3]. When it comes to the block errors evaluation, since this fault is related to the control logic of the device, we may define the cross section as

$$\sigma_{\text{device}} = \frac{N}{F} \quad (3.8)$$

where the memory size is removed from the equation, and the cross section is device-based.

From the calculated events cross sections, we define the SER expressed in Failure In Time (FIT) per Mb. 1 FIT/Mb is equal to one failure per billions of working hours per Mb [125, 126]. The equation is

$$SER_{FIT/Mb} = \sigma_{\text{bit}} \times (1024 \times 1024) \times 10^9 \times j \quad (3.9)$$

for the SBU and stuck bit, where  $1024 \times 1024$  (bits) is the Mb coefficient,  $10^9$  is the FIT definition, and  $j$  is the flux at New York (sea level) outdoors for a mean solar activity defined in JEDEC JESD89A, being  $6.5 \text{ n/cm}^2/\text{h}$  for the thermal energies' ( $< 400 \text{ meV}$ ), and  $13 \text{ particles/cm}^2/\text{h}$  for the high energy neutrons ( $> 10 \text{ MeV}$ ) [31, 81, 126]. Being slightly modified in the evaluation of the block errors SER, where the Mb coefficient is removed from the equation, which becomes

$$SER_{FIT} = \sigma_{\text{device}} \times 10^9 \times j \quad (3.10)$$

Table 3.4 presents the estimated cross sections related to the thermal neutron test campaign, while Table 3.5 presents the estimated cross sections and SER for the atmospheric-like neutron test campaign. For the presented results,  $F$  is the total cumulative run fluence. However, for the specific case of SBUs under atmospheric-like neutron beam,  $F$  is the cumulative run fluence for static tests, since no SBU was identified under dynamic mode (the single



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SBU detected under Dynamic Classic was not considered). The values were calculated using a 95% confidence interval and a fluence uncertainty of 10% in both scenarios.

**Table 3.4** – The overall estimated cross sections with 95% confidence intervals using a fluence uncertainty of 10%, and SER. The values were calculated using the Equation 3.7–3.10 for the fault types identified in this study. The results presented in this table were identified under thermal neutron irradiation.

Fault type	$\sigma$	$\sigma$		SER
		Lower limit	Upper limit	
SBU	$3.43 \times 10^{-20}$	$2.00 \times 10^{-20}$	$5.45 \times 10^{-20}$	$2.3 \times 10^{-4}$
	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	FIT/Mbit
Stuck bit	$6.68 \times 10^{-20}$	$4.55 \times 10^{-20}$	$9.37 \times 10^{-20}$	$4.5 \times 10^{-4}$
	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	FIT/Mbit
Block error	$1.79 \times 10^{-12}$	$9.75 \times 10^{-13}$	$3.01 \times 10^{-12}$	$1.1 \times 10^{-2}$
	cm <sup>2</sup> /device	cm <sup>2</sup> /device	cm <sup>2</sup> /device	FIT

**Table 3.5** – The overall estimated cross sections with 95% confidence intervals using a fluence uncertainty of 10%, and SER. The values were calculated using the Equation 3.7–3.10 for the failures types identified in this study. The results presented in this table were identified under atmospheric-like neutron irradiation.

Fault type	$\sigma$	$\sigma$		SER
		Lower limit	Upper limit	
SBU	$2.86 \times 10^{-17}$	$2.53 \times 10^{-17}$	$3.19 \times 10^{-17}$	$3.9 \times 10^{-1}$
	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	FIT/Mbit
Stuck bit	$1.48 \times 10^{-17}$	$1.30 \times 10^{-17}$	$1.66 \times 10^{-17}$	$2.0 \times 10^{-1}$
	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	cm <sup>2</sup> /bit	FIT/Mbit
Block error	$4.48 \times 10^{-11}$	$3.08 \times 10^{-11}$	$6.23 \times 10^{-11}$	$5.8 \times 10^{-1}$
	cm <sup>2</sup> /device	cm <sup>2</sup> /device	cm <sup>2</sup> /device	FIT

### 3.7 Conclusion and Discussion

The effects of neutron irradiation in a self-refresh DRAM were described. Different kinds of faults were identified from static and dynamic test modes realized during two test campaigns with thermal and atmospheric-like neutrons. Besides the occurrence of SBUs, the tests showed permanent and temporary stuck bits, which already had been reported in several studies, presenting different fault mechanisms, with the most probable cause being the irradiation impact on the variable retention time phenomenon.

Tests targeting the retention time of the damaged cells show that the fault mechanism of the stuck bits and SBUs present a very similar behavior, being the main difference the degradation level on the cells' retention time. The retention time tests also show that, experimentally, there is a difference between the self-refresh and read operation, which should lead to a difference in the equivalent stored charged in the cell's capacitors. The damage induced in both the cells with SBUs and stuck bits was also found to anneal during high-temperature annealing tests. The higher the annealing temperature, the more the cells retention time was found to recover.

Furthermore, block errors were observed in four different patterns, with intermittent word errors in vertical and horizontal sequential logical addresses, and also presenting divided vertical lines with all bits within a word with errors, and a sequential error with dependency in the addressing order.

Cross sections for the different kinds of faults were estimated, showing that the memory is not very sensitive to thermal neutrons. However, it is necessary to consider that vertical and horizontal block errors present a significant quantity of word errors within an event, where, from a user point of view, it could represent an issue in critical applications.



# Chapter 4

## Study on a Synchronous Dynamic RAM

This Chapter presents contents based on the author's publications [IE-2], [JO-6] and [IE-11].

This Chapter analyses the response of SDRAMs to neutron irradiation. First, it is introduced the SEEs induced by heavy-ion [127] and electron [72] irradiation, which are co-authored works from the research group and the full citation is provided above. Therefore, three different generations of the same device with different node sizes (63, 72, and 110 nm) were characterized under an atmospheric-like neutron spectrum at the ChipIr beamline in the Rutherford Appleton Laboratories, UK. The memories were tested with a reduced refresh rate to expose more SEUs, and under similar conditions provided by a board specifically developed for this type of study in test facilities. The neutron-induced failures were studied and characterized, presenting the occurrence of SBUs and stuck bits. The cross sections for each type of event and technology node show that the 110 nm model is more sensitive to neutron-induced SEEs than the other models.

### 4.1 Synchronous Dynamic RAM

The DRAM cell structure and basic operations are described in Section 3.1. DRAM devices have different operation modes that are classified as asynchronous and synchronous. The asynchronous mode operates based on control signals that clearly should respect the device access time restrictions. In comparison, the synchronous mode has a clock dependency, which is the case of SDRAMs [76]. Nowadays, several JEDEC [128] standards are adopted in the development of DRAM technologies.

The tested devices in this study belong to different generations of a memory device produced by ISSI that use different manufacturing node sizes: 110 nm for IS42S16320B [129],

72 nm for IS42S16320D [130], and 63 nm for IS42S16320F [131]. The memories are a Single Data Rate (SDR) SDRAMs, with 536,870,912 bits organized on four banks with 8192 rows and 1024 columns of 16 bits. The maximum operating frequency is 143 MHz, with a 3.3 V input supply voltage, and packaged in 54-pin TSOP-II packages.

## 4.2 Heavy-ion-induced Effects

This section summarises the results from heavy-ion microbeam irradiation on one of the technology nodes described in this chapter. More details of this work can be found in [127].

The heavy-ion-induced effects were investigated using two specimens of the 63 nm IS42S16320F. For the heavy-ion exposure, the specimens were delidded by a chemical process laying the die bare for irradiation. The tests were conducted with the linear accelerator UNILAC at the GSI facility in Darmstadt, Germany, with a micrometer ion beam with two different ions: gold (Au) and Calcium (Ca).

The DUTs were controlled with a DE0-CV FPGA development board. The board used the Nios II soft-core to implement the tests algorithms and the provided SDRAM memory controller to interface the processor and the memory device. The memory controller was also slightly modified to add the capability to modify the frequency in which the controller sends the auto-refresh command to the memory. The nominal refresh frequency is 128 kHz, which means that the command is executed 8192 times every 64 ms [131]. Furthermore, the tests used the March-C and Dynamic Stress algorithm (both are described in Section 3.5).

Since this study used a microbeam, it could target the irradiation on specific regions of the memory. In this case, no upsets or errors were identified when irradiating regions of the memory that were outside the memory array. Besides the occurrence of bits upsets, a similar work presented the occurrence of SEFIs. However, the target memory in this study was the 110 nm version (IS42S86400B) [129]. Furthermore, the test was performed with a broad beam, and its exact location on the device die can not be readily obtained. In our case, when targeting the array, the reported results are in line with the findings presented in the previous Chapter (Chapter 3). In this work, it is reported the occurrence of SBUs and stuck bits. The stuck bits also presented an intermittent behaviour, showing a dependency on the wait time between a write and read operations (only the refresh commands are applied). The number of induced stuck bits as a function of cumulative fluence of Au ions presented a linear behaviour, as has been previously observed, e.g., in [132]. However, this trend was not the same with the Ca ions. For the nominal refresh frequency (128 kHz), it was identified only one stuck bit, showing that the device is less sensitive to Ca ions than the Au ions, which

can be correlated to the lower LET, since the  $^{197}\text{Au}$  ion has a LET of  $94 \text{ MeV}/(\text{mg}/\text{cm}^2)$ , and the  $^{48}\text{Ca}$  has a LET of  $16 \text{ MeV}/(\text{mg}/\text{cm}^2)$ .

The unit exposed to Ca ions was tested under three different points of refresh frequency, the nominal one that is 128 kHz, a minimum refresh frequency value which was experimentally defined (the lowest refresh frequency where all the bits in the memory still manage to retain data before the irradiation) as 2.5 kHz, and a point also using half of the value defined as the minimum, which is 1.25 kHz. The first point (128 kHz) presented the case of only one stuck bit. In the second point (2.5 kHz) there was linear increase behaviour. However, the number of induced stuck bits was low, reaching less than 20 bits. The third point, using half of the minimum refresh frequency (1.25 kHz), had a quick increase in the begging of the irradiation run followed by a more linear behaviour. This can be explained by the radiation-induced degradation of the retention capability of the cell, which will present a more significant impact if the cells are operating with a very low refresh.

Finally, this work also identified an annealing phenomenon on the stuck cells. This behavior was seen with a short time scale anneal. However, this annealing process was identified only in a portion of the affected cells, and the number of stuck bits after this short time remains constant (considering the time scale in which the data was acquired).

### 4.3 Electron-induced Effects

This section summarises the results from electron irradiation on one of the three technology nodes that this Chapter describes, the model IS42S16320B, with 110 nm. More details of this work can be found in [72]. The electron-induced effects are a major concern for space missions, mainly for the Jovian environment, which presented a harder energy spectrum around Jupiter, in comparison with the one presented in the Van Allen radiation belts [133, 134]. The main objective of the presented work is to investigate the possibility of the occurrence of stuck bits due to the impact of single electrons. Also, the implication of the usage of target SDRAMs in the Jovian environment is discussed since this device is a candidate to be used onboard in the JUICE (JUperiter ICy moons Explorer) mission, from the European Space Agency (ESA).

The presented results are based on two test campaigns. The first was performed at VESPER (the Very energetic Electron facility for Space Planetary Exploration missions in harsh Radiative environments) [135], which is located at CERN, using high-energy electrons with a range from 60 up to 100 MeV. The second was performed at RADEF with the Varian Clinac (Clinical LINear ACcelerator) 2100 CD [136].

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During these tests, the memories were driven using the previously described setup (Section 4.2) based on the DE0-CV FPGA development board and applying the March C-algorithm Equation 3.1.

The results presented in this work are also in line with the ones from Chapter 3, with the identification of SBUs and stuck bits. The fault mechanism of both effects is put in relation, and it is suggested to be the same. The conclusion is based on the similarity in the radiation-induced degradation of the retention time of the cells.

Also, the errors have shown a sudden increase at a certain dose level (electron fluence). A linear trend characterises this behaviour up to this certain dose level, and after it changes for a power-law trend. It is argued that this first part originates from SEEs induced by electron irradiation, and the second part is attributed to the accumulation of smaller damage clusters, having a dependency on the dose rate. In this light, with three specimens of the same device (110 nm memory), it shown that at different dose rates at 20 MeV of energy, the critical dose rate that enables the change in the behaviour on the cumulative number of stuck bits is lower for higher dose rates.

Targeting the expected electron environment on the JUICE mission, in-flight predictions for the 110 nm model were performed. The predictions were based on the estimated cross sections, with an 11.1 years mission duration, and taking into account different phases of the mission, where the system would receive different fluxes of particles. A non-shielded and a 15 mm shield scenario is presented, showing that the estimated number is low, with a total of 3.8 errors with a non-shielded scenario and an even lower number of 1 error with the shielded scenario. Additionally, since a dose-rate dependency was observed in this study, tests with low electron flux and dose rate could contribute to fully estimating the target device's behavior during the mission. Another important aspect should be the temperature. In this study, an annealing behavior was also identified at room temperature, and its effects would also contribute to the predictions.

## 4.4 A Comparative Study of the Technology Impact on the Neutron-induced Effects

This study investigates the radiation effects in three different memory generations of the same SDRAM, each memory model with a different technology node size. The devices were characterized under irradiation with an atmospheric-like neutron spectrum. Other studies have characterized these memory chips under different particle and energy spectra, revealing that the memory cells in DRAMs are susceptible to different types of radiation-induced

## 4.4 A Comparative Study of the Technology Impact on the Neutron-induced Effects

upsets, including SEU, SEL, SEFI, and stuck bits [137]. Stuck bits have also been studied in e.g. [138, 97–99]. Studies on stuck bits have been made by using different types of particle irradiation, including protons and neutrons [104, 100], heavy ions [139] and Section 4.2, and electrons [72], as summarized in Section 4.3. The stuck bits do often have an intermittent behavior, where the memory cells have a variable retention time [100, 101]. Furthermore, the neutron-induced effects are more deeply addressed in Chapter 3.

The approach adopted for this study consists of comparing the devices' neutron-induced failures, providing an assessment of the memories' resilience across the different generations. In order to ensure a comparable scenario, the memories were exposed simultaneously under the effective beam area using the same controller board, which assigns similar electrical and behavioral characteristics. During the experiment, static and dynamic test algorithms were run to acquire the location and number of the faults. Also, a round-robin strategy was adopted, which executed static and dynamic tests on the different memories with a rotating schedule to optimize the beam time utilization during each run. The main objective of this study is to evaluate the evolution of radiation impact across the different generations of the same device.

### 4.4.1 Devices under test

In this study, the tested devices are different generations of a memory device produced by ISSI, using different manufacturing node sizes: 110 nm for IS42S16320B [129], 72 nm for IS42S16320D [130], and 63 nm for IS42S16320F [131]. The device's description was already given in the previous section. The tested components are summarized in Table 4.1.

**Table 4.1** – Summary of Specimen Used in the Experiments.

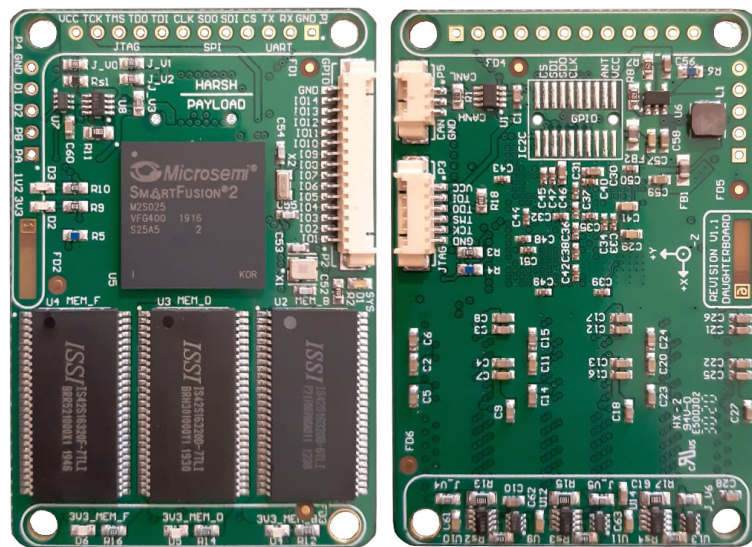
Memory	Node size (nm)	DUT IDs
IS42S16320B	110	B1, B2
IS42S16320D	72	D1, D2
IS42S16320F	63	F1, F2

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These devices were mounted in a tailored platform, designed to be used for experimental evaluation in test facilities, and ready for actual space environment missions. This approach was adopted to extend the study of these memories from a ground-based analysis, more intrusive and broad, to a space assessment, the actual targeted environment. For this reason,



## Study on a Synchronous Dynamic RAM



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**Figure 4.1** – Top and bottom view of the HARSH board.

the development of a tailored platform was required, leading to the design and production of the board presented in Figure 4.1 (known as *Harsh Environment CubeSat Payload* and herein referred to as “HARSH”).

The HARSH board consists of the main controller, a Microsemi system-on-a-chip FPGA (SmartFusion2 M2S025), and the SDRAM chips themselves integrated with a small form of 6-layers PCB. Also, there are latch-up monitors for each memory and interfaces for integration with a CubeSat platform. The board uses the FloripaSat [140] missions payload standard, targeting the FloripaSat-2 [141] mission scheduled to be launched in 2022, and follows a simplified space application design guideline.

The main design considerations and objectives were to produce a reliable platform with commercial off-the-shelf (COTS) components and reasonable development efforts. In order to provide the most accurate results, the memories should have the most similar parameters and test conditions. To accomplish that, the other components on the HARSH board were selected due to their known degree of radiation sensitivity [142] and the board layout followed the applicable space-related criteria proposed by ESA guidelines (ECSS-Q-ST-70-12C). The guideline was not entirely fulfilled due to the proposed application scope of the HARSH board, resulting in a similar approach discussed in [143].

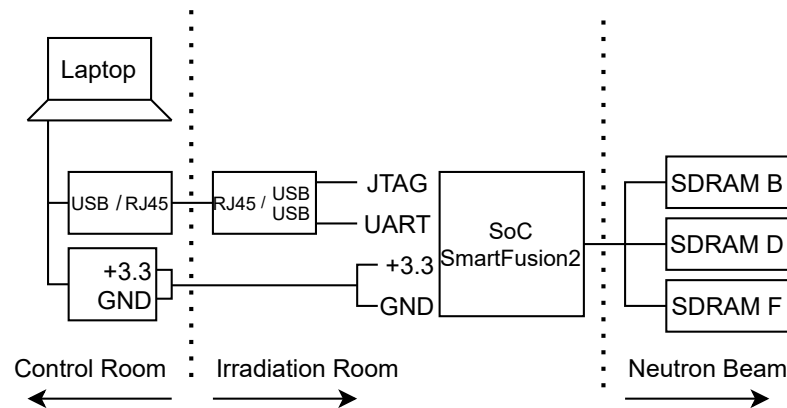
## 4.4 A Comparative Study of the Technology Impact on the Neutron-induced Effects

### 4.4.2 Test facility

The test campaign [144] was carried out at the Rutherford Appleton Laboratories, UK, using the ChipIr beamline at the ISIS Neutron and Muon Source. The beamline is dedicated to the study of single event effects on electronics, and it is designed to provide an atmospheric-like neutron spectrum. More details about the beamline can be found in [32, 109, 108], and were already previously described in Subsection 3.4.2.

### 4.4.3 Test procedures and setup

A schematic diagram of the test setup is shown in Figure 4.2. The power supplied to the board was monitored in order to identify SELs. The run-time tests results were logged through a serial port with the logical addresses, error data per address, error flags, and operation status. Functional tests of the memory controller were performed between the runs to ensure proper functionality during the experiment sessions.



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**Figure 4.2** – Schematic diagram of the experimental setup used for exposing the DUT under the beam and acquiring the logs from the board to a remote computer.

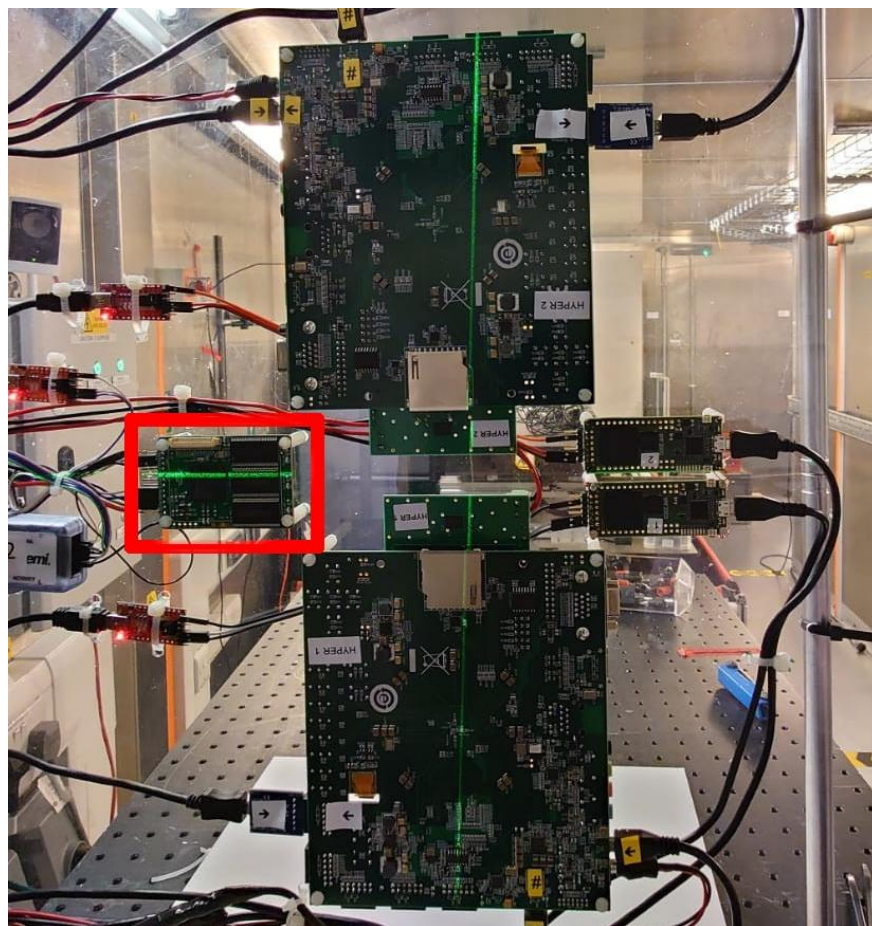
During each run session, the memories were tested with static and dynamic test modes using a round-robin strategy to operate the same amount of time with each memory and with the closest conditions. This test procedure is as follows: one memory is under a dynamic test mode per run in a session, while the other two memories are subjected to static test mode. After a run of sufficient neutron fluence, the memories shift the test mode that is being executed. This approach distributes dynamic and static tests over the three samples.

The nominal refresh rate of the memories is 8192 refresh operations every 64 ms (which corresponds to sending an auto-refresh command at a frequency of 128 kHz). In these tests, a lower refresh frequency was used to detect a higher number of errors and increase

## Study on a Synchronous Dynamic RAM

the statistics of the tests. This is discussed, e.g., in [145], so that a lowering of refresh frequency could be used to simulate an increase in temperature, where the memories are more susceptible to radiation-induced errors [146, 147]. In the experiments described in this paper, an auto-refresh command frequency of 6.1 kHz was used throughout all irradiations and characterizations, corresponding to each bit being refreshed at intervals of 1.34 s. No error was present in the pristine memories at this refresh rate.

Due to the shared utilization of the beamline with other experiments, only one HARSH board was evaluated for a given session, and two identical HARSH boards (using memories of the same manufacturing lots) were used during the test campaign. The memories were positioned in the beam in a way to ensure full coverage by the neutron field while keeping the controlling systems on the board outside the beam. The setup in the beam is presented in Figure 4.3. The local environment was at room temperature.



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**Figure 4.3** – Test boards fixed in a shared mounting frame ready for the experiment (HARSH board in the red rectangle).

#### 4.4 A Comparative Study of the Technology Impact on the Neutron-induced Effects

The evaluation of the three memories is based on the execution of two different test modes: static and dynamic mode. In static mode, the memories are written with a known data pattern (e.g., solid '0', solid '1', or checkerboard patterns), and the devices are exposed to the radiation during a time interval to reach a defined fluence. Afterward, the memories' contents are read back, and the corrupted bits are sent to a host computer as error frames. These error frames are logged as described in the Subsection 4.4.3.

Previous studies on the DUTs have shown that the mechanism of SBUs and stuck bits are suggested to be the same: degradation of the retention time capabilities of the cells (Chapter 3 and [72]) at different degrees. Then, the procedure described in Figure 4.4 was applied to understand if a read performed just after a write operation could sensitize a fault. The procedure is composed of a read operation, herein referred to as 's1', which has the objective to identify the expected faults (SBUs and stuck bits). A read-write-read operation is performed in the faulty address when an error is detected in 's1'. The read 's2' is performed to confirm the error in the memory cell, and then write-read accesses are executed to identify the retention capability of the cell since every operation in a DRAM cell refreshes its value. The read 's3' would identify a fault that is not related to degradation on the retention capability of the cell but permanent damage to its structure.

```
1: procedure READ_RETENTION(pattern)
2:   for addr = startaddr to endaddr do
3:     data ← sdram_read(addr)                                ▷ s1
4:     if data != pattern then save_error_frame()
5:       data ← sdram_read(addr)                                ▷ s2
6:       if data != pattern then save_error_frame()
7:     end if
8:     sdram_write(addr, pattern)
9:     data ← sdram_read(addr)                                ▷ s3
10:    if data != pattern then save_error_frame()
11:    end if
12:  end if
13: end for
14: end procedure
```

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**Figure 4.4** – Read retention procedure

In dynamic mode, the memory is constantly accessed through read and write operations. This approach enables the detection of functional faults and emulates a more close to a real application [110, 111]. For this purpose, the March C- (3.1) was applied.

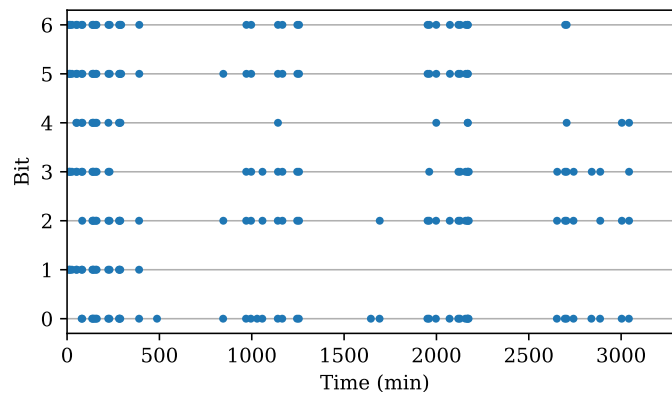
#### 4.4.4 Results and discussion

The DUTs were exposed to the atmospheric-like neutron beam reaching a cumulative fluence of neutrons over 10 MeV of  $\approx 1.3 \times 10^{12}$  n/cm<sup>2</sup> on the DUTs B1, D1 and F1, and  $\approx 7.2 \times 10^{11}$  n/cm<sup>2</sup> on the DUTs B2, D2 and F2. Considering the ChipIr average neutron flux, we run  $\approx 113$  h of experiments.

Two different types of faults were observed during the irradiation of the memories. The first type was SBU (bit-flip), which manifested as one faulty read of a bit address during the tests, where the bit remained operational after rewriting the memory cell. The other type was the stuck bit, which was a bit that returned a faulty value multiple times, even after being rewritten.

The stuck bits were, in general, intermittently stuck, not necessarily having many repetitions of returning a faulty value after rewriting. Therefore, all bits which experienced more than one error were categorized as stuck.

An example of the behavior of the stuck bits can be seen in Figure 4.5, where the detected errors in 7-bit addresses are shown for the tests on the DUT B1.



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**Figure 4.5** – Timeline plot from a portion of stuck bits in memory B1. The bits are numbered as 0 - 6, and each row shows the behavior of one bit along with the test campaign.

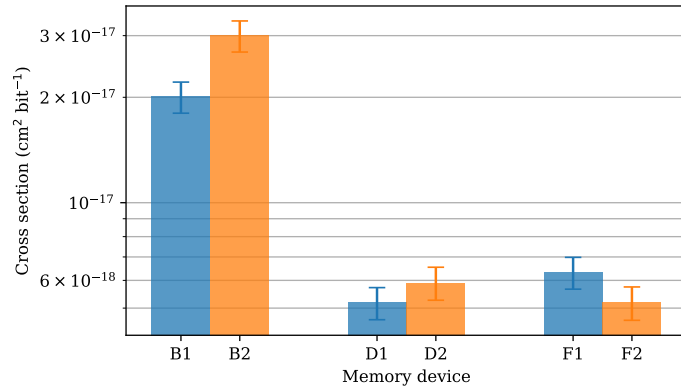
To evaluate the memory sensitivity to the presented errors, the fault types were divided into SBUs and stuck-at bits. The event cross section ( $\sigma$ ) as:

$$\sigma = \frac{N}{F \times M} \quad (4.1)$$

where  $N$  is the number of events,  $F$  is the cumulative fluence in particles/cm<sup>2</sup>, and  $M$  is the number of bits [3]. The calculated cross section for stuck bits is shown in Figure 4.6,

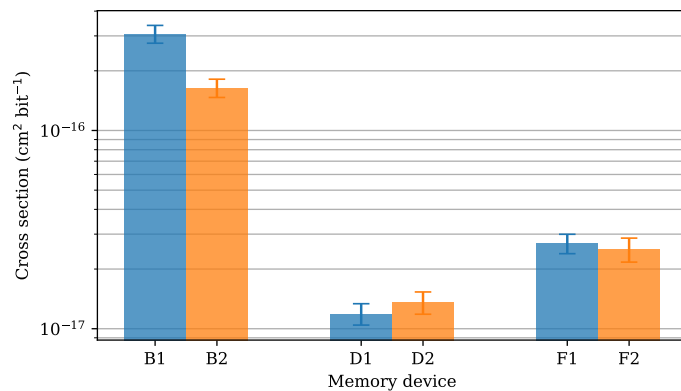
#### 4.4 A Comparative Study of the Technology Impact on the Neutron-induced Effects

and Figure 4.7 presents the calculated cross section for SBUs. The error bars in the figures represent a 95 % confidence interval with a 10 % beam fluence uncertainty.



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**Figure 4.6** – Stuck bit cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.



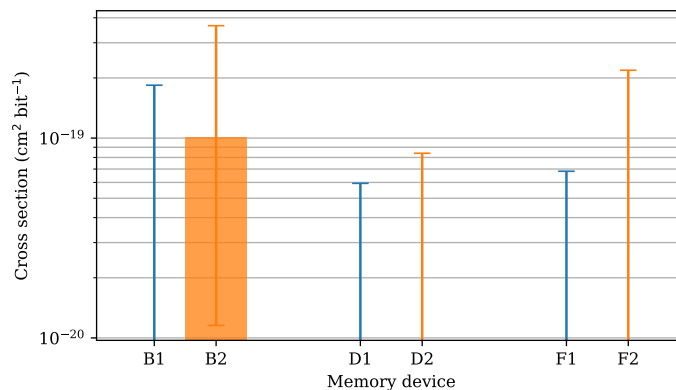
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**Figure 4.7** – SBU cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.

During irradiation, bytes containing two upset bits were also observed. Bytes with two upsets at one occasion are here called 2-BUs (two-bit upsets), and the cross section for this type of event is shown in Figure 4.8. This was only observed for two bytes in device B2.

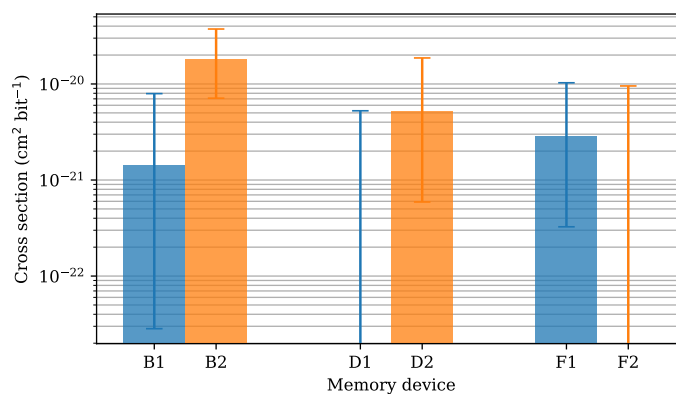
Bytes which repeatedly showed two bits with error were more common and were observed in four of the tested devices. The cross section for this error mode is presented in Figure 4.9.

Common among the bytes that have two bits in error is that one or both of the bits also appeared at different moments within the test runs. These faulty bits have thus not likely been affected by the same incident particle, but rather they are stuck and intermittently stuck bits that accumulate and happen to be in the same byte of the memory.



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**Figure 4.8** – 2-BU cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.



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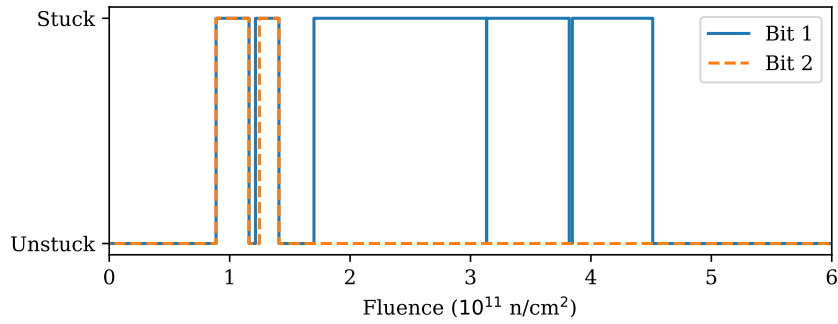
**Figure 4.9** – 2-Stuck bits cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.

An example of the pattern that represents two intermittent stuck bits in one word is shown in Figure 4.10. In the figure, a bit is shown as stuck if the individual bit has an error during a test (static or dynamic) and unstuck if it has no upsets for the test duration. It can be seen that often only one of the bits has upsets, and occasionally both have upsets at the same time. The shown example is from sample B1.

Since a widely used Error Detection and Correction (EDAC) algorithms can handle one error, but not two, per byte, so the bytes containing two fault bits represent a more critical scenario. The error cross section for this and the other fault modes are, of course, higher in these figures due to the low refresh frequency used during the tests than if the nominal refresh frequency would have been used.

Analysis from the *Read Retention* procedure (described in Figure 4.4) shows that SBUs and stuck bits were spotted only in the states ‘s1’ and ‘s2’. The state ‘s3’ did not return any

#### 4.4 A Comparative Study of the Technology Impact on the Neutron-induced Effects



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**Figure 4.10** – Intermittent stuckness pattern of two bits within the same memory byte.

error in the memory cells. It happens as the write-read operations are performed one after the other, without a time interval (besides the one imposed by the controller part of the system), and also, each operation in the memory cell (i.e., write, read or refresh) restores the cells charge. The fact that no errors were observed in state ‘s3’ is in line with the SBUs and stuck bit fault mechanism. It suggests that there is a degradation of the retention time of the cells and shows that the cell, even with a degraded retention capability, can retain the charge for a minimum time.

A further evaluation was performed after irradiation in the memories B2, D2, and F2. A write-read operation was performed with both solid data patterns. It is a procedure that enables the identification of stuck bits after the test. Also, using a nominal refresh rate, the same operation was performed, showing a significant decrease in the number of stuck bits, which is directly related to the fault mechanism. The results are presented in Table 4.2.

**Table 4.2** – Number of Stuck Bits After Irradiation According the Refresh Rate.

DUT ID	Node Size	Refresh Rate			
		6.1 kHz		128 kHz	
		Solid ‘0’	Solid ‘1’	Solid ‘0’	Solid ‘1’
B2	110 nm	7611	7954	32	48
D2	72 nm	786	876	1	2
F2	63 nm	589	631	0	0

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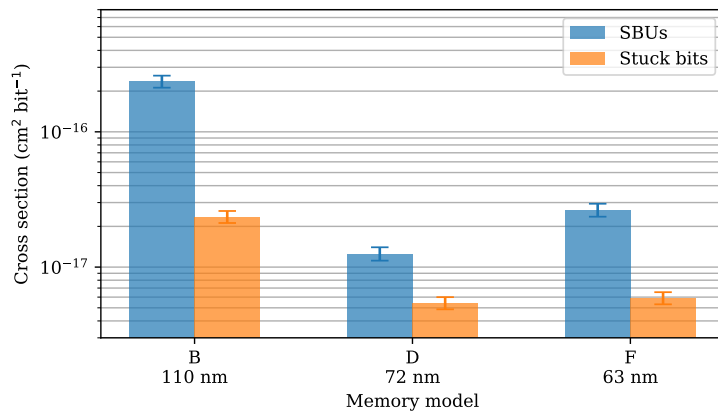
Furthermore, during the tests, the current was monitored by the latch-up monitors, which did not spot any occurrence of SELs.



#### 4.4.5 Comparison among the different technology nodes

Comparing the results obtained for the different device types B, D, and F, what can be seen is that type B is more sensitive than the others regarding SBUs and stuck bits. However, the other two device types D and F, with node sizes 72 nm and 63 nm respectively, present very little difference in their sensitivity, with type F showing a slightly increased SBU cross section over type D in Figure 4.7.

The differences between the sensitivity of the memory devices are likely affected by other design changes in the devices than just the change of node size since the sensitivity evolution is not following a visible trend with the technology node scaling. This is shown on Figure 4.11, which presents the combined SBU and stuck bit cross sections for each tested device model. In between two consecutive generations of technology nodes, there are effects coming from architectural and material improvements that tend to reduce the neutron-induced effects and other parasitic phenomena. On the other hand, the technology shrinking might lead to a higher radiation sensitivity for the individual cells. On this basis, we can consider that the transition from model B to D, the architecture, and material improvement had a larger effect than the shrinking. Also, since model B has the largest node size at 110 nm, the higher sensitivity and error cross section could be related to this memory having a larger cross sectional area of the sensitive volume due to the larger node size. For the transition from D to F, the shrinking seems to be slightly stronger than the architectural and material improvements (if any). However, the exact changes in the structure and design of the memories between models are not known to the authors.



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**Figure 4.11** – The SBU and stuck bit cross sections for the tested devices as a function of the technology node size. The cross section at each point is the combined for the two tested samples of each model.

### 4.5 Conclusion

In this Chapter, a comparative study on the neutron-induced effects on three different technology node SDRAMs is presented. From the realized tests, the induced effects were analyzed, leading to the identification of SBUs, and intermittently stuck bits. Also, on very specific occasions, we identified the occurrence of two bit-flips or two stuck bits in a single byte.

The cross sections for the different kinds of faults were estimated for each DUT, showing that the difference in radiation sensitivity between the three different memory types seems to come not only from the technology node sizes but also from other changes in the design between the different memory generations.

Future studies of these memories using the HARSH board setup are planned and will include tests at different radiation sources, refresh frequencies, and studies of annealing of the radiation-induced stuck bits.



## Chapter 5

# An Application Case Study: Reliability on Approximate Computing Systems

This Chapter presents contents based on the author's publications [JO-1], [IE-4] and [IE-6].

Convolutional Neural Networks (CNNs) are currently one of the most widely used predictive models in machine learning [148]. Recent studies have demonstrated that hardware faults induced by radiation fields, including cosmic rays, may significantly impact the CNN inference leading to wrong predictions [149, 150]. Therefore, ensuring the reliability of CNNs is crucial, especially when deployed in safety- and mission-critical applications, such as robotics, aeronautics, smart healthcare, and autonomous driving. In the literature, several works propose reliability assessments of CNNs mainly based on statistically injected faults. This Chapter presents a framework to assess the reliability of CNN applications. In this light, this study proposes the use of realistic fault models retrieved from radiation tests and makes use of an emulator to inject the models according to experimentally computed event rates. Radiation-based physical injections and emulator-based injections are performed on three CNNs (LeNet-5) exploiting different data representations. Their outcomes are compared, and the software results evidence that the emulator is able to reproduce the faulty behaviors observed during the radiation tests for the targeted CNNs. This approach leads to a more concise use of radiation experiments since the extracted fault models can be reused to explore different scenarios (e.g., impact on a different application).

### 5.1 Assessing the reliability through fault injections campaigns

Reliability assessment is always a costly phase. It is usually carried out by artificial Fault Injections (FIs) into the application under test. Depending on how faults are injected, a simple taxonomy of FI techniques can be built [151]. **Physical-based** FIs expose the system implementation to the same external conditions with respect to the in-field application, and therefore they guarantee a precise reliability assessment. However, they are also expensive in terms of hardware resources and, w.r.t. radiation experiments, beam time. Moreover, they generally suffer from low controllability and observability, making complex the analysis of the obtained results. On the other hand, **software-based** FIs modify the behavior of the software to simulate hardware fault occurrences. The cost of software-based FI is lower when compared to physical-based FIs but it leads to a higher degree of controllability and observability. However, the precision assessment of a software-based FI strictly depends on the quality of the adopted fault models. For these reasons, **model-based** FIs can be considered a good trade-off between costs and precision. Model-based FIs work on a model of the application, i.e., usually, a hardware description language (HDL) model, where faults are injected during the model simulation or emulation. Therefore, injected faults are more close to a physical-based FI, but the simulation/emulation time can become quickly unpractical, even if high abstraction level models are used (e.g., Register-Transfer Level (RTL) model versus transistor model).

### 5.2 Related Works

In the literature, several works have been proposed in the last years for addressing the reliability assessment of CNNs. Concerning physical-based FI, it can be cited [149], where the reliability dependence on three different Graphics Processing Unit (GPU) architectures (Kepler, Maxwell, and Pascal) was evaluated executing the Darknet Neural Network [152] when exposed to atmospheric-like neutrons. In [153], the authors analyze the reliability of a 54-layer Deep Neural Network injecting faults in the network weights and input data using an accelerated neutron beam for studying transient errors and FI tests to simulate permanent faults. The inferences target floating-point values and the results show that object detection networks tend to generate wrong results when exposed to hardware faults.

Among software-based FI, Li *et al.* [154] analyzes the error propagation through different abstraction layers. The authors used an open-source framework, Tiny-CNN [155], to inject faults in specific layers. Further examples of software-based FI techniques for CNNs are

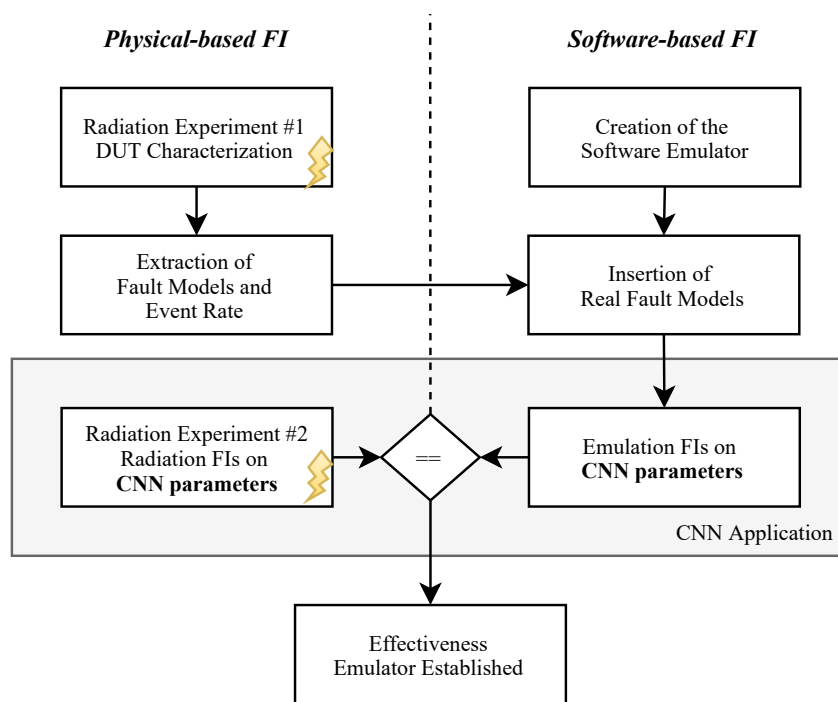
provided in [156–158]. A model-based FI approach is shown in [159], where the authors explore the resilience of an RTL model of a neural network accelerator. The work focuses on a High-Level Synthesis approach to characterize its vulnerability, injecting permanent and transient faults in various components in the RTL design.

A further framework developed to study the behavior of hardware errors in deep learning accelerators is Fidelity [160]. It is able to model a class of hardware errors (transient) in software with high accuracy, only leveraging on high-level design information obtained from architectural descriptions. In Fidelity, it is possible to inject bit-flips in weights, input images, and output neurons. In this context, it is also worth mentioning Ares [161], a framework for quantifying the resilience of DNNs. Ares targets permanent faults occurring in memory and injects errors at the application level: in weights, activators, and hidden states through bit-flips. Also, in [150], the authors applied several FIs on the configuration memory of the FPGA in order to understand the impact on the reliability of CNNs implemented on this type of device. Very recently, Xu *et al.* [162] proposed a FI framework running on a Xilinx ARM-FPGA platform to investigate the system exceptions that may occur due to the presence of permanent faults.

### 5.3 Proposed Approach

A key point to achieve a meaningful reliability assessment relies on the accuracy of the injected fault models and the possibility to emulate their behavior. For this reason, this work provides a comprehensive methodology for reproducing the incidence of real faults on a CNN application by relying on a software emulator. The flowchart of the proposed approach is shown in Figure 5.1. Starting from the characterization of the target device under an external source of errors (*radiation experiment #1*), it is extracted a real set of fault models and event rates, which are used to configure and feed the software emulator. This software-based framework is capable of injecting the fault models extracted from the DUT characterization on the parameters (i.e., weights and biases) of a CNN application. Therefore, in order to establish the effectiveness of the methodology, in parallel, radiation FIs (*radiation experiment #2*) are also carried out targeting the DUT storing the CNN parameters. Finally, the outcomes from the emulator are analyzed, and a correlation between the physical-based FI and software-based FI is provided in Section 5.6.

## An Application Case Study: Reliability on Approximate Computing Systems



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**Figure 5.1** – Flow diagram of the proposed approach.

Since memories are a high contributor of soft errors in systems [163–165], this work focuses on this type of device, which, for this purpose, has been exposed to an accelerated atmospheric-like neutron beam. The DUT is a commercial pSRAM (HyperRAM, presented in Chapter 3) memory that, in the system, has the role of storing the CNN parameters. As already pointed out, radiation-based FIs lead to a precise reliability assessment (i.e., the DUT is exposed to a realistic harsh environment) at a high cost in terms of hardware resources and exposure time. Therefore, the proposal focuses on the physical characterization of the DUT through radiation experiments to extract the event rates and fault models. Thanks to this characterization, this study makes use of a software emulator to reproduce the incidence of such realistic fault models and to evaluate their effect on CNN inferences. In particular, it targets the use of CNNs for edge computing and, therefore, for low-power embedded devices with limited resources. In our scenario, the CNN is implemented as a bare-metal application executed on a low-power CPU. The ultimate goal is to have the flexibility of a software-based fault injector with a reliability assessment precision close to the physical one, thanks to the characterization made on the actual device in realistic environmental conditions (through an accelerated neutron beam).

The noteworthy difference between the above-mentioned existing FI frameworks and the proposed one is the injection methodology and the closeness to physical injection. While

most of the approaches that can be found in the literature rely on injecting random errors in a statistical way, our emulator injects faults based on realistic fault occurrences and more real fault models (such as block errors that are generally not considered) derived from actual radiation test campaigns. Moreover, the occurrence rate of the different fault models also reflects the actual experimental data (error cross section).

## 5.4 Radiation Experiments

The radiation test campaigns [107, 144] were carried out at the Rutherford Appleton Laboratories, UK, where an atmospheric-like neutron spectrum is delivered in the ChipIr beamline at the second target station of the ISIS neutron source. The ChipIr facility provides a neutron flux of about  $5 \times 10^6$  n/cm<sup>2</sup>/s for energies above 10 MeV [32]. More details about the beamline are given in Subsection 3.4.2.

First, in Subsection 5.4.1 it is provided an overview of the fault models that have been extracted from the DUT characterisation procedure detailed in Chapter 3. Next, in Subsection 5.4.2, it is presented the radiation tests on CNN applications and introduced a test scenario, where the DUT is storing only the parameters of a CNN (i.e., the weights and biases). With the presented scenario characteristics and correlating the results obtained by the DUT characterization, it is estimated the number of occurrences of the three different fault models during the execution of CNNs (Subsection 5.4.3). These outcomes are the basis for using the emulator in which the real fault models identified under radiation are injected in CNN applications, leveraging software-based FI and allowing an in-depth analysis.

### 5.4.1 DUT Characterization

The DUT is the S27KS0642GABHI020, a 64 Mib HyperRAM<sup>TM</sup> self-refresh DRAM manufactured by Cypress Semiconductor. The evaluation of the device is based on the execution of two different memory test modes: static and dynamic. The static test mode consists of writing the memory cells with a known data pattern (e.g., solid ‘0’, solid ‘1’, and checkerboard patterns). The memory is then exposed to radiation to reach a defined particle fluence, and finally, a readback operation is performed to collect radiation-induced faults [110, 111]. Moreover, applying a dynamic test mode aims to identify functional faults during the emulation of real applications that constantly access the memory with write and read operations. The dynamic mode was executed using four different memory test algorithms: March C-, Dynamic Stress, Dynamic Classic, and mMats+ [110, 113]. The DUT was exposed to a cumulative neutron



fluence of about  $8 \times 10^{11}$  n/cm<sup>2</sup>, which, by considering the ChipIr average neutron flux, means approximately 45 h of experiments.

Three different types of faults were observed during the test executions. The first fault type consists of SBUs, appearing as a ‘0’ to ‘1’ and ‘1’ to ‘0’ transition. A write operation was sufficient to erase these SBUs, and they just occur once in the memory array. The second one recalls the stuck-at bit fault, which appears as permanent or temporary. The stuck-at bit fault results in memory cells that had their retention time affected by a particle impact, resulting in a cell that always returns the same value. The third type of fault consists of block errors that cause a high concern for the application due to their extension. They appear in different shapes and affect different regions of the memory. This kind of fault had been identified in four different patterns, with intermittent word errors in vertical and horizontal sequential addresses, affecting up to 2,048 addresses with the vertical pattern and 1,024 addresses with the horizontal pattern. These block errors are likely generated by a temporary malfunction of the sense amplifier or register that serves a column of the affected memory addresses. A more detailed view of this behavior is described in Chapter 3.

Table 3.5 presents the estimated cross sections and SER for each fault type. The reader should notice that the HyperRAM is not protected with ECC. Indeed, in embedded applications, its implementation may come at the cost of extra circuitry with power/performance overheads. For this reason, all occurrences of SBUs and stuck-at bits are considered without any filtering. Since CNNs have inherent resiliency to faults [166], the use of memory without ECC is justified. On the other hand, block errors may be catastrophic for a safety-critical application since they generate more than one bit-flip per word. Thus, in any case, the introduction of ECC would not be capable of protecting the system against this kind of fault. It is important to underline that the presented DUT characterization results can be exploited to set up a fault injector to evaluate the behavior of any kind of application running on a computing system equipped with the chosen pSRAM. Furthermore, the presented experimental methodology itself can be clearly applied to any other memory device.

### 5.4.2 Radiation Tests on the CNN Application

This section presents the radiation tests performed on a CNN application. These tests target the evaluation of the radiation-induced impact on the application and also are the base to verify the correctness of the emulator outcomes. To establish an actual case study, the analysis of the radiation-induced impact on a CNN application is done by using three different neural networks with different data types based on the same LeNet-5 [167] architecture. Although proposed in 1998, LeNet-5 is currently being used as a valid and popular benchmark to introduce advances in research and present new ideas. Furthermore, the advantage of

its adoption is mainly due to the size meeting the constraints of the embedded system environment with limited storage capacity. For the same reason, the simulation time required to run inferences during radiation tests is contained, with associated costs. Targeting a more complex embedded system, where the resources constraints are more relaxed, the use of deeper CNNs and larger datasets should also be considered.

### 5.4.2.1 CNNs Implementation

The CNN architecture consists of three Convolutional Layers (CONV) followed by two Fully Connected (FC) layers and has a total of 61,470 parameters, of which 50% are in the convolutional layers. With respect to the original LeNet-5 structure, in this model, it was removed the last SoftMax layer in order to bind the last FC layer to the classification output. The model was trained on the MNIST handwritten digit dataset by using 32 x 32-pixel cropped pictures. The training set contained 48,000 images, with an additional 12,000 for the validation set and 10,000 for the testing set. The learning rate started at 0.05, with the decay of  $5 \times 10^{-4}$  every 375(\*128) iterations, and momentum was set to 0.9. The training was done by using the open-source framework N2D2 [168]. The LeNet-5 model description that was used is available in the framework itself. In this work, “accuracy” is defined as the CNN capability to correctly classify the input picture. The accuracy is computed by using the top-1 score [167]. The achieved accuracy over the 10,000 testing images is 99%.

After the training, the N2D2 framework was exploited to export the trained network as C code using three different data representations:

- *Float 32*: weights are represented by 32-bit floating-point real numbers;
- *Int 16*: weights are quantized as 16-bit integers;
- *Int 8*: weights are quantized as 8-bit integers;

The C code was ported to a Xilinx Zynq-7000 based system. This device is an SoC, which provides an ARM Cortex™ A9 processor attached to a 28 nm Artix®7 FPGA. The CNN application was ported to this embedded system with the use of three external memories: two units of the MT41K128M16JT-125, which is a 2 Gb SDRAM DDR3L from Micron Technologies, and the DUT (HyperRAM) described in Subsection 5.4.1. Furthermore, to increase the reliability of the system, the SoC configuration memory was monitored by the commercial Xilinx scrubber, the Soft Error Mitigation (SEM) core, which reports detected SBUs, and, when possible, corrects them [169]. Figure 3.2 depicts the top-level diagram of the system.

### 5.4.2.2 Test Procedure

The testing set was processed by the three versions of the network. Depending on the data representation, the accuracy of the CNN may present a slight degradation compared to the precise CNN (i.e., the one using 32-bit floating-point representation). The obtained accuracy based on the testing set (10,000 images) was 99.07% for *Float 32* and *Int 16*, and 99.05% for the *Int 8* version. It is interesting to point out that the accuracy degradation is really minor and affects only the *Int 8* data representation, which was expected because of the intrinsic error resilience of the CNN. On the other hand, the memory footprint presents a significant reduction thanks to the approximation in the data representation.

Since the memory layout for an application is divided in sections [170], which generally are:

- *text*: executable instructions,
- *data*: constants (*.rodata*) and statically allocated variables,
- *heap*: dynamically allocated variables,
- *stack*: store parameters for function calls, return addresses, and local variables.

The memories sections of the CNN code were split into two memory devices in order to restrict the source of errors and enable a higher capability of analysis. Then only the *rodata* (read-only data segment) is allocated in the HyperRAM. This section contains static constant data and is mainly composed of CNN layers weights and biases. Moreover, it uses approximately 505 kB in the *Float 32* CNN, 273 kB in *Int 16* CNN, and 154 kB in *Int 8* CNN. In this case, the CNN parameters (weights and biases) are stored in the DUT according to the compiled code with GCC, which has the following relation: *Int 8*, 1 weight/bias, 1 byte; *Int 16*, 1 weight/bias, 2 bytes, and in *Float 32*, 1 weight/bias, 4 bytes. Furthermore, during the radiation test campaigns, the boards were mounted in the setup in a configuration that exposed only the DUTs to the beam, with more than one DUT at the same time.

In addition, to have a more in-depth view of the memory behavior, at the end of each run, a readback operation in the *rodata* contents is performed, enabling the identification of SBUs, stuck-at bits, and block errors.

Henceforth, “run” is defined as the inference of a set of images (e.g., 2,000 or 1,000 images), starting from image ‘0’ up to the last image within the dataset or when the execution is stopped. This definition is done since some runs did not achieve the end of their execution once a functional interruption occurred, which did not affect the DUT (HyperRAM), but other parts of the computation system. In these cases, it is considered for calculation only the processed images within a run.

During the first part of the test, the target was the inference of 2,000 images per run. However, mostly for the *Float 32* version, which demands more time to be completed, the computing system suffered a functional interruption, and the execution failed before its end, resulting in runs without the readback operation. The radiation experiments were performed under an atmospheric-like neutron beam. Neutrons interact with matter and, through the processes of elastic and inelastic scattering and nuclear reactions, result in charged nuclear recoils [82, 83, 12]. When the neutron beam impinges on the DUT, the generated recoils might not only lead to the SEEs in the device itself, but also be scattered in its vicinity, affecting the surrounding devices. Then, considering that the execution time of the *Float 32* version is higher when compared to the other versions (*Int 8* and *Int 16*), and adding it to the time needed to complete the 2,000 inferences, the probability of having some particles hitting other parts of the setup electronics increases within a run with these characteristics. The dataset was then reduced to 1,000 images to increase the possibility of having complete runs. Additionally, the data were filtered in order to consider only the part concerning the inferences before the controlling system failure. The data concerning each inference are independent, so all the data coming up to the last non-failing inference (at the controlling system level) can be considered good for the analysis. This choice was adopted in order to optimize the use of the available beam time by stopping the ongoing run after a fixed timeout in the communication between the controller part and the acquiring system and then starting a new run. Furthermore, concerning the failure in the controlling part of the system, this was not explored since it was out of the scope of this study.

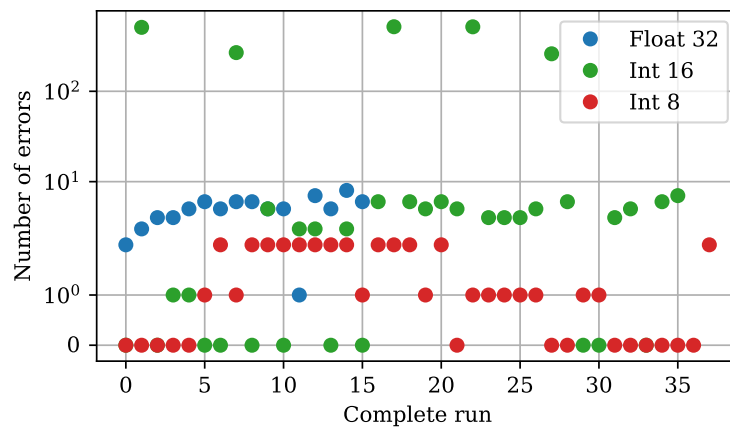
From the total number of runs, 57.96% were completed. For the three CNN versions, the golden accuracy for both datasets was the same, 99.15% (2,000) and 99.30% (1,000). During the tests, the number of inferences for each CNN version was similar. The number of inferences were 44,370 for *Float 32*; 57,680 for *Int 16*, and 52,595 for *Int 8*.

### 5.4.2.3 Test Results

Figure 5.2 presents a summary of the readback operation performed in the memory addresses containing the CNN weights and biases. The graph presents the number of errors identified in these addresses after executing a run of the CNN. A bitmap is generated from the readback operation, and it presented the same effects on the memory running the CNN and the ones from the DUT characterization test. From the five-block identified errors, all of them appeared as a vertical line of errors. In Figure 5.2, they are represented as the five highest points (above  $10^2$  in y-axis), and they were identified only in the *Int 16* version. Most of the runs with *Float 32* version did not reach the readback operation, which may result in the lack of identification of this kind of effect. Also, for the *Int 8* version, the memory usage is low, and

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it is kindly possible that block errors occurred in the memory but in an address range that was not used by the application. An example of a block error is depicted in Figure 5.3, where the red lines are used to delimit the region. The grey zones represent the memory region used by the CNN application, and each bit identified with an error appears as a black pixel. A zoom-in is added to enhance the bitmap visibility.



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**Figure 5.2** – The number of bytes with errors identified with the readback operation performed at the end of each run.

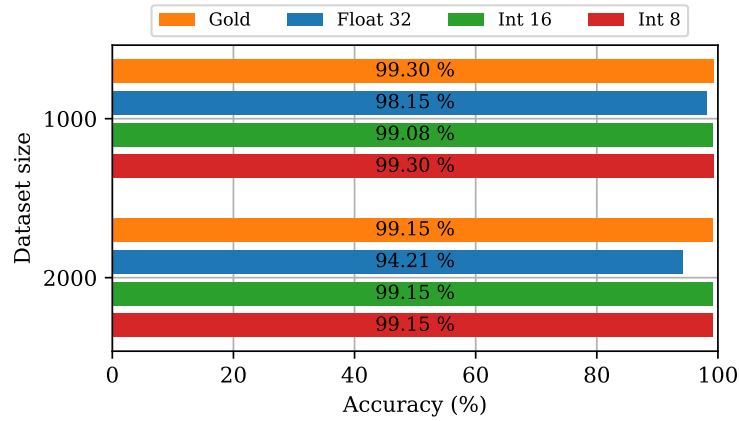


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**Figure 5.3** – Bitmap obtained from a readback operation after a run of a CNN *Int 16* version. Each pixel represents a bit; each bit that was identified with an error appears in black. The red lines are used to limit the region. The grey zone represents the memory usage. Zoom-in is added to increase the visibility of the block event.

The total accuracy for the proposed scenario is presented in Figure 5.4. This graph considers the total images per data representation and targets the dataset size used during the runs. The expected result is presented, showing degradation in the *Float 32* and *Int 16* versions. All the runs with the *Int 8* version returned the expected value. Additionally,

from the total runs, 6.37% presented a difference in the final accuracy. In which, Table 5.1 summarises these faulty runs by presenting the first image with a faulty inference and the final accuracy obtained from this run.



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**Figure 5.4** – Accuracy obtained from the results of the proposed test scenario.

From these faulty runs, one case, in particular, was able to increase the final accuracy by resulting in the correct inference of some digits when compared with a non-faulty (gold) run, where the inference results in a wrong prediction. This behavior occurred for two images in the faulty run number 10 (according to Table 5.1), where the gold run returns the digit ‘3’, being the expected the digit ‘5’. This run, where a block error was identified, resulted in the right value (‘5’) for both images, and the final accuracy increased from 99.3% to 99.5%. This case is really interesting and proves that CNN resilience assessment is quite different with respect to classical applications. The difference stems from the fact that CNNs are always an approximation of a function, in our case, a classifier. Thus, a fault can deviate the behavior of the CNN not only from good to wrong prediction (the majority of the cases) but also from **wrong** to **good** prediction.

The second case is related to an execution based on the *Float 32* version (faulty run number 5), where the output vector returned all the values as a floating-point exception (NaN, “Not a Number”), which resulted in an invalid floating-point operation. This behavior invalidated the top-1 score, and the final output was defined as a digit ‘0’. Again, this case is really interesting because it cannot be considered as a usual silent data corruption (that is, by definition, non-detectable). Here, by analyzing the CNN outputs, it is possible to detect the faulty behavior and thus trigger an error signal/trap.

For the other faulty runs, targeting the complete ones, in four of them, a block error was identified during the readback operation. The other two presented a particular behavior. First, run number 7, the output vector presented the corrected top-1 score, but the output

Table 5.1 – Summary of the runs that return a faulty accuracy based on the proposed scenario tests.

Faulty run	CNN version	Dataset size	First faulty inference [image no.]	Run accuracy [%]	Expected accuracy [%]
1	Int 16	2,000	1,345	99.10	99.15
2*	Float 32	2,000	1,384	84.36	99.09
3	Int 16	2,000	583	99.10	99.15
4*	Float 32	2,000	120	19.96	99.24
5*	Float 32	1,000	720	98.91	99.24
6*	Int 16	1,000	988	98.00	99.30
7	Int 16	1,000	102	99.20	99.30
8	Int 16	1,000	720	93.60	99.30
9	Float 32	1,000	673	70.40	99.30
10	Int 16	1,000	189	99.50	99.30

\* Incomplete runs.

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application returned a faulty inference, giving a digit ‘0’ instead of ‘2’. This result may be correlated with a register or a variable allocated in the external memory (DDR3). Second, run number 9, after the first faulty inference, the output vectors returned the same wrong value for all subsequent inferences, having the digit ‘3’ as a result of the top-1 score. Also, it is interesting to highlight that the incomplete runs presented similar behavior.

### 5.4.3 Execution Soft-Error Rate

To extract the expected number of events within a run, based on the SER (3.9), it was defined the Execution Soft Error Rate (E-SER) as:

$$E - SER_{SBU | stuck-at} = \sigma_{bit} \times M \times \bar{\phi} \times t \tag{5.1}$$

where  $\sigma_{bit}$  is the calculated cross section for SBUs or stuck-at bits,  $M$  is the memory size in bits used by the application (stored in the DUT),  $\bar{\phi}$  is the average neutron flux during the test campaigns, and  $t$  is the application execution time in seconds. The same approach is used to define the E-SER related to block errors, in this case, since the block errors are device

related, the rate is defined as:

$$E - SER_{BE} = \sigma_{\text{device}} \times \bar{\phi} \times t \quad (5.2)$$

From the E-SER definition, it is possible to calculate the expected event rate based on the presented radiation tests. The calculated values are presented in Table 5.2.

**Table 5.2** – Estimated event rate for the both test scenario. The results are calculated based on the definition of (5.1) and (5.2).

Dataset size	CNN version	E-SER [events/run]		
		SBUs	Stuck bits	Block errors
1,000 images	Float 32	0.84	0.43	0.32
	Int 16	0.24	0.12	0.17
	Int 8	0.08	0.04	0.10
2,000 images	Float 32	1.53	0.79	0.59
	Int 16	0.48	0.25	0.34
	Int 8	0.17	0.08	0.21

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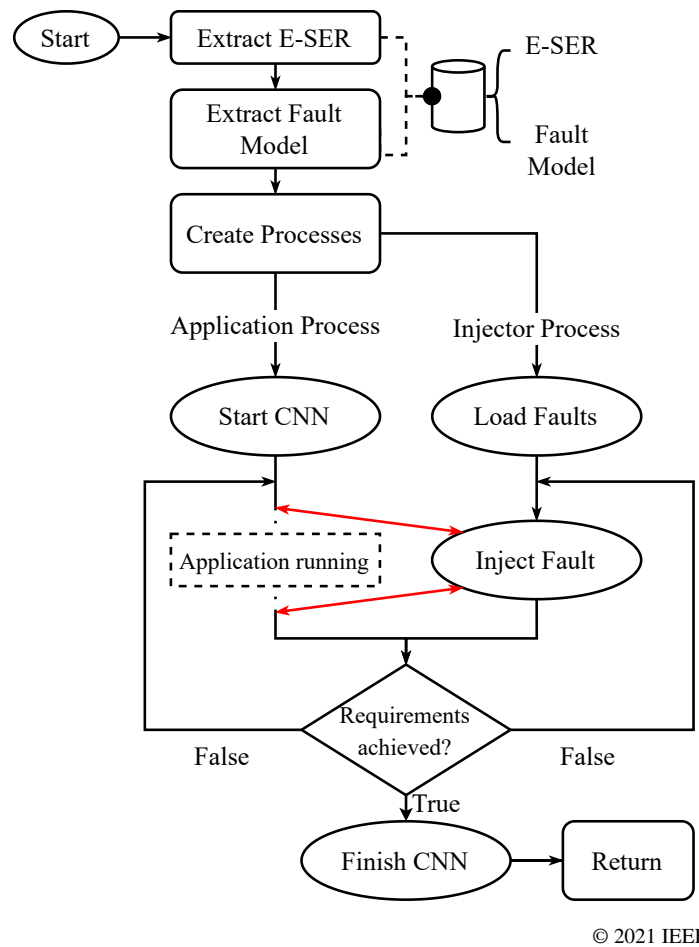
## 5.5 Emulator

Three types of radiation-induced faults were extracted from the execution of static and dynamic test modes on the HyperRAM memory: SBUs, stuck-at bits, and block errors. Since the occurrence of such faults was independent of the running application (the characterization tests and the CNNs were running on separate DUTs in the radiation tests), a software emulator was used to reproduce their incidence and to assess their effects on CNN applications.

Figure 5.5 depicts a top-level diagram of the emulator. The application process is responsible for running the target neural network, and the injector process is responsible for introducing errors in memory locations. Both processes are executed in parallel and share the same memory resources. Also, they are implemented with concurrency control mechanisms. The E-SER and the fault models should be provided, and the injector process will use these inputs to determine where and when a fault should be injected into the running application.

The emulator can work with the three observed fault models: SBUs, stuck-at bits, and block errors. While for SBUs and stuck-at bits, the faulty location, as well as the injection time, are randomly selected, emulating the block errors requires a specific parser. As





**Figure 5.5** – Emulator top level diagram.

described before, e.g., if up to 2048 sequential memory addresses are affected by an error, a block error is identified in a specific region of the HyperRAM memory. However, to inject these block errors into the application parameters, it is first necessary to see whether their corresponding addresses match (the physical addresses returned from the radiation test campaigns with the virtual addresses of the application). For this purpose, a specific parser was created to map the physical addresses of the memory to the virtual addresses seen by the main process.

Faults in the HyperRAM memory are reported at the end of the radiation test campaign. These reports include for each corrupted memory address: a timestamp, an identifier related to the target experiment, a counter named dynamic cycle, the physical address affected by the fault, the corresponding error data, and the specific cycle of the dynamic test. Then, starting from those sets of reports and knowing the virtual addresses of the CNN application, the parser was created and included in the emulator architecture. The fault lists that are provided

to the emulator have rows in the form:

$$\langle \textit{physical\_address} \rangle \langle \textit{bit\_position} \rangle \langle \textit{bit\_type} \rangle$$

Then, the emulator internally maps the addresses from physical to virtual and, if there is a match, the block errors are injected in the corresponding memory addresses of the application. The emulator can inject in both weights and biases of the CNN applications, that is the same portion of data allocated in the *rodata* memory section under radiation (Subsection 5.4.2).

## 5.6 Results Analysis

In this section, a correlation between the results obtained during the radiation experiments is done alongside the analysis of the outcomes from the emulator experiments. Experiments were performed on three different CNN applications based on the LeNet-5 model; the same CNNs that were used for the radiation experiments described in Subsection 5.4.2. Since the emulator can inject in both weights and biases parameters, it is capable to exactly reproduced the configuration of the proposed radiation test scenario, where the *.rodata* section of the memory hosting weights and biases was under radiation. Therefore, the same dataset of 1,000 images was chosen from MNIST for a single run. For every CNN application, the injection campaigns of the three fault models (SBUs, stuck-at bits, and block errors) were driven by the event rate parameter defined in Subsection 5.4.3 and calculated in Table 5.2.

### 5.6.1 SBUs and Stuck Bits

The first set of experiments dealt with SBUs and stuck-at bits for all the targeted CNNs. For each of them, the emulator was configured to carry out five different experiments with the two fault models. First, the E-SER retrieved from the radiation test campaigns was used to assess the CNNs reliability. Then, it was tuned to study worst-case scenarios on the same CNN application. The target is the evaluation of the CNNs resilience when a growing number of SBUs or stuck bits affected the network weights and biases at a random time. Both the faulty weight/bias location and the bit position within it are randomly chosen. Then, SBUs are injected through bit-flips, while stuck bits introduce a permanent ‘0’ or ‘1’ in the specific bit position of a given weight or bias.

The error rate for the injection campaigns are provided in Table 5.3. At the beginning (row *1x*), the emulator was set up with the nominal E-SERs for both SBUs and stuck-at bits (the one calculated in Table 5.2). Then, the E-SER was incremented by 25 times (*25x*), 50 times (*50x*), 75 times (*75x*), and 100 times (*100x*). Columns 2 and 3 from Table 5.3

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**Table 5.3** – Details of SBUs and stuck-at bits injection for the CNNs *Float 32*, *Int 16*, *Int 8* with an increasing E-SER: 1x, 25x, 50x, 75x, 100x.

E-SER	<i>Float 32</i>			<i>Int 16</i>			<i>Int 8</i>		
	SBUs <sup>a</sup>	Stuck bits		SBUs <sup>a</sup>	Stuck bits		SBUs <sup>a</sup>	Stuck bits	
		Stuck bit <sup>a</sup>	Total <sup>b</sup>		Stuck bit <sup>a</sup>	Total <sup>b</sup>		Stuck bit <sup>a</sup>	Total <sup>b</sup>
1x	0.84	0.43	25	0.24	0.12	6	0.08	0.04	2
25x	21	11	550	6	3	150	2	1	50
50x	42	21	1,050	12	6	300	4	2	100
75x	63	32	1,600	18	9	450	6	3	150
100x	84	43	2,150	24	12	600	8	4	200

<sup>a</sup> Refers to the number of SBUs or stuck bits injected per run.

<sup>b</sup> Total indicates, in the case of stuck bits, the total number of injected faults within the 50 runs.

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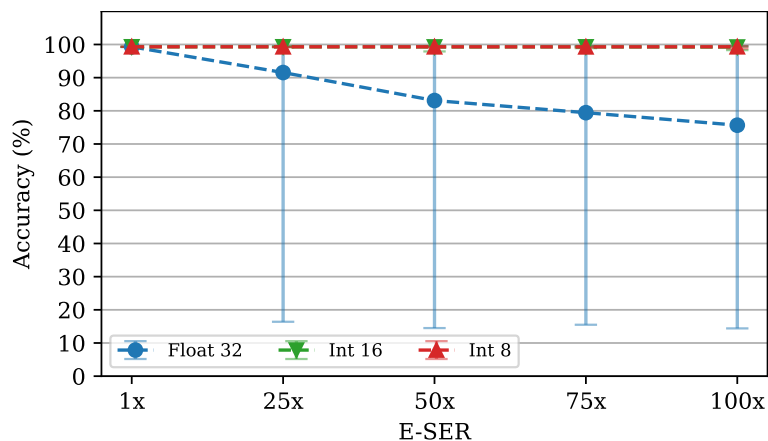
report the number of SBUs and stuck-at injected during each run. Since stuck-at bits are accumulated, in Column 4 it is reported the total amount of faults that have been injected at the end of all runs. The same reasoning is applied to the other two CNNs. It is worth reminding that a run is defined as the inference of a set of 1,000 images from MNIST. A golden run (run without injected faults) over this set achieves the 99.30% accuracy for the three CNNs.

As for the nominal E-SER (*1x*), injecting a non-integer number of SBUs or stuck-at bits during a run was not feasible. Therefore, they have been approximated as follows:

- *CNN Float 32*: For SBUs, one single random fault was injected during a single run; for stuck-at bits, one single fault was injected every 2 runs.
- *CNN Int 16*: For SBUs, one single random fault was injected every 4 runs; for stuck-at bits, one single fault was injected every 8 runs.
- *CNN Int 8*: For SBUs, one single random fault was injected every 16 runs; for stuck-at bits, one single fault was injected every 32 runs.

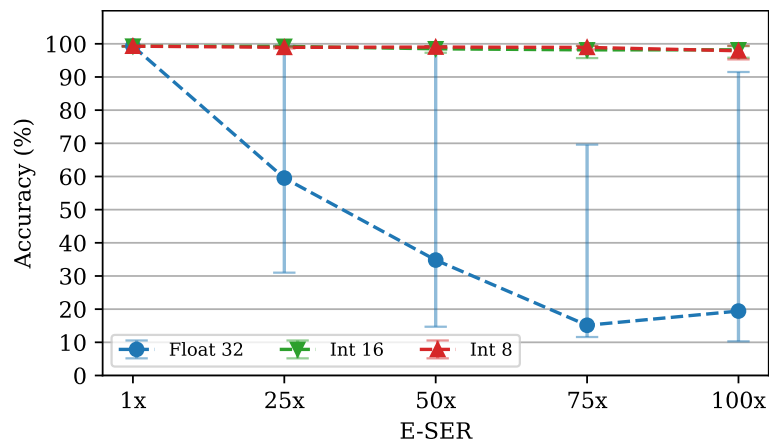
The big difference was that, while for SBUs, the fault remained active only during a single run, the stuck-at bits were accumulated over the runs. For each of them, the experiment was repeated 50 times with SBUs or stuck-at, affecting random fault locations (weights or biases), layers, and bit positions. The same reasoning was applied for higher E-SER (*25x*, *50x*, *75x*, *100x*) by injecting SBUs or stuck-at bits according to the terms specified in Table 5.3.

Experimental results are shown in Figure 5.6 and Figure 5.7, where the average accuracy value is depicted for the three CNNs under assessment, along with the minimum and the maximum value achieved during the 50 runs (small error bars). At first glance, it is apparent that the CNN application most affected by the occurrence of stuck-at bits and SBUs is the *Float 32*. Indeed, as the number of faults increases, the *Float 32* accuracy considerably decreases. This effect confirms the outcome of the radiation test campaigns, where the *Int 16* and the *Int 8* CNNs show greater resilience. Then, regarding the nominal E-SER ( $1x$ ), data show that the final network accuracy for the three CNNs was not affected for stuck-at bits, staying at 99.30%. For SBUs affecting the *Float 32* CNN, the final accuracy was equal to 99.29%: only a single run among the fifty was faulty. This is in line with the results coming from the radiation test campaigns. For instance, regarding the *Float 32* CNN application under neutron radiation, despite the occurrence of SBUs or stuck-at bit faults (as highlighted in Figure 5.2), only 1 complete run over 17 was faulty. The remaining 16 were able to withstand such radiation-induced faults without compromising accuracy. Besides, with the nominal E-SER ( $1x$ ), the two integer CNNs (*Int 16* and *Int 8*) keep the golden accuracy (99.30%) over the 50 runs, in line with the radiation test campaigns results. Indeed, as shown in Figure 5.2, despite some errors appear at the end of the inference process of *Int 16* and *Int 8* CNNs, in the latter case, they do not affect the final accuracy percentage at all. In the former, the accuracy degradation that is discussed in Table 5.1 is more related to the occurrence of block errors. Next, as the E-SER increases, the final network accuracy considerably decreases in the *Float 32* CNN. Contrarily, the increase of the E-SER slightly influences the final accuracy value in both *Int 16* and *Int 8*. Only with a E-SER  $100x$  it is observed a small degradation (respectively 1% and 2%) when the *Int 16* and *Int 8* CNNs are affected by stuck-at bits.



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**Figure 5.6** – Accuracy variation based on the increase of the SBUs E-SER for the three CNNs.



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**Figure 5.7** – Accuracy variation based on the increase of the stuck-at E-SER for the three CNNs.

Generally, the graphs point out that stuck-at bits are more critical than SBUs. Indeed, once stuck-at bits appear, they accumulate over 50 runs. A last observation in the *Float 32* CNN is related to the scenarios *75x* and *100x* for stuck-at bits. Although the quantity of injected faults was higher in the second case, the results suggest that the choice of the faulty bit positions (random in our experiments) plays a crucial role in the final accuracy assessment. Consistent with the results achieved in [154, 157], it is shown that faults affecting the exponent bits are the most critical, leading in many cases to NaN values. This specific outcome mirrors and perfectly reproduces the faulty behaviour that was observed during the radiation tests, as described in Subsection 5.4.2.

### 5.6.2 Block Errors

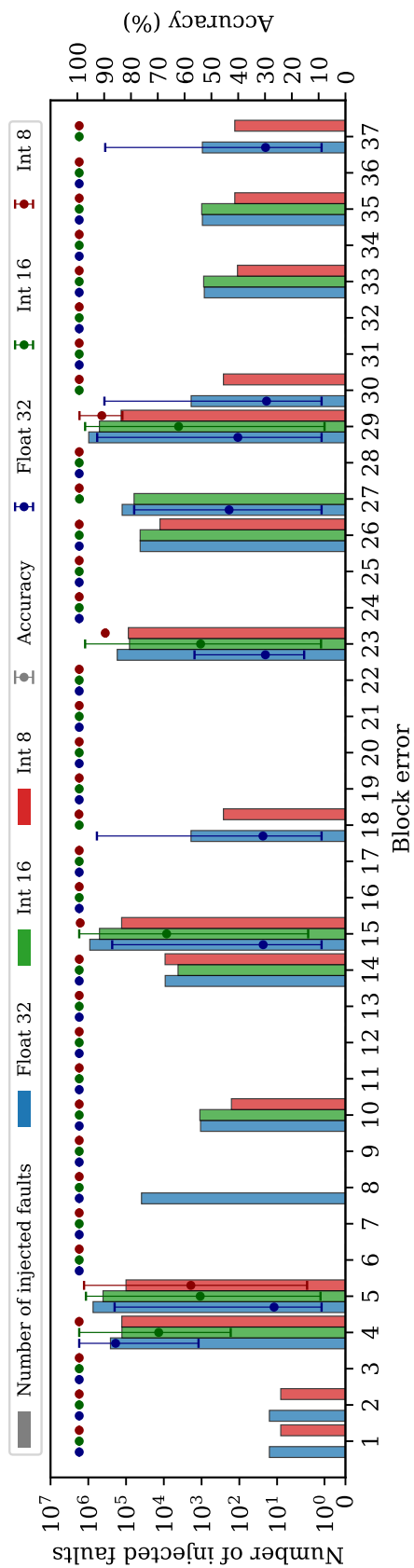
From the application of static and dynamic characterization tests during the atmospheric-like neutron radiation (Subsection 5.4.1), a total of 37 block errors (BEs) were identified in the HyperRAM memory. The purpose of the following experiments is to inject these block errors into the three CNN application parameters (weights and biases) only if their physical and virtual addresses match. To this end, the parser described in Section 5.5 is used, and if there is a correspondence between addresses, the emulator injects a stuck-at bit in the specific bit position of the respective weight or bias. For the sake of clarity, the fault lists are not randomly generated (as for SBUs and stuck-at bits), but they derive from the radiation test campaigns. In Table 5.4, for each CNN application, it is provided the details on the number of BEs matching the addresses, the total faults that can be introduced into the application parameters, and, for the sake of completeness, the memory footprint of the given CNN application in the HyperRAM memory.

The number of injected faults for each single BE is illustrated in Figure 5.8, looking at the y-axis on the left. It is also worth noticing that their incidence can also vary from a few faults injected (e.g., BE1 and BE2 with only 8 faults in the *Int 8* CNN) up to many ones (e.g., BE29 with 972,960 in the *Float 32* CNN).

**Table 5.4** – Block Error Injection Details

<b>CNN Application</b>	<b>Total Injected BEs</b>	<b>Total Injected Faults</b>	<b>Memory Footprint (kB) (.rodata)</b>
Float 32	17	3,278,656	505.81
Int 16	11	1,714,007	273.17
Int 8	15	605,922	154.11

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**Figure 5.8** – Number of injected stuck-at faults for each single block error for each CNN application (y-axis on the left). Average accuracy value for each single block error affecting at a random time a run (y-axis on the right).

First, it is calculated for each CNN the impact of each single BE occurring during a run at a random time. Dealing with random injection times, each block error was injected 50 times in 50 different random moments (during the run of 1,000 inferences). The y-axis on the right of Figure 5.8 shows the average accuracy value achieved at the end of the 50 runs. The error bars highlight the minimum and maximum accuracy values. Particularly worth of note is the minimum: it was computed at time zero, meaning that the BEs were injected before running the 1,000 inferences. In ten cases (seven in *Float 32* and three in *Int 16*) it was less than the 10%. The maximum of the error bars represents the accuracy obtained when the random time was close to the end of the 1,000 inferences, and in some cases, it was slightly higher than the golden. Considering a block error that affects the inferences, the impact on the final accuracy will clearly have a dependency on the moment that these faults are injected. Since the final accuracy is based on the 1,000 inferences result, the fault injection occurring more close to the beginning of the run will cause a more drastic impact on the final accuracy, and the opposite is also true.

The following analysis is related to the block errors E-SER presented in Table 5.2 for the 1,000 images dataset. The target is the evaluation of the CNNs resilience when a growing number of BEs affected the CNN parameters (weights and biases). In Table 5.5 it is reported the details of the injection campaign, specifically the amount of BEs that are injected in a single run. The reader should note that BEs are not accumulated over the runs, albeit being stuck at a value.

First, the emulator was set up with the nominal E-SER (1x) for every CNN application. Then, the E-SER was incremented by 25 times (25x), up to 100 times (100x). Experimental results are shown in Figure 5.9. For each point on the x-axis, the run was repeated 50 times, with 50 different random sorts of BEs and various random times. The y-axis reports the average final accuracy along with the error bars (depicting the minimum and the maximum value reached). The x-axis reports the increasing E-SER, for which the amount of injected BEs is specified in Table 5.5.

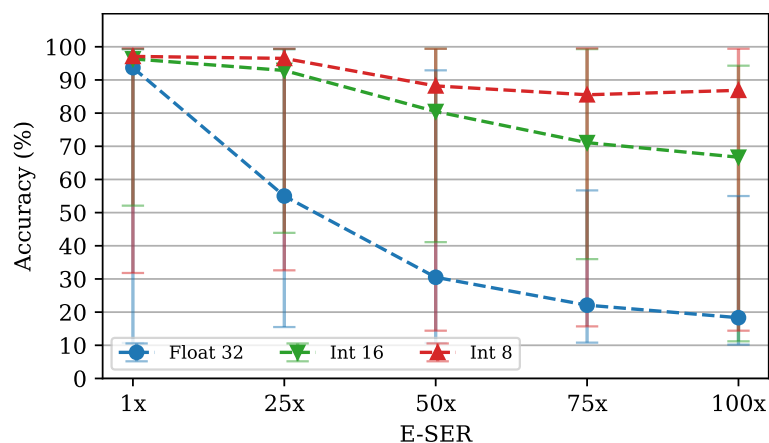


## An Application Case Study: Reliability on Approximate Computing Systems

**Table 5.5** – Details of block error injections for the CNNs *Float 32*, *Int 16*, *Int 8* with an increasing E-SER: 1x, 25x, 50x, 75x, 100x

E-SER	Total Runs	CNN		
		Float 32	Int 16	Int 8
1x	50	0.32	0.17	0.1
25x	50	8	4	3
50x	50	16	9	5
75x	50	24	13	8
100x	50	32	17	10

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**Figure 5.9** – Accuracy variation based on the increase of the block errors E-SER for the three CNNs.

Experimental results from Figure 5.9 suggest that depending on either the injection time, the BE sorting, or the amount of BEs, the final accuracy can consistently vary, with a non-negligible difference between the maximum and the minimum error bar. In particular, it was observed that the minimum accuracy value was always reached when the first injected BE belonged to the above-described set of the most critical BEs for all the CNNs.

Moreover, the graph shows that the final average decreases as the E-SER increases, in other words, as the number of BEs occurring in a run increases in the three CNNs. It is worth noting that, once again, the results show a greater resilience for the *Int 16* and, above all, *Int 8* CNNs when the number of BEs grows. This is in line with the outcome of the radiation tests.

### 5.7 Conclusion

Concluding, it is worth pointing out the following considerations. So far, an enormous effort has been spent in the literature to investigate the reliability of CNNs against transient and permanent faults (e.g., SBUs and stuck-at). At the same time, it must be said that the single fault assumption is not totally realistic. CNNs, like many other applications, mainly suffer the occurrence of multiple faults. However, the establishment of a proper multiple fault injection strategy is still an open challenge and is not a trivial task: the combinations of fault locations can exponentially explode. Therefore, the block errors injection can be considered as a first realistic attempt to cover multiple faults based on radiation tests results.

In this work, software FI campaigns were executed on the three CNNs and by exploiting the three types of faults. Experimental results revealed that, in line with the outcomes of the radiation tests, the least resilient CNN application is the one adopting the floating-point data representation; the most resilient is the one using an 8-bit integer data type.

The greatest advantage of the proposed approach consists in the possibility of injecting realistic fault models. Indeed, despite that radiation-based FIs provide precise reliability assessments, they are extremely costly. Based on the findings in this study, the proposed approach could be complementary to physical testing and may allow optimizing time and costs. Notwithstanding, since the aim of the work is to present this idea, one drawback could be the adoption of three neural networks all based on a single architecture, i.e., LeNet-5. The principal reasons are related to radiation costs and the limited storage capacity of the targeted embedded device. Nevertheless, it is important to underline that one of the goals of the work is to investigate the reliability of different data representations, therefore the need to use only one architecture.



# Chapter 6

## Summary and Conclusions

This thesis focuses on the study of radiation-induced effects, with more emphasis on soft errors in memory devices. Using COTS devices in avionics, space missions, or particle accelerators, requires understating their behavior when exposed to harsh environments, such as the radiative space ones. Furthermore, memories devices are known to be one of the highest contributors of soft errors in electronic systems and represent the best candidate for studying soft errors, mostly because of their intrinsic capability to store a fault track. Then, with a focus on space and avionics (atmospheric) environments, this thesis presented the findings of a three-year investigation into the radiation-induced effects on different memory devices when exposed to different radiation sources.

Heavy-ions, which represent a high concern in space missions, have been used as a radiation source to explore the SEEs on an SLC Flash memory. This Flash memory will be part of the RES (Radiation Effects Study) experiment, which will be launched with the MTCube 2 CubeSat. The study on this memory leads to the identification of different faults. The simplest ones are the SBUs occurring in the memory array. The bit-flip transition always occurred from a logic '0' to '1', which is expected on this technology since a charged floating gate is, by convention, normally used to represent the logic '0', and an ionizing particle passing through a charged floating gate can lead to a discharge, affecting the transistor voltage threshold and then corrupting the stored information. Additionally, the occurrence of small clusters of errors, defined as MCUs, were identified, showing the same behavior as SBUs. MCUs may appear due to charge sharing in the bit line or because of secondary particles generated at angles. These tests also reveal the occurrence of vertical lines of errors affecting all blocks within the memory plan enclosed in a single column.

The tests outcomes revealed that for lower LET, up to  $4.2 \text{ MeV.cm}^2/\text{mg}$ , the memory was susceptible only to SBUs. However, for higher LETs, the three types of errors occurred, showing the small clusters as the predominant fault. Both SBUs and small clusters (in which

## Summary and Conclusions

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the affected words belong to different memory pages) would not be sufficient to overload an ECC implementation, which is highly recommended and, according to the DUT datasheet, should be implemented with a minimum 8-bit ECC per 540 bytes of data. Additionally, the vertical lines occurred with an effective LET of at least  $10.1 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ . This large-scale data corruption event affects word columns across the memory plane. Its mitigation process includes a power cycle and an erase operation in all the affected blocks, which, if applied, will lead to data loss.

This thesis also presented the neutron-induced effects in different COTS DRAMs, which is a high concern in nuclear power plants and the atmospheric environment. First, targeting the thermal and atmospheric-like spectra, a pSRAM was used as DUT. The pSRAMs present a DRAM memory array in which the refresh electronics are embedded in the memory chip and thus appear to the host like SRAMs. This study proposed a similarity of the fault mechanism between SBUs and stuck bits. The memory cells, in which an SBU or stuck bit was identified, were studied in post-radiation tests, and their retention capability was characterized and compared. These tests have shown that the degradation is high in cells in which an SBU was identified and even higher for the ones with a stuck bit. The main difference between the two fault models is in the different level of degradation caused by the particle strike. However, concerning the fault mechanism, as presented in [99–101], the most probable interpretation is displacement damage that leads to a reduction in the retention capability of the cells. This interpretation is also supported by the thermal annealing presented on these damaged cells that recovered at high temperatures.

Additionally, the study showed that the self-refresh and an actual read operation lead to different refresh efficiency of the DRAM cell. Since the internal device design and architecture is not available, based on experimental data, it is concluded that the self-refresh circuitry accesses the memory cell for a period shorter than an actual read/write access. The DRAM functionally is based on the charge stored in the cell's capacitor. Clearly, the larger access time allows a larger stored charge.

The pSRAM study also highlighted the occurrence of SEFIs, which were defined as block errors, leading to, e.g., vertical lines composed of multiple errors within up to 2,048 addresses. Block errors can represent a real threat to safety-critical applications since the implementation of a simple ECC would not be capable of protecting the system against this kind of event.

Following the neutron-induced effects, a comparative study on three different technology nodes (110 nm, 72 nm, and 63 nm) of an SDRAM device was presented in Chapter 4. The device was subject to an atmospheric-like spectrum, and it was identified SBUs and stuck bits. The comparison, based on the bit cross section of each effect, showed a higher sensitivity on

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the oldest generation (110 nm), revealing that the single event effects tend to reduce because of architectural and material improvements despite the higher integration. Moreover, from the 72 nm to 63 nm, a slight increase on the cross section shows that in this case, the higher sensitivity due to higher integration seems to be stronger than the (potential) architectural and material improvements. It is essential to highlight that the exact changes in the structure, design, and materials between the models are not publicly available, and then, the analysis remains on a high-level perspective.

Finally, a sensitive application case study was presented to assess the reliability impact of the radiation-induced faults on CNN applications. This study was made through fault injection campaigns by emulation, based on the fault models extracted by exposing a COTS memory device under neutron irradiation. In this study, an approach was proposed to cover the multiple faults that may occur, in this case, on the target memory device. In this study, three data representations were exploited to create three versions of the same CNN model. These versions (*Float 32*, *Int 16*, and *Int 8*) were implemented in an embedded system using the same pSRAM that was characterized in Chapter 3. One of the goals of this study was to investigate the reliability of different data representations, showing, in this case study, that the most resilient implementation is the one using an 8-bit integer data type. The second goal was to explore the use of the fault models extracted from the radiation tests to define an emulator capable of injecting the realistic faults on the same CNN and that can be generalized for other applications.

In summary, the evolution of technology, which is not only related to the shirking of technology nodes but also the use of new materials, brings with each new advance the need to understand how this new technology can respond to different types of interference such as those related to radiative environments, always making necessary to study the effects of radiation on electronic devices. The studies presented in this thesis contribute to the advancement of this knowledge and evaluate its impact not only at the device level but also from an application point of view. Furthermore, the approach presented in Chapter 5 brings a comprehensive methodology to assess the reliability of applications, such as CNNs, which despite the claimed built-in resiliency, that comes with their iterative nature and learning process, there is a pressing need for evaluating their reliability, with special attention on the resource-constrained systems and safety-critical applications.



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