Improving robustness of STM32 microcontrollers subjected to impulse stress by controlling their frequency response

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Amélioration de la robustesse des microcontrôleurs STM32 soumis à un stress en impulsion par contrôle de leur réponse

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Abstract

Electromagnetic compatibility (EMC) is one of the key aspects of modern technology where different electric devices are used together to build an electronic application. In this context, the compliance of a device to EMC standards reduces the chance of critical failures improving the reliability of electronic products. EMC embraces all different kind of domains and it applies to various devices from large electric installations to portable devices or to integrated circuits (IC). This work focuses on EMC susceptibility for microcontrollers, that is the ability of a microcontroller to work correctly in a disturbed electromagnetic environment. Microcontrollers are employed in many different applications requiring different levels of immunity for different kind of stresses. This research work studies the susceptibility of standard STM32 microcontrollers against electrical fast transient events as defined by IEC 61000-4-4 standard for Fast Transient Burst (FTB). FTB test consists of injecting high voltage and repetitive spikes on the supply of the electronic devices. Studying the device behavior under stress condition and analyzing the failure mechanisms give important hints related to its immunity threshold. Some high-level system strategies have been proposed to improve the robustness of an electronic equipment to electrical fast events but few studies are dedicated to ICs or packages protection solutions. This works starts from the hypotheses of the resonances of the power distribution network (PDN) of the microcontroller being correlated with FTB immunity thresholds. As a consequence, some modelling and measuring techniques are presented to find the resonances in a specific Device Under Test (or DUT) composed of a Printed Circuit Board (PCB), a die package and a silicon die. Finally, the methodology is applied to some DUT configurations to show the correlation between the resonance characteristics of the PDN and the FTB immunity levels. This work opens up the possibility of using resonance analysis in the study of the influence of different design choices on EMC susceptibility such as package and die size and thus it gives a interesting predictive tool to be used during the design phase of a microcontroller.

Keywords : EMC, EMS, FTB, EFT, IEC 61000-4-4, Power distribution network, Resonance, Microcontroller

La compatibilité électromagnétique (CEM) est l'un des aspects clés de la technologie moderne où différents appareils électriques sont utilisés ensemble pour créer une application électronique. Dans ce contexte, la conformité d'un appareil aux normes CEM réduit le risque de défaillances critiques améliorant la fiabilité des produits électroniques. La CEM englobe tous les types de domaines et s'applique à divers appareils, des grandes installations électriques aux appareils portables ou aux circuits intégrés (IC). Ce travail porte sur la susceptibilité électromagnétique des microcontrôleurs, c'est-à-dire la capacité d'un microcontrôleur à fonctionner correctement dans un environnement électromagnétique perturbé. Les microcontrôleurs sont utilisés dans de nombreuses applications différentes nécessitant différents niveaux d'immunité pour différentes typologies de perturbations. Ce travail de recherche étudie la susceptibilité des microcontrôleurs standard STM32 aux événements électriques transitoires rapides tels que définis par la norme IEC 61000-4-4 en introduisant le Fast Transient Burst (FTB) test. Le test FTB consiste à injecter des trains d'impulsions haute tension sur l'alimentation des appareils électroniques. L'étude du comportement du dispositif et l'analyse des mécanismes de défaillance donnent des indications importantes sur son seuil d'immunité. Certaines stratégies système de haut niveau ont été proposées pour améliorer la robustesse d'un équipement électronique aux perturbations électriques rapides mais peu d'études sont consacrées aux solutions de protection dans les circuits intégrés ou dans les boîtiers. Ce travail part des hypothèses de résonances du réseau de distribution d'énergie (PDN) du microcontrôleur étant corrélées avec des seuils d'immunité FTB. En conséquence, certaines techniques de modélisation et de mesure sont présentées pour trouver les résonances dans un dispositif sous test (ou DUT) spécifique composé d'une carte de circuit imprimé (PCB), d'un boîtier et d'une puce en silicium. Enfin, la méthodologie est appliquée à certaines configurations de DUT pour montrer la corrélation entre les caractéristiques de résonance du PDN et les niveaux d'immunité FTB. Ce travail ouvre la possibilité d'utiliser l'analyse de résonance dans l'étude de l'influence de différents choix de conception sur la susceptibilité CEM tels que la taille du boîtier et de la puce et donne ainsi un outil prédictif intéressant à utiliser pendant la phase de conception d'un microcontrôleur.

Keywords: CEM, EMS, FTB, EFT, IEC 61000-4-4, Resonance, Microcontrolleur

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Contents

List of Figures

List of Tables

List of Terms

CPU	Central Processing Unit.
DSO	Digital Storage Oscilloscope.
DUT	Device Under Test.
EFT	Electrical Fast Transient.
EM	Electromagnetic.
EMC	Electromagnetic Compatibility.
EMF	Electromotive Force.
EMI	Electromagnetic Interference.
EMS	Electromagnetic susceptibility.
ESD	Electrostatic Discharge.
FTB	Fast Transient Burst.
IC	Integrated Circuit.
IEC	International Electrotechnical Commission.
IO	Input Output interface.
IP	Intellectual Property.
MIM	Metal-Insulator-Metal.
MOM	Metal-Oxide-Metal.
PCB	Printed Circuit Board.

PDN	Power Distribution Network.
RAM	Read-Only Memory.
RF	Radio Frequency.
RISC	Reduced Instruction Set Computer.
SMD	Surface-Mount Device.
STM32	32-bits STMicroelectronics Microcontroller.
TEM	Transverse Electromagnetic.
TLP	Transmission Line Pulse.

Introduction

This PhD work took place in STMicroelectronics, a leader company in the semiconductor industry, in collaboration with Polytech'Lab, a recognised microelectronic laboratory attached to University of Côte d'Azur and financed by the ANRT (Association Nationale Recherche Technologie). This thesis was carried out inside the Microcontroller Division of STMicroelectronics whose design center is held in Rousset, France. Since the very first 8-bit microcontrollers at the beginning of the 2000s, microcontroller industry was driven by the well known Moore's Law which predicted device scaling as to double the number of transistors every 2 years in an integrated circuit. The global effort to follow this trend led ICs and especially microcontrollers and microprocessors to become more and more complex allowing the development of different type of applications. In recent years Moore's law is no longer taken as the reference, indeed, nowadays, applications are not driven by the development of new technologies but instead, new application domains require More Moore technologies. As described in the 2015 ITRS annual report, these new applications dictated the need for More Moore platform to bring the PPAC (Performance Power Area Cost) value for node-to-node scaling (every 2-3 years):

- Performance: >30% more maximum operating frequency at constant energy
- Power: >50% less energy per switching at a given performance
- Area: >50% area reduction
- Cost: <25% wafer cost

. These design challenges along with the need of ICs to be used in a variety of different applications represent a real challenge for reliability and electromagnetic

compatibility. ITRS defines the reliability long term challenge (2023-2030) as follows:

> There are some special applications for which reliability is especially challenging. First there are the applications in which the environment subjects the ICs to stresses much greater than found in typical consumer or office applications.[...]In addition, aviation and space-based applications also have a more severe radiation environment.[...]Second, there are important applications (e.g., implantable electronics, safety systems) for which the consequences of an IC failure are much greater than in mainstream IC application.[1]

In this context, this PhD work focuses on a particular susceptibility aspect defined by the international standard IEC 61000-4-4, the electrical fast transient or fast transient bursts (or FTB). Fast transient burst susceptibility is often studied and analysed at the end of the electric equipment fabrication and it is rarely taken into consideration during IC design. Few studies focus on FTB immunity solutions at chip level, instead they more often cover system-level solutions as filtering or shielding technique.

This PhD objective is to find whether different design choices during the initial phase of development of a microcontroller are correlated to different immunity levels against FTB. To achieve that, the manuscript is organised in three main chapters. The first chapter serves as a general introduction to microcontrollers and EMC tests performed in STMicroelectronics. Among these tests, the electrostatic discharge, the radiated emission and the fast transient burst test are introduced. In the second half of the first chapter, some concepts about FTB propagation and amplification are explained. In this chapter the power distribution network (PDN) and the resonances associated to it are found to be a key element in the propagation mechanism of the stress.

The second chapter details the modelling techniques adopted to create an electrical model of a device under test (DUT) composed of a printed circuit board (PCB), a package and a silicon microcontroller die. Once created, this model would help finding the resonances of the PDN. The second part of this chapter reviews some of the most used measuring methods to evaluate the resonances of

the PDN and a novel one is introduced. This new method allows us to highlight internal resonances of the die PDN.

In the third chapter a real microcontroller fabricated by STMicroelectronics is taken as a test case. Modelling and measurement techniques described in chapter 2 are applied to several configurations to find the resonances of the PDN. Some correlation between the resonances and FTB immunity threshold are found and presented at the end of this chapter. These results helped giving IC designer some design guidelines to make microcontroller more robust to FTB stress.

A general conclusion ends this manuscript resuming all the key elements and concepts and giving some perspectives.

Chapter 1

State of the art of EMC

Contents

This chapter serves as a general introduction to electromagnetic compatibility for integrated circuits and it is subdivided into four main sections. Section 1 introduces the microcontroller, which is the integrated circuit used throughout the entire manuscript as the device under test. Section 2 presents some general concepts and definitions about electromagnetic compatibility. Section 3 focuses on the electromagnetic compatibility tests performed in STMicroelectronics, in this section the Fast Transient Burst test is presented and explained. Section 4 lays the foundations for the work presented in this report highlighting some of the major contributions about electrical fast transient in microcontrollers done in previous

research works. The chapter ends with a conclusion gathering the most important information to keep in mind before reading chapter 2.

1.1 Microcontroller

A microcontroller is an integrated circuit (IC) which embeds all the intellectual properties (IPs) useful to process, store and share data. The typical architecture is shown in Figure 1.1. The most important blocks are:

- Central Processing Unit or CPU whose task is to fetch, decode and execute instructions.
- Storage Units as FLASH and RAM memories which are responsible for keeping the data over time.
- Analog Units which are responsible for managing and monitoring the power supply of the system as well as providing some analog features such as analog to digital conversion, voltage references, and internal oscillators.
- Input/Output interfaces or IO which guarantee the communication between the external environment of the microcontroller and the internal processing unit.

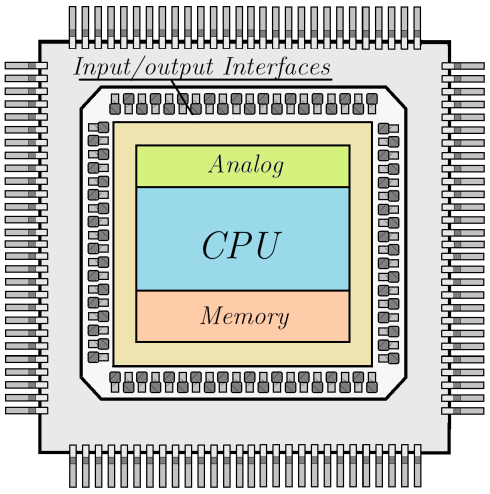


Figure 1.1: General microcontroller architecture

Microcontrollers are one of the most popular integrated circuits and they are used in most electronic applications, either consumer or industrial, which do not require too aggressive performances. This is due to their competitive cost and enormous versatility. Even though all the microcontrollers share the same macro-functions, different families of products are developed in STMicroelectronics to address different application domains.

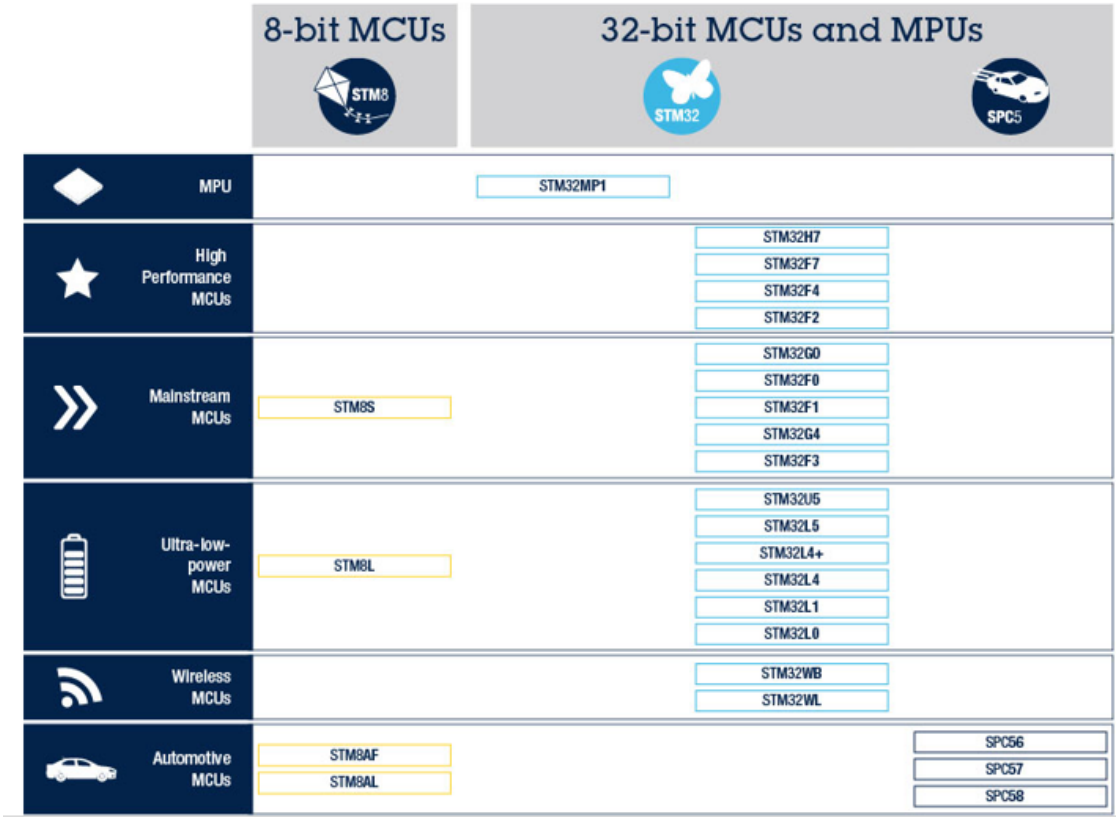


Figure 1.2: STMicroelectronics microcontrollers portfolio

As it can be seen in Figure 1.2, STMicroelectronics portfolio is varied and it is divided into three main categories depending on the internal architecture of the device. The first category is the 8-bit microcontroller which is currently designed for applications that do not require large computing capacity or complex communication protocols. The second is the microprocessor which, unlike the microcontroller, is a device characterized by a large computing capacity, higher operating frequencies, and a high number of IOs allowing effective communication with external

memories. The microprocessor is not a stand-alone device, indeed most of the silicon area is dedicated to the CPU only, reducing the analog functions and storage capacity to the minimum. Usually this kind of device is employed together with other external devices like power management IC or memories. The third category, 32-bit microcontroller family, offers the most balanced solution in term of versatility, power consumption and performance. STM32 microcontrollers are divided into many subcategories following their functionalities and electrical characteristics. All STM32 microcontrollers are based on a 32-bit Advanced RISC Machine (ARM) cortex architecture which defines the instruction set and the internal CPU architecture. Among the high-performance microcontrollers, the STM32H7 family is the one that offers the highest connectivity and memory density, ideal for enhanced graphical user interfaces. Here are some key parameters:

- 480 MHz processor operational frequency
- 2 MBytes Flash memory
- 1 MByte RAM memory
- Octospi, Ethernet and TFT-LCD communication protocols

STM32 Mainstream MCUs integrate an ARM cortex M0 + processor and it is the family that most maximizes flexibility for upgrades with minimum cost. STM32 ultra-low-power microcontrollers offer designers of energy-efficient embedded systems and applications a balance between performance, power, security, and cost effectiveness providing consumption down to hundreds of nA. The wireless microcontrollers cover Sub-GHz as well as 2.4 GHz frequency range operation providing Bluetooth LE 5.2, IEEE 802.15.4 and other widely used communication protocols. The great versatility of microcontrollers is a great commercial advantage, nevertheless it brings with it enormous scientific challenges in terms of analog design, power and signal integrity, and electromagnetic compatibility. Indeed, all these families of microcontrollers are designed to be as flexible as possible and to cover the largest number of applications while always ensuring functionality and robustness. A great amount of research and development is therefore dedicated to the study of new methodologies to make microcontrollers efficient and robust regardless of the use that the end customer will make of them. Today, electromagnetic compatibility is one of most critical areas where a part of the efforts are put into making the microcontroller suitable for all electromagnetic environments.

1.2 Electromagnetic Compatibility

1.2.1 Introduction

Electromagnetic compatibility or EMC studies the ability of an electric or electronic equipment to work satisfactorily without introducing intolerable electromagnetic disturbances to other devices sharing the same electromagnetic environment and to perform as intended without degradation in the presence of an electromagnetic disturbance [2]. EMC is divided into two major macro-areas: electromagnetic susceptibility (or EMS) and electromagnetic emission (or EMI). The EMS studies the robustness or immunity of an electronic device to electromagnetic stress. In this case, the device under test or DUT is considered as a victim and the electromagnetic environment as the aggressor. The EMI focuses on the study and reduction of electromagnetic interferences intentionally or unintentionally produced by an electronic device. In this case the DUT is considered as an aggressor and the surrounding environment is the victim. Each electronic product sold on the market must comply with many EMC standards that were defined by international organizations, these standards define the limits and methods of measuring the disturbances emitted and received. Since 1/1/1996, compliance with all the electromagnetic compatibility standards is guaranteed by the CE marking depicted in Figure 1.3.

Figure 1.3: CE Label

Today, in Europe, to obtain the CE mark it is necessary to comply with the 2014/30/EU directives which define the essential requirements to be met in terms of EMC. The typical procedure to obtain the CE mark is shown in Figure 1.4.

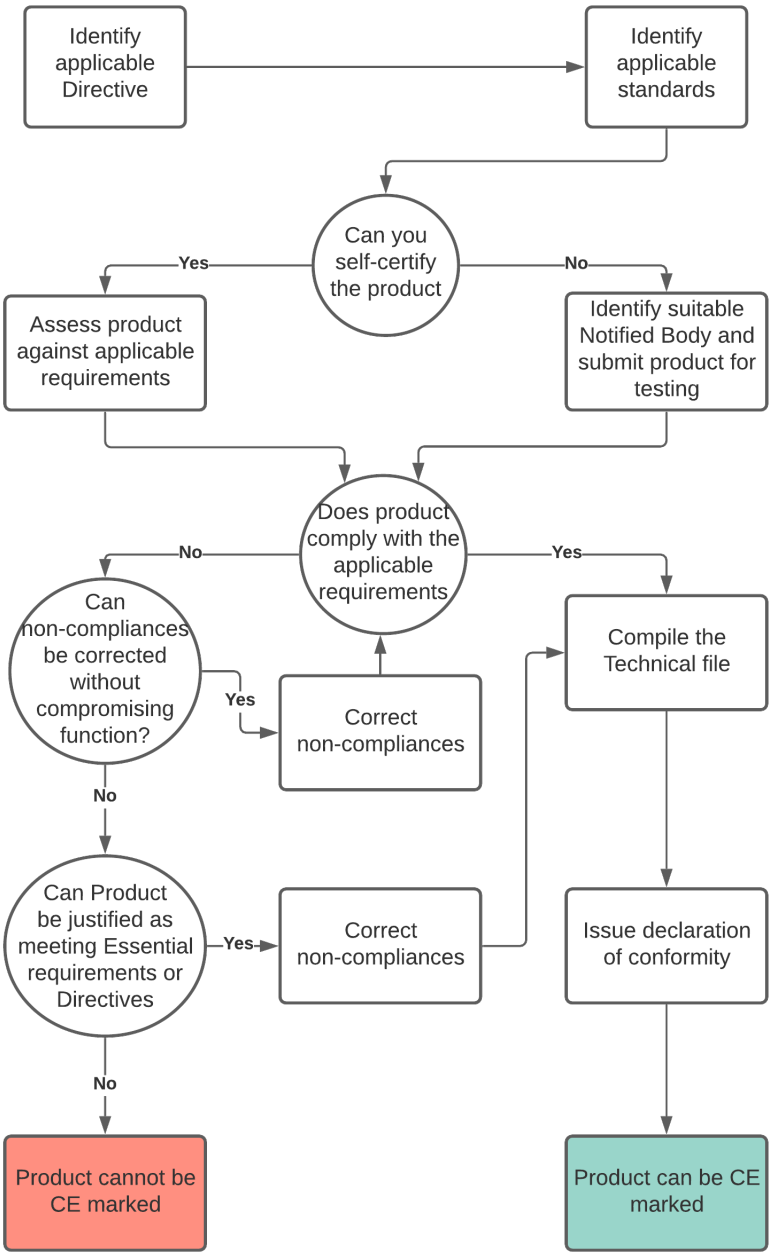


Figure 1.4: CE Marking flowchart [3]

1.2.2 Electromagnetic perturbations and coupling

The EMC studies electromagnetic perturbations and a first classification is made on the basis of the way in which these perturbations propagate. Electro-

magnetic perturbations are classified according to the medium of propagation in three types:

- **Conducted perturbations**: propagate by means of electrical cables such as power or communication cables
- **Radiated perturbations**: propagate by means of an electric, magnetic, or electromagnetic field
- **Electrostatic discharges** are due to contact with an electrically charged conductor.

Electromagnetic perturbations are injected into electronic device or circuit following different types of coupling regardless of the conducted or radiated propagation mode. We can differentiate four basic types of coupling:

- *common-impedance coupling*
- *capacitive coupling*
- *inductive coupling*
- *electromagnetic coupling*

Understanding the way perturbations are propagated is fundamental to find and design the most effective protection, thus a brief description of these types of coupling is presented below.

Common impedance coupling

Common impedance coupling occurs when two electronic devices or circuits share a common conductor, any current flowing in one device will produce a voltage on the second one. Figure 1.5 shows a typical circuit configuration affected by common impedance coupling.

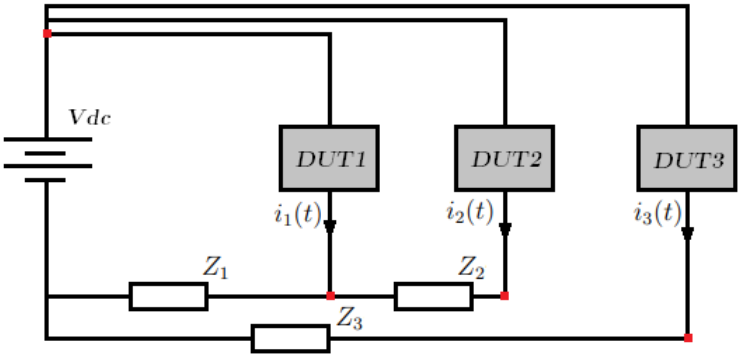


Figure 1.5: Common impedance coupling on the ground path

In this example, the ground path is common between DUT_1 and DUT_2 and the impedance of the line is Z_1 and Z_2. DUT_3 instead has its own ground path to the supply. Considering $i_1(t)$, $i_2(t)$ and $i_3(t)$ the supply current of DUT_1, DUT_2 and DUT_3 respectively, the ground reference voltage is obtained with Kirchhoff's laws:

$$V_{gnd}^{DUT_1} = Z_1[i_1(t) + i_2(t)] \tag{1.1}$$

$$V_{gnd}^{DUT_2} = Z_1[i_1(t) + i_2(t)] + Z_2 i_2(t) \tag{1.2}$$

$$V_{gnd}^{DUT_3} = Z_3 i_3(t) \tag{1.3}$$

As shown with equations 1.1 and 1.2 the reference voltage of DUT_1 is function of the current of the circuit DUT_2 and viceversa. On the other hand, as DUT_3 ground path is isolated from the others, $V_{gnd}^{DUT_3}$ does not depend on the noise generated by DUT_1 and DUT_2. Depending on the system architecture there are several possibilities to reduce or cancel the impact of common impedance coupling. Some are mentioned below:

- avoid power or signal common path between sensitive circuits and high current circuits
- reduce the impedance by using proper supply planes during Printed Circuit Board (or PCB) design
- place decoupling capacitors as close as possible to the aggressor circuit to help providing fast transient current spikes.

Capacitive coupling

Capacitive coupling occurs between two charged conductors separated by an insulating material. An example is provided in Figure 1.6.

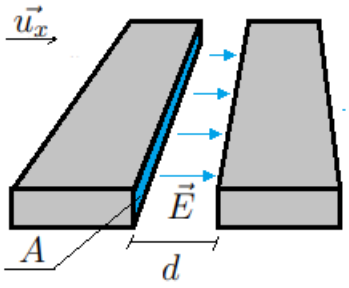


Figure 1.6: Capacitance between two conductors

The capacitance between the two conductors charged with $\pm q$ is defined as:

$$C = \frac{q}{V} \tag{1.4}$$

where V is the potential difference across the capacitor. The electric field $\vec{E}$ between two parallel conductors plates is:

$$\vec{E} = \frac{q}{A\varepsilon_0}\vec{u_x} \tag{1.5}$$

or

$$|E| = V\,d \tag{1.6}$$

From equations 1.5 and 1.6 the plane capacitance formula is found:

$$C = \varepsilon_0 \frac{A}{d} \tag{1.7}$$

Equation 1.7 is not accurate for $A \ll d^2$ but it remains a valid approximation. To obtain the correct capacitance value, the fringe electrostatic field shall be taken into account [4].

The capacitance-induced current $i_i(t)$ is equal to:

$$i_i(t) = C\frac{dv_1(t)}{dt} \tag{1.8}$$

Either increasing the distance between the conductors d or reducing the surface A are the most effective solutions to lower capacitive coupling. Ground planes are also employed to diverge electric field lines and therefore reduce the total capacitance between two conductors as depicted in Figure 1.7.

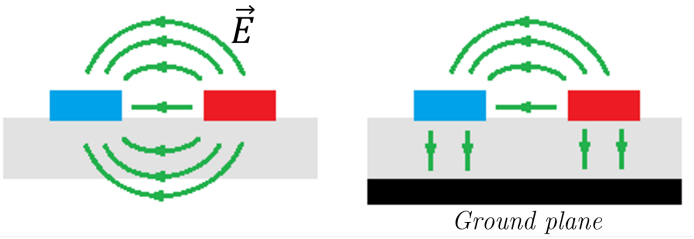


Figure 1.7: Ground plane effect on capacitive coupling between two tracks

Inductive coupling

Current flowing in a conductor produces a magnetic field H as shown in Figure 1.8.

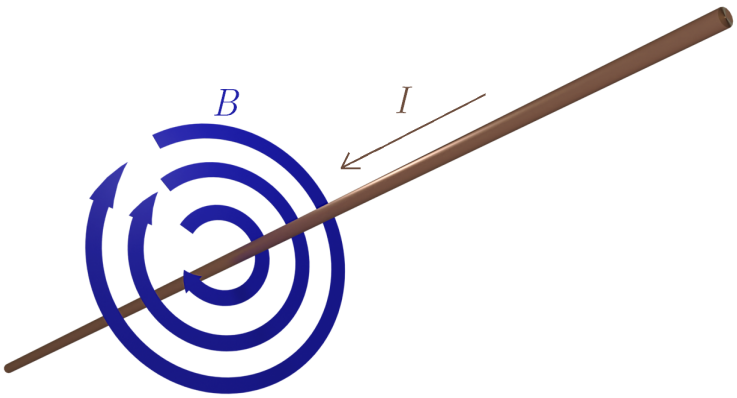


Figure 1.8: Magnetic field B generated by current flowing in a wire

The magnitude of the generated field is given by Ampère's law:

$$|B| = \frac{\mu_0 i(t)}{2\pi r} \tag{1.9}$$

If a magnetic field crosses a closed loop of conductor an electromotive force or

EMF is then produced equal to (Faraday's law):

$$V_{emf} = -\frac{d\Phi(B)}{dt} \tag{1.10}$$

By combining equations 1.9 and 1.10 we find that the perturbations generated in the victim circuit is proportional to the current variation over time of the aggressor circuit. The equation 1.11 is a good approximation if the magnetic field is perpendicular to the surface S and constant all over the loop:

$$\xi_{emf} \approx -\frac{\mu_0 S}{2\pi r}\frac{di(t)}{dt} \tag{1.11}$$

where r is the distance from the aggressor circuit. Large closed loop surfaces in sensitive circuits have to be avoided or reduced in order to diminish the inductive perturbations. This can be achieved by using short connections between different components in the PCB or by shielding the sensitive circuit with a metallic chassis.

Common mode and differential mode perturbations

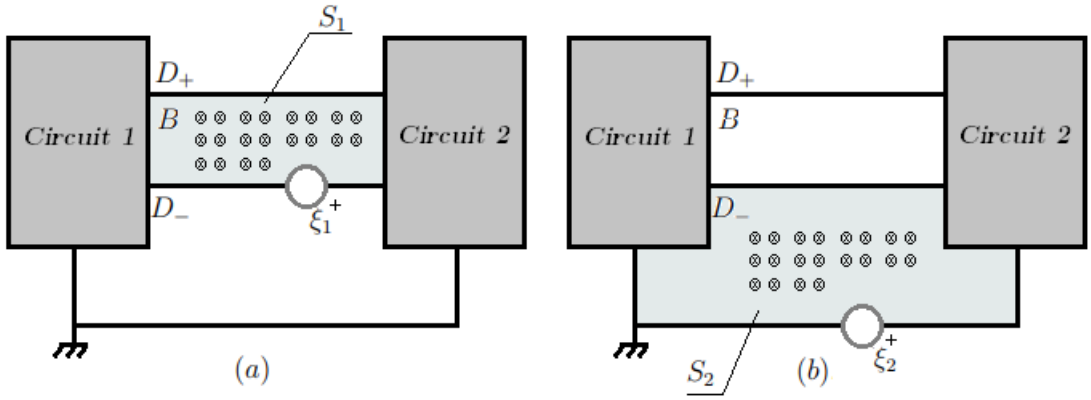


Figure 1.9: Common mode and differential mode noise generation

Figure 1.9 shows the difference between common mode and differential mode perturbation in case of inductive coupling. Consider D_+ and D_- two conductors carrying information from circuit 1 to circuit 2. Surface S_1 is the area between the two conductors. If a magnetic field goes through S_1 an electromagnetic force ξ_1 is generated in the same loop as depicted in Figure 1.9 (a). ξ_1 is considered

as a differential mode perturbance as it changes the differential voltage between the two conductors. Now consider the loop surface S_2 between the conductors and the ground reference. If a magnetic field goes through S_2, the generated EMF ξ_2 is associated to the ground loop as shown in Figure 1.9 (b). The differential voltage between conductor D_+ and D_- is not changed, instead ground reference is changed in the same way for both. In this last case, the perturbation is defined as a common-mode noise.

The most important coupling phenomena have been described, a detailed description of the EMC tests applied to STM32 microcontrollers is given in the next section.

1.3 STM32 EMC Standard Tests

Three main tests are performed to evaluate the electromagnetic susceptibility and interference of STM32 microcontrollers: the electrostatic discharge, the radiated emission and the fast transient burst test.

1.3.1 Electrostatic Discharge (ESD)

Test description

The electrostatic discharge is a common physical phenomenon which occurs between two charged materials which are brought in contact. If the electrical potential of the two materials is different, then a charge transfer takes place. There are several ways to get a material (human body included) charged like tribo-electric effect and induction. Generally, the potential difference involved in ESD events between human body and an electronic device is few kVs up to 10kVs and couples of Ampère of current for a short period of time, generally less than 100 nanoseconds. ESD events are modelled differently depending on how the discharge occurs, the most important ones are:

- Human Body Model (HBM) which represents the electric discharge from a charged human body to a grounded device;

- Machine Model (MM) which simulates a discharge from a charged machine to a grounded device;
- Charged Device Model (CDM) which represents the discharge from a charged device to a grounded equipment.

The electrical characteristic of the stress is different in each model. In particular, the differences are related to the time duration and the current intensity of the stress, Figure 1.10 resumes the electrical models and key parameters of the associated pulses taken from the JEDEC and IEC standards.

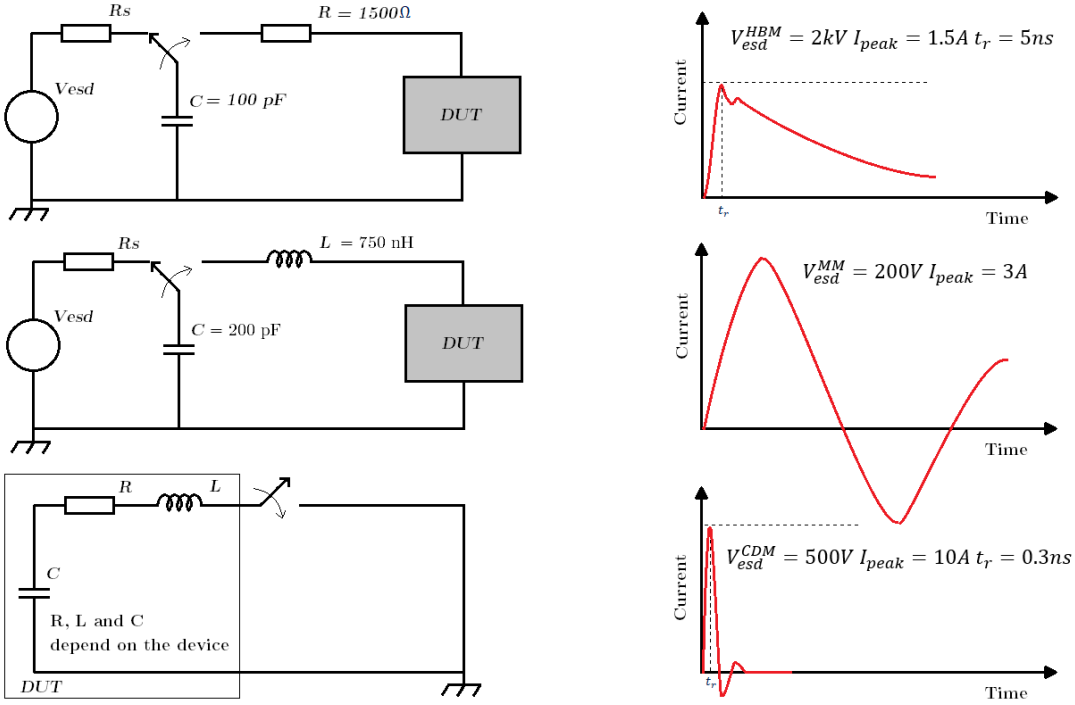


Figure 1.10: HBM (a), MM (b) and CDM (c) electrical model and waveform shape

Each of the microcontroller pin are tested with a zapping machine in PS-mode and NS-mode [5] as depicted in Figure 1.11.

For HBM, each pin is tested from 200V up to 4kV, then the device immunity is determined according to JEDEC standard as listed in Table 1.1 [6].

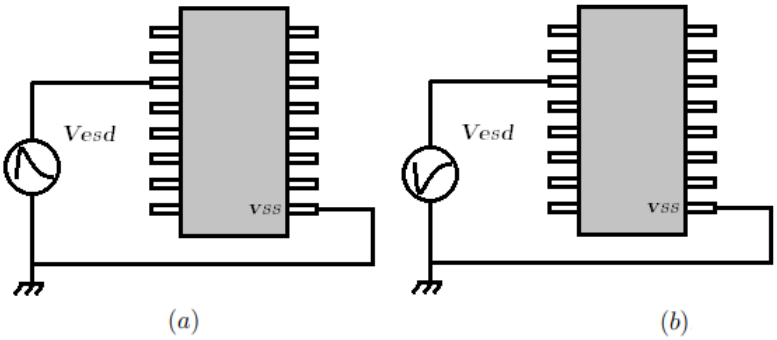


Figure 1.11: PS-mode (a) and NS-mode (b)

Classification	Voltage Range
0A	< 125
0B	125 to 250
1A	250 to 500
1B	500 to 1000
1C	1000 to 2000
2	2000 to 4000
3A	4000 to 8000
3B	> 8000

Table 1.1: HBM Immunity classification

Failure mechanism

ESD failures in microcontrollers are often related to either high current density or high temperature generation or high electric field. These phenomena lead typically to three main failure mechanisms:

- Oxide breakdown;
- Metalisation burn-out;
- latch-up.

Oxide breakdown occurs when the electric field in the gate oxide exceeds 10 MV/cm. Typically, oxide breakdown leads to low-resistance short between the transistor gate and drain/source. Metalization burn-out occurs when high current density flow in interconnections and contact causing metal melting and contact fusion. Figure 1.12 show both oxide breakdown and contact fusion on a I/O pad after applying ESD stress on it.

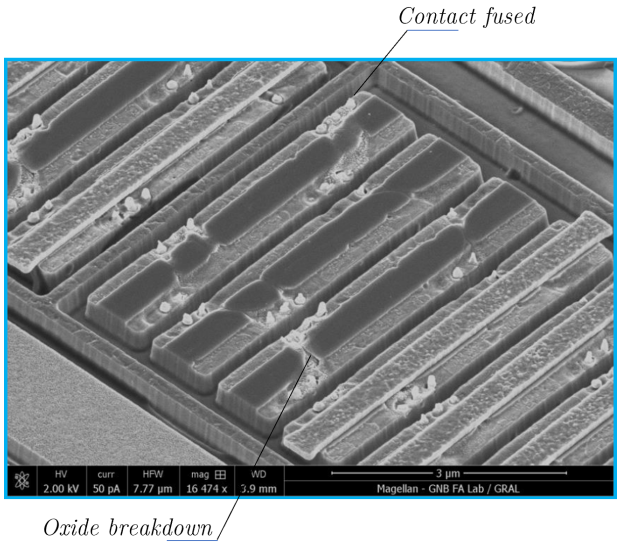


Figure 1.12: Oxide breakdown and contact fusion

Latch-up is a condition where a low conducting path is formed between a supply and ground [7], this is due to parasitic bipolar transistors polarization in CMOS technology. Figure 1.13 is a cross section of a CMOS output buffer with the main lateral and vertical bipolar transistors drawn. If the voltage on the PAD increases above the diode threshold V_{be} then the PN diode formed by PMOS drain and Nwell is forward biased. Minority carriers diffuse in to the N-well substrate and eventually reach the P-substrate region to be collected by V_{ss}. If this happens, the Q_i PNP transistor is then activated.

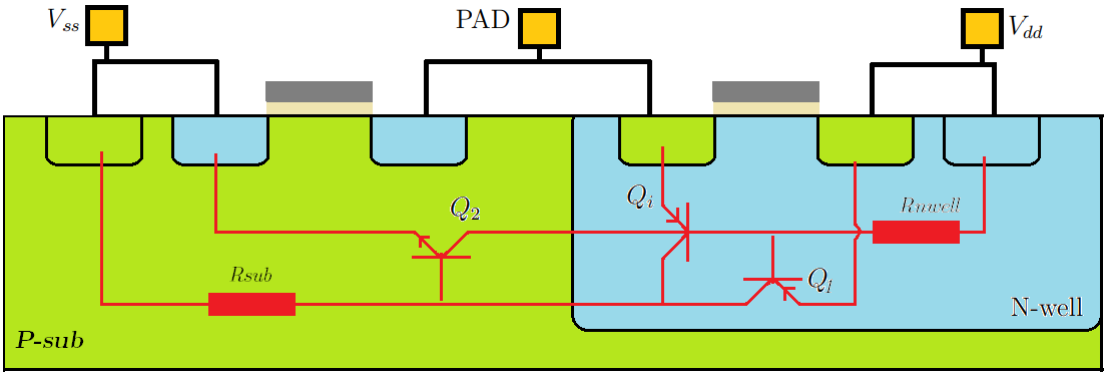


Figure 1.13: CMOS bipolar structures

If Q_i collector current and the substrate resistance are high enough, Q_2 NPN

transistor is turned on sourcing current from N-type well. Current flowing from the Nwell to V_{ss} potentially activates Q_1 PNP transistor and a positive feedback loop occurs. Under these condition a self-sustained structure is activated between V_{dd} and V_{ss} and it is shown in Figure 1.14.

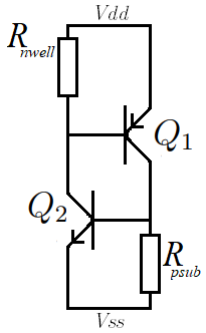


Figure 1.14: Latchup structure

Latch-up may involve high current leading to dangerous heat generation causing physical damage. Identifying potential latch-up configurations is not always straight forward as parasitic structures depend on the physical layout of the circuit and on the characteristics of the technology node in use. Nevertheless, many common techniques are employed in modern circuit to mitigate the problem as: reducing the substrate resistance path by adding several guard-ring around the critical devices or spacing the transistor elements to lower the current gain of parasitic structures. Actual latch-up test for microcontrollers relies on JESD78C standard [6]. A transient current pulse up to $\pm 100mA$ is injected into the input/output port of the devices to determine whether the latch-up phenomenon is installed or not.

Immunity solution

When ESD events occur on a IO port of the device, current must find a way to flow from the stressed pin to the ground. ESD protections are designed to divert the ESD current from sensitive circuits while avoiding the generation of high potential differences inside the die which may cause oxide breakdowns. Furthermore, ESD protection structures must be triggered by ESD events only and they shall

not interfere with the normal operation of the device. In [8] a general whole-chip ESD network protection is presented in Figure 1.15.

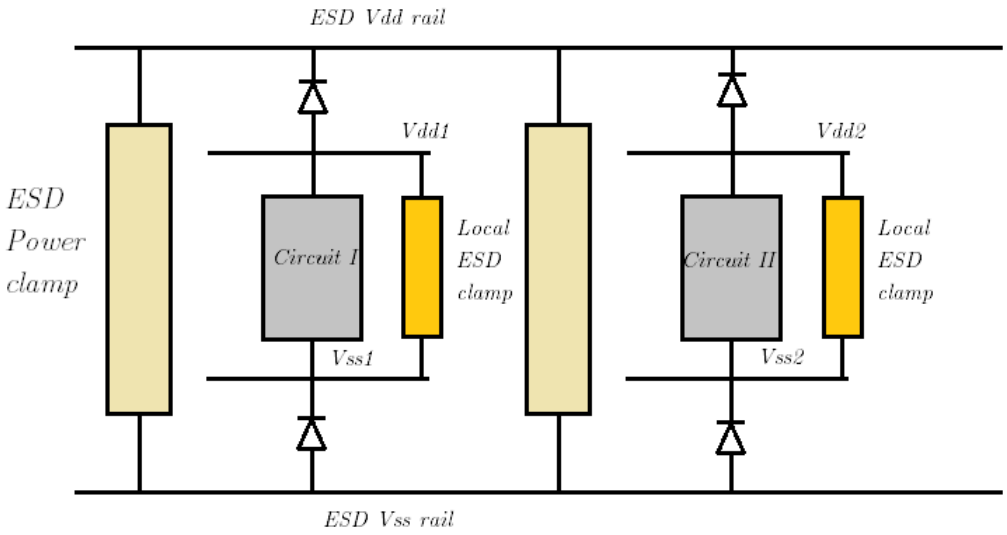


Figure 1.15: ESD structure in chip

Three main elements are identified:

- Dedicated ESD power rails to divert current from standard power rail used during normal operation;
- Low resistance and fast diodes to deviate the stress from critical path.
- ESD clamp structures which are responsible of creating a low conductive path between the stress pin and the ground.

Typically, ESD protection structures are constituted by devices which are fabricated to operate when a certain voltage level is reached across them, they are called snap-back devices. The most implemented snap-back device in CMOS technology is the Grounded-Gate N-type MOSFET (GGNMOS) [9], [10]. GGNMOS characteristic and electrical model is presented in Figure 1.16.

As drain voltage increases the PN junction becomes more strongly reverse biased causing eventually avalanche breakdown at V_{t1}. When this occurs, the large amount of current flowing in the substrate resistance activates the parasitic NPN

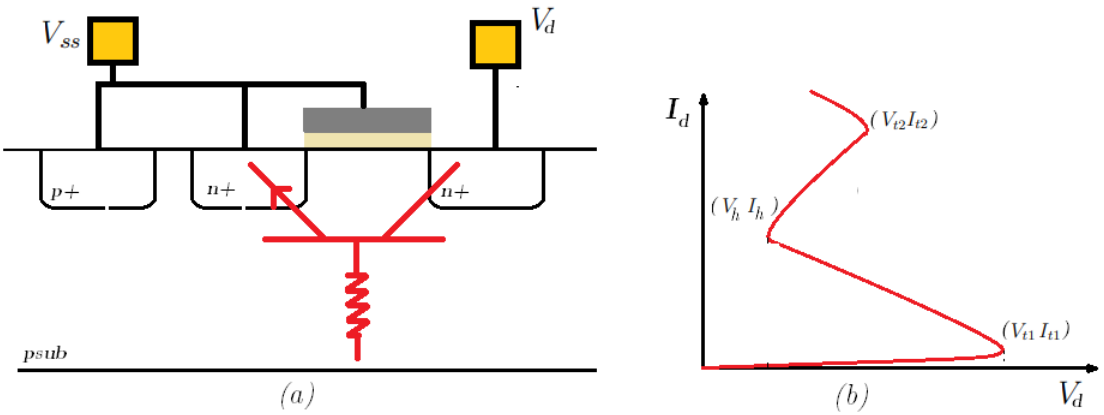


Figure 1.16: Snap-back mechanism and characteristics

structure shorting drain and source. Under these conditions, high current I_h flows in the protection while keeping the drain voltage low (V_h). If the current keeps increasing above a certain limit I_{t2} the protection goes in a thermal breakdown leading to not reversible physical damage. Snap-back devices are usually designed to be triggered with a voltage V_{t1} below the oxide breakdown voltage and to be capable of driving large amount of current before going into thermal breakdown. Several studies have been proposed to optimise the behaviour of GGNMOS to guarantee a predictive and uniform trigger threshold [11]–[14]. Other solutions consist in non-snapback based transient clamp which are analog circuits which create a low conductive path during the ESD event. These circuits are designed to guarantee the detection of the ESD event by analysing the timing characteristics and they are designed to evacuate the high current avoiding electromigration issues. Transmission Line Pulse or TLP is generally used to characterise all ESD protections [15]. TLP consists in sending a variable voltage pulse to the device under test. Electrical characteristics of the protection are extracted by combining the reflected pulse and the current absorbed by the device. TLP main advantage is the fact that the device is characterised with high voltage and current pulse for a short period of time. In that way, a full electrical characterisation is possible without incurring in thermal breakdown. Correlations between TLP results and actual HBM/CDM standard tests are subject of various studies in literature [16] making this method an interesting complementary test for evaluating ESD immunity.

1.3.2 Radiated Emission

Test description

As introduced in the previous sections, current flowing through a wire generates an electromagnetic perturbation which is described by Lenz's law. The radiated emission test was introduced to guarantee that the total EM emission of an electronic device does not exceed given limits. EM emission limits and test methodology for integrated circuits are defined in IEC 61967 [17]. Radiated emissions are measured for each STMicroelectronics microcontroller following the IEC 61967-2 standard which describes the routine to evaluate the EM emission using a Transverse Electromagnetic or TEM cell in the range 150 kHz up to 1 GHz. Within STMicroelectronics, five classes separated by four levels are defined and presented in Figure 1.17 and Table 1.2.

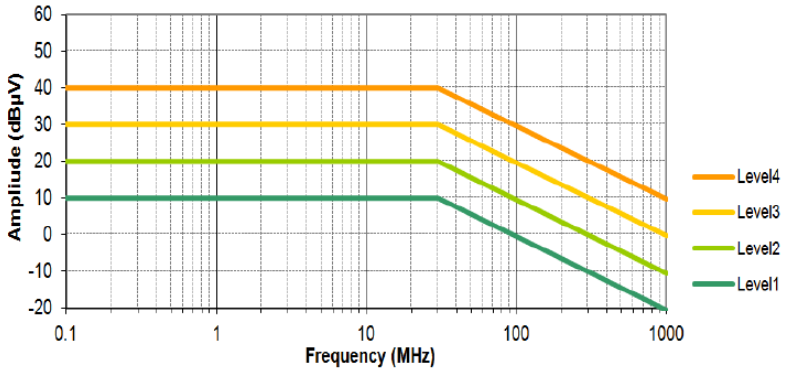


Figure 1.17: STMicroelectronics Radiated Emission levels (taken from [18])

Failure mechanism and immunity solutions

Radiated emission may be critical not only for the near electronic devices but also for the microcontroller itself, this phenomenon is called auto-susceptibility. Indeed, radiated emissions generated by a localised circuitry in the microcontroller

Classification	Actions
5	High risk. Not recommended. Require extra design measures and costs (metal shields, filtering). Module may not be able to pass the radiated emission limits.
4	May require extra design measures and use of EMC design rules. Cost to pass the module radiated emission limits.
3	Moderate risk, more flexibility in EMC design rules adherence than Class 4.
2	Minimal risk, more flexibility in EMC design rules adherence than Class 3.
1	No risk, most flexibility in EMC design rules adherence, cost reduction opportunity (single sided PCB).

Table 1.2: STMicroelectronics Radiated Emission zones

could compromise the functionality of another circuit closed to the same silicon die. Most of the time, radiated emissions cause clock glitches which put the device in an unknown and unsafe state. A previous thesis work described in details the issues of radiated emission in STM32 micro-controller and many publications cover this domain [19], [20]. In this work, many correlations between simulation and measurement were given and finally some solutions were proposed. In particular, for STM32, several techniques are adopted to reduce the overall emission such as minimizing all the current loops by having an efficient pin out distribution, reducing the rising and falling time of signal down to the minimum value required for the application, and integrating more capacitance on the silicon die [21].

1.3.3 Fast Transient Burst (FTB)

Fast transient burst (FTB) or Electrical fast transient (EFT) belongs to the EM susceptibility test and was introduced with the IEC 61000-4-4 standard [22]. The object of this standard is to establish a common reference in order to evaluate the immunity of an electronic equipment when subjected to electrical fast transient events on supply and signal ports. Fast transient bursts typically occur in presence of high inductive electro-mechanical components such as relay or electric motors. Indeed, every time a heavy inductive or capacitive load is switched on, a large

amount of energy is transferred from the power supply to the device. During the transfer, part of the energy is lost due to coupling mechanisms and it is injected as perturbation in other parts of the circuit. A typical example is given in Figure 1.18:

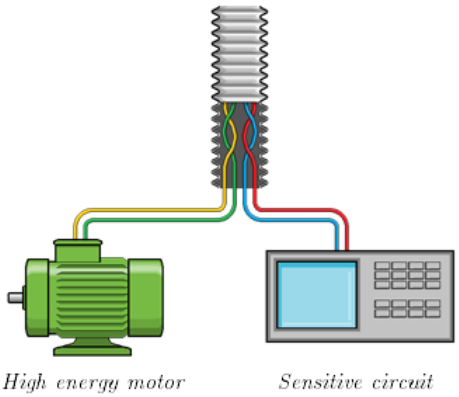


Figure 1.18: Electrical fast transient noise coupling between circuits

A sensitive electronic circuit is plugged in vicinity of a high current motor. When the motor turns on, several fast high current peaks occur in the supply distribution. These current peaks are converted into voltages due the parasites elements of the transmission line and eventually they are coupled to the power supply network of the sensitive low-power circuit. In this context, if the sensitive device is not protected, the perturbation may compromise its functionality. As mentioned in previous section, the resulting stress may be in common mode or differential mode depending whether the perturbation is coupled on both the supply conductors (V_{dd} and V_{ss}) or just on one of them. This thesis work focuses on the common mode stress but the same approach is valid for differential FTB stress.

Test description

FTB test for microcontrollers is inspired from the IEC 61000-4-4 but it is adapted to integrated circuit testing. Figure 1.19 shows the typical hardware setup.

The device under test (DUT), in this case a microcontroller, is welded on a Printed Circuit Board (PCB) whose layout is derived from the IEC 61967-2 stan-

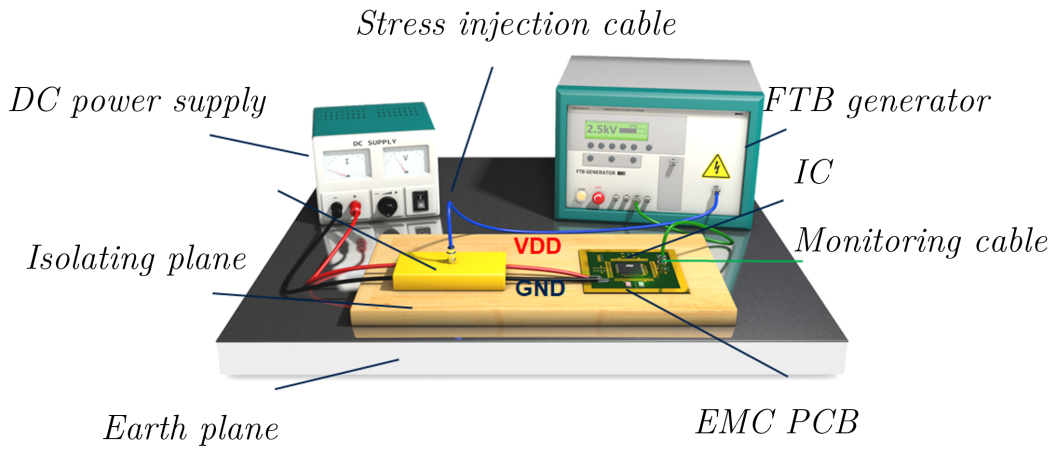


Figure 1.19: FTB bench in STMicroelectronics (adapted from [23])

dard. The PCB is a dual layer board which embeds a minimum set of components to have the microcontroller working properly. The PCB is powered by a DC power supply at the nominal operating voltage, typically 3.3V. A FTB generator, here a Schaffner NSG2025, is used to generate the stress pulses which are coupled to the DUT through a capacitive coupler (yellow in Figure 1.19). The capacitive coupler is designed to couple the stress to the DUT main supply network. Series inductance are added between the coupler and the DC power supply in order to avoid the stress to propagate to the DC generator. A simple electrical model of the FTB bench is given in Figure 1.20:

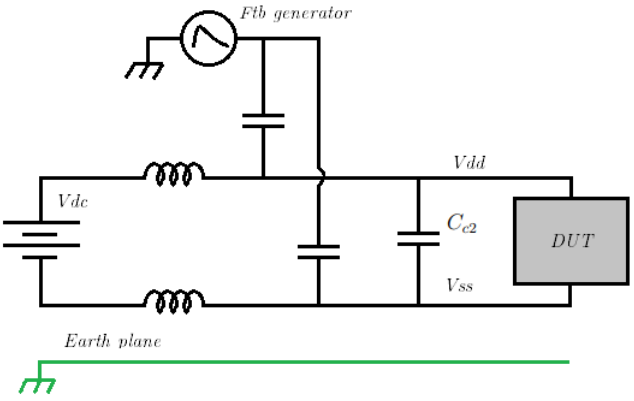


Figure 1.20: FTB bench electrical scheme

Thanks to this setup, a common mode perturbation is injected into the PCB and thus into the DUT. Capacitor C_{c2} is added to force a common mode only perturbation on the supply by reducing the differential noise. During the test, the microcontroller is executing a specific EMC code whose objectives are:

- Activate the most sensitive part of the circuit like the internal or external oscillator and executing high priority task such as memory access.
- Provide some error outputs if it detects any malfunctions.

In STMicroelectronics, the FTB evaluation is standardised through a specific test protocol which is described in Figure 1.21:

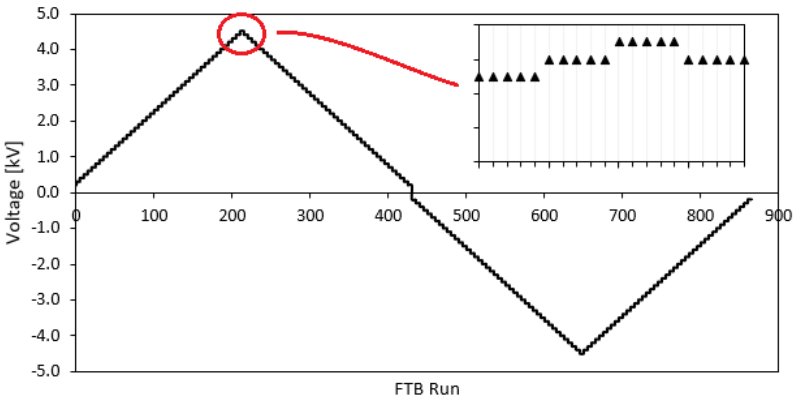


Figure 1.21: FTB test routine

The FTB generator is controlled through a LabView interface which guarantees the correct execution of the test routine. Initially, the FTB generator is set to the minimum voltage, 200V, and then the voltage is increased by step of 100V until it reaches the maximum value 4500V. Once the DUT is tested for positive voltage value the same procedure applies starting from -200V to -4500V. For each voltage step, five test runs are performed. If the results of five consecutive runs are negative, then the immunity voltage threshold is found and the test stops. Each test run lasts 12s where several pulses are sent to the DUT. The characteristics of the test run are depicted in Figure 1.22.

The pulse frequency is 5 kHz, so each pulse is 200 μs apart. 75 pulses are grouped together into bursts which are sent every 300 ms. The pulse shape produced by the FTB generator into 50 Ω load is shown in Figure 1.23.

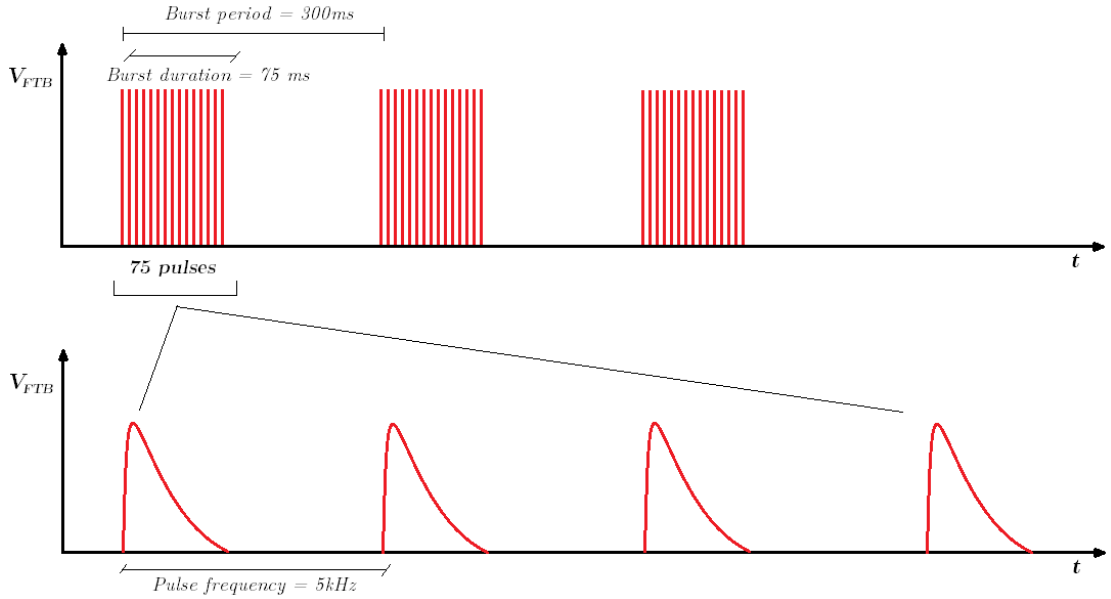


Figure 1.22: FTB burst characteristics

The pulse shape equation is:

$$V_{FTB}(t) = A\left[\frac{0.92}{k_{FTB}}\frac{\left(\frac{t}{\tau_r}\right)^{1.8}}{\left(1+\frac{t}{\tau_r}\right)^{1.8}}e^{-\frac{t}{\tau_w}}\right] \tag{1.12}$$

where

A	Pulse peak amplitude. From 200V to 4700V
k_{FTB}	$e^{-\frac{\tau_r}{\tau_w}\left(1.8\frac{\tau_w}{\tau_r}\right)^{0.55}}$
τ_w	$50 \pm 10ns$
τ_r	$5 \pm 1.5ns$

Table 1.3: Pulse parameters

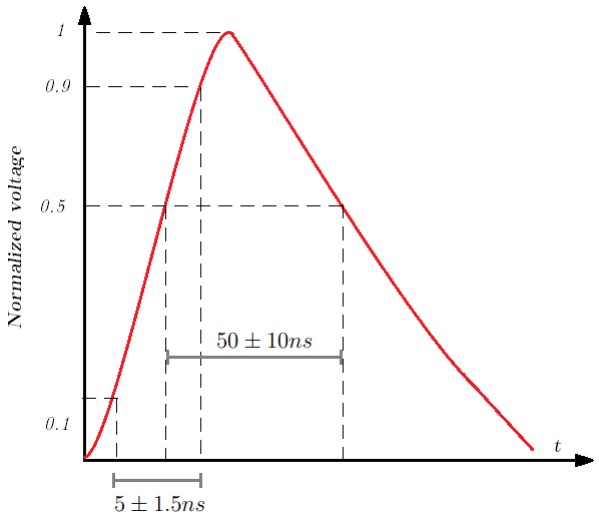


Figure 1.23: FTB pulse shape

Table 1.4 gives the values for low, normal, and high immunity threshold definition.

Voltage Threshold	**Comment**
< 2500	Very high risk. Very poor immunity behaviour. Design change mandatory.
$2500 < V < 3200$	High risk. Poor immunity behaviour. Design change mandatory.
$3200 < V < 3500$	Moderate risk. Standard immunity.
$3500 < V < 4500$	Minimal risk, High immunity.
> 4500	Very strong immunity.

Table 1.4: STMicroelectronics FTB threshold definition

Failure mechanism

If a system failure is detected during the execution of the test routine, the microcontroller rises internal flags corresponding to the failure mechanism and reset itself. After the FTB test routine, these flags are read by the LabView interface automatically. There are three main types of error flags which can occur:

- Hard fault which groups all the faults that are not related to a specific internal flag. For example, hard fault flag may be raised if the CPU tries

to access a non allocated part of the memory or if the memory address is wrong;

- Brownout Reset or Power-On reset (POR) which is raised whether the power supply drops down to a limit value defined by the power management unit;

- Watchdog timer which is raised by an internal CPU timer when the device is stuck in an undetermined state

Although flags give an hint on the potential cause of system failure they can not be used to determine precisely which part of the circuit failed. Indeed, a microcontroller is a very complex system with several billions of devices and interconnections each of which may be responsible of the failure.

Immunity solutions and thesis objective

As mentioned in the introduction of this section, FTB test has been introduced to evaluate the robustness of an electronic or electric equipment. Today, most of the research works focuses on system-level solutions like common mode choke filters or grounding technique [24] [25] [26] [27]. Although these solutions are effective, their cost in term of money and PCB area are not to be underestimated. In this context, this research work tries to explore new solutions to be implemented at silicon level, thus in the microcontroller. The objective of this work is to give some solutions to micro-controller manufacturers in order to improve the FTB immunity while keeping the cost as low as possible. Indeed, with the continuous scaling down of transistors size along with the need of more and more robust and secure devices the EMC problems become increasingly important. STMicroelectronics has been one of the first semiconductor company to show interest in FTB immunity in integrated circuits. Most of the knowledge about FTB in a microcontroller has been introduced in the PhD work "Etude et modélisation des perturbations produites au sein des microcontrôleurs STM32 soumis à des stress en impulsion" thanks to the collaboration between STMicrolectronics and Polytech'Lab [23]. The present work deepens some concepts trying to give a simulation and measurement method to evaluate FTB immunity. As Yann Bacher's work has been the starting

point of this thesis, the next section presents some of the main concepts and results of his work.

1.4 FTB concepts

In this section, some of the concepts related to FTB propagation in a micro-controller based system are introduced. In particular, the theory of the resonance frequencies of the power distribution network being the key to understand FTB immunity is presented. This section ends with a brief explanation of the existing resonance measurement setup in STMicroelectronics and its application on two test cases.

1.4.1 Common mode to differential mode conversion

Bursts coming from the FTB generator are injected to the DUT main supply network as a common mode noise as explained in the previous subsection 1. This implies that the generated pulses are present both on the V_{dd} and V_{ss} of the power distribution network (PDN). The reference of theses pulses is the metallic chassis of the bench which is tied up with the Earth of the electric installation. Figure 1.24 shows pulses propagation path toward the DUT.

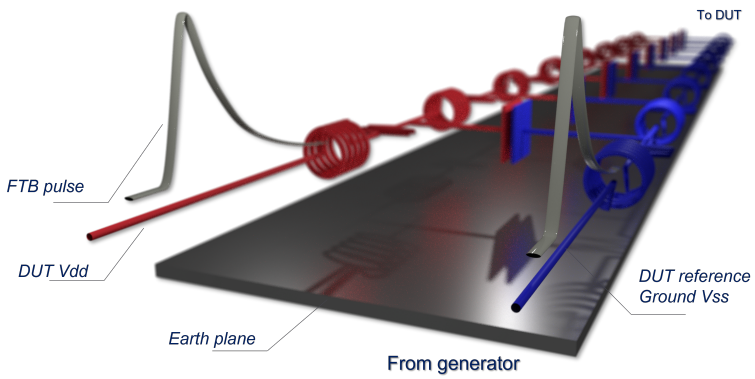


Figure 1.24: FTB pulse propagation from generator to DUT

The supply voltage at DUT is given by equation 1.13:

$$V_{supply} = \left[{V_{dd}}^{DC} + A_1 {v_{dd}}^{ftb}(t + \Delta t_1)\right] - \left[{V_{ss}}^{DC} + A_2 {v_{ss}}^{ftb}(t + \Delta t_2)\right] \quad (1.13)$$

Theoretically, if the pulses have the same amplitude ($A_1 = A_2$) and the same propagation speed ($\Delta t_1 = \Delta t_2$), they will arrive at the same time to the DUT. If that occurs, the DUT is not able to sense any difference on its power supply as the differential voltage would be kept constant and equal to the DC power supply. If the differential voltage on the supply remains equal to the DC voltage then the DUT should operate as if no stress was applied and so any protection against FTB would be useless. However, this is not the case as laboratory measurements prove that the DUT is stressed by FTB pulses which could lead to critical fail in most of the applications. A possible explanation is the common-mode to differential-mode conversion already presented previously in this chapter. Indeed, even assuming that the two pulses are injected at the same time with the same amplitude on both conductors, a slight physical asymmetry along the propagation path is sufficient to convert the common mode stress to a differential power supply noise. Asymmetry between V_{dd} and V_{ss} may be caused by many factors such as length or material difference. To show the impact of a small asymmetry on the common to differential mode conversion consider the circuit in Figure 1.25:

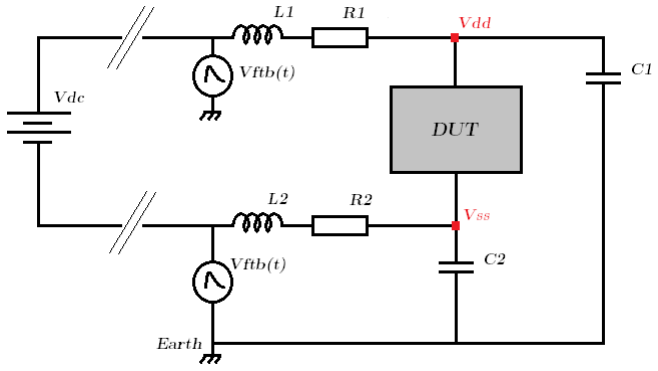


Figure 1.25: RLC circuit example to show common to differential mode conversion

V_{dd} rail is modeled with R_1,L_1, and C_1. V_{ss} rail is modeled with R_2,L_2, and C_2. The same stress is applied on V_{dd} and V_{ss} lines, the power supply close to the DUT is $V_{supply}(t) = V_{dd}(t) - V_{ss}(t)$. If $R_1 = R_2$, $L_1 = L_2$, and $C_1 = C_2$ then the

differential voltage $V_{supply}(t)$ is equal to V_{DC}. Now consider values from Table 1.5:

RLC values		
R[Ω]	L[nH]	C[nF]
$R_1 = R_2 = 0.1$	$L_1 = 1.05$, $L_2 = 1.00$	$C_1 = C_2 = 2$

Table 1.5: RLC values for sample circuit

In this case, a difference of around 5% of the value of the inductance is sufficient to create a differential signal on the supply. In particular, assuming $v_{ftb}(t)$ is a step signal from 0V to 3.3V the resulting V_{supply} is a sinusoidal signal whose amplitude decays exponentially as shown in Figure 1.26.

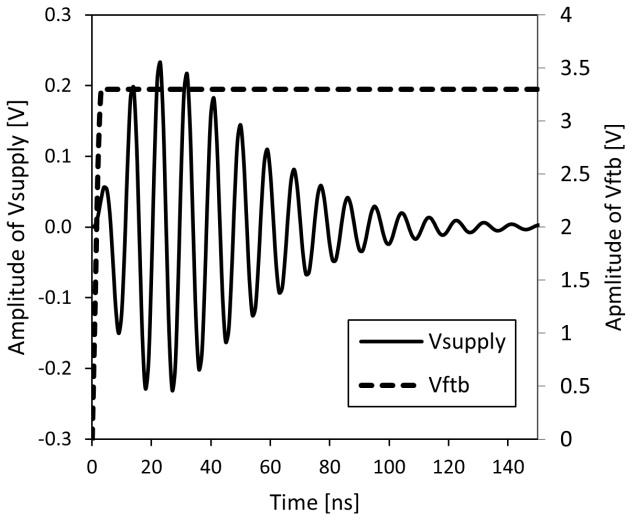


Figure 1.26: Differential signal on V_{supply}

This simple example shows how important is the power distribution network and its parasitic elements in the FTB stress propagation. Nowadays, total symmetry in the PDN is unrealistic even in the simplest circuit either for design constraints or manufacturing capability. In this context, studying the PDN electrical characteristics may be a key element to understand FTB immunity.

1.4.2 Resonance analysis

The most efficient way to study PDN electrical characteristics is in frequency domain. Indeed, the circuit in figure 1.25 could be replaced by its transfer function $H(f)$ which is the Laplace transform of its impulse response in time domain as represented in figure 1.27.

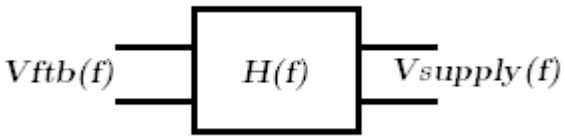


Figure 1.27: Sample circuit in frequency domain

The output signal is easily obtained by multiplying the input signal $V_{ftb}(f)$ by $H(f)$. The frequency spectrum of the FTB pulse can be calculated applying Fourier transform to the pulse equation 1.12. A simplified formula is given in:

$$V_{ftb}(f) = \frac{A\,(\tau_w - \tau_r)}{\sqrt{[1 + 4\pi f^2 \tau_w^2] + [1 + 4\pi f^2 \tau_r^2]}} \tag{1.14}$$

Figure 1.28 shows the simulated and measured frequency spectrum of the FTB pulse:

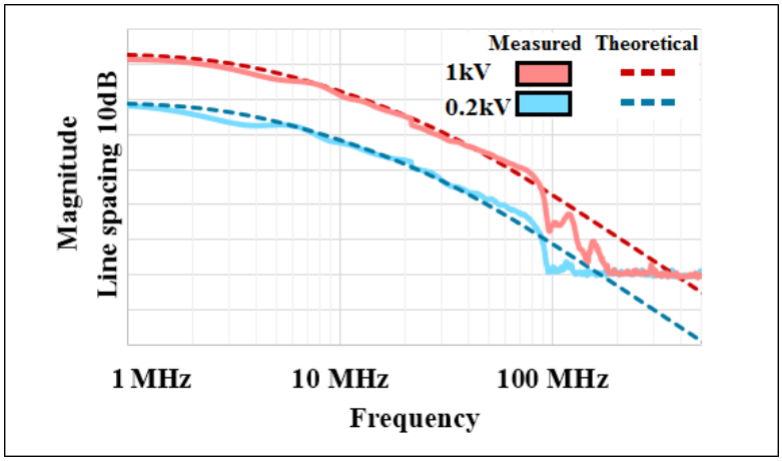


Figure 1.28: Simulated and measured frequency spectrum of $v_{ftb}(t)$

$V_{supply}(f)$ is calculated as $V_{dd}(f) - V_{ss}(f)$ where:

$$V_{dd}(f) = \frac{v_{ftb}(f)/(jwC_1)}{R_1 + jwL_1 + 1/(jwC_1)} \text{ and } V_{ss}(f) = \frac{v_{ftb}(f)/(jwC_2)}{R_2 + jwL_2 + 1/(jwC_2)} \quad (1.15)$$

so,

$$H(f) = \frac{1/(jwC_1)}{R_1 + jwL_1 + 1/(jwC_1)} - \frac{1/(jwC_2)}{R_2 + jwL_2 + 1/(jwC_2)} \quad (1.16)$$

Both transfer functions $V_{dd}(f)$ and $V_{ss}(f)$ show resonance peaks whose frequencies and amplitudes are defined by Equation 1.17 and Equation 1.18 :

$$A_1 = \frac{1}{R_1}\sqrt{\frac{L_1}{C_1}} \qquad \text{and} \qquad A_2 = \frac{1}{R_2}\sqrt{\frac{L_2}{C_2}} \quad (1.17)$$

$$w_{0_1} = \frac{1}{\sqrt{L_1 C_1}} \qquad \text{and} \qquad w_{0_2} = \frac{1}{\sqrt{L_2 C_2}} \quad (1.18)$$

Values from Table 1.5 are used in equations 1.17 and 1.18 to obtain the frequency spectrum depicted in Figure 1.29:

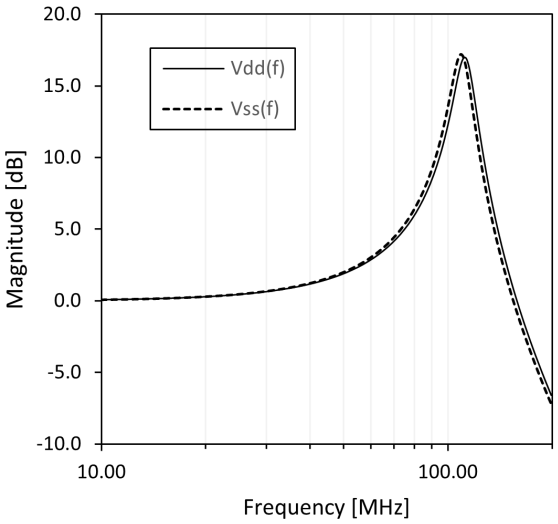


Figure 1.29: $V_{dd}(f)$ and $V_{ss}(f)$ frequency spectrum

$H(f)$ is plotted in Figure 1.30:

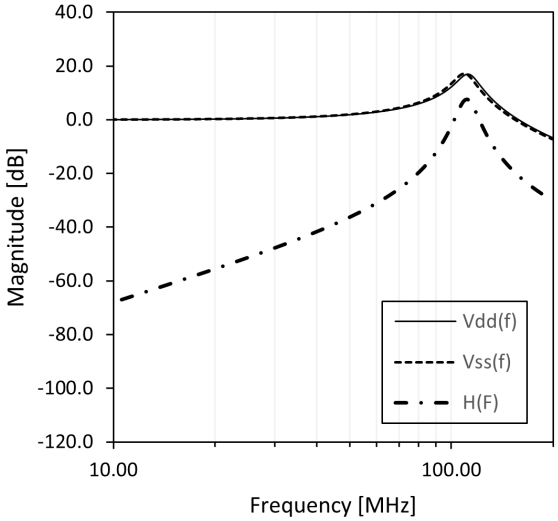


Figure 1.30: $H(f)$ frequency spectrum

Then the output is simply given by Equation 1.19:

$$V_{supply}(f) = H(f)V_{ftb}(f) \tag{1.19}$$

In the example (cf. Figure 1.25) v_{ftb} is considered as a step function. So the output $V_{supply}(f)$ could be approximated to the inverse Fourier transform of $H(f)$:

$$V_{supply}(t) \approx h(t) = \mathcal{F}^{-1}(H(f)) \tag{1.20}$$

In conclusion, Figure 1.30 and Figure 1.26 are the same representation of the common mode to differential mode conversion due to asymmetry of the PDN in time and frequency domain. Modifying the frequency behaviour of the PDN will change the common to differential mode conversion. If this is correlated to FTB propagation, then the FTB immunity could be controlled by mastering the resonances of the PDN. Circuit in Figure 1.25 is used to demonstrate that. A shunt capacitor C_s is added between $V_{dd}(f)$ and $V_{ss}(f)$ to modify the PDN frequency spectrum as shown in Figure 1.31.

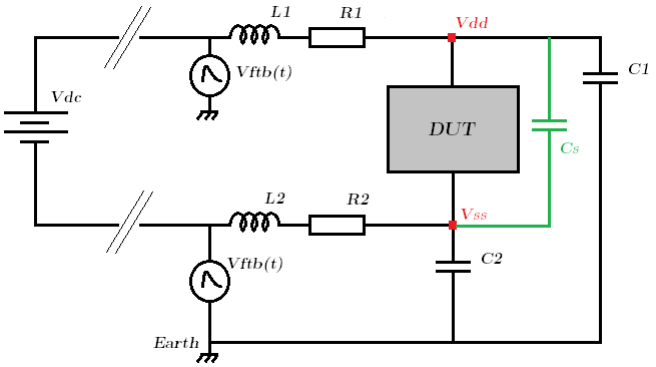


Figure 1.31: Modified RLC circuit

The new transfer function $H_1(f)$ is compared to $H(f)$ in Figure 1.32.

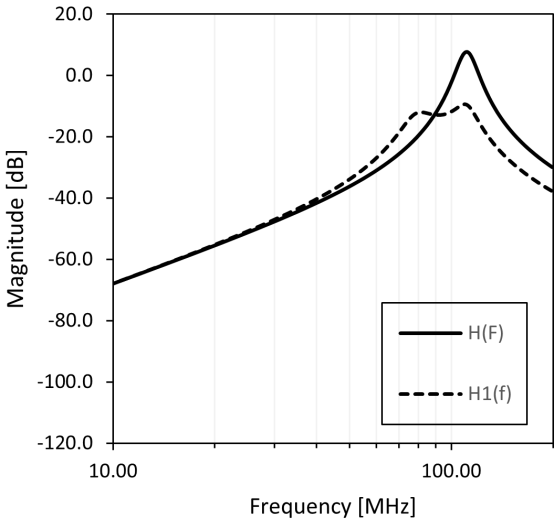


Figure 1.32: $H_1(f)$ versus $H(f)$

As it can be seen, adding C_s has a direct impact on the frequency behaviour of the PDN. In this, case the spectrum is shifted toward lower frequencies and the amplitude is lowered. In time domain V_{supply_1} is compared to V_{supply} in Figure 1.33.

Through this simple example, the common to differential mode conversion has been introduced and the PDN spectrum has been identified to be one of the main responsible. Furthermore, modifying the PDN spectrum is an interesting way to

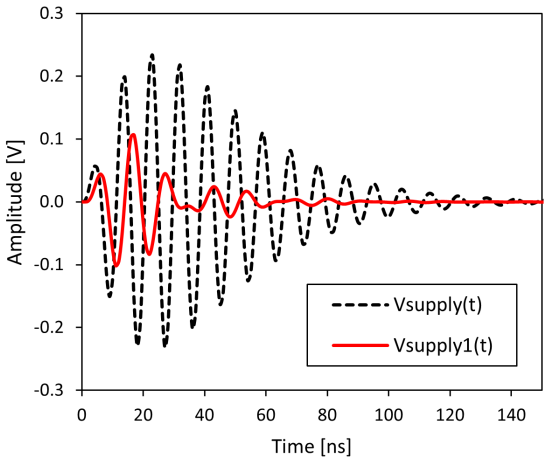


Figure 1.33: V_{supply_1} versus V_{supply}

change the propagation of the differential stress and the resonances have been found to be the key element for the attenuation and amplification of the stress.

Nevertheless many important questions are still open and this is work tries to give an answer to all:

a) Is there a correlation between PDN resonance frequencies and the FTB immunity of such a complex integrated circuit (IC) as the microcontroller?
b) How could the PDN resonances of a microcontroller based system be measured?
c) Can the resonances of the system be predicted to be able to anticipate FTB immunity during design phase?
d) How can the resonances be modified to improve immunity to be aligned with low cost STM32 development strategy?

Many works and papers have tried to answer some of the questions but still no clear evidence is given [28]–[30]. In particular, many resonances measurement methods have been presented to evaluate the PDN spectrum of a microcontroller-based system such as:

- Global resonances (GR) method
- On-die measurements
- Near field measurement method

These methods have been introduced and deeply explained in Yann Bacher thesis work "Etude et modélisation des perturbations produites au sein des microcontrôleurs STM32 soumis à des stress en impulsion".

1.5 Conclusion

This chapter introduced the context and the objectives of this thesis work. Micro controller are considered the device under test all along the dissertation. Electromagnetic compatibility was briefly introduced and all the different EMC test performed to micro-controller in STMicroelectronics were explained. This work focuses on the Fast Transient Burst test which was introduced and explained in section 1.3. The shape and the propagation mechanism of FTB were detailed in section 1.4. Some of the bibliographical results related to FTB were shown and explained through simple examples. The analysis of the resonances of the power distribution network are found to be an interesting method to understand the common to differential mode conversion which is thought to be correlated to FTB immunity. Finally, four main questions are presented:

- 1) Are resonances correlated to FTB immunity of microcontrollers?
- 2) How can we measure the resonances of the PDN?
- 3) How can we predict the resonances during design phase?
- 4) how do we change the resonances to improve microcontroller immunity to FTB?

Next chapter gives the fundamental instruments to answer some of those questions. Indeed, the first part of the Chapter 2 is dedicated to the modelling methodology. This approach is used to create an electrical model of the DUT consisting in three elements: the PCB, the package, and the integrated circuit. In the second part of the chapter, some details about the resonance measurements are given and, in particular, a novel measurement bench is presented.

Chapter 2

Modelling and measurement flow for resonance analysis

Contents

This chapter aims to give all the details about PDN modelling and measurement in a microcontroller-based system. General and specific guidelines are described when it comes to model the PCB, the package and the die. Some interesting measurement methods are presented in the second part of the chapter. The description of a novel measurement bench along with a brief conclusion ends the chapter. The modelling and measurement technique described in this chapter will be applied in chapter 3 to some real DUT configurations to find whether PDN resonance frequencies are related to FTB immunity.

2.1 Modelling the DUT

In chapter 1, the importance of PDN characteristics for FTB immunity was hypothesised. In particular, PDN is considered the principal element contributing to the common to differential mode conversion due to asymmetric supply distribution between V_{dd} and V_{ss}. This asymmetry causes a stress propagation time delay difference which leads to a noise generation on top of the supply. At the end of chapter 1, frequency-domain resonance analysis was introduced as the most convenient tool to study PDN characteristics. That being said, creating an electrical model of the PDN of the DUT is fundamental to:

- simulate the PDN behaviour in frequency domain to find and predict the resonances of the DUT
- study and find the principal contributors to a resonance phenomenon
- see how different DUT configurations affect global resonances.

Device Under Test definition

Before going into details of PDN modelling, it is important to define a typical DUT. Figure 2.1 shows the typical DUT configuration considered in this work.

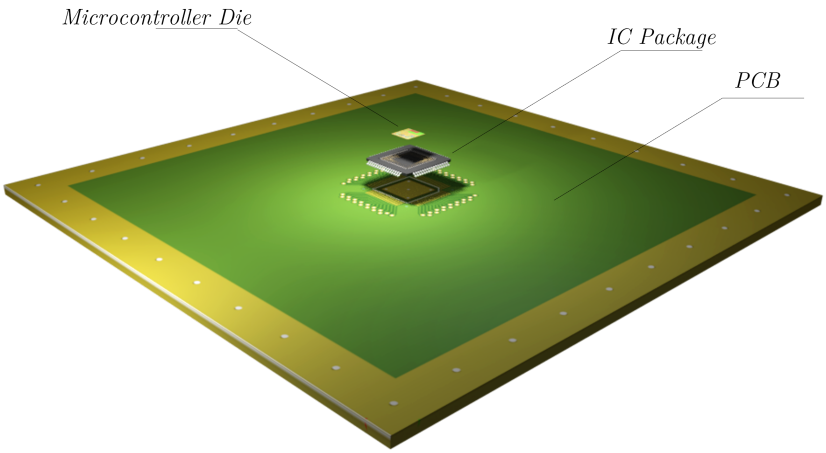


Figure 2.1: Device Under Test

Three elements build the DUT: the PCB, the package, and the silicon die. In the next paragraph, the modelling approach for each element is described. The objective is to create a final electrical model as shown in Figure 2.2 which will be used to study the resonances of the entire system.

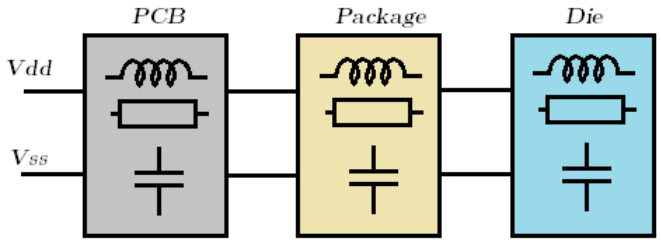


Figure 2.2: Total electrical model of the DUT

2.1.1 PCB Modelling

The PCB is the first element which is encountered by the FTB stress in its way toward the IC die. The PCB is thus responsible for the first attenuation-amplification mechanism of the stress and its modelling is crucial. The PCB is designed to comply with standard electromagnetic requirements and to provide easy access to functional test points, from that its name EMC board. Its design is far from being ideal and it is not representative of a final customer PCB. Nevertheless, using the same not-optimal PCB design approach allows direct comparison between different products and helps highlighting the weaknesses of the system. Figure 2.3 shows a typical EMC board.

The design and layout of the EMC board used for FTB immunity is inspired from the 61967-1 IEC standard for radiated emission. It consists of a two layers board with the following characteristics:

- Layer 1 is entirely used as a ground plane. PCB is designed to have the IC welded alone on the this side of the board
- Layer 2 is used as a power and signal plane. All the components other than the DUT are placed on this side.

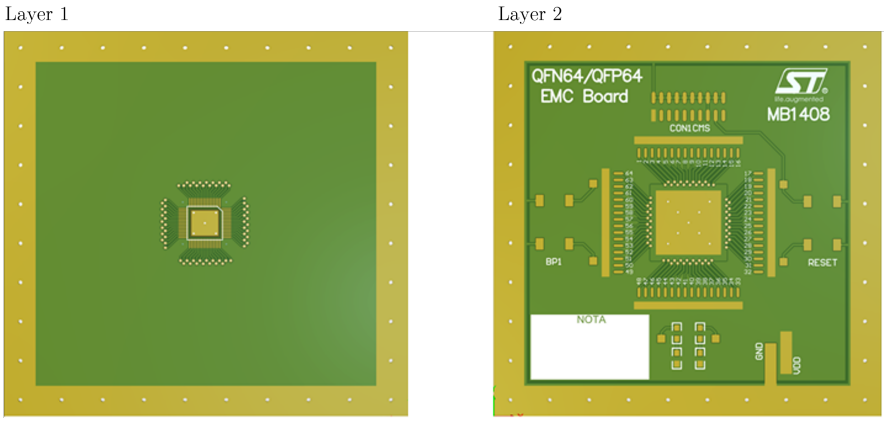


Figure 2.3: Generic EMC board as defined in 61967-1 IEC

- The area underneath the IC is connected to the ground plane through multiple via connection 10 mm far apart and with a hole diameter larger than 0.2mm (see Figure 2.4)

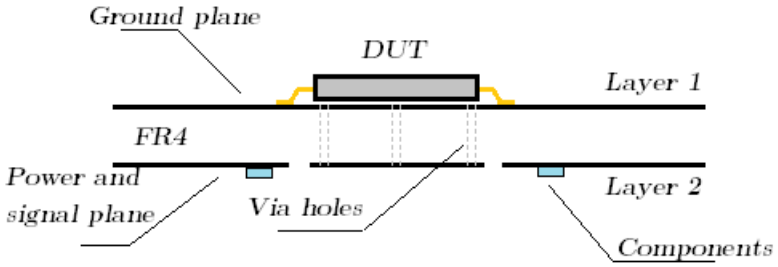


Figure 2.4: Cross-section of standard EMC board

Other manufacturing characteristics are summarized in Table 2.1:

Thickness	1.6 mm
Insulator	FR-4
Track-to-track clearance	0.2mm
Track width	0.3mm
Copper thickness	35μm
PCB dimensions	100mm x 100mm

Table 2.1: EMC board manufacturing characteristics

There are two different ways to model the PCB, the first is by-hand using classical equations, the second using 3D high-accuracy software. Due to low complexity, the PCB can be easily modeled by-hand. The most important parameters to be taken into account are:

- PCB intrinsic capacitance
- Track and vias partial inductance
- Track mutual inductance
- Track high frequency impedance
- Decoupling capacitors impedance.

In the following paragraph a brief description of the electrostatic and electromagnetic properties of the interconnections to be considered as well as the equations used to build the model are presented.

PCB intrinsic capacitance and decoupling capacitor characteristics

PCB intrinsic capacitance is derived from the coupling between V_{dd} and V_{ss} plane as depicted in Figure 2.5

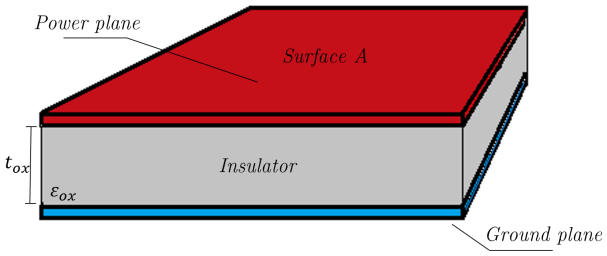


Figure 2.5: Power planes capacitance

The overall plane capacitance is defined as:

$$C_{PCB} = A\frac{\epsilon_{ox}}{t_{ox}} \tag{2.1}$$

where A is the area of the portion of the PCB where V_{dd} and V_{ss} are face to face, ϵ_{ox} is the dielectric constant of FR-4 which is about 4 times vacuum electric permittivity (ϵ_0) and t_{ox} is approximately the thickness of the PCB, 1.6 mm. The

estimated area A for the proposed board in Figure 2.3 is 60cm^2 and then the calculated plane capacitance is:

$$C_{PCB} = 6000\frac{4 \cdot 8.854 \cdot 10^{-15}}{1.6 \cdot 10^{-3}} \approx 135pF \tag{2.2}$$

This value does not take into account fringe capacitance. In order to find the value of the capacitance empirically, a simple set up is proposed in Figure 2.6 *(a)*.

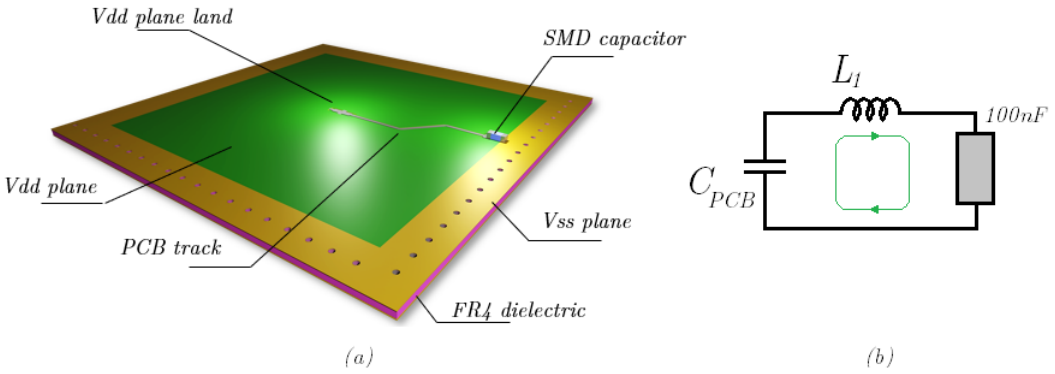


Figure 2.6: Intrinsic capacitance evaluation setup

A surface-mount device (or SMD) 100nF capacitor is soldered on the top layer between V_{dd} and V_{ss} power planes. The connection on the reference ground is done by welding the component directly on the V_{ss} plane. A track of some centimeters is used to connect the capacitor to the V_{dd} plane. The equivalent electrical schematic is given in Figure 2.6 *(b)*. The resonance is then measured using the methodology explained later in this chapter and the result is given in Figure 2.7.

As it can be observed in Figure 2.7 a resonance appears at about 100MHz. The origin of this resonance are not to be found in the oscillation between the track inductance L_1 and the 100nF capacitor, but instead the internal PCB capacitance is the oscillating element. Indeed, a typical 100nF SMD capacitor characteristic is shown in Figure 2.8.

The overall impedance reaches a minimum when the reactance of the capacitor equals that of the inductance. This occurs at a frequency $f = \frac{1}{2\pi\sqrt{LC}} \approx 35MHz$.

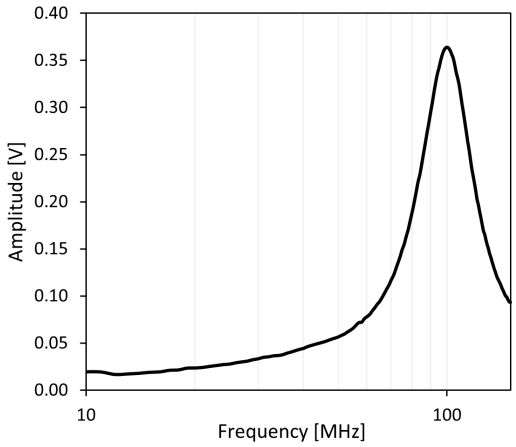


Figure 2.7: PCB connected to 100nF capacitor resonance measurement

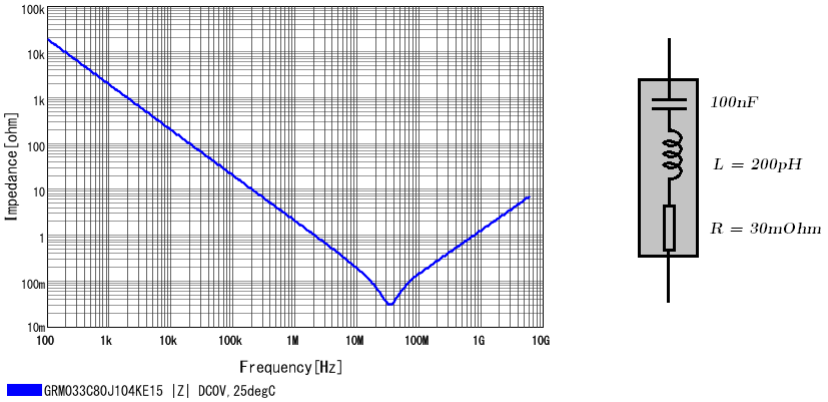


Figure 2.8: 1005 SMD 100nF multiceramic capacitor from Murata catalog [31]

Above 35MHz the capacitor is no longer considered a capacitance but as an inductance whose value is about 200 pH. In conclusion, the impedance of the capacitor is negligible compared to the other entities in the circuit of Figure 2.6 and it can be considered a short to the ground closing the loop. The circuit then is simplified as depicted in Figure 2.9.

The peak observed at 100MHz is then caused by the resonance phenomenon between the intrinsic PCB capacitance and the track leading to the SMD capacitor. To extract correctly the value of the capacitance, small SMD capacitors are added in parallel to the PCB power planes. The characteristic of these capacitors is

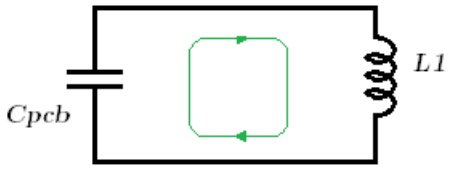


Figure 2.9: PCB electrical model simplified

chosen to have a zero-reactance frequency far above 100MHz. Figure 2.10 shows the results of the resonance measurement for different values of added capacitance C_{add}.

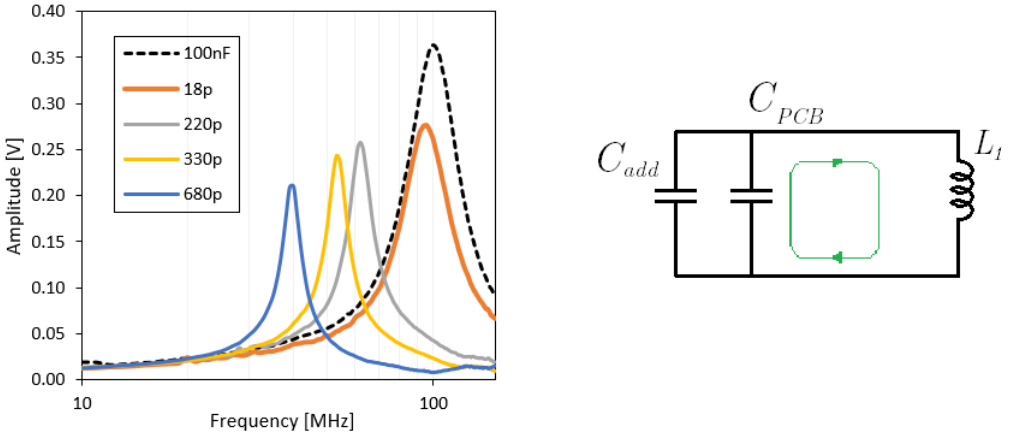


Figure 2.10: C_{PCB} extraction using C_{add}

Resonance frequencies are calculated using Equation 2.3:

$$f_{res} = \frac{1}{2\pi\sqrt{L_1(C_{PCB} + C_{add})}} \tag{2.3}$$

C_{PCB} can be extracted by taking the ratio between the resonance frequencies as follows:

$$\frac{{f_{res}}^{C_{add1}}}{{f_{res}}^{C_{add2}}} = \sqrt{\frac{C_{PCB} + C_{add2}}{C_{PCB} + C_{add1}}} \tag{2.4}$$

The results are given in Figure 2.11. The average extracted capacitance is about 130 pF which is aligned with previous theoretical calculation.

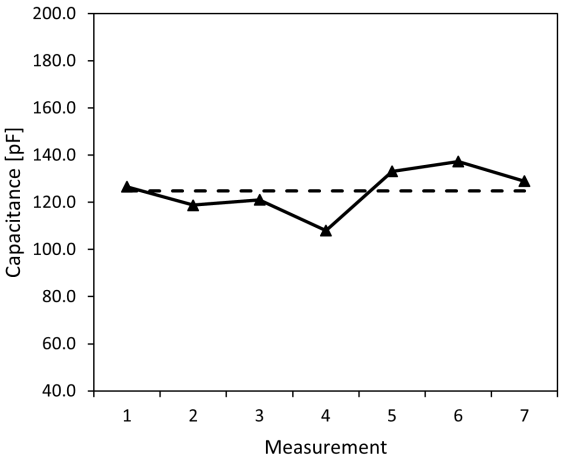


Figure 2.11: C_{PCB} extraction results

Track partial and mutual inductance

Several papers were dedicated to inductance definition and calculation for electronic circuits [32],[33],[34],[35]. Circuit inductance or auto-inductance definition comes from Ampère-Laplace equations. Indeed, every current-flowing circuit produces a magnetic field. Part of the generated flux concatenates with the circuit loop itself, it is called *induction flux* Φ. The induction flux of a circuit is proportional to the current i flowing through the circuit and to the geometry and material property of the loop whose boundary is delimited by the circuit itself (Equation 2.5).

$$\Phi = L \cdot i \tag{2.5}$$

Thus, L depends **only** on the shape of the circuit and on the magnetic property of the medium. So, inductance exists only in closed loop circuit and it's not an intrinsic property of a material, for this reason non-intentional inductance in a circuit is also called *loop inductance*. Loop inductance can be mathematically calculated if and only if the loop is known. Most of the time this is not the case as the return path is often unknown. To overcome this problem many research works focused on a way to assign an inductance value to a segment of the loop without considering the return path. This was mathematically achieved introducing the concept of *partial inductance* [36], [37]. The general definition of partial inductance

is given by Paul Clayton in his book as follows: "The self partial inductance of a segment of a current loop is the ratio of the magnetic flux between the current segment and infinity and the current of that segment" [38].

Figure 2.12 shows the typical EMC board trace defined by the IEC standard. The total self partial inductance is given by the segment on top and bottom layer

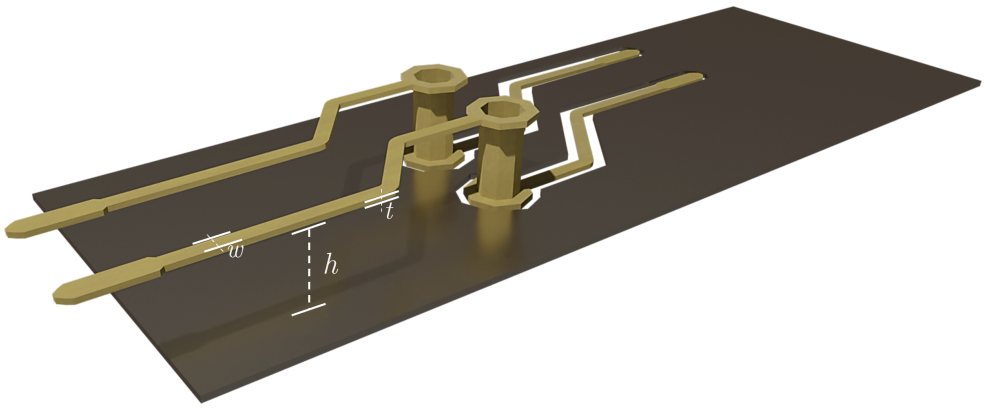


Figure 2.12: EMC PCB traces on top and bottom layer

plus the inductance of the via. Rectangular cross section microstrip over a ground plane partial inductance is given by Hoer and Love equation [39]:

$$L = \frac{\mu_0}{2\pi w^2}\left[lw^2 \ln\left(\frac{l}{w} + \sqrt{\left(\frac{l}{w}^2\right) + 1}\right) + l^2 w \ln\left(\frac{w}{l} + \sqrt{\left(\frac{w}{l}^2\right) + 1}\right) + \frac{1}{3}\left(l^3 + w^3\right) - \frac{1}{3}\left(l^2 + w^2\right)^{3/2}\right] \qquad t \to 0 \tag{2.6}$$

where l is the lenght of the wire, t is the thickness of the wire, w is the width of the wire. Figure 2.6 is valid for very low thickness compared to w. For extremely wide ($l \ll w$) or long ($l \gg w$) PCB lands Equation 2.6 can be simplified as follows:

$$\frac{L}{l} \approx \frac{\mu_0}{2\pi}\begin{cases} \ln\left(2\frac{l}{w}\right) + 0.5 + \frac{w}{3l} & l \gg w \\ \frac{l}{w}\left(\ln\left(\frac{2w}{l}\right) + 0.5 + \frac{l}{3w}\right) & l \ll w \end{cases} \tag{2.7}$$

Figure 2.13 shows the inductance per unit length value as a function of the total length for long lands.

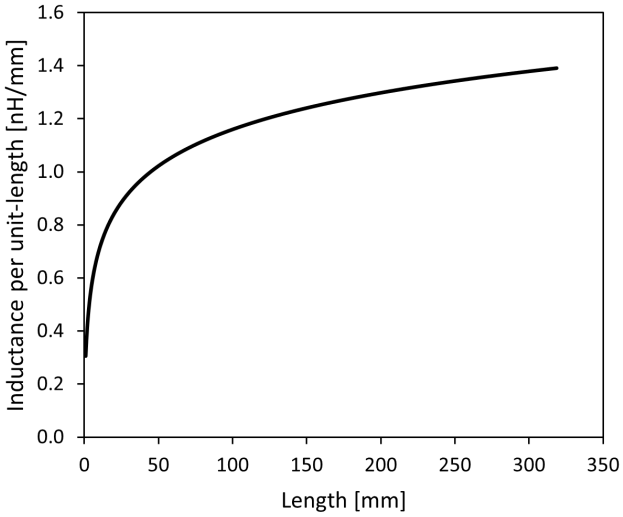


Figure 2.13: Inductance per unit length for wide PCB lands

Considering parameters from Table 2.1 and applying Equation 2.7 the partial inductance per unit-lenght is:

$$L \approx 1.2nH/mm \tag{2.8}$$

To verify the calculation a similar approach to the intrinsic PCB capacitance is done. The SMD 100nF capacitor is soldered at four different distances: 1cm, 2cm, 3cm, and 4cm. The measured resonances for each case are shown in Figure 2.14.

The measured frequency are extracted in Table 2.2:

Length	**1cm**	**2cm**	**3cm**	**4cm**
Frequency	92MHz	77MHz	68MHz	54MHz

Table 2.2: Resonance frequency value for different microstrip lengths

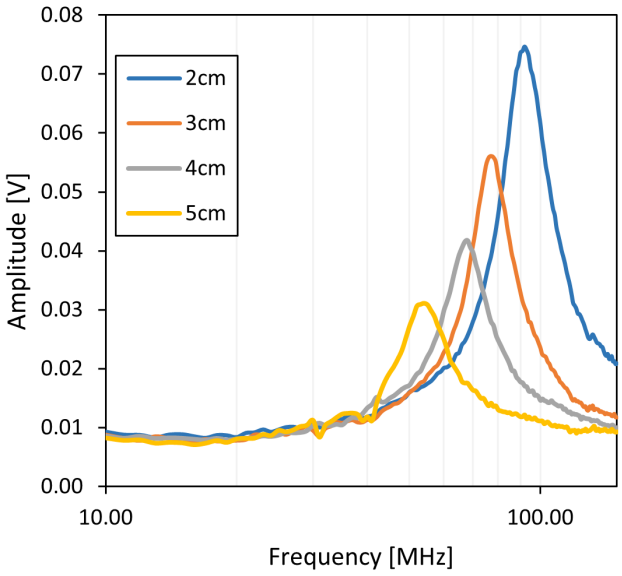


Figure 2.14: Resonance frequency for different microstrip lengths on EMC board

The inductance value can be easily obtain as follows:

$$L_i = \frac{1}{(2\pi f_i)^2 C_{PCB}} \tag{2.9}$$

Using Equation 2.9 the average inductance per unit length found is 1.1 nH/mm which is coherent with Equation 2.8.

Another important parameter related to the inductance is the *mutual inductance*. Indeed, the magnetic field flux produced by a circuit 1 through a circuit 2 is given by:

$$\Phi_{1,2} = M_{1,2} i_1 \tag{2.10}$$

$M_{1,2}$ is called mutual inductance coefficient and it depends on all the geometrical factors of the circuits as the loop shape and orientation. As for loop inductance, to build a lumped element circuit model we need the mutual inductance of a single segment. The partial mutual inductance is then defined as " the ratio of the magnetic flux (produced by the current of the first segment) that penetrates the surface between the second segment and infinity and the current of the first segment" [38]. The mathematical formula for partial mutual inductance between

two PCB lands is very complicated and it is not presented in this context. An approximated formula is given in Equation 2.11 valid for $D \ll l$, that is distance between the conductors is negligible compared to their length.

$$\frac{M_p}{l} = \frac{\mu_0}{2\pi}\left(\ln\left(\frac{2l}{D}\right) - 1\right) \tag{2.11}$$

Considering track to track clearance of 0.2mm, the partial mutual inductance is equal to 0.45nH/mm The actual mutual inductance for EMC board can also be extracted with multiple measurement presented below:

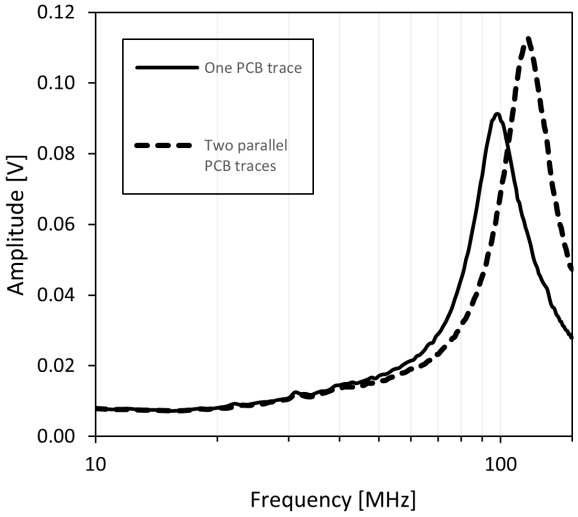


Figure 2.15: Resonance frequency for single or double microstrip

Figure 2.15 shows the resonance behaviour for two different cases: a single microstrip versus two identical parallel microstrip as Figure 2.12 depicts. The equivalent inductance of two parallel wire with the same current direction is :

$$L_{eq} = \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M} \tag{2.12}$$

which is simplified if $L_1 = L_2 = L$ to:

$$L_{eq} = \frac{L^2 - M^2}{2L - 2M} = \frac{L + M}{2} \tag{2.13}$$

The equivalent inductance can be calculated also knowing the partial inductance per unit length of one of the wire through the following equation:

$$\frac{L_{eq}}{L_1} = \left(\frac{f_1}{f_{eq}}\right)^2 \tag{2.14}$$

where f_{eq} is the resonance frequency found with two parallel microstrips (see Figure 2.15). By combining Equations 2.13 and 2.14 and taking 1.2 nH/mm (see Equation 2.8), the mutual inductance per unit length is equal to :

$$\frac{M}{l} \approx 0.4nH/mm \tag{2.15}$$

Generally, for electrical simulation, the coupling coefficient K is more convenient; it is defined as:

$$K = \frac{M}{L_1 L_2} \tag{2.16}$$

For EMC board the measured K is then equal to 0.4.

Another element to model is the via. A via is a drill on the PCB plated with some conductive material which is used to interconnect signals on different PCB layers. For high-frequency application vias shall not be neglected as they represent a real barrier to high-speed signal [40]. Figure 2.16 shows a 3D model of a typical via used for EMC board.

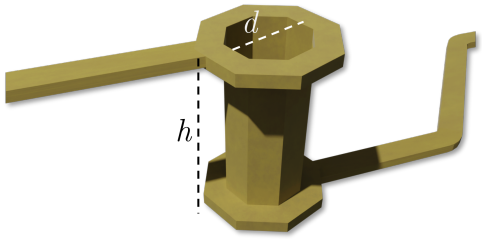


Figure 2.16: Via 3D model

The partial inductance of a via is similar to that of a round wire, that is:

$$\frac{L_{via}}{h} = \frac{\mu_0}{2\pi}\left(\ln\left(\frac{4h}{d}\right) - 1\right) \tag{2.17}$$

where d is the diameter of the hole and h is the height of the via. Given a PCB thickness of 1.6mm and hole diameter of 0.3mm, via inductance is about 0.4nH.

Track resistance

The resistance of a PCB land is given by Equation 2.18.

$$R = \rho \frac{l}{e\, w} \tag{2.18}$$

where ρ is the resistivity of the material, l is the length, w the width, and e is the thickness of the conductor. EMC PCB is designed with 35μm thick copper microstrip of 0.3mm width. Then, the overall resistance per unit length is about:

$$\frac{R}{l} = \frac{1.68 \cdot 10^{-5}}{35 \cdot 10^{-3}\, 0.3} = 1.6 m\Omega/mm \tag{2.19}$$

Since the frequency spectrum of FTB stress extends up to hundreds of MHz, some higher frequency physical behaviour such as skin effect [41] [42] shall be taken into account. Skin effect is the phenomenon for which current distributes on the surfaces of the conductor as the frequency increases. Indeed, at high frequency current is not uniformly distributed on the volume of the conductor but instead concentrated in a thin layer under the surface. As the conductive surface decreases the overall resistance increases over the frequency. The thickness of this layer is called *skin depth* δ which is defined by Equation 2.20:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{2.20}$$

For a round conductor of radius r (see Figure 2.17 (a)) the high frequency resistance taking into account skin effect is then:

$$\frac{R}{l} = \frac{\rho}{\pi \left(r^2 - (r-\delta)^2 \right)} \approx \frac{\rho}{2\pi r \delta} \tag{2.21}$$

For rectangular cross section the current is distributed in a thin layer which is proportional to the skin depth, that is $k\frac{\delta}{2}$ [43] as shown in Figure 2.17 (b).

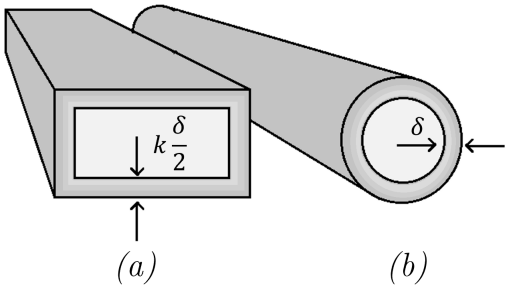


Figure 2.17: Skin effect for rectangular (a) and round (b) cross section conductors

Assuming the same layer thickness for all edges the high frequency resistance is then:

$$\frac{R}{l} \approx \frac{\rho}{k\pi\delta(w+e)} \tag{2.22}$$

where k is a mathematical constant between 1 and 2. Considering $k = 2$ for wide PCB lands, the DC and AC (100MHz and 500MHz) resistance for EMC board traces are given below:

$$\frac{R}{l} \approx \begin{cases} 1.6\ m\Omega/mm \text{ for low frequency} \\ 3.8\ m\Omega/mm \text{ at 100MHz } (\delta = 6.6\ \mu\text{m}) \\ 8.7\ m\Omega/mm \text{ at 500MHz } (\delta = 2.9\ \mu\text{m}) \end{cases} \tag{2.23}$$

The most important parameters to take into account when modelling by-hand a PCB have been discussed. Nowadays many software exist capable of extracting an electrical netlist from the layout of the board. Despite those software being far more accurate, their results are hard to be used for research and deep study as the models behind are too complex. By-hand modelling allows a real understanding of the physical phenomena and it should be used along with computing software to build every electrical model.

2.1.2 Package Modelling

IC package plays an important role in term of parasites brought to the DUT. Nowadays, microcontrollers are often sold in three main package categories: Flat

leadframe package (QFPxx), Ball-grid array (BGA) or Chip-size packages (CSP). These three packages offer different characteristic and complexity. In QFP packages, the die pads are connected to the external pins usign wire bond connection, the main disadvantage is then low pin density and high inductance connections. This package is suitable for low-speed and low-power applications. In BGA package, the pins are conductive balls which lay under the chip. This allows a better density with smaller packages. In CSP package, die pads are typically connected to routing interconnection layers in the package through bumps. This allows the best pins density for high number of IOs. CSP provide also the lowest impedance between the die and the PCB and they are mainly used for high speed devices as microprocessor.

Modelling an IC package is complex as the geometries involved are small and diverse, therefore by-hand modelling may lead to strong inaccuracy. Many 3D electromagnetic software provide solutions to correctly extract an electrical model of a given package. The software used in this work is Q3D Extractor by Ansys [44]. This tool generate a RLCG netlist by analysing the 3D model of an electromechanical structure. For this work only lead-frame packages are considered as they are the most critical packages for EMC evaluation. Figure 2.18 shows a 3D render of a QFP64 package, that is 64 IO pins in a quad flat package.

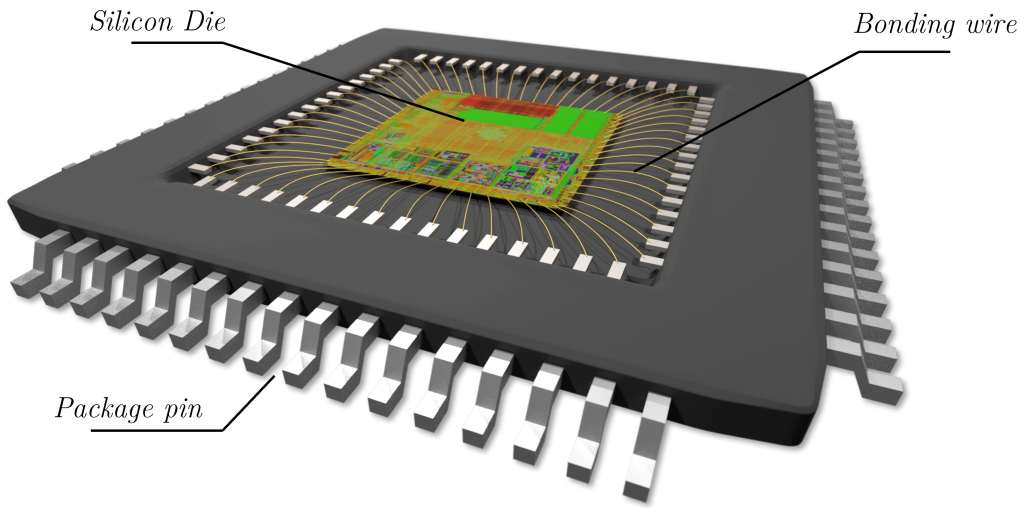


Figure 2.18: QFP64 package

A QFP package is composed of two elements: the leadframe and the bonding wire. Figure 2.19 shows in details the QFP structure. The leadframe consists of a central metallic die pad tied generally at the ground reference and several leads which carry the signals out of the package. At the end of each lead, bonding wires provide the connection between the leadframe and the integrated circuit. These bonding wire are welded on both edges and they are typically made of gold to decrease resistance.

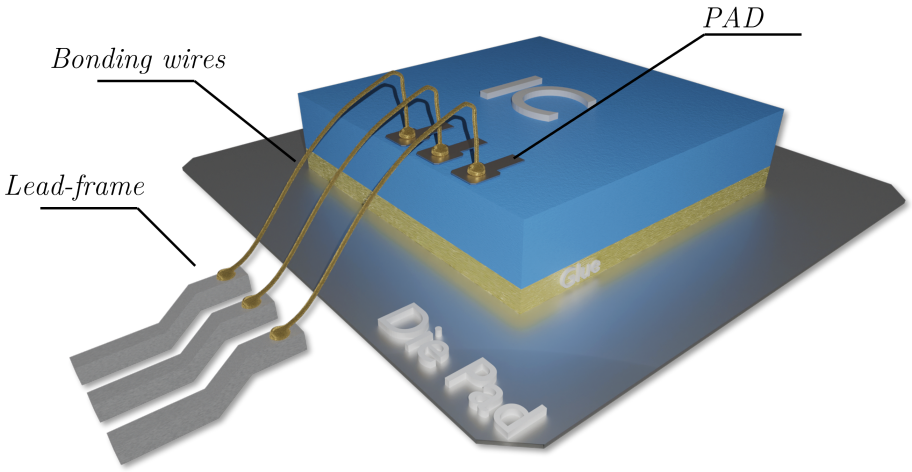


Figure 2.19: QFP64 internal structure

Leadframe and bonding wire shape and length depends on the package and on the die size. The smaller the die size compared to the package, the longer the bonding wire will be. Sometimes, for large packages for radio frequency (or RF) circuits, the die position is shifted to one side to allow shorter connection for RF intellectual properties or IP.

As it was said before, 3D electromagnetic software are generally used to extract electrical netlist of small and complex geometry. In particular, Q3D Extractor gives an RLCG netlist as output. During the extraction setup, the operating frequency has to be fixed in order to correctly extract the model. For this study, 100MHz is an acceptable value. The lumped element circuit issue from Q3D simulations is structured as Figure 2.20 shows.

For each external pin connected to a microcontroller pad, the impedance of the

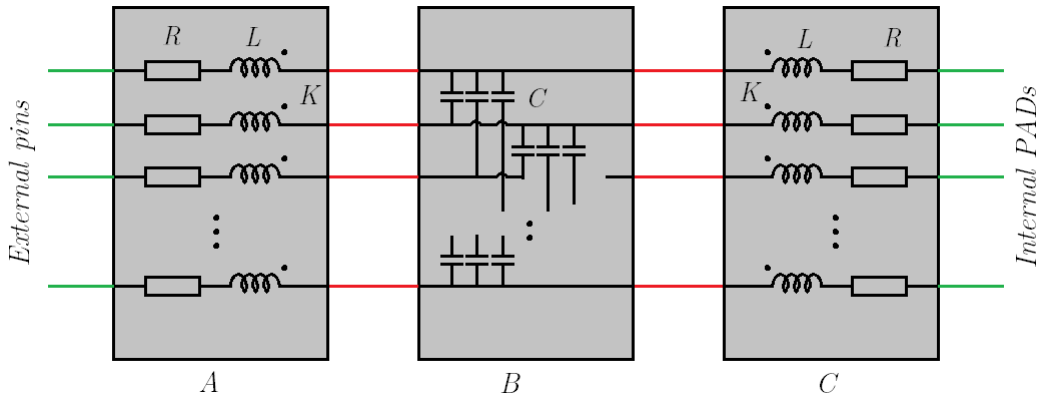


Figure 2.20: RLC electrical model generated by Q3D Extractor

path is split in two subcircuits A and C in Figure 2.20. Each of the subcircuit is constituted by half of the total resistance and half of the total inductance. Furthermore the mutual coefficient K is given for every possible pair of conductor. Subcircuit B completes the model by defining the capacitive coupling between each of the conductor. As previously mentioned, this subdivision is purely a mathematical artefact and it does not represent in any mean a physical reality. A sample simulation is run on an QFP64 standard package with 4 mm^2 die inside whose bonding diagram is shown in Figure 2.21. In red, V_{dd} and V_{ss} bonding wire are highlighted. Bonding wire length is between 2 and 3 mm depending on the pin position on the package.

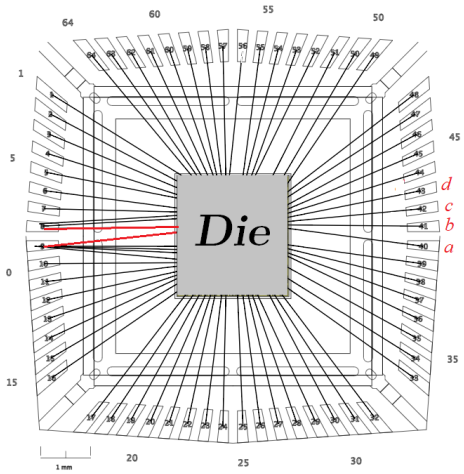


Figure 2.21: Bonding diagram of a sample QFP64 package

Average value of the parameters extracted from Q3D are given in Table 2.3.

R_{tot}	L_{tot}	C_{tot}
0.2Ω	4nH	0.1pF

Table 2.3: RLC parameters issued from Q3D simulation on QFP64 package

Another interesting parameter is the mutual coefficient K which is extracted for every pair of conductors. K depends on the distance between two bonding wires. Consider 4 side-by-side bonding wires a, b, c and d (cf. Figure 2.21). The extracted mutual coefficient K between a and b is 0.39, 0.24 between a and c, 0.16 between a and d and less than 0.1 for larger distances.

2.1.3 Die Modelling

The last element to model is the PDN of the IC, in our case a generic microcontroller. Microcontrollers are generally very complex ICs which embed up to billions of transistors and even more interconnections. Creating an electrical model of such a complex circuit is far from being an easy task and software are not able to handle the great number of devices and nets which are present inside. For this reason, some simplifications and approximations must be done. In order to properly simplify the task, we have to remind the initial hypothesis of this work and the reason why modelling the IC could be usefull. Indeed, the goal is to create an electrical model of a generic DUT made of PCB, package, and IC to find the resonances occurring on the power distribution network. The hypothesis being that the PDN and its resonances are responsible for the amplification of the FTB stress. The PDN of a microcontroller is generally subdivided in different domains:

- The main power domain which comes directly from an external source. Typically, it is a 3.3V supply.
- The internal power domain which is derived from the external one but adjusted and regulated for core devices. Typically, its value is about 1.1 V.
- The analog supply which is typically shorted with the main supply at PCB or package level but it usually benefits of a independent bonding wire. This allowing little impedance coupling and so a cleaner supply.

Figure 2.22 shows a typical PDN diagram of a microcontroller.

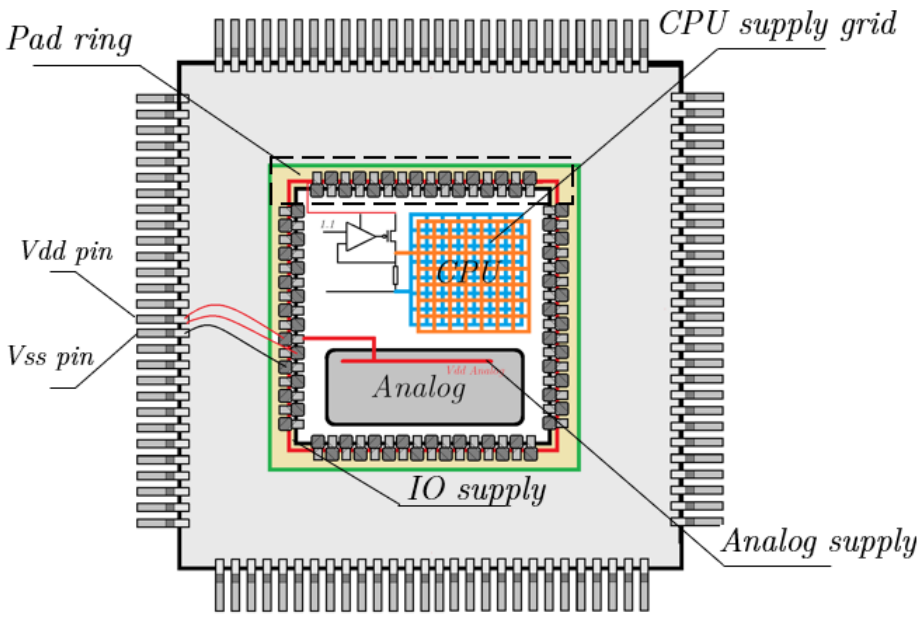


Figure 2.22: Power supply domain distribution

The main power domain provides supply to all the peripheral IPs around the chip which are called IO (Input/output). The analog supply is used by all analog IP like Digital-to-analog converter, regulator, power management units, internal oscillators and many others. The internal power domain or core supply is usually derived from the main supply with a Low-Dropout regulator or DC-DC converter. This supply is used for the CPU where low threshold voltage devices are employed. As FTB stress is applied on the external main supply of the device, only power supply directly coming from a package pin will be considered. Indeed, as a first approximation the core supply is considered isolated and well protected. Thus, only the main power supply and analog supply have to be modelled. These two power supplies share usually the same package pin but different bonding to decrease impedance coupling (see Figure 2.23).

The modelling of the main and analog PDN can be subdivided into two different tasks: the RLC estimation of the interconnections and the modelling of the active devices.

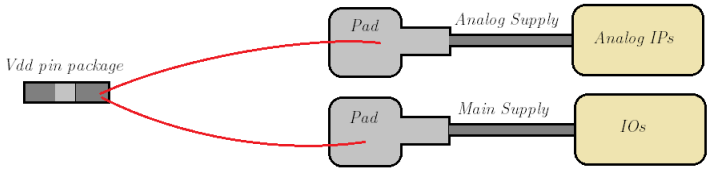


Figure 2.23: Double bonding for analog and main domain

Die interconnections modelling

The objective is to create an electrical model of the main power distribution interconnections at silicon level. As depicted in Figure 2.22, the main PDN is mainly constituted by power rails running all around the chip which bring most of the parasitic elements. These power rails are designed under the pads and provide supply to all the IO interfaces such as General-Purpose IO (or GPIO), USB interfaces etc... The power rails and the IOs form a ring which defines the boundary of the chip, this ring is also called the pad ring. IOs definition are one of the most critical element during the design phase as their size could seriously impact the overall die size. In particular, an IC is called pad-limited if the number and the area of the IOs employed in a product limit the down-scaling of the die. Otherwise, a product is called core-limited if the area of the internal circuitry imposes the die size. In the first case, the internal area of the die will be partly empty, in the second case the pad ring will present some filler cells (no active device inside) which guarantee power rails continuity. Figure 2.24 shows part of the pad ring:

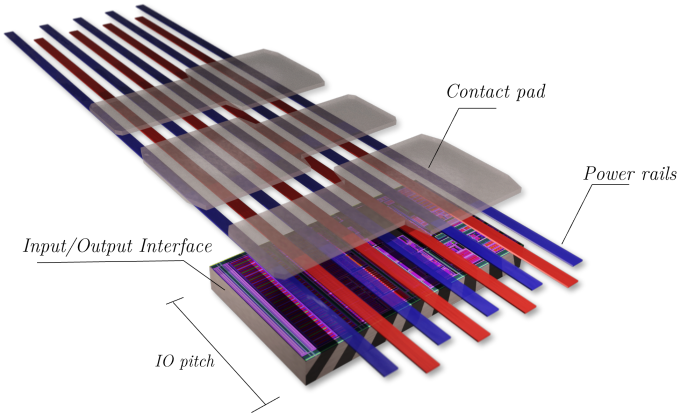


Figure 2.24: Pad ring structure

The total resistance and inductance of the pad ring is given by the resistance and inductance per pitch multiplied by the number IOs around the chip. In order to have low resistance path for the supply, the rails are designed using multiple metal layers. Typically, for a six metal layers technology process, the first and the second one are reserved for internal connections between the devices and from third up to the last one are used to carry the supply around the chip (see Figure 2.25).

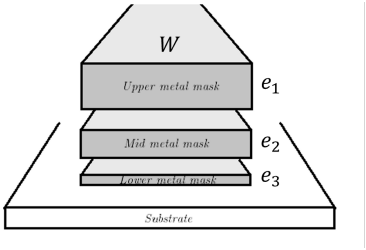


Figure 2.25: Power rails cross section

By knowing the thickness of each layer e and the width w the resistance is found using Equation 2.18. The typical resistance per unit length of a padring is around 0.6Ω/mm. The inductance is calculated with Equation 2.7 which gives a value of 0.2nH/mm. The capacitance between each of the conductor is found by simulation as presented in the next paragraph.

Device modelling

Every active device used in an IP contributes to the total impedance of the PDN. Generally, an IP powered between V_{dd} and V_{ss} can be modelled by a resistance and a capacitance as depicted in Figure 2.26.

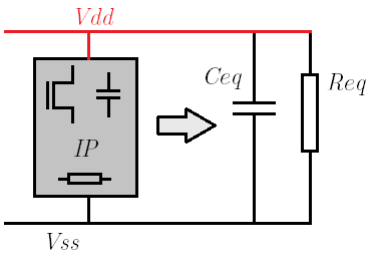


Figure 2.26: IP modelling

The resistance represents the consumption or the leakage of the IP on the supply, the capacitance is given by the sum of the intended capacitances with the parasitic capacitances of the devices. Consider a MOSFET transistor, its cross section is shown in Figure 2.27.

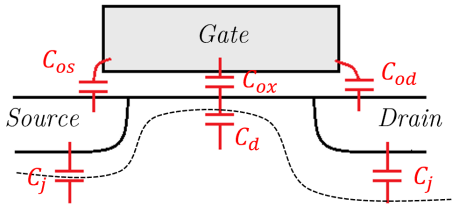


Figure 2.27: MOSFET cross section parasitic capacitance

The most important capacitance are described below:

- C_{ox} is the fixed capacitance between the gate and the substrate. Its value depends on the thickness t_{ox} of the oxide and on the surface of the device $A = W \cdot L$.

$$C_{ox} = A\frac{\epsilon_{ox}}{t_{ox}}$$

- C_d is the depletion-layer capacitance, its value depends on the wideness W_d of the depletion region which ultimately depends on the voltage applied on the gate [45].

$$C_d = \frac{\epsilon_s}{W_d}$$

  The overal gate capacitance is then given by the series combination between C_d and C_{ox}:

$$C_{gate} = \frac{C_{ox}C_d}{C_{ox} + C_d}$$

- C_{os} and C_{od} are the overlap capacitance and their value depends on the overlap between the gate and source/drain implantation.

- C_j is the junction capacitance that for reversed junction is determined mostly by the depletion layer capacitance C_d

The simulation result of the MOSFET capacitance in a standard 90nm CMOS process with $t_{ox} \approx 70 \cdot 10^{-10} m$ is shown in Figure 2.28:

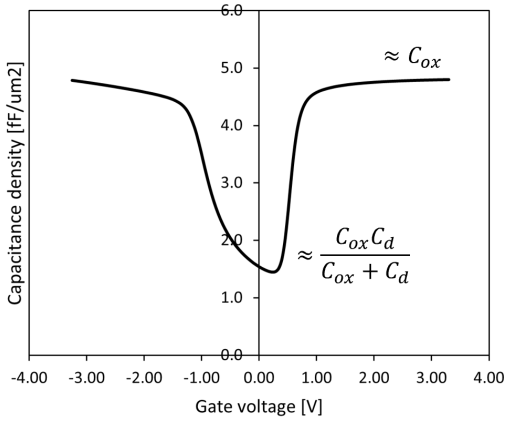


Figure 2.28: C-V plot for 90nm standard CMOS process

The capacitance value around 0V until the threshold voltage (around 0.7V) of the device follows the variation of the depletion region. Above the threshold voltage, in strong inversion, the capacitance is constant and equal to C_{ox}. The typical value for a 70Å oxide thickness process is around 5fF/μm^2. For accurate results, the overall capacitance of an IP can be found simulating the post-layout netlist of the circuit. Indeed, post-layout netlist groups all the parasitic information related to interconnections and device capacitance. Figure 2.29 shows the result small signal simulation of a typical General purpose IO in a microcontroller .

The DC polarisation voltage V_{DC} used for this simulation is set to 3.3V, the small input signal amplitude is 1V. The simulated DC current $(I^{AC})_{f=0}$ is equal to:

$$I_{DC} = \left(I^{AC}\right)_{f=0} = 10^{\frac{I_{DCdB}}{20}} = 10^{\frac{-206.13}{20}} = 49pA \tag{2.24}$$

The equivalent DC resistance shown in Figure 2.26 is then $R_{eq} = 20.4G\Omega$. As the frequency increases the impedance of the IP decreases and the current is then proportional to:

$$I_{AC} = I_{DC}\sqrt{1 + (2\pi f C_{IO})^2} \tag{2.25}$$

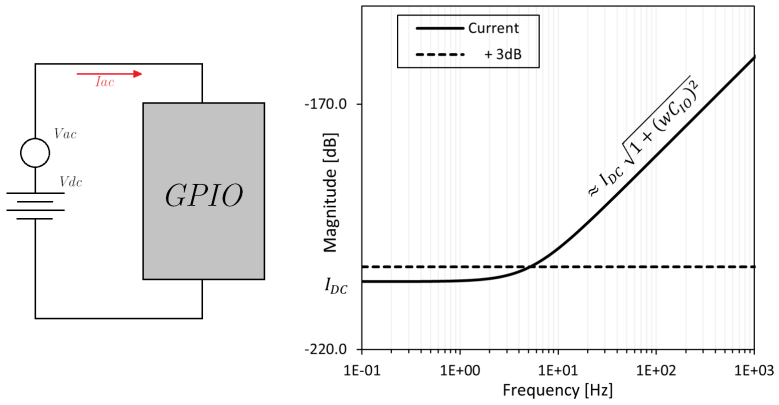


Figure 2.29: AC current simulation in standard IO interface

The +3db frequency allows the extraction of the equivalent capacitance:

$$C_{IO} = \frac{1}{2\pi f_{+3db} R_{eq}} \approx 1.4pF \tag{2.26}$$

It's interesting to notice that adding the gate surface of each transistor inside the IO and multiplying it by the capacitance density shown in Figure 2.28 a total capacitance of 3.2pF is found, which is 2.35 times the simulated capacitance. The factor 2.35 could be used for first order capacitance estimation for IPs of the same technological node if the total surface of used transistor is known.

The modelling of circuit inside the die has been described; indeed the impedance of the power rails were calculated with classical equations using their geometry and the impedance of the circuit powered by the rails were simulated through AC simulation on post-layout netlists. The same approach is valid for every circuit which has to be modelled inside the silicon die. As the pad ring was used for the modelling methodology description the global electrical model is presented in Figure 2.30. In this model, the parallel equivalent resistance of each IO is not represented. For small die size the presented electrical model can be simplified by assuming that the total inductance is negligible compared to the bonding inductance. Indeed, consider the circuit in Figure 2.31, where L_0 is the bonding wire inductance of the V_{dd} path and L_i is the inductance of the lumped model presented in Figure 2.30. For the sake of clarity R is not considered.

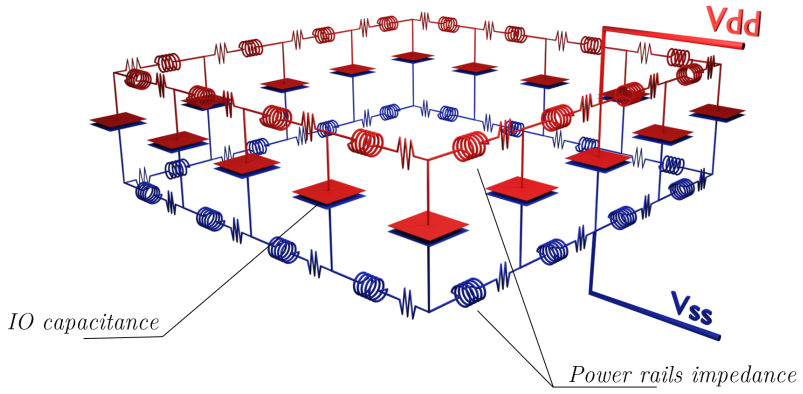


Figure 2.30: Pad ring final electrical model

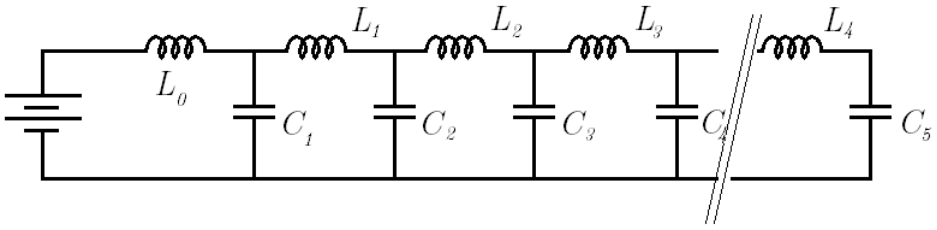


Figure 2.31: LC Pad ring equivalent circuit

For $L_i \ll L_0$ the circuit acts as a simple RLC circuit where:

$$\begin{cases} L = L_0 \\ C = \sum_i C_i \end{cases} \tag{2.27}$$

In conclusion, the modelling methodology for the EMC PCB, a standard package and a microcontroller was discussed. The following table resumes the most important equations and the orders of magnitude used in this chapter.

	Equation	Value
PCB	$C_{PCB} = A\frac{\epsilon_{ox}}{t_{ox}}$	$C_{PCB} \approx 140pF$
	$\frac{L_p}{l} \approx \frac{\mu_0}{2\pi}\left[\ln\left(2\frac{l}{w}\right) + 0.5 + \frac{w}{3l}\right]$	$L_p \approx 1.1nH/mm$
	$\frac{M_p}{l} = \frac{\mu_0}{2\pi}\left(\ln\left(\frac{2l}{D}\right) - 1\right)$	$M_p \approx 0.4nH/mm$
	$K = \frac{M}{L_1 L_2}$	$K \approx 0.4$
	$\frac{L_{via}}{h} = \frac{\mu_0}{2\pi}\left(\ln\left(\frac{4h}{d}\right) - 1\right)$	$L_{via} \approx 0.4nH$
	$\frac{R}{l} \approx \frac{\rho}{k\pi\delta(w+e)}$	$R \approx 3.8m\Omega/mm$
Package	$L_p = \frac{\mu_0}{2\pi} l\left(\ln\frac{2l}{r_w} - 1\right)$	$L_{bonding} \approx 4nH$
	$M_p = \frac{\mu_0}{2\pi} l\left[\ln\left(\frac{l}{d} + \sqrt{\left(\frac{l}{d}\right)^2 + 1}\right) - \sqrt{\left(\frac{d}{l}\right)^2 + 1} + \frac{d}{l}\right]$	$K = 0.4$
Die	C_{device} from simulation	$C \approx 5fF/\mu m^2$
	R_{rail} from layout analysis	$R \approx 0.6\Omega/mm$
	R_{IO} from simulation	$R > 10G\Omega$
	C_{IO} from simulation	$C > 1pF$
	L_{rail} from layout analysis	$L \approx 0.2nH/mm$

Table 2.4: Summary of RLC value for PCB, package and microcontroller presented in this chapter

2.2 Measuring the DUT

In the previous section, the modelling methodology was discussed and some measurements were shown to confirm theoretical calculations. These measurements were possible thanks to the setup described in this section. Before describing the actual setup, a brief analysis of existing resonances measurement methods is presented. The objectives of a measurement methodology are the following:

- It shall provide a clear image of the resonances of a system.

- It should not interfere with the DUT and so it should not introduced unwanted resonances in the critical frequency window (hundreds of MHz).
- As FTB is a fast common mode stress, a small difference in the DUT configuration (eg. connectors, cables etc...) could modify the immunity threshold of the device. In this context, the PCB should be kept identical to the one used for FTB estimation.
- It shall be executed automatically.

2.2.1 Resonance measurements in literature

The most important measurement methods proposed in literature for resonance analysis are [23] [29] [30]:

- The Global Resonance method
- The Near-field measurement method
- On-die measurement method

Global Resonance method

Figure 2.32 shows the general setup for the global resonance method. The DUT

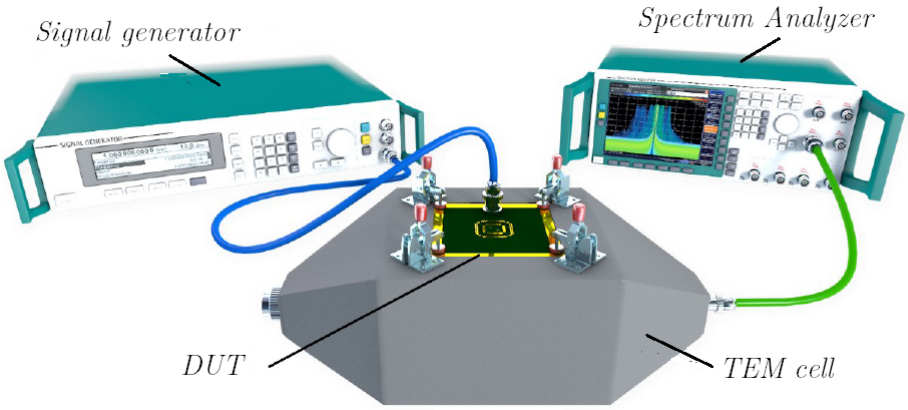


Figure 2.32: Global Resonance Method setup

is not powered and it is installed in a TEM cell which is connected to a spectrum analyzer. A signal generator sends a sinusoidal signal on the power supply of the device. The amplitude of the applied signal is set just below the threshold voltage of the core devices in order to minimize the non linearities. As the signal propagates in the DUT, the excited PDN starts radiating an electromagnetic field. The EM field couples with the septum of the TEM cell, the resulting signal is then amplified and sent to the spectrum analyzer. By sweeping the frequency of the input sinusoidal signal, the frequency response of the DUT can be measured. The main advantages of this method are:

Advantages	**Disadvantages**
No DUT modification needed to perform the measurement	DUT is not powered, on die capacitance effect is not visible
Automatic setup	Correlate the measurement with EM simulation is complicated
Simple and fast execution	No spatial accuracy on the measurement

Table 2.5: Global Resonance method advantages and disadvantages

Near-field measurement method

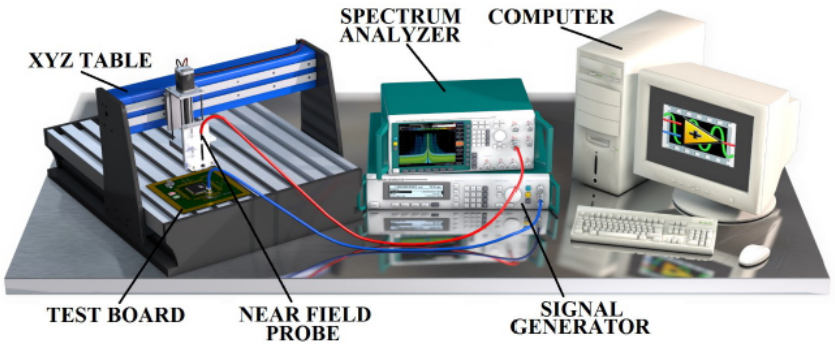


Figure 2.33: Near-field measurement setup

The near-field measurement is similar to the global resonance method but it improves the spatial accuracy by substituting the TEM cell with a near-field probe. The probe is placed above the microcontroller and it is moved step by step with a XYZ table. The captured EM is then displayed on the spectrum analyzer.

Advantages	**Disadvantages**
No DUT modification needed to perform the measurement	DUT is not powered, on die capacitance effect is not visible
Automatic setup	Correlate the measurement with EM simulation is very complicated
Very high spatial accuracy at high frequency	Very long measurement and complexity

Table 2.6: Near-field measurement method advantages and disadvantages

On-die measurement method

One of the critical point of the FTB evaluation is that no measurement is possible during the test. Indeed, the generated common mode noise perturbs all the electrical equipments in the vicinity and no reliable measure is possible. The idea behind the on-die measurement is to measure the injected stress from inside the microcontroller, store the result of the measurement and the get the results out of the silicon once the FTB stress is terminated. This is achieved with a analog to digital flash converter placed in a specific area inside the microcontroller. The ADC measures the stress on the main supply domain and convert it in a binary code. The code is then sent out of the die after a time delay. Despite being an interesting solution, this solution requires an important silicon surface and so an unacceptable high cost for standard STM32 platforms.

2.2.2 Resonance Analyzer

A new measurement setup was developped to be able to easily characterize the

resonances of the DUT. The measurement bench is shown in Figure 2.34.

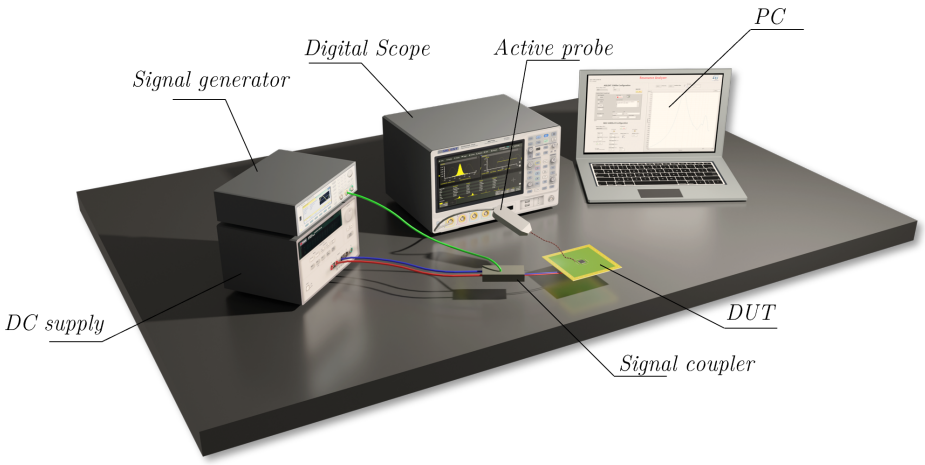


Figure 2.34: Resonance analyzer bench

The general principle is the following: a sinusoidal signal is sent on top of the DC power supply to the DUT. The residual signal is probed the closest possible to the microcontroller and plotted on the digital storage oscilloscope (or DSO) which calculate the peak-to-peak value. By sweeping the frequency of the input signal, a LabView routine is able to trace the amplitude measured by the oscilloscope as a function of the input frequency. To have the measurement working properly some details shall be discussed.

Inputs

The DUT is powered by a DC power supply at the nominal voltage, typically 3.3V. A waveform generator produces a sinusoidal signal whose amplitude is set to 0dBm on a 50Ω load. This corresponds to an amplitude of 315 mV peak which, once added to the nominal voltage, leads to 3.615V as the maximum value on the supply. The amplitude is chosen to be high enough to have still a sufficient amplitude to be probed by the oscilloscope, but not too high to exceed the absolute maximum rating of the microcontroller. The coupler is an electronic circuit designed to

couple the input signal to the PDN of the DUT without damaging the DC power supply. The principle schematic is given in Figure 2.35.

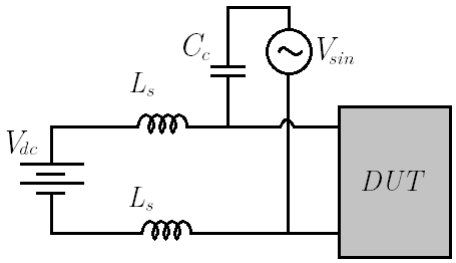


Figure 2.35: Coupler principle schematic

L_s are series inductances used to avoid the input signal V_{sin} to propagate towards the DC power supply. Their value has to be carefully chosen to avoid spurious reset diring the start-up routine of the microcontroller. Indeed, every microcontroller has a different current profile at start. If the inductance value is too high, they may compromise the start-up phase of the device by limiting the current. C_c are a bank of capacitors which have to let the input signal pass without any attenuation for a given input load. Indeed, the frequency response of the coupler should be flat for frequency less than 200 MHz.

DUT

The hardware DUT configuration shall be the same as the one used for FTB evaluation. Indeed, this measurement method does not require any modification in the PCB. Nevertheless, some software adjustment must be done. The goal is to obtain the pure resonance frequencies of the PDN. For that reason the microcontroller is powered but it is set to an idle state, the Wait For Interrupt (or WFI) state. In this state, the device is on hold waiting for an interrupt event to wake up and to continue the fetch-decode-execute cycle. This avoids the generation of unwanted resonances produced by the internal activity (like oscillators) which could cover or modify the intrinsic resonances of the PDN. Furthermore, the firmware is coded in order to have two IOs set in output mode respectively to '1' and '0'. By setting to '1' and '0', the output of the two IOs are direct images of the V_{dd} and

V_{ss} inside the die (see Figure 2.36). The choice of the IOs is important to avoid any filtering on the output signal up to hundreds of MHz.

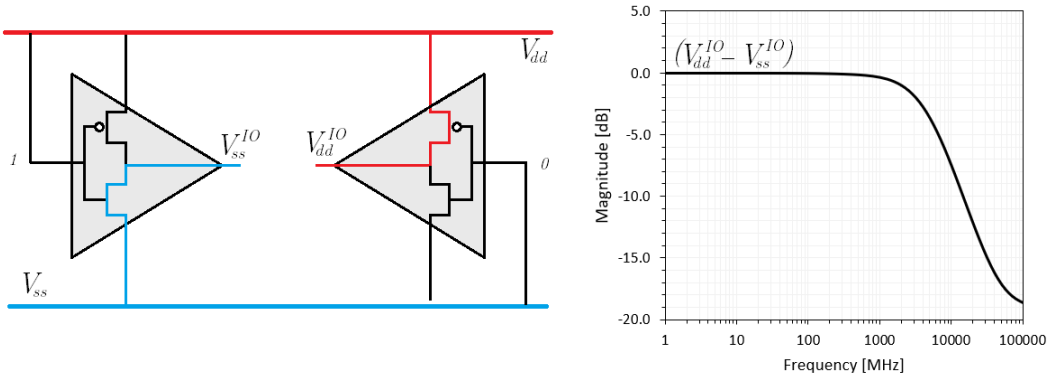


Figure 2.36: IO configuration used to set the measurement points and its transfer function

Output

The PDN is measured with a wide band differential active probe between the two IOs. The probe features a high common mode rejection and low input capacitance. Its high impedance at both input allows good single-ended measurement without introducing a ground loop. The input model of the probe is shown in Figure 2.37 [46]. The differential input capacitance C_i is around 0.1 pF while

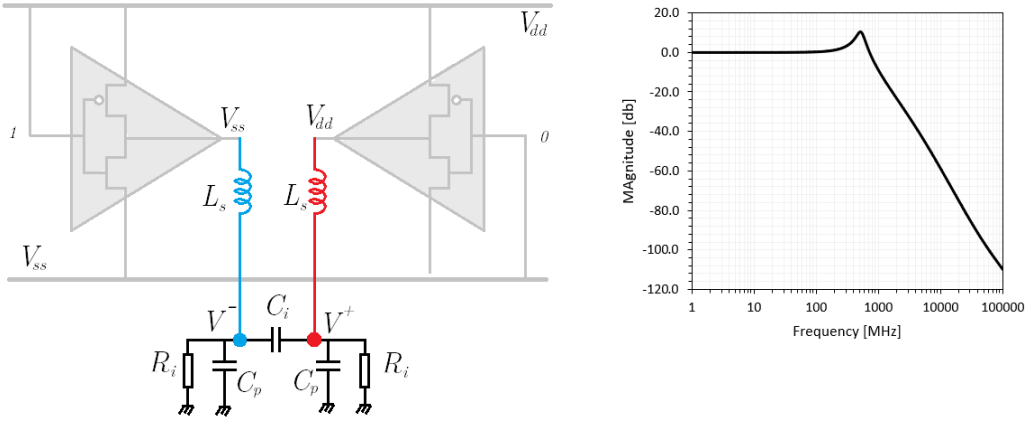


Figure 2.37: Probe input model and simulation

the common mode capacitance C_p is 3pF. The input resistance to earth ground is

1MΩ. L_s is the total estimated inductance from the IOs pad to the probe, in this case 30 nH. The signal is then plotted on a digital oscilloscope which is controlled by a Labview routine. The LabView program front panel is given in Figure 2.38.

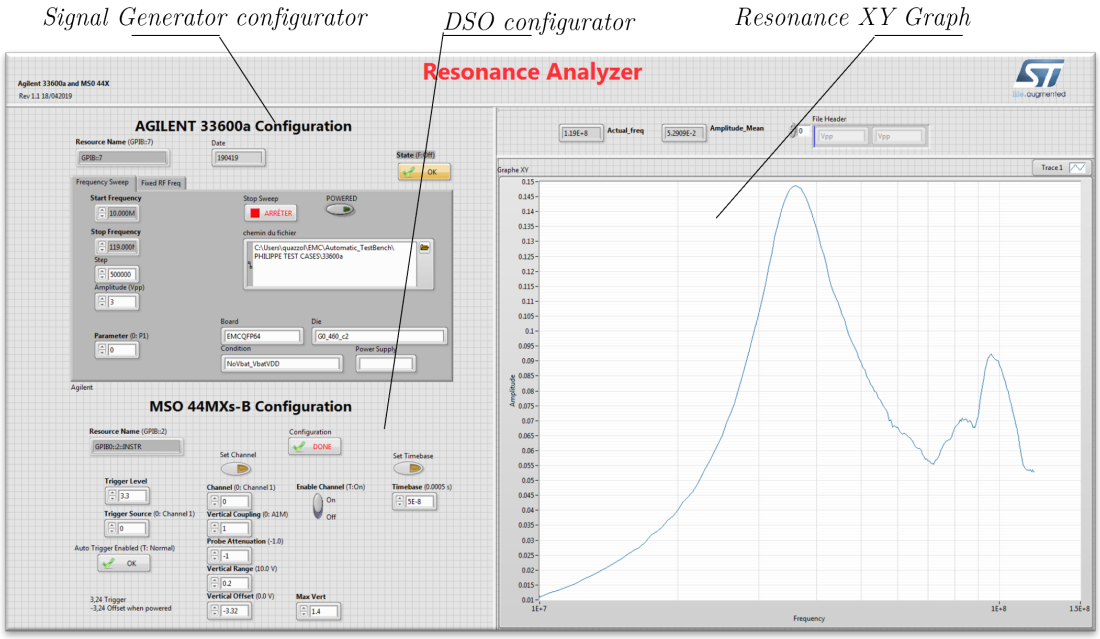


Figure 2.38: LabView Resonance Analyzer front panel

The program accomplishes three different tasks:

- Configuration of the digital oscilloscope: the program sets the trigger and the horizontal scale automatically to have the highest accuracy.
- Configuration of the signal generator by setting the amplitude and managing the frequency sweep in time.
- Plotting the results.

Frequency is increased by step of 1MHz from 1 to 150 MHz. For each frequency step, the DSO measures 30 times the peak-to-peak amplitude and sends it to the program. The LabView program then computes the mean and the standard deviation and plot the results in a XY graph.

2.3 Conclusion

This chapter started from the initial hypothesis about the resonances being correlated to FTB immunity to describe two fundamental aspects: the modelling and the measurement techniques of a DUT. Indeed, a good modelling methodology is important to be able to find and to explain the resonances of a system. The presented DUT is defined by a PCB, a package and a microcontroller silicon die. The PDN modelling of each of these parts was deeply discussed with equations and examples. In particular, by hand modelling was recommended for low complexity PCB to better understand the phenomena behind the resonances. For package modelling, ANSYS Q3D tool and the mathematical models it produces were discussed. A software modelling toll is indeed mandatory for high density geometry like QFP, BGA or CSP packages. The PDN of the microcontroller was analysed and some necessary approximations and simplifications were adopted and explained. Post-layout simulations and process technology knowledge are essential to establish a first-order electrical model of such a complex system. In the second part of the chapter some interesting methods for measuring resonances of a DUT were presented: the global resonances method, the near-field measurement and a on-die measurement circuit. The advantages and disadvantages of each of the method were presented and a novel method was discussed: the resonance analyzer. This measurement setup combines most of the advantages of the global resonance and near-field method. Indeed, it allows a valuable evaluation of intrinsic resonances of the PDN using standard electronic equipment and for a low-cost. In the next chapter, the modelling and measurement techniques presented in this chapter are applied to some DUT configurations in order to prove the initial hypothesis by:

- Finding the resonances of the DUT by simulation and by measure.
- Evaluating the FTB immunity of such configurations and correlate them with the resonances
- Evaluating some immunity techniques by simulation and measurement

Chapter 3

Resonance analysis and FTB measurements applications

Contents

In this chapter, the modelling and measurement techniques described in Chapter 2 are applied on several DUT configurations. In particular, the PCB, the package, and the die model are combined together to built the total DUT electrical model. Thanks to this model, the impact of some parameters on resonances is discussed. In particular, the effect of different decoupling capacitance configurations on PCB, the measurement point and the die polarisation are analysed. To complete the analysis three configuration are chose as examples and both resonances and FTB evaluation results are given. The resonances of each configuration is found by simulation and measurement showing a good correlation of both amplitude and frequency. Furthermore, FTB test is performed for each of the configurations and the results are compared to the resonance levels obtained to verify whether resonances are a useful tool for FTB immunity evaluation.

3.1 DUT identification

In Chapter 2, electrical models for PCB, package and die were introduced. A particular DUT configuration is chosen as test case and is detailed in the following paragraph.

The microcontroller chosen as test case is one of the smallest microcontroller ever produced by STMicroelectronics. Indeed, it belongs to the mainstream microcontroller family which, in this work, will be referenced as *STM32X*. Some of the main features are:

- Arm Cortex-M0+ at 64MHz
- Maximum IOs count
- Low power features as Shutdown and standby modes.
- Smallest possible package down to 8-pin.

This microcontroller represents one of the most challenging project in term of EMC compatibility. Indeed, the microcontroller die size is reduced to minimum. Furthermore, marketing objective was to maximise the IOs pin count by reducing the number of supply pair as much as possible for small packages (up to 64 pins) as depicted in Figure 3.1.

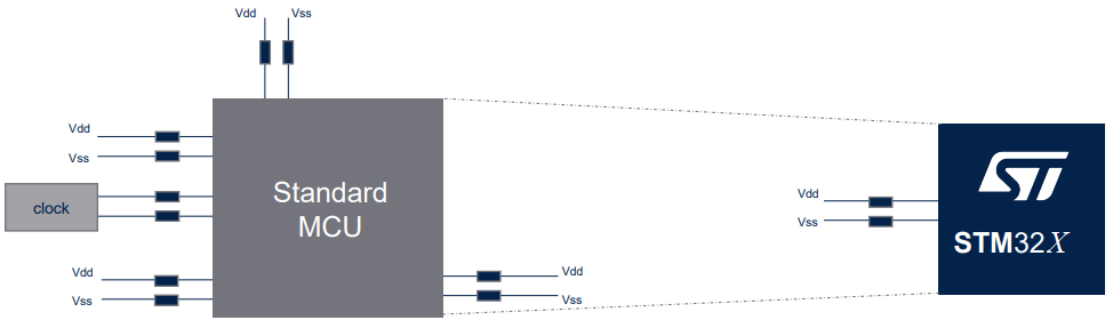


Figure 3.1: STM32X supply configuration vs standard STM32

These design choices led to some EMC major issues. One of the most critical was indeed the FTB susceptibility. During FTB test, the positive and negative threshold for the 64-pin package are shown in Table 3.1.

Configuration	$\mathbf{FTB^{+}_{Vth}}$	$\mathbf{FTB^{-}_{Vth}}$
STM32X - cut 1.0 - LQFP64	+2.0kV	-2.9kV

Table 3.1: STM32X FTB negative and positive immunity threshold

As it can be seen, the immunity threshold levels are far from the minimum acceptable value (4.5kV) and so, some solutions had to be found and implemented on a new silicon cut 2.0 before selling it on the market. In this context, this DUT is a great test case and opportunity to verify whether the resonance modelling and measuring approach developed could be used as a EMC tool to understand and improve susceptibility. In particular, different configurations are studied to show both package and die influence on resonances and FTB behaviour. PCB immunity solutions are not considered in this work as the PCB depends often on the application. Instead, any package or die solution found could represent a real added value to the product and to the company. In the next paragraphs three main configurations are studied depending on the package and the silicon die revision. These configurations are presented in Table 3.2.

Name	PCB	Package	Die
A	IEC 61967-2	LQFP64	STM32X Cut 1.0
B	IEC 61967-2	LQFP64	STM32X Cut 2.0
C	IEC 61967-2	LQFP32	STM32X Cut 2.0

Table 3.2: DUT Configurations

The PCB was already discussed in Chapter 2 and it is the same for the three configurations. Configuration *A* and *B* have the same LQFP64 package but different microcontroller dies, respectively *Cut 1.0* and *Cut 2.0*. The differences between these two silicon cuts are explained later in the chapter. Configuration *C* is built with *Cut 2.0* silicon die but in a smaller package, the LQFP32.

3.2 Resonance simulation and measurement for configuration A

The comprehensive electrical model is obtained following the steps presented in chapter 2. In particular, it is built by combining the EMC PCB, the LQFP64 and the microcontroller model. As said in chapter 2, we are interested only in the main PDN of the devices, that is the one where the FTB stress is injected into. Looking at the main PDN of the microcontroller three main power domains are identified:

- Primary IO power domain which supplies most of the Input/Output interfaces
- Secondary IO power supply which supplies small low-power circuits providing few functionalities while in battery mode. In normal mode (no battery) this domain is internally shorted to the primary IO domain through a power switch whose impedance is tens of ohms.
- Analog power domain which supplies all the analog circuits such as the power management unit, DAC and internal oscillators.

The overall capacitance of each domain is given by the sum of the capacitances of the devices inside and it is given in Table 3.3:

$\mathbf{C_{IO1}}$	$\mathbf{C_{IO2}}$	$\mathbf{C_{ana}}$
260pF	10pF	100pF

Table 3.3: Power domain extracted capacitance

The PDN of the LQFP64 package consists of only three paths, two for the positive supply voltage and one for ground. Indeed, the analog and the primary IO power domain are bonded together on the same pin V_{DD}, the secondary IO power domain is bonded to a dedicated external pin V_{BAT}. The ground of the entire chip is the P-substrate and no isolated P-type diffusions are present. Multiple ground pads are bonded to an unique package pin V_{SS}. Figure 3.2 shows the actual bonding diagram and pinout of configuration A.

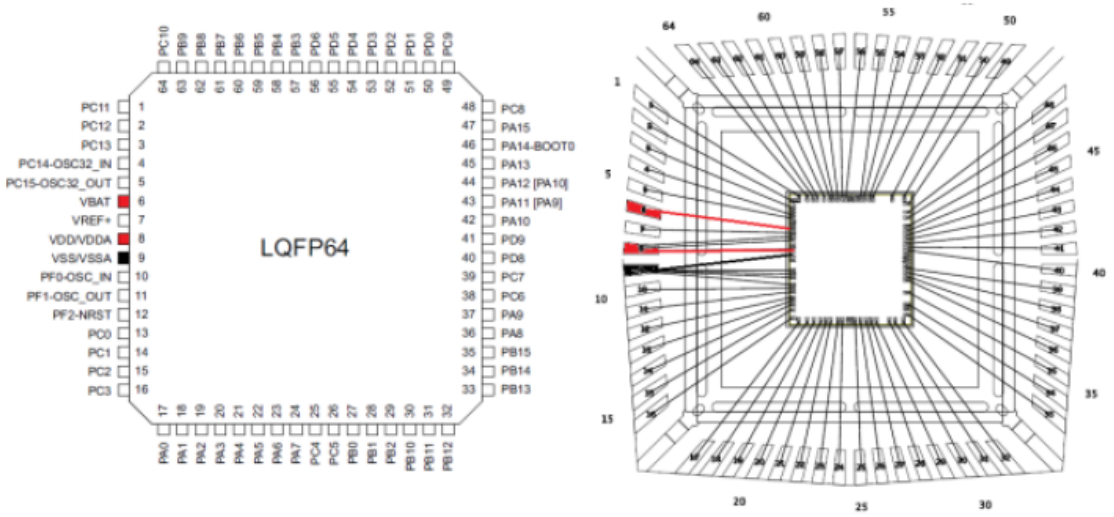


Figure 3.2: Configuration A bonding diagram and pinout

At PCB level, package pins are connected following the EMC standard and the microcontroller datasheet. In particular, V_{DD} and V_{BAT} pins are connected each to a 100nF decoupling capacitor on the top layer, and V_{SS} pin is directly shorted to the PCB ground plane as depicted in Figure 3.3.

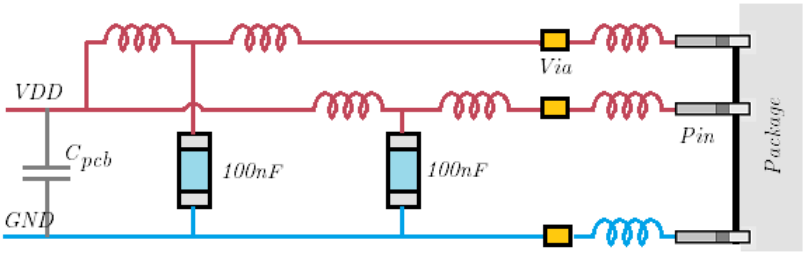


Figure 3.3: PCB simplified model for configuration A

As presented in Chapter 2, the RLC model of PCB and package is obtained respectively by hand calculation and using Q3D software. Die model is deduced by layout analysis and simulation. The total simplified model is then shown in Figure 3.4.

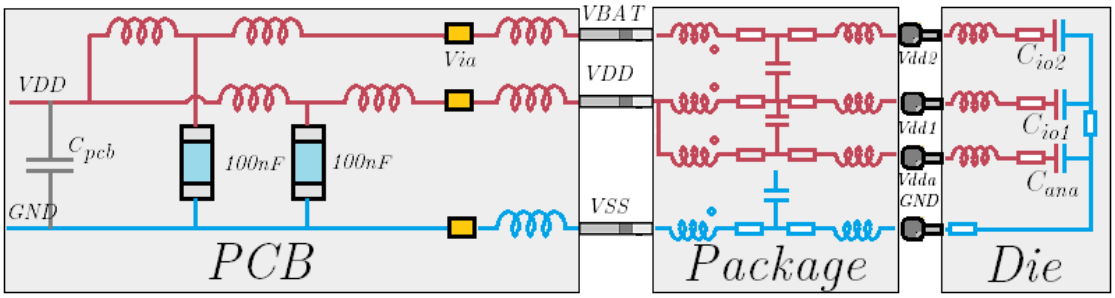


Figure 3.4: Complete simplified model for configuration A

Simulation and measurement results are given in Figure 3.5.

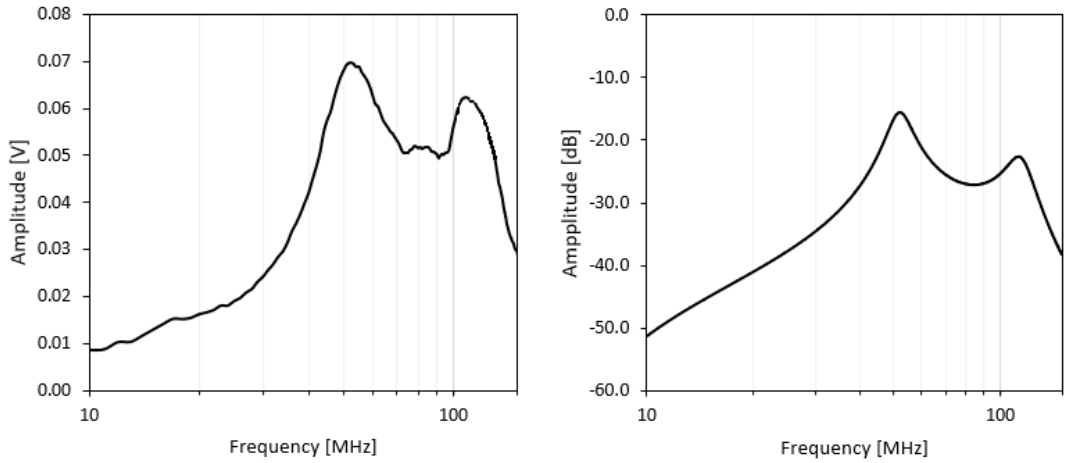


Figure 3.5: Measurement (a) and simulation (b) on Configuration A

Simulation and measurement results show two main resonances in the critical frequency window: one dominant at 53 MHz and a second one at about 120 MHz which could be related to FTB low immunity. Some modifications of either the PCB, the package or the die would lead to different frequency behaviour and thus it could be used to determine whether those resonances are related to low FTB immunity. To be able to change the resonances efficiently, it's important to understand where they come from and which design element contributes the most to them.

PCB influence on resonances

Two different configurations were chosen to highlight the impact of decoupling placement on the resonances of the system. First one is obtained by keeping only the V_{DD} decoupling capacitor, the second one only V_{BAT} capacitor.

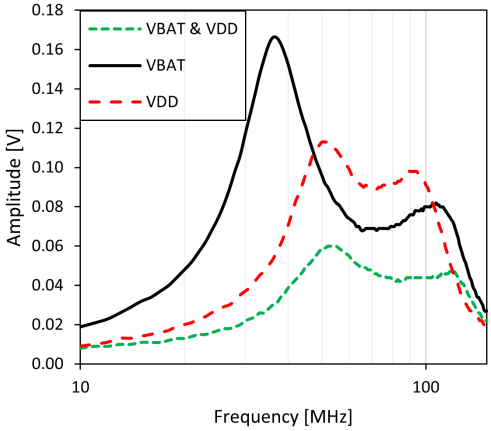


Figure 3.6: Resonances for different PCB configurations

In section 3.3 these resonances are shown to be correlated to different levels of FTB immunity. It's interesting to notice that the dominant frequency is shifted to lower frequency when V_{BAT} capacitor is the only one welded on the board. The second frequency is less affected by the left shift. This is explained considering the two resonance frequencies generated by two different RLC loops which resonate independently in a first order approximation. This two loops are highlighted in Figure 3.7.

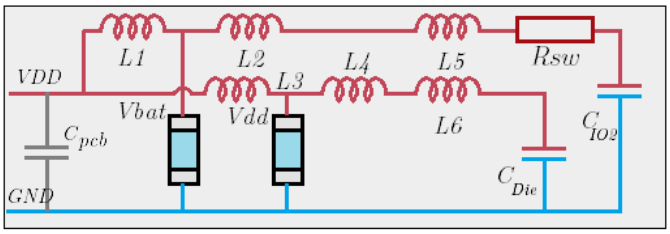


Figure 3.7: RLC resonant loops

L_1 to L_6 are generic inductances brought by PCB connection and package. Their value is extracted following Table 2.4. $L_1 = L_3 \approx 10nH$ and $L_4 + L_6 =$

$L_2 + L_5 \approx 15nH$. C_{die} is the intrinsic die capacitance given by the primary IO power domain and the analog part. A first resonant loop is given by L_4, L_5 and C_{die} This correspond to the first resonant frequency ${f_1}^{-1} = 2\pi\sqrt{(L_4 + L_5)C_{die}}$. The second resonant frequency is given by C_{PCB}, L_1, V_{BAT} or C_{PCB}, L_2, V_{DD}. As presented in chapter 2, this correspond to the resonance frequency of the EMC board at about 120 MHz. By looking at Figure 3.6, it can be noticed that the first peak is given by the resonance of the die capacitance with the inductance of the line connecting to the closest decoupling capacitor (L_4 and L_6). In that sense, having both V_{DD} and V_{BAT} capacitance produces the same first resonance in term of frequency. Instead, when only V_{BAT} capacitor is present the total inductance between C_{die} and the closest capacitor is increased by L_3 and L_1, thus causing the frequency to shift to a lower frequency around 38 MHz.

Internal and external resonances

In previous paragraph the resonance of the die and of the PCB were introduced. The frequency of these resonances depends on the global characteristics of the RLC network, the amplitude instead depends on the measurement point. Indeed, according to the measurement point the relative amplitude is different. Figure 3.8 shows the same RLC network where the probing point is either on the decoupling capacitor or inside the die by using two IOs as explained in chapter 2.

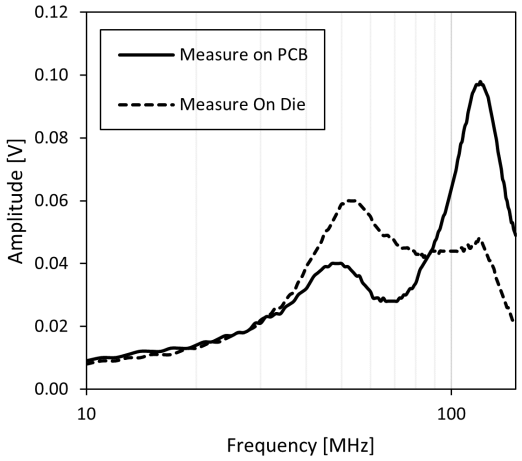


Figure 3.8: Internal versus external resonances

As it can be seen, resonances amplitudes are not the same depending on the measure point. Indeed, the PDN of the die is resonating at the first resonance frequency, while the PCB is aligned to the second one. This is crucial because it suggests that the first resonance is most likely the most important one to be considered in order to reduce FTB propagation inside the microcontroller. To validate this behaviour a specific software was developed to make 16 IOs, from PA0 to PA15 (cf. Figure 3.2), commuting at the same time. The simultaneous switching noise is measured through two IOs, PC10 and PC11. Having all the IOs commuting at the same time excites the internal power distribution network making it oscillating at its natural frequency. The results are given in Table 3.4:

Probing point	**Toggling IO**	**VDD cap**	**VBAT cap**	**Frequency**
PC10-PC11	PA0:PA15	100nF	100nF	53.8 MHz
PC10-PC11	PA0:PA15	NA	100nF	37 MHz
PC10-PC11	PA0:PA15	100nF	NA	55.1 MHz

Table 3.4: PDN internal natural oscillation when 16 IOs switching simultaneously

As it can be seen, the internal natural frequency corresponds to the first resonance obtained in simulation and measure for each of the decoupling capacitor configuration.

Die polarisation impact on resonances

As seen in chapter 2, die capacitance is mainly due to the sum of the capacitances of each device. The value of the capacitance is then dependent on the polarisation voltage of the chip. Figure 3.9 shows the impact of die polarisation on the resonances of the system. For this comparison the probing point is fixed on the PCB as die probing is not functional when the microcontroller is not powered.

As it can be seen, first resonance is affected by the polarisation. Indeed, when the microcontroller is not powered only the total die capacitance is reduced to the minimum value. By comparing the resonance frequencies the percentage drop of total capacitance at 0V is easily calculated as:

$$\Delta C_{die} = \frac{f_{3.3V}}{f_{0V}} = 40\% \tag{3.1}$$

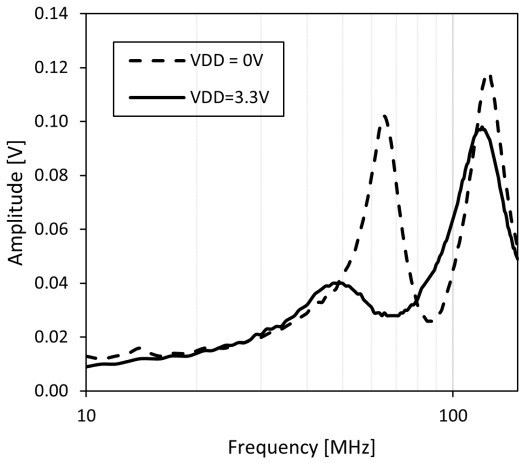


Figure 3.9: Polarisation influence on resonances

In conclusion, as most of the embedded capacitance depends on the voltage, the polarisation of the device and of the circuits inside plays an important role in the amplification of the stress. A better way to prevent low power circuits to be more sensitive to FTB would be using voltage independent capacitance solutions. This is presented in the next section.

3.3 Resonances and FTB immunity correlation

In the previous section, the resonances of the PDN of the configuration *A* was shown. In particular, two main resonances were found to be in the critical frequency window of tens MHz. A dominant one related to the die capacitance and a second one generated by the EMC PCB design. Despite the resonances being found both on simulation and measurement, the correlation with its low immunity threshold against FTB is still to be proved. In this section some modifications are applied both on die and package to change the resonance spectrum of the DUT and see if any susceptibility improvement is observed.

Die capacitance effect

In previous section, die capacitance polarisation was found to be an effective

way to change the first dominant resonance peak. Furthermore, the first resonance was found to be the natural oscillation frequency of the internal PDN. The natural consequence would be to try to change the resonance amplitude and frequency in order to see if that improves the overall FTB immunity of the device. To do so many possibilities open up:

- Improve IP robustness by changing the design
- Change decoupling capacitor placement so as to decrease the total inductance between it and the die capacitance. This is done by changing the layout of the PCB or by changing the package into something more complex as "System in Package" where decoupling capacitor are placed inside.
- Add decoupling capacitor inside the die.

The first solution is not a profitable solution as, at present, the real cause of system failure under FTB stress are not known. As it was said in the first chapter, FTB failure mechanism is most of the time categorised as Hardfault, that is the CPU cycle somehow interrupts the normal execution. In that sense, other things than improving the robustness of all the IPs building the microcontroller is useless. Yet, this would be extremely expensive in design cost and would certainly impact die size and so the total chip cost. The second solution is interesting and some applications are given in the general conclusion of this manuscript, yet the EMC PCB is defined by the IEC standard and as long as the same PCB is used for the evaluation of all the microcontrollers it can be used to do comparison of the immunity of different devices. Furthermore, as a semiconductor company STMicroelectronics is not interested in studying PCB solution to EMC problems as the circuit board is always designed by the final customer and it depends on the application where the microcontroller is employed. Last solution is the best as it does not require any change in the design of the microcontroller. Nevertheless, adding on-die capacitance should not result in an increased die size as it would be in contrast with the STM32 low-cost mainstream philosophy.

To change resonance frequencies of the configuration A, some internal capacitances were added in a second development cut of the microcontroller. In this cut 2.0, the design functionalities and IPs are kept identical not to compromise the study. The choice of the capacitance to add and the placement is fundamental.

As the microcontroller is a mainstream component, some silicon area is generally wasted. Indeed, most of the block coming from previous microcontroller generations are reused to build a new device. In that process, it's impossible to guarantee that the 100% of the silicon chip area is filled with active devices. For cut 2.0, all the empty space both in the core and in the pad ring was filled with decoupling capacitor. Figure 3.10 shows the layout of the complete microcontroller, black zones identify regions where there is no N/P implantation. Red boxes in cut 2.0 identifie the zones where capacitance is added.

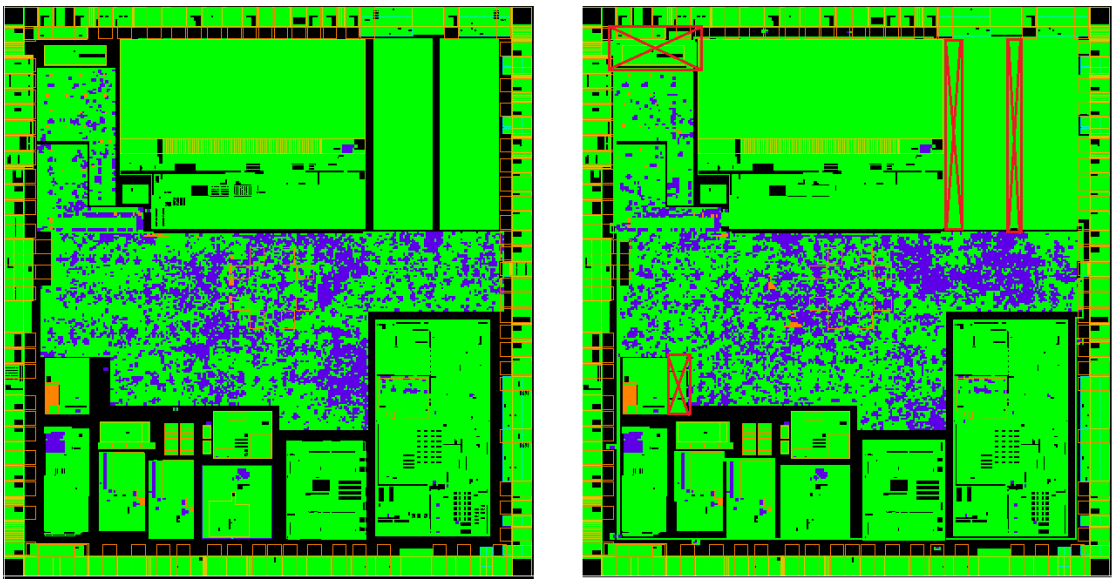


Figure 3.10: Cut 1.0 versus cut 2.0 microcontroller layout

The total added capacitance in padring and in core is given in Table 3.5.

Cut	$\mathbf{C_{Die}}$
1.0	260pF
2.0	930pF

Table 3.5: Cut 1.0 versus Cut 2.0 on-die capacitance

The choice of the capacitance to be integrated depends on the technology. Usually different types of capacitor are available in a design kit. Table 3.6 shows the principal ones.

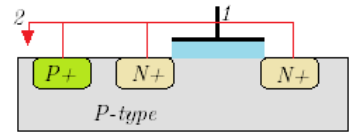
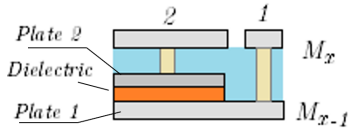
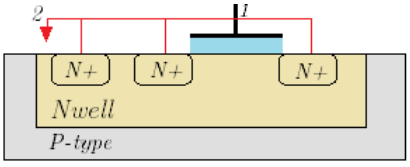
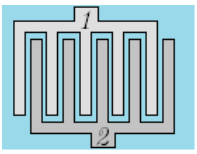
Capacitor	Structure
PMOS or NMOS	
MIM	
Native NMOS	
MOM	

Table 3.6: Standard capacitor structures in CMOS technology

Standard PMOS/NMOS capacitors are easy structure with good capacitance per unit-area value. The main disadvantages are the high inaccuracy and the important Process-Voltage-Temperature (or PVT) dependence. Metal-Insulator-Metal (or MIM) capacitors are built with extra mask layer allowing thin distance between the two metallic plates. Their use is limited as having supplementary masks increases a lot the fabrication cost of the device. Metal-Oxide-Metal (or MOM) capacitor are the most used device when a high value capacitance is needed. The capacitance value is given by the distance between each finger of the inter-digit structure. With the increasing metal layers available and with the shrinking of the metal distances, MOM capacitor have become the best solution providing high capacitance per unit-are value. The main drawback is that MOM capacitor uses the same metal layers as the signals and power interconnections. So, this kind of capacitor takes away most of the routing possibilities. Its use is not possible in padring as power rails running all around the chip are drawn using as many metal layer as possible to decrease impedance. In the core as well using MOM capacitor would require a complete re-routing of all the signals which is unacceptable for

a cut 2.0 development. In this context, the best choice is the Native NMOS capacitor. It is a NMOS structure where the Pwell is replaced by a Nwell. Under these condition, the NMOS voltage threshold is near 0V, so the channel is built as soon as a gate voltage is applied. This allows a high value capacitance even at low voltages as shown in Figure 3.11. The main drawback is that having the Nwell at 0V requires a strong P-type substrate polarisation in order to avoid latch-up issues. This is accomplished by a massive use of guard ring barriers around the Native NMOS.

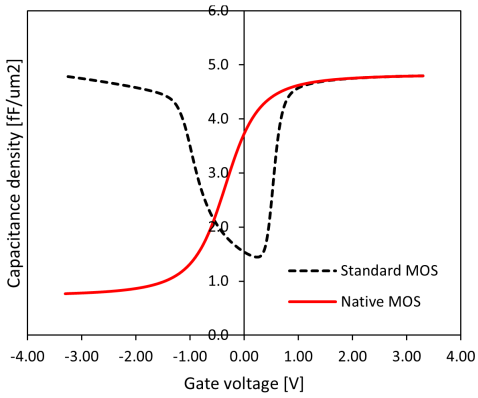


Figure 3.11: Standard versus native MOS capacitance in 90nm CMOS process

In order to see the impact of the added capacitance on the cut 2.0, a simulation is performed on the model presented in Figure 3.4. The results are given in Figure 3.12:

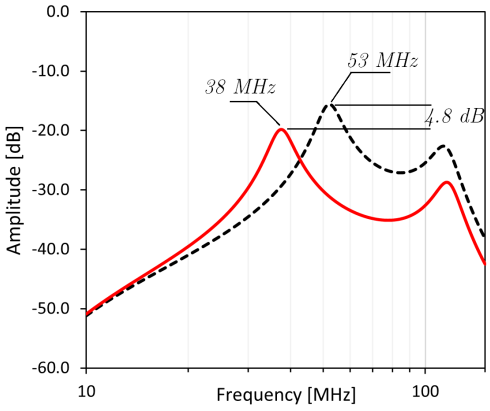


Figure 3.12: Cut 1.0 versus Cut 2.0 resonance simulation

As predicted first resonance peak of cut 2.0 should be shifted towards lower frequency and it's amplitude reduced approximately by a factor of:

$$\frac{A_{cut2.0}}{A_{cut1.0}} = \sqrt{\frac{{C_{die}}^{cut1.0}}{{C_{die}}^{cut2.0}}} = 0.53 \quad (\approx -5.5\text{dB}) \tag{3.2}$$

Both resonance measurements and FTB test results are given in Figure 3.13 and Table 3.7.

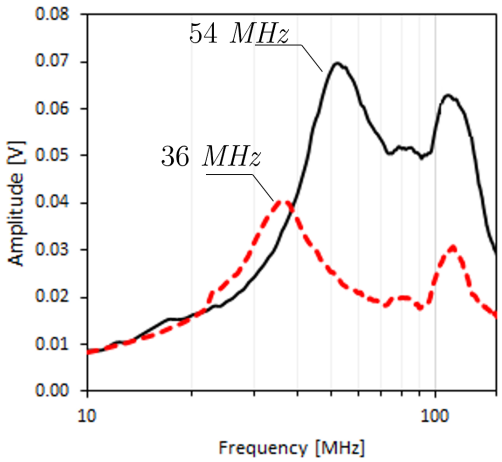


Figure 3.13: Resonance measurement for cut 1.0 and cut 2.0

	$\mathbf{FTB^{+}_{Vth}}$	$\mathbf{FTB^{-}_{Vth}}$
Cut 1.0	+2.3kV	-3.0kV
Cut 2.0	4.5kV	-4.5kV

Table 3.7: Cut 1.0 versus Cut 2.0 FTB results

As it can be seen, the resonance measurements confirm the resonance and amplitude change predicted with simulation, the observed amplitude reduction is approximately 5dB. Furthermore, FTB results on cut 2.0 are positive with a considerable improvement in fast transient stress immunity. The failure threshold is increase both for positive and negative stress up to 4.5kV which sets this microcontroller as one of the more robust device (for EMC) in STMicroelectronics portfolio. In conclusion, the resonance analysis is found to be a useful and predictive tool for FTB evaluation. The same approach is used to see if any other

parameters could affect the FTB performances. The following study is done on the third configuration C presented in Table 3.2. Configuration C is built with the same robust microcontroller (Cut 2.0) but with a smaller package LQFP32. The bonding diagram as well as the pin-out is given in Figure 3.14.

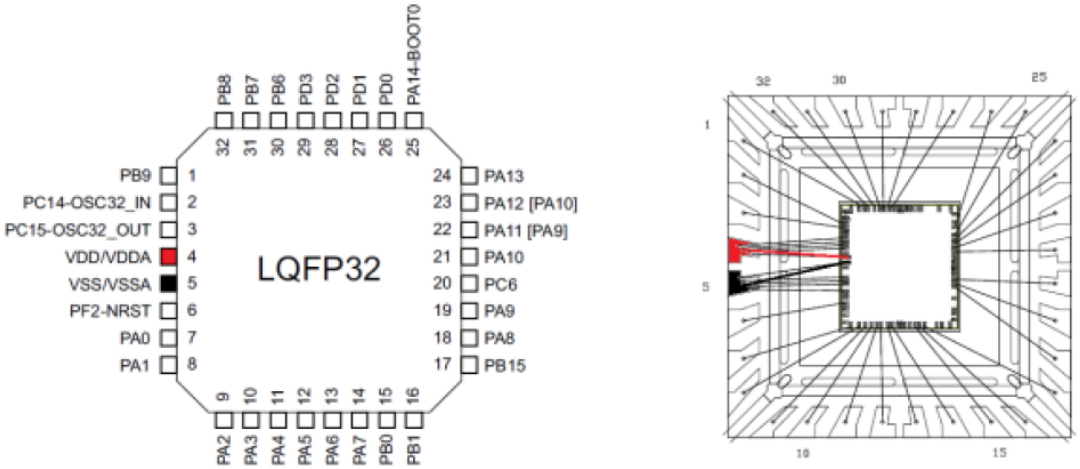


Figure 3.14: LQFP32 package for configuration C

As shown in Figure 3.14 in LQFP32 the V_{BAT} pin is missing as the pad is internally bonded together with V_{DD} to the external main supply pin. The RLC model built for configuration A and B is still valid with few modifications as depicted in Figure 3.15:

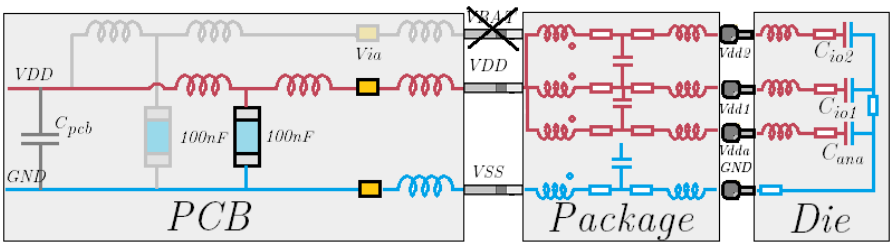


Figure 3.15: Complete simplified model for configuration C

The simulation and measurement results are given in Figure 3.16.

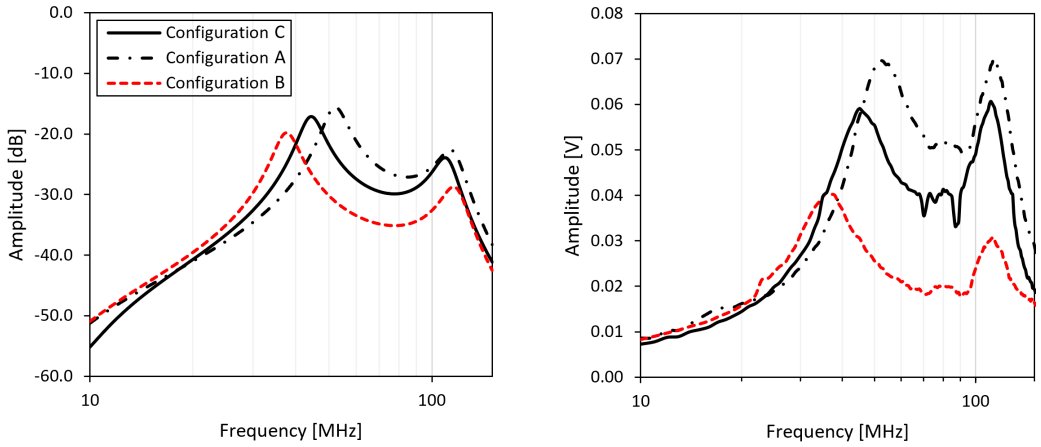


Figure 3.16: Configuration comparison simulation and measurements

As it can be seen, configuration with LQFP32 package shows a higher resonance frequency than the same configuration but with LQFP64 (B), this is mainly due to lower inductance value for shorter bonding wires. This configuration, as for resonance analysis, stands in the middle between configuration A and B and this is confirmed also by FTB results presented in Table 3.8.

Name	**Configuration**	$\mathbf{FTB^{+}_{Vth}}$	$\mathbf{FTB^{-}_{Vth}}$
A	Cut 1.0 LQFP64	+2.3kV	-3.0kV
B	Cut 2.0 LQFP64	4.5kV	-4.5kV
C	Cut 2.0 LQFP32	3.3kV	-3.9kV

Table 3.8: FTB results

In conclusion, through this real application the resonances are proved to be correlated to FTB immunity thresholds.

3.4 Conclusion

In this chapter a real application case is analysed. In particular, three different configurations of the same STM32 mainstream microcontroller are chosen. The

first one is the reference showing very low FTB immunity. The second one is defined by the same PCB and package but with some modifications of the microcontroller consisting in more on-die capacitance. The third one is selected with a smaller package LQFP32. These three configurations are evaluated with the Resonance Analyzer and the PDN resonances are extracted and compared. These examples show the influence of some of the parameters of the model on the global resonances of the system, in particular, the package and the die capacitance. Furthermore, each of the cases are tested in EMC laboratory against electrical fast transient events and a strong correlation between PDN resonances and FTB immunity is found. Indeed, the second configuration, the one showing resonances with the lowest amplitude and frequency is found to be the most robust with FTB threshold above 4.5kV. The effect of the package and on the PCB capacitance is also highlighted. Indeed, the smallest package with the a reduced number of supply pin is found to be more sensible to EMC perturbations which is aligned with the results found in the precedent thesis work [23].

General conclusion and perspectives

Nowadays, MCU are used in many applications covering a massive market. CMOS technology evolution allows to realize more complex ICs. Then EMC becomes a major issue for such devices or MCU. This work focuses on the IEC 61000-4-4 standards which was adapted to evaluate the robustness of a STM32 microcontroller against electrical fast transient events.

In the first chapter the DUT was introduced: the microcontroller. Indeed, this device is an excellent example as it is one of the most used integrated circuit in modern society, its application varies from consumer electronic to high-risk military or spatial applications. In these domains, the EMC robustness is a real concern as no system failure is tolerated. Throughout the entire first chapter, some fundamental EMC tests were explained such as electrostatic discharge, radiated emission and electrical fast transient events. The laboratory tests and protocols as well as some of the immunity solution were presented. Last section of the first chapter is dedicated to the introduction of the core concepts about the FTB. FTB stress is presented as a common mode perturbation propagating from the generator to the microcontroller power distribution network. FTB stress is converted in a differential stress on the supply by the asymmetry of the power distribution network either of the PCB, the package or the die. From this assumption, the hypothesis of analysing the resonance frequencies of the PDN and correlate them to FTB immunity was the starting point of this thesis work.

To accomplish that, a modelling flow and a measurement method had to be developed. This is the core of the second chapter. Indeed, taking a sample DUT configuration all the modelling steps which allows the generation of a SPICE RLC

electrical model were detailed. In particular, the PCB, the package and the die were considered. For each of these elements, the key parameters were presented; equations and calculations methods are explained. In the second part of the chapter, a review of the most important resonance analysis measurement bench was presented. The advantages and disadvantages of each bench were discussed and finally, a novel setup was presented.

In the third chapter, the tools developed in chapter 2 are employed to validate the initial hypothesis presented in chapter 1. To do that, a real STM32 microcontroller was taken as DUT. This microcontroller targeted a very precise market segment of low cost and mainstream devices. It was the first 32-bit microcontroller produced by STMicroelectronics to maximise the IO count at the expense of supply pair pins. Furthermore, at that time, it was the smallest microcontroller ever fabricated with only 4 mm^2. This microcontroller showed very low EMC performances with FTB threshold far below the minimum acceptable value. Using resonances knowledge and model, it was possible to identify the weaknesses of this product and to see the impact of some non-impacting silicon and package modification on the resonances of the system. Resonances were found to be a good indicator of FTB robustness and eventually, the second development cut showed impressive EMC performances. This product is today commercialised as being the best solution for critical EMC application. This entire study shows that playing with the global resonances of a DUT we can improve or deteriorate the EMC performances of whatever devices. Nevertheless, we still know very little about FTB mechanism failure. Today, we do not know why a certain level of resonances is critical for the microcontroller and what kind of electrical failure occurs. Indeed, a microcontroller is a very complex integrated circuit and billions of transistors are connected together to build thousand of different IP. Each of this transistor or interconnection could be the responsible of hard-fault failure. As said in chapter 1, any measure during FTB stress is not reliable as the common mode nature of the stress perturbs every electronic equipment in the laboratory.

Furthermore, today the build-in-self test architecture to cover CPU hard-faults is not developed enough to precise locate the weaknesses and probably will never do in general purpose IC. Nevertheless, working with some global aspects as resonances helps giving some EMC guideline to designer and marketing when ad-

dressing an application. Indeed, most of the design work for general purpose microcontroller is the re-use of existing solutions or architecture a few impacting modifications are done from a STM32 generation to the following. The knowledge acquired from this work has been taken into consideration for other STM32 developments and a specific FTB check has been inserted in the design flow which allowed a first silicon cut success (in term of EMC) for a particular STM32. On the other hand, the electrical model developed along with the measurement bench are a good predictive tool be able to evaluate different PCB configuration and allows rising red or green flags on some marketing choices. Figure 3.17 shows a typical

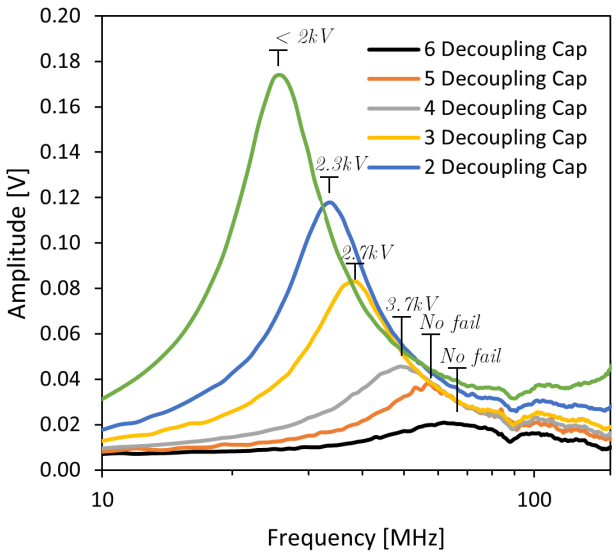


Figure 3.17: Decoupling capacitor number, resonances and FTB immunity.

application where guidelines about the minimum number of decoupling capacitor needed for a certain FTB immunity could be given or specified in the datasheet of the product. IEC 61000-4-4 was introduced as an electric equipment standard. Every final electronic equipment such as Personal computers, fridges, cars, trains and many more have to comply with this standard. The FTB immunity of these equipments is usually evaluated at the final stages of the design and it does not concerns the local robustness of individual microchips embedded but rather the total electric system. For that reason, today, most of the research on FTB issues is dedicated to system level solutions as common mode filter or shielding. Few stud-

ies propose analytical model and solution to improve susceptibility in integrated circuits and this study is among them. This research may be seen as a complement to all the studies done at high level system thinking that making all the ICs more robust would lead to a more robust electric equipment. Next steps would be to use the modelling methodology and measuring bench to investigate other solutions and to compare them in term of efficacy and cost. As said before, FTB research is still at the beginning and most of the standard protections are designed empirically and represent a huge cost in term of PCB development and components. The presented flow could be applied to evaluate classical FTB protection to see if some optimisation is possible to either improve immunity or decrease the cost.

Bibliography

[1] T. I. T. R. for Semiconductor, *More moore*, 2015.

[2] EU, "Directive 2014/30/eu of the european parliament and of the council on the harmonisation of the laws of the member states relating to electromagnetic compatibility," 2014.

[3] "Ce marking." (), [Online]. Available: `https://cemarking.net/basic-steps-ce-marking-process/`.

[4] A. Hardock, D. Dahl, H.-D. Brüns, and C. Schuster, "Efficient calculation of external fringing capacitances for physics-based pcb modeling," in *2015 IEEE 19th Workshop on Signal and Power Integrity (SPI)*, 2015, pp. 1–4. DOI: 10.1109/SaPIW.2015.7237396.

[5] O. Semenov, H. Sarbishaei, and M. Sachdev, *ESD Protection Device and Circuit Design for Advanced CMOS Technologies*. 2010.

[6] JEDEC, *Jesd78c*, 2010.

[7] M. Johnson, R. Cline, S. Ward, and J. Schichl, *Latch-up*, 2015.

[8] M.-D. Ker and H.-C. Jiang, "Whole-chip esd protection strategy for cmos integrated circuits in nanotechnology," in *Proceedings of the 2001 1st IEEE Conference on Nanotechnology. IEEE-NANO 2001 (Cat. No.01EX516)*, 2001, pp. 325–330. DOI: 10.1109/NANO.2001.966442.

[9] J. Shi, "Esd characteristics of ggnmos device in deep sub-micron cmos technology," in *2016 International Conference on Audio, Language and Image Processing (ICALIP)*, 2016, pp. 327–331. DOI: 10.1109/ICALIP.2016.7846533.

[10] M. Paul, C. Russ, B. S. Kumar, H. Gossner, and M. Shrivastava, "Physics of current filamentation in ggnmos devices under esd condition revisited," *IEEE Transactions on Electron Devices*, vol. 65, no. 7, pp. 2981–2989, 2018. DOI: 10.1109/TED.2018.2835831.

[11] K.-H. Oh, C. Duvvury, K. Banerjee, and R. Dutton, "Impact of gate-to-contact spacing on esd performance of salicided deep submicron nmos transistors," *IEEE Transactions on Electron Devices*, vol. 49, no. 12, pp. 2183–2192, 2002. DOI: 10.1109/TED.2002.803627.

[12] J.-H. Lee, J. Shih, D.-H. Yang, J. F. Chen, and K. Wu, "A novel esd device structure with fully silicide process for mixed high/low voltage operation," in *2008 15th International Symposium on the Physical and Failure Analysis of Integrated Circuits*, 2008, pp. 1–4. DOI: 10.1109/IPFA.2008.4588153.

[13] W. Wang, S. Dong, L. Zhong, J. Zeng, Z. Yu, and Z. Liu, "Ggnmos as esd protection in different nanometer cmos process," in *2014 IEEE International Conference on Electron Devices and Solid-State Circuits*, 2014, pp. 1–2. DOI: 10.1109/EDSSC.2014.7061085.

[14] M.-D. Ker, W.-Y. Chen, W.-T. Shieh, and I.-J. Wei, "New ballasting layout schemes to improve esd robustness of i/o buffers in fully silicided cmos process," *IEEE Transactions on Electron Devices*, vol. 56, no. 12, pp. 3149–3159, 2009. DOI: 10.1109/TED.2009.2031003.

[15] I. Compliance. "Transmission line pulse testing: The indispensable tool for esd characterization of devices, circuits and systems." (2017), [Online]. Available: https://incompliancemag.com/article/transmission-line-pulse-testing-the-indispensable-tool-for-esd-characterization-of-devices-circuits-and-systems/.

[16] R. Ma, L. Wang, C. Zhang, *et al.*, "Tlp and hbm esd test correlation for power ics," in *2013 IEEE International Conference of Electron Devices and Solid-state Circuits*, 2013, pp. 1–2. DOI: 10.1109/EDSSC.2013.6628149.

[17] IEC, "Circuits intégrés – mesure des émissions électromagnétiques, 150 khz à 1 ghz," 2002.

[18] J.-P. LECA, "Modélisation et réduction des émissions électromagnétiques dans les microcontrôleurs," PhD, Université de Nice-Sophia Antipolis, 2012.

[19] J.-P. Leca, N. Froidevaux, H. Braquet, and G. Jacquemod, "Emi modeling of a 32-bit microcontroller," in *2011 8th Workshop on Electromagnetic Compatibility of Integrated Circuits*, 2011, pp. 230–234.

[20] ——, "Emi modeling of a 32-bit microcontroller in wait mode," in *2010 IEEE International Behavioral Modeling and Simulation Workshop*, 2010, pp. 13–18. DOI: 10.1109/BMAS.2010.6156591.

[21] J. P. Leca, N. Froidevaux, P. Dupré, G. Jacquemod, and H. Braquet, "Emi measurements, modeling, and reduction of 32-bit high-performance microcontrollers," *IEEE Transactions on Electromagnetic Compatibility*, vol. 56, no. 5, pp. 1035–1044, 2014. DOI: 10.1109/TEMC.2014.2304744.

[22] I. 6.-4.-4. Standard, *Electromagnetic compatibility (emc) – part 4.4: Testing and measurement techniques – electrical fast transient/burst immunity test*, 2004.

[23] Y. BACHER, "Etude et modélisation des perturbations produites au sein des microcontrôleurs stm32 soumis à des stress en impulsion," PhD, Université de Nice-Sophia Antipolis, 2017.

[24] A. Kamath and B. Nayak, "Common mode filter design for burst type pulses," in *2016 International Conference on ElectroMagnetic Interference Compatibility (INCEMIC)*, 2016, pp. 1–4. DOI: 10.1109/INCEMIC.2016.7921521.

[25] Z. Zhou and Q. Jiang, "Analysis of the effectiveness of ferrite core for improving eft immunity," in *2002 3rd International Symposium on Electromagnetic Compatibility*, 2002, pp. 718–721. DOI: 10.1109/ELMAGC.2002.1177531.

[26] S. Gulhane and A. Ratnaparkhe, "Grounding technique for eft and surge test," in *2016 International Conference on ElectroMagnetic Interference Compatibility (INCEMIC)*, 2016, pp. 1–2. DOI: 10.1109/INCEMIC.2016.7921492.

[27] H. GAO, G. LUO, H. LIN, M. ZHAO, and Y. JU, "Modeling of small common-mode choke for eft interference suppression at analog input port," in *2019 12th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2019, pp. 228–230. DOI: 10.1109/EMCCompo.2019.8919724.

[28] L. Quazzo, Y. Bacher, N. Froidevaux, H. Braquet, and G. Jacquemod, "Resonance analysis methods for estimation of ftb propagation in integrated circuits," in *2018 IEEE Radio and Antenna Days of the Indian Ocean (RADIO)*, 2018, pp. 1–4. DOI: 10.23919/RADIO.2018.8572449.

[29] Y. Bacher, L. Quazzo, H. Braquet, N. Froidevaux, and G. Jacquemod, "Novel measurement set-ups of ftb stress propagation in an ic," in *2018 Progress in Electromagnetics Research Symposium (PIERS-Toyama)*, 2018, pp. 513–519. DOI: 10.23919/PIERS.2018.8598206.

[30] Y. Bacher, N. Froidevaux, P. Dupre, H. Braquet, and G. Jacquemod, "Resonance analysis for emc improvement in integrated circuits," in *2015 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2015, pp. 56–60. DOI: 10.1109/EMCCompo.2015.7358330.

[31] Murata. "Grm033c80j104ke15 characteristic data." (2022), [Online]. Available: https://www.murata.com/en-global/products/productdetail?partno=GRM033C80J104KE15%23.

[32] C. Holloway and E. Kuester, "Net and partial inductance of a microstrip ground plane," *IEEE Transactions on Electromagnetic Compatibility*, vol. 40, no. 1, pp. 33–46, 1998. DOI: 10.1109/15.659518.

[33] C. L. Holloway, E. F. Kuester, A. E. Ruehli, and G. Antonini, "Partial and internal inductance: Two of clayton r. paul's many passions," *IEEE Transactions on Electromagnetic Compatibility*, vol. 55, no. 4, pp. 600–613, 2013. DOI: 10.1109/TEMC.2013.2253470.

[34] F. Leferink, "Inductance calculations; methods and equations," in *Proceedings of International Symposium on Electromagnetic Compatibility*, 1995, pp. 16–22. DOI: 10.1109/ISEMC.1995.523511.

[35] A. Ruehli, C. Paul, and J. Garrett, "Inductance calculations using partial inductances and macromodels," in *Proceedings of International Symposium on Electromagnetic Compatibility*, 1995, pp. 23–28. DOI: 10.1109/ISEMC.1995.523512.

[36] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM Journal of Research and Development*, vol. 16, no. 5, pp. 470–481, 1972. DOI: 10.1147/rd.165.0470.

[37] E. B. Rosa, "The international electrical units 1893–1910," *Proceedings of the American Institute of Electrical Engineers*, vol. 29, no. 7, pp. 1325–1334, 1910. DOI: 10.1109/PAIEE.1910.6659900.

[38] C. R. Paul, *Inductance: Loop and Partial*. 2010.

[39] C. Hoer and C. Love, "Exact inductance equations for rectangular conductors with applications to more complicated geometrie," in *JOURNAL OF RESEARCH of the National Bureau of Standard*, vol. 69C, 1965.

[40] M. MOIGN, J.-P. LECA, N. Froidevaux, Y. LEDUC, and G. JACQUEMOD, "Effect of ssn on signal and power integrity on 32-bit microcontroller : Modeling and correlation," in *2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, 2019, pp. 193–196. DOI: 10.1109/PRIME.2019.8787742.

[41] H. B. Dwight, "Skin effect in tubular and flat conductors," *Transactions of the American Institute of Electrical Engineers*, vol. XXXVII, no. 2, pp. 1379–1403, 1918. DOI: 10.1109/T-AIEE.1918.4765575.

[42] H. Wheeler, "Formulas for the skin effect," *Proceedings of the IRE*, vol. 30, no. 9, pp. 412–424, 1942. DOI: 10.1109/JRPROC.1942.232015.

[43] C. R. Paul, *Analysis of multiconductor transmission lines*. 2008.

[44] Ansys. "Q3d exctractor multiphysics parasitic extraction & analysis." (), [Online]. Available: https://www.ansys.com/products/electronics/ansys-q3d-extractor.

[45] S. Sze and K. K. NG, *Physics of semiconductor devices*. 2006.

[46] T. LeCroy, *Ap033 active differential probe*, 2017.

Appendix A

Publications

1. Y. Bacher, L. Quazzo, N. Froidevaux, H. Braquet and G. Jacquemod, "Near field measurement bench and on-chip sensor for FTB stress propagation analysis," 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Bordeaux, 2018, pp. 285-288, doi: 10.1109/ICECS.2018.8618040

2. L. Quazzo, Y. Bacher, N. Froidevaux, H. Braquet and G. Jacquemod, "Resonance Analysis Methods for Estimation of FTB Propagation in Integrated Circuits," 2018 IEEE Radio and Antenna Days of the Indian Ocean (RADIO), Mauritius Island, 2018, pp. 1-4, doi: 10.23919/RADIO.2018.8572449

3. Y. Bacher, L. Quazzo, H. Braquet, N. Froidevaux and G. Jacquemod, "Novel Measurement Set-Ups of FTB Stress Propagation in an IC," 2018 Progress in Electromagnetics Research Symposium (PIERS-Toyama), 2018, pp. 513-519, doi: 10.23919/PIERS.2018.8598206

4. L. Quazzo, Y. Bacher, N. Froidevaux, H. Braquet and G. Jacquemod, "Analysis of FTB stress propagation in an Integrated Circuit," 2019 15th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Lausanne (Switzerland), 2019, pp. 185-188, doi: 10.1109/PRIME.2019.8787823

5. L. Quazzo, N. Froidevaux, H. Braquet and G. Jacquemod, "PDN Resonance Frequencies and FTB Robustness Correlation," 2019 12th International Workshop on the Electromagnetic Compatibility of Integrated Cir-

cuits (EMC Compo),Haining (China) 2019, pp. 37-39, doi: 10.1109/EMC-Compo.2019.8919757

6. L. Quazzo, Y.Bacher, H. Braquet, N. Froidevaux and G.Jacquemod, "STM32 microcontroller FTB susceptibility and modeling", RF and Microwave, Paris, 2019

7. L. Quazzo, Y.Bacher, H. Braquet, N. Froidevaux and G.Jacquemod, "Nouvelles méthodes d'analyse et de mesure de la propagation du stress FTB dans un circuit intégré", JNM, Caen, 2019

8. L. Quazzo, N. Froidevaux, G. Jacquemod and H. Braquet, "Amélioration de la robustesse des mircocontrôleurs STM32 soumis à un stress FTB en impulsion par contrôle de leur réponse", JNRDM, Montpellier, 2019

Electromagnetic compatibility (EMC) is one of the key aspects of modern technology where different electric devices are used together to build an electronic application. In this context, the compliance of a device to EMC standards reduces the chance of critical failures improving the reliability of electronic products. EMC embraces all different kind of domains and it applies to various devices from large electric installations to portable devices or to integrated circuits (IC). This work focuses on EMC susceptibility for microcontrollers, that is the ability of a microcontroller to work correctly in a disturbed electromagnetic environment. Microcontrollers are employed in many different applications requiring different levels of immunity for different kind of stresses. This research work studies the susceptibility of standard STM32 microcontrollers against electrical fast transient events as defined by IEC 61000-4-4 standard for Fast Transient Burst (FTB). FTB test consists of injecting high voltage and repetitive spikes on the supply of the electronic devices. Studying the device behavior under stress condition and analyzing the failure mechanisms give important hints related to its immunity threshold. Some high-level system strategies have been proposed to improve the robustness of an electronic equipment to electrical fast events but few studies are dedicated to ICs or packages protection solutions. This works starts from the hypotheses of the resonances of the power distribution network (PDN) of the microcontroller being correlated with FTB immunity thresholds. As a consequence, some modelling and measuring techniques are presented to find the resonances in a specific Device Under Test (or DUT) composed of a Printed Circuit Board (PCB), a die package and a silicon die. Finally, the methodology is applied to some DUT configurations to show the correlation between the resonance characteristics of the PDN and the FTB immunity levels. This work opens up the possibility of using resonance analysis in the study of the influence of different design choices on EMC susceptibility such as package and die size and thus it gives a interesting predictive tool to be used during the design phase of a microcontroller.

Keywords : EMC, EMS, FTB, EFT, IEC 61000-4-4, Power distribution network, Resonance, Microcontroller

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La compatibilité électromagnétique (CEM) est l'un des aspects clés de la technologie moderne où différents appareils électriques sont utilisés ensemble pour créer une application électronique. Dans ce contexte, la conformité d'un appareil aux normes CEM réduit le risque de défaillances critiques améliorant la fiabilité des produits électroniques. La CEM englobe tous les types de domaines et s'applique à divers appareils, des grandes installations électriques aux appareils portables ou aux circuits intégrés (IC). Ce travail porte sur la susceptibilité électromagnétique des microcontrôleurs, c'est-à-dire la capacité d'un microcontrôleur à fonctionner correctement dans un environnement électromagnétique perturbé. Les microcontrôleurs sont utilisés dans de nombreuses applications différentes nécessitant différents niveaux d'immunité pour différentes typologies de perturbations. Ce travail de recherche étudie la susceptibilité des microcontrôleurs standard STM32 aux événements électriques transitoires rapides tels que définis par la norme IEC 61000-4-4 en introduisant le Fast Transient Burst (FTB) test. Le test FTB consiste à injecter des trains d'impulsions haute tension sur l'alimentation des appareils électroniques. L'étude du comportement du dispositif et l'analyse des mécanismes de défaillance donnent des indications importantes sur son seuil d'immunité. Certaines stratégies système de haut niveau ont été proposées pour améliorer la robustesse d'un équipement électronique aux perturbations électriques rapides mais peu d'études sont consacrées aux solutions de protection dans les circuits intégrés ou dans les boîtiers. Ce travail part des hypothèses de résonances du réseau de distribution d'énergie (PDN) du microcontrôleur étant corrélées avec des seuils d'immunité FTB. En conséquence, certaines techniques de modélisation et de mesure sont présentées pour trouver les résonances dans un dispositif sous test (ou DUT) spécifique composé d'une carte de circuit imprimé (PCB), d'un boîtier et d'une puce en silicium. Enfin, la méthodologie est appliquée à certaines configurations de DUT pour montrer la corrélation entre les caractéristiques de résonance du PDN et les niveaux d'immunité FTB. Ce travail ouvre la possibilité d'utiliser l'analyse de résonance dans l'étude de l'influence de différents choix de conception sur la susceptibilité CEM tels que la taille du boîtier et de la puce et donne ainsi un outil prédictif intéressant à utiliser pendant la phase de conception d'un microcontrôleur.

Keywords : EMC, EMS, FTB, EFT, IEC 61000-4-4, Resonance, Microcontrolleur