High-efficiency Si solar cell including tunnel junction for tandem photovoltaic cells

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Abstract

2-terminal (2T) crystalline silicon (c-Si) based tandem solar cell is an approach to overcome the Shockley-Queisser efficiency limit of single-junction solar cells. The objective of this thesis is to fabricate a low-resistance c-Si tunnel junction and implement it as the interconnection in 2T Si-based tandem solar cells. The proximity rapid thermal diffusion technique is applied in this work to fabricate the Si tunnel junctions with a damage-free surface. The fabrication and characterization of p^{++}/n^{++} tunnel junction on (111)-oriented Si wafer are presented. Several parameters of the tunnel junction fabrication process are investigated. The adjustment of the n^{++} emitter by a two-step rapid thermal annealing has effectively facilitated the fabrication of the p^{++}/n^{++} tunnel junction. Si tunnel diodes have been fabricated to characterize the electrical properties of tunnel junctions. The peak current density of the tunnel diodes is within the range of 140-192 A/cm^2 with a peak to valley current ratio of 1.9-3.2. Afterwards, the p^{++}/n^{++} tunnel junction was implemented in III-V nanowires/Si tandem solar cells. Despite the defectuosity of the nanowires array, an increase of the open-circuit voltage was observed in tandem solar cells in comparison with that of sole single-junction Si solar cells. The fabricated tunnel junctions can be integrated with other top cell materials such as perovskites and copper indium gallium selenide. The application of Si tunnel junctions obtained by proximity rapid thermal diffusion will improve the development of competitive high-efficiency c-Si based tandem solar cells.

Keywords: Si tunnel junction, proximity rapid thermal diffusion, tandem solar cell

Résumé

La cellule photovoltaïque tandem à base de silicium cristallin (c-Si) avec 2 terminaux (2T) est une solution permettant de dépasser la limite de Shockley-Queisser. L'objectif de ce travail de thèse est de réaliser une jonction tunnel en c-Si présentant une résistance faible afin de l'intégrer comme interconnexion des 2 sous-cellules constitutives de la tandem. La technique de diffusion thermique rapide par proximité est appliquée pour fabriquer les jonctions tunnel en silicium en minimisant les dommages causés à la surface du SIlicium. La fabrication et la caractérisation de la jonction tunnel p^{++}/n^{++} sur un substrat de silicium orienté (111) sont présentées. Plusieurs paramètres du processus de fabrication de la jonction tunnel sont étudiés. L'ajustement de l'émetteur n^{++} par un recuit thermique rapide en deux étapes a effectivement facilité la réalisation de la jonction tunnel p^{++}/n^{++}. Des diodes tunnel en silicium ont été fabriquées pour caractériser les propriétés électriques des jonctions tunnel. Le pic de densité de courant des diodes tunnel se situe entre les valeurs 140 et 192 A/cm^2 avec un ratio de courant de pic à vallée de 1,9 à 3,2. Par la suite, cette jonction tunnel p^{++}/n^{++} a été intégrée dans des cellules photovoltaïques tandem nanofils III-V/Si. Malgré la défectuosité des réseaux de nanofils, une augmentation de la tension de circuit ouvert a été observée dans les cellules photovoltaques tandem par comparaison avec celle de la cellule solaire à simple jonction. Ce type de jonction tunnel peut également être intégré à d'autres types de cellules en dessus, par exemple les pérovskites ou le CIGS. L'application de jonctions tunnel en Si obtenues par la technique de diffusion thermique rapide à proximité pourrait faciliter le développement de cellules photovoltaïques tandem compétitives à haut rendement à base de c-Si.

Mots-clés: jonction tunnel en silicium, diffusion thermique rapide par proximité, cellule photovoltaïque tandem

Contents

List of Abbreviations

Abbreviation	Description
a-Si	amorphous silicon
AM	airmass
BCB	benzocyclobutene
CIGS	copper indium gallium selenide
CVD	chemical vapor deposition
EQE	external quantum efficiency
HF	hydrofluoric acid
HSQ	hydrogen silsesquioxane
IBC	interdigitated back contact
IQE	internal quantum efficiency
ITO	indium tin oxide
LPCVD	low pressure chemical vapor deposition
LYDOP	Leaktight Yield Doping
MBE	molecular beam epitaxy
MOCVD	metal-organic chemical vapor deposition
mono-Si	monocrystalline silicon
NW	nanowire
PECVD	plasma-enhanced chemical vapor deposition
PERC	Passivated Emitter and Rear Cell
poly-Si	polycrystalline silicon
PRTD	proximity rapid thermal diffusion
RIE	reactive ion etching
rpm	revolutions per minute
RTA	rapid thermal annealing
RTD	rapid thermal diffusion
SA	selective area
SHJ	silicon heterojunction
SMU	source measure unit

SQ limit	Shockley-Queisser limit
TCA	transparent conductive adhesives
TCO	transparent conductive oxides
TLM	transfer length method
VLS	vapor-liquid-solid
µc-Si	microcrystalline silicon

Chapter 1 Introduction of photovoltaics and silicon-based tandem solar cells

1.1 Photovoltaic cells

1.1.1 Introduction of photovoltaic cells

1.1.1.1 Brief history of photovoltaic cells

The photovoltaic effect was first discovered by the French physicist Alexandre Edmond Becquerel in 1839 [1]. He placed two coated platinum electrodes in an electrolyte solution and found that voltage and current were generated once the electrodes were illuminated. In 1877, Englishmen William Adams and Richard Day demonstrated that it was possible to generate current in semiconductor selenium merely by light [2]. This led to the first thin-film selenium solar module fabricated by an American inventor Charles Edgar Fritts in 1883 [3].

The first p-n junction silicon solar cell with an efficiency of up to 6% was invented in 1954 [4]. In the following years, the efficiency was raised to 10%. Gallium arsenide (GaAs) and other alternative materials for solar cells were also presented apart from silicon. But the solar modules were only used for specific applications such as spacecraft because of the high cost until the early 1970s. Driven by the oil crisis in the 1970s, the public interest in solar cells for terrestrial application increased in that decade. Many companies started to develop photovoltaic modules and systems for terrestrial applications [5].

1.1.1.2 State of the art of photovoltaic cells

Nowadays, plenty of solar cells have been invented. The most two common types are crystalline solar cells and thin-film solar cells.

Crystalline solar cells are the most widespread application in the photovoltaic field. They are wafer cells made from crystalline silicon or III-V semiconductors. Several technologies were developed for producing higher efficiency crystalline silicon solar cells, such as PERC (Passivated Emitter and Rear cell), IBC (interdigitated back contact) solar cell, and SHJ (silicon heterojunction) solar cell. Crystalline silicon is either monocrystalline silicon (mono-Si) or polycrystalline silicon (poly-Si). The reported efficiency record for a mono-Si solar cell is now 25%, obtained with a PERC solar cell [6]. The highest efficiency of the mc-Si solar cell is 24.4%, lower than mono-Si [7]. But the cost of mc-Si solar cells is normally less than that of the mono-Si solar cells. Thanks to the abundance of silicon element and mature fabrication technologies, Si-based solar cell has been commercialized and dominant in the photovoltaic field till now. III-

V semiconductor wafers can also be used to fabricate solar cells with high efficiency. They are mainly employed for space applications and concentrator photovoltaics due to the high cost of materials [5].

Thin-film solar cells are made from films that are much thinner than wafers, thus requiring a little amount of material, due to higher absorption coefficient, and processed at a lower temperature than c-Si. In contrast to wafer-based solar cells, thin-film solar cells need a carrier to give them mechanical stability. Glass, stainless steel, or polymer foils are usually used as carrier materials, indicating that it is possible to produce flexible thin-film solar cells. In addition to being used in the wafer cells, silicon and III-V semiconductor materials can also be deposited to make thin-film solar cells. Silicon is used in two forms, amorphous silicon (a-Si) and microcrystalline silicon (µc-Si). Chalcogenide solar cells are another kind of thin-film solar cell, with CIGS (copper indium gallium selenide) and CdTe (cadmium telluride) solar cells as typical. The efficiency of the CIGS solar cell can reach 23.35% at present [8]. Besides the inorganic solar cells, organic solar cells and hybrid organic-inorganic solar cells are also researched. Perovskite solar cells and dye-sensitized solar cells are two typical hybrid organic-inorganic solar cells that attract a lot of attention. So far, the highest efficiency of perovskite solar cells is 22.6%, while that of dye-sensitized solar cells is 11.9% [9], [10]. Thin-film solar cells were expected to become much cheaper than wafer-based solar cells. However, due to the current price decline in silicon wafers, thin-film solar cells are not yet comparable to crystalline solar cells in commercial use.

In addition to the crystalline and thin-film solar cells, many advanced emerging technologies have appeared to fabricate high-efficiency solar cells that can overcome the efficiency limit for single-junction solar cells. These technologies include multijunction solar cells, concentrator photovoltaics, quantum dots solar cells, intermediate band solar cells, spectral up and down-conversion, multi-exciton generation, and hot carrier solar cells. Most of them are still in the fundamental research phase and it will take time to be implemented in PV modules. However, tandem cells, especially c-Si based tandem cells, are expected to be mass produced around 2023 [11].

1.1.2 Physics of p-n junction solar cell

1.1.2.1 Solar radiation

Solar radiation is the basis of photovoltaic cells. The sun is a gigantic nuclear fusion

reactor where hydrogen atoms are converted to helium atoms and generates tremendous energy. The temperature at the core of the sun is about 15 million degrees Celsius. The generated energy is released into space in the form of radiation. The total power of the radiation is about 3.8×10^{26} W. Only a small fraction of the radiation, 1.7×10^{18} W, reaches the earth [5]. The received power density or irradiance on the earth is calculated to be 1357 W/m^2, named as the solar constant. It is the irradiance outside the earth's atmosphere. The carrier of radiant solar energy is the photon. Solar cells absorb photons of appropriate energy and convert them into electrical energy. Therefore, it is important to know the spectral distribution of solar radiation.

According to Planck's law of radiation, the surface temperature determines the spectrum of the radiation. The surface temperature of the sun is 5778 K and thus leads to the idealized black-body radiation spectrum shown in Figure 1.1. The solar spectrum measured outside the earth's atmosphere is approximate to the idealized line. AM0 stands for the Air Mass 0, meaning that the sunlight has not passed through the atmosphere. The Air Mass coefficient is the ratio of the path length of sunlight when passing through the atmosphere to the shortest path length of the sunlight when the sun is at the zenith. It is given as:

$$\mathrm{AM} = \frac{L}{L_0} = \frac{1}{\cos\theta} \tag{1.1}$$

with L is the actual path length of the sunlight, L_0 is the shortest path length of the sunlight, θ is the zenith angle.

Due to the reflection, absorption, and scattering, the solar irradiance is reduced after passing through the atmosphere. The real solar spectrum changes with the path length of the sunlight. The Air Mass coefficient characterizes the effect of path length on the reduction of solar irradiance. Therefore, the spectrum outside the atmosphere is designated by AM0. When the sun is at its zenith, the spectrum is called AM1. The standard spectrum for characterizing terrestrial solar cells is AM1.5 when the zenith angle is 48°.

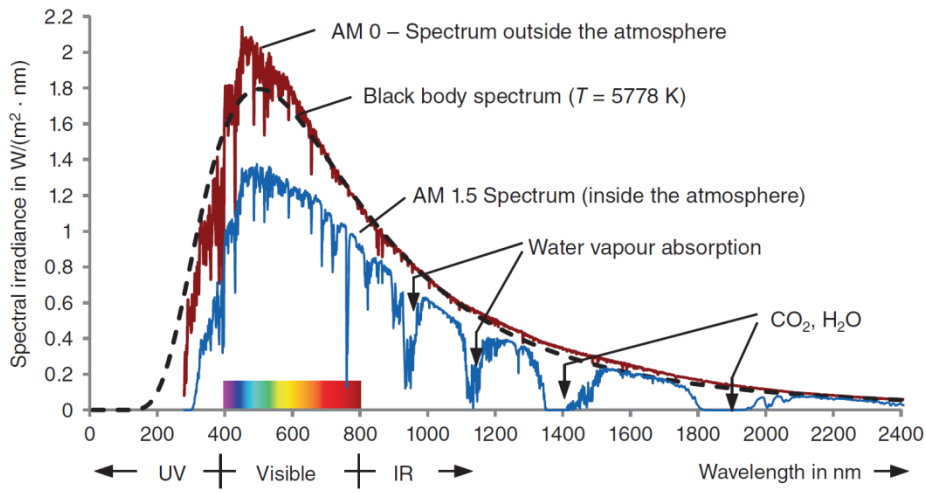


Figure 1.1 *Spectrum outside and inside the atmosphere [12].*

1.1.2.2 Carrier generation and recombination

When a semiconductor is illuminated, it absorbs the photons with energy equal to or greater than its bandgap. As a result, electrons from the valence band are excited to the conduction band and corresponding holes are produced in the valence band. This process is the generation of electron-hole pairs. In the doped semiconductors, the absorption of photons increases the number of both majority and minority carriers. The number of light-generated carriers is less than the number of existing majority carriers due to doping. Oppositely, the amount of the light-generated carriers is more than the existing minority carriers. Therefore, the light-generated carriers significantly impact the minority carriers.

Recombination is an unavoidable process in the semiconductor that is reverse to the generation. Electrons and holes are annihilated in this process. Generally, there are three types of recombination, radiative recombination, trap-assisted recombination, and Auger recombination.

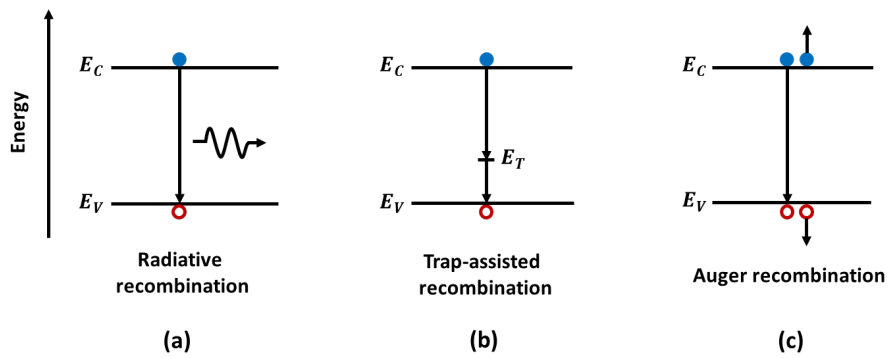


Figure 1.2 *Recombination mechanisms in semiconductors: (a) radiative recombination, (b) trap-assisted recombination, and (c) Auger recombination.*

Radiative recombination, also known as band-to-band recombination, is a spontaneous transition process in which an electron from the conduction band migrates to an unoccupied state in the valence band and releases a photon. It is the dominant recombination process in direct bandgap semiconductors.

Trap-assisted recombination is usually called Shockley-Read-Hall recombination or SRH recombination. It is a non-radiative process facilitated by impurities or lattice defects. These recombination centers introduce allowed energy levels called trap states within the forbidden gap. An electron can be trapped at this kind of state and consequently recombines with a hole that is attracted by the trapped electron. It is a non-radiative process and the excess energy is dissipated into the lattice in the form of heat. Trap-assisted recombination at the surface of a semiconductor is known as surface recombination. The dangling bonds caused by the discontinuation of the crystal lattice promote recombination. In solar cells, surface passivation can reduce the dangling bonds, thereby reducing the surface recombination.

Auger recombination is also a non-radiative recombination mechanism. It is a three particles process. The energy and momentum of the recombining electron and hole are transferred to a third carrier, rather than emitting the energy as heat or as a photon. Then the third carrier losses its excess energy in the form of heat. Auger recombination dominates in silicon and other indirect bandgap materials.

The generation and recombination of electron-hole pairs are crucial to the conversion efficiency of solar cells. Various technologies have been developed to enhance the carrier generation as well as weaken the carrier recombination to increase efficiency.

1.1.2.3 Working principle of p-n junction solar cell

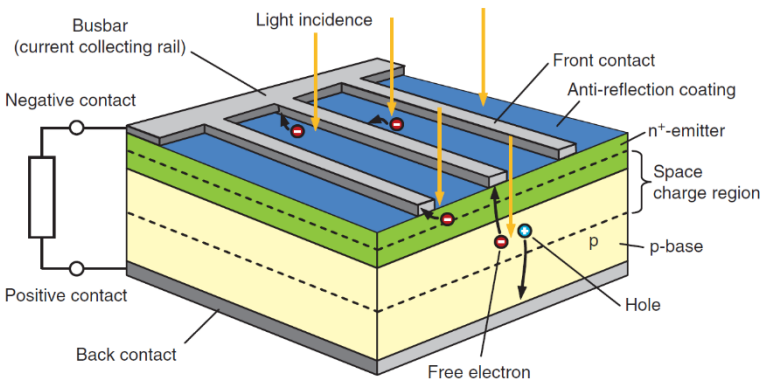


Figure 1.3 *Configuration of a typical silicon solar cell [12].*

The configuration of a conventional p-n junction solar cell is shown in Figure 1.3. It basically consists of a p-n junction diode. When the solar cell is illuminated, penetrating photons with energy equal to or greater than the bandgap are absorbed and generate free electron-hole pairs. The generated electrons and holes in the depletion region are immediately separated by the built-in electric field [13]. Then electrons migrate to the n-side and holes migrate to the p-side, causing a current flowing from n-side to p-side in the depletion region. This current is called photocurrent I_L. As a result, the potential on the n-side decreases and the potential on the p-side increases. Thus, a potential difference appears, and this phenomenon is called the photovoltaic effect. An ideal solar cell can be modeled by a current source I_L in parallel with a passive diode [12]. If the solar cell is connected to the load, a current will flow through the load due to the existence of potential difference.

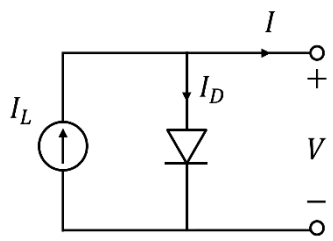


Figure 1.4 *Equivalent circuit of an ideal solar cell.*

Not all the light-generated electron-hole pairs contribute to the photocurrent. The photocurrent is determined by the migration of minority carriers in the depletion region. Most of the minority carriers generated in the electrical neutral region recombine before reaching the depletion region. Only a portion of them generated within the diffusion length can diffuse to the depletion before recombining and swept by the electric field to their respective majority carrier side of the junction. Generally, the diffusion length of electrons in the p-type semiconductor is higher than that of holes in the n-type with the same doping concentration. Hence, the electrons can be collected more effectively than holes outside the depletion region.

Besides, the amount of the photocurrent depends on the number of photons that are absorbed by the solar cell. The penetration depth of the photons in the solar cell should also be considered. Therefore, the p-n junction of the solar cell is normally asymmetrically doped, containing a thin highly doped n-type emitter on the illuminated side and a moderately p-type doped base on the rare side.

1.1.2.4 Characteristics of solar cell

1.1.2.4.1 *I-V* characteristics

When the solar cell is connected to the external load, the relation curve between the current through the load and the voltage across the load is the current-voltage (*I-V*) characteristic of the solar cell (Figure 1.5).

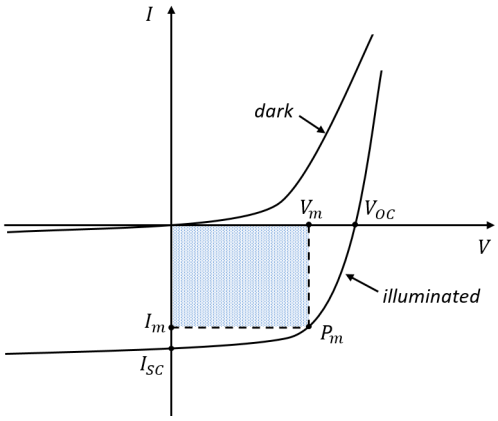


Figure 1.5 *Current-voltage characteristics curves of a solar cell in the dark and illumination conditions.*

In the dark condition, there is no photocurrent generated and the solar cell behaves like a normal p-n junction diode. Its behavior follows the Shockley equation when a voltage U is applied,

$$I_{dark} = I_s\left[\exp\left(\frac{qU}{nk_0T}\right) - 1\right]. \tag{1.2}$$

Here $I_s = Aq(\frac{D_n n_{p0}}{L_n} + \frac{D_p p_{n0}}{L_p})$, represents the reverse saturation current. A is the solar cell area, D_n and D_p are diffusion coefficient of the electron, hole respectively, $L_n$and L_p are diffusion length of the electron, hole respectively, n_{p0} is the electron concentration in a p-type material at thermodynamic equilibrium, p_{n0} is the hole concentration in an n-type material at thermodynamic equilibrium, n is the ideality factor of the diode and it equals to 1 for ideal diodes.

When the solar cell is under illumination, the output voltage V causes a current I_D flow through the diode, which is given by

$$I_D = I_s\left[\exp\left(\frac{qV}{k_0T}\right) - 1\right]. \tag{1.3}$$

The direction of I_D is opposite to the direction of I_L. Therefore, the output current is

$$I = I_L - I_D = I_L - I_s\left[\exp\left(\frac{qV}{k_0T}\right) - 1\right]. \tag{1.4}$$

(1) Short-circuit current I_{sc}

When the solar cell is short-circuited at its connections, the output current is the short-circuit current I_{sc}. $I_D = 0$ in this condition, thus

$$I_{sc} = I_L. \tag{1.5}$$

It means that the short-circuit current I_{sc} is equal to the photocurrent I_L in an ideal solar cell. The short-circuit current strongly depends on the optical properties of the solar cell, such as the absorption and reflection of sunlight.

(2) Open-circuit voltage V_{oc}

According to the equation Eq.(1.4), the output voltage V is calculated as

$$V = \frac{k_0T}{q}\ln\left(\frac{I_L - I}{I_s} + 1\right). \tag{1.6}$$

The open-circuit voltage V_{oc} is the output voltage when the load is infinite. In this case, $I = 0$, so that

$$V_{oc} = \frac{k_0T}{q}\ln\left(\frac{I_L}{I_s} + 1\right) = \frac{k_0T}{q}\ln\left(\frac{I_{sc}}{I_s} + 1\right). \tag{1.7}$$

V_{oc} is the maximum output voltage of an ideal solar cell. It mainly depends on the reverse saturation current and photocurrent. Since the reverse saturation current is determined by the recombination, V_{oc} reflects the amount of recombination in the solar cell.

(3) Maximum output power P_m

The output power P of a solar cell is the product of output voltage and output current, varying with the load:

$$P = V \cdot I = VI_L - VI_s\left[\exp\left(\frac{qV}{k_0T}\right) - 1\right]. \tag{1.8}$$

When the load changes, there is a point that makes the output power is maximum,

$$P_m = V_m \cdot I_m. \tag{1.9}$$

This point is called maximum power point. It is the optimal operating point of a solar cell. The corresponding V_m and I_m are respectively called maximum power point voltage and maximum

power point current.

(4) Fill factor FF

The fill factor FF is the ratio of the maximum output power to the product of V_{oc} and I_{sc} when the solar cell works under the optimal operating condition:

$$FF = \frac{P_m}{V_{oc} \cdot I_{sc}} = \frac{V_m \cdot I_m}{V_{oc} \cdot I_{sc}}. \tag{1.10}$$

It is an important parameter that reveals the quality of a solar cell. Typical values for efficient silicon solar cells are between 0.75 and 0.85 [12].

(5) Conversion efficiency η

The conversion efficiency η describes the proportion of the incident optical energy that can be converted into electrical energy. It is given by

$$\eta = \frac{P_m}{P_{in}} = \frac{FF \cdot V_{oc} \cdot I_{sc}}{P_{in}} \tag{1.11}$$

where P_{in} is the incident power. It is often used to compare the performance of one solar cell with another. Considering that it is relevant to the incident light, the measurement conditions should be carefully controlled.

In reality, no solar cell is ideal so that the series resistance R_S, shunt resistance R_{Sh} and ideality factor n should also be considered. The equivalent circuit of a standard solar cell is shown in Figure 1.6.

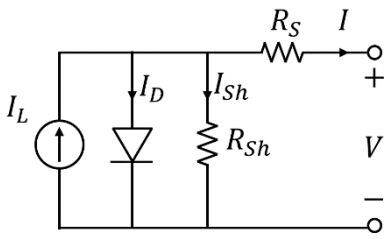


Figure 1.6 *Equivalent circuit of a standard solar cell.*

The series resistance R_S consists of the resistance of the semiconductor material, contact resistance at the metal-semiconductor interface, and the resistance of the metal contacts. It leads to the reduction of the output voltage V. The current flows through the diode I_D is shown as:

$$I_D = I_s\left[\exp\left(\frac{q(V + I \cdot R_S)}{k_0 T}\right) - 1\right]. \tag{1.12}$$

The shunt resistance R_{Sh} is caused by the leak current. Generally, the leak current contains the leak current at the edge of the solar cell as well as the internal leak current caused by crystal defects and impurities in the p-n junction. Low R_{Sh} provides an alternative path for the photocurrent:

$$I_{Sh} = \frac{V + I \cdot R_S}{R_{Sh}}. \tag{1.13}$$

The ideality factor n shows how much the properties of a diode resemble the ideal diode properties. For an ideal solar cell $n = 1$, but for real solar cells, n varies from 1 to 2. Hence,

$$I_D = I_s\left[\exp\left(\frac{q(V + I \cdot R_S)}{n k_0 T}\right) - 1\right]. \tag{1.14}$$

As a consequence, the current-voltage characteristics of the solar cell is modified as

$$I = I_L - I_s\left[\exp\left(\frac{q(V + I \cdot R_S)}{n k_0 T}\right) - 1\right] - \frac{V + I \cdot R_S}{R_{Sh}}. \tag{1.15}$$

1.1.2.4.2 Quantum efficiency

The Quantum efficiency of the solar cell indicates the amount of electron-hole pairs produced by incident photons with a certain wavelength. It reflects the contribution of photons with different energies to the short circuit current. There are two types of quantum efficiency: external quantum efficiency and internal quantum efficiency.

External quantum efficiency (EQE) is the ratio of the number of electron-hole pairs usable for the photocurrent to the number of incident photons with a certain wavelength.

$$\mathrm{EQE} = \frac{I_{sc}(\lambda)}{q\phi(\lambda)}, \tag{1.16}$$

where q is the elementary charge and $\phi(\lambda)$is the incident photon flow with wavelength λ.

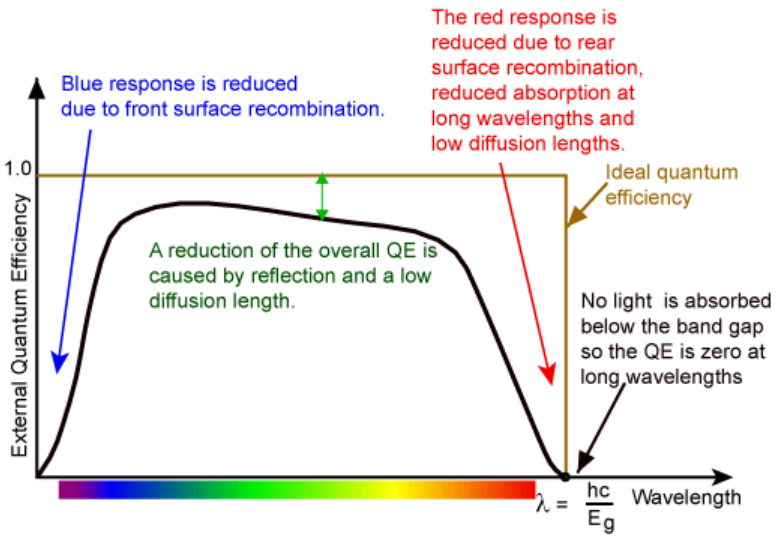


Figure 1.7 *External quantum efficiency of a silicon solar cell [14].*

Internal quantum efficiency (IQE) is the ratio of the number of usable electron-hole pairs to the number of absorbed photons with a certain wavelength. In this case, the losses caused by reflection and transmission are considered. IQE is given by

$$\mathrm{IQE} = \frac{\mathrm{EQE}}{1 - \mathrm{reflection} - \mathrm{transmission}}. \tag{1.17}$$

1.1.2.5 Efficiency limit of single-junction solar cell

The conversion efficiency of single-junction solar cells can never reach 100% due to many factors. There are three principal loss processes in the single-junction solar cell: transmission losses, thermalization losses, and radiative recombination.

Transmission losses and thermalization losses are caused by the spectral mismatch between the energy distribution of photons in the solar spectrum and the bandgap of the semiconductor material. Photons with energy lower than the bandgap cannot be absorbed, thus no electron-hole pairs are generated by this portion of the solar spectrum. Photons with energy greater than the bandgap can generate electron-hole pairs and the excess energy is released to crystal lattice in the thermalization process. Figure 1.8 shows the losses due to spectral mismatch in an ideal Si solar cell. Thermalization losses and transmission losses can be avoided by emerging high-efficiency solar cells approaches, such as multijunction solar cells, intermediate solar cells, multi-exciton generation, and so on. Losses due to radiative recombination are fundamental and cannot be avoided.

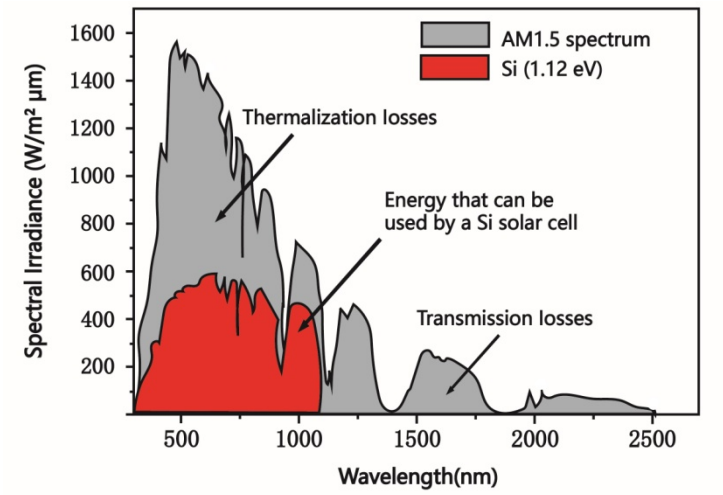


Figure 1.8 *Spectral losses in an ideal crystalline Si solar cell [15].*

The ultimate theoretical efficiency limit of single-junction solar cells was calculated by Shockley and Queisser in 1961 [16]. They proposed a detailed balance limit based on several assumptions. First, all photons with energy greater than the bandgap are absorbed; each of them produces an electron-hole pair. Second, the mobility of carriers is infinite in the material, such that the separation of the quasi-Fermi levels throughout the entire device is equal. Third, there is no other loss mechanism in the solar cell except for the radiative recombination. Fourth, the sun and the solar cell are assumed to be blackbodies with a temperature of 6000 K and 300 K respectively. Besides, the solar cell is illuminated by non-concentrated sunlight. As a consequence, the dependence of the ultimate efficiency upon the bandgap of the semiconductor is demonstrated (as shown in Figure 1.9).

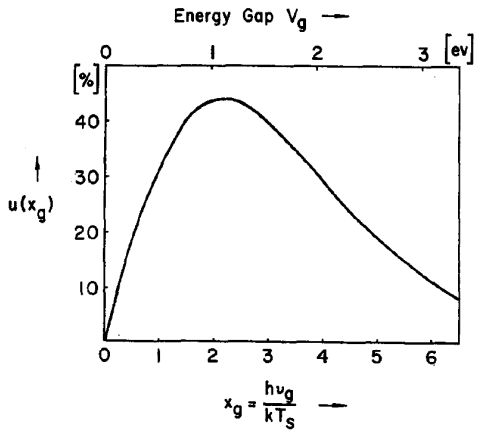


Figure 1.9 *Dependence of the ultimate efficiency $u(x_g)$ upon the bandgap V_g of the semiconductor [15].*

The detailed balance limit is also known as the Shockley-Queisser limit or SQ limit. According to the SQ limit, the ultimate efficiency of single-junction Si (V_g = 1.12 eV) solar cell

is approximate 32%. However, the SQ limit is based on the assumption that only radiative recombination exists in the solar cell, which is not suitable for Si solar cells. Silicon is an indirect bandgap semiconductor where non-radiative Auger recombination is dominant. Taking this constraint into account, the theoretical efficiency limit of a single-junction Si solar cell is calculated as 29.4% [17].

1.2 Si-based tandem solar cells

Up to now, the highest efficiency of the single-junction Si solar cell is 26.7%, approaching the SQ limit [18]. This result is obtained in an amorphous silicon/crystalline silicon heterojunction solar cell with interdigitated back contacts. The multijunction solar cell is a viable pathway to overcome the limit by stacking materials with different bandgaps together. The top cell and the bottom cell absorb different portions of the solar spectrum, thus reducing the thermalization losses, as shown in Figure 1.10 (b).

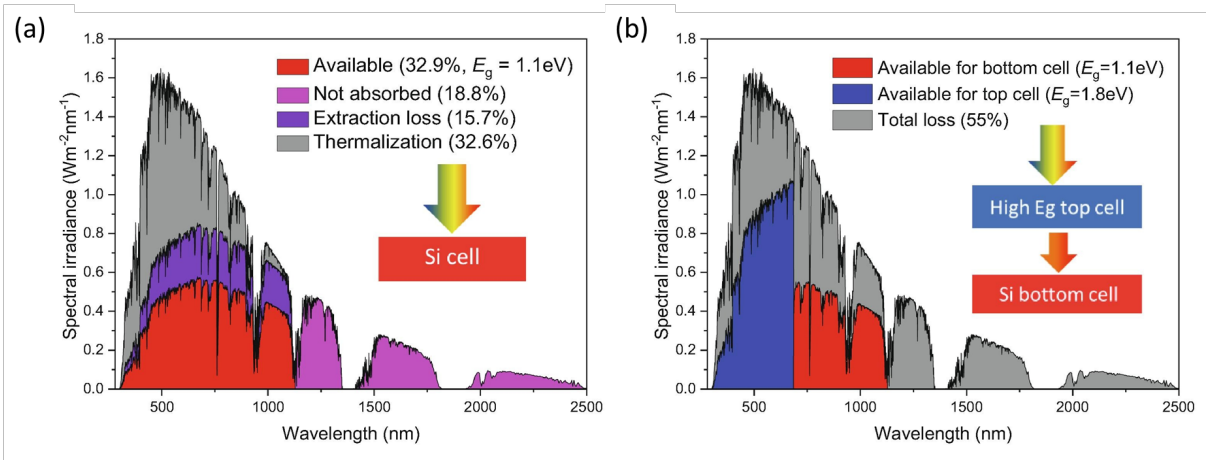


Figure 1.10 *Losses and maximum available solar energy of (a) a silicon single-junction solar cell and (b) a Si-based tandem solar cell, illustrated in the AM1.5G solar spectrum [19].*

For instance, in the GaAs/Si tandem solar cell, GaAs mainly absorbs visible spectrum while Si mostly absorbs near-infrared spectrum. Consequently, the total EQE is increased, as shown in Figure 1.11. The dual-junction (2J) solar cell is the simplest multijunction structure. It is attractive due to the great efficiency gain and the lowest incremental fabrication cost over single-junction devices compared with other multijunction solar cells [21].

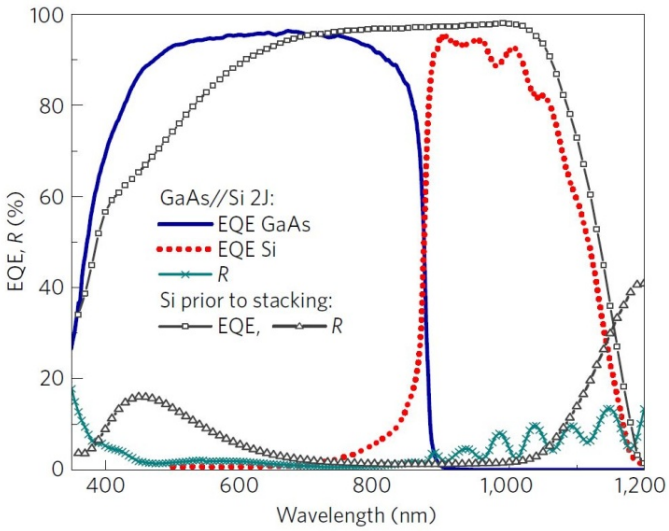


Figure 1.11 *EQE and reflection curves of GaAs/Si dual-junction solar cell and the used Si heterojunction solar cell before stacking [20].*

When designing high-performance tandem solar cells, the choice of bandgaps is crucial. The optimal bandgap combination of the 2J solar cell is around 1.62 eV and 0.91 eV, giving a limiting efficiency of 42.8% [22]. For 2J Si-based tandem solar cells, the maximum efficiency is around 42.4% with a 1.72 eV top cell. III-V compound semiconductor, perovskite, and chalcogenide are good candidates for top cells due to the wide range of bandgap energies.

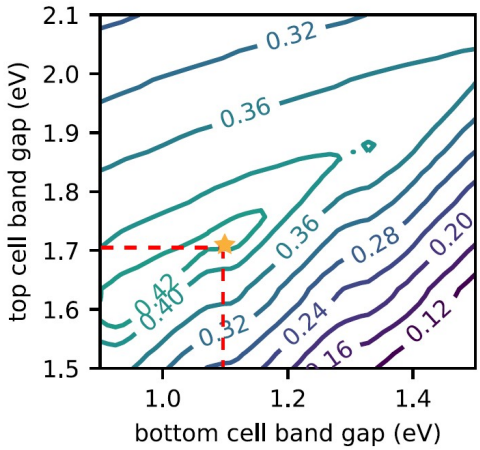


Figure 1.12 *Efficiency contours of 2J tandem solar cells against the bandgaps of top and bottom cells [22].*

Generally, Si-based tandem solar cells are known as four-terminal (4T), two-terminal (2T), and three-terminal (3T) depending on the configuration, as shown in Figure 1.13. The details of these three kinds of Si-based tandem solar cells are described as follows.

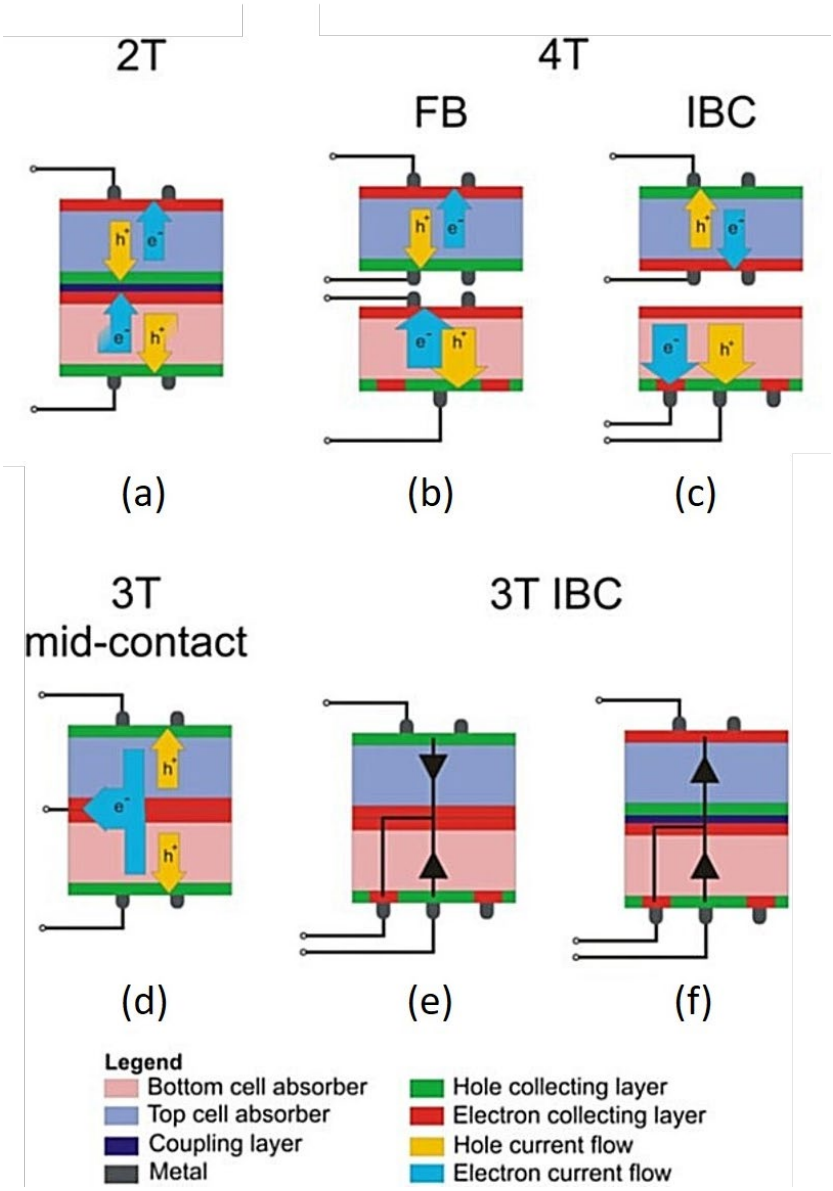


Figure 1.13 *Different internal interconnection schemes for 2J solar cells: (a) series-connected 2T tandem cell; Independently operating 4T tandem cells using (b) front-back (FB) contacted and (c) IBC bottom cells; 3T tandem cell with (d) mid-contact, (e) IBC bottom cell within a bipolar junction transistor, and (f) IBC bottom cell with a tunnel junction. Blue and yellow arrows indicate the current pathways of electrons and holes, while the thickness of the arrows qualitatively illustrates the respective current densities. Black equivalent circuit models in (e) and (f) highlight the arrangement of cell diodes [23].*

1.2.1 2T Si-based tandem solar cells

In 2T Si-based tandem solar cells, the two subcells are connected in series by an interconnection. A significant benefit of the 2T device is that it has only two terminals and can be operated as a standard single-junction solar cell, thus greatly simplifies its integration in PV modules and systems. In addition, there is no intermediate electrode as in 4T devices, thereby reducing the series resistance and parasitic absorption. Generally, 2T Si-based tandem solar

cells can be fabricated by direct growth or wafer bonding.

When directly growing tandem solar cells, an interconnection such as tunnel junctions or recombination layers are typically used to electrically connect the subcells [24]-[32]. Epitaxial growth of top cells on Si substrates is a straightforward approach that has been attractive for decades [33]-[41]. The benefit of direct epitaxial growth is that only one substrate and one epitaxial process are needed, thus reducing the manufacturing cost and complexity. When III-V materials are used as the top cell, the lattice mismatch between them and Si has always been a challenge. Therefore, the graded buffer layers grown by the metamorphic epitaxy have been widely used to transfer the lattice constants of silicon to that of III–V materials [36]-[41]. Monolithically epitaxial grown $GaAs_{0.75}P_{0.25}$/Si 2J solar cell with an efficiency of 23.4 ± 0.3% was demonstrated by Lepkowski, D. L. *et al.* [42]. The $GaAs_{0.75}P_{0.25}$ top cell and Si bottom cell are connected by p^{++}/n^{++}-$GaAs_{0.75}P_{0.25}$ tunnel junction and step-graded $GaAs_yP_{1-y}$ buffer layer grown by metal-organic chemical vapor deposition (MOCVD). 25.0% efficient $GaAs_{0.75}P_{0.25}$/Si 2J solar cell grown by molecular beam epitaxy (MBE) was reported by Fan, S. *et al.* [41]. They improved the performance of the tandem cell by utilizing an AlGaAsP back surface field (BSF) layer and a backside textured Si bottom cell.

The recombination layers used in the monolithic tandem solar cells can be metal interconnects, transparent conductive adhesives (TCAs), or nanocrystalline silicon recombination junctions [27]-[32]. Monolithic perovskite/silicon tandem with a certified power conversion efficiency of 29.15% was reported by Al-Ashouri, A. *et al.*, exceeding the efficiency world record for a single-junction Si solar cell [43]. They used a self-assembled monolayer that provides both fast extraction and efficient passivation at the hole-selective interface as the interconnection. Soon after this, Oxford PV announced that they have fabricated a monolithic 2T perovskite/Si tandem solar cell with a certified efficiency of 29.52% [44].

When connecting subcells by wafer bonding, the lattice mismatch problem during the epitaxy growth process can be bypassed. For example, III-V top cells with good crystal quality can be grown on lattice-matched GaAs or Ge substrates and then transferred to Si bottom cell. The GaAs or Ge substrates are subsequently removed. Because the top cells are grown before bonding, there is no temperature limitation associated with the bottom cell. $Al_{0.1}Ga_{0.9}As$/Si 2J solar cell with an efficiency of 25.2% measured under a 600 nm-peaked halogen white light source of a one-sun intensity was reported [45]. $Al_{0.1}Ga_{0.9}As$ top cell was grown on a GaAs

substrate by MBE and layer-transferred onto a Si bottom cell through the p^+-GaAs/n^+-Si direct fusion bonding at 300 °C and subsequent removal of the GaAs substrate. Another 2J III-V/Si solar cell fabricated by Surface-Activated direct wafer Bonding (SAB) was reported in 2019, with an efficiency of 21.1 ± 1.5% at one-sun condition [46]. In their work, the III-V top cell is a heterojunction formed by an n-$Ga_{0.5}In_{0.5}P$ emitter and a p-$Al_{0.2}Ga_{0.8}As$ base.

One of the challenges for the wafer bonding method is the reuse of the high-cost epitaxial substrates for the top cells. Wafer bonding has to be combined with III-V substrate reuse strategies like epitaxial lift-off (ELO) or spalling to be cost-competitive [46], [47]. Besides, strict subcell surface treatments are required to achieve particle-free and mirror-polished surfaces with root-mean-square roughness values below 1 nm before bonding, increasing the processing complexity [48].

One of the shortcomings of 2T tandem solar cells is that the requirement of the current matching between the subcells limits the choices of materials in terms of bandgaps [22]. The fabrication process compatibility, such as fabrication temperature, should also be considered carefully.

1.2.2 4T Si-based tandem solar cells

In 4T Si-based tandem solar cells, the subcells are fabricated separately and then joined together by mechanical stacking. An optically transparent insulating layer is indispensable between subcells. The two subcells in 4T tandem solar cells are only optically coupled but not electrically, hence no current matching requirement. The subcells can be independently optimized during the fabrication process. The fabrication flexibility eliminates the constraint for the orientation or polarity of subcells, thus allowing more choices for top cell materials. Besides, 4T tandem solar cell has lower sensitivity to spectral variations compared with 2T device according to the simulation result [49].

Up till now, the highest efficiency of III-V/Si 2J solar cell is 32.8%, achieved by mechanically stacking GaAs on SHJ bottom cell [20]. The GaAs top cell is grown by metalorganic vapour phase epitaxy (MOVPE) and attached to a glass slide which is stacked on the separately fabricated SHJ cell using a transparent adhesive. For 4T perovskite/Si tandem solar cells, maximum efficiency of 26.7% was achieved in 2018 [50]. The perovskite top cell is stacked on a high-performance PERC-Si cell.

Even though high efficiencies have been achieved in 4T tandem solar cells, there are

several disadvantages of this configuration. The additional contact (metal grids, or/and transparent conductive layer) at the backside of the top cell increases the optical and resistive losses. The insulating layer between two subcells and the additional contact also increases the material cost. Furthermore, the 4T designs are currently incompatible with monolithic growth. More electrodes and inverters are demanded in 4T devices, increasing its complexity and cost of integration in PV modules and systems [51].

1.2.3 3T Si-based tandem solar cells

Compared with the conventional 2T and 4T tandem solar cells, 3T tandem solar cells combine the advantages of 2T and 4T solar cells designs. In 3T tandem solar cells, independently working subcells allow comparable design flexibility as in 4T tandem solar cells and thus result in higher cell efficiency and energy yield [23], [49]. At the same time, the monolithic design avoids the use of extra transparent interconnection layers, insulating layers, and intermediate electrodes. Compared with 2T tandem solar cells, the adding of the third contact in 3T tandem solar cells eliminates the requirement of current matching [52]. In general, there are two types of 3T tandem solar cells depending on the configuration of contacts, either with a front contact, a back contact, and a mid-contact (Figure 1.13 (d)), or with one front contact and two back contacts (Figure 1.13 (e) and (f)).

In mid-contact 3T tandem solar cells, the mid-contact collects the current from the physical contact between the two absorbers, thus avoiding the need for a tunnel junction between two subcells [53]. However, the fabrication of transparent and highly conductive middle electrodes remains a challenge and the lateral current collection between the two absorbers limits the area of the devices. Therefore, it is beneficial to move the mid-contact to the back side of the bottom cell.

The 3T tandem solar cells with one front contact and two back contacts are consist of a top cell with front contact and an IBC Si bottom cell. The first 3T Si-based tandem solar cell with IBC Si bottom cell was reported by Nagashima T. [54]. In their work, $Al_{0.3}Ga_{0.7}As$ was used as the top cell and was stacked on Ge or Si bottom cell with two back contacts. This configuration avoids the need for transparent and highly conductive middle electrodes. Besides, there is no requirement for lateral current collection in this kind of tandem solar cells, thus allowing the fabrication of large-scale devices.

In 3T tandem solar cells, the maximum power point is determined for total power instead

of individually for each of the subcells [53]. The first experimental realization of 3T perovskite/Si tandem solar cell with an IBC SHJ bottom cell was reported to yield a combined stabilized conversion efficiency of 17.1% under maximum power point conditions [55]. The efficiency of an optimized 3T perovskite/Si tandem solar cell with a conventional SHJ bottom cell was calculated to be 32% [56]. 3T GaInP/Si tandem solar cell was reported to achieve an efficiency of 27.3 ± 1.0% [57]. In their work, the GaInP top cell and the IBC Si bottom cell were bonded by a TCA consisting of silver-coated microspheres embedded in epoxy.

In spite of the many advantages of 3T Si-based tandem solar cells, their disadvantages cannot be ignored. Because the 3T device does not have an easily replicated unit that can be connected together in series, the interconnection design of 3T tandem cells is more complex than that of 2T and 4T tandem cells [53].

Overall, 2T, 4T, and 3T Si-based tandem solar cells have their own advantages and drawbacks. Even though the performance of the 4T device is better than that of the 2T device according to the efficiency in some cases, the 2T device is more promising for terrestrial applications due to the easier integration in modules and lower cost. So far, the 2T monolithically integrated device is the only configuration established for commercial application thanks to its simple interconnection scheme [51], [58]. This is the configuration we will use in this thesis which is part of the HETONAN (acronym for “High-efficiency tandem solar cells based on III-V nanowires on silicon”) project.

1.2.4 III-V nanowires/Si tandem solar cells

As mentioned before, III-V compound semiconductor, perovskite, and chalcogenide are all good choices to be used as top cells in Si-based tandem solar cells. Among these candidates, III-V semiconductor solar cells are more attractive to us due to their remarkable efficiency and long-term reliability. The most efficient solar cell in the world is a III-V multijunction cell with an efficiency of 47.1% in a six-junction inverted metamorphic concentrator solar cell [59]. As a consequence, III-V solar cells play an irreplaceable role in space applications. After the development of several decades, the manufacturing technique of III-V solar cells has matured. However, the expensive material and processing limit the terrestrial applications of III-V solar cells. In order to reduce costs while maintaining high efficiency, III-V/Si tandem solar cell is a promising approach by replacing expensive Ge or GaAs substrates with cheaper Si substrates.

Considering the lower complexity of manufacturing and easier integration in photovoltaic

modules, 2T III-V/Si tandem solar cells have been studied [58]. Heteroepitaxy growth is a convenient approach to directly integrate III-V solar cells onto Si substrate [60], [61]. Nevertheless, the lattice mismatch between III-V materials and Si is a significant challenge for integration. To overcome this limit, III-V nanowires (NW)-based solar cells have been investigated by scientists since the mid-2000s [62]-[65].

Benefit from the small lateral dimension, lattice-mismatch-induced strain can be relaxed through the NW's sidewall, making it possible to direct epitaxy III-V NWs on Si [66]. What's more, NWs also reduce the reflection of light and increase the light-trapping of sunlight [64]. The theoretical limiting efficiency of two-junction GaAsP NWs/Si tandem solar cells is calculated to be 33.8% (1 sun, AM 1.5G) and 42.3% (500 suns, AM 1.5D) [67]. It indicates that III-V NWs/Si tandem solar cells are capable of competing with today's three- and four-junction solar cells. To date, there are only two reported experimental work on III-V NWs/Si tandem solar cells. The first realization of III-V NWs/Si tandem cells was reported by Yao, M. *et al*. in 2015 [62]. In their work, GaAs NWs top cell with an area of 1 mm^2 was grown by MOCVD on (111)-oriented Si bottom cell and the two subcells were connected by a low-resistance n^+-GaAs/p^+-Si heterojunction. An open-circuit voltage of 0.956 V and an efficiency of 11.4% were observed. The other fabricated III-V NWs/Si tandem solar cells was reported by Wood, B. A. *et al*. in 2017 [68]. $GaAs_{0.75}P_{0.25}$ NWs array with an area of 100 µm × 100 µm was grown on Si solar cells by MBE. The two subcells were connected by p^+-$GaAs_{0.75}P_{0.25}$/n^+-Si heterojunction. Because the bandgap of $GaAs_{0.75}P_{0.25}$ (1.7 eV) is higher than that of GaAs (1.42 eV), the open-circuit voltage of the tandem solar cell was increased to 1.16 V. Nevertheless, the efficiency of this $GaAs_{0.75}P_{0.25}$ NWs/Si tandem cell was only 3.51%, lower than that of GaAs NWs/Si tandem cell.

When using NWs as the top cell, there are two main configurations for the p-n junction, axial junction and radial junction, as shown in Figure 1.14. In axial junction, the direction of carrier extraction is parallel with the light absorption direction. Hence the height of the NWs with an axial junction is limited given the carrier diffusion length. While in the radial junction, the directions of light absorption and carrier extraction are decoupled into orthogonal spatial directions [69]. The NWs are allowed to keep long in the light incident direction to obtain optimal light absorption. At the same time, the small radius of NWs guarantees effective carrier collection as the carrier extraction direction is radial. Because the minority carrier diffusion length is generally longer than the NW radius, the NWs with radial junction are more

tolerant to the bulk defects which decrease minority carrier lifetimes [64]. NWs with radial junctions can achieve high efficiency with lower materials quality than in axial junction NWs.

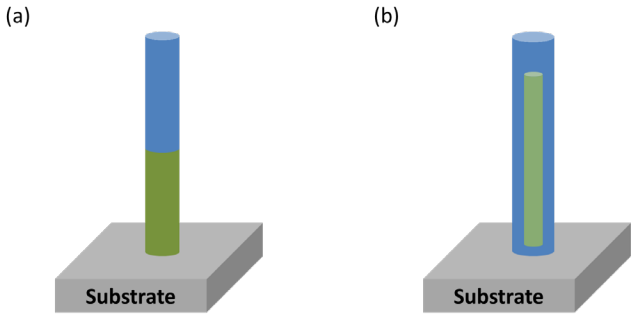


Figure 1.14 *Schematic of NW with (a) an axial junction and (b) a radial junction. Different colors represent different materials or the same material with different dopants.*

Therefore, a project named HETONAN funded by ANR (Agence Nationale de Recherche, ANR-15-CE05-0009-04) is carried out. The objective of this project is to fabricate high-efficiency III-V NWs/Si tandem solar cells. III-V NWs array with a radial junction is grown by molecular beam epitaxy (MBE) as the top cell and monocrystalline Si is used as the bottom cell (Figure 1.15). A low-resistance Si tunnel junction (p^{++}/n^{++}) is implemented on the top of the bottom cell in order to electrically connect the two sub-cells. (111)-oriented Si substrate is required to guarantee the high vertical yields of III-V NWs epitaxy [70].

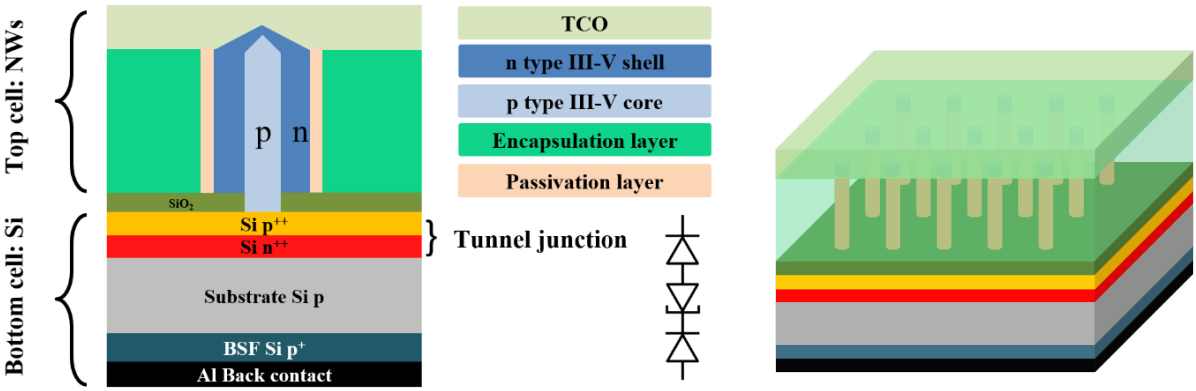


Figure 1.15 *Schematic of targeted III-V NWs/Si tandem solar cell in HETONAN project.*

1.3 Tunnel junction

As mentioned above, an interconnection is required to connect subcells in 2T monolithically integrated Si-based tandem solar cells. This interconnection should feature low electrical resistivity as well as high optical transmissivity. Normally, transparent conductive oxides (TCO) or interband tunnel junctions are adopted to satisfy these requirements. However,

the temperature tolerance of TCO makes them incompatible with a high-temperature top cell fabrication process. For example, degeneration of the electrical properties of indium tin oxide thin films has been observed when the annealing temperature reaches 500 °C [71], [72]. Besides, the parasitic absorption of TCO and its refractive index mismatch with silicon can lead to optical loss [73], [74]. Therefore, interband tunnel junction is used as the interconnection in this thesis. It is a reversed p-n junction that exists between the p-n junctions of the top cell and the bottom cell. Considering the requirement of current-match between subcells in 2T devices, tunnel junction allows effective current to flow with minimal voltage drop from one cell to the next based on the quantum tunneling phenomenon [75].

1.3.1 Physics of tunnel junction

1.3.1.1 Quantum tunneling

Quantum tunneling is a phenomenon in which quantum particles can penetrate or pass through a potential barrier whose maximum height is higher than the kinetic energy of the particles. It exclusively occurs on the quantum scale and there is no counterpart in classical mechanics. This phenomenon can be explained by the Heisenberg uncertainty principle that the position Δx and momentum Δp of an object can never be measured accurately at the same time, which is known as:

$$\Delta p \cdot \Delta x \geq \hbar/2 [76]. \tag{1.18}$$

It means that electrons should be described by wave functions rather than particles when it comes to position. The wave function Ψ must satisfy the Schrödinger equation:

$$\frac{\mathrm{d}^2}{\mathrm{d}x^2}\Psi + \frac{2m}{\hbar^2}[E - V(x)]\Psi = 0 \ [77]. \tag{1.19}$$

The square of the wave function amplitude at a certain location represents the probability that an electron is observed at that location. When an electron collides with a potential barrier, the amplitude of the wave function decreases exponentially in the barrier. Once the wave function departs the barrier, its amplitude does not decay anymore. Therefore, the probability of the wave function passing through the barrier is nonzero. If the barrier is thin enough, the decrease of the amplitude will be minuscule and there is a great probability for the electron to be observed on the other side of the barrier. This phenomenon exists only from the perspective of quantum mechanics, so it is called quantum tunneling. It has important

applications in tunnel diodes, quantum computing, scanning tunneling microscope, and so on.

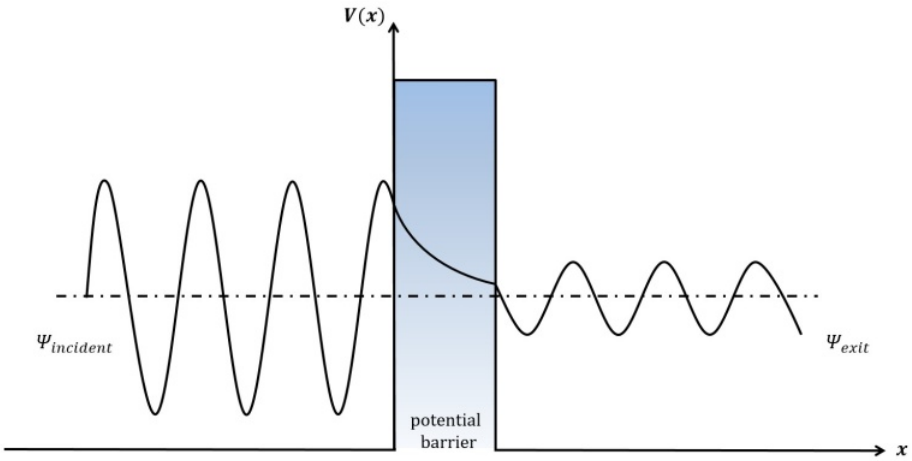


Figure 1.16 *Schematic diagram of quantum tunneling.*

1.3.1.2 *I-V* characteristics of the tunnel junction

A tunnel junction can be formed by a heavily doped p-n junction in which both the p- and n-sides are degenerate. The first quantum electron device based on tunnel junction, known as tunnel diode, was invented by Esaki in 1957 [78]. A tunnel diode simply consists of a tunnel junction and two terminals. Fermi levels of tunnel junction on p-side and n-side are located within the allowed bands as shown in Figure 1.17. The bottom of the conduction band on the n-side is lower than the top of the valence band on the p-side. It means that there are identical energy states in the conduction band of the n-side and the valence band of the p-side. Because the tunnel junction is highly doped, the depletion region is narrow enough (5-10 nm) for electrons to tunnel through, resulting in the generation of tunneling current [13]. The current-voltage characteristic of the tunnel junction is shown in Figure 1.18. The forward current of a tunnel diode is composed of diffusion current and tunneling current. If a small forward voltage is applied, the diffusion current is very low and the tunneling current plays an important role.

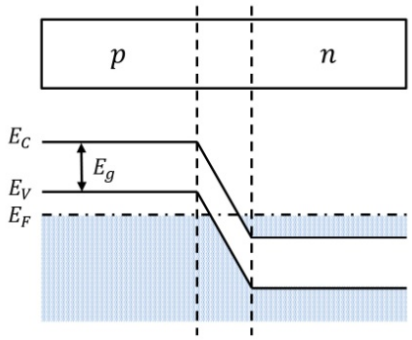


Figure 1.17 *Band structure of a tunnel junction.*

When no voltage is applied, the tunnel diode is at the condition of thermal equilibrium and the Fermi level is continuous. There is no unoccupied state below the Fermi level and no occupied state above the Fermi level. Therefore, no electrons tunnel through the depletion region in this case, corresponding to point 0 in Figure 1.18.

When a small forward bias V is applied, the band on the n-side raises qV relative to the p-side. There are occupied states below the Fermi level on the n-side and unoccupied states above the Fermi level on the p-side with the same energy states. So, some electrons in the conduction band on the n-side move to the p-side by tunneling, forward current from p-side to the n-side generated, corresponding to point 1.

More and more electrons tunnel from n-side to p-side as the forward bias increases. As a result, the tunneling current keeps increasing until the Fermi level of the p-side is the same as the bottom of the conduction band of the n-side, which corresponds to point 2 in the *I-V* curve. At this point, the flux of tunneling electrons is maximum so that the tunneling current reaches its peak value.

If the forward bias is further increased, fewer electrons will tunnel through the barrier due to the decrease of available energy states on both sides. The tunneling current then decreases as the voltage increases, known as the negative differential resistance, as shown at point 3. This is a peculiarity of tunnel diodes.

When the forward bias is increased to V_v, the bottom of the conduction band on the n-side has the same energy level as the top of the valence band on the p-side. There are no more available quantum states on both sides and hence the tunneling current should decrease to zero. However, the valley current is much bigger than the forward diffusion current in practice. The excess current is attributed to the existence of impurities or defects in the bandgap [79]. When the forward bias is higher than V_v, the barrier height decreases and the current is gradually dominated by forward current [80].

When a reverse bias is applied, the band of the p-side raises relative to the n-side. The valence band electrons of the p-side tunnel into the conduction band of the n-side, resulting in reverse tunneling current. The reverse tunneling current increases with the increase of reverse bias, as shown at point 5.

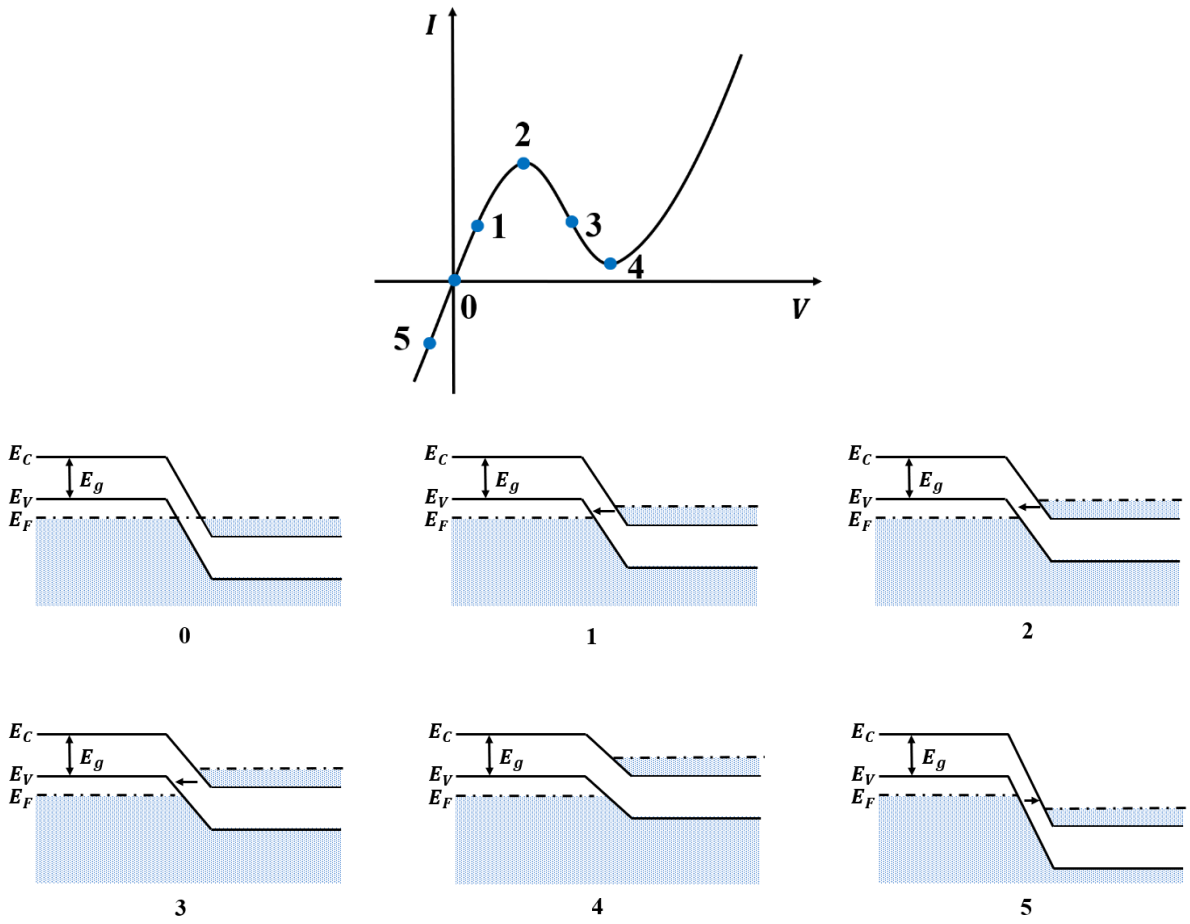


Figure 1.18 *Current-voltage characterization of the tunnel junction and corresponding band structures.*

In this chapter, the working principle and the efficiency limit of single-junction solar cells have been reported. One approach to overcome this limit is to use multijunction solar cells. Therefore, three kinds of dual-junction Si-based tandem solar with different configurations (4T, 2T, and 3T) have been introduced. Among them, 2T Si-based tandem solar is more attractive to us due to its simple integration in modules and lower cost. The tunnel junction has been chosen as the interconnection in 2T Si-based tandem solar. The working principle and characterization of tunnel junctions have been presented.

1.4 Objective and outline of the thesis

The objective of this thesis is to fabricate Si tunnel junction and implement it as the interconnection in the tandem solar cells. As mentioned before, this thesis is part of the HETONAN (acronym for “High-efficiency tandem solar cells based on III-V nanowires on silicon”,

granted by ANR) project. The ultimate purpose of this project is to develop a high-efficiency tandem solar cell structure by combining a planar Si bottom cell with a III-V nanowires (NWs) top cell. The two subcells will be connected in series by a low-resistance Si tunnel junction elaborated in this thesis. The outline of this thesis is shown as follows.

In Chapter 2, the fabrication and characterization methods of tunnel junctions will be introduced. First, we will compare different tunnel junction fabrication approaches and then explain why we choose proximity rapid thermal diffusion (PRTD) for our research. Afterwards, characterization methods of tunnel junctions will be presented. We will compare two typical techniques which are used to characterize doping profiles of tunnel junctions, the secondary ion mass spectrometry (SIMS) and the electrochemical capacitance-voltage (ECV) profiler. The working principle of these two techniques will be presented. To characterize the electrical properties of tunnel junctions, tunnel diodes should be fabricated. Therefore, a semiconductor characterization system used for the *I-V* characterization of tunnel diodes will be introduced.

Chapter 3 will focus on the fabrication and characterization of p^{++}/n^{++} tunnel junction on (111)-oriented Si wafer. Firstly, the investigation of different impact factors during the tunnel junction fabrication process will be presented. The formation of n^{++} emitters diffused by the photovoltaic industrial technique (LYDOP, acronym for Leaktight Yield Doping) and the p^{++} layer obtained by boron PRTD will be described. After optimizing the different impact factors, an optimized fabrication process of Si p^{++}/n^{++} tunnel junction will be proposed. Secondly, the fabrication and characterization of Si tunnel diodes will be presented. These tunnel diodes can demonstrate the electrical properties of the fabricated tunnel junctions.

Chapter 4 will show the implantation of p^{++}/n^{++} Si tunnel junctions in solar cells. First, the fabrication processes of single-junction Si solar cells with and without p^{++}/n^{++} Si tunnel junction on the surface will be displayed. The characterization results of these Si solar cells will be compared to investigate the impact of tunnel junctions on the performance of the solar cell. Second, the implementation of p^{++}/n^{++} Si tunnel junction in III-V NWs/Si tandem solar cells will be reported. The development of the fabrication process of NWs/Si tandem solar cells will be described. After this, the fabrication process and characterization results of our first trial of targeted III-V NWs/Si tandem solar cells will be presented.

Chapter 2 Tools for fabrication and characterization of the tunnel junction

2.1 Introduction

In this chapter, the tools used to fabricate and characterize tunnel junctions are reported. The first section introduces four tunnel junction fabrication approaches. In the second section, the methods to characterize doping profiles and electrical properties of tunnel diodes are presented. Two typical techniques used to measure the distribution of the dopants and a semiconductor characterization system used for the *I-V* characterization are introduced.

2.2 Tunnel junction fabrication technique

A shallow as well as heavily doping profile is necessary to form the tunnel junction. Several methods such as molecular beam epitaxy, chemical vapor deposition (CVD), ion implantation, and rapid thermal diffusion can reach the requirement.

2.2.1 Molecular beam epitaxy

MBE is a typical epitaxy method for depositing single-crystalline thin films under ultra-high vacuum (UHV, 10^{-7}-10^{-12} Torr) conditions. During the growth process, one or more thermal molecular beams interact with the crystalline substrate [81]. The main advantage of MBE is that the UHV environment ensures precise control of the dopant concentration and junction depth [82]. Various procedures are studied to obtain high as well as shallow doping layers. Si p^+-i-n^+ Esaki diodes on (100) substrate have been fabricated by two typical methods, in-situ low-temperature MBE combined with ex-situ post-annealing [83] and low-temperature MBE without post-annealing process [84]. Concentrations of the donors and acceptors reach higher than 10^{20} cm^{-3} in both cases.

However, MBE is too expensive for commercial production due to the requirement of UHV and the complex maintenance procedures [85]. Furthermore, the slow growth speed is not suitable for high throughput.

2.2.2 Chemical vapor deposition

Chemical vapor deposition (CVD) is a deposition method to produce various forms of materials, including monocrystalline, polycrystalline, and amorphous. Different from MBE, in which growth is controlled by kinetics, CVD is a growth technique dominated by thermodynamics [85]. During the CVD process, a thin solid coating is deposited on the

underlying heated substrate because of the chemical reaction from the vapor or gas phase [86]. It is an atomistic surface modification process and does not require a very high vacuum. The deposition rate of CVD is much higher compared with MBE. CVD films are generally quite conformal and with very high purity.

Various highly doped tunnel junctions have been fabricated by CVD during the last decades. Regarding Si-based tandem solar cells, MOCVD is usually used to grow metamorphic III-V tunnel junctions for III-V/Si tandem solar cells. For example, metamorphic $Al_{0.2}Ga_{0.8}As_{0.75}P_{0.25}/GaAs_{0.75}P_{0.25}$ tunnel junction grown by MOCVD designed for GaAsP/Si tandem solar cell have been reported [87][88]. MOCVD can also epitaxy III-V materials on highly doped Si emitters to form hybrid III-V/Si tunnel junctions [62].

While plasma-enhanced chemical vapor deposition (PECVD) and low-pressure chemical vapor deposition (LPCVD) are usually used to deposit a-Si tunnel junction or poly-Si tunnel junction for perovskite/Si tandem solar cells. For example, in the first monolithic perovskite/silicon tandem solar cell, an n^{++} hydrogenated a-Si layer was deposited by PECVD on a p^{++} c-Si emitter to form an n^{++}/p^{++} tunnel junction [89]. After the dopant activation annealing at 680 °C, the dopant concentration on the n^{++}/p^{++} Si interface is 10^{19}-10^{20} cm^{-3} according to the secondary ion mass spectrometry (SIMS) measurement. p^{+}/n^{+} poly-Si tunnel junctions with high-temperature stability that can be used for PERC have been reported by two groups, deposited by PECVD and LPCVD respectively [90][91]. The p^{+}/n^{+} poly-Si tunnel junction deposited by PECVD has active doping concentrations as high as 1.8×10^{20} cm^{-3} in the p^{+}- and 1.0×10^{20} cm^{-3} in the n^{+}-region after annealing at 800 °C. In addition, nano- or microcrystalline silicon tunnel junctions deposited by PECVD at low temperature (200 °C) have also been studied to satisfy the requirement of SHJ bottom cells used in perovskite/silicon tandem solar cells [32][92].

Even though CVD is a remarkable technique for film deposition, its disadvantages cannot be ignored. The property of the precursors is one of the primary disadvantages [86]. The precursors of CVD need to be volatile at near-room temperature, which is non-trivial for most of the elements in the periodic table. Besides, the precursors can be highly toxic, explosive, or corrosive, hence extremely strict safety precautions are required. What's more, the byproducts of CVD reactions can also be hazardous.

2.2.3 Ion implantation

Ion implantation is a technique that introduces impurities into solids by accelerating selected ion species with an electrical field. Its primary application is the electrical doping of semiconductors in the semiconductor industry [93]. The ions with adequate doping species are projected towards the semiconductor wafers which are fixed on the wafer holder. These ions are generally produced from a gas source, thus guaranteeing the purity of the source [94]. The key advantage of ion implantation is that the number of impurities introduced into the substrate and the penetration depth of the ions can be precisely controlled.

An n^{++}/p^{++} Si tunnel junction produced by ion implantation for the tandem solar cell was demonstrated by Bellanger, P. *et al*. in 2018 [95]. It is realized by successive implantation steps of boron and arsenic ions on an n-type c-Si wafer. The active concentration of donor and acceptor near the surface reach values of 3×10^{20} and 6.9×10^{19} cm^{-3}, respectively. The depth of the tunnel junction is around 70 nm.

The major disadvantage of ion implantation is the inevitable damage of the target wafer during the projected ions stopping process [94]. The violent collision of the ions with the target atoms displaces the latter from their equilibrium lattice site. The accumulation of displacement damage can result in the amorphization of the crystalline structure. Therefore, subsequent thermal annealing is necessary for ion implantation to reduce the lattice damage.

2.2.4 Rapid thermal diffusion

Thermal diffusion is commonly used to fabricate highly doped emitters for c-Si solar cells in the industrial process. The doping procedure includes the deposition of dopants source and drive-in process. However, the standard thermal diffusion process is not suitable to fabricate tunnel junction which requires an abrupt junction interface. Rapid thermal diffusion (RTD) is a technique using a solid diffusion source to achieve extremely shallow and highly doped junctions [96]. During the RTD process, the wafer is heated to a high temperature in seconds by high-intensity lamps or lasers, with a fast ramp and short baking time to activate the dopants. It is a low-cost method because it does not need a vacuum environment and has a low thermal budget. RTD has advantages such as high activation of implanted impurities and low redistribution of dopants compared with the conventional furnace diffusion process [97]. What’s more, RTD avoids the structural damage in the Si crystal, which is the main advantage over ion implantation [98]. Thus, the junction fabricated by RTD is suitable for integration with

other materials on the surface. Given all the features of RTD, it is chosen to fabricate Si tunnel junction in our research.

2.2.4.1 Diffusion theory

1) Impurity diffusion mechanism

Diffusion is a relatively straightforward process where the impurities can be introduced into the selected regions of a semiconductor. The diffusion of impurities in the crystal lattice plays an important role in altering the electronic properties of the semiconductor. This process is not only influenced by the concentration gradient, but also by temperature, crystal structure, and defect concentration [99].

The movement of impurity atoms in the lattice is realized by a series of random jumps which are driven by different diffusion mechanisms. Four major diffusion mechanisms of impurity atoms in silicon lattice are outlined below.

a) Interstitial diffusion

Figure 2.1 *Impurity diffusion by the interstitial mechanism*

Interstitial diffusion is a process that an impurity atom jumps from one interstitial site to another adjacent interstitial site in the lattice. It is a relatively rapid process because there are a number of this type of vacant sites in a semiconductor. The movement of lithium and sodium atoms in silicon is driven by this mechanism. However, the diffusion of impurities by this mechanism has no direct contribution to modifying the electronic properties of the semiconductor.

b) Substitutional diffusion

Figure 2.2 *Impurity diffusion by the substitutional mechanism*

The impurity atom in the substitutional diffusion process moves from one lattice site to another, thus substituting for the original host atom. It is necessary that the adjacent site is vacant, which means that vacancies must be present in the lattice to enable substitutional diffusion. Since the equilibrium concentration of vacancies is quite low, the rate of substitutional diffusion is slower than that of interstitial diffusion.

c) Interstitial-substitutional diffusion

In this case, the impurity atoms occupy interstitial as well as substitutional sites. It includes the dissociative mechanism and kick-out mechanism. In dissociative diffusion, a substitutional impurity atom leaves the lattice site and becomes an interstitial, producing a vacancy. Copper and nickel move in silicon through this mechanism. The effective diffusivity depends on both impurity concentration and crystal quality.

Figure 2.3 *Impurity diffusion by the dissociative mechanism*

The kick-out mechanism is an alternative pathway for interstitial diffusion. During this process, a rapid-moving interstitial diffuser moves into a lattice site by displacing an original host atom. As a result, a self-interstitial is generated. The behavior of gold and platinum in silicon can be described by this mechanism.

Figure 2.4 *Impurity diffusion by the kick-out mechanism*

d) Interstitialcy diffusion

Interstitialcy diffusion is a modified version of substitutional diffusion. Substitutional impurity atoms located in the lattice site are pushed into interstitial sites by the interstitial host atoms, resulting in the annihilation of self-interstitials. Then, these impurities diffuse to their adjacent substitutional sites and create new self-interstitials. It means that the interstitial

position of the diffusing impurity atoms is just a transition state as they move from one substitutional site to another. During this process, new substitutional sites always appear, leading to the concentration of vacant substitutional sites higher than its equilibrium value. Consequently, the rate of interstitialcy diffusion is somewhat faster than that of substitutional diffusion. The diffusion of boron and phosphorus in silicon is dominated by this mechanism.

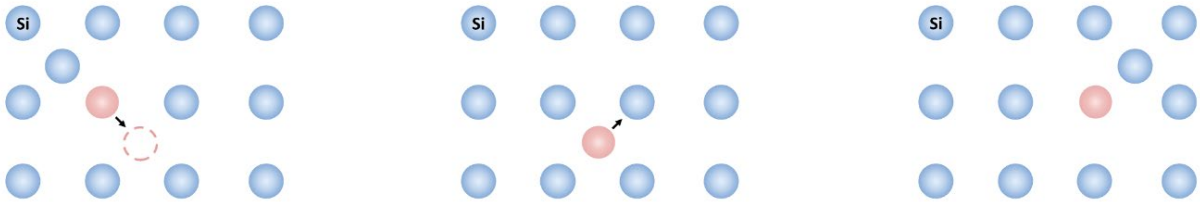


Figure 2.5 *Impurity diffusion by the interstitialcy mechanism*

2) Diffusion equation

Even though the jumping of impurities in a semiconductor is random, directed movement occurs statistically if there is an impurity concentration gradient. The correlation between the net flux of diffusing impurities and concentration gradient can be described by Fick's first law:

$$\vec{J} = -D\nabla C \tag{2.1}$$

where $\vec{J}$ is the flux density in $cm^{-2}\cdot s^{-1}$, D is the diffusivity in $cm^{2}\cdot s^{-1}$, C is the volume concentration in cm^{-3}. It indicates that the flux density is directly proportional to the concentration gradient under diffusion conditions. When applied in a one-dimension case, Fick's first law becomes:

$$J = -D\frac{\partial C}{\partial x} \tag{2.2}$$

where x is the distance in cm.

Although Fick's first law describes the diffusion process accurately, the flux density of impurities is not convenient to measure. And it is only applicable to steady-state diffusion where $\vec{J}$ and C do not vary with time.

Thus, Fick's second law is derived for non-steady-state diffusion case:

$$\frac{\partial C}{\partial t} = \nabla \cdot (D\nabla C) \tag{2.3}$$

where t is the diffusion time in s, C is the volume concentration which is a function of both time and position. It has more readily measurable quantities and predicts the change of concentration over time. In isotropic materials, such as Si, when the concentration varies only

along x direction, Eq.(2.3) becomes:

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \tag{2.4}$$

When D is independent of concentration and hence of position, it simplifies to:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \tag{2.5}$$

The solutions of Eq.(2.5). under two typical situations are presented respectively as follows.

a) Unlimited impurity source

When a wafer is exposed to an infinite amount of impurity, the surface concentration of impurity can be considered as constant during the diffusion process. The solution of Eq.(2.5) is:

$$\frac{C - C_s}{C_0 - C_s} = \mathrm{erf}\left(\frac{x}{2\sqrt{Dt}}\right) \tag{2.6}$$

where C_s is the impurity concentration at the surface in cm^{-3}, C_0 is the initial impurity concentration in the substrate and erf is the error function:

$$\mathrm{erf}\, z = \frac{2}{\sqrt{\pi}}\int_0^z \exp(-u^2)\, du \tag{2.7}$$

If $C_0 = 0$,

$$C(x,t) = C_s\, \mathrm{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \tag{2.8}$$

where erfc is the complementary error function defined by:

$$\mathrm{erfc}\, z = 1 - \mathrm{erf}\, z \tag{2.9}$$

A sketch of impurity concentration for various diffusion times is shown in Figure 2.6. Its most significant feature is that the surface concentration is constant whereas the diffusion depth increases with time.

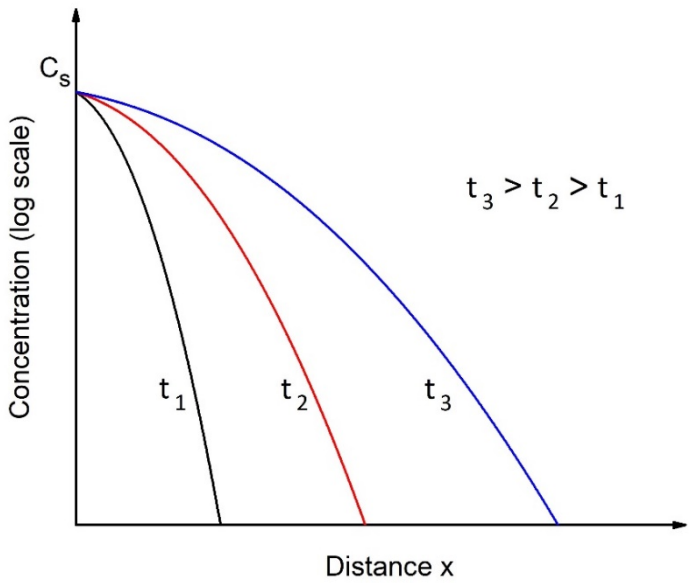


Figure 2.6 *Unlimited-source diffusion profile*

b) Limited impurity source

When a finite quantity of impurity is placed on the wafer at the beginning, the solution of Eq.(2.5) is given by:

$$C(x,t) = \frac{Q_0}{\sqrt{\pi D t}} exp\left(-\frac{x^2}{4Dt}\right) \tag{2.10}$$

where Q_0 is the total amount of impurity placed on the surface prior to diffusion.

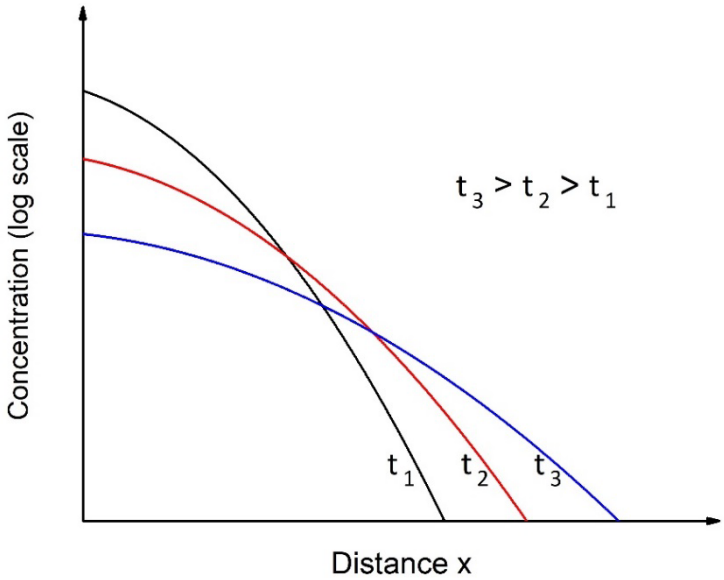


Figure 2.7 *Limited-source diffusion profile*

A sketch of impurity concentration profile evolution versus time in this case is shown in Figure 2.7. It shows that the surface concentration decreases as with increasing time, which is

different from the unlimited-source case.

2.2.4.2 Spin-on doping

Spin-on doping, also known as the spin-on dopant or spin-on diffusant, is an economical and facile technology to provide impurity sources for thermal diffusion. It is often called SOD by the acronym. Uniform and consistent doping layers can be obtained by this method.

The procedure of SOD is shown in Figure 2.8 (a). It must be carried out under ventilation. The substrate is put on the vacuum chuck of a wafer spinner (SPS-Europe SPIN150 wafer spinner is used in this thesis). The solution containing polymer and dopants is dripped at the center of the substrate. Then the substrate rotates at a high speed to spread the solution over the whole surface. After spinning, the substrate is immediately baked on the hotplate for desolvation and then a layer of SOD film is formed on the surface. The thickness of the film can be modified by adjusting spinning parameters, such as spinning acceleration, spinning speed, and spinning time.

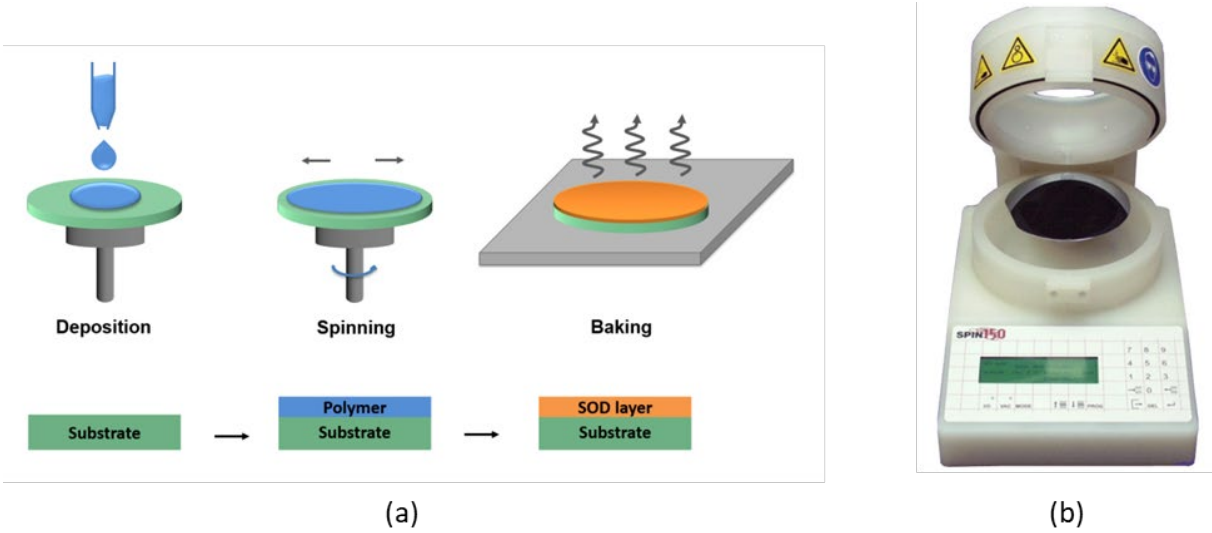


Figure 2.8 *(a) spin-on doping process; (b) SPS-Europe SPIN150 wafer spinner.*

Borofilm100 and Phosphorofilm from Emulsitone Co, containing boric acid or phosphoric acid, are generally employed as polymer solutions to provide boron or phosphorus dopants for Si substrates [100]. These solutions should be stored in the fridge and taken out in advance before use until they become room temperature. Si substrates are previously cleaned by hydrofluoric acid (HF, 5%) and Piranha solution (H_2SO_4 50% + H_2O_2 50%) to form a hydrophilic SiO_2 layer for spinning. The cleaning process is completed after deionized (DI) water rinsing and nitrogen (N_2) drying. Normally, the spinning acceleration is 400 rpm/s for Borofilm while

3000 rpm/s for Phosphorofilm. The spinning speed is 3000 rpm and the spinning time is 30 s for both solutions. The wafers are baked at 200 °C for 10 min after spinning to evaporate the solvents and then can be used to fabricate shallow junctions combined with rapid thermal diffusion. The reactions during the high-temperature annealing process are shown as follow:

$$2B_2O_3 + 3Si \rightleftarrows 3SiO_2 + 4B \tag{2.11}$$

$$2P_2O_5 + 5Si \rightleftarrows 5SiO_2 + 4P \tag{2.12}$$

In this thesis, Borofilm100 was used to provide boron dopants for Si substrates.

2.2.4.3 Proximity rapid thermal diffusion

As mentioned above, RTD is chosen to fabricate tunnel junctions in our research. However, there is a problem of boron diffusion with the SOD wafer. After annealing, a residue layer that is difficult to remove formed on the surface. It is a boron-rich layer and cannot be removed by HF. This layer is composed of SiB_4 or SiB_6 according to the literature [101].

Therefore, an alternative process called proximity rapid thermal diffusion (PRTD) is proposed. The arrangement of this method is shown in Figure 2.9. The SOD source wafer and the target wafer are stacked together and separated by thin spacers. Small 280-µm thickness silicon pieces are adopted. During the heating process, the dopants are released from the SOD source and transport across the short space to the device wafer in a nitrogen or air ambient.

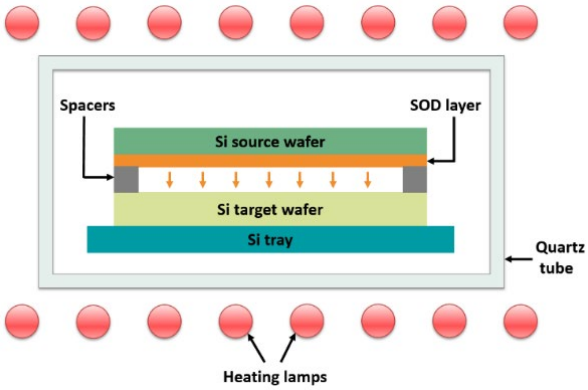


Figure 2.9 *Schematic diagram of the proximity rapid thermal annealing diffusion process*

A comparison of boron diffusion into silicon obtained by RTD and PRTD is shown in Figure 2.10 [102]. It shows that the formation of a residue layer on the target wafer is effectively avoided by PRTD.

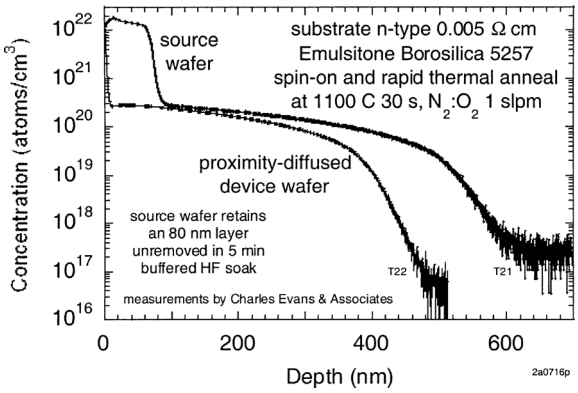


Figure 2.10 *SIMS measurements of boron diffusion into silicon comparing the profile obtained from a source wafer in direct contact with the spin-on diffusant with the profile resulting from proximity diffusion from the source wafer [102].*

ADDAX rapid thermal annealing (RTA) equipment, as shown in Figure 2.11, is adopted to implement the PRTD process. The tungsten halogen lamps are used to heat the wafers. Temperature is controlled by the lamp intensity through a computer system. A 4-inches Si wafer is employed as the sample holder and its back surface should be unpolished to reduce the reflection of light. The real-time temperature of the sample is indirectly measured by a temperature sensor put on the Si holder. Compressed air or N_2 is applied to fill the reaction chamber depending on the dopants.

Figure 2.11 *ADDAX rapid thermal annealing equipment*

A typical temperature profile of the annealing process (with the heating ramp of 100°C/s, 10 s of the plateau) is shown as follow:

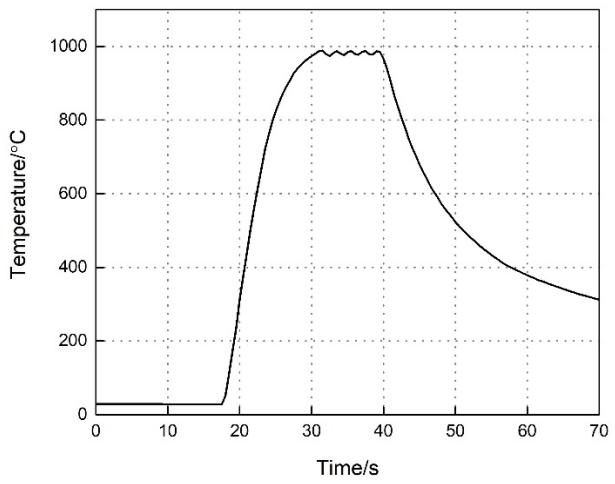


Figure 2.12 *A typical temperature profile of the RTD process*

2.3 Characterization methods of the tunnel junction

2.3.1 Doping profile characterization

Characterization of dopant distributions is necessary after the PRTD process. Secondary ion mass spectrometry (SIMS) and electrochemical capacitance-voltage (ECV) profiler are two typical techniques to obtain doping profiles.

2.3.1.1 Secondary ion mass spectrometry

SIMS is a microanalytical technique to understand the composition of solid materials. It is one of the mass spectrometry methods that use a mass spectrometer to separate ions by their mass to charge ratio. SIMS derives compositional information by analyzing detected secondary ions resulting from the bombardment of primary ions on the surface [103]. The focused energetic primary ions beam induces the emission of atoms and molecules from the solid's surface, a small percentage of which exists in the ionized state. Then the emitted ions, known as secondary ions, are collected by an ion extractor and then passed through a mass analyzer. Eventually, the ions reach the detector and output data in a format of mass spectrum, spatial image, or depth profile.

In order to obtain the depth profile, the material in the spatial region of interest is required to be removed. It is realized by sputtering with an ion beam in SIMS. This is a destructive technique, but the amount of removed material is quite small. The intensities of specific secondary ions and sputtering time are the values recorded. Then a plot of

concentrations versus depth is derived. The depth of measurement can vary from a few nanometers to several microns, depending on the sputtering time. However, the depth resolution of SIMS generally degrades with depth. When used to measure the dopants profile, the SIMS result shows the concentration of all dopant atoms in the substrate, including the inactivated ones.

2.3.1.2 Electrochemical capacitance-voltage profiler

ECV profiler is a common tool for measuring the active carrier concentration profiles in semiconductor layers. This technology uses a semiconductor-electrolyte Schottky-like contact to create a depletion region in which there are no carriers but immobile ionized charges. These charges come from dopants and electrically active defects. This depletion region behaves like a capacitor due to the presence of ionized charges. Capacitance measurements provide the information of active dopants and electrically active defects densities. The main part of the ECV profiler is the electrochemical cell.

The schematic illustration of the electrochemical cell is shown in Figure 2.13. The sample is pressed against a sealing ring filled with electrolytes. The size of the sealing ring defines the etching area of the semiconductor. The depletion region is created by applying a potential between the semiconductor and the electrolyte.

Generally, there are two basic steps of ECV profiling. The first step is the determination of carrier concentration by measuring the differential capacitance of the Schottky barrier produced at the semiconductor-electrolyte interface. According to the Mott-Schottky equation, there is a linear relationship between $\frac{1}{C^2}$ and V, with C the interfacial capacitance and V the applied voltage:

$$\frac{1}{C^2} = \frac{2}{\varepsilon_0 \varepsilon_r q N A^2}\left(V - V_{fb} - \frac{k_0 T}{q}\right) \tag{2.13}$$

Here ε_0 is the permittivity of free space, ε_r the relative permittivity of the semiconductor, q the charge of the electron, N the carrier concentration, A the effective contact or etching area, V_{fb} the flatband potential, k_0 the Boltzmann constant, and T the absolute temperature.

Thus, the charge carrier concentration of the semiconductor at the edge of the junction depletion layer is given by

$$N = \frac{2}{\varepsilon_0 \varepsilon_r q A^2 \cdot d(\frac{1}{C^2})/dV} \tag{2.14}$$

N is inversely proportional to the slope of $\frac{1}{C^2}(V)$. Besides, the measurement accuracy of the contact area A is essential for the precise profile.

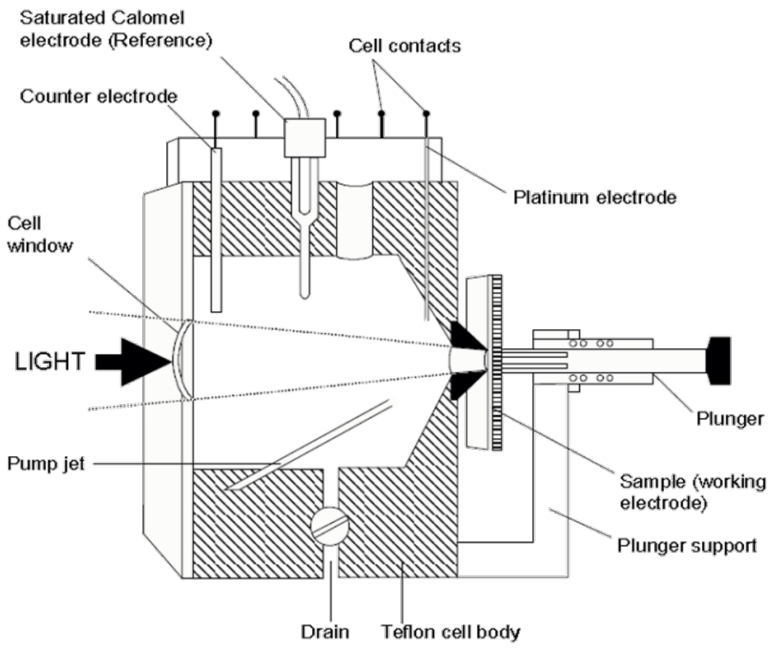


Figure 2.13 *Schematic illustration of an electrochemical cell [104]*

The second step is controlled etching of semiconductors via electrochemical anodic dissolution between successive capacitance measurements. Positive voltage is applied to the semiconductor while negative voltage is to the electrolyte. Holes are needed to etch the semiconductor material under electric control. For example, to etch one silicon atom, 4 holes are needed to release the 4 valency electrons under electric control. As a result, the positively ionized silicon atom core dissolves into the electrolyte fluid and drifts to the negatively charged current electrode.

When the surface of the semiconductor is p-type, the majority carriers are holes and they are pushed towards the semiconductor surface by the bias. When the surface of the semiconductor is n-type, UV light should be applied to generate electron-hole pairs since there are no available holes. Then the holes are pushed towards the semiconductor surface and electrons are pulled inside the semiconductor.

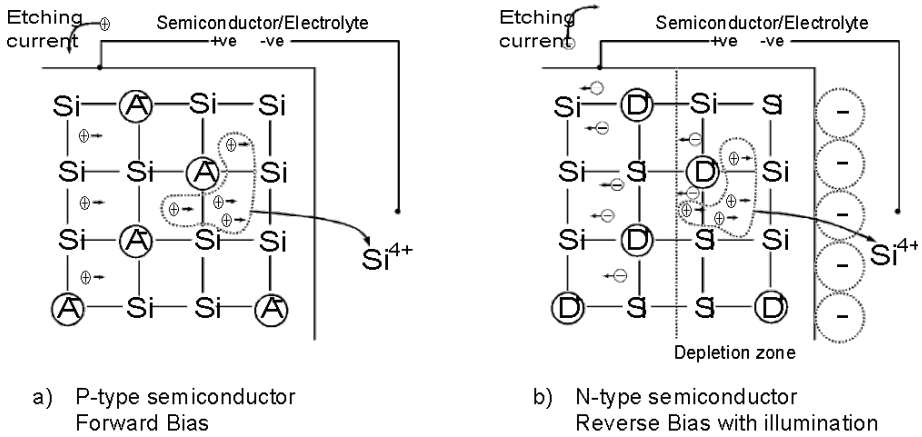


Figure 2.14 *ECV etching diagram of p-type and n-type silicon wafer [104]*

The semiconductor dissolution rate is controlled by the electric current flowing in/out of the semiconductor surface. The etched depth is calculated by Faraday's laws of electrolysis:

$$W_{etch} = \frac{M}{N_A q z \rho A} \int I(t) dt \tag{2.15}$$

M is the molar mass of the semiconductor, N_A is the Avogadro constant, z is the number of valency electrons per molecule/unit, ρ is the density of semiconductor, and $I(t)$ is the dissolution current that changes with time.

By repeating the two steps above, the doping profile of the semiconductor can be obtained. This method is destructive but the measurement depth is unlimited.

Compared with SIMS, the operation of ECV is less complex and no vacuum system is required. In addition, the ECV measurement result indicates the concentration of active dopants which directly determines the electrical properties of the semiconductor. Thus, an ECV profiler named Wafer Profiler CVP21 is utilized in our research.

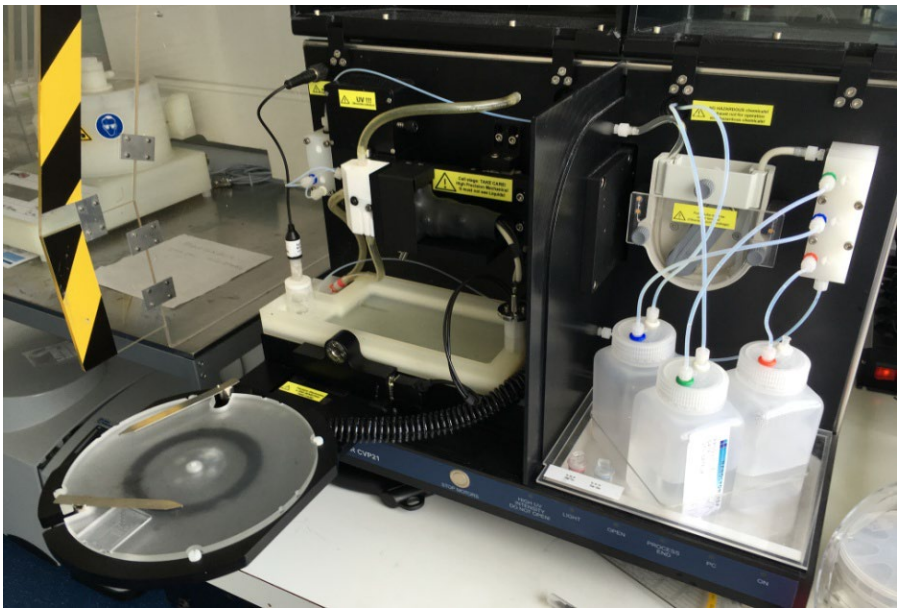


Figure 2.15 *Wafer Profiler CVP21*

2.3.2 *I-V* characterization

To study the electrical properties of the p^{++}/n^{++} tunnel junction, it is necessary to fabricate Si tunnel diodes and then measure their *I-V* performance. In this work, the *I-V* characterization of Si tunnel diodes is measured by a Keithley 4200-SCS Parameters Analyzer [105]. The Keithley 4200-SCS Parameter Analyzer delivers synchronizing *I-V*, capacitance-voltage (*C-V*), and ultra-fast pulsed *I-V* measurements. It is a turnkey system solution for the electrical characterization of devices.

When using the Keithley 4200-SCS Parameters Analyzer for the *I-V* characterization of Si tunnel diodes, the measurements are performed in dark conditions at room temperature. Two source measure units (SMUs) are used to connect the cathode and anode of the tunnel diode respectively. The SMU operates as a voltage or current source and simultaneously measures voltage and current with high resolution and accuracy. In this work, SMU operates as a voltage source and sweeping mode is applied. Linear forward voltage sweeps through the anode of the tunnel diode and *I-V* is measured.

Figure 2.16 *Keithley 4200-SCS Parameters Analyzer [105]*

2.4 Conclusion

In this chapter, four techniques used to fabricate Si tunnel junctions are first presented. After comparing these methods (MBE, CVD, ion implantation, and PRTD), we decided to use PRTD for our research due to its low cost and simplicity. When characterizing the doping profile of Si tunnel junctions, ECV is chosen because of the convenience of operation. It measures the concentration of active dopants which directly determines the electrical properties of the semiconductor. To characterize the electrical properties of Si tunnel junctions, a semiconductor characterization system named Keithley 4200-SCS Parameters Analyzer is applied. It measures the *I-V* performance of Si tunnel diodes fabricated based on the obtained tunnel junctions.

Chapter 3 Fabrication and characterization of the Si p^{++}/n^{++} tunnel junction

3.1 Introduction

In this chapter, the fabrication and characterization of the Si p^{++}/n^{++} tunnel junction are presented. The first section focuses on the investigation of different impact factors during the tunnel junction fabrication process. An optimized fabrication process of Si p^{++}/n^{++} tunnel junction is proposed at the end of the first section. The second section describes the fabrication and characterization of Si tunnel diodes. It demonstrates the electrical properties of the Si p^{++}/n^{++} tunnel junction fabricated by PRTD.

3.2 Study of parameters influencing tunnel junction fabrication process

To fabricate the Si p^{++}/n^{++} tunnel junction, highly doped n^{++} layer and p^{++} layer are required. Generally, P atoms are first doped into the Si substrate to form the n^{++} emitter. Then, B atoms are introduced to compensate P atoms near the surface and form the p^{++} layer. In this work, a series of (111)-oriented n-type Czochralski monocrystalline Si substrates with low resistivity (< 0.01 Ω·cm) are adopted to investigate the fabrication process of Si p^{++}/n^{++} tunnel junction. Several parameters that influence the fabrication process are studied and they are described in detail as follows.

3.2.1 Formation of the n^{++} emitter

First, the influence of the n^{++} emitter profile was studied. Standard phosphorus oxy-chloride ($POCl_3$) thermal diffusion was carried out to form the n^{++} emitter by a photovoltaic industrial technique (LYDOP, acronym for Leaktight Yield Doping). This step was realized at the CIME Nanotech (Centre Interuniversitaire de MicroElectronique et Nanotechnologies) in Grenoble. During this process, Si substrates were placed into the quartz furnace and were heated up to 875 °C and then held for 20 min. A flow of nitrogen is used as the carrier for the liquid dopant source $POCl_3$. Oxygen is also introduced into the furnace to form phosphorus pentoxide (P_2O_5) as well as prevent halogen pitting effects. The primary reactions in the furnace are shown as follow:

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \tag{3.1}$$

$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P \tag{3.2}$$

After thermal diffusion, a thin layer of phosphosilicate glass, also known as PSG by the acronym, formed on the surface of the Si substrate. This PSG layer can be removed by HF:

$$SiP_2O_7 + 6HF + H_2O \rightarrow H_2SiF_6 + 2H_3PO_4 \tag{3.3}$$

Thus, the wafers were cleaned by a sequence of chemical baths before ECV measurement:

- 1 min dip into 5% HF to remove the PSG layer;
- 15 min dip into piranha solution to oxidize the surface of the substrate, consuming few angstroms of Si wafer where impurities and contaminants might exist;
- 10 s dip into 5% HF to remove the oxidation layer formed by the piranha solution.

Each step was followed by DI water rinsing and N_2 drying. DI water rinsing and N_2 drying were carried out after each chemical bath. For simplicity, the rinsing and drying processes are omitted in the following text.

In this work, four series of n^{++} emitters were successively adopted for the research. The doping profiles of these four series of n^{++} emitters measured by ECV are shown in Figure 3.1. It shows that the concentration of active P atoms is around 4×10^{20} cm^{-3} near the surface of the first series of n^{++} emitters. The thickness of the layer with an electron concentration higher than 1×10^{20} cm^{-3} is more than 100 nm. Because the width of the first series of n^{++} emitters is too thick, the recipe of LYDOP has been adjusted to get thinner n^{++} emitters for the other three series. It should be noticed that there are slight differences between them due to the different $POCl_3$ thermal diffusion processes.

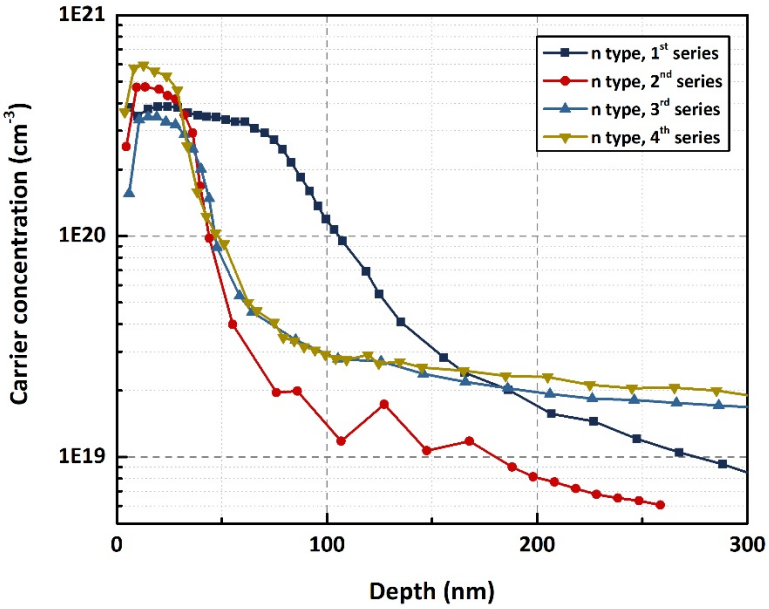


Figure 3.1 *ECV doping profile of four series of initial n^{++} emitters formed by $POCl_3$ diffusion under different conditions. The 1st series was doped at 875 °C for 20 min; The 2ed, 3rd, and 4th series were doped at 840 °C for 25 min.*

Si substrates with the first series of n^{++} emitters were first used as the target wafer to fabricate p^{++}/n^{++} tunnel junctions. The plateau temperature of PRTD was set as 1000 °C and kept for 15 s. After the B PRTD process, the target wafer was cleaned by HF (5%, 30 s), piranha (15 min), and HF (5%, 10 s) before ECV measurement. Holes or fewer electrons were expected to be detected near the surface. However, the electron concentration of the n^{++} emitter increased after B diffusion and no active B atoms were detected. The maximum electron concentration reaches 6.8×10^{20} cm^{-3} near the surface, as shown in Figure 3.2. It suggests that there might be a layer of Si containing plenty of inactive P atoms existing on the surface. This layer, generally known as the "dead zone", was formed during the thermal diffusion process of $POCl_3$ [106]-[108].

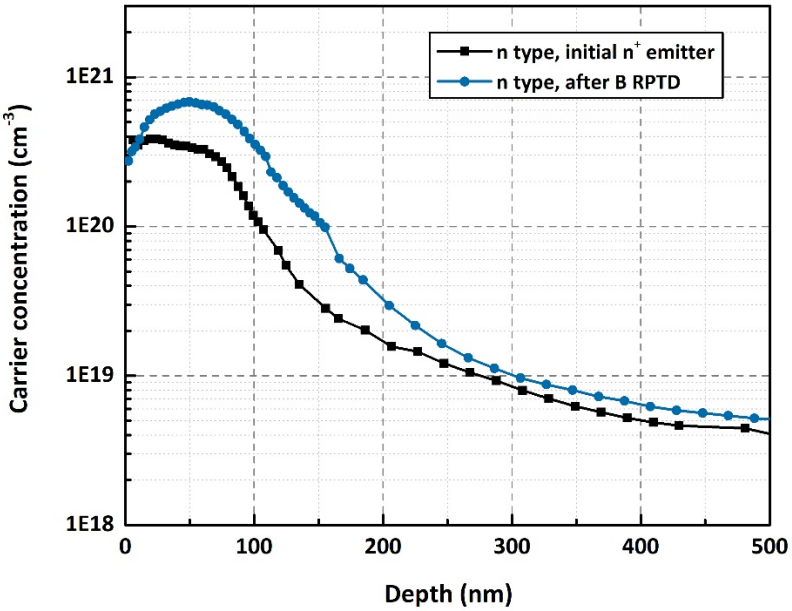


Figure 3.2 *ECV doping profile of initial n^+ emitter before and after a B PRTD at 1000 °C for 15 s*

To verify this presumption, an RTA without the B source wafer was carried out on the Si substrate with an n^{++} emitter. The substrate was annealed at 1000 °C for 15 s under air ambient. It was then characterized by ECV after the cleaning process. Figure 3.3 shows the resulting profile, very similar to the one in Figure 3.2, and that the maximum electron concentration near the surface is more than 1×10^{21} cm^{-3}. It demonstrates the existence of the "dead zone" where inactive P atoms were activated during the RTA process. Such a high n doping level, much higher than the solubility of B atoms in Si, prevents the realization of the tunnel junction. Therefore, this layer (around 100 nm) should be removed first to facilitate the compensation of B atoms for P atoms near the surface.

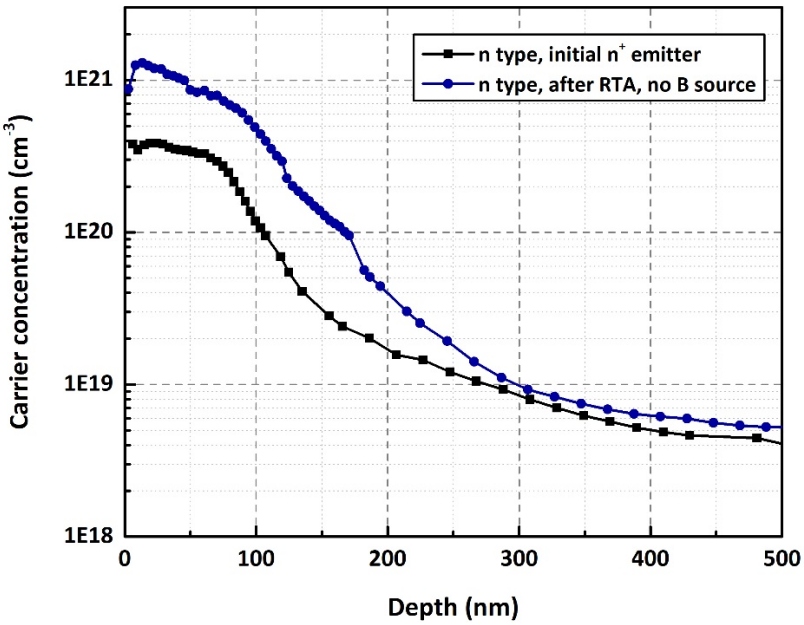


Figure 3.3 *ECV doping profile of initial n^{++} emitter before and after RTA without B source wafer at 1000 °C for 15 s*

3.2.2 Adjustment of n^{++} emitter

3.2.2.1 RIE etching

To remove the "dead zone" and reduce the thickness of the n^{++} emitter, reactive ion etching (RIE) is a feasible method that can remove the surface Si layer by etching. Therefore, Nextral NE 110 reactive ion etcher was applied to etch the n^{++} emitter. During the etching process, a gas mixture consisted of sulfur hexafluoride (SF_6) and argon (Ar) generated the plasma for etching Si. The flow rates of SF_6 and Ar were set as 5 sccm and 20 sccm respectively. The applied RF power was 60 W and the reaction took place under a chamber pressure of 15 mTorr. The Si etching rate was 90 nm/min according to the test result.

Two Si substrates with the same n^{++} emitters were etched for 90 nm and 120 nm separately to investigate the appropriate etching thickness. After etching, these two samples were cleaned by HF (5%, 10 s), piranha (15 min), and HF (5%, 10 s). The doping profiles of these two samples are shown in Figure 3.4 (a). Compared with the initial n^{++} emitter doping profile, the doping profiles of these two samples after etching shift the corresponding etching thickness. It shows that the real etching thicknesses are in accordance with the planned etching thicknesses. The "dead zone" and most of the P highly doped region have been

removed. Subsequently, they were used as the target wafers for B PRTD.

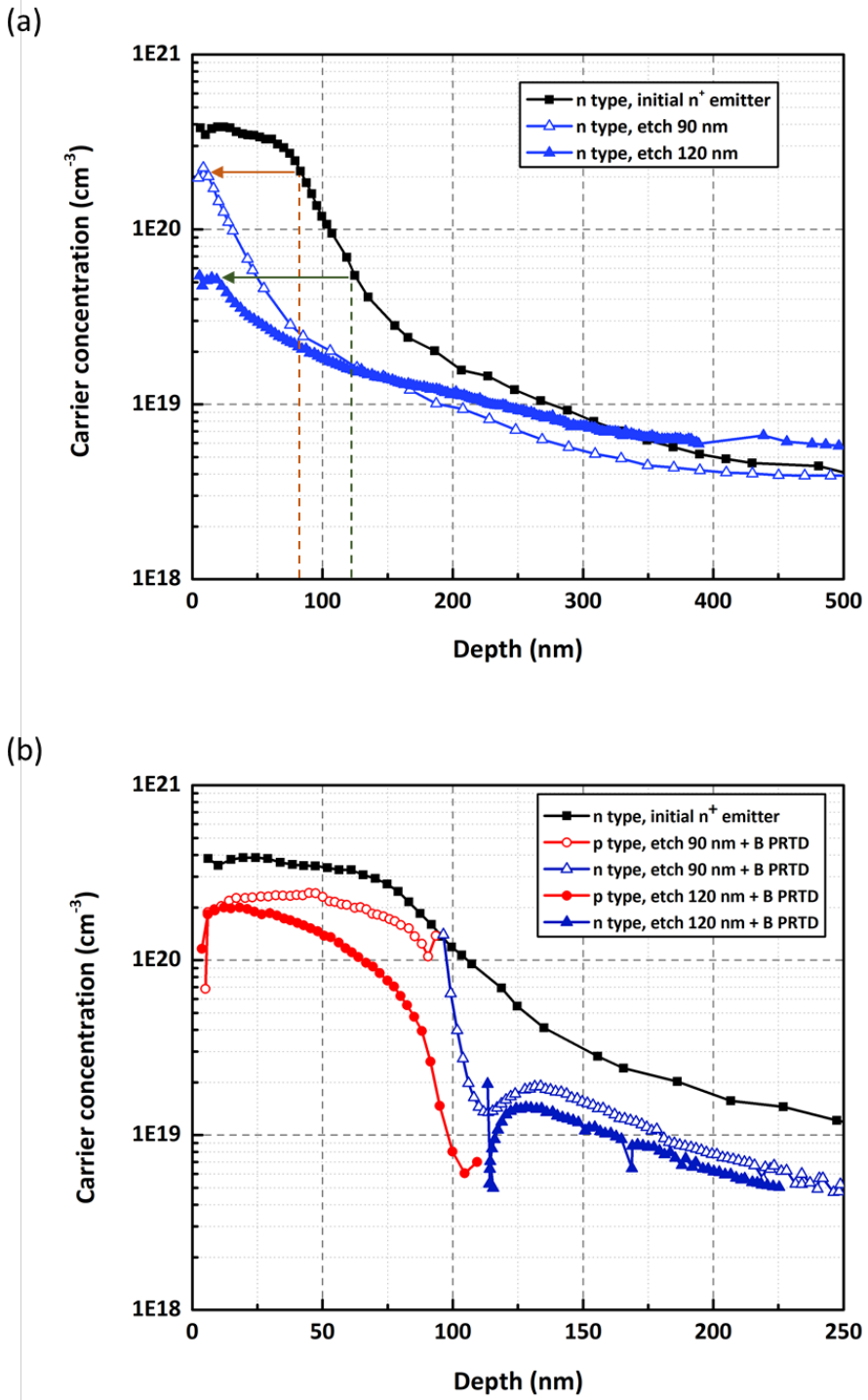


Figure 3.4 *(a) ECV doping profile of wafers etched for 90 nm and 120 nm; (b) ECV doping profile of wafers that are etched for 90 nm and 120 nm followed by B PRTD at 1020 °C for 15 s.*

The B PRTD was performed at 1020 °C for 15 s. After cleaning, holes were detected on both samples by ECV (Figure 3.4 (b)). The thicknesses of the p^{++}-layer are approximately 100 nm and the maximum carrier concentrations are both higher than 1×10^{20} cm^{-3}. It means that

the p^{++} layer for forming the tunnel junction has been achieved. However, the electron concentration of the n-type region near the junction is less than 2×10^{19} cm^{-3}, which is not sufficient to form the tunnel junction. It suggests that the n^{++} emitter should be etched less than 90 nm to preserve more P atoms near the surface.

Consequently, two other Si wafers with the same n^{++} emitter as above were etched by RIE for 60 nm. The same B PRTD was implemented on one of them. However, no holes were detected on this sample after B diffusion, suggesting the presence of excessive P atoms near the surface (Figure 3.5(a)). Therefore, the other wafer was further etched 20 nm, which means 80 nm in total, to remove more P atoms. Nevertheless, there are still no holes were detected after the same B PRTD process (Figure 3.5(b)). Compared with the result of sample etched 90 nm, it shows that a subtle adjustment of etching thickness may result in a very different doping result.

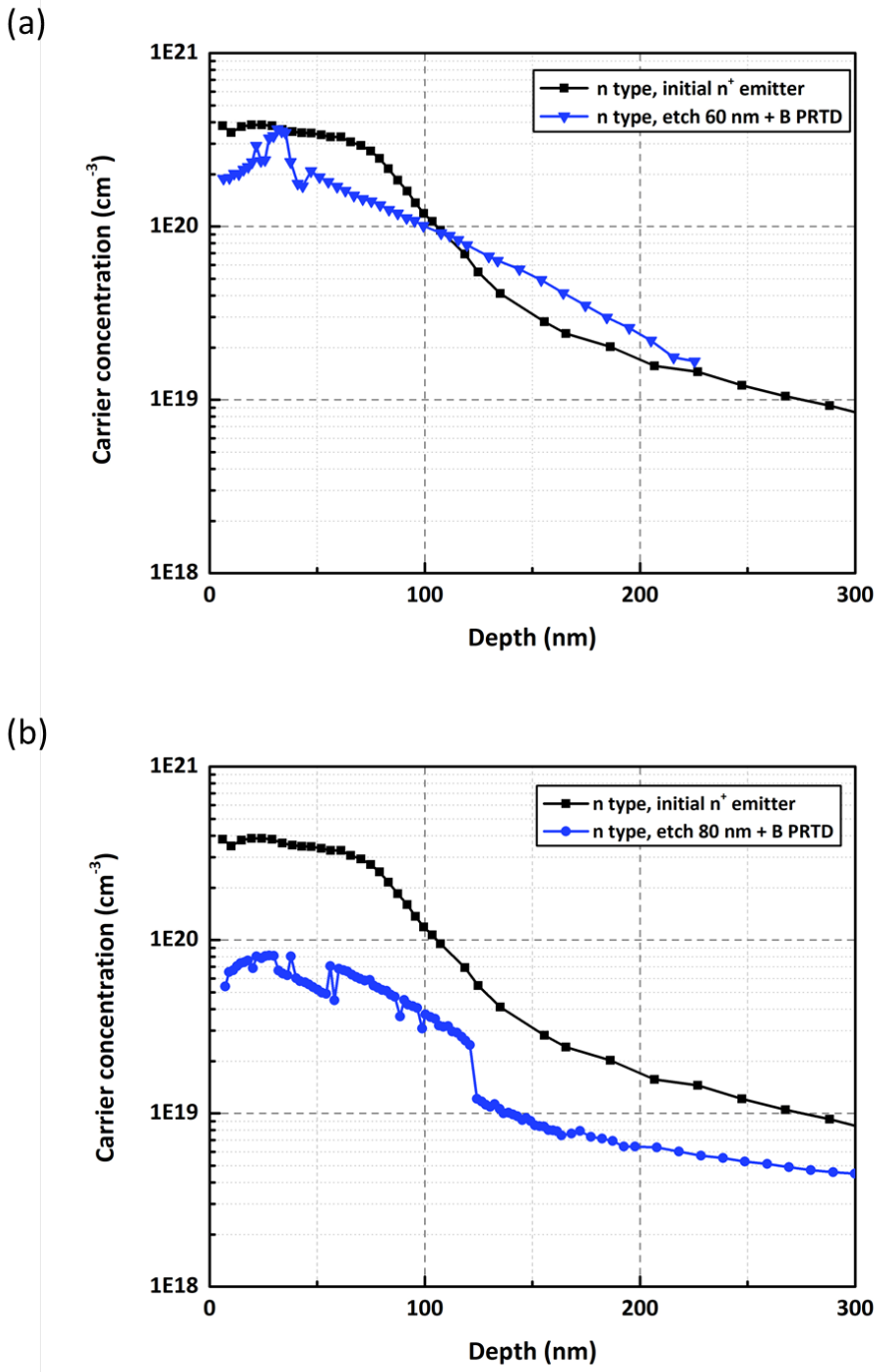


Figure 3.5 *(a) ECV doping profile of wafer etched for 60 nm and followed by B PRTD at 1020 °C for 10 s; (b) ECV doping profile of wafer etched for 80 nm and followed by B PRTD at 1020 °C for 10 s.*

The above results show that it is tricky to etch the appropriate thickness of the n^{++} emitter. If the emitter is excessively etched, the concentration of P atoms would be too low to form the tunnel junction. Conversely, no B atoms would be detected on the surface when the etching thickness is not enough. What's more, RIE introduces the lattice damage near the surface of the Si wafer and generates defect centers in the deeper layer [109]. Consequently, an

alternative approach is required to adjust the n^{++} emitter profile.

3.2.2.2 Two-step RTA in air and N_2

According to the literature, annealing in N_2 can lower the phosphorus surface concentration in Si wafer [102]. Therefore, we decided to adopt this method to reduce the n^{++} emitter doping concentration near the surface. RTA at 1020 °C under N_2 ambient was performed on two Si substrates with the second series of n^{++} emitter for 8 s and 15 s separately. Doping profiles show that the concentration of P atoms near the surface decreases after annealing in both cases, demonstrating that annealing in N_2 has effectively reduced the effect of the "dead zone" (Figure 3.4 (a)). The doping level of the one annealed for 15 s is lower than the one annealed for 8 s near the surface. This phenomenon is caused by the exodiffusion of P atoms. During the annealing process, surface P atoms can leave the Si wafer and escape into the gaseous ambient. As a result, both active and inactive P atoms on the surface are reduced.

Whereas, the P concentration of the one annealed for 15 s is higher than the one annealed for 8 s in a certain region away from the surface, which is significant between 40 nm and 120 nm. It is because the diffusion into Si wafer and exodiffusion into gaseous ambient occur simultaneously for P atoms. Therefore, when time increases, the concentration of P atoms decreases on the surface while increases in the deeper region.

Afterwards, B PRTD was carried out on these two substrates after cleaning and holes were only detected on the one annealed for 15 s (Figure 3.4 (b)). For the one annealed in N_2 for 8 s, no holes were detected and the electron concentration decreased to 9×10^{18} cm^{-3} near the surface. It shows that the exodiffusion of P atoms for 8 s is not enough to obtain an appropriate emitter for B atoms to compensate. For the one annealed for 15 s, the concentration of holes reaches 8×10^{19} cm^{-3} while the concentration of electrons reaches 9×10^{19} cm^{-3} near the junction. It suggests that RTA in N_2 for 15 s can make the n^{++} emitter suitable to later form the tunnel junction.

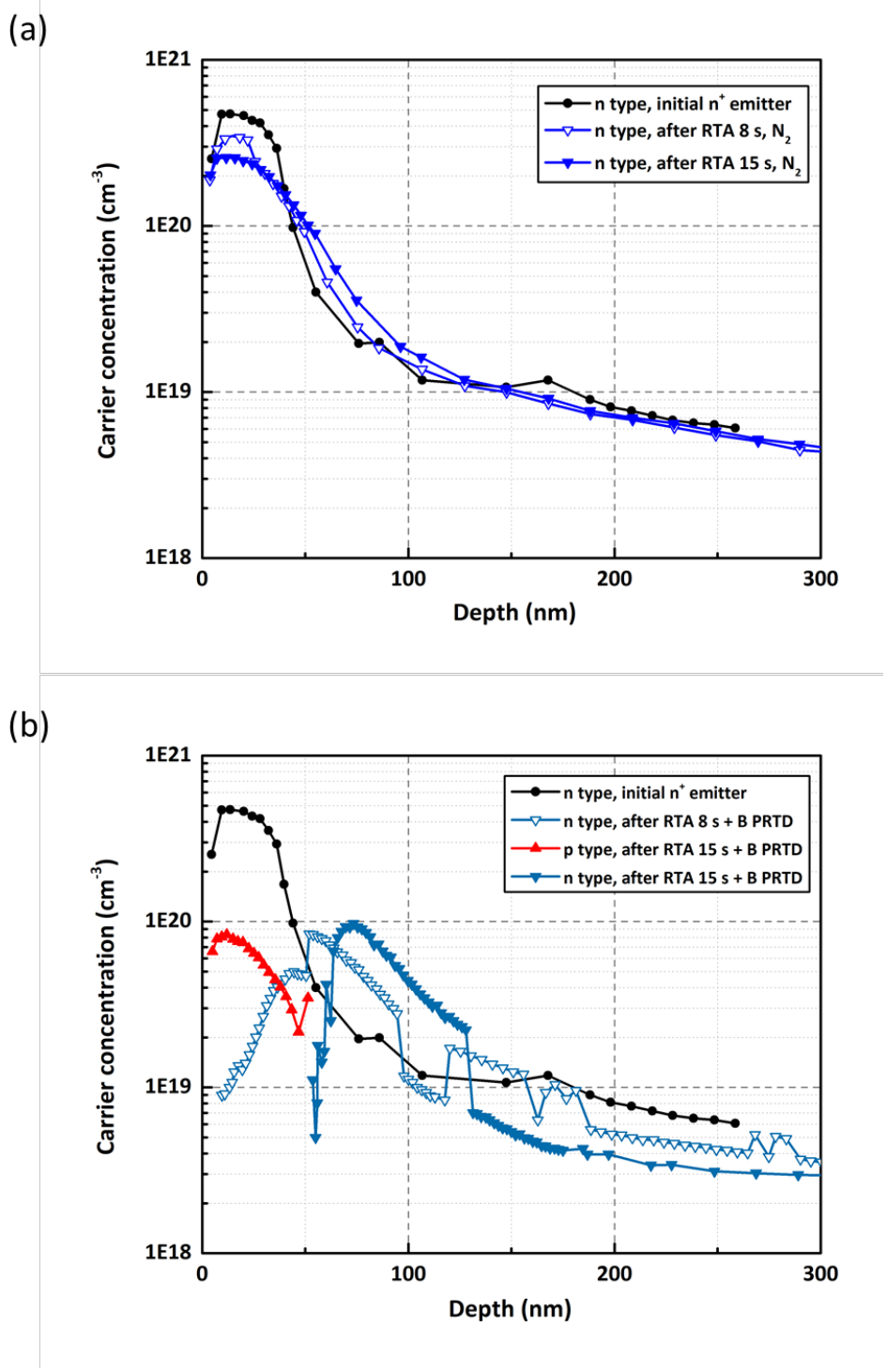


Figure 3.6 *(a) ECV Doping profile of n^+ emitter after RTA at 1020 °C under N_2 ambient for 8 s and 15 s; (b) ECV doping profile of n^+ emitter after RTA at 1020 °C under N_2 ambient for 8 s and 15 s and then followed by B PRTD at 1020 °C for 10 s.*

However, when B PRTD was carried out on other same n^{++} emitters annealed in N_2 for 15 s, fewer B atoms or no B atom was detected near the surface (Figure 3.7). It shows that the unavoidable subtle differences during the RTA and B PRTD processes can lead to varied results.

Therefore, the tunnel junction fabrication process needs to be carefully optimized to guarantee reproducibility when the n^{++} emitter profile is modified, even slightly.

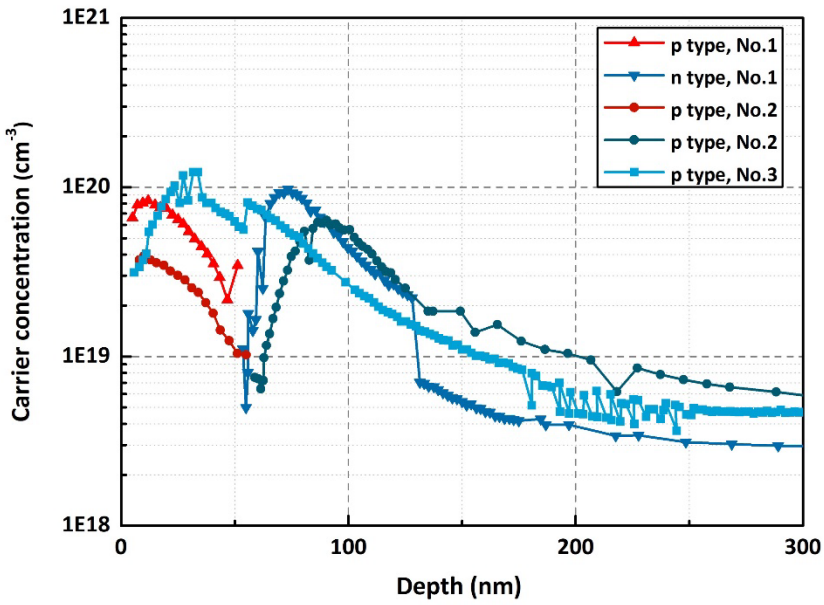


Figure 3.7 *ECV doping profile of three samples (named No.1, No.2, and No.3) with same initial emitter after RTA at 1020 °C under N_2 flow for 15 s and then followed by B PRTD at 1020 °C for 10 s.*

Apart from the "dead zone" near the surface, abrupt change of the initial n^{++} emitter profile is also a threat to the fabrication of p^{++}/n^{++} tunnel junction. RTA in air ambient was carried out to solve this problem. A Si substrate with n^{++} emitter was annealed at 1020 °C for 15 s in air. After annealing, significant redistribution of P atoms was observed (Figure 3.8). P atoms near the surface diffused deeper into the wafer hence the doping profile became relatively flat.

Compared with the one annealed in N_2 for the same time, the active P atoms concentration of the one annealed in the air is higher both near and away from the surface. It is due to the formation of silicon oxide at the surface in the air ambient. Because the segregation coefficient of P atoms in the Si-SiO_2 system is bigger than 1, which means that the equilibrium concentration of P atoms in Si is higher than the equilibrium concentration of P atoms in SiO_2, the growing oxide layer prevented the exodiffusion of P atoms [110]. In addition, the diffusivity of P atoms in SiO_2 is lower than the diffusivity of P atoms in Si, resulting in a pileup of P atoms formed at the silicon surface.

Meanwhile, the doping profile shows that P atoms diffuse into the silicon wafer faster in

an air ambient than in N_2. The diffusivity of P atoms increases significantly in air ambient for the reason that it is dominated by the interstitialcy mechanism. In the oxidizing ambient, incomplete oxidation occurs at the Si-SiO_2 interface, resulting in the generation of silicon interstitials in excess of equilibrium value. As mentioned in Chapter 2, interstitialcy diffusion is a modified version of substitutional diffusion with the participation of self-interstitials. Therefore, an increased concentration of silicon interstitials enhances the diffusivity of P atoms.

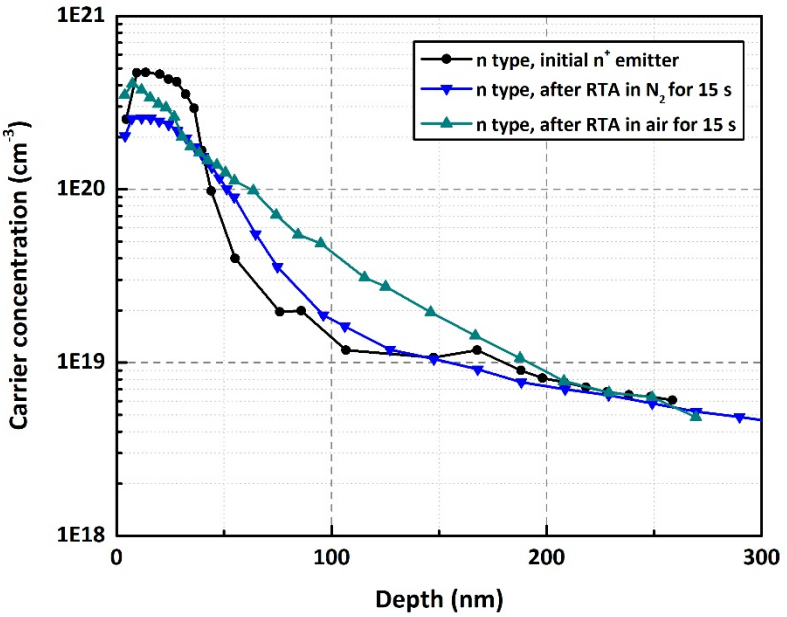


Figure 3.8 *ECV doping profile of n^{++} emitter after RTA under N_2 and air ambient at 1020 °C for 15 s separately*

Considering the above results, we propose a two-step RTA consisting of RTA in N_2 and air to adjust the profile of a standard n^+ emitter. RTA in N_2 can reduce the concentration of P atoms, while RTA in the air can lead to the redistribution of P atoms. The doping profiles of the n^{++} emitter before and after two-step RTA are shown in Figure 3.9. The initial n^{++} emitter is slightly different from the above emitter. The annealing temperature was set as 1020 °C. The n^{++} emitter shown in Figure 3.9 (a) was first annealed under N_2 flow for 60 s and then annealed under air flow for 30 s. While the n^{++} emitter shown in Figure 3.9 (b) was first annealed under air flow for 30 s and then annealed under N_2 flow for 60 s. After two RTAs, a significant difference between the two n^{++} emitter doping profiles is observed, showing the impact of the order of these two RTAs. Therefore, the order of RTA in N_2 or air can be changed according to the emitter profile. This 2 RTAs combination will allow the adjustment of the n-type profile for

effective incorporation of B atoms to form the desired p^{++}/n^{++} tunnel junction.

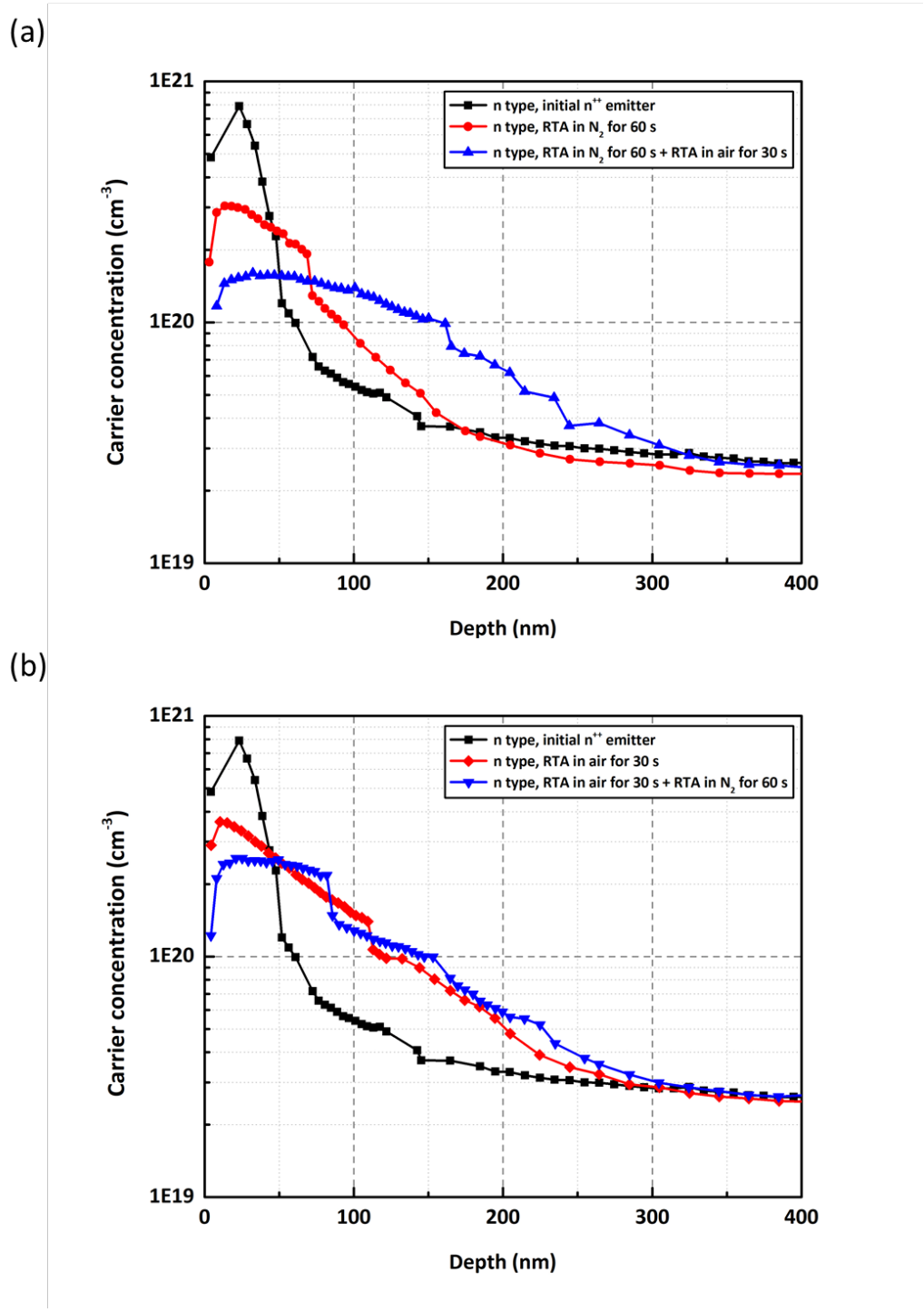


Figure 3.9 *ECV doping profiles of the n^{++} emitter before and after two different two-step RTA processes: (a) First annealed under N_2 flow for 60 s and then annealed under air flow for 30 s; (b) First annealed under air flow for 30 s and then annealed under N_2 flow for 60 s. The annealing temperature was all set as 1020 °C.*

3.2.3 RTA temperature and time of B diffusion process

To compensate active P atoms with a doping concentration higher than 1×10^{20} cm^{-3},

abundant B atoms should be introduced into the Si wafer. Therefore, as a preliminary study, B deposition was carried out on n-type Si substrates without an n^{++} emitter to study the diffusion behavior of B atoms.

(100)-oriented prime Si wafers with a resistivity of 1-20 Ω·cm were adopted to prepare the B source wafers. These wafers were cleaned by HF (5%, 20 s) and piranha solution (15 min) to form a hydrophilic layer on the surface. Then Borofilm100 was deposited and spread homogeneously on the Si wafers by spin-on doping. The spinning acceleration is 400 rpm/s and the maximum spinning speed is 3000 rpm. The total time of acceleration and spinning at maximum speed is 30 s. The wafers were subsequently baked at 200 °C for 10 min to evaporate the solvent. After this, a solid SOD layer of ~ 190 nm formed on the surface of B source wafers and it would transfer into borosilicate glass (BSG) during the diffusion process. The (111)-oriented n-type Si substrates used as target wafers were cleaned by HF (5%, 30 s), piranha (15 min), and HF (5%, 10 s) successively just before PRTD.

During the PRTD process, the B source wafer and target wafer were stacked vertically in the furnace of ADDAX, as shown in Figure 2.9. They were separated by 280 µm-Si spacers. The PRTD was implemented under air flow (75% N_2: 25% O_2). Same as the diffusion of P atoms in Si, the diffusion of B atoms in Si is also dominated by the interstitialcy mechanism. The diffusivity of B atoms in silicon can be enhanced with the presence of oxygen.

Firstly, the plateau temperature was set as 950 °C, 1000 °C, and 1020 °C respectively, with a duration time of 10 s. After PRTD, the target wafers were cleaned by HF (5%, 30 s), piranha (15 min), and HF (5%, 10 s). The doping profiles characterized by ECV after cleaning are shown in Figure 3.10. It presents the hole concentration of target wafers, corresponding to the concentration of active B atoms.

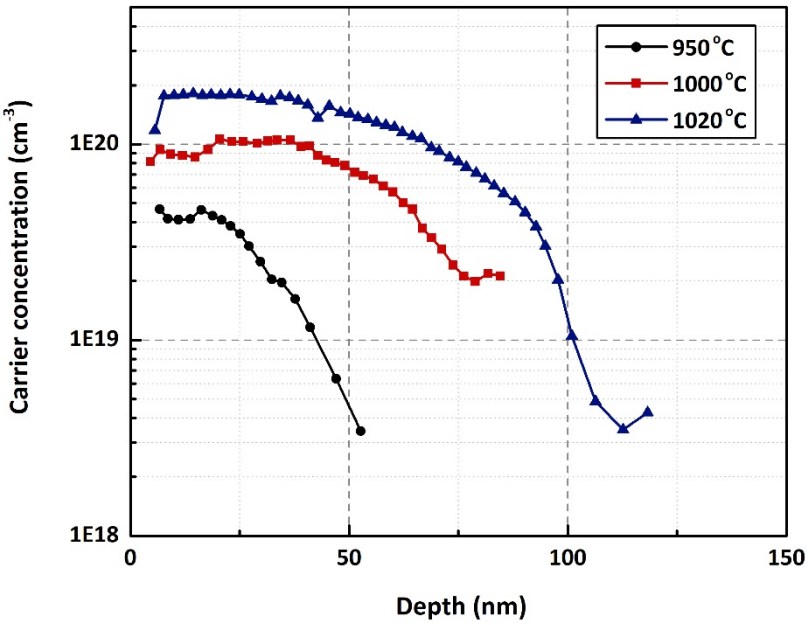


Figure 3.10 *ECV doping profile of active B atoms achieved by B PRTD, with a plateau time of 10 s and plateau temperature of 950 °C, 1000 °C, and 1020 °C respectively.*

The result shows that both the doping concentration and doping depth of B increase with the temperature. This phenomenon is caused by two factors, solubility and diffusivity of B atoms in Si. The solubility curve of common dopants in (111)-oriented Si is shown in Figure 3.11. It demonstrates that the solubility of B atoms in Si increases with temperature under 1100 °C. Thus, more B atoms can be introduced into Si when the temperature changes from 950 °C to 1020 °C, increasing the concentration of holes.

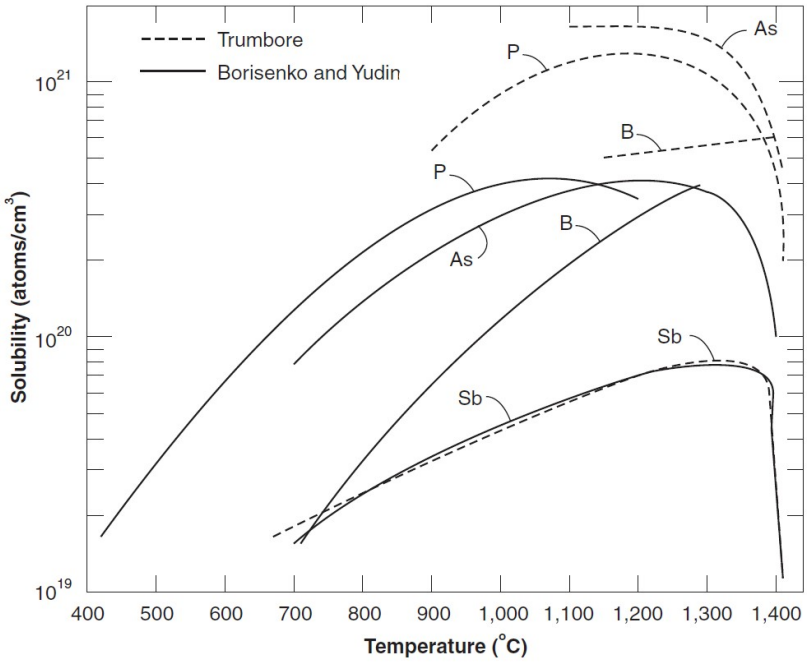


Figure 3.11 *Solid solubility of common dopants in (111) silicon [110]-[112]*

The diffusion depth of B atoms depends on the diffusivity of B in Si. As mentioned in section 2.2.4.1, the diffusion of B atoms in Si is dominated by the interstitialcy mechanism. Intrinsic diffusion occurs when the B doping concentration is less than the intrinsic carrier concentration, which is independent of dopant concentration [113]. The intrinsic diffusivity of B atoms in Si is given by [110], [113]:

$$D_i = 0.76e^{-3.46/kT}\ \mathrm{cm}^2/\mathrm{s} \tag{3.4}$$

where D_i is the intrinsic diffusivity, k is the Boltzmann's constant, and T is the temperature in degrees Kelvin.

When the B doping concentration is higher than the intrinsic carrier concentration, extrinsic diffusion which is dependent on the carrier concentration occurs. The extrinsic diffusivity of B in Si is given by:

$$D_x = D^0 + D^+\left[\frac{p}{n_i}\right] \tag{3.5}$$

where

$$D^0 = 0.037e^{-3.46/kT}\ \mathrm{cm}^2/\mathrm{s} \tag{3.6}$$

and

$$D^+ = 0.76e^{-3.46/kT}\ \mathrm{cm}^2/\mathrm{s} \tag{3.7}$$

Here D_x is the extrinsic diffusivity, D^0 is the neutral vacancy - impurity diffusion, D^+ is the

positively charged vacancy-impurity diffusion, p is hole concentration and n_i is the intrinsic carrier concentration.

The diffusivity of B atoms in Si versus temperature is plotted in Figure 3.12. It shows that the diffusivity of B atoms increases as the temperature increases. Meanwhile, the diffusivity increases with the increasing boron concentration when the temperature is the same. It could explain why B atoms diffuse more deeply in silicon when temperature increases.

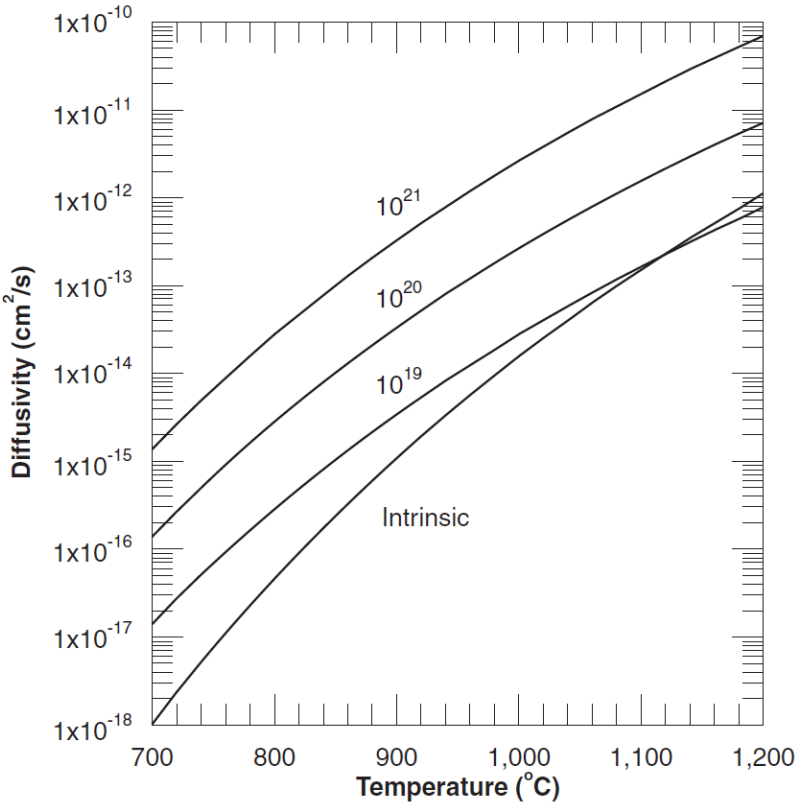


Figure 3.12 *Diffusivity of boron in silicon versus temperature and boron concentration, the unit of boron concentration is cm^{-3}. [110]*

Considering that a high as well as shallow doping profile is required to form the tunnel junction, 1000 °C - 1020 °C is appropriate for B diffusion.

Secondly, the effect of PRTD time on B diffusion was studied. According to the above result, the plateau temperature was kept as 1020 °C while plateau time varied from 10 s to 30 s. The target wafers were also cleaned by HF (5%, 30 s), piranha (15 min), and HF (5%, 10 s) before ECV measurement. Active-B doping profiles are shown in Figure 3.13. It indicates that for diffusion time up to 20 s, surface concentration is stable while doping depth increases. When increasing time up to 30 s, then surface doping concentration is decreased. The distributions of B atoms are consistent with the limited impurity source diffusion profiles

shown in Figure 2.7.

Therefore, as a conclusion of these preliminary experiments, the PRTD of the B atoms should be carried out at a plateau temperature of 1000 °C - 1020 °C for 10 - 15 s to form a high as well as shallow B doping layer.

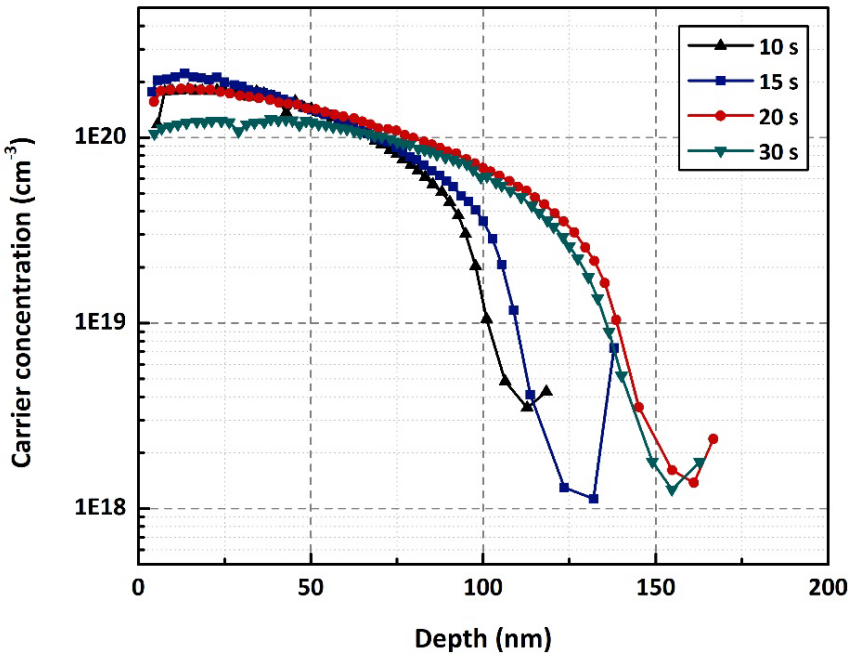


Figure 3.13 *ECV doping profile of active B atoms achieved by B PRTD, with a plateau temperature of 1020 °C and plateau time of 10 s, 15 s, 20 s, and 30 s respectively.*

After the adjustment of n^{++} emitter and the investigation of B PRTD process, a two-step RTA and B PRTD was performed on a Si wafer with an n^{++} emitter to fabricate the p^{++}/n^{++} tunnel junction. The Si wafer was first annealed in air at 1020 °C for 15 s and then it was cleaned by HF (5%, 30 s), piranha (15 min), and HF (5%, 10 s). The second RTA was carried out in N_2 at 1020 °C for 15 s. After another cleaning, B PRTD was realized in the air at 1020 °C for 10 s. The final doping profile of this sample is shown in Figure 3.14. B atoms were detected on the surface and the depth of tunnel junction is around 60 nm. The concentration of active B atoms is ~ 1.2×10^{20}-2×10^{20} cm^{-3} near the surface, while the concentration of active P atoms is ~ 1×10^{20}-1.2×10^{20} cm^{-3} near the depletion region. Both of them are high enough to meet the requirement of forming a tunnel junction. The width of the depletion region is about 4.6-5.3 nm according to the calculation:

$$W_{depl} \simeq \sqrt{\frac{2\varepsilon_r \varepsilon_0 V_d}{q}\left(\frac{1}{N_D}+\frac{1}{N_A}\right)} \tag{3.8}$$

$$V_d = \left(\frac{k_0 T}{q}\right) ln \frac{N_D N_A}{{n_i}^2} \tag{3.9}$$

where ε_r is the relative permittivity of Si, ε_0 is the vacuum permittivity, q is the elementary charge, N_D is the concentration of active P atoms, N_A is the concentration of active B atoms, k_0 is the Boltzmann constant, T is the temperature equals to 300 K and n_i is the intrinsic carrier concentration of Si at 300 K. This result demonstrates that p^{++}/n^{++} tunnel junction can be realized by B PRTD after a two-step RTA.

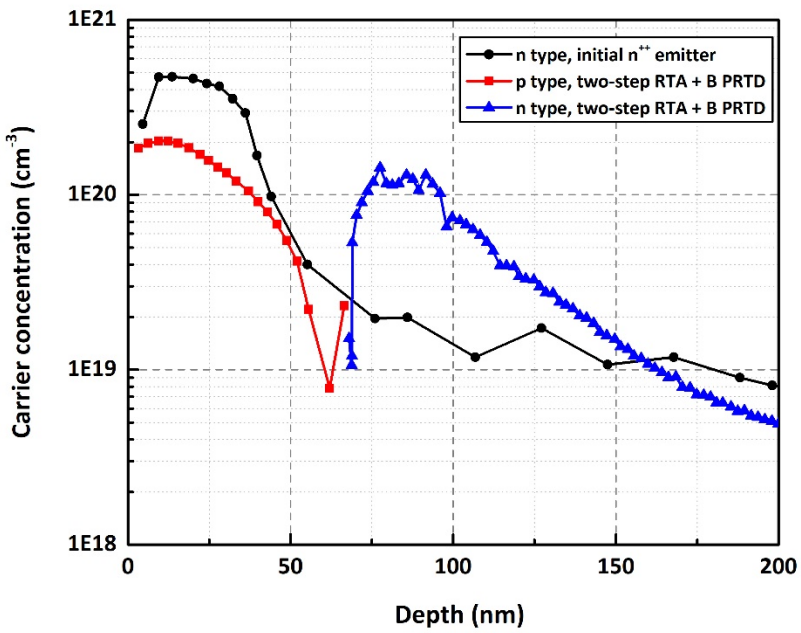


Figure 3.14 *ECV doping profile of Si wafer after two-step RTA, under N_2 and air ambient at 1020 °C for 15 s separately and then followed by B PRTD at 1020 °C for 10 s.*

3.2.4 Cleaning process

The cleaning process was also observed to affect the fabrication of tunnel junction except for the B PRTD process and n^{++} emitter profile. Generally, the Si wafer is cleaned by HF (5%), piranha solution (15 min), and HF (5%) before and after each annealing process. Since piranha solution is a mixture of concentrated H_2SO_4 and H_2O_2, which is hazardous, extreme caution is required during the cleaning procedure. Considering the safety and convenience of operation, UV/ozone cleaner was used instead of the piranha solution. Both piranha solution and

UV/ozone cleaner can remove the organics from the surface of the Si wafer. Moreover, they can oxidize the superficial Si substrate where impurities and contaminants might exist.

Thus to compare these two cleaning procedures, a Si wafer with n^{++} emitter was cut into two pieces and then annealed at 1020 °C for 15 s in air ambient. One piece of them was cleaned by HF (5%) + piranha (15 min) + HF (5%) before and after the RTA process. While the other one was cleaned by HF (5%) + UV/ozone (15 min) + HF (5%). Completely different doping profiles were observed on these two samples after annealing, as shown in Figure 3.15. The doping profile of the one cleaned by UV/ozone increased dramatically. It might be caused by the residual of the "dead zone" on the surface. A large number of inactive P atoms existing in the "dead zone" were activated during the RTA process. As the formation of silicon oxide at the surface rejected the exodiffusion of P atoms, the excess atoms diffused deeper into the Si wafer.

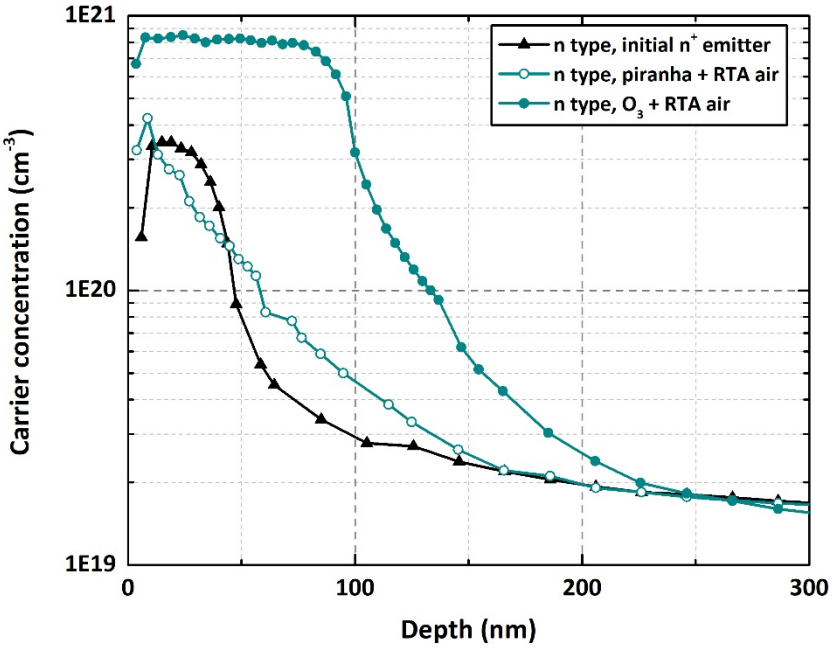


Figure 3.15 *ECV doping profile of Si wafer after cleaned by HF (5%) + piranha (15 min) + HF (5%) or HF (5%) + UV/ozone (15 min) + HF (5%) and then RTA under air ambient at 1020 °C for 15 s.*

To verify this assumption, the same process as above was carried out on two other Si wafers, except that the RTA ambient was changed to N_2. After annealing, the doping profile of the one cleaned by UV/ozone is higher than the one cleaned by piranha near the surface. Whereas, both doping profiles decreased after annealing. It indicates that both active and

inactive P atoms escape into the gaseous ambient during the RTA process under an N_2 environment.

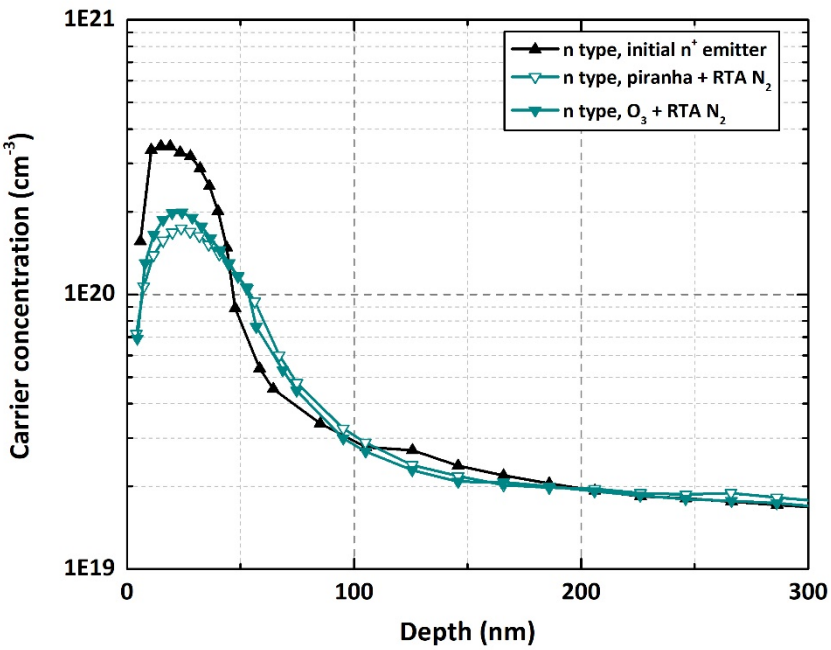


Figure 3.16 *ECV doping profile of Si wafer after cleaned by HF (5%) + piranha (15 min) + HF (5%) or HF (5%) + UV/ozone (15 min) + HF (5%) and then RTA under N_2 ambient at 1020 °C for 15 s.*

Given these two different results, we speculated that the silicon oxidizing capacity of UV/ozone is lower than that of piranha. During the cleaning process before annealing, a superficial layer of Si was oxidized by piranha or UV/ozone and then removed by HF. As a result, the "dead zone" was totally or partially removed depending on the thickness of silicon oxide. Ellipsometer was used to measure the thickness of the silicon oxide layer after piranha or UV/ozone cleaning. However, the thickness of silicon oxide is around 2 nm in both cases and accurate values were not achieved.

Therefore, an indirect method was applied to reflect the oxidation capacity of piranha and UV/ozone. A Si wafer with the same n^{++} emitter as above was cut into two pieces and then annealed at 1020 °C for 15 s in air ambient. One piece of them was cleaned by HF (5%) + piranha (35 min) + HF (5%) before and after the RTA process. While the other one was cleaned by HF (5%) + UV/ozone (75 min) + HF (5%). The doping profiles of them after annealing were shown in Figure 3.17. It shows that the doping profile decreases as the cleaning time of UV/ozone increases from 15 min to 75 min. The doping profile of the one cleaned by piranha

for 15 min is between the one cleaned by UV/ozone for 35 min and 75 min. It indicates that the silicon oxidizing capacity of UV/ozone cleaner is lower than that of piranha solution. The silicon oxide layer formed in piranha solution during 15 min is thicker than that formed in UV/ozone cleaner during 15 min. Consequently, it was decided to replace the 15 minutes of piranha cleaning with 60 minutes of UV/ozone cleaning.

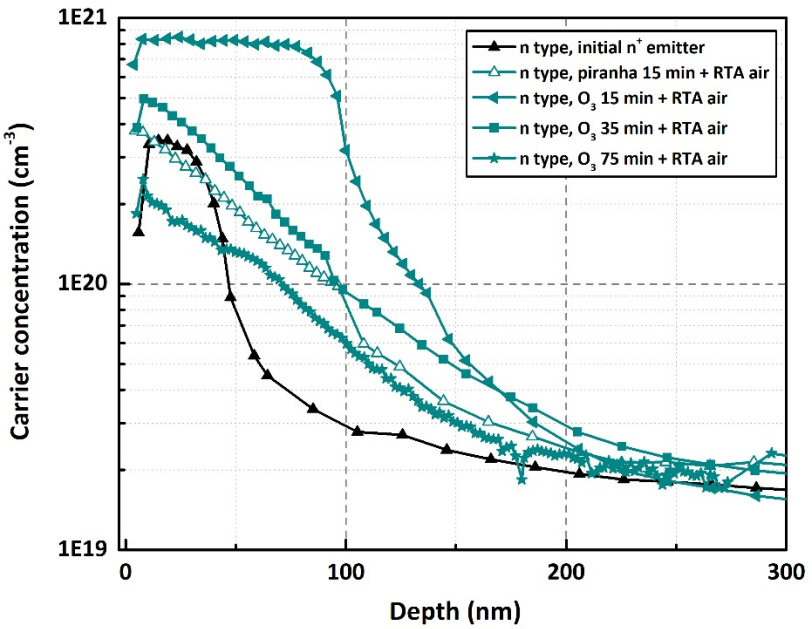


Figure 3.17 *ECV doping profile of Si wafer after cleaned by HF (5%) + UV/ozone + HF (5%) and then RTA under N_2 ambient at 1020 °C for 15 s. The time of the UV/ozone process is 15 min, 35 min, or 75 min separately.*

To demonstrate the effectiveness of 60 min-UV/ozone cleaning, two-step RTA and a subsequent B PRTD were performed on a Si wafer with an n^{++} emitter. The Si wafer was cleaned by HF (5%) + UV/ozone (60 min) + HF (5%) before and after each annealing process. A p^{++} type layer of ~40 nm was observed near the surface after the whole procedure. The concentration of active B atoms is ~ 2×10^{20} cm^{-3} while that of active P atoms is ~ 1×10^{20} cm^{-3} near the depletion region (Figure 3.18). This result demonstrates that 15 minutes of piranha solution can be replaced by 60 minutes of UV/ozone cleaner during the chemical cleaning process of the Si wafer.

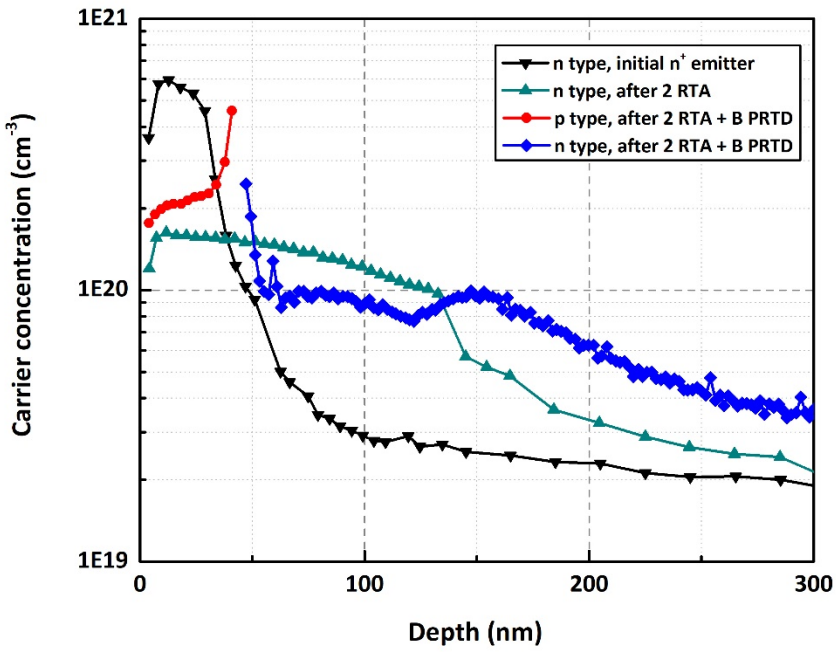


Figure 3.18 *ECV doping profile of Si wafer after two-step RTA, under N_2 and air ambient at 1020 °C for 15 s separately and then followed by B PRTD at 1020 °C for 10 s. The wafer was cleaned by HF (5%) + UV/ozone (60 min) + HF (5%) before and after each annealing process.*

3.2.5 Spin-on speed to make B source wafer

In addition to the factors mentioned above, the spinning speed to make the B source wafer also affects the formation of the p^{++}/n^{++} tunnel junction. Generally, the spinning speed is 3000 rpm for Borofilm100. In consideration of the high concentration of P atoms near the surface, the spinning speed might be reduced to 2000 rpm to introduce more B atoms into SOD film.

Thus, two Si substrates cleaned by HF (5%, 10 s) and piranha (15 min) were prepared for Borofilm100 deposition. The spinning speed was set as 2000 rpm and 3000 rpm separately. After baking, homogeneous SOD films were obtained on both substrates. Then ellipsometer was adopted to measure the thickness of SOD films. It is ~ 190 nm for the one of 2000 rpm while ~ 160 nm for the one of 3000 rpm. These two wafers were then used as B source wafers in the same B PRTD process. The doping profile of them is shown in Figure 3.19 after B diffusion. Higher concentration and deeper depth of B atoms are observed on the one with a B source wafer of 2000 rpm above. It shows that the spinning speed of making B source wafer obviously affects the formation of p^{++}/n^{++} tunnel junction. Different spinning speeds can be set

depending on the initial n^{++} emitter profile.

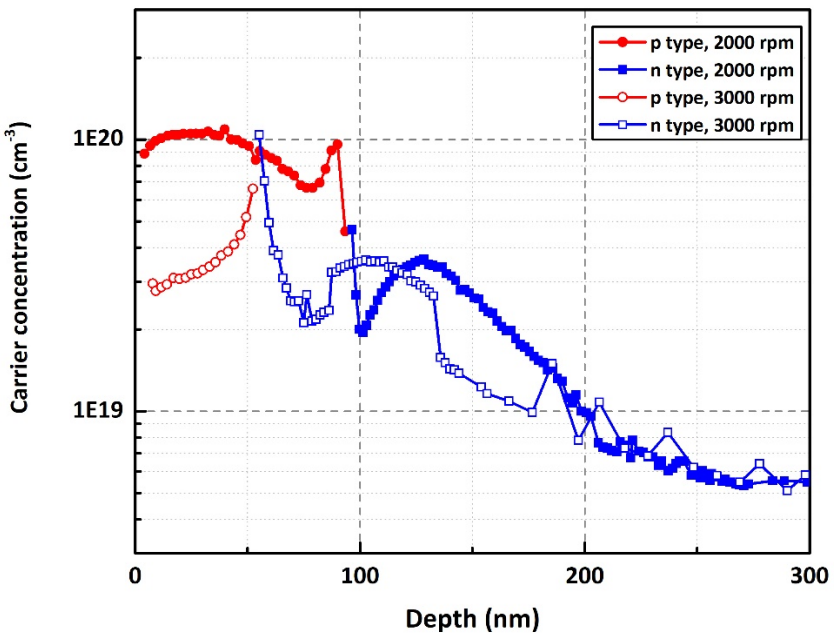


Figure 3.19 *ECV doping profiles of Si wafers after B PRTD. The B source wafers are obtained by a spinning speed of 2000 rpm or 3000 rpm.*

3.2.6 Optimized fabrication process

After investigating all the factors mentioned above, the optimized fabrication process of Si p^{++}/n^{++} tunnel junction is shown in Table 3.1 and is described in detail as follows.

The first step is the preparation of the n^{++} emitter. It is produced by traditional $POCl_3$ thermal diffusion through LYDOP. However, this step results in the formation of a “dead zone” presenting excessive P atoms near the surface, avoiding compensation when incorporating B atoms. Therefore, an adjustment of this n^{++} emitter profile is realized by a two-step RTA. Generally, the first RTA is carried out under N_2 flow at 1020 °C for 15 s in order to exodiffuse the P atoms from the “dead zone”. The second RTA is carried out under air flow at 1020 °C for 15s to redistribute P atoms, resulting in a relatively smoother doping profile. The time and temperature of RTA can be slightly changed according to the initial n^{++} emitter profile. The order of the two annealings can also be exchanged. The Si wafer is cleaned by HF (5%) + UV/ozone (60 min) + HF (5%) before and after each annealing process.

Secondly, the B source wafer is prepared by the spin-on doping of Borofilm 100 solution on Si substrate. Normally, the spinning acceleration is set as 400 rpm/s and the spinning speed

is set as 3000 rpm. The total time of acceleration and spinning at maximum speed is 30 s. As a result, ~ 160 nm of SOD film is obtained. While the spinning speed can also be decreased to 2000 rpm to form a SOD film of ~ 190 nm if the doping level of the n^{++} emitter is too high.

The final and crucial step is the B PRTD. This process has to be performed under air flow. The temperature of B PRTD changes between 1000 °C to 1020 °C. The time of the B PRTD is 10-15 s.

As a result of these steps, a p^{++}/n^{++} tunnel junction with a damage-free surface on (111)-oriented Si wafer can be obtained. In addition, similar results can be obtained in (100)-oriented Si wafers.

Table 3.1 *Optimized parameters of Si p^{++}/n^{++} tunnel junction fabrication process*

Process	**Optimized parameters**	
Cleaning	HF (5%) + UV/ozone (60 min) + HF (5%) + DI water rinse	
SOD of Borofilm 100	Acceleration (rpm/s)	400
	Spin speed (rpm)	2000 or 3000
	Total time (s)	30
Two-step RTA	Temperature (°C)	1020
	Time (s)	15
	Ambient	1st N_2, 2ed air or reverse
B PRTD	Temperature (°C):	1000-1020
	Time (s)	10-15
	Ambient	Air

3.3 *I-V* characterization of the tunnel junction

3.3.1 Fabrication and characterization of tunnel diodes with vertical tunnel junction

Si tunnel diode was fabricated to characterize the electrical properties of p^{++}/n^{++} tunnel junction. A vertical p^{++}/n^{++} tunnel junction was prepared on an n-type 2-inch (111)-oriented Si substrate with a resistivity of ~ 0.01 Ω·cm. The doping profile of the tunnel junction is shown in Figure 3.20. The depth of the tunnel junction is around 80 nm. The concentration of active B atoms is ~ 8×10^{19}- 1.7×10^{20} cm^{-3} near the surface, while the concentration of active P atoms

is ~ 5×10^{19}-8×10^{19} cm^{-3} near the depletion region. The width of the depletion region is 5.3-7.0 nm according to the calculation, showing that it is suitable for interband tunneling [78], [102], [114]-[116].

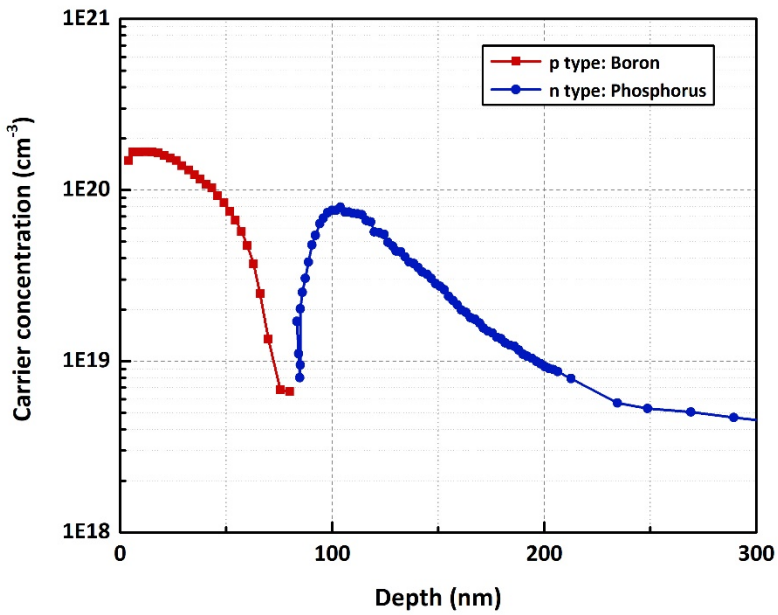


Figure 3.20 *ECV doping profile of the Si wafer adopted to fabricate tunnel diodes after B PRTD.*

3.3.1.1 Configuration and fabrication process

The fabrication process of tunnel diodes with vertical p^{++}/n^{++} tunnel junction is briefly illustrated in Figure 3.21 and it is explained in detail as follows:

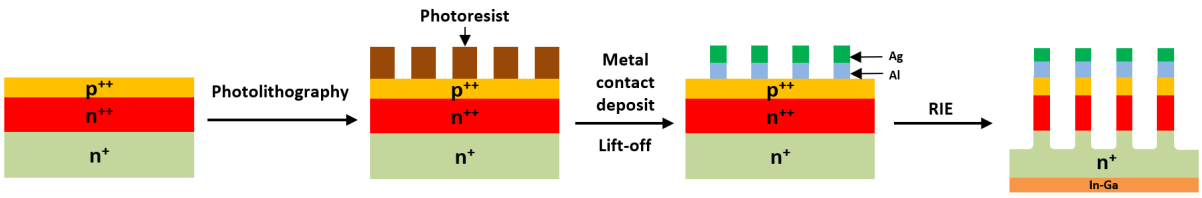


Figure 3.21 *The fabrication process of tunnel diodes with vertical p^{++}/n^{++} tunnel junction.*

- Photolithography was carried out for the preparation of metal front contact deposition. Negative photoresist nLOF 2070 was deposited on the sample by spin-on coating with a thickness of ~ 7 µm. After exposure and development, an array of cylindrical holes was obtained. The diameter of the holes is 200 µm and the array period of two perpendicular directions is 2 mm.

- Then the sample was cleaned by HF (5%) + UV/ozone (30 min) + BOE (Buffered oxide etch) just before the metal contact deposition by vacuum evaporator. 500 nm of Al was deposited as the front contact of the tunnel diode. 500 nm of Ag was deposited to protect Al contact during the etching process.
- 300 nm of silicon was etched by RIE to obtain isolated mesa tunnel diodes. The schematic of an isolated tunnel diode is shown in Figure 3.22.
- An annealing process was performed under N_2 flow at 400 °C for 40 s to optimize the electrical contact between Al and p^{++}-Si.
- In-Ga was smeared on the back surface of the sample to stick it on a piece of copper for the electrical characterization.

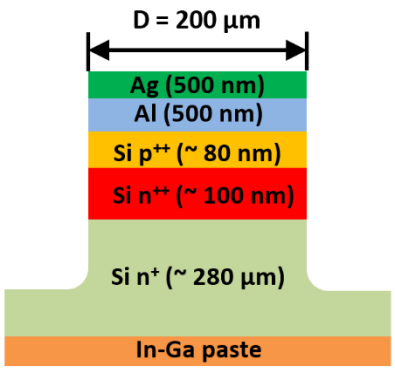


Figure 3.22 *The structure of an isolated p^{++}/n^{++} Si tunnel diode.*

3.3.1.2 *J-V* characterization

The current-voltage (*I-V*) characterization of tunnel diode was performed on Keithley 4200-SCS Parameter Analyzer at room temperature in dark conditions. The current density-voltage (*J-V*) characterization result of three diodes at different positions of the wafer is shown in Figure 3.23. The *J-V* curves are all almost linear around 0 V. Negative differential resistance behavior is observed when the bias is higher than a certain threshold (~ 0.7 V). It demonstrates the existence of tunnel diodes.

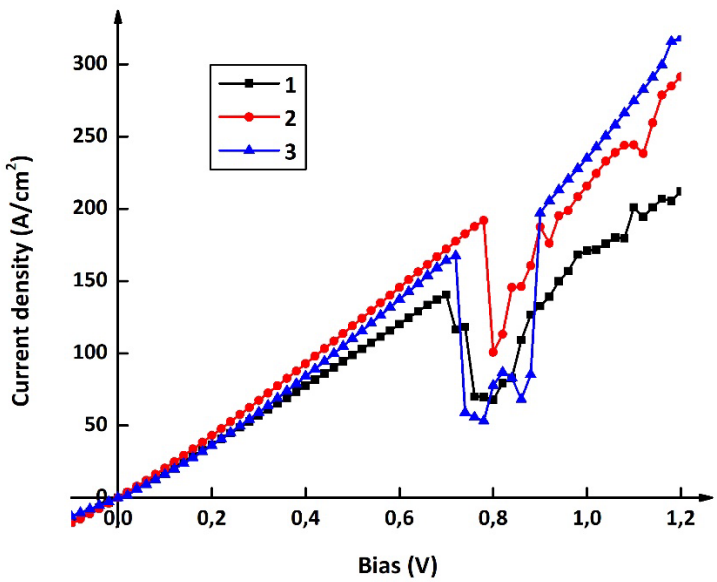


Figure 3.23 *J-V characterization of three p^{++}/n^{++} Si tunnel diodes at different positions of the sample annealed under N_2 flow at 400 °C for 40 s.*

Table 3.2 shows the performance of tunnel diodes in this sample. The peak to valley current ratio (PVCR) of these tunnel diodes is 1.19-3.15 while the peak current density (PCD) of them reaches 140-192 A/cm^2. The specific series resistance of the tunnel diode at low bias is about 4-5 mΩ·cm^2, which is experimentally defined as the slope of the *J-V* curve at $V = 0$. The expected specific series resistance is ~ 0.3 mΩ·cm^2, mainly arising from the n^+-Si substrate whose resistivity is ~ 0.01 Ω·cm. According to the literature, the specific contact resistance between Al and p^{++}-Si is 10^{-6}-10^{-5} Ω·cm^2 when the doping level of p-type Si is 10^{20}-10^{21} cm^{-3} [117]-[119]. Therefore, we calculated the specific series resistance of the tunnel diode with the assumption that the specific contact resistance between Al and p^{++}-Si is 10^{-5} Ω·cm^2. The higher specific series resistance we observed may be due to the high contact resistance between Al and p^{++}-Si, which decreased the performance of tunnel diodes. Incomplete surface cleaning after photolithography or the formation of native oxide on Si surface before Al deposition can lead to high Al/p^{++}-Si contact resistance. Several intentional methods could be adopted to optimize the tunnel diodes such as adjusting the contact-annealing temperature.

Table 3.2 *Performance of three p^{++}/n^{++} Si tunnel diodes at different positions of the sample annealed under N_2 flow at 400 °C for 40 s. The series resistance is the total resistance of tunnel diodes at V = 0.*

	PCD (A/cm^2)	Peak current position (V)	PVCR	Series resistance (Ω)	Specific series resistance ($m\Omega \cdot cm^2$)
1	140.4	0.70	2.07	15.6	5.0
2	191.9	0.78	1.91	12.7	4.0
3	167.4	0.72	3.15	13.2	4.1

The performance of the fabricated p^{++}/n^{++} tunnel diodes in this work is comparable with the p^{++}/n^{++} tunnel diodes prepared by other methods on (100)-oriented Si wafers (shown in Table 3.3). As the maximum current density in tandem solar cells is expected to be ~20 mA/cm^2, this tunnel junction can be applied not only in tandem solar cells operating under standard illumination conditions but also in those operating under concentrated light conditions.

Table 3.3 *Comparison of the performance of p^{++}/n^{++} Si tunnel diodes fabricated by different techniques.*

Reference	Approach	Dopants	Orientation	PCD (A/cm^2)	PVCR
DASHIELL [83]	MBE	B/P	<100>	47000	1.3
WANG [102]	P-RTD	B/P	<100>	5.6-7.2	-
BELLANGER [95]	Implantation	B/Ar	<100>	50	1.7
This work	P-RTD	B/P	<111>	140-192	1.9-3.2

3.3.2 Fabrication and characterization of Si tunnel diodes with lateral tunnel junction

To avoid the current loss in the n^+-substrate and better characterize the electrical property of the fabricated Si p^{++}/n^{++} tunnel junction, tunnel diodes with lateral tunnel junctions were designed and fabricated. Two Si substrates were adopted as the reference wafers for the measurement of doping profile by ECV. They have the same n^{++} emitter as that used for the fabrication of tunnel diodes. The two-step RTA process was carried out on the sample and reference wafers to adjust the n^{++} emitter profile. The first RTA was performed under N_2 flow at 1020 °C for 60 s and the second RTA was performed under N_2 flow at 1020 °C for 30 s. Three wafers were cleaned by HF (5%) + UV/ozone (60 min) + HF (5%) before and after each annealing.

3.3.2.1 Fabrication process

The fabrication process of Si tunnel diodes with lateral p^{++}/n^{++} tunnel junction is briefly illustrated in Figure 3.24 and it is explained in detail as follows:

- 100 nm of SiO_2 was deposited by PECVD on the n^{++} emitter of the sample prepared by two-step RTA and cleaning. This SiO_2 layer was used as a mask to prevent B atoms from diffusing into the n^{++} emitter during the B PRTD process. The same manipulation was carried out on one of the reference wafers.
- The first photolithography was carried out for the preparation of SiO_2 etching. Negative photoresist nLOF 2070 was deposited on the sample by spin-on coating with a thickness of ~ 7µm. The same photoresist was adopted for all the photolithography in this fabrication process. To obtain lateral tunnel diodes of different diameters, a mask with three types of circular patterns was adopted. The diameters of the circles were 50, 100, 200 µm respectively. After exposure and development, three arrays of cylindrical holes with a period of 2 mm were obtained on the sample. The actual diameters of the holes measured by optical microscope were ~ 35, ~ 95, ~ 198 µm respectively. The use of a thinner resin is required to reduce the difference between the targeted and realized hole diameter for the smaller one.
- Then the sample was dipped into BOE solution for 65 s to remove the SiO_2 that was not covered by the photoresist.
- After BOE etching and cleaning, the sample was dipped into acetone to remove the photoresist.
- B PRTD was performed on the sample and two reference wafers under air flow at 1000 °C for 10 s to achieve Si p^{++}/n^{++} tunnel junctions. The doping profiles of the reference wafers with and without a SiO_2 mask after B BPRTD are shown in Figure 3.25. The doping profile of the reference wafer with SiO_2 mask after B PRTD shows that 100 nm-SiO_2 has effectively prevented the diffusion of B atoms. The doping profile of the tunnel junction was assumed to be similar to the one without the SiO_2 mask. For the reference wafer, the thickness of the p^{++} layer is ~ 65 nm. The concentration of active B atoms reaches ~ 2.8×10^{20} cm^{-3} near the surface, while the concentration of active P atoms is ~ 1.4×10^{20} cm^{-3} near the depletion region.
- The second photolithography with an alignment process was carried out for the preparation of metal contact deposition. A mask of circular patterns with the same period as before was adopted. The diameter of the circles was 300 µm. After the second photolithography, holes with a diameter of 300 µm appeared above each tunnel junction. The other area of the sample was covered by the photoresist with a thickness of ~ 7µm.

- 500 nm of Al was deposited by vacuum evaporator to form the contact with p^{++}-Si. The sample was cleaned by BOE for 15 s just before the Al deposition.
- The third photolithography with an alignment process was carried out for the preparation of the contact with n^{++}-Si. A mask of ring patterns with the same period as before was adopted. The inner diameter of the ring was 500 µm while the outer diameter was 800 µm.
- To expose the n^{++} emitter, the sample was dipped into BOE solution for 65 s to remove 100 nm of SiO_2.
- 500 nm of Al was deposited by vacuum evaporator to form the contact with n^{++}-Si. The sample was cleaned by BOE for 15 s just before the Al deposition.
- The lift-off process was carried out in acetone to remove the photoresist.
- An annealing process was performed under N_2 flow at 400 °C for 40 s to optimize the electrical contact between Al and Si.

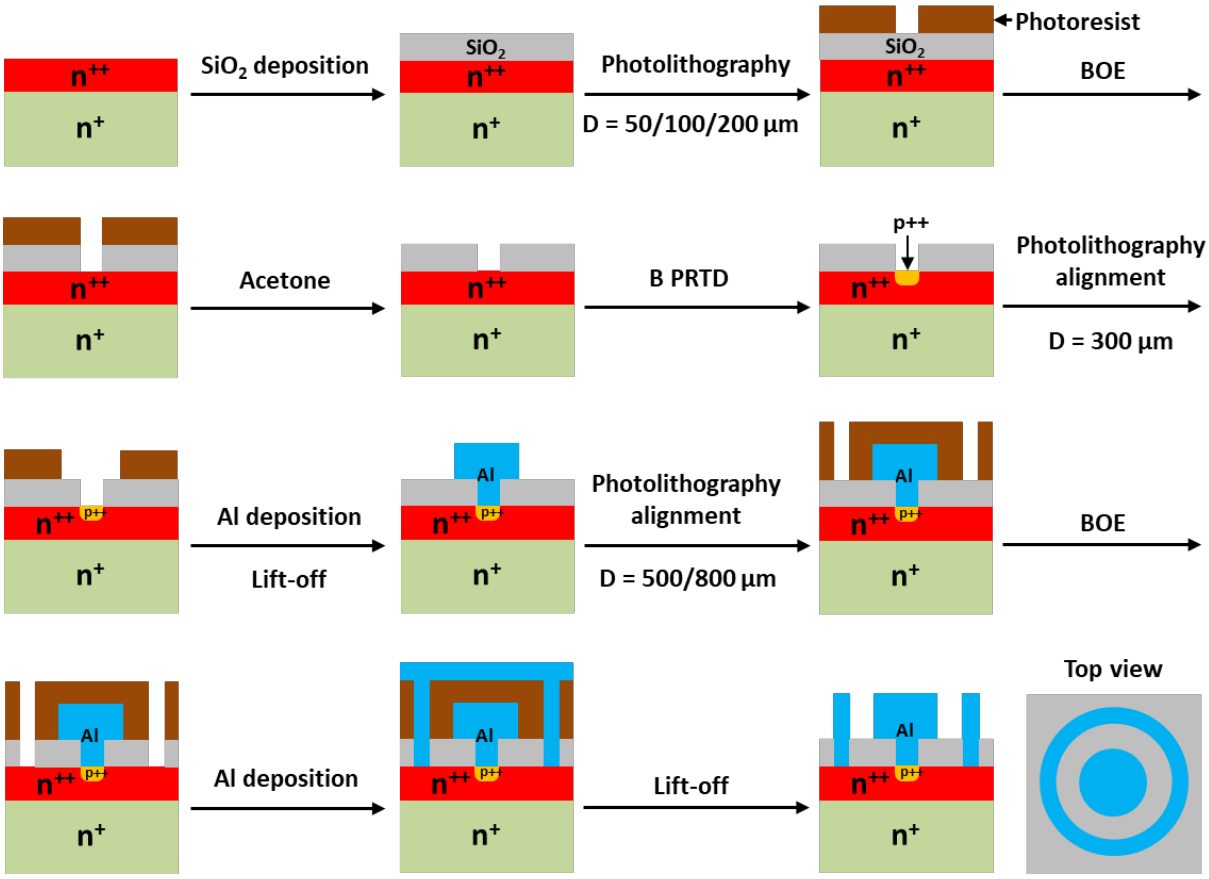


Figure 3.24 *The fabrication process of the Si tunnel diode with lateral p^{++}/n^{++} tunnel junction.*

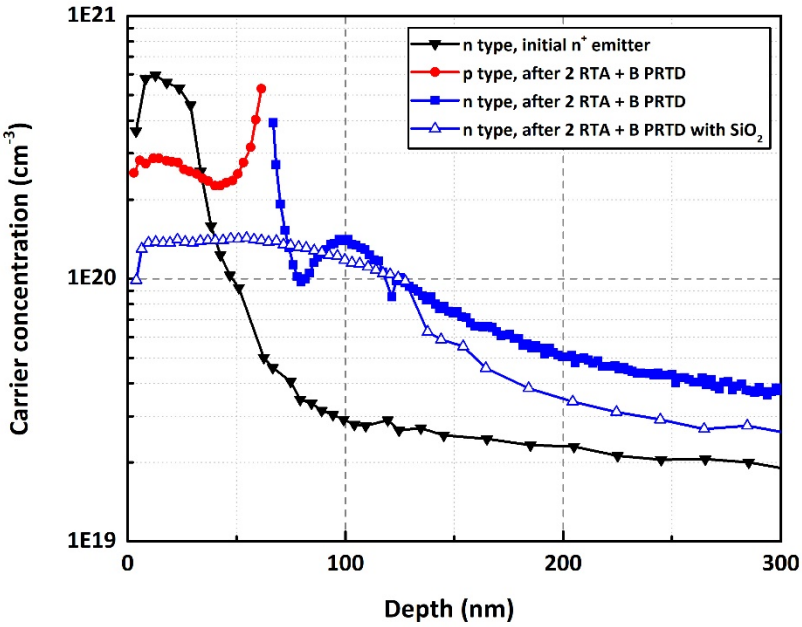
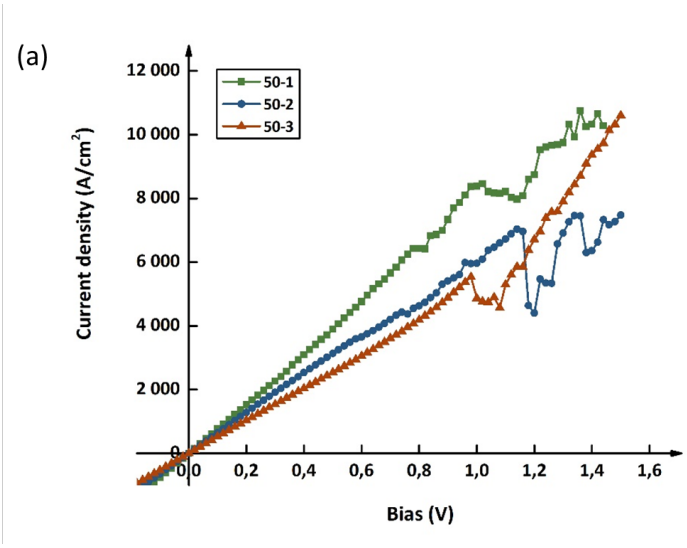


Figure 3.25 *Doping profile of the reference wafers with and without SiO_2 mask for lateral tunnel junction.*

3.3.2.2 *J-V* characterization

J-V characterization result of diodes with different diameters at different positions of the wafer is shown in Figure 3.26. The performance details of each lateral tunnel diode are listed in Table 3.4.



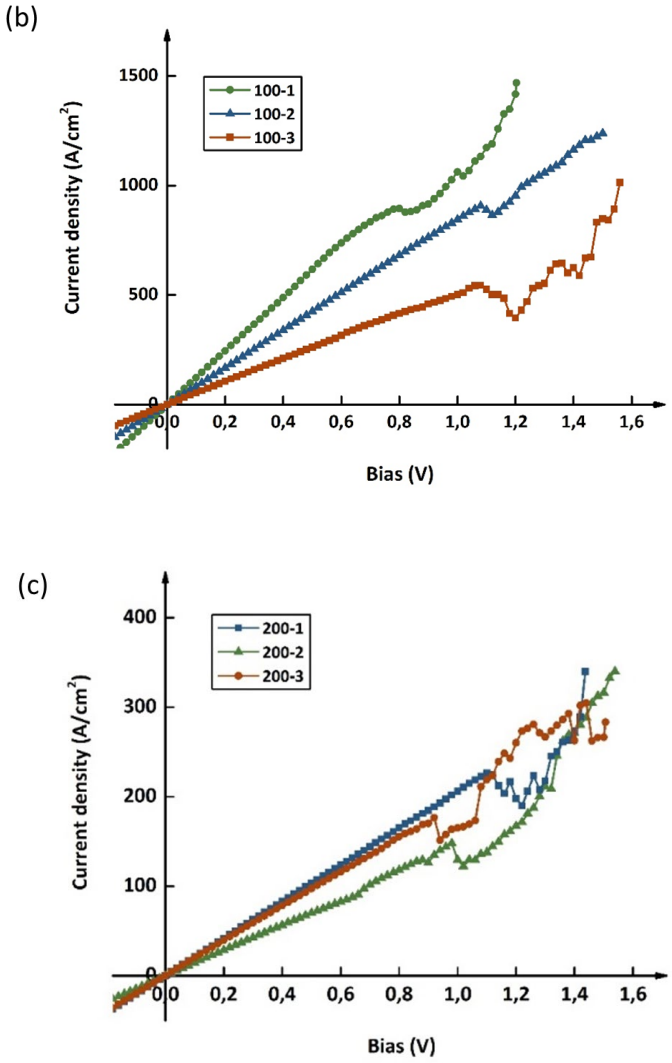


Figure 3.26 *J-V characterization of lateral p^{++}/n^{++} Si tunnel diodes at different positions of the sample annealed under N_2 flow at 400 °C for 40 s. The diameters of the tunnel junctions are (a) 50 µm, (b) 100 µm, (c) 200 µm.*

All the *J-V* curves shown in Figure 3.26 are almost linear around 0 V. Negative differential resistance behaviors are observed when the bias is higher than a certain threshold, indicating the existence of tunnel diodes. The *J-V* curves of the tunnel diodes with diameters of 50 µm and 100 µm show a significant variation. This might be caused by the imperfect development during the second photolithography progress. There was some photoresist residue at the edge of the holes. The use of a thinner resin may resolve this problem.

Table 3.4 *Performance of lateral p^{++}/n^{++} Si tunnel diodes with different diameters at different positions of the sample annealed under N_2 flow at 400 °C for 40 s. The series resistance is the total resistance of tunnel diodes at V = 0.*

	Diameter (µm)	Peak current (mA)	PCD (A/cm^2)	Peak current position (V)	PVCR	Series Resistance (Ω)	Specific series resistance ($m\Omega \cdot cm^2$)
50-1	35	81.5	8471	1.02	1.06	13.2	0.13
50-2	35	67.7	7037	1.14	1.60	16.4	0.16
50-3	35	53.3	5540	0.98	1.21	20.2	0.19
100-1	95	63.5	895	0.80	1.02	11.5	0.81
100-2	95	64.4	908	1.08	1.05	16.7	1.18
100-3	95	38.6	544	1.08	1.37	26.7	1.90
200-1	198	69.7	227	1.10	1.19	15.7	4.84
200-2	198	45.6	148	0.98	1.21	23	7.08
200-3	198	54.4	177	0.92	1.17	16.7	5.13

Compared with vertical tunnel diodes in section 3.3.1, lower PVCRs are observed in these lateral tunnel diodes, suggesting the presence of higher excess current [121]. The contamination of the RTA furnace was not noticed until the fabrication of lateral tunnel diodes was finished. As a result, unwanted impurities were introduced into the p^{++}/n^{++} tunnel junction, increasing the excess current. There is no obvious difference between the series resistance of vertical and lateral tunnel diodes at the low bias (~ 0 V). It suggests that the excessively high specific series resistance observed in the vertical tunnel diode does not arise from the n^+-Si substrate. The contact between Al and highly doped Si needs to be carefully studied.

3.3.3 Optimization of Al/Si contact

To optimize the electrical contact between Al and Si, the impact of the contact fabrication process and annealing process on the Al/Si contact resistance was investigated. The transfer length method (TLM) was carried out to measure the contact resistance between them.

The measurement principle of TLM is shown in Figure 3.27. The black rectangles represent identical metal contacts lying on a semiconductor (Figure 3.27(a)). The total resistance R_t between two points on contacts can be expressed as:

$$R_t = 2R_m + R_{semi} + 2R_c \approx R_{semi} + 2R_c \tag{3.10}$$

Here R_m is the resistance of metal contact, R_{semi} is the semiconductor resistance, R_c is the contact resistance at the metal/semiconductor interface. Generally, R_m is very small compared with R_{semi} and R_c, so it can be ignored.

The R_{semi} between two metal contacts is given by:

$$R_{semi} = R_{sh}\frac{d}{Z} \tag{3.11}$$

Here R_{sh} is the sheet resistance of the semiconductor, d is the contact spacing, Z is the width of the metal contact. Thus, the expression of total resistance is changed to be:

$$R_t = \frac{R_{sh}}{Z}d + 2R_c \tag{3.12}$$

It indicates that there is a linear relationship between the total resistance and the contact spacing. By measuring the voltage and current between every two adjacent contacts, a plot of total resistance R_t versus contact spacing d can be obtained, as shown in Figure 3.27(b). The intercept of the fitted line at $d = 0$ means $R_T = 2R_c$, giving the contact resistance R_c. As the slope of the fitted line is R_{sh}/Z, the sheet resistance of the semiconductor can also be derived.

Considering the correlation between the contact resistance and contact area, specific contact resistance ρ_c is a more practical parameter due to its independence of the contact area. ρ_c is given by:

$$\rho_c = R_c A_c \tag{3.13}$$

Here A_c is the contact area. Because the current flow through the contact is not uniform, as shown in Figure 3.27(c), the physical contact area is not equal to the effective area. Thus, transfer length L_T is introduced and defined as [120]:

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{3.14}$$

L_T represents the effective contact length. It leads to

$$\rho_c = R_c A_c = R_c L_T Z \tag{3.15}$$

Combining Eq.(3.12), Eq.(3.14), and Eq.(3.15),

$$R_t = \frac{R_{sh}}{Z}(d + 2L_T) \tag{3.16}$$

is derived. It suggests that $-d = 2L_T$ when $R_t = 0$, corresponding to the intercept of the fitted line at $R_t = 0$, as shown in Figure 3.30(b).

After obtaining the R_c and L_T from the R_t versus d plot, the specific contact resistance

ρ_c can be calculated. Therefore, Al TLM patterns were fabricated on n++-Si and p++-Si to study their specific contact resistances in this work.

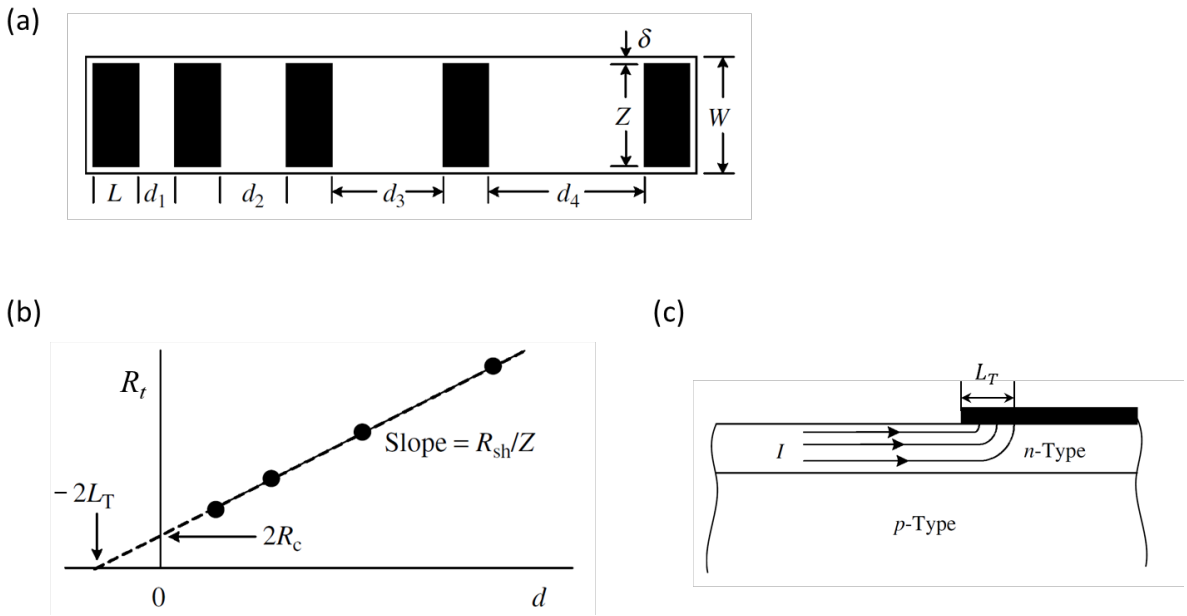
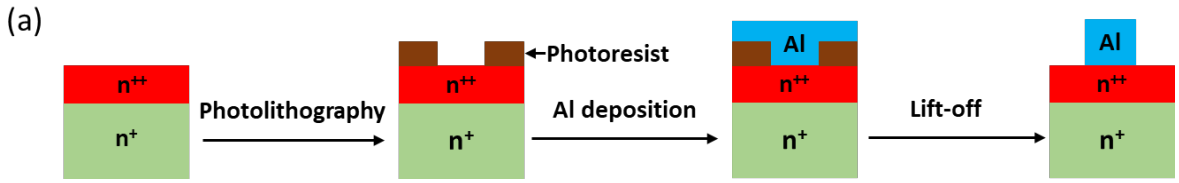


Figure 3.27 *(a) The top view of a TLM structure; (b) The plot of the total resistance versus contact spacing; (c) The current transfer from semiconductor to metal, represented by arrows [120].*

First, two different processes were carried out to fabricate the Al TLM pattern on (111)-oriented n+-Si substrates with an n++-Si layer. These two processes were designed to study the influence of the photolithography process on Al/Si contact. The fabrication processes including Al lift-off process or Al etching process to make one Al contact are shown in Figure 3.28 (a) and Figure 3.28 (b) respectively. The main difference between them is the order of the photolithography and the Al deposition. In Figure 3.28 (a), Al is deposited after the photolithography process, might leaving some photoresist residue at the Al /Si interface. In Figure 3.28 (b), Al is deposited before the photolithography process, making sure that there is no photoresist residue between Al and Si. The doping concentration of the n+-Si substrate and n++-Si layer is about 2 × 10^{19} cm^{-3} and 1.5 × 10^{20} cm^{-3}, respectively.



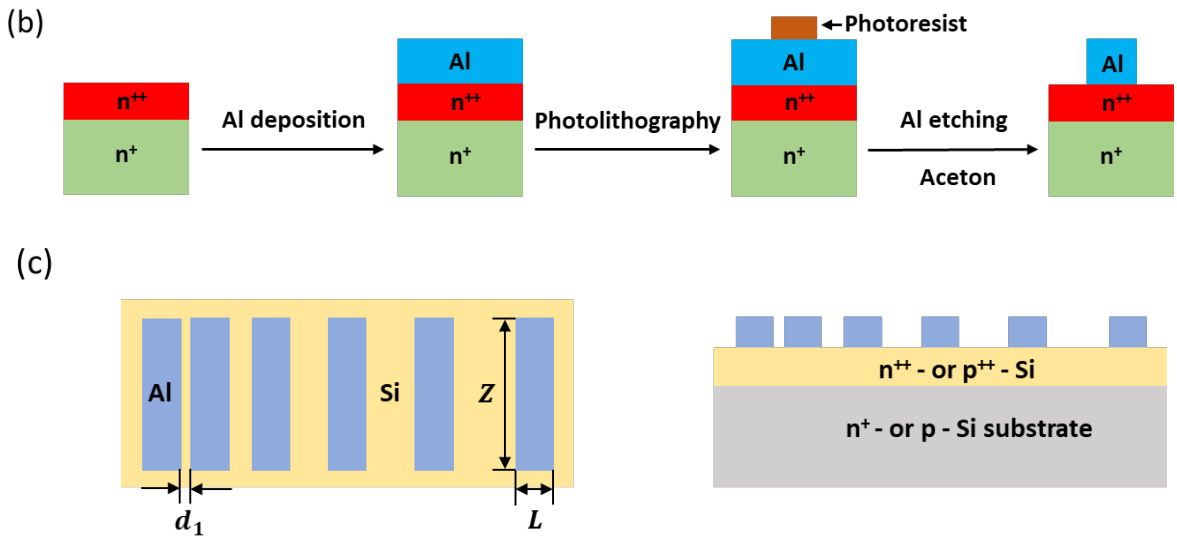


Figure 3.28 *Fabrication processes of one Al contact of TLM configuration in (a) series A and (b) series B; (c) Top view (left) and side view (right) of the fabricated TLM configuration, Z = 5 mm, L = 1mm, d_1 = 100 µm. The contact spacing increases from 100 µm to 500 µm, with an increase of 100 µm between two adjacent spacings.*

The same processes were carried out on (111)-oriented p-type Si substrates with a p^{++}-Si layer. The doping concentration of the p-Si substrate and p^{++}-Si layer is about 1×10^{16} cm^{-3} and 1.5×10^{20} cm^{-3}, respectively. The top and side views of the sample with the entire TLM structure are shown in Figure 3.28 (c). For simplicity, the TLM samples fabricated following Figure 3.28 (a) were named as series A-n and A-p, while the others fabricated following Figure 3.28 (b) were named as series B-n and B-p. Each series has four samples.

Four different treatments were performed on these TLM samples, as shown in Table 3.5. The annealing processes were named No.1, No.2, and No.3, respectively. The Nabertherm furnace used in the No.2 annealing process is a conventional furnace. The samples treated by No.4 are used as the reference, without any annealing. The annealing temperatures were all set as 400 °C. The forming gas is a mixture of N_2 (95%) and H_2 (5%).

Table 3.5 *TLM samples treated by different annealing processes*

Sample name	Treatment name	Equipment	Atmosphere	Time
A-n-1 B-n-1 A-p-1 B-p-1	No.1	ADDAX RTA	N_2	40 s
A-n-2 B-n-2 A-p-2 B-p-2	No.2	Nabertherm furnace	N_2	15 min
A-n-3 B-n-3 A-p-3 B-p-3	No.3	Nabertherm furnace	Forming gas	15 min
A-n-4 B-n-4 A-p-4 B-p-4	No.4	-	-	-

After the annealing process, current and voltage between every two adjacent contacts were measured to obtain the total resistance. Then the figures of total resistance versus contact spacing were plotted. The results of Al/n^{++}-Si and Al/p^{++}-Si are shown as follows.

a) TLM result of Al/n^{++}-Si samples

Figure 3.29 shows the plots of the total resistance versus contact spacing for eight Al/n^{++}-Si TLM samples. Linear relationships are observed on all samples. The samples with an annealing process all have a lower total resistance compared with the reference samples. The total resistance of the reference sample A-n-4 is much higher than that of B-n-4, showing the impact of the photolithography process.

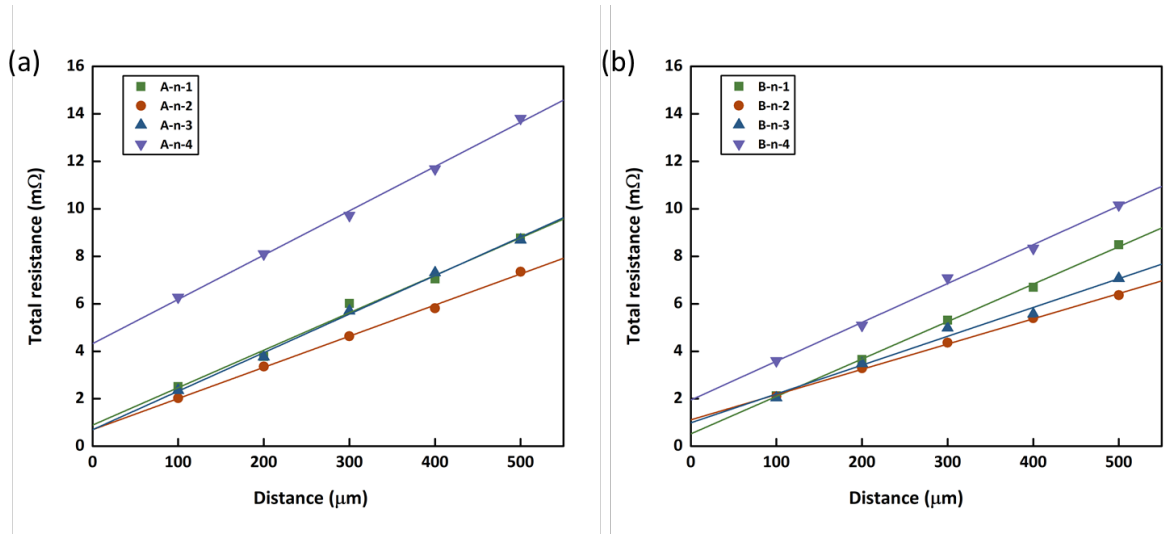


Figure 3.29 *Plots of the total resistance versus contact spacing for (a) series A-n and (b) series B-n of Al/n^{++}-Si TLM samples.*

The Al/n^{++}-Si specific contact resistance calculation results are shown in Table 3.6. The lowest specific contact resistance is 2.16×10^{-7} Ω·cm^2, obtained on sample B-n-1 which is annealed by RTA. The Al/n^{++}-Si specific contact resistance results are in agreement with the results obtained at similar conditions reported in the literature, which is 10^{-7}-10^{-5} Ω·cm^2 when the doping level of n-type Si is 10^{20}-10^{21} cm^{-3} [117]. It is noticed that the same annealing process has different impacts on two series of samples. The magnitude decrease of the specific contact resistance is observed in series A-n samples. However, the impact of annealing on series B-n samples is not as significant as that on series A-n samples, except for the one annealed by RTA. After annealing, the impact of the photolithography process is no longer apparent.

Table 3.6 *Specific contact resistance calculation results of Al/n^{++}-Si samples*

	No.1	**No.2**	**No.3**	**No.4**
ρ_c of series A-n (Ω·cm^2)	6.28×10^{-7}	4.65×10^{-7}	3.74×10^{-7}	1.25×10^{-5}
ρ_c of series B-n (Ω·cm^2)	**2.16×10^{-7}**	1.45×10^{-6}	9.98×10^{-7}	2.90×10^{-6}

b) TLM result of Al/p^{++}-Si samples

The plots of the total resistance versus contact spacing for eight Al/p^{++}-Si TLM samples are shown in Figure 3.30. Different from the Al/n^{++}-Si TLM samples, no obvious optimization is observed in Al/p^{++}-Si TLM samples after the annealing process. Besides, there is no obvious

difference between the total resistances of reference sample A-p-4 and sample B-p-4. It indicates that the impact of the photolithography process on Al/p^{++}-Si contact can be neglected.

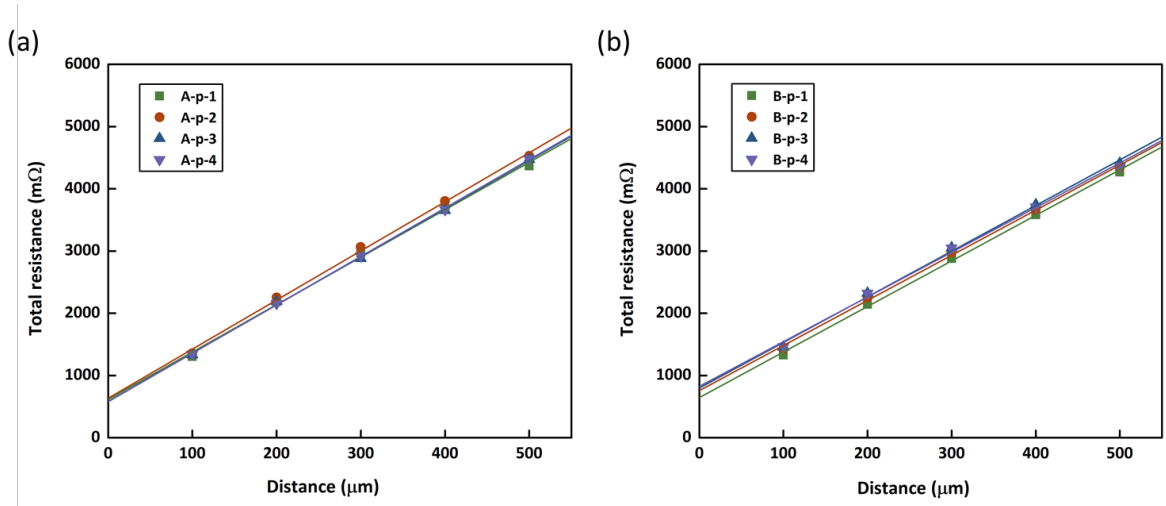


Figure 3.30 *Plots of the total resistance versus contact spacing for (a) series A-p and (b) series B-p of Al/p^{++}-Si TLM samples.*

The Al/p^{++}-Si specific contact resistance calculation results are shown in Table 3.7. It shows that the specific contact resistance between Al and p^{++}-Si is about three times higher than that between Al and n^{++}-Si. The lowest Al/p^{++}-Si specific contact resistance is 5.39×10^{-4} Ω·cm^2, obtained on the sample A-p-4 without annealing. This value is higher than the results reported in the literature, which is 10^{-6}-10^{-5} Ω·cm^2 when the doping level of p-type Si is 10^{20}-10^{21} cm^{-3} [117]-[119].

Table 3.7 *Specific contact resistance calculation results of Al/p^{++}-Si samples*

	No.1	**No.2**	**No.3**	**No.4**
ρ_c of series A-p (Ω·cm^2)	6.20×10^{-4}	6.37×10^{-4}	5.50×10^{-4}	**5.39×10^{-4}**
ρ_c of series B-p (Ω·cm^2)	7.10×10^{-4}	9.88×10^{-4}	1.09×10^{-3}	1.19×10^{-3}

The above results show that the contact between Al and n^{++}-Si can be optimized by annealing at 400 °C for 40 s to get a specific contact resistance of 2.16×10^{-7} Ω·cm^2. The three annealing processes that we adopted are not suitable to reduce the contact resistance between Al and p^{++}-Si. The impact of the photolithography process on Al/n^{++}-Si contact or Al/p^{++}-Si contact is not significant when the annealing process is performed. It suggests that

the high specific series resistance of our tunnel diodes is not caused by the incomplete surface cleaning after photolithography. Therefore, the formation of native oxide on the Si surface before Al deposition and the inappropriate annealing process could be the main reason for the inferior Al/p^{++}-Si contact. The optimization of Al/p^{++}-Si contact remains to be investigated in the future. Al deposition equipment with an in-situ cleaning system might be a choice. We did not study it further in this work because of the time.

3.4 Conclusion

In summary, the fabrication and characterization of p^{++}/n^{++} Si tunnel junction on (111)-oriented c-Si substrate is demonstrated in this chapter. The n^{++} emitter is formed by the photovoltaic industrial technique (LYDOP system) while the p^{++} layer is obtained by boron PRTD. The initial n^{++} emitter profile is highly doped near the surface and then decreases abruptly away from the surface, making it difficult to form a tunnel junction. By introducing a two-step RTA, the n^{++} emitter profile is adjusted to be more suitable for B atoms to compensate. At the same time, sufficient P atoms are maintained to form the n^{++}-layer in the tunnel junction. After boron PRTD, Si p^{++}/n^{++} tunnel junction with a depletion region of 5.3-7.0 nm-width is achieved. Based on this, Si p^{++}/n^{++} tunnel diode is fabricated to characterize the electrical properties of the tunnel junction. A peak current density of 192 A/cm^2 is observed in the tunnel diode. It indicates that the fabricated tunnel junction can be applied not only in standard tandem solar cells but also in concentrated solar cells.

Chapter 4 Implementation of tunnel junction in solar cells

4.1 Introduction

This chapter presents the implementations of p^{++}/n^{++} Si tunnel junction in solar cells. In the first section, the fabrication and characterization of single-junction Si solar cells with p^{++}/n^{++} Si tunnel junction on the surface are presented. Standard Si solar cell is also studied to investigate the impact of tunnel junction on the performance of the solar cell. The second section reports the implementation of p^{++}/n^{++} Si tunnel junction in III-V NWs/Si tandem solar cells. The fabrication process of NWs/Si tandem solar cells is developed before the first trial of fabrication and characterization of the targeted III-V NWs/Si tandem solar cell.

4.2 Fabrication and characterization of Si solar cells

4.2.1 Fabrication process of Si solar cells

2-inch (111)-oriented p-type CZ Si substrates with a doping concentration of ~ 1×10^{16} at/cm^3 were used to fabricate the solar cells. We used a standard Al-BSF technology. The fabrication process is briefly illustrated in Figure 4.1 and it is explained as follows:

- Standard $POCl_3$ thermal diffusion by LYDOP at 870 °C for 20 min was performed on the Si substrate to form the n^{++} emitter.
- HF (5%) + piranha (15 min) + HF (5%) was used to remove the phosphosilicate glass (PSG) layer forming during the diffusion process.
- Si on the backside was etched by RIE (SF_6 (5 sccm)/A_r (20 sccm), 15 mTorr, 60 W) to remove the n^{++} layer.
- 3 µm of Al was deposited on the backside by evaporation.
- The sample was then annealed at 750 °C for 10 s under N_2 flow to form the p^+ back surface field (BSF) layer.
- 75 nm of SiN_x passivation layer was deposited on the front side by PECVD.
- Photolithography was carried out to prepare the fabrication of front contact.
- SiN_x uncovered by photoresist was etched by BOE for 22 min to expose the front contact area.
- Ti/Pd/Ag (50 nm/50 nm/400 nm) was deposited by evaporation as the front contact.
- Lift-off in acetone was carried out to remove the photoresist.

- Annealing at 320 °C for 1 min under N_2 flow was performed to improve the electrical contact between Ti/Pd/Ag and n^{++}-Si.

The fabricated standard Si solar cell was named as sample A. At the same time, Si solar cell with p^{++}/n^{++} planar tunnel junction on the surface was also fabricated and it was named as sample B. The fabrication process of sample B is briefly illustrated in Figure 4.2. Compared with the fabrication process of sample A shown in Figure 4.1, there are two differences in Figure 4.2. First, two-step RTA and B PRTD (Proximity Rapid Thermal Diffusion) were carried out on the front side after the removal of the n^{++}-layer on the backside. As a result, Si p^{++}/n^{++} planar tunnel junction was implemented on the surface. Second, 500 nm of Al was used as the front contact instead of Ti/Pd/Ag. Annealing at 370 °C for 1 min under N_2 flow was performed to improve the electrical contact between Al and p^{++}-Si.

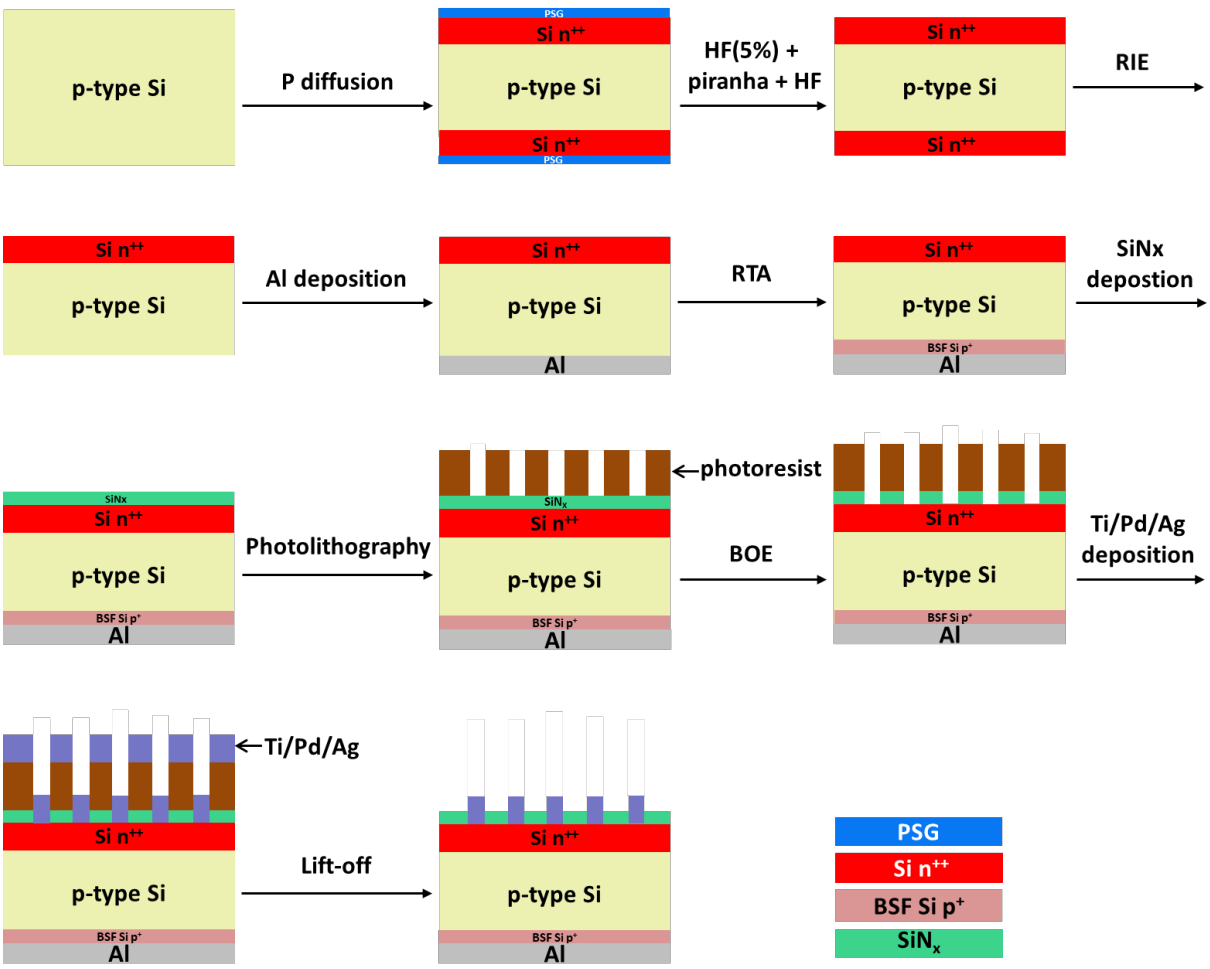


Figure 4.1 *Fabrication process of sample A (standard Si solar cell).*

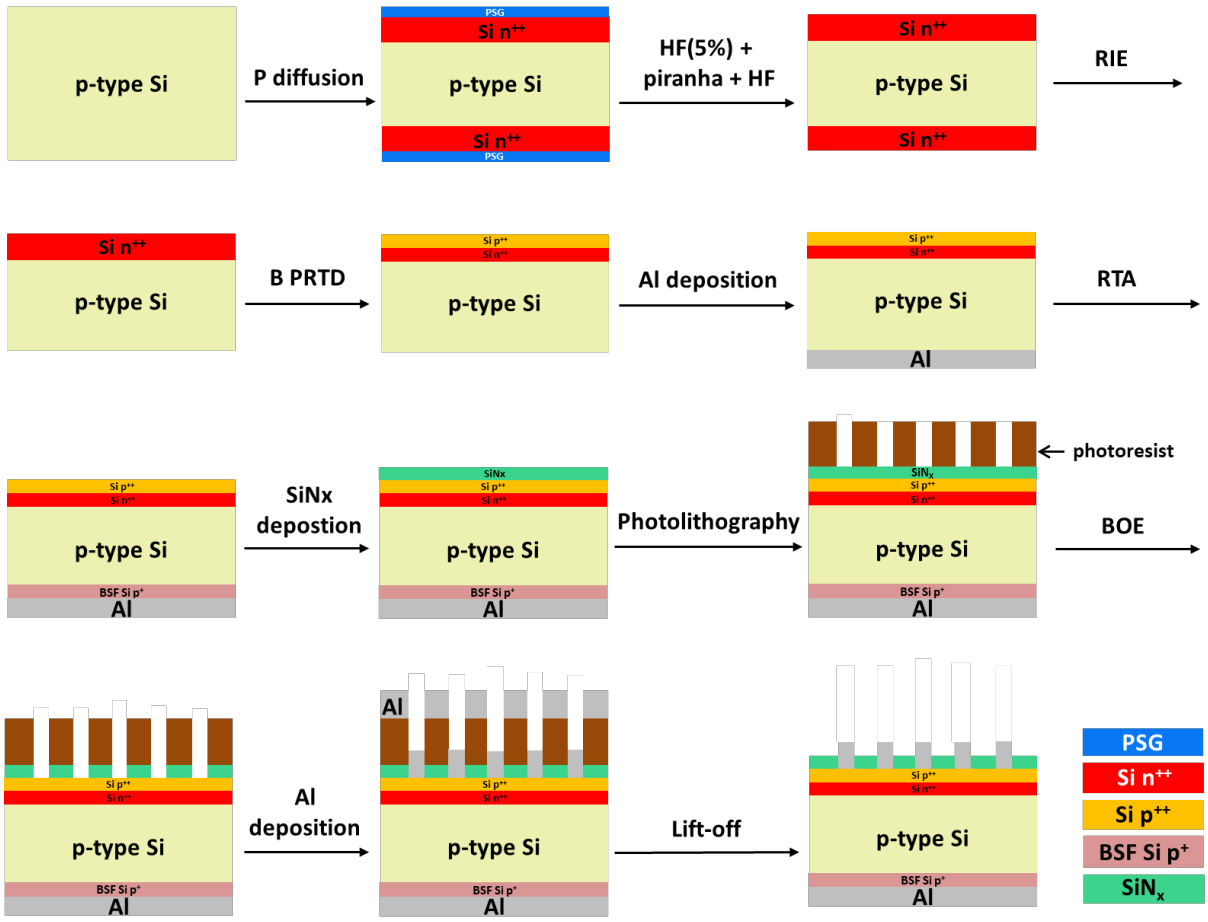


Figure 4.2 *Fabrication process of sample B (Si solar cell with planar tunnel junction on the surface).*

4.2.2 Characterization of Si solar cells

4.2.2.1 *J-V* and efficiency characteristics

The current density-voltage (*J-V*) curve and efficiency of samples A and B were characterized by Sinton instruments FCT-350 under standard test conditions. The samples were measured under an irradiance of 1000 W/m^2 with an AM1.5 spectrum and they had a temperature of 25 °C during the measurement process.

The measurement results are shown in Figure 4.3 and Table 4.1. Compared to sample A, sample B shows a degraded performance. The V_{oc} of sample A is 593.1 mV while that of sample B is 477.0 mV. The maximum efficiency of the solar cell decreases from 13.09% (sample A) to 5.67% (sample B) due to the presence of a planar tunnel junction on the surface. Suns-Voc curves without the effects of series resistance are also displayed in Figure 4.3. The drop of the voltage between Suns-Voc and *J-V* curves at the maximum power point reflects the series resistance of solar cells [122]. The voltage deviation of Suns-Voc and *J-V* curves in sample B is

bigger than that in sample A, indicating that the series resistance of sample B is higher than that of sample A. The higher series resistance in sample B may be caused by the inferior contact between the Al and p^{++}-Si on the front side, as it was discussed in section 3.3.3.

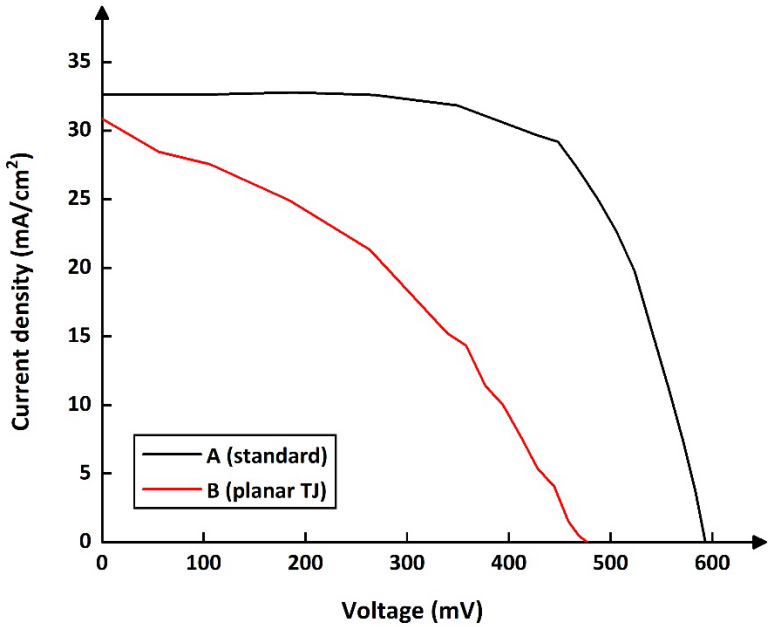


Figure 4.3 *Light J-V curve of samples (a) A and (b) B.*

Table 4.1 *Electrical performance and efficiency of samples A and B.*

Sample	V_{oc} (mV)	V_{mp} (mV)	J_{sc} (mA/cm²)	J_{mp} (mA/cm²)	*FF* (%)	Max efficiency (%)
A	593.1	448.2	32.6	29.2	67.7	13.09
B	477.0	278.4	30.9	20.4	38.5	5.67

4.2.2.2 External quantum efficiency

The external quantum efficiency (EQE) of samples A and B were measured to give us some information regarding the photogenerated current. The result in Figure 4.4 shows that the EQE of sample B is lower than sample A, especially at the short wavelength range (300-400 nm). It indicates that the carrier collection capabilities of the solar cell have been degraded with the presence of a planar tunnel junction on the surface. Photogenerated carriers recombine without being collected in the heavily doped tunnel junction, thus increasing the surface recombination. When the Si solar cell is used as the bottom solar cell in tandem solar cells, it mainly absorbs the light in the infrared wavelength range. Therefore, when the planar tunnel junction is applied in tandem solar cells, the influence of the surface recombination caused by

the tunnel junction will be less severe as the absorption of IR occurs in the volume of the absorber. In addition, there is a noticeable reduction of EQE in sample B in the infrared wavelength range (850-1100 nm). This reduction may be caused by the imperfect cleanliness of the RTA furnace that was used to fabricate tunnel junctions. Undesired impurities were introduced into the Si wafer during the annealing process, thus reducing the carrier diffusion length.

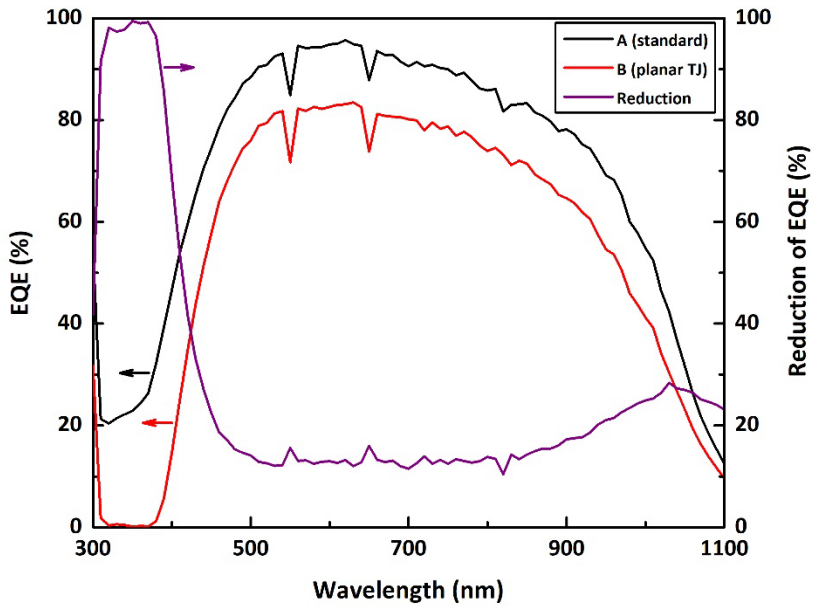


Figure 4.4 *External quantum efficiency (EQE) of samples A and B (left axis) and the reduction of EQE in sample B compared with that in sample A (right axis).*

4.2.3 Optimization of Si solar cell with tunnel junction on the surface

Considering that the NWs partially cover the Si bottom solar cell in our targeted III-V NWs/Si tandem solar cell, as shown in Figure 1.15, localized tunnel junctions are proposed to be used as the electrical connection. The performance of the Si solar cell is supposed to be improved by using localized tunnel junctions instead of the planar tunnel junction. Therefore, Si solar cell with localized tunnel junction beneath the front contact was fabricated following the fabrication process in Figure 4.5. This solar cell was named as sample C. Compared to the fabrication process of sample B, the SiN_x passivation layer of sample C was partially etched by BOE before the fabrication of tunnel junction. During the B PRTD process, the residual SiN_x functioned as the mask to prevent the diffusion of B atoms, resulting in localized tunnel junctions. Front Al contact was deposited directly above the p^{++}/n^{++} localized tunnel junctions.

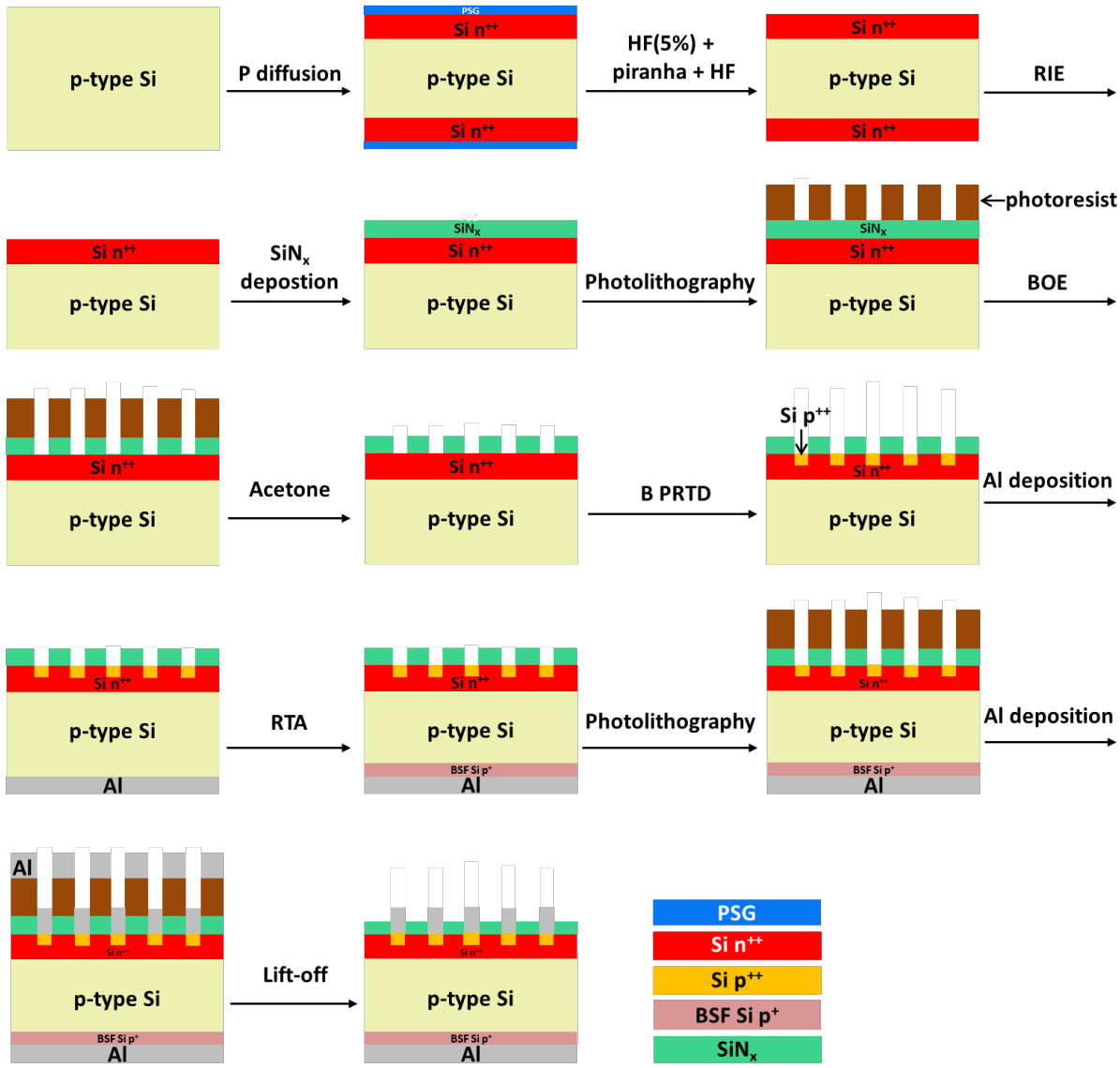


Figure 4.5 *Fabrication process of sample C (Si solar cell with localized tunnel junction on the surface).*

The *J-V* curves under the illumination of samples A, B, and C are shown in Figure 4.6 (a). The maximum efficiency of sample C was measured to be 10.43% with a V_{oc} of 564.6 mV, higher than that of sample B. The surface recombination has decreased by reducing the tunnel junction area. The EQE reduction in sample C compared with that in sample A at the short wavelength range (300-400 nm) was also observed to be reduced due to less surface recombination. Therefore, it is necessary to use localized tunnel junction instead of planar tunnel junction in our targeted III-V NWs/Si tandem solar cell to achieve high performance. Besides, it should be noticed that the reduction of EQE in the infrared wavelength range (850-1100 nm) in sample C is similar to that in sample B. It shows that this reduction is induced by the tunnel junction fabrication process. It is proposed to improve the EQE of solar cells with

tunnel junctions by improving the cleanliness of the RTA furnace.

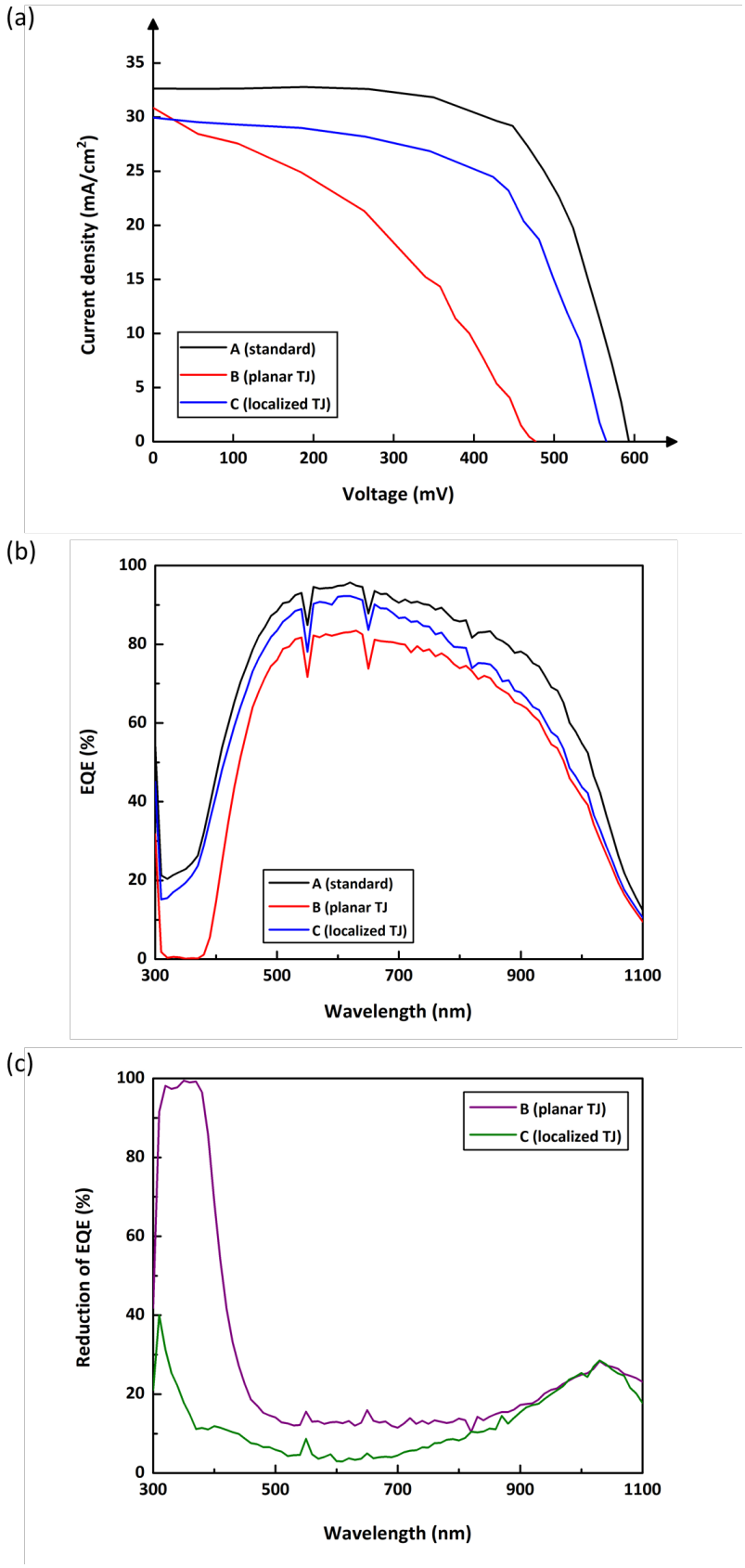


Figure 4.6 *(a) Light J-V and efficiency of sample C; (b) External quantum efficiency (EQE) of sample C; (c) Reduction of EQE in sample B and sample C compared with that in sample A*

Table 4.2 *Electrical performance and efficiency of samples A and B.*

Sample	V_{oc} (mV)	V_{mp} (mV)	J_{sc} (mA/cm^2)	J_{mp} (mA/cm^2)	*FF* (%)	Max efficiency (%)
C	564.6	421.6	30.0	24.7	61.66	10.43

4.3 Fabrication and characterization of NWs/Si tandem solar cell

4.3.1 Introduction of NWs/Si TSC fabrication process

The fabrication processes of solar cells based on NW arrays have been reported in the literature [62], [63], [123]-[128]. Generally, there are three primary steps to fabricate NWs solar cells: synthesizing NWs, planarizing NW arrays, and depositing contact.

When synthesizing NWs, two fundamental approaches can be used, the top-down approach and the bottom-up approach. The top-down approach fabricates NWs by selectively etching away materials from bulk starting form. Uniform NW arrays can be obtained by this approach. What's more, the NWs are typically etched to be tapered in the morphology, which is beneficial for light absorption [129]. InP NWs solar cell with an efficiency of 17.8% has been fabricated by dry-etching an InP planar solar cell [130]. It is the most efficient III-V NWs solar cell reported so far.

Different from the top-down approach, the bottom-up approach grows NWs directly on substrates through disordered starting materials by providing appropriate conditions, such as reactants, temperature, and pressure. Compared with the top-down approach, the bottom-up approach offers greater control and possibilities in device design [131]. Therefore, III-V NWs used for solar cells are mostly grown by this method. The dominant modes of the bottom-up approach to growing III-V NWs include selective area (SA) growth and vapor-liquid-solid (VLS) growth, usually carried out by MBE or MOCVD.

The SA growth uses patterned holes in an inert mask on the growth substrate to define the location of NW growth. When growth conditions are carefully tailored, low-index faceted nanowires are formed at these locations, and the nucleation energy anisotropy ensures continued one-dimensional growth [132]. The first III-V NWs/Si tandem cells, with an open-circuit voltage of 0.956 V and an efficiency of 11.4%, were realized through SA growth by MOCVD [62]. Nevertheless, The SA growth typically suffers from the defects accommodated in the interface and it is typically carried out at higher temperatures (up to 750 °C) [133]. The

crystal quality and the thermal budget of the SA growth are issues of concern.

The VLS growth is a mode of NW synthesis where beams or flows of molecular or atomic gaseous precursors (vapor) impinge or diffuse into droplets of molten metals (liquid) on a substrate (solid). Once the droplets are supersaturated by the precursors, these precursors react, leading to nucleation at the droplet/substrate interface and subsequent growth of the first monolayer of the NWs. As a result, a new solid/liquid interface forms between the droplets and the grown NWs. As long as precursors are provided, the process can continue and determine the axial growth of the NWs. The NW growth by the VLS mechanism is catalyzed by the particle on top of the NW, allowing for fast localized growth with efficient use of material [134]. According to the type of catalyst particle, the VLS growth can be classified into foreign metal-catalyzed growth and self-catalyzed growth.

The foreign metal-catalyzed growth is a process in which a foreign metal is carried out as the catalyst. This method enables the growth parameters to be adjusted independently, allowing growth to be optimized with high reproducibility. So far gold (Au) has been the most used catalyst material for the growth of III−V NWs. The first solar cell based on the III-V NWs array is obtained via Au-assisted VLS growth. A disordered array of GaAs NWs with a radial p-n junction was grown by MBE on GaAs(111) substrate [123]. However, Au-assisted VLS growth suffers from some drawbacks when it is applied for the fabrication of Si-based tandem solar cells. Because Au can easily diffuse into bulk Si even at moderate temperatures, creating deep recombination centers and degrading the performances of the Si bottom cell. Besides, the Au particles cannot be removed in situ, an extra post-growth etching step is required to avoid the parasitic light absorption in Au.

Therefore, self-catalyzed VLS growth, in which the catalyst is made of one of the NW elements and can be removed in situ, is required to grow III-V NWs in Si-based tandem solar cells. The first example of self-assisted GaAs NWs grown by MBE was reported by Fontcuberta *et al.* in 2008 [135]. They synthesized GaAs NWs on a GaAs substrate with (111)B orientation by Ga-catalyzed VLS growth. Soon after this, Jabeen *et al.* reported the self-catalyzed growth of GaAs NWs on cleaved facets of Si(100) wafers [136]. This result demonstrated that IIII-V NWs can be directly integrated on Si substrate, thus stimulating the development of III-V NWs/Si tandem solar cells.After synthesizing NWs, the NW arrays are usually planarized by spin-coating with polymer to fabricate devices. The formed planarization surface makes it suitable for depositing contact on top of NWs. Then the polymer is partially etched to expose

the tips of NWs for the deposition of electrical contact. ITO is generally used as the contact for NWs thanks to its high optical transparency and electrical conductivity.

Referring to processes in the literature, we designed the fabrication process of our targeted III-V NWs/Si tandem solar cell. This process is briefly illustrated in Figure 4.7 and it is explained as follows:

- Performing traditional $POCl_3$ thermal diffusion by LYDOP on (111)-oriented p-type Si substrate to form the n^{++} emitter.
- Carrying out B PRTD on the backside of the Si substrate to form the BSF layer. This step is equivalent to the first RTA in air of the two-step RTA to adjust the doping profile of the Si n^{++} emitter.
- Carrying out the second RTA of two-step RTA in N_2 to further adjust the doping profile of the Si n^{++} emitter.
- Implementing the Si p^{++}/n^{++} tunnel junction on the front side of the by B PRTD.
- Fabricating SiO_2 patterned mask by electron beam lithography (by our collaborator at C2N).
- Growing III-V NWs top cell by MBE via self-catalyzed VLS growth (by Marco Vettori at INL).
- Encapsulating III-V NWs by polymer to provide mechanical stability to the cell.
- Etching the polymer to expose the tips of NWs to ensure efficient contact between n-GaAlAs and indium tin oxide (ITO).
- Depositing ITO top contact by sputtering.
- Depositing Al as the front contact.
- Depositing Al or using In-Ga as the back contact.

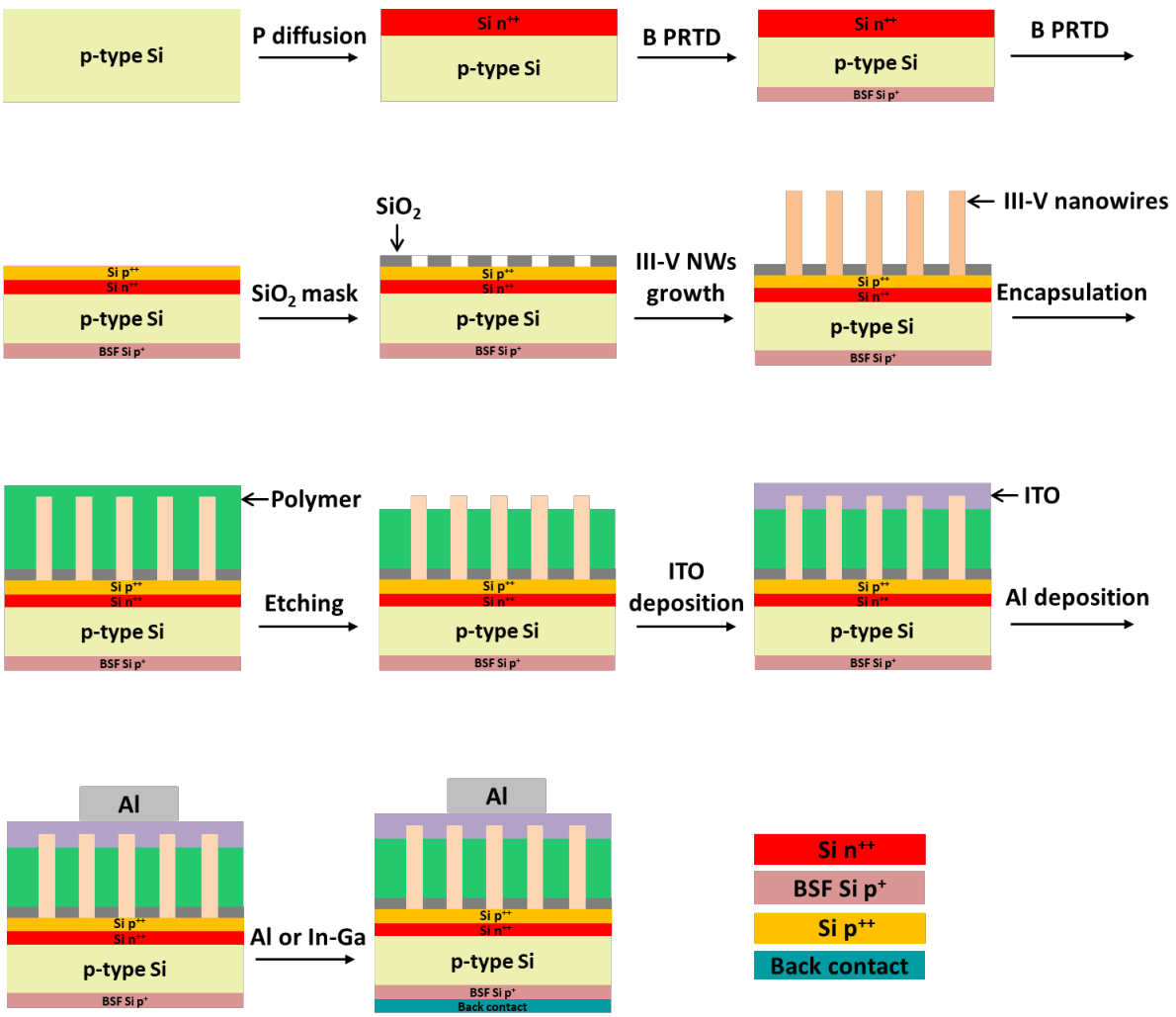


Figure 4.7 *The fabrication process of the NWs/Si tandem solar cell.*

As the fabrication of Si bottom solar cell with p^{++}/n^{++} tunnel junction, SiO_2 patterning, and NWs growth have all been established, the investigations of encapsulation of NWs, etching of polymer, and ITO deposition are reported in the following.

4.3.2 Development of NWs/Si tandem solar cell fabrication process

4.3.2.1 Encapsulation of NWs

To improve the mechanical stability of the NWs top cell, transparent and insulating polymers need to be used to fill the space between nanowires [62], [63], [124]-[128]. The filling polymer also provides a planarization layer for the deposition of a smooth low sheet resistance ITO top contact [63]. Hydrogen silsesquioxane (HSQ) and benzocyclobutene (BCB) are materials commonly used to encapsulate NWs in solar cells [124]-[138]. In this work, we tested both HSQ and BCB as the encapsulation layer.

a) HSQ

HSQ is an inorganic compound with a chemical formula of $(HSiO_{3/2})_n$. Generally, HSQ is deposited on the target sample followed by spin coating and baking. It can be converted to porous silicon oxide after appropriate heat treatment [139]-[142]. The thickness of the silicon oxide layer varies mainly with the set parameters of spin coating as well as the characteristics of NWs.

To investigate the appropriate HSQ encapsulation process project in this study, two 1 × 1 cm^2 patterned Si wafers with epitaxial NWs were first used. They were named as sample H1 and sample H2. The lengths NWs in sample H1 and sample H2 were 1.4 ± 0.1 µm and 2.2 ± 0.1 µm, respectively. A droplet of HSQ was deposited on each sample followed by a spin coating process. For sample H1, the acceleration and speed of spin coating were 1500 rpm/s and 1500 rpm, respectively. While for sample H2, the acceleration and speed of spin coating were 3000 rpm/s and 3000 rpm respectively. The spin coating time was 1 min for both two samples. Both of them were subsequently heated on a hot plate under air ambient at 300 °C for 1 min. Considering the higher acceleration and speed of spin coating for sample H2, the same encapsulation procedure was performed twice on sample H2 to obtain a relatively thick encapsulation layer.

After the HSQ encapsulation process, sample H1 and sample H2 were observed by scanning electron microscope (SEM) and the results are shown in Figure 4.8. The NWs are not completely covered by HSQ in both cases. According to the lengths of NWs and the length of the emerging tips of NWs, the estimated thickness of HSQ in sample H1 and sample H2 is around 1.1 µm and 1.5 µm, respectively. It has been noticed that several cracks appeared on the surface of the encapsulation layer of sample H1, probably caused by improper heat treatment. Dark/bright contrast is observed on the surface of sample H2, showing the inhomogeneity of the encapsulation layer. This might be caused by the two overlapping encapsulation layers.

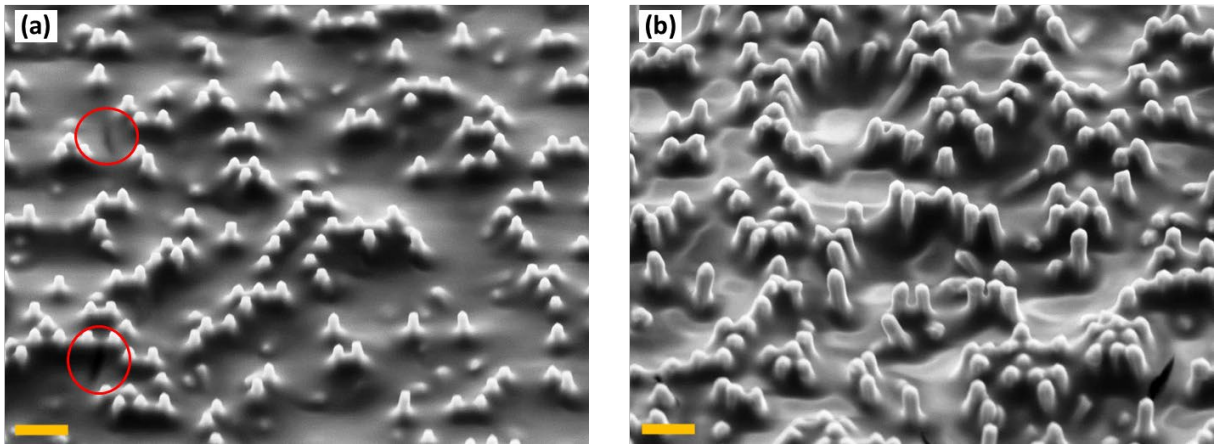


Figure 4.8 *(a) SEM image (45°-tilted) of sample H1 after spin coating and baking of HSQ; (b) SEM image (45°-tilted) of sample H2 after spin coating and baking of HSQ twice. The scale bars correspond to 1 µm.*

Etching of the HSQ was also studied to expose the tips of NWs for the preparation of ITO deposition. Sample H1 was dipped into HF solution (1%) for 40 s. After the etching process, obvious cracks and holes around the NWs are observed, which might be due to the excessive etching time. Thus, sample H2 was dipped into HF solution (1%) for a shorter time of 7 s. However, holes around the NWs are also observed in sample H2, even though they are smaller than the holes in sample H1. Moreover, residues of HSQ are still present on the tips of some NWs, indicating that 7 s is not sufficient.

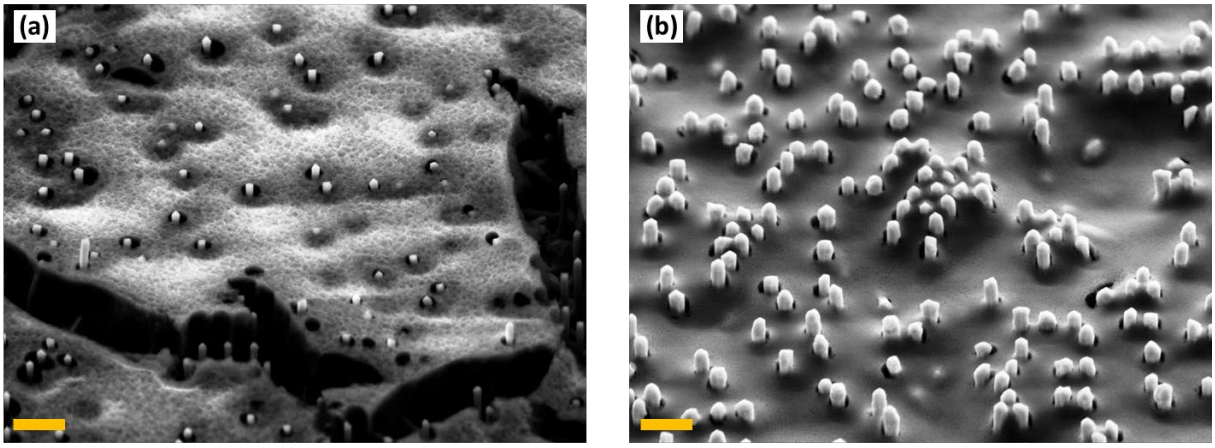


Figure 4.9 *(a) SEM image (45°-tilted) of sample H1 after being etched by HF solution (1%) for 40 s; (b) SEM image (45°-tilted) of sample H2 after being etched by HF solution (1%) for 7 s. The scale bars correspond to 1 µm.*

Therefore, a third patterned Si wafers with epitaxial NWs named as sample H3 was encapsulated by a new process. Considering the homogeneity of the encapsulation layer, the same spin coating process as sample H1 was carried out on sample H3. A three-step annealing process, as shown in Table 4.3, was performed on sample H3. SEM image of sample H3 after

the annealing process is shown in Figure 4.10 (a). The NWs are almost completely covered by HSQ. Then sample H3 was dipped into HF solution (1%) for 10 s. After etching, holes around the NWs appeared and the morphology of some NWs changed, for instance, crooked NWs are observed. Morphological changes of NWs encapsulated by HSQ after baking have also been reported in the literature [143]. The sawtooth structure has been observed in NWs encapsulated by HSQ after baking at a certain temperature. The baking temperature threshold lies between 350 °C and 400 °C. During the annealing process, Si-H bonds dissociate from the HSQ to form silicon oxide. The structure and chemical changes cause the densification and shrinkage of the HSQ layer. Accordingly, a large intrinsic stress is generated inside the encapsulation layer and can transfer to the NWs, resulting in the morphological changes of NWs.

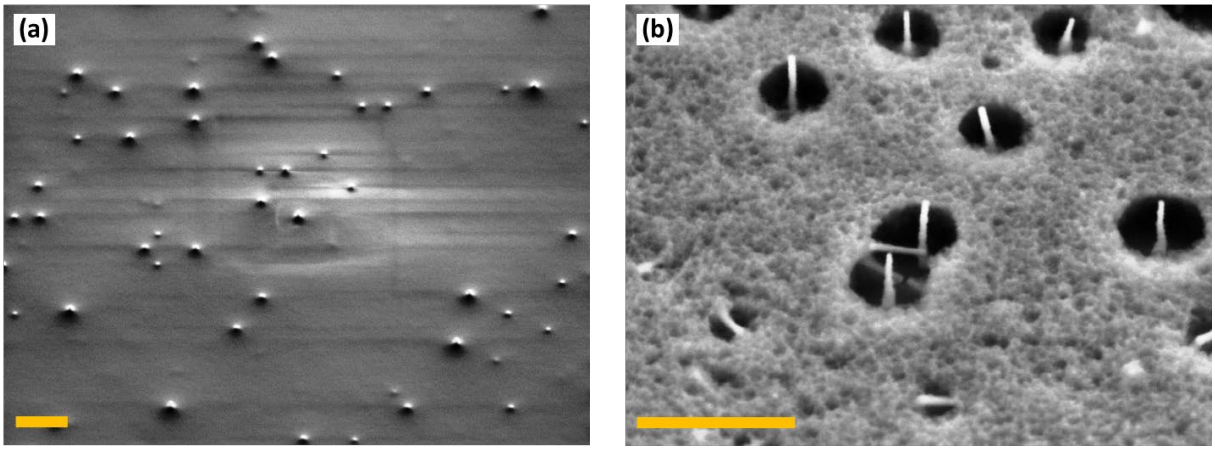


Figure 4.10 *(a) SEM image (45°-tilted) of sample H3 after spin coating and baking of HSQ; (b) SEM image (45°-tilted) of sample H3 after being etched by HF solution (1%) for 10 s. The scale bars correspond to 1 µm.*

Table 4.3 *Annealing parameters of HSQ for sample H3*

Step	Annealing type	Atmosphere	Temperature (°C)	Time
1st	Hot plate	Air	150	20 min
2ed	Hot plate	Air	350	60 min
3rd	RTA	N_2	600	75 s

Other HSQ encapsulation procedures with different heat treatments have also been performed [144]. However, none of them were able to meet the requirement of our study.

b) BCB

Benzocyclobutene (BCB) is a thermosetting polymer that is usually employed in microelectronic circuits and interconnection applications due to its low dielectric constant. It has a chemical formula of C_8H_8. The BCB solution that we used is CYCLOTENE 3022-35 electronic resin produced by Dow Chemical Company.

Similar to HSQ, BCB is liquid at room temperature and turns into a solid state when heated. Generally, it is deposited on the target sample followed by spin coating and heat treatment. The thickness of the BCB layer can be affected by several factors, such as acceleration of spin coating, spin speed, spin time, and the presence of NWs. According to the literature, 1.7-µm-thick BCB can be obtained on a Si wafer when the spin speed is 9000 rpm and the spin time is 30 s [145]. When BCB is used to encapsulate NWs, the thickness of BCB is around 3.5 µm with a spin speed of 3000 rpm for 60 s [146]. Considering that the length of NWs that we used generally varies between 1.2 µm and 2.5 µm, the dependence of deposited BCB thickness on the spin coating process was investigated. For the convenience of measurement, BCB deposition was first carried out on Si wafers.

BCB was deposited on seven identical Si wafers followed by different spin coating processes. These samples were named S1-S7. The acceleration and spin speed of each sample were varied, as shown in Table 4.4. The spin time was set as 80 s to obtain a BCB layer thinner than 3.5 µm and a soft baking process of 90 s at 100 °C was carried out after spin coating to remove the residual solvent. Then the samples were heated in a furnace under N_2 flow to cure BCB. The curing process followed the recommended full cure profile [147]:

- 15-minute ramp to 100 °C;
- 15-minute soak at 100°C;
- 15-minute ramp to 150°C;
- 15-minute soak at 150°C;
- 60-minute ramp to 250°C;
- 60-minute soak at 250°C;
- Cool down to ambient temperature.

The thickness of the BCB layer before and after the curing process was measured by Filmetrics F20 Thin-Film Analyzer. The result in Table 4.4 shows that the thickness of the BCB layer decreases as the acceleration and spin speed increase. The thickness of the BCB layer varies from 750 nm to 1332 nm when the spin coating process changes. A thickness shrinkage of ~ 10% is observed after the curing process.

Table 4.4 *Spin coating parameters of BCB deposition and corresponding thickness of BCB layer before and after curing process.*

	S1	S2	S3	S4	S5	S6	S7
Acceleration of spin coating (rpm/s)	300	300	300	300	500	500	1000
Spin speed of spin coating (rpm)	3000	5000	8000	10000	8000	10000	10000
BCB thickness before curing (nm)	1450	1447	1289	1099	1114	1053	851
BCB thickness after curing (nm)	1332	1287	1155	984	1000	944	750
Shrinkage in curing process (%)	8.1	11.1	10.4	10.5	10.2	10.4	11.9

When encapsulating NWs, the thickness of deposited BCB will increase compared to that deposited on a Si wafer with the same spin coating parameters. What's more, the shrinkage of BCB after curing will introduce intrinsic stress and might damage NWs. To investigate the difference between BCB deposition on the samples with and without the presence of NWs, BCB was deposited on two samples with GaAs NWs grown on unpatterned substrates. These two samples were named N1 and N2. The density, length, and diameter of NWs are similar for the two samples. The density of NWs is about 2 NWs/µm^2. The length of NWs is 2.3 ± 0.3 µm and the diameter of them is 78 ± 8 nm. The SEM images of two samples before BCB deposition are shown in Figure 4.11.

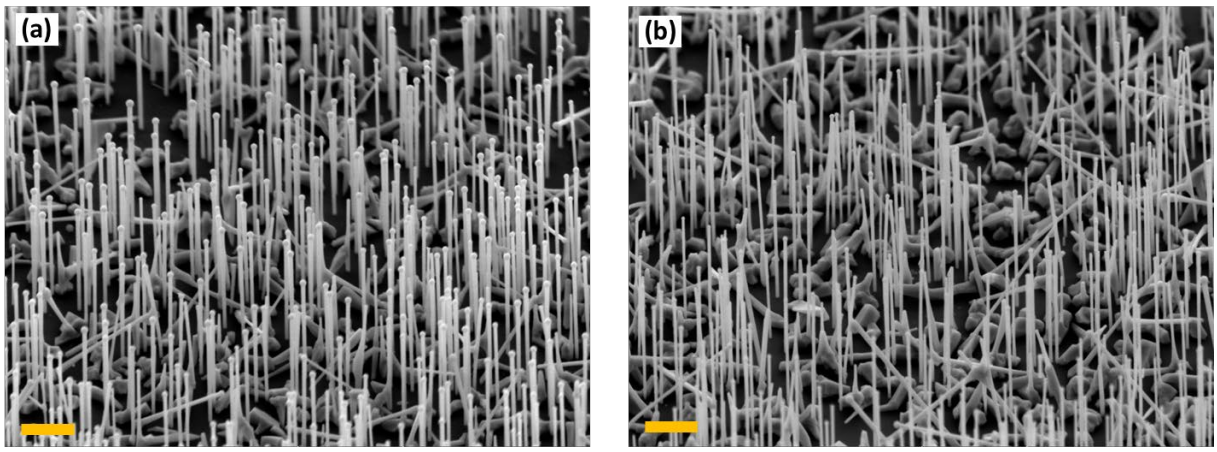


Figure 4.11 *SEM image (45°-tilted) of sample (a) N1 and (b) N2 before BCB deposition. The scale bars correspond to 1 µm.*

Due to the presence of NWs, the thickness of BCB was expected to be thicker when deposited by the same process as on Si wafers. For the convenience of BCB thickness measurement, the spin coating parameters to obtain thin BCB layers were chosen to avoid NWs being fully covered by BCB. Therefore, the spin coating process of samples N1 and N2 was set to be the same as that of samples S6 and S7, respectively. The spin time of samples N1 and N2 was 80 s and the spin speed was 10000 rpm. The acceleration of spin coating was 500 rpm/s for sample N1 while it is 1000 rpm/s for sample N2. After deposition, the same soft baking process as above was performed on the two samples. Then the samples were observed by SEM before the curing process. The cross-section SEM images of samples N1 and N2 are shown in Figure 4.12 (a) and Figure 4.12 (b), respectively. The thickness of the BCB layer is about 1927 nm in sample N1 while it is about 1708 nm in sample N2. Compared with the BCB thickness of sample S6 and S7 after the soft baking process, which is 1053 nm and 851 nm respectively, the BCB thickness of sample N1 and N2 approximately doubled.

The same curing process as above was performed on samples N1 and N2. SEM images of samples N1 and N2 after curing are shown in Figure 4.12 (c) and Figure 4.12 (d), respectively. After curing, the NWs did not bend and no hole was observed around the NWs. Besides, there was no crack on the surface. This result demonstrates that NWs can be well encapsulated by BCB through the encapsulation process described above.

However, NWs clusters were observed after BCB encapsulation. This is due to the insufficient time between BCB deposition and spinning. After BCB deposition, it is recommended to wait 12 min for the BCB solution to penetrate to the root of the NWs [148]. Whereas, we started the spinning process directly after depositing BCB on the samples. For the following samples, the clusters can be avoided if we leave enough time during the BCB deposition and spinning. Besides, the NWs clusters can also be avoided when the density of NWs decreases.

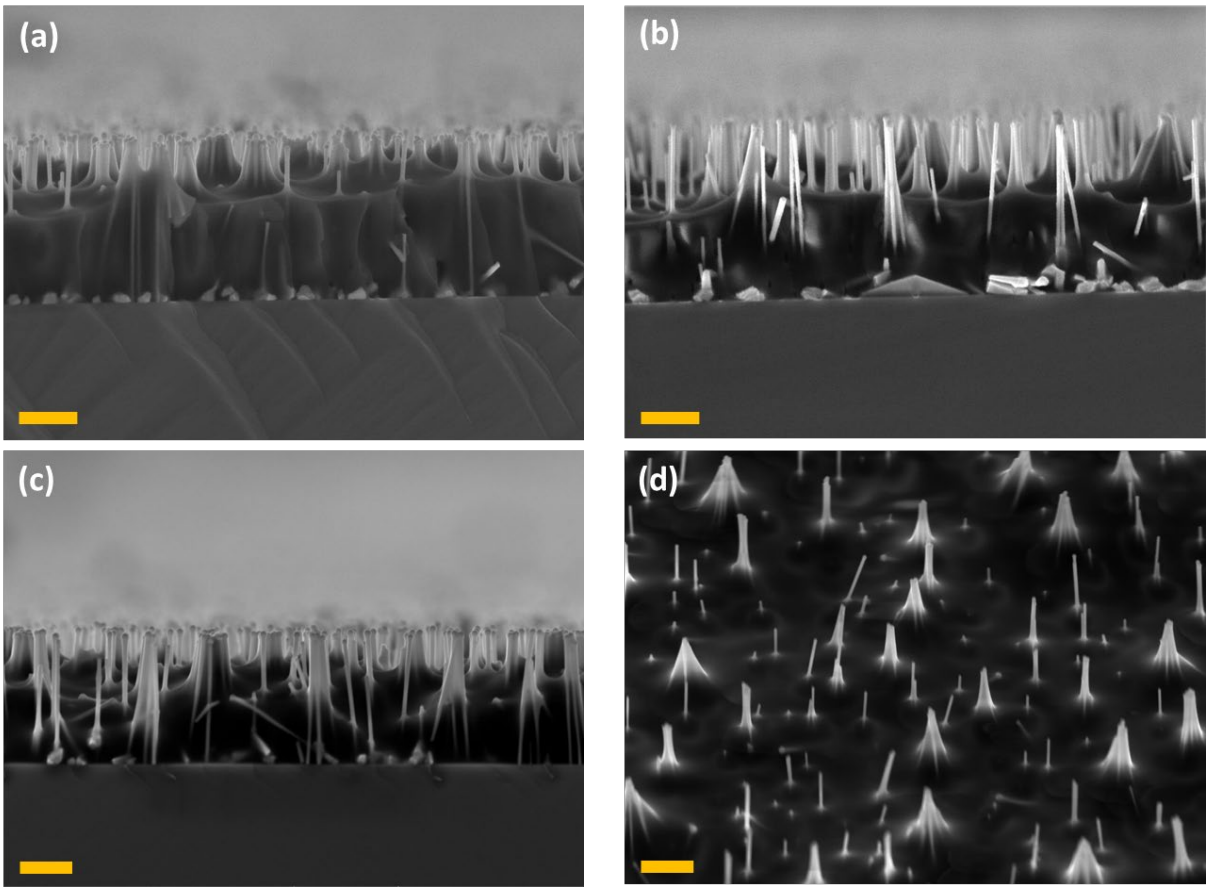


Figure 4.12 *Cross-section SEM image of sample (a) N1 and (b) N2 after soft baking of BCB; SEM image (45°-tilted) of sample (c) N1 and (d) N2 after the BCB curing process. The scale bars correspond to 1 µm.*

4.3.2.2 Etching of polymer

After being encapsulated by BCB, the tips of the NWs should be exposed for the deposition of ITO contact. BCB can be etched by SF_6/O_2 in the RIE reactor [149]. To investigate the etch rate, RIE etching of BCB was first carried out on samples S1-S7, which have BCB on Si wafers. The samples were etched at 100 mTorr chamber pressure under a 1:4 gas mixture of SF_6:O_2 (SF_6=5 sccm, O_2=20 sccm). The influence of RF power on etching rate was studied. The RF power was set as 50 W, 70W, and 100 W to etch difference samples. The BCB etching rate result is shown in Figure 4.5 and Figure 4.13. The etching rate increases almost linearly with increasing RF power. The etching rate changed from 216 nm/min to 474 nm/min as the RF power increased from 50 W to 100 W.

Table 4.5 *Dependence of the BCB etching rate on RF power of plasma RIE.*

RF power (W)	Sample	Etching rate (nm/min)	Average etching rate (nm/min)
100	S1	474	474
70	S2	344	324
	S3	327	
	S4	300	
50	S5	203	216
	S6	239	
	S7	206	

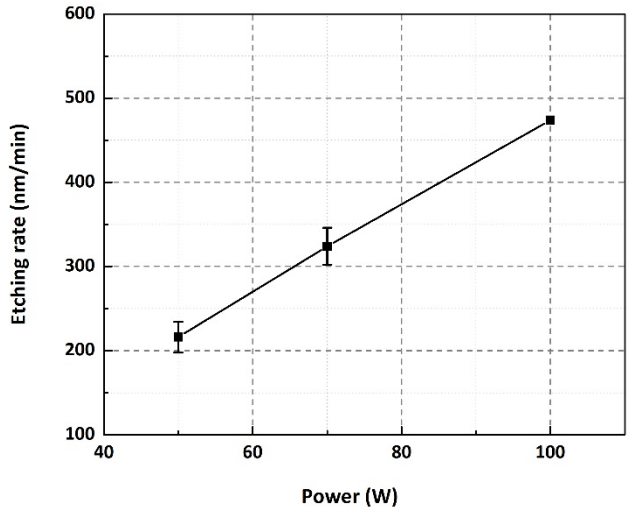


Figure 4.13 *Dependence of the BCB etching rate on RF power of plasma RIE.*

When the same etching process was performed on samples with NWs, the etching rate was expected to be different. To reduce the impact of BCB etching on NWs, low RF power of 50 W was chosen to etch the samples with NWs.

Sample N1 was cut into two pieces and they were etched for 2 min and 4 min, respectively. After etching, they were observed by SEM and the results are shown in Figure 4.14. The BCB covering on the tips of NWs has been completely removed after etching except for those in NWs clusters. What's more, the NWs were not damaged during the etching process. For the one etched for 4 min, some holes appeared around the NWs, indicating that it was over-etched.

According to the statistical result, the average length of the exposed tips in the sample after 2-min etching is 1053 nm while it is 1269 nm in the one after 4-min etching. The BCB etching rate for this sample with NWs is 108 nm/min, which is about half of the etching rate of BCB on Si wafers.

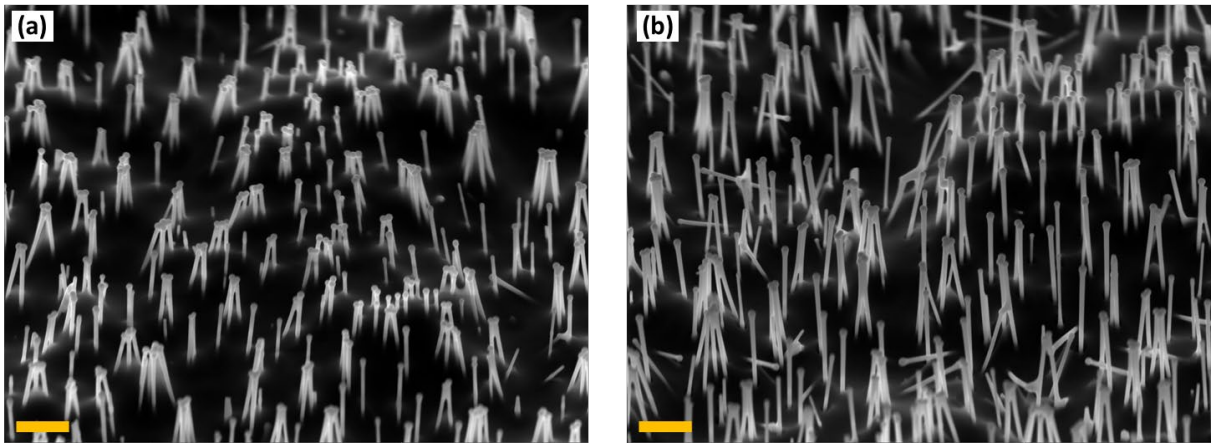


Figure 4.14 *SEM image (45°-tilted) of sample N1 etched by RIE for (a) 2 min and (b) 4 min. The scale bars correspond to 1 µm.*

Because the purpose of BCB etching is to expose the tips of NWs, it is not necessary to etch too much BCB. Therefore, a 1-min etching was performed on sample N2 to verify whether a short-time etching is sufficient to obtain BCB-free tips. Figure 4.15 shows that 1 min is enough to remove all the BCB covering on the tips of NWs except for those in NWs clusters. The average length of the exposed tips before and after etching is 1015 nm and 1118 nm, respectively. Thus the etching rate for this sample is about 103 nm/min, similar to the result of sample N1.

The same problem of samples N1 and N2 during etching is that the BCB in NWs clusters cannot be removed ideally. This problem can be solved automatically if the BCB encapsulation process is optimized by waiting 12 min before starting spinning to avoid the formation of NWs clusters. To verify this assumption, BCB encapsulation was performed on a third sample with NWs grown on an unpatterned substrate. This sample was referred to as sample N3.

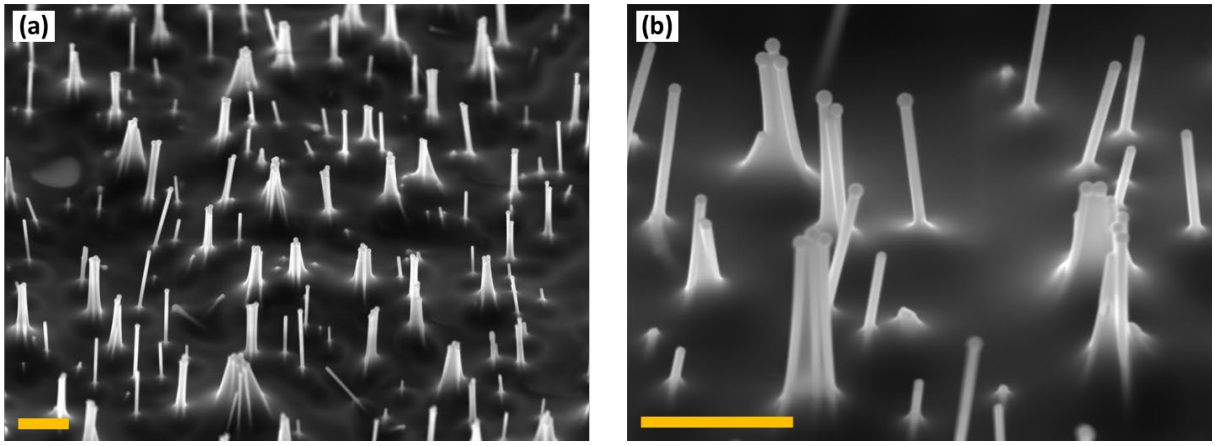


Figure 4.15 *SEM image (45°-tilted) of sample N2 etched by RIE for 1 min. The scale bars correspond to 1 µm.*

Sample N3 has p-n core/shells GaAs/$Al_{0.2}Ga_{0.8}As$ NWs on the surface. The length of NWs of sample N3 is 1.2 ± 0.1 µm and the diameter of NWs is 238 ± 16 nm. These NWs are shorter and thicker than the NWs of samples N1 and N2. The density of NWs is about 5.0 NWs/μm^2, higher than that of samples N1 and N2. After depositing BCB on sample N3, we waited 12 min before started the spinning process. The spinning process of sample N3 was the same as that of sample N2, with an acceleration of 1000 rpm/s and a spin speed of 10000 rpm. The same soft-baking and curing process as described above was carried out on sample N3.

SEM images of sample N3 before and after the BCB encapsulation process are shown in Figure 4.16. The NWs have been homogeneously covered by BCB and no crack was observed. The thickness of BCB is close to the length of NWs. After 1 min of etching, the BCB on the tips of NWs has been removed. According to the statistical result, the diameter of NWs is almost the same as before etching. It indicates that the employed etching process can effectively remove the BCB from the tips of NWs without damaging the NWs.

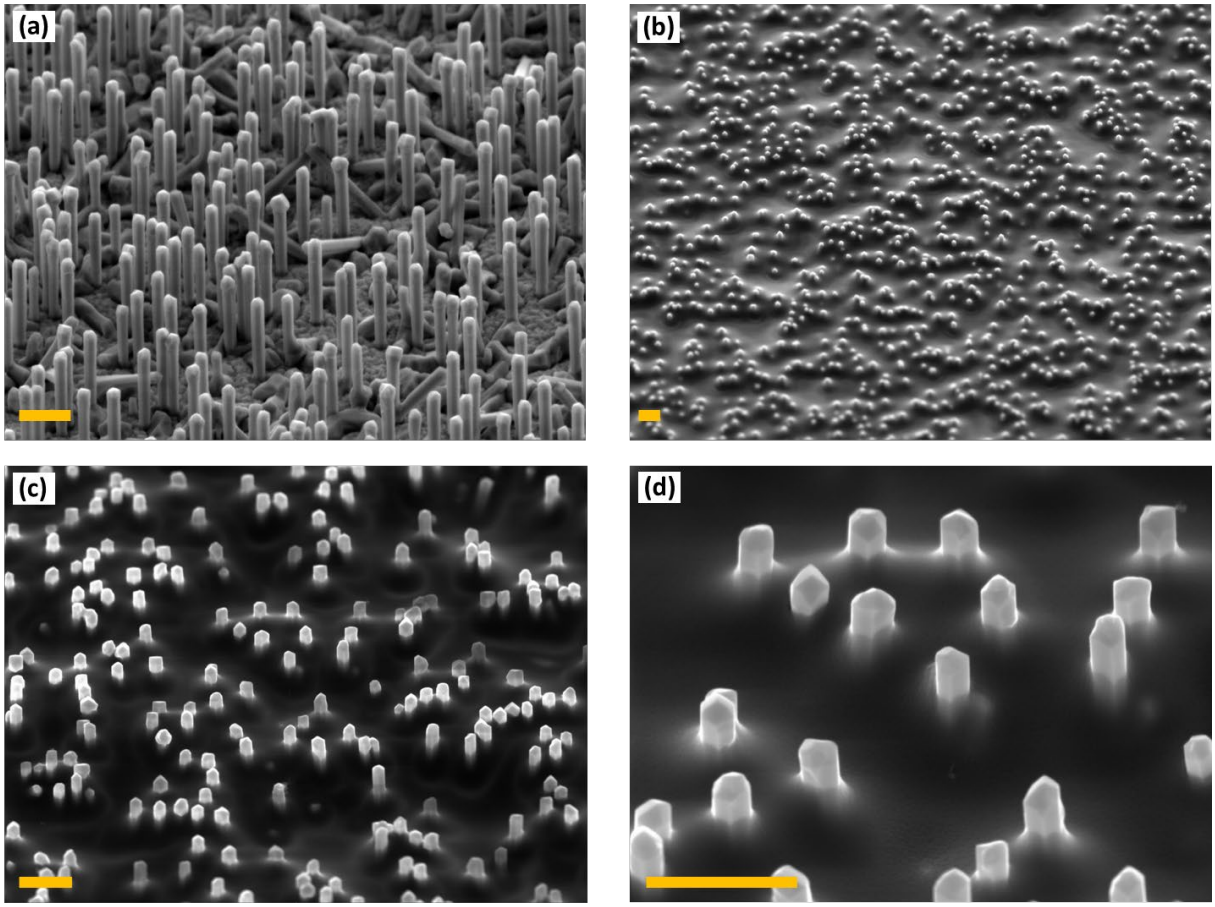


Figure 4.16 *SEM image (45°-tilted) of sample N3 (a) before and (b) after BCB encapsulation process; (c) and (d) SEM image (45°-tilted) of sample N3 etched by RIE for 1 min. The scale bars correspond to 1 µm.*

After testing on NWs grown on unpatterned substrates, one more test was carried out on a sample with NWs grown on the patterned substrate. This patterned sample, named sample N4, has p-n core/shell GaAs/$Al_{0.2}Ga_{0.8}As$ NWs. The length of NWs is about 2.5 µm and the diameter is 220 ± 7 nm. SEM images of the central and edge area of sample N4 after the BCB encapsulation process are shown in Figure 4.17 (a) and Figure 4.17 (b). The thickness of BCB is close to the length of NWs at the edge area. The sample was etched for 30 s to remove the BCB covering on the tips of NWs. As shown in Figure 4.17 (c) and Figure 4.17 (d), 30 s of etching is sufficient to obtain BCB-free tips. After etching, the diameter of NWs is 218 ± 21 nm, similar to that before etching. This result indicates that sample N4 is ready for the ITO deposition process.

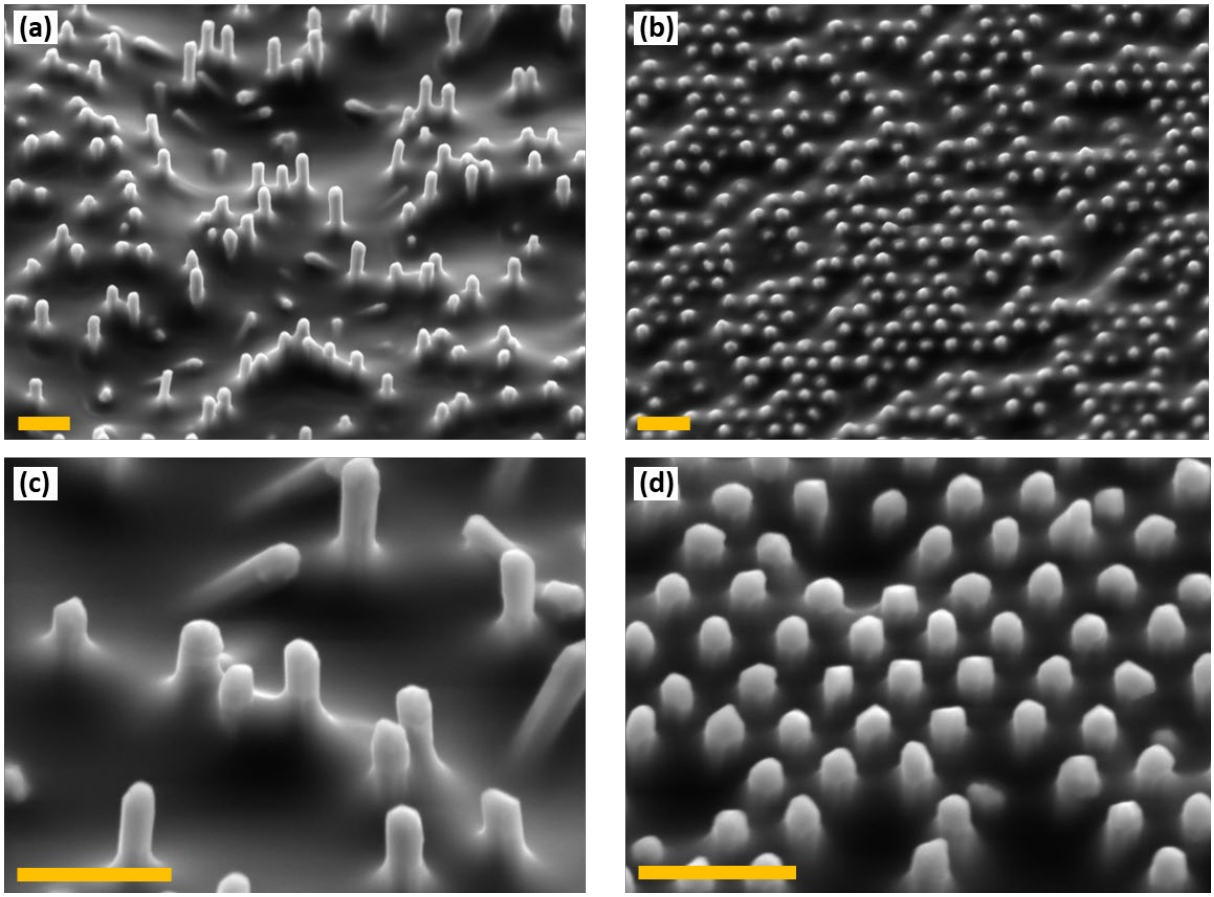


Figure 4.17 *SEM image (45°-tilted) of the (a) central and (b) edge area of sample N4 after BCB encapsulation process; SEM image (45°-tilted) of the (c) central and (d) edge area of sample N4 etched by RIE for 30 s. The scale bars correspond to 1 µm.*

4.3.2.3 ITO contact deposition

To form the front ITO contact, 25 nm of indium (In) and 100 nm of ITO was deposited on sample N4. The In was deposited by evaporation while ITO was deposited by magnetron sputtering. The insertion of In layer between ITO and NWs aims to reduce the sheet resistance of the contact layer. According to the literature, the sheet resistance of annealed ITO (500 nm) film on the glass slide is 21 Ω/□, while that is 13 Ω/□ for annealed In/ITO (25/500 nm) film [150]. The samples were annealed at 400 °C for 30 s in N_2 ambient in these cases. However, given the glass transition temperature of BCB, the annealing temperature of ITO contact was decided to be no more than 350 °C in this work [151]-[153]. Therefore, sample N4 was annealed at 250 °C for 4 min under N_2 flow following the annealing procedure mentioned in the literature [63].

SEM images of sample N4 after ITO annealing are shown in Figure 4.18. Extremely granular ITO is observed on the surface. This might be caused by the evaporated In layer,

whereas in the literature the sputtered In could be more uniform [63]. The granular ITO would degenerate the optoelectronic properties of the solar cell if it was used as the top contact. Considering that the In cannot be deposited by sputtering in our laboratory, we decided to adopt the sole ITO as the top contact for NWs.

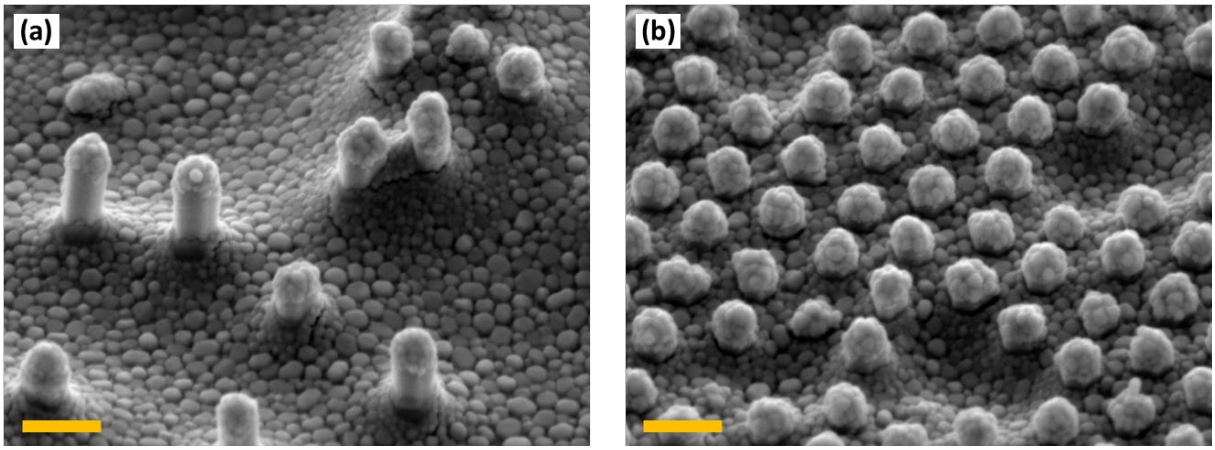


Figure 4.18 *SEM image (45°-tilted) of the sample N4 after In/ITO deposition and annealing at 250 °C for 4 min under N_2 flow. The scale bars correspond to 500 nm.*

To reuse sample N4 for ITO deposition tests, sample N4 was dipped into Hydrochloric acid (HCl) aqueous solution (1:1 HCl to DI water volumetric ratio, where HCl is the standard 37% HCl solution) for 10 min to remove the deposited In and ITO [154]. SEM images of sample N4 after removal of In/ITO are shown in Figure 4.19. The ITO granule on the surface has been removed and some holes appeared around the NWs. For the following test, the influence of the holes is negligible as the purpose of the test is to study the performance of the deposited ITO.

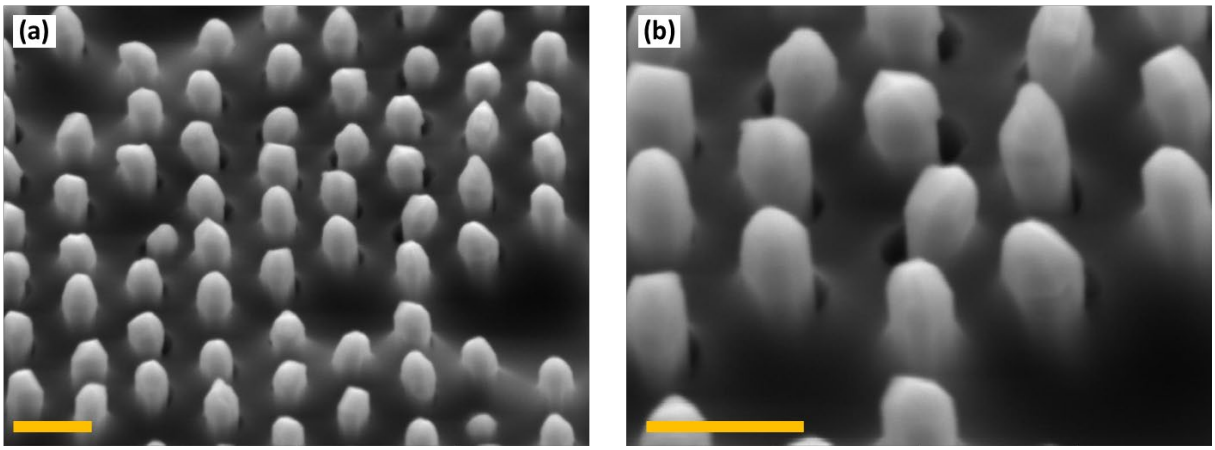


Figure 4.19 *SEM image (45°-tilted) of the sample N4 after the removal of In/ITO layer. The scale bars correspond to 500 nm.*

100 nm of ITO was redeposited by magnetron sputtering on sample N4 followed by an

anneal at 250 °C for 30 min under N_2 flow. After annealing, uniform ITO was observed on the tips of NWs and the surface of sample N4, as shown in Figure 4.20. Some tips of the NWs were not completely covered by ITO at the area near the holes. This phenomenon can be avoided if the tips of NWs are less exposed and more ITO is deposited.

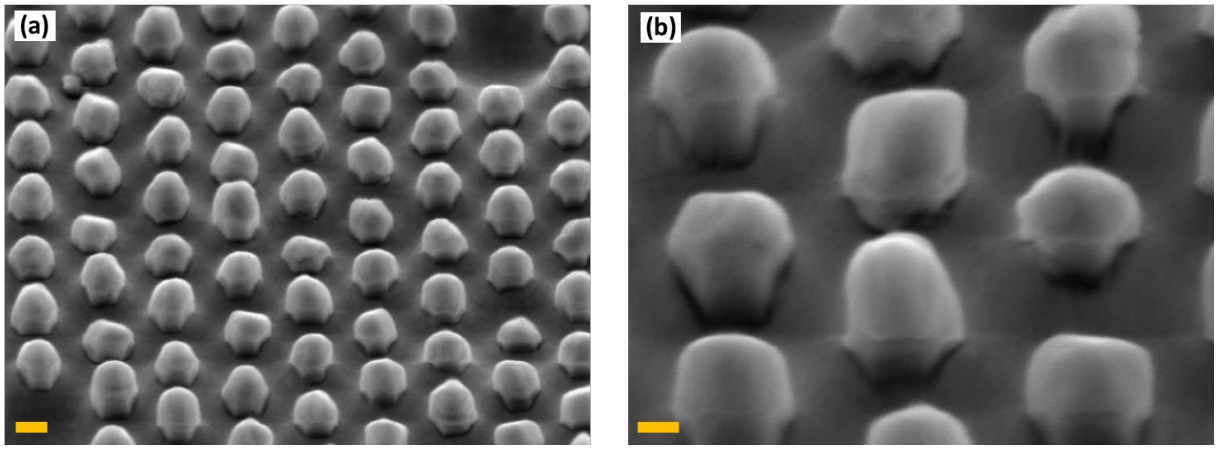


Figure 4.20 *SEM image (45°-tilted) of sample N4 after the redeposition of 100-nm ITO and annealing at 250 °C for 30 min under N_2 flow. The scale bars correspond to 500 nm.*

Considering that a long-time anneal may reduce the sheet resistance of ITO, a further anneal at 250 °C for 120 min under N_2 flow was performed on sample N4 to test the thermal stability of deposited ITO. The result of ITO on sample N4 after two anneals is shown in Figure 4.21. No noticeable changes were observed compared with the results obtained after the first anneal. It indicates that the deposited ITO can sustain an anneal at 250 °C for at least 150 min.

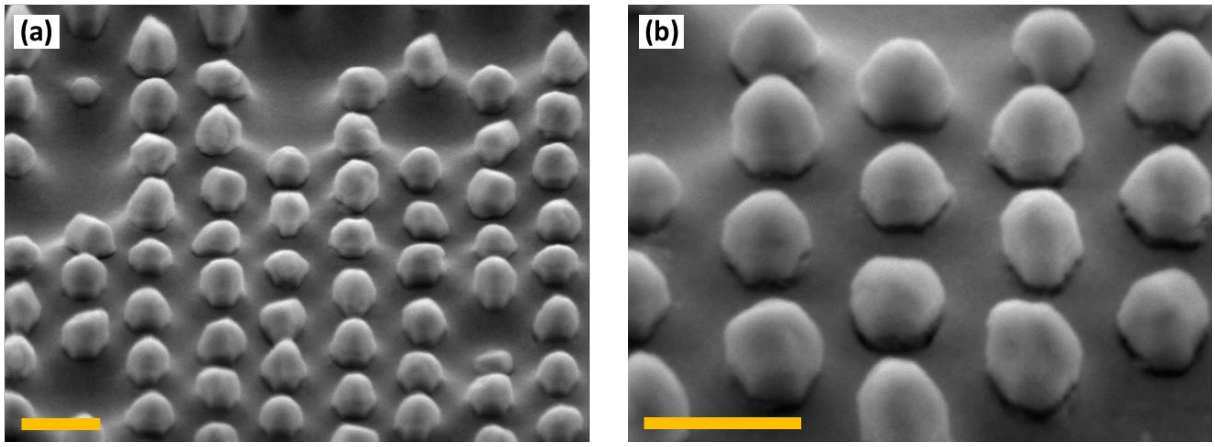


Figure 4.21 *SEM image (45°-tilted) of sample N4 after the redeposition of 100-nm ITO and annealing at 250 °C for 150 min (30 min + 120 min) under N_2 flow. The scale bars correspond to 500 nm.*

Simultaneously, the effect of the annealing process on ITO sheet resistance and ITO/$Al_{0.2}Ga_{0.8}As$ specific contact resistance was also investigated.

a) Sheet resistance of ITO

To study the impact of the annealing process on ITO sheet resistance, ITO was deposited by magnetron sputtering on a GaAs substrate. Three series of samples with different thicknesses of ITO were obtained. They were named series I1, I2, and I3. Each series has four identical samples, named 1, 2, 3, and 4. The sheet resistance of these samples before annealing is shown in 0. It shows that the sheet resistance increases as the ITO thickness decreases.

Table 4.6 *Thickness and sheet resistance before annealing of series I1, I2, and I3 samples.*

Series name	Thickness (nm)	Sheet resistance before annealing (Ω/□)
I1	122	302
I2	111	322
I3	80	327

Firstly, the effect of annealing time on sheet resistance was studied. Six samples, two from each series, were annealed at 250 °C for 30 or 120 min under N_2 flow. The sheet resistance of them after anneal is shown in Table 4.7. The ratio of sheet resistance before and after annealing was also calculated. The result indicates that the impacts of annealing at 250 °C for 30 min and 120 min are comparable for the samples. Therefore, given the thermal budget, 30 min of annealing is adopted for the following tests.

Table 4.7 *Sheet resistance of series I1, I2, and I3 samples after annealing at 250 °C for 30 or 120 min under N_2 flow.*

Annealing time (min)	Sample	Sheet resistance after annealing (Ω/□)	Ratio of sheet resistance before and after annealing
30	I1-1	52	5.9
	I2-1	53	6.1
	I3-1	69	4.7
120	I1-2	59	5.2
	I2-2	56	5.8
	I3-2	63	5.2

Secondly, the effect of annealing temperature on sheet resistance was studied. Another six samples, two from each series, were annealed for 30 min at 300 °C, or 350 °C under N_2 flow.

The sheet resistance after annealing and the ratio of sheet resistance before and after annealing are shown in Table 4.8. The result suggests that the sheet resistance of the samples annealed at 350 °C is significantly lower than the other samples.

The above results indicate that annealing at 350 °C for 30 min under N_2 flow is appropriate to get a low sheet resistance of ITO.

Table 4.8 *Sheet resistance of series I1, I2, and I3 samples after annealing for 30 min at 250, 300, or 350 °C under N_2 flow.*

Annealing temperature (°C)	Sample	Sheet resistance after annealing (Ω/□)	Ratio of sheet resistance before and after annealing
250	I1-1	52	5.9
	I2-1	53	6.1
	I3-1	69	4.7
300	I1-3	47	6.4
	I2-3	53	6.1
	I3-3	65	5.0
350	I1-4	44	6.9
	I2-4	33	9.8
	I3-4	47	7.0

b) Specific contact resistance between ITO and $Al_{0.2}Ga_{0.8}As$

Apart from the sheet resistance of ITO, the impact of the annealing process on the specific contact resistance between ITO and $Al_{0.2}Ga_{0.8}As$ was also investigated. A similar ITO TLM pattern as described in Chapter 3 was fabricated. 100 nm of ITO was deposited on an n^+-$Al_{0.2}Ga_{0.8}As$/GaAs substrate by magnetron sputtering. The thickness of the n^+-$Al_{0.2}Ga_{0.8}As$ layer is 200 nm and its doping concentration is 1.6×10^{19} cm^{-3}. For measurement convenience, 400 nm of Al was also deposited on ITO by evaporation. The ITO TLM configuration is shown in Figure 4.22.

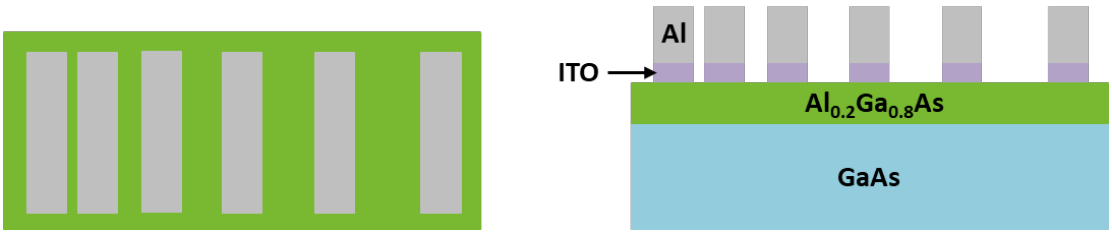


Figure 4.22 *Top view (left) and side view (right) of the fabricated Al/ITO TLM configuration on $Al_{0.2}Ga_{0.8}As$/GaAs substrate.*

Various annealing treatments under N_2 flow were carried out on three different samples, as shown in Table 4.9. The lowest ITO/n^+-$Al_{0.2}Ga_{0.8}As$ specific contact resistance was observed on the sample annealed at 350 °C for 30 min, which is 4.84 × 10^{-2} Ω·cm^2. This result is comparable to the specific contact resistance of ITO/n^+-GaAs reported in the literature [150], [155]. When the doping level of GaAs is 1.5 × 10^{19} cm^{-3}, the specific contact resistance of ITO/n^+-GaAs varies from 10 Ω·cm^2 to 3 × 10^{-2} Ω·cm^2 as the annealing temperature changes from 200 °C to 500 °C [155]. As mentioned before, the annealing temperature for ITO in this work should be no more than 350 °C considering the existence of BCB. What's more, the annealing process to obtain the lowest ITO/n^+-$Al_{0.2}Ga_{0.8}As$ specific contact resistance is consistent with the annealing process to obtain the lowest sheet resistance of ITO. Thus, an anneal at 350 °C for 30 min under N_2 flow was decided to be performed on the NWs/Si tandem solar cell.

Table 4.9 *Specific contact resistance of ITO/n^+-$Al_{0.2}Ga_{0.8}As$ after annealing.*

Temperature (°C)	Time (min)	Equipment	Specific contact resistance (Ω·cm^2)
300	30	Tubular furnace	9.50 × 10^{-2}
350	1	ADDAX RTA	1.22 × 10^{-1}
350	30	Tubular furnace	4.84 × 10^{-2}

4.3.2.4 Realization of NWs/Si tandem solar cell

After the investigations of encapsulation of NWs, etching of BCB, and ITO deposition, two 1 × 1 cm^2 NWs samples named C1 and C2 were adopted to fabricate solar cells. Sample C1 was used to fabricate p-i-n GaAs NWs single-junction solar cell while sample C2 was used to fabricate GaAs/$Al_{0.2}Ga_{0.8}As$ NWs/Si tandem solar cell. The configuration of samples C1 and C2

are shown in Figure 4.23. In sample C1, radial p-i-n GaAs NWs were grown on a (111)-oriented p^+-type Si substrate. In sample C2, radial GaAs/$Al_{0.2}Ga_{0.8}As$ core-shell NWs were grown on a (111)-oriented p-type Si substrate with a p^{++}/n^{++} tunnel junction on the front side and a BSF layer on the backside. The patterned area in these two samples was 0.9 cm x 0.9 cm. Both the NWs in samples C1 and C2 have an $Al_{0.5}In_{0.5}P$ passivation shell.

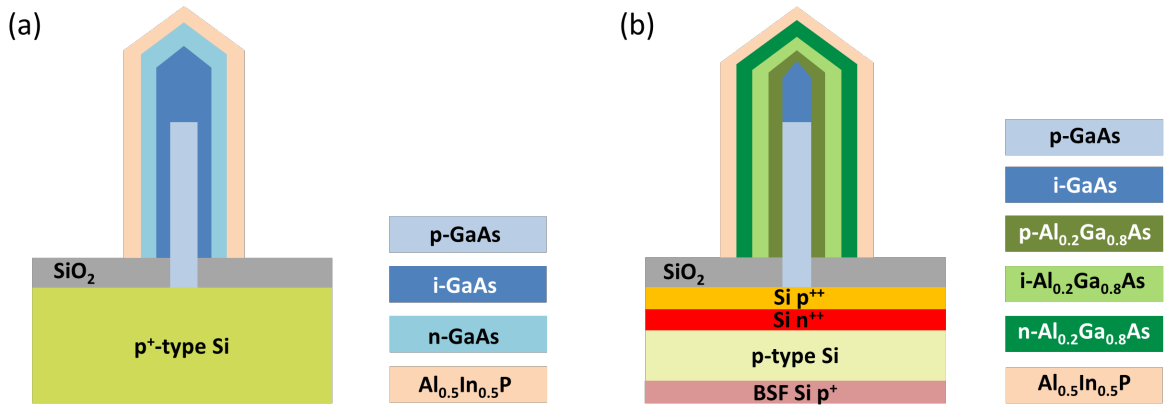


Figure 4.23 *The configuration of samples (a) C1 and (b) C2 before encapsulation.*

SEM images of samples C1 and C2 before encapsulation are shown in Figure 4.24 (a) and Figure 4.24 (b). The length of NWs is about 2.5 µm in both samples. The diameter of NWs in samples C1 and C2 is 217 ± 8 nm and 182 ± 11 nm, respectively. The vertical yield of NWs is ~ 90% in sample C1 while that is ~ 65% in sample C2. A droplet of BCB was deposited on samples C1 and C2 respectively. After waiting 12 minutes, the samples were spun for 80 s at 10000 rpm. The acceleration of spin coating was 1000 rpm/s. Soft baking and cure were carried out after the spin coating process. As a result, NWs in samples C1 and C2 were homogeneously embedded in the BCB layer, as shown in Figure 4.24 (c) and Figure 4.24 (d). To expose the tips of NWs, sample C1 was etched by RIE for 30 s and sample C2 was etched for 1 min. Figure 4.24 (e) and Figure 4.24 (f) show that the BCB on the tips of NWs has been removed and samples C1 and C2 are ready for ITO deposition. The exposed $Al_{0.5}In_{0.5}P$ passivation layer was removed by HCl (10%, 25 s) just before the ITO deposition. 150 nm of ITO was deposited by sputtering at room temperature followed by annealing at 350 °C for 30 min under N_2 flow. After annealing, conformal ITO coating was observed on the surface of samples C1 and C2, shown in Figure 4.24 (g) and Figure 4.24 (h). For the convenience of measurement, an array of Al spots was deposited by evaporation as the front contact after photolithography. The Al spots have a diameter of 200 µm and a period of 2 mm. Samples C1 and C2 were pasted on a copper sheet by In-Ga alloy for the *J-V* characterization. In-Ga alloy also functioned as the back contact of

the solar cell.

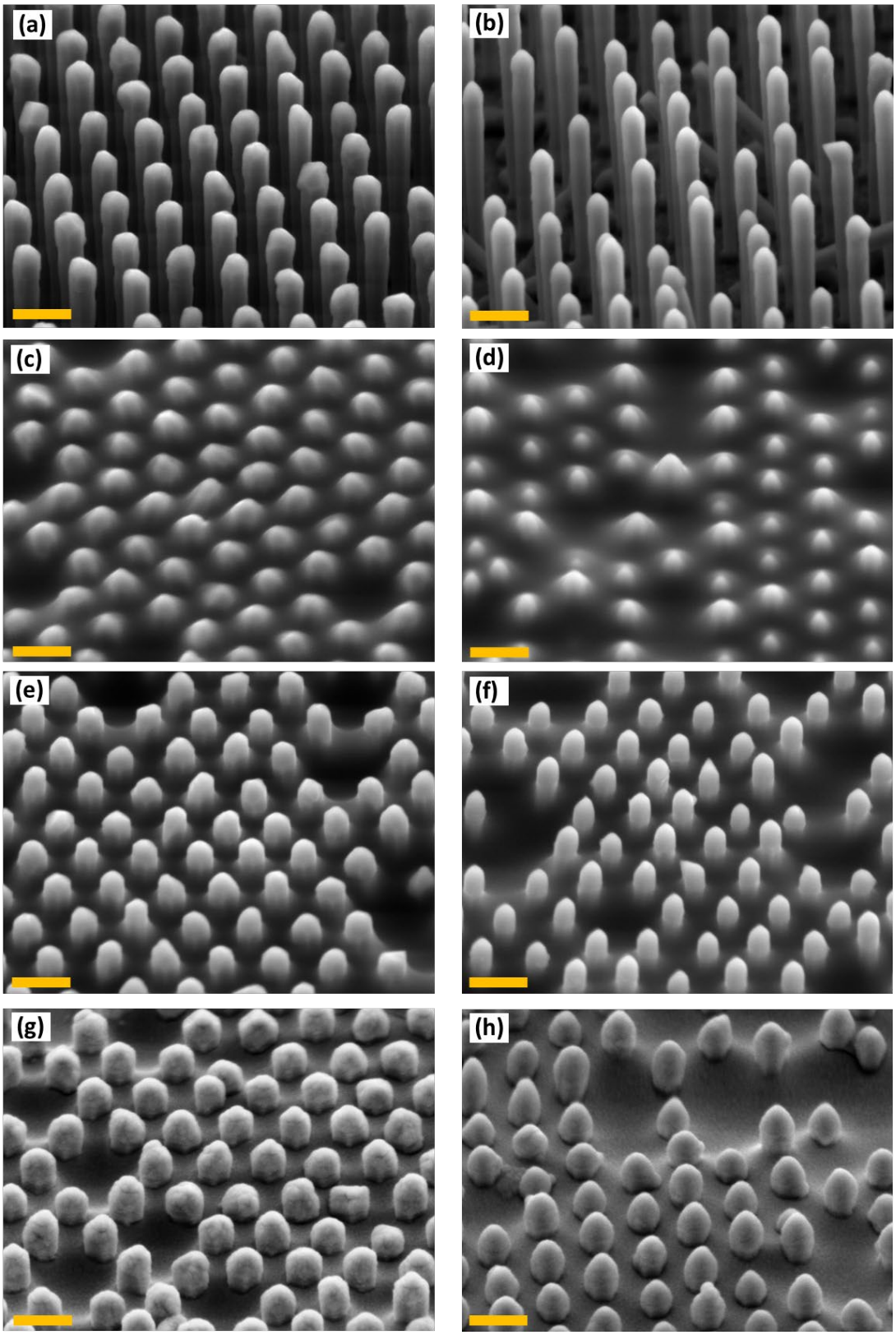


Figure 4.24 *SEM image (45°-tilted) of samples (a) C1 and (b) C2 before encapsulation; samples (c) C1 and (d) C2 after BCB encapsulation and cure; samples (e) C1 and (f) C2 etched by RIE for 30 s and 1 min respectively; samples (g) C1 and (h) C2 after 150-nm ITO deposition followed by annealing at 350 °C for 30 min under N_2 flow. The scale bars correspond to 500 nm.*

4.3.3 *J-V* characterization of NWs/Si tandem solar cell

Before current density-voltage (*J-V*) measurement, the edge of samples C1 and C2 were cut by laser to avoid the edge effect. After cutting, the size of samples C1 and C2 became 6 × 6 mm^2 and 8 × 8 mm^2, respectively. The *J-V* characterization of the samples C1 and C2 was carried out under the dark condition and AM1.5 spectrum condition. The dark and light *J-V* curves of samples C1 and C2 are shown in Figure 4.25.

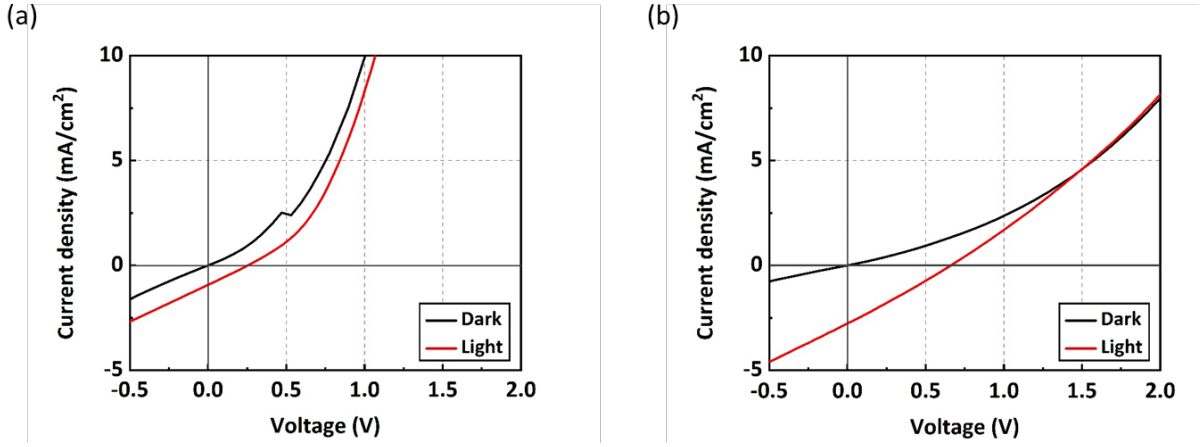


Figure 4.25 *Dark and light J-V of samples (a) C1 (p-i-n GaAs NWs solar cell) and (b) C2 (GaAs/$Al_{0.2}Ga_{0.8}As$ NWs/Si tandem solar cell).*

Diode behavior was observed under both dark and illuminated conditions in samples C1 and C2. An open-circuit voltage (V_{oc}) of 0.25 V is observed in sample C1 while that is 0.66 V in sample C2. It should be noticed that the V_{oc} of sample C2 is higher than that of our fabricated standard single-junction Si solar cell, which is 0.59 V (shown in section 4.2.2.1, Table 4.1). It indicates that the p^{++}/n^{++} Si tunnel junction produced by PRTD electrically connects the III-V NWs top cell and Si tandem solar cells. The short-circuit current density of samples C1 and C2 is 0.92 mA/cm^2 and 2.77 mA/cm^2 respectively. The performance of GaAs/$Al_{0.2}Ga_{0.8}As$ NWs/Si tandem solar cell is better than p-i-n GaAs NWs single-junction solar cell.

However, the performance improvement in the tandem solar cell is much lower than expected. This inferior performance may be caused by several issues. First, the shunt resistance of the top cell is too low. As the vertical yield is not 100%, some NWs were not straight or absent thus generated some local shunts. The tilted or broken NWs can also degrade light absorption by introducing unwanted shadows and disrupting the period of NWs array. Besides, the doping concentration of n-$Al_{0.2}Ga_{0.8}As$ NWs is unknown. The contact between ITO and $Al_{0.2}Ga_{0.8}As$ NWs might be a Schottky contact rather than an Ohmic contact, which could

lead to poor carrier collection.

The performance of the tandem solar cell could be improved by three possible ways. Firstly, the vertical yield of NWs should be increased to 100% to prevent the local shunts and unwanted shadows. Secondly, the contact between ITO and n-$Al_{0.2}Ga_{0.8}As$ NWs should be optimized to obtain an Ohmic contact. Highly doped $Al_{0.2}Ga_{0.8}As$ NWs and a proper annealing process are required. Thirdly, localized p^{++}/n^{++} Si tunnel junction can be used instead of planar tunnel junction to reduce the recombination on the surface of Si bottom solar cell.

All NWs reported above were grown at INL by Dr. Marco VETTORI.

4.4 Conclusion

The implementation of p^{++}/n^{++} Si tunnel junction in single-junction Si solar cells and III-V NWs/Si tandem solar cells have been reported in this chapter. Compared to the fabricated standard Si solar cell whose efficiency is 13.09%, the efficiency of the single-junction Si solar cell with planar p^{++}/n^{++} Si tunnel junction on the surface decreased to 5.67%. This performance degradation is mainly caused by the high series contact resistance between Al front contact and p^{++}-Si. Besides, the recombination of minority carriers generated in the tunnel junction and surface recombination reduced the carrier collection capability. To reduce the surface recombination, a solar cell with localized tunnel junctions beneath the front contact was fabricated, achieving maximum efficiency of 10.43%. It suggests that the performance of tandem solar cells can be improved by replacing the planar tunnel junction with the localized tunnel junction in the bottom solar cell.

To investigate the effectiveness of the p^{++}/n^{++} Si tunnel junction in tandem solar cells, the fabrication and characterization of GaAs/$Al_{0.2}Ga_{0.8}As$ NWs/Si tandem solar cells have been presented. A p-i-n GaAs NWs single-junction solar cell was also fabricated as the reference. Before implementing the planar p^{++}/n^{++} Si tunnel junction into the tandem solar cell, the fabrication process of the NWs solar cell was developed. The encapsulation of NWs by polymer was first studied to improve the mechanical stability of the NWs and to provide a planarization layer for contact deposition. HSQ and BCB have been tested and BCB was chosen due to its better performance in this work. Then the BCB encapsulation layer was etched by SF_6/O_2 in a RIE reactor to expose the tips for ITO contact deposition. An open-circuit voltage of 0.66 V was observed in the GaAs/$Al_{0.2}Ga_{0.8}As$ NWs/Si tandem solar cell. This value is higher than the 0.25

V in p-i-n GaAs NWs single-junction solar cell and 0.59 V in our fabricated standard Si solar cell. It proves that the III-V NWs top cell and Si bottom solar cell have been electrically connected by the p^{++}/n^{++} Si tunnel junction produced by PRTD.

Conclusion and perspectives

Conclusion

In this thesis, we presented the fabrication of high-quality and robust p^{++}/n^{++} Si tunnel junction on (111)-oriented c-Si substrate that can be used as the interconnection in 2T Si-based tandem solar cells. The implementation of the fabricated p^{++}/n^{++} Si tunnel junction in single-junction Si solar cells and III-V NWs/Si tandem solar cells was also reported.

First, the fabrication process of p^{++}/n^{++} Si tunnel junction was investigated. The n^{++} emitter was formed by thermal diffusion of phosphorus (using LYDOP system) while the p^{++} layer was obtained by boron spin on dopant followed by proximity rapid thermal Diffusion (PRTD). The initial doping profile of the n^{++} emitter profile was too high near the surface and then decrease abruptly away from the surface, making it difficult to form a tunnel junction. To solve this problem, a two-step RTA, consisting of RTA in N_2 flow and RTA in air flow, was carried out to adjust the n^{++} emitter profile. This approach reduced the doping concentration near the surface and made the doping profile relatively flat, making the n^{++} emitter more suitable to favor higher B atoms concentration at the surface. At the same time, other parameters during the tunnel junction fabrication process were also discussed, such as the cleaning process, RTA temperature and time for B diffusion. By studying different influencing factors, an optimized fabrication process of Si p^{++}/n^{++} tunnel junction was proposed. Si p^{++}/n^{++} tunnel junction with a depletion region of 3.78 nm-width was achieved following the optimized fabrication process.

After the realization of p^{++}/n^{++} tunnel junction, Si tunnel diodes were fabricated to characterize their electrical properties. A peak current density of 192 A/cm^2 was observed in the tunnel diode with planar p^{++}/n^{++} tunnel junction, which makes it a state-of-the-art result. It indicates that the fabricated tunnel junction can be applied not only in standard tandem solar cells but also in concentration solar cells. However, the specific series resistance of the tunnel diode at low bias is about 4-5 mΩ·cm^2, higher than expected (<0.3 mΩ·cm^2). It might be due to the high contact resistance between Al and p^{++}-Si. To optimize the electrical contact between Al and Si, the impact of the contact fabrication process and annealing process on the Al/Si contact resistance was investigated. TLM pattern was carried out to measure the contact resistance between them. The lowest specific contact resistance of Al/n^{++}-Si (2.16×10^{-7} Ω·cm^2) was obtained on the sample annealed at 400 °C for 40 s, consistent with the reported results.

While the lowest specific contact resistance of Al/p^{++}-Si (5.39×10^{-4} Ω·cm^2) was obtained on the sample without annealing. It means that our proposed annealing process for Al/p^{++}-Si contact was ineffective and it remains to be optimized. Nevertheless, the Al/p^{++}-Si contact will be bypassed when the tunnel junction is implemented as an interconnection in tandem solar cells.

As the ultimate objective of this thesis is to implement the Si tunnel junction in tandem solar cells, the influence of tunnel junction on Si bottom cells was studied. The fabrication of and characterization of single-junction Si solar cells with and without planar p^{++}/n^{++} Si tunnel junction on the surface were reported. Compared with the Si solar cell without tunnel junction whose efficiency is 13.09%, the efficiency of the single-junction Si solar cell with planar p^{++}/n^{++} Si tunnel junction on the surface decreased to 5.67%. This performance degradation is mainly caused by the high series contact resistance between front contact and p^{++}-Si. Moreover, recombination of minority carriers generated in tunnel junction and surface recombination between SiN_x and p^{++}-Si also degraded the performance of the solar cell. In order to reduce the surface recombination, a solar cell with localized tunnel junctions beneath the front contact was fabricated, achieving maximum efficiency of 10.43%. It suggests that the performance of tandem solar cells can be improved by replacing the planar tunnel junction with the localized tunnel junction in the bottom solar cell.

In the end, the effectiveness of our fabricated planar p^{++}/n^{++} Si tunnel junction in GaAs/$Al_{0.2}Ga_{0.8}As$ NWs/Si tandem solar cells (9×9 mm^2) was demonstrated. Before implementing the planar p^{++}/n^{++} Si tunnel junction into the tandem solar cell, the fabrication process of the NWs (core-shell junction) solar cell was developed. A p-i-n GaAs NWs single-junction solar cell was fabricated as the reference. The NWs were encapsulated by BCB (Benzocyclobutene) polymer through deposition, spin coating, and curing. Then the NWs were etched by RIE with SF_6/O_2 mixture to expose the tips of NWs for ITO contact deposition. 100 nm of ITO was deposited by sputtering as the front contact, followed by an anneal at 350 °C for 30 min under N_2 flow. This annealing process is appropriate for obtaining low sheet resistance of ITO and low ITO/$Al_{0.2}Ga_{0.8}As$ specific contact resistance without damaging the BCB encapsulation layer. An open-circuit voltage of 0.66 V was observed in the GaAs/$Al_{0.2}Ga_{0.8}As$ NWs/Si tandem solar cell. This value is higher than the 0.25 V of p-i-n GaAs NWs single-junction solar cell and 0.59 V of our fabricated standard Si solar cell. It proves that the III-V NWs top cell and Si bottom solar cell have been electrically connected by the p^{++}/n^{++}

Si tunnel junction produced by PRTD.

Perspectives

Based on the high-quality and robust p^{++}/n^{++} Si tunnel junction, it is promising to achieve high-efficiency III-V NWs/Si tandem solar cells in the future. To improve the performance of the tandem solar cell, it is important to increase the vertical yield of NWs as well as to optimize the contact between NWs and ITO. In addition, the planar p^{++}/n^{++} Si tunnel junction could be replaced by localized p^{++}/n^{++} Si tunnel junction beneath the NWs.

Furthermore, the clean and damage-free surface obtained by PRTD allows the Si tunnel junction to be combined with other top cell materials, such as perovskites or CIGS. The application of Si tunnel junction obtained by this economical and simple procedure may facilitate the development of competitive high-efficiency c-Si based tandem solar cells.

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Appendix

Reactive Ion Etching (RIE)

Reactive ion etching (RIE) is a plasma process where radicals and ions excited by radio frequency (RF) electric field etch the substrate in a low-pressure chamber [1]. In this work, Nextral NE 110 reactive ion etcher using capacitively coupled plasma is applied to etch Si and BCB (Figure 1 (a)). The schematic of the principal part of RIE is shown in Figure 1 (b). There are two parallel metal plates in a cylindrical vacuum reaction chamber. During the etching process, the RF voltage is applied across these two parallel metal plates, generating an oscillating electromagnetic field between them. The industrial standard frequency of the RF voltage is 13.56 Megahertz. This electromagnetic oscillating field ionizes the gas molecules by knocking electrons free from atoms. The electrons are accelerated by the electromagnetic field and cause an ionization avalanche, creating a plasma to etch the substrate.

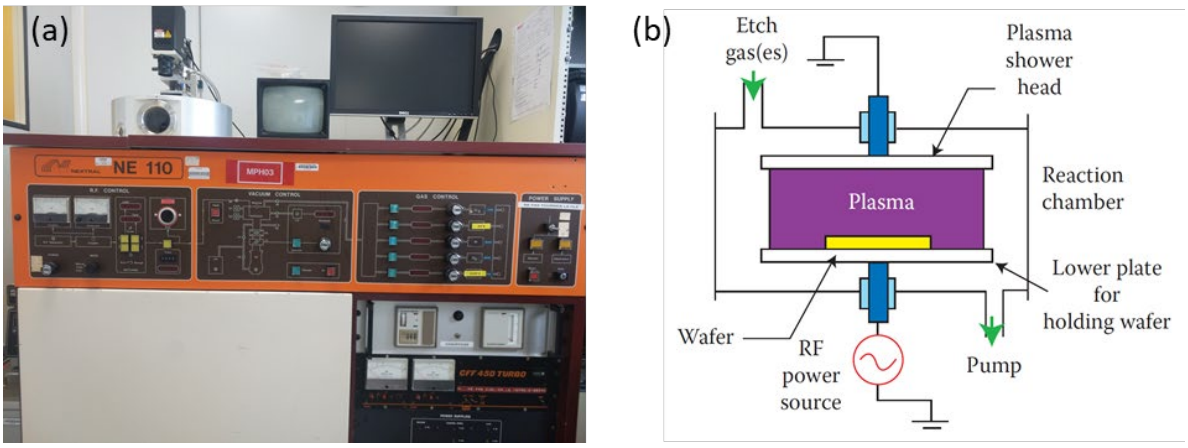

Figure1 *(a) Nextral NE 110 reactive ion etcher; (b) Schematic of the principal part of an RIE [2].*

RIE is a dry etching process that combines chemical etching reactions and physical ion bombardment. The etching rate of RIE is faster than either spontaneous chemical etching or pure physical ion bombardment. Because ion bombardment is directional, RIE has an anisotropic character with a reduced lateral etching rate. By adjusting etching parameters, such as chamber pressure, gas flow, and RF power, the etching characteristics can be precisely controlled in RIE.

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List of publications

Publication

Li, X., Fave, A., & Lemiti, M. (2021). Si tunnel junctions obtained by proximity rapid thermal diffusion for tandem photovoltaic cells. *Semiconductor Science and Technology*. https://doi.org/10.1088/1361-6641/ac2aef

Communications

1. Li, X., Lemiti, M., & Fave, A. (26-29 January 2021). c-Si tunnel junctions obtained by proximity rapid thermal diffusion for tandem photovoltaic cells. *Journées Nationales du PhotoVoltaïques 2020*, Online conference, Oral presentation.
2. Li, X., Fave, A., & Lemiti, M. (9-12 September 2019). Fabrication procedure of c-Si tunnel junction for tandem photovoltaic cells European *Photovoltaic Solar Energy Conference and Exhibition*, Marseille, France, Poster.
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FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : LI
(avec précision du nom de jeune fille, le cas échéant)

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Prénoms : Xiao

TITRE : High-efficiency Si solar cell including tunnel junction for tandem photovoltaic cells

NATURE : Doctorat

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RESUME : La cellule photovoltaïque tandem à base de silicium cristallin (c-Si) avec 2 terminaux (2T) est une solution permettant de dépasser la limite de Shockley-Queisser. L'objectif de ce travail de thèse est de réaliser une jonction tunnel en c-Si présentant une résistance faible afin de l'intégrer comme interconnexion des 2 sous-cellules constitutives de la tandem. La technique de diffusion thermique rapide par proximité est appliquée pour fabriquer les jonctions tunnel en silicium en minimisant les dommages causés à la surface du SIlicium. La fabrication et la caractérisation de la jonction tunnel p^{++}/n^{++} sur un substrat de silicium orienté (111) sont présentées. Plusieurs paramètres du processus de fabrication de la jonction tunnel sont étudiés. L'ajustement de l'émetteur n^{++} par un recuit thermique rapide en deux étapes a effectivement facilité la réalisation de la jonction tunnel p^{++}/n^{++}. Des diodes tunnel en silicium ont été fabriquées pour caractériser les propriétés électriques des jonctions tunnel. Le pic de densité de courant des diodes tunnel se situe entre les valeurs 140 et 192 A/cm^2 avec un ratio de courant de pic à vallée de 1,9 à 3,2. Par la suite, cette jonction tunnel p^{++}/n^{++} a été intégrée dans des cellules photovoltaïques tandem nanofils III-V/Si. Malgré la défectuosité des réseaux de nanofils, une augmentation de la tension de circuit ouvert a été observée dans les cellules photovoltaques tandem par comparaison avec celle de la cellule solaire à simple jonction. Ce type de jonction tunnel peut également être intégré à d'autres types de cellules en dessus, par exemple les pérovskites ou le CIGS. L'application de jonctions tunnel en Si obtenues par la technique de diffusion thermique rapide à proximité pourrait faciliter le développement de cellules photovoltaïques tandem compétitives à haut rendement à base de c-Si.

MOTS-CLÉS : jonction tunnel en silicium, diffusion thermique rapide par proximité, cellule photovoltaïque tandem

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