Contribution to the design and control of the extended overlap-alternate arm converter

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Contribution to the Design and Control of the Extended Overlap-Alternate Arm Converter

Contribution au Dimensionnement et à la Commande de Convertisseur Extended Overlap Alternate Arm Converter (EO-AAC)

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Contexte de la thèse

L'utilisation massive des ressources d'énergie fossiles telles que le charbon, le pétrole ou le gaz naturel a grandement participer au réchauffement climatique dû à l'émissions de dioxyde de carbone (CO_2). Dans l'objectif de ralentir l'augmentation de la température à la surface de la planète, une des actions possible consiste à repenser la manière dont l'électricité est produite. La production d'électricité était principalement basée sur l'utilisation de centrale à charbon, au gaz ou encore nucléaire. Afin d'améliorer l'impact carbone de la production d'électricité, il conviendrait de remplacer ces centrales à charbon ou au gaz par des sources d'énergie dites "renouvelables" telles que l'éolien et le solaire. Néanmoins, effectuer ce remplacement tout maintenant le niveau de résilience du réseau de transport actuel représente un réel défi.

En Europe, le potentiel de l'éolien offshore est très élevé, par exemple en mer du nord qui est en parti exploité par l'Allemagne, mais très souvent fortement éloigné des principaux points de consommation. Un rapatriement de cette énergie lointaine vers les consommateurs est donc nécessaire. Étendre le réseau de transport actuel en se basant sur des liaisons aérienne ou souterraine à courant alternatif (AC) est souvent in-envisageable pour deux raisons principales. La première concerne l'acceptation des personnes pour de nouvelles lignes aérienne principalement dû a une certaine méfiance vis-à-vis des ondes électromagnétiques générées par les conducteurs. La deuxième, technique, concerne la distance limite de transmission de l'énergie en alternatif au travers de câble sous-marins ou enterrés. Le couplage capacitif entre conducteurs enterrés augmente avec la longueur de la liaison et donc la consommation de puissance réactive de la liaison. Ainsi, la transport de l'énergie au travers de liaison sous-marine/souterraine à courant continu (DC) apparait comme une nécessité afin de permettre une intégration plus massive des sources renouvelables.

Contrairement à la transmission d'énergie par courant alternatif, dépendante de machines tournantes (ex: machine synchrone) et de transformateurs, l'utilisation de la technologie à courant continu nécessite une conversion statique de l'énergie au travers de convertisseurs d'électronique de puissance dédiés aux applications Haute Tension et Courant Continu (HVDC). Historiquement, le transport d'énergie au travers de liaison HVDC était réalisé au travers de convertisseurs à base de thyristors nommés LCC (Convertisseur Commuté par la Ligne), mais l'émergence des transistors de puissance IGBT (Transistor Bipolaire à Grille Isolée) dans les années 90 a permis d'envisager d'autres topologies telles que les convertisseurs à modulation de tension nommés VSC (Voltage Source Converter). Parmi les convertisseurs à modulation de tension, seules trois topologies ont étés implantées sur le réseau de transport. On retrouve notamment des structures classiques telles que les modulateurs 2-Niveaux et 3-Niveaux de type A-NPC (Active-Neutral Point Clamped), mais également des technologies de convertisseurs plus récente qualifiées de structures modulaires, notamment le Convertisseur Modulaire Multiniveaux (MMC). Les topologies traditionnelles de VSC nécessite une fréquence de modulation élevées afin de maintenir un taux de distorsion harmonique convenable dans les courant in-

jectés sur le réseau alternatif, cependant, il en résulte que les pertes d'énergie engendrées par la commutation des interrupteurs de puissance sont élevées (de l'ordre de 1 à 2%). De plus, la nécessité de monté en tension pour le réseau de transport HVDC impose une connexion en série de transistors impliquant une problématique de synchronisation des commutations et d'équilibrage des tensions aux bornes des interrupteurs. La classe des convertisseurs modulaires est basée sur l'utilisation de piles de Sous-Modules (SMs) permettant ainsi une approche multi-niveaux dans la modulation de tension. Cela permet de faciliter la monté en tension du convertisseur (et donc en puissance), de diminuer la fréquence de modulation pour un faible niveau d'harmonique rejetées et de fonctionner à rendement très élevée (∼99%).

Les convertisseurs hybrides-modulaires

Depuis l'apparition du MMC et son utilisation comme convertisseur AC/DC pour les réseaux HVDC, l'intérêt pour les structures modulaires pour les applications haute tension/haute puissance n'a cessé de croitre. Cet intérêt à donné naissance à une nouvelle classe de convertisseurs d'électronique de puissance que l'on peut nommer: les convertisseurs hybrides modulaires.

Malgré certains avantages indéniables, le MMC, comme tout convertisseurs, a certains inconvénients tels que son incapacité a bloquer le courant de défaut lors d'un court-circuit côté DC (possible dans certains cas mais impact négatif sur le rendement) ou encore sont besoin stockage d'énergie interne élevé pour garantir un fonctionnement linéaire de la modulation de tension. La classe des convertisseurs hybrides-modulaires ambitionne de contourner certains inconvénients du MMC tout en gardant ces principaux avantages. L'un de ces convertisseurs pouvant potentiellement challenger le MMC, est le Convertisseur à Bras Alternés (AAC) dans un mode de fonctionnement dit à Empiètement Étendu (EO-AAC) qui représente le sujet de ces travaux de thèse.

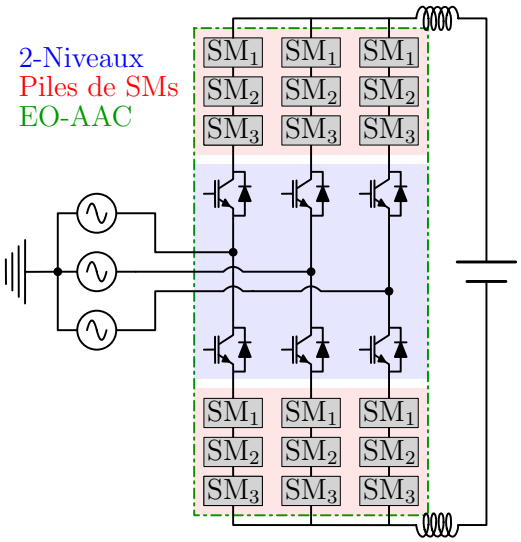


Figure 1 – Convertisseur à Bras Alternés - Mode de fonction à Empiètement Etendu (EO-AAC)

Comme le montre la Figure 1, le convertisseur EO-AAC est composé d'une structure 2-Niveaux haute tension (mise en avant dans le cadre bleu), qui implique la mise en série de transistors de puissance, et d'un pile de SMs dans chaque demi-bras (misent en avant dans le cadre rouge). Cet association de ces deux éléments (provenant des topologies 2-Niveaux et MMC) implique donc que la structure résultante, EO-AAC, est une structure hybride.

Les travaux existants sur cette structure montre qu'il est possible d'obtenir la capacité de blocage du courant de défaut lors de court-circuit côté DC avant un impact réduit sur le rendement du convertisseur ainsi qu'une empreinte au sol réduite comparé à un MMC de capacité en puissance équivalente.

Néanmoins, l'aspect de hybride de cette structure impose des contraintes en fonctionnement et sur la commande du convertisseur restant partiellement exploré. De plus, le fonctionnement et le comportement de ce convertisseur connecté au réseaux HVDC demeure très faiblement étudié malgré l'importance de ce sujet. Ainsi, l'objectif principale de ces travaux est de répondre à la question suivante : Le EO-AAC, peut-il réellement challenger le MMC pour les applications réseaux HVDC ? Pour y répondre, une étude rigoureuse comportant de l'analyse statique, dynamique et réseau a été menée.

Plan de la thèse

Le plan de la thèse s'articule autour de quatre chapitres.

- **Chapitre 1:** Une introduction à la modulation de tension pour les système de conversion AC/DC est donnée dans un premier temps pour ensuite présenter la structure EO-AAC. Ce chapitre revient notamment sur, comment générer un flux de puissance active au travers d'un convertisseur qu'il soit 2-Niveaux commandé en pleine-onde ou en Modulation à Largeur d'Impulsion (MLI) mais également multi-niveaux tel que le MMC. Ces caractéristiques fondamentales sont ensuite réutilisées afin d'introduire de manière systématique la structure EO-AAC. Grâce à cette introduction, la plupart des degrés de liberté exploitable par la commande sont mis en avant.

- **Chapitre 2:** Une étude de dimensionnement en régime permanent est réalisée dans ce chapitre. Celui-ci s'articule autour d'un modèle statique du convertisseur intégrant les degrés de liberté de la commande afin de les exploités pour obtenir un dimensionnement du convertisseur le plus avantageux possible. Ainsi, sur la base de ce modèle statique, on s'intéresse au nombre d'éléments actifs dans le convertisseurs, à l'estimation de stockage d'énergie interne requit pour fonctionner ainsi qu'à l'estimation des pertes dans la structure. La méthodologie appliqué dans ces travaux et les outils développés ayant pour but d'être générique et exploitable pour d'autres topologies modulaires.

- **Chapitre 3:** Dans ce chapitre, la commande du convertisseurs est développée, depuis la commande dite de "bas niveaux" (proche du composant) jusqu'à la couche supérieur dite "haut niveaux" (boucle de régulation). Cette étude met l'accent sur la partie haut niveaux du contrôle, et notamment le contrôle de l'énergie stockée dans le convertisseurs. L'une des principales difficultés du EO-AAC quant à sa commande vient de l'aspect "discontinu" dans la régulation de l'énergie stockée dans chaque pile de SMs. Ainsi dans cette thèse, on introduit les notions de contrôle total et d'équilibrage horizontale et verticale dans la commande du EO-AAC permettant une distribution égale de l'énergie entre chaque pile de SMs en transitoire et en régime permanent. Finalement, il est démontré que grâce à la continuité du contrôle total il est possible d'obtenir un modèle d'ordre réduit et continu du EO-AAC en négligeant l'impact des boucles d'équilibrage horizontale et verticale. Ce modèle réduit permet, pour la première fois, d'envisager le EO-AAC dans étude de stabilité du réseau en petits signaux.

- **Chapitre 4:** L'intégration du convertisseur dans un environnement réseaux est détaillé dans ce chapitre. Il comporte deux principales point de discussions: la connexion au

réseau HVDC et les régimes de fonctionnement anormaux (exemple déséquilibre AC). La connexion au réseau HVDC est traité dans le cas d'une liaison point à point et étendue a un réseau multi-terminaux (MTDC). Grâce au développement du modèle réduit, il est montré que, comme le MMC, le EO-AAC peut participer au réglage de la tension DC en partageant sont énergie stockée avec le réseau HVDC. Cette participation à la stabilisation du bus DC est, aux valeurs de dimensionnement prés, strictement la même que le MMC malgré un fonctionnement interne des convertisseurs très différent. Cependant, cette différence de fonctionnement est mise en avant lorsque les conditions de fonctionnement ne sont plus idéales telles que lors d'un déséquilibre en tension sur le réseau. Dans ces conditions, la structure atteint ses limites mais également la commande bâti dans le Chapitre 3. Cela suppose donc de repenser une commande du EO-AAC ayant pour contraint le fonctionnement du convertisseur dans le cas du réseau alternatif déséquilibré.

Conclusions de la thèse

Les convertisseurs électroniques de puissance et les systèmes à courant continu sont les clés pour améliorer l'intégration des sources renouvelables à distance ainsi que le renforcement de certaines régions. Le convertisseur modulaire multi-niveaux s'est avéré être la topologie la plus appropriée pour atteindre ces objectifs. Cependant, les topologies émergentes combinant d'une part l'aspect modulaire du MMC et les fonctionnalités des convertisseurs AC/DC les plus simples comme l'Eo-AAC peuvent remettre en cause le MMC.

Cette thèse vise à étudier le fonctionnement, la conception et la commande des EO-AAC. Dans ce qui suit, les principales conclusions du chapitre sont résumées :

1. Une approche méthodologique expliquant l'origine de la topologie AAC et le principe de fonctionnement principal de l'EO-AAC ont été détaillés dans le Chapitre 1. L'idée principale derrière la topologie AAC est de faire fonctionner simultanément deux types de modulation: la commande pleine onde et la modulation de tension. Cependant, chaque méthode a ses propres spécificités. La modulation pleine onde nécessite que le convertisseur fonctionne comme une source de tension en fixant l'amplitude des tensions alternatives mais l'angle est un degré de liberté. Le contrôle de la tension modulée permet de fournir l'amplitude de la tension et son angle en degrés de liberté. Lorsqu'ils sont combinés, un convertisseur avec deux fois moins de SM qu'un MMC est obtenu. Néanmoins, son fonctionnement est limité à un certain indice de modulation fixé par la modulation pleine onde et le courant continu est toujours une quantité modulée fortement ondulée à six fois la fréquence de réseau. Le mode empiété est introduit pour permettre la mise en œuvre d'un schéma de contrôle d'énergie assurant l'équilibre de puissance dans le convertisseur et récemment étendu jusqu'à ce qu'une stratégie dédiée de filtrage actif du courant continu puisse être mise en œuvre. C'est dernière modification a donné lieu au EO-AAC.

2. L'EO-AAC a besoin de plus de SM par pile pour obtenir le filtrage actif du courant continu. Alors, la technique d'injection de tension homopolaire (ZSVI) a été réalisée pour diminuer le nombre de SM dans le convertisseur. Ainsi, le chapitre 2 a suivi l'impact du ZSVI sur le dimensionnement des composants de puissance, la capacité des SM et l'estimation des pertes. Ainsi, cette étude révèle que pour obtenir un blocage du défaut DC à haute tension alternative, il faut environ 25% moins de SM que le MMC. Le besoin en énergie est de l'ordre de 10-15 kJ/MVA. On estime que les pertes sont similaires à celles du HB-MMC fonctionnant à un faible indice de modulation (c'est-à-dire inférieur

à 1). Cependant, avec une petite amélioration, le HB-MMC restera plus efficace que l'EO-AAC.

3. Dans le chapitre 3, une évaluation globale des contrôleurs a été détaillée. Du contrôleur de bas niveau, une exigence a été clairement mise en évidence. La nécessité d'une compensation appropriée de l'ondulation de tension du condensateur SM est très importante pour maintenir un filtrage actif efficace du courant continu. Dans une deuxième partie du chapitre, le contrôle haut niveau a été détaillé: le contrôle des courants alternatifs, du courant continu et de l'énergie stockée dans les piles de SMs. Une combinaison a été proposée réalisant un contrôle continu de l'énergie totale. Deux autres commandes, purement séquentielles, sont réalisées à des fins d'équilibrage horizontal et vertical. Ces comportements séquentiels impliquent une injection transitoire d'harmoniques sur le courant alternatif ou continu. Cependant, grâce à une dynamique continue, il est prouvé que l'EO-AAC exécute une dynamique similaire à celle du MMC, comme le soutient le modèle d'ordre réduit développé. Ainsi, la principale conclusion de ce chapitre est l'équivalence des deux convertisseurs du point de vue du réseau.

4. Pour étudier la dynamique du convertisseur lorsqu'il est connecté au réseau, le chapitre 4 fournit plusieurs cas de test basés sur le logiciel EMTP-RV. Ainsi, il est d'abord présenté un moyen d'obtenir un support de tension continue grâce à l'énergie interne du convertisseur initialement conçu pour le MMC. Cela a été possible grâce au contrôle continu de l'énergie totale basée sur la puissance continue. Ainsi, en rassemblant tous les contrôleurs conçus jusqu'à présent et les techniques de contrôle de la tension continue, des liaisons HVDC point à point ainsi que MTDC ont été simulées, montrant l'efficacité de l'EO-AAC. De plus, des tests d'interopérabilité de MMC ont été effectués, montrant les bonnes performances de l'ensemble du système, même en cas de MMC avec contrôle CCSC. Enfin, quelques ouvertures concernant la gestion de l'énergie en cas de défaut DC, système AC déséquilibré ont été présentées.

Aux travers des travaux menés au cours de cette thèse, il nous est possible de donner un avis général sur la topologie EO-AAC. Du point de vue de la conception et de l'encombrement, cette topologie est extrêmement intéressante car elle permet un fonctionnement similaire au MMC avec un nombre réduit de composants et de bras conducteurs. Cependant, ce dernier point est aussi ce qui semble être la principale limite de cette topologie comme souligné dans le Chapitre 4. Par exemple, dans le cas du contrôle de l'énergie par la puissance DC, plusieurs opérations sont assurées par un seul bras du convertisseur. (filtrage actif, contrôles total, horizontal et vertical). Ainsi, chaque fois qu'un déséquilibre potentiel se produit, ce manque de contrôlabilité et cette sensibilité élevée à l'indice de modulation peuvent être un problème.

Malgré une conclusion mitigée sur la topologie EO-AAC, il est à noter que l'étude de topologies aussi complexes (l'EO-AAC en est une parmi d'autres) nous a permis de prendre du recul sur la façon de contrôler certaines structures classiques comme le MMC. , STATCOM modulaire basé sur la méthodologie développée dans cette thèse.

Introduction to HVDC Systems

1 Context and motivations

The massive use of fossil energy sources, oil, coal and natural gas has largely participated to the global warming due to carbon dioxide emissions [2, 3]. To slow down the increasing of the global temperature, one of the possible action is to rethink the way that electricity is produced. So far, electricity power plants were mainly based on coal, natural gas, nuclear reactors. Replacing the fossil fuels based power plants by renewable sources like solar or wind farms while maintaining the same level of resilience for the power system is a huge challenge.

In Europe, large amounts of renewable energy are available on remote locations, often offshore or near the sea [4, 5]. Expanding the current AC transmission system to bring these energy to the comsuption point is often not possible for two main reasons. Firstly, the acceptance of people for new lines is becoming more and more difficult to obtain. Then, the transmission of a large amount of power for a long distance are restricted for HVAC cables [6]. For these reasons, but also economical [7], High Voltage Direct Current transmission schemes (HVDC) are now becoming more and more relevant [8] to enhance the massive integration of renewable sources.

Unlike AC transmission system that relies on rotating electric fields through machine and transformer windings, the HVDC system is based on a static conversion of the energy for which dedicated power-electronics devices have developped. Up to 30 years ago, the most suitable technology in HVDC was the thyristor-based Line Commutated Converter (LCC) technology, but the Voltage Source Converter (VSC) technology is now well established in HVDC. There are different topologies of VSC, but only three of them have been adopted for real project: *2-level*, *3-level* Active-Neutral Point Clamped [9] (A-NPC) and *Modular* topologies [10–12]. Traditional topologies of VSC have a high switching frequency (1–2 kHz) for obtaining a low harmonic distortion, leading to higher switching losses as well as high voltage stresses. In high power applications, the conversion losses result in high cost for the grid operators [13]. For this reason, a new *Modular* VSC technology taking advantages of the principle of cascaded cells called Modular Multilevel Converters (MMC) introduced in [14]. The main advantage for this new class of converter is the possibility of working with lower switching frequencies (only several times the fundamental frequency), while simultaneously achieving better harmonic performance compared to traditional VSCs [15–17].

HVDC projects based on VSC-HVDC technologies highly increased these last twenty years. Thanks to Pr. Mike Barnes from the University of Manchester providing the monthly "VSC-HVDC NEWSLETTER", the information about the number of VSC-HVDC projects in operation, or not, is easily obtained for the community. Thus, as reported in this newsletter (dated to June 2021) some 47 projects are commissioned around the world while 55 are being commissioned within the 10-15 years.

2 Main Principles for the HVDC Systems

2.1 Point-to-point schemes

The most common configuration for HVDC projects is the so-called "point-to-point" scheme, which is depicted in Figure 2. In this configuration, there are two AC-DC converters intefaced through a DC conductor which may be a cable or an Over-Head Line (OHL). One of each converter inFigure 2 has a specific function. One converter is in charge of the power flow in the DC link, while the other fixes the DC voltage to a certain level as it will detailed in Chapter 4. The advantage of this configuration with respect to the classical AC lines is the ability to control the power flow in the system [18].

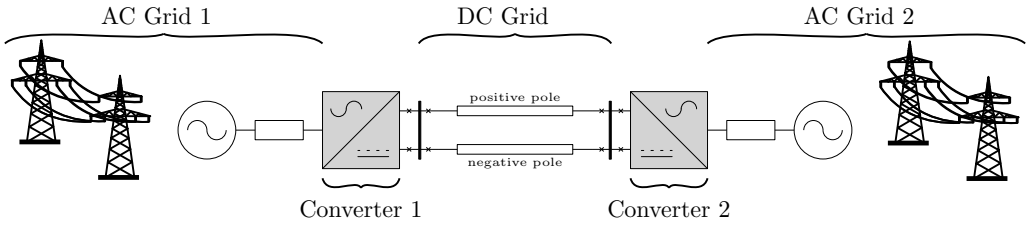


Figure 2 – Example of HVDC point-to-point scheme

Figure 2 depicts a symmetric monopole scheme which providing positive and negative poles and grounded middle point. Different types of scheme exist [19]: the asymmetric monopole using either earth or metallic grounded as a return, and the symmetric bipolar scheme requiring "twelve pulse" bridges (in both LCC or VSC technology) but more resilient in case of fault on one pole since the other one can be used to still convert energy.

Even if the list of HVDC link in the world is very extensive nowadays, the modern history of VSC-based HVDC link is remarked by three main disruptive events:

1. **2009**: ABB commissioned the first offshore HVDC system *BorWin1* which was the first one to use VSC for the converter stations [20, 21].
2. **2011**: The first HVDC system using Modular Multilevel Converters; *Trans Bay Cable* commissioned by Siemens [22, 23].
3. **2015**: First HVDC link with MMCs for transmitting power in the GW range called *Inelfe*, which was commissioned by Siemens [24].

2.2 Multi-Terminal DC schemes

When more than two converter stations are connected to the same DC grid, the configuration is referred as a "Multi-Terminal DC" system (MTDC). As illustrated on Figure 3, a MTDC system can be radial (mostly in case of three terminals or long distance between converter stations) or meshed like the current AC transmission system.

These schemes, regardless of the system topology are expected to provide additional features compared to point-to-point HVDC links, such as:

- More flexibility in power dispatch [8]
- Optimized assets for offshore wind farm connection to shore and power transmission capability [25]
- Frequency support to onshore grids [26, 27]

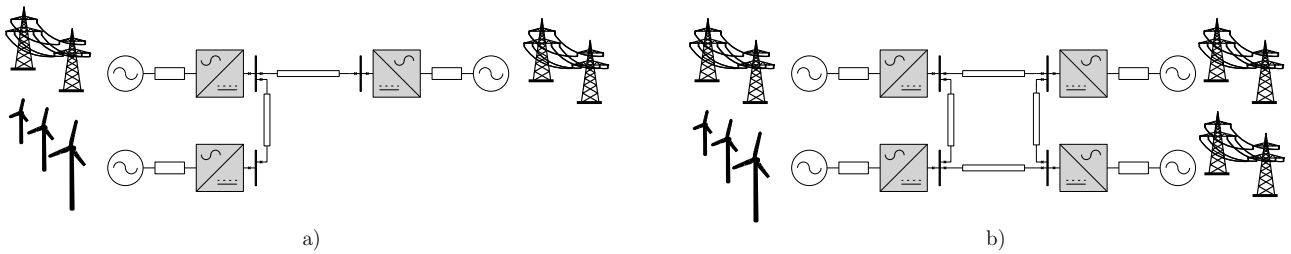


Figure 3 – MTDC System: a) radial b) meshed

- More reliability (can operate or at least partially operate even if one element is out of service) [28]

To control the power flows in a DC system, meshed or radial, two layers of controllers are likely to be used [29]. The first control layer is managed by TSOs to dispatch suitable converter set-points in order to achieve a precise power flow control [30]. Also, in case of a contingency, it would automatically adapt set-points to find a new stable operating point [31]. Second, there are local controlers inside the HVDC stations such as DC voltage droop control used to the adjustments of set-points in real-time [32].

MTDC real projects

As for HVDC link, MTDC systems develoment has reached some milestones with the following project.

Even if the list of HVDC projects in the world is very extensive nowadays, the modern history of VSC-based HVDC systems is remarked by four main disruptive events:

1. **2013**: First three-terminal "multivendor" MTDC grid with MMCs commissioned by the State Grid Corporation of China (SGCC) [33].
2. **2020**: First four terminal MTDC system including MMC with ±500 kV DC comissioned as the Zhangbei project by SGCC. [34, 35].
3. **2020**: First Hybrid-MTDC system including LCC and MMC with ±800 kV DC known as Wudongde HVDC project. It has been put in operation by China Southern Power Grid (CSG). [36].

Most of them are situated in China. The firsts were the well known Nan'ao and Zhoushan projects [37, 38] in 2013 and 2014 respectively.

The latest MTDC systems have been commissioned with outstanding voltage and power ratings. The Zhangbei project [34,35] which connects four regions including the city of Beijing. The nominal DC grid voltage is ±500 kV, stations ratings are 3000 MW and 1500 MW. The project also includes the use of DC breakers, which is a key point in the development of future DC systems. The second project, called Wudongde-UHVDC also highlights another important situation that may occur more often in the future: the interoperation between different kind of stations, also called hybrid MTDC systems. This project is very particular in respect of others since a 8000 MW LCC station is connected to two VSC stations (i.e. 5000 MW and 3000 MW). So far, the goal of 8000 MW is not reached.

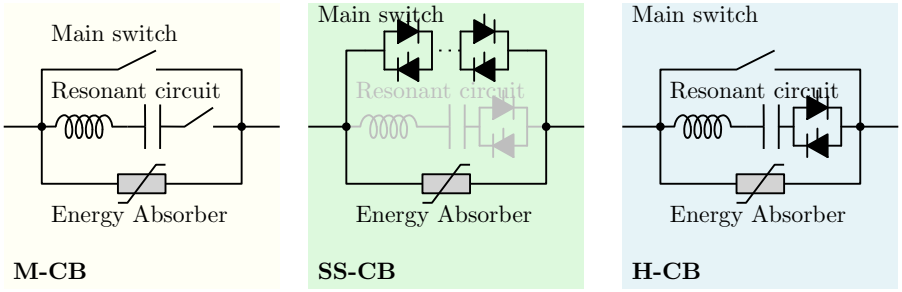
Thus, these last two projects have presented the main concerns for future HVDC systems investigated these past years:

- the DC fault blocking capability through DC Circuit Breaker (DCCB) [39, 40], or not
- the interconnections between different topologies (even different modulators i.e. current and voltage source)

DC circuit breaker

One of the key element to enable the expansion of MTDC schemes around the world is the protection in case of DC-Fault. Unlike the AC system which is highly inductive, a DC system has no natural current rising limitation like transformers, generators etc... In case of a DC-fault, the current rising is very high, requiring a very fast current interruption is mandatory [39]. Moreover, there is no zero crossing on DC side. To tackle this issue, specific DC Circuit Breakers (DCCB) have been developed as in the European project PROMOTioN [41].

DCCBs are organised around three main categories. First, the Mechanical-CB which is leave a part in favour of newer topologies like the Solid State-CB (SS-CB) based on power-electronics devices like Gate Commutated Thyristors (GCTs) [40] or more recently, Hybrid-CB (H-CB). This last structure of CB features an ultra-fast mechanical switch and a solid-state part. The solid-state part participates to the current extinguish allowing to open the mechanical switch. These DCCBs are conceptualised below:



a) b) c)

Figure 4 – Simplified illustration of DCCBs topologies: a) M-CB b) SS-CB c) H-CB

In each topology of DCCBs are found three characteristcs elements: the main switch (mechanical or semi-conductor) an auxiliary switch that can activate a resonant circuit (some SS-CB are not containing a resonnant circuit [39]) and an energy absorber [42–44]. Depending on the topology, the opening of the main switch and the fault isolation can be achieved in a few ms. For instance, the Zhangbei project tests report a fault isolation in less than 3 ms.

3 Power Electronics for HVDC system

As mentioned in a previous section, currently, three types of AC/DC stations may be found in operation on the grid: LCC, 2-level and 3-level topologies and the MMC.

3.1 Line Commutated Converter

In the history of HVDC system, LCCs were the first conversion station to be used (with mercury-arc valves then replaced by thyristors). The LCC is a current-source converter; that means a modulation of the DC current to generate the AC ones. As a result, the DC voltage is modulated using the line-to-line voltages. This is depicted on Figure 5 where the modulated variables are labelled in red. The main principle of the LCC it to switch ON valves according to the firing angle reference α in order to vary the average value of the DC voltage v_m. Hence, the power reversal is achieved by DC voltage polarity reversal. The OFF switching is not controllable in basic thyristors.

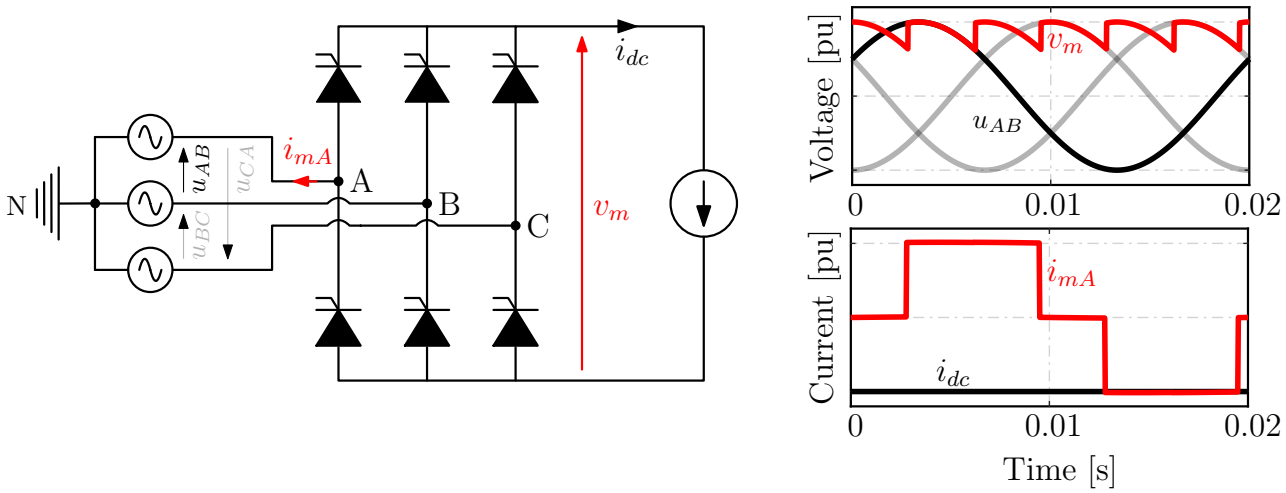


Figure 5 – Simplified illustration of a six-pulses LCC - Modulated quantities waveforms for $\alpha = 20$ degrees

Using LCC topologies as interface between AC and DC system present some advantages. Thyristors are very efficient regarding ON-state voltage drops [45–47] and can withstand high ratings in terms of continuous current and voltage blocking capability [48]. Therefore, HVDC stations using LCCs are likely to be generate a very level of losses. Hence, their power capability is huge, especially in case of bipolar link where twelve pulses bridges are used.

Despite these important features, LCCs also suffer from shortcomings. As the converter is not fully controllable active and reactive components in the AC side are coupled. Thus, the load angle of the AC currents is strongly linked to the value of α [49]. In addition to this inherent reactive power generation, low order harmonics in modulated quantities are observed. Thus, on the AC side is needed a compensation of the reactive power and a passive filter. A second passive filter is needed on the DC side. It is also reported that the OFF switching may fail in some conditions often caused by AC voltage drops with high DC current or when connected to a weak grid. It results in a short-circuit of the DC side.

3.2 Voltage-source topologies

This section presents some basics about the 2-level and the MMC topologies as more detailed will be provided in Chapter 1. The 3-level A-NPC structure is not fundamentally different from the 2-level, so focusing on the this latter is sufficient. As in the LCC, the origin of the VSC comes from the kind of modulation that is performed. Most of the time, the modulation of a DC voltage is used, thus, 2-level converter and MMC are a part of the VSC class.

A 2-level VSC, depicted on Figure 6 a), is based on Insulated Gate Bipolar Transistors (IGBT) which are controllable at turn ON and OFF. As a result, the controllability can be improved compared to the LCC, as well as the harmonic distortion of currents if the modulation frequency is sufficiently high. On the other hand, IGBTs presents higher ON-state voltage drops and smaller ratings than thyristors increasing conduction loss. Moreover, the hard switching of transistors introduces high switching losses depending on the modulation frequency. In HVDC application, the switch assembly is made by several IGBTs connected in series as LCC valves [50], [51]. The switching needs for a perfect synchronism at the opening and closing to preserve the integrity of all switches. It becomes particularly challenging at high voltage and high frequency. Some solutions are reported in [52–56] which aims to use active or passive

approaches to synchronise gate signals and balance voltage across IGBTs.

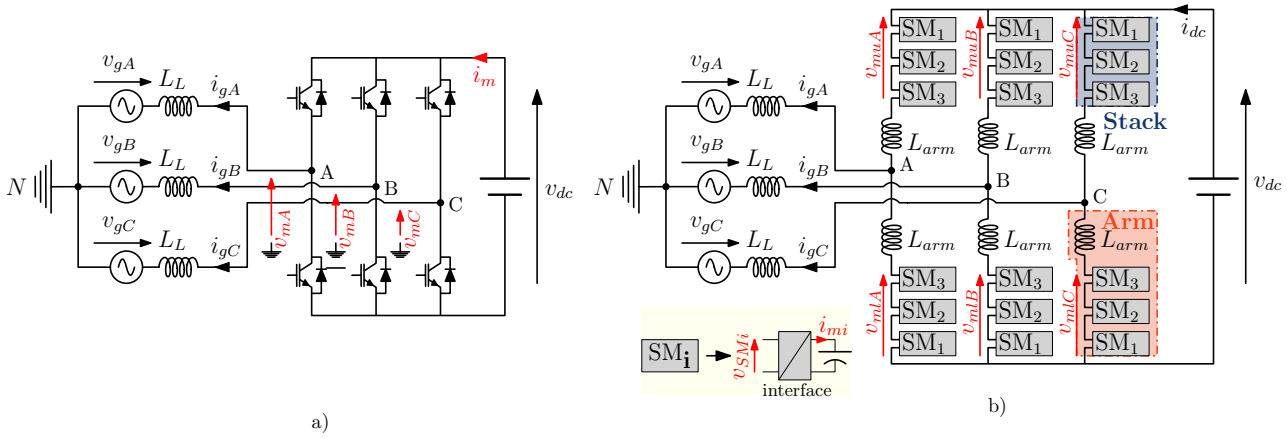


Figure 6 – Simplified illustration of a) 2-level VSC and b) MMC including 3 SMs per stack

The MMC is fundamentally different from the 2 or 3-level topologies. This difference lies in the modulated quantities. Compare Figure 6 a) and b). A 2-level topology, modulates one of the AC and DC side quantity at the same time. With MMC, none of the grid side quantities are modulated. The modulation stage is internal and freed from the nature of the sources that are connected to the MMC terminals. This property comes from the elements constituting the arms. A MMC is composed of stack of SMs as presented on Figure 6 a). A SM, is composed of a floating capacitor interfaced through a small converter like the Half-Bridge (HB), the Full-Bridge (FB) or many others... By controlling this interface, the SM capacitor can be inserted or by-passed so that a multilevel modulated voltage waveform can be synthesized. In HVDC, several hundreds of SM are involved almost removing the needs for passive filtering.

The use of stacks of SMs also provide a significant advantages over classical topologies since it is no necessary to switch all the SMs at the same time and at high frequency. The insertion or the bypass of a SM is a punctual action, which, in average occurs a few times per fundamental period (i.e. the modulation frequency is less than 100-300 Hz) [57]. Thus, the overall switching losses decreased leading to a VSC-HVDC station with a very high efficiency challenging the LCCs for power ratings in the range of 1000-1500 MW (even 3000 MW according to newest projects).

Finally, one question may raise nowadays. More and more projects are based on MMC which has proven to be a powerful converter for many important points: modular hardware, energy efficiency, controllability, dynamics, system services etc... this is undeniable. So, can the MMC be challenged in the range where it is the best ? Some solutions are worth being studied.

3.3 Modular hybrid topologies

First of all, let us provide a possible definition of Modular hybrid topologies which is important for the following of the section and Chapter 1.

Def: *A modular hybrid topology uses the principle of stack of SMs. These stacks of SMs are combined to different topologies which are not limited to VSC. This combination of two modulators form an hybrid modulation scheme that must guarantee a proper functioning of the*

resulting topology.

Over the years, many proposals for hybrid topologies suitable for HVDC (and even MVDC) have been published where the main of them and some others can be found in [58–72]. Until now, none of these solutions are proposed for commercial solution. A simplified illustration for some of them (the most "basic") is proposed in the following.

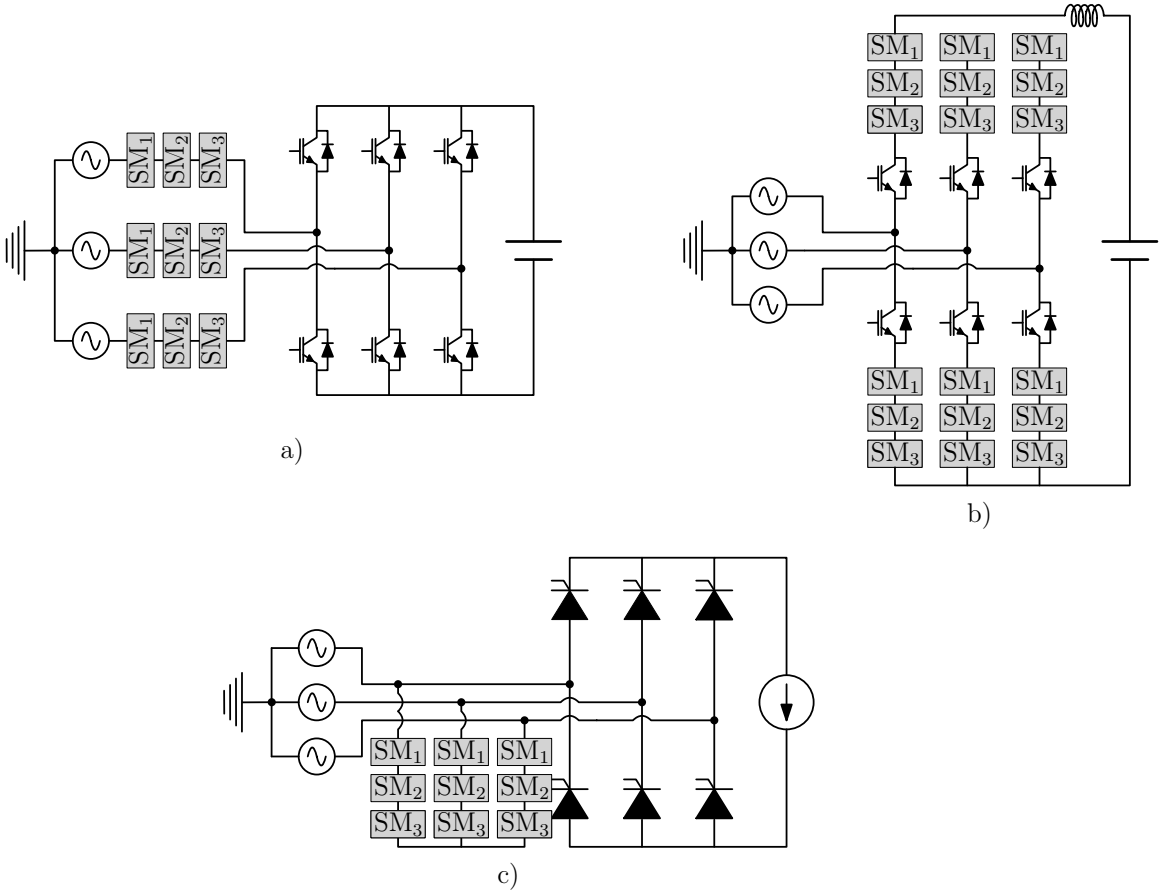


Figure 7 – Simplified illustration of a) Hybrid VSC with AC side stacks b) Hybrid VSC with DC side stacks and c) Hybrid LCC with single-star connected stacks

On Figure 7 are presented some of the simplest hybrid topologies based on both VSC and LCC technologies. Depending on the the initial converter, the stacks of SMs may act as an active filter of voltage or current. Thus, these kind of HVDC stations are expected to be more compact than a MMC with equivalent functionalities. Among these three topologies, b) is very similar to the MMC. It is called the Alternate Arm Converter (AAC) [64], more precisely, according to this figure this is an Extended Overlap-Alternate Arm Converter (EO-AAC) [71]. In this thesis, this last topology is studied.

4 Main Contributions and Layout of the Thesis

At the beginning of this research project (2017), the literature about AACs was limited to proof for the good working of the converter [64, 72–74], some steady-state analyses [1, 75]. The control of the converter was incomplete (or at least unpublished..) and finally the question of the dynamic behaviour when connected to the grid essentially focused on faulty conditions [19]. Based on this previous works, the following questions raise:

1. How to operate this hybrid topology and generate the appropriate hybrid modulation scheme?
2. How to improve the existing works on the converter steady-state analysis?
3. What is the appropriate approach to control internal dynamics?
4. Is the converter able to provide similar properties to MMC despite its hybrid operation?

This Thesis, which aims to answer the aforementioned questions, deals with the steady-state and dynamic modelling of the Extended Overlap Alternate Arm Converter. The idea is to adopt a step-by-step approach by establishing a solid basis for the analysis of this converter.

The main contributions and the layout of this work are listed below:

1. Chapter 1 presents a methodology explaining the origins of the AAC topology similarly to [58], but then, a rigorous approach highlights most of the degrees of freedom of the structure to be exploited by the control.
2. In Chapter 2, a detailed steady-state model considering each operating modes, the impact of the control, is proposed for the estimation power electronics devices sizing and passives as well. This steady-state model is extended to losses estimation.
3. Chapter 3 provides a comprehensive description of the dynamics modelling and control. A control structure allowing to manage every state-variables in the system is proposed and validated through strong events. A comparison between the MMC and EO-AAC dynamics is performed. Similarities and differences highlighted. From these similarities a reduced order model structure common to both topology is presented.
4. Chapter 4 is interested to the HVDC and HVAC grid connection. Thanks to the above simplified models, it is proven that DC voltage support using EO-AAC is possible using the exact same principle than MMC. This is extended to MTDC where the possible interoperation between EO-AAC and MMC is shown. The operations under abnormal conditions as the DC-Fault and the unbalanced AC system are presented highlighting limitations and providing leads for future works.

5 List of publications derived from this work

The publications resulting from this Thesis project and Master student supervision are listed below.

- **Journal I**: "*Energy and Director Switches Commutation Controls for the Alternate Arm Converter*". **P. Vermeersch**, F. Gruson, X. Guillaud, M.M.C. Merlin, P. Egrot. Mathematics and Computers in Simulation, 2018.
- **Journal II**: "*A Novel DC Fault Ride Through Control Methodology for Hybrid Modular Multilevel Converters in HVDC Systems*". E. Shahriari, F. Gruson, **P. Vermeersch**, P. Delarue, F. Colas, X. Guillaud IEEE Transactions on Power Delivery, 2020.

- **Journal III**: "*Full Energy Management of EO-AAC: Toward a Dynamic Equivalence with MMC*". **P. Vermeersch**, F. Gruson, M.M.C. Merlin, X. Guillaud, P. Egrot. IEEE Transactions on Power Delivery, 2021.

- **Conference I**: "*Energy Control for the Alternate Arm Converter*". F. Gruson, **P. Vermeersch**, X. Guillaud, P. Egrot. IEEE PES PowerTech, 2017.

- **Conference II**: "*Director switches commutation control for the Alternate Arm Converter*". **P. Vermeersch**, F. Gruson, X. Guillaud, M.M.C. Merlin, P. Egrot. Electrimacs, 2017.

- **Conference III**: "*Control Design of MMC prototype based on OP 5600 Real Time Simulation and eMEGASIM*". **P. Vermeersch**, M. Belhaouane, N. Stankovic, F. Colas, X. Guillaud. opal-rt's 10th International conference on real-time Simulation, 2018

- **Conference IV**: "*On Stored Energy Requirement in the Alternate Arm Converter*". **P. Vermeersch**, F. Gruson, M.M.C. Merlin, X. Guillaud, P. Egrot. IEEE PES Powertech 2019.

- **Conference V**: "*A Stored Energy Control based Active DC Filter for the Alternate Arm Converter with an Extended Overlap Period*". **P. Vermeersch**, F. Gruson, X. Guillaud, M.M.C. Merlin, P. Egrot. EPE ECCE EUROPE 2019.

- **Conference VI**: "*Impact on the electrical characteristics, waveforms and losses of the zero-sequence injection on the Modular Multilevel Converter*". F. Gruson, **P. Vermeersch**, P. Delarue, P. Le Moigne, F. Colas, H. Zhang, M. Belhaouane, X. Guillaud. EPE ECCE EUROPE 2020

- **Conference VII**: "*EMT Simulation of an HVDC Link based on Extended Overlap-Alternate Arm Converter*". **P. Vermeersch**, F. Gruson, P. Egrot, X. Guillaud, F. Colas. CIGRE 2022. UNDER REVIEW

Chapter 1

The AC/DC Conversion for HVDC System

1.1 Introduction

This chapter comes back to the basics of Voltage Source Converter (VSC) topologies and control. It is organised as it follows. The first part recall the square-wave modulation, called in this thesis full-wave control, highlighting the current and voltage waveforms and the way to achieve active power control. Then, in the second part, the principle of modulated voltage control is explained through the two main topologies: the 2-level VSC and the Modular Multilevel Converter (MMC). Finally, the third part of the chapter is composed of two main steps. First, the Alternate Arm Converter (AAC) topology is introduced as an hybrid solutions combining features of full-wave and modulated voltage controls. The different degrees of freedom of the control are explained in addition to the overlap operating mode mandatory for stable operation in both steady-state and transients situations. The second step fully exploit the potential of the overlap operating mode leading to the description of the Extended Overlap-AAC (EO-AAC) the main subject of the thesis.

Note : As a general rule for this chapter, every topologies studied are based on the assumption that the nominal active power is 1 GW and the DC bus voltage 640 kV. Moreover, every curves drawn in per-unit (pu) are obtained on the basis of the DC bus voltage.

1.2 Full-wave controlled 2-Level VSC

The 2-Level VSC, illustrated on Figure 1.1. The AC side is composed of a three-phase voltage source in series with an inductance L_L. The DC side is connected to a constant voltage source. This configuration calls for a current bi-directionality for the DSs (i.e. $DS_{(u,l)J}$). For high power application, since its inception, the IGBT has been the preferred solution thanks to suitable voltage and current ratings (up to 6.5 kV or above 1 kA).

The DC voltage v_{dc} is modulated in order to generate a set of three-phase AC voltages called v_{A0},v_{B0} and v_{C0}. Let us define G_{DSuA} and G_{DSlA} the gate signals of the upper and lower Director Switches (DS) of leg A so that

$$v_{A0} = (G_{DSuA} - G_{DSlA}) \frac{v_{dc}}{2} \tag{1.1}$$

If we define v_{vA}, the converter output AC voltage driving the AC currents such as

$$v_{vA} = v_{A0} - v_{N0} \tag{1.2}$$

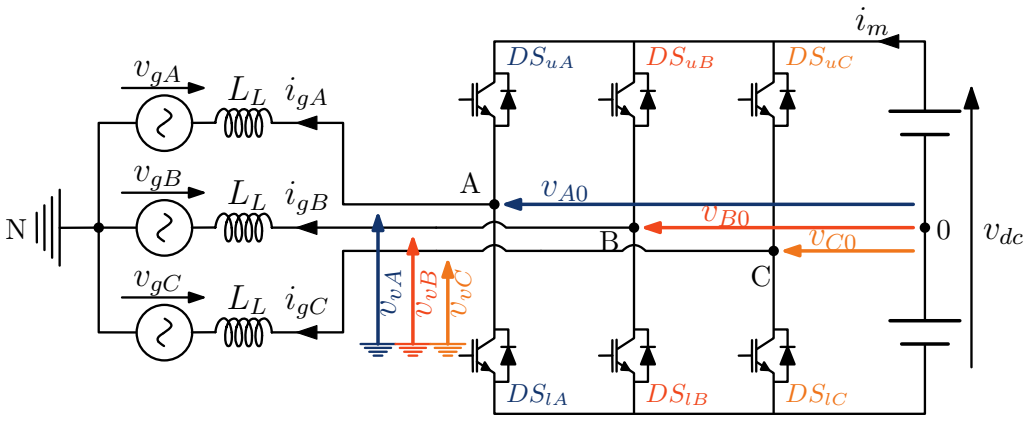


Figure 1.1 – 2-Level Voltage Source Converter

and assume the AC side to be balanced, the zero sequence voltage v_{N0} is derived as it follows

$$v_{N0} = \frac{1}{3}v_{A0} + \frac{1}{3}v_{B0} + \frac{1}{3}v_{C0} \tag{1.3}$$

leading to

$$v_{vA} = \frac{2}{3}v_{A0} - \frac{1}{3}v_{B0} - \frac{1}{3}v_{C0} \tag{1.4}$$

The three-phase grid voltages are defined as

$$v_{gJ} = V_g\sqrt{2}\sin(\omega_g t + \theta_J) = \hat{V}_g \sin(\theta_g + \theta_J) \tag{1.5}$$

with ω_g the grid frequency and $\theta_J = [0; -\frac{2\pi}{3}; \frac{2\pi}{3}]$.

The principle of the full-wave modulation is to switch twice per period. These switching times are a degree of freedom. Therefore, let us introduce δ such that the gate signals of each DS are determined using the following equations.

$$\begin{aligned} G_{DSuA} &= 1 \text{ if } \theta_g \in [-\delta\ ;\ \pi - \delta] \\ G_{DSlA} &= 1 \text{ if } \theta_g \in [\pi - \delta\ ;\ -\delta] \end{aligned} \tag{1.6}$$

Applying (1.6) to get the desired switching pattern gives the following waveforms if we consider δ equals to 15 degrees.

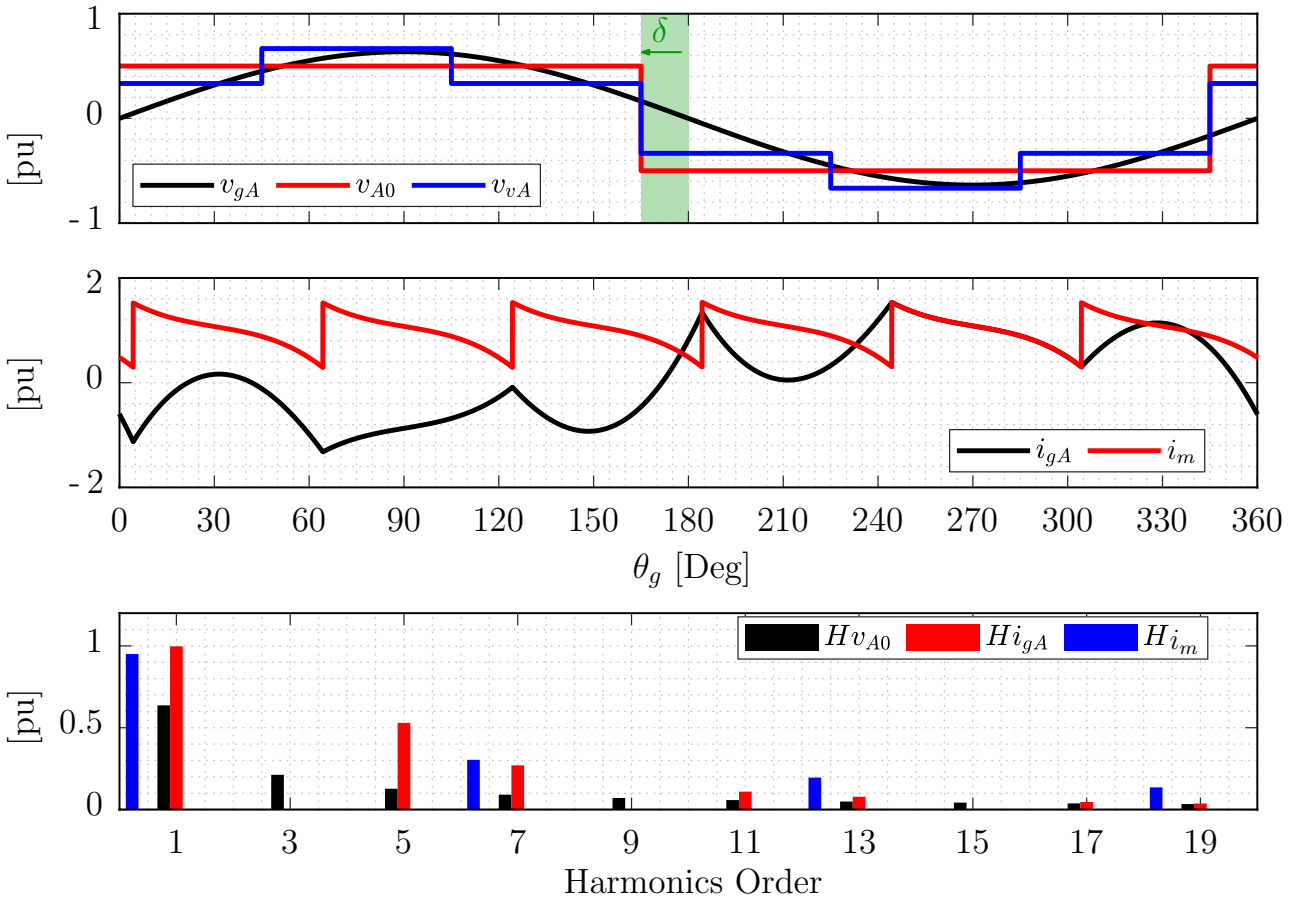


Figure 1.2 – Voltage and current waveforms of full-wave controlled 2-level Converter with $\delta = -15°$

As visible on Figure 1.2, most of the electrical quantities resulting from the full-wave modulation are composed of low order harmonics suggesting the need for bulky passive filters in both sides. The modulated voltages are the well-know 2-level voltages (v_{J0}) between $\pm\frac{v_{dc}}{2}$ while v_{vJ} is a 4-level voltage that can be equal $\pm\frac{2v_{dc}}{3}$ and $\pm\frac{v_{dc}}{3}$.

After this brief recall about the full-wave control, let us introduce how to achieve the active power control with such a modulation scheme. Assuming a balanced operation, a single-phase representation is used in the following lines and the index of the phase is removed. Only the fundamental component of v_v is considered:

$$v_{v1} = V_{v1}\sqrt{2}\sin(\theta_{v1}) \tag{1.7}$$

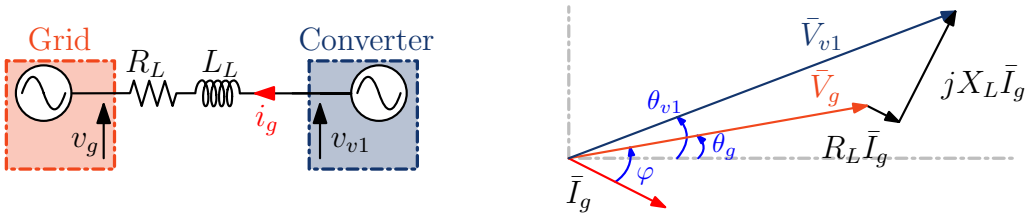
where V_{v1} and θ_{v1} are respectively the RMS value and the angle of the v_{v1}. It can demonstrated that

$$V_{v1} = \frac{1}{\sqrt{2}}\frac{4}{\pi}\frac{v_{dc}}{2} \tag{1.8}$$

showing that V_{v1} only depends on the value of the DC bus voltage and cannot be modified by the control. However, it is worth mentioning that full-wave control achieves the highest modulation index value possible for a conventional converter. This modulation index, noted m has for definition

$$m = \frac{2V_{v1}\sqrt{2}}{v_{dc}} = \frac{4}{\pi} \tag{1.9}$$

Then, if we focus on the fundamental, the following graphs can be obtained.



a) Simplified Model

b) Phasor Diagram

Figure 1.3 – Simplified representation and phasor diagram of two voltage sources interconnected by an inductance

Figure 1.3 a) presents a simplified model of the AC side where the grid voltage v_g and v_{v1} are interfaced through R_L and L_L. From this system, a phasor diagram can be drawn (Figure 1.3 b)). When neglecting the resistance, the well known expression of the active P_{ac} and reactive Q powers can be written:

$$P_{ac} = \frac{3V_g V_{v1} \sin(\theta_{v1} - \theta_g)}{X_L} \tag{1.10a}$$

$$Q = \frac{3V_g \left(V_{v1} \cos(\theta_{v1} - \theta_g) - V_g\right)}{X_L} \tag{1.10b}$$

Replacing V_{v1} by its value derived in (1.8), and $\theta_{v1} - \theta_g$ by δ gives the active and reactive power expressions of a full-wave controlled 2-level VSC

$$P_{ac} = \frac{\frac{6}{\pi\sqrt{2}} V_g v_{dc} \sin(\delta)}{X_L} \tag{1.11a}$$

$$Q = \frac{\frac{6}{\pi\sqrt{2}} V_g v_{dc} \cos(\delta) - 3V_g^2}{X_L} \tag{1.11b}$$

The equations of (1.11) show that δ controls the active power and affects at the same time the reactive power. This later cannot be managed independently since a degree of freedom is missing. Finally, by reversing (1.11a), a basic control scheme can be derived in order to compute the value of δ for a given active power set points as illustrated on Figure 1.4.

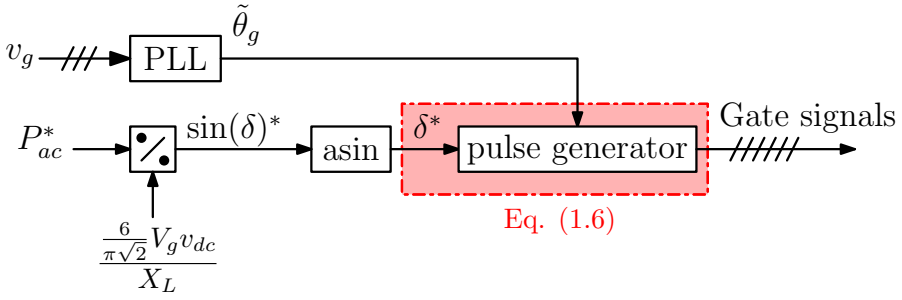


Figure 1.4 – Open-loop control scheme of full-wave controlled 2-Level VSC

where the reference for δ is derived as it follows

$$\delta^* = \arcsin\left(\frac{P_{ac}^* X_L}{\frac{6}{\pi\sqrt{2}} V_g v_{dc}}\right) \tag{1.12}$$

If this control scheme and DS synchronisation procedure are applied then the active power can be controlled as shown by on Figure 1.5. This simulation is achieved using the parameters of Table 1.1.

Parameters	Value SI	Value p.u
Rated power (S_n)	1.04 GVA	1
Nominal active power (P_n)	1 GW	0.96
Nominal reactive power (Q_n)	300 MVAR	0.29
DC Voltage (v_{dc})	640 kV	1
Grid Frequency (f_g)	50 Hz	1
RMS AC Voltage L-to-L (U_g)	500 kV	$\sqrt{3}$
RMS AC Voltage L-to-G (V_g)	288.67 kV	1
Leakage inductance (L_L)	116.6 mH	0.15
Leakage resistance (R_L)	60 mΩ	0.005

Table 1.1 – Simulation parameters of the full-wave controlled 2-level converter

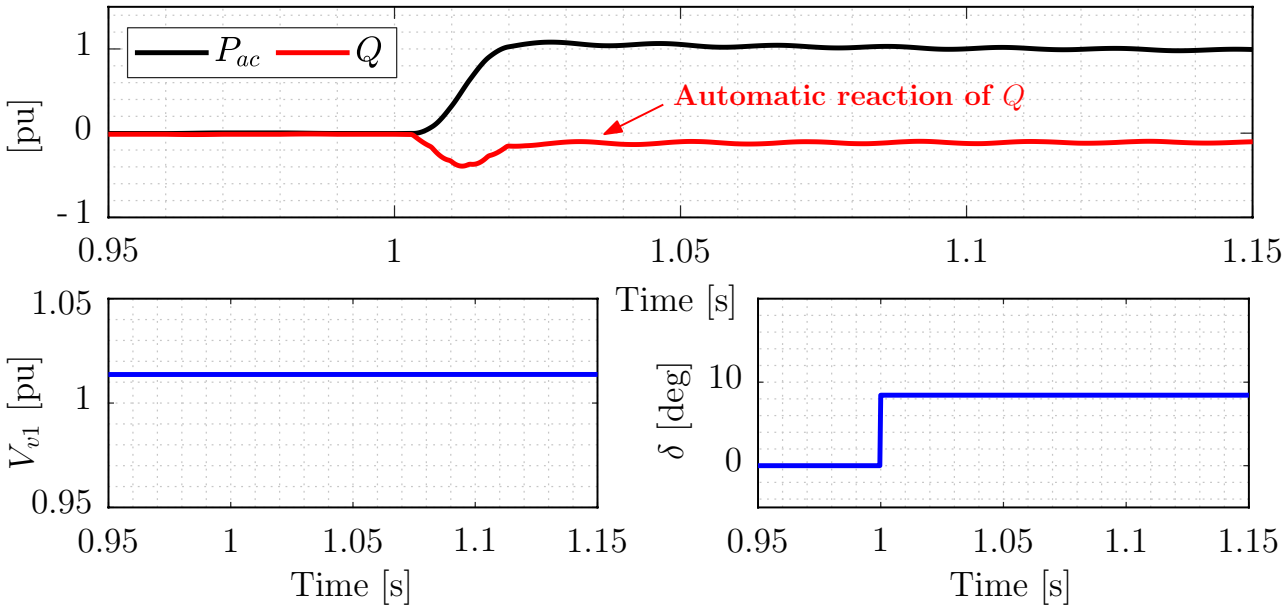


Figure 1.5 – Dynamic response of the 2-Level VSC in full-wave control

Figure 1.5 highlights power dynamics under an active power step of 1 GW at 1 second. Due to the high harmonic content in the AC current, the measurement of the powers is obtained through filters explaining this smooth transient. Note that V_g has been chosen in order to limit reactive power.

To conclude this section on full-wave controlled VSC, three main observations stand out. First, the active power is controlled by shifting the gate signals of all DSs by an angle named δ. Second, the reactive power is not controlled, VAR compensators are therefore needed (using passive or active devices). The final point introduces the main drawback of such control schemes which are the low order harmonics in modulated quantities and AC currents. In both sides, bulky passive filters are required, or active filtering solutions.

1.3 Modulated voltage control

Technology improvements have led to a significant increase of power-electronics device switching frequency. Hence, the harmonic content of modulated quantities has been improved and a new degree of freedom introduced. Unlike the full-wave control, it is now possible to modulate the AC voltage amplitude. One of these solutions providing amplitude modulation is the well-known Pulse Width Modulation (PWM) scheme. Its main principle is to fix the switching frequency higher than the grid one (e.g. a few kHz). In a simplified way, its working principle is recalled as it follows.

First of all, let us introduce the three-phase modulation signals m_{vA},m_{vB} and m_{vC} such as:

$$\begin{aligned} m_{vA} &= m_{A0} - m_{N0} \\ m_{vB} &= m_{B0} - m_{N0} \\ m_{vC} &= m_{C0} - m_{N0} \end{aligned} \tag{1.13}$$

according to (1.2). Neglecting the zero sequence component m_{N0} gives sinusoidal modulation functions

$$\begin{aligned} m_{vA} &= m_{A0} = \hat{M}_{vA} \sin(\theta_g + \theta_{vA}) \\ m_{vB} &= m_{B0} = \hat{M}_{vB} \sin(\theta_g + \frac{2\pi}{3} + \theta_{vB}) \\ m_{vC} &= m_{C0} = \hat{M}_{vC} \sin(\theta_g + \frac{4\pi}{3} + \theta_{vC}) \end{aligned} \tag{1.14}$$

From this sinusoidal modulation signals, transistors gate signals are generated using, for instance, the triangular carrier based approach. Both signals are sent to a comparator, which, if the modulation signal is above the carrier command for the upper DS to be switched ON and vice-versa.

Let us move to a single-phase representation. When using the average converter model it can be written

$$\langle v_v \rangle_{T_{sw}} = \langle m_v \rangle_{T_{sw}} \frac{v_{dc}}{2} \tag{1.15}$$

where T_{sw} is the switching period. It would results in the following waveform of Figure 1.6.

If the 2-Level converter uses a PWM scheme, v_v is composed of 5 levels 0, $\pm\frac{2v_{dc}}{3}$ and $\pm\frac{4v_{dc}}{3}$. Compared to the full-wave modulation, the level 0 has been obtained. However, the main change regards the harmonic content and especially the gap between the fundamental and the first harmonics. Thus, if the average value of v_v over the switching period is calculated, the fundamental clearly appears in red.

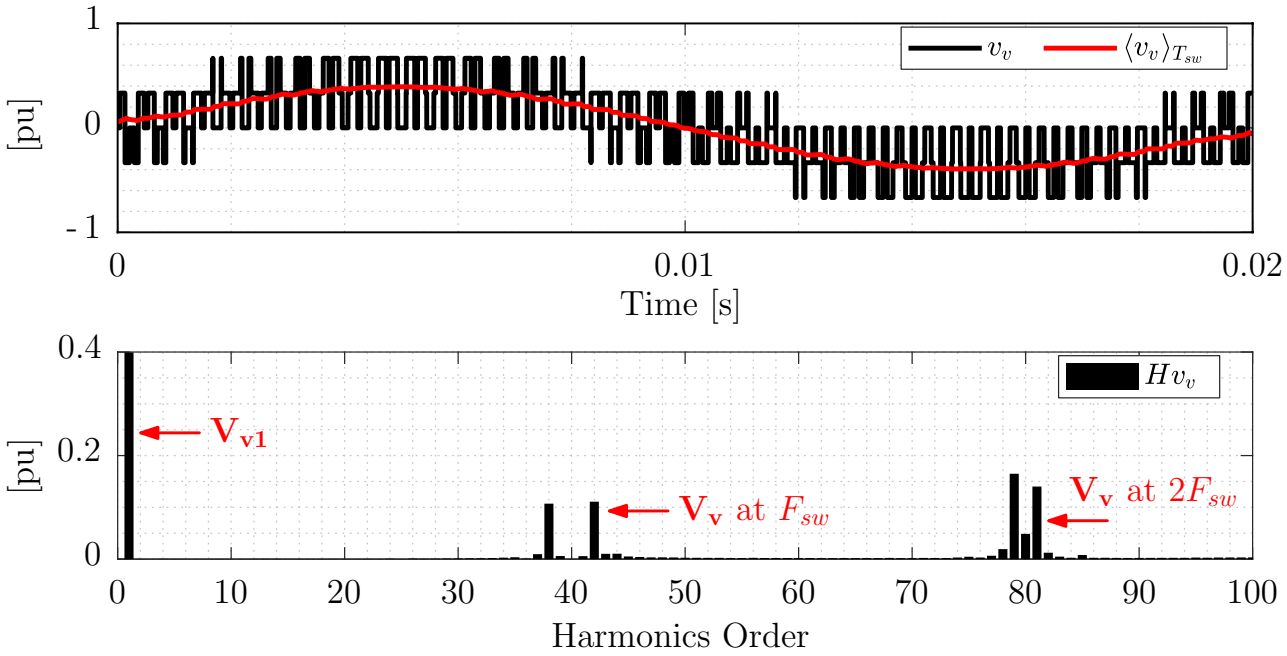


Figure 1.6 – Illustration of a PWM 2-Level converter based on 2 kHz carrier and $\hat{M}_v = 0.8$

To analyse the way to achieve power control, let us focus on the fundamental of v_v.

$$v_{v1} = m_v \frac{v_{dc}}{2} = \hat{M}_v \frac{v_{dc}}{2} \sin(\theta_g + \theta_v) \tag{1.16}$$

where the peak value of the AC voltage is given by

$$\hat{V}_{v1} = \hat{M}_v \frac{v_{dc}}{2} \tag{1.17}$$

and $\hat{M}_v$ is

$$\hat{M}_v \in \left[0; \frac{2}{\sqrt{3}}\right] \tag{1.18}$$

if the zero sequence component m_{N0} is used.

Now, as in the full-wave control, active and reactive power equations of (1.10) can be derived using the same phasor diagram but using (1.17).

$$P_{ac} = \frac{3M_v \frac{v_{dc}}{2} V_g \sin(\theta_{v1} - \theta_g)}{X_L} \tag{1.19a}$$

$$Q = \frac{3M_v \frac{v_{dc}}{2} V_g \cos(\theta_{v1} - \theta_g) - 3V_g^2}{X_L} \tag{1.19b}$$

These expressions are very similar to those of the full wave control but the difference lies in the independent reactive power control thanks to the management of the voltage magnitude.

From these steady-state power equations, an open-loop control scheme could be designed following a similar procedure as for the full-wave control, but in practice a current loop is implemented as in Figure 1.7 to get a closed-loop control on AC currents.

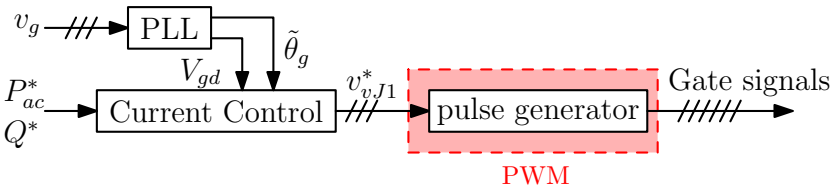


Figure 1.7 – Simplified closed-loop control scheme of PWM 2-Level converter

This controllers can be, for instance, implemented in the Synchronous Rotating Frame (SRF) using dq0 coordinates. In such case, one axis current (e.g. d) is related to the active part while the second is for the reactive part depending on the chosen rotation matrix in the PLL.
Finally, if we apply a closed-loop control on AC currents, then, the dynamic results of Figure 1.8 are obtained.

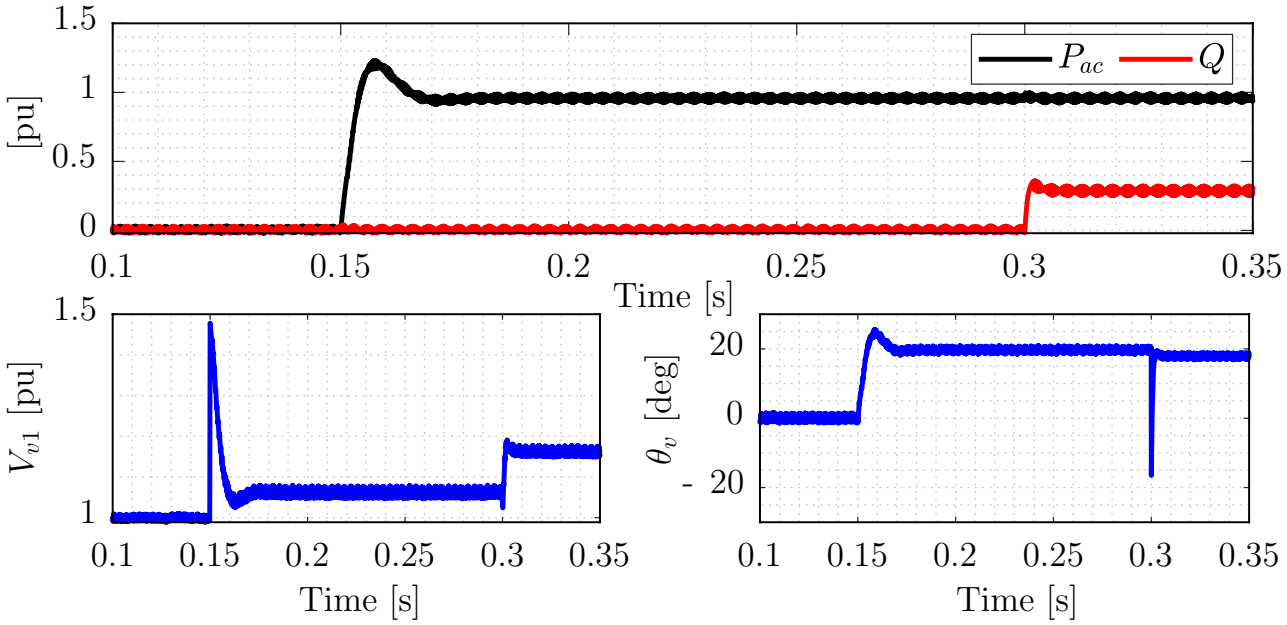


Figure 1.8 – Simulation results of PWM 2-Level converter including current controller

On the first graph of Figure 1.8 are depicted the active and reactive power responses to a step change on their references (respectively 1 GW and 300 MVAR). These curves highlight the effective decoupled control of both power components thanks to phase and amplitude modulation of v_v. The amplitude of V_{v1} and the value of θ_v are presented on the two last graphs where it is clearly visible that θ_v mostly governs the active power and V_{v1} the reactive power.

Conclusion on modulated voltage control using 2-Level topology

The principle of modulated voltage control and its application to 2-level converter has been recalled. Unlike the full-wave control, this technique allows simultaneous phase and amplitude modulation of the AC voltage fundamental featuring decoupled control of active and reactive powers. This capability is particularly useful for grid applications in order to get independent control of AC voltage and frequency. In addition to the AC powers decoupling, the modulation of v_{vJ1} through the increasing of the switching frequency, removes low order harmonics allowing to reduce passive filters size.

However, there are also some drawbacks in using this modulation scheme. The first one is the losses. Indeed, the increasing of the switching frequency has led to an increase of the switching losses.

1.4 The Modular Multilevel Converter

A second solution to get modulated voltage control and low order harmonics suppression from the modulated voltages is to consider the multi-level approach. So far, two topologies multilevel converter have been installed on the grid: the Active-Neutral Point Clamped (A-NPC) [9], and the MMC [14]. This section focuses on MMC which represents the most advanced and planned multilevel topology for future HVDC system. Its structure is illustrated as it follows.

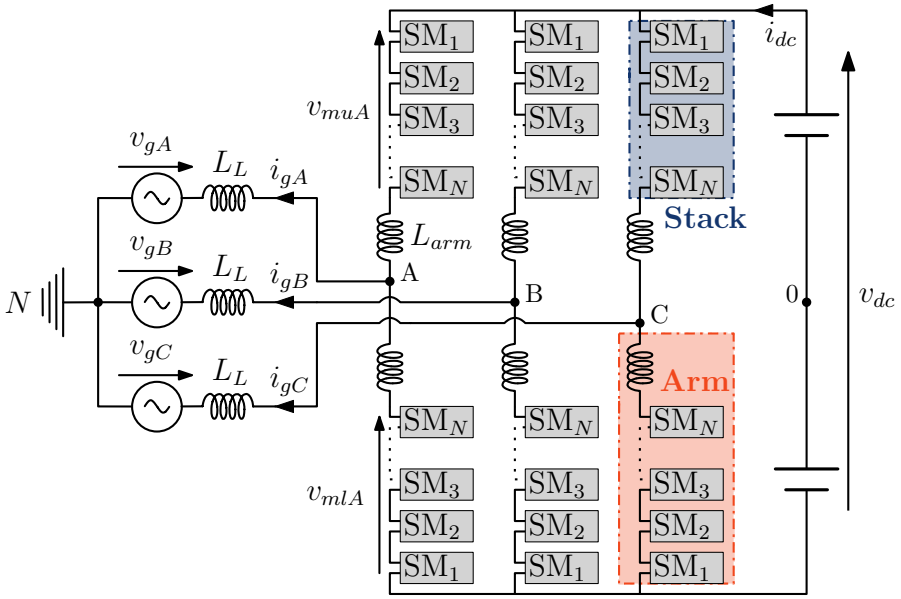


Figure 1.9 – Representation of the MMC

The operating principle of the MMC is very different from classical converter topologies since each MMC arm is never disconnected from the current path through a DS as in the 2-Level VSC. This is made possible by the use of a stack of Sub-Modules (SMs). A stack of SMs is made by a series connection of several elementary components which are small-scale power electronics devices interfacing a floating capacitor [76–79]. This continuous operating mode of the MMC arms involves that, from the DC side perspectives, four voltage sources are connected in parallel (three legs and the DC bus). To avoid uncontrolled power exchange between these sources (through circulating currents), arm inductors have been used. Therefore, each MMC arm is composed of a stack of SMs and an inductor.

Through the gate signals of each SM, the capacitors can be inserted in, or by-passed from, the main current path in order to achieve a characteristic staircase illustrated on Figure 1.10

Thanks to these devices, the MMC has been presented to the community as a suitable solution for HVDC system involving a DC voltage at several hundreds of kV. To approximate the sinusoidal reference voltage, the MMC is equipped with many SMs per stack (N_{SM}) to get a modulated voltage with $N_{SM} + 1$ levels according to Figure 1.10. In the particular case of MMC-HVDC, hundreds of SMs are involved (e.g. 400).

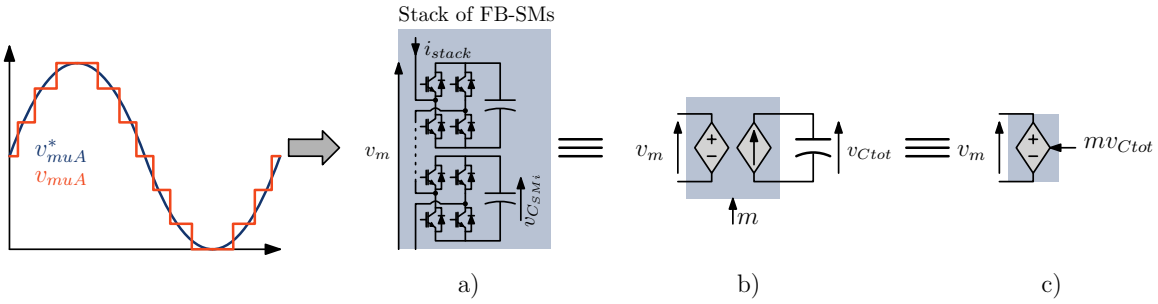


Figure 1.10 – Illustration of MMC modulated voltage waveforms and a) stack of Full-Bridge SMs, b) Average Stack Model, c) Modulated voltage source

In this chapter, we are focusing on principles, then, a stack of SMs is reduced to its average model as in Figure 1.10 b). It results in the following simplified representation of the MMC of Figure 1.11.

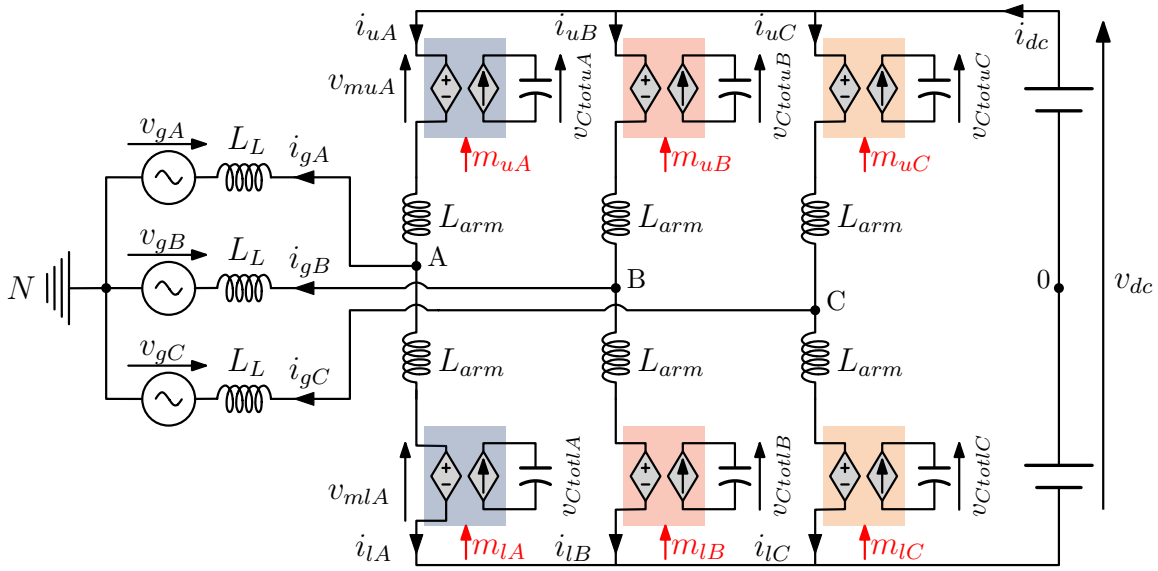


Figure 1.11 – Simplified scheme of the MMC

Compared to conventional converters, the insertion of an internal energy storage devices in the converter arms totally decouple the AC and DC voltages in the sense that the DC bus voltage is no longer used for the modulation of v_{vJ}. Considering single-phase representation, modulated voltages are generated using the internal voltage called v_{Ctot} (see Figure 1.10) such as:

$$\begin{aligned} v_{mu} &= m_u v_{Ctotu} \\ v_{ml} &= m_l v_{Ctotl} \end{aligned} \tag{1.20}$$

Each of these modulated voltages can used to control one of the MMC arm currents (i.e. i_u and i_l). In order to decouple AC and DC quantities, a "sum" (Σ) representation is often used so that Σ variables stand for the DC components in the arm quantities. Regarding the AC side, notations i_g and v_v are kept for the sake of consistency. Thus let us introduce:

$$\begin{aligned} v_v &= \frac{-v_{mu} + v_{ml}}{2} \\ v_\Sigma &= \frac{v_{mu} + v_{ml}}{2} \end{aligned} \tag{1.21}$$

where v_Σ is the so-called differential voltage [80, 81] or DC common mode voltage [82] around $v_{dc}/2$. It is also interesting to note that, unlike the 2-Level VSC the voltage v_v is fictitious. Indeed, applying the KVL leads to the following description of v_v

$$v_v = v_g + \left(L_L + \frac{L_{arm}}{2}\right)\frac{di_g}{dt} + \left(R_L + \frac{R_{arm}}{2}\right)i_g \tag{1.22}$$

which highlights the implication of half of the arm inductors on the AC side dynamics and the fact that it cannot be measured in practice.

If a sufficient number of SMs is used, it is possible to assume the modulation function $m_v = m_{v1}$ and by considering the zero sequence voltage to be zero, it can be demonstrated that

$$m_v = \hat{M}_v \sin(\theta_g + \theta_v) \tag{1.23}$$

m_Σ the DC side modulation function is assumed to be constant.

$$m_\Sigma = M_\Sigma \tag{1.24}$$

Now considering the voltages v_{Ctotu} and v_{Ctotl} yields

$$\begin{aligned} v_v &= \hat{M}_v \left(\frac{v_{Ctotu} + v_{Ctotl}}{2}\right) \sin\left(\theta_g + \theta_v\right) \\ v_\Sigma &= M_\Sigma \left(\frac{v_{Ctotu} + v_{Ctotl}}{2}\right) \end{aligned} \tag{1.25}$$

It results in the waveforms of Figure 1.12 assuming a MMC including 20 SMs per stack and constant capacitor voltages.

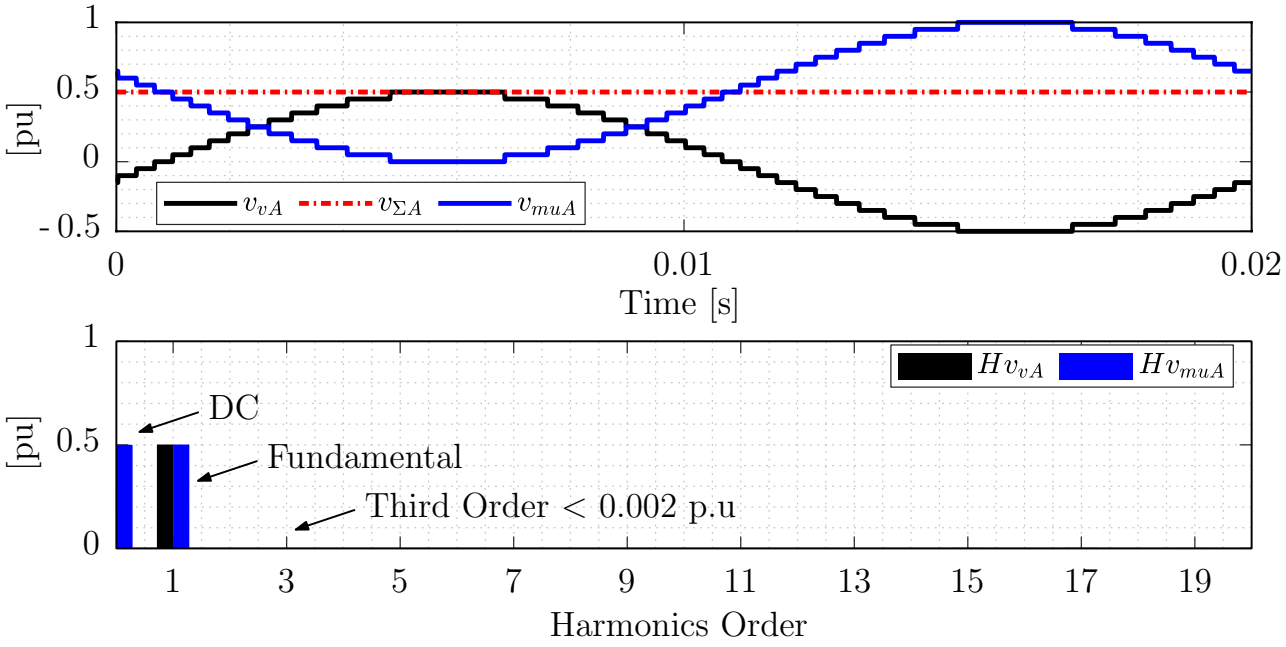


Figure 1.12 – Principle of modulation in MMC including 20 SMs per stack

Thanks to the multi-level approach, modulated voltages are almost sinusoidal and only composed of small voltage steps provided by the insertion or the by-pass of SMs. As a results,

v_{vA} harmonic content is highly reduced involving AC current almost harmonics free. Obviously, the more the MMC has voltage levels, the less AC currents contains harmonics. Moreover, in steady-state each MMC leg generates a constant DC voltage making the DC current flowing through the converter terminals naturally smooth.

The dimensioning of the stacks of SMs is based on the steady-state analysis of modulated voltages peak value. To illustrate, let us consider an operating point at zero power. Thus, $v_v = v_g$ and $v_\Sigma = v_{dc}/2$. The peak positive for v_{mu} is derived as it follows where the modulation index m is introduced

$$\hat{V}_{mu} = \frac{V_{dc}}{2} + \hat{V}_g = \frac{V_{dc}}{2}(1+m) \tag{1.26}$$

Thus, to achieve a modulation index close to 1, (1.26) shows that a MMC stack must be sized for the DC bus voltage. This constraint explains the large number of SMs per stack in HVDC-MMC operating at 640 kVdc. For this reason, most of the time in MMC including Half-Bridge SMs (HB-SMs) the nominal value for v_{Ctot} (V_{Ctot0}) is set to

$$V_{Ctot0} = V_{dc} \tag{1.27}$$

As in the PWM-VSC, it is possible to achieve both modulation of M_v and θ_v but also of m_Σ. As above, let us describe power equations.

$$P_{ac} = \frac{3M_v\left(\frac{v_{Ctotu}+v_{Ctotl}}{2}\right)V_g\sin(\theta_v-\theta_g)}{X_L} \tag{1.28a}$$

$$Q = \frac{3M_v\left(\frac{v_{Ctotu}+v_{Ctotl}}{2}\right)V_g\cos(\theta_v-\theta_g) - 3V_g^2}{X_L} \tag{1.28b}$$

$$P_{dc} = 2m_\Sigma\left(\frac{v_{Ctotu}+v_{Ctotl}}{2}\right)i_{dc} \tag{1.28c}$$

The modulation of v_Σ allows having a control of the DC power which is the main specificity of the MMC. From the above considerations, it is possible to derive closed-loop controllers that would lead to the following simplified control scheme of Figure 1.13.

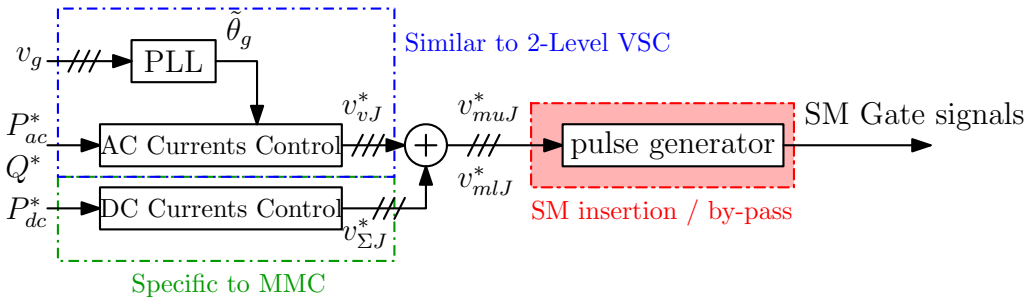


Figure 1.13 – AC side Simplified control scheme of MMC

It is very similar to the 2-level converter control since the AC controllers are the same, however, the modulation of v_Σ introduces a new degree of freedom. Applying this control scheme in a time domain simulation gives the results of Figure 1.14 providing response of AC (active and reactive) and DC powers.

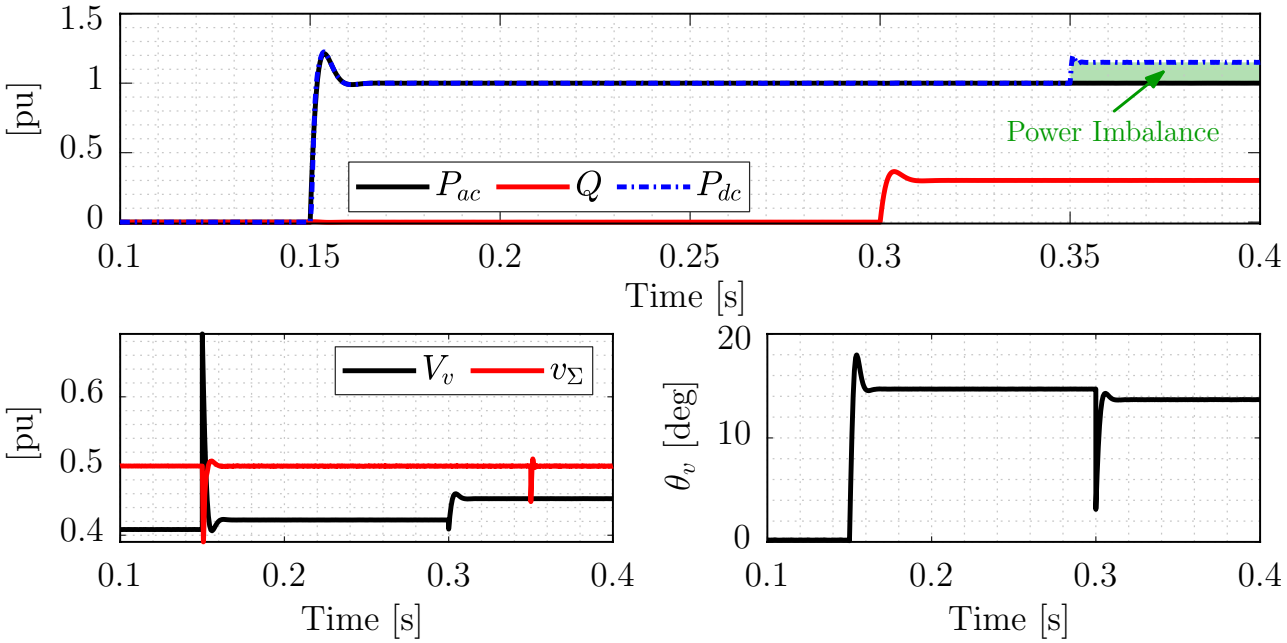


Figure 1.14 – Simulation results of 401 Levels MMC including AC and DC current controllers

As indicated in the Figure 1.14, the active and reactive powers on the AC side can be decoupled thanks to M_v and θ_v. However, the most interesting point of this simulation result concerns the event at 0.35 second. Indeed, it is also true that m_Σ is decoupled from θ_v meaning that P_{ac} is decoupled from P_{dc}. However, if these two control degrees of freedom are managed in a non-coordinated way, then a power imbalance can occur as highlighted in green. However, this difference of active power is supported by the MMC internal energy. So, to ensure the coordinated control of m_Σ and θ_v an energy management is used.

MMC energy management

The introduction of a storage device inside the converter arms and its use for voltage modulation introduces an intermediate step in the energy conversion. Hence, the energy conversion becomes indirect and involves a decoupling between the AC and DC active powers (no straight relation between i_g and i_{dc} thanks to m_v and m_Σ) and a possible deviation of the SM capacitor state of charge. To keep the capability of modulating v_Σ and V_v such a case must be avoided. To describe this important notion of MMC, the converter scheme depicted on Figure 1.15 is now including the different current components that may be found in a MMC arm.

In red line is depicted the AC component of the arm currents defined as

$$i_g = i_u - i_l \tag{1.29}$$

In blue and green lines are respectively presented the DC and the circulating components of the arm currents that belong to the Σ representation. The reason why these components have been separated lies in the fact that, circulating currents (i.e. internal MMC currents not reflected in the AC or DC side) are expected to be zero in steady-state, and hence, not participating in the active power flow[1] while the DC component is responsible for the power transfer and fairly assumed to be equals to $i_{dc}/3$. They can be represented through one single current i_Σ such as

[1]Chapter 3 provide some details about MMC control and the role of circulating currents

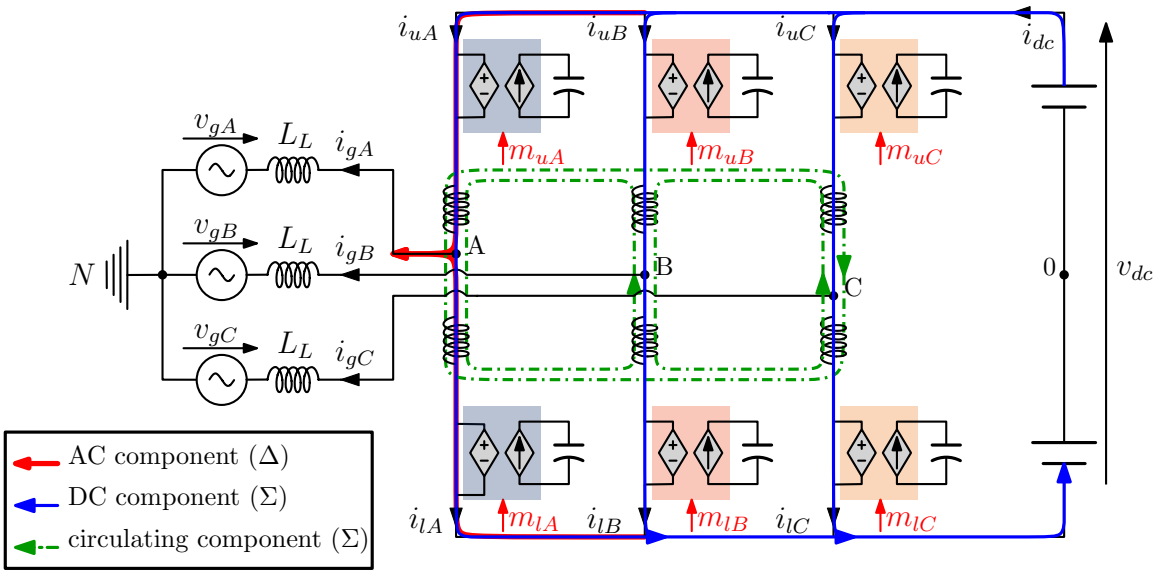


Figure 1.15 – Simplified scheme of the MMC

$$i_\Sigma = \frac{i_u + i_l}{2} \tag{1.30}$$

Through v_Σ, v_v, i_Σ and i_g the decoupling between the AC and DC active powers can be described. So let us focus on the upper stack. The power that is absorbed or furnished by the SM capacitors in instantaneous value (p_u) can be expressed as

$$\begin{aligned} p_u &= v_{mu} i_u \\ &= (v_\Sigma - v_v)\left(\frac{i_g}{2} + i_\Sigma\right) \end{aligned} \tag{1.31}$$

where the active power part (P_u) can be isolated by deriving the average value of this power over the fundamental period.

$$\begin{aligned} P_u &= \frac{1}{2\pi}\int_0^{2\pi} \left(v_\Sigma - \hat{V}_v \sin(\theta_g + \theta_v)\right)\left(\frac{\hat{I}_g}{2}\sin(\theta_g + \varphi) + i_\Sigma\right) \mathrm{d}\theta \\ &= \underbrace{v_\Sigma i_\Sigma}_{\simeq P_{dc}/6} - \underbrace{\frac{V_v I_g}{2}\cos(\theta_v - \varphi)}_{\simeq P_{ac}/6} \end{aligned} \tag{1.32}$$

In practice to achieve P_u in case of transient and steady-state situations, a closed-loop control scheme on the energy storage device dynamics can be implemented. This is the energy management [81, 83]. By using either i_Σ or i_g the level of energy inside the converter can remain stable, and the other current will be in charge of the active power control required for the system operation.

Conclusion on MMC

This section has presented the main working principles of the Modular Multilevel Converter which, unlike conventional converters, includes a stack of SMs with internal energy devices

allowing (i) to get almost harmonics free modulated voltages and (ii) continuous operation of its six arms. It has been demonstrated that three degree of freedom exist in the control with different use. As in the 2-Level VSC, M_v and θ_v are used to decouple active and reactive powers. The use of internal energy storage devices has led to a decoupling between the AC and DC side active powers through the modulation function m_Σ

Therefore, the main features of a MMC are the high quality of both the AC and DC currents, and extended controllability. However, this converter is not without drawbacks. Indeed, it can be noted three main issues:

1. In its Half-Bridge version (HB-MMC) six large arm inductors are required to limit DC-fault current rising leaving times for the AC breakers to be opened. [84, 85]

2. Stacks must be designed for at least the DC voltage to achieve modulation index close to 1. A high number of SMs is therefore needed.

3. The insertion of capacitors in the main current path involves voltage oscillations. The amount of required stored energy is about 40 kJ/MVA [86] increasing the converter station volume.

To improve these points, a new class of modular hybrid converters has emerged. The main idea of these converters is to combine advantages of conventional and modular topologies and controls as well. This is the focus of the next section.

1.5 Hybrid Topologies with Active Filtering Capability and Powers Decoupling

1.5.1 Introduction

As highlighted on Section 1.1, the full-wave control is a simple solution to control the active power, however, it induces uncontrolled reactive power and high harmonic content including low order harmonics. On the other hand, the modulated voltage control allows decoupling active and reactive powers and low order harmonic removal. The 2-level topology is a good solution for a wide range of application; however, it cannot be applied on very high power application. Currently, in the class of converter equipped with voltage modulation, the MMC is the only solution used in the field of HVDC application but its main drawback lies in the large number of SMs to synthesise both AC and DC components of modulated voltage.

This section analyse how the combination of both previous modulation schemes can limit the SM requirement and by extension the footprint of a converter station.

1.5.2 Modulation of v_v and Active Filtering of AC currents

Consider a full-wave controlled 2-Level VSC. To obtain active and reactive powers decoupling as well as sinusoidal AC currents, this basic topology can be combined with stacks of SMs. Two possible approaches exist and discussed hereafter.

First solution : Filtering of the output AC voltages

The filtering of the output voltage supposes to connect, in series with the converter's AC terminals, a stack of SMs to apply a sinusoidal voltage across the transformer windings [72]. This

principle is illustrated on Figure 1.16 where stack of SMs are represented using a modulated voltages source symbol for simplicity.

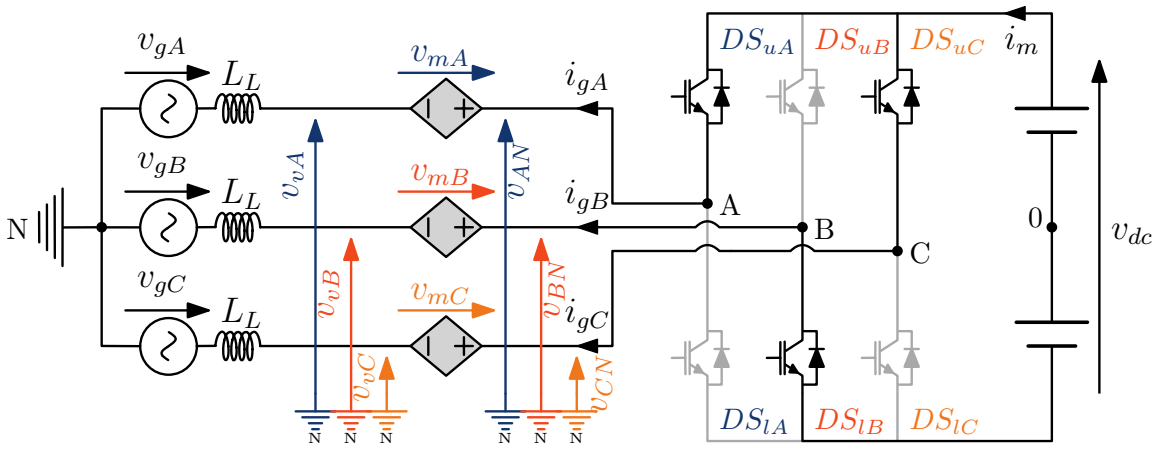


Figure 1.16 – 2-Level converter including series AC voltage active filters

As in the previous sections, the set of three-phase voltages v_{vA},v_{vB} and v_{vC} still control the active and reactive powers. The controllers define the amplitude ($\hat{M}_v$) and angle (θ_v) for the reference signals v^*_{vA},v^*_{vB} and v^*_{vC} according to P^*_{ac} and Q^*.

As shown in Figure 1.2, the voltage modulated by the 2-Level converter are now called v_{AN},v_{BN} and v_{CN} and still composed of four levels. The angle of their fundamentals is fixed by δ. The only modification that can be done on this waveform is a phase shift through δ. If we apply Kirchhoff's voltage law (KVL) on phase A

$$v_{vA} = v_{AN} - v_{mA} \tag{1.33}$$

Hence the waveforms for the modulated voltages is deduced

$$v^*_{mA} = v_{AN} - v^*_{vA} \tag{1.34}$$

Figure 1.17 present the principles and voltage waveforms. In order to generate a sinusoidal waveform for v_{vA}, v_{mA} must compensates the harmonics of v_{AN}. There is, nonetheless, a real issue with the use of this active filtering solution. Indeed, it is clearly visible that v_{mA} is composed of voltage discontinuities introduced by the switching of the DSs and therefore by the different levels of v_{AN}. Thus, handling such discontinuities reveals to be complex (i.e. many SMs to be switched simultaneously) introducing AC current distortion.

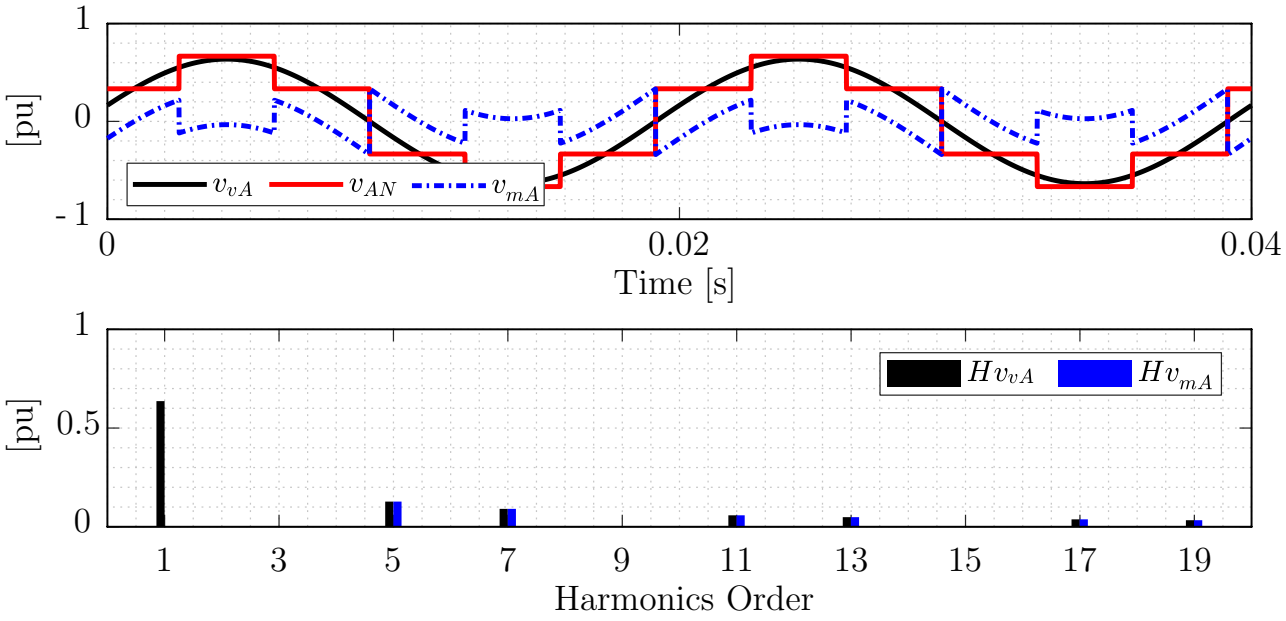


Figure 1.17 – Voltage waveforms of full-wave controlled 2-level converter including series AC active filters ($\theta_v = 15°$)

Second solution : Filtering of $\mathbf{v_{J0}}$

As described by (1.4), the voltages applied on the transformer windings derive from the internal AC voltages v_{A0},v_{B0} and v_{C0}. This second solution lies in the filtering of these voltage instead of considering the converter output voltages. To do so, the active filters are integrated inside the converter as shown on Figure 1.18. This figure considers a configuration where DS_{lA},DS_{uB} and DS_{lC} are opened (i.e. DS in grey).

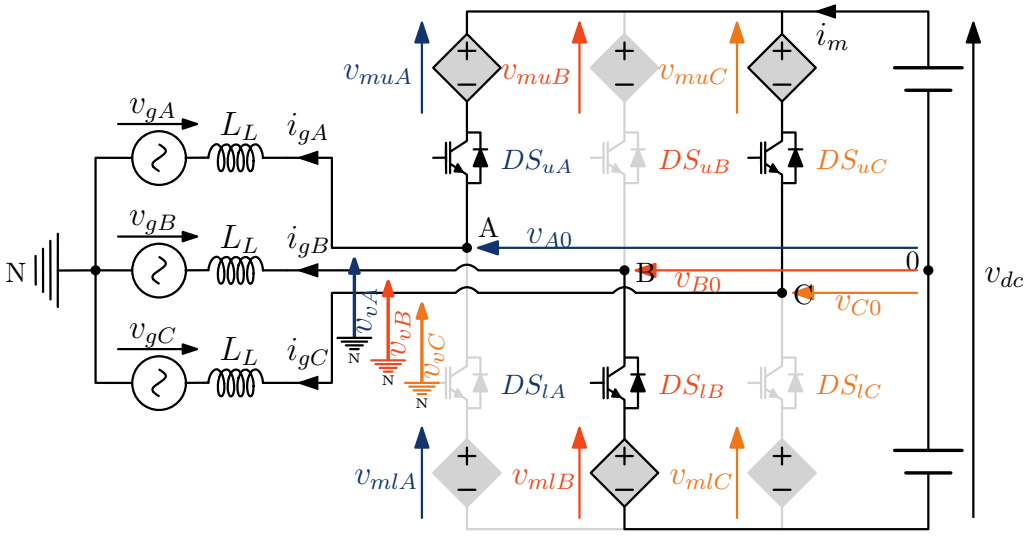


Figure 1.18 – 2-Level converter with integrated AC voltage active filters

If we consider the zero sequence voltage v_{N0} equals to zero and focus on the leg A then

$$v_{vA} = v_{A0} \tag{1.35}$$

To obtain a sinusoidal waveform for v_{vA}, v_{A0} must only include a fundamental component. By

applying the KVL yields the reference for the upper modulated voltage

$$v^*_{muA} = \frac{v_{dc}}{2} - v^*_{vA} \tag{1.36}$$

While the following references must be generated for the lower modulated voltage

$$v^*_{mlA} = \frac{v_{dc}}{2} + v^*_{vA} \tag{1.37}$$

The introduction of the modulated voltage sources inside the converter arms leads to a sequential operating modes of these devices according to the DSs state. Considering a single-phase representation yields

- If $\theta_g \in [-\delta; \pi - \delta]$ then DS_u is ON and $v_v = v_{dc}/2 - v_{mu}$
- If $\theta_g \in [\pi - \delta; -\delta]$ then DS_l is ON and $v_v = -v_{dc}/2 + v_{ml}$

Once a DS is open, the stack stops modulating the AC component v_v and maintain a constant voltage to limit the maximal voltage it must generate, and hence its design. This is illustrated on Figure 1.19.

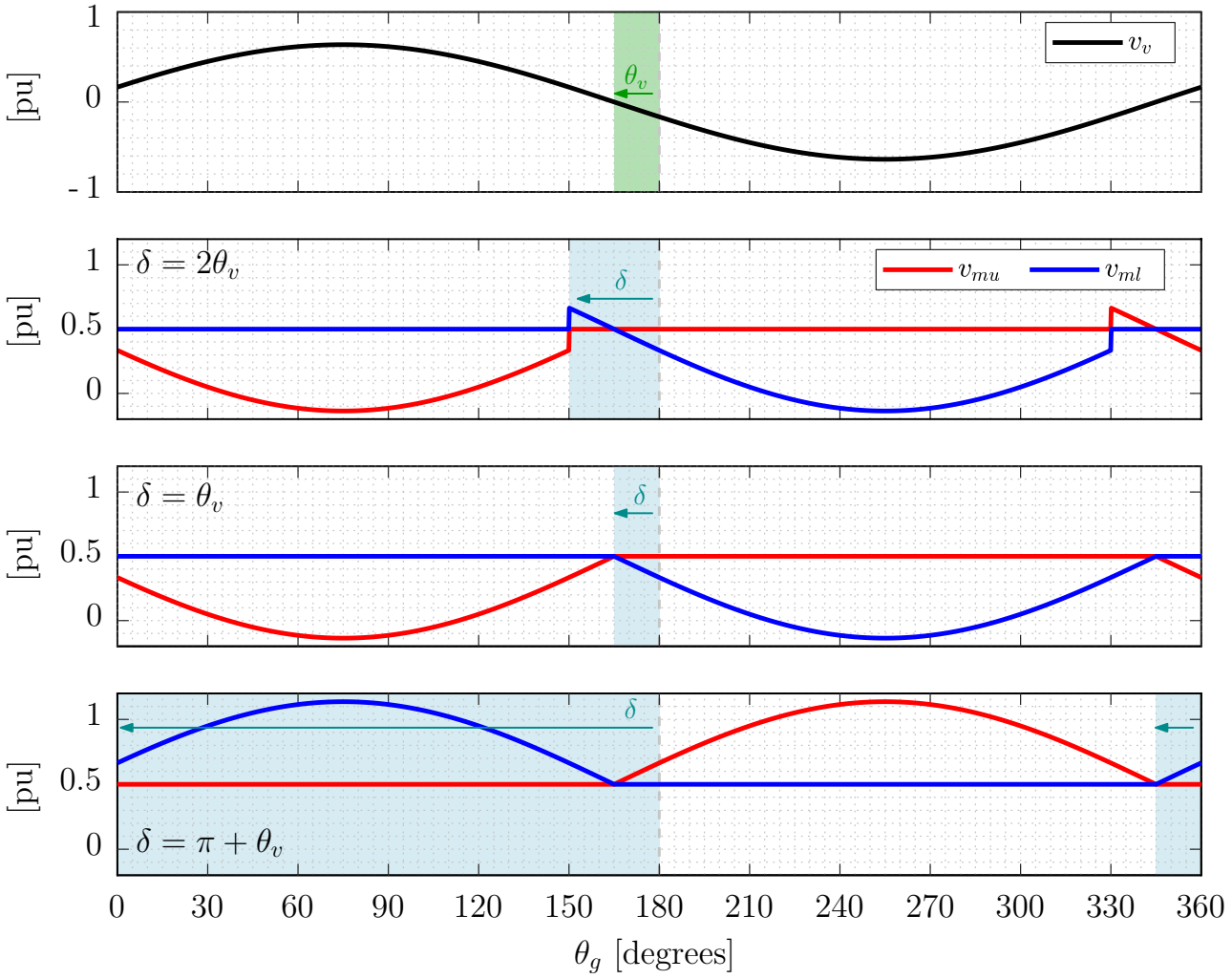


Figure 1.19 – Voltage waveforms of full-wave controlled 2-level converter with integrated active filters ($\theta_v = 15°$)

As afore mentioned, v_v is defined in angle and magnitude by the active and reactive power references. However, v_{mu} and v_{ml} can have different references. Indeed, the angle δ driving the control the DSs is a degree of freedom that may be used to adjust the modulated voltages as presented on Figure 1.19. On Figure 1.19 a), v_v is drawn for θ_v set to 15 degrees.
The other graphs illustrate v_{mu} and v_{ml} in case of $\delta = 2\theta_v$, $\delta = \theta_v$ and $\delta = 180^o + \theta_v$. It is clearly visible that the best case is $\delta = \theta_v$. Indeed, the sinusoidal component of v_v is always subtracted to $v_{dc}/2$, hence, the maximal positive value for v_{mu} is $v_{dc}/2$. As stated above, the MMC stacks are often designed for the whole DC bus while in this case, stacks of SMs must be designed for at least

$$\hat{V}_m = \frac{V_{dc}}{2} \tag{1.38}$$

where $\hat{V}_m$ is the peak modulated voltage. Such small stack design is allowed thanks to the DSs which, once open, block the remaining voltage across the arm. The expression of the voltage across one DS is

$$v_{DS} = v_{dc} - v_{ml} - v_{mu} \tag{1.39}$$

Let us consider the case where the upper DS of a phase leg is closed and the lower one opened. Thus, in such case v_v is modulated through v_{mu}. It gives

$$v_{DSl} = v_{dc} - v_{ml} - \underbrace{\frac{v_{dc}}{2} + \hat{V}_v \sin(\theta_g + \theta_v)}_{v_{mu}} \tag{1.40}$$

To minimise v_{DSl}, this expression shows that it is needed to maximise v_{ml}. It means that v_{ml} is set to $\frac{v_{dc}}{2}$ according to (1.38). Hence,

$$v_{DSl} = v_{dc} - \underbrace{\frac{v_{dc}}{2}}_{v_{ml}} - \underbrace{\frac{v_{dc}}{2} + \hat{V}_v \sin(\theta_g + \theta_v)}_{v_{mu}} = \hat{V}_v \sin(\theta_g + \theta_v) \tag{1.41}$$

Figure 1.20 shows its waveform.

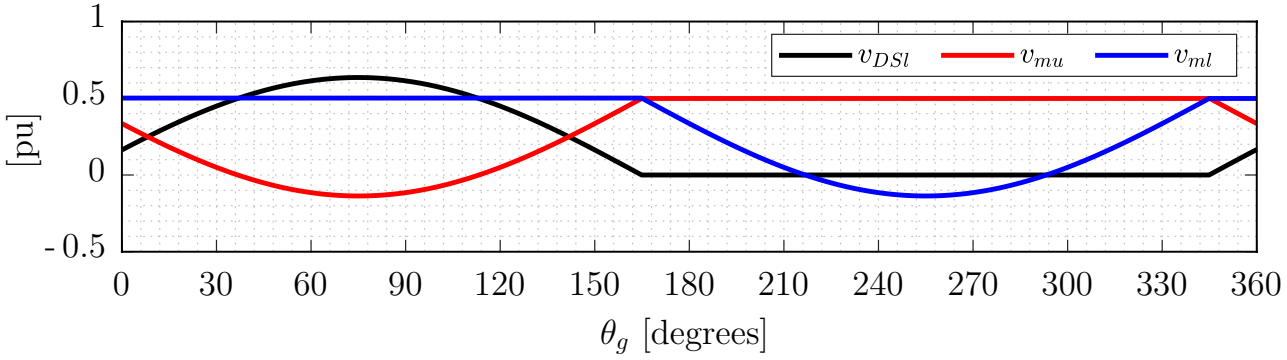


Figure 1.20 – Waveforms of v_{DSlA},v_{muA} and v_{mlA}

Thus, the peak value across the DS ($\hat{V}_{DS}$) can be estimated to

$$\hat{V}_{DS} = \hat{V}_v \tag{1.42}$$

This section has introduced the main principle of the Alternate Arm Converter (AAC) defined as a hybrid converter combining features of the 2-level converter and MMC in [73].

Thanks to the use of stacks of SMs in each of its arms, the AAC is able to have a complete control of the active and reactive current components. In addition, an appropriate control of the DS, reduces by two the number of SMs compared to a MMC representing one of the major assets of this topology.

However, as introduced in the section dedicated to the MMC, the use of the stack of SMs including storage devices involves an "absolute" need for a power balance to avoid energy deviation. For some of these converters, their internal level must be managed. As introduced in the following section, the sequential operations of the AAC creates a specific operating point called the energy sweet-spot ensuring a natural power balance.

1.5.3 Introduction to the energy sweet-spot

SM capacitor voltages can oscillate due to the AC components in the arm power, however, their average state of charge must remain constant in steady-state. Hence, the average value of the arm power must be zero in average over a period of the fundamental. Let us focus on a single-phase representation.

If DS_u is closed ($\theta_v \leq \theta_g \leq \theta_v + \pi$)

$$\begin{aligned} v_{mu} &= \frac{v_{dc}}{2} - v_v \\ i_u &= i_g \end{aligned} \tag{1.43}$$

and

$$p_u = \left(\frac{v_{dc}}{2} - v_v\right) i_g \tag{1.44}$$

If DS_l is closed ($\theta_v + \pi \leq \theta_g \leq \theta_v$), the arm current is zero and p_u as well.

Then the active power P_u is derived as it follows

$$\begin{aligned} P_u &= \frac{1}{2\pi} \int_{-\delta}^{\pi-\delta} v_{mu} i_g \, \mathrm{d}\theta_g \\ &= \frac{1}{2\pi} \int_{-\delta}^{\pi-\delta} \left(\frac{v_{dc}}{2} - \hat{V}_v \sin(\theta_g + \theta_v)\right) \hat{I}_g \sin(\theta_g + \varphi) \, \mathrm{d}\theta_g \\ &= \frac{v_{dc} I_g}{\sqrt{2}\pi} \cos(-\delta + \varphi) - \frac{V_v I_g}{2} \cos(\theta_v - \varphi) \end{aligned} \tag{1.45}$$

This power must be zero.

First of all, consider the case where the reactive power is zero (i.e. the load angle φ is zero) and $\delta = \theta_v$ as suggested in the above section. It leads to

$$\hat{V}_v = \frac{4}{\pi} \frac{v_{dc}}{2} \tag{1.46}$$

From (1.46) and for a given value of v_{dc}, a strict condition on the AC voltage fundamental magnitude ensuring the power balance ($P_u = 0$) has been be derived. This condition is called the sweet-spot [64] and it highlights that for a specific ratio between the AC and DC voltages, the power balance is naturally achieved. Moreover, it can be seen that this ratio corresponds to the modulation index of full-wave controlled 2-level VSC. This simplified expression highlights the importance of the coordinated management of the two modulation schemes as defined in the introduction.

The expression of the energy sweet-spot can be generalised to the case where reactive power is exchanged and $\delta \neq \theta_v$

$$\hat{V}_v = \frac{4}{\pi}\frac{v_{dc}}{2}\frac{\cos(-\delta+\varphi)}{\cos(\theta_v-\varphi)} \tag{1.47}$$

The expression (1.47) suggests that the angles φ,θ_v and δ are involved in the power balance. At this stage, maintaining the power balance inside the converter is possible by using δ and φ. This is illustrated on Figure 1.21 where v_g has been set to the sweet-pot in order to limit P_u (since v_v will be closed to (1.46)). The first graph shows P_u for a variation of Q if $\delta = \theta_v$. The second graph considers a variations of both Q and δ.

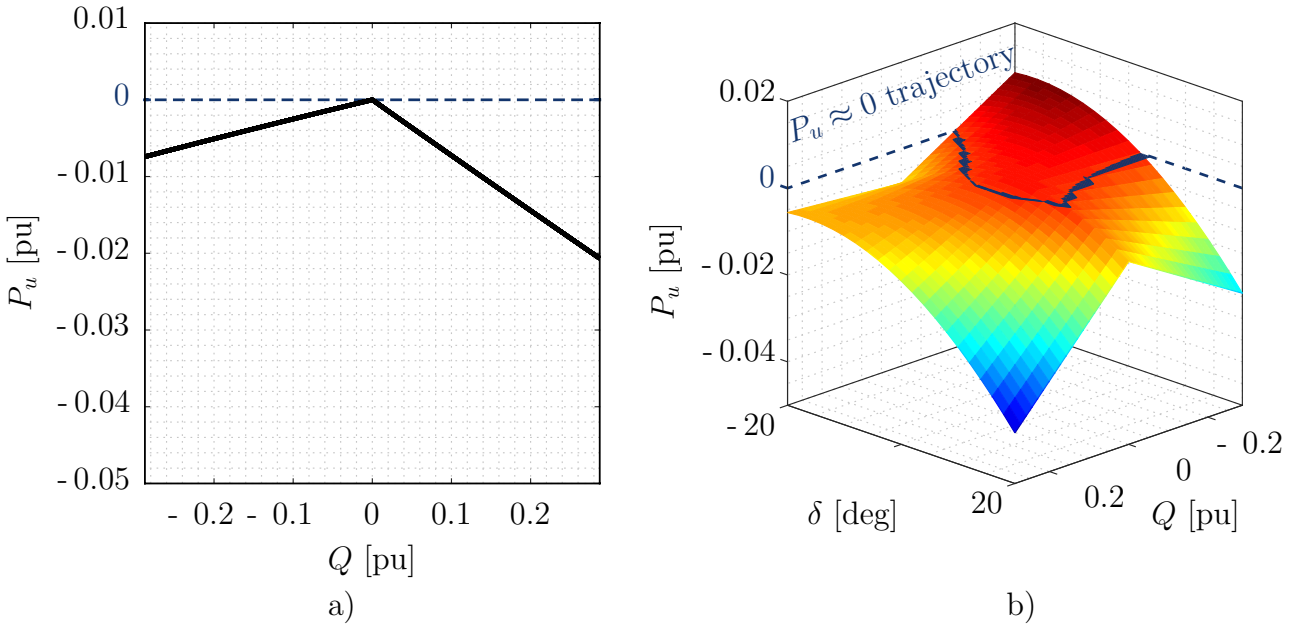


Figure 1.21 – Evolution of P_u: a) for a variation of of Q with $\delta = \theta_v$, b) for a variation of Q and δ

As shown by Figure 1.21 a), since v_g has been properly chosen according to the sweet-spot condition, in case of Q equals to 0, then $V_v = V_g$ fulfilling (1.46). Figure 1.21 b) shows the case where both δ and φ (through Q) are varied. A trajectory $P_u = f(\varphi, \delta)$ allowing to achieve zero average power has been highlighted thus fulfilling Equation (1.47).

Through these two graphs, the use of the reactive power and the DS control angle to maintain the energy inside the AAC stable has been presented. However, this solution presents significant disadvantages:

1. The reactive power is no more dedicated to a function like AC voltage control. In other word, the AC powers decoupling obtained through modulated voltage control is lost.

2. By varying δ, modulated voltage discontinuities will appear and stacks over-sizing as pointed out by Figure 1.19.

In order to keep an independent control of both active and reactive powers and $\delta = \theta_v$, another degree of freedom must be found. To solve this problem, the overlap operating mode has been proposed.

1.5.4 The overlap operating mode

The overlap operating mode is a MMC like mode where the two DSs are closed at the same time. The duration of this operating mode is called the overlap period. This is illustrated on Figure 1.22 where the leg A operates as a MMC leg and is therefore able to maintain its own energy stable by driving the current i_Σ depicted in green, also called the overlap current.

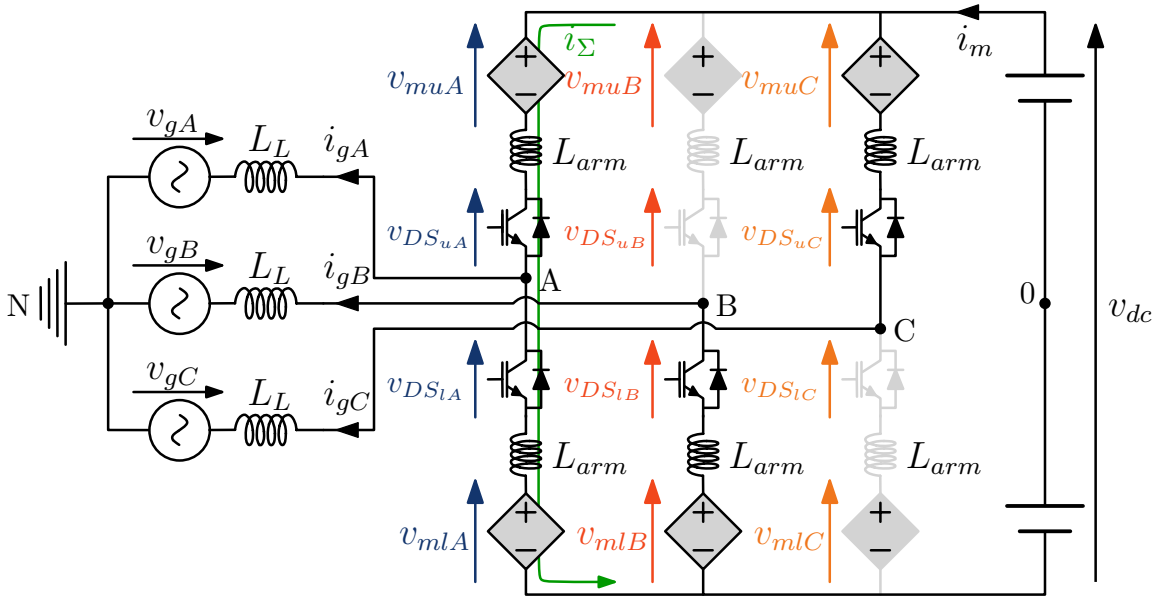


Figure 1.22 – AAC topology including leg A in overlap operating mode

It is needed for each leg to be stable from the energy perspectives. Thus, each leg operates in a sequential way the overlap operating mode. The introduction of this MMC mode requires the use of arm inductors to avoid a straight connection between the stack of SMs and the DC bus. The leg in overlap must have each of its stacks participating to the voltage modulation using the following expressions

$$\begin{aligned} v^*_{mu} &= v^*_\Sigma - v^*_v \\ v^*_{ml} &= v^*_\Sigma + v^*_v \end{aligned} \tag{1.48}$$

which are the exact same expressions than the MMC modulated voltages so that both of the AC and DC components in the arm currents of the leg in overlap mode can be controlled.

To achieve this overlap period, the conduction period of each arm is increased. The length of overlap period θ_{ovl} and its position according to δ are two degrees of freedom having a great impact on the sizing of the stacks of SMs. This is illustrated on Figure 1.23 where θ_{ovl} is set to 30 degrees where two case are considered.

Case 1:

$$\begin{aligned} G_{DSu} = 1 \text{ if } \theta_g \in [-\delta; \pi - \delta + \theta_{ovl}] \\ G_{DSl} = 1 \text{ if } \theta_g \in [\pi - \delta + \theta_{ovl}; -\delta] \end{aligned}$$

Case 2:

$$\begin{aligned} G_{DSu} = 1 \text{ if } \theta_g \in \left[-\delta - \frac{\theta_{ovl}}{2}; \pi - \delta + \frac{\theta_{ovl}}{2}\right] \\ G_{DSl} = 1 \text{ if } \theta_g \in \left[\pi - \delta - \frac{\theta_{ovl}}{2}; -\delta + \frac{\theta_{ovl}}{2}\right] \end{aligned} \tag{1.49}$$

The first case of Figure 1.23 consider the overlap period to be executed after δ. As visible in the area filled in blue, once the overlap period is activated the lower stack experiences a discontinuity to reach its reference. As in the determination of δ according to θ_v, a better choice exists. The second case highlights that an even distribution of the overlap period around δ avoids any voltage discontinuity and decrease the peak values of modulated voltages as well

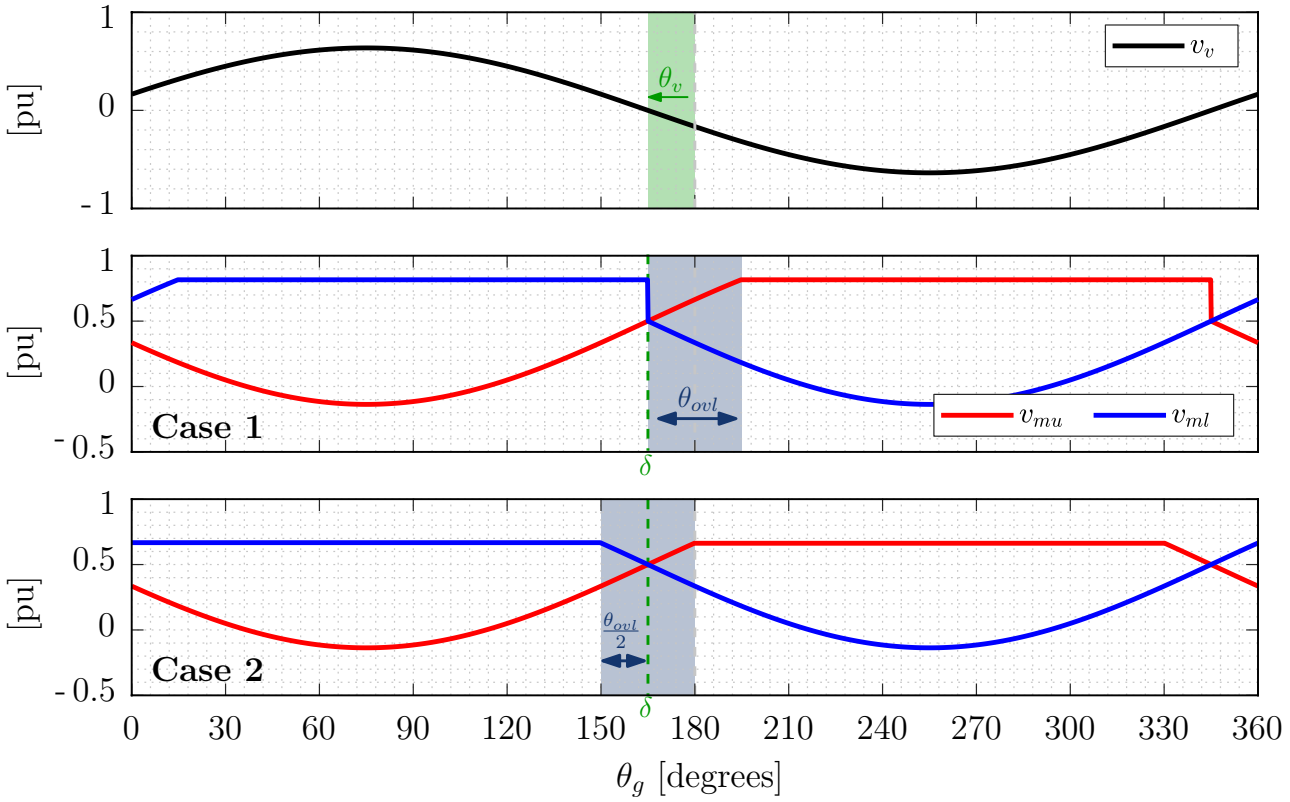


Figure 1.23 – Illustration of v_{mu} and v_{ml} for different position of the overlap period with respect to θ_v

gate signals for upper and lower DS are therefore computed by using the second case where the overlap period is evenly distributed around δ. In fact, it corresponds to the zero crossing of v_v.

Since the overlap mode increases the conduction period of each arm, it consequently modifies the sizing of the stack of SMs. The initial design including half of a MMC stacks (i.e. $V_{dc}/2$) is no more valid. According to Figure 1.23, the positive peak value for modulated voltages is now given by

$$\hat{V}_m = \frac{V_{dc}}{2} + \hat{V}_v \sin\left(\frac{\theta_{ovl}}{2}\right) \tag{1.50}$$

and includes a part of the AC component as a function of the overlap period length. So, the more a stack is conducting, the more it should generate positive voltage, thus increasing its sizing. However, the DS design benefits from this longer conduction period as depicted on Figure 1.24. In black line is the voltage across DS_l in case of $\theta_{ovl} = 30$ degrees while the grey line corresponds to the previous one of Figure 1.20.
The expression (1.40) remains the same and is recalled below

$$v_{DSl} = v_{dc} - v_{ml} - \underbrace{\frac{v_{dc}}{2} + \hat{V}_v \sin(\theta_g + \theta_v)}_{v_{mu}} \tag{1.51}$$

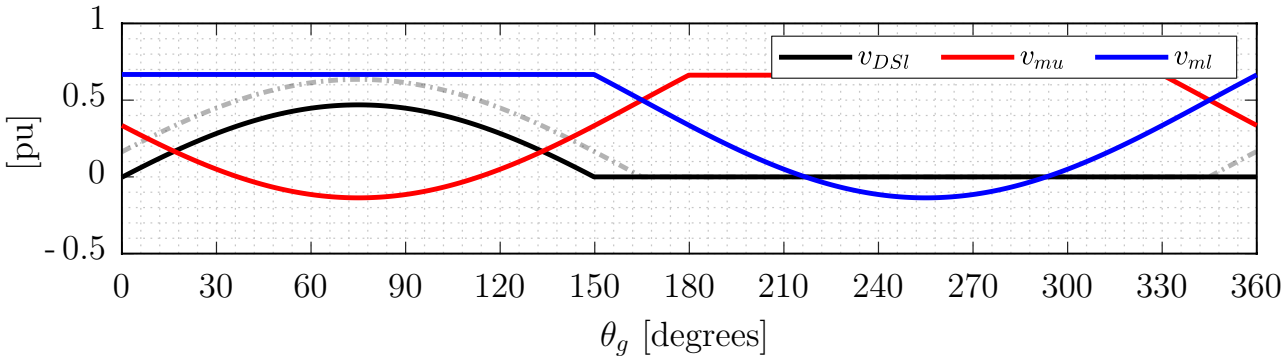


Figure 1.24 – Illustration of v_{DSlA}, v_{muA} and v_{mlA} for θ_{ovl} set to 30 degrees

As it was done previously, to minimise the voltage across the DS, v_{ml} is maximised. Compared to the case of the AAC without overlap period, a stack is now equipped with more SMs to generate, at least, (1.50). So, v_{ml} is replaced by this expression.

$$v_{DSl} = V_{dc} - \underbrace{\frac{V_{dc}}{2} + \hat{V}_v \sin\left(\frac{\theta_{ovl}}{2}\right)}_{v_{ml}} - \underbrace{\frac{V_{dc}}{2} + \hat{V}_v \sin(\theta_g + \theta_v)}_{v_{mu}} \tag{1.52}$$

the above equation allows deriving the required voltage blocking capability of a DS with respect to the overlap period.

$$\hat{V}_{DS} = \hat{V}_v \left(1 - \sin\left(\frac{\theta_{ovl}}{2}\right)\right) \tag{1.53}$$

The voltage blocking capability of the DSs can be decreased with the increase of θ_{ovl}.

The impact of the overlap period on the dimensioning of the stacks and the DSs is now completed. Let us investigate its impact on the power balance which is the main reason why the overlap mode has been introduced. To do this, similar derivations as the sweet-spot demonstration are detailed. According to Figure 1.23,

DS_u **and** DS_l **are closed IF** $\left(-\delta - \frac{\theta_{ovl}}{2} \leq \theta_g \leq -\delta + \frac{\theta_{ovl}}{2}\right)$ **OR** $\left(\pi - \delta - \frac{\theta_{ovl}}{2} \leq \theta_g \leq \pi - \delta + \frac{\theta_{ovl}}{2}\right)$

$$\begin{aligned} v_{mu} &= \frac{v_{dc}}{2} - v_v \\ i_u &= \frac{i_g}{2} + i_\Sigma \end{aligned} \tag{1.54}$$

and

$$p_u = \left(\frac{v_{dc}}{2} - v_v\right)\left(\frac{i_g}{2} + i_\Sigma\right) \tag{1.55}$$

Only DS_u **is closed IF** $\left(-\delta + \frac{\theta_{ovl}}{2} \leq \theta_g \leq \pi - \delta - \frac{\theta_{ovl}}{2}\right)$

$$\begin{aligned} v_{mu} &= \frac{v_{dc}}{2} - v_v \\ i_u &= i_g \end{aligned} \tag{1.56}$$

and

$$p_u = \left(\frac{v_{dc}}{2} - v_v\right) i_g \tag{1.57}$$

Then, by deriving the average value of p_u according to the operating mode and over the fundamental period yields:

$$P_u = \frac{v_{dc} I_g}{\sqrt{2}\pi} \cos(-\delta + \varphi) \cos\left(\frac{\theta_{ovl}}{2} + \varphi\right) - \frac{V_v I_g}{2} \cos(\theta_v - \varphi) + v_{dc} i_\Sigma \left(\frac{\theta_{ovl}}{\pi}\right) \tag{1.58}$$

From the expression of (1.58) it is possible to describe two ways for maintaining the power balance. The first one is a new expression of the energy sweet-spot. Indeed, the sweet-spot has been defined has a natural way to achieve power balance, meaning that, i_Σ and P_u are zero. Thus, the new expression of the sweet-spot is given by

$$\hat{V}_v = \frac{4}{\pi} \frac{v_{dc}}{2} \frac{\cos(-\delta + \varphi) \cos\left(\frac{\theta_{ovl}}{2} + \varphi\right)}{\cos(\theta_v - \varphi)} \tag{1.59}$$

where the basis value introduced the full-wave control of the DS is still present but the overlap period tends to decrease the "ideal value" of $\hat{V}_v$. The other way to maintain the power balance in the converter lies in the use of i_Σ. By using (1.58) the steady-state expression of this current for $P_u = 0$ can be derived as it follows

$$i_\Sigma = I_g \left(-\frac{1}{\sqrt{2}\pi} \cos(-\delta + \varphi) \cos\left(\frac{\theta_{ovl}}{2} + \varphi\right) + \frac{V_v}{2 v_{dc}} \cos(\theta_v - \varphi) \right) \left(\frac{\pi}{\theta_{ovl}}\right) \tag{1.60}$$

leading to a complex expressions where many parameters are involved. Due to the existence of the energy sweet-spot, it seems clear that the more the converter operates far from this point, the more P_u is high and hence the overlap current magnitude. Moreover, as the power balance is a matter of average value, the smaller is the overlap period, the higher is the instantaneous overlap current to compensate. To highlight the amplitude of this currents, the following figure presents it for a fixed set of parameters: $\delta = \theta_v = 15$ degrees $\varphi = 0$, $v_{dc} = 1$ p.u and the nominal value V_v is $\frac{2}{\pi} v_{dc}$.

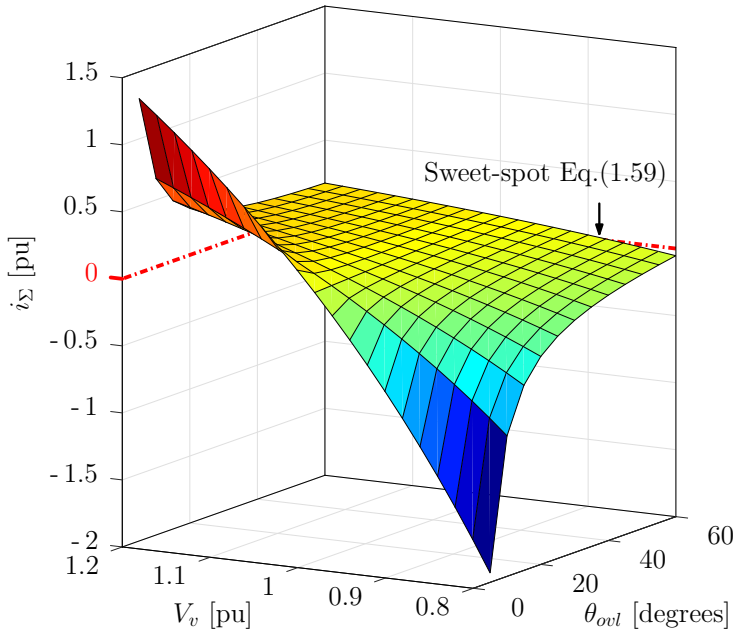


Figure 1.25 – Overlap current magnitude according to θ_{ovl} and V_v

As shows Figure 1.25, since the magnitude of i_Σ is divided by the overlap angle, then this current changes in non-linear way. At very low overlap angle the demand for balancing current becomes unrealistic and increase during transients. On the other hand, the longer is the overlap period, the more the magnitude of i_Σ is stabilised and become almost linearly dependent of V_v. However, the design of the stack increases.
By considering an overlap angle of 30 degrees, the arm current i_u and the DC current i_m can be obtained if sinusoidal AC currents are assumed. They are depicted on Figure 1.26.

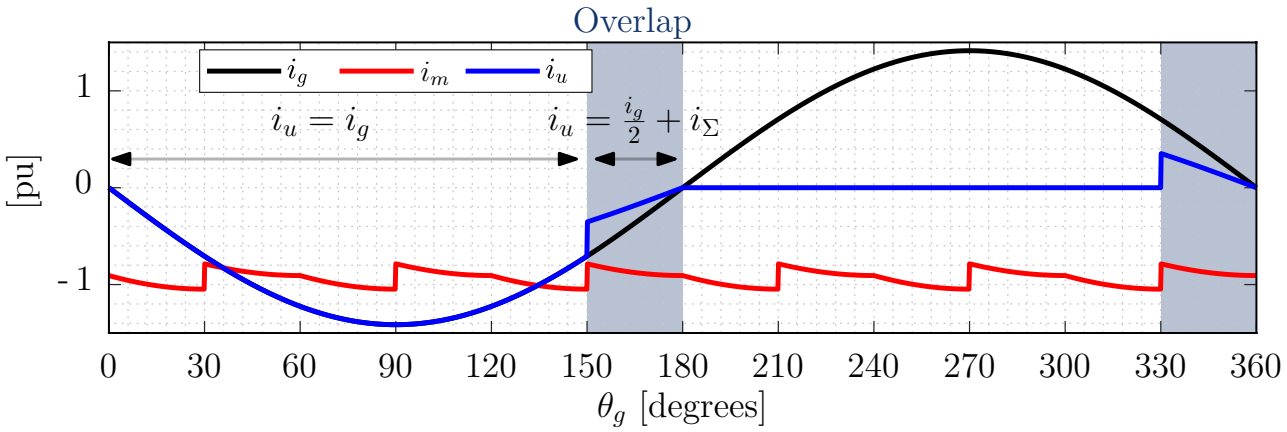


Figure 1.26 – Illustration of i_g,i_m and i_u in case of rectifier operating mode

The changes in the arm current expressions explain the discontinuities observed at each beginning or end of the overlap period. With the chosen set of values, $\theta_{ovl} = 30$ degrees and $\delta = \theta_v = 15$ degrees, these discontinuities appears at the beginning of the overlap period. In some cases, the arm current is still positive at the end of the overlap period and the series connection between the DS and the arm inductor prevents from hard switching. To avoid high voltage spike at the opening, a soft switching procedure is required. So far, different techniques have been presented in [87–91] to achieve a Zero Current Switching (ZCS) of the DSs. With such techniques, the overlap current i_Σ is in charge of two essential functions achieved in a sequential way.

1. During most of the overlap period, the control is in "energy management mode" as in Figure 1.26. i_Σ is equal to (1.60).

2. Before the end of the overlap mode, the control switch to "ZCS mode" in order to set the arm current reference to zero in order to open the arm. The reference for i_Σ is modified.

For HVDC system it is very important to get smooth DC bus current in steady-state. As visible on Figure 1.26, the current i_m is composed of a large six-pulses ripple. This current ripple is made by the AC components in the conducting arm currents and the overlap current. It is not acceptable for an HVDC link to operate with such current oscillations in stead-state, then a filter is needed. Two solutions of DC current filtering exist and discussed below.

1.5.5 Filtering of the DC current

The alternation of the arm current makes the DC current inherently composed of a large six-pulse ripple. As for the AC side, it is possible to suppress DC current harmonics through two approaches: the passive filter or the active filter.

Passive DC current filter

The first solution to absorb the DC current harmonics relies on the LC filter as proposed in [1]. In [92] another type of arrangement is proposed using the DC cable as a part of the filter, however, for the purpose of this section a second-order low pass filter as presented on Figure 1.27 is considered.

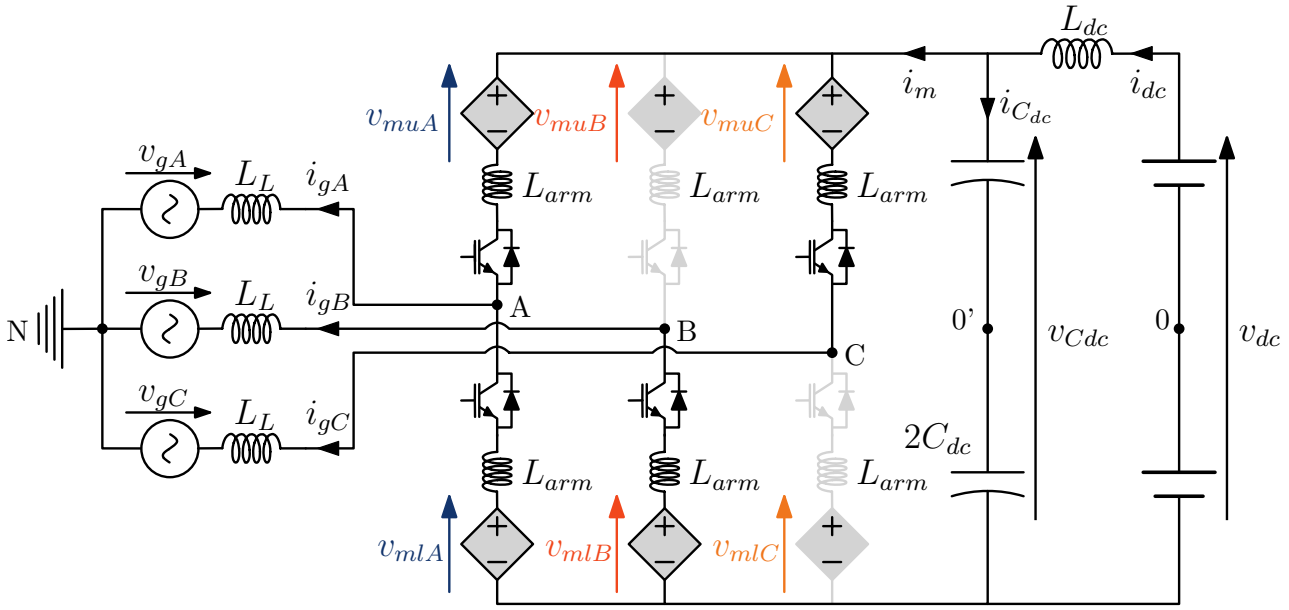


Figure 1.27 – AAC with passive DC filter

Let us introduce i_{Cdc} the current flowing inside the filter capacitor (C_{dc}) and i_{dc} the DC bus current. To keep v_{Cdc}, the voltage across C_{dc} almost constant, in [1] a design of this capacitor is proposed where the energy requirement of this capacitor ($H_{C_{dc}}$) is estimated to 4.4 kJ/MW to maintain the voltage oscillation in the range of ±2.5%. The DC capacitor C_{dc} is obtained according to its energy requirement such as

$$H_{C_{dc}} = \frac{0.5 C_{dc} V_{dc}^2}{P_{dcb}} \rightarrow C_{dc} = \frac{2 H_{Cdc} P_{dcb}}{V_{dc}^2} \tag{1.61}$$

The LC filter is characterised by a second order equation such as:

$$H(\omega) = \frac{1}{1 + \frac{L_{dc}}{R_{dc}} j\omega - L_{dc} C_{dc} \omega^2} \tag{1.62}$$

by using (1.62) and (1.61) the value of the DC reactor according to a desired cut-off frequency is derived

$$L_{dc} = \frac{1}{C_{dc} \omega_0^2} \tag{1.63}$$

According to the converter ratings $C_{dc} = 10\mu$F and by arbitrarily defining ω_0 equals to 628 rad/s (i.e. 100 Hz) it is obtained L_{dc} is 236 mH.

The first graph of Figure 1.28 presents the currents previously defined. The result is a DC bus current i_{dc} almost constant and most of the ripple is flowing inside the capacitors. This current ripple, in return, introduces a six pulse ripple in v_{Cdc}.

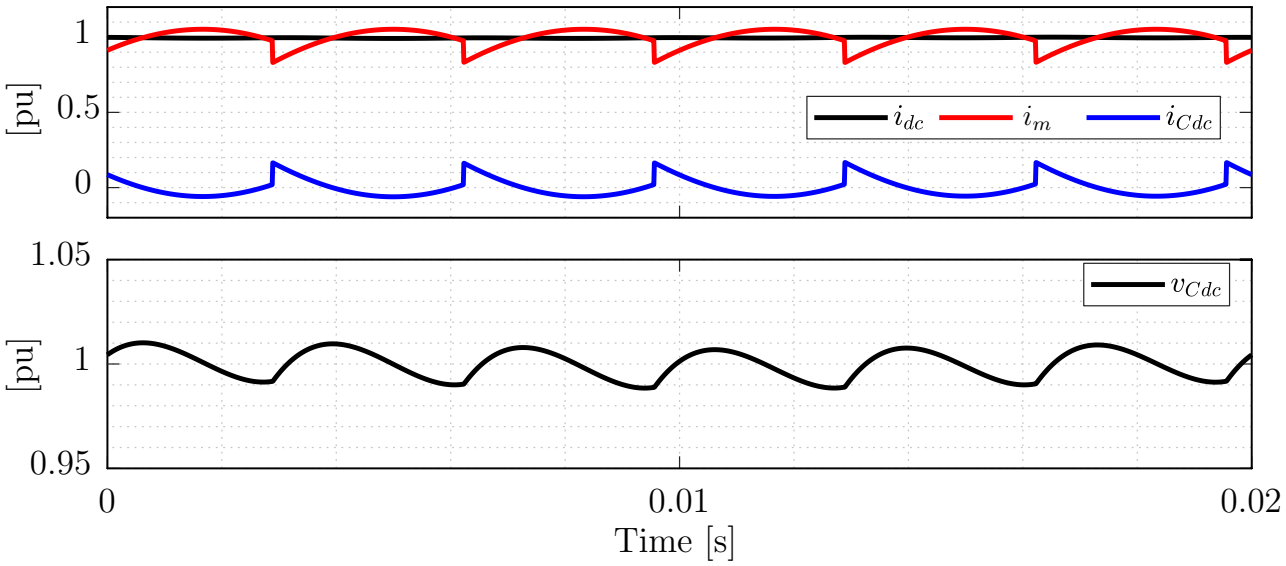


Figure 1.28 – Simulation results of an AAC with passive DC filter

The passive filter allows to get smooth DC current, however, its design is bulky due to low order harmonics. Moreover, it introduces two new states in the system to be controlled to prevent undesired behaviours (e.g. poor damped transient oscillations). However, this topology does not necessitate a large overlap period (typ. less than 30 degrees [92]). The number of additional SMs per stack is therefore low. Considering the case where θ_{ovl} is 30 degrees, by using (1.50) and (1.53) the converter would be approximately designed for at least

$$\begin{aligned} \hat{V}_m &\approx \frac{V_{dc}}{2} + \frac{\hat{V}_v}{4} \approx 0.66 V_{dc} \\ \hat{V}_{DS} &\approx \frac{3}{4}\hat{V}_v \approx 0.48 V_{dc} \end{aligned} \tag{1.64}$$

by assuming $\hat{V}_v$ close to the sweet-spot condition.

The active filter solution presented below has the advantages to avoid the use of such bulky passive filter while performing the same steady-state and better transient behaviours.

Active DC current filter

Fundamentally, the active filtering of the DC current is equivalent to the passive filtering approach since it is based on the insertion of a dedicated path for the current harmonics. It can be created by introducing a modulated current source at the converter output controlled in order to absorb the DC current ripple as drawn on Figure 1.29.

A modulated current source can be built using a modulated voltage source in series with an inductor. By modulating the voltage v_m^{dc}, the current flowing through the parallel branch i_m^{dc} can be controlled to absorb the current ripple at the converter output as in Figure 1.29. However, to avoid an additional dedicated circuit, it is possible to integrate this active filtering function inside the AAC. Indeed, the converter can be divided in two main parts as in Figure 1.30.

- In the green frame, the 2 legs in non-overlap mode + the AC side
- In the blue frame, the leg in overlap mode

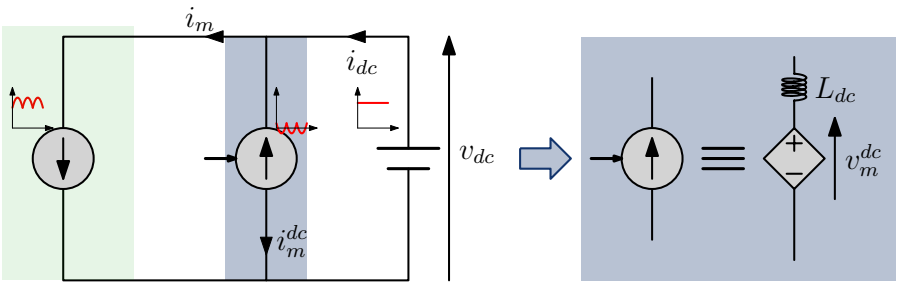


Figure 1.29 – Illustration of the DC current active filter principle

The green part can be modelled by a current source. The blue part, by a single voltage source in series with a inductance (i.e. $2L_{arm}$). Note that the leg A, in overlap mode, is shifted close to the DC side to simplify the understanding.

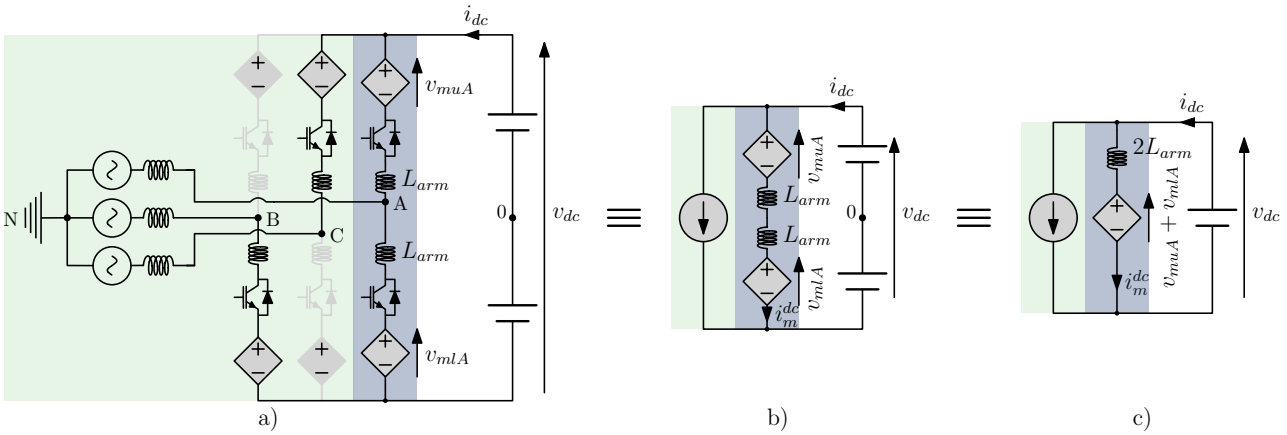


Figure 1.30 – a) Highlight of ripple source (in green) and active filter (in blue) b) DC side equivalent model c) DC side simplified model

The comparison between Figure 1.30 c) and Figure 1.29 shows that the leg in overlap mode can be used as a DC current active filter. This solution avoid using a dedicated circuit to achieve this functionality, for instance, a complete MMC leg, the leg A absorbs the AC components in the DC current coming from the two other conducting arms of leg B and C. Since the overlap mode is distributed among the three legs, thus sequential, while the active filtering functionality must be continuous. This imposes a strong constraint : there must be, at any time, one leg in overlap mode. The overlap mode is activated twice per period which means that if θ_{ovl} is equal to 60 degrees, the constraint is respected. It leads to six different converter states where three of them are presented on Figure 1.31.

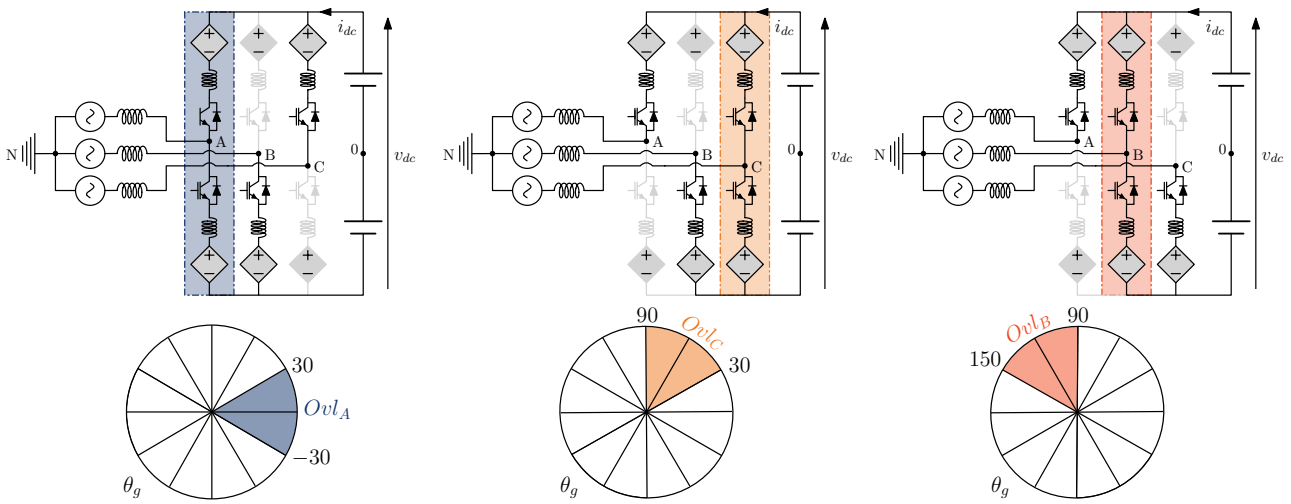


Figure 1.31 – Illustration of three AAC states (over six) in case of a 60 degrees overlap period

Thereby, there is always a path where the DC current ripple can flow in to get a constant DC current. However, this solution can still be improved. As shows Figure 1.31, the equivalent inductance governing the DC side dynamics ($2L_{arm}$) is distributed within the converter arms and activated in a sequential way. The active filtering function being continuous and thanks to the 60 degrees overlap period, the arm inductors can be replaced by a single DC reactor connected on the DC bus. This topology presented on Figure 1.32 is called the Extended Overlap-Alternate Arm Converter (EO-AAC) [71] the latest evolution of the original AAC topology.

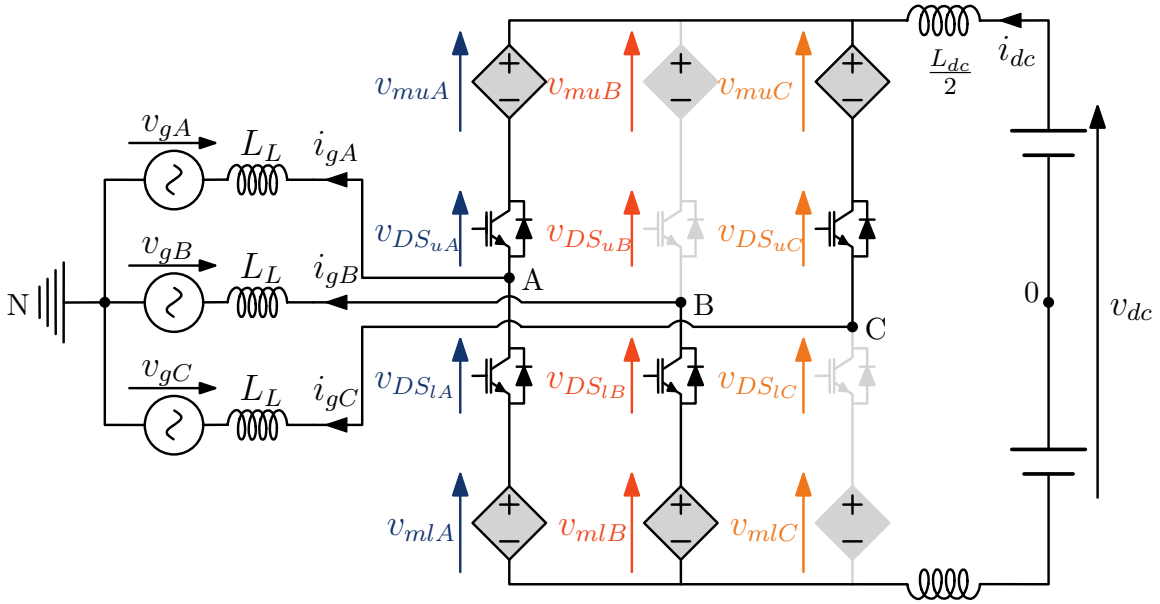


Figure 1.32 – The Extended Overlap Alternate Arm Converter (EO-AAC)

This topology implies two main interesting changes. First of all, the number of explicit inductors has been reduced from six to two. Then, the DSs are no more connected to a current source allowing the hard switching[2].

[2]Soft switching is still preferable from the efficiency point of view but voltage stresses caused current source opening is no more an issue as before.

On the basis of steady-state results, the following current waveforms would be obtained:

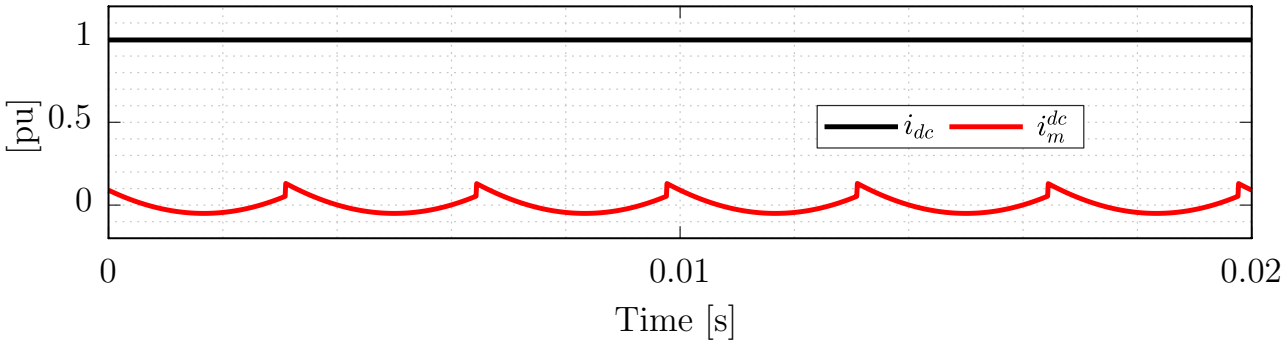


Figure 1.33 – Illustration of i_{dc} and i_m^{dc} of the EO-AAC

Current waveforms presented on Figure 1.33 are particularly similar to those obtained with the passive filter excepted that modulated voltages can provide better transients and oscillations damping that makes the DC current smooth and controllable during transients. However, increasing the overlap period length has increased the need for SMs inside each stack. By using (1.50) and (1.53) and $\theta_{ovl} = 60$ degrees, it is approximately obtained

$$\begin{aligned} \hat{V}_m &= \frac{V_{dc}}{2} + \frac{\hat{V}_v}{2} \approx 0.82 V_{dc} \\ \hat{V}_{DS} &= \frac{1}{2}\hat{V}_v \approx 0.32 V_{dc} \end{aligned} \tag{1.65}$$

which is the minimal EO-AAC design. The number of SMs per EO-AAC stacks will be close to the MMC stacks design (about 18% less), however, one degree of freedom has not been used so far: the Zero Sequence Voltage Injection (ZSVI).

1.6 Chapter Conclusion

This chapter has presented a possible origin of the Alternate Arm Converter.

This topology is made by an assembly of two different types of converters allowing to distribute the DC bus voltage across two different devices: A stack of Sub-Modules (SMs) and a Director Switch (DS). A SM is made of a floating capacitor interfaced through a power electronics device whereas a DS is built from a serial connection of power switches. Thus, compared to topologies like MMC with the same power rating, the introduction of the DSs makes possible to decrease the overall footprint a converter station since DSs take less volume than a stack of SMs.

In the ideal case, it has been demonstrated that half the MMC SM requirement can be achieved, however, the need for SM energy balancing calls for the introduction of an overlap period thus increasing the number of SMs per stack.

Finally, if a DC current active filtering function is desired, then, this overlap period must be extended to 60 degrees providing one of the three converter legs in overlap mode at any time. In the meantime, this extension of the overlap period has led to a simplification of the converter structure since the arm inductors can be replaced by one single DC bus reactor. This topology has been called the Extended Overlap-Alternate Arm Converter (EO-AAC). Despite these improvements, the EO-AAC deceptively exhibits a large number of SMs estimated to more than 80% of the MMC requirement.

Therefore, Chapter 2 will provide a steady-state analysis in order to, first reduce the number of SMs through the injection of zero sequence voltage and then, study the energy requirement and power losses.

Chapter 2

Steady-State Analysis

2.1 Introduction

The steady-state analysis of converters allows determining the sizing equations for any devices. Let us recall the EO-AAC topology with a more complete representation than in the previous chapter.

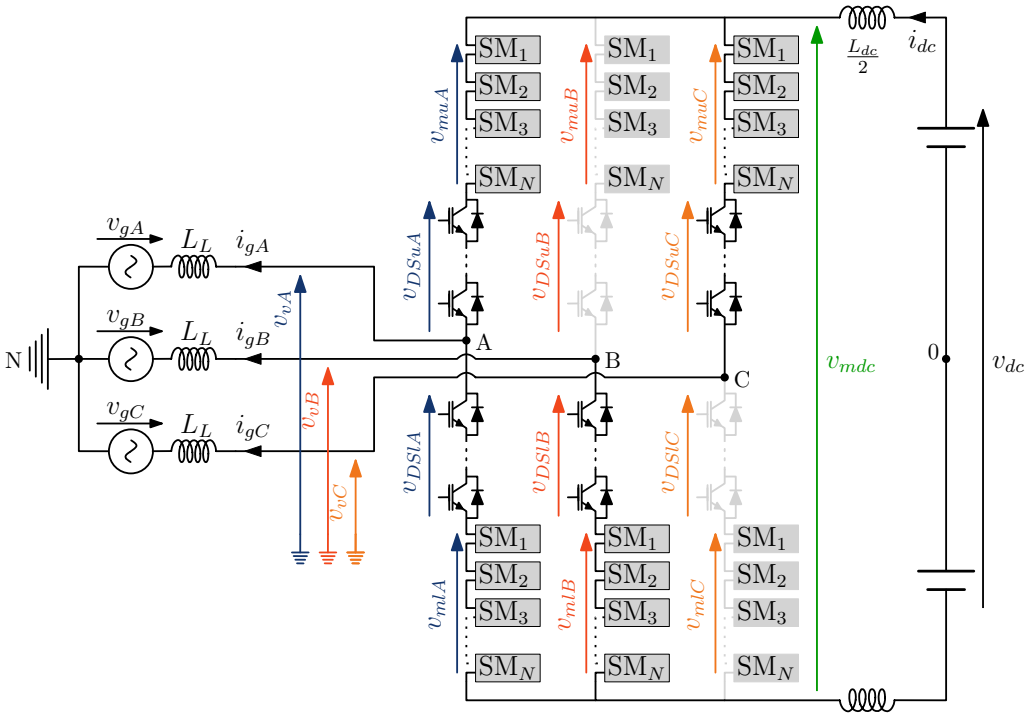


Figure 2.1 – The EO-AAC under a given circuit configuration

In Chapter 1, it has been demonstrated that the extended-overlap period has led to an increase of the SM requirement. In order to decrease this number of SMs per stack, the first part of this chapter is oriented on Zero Sequence Voltage Injection (ZSVI) and its impact on both the $\hat{V}_m$ and $\hat{V}_{DS}$. Moreover, the choice of the SM topologies is demonstrated.

Then, as the SMs interface a capacitor called C_{SM} which is inserted in the current path including AC components, the second part of the chapter details the estimation of the energy requirement used to determine the SM capacitance. This section will provide a comparison between MMC, AAC and EO-AAC under different cases.

Finally, the last part of the chapter is dedicated to the losses estimation study.

2.2 Sizing of Stacks of SMs and DSs including ZSVI

In the previous chapter, it has been demonstrated that an EO-AAC stack of SMs dimensioning is achieved by using

$$\hat{V}_m = \frac{V_{dc}}{2} + \hat{V}_v \sin\left(\frac{\theta_{ovl}}{2}\right) = \frac{V_{dc}}{2} + \frac{\hat{V}_v}{2} \tag{2.1}$$

and the required voltage blocking capability of DS is estimated as it follows:

$$\hat{V}_{DS} = \hat{V}_v \left(1 - \sin\left(\frac{\theta_{ovl}}{2}\right)\right) = \frac{\hat{V}_v}{2} \tag{2.2}$$

but these equations do not consider the use of the Zero Sequence Voltage Injection (ZSVI), i.e. v_{N0}, that may improve the design of the stacks. In this section it is proposed to apply this technique to the EO-AAC as introduced in [93].

To avoid interaction with the active and reactive powers, the fundamental of v_{N0} must be a third harmonic and additional harmonics multiple of three can be added. In this work, the second solution is considered for its simplicity of implementation described by the following equation [94]:

$$v_{N0} = (\min[v_{vj}] + \max[v_{vj}]) \tag{2.3}$$

By using (2.3), the waveform of Figure 2.2 are obtained.

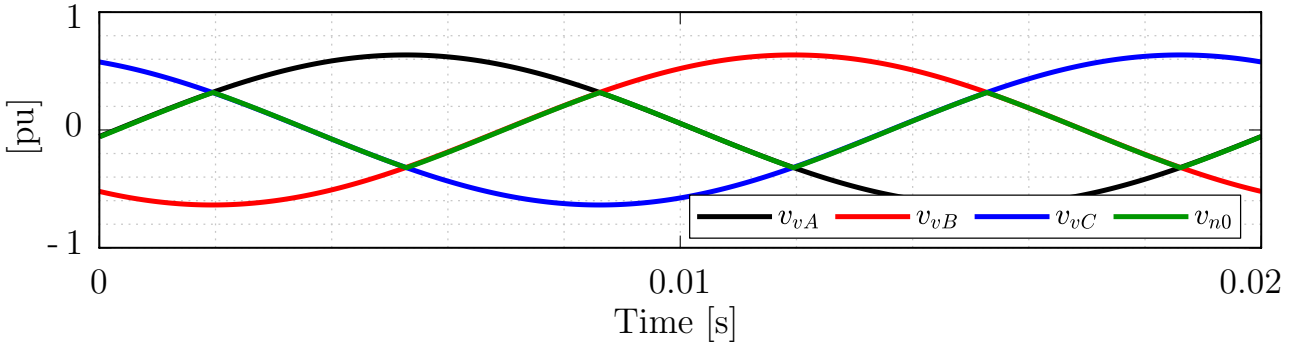


Figure 2.2 – Illustration of v_{N0} using Eq.(2.3)

It results in a triangular waveform, naturally synchronous with v_v and its magnitude is given by:

$$\hat{V}_{N0} = k_{N0} \frac{\hat{V}_v}{2} \tag{2.4}$$

where k_{N0}, as it will be presented in this section, is a coefficient used to vary the injection of zero sequence voltage in modulated voltages.

2.2.1 Modulated voltage peak value estimation according to k_{N0}

According to Figure 2.1, steady-state modulated voltages expression including ZSVI can be expressed as it follows

$$\begin{aligned} v_{mu} &= \frac{V_{dc}}{2} - v_v - v_{N0} \\ v_{ml} &= \frac{V_{dc}}{2} + v_v + v_{N0} \end{aligned} \tag{2.5}$$

in the case where the arm is conducting. In blocked state, modulated voltage are saturated to a constant value minimising $\hat{V}_{DS}$. Figure 2.3 shows v_v,v_{N0} and v_{mu}.

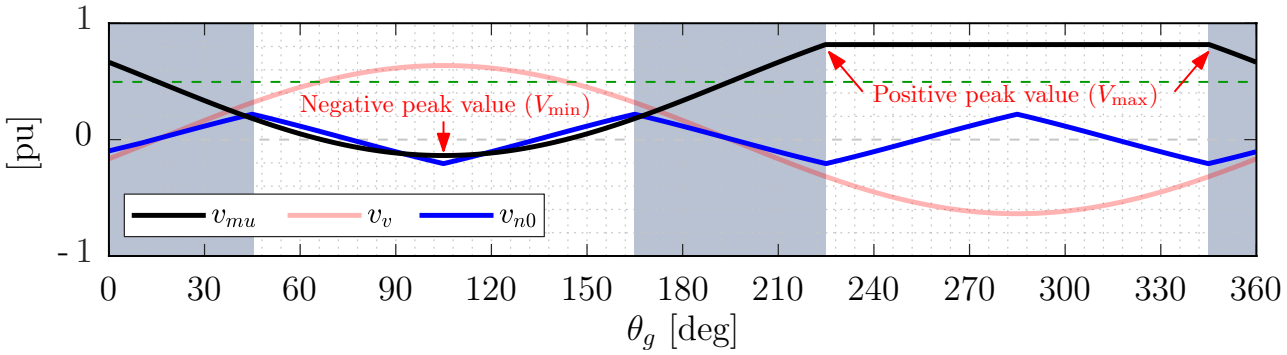


Figure 2.3 – v_{mu} (without ZSVI),v_v and v_{N0}

Chapter 1 has been focused on determining the positive peak value of the modulated voltages and has considered it as the sizing point leading to (2.1). As highlighted on this figure, in modulated voltages there is, indeed, a positive peak value ($V_{\max}$), but also a negative peak value ($V_{\min}$). Each of these values is impacted by the zero sequence voltage in a different way.

According to Figure 2.3, $V_{\max} > |V_{\min}|$ in normal operation, so, to decrease the sizing of the stacks it is needed for v_{N0} to pull down $V_{\max}$. The voltage v_{N0} is minimal (negative peak value) when $V_{\max}$ is reached. Introduce $V_{\max 0}$ and $V_{\min 0}$ the positive and negative peak values of v_m including ZSVI depicted on Figure 2.4.

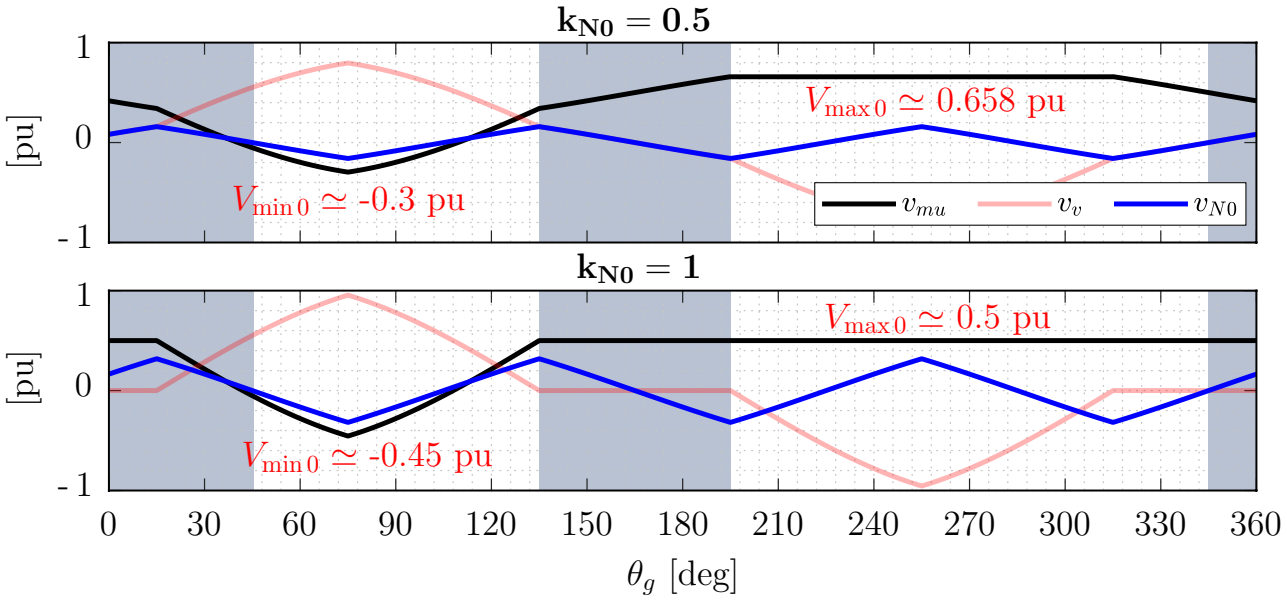


Figure 2.4 – Modulated voltage waveform for different values of k_{N0}

As shown by these last two graphs, increasing k_{N0} reduces the positive peak value of v_m, however, the negative one is increased. However, in normal operation, $V_{\max 0} > |V_{\min 0}|$ for any value of k_{N0}. Thus, an EO-AAC stack is sized for

$$\hat{V}_m = \max\left[V_{\max 0}\,;\,|V_{\min 0}|\right] = V_{\max 0} \tag{2.6}$$

The main effect of the ZSVI is to "flatten" v_v during the overlap period while increasing its peak value. On the right side of each graph there is, indeed, a decreasing of $V_{\max 0}$ down to 0.5 p.u if k_{N0} is equal to 1. This described by the following equations.

$$V_{\max 0} = \underbrace{\frac{V_{dc}}{2} + \frac{\hat{V}_v}{2}}_{V_{\max}} - \hat{V}_{N0} \tag{2.7}$$

and

$$V_{\min 0} = \underbrace{\frac{V_{dc}}{2} - \hat{V}_v}_{V_{\min}} - \hat{V}_{N0} \tag{2.8}$$

In (2.4), it is introduced that $\hat{V}_{N0}$ can be modulated through k_{N0}., then, it is replaced in (2.7)

$$V_{\max 0} = \frac{V_{dc}}{2} + \hat{V}_v \left(\frac{1}{2} - \frac{k_{N0}}{2}\right) \tag{2.9}$$

and

$$V_{\min 0} = \frac{V_{dc}}{2} - \hat{V}_v \left(1 + \frac{k_{N0}}{2}\right) \tag{2.10}$$

From (2.9) and (2.10), it is clearly visible that if k_{N0} is equal to 1 then $V_{\max 0}$ no more includes the AC component v_v as in the case of the AAC without overlap period. For instance, assuming the converter to be connected to a DC bus of 640 kV and $k_{N0} = 1$, stacks would sized for 320 kV meaning a number of SMs (N_{SM}) equals 200 SMs if 1.6 kV SMs technology is used. However, this gain is reported on $V_{\min 0}$. To handle negative voltage some Full Bridge-SMs (FB-SMs) must be incorporated in the stack. Graphically, it can be represented as it follows

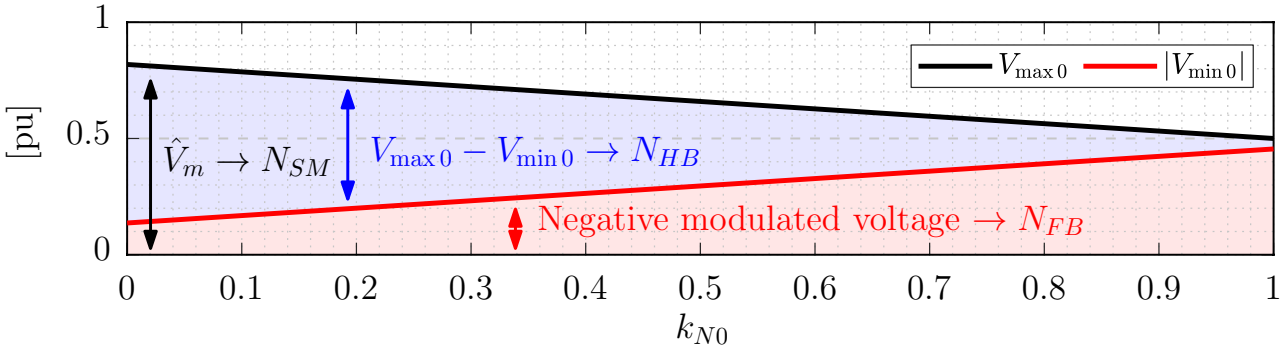


Figure 2.5 – $V_{\max}$ and $V_{\min}$ according to k_{N0}

The number of FB-SMs (N_{FB}) is given by

$$N_{FB} = \left\lceil \frac{|V_{\min 0}|}{V_{SMn}} \right\rceil \tag{2.11}$$

where V_{SMn} is the nominal SM voltage. A FB-SM is capable of generating both positive and negative, so the number of Half-Bridge (HB) SMs is given by

$$N_{HB} = \left\lceil \frac{V_{\max 0} - |V_{\min 0}|}{V_{SMn}} \right\rceil \tag{2.12}$$

Thus, the more the ZSVI is used the more FB-SMs must be used instead of HB-SMs. At a certain point, the ratio between HB and FB SMs becomes so small that the entire stack should be based on FB-SMs.

2.2.2 DS voltage blocking capability according to k_{N0}

As visible on Figure 2.4, the introduction of the ZSVI has increased the peak value of v_v. In Chapter 1, it was reported that the voltage across the DS is determined by the peak value of the AC component as recalled in (2.2). Thus, it can be concluded that reducing the number of SMs per stack, is obtained at the expense of a higher voltage constraint across the DSs. This modification on the DS design is demonstrated based on the next figure which shows v_v, v_{DSu} and v_{N0}.

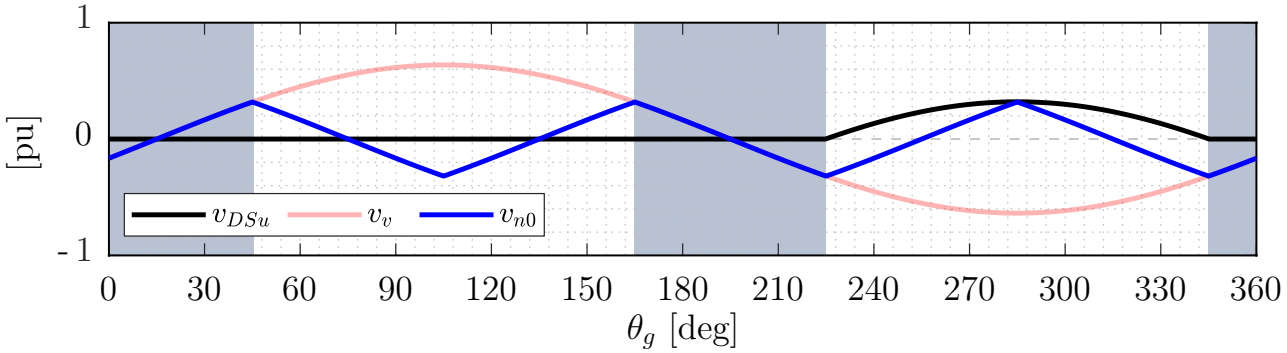


Figure 2.6 – Illustration of v_v, v_{DSu} and v_{N0}

On this figure, the zero sequence voltage is still assumed to follow (2.3). Considering the upper DS opened, then the DC side KVL gives

$$v_{DSu} = V_{dc} - v_{mu} - v_{ml} \tag{2.13}$$

As detailed in Chapter 1, the stack of SMs having its DS open should maximise its voltage in order to minimise the one across the DS. In that case, v_{mu} can be replaced by $V_{\max}$ and v_{ml} by (2.5).

$$v_{DSu} = V_{dc} - \underbrace{V_{\max 0}}_{v_{mu}} - \underbrace{\frac{V_{dc}}{2} - v_v - v_{N0}}_{v_{ml}} \tag{2.14}$$

According to Figure 2.6, the peak value of v_{DSu} is observed when v_v and v_{N0} are maximal.

$$\hat{V}_{DSu} = V_{dc} - \frac{V_{dc}}{2} + \hat{V}_v\left(\frac{1}{2} - \frac{k_{N0}}{2}\right) - \frac{V_{dc}}{2} + \hat{V}_v + \hat{V}_{N0} \tag{2.15}$$

leading to the following generic equation by replacing $\hat{V}_{N0}$ by (2.4)

$$\hat{V}_{DS} = \hat{V}_v\left(\frac{1}{2} + k_{N0}\right) \tag{2.16}$$

As presented by (2.16), the dimensioning of the DS increases faster than the decreasing of stack rating. While $V_{\max 0}$ decreases with a slope governed by $-k_{N0}/2$, $\hat{V}_{DS}$ increases by twice this slope as shown by Figure 2.7.

On the left side of Figure 2.7 is illustrated the DS voltage waveform. If k_{N0} is equal to -1, the rating of the DS is almost the full DC bus voltage (i.e. $3/2\hat{V}_v$) as suggested by (2.16).

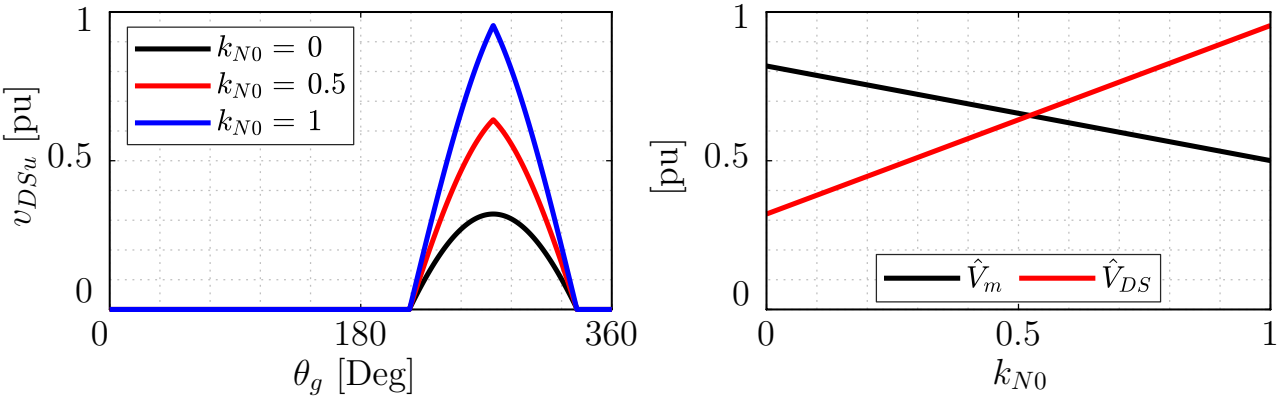


Figure 2.7 – DS voltage waveform and evolution of $\hat{V}_m$ and $\hat{V}_{DS}$ for different values of k_{N0}

2.2.3 DC-Fault Blocking Capability

In addition to its compact design, the EO-AAC has been presented as a DC-Fault tolerant topology unlike HB-MMC. However, the DC-Fault blocking capability requires some constraints on stack design and especially on the SMs topology which are proposed to be discussed in this section. Until now, the EO-AAC stacks are composed of both HB and FB-SMs and the ratio is determined by using $V_{\min 0}$. However, a constraint is missing to have a clear idea on how choosing this ratio between FB and HB SMs. The DC-fault blocking capability case provide a criterion to decide. First of all, let us present the waveform of v_{mu} in case of $v_{dc} = 0$.

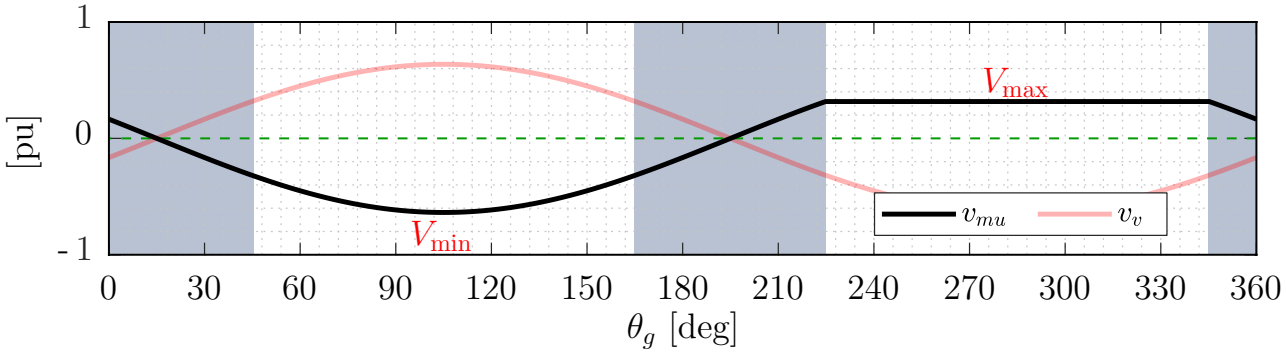


Figure 2.8 – Illustration of v_{muA} in case of pole-to-pole DC-Fault with $v_{N0} = 0$

In that case, by reconsidering (2.9) and (2.9) let us introduce $V_{\max 0-DCF}$ and $V_{\min 0-DCF}$ with DCF for DC-Fault such that

$$\begin{aligned} V_{\max 0-DCF} &= \hat{V}_v \left(\frac{1}{2} - \frac{k_{N0}}{2} \right) \\ V_{\min 0-DCF} &= -\hat{V}_v \left(1 + \frac{k_{N0}}{2} \right) \end{aligned} \tag{2.17}$$

The next figure presents their evolution according to k_{N0} as well as the one of $V_{\max 0}$. This figure shows that depending on the value of k_{N0}, the EO-AAC stacks design ($\hat{V}_m$) is based either on $V_{\max 0}$ for low values of k_{N0} or $V_{\min 0-DCF}$ for high values of k_{N0}. Moreover, it is also visible that the ratio between HB-SMs and FB-SMs (i.e. area in blue and red respectively as in Figure 2.5) becomes very small when considering the DC-Fault blocking capability. As a result, considering stacks entirely composed of FB-SMs might be more simple.

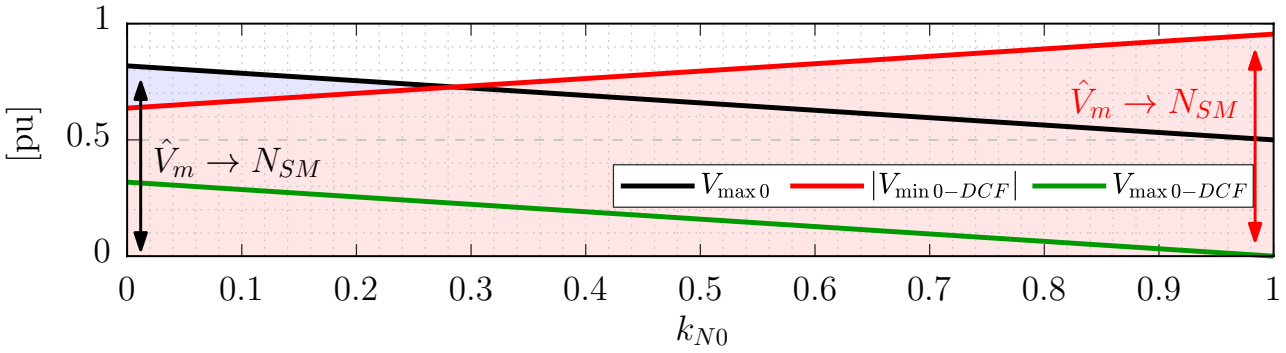


Figure 2.9 – Illustration of $V_{\max 0}$, $V_{\max 0-DCF}$ and $V_{\min 0-DCF}$ according to k_{N0}

2.2.4 Selection of the sizing of the Stacks and DSs

To determine the number of SMs inside each stack for the rest of the thesis, the minimal requirement ensuring the DC-fault blocking capability is considered. According to Figure 2.9, in case of DC-Fault, the most restrictive value is $V_{\min 0-DCF}$. Its minimal value is obtained for $k_{N0} = 0$, then

$$\hat{V}_m = \min\left[V_{\min 0-DCF}\right] = k_{ac}\hat{V}_v \tag{2.18}$$

where k_{ac} is used to met with the grid code requirement providing operating voltage margin constraint on grid connected devices. For the Continental Europe zone, it is required for power generating unit to remain connected between 0.85-1.1 p.u. (on 400 kVac system) for a specified duration. For instance, the range 0.9-1.05 is unlimited in time [95].
Since the number of SMs is fixed as low as possible in case of DC-Fault, it is nonetheless necessary to ensure the normal operation. It means that a value for k_{N0} in normal operation satisfying $V_{\max 0}(k_{N0}) = \hat{V}_m$. By re-arranging (2.9), it is possible to derive the appropriate value of k_{N0}

$$k_{N0} = 1 - \frac{2V_{\max} - V_{dc}}{\hat{V}_v} = 1 - \frac{2\hat{V}_m - V_{dc}}{\hat{V}_v} = 1 - \frac{2k_{ac}\hat{V}_v - V_{dc}}{k_{ac}\hat{V}_v} \tag{2.19}$$

Finally, from the value of $\hat{V}_m$ and k_{N0} the estimation of the DS voltage blocking capability is performed using

$$\hat{V}_{DS} = V_{dc} + \frac{k_{ac}}{2}\hat{V}_v \tag{2.20}$$

Numerical application

Consider V_{dc} =640 kV, $\hat{V}_g = \frac{2}{\pi}V_{dc}$, the AC side impedance of 0.15 p.u. (L_L) and the nominal reactive power (Q_n) of 300 MVAR. From the phasor diagram of Chapter 1, the RMS value of v_v can be derived if we neglect the coupling between M_v and θ_v:

$$V_v = \frac{Q_n X_L + 3V_g^2}{3V_g} \approx 301\text{kV} \tag{2.21}$$

According to the grid code, k_{ac} is equal to 1.1, so the number of SMs is

$$N_{SM} = \left\lceil \frac{k_{ac}\hat{V}_v}{V_{SMn}} \right\rceil \approx \left\lceil \frac{330e3}{1.6e3} \right\rceil \approx 293 \rightarrow 300 \text{ SMs} \tag{2.22}$$

using 1.6 kV SMs. So,

$$\hat{V}_m = 480 \text{ kV} \tag{2.23}$$

Thus, the minimal value of k_{N0} ensuring $V_{\max 0}(k_{N0}) = \hat{V}_m$ can be calculated

$$k_{N0} = 1 - \frac{2\hat{V}_m - V_{dc}}{k_{ac}\hat{V}_v} = 1 - \frac{2 \times 480e3 - 640e3}{468.8e3} \approx 0.32 \tag{2.24}$$

Finally,

$$\hat{V}_{DS} = V_{dc} + \left(\frac{3 - 4k_{ac}}{2}\right)\hat{V}_v = 640e3 + \left(\frac{3 - 4.4}{2}\right)426e3 \approx 380 \text{ kV} \tag{2.25}$$

Validation by simulation

To validate the theoretical approach, a time domain simulation has been performed in the case where the grid experiences an high voltage situation (i.e. k_{ac}=1.1). As in the beginning of this thesis, voltages are displayed according to the DC voltage value. Thus, $\hat{V}_m = 0.75$ p.u. and $\hat{V}_{DS} = 0.6$ p.u.

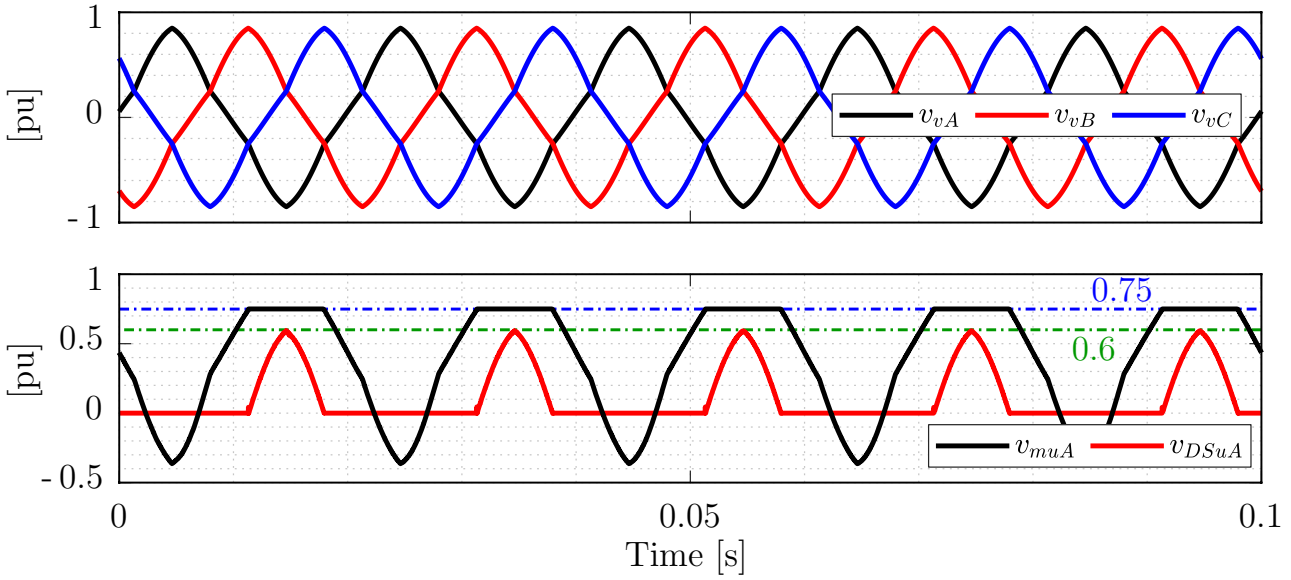


Figure 2.10 – Validation of the chosen EO-AAC design through EMT simulation

As shown by Figure 2.10, at the end of the conduction period of the arm the modulated voltage is saturated to 0.75 p.u. Then, with calculated value of k_{N0}, the observed peak value across the DS is 0.6 p.u.

Nevertheless, it is worth mentioning that such design has been obtained considering the requirement of Continental European zone and the DC-fault blocking capability in case of k_{ac}. Thus, depending of this coefficient stacks design can be lowered.

2.3 Estimation of Internal Energy Storage : Comparison with MMC

One of the most critical part in the design of a modular type converter lies is the sizing of the SM capacitors. In fact, all operations of these converters depend on the voltage provided by the capacitors. The mix between AC and DC components in the arm quantities introduces capacitor voltage oscillations due to the instantaneous power components as highlighted on the next figure.

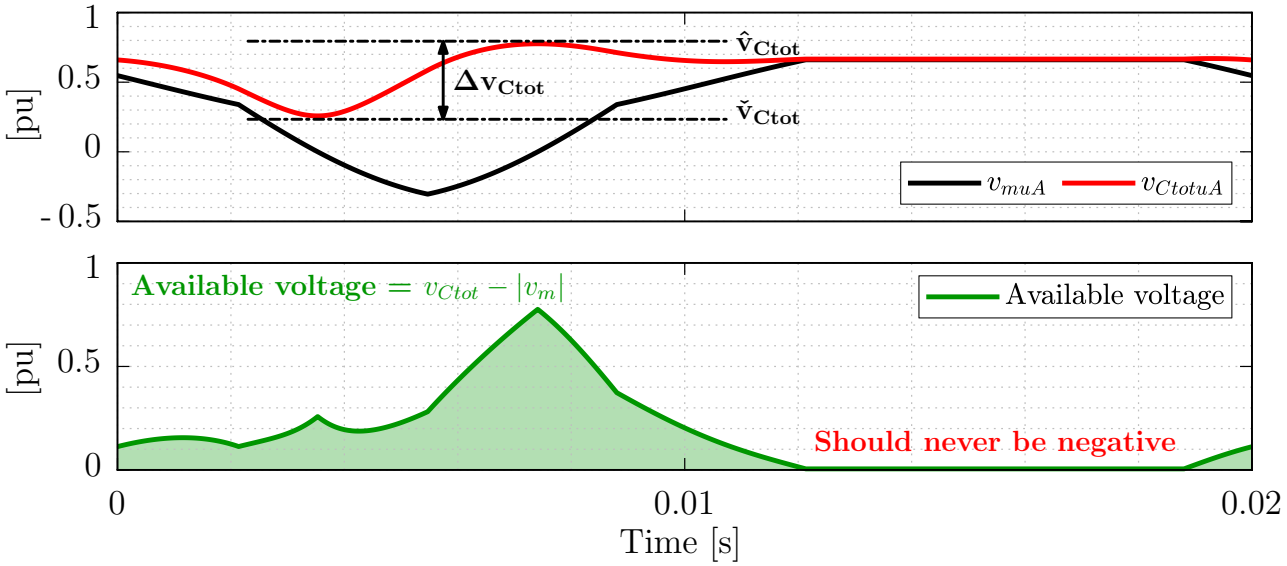


Figure 2.11 – Illustration of v_{CtotuA}, v_{muA} and the voltage availability

In Chapter 1, it has been introduced that a stack of SMs can be modelled using an average stack model that consists in an equivalent chopper interfacing one equivalent capacitor C_{tot}. The first graph of Figure 2.11 shows its voltage (v_{Ctot}) which is likely to vary. To determine the value of this equivalent capacitor, a first method proposed [1] estimates the energy that should be embedded inside each stack to met with a criteria on Δv_{Ctot} defined as $\hat{v}_{Ctot} - \check{v}_{Ctot}$ (i.e. max - min).
A second method [75, 86] treats this problem in a different way since it focuses on the peak value of v_{Ctot} ($\hat{v}_{Ctot}$) and the voltage availability drawn on the second graph which also depends on the average value of v_{Ctot}. The second parameter must satisfy

$$v_m \leq v_{Ctot} \tag{2.26}$$

This method determine the energy requirement on the basis of these two parameters. The final step of this method consists in the derivation of an appropriate energy reference, to modify the average value of v_{Ctot}, that creates a strong dependence between control and converter design. Moreover, it supposes to have a control of the converter's internal energy, which, as seen in the MMC literature over the years is not always the case.

Therefore, in this thesis the first method has been used since the peak-to-peak capacitor voltage oscillation is independent from the control. However, it is important to note that such method does not guarantee voltage availability at any time.

2.3.1 Basics of Stored Energy Requirement Estimation according to Δv_{Ctot} [1]

The instantaneous energy within a stack is defined by

$$w_{Ctot} = \frac{1}{2} C_{tot} v_{Ctot}^2 \tag{2.27}$$

If the average value of v_{Ctot} is assumed to be maintained around its nominal value V_{Ctot0}, then, v_{Ctot} can be expressed as

$$v_{Ctot} = V_{Ctot0} \left(1 + \delta v_{Ctot}\right) \tag{2.28}$$

where δv_{Ctot} is the voltage oscillation introduced by the AC components in the arm quantities. This oscillation is assumed to be evenly distributed around V_{Ctot0}. The above expression can be injected in (2.27) to get

$$w_{Ctot} = \frac{1}{2} C_{tot} V_{Ctot0}^2 \left(1 + \delta v_{Ctot}\right)^2 \tag{2.29}$$

As a result, let us now define $\hat{\delta} w_{Ctot}$ and $\check{\delta} w_{Ctot}$ as

$$\begin{cases} \hat{\delta} w_{Ctot} = \dfrac{1}{2} C_{tot} V_{Ctot0}^2 \left(1 + \delta v_{Ctot}\right)^2 \\ \check{\delta} w_{Ctot} = \dfrac{1}{2} C_{tot} V_{Ctot0}^2 \left(1 - \delta v_{Ctot}\right)^2 \end{cases} \tag{2.30}$$

and $\Delta w_{Ctot} = \hat{\delta} w_{Ctot} - \check{\delta} w_{Ctot}$. It results:

$$\begin{aligned} \Delta w_{Ctot} &= \frac{1}{2} C_{tot} V_{Ctot0}^2 \left(1 + 2\delta v_{Ctot} + \delta v_{Ctot}^2 - 1 + 2\delta v_{Ctot} - \delta v_{Ctot}^2\right) \\ &= \frac{1}{2} C_{tot} V_{Ctot0}^2 4\delta v_{Ctot} \end{aligned} \tag{2.31}$$

At this stage, we are now able to express the energy fluctuation according to the nominal stored energy and allowed capacitor voltage ripple. However, this expression lacks of generality. In this thesis an expression that fits to any converter ratings has been preferred but requires to introduce H_C used to describe the energy requirement. In case of modular type converters, the expression of H_C for any AC/DC converter comprising N stacks is

$$H_C = \frac{N \frac{1}{2} C_{tot} V_{Ctot0}^2}{S_n} \tag{2.32}$$

with S_n the rated power. Thanks the expression of H_C it is possible to replace the expression of C_{tot} in (2.31) to obtain:

$$\Delta w_{Ctot} = \frac{4 H_C S_n \delta v_{Ctot}}{N} \tag{2.33}$$

Thus, for any converter ratings / design (or even topology) we can determine how much energy must be embedded to met with design specifications using the following formulae

$$H_C = \frac{N \Delta w_{Ctot}}{4 S_n \delta v_{Ctot}} \tag{2.34}$$

in kJ/MVA.

As shown by (2.34), the core of this work to determine H_C lies in the derivation of Δw_{Ctot} since all other parameters like δv_{Ctot} are fixed. This energy fluctuation is introduced by instantaneous arm power composed of AC components. The expression of the power through C_{tot} can be written as

$$p_{Ctot} = v_{Ctot} i_{Ctot} = v_m i_{arm} \tag{2.35}$$

under the assumption that the model loss less. Using the above equation, w_{Ctot} can be expressed in a second way such as

$$w_{Ctot} = W_{Ctot} + \delta w_{Ctot} = W_{Ctot} + \int_0^t p_{Ctot}\, dt = W_{Ctot} + \int_0^t v_m i_{arm}\, dt \tag{2.36}$$

In practice after retrieving numerically calculated points, Δw_{Ctot} is determined on the basis of the following equation.

$$\Delta w_{Ctot} = \max\left[\int_0^t v_m i_{arm}\, dt\right] - \min\left[\int_0^t v_m i_{arm}\, dt\right] \tag{2.37}$$

The quantities v_m and i_{arm} must therefore be derived in steady state. As shown in (2.37) this steady-state modelling depends on different parameters as the P_{ac},Q set point and voltages magnitude. Moreover, the control law can be also be involved in steady-state quantity waveform (for instance the ZSVI) and has to be taken into account.

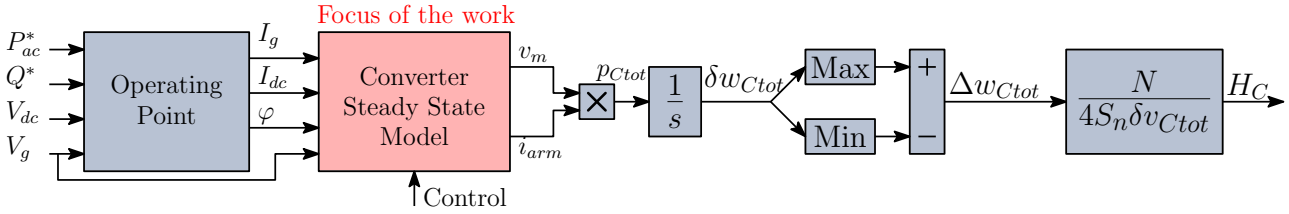


Figure 2.12 – Generic flow-chart for determination of H_C in modular converters

In the following, analytical steady-state models for MMC, AAC (no DC current active filtering) and EO-AAC are developed in order to determine the impact of the different main parameters that are highlighted further. These model are based on the next assumptions:

1. the DC component in modulated voltage is equal to $\frac{V_{dc}}{2}$
2. $v_v = v_g$ meaning the AC side impedance is neglected

2.3.2 Assessment of stored energy requirement in MMC

The MMC energy requirement has been analysed in many different works [96–101] and represents now a kind of standard to which other converters should be compared in order to claim their improvement in terms of energy requirement. According to Chapter 1 and by assuming a single-phased representation leads the following expressions and waveforms of Figure 2.13.

$$\begin{aligned} v_{mu} &= \frac{V_{dc}}{2} - \hat{V}_g \sin(\theta_g) \\ i_u &= \frac{I_{dc}}{3} + \frac{\hat{I}_g}{2} \sin(\theta_g + \varphi) \end{aligned} \tag{2.38}$$

From these descriptions of arm quantities, the power that flows through the MMC capacitors (p_{Ctot}) can be derived.

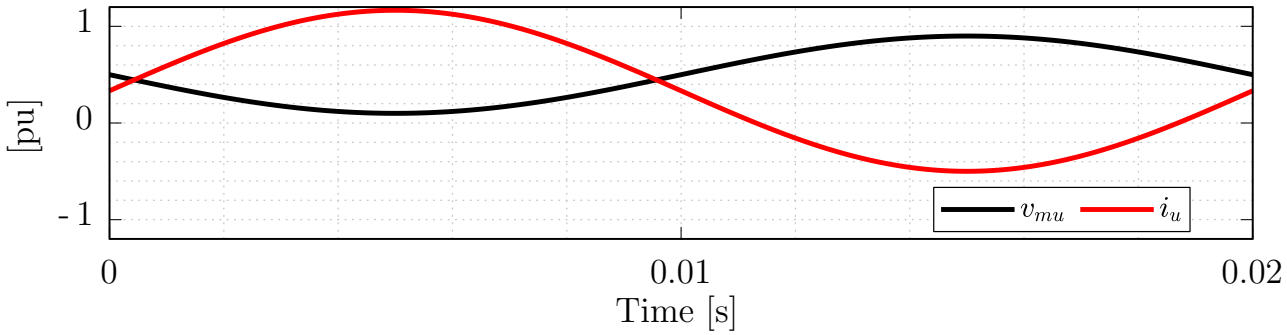


Figure 2.13 – MMC upper modulated voltage and arm current waveforms

$$p_{Ctot} = S\left[\frac{1}{3m}\sin(\theta_g+\varphi)+\frac{1}{6}\cos(2\theta_g+\varphi)-\frac{m}{6}\cos(\varphi)\sin(\theta_g)\right] \tag{2.39}$$

From this basic equation (2.39), where the modulation index m is introduced as well as the apparent power S, parameters to be studied can be determined but also the dominant harmonic in the energy fluctuation.
It seems clear that the load angle φ, the modulation index m and the grid frequency θ_g are highly involved in the power harmonics. The grid frequency is fairly assumed to be fixed since its deviation cannot be large. The only parameters to be studied are φ and m.

It is also interesting to note that, MMC arm power is essentially composed of a fundamental component and a second order harmonic. At low modulation index (e.g. below 1) the fundamental component is the most constraining harmonic. Since the second order harmonic is independent from m, at high modulation index value, this harmonic would become higher than the fundamental component. These observations are visible on Figure 2.14 where the energy fluctuation according to m and H_C according to m and φ are illustrated.

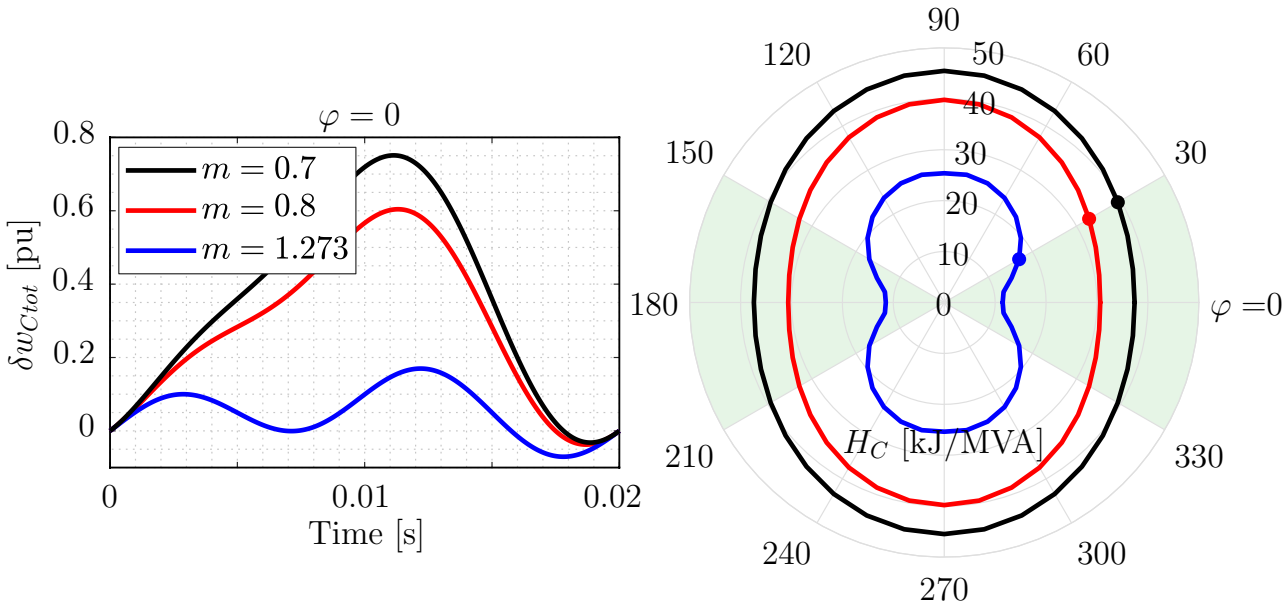


Figure 2.14 – Illustration of MMC stack energy fluctuation ($\varphi = 0$) and H_C in kJ/MVA with pure sinusoidal and DC modulation

The value of H_C depicted by the circles on Figure 2.14 are based on the assumption that the converter operates at its rated power, no matter the load angle. However, in practice an HVDC

converter station is more likely to operate in the range of $\varphi = \pm 30$ degrees (even less) at the rated power. Therefore, the following analyses focus on the area filled in green. The highest values for H_C are obtained when the converter is running with reactive power. This result is explained by the third term of (2.39) which increases the overall fundamental component as long as there is reactive power in the system. On the other hand, increasing the modulation index allows reducing the energy fluctuation.

In case of the most common modulation index value (i.e. $m = 0.8$), H_C is about 33 kJ/MVA to operate in the range of $\varphi = \pm 30$ degrees. The grid code asks for converters to remain connected in case of lower AC voltage, therefore lower modulation index. Considering $m = 0.7$ leads to $H_C \approx 40$ kJ/MVA the well-known values of MMC energy requirement. Finally, assuming the converter operating with $m = 1.273$ (i.e. $4/\pi$ as AACs) reduces the amount of stored energy down to ~17 kJ/MVA. This results highlights the interest of operations at high modulation index since energy fluctuation components at the fundamental frequency are highly decreased.

Validation of MMC steady-state model

In the L2EP Lab, there is an existing 20 SMs per stack HB-MMC prototype which is proposed to be used for the design validation. This small-scale converter embeds 40 J/kVA resulting in SM capacitance of 8 mF. The converter is connected on the DC side to a voltage source of 400 V and the AC side line-to-line voltage is 200 V. Thus, m is equal to 0.816. To validate the theoretical analysis, since H_C is fixed, it is proposed to examine the value Δv_{Ctot} and to compare it to then expected value given by:

$$\Delta v_{Ctot} = \sqrt{\frac{2\Delta w_{Ctot}}{C_{tot}}} \tag{2.40}$$

The results are as it follows.

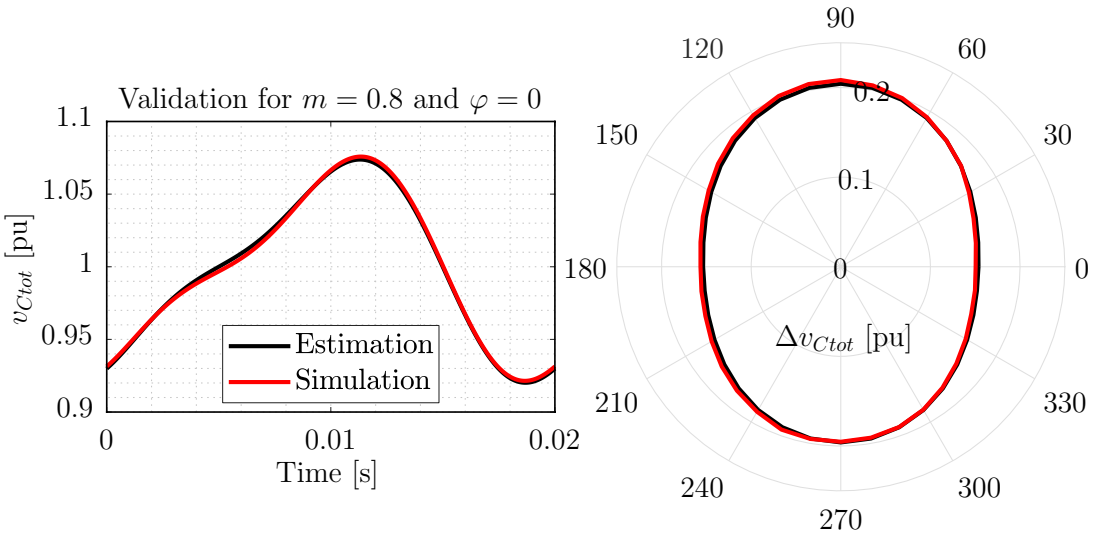


Figure 2.15 – Comparison between theoretical results and simulation for MMC with sinusoidal simulation for $m = 0.8$

The first case is the MMC with sinusoidal modulation as above studied. The first graph of Figure 2.15 shows the waveform of v_{Ctot}, both curves are almost superimposed showing that

analytical can captures the main information with sufficient precision. As a result, Δv_{Ctot} is plotted for all load angle values showing that the criterion is respected.

This model can be updated to take into account changing in the converter's control. For instance, MMC's SM capacitor design has been analysed including different types of control laws. These controls can be summarised as (i) non-sinusoidal modulation through ZSVI and (ii) circulating current injection (CCI) at twice the grid frequency [102–106].

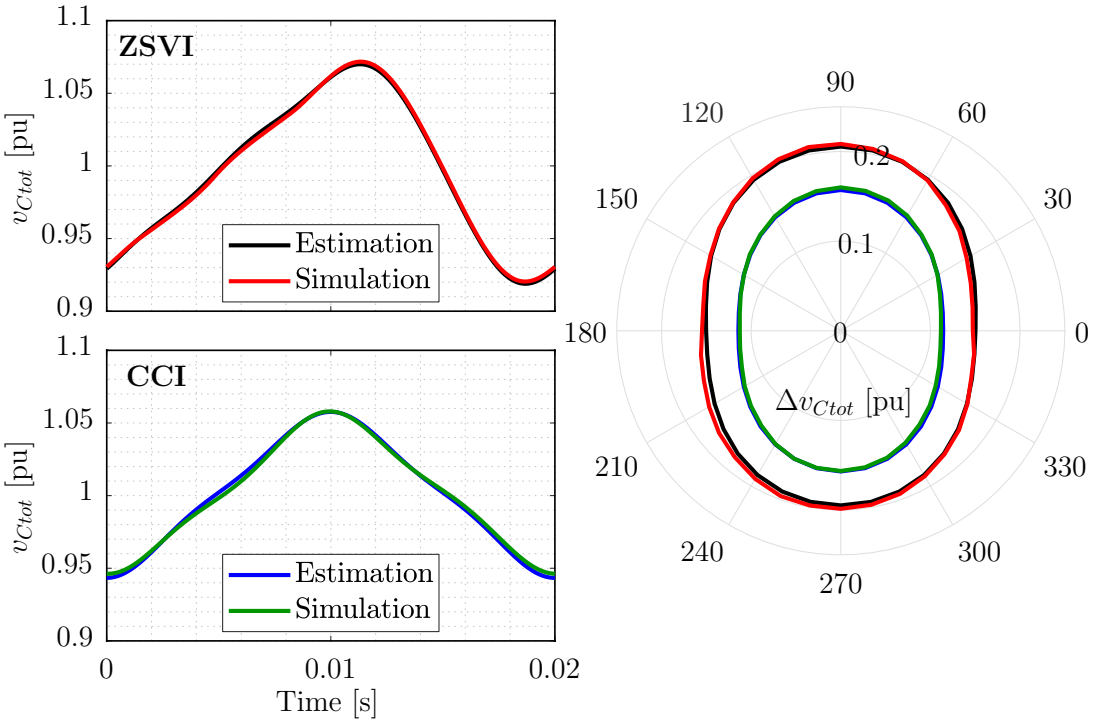


Figure 2.16 – Comparison between theoretical results and simulation for MMC with ZSVI and CCI for $m = 0.8$

To highlight the impact of these voltage and current harmonic injection and more generally the impact of the control, steady-state models have been derived and compared to the EMT simulation on Figure 2.16. The steady-state modelling reproduces with fidelity v_{Ctot} and $\Delta_{v_{Ctot}}$. There are minor differences coming the different assumptions in the model, but in overall the main information is well captured.

From this figure, it is interesting to note that the ZSVI does not involve a modification on the value of H_C derived on the basis of Δv_{Ctot}. On the other hand, when using CCI there is a real positive impact on $\Delta_{v_{Ctot}}$. In this case, H_C can be decreased by almost 25% compared to the basic MMC result.

2.3.3 Assessment of stored energy requirement in AAC

The short MMC study has provided the fundamentals of energy requirement estimation according to the different degrees of freedom in the models. The AAC requires the same kind of derivation, however, according to the state of the DSs, the expression of the arm current varies, and by extension the power through the stack as well. This can be summed up by the following four intervals where v_v is still assumed to be equal to v_g.

$$\begin{cases} \text{Interval 1: } \theta_g \in \left[-\dfrac{\theta_{ovl}}{2}; \dfrac{\theta_{ovl}}{2}\right] \text{ Overlap mode} \\ \text{Interval 2: } \theta_g \in \left[\dfrac{\theta_{ovl}}{2}; \pi - \dfrac{\theta_{ovl}}{2}\right] \text{ Non-overlap mode} \\ \text{Interval 3: } \theta_g \in \left[\pi - \dfrac{\theta_{ovl}}{2}; \pi + \dfrac{\theta_{ovl}}{2}\right] \text{ Overlap mode} \\ \text{Interval 4: } \theta_g \in \left[\pi + \dfrac{\theta_{ovl}}{2}; -\dfrac{\theta_{ovl}}{2}\right] \text{ Blocked mode} \end{cases}$$

In order to have a complete overview of the energy requirement in AACs, different cases are presented as stated below.

- AAC with a Short Overlap (SO-AAC)
- AAC with an Extended-Overlap period without DC current active filtering
- EO-AAC

However, due to the complex operation of AACs requiring to derive power expressions in both non-overlap and overlap modes, the following subsections do not display derivations which are provided in Appendix B.

Energy requirement in SO-AAC

Let us first assume a converter leg in **Non-overlap mode** and the upper arm conducting. The upper modulated voltage and arm current are defined as:

$$\begin{aligned} v_{mu} &= \frac{V_{dc}}{2} - \hat{V}_g \sin(\theta_g) \\ i_u &= \hat{I}_g \sin(\theta_g + \varphi) \end{aligned} \tag{2.41}$$

Once the leg goes into **Overlap mode**, a similar MMC behaviour is observed. Half of the AC current is flowing through the upper arm as well as a DC component i_Σ used to balance the converter internal energy. Under such consideration it is obtained

$$i_u = i_\Sigma + \frac{\hat{I}_g}{2} \sin(\theta_g + \varphi) \tag{2.42}$$

v_{mu} remains the same.

In Chapter 1, the steady-state expression of i_Σ was provided including the magnitude of v_v as well as its angle. It recalled here:

$$i_\Sigma = I_g \left(-\frac{1}{\sqrt{2}\pi} \cos(\delta + \varphi) \cos\left(\frac{\theta_{ovl}}{2} + \varphi\right) + \frac{V_v}{2v_{dc}} \cos(\theta_v - \varphi) \right) \left(\frac{\pi}{\theta_{ovl}}\right) \tag{2.43}$$

However, thanks to the assumption that $v_v = v_g$ a simplified expression can be derived as it follows:

$$i_\Sigma = \frac{m I_g \cos(\varphi)}{2\sqrt{2}} \left(-\frac{4}{m\pi} \cos\left(\frac{\theta_{ovl}}{2}\right) + 1 \right) \left(\frac{\pi}{\theta_{ovl}}\right) \tag{2.44}$$

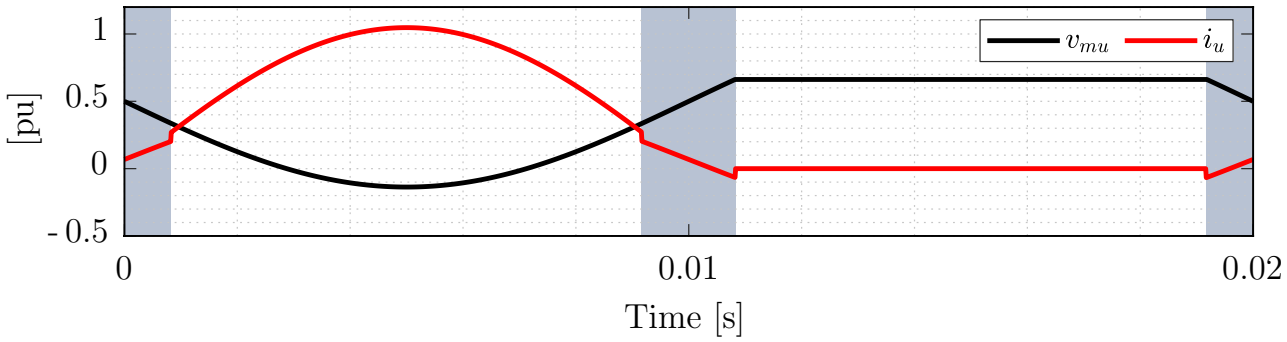


Figure 2.17 – Illustration of v_{mu} and i_u for $\theta_{ovl} = 30$ degrees

where the only parameters that are involved are, the modulation index, the load angle and the overlap period. Through these expressions of modulated voltage and arm current their waveform are illustrated as it follows.

The changing of arm current expression between non-overlap and overlap modes is highly visible. During the non-overlap mode, the current i_Σ is constant in steady-state explaining this linear waveform of i_u.

Since modulated voltage and arm current expressions are similar to the MMC ones, it can be deduced that parameters impacting the value of H_C in AACs are φ and m. Due to the existence of the sweet-spot it is consider a deviation of $\pm 10\%$ for m which has for nominal value $4/\pi$ (1.273). Results of energy fluctuation waveform and H_C estimation are provided on Figure 2.18 where θ_{ovl} is set to 30 degrees.

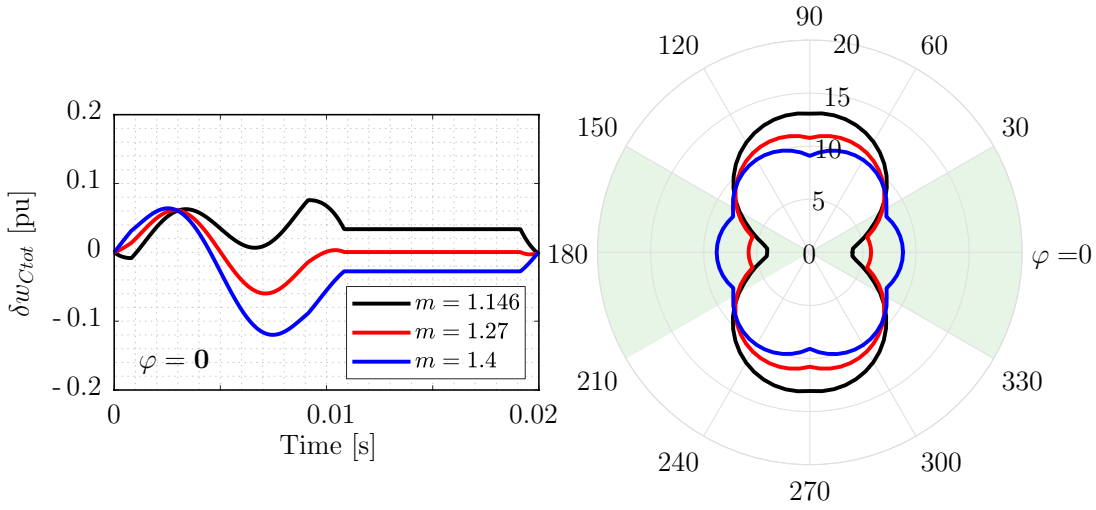


Figure 2.18 – Illustration of AAC stack energy fluctuation ($\varphi = 0$) and H_C in kJ/MVA with $\theta_{ovl} = 30$ degrees

Interestingly, it can be noticed that SO-AACs capacitor voltages must absorb a very small harmonics at the fundamental frequency. Indeed, as introduced in the MMC study, the fundamental component decrease with m while the second order harmonic remains constant. It explains the waveforms exposed on Figure 2.18 essentially containing oscillations at twice the fundamental.

On the other hand, the impact of both φ and m seems to be coupled. Let us have a look at the H_C curves. It is visible that for $m = 4/\pi$ the energy requirement increases with the load angle, the same for low modulation index. If m is increased then it becomes the impact of φ

becomes less clear since the curve is horizontally stretched.

However, thanks to its high modulation index and reduced arm conduction period, SM capacitors experiences reduced energy fluctuation allowing to relax their design compared to the MMC. As a results, the SO-AAC needs less than 10 kJ/MVA to achieve ±10% of capacitor voltage oscillation in the range of $\varphi = \pm 30$ degrees at the rated power.

Energy requirement in AAC with an Extended Overlap period (No DC current active filter)

Now, let us consider an overlap angle of 60 degrees. Modulated voltage and arm current has not changed, only the overlap mode has been extended. The waveforms are as it follows

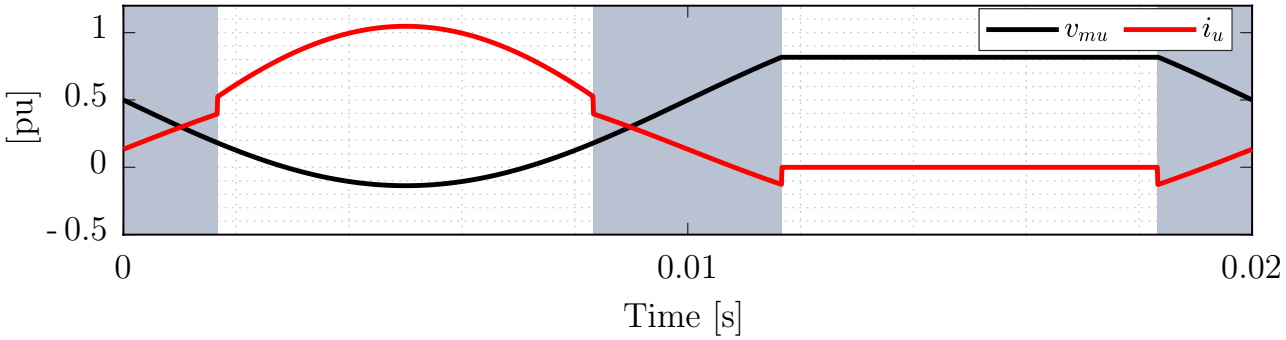


Figure 2.19 – Illustration of v_{mu} and i_u for $\theta_{ovl} = 60$ degrees

Considering these waveforms leads to Figure 2.20.

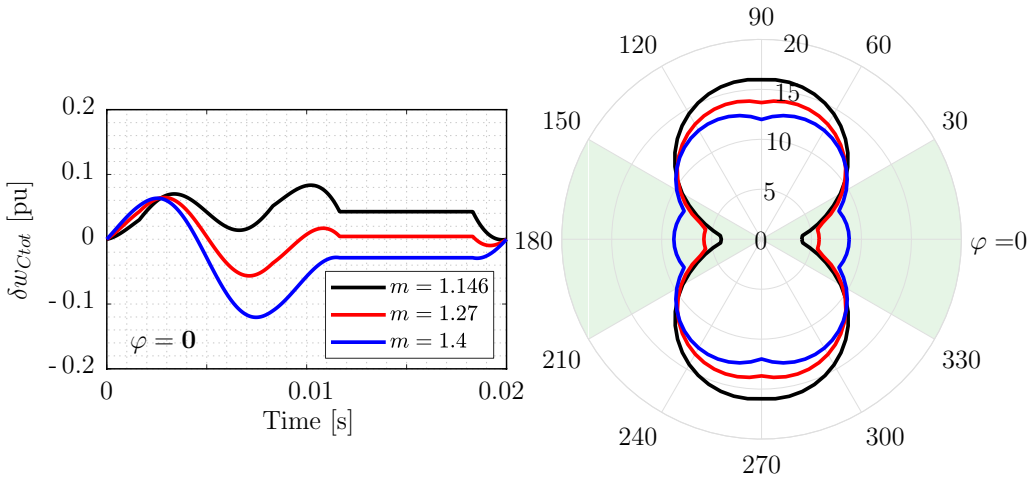


Figure 2.20 – Illustration of AAC stack energy fluctuation ($\varphi = 0$) and H_C in kJ/MVA with $\theta_{ovl} = 60$ degrees

Increasing the overlap angle and therefore the arm conduction period has led to an increase of the energy fluctuation and hence H_C. This increasing is essentially attributed to the fact that the power is integrated over a longer period. At low load angle, H_C seems to be not really impacted as it remains almost unchanged. However, exchanging reactive power clearly impact the value of H_C. In overall and for all modulation index value, an increase of 2.5 kJ/MVA must be considered when using extended overlap period but without DC current active filter.

Energy requirement in EO-AAC

The previous section has given the key figures about the energy in AAC without active filtering of the DC current. In this part, the energy is analysed in case of the EO-AAC meaning that the DC current is actively filtered by the converter. This active filtering function involves a changing in the arm current expression and waveform since the current ripple is absorbed by the leg in overlap mode.
In this case, the current i_Σ is more constant in steady-state. According to Figure 2.1

$$\begin{aligned} i_{dc} &= \frac{i_{uA}+i_{lA}}{2}+\frac{i_{lB}}{2}+\frac{i_{uC}}{2} \\ &= i_{\Sigma A}-\frac{\hat{I}_{gB}}{2}\sin\left(\omega t+\frac{2\pi}{3}+\varphi\right)+\frac{\hat{I}_{gC}}{2}\sin\left(\omega t-\frac{2\pi}{3}+\varphi\right) \end{aligned} \tag{2.45}$$

From (2.45) the expression of the overlap current in leg A, if the AC side currents are balanced, is derived

$$i_{\Sigma A} = I_g\left(\frac{3m\cos(\varphi)}{2\sqrt{2}}\pm\frac{\sqrt{3}}{\sqrt{2}}\cos(\omega t+\varphi)\right) \tag{2.46}$$

and leads to Figure 2.21.

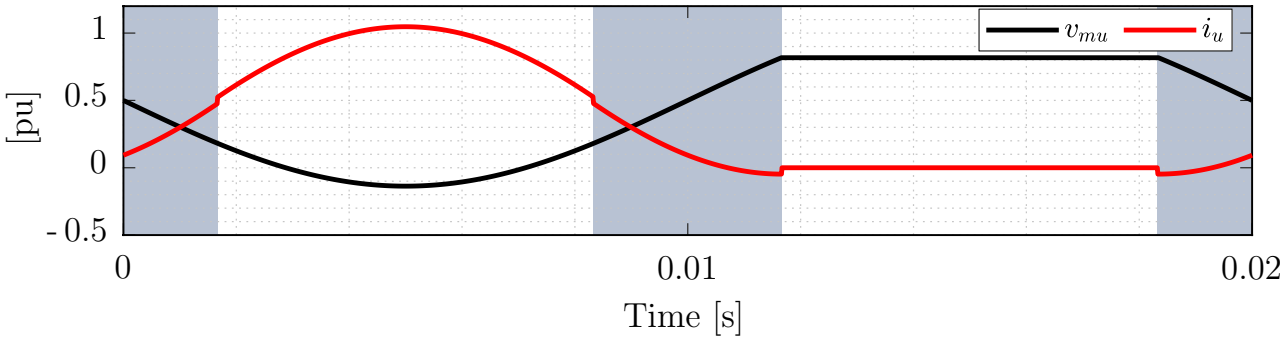


Figure 2.21 – Illustration of v_{mu} and i_u in EO-AAC

The harmonic introduced by this control technique in the arm current is a piecewise fundamental component. The impact of this component is now highlighted on Figure 2.22.

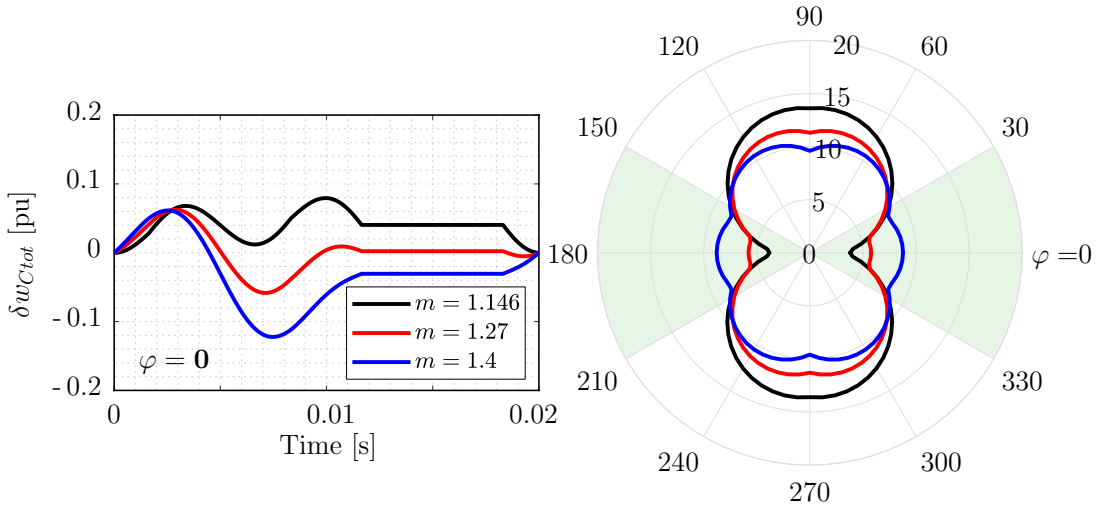


Figure 2.22 – Illustration of EO-AAC stack energy fluctuation ($\varphi = 0$) and H_C in kJ/MVA

The energy fluctuation waveform has not significantly changed compared to Figure 2.18. The energy fluctuation remains essentially composed of a second order. However, the combination of the overlap length increasing and the absorption of the DC current ripple makes the energy requirement the same as the SO-AAC with $\theta_{ovl} = 30$ degrees. Thus, compared to the previous case where θ_{ovl} was equal to 60 degrees, the value of H_C has been reduced.

To highlight this gain, these three cases a depicted on Figure 2.23. As visible on this figure, there is indeed a reduction of the energy fluctuation occurring at high load angle value. Thus, the active filtering control almost cancel the increasing introduced by the extended overlap period.

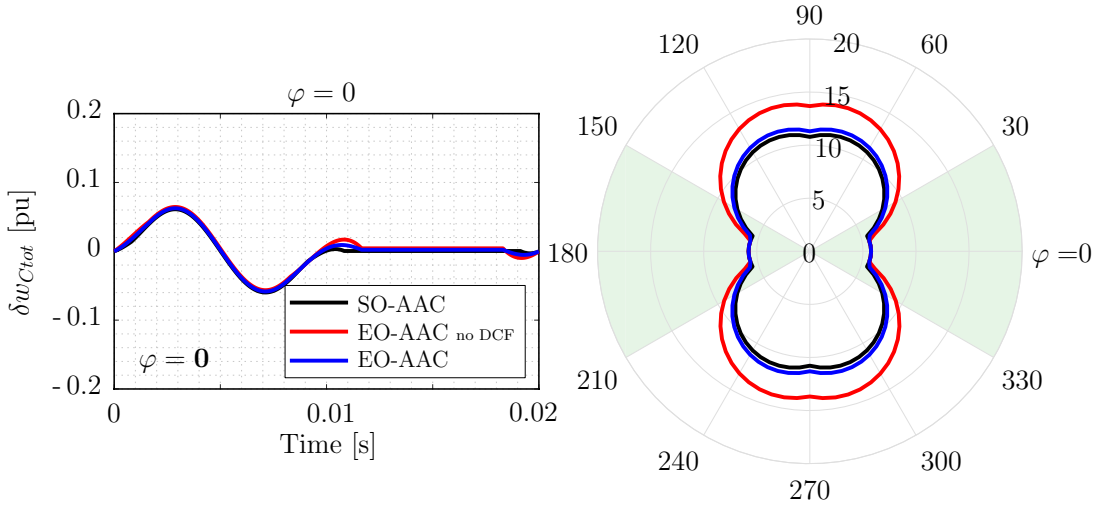


Figure 2.23 – Comparison between SO-AAC, EO-AAC without DC current active filter and EO-AAC

In summary, the EO-AAC allows removing of a bulky passive filter without increasing the required amount of energy when compared to the SO-AAC. However, as highlighted in the active power devices sizing section, to be really competitive, the EO-AAC should reduce its SM requirement, so the injection of zero sequence voltage must be analysed.

EO-AAC with ZSVI

The use of the ZSVI modifies the modulated voltage expression. We can write for both operating modes

$$v_{mu} = \frac{V_{dc}}{2} - \hat{V}_g \sin(\theta_g) - k_{N0} v_{N0}(\theta_g) \tag{2.47}$$

the arm current expressions remain the same. The following waveforms are obtained.

The introduction of the ZSVI in the modulated voltages increases the energy fluctuation and therefore H_C. This increasing of δw_{Ctot} derives from the interaction between the zero sequence voltage and the grid current. This interaction leads to a second order harmonic higher than the case without ZSVI. For $\varphi = 0$, H_C is almost multiplied by three if $k_{N0} = 1$ (from ∼5 to ∼15 kJ/MVA) while for $\varphi = \pm = 30$ degrees, it is multiplied by two. So, the ZSVI has a very high impact on the energy requirement if the converter is not running with reactive power.

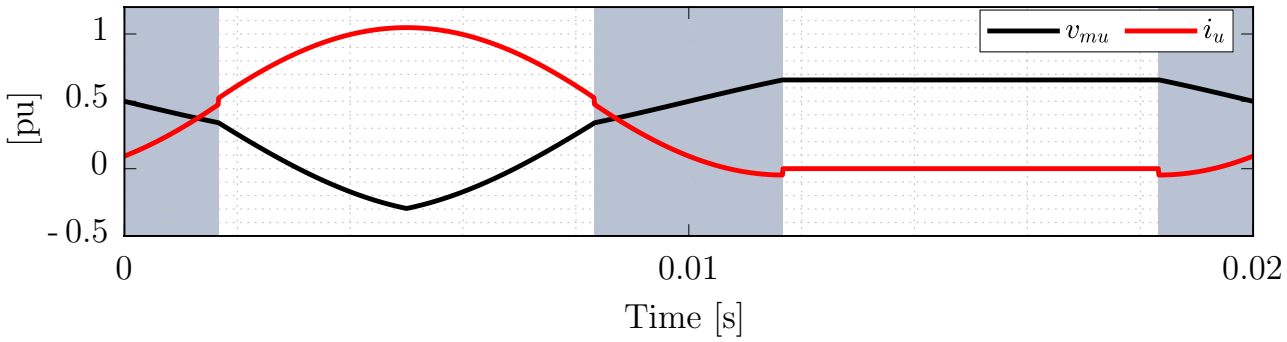


Figure 2.24 – Illustration of v_{mu} and i_u in EO-AAC for $k_{N0} = 0.5$

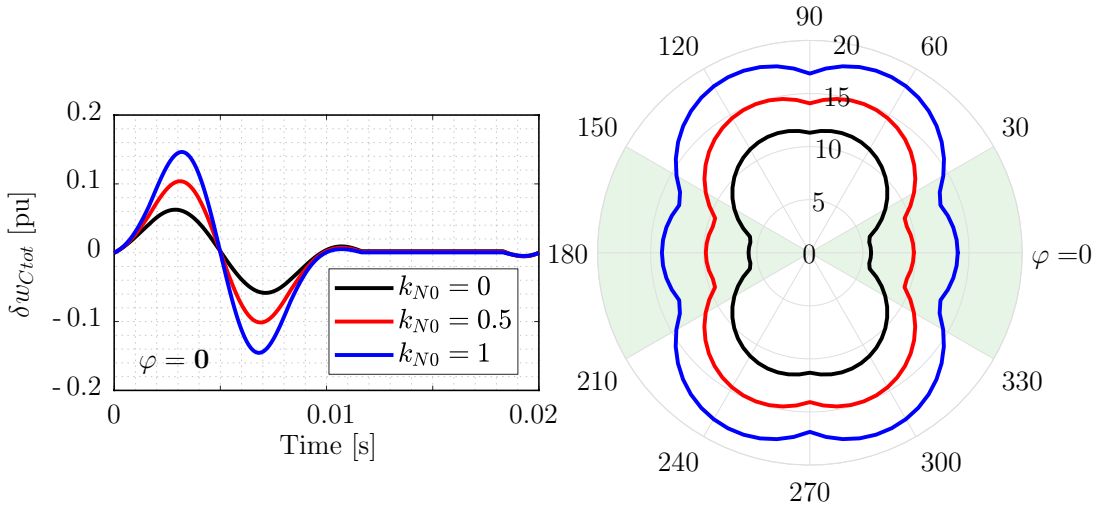


Figure 2.25 – Illustration of EO-AAC stack energy fluctuation ($\varphi = 0$) and H_C in kJ/MVA for different values of k_{N0} and $m = 4/\pi$

Validation of the EO-AAC study

Now, the estimation of the energy requirement is proposed to be validated. As for the MMC, the value of H_C has been fixed to retrieve Δv_{Ctot}. It is set to 15 kJ/MVA in order to operate in any cases (high value of k_{N0} and deviation of the modulation index). Results focus on $k_{N0} = 0$ and 0.5.

Figure 2.26 presents on the left graph v_{Ctot} where the upper graph is for $k_{N0} = 0$ while the second one is for 0.5. In both cases, the estimation using the steady-state modelling match with the simulation. Regarding the values of Δv_{Ctot} the constraint of $\pm 10\%$ is respected showing precision of the model. There are some differences, especially at load angle value, coming from the AC side impedance that has been neglected in the model.

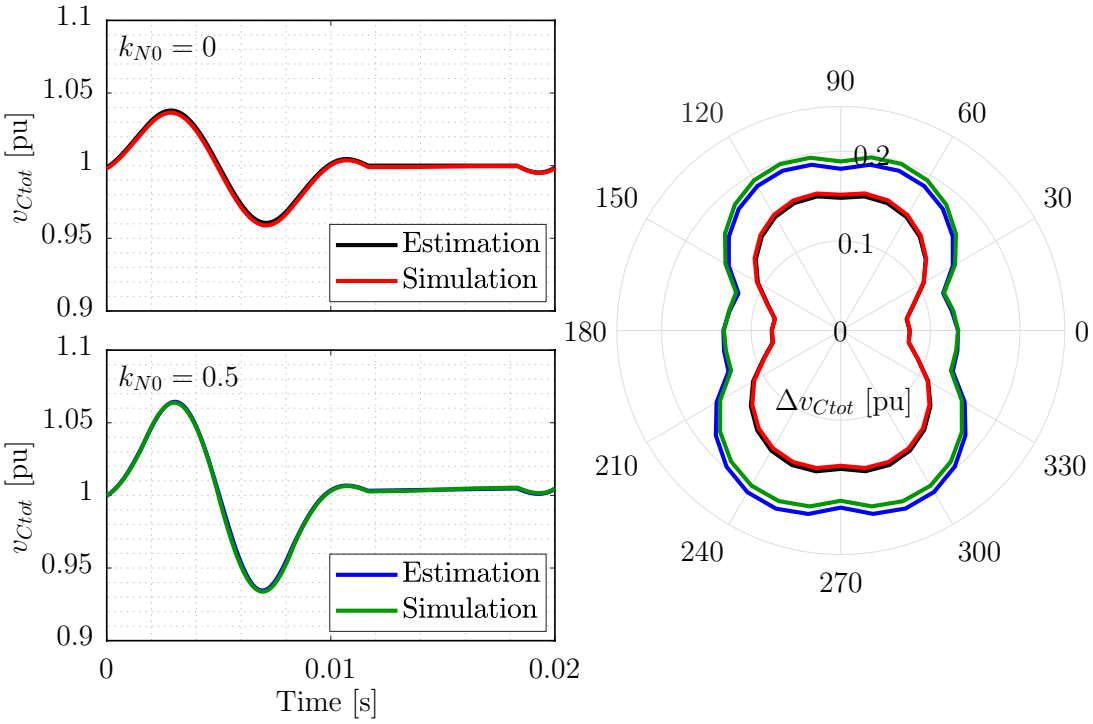


Figure 2.26 – Comparison between theoretical results and simulation for EO-AAC without and with ZSVI and $m = 4/\pi$

2.3.4 Sub-Module Capacitance Selection

In the previous section, the number of SMs (300) as well as the value of k_{N0} (0.32) have been derived according to some constraints in case of DC fault. In this section, the appropriate value of H_C to achieve operation at rated power for $\varphi = \pm 30$ degrees, 10% of modulation index deviation and ZSVI is calculated. The results is depicted on Figure 2.27.

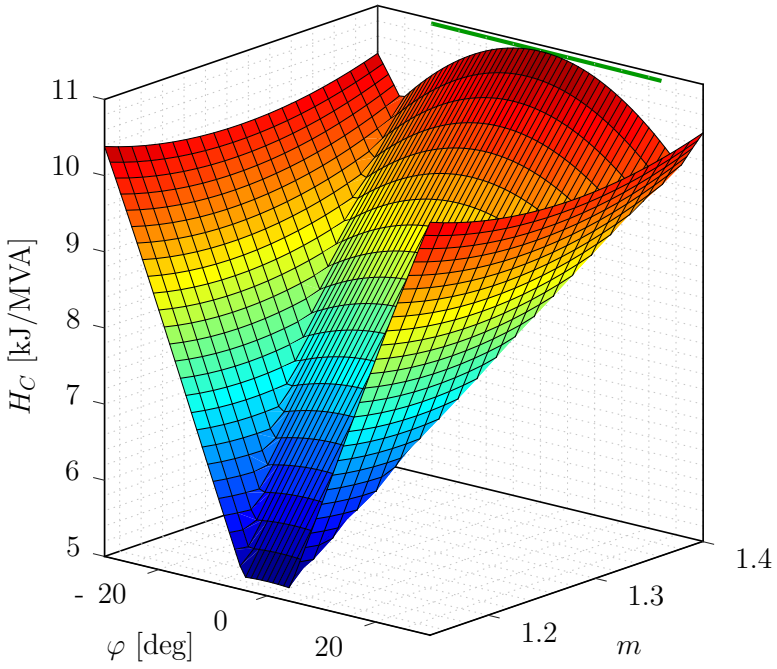


Figure 2.27 – Value of H_C according to $m \in [0.9; 1.1] \times 4/\pi$, $\varphi \in \pm 30$ degrees and k_{N0}=0.3

As visible on this figure, the critical case is the operation with $\varphi = 0$ and $m = 1.4$ as highlighted by the green line. In that case, the value of H_C should be at least 11 kJ/MVA. To determine the minimal value of the SM capacitance, let us first recall

$$H_C = \frac{N_{stack} \frac{1}{2} C_{tot} V_{Ctot0}^2}{S_n} \tag{2.48}$$

with

$$\begin{aligned} C_{tot} &= \frac{C_{SM}}{N_{SM}} \\ V_{Ctot0} &= N_{SM} V_{SMn} \end{aligned} \tag{2.49}$$

Combining these equations leads to

$$C_{SM} \geq \frac{2 H_C S_n}{N_{stack} N_{SM} V_{SMn}^2} \tag{2.50}$$

the converter that is studied in this thesis has equivalent power ratings than MMC of the INELFE link, about 1 GW and 300 MVAR. It yields

$$C_{SM} \geq \frac{0.011 \times 1.044e9}{3 \times 300 \times 1600^2} \geq 5 \text{ mF} \tag{2.51}$$

Finally, an EMT simulation has been performed using this minimal energy requirement. The simulation parameters are $\varphi = 0$ and $m = 1.4$.

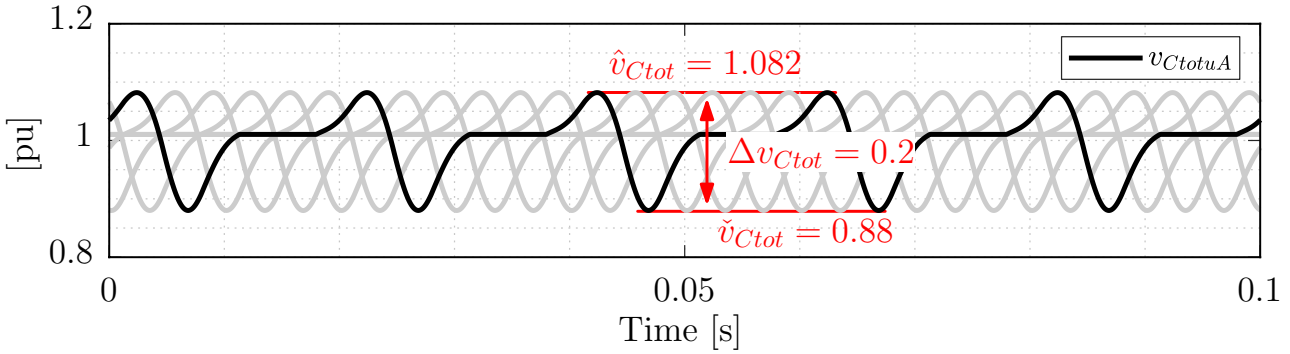


Figure 2.28 – Validation of the minimal SM capacitance estimation

The result provided on Figure 2.28 highlights the precision of the analytical modelling of the power flowing the EO-AAC stacks.

2.3.5 Conclusion on energy requirement analysis

To conclude this section on energy requirement in AC/DC converters, it has been highlighted that parameters like the modulation index, the load angle are highly involved in the SM capacitor voltage oscillations. Control laws achieving harmonic injection in the arm quantities are degrees of freedom that may be use to reduce, in some cases, the energy requirement.

Thanks to its high modulation index, AACs in general exhibit lower SM capacitance ($\geq$ 5 mF for the EO-AAC) compared to MMC (about 13.5 mF for H_C=40 kJ/MVA) which, in addition to its reduced number of SMs, allows decreasing the volume of the HVDC converter station. Finally, the EO-AAC topology is featuring both low energy requirement and passive

DC filter removal. It may results in a very compact design. The use of the ZSVI mitigate this point, but nonetheless the value of H_C remains low.

It is also important to note that, the results that are presented in this section are valid for the criterion of the peak-to-peak energy. Considering the constraint of the voltage availability, the results would be different especially in case of "STATCOM" mode when the converter only exchanges reactive power and requires to increase V_v. However, the required reactive power capability for grid connected converter being as a fraction of the active one (about 30%), the difference between these two approaches may not be significant.

2.4 Losses Estimation In Modular Converters

In conventional converters, the losses estimation can be achieved in a fully analytical way. For instance, a PWM based 2-Level topology has its switching frequency fixed rendering a priori derivation of the switching instances possible. Thus, conduction and switching losses can be estimated according to formulae. In HVDC modular converters, achieving losses study using equations reveals to be (i) complex and (ii) not precise since the switching pattern of the SMs cannot be pre-determined and the switching frequency not fixed. As a consequence, computer aided and simulation based losses estimation is a valuable solution to deal with the operations of such converters where switching instances are not predictable. However, such methods can be time consuming. In this thesis, an hybrid method combining a priori knowledge of the converter and simulation has been used.

2.4.1 Description of Stacks Operation and Switching Pattern of SMs

To understand the reason why the estimation of losses in stack of SMs is challenging to achieve with precision in an analytical way, this section slightly went back to the functioning of these devices. This short presentation is independent from the SM topology and can be considered as a generic observation.

First of all, let us consider the EO-AAC modulated voltage generated by a stack comprising 5 SMs. For the sake of simplicity the SM capacitor has a huge capacitance. This assumption involves a constant voltage equals to the nominal one (V_{Csm0}). In that case, the SM insertion index (n) time function is given by

$$n(t) = \text{round}\left(\frac{v_m(t)}{V_{Csm0}}\right) \tag{2.52}$$

and represented on Figure 2.29.

From this assumption, the isolation of the main switching instances [107] can be determined based on a linear approximation highlighted by the red dashed line on the first graph of Figure 2.29. This linear approximation makes possible to get $\Delta n/\Delta t$ allowing the derivation of the switching instances. The control signals of each SM are illustrated on the right side of Figure 2.29.

However, once the SM capacitors are selected according to the previous section, their voltages are no more constant and extra switching occurs to balance the energy deviation of each SM in a such way that all these voltages are kept in closed range. This function is commonly called Voltage Balancing Algorithm (VBA) [108–110]. This algorithm is therefore out of any physical consideration and difficult to model with equations as well as the dispersion between

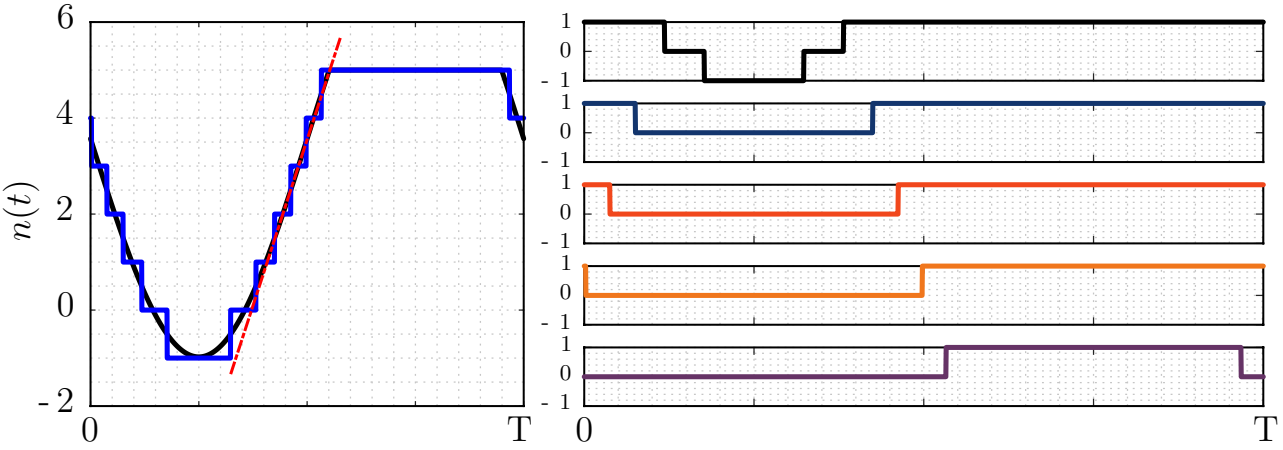


Figure 2.29 – Illustration of a stack switching pattern including infinite SM capacitance

SMs. Thus, by including the VBA and appropriate SM capacitance value, the insertion index function becomes

$$n(t) = \text{round}\left(N_{SM} \times \frac{v_m(t)}{v_{Ctot}(t)}\right) \tag{2.53}$$

The control signals G of i^{th} SM becomes as a function of

$$G_i(t, n, v_{Csmi}, i_{arm}, ...) = [-1; 0; 1] \tag{2.54}$$

Leading to a modified switching pattern illustrated on Figure 2.30

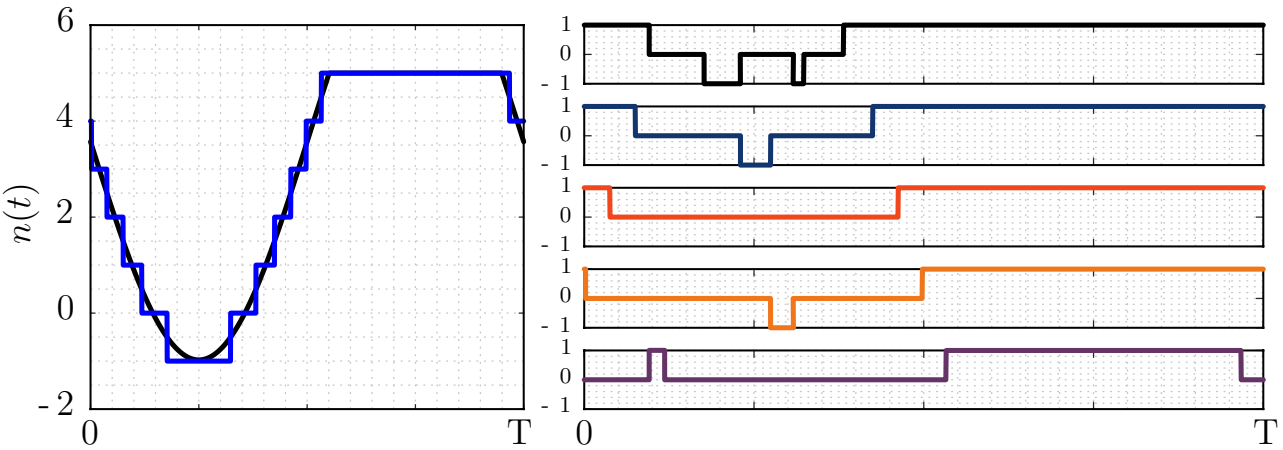


Figure 2.30 – Illustration of a stack switching pattern including adapted SM capacitance and BCA

As shows Figure 2.30, even if the time function of n has not been modified, because of the power that flows through SM capacitors, the VBA has to keep all SM capacitor voltages in certain range and therefore modify the original switching pattern of the stack. It results that, a higher switching frequency than Figure 2.29.

As a consequence, it is easily conceivable that describing the losses in modular converters using analytical description is very difficult due to this algorithm and requires the use of, at least, a simulation including one stack and one CBA.

2.4.2 Losses Estimation Methodology

The estimation of the losses in such complex converter should always comes with a questioning about the use of these analyses. Designing a real system or prototype including the cooling system requires hybrid electro-thermal model to estimate junction, case and heat-sink temperatures to avoid potential underestimation. On the other hand, studying the impact of different controls or modulation schemes may not requires complex models. In that sense, and because the aim of this thesis was not to design a real prototype, the choice of a simplified model is justified.

The estimation of losses in the MMC has been widely covered in the literature according to different methods. In [111, 112] junction temperature has been considered to get precise results or as in [113] to highlight the difference of utilization between SMs explaining differences in terms of temperature. On the opposite side [107,112,114] present analytic estimations and [115] confirms the lack of precision on switching losses. Between these approaches, there are simulation of converters assuming either constant junction temperature or linear $v(i)$ characteristics of devices to compute losses from a detailed time domain simulation as in [116]. These methods feature precision in the estimation of the switching pattern but reveal to be long.

In this work, an hybrid method combining a priori knowledge and time domain simulation has been used to get fast estimation. So far, the steady-state model of the converter has proven its precision in terms voltage across devices and energy fluctuation. This method therefore relies on the use of a coded steady-state model of the EO-AAC to get arm quantities. It allows to skip the use of detailed time domain simulation of the whole converter but to keep only the essential ones : one stack and VBA simulation. The interest of doing losses estimation in that way is (i) the great reduction of the computation time of each iteration and (ii) the extended use of the different models that have been derived. The method's flowchart is illustrated on Figure 2.31.

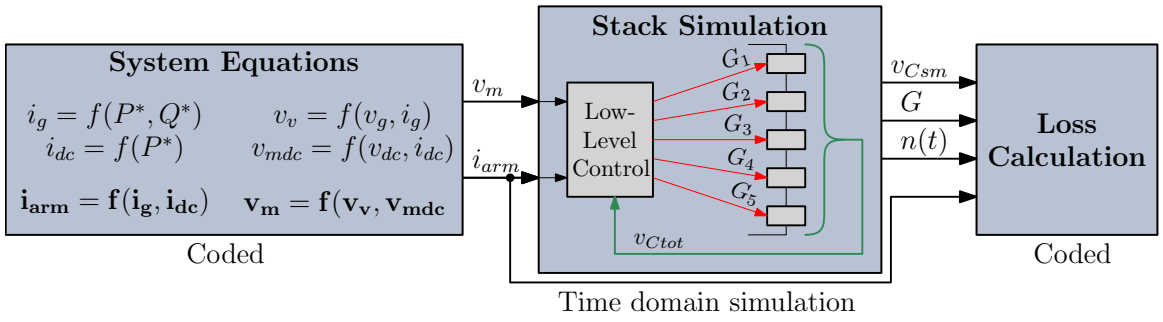


Figure 2.31 – Flow-Chart of losses estimation method

Comparison between full EMT simulation and the proposed hybrid analytic-time domain simulation on stack quantities

To guarantee an acceptable level of precision, the proposed method is compared to a detailed simulation of the EO-AAC. The elements that are compared are

- the modulated voltage and arm current waveforms
- the SM capacitor voltages as well as v_{Ctot}
- and the switching frequency distribution among each SM and the average one.

A first figure resume the comparison between both models in terms of electrical quantities waveforms. This is shown on Figure 2.32. This figure shows first the insertion index function, both curves almost perfectly match. The amplitude is the same, the angle is well reproduced. Then, v_{Ctot} is presented on the second graph, the two curves are almost superimposed. Finally, the upper arm current of leg 'A' is presented and as the other quantities it is well captured. This test case was not considering the ZSVI, this is just an option of the model which would not change the accuracy.

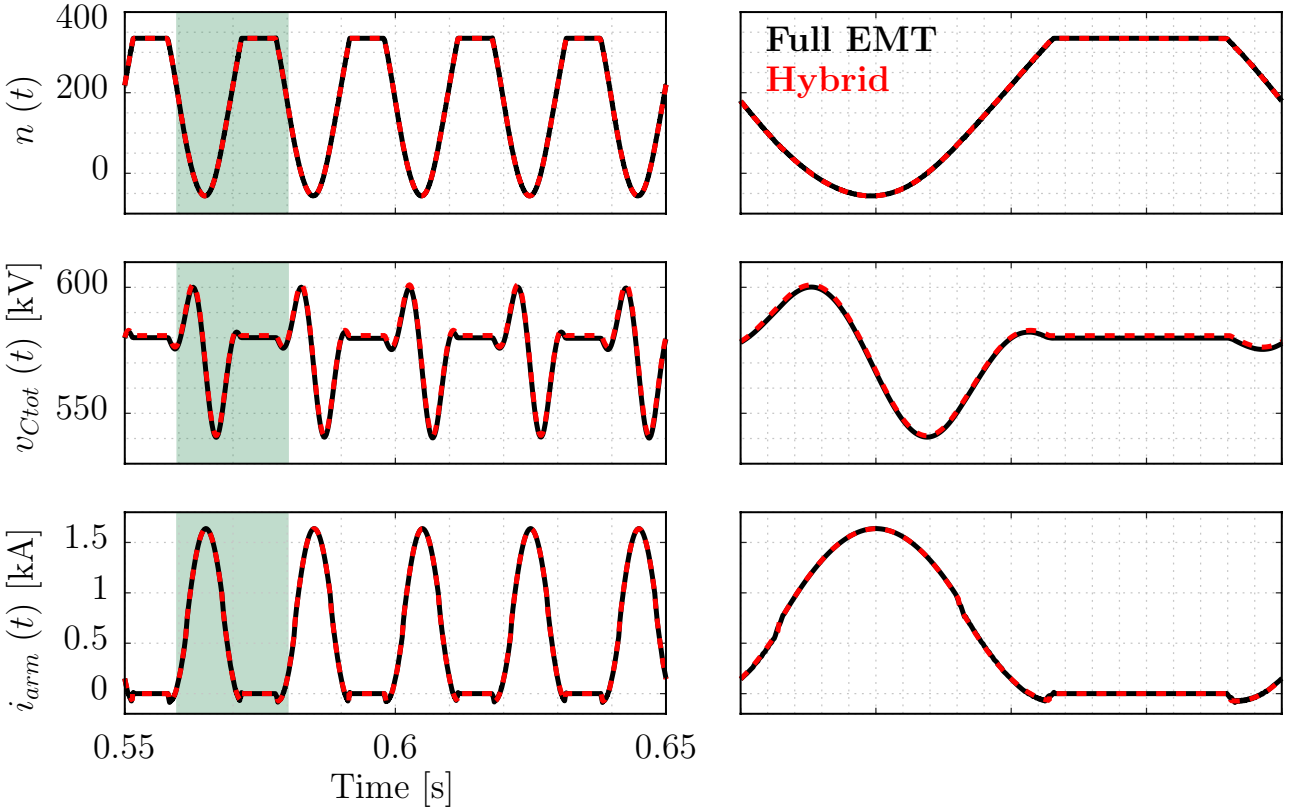


Figure 2.32 – Electrical quantities comparison between a full EMT simulation and the Hybrid proposed simulation

Now, the switching of the SMs is compared over two elements which are: the switching frequency distribution among the SMs and the average. For both simulations, the VBA is achieved within a time step of 5μs and a tolerance of 200 V between the most and least charged SM capacitors is introduced.

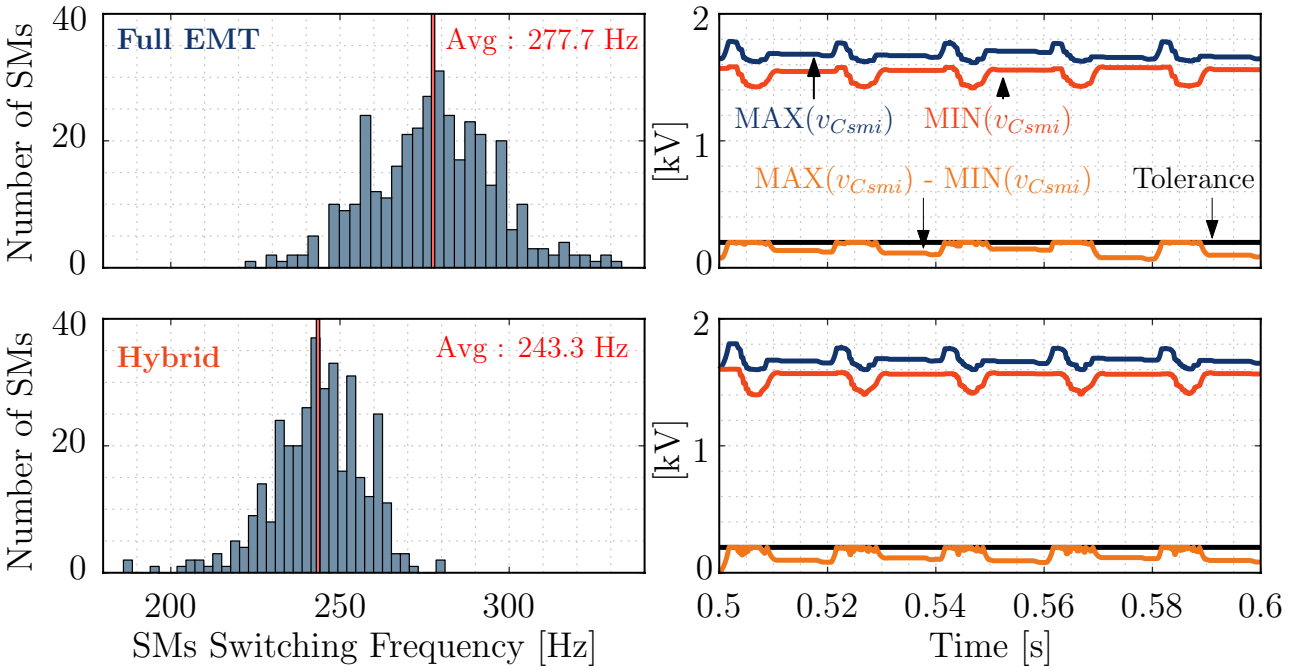


Figure 2.33 – Comparison between the full EMT simulation and the proposed Hybrid method on stack switching

On the left side of Figure 2.33 are displayed the frequency distribution of SMs for each type of simulation and the average switching frequency. Even if all electrical quantities match between the two types of simulation, the switching frequencies are not. In the case of the EMT simulation, maximal and minimal values are comprised between ∼220 and ∼330 Hz and an average value of 277.7 Hz is calculated. Regarding the hybrid simulation, the switching frequency is between ∼180 and ∼280 Hz with an average value of 243.3 Hz. It is clear that the difference between both models is relatively high, around 14.4%, and not really coherent with the previous results. Trying to understand where this difference may come from, needs to observe the action of the CBA. This is depicted on the right side of Figure 2.33. On these graphs are illustrated the maximal and minimal capacitor voltage values and their difference with regard to the tolerance. These results are quite similar. The small differences that are observed, do not explain 14% deviation of the average switching frequency. Thus, the remaining parameters that is not considered in the coded model are (i) the the current controllers , (ii) the integration of several stacks in the EMT simulation. The current ripple can interact with the proportional gain of the current controllers which may request more often the insertion or the by-pass of SMs. The final comparison is provided on Figure 2.34.

On this figure are presented the total losses (i.e. conduction and switching) and the execution time. The comparison is made for the extreme cases where the converter operates at the rated power ($\pm P_n$ and $\pm Q_n$). As expected, there are some differences in the losses estimation which is in the order of 300 kW. Considering about 9 MW of total losses gives a relative error of 3.33%. This small error is tolerable since the execution time has been reduced by 6∼7, depending on the operating point.

So, in overall, this method gives satisfying results, however, as all methods using a part of analytic equations, it suffers of a lack of precision on switching losses.

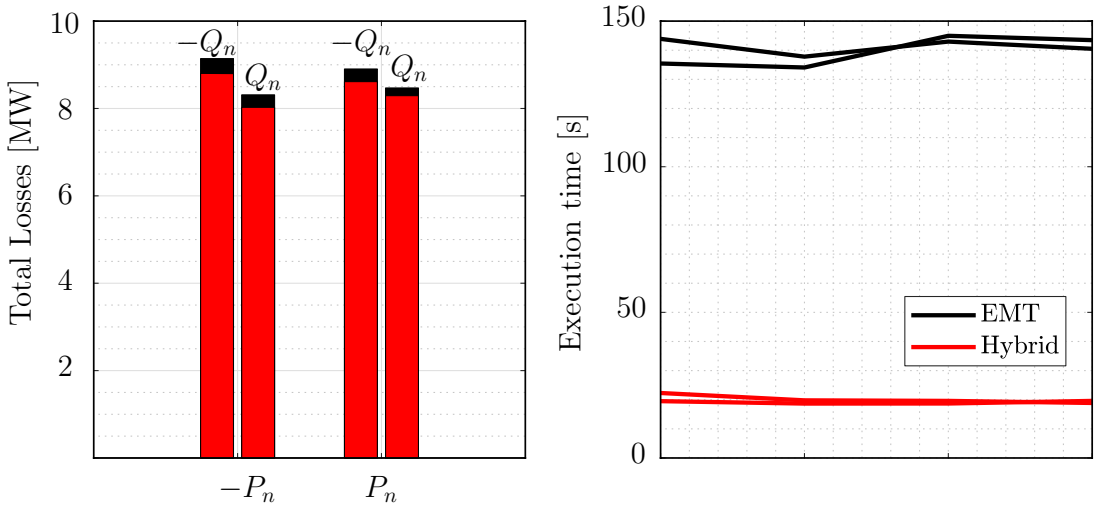


Figure 2.34 – Comparison between the full EMT simulation and the proposed Hybrid simulation on losses estimation

2.4.3 Losses Estimation Results

First of all, let us introduce devices that have been selected for this study. As reported in [71, 88] and mentioned in Chapter 1, the DS are soft-switched. This soft-switching as well as the number of series connected devices invite the use power switches with high voltage and current capability. In [117], a comparison between semiconductors is achieved between IGBTs, Injection Enhanced Bipolar Transistor (IEGTs) and Integrated Gate Control Thyristors (IGCTs).

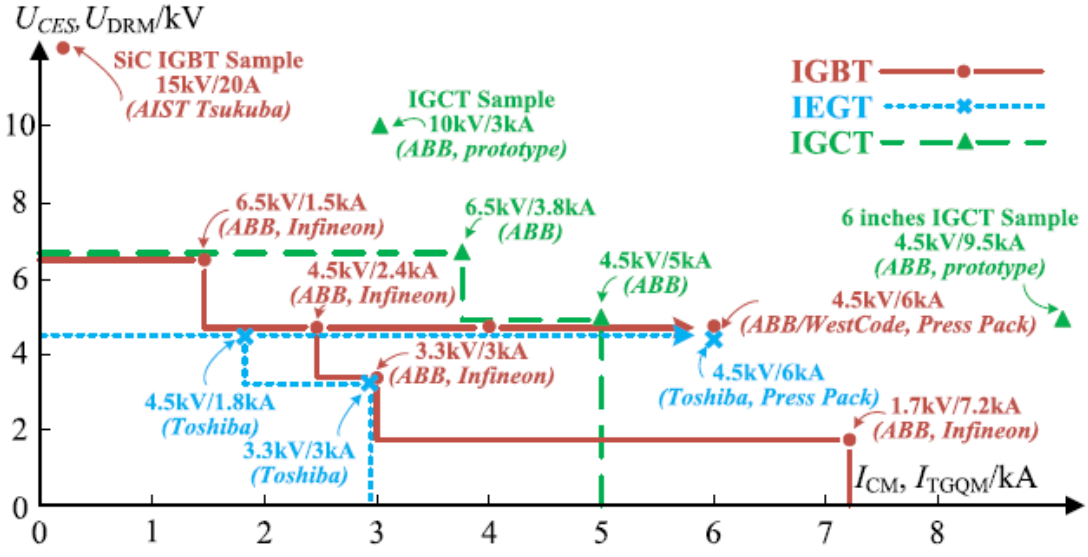


Figure 2.35 – Comparison of voltage and current ratings of power devices in 2017 [117]

The rated power of the converter is about 1.044 GVA and the peak value of the arm current is about 1.7 kA while its RMS value is 0.8 kA. Thus, power devices with 1.5 kA (DC) capability are sufficient. In this current range, the classical IGBT modules Infineon FZ1500R33HL3 (3.3 kV/1.5 kA) have been considered for the SMs.

Regarding the DSs, different choices have been tested. First, a full IGBT based converter is tested using Infineon modules. Second, the IEGTs Toshiba ST1500GXH24 press-pack device enabling 4.5 k/1.5 kA. Finally, the IGCT press-pack device ABB asymmetric 5SHY 35L4520 and its associated fast-recovery diode 5SDF 20L4520, both rated to 4.5kV/1.7kA [118].

Thanks to the soft-switching of the DS, ON-state voltage drop characteristics are the most important factor to consider in their losses estimation. The next graphs display them for each device.

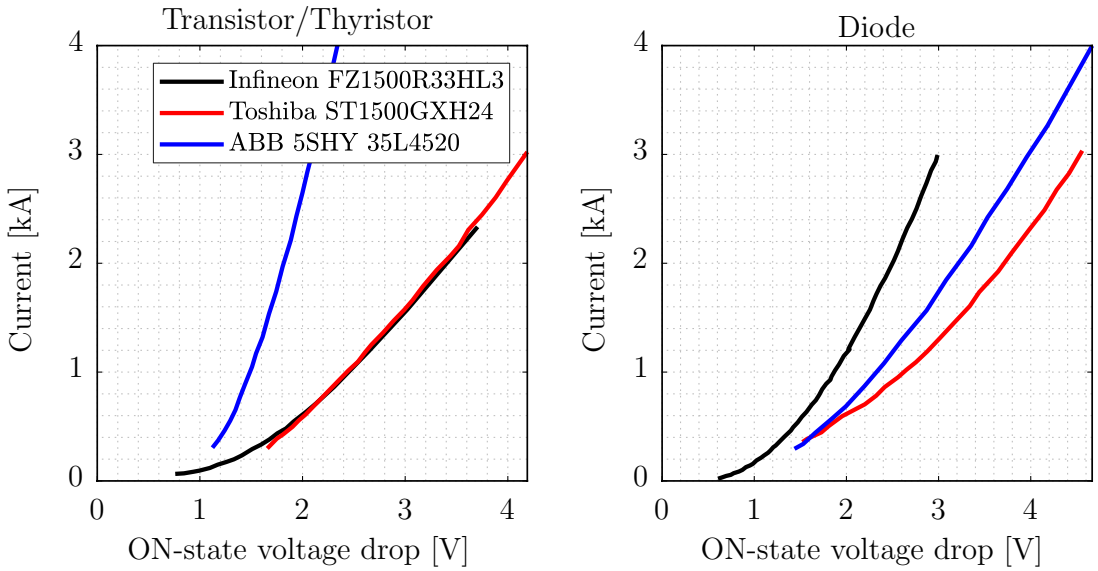


Figure 2.36 – Static characteristics comparison between IGBT, IEGT and IGCT considering a junction temperature equals to $125^{\circ C}$

As shown by Figure 2.36, IGBTs and IEGTs exhibits similar voltage drops. On the other hand, the IGCT, which is not based on transistor technology, presents much better characteristics. Regarding diodes, the IGBT modules provides the best performances.
Let us recall the design we used so far.

$$k_{N0} = 0.32$$
$$N_{SM} = 300$$
$$\hat{V}_{DS} = 380 \text{ kV}$$

considering utilisation factors of 60% leads to IEGTs and IGCTs with nominal voltages equal to 2.7 kV. Thus, the number of power devices that compose a DS is

$$N_{IGBT} = 240$$
$$N_{IEGT} = 141$$
$$N_{IGCT} = 141$$

comprising the transistors/thyristors and diodes. In practice, an additional snubber is used to protect the IGCT at turn off due to the use of the anti-parallel diode [112, 119]. In this thesis the snubber will not be considered since its impact on power losses represents about one or two tenth of the switch losses with regard to the results shown in [112].

Results of the losses estimation are summarised below.

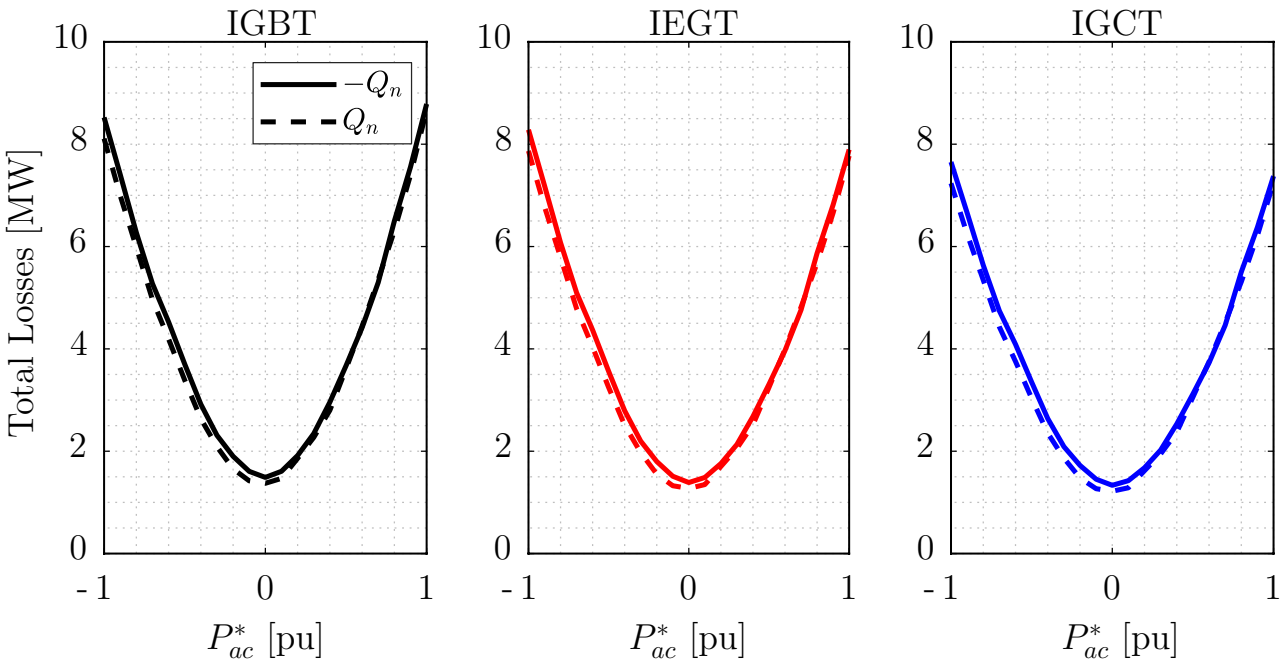


Figure 2.37 – Losses estimation results for a variation of the AC side active power reference. In normal line the reactive power is set to a constant value $-Q_n$. In dashed line it is Q_n.

On Figure 2.37 are depicted the total losses including: the conduction losses, the switching ones and the ones in passive components (L_L and L_{dc}). As expected, the IGCT based DS provides the best results since conduction losses are dominant in modular type converters. Those losses are shown on the next graph.

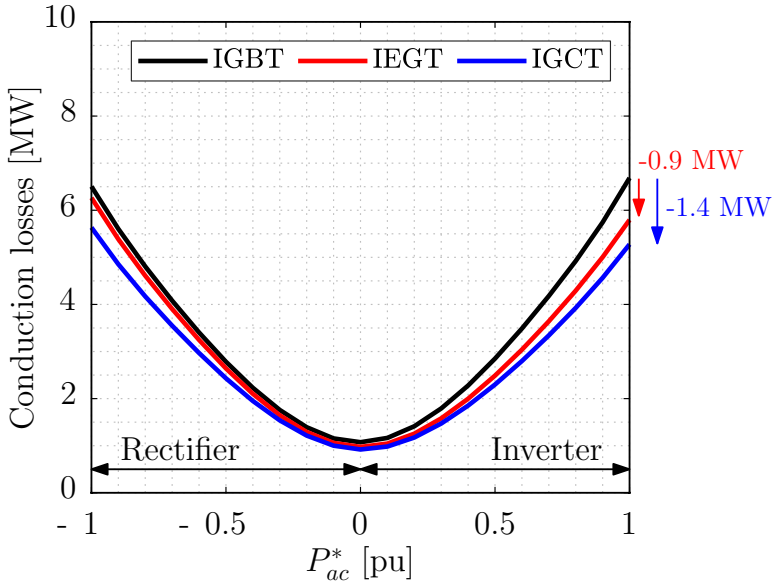


Figure 2.38 – Comparison of conduction losses between IGBT, IEGT and IGCT based DSs

As shown by Figure 2.38, the difference between each technology of power switches may be significant. First let us analyse the rectifier operating mode. In that case, the current mostly flows through the diodes of the DSs. Diodes of IEGTs and IGCTs having higher ON-state voltage drops but less numerous. Thus the difference with the IGBT case become small. On the other hand, in inverter operating mode, transistors/thyristors are the main conductors.

Thus, the reduced number of devices in case of IEGTs and IGCTs allows obtaining important gains, that may reach 0.9 MW and 1.4 MW respectively.

Thereby, through these figures it is highlighted that the choice of the DS technology may be very important despite the fact that EO-AAC stacks comprise many FB-SMs. This might even more through with higher value of k_{N0} since the voltage across the DSs increase by two times the decreasing of the number of SMs.

Finally, to provide an idea of the efficiency of an EO-AAC, the above results are compared to the MMC-HB including 400 SMs per stacks and a modulation index equals to 0.816. SMs are based on the Infineon IGBT modules as the EO-AAC.

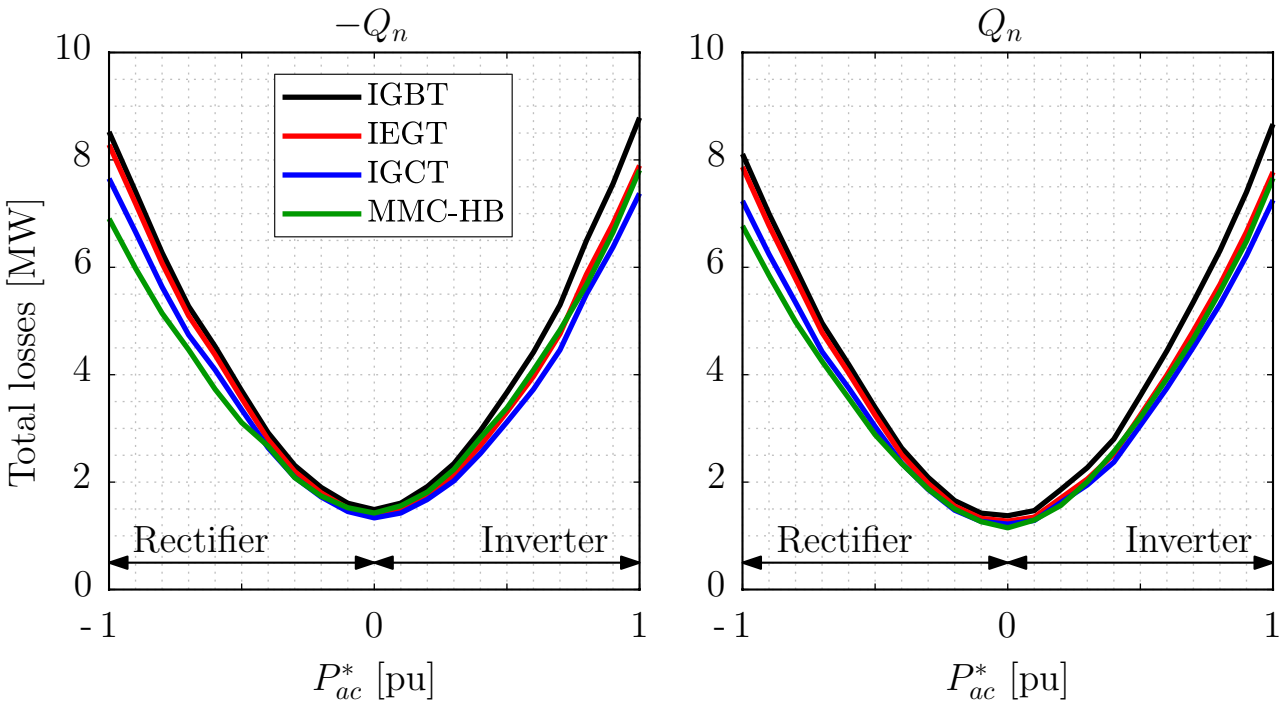


Figure 2.39 – Comparison of losses between EO-AAC and MMC-HB

The MMC-HB have been added in green on fig:Losses3. Compared to the EO-AAC, it is interesting to note that depending on whether the converter operates as an inverter or a rectifier the results of the comparison is different. Start with the rectifier operating mode. In that case, the MMC is significantly better than the EO-AAC all DS technologies included. However, once converters goes to the inverter operating mode, interestingly the EO-AAC can achieve similar losses with IEGT based DS and be more efficient with IGCTs.

However, these results have to be mitigated since they are obtained for a modulation index that is quite low which let us think that by injection of zero sequence voltage in MMC modulated voltages, to either increase the AC voltage or diminish the number of SMs per stack the conclusion would be similar to the rectifier operating mode. But nonetheless, despite its use of FB-SMs to get this DC-Fault blocking capability, the EO-AAC presents a very respectable level of losses.

2.5 Chapter Conclusion

In this chapter has been presented dimensioning of the EO-AAC. From choices that has been done in the first section

- DC-fault blocking capability with the minimal number of SMs
- Reactive power capability of 300 MVAR through an AC side impedance of 0.15 p.u.

a dimensioning of the stacks of SMs, the DSs, the SM capacitance and a losses analysis have been performed. These choices have led to

- 300 SMs per stack
- The rate of zero sequence voltage injection is set to $k_{N0} = 0.32$
- $C_{SM} \geq 5$ mF

suggesting a compact design as stated in [71] compared to HB-MMC.

As results of this design an estimation of the losses between $\sim$7 and $\sim$8.5 MW has been obtained. As highlighted in this section, the choice of the DS technology is highly important. Finally, a comparison between EO-AAC and MMC-HB losses has been carried out showing the equivalence between both converter is some operating. Nevertheless, with small adjustment, the MMC-HB can be remain more efficient than the EO-AAC.

Chapter 3

Dynamic Model and Control Structure Design of the EO-AAC

3.1 Introduction

The dynamic modelling and the derivation of a control structure of a power electronics device plays an important role in its operation. The control is often decomposed into a low-level controller (i.e. closed to the device) and a high-level controller regulating state variables. Applied on the EO-AAC, the following generic control organisation is obtained:

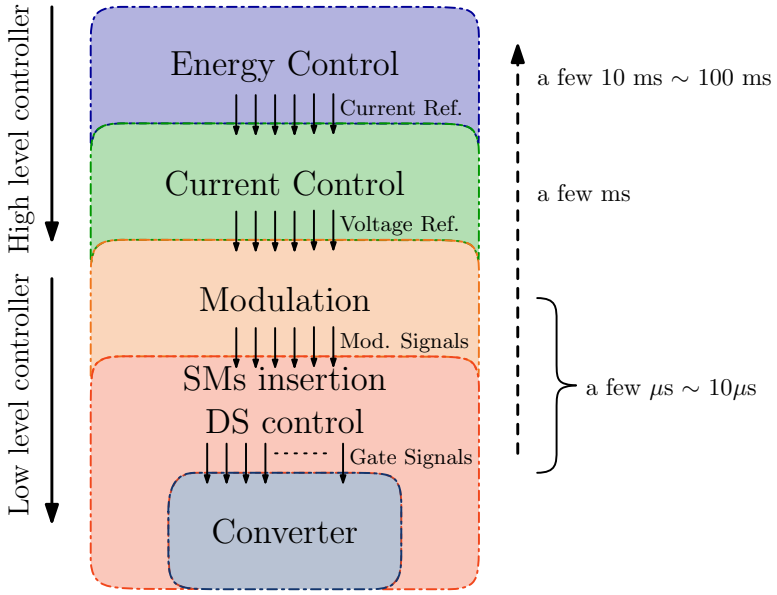


Figure 3.1 – Overall control structure of the EO-AAC

According to the control layers depicted on Figure 3.1, the execution time of each is different. The more the controller is closed to the device the more it has to be fast since it needs to deliver gate signals to drivers. External layers can be slower.

In this chapter each control layer is detailed, with a specific attention on the energy management as it can represent a key point in the dynamic operation of the EO-AAC connected to the grid.

3.2 Low-Level Controller

The Low-level controller consists in traducing modulated voltage references arising from the high-level controller into gate signals to control power switches of the SMs and the DSs. This control layer handle the hybrid operation of the converter (i.e. modified full-wave on DS and modulated voltage on stacks). As shown on Figure 3.1, the control layer is decomposed in two main parts, the modulation (i.e. voltage references normalisation) and the generation of SMs and DSs gate signals. The control of the DS has been detailed in Chapter 1, thus, in this chapter it is not recalled.

3.2.1 Insertion Index and SM Capacitor Voltage Balancing

For a stack of SMs, it is required to generate gate signals for each switching cells based on the insertion index n. In the literature there are essentially two ways to derive this insertion index. A first one relies on the use of multiple carrier based PWM (i.e. N_{SM} carriers for unipolar SMs) [120, 121], however, this solution becomes particularly complex and heavy to compute in case of HVDC stations equipped with hundreds of SMs. The second solution, more suitable for HVDC stations, has been introduced as a Nearest Level Modulation (NLM) [109, 122] and applies a rounding function on modulation signals in order to get the number of SMs to be inserted and by-passed.

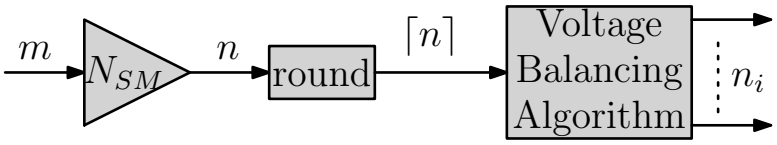


Figure 3.2 – Illustration of the Nearest Level Modulation

As shown on Figure 3.2, the modulation signal m is multiplied by the number of SMs (N_{SM}) to get the insertion function n. After that, a rounding function is applied and its output sent to the Voltage Balancing Algorithm (VBA). Such algorithms have been covered in the MMC literature [108, 123], but its main principle is recalled below.

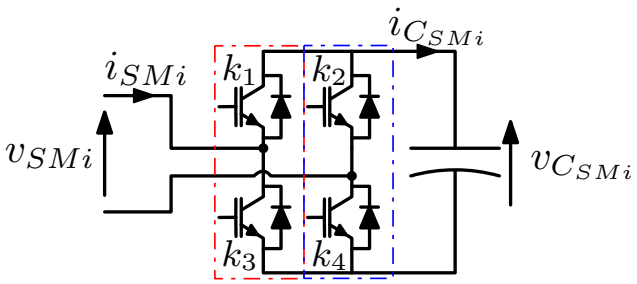


Figure 3.3 – A Full-Bridge SM

EO-AAC stacks are built with FB-SMs shown on Figure 3.3. It is composed of four power switches forming two vertical switching cells. Depending on the modulated voltage sign (sign of m) the output voltage v_{SMi} of the i^{th} SM can be forced to be positive or negative. Depending on the sign of the current i_{SMi} (i.e. the converter arm current) transistors or diodes are conducting. This is summarized on the next figure and table.

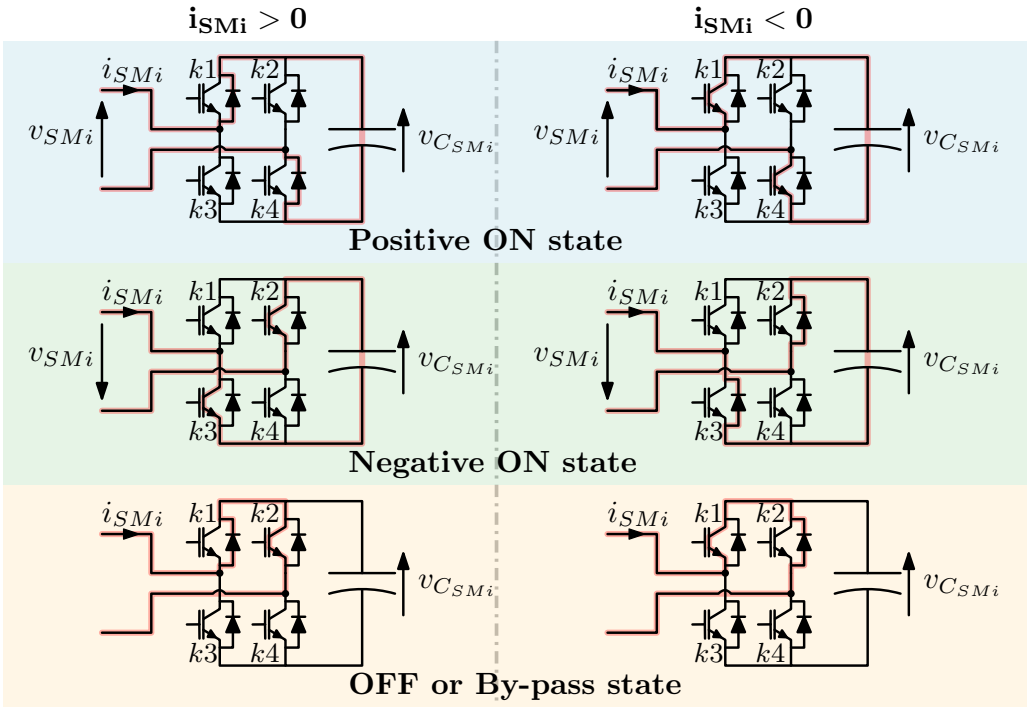


Figure 3.4 – Illustration of FB-SM states and current path

	i_{SMi} positive	i_{SMi} negative
v_{SMi} positive	D1 D4	T1 T4
v_{SMi} negative	T2 T3	D2 D3
v_{SMi} zero	D1 T2 or T3 D4	T1 D2 or D3 T4

Table 3.1 – Possible states of the FB-SMs and device utilisation

In case of the by-pass state, the upper or lower switches can be used. For the sake of simplicity the case where the upper switches are used has been chosen. As a result, by defining the logical states of each power switch Sk_1,Sk_2,Sk_3 and Sk_4, the SM output voltage and modulated current can be expressed

$$v_{SMi} = (Sk_1Sk_4 - Sk_2Sk_3)\, v_{C_{SMi}} \tag{3.1a}$$

$$i_{C_{SMi}} = (Sk_1Sk_4 - Sk_2Sk_3)\, i_{SMi} \tag{3.1b}$$

By defining the insertion index n_i, or modulation function, of the i^{th} SM such as

$$n_i = (Sk_1Sk_4 - Sk_2Sk_3) \quad \in [-1; 0; 1] \tag{3.2}$$

it yields

$$v_{SMi} = n_i v_{C_{SMi}} \tag{3.3a}$$

$$i_{C_{SMi}} = n_i i_{SMi} \tag{3.3b}$$

Using the relations of (3.3) involving the insertion index, the capacitor voltage and the arm current makes possible to simplify the FB-SM through a controllable voltage delivering the SM output voltage and a controllable current source traducing the insertion of the SM capacitor in the current path as illustrated on Figure 3.5.

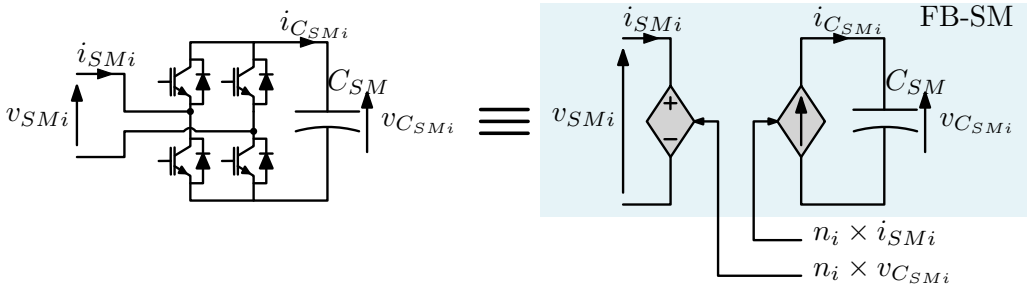


Figure 3.5 – A Full-Bridge SM with its simplified representation

According to Figure 3.5, the deviation of a SM capacitor voltage is given by:

$$\frac{dv_{C_{SMi}}}{dt} = \frac{1}{C_{SM}} n_i i_{SMi} \tag{3.4}$$

As a result of (3.4), it can be concluded that SM capacitor are charging if

$$n_i i_{SMi} > 0$$

and discharging if

$$n_i i_{SMi} < 0$$

Thus, the FB-SM offers two way for the capacitor voltages balancing. A first one, common with the HB-SM, depends on the sign of the arm current current. The second way exploits the bipolar voltage capability of the FB-SM so that some SMs are positively and negatively inserted. However, with this second technique, it is important to maintain the sum of $\sum n_i$ equals to $\lceil n \rceil$. Different types of balancing algorithm exist, one of the simplest relies on the arm current sign and a tolerance band illustrated as it follows

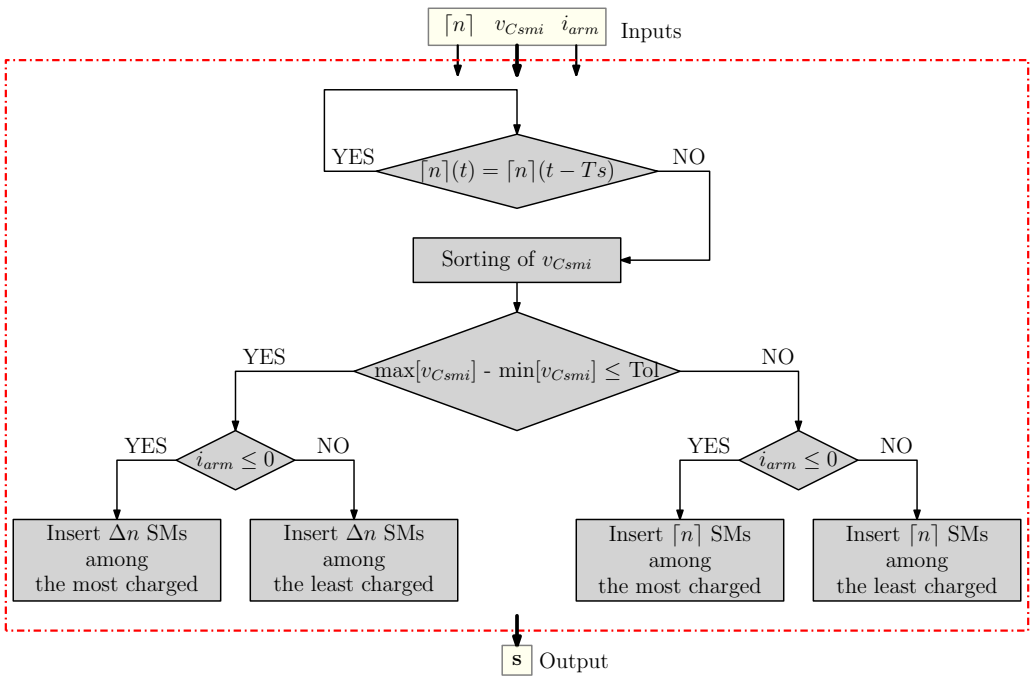


Figure 3.6 – Illustration of tolerance band VBA

Applying such algorithm would lead to the results presented onFigure 3.7 where a stack of 20 SMs has been considered as well as a tolerance of 0.1 p.u. between the most and least charged SM capacitors.

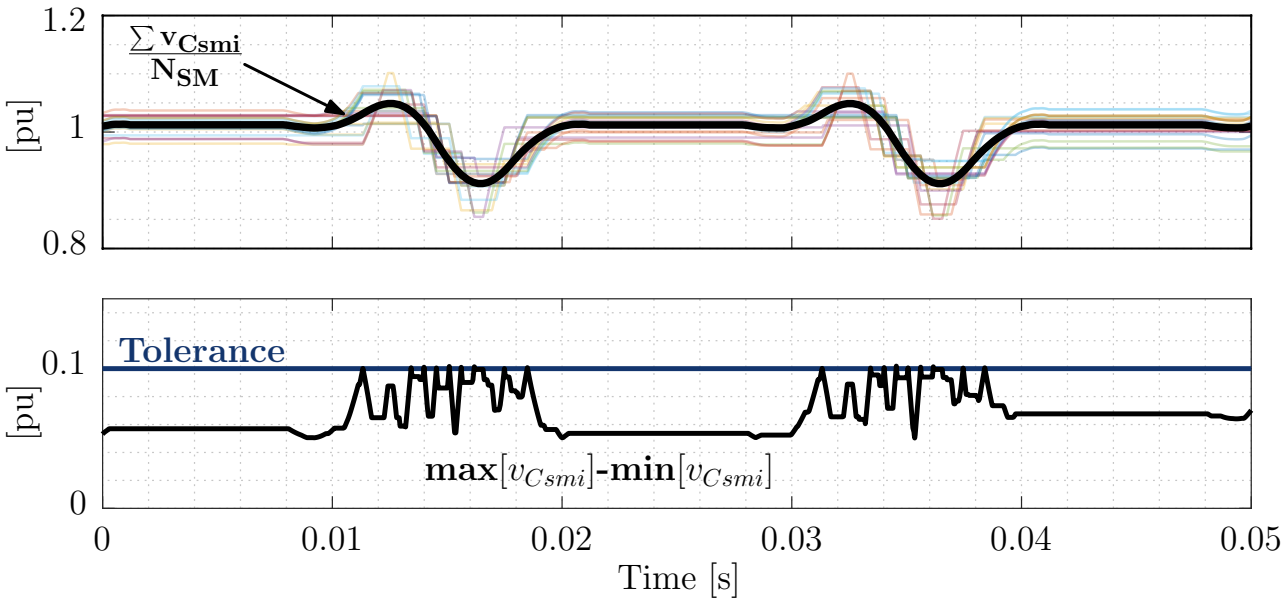


Figure 3.7 – Illustration of the SM capacitor voltages including Balancing Control Algorithm

Thanks to zero crossing of the modulated voltages and arm currents, the VBA is able to determine which SM should be inserted or by-passed to keep whole stack balanced. This is presented on the fist graph Figure 3.7. On the second graph is presented the compliance with the constraint defined by the tolerance. The choice of its value impacts (i) the voltage availability (i.e. $v_{Ctot} > |v_m|$) if it is too high and (ii) the switching frequency of the SMs if it is too low. However, as all SMs are kept within a desired band, an average stack model comprising one equivalent capacitance C_{tot} introduced in MMC literature [84] can be described.

Once the insertion indices are computed and sent to the drivers, finally, the modulated voltages are a consequence of the sum of all insertion indices and SM capacitor voltages:

$$v_m = \sum_{i=0}^{N_{SM}} v_{SMi} = \sum_{i=0}^{N_{SM}} n_i v_{C_{SMi}} \tag{3.5}$$

Under the assumption that all SM capacitor voltages are kept in a close range, it is a fair assumption to note

$$v_m = n\bar{v}_{C_{SM}} \tag{3.6}$$

with n is the sum of all insertion index n_i and $\bar{v}_{C_{SM}}$ the average SM capacitor voltage introduced on Figure 3.7. Therefore, for a stack comprising N_{SM} its equivalent arm capacitor voltage (v_{Ctot}) is simplified to

$$v_{Ctot} = N_{SM}\bar{v}_{C_{SM}} \tag{3.7}$$

allowing the introduction of modulation function m noted

$$m = \frac{n}{N_{SM}} \tag{3.8}$$

leading to

$$v_m = m \times v_{Ctot} \tag{3.9}$$

The modulated current that flows through the equivalent capacitor C_{tot}, thus called i_{Ctot} can be derived following the same procedure.

$$\sum_{i=0}^{N_{SM}} i_{C_{SMi}} = \sum_{i=0}^{N_{SM}} n_i i_{SMi} \tag{3.10}$$

once a stack of SMs is considered the current i_{SMi} is in fact the arm current i_{arm}. Introducing the modulation function m as in (3.8) leads to

$$\frac{1}{N_{SM}} \sum_{i=0}^{N_{SM}} i_{C_{SMi}} = m \times i_{arm} \tag{3.11}$$

with

$$\frac{1}{N_{SM}} \sum_{i=0}^{N_{SM}} i_{C_{SMi}} = i_{C_{tot}} \tag{3.12}$$

It results in an average model for the stacks well known in the MMC literature depicted on Figure 3.8.

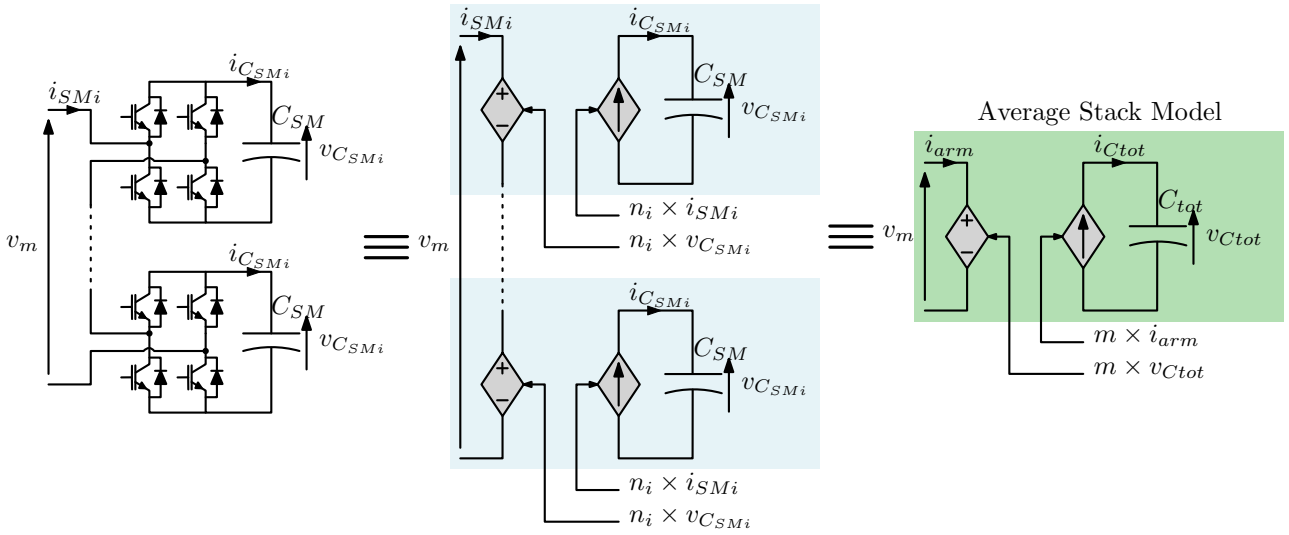


Figure 3.8 – A stack of Full-Bridge SMs with its simplified representations

More elaborated type of average stack model exist to capture, for instance, the blocked state of the SMs [124]. However, from this simple average stack model, studying the generation of the modulation signals m can be done.

3.2.2 Modulation Signals Generation

The derivation of the modulation signals m requires to normalise the modulated voltage references according to the voltage sources from which they are generated (e.g. 2-Level VSC it is $v_{dc}/2$). For a converter with embedded energy storage, and especially capacitive energy storage in the arm, the notion of DC bus voltage utilisation no longer exist since the output voltages become a function of the internal voltages v_{Ctot} as detailed in Chapter 1.

For MMC, normalization by a constant voltage has been proposed in many works [82, 125]. This modulation scheme is very simple to be implemented and offers 2-Level VSC like behaviour [126]. On the other hand, it introduces distortion in the AC voltages and currents as well. As

a result, this modulation scheme needs the well known circulating current suppressing control (CCSC) [81, 125]. In the overall AAC literature, all overlap lengths included, this question has been investigated in [127], where as it could be expected, distortion on the AC side was observed as well as higher energy balancing current. However, it was done for the SO-AAC and possible effect with the EO-AAC topology no established. So, let us define :

- Uncompensated modulation : $m = \dfrac{v_m^*}{V_{Ctot0}}$
- Compensated modulation : $m = \dfrac{v_m^*}{v_{Ctot}}$

with V_{Ctot0} the nominal value of v_{Ctot}. These two approaches have been applied on EO-AAC and results are presented on Figure 3.9.

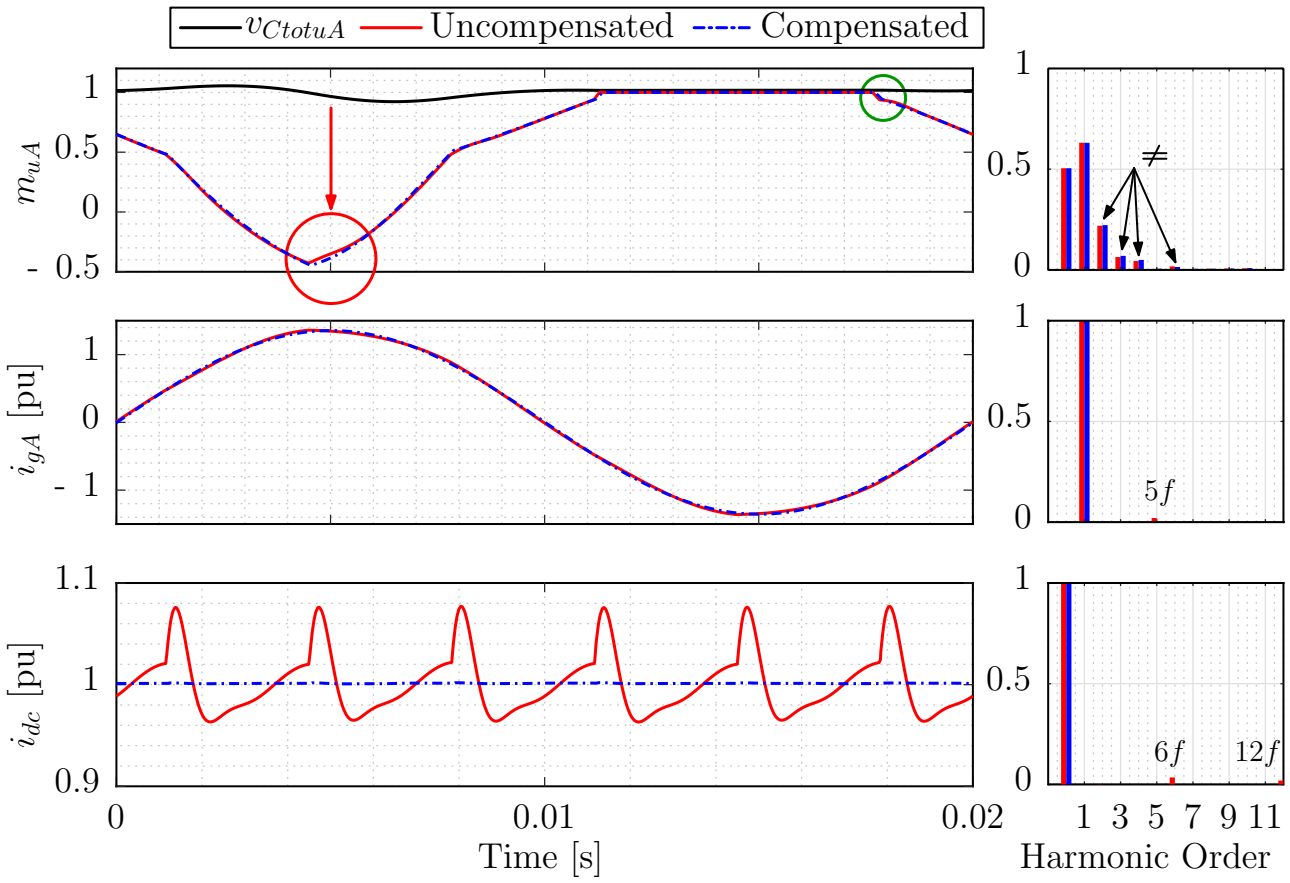


Figure 3.9 – Steady-state simulation results of the EO-AAC with Uncompensated and Compensated modulation schemes

The first graph presents the modulation signal m_{uA}, where in red is the uncompensated modulation and in dashed blue line the compensated one. The most visible difference is circled in red. It results that a fifth order harmonics observed on the AC currents. However, the quantity that is the most impacted by the modulation scheme is the DC current presented on the last graph. A ripple of 0.12 p.u. arising from the errors on modulated voltages circled in red and green is observed. The green error occurs at the beginning of the overlap period destabilising the absorption of the DC current ripple.

Finally, from the graph of the modulation signals m_{uA} and its Fourier analysis, it is highlighted that the main effect of the modulation scheme starts from the third-order harmonic

in modulated voltages. Thus, the use of ZSVI exacerbates these errors since it is essentially composed harmonics multiple of three. Running the same simulation without ZSVI confirms this analysis and reduces by two the DC current ripple. Therefore, it clearly appears that compensation of the voltage oscillations in SM capacitors is mandatory for the EO-AAC to maintain a good quality of AC and DC currents.

3.3 Current Models and Control Structure Design

The high-level controller is composed of two main layers, named external and internal layers. This section focuses on the internal one comprising the current controllers. To do so, this section and the following one are based on the EO-AAC model presented on Figure 3.10.

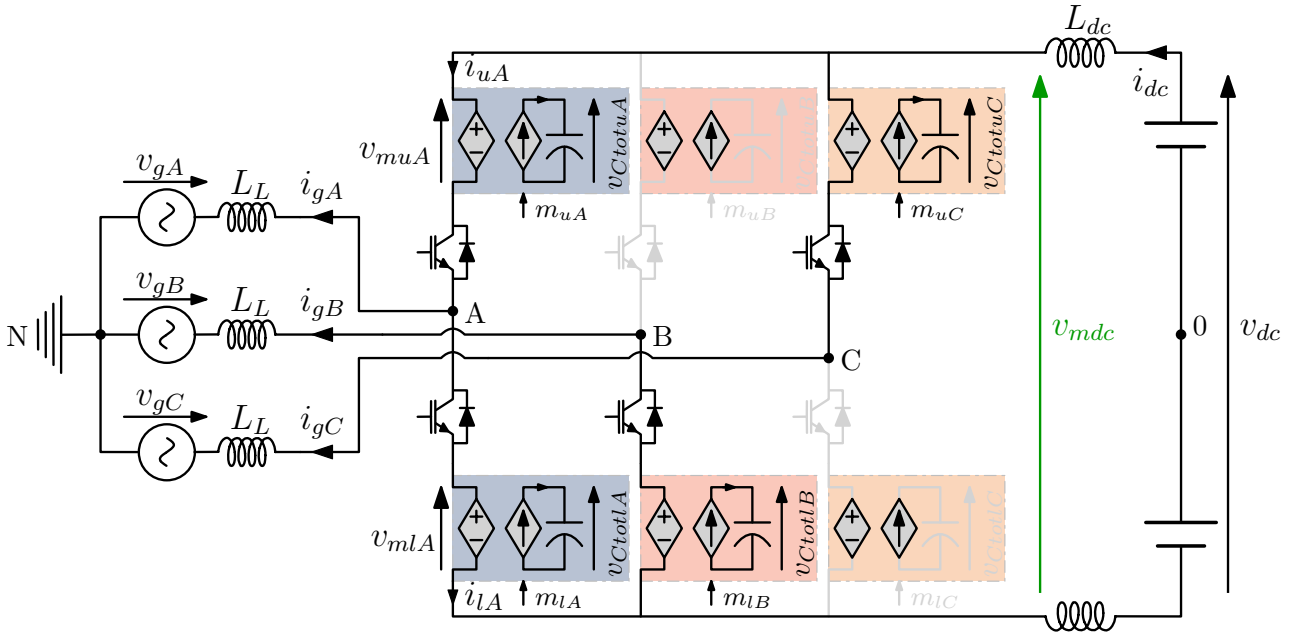


Figure 3.10 – EO-AAC including average stack model

Each stack of SMs is replaced the average stack model and its equivalent capacitor.

3.3.1 AC and DC side Dynamic Models

To determine the AC and DC side dynamics, this section will decompose the operation of the converter as Non-overlap and Overlap mode. In addition, a single-phase representation is used is used to alleviate notations.

Non-overlap mode

During this operating mode, the conducting arms must participate to the AC voltage modulation, but, as a degree of freedom is missing in the control, they cannot participate to the DC bus current regulation. According to Figure 3.10

$$\begin{aligned} v_g + L_L\frac{di_g}{dt} + R_L i_g + v_{mu} - \frac{v_{mdc}}{2} + v_{N0} = 0 \\ v_g + L_L\frac{di_g}{dt} + R_L i_g - v_{ml} + \frac{v_{mdc}}{2} + v_{N0} = 0 \end{aligned} \tag{3.13}$$

As described by (3.13), despite their inability to regulate the DC bus current, arms in non-overlap operating mode must follow the fluctuation of the DC potential v_{mdc} due to the presence of the DC bus reactor. Let us now define the expression of the voltage v_v used to drive AC powers.

$$v_v = v_g + L_L \frac{di_g}{dt} + R_L i_g \tag{3.14}$$

so that

$$\begin{aligned} v_{mu} &= \frac{v_{mdc}}{2} - v_v - v_{N0} \\ v_{ml} &= \frac{v_{mdc}}{2} + v_v + v_{N0} \end{aligned} \tag{3.15}$$

which are the expressions defined in Chapter 1.

Overlap mode

In overlap operating mode, it has been mentioned that a MMC-like behaviour can be performed. Therefore, a similar current dynamics modelling can be done using the Σ and Δ representations [80, 128, 129]. Let us reconsider the equations of (3.13). Since both arms are now conducting, their actions must be coordinated to control the AC currents. It is realised by summing both equations.

$$v_g + L_L \frac{di_g}{dt} + R_L i_g + v_{N0} = \frac{v_{ml} - v_{mu}}{2} \tag{3.16}$$

where the expression of the v_v remains the same. The only difference between the overlap and non-overlap lies in the distribution of this AC component in the modulated voltages. This is an important point since in some AAC works it was reported that the presence of arm inductors led to a time-varying equivalent AC side impedance involving two expressions of v_v and AC power oscillations [89,90]. The amplitude of these oscillations depends on the ratio between the transformer impedance and the arm impedance. By using DC reactors, the EO-AAC overcome this issue.

Regarding the DC side dynamics, subtracting the equations of (3.13) gives:

$$v_{mdc} = v_{mu} + v_{ml} \tag{3.17}$$

with

$$v_{mdc} = v_{dc} - L_{dc} \frac{di_{dc}}{dt} - R_{dc} i_{dc} \tag{3.18}$$

Thus, the leg in overlap operating mode actively manage the DC current through the absorption of (i) the AC components coming from the two other conducting arms and (ii) additional components as it will be detailed in energy management part of this chapter.

3.3.2 Current Control Structure

Controlling currents in modular converter can be performed in two different ways. The first one considers separate AC and DC dynamics as in the above derivations. Therefore, there are controllers for the AC and DC currents. Another consists in the regulation of the arm currents [71, 130] with no explicit decoupling action. This approach is easier to implement by using state-space modelling and state feedback controllers. In this thesis, the first approach is considered to keep a decoupled control of the AC and DC currents.

AC current controllers

The AC current models contain two independent state variables to be controlled in the positive sequence. Two others components in the negative sequence can also be controlled [74, 131] but not studied here. To control those currents, there are different methods: some of them consists in the use resonant controllers in abc or $\alpha\beta 0$ frames [27]. The second type of method is using PI (Proportional-Integral) controller on $dq0$ components in the Synchronous Reference Rotating Frame (SRRF). In this thesis, this last method has been used.
Using (3.14) allows obtaining the control structure of the AC side currents assuming the use of the $dq0$ transformation.

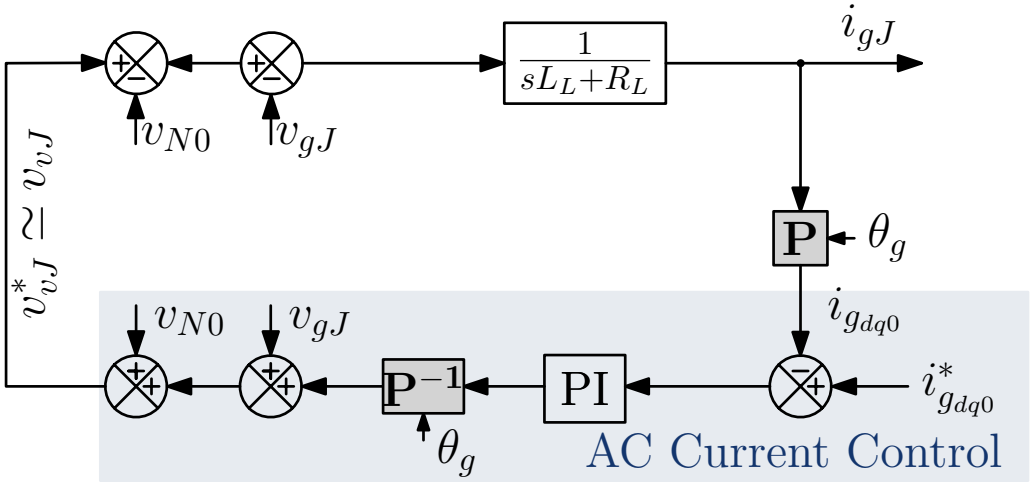


Figure 3.11 – AC current controller scheme

Figure 3.11 summarises the current controllers in both overlap and non-overlap modes. As above mentioned, the only change between these two modes lies in the distribution of the AC components v_v to the upper and lower stacks that is framed in yellow. Thanks to the use of compensated modulation which is based on a strict inversion of the average stack model, all this part can be assumed to be equal to 1. The $dq0$ transform noted $\mathbf{P}$ and its inverse transformation $\mathbf{P^{-1}}$ are in their power invariant forms

$$\mathbf{P} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta_g) & \cos\left(\theta_g - \frac{2\pi}{3}\right) & \cos\left(\theta_g + \frac{2\pi}{3}\right) \\ -\sin(\theta_g) & -\sin\left(\theta_g - \frac{2\pi}{3}\right) & -\sin\left(\theta_g + \frac{2\pi}{3}\right) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \tag{3.19a}$$

$$\mathbf{P^{-1}} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta_g) & -\sin(\theta_g) & \frac{\sqrt{2}}{2} \\ \cos\left(\theta_g - \frac{2\pi}{3}\right) & -\sin\left(\theta_g - \frac{2\pi}{3}\right) & \frac{\sqrt{2}}{2} \\ \cos\left(\theta_g + \frac{2\pi}{3}\right) & -\sin\left(\theta_g + \frac{2\pi}{3}\right) & \frac{\sqrt{2}}{2} \end{bmatrix} \tag{3.19b}$$

To simplify notations, the grid angle θ_g has been used. However, it is worth mentioning that in practice, the angle that is used is the estimated one, $\tilde{\theta}_g$, obtained through the PLL. In the following it is assumed that the synchronisation cancels the voltage on the q axis (V_{gq}). Thus, dq current references are derived as it follows:

$$\begin{aligned} i^*_{gd} &= \frac{P^*_{ac}}{v_{gd}} \\ i^*_{gq} &= \frac{Q^*}{v_{gd}} \end{aligned} \tag{3.20}$$

DC current control

It is now needed to control the DC current in addition to the AC ones. According to (3.18), the following scheme can be drawn

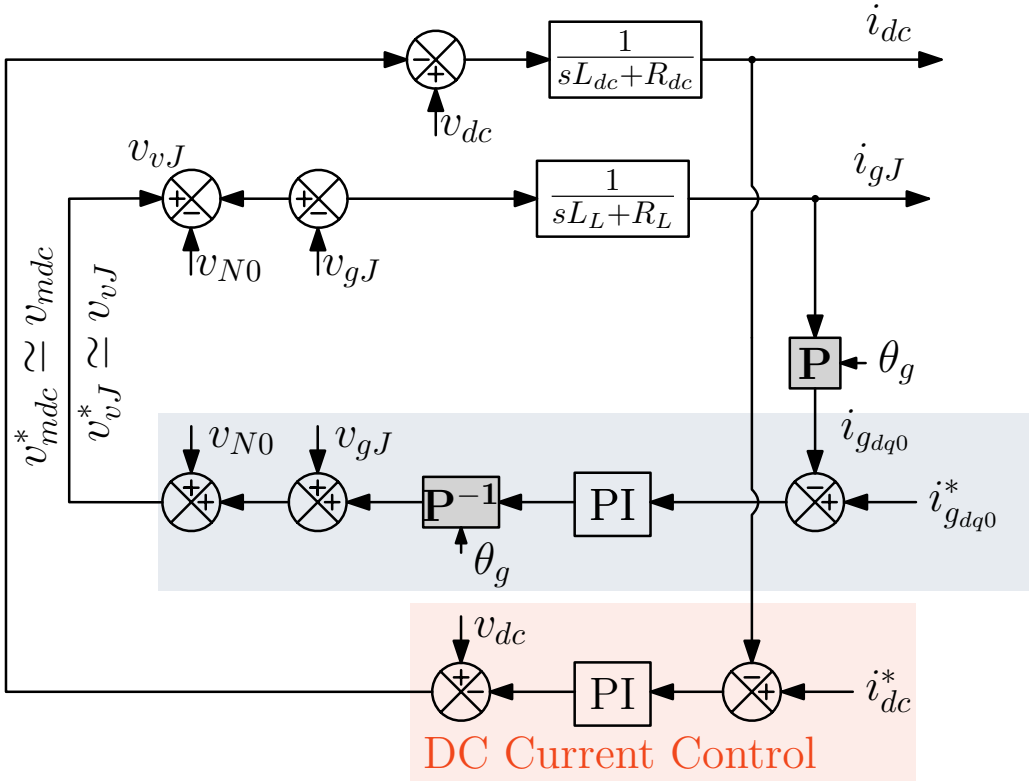


Figure 3.12 – AC and DC current controllers schemes - Overlap mode assumed

As both controllers are decoupled, the references for i_{dc} and i_{gd} (currents related to the active power) could be uncoordinated, however, the internal energy would deviate. To validate the overall current control structure, the following references are used:

$$\begin{aligned} i^*_{gd} &= \frac{P^*_{ac}}{v_{gd}} \\ i^*_{gq} &= \frac{Q^*}{v_{gd}} \\ i^*_{dc} &= \frac{P^*_{ac}}{v_{dc}} \end{aligned} \tag{3.21}$$

To validate the models and the control structures, an EMT simulation is performed using the parameters provided by Table 3.2.

Response time of the dq components is set 5 ms while the DC current is faster i.e. 1 ms. The response of the converter AC current control has been tested over different types of event as active and reactive power ramping, reversal and an active power step. The slew rate of the active power is limited to 1 GW per 50 ms while for the reactive power it is 300 MVAR per 50 ms. As suggested by the waveforms observed on Figure 3.13, the converter easily tracks references to operate at any desired operating point as long as this one is in the PQ envelop provided by the available voltage in SM capacitors [132, 133]. The AC currents are harmonics free as it was presented in Chapter 1.

Parameters	Value SI	Value p.u
DC Voltage (v_{dc})	640 kV	1
RMS AC Voltage L-to-L (U_g)	500 kV	$\sqrt{3}$
DC inductor (L_{dc})	20 mH	0.004 p.u
DC resistance (R_{dc})	50 mΩ	0.0002 p.u
Leakage inductance (L_L)	116.6 mH	0.15 p.u
Leakage resistance (R_L)	60 mΩ	0.005 p.u
Rated power (S_n)	1.04 GVA	1 p.u
Nominal active power (P_n)	1 GW	0.96 p.u
Nominal reactive power (Q_n)	300 MVAR	0.29 p.u
Stacks nominal voltage	480 kV (300 SMs)	0.75 p.u
Stored Energy (H_C)	11 kJ/MVA	11 ms

Control Parameters	Value
Response time (tr_{ig})	5 ms
Damping ratio (ζ_{ig})	0.7
Response time (tr_{idc})	1 ms
Damping ratio (ζ_{idc})	0.7

Table 3.2 – EO-AAC and control main parameters

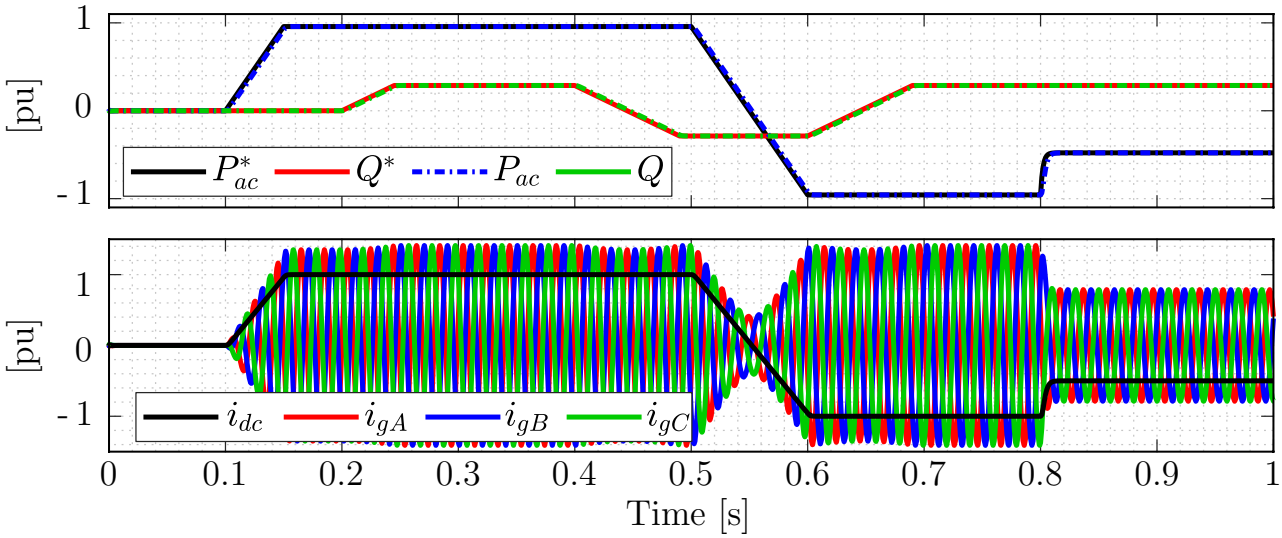


Figure 3.13 – Response of the EO-AAC to a variation of the active and reactive power references

As expected, since both models are decoupled, the introduction of the DC side current loop has not affected the AC side controllers. As shown on the second graph, the DC current is smooth in both steady-state and during transients. The current controller easily tracks the reference so that i_{dc} gets the desired value to keep the AC and DC powers close to each other.

Obtaining these results need to achieve a proper distribution of the modulated voltages on the conducting arm. This is discussed in the following.

Modulated voltage components distribution

The control of the DSs makes the EO-AAC as a sequential system. Thus, AC and DC modulated voltages (v_v and v_{mdc}) are distributed according to the logical state of a DS (G_{DS}). Let us introduce this sequential aspect in the following equation considering one upper arm:

$$v_{mu} = G_{DSu}.\left(\frac{v_{mdc}}{2} - v_v - v_{N0}\right) + \overline{G_{DSu}}.\hat{V}_m \tag{3.22}$$

where X is the state and $\bar{X}$ the complementary state. If the arm is conducting, the stack participate to the voltage modulation, whereas if $\overline{G_{DSu}} = 1$, the modulated voltage is saturated to its maximal value $\hat{V}_m$ (i.e. all SMs inserted). Extended to all six stacks, gives the following matrix interpretation:

$$\begin{bmatrix} v^*_{muA} \\ v^*_{mlA} \\ v^*_{muB} \\ v^*_{mlB} \\ v^*_{muC} \\ v^*_{mlC} \end{bmatrix} = \begin{bmatrix} -G_{DSuA} & 0 & 0 & G_{DSuA} & \overline{G_{DSuA}} \\ G_{DSlA} & 0 & 0 & G_{DSlA} & \overline{G_{DSlA}} \\ 0 & -G_{DSuB} & 0 & G_{DSuB} & \overline{G_{DSuB}} \\ 0 & G_{DSlB} & 0 & G_{DSlB} & \overline{G_{DSlB}} \\ 0 & 0 & -G_{DSuC} & G_{DSuC} & \overline{G_{DSuC}} \\ 0 & 0 & G_{DSlC} & G_{DSlC} & \overline{G_{DSlC}} \end{bmatrix} \begin{bmatrix} v^*_{vA} + v_{N0} \\ v^*_{vB} + v_{N0} \\ v^*_{vC} + v_{N0} \\ \frac{v^*_{mdc}}{2} \\ \hat{V}_m \end{bmatrix} \tag{3.23}$$

where, the maximal voltage $\hat{V}_m$ is assumed to be the same for every stacks to simplify. The modulated voltage v_{mdc} is common to all six stacks since the DC inductors is common all three legs. In the following, this distribution matrix will be named $\mathbf{D}$

$$\begin{bmatrix} v^*_{muA} \\ v^*_{mlA} \\ v^*_{muB} \\ v^*_{mlB} \\ v^*_{muC} \\ v^*_{mlC} \end{bmatrix} = \mathbf{D} \begin{bmatrix} v^*_{vA} + v_{N0} \\ v^*_{vB} + v_{N0} \\ v^*_{vC} + v_{N0} \\ \frac{v^*_{mdc}}{2} \\ \hat{V}_m \end{bmatrix} \tag{3.24}$$

leading to the following figure

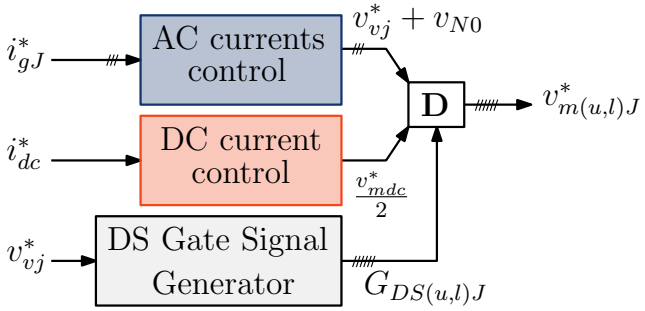


Figure 3.14 – Simplified illustration of the high-level controller internal layer and modulated components distribution

The DS gate signal generator has been discussed in Chapter 1, so we will not go back on that point. The AC and DC current controllers are proposed to be detailed in the next section.

As a conclusion of this section, current control structures have been detailed and validated using time domain simulation. It has been shown that output currents can be harmonics free in steady-state and transients thanks to the full-control of AC and DC dynamics provided by the extended-overlap operation. It is now necessary to set proper reference to AC and DC currents on the basis of system requirements or internal requirement such as the energy controllers.

3.4 Control of the Internal Stored Energy

The energy control, or management, is the most crucial part of the control to ensure the good working of a modular type converter. The insertion of the stacks of SMs has led to a indirect behaviour of energy conversion. Therefore, in some cases the AC and DC active powers may be different resulting in an internal energy deviation. This requires the implementation of an energy management that guarantee the power balance in steady-state to avoid the converter to run without available voltage. This calls for an update of the high-level control scheme depicted on Figure 3.14.

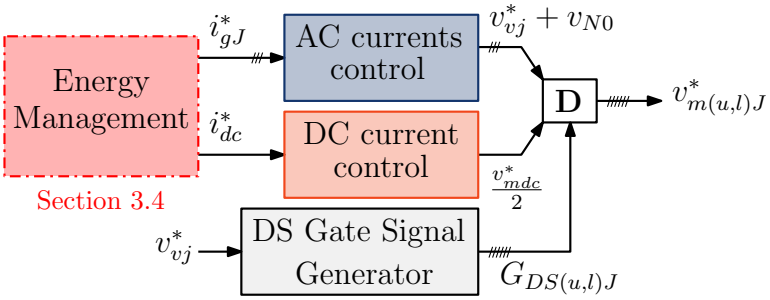


Figure 3.15 – Simplified illustration of the high-level controller internal and external layers

As shown by Figure 3.15, the core of this section lies in the generation of AC and DC current references based on active power requirements for both system and internal power balance needs. However, different approaches exist and discussed below for MMC and EO-AAC.

Brief state of the art of MMC energy management

The continuous operation of the MMC makes its internal energy inherently stable in steady-state and during smooth transients. Indeed, without considering parameter deviations, AC and DC current components are evenly distributed through the converter arms so that there is an inherent power balance and energy distribution between stacks. However, in case of faster transients, unequal distribution of energy among stacks may appear. To improve this transient behaviour two main solutions have been investigated. The first one lies in the use of the uncompensated modulation (or at least with constant DC component) and the well known open-loop control scheme named CCSC [125]. This scheme has the benefit of providing asymptotic stability [126] while being very simple. However, the transient behaviour is not satisfying as the DC current remains uncontrolled. In [134], a closed loop control scheme on the total energy to get DC current control has been proposed to enhance the transient behaviour and stability.
The second solution is a full energy management where all variables related to the energy in capacitors are controlled. There are different ways to control these energies [83, 135] featuring, for instance, the ability to maintain the energy across legs and arms [27, 136] or to prevent AC side oscillations to be reflected on the DC side [137]. In general, the closed-loop control scheme is characterised by an improvement of the converter dynamic performances as well as a better use of the MMC control degree of freedom. This highlighted on the next figure, where the converter response is tested against a active power step of 1 p.u.

As depicted by Figure 3.16 the full energy management provides significant improvement in terms of dynamic response compared to the classical CCSC [125]. The control CCSC including the zero sequence control (i.e. the DC current) [134] provides intermediate behaviour as it mixes closed and open-loop control schemes.

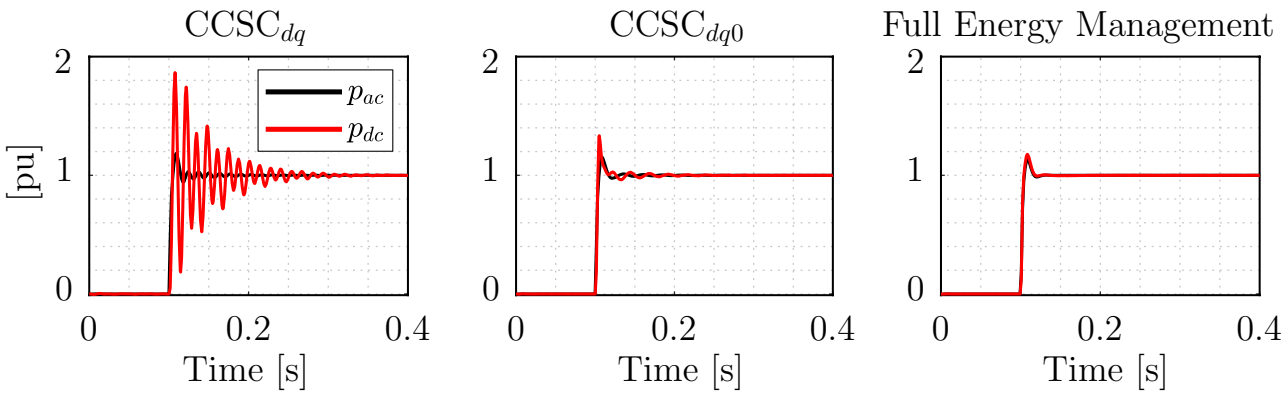


Figure 3.16 – Comparison of MMC response using open-loop and closed-loop control on its internal energy

The MMC literature has shown over the years that this part of the control clearly stays as a degree of freedom which does not prevent the converter from working properly, especially if transients are rather slow. Hence, none of these methods is unanimously accepted so far.

Proof of the need for an energy closed-loop control in EO-AAC

In this section, it is proposed to highlight the energy behaviour of the EO-AAC without energy control in case of an active power step of 1 p.u. The reference for i_{gd} and i_{dc} are based on P^*_{ac} as in (3.21).

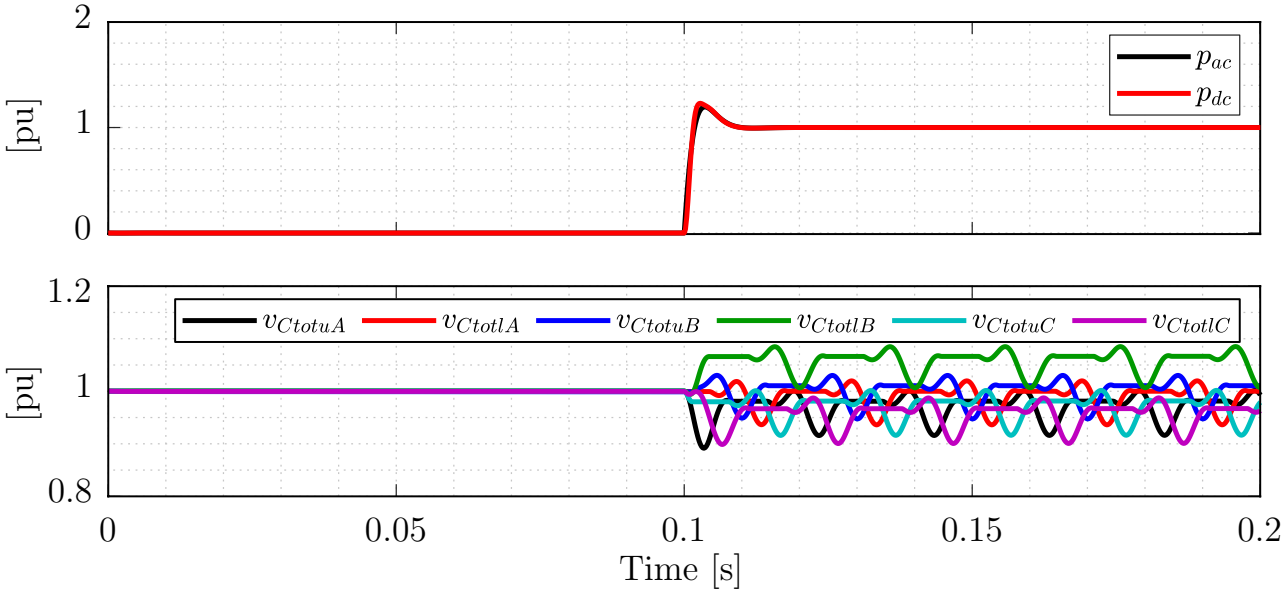


Figure 3.17 – Simulation results of an EO-AAC without energy control

As shown by Figure 3.17, due to the non-overlap mode, the energy inside the EO-AACs become unequally distributed. Hence, some stacks may be overcharged or undercharged. So, unlike the MMC which has its internal energy naturally stable, it is mandatory to derive a closed-loop control structure ensuring the power balance in each stack.

3.4.1 AACs Energy Control Review

Since the advent of the AAC topology, different approaches to maintain its internal energy stable have been proposed and described in this section. It should be noticed that most these works were originally designed for the SO-AAC, so without DC current active filtering, thus some of them are not suitable for the EO-AAC.

In [138], the use of zero sequence current has been proposed to maintain the total stored energy stable without the use of overlap period. This technique needs a star transformer in order to create a physical link between the neutral and the middle point of the DC bus as depicted on Figure 3.18.

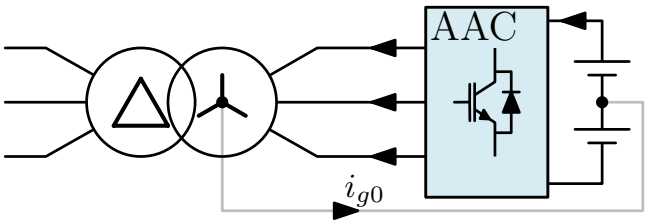


Figure 3.18 – Illustration of the energy management through common mode current

As the common mode is distributed inside each leg (and arm depending on the DS states), the distribution of the energy among stacks cannot be controlled. The middle point of the DC bus and the neutral being connected, the use of v_{N0} is dedicated to the current control. Moreover, the common mode current is composed of a third order harmonic which visible on the DC current. This control technique is therefore not suitable with the EO-AAC topology.

In the first chapter, it has been demonstrated that the energy balance depends on several parameters. One of them is the switching times of the DSs (i.e. by shifting the integral boundaries). Indeed, by modifying the switching pattern of the DS, the current can be distributed as desired and the energy as well. This is the second method, which is so far partially exploited. For instance, in [139–141] the length of the overlap period is varied to modify the exchange of energy between the leg in overlap mode and the DC bus. In [142], the combination load angle (φ) and DS switching times (δ) is used to follow the trajectory $P_u = 0$ highlighted on the Figure 1.21 in Chapter 1. In fact, they shift the energy sweet-spot where it is needed to maintain the power balance. Operation at low modulation index can be achieved to replace FB-SMs by HB-SMs. It results in a converter with low losses (even lower than HB-MMC), however, the DC-Fault blocking capability has been lost. Moreover, results that are presented focuses on inverter operation where, at the end of the conduction period the arm current is negative (800-900 A) and only diode blocking is required. In rectifier operating mode, the question of the ZCS of the transistors with such high current to be quickly cancelled should be addressed. These techniques using the switching times of the DS, are, as mentioned above, partially exploited. Indeed, the use of the angle δ and θ_{ovl} can manage the level of energy within a leg or in the converter (the total one). The way these techniques are used does not provide the balancing between upper and lower stacks. So, at least three controllers are missing to achieve the full energy management. Their impact on stack design is also questionable.

The final solution, and the one investigated in this thesis, relies on the use of the overlap current. As in the MMC, it is possible for the EO-AAC exchange power with the DC bus through the overlap current, i.e. a current that flows trough the leg in overlap mode. This type of energy controller has been studied in different works [90, 91, 120, 138] where most of

them left some of the energy variables remaining uncontrolled. Therefore, in this section a systematic modelling approach is proposed which allows building a full energy management control structure unlike the above cited works.

3.4.2 Basics of Energy Dynamic Models

The EO-AAC is composed of six stacks that are, basically, tanks of energy. Without considering DSs, the EO-AAC can be simplified in average as in Figure 3.19.

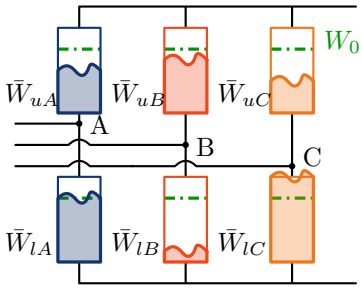


Figure 3.19 – Simplified average representation of the EO-AAC

These tanks of energy, have a nominal value to be respected in average so that:

$$\bar{W}_{uA} = \bar{W}_{lA} = \bar{W}_{uB} = \bar{W}_{lB} = \bar{W}_{uC} = \bar{W}_{lC} = W_0 \tag{3.25}$$

where $\bar{W}_{(u,l)J}$ are the average level of energy in each stack. However, as shown on Figure 3.19 and Figure 3.17, there might be differences of energy levels between two arms of the same phase-leg,

$$\bar{W}_{uJ} \neq \bar{W}_{lJ} \tag{3.26}$$

but also between two legs

$$\bar{W}_{uA} + \bar{W}_{lA} \neq \bar{W}_{uB} + \bar{W}_{lB} \neq \bar{W}_{uC} + \bar{W}_{lC} \neq 2W_0 \tag{3.27}$$

As a result, the total energy (W_{tot}) defined as the sum of all stack energies may be different from its nominal value such as

$$W_{tot} \neq 6W_0 \tag{3.28}$$

To avoid those inequalities in steady-state, and as aforementioned, six controllers are needed. A first way would consists in applying a closed-loop control on each stack energy to get an arm current reference. To derived these models let us first introduce

$$\bar{W}_{(u,l)J} = \frac{1}{2} C_{tot} V^2_{Ctot(u,l)J} \tag{3.29}$$

Thus,

$$\begin{aligned} \frac{d\bar{W}_{(u,l)J}}{dt} &= \left\langle v_{Ctot(u,l)J} \times i_{Ctot(u,l)J} \right\rangle_T \\ &= \left\langle v_{m(u,l)J} \times i_{(u,l)J} \right\rangle_T \end{aligned} \tag{3.30}$$

where T is the fundamental period and if losses in stacks of SMs are neglected. Applying this approach would lead to six arm current references including coupled AC and DC components.

However, in the above section, it has been presented that AC and DC currents are controlled instead of the arm currents. Decoupled AC and DC current references are therefore needed. To do so, stack energies combinations have been proposed in MMC literature and the same kind of modelling is presented on Figure 3.20.

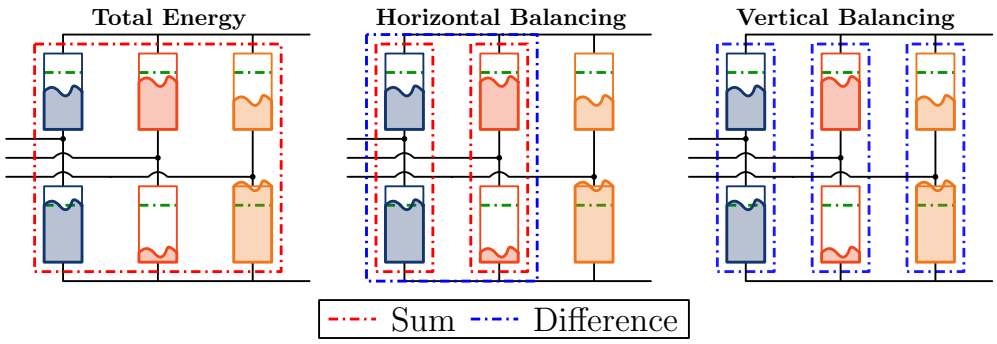


Figure 3.20 – Proposed stack energy combinations

As depicted on Figure 3.20, there are three main combinations providing six 'combined state-variables'. On the left is presented the total energy involving the sum of all stack energies. In the middle, the horizontal balancing that represent the differences of energy between two legs. Finally on the right side is illustrated the vertical balancing showing the unequal distribution of energy between arms. The aim of the following sections is to derive models and controllers for each combination.

3.4.3 Total Energy Control

The total stored energy, for any converter equipped with capacitive energy storage devices, can be written as

$$W_{tot} = \frac{1}{2} C_{tot} \sum_{J=A,B,C} v_{Ctot(u,l)J}^2 \tag{3.31}$$

from a physical point of view, the total energy interfaces the AC and DC powers. Its deviation is written as

$$\frac{dW_{tot}}{dt} = p_{dc} - p_{ac} \tag{3.32}$$

To obtain such simplified form, the following derivations are realised.

$$\frac{dW_{tot}}{dt} = \sum_{J=A,B,C} v_{m(u,l)J} \times i_{(u,l)J} \tag{3.33}$$

Applied on the circuit configuration described on Figure 3.10 gives:

$$\begin{aligned}
\frac{dW_{tot}}{dt} &= \sum_{J=A,B,C} v_{m(u,l)J} \times i_{(u,l)J} \\
&= v_{muA} i_{uA} + v_{mlA} i_{lA} + \underbrace{v_{muB} i_{uB}}_{=0} + v_{mlB} i_{lB} + v_{muC} i_{uC} + \underbrace{v_{mlC} i_{lC}}_{=0} \\
&= v_{muA} i_{uA} + v_{mlA} i_{lA} + v_{mlB} i_{lB} + v_{muC} i_{uC} \\
&= v_{mdc} \left(i_{\Sigma A} - \frac{i_{gB}}{2} + \frac{i_{gC}}{2} \right) - v_{vA} i_{gA} - v_{vB} i_{gB} - v_{vC} i_{gC}
\end{aligned} \tag{3.34}$$

where

$$i_{dc} = i_{\Sigma A} - \frac{i_{gB}}{2} + \frac{i_{gC}}{2} \tag{3.35}$$

and

$$p_{ac} = v_{vA} i_{gA} + v_{vB} i_{gB} + v_{vC} i_{gC} \tag{3.36}$$

Considering dq components of the AC side quantities and v_{mdc} closed to v_{dc} leads to a simplified model

$$\frac{dW_{tot}}{dt} = v_{dc} i_{dc} - v_{gd} i_{gd} \tag{3.37}$$

In normal operation, AC and DC powers are constant, then, the total energy is harmonics free. Thus, a measurement filter is not necessary. Moreover, this energy combination can provide a reference for i_{gd} or i_{dc} suitable with above current controllers. Both possibilities are presented.

DC power based total energy control

Obtaining a DC current reference using the total energy control needs the following scheme.

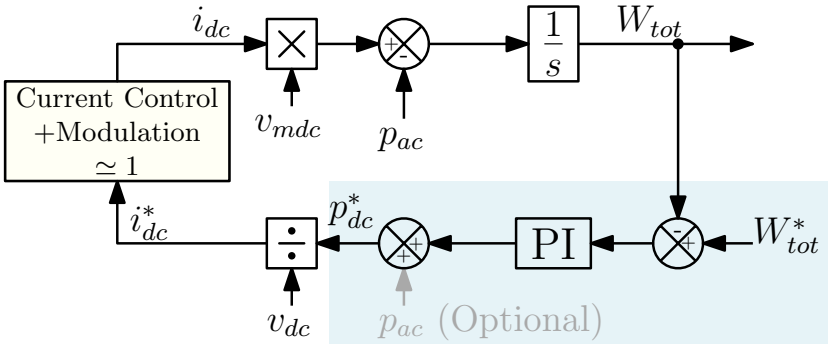


Figure 3.21 – DC power based total energy controller

As visible on Figure 3.21 the impact of the DC current dynamics is neglected, since, the principle of cascaded loops imposes the external controllers to be much slower than the internal ones to avoid interactions between them. In that case, this is the interaction between current and energy closed-loop poles. According to Table 3.2, the response time of the DC current control is 1 ms, then, the total controller dynamics is set to 50 ms and its damping ratio equals to 1. The feed-forward compensation of p_{ac} in the control is optional. Depending on whether it is compensated or not, in case of active power transient the dynamics response of the total energy will be different since the controller will have to compensate with its own dynamics. In the following, this disturbance will compensated to limit the effort of the controller.
The simulation case is

1. at 0.05 second, an active power ramp of 1 GW / 50 ms
2. at 0.15 second, a step change on the total energy reference from 1 to 1.1 p.u.

and results are presented on Figure 3.22 where the AC and DC active powers and currents are presented on the two first graphs. The last one presents the six v_{Ctot} and the total energy W_{tot}. During the power ramping, stack energies are kept stable and almost balanced, W_{tot} remains around 1 p.u.
.

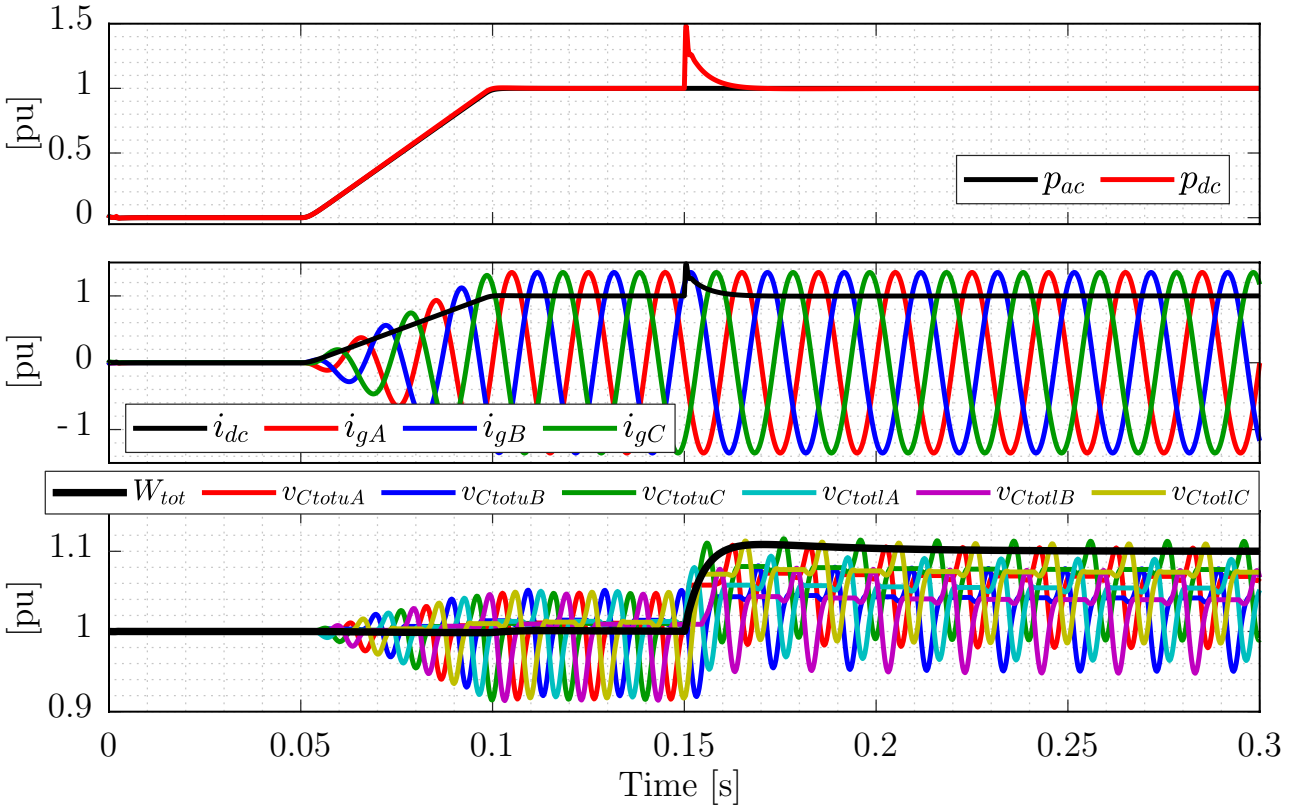


Figure 3.22 – Simulation results of DC power based total energy controller

During the step change on W_{tot}^*, the controller asks for the DC bus to provide the power so that W_{tot} can reach its new reference value. High DC current spike is observed due to the proportional gain and then the integral part ensure the zero steady-state error within the expected dynamics. This fast transient on W_{tot}, and by extension p_{dc}, results in an unbalance of energy between each stack.

AC power based total energy control

The total energy control through the AC side power is achieved using the scheme of Figure 3.23.

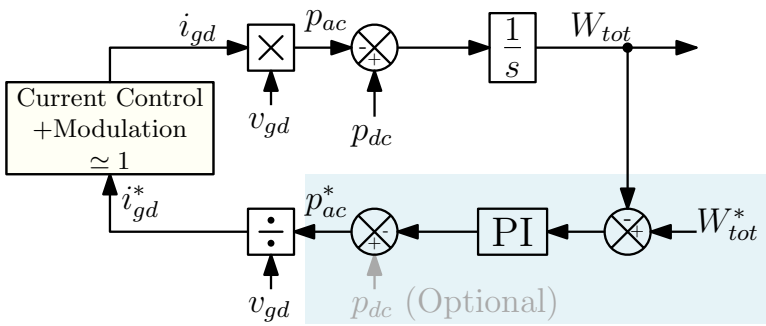


Figure 3.23 – AC power based total energy controller

The current loops and the modulation are supposed to be ideal, then, there are assimilated to an unitary gain in the derivation of the total energy controller. Compared to the DC power based controller, the AC current controllers are slower (i.e. 5 ms while the DC is controlled

in 1 ms) but the dynamics of the total energy control loop is still set to 50 ms. Results are presented on Figure 3.24, where it is clearly visible that the total energy is more oscillating during the disturbance reject due to the slower response time of the current control. During the step change on the energy reference, the dynamics of the total energy control loops is very similar to the previous case. Thus, the only differences between both techniques would lie in the current control dynamics, the disturbance reject and, in practice, the PLL dynamics which is neglected here since the converter is connected to an infinite AC source.

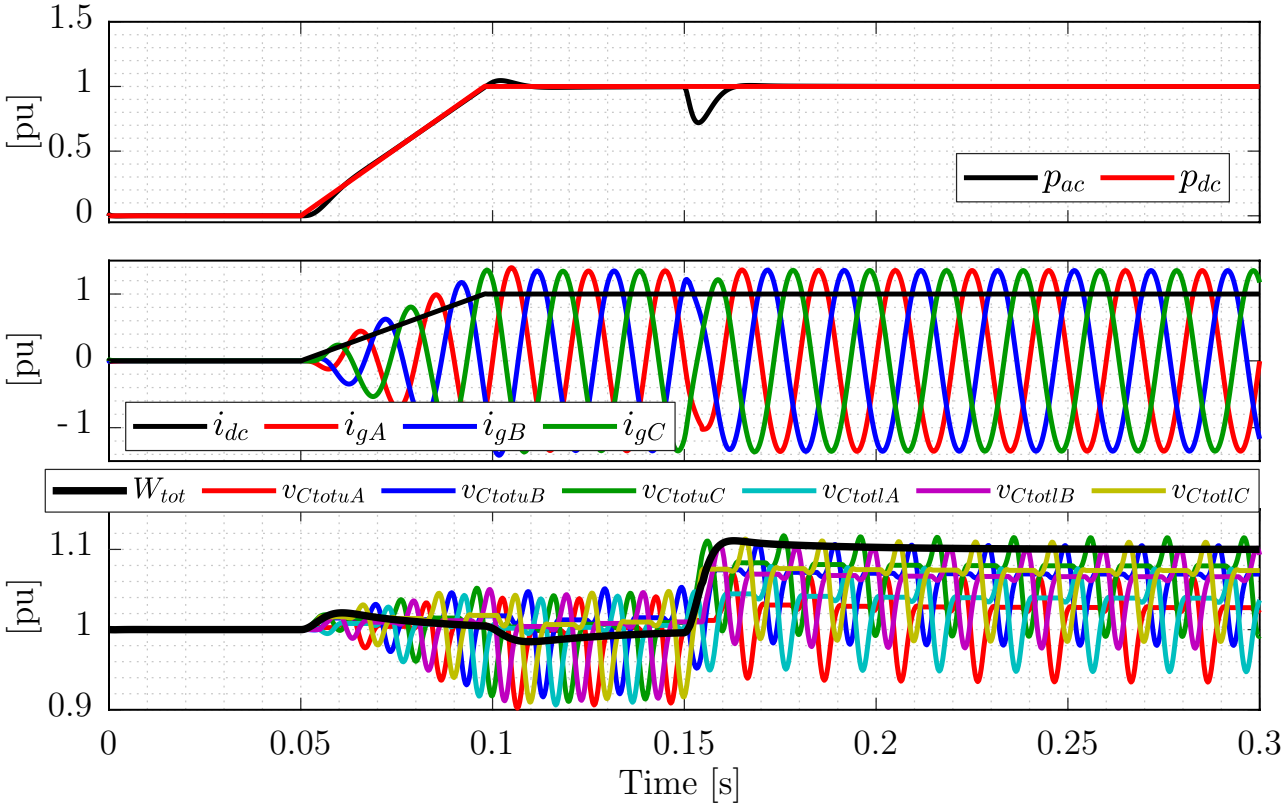


Figure 3.24 – Simulation results of AC power based total energy controller

Two total energy control options have been presented. However, under severe events (e.g. brutal load/generator disconnection) stack energies become unbalanced requiring the implementation of the horizontal and vertical balancing controllers.

3.4.4 Horizontal Balancing

The principle of the horizontal balancing consists in the correction of the energy level differences between two legs. The energy deviation within a single leg must therefore be derived. Let us introduce the single-phase notation W_Σ such as

$$W_\Sigma = \frac{1}{2} C_{tot} \left(v_{Ctotu}^2 + v_{Ctotl}^2 \right) \tag{3.38}$$

Its deviation can be expressed as it follows

$$\frac{dW_\Sigma}{dt} = v_{mu} i_u + v_{ml} i_l \tag{3.39}$$

which involves the sum of the power flowing through the upper and lower stacks. Unlike the total energy model, single-phased representation contains even order harmonics (essentially at

twice the grid frequency) requiring the average modelling to focus on the single-phased AC and DC active powers. Thus,

$$\frac{d\bar{W}_{\Sigma}}{dt} = \frac{1}{2\pi}\int_{0}^{2\pi} \left(v_{mu}i_{u} + v_{ml}i_{l}\right)\ \mathrm{d}\theta_{g} \tag{3.40}$$

where $\bar{W}_{\Sigma}$ is an average value over the fundamental period (T). In the first chapter, the average power through one upper stack has already been calculated and its expression recalled below.

$$\frac{d\bar{W}_{u}}{dt} = \frac{v_{dc}I_{g}}{\sqrt{2}\pi}\cos(\delta+\varphi)\cos\left(\frac{\theta_{ovl}}{2}+\varphi\right) - \frac{V_{v}I_{g}}{2}\cos(\theta_{v}-\varphi) + \frac{v_{dc}}{2}i_{\Sigma}\left(\frac{\theta_{ovl}}{\pi}\right) \tag{3.41}$$

Considering the operation of the upper and lower arms symmetrical, then, the average power through the lower stack is the same. To simplify the model some assumptions can be done such as $\delta = \theta_v$ and V_v closed to V_g, so that a simplified expression is obtained

$$\frac{d\bar{W}_{\Sigma}}{dt} = v_{dc}i_{\Sigma}\left(\frac{\theta_{ovl}}{\pi}\right) + P_{ac}\left(\frac{4}{m\pi}\cos\left(\frac{\theta_{ovl}}{2}\right) - 1\right) \tag{3.42}$$

Due to single-phased modelling, P_{ac} is not the three phase active power. The model (3.42), shows that the energy within a leg can be either controlled through the overlap current i_{Σ} or the grid current i_g. So basically, through the DC or the AC active power. However, the sum of these three levels of energy is equal W_{tot} which is already controlled as detailed in the above section. So, it is not possible to control each leg energy in a decoupled way. For this reason, it is mandatory to have a control of the energy difference between two legs. Let us introduce:

$$\begin{aligned} W_{\Sigma x} &= W_{\Sigma A} - W_{\Sigma B} \\ W_{\Sigma y} &= W_{\Sigma A} - W_{\Sigma C} \end{aligned} \tag{3.43}$$

Only two models and controllers are necessary since the energy difference between legs generates two independent state-variables. As a result, all variables in (3.42) are transformed in xy variables:

$$\begin{aligned} P_{acx} &= P_{acA} - P_{acB} \\ P_{acy} &= P_{acA} - P_{acC} \end{aligned} \tag{3.44}$$

and

$$\begin{aligned} i_{\Sigma x} &= i_{\Sigma A} - i_{\Sigma B} \\ i_{\Sigma y} &= i_{\Sigma A} - i_{\Sigma C} \end{aligned} \tag{3.45}$$

To generate decoupled references, it is necessary to inverse the transformation. To be reversible, a third axis is needed and called z. The complete transformation is therefore called $\mathbf{T}_{xyz}$ and defined as

$$\mathbf{T}_{xyz} = \begin{bmatrix} 1 & -1 & 0 \\ 1 & 0 & -1 \\ 1 & 1 & 1 \end{bmatrix} \tag{3.46}$$

and leads to:

$$\begin{aligned} \frac{d\bar{W}_{\Delta x}}{dt} &= v_{dc}i_{\Sigma x}\left(\frac{\theta_{ovl}}{\pi}\right) + P_{acx}\left(\frac{4}{m\pi}\cos\left(\frac{\theta_{ovl}}{2}\right) - 1\right) \\ \frac{d\bar{W}_{\Delta y}}{dt} &= v_{dc}i_{\Sigma y}\left(\frac{\theta_{ovl}}{\pi}\right) + P_{acy}\left(\frac{4}{m\pi}\cos\left(\frac{\theta_{ovl}}{2}\right) - 1\right) \end{aligned} \tag{3.47}$$

From (3.47) two control outputs are possible. Basically, both solution generate single-phased active power unbalance so that, transiently, the energy can be evenly distributed inside each leg. Both solutions are presented.

First solution : DC overlap current

Considering the AC side balanced, then, the model described in (3.47) can be simplified as:

$$\begin{aligned}\frac{d\bar{W}_{\Delta x}}{dt} &= v_{dc} i_{\Sigma x}\left(\frac{\theta_{ovl}}{\pi}\right)\\ \frac{d\bar{W}_{\Delta y}}{dt} &= v_{dc} i_{\Sigma y}\left(\frac{\theta_{ovl}}{\pi}\right)\end{aligned} \tag{3.48}$$

To avoid the product $v_{dc} \times i_{\Sigma(x,y)}$ to be zero, these currents must be composed of a DC component. For this reason, these current are now noted $i^{dc}_{\Sigma(x,y)}$. There is only one leg in overlap mode, meaning that the references of these currents must be decoupled. The inverse transformation of $\mathbf{T}_{xyz}$ with a little refinement is used.

$$\begin{bmatrix}\Delta i^*_{\Sigma A}\\ \Delta i^*_{\Sigma B}\\ \Delta i^*_{\Sigma C}\end{bmatrix} = \mathbf{T}^{-1}_{xyz}\begin{bmatrix}i^{dc*}_{\Sigma x}\\ i^{dc*}_{\Sigma y}\\ 0\end{bmatrix} = \begin{bmatrix}1/3 & 1/3 & 1/3\\ -2/3 & 1/3 & 1/3\\ 1/3 & -2/3 & 1/3\end{bmatrix}\begin{bmatrix}i^{dc*}_{\Sigma x}\\ i^{dc*}_{\Sigma y}\\ 0\end{bmatrix} \tag{3.49}$$

Since the horizontal balancing role is to adjust single-phased active powers, then, in abc frame these references are "small" variations noted $\Delta i_{\Sigma J}$. The z axis reference is set to zero since, it can be demonstrated that the sum of Δi_{gJ} is zero. However, on the DC side, only one current is controllable, i_{dc}. Thus, to modify the active power through one leg, it is mandatory to act on i_{dc}. Then, the DC current reference is modified so that

$$i^*_{dc} = i^*_{dc,W_{tot}} + \Delta i^{dc*}_{\Sigma J} \tag{3.50}$$

where $i^*_{dc,W_{tot}}$ is the reference calculated by the total energy control and $\Delta i^{dc*}_{\Sigma J}$ the additional DC component used to regulate the energy specifically in the leg in overlap mode. Considering the total energy control using the DC side power, then it would results in the following control scheme and DC current reference generation where the reference selection for the horizontal balancing is highlighted by the selector in grey frame.

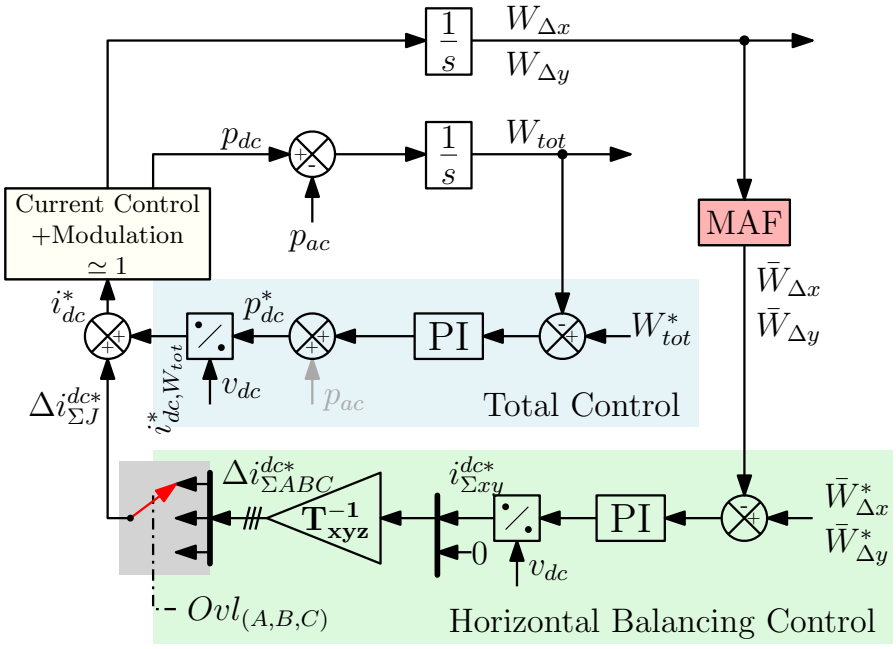


Figure 3.25 – Model and Control structure of DC power based Horizontal balancing

The extraction the average deviation of $\bar{W}_{\Delta x}$ and $\bar{W}_{\Delta y}$ needs a filter to avoid harmonics in current references (but also to focus on the active powers). The discrete Moving-Average-Filter (MAF) has been chosen for its ability to remove any harmonics from signals even if its output delay can be large [143]. This delay depends on the harmonics order to be filtered, the length of the sliding window etc... To limit this delay, the window is derived based on lowest harmonic order in the energy measurement. Balancing controls are performed over several fundamental periods which is larger than the filter delay.

According to (3.50) and Figure 3.25, the balancing controllers generate three current references with different magnitudes, but, only one at any time is taken into account by the DC current controller. During transients, these difference of magnitude will affect the DC current reference as shown Figure 3.26.

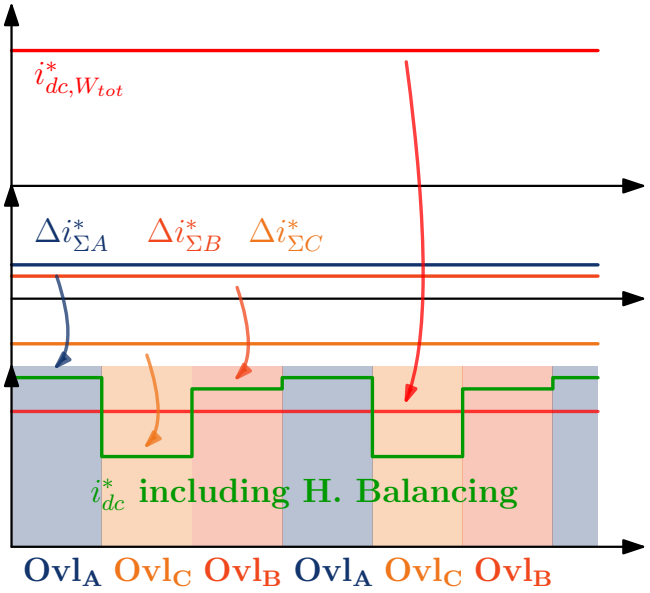


Figure 3.26 – Illustrated of the DC current ripple introduced by DC power based Horizontal Balancing

As shown this illustration, depending on the leg in overlap mode (modelled by the selector framed in grey) the DC current reference contains an additional time-varying DC offset which becomes zero in steady-state. This figure presents the main principle where DC overlap current references are constant during the whole fundamental period. During transient it is not. Moreover, to be effective, this control needs the DC current to reach steady-state before the next rotation of the overlap mode. The overlap period being equals to 60 degrees, so 3.333 ms for 50 Hz AC grid, the DC current control response should be faster than this value. This constraint explains the reason why, during the validation of the current controllers, AC side dynamics were 5 ms while de DC side was fixed to 1 ms.

To validate the horizontal balancing control a time domain simulation has been performed. The simulated scenario is similar to the one of the total energy. First, a power ramp is applied in order to reach the nominal operating point and then, a step change on the references $\bar{W}^*_{\Delta(x,y)}$. The step change involves a difference of energy level between leg A and B ($\bar{W}^*_{\Delta x}$) of 0.05 p.u and between A and C ($\bar{W}^*_{\Delta y}$) of 0.1 p.u. The control loops gains are computed on the basis of a response time of 100 ms with a damping ratio of 0.7.

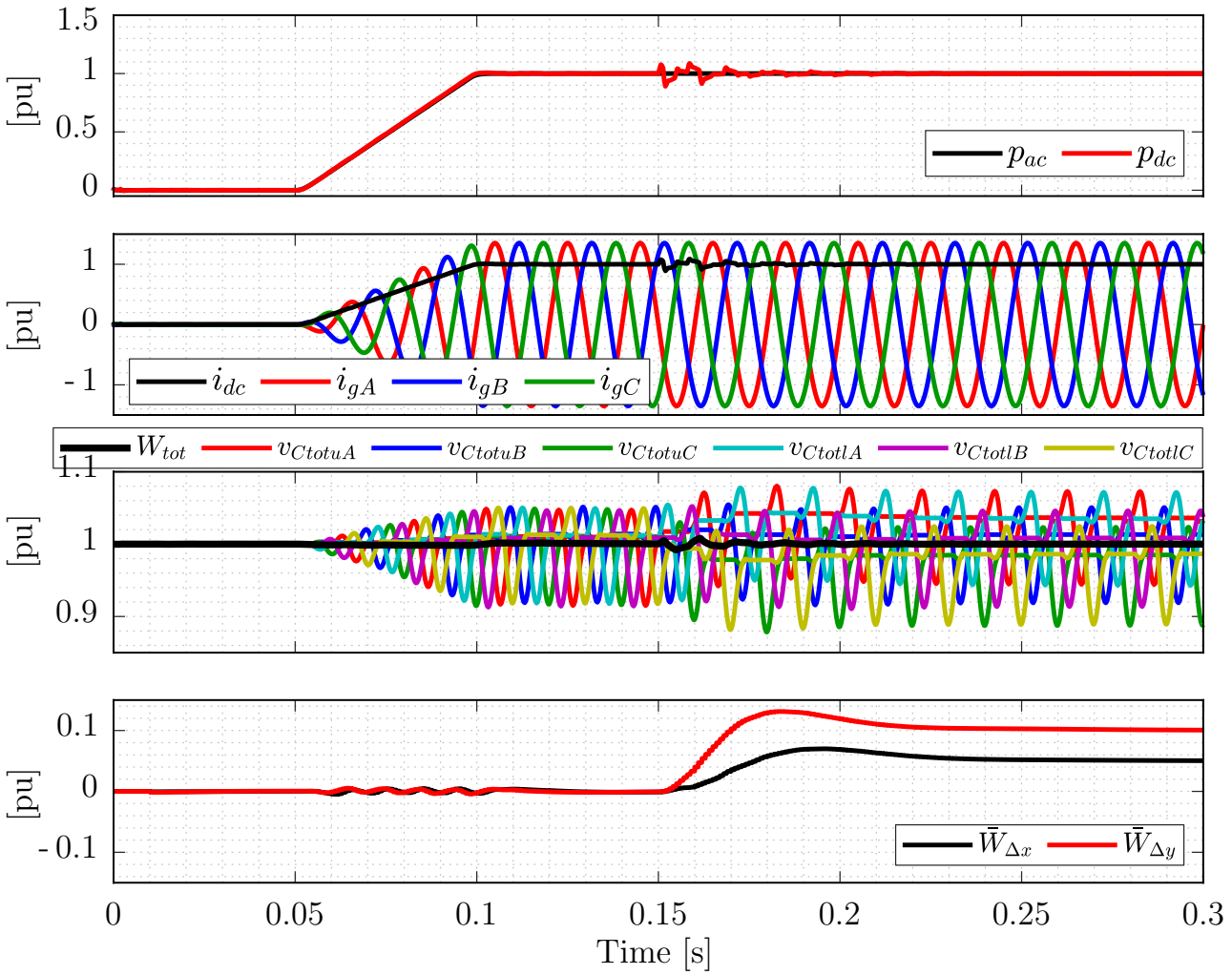


Figure 3.27 – Validation of DC power based Horizontal balancing

The simulation results are presented on Figure 3.27. The last graph of this figure presents $\bar{W}_{\Delta x}$ and $\bar{W}_{\Delta y}$. During the power ramping these quantities are kept stable and some oscillations are observed. The transient of the energy filters is responsible of this unfiltered harmonics which nonetheless are suppressed in steady-state. At the step change on energy references, balancing controller computes the appropriate references $i^*_{\Sigma J}$ so that an imbalance of energy appears between the three legs. Thus, within 100 ms, $\bar{W}_{\Delta x}$ and $\bar{W}_{\Delta y}$ reach their references and, as shown on the third graph, v_{Ctot} of each leg have different values.

During the step change on the energy references, the ripple introduced by this control technique is highly visible, and, inevitable with such approach. However, such test case is not expected to be used in real cases, so, as most of the time power ramping is performed then even in transient the DC current is almost without harmonics caused by the control.

Second solution : Injection of negative sequence current

Instead of using the DC side power, the second solution generates a transient unbalance on the AC currents. In that case, the average values of each overlap current is assumed to be balanced as well as v_g. These assumptions allow simplifying (3.47) such as:

$$\begin{aligned}\frac{d\bar{W}_{\Delta x}}{dt} &= V_g I_{gx}\left(\frac{4}{m\pi}\cos\left(\frac{\theta_{ovl}}{2}\right)-1\right)\\ \frac{d\bar{W}_{\Delta y}}{dt} &= V_g I_{gy}\left(\frac{4}{m\pi}\cos\left(\frac{\theta_{ovl}}{2}\right)-1\right)\end{aligned} \tag{3.51}$$

As the horizontal balancing adjust the single-phased active power, then, $I_{g(x,y)}$ are defined by

$$\begin{aligned}I_{gx} &= \Delta I_{gA} - \Delta I_{gB}\\ I_{gy} &= \Delta I_{gA} - \Delta I_{gC}\end{aligned} \tag{3.52}$$

where ΔI_{gJ} is the unbalanced part of the real components of the AC current. With such control techniques, zero sequence current reference is generated but the Δ arrangement of the transformer prevent from having this component. Thus, similarly to MMC or Modular STATCOM [144–146] a modification of the current reference has been performed in order to suppress the zero sequence component. In this thesis, it is done as it follows. First, the controllers generates RMS current references which are transformed into sinusoidal references using $\mathbf{Z}$:

$$\mathbf{Z} = \sqrt{2}\begin{bmatrix}\sin(\theta_g) - \sin(\theta_g - \frac{2\pi}{3}) & 0\\ 0 & \sin(\theta_g) - \sin(\theta_g + \frac{2\pi}{3})\end{bmatrix} \tag{3.53}$$

so that

$$\begin{bmatrix}i^*_{gx}\\ i^*_{gy}\end{bmatrix} = \mathbf{Z}\begin{bmatrix}I^*_{gx}\\ I^*_{gy}\end{bmatrix} \tag{3.54}$$

Then, the inverse transformation of xyz is reapplied by setting the z axis to zero as illustrated on Figure 3.28.

The control structure of the AC side power based horizontal balancing gives references for the AC currents in abc frame which then transformed into dq references in order to be controlled. No sequence decomposition has been used meaning that there will be oscillation at twice the grid frequency on dq components. Note that in this figure the total energy control is based on DC side power, a full AC power based approach is also possible.

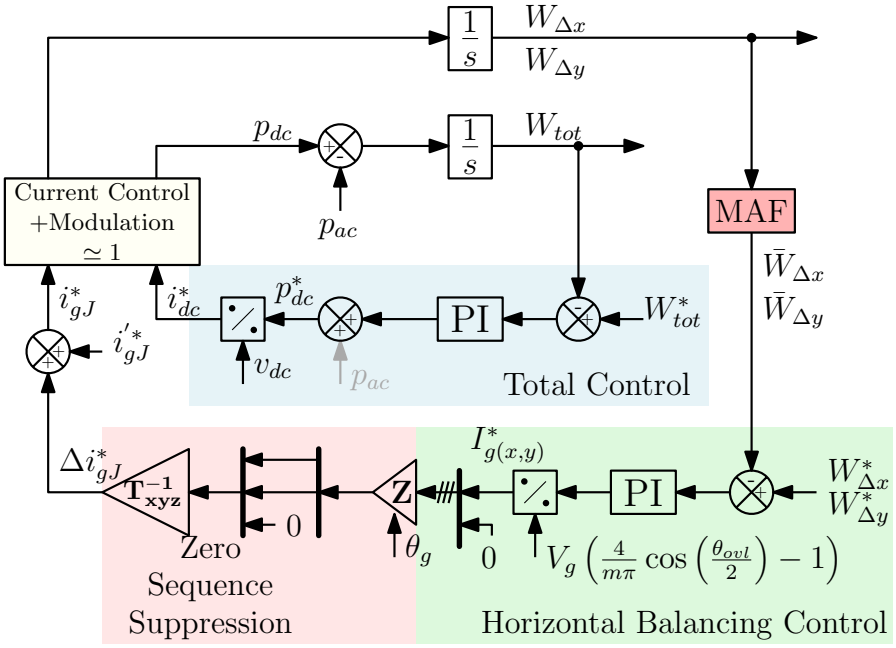


Figure 3.28 – Model and Control structure of the AC power based Horizontal balancing

The dynamic behaviour is now tested under the same scenario than the DC power based control. Results are presented on Figure 3.29. The first graph of this figure shows AC and DC active powers, where, a second harmonic clearly appears due to the unbalanced AC current references. Regarding the dynamics of the control, it is visible at the step change on the energy reference for $\bar{W}_{\Delta x}$ and $\bar{W}_{\Delta y}$ provides similar behaviour than the DC power based approach.

Discussion on Horizontal Balancing

This section has presented two main approaches in the derivation of a control structure achieving the horizontal balancing. Both structures have a common point which is the transient injection of active power oscillations. The DC power based approach appears as being very simple in terms of implementation but require fast response time for the DC current to be effective. It should be less than the overlap period. On the other hand, the AC power approach allows to have continuous control of these dynamics, however, unbalanced currents are required. In the following the DC power based approach is used to avoid the generation of unbalanced current for the purpose of energy balancing in normal operation. However this solution reveals to be interesting and effective in case of DC-Fault as reported in [146] if the DC bus is no more available to exchange energy.

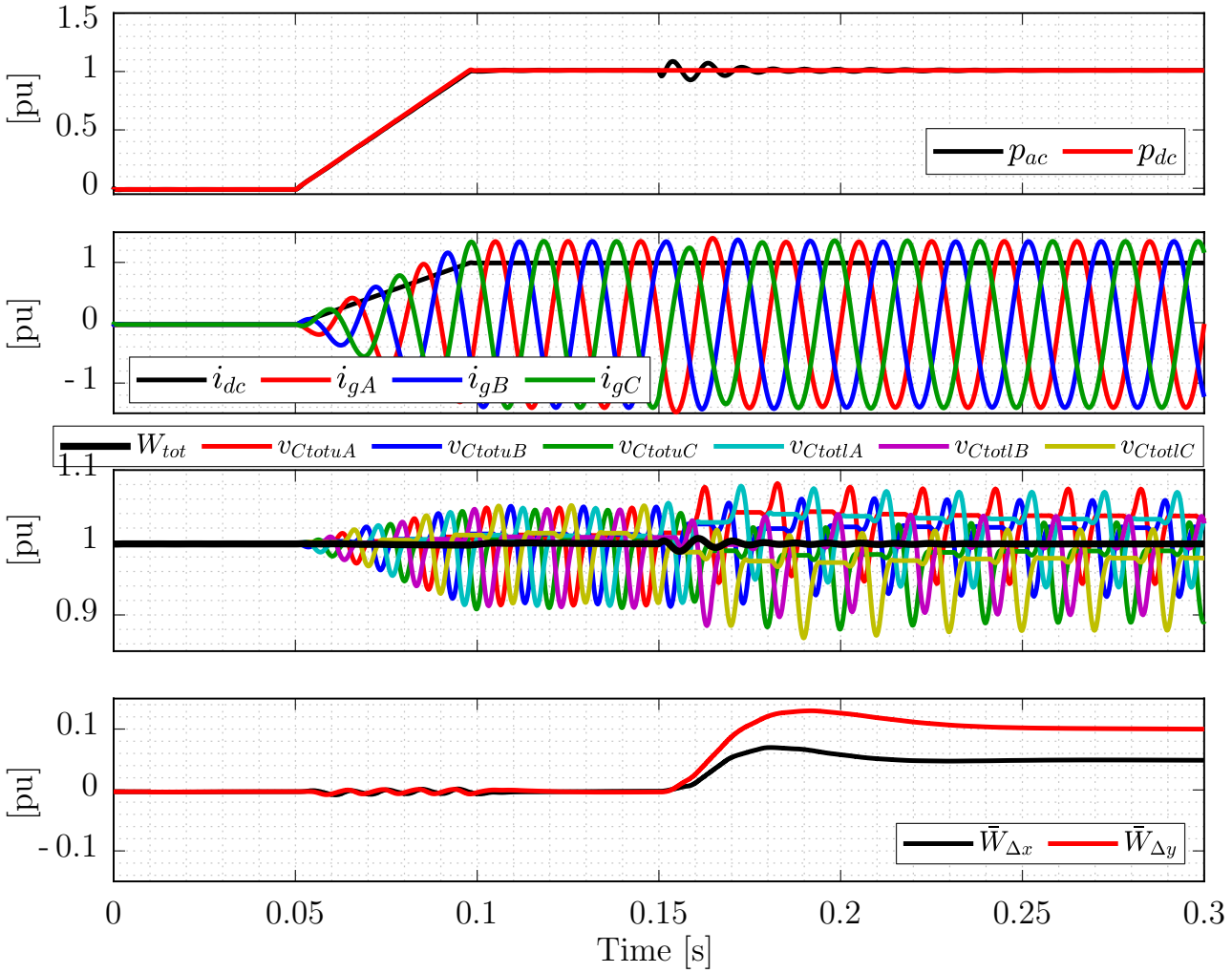


Figure 3.29 – Results of AC side power based Horizontal balancing controller

3.4.5 Vertical Balancing

Three energy controllers have been derived so far. Three other are therefore needed to keep in balance upper and lower stacks which is aim of the vertical balancing. As depicted on Figure 3.20, the vertical balancing control is done through a single-phased approach unlike the previous ones. However, according to (3.42), the average energy deviation within stacks is the same for the uppers and lowers, so, their difference is theoretically zero. To control this difference, it means that new components in the arm quantities are needed. For instance, in MMC literature it is well known that circulating currents can be composed of DC and AC components allowing to manage different variables at the same time. To apply the same principle, let us achieve a very simple analysis. If the overlap mode is assumed, then, the power flowing through the upper and lower stacks is:

$$\begin{aligned} \frac{dW_u}{dt} &= \left(\frac{v_{mdc}}{2} - v_v - v_{N0}\right) \times \left(i_\Sigma + \frac{i_g}{2}\right) \\ \frac{dW_l}{dt} &= \left(\frac{v_{mdc}}{2} + v_v + v_{N0}\right) \times \left(i_\Sigma - \frac{i_g}{2}\right) \end{aligned} \tag{3.55}$$

Introducing W_Δ as the difference of energy between two upper and lower stacks yields

$$\frac{dW_\Delta}{dt} = v_{mdc} i_g - 2 v_v i_\Sigma - 2 v_{N0} i_\Sigma \tag{3.56}$$

To achieve the energy management, the generation of active power exchanged between upper and lower stacks is mandatory. Then, one of these terms of Equation (3.56) must have its average value different from zero. It means:

1. $\langle v_{mdc} i_g \rangle_T \neq 0$ involving a DC zero sequence component in grid currents
2. $\langle -2 v_v i_\Sigma \rangle_T \neq 0$ involving an AC component in overlap currents
3. $\langle -2 v_{N0} i_\Sigma \rangle_T \neq 0$ involving a DC component in zero sequence voltage

The above requirements show that an interaction between the AC and DC side quantities is needed. It is either required to inject an AC component in the overlap current or a DC component in the AC side quantities. The use of the DC zero sequence current is avoided. The injection of a DC component in v_{N0} needs to study the impact on the transformer, protections and the grounding of HVDC stations. Thus, it remains the AC component in the overlap current. In the following i_Σ will be composed of a DC component to achieve the horizontal (i_Σ^{dc}) and and AC one named i_Σ^{ac}.

As a first solution, to achieve this vertical balancing, the AC component in the overlap current is assumed to be sinusoidal at the fundamental frequency.

$$\begin{aligned} \frac{d\bar{W}_{\Delta J}}{dt} &= -2 \left\langle \hat{V}_{vJ} \sin(\theta_g + \theta_v) \times \hat{I}_{\Sigma J}^{ac} \sin(\theta_g + \varphi_\Sigma) \right\rangle_T \\ &= -2 V_{vj} I_{\Sigma j}^{ac} \cos(\theta_v - \varphi_\Sigma) \end{aligned} \tag{3.57}$$

To minimize current magnitudes, it is wise to keep i_Σ^{ac} aligned with v_v in order to avoid useless reactive current. So, $\varphi_\Sigma = \theta_v$. As presented in [80, 83] this is the same principle for MMC. To illustrate this idea, the following simulation result is based on injection of sinusoidal AC component in overlap currents. The controller is tested against an active power step of 0.5 p.u. under an initial operating point of 0.5 p.u. The expected response time is 100 ms.

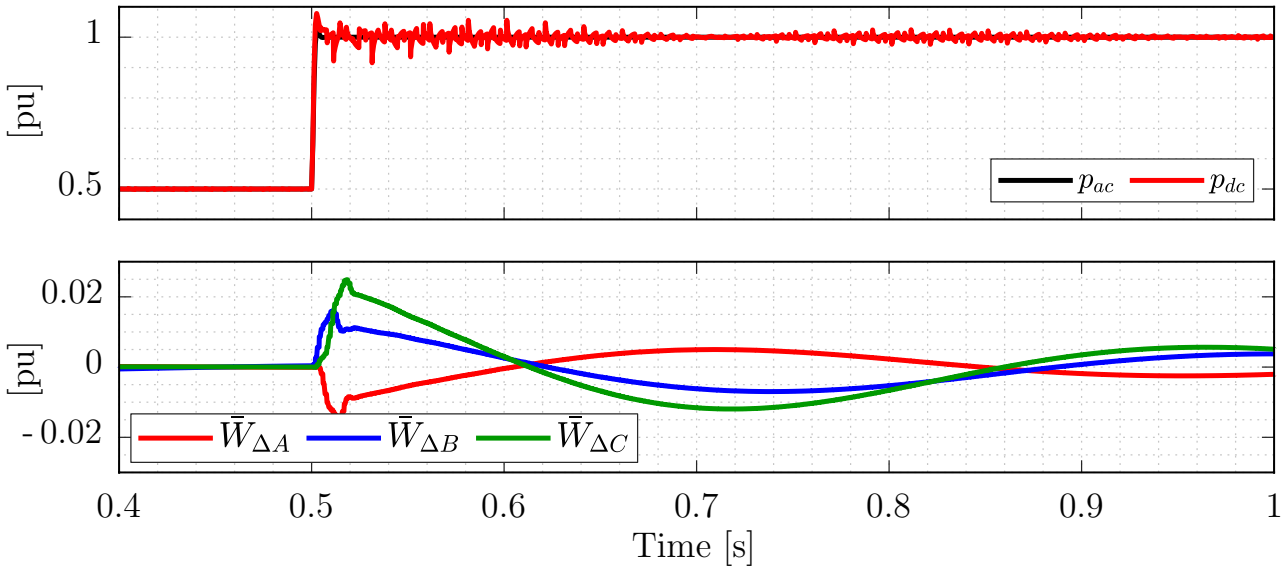


Figure 3.30 – Simulation of EO-AAC including MMC Vertical balancing controllers

The results of Figure 3.30 shows that upper and lower are getting balanced, however, the dynamics is absolutely not respected. Let us describe the issue with sinusoidal AC components.

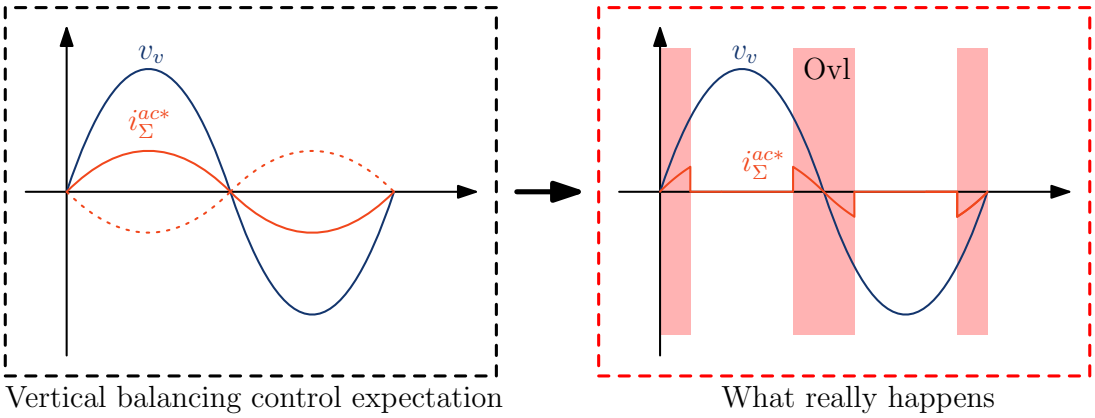


Figure 3.31 – Illustration of the AC overlap current reference generation with sinusoidal AC components

As illustrated by Figure 3.31, deriving the vertical balancing model using AC components at the grid frequency supposes that this current can flow through the leg during the entire period. However, the overlap period being fixed to 60 degrees.Therefore, it is required to derive a model considering the effective period of the AC component. Since the energy is controlled two times in a period (i.e. two overlap periods), a simple adaptation gain is necessary:

$$\frac{d\bar{W}_{\Delta J}}{dt} = -2V_{vj}I_{\Sigma j}^{ac}\left(\frac{\theta_{ovl}}{\pi}\right) \tag{3.58}$$

To compensate the discontinuity of the energy controllers, the magnitude of the AC component is increased by 3.

To maximize the power transfer with a reduced signal magnitude, the use of crest factor criterion is useful to find the best waveform. The crest factor (CF) is defined as it follows for a signal noted s

$$\mathrm{CF} = \frac{|\hat{s}|}{s_{RMS}} \tag{3.59}$$

According to this criterion, a square waveform has a CF of 1 since the RMS value of alternative square waveform is equal to its amplitude. This was indicated in [19,147]. Graphically it gives:

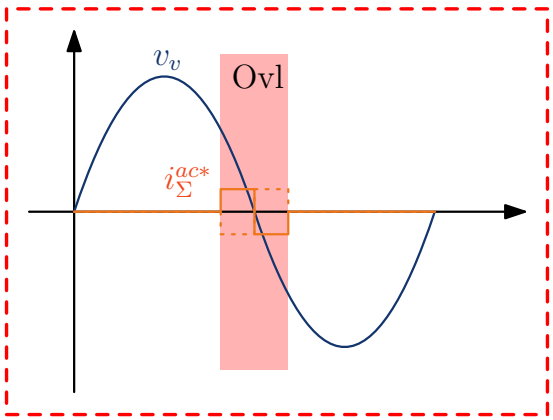


Figure 3.32 – Illustration of the vertical balancing principle using square waveform AC component in overlap current

Based on Figure 3.32, the energy deviation between upper and lower stacks in average value can be derived

$$\begin{aligned}\frac{d\bar{W}_{\Delta}}{dt} &= \frac{1}{\pi}\left(\int_{-\delta-\frac{\theta_{ovl}}{2}}^{-\delta} -2\hat{V}_v \sin(\theta_g+\theta_v) i_{\Sigma}^{ac} \mathrm{d}\theta + \int_{-\delta}^{-\delta+\frac{\theta_{ovl}}{2}} 2\hat{V}_v \sin(\theta_g+\theta_v) i_{\Sigma}^{ac} \mathrm{d}\theta_g\right) \\ &= \frac{-4\hat{V}_v i_{\Sigma}^{ac}}{\pi}\left(1-\cos\left(\frac{\theta_{ovl}}{2}\right)\right)\end{aligned} \tag{3.60}$$

Finally,(3.60) presents the model describing the energy deviation between upper and lower stacks in case square wave formed AC overlap current. Before introducing the control structure, it is important to note that, due to the sequential behaviour of the EO-AAC, this AC component is visible on the DC current as for horizontal balancing current. So, the reference $i_{\Sigma J}^{ac*}$ is added to the actual DC current reference such as:

$$i_{dc}^{*} = i_{dc,W_{tot}}^{*} + \Delta i_{\Sigma J}^{dc*} + i_{\Sigma J}^{ac*} \tag{3.61}$$

Using this equation allows determining the control structure.

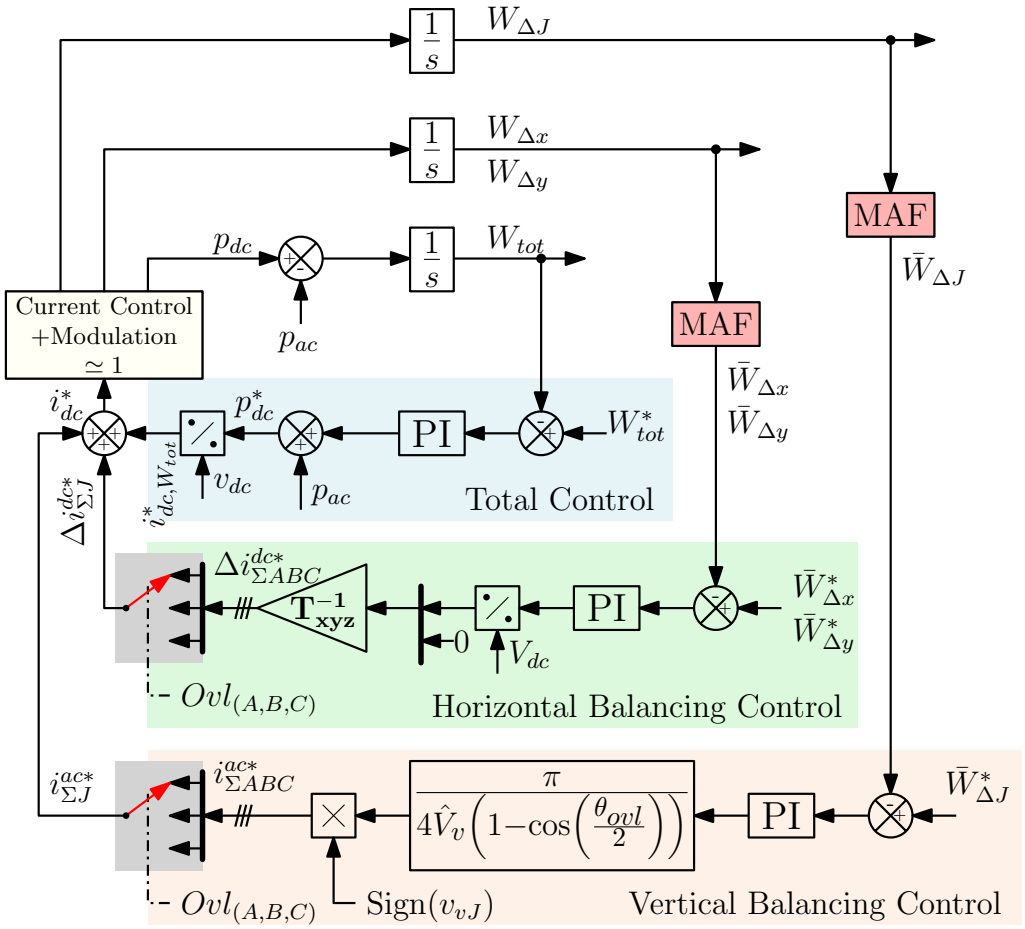


Figure 3.33 – Models and DC power based full energy management control structure of the EO-AAC

The control structure illustrated on Figure 3.33 considering the AC component in the overlap current shows that through one single current three main functions are achieved: the total energy control, the horizontal and vertical balancing. For this latter, to generate the alternative waveform of $i^{ac}_{\Sigma J}$ in phase with its respective v_{vJ}, the current reference is multiplied by a sign function applied on v_{vJ}. This complete control structure allows maintaining stable the energy inside the converter even in case of large disturbance as it will be demonstrated in the following simulation.

First of all, the vertical balancing controllers are proposed to be validated under a similar scenario as the other controllers. A power ramping is first applied, then, a step change on $\bar{W}^{*}_{\Delta J}$ is applied. The dynamics of this control is fixed 200 ms and its damping ratio to 0.7. After the step change on energy references, $\bar{W}_{\Delta A} = 0.05$ p.u, $\bar{W}_{\Delta B} = 0$ p.u and $\bar{W}_{\Delta C} = -0.05$ p.u. Simulation results are presented on Figure 3.34.

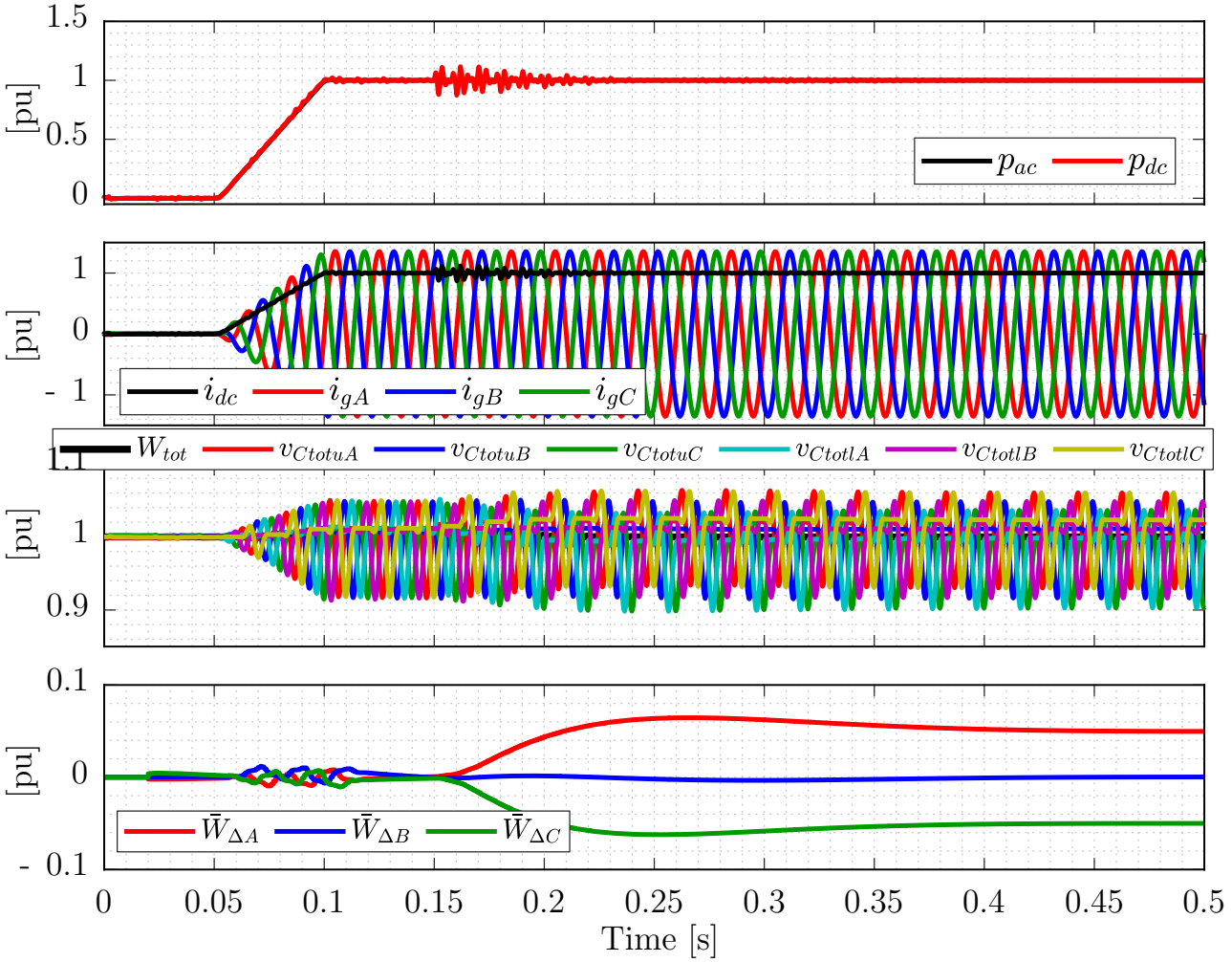


Figure 3.34 – Simulation of the EO-AAC including Vertical balancing controllers

During the power ramping, all stacks are kept stable through the combined actions of the full energy management structure. As shown the last graph, $\bar{W}_{\Delta J}$ are maintained around zero despite transient on active power. Some oscillations due to transient on energy filters are observed. At 0.15 second, the step change on energy reference is applied, and references are tracked with the expected dynamics (i.e. about 200 ms). However, as for the horizontal balancing, the DC current must be transiently disturb to transfer energy between upper and lower stacks. The faster is the transient, the more it will be necessary the balance upper and

lower stacks and the higher will be this DC current disturbance.

Nonetheless, in case of power ramping (which is more likely to occur in real application) the DC current ripple is very small.

3.5 On Dynamic Equivalence between EO-AAC and MMC

Some AAC studies have presented results about the comparison on steady-state quantities and transient behaviour [148, 149] of MMC and AAC. However, all these studies are based on the topology including short overlap which is impacted by the dynamics of the passive DC filter. As a full dynamics control for EO-AAC has been developed in this chapter, a fair comparison with the MMC on dynamic events is possible. So far, it is admitted that MMC is known for being extremely robust and dynamically powerful thanks to its high degree of controllability.

3.5.1 Recall of MMC's Dynamics Modelling and Control

The AC side dynamics of a MMC is very similar to the EO-AAC since each stacks participate to the AC voltage modulation. This dynamics is governed by the following single-phased model

$$v_v = v_g + \left(L_L + \frac{L_{arm}}{2}\right)\frac{di_g}{dt} + \left(R_L + \frac{R_{arm}}{2}\right)i_g + v_{N0} \tag{3.62}$$

The presence of arm inductors increases the overall AC side impedance in open-loop. Regarding the DC side, there is real difference between both converters. Indeed, the MMC is able to control each of the DC components that flow inside legs. This is given by the next single-phased model

$$v_\Sigma = \frac{v_{dc}}{2} - L_{arm}\frac{di_\Sigma}{dt} - R_{arm}i_\Sigma \tag{3.63}$$

Leading to 5 independent state-variables related to the arm currents. Two dq components for the AC side, and three DC components. As a recall, only three state-variables can be controlled at the same time in the EO-AAC: two dq components and the DC current.

Regarding the energy dynamics, the same energy combinations can be performed to decouple total, horizontal and vertical balancing controllers. The DC power is assumed to be used for the energy management.

$$\frac{dW_{tot}}{dt} = p_{dc} - p_{ac} \tag{3.64}$$

Then, the horizontal balancing is still applied using the xyz transformation.

$$\begin{aligned}\frac{d\bar{W}_{\Delta x}}{dt} &= v_{dc}i^{dc}_{\Sigma x}\\ \frac{d\bar{W}_{\Delta y}}{dt} &= v_{dc}i^{dc}_{\Sigma y}\end{aligned} \tag{3.65}$$

As above mentioned, the vertical balancing is done by using sinusoidal AC components leading to

$$\frac{d\bar{W}_{\Delta J}}{dt} = -2V_{vJ}I^{ac}_{\Sigma J} \tag{3.66}$$

As reported in [83, 144] these AC components can be transformed so that they sum up to zero as it was done for the AC side power based horizontal balancing. To alleviate the next figure,

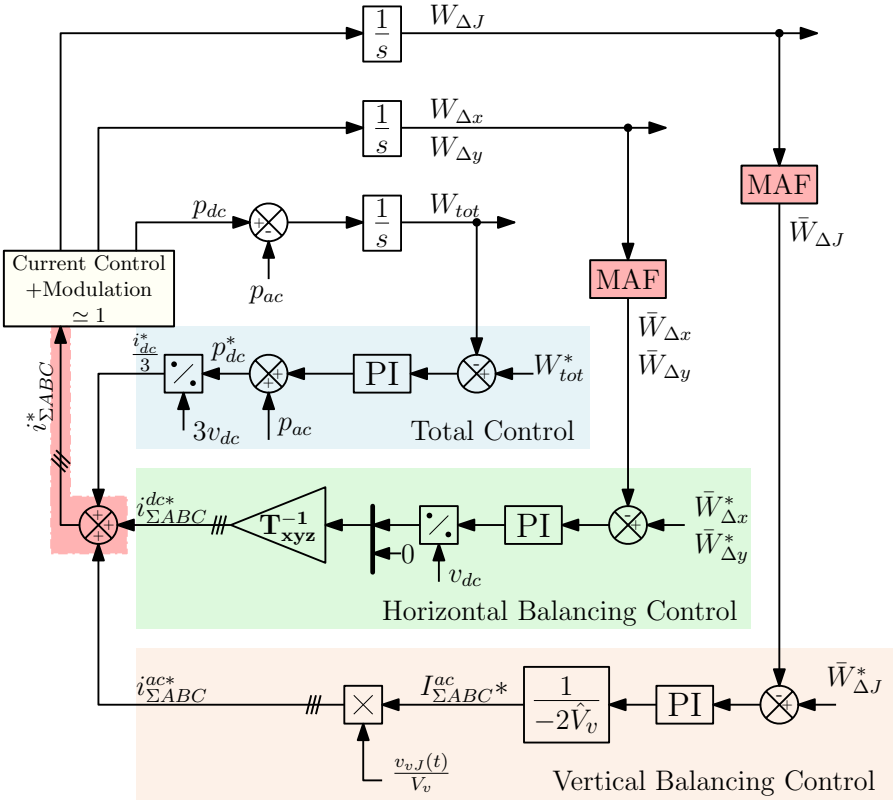


Figure 3.35 – MMC energy control scheme

this transformation will not be displayed. The overall control structure of an MMC including full-energy management is provided on Figure 3.35.

On this figure, the element inside the red box is different from the EO-AAC control. This difference, lies in the distributed effort to each converter leg thanks to the continuous control of the DC side single-phase current dynamics. Each leg participate to the total energy regulation whereas in the EO-AAC, only the leg in overlap mode supports this control. Moreover, the horizontal and vertical balancing control are performed in a continuous way. Despite some differences on the way to achieve the power balance, it is important to note that MMC and EO-AAC provides a continuous decoupling of the three-phase active power. This important properties will be further used, but first, let us demonstrate the dynamic equivalence between the EO-AAC and the MMC.

3.5.2 Response to active power reference changing

The active power step changing is probably one of the best way to show the effectiveness of a modular type converter controllers. The active power is involved in current and energy controllers, so, it is the best quantity to vary for the purpose of converter response testing. The main converter and control parameters are provided on the next table.

Parameters	EO-AAC	MMC
S_n	1.04 GVA	1.04 GVA
P_n	1 GW	1 GW
Q_n	300 MVAR	300 MVAR
v_{dc}	640 kV	640 kV
U_g	500 kV	320 kV
L_L	116 mH	60 mH
L_{arm}		50 mH
L_{dc}	20 mH	
Stacks nominal voltage	480 kV	640 kV
H_C	15 kJ/MVA	40 kJ/MVA

Control Parameters	Value
tr_{ig}	5 ms
ζ_{ig}	0.7
tr_{idc}	1 ms
ζ_{idc}	0.7
$\mathrm{tr}_{i\Sigma}$	1 ms
$\zeta_{i\Sigma}$	0.7
tr_{Wtot}	50 ms
ζ_{Wtot}	0.7
tr_{WH}	100 ms
ζ_{WH}	0.7
tr_{WV}	100 ms
ζ_{WV}	0.7

Table 3.3 – EO-AAC and MMC main parameters

In order to make a fair comparison between both converters, the dynamics of each control loops is the same. The abbreviations W_H and W_V stands for Horizontal and Vertical controllers. Results are presented on Figure 3.36.

The first and overall remark is that both converters remarkably response to this severe event. On the right side are the EO-AAC results and on the left side the MMC. From the AC side point of view, they have the exact same behaviour. This was expected since in both converters the AC power is always under control with a sufficient number of conducting stacks (i.e. at least 3). The main difference lies in their use of the DC power to keep their stack energies balanced. While the EO-AAC inject square wave-formed current harmonics in the DC current to achieve horizontal and vertical balancing, thanks to its continuous control of each stack energy, the MMC leaves the DC current harmonic free. Nevertheless, every stacks are balanced after 100-150 ms for both converters. This result shows that despite its natural discontinuous internal behaviour the EO-AAC, when properly controlled, has an equivalent controllability to the MMC (in average). Of course, the continuous control of the MMC gives more flexibility.

The previous simulation has depicted the dynamic behaviour of both converters based on an event which is not likely to occur on real power system. To mitigate the above large DC current ripple, a simple power ramping of 10 p.u. per second is performed to highlight that in such case, this ripple is almost negligible.

As presented on Figure 3.37, power ramping decrease the need for energy balancing among stacks since the power dynamics is slower than the cycles of overlap and non-overlap modes. Thus, in case of more realistic dynamic event, the EO-AAC can achieve similar DC current waveform during transient.

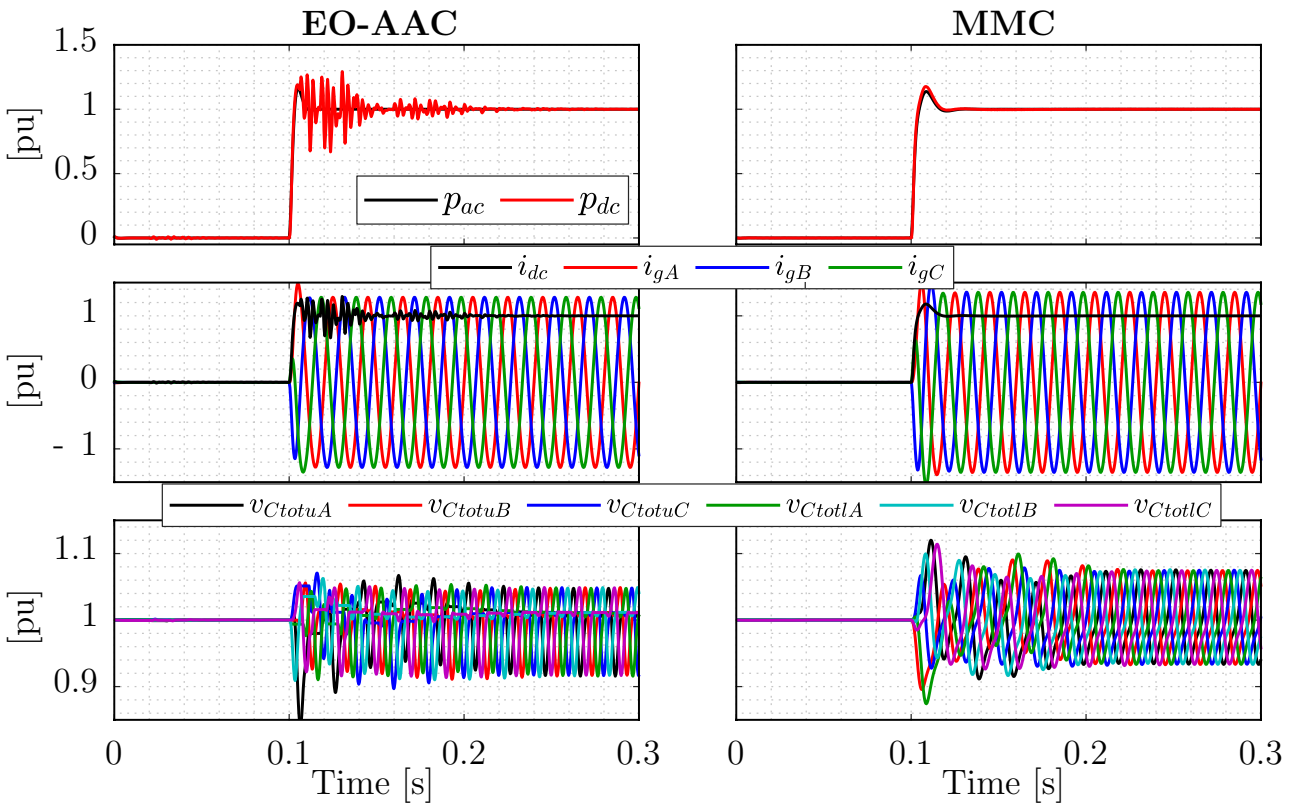


Figure 3.36 – EO-AAC and MMC dynamic behaviour comparison against a 1 p.u active power step event

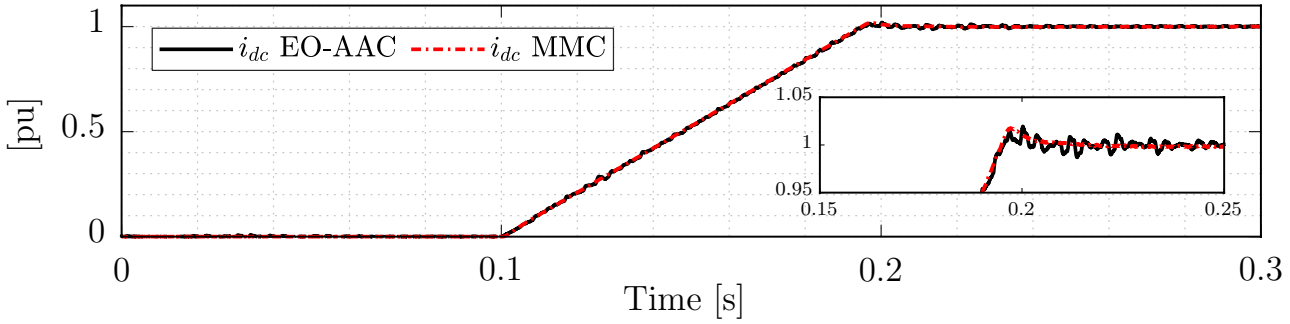


Figure 3.37 – EO-AAC and MMC DC current waveform comparison against an active power ramping

3.5.3 Common reduced order model for power system analysis

The control similarities between the EO-AAC and the MMC have been established in the previous section. In the current section, it is proposed to derive a Reduced Order Model (ROM) capturing the main dynamics of both converters. For MMC, several works have been done on finding proper simplified models [150–155]. Some of these models consider a representation of the arm quantities in Σ and Δ representation, however, this was possible since MMC arms operate continuously. Pursuing a similar quest for the EO-AAC is not straightforward since the arms operate in a different way.

In Section 3.5.1, it was concluded that some differences in the way to manage the energy exist, but, a fundamental characteristic is shared between both topologies: the constant decoupling of the AC and DC side active powers. This property is exploited to derive a continuous

and Linear Time Invariant (LTI) model. This model is intended to be freed from the DS switching.

Derivation of a Reduced Order Model

The LTI dynamics model of the AC side currents can be expressed using dq coordinates such that

$$\begin{aligned} v_{vd} &= v_{gd} + L_L \frac{di_{gd}}{dt} + R_L i_{gd} - \omega_g L_L i_{gq} \\ v_{vd} &= v_{gq} + L_L \frac{di_{gq}}{dt} + R_L i_{gq} + \omega_g L_L i_{gd} \end{aligned} \tag{3.67}$$

with ω_g the grid frequency. The DC current model is

$$v_{mdc} = v_{dc} - L_{dc} \frac{di_{dc}}{dt} - R_{dc} i_{dc} \tag{3.68}$$

These AC and DC side current dynamics can be represented through the following scheme of Figure 3.38.

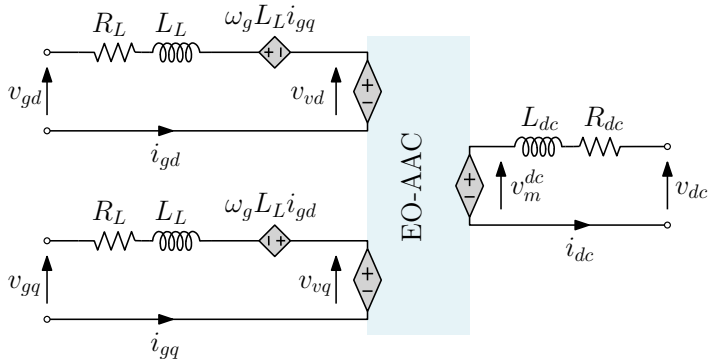


Figure 3.38 – Simplified model of AC and DC side current dynamics

These three current dynamics are decoupled from a functional point of view, however, they all depends on the energy within the converter and more precisely on the voltage availability provided by each v_{Ctot}. A simple expression of the internal energy as an interface between these currents is needed. As a reminder of the first chapter, AC and DC components in the modulated voltages are a function of v_{Ctot}. Modulation signals described as it follows

$$\begin{aligned} v_v &= -\hat{M}_v \sin(\theta_g + \theta_v) \times v_{Ctotu} \rightarrow \text{ If the upper arm is ON} \\ &= \hat{M}_v \sin(\theta_g + \theta_v) \times v_{Ctotl} \rightarrow \text{ If the lower arm is ON} \\ &= \hat{M}_v \sin(\theta_g + \theta_v) \times \frac{v_{Ctotu} + v_{Ctotl}}{2} \rightarrow \text{ If overlap mode} \end{aligned} \tag{3.69}$$

and

$$\begin{aligned} \frac{v_{mdc}}{2} &= \frac{m_{dc}}{2} \times v_{Ctotu} \rightarrow \text{ If the upper arm is ON} \\ &= \frac{m_{dc}}{2} \times v_{Ctotl} \rightarrow \text{ If the lower arm is ON} \\ &= \frac{m_{dc}}{2} \times \frac{v_{Ctotu} + v_{Ctotl}}{2} \rightarrow \text{ If overlap mode} \end{aligned} \tag{3.70}$$

Deriving dq components of the modulated voltages according to (3.69) and the converter configuration used so far (i.e. leg A in overlap mode, lower arm B and upper arm C conducting) would lead to the following results where, the amplitude invariant form of the $dq0$ transformation has been used:

$$\begin{aligned} v_{vd} &= \frac{2}{3}\left[\frac{v_{CtotuA}+v_{CtotlA}}{4}\hat{M}_{vA}\cos(\theta_{vA}) + \frac{v_{CtotlB}}{2}\hat{M}_{vB}\cos(\theta_{vB}) + \frac{v_{CtotuC}}{2}\hat{M}_{vC}\cos(\theta_{vC})\right] \\ v_{vq} &= \frac{2}{3}\left[\frac{v_{CtotuA}+v_{CtotlA}}{4}\hat{M}_{vA}\sin(\theta_{vA}) + \frac{v_{CtotlB}}{2}\hat{M}_{vB}\sin(\theta_{vB}) + \frac{v_{CtotuC}}{2}\hat{M}_{vC}\sin(\theta_{vC})\right] \end{aligned} \tag{3.71}$$

If the AC is balanced then,

$$\begin{aligned} M_{vA} = M_{vB} = M_{vC} = M_v \\ \theta_{vA} = \theta_{vB} = \theta_{vC} = \theta_v \end{aligned} \tag{3.72}$$

leading to

$$\begin{aligned} v_{vd} &= m_d \times \frac{1}{6}\left[v_{CtotuA} + v_{CtotlA} + 2v_{CtotlB} + 2v_{CtotuC}\right] \\ v_{vq} &= m_q \times \frac{1}{6}\left[v_{CtotuA} + v_{CtotlA} + 2v_{CtotlB} + 2v_{CtotuC}\right] \end{aligned} \tag{3.73}$$

and

$$\begin{aligned} m_d &= \hat{M}_v\cos(\theta_v) \\ m_q &= \hat{M}_v\sin(\theta_v) \end{aligned} \tag{3.74}$$

The DC component v_{mdc} is common to all arms. It yields:

$$v_{mdc} = \frac{m_{dc}}{2}(v_{CtotlA} + v_{CtotuA}) = m_{dc}v_{CtotlB} = m_{dc}v_{CtotuC} \tag{3.75}$$

The average DC component in modulated voltages can be obtained following the same approach:

$$v_{mdc} = m_{dc} \times \frac{1}{6}\left[v_{CtotuA} + v_{CtotlA} + 2v_{CtotlB} + 2v_{CtotuC}\right] \tag{3.76}$$

As shown by (3.71) and (3.76), the AC and DC modulated components (i.e. dq and averaged DC) are generated based on the term highlighted in red named v_{Ctot}^{mod}

$$v_{Ctot}^{mod} = \frac{1}{6}\left[v_{CtotuA} + v_{CtotlA} + 2v_{CtotlB} + 2v_{CtotuC}\right] \tag{3.77}$$

v_{Ctot}^{mod} is a time-varying combination of $v_{Ctot(u,l)J}$ that depends on $G_{DS(u,l)J}$. The equation (3.77) is only valuable for the circuit configuration used in this thesis. If it is extended to the other cases, then, $v_{v(d,q)}$ and v_{mdc} would be generated on the basis of the waveform illustrated on Figure 3.39.
The area filled in blue corresponds to the capacitor voltages combination described by the equation (3.77). Since, four among six stacks are conducting, the capacitors voltage ripple do not sum to zero explaining this six pulse ripple visible on v_{Ctot}^{mod}. To get output current without harmonics, $m_{(d,q)}$ and m_{dc} must compensate this time-varying voltage. The simplified model is expected to remove the effect of DS commutation, therefore, considering a time-varying circuit is not the aim. Regarding the amplitude of this variation (about 1%) and knowing that, in

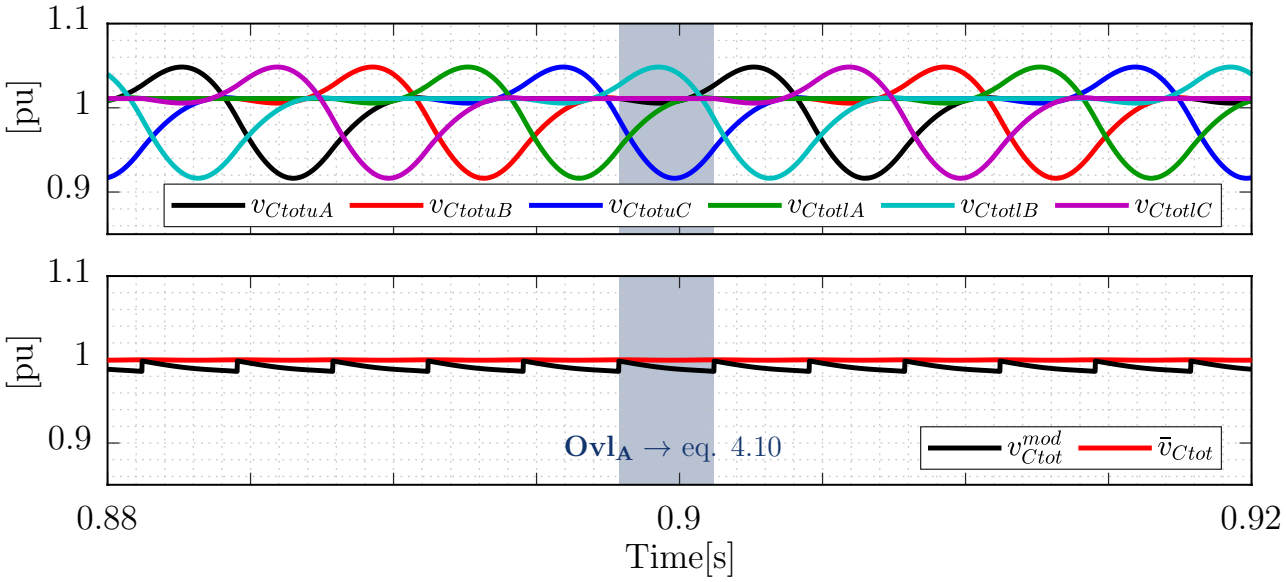


Figure 3.39 – Illustration of the time-varying voltage v^{mod}_{Ctot} and $\bar{v}_{Ctot}$

average, each of the stacks participate equally to the generation of AC and DC components allows considering

$$\bar{v}_{Ctot} = \frac{1}{6}\left[v_{CtotuA} + v_{CtotlA} + v_{CtotuB} + v_{CtotlB} + v_{CtotuC} + v_{CtotlC}\right] \tag{3.78}$$

the average capacitor voltage defined for any circuit combinations and illustrated on Figure 3.39. This assumption gives simplified expression of modulated voltages

$$\begin{aligned} v_{vd} &= m_d \bar{v}_{Ctot} \\ v_{vd} &= m_q \bar{v}_{Ctot} \\ v_{mdc} &= m_{dc} \bar{v}_{Ctot} \end{aligned} \tag{3.79}$$

AC and DC side dynamics are now interfaced through one single capacitance (C_{eq}) providing a voltage $\bar{v}_{Ctot}$. Since this equivalent voltage gather all stacks, then, the dynamics of this capacitor is equivalent the total energy model. According to Figure 3.38, the active powers in both sides are

$$\begin{aligned} p_{ac} &= v_{vd} i_{gd} + v_{vq} i_{gq} \\ p_{dc} &= v_{mdc} i_{dc} \end{aligned} \tag{3.80}$$

thus

$$\frac{dW_{tot}}{dt} = v_{mdc} i_{dc} - v_{vd} i_{gd} + v_{vq} i_{gq} \tag{3.81}$$

knowing that there is six stacks leads to

$$C_{eq} = 6C_{tot} \tag{3.82}$$

The simplified reduced order model for EO-AAC is therefore illustrated below
As shown by Figure 3.40, thanks to the extended-overlap operation, the converter can be reduced as simple modulated voltage and current sources on AC and DC side interfaced trough a single capacitor. This model is referred as a reduced order model (ROM) since the converter independent state-variables to be controlled drops from 9 to 4. This model is exactly the as for MMC described by [156] where the AC and DC side are interfaced through a single capacitor equals to $6 \times C_{tot}$. For MMC, the open-loop AC side impedance is $Z_L + Z_{arm}/2$ and the equivalent DC side reactors is $(2/3)L_{arm}$.

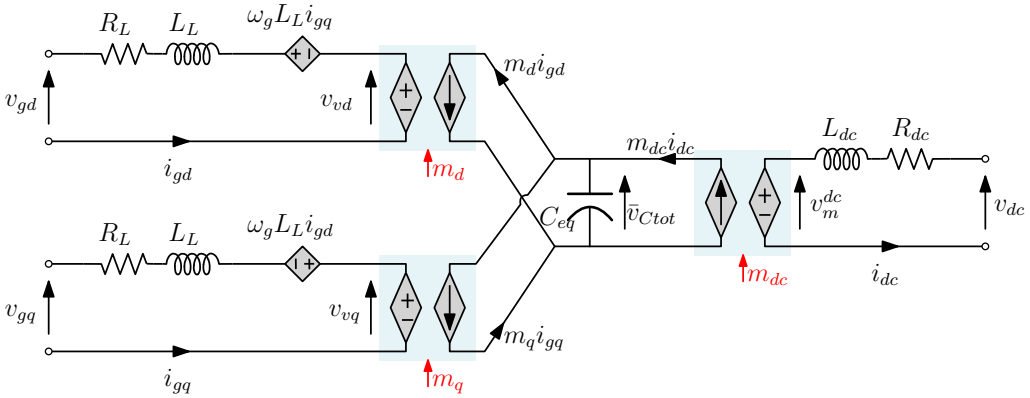


Figure 3.40 – Reduced Order Model of EO-AAC

Model validation including closed-loop control

The validity of this model is presented in section by comparing EMT type models (detailed) and the simplified one. The detailed model includes a closed-loop control on each state-variables, so the ROM must have the same control. Using the above models gives Figure 3.41.

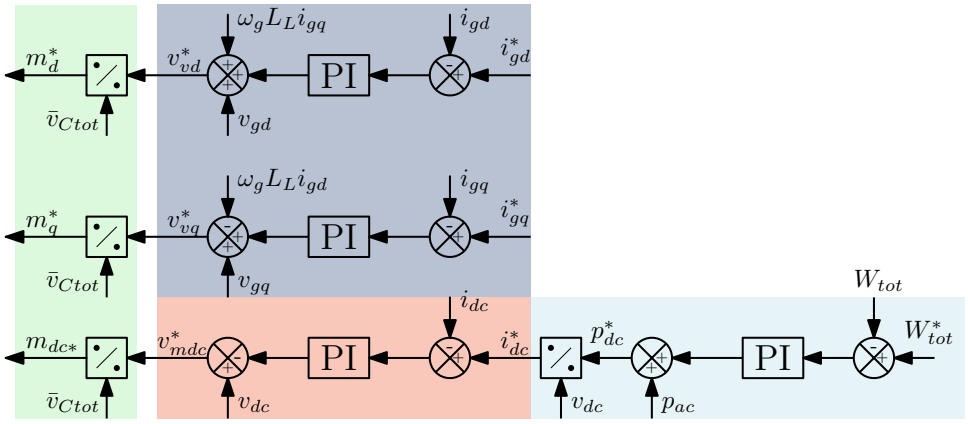


Figure 3.41 – Control structure of EO-AAC's reduced order model

The first test to compare both models is a simple power ramping. A slope of 20 p.u./s is applied on i_{gd}^*. As shown by Figure 3.42, despite the internal discontinuous nature of the EO-AAC, the ROM is able to capture the main states dynamics (i_{gd},i_{gq},i_{dc} and W_{tot}) with precision.

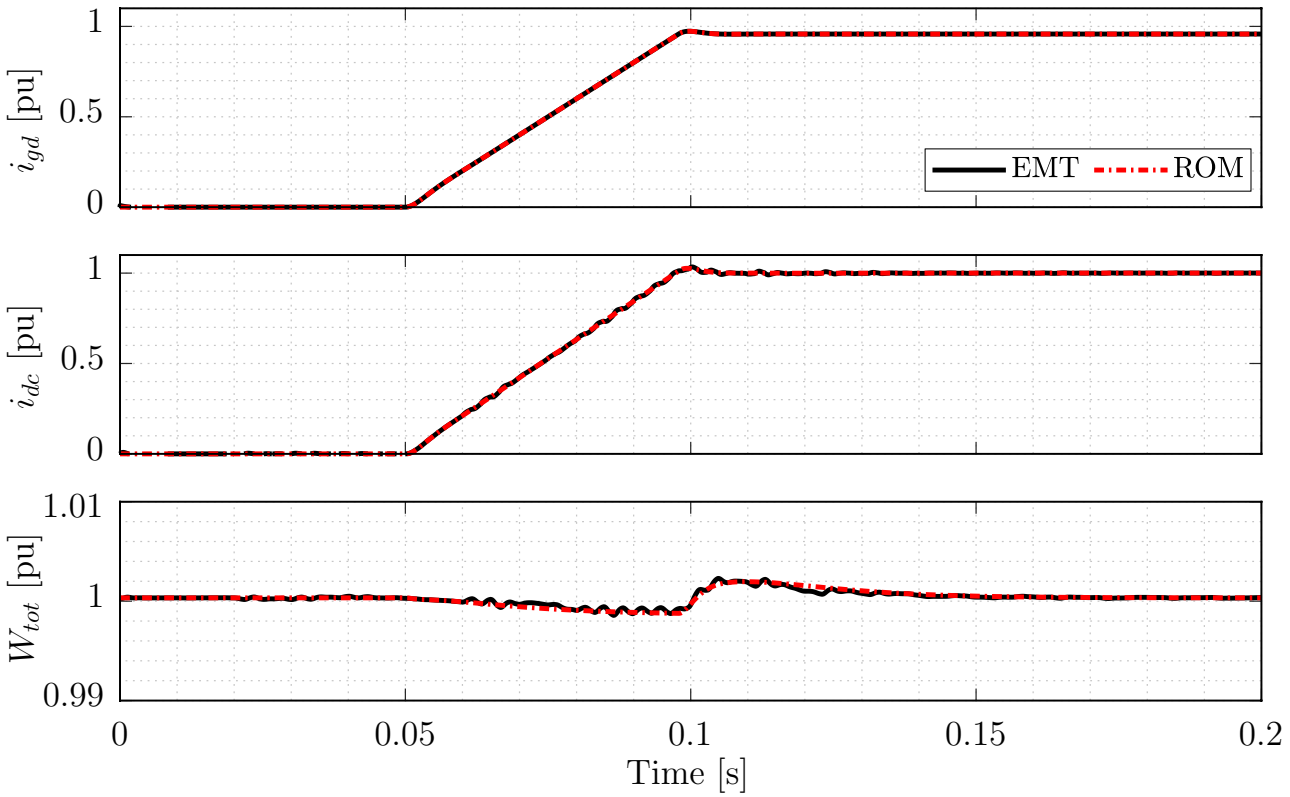


Figure 3.42 – Comparison EMT Simulation and ROM

Since the ROM gather all stack energies it cannot capture dynamics related to horizontal and vertical balancing controllers, however, the additional small ripple visible on W_{tot} and i_{dc} can be fairly disregarded.

Different use for the EO-AAC ROM

The previous section has detailed the derivations and assumptions that have allowed to describe a simplified ROM of the EO-AAC capturing its main dynamics. As aforementioned, this model is the same for the MMC. Some comparisons between MMC and EO-AAC are now possible since models are comparable.

Dynamic behaviour assessment: A first simulation scenario which considers an active power step of 0.5 p.u. under an initial operating point of 0.5 p.u is proposed. Results are depicted on Figure 3.43 and since this simulation focuses on active powers, the q axis is not displayed. The main remark that arises from these curves is the similar behaviour between MMC and EO-AAC and especially on current dynamics. This was already observed in the previous section using detailed models. For both converters pole placement control design has been used, which involves that there step response is similar. There is a small difference observed on $\bar{v}_{Ctot}$ which rely on the value of H_C. The delay in the DC power regulation (i.e. measurement, energy + current controller dynamics) creates a transient deficit of energy, better supported by the MMC thanks to its higher amount of internal stored energy

For the sake of comparison, consider an EO-AAC with H_C equals to 40 kJ/MVA, the results of

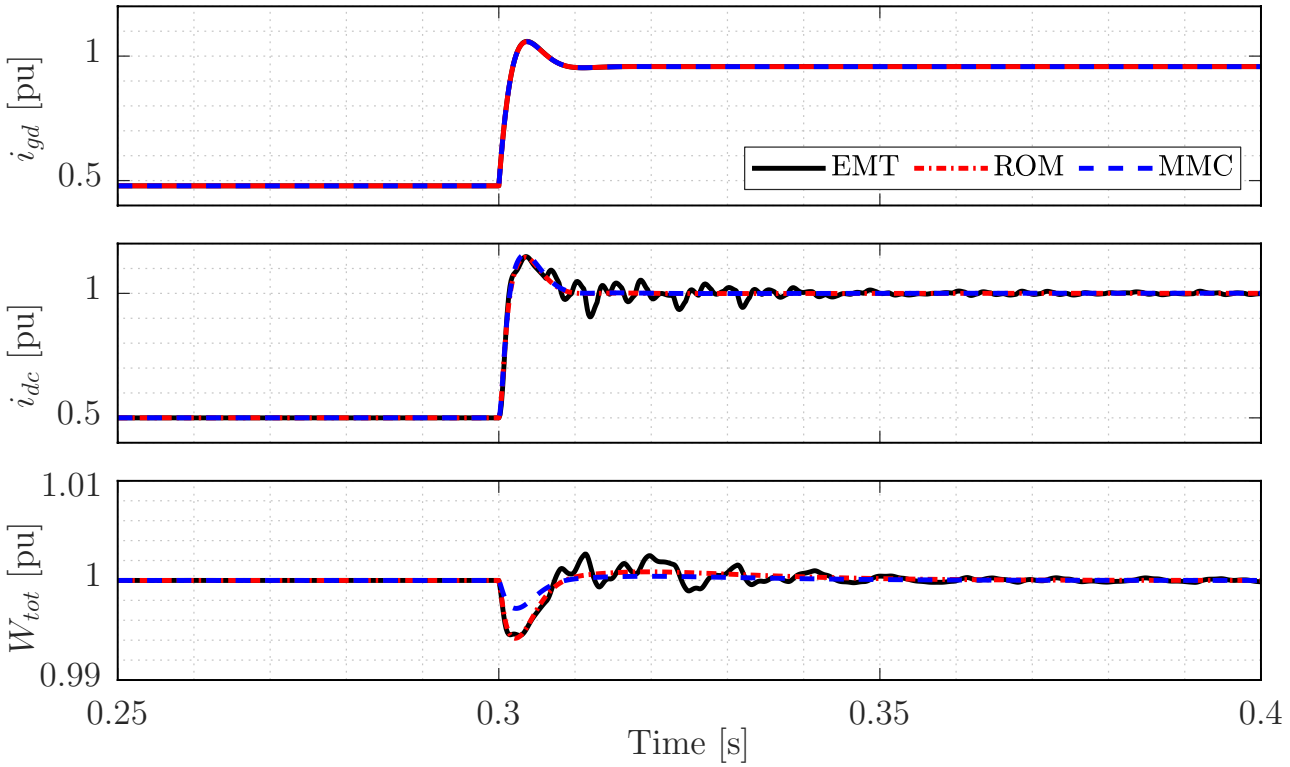


Figure 3.43 – Comparison EMT Simulation, ROM and MMC

Figure 3.44 are obtained. It clearly appears that both converters present almost the exact same response. The EMT simulation on black curves presents ripple due to balancing controllers but nonetheless the response is very similar.

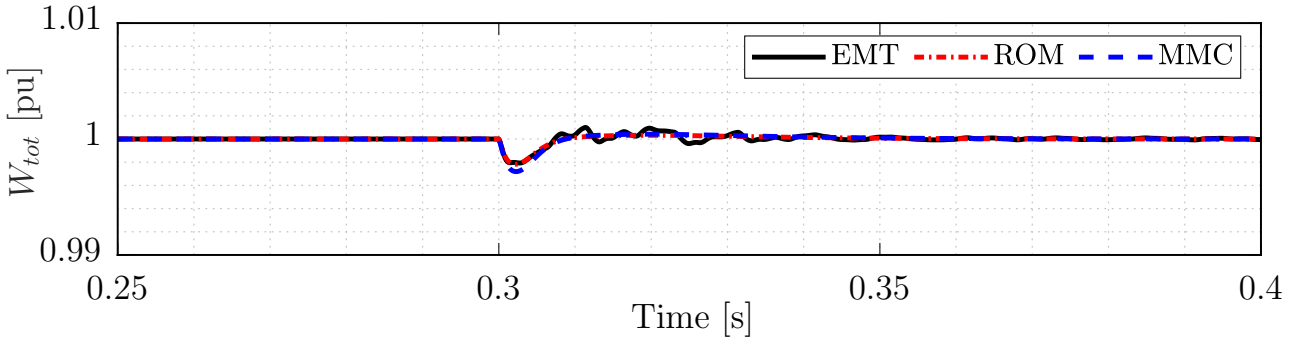


Figure 3.44 – Comparison EMT Simulation, ROM and MMC for H_C equals to 40 kJ/MVA in both converters

These simulations have established a real dynamic equivalence between MMC and EO-AAC, which, thanks to the continuous nature of the ROM can be confirmed through small signal stability.

Small signal stability analysis: Time domain simulations done so far, were including all non-linearities (even switching for EMT simulation) which are complex to analyse, especially when considering AC and DC systems. For power system studies, it is common to simplify models by linearisation around an equilibrium point (x_0,u_0) which reasonably capture the

converter dynamics. This model is referred as Linear Time Invariant (LTI). One of the powerful tools for these systems analyses is the small stability analysis through calculation of the **A** matrix eigenvalues (i.e. poles of the system).
Each converter dynamics is now modelled in a state-space form such as

$$\begin{aligned} \dot{\mathbf{X}} &= \mathbf{AX} + \mathbf{BU} \\ \mathbf{Y} &= \mathbf{CX} + \mathbf{DU} \end{aligned} \tag{3.83}$$

where the system states are

$$\mathbf{X} = \Big[\underbrace{i_{gd}\ i_{gq}\ i_{dc}\ W_{tot}\ \theta_g}_{\text{Physical states}}\ \underbrace{\zeta_{igd}\ \zeta_{igq}\ \zeta_{W_{tot}}\ \zeta_{PLL}}_{\text{Control integrator states}}\Big]^\top \tag{3.84}$$

and inputs

$$\mathbf{U} = \left[i^*_{gd}\ i^*_{gq}\ W^*_{tot}\right]^\top \tag{3.85}$$

Assuming the converter operating around an equilibrium point gives

$$\begin{aligned} \mathbf{\Delta\dot{x}} &= \mathbf{A\Delta x} + \mathbf{B\Delta u} \\ \mathbf{\Delta y} &= \mathbf{C\Delta x} + \mathbf{D\Delta u} \end{aligned} \tag{3.86}$$

Based on this linear model, eigenvalue extraction can be achieved for a given active and reactive power set points. Considering $P_{ac} = 1$ p.u. leads the following figure: From the eigenvalues

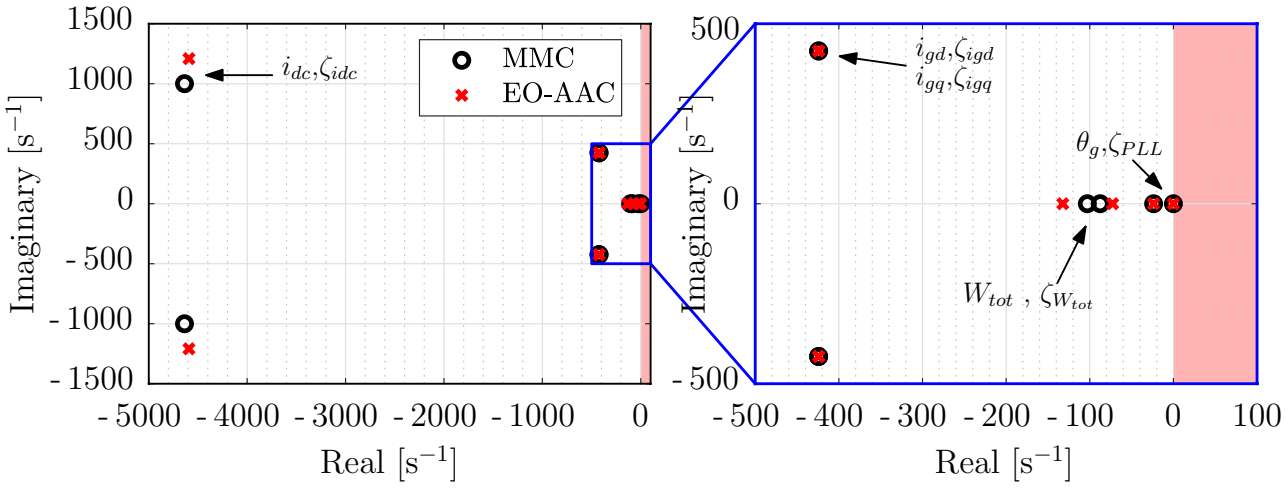


Figure 3.45 – MMC and EO-AAC eigenvalues of linearised ROM

analysis of Figure 3.45, the small differences observed on the time domain simulation are retrieved. Indeed, by time domain simulation it was observed that the energy response was slightly different between both topologies. According to Figure 3.45 W_{tot} presents the same damping but faster in case of EO-AAC (i.e. $-132 + i0$ for EO-AAC and $-102 + i0$ for MMC). As a result, poles related to the DC current dynamics are impacted. On the other hand, AC side current poles are exactly at the same place since the output impedance is 0.15 p.u. for both.

3.6 Chapter Conclusion

This chapter has provided a thorough study of the control for the EO-AAC, from the firing of the SMs to the energy management. As a first requirement, it has been highlighted the importance of a compensated modulation scheme (i.e. consideration of capacitor voltage ripple) to achieve an efficient filtering of the AC modulated voltages and DC current.
Then, a control structure providing a closed-loop control on each state-variable has been proposed where the main part reside in the energy management and the different combination that are used. However, as a drawback of the current-based energy management, due to the single-leg in overlap mode the DC current is transiently rippled. Those ripples are highly linked to strength of the event.
In the last part of the chapter, a reduced order model has been proposed to enable power system analysis which reveals to be the same for the MMC. Finally, in this chapter, an equivalence between the MMC and the EO-AAC has been established thanks to the proposed control structure.

Chapter 4

Application to the HVDC and HVAC Grid Connection

4.1 Introduction

The previous chapters have detailed both the steady state aspect for sizing purposes and the dynamic aspect to determine the control structure of the EO-AAC. All of these works were based on the assumption that the converter was connected to two infinite AC and DC voltage sources.

In this chapter, the connection to the grid will be discussed, and more specifically the connection to the HVDC system. It is organized into three main parts. First, the point-to-point HVDC link is addressed. This study is initially based on the use of the reduced order model detailed in Chapter 3 in order to validate the general principles. The contribution that energy management of the converter can have is highlighted. Then, the general validation is done using the detailed model of the EO-AAC under EMTP-RV software.

Secondly, the case of the MTDC system is considered. This study is based on a distributed management of the DC voltage through a droop control. Through this section, the importance of energy sharing from converters for DC voltage support is developed. Various controls provided for this purpose are tested. The interoperation between different modular stations is presented.

The last section of the chapter is devoted to specific operating regimes, such as the case of the DC fault or the unbalanced HVAC grid. The objective of these studies is to highlight certain limitations of EO-AAC due to its sequential operation but also leads for future research.

4.2 Control of an HVDC-Link

In this section, the case where two EO-AACs are connected through a HVDC link is addressed. The basic principles of such system is very simple since one station must control the power while the second one controls the DC voltage across its terminals. This is illustrated on Figure 4.1.

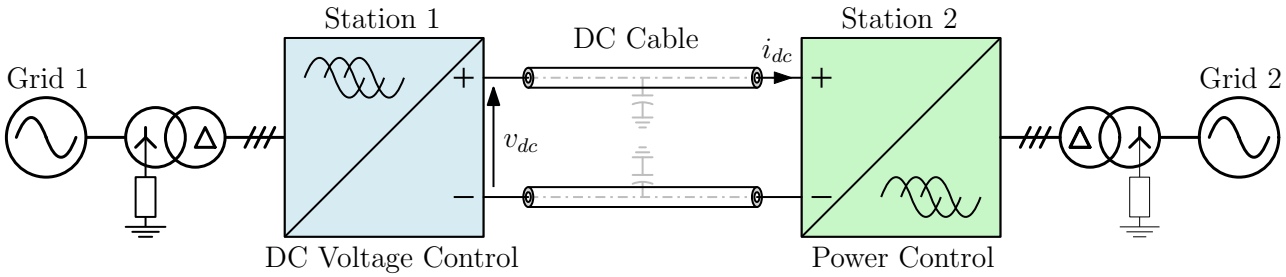


Figure 4.1 – HVDC link representation

One of the most crucial point for HVDC system (in addition to converter stations) are the cables whether from an economic or installations point of view [157]. Modelling such components is also particularly complex and requires dedicated research works to tackle this issue. So far, different kinds of modelling have been derived, some of them are suitable for EMT simulation such as in EMTP-RV or PSCAD following the principle of Universal Line Model (ULM) detailed in [158]. This model, in EMTP-RV, is called "wideband" model. However, these models are very complex as they need a priori determination of frequency dependent parameter matrices related to propagation and admittance matrices. On the other hand, there are cable models with constant parameters [159–161] but using cascaded cells to get the desired frequency behaviour. Such models has the merits of being simpler (in case of low number of cells) and suitable for system analysis as they can be reproduced using state-space representation.

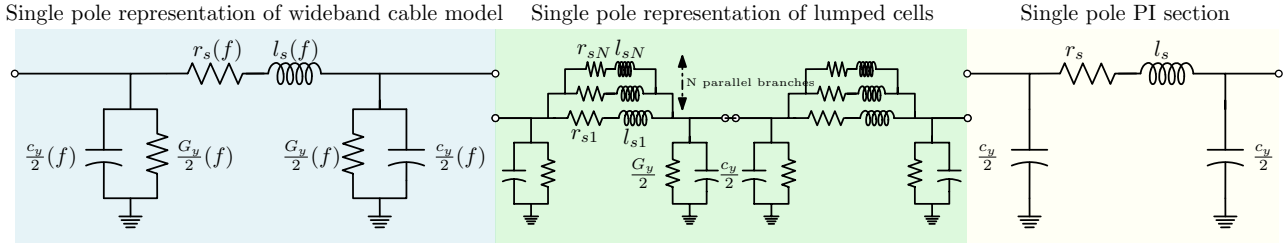


Figure 4.2 – DC cable models: a) wideband b) cascaded cells with constant parameters c) PI-section

Some idea about the representation of these models is proposed in Figure 4.2 for one pole (i.e. positive/negative to ground). The main parameters, r_s and l_s for series resistance and inductance, c_y and G_y for shunt capacitance and conductance, are determined on the basis linear parameters per km. Finally, it is also possible to represent each cable pole through a simple PI section. A small comparison between them is presented further in the section.

To build the DC voltage controllers, that is equipped station 1 of Figure 4.1, considering such detailed representation is unnecessary. Indeed, most of the energy within a cable is stored in an electrostatic from, so basically in the equivalent cable capacitance C_{dc} due to the very high voltage. Thus, focusing on the voltage dynamics across this capacitance is sufficient (proofs are provided once detailed cable models are used). To derive the control structure let us fist consider a simplified case.

4.2.1 Control of an EO-AAC connected to a variable DC voltage

Depending on the VSC-HVDC station topology, the DC voltage dynamics can either rely on C_{dc} in addition to the filter capacitor in case of 2-Level VSC, or only on C_{dc} for modular-type stations. HVDC cable provides about 0.2 μF per km, which, according to the voltage and power ratings (640 kV and 1 GW) gives about 0.04 kJ/MW/km of stored energy (or 40 μs/km). So, the removal of DC filter makes the DC voltage control even more important than it was for 2-level converter. Less energy means a DC voltage more subject to deviation in case of active power transient. Therefore, the following is focused on modular converter without DC bus capacitor that represent one of the worst cases. To build the controller, the following scheme is considered:

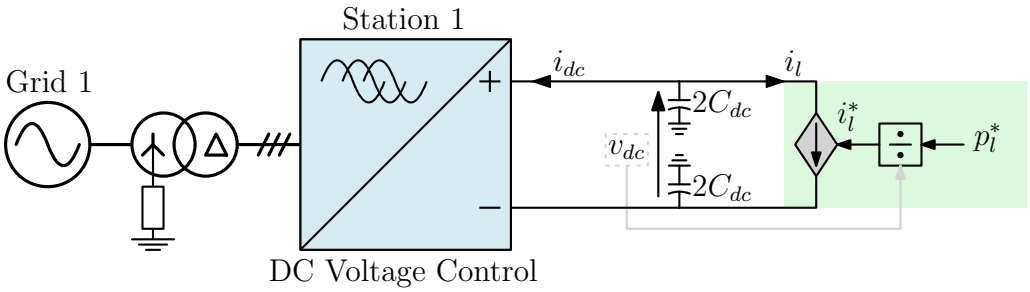


Figure 4.3 – Simplified HVDC link representation

Station 1 is connected to the HVDC link which interfaces a basic power injector delivering a power p_l through the link. The power balance in the link is therefore governed by

$$\frac{1}{2}C_{dc}\frac{dv_{dc}^2}{dt} = p_l - p_{dc} \tag{4.1}$$

where, in this case, p_{dc} is the DC power on converter side. The DC power has been used so far to maintain the power inside the converter, so, and knowing that losses are about 1% then let use modify (4.1)

$$\frac{1}{2}C_{dc}\frac{dv_{dc}^2}{dt} = p_l - p_{ac} \tag{4.2}$$

The model (4.2) is therefore the same as for 2-Level converter which are not able to manage DC components in the arm quantities. The EO-AAC ROM control including DC voltage control is obtained and presented on Figure 4.4. The complete control structure comprising balancing controllers would be more complex without improving the understanding of the DC voltage control. This section, and the following one are therefore not considering the detailed model of EO-AAC.

As shown by this figure, the DC voltage control gives a reference for i_{gd}. However, there is an important point of this control related to the compensation of p_l depending on communication between each converters. For long distance transmission, communication delays may be important thus it is assumed that no communication exists. As a result, disturbances are compensated with the dynamics of the controller.

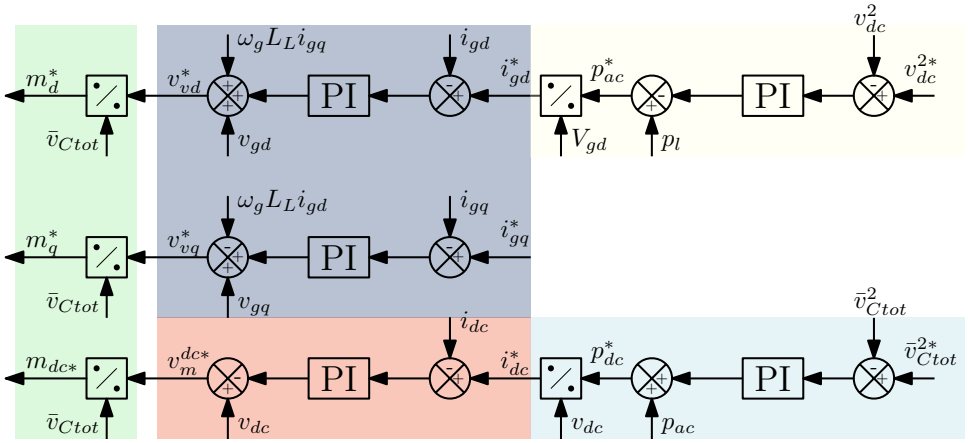


Figure 4.4 – Control structure of EO-AAC ROM comprising DC voltage control

Simulation results

An HVDC link of 300 km is simulated. The equivalent DC capacitance is 72 μF (according to the geometry of the link in EMTP-RV the linear capacitance is 0.24 μF/km). The DC link stored energy is therefore equals to 14.7 kJ/MW. The DC voltage response time is set to 100 ms and the damping ratio to 1. The scenario, is an active power step of 300 MW on p_l^*.

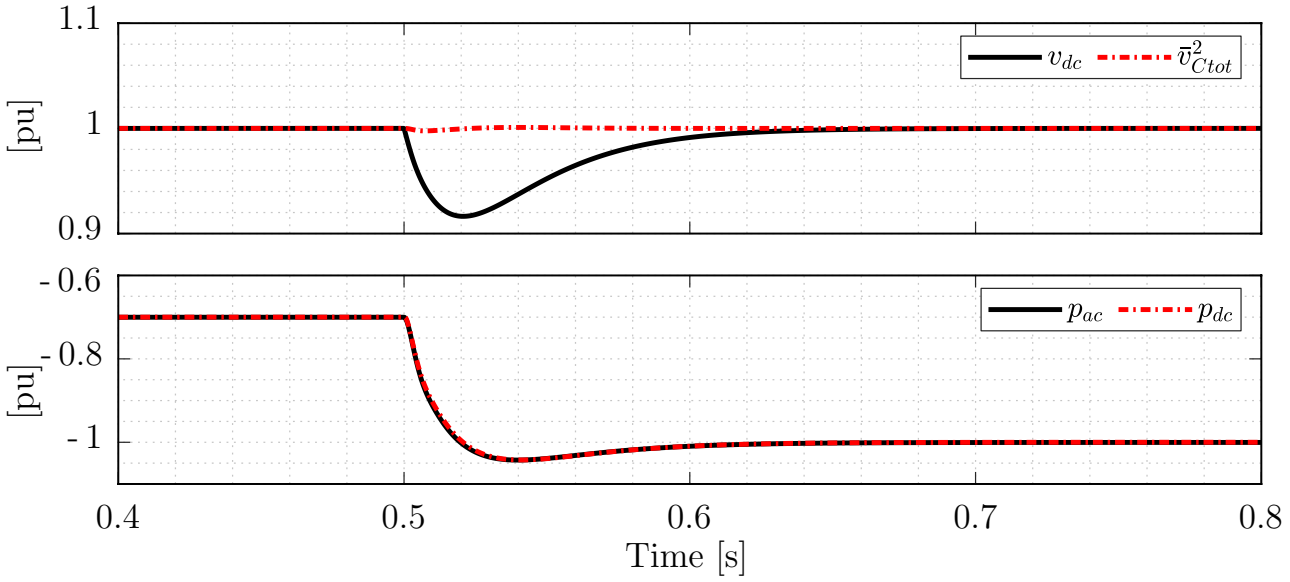


Figure 4.5 – Simulation of the simplified HVDC link with EO-AAC ROM

As shown by Figure 4.5, at power step instance, there is a deficit of power enforcing the DC cable to discharge. Then, the DC voltage controller adapts p_{ac}^* to restore the DC voltage level up to its nominal value. The total energy controller derive the DC power reference to maintain stable $\bar{v}_{Ctot}^2$. This uncoordinated management of the DC power and voltage level may in some cases increase even more the power imbalance at both cable ends.

As proposed in [162], a coordinated management of the MMC internal energy and DC voltage level is possible. This DC voltage support is the aim of the next section.

4.2.2 DC voltage dynamics improvement

The principle of the DC voltage support can be simply illustrated through the EO-AAC ROM as in Figure 4.6.

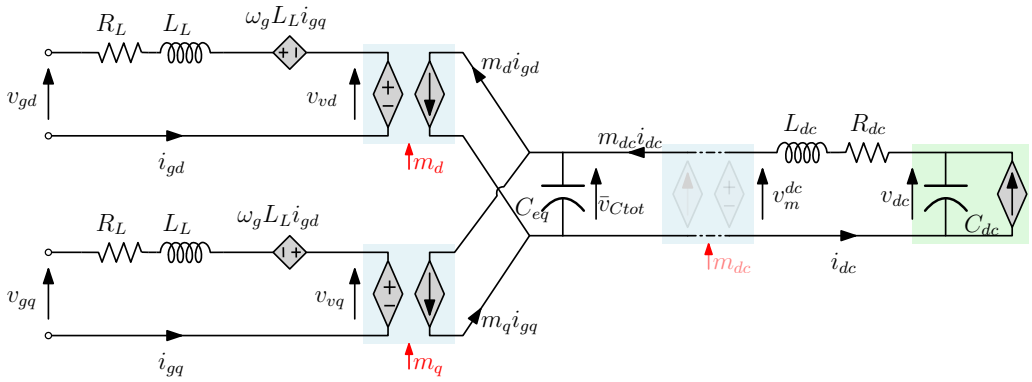


Figure 4.6 – Illustration of DC voltage support concept using modular converter internal energy

The main idea resides in creating a link between v_{dc} and $\bar{v}_{Ctot}$ as shows Figure 4.6. From a graphical point of view, it lies in a specific adjustment of the modulation function m_{dc} so that both EO-AAC and DC cables capacitances are virtually connected in parallel to increase the overall DC side capacitance. For instance, this principle has already been observed in MMC in both open-loop [126] and closed-loop control [162] on the energy. Applying this principle to EO-AAC is possible thanks to its constant decoupling of AC and DC side providing a continuous control of $\bar{v}_{Ctot}^2$. Let us reconsider the DC voltage dynamics model

$$\frac{1}{2}C_{dc}\frac{dv_{dc}^2}{dt} = p_l - p_{dc} \tag{4.3}$$

Until now, the DC power has been replaced by p_{ac} to mimic 2-level VSC like DC voltage control. However, as the energy conversion is not direct due to the internal storage devices, then, another expression of the DC power exist.

$$p_{dc} = p_{ac} + \frac{1}{2}C_{eq}\frac{\bar{v}_{Ctot}^2}{dt} \tag{4.4}$$

Then, a modified model of the DC voltage deviation considering the intermediate stage of the energy conversion is obtained.

$$\frac{1}{2}C_{dc}\frac{dv_{dc}^2}{dt} = p_l - p_{ac} - \frac{1}{2}C_{eq}\frac{\bar{v}_{Ctot}^2}{dt} \tag{4.5}$$

showing that if $\bar{v}_{Ctot}^2$ is managed according to v_{dc}^2 would leads to a DC voltage dynamics governed by an equivalent DC capacitance composed of the contribution of the converter.

$$\frac{1}{2}\left(C_{dc} + C_{eq}\right)\frac{dv_{dc}^2}{dt} = p_l - p_{ac} \tag{4.6}$$

Virtual capacitor control [163]

As introduced in Chapter 2, stacks of the EO-AAC are designed for less than the DC voltage, enforcing to introduce k_m such that

$$\frac{1}{2}C_{eq}\bar{v}_{Ctot0}^2 = \frac{1}{2}C_{eq}k_m^2 V_{dc0}^2 \tag{4.7}$$

The energy within the EO-AAC was so far controlled to this nominal value involving that $\bar{v}_{Ctot}^{2*} = \bar{v}_{Ctot0}^{2}$, but, a second solution is possible and lies in the modification of the total energy reference. This strategy, initially proposed in [162] and then improved by [163], considers that the energy reference can be expressed as:

$$\bar{v}_{Ctot}^{2*} = \bar{v}_{Ctot0}^{2*} + \Delta\bar{v}_{Ctot}^{2*} \tag{4.8}$$

so that

$$\Delta\bar{v}_{Ctot}^{2*} = k_{vc}k_m^2\left(v_{dc}^2 - V_{dc0}^2\right) \tag{4.9}$$

where k_{vc} is the virtual capacitor coefficient used to modulate the implication of the converter energy in the DC voltage dynamics. This strategy has been called Virtual Capacitor Control [163] and initially designed for MMC and proposed to be extended to the EO-AAC. Assuming that the total energy effectively controlled as it was validated in the previous chapter, then $\bar{v}_{Ctot}^{2} \simeq \bar{v}_{Ctot}^{2*}$

$$\frac{1}{2}\left(C_{dc} + k_{vc}k_m^2 C_{eq}\right)\frac{dv_{dc}^2}{dt} = p_l - p_{ac} \tag{4.10}$$

as a result, the equivalent capacitance governing the voltage dynamics is increased. To get a generic modelling of such control strategy, it is possible to include the variables H instead of C

$$\begin{aligned} H_C &= \frac{C_{eq}k_m^2 V_{dc0}^2}{2S_n} \\ H_{dc} &= \frac{C_{dc}V_{dc0}^2}{2P_{dcb}} \end{aligned} \tag{4.11}$$

which, once injected in (4.10) gives

$$\frac{1}{V_{dc0}^2}\left(2H_{dc}P_{dcb} + 2k_{vc}H_C S_n\right)\frac{dv_{dc}^2}{dt} = p_l - p_{ac} \tag{4.12}$$

highlighting that the only quantity that matters in voltage dynamics is H. By reconsidering the control structure of the EO-AAC simplified model including DC voltage support yields

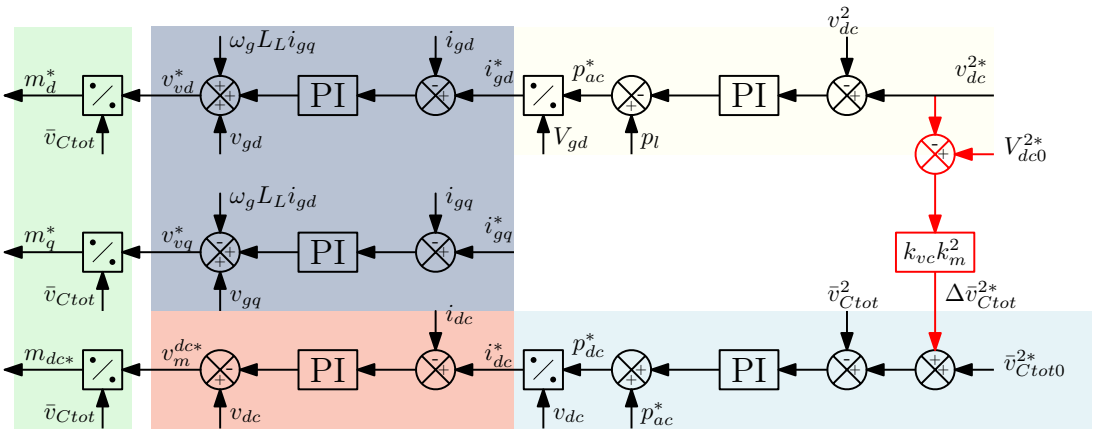


Figure 4.7 – Control structure of EO-AAC ROM comprising DC voltage control and support

To improve the response of the whole system, instead of compensating the measurement of the AC power in the total energy controller, as it was done so far, the reference coming from the DC voltage control is injected. Thus, the dynamics of the current controller is removed.

Simulation results

Applying this control scheme to the simplified HVDC link leads to the following results where the simulation scenario is the same as before, i.e. a power step on p_l^*. The only change lies in the value of the virtual capacitor coefficient k_{vc}, now set to 1s. The effectiveness of such control strategies is clearly visible on the first graph of Figure 4.8, where compared to Figure 4.5 the transient of the DC voltage deviation is lower.

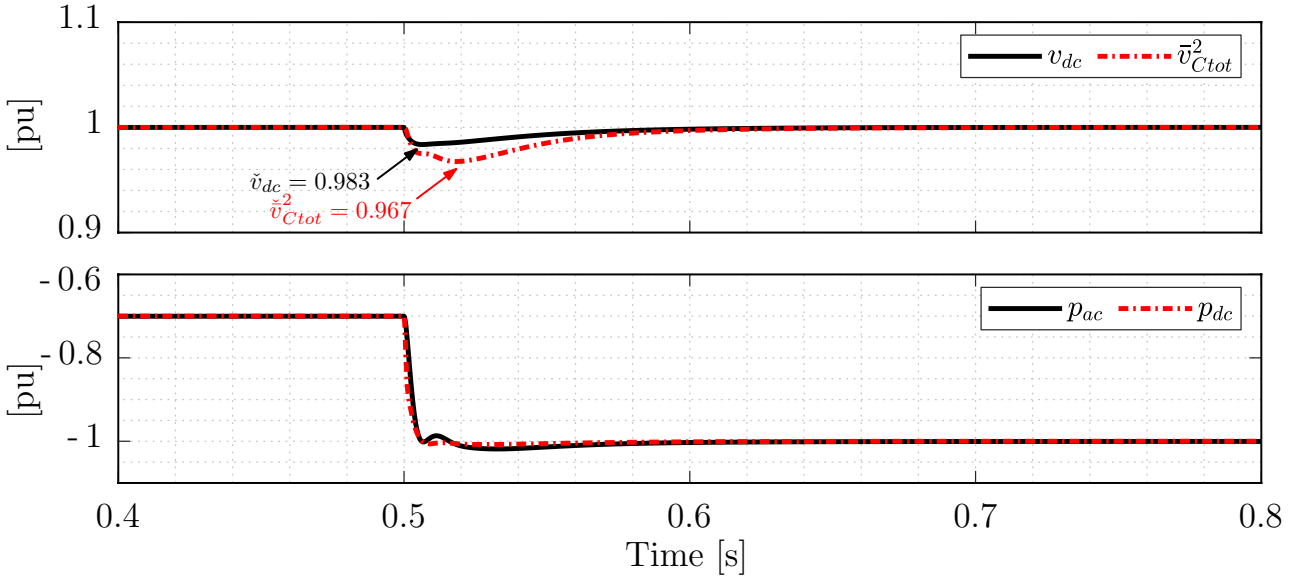


Figure 4.8 – Simulation of the simplified HVDC link with EO-AAC ROM and DC voltage support ($k_{vc} = 1$)

Indeed, without support of the EO-AAC internal energy, the minimal value of v_{dc} ($\check{v}_{dc}$) reached about 0.92 p.u. while with k_{vc} equals to 1 the DC voltage drop is limited to 0.983 p.u.. It also interesting to note that, this is made possible by sharing only 3.3% of the converter internal energy (i.e. the energy drops to 0.967 p.u. on Figure 4.8). Such small discharge can effectively improve the HVDC system resilience against active power transient, however, it is important to verify the effect on stack energies (so on $v_{Ctot(u,l)J}$). This will be discussed in Section 4.2.3. As above-mentioned, through k_{vc} it is possible to adjust the contribution of the converter to the DC voltage dynamics as shown by the Figure 4.9 where this coefficient is varied between 1 and 2.5.

It is visible on Figure 4.9 that increasing the value of k_{vc} is not very interesting since the reduction of the DC voltage deviation appears as being non-linear with k_{vc}. Actually, as pointed out in [163], such strategy relies the dynamics of the converter internal quantities, and these dynamics must be sufficiently fast. However, increasing internal dynamics for the purpose of a few tenth of percent appears as being useless. Thus, in this condition (HVDC link of 300 km and the chosen controllers dynamics), the following will consider k_{vc} equals to 1.

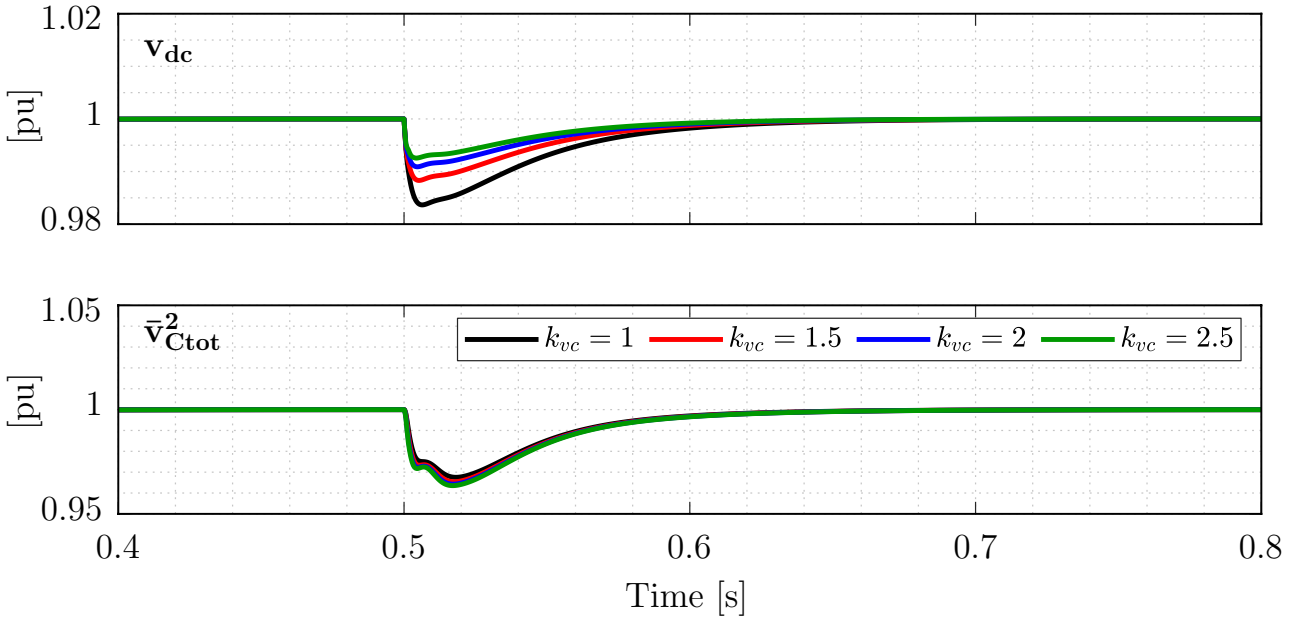


Figure 4.9 – Simulation of the simplified HVDC link with EO-AAC ROM and DC voltage support ($k_{vc} = 1$)

Impact of chosen cable model

The same simulation has been performed using different types of cable models. The wideband, the single PI cell with constant parameters and the equivalent capacitance, see Figure 4.2)
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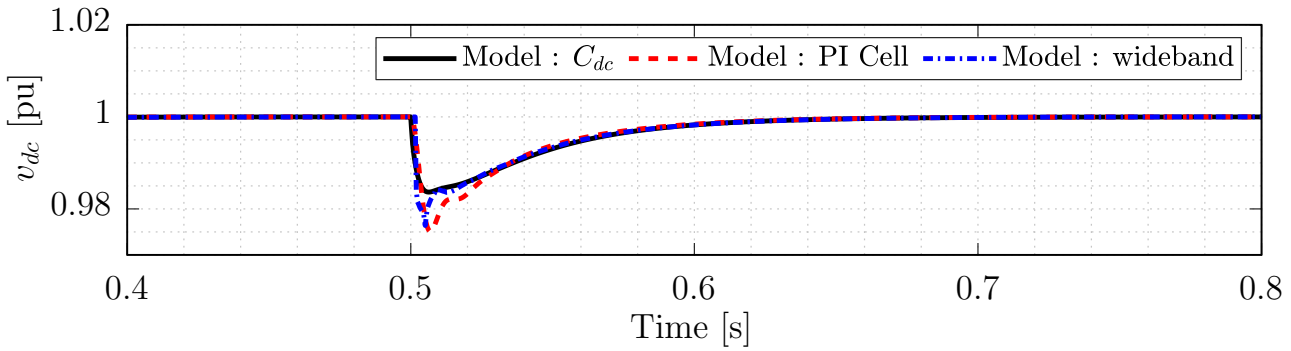

Figure 4.10 – Comparison of v_{dc} under different DC cable models ($k_{vc} = 1$)

From the results obtained on Figure 4.10, the wideband model clearly behaves differently at power step instance since its high frequency behaviour is different from the other models. However, from an overall dynamics point-of-view each model is comparable thus supporting the assumption of the equivalent capacitor during the control design. In the following, for detailed simulation, the wideband model will be considered.

4.2.3 Detailed HVDC link : Different application cases

The above sections have introduced some fundamentals about DC voltage control using modular type converters through the ROM. This model has the merit of simplifying the analysis, however, it is now needed to validate the above results using detailed models. A complete HVDC link is now tested still using EMTP-RV, but, now cable models are based the wideband model to get more realistic results than the equivalent capacitance.

Two EO-AACs without DC voltage support

In that simulation, two EO-AACs are interfaced through a DC cable of 300 km. It is possible to make each of the EO-AAC participating to the DC voltage dynamics, or not. A first simulation is carried out without participation of the converters to highlight the interest of this strategy for EO-AAC. The scenario is the same as before, an active power step of 300 MW applied to p^*_{ac} of Station 2 which control the power through the link. Results are presented on Figure 4.11 and very different from those obtained with the ROM. Indeed, DC side quantity are highly rippled during transients. These ripples observed on v_{dc} and i_{dc} are coming from the horizontal and vertical controllers that transiently injects square-wave ripple in i_{dc} to maintain an even distribution of the energy inside the converter.

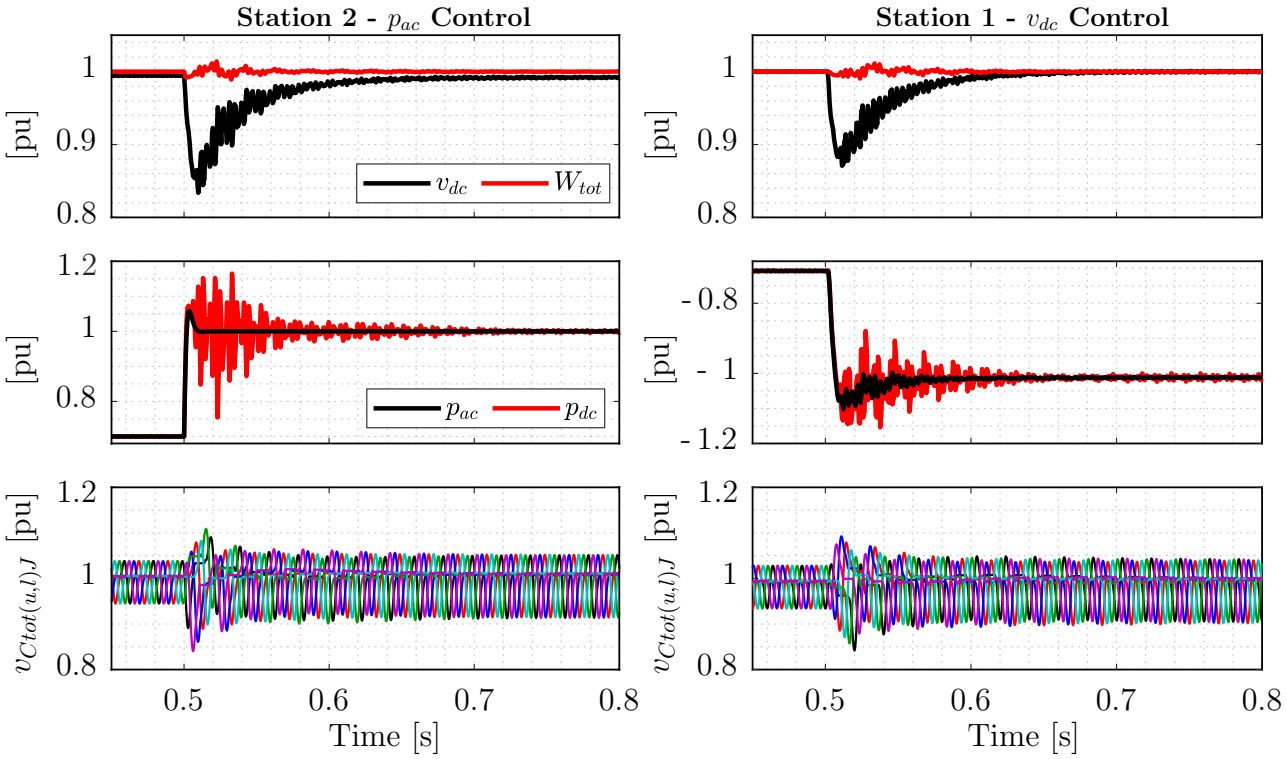

Figure 4.11 – Detailed HVDC link simulation results - No DC voltage support

As mentioned in Chapter 3, power steps highly disturb the vertical balancing controller since the fast transient leads to an unbalance of the energy between upper and lower stacks. This is caused by the alternation of the arm. Then, there is no way to improve this point. The second point is, when the DC bus voltage was stiff, the horizontal balancing controllers were not so involved. However, once the DC voltage is no longer constant, these controllers have to deal with higher energy unbalance between legs. To explain this phenomenon, let us recall the

simplified average horizontal balancing model (in xy basis):

$$\underbrace{\frac{d\bar{W}_{\Delta(x,y)}}{dt}}_{P_{W(x,y)}} = v_{dc} I_{\Sigma(x,y)} - P_{ac(x,y)} \left(\frac{4}{m\pi} \cos\left(\frac{\theta_{ovl}}{2}\right) - 1 \right) \tag{4.13}$$

where m, if we do not suppose $v_v = v_g$ is equal to

$$m = \frac{2\hat{V}_v}{v_{dc}} \tag{4.14}$$

As a result, considering a DC voltage drop, the reference for I_Σ is

$$I_\Sigma^* = \underbrace{\frac{1}{v_{dc}} \underbrace{\left(P_{W(x,y)}^* + P_{ac(x,y)} \underbrace{-P_{ac(x,y)} \frac{2v_{dc}}{\hat{V}_v} \cos\left(\frac{\theta_{ovl}}{2}\right)}_{\text{Decrease}} \right)}_{\text{Increase}}}_{\text{Increase}} \tag{4.15}$$

and as highlighted by the under-braces, this reference is increasing. Firstly, due to the division by v_{dc}. Then, due to the presence of the modulation index in the model introduced by the existence of the energy sweet-spot. The sweet-spot is shifted according to the value of v_{dc} and $\hat{V}_v$ and impact the value of the balancing currents.

Two EO-AACs with DC voltage support

Originally, the application of DC voltage support using MMC internal energy was dedicated to limit DC voltage deviation so that modulated voltages were not going into the over-modulation region (i.e. $v_{Ctot} > v_m > 0$). The EO-AAC is composed of FB-SMs, then, the modulation boundaries are $v_{Ctot} > v_m > -v_{Ctot}$. The purpose of the DC voltage support is therefore to limit (i) DC over-voltage and (ii) the need for horizontal balancing currents. This is presented on the next figure.

As depicted on Figure 4.12, the main interest lies in the reduction of the balancing currents. In that case, both converters are using their energy to support v_{dc}. On Figure 4.11, the DC power ripple peak-to-peak value was about 0.4 p.u., whereas now it goes down to 0.15 p.u while improving the DC voltage dynamics. Moreover, it is worth mentioning that, the use of the energy inside the SM capacitors has not created a higher drops of one of the six v_{Ctot}. Indeed, by comparing both figures the minimal value of v_{Ctot} that can be observed is the same, about 0.85 p.u. for Station 2. The results are even better on Station 1. This means, in that specific case, the performances of the whole system have been improved, without creating potential voltage unavailability ($|v_m| > v_{Ctot}$).

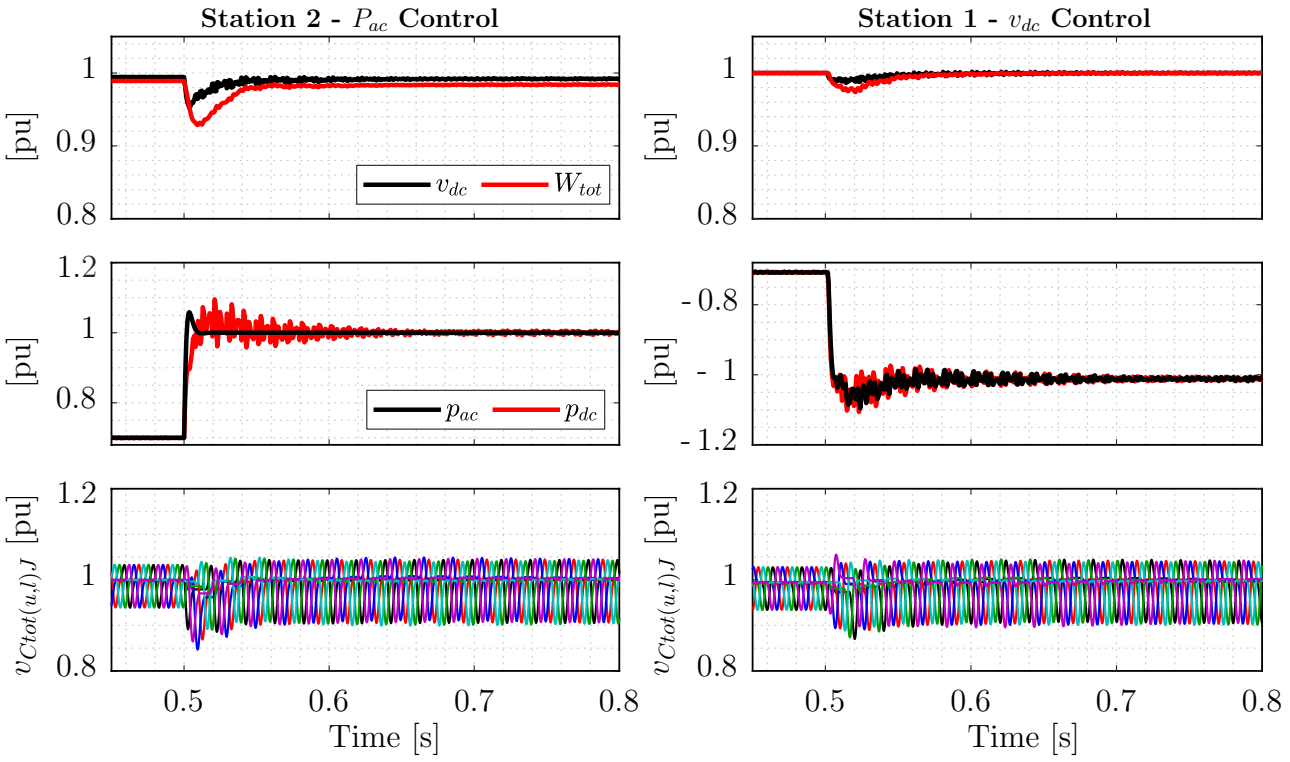

Figure 4.12 – Detailed HVDC link simulation results - With DC voltage support

The question of the voltage availability was raised for MMC by [163] in order to design the value of k_{vc}. On Figure 4.13 is illustrated each modulated voltage reference (v_m^*), v_{Ctot} and required voltage ($v_{Ctot} - |v_m^*|$).

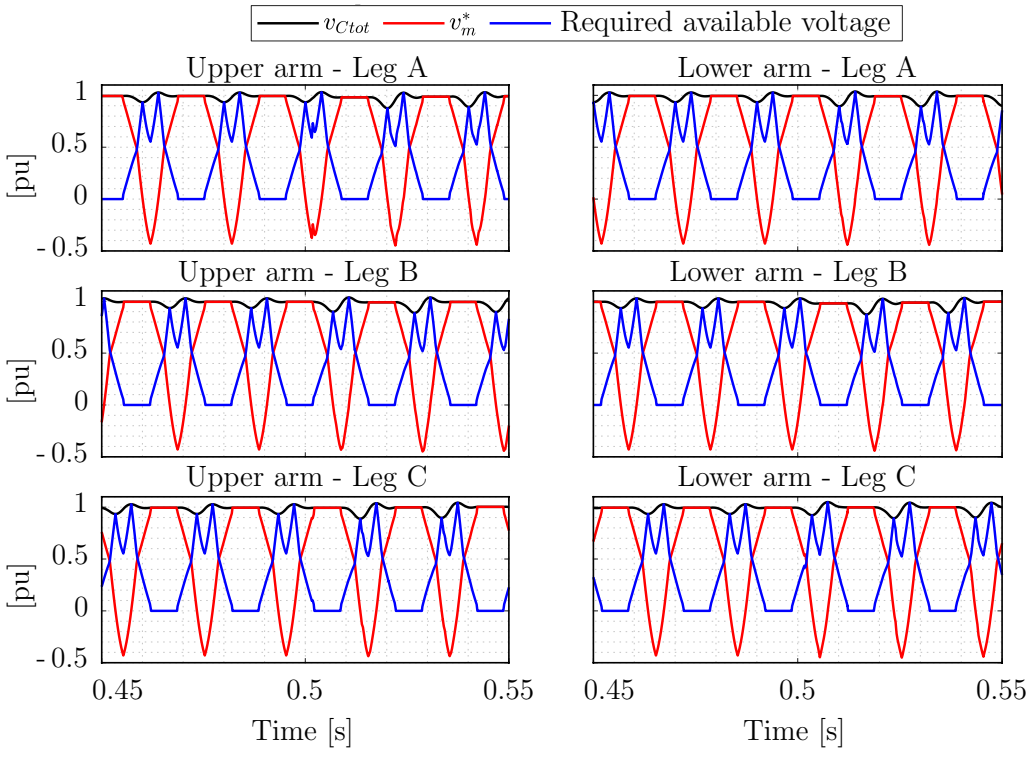

Figure 4.13 – Illustration of voltage availability in case of DC voltage support

As described in Chapter 2 and visible on Figure 4.13, v_{Ctot} is essentially composed of a second order harmonic, then, maximal and minimal values of v_{Ctot} are not corresponding with the peak values of v_m. On the red line is the reference for each v_m and in blue is the difference between v_{Ctot} and the absolute value of v_m^*. As shown by these graphs, the reference of v_m^* never exceed the value of v_{Ctot}, otherwise, the blue line would be negative.

Therefore, the EO-AAC is less sensitive to the choice of k_{vc}, which, as aforementioned, has no real interest to go above 1 under the considered conditions. However, more extensive studies, through iterative simulations in may be needed to confirm this claim.

Comparison of HVDC link based on ROM and detailed model of EO-AAC

The two above simulation results has proven that DC voltage support through EO-AAC thanks to the decoupling between p_{ac} and p_{dc} and the effort provided by the leg in overlap mode. This section is now interested in providing a small comparison between both models in order to attest of the validity of the ROM in spite of the power and DC voltage ripple introduced by the vertical and horizontal balancing controllers in the detailed model. The simulation scenario remains the same and each converter is providing DC voltage support with k_{vc} equals to 1.

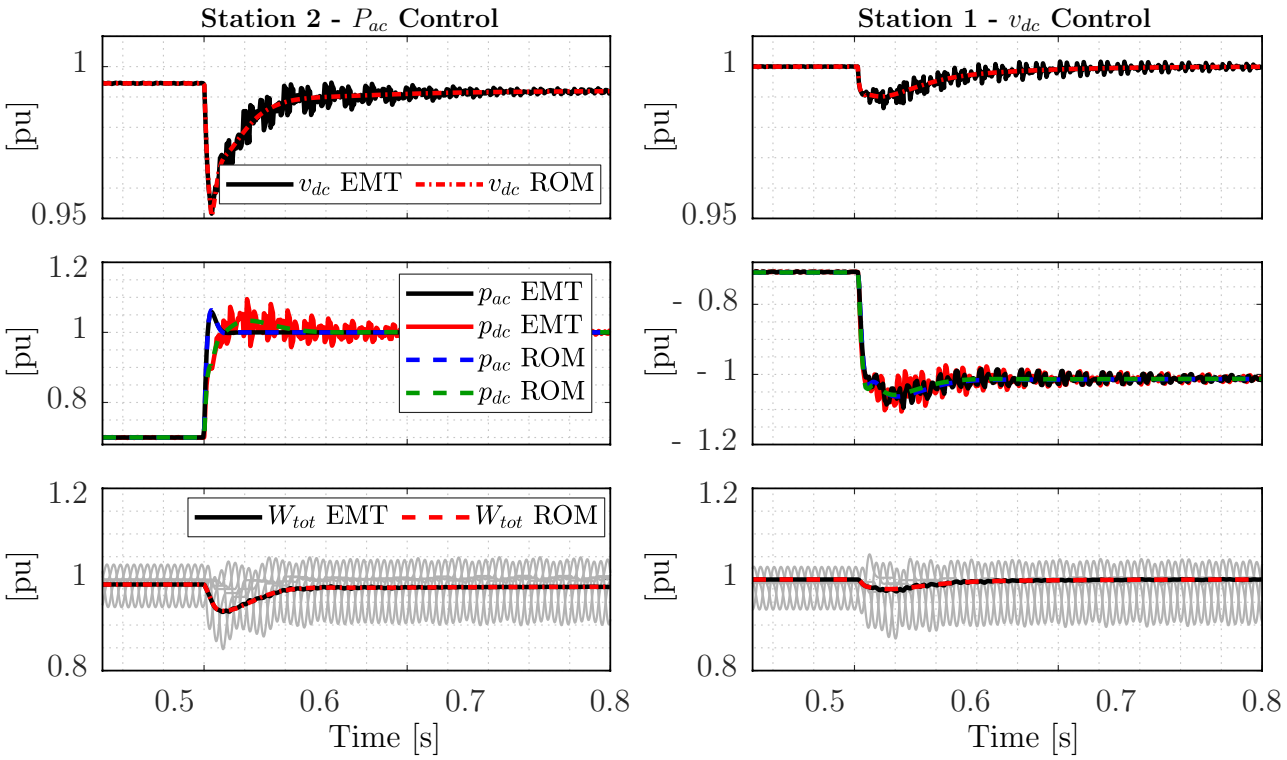

Figure 4.14 – Comparison of HVDC link comprising detailed model or ROM of EO-AAC

Results presented on Figure 4.14 highlight almost a perfect matching between each curve. Despite the ripples introduced by balancing controllers, both models have the exact same dynamics that confirms the interest of including EO-AACs for system studies in its reduced order form.

Inter-operation of EO-AAC and MMC

One of the possible future situation, with the development of HVDC system, is the inter-operation between different converter topologies. Some studies has tackled this point, for

example in the European project BestPath interoperability study including multi-vendor (and multi-controller) [164, 165] or more recently inter-operation of LCC and VSC with bi-polar voltage capability (e.g. FB-MMC) [166].

In this part, the interest is not on providing an exhaustive study of the possible inter-operations between structures, but a simple HVDC link interfacing a MMC and an EO-AAC. Each converter is equipped with a similar controller as detailed in Chapter 3. The MMC is therefore including total, horizontal and vertical controllers for outer layer of the control while the internal one includes AC, DC and circulating current controllers. The chosen configuration is: EO-AAC in v_{dc} control mode involving the MMC to control the power. Results are illustrated on Figure 4.15. Each converter is including $k_{vc} = 1$.

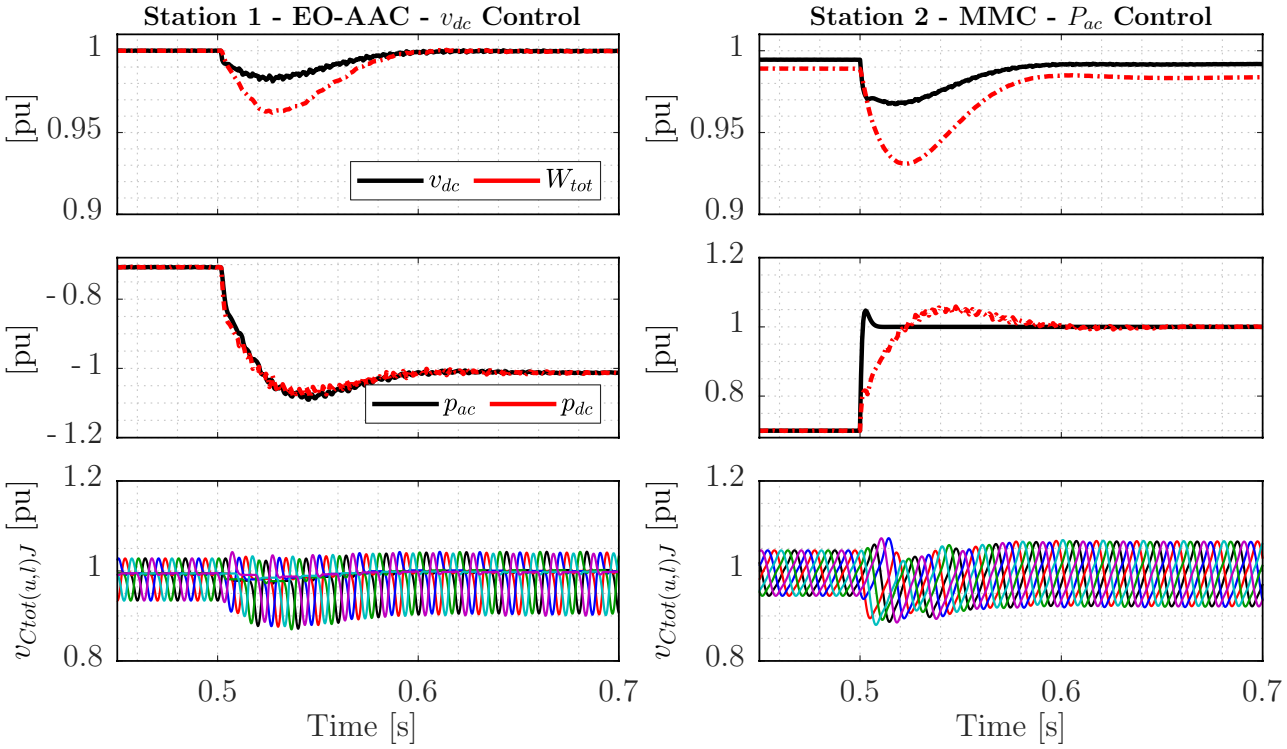

Figure 4.15 – HVDC Link including an EO-AAC and a MMC

First of all, the introduction of both types of station is properly working. From the point of view the authors, it clearly lies in their ability to control the DC current guaranteeing stability of the main DC link poles (i_{dc} and v_{dc}). The evolution of the DC voltage and power is smoother than the previous cases. This result comes from the higher amount of stored energy in the MMC which dictates the dynamics of the whole system. As an example, applying on MMC k_{vc} equals to 0.375 would increase the DC voltage dynamics by the same amount of energy than two EO-AACs and would leads to the exact same results obtained on Figure 4.13.

As a conclusion of this small study, which obviously deserves to be extended, the inter-operation of modular-converter topology may rely on their ability to control the DC current.

4.3 Control of a Multi-Terminal DC Grid

A multi-terminal DC (MTDC) grid is by definition composed of more than two converter stations. Associating a role to each converter, as it was done for the point-to-point configuration, becomes more complex. Therefore, a distributed approach is often used to mimic AC system primary frequency control. The distributed approach, also called droop-control, essentially operates on steady-state value to limit the frequency deviation by adjustment of the active power reference. Thus, each converter, or unit connected equipped with droop-control participate to the frequency regulation with its own capacity (participation as a fraction of the basis power e.g. 5%) to guarantee an expected frequency deviation in steady-state.

Reproducing the same principle for MTDC has been treated in different studies. As a general observation, there is a typical response equation governing a droop controlled DC system

$$\Delta p^*_{ac} = -\frac{1}{K_{\text{vdc}}}\Delta v_{dc} \tag{4.16}$$

The only difference lies in the derivation of the droop gain K_{vdc} which has been tackled in many works, involving either fixed [167–170] or adaptive [171] values. Nevertheless, it appears that in most of these works, due to the complexity of modelling and analysis of detailed MTDC system, an LTI model is developed in order to simplify the derivation of the droop gain. In this thesis, the focus was not on droop gain design so a methodology proposed in [169] has been used.

4.3.1 DC voltage droop gain design

A MTDC system comprising 3 modular converter stations is illustrated on the following figure.

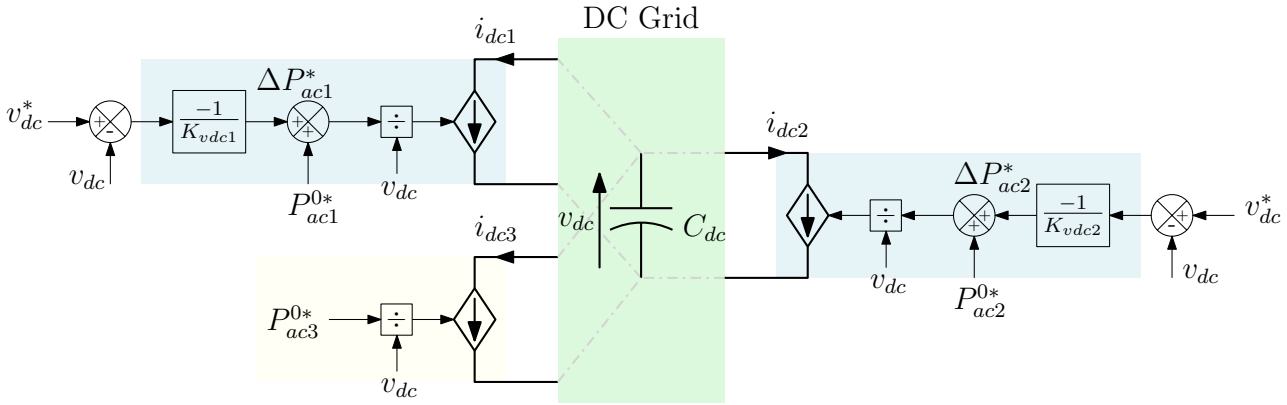

Figure 4.16 – Simplified 3 terminals MTDC grid

Each converter is modelled as a power injector feeding the DC grid equivalent capacitance C_{dc}. For the sake of simplicity, DC cables are merged and form an equivalent energy storage device which is the sum of each cable capacitance. Framed in blue are the converters equipped with droop controller (i.e. station 1 and 2) while station 3 is not. Assuming loss less converters, yields:

$$v_{dc} i_{dci} = p_{aci} \tag{4.17}$$

in case of exact modulation and fast tracking of current references gives:

$$v_{dc} i_{dci} = p^*_{aci} \tag{4.18}$$

it comes

$$C_{dc}\frac{dv_{dc}}{dt} = -\sum i_{dci} = \frac{-1}{v_{dc}}\sum p^*_{aci} \tag{4.19}$$

From this equation, an LTI model can be derived considering the equilibrium point ($\dot{x_0} + \dot{\Delta x}; u_0 + \Delta u$) such as

$$C_{dc}\left(\dot{v}_{dc0} + \Delta\dot{v}_{dc}\right) = \frac{-1}{v_{dc0} + \Delta v_{dc}}\sum p^*_{aci0} + \Delta p^*_{aci} \tag{4.20}$$

that gives after some derivations

$$C_{dc}\Delta\dot{v}_{dc} = \frac{-1}{v_{dc0}}\sum \Delta p^*_{aci} \tag{4.21}$$

where high order terms has been removed and quantities at the equilibrium point simplified.

Let us now introduce, N_S the number of stations and N_{Sd} the number of stations equipped with droop control. As shown by (4.21), the DC voltage deviations depends on the sum of Δp^*_{aci} provided by droop controllers. Then, the dynamics of the MTDC linearised model is given by the following equation in per-unit to deal with different power basis

$$\Delta v_{dc,pu} = \frac{\sum_1^{N_{Sd}} \frac{K_{vdci}}{P_{dcbi}}}{1 + \frac{v_{dc0}C_{dc}V_{dcb}}{\sum_1^{N_{Sd}} \frac{K_{vdci}}{P_{dcbi}}}s}\frac{P_{dcbi}}{V_{dcb}}\Delta p^*_{aci,pu} \tag{4.22}$$

with V_{vcb} the DC voltage base value, P_{dcbi} the DC power base value of the i station. This transfer function is derived in case of a power change of the i station. Then, the simplification under equally rated station has led to

$$\Delta v_{dc,pu} = \frac{\frac{K_{vdc}}{N_{Sd}}}{1 + \frac{K_{vdc}}{N_{Sd}}2H_{dc}s}\Delta p^*_{aci,pu} \tag{4.23}$$

The droop gain is therefore derived on the basis of the above transfer function DC gain:

$$k_{vdc} = \frac{N_{Sd}\Delta v_{dc}}{\Delta p^*_{aci,pu}} \tag{4.24}$$

As a result, the response time of the DC voltage is

$$\mathrm{tr}_{v_{dc}} = 3 \times \frac{K_{vdc}}{N_{Sd}}2H_{dc} \tag{4.25}$$

In the following, the droop gain will be chosen so that the external and internal loops of the control are decoupled (to avoid interaction and hence instability). This is done by setting external loops around ten times the dynamics of the internal. According to the previous sections, the internal loops in the control of the AC currents. By assuming, $\mathrm{tr}_{v_{dc}} = 10 \times \mathrm{tr}_{i_g}$, (4.25) is re-arranged to get:

$$K_{vdc} = \frac{10N_{sd}\mathrm{tr}_{i_g}}{6H_{dc}} \tag{4.26}$$

from this "maximal" DC voltage dynamics, the admissible ΔP_{ac} with respect to Δv_{dc} is determined to run the simulations.

$$\Delta P^*_{aci,pu} = \frac{N_{sd}\Delta v_{dc}}{k_{vdc}} \tag{4.27}$$

EMT simulation results

For the sake of simplicity a first simulation is carried out using reduced order models. To determine the values of K_{vdc} it is considered a DC voltage deviation of ± 10%, and only two stations equipped with a droop controller. Cable lengths are specified on Figure 4.17 leading to an equivalent capacitance of 76.8 μF equivalent to 15.7 kJ/MW of stored energy. According to (4.24) and (4.25), droop gain and voltage dynamics can be estimated according to $\Delta p^*_{ac,pu}$. A power system, to be resilient, needs to follow the principle of N-1 which involves that the system must remain in operation in case of the lost of one unit. In that case, it is one converter of 1 GW. The droop gain should be design on the basis of 1 p.u., but in the considered case, a limitation exist as highlighted on Figure 4.18.

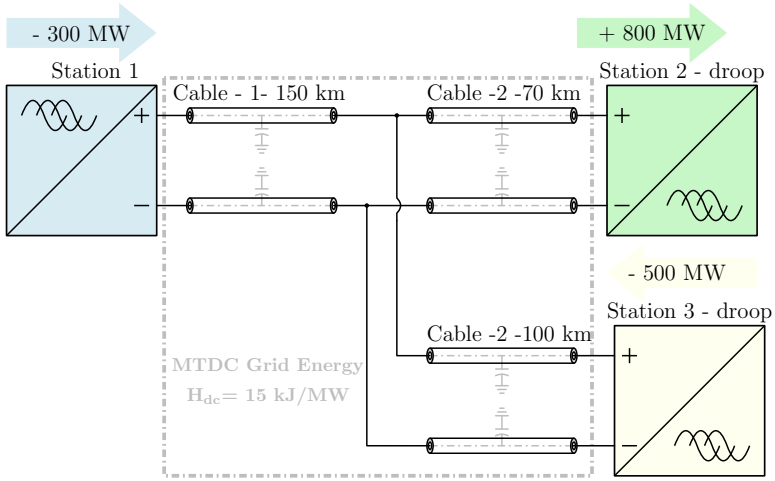

Figure 4.17 – Considered 3 terminals MTDC grid

Due to low stored energy in DC cables, the dynamics of the voltage highly increase with droop gain design. It results that the outer power loop gets closer to the AC current control dynamics until a stability limit is found around $\Delta p^*_{ac,pu} = 0.325$ p.u.

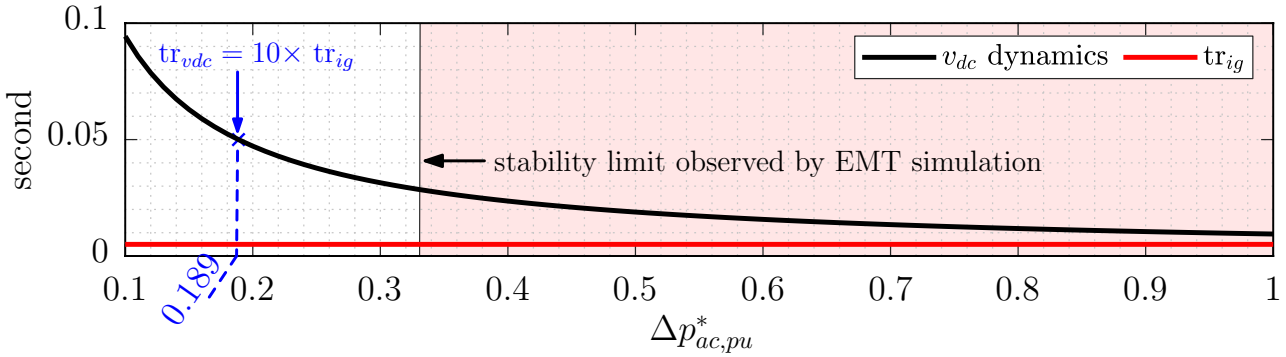

Figure 4.18 – Illustration of DC voltage dynamics according to $\Delta p^*_{ac,pu}$ and $\Delta v_{dc,pu} = 0.1$ p.u.

Thus, in that condition the principle of N-1 is not achieved. However, a first results is presented below which suppose the lose of station 1 and therefore 300 MW.

This simulation presented on Figure 4.19 operates closed to the stability limit. The DC voltage dynamics is near from 30 ms (i.e. six times the response of AC currents). The steady-state value of 0.9 p.u. is respected, however, interaction with the inner-loops creates oscillations on the DC voltage values at each converter terminals.

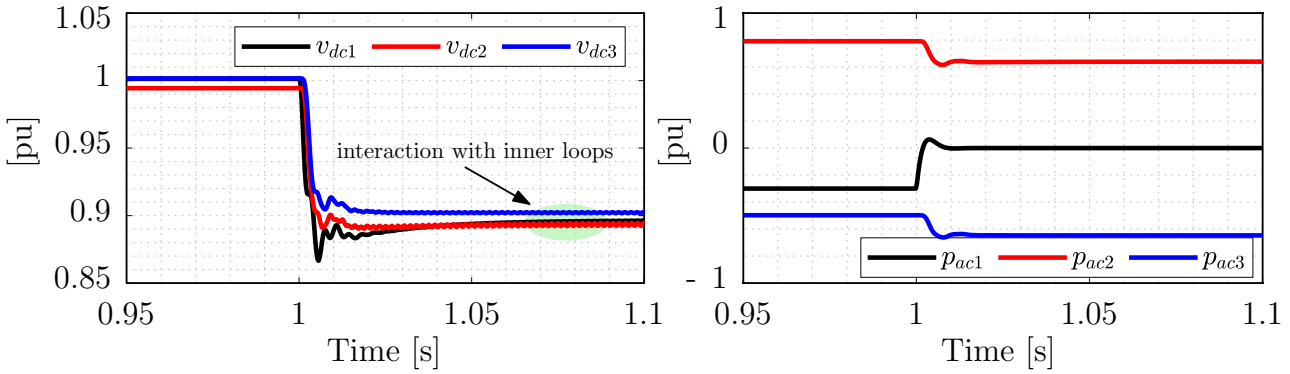

Figure 4.19 – Simulation of 3 terminals DC grid including 3 EO-AAC ROM and 2 droop controllers

4.3.2 Operation including converter's energy sharing

The use of the energy within converters to improve DC voltage dynamics was so far used to limit DC voltage deviation in point-to-point configuration. In droop-controlled MTDC system, the aim is not to limit the DC voltage deviation since the steady-state is defined by the droop gain, but to improve the system resilience. The idea is to increase the admissible $\Delta p^*_{ac,pu}$ while conserving the dynamics of the DC voltage ten times slower than the one of the AC currents. The next figure conceptualise the energy sharing in a MTDC grid which is the same as in the point-to-point configuration.

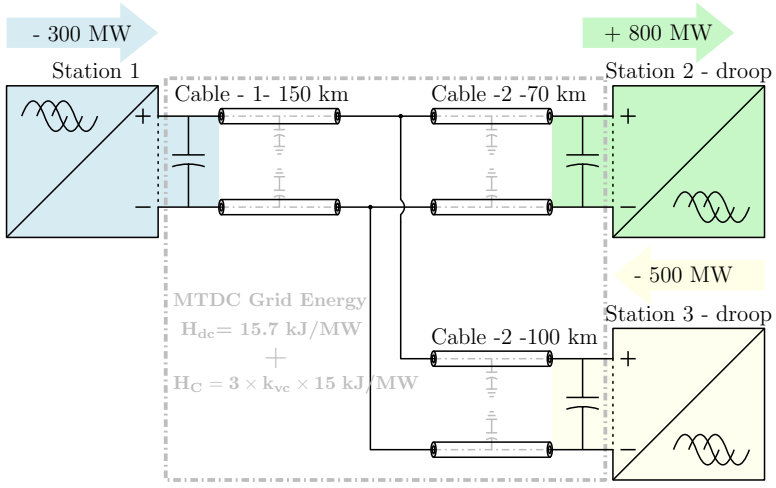

Figure 4.20 – Considered 3 terminals MTDC grid including converter's energy sharing

The energy sharing between converters and DC bus can be represented as a physical capacitor connected at the converter DC terminals. So, basically like 2-Level VSC including filter's capacitors. It results that the energy of DC grid becomes

$$H_{mtdc} = H_{dc} + 3k_{vc}H_C \tag{4.28}$$

if the converters are assumed to participate to the DC voltage dynamics. This additional functionality does not call into question the above derivations but just small update regarding the response time of v_{dc}.

$$\mathrm{tr}_{v_{dc}} = 3 \times N_{Sd} 2H_{mtdc} \tag{4.29}$$

Thus, as it was done in the previous case, the $\mathrm{tr}_{v_{dc}}$ can be plotted according to $\Delta p^*_{ac,pu}$.

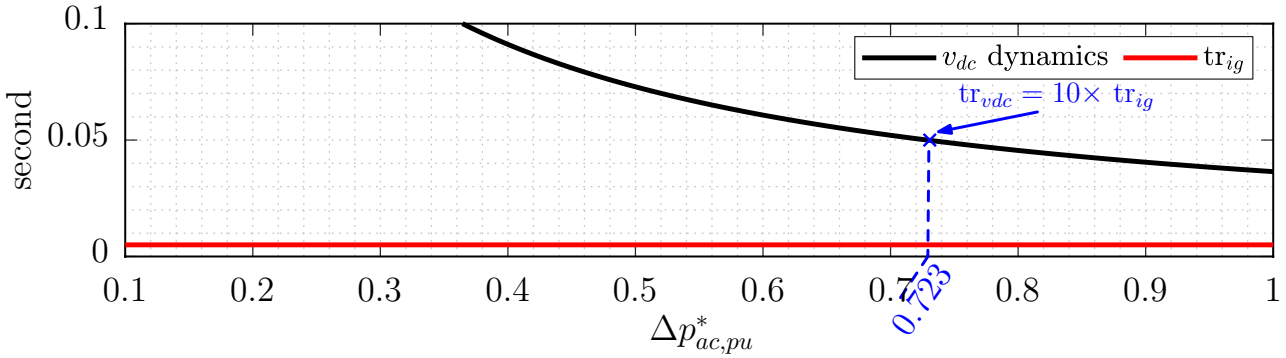

Figure 4.21 – Illustration of DC voltage dynamics according to $\Delta p^*_{ac,pu}$ and $\Delta v_{dc,pu} = 0.1$ p.u. for three EO-AACs sharing their internal energy

The energy within cables is approximately the same as in the EO-AAC, thus, the effective H_{mtdc} has been increased by four resulting in a shifting of the response time curve. For $\mathrm{tr}_{v_{dc}} = 10\times\mathrm{tr}_{i_g}$, the resilience of the MTDC system is nearly increased by four to reach 0.723 p.u. in terms power outage.

Simulation results for $\Delta p^*_{ac,pu} = 0.7$ p.u.

As in the previous simulation, the converter station 1 generates the DC power variation, which in this case is fixed to 0.7 p.u. meaning that the operating point of this converter goes from -0.3 to 0.4 p.u. The scenario is not realistic, however, the goal is to validate principles to reach detailed simulations including detailed converters.

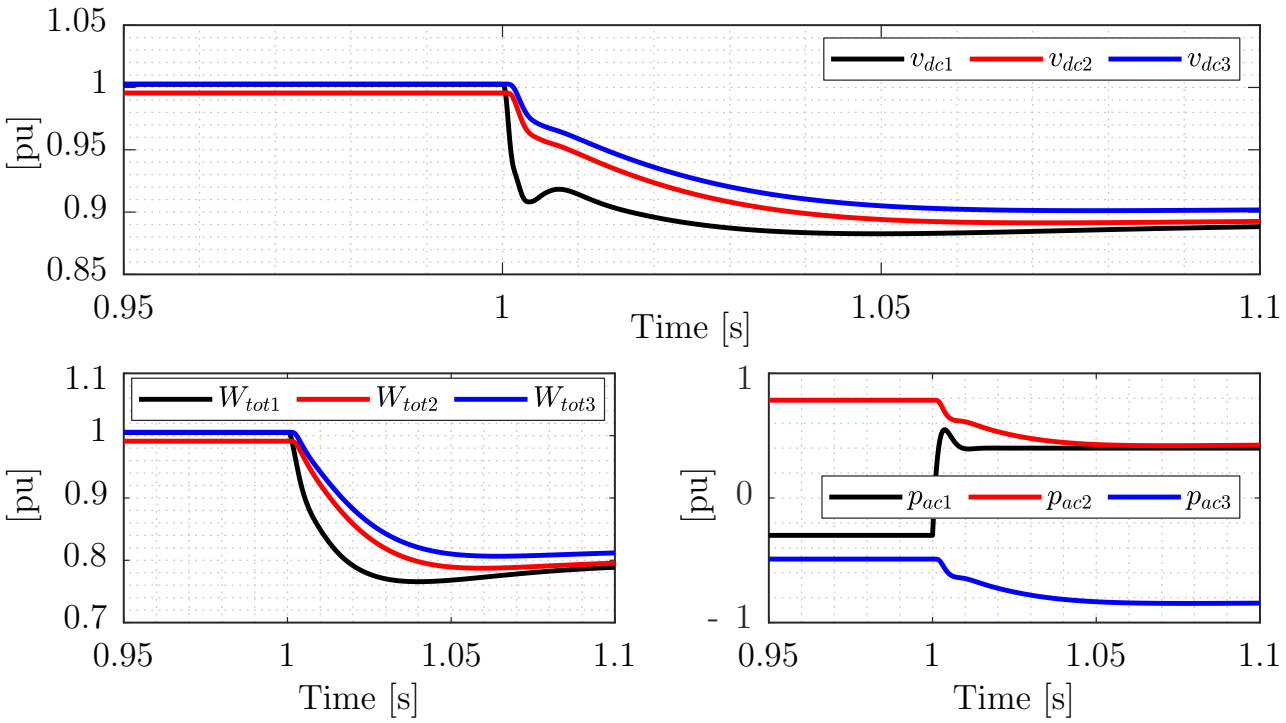

Figure 4.22 – Simulation of 3 terminals DC grid including 3 EO-AAC ROM sharing their internal energy and 2 droop controllers

Unlike Figure 4.19, these results shows an effective decoupling between inner and outer

loops since no oscillations are present on v_{dc} in steady-state. In addition, the DC system has been able to deal with the large DC power variation obtained at the expense of a large amount of energy deviation inside EO-AACs. The steady-state expression of the energy W_{tot} is given by (4.8) under the assumption that the energy is equal to its reference

$$W_{tot} = W_{tot0} + k_{vc}k_m^2\left(v_{dc}^2 - V_{dc0}^2\right) \simeq W_{tot0} - 0.19 \text{ p.u.} = 0.81 \text{ p.u.} \pm \text{ voltage drops} \quad (4.30)$$

Such decrease of the internal energy represent the main drawbacks of this technique to improve DC voltage dynamics. Moreover, as long as secondary and tertiary action does not bring the DC voltage closed to its nominal, the converter will run with this energy deficit. Thus, in [134], an improvement has been proposed to avoid steady-state energy deviation.

4.3.3 Operation under DC power derivative control

The principle of the DC power derivative control can be easily explained by recalling the DC voltage dynamics

$$\frac{1}{2}C_{dc}\frac{dv_{dc}^2}{dt} = p_l - p_{dc} \quad (4.31)$$

The difference is that now the DC voltage is controlled by the DC power. Therefore, the AC one must control the energy in the converter as in Chapter 3. However, to get DC voltage dynamics improvement, it is necessary to introduce a derivative term according to v_{dc}^2 giving the following reference of p_{dc}

$$p_{dc}^* = p_{dc0}^* + p_{k_{vdc}}^* + \underbrace{\frac{1}{2}C_{eq}k_d k_m^2\frac{dv_{dc}^2}{dt}}_{\text{Derivative action}} \quad (4.32)$$

with $p_{k_{vdc}}^*$ is the power reference arising from the droop control and k_d the derivative coefficient used to modulated the participation of the converter energy (similarly to the virtual capacitor coefficient). Assuming the DC power equals to its reference yields the effective voltage dynamics

$$\frac{1}{2}\left(C_{dc} + C_{eq}k_d k_m^2\right)\frac{dv_{dc}^2}{dt} = p_l - p_{dc0}^* - p_{k_{vdc}}^* \quad (4.33)$$

Interestingly, this derivative action allows keeping the energy reference to its nominal value since there is no more "strong coupling" between the reference of both side power references. However, if the energy is maintained constant despite the DC voltage support, then, the stress is reported on the AC side requiring a particular attention if a weak grid is interfaced. Applying this control strategy leads to the following control scheme

where, as shown by Figure 4.23, the derivative action is filtered to (i) respect causality principle and (ii) limit fast power changes. It is also notable that the disturbance compensation in the energy control is now optional. As above-mentioned, keeping the energy constant increases the stress on the AC side, however, it is possible to limit this stress by removing the disturbance compensation leaving the control doing this task with a slower dynamics. In the following both options are displayed.

Simulation results for $\Delta p_{ac,pu}^* = 0.7$ p.u.

Results presented on Figure 4.24 gives a similar behaviour obtained with "classical" energy sharing strategy, however, the derivative action slightly increase the reaction of the DC power

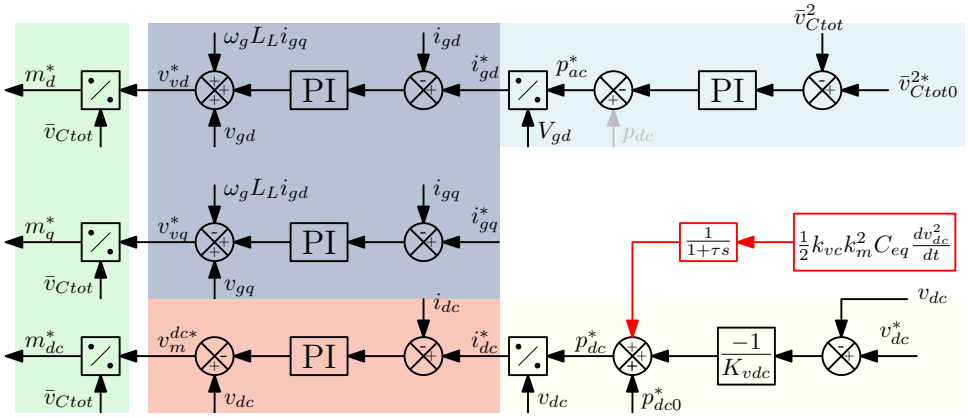

Figure 4.23 – Control structure of EO-AAC ROM using DC power derivative control

during event. To avoid high power spikes to be spread in p^*_{dc}, the cut-off frequency of the washout low pass filter has been set to 100 Hz corresponding to 10 times the DC current response time. The two last graphs shows that indeed, the converter energies return to their nominal state and AC power are smooth.

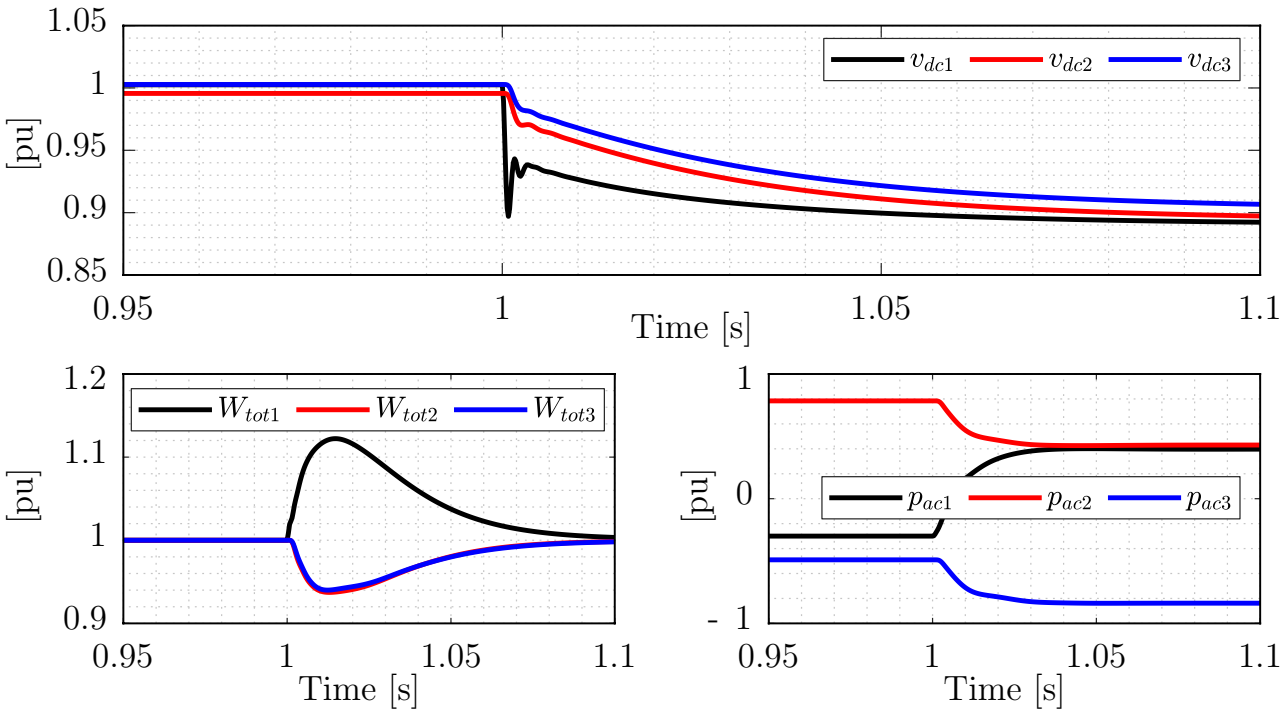

Figure 4.24 – Simulation of 3 terminals DC grid including 3 EO-AAC ROM using DC power derivative control and 2 droop controllers

As a conclusion, this second approach for DC voltage dynamics improvement in a MTDC system provides similar transients (depending on the washout filter tuning) while conserving a constant level of energy in steady-state. For this reason, the following simulations including detailed EO-AACs will be based on this control approach leaving aside the virtual capacitor control used so far.

4.3.4 Detailed EMT Simulations

Detailed converter models are now implemented in EMTP-RV software and interfaced through wideband cable models. As it was done for point-to-point configuration, the idea is to validate the overall behaviour compared to simulation including ROM. At the end of this section, different converter topologies are included.

Three EO-AAC stations

The performed simulation has its results presented on Figure 4.25. As in the HVDC point-to-point link, transient DC voltage oscillations are observed due to the need for vertical and horizontal balancing currents. However, results are very similar to those obtained with ROM showing the effectiveness of the controllers and the converter to deal with large DC power deviation.

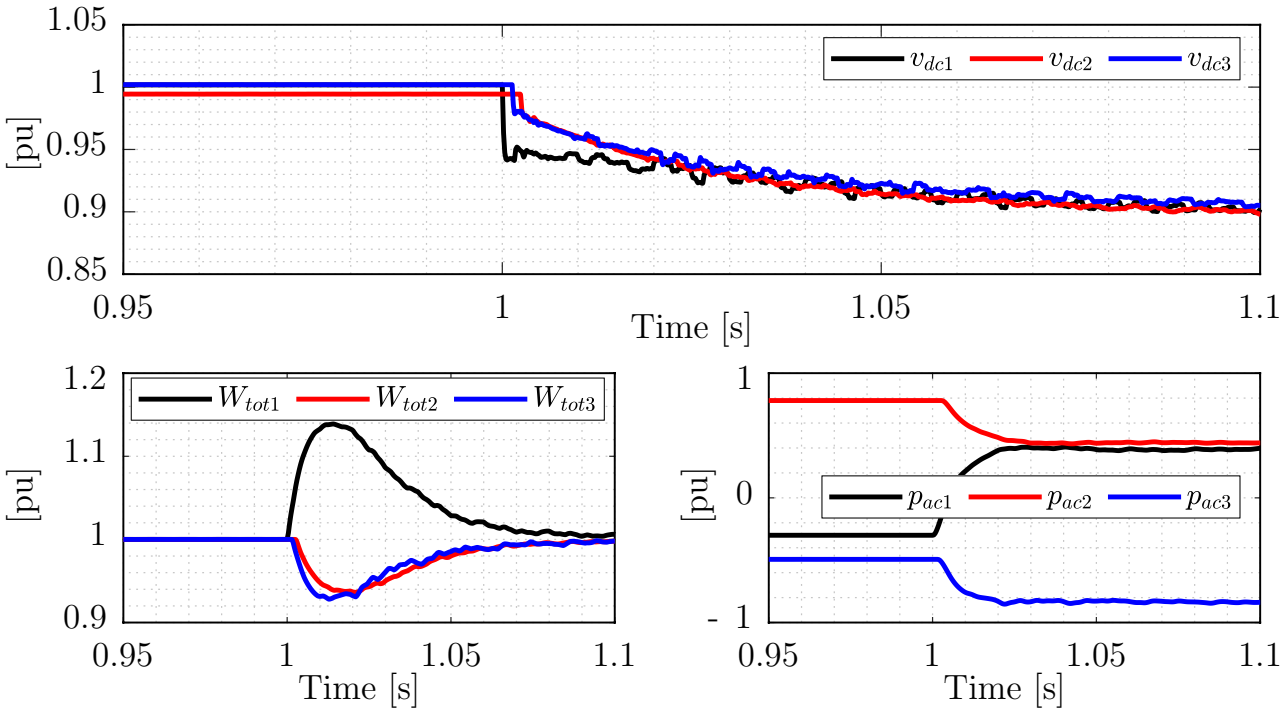

Figure 4.25 – Simulation of 3 terminals DC grid including 3 EO-AACs using DC power derivative control and 2 droop controllers

Interoperation of EO-AAC and MMC stations

This case consider the HVDC station 1 to be replaced by a MMC. The MMC, as in the point-to-point HVDC link is equipped with an energy management in xyz basis and a derivative control of the DC power. Since the MMC embeds more energy than the EO-AAC, for the same $\Delta P_{ac,pu}$ (0.7 p.u.) the dynamics of the DC voltage will be slower.

Results are presented on Figure 4.26, the time scale remains the same as the previous simulation, hence, the steady-state is not reached since the DC voltage dynamics is slower. Nevertheless, as in the case of the HVDC link, the interoperation between these two different topologies is achieved.

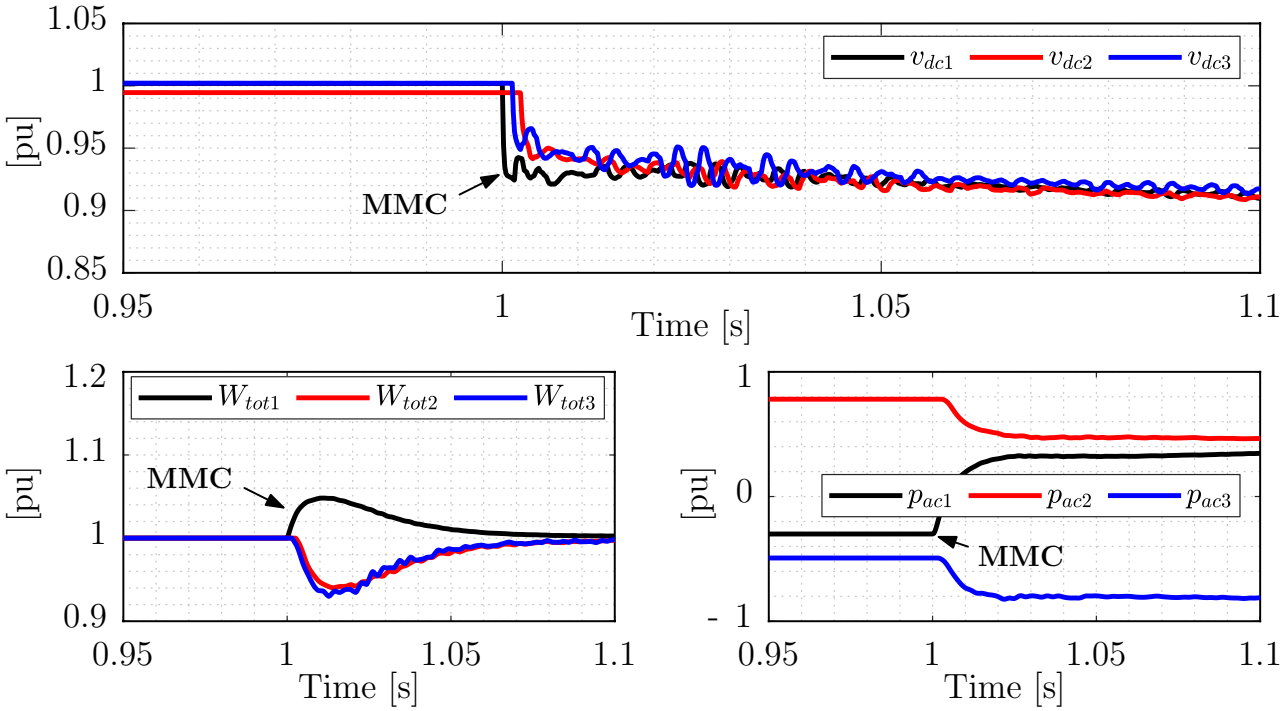

Figure 4.26 – Simulation of 3 terminals DC grid including 2 EO-AACs and 1 MMC using energy controllers

In [152] it is detailed that control parameters also highly impact the interaction between different stations and their potential interoperation. Then, more detailed study should be addressed by modifying control parameters since this work consider the same closed-loop dynamics for EO-AACs and MMCs.

4.4 Operation during abnormal conditions

The above sections have presented the main results that may be obtained with an EO-AAC connected to to a DC system and nominal conditions. The operations under abnormal conditions such as the DC-fault or unbalanced AC system are now presented. This section intends to provide some understanding about the most critical points during these operating modes and solutions to be explored in future works.

4.4.1 DC-Fault

The DC-Fault operation of the AAC (all overlap length included) has been investigated in some works [74, 172] and practically validated in [71, 173]. It is admitted that as long as $|v_m|$ is lower than v_{Ctot}, then, thanks to the FB-SMs the DC fault blocking capability is obtained.

However, the energy appears as being uncontrolled during such conditions. However, to keep the DC-fault blocking capability it is important to maintain the level of energy inside each stack.

Analysis of the control strategy

When the DC-Fault occurs, it is necessary for the stations to be switched into current limitation mode. Here, it is chosen to cut off the power to avoid short-circuit feeding. In this

section, let us assume one station dealing with a DC-fault where v_{dc} is zero. Once the fault is detected and over-current protection activated, the active power is set to zero. During such condition, let us highlight in a very simple way the possible choices to maintain the energy stable:

$$\frac{dW_{tot}}{dt} = -p_{ac} \tag{4.34}$$

$$\frac{d\bar{W}_{\Delta(x,y)}}{dt} = -P_{ac(x,y)} \tag{4.35}$$

$$\frac{d\bar{W}_{\Delta J}}{dt} = -2V_{vJ}I^{ac}_{\Sigma J} \tag{4.36}$$

As shown by these models, which are simplified compared to Chapter 3, for leg energy controllers (i.e. total and horizontal) it possible to use the AC side active powers. On the other hand, the vertical balancing controllers has no choices than using AC component in the overlap current. However, the fact there is only one leg in overlap mode means that these AC components will be, transiently, visible on the DC current despite the fault.

Simulation results

To illustrate the above analysis, a time domain is performed based on the following simplified HVDC link.

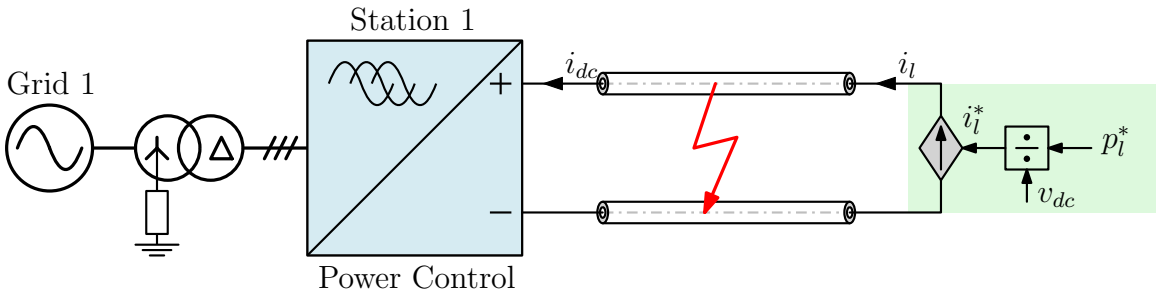

Figure 4.27 – Illustration of the consider HVDC link of DC-Fault response test

A converter station in active power control mode is considered to be interconnected through DC cables to a power injector. The DC fault occurs at 0.4 seconds. The converter initially operates in normal conditions at the rated power 1.044 GVA using DC power based energy management. Once the DC-Fault is detected, the total and the horizontal controllers switch to AC power while the reactive power is maintained constant. Results are as presented on Figure 4.28.

On the first graph is depicted the DC voltage measurement at the EO-AAC terminals. At the fault occurrence, the DC voltage quickly drops enforcing protections (over-current essentially) of the power injector and the EO-AAC to cut off the power. AC and DC powers are presented on the second graph. This fast transient on active power needs for energy re-balancing. As visible on v_{dc} and p_{dc} there is small ripple introduced by the vertical balancing controllers.

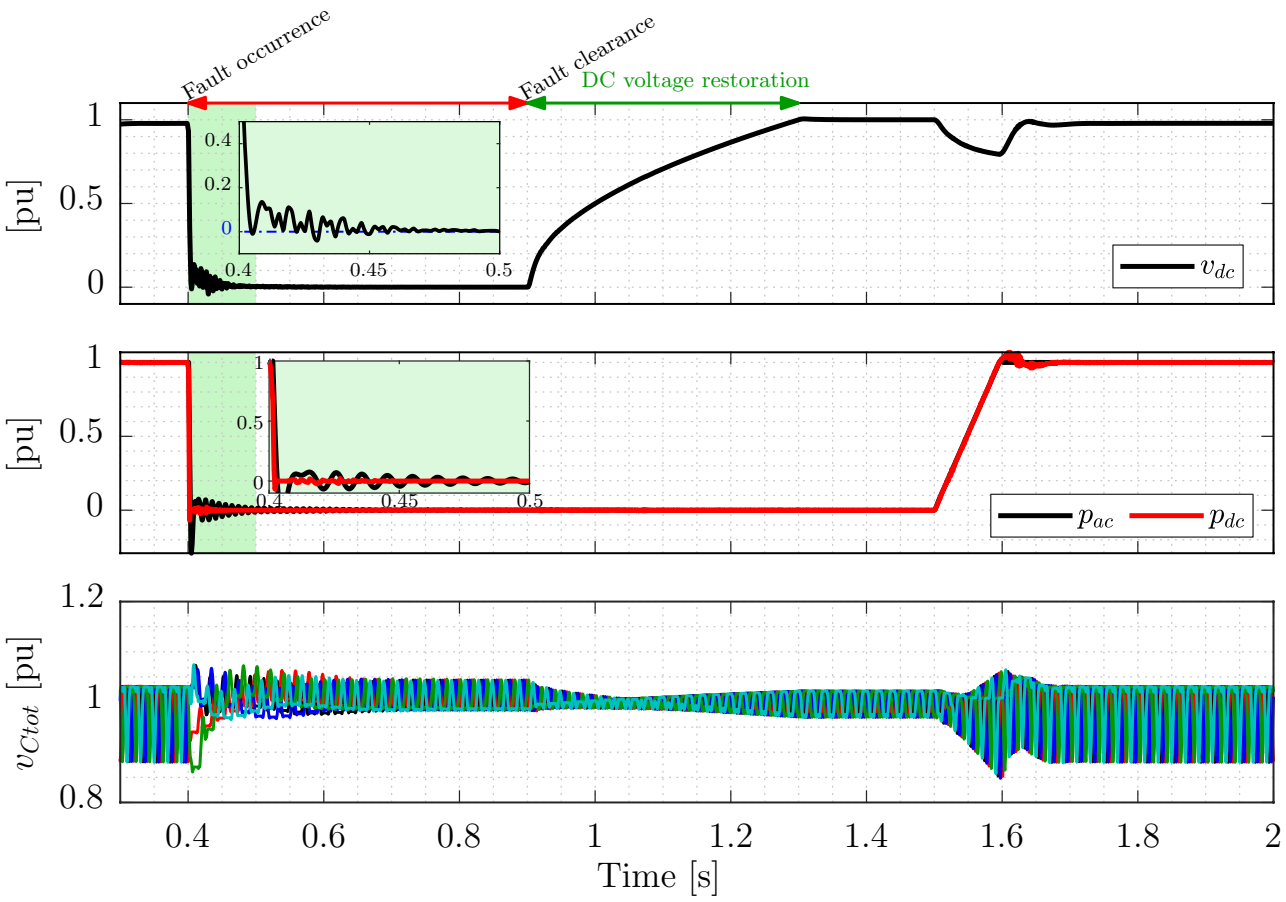

Figure 4.28 – Simulation of the EO-AAC response to a DC-Fault

Consideration about the DS control

The above simulation has not considered any changing on the DS control. However, there is degree of freedom that have been detailed in [147] and stated below.

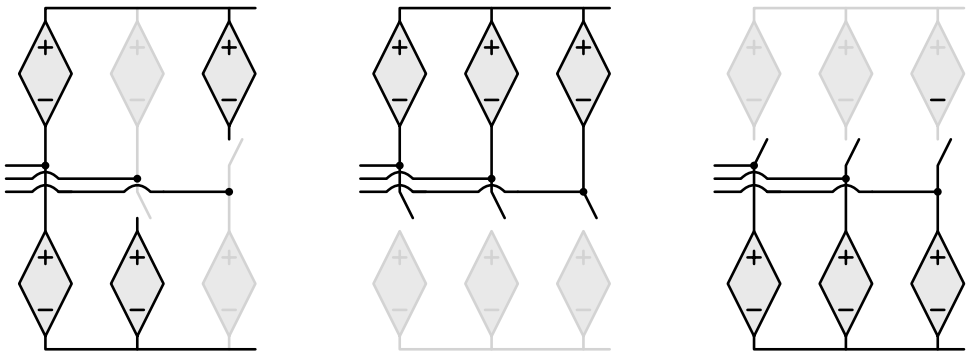

Figure 4.29 – Illustration of the different DS control modes of the EO-AAC in case of DC-Fault

The Mode A is the normal mode which means that no modification is done on the DS control. The modes B1 and B2 are the upper and lower single-star modes that require to activate all DSs of each upper or lower arms.

Since the above section was based on the mode A, to achieve single-star STATCOM operation it is necessary to slightly reconsider the energy management. The difference between the modes A and B lies in the vertical balancing. Indeed, once the upper or the lower stacks are isolated, then, the vertical balancing must deactivated. The total and the horizontal controllers remains as in (4.34) and (4.35).

4.4.2 Unbalanced AC system

This section provides some results about the EO-AAC response to unbalanced AC system. The aim of this section is to highlight issues to be tackled for maintaining as constant as possible to the DC side power and the DC voltage in order to avoid potential instability of other stations due to oscillations. Faulty conditions like phase-to-ground will not be considered.

Control Modification

To achieve constant DC power during transient and steady-state, a small modification of the control strategy is necessary. Assume an unbalanced AC system, in abc frame the AC side power is expressed as:

$$\begin{aligned} p_{ac} =& V_{gA}I_{gA}\cos(\varphi A) + V_{gB}I_{gB}\cos(\varphi_B) + V_{gC}I_{gC}\cos(\varphi_C) \\ & \underbrace{-V_{gA}I_{gA}\cos(2\theta_g+\varphi A) - V_{gB}I_{gB}\cos(2\theta_g+\varphi_B) - V_{gC}I_{gC}\cos(2\theta_g+\varphi_C)}_{\text{No more sums up to zero}} \end{aligned} \tag{4.37}$$

By considering the expression of the total energy

$$\frac{dW_{tot}}{dt} = p_{dc} - p_{ac} \tag{4.38}$$

W_{tot} is now containing oscillations at twice the fundamental frequency. Therefore, p_{dc} is not constant. To maintain the DC power harmonics free, a simple approach is considered. The fundamental idea is to enforce the total energy to act as a buffer avoiding oscillations to be spread on the DC side.

The first modification to be done is the use of filter on W_{tot} measurement. The filter allows the controller to provide a constant power reference. However, it needs to decrease the bandwidth of the total controller. Until now, the response time was to 50 ms, now it is set to 100 ms. At this stage, two choices are possible and summarised on the next schemes.

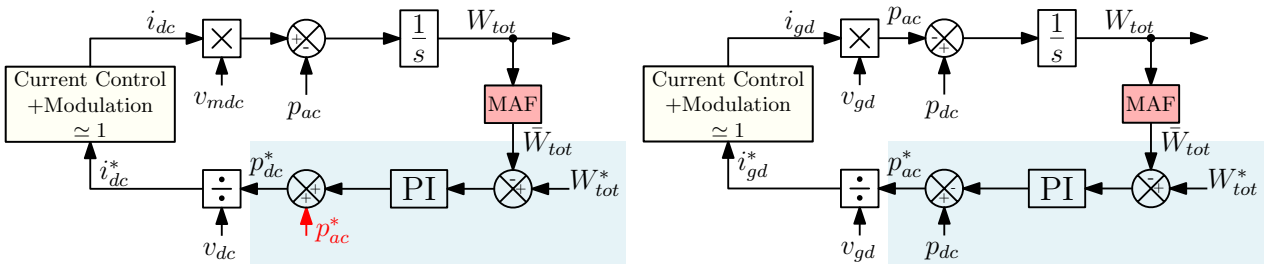

Figure 4.30 – Total energy control loop providing constant DC power reference in case of unbalanced AC system: a) DC power approach b) AC power approach

If the DC power based approach is considered then the disturbance compensation (p_{ac}) should be based on its reference p^*_{ac}. Hence, if the MAF is properly tuned, the DC power reference is constant. If the AC power controls the energy, then, no other modifications are necessary.

Presentation of the test case

The converter is assumed to be interfaced through a transformer and an unbalanced appears on the primary side of the transformer. For the sake of simplicity, these voltages are called v_{gJ} as in the previous chapters. Waveforms are as it follows:

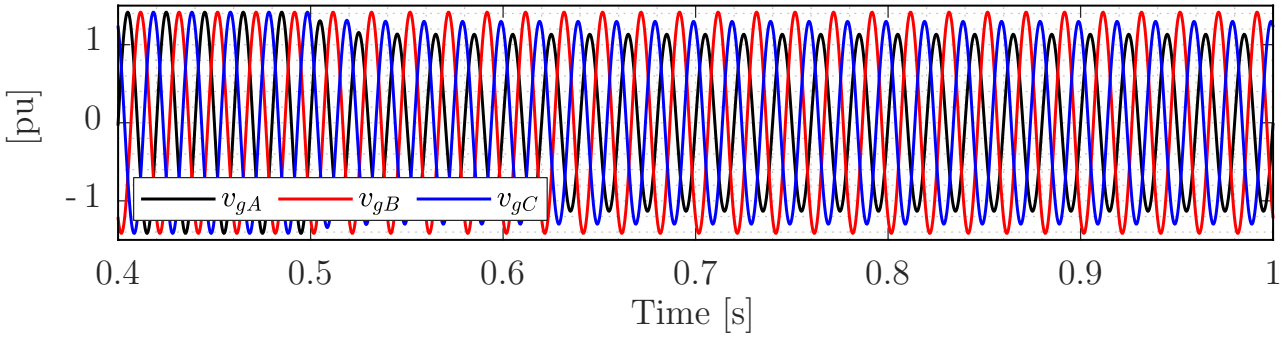

Figure 4.31 – Illustration of the unbalanced AC voltage test case

The transformer arrangement makes the zero sequence voltage equals to zero. As a result it is obtained $V_{gA} = 0.8$ p.u., $V_{gB} = 1$ p.u. and $V_{gC} = 0.9$ p.u.

MMC response to unbalanced AC system – DC power based energy control

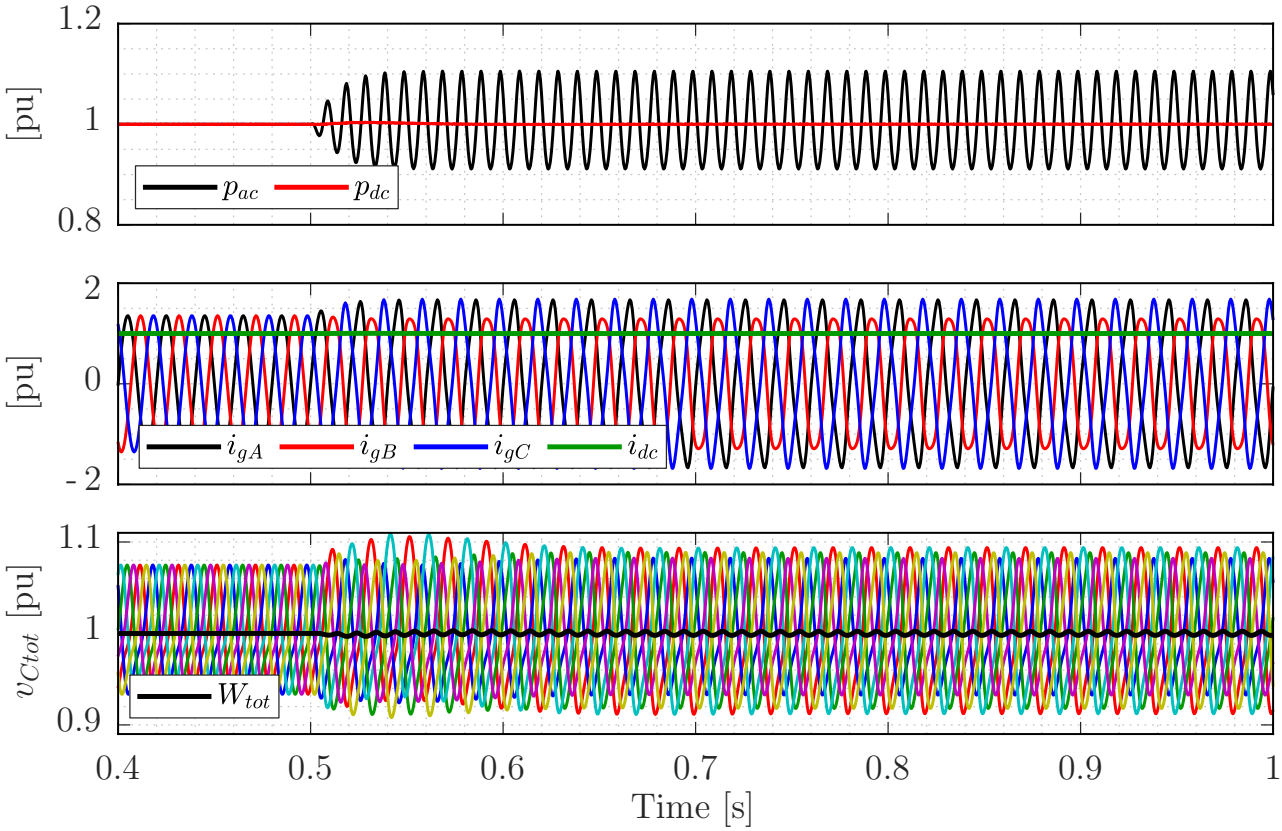

Figure 4.32 – Response of a MMC to a voltage unbalance performing constant DC power

The voltage unbalance is applied at 0.5 second. It results in an oscillatory term in p_{ac}. As shown by Figure 4.32, the DC power is maintained constant and W_{tot} acts as a buffer. As the

negative sequence remains uncontrolled, non-sinusoidal modulated voltage are generated and a second order harmonic appears in the AC currents.

This simulation has illustrated that MMCs can absorb AC side power oscillations to keep DC side quantity constant. This feature is almost natural when using total energy control in average value. Of course, it is possible to improve this result by appropriate reference calculation of the negative sequence currents.

Now, let us consider the EO-AAC.

EO-AAC response to unbalanced AC system – DC power based energy control

The same scenario as above is simulated. The total energy is now based on Figure 4.30 and the bandwidth of the total energy control reduced. Results are presented on Figure 4.33.

Similarly to the MMC, since the total energy is controlled in average value, then, a constant DC current reference ($i_{dc,wtot}$ of Chapter 3) is obtained. However, simulation result shows that the DC power and the DC current are highly rippled. The energy is transiently disturbed and returns to its nominal level in steady-state (now shown on this figure which focus on the transient).

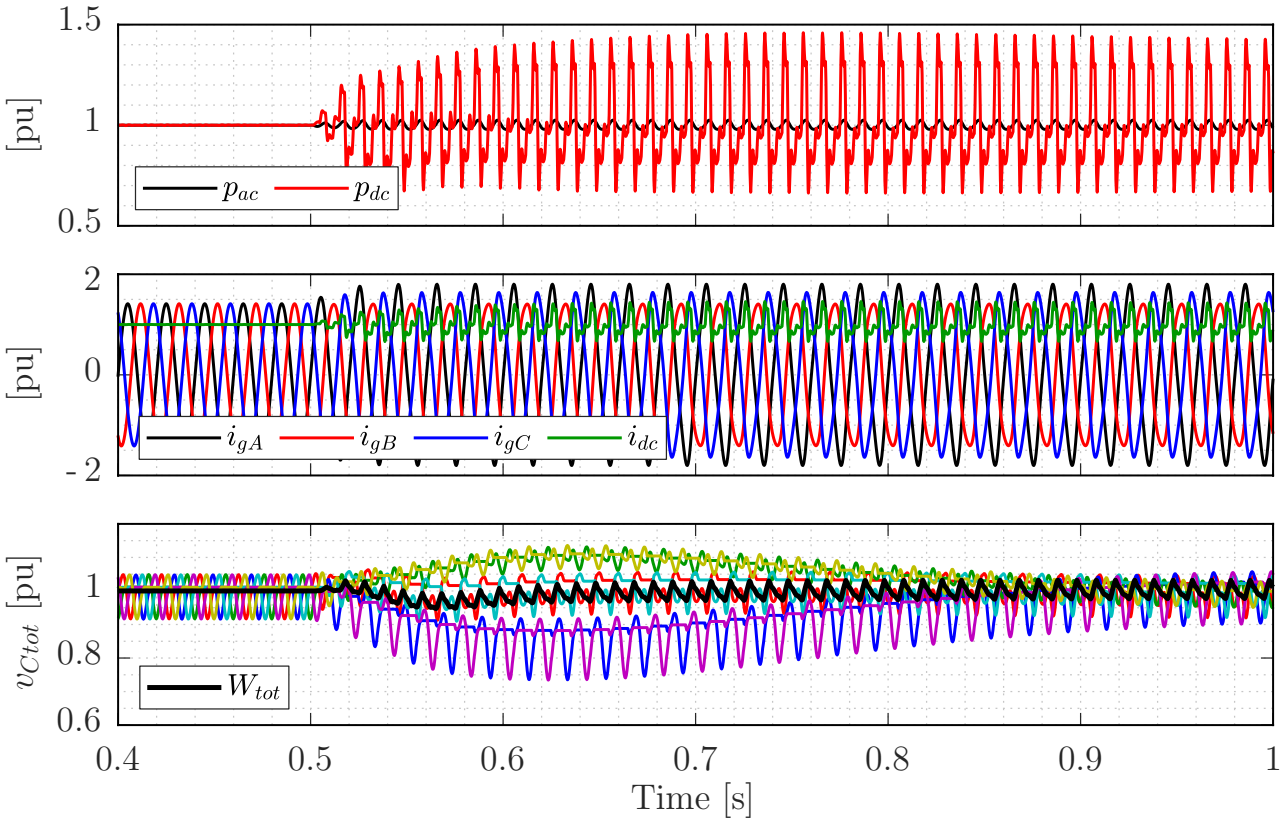

Figure 4.33 – Response of a EO-AAC to a voltage unbalance performing constant DC power

To explain this result, the expression of the leg energy deviation ($W_{\Sigma J}$) is recalled.

$$\frac{d\bar{W}_{\Sigma J}}{dt} = v_{dc} i_{\Sigma J} \left(\frac{\theta_{ovl}}{\pi}\right) + P_{acJ} \left(\frac{4}{m_J \pi} \cos\left(\frac{\theta_{ovl}}{2}\right) - 1\right) \tag{4.39}$$

In case of an unbalanced system, modulation index m are no more balanced, then they are called m_J and still defined as

$$m_J = \frac{2\hat{V}_{vJ}}{v_{dc}} \tag{4.40}$$

In steady-state it is obtained:

$$i^*_{\Sigma J} = \frac{1}{v_{dc}} \left[P_{acJ} \left(1 - \frac{4}{m_J \pi} \cos\left(\frac{\theta_{ovl}}{2}\right)\right)\right] \left(\frac{\theta_{ovl}}{\pi}\right) \tag{4.41}$$

Thus, from the above equations it appears that the amplitude of each $i_{\Sigma J}$ must be different in case of unbalance AC voltages. These amplitudes are calculated by the horizontal controllers. As a result, since there is only leg in overlap mode, then, this difference of amplitude will be observed on the DC current explaining the large DC power oscillation of Figure 4.33. This is depicted on the next figure.

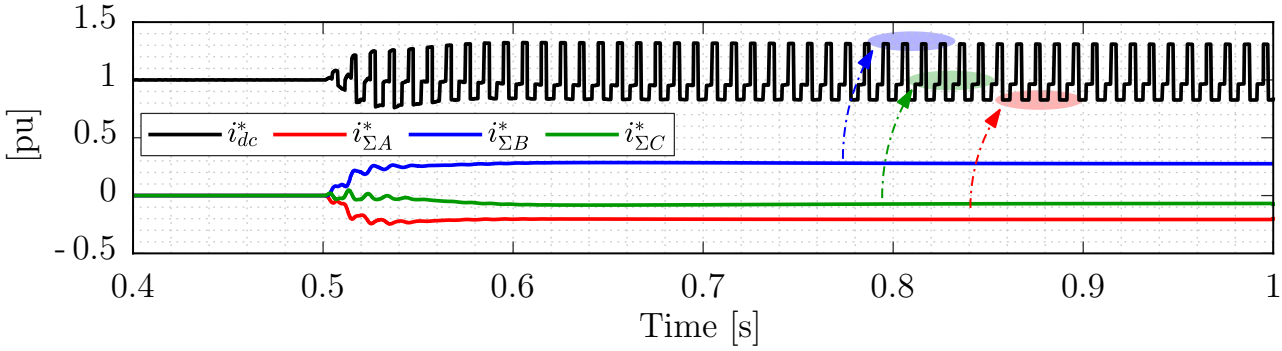

Figure 4.34 – Illustration of the Horizontal balancing current references and the DC current reference

To avoid this large DC power oscillation caused by the horizontal balancing, by using (4.39) only one solution is possible :

To control the AC side so that the AC voltages and singled-phased active power are balanced. In thee-wire system, negative sequence currents provide to additional degree of freedom to the control. However, these degree of freedom are often related to the removal of active and reactive power oscillations [174], thus, questioning the feasibility of this solution.

As a second degree of freedom to improve this large harmonics injection on DC current, the AC power based energy controller may be interesting.

EO-AAC response to unbalanced AC system – AC power based energy control

The total and the horizontal balancing controllers are now based on the AC side power. The vertical balancing remains unchanged. The same simulation has been performed leading to the result of Figure 4.35.

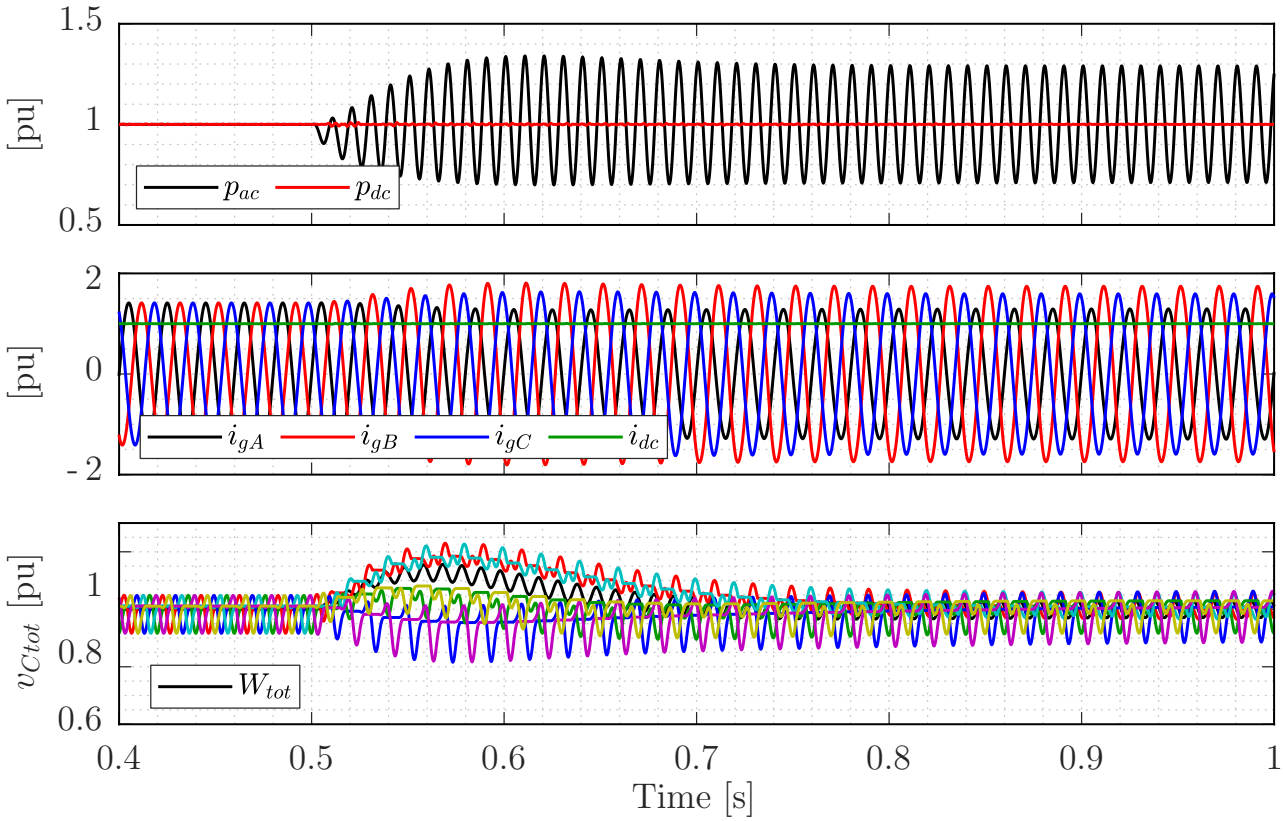

Figure 4.35 – Response of a EO-AAC to a voltage unbalance performing constant DC power - AC power based energy control

Figure 4.35 confirms that maintaining ripple free DC current in steady-state is possible by using AC power based horizontal balancing control. There is a small transient ripple due to the vertical which goes back to zero in steady-state with respect to its dynamics. However, due to the unbalanced single-phased modulation index, the AC side active power in each leg cannot be balanced (fixed by the need for energy balancing). Thus, a large second order harmonic due to the unbalanced active power references is observed. In that case, a proper management of the negative sequence preserving the stability of the horizontal balancing control loop would benefit to the system.

4.5 Conclusion

In this chapter the application of connection to the HVDC and HVAC grid (to a lesser extent), has been detailed.

Through these studies different facts were established through simulations and demonstrated with the dynamic models derived in chapter 3. Thus, the similarity in the behaviour of MMC and EO-AAC converters led us to propose the use of the converter's internal stored energy in order to support the DC voltage during transient events. Interestingly, it was observed and then demonstrated that the use of this type of strategy is greatly beneficial for the converter because it makes it possible to reduce the adjustment effort of the horizontal balancing control loops which are very sensitive to the modulation index.

A similar approach has been taken in the case of a radial MTDC system. The use of energy from converters allows a fictitious increase in the equivalent energy of the DC grid, thus improving its resilience (e.g. in case loss of a generator). It has also been shown that interoperating with the MMC is possible. The explicit control of the DC current contributes to this possibility.

Finally, the cases of the DC fault and the unbalanced AC system highlighted some limitations of the EO-AAC and future works. Using horizontal and vertical balance control with a sequential system such as AAC does not keep harmonics internally like the MMC would. This property was particularly observed in the case of unbalanced AC system.The high sensitivity of the horizontal balancing to the balance of active powers and modulation indices (in single-phase) does not make it possible to maintain a constant DC power if this later is in charge of the energy management. On the other hand, if the AC power is responsible for the energy control then it is possible to maintain DC quantities constant, but the power oscillations at twice the fundamental frequency are high.

In summary, the horizontal balancing controller are very sensitive to the HVAC and HVDC grid voltages due to their sequential behaviour. This control loops would deserve a special attention in order to improve the steady-state performances of the EO-AAC connected non-perfect AC and DC sources.

Conclusions and Future Research

Power electronics devices and DC systems are the keys to enhance the integration of remote renewable sources as well as the reinforcement of some regions. The Modular Multilevel Converter has proven to be the most suitable topology to met with these objectives. However, emerging topologies combining on one hand the modular aspect of the MMC and features of the most simple AC/DC converters (e.g. six-pulses bridges) as the Extended Overlap-Alternate Arm Converter may challenge the MMC.

This Thesis aims at studying the operations, the design and the control of the EO-AACs. In the following, the main Chapter conclusions are summarized:

1. A methodological approach explaining the origin of the AAC topology and the main operating principle of the EO-AAC have been detailed in Chapter 1. The main idea behind the AAC topology is to operate at the same time two types of modulation schemes: the basic *full-wave (or square-wave)* and the *modulated voltage* controls. However, each scheme has its own specificities. The full-wave modulation requires the converter to operate as a voltage source by fixing the AC voltages magnitude but the angle is a degree of freedom. Modulated voltage control allows providing the voltage magnitude and its angle as degrees of freedom. When combined, a converter with half of the MMC SM requirement is obtained, but, its operation is restrained to certain modulation index fixed by the full-wave modulation and the DC current is still a modulated quantity containing a large six pulse ripple. The overlap mode is introduced to enable the implementation of an energy control scheme ensuring the power balance in the converter and recently extended until a dedicated active filtering strategy of the DC current can be implemented. This is the EO-AAC.

2. The EO-AAC needed more SMs per stack to achieve the active the active filtering of the DC current. Then, the Zero Sequence Voltage Injection (ZSVI) technique has been performed to decrease the number of SMs. Thus, Chapter 2 has followed the impact of the ZSVI on the sizing of the power devices, the SM capacitance and losses estimation. Thus, this study reveals that to achieve DC-Fault blocking at AC high voltage about 25% less SMs is needed than the MMC. The energy requirement is the range of 10-15 kJ/MVA. Losses are estimated to be similar to the HB-MMC operating at low modulation index (i.e. less than 1). However, with small improvement the HB-MMC will remain more efficient that the EO-AAC.

3. In Chapter 3, an overall assessment of the controllers have been detailed. From the low-level controller, a requirement has been clearly highlighted. The need for a proper compensation of SM capacitor voltage ripple is highly important to maintain an efficient active filtering of the DC current. As a second part of the chapter, the high-level control was detailed showing the control of AC and DC currents and stacks energy. A combination has been proposed achieving a continuous control of the Total energy. Two

other controls, purely sequential are achieved for the purpose of horizontal and vertical balancing. There sequential behaviours involve a transient injection of harmonics on the AC or DC power. However, thanks to some continuous dynamics it is proven that the EO-AAC performs similar dynamics than MMC as supported by the developed reduced order model. Thus, the main conclusion of this chapter is equivalence of both converters from the grid perspectives.

4. To study the dynamics of the converter when connected to the grid, Chapter 4 provides several test cases based on EMTP-RV software. Thus, it is first presented a way to achieve DC voltage support through converter's internal energy initially designed for MMC. This was possible thanks to the continuous control of the total energy based on the DC power. Gathering all controllers designed so far and DC voltage control techniques, point-to-point HVDC links as well as MTDC has been simulated showing the effectiveness of the EO-AAC. Moreover, some test about interoperation of MMC based on open and closed control were carried out showing the good performances of the whole system even in case of MMC with CCSC control. Finally, some opening concerning the energy management in case of DC-fault, unbalanced AC system were presented.

Through the work carried out during this thesis, it is possible for us to give a general opinion on the EO-AAC topology. From the design and footprint point of view, this topology is extremely interesting because it allows operation similar to the MMC with a reduced number of components and conductive arms. However, this last point is also what seems to be the main limitations of this topology as highlighted in the last Chapter 4. For instance, in the case of energy control by the DC power, several operations are ensured by a single leg of the converter (active filtering, total, horizontal and vertical controls). Thus, whenever a potential imbalance occurs this lack of controllability and this high sensitivity to the modulation index can be a problem.

Despite a mitigated conclusion on the EO-AAC topology, it should be noted that the study of such complex topologies (the EO-AAC is one among others) allowed us to take a step back on how to control some classical structures such as the MMC, modular STATCOM based on the methodology developed in this thesis.

Future Research

From this Thesis, various works are still required to fully exploit the EO-AAC:

- As pointed out in the Chapter 1 and several publications, the DS switching times are highly involved in the energy deviation. In this thesis, it was chosen to minimize stacks ratings by synchronising DS control and modulated AC voltages. However, as highlighted in M.M.C Merlin's thesis, with some mathematical manipulation it can be shown that angles may be involved in the horizontal and vertical balancing and therefore be used to control these quantities.
- The unbalanced situation with DC side power based horizontal balancing is critical case. One of the solution that should be investigated lies in the generation of balanced single-phased active powers and voltages, if it is possible. A second solution is by using DS control angles, but the design part should be re-addressed.
- Fast transients may occurs in 100% power electronics based power system. As highlighted in Chapter 3, the vertical balancing is highly disturbed if the transient is faster the arm rotation cycle. A proper choice of the reference saturation, control dynamics may

be required. Also the use of a DC component in the common mode voltage may be investigated, especially its impact on transformer, protection etc...

- In Chapter 4, and recently in [166], the question of the interoperation between AAC and MMC or LCC has been tackled. With the proposed controllers, most of these questions (about EO-AAC and MMC) has been solved by the reduced order model, however, more investigations would be interesting for EO-AAC/LCC and more.
- Finally, according to the first Chapter, the EO-AAC topology has been obtained by integration of several function into the full-wave controlled 2-Level VSC: Active filtering of the AC voltages and the DC current. However, for both active filtering function, it is possible to have an external system to perform it. Typically, an external stack connected in parallel to the DC bus dedicated to the DC current filtering. Thus, the absorption of the current at the output of the converter will be independent from the horizontal balancing controllers. It would results in a constant DC current in any cases.

More generally, the work that has been done in this thesis, and especially the methodology that has been applied could be applied to different hybrid topologies combining LCC and stack of SMs.

These last 4-5 years, the question of a power system without synchronous machine has found a response in the grid forming control of solid state device. As pointed in [175], to limit frequency deviation, these converters equipped with grid forming control which are supposed to provide synchronous machine-like behaviour (i.e. synthetic inertia). However, in some conditions the overload capability of a converter may be reached calling into question the current design of high voltage stations. Among these solutions, the evolution Silicon Carbide (SiC) devices may propose, in the future, significant improvement over Si devices. But they should first met with the actual standard (about 3 kV and 1.5 kA).

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Appendix A

The Short Overlap-Alternate Arm Converter

The original publication of the AAC was considering that the overlap should be limited. After the publication of the EO-AAC in 2018, this "first" AAC topology has been called "Small Overlap"-AAC (SO-AAC). In this appendix, some key points about this topology are detailed.

As the EO-AAC, the SO-AAC alternates between Non-overlap and Overlap operating modes. However, since the overlap period is less than 60 degrees, then, some times there is no leg in overlap mode. As a result, the DC current is not regulated during a few ms per grid cycle and therefore a dedicated a filter is needed since the converter behaves as a basic current rectifier from the DC side perspectives. The topology and its filter are recalled on the next figure.

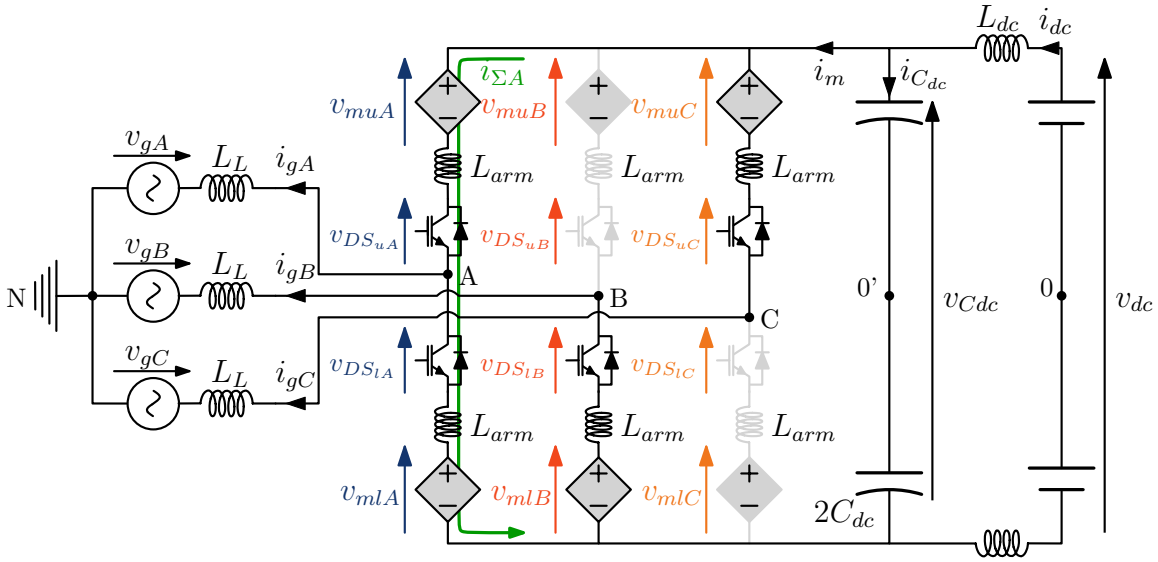

Figure A.1 – The SO-AAC

For the SO-AAC, there are three important points to be considered :

1. The current control on the DC side
2. The commutation process of the DSs at turn-off
3. The energy management

Regarding other operations, there are to the EO-AAC

A.1 Modelling and Control of Currents in SO-AAC

Most the ideas provided in this appendix can be found in [89]. There are two main differences between an EO-AAC and a SO-AAC regarding the current dynamics modelling.

A.1.1 AC current dynamics modelling

First, let us consider the AC side dynamics. If the leg is in **Non-overlap mode** it is obtained:

$$\begin{aligned} v_g + (L_L + L_{arm})\frac{di_g}{dt} + (R_L + R_{arm})\, i_g + v_{mu} - \frac{v_{Cdc}}{2} + v_{N0'} = 0 \\ v_g + (L_L + L_{arm})\frac{di_g}{dt} + (R_L + R_{arm})\, i_g - v_{ml} + \frac{v_{Cdc}}{2} + v_{N0'} = 0 \end{aligned} \tag{A.1}$$

Let us now define the expression of the voltage v_v used to drive AC powers according to (A.1).

$$v_v = v_g + (L_L + L_{arm})\frac{di_g}{dt} + (R_L + R_{arm})\, i_g \tag{A.2}$$

so that

$$\begin{aligned} v_{mu} &= \frac{v_{Cdc}}{2} - v_v - v_{N0'} \\ v_{ml} &= \frac{v_{Cdc}}{2} + v_v + v_{N0'} \end{aligned} \tag{A.3}$$

which are very similar to the EO-AAC equations. Actually, the main changes between both topologies regards the equivalent impedance of the AC side (Z_L for the EO-AAC and $Z_L + Z_{arm}$ for the SO-AAC).

Concerning the **Overlap mode**, the voltage v_v, used to drive the AC currents, has a new expression. Indeed, during the operating mode, the AC current can be fairly assumed to be equally split between both converter arms leading to the following expression:

$$v_v = v_g + \left(L_L + \frac{L_{arm}}{2}\right)\frac{di_g}{dt} + \left(R_L + \frac{R_{arm}}{2}\right) i_g \tag{A.4}$$

The Equation (A.4) shows that using arm inductors and overlap operating modes introduces a time-varying equivalent impedance of the AC side. Indeed, the impedance in overlap mode is now $Z_L + Z_{arm}/2$. However, in most of the works made on this topology, this variation of the AC side impedance is neglected since the transformer leakage impedance is often much larger than the arm inductors thanks to the FB-SMs. Since, in average, the converter legs are mostly in Non-overlap mode, then, the chosen value of the equivalent impedance for the control design is $Z_L + Z_{arm}$.

Based on these models, the AC side currents will be used to control the active and reactive powers on the AC side using the dq components as in Chapter 3.

A.1.2 Overlap current dynamics modelling

Once the leg goes into the overlap operating, a MMC like behaviour can be performed. One of the MMC feature is the control of the DC components in its arm currents. The SO-AAC

can reproduce this feature by controlling the Overlap current called i_Σ in Figure A.1.
From the DC side perspectives it can be written:

$$v_{Cdc} = v_{ml} + L_{arm}\left(\frac{di_l}{dt} + \frac{di_u}{dt}\right) + R_{arm}\left(i_l + i_u\right) + v_{mu} \tag{A.5}$$

From the MMC litterature, it is well-known that summing upper and lower quantities allows to isolate the DC components, so i_Σ (the overlap current) and the voltage driving this current v_Σ. Their definitions is given below:

$$\begin{aligned} i_\Sigma &= \frac{i_u + i_l}{2} \\ v_\Sigma &= \frac{v_{mu} + v_{ml}}{2} \end{aligned} \tag{A.6}$$

Then, it yields:

$$\frac{v_{Cdc}}{2} = v_\Sigma + L_{arm}\frac{di_\Sigma}{dt} + R_{arm} i_\Sigma \tag{A.7}$$

This model, is exactly the same for MMC. However, due to the temporary nature of the overlap mode, the control of each overlap current (three legs...) is sequentially activated.

A.1.3 Control structure and validation

Based on the above models, a control structure can be derived by model inversion. It is depicted bellow.

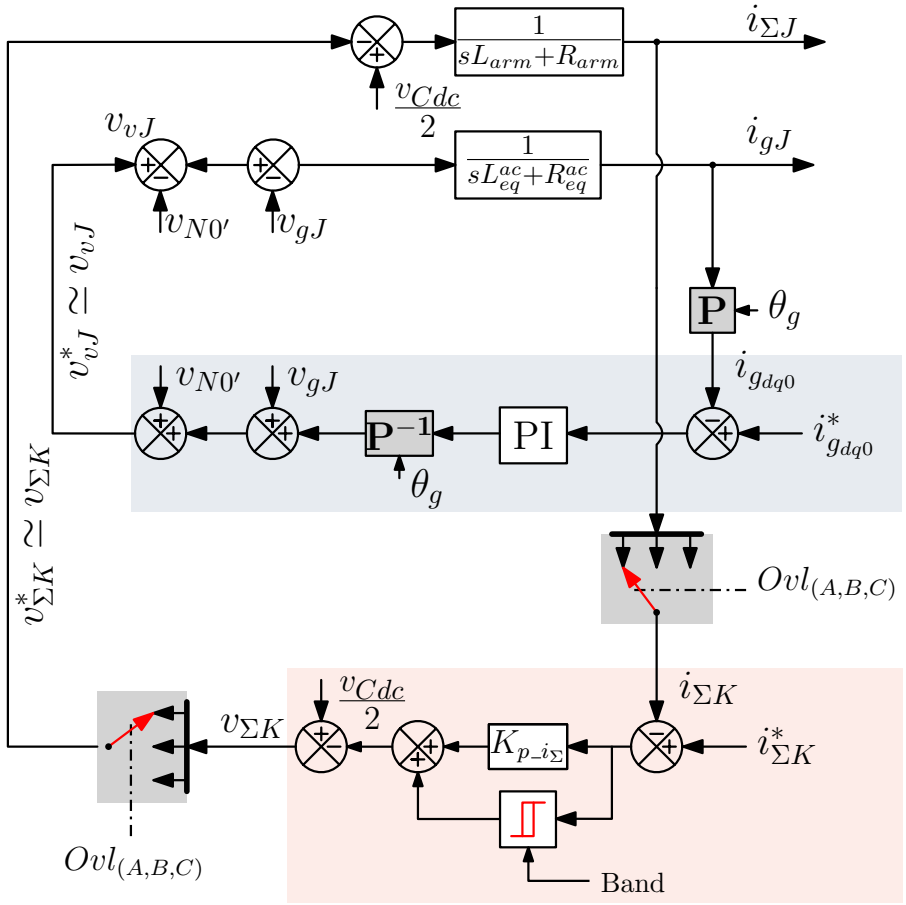

Figure A.2 – Current controllers of the SO-AAC

As visible on Figure A.2, the current control on the AC remains the same to the EO-AAC one. In that case, the equivalent impedance is considered:

$$\begin{aligned} L_{eq}^{ac} &= L_L + L_{arm} \\ R_{eq}^{ac} &= R_L + R_{arm} \end{aligned} \tag{A.8}$$

For the following, L_L has its value equals to 0.15 p.u. (113 mH) while L_{arm} is set to 0.01 p.u. (8 mH). Both parasitic resistance are set to 0.005 p.u. (1.2 Ω).

Regarding the control of the overlap current, since it has to be sequential, selectors are introduced. Thus, the legs in non-overlap mode operate in open-loop while the leg in overlap mode indicated by the index K on Figure A.2 operates in closed-loop. The most common solution to control the overlap current is the hysteresis controller which allows having a zero average steady-state error and a fast dynamics. However, this controller often activates (positively or negatively) only one SM to control the current, so, to improve the behaviour of the current control (in some cases where more than one SM could be needed) an additional proportional gain is used.

Overlap current controller tunning:
The hysteresis band is derived based on the following derivations:

$$\begin{aligned} \frac{v_{Cdc}}{2} &= v_\Sigma + L_{arm}\frac{di_\Sigma}{dt} + R_{arm}i_\Sigma \\ \frac{v_{Cdc}}{2} &\simeq v_\Sigma + L_{arm}\frac{\Delta i_\Sigma}{\Delta t} \end{aligned} \tag{A.9}$$

Considering

$$\frac{v_{Cdc}}{2} - v_\Sigma = v_{Hyst} \tag{A.10}$$

yields:

$$\Delta i_\Sigma = \frac{v_{Hyst}\Delta t}{L_{arm}} \tag{A.11}$$

with Δt chosen according to the controller frequency f_c (Time step T_c). Let us suppose the hysteresis band fixed to a given value, it should met with:

$$\frac{L_{arm}\Delta i_\Sigma}{v_{Hyst}} \geq T_c \tag{A.12}$$

In this appendix, a controller frequency of 50 kHz is considered while the hysteresis controller is assumed to activate only one SM, so v_{Hyst} is assumed to be closed 1.6 kV in average (thanks to voltage balancing algorithm). The hysteresis band is fixed to 20 A (slightly more than 1% of the DC current in case of 1 GW and 640 kVdc). It yields:

$$\frac{L_{arm}\Delta i_\Sigma}{v_{Hyst}} = \frac{0.008 \times 20}{1600} = 100\mu s \tag{A.13}$$

About five controller time steps.

The proportional gain is essentially used to furnish, transiently, more SMs for the overlap current controller (as any linear/non-linear controller response during a transient). This gain is calculated as it follows:

$$K_{p_{i_\Sigma}} = \frac{L_{arm} - R_{arm}\mathrm{tr}_{i_\Sigma}}{\mathrm{tr}_{i_\Sigma}} \tag{A.14}$$

with tr_{i_Σ} the desired dynamics of the overlap current.

Validation through EMT simulation

The first figure present the response of the AC current loops.

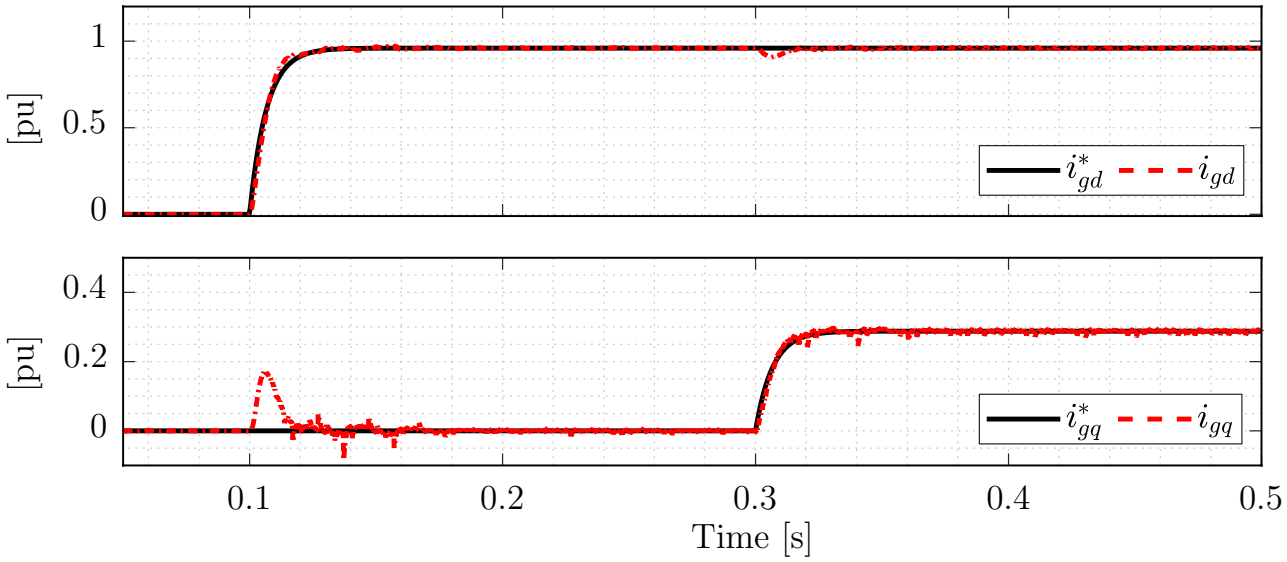

Figure A.3 – Validation of AC current controllers of the SO-AAC

Controllers are tested against active and reactive power reference changes. Due to the time-varying equivalent impedance on the AC side, there will be in steady-state a small six pulse ripple on the both active and reactive powers. Nonetheless, references are easily tracked.

Regarding the overlap current control, this controller always has to deal with transient since the overlap mode is activated et deactivated twice per grid cycle. Thus, focusing on one single grid cycle is sufficient.

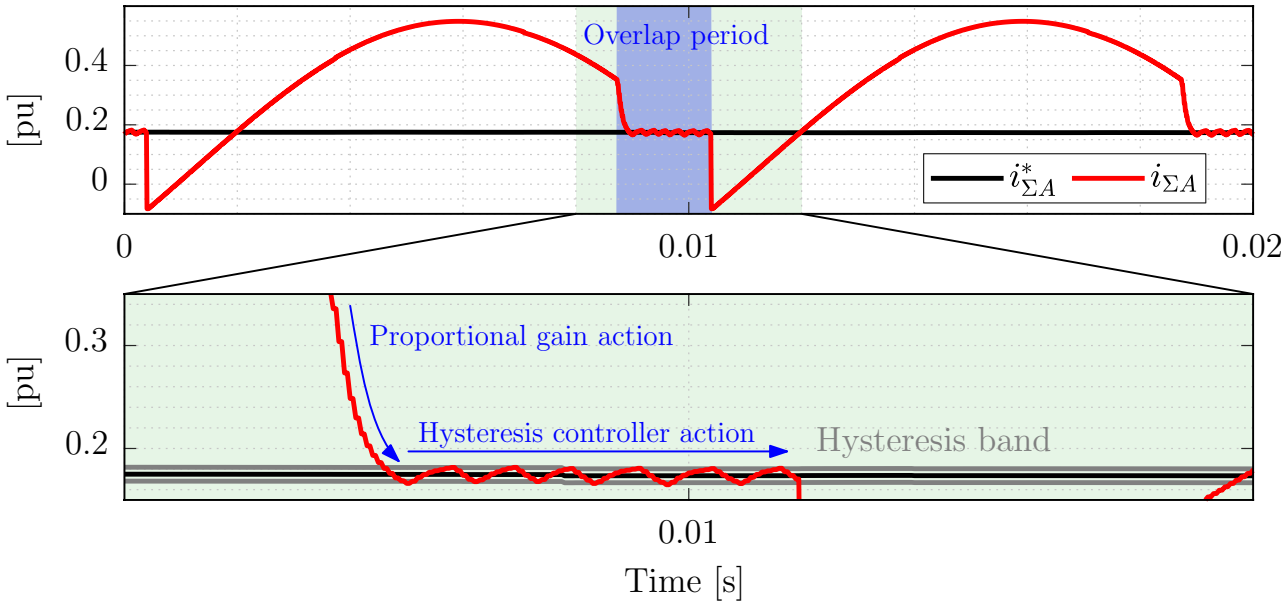

Figure A.4 – Validation of overlap current controllers of the SO-AAC

As visible on Figure A.4, a constant reference for the overlap current of the leg A has been

fixed. This reference is tracked during the overlap period framed in blue, its length has been set to 30 degrees (i.e. 1.6666 ms). A zoom is proposed on the green zone where the actions of the proportional gain and the hysteresis controller are highlighted. The proportional gain is responsible for the fast decreasing of the overlap current which is then maintained between hysteresis band (i.e. ± 10 A).

From this figure, it can be clearly highlighted that one of the shortcomings of the SO-AAC is the very fast dynamics needed for the overlap current control. This is especially true for lower values of overlap period.

A.2 Zero Current Switching (ZCS) of the DSs

The association of the arm inductors and the DSs prevent from hard switching the DS at turn-off. However, in most of the cases, when the DS is supposed to be turned off the current is not close to zero. It can be depicted by using the previous simulation result with a focus on one arm current and DS voltage:

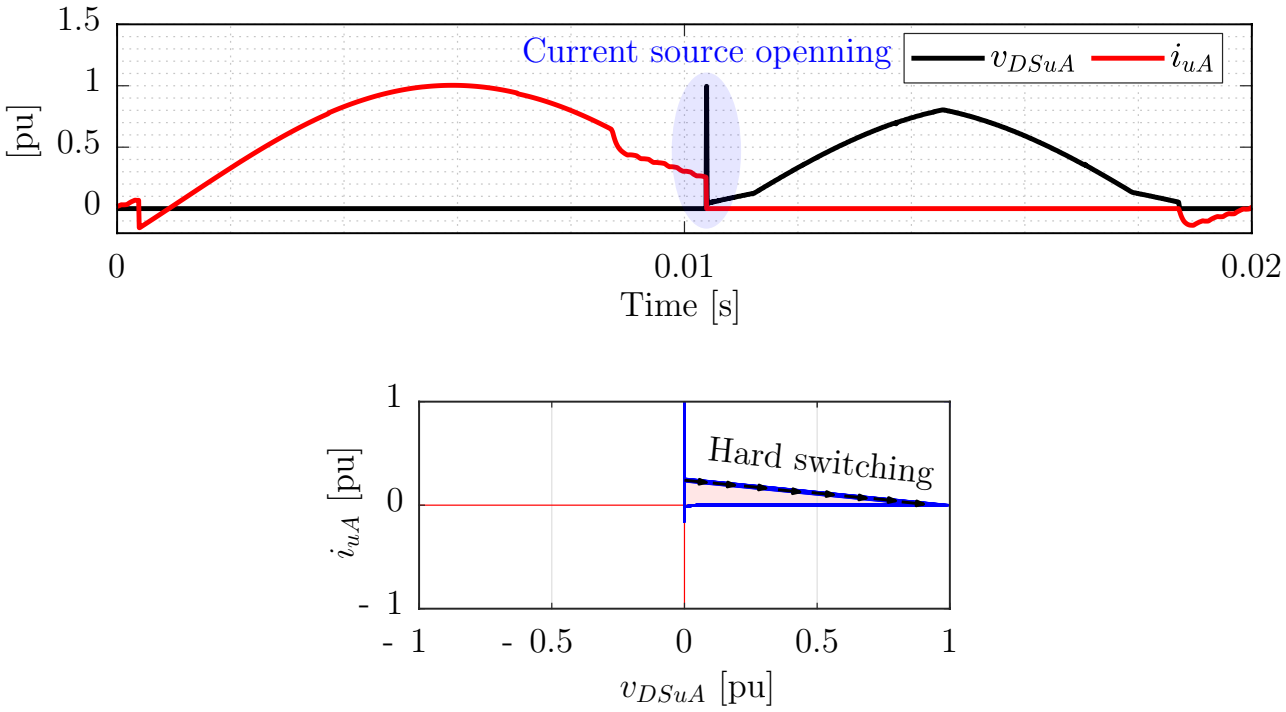

Figure A.5 – Illustration of the DS hard switching at turn off

The hard switching is highlighted on Figure A.5 by the area filled in blue resulting in a current source opening. Then, a voltage spike has to be supported by the DS. The second graph shows $i_{uA}(v_{DSuA})$ that represents the VI trajectory of the DS. The turn on is soft, but, the hard switching at turn off is highlighted by the excursion in the positive quadrant.

A.2.1 Soft switching technique

The considered method to open an SO-AAC arm consists in using the natural blocking of the diodes. It supposes that the arm current is flowing diodes and not transistors. The end of the conduction period of the arms happens at the end of one overlap period, during this

operating mode arm currents are expressed such as:

$$\begin{aligned} i_u &= \frac{i_g}{2} + i_\Sigma \\ i_l &= -\frac{i_g}{2} + i_\Sigma \end{aligned} \tag{A.15}$$

The general idea of the soft switching is to cancel the arm current. According to the above equation two choices are possible. The first one is to use i_g to oppose i_Σ while the second possibility is the opposite case. It chosen to keep AC currents harmonics free, then, the overlap current will be used to oppose i_g. If the upper arm is controlled to be zero:

$$i^*_{\Sigma_{ZCS}} = -\frac{i_g}{2} \tag{A.16}$$

where $i^*_{\Sigma_{ZCS}}$ is the overlap current reference dedicated to the ZCS of the DS. On the other hand, if the lower arm is controlled to zero

$$i^*_{\Sigma_{ZCS}} = \frac{i_g}{2} \tag{A.17}$$

By using this reference for the control of the overlap current, it is ensured that the arm current is close to zero. However, as it was mentioned earlier it is needed to make sure that diodes are conducting at the end of the overlap period. Then, a bias should be used to make sure that no zero crossing will occur.

$$i^*_{\Sigma_{ZCS}} = \pm\frac{i_g}{2} + \Delta i_{ZCS} \tag{A.18}$$

All the method that has been used for the soft switching of the DS relies on Δi_{ZCS}. Depending on the value of this bias, the arm current can be slightly positive or negative, both position will be used.

The method can be described in three main steps:

1. The arm current is brought to a negative value : $i^*_{\Sigma_{ZCS}} = \pm\frac{i_g}{2} - \Delta i_{ZCS} \rightarrow$ diodes enter in conduction mode.
2. The arm current is maintained negative. Transistors are turned-off without current flowing through them.
3. The arm current is brought zero in order to block diodes :$i^*_{\Sigma_{ZCS}} = \pm\frac{i_g}{2} + \Delta i_{ZCS} \rightarrow$ the bias is positive in order to saturate the control which in consequence maintained reverse-biased diodes (unable to restart conduction).

The bias is essentially calculated on the basis of the hysteresis band. In order to make sure that there is zero crossing, it is chosen to define Δi_{ZCS} equals to two times the hysteresis.

A.2.2 Validation through EMT simulation

The same simulation has been performed, but now, the strategy to softly open the DS has been implemented. Results are provided as it follows.

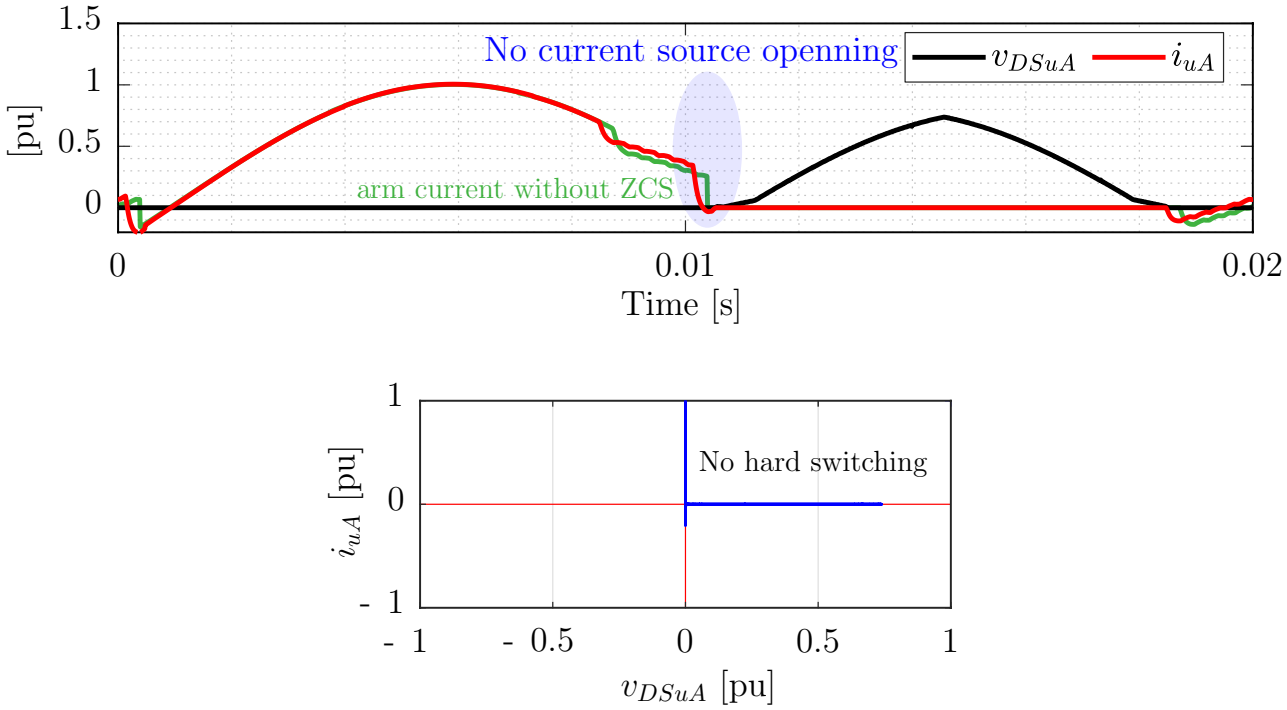

Figure A.6 – Illustration of the DS soft switching at turn off

The green curve is the arm current waveforms obtained in the previous simulation to highlight the difference between the red curve which is the arm current including ZCS strategy. As we can see, before the end of the conduction period, the arm current is brought near to zero, firstly negative and then zero to block diodes. As a result, there is no voltage spike due to current opening and the VI trajectory of the DS on the second almost perfectly overlap the XY axis meaning "lossless" commutations.

A.3 Energy Management in SO-AAC

In addition to the ZCS of the DS, the overlap period, and therefore the overlap current, is used to ensure the power balance inside the converter. These two tasks must be achieved within the overlap period which is organised as follows:

1. The energy management is executed first and for most of the overlap period
2. Several hundreds of microseconds (e.g. 300) before the end of the overlap period, the reference of i_{Σ} switch to ZCS mode. The energy returns into an uncontrolled state.

The energy management in the SO-AAC is not fundamentally different from the EO-AAC. The converter still require horizontal and vertical balancing controllers to operate. In fact, there is only one difference between the control structure derived in Chapter 3 and the one in this appendix. Indeed, in case of the EO-AAC both AC and DC powers are continuously regulated. In the SO-AAC case, there are moments where the DC current is uncontrolled enforcing to derived an average model of the total energy deviation.

According to Figure A.1, the total energy can be written as

$$\frac{dW_{tot}}{dt} = v_{muA}i_{uA} + v_{mlA}i_{lA} + v_{mlB}i_{lB} + v_{muC}i_{uC} \tag{A.19}$$

The average value of this equation is given by:

$$\frac{d\bar{W}_{tot}}{dt} = v_{dc} i_{\Sigma} \left(\frac{\theta_{ovl}}{\pi} \right) + P_{ac} \left(1 - \frac{4}{m\pi} \cos \left(\frac{\theta_{ovl}}{2} \right) \right) \tag{A.20}$$

which is the three phase form of the equations single-phase stored energy deviation derived in Chapter 3 to build the horizontal balancing controllers. Thus, the only difference between the SO-AAC and the EO-AAC lies in the compensation of the uncontrollable part of the DC power (highlighted in red) which only exist for SO-AAC.

All others energy control loops, horizontal and vertical balancing controllers remain the same as in Chapter 3. It results in the following control structure.

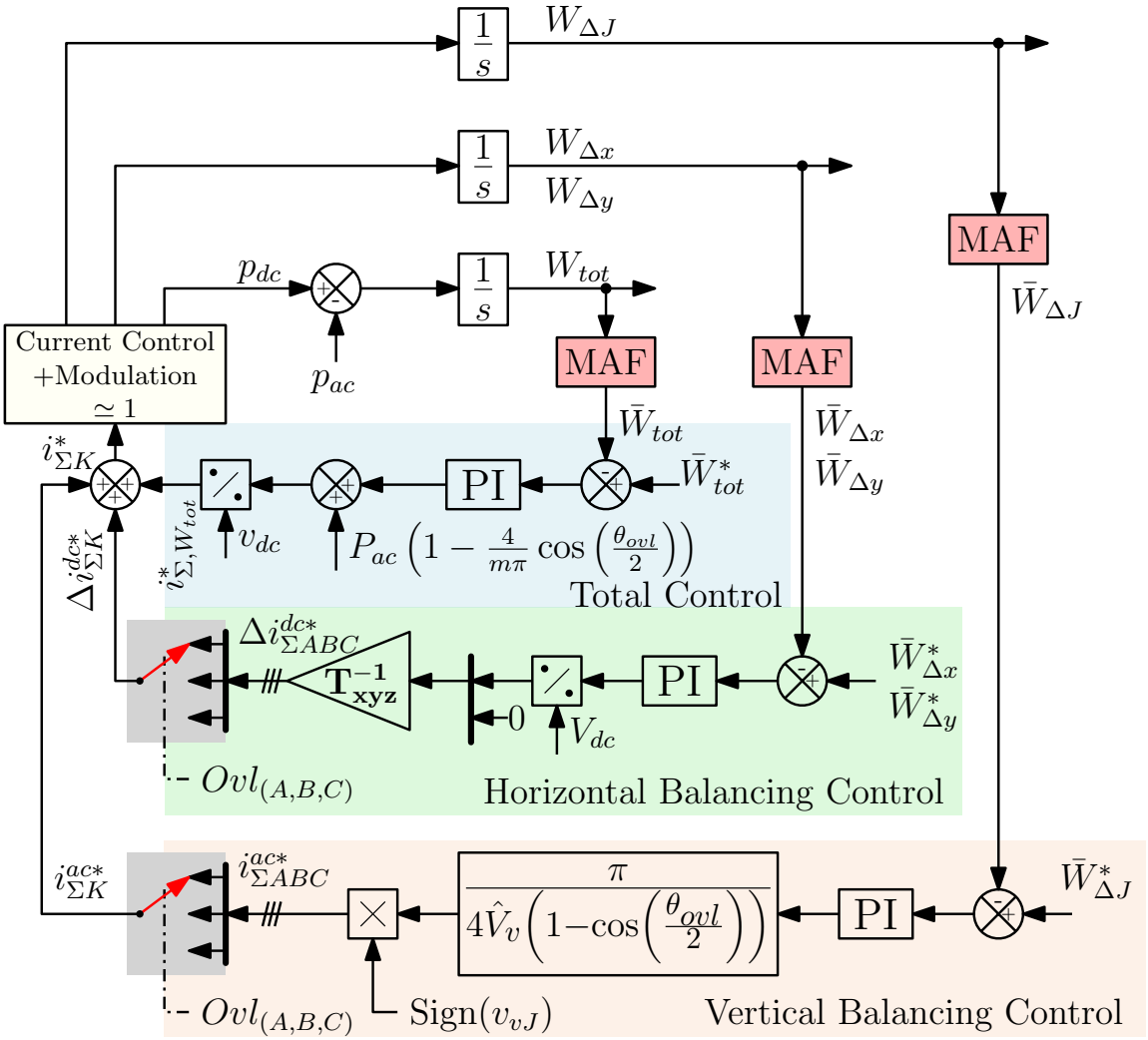

Figure A.7 – Energy control structure of the SO-AAC

Similarly to the EO-AAC, there is one leg that support the total energy deviation and a small adjustment is then applied to rebalance energy between legs. However, there is one function less to be achieved by this leg : the active filtering of the DC current. Hence, the constraint on the DC side control is relaxed.

The control structure is equivalent to the one detailed in Chapter 3. Considering the simulation done before, the following results are obtained. It is worth mentioning that the DC quantities display on the following are measured before the filtering of the DC current. For

this reason the current and the power that are presented are named i_m and p_{DCm} since these quantities are modulated ones.

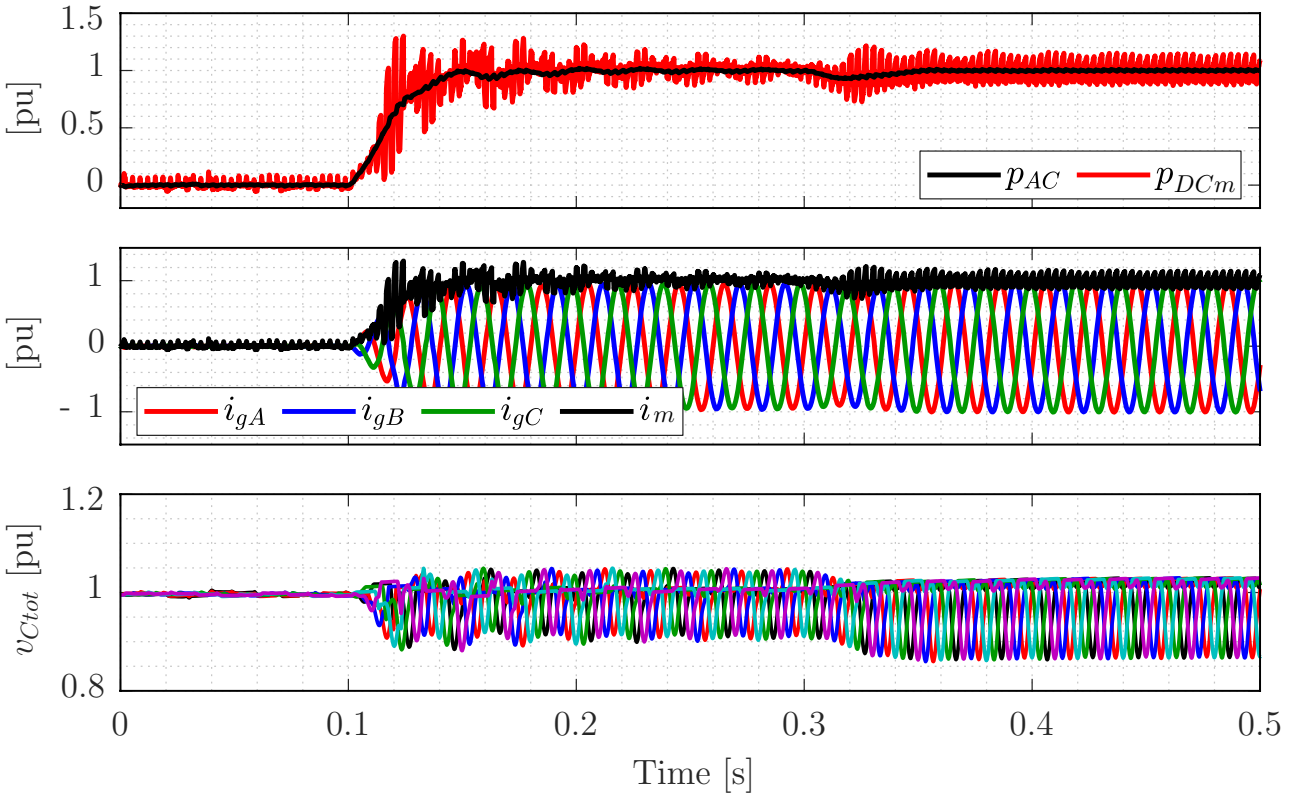

Figure A.8 – Validation of the Energy control structure of the SO-AAC

Figure A.8 shows the response of the SO-AAC to the AC side events of Figure A.3 (i.e. change on active and reactive power references). As visible on this figure, the DC side power (before the filter) is highly disturbed during transients due to high balancing currents. Indeed, the shorter is the overlap period the higher is the magnitude of the balancing current increasing the constraint on the overlap period which requires extremely fast dynamics to met with the need for energy balancing and ZCS of the DS.

However, we see that the converter is able to deal with these events quite easily. The energy remains stable and well distributed inside each stack.

A.4 Conclusion on SO-AAC

In this appendix, a quick overview of the SO-AAC operations has been proposed. In overall, the operations of that topology, compared to the EO-AAC, appears as being more complex for one main reason: the overlap current control.

Indeed, through the different simulation carried out, it has been highlighted the very dynamics required to control this currents and the constraint that is put on it. To maximize the energy management time, the duration of the ZCS must be reduce increasing even more the constraint on the current. Of course, other techniques of control exist, like blocked state SMs proposed by M.M.C. Merlin that do not rely on a explicit current control. However, this point may be very problematic for practical implementation.

Appendix B

Power Derivations

B.1 MMC with sinusoidal modulation

$$\begin{aligned} v_{mu} &= \frac{V_{dc}}{2} - \hat{V}_g \sin(\theta_g) \\ i_u &= \frac{I_{dc}}{3} + \frac{\hat{I}_g}{2} \sin(\theta_g + \varphi) \end{aligned} \tag{B.1}$$

From these descriptions of arm quantities, the power that flows through the MMC capacitors (p_{Ctot}) can be derived.

$$\begin{aligned} p_{Ctot} &= \left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t)\right)\left(\frac{I_{dc}}{3} + \frac{\hat{I}_g}{2} \sin(\omega t + \varphi)\right) \\ &= \frac{V_{dc}\hat{I}_g}{2} \sin(\omega t + \varphi) - \hat{V}_g \hat{I}_g \sin(\omega t)\sin(\omega t + \varphi) + \frac{V_{dc} I_{dc}}{6} - \frac{\hat{V}_g I_{dc}}{3} \sin(\omega t) \end{aligned} \tag{B.2}$$

The above equations shows that stack powers are composed of a fundamental and a second order harmonic deriving from the combination between AC and DC quantities. This equation is poorly readable, it is therefore chosen to replace DC quantities by equivalence on the AC side using the modulation index (m) defined in Chapter 1.

$$p_{Ctot} = V_g I_g \left[\frac{1}{m} \sin(\omega t + \varphi) - \frac{1}{2}\left(\cos(\varphi) - \cos(2\omega t + \varphi)\right) + \frac{\sqrt{2}}{m} \frac{m\cos(\varphi)}{2\sqrt{2}} - \frac{\sqrt{2} m \cos(\varphi)}{2\sqrt{2}} \sin(\omega t)\right] \tag{B.3}$$

Finally, as all terms are now related to AC quantities, it is possible to simplify all these expressions by considering the three-phase apparent power S to get

$$p_{Ctot} = S\left[\frac{1}{3m} \sin(\theta_g + \varphi) + \frac{1}{6} \cos(2\theta_g + \varphi) - \frac{m}{6} \cos(\varphi)\sin(\theta_g)\right] \tag{B.4}$$

B.2 MMC with ZSVI

When considering the ZSVI in a steady-state analytic model, the expression (2.3) is not suitable. As presented above, this voltage follows a triangular waveform that may be approximated by its Fourier expansion given by (B.5).

$$
\begin{aligned}
v_{n0} &= k_{n0}\hat{V}_g \frac{4}{\pi^2} \sum_{k=0}^{\infty} \frac{(-1)^k}{(2k+1)^2} \sin\left((2k+1)3\omega t\right) \\
&= k_{n0}\hat{V}_g \frac{4}{\pi^2} \left(\sin(3\omega t) - \frac{1}{9}\sin(9\omega t) + ...\right)
\end{aligned}
\tag{B.5}
$$

In order to keep all equations as clear as possible, the following derivations which concern stack power in MMC with ZSVI, only the fundamental is considered (i.e the third harmonic).

$$
p_{Ctot} = \underbrace{\left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t)\right)\left(\frac{I_{dc}}{3} + \frac{\hat{I}_g}{2}\sin(\omega t + \varphi)\right)}_{\text{Eq. A.4}} \underbrace{-v_{N0}\left(\frac{I_{dc}}{3} + \frac{\hat{I}_g}{2}\sin(\omega t + \varphi)\right)}_{p_{Ctot0}} \tag{B.6}
$$

As it can be expected, (B.6) shows that all previous derivations are still valuable while the ZSVI only add a new contribution to the stack power. So, only this new contribution is derived and named p_{Ctot0} with the index $'0'$ is for the ZSVI. Focusing on the third harmonic gives:

$$
\begin{aligned}
p_{Ctot0} &= -k_{n0}\hat{V}_g \frac{4}{\pi^2}\sin(3\omega t)\left(\frac{mI_g\cos(\varphi)}{2\sqrt{2}} + \frac{\hat{I}_g}{2}\sin(\omega t + \varphi)\right) \\
&= S\left[-\frac{2k_{n0}m\cos(\varphi)}{3\pi^2}\sin(3\omega t) - \frac{2k_{n0}}{3\pi^2}\left(\cos(2\omega t - \varphi) - \cos(4\omega t + \varphi)\right)\right]
\end{aligned}
\tag{B.7}
$$

In MMC, k_{N0} is best at 0.5. Exceeding this value increases peak value of modulated voltage. It is finally obtained:

$$
\begin{aligned}
p_{Ctot} = S\Bigg[&\frac{1}{3m}\sin(\omega t + \varphi - \frac{m}{6}\cos(\varphi)\sin(\omega t) \\
&+ \frac{1}{6}\cos(2\omega t + \varphi) - \frac{1}{3\pi^2}\cos(2\omega t - \varphi) \\
&- \frac{m\cos(\varphi)}{3\pi^2}\sin(3\omega t) + \frac{1}{3\pi^2}\cos(4\omega t + \varphi)\Bigg]
\end{aligned}
\tag{B.8}
$$

As shown on (B.8) the ZSVI essentially interacts with the second order harmonic by decreasing it. Moreover, the third order harmonic allows decreasing peak values of modulated voltages which in consequence slightly reduces the integral of the power.

B.3 MMC with second order harmonic injection

In MMC, the energy deviation within a single leg can be expressed as

$$
\frac{dW_\Sigma}{dt} = 2V_{dc}i_\Sigma - V_g I_g\cos(\varphi) + V_g I_g\cos(2\omega t + \varphi) \tag{B.9}
$$

Assuming the energy controller providing a reference for i_Σ and this reference well tracked by the current control, then in steady-state it is obtained:

$$
\begin{aligned}
i_\Sigma &= \frac{V_g I_g\cos(\varphi) - V_g I_g\cos(2\omega t + \varphi)}{V_{dc}} \\
&= \frac{I_{dc}}{3} - \frac{mI_g}{2\sqrt{2}}\cos(2\omega t + \phi)
\end{aligned}
\tag{B.10}
$$

Then, the contribution of the second order current harmonic would lies in the following equation:

$$p_{Ctot} = \underbrace{\left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t)\right)\left(\frac{I_{dc}}{3} + \frac{\hat{I}_g}{2}\sin(\omega t + \varphi)\right)}_{\text{eq. A.4}} - \underbrace{\left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t)\right)\frac{mI_g}{2\sqrt{2}}\cos(2\omega t + \phi)}_{p_{Ctot2\omega}} \tag{B.11}$$

where the power related to the second order current harmonic injection $p_{Ctot2\omega}$ is

$$p_{Ctot2\omega} = -\frac{1}{6}\cos(2\omega t + \varphi) + \frac{m}{12}\sin(3\omega t + \varphi) - \frac{m}{12}\sin(\omega t + \varphi) \tag{B.12}$$

Combining (B.12) with (2.39) gives:

$$p_{Ctot} = S\left[\frac{4 - m^2}{12m}\sin(\omega t + \varphi) - \frac{m}{6}\cos(\varphi)\sin(\omega t) + \frac{m}{12}\sin(3\omega t + \varphi)\right] \tag{B.13}$$

The injection of the second order current harmonic suppress the second harmonic in SM capacitor voltage ripple as visible in (B.13). It is also notable that a small decreasing of the fundamental term harmonic is observed since the last term of (B.12) is negatively added to the first one of (2.39). The main interest of using second order current harmonic therefore lies in its independence from the modulation.

B.4 Short-Overlap AAC

As a recall, the conduction intervals of the arm are stated below

$$\begin{cases} \text{Interval 1: } \theta_g \in \left[-\frac{\theta_{ovl}}{2}; \frac{\theta_{ovl}}{2}\right] \text{ Overlap mode} \\ \text{Interval 2: } \theta_g \in \left[\frac{\theta_{ovl}}{2}; \pi - \frac{\theta_{ovl}}{2}\right] \text{ Non-overlap mode} \\ \text{Interval 3: } \theta_g \in \left[\pi - \frac{\theta_{ovl}}{2}; \pi + \frac{\theta_{ovl}}{2}\right] \text{ Overlap mode} \\ \text{Interval 4: } \theta_g \in \left[\pi + \frac{\theta_{ovl}}{2}; -\frac{\theta_{ovl}}{2}\right] \text{ Blocked mode} \end{cases}$$

The instantaneous power flowing through the SO-AAC depends on the interval described above. Thus, two variables are introduced:

- $p_{Ctot,novl}$ the power during the non-overlap mode
- $p_{Ctot,ovl}$ the power during the overlap mode

Still considering the assumptions that AC components are balanced and inductors neglected, then, the power flowing through the upper stack of the leg in **non-overlap mode** is

$$\begin{aligned} p_{Ctot,novl} &= \left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t)\right)\hat{I}_g \sin(\omega t + \varphi) \\ &= \frac{V_{dc}}{2}\hat{I}_g \sin(\omega t + \varphi) - V_g I_g \cos(\varphi) + V_g I_g \cos(2\omega t + \varphi) \\ &= S\left[\frac{2}{3m}\sin(\omega t + \varphi) - \frac{1}{3}\cos(\phi) + \frac{1}{3}\cos(2\omega t + \varphi)\right] \end{aligned} \tag{B.14}$$

The power in non-overlap mode given by (B.14) is similar to the MMC stack power excepted that a DC component is still remaining. This DC component is related to presence of the energy sweet-spot. To compensate the energy sweet-spot and ensure the power balance, the expression of i_Σ is:

$$i_\Sigma = \frac{mI_g\cos(\varphi)}{2\sqrt{2}}\left(-\frac{4}{m\pi}\cos\left(\frac{\theta_{ovl}}{2}\right)+1\right)\left(\frac{\pi}{\theta_{ovl}}\right) \tag{B.15}$$

From (B.15) and assuming an even distribution of the AC currents within the two arms gives the expression of the power that flows through the upper stack in **overlap mode**:

$$\begin{aligned} p_{Ctot,ovl} =& \frac{p_{Ctot,novl}}{2} + p_{Ctot,ovl,\Sigma} \\ & \underbrace{\left(\frac{V_{dc}}{2}-\hat{V}_g\sin(\omega t)\right)\frac{\hat{I}_g}{2}\sin(\omega t+\varphi)}_{\text{half of eq. A.14}} + \underbrace{\left(\frac{V_{dc}}{2}-\hat{V}_g\sin(\omega t)\right)i_\Sigma}_{p_{Ctot,ovl,\Sigma}} \end{aligned} \tag{B.16}$$

the power induced by the overlap current named $p_{Ctot,ovl,\Sigma}$ can be derived as it follows

$$\begin{aligned} p_{stack,ovl,\Sigma} &= \left(\frac{V_{dc}}{2}-\hat{V}_g\sin(\omega t)\right)\frac{mI_g\cos(\varphi)}{2\sqrt{2}}\left(-\frac{4}{m\pi}\cos\left(\frac{\theta_{ovl}}{2}\right)+1\right)\left(\frac{\pi}{\theta_{ovl}}\right) \\ &= S\left[\left(-\frac{4\cos(\varphi)}{m\theta_{ovl}}\cos\left(\frac{\theta_{ovl}}{2}\right)+\frac{\pi\cos(\varphi)}{\theta_{ovl}}\right)\left(\frac{1}{6}-\frac{m}{6}\sin(\omega t)\right)\right] \end{aligned} \tag{B.17}$$

It results the overall power expression in overlap mode

$$\begin{aligned} p_{Ctot,ovl} =& \frac{\text{Eq. (2.14}}{2} + \text{Eq. (A.17)} \\ =& S\left[\cos(\varphi)\left(-\frac{1}{6}+\frac{\pi}{6\theta_{ovl}}-\frac{4}{m\theta_{ovl}}\cos\left(\frac{\theta_{ovl}}{2}\right)\right)\right. \\ & +\frac{1}{3m}\sin(\omega t+\varphi)-\left(-\frac{4\cos(\varphi)}{m\theta_{ovl}}\cos\left(\frac{\theta_{ovl}}{2}\right)+\frac{\pi\cos(\varphi)}{\theta_{ovl}}\right)\frac{m}{6}\sin(\omega t) \\ & \left.+\frac{1}{6}\cos(2\omega t+\varphi)\right] \end{aligned} \tag{B.18}$$

This last equation presented above shows the evolution of power through stack in overlap mode. It is clear that the power model of AAC is much more difficult to analyse a priori. There are DC, ω and 2ω components which essentially depend on the m, φ and θ_{ovl}. However, there is common general tendency with the MMC which is the higher m, the lower will be the power harmonics.

B.5 Extended-Overlap AAC with sinusoidal modulation

In this case, the current i_Σ is more constant in steady-state. According to Figure 2.1

$$\begin{aligned} i_{dc} &= \frac{i_{uA}+i_{lA}}{2}+\frac{i_{lB}}{2}+\frac{i_{uC}}{2} \\ &= i_{\Sigma A}-\frac{\hat{I}_{gB}}{2}\sin\left(\omega t+\frac{2\pi}{3}+\varphi\right)+\frac{\hat{I}_{gC}}{2}\sin\left(\omega t-\frac{2\pi}{3}+\varphi\right) \end{aligned} \tag{B.19}$$

From (B.19) the expression of the overlap current in leg A, if the AC side currents are balanced, is derived

$$i_{\Sigma A} = I_g \left(\frac{3m\cos(\varphi)}{2\sqrt{2}} \pm \frac{\sqrt{3}}{\sqrt{2}} \cos(\omega t + \varphi) \right) \tag{B.20}$$

In a similar way to SO-AAC, the analysis is best achieved by considering distinctly the non-overlap and overlap mode. The non-overlap mode is basically the same as before, thus the power equation that governs this mode remains (B.14). Only the power expression in overlap mode changes. In (B.20) the use of $\pm$ is for the overlap periods found in Interval 1 and Interval 3. They are 180 degrees shifted involving in one case the second term is positive while in other one it is negative. Considering this expression of overlap current gives the expression of the power

$$p_{Ctot,ovl} = \underbrace{\left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t) \right) \frac{\hat{I}_g}{2} \sin(\omega t + \varphi)}_{\text{half of eq. A.14}} + \underbrace{\left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t) \right) i_\Sigma}_{p_{Ctot,ovl,dcf}} \tag{B.21}$$

In (B.21) only the part related to the overlap current needs to be derived as the contribution of the AC current is half of (B.14). The overlap current is defined in (2.46) and its contribution to the instantaneous power named $p_{Ctot,ovl,dcf}$ for DC filtering.

$$\begin{aligned} p_{Ctot,ovl,dcf} &= \left(\frac{V_{dc}}{2} - \hat{V}_g \sin(\omega t) \right) I_g \left(\frac{3m\cos(\varphi)}{2\sqrt{2}} \pm \frac{\sqrt{3}}{\sqrt{2}} \cos(\omega t + \varphi) \right) \\ &= S \left[\cos(\varphi) \left(\frac{1}{2} - \frac{m}{2} \sin(\omega t) \right) \pm \frac{1}{m\sqrt{3}} \cos(\omega t + \varphi) \pm \frac{1}{2\sqrt{3}} \left(\sin(2\omega t + \varphi) - \sin(\varphi) \right) \right] \end{aligned} \tag{B.22}$$

Then it is obtained

$$\begin{aligned} p_{Ctot,ovl} =& \frac{\text{Eq. (A.14)}}{2} + \text{Eq. (A.27)} \\ =& S \left[\frac{2}{6} \cos(\varphi) \pm \frac{1}{2\sqrt{3}} \sin(\varphi) \right. \\ &+ \frac{1}{3m} \sin(\omega t + \varphi) - \frac{m\cos(\varphi)}{2} \sin(\omega t) \pm \frac{1}{m\sqrt{3}} \cos(\omega t + \varphi) \\ &\left. + \frac{1}{6} \cos(2\omega t + \varphi) \pm \frac{1}{2\sqrt{3}} \sin(2\omega t + \varphi) \right] \end{aligned} \tag{B.23}$$

B.6 EO-AAC with ZSVI

$$p_{Ctot,novl} = \text{Eq. A.14} + p_{Ctot,novl,0} \tag{B.24}$$

where as for the MMC, the index '0' means the contribution of the ZSVI derived as

$$\begin{aligned} p_{Ctot,novl,0} &= -v_{n0} i_g \\ &= -k_{N0} \hat{V}_g \frac{4}{\pi^2} \sin(3\omega t) \hat{I}_g \sin(\omega t + \varphi) \\ &= S \left[-\frac{2k_{N0}}{3\pi^2} \left(\cos(2\omega t - \varphi) - \cos(4\omega t + \varphi) \right) \right] \end{aligned} \tag{B.25}$$

Introducing (B.25) in (B.14) gives

$$\begin{aligned} p_{Ctot,novl} =& S\left[\frac{2}{3m}\sin(\omega t+\varphi)-\frac{1}{3}\cos(\phi)\right. \\ &\left.+\frac{1}{3}\cos(2\omega t+\varphi)+\frac{2|k_{N0}|}{3\pi^2}\cos(2\omega t-\varphi)-\frac{2|k_{N0}|}{3\pi^2}\cos(4\omega t+\varphi)\right] \end{aligned} \tag{B.26}$$

The equation (B.26) shows that, the second order harmonic is increased due to the interaction between the fundamental of v_{N0} an the grid current. Then, **in overlap mode the power is**

$$p_{Ctot,ovl} = \frac{\text{Eq. A.30}}{2} + \text{Eq. A.26} + p_{Ctot,ovl,dcf,0} \tag{B.27}$$

Actually, as described in the above equation, only the interaction between the overlap current with active filtering and the ZSVI must be derived as it follows.

$$\begin{aligned} p_{Ctot,ovl,dcf,0} &= -k_{N0}\hat{V}_g\frac{4}{\pi^2}\sin(3\omega t)I_g\left(\frac{3m\cos(\varphi)}{2\sqrt{2}}\pm\frac{\sqrt{3}}{\sqrt{2}}\cos(\omega t+\varphi)\right) \\ &= S\left[-\frac{6mk_{N0}\cos(\varphi)}{3\pi^2}\sin(3\omega t)\pm\frac{2\sqrt{3}k_{N0}}{3\pi^2}\left(\sin(2\omega t-\varphi)+\sin(4\omega t+\varphi)\right)\right] \end{aligned} \tag{B.28}$$

Contribution au Dimensionnement et à la Commande de Convertisseur Extended Overlap Alternate Arm Converter (EO-AAC)

Ces travaux de thèse portent essentiellement sur la modélisation, le dimensionnement et la commande d'un convertisseur de type hybride-modulaire nommé : Extended Overlap-Alternate Arm Converter (EO-AAC). Le premier objectif de cette thèse consiste dans la mise en place d'une démarche systématique dans l'analyse du fonctionnement de ce convertisseur pour en comprendre les principes mais également pour permettre un mise en avant claire des degrés de liberté exploitable par la suite. Depuis l'analyse du fonctionnement du convertisseur, un modèle statique est développé dans le but de réaliser une étude de dimensionnement. Les convertisseurs modulaires sont généralement composés d'un grand nombre de composants semi conducteurs et passifs a dimensionnés tels que les Sous-Modules, les Director Switches et les condensateurs de Sous-Modules. Ensuite, les modèles du dynamique du convertisseur sont calculés afin de contrôler chaque grandeur d'états. Il est mis en évidence l'absolue nécessité d'une commande en boucle fermée pour l'énergie stockée en interne du convertisseur donnant lieu l'utilisation de trois principales fonctions: le contrôle totale et les équilibrages horizontaux et verticaux. Grâce à la commande développée, un modèle réduit du EO-AAC s'affranchissant de sont aspect séquentiel est mit évidence notamment pour des études réseaux. Enfin, la connexion au réseau électrique qu'il soit AC ou DC est étudiée afin de mettre en avant les capacités mais également les faiblesses du cette structure.

Mots clés

«Réseaux à courant continu multi-terminaux», «Convertisseur modulaire multiniveaux», «Électronique de Puissance», «Convertisseur hybride-modulaire».

Contribution to the Design and Control of the Extended Overlap-Alternate Arm Converter

These thesis works mainly focus on the modeling, sizing and control of a hybrid-modular converter named: Extended Overlap-Alternate Arm Converter (EO-AAC). The first objective of this thesis consists in the implementation of a systematic approach in the analysis of the operation of this converter to understand the principles but also to allow a clear highlighting of the exploitable degrees of freedom thereafter. From the analysis of the operation of the converter, a steady-state model is developed in order to carry out a sizing study. Modular converters are generally made up of a large number of semiconductor and passive components such as Submodules, Director Switches, and Submodule capacitors to be dimensioned. Then, dynamic models of the converter are derived in order to control each state variables. It highlights the absolute need of closed loop control for the energy stored internally of the converter, giving rise to the use of three main functions: total control and horizontal and vertical balancing. Thanks to the control developed, a reduced model of the EO-AAC which does not have its sequential aspect is highlighted, in particular for power system studies. Finally, the connection to the grid, whether AC or DC, is studied in order to highlight the capacities but also the weaknesses of this structure.

Keywords

«HVDC transmission», «Modular multilevel converter», «Alternate Arm Converter», «Power Electronics», «Interoperability in MTDC grids».