



Analysis, modelling and reduction of the simultaneous switching noise generated by the high data rate IOs of a STM32 microcontroller

Mélanie Moign

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$$\rho \left(\frac{\partial v}{\partial t} + v \cdot \nabla v \right) = -\nabla p + \nabla \cdot T + f$$

$$e^{i\pi} + 1 = 0$$

THÈSE DE DOCTORAT

Analyse, modélisation et réduction du bruit
de commutation simultanée généré par les
interfaces d'Entrées/Sorties haute vitesse
dans les microcontrôleurs STM32

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du grade de docteur en Sciences**
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Analysis, modelling, and reduction of the simultaneous switching noise generated by the high data rate IOs of a STM32 microcontroller

This thesis has been accomplished in the frame of a “Cifre convention” between the laboratory Polytech’lab and the company STMicroelectronics and is centered on the domain of electromagnetic compatibility (EMC). The rapid and constant evolution of microcontrollers (MCU) and the increase of their performance has led to an important degradation of their behavior regarding the EMC. For example, the Simultaneous Switching Noise (SSN) is a subject known since the 80s but that became a source of failure through the years because of, among other things, the increase of communication signals frequency. This thesis is focused on the study of this SSN effect in the constrained environment of the STM32. A modeling methodology of a complete system defined by the die, the package, and the Printed Circuit Board (PCB) has been validated thru a vast campaign of comparison between simulations and measurements. These simulations allow, on one hand, to investigate the root cause of a product failure and on the other hand, to observe the SSN effect to points that are physically unreachable in measurement.

This work allowed the definition of the main design rules to be applied to the chip, the package, and the PCB in order to improve the MCU robustness regarding the SSN effect. To conclude, this thesis presents a new development approach for designers with the use of a predictive model. This predictive model allows the anticipation of the future MCU behavior regarding EMC problematic and this, directly at the design stage. Considering the very fast evolution of the CMOS technology and therefore of the MCU, being able to anticipate these issues is a real advantage in the objective of being more competitive on the market with more robust and reliable products.

Keys words: Electromagnetic Compatibility (EMC), Input/Output interface (IO), Simultaneous Switching Noise (SSN), Auto-susceptibility, Power distribution network (PDN), ICEM model, microcontroller modeling

Analyse, modélisation et réduction du bruit de commutation simultanée généré par les interfaces d’Entrées/Sorties haute vitesse en technologie CMOS dans les microcontrôleurs STM32

Cette thèse réalisée dans le cadre d’une convention Cifre entre le laboratoire Polytech’Lab et la société STMicroelectronics, porte sur le domaine de la compatibilité électromagnétique (CEM). L’évolution continue et très rapide des microcontrôleurs (MCU) en vue de l’accroissement de leurs performances a malheureusement entraîné une dégradation importante de leur comportement vis-à-vis de la CEM. Par exemple, le bruit de commutation simultanée (BCS), connu depuis les années 80, est devenu une source de défaillance du MCU en raison notamment de l’augmentation des fréquences des signaux de communication. Cette thèse s’inscrit dans l’étude de ce phénomène au sein de l’environnement très contraint du microcontrôleur STM32. Une méthode de modélisation d’un système complet puce/boîtier/circuit imprimé a été élaborée et validée par une importante campagne de comparaison entre mesures et simulations. Ces dernières permettent de pouvoir, d’étudier les principales défaillances d’un produit, et d’autre part observer l’effet du BCS à des endroits physiquement inatteignables en mesure.

Ce travail a permis de définir les principales règles de conception à appliquer sur la puce, le boîtier et le circuit imprimé pour améliorer la robustesse du MCU au bruit BCS. Pour conclure, nous avons présenté une nouvelle approche de travail avec le développement d’un modèle prédictif permettant l’anticipation du comportement d’un futur MCU face aux problèmes de CEM, et cela, dès la phase de conception. Compte tenu de l’évolution très rapide de la technologie CMOS et des MCU, réussir à anticiper ces problèmes est un réel avantage pour pouvoir rester compétitif sur le marché avec des produits plus robustes et fiables.

Mots clés : Compatibilité électromagnétique, Auto-susceptibilité, Périphérique d’entrée/sortie, Bruit à commutation simultanée, Réseau de distribution d’alimentation, Model ICEM, modélisation

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Acronyms List

ADC	ANALOG TO DIGITAL CONVERTER
BGA	BALL GRID ARRAY
BJT	BIPLOR JUNCTION TRANSISTOR
BSIM	BERKELEY SHORT-CHANNEL IGFET MODEL
CMOS	COMPLEMENTARY METAL OXIDE SEMICONDUCTOR
CPU	CENTRAL PROCESS UNIT
CSP	CHIP SCALE PACKAGE
DAC	DIGITAL TO ANALOG CONVERTER
DDR	DOUBLE DATA RATE
DIP	DUAL IN LINE PACKAGE
DUT	DEVICE UNDER TEST
EM	ELECTROMAGNETIC
EMC	ELECTROMAGNETIC COMPATIBILITY
EME	ELECTROMAGNETIC EMISSION
EMI	ELECTROMAGNETIC INTERFERENCE
EMMC	EMBEDDED MULTI-MEDIA CONTROLLER
EMS	ELECTROMAGNETIC SUSCEPTIBILITY
ESD	ELECTROSTATIC DISCHARGE
ET	EXTERNAL TERMINAL
FEM	FINITE ELEMENTS METHOD
FET	FIELD EFFECT TRANSISTOR
HSPI	HEXASPI
IA	INTERNAL ACTIVITY
IBC	INTER-BLOCK COUPLING
IBIS	INPUT/OUTPUT BUFFER INFORMATION SPECIFICATION
IC	INTEGRATED CIRCUIT
ICEM	INTEGRATED CIRCUIT EMISSION MODEL
ICEM-CE	INTEGRATED CIRCUIT EMISSION MODEL – CONDUCTED EMISSION
IEC	INTERNATIONAL ELECTROTECHNICAL COMMITTEE
IMIC	INPUT/OUTPUT MODEL FOR INTEGRATED CIRCUIT

IO	INPUT/OUTPUT INTERFACE
IP	INTELLECTUAL PROPERTIES
IT	INTERNAL TERMINAL
JEITA	JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION
LCD	LIQUID CRYSTAL DISPLAY
LECCS	LINEAR EQUIVALENT CIRCUIT AND A CURRENT SOURCE MODEL
MCU	MICROCONTROLLER
MOM	METHOD OF MOMENTS
MOSFET	METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR
MPU	MICROPROCESSOR
NVM	NON-VOLATILE MEMORY
P&G	POWER AND GROUND
PCB	PRINTED CIRCUIT BOARD
PDK	PROCESS DESIGN KIT
PDN	POWER DISTRIBUTION NETWORK
PI	POWER INTEGRITY
PVT	PROCESS, VOLTAGE, TEMPERATURE
QFP	QUAD FLAT PACKAGE
RGB	RED, GREEN, BLUE
SI	SIGNAL INTEGRITY
SIP	SYSTEM IN PACKAGE
SOC	SYSTEM ON CHIP
SOP	SMALL OUTLINE PACKAGE
SSN	SIMULTANEOUS SWITCHING NOISE
TFT-LCD	THIN FILM TRANSISTOR LIQUID CRYSTAL DISPLAY
TL	TRANSMISSION LINE
VTC	VOLTAGE TRANSFER CHARACTERISTIC

General Introduction

Over the last few decades, the electronics industry has undergone a major evolution, particularly in the field of embedded systems. Designers have thus developed circuits with high integration density that allow multiple functionalities to coexist, while minimizing production costs. However, this increase of electrical performance has a negative repercussion on its reliability and in particular for its electromagnetic compatibility (EMC). EMC problems remain today one of the main causes of re-design of Integrated Circuits (ICs) [1]. Due to the lack of possibilities for internal measurement and reliable prediction, the IC design is frequently modified after the EMC qualification phases because their operation is not guaranteed in several conditions. In order to avoid additional production costs, designers have recently been trying to study and anticipate this problem.

Microcontrollers (MCUs) are considered as versatile IC used in many different applications of embedded system. Due to this strong presence of MCUs in everyday connected objects, the market has become ultra-competitive, resulting in a frantic race for performance. Thus, it becomes essential for a company to ensure MCU robustness and reliability especially in terms of EMC issues. It is in this framework that this research was carried out within the IO team (Input/Output interface) of the STMicroelectronics microcontroller division, one of the world leaders in the MCU market and in collaboration with Polytech'lab, a microelectronic laboratory attached to the University Côte d'Azur. EMC problems have already been studied in this team. The emission aspect (EMI) was studied by J.P Leca [2] who defended his thesis in 2012 and susceptibility aspect (EMS) against external aggressions was studied by Y. Bacher 2017 and L. Quazzo in 2022 [3].

This thesis is focused on another type of EMC problem, the susceptibility of the chip face to an internal aggression. Due to the complex evolution of MCU, they are more and more

subject to these new types of disturbances commonly named auto-susceptibility. It is a merging of the two previous subjects since the MCU degrades its performance because of an internal noise emission. One of this phenomena is the Simultaneous Switching Noise (SSN), which is a topic that becomes more problematic through the years because MCU evolution leads to a lowering of susceptibility thresholds and to an increase of the internal emission level.

In the literature, there is a large number of publications about these SSN problems with the first one dated from the mid-90s and are mainly interested in the mechanism of generation of this noise with some preliminary design solutions. Later on, researchers focused more on studying the impact of SSN on some functional blocks in order to propose some solutions to reduce these disturbances at chip or package level. However, although they are numerous and referential to establish state of the art, these works are not sufficient to solve this problem given the market competition where the MCU must be cheap, small and with the best performance possible, leading to several constraints for proposed solutions. In view of all of this, it has therefore become essential for all designers to control the EMC product by developing innovative methods to measure, analyze, understand, and predict the electromagnetic performance of the MCU. For that purpose, this manuscript developed the research carried out on the SSN problematic.

The first chapter details all necessary knowledge to properly understand this SSN effect. For that, a summary is given of the state of the art to explain the origin of SSN. Next, MCU produced by STMicroelectronics are introduced and all linked elements to properly understand the SSN with some explanations about package and EMC at die level.

The second chapter is dedicated to the development of a modeling method for a complete system defined by a chip with its package and a Printed Circuit Board (PCB). This modeling method is based on the ICEM standard. Then, we will explain a validation process developed through comparisons between measurements and simulations on a 1st DUT. This step is essential to ensure that the simulations reflect the physical MCU behavior in order to study the SSN.

The third chapter is divided into two parts. The first part presents a complete modeling of a manufactured MCU based on the methodologies developed in chapter 2. This product study allows observation of the in-die noise and understanding of which parameters are influencing the SSN. Thanks to this, we will provide first design rules for die/package/PCB in order to improve the product robustness against SSN effects. This study also allowed to fix a failure on the product detected during the qualification phase. The second part presents the development

of a predictive model used to anticipate the MCU behavior for a specific high-data rate communication. The implementation of modeling methods that allows the prediction of the susceptibility of an internal block is an effective approach to analyze the behavior of an IC with respect to a disturbance. Nevertheless, these methods require a real expertise because there is no modeling and/or simulation procedure integrated in Computer Aided Design tools to understand the effect induced by electromagnetic disturbances through the IC.

Finally, this manuscript will be concluded with a summary of the work carried out in this study and some perspectives are presented.

Chapter 1. Background knowledge to understand the SSN effect

1. Introduction

Nowadays, Integrated Circuits (IC) play an important role in modern society, being used in most electronic appliances. Any electronic component created as one flat and small piece of semiconductor technology could be considered as an IC. This is the case for microcontrollers (MCU), microprocessors (MPU), several types of memories or sensors, etc. The development of IC is mainly based on the CMOS technology (Complementary Metal Oxide Semiconductor) and MOS transistors continue to follow Moore's Law: their size is divided by two every 18 months. This rapid and constant evolution of technology and MCU performance has led to an important degradation of MCU behavior in terms of Electromagnetic Compatibility (EMC) and it must be considered in order to stay competitive on the market. In this context, we propose to study an EMC problematic defined by the Simultaneous Switching Noise (SSN) generated by high-speed data rate Input/Output interfaces (IOs).

This chapter is dedicated to the definition of the thesis context with a first section that introduces 32-bits STM32 microcontroller defined as the device under test (DUT). Then, the second section details the semiconductor technology used for MCU development with a reminder of the MOS transistor origin and of its basic behavior in strong inversion. A third section briefly details Electromagnetic Compatibility (EMC) at MCU level. Finally, a fourth section details the SSN effect based on all knowledge acquired through this chapter.

2. Microcontroller (MCU)

2.1. MCU overview

MCUs are used in a lot of embedded systems such as smartphones, smart watches, earphones but also in other domain such as automotive, medical, aeronautic, ... An MCU is

defined as a tiny System on Chip (SoC) composed of different blocks. Figure 1-1 schematizes this IC which incorporates:

- A Central Process Unit (CPU) or processor defined as the MCU core. The CPU could be seen as the “device brain”.
- Several analog peripherals like ADC (Analog to Digital Converter) and DAC (Digital to Analog converter) which allows the communication between analog devices and the processor. Analog peripherals also include among other functionalities the power management of the MCU.
- Different types of memories as Flash, RAM or ROM used by the processor to store data and program instructions.
- Inputs/Outputs peripherals (IOs) that can be defined as an interface between the processor and the “outside world”. Figure 1-1 depicts the IOs distribution all around the MCU, creating a ring of pads commonly named “Pading”.

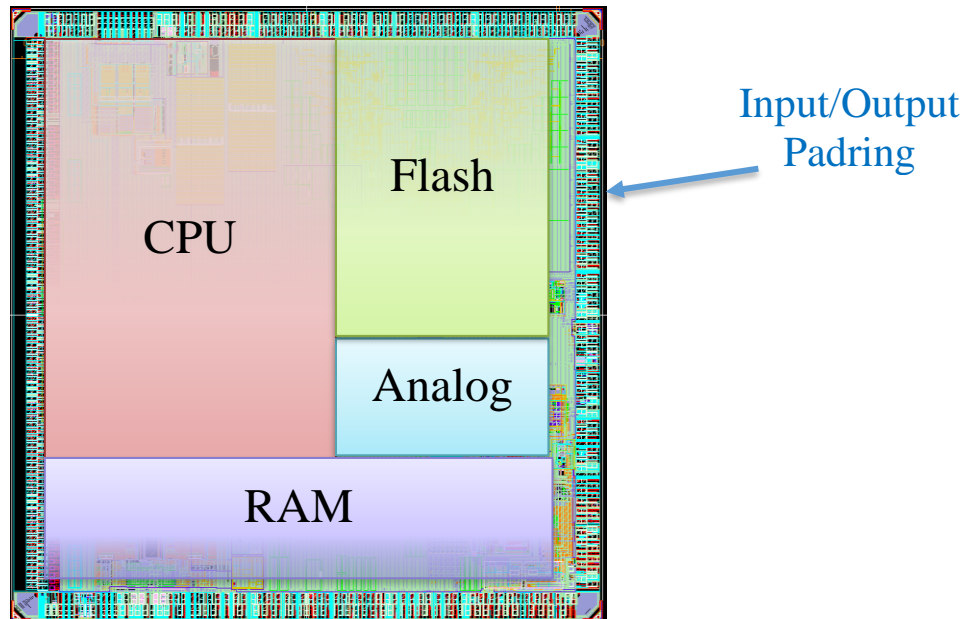


Figure 1-1: Schematic diagram of an MCU

In the next section the STM32 family, which are 32-bits microcontrollers manufactured by the STMicroelectronics company, is presented as the Device Under Test (DUT). In order to help the understanding of this thesis problematic, particular attention is given to the pading definition and to the MCU’s package because they are important contributors to the SSN effect. Finally, the origin of SSN is explained thanks to the definition of the MOS transistor.

2.2. STMicroelectronics microcontroller family

The STMicroelectronics company produces different MCUs and in particular the STM32. In order to satisfy all market needs, several types of MCU are produced. Each of them offers different functionalities regarding the size of the flash, the CPU frequency, the supply value for core and IOs, etc... Figure 1-2 depicts the “STMicroelectronics family” with all different manufactured products which are regrouped depending on their main functionalities and their purpose. A short definition of each of them is given below:

- A high-performance MCU includes a Non-Volatile Memory (NVM) in order to have a high performance for code execution and data processing.
- A mainstream MCU answers to the basic needs of the market where time and costs are essential.
- An ultra-low power MCU is a trade-off between cost, performance and power efficiency.
- A wireless MCU is able to run LoRaWAN protocol and, thanks to its functionalities will be favored by an RF designer.
- An automotive MCU will answer to many automotive applications and will also meet automotive constraints such as a temperature junction up to 165°C [4].

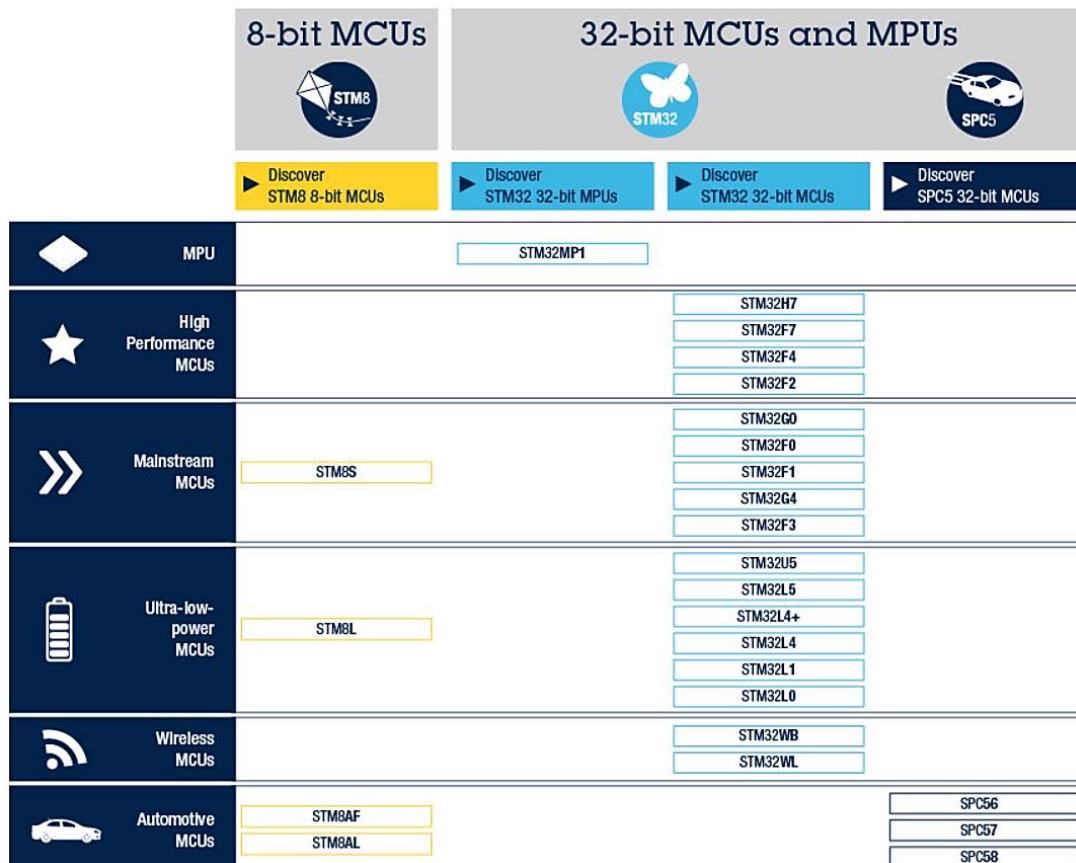


Figure 1-2: STM32 Family

2.2.1. Input/Output interfaces (IOs)

IOs are used to make the link between the MCU's core and its external environment. In other words, each time a communication is settled between the MCU and an external component, this communication is done through IOs by using a dedicated communication protocol. For example, if the MCU needs to communicate with an SD Card reader, this will be done with the EMMC (Embedded Multi-Media Controller) communication protocol through IOs interface. Nowadays, to remain competitive on the market an MCU needs to handle many of these protocols like USB type C, the SDMMC, the xSPI – where x is the number of bits transferred from the DualSPI to HexaSPI-, the I2C/I3C, etc. Each of these protocols has its own particularities and specifications as the operating frequency, the number of switching IOs, etc. Moreover, they are also generally defined by standards to ensure homogeneity between all manufacturers. It would be too long to provide more details regarding these protocols because, there are many different possibilities for the power supplies values, the data rate frequency, etc. Nevertheless, we will define the HexaSPI, in the last chapter because it was used in the frame of research activities conducted for a future STM32.

Regarding the IO design, one real structure is displayed in Figure 1-3. Such picture might not be easy to understand at first sight but it illustrates the complexity of current IOs. This complexity comes from all functionalities proposed by an IO like analog switches, different frequencies of work, Schmitt trigger to decrease noise perturbation, or the signal transmission for different power supplies value -for example, a 5V signal as input is transmitted to the core in a 1.2V signal-. This Figure 1-3 also shows the IO's pad used to establish the IO's connection to the outside.

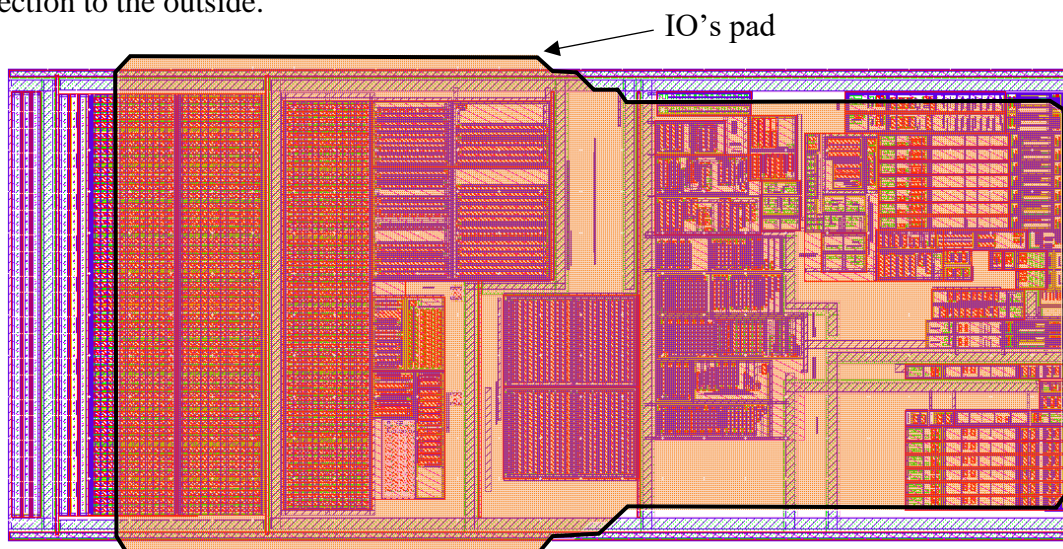


Figure 1-3: Example of IO's layout

2.3. MCU Packages overview

An MCU is defined by the die embedded in a package. The package is used to protect the die from its external environment but also to preserve its electrical characteristics. Of course, the package is used to facilitate the connection between the die and the Printed Circuit Board (PCB). For example, the package will establish the connection from the IO's pad to a track of the PCB and also the connections for all power supplies. Through the years, the packages evolved from a basic protection enclosure to a key element of the MCU performance. The science of integrated circuit packaging progressed radically providing more IOs connections, a better power dissipation, more resistance to temperature and humidity and even a package that embedded SiP (System in Package) bypass capacitor to optimize noise decoupling. Nowadays, there are different types of packages used for MCUs, the physical characteristics of the three most used packages are detailed below:

- QFP (Quad Flat Package): From a physical point of view, it is composed of leadframes and bonding. The bonding is a gold or an aluminum wire that creates the connection from a die's pad to the leadframe. Then, the leadframe goes from the bonding to the outside of the package and will be soldered on the PCB. The size of this package is mainly constrained by the die's cavity in the center of the package. Figure 1-4 illustrates a QFP package with the die cavity area, bonding, and lead frame.

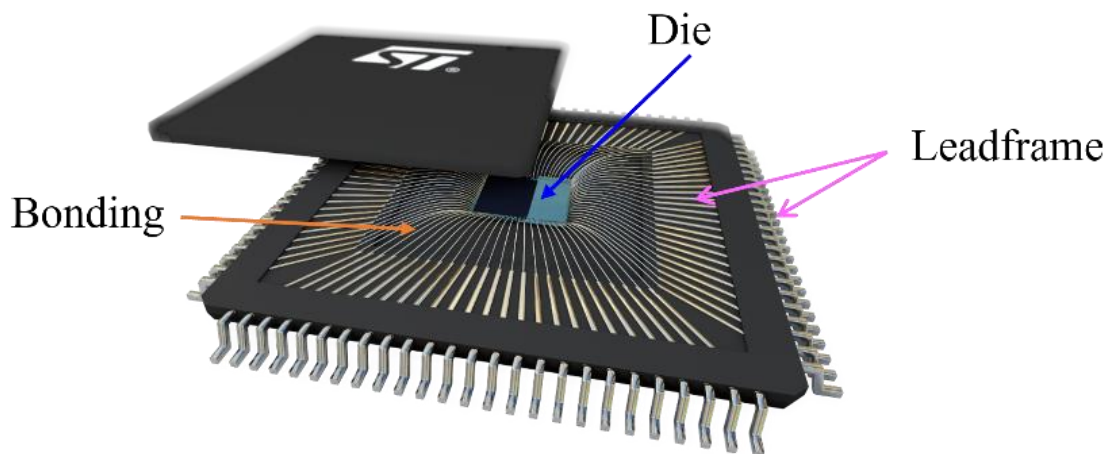


Figure 1-4: QFP package illustration

- BGA (Ball grid array): This package is based on the same principle as QFP, the only difference is regarding external leadframes, replaced by balls for this package. Figure 1-5 shows an example of a BGA layout where only a few connections appear. IOs pads are represented in orange, then bonding in blue, leadframe in pink, and balls in green.

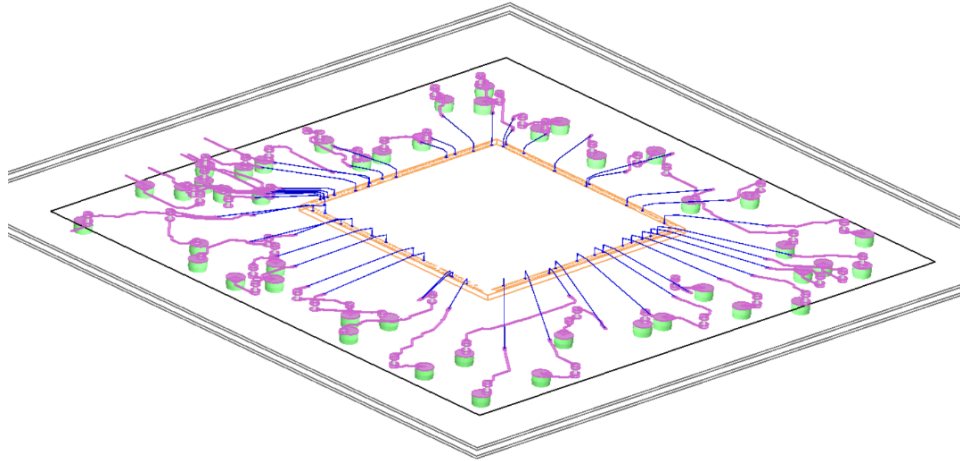


Figure 1-5: BGA layout

- CSP (Chip Scale Package): This is one of the new packages, where optimization is the corner stone of its design. For this one, there is no bonding but only “fan-in” routing. The “fan-in” routing describes the development of the connection from the padding to the package center. Reversely, the “fan-out” will be the connection development from the padding to the outside in the principle of QFP or BGA. Thanks to this fan-in routing, the size of a CSP package is limited to the die size as illustrated in Figure 1-6. Then, its external connections are done via balls, in the same way as with the BGA.

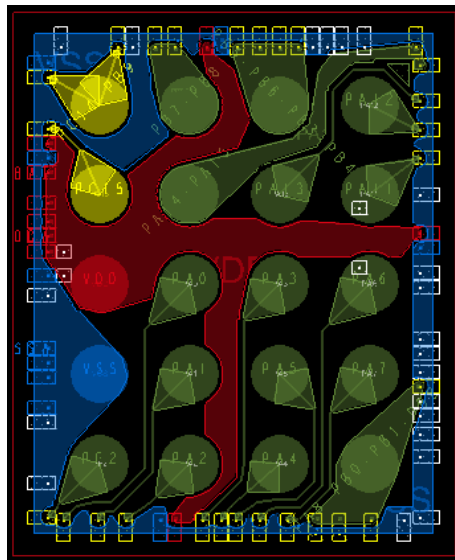


Figure 1-6: Routing example for CSP package

For the purpose of illustrating the MCU packaging evolution, Table 1-1 summarizes the main packages used for MCU, their main connection characteristics and the maximum I/Os connection allowed by each package [5].

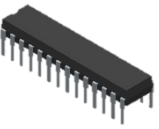
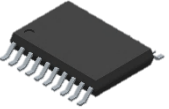


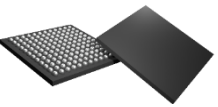
Packaging	Definition	Max allowed IOs
	<u>Dual In line Package (DIP)</u> Through hole mounted package with wirebond	40
	<u>Small Outline Package (SOP)</u> Surface Mounted package, with wirebond	100
	<u>Quad Flat Pack (QFP)</u> Surface mounted package with wirebond	250
	<u>Ball Grid Array (BGA)</u> Surface mounted package with wirebond and short routing and balls	100
	<u>Chip Scale Package (CSP)</u> Surface mounted package without bonding and with custom routing and balls	>5000

Table 1-1: Different packages overview

We can see that there are two categories of packages concerning the way they are connected to the PCB as presented in Table 1-1. The first category is the “through hole” package. Connection to the PCB is achieved by pins that are inserted and soldered into holes, predrilled into the PCB. The second category is the “surface mounted” package which is the most widespread nowadays. In this case, the lead pins or leadframe are soldered directly on the top layer of the PCB thanks to its flat structure. The use of surface mounted package technology became dominant because of the gain of space on PCBs. Indeed, because there is no need to drill holes into the PCB, it is possible to optimize the space by soldering different packages on both sides of the board.

2.4. MCU evolution

This section is dedicated to the MCU definition from several points of view: the general structure of the die, the specific block of the Input/Output Interface, the packages to embed a die and the STM32 family. To conclude this section, an overview of the MCU evolution through the years is provided. The MCU characteristics never stopped to evolve in terms of packages, dies and performance. The package, had to become as small and as cheap as possible, whilst at

the same time, increasing IOs connections and decreasing the supplies connections. In parallel, the die performance was increased as well as its operating frequency and its size, and its power supplies values were reduced. Moore's Law could be used to illustrate this MCU evolution: In 1965, Gordon Moore, using three points on the graph, extrapolated the trend predicting that the component number per IC would double every 18 months. When he outlined the IC future, he predicted it for the next 10 years. Finally, he presented a brilliant analysis of the IC future with the famous "Moore's Law" which already predicted the spread of electronics. Moreover, this rule even became a challenge in the semiconductor industry with a time slot reduction - the component number per IC would double every 18 months, the every 12 month, ect- [6]. To illustrate this IC evolution, a graph has been drawn in Figure 1-7, which illustrates 50 years of evolution for three specific points [7], [8], [9]. The first notable evolution is the size decrease of the CMOS technology with a transistor of 10 μm in 1970 and a transistor of 5 nm in 2022. The second main evolution is the number of transistors counted per thousand, illustrated in the same way with Moore's law. The third parameter is the CPU frequency evolution. Nowadays, we even speaking of the more than Moore law where the goal is a specific application instead of the new technology developments [10].

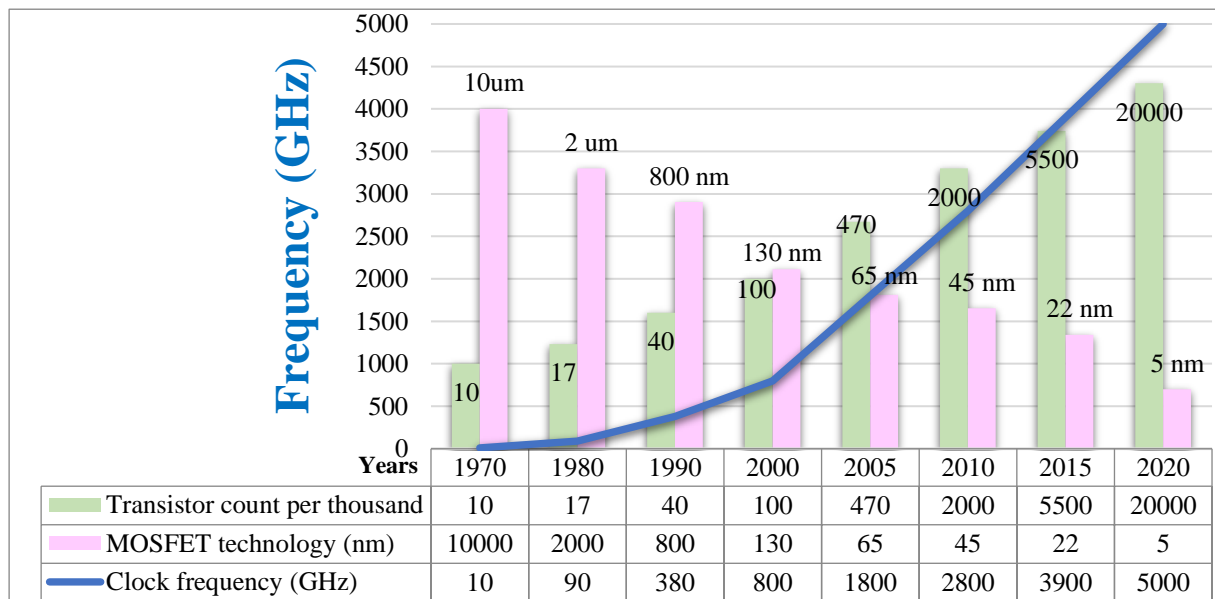


Figure 1-7: 50 years of Microprocessor trends

3. MOS Transistor

The MCU evolution is mostly due to the decrease in size of the MOS transistor. Indeed, the semiconductor technology is in constant evolution whether for its miniaturization or for its

manufacture and performance. Before going deeper into details of its creation, its structure definition and other specifications, a simplistic model of a MOS can be introduced in Figure 1-8.

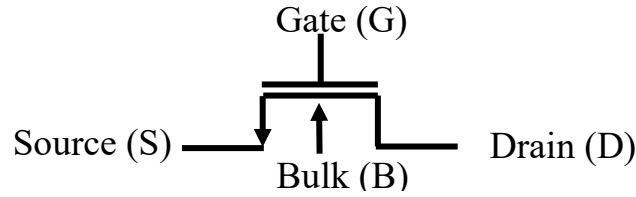


Figure 1-8: Simple structure of MOS transistor

This structure reveals four terminals with the source (S), the drain (D), the bulk (B) and the gate (G) where source and drain could be interchangeable because of the device symmetry. From a basic point of view, the transistor operation can be considered as a switch. When the voltage at the gate (V_G) is “high” and upper than the threshold voltage (V_T), the transistor establishes a “connection” between the source and the drain. Otherwise, the transistor isolates the source and the drain from each other in the case of a “low” V_G [11]. This section introduces the MOS behavior to help the understanding of the IO switching and SSN origin for later.

3.1. MOSFET history

The explanation of transistor technology and semiconductor effect began in 1833 with Michael Faraday when he described the “extraordinary case” of the electrical conduction that increases with the temperature of silver sulfide crystals and defined as the first semiconductor effect [12]. In 1938, B. Davydov, N. Mott and W. Schottky defined the semiconductor effect by the setup of an asymmetric barrier to current flow created by the electrons’ concentration on the surface of the semiconductor. This is considered as the first demonstration of the semiconductor effect [13].

In 1947, W. Shockley, J. Bardeen and W. Brattain presented their “magnificent Christmas present” which they named the “transistor” at a press conference. This first solid-state device was created with two gold contacts placed close to each other. They were held with a plastic wedge on a small slab of germanium with high purity [14]. Figure 1-9 is the picture of this first transistor known as the bipolar point-contact transistor [14]. In 1948, W. Shockley introduced the bipolar junction transistor (BJT) where both electron and electron holes could carrier charge. The BJT required 3 years of process development in order to be manufactured in quantity but became the first device used for the next three decades. In 1952, the first “transistorized consumer product” appeared on the market with the hearing aid from Sonotone. It was developed with one transistor which operated with two vacuum tubes and each transistor

cost \$229.50 USD. In 1956, the discovery of the transistor point-contact transistor was rewarded with the Nobel Prize for physics for “their research on semiconductors and their discovery of the transistor effect” [15]. Less than thirteen years later, J. Atalla and D. Kahng demonstrated the first field-effect transistor (FET) and developed the MOSFET.



Figure 1-9: First semiconductor created

From this first bipolar transistor (BJT) in 1947 to the CMOS design (complementary metal oxide Semiconductor) today, the evolution never stopped from all points of view: the manufacturing process and the tests procedure [16], [17], the materials of the transistor and its technology [18], [19] as well as theories, equations, and demonstrations for semiconductor effect [20], [21]. All of this leading to the electronics proliferation that we now take for granted in our everyday. Indeed, if the last few decades are analyzed, each generation could see the arrival of electronic devices in its daily life like home-computers, mobile phones, smart watches, virtual reality headsets, and so on. This change of common life and, more generally of the electronics world originated from the transistor discovery and evolution as it became the first technology used for the development of ICs.

3.2. MOSFET Structure

The purpose of this subsection is a reminder of the physical transistor structure through a simplified n-type MOS (NMOS) shown in Figure 1-10. The connection with the transistor's terminals is made by metallic contacts. The NMOS transistor is manufactured on a p-type bulk also named substrate or well. The source and the gate are defined with two doped n regions. The gate is defined by a conductive piece of polysilicon or metal, isolated from the bulk with a silicon dioxide (SiO_2 or High-K dielectric). Another element to point out within this simplified structure, is the definition of L , the length of the gate which is the “source-drain path”, and W its width. The principal action of the device occurs under the gate oxide in the substrate region with electron movement from the source to the drain depending on the V_G voltage [22]. The

last and forth terminal is the bulk (B) used to set the bulk potential. The potential of the bulk has an important influence on the device characteristics even if generally, this bulk is directly connected to the minimum or the maximum potential of the circuit -for the NMOS, the bulk is connected to the minimum one-.

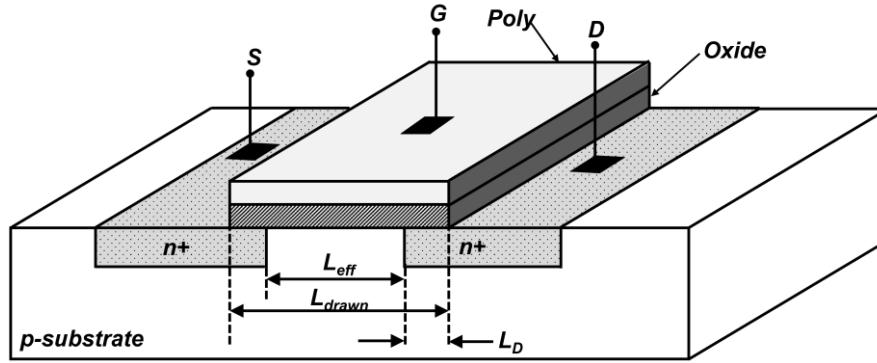


Figure 1-10: MOS structure

Finally, this CMOS technology embeds NMOS and PMOS transistors where PMOS is basically obtained by inverting all doping types including the bulk one [22], [23]. Hence, the two of them have an “opposite” behavior which permits a wide range of possibilities in CMOS design. The procedure required to manufacture this transistor and by consequence an IC is complex and involves different steps such as : Oxide growth, thermal diffusion, Ion implantation, definition of active area, photolithography, metallization, etc.[23]. Because this is not the main subject of this thesis this subsection didn’t detail all of those steps. Nevertheless, should you like to know more, there are many books available on the market with all explanations [22], [23].

3.3. CMOS model and behavior

For IC design, models are used to facilitate work and comprehension of a schematic. Maybe the best known example is the plan for a house construction where walls, stairs and so on are modeled with different geometrical forms. In electronic design, a model is used to represent a component or an object in a schematic. In CMOS technology there are different levels of complexity and accuracy for a model, going from the simplest one drawn by hand to a more complex one, as close as possible to the real structure, and used for computer simulations. For a transistor, standards are available to define the model that can be used for electronic simulations such as SPICE. One of these models is the BSIM (Berkeley Short-Channel IGFET Model) that provides a physical-based, accurate and predictive model of the transistor for SPICE [24], [25]. Another model to be mentioned is the EKV MOS model

developed by C. Enz, F. Krummenacher and E. Vittoz who named their model from their family name [26]. The EKV model is one of the most used by analog designers because it is an accurate and predictive model without discontinuity between operational regions [27]. Finally, symbols used for NMOS and PMOS are introduced in Figure 1-11 as well as useful voltages and currents [28].

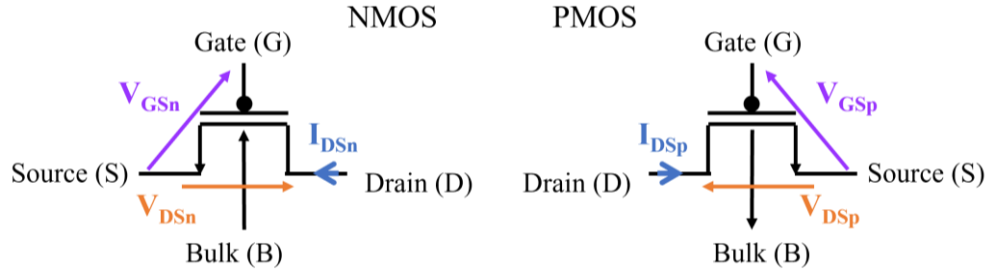


Figure 1-11: NMOS and PMOS Model

For a first approach, the transistor behavior has been simplified by a controllable switch depending on the voltage applied to the gate. In reality, this is more complex and will be defined by several parameters listed below:

- Size of W and L , the channel width and length defining the “source-drain path size”
- Value of V_{DS} and V_{GS} respectively, the voltage between source/drain and source/gate for a polarization mode in weak, moderate, and strong inversion
- Value of V_T : the threshold voltage defined by the transistor characteristics
- Technology characteristics as μ_n or μ_p and C_{ox} . Respectively the electron average mobility in the channel and the oxide capacitance. To note, the factor $\mu_n * C_{ox}$ is defined as the device transconductance parameter.

Then, the transistor’s behavior could be characterized by the current I_{DS} because its equation is taking into account the characteristics listed above. From that, the transistor’s behavior could be summarized with four different regions of operation [2], [23], [29]. Here we will only introduce the transistor behavior for a strong inversion because these explanations will be sufficient to study the IO behavior and in particular the SSN. A complete study of the transistor in weak, moderate and strong inversion can be found in the book of C. Enz [27].

The first region is the cut-off one also named subthreshold voltage. The transistor behavior is defined as “blocked”, and the switch is open. In that case, there is no current flow which means the I_{DS} is equal to zero, only the leakage current can be measured. The transistor is in this region when $V_{GS} < V_T$.

The second region, named the linear, Ohmic or triode region, represents the region where the transistor operates like a resistor. The transistor operates in linear when $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$ with the I_{DS} calculation defined by the Equation 1-1. Moreover, when $V_{DS} \ll V_{GS} - V_T$ the associated resistance is defined by the Equation 1-2.

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Equation 1-1: I_{DS} current in linear region and a strong inversion

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

Equation 1-2: Equivalent resistance of MOS in linear region

Third region is the saturation one and occurs with $V_{GS} > V_T$ and $V_{DS} > V_{GS} - V_T$. A saturated transistor basically operates as a current source and is relatively independent of V_{DS} . Equation 1-3 provides the associated formula for the I_{DS} calculation.

$$I_{DS} = \frac{\mu_n C_{ox}}{2} * \frac{W}{L} * (V_{GS} - V_{TH})^2$$

Equation 1-3: I_{DS} current in saturation region and a strong inversion

The fourth and last region is the avalanche one. This region is reached when V_{DS} become superior to the maximum V_{DS} handled by the transistor and could lead to the transistor breakdown.

These four regions are summarized in Figure 1-12, where I_{DS} is defined in function of V_{GS} in the right figure and in function of V_{DS} in the left figure [29]. It is to be noted that, equations are defined here for the NMOS but can also be used for the PMOS with an opposite sign and μ_p instead of μ_n .

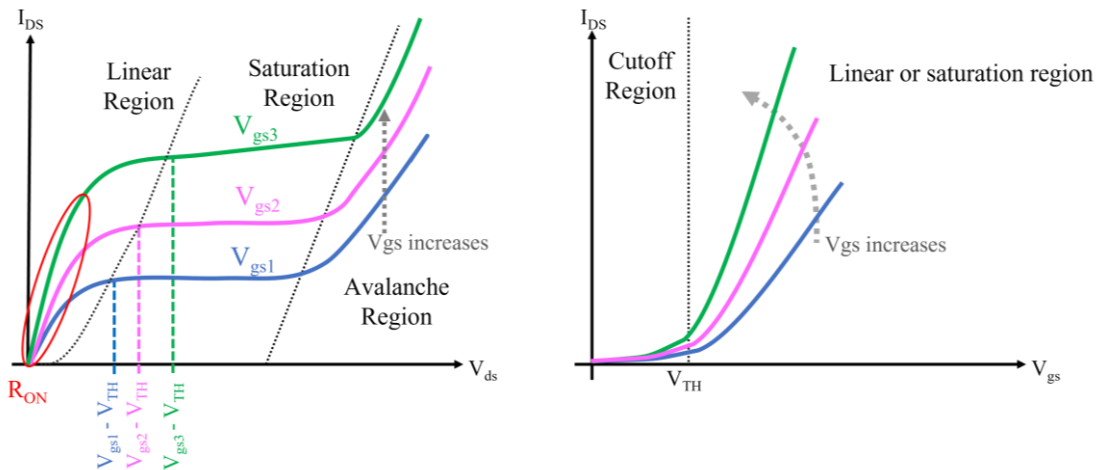


Figure 1-12: MOS Behavior with, Left: I_{DS} in function of V_{DS} and Right: I_{DS} in function of V_{GS}

3.4. Conclusion

This section summarized the CMOS technology with the basic behavior of the MOS transistor in strong inversion. These details of MOS model and behavior are useful to understand the origin of SSN effect that will be introduced later in this chapter. The sections 1 and 2 were used to describe the general evolution of MCU performance thanks to the MOS technology. One example can be cited from Intel website to illustrate this evolution [30]: *“The original transistor built by Bell Labs in 1947 was large enough that it was pieced together by hand. By contrast, more than 100 million 22 nm tri-gate transistors could fit onto the head of a pin [and this, less than 60 years later]”*

Such performance evolution always implies some drawbacks. Indeed, when the MCU increases its operating frequency, decreases its size and its power supply values -as well as the amount of power supply pins for package- this creates new MCU constraints in terms of electromagnetic compatibility (EMC) like the problem of SSN. If these constraints are neglected, this could lead to an MCU failure, so they must be considered and anticipated in order to stay competitive on the market. Section 4 will go through the definition of EMC from a general point of view and regarding the SSN in particular. Then, section 5 will provide explanation about the SSN origin and its impact inside an MCU, based on the knowledge acquired with the MCU and the CMOS technology presentation.

4. Understanding electromagnetic compatibility

4.1. Introduction and EMC definition

Because a microcontroller is a multi-application and versatile device, it has to be compatible with many environmental constraints. For example, an MCU must be able to work at high and also low temperature – generally, from -40°C to 125°C-, it must also resist to humidity, and it needs to have a certain level of electromagnetic compatibility (EMC). Nowadays, EMC is a phenomenon that concerns everyone. For example, passengers on airplanes need to turn off their mobile phones during landing and take-off. The EMC principle could be summarized as a system that must display its expected behavior when it is placed in a disturbed environment where interferences are generated by the system itself or by another electrical components in its environment [31]. A general definition for EMC can be cited from the International Electrotechnical Commission (IEC).

“The ability of a device, equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbance to anything in that environment”[32].

Two facts can be pointed out from this EMC definition. The first point is the principle of level and tolerance highlighted with “the ability to function satisfactorily” and the “intolerable electromagnetic interference”. In other words, there are levels of susceptibility but also levels of electromagnetic emission accepted depending on the equipment usage. Nowadays, this is classified with standards that define limits for emitted and received interferences [3]. Figure 1-13 vulgarizes this classification with minor, medium or major issues. For example, if an interference disturbs the TV and impedes watching a movie this is a minor issue. Now, with the aircraft example, if an interference disturbs the aircraft systems, this could lead to injuries or deaths, which is definitely a major issue. So, in order to release an MCU or any electronics device on the market, the device must comply with requirements defined by the European directives to guarantee the EMC compliance and to obtain the CE marking.

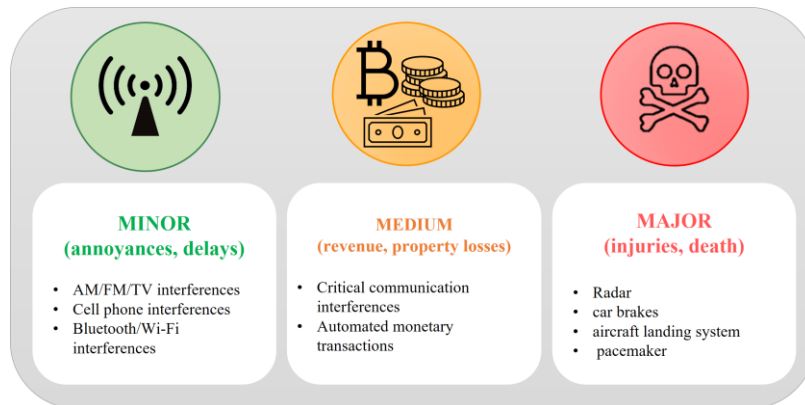


Figure 1-13: EMC issues gravity

The second point to be noted is the difference between the susceptibility of a system to an electromagnetic interference and the generation of this interference by a system, dividing the EMC problematic in two parts. On one hand, the electromagnetic susceptibility (EMS) studies the immunity of the device in the presence of an interference. In that case, the electronic device is considered as the victim of its electronic environment. On the other hand, the electromagnetic interference (EMI) defines the device as an aggressor and studies its perturbation generation. Finally, the dissociation between intra-system and inter-system perturbation should be highlighted. In the case of inter-system, the electronic device is the victim of an external EMI generated in its electromagnetic environment as this is the case

with the example of aircraft and cellphone. In the case of intra-system, the victim is disturbed by an internal EMI, generated by the system itself leading to an auto-susceptibility problem. This is summarized with a diagram in Figure 1-14 [32].

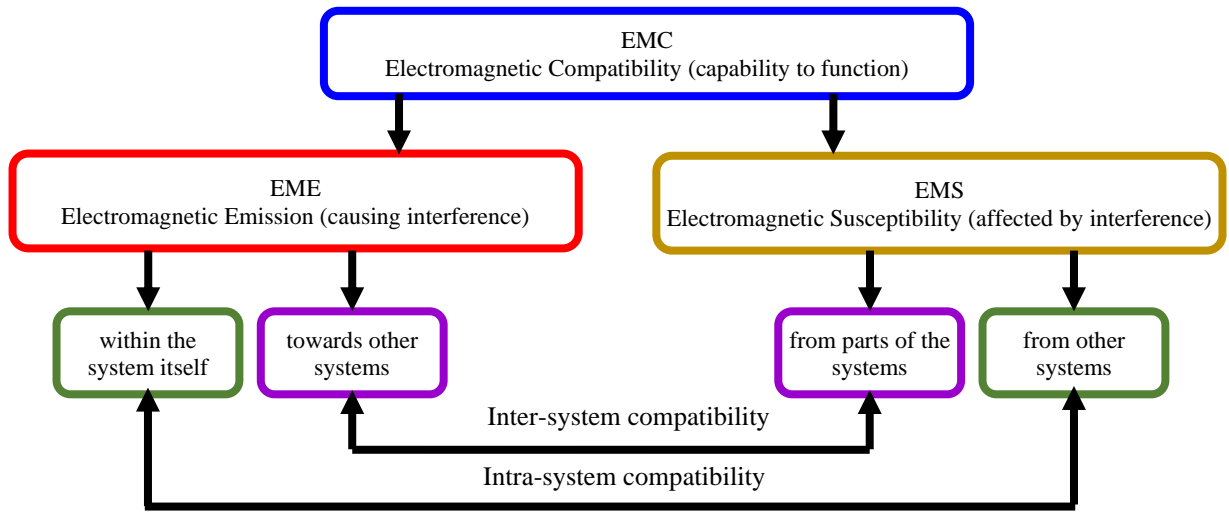


Figure 1-14: Relation between various EMC terms

In this section, the EMC origin is explained with the Maxwell equations. Then, additional explanation regarding EMI and EMS are given as well as the propagation path between them. Finally, this section explains how the SSN is part of the EMC consideration into an MCU.

4.2. The physics behind EMC

The base of electromagnetic theory is given with Maxwell's equations which give the possibility to define the electromagnetic state of an environment in any point and at any instant. Even if electromagnetic principles were highlighted by many physicists such as Faraday, Ampere and Gauss, it was James C. Maxwell in 1860, who determined the equations that define the Electromagnetic Field (EM), composed of the electric field intensity vector \vec{E} (in V.m^{-1}) and the magnetic flux density vector \vec{B} (in Wb.m^{-2}) [33], [34]. Some approximations are generally made such as lumped-circuit model, initial and limit conditions -as long as the problem is electrically small- because being able to find a solution to those equations is not a simple process. Whatever equation's complexity as mentioned by C.R. Paul in his book [35]:

“Maxwell's equations form the cornerstones of electromagnetic phenomena [...]. We should always be cognizant of the fact that Maxwell's equations govern all electromagnetic phenomena and their [the equations] complexity does not change this fact”.

Using Maxwell's theory, it is possible to define the EM field creation, to understand if this is a magnetic or electric field but also to determine how it is propagated [5] [35]. Table 1-2 gives a summary of Maxwell's equations with their integral forms as well as their differentials form -also named local or punctual-.

Faraday Law	$\nabla E = -\frac{\partial B}{\partial t}$	$\oint_{\partial \Sigma} E \cdot dl = -\frac{d}{dt} \iint_{\Sigma} B \cdot dS$
Ampere's Law	$\nabla B = \mu_0 \left(J + \varepsilon_0 \frac{\partial E}{\partial t} \right)$	$\oint_{\partial \Sigma} B \cdot dl = \mu_0 \left(\iint_{\Sigma} J \cdot dS + \varepsilon_0 \frac{d}{dt} \iint_{\Sigma} E \cdot dS \right)$
Gauss's Law	$\nabla E = \frac{\rho}{\varepsilon_0}$	$\iint_{\partial \Omega} E \cdot dS = \frac{1}{\varepsilon_0} \iiint_{\Omega} \rho \cdot dV$
Gauss's law for magnetism and charge conservation	$\nabla B = 0$	$\iint_{\partial \Omega} B \cdot dS = 0$

Table 1-2: Maxwell's equations

4.3. Electromagnetic susceptibility and coupling path

The electromagnetic susceptibility (EMS) is the ability of a device to operate without degradation of its performance in the presence of an EMI. Based on the standard IEC 62132, effects of electromagnetic perturbations on an IC are classified in four categories. This norm defines the device susceptibility level based on the observed EMI consequences [36]. This is summarized with Table 1-3:

Level	Observations
A	Normal performance
B	Temporary functionalities degradations or even a loss of functionalities. The nominal operation is recovered after the failure removal.
C	Temporary functionalities degradations or even a loss of functionalities. The nominal operation is recovered after the removal of the failure and a reset of the product.
D	Permanent functionalities degradations dues to a system damage

Table 1-3: Failure level classification for a system disturbed by an EMI

Different parameters could influence the susceptibility of an IC. Besides the perturbation characteristics, there are also the design choices and the technology used as well as the IC usage [36]. More details about the STM32 susceptibility can be found in the thesis of Y. Bacher [3].

If a device is susceptible to interference, it means that there is a coupling path between the EMI and the EMS. By analogy to the Maxwell equations, the coupling path is defined as the electromagnetic interference propagation. Basically, a disturbance could be propagated through two different paths. Firstly, we will speak of conducted emission when a noise propagates through a physical connector. For example, when a light at home shortly lose intensity -or blinks- because an electronic device required too much power. Then, we will speak of radiated emission when the noise is propagated through “the air” and disturb another device in its environment. This is the case for the example of the cellphone used in the airplane mentioned before. Inside the MCU, the same principle of intra-system radiated and conducted emission is found. An example of radiated emission could be cited in the internal memory perturbation studied by J.P. Leca thesis [2]. Then, the SSN effect is defined as a conducted emission where interference generated by an IO is propagated through power and ground supply lines. Figure 1-15 provides an example of intra-system propagation with conducted emissions through power and ground generated by the core or by switching IOs and radiated emission generated by the memory and propagated through air.

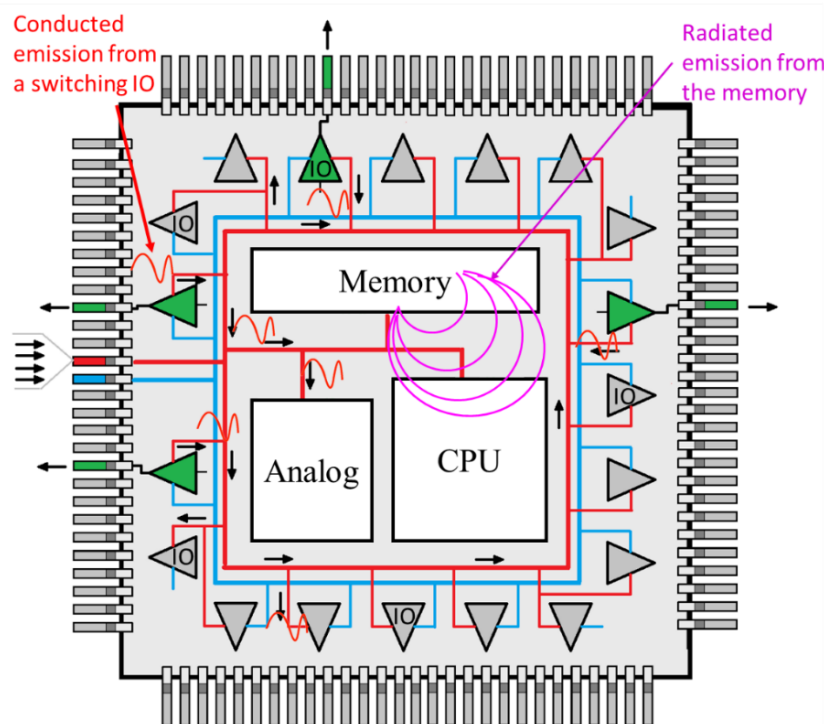


Figure 1-15: Auto-susceptibility of an Integrated Circuit

It is worth to be noted that an MCU is also susceptible to inter-system EMI propagated by conduction and radiation. The radiated emission could appear between two components close to each other and an interference could be propagated by conduction through any PCB physical connection.

4.4. Electromagnetic interference (EMI)

From a general point of view, external EMI can be classified by its level of power and its frequency of work as illustrated in Figure 1-16 [36].

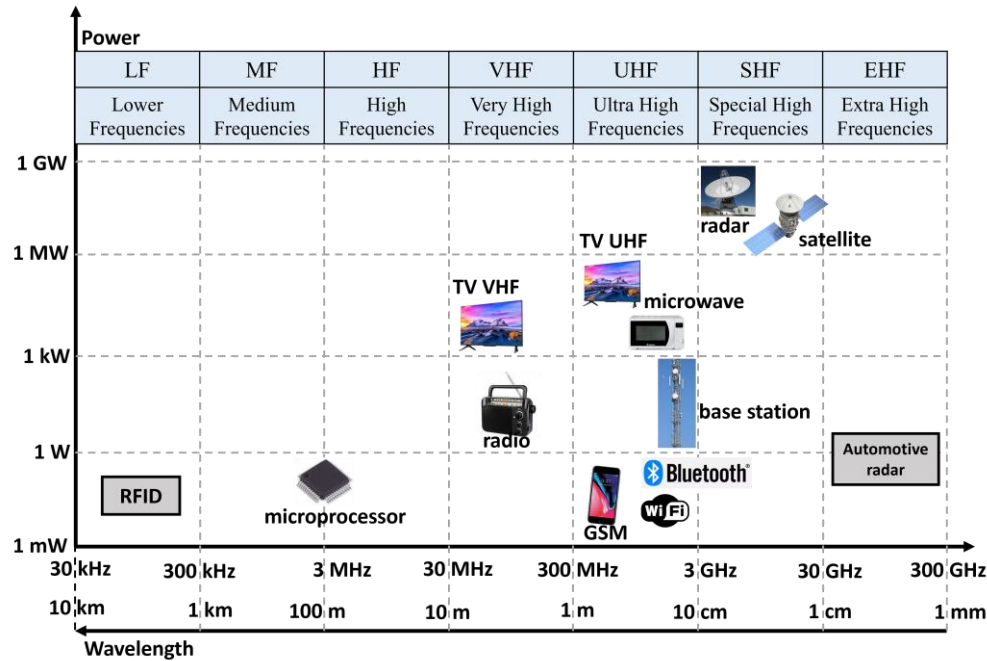


Figure 1-16: EMI classification overview

There are many different possible sources for an EMI and an overview of them is depicted in Figure 1-16. External EMI is the best known as it can be encountered by everyone in modern life as illustrated in Figure 1-17 [3]. It is mainly classified in two categories: natural or industrial. For natural noise, the source could be an atmospheric noise, a magnetic storm, a thunderstorm, etc. In contrary, any perturbation that emanate from a manmade object will be considered as an industrial EMI. This is the case with radio and wireless communications, motors, powerlines, Electrostatic discharge (ESD), but also from another integrated circuit close enough to the MCU on a PCB [3].

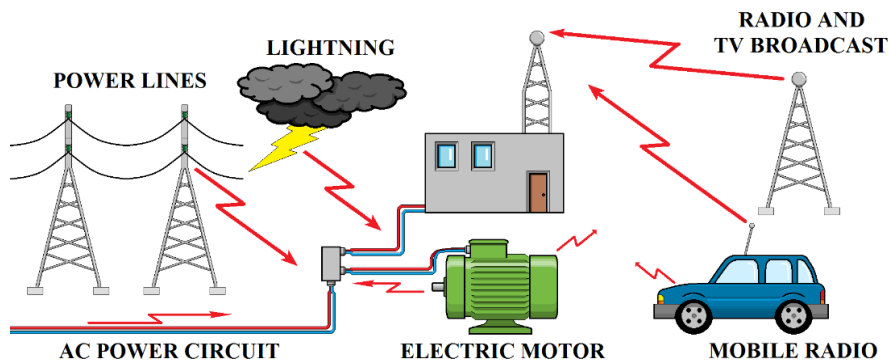


Figure 1-17: External EMI usual sources [3]

5. From the CMOS inverter to the Simultaneous Switching Noise

In the bibliography, demonstration of SSN effect can be found in scientific papers from 1985 and even earlier [37]. In this section, we will explain the origin of this phenomenon, based on MOS transistor knowledge introduced in previous paragraphs. Then, the SSN effect at the MCU level will be defined, justifying in the same way the purpose of this thesis.

5.1. CMOS Inverter

5.1.1. Inverter principle

The CMOS inverter is one of the most basic circuits in analog and mixed design composed only of one PMOS and one NMOS transistors. Figure 1-19 schematizes this circuit including all notations for currents and voltages as V_{DS} the drain-source voltage and V_{GS} the gate-source voltage for transistors. The inverter behavior can be described as follows: when V_{in} is low and equal to V_{SS} the PMOS is in linear region and the NMOS in the cut-off region, leading to a logical '1' for the output. Reversely, when V_{in} is high and equal to V_{DD} , the PMOS is off and the NMOS is conducting which implies a logical '0' on the output [11].

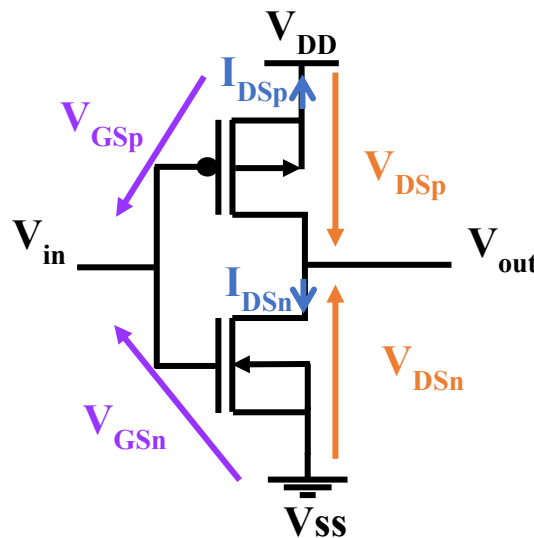


Figure 1-19: Basic inverter schematic

5.1.2. Voltage transfer characteristic

The voltage transfer characteristic (VTC) of a CMOS inverter is defined by the waveform of V_{OUT} in function of V_{IN} . This waveform is obtained by the superposition of the two I-V curves of each transistor. For a quick reminder, the I-V curve represents the I_{DS} current in function of the V_{DS} voltage for different values of V_{GS} . Figure 1-12 illustrated this for an NMOS transistor. Of course, for a PMOS transistor, this I-V curve will be on the "opposite" side which means it has to be "flipped over" compared to the NMOS curve. It is also necessary to express each of these I-V curve in function of V_{IN} and V_{OUT} . Figure 1-20 illustrates the typical I/V curves and for that, the following assumption needs to be made [38]:

- $I_{DSn} = -I_{DSP} = I_{SDP}$
- $V_{GSn} = V_{in}$ and $V_{DSn} = V_{out}$
- $V_{GSp} = V_{IN} - V_{DD}$ and $V_{DSp} = V_{OUT} - V_{DD}$

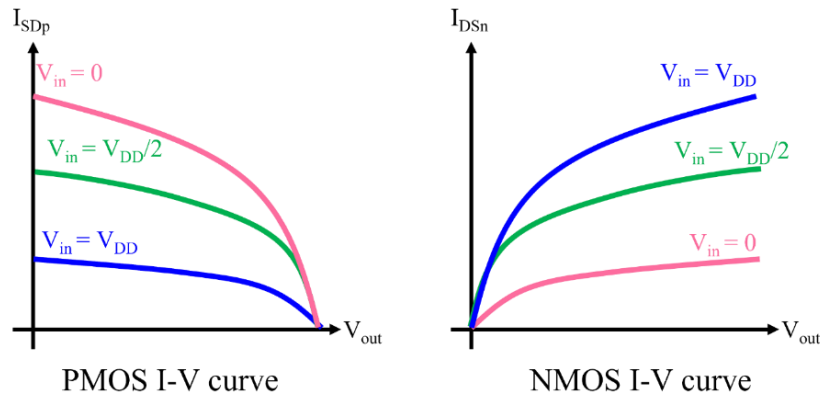


Figure 1-20: I-V curve for PMOS and NMOS

Finally, it is then possible to superpose the two curves, as depicted in Figure 1-21 [39].

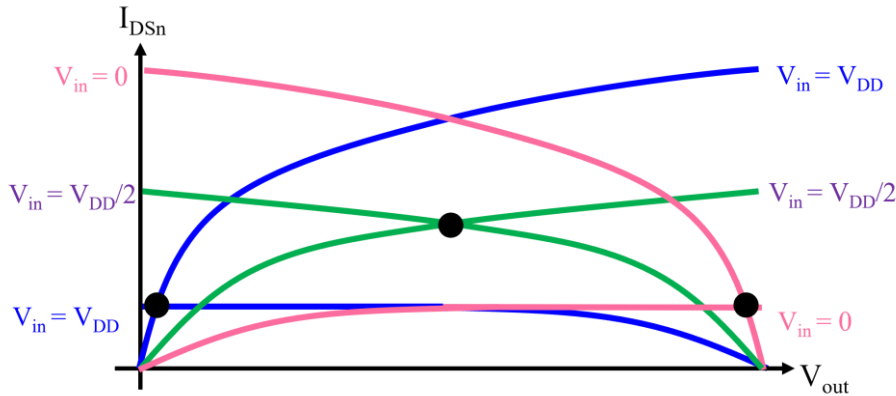


Figure 1-21: I-V curve of NMOS and PMOS superposition

Once this waveform is obtained, we can extract the VTC waveform by identifying the value of V_{IN} and V_{OUT} at each crossing point -defined with a black dot in Figure 1-21-. Figure 1-22 illustrates the final VTC waveform obtained and Table 1-4 summarizes this waveform in terms of input and output values and transistor operation.

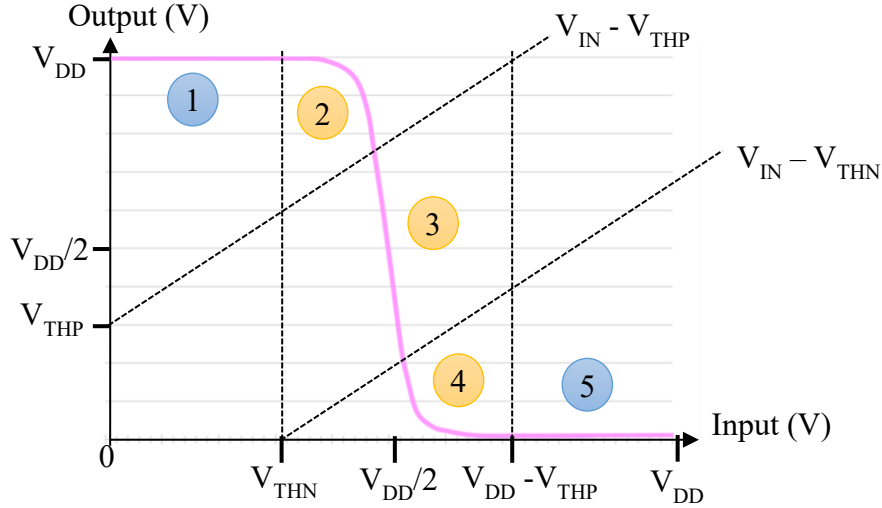


Figure 1-22: Voltage Transfer Characteristics of an Inverter

Region	Input Voltage V_{IN}	Output Voltage V_{OUT}	NMOS Transistor	PMOS Transistor
1	$V_{IN} \leq V_{THN}$	$V_{OUT} = V_{OH} = V_{DD}$	Cut-off	Linear
2	$V_{THN} \leq V_{IN} \leq V_{OUT} - V_{THP}$	$V_{OUT} > V_{DD}/2$	Saturation	Linear
3	$V_{IN} \approx V_{DD}/2$	$V_{OUT} \approx V_{DD}/2$	Saturation	Saturation
4	$V_{OUT} + V_{THN} \leq V_{IN} \leq V_{DD} + V_{THP}$	$V_{OUT} < V_{DD}/2$	Linear	Saturation
5	$V_{IN} \geq V_{DD} - V_{THP}$	$V_{OUT} = V_{OL} = 0$	Linear	Cut-off

Table 1-4: Voltage Transfer characteristics table

This demonstration has been done with the specific purpose of highlighting the three specific regions 2, 3 and 4. In these ones, PMOS and NMOS could be simultaneously in saturation mode or in saturation/linear mode. In other words, there are states where both of the transistors are conducting at the same time leading to a resistive current path between the power and the ground.

5.1.3. Dynamic properties of the inverter

For this study, the schematic of the inverter has been redrawn in Figure 1-23 where a load capacitor was added to the output. Generally, the inverter is used to control an electronic block or to transmit information. Whatever is connected to its output, we can assimilate it to a

load capacitor where its value is defined by the circuit complexity. Figure 1-24 illustrates the transient response of the inverter.

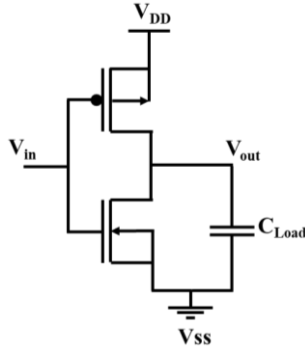


Figure 1-23: Inverter Schematic with Cload

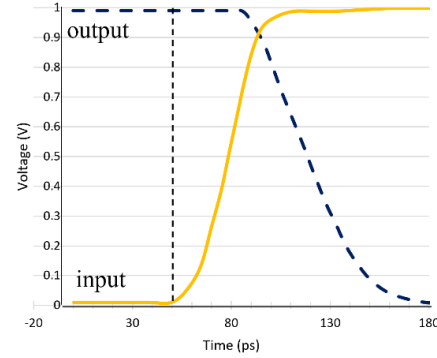


Figure 1-24: Inverter transient behavior

This dynamic study is divided into two points. The first one is the propagation delay which appears between the input and the output state change. This delay can be calculated with the Equation 1-4 where R_{eqn} and R_{eqp} are the equivalent resistance of NMOS and PMOS and C_{load} the load capacitor connected to the output inverter [40]. This propagation delay can be improved by reducing the load capacitor value or by increasing transistor size. In the same way, these parameters will have an effect on inverter rising and falling time.

$$t_{pg} = 0.69 * C_{load} \left(\frac{R_{eqp} + R_{eqn}}{2} \right)$$

Equation 1-4: Inverter propagation delay

The second point to be studied is the transient current of the inverter defined on one hand, by the overlap current and on the other hand, by the charging and discharging current. The overlap current also named through current appears when both transistors are conducting. From the VTC waveform we know that both transistors are conducting in region 2, 3 and 4 with the current which is flowing directly from V_{DD} to V_{SS} . The maximum through current $I_T(max)$ is given by Equation 1-5 [40].

$$I_T(max) = \frac{K_N K_P}{2(\sqrt{K_N} + \sqrt{K_P})} (V_{DD} - V_{THP} - V_{THN})^2$$

Equation 1-5: Through current formula

$$K_N = \mu_n C_{ox} \frac{W_n}{L_n} \quad \text{and} \quad K_P = \mu_p C_{ox} \frac{W_p}{L_p}$$

Equation 1-6: Constant definition for the through current formula

Then, the discharging current is created by the load capacitor. Figure 1-25 illustrates this phenomenon with the schematization of the current flow at the specific moment of state change. On the left schematic, the low input implies the output to switch from a logical 0 to a logical 1. At this moment, the discharged capacitor requires to be quickly charged thanks to the PMOS conduction, creating a current consumption on the V_{DD} . Reversely, for a high input and an output from high to low, the capacitor will be discharged through the NMOS transistor to the ground. So, during the charge or the discharge, a current consumption appears on the power or on ground defined as the “discharging current” I_D and calculated with Equation 1-7. Where C_{Load} is the load capacitor and $T_{F/R}$ the inverter falling or rising time.

$$I_D = C_{Load} \frac{dV}{dt} \approx C_{Load} \frac{V_{DD}}{T_{F/R}}$$

Equation 1-7: Discharging current formula

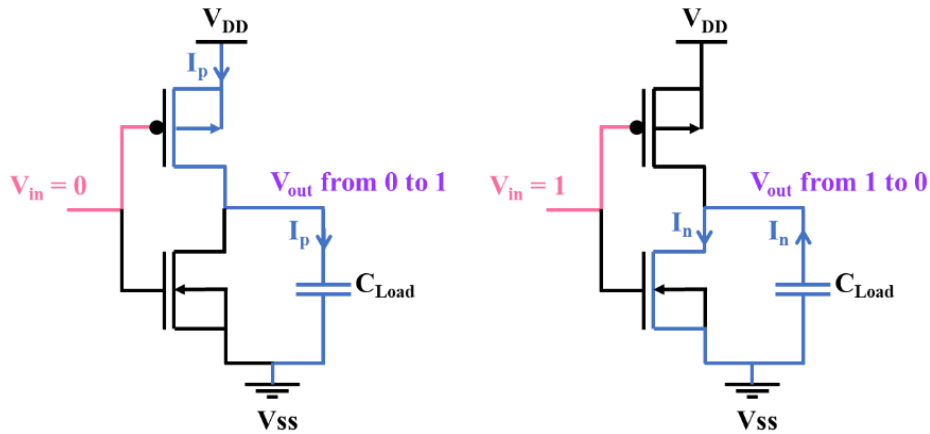


Figure 1-25: Current flow for the capacitor charge and discharge

To complete this inverter dynamic study, a simulation has been done with a standard CMOS inverter with different C_{load} values as illustrated in Figure 1-26. Then the conclusions are:

- The rising edge of the current peak -also named switching current or di/dt - is defined by the through current.
- The falling edge of the switching current is defined by the charging/discharging current required by the load capacitor. We can conclude that: the smaller the capacitor is, the smaller the di/dt duration will be.
- This simulation also depicts the effect of the load capacitor on the output where the output rising time increases proportionally to the load capacitor. Of course, if the rising time increases, then the propagation delay increases in the same way.

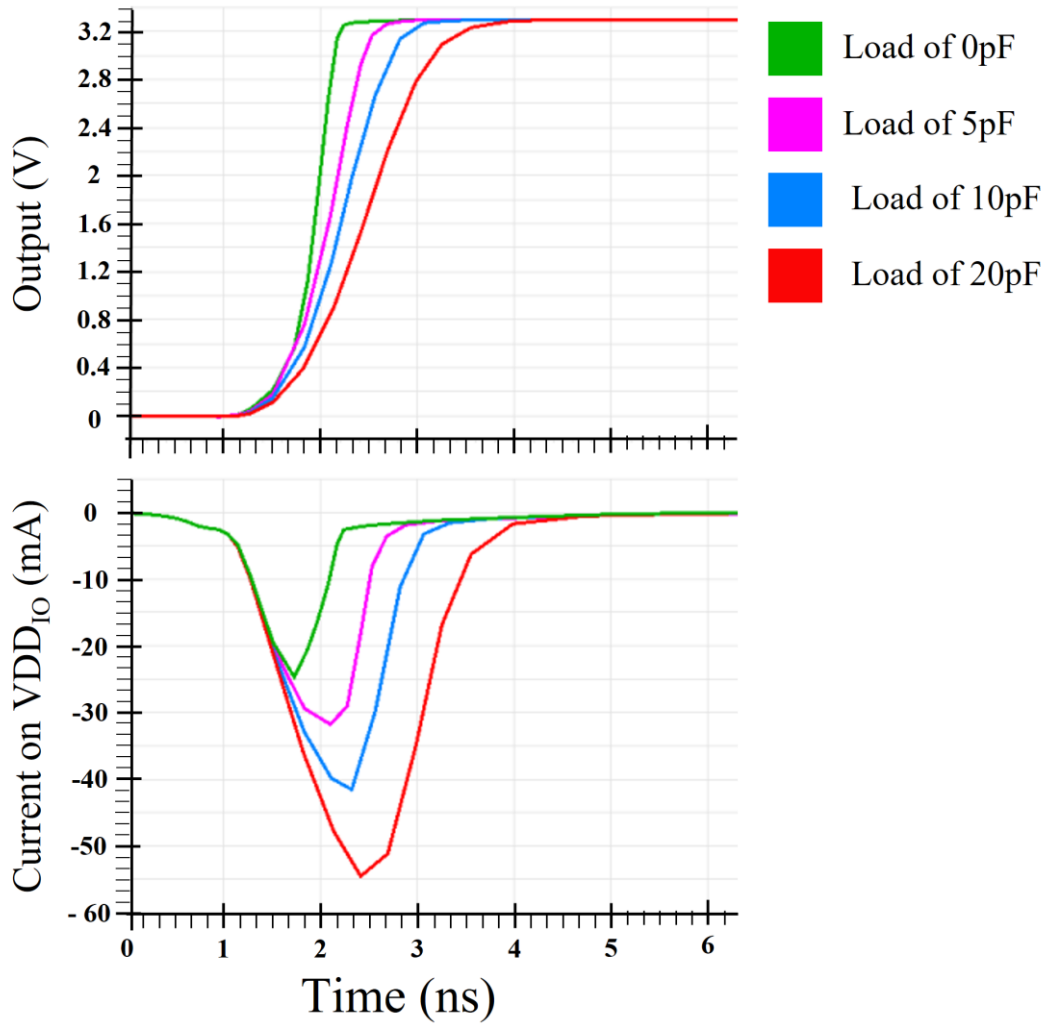


Figure 1-26: Impact of the C_{load} on rising time and current peak for a basic inverter

5.2. Simultaneous Switching Noise (SSN) effect

Delta-I noise, power bounce or ground bounce are different terminologies to determine the same problematic of the Simultaneous Switching Noise (SSN). The SSN effect is defined as a voltage drop on power or ground supply. It is created by a current peak di/dt flowing through passive elements of an RL circuit -a resistance, an inductance-. The origin of the current peak di/dt is known thanks to all explanations provided in the inverter subsection. Nevertheless, the demonstration was made from an ideal point of view because the inverter's supplies were considered as ideal. In reality, the Power Distribution Network (PDN) of the same inverter is characterized by the passive elements of the RL circuit [41]. In conclusion, the real schematic of an inverter will be composed of the inverter with its load capacitor with the parasitic elements of the PDN as summarized in Figure 1-27 [34]. Then, for each inverter state change, the current

peak generated will flow through these parasitic elements, leading to a voltage variation defined by the Equation 1-8.

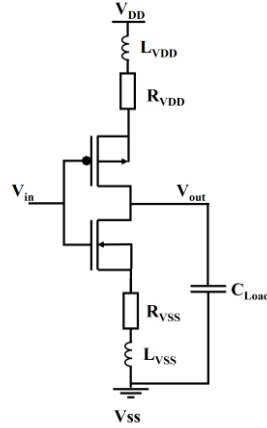


Figure 1-27: Inverter schematic with PDN's parasitic elements

$$\Delta V = L_{VDD/VSS} * \frac{di}{dt} + R_{VDD/VSS} * i$$

Equation 1-8: Simultaneous Switching Noise basic equation

5.3. Simultaneous Switching Noise (SSN) at the MCU level

For this explanation it is necessary to go back to the IO design and its behavior and to keep in mind that, the IO is the link between the MCU core and its external environment. Among all blocks that compose the IO, the output buffer is the one used to transmit information from the MCU's core to the outside and reversely for the input buffer. Figure 1-28 illustrates the IO black box related to these buffers.

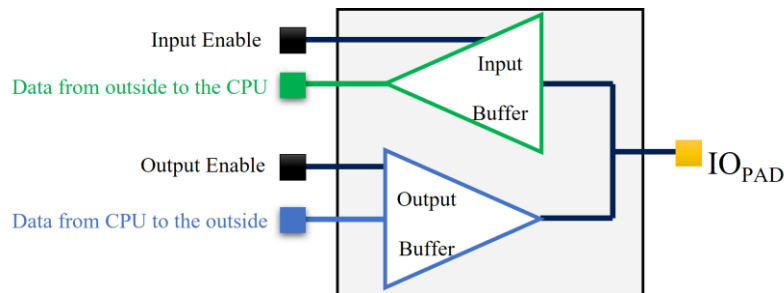


Figure 1-28: Schematic representation of a general purpose Input/Output interface black box

An output buffer could be schematized by two consecutive inverters with RL parameters of the PDN defined by the power supplies connection to V_{DDIO} and V_{SSIO} . Similarly, the schematic also takes into account the parasitic elements of interconnection wire and the load capacitor. Figure 1-29 illustrates this schematic.

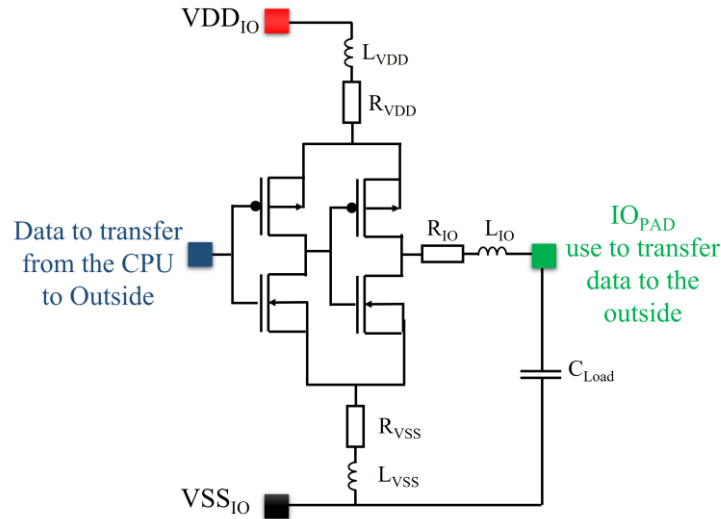


Figure 1-29: IO's Output buffer schematic

So, each time this output buffer switches to transmit information from the core to the IO_{PAD} and the outside, the switching current will be generated on the IO power supplies. The parasitic inductance and resistance of the PDN are defined by the connection made by the die, the package, and the PCB. The physical PCB characteristics will bring parasitic elements for any connection and their values will depend on the connection geometry. For example, a ground plane will have a small inductance of only 1 or 2 nH whereas the tracks for IO connections are defined by a 10 nH inductance or even more. Similarly, the package connections will be defined by parasitic elements in function of the package definition. Table 1-5 provides an example of typical values according to the package geometry. This table doesn't include balls parasitic elements as they are considered negligible [43]. Finally, concerning the parasitic elements of the die, they are mainly associated to rails that distribute the V_{DDIO} and V_{SSIO} to all IOs around the padring. The padring has been introduced in the MCU section, but for a quick reminder, this term defines IOs that are spread all around the die. Because each IOs has its own pad connection, the whole thing is commonly named the padring.

Lead/routing value	Resistance (Ω)		Inductance (nH)		Capacitance (pF)	
	Corner	Center	Corner	Center	Corner	Center
DIP (14 pins)	1.15	0.05	7.0	3.0	0.65	0.25
QFP (128 pins)	1.2	0.8	4.5	2.4	0.1	0.05
BGA (145 pins)	0.4	0.2	1.7	0.9	0.08	0.04
CSP (176 pins)	0.3	0.3	0.4	0.4	0.08	0.08
Wirebond	0.05	0.5	0.45	7.7	Neglected	Neglected

Table 1-5: Parasitic values example of Leadframe/routing/wirebond for a package [43]

To summarize, any time an IO is switching, it will disturb its own supplies as well as the supplies of IOs around it. For MCUs this generally involves several switching IOs leading to the modification of the SSN formula with Equation 1-9 where N is the number of switching IOs [44]. To illustrate the number of switching IOs impact on the di/dt and on the ΔV a simulation is shown in Figure 1-30, with $L_{VDD/VSS} = 1\text{nH}$, $R_{VDD/VSS} = 0.1\Omega$, $C_{Load} = 10\text{pF}$ and a SPICE netlist used for IOs developed in 40nm technology.

$$\Delta V = N * \left[L_{VDD/VSS} * \frac{di}{dt} + R_{VDD/VSS} * i \right]$$

Equation 1-9: SSN equation for N switching IOs

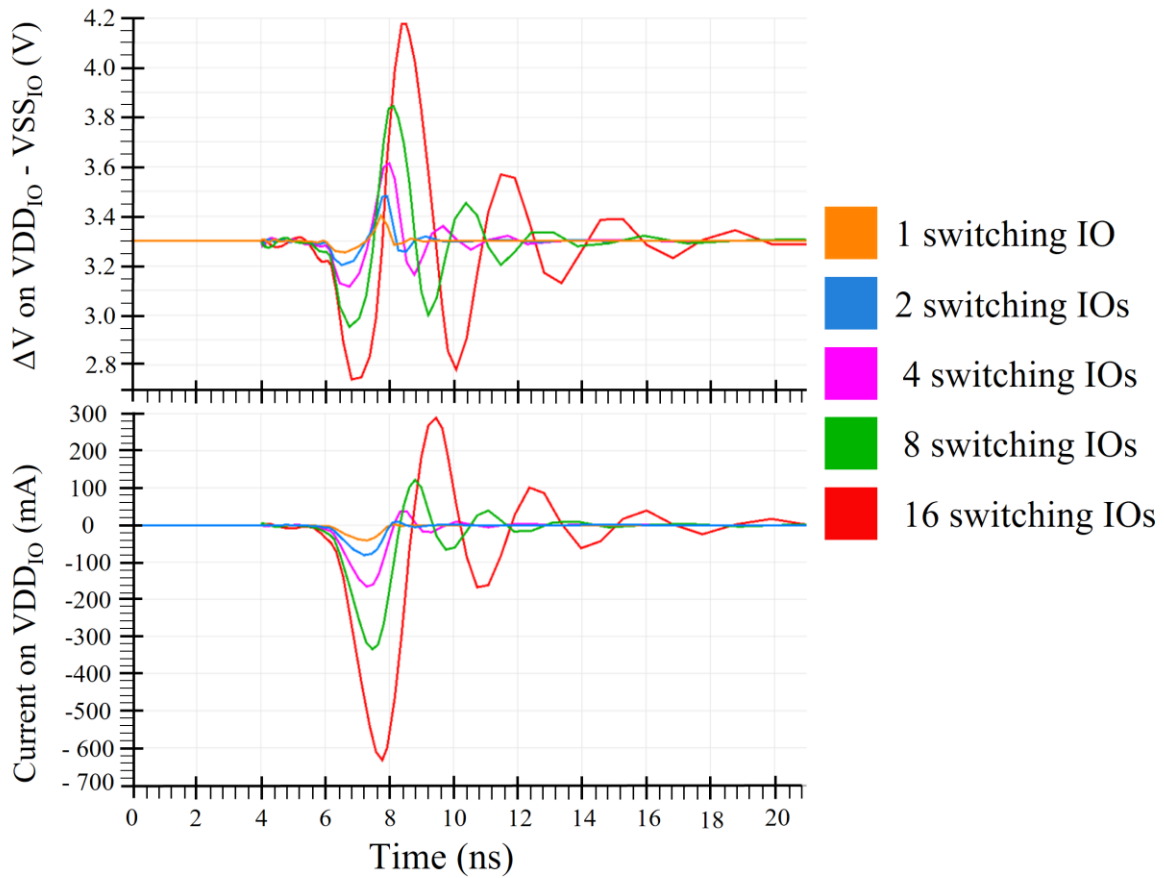


Figure 1-30: SSN effect on VDD_{IO} in function of the number of switching IOs

Nevertheless, the Equation 1-9 is used for a given number of N but, a “saturation effect” can be observed for a large number of SSO. This phenomenon is explained by IOs specifications degradation. Indeed, from a certain level of noise there will be a degradation of IOs specifications and especially for rising or falling times. As a consequence, for a large number of SSO, rising/falling time are slower than expected, leading to a smaller di/dt generated by an IO and leading to this phenomenon of “saturation effect” observable Figure 1-31. This figure shows a simulation done in the same condition as Figure 1-30 but in this case, the plot represents

the noise ΔV_{Noise} in function of the number of switching IOs (N). ΔV_{Noise} is the peak-peak observed on $V_{DDIO} - V_{SSIO}$ and it could be approximated with Equation 1-10. This equation is obtained by observation on the waveform -as drawn with green lines- , with E the maximum value reached by the curve, N the number of switching IOs.

$$\Delta V_{\text{Noise}} = E \left(1 - e^{\frac{-N}{14}} \right)$$

Equation 1-10: First order approximation of the ΔV_{Noise} in function of the number of switching IOs

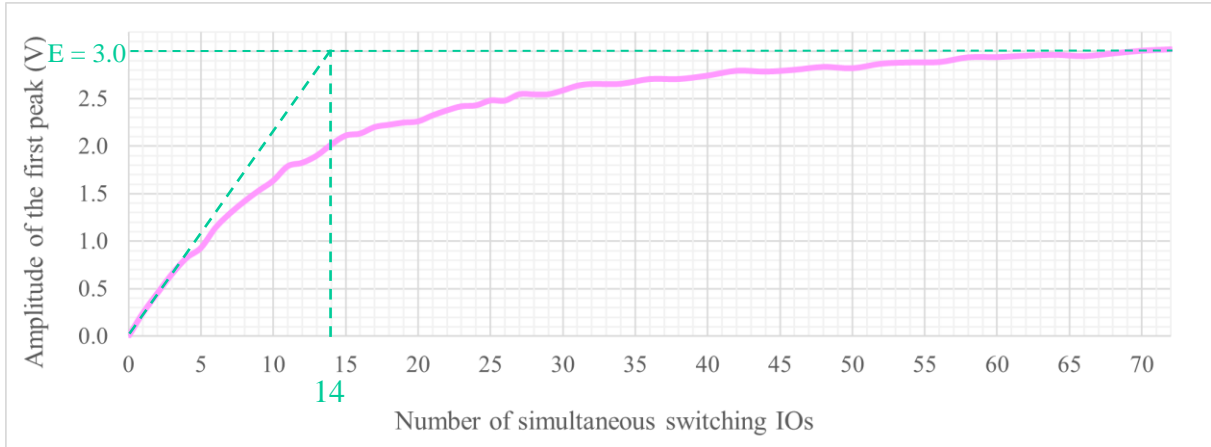


Figure 1-31: Simulation extraction of the overshoot noise amplitude in function of the number of SSO

MCU performance can be degraded by the voltage drop created by the SSN and especially IO's specification. Indeed, with too much power variation the IO's rising and falling time, the propagation delay, and the duty cycle will be deteriorated. Unfortunately, these same parameters are key when defining a communication protocol; For example, a given protocol may require that the duty cycle is comprised between 45% and 55% to ensure the communication-. In conclusion, the SSN effect, could lead to a communication failure or even more if it is not properly anticipated. Of course, as the SSN is a problem known for a few decades now, solutions already exist to reduce the SSN impact like defining a skew between the P-channel and the N-channel in order to limit the through current. The most important design optimization to highlight here, is the application of the CMOS controlled slew rate solution on the output buffer [45], [46], [47]. Thanks to this solution, IOs specifications can be "controllable" in order to reduce the di/dt generated. Obviously, the use of this solution will limits the operating frequency. An example is shown in Table 1-6 where we can see the specification of an IO designed by STMicroelectronics where there are 4 speed modes in function of the IO usage. Depending on the operating frequency needed by the communication, the IO could be settled in the associate mode and this affects rising and falling time as well as the switching current generated. From a more technical point of view, the IO is also controlled

by a block named compensation block which provides 8 signals in function of the full PVT range (Process, Voltage, Temperature) in order to optimize the di/dt based on the CMOS controlled slew rate solution. This is also illustrated with the Figure 1-32 where a simulation is settled at 3.3V and ambient temperature, for a switching IO at 1MHz and load capacitor of 20pF -ground and power connection assumed ideal-. On it, we can see the difference of the four di/dt depending on the IO speed mode.

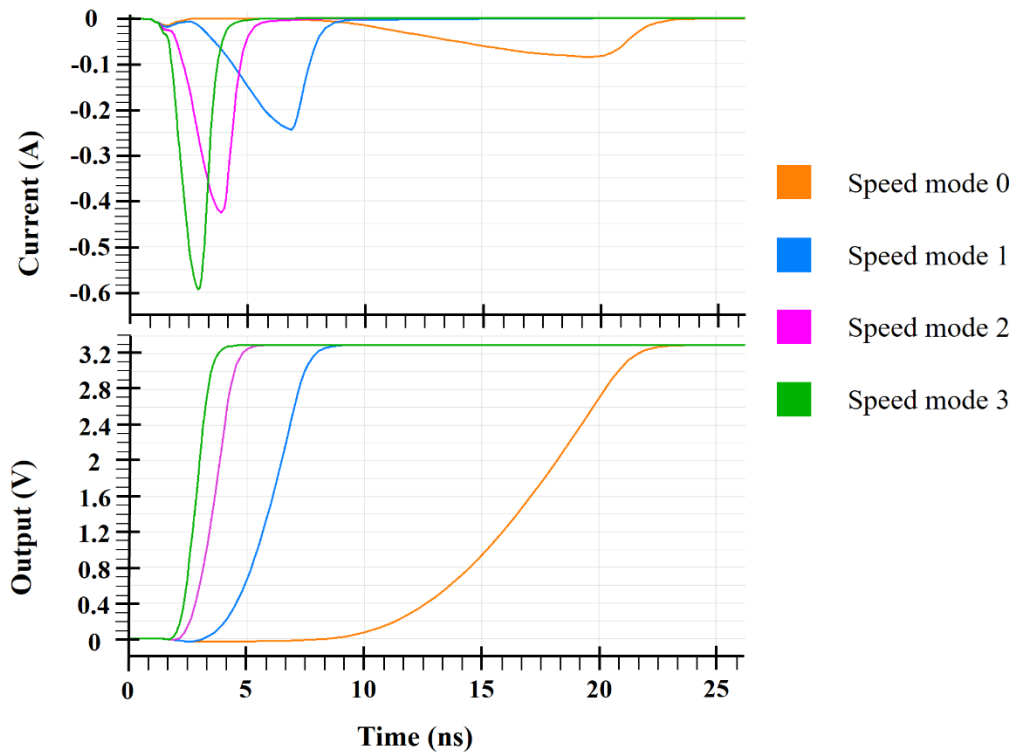


Figure 1-32: Example of the current peak depending on the IO speed mode

Supply (V)	Speed mode	Max frequency (MHz)	Max T_R and T_F (ns)	current slope (mA/ns)
3.3	0	20	8.5	5.5
	1	50	3	8
	2	100	1.7	27
	3	166	1.2	57

Table 1-6: Example of IO speed mode

6. Conclusion

This chapter provides all the necessary knowledge to properly understand the SSN effect. It started with the MCU definition, regarding the die composition and its enclosure into a package. Then it defined the MOS transistor, the main semiconductor technology used in all integrated circuits. The SSN effect was also explained, based on the understanding of the basic behavior of a CMOS analog inverter. With this chapter we now better understand the MCU auto-susceptibility created by the SSN.

Through this chapter a focus was put on the MCU general evolution in terms of die, package, and performance in relation with the CMOS technology evolution. The highlight of this evolution is the common thread of the chapter to justify the purpose of this thesis. Indeed, we came at a point where the SSN effect is becoming a real problem leading to many MCU failures nowadays when it was only a minor drawback a few decades ago. The SSN problematic must then be anticipated at the design stage thanks to simulations. For that, chapter 2 details a methodology to model and validate a complete system and chapter III will introduce the main design rules created thanks to simulations with a modeled STM32. We will conclude this chapter with a highlight regarding the constraints added by the STM32, as it is a mass-market device, it must respect several constraints to be competitive on the market. For example, it must stay cheap and small, and the package pin distribution are restrained by the rule : The most IOs pins possible and the fewest supply pins possible. This implies that any solution found to limit the SSN effect and guarantee the STM32 robustness must fit in this restrained environment.

Chapter 2. Modeling and validation

1. Introduction

This chapter is focused on the principle of a model development for a complete system, which is defined by a die embedded in a package and implemented on a PCB (Printed Circuit Board). The development of this model opens a lot of research possibilities. Firstly, in simulation, it is possible to access specific points that would not be reachable in practice. For example, unless we have a specifically manufactured package, it is not possible to observe the power supply directly in the die or at ball level for a BGA or a CSP package when the package is welded on the board. Secondly, in simulation it is possible to evaluate different topologies faster than with a physical implementation that requires a manufacturing process. For example, the modification of a bypass capacitor value and placement that is simple in simulation but would require a new board design and manufacturing for a physical implementation. Thus, the aim of such a model is to be able to work only in simulation and to allow a wider range of research than with real measurements meanwhile saving time and money. With this model we can determine which parameters are the biggest contributors to the Simultaneous Switching Noise (SSN) effect and which parts of the die are the most sensitive to it. In addition to this, it is also possible to propose new solutions to limit the SSN effect and to improve microcontroller robustness. Of course, this model has to be developed with a particular attention regarding the choice of the parameters used for its development and the values extractions methodology. Moreover, an important part of the development is the model refinement thanks to a solid validation where measurements and simulations are compared. So, this chapter details the model development for an existing microcontroller based on specific standards provided by IEC (the International Electrotechnical Committee). It also details all the steps for this development, from the padding of the die to all the different connections of the board and encompassing the package connections. After that, a section is dedicated to the correlation procedure developed during this thesis.

2. The Integrated Circuit Emission Model (ICEM) standard

2.1. Standards provided by IEC organization

The IEC is an organization that publishes international standards from a global and neutral point of view. Standards published by IEC provide a conformity assessment for different subjects such as measurement specifications, devices, equipment, and components. These standards can be related to electrical and electronic domain such as for smart buildings, cyber security, semiconductors, medical equipment, [48]. The interesting ones for the SSN study are the ones which focus on the electromagnetic compliance. For this domain, we can find a lot of standards about different subjects such as measurement methodology with specific equipment or even standards to develop a model that can be used in simulation. The first document introduced here is the technical report IEC 62014-3 [49]. It defines the standard ICEM (Integrated Circuit Emission Model) which provides guidelines for an electrical model development. The ICEM standard is used when the purpose is to study the Electromagnetic Interference (EMI) behavior only by simulation for any electronic component. In other words, it provides general information for the purpose of establishing the model of an internal activity and its associated coupling mechanisms that can be implemented in different formats -IBIS, SPICE, ...-. The single approach of ICEM modeling can cover three different mechanisms listed below and summarized in Figure 2-1 [49] :

- The conducted emissions through supply lines. The EMI is a current peak which flows through power supply lines.
- The conducted emissions through IOs interfaces. Each PCB line connected to the output of an IO can act as an antenna. For this type of conducted emission the EMI is propagated by these antennas. [49]
- The radiated emissions of the IC. An electromagnetic field is created by the internal current that flows in a low impedance loop.

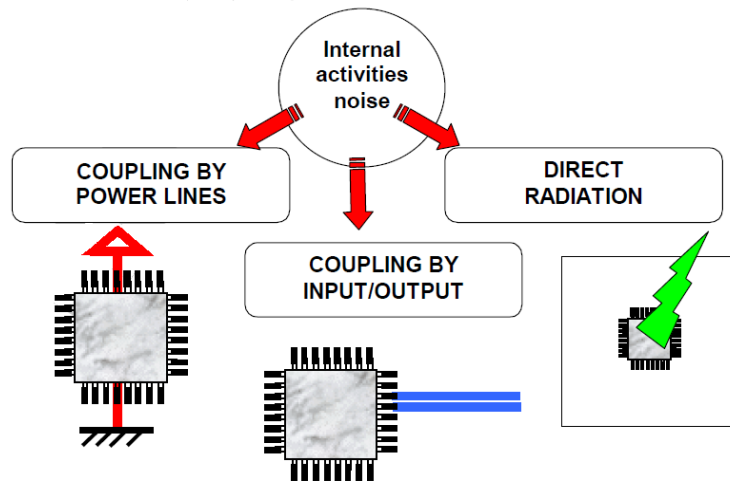


Figure 2-1: The three types of emissions defined by the standard IEC 62014 [49]

The SSN generated by the switching of an IO can be classified in the first point listed here which is the conducted emission through power supply lines. For conducted emission only, the standard 62433-2 [50] provides additional details to the ICEM with the ICEM-CE (Integrated Circuit Emission Model – Conducted Emission). IEC details this ICEM-CE as the standard that can be used for the EMI observation of conducted emission regarding an MCU soldered on a PCB. As it is explained in this document, a conducted emission can have two different origins which are reminded below [50]:

- Conducted emissions through power and ground lines
- Conducted emissions through IOs terminals

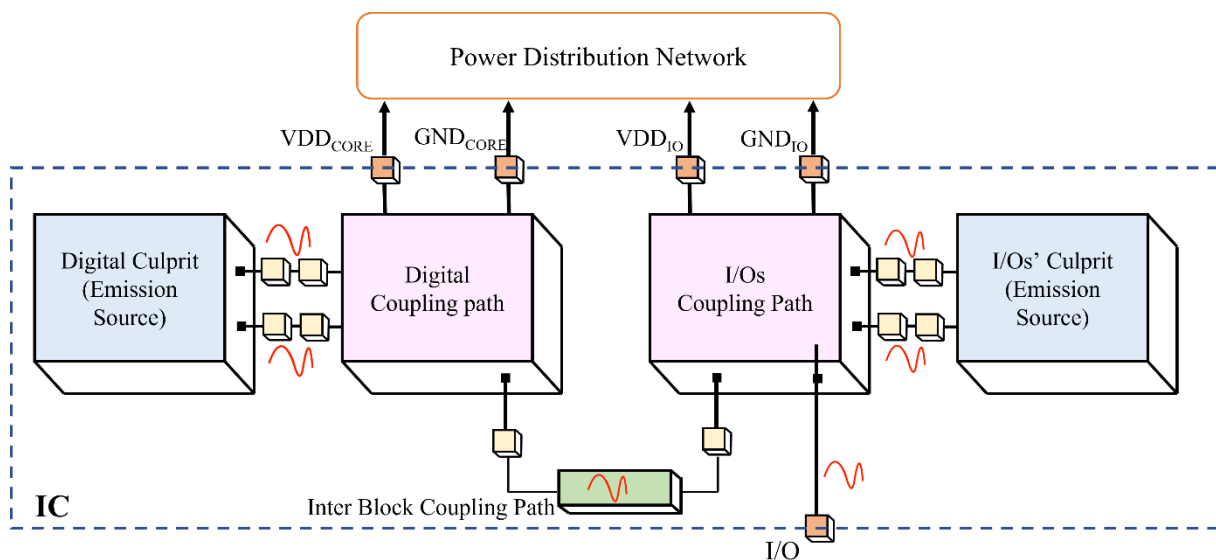


Figure 2-2: Example of Conducted Emission detailed by the standard IEC 62433-2

Figure 2-2 above extracted from the standard IEC 62433 [50] shows an example of the conducted emissions for an active Integrated Circuit (IC). As we can see, electromagnetic noise is created by any active switching devices which can be IOs or the core. The EMI is then propagated through a coupling path to external terminals defined by pins or pads. Coupling paths can be IOs lines but also the power distribution network (PDN). Finally, depending on the circuit definition and especially the PDN characteristics -including decoupling elements-, some of the EMI generated by the core can propagate to the IOs PDN through the Inter Block Coupling (IBC) Path.

2.2. ICEM-CE standard

The ICEM-CE model is defined in purpose to develop and write a model in order to study in simulation the IC behaviors in terms of EMC. Still extracted from the two cited standards the ICEM-CE splits any IC in five different blocks as listed below and illustrated in Figure 2-3 [49], [50].

The five different blocs are then:

- The Internal Activity (IA) which represents the noise generated by an active component of the IC. This block is modeled by an independent source of current or an independent source of voltage.
- The Internal Terminal (IT) models the connection between the IA block and another internal component of the integrated circuit.
- The PDN which represents the coupling path used for noise propagation. The PDN is modeled with passive components which are generally inductance, resistance, and capacitor. It is connected with IA through IT.
- The Inter-Block coupling (IBC) that models any coupling between two blocks is defined as an IBC. In the same way than the PDN, the IBC is modeled with passives components.
- The External Terminal (ET) represents the connection between the IC and an external component. For example, the connection between the ideal power supply and the IC's power supply is done with two ET -one for the power and one for the ground-.

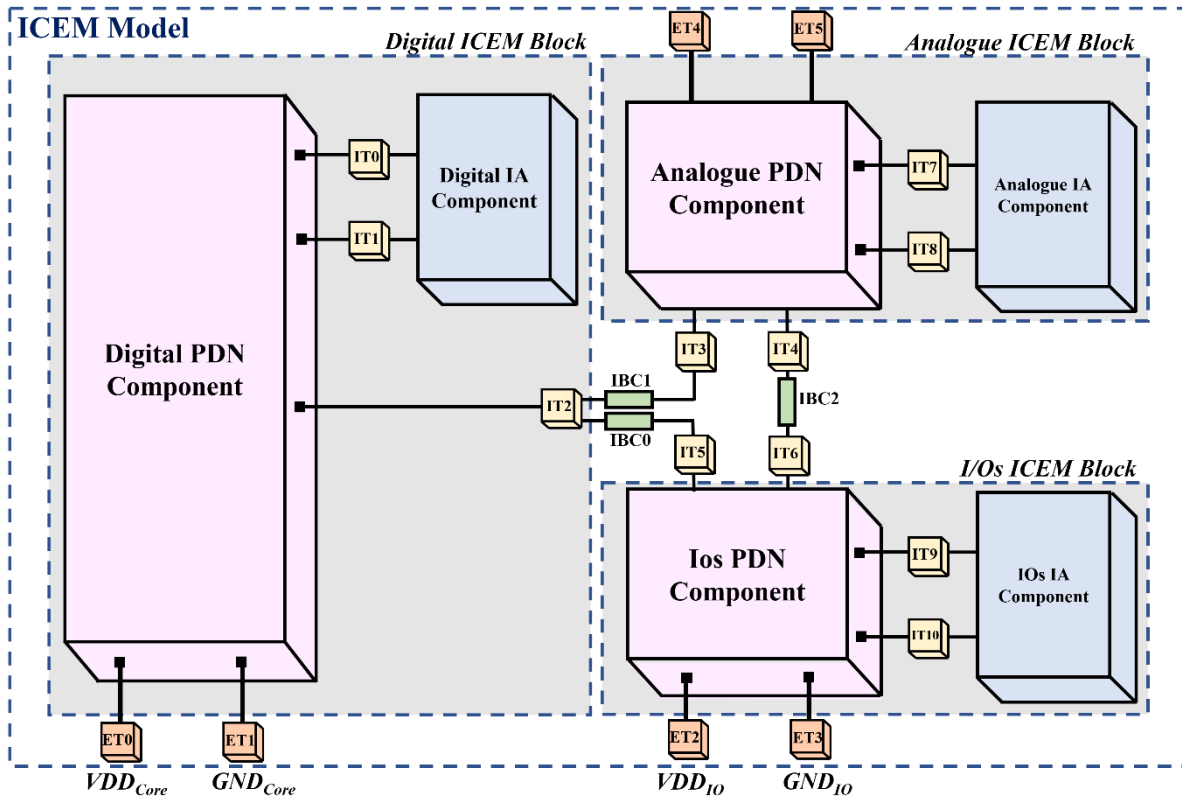


Figure 2-3: ICEM-CE schematic

To summarize, in order to study MCU behavior in terms of SSN effect, it is important to develop an accurate model based on these two standards. With the objective to write this model, based on the definition of the ICEM-CE, the next section will detail the model development step by step. Regarding the die, the model will be done only for the padding which is defined by all IOs of the MCU and their associated supplies. Because power supplies are generally dissociated in a MCU with appropriate decoupling, other blocks of the MCU like memory or the core are not included in this model in order to keep focus on the IOs and the SSN effect. After the analysis of the die, we will detail the model development to cover the connections created by the package and the board.

3. Model of an existing microcontroller

3.1. IO model

First of all, the modeling of the complete system can be started from the inside of the die with the IO description. This model is done in two steps with, on one hand the model of the design itself and on the other hand, the model of the IO's activity. For the IO design, it is

considered and modeled as a bypass capacitor and a resistance in parallel between the rail of V_{DDIO} and the rail of V_{SSIO} [2]. These capacitance and resistance are determined by the intrinsic characteristics of MOSFET transistors used in the design but also sometimes by a capacitor added by the designer himself. Figure 2-4 illustrates the model for an IO design.

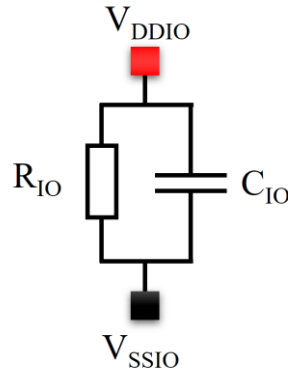


Figure 2-4 : IO's schematic model

For a better understanding of this model, a small-signal AC simulation can be done. This simulation shows the total impedance of an IO and demonstrates that its behavior is similar to a first order RC low-pass filter. An example of this simulation is shown in Figure 2-5. To be noted, the vertical axis defines the magnitude in decibel-Ohm ($\text{dB}\Omega$), to convert the value in Ohm, the Equation 2-1 must be used.

$$y [\text{dB}\Omega] = 20 * \log(x)$$

Equation 2-1: Conversion Ohm in decibel

$$x [\Omega] = 10^{\frac{y}{20}}$$

Equation 2-2: Conversion decibel in Ohm

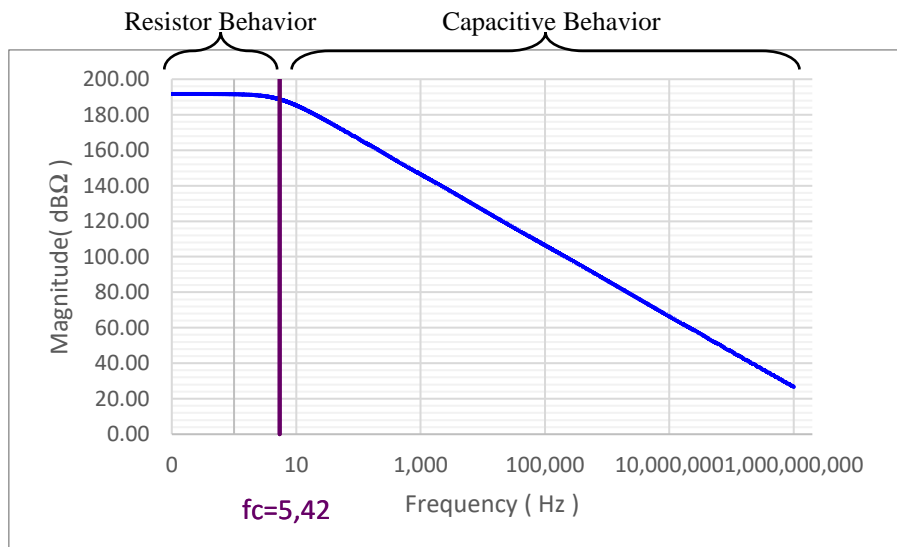


Figure 2-5: small-signal AC simulation showing an IO's impedance

Because the IO has a RC low pass filter behavior, the basic equations of this filter can be used to compute the resistance and the capacitance value with Equation 2-3 and Equation 2-4 [29]. In these equations, the first parameter GdB_{MAX} defines the maximum magnitude that can be found directly by simulation. The second parameter is the cut-off frequency f_c reached when the waveform is equal to GdB_{fc} -calculated using the Equation 2-5-.

$$R_{IO} = 10^{\frac{GdB_{MAX}}{20}}$$

Equation 2-3 : Formula for the inactive IO resistance model

$$C_{IO} = \frac{1}{2 * \pi * R * f_c}$$

Equation 2-4: Formula for the IO's capacitor model

$$GdB_{fc} = GdB_{MAX} - 3dB$$

Equation 2-5 : Magnitude calculation for cut-off frequency

With the example of Figure 2-5, the measured values on the waveform are $f_c = 5,42Hz$, $GdB_{max}=192dB$ and $Gdb_{fc}=189dB$. Then, the resistance and capacitor values are $R_{IO}=5G\Omega$ and $C_{IO} = 7,6pF$. We can note that the resistance is equal to 5 $G\Omega$. Most of the time, this resistance is always upper 1 $G\Omega$ minimum and in this case, it can be considered as an open circuitry which means, it is possible to remove the resistance of the model without modifying the IC behavior.

The second step to complete and finish this IO model, is to represent the IO activity. To remind an ICEM definition, the source of electromagnetic noise is modeled by the internal activity modeled by a current source or a voltage source. Based on the state of the art chapter, the IO can be considered as the source of the electromagnetic noise because it generates a current peak on power and ground supply lines at each IO's transition or switching. That is why, a source of current is added between the die's rail of V_{DDIO} and the die's rail of V_{SSIO} . For an active IO, this source will be equal to the di/dt generated by the switching IO. For an inactive IO, this source will simply be equal to 0. To determine the di/dt generated by an IO, the first possibility is to compute a slope calculation where ΔI and ΔT are extracted thanks to a transient simulation. Nevertheless, if the simulation is not possible the di/dt can be approximated as a basic triangle as depicted in Figure 2-6 where I_{MAX} and the Peak duration are computed with Equation 2-6, where C_{load} is the load capacitor value, V_{dd} the power supply and $T_{R/F}$ the IO rising or falling time and $T_{R/F}$ determines the peak duration. Of course, this solution is an approximation based on capacitor formula and simulations observation. This formula can be

used when absolutely no information is available from the design, as transistors size in order to calculate the trough current -cf. State of the art chapter-.

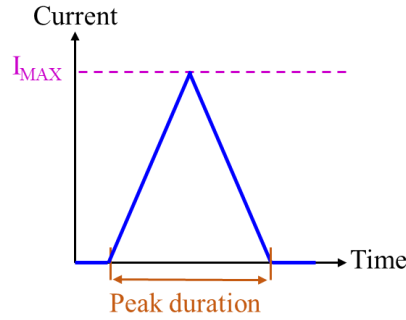


Figure 2-6: Current peak notation

$$I_{MAX} = \frac{2,4 * C_{load} * Vdd}{T_{R/F}}$$

Equation 2-6: Formula for the maximum current peak value

Then, the final IO model is obtained as represented in Figure 2-7 where there is the current source in parallel with the capacitance.

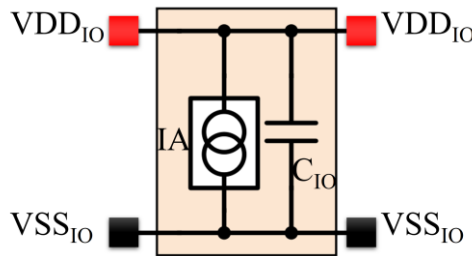


Figure 2-7: Final IO model

3.2. Die's power supplies line model

The next block to model regarding the die is its PDN. As the purpose is to study the SSN effect, the only PDN which is interesting for our model is the distribution of the Power and the Ground (P&G) used for IO's supply. Generally, this distribution is made with two rails -one for power and one for the ground- which are all around the MCU on different levels of metallic rails.

The ICEM standard details the PDN's model as a RLC circuit created by parasitic elements. In other words, the model of P&G rails of the die is defined by an inductance and a resistance in series for power and the same for the ground plus a capacitor which is connected between these two rails. The rationale for having a capacitor has already been explained with the IO model constitution. For the inductance and the resistance, their values can be defined

based on Vrignon's paper which provides equations 2-7 and 2-8 for calculation [29]. These equations use the rail characteristics and geometry. Most of the parameters defined in these equations can be directly extracted from the rail measurement as illustrated in Figure 2-8. For other parameters -such as square resistance- and as detailed under equations, this kind of information are directly provided by the manufacturer with the PDK (Process Design Kit). Finally, because the distribution of P&G is made on different levels of metal, the calculation has to be done for each level of metals and by considering the impedance parallelization.

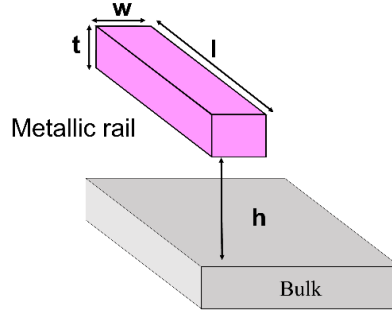


Figure 2-8: Die metallic rails geometry

$$R_{DIE} = R_{square} * \frac{l}{w} = \frac{\rho}{t} * \frac{l}{w}$$

Equation 2-7: Formula for parasitic resistance of a die's rail: R_{DIE}

$$L_{DIE} = \frac{\mu_0 * \mu_R}{2 * \pi} * l * \left[\ln \left(\frac{4 * h}{w} \right) + 1 \right]$$

Equation 2-8 : Formula for parasitic inductance of a die's rail: L_{DIE}

For these equations, parameters are defined as follow:

- R_{square} = Square resistance also named sheet resistance (per square). This is a measurement of resistance of thin film that is nominally uniform in thickness. This parameter depends on the metal characteristics $= \frac{\rho}{t} [\Omega/\square]$
- l = Length of the rail [m]
- w = Width of the rail [m]
- ρ = electrical resistivity of the material. $\rho_{Cu} = 1.72 \cdot 10^{-8}$ - $\rho_{Au} = 1.72 \cdot 10^{-8} [\Omega.m]$
- t = thickness of the rail [m]
- μ_0 = Constant of Vacuum permeability $= 4\pi \cdot 10^{-7} [H.m^{-1}]$
- μ_R = Relative permeability $= 1$ for Al, Cu, Air, Si $[H.m^{-1}]$
- h = rail's height from the bulk [m]

Finally, Figure 2-9 represents the equivalent model for one IO with its associate PDN where the IO can be active -Current source which generates the peak current & the bypass capacitor- or inactive -Current source equal to zero plus the same bypass capacitor-. In this model, the PDN of the die is represented by parasitic elements with the inductance and the resistance of the power and the ground.

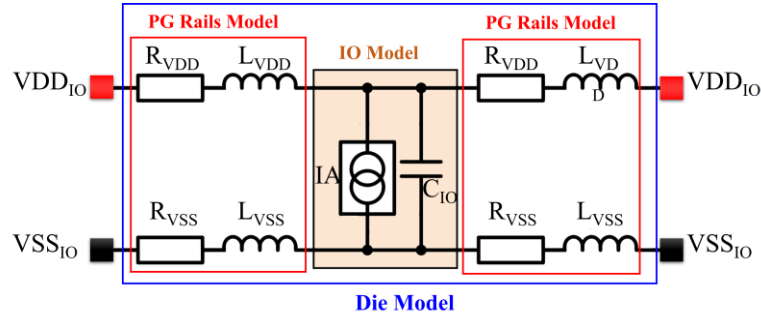


Figure 2-9: Die model with active/inactive IO and PDN

It is important to highlight that the illustration above represents only a part of the padding, as there is only one IO with its associated portion of supplies. Indeed, parasitic elements are brought by the characteristics of the metallic rails which means these parasites are distributed all around the padding almost uniformly. However, in order to be closer to the physical layout, it is preferable to define parasitic elements of the PDN per IO instead of one big value for the whole padding. In this way, each IO has its own parasites for P&G and it allows small values of resistance and inductance. Figure 2-10 depicts the final model of the padding with several IOs which can be active or not and their own parasitic elements for P&G rails.

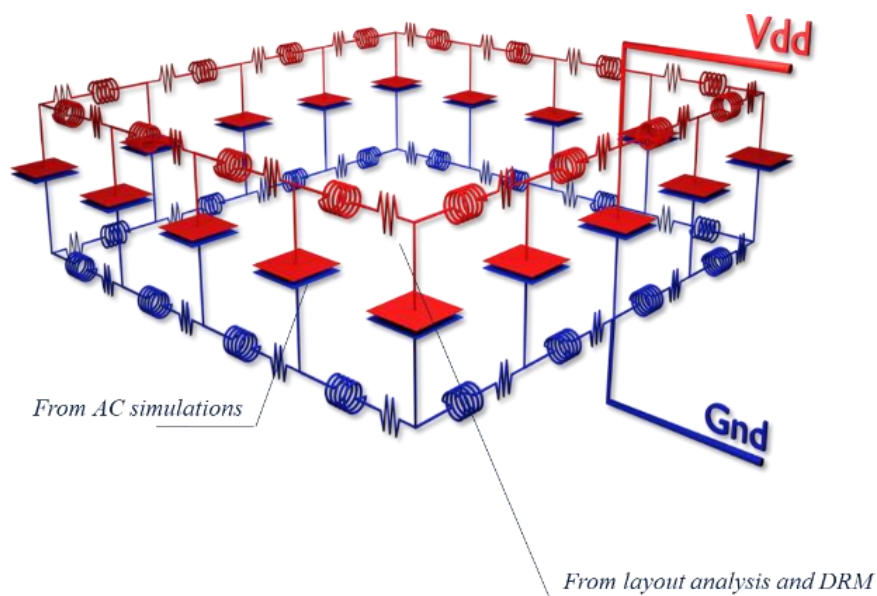


Figure 2-10: Representation of the die model

3.3. Package's PDN

Figure 2-11 shows an example of the connection for a QFP package. By analogy with the ICEM standard, there are ITs (Internal Terminals) that define the connections between each IO's pad and its associate bonding. Then, the PDN is defined by the addition of bonding and leadframe when the IBC (Inter Bloc Coupling) is the coupling between two close connections. Finally, the ET (External Terminal) is the welding of the leadframe on the PCB.

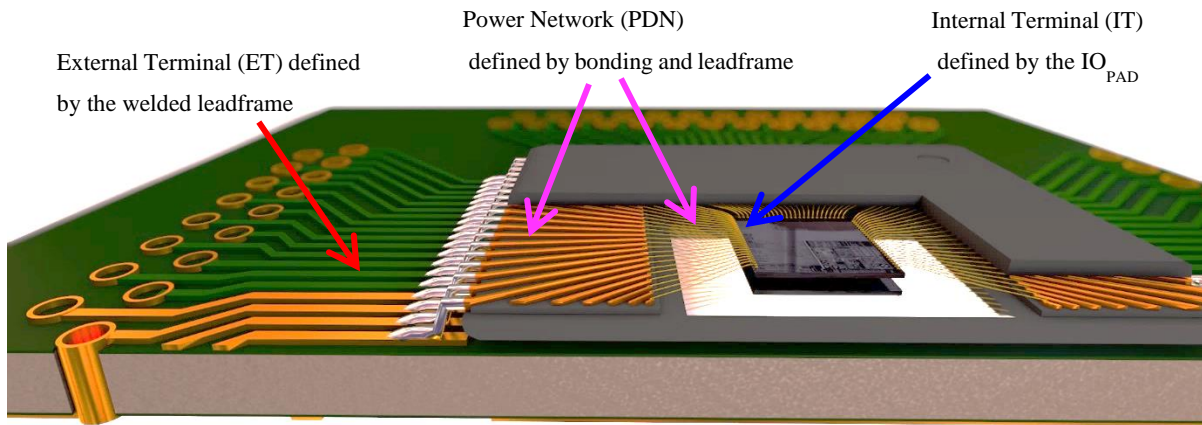


Figure 2-11: Sectional view of package welded on a board

Another interesting point from this Figure 2-11 is the difference of size between the die and the package. For example, with a die of $5 \times 5 \text{ mm}^2$, the size of a BGA package can reach more than $13 \times 13 \text{ mm}^2$ and a QFP more than $24 \times 24 \text{ mm}^2$. This difference of size can be explained by package constraints such as bonding length, separation distance between two bondings, cavity for the die, ect. Because of its size, the package is an important contributor to the SSN level due to the parasitic elements brought by the PDN connection [2] [29]. Indeed, in a basic point of view, we could consider a parasitic inductance of 1 nH/mm for bonding and for leadframe. With the example of a $24 \times 24 \text{ mm}^2$ QFP, the length of a wire bonding is around 3.5 mm when the length of a lead frame is equal to 9 mm which represents a total of 12.5 nH of parasitic inductance added by connection for this package. This example demonstrates the package's influence on the parasitic values of the PDN.

The purpose here is to establish the model of the entire package still by following the ICEM-CE. This model needs to include the RLC passive components for each connection from the IT to the ET. In other words, the bonding and the lead frame have to be modeled. For that, two methodologies exist, both of them are presented in the following subsections.

3.3.1. Hand calculation of PDN package

The first methodology for parameters extraction is by hand calculation of the RLC value. In other words, the parasitic values will be extracted by applying equations based on package geometry. For bonding model, equations of inductance and resistance are defined for round wire with Equations 2-9 and 2-10 [29], [41], [51]. Finally, Equation 2-11 is used to calculate the mutual inductance and equations 2-12 and 2-13 are used for the two different capacitance calculations [5], [41]. Parameters needed for these equations are defined below and are also schematized in Figure 2-12.

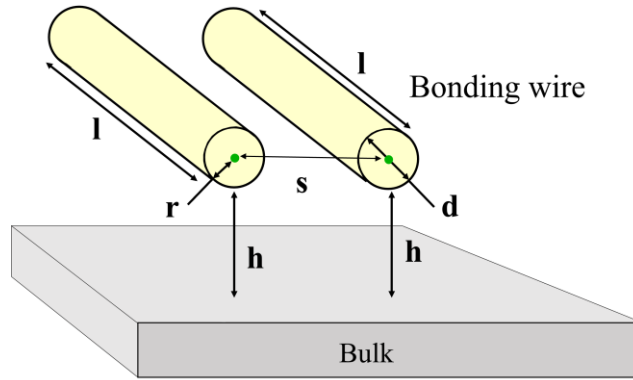


Figure 2-12: Schema of bonding wire and associated parameter

$$L_{\text{BONDING}} = \frac{\mu_0 * \mu_R}{2 * \pi} * l * \ln \left(4 * \frac{h}{d} \right)$$

Equation 2-9: Formula for parasite inductance of a bonding: L_{BOND}

$$R_{\text{BONDING}} = \frac{\rho * 4 * l}{\pi * d^2}$$

Equation 2-10: Formula for parasite resistance of a bonding: R_{BOND}

$$M_{\text{BOND}} = 5 * d \left[\ln \left(\frac{2(l_1 + l_2)}{s} \right) - 1 + \frac{s}{2 * (l_1 + l_2)} * \left(\frac{s}{2} * (l_1 + l_2) \right)^2 \right] = \frac{K}{\sqrt{L_1 * L_2}}$$

Equation 2-11: Formula of the mutual inductance between two bonding: K_{BOND}

$$C_{\text{BOND/BULK}} = \frac{2 * \pi * \epsilon_0 * \epsilon_r}{\ln \left(\frac{2 * h}{r} \right)}$$

Equation 2-12: Formula of the capacitance between a bonding and the bulk: $C_{\text{BOND/BULK}}$

$$C_{\text{BOND1/BOND2}} = \frac{\pi * \epsilon_0 * \epsilon_r}{\ln \left(\frac{s}{2 * r} + \sqrt{1 - \left(\frac{2 * r}{s} \right)^2} \right)}$$

Equation 2-13: Formula of the capacitance between two bonding: $C_{\text{BOND1/BOND2}}$

Where,

- l = Length of the bonding [m] (l_1 / l_2 Respectively the length of bonding 1 and bonding 2 for mutual calculation)
- d = Bonding's diameter [m]
- h = Height of the bonding from the bulk [m]
- ρ = electrical resistivity of the material. $\rho_{Cu} = 1.72 \cdot 10^{-8}$ - $\rho_{Au} = 1.72 \cdot 10^{-8}$ [$\Omega \cdot m$]
- μ_0 = Constant of Vacuum permeability = $4\pi \cdot 10^{-7}$ [$H \cdot m^{-1}$]
- μ_R = Relative permeability = 1 for Al, Cu, Air, Si [$H \cdot m^{-1}$]
- r = Bonding's radius [m]
- s = distance between the two bonding (from the center of each bonding) [m]

Because leadframe and bonding don't have the same geometry, equations are not the same regarding parasite calculations. For a leadframe, the value of parasitic inductance and resistance can be defined by calculation with Equations 2-14 and 2-15 based on the thesis of M. Leca [2]. The Equation 2-16 allows calculation of the parasitic capacitance which appears between a leadframe and the ground where the Equation 2-17 is used to calculate the parasitic capacitor value between two lines [5], [52]. Finally, the Equation 2-18 gives the possibility to calculate the mutual inductance between two different leadframe which also provide K , the coefficient of magnetic coupling between the conductor 1 and 2. Most of the equations parameters which are defined here can be measured directly on the leadframe geometry as depicted in Figure 2-13.

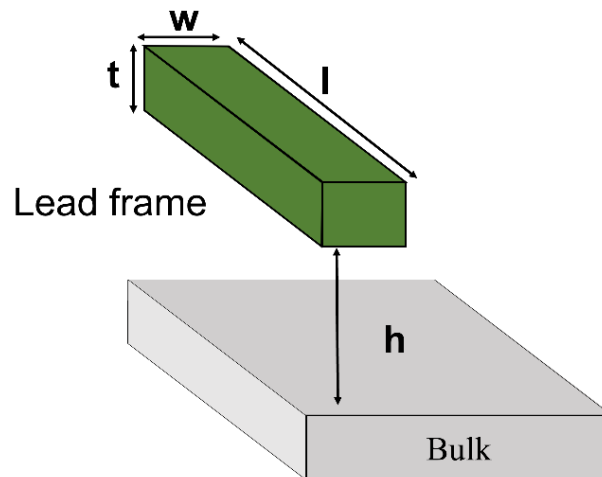


Figure 2-13: Lead frame and bonding geometry

$$L_{\text{LEAD FRAME}} = \frac{\mu_0 * \mu_R}{2 * \pi} * l * \left[\ln \left(\frac{2 * l}{w * t} \right) + 0.5 + \frac{0.447(w + t)}{2 * l} \right]$$

Equation 2-14: Formula for parasite inductance of a lead frame: L_{LEAD}

$$R_{\text{LEAD FRAME}} = \frac{\rho}{t} * \frac{l}{w} = R_{\text{SQUARE}} * \frac{l}{w}$$

Equation 2-15: Formula for parasite inductance of a lead frame: R_{LEAD}

$$C_{\text{BULK}} = \epsilon_0 * \epsilon_R * \left\{ 1 * 1.10 * \frac{w}{h} + 0.79 \left(\frac{w}{h} \right)^{0.1} + 0.59 \left(\frac{e}{h} \right)^{0.53} + \left[0.52 \left(\frac{w}{h} \right)^{0.01} + 0.46 \left(\frac{t}{h} \right)^{0.17} \right] * \left[1 - 0.87e^{-\frac{d}{h}} \right] \right\}$$

Equation 2-16: Formula for parasite capacitance between a lead frame and the bulk: $C_{\text{LEAD/BULK}}$

$$C_{\text{COUPLING}} = \epsilon_0 * \epsilon_R * l * \left\{ \frac{e}{d} + 1.21 \left(\frac{t}{h} \right)^{0.1} * \left(\frac{d}{h} + 1.15 \right)^{-2.22} + 0.25 * \ln \left(1 + 7.17 \frac{w}{d} \right) * \left(\frac{d}{h} + 0.45 \right)^{-0.64} \right\}$$

Equation 2-17: Formula for parasite capacitance between two leads: $C_{\text{LEAD1/LEAD2}}$

$$M = \frac{\mu_0 * \mu_R}{2 * \pi} * l * \left[\ln \left(\frac{2 * l}{w + e} \right) - 1 \right] = \frac{K}{\sqrt{L_1 * L_2}}$$

Equation 2-18: Formula for the Mutual inductance between two leads: $K_{\text{LEAD1/LEAD2}}$

Where,

- R_{SQUARE} = Square resistance depends on the metal characteristics = $\frac{\rho}{t}$ [Ω/\square]
- l = Length of the lead frame/bonding [m]
- w = Width of the lead frame [m]
- t = Thickness of the lead frame [m]
- d = Bonding's diameter [m]
- h = Height of the lead frame/bonding from the bulk [m]
- ρ = electrical resistivity of the material. $\rho_{\text{Cu}} = 1.72 \cdot 10^{-8}$ - $\rho_{\text{Au}} = 1.72 \cdot 10^{-8}$ [$\Omega.m$]
- μ_0 = Constant of Vacuum permeability = $4\pi \cdot 10^{-7}$ [$H.m^{-1}$]
- μ_R = Relative permeability = 1 for Al, Cu, Air, Si [$H.m^{-1}$]

At the end and after formula computation, the model of the package can be schematized as depicted in Figure 2-14 with parasitic inductance and resistance of bonding and lead frame as well as the different capacitors and the coefficient of coupling K .

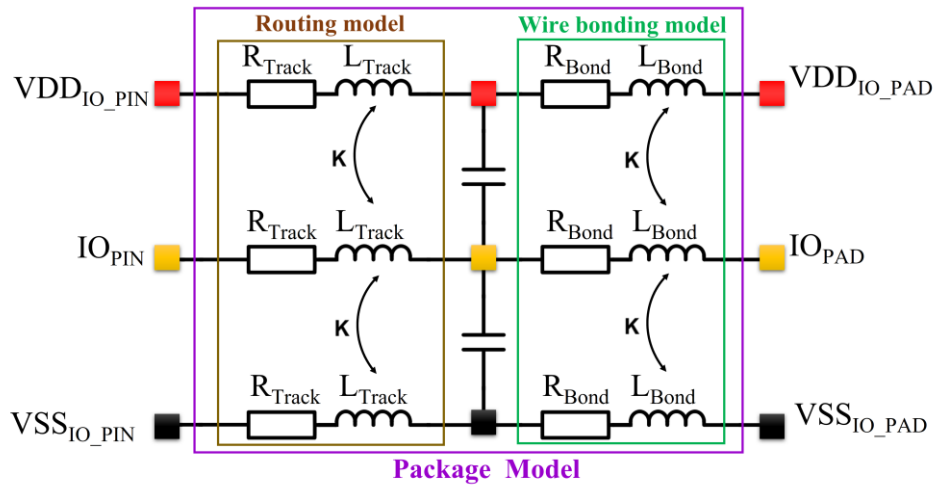


Figure 2-14: Model of the package overview

It is to be noted that, this method is a first order approximation, that allows anyone to develop a package model quite quickly. However, as it is a first order, it is not the most accurate compared to the second method that uses specific software. This second method is introduced in the next subsection.

3.3.2. PDN's extraction by software

The second method for the development of the model consists of using the commercial software AnsysTM tools and more particularly Ansys SiwaveTM [53]. First of all, Siwave imports and converts a layout design from almost any design tools (Redhawk, Totem, Altium, Candence Layout, ...). This import will include all different types of vias, routing, bonding, plane, ect but also all layers of the package with their physical characteristics. Once the layout exportation is done, Siwave allows many possibilities perform such as EMC analysis with Far/Near fields calculation, electromigration analysis, the generation of IBIS model, the extraction of broadband S-parameter model, This S-parameter model is the one used for the PDN's extraction. It is obtained by using MoM and FEM methods (Method of Moments and Finite Elements Methods) as illustrated in Figure 2-15 [54].

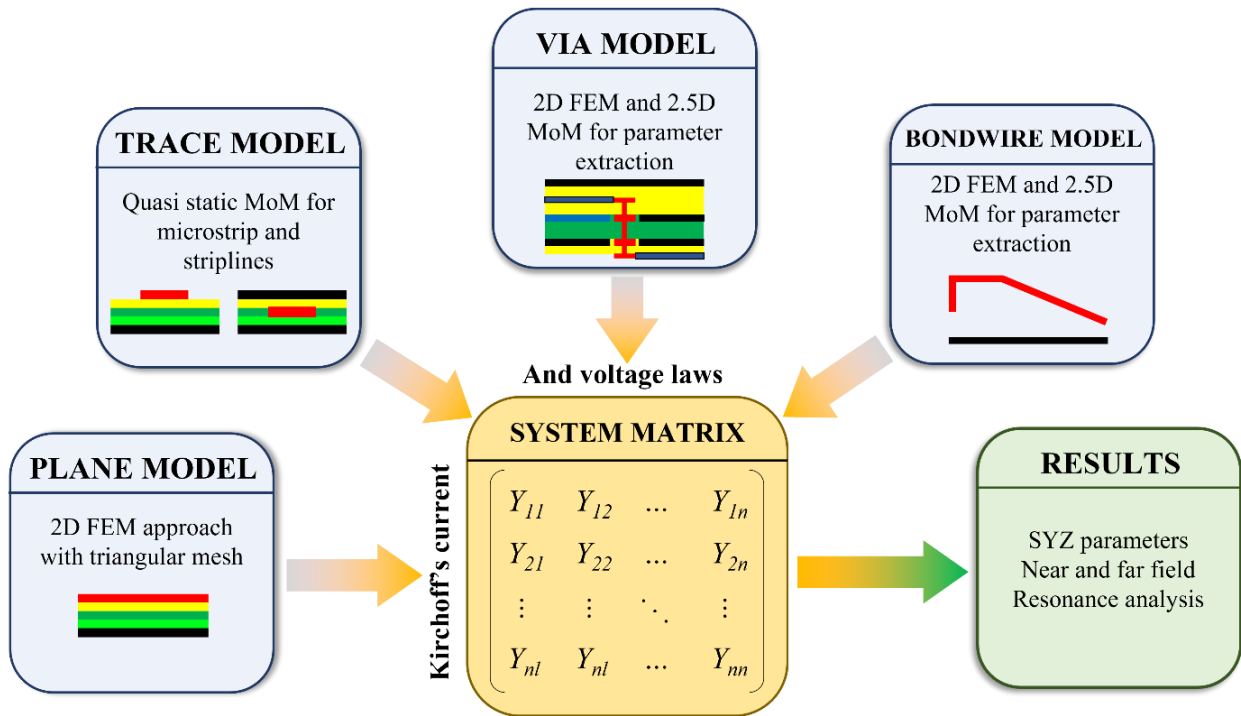


Figure 2-15: SIwave solver workflow

This software offers two possibilities for the extraction of the package's model. The first one is the extraction of the S-parameter model. It is a broadband model which defines the entire package with all parasitic components including all coupling factors. The advantage of this model is that it is accurate at each frequency of work including DC but, the simulation time will be adversely impacted. The second one is the extraction of an RLC netlist. This is a spice netlist, still for the entire package, which include all passive parasites as well as mutual terms, extracted at a specific frequency of work for the purpose of taking into account skin effect. This second method has the advantage that it is faster for simulation, but it will be less accurate than the S-parameter method because the extraction is done at a given frequency [55].

This second method for the development of the package model is more complex and more accurate than the first one. Of course, with the calculation method some approximations are generally done. For example, the calculation is done for one or two bonding or leadframes and the same value is used all around the package but, this value can change by more than 20% depending if it is calculated in the middle of the package or in a corner [29]. By doing the extraction with AnsysTM a complete model is obtained but, the set-up of the software can be really complex. It is also important to note that similar and free software developed by Etienne Sicard is available [56]. Finally, Figure 2-16 schematizes the model obtained by software extraction.

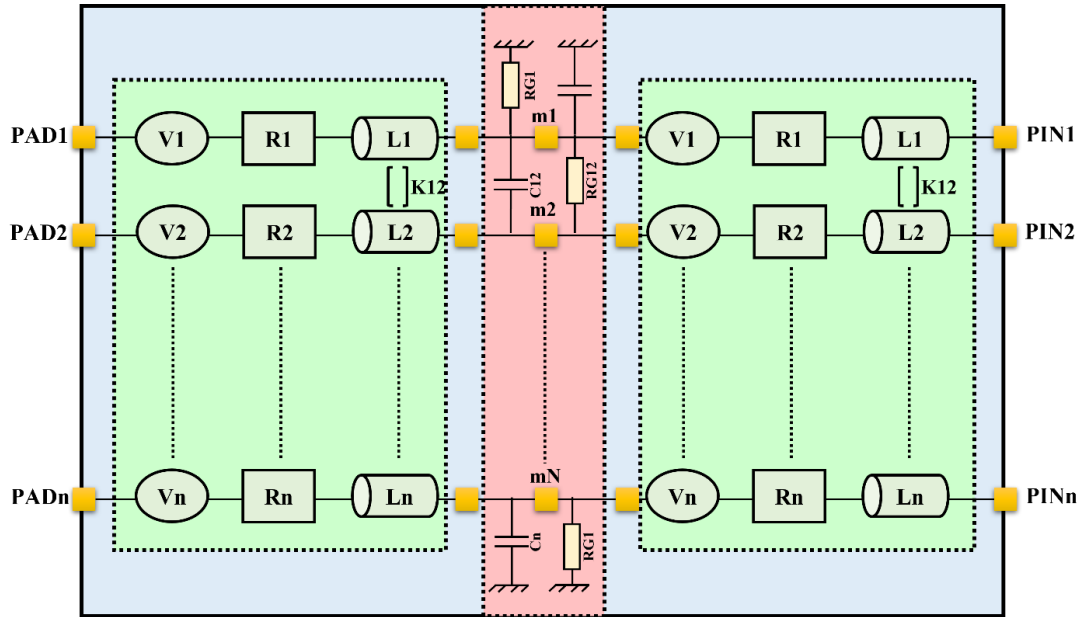


Figure 2-16: Model of the package and parameters extraction using Siwave™

3.4. PCB model

For a PCB model development, the methodology is virtually the same as for package. In other words, a PCB can be calculated by hand with formulas based on the geometry or it can be extracted by software using the Ansys™ framework. Figure 2-17 provides a schematization of a PDN model for a PCB.

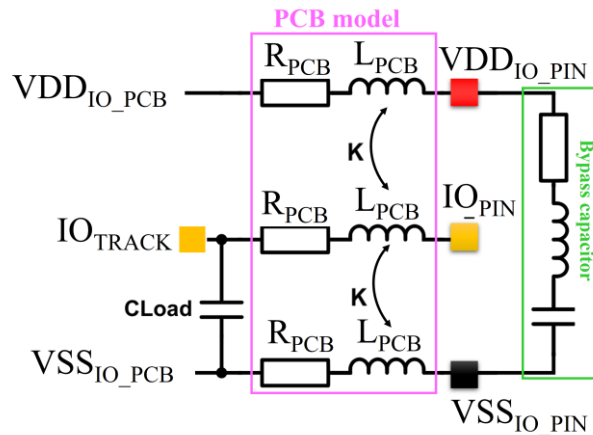


Figure 2-17: Model of PCB to create

A PCB is a more complex circuit than a package. Whereas a package generally includes only bonding and leadframe in an almost uniform distribution -ex: leadframe and bonding are distributed uniformly all around the MCU with a difference around 20% between the smaller and the longer one- this is not the case with a PCB. A PCB can be small with only few connections, but it can also be really complex with different planes for power and ground,

different types and numbers of vias, different lengths and types of connections, ect. As a matter of fact, it is up to the designer to determine where the model can be approximated in function of the parameters observed. The example of a board named Discovery board, designed by STMicroelectronics, can be used. This board embeds a lot of communication connections as an USB-C, an LCD driver, memories, an ethernet connection, ect. Generally, all of these communications are not used at the same time, which means, it is up to the designer to erase all unused communications -including all the connections between the MCU and the communication connector-.

3.4.1. Hand calculation of the PCB model

To perform a hand calculation of the PCB model, package formulas can be reused for the PCB's lines. However, in order to have an accurate model, some points need to be added:

- Model of a plane (especially for power and ground).
- Model of a via (especially for vias which are used for bypass capacitor connection).
- Mutual inductance: Between IO trace and ground plane and between two close vias.
- Model of a by-pass capacitor.

For the bypass capacitor, RLC models are generally provided on the website of the capacitor manufacturer for any capacitor sizes and values. Then, the connection between these by-pass capacitors and the external package connection has to be modeled. Generally, this connection includes a via plus a routing for the capacitor welding. To be as accurate as possible, the model is done as following: two vias -one for the ground connection and one for the power connection- including the coupling factor between these two vias plus the capacitor routing and finally the capacitor itself. This model is illustrated in Figure 2-18 for a better understanding.

6 Layers PCB

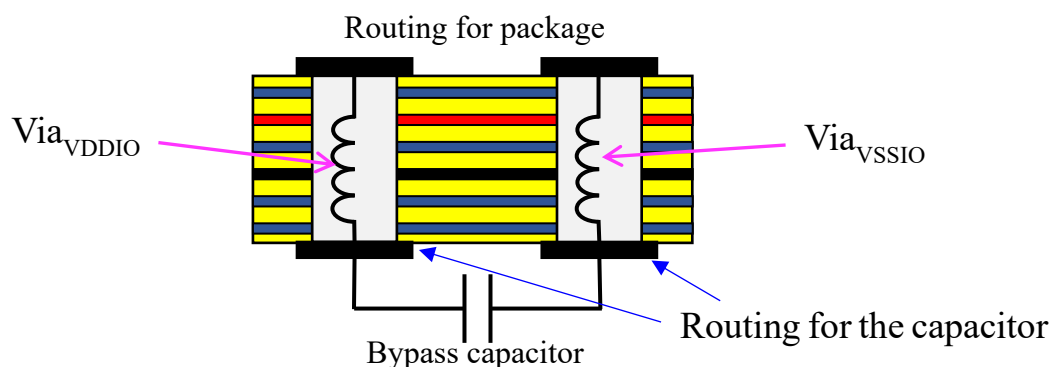


Figure 2-18: Model of two vias with a bypass capacitor

Then, Equations 2-19 and 2-20 are used to compute the via inductance and resistance from the work of Goldfarb and Pucel [57] with h the height, r the radius, t the thickness, μ_0 the free-space permeability and σ the metal conductivity. It is also possible to find a calculator on the internet for via parameter extraction [58]. Finally, in order to determine the mutual inductance between two vias, the Equation 2-11 can be reused -equation for mutual inductance between two bonding-.

$$L_{VIA} = \frac{\mu_0}{2 * \pi} \left[h * \ln \left(\frac{h + \sqrt{(r^2 + h^2)}}{r} \right) + \frac{3}{2} * \left(r - \sqrt{(r^2 + h^2)} \right) \right]$$

Equation 2-19: Formula for via's parasitic inductance

$$R_{VIA} = R_{dc} \sqrt{1 + \frac{f}{f_\delta}}$$

Equation 2-20: Formula for via's parasitic resistance

$$f_\delta = \frac{1}{\pi * \mu_0 * \sigma * t^2}$$

Equation 2-21: f_δ definition for the via resistance

For a plane model, this is a more complex problematic. Many books and articles propose different methods and points of view for plane impedance extraction. As this is a first order model, we will represent the model of a plane as an impedance per square in function of the frequency defined by Equation 2-22 [5]. In reality, a plane modeling is more complex as, this formula is for an ideal plane without any hole due to vias or any splits due to different traces. If the plane has too many slots, another approach needs to be considered such as modeling with π -method [59].

$$R = \begin{cases} \frac{\rho}{e} & \text{in DC} \\ \frac{\rho}{e} * \sqrt{f} & \text{in AC} \end{cases}$$

Equation 2-22: Impedance of a plane

3.4.2. PCB modeling by software

Where the model by hand is more complex for PCB than for package, this is not the case for the model developed by software. The same methodology can be used here through

Ansys SiwaveTM. Moreover, the model constituted by software has additional advantages in this case. The first one is the possibility, in an easy way, to erase all components and connections that are not useful for the model. The second one is the possibility to import in the same project the board and the package from two different data bases for the purpose of working on a single circuit. Indeed, the software can recreate the solder connection between the package and the board based on the package footprint in a really quick and easy way. Finally, if the package and the PCB are in a same project, the extraction can be done directly from the die pad to the external terminal of the board which means that potential coupling between package and board will be taken into account. The only drawback of this method is the time of setup and simulations. Because the board merges different types of traces and planes, the setup of the extraction has to be done with a particular attention. Also because of all coupling calculation the extraction could take more than a week. That is why it is up to the designer to define which parameters are useful for his work of modeling.

3.5. Final model for simulation

In the former sections, we have explained the different steps to model a complete system; in particular the methodology to model the die -IOs and the distribution of their power supplies-, the associated package and the board. In comparison with the ICEM-CE model, we have modeled the complete system with the internal activity, PDN and IBC but also by identifying Internal/External Terminals. This resulting model is summarized in Figure 2-19.

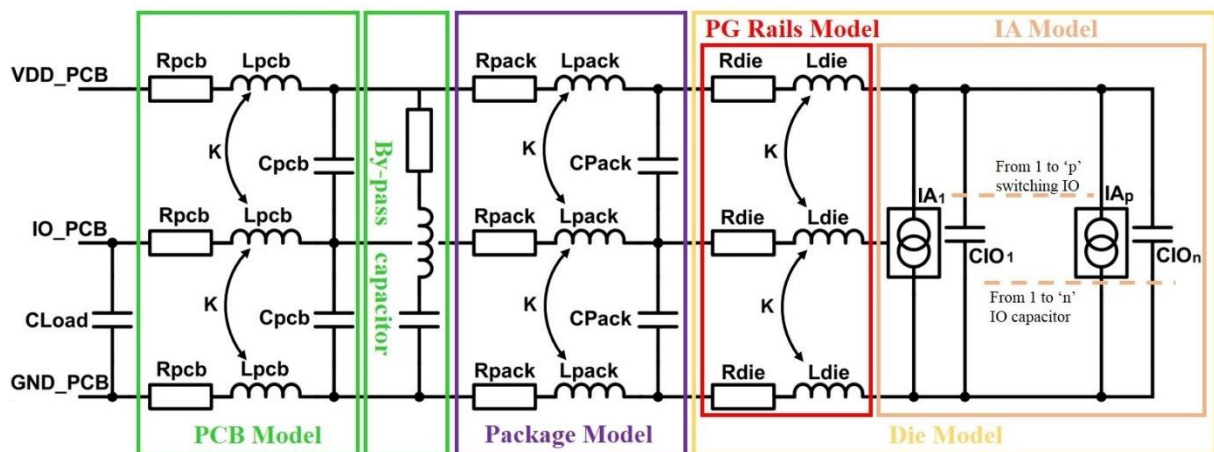


Figure 2-19: ICEM-CE modeling of a complete system

Once all of these steps are done, the final model will be implemented in Cadence Software by the merge of different spice netlists in a simulation file. Figure 2-20 represents this final model obtained for simulation. Concerning the die model there is on one hand, IO that can be ON or OFF and, on the other hand, rails' PDN. Then, each of them is connected to the PDN of the package which is then connected to PDN of the PCB. Package and PCB model include all couplings and capacitors.

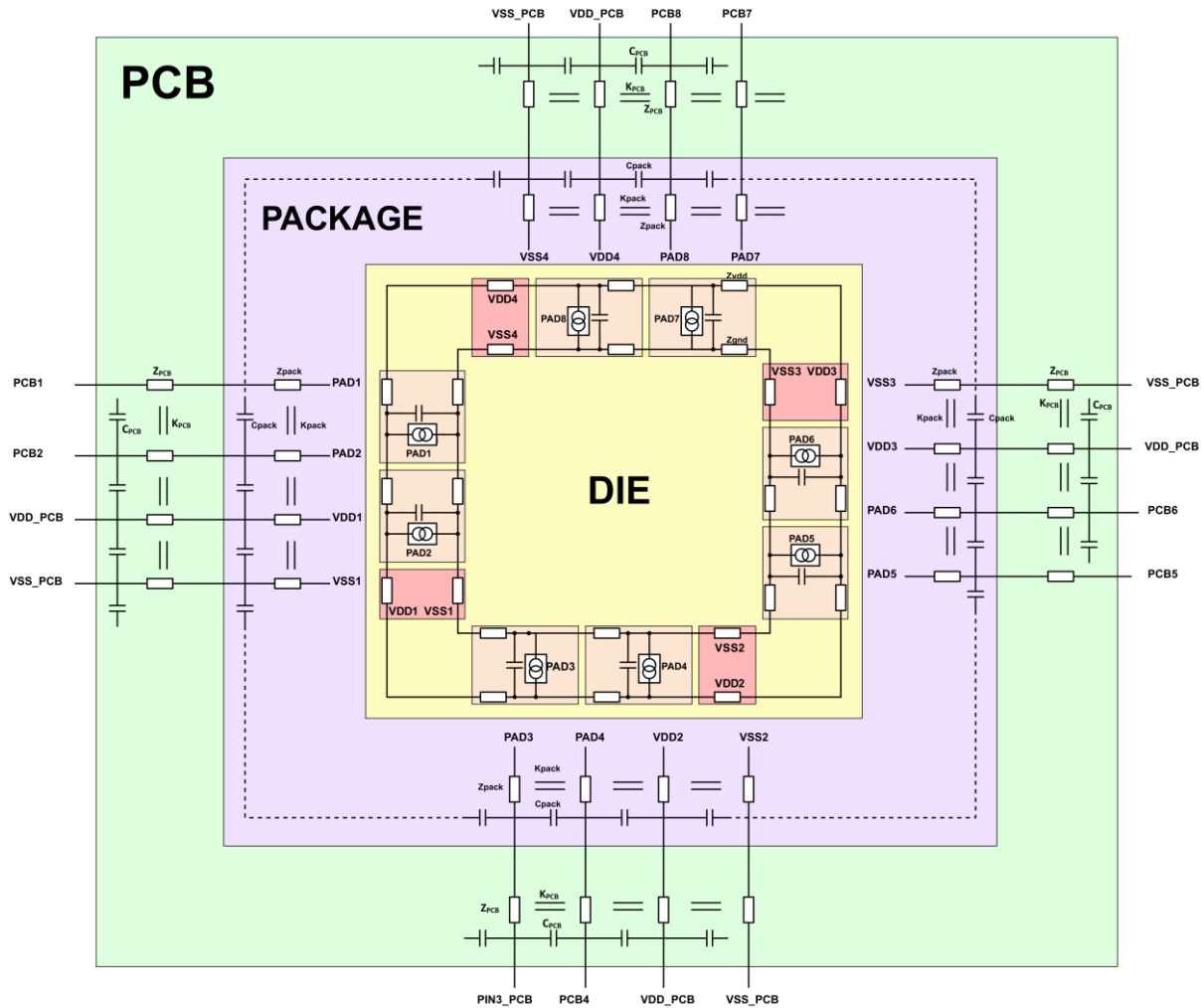


Figure 2-20: Representation of a final model obtained for simulation

Before moving on to the next steps of validation and refinement of the model, there is a last point to evoke. Here, we detailed the system modelling based on the ICEM standard. Nevertheless, other modelling principles exist. Most known might be the three below :

- The IBIS (Input/Output Buffer Information Specification) was developed by Intel in the 90s [60]. It is defined by an ASCII file used to describe the IO behavior which reduces a lot the time simulation. Nevertheless, the IBIS standard is more focused on signal

integrity and does not take into account the influence of the internal activity on the power supply and then, the repercussion this will have on the IO behavior.

- The IMIC (Input/Output model for Integrated Circuit) was developed in 2001 by the Japan Electronics and Information Technology Industries Association (JEITA) [61]. It is similar to the IBIS standard but defined with a SPICE format with tabulated transistor models in order to hide the technology used. It also overcomes some IBIS drawbacks. For example, the RLC network can be added to the power supply.
- The LECCS (Linear Equivalent Circuit and a Current Source model) was developed by the Osaka University in Japan in 2004 [62]. This standard is the closest to the ICEM standard but it was developed to study RF products and therefore allows modeling only in the frequency domain.

In order to not complicate the reading of this manuscript, these three standards are only cited and introduced here. However, more information can be found in M. Vrignon thesis [29] or M. Sicard book [5]. The final choice for the model development was to use the ICEM standard because it is the one that takes into account both signal and power integrity. Moreover, it is also the only one which permits to study the Internal Activity impact on the power supply as well as the IO's behavior face to this disturbance.

4. Model validation

In this chapter II we have detailed all steps needed to go through a model development of an existing microcontroller based on the ICEM-CE. The aim of such a model is to be able to study a complete system -a die with its associated package and PCB- regarding the SSN effect. Before going through this phase of research it is important to validate the developed model and, if necessary, to refine parameter's values. This validation step is necessary to ensure that what it is seen in simulation is as close as possible of the real MCU's behavior especially in terms of SSN. This section will details the correlation procedure established to validate this model. For a better understanding, the first Device Under Test (DUT) used for the definition of the correlation procedure will be briefly explained in the next subsection. Then the subsequent sections will detail a methodology of comparison for power and signal observations. Finally, we will give some axes of research to modify the model should it appear not to be well correlated with measurement.

4.1. Device under Test

With the purpose of a better understanding of the validation procedure, the first thing introduced here is the first Device Under Test (DUT) used for the model development and validation. This DUT was one of the biggest 32 bit microcontroller (STM32) designed by STMicroelectronics. The die is composed of 324 IOs distributed on the padding, and the package has 448 balls. As a matter of fact, the number of balls is bigger than the die's IOs because of other signals (balls for the core, for the different power and ground supplies, ...). This package BGA 448 was chosen because it is the biggest one for this die, smaller packages also exist where some IOs are not connected. Regarding package's power connections, on one hand there are 35 V_{DDIO} -IOs' power supply- and 49 V_{SS} - MCU's general ground- that defines the power connection between the die and the package. On the other hand, there are 7 balls of V_{DDIO} and 54 balls of V_{SS} to establish the supply connections between the package and the PCB. Finally, the board was a generic board as visible in Figure 2-21. This kind of board is also produced by STMicroelectronics and, as shown in the board's picture in Figure 2-21, it allows a lot of measurement possibilities. Indeed, there are three lines of connectors on each side of the board. Two different lines for ground and power propagation from the external sources, one line for the power propagation also from the external source and one line for all MCU's connection. In other words, it is possible to connect any component (as a capacitor or a probe) between an IO's output and the ideal ground or the ideal power. Finally, the board includes 10 by-pass capacitors 0402 of 1 μ F soldered under the board. The only drawback of a generic board is its size which involves a really important parasitic resistance and inductance for all connections. Indeed, a line (from package to external plot) is defined with $L_{TRACK}=50\text{nH}$ and $R_{TRACK}=1,5\Omega$. Also, in addition to this, all measurements were done with a 500MHz Band Width oscilloscope and passives probes ($C_{probe}=8\text{pF}$, $R_{probe}=10\text{M}\Omega$).

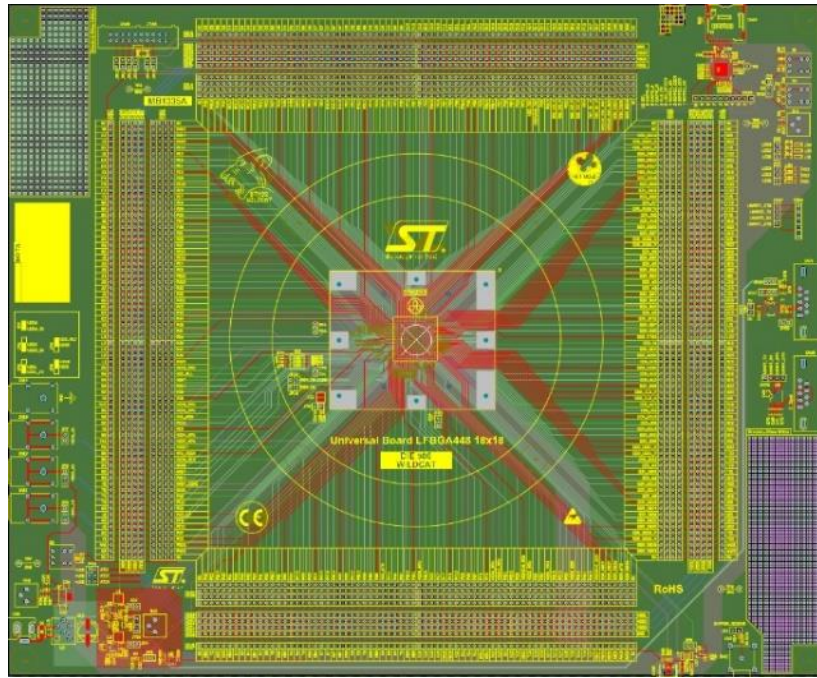


Figure 2-21: Picture of the discovery board designed by STMicroelectronics

The testbench used for validation needs to explore different tests in order to cover all possibilities. For that, several parameters need to be changed and, each time, observations regarding power and signal needs to be done for the correlation. Below all parameters modified during measurement are listed. Obviously, only one parameter can be changed at a time in order to be accurate.

- Load capacitor value connected to IO's output: 0nF, 5nF, 20pF.
- Number of simultaneous switching IOs: 1IOs, 2IOs, 4IOs, 8IOs, 16IOs, ...
- Position of this switching IOs versus P&Gs: Close as possible to the ideal power vs as far as possible.
- Position of switching IOs versus others IOs: All grouped in the same location vs distributed to the maximum on the boards.
- IOs speeds: IOs are always designed with 4 possible speeds. The di/dt -the current peak generated by the switch- is defined by the design and will grow proportionally to the IO's speeds.

As a matter of fact, in the test cases listed here, all of the possibilities can not be applied because of the board design, as this is the case with the generic board used for this validation development and introduced in the DUT section. Nevertheless, it is up to the designer to do as many of these tests as possible depending on the board possibilities.

4.2. Power observation for power integrity measurement

The power integrity (PI) represents the management of the power quality for the purpose of always having a consistent voltage level seen by the die. Here, the objective is to validate the power and ground behavior of the model thanks to a comparison with measurement and this by the application of possible testcases cited previously.

For the correlation on power observation, specific points have been determined for the comparisons. These points are:

- Oscillation of the first ringing frequency
- The first oscillation amplitude

These measurements will be done on the power and ground lines when IOs are switching with the distinction of rising and falling edge. Another point to mention regards the ground plane of the board if it is properly designed then the SSN effects may not be measurable on the external pins/connectors. In that case, one solution could be to set an IO to a logical and continuous '0' as close as possible to the other switching IOs. By doing this, the IO's output will reflect the die's ground but slightly filtered by the IO design. Nevertheless, this setup of the IO can also be applied in simulation so the comparison could still be done. Otherwise, it is possible to stay focused only on power line. Figure 2-22 here gives an example of the correlation observation for the DUT's power lines. In this comparison, there are 16 SSO (simultaneous switching IOs). Table 2-1 represents the associated value for the comparison.

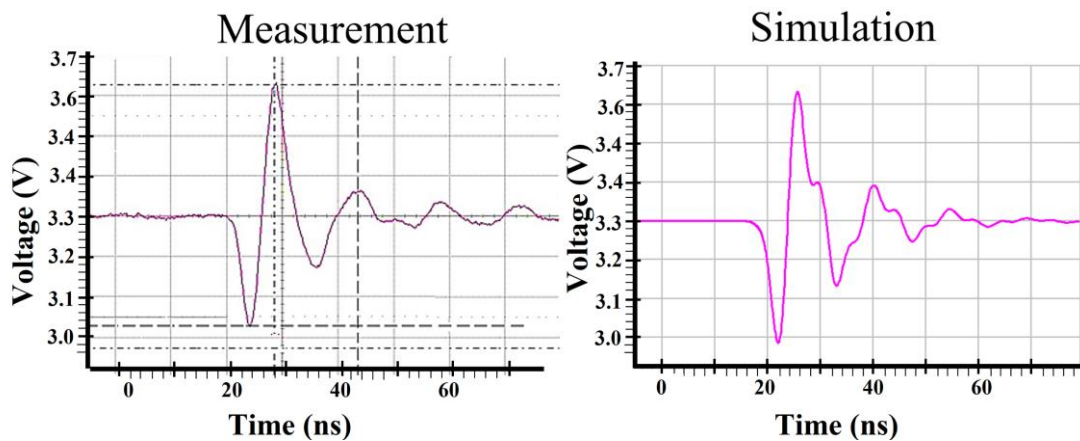


Figure 2-22: Comparison measurement vs simulation for power observation

Parameters	Simulation	Measurement
Ringing frequency	68 MHz	66 MHz
First amplitude (peak to peak)	650mV	600mV

Table 2-1: Comparison of simulations and measurements values for power observation

We can see thanks to Table 2-1 or in Figure 2-22 that the difference between measurement and simulation is less than 10%, validating the model regarding power behavior. The model could be validated if the difference between measurement and simulation is less than 15%. Of course, this is only one example introduced here to illustrate the validation procedure.

4.3. Signal observation through signal integrity

The term signal integrity (SI) defines the signals quality to ensure good system operation inside the specified usage domain. Here, the purpose is still to validate the simulated model by studying the signal integrity. In the same way as with power observation, specific points have been set for the comparison between simulation and measurement.

These points are:

- The resonance frequency value of the oscillation created by an IO's change of state
- The first amplitude value of this resonance
- The rising or falling time of an IO between 30% and 70% (percentage depending on the power supply value).

As a matter of fact, identically to the power observation, these points need to be compared for the entire testbench to ensure the model validation. Figure 2-23 shows an example of the comparison done with 16 switching IOs, each with a load capacitor of 15pF.

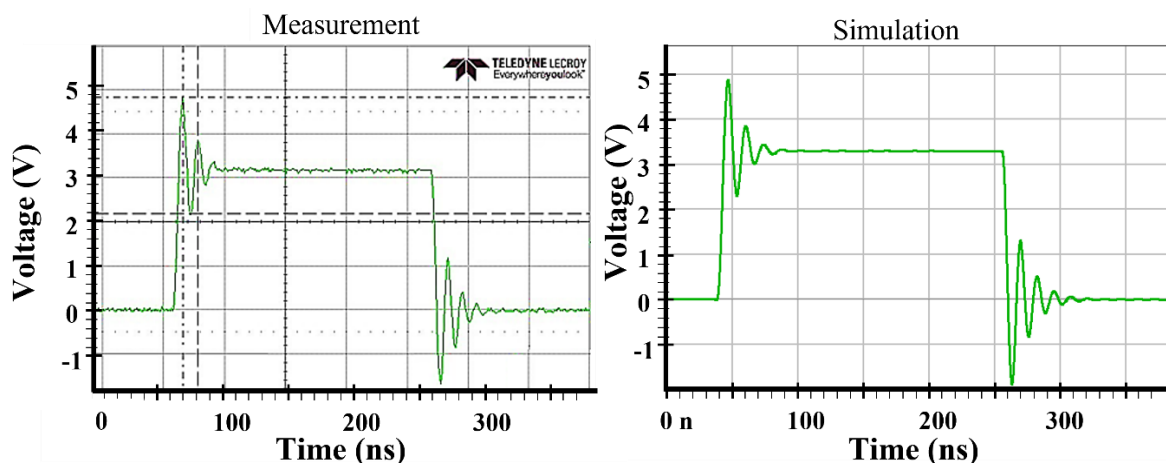


Figure 2-23: Comparison between measurement and simulation for signal observation

Parameters	Simulation	Measurement
Rise/fall time	1.5ns	1.5ns
Overshoot amplitude	2.5V	2.7V
Ringing frequency	74MHz	80MHz

Table 2-2: Comparison of simulations and measurements values for signal observation

We can see thanks to Table 2-2 or in Figure 2-23 that the difference between measurement and simulation is less than 10% of error, thereby validating the model regarding the signal behavior. With these comparisons of power and signal correlation we can confirm that the model created has the expected behavior, similar to the physical MCU.

4.4. Model refinement in case of a non-validation

We detailed the final validation of the model with the comparison between simulations and measurements. Before reaching this final one, several comparisons were done because the error margin was more than 15% leading to the conclusion that the model could not be validated and must be refined. In that case, it could be complicated to find if the problem comes from a mistake or an omission in the model. For example, for the model of DUT introduced in section 4.1 and used for this validation procedure development, the model was done by hand calculation and didn't fit with measurements. After several paths of refinement, it appeared that an element was missing in the board model. This was found, thanks to the research paths detailed in next subsections. Obviously, this is not covering the entire possibilities, but it introduces the main subjects. To be noted, IO's setup needs to be checked before going further as this the origin of the di/dt and, due to its complexity, a setup mistake could happen quickly.

4.4.1. Load capacitor

The rising and falling time of an IO is mainly defined by the capacitor connected to its output. The value of this capacitor is defined by the addition of different capacitors of circuit defined by:

- The load capacitor connected to the output. This one could be defined by the external component connected at the end of the line for the communication. For example, an external memory which communicates with the HexaSPI communication protocol adds 6pF per IO.

- The capacitor of the probe which must be considered in the model, at the same place as the measurement
- The capacitor of the PCB's line

If the rising or falling time aren't correlated, the first thing to do is to determine the difference of this capacitor value between simulation and measurement. In that way, an additional simulation could be done. This simulation is an abacus of rising/falling edge in function of the total output capacitor. An example of an abacus is defined in Figure 2-24, still based on the IO of our DUT where the rising and falling time are not identical due to IO's design.

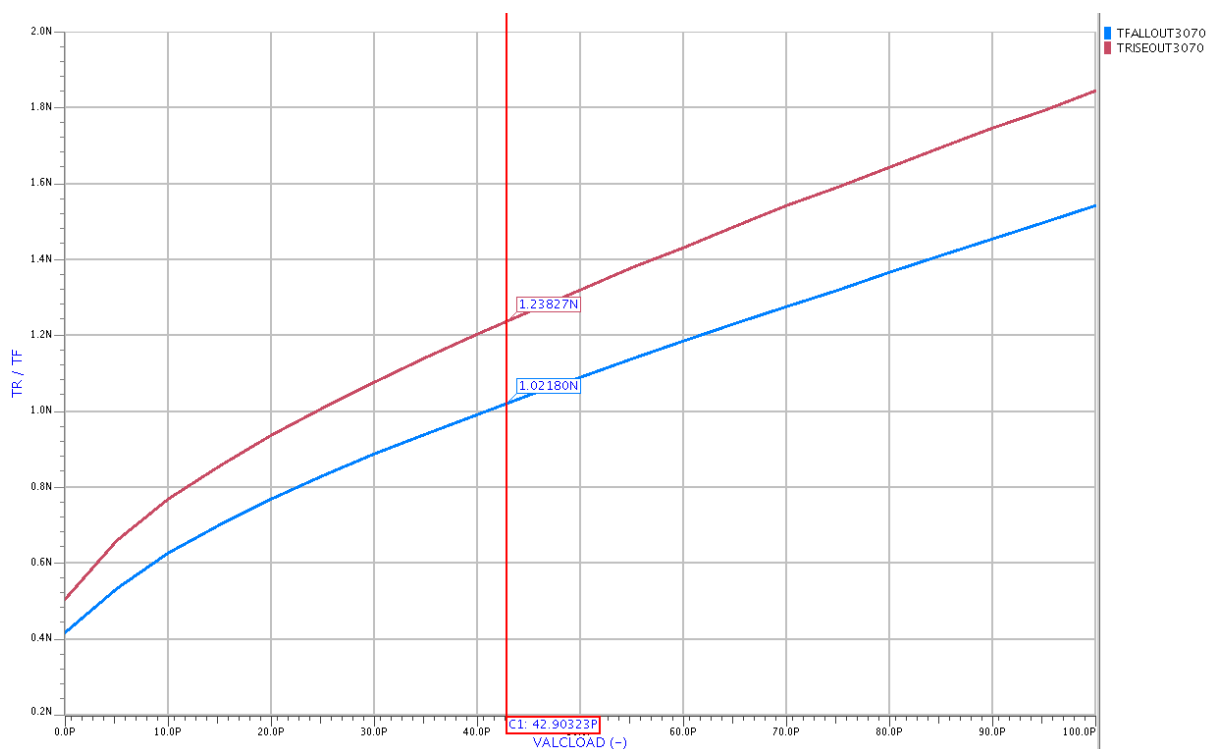


Figure 2-24: Abacus of rising/falling time in function of load capacitance

Thanks to this abacus it is possible to observe the value expected in our model for the output capacitor and to modify the proper parameter. For the probe, especially if it is a passive one, it has to be considered in the model. For the load capacitor used to emulate an external component, its value can generally be checked in the datasheet. Finally, if it is not one of those two possibilities then, the problem is certainly from the model development itself. In that case, other comparisons might be wrong such as resonance frequency and another path of research should be followed.

4.4.2. Skin effect

When ringing frequency and noise amplitude on signal and power is not correlating between measurement and simulation it can be interpreted as an incorrect value for R, L, C component of the model. In that case, one of the paths of research could be the skin effect. Mainly this effect illustrated in Figure 2-25 is an increases of the conductor effective resistance because of the decrease of the conductor effective section. It is a physical phenomenon of any connection where electric current flows at the “skin” of the conductor proportionally to the frequency of an alternating current. So, the more the frequency increases and the more the current flows only at the conductor “skin” and the more the effective resistance of a conductor is big [63], [64], [65].

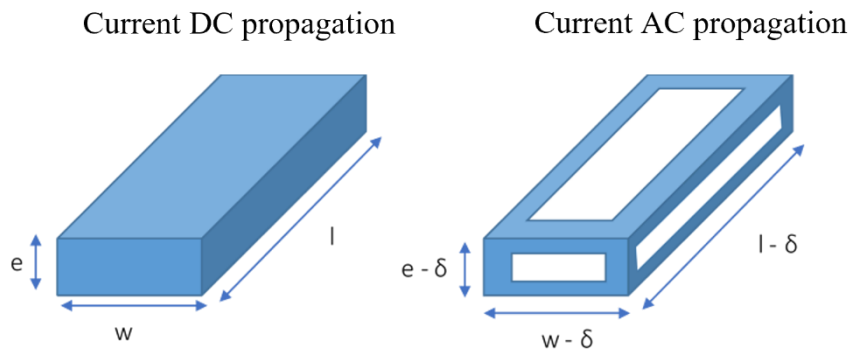


Figure 2-25: Illustration of the skin effect

In this study, the frequency of the alternating current defines the signal propagation and it is $1/T_{R/F}$ where $T_{R/F}$ is the average of rising/falling time. For example, for a communication protocol where IO have a rising/falling time of 2ns, the equivalent frequency is 500MHz. So, this skin effect also named skin depth needs to be considered if the signal propagation will have an impact. The software extraction directly provides this option with an extraction at a specific frequency. For the hand extraction, the skin factor δ is calculated with Equation 2-23 and should be added in the computations as illustrated in Figure 2-25. There are also calculators available on the internet [66].

$$\delta = \sqrt{\frac{\rho}{\mu * f * \pi}}$$

Equation 2-23: skin factor

4.4.3. Other paths for refinement

If the comparison is still not good after the check of the IO setup, the study of the load capacitor value and the confirmation of connector resistance then the problem should come from an omission in the model. In this case, it is up to the designer to find the parameter that influences the SSN and is not properly considered in the model. The most obvious could be cited:

- If the board includes a socket for the package connection, the socket should be modeled because it adds parasitic elements
- If the board includes physical connectors/contactors, they should be included in the model because they are also defined by parasitic elements
- The communication protocol should be confirmed
- The problem could also come from the oscilloscope band-width and sampling frequency

In that way, chapter 3 developed the study of several parameters highlighted during this thesis and which have an influence on the SSN effect.

5. Conclusion

We detailed, in this chapter, two methodologies to model a complete system defined by a die, a package, and a PCB. The first method is defined for a hand computation that could be done by anyone without the need for a software license but will be a first order model. The second method is characterized by a software parameter extraction which has the advantage of extracting a SPICE netlist including all parasitic parameters and coupling effect and this, by taking into account the skin effect. Of course, this software method has a better accuracy but requires a software license and specific knowledge to properly use it. Then, this chapter explained a validation methodology developed with a first device under test and done through an accurate comparison between measurements and simulations. This validation step is mandatory to ensure that the model is an accurate representation of the STM32 behavior in terms of SSN. Finally, once a model is developed, it is possible to work only by simulation and it is real advantage in this EMC study.

- Firstly, it allows observing an MCU failure in a quicker and cheaper way than with physical measurements as there is no need of specific manufacture.

- Secondly, it allows some observations that would not be feasible in measurement except with specific and expensive package or PCB. For example, the SSN can be directly examined at die level.

In conclusion, these steps of modeling and validation are mandatory in order to modify the EMC approach by anticipating the SSN effects at the design stage as mentioned in chapter 1. The next chapter is focused on this, with firstly, the simulation study of an STM32 failure leading to the proposal of first design rules. The second part of the chapter is focused on the predictive model development, in order to anticipate the MCU behavior for a specific communication protocol.

Chapter 3. Simulations and results

1. Introduction

This final chapter is dedicated to the presentation of the design rules developed during this thesis. This chapter is divided into two parts. The first one introduces the model developed for a complete system defined as the 1st DUT and composed of an STM32 and a board designed by STMicroelectronics. After the model validation, simulations will show the comparison of this model with different test cases to study the parameters that influence the SSN. The main simulation results will be introduced and used to conclude about design rules recommended to ensure the MCU robustness against SSN effects. Then, the second part of this chapter is dedicated to a 2nd DUT defined by MCU in the design process and for the specific HexaSPI communication. This second part will firstly present the HexaSPI communication to allow a better understanding of constraints linked to the protocol. Then, the predictive model achieved and the main issues met during its development is detailed. We will use simulations of this model to justify guidelines and design modifications in order to guarantee the MCU robustness and the communication efficiency. Finally, the predictive model developed is compared through the validation procedure and is refined, based on these measurement comparisons.

2. Work on a manufactured MCU

The choice of this 1st DUT has been made due to an issue discovered at the MCU validation stage. The SSN was suspected as the origin of these perturbations because performance degradations were observed when communication between the MCU and an LCD driver (Liquid-Crystal Display) was settled as illustrated in Figure 3-1.

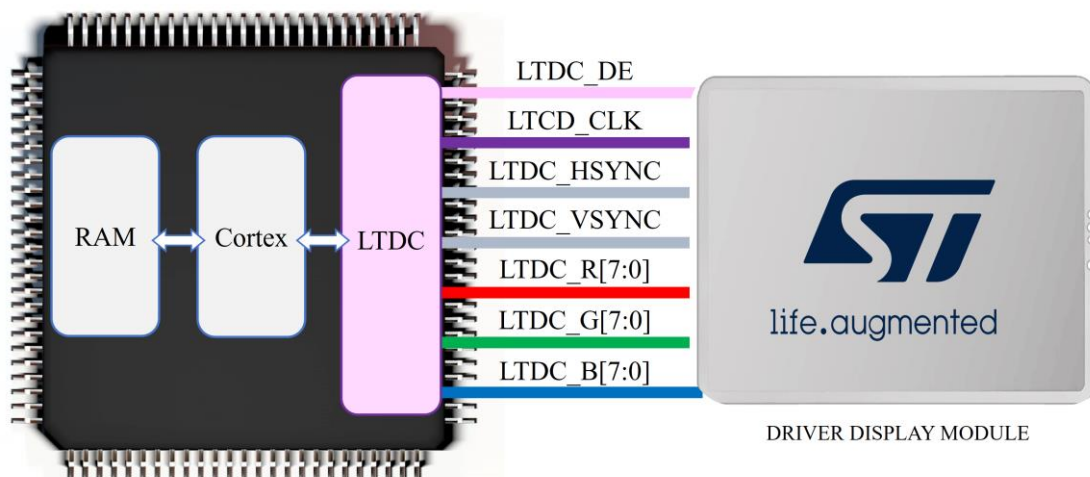


Figure 3-1: LTDC communication

This product is the best example to demonstrate the EMC workflow explained in chapter 1. Indeed, during the design stage, this communication was not considered and after the MCU manufacture, it appears that this communication was leading to MCU's performance degradation resulting in an important delay in terms of release on the market in order to resolve this problem. Then the purpose of the study is to find a solution to this issue and also to understand which parameters have influenced the SSN impacts. Finally, simulations will be used to justify new design rules to apply on this product.

2.1. 1st Device under test

2.1.1. TFT-LCD communication

The TFT-LCD protocol (Thin Film Transistor Liquid Crystal Display) more commonly named LTDC is used to display a movie on LCD screens. To achieve this, the MCU addresses a controllable CMOS matrix as shown in Figure 3-2. The size of the CMOS matrix is characterized by the screen pixel number and each pixel is controlled by three transistors -one transistor per RGB color (Red Green Blue) -. CMOS matrices are used to increase the screen performance in terms of time responses and stability [67]–[70].

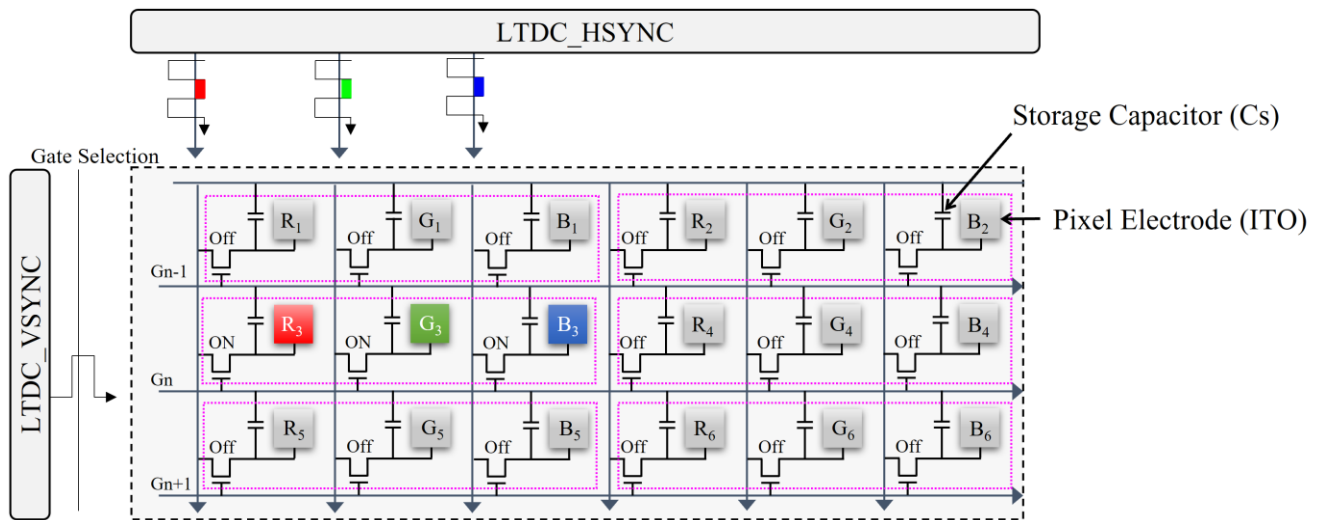


Figure 3-2: CMOS matrix principle for LTDC driver

To operate, this communication requires:

- 1 IO to enable the communication with the “LTCD_DE”
- 1 IO used for the clock establishment with the “LTCD_CLK”

- 21 Simultaneous Switching Outputs (SSO) to address simultaneously 7 pixels, working at 90MHz frequency and with a maximum spread of 1.5ns between the 21 data through “LTCD_R[7:0], LTCD_G[7:0], LTCD_B[7:0]”
- 2 IOs to address the selected line and column of the matrix working at 90MHz with “LTCD_HSYNC” and “LTCD_VSYNC”

2.1.2. DUT board

The DUT used for this work is defined by a complete system manufactured by STMicroelectronics. The board is a Discovery board which provides an overview of all possible communications offered by the STM32. Figure 3-3 is a picture of this board highlighting the different components such as the LTCD driver and the power management for IO's supplies. Moreover, the IO's supplies are decoupled with 8 bypass capacitors of 1 μ F with a 0201 body size which is equal to a length of 0.6mm and a width of 0.3mm.

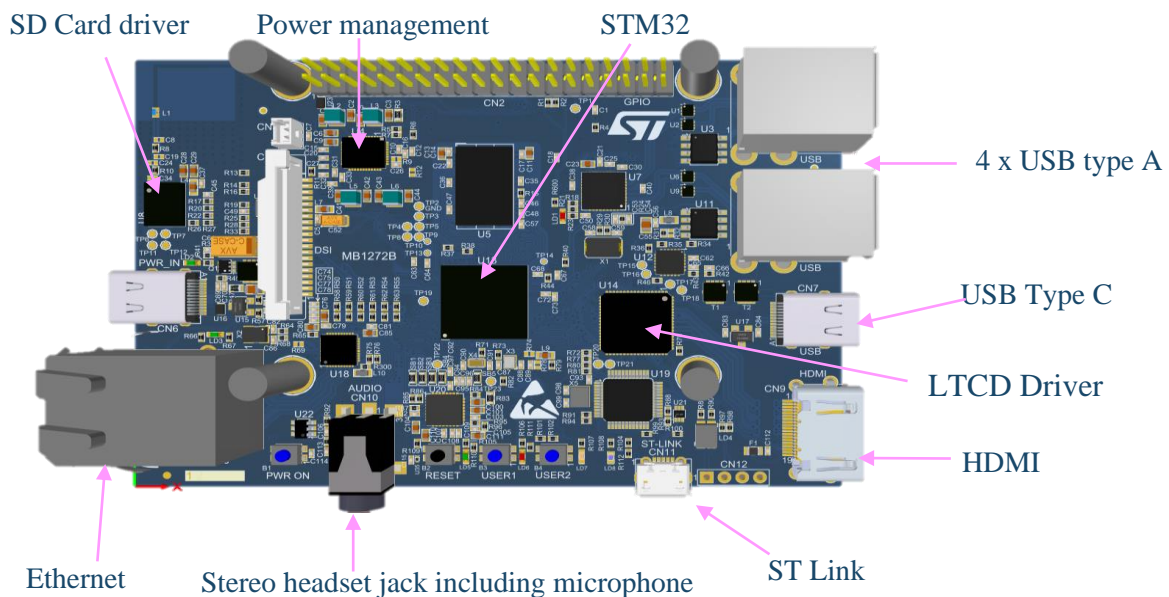


Figure 3-3: Discovery board overview

2.1.3. STM32 of the DUT

The STM32 package is a 361 balls BGA which we will name BGA n°1 for a better understanding in this chapter. BGA n°1 has on one hand, 7 V_{DDIO} balls and 49 V_{SS} balls for external supply connection and on the other hand, 35 V_{DDIO} and 49 V_{SS} connections between package and padding. The die's padding is composed of 354 IPs (Intellectual Properties) defined by several functional blocks as power management and distribution, 324 IOs with different specificities as I2C or analog switch option, the crystal clock management, etc. The particularity

of this padding is the “shunt” done on the left side of the padding, allocated to the external memory communication which has its own and isolated supplies. This part of the padding is not considered in the study as it is isolated from all others IOs. Figure 3-4 schematize this padding with the IOs distribution and IOs used for the LTCD communication but also the highlight of power and ground connection.

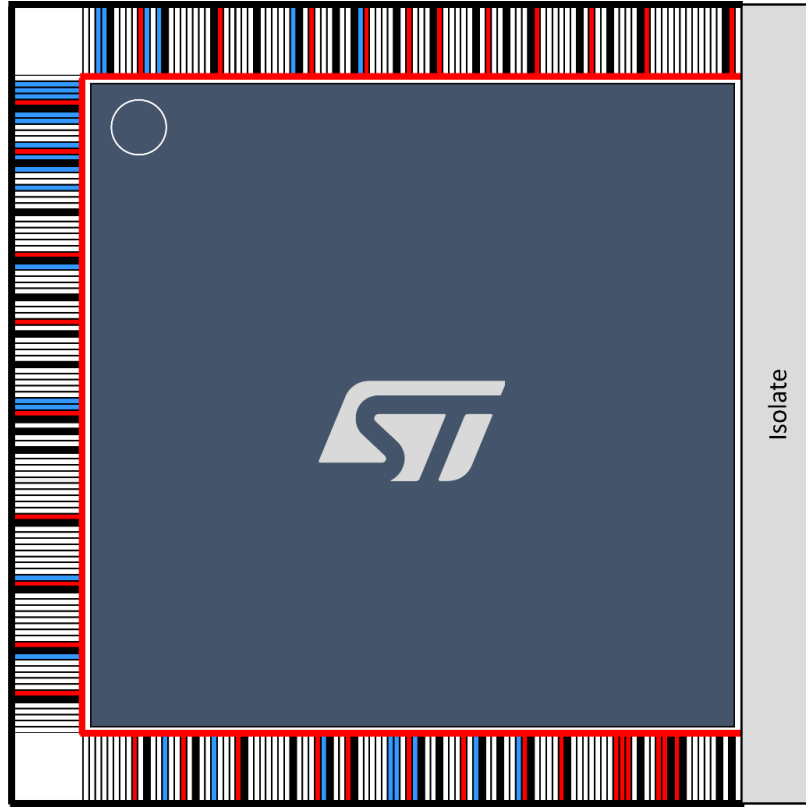


Figure 3-4: 1st DUT Padding schematic

Finally, IOs have been designed in a 40 nm CMOS technology and can be supplied at 3.3V or 1.8V. Table 3-1 summarizes their specifications in terms of operating frequency, rising and falling time and the associated di/dt .

Supply (V)	Speed mode	Max frequency (MHz)	Max T_R and T_F (ns)	Data max delay (ns)	current slope (mA/ns)
3.3	0	20	11	22	6
	1	50	5.5	12	25
	2	100	3.3	6.2	33
	3	166	2.2	5.2	55

Supply (V)	Speed mode	Max frequency (MHz)	Max T_R and T_F (ns)	Data max delay (ns)	current slope (mA/ns)
1.8	0	25	6.7	14	4
	1	50	4.2	8	12
	2	100	3.0	5.4	20
	3	166	2.2	3.7	55

Table 3-1: 1st DUT IO specifications

2.2. DUT modeling and validation

The model of the complete system was done following software modeling methods for the package and the PCB. One of the problems met during the board modeling was its complexity due to the large number of connections as already depicted in Figure 3-3. For the complete board modeling, parameter extraction took more than 1 week, and simulations based on this model as well. Then, the decision was made to shunt the board extraction to only useful connections with the points listed below and as illustrated in Figure 3-5:

- tracks used for the communication between the MCU and the LTCD driver.
- All power and ground connections including ground plane and bypass capacitor connections.
- The test point used for power measurement.

Two Spice netlists including all parasitic elements coupling have been extracted at 450MHz for the board and the package. Note that, the extraction has been made at 450MHz, based on the IO's rising time at 90MHz and supplied at 3.3V in order to consider the skin effect. Die's parameters are extracted based on computation method and the IO is defined with its SPICE netlist.

Finally, a complete model is obtained as illustrated in Figure 3-6 and Table 3-2 summarizes the associated values. This table is a model overview so only an average is provided for a better understanding and coupling value are not added because this factor changes a lot in depending on the track observed. The final model also considered the probe used for measurement and the load capacitor assimilated to the LTDC driver.

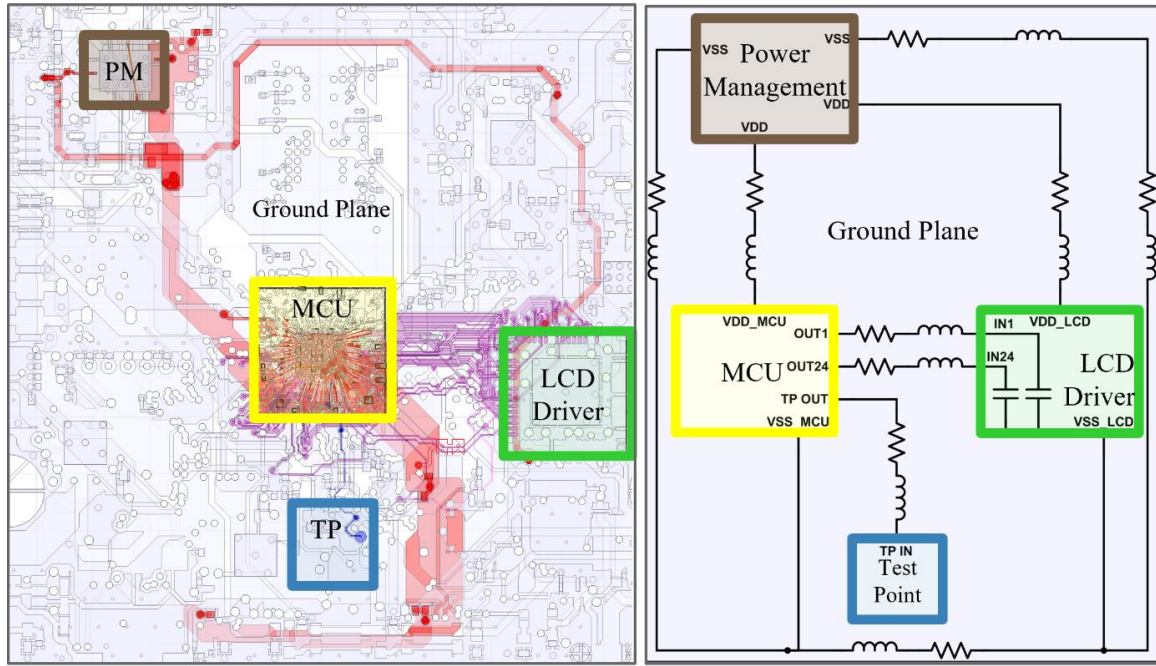
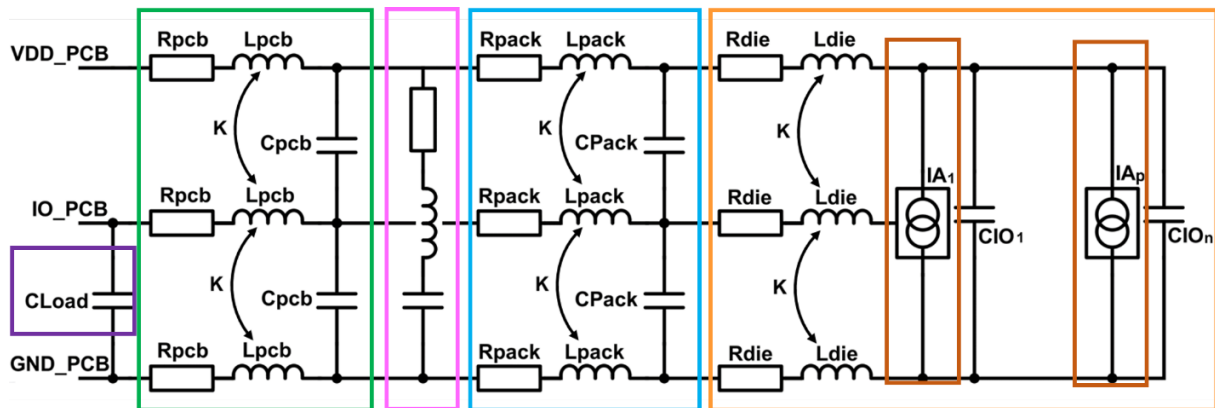


Figure 3-5: Overview of the board extracted


 Figure 3-6: Reminder of the ICEM for the 1st DUT model

Parameter	di/dt per IO	R	L	C
$IA_x R_{DIE} L_{DIE} C_{DIE}$	In function of the IO speed mode	65mΩ	50pH	3pF
$R_{PACK} L_{PACK} C_{PACK}$	/	0.8Ω	3nH	30fF
Bypass capacitor 0402 1uF	/	12mΩ	0.2nH	1uF
$R_{PCB} L_{PCB} C_{PCB}$ for track	/	0.8Ω	10nH	1pF
C_{LOAD}	/	/	/	5pF
Active probe	/	1MΩ	Neglected	0.9pF

 Table 3-2: Overview of the 1st DUT model values

When the model development for the complete system was finished, its validation was made through the comparison methodology explained in chapter II with a final error less than 15%, confirming the model accuracy. An example is shown in Figure 3-7 where the LTDC communication is settled with IO in speed 3, a 3.3V power supply, at ambient temperature and in typical process. For this figure, peak-peak voltage and the first resonance frequency are compared, and results are :

- Measurement : $V_{PP} = 510 \text{ mV}$ & $F_{\text{resonance}} = 225 \text{ MHz}$
- Simulation : $V_{PP} = 480 \text{ mV}$ & $F_{\text{resonance}} = 200 \text{ MHz}$

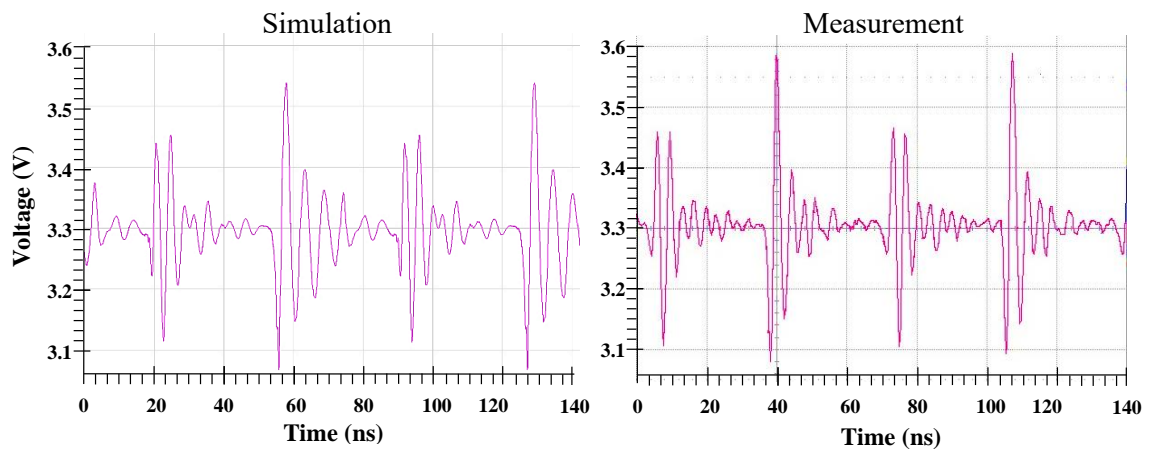


Figure 3-7: Simulation vs measurement comparison for model validation

Once the model is developed and validated through comparison procedure, it is then possible to study by simulations the MCU behavior in terms of SSN and to understand which parameter is influencing it. The next two sections summarize the main points highlighted with this first DUT.

2.3. Bypass capacitor placement

This section studies the influence of bypass capacitor placement on PCB with the highlight of via influence and on package with the use of SiP capacitors. For all simulations and measurements presented here, the communication LTDC was settled to 90MHz, ambient temperature, with a 3.3V supply and IO in speed 3 in order to recreate the observed failure.

2.3.1. At PCB level with via influence

The first parameter observed with these simulations has been the impact of vias. As a reminder, a via is used to connect the package with bypass capacitors both of them soldered on

each PCB top and bottom. Vias are generally used because there is not enough space between balls of a package for capacitor routing or, if it is possible this solution is generally too expensive for the consumer. In order to study the vias influence on the SSN, two simulations were settled. The first one is the simulation of the complete system introduced in the previous section 3.2. The second one is also the complete system with only one difference: vias are removed and bypass capacitors are directly connected to balls. These two cases are illustrated in Figure 3-8.

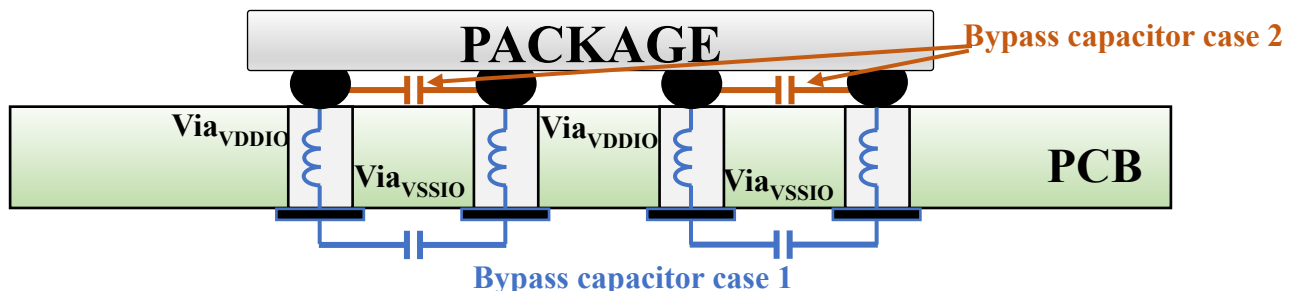


Figure 3-8: Bypass capacitors illustration for case 1 and case 2

The two simulations are compared with the observation of noise level and this at two different points: directly at supply balls named “outside noise” and the second point is an in-die extract, reflecting the padding IO supplies and named “inside noise”. Figure 3-9 shows the simulation result. To be noted, the noise level is the voltage variation measured on $V_{DDIO} - V_{SSIO}$. As we can see, this figure highlights the vias influence on the SSN with a noise reduction of 70% at balls level and a reduction of 36% at die level. Moreover, to have an idea of the via parasitic elements, an extract has been done on the DUT for two vias -one for V_{DDIO} and one for V_{SS} - from the ball package to the bypass capacitor pin, so it includes the via and the capacitor routing. It appears that the whole connection is defined by an inductance of 2nH and a coupling between the two vias of $k=0.35$.

Finally, observations of these power supplies were done in test points that would not be accessible with a probe for this DUT. Indeed, the package balls are soldered on the PCB without access for physical measurement. In the same way, the package is not a specific manufactured one which means the die is totally enclosed without probe access. But, as this model was validated with measurements/simulations comparisons, we know its accuracy regarding the MCU behavior in terms of SSN.

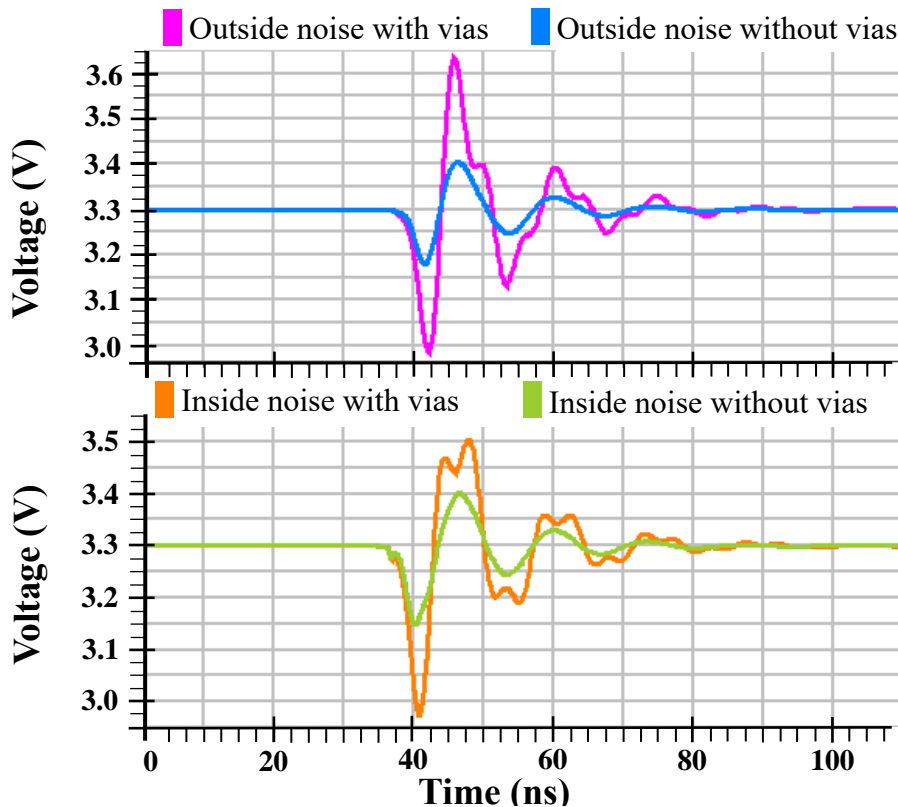


Figure 3-9: Simulations with and without vias

2.3.2. At package level with SiP

In the previous simulation, the bypass capacitor was connected directly at ball level, putting the capacitor closer to the EMI generation. This study of vias influence leads to this second path of research : what is the impact of bypass capacitor placement on the SSN noise. A part of the answer is given in the previous study because it is seen that the noise is reduced when vias are removed. Then, a second study is done with a SiP package (System in package). We cited this package in the state of art chapter but as a reminder, it is a package which directly embedded the bypass capacitors. So, this package BGA n°2 was re-designed in order to add SiP capacitors while keeping the design as close as possible to the original package defined as the BGA n°1. The package design as well as the bypass capacitor values and placements were decided by package designer and its layout is shown in Figure 3-10. On this figure, it can be seen, in red the V_{DDIO} bonding and the associated 7 balls, and in a similar way, in blue all GV_{SS} connections. Leadframe connection are transparent for a better layout readability. Also shown on this figure, pink boxes to localize SiP capacitors defined by :

- 3 capacitors : 0201 of $1\mu F$
- 4 capacitors : 0201 of 220pF

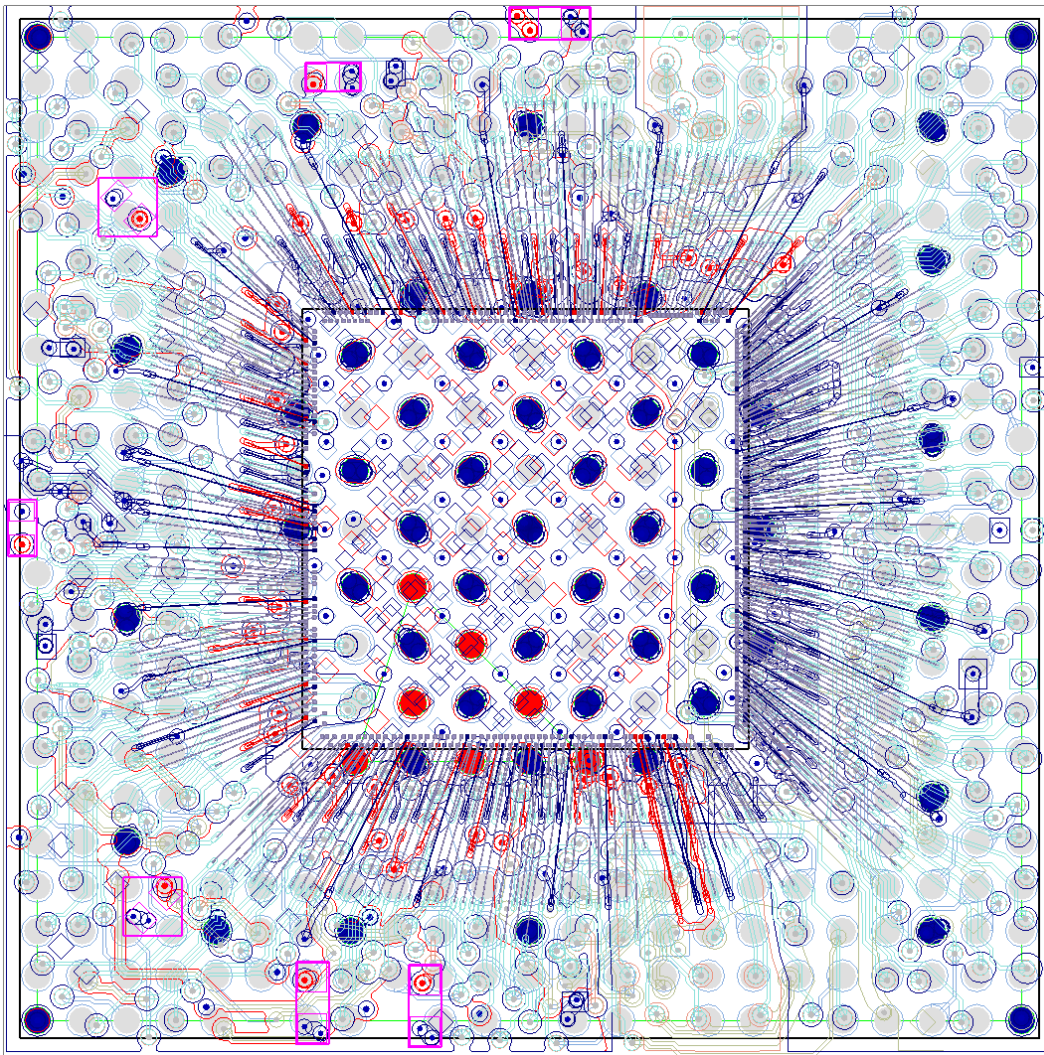


Figure 3-10: Layout of the BGA n°2 with SiP capacitors

This new package was modeled through software extraction to obtain the SPICE netlist. Then, the first observation was to compare the two BGA designs with a simulation in the frequency domain as follows:

- Simulation 1 : The first and complete DUT with BGA n°1 modeled and introduced in the beginning.
- Simulation 2 : The same padding and PCB as the one simulated, with this BGA n°2 and the 7 SiP capacitors connected.
- Simulation 3 : The same padding and PCB than simulation one, with this BGA n°2 and the 7 SiP disconnected.

Once again, the possibility to disconnect the SiP capacitor is a real advantage of the simulation because it could be complicated to open the package and physically unsolder them.

The final AC comparison is shown in Figure 3-11. Moreover, it is important to highlight that the padding and the PCB are exactly the same, only the package changed with BGA n°1 vs BGA n°2. To be noted, the vertical axis defines the magnitude in decibel-Ohm ($\text{dB}\Omega$), to convert the value in Ohm, the Equation 2-1 must be used.

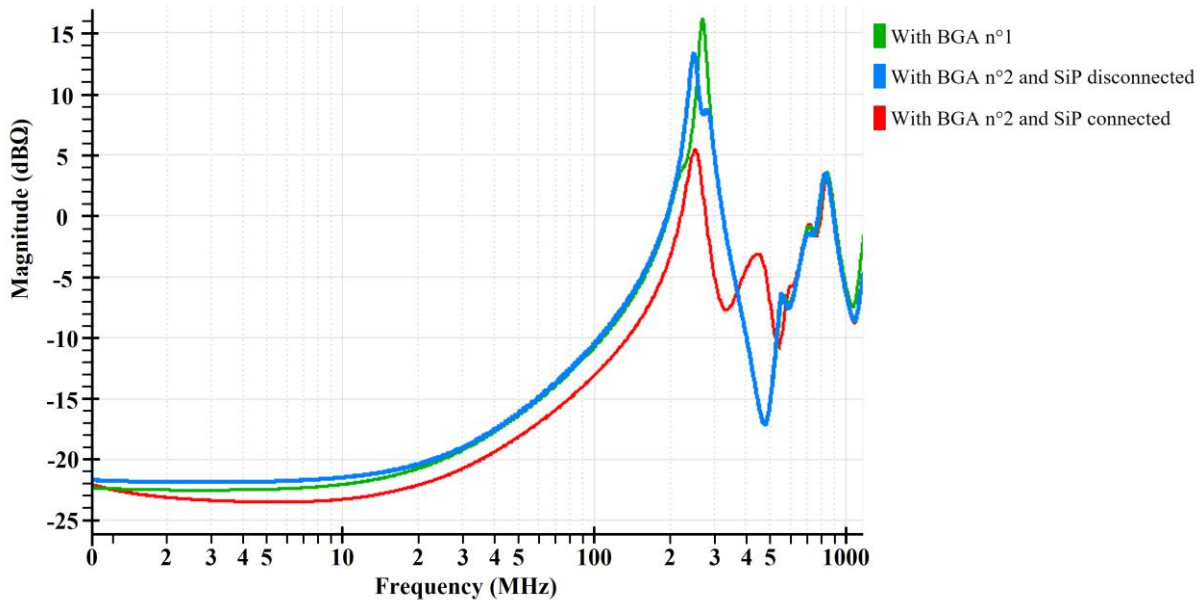


Figure 3-11: AC simulations for package comparison

Then the impact of SiP capacitors is observed by simulation and by measurement as follows:

- Setup 1 : PCB discovery board + basic 361 balls BGA n°1 + Pading of 354 IPs
- Setup 2 : PCB discovery board + 361 balls BGA n°2 with SiP + Pading of 354 IPs.

For the measurements, they are done with an active probe plotted between the Test Point (TP) and a resistance connected to the ground next to this TP, already shown in Figure 3-5. Then, the comparison is done with the LTDC communication settled at 90MHz, at 3.3V and for IOs in speed 2 and 3. The Figure 3-12 illustrates this measurement in speed 3.

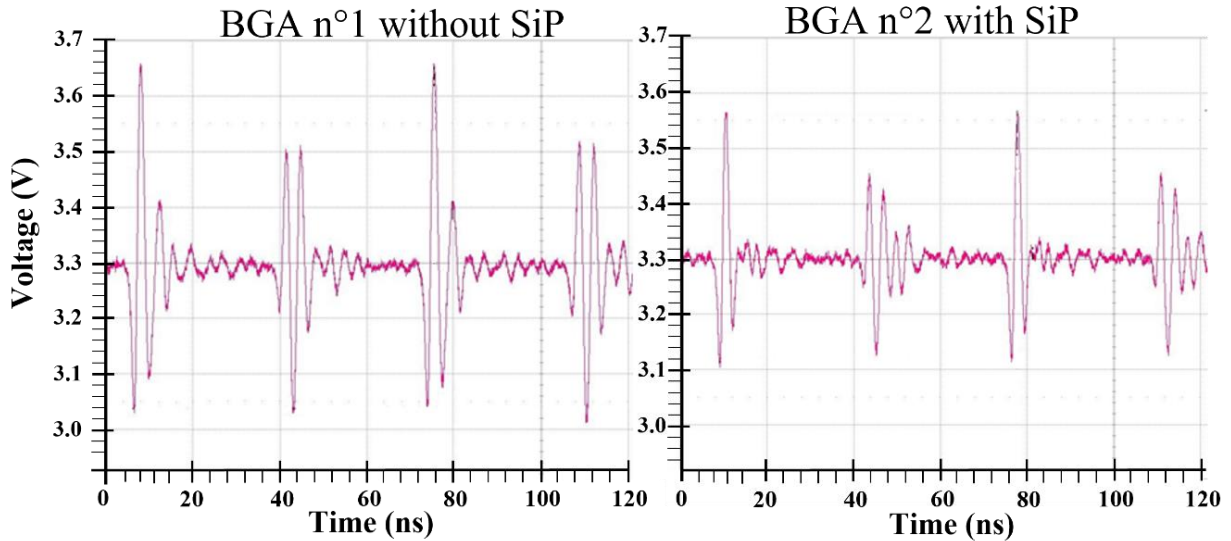


Figure 3-12: Noise level ($V_{DDIO} - V_{SSIO}$) measured with BGA without SiP (left) and BGA with SiP (right)

The same observations are also done in simulations, allowing at the same time to measure the noise reduction at padding level. Table 3-3 summarizes all of this work, for IOs in speed mode 2 and 3 and for measurement and simulation.

IO speed mode	Noise measured on TP		Noise simulated on TP		Noise simulated on padding	
	Speed 2	Speed 3	Speed 2	Speed 3	Speed 2	Speed 3
BGA n°1 without SiP	430 mV	520 mV	440 mV	500 mV	420 mV	480mV
BGA n°2 with SiP	320 mV	370 mV	290 mV	365 mV	180 mV	220mV
Noise reduction	25 %	29 %	34 %	27 %	57 %	54 %

Table 3-3: Summary of BGA vs SiP comparison in measurement and simulation

The impact of SiP capacitors clearly seen with this study and shown in Table 3-3 with a noise reduction of more 50 % at padding level which also shows the influence of bypass capacitors placement on the SSN.

2.4. Conclusion

A summary of all studies made in this section is provided in Table 3-4 :

	Package	PCB	Comment
1	BGA n°1 : Original 361 BGA	Original discovery board	Original model of the DUT
2	BGA n°1	Board model modified. Vias are removed and capacitors connected to balls	Compared with case 1 to observe vias influences
3	BGA n°2 with 7 SiP capacitors	Original discovery board	Compared with case 1 in with an AC simulation to study design difference between BGA n°1 and BGA n°2. SiP capacitor disconnected in the model
4	BGA n°2	Original discovery board	Compared with case 1 in measurement and in simulation to observe the SiP capacitor effect

Table 3-4: Summary of all studied cases on the 1st DUT

With simulations and measurements of this 1st DUT, we demonstrated the influence of bypass capacitor placement at PCB and package level. The conclusion of this work is :

- Vias is a major influencer of the SSN effect by adding parasitic elements on the PDN.
- The bypass capacitor placement must be considered with attention and put as close as possible to the SSN origin as illustrated with SiP capacitor.

To conclude this study of an existing MCU, we need to remember that this DUT was chosen because an issue appears due to the SSN generated by an LTDC communication. To resolve the problem and based on the conclusion of this work, the board was optimized with vias parallelization, and the decrease of bypass capacitor routing and board design recommendations were written for consumer. The SiP package wasn't keep because it was considered too expensive for the market. Finally, IOs design have been changed to reduce the di/dt .

3. Predictive model for future MCU

The second part of this chapter III is dedicated to the anticipation of future MCU behavior regarding the specific HexaSPI communication protocol. This section is divided into several parts. Firstly, we will introduce the HexaSPI communication and all specifications required to ensure the correct behavior of this high-data rate communication. Then the methodology to develop such a model as well as the main predictive model in order to study the MCU behavior and ensure its robustness against SSN will be defined. This part also includes the two main issues encountered during the development. From this model simulations were settled to work in cooperation with board and package designer. For the package, the predictive model helped to define the CSP layout by observing the difference between 1 layer and 2 layers CSP. For the board, the previous work was applied with vias optimization and bypass capacitor placement. Finally, this predictive model helped to justify the addition of in-die bypass capacitor placement in order to decouple the noise as close as possible to the EMI.

3.1. HexaSPI communication protocol

The xSPI (eXpanded Serial Peripheral Interface) is a protocol used to communicate with a Non Volatile Memory defined by the JESD 251 standard [71]. This standard provides specification and minimum requirements for the communication compliance. The HexaSPI is characterized as a Double Data Rate (DDR) communication to write or read information with one or two external memories as illustrated in Figure 3-13.

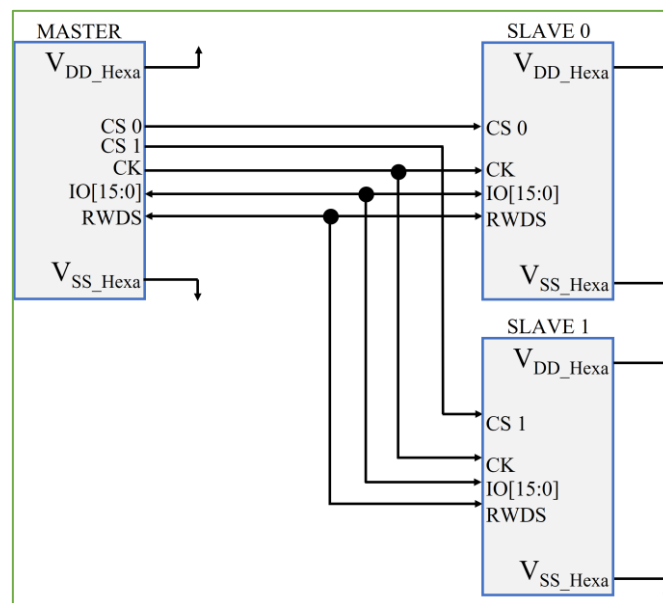


Figure 3-13: HexaSPI overview

This communication can operate up to 133MHz for a 3.3V power supply and up to 200MHz for a 1.8V power supply and it requires :

- 16 Simultaneous Switching IOs for an Hexa communication
- 1 Clock (CLK) at 3.3V or 1 Clock (CLK) plus 1 $\overline{\text{Clock}}$ (nCLK) in opposition phase at 1.8V
- 2 Chip Select (CS) in case of double memory connection.
- 2 signals named RWDS (Read Write Data Strobe) to define if the MCU will read or write data to or from the memory.

It is also characterized with specific timing constraints as illustrated in Figure 3-14.

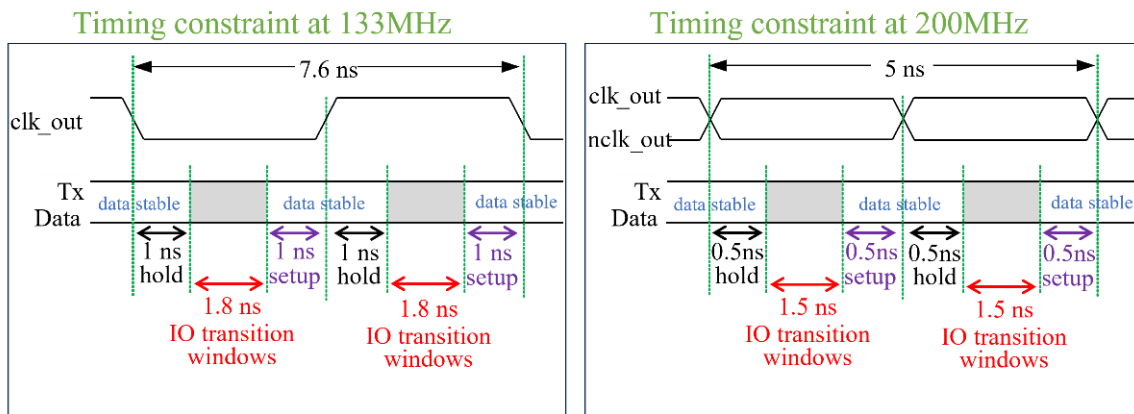


Figure 3-14: HexaSPI Timing constraint

Finally, in addition to these timing constraints, the communication must respect the specifications listed in the Table 3-5. These constraints are a summary of the one extracted from the JESD and ones from STMicroelectronics.

Parameter	Constraint
ΔV on padding ($V_{DDIO} - V_{SSIO}$)	$\Delta V < 0.2 * V_{DDIO}$
Duty Cycle (DTC) for Clock and IOs	$45\% \leq DTC \leq 55\%$
V_{IL} & V_{IH} at T_{SETUP} & T_{HOLD}	$IO < V_{IL} = 0.3 * V_{DDIO}$ $IO > V_{IH} = 0.7 * V_{DDIO}$
nCLK & CLK crossing (only for 1.8V)	$0.4 * V_{DDIO} = 0.72V < \text{Crossing} < 0.6 * V_{DDIO} = 1.08V$

Table 3-5: HexaSPI specifications

The aim is to develop a predictive model to anticipate the MCU behavior for this HexaSPI (HSPI) communication in order to guarantee the product robustness regarding all specifications.

3.2. Predictive model development

This study of HSPI communication was made for a future MCU which means, there are no database available to create a model and it has to be done in a predictive way, based on the product specifications and on specific knowledge acquired during previous modeling.

A predictive model is achieved by applying a recursive work as follow:

1. Model development with hypotheses based on the known product specification and with comparison with manufactured product.
2. Model simulations and observations of the MCU behavior.
3. Conclusions from the simulations to understand if the MCU fulfill all the expected specifications
 - If the answer is no, this recursive work restarts to the beginning but first, we need to determine if the problem is:
 - An omission or a wrong hypothesis
 - A real issue found and the MCU robustness must be improved
 - If the answer is yes, the final conclusion and all guidelines can be summarized.

3.2.1. Die predictive model

This subsection explains the final model developed through this iteration procedure. Then, the next subsections detail the main refinement done during this iteration stage to obtain this final model.

The first part developed for this model was the die part with IOs and the associated supplies. The IO model is based on a designed IO in a similar technology with $di/dt = 50 \text{ mA/ns}$, a $T_{R/F} = 0.9 \text{ ns}$ and $C_{IO} = 5.5 \text{ pF}$. For the die's PDN, a resistance and an inductance are connected to each IO's power and ground to define the PDN parasitic element with $R = 3\text{m}\Omega$ & $L = 1.5\text{pH}$. Moreover, the first decision made was to shunt the HexaSPI supplies from the rest of the padding in order to protect other IOs from the SSN generated by this high-data rate communication and reversely. Finally, the IOs distribution and power and ground pads for this padding section is depicted in Figure 3-15.

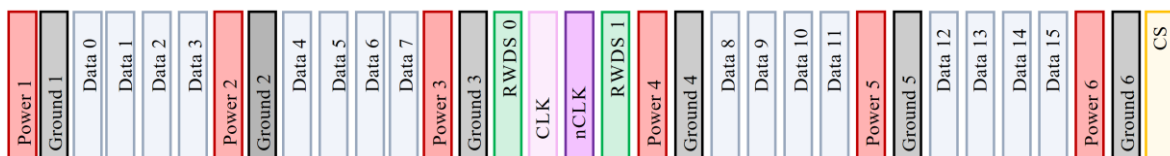


Figure 3-15: Padding distribution for the HexaSPI

3.2.2. Package predictive model

The main package used for this predictive model was the BGA and this model was defined from a previous package where the die size was equivalent. The final model of this package dissociates parasitic elements in three categories:

- connection for power and ground; The study of previous package highlighted an optimization of power and ground connection with the use of centered balls. In consequence, their connections and impedances were smaller.
- connection for CLK and nCLK; During the model development, it appears that these signals are the most sensitive ones especially because of the crossing specification between CLK and nCLK at 1.8V. So, their connections were optimized but, parasitic elements are bigger than the one defined for power and ground as centered balls are kept for power and ground connection and cannot be allocated for signals.
- connection for all other data.

This package model also incorporates a coupling factor at two levels. To properly understand the factors applied, an example is drawn in in Figure 3-16, based on the HSPI distribution. The justification of the coupling factor is detailed in the subsection “3.2.4. Issue with coupling factor”

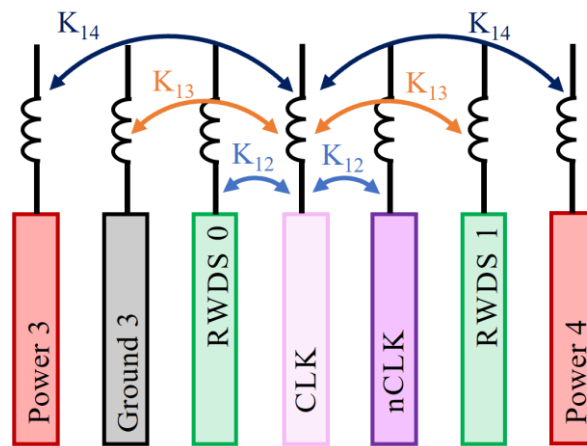


Figure 3-16: Coupling factor illustration

Finally, the predictive model of the BGA package is defined with 4 V_{DD_Hexa} balls and 4 V_{SS_Hexa} balls and is summarized as follow:

- Data connection : $R_{IO} = 0.5 \, \Omega$ & $L_{IO} = 2.8nH$
- CLK and nCLK connection : $R_{CLK} = 0.3 \, \Omega$ & $L_{CLK} = 2nH$
- Power and ground connection : $R_{PG} = 0.2 \, \Omega$ & $L_{PG} = 1.4nH$
- Coupling factor : $k_{12} = 0.35$ & $k_{13} = 0.25$ & $k_{14} = 0.2$

This BGA model is the main package used for simulation but, the HexaSFI study also leads to the use of different packages such as the CSP and the QFP. For a better readability of this chapter, the other package models will be detailed later (cf. sections 3.4 and 3.5).

3.2.3. Board predictive model

To finish this predictive model development, the board model is missing and it is the most complicated to characterize. Indeed, an STM32 is a mass-market product and this means the board's parasitic elements can have any values depending on the customer design. After several tries it appeared that it was not possible to anticipate all of these possible values so the decision was made to develop a simplified board model where values are extracted from a Discovery board with the most optimized connection. Then, coupling factors are considered in the same way as for the package. This model also includes the load capacitor to emulate the external memory connection with a $C_{load} = 6$ pF and a transmission line for each IOs connection, justified in the subsection "3.2.5. Issue with Transmission line". Finally, via are added with the rule 1 via per ball and 1 bypass capacitor of 100nF per power and ground pair.

The final board model is summarized below:

- For each IO , a transmission line defined as follow : $Z = 50 \Omega$ & $TD = 0.35$ ns
- From the bypass capacitor pin connection to the ideal supply:
 - V_{DD_Hexa} to ideal power supply $\Leftrightarrow L_{VDD} = 10$ nH & $R_{VDD} = 0.1 \Omega$
 - V_{SS_Hexa} to ideal ground supply $\Leftrightarrow L_{VSS} = 1$ nH & $R_{VSS} = 0.01 \Omega$
- Via definition : $R_{via} = 0.08$ m Ω & $L_{via} = 1.2$ nH
- Coupling
 - Between two vias for a 0402 capacitor $k = 0.3$
 - Between two vias for a 0201 capacitor $k = 0.35$
 - Between two IOs : $k_{12} = 0.41$ & $k_{13} = 0.27$
 - Between power and ground $k_{PG} = 0.6$
 - No coupling for CLK and nCLK

3.2.4. Issue with coupling factor

The coupling factor in package and PCB was one of the refinements applied on the model. In order to observe the coupling effect a simulation was settled with different k factors as follow:

- $K_{12} = 0.35$; $K_{13} = 0.25$; $K_{14} = 0.2$; $K_{15} = 0.15$; $K_{16} = 0.10$; $K_{17} = 0.08$

In this list, the index number represents the distance between two signals. For example, based on the padding distribution of the HexaSPI, if the observed signal 1 is the clock, then, the coupling between the clock and data 7 or the clock and ground 4 is assimilate to k_{14} . The coupling effect for different k factor is shown in Figure 3-17.

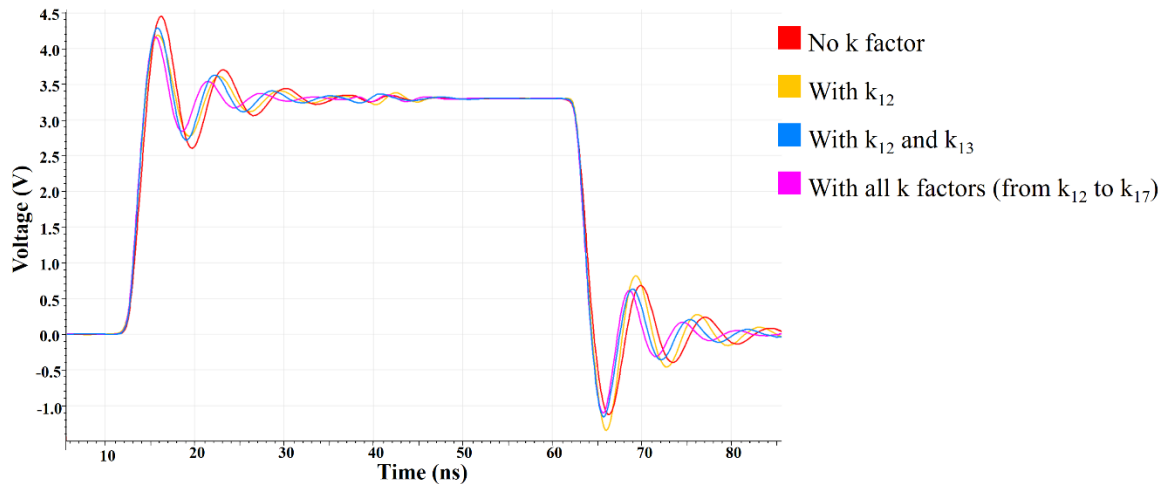


Figure 3-17: Coupling factor effect simulated

The aim of this simulation was to observe the impact of coupling factor and as we can see, there is a difference between no coupling at all and the use of coupling factor. However, an approximation needs to be made in order to lighten the simulation files. From this simulation, we can conclude that only coupling factors k_{12} and k_{13} could be used in the model hypothesis because only a slight difference is observed between the blue and the pink curve. Moreover, it also leads to a PCB recommendation to isolate the CLK and nCLK from other IOs with a “ground shield” in order to protect them of a coupling disturbance because they are the main sensitive signals.

3.2.5. Issue with Transmission line

The transmission line is at the time a model refinement and a guideline applied and was added in the model because the communication didn't meet required specifications. This is illustrated in Figure 3-18 where a simulation is settled at 1.8V for a 200MHz communication. On this figure, we can see that the clock didn't reach the 1.8V for its high state and the crossing between CLK and nCLK is equal to 0.2 V and 1.5V instead of being in specification which is between 0.85 and 1.05V leading to a communication failure.

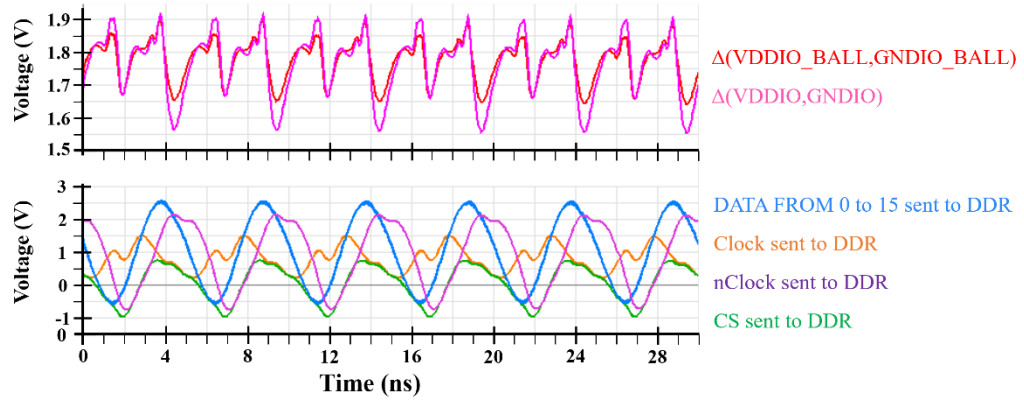


Figure 3-18: Issue observed on clocks crossing without transmission line

This phenomenon was observable even when tracks for IOs connections were considered as ideal. The solution to add transmission line was decided after different tries such as

- Board optimization for supplies with the decrease of parasitic elements values.
- Isolation of CLK and nCLK by removing all coupling factors.
- The addition of a delay between all IOs.

None of these solutions resolved the problem, even if the padding noise level was smaller than 10%. The only working solution found was the use of transmission line (TL) for the PCB. Then, the PCB tracks were refined with a model of a TL provided by Eldo which includes skin effect [72], [73]. Parameters of the TL were defined with an impedance $Z_0 = 50 \, \Omega$ and a time propagation of 350 ps, based on the recommendation found in the JESD 251 standard [71]. The results obtained with the modified model and transmission lines added are shown in Figure 3-19. From this issue, a PCB guideline was added regarding transmission line for IOs connections.

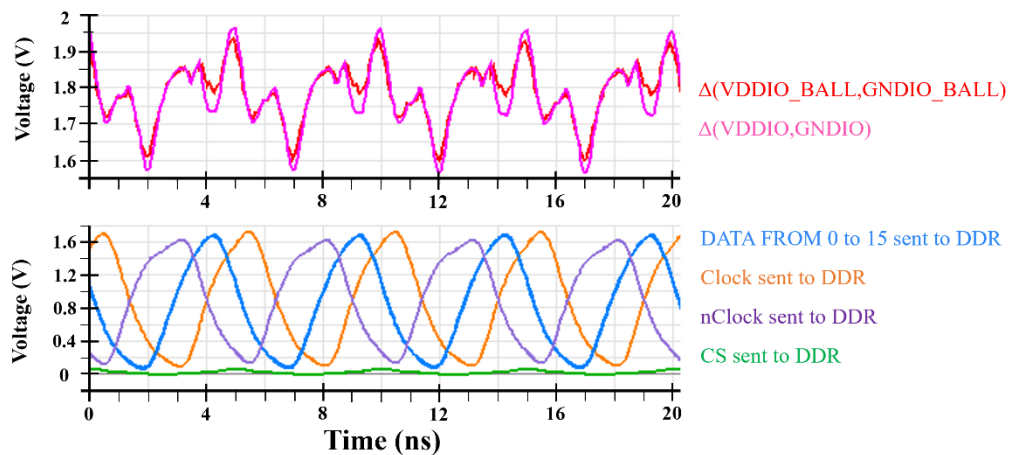


Figure 3-19: Simulation with transmission line to compare with Figure 3-18

3.3. Study at board level

Once this predictive model is finished, the first study was done at board level with a focus on bypass capacitors placement and vias influences. This work was done in cooperation with a PCB designer who provided a first design developed only for power and ground routing, as illustrated in Figure 3-20. We can see on it, 4 V_{SS_Hexa} balls with 7 associated vias and 4 V_{DD_Hexa} balls with 4 associated vias. Then there are four 0402 bypass capacitors of 100nF. To be noted, Figure 3-20 didn't show the different board layers for a better readability, the board is defined by 6 layers with two ground planes on level 2 and 5 and a power trace on level 4.

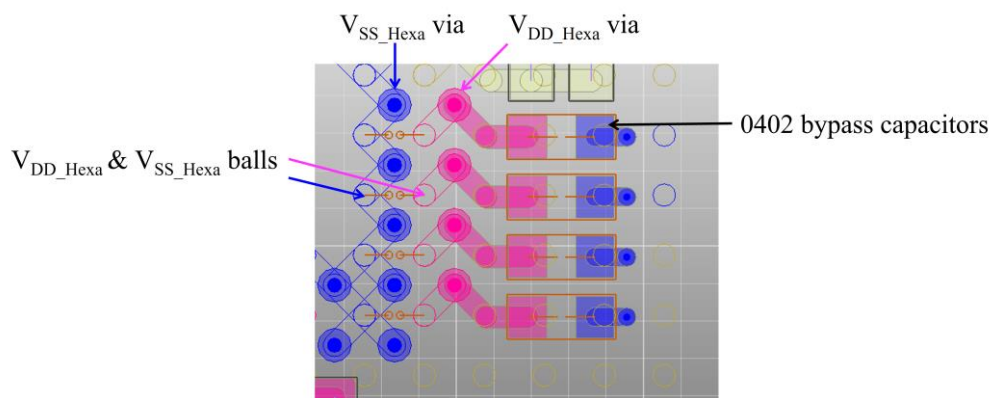


Figure 3-20: 1st board design for the HexaSPI power and ground

The simulation test bench was based on the die and BGA package detailed in the predictive model introduced in sections 3.2.1 and 3.2.2. Then, the PCB model is divided into two parts:

- the power and ground connections are extracted by software from the provided design
- The TL model provided by Eldo is used for all IOs connections.

Moreover, the study was carried on for the full PVT (Process Voltage Temperature) range guaranteed for this MCU and the corner cases are given in Table 3-6.

PVT case	Transistor Process	Voltage (V)		Temperature (°C)
		3.3V	1.8V	
1	Slow-Slow Rmax	2.7	1.62	-40
2	Typical	3.15	1.8	25
3	Fast-Fast Rmin	3.6	1.98	125

Table 3-6: PVT cases used for simulation

With this test bench, we were able to analyze if the communication fit the specifications requirement of the protocol. Table 3-7 summarized the three PVT cases, for a 3.3V supply and a 133MHz communication. In this table $\Delta V = V_{DD_Hexa} - V_{SS_Hexa}$ represents the noise level observed. Values out of specification are highlighted in red.

Parameters	PVT case 1	PVT case 2	PVT case 3
ΔV at padring level	0.44 V	0.75V	0.71V
ΔV at ball level	0.32 V	0.5V	0.53V
Duty Cycle	DTC (CLK) = 51.3 % DTC (IOs) = 50.7 %	DTC (CLK) = 50.9 % DTC (IOs) = 49.3 %	DTC (CLK) = 50.9 % DTC (IOs) = 49.3 %
V_{IL} & V_{IH} at T_{SETUP} & T_{HOLD}	$V_{IL} = 0.65$ V $V_{IH} = 2.1$ V	$V_{IL} = 0.13$ V $V_{IH} = 2.8$ V	$V_{IL} = 0.09$ V $V_{IH} = 3.6$ V

Table 3-7: Summary of specification observed in simulation for the three PVT cases

The noise measured on padring was at the upper limit of the specification, but thanks to simulation we were able to justify the board optimization and especially for vias and bypass capacitors placement. Firstly, capacitors were changed from 0402 to 0201 where 0402 is capacitor of 0.4x0.2mm and 0201 is a capacitor of 0.2x0.1 mm. Their specifications are as follow:

- $C_{0402} = 98.7$ nF & $L_{0402} = 0.276$ nH & $R_{0402} = 19.6$ m Ω
- $C_{0201} = 74.5$ nF & $L_{0201} = 0.2$ nH & $R_{0201} = 35.8$ m Ω

From these specifications, we can see that the capacitor value of 0201 is not equal to 100nF but it is due to its design. However, the impedances profile of the two capacitors are equivalent with approximately the same cut-off frequency as illustrated in Figure 3-21.

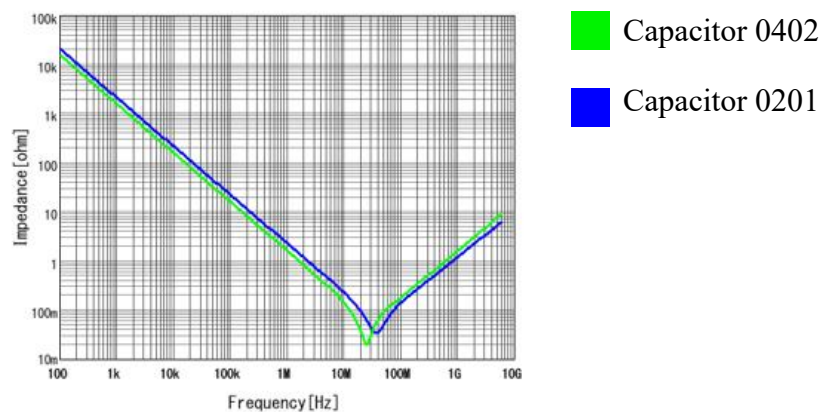


Figure 3-21: Capacitor cut-off comparison between 0402 and 0201

The gain of space thanks to this capacitor modification allowed them to be put them closer to balls and to reduce the associated connection routing. In addition, a vias parallelization has been recommended with 9 V_{SS_Hexa} vias and 9 V_{DD_Hexa} . The final modification concerned the board's layers with a power plane on level 5 and a ground plane on level 2 when before there were two ground planes on level 2 and 5 and only a power trace. The final proposed solution is illustrated in Figure 3-22 with five 0201 bypass capacitors of 100nF.

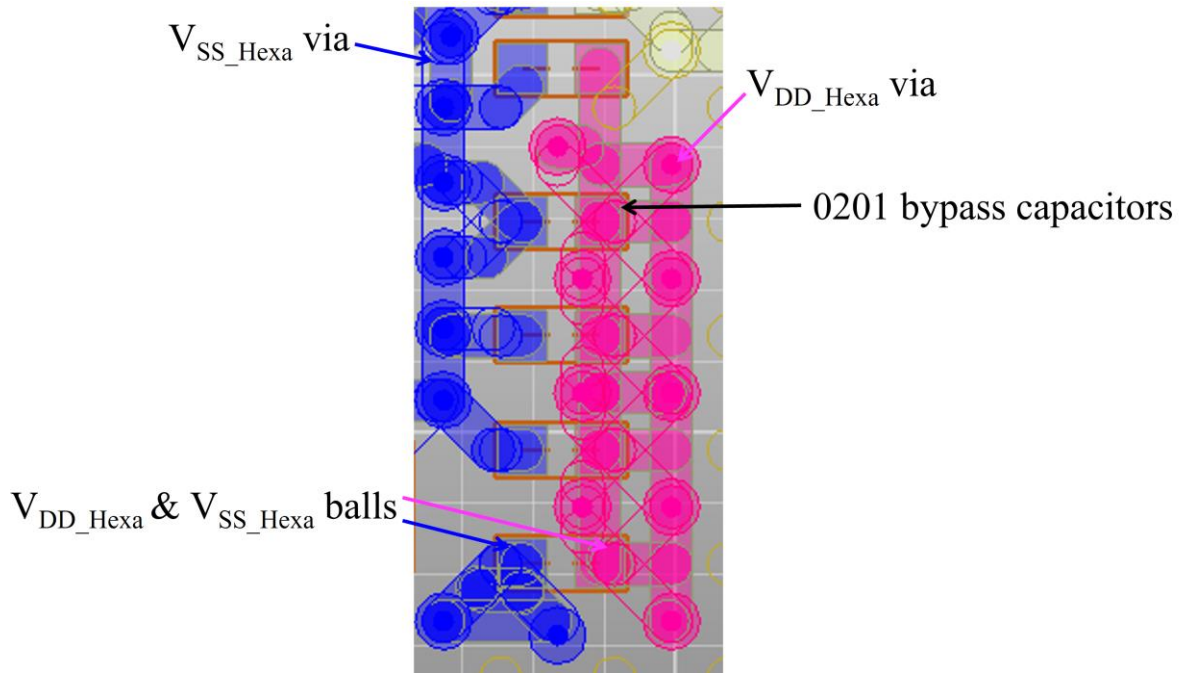


Figure 3-22: Final proposed board design

Table 3-8 summarizes the final values in the three PVT cases for a 3.3V supply and a communication operating at 133MHz in order to compare with Table 3-7. We can see that all parameters respect the specifications and the noise at padding level is reduced more than 26%.

Parameters	PVT case 1	PVT case 2	PVT case 3
ΔV at padding level	0.32 V	0.54 V	0.53 V
ΔV at ball level	0.21 V	0.31 V	0.35 V
Duty Cycle	DTC (CLK) = 50.6 % DTC (IOs) = 51.7 %	DTC (CLK) = 50.9 % DTC (IOs) = 50.2 %	DTC (CLK) = 48.8 % DTC (IOs) = 48.2 %
V_{IL} & V_{IH} at T_{SETUP} & T_{HOLD}	$V_{IL} = 0.7$ V $V_{IH} = 2.2$ V	$V_{IL} = 0.15$ V $V_{IH} = 2.8$ V	$V_{IL} = 0.1$ V $V_{IH} = 3.6$ V

Table 3-8: Summary of final values obtained with the board re-designed

3.4. Study at package level

The second work completed with this predictive model was at package level with a study of two CSP design. The purpose here was to determine if the package might be designed with a package of one or two layers. A one layer package is cheaper than a 2-layer one but implies more constraints on the package routing and reduces the balls capability. This study was done in cooperation with a package designer who provided the two package layout shown in Figures 3-23 and 3-24. The first picture shows the 1 layer package with, in blue the V_{SS_Hexa} , in orange the V_{DD_Hexa} , in yellow CLK/nCLK and in pink all other data connections. The second picture shows the 2 layers package with, in blue the V_{SS_Hexa} , in pink the V_{DD_Hexa} , in yellow CLK/nCLK and in purple all other data connections. As we can see on these two figures, the 2-layer package allows a better connection for power and ground but also to allows smaller routing for the clocks, as recommended in the predictive model development.

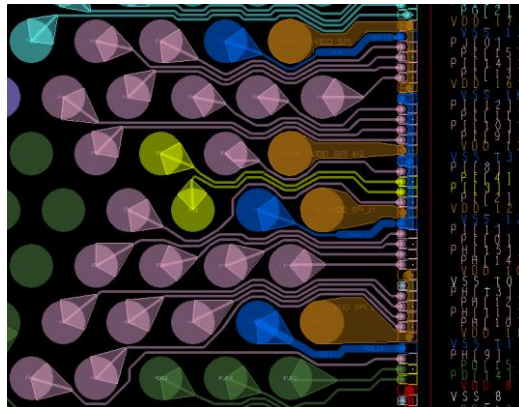


Figure 3-23: CSP design with 1 layer

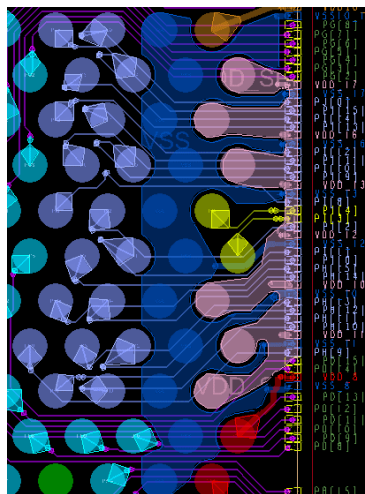


Figure 3-24: CSP design with 2 layers

In order to compare these two packages, the simulations were mainly focused on the number of balls. For that, parameters defined in the predictive models are used for the die, transmission lines and vias model and the two packages are modeled with software extraction. Moreover, to have a better idea of the package influence, the board power supply is assumed ideal – no parasitic elements for V_{DD_Hexa} and V_{SS_Hexa} on the board-. Finally, two setups are settled:

- Setup 1: Vias are added identically on both packages:
 - 4 via from $V_{DD_Hexa_Ball}$ to an ideal 3v15
 - 3 via from $V_{SS_Hexa_Ball}$ L to an ideal 0
- Setup 2: Via are added following ball numbers :
 - 4 $V_{DD_Hexa_Ball}$ via and 3 $V_{SS_Hexa_Ball}$ via for the 1 layer
 - 6 $V_{DD_Hexa_Ball}$ via and 11 $V_{SS_Hexa_Ball}$ via for the 2 layers

Simulations are settled for these two setups and on both packages. Tables 3-9 and 3-10 summarized the communication specification from these two setups with a communication established at 3.3V, in typical process and ambient temperature and operating at 133MHz.

Parameter	CSP 1 Layer	CSP 2 Layer
ΔV at padring level	0.615 V	0.55 V
ΔV at ball level	0,475 V	0.52 V
Duty Cycle	DTC (CLK) = 50.9 % DTC (IOs) = 48.7 %	DTC(CLK) = 50.8 % DTC(Ios) = 48.5 %
V_{IL} & V_{IH} at TSETUP & THOLD	$V_{IL} = 0.02$ V & $V_{IH} = 3.1$ V	$V_{IL} = 0$ V & $V_{IH} = 3.1$ V

Table 3-9: Specification comparison of the two packages for setup 1

Parameter	CSP 1 Layer	CSP 2 Layer
ΔV at padring level	0.615 V	0.37 V
ΔV at ball level	0.475 V	0.32 V
Duty Cycle	DTC (Clk) = 50.9 % DTC (IOs) = 48.7 %	DTC(CLK) = 50.7 % DTC(IOs) = 49.8 %
V_{IL} & V_{IH} at TSETUP & THOLD	$V_{IL} = 0.02$ V & $V_{IH} = 3.1$ V	$V_{IL} = 0$ V & $V_{IH} = 3.1$ V

Table 3-10: Specification comparison of the two packages for setup 2

Table 3-9 demonstrates the utility to have a 2-layers CSP in order to optimize power and ground connections and Table 3-10 demonstrated again the via influence. Based on these simulations, the final choice for the CSP package was to choose the 2 layers one, in order to optimize the internal routing and to allocate more balls to supply with a guideline for customer; one via per ball because this recommendation is easier and cheaper to apply than vias parallelization.

3.5. Study at die level

The board optimization was done for the Discovery board designed by STMicroelectronics but we have to reminder that an STM32 is a mass-market product. This means it is up for the customer to do the board design and, even if we give recommendations, all PDN could not be anticipated. Then this final solution proposed is to add a bypass capacitor directly at die level to decouple as close as possible to the noise origin. Nevertheless, solution this requires more space in the die so it must be strongly justified. This capacitor was designed with MOS transistors for a total area of 3000x49um. Its maximum value is reach for 700pF. Moreover, three control bits are used to allow customer to program this capacitor in function of its board PDN as follows :

- Capacitor OFF
- Capacitor ON with 1/3 of its value (233 pF)
- Capacitor ON with 2/3 of its value (466 pF)
- Capacitor ON with its full value (700 pF)

To observe this capacitor effect, a simulation was done in frequency and time domain, still with the predictive model introduced in section 3.2 for die, package, and board. To be noted, the vertical axis defines the magnitude in decibel-Ohm (dBΩ), to convert the value in Ohm, the Equation 2-1 must be used.

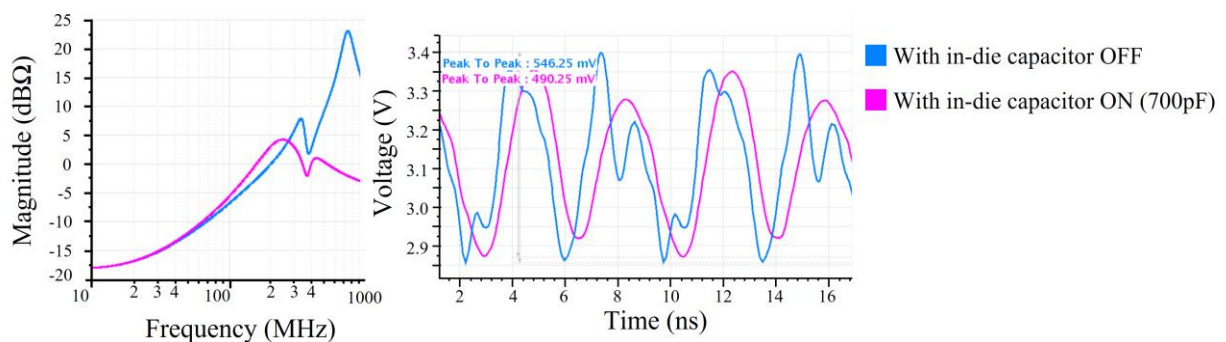


Figure 3-25: Simulation in frequency and time domain, with in-die capacitor OFF and ON

The AC simulation shows the improvement of the power supply network with an important decrease of its impedance after 300MHz. This simulation also shows a slight increase in impedance between 100MHz and 300MHz which corresponds to the operating range of the HSPI communication. These observations are confirmed with transient simulation where noise at padding level is only reduced by approximately 60 mV. However, 60 mV represents a 10% decrease in the noise level, and this, with a predictive model where the communication is already guaranteed and the board optimized.

In order to confirm the impact that this capacitor could have, the same simulations were done in frequency and time domain but this time, the predictive model is modified with a QFP package instead of BGA. For that, from the BGA model, we modified parasitic elements of all connections with $L = 5 \text{ nH}$ & $R = 0.3 \Omega$.

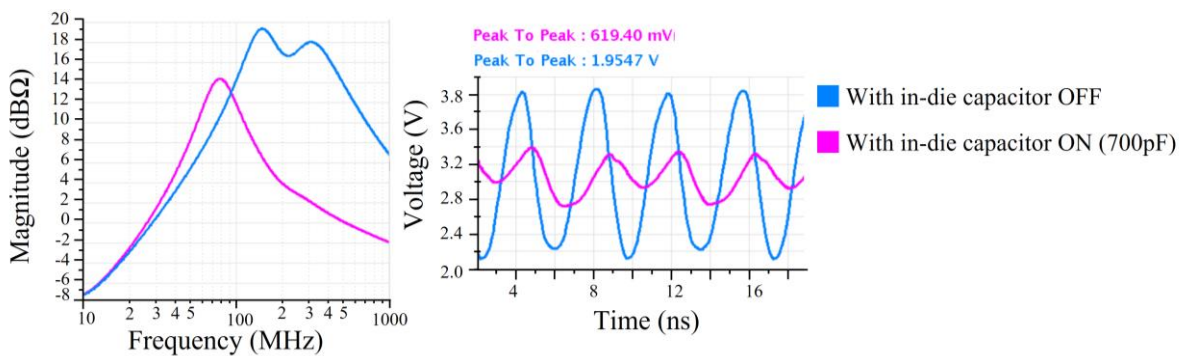


Figure 3-26: Observations of the in-die bypass capacitor effect with simulations in the frequency and the time domain

This time, the in-die capacitor has an important impact on the circuit PDN. From the AC simulation, we can see an important decrease from 100MHz and this correlates with the transient simulation where the noise at padding level is reduced by 3 with a peak-peak of 1.95V with the capacitor OFF and a peak-peak of 0.62V for a capacitor ON so a noise reduction of almost 70%.

3.6. STM32 produced and predictive model refinement

Once the product was manufactured, it provided the opportunity to confirm the predictive model by comparing the simulations with measurements, still by following the same validation process introduced in chapter 2. The only product available for measurement was a discovery board developed for this STM32 with a BGA package. Once the validation methodology applied, it appears that the model needs to be refined for the five points as developed below.

Firstly, a simulation extraction with Siwave of parasitic elements for package and board was made simultaneously in order to have a better model of the 50Ω transmission line. For that, the package was virtually mounted on the PCB and only one extraction was done to model the whole PDN from the die's pad to the external component such as the external memory and the ideal power supply. The advantage of this simulation is to include the package connection in the transmission line where, in the predictive model, the transmission line was directly defined at PCB level without taking into account the package impedance.

Secondly, and as reminder, we decided to shunt the HexaSPI power supply lines from the rest of the padding to isolate both of them from the SSN effect. Then, these supplies had their own ball connections also isolated. The unexpected case, due mainly to a lack of communication between teams was the merging of all supplies at board level. Indeed, the PCB didn't dissociate the different supplies but merged all of them with one ground plane and one power trace. This had two consequences.

- We had to do an extraction of the complete board -still with the package virtually mounted on it-. This model took into account all supplies with their associated bypass capacitors.
- The die model had to be refined with the extraction of the padding capacitance computation connected to its own metallic rails and balls but merged at ball level.

Thirdly, a problem was encountered during measurement because it was an optimized board. Indeed, there is no measurement points for signal or power observation. The validation process was done by scratching IOs tracks on the PCB, modifying at the same time the adapted line. Consequently, we modified the board model and recreated these measurement points for its extraction.

Fourthly, another modification applied on the predictive model was regarding the communication protocol itself. In the predictive model, the communication was settled with the 16 synchronous switching IOs but it was not the case with the external memory connected to this board.

Finally, the abacus of load capacitance in function of the IOs rising and falling time was done in simulation to figure out that the load capacitor was equal to 3pF instead of the 6pF defined in the predictive model, also due to this external memory.

Once the model was refined, the final comparison between simulation and measurement is presented in Figure 3-27 where a switching IO for a 1.8V supply, operating at 160MHz is shown.

The signals observations are:

- Measurement : $V_{\text{peak-peak}} = 770\text{mV}$ & $F_{\text{resonance}} = 345\text{MHz}$
- Simulation : $V_{\text{peak-peak}} = 750\text{mV}$ & $F_{\text{resonance}} = 380\text{MHz}$

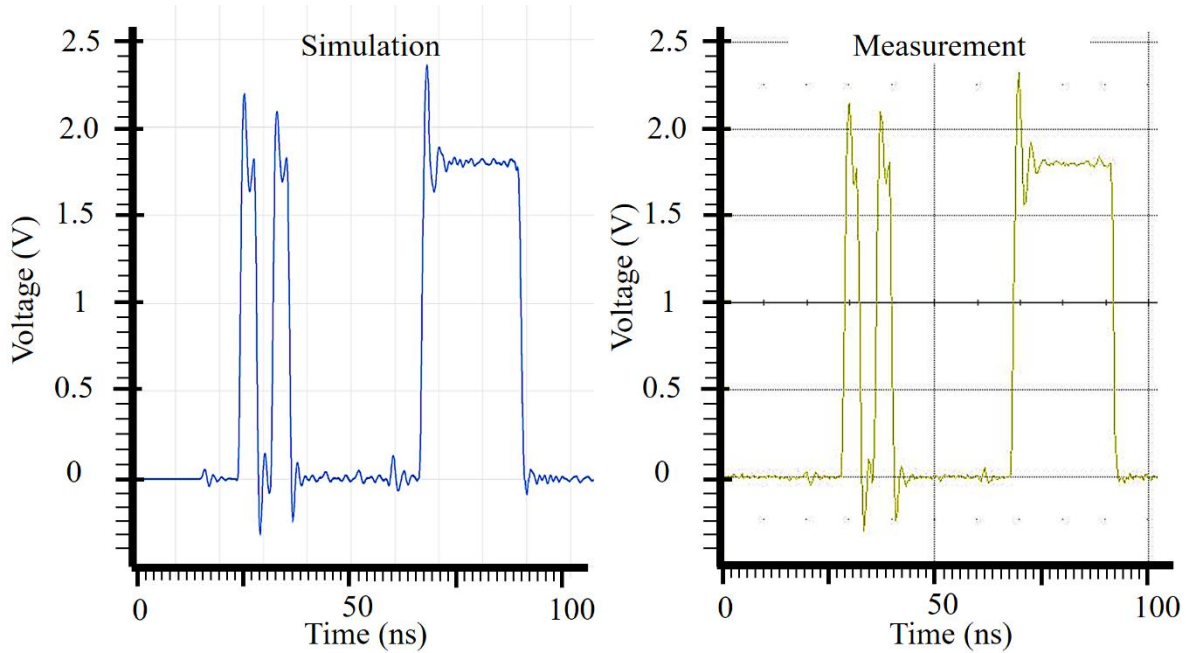


Figure 3-27: Comparison between simulation and measurement of the refined model

These results demonstrate a good agreement between the final simulations and the measurement and validate the global methodology proposed (model development, comparison, and refinement).

3.7. Conclusion

We can start the conclusion of this chapter by resuming solutions applied thanks to the predictive model. These solutions are:

- The guideline for the customer to develop their PCB with a 50Ω adapted line on each IO's output. Obviously, these adapted lines were also added to the board developed by STMicroelectronics.
- The board studied with this predictive model, in cooperation with the board designer (i.e. the discovery board), was modified regarding the optimization of vias and bypass capacitors placement. To note, this solution was not applied on the first version of the

discovery board because it was not compatible with the use of a socket. A socket is necessary for first tests because it allows to insert and remove the chip without the use of a soldering iron. This solution might be applied on the next board revision.

- The CSP with 2 layers has been characterized by the company and is now the “official” package used for this product but also for all the future ones -instead of the package CSP 1 layer-.
- The in-die bypass capacitor was added as explained previously.

Regarding this in-die bypass capacitor, once the product was manufactured, it offered the possibility to measure the impact of this capacitor. The conclusion observed from measurements is there was no difference -or only a few mV- observed in the noise amplitude whether the capacitor was OFF or ON and equal to 1/3 or 2/3 or 3/3 of its total value. To remind, from firsts simulations, we expected only a slight noise reduction -around 50mV- with the BGA package thanks to this capacitor. However, with all parameters refined, the noise level is smaller than predicted, due to different parameters. In first, the communication was modified which decreases the noise generated. Secondly, the board was much more optimized than predicted, due to the merging of all power supplies at board level. Nevertheless, this “no difference” observed in measurement is also found in simulation and justified by these refined parameters and this noise smaller than expected.

To conclude this chapter, this predictive work was really useful to anticipate the MCU behavior directly at the design stage and helped to modify package and board design, to add an in-die bypass capacitor but also to develop some guidelines in order to improve the MCU robustness. This model had to be refined regarding a few points as the board modification or the communication established but we can say that more of these refinements were due to a lack of communication with other teams than due to a wrong hypothesis. Then, procedure to develop such model can be kept and reused for future products. Finally, it must be highlighted that absolutely no issues were found at the qualification stage of the MCU and especially for this communication that has never been done by our team. It is now a product which is released on the market. This product is highly competitive, without any feedback issues from customers.

General conclusion and perspectives

Despite the many advantages of the MCU, they have become more and more sensitive in terms of electromagnetic compatibility. The evolution of CMOS technology, the systems miniaturization, the increase in the number of transistors, the operating frequency and the general MCU complexity are at the origin of a higher electromagnetic emission and a lower susceptibility threshold. It is now essential to study and predict the EMI propagation and the EMS of a device, in order to anticipate a failure and avoid costly redesign phases. In this context, we tried to contribute, from the design phase of MCU to the best consideration of the auto-susceptibility problem created by the Simultaneous Switching Noise. This study is part of a CIFRE thesis between Polytech'lab and STMicroelectronics and was developed through three chapters in this manuscript.

The first chapter was focused on the SSN origin. For that, an attention was given to the CMOS technology and MCU evolution aiming to justify the study of this auto-susceptibility problem. Then, this chapter defined the EMC problematic in the MCU domain in order to better understand how the SSN effect is contributing to it. We also examined the state of the art on the SSN subject itself, starting with the origin and the CMOS inverter behavior and finishing with the highlight of SSN phenomenon at the MCU level.

The second chapter is dedicated to a modeling methodology in order to study the SSN effect only by simulation. The model creation is based on the ICEM-CE standard provided by the IEC company and considers a complete system with the die and the IOs padding, the package and the associate PCB. To remind, there are other standards developed for the system modelling as the IBIS IMIC. We decided to work with the ICEM standard because it takes into account signal integrity as well as power integrity. Moreover, this standard considers the power supply degradation due to the internal activity as well as the effect of this degradation on the IO's behavior which is not the case with other ones as the IBIS standard. To resume, this standard is the most complete solution to study the SSN effect. For an accurate understanding of this standard, we detailed all steps to create an electrical model either by hand calculation or by software extraction. Finally, this chapter explains a validation process based on comparison between measurements and simulations in order to guarantee the model behavior accuracy in terms of SSN effect.

The third chapter is dedicated to results and conclusions achieved throughout this thesis and is divided into two main parts. The first part was dedicated to a 1st DUT studied because an MCU issue appeared at the qualification stage due to the TFT-LCD communication. For that, the methodology detailed in chapter 2 was applied in order to investigate the problem in simulation. So, after the model development and validation, we understood which parameters were influencing the SSN with the highlight of vias impact and the advantages of SiP capacitors embedded in a package. To remind, the solution of the BGA package that embeds SiP bypass capacitors was not kept due to the price of this solution being judged too expensive. Despite the advantage of these SiP capacitors, the fact that we didn't use it, reminds us that this thesis was carried out in the constrained environment of the STM32. This MCU is a mass-market product and because of this, the product must remain small and cheap to be competitive on the market. Nevertheless, this work helped to find other solutions with the re-design of IOs in order to reduce the generated noise and the board optimization based on our simulation conclusions. Nowadays, this MCU was qualified and commercialized and no issues due to the SSN effect are observed anymore.

The second part was dedicated to the development of a predictive model for a high-data rate communication with an external memory named HexaSPI. The purpose of this work was to ensure the MCU robustness by anticipating its behavior. The model was developed based on specific knowledge acquired during this thesis and methodology of chapter 2. Through its development, first guidelines were introduced with the transmission line and the coupling isolation of the two clocks. This model was then used to optimize board and package design directly at the design stage with a cooperative work with designers. Finally, simulation from this model was used to justify the addition of an in-die capacitor to decouple the disturbance as close as possible to the EMI generation. This controllable capacitor is an added value to the product robustness because, the STM32 is a mass market product and it allows adaption of the power supply network according to the board characteristics designed by the customer. This model was validated through the validation process developed in chapter 2 and some refinements were applied to it, mainly due to a lack of communication between different teams. Nevertheless, the product qualification demonstrated a strong robustness of the product regarding the HexaSPI communication and it is now one of the market leader products used in smart-watches. This work then answered to the original problematic; be able to predict the MCU behavior directly at the design stage in order to find the solution that will suit the environmental constraints of the SM32.

As a matter of fact, new research perspectives can be developed from this work. The first one is to compete the already created and functional package by reducing the power and ground balls thus allowing more connections for IOs or reducing the package size thanks to in-die bypass capacitor and leading to improve market competitiveness. The second area of research concerns the use of QFP packages for high-speed communications in particular for the HSPI communication. For the moment, the performance of the HSPI is not guaranteed on the QFP due to its large value of parasitic elements. However, we have demonstrated in chapter 3 the impact that the in-die capacitor could have on the SSN for this type of package. Thanks to these simulations, future proposed products will incorporate HSPI communication in QFPs and we will be able to observe the capacitor effect in measurement but for sure, its robustness will be improved.

We will conclude this manuscript with some “gold rules” observed during this thesis to limit the SSN effect and improve the MCU robustness.

First, at the die level the di/dt defined the current variation generated by a switching IO might be reduced to a maximum with an optimization of the design. Then, an in-die bypass capacitor might be used for high data rate communication to have this decoupling effect as close as possible to the source of the interference.

Secondly, at the package level, an optimized package should always be favored. Indeed, CSP package involves smaller parasitic values than QFP or even BGA for example.

Thirdly, at the board level, a transmission line must be used for high data rate communication. Obviously, planes for power and ground plane will have a positive impact on noise reduction. Finally, we demonstrate the importance of the bypass capacitor placement as well as the influence of vias on the noise level. These are two rules that must be strongly emphasized because they are too often neglected.

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International conferences

1. M. Moign, J.-P. Leca, N. Froidevaux, G. Jacquemod, Y. Leduc, "Analysis, modelling and measurement of the SSN effects on an integrated circuit", IEEE EMC Magazine, 2022
2. M. Moign, J.-P. Leca, N. Froidevaux, G. Jacquemod, Y. Leduc, "Impact of bypass capacitors placement on SSN in an MCU based system : Modeling and measurement", EMC Compo, Haining, Hangzhou, China 2019
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4. M. Moign, J.-P. Leca, N. Froidevaux, G. Jacquemod, Y. Leduc, H. Braquet "Impact des vias et du placement des capacités de découplage sur le bruit à commutation simultanée au sein des microcontrôleurs 32 bits", XXIIèmes Journées Nationales Microondes, Limoges, Juin 2022
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