



# Space Charge Doped p-n Junction: 2D Diode with Few-layer Indium Selenide

Wenyi Wu

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Sorbonne Université

Physique et Chimie des Matériaux (ED397)

*Institut de minéralogie, de physique des matériaux et de cosmochimie*

**Space Charge Doped  $p$ - $n$  Junction: 2D Diode with  
Few-layer Indium Selenide**

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Thèse de doctorat de physique

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# Abstract

## English version

This work combines the singular properties of 2D materials with an innovative technique used for changing the electronic properties of ultra-thin films to propose a new technology for making the simplest bipolar electronic device, the diode. Firstly we identify semiconducting materials which can be fabricated in ultra-thin layers. Secondly, we use a proprietary technique called Space Charge Doping developed in our group for doping the material, either  $n$  or  $p$ . Finally, we obtain diode characteristics from the device. The manuscript begins with a review of different materials and properties. In the family of 2D materials, our choice was a *III-VI* layered semiconductor with a direct bandgap: InSe. We also chose a completely different kind of material, polycrystalline CdO, which is neither layered nor has a direct bandgap but is easy to fabricate in the ultra-thin film form and has high carrier mobility. After preliminary experiments, we chose InSe and fabricated devices of ultra-thin, few atomic layer InSe thin films. We chose to develop in parallel two different geometries for the  $p$ - $n$  junction diode. We were able to obtain rectifying behavior for each geometry implying that our space charge doping approach was successful in producing microscopically, spatially differentiated doping in each device. We discuss the obtained  $I$ - $V$  characteristics and the inherent limitations of the devices (local heating, hysteresis) and suggest improvements for future experiments and ways of obtaining more efficient and stable functioning and geometry as part of the perspectives of this thesis.

## Version française

Ce travail allie les propriétés singulières des matériaux 2D à une technique innovante utilisée pour modifier les propriétés électroniques des films ultra-minces pour proposer une nouvelle technologie permettant de réaliser le dispositif électronique le plus simple, la diode. Tout d'abord, nous identifions les matériaux semi-conducteurs pouvant être fabriqué en couches ultra-minces. Deuxièmement, nous utilisons une technique appelée dopage par charge d'espace développée dans notre groupe pour le dopage  $n$  ou  $p$  des matériaux. Enfin, nous obtenons les caractéristiques de diode des dispositifs. Le manuscrit commence par une revue des matériaux. Dans la famille des matériaux 2D, notre choix s'est porté sur un semi-conducteur en couches  $III-VI$  avec une bande interdite directe : InSe. Nous avons aussi choisi un type de matériau très différent, le CdO polycristallin qui n'est pas lamellaire et n'a pas une bande interdite directe, mais qui est facile à fabriquer sous forme de film ultra-mince avec une grande mobilité de porteurs. Après des expériences préliminaires, nous avons choisi InSe et fabriqué des dispositifs de films ultra minces de InSe. Nous avons développé en parallèle deux géométries pour la diode p-n. Nous avons pu obtenir un redressement pour chaque géométrie, ce qui implique que notre approche de dopage par charge d'espace a réussi à produire un dopage différencié spatialement dans chaque dispositif. Nous discutons des caractéristiques  $I-V$  obtenues et les limitations inhérentes aux dispositifs (chauffage local, hystérèses) et suggérons des améliorations afin d'obtenir un fonctionnement plus efficace et stable dans le cadre des perspectives de cette thèse.

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# General introduction

This thesis combines the singular properties of 2D materials with an innovative technique used for changing the electronic properties of ultra-thin films to propose a new technology for making the simplest bipolar electronic device, the diode. The diode is the workhorse of modern-day electronics but also the device which when made with materials with high light-emitting efficiency and a direct band gap (light-emitting diode, LED) can be used for producing light in an energy-efficient way. It is estimated that one fourth of the earth's energy consumption is for lighting purposes and that LED's can result in energy savings of more than an order of magnitude with respect to regular light bulbs since they convert electrical current to light much more efficiently[1]. The Nobel committee recognized this in awarding the 2014 Nobel prize in Physics to Akasaki, Amano and Nakamura for their invention of the blue LED. Light from LED's is typically in a small spectral range when compared to light from a tungsten filament standard light bulb, because it originates in an electronic transition synonymous with the (direct) band-gap of the semiconductor material of the underlying diode. Until the Nobel invention, LED's on the blue side of the spectrum were lacking, making it impossible to use LED's producing white or yellow light. This lack of blue LED's was due to the difficulty of producing a diode from a material with a band-gap in the range of blue light. A diode, as we shall see below is made of a bipolar junction between two regions of a material in which one region has majority carriers which are holes ( $p$ ) and the other regions which has majority carriers which are electrons ( $n$ ). If the band-gap of the underlying material is direct, one can expect emission of light at the band-gap energy when current flows through the junction and results in the recombining of holes and electrons. So two elementary requirements for the LED are a material which



1. has a direct band-gap in the required energy range
2. can be doped both  $n$  and  $p$

As can be seen through the story of the blue diode each of these can be a very difficult problem. While engineering band gaps has been an integral part of the semiconductor revolution, it was a challenge to find a material with a large direct band gap. GaN filled this void but the next problem was to dope GaN with  $p$  and  $n$  type of carriers. This doping is routinely accomplished chemically in semiconductors using impurities which are not iso-electronic with the host material, introducing free holes or electrons. However bipolar doping has been a recurrent problem in solid state chemistry and physics. For a variety of reasons it is easy to dope materials with one type of carriers (usually  $n$ , in many simple oxides, as seen for example in the wide gap semiconductor ZnO) but nearly impossible to dope with the other type of carriers. This has limited the optoelectronic impact of semiconductor devices and overcoming this difficulty in GaN was important enough to merit the Nobel prize.

In this work we make first steps to attack these problems through a different approach. Firstly, we use the enormous amount of work and knowledge compiled in the last few years in the field of 2D materials to identify materials with a (direct) band-gap which can be fabricated in ultra-thin layers through exfoliation. Secondly, we use a proprietary technique called Space Charge Doping (SCD) developed in our group for doping the material either  $n$  or  $p$ . This technique is electrostatic in nature and fundamentally differs from chemical doping. It is applied directly to the device made from an ultra-thin layer on a glass substrate. Finally, we obtain diode characteristics from the device. Time limitations and other difficulties and constraints encountered prevented us from verifying the light emission properties of our device.

In chapter 1 we introduce the elementary equations and physics encountered in a  $p$ - $n$  junction diode. We then give a brief introduction to relevant 2D materials. We finish with a brief review of some relevant devices of 2D materials.

In chapter 2 we take an in-depth look at the technical aspects of this work. We describe in detail the methods of fabricating our ultra-thin samples and the space charge doping method. We also detail the main characterization methods involved, including Raman spectroscopy, atomic force microscopy and X-ray diffraction. We describe the device fabrication methods which take into account the nature and sensitivity of the chosen materials. Finally, we describe the transport methods used to measure and characterize our devices.

In chapter 3 we describe the materials used in this thesis. In the family of 2D materials our choice was a *III-VI* layered semiconductor with a direct band gap: InSe. We also chose a completely different kind of material, polycrystalline CdO which is neither layered nor has a direct band-gap, but is easy to fabricate in the ultra-thin film form and has a high mobility. CdO was chosen as an eventual fall-back solution in case InSe devices failed to work, and as will be seen, this was not the case. We close this chapter by explaining the final choice of InSe.

In chapter 4, we show the main experimental results of our thesis on devices of ultra-thin, few atomic layer InSe thin films. We chose to develop in parallel two different geometries for the  $p$ - $n$  junction diode. We were able to obtain rectifying behavior for each geometry implying that our space charge doping approach was successful in producing microscopically differentiated doping in each device. We discuss the obtained  $I$ - $V$  characteristics and the inherent limitations of the devices (local heating, hysteresis).

Finally, in chapter 5, we summarize the results of this thesis and suggest improvements for future experiments. This work has laid the foundations for

obtaining light emission from such devices and also obtaining more efficient and stable functioning and geometry. These perspectives are discussed.

# Chapter 1.

## Introduction to the $p$ - $n$ junction and two-dimensional materials

### 1. 1 $p$ - $n$ junction

$p$ - $n$  junctions are fundamental in modern electronic applications and in understanding other semiconductor devices. The  $p$ - $n$  junctions theory serves as the foundation of the physics of semiconductor devices. The term diode always means a semiconductor device, adequately known as the  $p$ - $n$  junction diode. The developments of transistor and solar cells are also based on the discovery of  $p$ - $n$  junction.

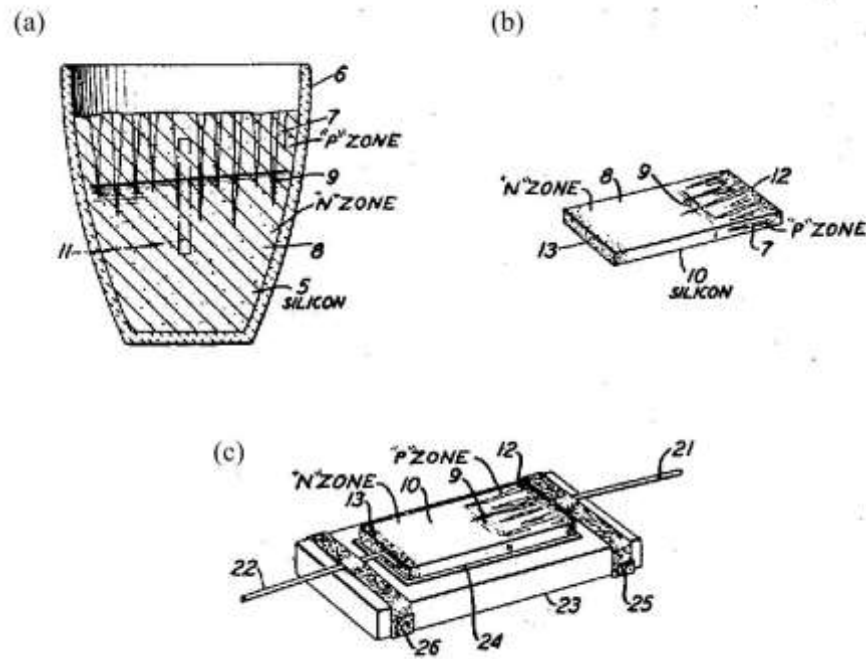


Figure 1.1 (a) shows in cross section an ingot of fused silicon within a silica crucible from which ingot material may be cut for the original invention of the  $p$ - $n$  junction. (b) illustrates the device of another form cut from the ingot of (a). (c) shows the cell of (b) in a modified form of mounting. Reprint from reference [2].

In 1939, the  $p$ - $n$  barrier was discovered by Russell Ohl at Bell Labs[3]. On one Si wafer, two parts containing different impurities were found. Ohl and his colleagues found contrasting electrical properties near the boundary separating these regions of the crystal. The first impurity was phosphorus, which generated a slight excess of electrons as carriers in one region of the sample; the other impurity was boron, which created a slight deficiency of electrons in the other region. They defined the regions  $n$ -type (for negative) and  $p$ -type (positive) regions; the interface where these regions met became known as the " $p$ - $n$  junction." Light striking this junction stimulated electrons to flow from the  $n$ -side to the  $p$ -side, resulting in an electric current. Thus, even before significant knowledge existed about dopants and their behavior in a semiconducting crystal,

electrochemists already described  $p$ - $n$  junctions and developed related silicon photovoltaic devices.

The basic theory of current-voltage characteristics of  $p$ - $n$  junctions was established by Shockley. This theory was then extended by Sah, Noyce, and Moll. An original  $p$ - $n$  junction model is a two-terminal device, with a boundary or interface between two types of semiconductor materials,  $p$ -type and  $n$ -type. When the  $p$ -type and  $n$ -type semiconductors are in contact, the carriers in the two parts have a distribution gradient due to their changing concentration, and the carriers will diffuse toward the other part. As a result, the opposite sign of the ionized charge is left in the region, thus forming a built-in electric field with the corresponding region across the junction. The built-in electric field also induces a drift motion for carriers. The direction of drift is opposite to that of diffusion due to the concentration gradient. In the absence of an external field, diffusion and drift of carriers will reach a state of dynamic equilibrium, forming a ‘space charge’ in the region of the junction.

Considering the thermal equilibrium condition without applied voltage or current, from the current equation of drift and diffusion, the total electron current  $J_n$  flowing through the  $p$ - $n$  junction should be equal to the drift current density of electrons

$$q\mu_n n \mathcal{E} \tag{1.1}$$

with diffusion current density  $q\mu_n \frac{kT}{q} \frac{dn}{dx}$  (in a one-dimensional along the  $x$  direction)

$$J_n = 0 = q\mu_n \left( n\mathcal{E} + \frac{kT}{q} \frac{dn}{dx} \right) = \mu_n n \frac{dE_f}{dx} \tag{1.2}$$

Similarly, the hole current density is

$$J_p = 0 = \mu_p p \frac{dE_f}{dx} \quad 1.3$$

The above two formulas also represent the relationship between the change in Fermi level with position and current density. For the equilibrium state of the *p-n junction*,  $J_n$  and  $J_p$  are both equal to 0. So  $\frac{dE_f}{dx} = 0$ ,  $E_f$  is a constant.

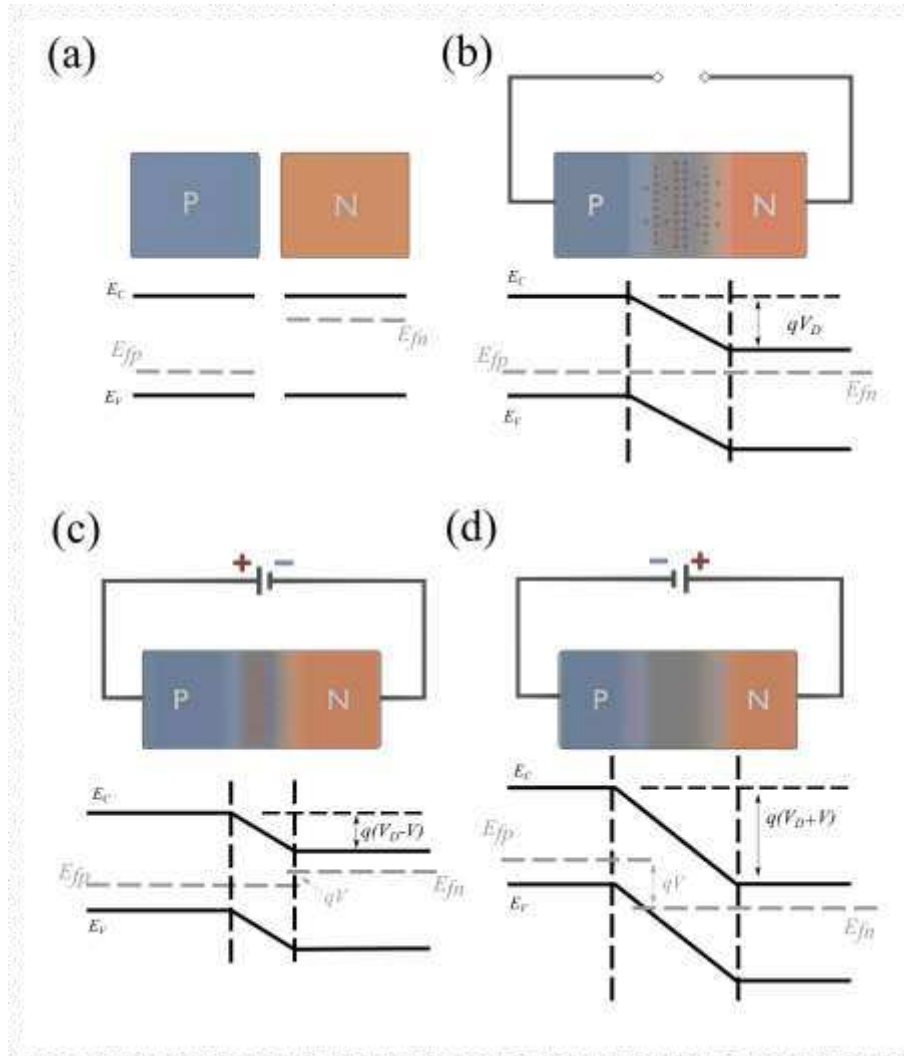


Figure 1.2 Effects of bias at a *p-n junction*. (a) For different semiconductor types, the Fermi level of the *p*-type semiconductor is closer to the valence band, and the Fermi level of the *n*-type semiconductor is closer to the conduction band. (b), (c) and (d) respectively show the changes of the internal

transition region width and electrical field of the  $p$ - $n$  junction under different bias states.

Due to the change in potential energy in the space charge region the energy bands change along the direction of the junction. This bending of the valence and conduction bands affect the electronic motion in the semiconductor. When an electron moves from the  $n$ -region with low energy to the  $p$ -region with high energy it has to overcome a "high slope" to reach the  $p$ -region. Similarly, holes must overcome this "high slope" of potential energy when going from the  $p$  to the  $n$  region. This is referred to as the barrier of the  $p$ - $n$  junction. The barrier height is equal to built-in potential created by the space charge at the junction.

Another intuitive way of understanding this is to consider two separated pieces of a semiconductor, one  $n$ -doped and the other  $p$ -doped. The Fermi level in the  $n$ -doped semiconductor is close to the conduction band, while the Fermi level in the  $p$ -doped semiconductor is close to the valence band. While connecting the two pieces together in a thought experiment, the Fermi level equalize thus shifting the bands up on the  $p$ -side, and down on the  $n$ -side. The value of the built-in potential  $V_D$  is given by the band shift as shown in Figure 1.2

When an external voltage is applied, the  $p$ - $n$  junction is in a non-equilibrium state. The external voltage is applied in the forward direction when the positive electrode of the power supply is connected to the  $p$ -side of the junction and the negative electrode to the  $n$ -side. The reverse direction is the opposite. As shown in Figure 1.2 and Figure 1.3, when applying a forward bias the external potential essentially decrease the barrier height, allowing more current to flow through the junction. Inversely, a reverse bias increases the barrier height, preventing flow of majority carriers.



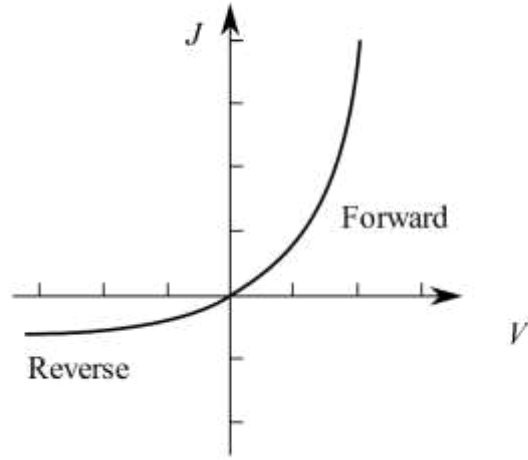


Figure 1.3 Schematic of ideality *p-n* junction *I-V* characteristic.

The total current is described by the Shockley equation, which is the ideal diode law.

$$J = J_p + J_n = J_0 \left( \exp \left( \frac{qV}{nkT} \right) - 1 \right) \quad 1.4$$

Where  $J_0$  is recombination current or saturation current,  $V$  is the externally applied bias,  $k$  is Boltzmann constant,  $n$  is known as the ideal diode factor. In the forward direction (positive bias on the *p*-side) for  $V > 3kT/q$ , the current density increases exponentially with the bias. Generally,  $\exp \left( \frac{qV}{kT} \right) \gg 1$ , the equation above can be expressed as

$$J = J_0 \exp \left( \frac{qV}{nkT} \right) \quad 1.5$$

In the reverse direction, the current density saturates at  $-J_0$ . Rectification of the current through the *p-n* junction is an important characteristic. The other is that temperature has a great influence on current density implying that diode characteristics can be correctly interpreted only for fixed temperatures.

## **1. 2D Materials**

Two-dimensional materials are substances with a thickness of a few nanometers or less. Electrons in these materials are free to move in the two-dimensional plane, but their restricted motion in the third direction is governed by quantum mechanics. Initially, some physicists believed that freely standing perfectly two-dimensional materials are difficult to form in a stable way: a strictly two-dimensional material could be unstable to vibration caused by thermal fluctuations, forming other relatively stable disorder or three-dimensional configurations. Layered atoms could gather into nanoparticles or non-uniform films through wrinkling and rolling to reduce surface tension.

Beginning in the 1960s, some experimental physicists developed and enriched mechanical cleavage technology and liquid-phase cleavage technology and obtained possibly single-layer  $\text{MoS}_2$ , 2H phase tantalum disulfide ( $2\text{H-TaS}_2$ ), and niobium disulfide ( $\text{NbS}_2$ ), Maybe two layers of niobium diselenide ( $\text{NbSe}_2$ ) and other materials. In 2004, Novoselov, Geim and colleagues obtained monocrystalline graphene films from graphite bulk by micromechanical cleavage technique [4], which started a boom in two-dimensional materials research. They were awarded the Nobel Prize in Physics in 2010. With subsequent research the family of two-dimensional materials has expanded in many directions such as two-dimensional transition metal carbides, nitrides or carbonitrides (MXenes), noble metals, metal organic framework materials (MOFs), covalent organic frameworks (COFs), polymers, black phosphorus, silicene, antimony, inorganic perovskites and organic-inorganic hybrid perovskites.

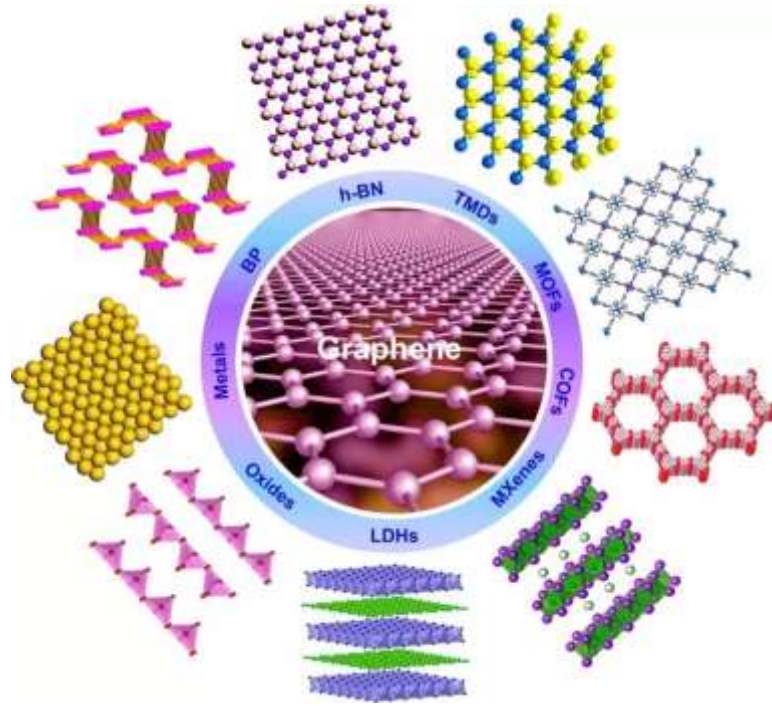


Figure 1.4 Schematic illustration of different kinds of typical ultrathin 2D nanomaterials such as graphene, h-BN, TMDs, MOFs, COFs, MXenes, LDHs, oxides, metals, and BP. Reference from [5].

The demand for different applications has greatly stimulated the development of different methods for preparing two-dimensional nanomaterials. Currently mature synthesis methods include: micromechanical cleavage, mechanical force assisted liquid exfoliation, ion insertion assisted liquid exfoliation, ion exchange assisted liquid exfoliation, oxidation assisted liquid exfoliation, selective etching liquid exfoliation, chemical vapor deposition (CVD) and wet chemical methods, etc. Since the two-dimensional materials obtained by different preparation methods may have different structural characteristics and varying physical, electronic, chemical and surface properties it is essential to perform in-depth characterization of the materials. Obtaining the precise size, composition, thickness, crystal phase, doping, defects, vacancies, strain, electronic state and surface state is very important for understanding the relationship between the structural characteristics and properties of the prepared two-dimensional nanomaterials.

A series of advanced technologies are used to characterize these materials, such as optical microscope, scanning probe microscope (SPM), electron microscope, X-ray absorption fine structure spectroscopy (XAFS), X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy, etc. Two-dimensional nanomaterials have great potential in a wide range of applications, such as electronic/optoelectronic devices, catalytic, energy storage and conversion, sensors, and biomedicine and have become the a popular research topic in the field of condensed matter physics, materials science, chemistry, and nanotechnology. However for basic research purposes, the method of choice for making few layer samples and devices of 2D materials remains mechanical exfoliation because it ensures the crystal quality and purity of the bulk precursor crystal, is an easily applicable method and can be extended to most layered materials. A variant of this method, developed in our group was used in this work for making few layer samples of layered bulk Indium Selenide.

Below we cite some chosen aspects of specific and remarkable properties of these materials which make them interesting for research especially with micro and optoelectronics applications in view.

- **Electronic properties:** Bulk MoS<sub>2</sub> is an indirect bandgap semiconductor with a gap of about 1.3 eV check[6]. Single layer MoS<sub>2</sub> is a direct bangap semiconductor with a gap of about 1.9 eV[7]. Similarly InSe is a direct bandgap semiconductor with a gap of about 1.25 eV[8]. However few layer InSe (less than 5-7 layers) is an indirect bandgap semiconductor with a gap of about 1.47 eV[9].

- **Transport properties:** As is well known, monolayer graphene exhibits extremely high mobility, even at room temperature[4].

- **Quantum properties:** Graphene exhibits the quantum Hall effect, notably also at room temperature[10]. Monolayer NbSe<sub>2</sub> has been shown to exhibit the so-called Ising pairing in its superconducting state[11]

- **Quantum properties:** Monolayer MoS<sub>2</sub> has been shown to exhibit properties where charge carriers in different ‘valleys’ or parts of the Brillouin zone couple to different polarizations of incident light, promoting the possible future technological field of valleytronics[12, 13].

All these examples illustrate the promise of these new materials and 2D physics that flow from their properties. In this work we have chosen to investigate the possibility of revisiting an ‘old’ device, the bipolar diode with a new technology.

### **1. 3 Devices of 2D materials**

The novel characteristics of two-dimensional materials as unit elements in electrical and optoelectronic systems, and their possible and eventual integration with complementary metal oxide semiconductor technologies have attracted widespread attention. From insulator boron nitride, semiconductor transition metal sulfide, to metallic graphene, the diversity of two-dimensional materials shows their multiple applications in various fields. The combination of various stacked and arranged two-dimensional materials may bring important scientific discoveries and substantial technological improvements. While current technology relies on years of development and maturation around three-dimensional semiconductors such as silicon or gallium arsenide, there is still a demand for improvement, especially regarding energy efficiency, performances, or innovative technologies such as flexible and transparent electronics. The unique optical and electrical properties of two-dimensional materials may play an important role in generation devices. Below we give a few examples of devices developed from 2D materials that further exemplify the possibilities of this research field and situate our work in the broader field.

The earliest and attractive research on two-dimensional materials is the research on graphene. Utilizing its semi-metallic properties, graphene can be

used as a high carrier mobility buffer for semiconductors and metal electrodes[14, 15]; such hybrid devices are more conducive to the extraction and transfer of electrons, and eliminate work function difference and contact resistance, improving the performance of electronic components.

As a zero band-gap semi-metal, the application of graphene in semiconductor devices is however quite restricted. The attention has been taken much more by TMDs materials for electronic and optoelectronic devices. The transition from indirect to direct as a function of the number of the layers is also a considerable feature of TMDs. For example, the bandgap of MoS<sub>2</sub> varies from 1.2 eV of indirect bandgap in multilayer to 1.9 eV of direct bandgap in a single layer, which is a crucial fact for designing efficient photo-detectors[16]. Report on photo-detector base on mechanically cleaved MoS<sub>2</sub> could achieve a maximum external photoresponsivity of 880 AW<sup>-1</sup>[17]. potential applications is the possibility of inducing a semiconductor metal transition through electrostatic doping[18-20].

In recent years, as an insulating two-dimensional materials, *h*-BN have also received attention as excellent dielectric materials, With a bandgap of 5.9 eV [21]. It has potential applications for 2D materials based high-quality gate dielectrics and transistors[22-24], tunneling junctions[25-27], and has become an indispensable component in the research and application of many two-dimensional nanomaterials. In addition to insulating properties, *h*-BN nanosheets also have an atomically smooth surface, and there are no redundant void bonds and charge traps, making them an ideal support substrate for 2D electronic products[28-30]. In some electrical devices, although *h*-BN itself does not participate in the generation and transmission of carriers, the performance of the device can be improved by several orders of magnitude. This aspect benefits from the smooth and uniform support so that the two-dimensional material stacked with *h*-BN can be displayed in the flattest and stretched form. Furthermore, due to the chemical inertness and insulation of *h*-BN, it also provides the function of packaging and preventing device aging.[31-33]. For example, by combining the *h*-

BN encapsulation with a 1D electrical contact, graphene transistors achieved ballistic transport with record mobility of  $10^6 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [31]. For other two-dimensional semiconductor materials like  $\text{MoS}_2$  and  $\text{WSe}_2$ , the function of improving device performance has also been reported[34, 35].

Given the excellent performance of a two-dimensional material, different two-dimensional materials stacked on each other to form a vertical heterojunction through van der Waals forces also achieve distinctive properties and extraordinary performance[36]. A large number of two-dimensional materials provide a vast resource library for the research of van der Waals heterojunction. The graphene/ $\text{MoS}_2$  heterostructure shows an increase in light responsiveness by several orders of magnitude compared to  $\text{MoS}_2$  alone[37, 38]. Some environmentally sensitive two-dimensional materials, like  $\text{InSe}$ , can also be protected by forming heterojunctions with graphene[15]. Different two-dimensional semiconductor materials were deposited by chemical weather deposition, and van der Waals heterogeneous *p-n* junctions formed by  $\text{MoS}_2/\text{WSe}_2$  and  $\text{WS}_2/\text{WSe}_2$  were also reported[39].

## **Chapter 2.**

# **Experimental methods and techniques**

In this chapter, the methods and techniques used for the fabrication and characterization of InSe and CdO devices will be introduced in detail. The fabrication of a few-layer InSe and CdO thin films samples has been carried out with two different methods. We applied the Anodic Bonding method to fabricate the InSe sample, which was invented by professor Abhay Shukla to fabricate two-dimensional layered materials on a glass substrate [40]. The CdO samples on glass have been prepared with the sol-gel spin coating method, which is a widespread technique for optical/electronic thin films [41, 42]. The samples are characterized after fabrication with optical microscopy, atomic force microscopy (AFM), Raman spectroscopy, and X-ray diffraction (XRD). Metallic leads are then evaporated on the samples to allow electronic transport measurements.



## 2. 1 Anodic bonding method for 2D materials fabrication

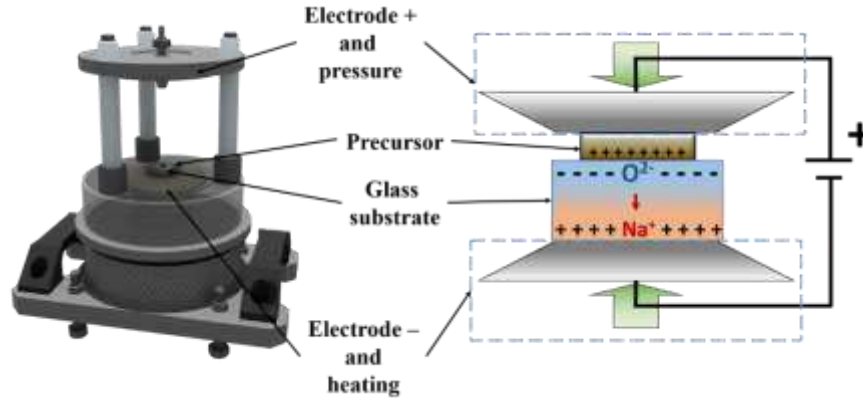


Figure 2.1 Left: the model of our anodic bonding apparatus. Right: the schematic of anodic bonding principle. The motion of the  $\text{Na}^+$  ions under the electric field with the red arrow. A micromanipulator tip or anvil can substitute the top electrode.

Commercial glasses are formed by amorphous networks of certain glass-forming oxides, mostly silica. The arranged atoms in the glass are linked together by the same forces as in crystals, however without long-range order, as the glass can be considered a solid 'frozen' supercooled liquid[43]. The physical properties of glasses depend crucially on the oxides entering its composition, specifically on the different cations and their concentrations. Indeed, cations in glass can be divided into two broad categories: molecules, the network modifiers, like sodium, bond covalently with oxygens to form chains of octahedron-like molecules, the *network modifiers*, like sodium, remain essentially ionized and compensate for the negative charge of un-bridging oxygens[44, 45].

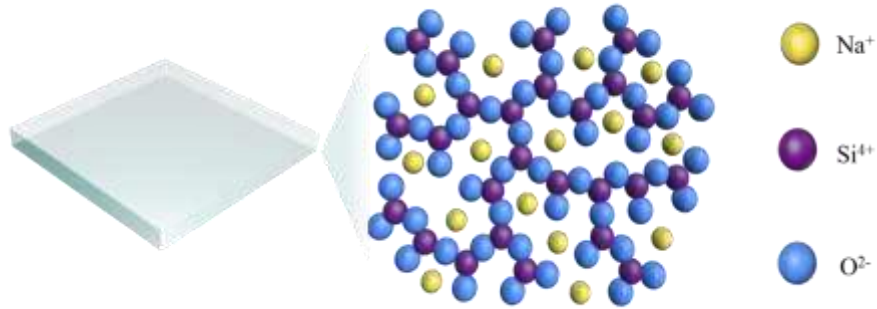


Figure 2.2 Glass structure at the atomic level. Oxygen and silicon atoms form a network that is locally disturbed by unbridged sodium ions [46].

The anodic bonding method was first invented in the late 60 s to bond glass to silicon wafers or metals without any intermediary, which has great applications in the electronic and microfluidic fields[47-50]. The operative principle of anodic bonding is based on the structural characteristics of the glass, which we introduced: as sodium ions act as network modifiers in the glass, they are weakly bound to the amorphous silica network. Thus, at moderately high temperatures, the mobility of sodium ions in the glass rises exponentially with an Arrhenius law, which allows them to drift in the glass under an applied electric field. In practice, as shown in Figure 2.2, the glass/wafer stack is heated between 200 - 500 °C, and then a high potential (200 – 1000 V) is applied across the stack. The drifting of sodium ions away from the interface between the two materials creates a layer of negative charges in the glass and a mirrored positive charge in the wafer. The electrostatic force between the two charge layers ensures a strong bond between the two materials[49, 51].

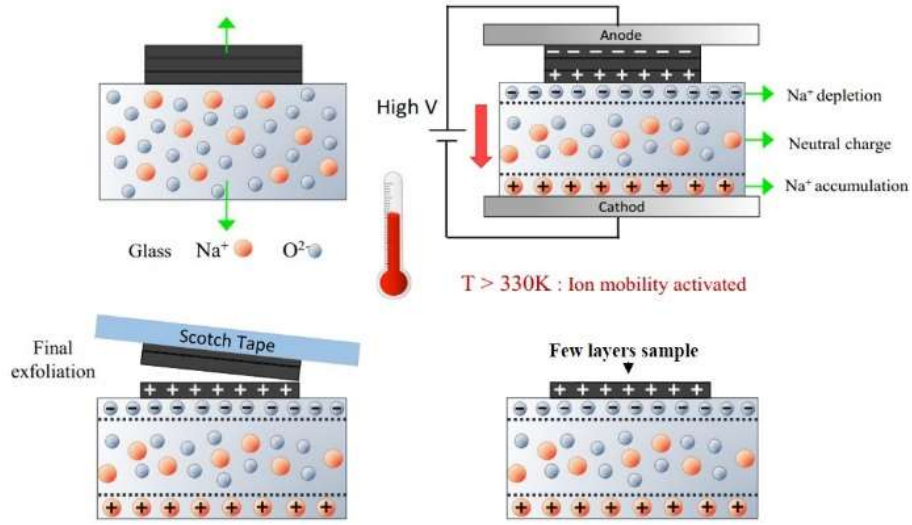


Figure 2.3 Schematic of anodic bonding principle applied on 2D materials fabrication.

The group of Prof. Shukla, in Sorbonne Université, first developed this technology for producing large-area graphene samples[40, 52], and two-dimensional samples of layered materials in general as a natural, agile and inexpensive method[53, 54]. The application of the anodic bonding method on two-dimensional layered materials fabrication is as follows. First, the glass substrates are cleaned in ultrasonic baths of acetone and ethanol then dried with nitrogen gas. Then precursor flakes of the bulk layered material are selected and deposited onto the cleaned glass surface. The anodic bonding is then carried out on this stack: at high temperatures ( $100\text{ }^{\circ}\text{C} - 300\text{ }^{\circ}\text{C}$ ), the  $\text{Na}^+$  ions being relatively mobile, they migrate across the glass substrate under the influence of the applied field[51] towards the cathode at its back. The static oxygen ions left behind to create a negative space charge on the glass surface at the interface and high electrostatic field with the positively charged layered materials. This field leads to intimate atomic contact between the substrate and the sample. After a few minutes, the material is bonded to the glass substrate and the electric field can

be removed. The next step is to cleave the precursor off the glass substrate using adhesive tape or another way. Large areas of few atomic layer parts of the precursor are retained on the glass substrate, bonded electrostatically to it.

The anodic bonding method has many advantages. We can get high quality, large area, and pure sample, as confirmed by Raman spectroscopy measurement and AFM. Hence this technology is relevant for immediate application in nanotechnologies and nano-electronics[[15](#), [46](#), [54](#), [55](#)].

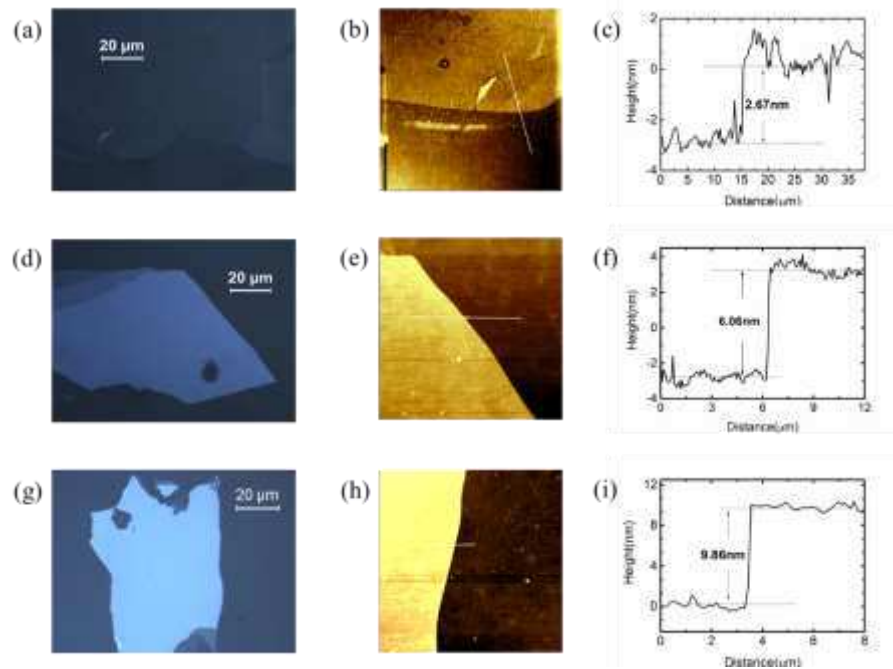


Figure 2.4 Microscope images and the corresponding AFM images of InSe few layers sample on the glass substrate. (a), (b) and (c) are from layered InSe sample with about 2.5 nm thickness. (d), (e) and (f) are from 6 nm thickness InSe sample. (g), (h) and (i) are from about 10 nm thickness InSe sample. All the presented InSe few layers devices are fabricated by anodic bonding method.

Three large area samples of InSe with different thicknesses are shown in Figure 2.4

## **2. 2 Sol-gel spin coating**

Thin CdO films have been prepared by several deposition methods in the literature. In our work, we mainly choose the sol-gel method. It is a cost-effective and straightforward method for depositing thin films with a large area on a smooth substrate surface. The sol-gel process is a method for producing solid materials from small molecules in solution. The most technologically important aspect of sol-gel processing is that, prior to gelation, the solution (or sol) can be prepared as thin films by such standard processes as dipping, spinning, or spraying. Compared to conventional thin film deposition processes, such as CVD, evaporation or sputtering, sol-gel film formation requires considerably less equipment and is potentially less expensive.

Usually, spin coating is divided into four stages: deposition, spin-up, spin-off and heat treatment[56]. An excess of liquid is dispensed on the surface during the deposition stage. In the spin-up stage, the liquid flows radially outward, driven by centrifugal force. In the spin-off stage, excess liquid flows to the perimeter and as a droplet. As the film thins, the rate of removal of excess liquid by spin-off slows down because of two combined phenomena: firstly, the resistance to flow increases with decreasing film thickness; secondly, the viscosity increases with the concentration of the nonvolatile components. In the fourth stage, we can attribute the steps of drying, annealing, and sintering to the heat treatment process. The purpose of heat treatment of the sample is to achieve irreversible dehydration of the sol-gel and to eliminate pores and residual stress in the gel. This is a process for converting a porous multi-body polymer gel into a densified polycrystalline film.

The precursor solution for CdO films fabrication was found in the literature[42], and prepared by the following procedure: 2 g cadmium acetate dehydrate was dissolved in 7 ml of methanol. Then, 0.11 ml of glycerol was added. A mixed solution included 7 ml methanol and 0.52 ml of trimethylamine was prepared and added subsequently to the transparent solution. The whole process is under slow constant stirring and at room temperature. The resulting solution can be used overnight for spin coating. The solution can be used for several days after which a slight turbidity will appear.

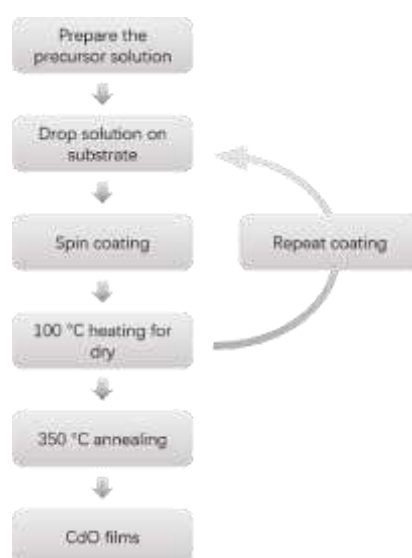


Figure 2.5 The preparation process of cadmium oxide film.

We drop on a cleaned glass substrate and place on the spin-coating apparatus. The rotation speed is selected to achieve the desired thickness. The sample is then dried on a 100 °C hot plate for 30 minutes to evaporate the remaining solvent in the coating process. Additional drops of solution are spin-coated then dried at 100 °C as needed to achieve the desired final thickness. The dried film is then moved to the muffle furnace. The temperature is increased slowly to 350 °C and maintained for one hour. This process is to further evaporate the residual

solution, and more importantly, to densify the polycrystalline particles by sintering. After sintering, a CdO film with compact structure is formed on the surface of the glass substrate. The films cover the entire glass substrate is shown in Figure 3.3 with the characterization of AFM and XRD.

### **2. 3 AFM (Atomic Force Microscope)**

AFM was invented by G. Binnig, C. F. Quate and Ch. Gerber in 1986 based on the scanning tunnelling microscope (STM). This microscopy can be applied to not only electrically conductive samples but semiconductors and insulators[57]. The schematics of the AFM principle and the tapping mode (also called AC mode) of AFM are shown in Figure 2.6 (b). Here is the basic principle of AFM: The key component of AFM is a microscopic cantilever with a thin probe used to scan the surface of the sample. The cantilever, usually made of silicon or silicon nitride with tens to hundreds of microns in size, will be deflected in response to the force between tip and sample when the tip is brought into proximity of a sample surface according to Hooke's law. Typical forces range from  $10^{-11}$  to  $10^{-6}$  N between probing tip and samples. The offset of cantilever caused by the force is measured by the laser beam on the microcantilever reflected to the photodiode array

When scanning at a constant height, the probe is likely to approach the surface and cause deformation. Therefore, a feedback system is usually used to maintain a constant height between the probe and the sample surface. Commonly, the sample is placed on a piezoelectric tube and can be moved in the z direction to maintain a constant distance from the probe, and moved in the x and y directions to achieve scanning.

The main working modes of AFM include static mode and dynamic mode. In the static mode, the cantilever is drawn across the surface of the sample, and the height map of the surface can be directly obtained from the deflection of

the cantilever. In the dynamic mode, the cantilever vibrates at or near its fundamental frequency or harmonics, and its amplitude, phase, and resonance are related to the force between the probe and the sample. The change of these parameters relative to the vibration of the external reference can give the properties of the sample.

Two working modes correspond to three imaging modes: contact mode (also called static mode), non-contact mode, and tapping mode (also called AC mode or intermittent contact). Typically, for the contact mode, the tip and sample are very close, the overall force is repulsive, and the tip is controlled by static deflection. In the non-contact mode, the tip and sample are relatively far, the overall force is attractive, and the tip is controlled by resonance frequency. In the common tapping mode, in which the working distance is between contact mode and non-contact mode, the tip is controlled by oscillation amplitude.

Unlike electron microscopes that can only provide two-dimensional images, AFM provides true three-dimensional surface maps. At the same time, AFM does not require any special treatment of the sample, such as copper or carbon plating, which will cause irreversible damage to the sample. Third, the electron microscope needs to operate under high vacuum conditions, and the atomic force microscope can work well under normal pressure or even in a liquid environment. This can be used to study biological macromolecules and even living biological tissues.



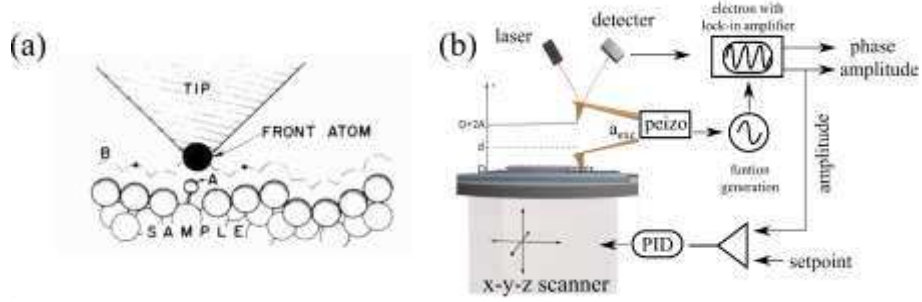


Figure 2.6 (a) Description of the principle of the AFM operation which referenced from [57], Under the effect of Hooke's law, tip will always have a certain distance from sample. (b) Schematic diagram of atomic force microscope: detector and feedback electronics detector and feedback circuit; photodiode; laser; sample surface; cantilever and tip micro cantilever and probe; scanner piezoelectric scanner

In the experiments, AFM scanning was performed on Scanning Probe Microscope SmartSPM-1000 instrument (AIST-NT) in ambient condition. We used tapping mode (AC mode) for all the two-dimensional sample, and high-resolution images are obtained [40, 46, 52-55, 58, 59].

## 2. 4 Raman spectroscopy

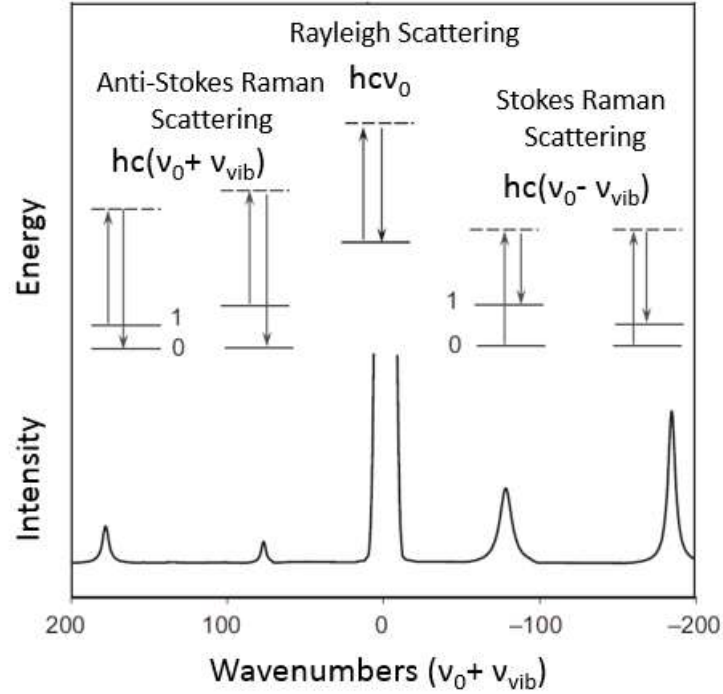


Figure 2.7 Schematic illustration of Rayleigh scattering as well as Stokes and anti-Stokes Raman scattering[60].

In Raman scattering, the energy of inelastic scattered radiation from a monochromatic laser beam incident on the sample is analyzed to obtain information on the scattering processes and the physics of the sample. In our case, the scattering is from phonons. The scattered radiation can be divided into several categories according to the frequency of the out-coming photons: The first type is Rayleigh scattering, which is the predominantly elastic scattering of light and the frequency of outcoming photons is the same as the frequency of the incident photons. The second type is caused by a scattering centers (molecules or dust particles) whose wavenumber changes less than  $10^{-5} \text{ cm}^{-1}$ . This type of scattering is called Mie scattering. The third type is the scattering produced by the interaction between the incident light wave field and the elastic wave in the medium

(acoustic phonons), and the wavenumber change is about  $0.1 \text{ cm}^{-1}$ , which is called Brillouin scattering. There is another type, scattering with a wavenumber change greater than  $1 \text{ cm}^{-1}$ , which is equivalent to molecular rotation, vibrational energy level, and electronic energy level transitions, called Raman scattering. In our case, we will be looking at Raman scattering due to optical phonons. The inelastic scattering of light was predicted as early as 1923, but it was not actually observed until 1928. The Raman effect is named after the observer. It was observed by C. V. Raman and K. S. Krishnan[61] using sunlight, and C. V. Raman was awarded the Nobel Prize in 1930. In this part, we will introduce the application of Raman spectroscopy.

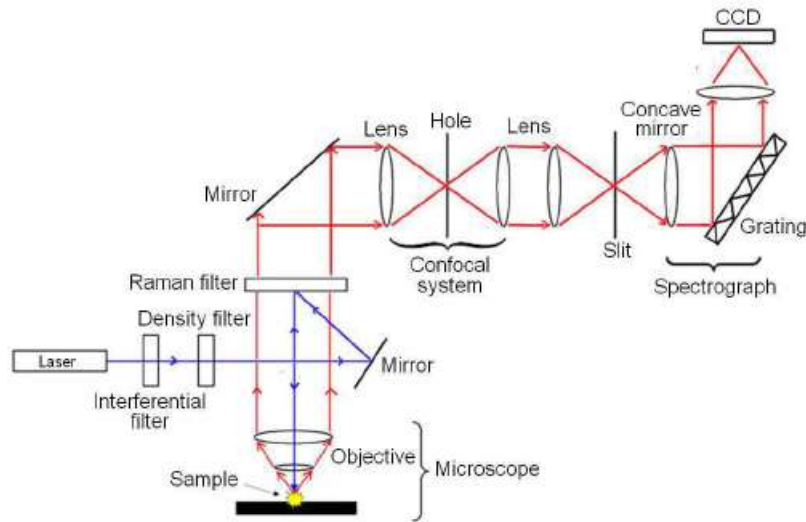


Figure 2.8 Schematic of our Raman spectroscopy system.

In the case of 2D materials and thin films, Raman spectroscopy represents a fast and non-destructive tool for the study of the properties of the materials. In our Raman experiments, micro Raman spectroscopy was performed using Xplora Raman spectrometer (Horiba Jobin-Yvon) in back scattering geometry under ambient conditions. Two laser wavelengths can be used as the excitation source: a green laser at 532 nm and a red laser at 638 nm. The schematic of

our Raman spectroscopy system is shown in Figure 2.8. The confocal system is composed of lenses, a hole, and a slit. The hole is responsible for spatial and axial resolution and the slit is responsible for spectral resolution. The microscope is critical in the  $\mu\text{m}$ -scale 2D sample measurement. In our measurement, the 100X objective is used for the samples. The spectrograph is composed of lenses and a grating. The grating separates the different wavelengths of the Raman scattering signal.

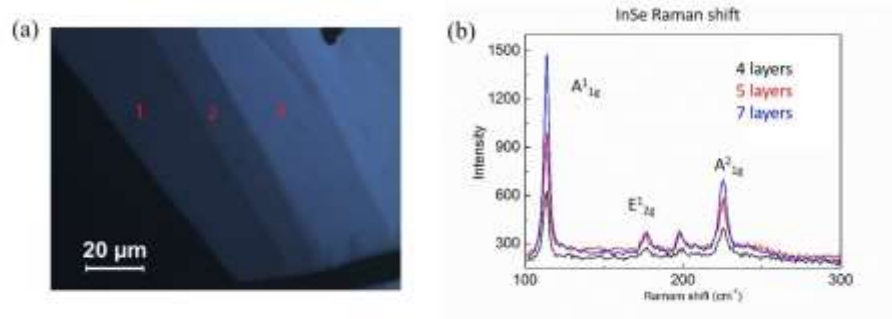


Figure 2.9 Raman characterization of a few-layer InSe (a) Optical image of InSe. (c) Raman spectra of a few-layer InSe.

Comparing the InSe data in Figure 2.9 with published results for the bulk[62-65], we identify the peaks at  $114\text{ cm}^{-1}$ ,  $176\text{ cm}^{-1}$  and  $226\text{ cm}^{-1}$  with  $A_{1g}^1$ ,  $E_{2g}^1$  and  $A_{1g}^2$  modes, the weak peak at around  $200\text{ cm}^{-1}$  which corresponds to the  $\epsilon$  polytype[66]. This peak is systematically absent in the bulk samples indicating perhaps that the occurrence of the  $\epsilon$  polytype provides an easier preferential cleaving plane for the sample. This part of the discussion has been corroborated by TEM in Chen's research[15].

## **2. 5 XRD (X-ray diffraction)**

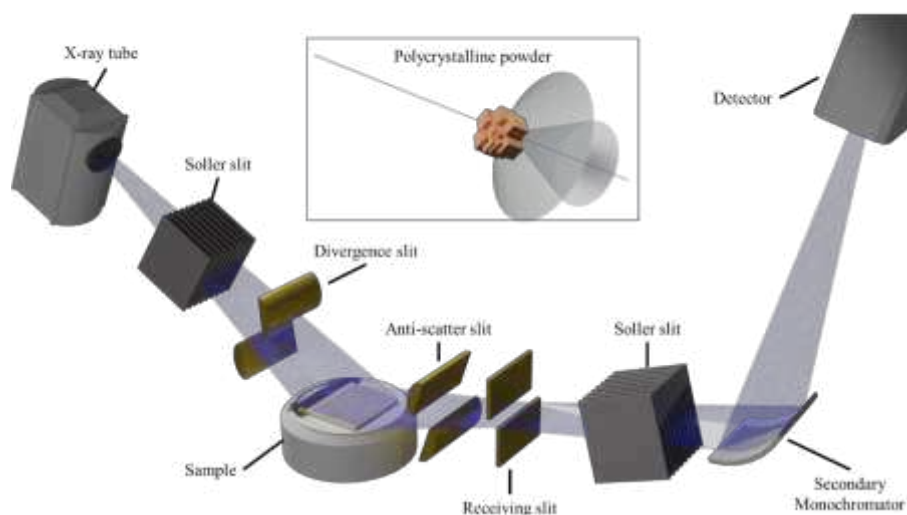


Figure 2.10 Schematization of the X-ray diffraction apparatus.

X-ray diffraction (XRD) is one of the most used tools to analyze the crystal structure of a material. X-rays were accidentally discovered by W. C. Röntgen in 1895 while studying the high-voltage discharge phenomenon of vacuum tubes. This great discovery made Roentgen the first Nobel Prize winner in the world in 1901. In 1912, the M. von Laue discovered X-ray diffraction on crystals with his creative experiment. X-ray diffraction is a method of analyzing the crystal structure, lattice parameters, crystal defects (dislocations, etc.) of different materials, the content of different structural phases, and internal stress using the phenomenon of X-ray diffraction in the crystal. This method is an indirect method based on a specific crystal structure model. That is, the crystal structure and lattice parameters of the sample are analyzed and calculated according to the characteristics of the X-ray signal that is diffracted with the crystal sample, and high accuracy can be achieved. The wavelength is shorter than that of visible light, about the same order of magnitude as the crystal lattice parameters, at  $10^{-8}$  cm or so.

The X-ray wavelength used for crystal structure analysis is generally 0.25~0.05 nm.

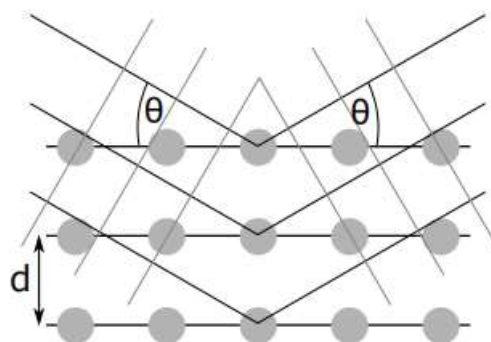


Figure 2.11 Illustration of the Bragg law.

**Bragg's law:** Diffraction in a given direction is basically due to the relationship between the phases of all waves reflected by each unit cell of the crystal in that direction. Light rays passing through different points of the crystal follow light paths of different lengths. This difference causes the amplitude of the final wave to change; when the phase difference is 180 degrees, the waves cancel each other out. In contrast, when the waves are in phase, the final wave amplitude is the sum of the amplitudes of each wave. Since the crystal is composed of a large number of unit cells, the constructive interference between all unit cells will produce a sufficiently strong beam that can be measured with an X-ray detector.

All the following parameters are used to describe what has been shown in Figure 2.11. The condition of the wave being in phase is that the

difference in optical path length is zero or an integer multiple of  $n$  times wavelength. In a crystal, the optical path difference between atoms at equivalent positions in different unit cells is

$$2d\sin\theta \quad 2.1$$

Where  $d$  is the distance between parallel planes connecting equivalent points of the lattice. Therefore, the angles at which we observe constructive interference are given by Bragg's law:

$$2d\sin\theta = n\lambda \quad 2.2$$

As in the case of atomic elastic scattering, crystal diffraction can be interpreted as the specular reflection of X-rays passing through all planes of the crystal at a certain angle  $\theta$  incident beams, separated by a distance  $d$  satisfying Bragg's law. Therefore, the points in the diffraction pattern are called "reflections".

**Miller indices:** In order for Bragg's law to maintain a set of parallel reflection planes, they must cross the axis of the unit cell by an integer multiple. The crystal reflection is identified by three numbers  $h$ ,  $k$  and  $l$  equal to the number of intersections of the plane and the axis  $a$ ,  $b$  and  $c$ .  $h$ ,  $k$  and  $l$  are called Miller indices. Mathematically, the vector described by the Miller index is perpendicular to the reflection plane in the coordinate system defined by the crystal lattice.

## 2. 6 Device fabrication

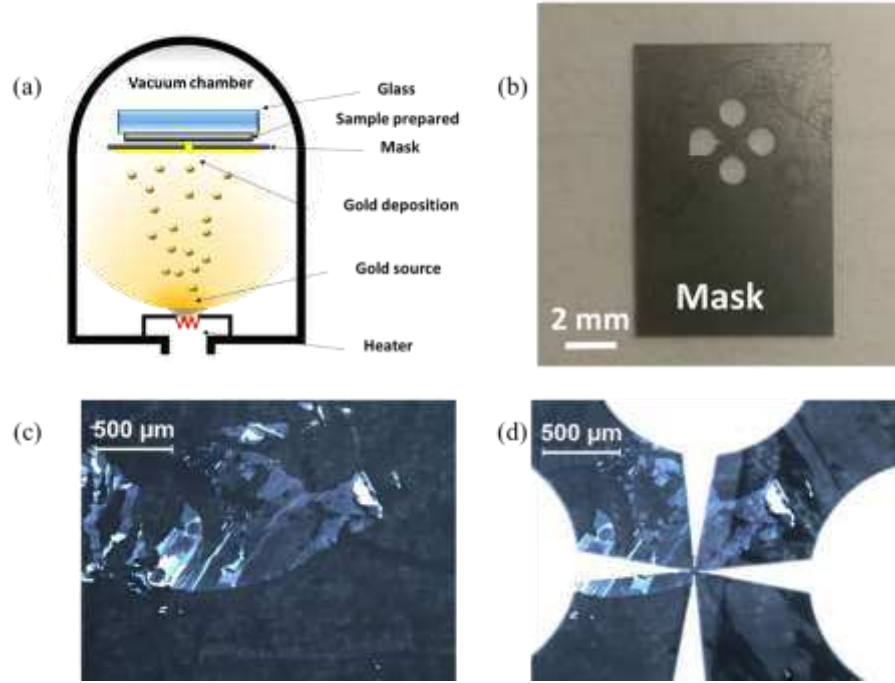


Figure 2.12 (a) Schematization of the thermal evaporator apparatus. (b) Mask used for the contact deposition. (c) One InSe sample before and (d) deposition of gold contacts.

To perform electronic transport measurement on a few nanometer-thick samples, we need to connect it in an electric circuit. This is achieved by evaporating a metallic circuit on the substrate with small leads covering the edges of the area of interest and further bigger pads that can be connected to the external apparatus.

There are many ways to define the geometry of the metallic leads, such as electronic or optical lithography. While these two methods have good spatial resolution and very well defined contact leads, they have an intrinsic pollution problem: both use polymer resins deposited directly over the sample. These resins leave residues on the surface of the sample, which can be detrimental to the electronic properties of the thin material.



We decided to use stencil masks to avoid this chemical contamination. The masks are made of a sheet of 0.5 mm steel, with holes shaped like the intended contact leads circuit (Figure 2.12). Before evaporation, the masks are carefully aligned on top of the sample under a binocular with two micro-positioning stages (one moving the sample, the other moving the mask) then held in place either by double-sided adhesive tape or PMMA drops acting as glue.

Due to fabrication constraints on the mask, the thinnest leads connected to the sample are 10 microns wide and 35 microns apart. This limits the lateral size of usable few-layer InSe to a minimum of 50 microns. There is no limitation for CdO films as they cover the whole substrate, and millimeter size masks can be used.

After the mask is aligned and fixed, the metal used for the contacts is evaporated in an Edward thermal evaporator in the cleanroom facilities of the Ecole Normal Supérieure.

The choice of metal used for the contact is crucial to avoid Schottky barriers at the interface between the material and the metal and make Ohmic contacts. From previous experience in the group, gold has been used in this work. An example of a device before and after deposition is shown in Figure 2.12 (c) and (d). These four contact geometry has been chosen to allow 2-wire and 4-wire transport measurements, as discussed further.

The final step of device fabrication is to refine the geometry of the device. As anodic bonding leaves several flakes on the substrate, it is important to constraint the current flow to the area of interest. While this can be done with plasma etching, it would require another step of lithography on polymer resins. Hence, to avoid the use of these resins, we used a mechanical approach. The final shape of the device is therefor defined by scratching the surface of the substrate with a tungsten needle controlled by a micro-manipulator. The tip radius of the needle is about 10 microns.

## 2.7 Transport

### two-wire measurement

In the measurement of an electronic component with two-wire measurement, the test current is forced through the component by leads, and multi-meter measures the voltage across its terminals. Similarly, we can also apply a test voltage across the electronic components, and the multimeter measures the current to give the component's resistance. This is known as a two-wire measurement. In an ideal state, the test results of these two sources are the same. In the actual test process, considering the thermal effects of electronic devices, we usually choose a voltage source and measure the current flowing through the sample.



Figure 2.13 Two-wire measurement usually plugin lead resistance affecting measurement accuracy.

In a two-wire measurement, as shown in Figure 2.12, the value of resistance measured also include the resistance of the test leads (which might be of 10 - 100 $\Omega$  in a cryostat) and, more importantly for 2D materials, the contact resistance between the metallic leads and the actual material. Therefore, the voltage measured by the meter will not be the true value of the voltage across the

component. Considering that in actual measurement, our samples usually have very high resistance values, the volt-drop caused by lead resistance can usually be considered negligible, but not the contact resistance. Hence, we need to use 4-wire measurements to accurately measure the resistivity of 2D samples, while 2-wire measurements will be used to measure diode devices.

#### Four-wire measurement

To accurately measure the resistivity of material without measuring the resistance of the test leads or the contact resistances, we use 4-wire measurements in which two wires are used to inject current in the material, and two other wires measure the voltage drop across the sample. The high impedance of the voltmeter ensures the current leakage through the measurement loop is negligible, provided the resistance of the sample is small compared to that of the voltmeter's impedance.

We adopt the van der Pauw geometry as it allows us to measure the resistivity and the Hall coefficient of a thin sample of homogeneous thicknesses, and is well suited for samples of arbitrary shape. In the van der Pauw geometry, the four contacts are placed around the perimeter of the sample. In contrast to the other 4-wire measurement geometry - the linear Hall bar - which provides the resistivity in the sensing direction, the van der Pauw method provides an average resistivity of the sample[67]. Generally speaking, there are several elements to consider to measure semiconductors with the van der Pauw method[68].

1. The contacts are placed at the circumference of the sample.
2. The contacts are sufficiently small compared to the lateral sample size.
3. The sample is homogeneous in thickness.
4. The surface of the sample is singly connected. For example, the sample does not have isolated holes.

In practice, we use “clover-shaped” samples, which relieves the constraints of having small contacts at the circumference of the sample. The clover shape is produced by mechanically scratching the sample with a needle between the evaporated metallic leads.

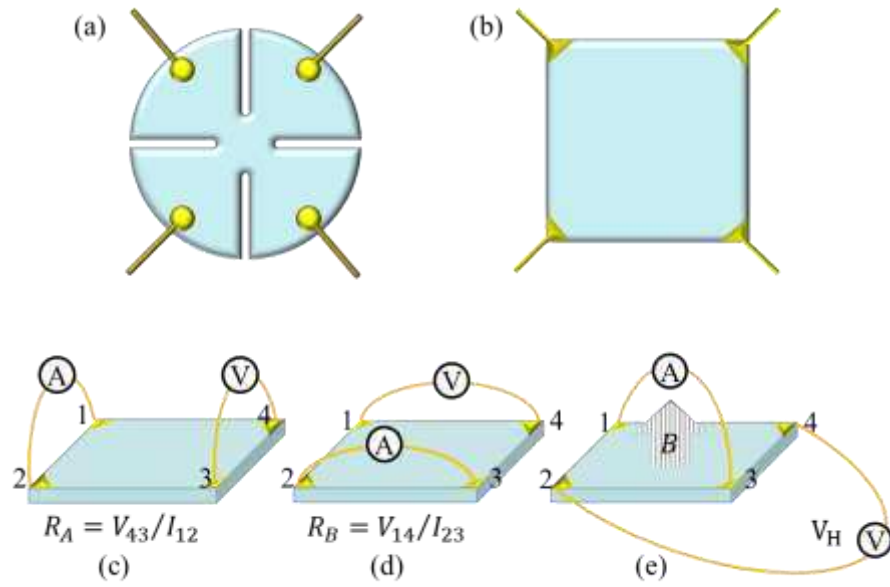


Figure 2.14 (a) Idealized model of van der Pauw method with "clover-shaped" in which the influence of contacts has been reduced considerably. (b) Sample geometry for van der Pauw resistivity and Hall effect measurements. (c) and (d) Schematic of a van der Pauw configuration used in the determination of the two characteristic resistances  $R_A$  and  $R_B$ . (e) Schematic of a van der Pauw configuration used in the determination of the Hall voltage  $V_H$ .

As Figure 2.14 shown, the  $R_A$  is calculated from the ratio  $V_{43}/I_{12}$ , and the  $R_B$  is calculated from the ratio  $V_{14}/I_{23}$ . From these two values, the  $R_s$  is derived from:

$$R_s = \frac{\pi}{\ln(2)} \frac{R_A + R_B}{2} f \quad 2.3$$

$f$  is a correction factor which takes in to account the inhomogeneity of the sample through the ratio  $r$ , which is defined as  $R_A/R_B$  if  $R_A < R_B$  or  $R_B/R_A$  if  $R_B < R_A$ .  $f$  is given by

$$\cosh\left(\frac{r-1}{r+1} \ln(2)\right) = \frac{1}{2} \exp\left(\frac{\ln(2)}{f}\right) \quad 2.4$$

$f$  is always equal to or smaller than 1 (it is 1 when  $r = 1$ ), and it is not derivable analytically. In practice, a polynomial approximation can be used.

The van der Pauw geometry also allows for the measurement of carrier density and charge mobility through the Hall effect. By measuring the Hall coefficient and conductivity of semiconductor material, the main parameters such as the conductivity type, carrier concentration, and carrier mobility of the material can be obtained.

In this case, the contact configuration we adopted is shown in Figure 2.14 (e). When a current is passed in the sample, and a magnetic field is applied perpendicular to the sample surface, a transverse voltage (Hall voltage) appears in the direction perpendicular to the current and to the magnetic field, whose amplitude is given by

$$R_{Hall} = \frac{V_{Hall}}{I} = \frac{B}{qn_S} \quad 2.5$$

Where  $n_S$  is the surface charge density, and  $q$  is the charge of the charge carriers ( $+/-$  time the electron charge  $e$ ). The sign of the Hall voltage is determined by the type of charge carrier present in the sample, electrons or holes.

In practice, samples are never perfectly shaped and we measure a finite transverse voltage even at zero magnetic fields. This offset can be removed by anti-symmetrizing the measured voltage with respect to the magnetic field to recover the true Hall voltage. An alternative in the van der Pauw configuration

is to measure the transverse voltage along the two diagonals (effectively doing 2 Hall measurements), which allows canceling the offset by averaging them. This is particularly effective if the magnetic field direction cannot be reversed. The Hall mobility can be calculated using the Hall carrier density and sheet resistance as  $\mu_H = 1/(en_S R_S)$

## 2. 8 Space charge doping

Doping is an important process of the semiconductor industry as it allows us to modify and control the electronic properties of a semiconductor to match the needs of particular device architecture. In particular, doping allows changing the type of majority carriers in the material (electrons or holes) and their concentrations.

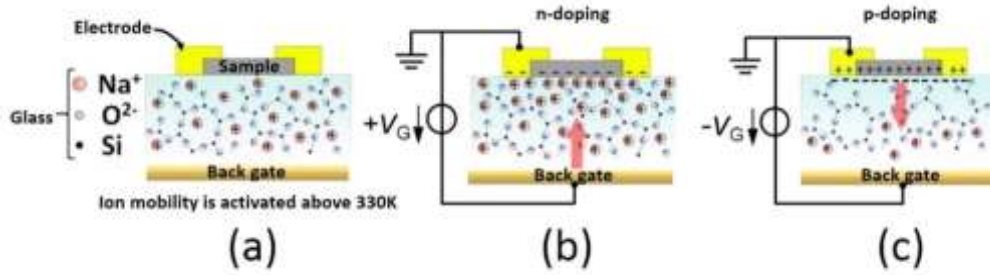


Figure 2.15 Two-dimensional material the schematize on a glass substrate and Na<sup>+</sup> ions drift under the effect of heat and the electric field.

The technique that we call Space Charge Doping is one of the methods for electrostatic doping of two-dimensional materials first applied by Shukla's group[46]. Contrary to chemical doping, where impurities are introduced in material to change its carrier density, electrostatic doping uses a capacitive effect to inject holes or electrons directly in the material. The maximum carrier density achieved with a standard field-effect transistor type device is limited by the insulator properties. New high-density techniques have been developed such as the Electric Double Layer Transistor (a.k.a. ionic liquid technique) and Space

Charge Doping, where a strong interfacial electric field is formed by a space charge layer of ions close to the surface of the material. The Space charge doping method is similar to the anodic bonding technique, which also exploits the presence of mobile ionic species in the glass to induce a charge imbalance at the glass-material interface. The mobility of positive sodium ions is increased by heating, and an applied electric field causes ion drift. The polarity of the electric field results in accumulation or depletion of sodium ions at the glass surface inducing, respectively, electron or hole doping in the material placed on the surface. In the case of graphene, extremely high doping levels are reached ( $> 10^2 cm^{-2}$  [46]), and SCD has been successfully applied to other materials [69]. More detail of the space charge doping on InSe and CdO will be discussed in the next chapter.

# Chapter 3.

## Materials

Microelectronic technology continuously needs to improve because of the fast-evolving demands of telecommunications, calculation power, and data treatment. Recent constraints (energy consumption) or developments (generating light through LEDs) impose new directions and requirements on this technology. It is thus on the lookout for efficient devices, which in general can be achieved through new materials. Existing technology is exclusively based on Si and microelectronic technologies, where a central and crucial aspect is the local doping of the material, as exemplified in the diode (chapter 1 section 1). In current technology, this is exclusively achieved through chemical doping. As we have discussed (chapter 2, section 7), new materials and technologies could offer an alternative way to achieve this. In this chapter, we define the materials that could be used to fabricate a diode device based on ultra-thin materials and electrostatic doping. First, we give ourselves a list of criteria which these materials must satisfy:

1. Clearly, the material must be a semiconductor, with a bandgap in the range of 1-2 eV for investigation of eventual light emission characteristics and a reasonable amount of thermally excited carriers at room temperature. For optoelectronics again, a direct bandgap is preferable.
2. The material must lend itself to reasonably easy device fabrication. By this, we mean in-house fabrication since, for a project of this complexity,



it is comfortable to have a mastery of all aspects of the device. We thus need materials that can be fabricated in our laboratory in few layers (if from a layered 2D material) or few nanometers thick thin film (if not). We possess this technology (anodic bonding) for 2D materials. For other materials, this limits us to a few commonly used techniques like evaporation, sputtering, spin-coating, or the sol-gel method. To avoid chemical contamination, we prefer to use mechanical shaping and shadow or stencil masks to contact our devices, thus we need a usable lateral area of at least 50 micrometers. In anodic bonded 2D material devices, this automatically precludes the use of single atomic layers of materials, notably TMDC, because they cannot be fabricated in these dimensions.

3. We need materials with reasonable resistance at ambient conditions. By definition, the surface of ultra-thin materials plays an important part in their properties, and often the whole material may be altered by interaction with ambient conditions. This can lead to erroneous results and degraded performance. Our choice then will be guided by materials which are stable to ambient over a few days at least.
4. As a practical choice, we decided to fine-tune our choice to two materials. A thesis is a limited-time project, and a bottleneck can arise, which may compromise further progress. For this reason, we decided to work with two materials until the last step of device making and characterization (chapter 4) to have a fall-back solution in case of problems at a later stage.
5. To narrow down our choice of materials, we consulted recent work on devices in particularly in layered 2D materials, but also in related areas, for example, in transparent conducting oxides. Our final choice, as will be seen in this chapter, is from these two families of materials.
6. A very important criterion for the chosen material is the possibility of doping it in an ambivalent way, which is to say with both  $n$  and  $p$ -type carriers. This point merits a more detailed discussion, which is given below.

The discussion below is based on the arguments developed in ‘Limits to doping in oxides’[70], Quoting from the abstract of this work:

“The chemical trends of limits to doping of many semiconducting metal oxides is analyzed in terms of the formation energies needed to form the compensating defects. The *n*-type oxides are found to have high electron affinities and charge neutrality levels that lie in midgap or the upper part of their gap, whereas *p*-type oxides have small photoionization potentials and charge neutrality levels lying in the lower gap. The doping-limit energy range is found to vary with the bulk free energy of the compound.” Indeed the article gives some useful guidelines for limits to doping, essentially in oxides. This is done by using the concepts of pinning energy[71-75] and the alignment of valence and conduction bands. Intuitively this means that the closer the band edge to the charge neutrality level, the easier it is for the material to be doped to the corresponding polarity. Robertson and Clark further remark that in chemical doping three criteria limit the possibility of doping a material:

1. Lack of solubility of the dopant material in the host matrix
2. Deep dopant level. This is the basis of the intuitive remark above since if the dopant level is too deep, it cannot be ionized and is not as effective as a dopant.
3. The final criterion is a key one. This concerns the formation of native defects, which are not due to the dopant but due to the host matrix. The movement of the Fermi energy due to doping can change the formation of the energy of native defects since they can become energetically favorable and compensate the dopant.

While the first criterion is not applicable to electrostatic doping, where there are no foreign chemical species involved, criteria 2) and 3) remain valid and regulate the possibilities of electrostatic doping in materials. In the following, we will examine materials in light of these criteria as calculated in the work of Robertson and Clark. Figure 3.1 below from this work shows “(a) Valence

and conduction band energies of various oxides vs vacuum level, with the doping limits, showing the dopable and undopable cases and (b) Similar plot, with the ligand bands aligned using their charge neutrality levels.”

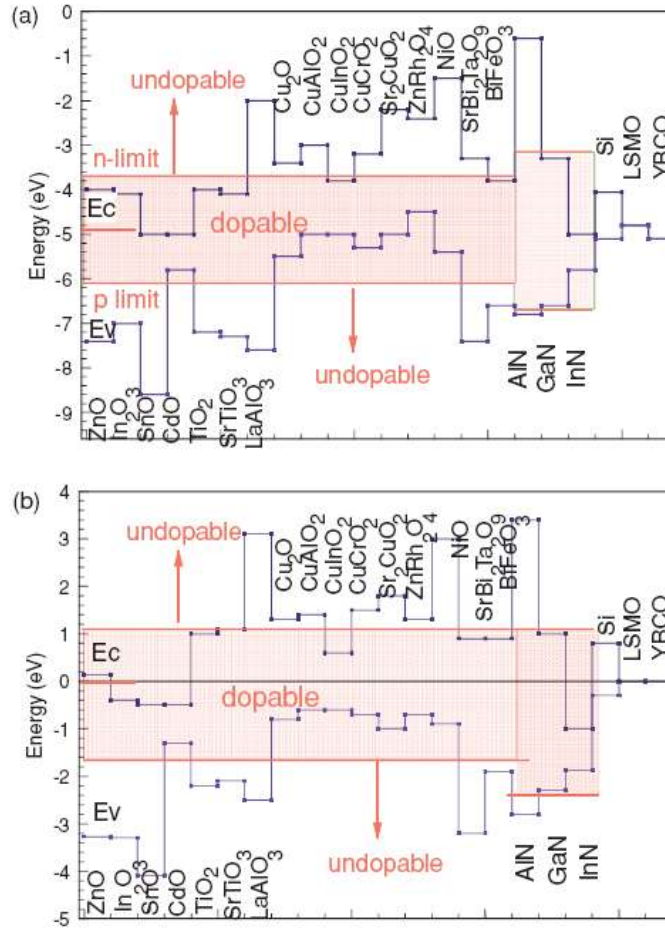


Figure 3.1 “(a) Valence and conduction band energies of various oxides vs vacuum level, with the doping limits, showing the dopable and undopable cases and (b) Similar plot, with the ligand bands aligned using their charge neutrality levels.”[70]

Some well-known facts can immediately be seen: ZnO is often intrinsically *n*-doped but not known in the *p*-doped form. Similarly, NiO or CuO<sub>2</sub> are *p*-doped but not easy to dope with *n* polarity. Finally, GaN, which according

to this calculation, should be possibly doped both  $n$  and  $p$ , nevertheless it should be more difficult to dope  $p$ , which is what has been observed experimentally. As we mentioned in the Introduction, this was the problem solved by the trio, which obtained the 2014 Nobel prize in Physics. We use Figure 3.1 to pinpoint two materials, one an oxide CdO, the other a layered semiconductor InSe. Both these choices will be explained and investigated in greater detail later in this chapter. Here we point out that CdO is among the very few oxides which exhibit the theoretical possibility of ambivalent doping. InSe does not figure in this calculation. However, an oxide of Indium does,  $\text{In}_2\text{O}_3$ , which is also intrinsically  $n$ -doped. According to this figure, it would be difficult to dope  $\text{In}_2\text{O}_3$  with  $p$  polarity. However, we remark that the ligand in InSe is Se, a substantially bigger atom than O, and thus the band-gap will be smaller (it is effectively a little above 1 eV). We can then expect the conduction band level to approach the dopable region in Figure 3.1 concerning  $\text{In}_2\text{O}_3$ . Our experiment, which we will detail later in this chapter, will bring some confirmation of these observations.

Layered semiconductors have appeared as promising materials as they can be fabricated in ultra-thin form like graphene and display a bandgap, which is mandatory for most microelectronic applications. The weakly bound van der Waals layered structure and strong in-plane bonds ensure the in-plane stability of the layers and their compatibility with a wide variety of substrates, including other layered materials, to build heterostructures. Such heterostructures have shown great promise for the fabrication of efficient, ultra-thin, large area, vertical heterojunctions for applications in opto-electronics[76].

Transition metal dichalcogenides (TMDs, for example,  $\text{MoS}_2$ ) have been widely studied in the last years as they offer good mechanical properties and are stable in air. However, TMDs display a direct bandgap only at the monolayer level, making them harder to use for photo-electronics applications. Even if monolayer fabrication is accounted for, strong interaction with the substrate can alter many appealing properties. *III-VI* semiconductors are a less-known group

of layered materials with some differences with respect to dichalcogenides. Indeed, their bulk bandgap is direct (roughly for 5-7 layers or more), which is useful for optoelectronic since multi-layer materials are easier to handle and are mechanically more stable. The band gaps of the family (InSe: 1.2 eV, GaSe: 2 eV, GaS: 3 eV) cover a large spectrum, notably the visible range permitting the choice of the material for a given application.

### 3. 1 Indium selenide

The earliest research report of Indium selenide (InSe) synthesis is provided as a member of the same family structure of In- and Ga- compounds by Klemm and Vogel[77]. Generally, single crystals of InSe have been obtained by Bridgman and Czochralski techniques. Parts of small samples also have been grown from the vapor phase by chemical transport[78]. Single-layer InSe has the same crystal structure, which consists of four close-packed monoatomic sheets in the sequence of Se-In-In-Se. However, different polytypes can be formed by stacking the single layers with particular sequences. Similar to GaSe, most InSe crystal performed as  $\beta$ - (space group of  $D_{6h}^4$ ),  $\epsilon$ - ( $D_{3h}^1$ ) and  $\gamma$ - ( $C_{3v}^5$ ) lattice polytypes[79-82], as shown in Figure 3.2 Unit cells of three kinds of Polytypes in InSe. (a)  $\beta$  polytype (b)  $\epsilon$  polytype (c)  $\gamma$  polytype[84].. A large number of mixtures of different polytypes that appear in bulk crystals grown from stoichiometric melts by the Bridgman method may lead to widely dispersed results in terms of structural, electrical, and optical properties. The  $\beta$ - and  $\epsilon$ - polytypes belong to the hexagonal system, and each unit cell contains eight atoms extended over two layers, with the same lattice parameters (  $a = b = 4.05 \text{ \AA}$ ,  $c = 16.93 \text{ \AA}$ ). The  $\gamma$ - polytype, with lattice parameters  $a = b = 4.05 \text{ \AA}$ ,  $c = 25.32 \text{ \AA}$ , has rhombohedral symmetry, and its unit cell contains four atoms. A stacking fault in  $\gamma$  of which the energy is small due to the weak van der Waals-type inter-layer bond constitutes locally hexagonal ( $\epsilon$  and  $\beta$ ) lattice types. The estimation of the perfectness of the crystal lattice, especially for the layered materials, is significant because of their polytypism and/or small stacking-fault energy[83].

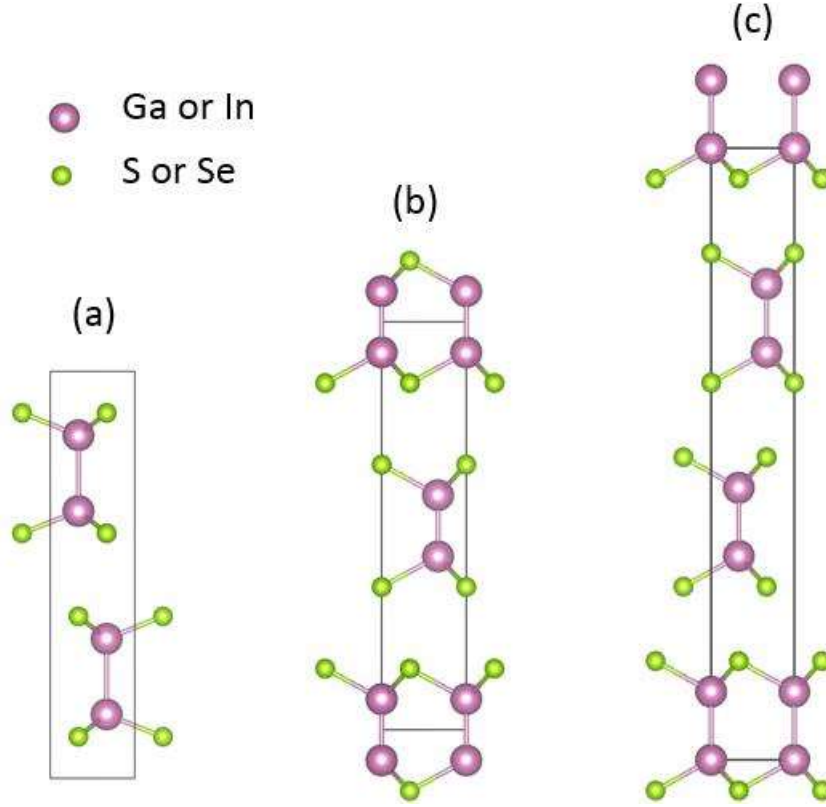


Figure 3.2 Unit cells of three kinds of Polytypes in InSe. (a)  $\beta$  polytype (b)  $\epsilon$  polytype (c)  $\gamma$  polytype[84].

Previous experiments in our group have shown that the InSe polytypes can be distinguished with high-resolution transmission electron microscopy and Raman spectroscopy[15]. As mentioned in chapter 2, a Raman peak at  $200\text{ cm}^{-1}$  is typical of the  $\epsilon$ -polytype in our few-layers InSe samples.

The InSe precursor we used is fabricated by the Bridgman method [85]. We used InSe primarily with small chemical doping with Si, which ensures a measurable sheet resistance and intrinsic  $n$ -doping in few nm InSe few-layer films. Intrinsic InSe films of similar thickness are extremely insulating.

The most appropriate laboratory synthesis method for few-layer two-dimensional materials is limited to mechanical exfoliation for now [86]. The anodic bonding variant that we have developed in our laboratory is the one we have

exclusively used to make few-layer InSe samples and devices in this work as explained in chapter 2. Contrary to MoS<sub>2</sub> with the well know direct (monolayer)-indirect (multilayer) transition[55], InSe has a different thickness-dependent behavior with an indirect bandgap for monolayer and a direct bandgap when exceeding a specifical thickness[87]. The photoluminescence (PL) peak and absorption-induced photoconductivity of the near-band edge undergo a strong blue shift. As the number of layers decreases, the photon energy gradually increases, which causes a blue shift with higher photon energy[88].

### **3. 2 Cadmium oxide**

Transparent conductive oxide (TCO) films are important in the fields of microelectronics and nanoelectronics and are mainly used for the development of optoelectronic devices. At present, different metal oxide materials are being extensively studied in order to find a low-cost and high-performance material to replace the existing semiconductor (such as ITO). In the past, transparent conductive oxides were mainly used as conductive electrodes of electronic devices, but now, through extensive research, they can be applied to most transparent active devices. Because of this interest in applications, several deposition methods in the literature have been used to prepare thin CdO films. In our work, we choose the sol-gel method. It is a simple and cost-effective method for depositing thin films with a large area on a smooth substrate surface.

One reason for choosing CdO was the ease of making thin films of this material. Another was the high electronic mobility in this material. However CdO has a distinct disadvantage with respect to InSe in that it possesses an indirect band-gap. Nevertheless, as a fall-back material in case of failure of InSe devices because of an unforeseen bottleneck, it is a convenient choice.

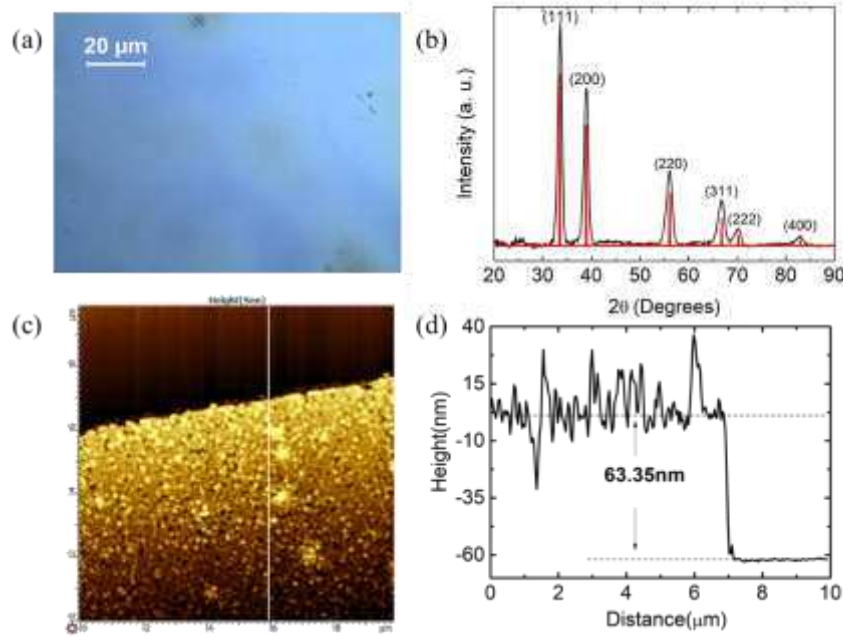


Figure 3.3 (a) Dense cadmium oxide film under X100 microscope observation. (b) XRD pattern of CdO thin films fabricated. (c) AFM topography image of CdO sample on the glass. (d) The corresponding height profiles across the paths marked by the line.

### 3. 3 Electrostatic doping of InSe and CdO

Below we give a few concepts which explain the procedure used in this work to dope our chosen materials and test the effect of doping. As explained in Chapter 2, we dope the thin film device using space charge doping and simultaneously measure the sheet resistance of the device. In some cases, the Hall effect, which needs an external magnetic field, was also measured. However, this measurement, though desirable, was not systematically possible in particular because of the large sheet resistance of InSe films.



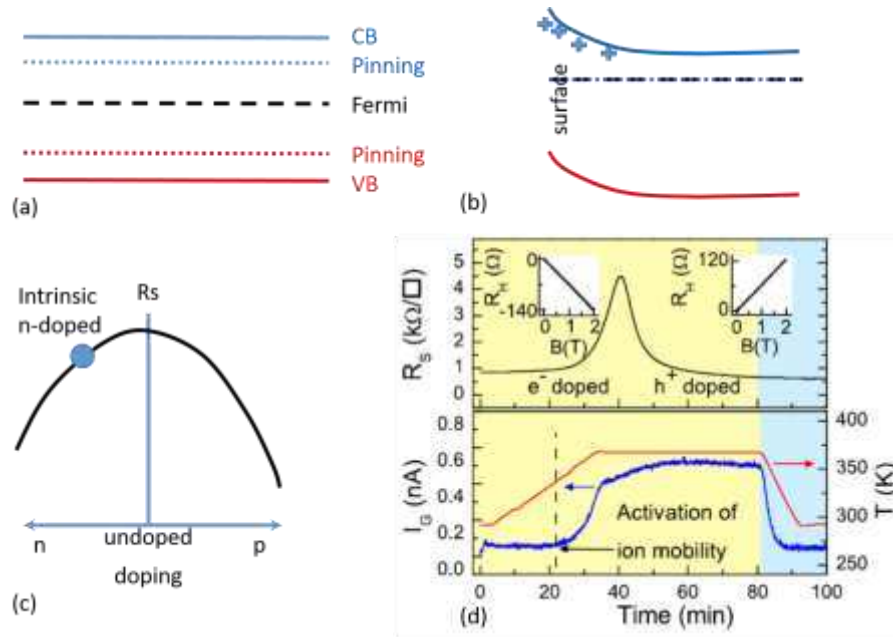


Figure 3.4 (a) Schematic band diagram of a semiconductor with the valence and conduction bands, the charge neutrality level, and pinning energy levels for defects. (b) under the field-effect through space charge doping, the surface of the sample can be charged where the Fermi level deviates from the charge neutrality level. It is the familiar concept of band-bending in device physics. (c) schematized expected behavior of the sheet resistance of a semiconductor when it is doped from its intrinsic state (here  $n$ -doped) to either a more  $n$ -doped or a  $p$  doped state. (d) the realization of this behavior is shown for the example of graphene[46].

In Figure 3.4, we give a schematic band diagram of a semiconductor with the valence and conduction bands, the charge neutrality level (which is the Fermi level for which the whole sample, and notably its surface, is neutral), and pinning energy levels for defects. In Figure 3.4 (b), we show how for example, under the field-effect through space charge doping, the surface of the sample can be charged in the surface region where the Fermi level deviates from the charge neutrality level. It is the familiar concept of band-bending in device physics. In

Figure 3.4 (c), we show the schematized expected behavior of the sheet resistance of a semiconductor when it is doped from its intrinsic state (here  $n$ -doped) to either a more  $n$ -doped or a  $p$  doped state. In Figure 3.4 (d), the realization of this behavior is shown for the example of graphene from earlier work in our group[46]. In the top panel, the sheet resistance of mono-layer graphene continuously varies from an  $n$ -doped value on the extreme left to a maximum for the intrinsic undoped sheet and then dropping again to symmetric lower sheet resistance on the  $p$  doped side. In the lower value, the details of space charge doping are shown where the sample is swept from its initial  $n$  doped state through the intrinsic and to a  $p$  doped state by the constant application of a gate voltage corresponding to  $p$ -doping. Thus, without measuring the Hall coefficient, we can qualitatively determine the polarity of the carriers by the variation of the sheet resistance as a function of the polarity of the applied gate voltage.

#### Doping and transport measurements of InSe devices

InSe samples are deposited on the soda-lime substrate through the anodic bonding method. The specific experimental process has been mentioned in chapter 2. The sample is placed in a custom made cryostat. Liquid Helium flow and a resistive heater can adjust the device temperature in the range 4-420 K. An external electromagnet capable of reaching a magnetic field of +/- 0.8T is used for Hall measurement. Space charge doping, electronic transport, and Hall measurement are all performed *in situ*.

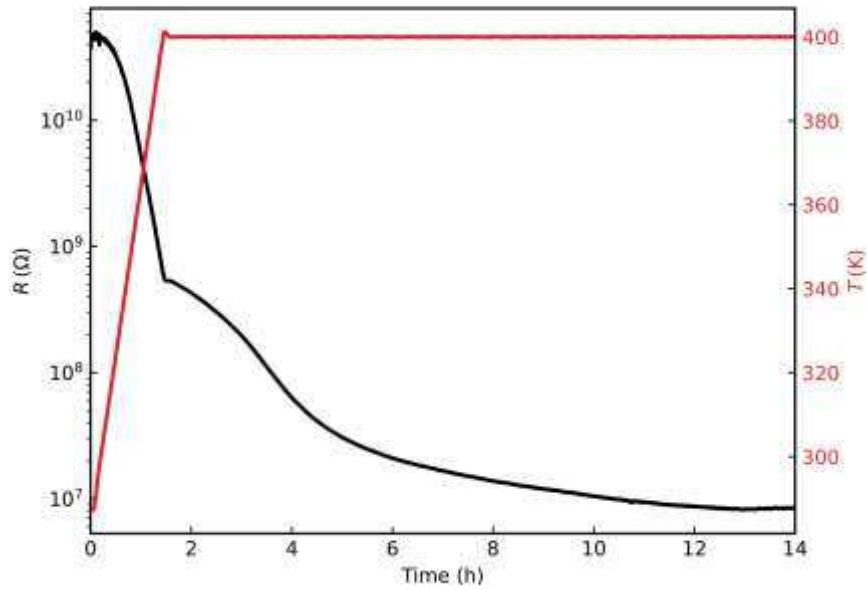


Figure 3.5 **Annealing:** typical variation of  $R_s$  in an InSe. Annealing at 400K for a few hours is in general enough to remove superficial impurities and decrease sample resistance to measurable levels.

The sheet resistance and carrier concentration were measured as a function of doping parameters (temperature, applied voltage, and polarity). The first step after placing the sample in the cryostat is annealing for removal of superficial impurities by evaporation, as shown in Figure 3.5. At first, the resistance of the sample was larger than the measuring range of the instrument. During the annealing process, the sheet resistance gradually decreased to  $M\Omega$  level. At 400K, the mobility of the ions in the glass substrate is also activated, preparing for the subsequent space charge doping of the sample [89].

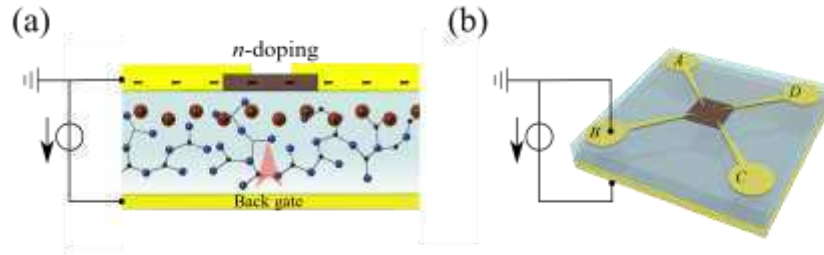


Figure 3.6 Schematic diagram of  $n$ -doping on InSe devices prepared on glass substrate. (a) Front view, (b) Perspective view.

The  $n$ -doping process by space charge doping is shown in Figure 3.6. The sheet Resistance  $R_s$  is measured with the van der Pauw method. The gate voltage is applied between the back gate and the sample. The gate current is generated by the tendency of ions to move in the glass. To a certain extent, it is an indication of doping efficiency.

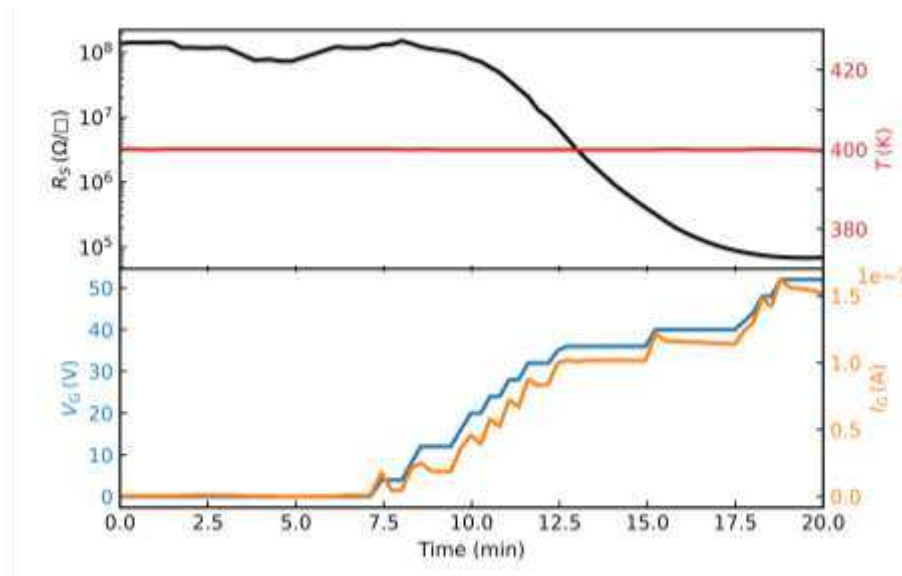


Figure 3.7 Doping of InSe sample with a positive gate voltage. The sample was heated to the doping temperature, and the voltage increase up to 50 V at 400 K.

$R_s$  (black line), gate current (orange line), gate voltage (blue line), temperature (red line).

A typical doping experiment is shown in Figure 3.7 Doping of InSe sample with a positive gate voltage. The sample was heated to the doping temperature, and the voltage increase up to 50 V at 400 K.  $R_s$  (black line), gate current (orange line), gate voltage (blue line), temperature (red line). The sample temperature is maintained at 400 K while the gate voltage is gradually increased to +50 V. The gate current is increasing with the gate voltage to values compatible with ionic drift in the glass. From the starting value of  $R_s \approx 1 \times 10^8 \Omega/\square$ ,  $R_s$  immediately decreases due to the increased space charge at the interface when the gate voltage is progressively increased to 50 V. After the  $n$ -doping process, the sheet resistance stabilizes at around  $1 \times 10^5 \Omega/\square$ , a drop of 3 orders of magnitude.

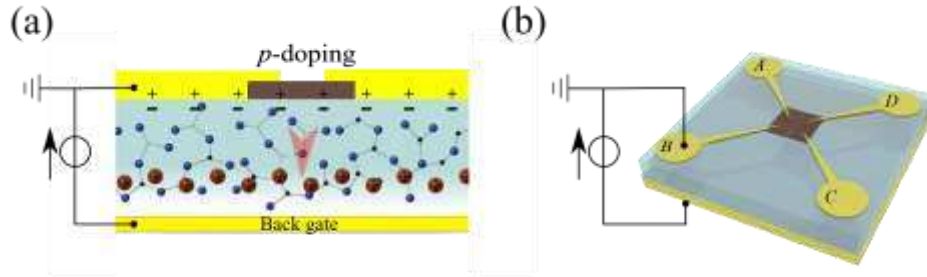


Figure 3.8 Schematic diagram of  $p$ -doping on InSe devices prepared on the glass substrate. (a) Front view, (b) Perspective view.

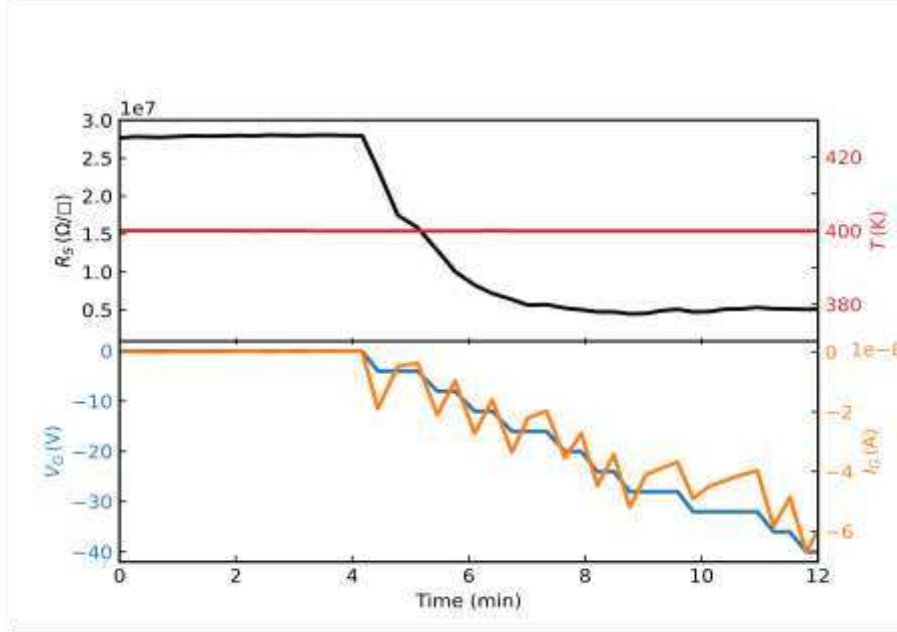


Figure 3.9 Doping of InSe sample with a negative gate voltage. The sample was heated to the doping temperature and the voltage decrease to -40 V at 400 K.

In Figure 3.8, we show the reverse process of *p*-doping for the same sample. It was first annealed overnight at 400 K with zero gate voltage  $V_G$  to neutralize the previous doping and "reset" the glass (without a gate voltage to hold them in place, the mobile ions drift back to their equilibrium position, destroying the space charge). The resulting measurements are shown in Figure 3.9. Initially  $R_s = 2.8 \times 10^7 \Omega/\square$ . We apply a gate voltage, which gradually decreases from 0 V to -40 V corresponding to hole doping. In the bottom part of Figure 3.9, it can be seen that the gate current changes the direction with the gate voltage; this is the result of the ion mobility and drift in the glass substrate. The  $\text{Na}^+$  accumulation is progressively reduced, finally leaving a negative oxygen ion space charge and a final  $R_s$  about five times lower than the initial one. In conclusion, in this sample, the initial doping state is close to the undoped state (the resistance maximum in Figure 3.7) because the resistance drops for doping of both polari-

ties. With increased  $n$  doping, the resistance decreases by three orders of magnitude. With  $p$ -doping (similar conditions for doping parameters), the resistance drops by less than an order of magnitude. This implies, as expected, that ambivalent doping is possible in these samples, and space charge doping is effective.

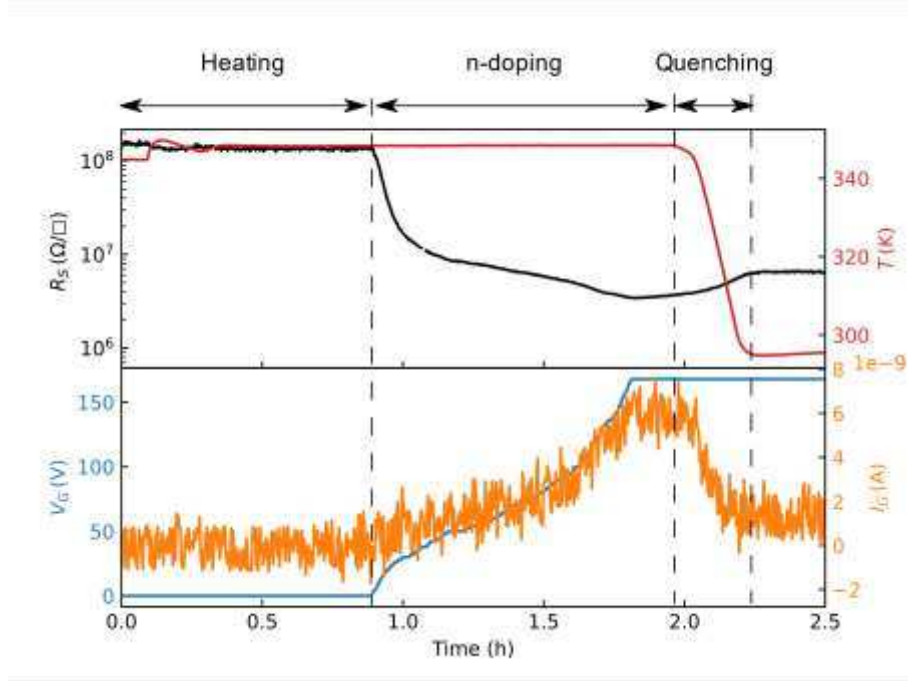


Figure 3.10 Doping of InSe sample with a positive gate voltage. The sample was heated to the doping temperature, and the voltage increase up to 168 V at 340 K.

In another InSe sample, we have tried different doping parameters. After annealing, as explained before, the doping process is shown in Figure 3.10. The initial intrinsic sheet resistance is about  $R_s = 1.1 \times 10^8 \Omega/\square$  at 340K (we use a lower doping temperature), which is a little higher than the value in Figure 3.7. As the temperature is lower, thermally excited carriers are lower, and the resistance higher. Here we quench the device to room temperature, which freezes ion mobility. The sheet resistance is again much smaller than the initial value

before doping. We thus confirm that the doping effect is retained after quenching to room temperature, and actually even in the absence of applied gate voltage since the space charge is frozen.

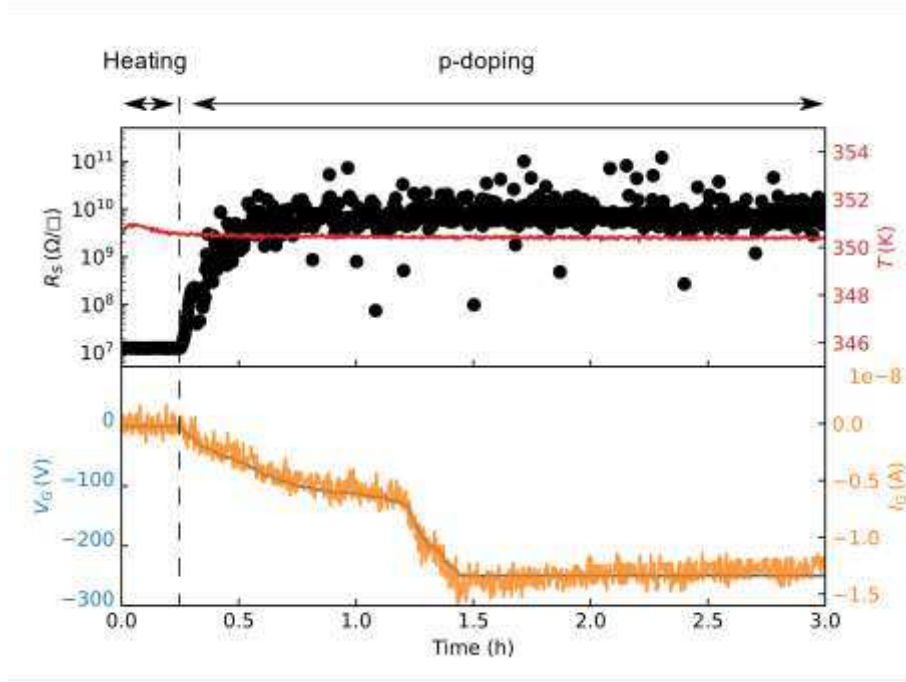


Figure 3.11 Doping of InSe sample with a negative gate voltage. The sample was heated to the doping temperature and the voltage decrease to -285 V at 350 K.

During the  $p$ -doping of the second sample, as shown in Figure 3.11, different behavior from the first InSe device appeared. After annealing operation for ‘resetting’ the device, as usual, we recovered the intrinsic sheet resistance  $R_s \approx 1 \times 10^7 \Omega/\square$ . We do the same  $p$ -doping process as Figure 3.8, except the doping temperature is kept at 350 K in line with the  $n$ -doping temperature for this device. As the gate voltage  $V_G$  gradually increases to a negative 285 V, the gate current  $I_G$  also gradually increases in the negative direction, but logically less than the value shown in Figure 3.9. This leads to an increase in the



sheet resistance of the device until the end of the experiment. At the doping temperature at 350 K, the ionic mobility in the glass is lower than at 400 K. Doping efficiency is correspondingly less. Here we can get a better idea of the initial doping condition of the device. It is actually closer to the situation indicated by the blue dot in Figure 3.4, near the undoped maximum, but in an  $n$ -doped state. So with smaller doping efficiency,  $n$ -doping results in lower  $R_s$ , but  $p$ -doping, which is now not efficient enough to dope the device to  $p$  polarity, probably transform it to an undoped state, near the resistance maximum, with the Fermi level corresponding to the charge neutrality level.

#### Hall measurements on InSe devices.

We now discuss Hall effect measurements to quantify the effect of doping on our devices. Both charge carrier densities and the Hall mobility are estimated after the various doping operations.

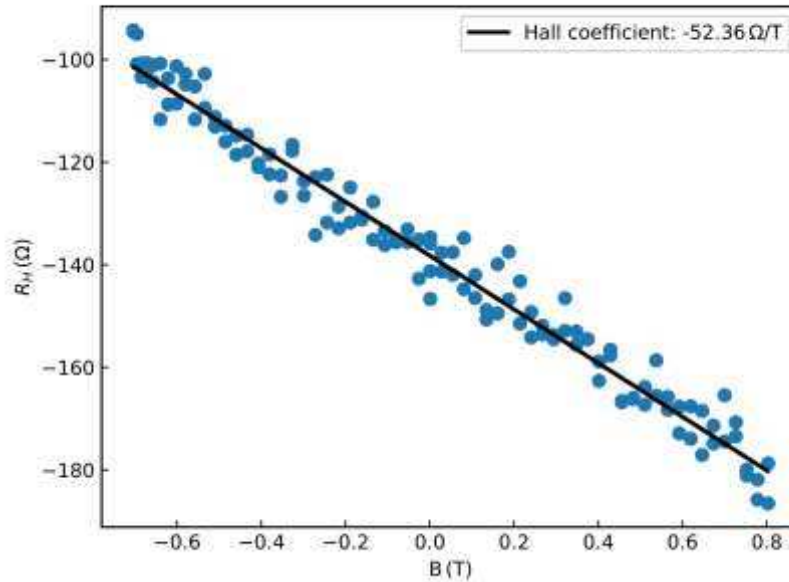


Figure 3.12 the Hall measurement of InSe at 400K.

The Hall measurement of another InSe sample taken at 400 K before any space charge doping is shown in Figure 3.12. The sheet resistance at this time is  $R_s = 1.06 \times 10^5 \Omega/\square$ , from the slope of the Hall voltage with the magnetic field, we get the carrier density  $n_s = 1.2 \times 10^{13} \text{ cm}^{-2}$ , and the Hall mobility  $\mu = 4.93 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . This sample has been doped at 400 K with only +20 V gate voltage, resulting in a final resistance of  $\sim 2.5 \times 10^4 \Omega/\square$  at 400 K. After the  $n$ -doping and quenching, the Hall measurement result is shown in Figure 3.13.

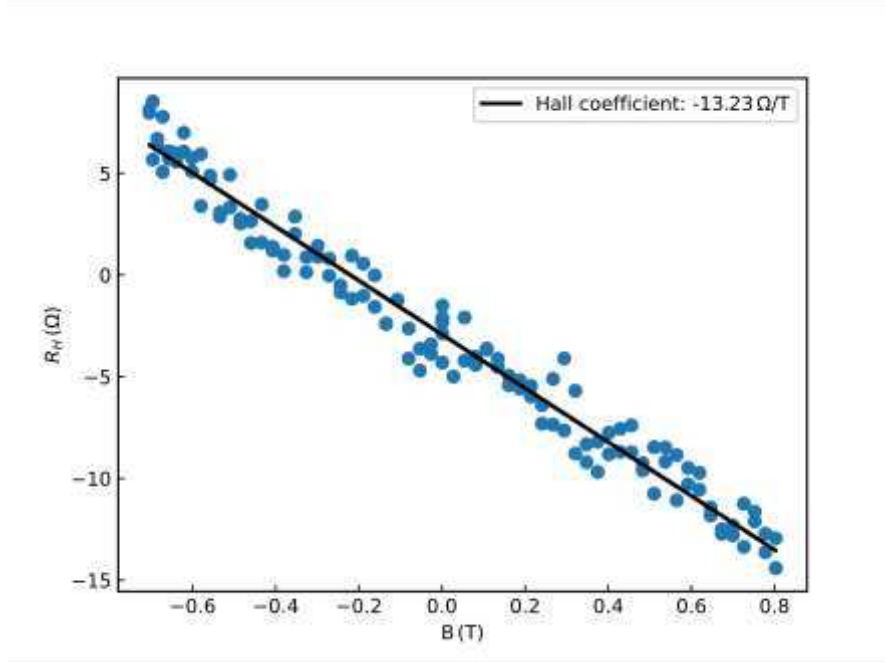


Figure 3.13 the Hall measurement of InSe after  $n$ -doping at 295 K.

The  $n_s$  is  $4.74 \times 10^{13} \text{ cm}^{-2}$ , at room temperature, which is a much higher carrier concentration than before. The Hall mobility at 295 K is  $2.58 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ ,

which is lower than before the doping, however, these numbers cannot be directly compared as they were measured at different temperatures. Unfortunately, we could not reproduce this experiment with a  $p$ -doping (because some contacts were unstable), but we have shown that space charge doping can reversibly  $n$ -dope and  $p$ -dope few-layer InSe samples with substantial changes in carrier density.

#### Doping and transport measurements of CdO devices

CdO devices were made by the sol-gel method. The thin films were, in general, about 50 nm thick. It is not an ideal thickness for the space charge doping method where the electrostatic doping is effective over about a few nm nearest to the glass surface. Since the sheet resistance is relatively low in these films, the effect of doping and especially the quantification through the Hall effect are problematic because of the parasite contribution of the undoped top part of the ‘thick’ film. A device of CdO (Figure 3.14) was doped continuously for a few hours with a negative gate voltage. As can be seen in Figure 3.14, the sheet resistance of the sample undergoes a bell-shaped transformation, increasing, then passing through a maximum and then decreasing again. It indicates that the initial doping is of  $n$ -polarity, as in the case of InSe and the situation shown in the schematic diagram of Figure 3.4. We thus confirm that in CdO, as in InSe, we can dope the device in an ambivalent manner with both  $n$  and  $p$  polarity.

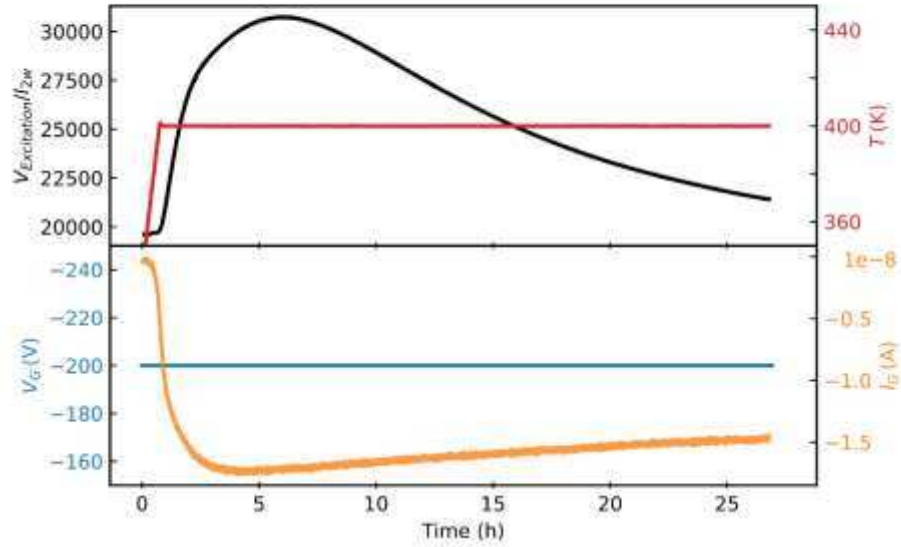


Figure 3.14 Doping of CdO sample with a negative gate voltage. The sample was heated to the doping temperature with 400K and the voltage with -200 V.

#### Hall measurements on CdO devices.

As for InSe, we discuss Hall effect measurements to quantify the effect of doping in our CdO devices. Both charge carrier densities and the Hall mobility are estimated after various doping operations.

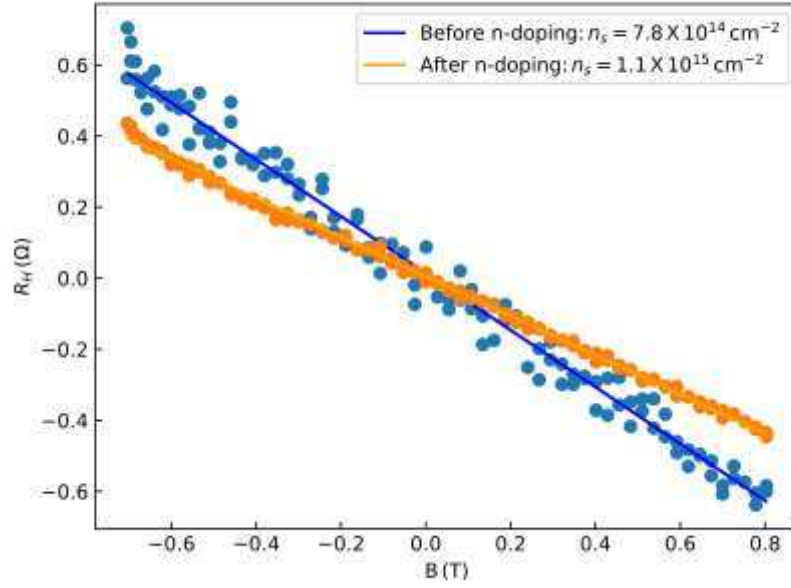


Figure 3.15 the Hall measurement of CdO before and after  $n$ -doping at room temperature.

A Hall measurement before and after the  $n$ -doping of a CdO device is shown in Figure 3.15. The measurement indicates that the carrier concentration during the  $n$ -doping process only marginally increased. The electron mobility also increased marginally from  $\mu_{H\text{-before}} = 2.85 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  to  $\mu_{H\text{-after}} = 3.22 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  respectively. This marginal increase with respect to the large increase seen in InSe is due to two reasons. Firstly the doping process itself is less effective given the high initial carrier concentration in CdO. In effect, the sheet resistance is several orders of magnitude lower than in InSe. Secondly, as we pointed out earlier, the sample is relatively thick, the undoped top part of the sample prevents a true quantitative estimation of parameters.

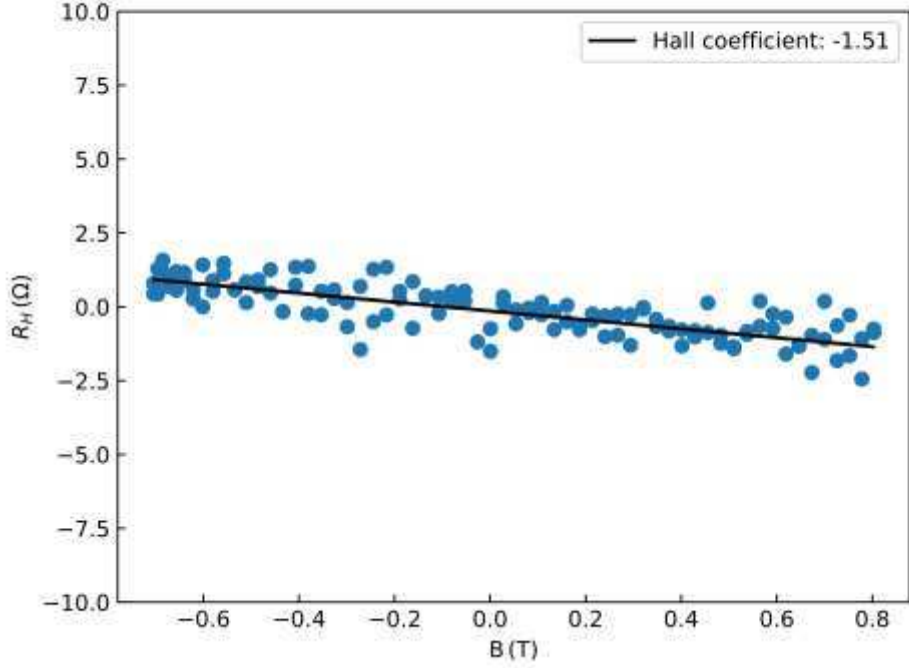


Figure 3.16 the Hall measurement of CdO after  $p$ -doping at 285 K.

In Figure 3.16, we show the Hall effect measurement for the CdO device of Figure 3.15, which was nominally doped from  $n$  to  $p$  polarity according to the sheet resistance as a function of doping. However, from the slope of the measured Hall resistance, we deduce  $n$  polarity for the doping for a sample, which is nominally  $p$  doped. Clearly, the effect of the sample thickness is responsible for this misleading result. While a few nm of the device closest to the glass surface probably change polarity as seen from the sheet resistance measurement, the bulk of the device maintains its  $n$  polarity as seen from the Hall measurement with a measured carrier concentration of  $n_s = 4.43 \times 10^{14} \text{ cm}^{-2}$  and a measured mobility  $\mu_H = 1.08 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .

### 3. 4 Choice of InSe

From the above results and discussion, it is clear that we can make devices of InSe and CdO, which we can dope in an ambivalent manner with both  $n$  and  $p$  polarity using our space charge doping technique. This is the basic criterion for fabricating a bipolar device. We can now progress to the fabrication of a bipolar device. However, we have a choice of two materials. Our final choice is to proceed with InSe. This choice was decided on the basis of the arguments which we exposed at the beginning of the chapter:

1. The bandgap of InSe varies from 1.26 eV (single layer) to 1.45 eV (bulk) according to the number of layers, and the gap changes from indirect to direct when the thickness increases, with the transition taking place between 5-7 layers. In this work, all InSe devices have a thickness between 10 and 15 layers, and the band-gap is thus direct.
2. The material must lend itself to reasonably easy device fabrication. Our anodic bonding technology and shadow mask technique for 2D materials is ideally suited for making InSe devices. For layered materials, making homogenous ultra-thin devices is easier than in materials like CdO made with the sol-get technique.
3. We need materials with reasonable resistance to ambient conditions. Ultra-thin InSe has been shown to resist to ambient conditions up to a few days[[15](#), [84](#)].
4. The possibility of doping in an ambivalent way, which is to say with both  $n$  and  $p$ -type carriers, has been demonstrated above for InSe.

In the next chapter, we will tackle the important and difficult challenge of achieving a bipolar device by successfully creating differential doping by the space charge method in a device of lateral size ~50 micrometers.

## Chapter 4.

# Formation of a tunable $p$ - $n$ junction in InSe through Space Charge Dop- ing

As different types of new two-dimensional materials have been continuously developed, some early research topics used in traditional materials have been re-excavated and used in the research of two-dimensional materials, and a series of studies have been developed on this basis. Among them, like the research of  $p$ - $n$  junction, the rise of two-dimensional material research has brought some possibilities that conventional bulk semiconductor materials cannot realize, and provided some new  $p$ - $n$  junction device configurations with flexible and excellent characteristics.

The stacking of two different two-dimensional materials is one of the most efficient strategies for preparing  $p$ - $n$  heterostructures. The different band gap values and doping types of two-dimensional materials provide various combinations of possibilities for  $p$ - $n$  junction structures. With the van der Waals heterostructure, the premier cases of thin  $p$ - $n$  junction invented by stacking  $n$ -type 2D material onto a  $p$ -type 2D material were demonstrated by Fang[\[59\]](#). Among the different two-dimensional materials, the previous studies and attempts on



TMDC materials are obviously the most common, such as WSe<sub>2</sub>-MoSe<sub>2</sub>[60], and there are also attempts to combine TMDC materials with other materials to form junctions, such as sandwiched junction with graphene introduced for MoS<sub>2</sub>-WSe<sub>2</sub> devices[61], or a combination of a material and a TMDC material, such as BP-MoS<sub>2</sub> vertical  $p$ - $n$  junction[62].

In addition, homojunction devices have also emerged at the same time. Homojunction means that the  $n$ -region and  $p$ -region of the  $p$ - $n$  junction are made of the same material, as for example, like a  $p$ - $n$  junction based on a single WSe<sub>2</sub> flake[63]. In this device, the  $p$ - $n$  junction is based on quantum-confinement effects between different layers. The metal contacts are placed on the single-layer WSe<sub>2</sub> and the double-layer WSe<sub>2</sub>, respectively. Homojunction can also be achieved by means of doping, which can be divided into chemical doping and electrostatic doping. The reduced thickness of 2D materials usually gives more flexible possibilities to external doping atoms or carriers introduced by chemical methods or electronic fields.

In this chapter, we focus on doping our thin-film devices with the space charge doping technique to realize a homojunction in InSe. After the successful attempts at doping the entire InSe device with the same polarity here, we will try to dope one side of the device with  $p$  polarity and the other side with  $n$  polarity. The challenge is thus to make an electrostatically doped lateral homojunction in a few-layer ( $\sim 10$  nm thick) InSe device with a lateral size of  $\sim 50$  micrometers.

## **4.1 Starting premise**

The principle of ambipolar doping is based on the space charge doping technique. We can think of the process of ambipolar doping as the process of simultaneous localized and differentiated space charge doping. In the previous chapter, we mentioned that the space charge doping process uses the electric field applied between the back gate and the device (the 2D material and the gold contacts) to drive the movement of ions in the glass. The space charge is formed

at the interface between the sample and the glass to achieve the purpose of electrical doping.

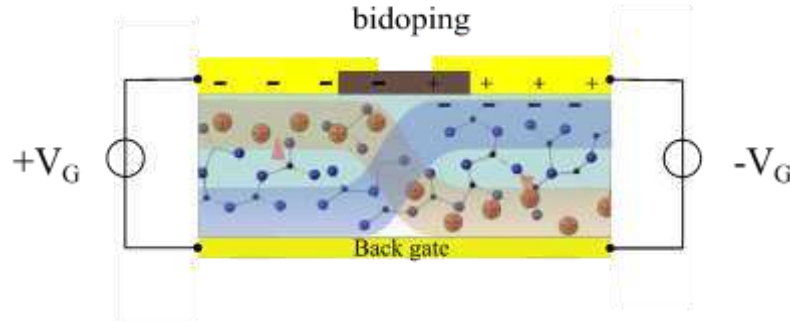


Figure 4.1 A schematic view of the simplest achievement of bipolar space charge doping.

As schematically shown in Figure 4.1, our aim is to achieve a 2D layered diode with the new technology developed in our laboratory, namely space charge doping, to dope the device simultaneously  $n$  and  $p$  in different parts so as to form a junction at the border between the two parts. This doping method does not introduce foreign atoms, defects or impurities, and the parameters (Gate voltage and sample temperature) are easy to control. To achieve this aim, we used two different sample geometries. Both resulted in devices with unidirectional current flow. In the next sections, we specify these two geometries, show the results obtained with each geometry and discuss them.

In the basic configuration, as explained in Chapter 2, four Au contacts are placed at four corners of the sample using Au evaporation through a shadow mask. This configuration is then modified with a micromanipulator and a metallic tip to mechanically shape the InSe thin film at the appropriate positions to obtain two different geometries. This ensures reliable in-situ measurement of resistance as well as space charge doping. Two different configurations were used and they are explained in detail in the following.

## **4. 2 Double side gates**

The first approach we use seeks to circumvent the constraints that are imposed by our rudimentary initial device geometry. Remember that we do not use photolithography or bottom-up growth methods to ensure minimum chemical contamination and good crystalline quality of the sample. Our sample and device shape is not deterministic and the contact geometry is imposed by the shadow mask. Given these constraints, we asked ourselves the best way to obtain localized  $n$  and  $p$  doping in the device. We decided that the use of the back gate (Figure 4.1) may not be precise enough to obtain the desired differentiated doping and a more effective way would be to ensure that the two zones of the sample ( $n$  and  $p$ ) were clearly delimited by ‘side’ gates. Side gates are electrodes which are placed ‘close’ to the zone of the sample to be electrostatically doped but not in electrical contact. By ‘close’, we mean considerably less than the distance to the back gate, which is 500 micrometers. Typically this geometry is achieved with a side gate distance between 30 and 100 micrometers. Below we give a more detailed explanation of how this geometry is achieved and the experiments performed with it.

This device geometry allows simultaneous space charge doping and measurement of the  $I$ - $V$  characteristics. This is achieved by shaping the few layers InSe with needles, as shown in Figure 4.2. The shaping creates a channel of InSe with a “V” shape connected to two gold source and drain contacts (which will become the anode and cathode of the diode), while the tip of the “V” sits between two other gold strips without touching them. Hence the two insulated gold strips form two side-gates that can be polarized through space charge doping without having a gate current going directly through the InSe layer. Since the doping circuit is disconnected from the device circuit in this configuration, we can measure the  $I$ - $V$  characteristics of the device during the doping. The two side-gate voltages being independent and applied with respect to the grounded back-gate, we can polarize both gates with the same sign (positive or negative)

to achieve unipolar doping of the sample, or with opposite sign to create a p-n junction in the tip of the “V”.

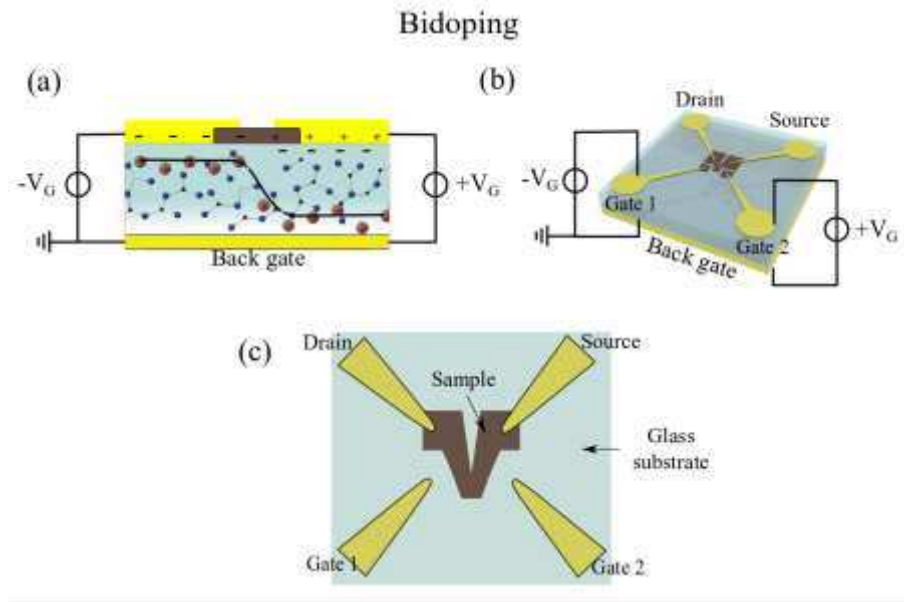


Figure 4.2 Schematic of bipolar doping on InSe devices prepared on the glass substrate. (a) Front view, different space charge accumulation caused by ambipolar ions draft in separate contacts. (b) Perspective view, two contacts set as side gates to provide ambipolar space charge doping, the  $I$ - $V$  characterization of the junction is measured with source and drain contacts. (c) schematic view of a contacted InSe sample mechanically shaped to the device geometry.

We present the first results of ambipolar doping on an InSe sample. As shown in Figure 4.3, the undoped device had a large resistance of  $5 \times 10^9 \Omega/\square$ . Applying asymmetrically positive voltage ( $n$ -doping) on both side-gates rapidly increased the current flowing through the device, while keeping the  $I$ - $V$  characteristic almost linear, thus decreasing the resistance. After a few volts, the resistance appears to saturate at  $1 \times 10^7 \Omega/\square$ .

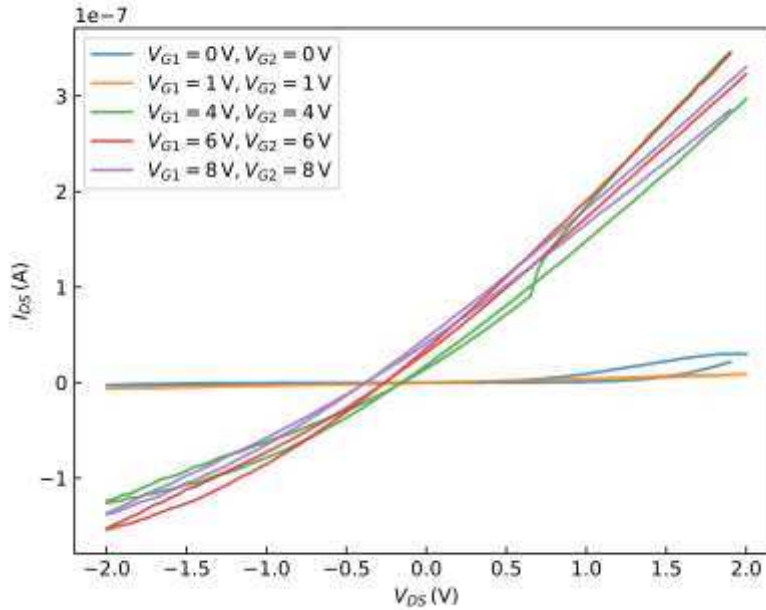


Figure 4.3  $I$ - $V$  characteristics of unipolar *n*-type space charge doping at .350K

After an annealing cycle to remove the previous space charge, the device can be polarized symmetrically in the opposite direction. As shown in Figure 4.4, the current in the device rapidly increases with *p*-doping, although the effect is smaller than with *n*-doping. These experiments need more explanations, as two effects are seen in the measurements:

- First, the slope of the  $I$ - $V$  characteristic is increasing, which represents the change in resistance of the device.

- Second, an offset is appearing and increasing with gate voltage. The offset can be measured at  $V_{ds} = 0$  V and is an artifact of the measurement configuration. Indeed, one contact (usually the source) is grounded, and so connected to the back-gate. Hence, part of the doping current is measured in the  $I$ - $V$ , creating the offset. (Note that the offset is also present in Figure 4.3) but it is more apparent in *p*-doping as the changes in resistance are smaller).

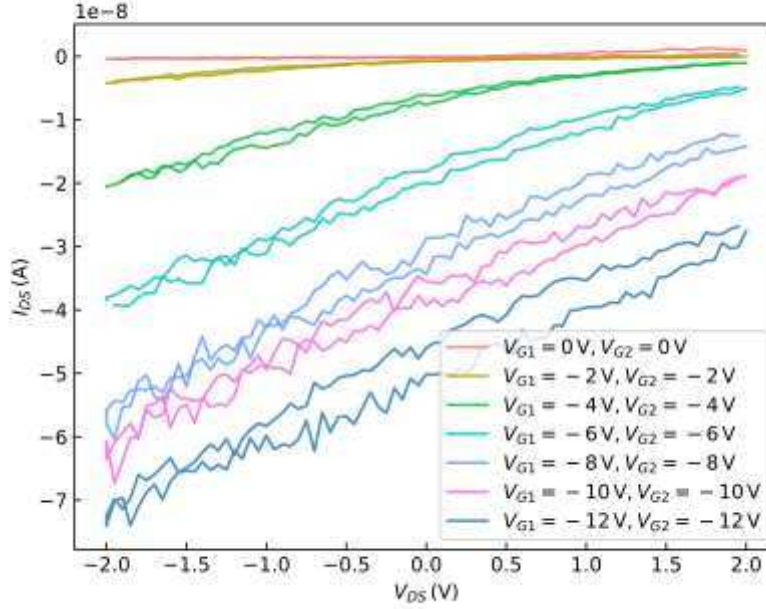


Figure 4.4  $I$ - $V$  characteristics of unipolar *p*-type space charge doping at 350K.

These two experiments are important to establish the validity of our approach as they demonstrate that two side-gates can be used effectively for space charge doping, with similar results compared to chapter 3. Indeed, the doping can change the resistance of the device by one or two orders of magnitude and is more effective on the *n*-side than on the *p*-side. We can also mention the major differences between back-gate doping and side-gate doping. First, the side-gate geometry does not ensure that the sample is uniformly doped, so it is irrelevant to compare the doping amplitudes quantitatively between the two geometries as parts of the device might be more resistive than others at any doping. Second, even considering the previous point, we can see that measurable changes in resistance occur at low voltages compared to the back-gate geometry, which would imply an increased doping efficiency with side-gate doping, albeit a localized

one. This is due to the reduced gate to sample distance, which effectively determines the field felt by the ions in the glass.

We can now present the results of asymmetric ambipolar doping. The sample was first annealed to removed previous doping attempts in the glass. Then, at the doping temperature of 350 K, one side-gate was polarized at a positive voltage, while the other side-gate was polarized to the opposite voltage. The  $I$ - $V$  characteristic was measured between  $\pm 4$  V during the doping process. As shown in Figure 4.5, we see the appearance of a rectifying behavior at relatively voltages ( $\pm 4$  V). We also see the appearance of a pronounced hysteresis in the  $I$ - $V$  curve.

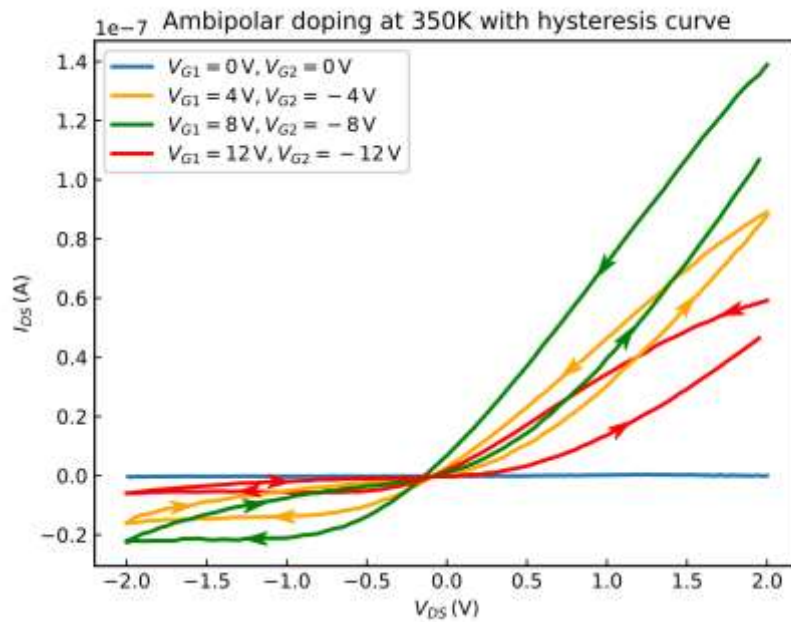


Figure 4.5  $I$ - $V$  characteristic curve after ambipolar doping mode at 350K with hysteresis.

We first try to explain the appearance of the hysteresis, which is related to temperature variations in the device during the measurements. Indeed, it is well known that the  $I$ - $V$  characteristics of diodes are susceptible to temperatures. According to the Shockley equation, the forward bias current is dominated by an exponential negatively dependent on temperature (i.e., at a given voltage, the current will decrease with increasing temperature). On the opposite, the reverse saturation current is also exponential but positively dependant on the temperature.

The current through an ideal, defect-free  $p$ - $n$  junction is described by the Shockley equation, given by

$$I_D = I_S \left( e^{\frac{qV_D}{nkT}} - 1 \right) \quad 4.1$$

whereby  $V_D$  is the extremally applied bias,  $k$  is Boltzmann constant,  $n$  is known as the ideal diode factor, and the saturation current  $I_S$  is

$$I_S = K_1 T^{\frac{5}{2}} e^{\frac{-E_g}{2kT}} \quad 4.2$$

Where  $K_1$  is a coefficient related to the material and geometry of the junction,  $E_g$  is the energy gap of materials[90].

Hence the behavior of a given diode depends on which temperature dependence prevails over the other. For instance, in silicon diodes, the forward current increases with increasing temperature, known as a *negative* temperature coefficient. Here we see on the forward characteristic that after the voltage has reached its maximum value in the forward sweep, the current measured in the backward sweep is larger. Considering that maximum heating occurs at the maximum power, it is plausible that the temperature of the junction is higher at the beginning of the backward sweep. We will therefore assume that our diode device behaves similarly to silicon diodes, i.e., the current at a given voltage increases with temperature.



We have established a very simple preliminary model to simulate the behavior of a diode with similar characteristics. First, the model considers only a perfect Schokley diode, with a particular ideality factor, and behaves as a negative temperature coefficient diode (the temperature coefficient is usually defined from the behavior of the voltage at constant current, rather than current at a constant voltage, hence it is negative here). Second, we consider a dynamical model in which we increase/decrease the input voltage at regular time steps ( $dt$ ). Third, at each new step, the temperature is modified by the electrical power in the junction and the cooling effect of the environment (substrate, gold contacts) through Newton's law of cooling.

$$\frac{dT}{dt} = R_{th}JV + \frac{T_0 - T}{\tau} \quad 4.3$$

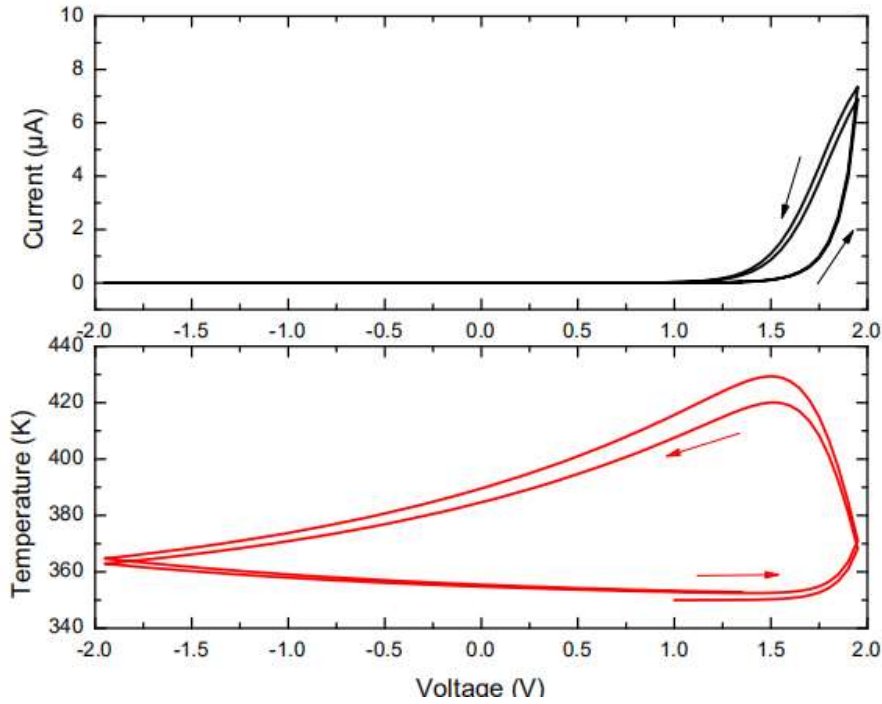


Figure 4.6 Simulation of a dynamical  $I$ - $V$  characteristic (top) and temperature (bottom) of a negative temperature coefficient diode. The simulation starts at +1V and 350 K.

As shown in Figure 4.6, with carefully chosen coefficients, we can qualitatively reproduce a similar hysteresis, as seen in our samples. However, two points can be raised:

\* The overall shape of the curve is very different from our experiments. This is most likely caused by the imperfections of our device that cannot be grasped by the perfect Schokley equation. A circuit with a resistance in series and another in parallel with the diode is a probably more accurate model of our device. However, the  $I$ - $V$  characteristics of such circuits are more complex to compute.

\* The coefficients used in the model are arbitrarily chosen without physical consideration, so it is not a quantitative model at this point.

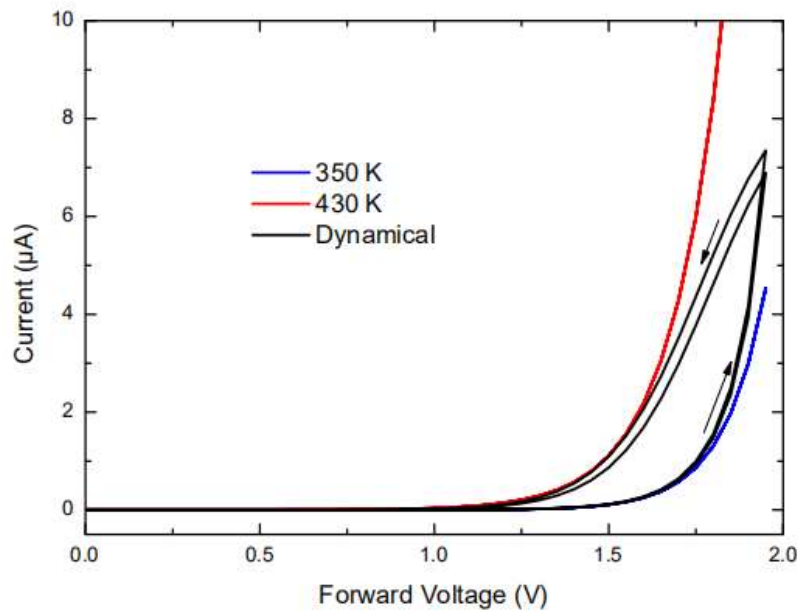


Figure 4.7 Comparison between the simulation presented in Figure 4.6 and an ideal diode at the two extreme temperatures.

Nevertheless, this simulation can give some insight into how to interpret experimental data. We have shown in Figure 4.7, the  $I$ - $V$  characteristic (limited to the forward part) of the dynamical simulation and compared it to the  $I$ - $V$  characteristic at constant temperatures for 350 K and 430 K (resp. minimum and maximum temperature in the simulation). While the simulation is clearly different from the two constant temperature curves, the forward sweep is clearly closer to the 350 K curve than the backward curve is to the 430 K. Indeed, as can be seen in Figure 4.6, while the backward sweep begins, the power output is still high enough to keep the temperature increase, and the diode only reaches a maximum temperature at 1.5 V. This behavior produces the more linear backward sweep curve seen in the simulation, and presumably in the experiment. Therefore, we can postulate that thermal effects are less important in the forward voltage sweep of the voltage characteristic. In the following discussion, we have thus separated forward sweeps and backward sweeps.

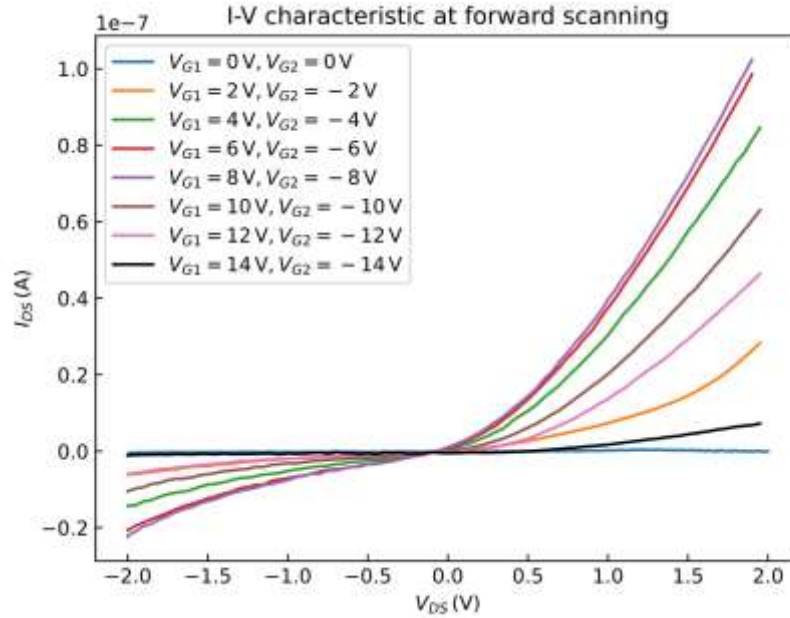


Figure 4.8  $I$ - $V$  characteristic curve after ambipolar doping at 350 K with only forward direction scanning.

The forward sweeps are shown in Figure 4.8. The diode-like rectification appears as soon as  $\pm 2$  V and increases with increasing voltage up to  $\pm 8$  V. Subsequent increases in doping voltages result in the diminution of current in the device. The degradation of the diode-like characteristic after  $\pm 8$  V may come from an irreversible degradation of the InSe layers at high doping levels.

Considering the most diode-like curves (e.g.,  $\pm 6$  V or  $\pm 8$  V), the  $I$ - $V$  curve, even in the forward sweep direction, is quite far from an ideal diode. This could be the result of non-negligible resistances acting in series and in parallel to the junction[64]. However, a detailed model has not been attempted at this point since, as we have shown in the model, thermal effects are most likely not negligible.

### **4.3 Two contact method**

An alternative, simpler, approach to implement ambipolar doping is to connect only two contacts on the sample and shape it in a narrow strip between these, as shown in Figure 4.9. This geometry is easier to implement than the double side gate method. However, it does not allow us to measure and dope simultaneously. Hence the difference in specific operations is that we distinguish the doping process from the two-wire  $I$ - $V$  measurement. The back gate under the glass is used as a unified reference to link the ground, and the two different side gates offer electric fields in two different directions. First, we will perform ambipolar doping at the doping temperature on the sample (Figure 4.9 (a) and (b)). After the doping process, the device is cooled to room temperature while maintaining the gate voltages, in order to freeze the accumulated space charges. The  $I$ - $V$  characteristic curve is then measured at room temperature (Figure 4.9 (c) and (d)).

While this method does not offer real-time  $I$ - $V$  characteristics, and also has the inconvenient of having both the glass and InSe connected in parallel during the doping (which means that some of the gate currents is lost in the InSe

and does not contribute to doping), many trials and errors gave the interesting results presented below.

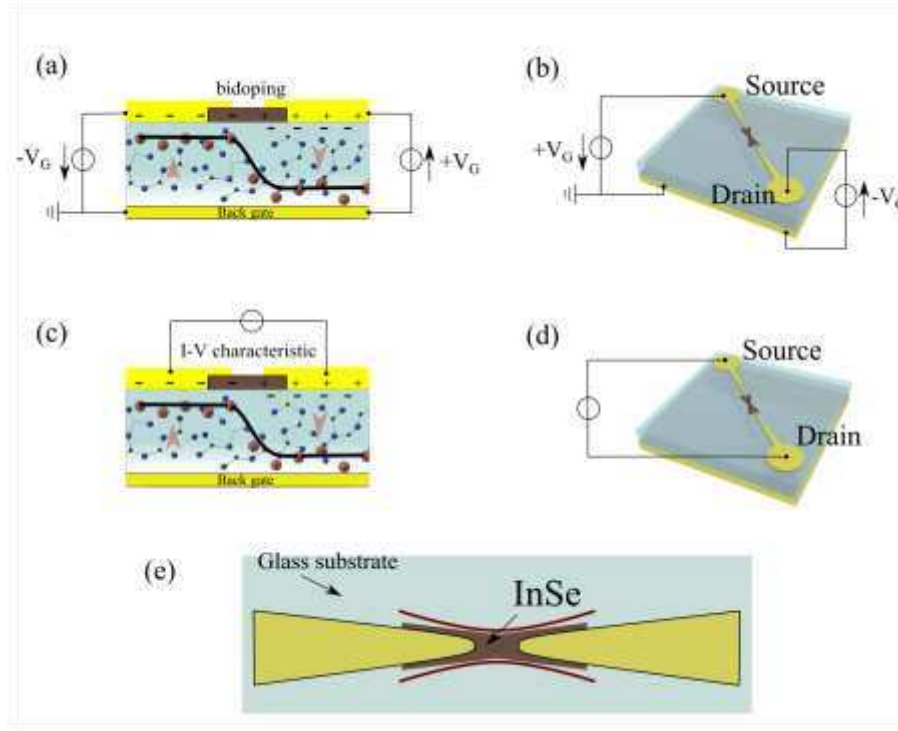


Figure 4.9 Schematic of ambipolar doping InSe with two contacts on the glass substrate. (a) Front view. (b) Perspective view. (c) I-V measurements after doping and quenching, front view (d) Perspective view, (e) schematics of the device geometry. The sample is mechanically shaped like a narrow strip.

After doping the sample with ambipolar  $\pm 4$  V at temperature 350K for 30 minutes, the samples were cooled to room temperature, and the IV characteristic was measured. As shown in Figure 4.10, there is a pronounced rectifying effect. However, there is also a pronounced hysteresis and a dependence on the number of cycles.

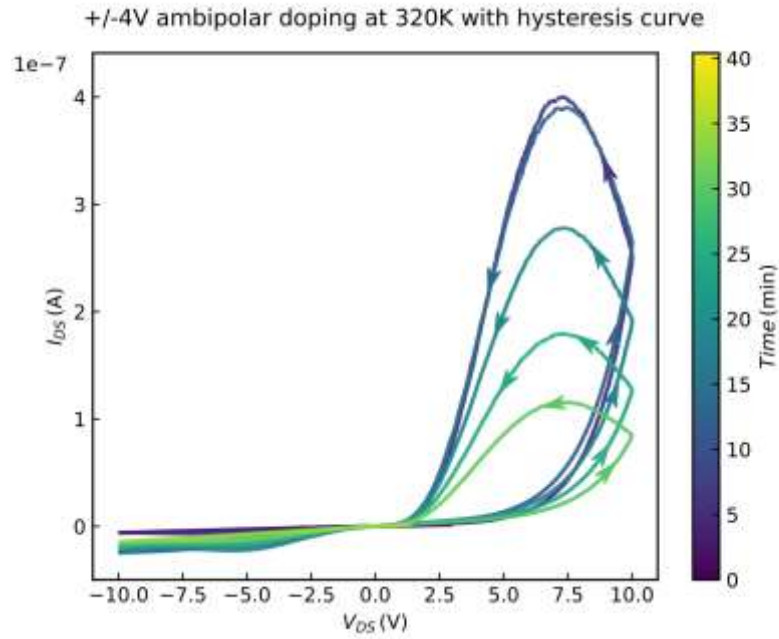


Figure 4.10 +/-4 V ambipolar doping mode at 320 K with hysteresis curves.

As for the double side-gate configuration, we can associate the hysteresis with heating effects during the sweep. Indeed, with a simulation similar to the one presented in chapter 4. 2, we can show that thermal effects can produce the characteristic non-monotonous behavior seen during the backward sweep. Such a simulation is presented in Figure 4.11 (parameters have been adapted to the voltage range and diode characteristics of this device).

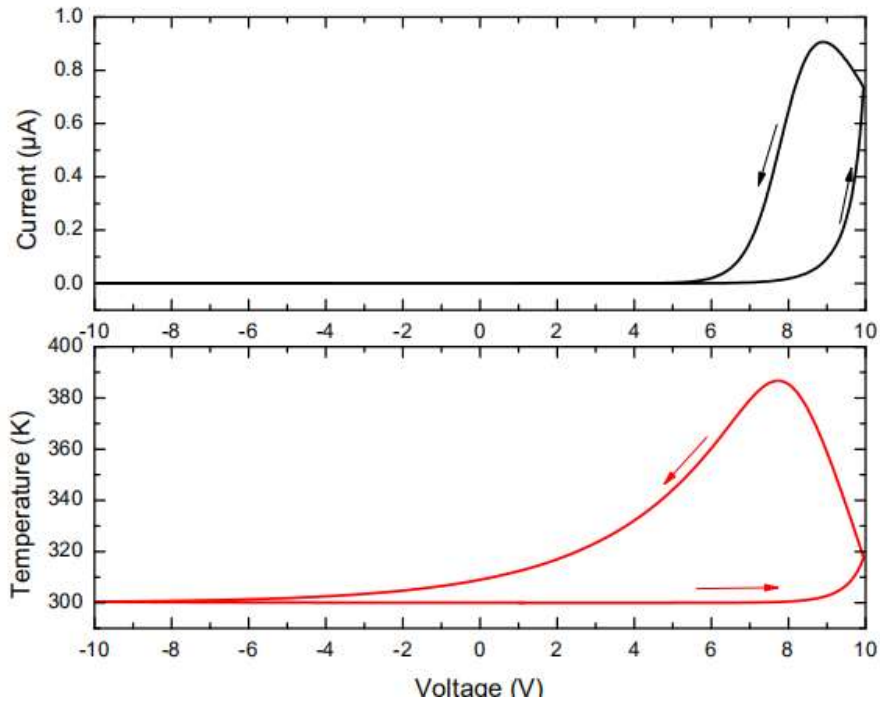


Figure 4.11 Simulation of a dynamical  $I$ - $V$  characteristic (top) and temperature (bottom) of a negative temperature coefficient diode. The simulation starts at +1V and 300 K.

The effect of temperature also explains the temporal dependence of the  $I$ - $V$  curve. Indeed, as each cycle locally heats the junction and its surroundings (i.e., the glass substrate), the mobility of sodium ions in the glass below the junction is periodically activated, thus removing part of the accumulated space charges that produce the  $n$  and  $p$  doping. Hence, each cycle removes the doping little by little.

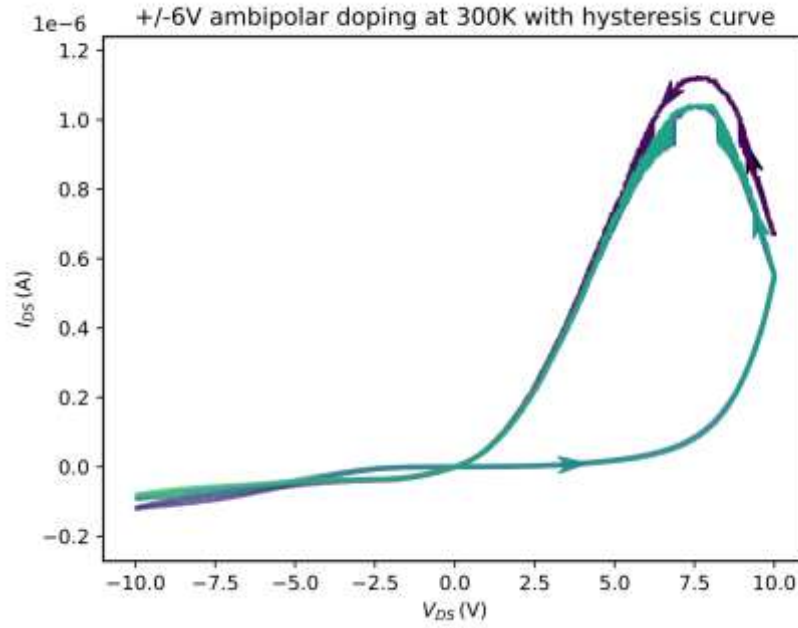


Figure 4.12 +/-6 V ambipolar doping mode at 300 K with hysteresis curves

The experiment was repeated with different doping parameters: +6 V and -6 V at 350 K for 30 minutes ( $I$ - $V$  at room temperature shown in Figure 4.12), then +2 V and -4V at 350 K for 30 minutes ( $I$ - $V$  at room temperature shown in Figure 4.13).



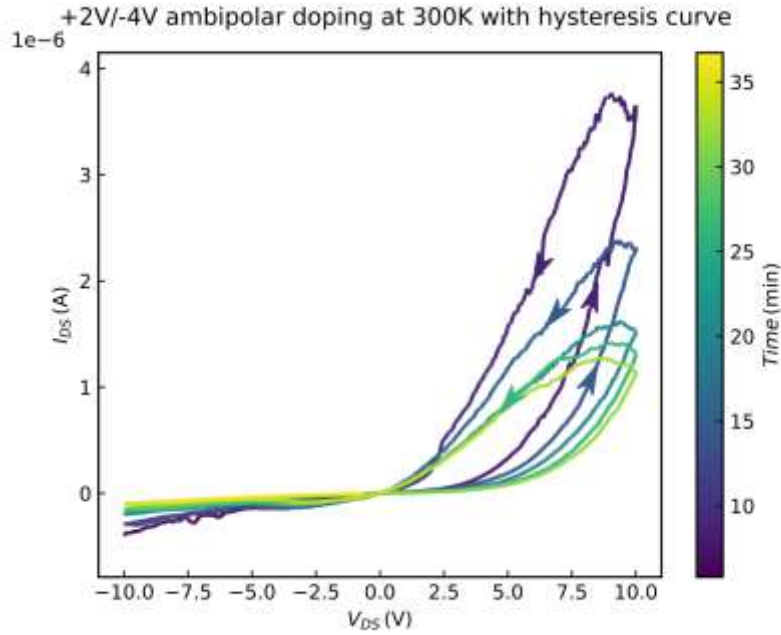


Figure 4.13 +2/-4 V ambipolar doping mode at 300 K with hysteresis curves

The results appear to be similar with different doping parameters. We found that ambipolar doping caused the sample to have a significant rectification effect, and this rectification effect increases as the difference between the side gates increases. However, in all experiments, the space charge accumulated at the interface of InSe and the substrate gradually vanishes as power going through the device locally heats the substrate. So, even if the value of the side gate controls the rectification effect of the diode, the  $I$ - $V$  characteristics evolve gradually over time.

A comparison of the initial  $I$ - $V$  characteristics at room temperature after the different ambipolar dopings is shown in Figure 4.14. It appears that the last doping with asymmetric values for doping is the most effective to get a rectifying diode behavior. This might be explained by the intrinsic doping behavior of InSe, which is more easily  $n$ -doped than  $p$ -doped. Hence a greater value of negative voltage might be needed to produce a  $p$ -doping level equivalent to the  $n$ -doping.

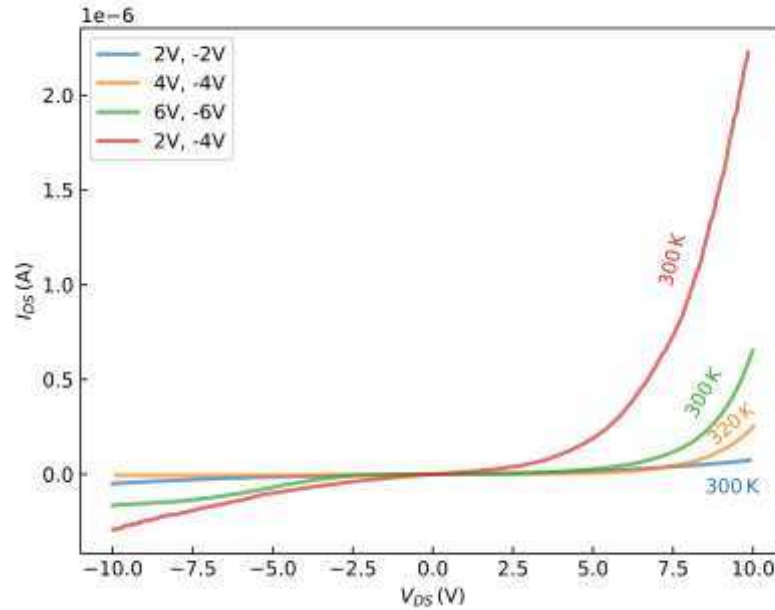


Figure 4.14 Comparison of  $I$ - $V$  characteristic curves with different parameters under forwarding scanning.

#### 4. 4 Discussion of results and conclusion

We have shown for the case of InSe that a few-layer device can be doped in a localized and differentiated way such that one zone is doped with  $n$  polarity and another zone with  $p$  polarity, with a junction separating them. This has been achieved with two different geometries both for the doping and for the  $I$ - $V$  measurement, clearly showing that the measured behavior is that of a rectifying junction and not some other effect or artifact.

Qualitative simulations based on the ideal diode equation for the  $I$ - $V$  characteristics and Newton's law of cooling for the heat dissipation in the device are convincingly close to the measured characteristics to conclude that:

1) Thermal dissipation in the devices causes continuous temperature change during  $I$ - $V$  measurement resulting in hysteresis and eventual loss of doping because of space charge drift and loss. The heat generation itself is due to the forward current and the high resistance of InSe, the small size of the device, which results in negligible thermal inertia, and eventually, the glass substrate, which is not a good thermal conductor. These conclusions are further justified by the near lack of hysteresis in the reverse bias part of the characteristics.

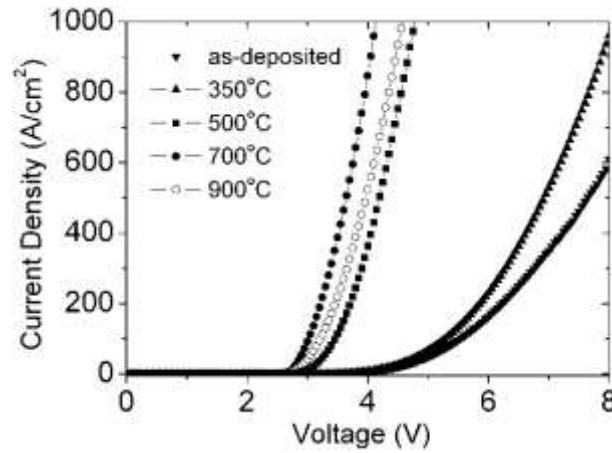


Figure 4.15 Forward  $I$ - $V$  characteristics of 4H-SiC PiN diodes after each RTA at different temperatures. Reprint from[91]

2) The junction formed in the device is probably far from the ideal abrupt form. This follows from the rudimentary device geometry. We can also quote from some results in the literature for ‘non-ideal’ junctions, for example, PiN junctions where the  $p$  and  $n$  zones are separated by an intrinsic insulating zone. Typically this leads to devices where in forward bias the take-off voltage is in the region of a few volts as seen in our devices[91].

## Chapter 5.

### Conclusion and perspectives

In this thesis, we have examined a new possibility of fabricating the most elementary microelectronic device, the bipolar  $p$ - $n$  junction diode. The motivation of this work is not only to introduce a new industrial technique for this circuit element but to explore the technical feasibility of this device with the eventual optoelectronic applications in mind which naturally include light emission from devices made on transparent glass substrates.

To this end, we have demonstrated the following points:

1) We have tested the feasibility of making thin-film devices on glass substrates using either a variant of mechanical exfoliation, which is our anodic bonding method for layered 2D materials, or the standard sol-gel method for the transition metal oxide CdO. We have shown that thin films thus made can be turned into simple devices with contacts transferred by evaporation through stencil masks.

2) We have further shown that these devices can be electrostatically doped using the technique of space charge doping, developed in our laboratory. This technique allows permanent and reversible doping of few nm thick material.

3) If the choice of the material is judiciously made, it can be doped both  $n$  and  $p$  in an ambipolar way. We have shown that this is possible for both the

materials shortlisted in this work, which is InSe and CdO. The first is a layered material (with a thickness of the order of 10 layers) and a direct bandgap semiconductor, while the second is a polycrystalline oxide thin film, which is an indirect bandgap semiconductor.

4) In the last step, we showed for the case of InSe that such a device could be doped in a localized and differentiated way such that one zone is doped with  $n$  polarity and another zone with  $p$  polarity, with a junction separating them.

5) We obtained this functioning for two different geometries with varying success and unilateral conductance for forward biasing as in a normal  $p$ - $n$  junction diode.

6) Finally, the detailed simulation of the working of these junctions was hampered by two possible mechanisms: firstly, by the thermal dissipation in the devices, which caused continuous temperature change during  $I$ - $V$  measurement, and secondly, imperfect and non-abrupt junction formation. Nevertheless, the qualitative simulation shows that these are effectively the reasons behind the measured device performance and give us directions to follow for future work.

Effectively, several points need further work and improvement. Below we discuss these problems and offer some suggestions as perspectives for this work.

1) Both geometries need to be optimized so that the measured characteristics resemble more closely the standard diode characteristics given by the diode equation. The junction needs to be more precisely defined by device shaping, and if possible, contacts placed closer together to limit the spatial extent of the junction region. The more abrupt the junction, the more the diode equation is applicable.

2) There is considerable dissipation in the sample leading to heating and to hysteresis in our diode characteristics. The dissipation could be because of the

low electrical conductivity of the sample and inefficient heat transfer with the insulating glass substrate. Another reason is the very small sample volume which means that there is no inertia and heat generated immediately increases the local temperature. Measurement at lower temperatures and experiments with higher conductivity samples could help to elucidate this problem.

3) Because of a lack of time and adequate apparatus, we could not examine the light emission characteristics of the device. We made measurements with a standard helium flow optical cryostat, which allows the use of a 20X objective with a sample distance of 12 mm. The solid angle collected in this measurement was not enough to detect photoluminescence from few-layer InSe. The solution to this problem is to use a Linkam optical stage where a 50X objective with a working distance of 4-5 mm can be used. This stage is now operational at the lab at the time of writing. This improves the solid angle and signal collection considerably. We also think that the use of a more efficient PL emitter like single-layer MoS<sub>2</sub> will improve this aspect. However, the smaller lateral size of samples of single-layer MoS<sub>2</sub> may be a problem for this option. Obtaining light emission will be a crucial step in eventual applications for such devices.

4) We have shown that CdO devices are, in principle possible. By making ultra-thin films (< 10 nm thickness), the possibility of diode devices with this material can be tested even if light emission is not possible here because of the indirect gap.

5) Clearly, this technique needs to be extended to other materials such as transition metal dichalcogenides. This will be one of the directions that may be followed in the future.



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