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CMOS 180 nm Compact Modeling Including Ageing Laws for Harsh Environment

Thi-Phuong-Yen Tran

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THÈSE PRÉSENTÉE
POUR OBTENIR LE GRADE DE
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ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR
SPÉCIALITÉ ÉLECTRONIQUE

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Soutenu le 03 Juin, 2022

**CMOS 180nm Compact Modeling Including Aging Laws
for Harsh Environment**

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Abstract

In the past decades, the demand for complicated functionality and high-density integration for Integrated Circuits (ICs) has resulted in metal-oxide-silicon (MOS) devices' scaling down. In this scenario, the reliability issues are the considerable concerns due to the device miniaturization, such as Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI) that seriously impact the device performance. In some application fields where the cost of failure is extremely high such as space, oilfield, or healthcare, the device must be able to stably and reliably work, especially at an extensive temperature range. Although device failure mechanisms have been intensively investigated in the past, the investigations of these mechanisms at high temperatures are seldom studied till now.

This thesis aims at developing the aging laws for $0.18\mu\text{m}$ CMOS technology to optimize circuit design for a targeted lifetime under extreme temperatures. We conducted an intensive aging test campaign for both nMOS and pMOS featuring several gate lengths. The intrinsic HCI and BTI mechanisms were characterized and modeled under typical operating voltages to avoid the risk of over-accelerating other wear-out mechanisms that are not supposed to be experienced in practical application. Our experiment is a long-term test during several months. Furthermore, this thesis presents measurement results above 200°C that have never been studied before in the literature for this technology.

The aging laws are finally integrated into an electronic design automation (EDA) environment to predict the evolution of the degraded transistor/circuit electrical parameters and the lifetime estimation due to the aging effects. In addition, the reliability tests at the circuit level have been performed to validate and verify the proposed aging models. This approach offers the possibility to assess and simulate the IC specification drift due to the aging effect in the early design phase and optimize the circuit design over lifetime.

Keywords— CMOS - Reliability - Hot Carriers Injection - Bias Temperature Instability- Circuit reliability simulation

Résumé

Au cours des dernières décennies, la demande de fonctionnalités complexes et de grande densité intégration des Circuits Intégrés (CI) a mené à une réduction de la taille des dispositifs métal-oxyde-silicium (MOS). Dans cette dynamique de développement, les problèmes de fiabilité sont les préoccupations majeures du fait de la miniaturisation du transistor, telles que injection de porteurs chauds (HCI) et instabilités thermiques (BTI) qui ont un impact important sur les performances du transistor. Dans certains domaines d'application où le coût des pannes est extrêmement élevé, comme l'espace, les champs pétrolifères ou les soins de santé, du transistor doit pouvoir fonctionner de manière stable et fiable, en particulier dans une plage de températures étendue. Bien que les mécanismes de défaillance des dispositifs aient été intensivement étudiés dans le passé, les investigations de ces mécanismes à hautes températures sont jusqu'à présent rarement étudiées.

L'objectif de cette thèse est de développer les lois de vieillissement de la technologie CMOS $0.18\mu\text{m}$ afin d'optimiser la conception des circuits pour une durée de vie ciblée sous des températures extrêmes. Nous avons mené une campagne intensive de tests de vieillissement pour nMOS et pMOS avec plusieurs longueurs de grille. Les mécanismes HCI et BTI intrinsèques ont été caractérisés et modélisés sous des tensions de polarisation de fonctionnement typique pour éviter le risque de sur-accélération d'autres mécanismes d'usure qui ne sont pas censés être vécus au cause de l'application. Notre expérimentation est un test à longue durée sur plusieurs mois. Cette thèse présente des résultats de mesure au-delà de 200°C qui n'ont jamais été étudiés auparavant dans la littérature pour cette technologie.

Les lois de vieillissement sont finalement intégrées dans un environnement de conception assistée par ordinateur (EDA) pour prédire l'évolution des paramètres électriques dégradés du transistor/circuit et l'estimation de la durée de vie selon les effets du vieillissement. De plus, les tests de fiabilité au niveau du circuit ont été réalisés pour valider et vérifier les modèles de vieillissement proposés. Cette approche offre la possibilité d'évaluer et de simuler la dérive de spécification du CI du fait du vieillissement dans la phase précoce de conception.

Keywords— CMOS - Hot Carrier Injection (HCI) - Bias Temperature Instability (BTI), simulation de circuit incluant la fiabilité.

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List of Abbreviations

API	Application Program Interface
ASIC	Application-Specific Integrated Circuit
CHC	Channel Hot Carrier
CHE	Channel Hot Electron
CHH	Channel Hot Hole
CMC	Compact Modelling Council
CMOS	Complementary Metal-Oxide-Semiconductor
CP	Charge Pumping
D-C	Defect-Centric
DAHC	Drain Avalanche Hot Carrier
EDA	Electronic Design Automation
EES	Electron-Electron scattering
ELR	Extrapolation in Linear Region
EM	Electromigration
eMSM	Extended Measure-Stress-Measure
ESD	Electrostatic Discharge
FIT	Failures In Time
HCI	Hot Carrier Injection
IC	Integrated Circuit
IGFET	Insulated-Gate Field-Effect-Transistor
II	Impact Ionization
LEM	Lucky Electron Model
MC	Monte Carlo
NBTI	Negative Bias Temperature Instability
OTF	On-the-Fly
PBTI	Positive Bias Temperature Instability
R-D	Reaction-Diffusion
RO	Ring Oscillator
SHE	self-heating effect
SILC	Stress Induced Leakage Current
SIV	Stress-Induced Voiding
SPICE	Simulation Program with Integrated Circuit Em- phasis
TDDDB	Time-Dependent Dielectric Breakdown
URI	Unified Reliability Interface
VLSI	Very Large Scale Integration
VTC	Voltage Transfer Curve

1 | Introduction

Metal-oxide-semiconductor (MOS) structures are essential components of most electronic devices used in daily life. The integration of billions of MOS field-effect transistors (MOSFETs) on microelectronic chips is the heart of electronic devices thanks to computation and control operations. Unfortunately, the speed and lifetime of these devices are limited by inevitably aging mechanisms over time, especially with ultra-scaled devices. This chapter discusses the impact of device scaling, the corresponding degradation phenomena, and the modeling attempts. Then, accordingly, the motivation for this Ph.D. research work is mentioned. Finally, we will summarize how this thesis contributes to a better understanding of the underlying aging mechanisms, reliability modeling, and integration of aging laws into a circuit simulator as well as its verification through ICs aging test results comparison.

1.1 CMOS Scaling and reliability

Transistor continuing scaled-down in size has led to significant improvements in the high-density integration, cost, speed, and power consumption for integrated circuits (ICs). Figure 1.1 depicts the miniaturization trend of the transistor which was formed in the early 1970s. The nano-electronic era began in 2003 when transistor sizes reduced to below 100 nm [1]. The parasitic capacitance and resistance continuously increased in the scaled devices; finally, 3D FinFETs were introduced and were gradually replaced bulk planar MOS transistors, which is a significant milestone in the semiconductor industry, paving the way for sub-22 nm FinFETs development with enhanced performance [2].

The transistor downscaling enables high-density integration and operation at lower supply voltages. The problem is that the power supply voltage of ICs cannot decrease proportionally with the process technology. The rapid reduction of device dimensions leads to increasing the electric field inside, negatively affecting device reliability. The aggressive electric field is the main factor that induces electromigration, dielectric breakdown, bias temperature instability, and hot carrier injection. Since then, transistor aging and reliability are

becoming increasingly difficult for IC designers, significantly when the transistor is scaled down to 10nm and below [3].

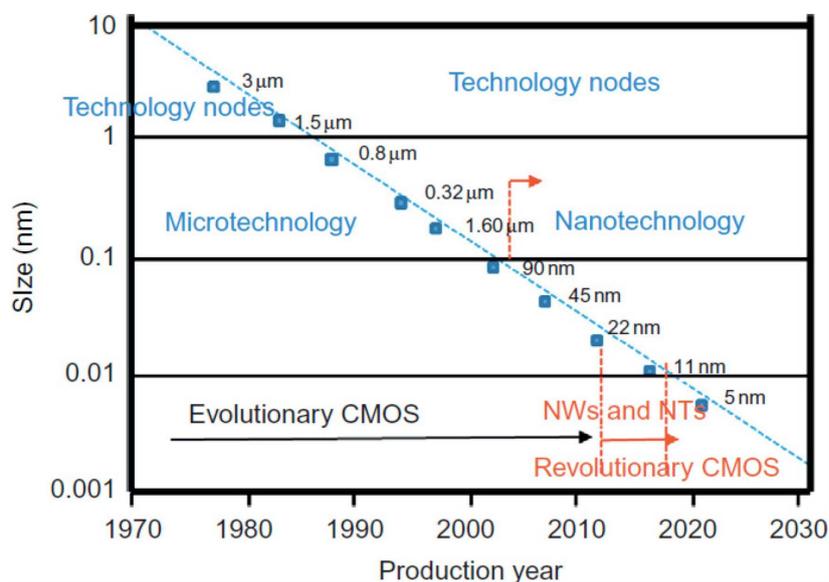


Figure 1.1: Miniaturization trend of the transistor dimension in different technology nodes as a function of time [2].

One of the most important requirements for modern IC designs is reliability. Degradation mechanisms cause changes in electrical device behavior, resulting in shortened circuit lifetime and degraded circuit performance over time. Therefore, transistor degradation has become a limiting factor and a significant challenge in IC designing for reliability-critical applications. In order to achieve reliable products, circuit performance failures due to transistor degradation must be adequately considered early in the circuit design phase. Lengthy and costly testing is required to assess circuit performance degradation over time, which raises the overall manufacturing cost. Therefore, a cost-effective method to estimate the lifetime of circuits due to wear-out mechanisms is critical.

The minimum device lifetime varies dramatically depending on the application. This could be as little as two or three years for a daily life device and as much as ten years or above for oilfield downhole tools, space applications or telecommunications devices [4], [5]. So far, the number of devices that require high reliability has been increasing, particularly in industrial applications where the cost of failure is extremely high. Therefore, understanding the physics mechanisms is essential to investigate unexpected failures and vulnerabilities. Due to the fact that aging mechanisms are complex and difficult to fully predict, many chip

designs today are often over-designed to ensure adequate margin for target lifetime operation [6], [7]. Wafer Level Reliability (WLR) trials are frequently used to estimate product reliability margins utilizing worst-case, Physics-of-Failure (PoF) techniques. These margins result in both speed and power performance penalties, which are becoming more severe in advanced CMOS nodes [8]. However, this traditional approach of over-designing a chip is no longer an wise choice, especially when competitors use effective techniques to reduce the need for overdesign.

There are the several well-known degradation mechanisms in MOSFET, finFET, or FD-SOI devices. They will affect the threshold voltage and drain current, causing the transistor operation to slow down. Some issues related to transistor scaling and reliability such as:

- **Hot carrier injection (HCI)** is a mechanism that occurs in transistors when electrons or a holes gain enough kinetic energy to overcome a potential barrier, becoming "hot" and then injected into a different area of the transistor. HCI represents a degradation in the gate dielectric of the device, forming electron and hole traps, increasing leakage current and causing threshold voltage shifts. Transistor becomes unstable over time and fail [9].
- **Negative bias temperature instability (NBTI)** is due to high electric fields degrading the dielectric with the presence of high temperature, which increases the transistor threshold voltage and reduces transistor switching speeds.
- **Time-dependent Dielectric breakdown (TDDB)** happens when applying high electric fields, causing total breakdown of the gate oxide and resulting in catastrophic transistor failure [10].
- **Electromigration (EM)**, which is one of the reliability concerns and caused by the transport of materials within a conducted wires. Electromigration has become increasingly important since the introduction of 14nm/16nm finFETs [11].
- **Thin wires** are the source of many aging-related problems such as stress-induced voiding [12]. Wires cannot scale proportionally with advanced nodes, causing large resis-

tance/capacitance issues.

- **Quantum effect** is another issue to consider in scaled transistors due to the very thin gate oxide. It is known that quantum mechanics cause uncertainty in the device. Some of the randomness failures cannot be avoided [13].
- **Self-heating effect (SHE)** is becoming much more serious in nano-scale devices [14]. There are fewer concerns about self-heating with a planar CMOS because of the numerous ways to dissipate heat with a planar device, but this is not the case with fin-FETs. The heat is trapped, and it is difficult for it to dissipate. SHE affects both the transistor itself and the metal level beneath.

Aging degradation is highly context-sensitive. Two identical transistors in two different designs will experience completely different age stress patterns and thus degrade differently. The degradation of one transistor will differ from another one in the the same design. Guard banding is a common solution to deal with this problem. However, at advanced nodes, guard banding can have an impact on both power and performance [15].

In order to investigate reliability during the IC design phase, several electronic design automation (EDA) vendors offer aging simulation built into SPICE [16]. The outstanding of the aging simulation is the ability to mimic the long-term behavior of transistors due to wear-out mechanisms. Table 1.1 presents the reliability simulation capabilities requested by Compact Modelling Council (CMC) vs. the various framework strategies [8].

Aging simulation enables designers to forecast how much the circuits will degrade over time. After aging simulation, each transistor will be updated its parameters based on where it is located in the circuit and what electrical stress it is experiencing during operation. Finally, we can see theoretically how its electrical characteristic changes after several years of operation.

Another issue is the methodology to define the reliability models. The accelerated life test including harsh conditions that will allow us to reduce a product life to three months or less so that the system reliability can be investigated and guaranteed accordingly. Traditionally, people perform accelerated aging test by applying the temperatures and biases beyond normal operations. On the one hand, an accelerated life test must be able to accelerate a

Framework strategy Capability	Application Programming Interface (UDRM, MOSRA, RelXpert)	Wrapper style flow (TSMC Modeling Interface) (TMIZ)	External wrapper program (VerilogA module)	Built-in simulator (equation written in simulator language)	End-Of-Life Models (aged SPICE corner)
Separation ageing flow from SPICE flow	Yes	No	Yes	No	No
Integration effort	No external .lib for ageing parameter and C code	Additional integration TMIZ dedicated options are written in .model	Additional scripting for files postprocessing	Additional integration steps	No
Ease at use	Yes	Yes	No additional postprocessing	Yes	Yes
Deployment in industrial flow	Yes	Yes	Limited due to additional postprocessing scripting	Yes	Yes
Equation implementation capability	Complex function capability to implement recovery contribution	Complex function capability to implement recovery contribution	Complex function capability to implement recovery contribution	Limited by CAD-vendor functions	No
Run time	Fast compiled c-code	Fast compiled c-code	Medium compiled c-code + Perl script	Slow interpreted function	Fast
Simulation capability	Very High 1M+ Xtor (SPICE-FastSPICE)	High Up to 100K Xtor (SPICE)	Low (memory limitations due to postprocessing)	High Up to 100K Xtor (SPICE)	Very High 1M+ Xtor (SPICE-FastSPICE)
Confidentiality of ageing equation	Yes compiled c-code	Yes compiled c-code	Yes compiled c-code	No Equations in netlist	No Equations in models

Table 1.1: Compact Modelling Council (CMC) table for reliability simulation frameworks vs required capabilities [8].

specific wear-out mechanism; on the other hand, it is also possible to quantify how much that condition accelerates the wear-out mechanism. There is a link between the accelerated stress conditions and the use condition to quantify the degree or amount of degradation. This quantification is also required to ensure that no extra degradation mechanism activates during the test, which does not exist in the normal use conditions. It is necessary to determine whether the aging behavior is uniform and consistent from accelerating to normal use conditions. The question is whether the data derived from the accelerated aging test can accurately predict the device used under normal operation for a given application. This is a significant consideration for any modeling approach that motivates this thesis work.

1.2 Motivation

Schlumberger is an oil field services company with expertise in designing and manufacturing downhole equipment. This equipment integrates many sensors, and the acquisition is performed by ASICs (Application Specific Integrated Circuit). When downhole tools are operated in oil and gas wells, ASICs are expected to reliably and stably work for several years at extreme pressures and temperatures, often in very corrosive conditions, with little opportunity for visual inspection of equipment. Therefore, the device reliability is essential

since it directly affects the company reputation, the economics of operating wells, the environment, and the safety of the area where the wells are located.

One of the most challenging tasks for mission-critical design is ensuring no failure during the specified lifetime for permanent application; no maintenance is allowed for permanent application in wells in production. Compared to daily-life applications with typical operating lifetimes of around three years, design for automotive applications needs up to 15 years [17]. The market is becoming more and more competitive. It continuously requires rigorous reliability levels for present technologies, with single-digit failure rates in FIT units (Failures In Time units) estimated as 1 FIT = 1 failure per one billion working hours.

At Schlumberger, an ASIC design can be validated and released if only it satisfies the strict qualification criteria. This qualification includes an accelerated life test under severe temperatures to verify whether the ASIC has met or failed its intended quality and reliability requirements. The qualification test duration depends on the tool mission profile. If the IC fails the qualification phase, the whole process must be re-spin which takes several months to years for IC redesign, fabrication, characterization, and qualification phase.

Therefore, it is necessary to develop a practical approach to predict the circuit degraded performance, since a minor shift of ASIC specification due to aging can negatively impact the performance of the tool metrology. As discussed previously, the aging processes are complex and hard to fully predict, many IC designs are often over-designed to ensure sufficient margin to meet the reliability requirements. However, in some technologies, this approach becomes cumbersome and may lead to a limited and ineffective circuit performance. With the trend of scaled-down devices for high-density circuit integration in the near future, reliability can be addressed at design phase and Schlumberger wants to benefit from the latest development in EDA tools to avoid respin in foundry if the ASIC performance is drifting above the acceptance criteria after several years of accelerated life test.

As a result, a dedicated methodology flow for IC reliability evaluation has been established [18], as demonstrated in Figure 1.2. The overall goal of this methodology is to provide accurate design solutions that will avoid many iterations in the design phase, foundry, and qualification, which are time and cost-consuming. It has been proven this unique methodology is technology independent and can be achievable with existing design tools [19], [20],

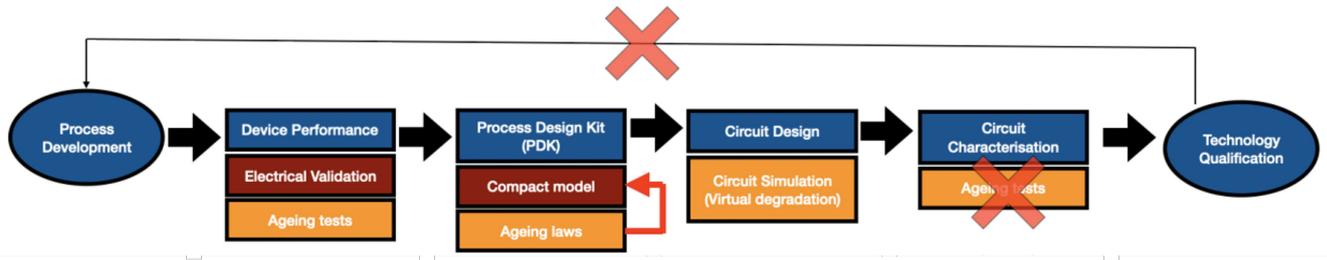


Figure 1.2: Methodology for circuit reliability prediction.

[21]. This approach is based on the following principles: First, the transistors are subjected to dedicated stress conditions, which trigger the degradation mechanisms. The aging tests are performed at the operating voltages and stress duration is up to 2,000 hours to avoid over-accelerating the device. Then, the aging laws are established with the aging parameters extracted from electrical measurements of the transistors before and during the aging test. Finally, aging laws are integrated directly into commercial software, allowing simulate the IC specification drift due to the aging effects, as well as the lifetime of the transistor during the design phase without waiting the circuit characterization.

1.3 Thesis organization

The research objective presented in this thesis was to define the aging laws and associated parameters for $0.18\mu\text{m}$ CMOS technology. Besides, we also considered the reliability assessment for $0.35\mu\text{m}$ CMOS technology to validate our approach further. The main failure mechanisms are HCI and NBTI, which are known as the top-most concerns for scaled CMOS technologies. We proposed the reliability models for a given technology based on the experimental observations. These models are feasible for implementation into the commercial software allowing us to simulate the aging behavior of a circuit at the early phase of IC design.

In Chapter 2, the device failure mechanisms are introduced, focusing on HCI and NBTI. The latest literature results for modeling and reliability are reviewed. Chapter 3 describes the device under test used in this work, the aging test configurations, and the measurement techniques. Chapter 4 presents the initial characterization of MOSFETs at the wafer level to investigate the technology stability and the compact model accuracy before

launching the aging tests. The aging results for HCI and NBTI suffering from extremely high temperatures (up to 210°C) after 2,000 hours of applying stress were reported. The reliability models explaining the experimental observations were proposed. Chapter 5 was devoted to implementation of the reliability models into a circuit simulator. In Chapter 6, the assessment of the aging degradation and simulation on the circuit level is reported. The circuit aging tests were characterized at temperature up to 235°C. Finally, the general conclusions and perspectives of this work are summarized in Chapter 7.

2 | MOSFET failure mechanisms: Description, Physics and Characterization

2.1 Introduction

The lifetime and reliability of an ASIC are considerably influenced by the degradation of transistor electrical characteristics over time. This chapter provides a general explanation of the most important MOSFET degradation mechanisms that have been considered during this PhD research thesis. Even though this chapter does not expect to provide a comprehensive coverage of the vast amount of literature available on the subjects under consideration, it is intended to provide the reader with a sufficient foundation to follow discussions of the experimental works presented in the following chapters.

Most of the chapter is dedicated to NBTI and HCI since these degradation mechanisms pertain to the experimental works given in Chapter 4 and 5.

Several mechanisms are related to CMOS reliability, however they are not covered here such as Latch-up [22], Electrostatic Discharge (ESD) [23], Time-Dependent Dielectric Breakdown (TDDB) [24], [25], Stress-Induced Voiding (SIV) [12], Electromigration (EM) [26]. Latch-up and ESD are not serious reliability issues in IC design industry. The detection of latch-up vulnerability as well as ESD prevention have been intensively researched and established a set of layout design guidelines which designers can follow to mitigate the risk of latch-up and ESD damages [27], [28], [29]. TDDB, SIV and EM degradation are significant for technology node below 100nm [30], therefore, are out of this research scope.

2.2 Bias Temperature Instability (BTI)

Bias Temperature Instability (BTI) is one of the most serious concerns for the reliability of semiconductor technologies, especially for HKMG (High-K Metal Gate) planar, FDSOI and FinFET devices [31], [32], [33], [34]. It is one of the most difficult phenomenon

to predict due to its complex behaviour. BTI causes the degradation observed in MOSFET characteristics by generating interface states at the dielectric interface and creating positively charged defects when the gate is biased in inversion regime at elevated temperatures. The typical stress temperature is commonly in the range of 30 to 250°C.

BTI is observed in both NMOS and PMOS. Negative Bias Temperature Instability (NBTI) is driven by negative gate voltage and mainly effects pMOS, while Positive Bias Temperature Instability (PBTI) is driven by positive gate voltage and affects nMOS. The considerable BTI impact is usually observed in pMOSFETs. In the devices having the length of channel larger than 90nm, the impacts of PBTI on nMOS is almost negligible compared to the effects of NBTI on pMOS [35] [36] as presented in Figure 2.1.

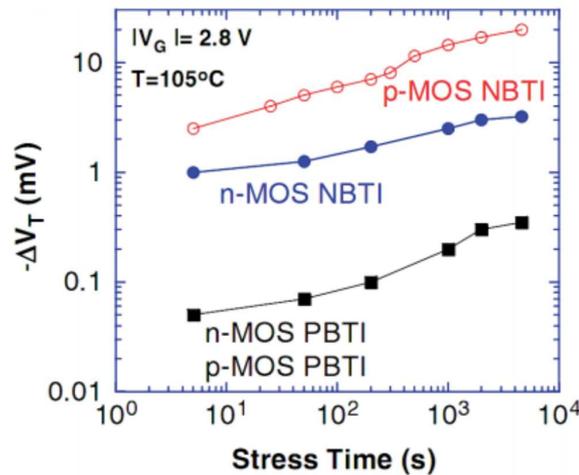


Figure 2.1: NBTI and PBTI comparison in nMOS and pMOS for $L > 90\text{nm}$ [36]

The most distinguishing characteristic of BTI is its recovery when the stress is removed, in which a partial restoration of the degraded characteristics is observed. This recovery dramatically impacts the stress conditions and methodology to characterize BTI. It is frequently considered as the most important factor that need to be monitored for precise BTI understating and modeling, as we will discuss in more detail later in this chapter.

2.2.1 NBTI stress configuration

NBTI configuration must be carefully chosen to ensure that the observed pMOSFET parameter shift accurately represents intrinsic NBTI wear-out and is not contaminated by

testing artifacts or by other mechanisms. Stressing in the cold holes regime (low gate voltage regime where electric field inside the gate oxide is $E_{ox} \approx 5\text{-}7\text{MV/cm}$. Refer to Equation 2.4 for the mathematical description) should be used to describe NBTI [37] because aggressive V_{gs} stress conditions may trigger other undesirable transistor damage mechanisms, such as hot hole injection or time-dependent dielectric breakdown (TDDB), resulting in considerable confusion with NBTI mechanism. Prior to conducting NBTI aging test, it is critical to choose the right NBTI stress bias configuration to accurately activate only NBTI damage encountered during the test. The lifetime prediction of NBTI damage requires accelerated stressing under sufficiently high V_{gs} conditions to observed a desired parametric shift within a short stress period (1000 - 10,000 seconds). This approach provides the necessary understating and modeling to extrapolate the impact of NBTI under normally used conditions. However, this aggressive NBTI stress is analogous to a typical gate TDDB reliability stress configuration. Some bulk defects activated by a sufficiently high V_{gs} conditions may be related to TDDB rather than NBTI [38].

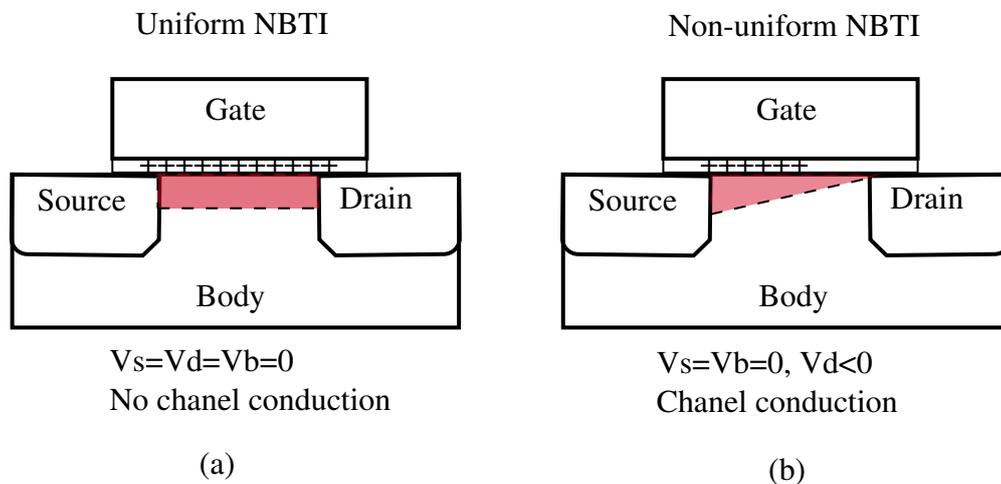


Figure 2.2: Two NBTI stress test configurations

There are two typical NBTI configurations as demonstrated in the Figure 2.2. The transistor is stressed in Figure 2.2(a) using a uniform NBTI with the channel inverted ($V_g < 0$) and the source, drain, and body grounded. Since $V_{ds} = 0V$, no channel current is observed in this scenario and this NBTI stress conditions are considered as symmetric. This is a common set-up to characterize NBTI in pMOSFET where the interface states and charged defects are distributed uniformly. Another NBTI configuration is demonstrated in Figure 2.2(b). In this

nonuniform scenario, NBTI damage is defined underneath the inverted channel area and it is common in analog circuits [39]. Note that NBTI may occur concurrently with other wear-out mechanisms, such as channel hot carrier mechanism, time-dependent dielectric breakdown... Another research had proved that NBTI damage in the nonuniform set-up is the main factor causing pMOSFET device shift under channel hot hole (CHH) condition ($V_{gs} = V_{ds} = V_{dd}$) due to self-heating effect (SHE) at drain junction [40].

Due to the fact that the uniform configuration is usually employed to determine NBTI degradation in pMOSFET devices during a reliability test, it will be the primary focus of this thesis.

2.2.2 Impact of NBTI damage to MOSFET key electrical parameters

MOSFETs are evaluated based on their key figures of merit (FOM) which are a generally accepted performance and efficiency indicator. The FOM of the MOS device are usually defined as:

$$* V_{th} = V_{gs} \text{ at } I_{ds} = W/L \times 100nA, V_{bs} = 0V, V_{ds} = 100mV$$

$$* I_{dlin} = I_{ds} \text{ at } V_{gs} = V_{gsmax}, V_{bs} = 0V, V_{ds} = 100mV$$

$$* I_{dsat} = I_{ds} \text{ at } V_{gs} = V_{gsmax}, V_{bs} = 0V, V_{ds} = V_{dsmax}$$

Since NBTI damage has significant impact on essential pMOSFET characteristics such as threshold voltage (V_{th}), linear (I_{dlin}) and saturation (I_{dsat}) drain current, transconductance (G_m), it has become the primary MOSFET reliability problem in current circuit design.

The direct experimental proof of NBTI damage and its impacts can be found in [41]. According to this research work, a symmetric NBTI configuration ($V_{gs} < 0$) was applied for 2500 seconds and followed by a relaxation phase in accumulation ($V_{gs} > 0$) for the next following 500 seconds. The drift of threshold voltage (V_{th}) and interface states density using charge pumping method were monitored during the test as Figure 2.3. The charge pumping (CP) technique is an effective method for characterizing the traps at the Si/SiO₂ interface in submicrometer MOS devices which was described described in [42].

The relative shift of interface states N_{it} and the rise of V_{th} achieves 1 when NBTI

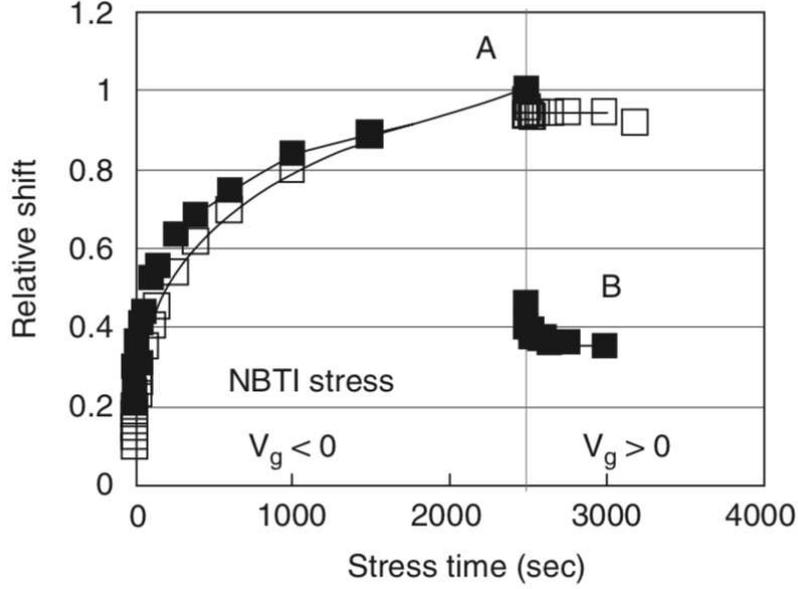


Figure 2.3: Drift of interface states concentration (open squares) and the threshold voltage (filled squares) under NBTI stress condition (phase A) and relaxation (phase B) [41]

stress is removed after 2500 seconds stressing (in phase A). It was observed that N_{it} concentration seems to remain constant throughout the relaxation phase, but the threshold voltage V_{th} shift progressively drops to a saturation value of roughly 0.4 after 500 seconds stressing. Indeed, the similar recovery behaviour obtained by introducing a positive bias after a negative bias stress can be also observed in [43], [44].

The unique relaxing behaviors of the N_{it} and V_{th} imply that the NBTI damage is a dual-stage mechanism. Because N_{it} concentration is found to remain constant throughout the recovery phase, N_{it} generated in a pMOSFET during the NBTI test cannot account for the whole NBTI-induced V_{th} shift. It should be noted that throughout this relaxation phase, the V_{th} recovers to a value that is higher than the fresh V_{th} . According to the findings of this experiment, the NBTI results in damage by two different mechanisms: the formation of interface states N_{it} and the generation of positively charged defects N_{ot}^+ . These oxide defects include two components: the non-relaxable (or a fixed) N_f^+ and the recoverable N_R^+ positively-charged defects. The total positive charged defects can be written as $N_{ot}^+ = N_f^+ + N_R^+$.

NBTI induces transistor characteristic degradation in several ways. The linear drain current I_{dlin} is decreased due to the decrease of flatband voltage (V_{FB}) and effective channel

mobility (μ_{eff}) that occurs during the stress. It is known that the shift in flatband voltage is caused by a rise of total positive charges in the dielectric layer, which leads to a reduction of threshold voltage V_{th} [45]:

$$\Delta V_{FB} = -\frac{Q}{C_{ox}} \times (\Delta N_{it} + \Delta N_f^+ + \Delta N_R^+) \quad (2.1)$$

The change in effective channel mobility μ_{eff} , which is influenced by the amount of N_{it} generated in the channel, is determined as contributing factor to a drop of drain current I_{on} and the increase of drain series resistance R_{ds} . It is possible to write I_{dlin} as follows [46]:

$$I_{dlin} = \frac{C_{ox} + (V_{gs} + V_{th,ext}) \times W \times \mu_{eff} \times V_{ds}}{L + C_{ox} \times (V_{gs} - V_{th,ext} \times W \times R_{ds})} \quad (2.2)$$

where $V_{th,ext}$ is the extrapolated threshold voltage which is directly related to flatband voltage V_{FB} by

$$V_{th,ext} = V_{FB} + 2\phi_B + \frac{\sqrt{4\epsilon q N \phi_B}}{C_{ox}} \quad (2.3)$$

where ϕ_B is Fermi potential, q is the electric charge measured in coulombs, and ϵ is relative permittivity of silicon. According to Equation 5.2, it is clear that the shift of threshold voltage relates to the change of flatband voltage: $\Delta V_{th,ext} = \Delta V_{FB}$.

Furthermore, NBTI damage also impacts the subthreshold regime characteristics by increasing the subthreshold swing (SS) and results in a decrease of the saturated drain current I_{dsat} [47].

2.2.3 NBTI physical mechanisms

In this section, we concentrate on the transistor damage under NBTI uniform stress configuration in cold hole regime and in inverted channel. Despite the intensive researches on NBTI degradation for more than 50 years with the huge quantity of experimental data, the basic physical mechanisms of NBTI remains controversial [48]. Some primary physical mechanisms contributing to NBTI damage have been proposed and graphically explained in Figure 2.4.

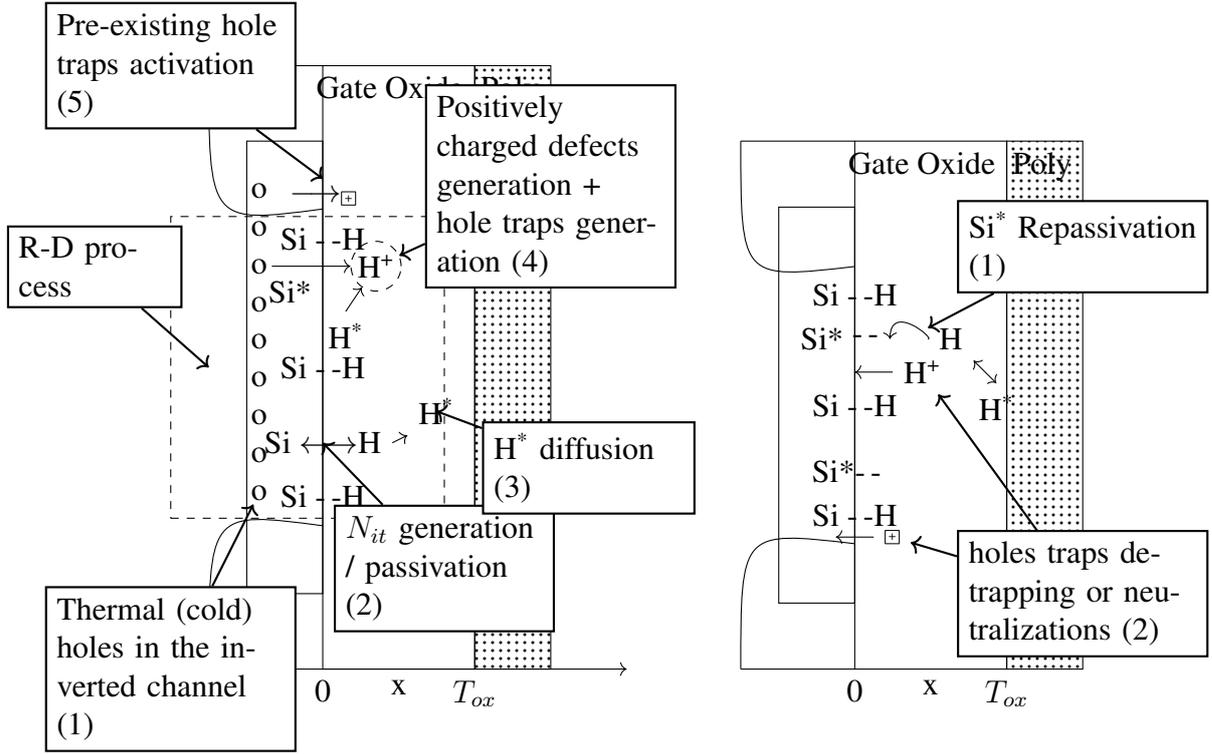


Figure 2.4: Main physical mechanisms contributing to NBTI damage (left) and physical mechanisms related to NBTI recovery (N_{it} repassivation and hole traps neutralization) [49]

After oxidation, majority of the Si atoms are connected to the oxygen and few Si atoms bind to hydrogen along the Si/SiO_2 interface as shown in Figure 2.4 (left). On the one hand, the N_{it} formation (Si^*) mostly is a consequence of the breaking of Si–H bonds at the dielectric interface assisted by the presence of thermal holes (1) through a reaction-diffusion process [50] [51], combining with an electrochemical reaction of N_{it} generation and passivation (2). Besides, a hydrogen (H^*) species can diffuse in the gate oxide and eventually enter to the poly-gate (3).

On the other hand, positively charged bulk defects are generated through different mechanisms under NBTI stress: i) Positive charged defect generation due to electrochemical reaction between holes and defects at the Si/SiO_2 interface (4) [52] or ii) Activation of preexisting hole traps (5) and trapping the holes by near-interface states by thermally-assisted tunneling [53], [54]. iii) Bulk trap formation by trapping of the diffusing species H^* .

The observed NBTI recovery at $V_g \geq 0$ V can be explained by two main physi-

cal processes demonstrated in Figure 2.4 (right). The process of N_{it} reduction through Si^* repassivation by the availability of H^* at the Si/SiO_2 interface (1) when the stress is removed. H^* species may travel in the gate oxide and repassivate with dangling bonds Si^* – [55]. Also, evidence of NBTI recovery due to a Nit repassivation has been discovered by employing a DC current-voltage method [56], [56]. Additionally, due to the change of electric field direction in the recovery phase, the hole inside the defects can be detrapped and the defects become neutralized by electrons injected from the gate (2) [57]. NBTI recovery has been receiving a lot of attention, however, no general agreement has been built regarding the relative contribution of N_{it} repassivation (supported by R-D process) and bulk trap neutralization [48].

The dependence of NBTI recovery rate on the temperature can be found in [58] which stated that high temperature can slow down recovery. Their experimental observation at $125^\circ C$ suggest that high temperature accelerates permanent oxide trap creation causing the reduction of recovery rate. According to their explanation, at elevated temperatures, the NBTI recovery is lower because H species are no longer available for repassivation due to the loss of H through diffusion into the poly gate or due to the generation of stable Hydrogen species that do not participate to the recovery process.

2.2.4 NBTI dependence on stress condition and experimental observation

BTIs are experienced by both pMOSFETs and nMOSFETs. However, PBTI degradation on nMOSFETs can be negligible while NBTI configuration in pMOS is the worst BTI case [43]. For this reason we will take more attention in this section to the pMOSFET NBTI degradation.

2.2.4.1 Dependence on the gate voltage

Although the presence of holes in inverted channel is required for NBTI degradation, neither threshold voltage shift nor the interface state generation rate are observed to be dependent on the hole channel concentration [59]. However, the NBTI degradation presents

a strong relationship with the oxide electric field applied during the stress as illustrated in Figure 2.5.

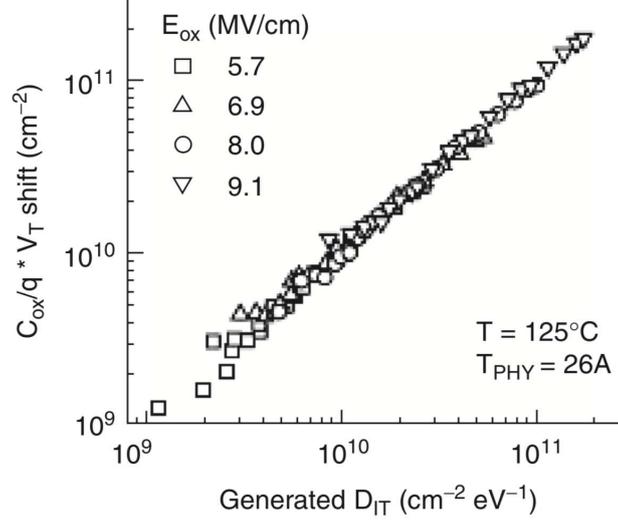


Figure 2.5: Dependency of V_{th} shift and N_{it} activation of several pMOSFETs in inverted channel at several gate oxide filed [60]

The degree of the NBTI-induced ΔV_{th} is consistently observed to depend on the applied gate stress voltage. It means that the larger degradation must occur at higher negative voltages as in Figure 2.6 [61]. More specifically, [62] also investigated NBTI degradation on different oxide thickness of several MOS devices demonstrating that NBTI degradation is dependent on the electric field generated in the oxide layer (E_{ox}), not on the absolute value of the gate voltage. When researching NBTI on a given oxide thickness, the NBTI degradation is observed to be related to the gate overdrive voltage $V_{ov} = |V_G - V_{th0}|$, this value directly corresponds to the oxide electric field $E_{ox} = V_{ov}/t_{ox}$ [35].

Several evidences of NBTI dependence on oxide electric field can be found in [63], [64]. From wide variety of experimental data, they have provided some NBTI models, for example, exponential model: $\Delta V_{th} \approx \exp(\gamma E_{ox})$ and power-law model: $\Delta V_{th} \approx (E_{ox})^n$ where E_{ox} is given by

$$E_{ox} = \frac{V_{gs} - V_{FB} - 2\phi_B}{T_{ox}} \quad (2.4)$$

2.2.4.2 Dependence on the temperature

As stated by [65], the degradation of NBTI is a temperature-dependent process. The

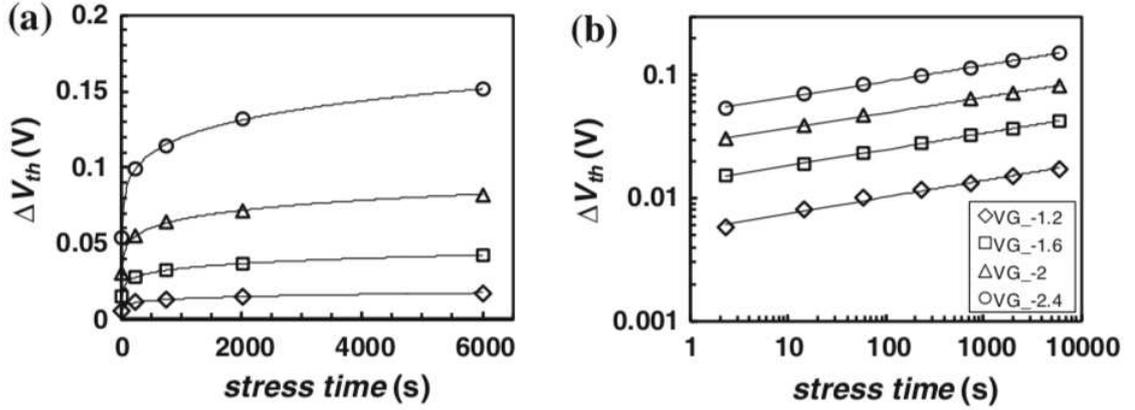


Figure 2.6: NBTI-induced ΔV_{th} for different gate voltage in lin–lin scale (a) and in log–log scale (b). Experimental data collected on pMOSFETs, $t_{ox} = 1.6nm$, $T = 125^\circ C$ [61]

experimental observations indicate that NBTI has an Arrhenius-like relationship on stress temperature, such that $\Delta D \approx \exp(-E_a/k_B T)$ where D is a degraded device parameter. E_a , k_B , and T are activation energy, Boltzmann constant, and temperature (in Kelvin), respectively. In this scenario, ΔV_{th} and ΔN_{it} have experimentally determined different values of activation energy, that are $E_a(V_{th}) = 0.063eV$ and $E_a(N_{it}) = 0.156eV$, giving the further evidence of the presence of both interface states (N_{it}) and charged defect. To clarify this point, if the threshold voltage shift was controlled only by ΔN_{it} , the activation energies of ΔV_{th} and ΔN_{it} should be identical (refer to Section 2.2.3 for details).

A detailed analysis of the stress and recovery NBTI kinetics for large range of temperature ($-40^\circ C$ to $300^\circ C$) suggested that ΔV_{th} during the stress test follows Arrhenius law with an activation energy around $0.12eV$, however, ΔV_{th} in relaxation phase could not be modeled by simple Arrhenius law [66]. Other researches investigated thermal effect ($T = -40^\circ C$ to $+165^\circ C$) to establish NBTI models, such as an Activated Barrier Double Well Thermionic model [67], Transient Trap Occupancy model [68]. Another NBTI investigation presented the emission and capture time constants of individual defects are thermally activated via Arrhenius law [69].

2.2.4.3 Time evolution

To comprehend the physics of NBTI degradation, it is necessary to understand not only

the gate oxide field and temperature dependency of the interface trap generation, but also their time dynamics. It is also a crucial condition for developing an appropriate extrapolation model for device lifetime. A distinguishing feature of the interface traps generation during NBTI stress is their fractional power law time dependence. As seen in Figure 3.10, the fractional time dependency of NBTI degradation decreases with increasing stress duration, presenting a saturation tendency [35].

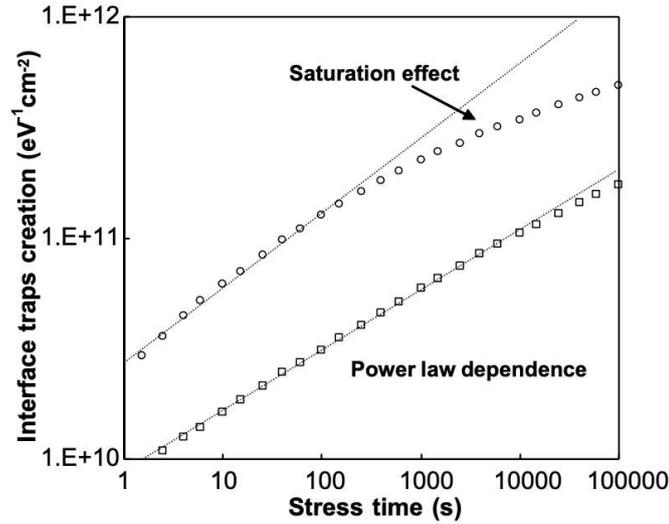


Figure 2.7: The generation of interface traps as a function of stress time at two different temperatures and a constant gate voltage, demonstrating power law dependency and saturation effects at longer stress duration [35]

It is well-known that saturation of defect generation inside the gate oxide impacts the time slope [70], [71]. With increased stress time, ΔV_{th} seems to saturate as illustrated in Figure 2.8. To quantify the observed saturation effect, the stress time was divided into several time regions to derive a power-law ($\Delta V_{th} = C \times t^m$) and calculate time exponent (m) for each area. Additionally, it is critical to note that the observed saturation effect is larger at lower stress voltages. At early stress times, the power-law time exponent m at $|V_g| = 4V$ is indeed greater than all the rest. The rise of the time exponent m as $|V_g|$ values decrease is related to the reduction in the V_{th} shift during the first stress periods [71].

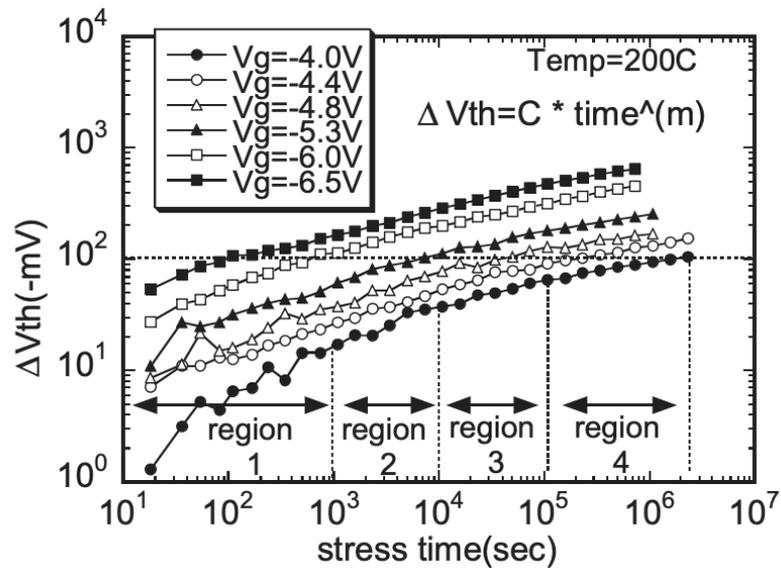


Figure 2.8: ΔV_{th} vs. stress time for several gate voltage at 200°C [71].

2.2.5 NBTI characterization

NBTI recovery is significantly related to the NBTI stressing and testing methodologies. One drawback that may lead to the inaccurate NBTI measurement results is the recovery phenomena which is induced by the hole detrapping/ neutralization of positive bulk traps by electron injection and subsequent interface states N_{it} repassivation. NBTI degradation was monitored in terms of the shift in threshold voltage (ΔV_{th}) which is a parameter directly tracking the damage at the interface [72].

2.2.5.1 Classical technique

It is the common approach with many interruptions: measure-stress-measure. In this approach, the given V_{gs} was applied to the device using uniform NBTI configuration ($V_{ds} = 0, V_{bs} = 0, V_{gs} < 0$). After a given time, the stress was interrupted to measure the shift of transistor parameters (V_{th}, I_d , ect.) due to NBTI damage. However, this method does not consider the delay time between the stress and the measurement in which the NBTI recovery occurs. To minimize the impact of the NBTI recovery during the periodical measurements, it is crucial to minimize the off-stress time between the ending of the stress and the beginning of the measurement. A long off-stress time may lead to inaccurate estimation of NBTI degradation. Since 2003, it was widely recognized that none of the classical methods can

characterize NBTI accurately [73].

2.2.5.2 On-the-fly technique

To limit the impact of NBTI recovery, on-the-fly (OTF) technique was introduced for the first time by [35], and this method keeps constantly growing and consolidating over time. Several variations of the OTF procedure has being proposed [74], [73], [72], [75], [76]. In this method, a very small value of V_{ds} (V_{ds} between $-25mV$ and $-100mV$) is applied that not to disturb the gate oxide field at a given V_{gs} , thus the same degradation behavior activated by NBTI is obtained respect to conventional method. The linear drain current I_{dlin} is measured without interrupt the V_{gs} , thus there is no delays. This method is based on the fact that, there is an experimental linear relation between ΔI_{dlin} and ΔV_{th} at given $V_{gs,measure}$ as monitored by conventional method:

$$\frac{\Delta I_{dlin}}{I_{dlin}}(t) = M_{exp} \times \Delta V_{th}$$

where M_{exp} is the experimentally extracted slope. The extraction M_{exp} defines the correspondence between ΔV_{th} and $\% \Delta I_{dlin}$ at the $V_{gs,measure}$. This equation is valid as long as the device is operating under strong inversion condition ($V_{gs} \geq V_{th}$). If the device is operating in subthreshold regime or weak inversion regime ($V_{gs} \ll V_{th}$), the relation between ΔI_{dlin} and ΔV_{th} is not linear anymore.

2.2.5.3 Fast switching methodology

The idea of this method is from the necessary to estimate the NBTI degradation under very short and controlled time delay, thus minimizing the impact of NBTI recovery. The measurement time is expected to be lower than $10\mu s$ to avoid any recovery, which is unsuitable in industrial environment because minimum response time of their equipment was around 2-3ms [76]

The basis idea of the fast switching method is monitoring the NBTI degradation at use conditions by means of a very short and controlled time delay to minimize the effect

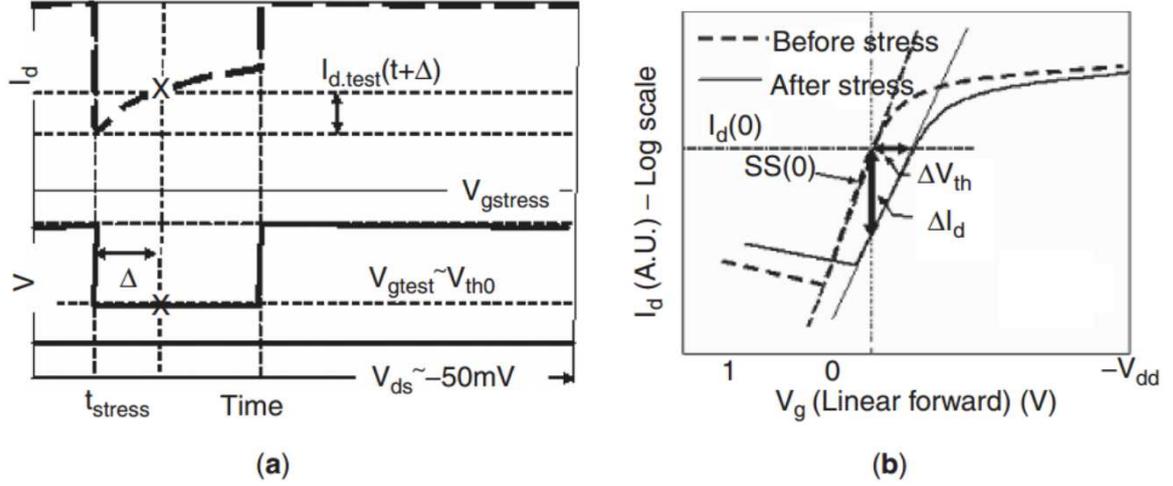


Figure 2.9: The basis idea of fast switching method [77]

of recovery during the measurement. This procedure is described in Figure 2.9(a). After a given stress time t_{stress} , $V_{gs, stress}$ is reduced to a constant value $V_{gs, test} \approx V_{th0}$ to measure the $I_{d, test}$. This value of $I_{d, test}$ is measured with very short time delay ($\Delta \approx 1\mu s$) after stress. According to the initial $I_{ds} - V_{gs}$ curve, an approximation of the threshold voltage shift can be obtained by horizontal shifting the stressed $I_{ds} - V_{gs}$ curve as shown in Figure 2.9(b).

2.2.6 NBTI models

There is no agreement on the underlying physical mechanism of NBTI, although there are hundreds of published researches over the previous half century. There is still a controversy about whether NBTI is diffusion-limited or reaction-limited [78], [79]. This disagreement leads to two main competing models in the community: Reaction-Diffusion model and Defect-Centric model.

2.2.6.1 Reaction-Diffusion model

The concept of a Reaction-Diffusion (R-D) model rapidly became the default explanation since its ability to successfully explain a large variety of experimental observed data [80]. With the recent recognition of the transient relaxation, the Reaction-Diffusion model was modified to agree with the experiments. However, the validity of the underlying physics

is still a question [81].

The R-D model have been established based on interface state generation along the dielectric interface:



where N_{it} , N_{ot} are interface states and oxide positive traps, respectively. X is a mobile species that can diffuse inside the gate oxide [82]. Despite of this equation indicating the equal roles of interface states N_{it} and positively charged defects N_{ot} , no correlation between these two components has been provided. R-D model is built based on the description of silicon dangling bond depassivation by eliminating Hydrogen. The N_{it} generation is described as $SiH \rightarrow Si^* + H$. The interface states N_{it} recovery can be defined using double-interface model [83]:



In the past, R-D model was introduced to explain the power-law time dependent with exponent 1/4 observed from experiment [50]. However, considering the relaxation phenomenon, the 1/6 time exponent for interface state generation was published more recently [80], [84], [78]. Although measured $t^{1/6}$ dependency is consistent with R-D theory for interface state generation, the defect distribution in the gate oxide is not given proper attention. It turns out N_{it} dominates the NBTI degradation while other contributors such as positively-charged defects are assumed negligible. The data analysis shows agreement with R-D model, but it could not convince proponents of Defect-Centric model [85].

2.2.6.2 Defect-Centric model

As discussed in section 2.2.3, the NBTI recovery became the interesting subject in early 2000s. The threshold voltage was observed reversible in the relaxation phase. The N_{it} had minor recovery while N_{ot} gave the dominant reversion leading to the idea that N_{ot} have the significant influence on ΔV_{th} . Additionally, measurements on ultra-scaled MOSFETs

providing individual de-trapping observation [86], further support the Defect-Centric (D-C) model which related to trap transformation assisting by reaction-limited processes [87].

In contrast with RD model which treats interface state generation and passivation as primary NBTI factor, D-C model considers them as simply another class of defect supported by the first-order reaction. This defect model attempts to capture the accurate physics of trapping defect in gate oxide, which is a complicated process.

D-C model has a solid basic in underlying physics, assisted by microscopic measurement of discrete defect, nonetheless, its ability to fully describe the broad data under several NBTI stress and conditions is still limited [78]. D-C model describes the microscopic behavior of discrete traps in relaxation phase by using Time-Dependent Defect Spectroscopy (TDDS) [88], it has not been proved its ability to model threshold voltage shift (ΔV_{th}) during NBTI stress (bias, temperature, duty cycle...) on various device types (HKMG, SiON, SiGe channel...). There are some researches support D-C model such as [89], [90], [91]. However, they are inadequate compared to R-D model which is able to explain NBTI degradation (both stress and recovery phase) over a broad range of stress conditions, as well as deals with a variety of device types. This is the strongest argument of R-D model against other competing models. [82], [78], [84], [32].

2.2.7 Concluding remarks

A general description of NBTI degradation considered in this work has been given in this chapter, and it will serve as a underlying physics for the discussion of the experimental results presented hereafter. We have discussed in detail the mechanism stress configuration as well as stress condition which are required to propose an intensive aging test campaign. We also reviewed the Reaction–Diffusion (R-D) model and Defect-Centric modes that pose significant doubts about the correctness of each approach.

2.3 Hot Carrier Injection

Hot carrier degradation was first reported in the early 1970s and since then the term has

become more and more popular in the reliability community. Carriers (electrons or holes) are channel carriers that gain significant kinetic energy by passing through high electric field regions. Under the HCI bias conditions, the lateral electric field is responsible for carrier heating, while vertical electric field supports the injection of hot carriers into the gate oxide through impact ionization, thereby causing the damage at the Si/SiO_2 interface. Hot carrier degradation is a major reliability concern, particularly as the dimensions of MOSFET transistors continue to shrink.

Hot carriers induce degradation on channel parameters such as decrease of the channel mobility and flat band voltage (V_{FB}), which in turn affect key characteristics such as linear and saturation drain current, threshold voltage, maximum transconductance, subthreshold slope, drain series resistance and the drain junction leakage.

2.3.1 Physical generation and injection mechanisms

Most of the researches have been focused on the channel hot carriers (CHC) generated in the channel region in inversion under saturation bias conditions ($V_{gs} > V_{th}$, $V_{ds} > V_{dsat}$). Channel carriers can gain enough energy to become energised when travelling along the channel. The drain collects most of these CHC, however, there is a small fraction being scattered toward the gate and injected into the oxide layer to form the bulk trap and gate additional leakage current. Additionally, they can also generate interface states by continue hitting the $Si - H$ bonds at the Si/SiO_2 interface and break them. Hot carrier degradation is considered one of the most critical reliability concerns in nMOSFETs.

Two factors that are responsible for HC generation: (1) The channel electric field in pinch-off region and/or (2) scattering events (impurity, electron-phonon scattering, electron-electron scattering, ect.) and secondary impact ionization (II).

2.3.1.1 Electric field in pinch-off region

Electric field is the main driving force causing the carrier heating and supports hot carrier injection into the gate oxide. Under the bias condition in the saturation, the lateral electric field in the pinch-off region provide the energy for channel carriers to become hot, while the vertical gate oxide field above the pinch-off region supports the injection of ener-

getic electrons/holes into the oxide layer by modifying the barrier height (ϕ_B) at the Si/SiO_2 interface.

As shown in Figure 2.10, when a positive gate-source voltage in nMOS is applied ($V_g > V_{th}$), the channel will be generated and the carriers (electron or holes) can travel along the channel between the drain and source. As the drain voltage increases, we reach a point where $V_{ds} = V_{gs} - V_{th}$ that is pinch-off region, at which the current becomes saturated.

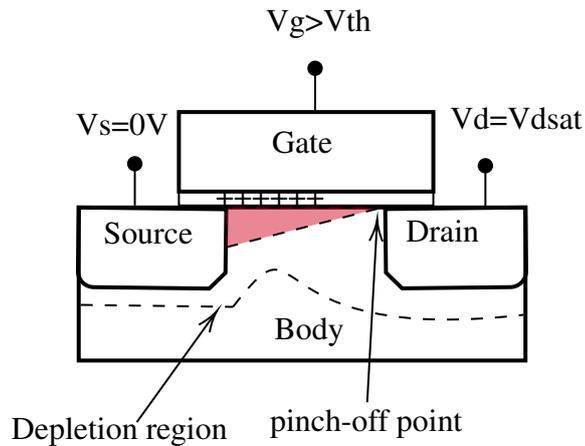


Figure 2.10: Pinch-off region

One of the main peculiarities of HCI is its strong localization [92] [93] [94]. Under the electric field, channel carriers accelerate from the source to drain and gain substantially high energy in the drain vicinity. Such hot carriers can cause the damage near the drain region by generating interface states (ΔN_{it}) and/or oxide-trapped charges (ΔN_{ox}) at Si/SiO_2 interface. As shown in Figure 2.11, the electric field, the carrier energy, and the interface state density get their maximal value near the drain spacer. It is well accepted that the electric field is responsible for the carrier heating and for the interface state generation as well. This consideration leads to the most popular HCI models namely Lucky Electron Model (LEM) proposed by [95].

It is worth to mention that for hot carriers generated by lateral field in the channel, the degradation is localized at the drain side where the pinch-off region is located [96]. Such localized degradation induces an asymmetric shift in the nMOSFET characteristics depending on the direction of the current flow in the channel, as shown in Figure 2.12.

In general, to be injected into the oxide layer, a hot carrier must have sufficiently large

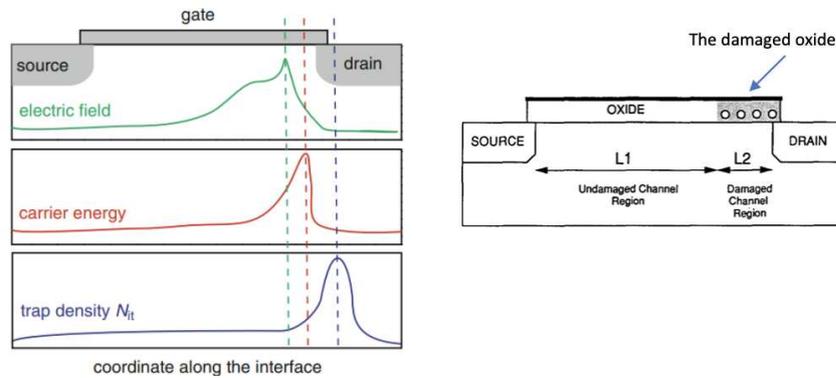


Figure 2.11: Schematic of lateral profiles under HCI condition of different quantities in a MOSFET (left) [92] and an illustration of a damaged MOS device due to HCI (right) [94].

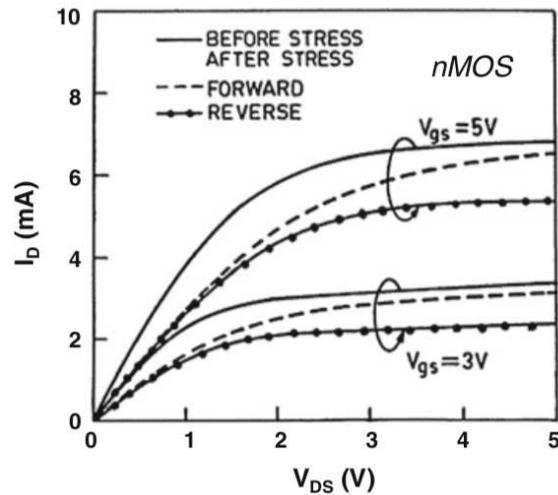


Figure 2.12: $I_{ds} - V_{ds}$ curves of a nMOSFET device before and after a HC stress. In the saturation regime ($V_{ds} > V_{gs}$), the shift of the characteristic depends on the direction of the current flow in the channel [96]

energy to surpass the barrier height (ϕ_B) at the Si/SiO_2 interface. That is $E_{electron} \geq 3.2eV$ for hot electron and $E_{hole} \geq 4.8eV$ for hot hole to surmount the barrier. However, this point is not adequate to explain the HC degradation in submicron MOS device in which the power supply is much smaller than 3.2V. Therefore, there are further mechanisms that are responsible for creating hot carrier at low V_{dd} , i.e., electron-phonon (e-p) scattering, electron-electron (e-e) scattering and secondary impact ionization (II2). The first two mechanisms are presented in the next two sections and the secondary impact ionization will be mentioned after that.

2.3.1.2 Electron-phonon scattering

Some channel electron with energy around qV_{ds} may lose their energy by emitting an optical phonon. There is the possibility that this optical phonon is absorbed by another electron, and in this way, the electron can accumulate the energy gradually to get the energy beyond qV_{ds} . The highest optical phonon energy is found around 63meV in silicon [97].

2.3.1.3 Electron-Electron scattering

Electron-Electron scattering (EES) is the energy exchange between electrons as a result of Coulomb interaction. For example, two electrons travel in the channel and enter the drain region with an energy qV_{ds} . There is a possibility that one of the electrons may transfer almost its kinetic energy to the other through EES event. Accordingly, the maximum energy of one electron after scattering is proximately $2 \times qV_{ds}$ and by this way, after some multiples EES events, an electron can gain enough energy to become a hot electron. The probability of EES events depends on the concentration of the carrier $n(E)$ in the pinch-off region where EES is active. Therefore, I_d is maximized at $V_{gs} = V_{ds}$ conditions, this also corresponds to the condition of the worst case CHC degradation in advanced submicron nMOSFET. The dependence of EES on carrier concentration is one of the reasons causing worst case CHC damage in nMOSFET as V_{gs} increases. The heavier electron concentration at high V_{gs} , the higher EES rate. Additionally, electron population is closer to the Si/SiO_2 interface creating higher possibility of injection into the dielectric layer [98]. EES is considered as a main role in carrier heating in submicron MOSFET operating in saturation regime where $qV_{dd} < E_G$.

2.3.1.4 Impact ionization (II)

When the sufficiently electrical force is applied to the device, the channel carriers can gain the kinetic energy larger than silicon bandgap ($E_G = 1.12eV$ at room temperature), it can break the Si valence bond by collision to generate the electron-hole pairs. This phenomenon is known as impact ionization (II) and can also be considered as a carrier-carrier scattering process. Each of generated carriers (electrons/holes) may also be energized by the electric field and generate additional electron-hole pairs, known as avalanche multiplication. This effect is mainly responsible for the avalanche breakdown of semiconductor junction [99]. Furthermore, II also affects the reliability of device in terms of excess the substrate leakage current. The substrate current I_{sub} is the direct measurement of the generated holes (in nMOS) or of the generated electrons (in pMOS) by II. Primary impact ionization (1II) is the II process that activated by the primary carriers. High lateral electric fields in pinch-off region is responsible for 1II. In other words, this process is controlled by the $V_{ds} - V_{dsat}$ difference. In nMOS device, the generated electrons may gain further kinetic energy to creating additional e-h pairs while the generated holes in this case are assumed not to contribute into creating further e-h pairs (if not, this case is considered as the secondary impact ionization). Hot carriers created by 1II are the source of the drain avalanche hot carrier injection. Under the saturation condition, the direct measurement of 1II rate is given by $R = I_{sub}/I_d$. Secondary impact ionization (2II) is activated by the byproduct of 1II. 2II takes place only if 1II occurs in pinch-off region. High vertical electric fields in the drain/substrate depleted junction are responsible for 2II. The 1II creates e-h pairs, in turn, becomes the source of 2II. In other words, the electrons are generated from the 1II will contribute to the drain current whereas the holes are diffuse forward to drain/substrate depleted region and then heated by vertical fields. These holes, again, may gain enough energy to generate further e-h pairs by collision with Si atoms. Holes created by 2II process contribute to substrate current and electrons flow back along the vertical electric field to contribute to drain current, or to inject into gate oxide. 2II phenomenon is considered as one of the sources of HCD at bias conditions where lateral electric field is not high enough to produce hot carriers [100].

2.3.1.5 Localized self-heating effects

The carriers in the channel before pinch-off point have low energies and they are assumed to be in thermal equilibrium with lattice due to the balance of emission and absorption of acoustic phonons. Acoustic phonons are primarily responsible for heat transfer in Silicon when it is in thermal equilibrium, since they take advantage of efficiently carrying heat. Therefore, there is quite small self-heating in the device before the pinch-off region. When electrons enter the pinch-off region, they gain large kinetic energy to become hot. Due to the high energy, these hot electrons can emit and absorb both acoustic phonons and optical phonons, however, they tend to interact with optical phonon much more strongly than acoustic phonon. The optical phonon is heavier and slower compared to acoustic phonon in term of carrying away the energy of carriers, therefore, causing the local self-heating at the region of their creation until it decays into acoustic phonons that transfer the heat away. The local self-heating phenomenon may lead to the increase T_{eff} at the region near the drain region. In pMOS, the temperature rising will aggravate the NBTI damage rate. Otherwise, the increased effective temperature can promote the impact ionization rate, exacerbating hot carrier damages even at low drain biases. The onset of self-heating will be much slower than hot carrier degradation because it requires a certain of time as in Figure 2.13 [101].

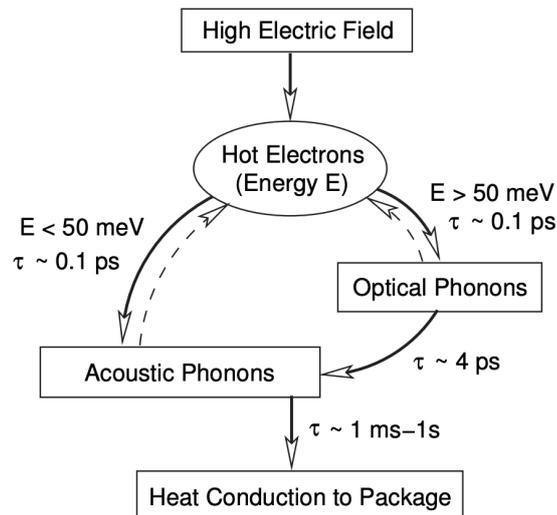


Figure 2.13: Diagram and characteristic time scales of the energy transfer processes in silicon [101].

2.3.2 HCI characterization

Channel hot carriers are generated in MOSFET inverted channel ($V_{gs} > V_{th}$) and directly related to the set-up of the saturation condition ($V_{ds} > V_{dsat}$). Under the bias condition in saturation, two regions are identified in the channel: the inverted channel region and the pinch-off region (where majority of HC is generated). In the linear regime ($V_{gs} > V_{th}, V_{ds} \geq V_{dsat}$), a continuous channel is formed entire channel and the channel field F is smaller than F_c , the critical field for velocity saturation. Therefore, in this linear region, velocity of the carrier is lower than velocity saturation v_{sat} . As the V_{ds} rises above V_{dsat} , we reach a point known as pinch-off at which carriers experience velocity saturation ($v = v_{sat}$) at the voltage V_{dsat} leading the saturated and constant current flow. Due to the high lateral electric field, carriers in pinch-off region are moving with saturated velocity and become energised.

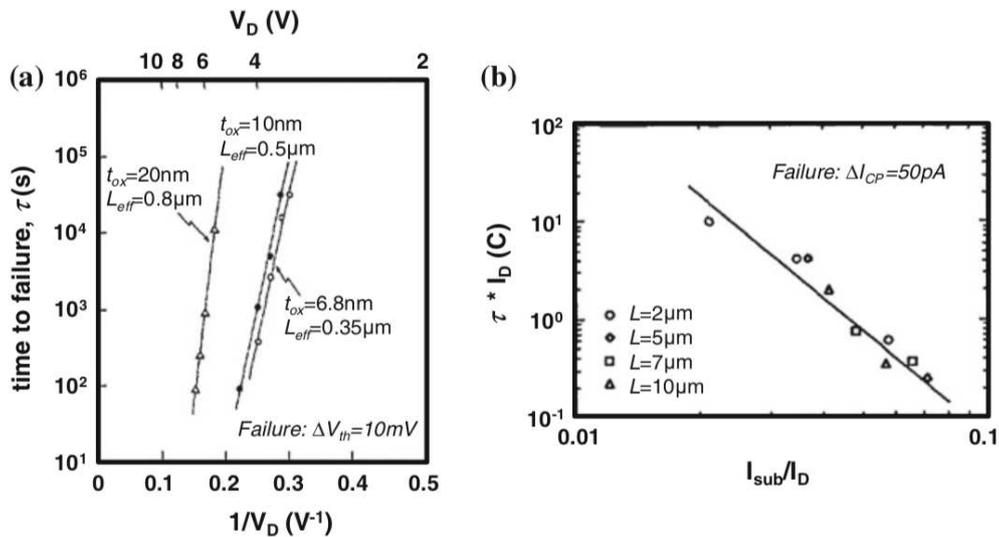


Figure 2.14: (a) HCI lifetime follows an exponential dependency on $1/V_D$ [102]. (b) The cumulative charge present in the channel before the device failure follows a power-law of the multiplication factor [103].

To appropriately understand the degradation of the I–V characteristic due to nonuniform carrier injection, it is necessary to examine the nonuniform spatial distribution of the interface state density and trapped-oxide charge. Due to the difficulty in interpreting the

degradation in the drain current characteristics, other characterization approaches such as modified lateral-profiling charge pumping are often applied [93].

To determine the device lifetime under Hot Carrier Injection, several device parameter shifts have been used as alternative failure criteria such as a drain current in the linear regime I_{dlin} , saturation current I_{dsat} , threshold voltage V_{th} , a transconductance G_m , or charge pumping current I_{cp} . Additionally, several acceleration models have been established to predict HCI degradation at operational application from the accelerated testing. [102] and [103] (Figure 2.14) suggested two of the most often utilized acceleration models as in Equation 2.8 and Equation 2.9, respectively.

$$t \propto \exp\left(\frac{1}{V_{ds}}\right) \quad (2.8)$$

$$t \times I_d \propto \left(\frac{I_{sub}}{I_s}\right)^{-m} \quad (2.9)$$

2.3.3 Summary

The summary of the HCI mechanism in nMOS is illustrated in Figure 2.15. HCI becomes serious at advanced nodes where the gate length is reduced below 100nm. In Figure 2.15, the carriers in the channel are accelerated by a high lateral electric field and suffer from scattering events (e-e, e-p). During traveling in the channel, they gain energy to become "hot", causing Impact Ionization and local-self heating in the pinch-off region. The carriers with enough high energy (3.7eV for electrons and 4.8eV for holes) can inject into the gate oxide under the support of the gate electric field. The increase of leakage current and charged defects may lead to transistor electrical characteristic shifts. This section has discussed the channel hot carrier (CHC) effects that occur in the inverted channel of MOSFETs, similar to applications in integrated circuits. Typically, two CHC bias stress scenarios are explored for validating CMOS technologies: conducting and nonconducting. The characteristics of these two CHC bias configurations, the methodology used to determine the CHC sensitivity of specific CMOS technology, and their effect on device shift have been mentioned.

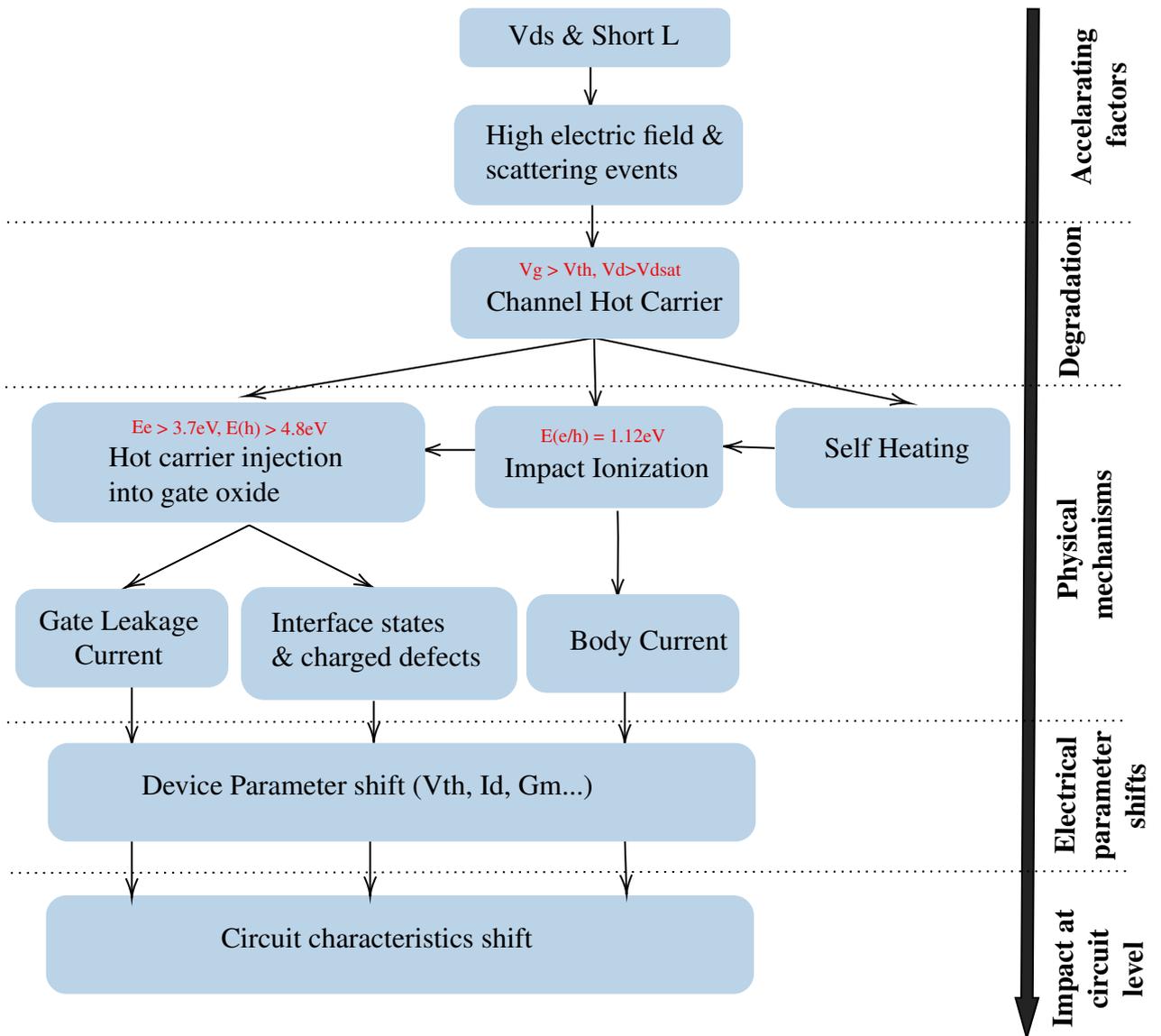


Figure 2.15: Hot carrier mechanisms taking place in MOSFET device

3 | Device Under Test and Experimental Procedure

This chapter describes the devices under test and the measurement techniques. Section 3.1 gives an overview of the testchip structure and devices under test. Section 3.2 will present the details of the technique and methodology implemented in this work, as well as the approaches used for assessing the device reliability from raw measurement data. Aging stress conditions are listed. Finally, in the last two sections, we present the experimental extraction method to estimate the threshold voltage shift due to aging and briefly introduce the well-known power-law equation.

3.1 Devices Under Test (DUT)

The test chip is designed for testing the impact of the HCI and BTI mechanisms on single transistors. It includes isolated MOS modules containing 1.8V nMOS 1.8V pMOS, 3.3V nMOS and 3.3V pMOS for high temperature test. Several feature sizes have been investigated: $W/L=20\mu\text{m}/0.18\mu\text{m}$, $W/L=20\mu\text{m}/0.35\mu\text{m}$, $20\mu\text{m}/0.5\mu\text{m}$ and $W/L=20\mu\text{m}/0.8\mu\text{m}$. The cross section of these nMOS and pMOS is presented in Figure 3.1. All transistors under test are triple-well isolated which provide better substrate noise isolation. These devices have been chosen because most of Schlumberger's ASIC are mixed-signal which requires good noise isolation.

Table 3.1 and Table 3.2 give the information of gate oxide thicknesses and the operating conditions provided in datasheet, respectively. In Table 3.2, functional operation of the device at conditions between maximum operating conditions and absolute maximum (or between minimum and absolute minimum) is not implied; however, exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions beyond absolute values may induce damages to the devices.

STI: Shallow Trench Isolation
POLY: poly silicon gate

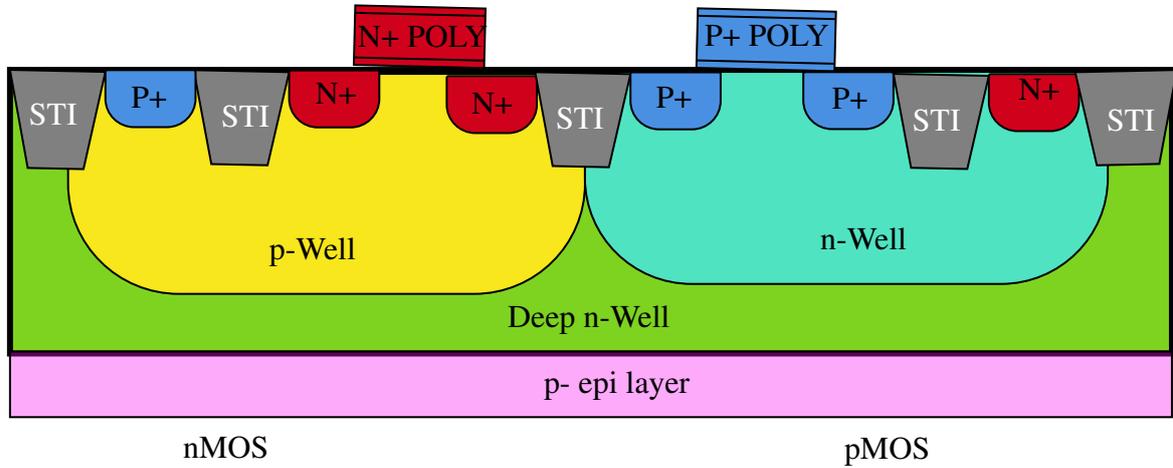


Figure 3.1: Cross section of nMOS and pMOS in this work

Type	Low value	Typical value	High value	Unit
1.8V nMOS	3.9	4.1	4.3	nm
1.8V pMOS	3.7	3.9	4.1	nm
3.3V nMOS	6.2	6.5	6.8	nm
3.3V pMOS	6.0	6.3	6.6	nm

Table 3.1: Gate oxide thickness

Type	Name	Temp. range	Abs. min	Min	Max	Abs. max
1.8V MOS	VDS	-40°C to 175°C	-2.3V	-1.98V	1.98V	2.3V
	VGS	-40°C to 175°C	-2.3V	-1.98V	1.98V	2.3V
3.3V MOS	VDS	-40°C to 175°C	-4V	-3.6V	3.6V	4V
	VGS	-40°C to 175°C	-4V	-3.6V	3.6V	4V

Table 3.2: Operating condition of isolated 1.8V and 3.3V MOSFETs

The testchips under test includes some modules for reliability characterizations as presented in Figure 3.2:

- BIP for bipolar transistor DC measurements
- CAPA - CAPF for capacitor measurements
- DIOA - DIOF for diode measurements
- MOSA - MOSF for MOS DC measurements
- RELA - RELD for MOS reliability characterization

- RESA - RESB for resistor measurements
- REL1 - REL2 corresponds to different bonding plans. REL1 is the bonding plan for 1.8V and 3.3V nMOS. REL2 is for 1.8V and 3.3V pMOS as listed in Table 3.3 and Table 3.4

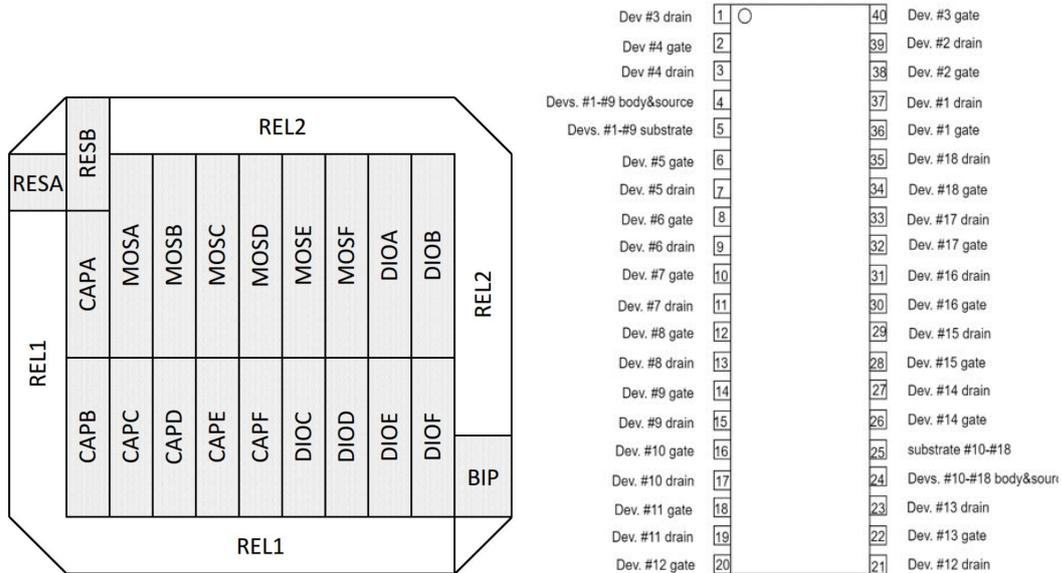


Figure 3.2: Overview of the testchip modules (right side) and DIL-40 package (left side)

	Device.	D	G	S,B	Parameters
1.8V nMOS	#1	37	36	4	W/L=10µm/0.18 µm, nfinger=2
	#2	39	38	4	W/L=10 µm /0.18 µm, nfinger=2
	#3	1	40	4	W/L=10 µm /0.18 µm, nfinger=2
	#4	3	2	4	W/L=10µm/0.18µm, nfinger=2
	#5	7	6	4	W/L=10µm/0.2µm, nfinger=2
	#6	9	8	4	W/L=10µm/0.22µm, nfinger=2
	#7	11	10	4	W/L=10µm/0.25µm, nfinger=2
	#8	13	12	4	W/L=10µm/0.5µm, nfinger=2
	#9	15	14	4	W/L=0.42µm/0.18µm, nfinger=2
3.3V nMOS	#10	17	16	24	W/L=10µm/0.35µm, nfinger=2
	#11	19	18	24	W/L=10µm/0.35µm, nfinger=2
	#12	21	20	24	W/L=10µm/0.35µm, nfinger=2
	#13	23	22	24	W/L=10µm/0.35µm, nfinger=2
	#14	27	26	24	W/L=10µm/0.4µm, nfinger=2
	#15	29	28	24	W/L=10µm/0.5µm, nfinger=2
	#16	31	30	24	W/L=10µm/0.6µm, nfinger=2
	#17	33	32	24	W/L=10µm/0.8µm, nfinger=2
	#18	35	34	24	W/L=0.42µm/0.35µm, nfinger=2

Table 3.3: Description of REL1 bonding plan into DIL-40 package. Green indicates the devices used for aging test.

	Device.	D	G	S.B	Parameters
1.8V pMOS	#1	37	36	4	W/L=10 μ m/0.18 μ m, nfinger=2
	#2	39	38	4	W/L=10 μ m /0.18 μ m, nfinger=2
	#3	1	40	4	W/L=10 μ m /0.18 μ m, nfinger=2
	#4	1.8V ESD pad verification at pads 2, 3			
	#5	7	6	4	W/L=10 μ m/0.2 μ m, nfinger=2
	#6	9	8	4	W/L=10 μ m/0.22 μ m, nfinger=2
	#7	11	10	4	W/L=10 μ m/0.25 μ m, nfinger=2
	#8	13	12	4	W/L=10 μ m/0.5 μ m, nfinger=2
	#9	15	14	4	W/L=0.42 μ m/0.18 μ m, nfinger=2
3.3V pMOS	#10	17	16	24	W/L=10 μ m/0.35 μ m, nfinger=2
	#11	19	18	24	W/L=10 μ m/0.35 μ m, nfinger=2
	#12	21	20	24	W/L=10 μ m/0.35 μ m, nfinger=2
	#13	3.3V ESD pad verification at pads 22, 23			
	#14	27	26	24	W/L=10 μ m/0.4 μ m, nfinger=2
	#15	29	28	24	W/L=10 μ m/0.5 μ m, nfinger=2
	#16	31	30	24	W/L=10 μ m/0.6 μ m, nfinger=2
	#17	33	32	24	W/L=10 μ m/0.8 μ m, nfinger=2
	#18	35	34	24	W/L=0.42 μ m/0.35 μ m, nfinger=2

Table 3.4: Description of REL1 bonding plan into DIL-40 package. Green indicates the devices used for aging test.

3.2 Aging test campaign and stress conditions

Before launching the aging tests, an initial characterization at wafer level was performed using probe station and equipment available at IMS laboratory. The details about the test bench and associated equipment can be found in Appendix A. At least 10 devices for each type were characterized to evaluate the typical technological dispersion. Furthermore, the measurements on wafer at different temperatures (25°C, 50°C, 125°C, 175°C, 200°C and 230°C) provided us data for evaluating the accuracy of the associated compact model and defined a reasonably extreme temperature for aging test campaign to avoid device catastrophic failure. After that, all dies were packaged into ceramic DIL-40 allowing performing the long-term tests at elevated temperatures.

An intensive aging test campaign for both nMOS and pMOS featuring different gate lengths was conducted using Schlumberger test facility as (Figure 3.3). BTI and HCI were characterized under operating voltage biases and elevated stress temperatures (25, 150°C, 210°C and 230°C). The duration of aging tests were up to 2,000 hours. Table 3.5 and Table 3.6 present bias stress conditions for 1.8V and 3.3V transistors; note that the asterisk (*) is

used to distinguish the stress conditions of 3.3V from 1.8V transistors.

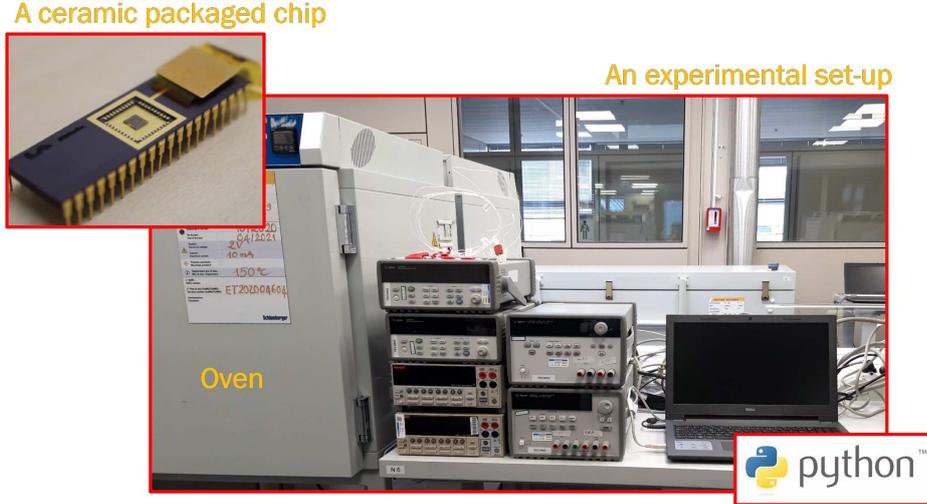


Figure 3.3: An aging test set-up at Schlumberger laboratory.

For HCI characterization, drain avalanche hot carrier (**DAHC**) in nMOS has been performed with $V_{gs} \approx 0.5V_{ds}$ corresponding to the maximum body current. This stress condition is commonly used in standard hot carrier characterization for low-voltage MOSFETs [104], [105], where the generated hot carriers are proportional to the body current and therefore, HCI degradation is maximized when body current achieves its peak value.

Channel hot electron (**CHE**) mechanism in nMOS or channel hot hole (**CHH**) mechanism in pMOS has been performed with maximum drain voltage and maximum gate voltage $|V_{gs}| = |V_{ds}|$, which corresponds to maximum device biases recommended in datasheet.

	$ V_{ds} $ (V)	$ V_{gs} $ (V)
DAHC	2.0	1.0
CHE	2.0	2.0
NBTI_1	0.05	1.8
NBTI_2	0.05	2.0
NBTI_3/CHH	2.0	2.0
PBTI	0.05	2.0

Table 3.5: Bias stress conditions for 1.8V transistors

For NBTI characterization, NBTI_1 and NBTI_2 correspond to two different $|V_{gs}|$ values (1.8V - 2.0V for 1.8V pMOS and 3.3V - 3.6V for 3.3V pMOS, respectively). In order

to activate uniform NBTI degradation, drain voltage $|V_{ds}|$ is kept quite small (0.05V - 0.1V) during the stress phase. A more aggressive $|V_{ds}|$ would have triggered unwanted HCI causing the overestimation of the NBTI degradation.

Because the CHH bias conditions combined with the presence of high temperature can activate NBTI, the CHH bias condition is also considered as NBTI_3 to investigate the contribution of high $|V_{ds}|$ to the NBTI degradation.

	$ V_{ds} $ (V)	$ V_{gs} $ (V)
DAHC*	3.6	1.8
CHE*	3.6	3.6
NBTI_1*	0.1	3.3
NBTI_2*	0.1	3.6
NBTI_3*/CHH*	3.6	3.6
PBTI*	0.1	3.6

Table 3.6: Bias stress conditions for 3.3V transistors

Regarding the impact of body bias (V_b) on NBTI and HCI degradation, literature results are somehow conflicting. In [106], the enhancement of NBTI degradation at high V_b is thought to be caused by substrate hot hole injection, which results in more interface state and positive charge generation, leading to worse NBTI degradation. In [51], threshold voltage shift was discovered to be independent of high V_b at the beginning of the test ($\approx 10^2s$) and then rapidly increasing with stress time. [107] reported an increase of threshold voltage shift for a value of the electric field in the gate oxide of about 9 MV/cm regardless the value of V_b . In addition, ΔV_{th} was stated independently of V_b by [35].

In the course of this thesis aging test campaign, the body bias is zero in all cases to reflect the real practical applications in Schlumberger circuits. The number of DUTs dedicated for this aging test campaign are listed in Table 3.7 and Table 3.8.

3.2. AGING TEST CAMPAIGN AND STRESS CONDITIONS

Temp.	W/L (μm)	Number of DUTs					
		DAHC	CHE	PBTI	NBTI_1	NBTI_2	NBTI_3/CHH
25°C	20/0.18	3	3	2	0	2	1
	20/0.5	1	1	0	0	0	0
150°C	20/0.18	3	3	2	2	2	1
	20/0.5	1	1	0	1	1	0
210°C	20/0.18	3	3	2	2	2	1
	20/0.5	1	1	0	1	1	0
230°C	20/0.18	0	3	1	0	0	0
	20/0.5	0	1	0	0	0	0

Table 3.7: DUTs (1.8V MOSFETs) dedicated for aging test: 52 devices in total.

Temp.	W/L (μm)	Number of DUTs					
		DAHC	CHE	PBTI	NBTI_1*	NBTI_2*	NBTI_3*/CHH*
25°C	20/0.35	1	1	1	1	1	1
	20/0.5	1	1	0	1	1	1
	20/0.8	1	1	0	1	1	1
150°C	20/0.35	1	1	1	1	1	1
	20/0.5	1	1	0	1	1	1
	20/0.8	1	1	0	1	1	1
210°C	20/0.35	1	1	1	1	1	1
	20/0.5	1	1	0	1	1	1
	20/0.8	1	1	0	1	1	1

Table 3.8: DUTs (3.3V MOSFETs) dedicated for aging test: 48 devices in total. The red parts indicate the missing results due to the test set-up issue.

3.3 Techniques and methodologies used in this work

As discussed in Chapter 2, the partial recovery of NBTI after stress conditions are reduced/removed is a critical feature. Therefore, one has to take care of the aging test protocol to fix it. Simple measurement approaches consisting of periodic stress interruptions for monitoring the full I–V characteristic of the DUTs are not appropriate for NBTI studies due to the significant relaxation observed after a few microseconds [50]. To deal with the NBTI relaxation time, two major techniques have been proposed in the literature. As mentioned in Chapter 2, the first technique includes the so-called Fast Measure-Stress-Measure techniques, which are based on capturing both the degradation and relaxation behaviour of NBTI. The second one includes the so-called On-The-Fly (OTF) techniques, which aim to monitor the entire NBTI-induced degradation without allowing any relaxation.

There were some experimental efforts to decrease delayed time between the stress phase and the subsequent measurement in order to minimise the recovery effect. While [108] measured with a time delay of 0.4 s, [58] published the NBTI results with a time delay of 1 ms, [109] and [110] reported with a time delay of 30 μs and 1 μs , respectively. Recently, [111] performed a massive fast measurement for NBTI with a time delay of 1 ns.

The rapid recovery following NBTI stress presents challenges for the characterisation of BTI, however, this recovery also contains important information about the defect kinetics that has been exploited by the extended measure-stress-measure (eMSM) technique [112], which is described as follows: It is decided to extend the recovery period in order to record threshold voltage recovery behaviour with time and then applying stress conditions again with incremental stress periods. Conveniently, if the stress times are increased exponentially by a factor of 10, the subsequent phases are often unaffected by the recovery effect [110], [113] as shown in Figure 3.4. Each interruption in stress results in recovery phases that quickly restored to the same trend as prior to the interruption [113].

The technique of choice used in this PhD thesis is the eMSM technique. The eMSM approach was chosen because it gives a huge amount of information without needing specific custom built circuitry for its implementation [114]. Regarding to our work, there was a long interruption ($\approx 60h$) of the aging test on all 3.3V transistors at $t = 800h$ because the

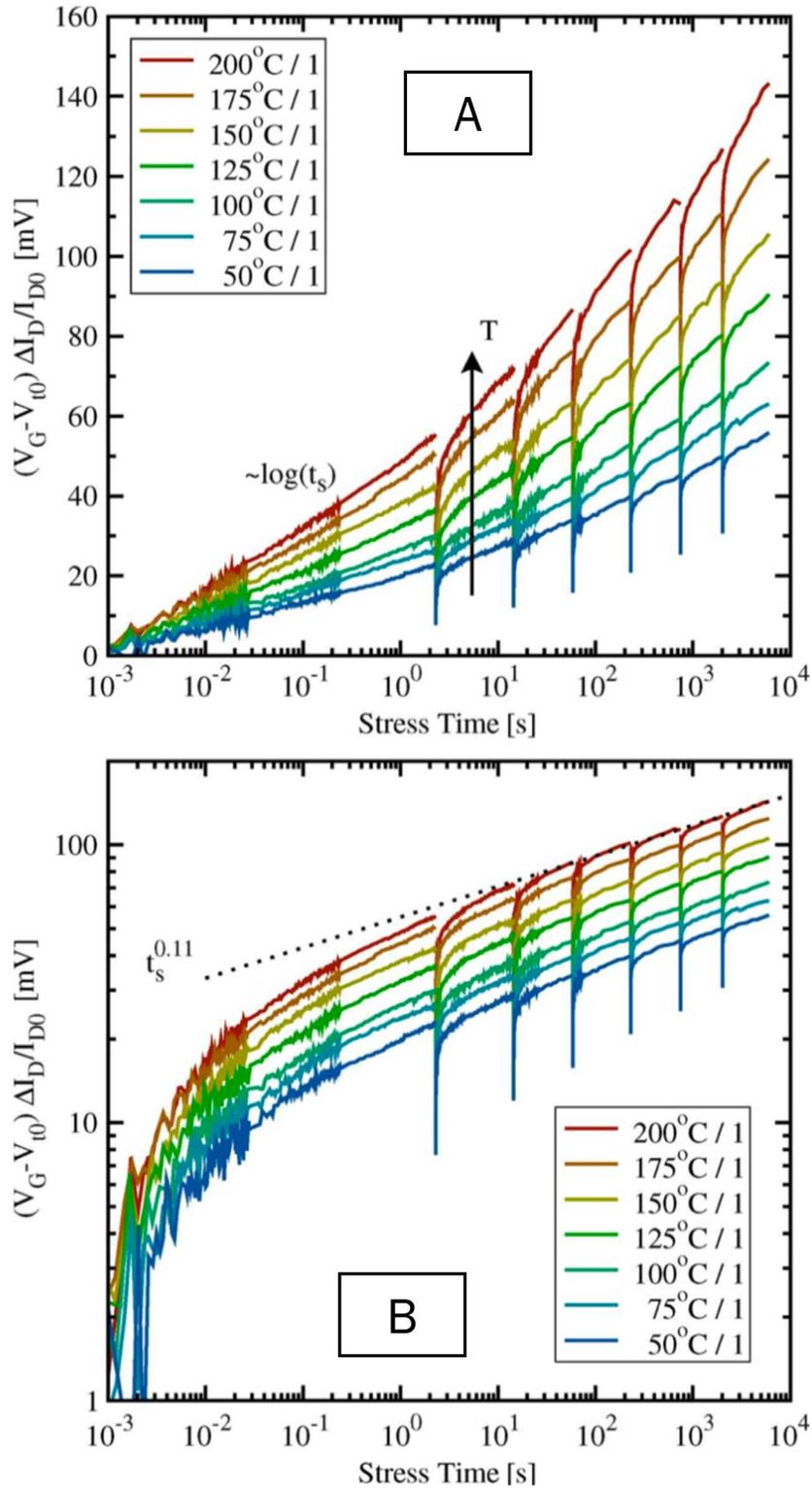


Figure 3.4: NBTI degradation of a pMOS under eMSM technique at different temperatures in lin-log (A) and log-log (B) scale. The measurements were conducted on pMOS with $T_{ox} = 1.4$ nm, $V_{gs} = -2$ V, and $E_{ox} \approx 8$ MV/cm [113]

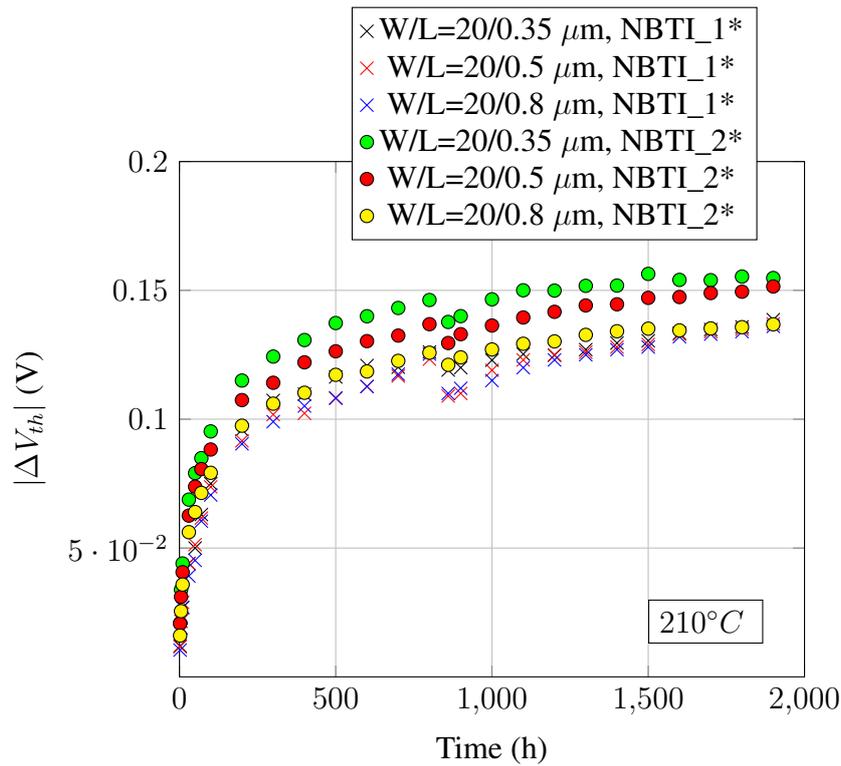


Figure 3.5: Threshold voltage degradation due to NBTI on 3.3V pMOS devices showing a recovery during the interruption at $t = 800h$

laboratory had an electrical shutdown during the weekend for maintenance. The aging tests were restarted again at $t = 860h$ and it shown a clearly reduction in ΔV_{th} . But the ΔV_{th} has quickly "restored" to the undisturbed level at $t = 1000h$ as in Figure 3.5. Refer to Figure 4.4 and Figure 4.5 in Chapter 4 to see the ΔV_{th} in log-log scale, which show the insignificant impact of recovery to the trend of NBTI degradation. The recovery effect were not observed in 3.3V nMOS (Figure 4.13 in Chapter 4)

Figure 3.6 depicts the implementation of the eMSM technique for DAHC characterization of nMOS devices. For simplicity, just the set up of DAHC test is described here. The real implementation is much more complicated than in Figure 3.6 to be able to perform all mechanisms under test at 25, 150, and 210°C. The system used for the reliability tests consisted of Keithley source meters (2410SM), data acquisitions (34970A) with switch units (34903 SU), power supplies and the ovens. The first Keithley source meter (denoted as K1) is used to measurement the drain and the second one (denoted as K2) is for the gate. The data acquisitions (34970A) consists of maximum three slots for inserting switch unit which

have 20 channels (switches) denoted from CH_1 to CH_20. The packaged chips are placed on a printed circuit board and put into the oven. The measurement system must be capable of the simultaneous application of voltage and measurement of current at the gate, drain, and substrate terminals of the device. Before any data collection, the repeatability of the monitored parameters (such as I_{dlin} , I_{dsat} , V_{th}) must be within 0.5%. In DAHC stress phase, the channels of the drain and the gate are switched to 2V and 1V. The source is switched to float on the one end. Note that the source, the body and the substrate are connected and grounded on the other end. In the characterization phase, the channels of the drain and the gate are switched to K1(+) and K2(+). The source is switched to K1(-) and K2(-) to measure the I-V characteristics. When one DUT is in characterization phase, the rest of DUTs are in stress phase. We have encrypted a dedicated Python programs to control the entire system through a GPIB interface. The use of a high-level programming language to operate the entire system enables advanced capabilities, such as the ability to construct complex measurement sequences that are conducted on multiple DUTs.

A final $I_{gs} - V_{gs}$ characteristic was recorded at the end of each characterization sequence to ensure that the DUT was still functional and no significant increase in gate leakage current was caused by exceed temperature and bias stress (due to Stress Induced Leakage Current (SILC) or Time-Dependent Dielectric Breakdown (TDDB) mechanisms), as this can affect the accuracy of the measured ΔV_{th} .

3.4 Vth extraction methodology

The threshold voltage V_{th} is a critical parameter in the analysis of MOS transistors. The classical definition of threshold, $\Phi_s = 2\Phi_F + V$ which links the surface potential, the Fermi level, and the channel potentials together. Threshold voltage may be fundamentally understood as the gate voltage value at which the transition between weak and strong inversion takes place. Because this transition is so gradual, no noticeable point in the I_{ds} vs. V_{gs} characteristic can be easily recognized as the threshold voltage. This is one of the reasons why several threshold voltage definitions have been offered in the literature. There are multiple theoretical definitions [115], [116], [117] as well as several experimental extraction methods

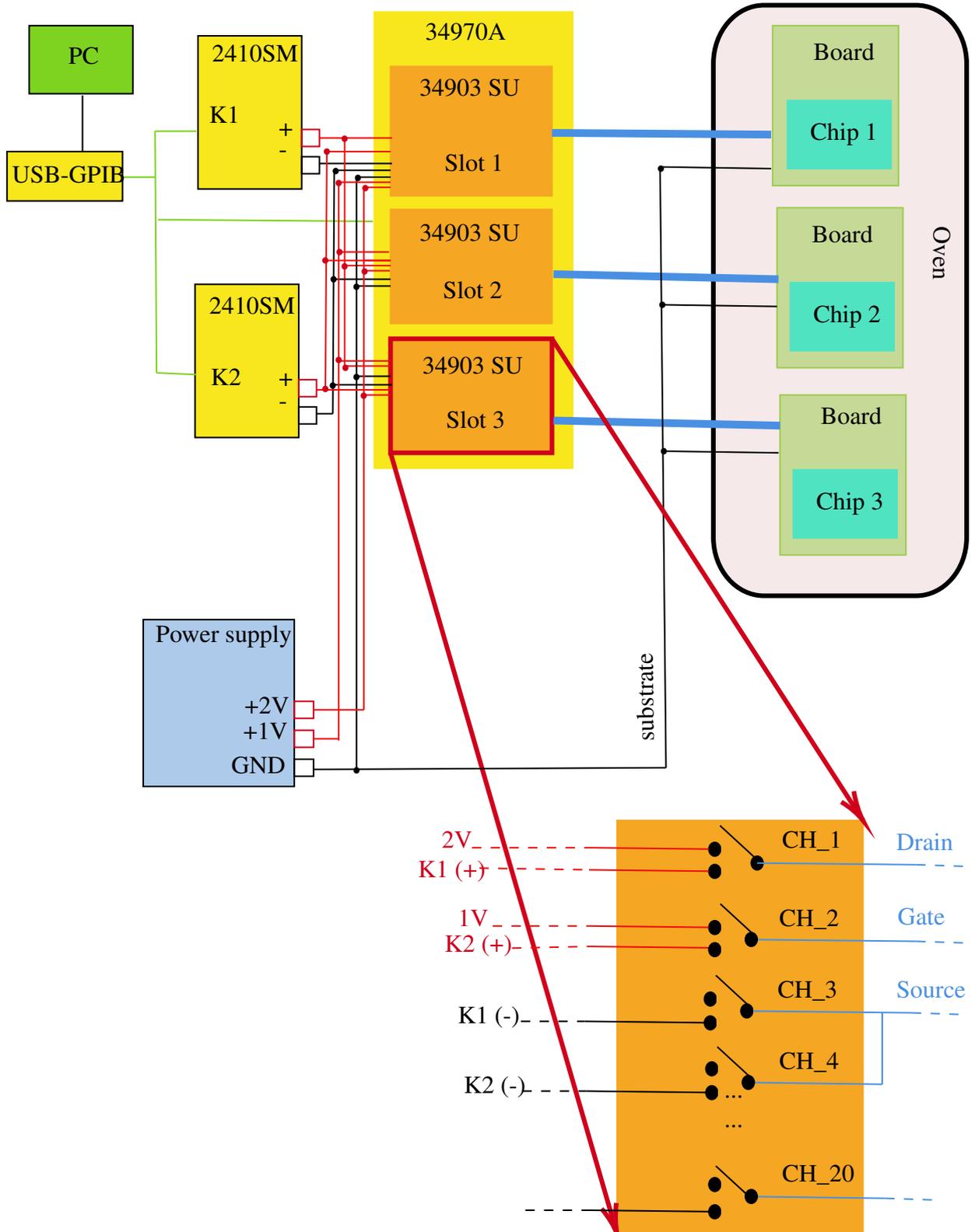


Figure 3.6: Experimental set-up for DAHC test

which are explained hereafter.

3.4.1 Constant Current Method

The Constant Current technique [118] calculates the threshold voltage as the gate voltage, V_{gs} , for a given arbitrary constant drain current, I_{ds} , and $V_{ds} = 100mV$. $W \times 10^{-7}$ is a typical number for this arbitrary constant drain current, where W and L are the channel width and length, respectively. This approach is commonly utilized in industry. Despite its simplicity, this technique has the significant problem of being completely dependent on an arbitrarily set value of the drain current level. This method is demonstrated in Figure 3.7, where different gate voltages at different drain current levels may be used to represent the threshold voltages.

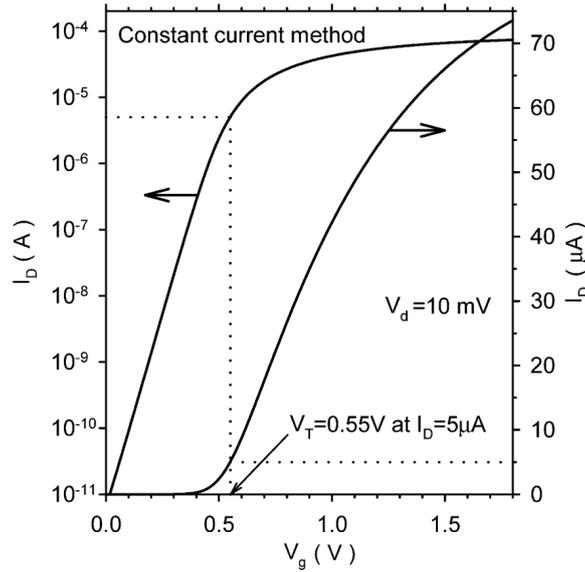


Figure 3.7: CC method implemented on the I_{ds} - V_{gs} transfer characteristics [118].

3.4.2 Extrapolation in the linear region method (ELR)

The ELR technique [118] is one of the most widely used threshold-voltage extraction methods. It entails determining the gate-voltage axis intercept (i.e., $I_{ds} = 0$) of the linear extrapolation of the I_{ds} - V_{gs} curve at its maximum first derivative value (i.e., the maximum transconductance, g_m), as shown in Figure 3.8. The value of V_{th} is derived by adding

$V_d = 2\text{V}$ to the resultant gate voltage axis intercept, which is 0.51 V for the device under consideration. The main disadvantage of this method is that the maximum slope point may be uncertain; as a result, the extrapolated V_{th} can be heavily impacted.

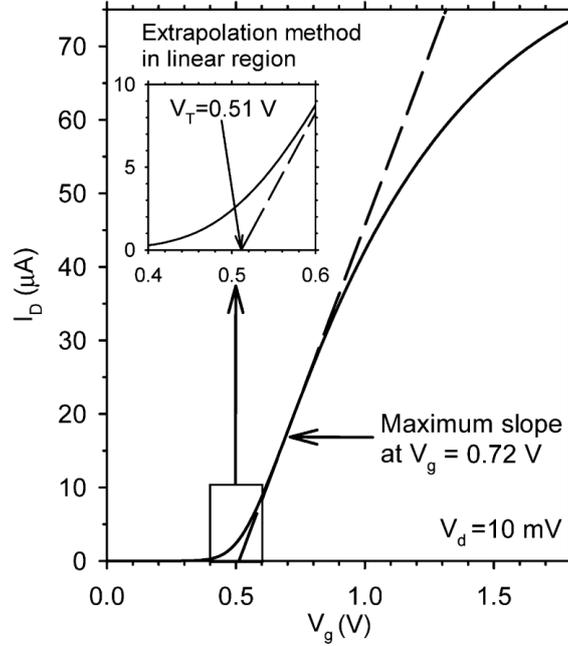


Figure 3.8: ELR method implemented on the $I_{ds}-V_{gs}$ transfer characteristics [118].

3.4.3 Transconductance extrapolation method in the linear region (GMLE)

GMLE technique developed in 1998 [118] implies that the threshold voltage is equal to the gate voltage axis intercept of the g_m-V_{gs} characteristics at their highest first derivative (slope) point. When the device is biased in the linear area, this technique is as follows (i) In weak inversion, the transconductance is exponentially related to the gate bias; (ii) In strong inversion, if the series resistance and mobility degradation are negligible, the transconductance approaches a constant value; (iii) In strong inversion, the transconductance decreases slightly with gate bias due to the series resistance and mobility degradation; and (iv) In the transition region between weak and strong inversion, the transconductance is linearly related to the gate bias. Figure 3.9 illustrates how this strategy is applied to the g_m-V_{gs} characteristics, resulting in an apparent value for V_{th} of just 0.44 V .

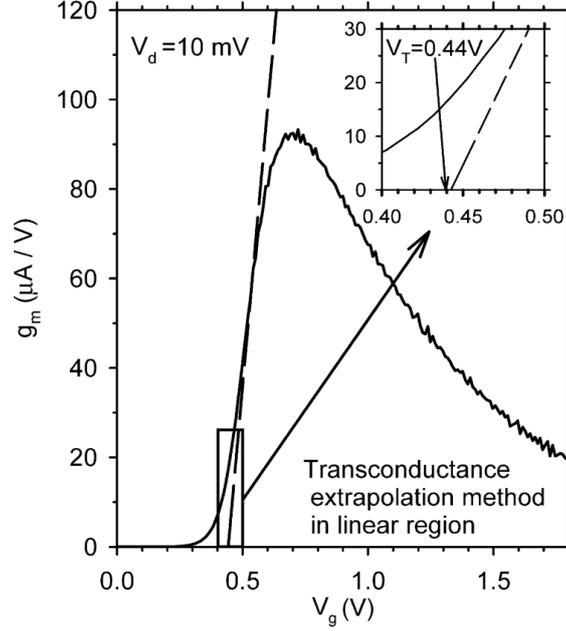


Figure 3.9: GMLE method implemented on the $g_m = dI_d/dV_g$ versus V_g characteristics [118].

3.4.4 Extrapolation method in the saturation region (ESR)

This method was used in this thesis work to extract the threshold voltage shift due to the aging. To determine the saturation threshold voltage V_{thsat} , the drain current must be measured as a function of gate voltage at $V_{ds} = V_{gs}$, ensuring that the device is operating in the saturation regime. The drain current in saturation mode obeys the square law:

$$I_{dsat} = \frac{W}{L} C_{ox} \mu \frac{1}{2} (V_{gs} - V_{th})^2 \quad (3.1)$$

Plotting $\sqrt{I_{ds}}$ versus V_{gs} , should result in a straight line that intercepts the V_{gs} axis in V_{th} , as in Figure 3.10. By fitting a straight line through the points, V_{th} can be found at the interception of the line with the V_{gs} axis.

3.5 Power-Law degradation

The simple power-law degradation is often encountered in literature and can be de-

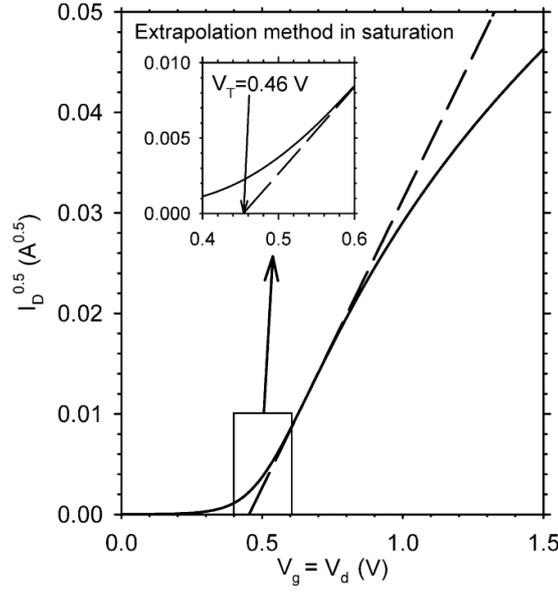


Figure 3.10: ESR method implemented on the measured $\sqrt{I_{ds}} \sim V_{gs}$ characteristics [118].

scribed in the form of

$$y = A \times x^n \quad (3.2)$$

where A is a constant, x is the stress time, n is a power-law time dependence which is in the range between 0 and 1. Note that the simple power law can be written as

$$\log y = \log A + n \log x \quad (3.3)$$

Thus, a power law function appears as a straight line on a log-log plot.

Equation 3.2 was already used to characterize BTI in 1978, and it was measured by the shift of the flatband voltage ΔV_{FB} as a function of stress time t and stress voltage V_g by [119]

$$\Delta V_{FB} \approx A |V_g|^\gamma t^n \exp\left(\frac{-E_a}{k_B T}\right) \quad (3.4)$$

where n is the power law time dependency (0.2 in the original work), A is the offset of ΔV_{FB} , and E_a is the activation energy. Since then, the power law description has been frequently used for BTI investigation to provide simple and relatively accurate assessments of degradation.

3.5.1 Conclusion

This chapter gave a general description of the devices under test. A vast number of transistors have been considered to investigate wear-out mechanisms. We performed the aging test campaign on 1.8V and 3.3V transistors with dedicated bias and temperature conditions to activate each intrinsic degradation mechanism (CHE/CHH, DAHC, NBTI, PBTI). The schematic of the test configurations and methodologies were described in detail. We applied the eMSM technique to capture transistor degradation during the aging tests, and threshold voltage shifts were extracted using ESR method. Finally, we introduced power law, which is often encountered in literature. This chapter gives the necessary information for readers before going deeper into the analysis of aging results presented in the next chapter.

4 | Experimental results and reliability modelling

4.1 Introduction

To develop the aging models and associated parameter values to the technologies under test, the aging test campaign was launched to investigate the wear-out mechanisms. The first activity of this campaign is the initial characterization of the transistors at wafer level as presented in Section 4.2. The second one is the aging tests of packaged chips at various temperatures up to 230°C. In most of the published research works [120] [121], [122], HCI and BTI characterizations have been conducted at elevated voltages beyond the safe operating conditions to accelerate the degradation within a short time (from seconds to several hours). This approach presents the risk of over-accelerating other different wear-out mechanisms that are not supposed to be experienced in circuit at normal operating conditions. Therefore, we performed a long-term test in which we characterized BTI and HCI degradation at the operating voltages with the stress time up to 2,000 hours. These experimental results are expected to reflect the real wear-out in practical application. Due to the aging effects, the transistor characteristics degrade gradually with stress time under dedicated stress conditions already explained in Table 3.5 and Table 3.6 (Figure 4.1). This chapter mainly focuses on the final results and analysis of the aging tests after the completion of the full 2000 hours and the derived aging models for HCI/NBTI are proposed after that.

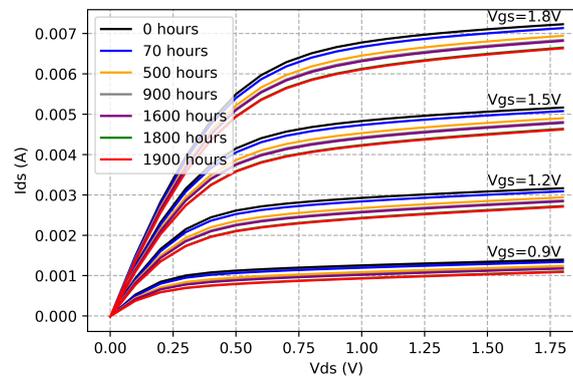


Figure 4.1: A nMOS device showing degradation of drain current under CHE bias condition at 150°C. Experimental data collected on W/L=20/0.18 μm 1.8V nMOS.

4.2 Initial characterization at wafer level

The DC initial characterization (before aging tests) was performed for temperatures exceeding 175°C to evaluate the compact model accuracy before aging test. Indeed, the temperature range exceeds the specification of the industrial technologies under test. The electrical characterization was measured within the safe operating area for several transistor geometries for both 1.8V and 3.3V isolated transistors. The detailed results are presented in Appendix A.

In this phase, at least 10 devices of each geometry were characterized at wafer level to evaluate the technology dispersion. According to our results, the average dispersion of less than 5% indicates the maturity of the technology. The measurements and simulations were compared for temperatures higher than 175°C for which the compact model associate to these technologies is not initially designed for. Depending on the operation regimes and biases, it shows that the compact model is not really accurate. The simulation differences compared to a mean measurement value are sometimes up to 15% in some cases, for instance, 1.8V nMOS (W/L=10/0.5 μ m) at room temperatures and 3.3V nMOS (W/L=10/0.35 μ m) at temperature above 200°C. Therefore, V_{th0} of the compact model have been slightly modified ($\pm 0.02 - 0.05V$) to fit the simulation results with the measurement ones. Finally, The DUTs are still well functional and present a low dispersion (below 5%) even at 230°C. The body leakage current potentially generated by the impact ionization were measured also. The peak of the body currents were found at $V_{gs} = 0.4 - 0.6V_{ds}$, which is in line with the value provided in the datasheet.

4.3 Bias Temperature Instability Modelling

As discussed in Chapter 2, BTI is a physical phenomenon related to the generation and activation of the interface traps and oxide trapped charges inside the dielectric layer. The mechanism is accelerated by elevated temperature (in the range of 100°C to 250°C) and high vertical electric field. BTI is observed in both nMOS and pMOS. Negative Bias Temperature Instability (NBTI) mainly impacts pMOS when negative gate voltage is applied and Positive

Bias Temperature Instability (PBTI) mainly impacts nMOS with positive gate voltage at elevated temperature. The sub sections hereafter present the BTI dependency as a function of V_{gs} , temperature, V_{ds} and gate length for 1.8V and 3.3V transistors.

4.3.1 Negative Bias Temperature Instability (NBTI)

Two configurations NBTI_1 and NBTI_2 bias conditions were applied at 150°C and 210°C to characterize NBTI degradation at different V_{gs} . According to our results, the threshold voltage shifts due to NBTI_1 and NBTI_2 bias voltages have been observed following a power-law as function of stress time (Figure 4.2):

$$\Delta V_{th} = A \times t^n \quad (4.1)$$

where A is the prefactor and n is the time exponent parameter. At 150°C, the value of n is in the range of 0.29-0.31 regardless of different $|V_{gs}|$ bias conditions. However, this value decreases down to 0.16-0.17 under 210°C with the similar stress voltages applied. These n values associated with their respective stress conditions are presented in the Table 4.1.

T°C	Bias type	n value
150	NBTI_1	0.29 - 0.31
	NBTI_2	0.31 - 0.32
	NBTI_3	0.30
	PBTI	Not clear
210	NBTI_1	0.17 - 0.18
	NBTI_2	0.16
	NBTI_3	0.18
	PBTI	0.18 - 0.23

Table 4.1: Value of n extracted from our experiments

According to Table 4.1, the values of n do not depend on bias stress conditions. However, it seems that n features a dependency according to the stress temperature, i.e, $n \approx 0.3$ at 150°C and $n \approx 0.18$ at 210°C.

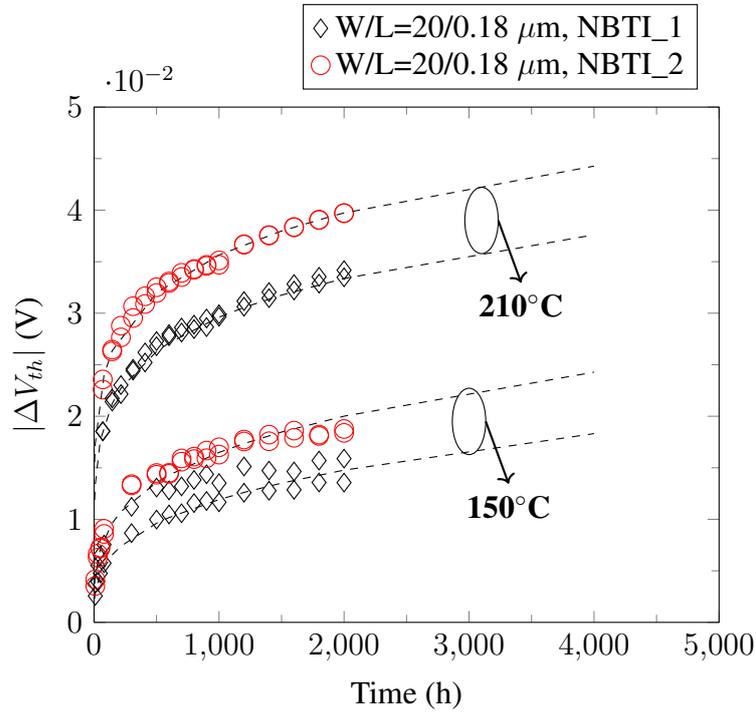
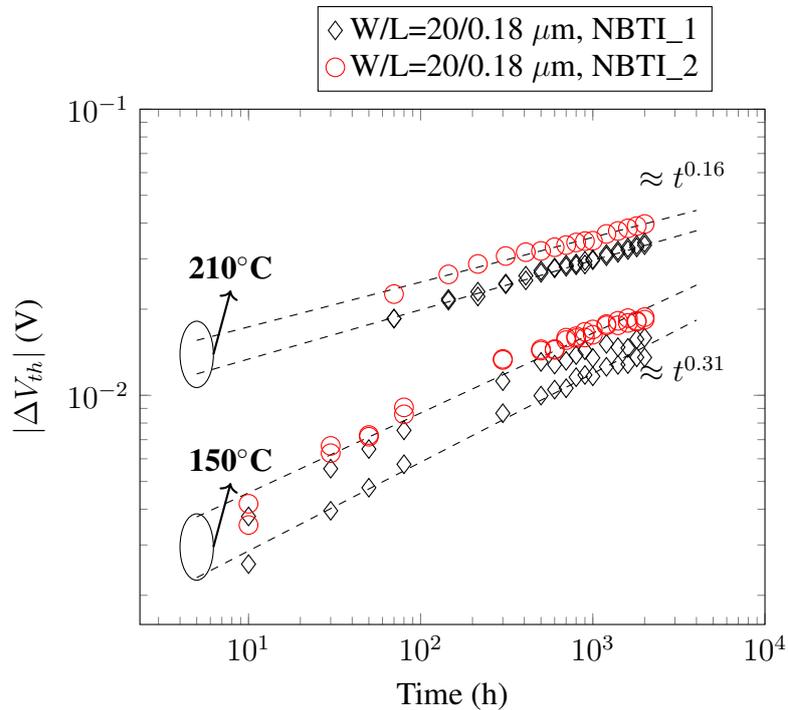

 (a) Measured NBTI-induced ΔV_{th} in linear-linear scale

 (b) Measured NBTI-induced ΔV_{th} in logarithmic-logarithmic scale

Figure 4.2: Measured NBTI-induced ΔV_{th} as a function of stress time under NBTI_1 and NBTI_2 at 150°C and 210°C. Experimental data collected on W/L=20/0.18 μm 1.8V pMOS. Dot lines are fitted lines to the experimental data.

Referring to published works [123], [124] on NBTI degradation for temperatures in the range of 100°C - 200°C, a various value of $n \approx 0.16 - 0.5$ are reported depending on the mobile species inside the oxide layer, i.e, H_2 or/and H_0 or/and H^+ using reaction-diffusion (R-D) model. In these works, the values of n have been considered independent with temperature, but n varies with stress time due to the creation and/or recombination of hydrogen ions during the test. Table 4.2 presents the reported value of n depending on the type of mobile species inside the dielectric layer.

Model	Reaction	Mobile Species	n value
I	$SiH + H^+ \rightleftharpoons Si^+ + H$	H	0.25
II	$SiH + H^+ \rightleftharpoons Si^+ + 0.5 H_2$	H_2	0.165
III	Model I and II	H, H_2	0.165-0.25
IV	$SiH + 2H^+ \rightleftharpoons Si^+ + H^+$	H^+	0.25-0.5
V	Models I, II and III	H^0 , H^+ , H_2	0.165-0.5
VI	Model I and trapping of H	H	> 0.25
VII	Model I and release of H	H	< 0.25
VIII	Model II and trapping of H_2	H_2	>0.165
IX	Model II and release of H_2	H_2	< 0.165

Table 4.2: Effect of different species on time exponent n [123]

From the experimental results, our proposal hypothesis here is that different temperatures can trigger different types of mobile species resulting in the discrepancy of n as presented in Table 4.2. Another inspected reason is the different NBTI recovery rates at different temperatures where the faster recovery may occur at higher temperature leading the different n values.

It is well-known that the saturation of defect generation in the gate oxide may lead to

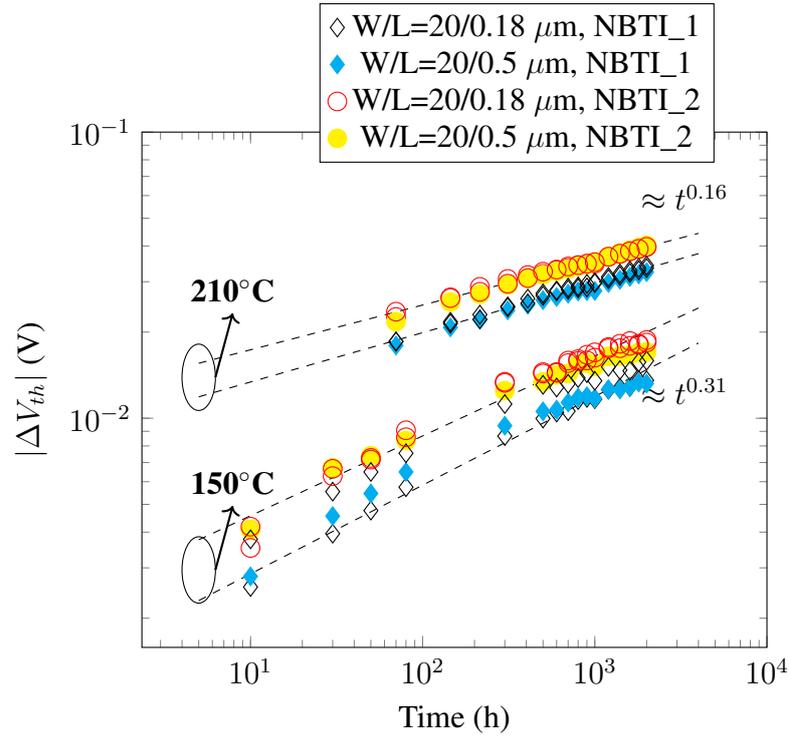
the saturation of the BTI degradation, eventually impact the time slope n [35], however, the saturation effect was not clearly observed in our 1.8V pMOS after 2,000h stressed.

NBTI is a homogeneous effect depending on the oxide electric field applied to the gate [125]. Therefore, NBTI does not depend on lateral electric fields and it should not exhibit any gate length dependence. However, some published studies indicate that the $|\Delta V_{th}|$ of p-MOSFET increases with the decreasing of channel length due to a spatially non-uniform degradation along the channel. It has been reported that the defect density near the gate edge and the gate source/drain overlapping regions is higher than that existing in the center region of the channel [126], [127], [128].

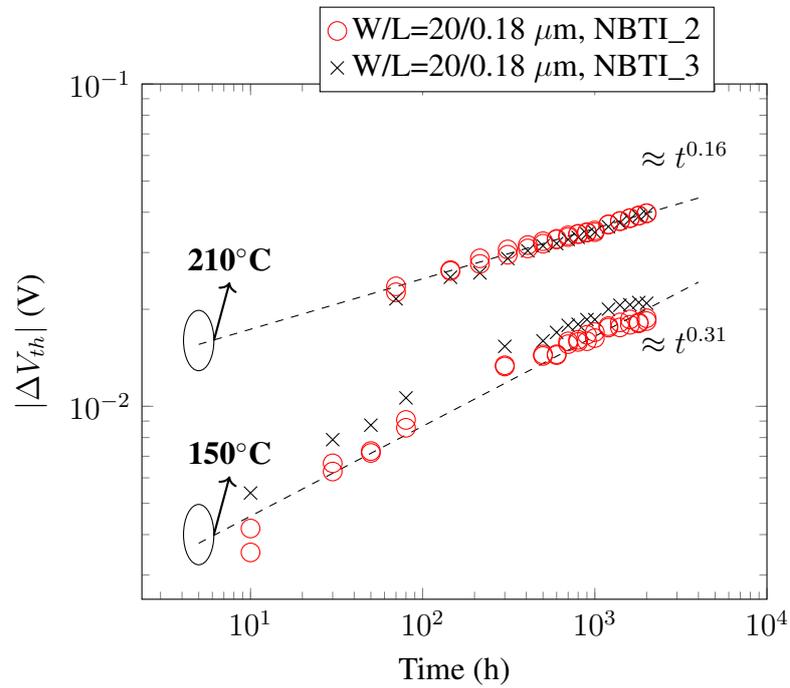
Our NBTI tests conducted on 0.18 μm and 0.5 μm gate length devices revealed the independence of BTI degradation. Our NBTI tests conducted on 0.18 μm and 0.5 μm gate length devices revealed the independence of BTI degradation on gate length value, i.e., the similar threshold voltage shifts have been obtained when applying the same stress conditions as shown in Figure 4.3 (a), implying that the defects are uniformly distributed in the whole channel of the transistors.

To investigate the role of $|V_{ds}|$ in NBTI degradation, we performed the aging test with NBTI_3 bias condition and compared the V_{th} with one suffering NBTI_2 bias condition under 150°C and 210°C. The high $|V_{ds}|$ in NBTI_3 bias condition may activate both NBTI and HCI. In our case, NBTI degradation was not affected by $|V_{ds}|$ for $|V_{ds}|$ lower than 2V. The ΔV_{th} under NBTI_2 and NBTI_3 are quite similar implying that HCI under NBTI_3 is negligible and $|V_{ds}|$ does not have a significant impact on NBTI degradation (Figure 4.3 (b)). With $|V_{ds}|$ lower than 2V, it is expected that holes have less chance to gain the energy up to 4.5eV to become channel hot carriers [49].

In 3.3V pMOS, NBTI degradation under NBTI_1*, NBTI_2* and NBTI_3* are well fitted with the power-law for temperature equal to 150°C (Figure 4.4). However, we observed a saturation behavior of threshold voltage shift for temperature equal to 210°C (Figure 4.5) and we cannot fit it with a single power-law equation. At beginning of the test, the ΔV_{th} features a time exponent close to $t^{0.3}$, while ΔV_{th} of the rest of the test features a time exponent close to $t^{0.18}$. Like for the 1.8V devices, the role of $|V_{ds}|$ in NBTI degradation appears not significant because the ΔV_{th} under NBTI_2* and NBTI_3* condition are approximately

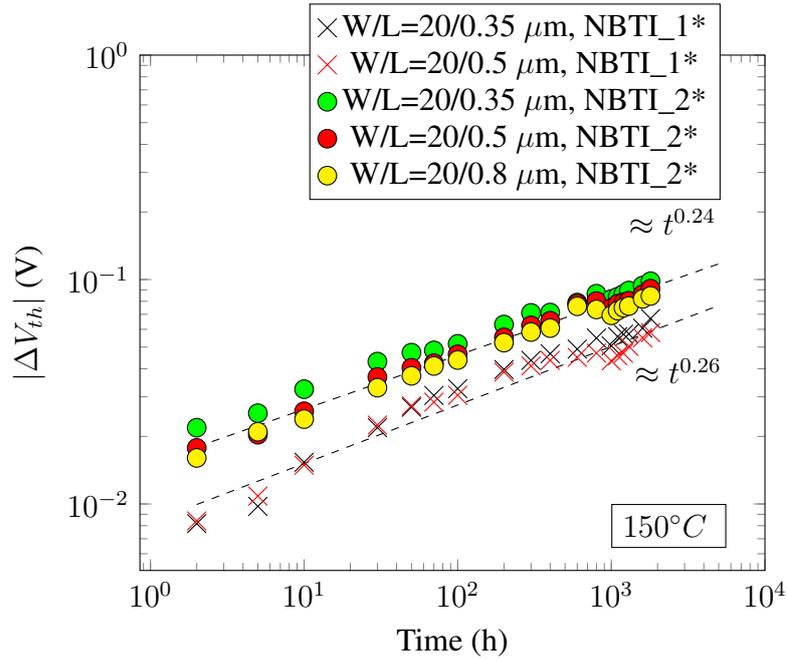


(a)

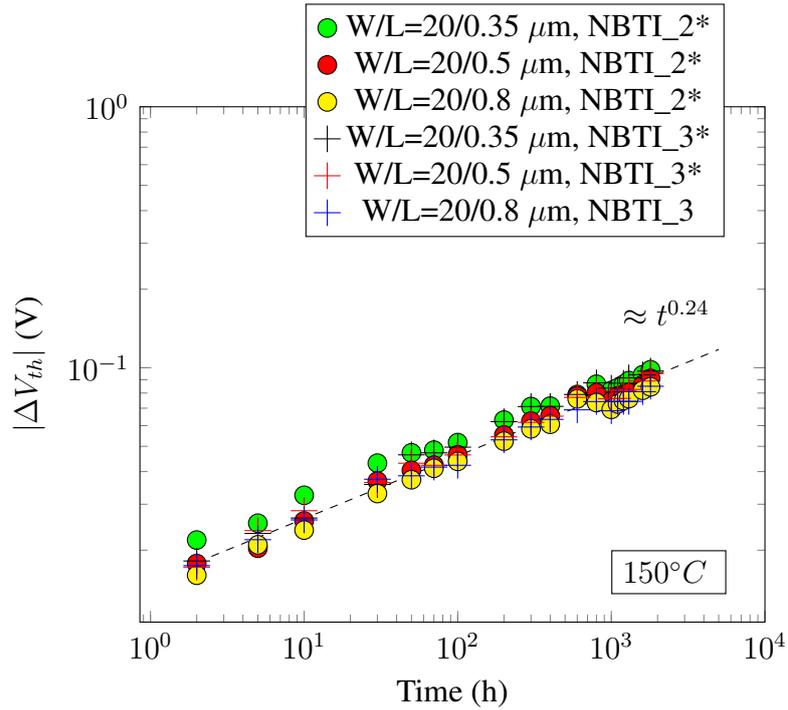


(b)

Figure 4.3: Measured NBTI-induced ΔV_{th} as a function of stress time under NBTI_1, NBTI_2 (a) and NBTI_2, NBTI_3 (b) at 150°C and 210°C . Experimental data in Figure (a) and Figure (b) were collected on $W/L=20/0.18 \mu\text{m}$ and $20/0.5 \mu\text{m}$ 1.8V pMOS.



(a)



(b)

Figure 4.4: Measured NBTI-induced ΔV_{th} as a function of stress time under NBTI_1*, NBTI_2* (Figure (a) and NBTI_2*, NBTI_3* (Figure (b)) at $150^\circ C$. Experimental data collected on $W/L=20/0.35\mu m$, $20/0.5\mu m$ and $20/0.8\mu m$ 3.3V pMOS. Note that the measurement data of $W/L=20/0.8\mu m$ in Figure (a) was missed due to the set-up issue as already mentioned in Table 3.8

equal as shown in Figure 4.4 (b) and Figure 4.5 (b).

As discussed in Chapter 2, the magnitude of the NBTI degradation was seen to be proportional to the applied gate stress voltage, i.e, higher negative voltages result in greater degradation. A study of NBTI degradation with varying gate oxide thicknesses [62] reported that the shift of threshold voltage ΔV_{th} does not depend on the gate oxide thickness. When investigating NBTI on DUTs with a given oxide thickness, the degradation depending on the gate overdrive voltage $V_{ov} = |V_{gs} - V_{th0}|$ is often observed, with this voltage being directly related to the oxide electric field ($E_{ox} \approx V_{ov}/t_{ox}$). The prefactor A in Equation 4.1 is commonly seen to follow a power-law of the applied V_{ov} .

$$A \propto E_{ox}^\gamma \approx \left(\frac{V_{ov}}{t_{ox}}\right)^\gamma \approx \left(\frac{|V_{gs} - V_{th0}|}{t_{ox}}\right)^\gamma \quad (4.2)$$

where γ is in typical range of [2.5-3] for Si device [61].

We fitted our experiment results to the Equation 4.2 and found that the values of γ are close to 3.3 for 1.8V pMOS and close to 3.0 for 3.3V pMOS (Figure 4.6(a)). Contrary with the pre-factor A , the time exponent n is independent with the applied gate voltage [35].

The temperature dependence of NBTI degradation is well known to follow an Arrhenius law [35]:

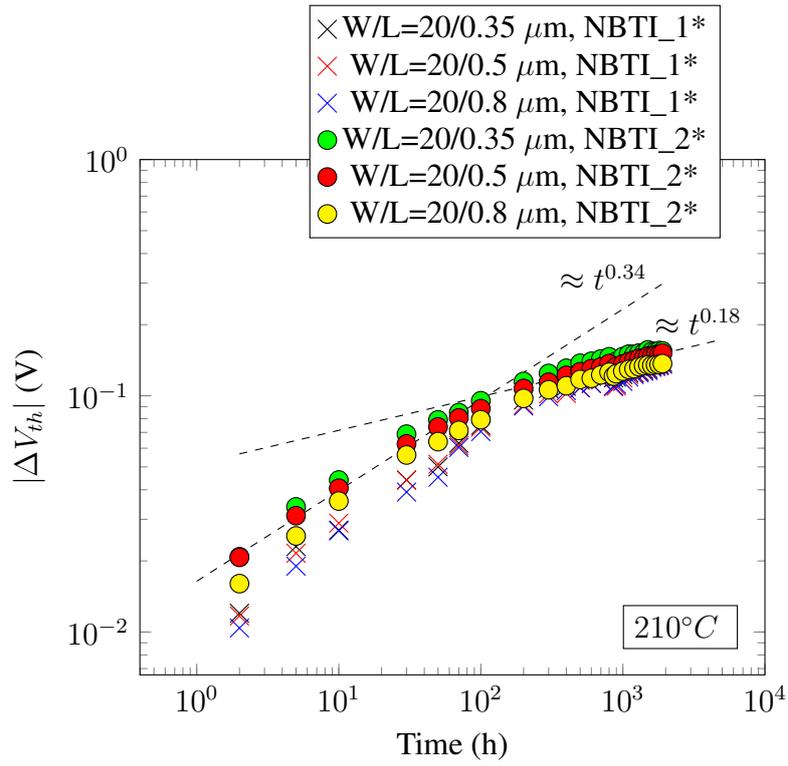
$$\Delta V_{th} \propto \exp\left(\frac{-E_a}{k_B T}\right) \quad (4.3)$$

where k_B is the Boltzmann constant, T is the stress temperature (in Kelvin), and E_a is the activation energy which was reported in the range of [0.06–0.08] eV [35], [0.1-0.2] eV [129], [130], [131], [132]. Our NBTI degradation results on 1.8V pMOS and 3.3V are following Arrhenius law with activation energy around [0.1 - 0.12] eV (Figure 4.6(b)).

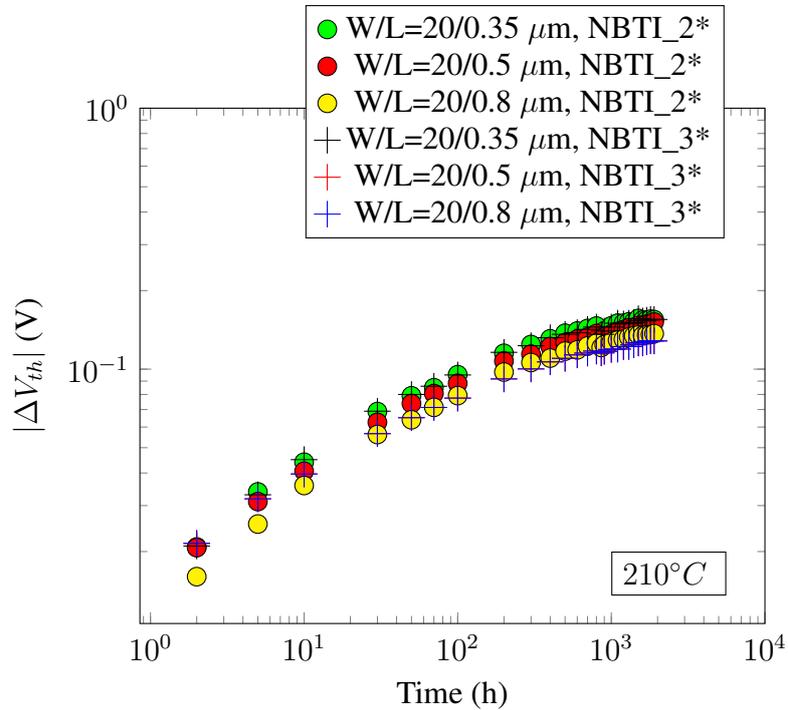
Our NBTI model based on stress time, oxide field, and temperature can be summarized into a compact analytic form that corresponds to the observations discussed above:

$$\Delta V_{th} \approx C \exp\left(\frac{-E_a}{k_B T}\right) \left(\frac{|V_g - V_{th}|}{t_{ox}}\right)^\gamma t^{n(T)} \quad (4.4)$$

where $n(T)$ implies the temperature dependence of the time exponent. When integrating NBTI model to the compact model, we choose n equals to 0.18 for T_{stress} higher than 200°C.

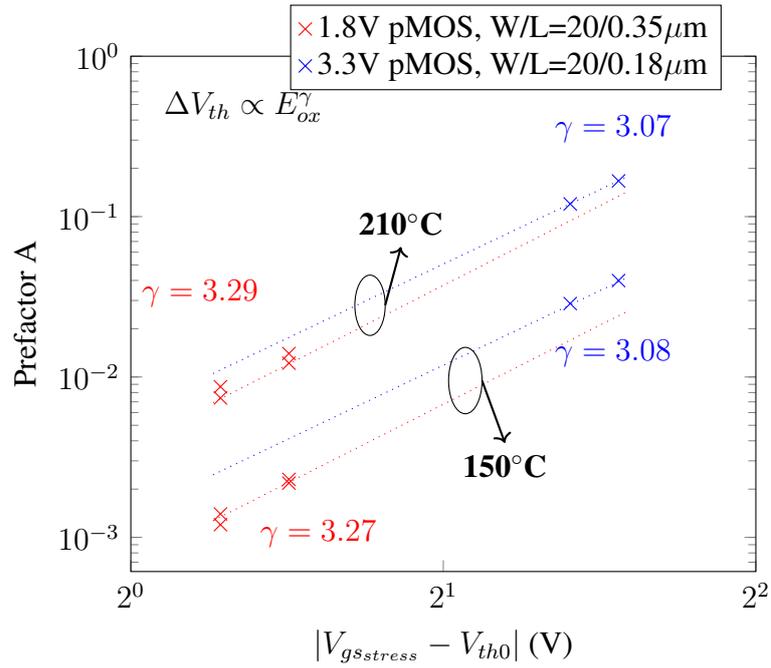


(a)

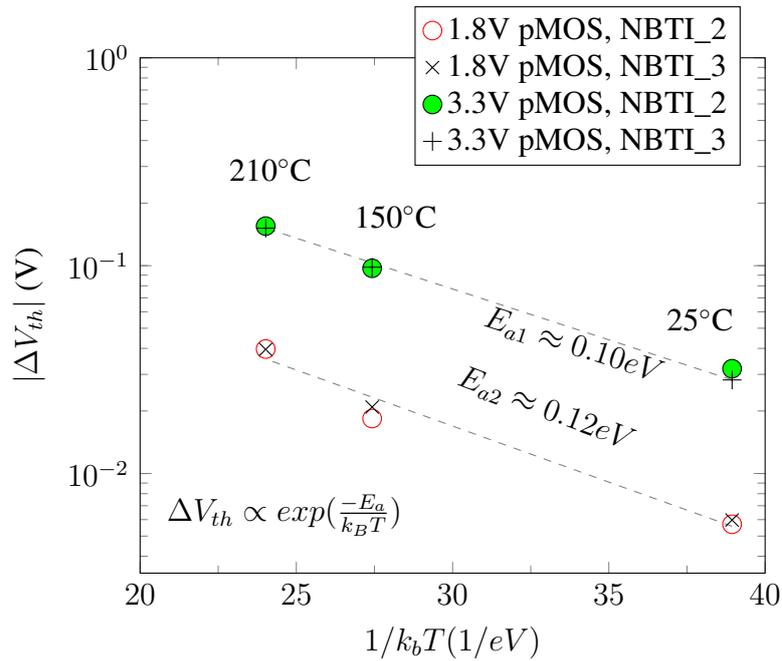


(b)

Figure 4.5: Measured NBTI-induced ΔV_{th} as a function of stress time under NBTI_1*, NBTI_2* (Figure (a)) and NBTI_2*, NBTI_3* (Figure (b)) at 210°C . Experimental data collected on W/L=20/0.35, 20/0.5 μm and 20/0.8 μm 3.3V pMOS.



(a)



(b)

Figure 4.6: The power-law prefactors A are fitted to a linear line with the applied electric field E_{ox} at 150°C and 210°C (Figure (a)). Temperature dependence of NBTI following Arrhenius law with activation energy $E_a=0.12\text{eV}$ and 0.1eV for 1.8V pMOS and 3.3V pMOS, respectively. Experimental data collected on $W/L=20/0.18\ \mu\text{m}$ 1.8V pMOS and $W/L=20/0.35\ \mu\text{m}$ 3.3V pMOS.

4.3.2 Positive Bias Temperature Instability (PBTI)

PBTI degradation in nMOS is usually neglected due to its limited impact. Our results after 2,000 hours stress show that PBTI degradation under 150°C show limited ΔV_{th} below 1.5%. However, PBTI becomes more pronounced at 210°C within the same stress period and bias conditions as the PBTI test at 150°C. PBTI degradation at 210°C also follows power-law with stress time and the prefactor A close to [0.01-0.02] and n close to 0.2 as shown in Figure 4.7.

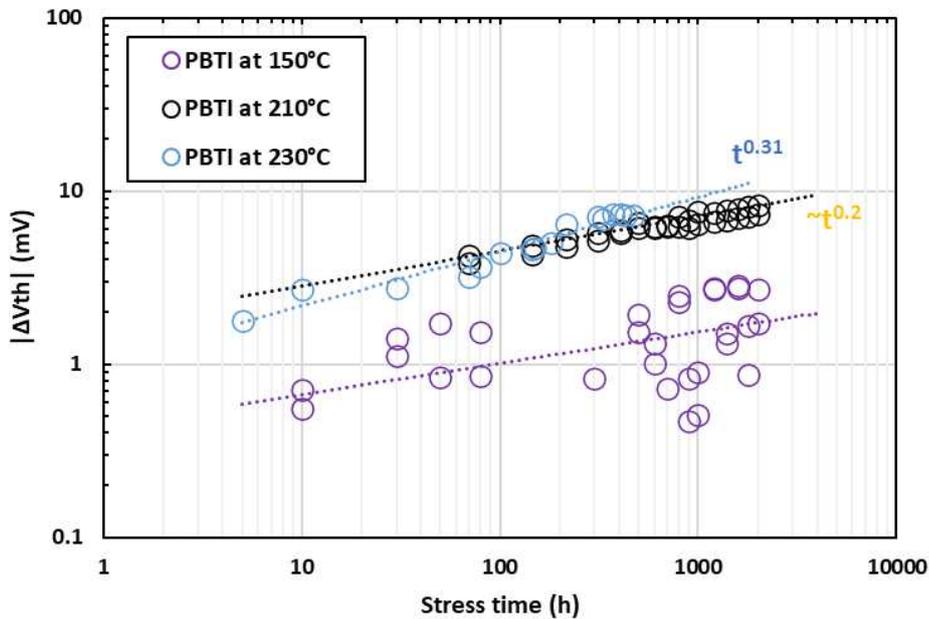


Figure 4.7: Threshold voltage shift ΔV_{th} associated with PBTI degradation under PBTI bias conditions at 150°C, 210°C and 230°C of W/L=20/0.18 μ m 1.8V nMOS.

4.4 Hot Carrier Injection Modelling

The body current is often considered as a criterion of HCI degradation. Therefore, the worst-case scenario is usually realized at DAHC bias conditions for which the maximum body current is obtained. With technology nodes lower than 0.1 μ m, the worst-case situation occurs at CHE/CHH bias condition ($|V_{gs}| \approx |V_{ds}|$) for both p- and n-channel [133].

Considering that the threshold energy Φ_B is 3.2 eV for electrons injected into the gate oxide [49], the HCI degradation has been assumed to occur since V_{dd} equal to 3.2V

is large enough. However, HCI degradation can be observed in advanced CMOS technologies with power supplies much lower than 3.2 V. Several mechanisms are responsible for heating up the channel carriers allowing hot carriers at low V_{dd} voltages injected into oxide layer: electron-phonon scattering (e-p), electron-electron scattering (e-e) and secondary impact ionization (II2) as discussed in Chapter 2. HCI degradation (both CHE and DAHC) is weakly dependent on the stress temperature [102], [103]. It has been reported that the HCI degradation in the case of the large gate length devices higher than $0.1\mu\text{m}$ increases when the temperature decreases, whereas the HCI in ultra-scaled devices becomes more serious at high temperature [133].

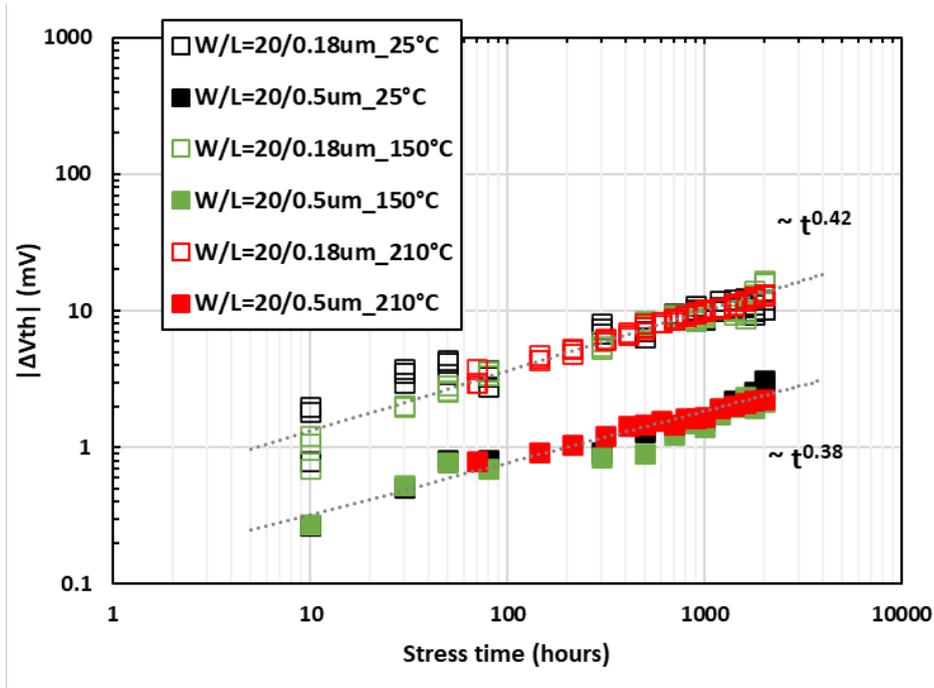
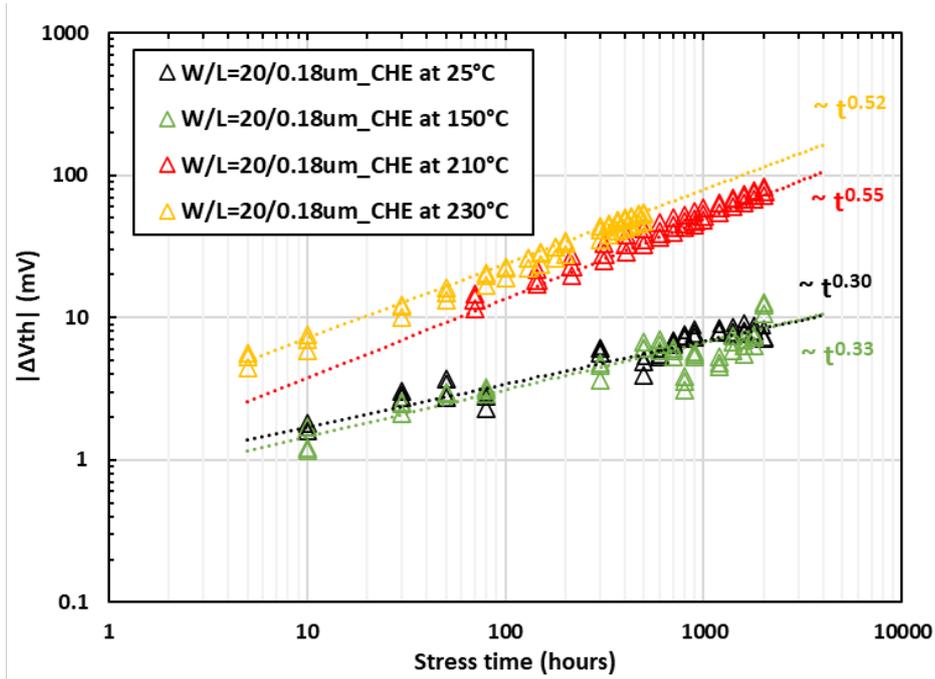
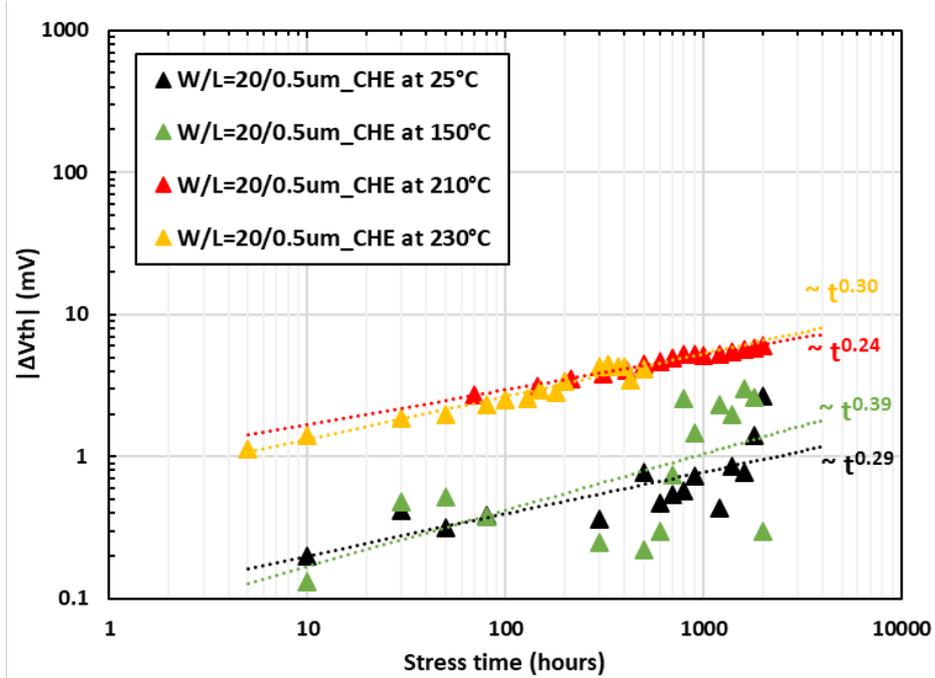


Figure 4.8: The threshold voltage shift ΔV_{th} under DAHC bias conditions at 25°C , 150°C , and 210°C of 1.8V nMOS. Experimental data collected on $W/L=20/0.18\mu\text{m}$ and $20/0.5\mu\text{m}$ 1.8V nMOS.

We performed both DAHC and CHE bias condition at 25°C , 150°C and 210°C . Like BTI, the threshold voltage shifts due to HCI also obey the power law with stress time. DAHC and CHE impact on V_{th} degradation are the same at 25°C and 150°C . However, CHE exceeds greatly DAHC at 210°C which was unforeseen. Figure 4.8 and Figure 4.9 present the threshold voltage shift due to DAHC and CHE mechanisms. According to their related



(a)



(b)

Figure 4.9: The threshold voltage shift ΔV_{th} under CHE bias conditions at 25°C, 150°C, and 210°C of 1.8V nMOS. Experimental data collected on (a) W/L=20/0.18 μm and (b) 20/0.5 μm of 1.8V nMOS.

power law values, DAHC exhibit poor relationship with temperature while CHE degradation becomes more and more serious at high temperature.

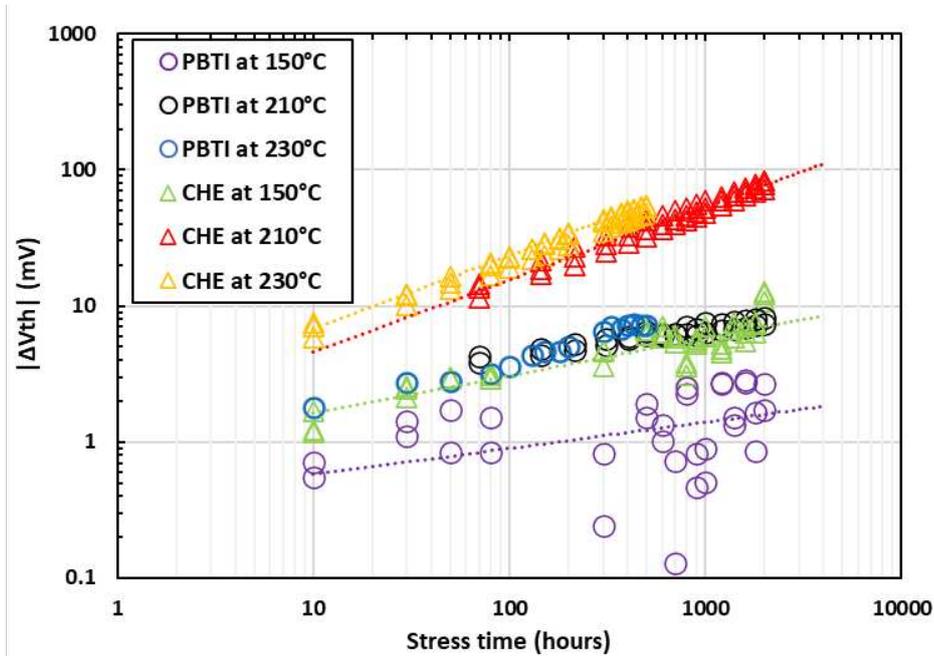


Figure 4.10: The threshold voltage shift ΔV_{th} under CHE and PBTI bias conditions at 150°C, 210°C and 230°C. Experimental data collected on W/L=20/0.18 μm 1.8V nMOS.

HCI degradation at extreme temperature (210°C) exhibits a complex behavior, which is the combination of PBTI and intrinsic CHE damage. Nevertheless, PBTI cannot support the entire CHE degradation at 210°C. According to our results, the magnitude of the V_{th} shifts at 210°C due to PBTI is rather small compared with the one caused by CHE (Figure 4.10). Therefore, we expected that CHE is strongly dependent on temperature when stress temperature exceeds a critical value where it is a complex combination of PBTI and other mechanisms (e-e, p-e, II2...). To investigate the temperature dependence of CHE, we conducted additional CHE aging tests at higher temperature above 230°C up to 500 hours as shown in Figure 4.9. We found an Arrhenius behavior with an activation energy is around 0.48 eV and we found that the critical temperature is around 150°C where it may activate other mechanisms (Figure 4.11).

Our HCI characterization on different transistor sizes (W/L=20/0.18 μm and 20/0.5 μm) presents an important dependence of the degradation according to the gate length. As shown

in Figure 4.8 and Figure 4.9, the smaller transistor exhibits larger threshold voltage shift which is in accordance with literature [133].

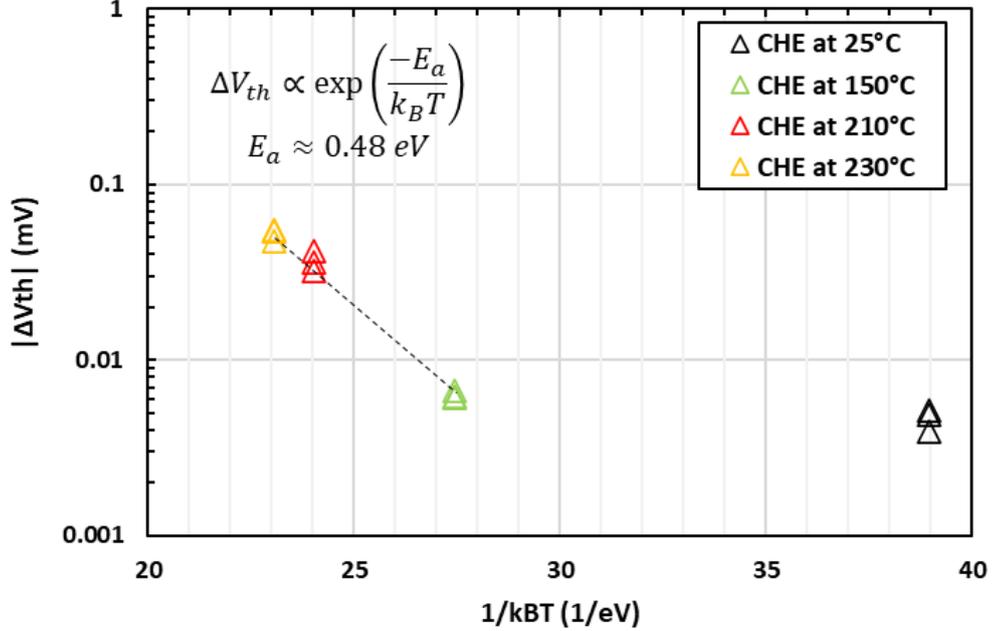


Figure 4.11: Temperature dependence of CHE following Arrhenius law with activation energy $E_a=0.48$ eV. Experimental data collected on $W/L=20/0.18$ μm 1.8V nMOS.

HCI in pMOS can be negligible since threshold voltage shift due CHH degradation is below 1% after 2,000 hours applying stress at 25°C as presented in Figure 4.12.

The most commonly HCI model was firstly proposed by [102] in which the device time-to-failed follows an exponential dependence on $1/V_d$. According to our results, we have slightly modified this model. Depending on the stress bias and temperature conditions, we proposed the model for nMOS degradation as follows:

i) For temperatures lower than 150°C, the gate voltage V_{gs} is greater than threshold voltage and lower than drain voltage V_{ds} ($V_{th} < V_{gs} \leq V_{ds}$):

$$\Delta V_{th} = C_1 \cdot \left(\frac{W}{L}\right)^m \cdot \exp\left(\frac{-\alpha}{V_{ds}}\right) t^n \quad (4.5)$$

For temperatures lower than 150°C, both CHE and DAHC are expected to be independent with temperature. $\alpha=1$, C_1 and m are fitted parameter extracted from the experiments.

ii) For temperatures greater than 150°C, the gate voltage V_{gs} is larger than drain voltage V_{ds} and great large than threshold voltage V_{th} ($V_{gs} \geq V_{ds} \gg (V_{th})$):

$$\Delta V_{th} = C_2 \cdot \left(\frac{W}{L}\right)^m \cdot \exp\left(\frac{-\alpha}{V_{ds}}\right) \cdot \exp\left(\frac{-E_a}{k_B T}\right) \cdot t^n \quad (4.6)$$

Above 150°C, CHE model integrates Arrhenius law, indicating the larger degradation at higher temperature as discussed above. $\alpha = 1$, $E_a = 0.48\text{eV}$. C_2 and m are fitted parameter extracted from the experiments.

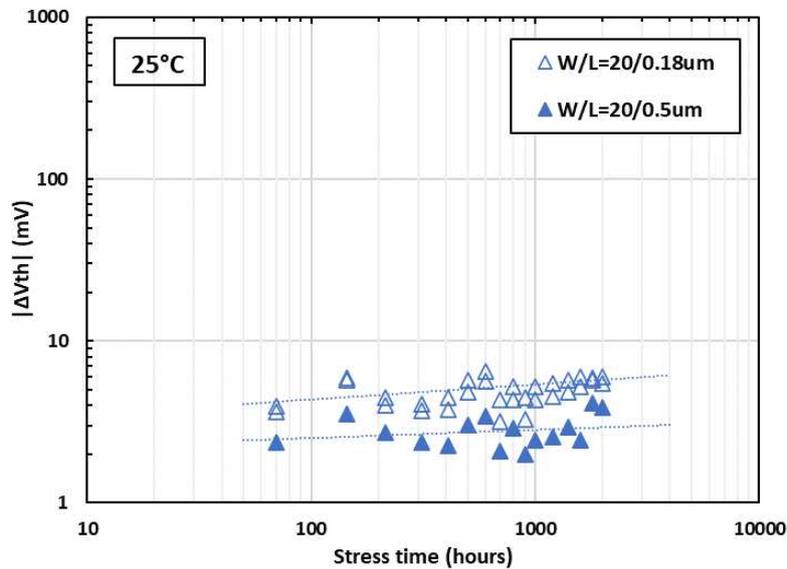


Figure 4.12: Threshold voltage shift ΔV_{th} associated with HCI degradation under CHH bias conditions at 25°C of the 0.18 μm and 0.5 μm 1.8V pMOS

HCI degradations in 3.3V MOSFETs are not as serious as NBTI even at extremely high temperature (210°C) as in Figure 4.13.

4.5 Conclusion

The above discussed experimental observations on 1.8V and 3.3V devices with several wear-out mechanisms can be summarized as:

(i) Both CHE and NBTI mechanisms are dominant at extreme temperatures above 200° for

1.8V transistors. DAHC and PBTI mechanisms are insignificant.

(ii) NBTI is a serious issue of 3.3V pMOS; while HCI can be negligible.

In summary, Figure 4.14 presents the competition among several degradation mechanisms for 1.8V and 3.3V MOSFETs. The reliability models have been established based on the experimental observations. The next chapter will present our approach to implement these aging models into the circuit simulator.

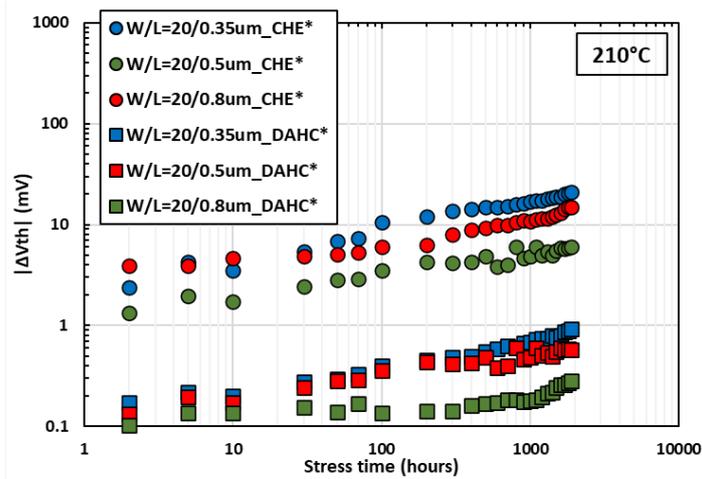


Figure 4.13: Threshold voltage shift ΔV_{th} associated with HCI degradation under CHE* and DAHC* bias conditions at 210°C of 3.3V nMOS. Experimental data collected on W/L=20/0.35, 20/0.5 and 20/0.8 μm 3.3V nMOS.

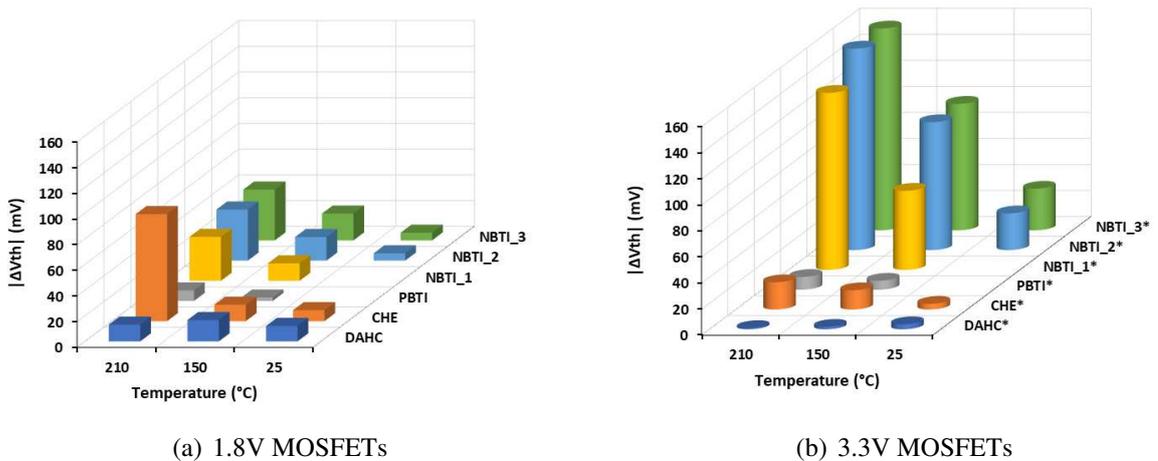


Figure 4.14: ΔV_{th} due to several wear-out mechanisms. Experimental data collected on W/L=20/0.18 μm 1.8V MOSFETs (Figure (a)) and on W/L=20/0.35 μm 3.3V MOSFETs.

5 | Integration of Aging Laws into circuit simulator

The previous chapter has introduced the mathematical equations for HCI/NBTI reliability models. In this chapter, we will focus on how to integrate these reliability models into a commercial software. First, a brief review of BSIM3v3 compact model for circuit simulation is presented. V_{th0} parameter in BSIM3v3 compact model is chosen to capture BTI/HCI degradation. After that, we introduce the Unified Reliability Interface (URI) which is an application program interface provided by Cadence that enable us to implement our reliability models into SPECTRE[®]. Then, we explain in detail the implementation procedure of the aging laws into SPECTRE[®]. The simulator embedded aging laws has the ability to predict aging behaviors of a circuit over time. This implementation is a preliminary step to develop a reliability tool for future ASIC designs in Schlumberger.

5.1 BSIM3v3 introduction

Along with the non-stop development of VLSI, circuit simulators (principally SPICE) have been considered as a necessary tools for circuit design to optimize performance and verify functionalities of circuits. Several commercial softwares such as SPECTRE[®] (Cadence[®]), SPICE (MicroSim), ELDO (Mentor Graphics), SSPICE (Silvaco) are widely employed SPICE for circuit simulations. The accuracy of the simulators is strongly dependent on the accuracy of the included device models. So far, device models have been divided into three categories: table lookup models [134], [135], numerical models [136], [137] and compact models, however, table lookup models and numerical models are less feasible for circuit simulator than compact models [138], [139].

Compact models are mathematical equations of discrete elements (diodes, resistors, capacitors) connected to describe complex behaviors of the device in the circuit. They are mainly based on physics and are commonly used in today's simulators. Since the 1970s, hundreds of MOSFET compact models have been reported [140] and integrated into some

circuit simulators. At that time, many large semiconductor companies were in the race to develop their transistor compact model. Therefore, most of the existing compact models were confidential and proprietary; just a tiny number that was released for free are well-known and widely used. Some compact models such as MOS1, MOS2, MOS3, BSIM1, BSIM2, BSIM3, BSIM4 were popular thanks to free source code licenses and can be downloaded freely. This chapter will focus on BSIM3v3 compact model, which has been widely used by industry for the 0.5, 0.35, 0.25, and 0.18 μm MOS technology nodes.

BSIM stands for Berkeley Short Channel IGFET Model. BSIM1 model was released for MOSFET 1 μm (and above) by Device Group at University of California (Berkeley) in 1987. This model introduced many fitting parameters (which did not have any physical meaning) for each model parameter to improve the model scalability, however, the accuracy of the model was not totally satisfying [141]. Furthermore, the channel length of MOSFETs has been continuously scaled down over years, raising challenges for device modelling. The appearance of new physical mechanisms in scaled devices forced BSIM to be extensively modified. As a result, compact model BSIM3v3 (BSIM3 version 3) was released in 1995 with significant improvements from BSIM1, BSIM2, and BSIM3v2 [142]. Table 5.1 provides the performance comparison of these models.

Model	Min L(μm)	Min T_{ox} (nm)	Model continuity	I_d accuracy in strong inversion	I_d accuracy in sub-threshold	Small signal parameter	Scalability
MOS1	5	50	Poor	Poor	Not modeled	Poor	Poor
MOS2	2	25	Poor	Poor	Poor	Poor	Fair
MOS3	1	20	Poor	Fair	Poor	Poor	Poor
BSIM1	0.8	15	Fair	Good	Fair	Poor	Fair
BSIM2	0.35	7.5	Fair	Good	Good	Fair	Fair
BSIM3v2	0.25	5	Fair	Good	Good	Good	Good
BSIM3v3	0.15	4	Good	Good	Good	Good	Good

Table 5.1: Performance comparison of several compact models [140]

BSIM3v3 compact model is the physics-based, deep-submicron MOSFET model for circuit designs. It includes analytical equations to present the complex behaviour of the

transistor drain current, I_{ds} , as a function of gate voltage V_{gs} , drain voltage V_{ds} , body voltage V_{bs} , and geometries (width, length). These model equations contain several effects observed in modern MOS devices, i.e, short and narrow channel effects on threshold voltage, channel length modulation, velocity saturation, bulk charge effect, self-heating, subthreshold conduction, and so on [142]. In 1997, the Compact Model Council (CMC) ¹ selected BSIM3v3 as the international first standard transistor model for IC simulation. Since then, it has been becoming popular in semiconductor industry.

5.2 Optimization of BSIM3v3 parameter for reliability simulation

It is well accepted that BTI and HCI induced physical damage impacts to channel mobility (μ_0) and flatband voltage (V_{FB}), which in turn affect key MOSFET model parameters such as linear (I_{dsLIN}), saturation (I_{dsSAT}) drain current and threshold voltage (V_{th}) [143], [144], [145], [146]. Therefore, to replicate the transistor failures, it is commonly adapted to tune many parameters in SPICE level simulations to predict it, which also varies from technology node to fabrication as well. According to [147] and [148], several BSIM parameters were modified to capture the aging behaviour such as V_{th0} (long-channel threshold voltage at zero substrate bias), μ_0 (low-field carrier mobility), v_{sat} (saturation velocity), and r_{dsw} (parasitic resistance per unit width). In [149], A_{gs} (gate bias coefficient of the bulk charge effect) and D_{sub} (Drain-Induced Barrier Lowering (DIBL) coefficient exponent in subthreshold region) were also taken into account to describe aging effects. In [150], seven parameters in original BSIM3v3 source code were tuned to simulate the impact of HCI, i.e, V_{th0} , K_1 (the first-order body-effect factor), μ_0 , μ_c (body-effect coefficient of mobility-degradation), A_0 (channel-length dependency parameter of the bulk charge effect), A_{gs} , and K_{eta} (body-bias coefficient of the bulk charge effect). Therefore, the aging behaviours have been considered to be very subjective and difficult to predict.

Based on our aging experimental results, the transistors suffer from a large deviation

¹CMC is a collaborative group in the Electronic Design Automation industry focused on the standardization of SPICE models

a large degradation in saturation regime. Threshold voltages primarily affected by BTI and HCI were extracted using ESR method (section 3.4.4). We have investigated the dependency of several BSIM3v3 model parameters on the electrical output characteristics to determine the primary parameters that are affected due to the aging effect. In our case, we found that the threshold voltage shift defined in BSIM3v3 is enough to reproduce HCI/BTI degradation. Hereafter, we will discuss about several important BSIM3v3 model parameters and their close relationship with threshold voltage (V_{th}), illustrating the major role of V_{th} to the output characteristics shift due to aging.

Threshold Voltage Model

Accurate modeling of threshold voltage (V_{th}) is one of the critical requirements for proper simulation of device characteristics. V_{th} can be used as a reference point to distinguish different device's operation regimes. If $|V_{gs}| > |V_{th}|$, the device is operating in the strong inversion regime and the drift current is dominant. If $|V_{gs}| < |V_{th}|$, the device is in weak inversion (subthreshold) regime and the diffusion current becomes dominant. If $|V_{gs}| \approx |V_{th}|$, the device operates in the transition regime where diffusion and drift current are equal. In order to quantify BTI and HCI degradation, the shift of the threshold voltage ΔV_{th} is often used since it represents the impact of charged defects in the gate oxide and at the interface on the transistor [143], [146].

The threshold voltage of a MOSFET for long channel length/width and uniform doping concentration is given as [142]:

$$V_{th} = V_{FB} + \phi_s + \gamma\sqrt{\phi_s - V_{bs}} = V_{th0} + \gamma(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) \quad (5.1)$$

where V_{FB} is the flat band voltage, V_{bs} is the body bias, ϕ_s is the surface potential, V_{th0} is the ideal threshold voltage at zero volt substrate bias, and γ is the substrate bias effect coefficient.

When the gate length of the device is scaled below $1\mu\text{m}$, the threshold voltage expression includes several physical effects such as vertical non uniform effect, lateral non uniform doping effect, short channel effect, and narrow channel effect. It can be summarised as:

$$\begin{aligned}
 V_{th} &= V_{th0} + V_{vertical-non-uniform-effect} \\
 &+ V_{lateral-non-uniform-doping-effect} \\
 &- V_{short-channel-effect} \\
 &- V_{narrow-channel-effect} \\
 &= V_{th0} + K_1(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}) - K_2 V_{bseff} \\
 &+ K_1 \left(\sqrt{1 + \frac{N_{LX}}{L_{eff}}} - 1 \right) \sqrt{\phi_s} + (K_3 + K_{3b} V_{bseff}) \frac{T_{ox}}{W_{eff} + W_0} \phi_s \\
 &- D_{VT0w} \left(\exp\left(-D_{VT1w} \frac{W_{eff} L_{eff}}{2l_{tw}}\right) + 2 \exp\left(-D_{VT1w} \frac{W_{eff} L_{eff}}{l_{tw}}\right) \right) (V_{bi} - \phi_s) \\
 &- D_{VT0} \left(\exp\left(-D_{VT1} \frac{L_{eff}}{2l_t}\right) + 2 \exp\left(-D_{VT1} \frac{L_{eff}}{l_t}\right) \right) (V_{bi} - \phi_s) \\
 &- \left(\exp\left(-D_{sub} \frac{L_{eff}}{2l_{t0}}\right) + 2 \exp\left(-D_{sub} \frac{L_{eff}}{l_{t0}}\right) \right) (E_{tao} + E_{tab} V_{bseff}) V_{ds} \tag{5.2}
 \end{aligned}$$

Refer to [142] for detailed explanations of Equation (5.2) and related physical effects. Vertical non-uniform doping effect is related to vertical doping concentration which is gradually decreasing with the depth of the substrate. Lateral non-uniform doping effect is referred to lateral doping concentration which is higher in the region near drain/source than in the middle of the channel. As channel length shrinks, the lateral doping concentration is higher leading to the threshold voltage increase. The short channel effect and narrow channel effect are phenomenon related to feature size (length and width) and drain voltage. Therefore, these effects mentioned above cannot be affected by wear-out mechanisms. The shift of V_{th} in Equation 5.2 due to aging can be inferred from the shift of flatband voltage V_{FB} , which in turn leads to the shift of V_{th0} .

Mobility model

Surface carrier mobility is one of the important parameters of BSIM compact model which depends on process parameters and bias conditions, such as gate oxide thickness, doping concentration, threshold voltage V_{th} , gate voltage V_{gs} ,... The unified equation of mobility is

given by:

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff}/E_0)^\nu} \quad (5.3)$$

$$E_{eff} \approx \frac{V_{gs} + V_{th}}{6T_{ox}} \quad (5.4)$$

where T_{ox} is the gate oxide thickness. E_{eff} is considered as the average electrical field in the inversion regime. μ_0 , E_0 and ν are obtained from experiment and they have different values for channel electrons and holes. Equation 5.3 and 5.4 show the close relationship between V_{th} and μ_{eff} .

Carrier drift velocity

According to semiconductor physics, the velocity of charged carriers is directly proportional to the electric field for values lower than the critical field, and the proportionality constant is referred to as the carrier mobility. However, if the electric field is increased beyond a particular value where velocity is saturated, the charged carrier's velocity does not change in response to the electric field anymore [151]. In BSIM3v3, carrier drift velocity model is a semi-empirical saturation velocity model as follows:

$$\begin{cases} v = \frac{\mu_{eff}E}{1 + (E/E_{sat})}, & (E < E_{sat}) \\ v = v_{sat}, & (E > E_{sat}) \end{cases} \quad (5.5a)$$

$$\quad (5.5b)$$

where E is the electric field, $E_{sat} = (2v_{sat})/\mu_{eff}$ is a critical field value. The carrier drift velocity is related to μ_{eff} , therefore, the change in V_{th} due to degradation can indirectly impact the carrier drift velocity.

Drain current model

The current equation for both linear and saturation current is given as:

$$I_{ds} = \frac{I_{dso}(V_{dseff})}{1 + \frac{R_{ds}I_{dso}(V_{dseff})}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right) \quad (5.6)$$

where

$$V_{dseff} = V_{dsat} - \frac{1}{2}(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}) \quad (5.7)$$

$$V_{dsat} = \frac{E_{sat}L(V_{gsteff} + 2v_t)}{A_{bulk}E_{sat}L + V_{gsteff} + 2v_t} \quad (5.8)$$

I_{ds0} is the intrinsic current, R_{ds} is a variable representing the influence of the parasitic resistances at the source and drain. V_{dseff} is the effective drain voltage, V_A is the Early Voltage. V_{ASCE} is the early voltage due to the substrate current induced body effect and it is a strong function of V_{ds} . A_{bulk} is a parameter accounting for the bulk charge effect. E_{sat} is proportional with μ_{eff} . Therefore, in the case of a threshold voltage V_{th} degradation due to the wear-out, drain current will decrease correspondingly.

5.3 Unified Reliability Interface Introduction

Due to the demand for high reliability of the sub-micron semiconductor technologies, many Electronic Design Automation (EDA) vendors have offered some built-in degradation models based on SPICE simulation. Several reliability simulation tools are available such as BERT (University of California, Berkeley), MOSRA (Synopsys), ELSO-UDRM (Mentor Graphics), PRESTO (NXP semiconductors) and RelXpert (Cadence). However, it is challenging to validate their model accuracy for each given semiconductor technology. Because there are no standard transistor degradation models, aging simulations from different EDA vendors can obtain different results for the same technologies under the same aging conditions. For this reason, besides developing built-in models, EDA vendors also provide an Application Program Interface (API), allowing users to embed their degradation models into the circuit simulator.

At Schlumberger, Cadence's products are used to design and simulate circuits. Cadence's solution Unified Reliability Interface (URI) offers the possibility to create user-defined reliability models and integrate them into a simulator which can be SPECTRE[®],

SPECTRE[®] Accelerated Parallel Simulator (APS) or RelXpert. SPECTRE[®] simulator is used in the scope of this work. As its name indicated, URI is an interface that provides means for implementing the reliability models and interacting with Cadence's simulator.

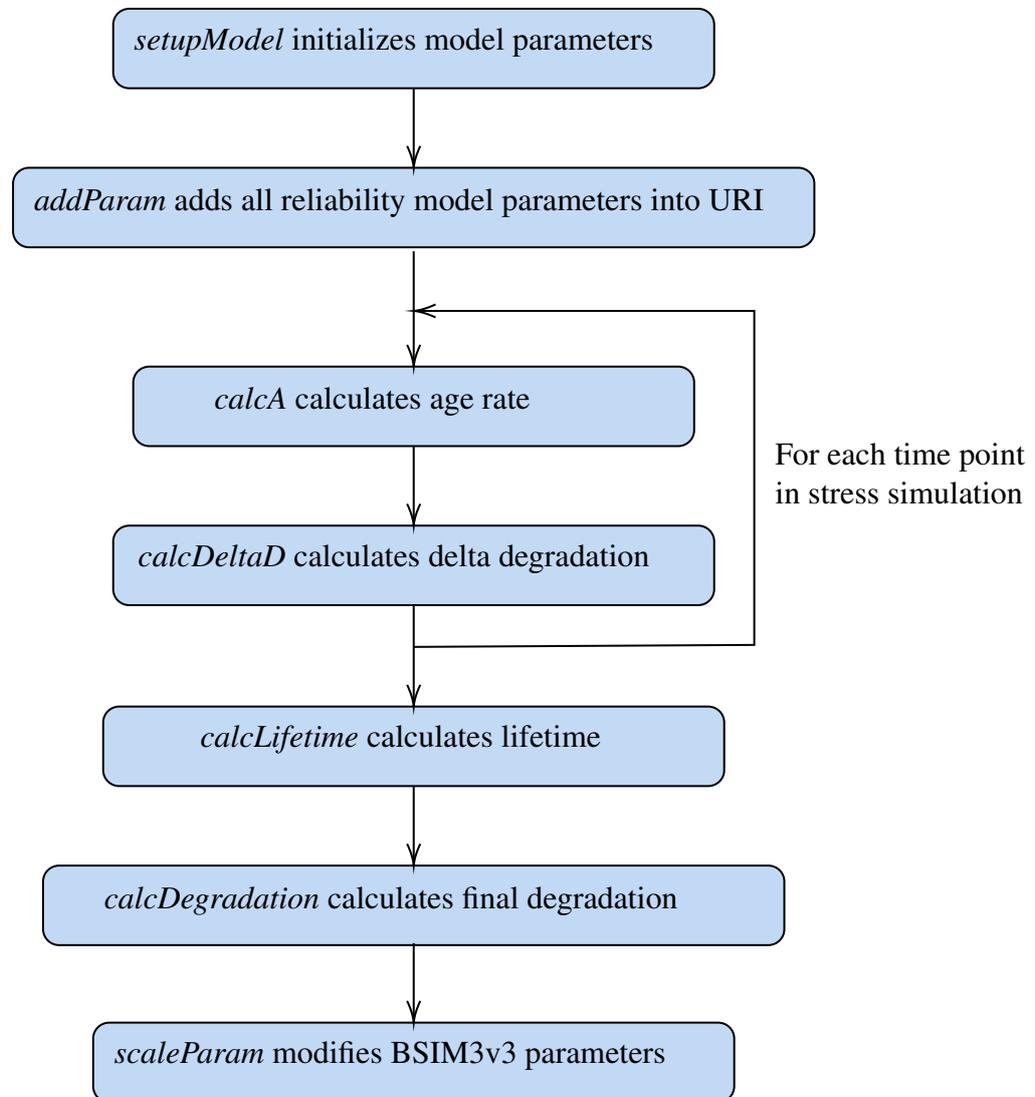


Figure 5.1: URI Call Sequence

Our reliability models have been integrated successfully into SPECTRE[®] simulator allowing to modify BSIM3v3 model parameters due to the aging effect. It has been done with URI by writing a C or C++ dynamic library, called URI library. We used C language to write this library, and the whole code for implementation of aging laws can be found in [Appendix B](#). The URI library contains required functions for reliability simulation, i.e, function

calcA for age rate calculation, *calcDeltaD* calculates delta degradation up to the simulation time in the transient time period, *calcDegradation* for degradation calculation at a specified future time, and *calcLifetime* for lifetime estimation. These functions can be identified and called by the SPECTRE[®] simulator during a reliability simulation. The URI call sequence is described in the Figure 5.1. When a reliability simulation is run, SPECTRE[®] simulator first loads the URI library and initializes reliability model's parameters for each transistor using *setupModel* and *addParam* functions. Then, a stress simulation (see details in 5.4.1), which is a transient analysis, is run. The functions *calcA* and *calcDeltaD* compute the age rate and degradation respectively due to HCI/NBTI at every time step of the transient analysis. The device's lifetime and final degradation are calculated by *calcLifetime* and *calcDegradation* functions. Finally, by using the function *scaleParam* URI library modifies BSIM3v3 parameter based on the calculated degradation.

One of the difficulties that we faced during the implementation of the reliability models was the limited access to BSIM3v3 parameters through URI. This limitation is due to Cadence's performance concern and to reduce the memory usage. For example, the NBTI degradation are modeled as Equation 5.9. It depends on the initial value of the threshold voltage, V_{th0} , which is a BSIM3v3 parameter. Since V_{th0} cannot be retrieved while running the reliability simulation, we introduced an additional reliability model parameter *rel_Vth0*. Similar to other reliability model parameters (e.g: C , γ , n ,...), *rel_Vth0* is defined in model card and is read at the beginning of reliability simulation. *rel_Vth0* is just an duplicate of V_{th0} . However, V_{th0} has different values depending on the device geometry (gate width and length), so selecting the correct value of V_{th0} for each device is difficult, especially in a circuit with hundreds of transistors with different sizes. This selection needs to be done automatically.

$$\Delta V_{th0} \approx C \exp\left(\frac{-E_a}{k_B T}\right) \left(\frac{|V_{gs} - V_{th0}|}{t_{ox}}\right)^\gamma t^{n(T)} \quad (5.9)$$

To overcome this obstacle, we have to add *if..else* conditional statement to the model card based on device's dimensions. In that way, we can get the right value of V_{th0} corresponding to different device's geometry and run the NBTI reliability simulation without accessing directly BSIM3v3 model parameters. Here is an example of the selection of V_{th0} :

```
simulator lang=spectre
parameters vth0_select=0
subckt nei (d g s b)
...
if ( 2.09e-007 <= w && w <= 5e-007 && 1.8e-007 <= 1 && 1 <= 5
    e-007){
parameters vth0_select = 0.59486757
}
if ( 2.09e-007 <= w && w <= 5e-007 && 5e-007 <= 1 && 1 <=
    0.000200001){
parameters vth0_select = 0.59856139
}
if ( 5e-007 <= w && w <= 0.000200001 && 1.8e-007 <= 1 && 1 <=
    5e-007){
parameters vth0_select = 0.68878118
}
if (5e-007<= w && w <= 0.000200001 && 5e-007 <= 1 && 1 <=
    0.000200001){
parameters vth0_select = 0.58895269
}
ends nei
*relxpert: .agemodel neimod agelevel=104
...
*relxpert: +rel_vth0      = vth0_select
```

5.4 Reliability simulation with SPECTRE®

The Figure 5.2 depicts all the steps in a reliability simulation with SPECTRE®. Netlist, SPICE models, and the reliability models created with URI are required for this simulation.

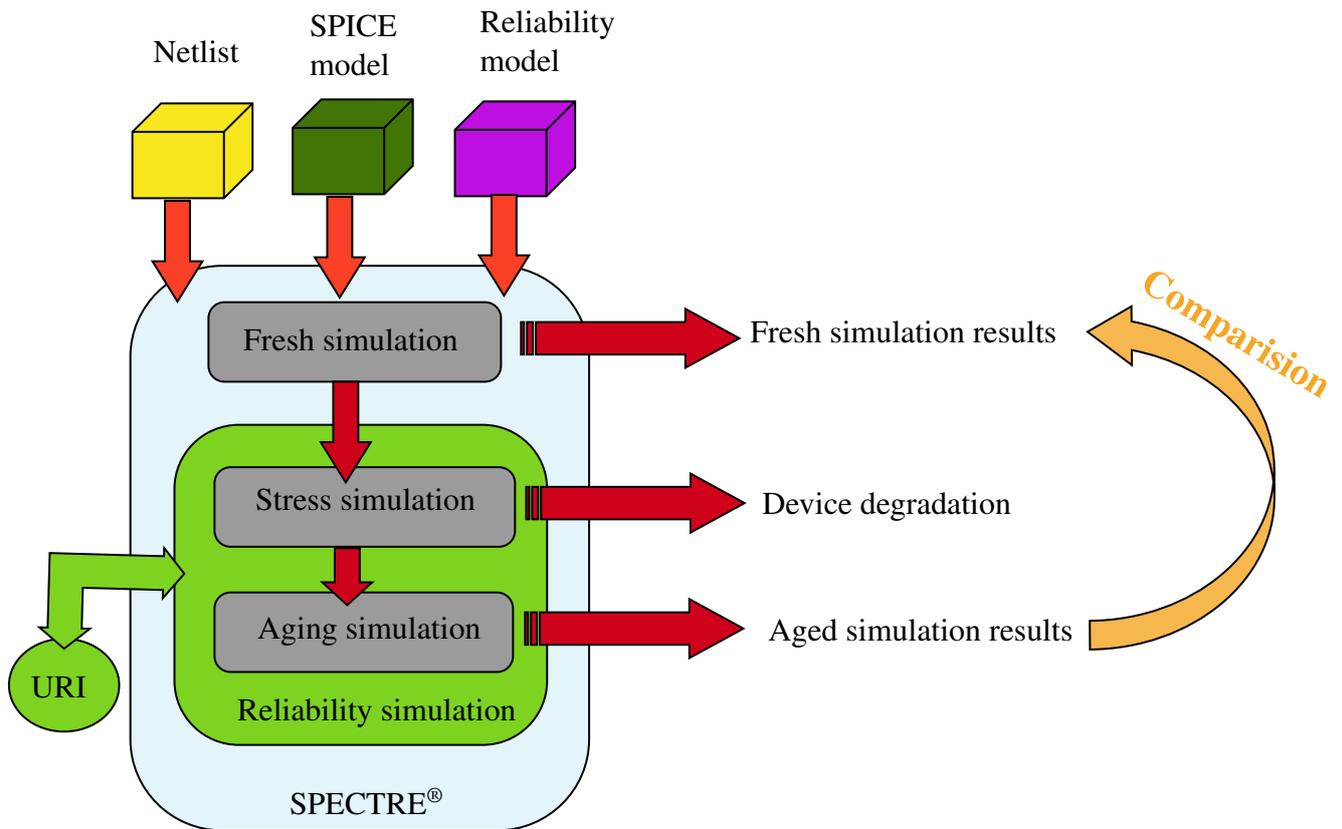


Figure 5.2: Reliability simulation with URI

First, a "fresh" simulation is run. The result of the "fresh" simulation is considered as an original/fresh state of devices. Next, a stress simulation is run to apply the stress conditions and calculate the degradation. Next, an aging simulation is carried out by applying the degradation calculated during the stress simulation. Finally, the "aging" simulation results can be compared to the fresh simulation to estimate the characteristic drift due to the aging effect. The relationship among fresh simulation, stress simulation and aging simulation is presented in Figure 5.3.

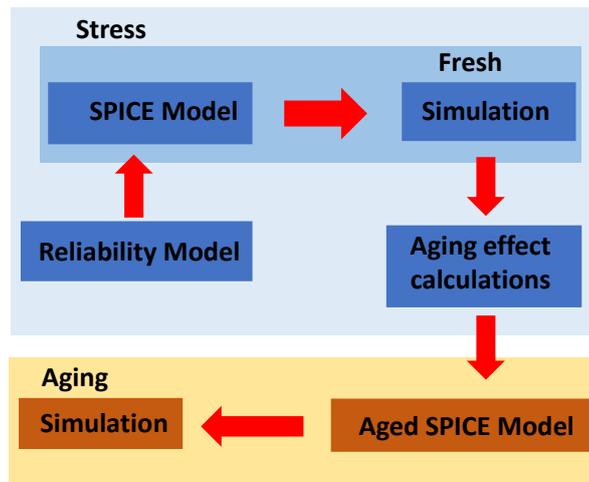


Figure 5.3: Relationship between the fresh simulation, stress simulation, and aging simulation.

5.4.1 Reliability block

For running a reliability simulation with SPECTRE®, a reliability block needs to be defined in the netlist. It composes a group of syntax to instruct SPECTRE® how to run the reliability simulation. More precisely, it contains control statements, stress simulation statements and aging simulation statements:

- **Reliability control statements:** used to control how the simulation behaves, for example: defining the time at which we want to calculate degradation (aging time), the devices which will be included/excluded from the reliability simulation, the path where the reliability URI library can be found, ...
- **Stress statements:** used to define a stress simulation. The bias conditions in this simulation are used to calculate the degradation. If we want to use the reliability simulation to foresee the behaviors of a circuit in N years (aging time), the stress conditions need to be closed to the actual operating condition applied to the circuit. This is because we can only run the stress simulation in a small amount of time (t_{sim}), and the degradation calculated during simulation time will be used to extrapolate the degradation after N years. Hence, the choice of the stress simulation is important and will affect the degradation result.

- **Aging statements:** used to define an aging simulation. Similarly to stress simulation, aging simulation or post-stress simulation is a transient analyse. SPECTRE® simulator applies the degradation at aging time to BSIM3v3 parameters then run a simulation. The result of this simulation can be used to compare with the fresh simulation, for which circuit is not degraded.

An example of reliability block embedded in a circuit netlist is shown bellow:

```
// Reliability block
my_rel_block reliability {

// Control Statements
age time=[1y]
deltad value = 0.1
uri_lib file = "../libURI.so" debug = 1 uri_mode=scaleparam
report_model_param value = yes

// Stress Statements
tran_stress tran stop=100ns param=Vds param_vec=[0ns 2 100ns
  2] param_step=1ns

// Aging Statements
tran_aging tran stop=100ns param=Vds param_vec=[0ns 0 100ns
  1.8] param_step=1ns
}
```

5.4.2 Reliability Graphical User Interface

There are two ways to run a reliability simulation. The first is creating reliability block directly in netlist which is a flexible way to configure and run reliability simulations with SPECTRE®. The second one is using Graphical User Interface (GUI) provided by Cadence. This approach can be done through Cadence Virtuoso Analog Design Environment (ADE). In ADE, reliability simulation can be chosen as Figure 5.4. Then, aging time, path to URI library, choice of simulator and other parameters can be configured as shown in Figure 5.5. Comparing to reliability block example in Section 5.4.1, these configurations are equivalent to the reliability control statements in the netlist. Since reliability model parameters, or fitted parameters, are read from model card, we need to add those parameters to model card and indicate path to these files, see Figure 5.6. An example of reliability simulation results is shown in Figure 5.7.

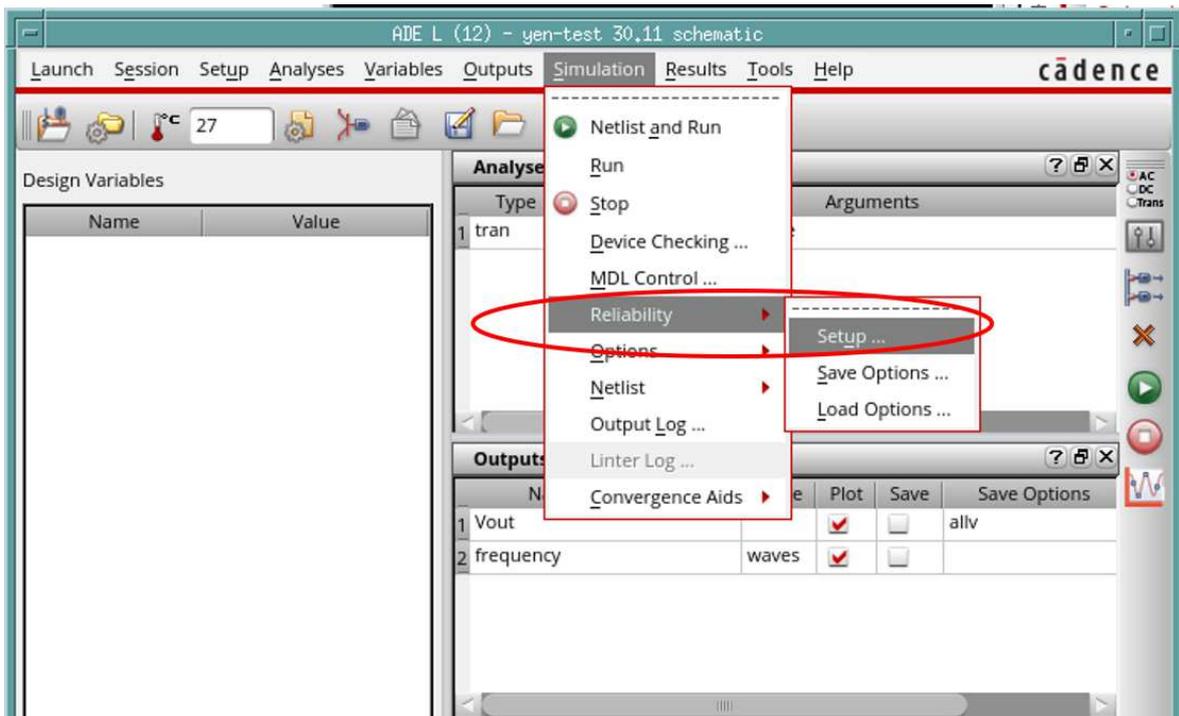


Figure 5.4: Reliability simulation with GUI

5.4. RELIABILITY SIMULATION WITH SPECTRE®

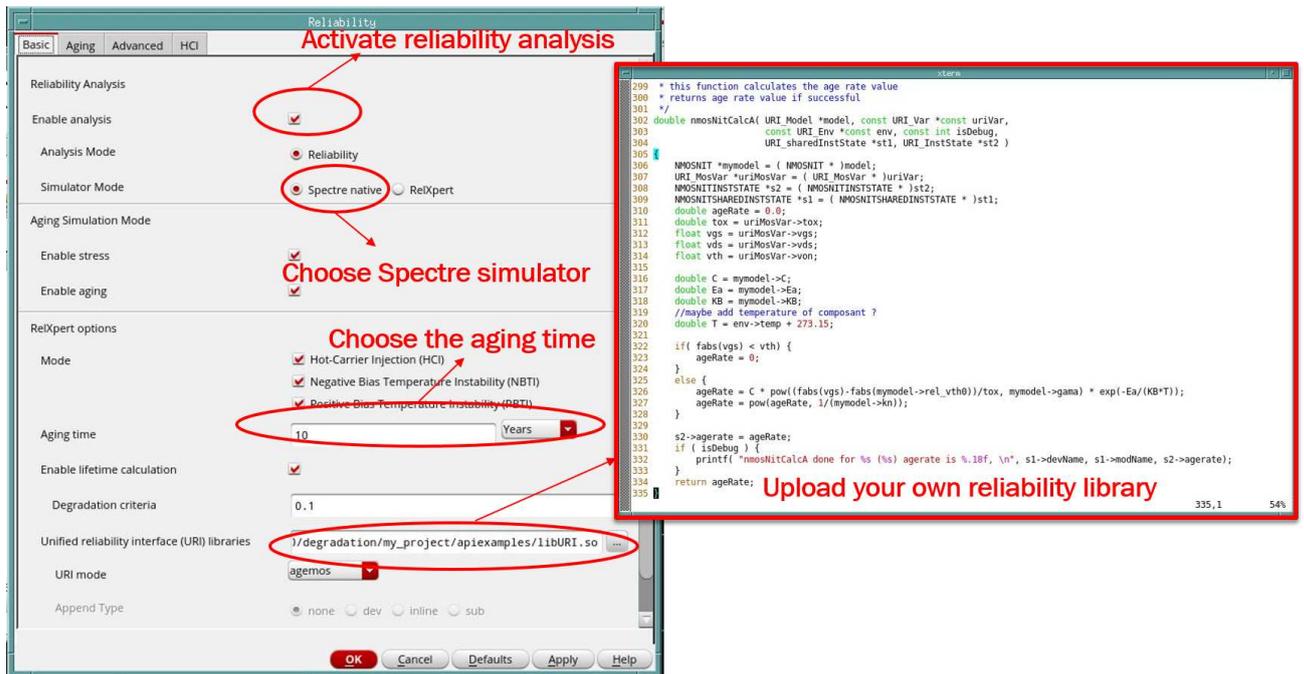


Figure 5.5: Configuration for reliability simulation with GUI

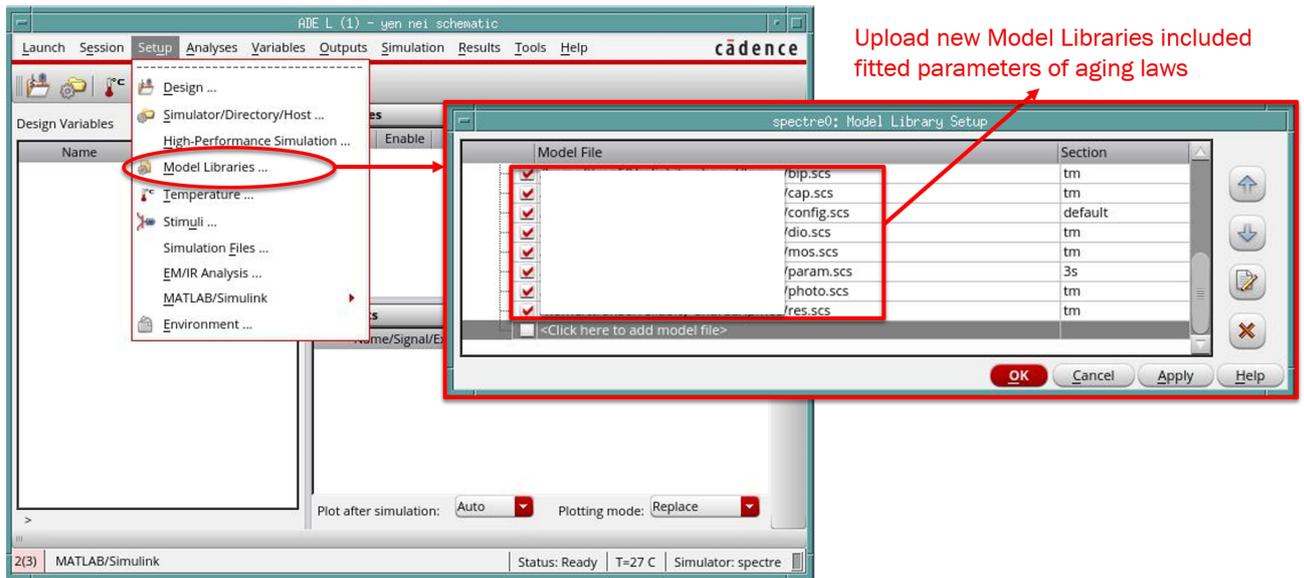


Figure 5.6: Configuration for reliability simulation with GUI

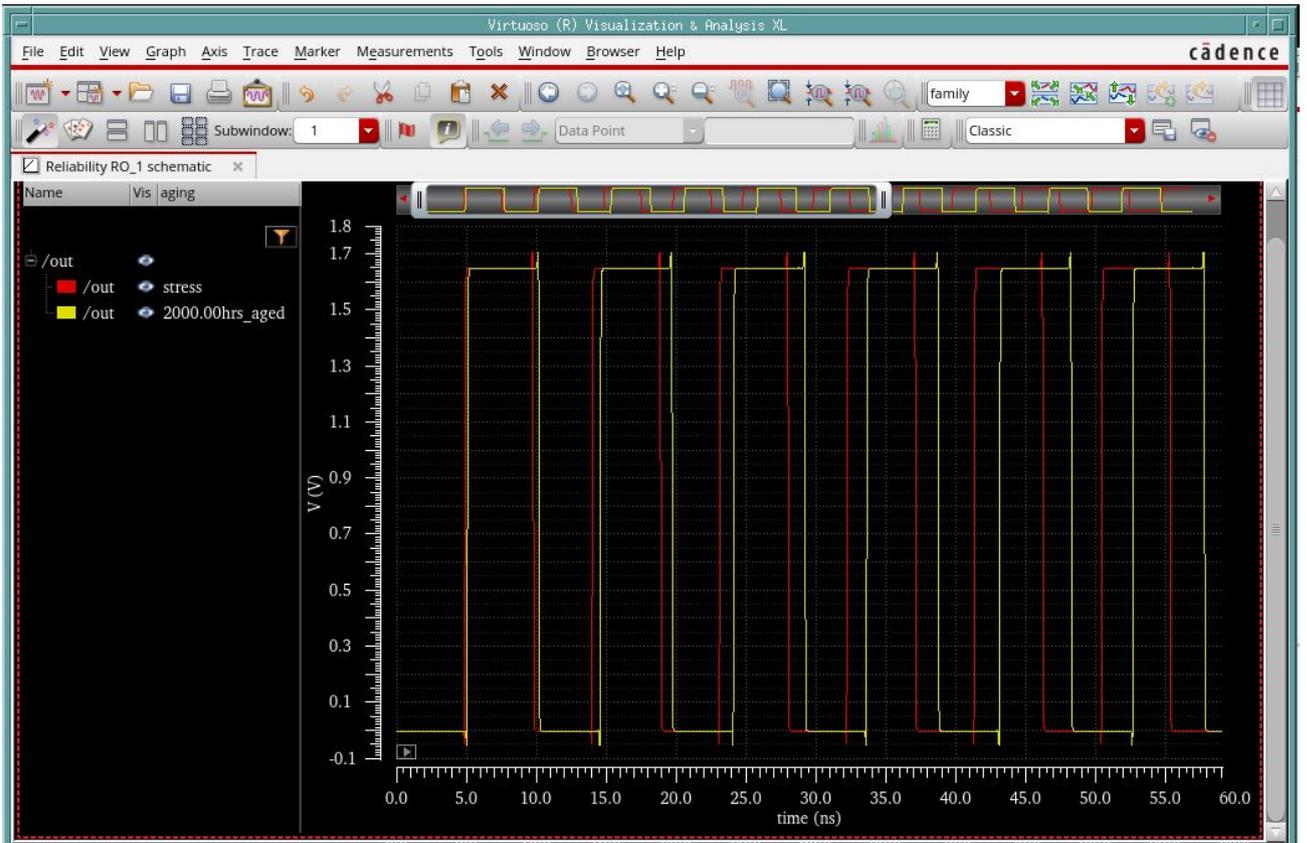


Figure 5.7: Fresh simulation (red line) and aging simulation result (yellow line) of a Ring Oscillator after 2,000 hours applying stress at 235°C.

5.5 Implementing aging-law equations

5.5.1 Degradation during stress simulation

Both our HCI and NBTI degradation models followed the time power law, t^n :

$$\Delta D(t) = A \times t^n \quad (5.10)$$

where D stands for Degradation, A is a function of bias conditions, device geometries,...

$$A = f(V_{ds}, V_{gs}, W, L, \dots) \quad (5.11)$$

During our aging test, a set of DC bias conditions is applied to the transistors, and it's unchanged over time. However, in circuit simulation, we need to have the possibility of running

simulations that represent a dynamic conditions of the circuit in reality. In other words, bias conditions of stress simulation are time-varying parameters. In order to satisfy this requirement, we have added time t as a parameter of A , it means:

$$A = f(V_{ds}, V_{gs}, W, L, t, \dots) \quad (5.12)$$

We can rewrite the degradation equation using the quasi-static approximation [152]:

$$\Delta D(t_{sim}) = A \cdot t_{sim}^n \quad (5.13)$$

$$\Delta D(t_{sim}) = (B \cdot t_{sim})^n = \left[\int_0^{t_{sim}} B dt \right]^n \quad (5.14)$$

with $B = A^{1/n}$, and t_{sim} is the simulation time.

B is what we call age rate, the amount of degradation per unit of time. The quasi-static approximation allows A to be used as a function of time and the degradation to be calculated with time-varying bias conditions. The calculation of age rate and degradation during stress time for NBTI (Equation 4.4) is implemented in functions *pmosYenCalcA* and *pmosYenCalcDeltaD* (alias of *calcA* and *calcDeltaD* respectively in figure 5.1) as below:

```

1  double pmosYenCalcA( URI_Model *model,
2      const URI_Var *const uriVar,
3      const URI_Env *const env, const int isDebug,
4      URI_sharedInstState *st1, URI_InstState *st2 )
5  {
6      PMOSYEN *mymodel = ( PMOSYEN * )model;
7      URI_MosVar *uriMosVar = ( URI_MosVar * )uriVar;
8      PMOSYENINSTSTATE *s2 = ( PMOSYENINSTSTATE * )st2;
9      PMOSYENSHAREDINSTSTATE *s1 = ( PMOSYENSHAREDINSTSTATE *
10     ↪ )st1;
11     double ageRate = 0.0;
12     double tox = uriMosVar->tox;

```

```

12     float vgs = uriMosVar->vgs;
13     float vds = uriMosVar->vds;
14     float vth = uriMosVar->von;
15
16     double C = mymodel->C;
17     double Ea = mymodel->Ea;
18     double KB = mymodel->KB;
19     double T = env->temp + 273.15;
20
21     if( fabs(vgs) < vth)
22     {
23         ageRate = 0;
24         printf("mosfet is in cutoff mode, agerate is set to
25         ↪ 0 vgs = %f vth=%.15f for %s (%s)\n", vgs, vth,
26         ↪ s1->devName, s1->modName);
27     }
28     else
29     {
30         ageRate = C *
31         ↪ pow((fabs(vgs)-fabs(mymodel->rel_vth0))/tox,
32         ↪ mymodel->gama) * exp(-Ea/(KB*T));
33         ageRate = pow(ageRate, 1/(mymodel->n));
34     }
35
36     if (ageRate < 0.0) abort();
37     s2->agerate = ageRate;
38     if ( isDebug ) {
39         printf( "pMosYenCalcA done for %s (%s) agerate is
40         ↪ %.18f, \n", s1->devName, s1->modName,
41         ↪ s2->agerate);

```

```

36     }
37     return ageRate;
38 }
39
40 double pmosYenCalcDeltaD( URI_Model *model,
41     const URI_Var *const uriVar, const int isDebug,
42     URI_sharedInstState *st1, URI_InstState *st2,
43     const URI_Env *const env )
44 {
45     PMOSYEN *mymodel = ( PMOSYEN * )model;
46     PMOSYENINSTSTATE *s2 = ( PMOSYENINSTSTATE * )st2;
47     URI_MosVar *uriMosVar = ( URI_MosVar * )uriVar;
48     PMOSYENSHAREDINSTSTATE *s1 = ( PMOSYENSHAREDINSTSTATE *
49     ↪ )st1;
50
51     double deltaD = s2->deltaD;
52     double n = mymodel->n;
53     double ageRate = s2->agerate;
54
55     if( ageRate > 0.0)
56     {
57         double tmpDeg = s2->agerate * uriMosVar->dt;
58         deltaD = pow( pow( deltaD, 1.0 / n ) + tmpDeg, n );
59         s2->deltaD = deltaD;
60     }
61
62     if ( isDebug ) {
63         printf( "pmosYenCalcDeltaD done for %s (%s),
64         ↪ deltaD=%.15f, ageRate=%.18f\n", s1->devName,
65         ↪ s1->modName, deltaD, ageRate);

```

```

63     }
64     return deltaD;
65 }

```

5.5.2 Degradation at aging time

Aging time is usually in the order of several years. We don't have enough computation resource to run the simulation over a long period of time. Even if we had enough resource, time is a constraint factor. Hence, we need to find a way to accelerate the simulation or extrapolate the degradation at aging time. During the stress simulation we have calculated the degradation as equation 5.13. At aging time t , we have:

$$\Delta D(t) = A.t^n \quad (5.15)$$

So the degradation at aging time t can be extrapolated as:

$$\Delta D(t) = \left(\frac{t}{t_{sim}} \right)^n \times \Delta D(t_{sim}) \quad (5.16)$$

Combining Equation 5.14 and Equation 5.16 allows us to implement the reliability models to Cadence simulator. This is implemented in function *pmosYenCalcDegradation* (an alias of *calcDegradation* in Figure 5.1):

```

1  double pmosYenCalcDegradation(URI_Model *model,
2      const URI_Var *const uriVar,
3      const double futuretime, const int isDebug,
4      URI_sharedInstState *st1, URI_InstState *st2,
5      const URI_Env *const env )
6  {
7      PMOSYEN *mymodel = ( PMOSYEN * )model;
8      PMOSYENINSTSTATE *s2 = ( PMOSYENINSTSTATE * )st2;

```

```

9     PMOSYENSHAREDINSTSTATE *s1 = ( PMOSYENSHAREDINSTSTATE *
    ↪ )st1;
10    double deg;
11
12    if ( isDebug ) {
13        printf( "Starting CalcDegradation(): ( dev: %s; mod:
    ↪ %s )\n", s1->devName, s1->modName );
14    }
15
16    deg = s2->deltaD * pow( futuretime / ( env->tStop -
    ↪ env->tStart ), mymodel->n );
17    if ( isDebug ) {
18        printf( "pmosYenCalcDegradation done, deg=%f \n",
    ↪ deg );
19    }
20    s2->totaldeg = deg;
21    return deg;
22 }

```

5.5.3 Scaling BSIM3v3 parameter and calculation of lifetime

In our reliability model, the degradation at aging time corresponds to the shift of BSIM3v3 parameter, V_{th0} . This shift is a positive value. The absolute value of degraded threshold voltage are always larger than the absolute value of its fresh value, which means:

$$|V_{th0}(t)| = |V_{th0}(t = 0)| + \Delta V(t) \quad (5.17)$$

with $\Delta V(t) > 0$.

So, for p-type MOS device, the degraded $V_{th0}(t)$ is:

$$V_{th0}(t) = V_{th0}(t = 0) - \Delta D(t) \quad (5.18)$$

For n-type MOS devices, we have:

$$V_{th0}(t) = V_{th0}(t = 0) + \Delta D(t) \quad (5.19)$$

The function *pmosYenScaleParam* (an alias of *scaleParam* in Figure 5.1) below shows the implementation for scaling BSIM3v3 parameter, V_{th0} .

```

1  double pmosYenScaleParam( URI_Model *model,
2      const double age, const char *const name,
3      const double value, const int isDebug,
4      const URI_Var *const uriVar, const
5      ↪ URI_sharedInstState *const st1,
6      const URI_Env *const env, const URI_InstState *const
7      ↪ st2 )
8  {
9      PMOSYEN *mymodel = ( PMOSYEN * )model;
10     PMOSYENSHAREDINSTSTATE *s1 = ( PMOSYENSHAREDINSTSTATE *
11     ↪ )st1;
12
13     if ( !strcasecmp( name, "VTH0" ) ) {
14         PMOSYENINSTSTATE *s2 = ( PMOSYENINSTSTATE * )st2;
15         double vthdeg = s2->totaldeg;
16         double sign;
17         if(value < 0.0) sign = -1;
18         else sign = 1;
19         double degraded = value + sign* vthdeg;
20         printf( "Beginning with vth0  %.15f, deg=%f  ending
21     ↪  value %.15f, defined para %.15f Starting
22     ↪  ScaleParam(): %s ( dev: %s; mod: %s )\n", value,
23     ↪  vthdeg, degraded, mymodel->rel_vth0, name,
24     ↪  s1->devName, s1->modName );

```

```

18     if(fabs(value - mymodel->rel_vth0) >
        ↪  fabs(0.00001*mymodel->rel_vth0))
19     {
20         printf("You have change the size of nmos/pmos,
        ↪  please readapte the value of rel_vth0,
        ↪  provied value %.15f, it should be %.15f\n",
        ↪  mymodel->rel_vth0, value);
21         abort();
22     }
23     return degraded;
24 } else {
25     return value;
26 }
27 }

```

By giving a specific degradation at which the device is considered to failure, for example 10% of V_{th0} , we can calculate the time required for this event to happen. This time is called the lifetime of the device. The degradation at lifetime can be given as an input to URI library via control statements of reliability block, see 5.4.1. From the Equation 5.16, we have the expression for the lifetime as below:

$$t = \left(\frac{\Delta D(t)}{\Delta D(t_{sim})} \right)^{1/n} t_{sim} \quad (5.20)$$

The lifetime calculation is implemented in function *pmosYenCalcLifetime()* (an alias of *calcLifeTime* in Figure 5.1):

```

1 double pmosYenCalcLifetime (URI_Model *model,
2     const double age, const double degAtLifetime,
3     const int isDebug, URI_sharedInstState *st1,
4     URI_InstState *st2, const URI_Env *const env)

```

5.5. IMPLEMENTING AGING-LAW EQUATIONS

```
5 {
6     PMOSYEN *mymodel = ( PMOSYEN * )model;
7     PMOSYENINSTSTATE *s2 = ( PMOSYENINSTSTATE * )st2;
8     PMOSYENSHAREDINSTSTATE *s1 = ( PMOSYENSHAREDINSTSTATE *
9     ↪ )st1;
10
11     double lt;
12
13     if ( isDebug ) {
14         printf( "Starting CalcLifeTime(): ( dev: %s; mod: %s
15         ↪ )\n", s1->devName, s1->modName );
16     }
17
18     lt = ( env->tStop - env->tStart ) * pow( degAtLifetime /
19     ↪ s2->deltaD, 1 / mymodel->n );
20
21     if ( isDebug ) {
22         printf( "pMosYenCalcLifetime done. Lifetime is
23         ↪ %f\n", lt);
24     }
25
26     return lt;
27 }
28 }
```

5.6 Conclusion

In this chapter, we have given an introduction of the BSIM3v3 compact model for circuit simulation. Besides, we have identified aging models following power law - for which a DC-to-transient translation is possible for reliability simulation. C code was used to build a dynamic library for URI supporting the integration of aging laws into SPECTRE® simulator. The circuit simulator embedded aging laws allows us to anticipate the electrical characteristic due to wear-out mechanisms, as well as the lifetime of a circuit at the early design time. This implementation is the primary step to develop the reliability tool for circuit design using SPECTRE® in Schlumberger.

6 | Verification and Validation of the compact model including aging laws

The intensive aging test campaign and the consistency of the obtained results presented in the previous chapter are important for the accuracy of the reliability simulation. This chapter will focus on validating reliability models implemented in SPECTRE[®] simulator at the circuit level. First, the excellent agreement of aged measurements and aged simulations at the transistor level laid the foundation for validating the proposed aging laws at the circuit level. The circuits used in this work are Inverters and Ring Oscillators, which are the primary circuits for aging assessments. The implementation of reliability models into SPECTRE[®] simulator allows for investigating the impact of aging degradation of a circuit under several biases and temperature stress conditions, regardless of various transistor dimensions.

6.1 Transistor level

The NBTI/HCI models presented in the previous chapter have been implemented into SPECTRE[®] simulator. The V_{th0} evolution as a function of time has been modeled based on the aging test results to simulate the degradation behavior of single transistors observed from experiments.

The compact model provided by the foundry just ensures DC characteristics accuracy lower than 175°C. Therefore, beyond this critical temperature, there is a large discrepancy between simulation and measurement ($\approx 14\%$). Before performing aging simulation, BSIM3 parameter (V_{th0}) has been slightly modified to obtain the better agreement between measurement and simulation of fresh transistors. We present in Figure 6.1 the schematic of the circuit for reliability simulation of a single transistor. Reliability simulations of a 1.8V nMOS and pMOS under CHE and NBTI_2 stress conditions were performed to validate the proposed aging laws. We obtained very good accuracy compared to experimental results even at extreme temperature close to 210°C as shown in Figure 6.2 and Figure 6.3.

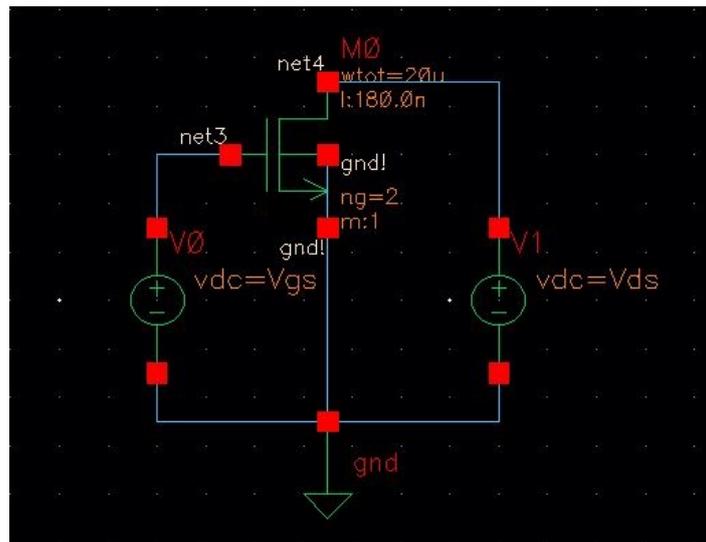


Figure 6.1: Schematic of 1.8V nMOS transistor for reliability simulation.

In order to reproduce the degradation in the aging tests, we need to apply the exact similar stress conditions in the experiments for reliability simulation. A feasible way is to define the aging conditions in the Reliability Block of the circuit netlist. An example of Reliability Block to run the reliability simulation for 1.8V nMOS under CHE stress condition is shown below:

```
// Fresh Statements
change0_0 alter param=Vgs value=1.8
change0_1 alter param=temp value=210
tran_fresh tran stop=100ns param=Vds param_vec=[0ns 0 100
ns 1.8] param_step=1ns

// Reliability Block
rel reliability {

// Control Statements
enable_ade_process value=yes
age time=[2000.0000h]
accuracy level=1
```

```

uri_lib file = ".../libURI.so"

// Stress Statements
change1_0 alter param=Vgs value=2
change1_1 alter param=temp value=210
tran_stress tran stop=100ns param=Vds param_vec=[0ns 2
    100ns 2] param_step=1ns

// Aging Statements
change2_0 alter param=Vgs value= 1.8
change2_1 alter param=temp value=210
tran_aging tran stop=100ns param=Vds param_vec=[0ns 0 100
    ns 1.8] param_step=1ns
}

```

First, the fresh simulation (at $t_{stress}=0$) will be performed by taking the conditions included in the *Fresh Statements*. Note that the reliability simulation is just available for transient analysis allowing to compute the circuit response as a function of time. Therefore, we assigned V_{ds} is a transient parameter which can be swept with time. For example, indicating in the code above, we simulated the I_{ds} - V_{ds} curve at $V_{gs}=1.8\text{V}$ and $T=210^\circ\text{C}$, while the V_{ds} is swept from 0 to 1.8V during 0ns to 100ns duration.

Then the second simulation applies the stress conditions and stress duration that are defined in *Control Statements* and *Stress Statements*. As in the code above, we applied a stress conditions $V_{gs}=2\text{V}$ and $V_{ds}=2\text{V}$ (V_{ds} is constant at 2V during the sweep from 0ns to 100ns). Stress duration is 2,000 hours and stress temperature is 210°C . The degradation will be calculated depending on the stress conditions and extrapolated to 2,000 hours.

The third simulation (aged simulation) will be performed with the same conditions as the fresh simulation to show the shift of electrical characteristics due to transistor degradation.

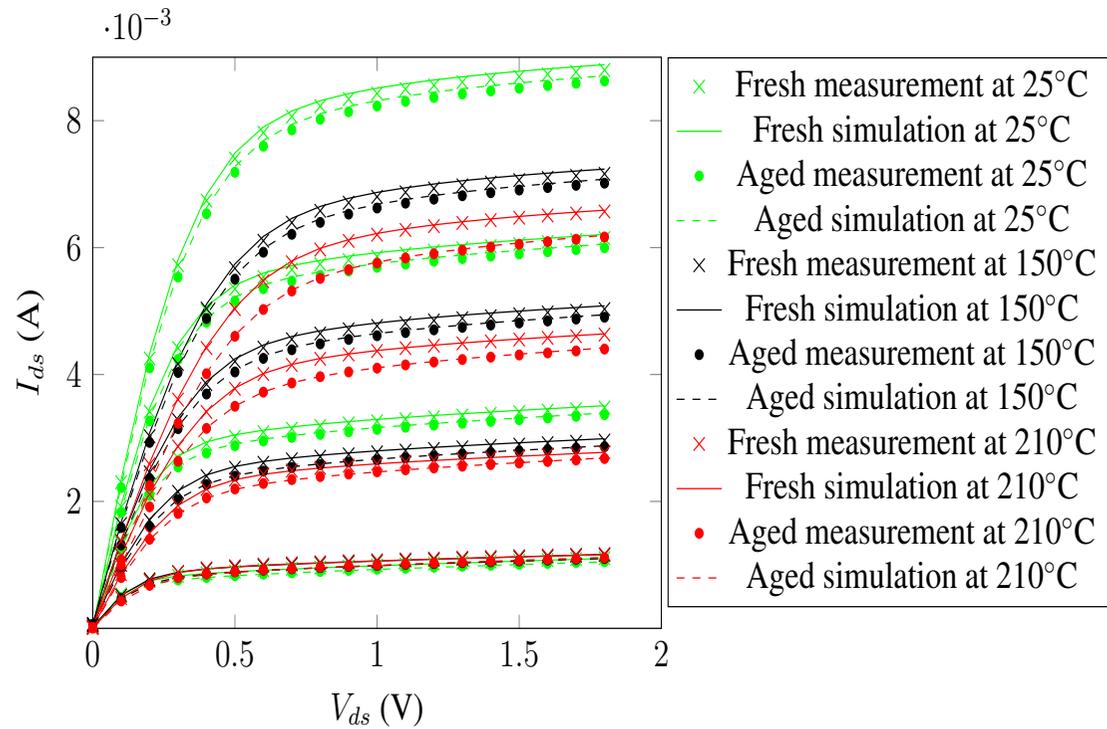


Figure 6.2: Comparison of aged simulations and aged measurements of a 1.8V nMOS ($W/L=20/0.18\mu\text{m}$) under CHE bias condition at 25°C, 150°C and 210°C after 2,000h stress. The values of V_{gs} are 0.9V, 1.2V, 1.5V and 1.8V, respectively.

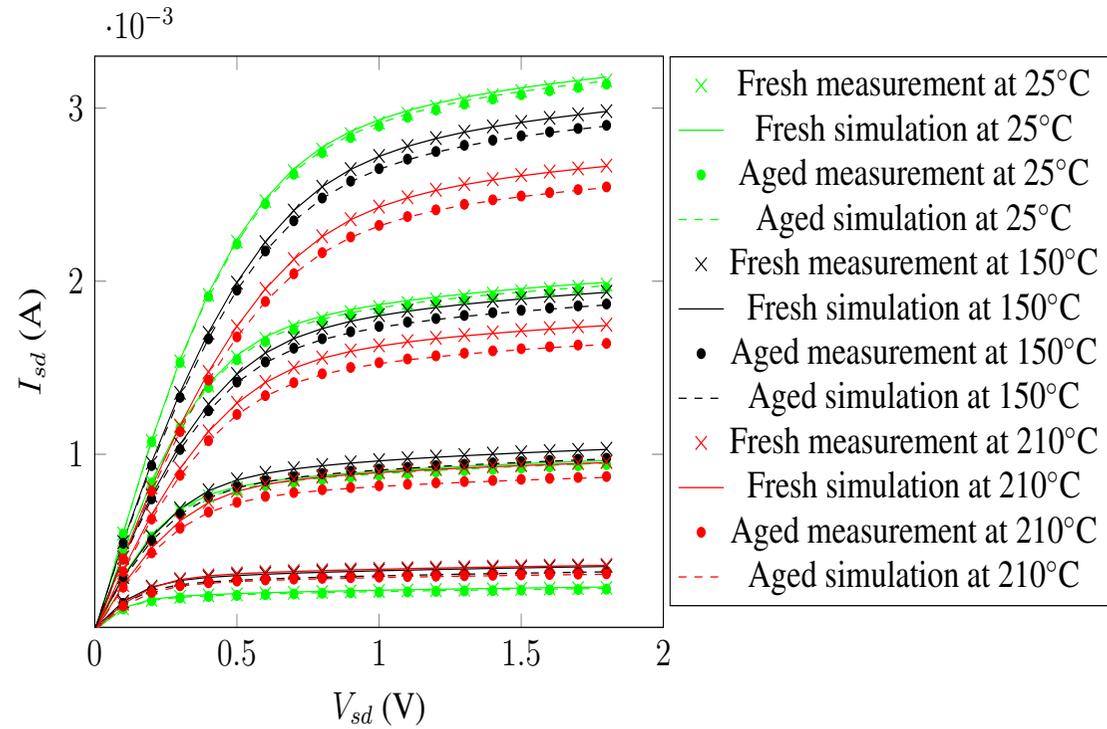


Figure 6.3: Comparison of aged simulations and aged measurements of a 1.8V pMOS ($W/L=20/0.18\mu\text{m}$) under NBTI_2 bias condition at 25°C, 150°C and 210°C after 2,000h stress. The values of V_{sg} are 0.9V, 1.2V, 1.5V and 1.8V, respectively.

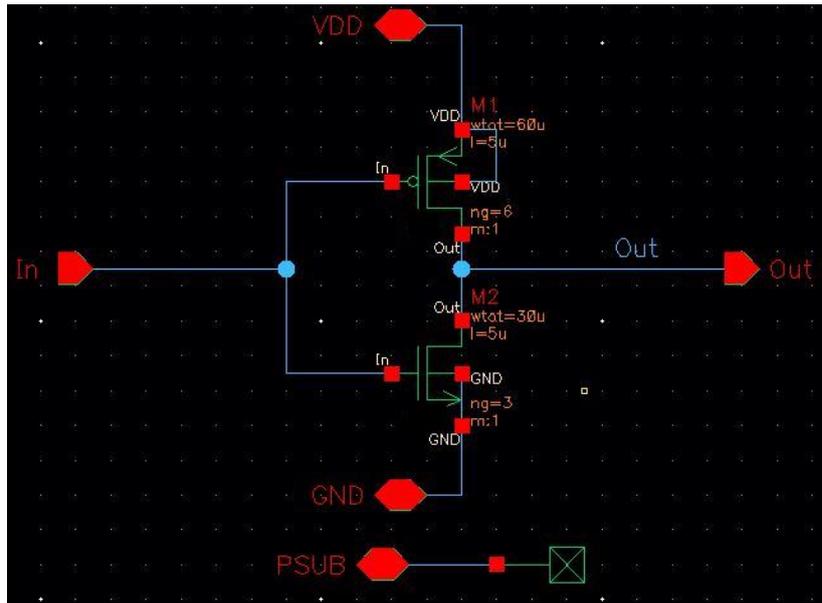
6.2 3.3V CMOS Inverters

The aging tests performed on 3.3V single transistors have shown that HCI and PBTI have a minor impact, while NBTI is dominant (Chapter 4). The NBTI model proposed in the previous chapter has been embedded into the SPECTRE[®] simulator, and it has shown an excellent agreement with measurements at the single transistor level. This section presents an experimental investigation of NBTI impact on CMOS inverters in which we applied a set of DC voltages at 150°C and 210°C for 2,000 hours. The results have shown that NBTI induces a shift in the inverter Voltage Transfer Curve (VTC), and it worsens under both elevated temperatures and high negative stress voltages. Many studies of NBTI impact on CMOS inverter reliability have been reported [153], [154],[155], [156], [157], [158]. Therefore, this section does not intend to give a deep physics and analysis of NBTI on inverter degradation. We will focus on validating and verifying the reliability models in the circuit simulator for as simple topology as the inverter. This validation will then be extended to the complicated circuit presented in the next section.

6.2.1 Inverter description

The samples under test are two types of CMOS inverter, denoted as Inv_1 and Inv_2. Inv_1 has aspect ratios of 60/5 μ m for pMOS and 30/5 μ m for nMOS as shown in Figure 6.4. Inv_2 has aspect ratios of 10/5 μ m for pMOS and 5/5 μ m for nMOS. Both of them are fabricated in 0.35 μ m CMOS technology qualified for high temperature applications.

The initial characterizations for Inv_1 and Inv_2 were performed at 25, 150, and 210°C. Inverter Voltage transfer curves (VTC) of five samples of each inverter type were measured to evaluate the dispersion of the fresh measurements. Figure 6.5 and Figure 6.6 present the stability and consistency of the inverter VTC at different temperatures. The simulation result at 25°C is not well fitted with measurements. This difference may be related to the process deviation. However, simulation result tends to converge with measurement results at higher temperatures.



(a)

Figure 6.4: Schematic of Inv_1

6.2.2 Inverter aging test

The aging tests on inverters were carried out on fully automated test benches. It includes power supplies for applying stress voltages, and Keithley source meters (2410SM) for voltage measurements. The DUTs were placed on the oven to perform the test at 150 and 210°C. The test protocol for Inv_1 and In_2 is as follows: during the aging test phase, a zero voltage was applied to the inverter input, while a voltage of 3.6V was applied to the V_{dd} and inverter output pads as Figure 6.7 [155], [156], [157], [158]. Therefore, during the aging phase, only pMOS of the inverter is stressed with $V_{sg}=3.6V$ and $V_{sd}=0V$. This stress condition is expected to activate intrinsic NBTI mechanism in pMOS. The general idea for this aging configuration is to investigate the impact of pMOS degradation due to NBTI mechanism on the overall circuit behavior. During the measurement phase, inverter were switched to Keithley source meters. A conventional DC configuration was used for the measurement phase where a DC voltage of 3V was applied to V_{dd} , the inverter inputs were swept from 0 to 3V with step size 0.2V and the outputs were monitored (measured). We encrypted a Python program to automate the switch between stress and measure configurations. The duration of the aging tests are 2,000 hours.

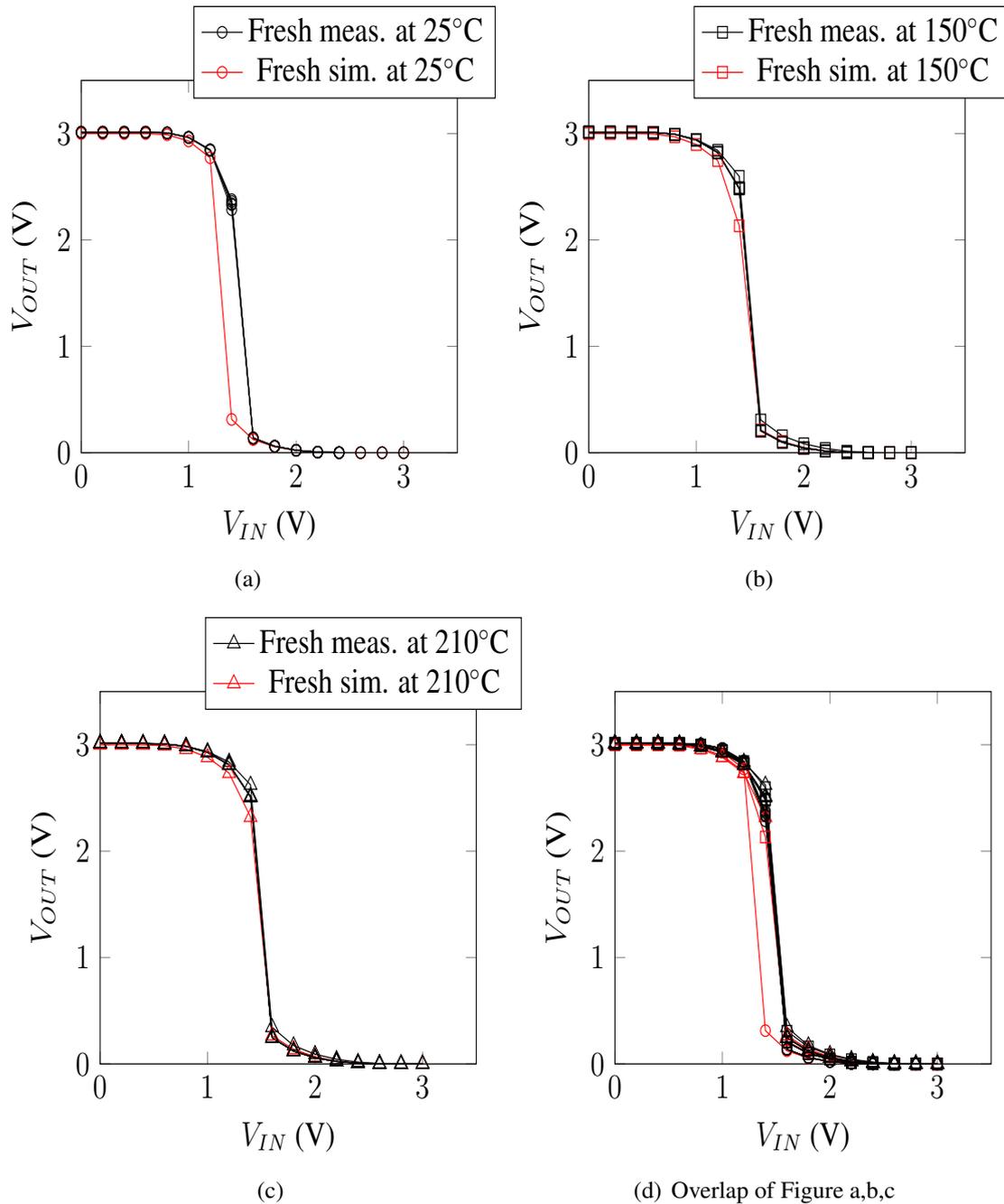


Figure 6.5: Inv_1 initial characterizations on five samples at several temperatures and the associated simulation results.

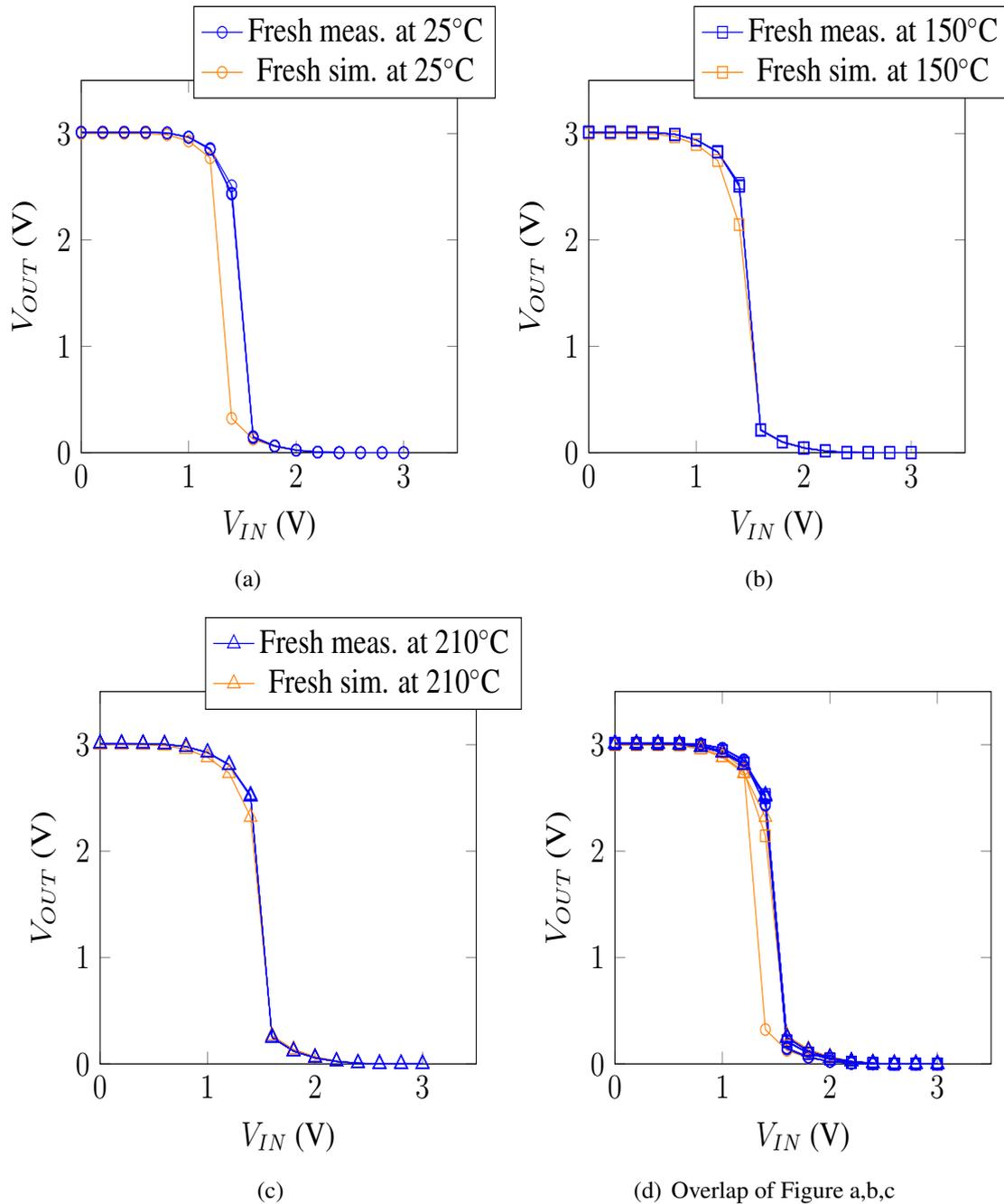


Figure 6.6: Inv_2 initial characterizations on five samples at several temperatures and the associated simulation results.

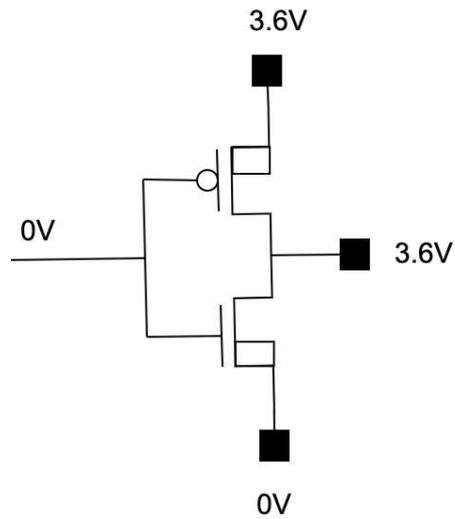


Figure 6.7: CMOS inverter configuration under NBTI stress

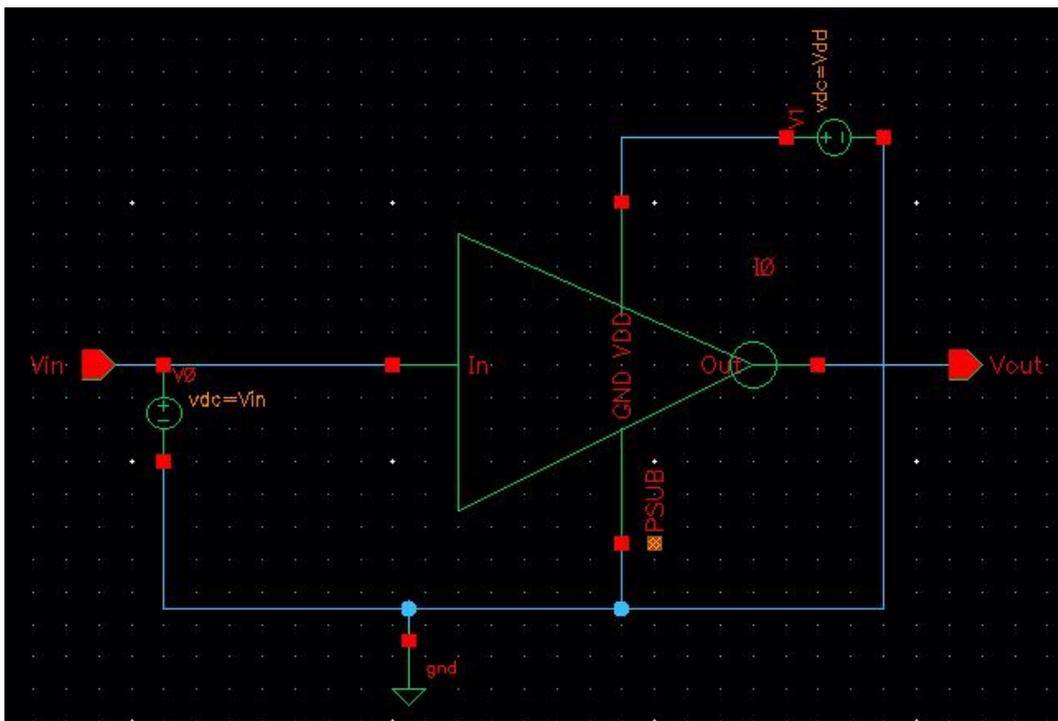


Figure 6.8: Configuration of an inverter for reliability simulation.

6.2.3 Reliability simulation results

Many published researches have reported the impact of NBTI on the CMOS inverter

voltage transfer curve [153], [154],[155], [156], [157], [158]. According to these results, VTC is shifted to the left due to NBTI degradation and the magnitude of the VTC shift increases with increased applied field and/or increased stress time. Therefore, we have performed reliability simulation on SPECTRE® under various stress voltages and stress time. The configuration for inverter reliability simulation is presented in Figure 6.8.

First, we run reliability simulation for Inv_1 with $V_{dd(stress)}$ equal to 2.5V, 3.6V and 3.9V at 210°C. The zero voltage is applied to the input all time during 2,000 hours stress. The aging simulation results at 2,000h are shown in Figure 6.9. We obtain the VTC shift increasing with increased $V_{dd(stress)}$ as expected.

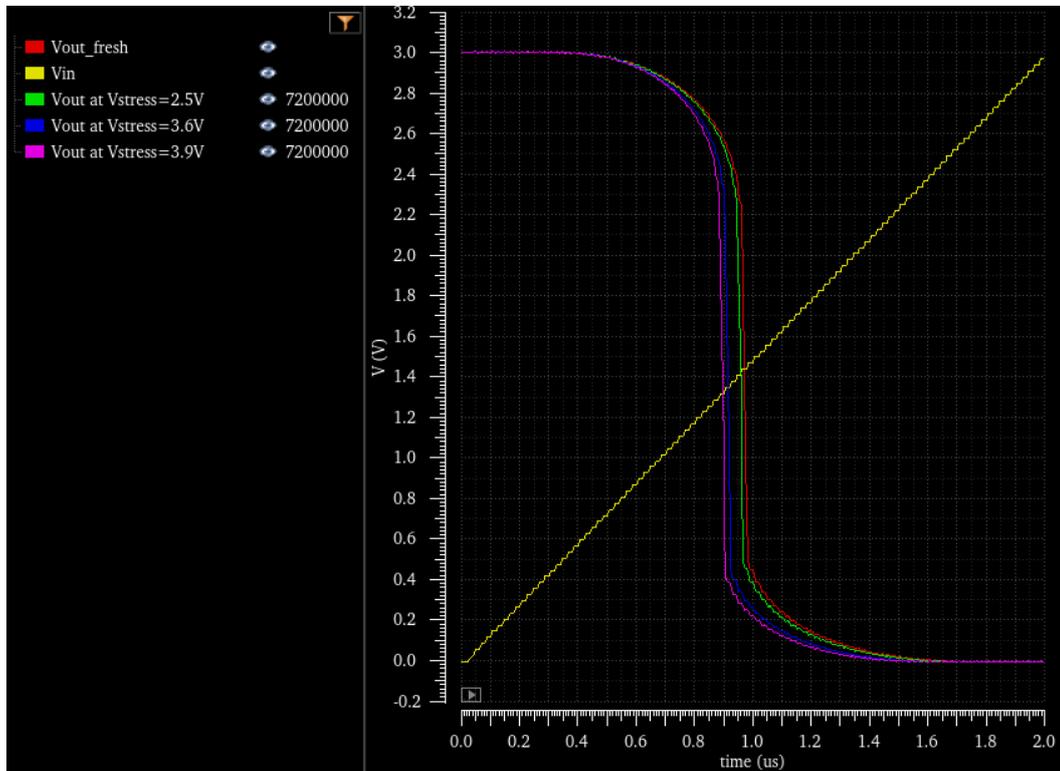


Figure 6.9: The aging simulation results of Inv_1 at 2,000h stress under $T=210^{\circ}\text{C}$ and $V_{dd(stress)}=2.5\text{V}$, 3.6V and 3.9V .

Then, we try another reliability simulation for Inv_1 with the constant $V_{dd(stress)}=3.6\text{V}$ with increased stress time. The zero voltage is applied to the inverter input all time during the stress phase. The simulation results after 2,000h, 5,000h and 10,000h are shown in the Figure 6.10. We get the VTC gradually shift to the left which is an excellent agreement with

the results in literature. Therefore, these simulation results have validated our approach. SPECTRE[®] simulator including our reliability models has the accurate capability of predicting the aging behavior of the circuit electrical characteristics.

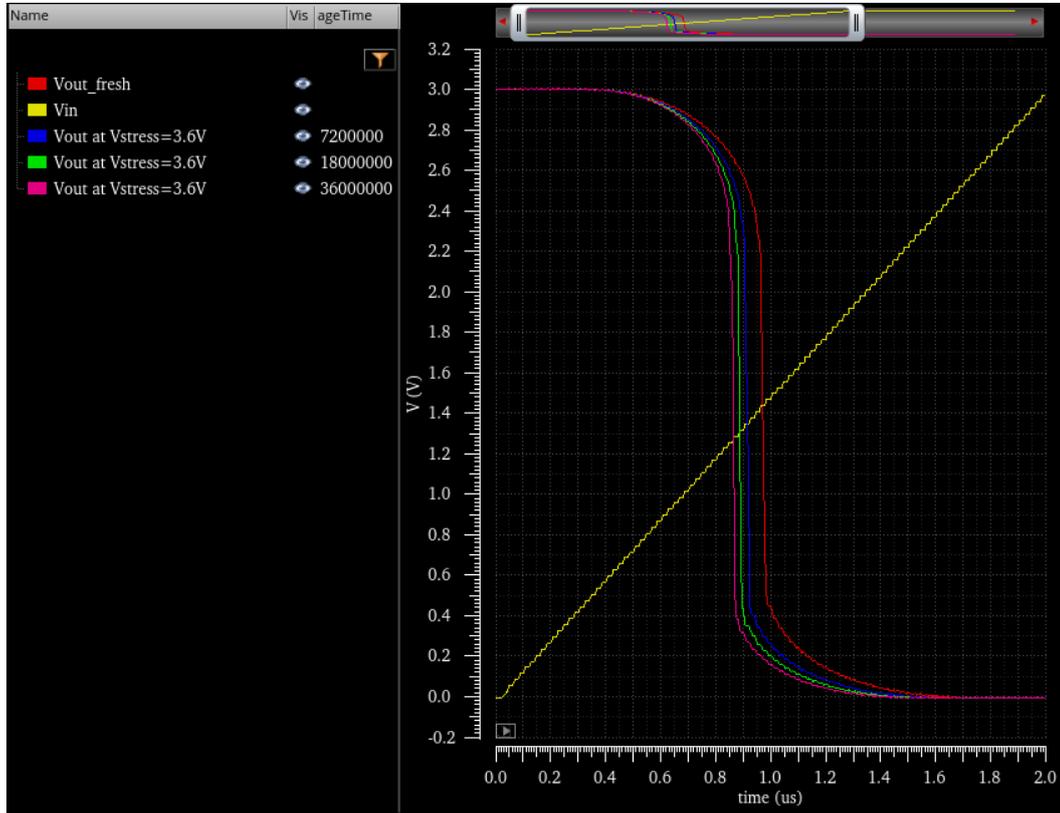


Figure 6.10: The aging simulation results of Inv_1 at 2,000h stress under $T=210^{\circ}\text{C}$ and $V_{dd(stress)}=3.6\text{V}$. The stress time are 2,000h, 5,000h and 10,000h. The aging time shown in this figure has been converted equivalently in seconds.

6.2.4 Reliability simulation results

We have conducted aging tests on Inv_1 and Inv_2 at $V_{dd}=3.6\text{V}$ and stress temperatures are 150 and 210°C for 2,000h. Before running the reliability simulation, the V_{th} of nMOS and pMOS are slightly modified ($\pm 0.02 - 0.05\text{V}$) to fit the fresh simulation with the fresh measurements. Finally, aged simulations are well fitted with the aged measurements even at extreme temperature as 210°C as shown in Figure 6.11 and Figure 6.12.

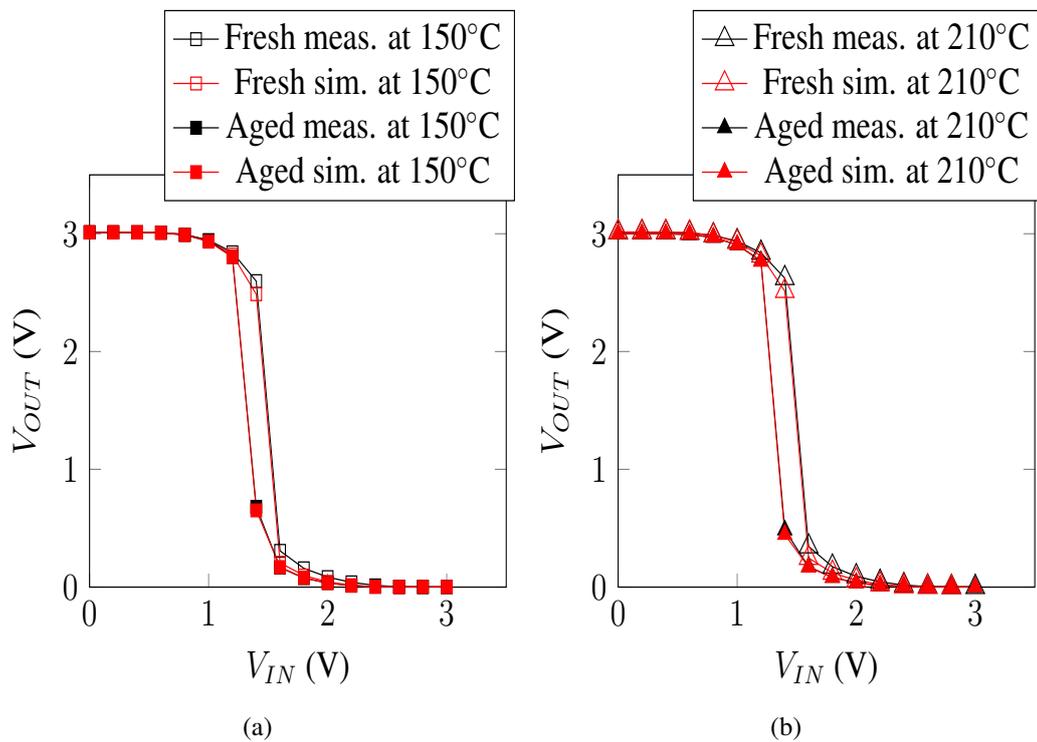


Figure 6.11: Comparison of measurements and simulations of Inv_1

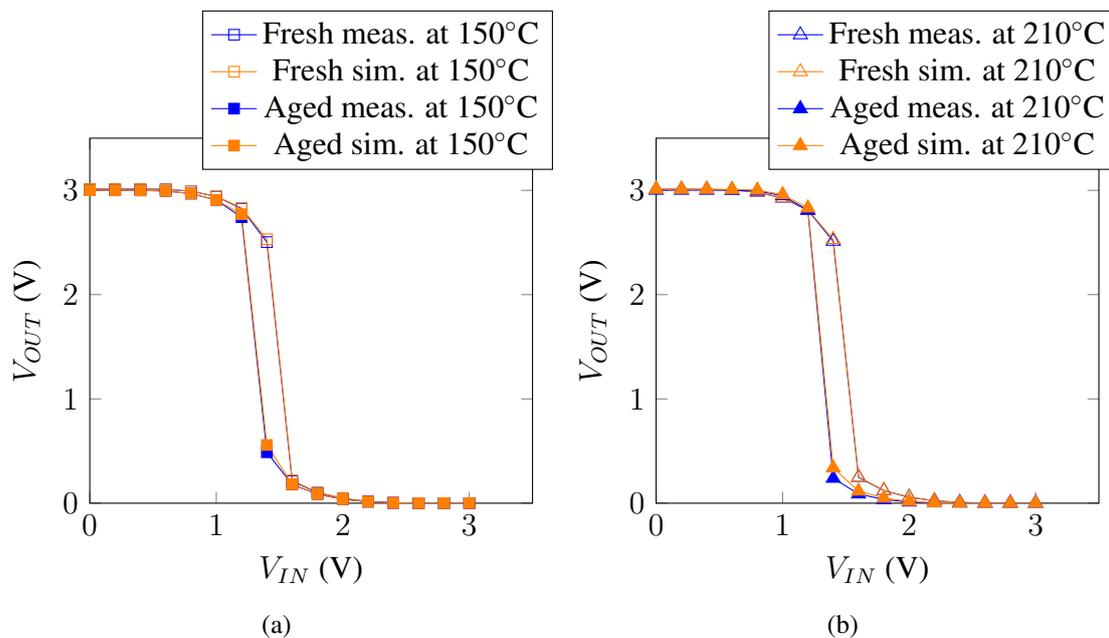


Figure 6.12: Comparison of measurements and simulations of Inv_2

6.3 Ring Oscillators

In previous sections, the aging models have shown an accuracy in reproducing experimental characteristics drifts in transistor-level and basis CMOS inverters. This section will present the aging measurements on several Ring Oscillators (ROs) fabricated in the $0.18\mu\text{m}$ and $0.35\mu\text{m}$ CMOS technology qualified for high temperatures. The resulting drifts will be compared to reliability simulations to assess the accuracy of the proposed reliability models in a complicated circuit and its computational efficiency in the SPECTRE[®] circuit simulator after implementing aging laws.

6.3.1 Ring Oscillator description

Ring Oscillator is the basic digital circuit that is frequently used to quantify the performance of digital products during the development of technology. Our team in Schlumberger has conducted a massive aging test campaign on several types of RO at different V_{dd} voltage and temperature conditions to validate the quality of the technology. In this work, we will take into account 16 RO types. Eight RO types fabricated in $0.18\mu\text{m}$ technology are denoted as RO_1 to RO_8, and the other eight types of RO fabricated in $0.35\mu\text{m}$ technology are named as RO_9 to RO_16. The RO_1 will be described in detail first.

The basic block diagram of RO_1 is shown in Figure 6.13. It consists of a NAND gate (NANDx1) and 12 ring oscillator units (d1m_ringo1_unit) as elementary circuit blocks of an odd number. The output of the last inverter is looped back to one of the inputs of a NAND gate. The output buffer (BUFx1) is used to drive a large load. A ring oscillator made up of inverters and a NAND gate makes it possible to start the oscillations of the circuit through the ENABLE logic signal as input. The frequency divider placed at the output reduces the raw RO frequency by one fourth, allowing the signal to go through long cable from the oven to the measurement instrument.

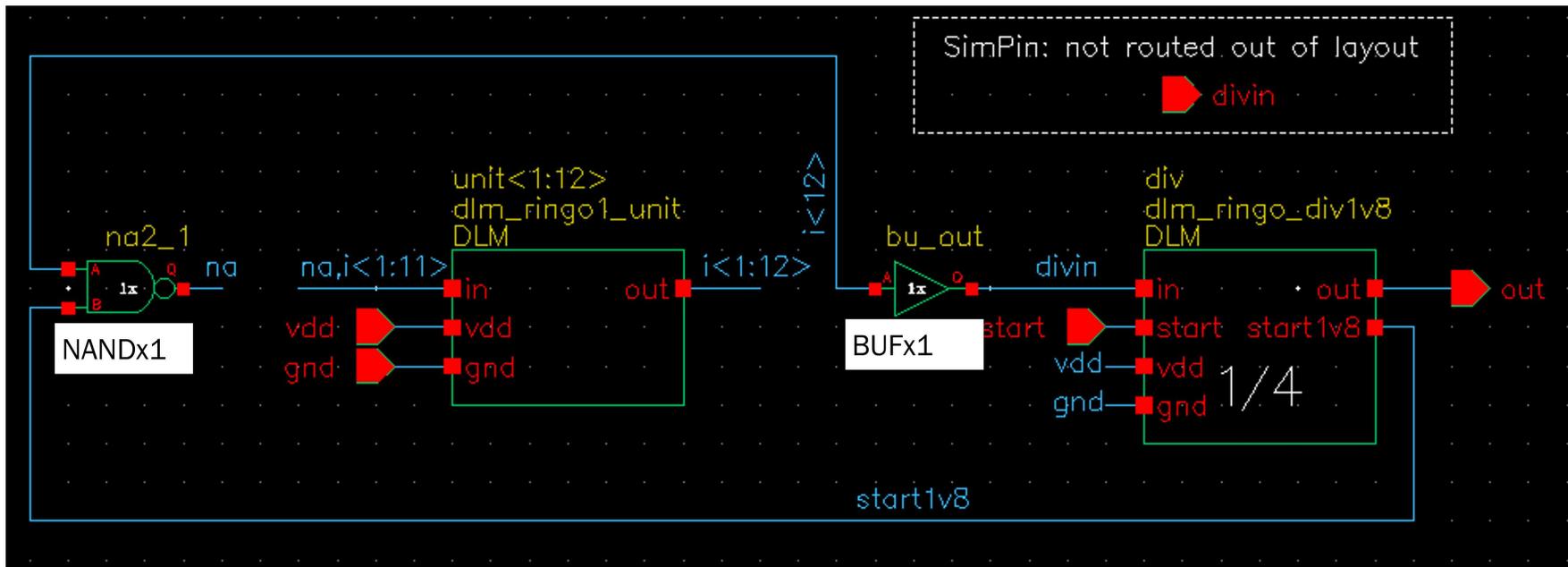


Figure 6.13: Basic block diagram

NAND gate (NANDx1)

The NAND gate placed at the input of the inverter chain allows the start or stop of the RO operation. The ENABLE input signal of the NAND gate triggers switching at the input of the first CMOS inverter, causing the oscillation and propagation of the signal to the last inverter. NAND gate is composed of pMOS $L/W=1.01\mu\text{m}/0.18\mu\text{m}$ and nMOS $L/W=0.89\mu\text{m}/0.18\mu\text{m}$. The schematic of NAND gate is shown in Figure 6.14.

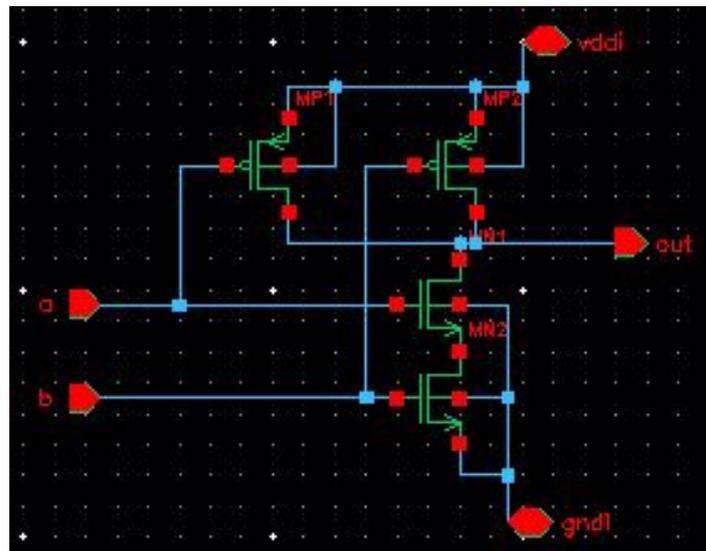


Figure 6.14: Schematic of NAND gate in RO_1.

Ring oscillator unit (dlm_ringo1_unit)

The characteristics of a RO are related to the number of logic gates or stages. In our case, RO_1 consists of a NAND gate connected with 12 ring oscillator units. A ring oscillator unit consists of an inverter (INVx1) and a buffer (BUFx1). The transistor dimensions forming the inverter (INVx1) are: $W/L=1.41/0.18\mu\text{m}$ for pMOS and $W/L=0.58/0.18\mu\text{m}$ for nMOS. This inverter cell and buffer cell have the smallest size in our digital test chip using in this work. The schematic of inverter (INVx1) and the buffer (BUFx1) is presented in Figure 6.15 and Figure 6.16, respectively.

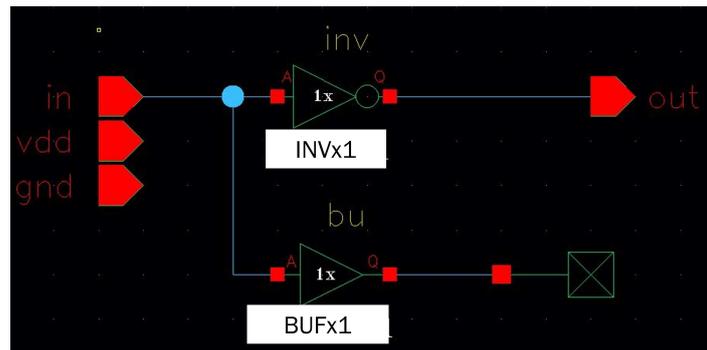


Figure 6.15: Schematic of ring oscillator unit (d1m_ringo1_unit)



Figure 6.16: Schematic of the buffer (BUFx1)

Frequency divider (d1m_ringo_div1v8)

A frequency divider is placed at the output of the inverter chain, allowing to measure of the frequency because it must be less than 1 MHz at the output of the divider to avoid noise and measurement inaccuracy. The structure of the frequency divider is depicted in Figure 6.17.

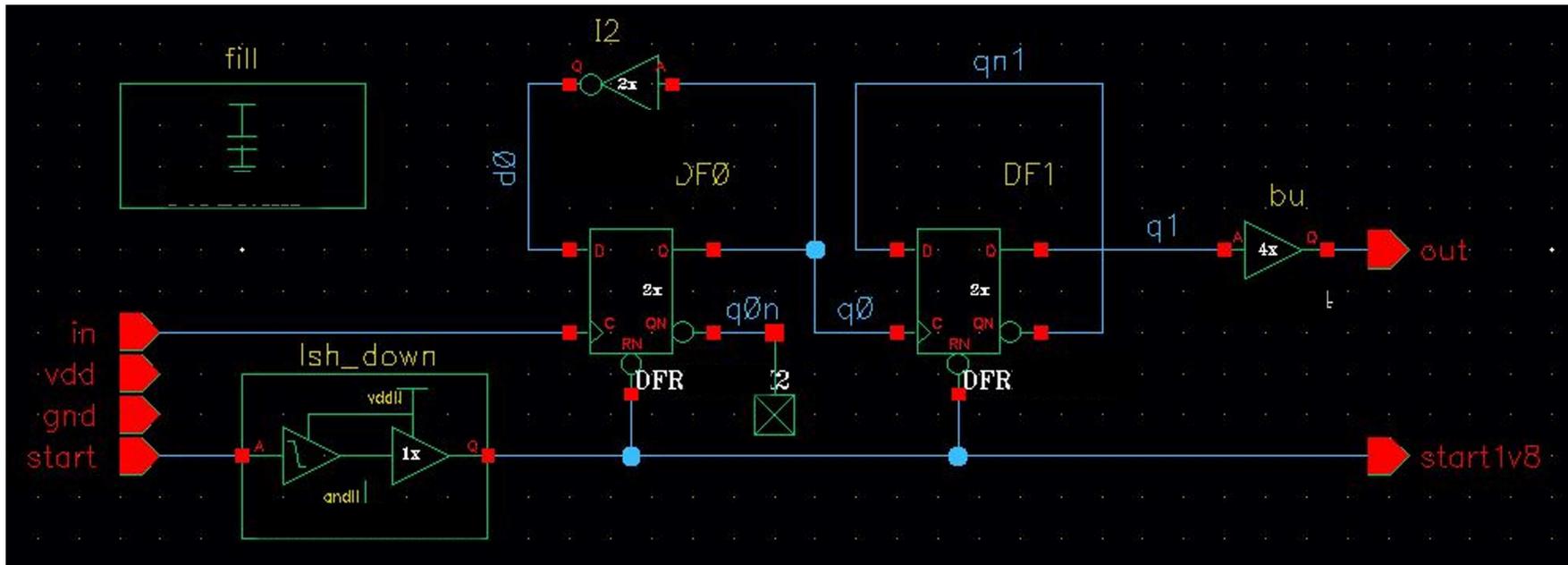


Figure 6.17: Schematic of frequency divider.

RO characteristics

RO1 uses minimum size inverter cell (INVx1) with an extra load of minimum buffer cell (BUFx1). We have performed initial characterizations on eleven RO_1 devices. The frequency range of RO1_1 at room temperature is 100 to 180 MHz with V_{dd} varying from 1.35V to 1.95V as shown in Figure 6.18a. As expected, ring oscillator frequency increases as the increase of supply voltage and decreases as the increase of temperature. The frequency dispersion of RO_1 is reduced at high temperatures as in Figure 6.18b. This observation is similar with initial characterizations at transistor level (Appendix A), where the dispersion of drain current is smaller at higher temperatures.

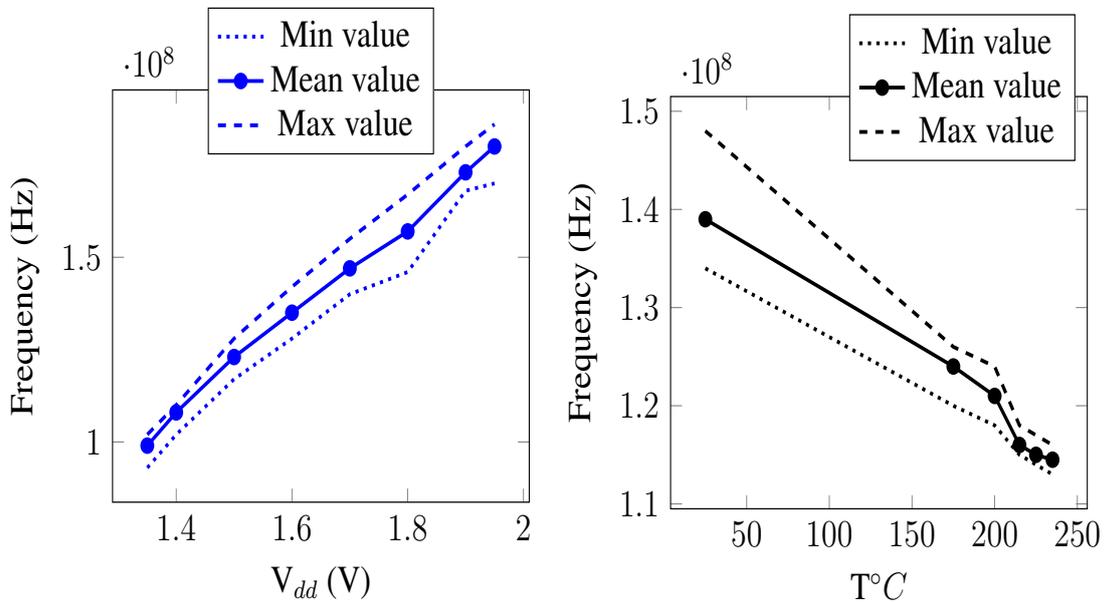
(a) RO_1 frequency vs. V_{dd} at 25°C(b) RO_1 frequency vs. $T^{\circ}C$ at $V_{dd} = 1.65V$

Figure 6.18: RO1 frequency dependence on V_{dd} and temperature. Eleven RO_1 devices was taken into account for initial characterizations before the aging tests.

Description of RO_2 to RO_16 for aging test

RO_1 to RO_8 were designed with 1.8V CMOS transistors ($0.18\mu m$ CMOS technology). The detailed information of the circuit schematics of RO_2 to RO_16 can be found in Appendix C.

- RO_2 uses minimum size inverter cell (INVx1) as RO_1 with an extra load of x8 buffer cell (BUFx8). Due to the higher load cell, ring oscillator frequency is less than half of

ring oscillator frequency of RO_1. At room temperature ring oscillator range is from 45 to 77 MHz at room temperature with V_{dd} varying from 1.35V to 1.95V.

- RO_3 uses x8 size inverter cell (INVx8) with an extra load of x8 buffer cell (BUFx8). RO_3 provides the highest ring oscillator frequency compared to the rest. At room temperature, Ring oscillator frequency range is 120 to 200 MHz with V_{dd} varying from 1.35V to 1.95V.
- RO_4 uses x8 size inverter cell (INVx8) with an extra load of four of x8 buffer cell (BUFx8). Oscillator frequency range at room temperature is 75 to 132MHz with V_{dd} varying from 1.35V to 1.95V.
- RO_5 uses minimum size 2-input NAND cell (NANDx1) with an extra load of x4 buffer cell (BUFx4). The other input of the NAND cell is connected to high level. Oscillator frequency range at room temperature is 54 to 98MHz with V_{dd} varying from 1.35V to 1.95V.
- RO_6 uses minimum size 2-input NOR cell (NORx1) with an extra load of x4 buffer cell (BUFx4). The other input of the NOR cell is connected to low level. Oscillator frequency range at room temperature is 45 to 88MHz with V_{dd} varying from 1.35V to 1.95V.
- RO_7 uses minimum size OR-NAND cell (OR-NANDx1) with an extra load of x4 buffer cell (BUFx4). The ring oscillator input is connected to one of OR input. The other OR input is connected to low level, and input of NAND is connected to high level. Oscillator frequency range at room temperature is 36 to 67MHz with V_{dd} varying from 1.35V to 1.95V.
- RO_8 uses minimum size AND-NOR cell (AND-NORx1) with an extra load of x4 buffer cell (BUFx4). The ring oscillator input is connected to one of AND input. The other AND input is connected to high level, and input of NOR is connected to low level. Oscillator frequency range at room temperature is 38 to 70 MHz with V_{dd} varying from 1.35V to 1.95V.

Ring oscillator RO_9 to RO_16 were designed with 3.3V CMOS transistors (0.35 μ m CMOS technology). Configuration of RO_9 to RO_16 are exactly as RO_1 to RO_8. The difference is the transistor type used for ring oscillator. In general, ring oscillator frequency by 3.3V CMOS transistor (RO_9 to RO_16) are faster than that of 1.8V CMOS transistor (RO_1 to RO_8) at room temperature. However, at high temperature, 3.3V CMOS transistor is slower than 1.8V CMOS transistor. V_{dd} dependency is smaller on 3.3V CMOS transistor than 1.8V CMOS transistor.

- RO_9 uses minimum size inverter cell (3V_INVx1) with an extra load of minimum buffer cell (BUFx1). Oscillation frequency at room temperature is 116 to 153MHz with the V_{dd} voltage varying from 2.7V to 3.9V.
- RO_10 uses minimum size inverter cell (3V_INVx1) with an extra load of x8 buffer cell (3V_BUFx8). Oscillation frequency at room temperature is 63 to 84MHz with the V_{dd} voltage varying from 2.7V to 3.9V.
- RO_11 uses x8 size inverter cell (3V_INVx8) with an extra load of x8 buffer cell (3V_BUFx8). RO_11 oscillation frequency at room temperature is 160 to 210 MHz with the V_{dd} voltage varying from 2.7V to 3.9V. This is the fastest ring oscillator in the digital test chip using in this work. Ring oscillator frequency on RO_11 (3.3V gate) is faster than that of RO_3 (1.8V gate) at room temperature.
- RO_12 uses x8 size inverter cell (3V_INVx8) with an extra load of four of x8 buffer cell (3V_BUFx8). RO_12 oscillation frequency at room temperature is 100 to 130 MHz with the V_{dd} voltage varying from 2.7V to 3.9V.
- RO_13 uses minimum size 2-input NAND cell (3V_NANDx1) with an extra load of x4 buffer cell (3V_BUFx4). The other input of the NAND cell is connected to high level. RO_13 oscillation frequency at room temperature is 69 to 94 MHz with the V_{dd} voltage varying from 2.7V to 3.9V.
- RO_14 uses minimum size 2-input NOR cell (3V_NORx1) with an extra load of x4 buffer cell (3V_BUFx4). The other input of the NOR cell is connected to low level. RO_14 oscillation frequency at room temperature is 66 to 91MHz with the V_{dd} voltage

varying from 2.7V to 3.9V.

- RO_15 uses minimum size OR-NAND cell (3V_OR-NANDx1) with an extra load of x4 buffer cell (3V_BUFx4). The ring oscillator input is connected to one of OR input. The other OR input is connected to low level, and input of NAND is connected to high level. RO_15 oscillation frequency at room temperature is 49 to 68 MHz with the V_{dd} voltage varying from 2.7V to 3.9V.
- RO_16 uses minimum size AND-NOR cell (3V_AND-NORx1) with an extra load of x4 buffer cell (3V_BUFx4). The ring oscillator input is connected to one of AND input. The other AND input is connected to high level, and input of NOR is connected to low level. RO_16 oscillation frequency at room temperature is 49 to 68 MHz with the V_{dd} voltage varying from 2.7V to 3.9V. Oscillation frequency is exactly same as RO_15.

6.3.2 Ring Oscillator aging test

In Schlumberger, our team have conducted a massive aging tests for digital test chip implemented ROs to qualify 0.18 μ m CMOS technology for high temperature application. ROs were stressed under various aging conditions: the V_{dd} ranges from 1.35V to 1.95V for 1.8V ROs and from 2.7V to 3.9V for 3.3V ROs; the stress temperatures are 25, 150, 175, 200, 215, 225, and 235°C. For the scope of this thesis, in the rest of this manuscript, we only present the aging test results at 235°C, and $V_{dd} = 1.95$ V and 3.9V for 1.8V ROs and 3.3V ROs, respectively; as Table 6.1.

RO type	Device	Stress Voltage	Stress Temperature
1.8V RO	RO_1 to RO_8	1.95V	235°C
3.3V RO	RO_9 to RO_16	3.9 V	235°C

Table 6.1: Stress conditions for ROs

The test protocol utilized in this work is described as follows: During the aging test, the terminal V_{dd} of RO is connected to corresponding power supply. The frequency were frequently measured during the aging test by frequency counter Keysight 53131A. A cus-

tomized test program for the test set-up was written in Python.

6.3.3 Reliability simulation results

The configuration for RO aging tests are presented in Figure 6.19. Reliability simulation result for RO_1 after 2,000h stress at 235°C at $V_{dd}=1.95V$ is shown in 6.20. The yellow line is the fresh output signal and the red line is the aged output signal after 2,000h applying stress, indicating the drift of the output signal with time.

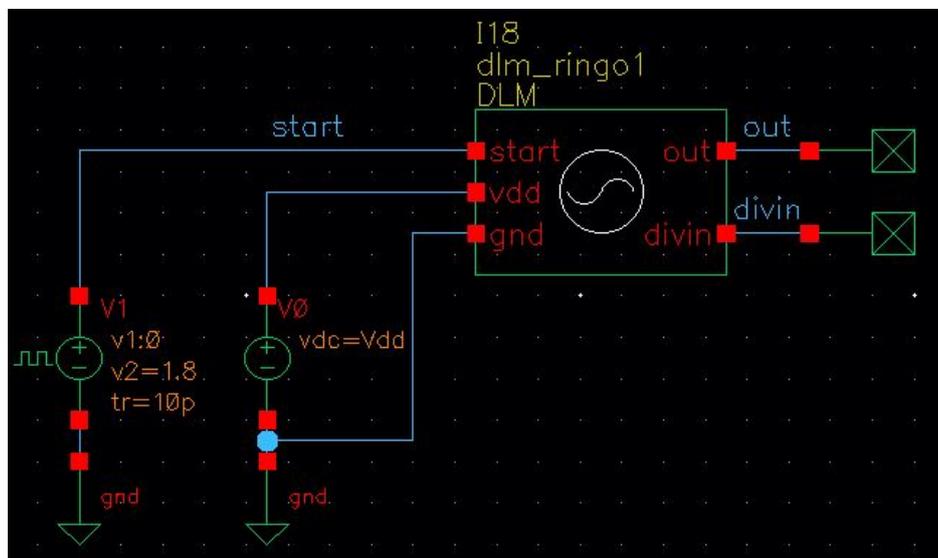


Figure 6.19: Aging test configuration for RO1

Aging degradation is highly context-sensitive. The transistors in a circuit will experience completely different age stress patterns and thus degrade differently. Our reliability models implemented in SPECTRE® simulator provides the ability to investigate the individual transistors aging in a complex circuit. The reliability simulation data shown that the degradation of one transistor differ from another one in the circuit as in Figure 6.21.

It is assumed that the first failure anywhere in the circuit will lead to the whole circuit to fail. However, it has been proven that some circuits may withstand several failures without stopping operation [159]. Therefore, it is difficult to investigate aging effects in complicated circuit in practice. Our reliability models implemented in URI (SPECTRE®) can calculate

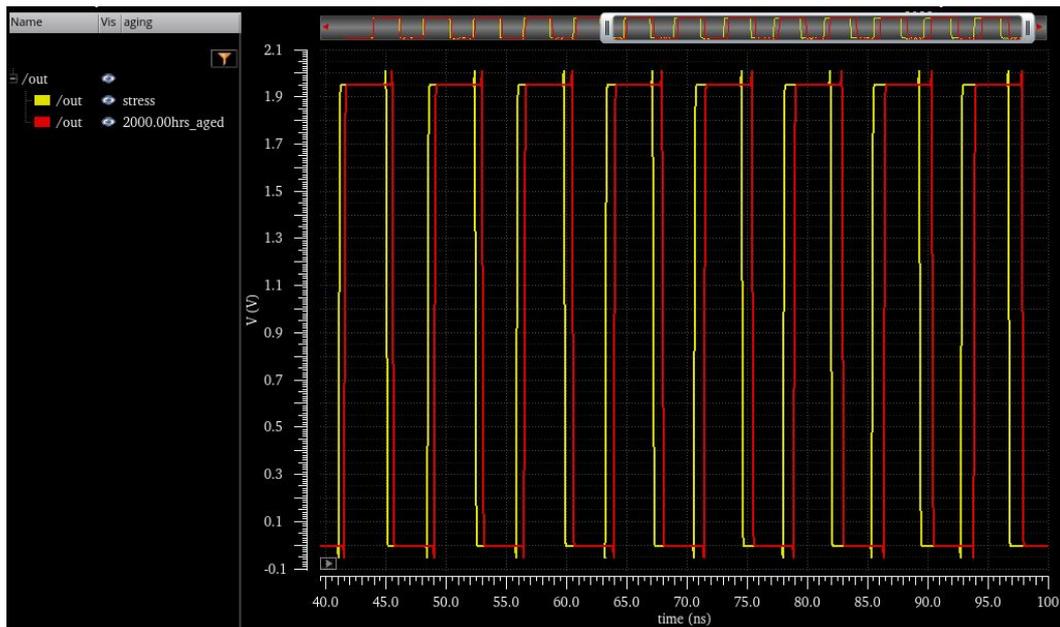


Figure 6.20: Reliability simulation result of output signal for RO_1 after 2,000h stress at 235°C and $V_{dd}=1.95V$

the degradation of each transistor depending on where it is located and how long stress condition is actually experienced in the circuit. Then, the lifetime of an individual transistor can be extrapolated. The C code for detailed implementation of transistor degradation and lifetime calculation can be found in Appendix B.

As in Figure 6.21, hundreds of transistors in RO_1 are listed in order of their hierarchy name as shown in *elem name*. The *Lifetime* is extrapolated and defined in years to reach the specific value of threshold voltage shift ΔV_{th} which is used as failure criterion. This ΔV_{th} value depends on the user, as in Figure 6.21, we define failure criterion as 0.05V. If the threshold voltage is larger than 0.05V, the transistor is considered to fail. *Degr*d is the degradation value (ΔV_{th}) after a specific stress time. *Age* is the age rate which have not integrated to the URI library yet, therefore, the column Age defaults to zero. *Age level* is related to type of aging mechanisms that transistor experienced. We have defined in the C code that AgeLevel=103 corresponds to CHE mechanism in nMOS, and AgeLevel=104 corresponds to NBTI mechanism in pMOS.

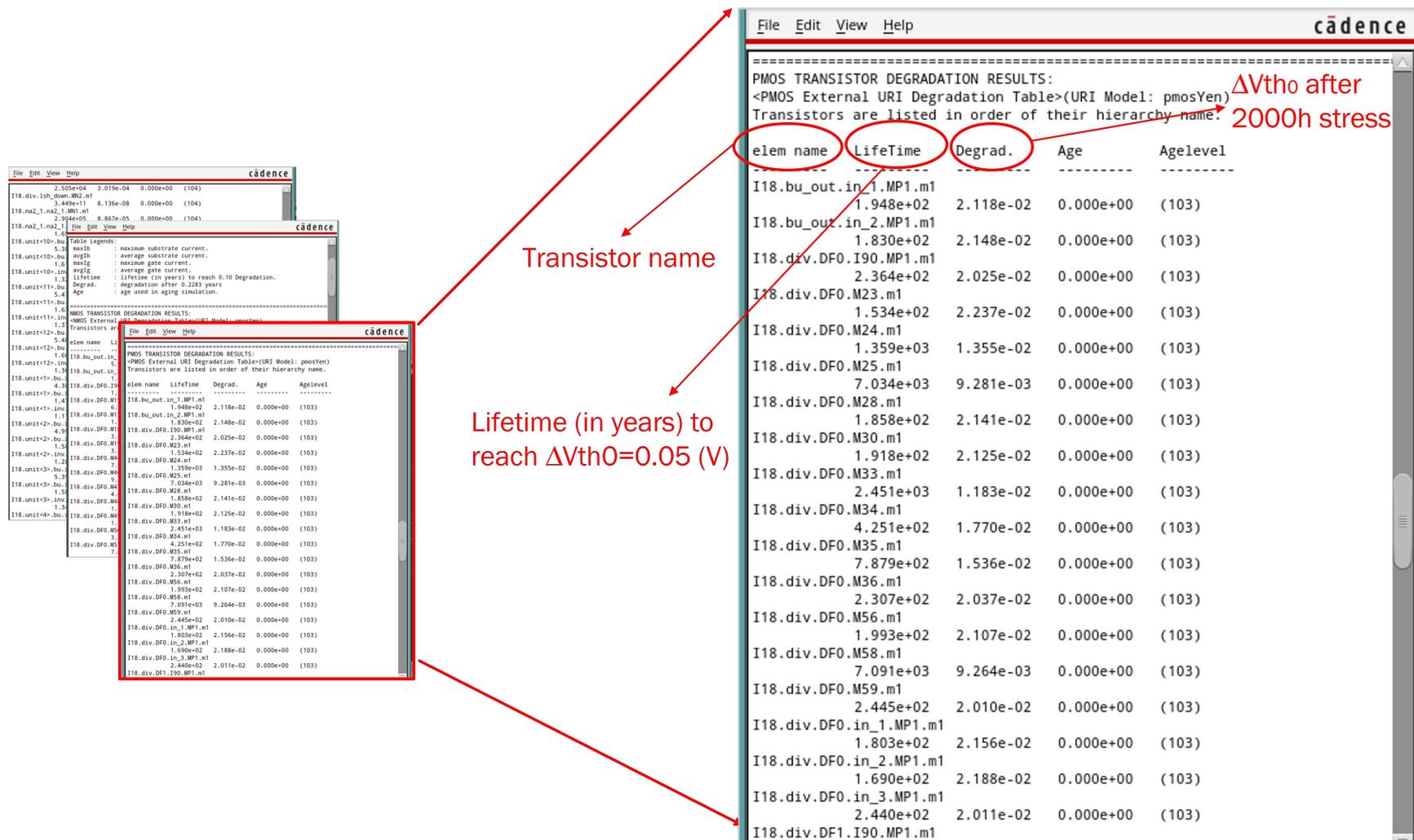


Figure 6.21: Reliability simulation data of RO_1 at 235°C and 2,000 hours stress.

Figure 6.22 shows the typical switching behavior of an inverter in RO. For high input signal $V_{in}=V_{dd}$, the output switches to $V_{out}=V_{ss}$, and vice versa. During the steady state, one device of the inverter is turned ON and operates in deep region with $|V_{gs}|=V_{dd}$ and $|V_{ds}|=0V$. The other is turned OFF with $|V_{gs}|=0V$ and $|V_{ds}|=V_{dd}$. Therefore, during the steady state at $V_{in}=V_{dd}$, nMOS transistor is experienced PBTI stress condition while pMOS is OFF. At $V_{in}=V_{ss}$, pMOS transistor is experienced NBTI stress condition while nMOS is OFF. During the switching, there is a short period that nMOS and pMOS entering the HCI stress conditions. Based on our aging results at transistor level, PBTI in nMOS and HCI in pMOS can be negligible due to their minor impact. Taking into these results, when RO is in operation, pMOS experiences NBTI degradation in most of time compared to HCI degradation on nMOS.

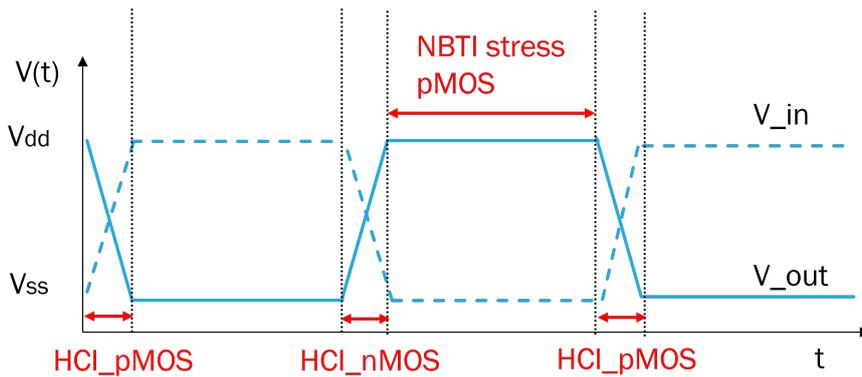


Figure 6.22: NBTI and HCI stress time window arising in inverter during RO operation

Figure 6.23 presents the schematic of inverter used in RO_1 and corresponding transistor degradation after running reliability simulation. The threshold voltage shift of pMOS (due to NBTI) is around 0.02 V, which is much larger than 0.000046 V of nMOS (due to HCI). This result is in agreement with the previous argument.

Furthermore, the reliability simulation can highlight the failed devices due to aging directly on the circuit schematic allowing designer can pay more attention to the vulnerable part of the circuit. First, designer defines the failure criterion as in Figure 6.24, i.e. $\Delta V_{th}=0.025V$ (just an example), then the transistor with the threshold voltage shift larger than 0.025V will be highlighted on the schematic (Figure 6.25A). Descending to the sub-circuit, the failed transistors can be found (Figure 6.25B-C). Zooming a failed transistor,

the stress time and corresponding degradation value is shown beside the transistor (Figure 6.25D).

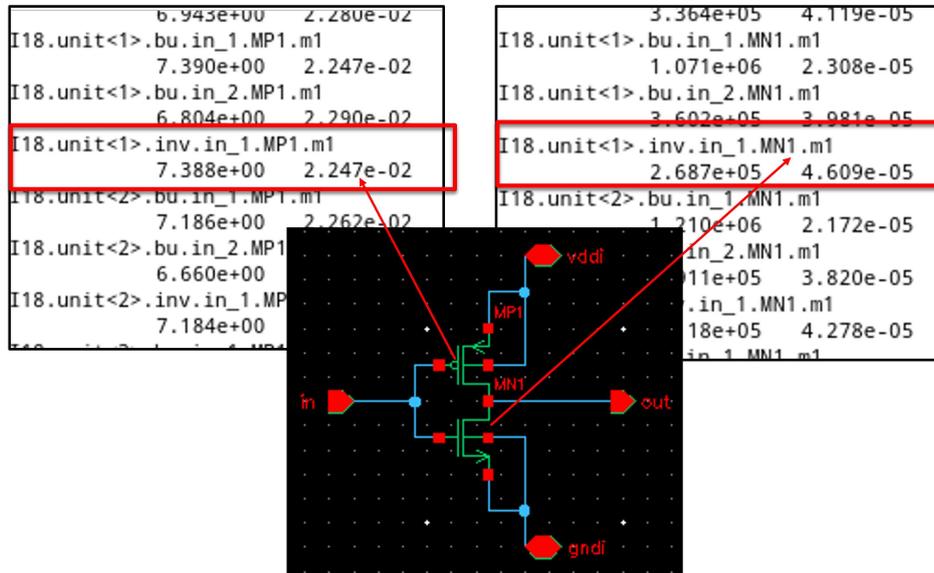


Figure 6.23: Schematic of an inverter in RO_1

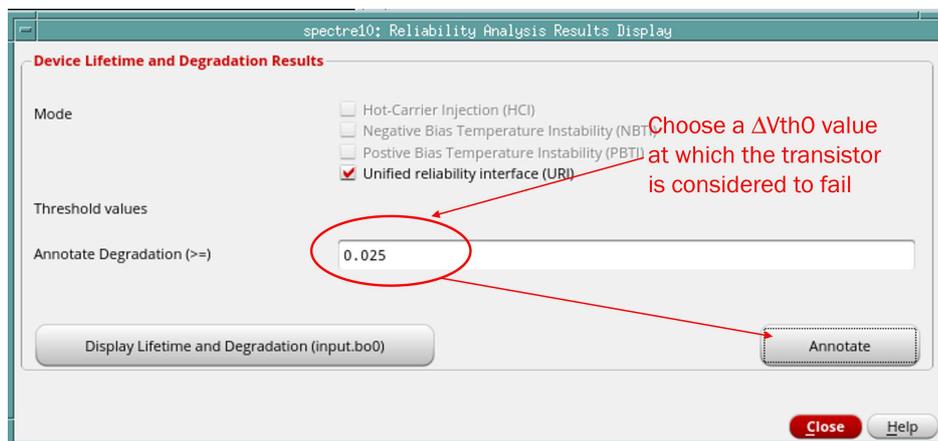


Figure 6.24: Reliability Analysis Result Display

According to reliability simulation, the transistors in the frequency divider tend to fail faster compared to other parts of the circuit depending on their own stress conditions.

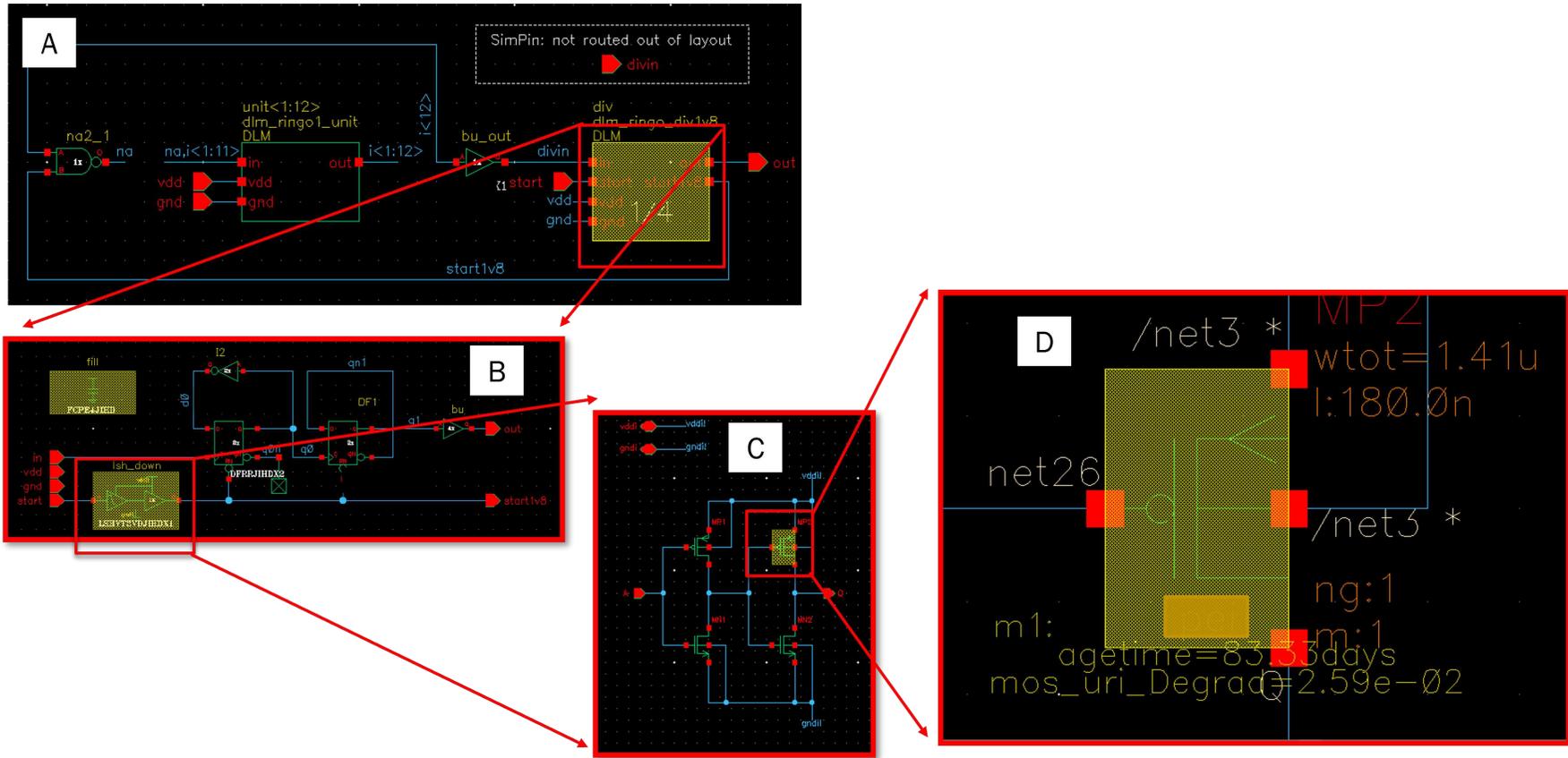


Figure 6.25: The transistor which meets the failure criteria is highlighted on the circuit schematic.

6.3.4 Validation of reliability models

It has been reported that aging degradation can cause the reduced and unstable oscillation frequency of ring oscillators. Therefore, the aged frequency measurements on three samples of each RO type will be presented hereafter. Aging conditions for ROs have been listed in Table 6.1 previously. The comparisons between aged measurements and aged simulation are in excellent agreement that validating our proposed reliability models for SPECTRE® simulator that presented in Figure 6.26, Figure 6.27, Figure 6.28, Figure 6.29 . In these figures, the frequency measurement and simulation data are collected at 2h, 20h, 200h and 2000h stress.

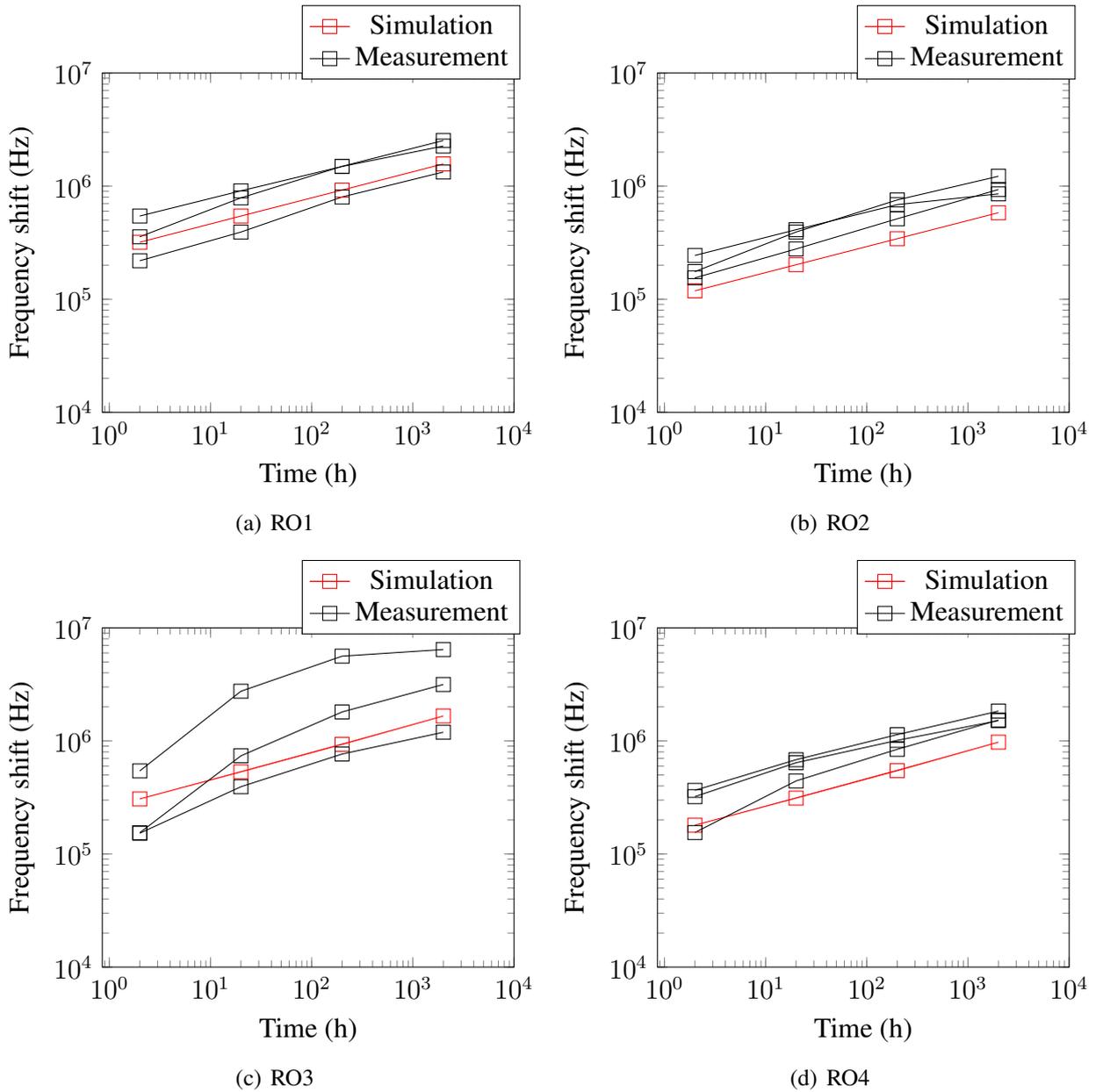


Figure 6.26: Comparison of aged measurements and simulation results of RO_1 to RO_4.

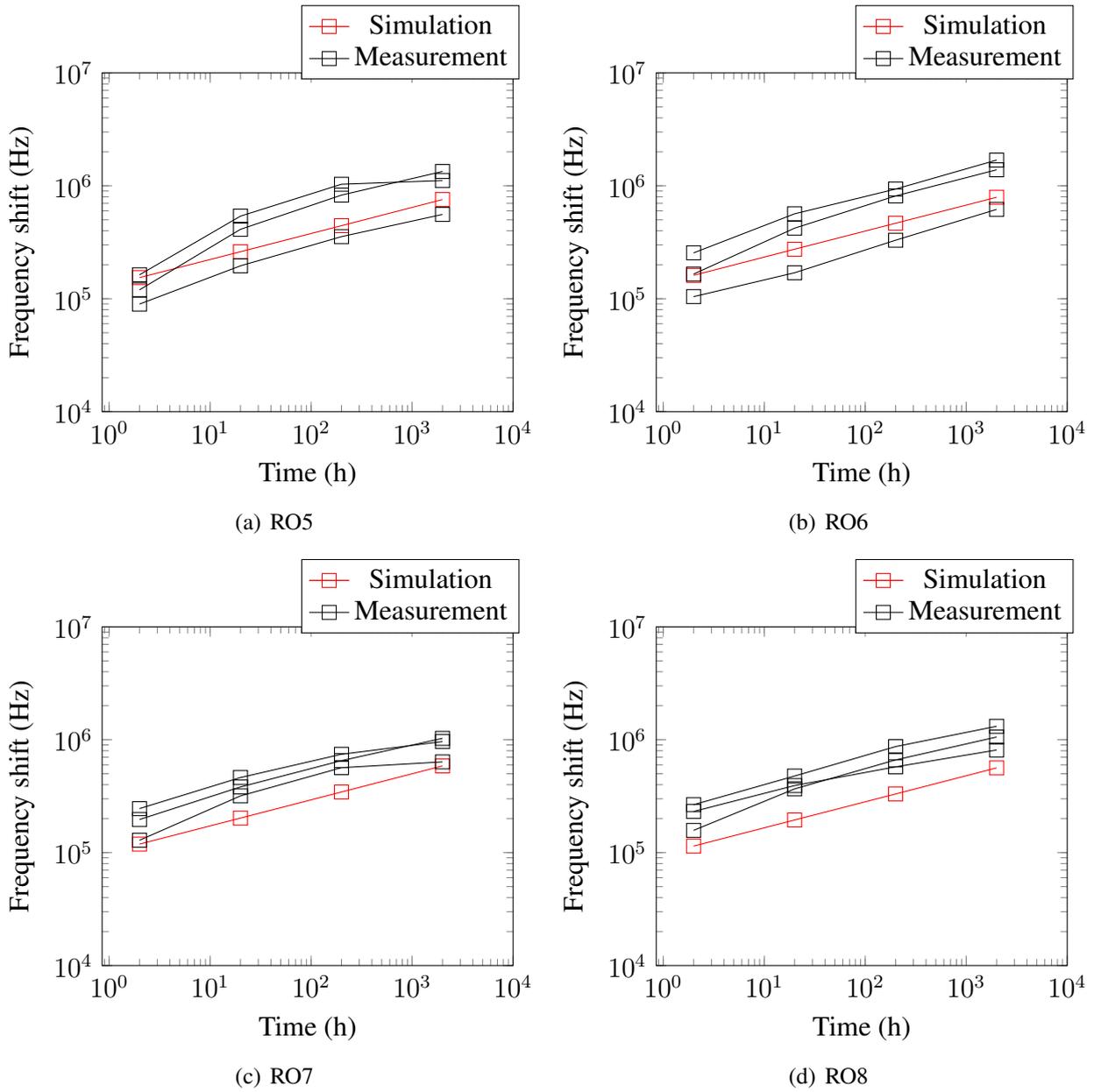


Figure 6.27: Comparison of aged measurements and simulation results of RO_5 to RO_8.

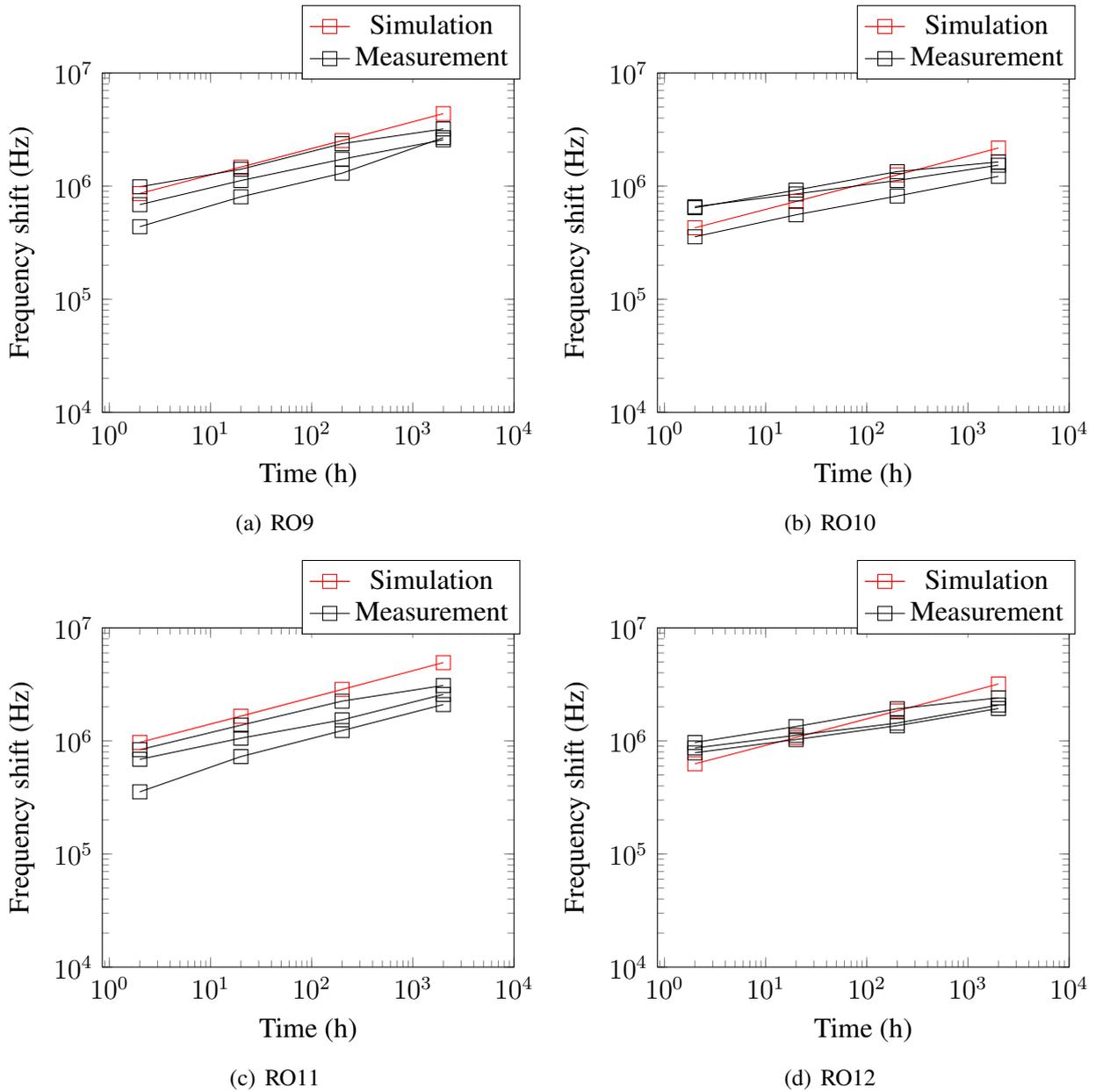


Figure 6.28: Comparison of aged measurements and simulation results of RO_9 to RO_12

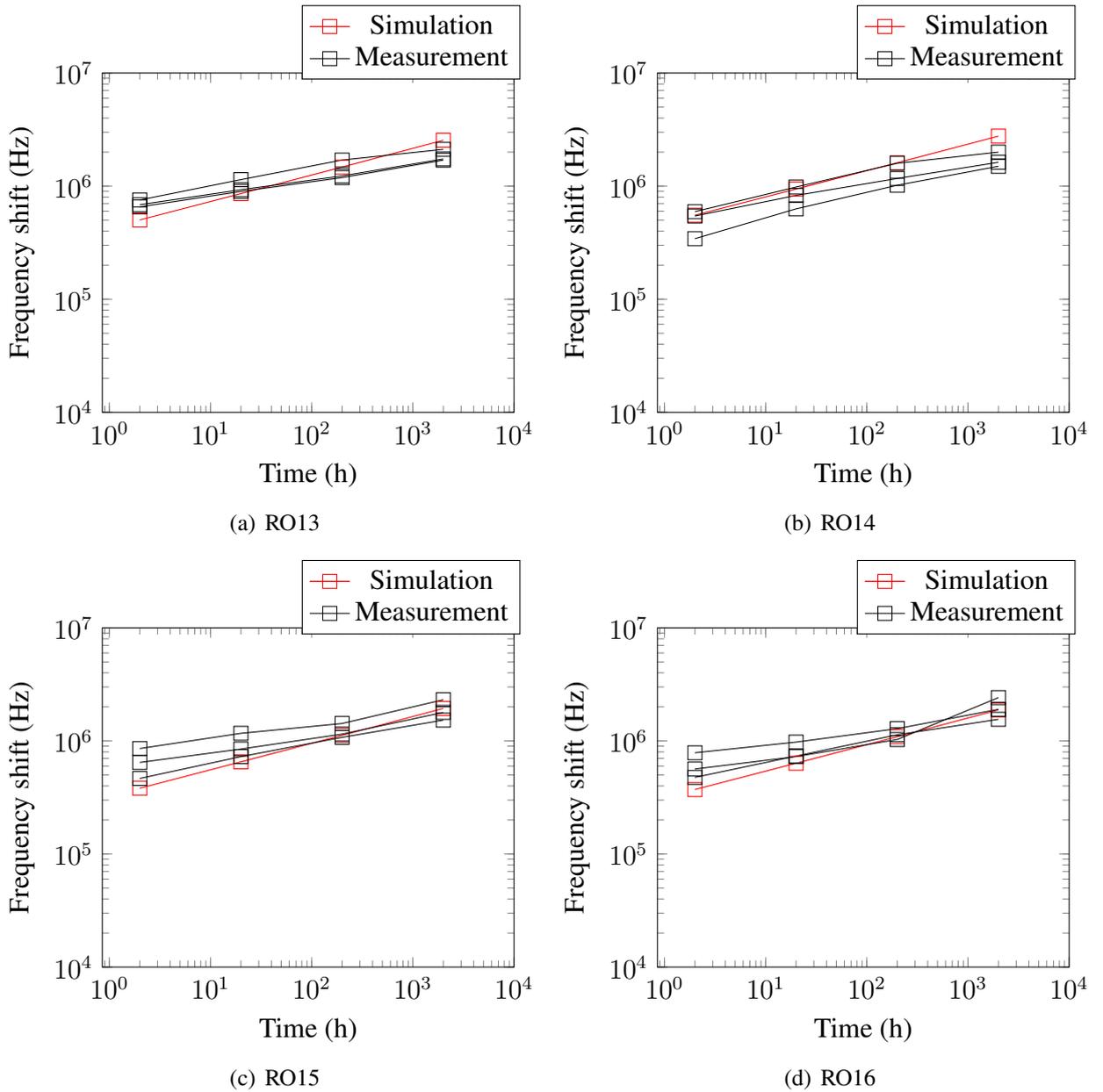


Figure 6.29: Comparison of aged measurements and simulation results of RO_13 to RO_16

6.4 Conclusion

Apart from establishing the reliability models, we have investigated the circuit degradation due to NBTI and HCI in order to provide the foundations for reliability simulation. To verify our model, we simulated circuits under NBTI and HCI conditions and compared the predicted characteristic shift to the one obtained from experiments. The reliability simulations shown a good agreement with the aged measurements, as well as its computational efficiency, making it appropriate for use as a reliability prediction tool in reliability-aware designs for target lifetime. Furthermore, the failed transistors in a circuit can be highlighted in the schematic level, allowing designers to deal with reliability issue at the early design phase.

7 | General conclusions and perspectives

The continuous downscaling of CMOS technology has posed challenges for reliability investigation. Electric fields and current densities of scaled transistors are more and more approaching their maximum values required for reliable operation. Although transistor failure mechanisms have been extensively researched for the last decades, the scope of investigations in operating conditions is still limited to conventional application domains involving mass markets. Some application areas requiring harsh working conditions at severe temperatures are rarely investigated, even though the associated electronic circuits turned out to be crucial for the application.

This PhD work included a broad study of the reliability of $0.18\mu\text{m}$ and $0.35\mu\text{m}$ technologies. We have performed the intensive aging test campaign to investigate a wide range of intrinsic wear-out mechanisms, such as CHE, DAHC, PBTI in nMOS, and CHH, NBTI in pMOS. Our experiments are long-term tests in which we investigated the degradations at the operating voltages with a stress time of up to 2,000 hours. Based on the experimental results, on $0.18\mu\text{m}$ technology, CHE and NBTI are dominant, especially at extreme temperatures, while PBTI and DAHC have a negligible impact. On the contrary, on $0.35\mu\text{m}$ technology, only NBTI is considered the most severe problem compared to other mechanisms such as CHE and PBTI. The experiments also highlighted the critical role of elevated temperature and device dimension dependencies contributing to aging.

A set of mathematical equations of the proposed aging model based on the dependencies of gate length, voltage biases, temperature, and stress time has shown to be an excellent ability to reproduce the experimental observations. The degradations follow a power law, which is a very well-known law. Despite its simplicity, it offers a reasonable estimation for the degradation and lifetime of devices, as well as the ability to integrate into the SPECTRE simulator. In our case, NBTI and CHE degradations of MOSFETs are described as a changing threshold voltage V_{th} following power law. Therefore, we can take advantage of the BSIM3v3 compact model, which is a threshold-voltage-based model, to add this shift to the threshold-voltage parameter in order to achieve the desired impact on the I–V curves. When evaluating

degraded I–V curves, it is commonly reported that the degradation behaviors are complicated and have been described using more than one compact model parameter. However, we have found that capturing the threshold voltage shift is enough to reproduce NBTI and HCI degradations. Moreover, keeping the reliability simulation model simple and minimizing the extra simulation time to a minimum value is preferable.

Our suggested models of reliability are relevant for DC stress conditions. However, the vast majority of actual circuits operate with time-varying bias conditions. As a result, we used quasi-static approximation to build a realistic DC-to-transient translation giving the opportunity to accurately simulate the circuit under dynamic stress.

Based on scalable reliability models, the aging laws integrated into the SPECTRE[®] simulator have demonstrated excellent accuracy at both single transistor and complex circuit levels. During this thesis work, several integrated circuits have been used to study the aging impacts: 3.3V inverters using 0.35 μ m CMOS technology, 1.8V Ring Oscillators using 0.18 μ m CMOS technology, and 3.3V Ring Oscillators using 0.35 μ m CMOS technology. These reliability models have been validated for various stress (voltages and temperatures) and geometry conditions, confirming their accuracy. Furthermore, the failure devices can be indicated directly on the circuit schematic, allowing designers to pay more attention to the vulnerable parts due to wear-out mechanisms during the early design phase.

To pursue this study, there are a few suggestions for further development in the future. Our reliability models following power law may be used to predict the lifetime of a transistor under normal working conditions. However, there is still a possibility that a slight uncertainty in the experimentally extracted parameters (e.g., the time exponent n) would result in an under- or overestimation of the product lifetime. Although we observed from the aging tests that the power-law time slope n is a temperature-dependent parameter, the dedicated model for n has not been established yet. We have taken the raw value of n extracted from experiments for reliability models. The validation of reliability models at the circuit level has shown excellent agreement with the aging measurements after 2,000 hours; however, for confident lifetime prediction under permanent application for oil production monitoring, it is crucial to define the relationship of power-law time slope n with temperatures, device dimensions and also NBTI recovery effect.

We have implemented several aging models into SPECTRE[®] simulator: CHE and DAHC models for 1.8V nMOS, NBTI models for 1.8V pMOS, NBTI models for 3.3V. Because PBTI in both 1.8V and 3.3V nMOS, CHH in 3.3V pMOS have little impact on transistor characteristics after 2,000 hours of applying stresses, we have skipped them. However, these mechanisms may become serious in the future node technologies, where the gate length and oxide layer are scaled significantly. In the future, we can model and integrate these mechanisms into the circuit simulator to widely investigate the electrical behavior of a circuit due to aging. In this scenario, further study is required on the combination of different mechanisms on a device, for instance, the interaction between NBTI and CHH in a pMOS [160], [161].

It is accepted that NBTI degradation is challenging to investigate due to its recovery behavior. According to several published papers, NBTI degradation consists of recoverable and permanent components. However, it is still controversial whether the permanent component is permanently damaged or eventually recovering with given enough "off" time. Furthermore, there are limited studies on the NBTI recovery rate at elevated temperatures. For a more accurate estimation of the circuit degradation, the model for NBTI recovery can be developed in the future.

Process variation has become an unavoidable issue in scaled devices, and the problem worsens with each new node. To predict the device specification shift over a long operation, it is essential to consider how process variation will impact the circuit lifetime. It is accepted that wear-out mechanisms are closely related to gate thickness which varies device to devices. Process variability is an inherent property of the devices we are dealing with, which cannot be eliminated during fabrication. The process variation leads to a time-dependent variability of aging results, making lifetime prediction more difficult. Therefore, we are developing in our team a reliability Monte Carlo (MC) simulation that considers the statistical effects of process variation on aging variation. The reliability MC simulation flow is demonstrated in Figure 7.1 that can predict the aging variation using current foundry MC model and our reliability models.

Last but not least, although RelXpert (Cadence) has offered the possibility to run reliability simulations at the circuit level, its capabilities are limited to CMOS circuits. On

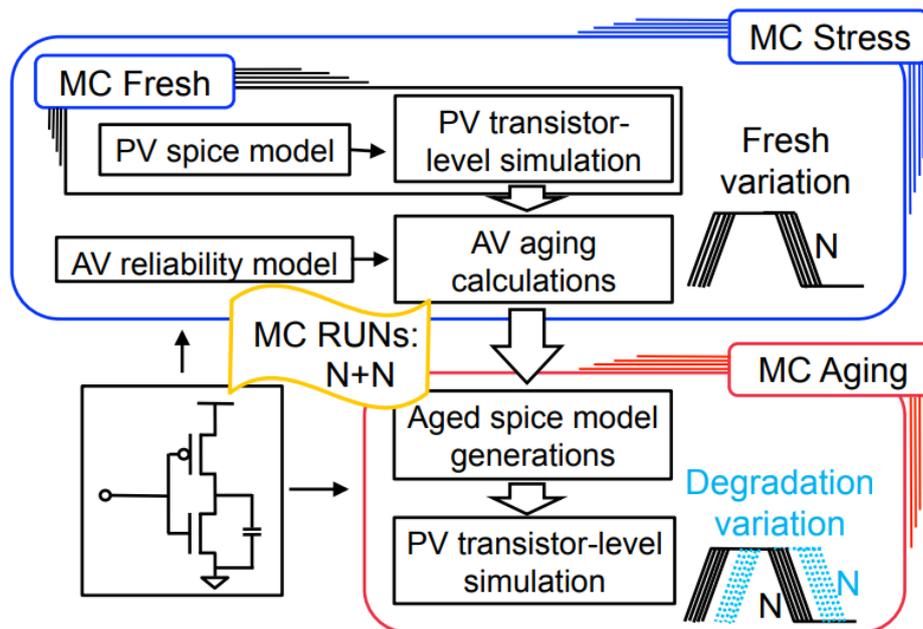


Figure 7.1: The reliability Monte Carlo (MC) simulation flow with process variation (PV) and age variation (AV) [162].

the one hand, our reliability models are customized for given CMOS technologies; therefore, they can give a degradation prediction with higher confidence. On the other hand, developing new reliability models for new devices and implementing them into SPECTRE® is possible. Some devices such as HKMG, ET-SOI, and FinFETs are generally based on the same structure compared to MOSFET; they may experience a similar aging pattern. Therefore, similar aging models with minor modifications can be applied to these devices. Thanks to the available SPECTRE simulator, Schlumberger can develop their own reliability tool to deal with aging issues in the future, not limited to bulk planar CMOS but to various types of devices.

Appendix A

The initial characterization were performed using probe station at 25, 50, 125, 175, 200 and 230 °C. The detailed results on several geometries are presented below.

Initial characterization results

❖ Four types of MOSFETs and two sizes of each type are used as devices under test. DC characterizations were performed at 6 different temperatures: 25°C, 50°C, 125°C, 175°C, 200°C, and 230°C. At least 10 devices were tested to evaluate the process deviation.

Device	W/L	Quantity
1.8V isolated nMOS	10um/0.18um	10 devices
	10um/0.5um	10 devices
3.3V isolated nMOS	10um/0.35um	10 devices
	10um/0.5um	10 devices
1.8V isolated pMOS	10um/0.18um	10 devices
	10um/0.5um	10 devices
3.3V isolated pMOS	10um/0.3um	10 devices
	10um/0.6um	10 devices

❖ Key figures of merit of the MOS device were recorded to compare with the simulation results:

- $V_{THcc} = V_{gs}$ at $I_{ds} = W/L \times 100nA$, $V_{bs} = 0V$, $V_{ds} = 100mV$
- $I_{Dlin} = I_{ds}$ at $V_{gs} = V_{gsmax}$, $V_{bs} = 0V$, $V_{ds} = 100mV$
- $I_{Dsat} = I_{ds}$ at $V_{gs} = V_{gsmax}$, $V_{bs} = 0V$, $V_{ds} = V_{dsmax}$

❖ The gate currents have very small values (around 1-2 pA) and these values do not change much at different temperatures, therefore, gate currents are not shown.

1.8V nMOS_ W/L = 10 μ m/0.18 μ m

1.8V nMOS_10 μ m/0.18 μ m												
	T°C	Simula- -tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device #10
VTHcc (V)	25°C	0.58	0.59	0.59	0.57	0.57	0.59	0.57	0.59	0.58	0.57	0.57
	50°C	0.56	0.57	0.57	0.56	0.56	0.57	0.55	0.56	0.56	0.55	0.55
	125°C	0.49	0.50	0.50	0.48	0.49	0.50	0.48	0.49	0.49	0.48	0.48
	175°C	0.45	0.45	0.45	0.43	0.44	0.44	0.43	0.44	0.44	0.43	0.43
	200°C	0.43	0.4	0.38	0.37	0.39	0.38	0.39	0.39	0.39	0.38	0.39
	230°C	0.4	0.36	0.34	0.34	0.35	0.34	0.35	0.35	0.34	0.34	0.35
IDlin (mA)	25°C	1.29	1.11	1.13	1.15	1.19	1.09	1.23	1.14	1.19	1.22	1.23
	50°C	1.20	1.05	1.08	1.13	1.11	1.05	1.13	1.05	1.12	1.14	1.15
	125°C	0.97	0.86	0.89	0.94	0.93	0.88	0.95	0.88	0.94	0.96	0.97
	175°C	0.85	0.77	0.79	0.83	0.83	0.78	0.84	0.79	0.83	0.85	0.86
	200°C	0.79	0.67	0.77	0.78	0.72	0.75	0.73	0.68	0.54	0.55	0.53
	230°C	0.74	0.60	0.35	0.69	0.66	0.64	0.67	0.63	0.67	0.68	0.67
IDSat (mA)	25°C	4.76	4.13	4.19	4.40	4.36	4.15	4.46	4.17	4.38	4.49	4.52
	50°C	4.61	3.97	4.05	4.28	4.21	4.01	4.29	4.02	4.25	4.34	4.38
	125°C	4.18	3.61	3.67	3.90	3.85	3.66	3.94	3.66	3.87	3.96	3.99
	175°C	3.91	3.39	3.45	3.66	3.62	3.44	3.70	3.43	3.65	3.73	3.76
	200°C	3.80	3.22	3.59	3.67	3.39	3.52	3.50	3.24	2.79	2.39	2.98
	230°C	3.64	3.03	3.16	3.41	3.26	3.24	3.12	3.09	3.26	3.33	3.19

Table 1: Key figures of merit of the MOSFETs extracted from I-V curves.

1.8V nMOS_10 μ m/0.18 μ m												
	T°C	Simula- -tion	Device #1	Device #2	Device# 3	Device #4	Device #5	Device #6	Device# 7	Device #8	Device #9	Device #10
Ibmax (nA) @Vds=1.8	200°C	151	536	9405	744	853	10992	665	540	498	1955	471
	230°C	132	631	575	830	756	772	757	636	793	835	707

Table 2: Body currents of MOSFETs extracted from Ibs - Vgs curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
IDlin (mA)	25°C	1.09	1.23	1.168	0.044	3.8 %	10.4 %
	50°C	1.05	1.15	1.101	0.0348	3.2 %	9.0 %
	125°C	0.86	0.97	0.92	0.034	3.7 %	5.4 %
	175°C	0.77	0.83	0.805	0.0276	3.4 %	5.6 %
	200°C	0.53	0.78	0.67	0.082	12.2 %	17.9 %
	230°C	0.36	0.69	0.62	0.059	9.5 %	19.4 %
IDsat (mA)	25°C	4.13	4.52	4.325	0.132	3.1 %	10.1 %
	50°C	3.97	4.38	4.18	0.134	3.2 %	10.3 %
	125°C	3.61	3.99	3.811	0.1288	3.4 %	9.7 %
	175°C	3.39	3.76	3.583	0.1244	3.5 %	9.1 %
	200°C	2.39	3.67	3.23	0.31	9.6 %	17.6 %
	230°C	3.03	3.41	3.21	0.09	2.8 %	13.4 %

Table 3: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value

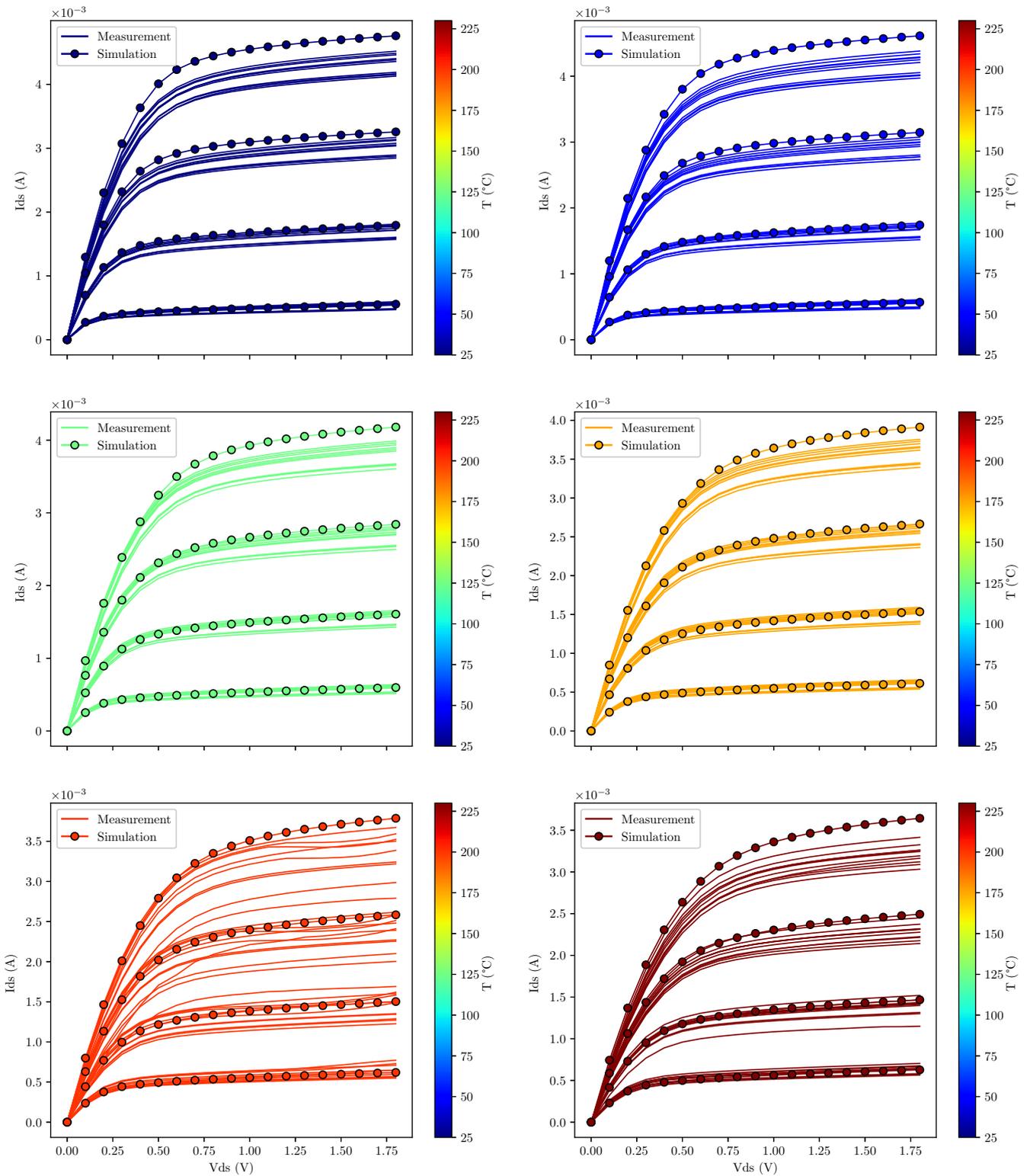


Figure 2: $I_{ds} - V_{ds}$ curves of 1.8V nMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures. The values of V_{gs} are 0.9V, 1.2V, 1.5V, 1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

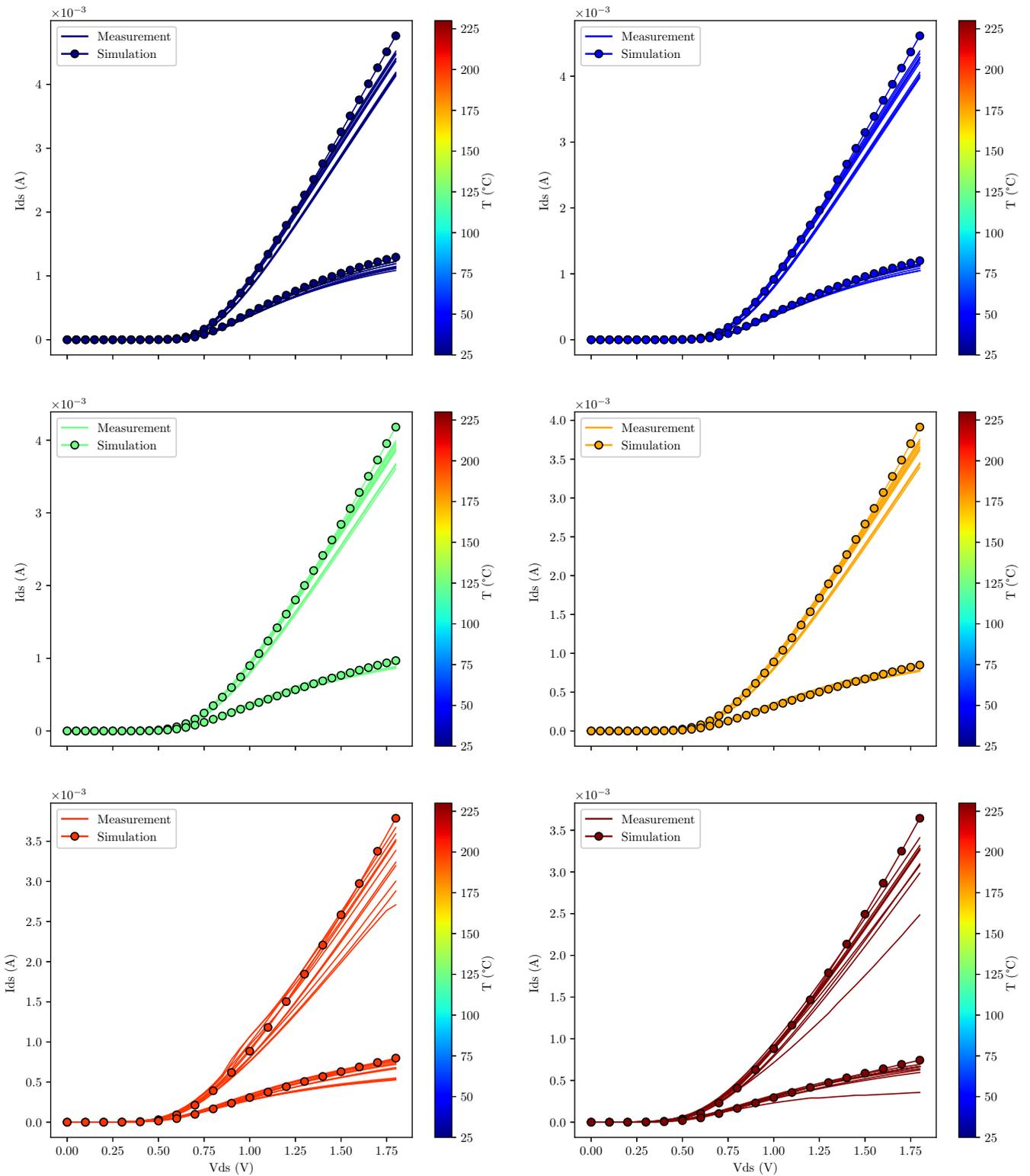


Figure 3: $I_{ds} - V_{gs}$ curves of 1.8V nMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures. Values of V_{ds} are 0.1V and 1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

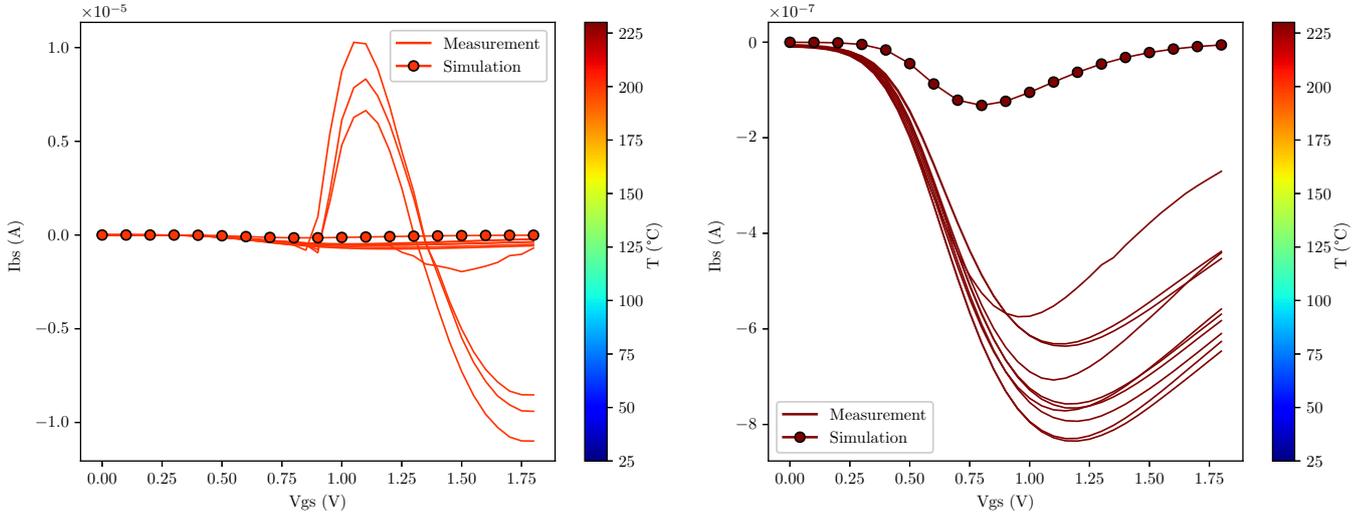


Figure 4: $I_{bs} - V_{gs}$ curves of 1.8V nMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures and $V_{ds}=1.8\text{V}$. The color indicates the according temperature.

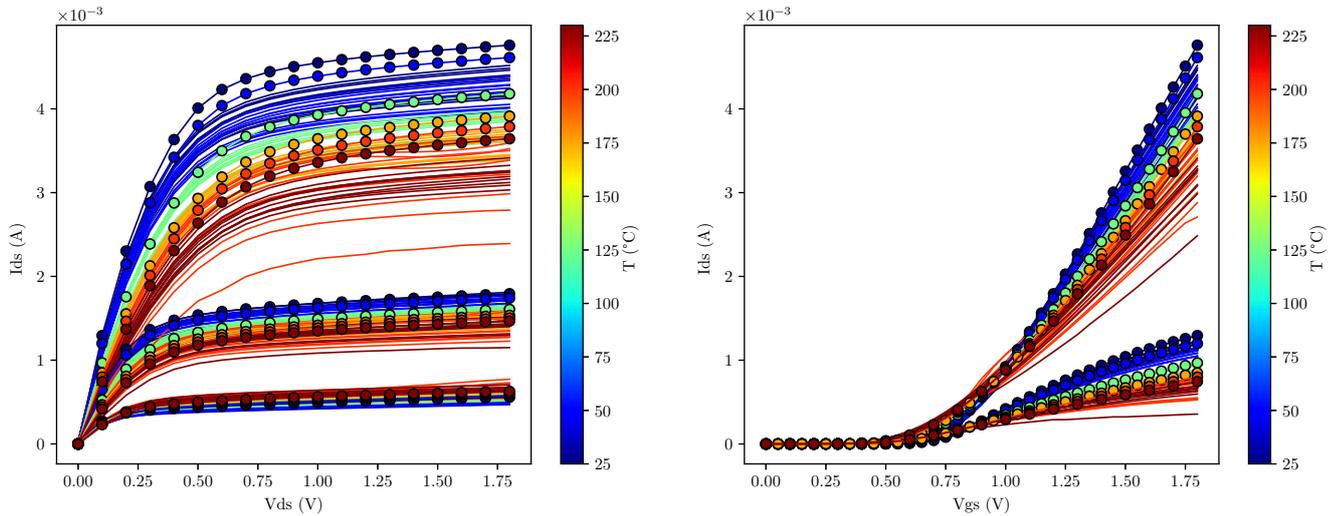


Figure 5: Comparisons of measurements (circle marks) and simulations (solid lines) of 1.8V nMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures. The color indicates the according temperature.

1.8V nMOS_ W/L = 10 μ m/0.5 μ m

1.8V nMOS_10 μ m/0.5 μ m												
	T $^{\circ}$ C	Simula- tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device #10
VTHcc (V)	25 $^{\circ}$ C	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.59	0.6	0.6	0.6
	50 $^{\circ}$ C	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6
	125 $^{\circ}$ C	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.54	0.54
	175 $^{\circ}$ C	0.49	0.49	0.49	0.49	0.49	0.49	0.49	0.49	0.49	0.49	0.49
	200 $^{\circ}$ C	0.48	0.42	0.42	0.43	0.43	0.42	0.42	0.42	0.42	0.43	0.43
	230 $^{\circ}$ C	0.43	0.38	0.39	0.39	0.39	0.38	0.39	0.38	0.38	0.38	0.39
IDlin (mA)	25 $^{\circ}$ C	0.44	0.40	0.39	0.41	0.41	0.41	0.41	0.40	0.41	0.41	0.41
	50 $^{\circ}$ C	0.40	0.37	0.38	0.38	0.38	0.37	0.38	0.37	0.38	0.38	0.38
	125 $^{\circ}$ C	0.30	0.29	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
	175 $^{\circ}$ C	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26
	200 $^{\circ}$ C	0.24	0.23	0.24	0.24	0.23	0.24	0.23	0.22	0.21	0.10	0.22
	230 $^{\circ}$ C	0.22	0.21	0.21	0.22	0.21	0.22	0.21	0.21	0.21	0.21	0.21
IDsat (mA)	25 $^{\circ}$ C	1.91	1.73	1.77	1.77	1.77	1.76	1.79	1.76	1.77	1.78	1.80
	50 $^{\circ}$ C	1.80	1.64	1.68	1.68	1.67	1.66	1.68	1.66	1.67	1.68	1.70
	125 $^{\circ}$ C	1.53	1.40	1.42	1.43	1.43	1.42	1.44	1.41	1.43	1.43	1.45
	175 $^{\circ}$ C	1.38	1.27	1.29	1.30	1.29	1.28	1.31	1.28	1.30	1.30	1.31
	200 $^{\circ}$ C	1.32	1.22	1.23	1.26	1.19	1.25	1.20	1.18	1.09	0.92	0.93
	230 $^{\circ}$ C	1.24	1.11	1.14	1.15	1.12	1.16	1.12	1.09	1.12	1.12	1.13

Table 4: Key figures of merit of the MOSFETs extracted from I-V curves.

1.8V nMOS_10 μ m/0.5 μ m												
	T $^{\circ}$ C	Simula- -tion	Device #1	Device #2	Device# 3	Device #4	Device #5	Device #6	Device# 7	Device #8	Device #9	Device #10
I _{bmax} (nA) @ V _{ds} =1.8V	200 $^{\circ}$ C	10.1	154	73	73	72	72	71	69	71	59	63
	230 $^{\circ}$ C	8.5	95	96	96	94	95	93	91	96	97	83

Table 5: Body currents of MOSFETs extracted from I_{bs} - V_{gs} curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
IDlin (mA)	25°C	0.39	0.41	0.406	0.0056	1.4 %	8.4 %
	50°C	0.37	0.38	0.377	0.0042	1.1 %	6.1 %
	125°C	0.29	0.30	0.299	0.0018	0.6 %	0.3 %
	175°C	0.26	0.26	0.26	0.0000	0.0 %	0.0 %
	200°C	0.10	0.24	0.22	0.024	11.3 %	9.1 %
	230°C	0.21	0.22	0.21	0.0033	1.6 %	4.8 %
IDSat (mA)	25°C	1.73	1.80	1.77	0.0120	0.7 %	7.9 %
	50°C	1.64	1.70	1.672	0.0120	0.7 %	7.7 %
	125°C	1.40	1.45	1.426	0.0108	0.8 %	7.3 %
	175°C	1.27	1.31	1.293	0.0110	0.9 %	6.7 %
	200°C	0.92	1.26	1.15	0.099	8.7 %	14.8 %
	230°C	1.09	1.16	1.13	0.015	1.3 %	9.7 %

Table 6: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value.

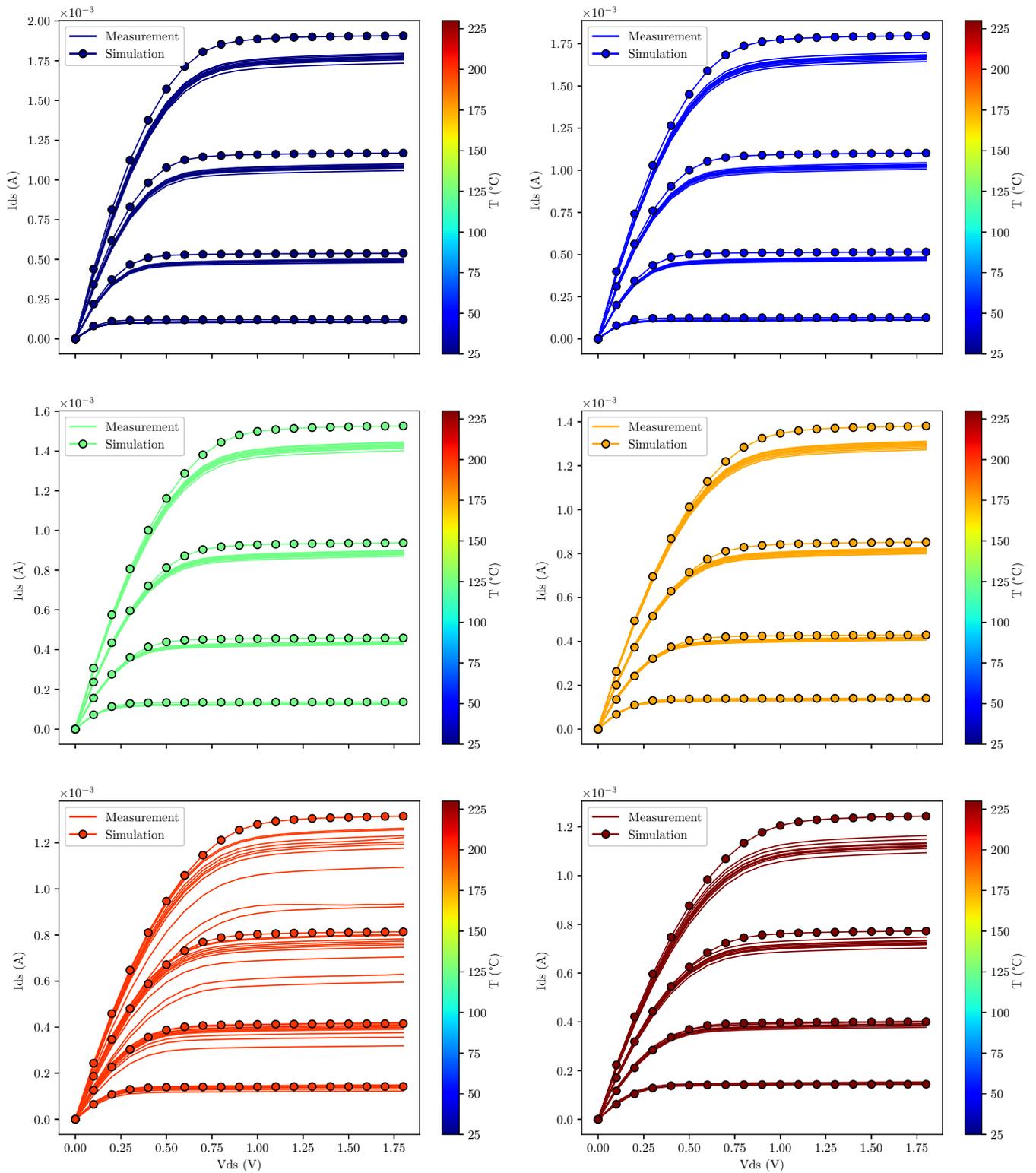


Figure 6: $I_{ds} - V_{ds}$ curves of 1.8V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures. The values of V_{gs} are 0.9V, 1.2V, 1.5V, 1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

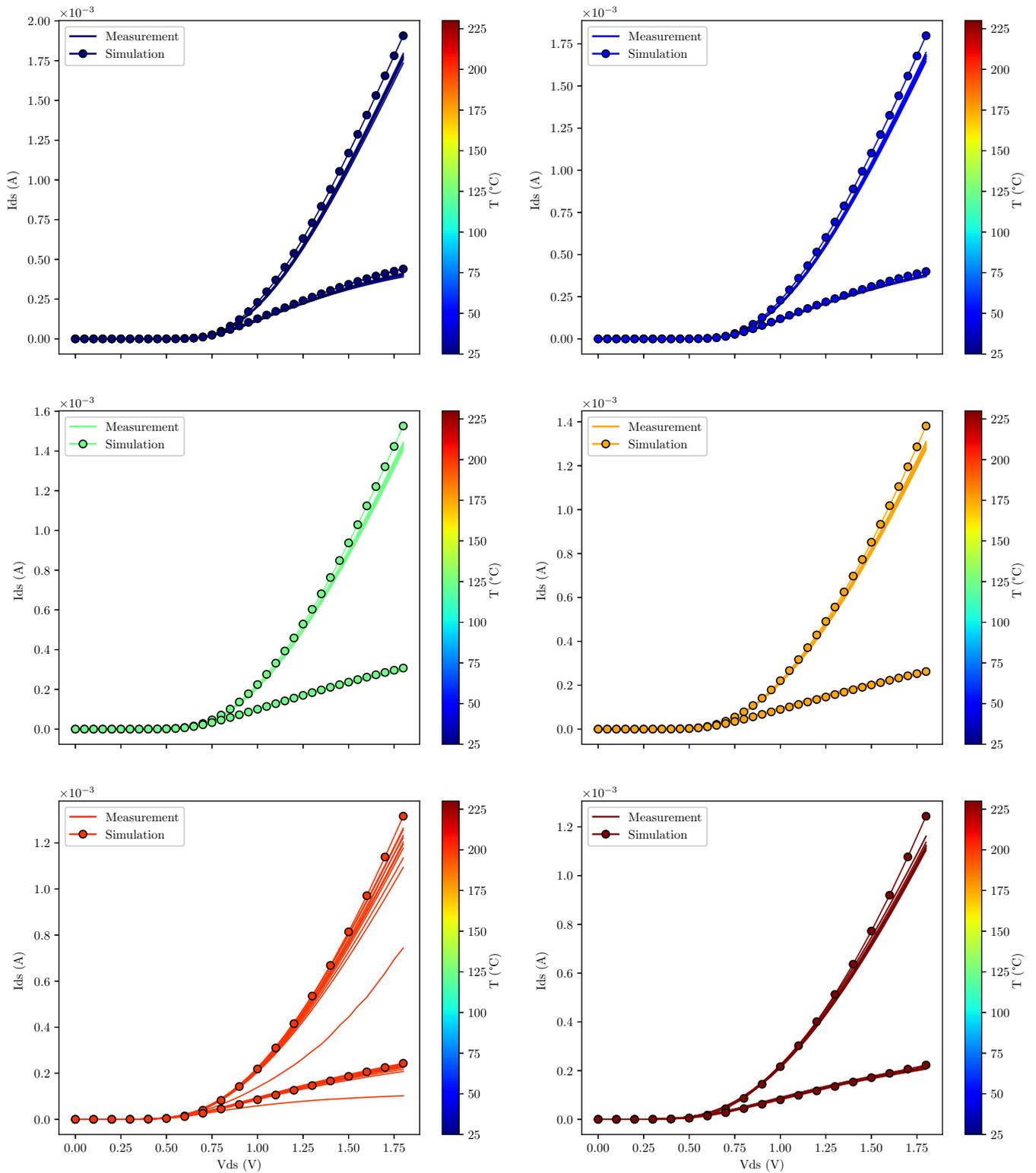


Figure 7: $I_{ds} - V_{gs}$ curves of 1.8V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures. Values of V_{ds} are 0.1V and 1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

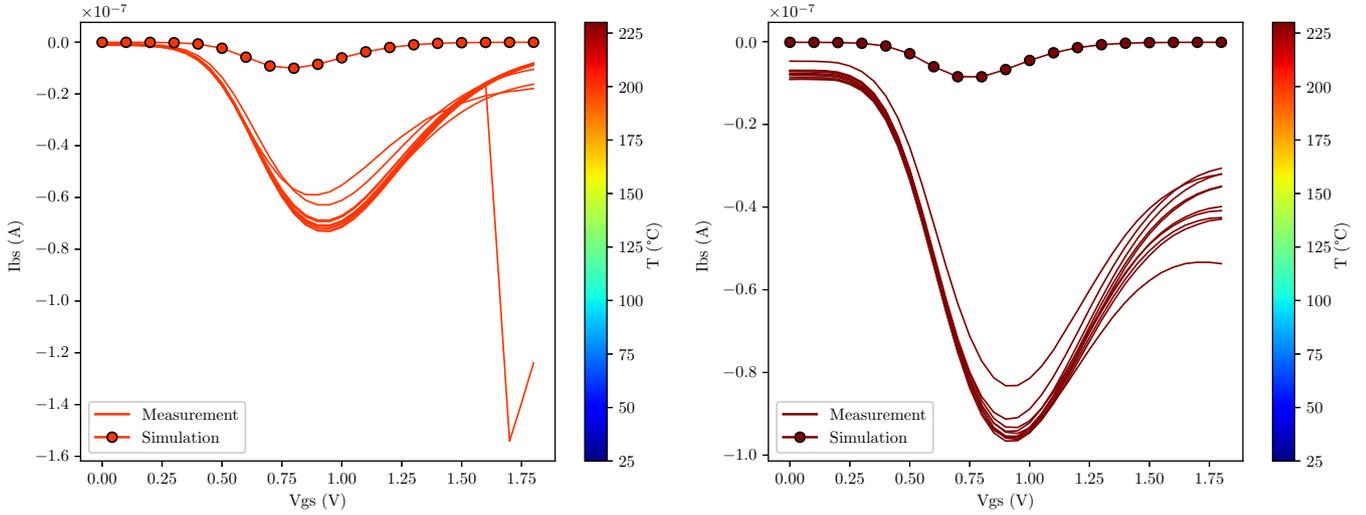


Figure 8: $I_{bs} - V_{gs}$ curves of 1.8V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures and $V_{ds}=1.8\text{V}$. The color indicates the according temperature.

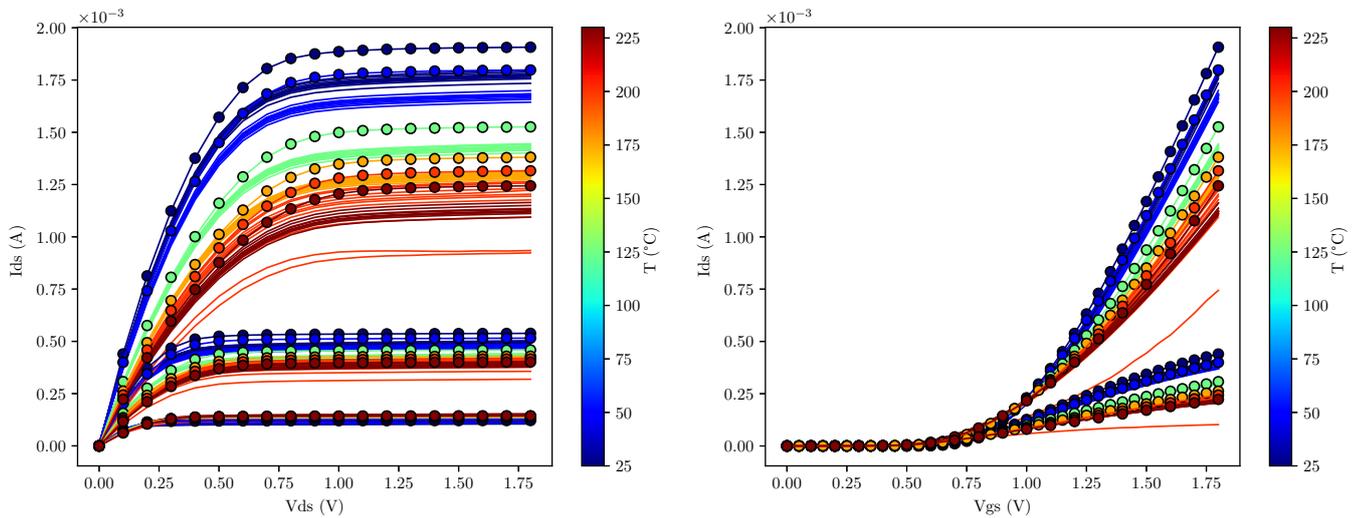


Figure 9: Comparisons of measurements (circle marks) and simulations (solid lines) of 1.8V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures. The color indicates the according temperature.

3.3V nMOS_ W/L = 10 μ m/0.35 μ m

3.3V nMOS_10 μ m/0.35 μ m												
	T°C	Simulation	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device #10
VTHcc (V)	25°C	0.66	0.72	0.72	0.71	0.71	0.72	0.71	0.71	0.70	0.71	0.70
	50°C	0.63	0.70	0.65	0.69	0.69	0.70	0.71	0.66	0.68	0.69	0.68
	125°C	0.55	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6	0.6
	175°C	0.50	0.55	0.55	0.55	0.55	0.55	0.55	0.55	0.55	0.54	0.55
	200°C	0.49	0.47	0.47	0.46	0.46	0.46	0.46	0.46	0.46	0.46	0.46
	230°C	0.46	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43
IDlin (mA)	25°C	0.75	0.71	0.72	0.73	0.73	0.71	0.74	0.71	0.73	0.74	0.72
	50°C	0.70	0.68	0.69	0.69	0.67	0.67	0.69	0.66	0.69	0.69	0.69
	125°C	0.57	0.56	0.57	0.58	0.58	0.57	0.58	0.56	0.58	0.58	0.58
	175°C	0.51	0.50	0.50	0.51	0.51	0.50	0.51	0.50	0.51	0.51	0.51
	200°C	0.48	0.41	0.42	0.43	0.42	0.42	0.42	0.41	0.37	0.18	0.38
	230°C	0.45	0.36	0.37	0.38	0.39	0.38	0.38	0.37	0.37	0.38	0.38
IDsat (mA)	25°C	6.18	5.47	5.49	5.58	5.57	5.46	5.61	5.45	5.62	5.63	5.59
	50°C	5.95	5.27	5.28	5.39	5.34	5.25	5.40	5.25	5.42	5.43	5.43
	125°C	5.31	4.70	4.71	4.81	4.79	4.70	4.82	4.69	4.84	4.86	4.86
	175°C	4.91	4.36	4.37	4.47	4.45	4.36	4.48	4.35	4.50	4.50	4.51
	200°C	4.73	4.11	4.19	4.25	4.23	4.23	4.22	4.08	3.84	3.33	3.97
	230°C	4.52	3.79	3.90	3.98	3.99	3.94	3.99	3.85	3.96	3.97	3.74

Table 7: Key figures of merit of the MOSFETs extracted from I-V curves.

3.3V nMOS_10 μ m/0.35 μ m												
	T°C	Simulation	Device #1	Device #2	Device# 3	Device #4	Device #5	Device #6	Device# 7	Device #8	Device #9	Device #10
I _{bmax} (nA) @ V _{ds} =3.3V	200°C	4540	5005	16370	5482	5437	5447	5339	4976	4897	3568	4975
	230°C	3970	4603	5096	5102	5137	5042	5041	4699	5112	5096	4825

Table 8: Body currents of MOSFETs extracted from I_{bs} - V_{gs} curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
IDlin (mA)	25°C	0.71	0.74	0.724	0.0100	1.4 %	3.6 %
	50°C	0.66	0.69	0.682	0.0096	1.4 %	2.6 %
	125°C	0.56	0.58	0.574	0.0072	1.3 %	0.7 %
	175°C	0.50	0.51	0.506	0.0048	0.9 %	0.8 %
	200°C	0.18	0.43	0.39	0.0450	11.7 %	23.1 %
	230°C	0.35	0.38	0.38	0.0082	2.19 %	18.4 %
IDsat (mA)	25°C	5.45	5.63	5.547	0.0636	1.1 %	11.4 %
	50°C	5.25	5.43	5.346	0.068	1.3 %	11.3 %
	125°C	4.69	4.86	4.778	0.0624	1.3 %	11.1 %
	175°C	4.35	4.51	4.435	0.0600	1.4 %	10.7 %
	200°C	3.33	4.25	4.04	0.1980	4.9 %	17.1 %
	230°C	3.74	3.99	3.91	0.0722	1.85 %	15.6 %

Table 9: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value.

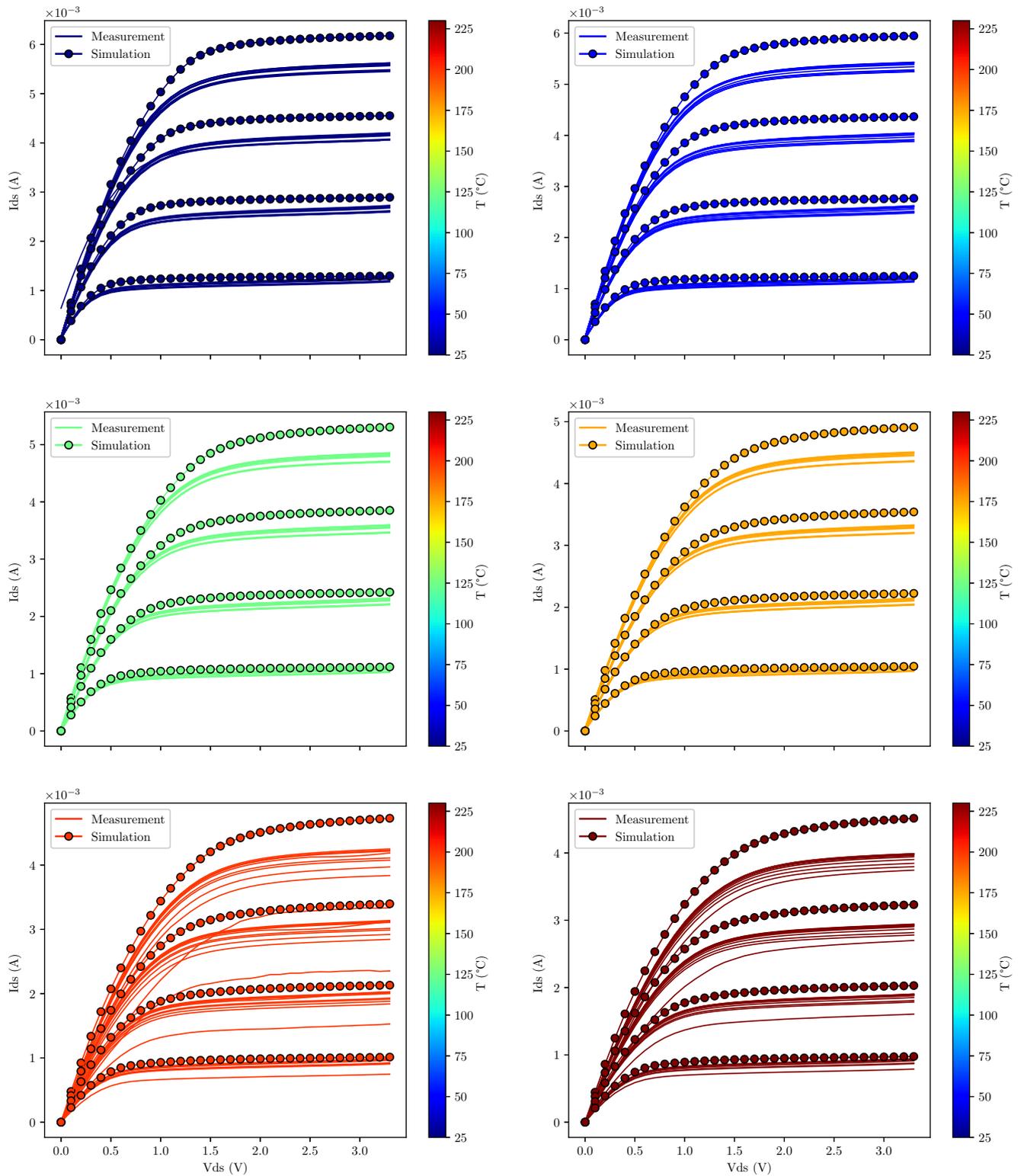


Figure 10: $I_{ds} - V_{ds}$ curves of 3.3V nMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures. The values of V_{gs} are 1.5V, 2.1V, 2.7V, 3.3V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

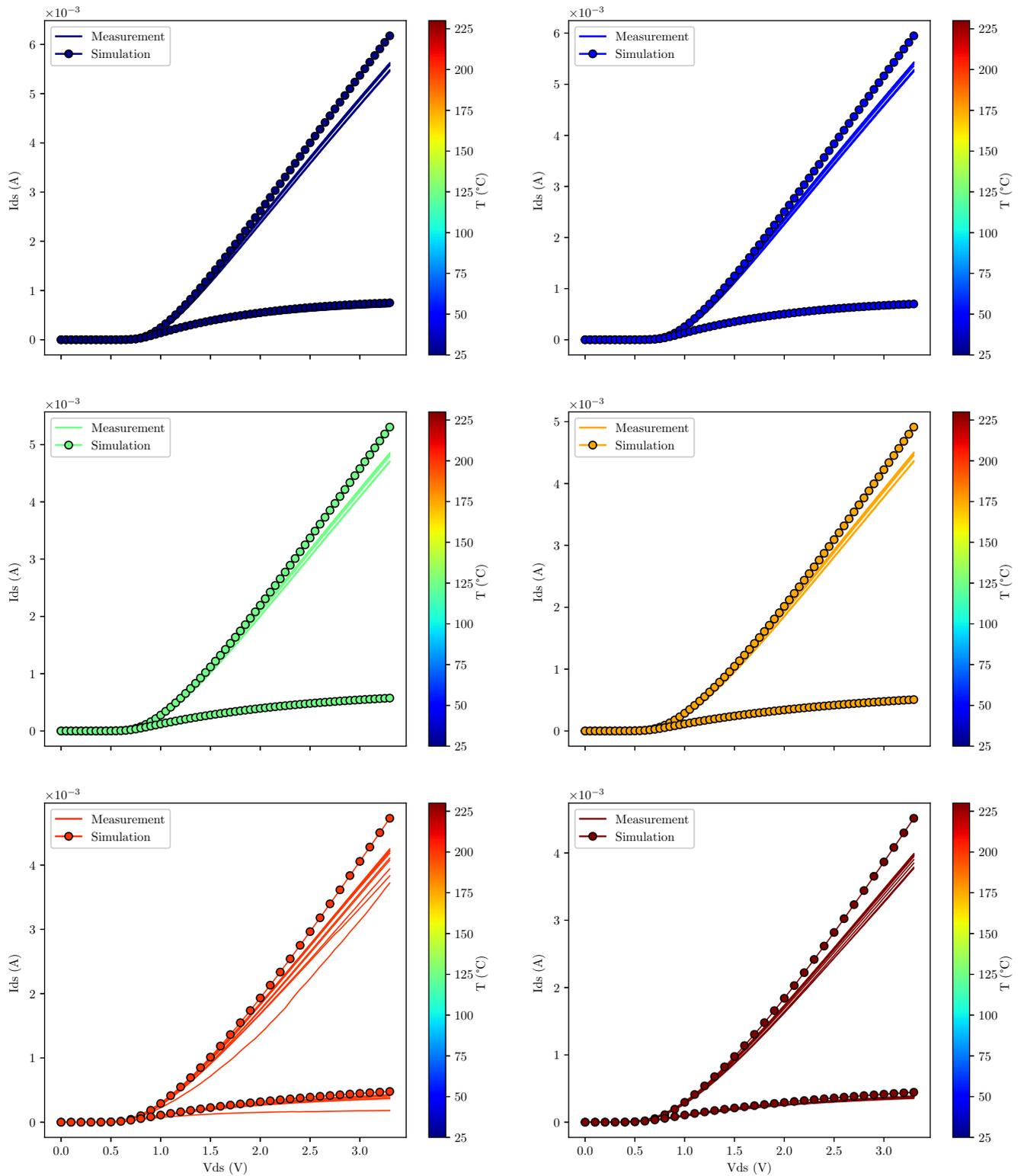


Figure 11: $I_{ds} - V_{gs}$ curves of 3.3V nMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures. Values of V_{ds} are 0.1V and 3.3V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

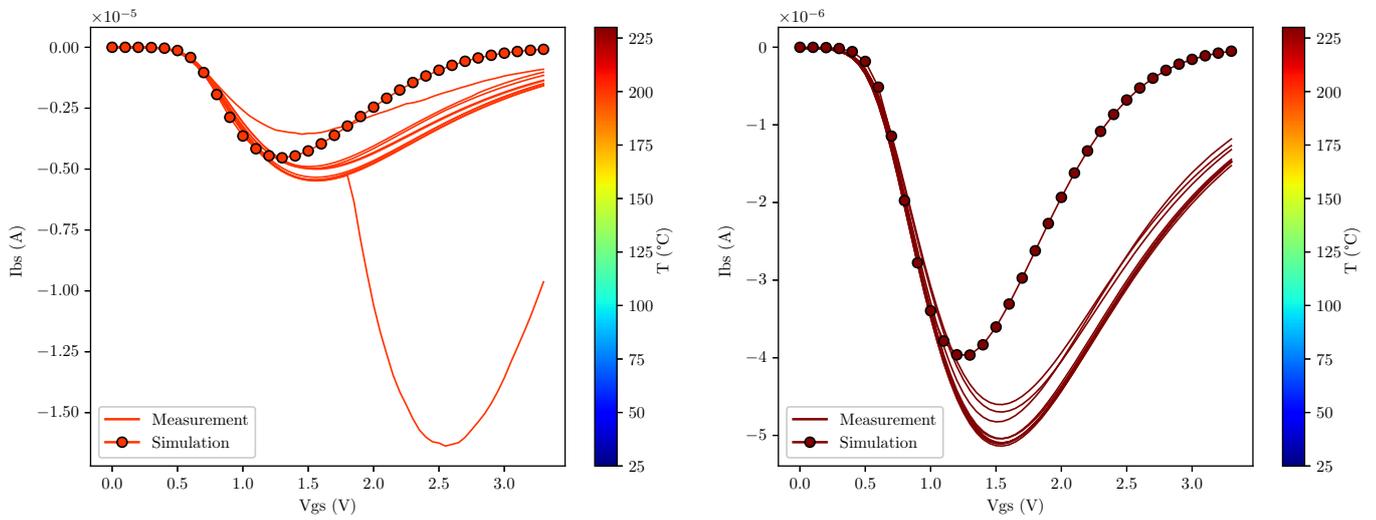


Figure 12: $I_{bs} - V_{gs}$ curves of 3.3V nMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures and $V_{ds}=3.3\text{V}$. The color indicates the according temperature.

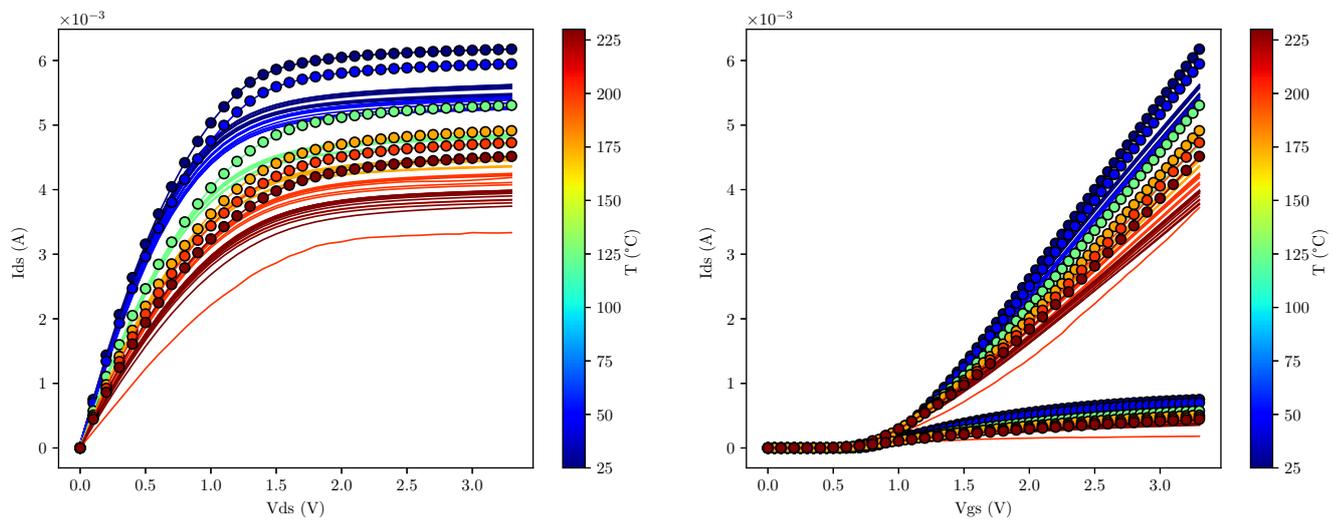


Figure 13: Comparisons of measurements (circle marks) and simulations (solid lines) of 3.3V nMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures. The color indicates the according temperature.

3.3V nMOS_ W/L = 10 μ m/0.5 μ m

3.3V nMOS_10 μ m/0.5 μ m												
	T $^{\circ}$ C	Simula- tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device #10
VTHcc (V)	25 $^{\circ}$ C	0.70	0.75	0.75	0.75	0.75	0.75	0.75	0.75	0.75	0.75	0.75
	50 $^{\circ}$ C	0.69	0.73	0.73	0.73	0.72	0.73	0.73	0.73	0.72	0.73	0.73
	125 $^{\circ}$ C	0.63	0.65	0.65	0.65	0.64	0.65	0.65	0.65	0.64	0.65	0.65
	175 $^{\circ}$ C	0.56	0.59	0.59	0.59	0.58	0.59	0.59	0.59	0.59	0.59	0.59
	200 $^{\circ}$ C	0.53	0.51	0.52	0.52	0.51	0.52	0.52	0.51	0.52	0.52	0.53
	230 $^{\circ}$ C	0.50	0.46	0.48	0.48	0.48	0.48	0.48	0.48	0.47	0.45	0.45
IDlin (mA)	25 $^{\circ}$ C	0.56	0.50	0.54	0.55	0.54	0.53	0.55	0.54	0.55	0.55	0.54
	50 $^{\circ}$ C	0.51	0.51	0.51	0.51	0.50	0.50	0.51	0.50	0.51	0.51	0.50
	125 $^{\circ}$ C	0.41	0.41	0.41	0.42	0.42	0.41	0.42	0.41	0.42	0.42	0.42
	175 $^{\circ}$ C	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36	0.36
	200 $^{\circ}$ C	0.33	0.29	0.30	-0.3	0.30	0.30	0.30	0.29	0.27	0.25	0.27
	230 $^{\circ}$ C	0.31	0.26	0.26	0.27	0.27	0.27	0.27	0.26	0.27	0.27	0.25
IDsat (mA)	25 $^{\circ}$ C	4.64	4.23	4.21	4.25	4.27	4.22	4.26	4.20	4.26	4.27	4.24
	50 $^{\circ}$ C	4.39	4.03	4.02	4.06	4.08	4.02	4.08	4.02	4.08	4.09	4.09
	125 $^{\circ}$ C	3.75	3.51	3.50	3.55	3.56	3.53	3.56	3.51	3.56	3.57	3.57
	175 $^{\circ}$ C	3.39	3.21	3.20	3.24	3.26	3.22	3.26	3.21	3.26	3.27	3.27
	200 $^{\circ}$ C	3.23	3.0	3.0	3.0	3.0	3.0	3.0	3.0	2.8	2.7	2.6
	230 $^{\circ}$ C	3.05	2.7	2.8	2.8	2.8	2.8	2.8	2.7	2.8	2.8	2.7

Table 10: Key figures of merit of the MOSFETs extracted from I-V curves.

ne3i_10um/0.5um												
	T $^{\circ}$ C	Simula- -tion	Device #1	Device #2	Device# 3	Device #4	Device #5	Device #6	Device# 7	Device #8	Device #9	Device #10
I _{bmax} (nA) @ V _{ds} =3.3V	200 $^{\circ}$ C	2430	2386	86950	2449	2419	2407	2466	2321	2302	2238	2174
	230 $^{\circ}$ C	2140	2240	2283	2323	2305	2274	2352	2198	2343	2354	2224

Table 11: Body currents of MOSFETs extracted from I_{bs} - V_{gs} curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
IDlin (mA)	25°C	0.50	0.55	0.539	0.0096	1.8 %	3.9 %
	50°C	0.50	0.51	0.506	0.0048	0.9 %	0.8 %
	125°C	0.41	0.42	0.416	0.0048	1.2 %	1.4 %
	175°C	0.36	0.36	0.36	0	0 %	0 %
	200°C	0.25	0.30	0.29	0.0139	4.85 %	13.8 %
	230°C	0.25	0.27	0.27	0.0054	2.03 %	14.8 %
IDsat (mA)	25°C	4.20	4.27	4.241	0.021	0.5 %	9.4 %
	50°C	4.02	4.09	4.057	0.0276	0.7 %	8.2 %
	125°C	3.50	3.57	3.542	0.0236	0.7 %	5.9 %
	175°C	3.20	3.27	3.24	0.024	0.7 %	4.6 %
	200°C	2.6	3.0	2.9	0.1318	4.51 %	11.4 %
	230°C	2.7	2.8	2.8	0.0408	1.47 %	8.9 %

Table 12: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value.

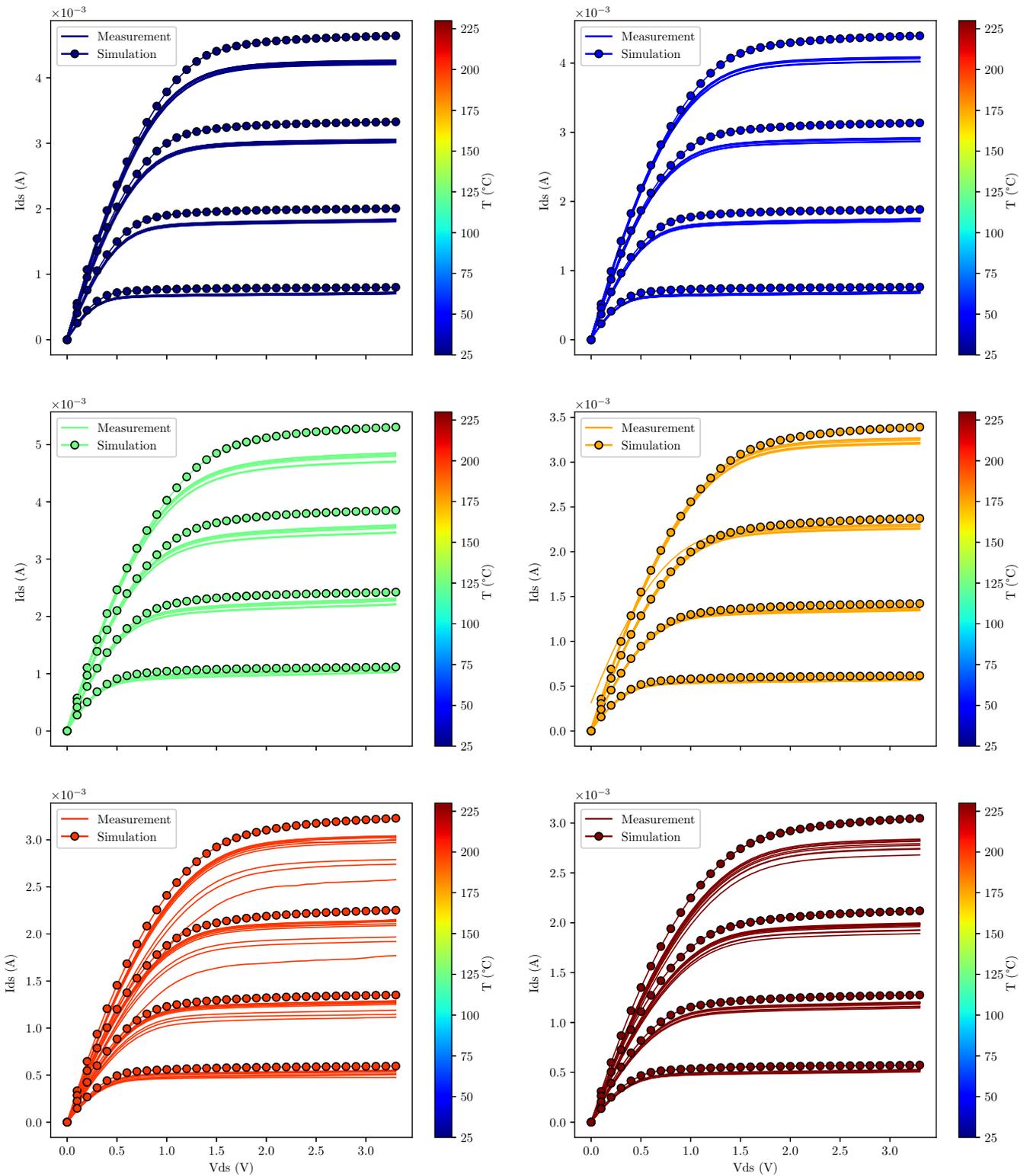


Figure 14: $I_{ds} - V_{ds}$ curves of 3.3V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures. The values of V_{gs} are 1.5V, 2.1V, 2.7V, 3.3V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

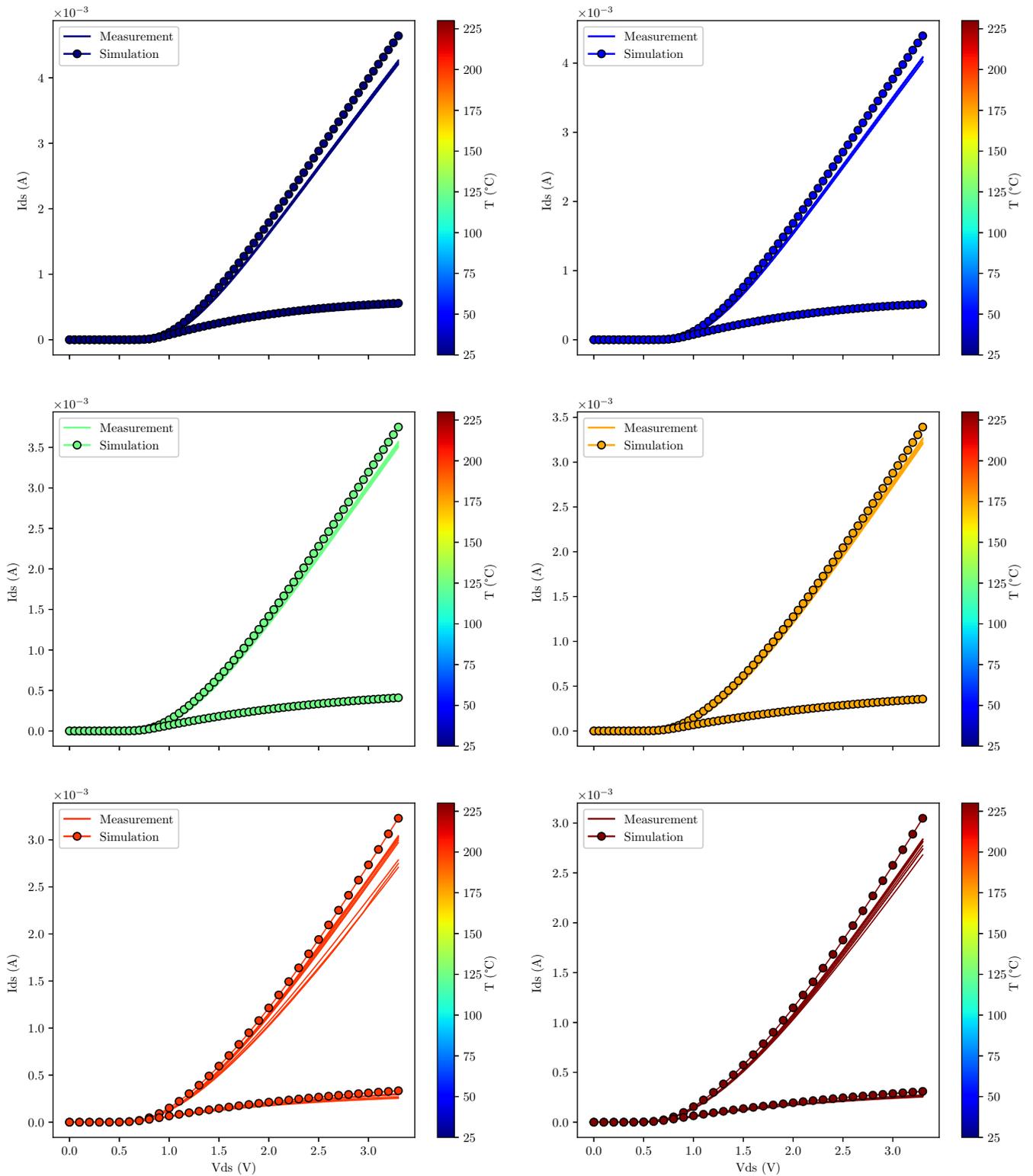


Figure 15: $I_{ds}-V_{gs}$ curves of 3.3V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures. Values of V_{ds} are 0.1V and 3.3V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

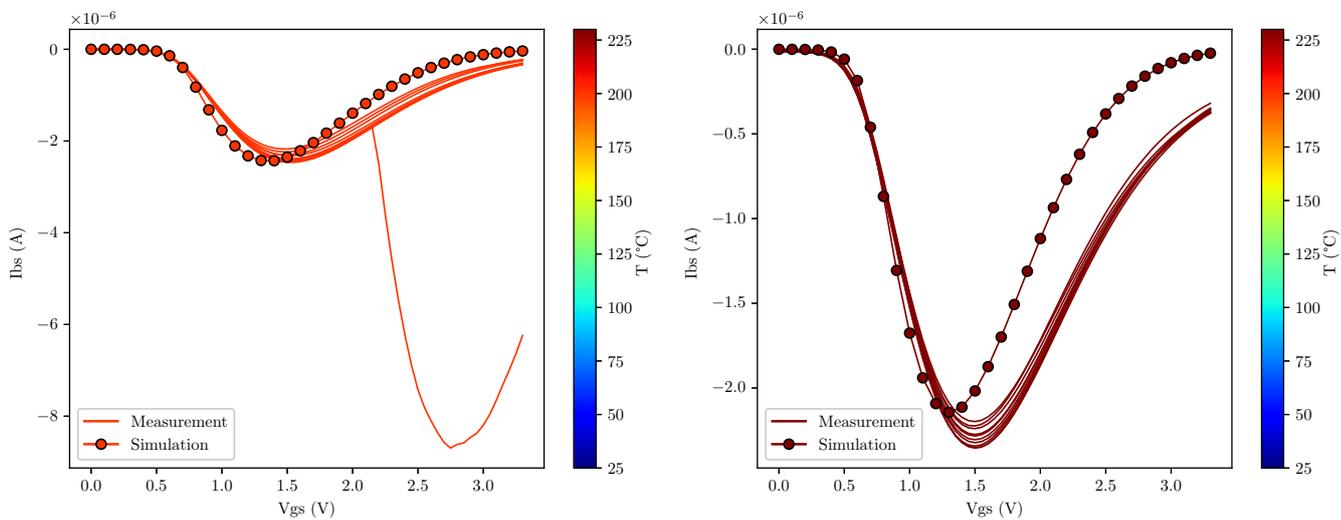


Figure 16: $I_{bs} - V_{gs}$ curves of 3.3V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures and $V_{ds}=3.3\text{V}$. The color indicates the according temperature.

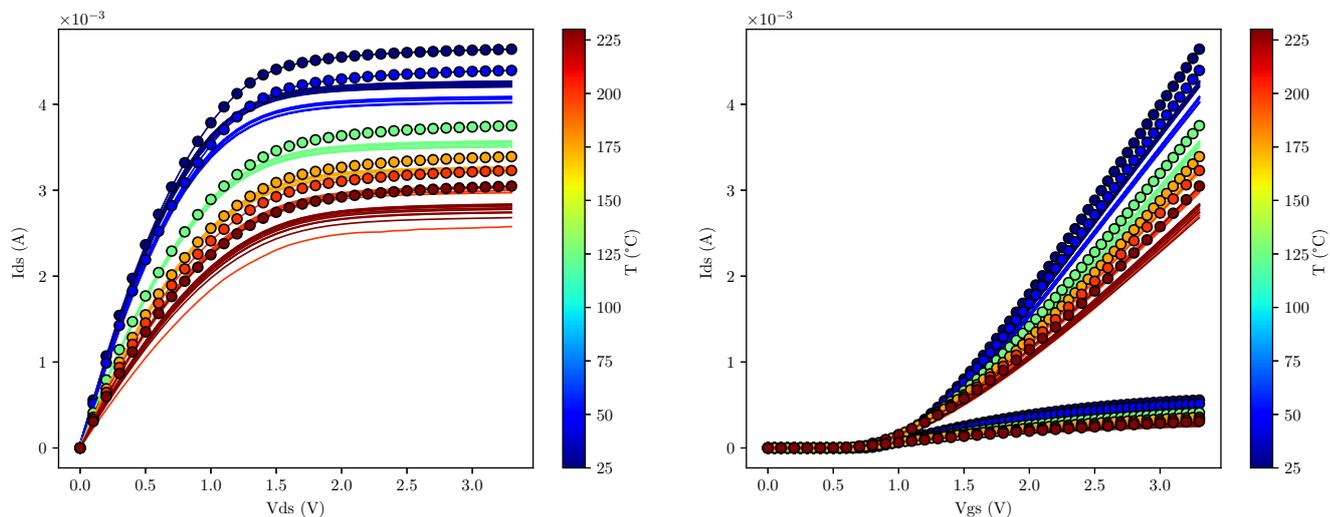


Figure 17: Comparisons of measurements (circle marks) and simulations (solid lines) of 3.3V nMOS ($W/L=10/0.5\mu\text{m}$) at different temperatures. The color indicates the according temperature.

1.8V pMOS_ W/L = 10 μ m/0.18 μ m

1.8V pMOS_10 μ m/0.18 μ m												
	T°C	Simula- tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device# 10
VTHcc (V)	25°C	-0.65	-0.65	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64
	50°C	-0.65	-0.67	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65
	125°C	-0.55	-0.54	-0.54	-0.55	-0.55	-0.55	-0.55	-0.55	-0.54	-0.54	-0.54
	175°C	-0.50	-0.50	-0.49	-0.48	-0.49	-0.50	-0.49	-0.50	-0.48	-0.49	-0.48
	200°C	-0.48	-0.61	-0.61	-0.62	-0.61	-0.61	-0.62	-0.62	-0.61	-0.61	-0.62
	230°C	-0.45	-0.60	-0.60	-0.59	-0.60	-0.59	-0.60	-0.59	-0.60	-0.60	-0.58
IDlin (mA)	25°C	-0.30	-0.31	-0.31	-0.32	-0.31	-0.30	-0.32	-0.30	-0.32	-0.32	-0.32
	50°C	-0.29	-0.29	-0.30	-0.30	-0.30	-0.29	-0.30	-0.29	-0.30	-0.30	-0.31
	125°C	-0.27	-0.26	-0.26	-0.27	-0.27	-0.26	-0.27	-0.25	-0.27	-0.27	-0.27
	175°C	-0.25	-0.24	-0.24	-0.25	-0.25	-0.24	-0.25	-0.24	-0.25	-0.25	-0.25
	200°C	-0.25	-0.23	-0.24	-0.25	-0.24	-0.25	-0.24	-0.22	-0.21	-0.19	-0.22
	230°C	-0.24	-0.22	-0.23	-0.24	-0.23	-0.23	-0.23	-0.21	-0.23	-0.23	-2.91E-04
IDsat (mA)	25°C	-1.70	-1.58	-1.62	-1.67	-1.62	-1.58	-1.65	-1.56	-1.66	-1.66	-1.69
	50°C	-1.69	-1.56	-1.59	-1.64	-1.59	-1.54	-1.62	-1.53	-1.62	-1.63	-1.66
	125°C	-1.64	-1.47	-1.50	-1.56	-1.51	-1.46	-1.55	-1.44	-1.54	-1.55	-1.57
	175°C	-1.61	-1.41	-1.44	-1.50	-1.46	-1.41	-1.48	-1.40	-1.49	-1.50	-1.51
	200°C	-1.59	-1.40	-1.48	-1.52	-1.44	-1.51	-1.42	-1.34	-1.26	-1.27	-1.29
	230°C	-1.58	-1.34	-1.43	-1.44	-1.40	-1.43	-1.37	-1.29	-1.39	-1.40	-1.16

Table 13: Key figures of merit of the MOSFETs extracted from I-V curves.

1.8V pMOS_10 μ m/0.18 μ m												
	T°C	Simula- tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device# 7	Device #8	Device #9	Device #10
Ibmax (nA) @ Vds=-1.8V	200°C	0.58	5	6	6	5	6	5	5	6	6	5
	230°C	0.73	16	13	11	10	12	11	10	11	12	27

Table 14: Body currents of MOSFETs extracted from Ibs - Vgs curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
IDlin (mA)	25°C	-0.32	-0.30	-0.313	0.007	2.2 %	4.1 %
	50°C	-0.31	-0.29	-0.298	0.0048	1.6 %	2.7 %
	125°C	-0.27	-0.25	-0.265	0.006	2.3 %	1.9 %
	175°C	-0.25	-0.24	-0.246	0.0048	2.0 %	1.6 %
	200°C	-0.25	-0.19	-0.23	0.0140	6.2 %	8.7 %
	230°C	-0.24	-2.91E-04	-0.20	0.0407	20.0 %	20.0 %
IDsat (mA)	25°C	-1.69	-1.56	-1.629	0.037	2.3 %	4.4 %
	50°C	-1.66	-1.53	-1.598	0.036	2.3 %	5.8 %
	125°C	-1.57	-1.44	-1.515	0.039	2.6 %	8.3 %
	175°C	-1.51	-1.40	-1.46	0.036	2.5 %	10.3 %
	200°C	-1.52	-1.26	-1.39	0.0825	5.9 %	14.4 %
	230°C	-1.44	-1.16	-1.37	0.0620	4.5 %	15.3 %

Table 15: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value.

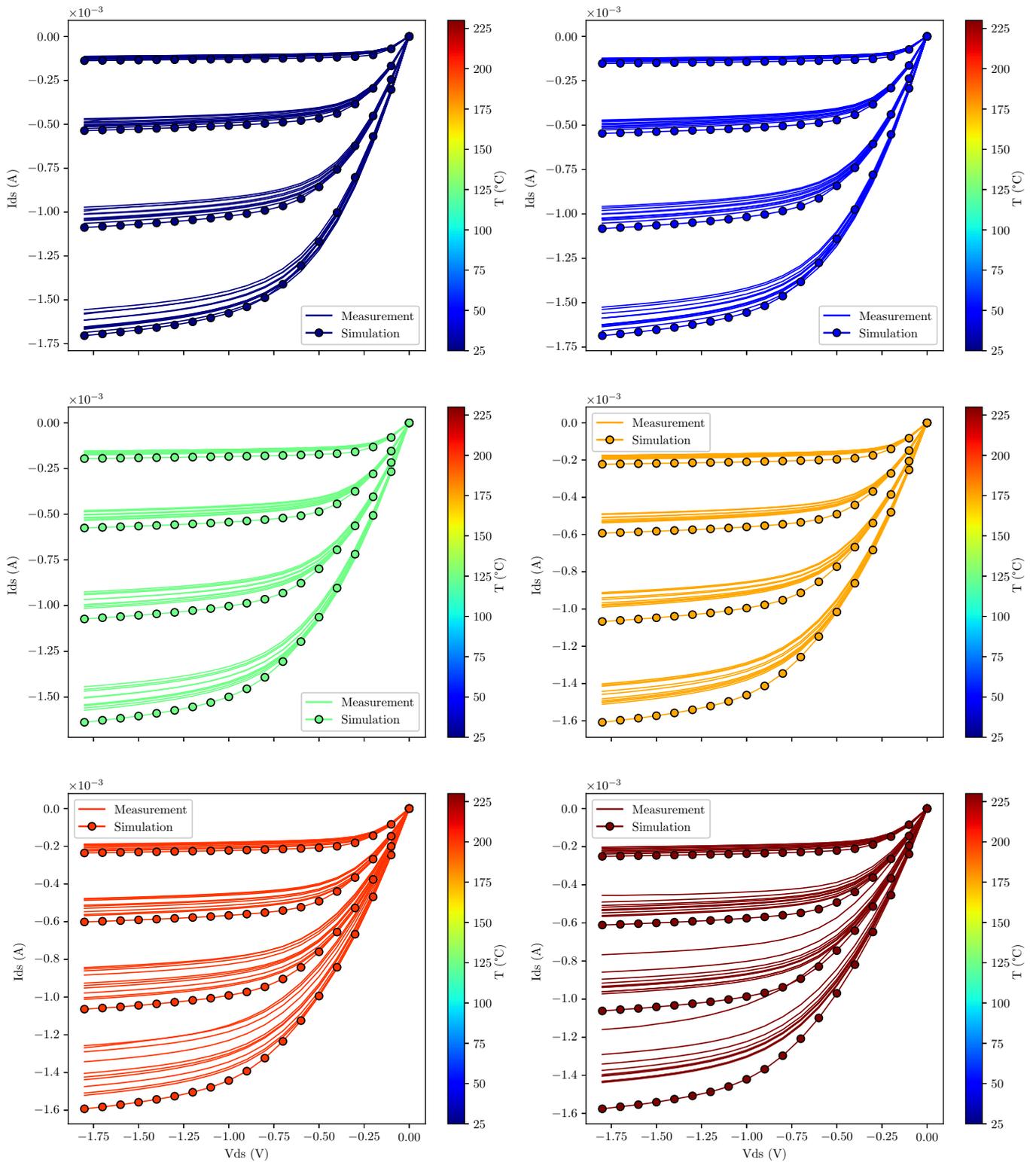


Figure 18: $I_{ds} - V_{ds}$ curves of 1.8V pMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures. The values of V_{gs} are -0.9V, -1.2V, -1.5V, -1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

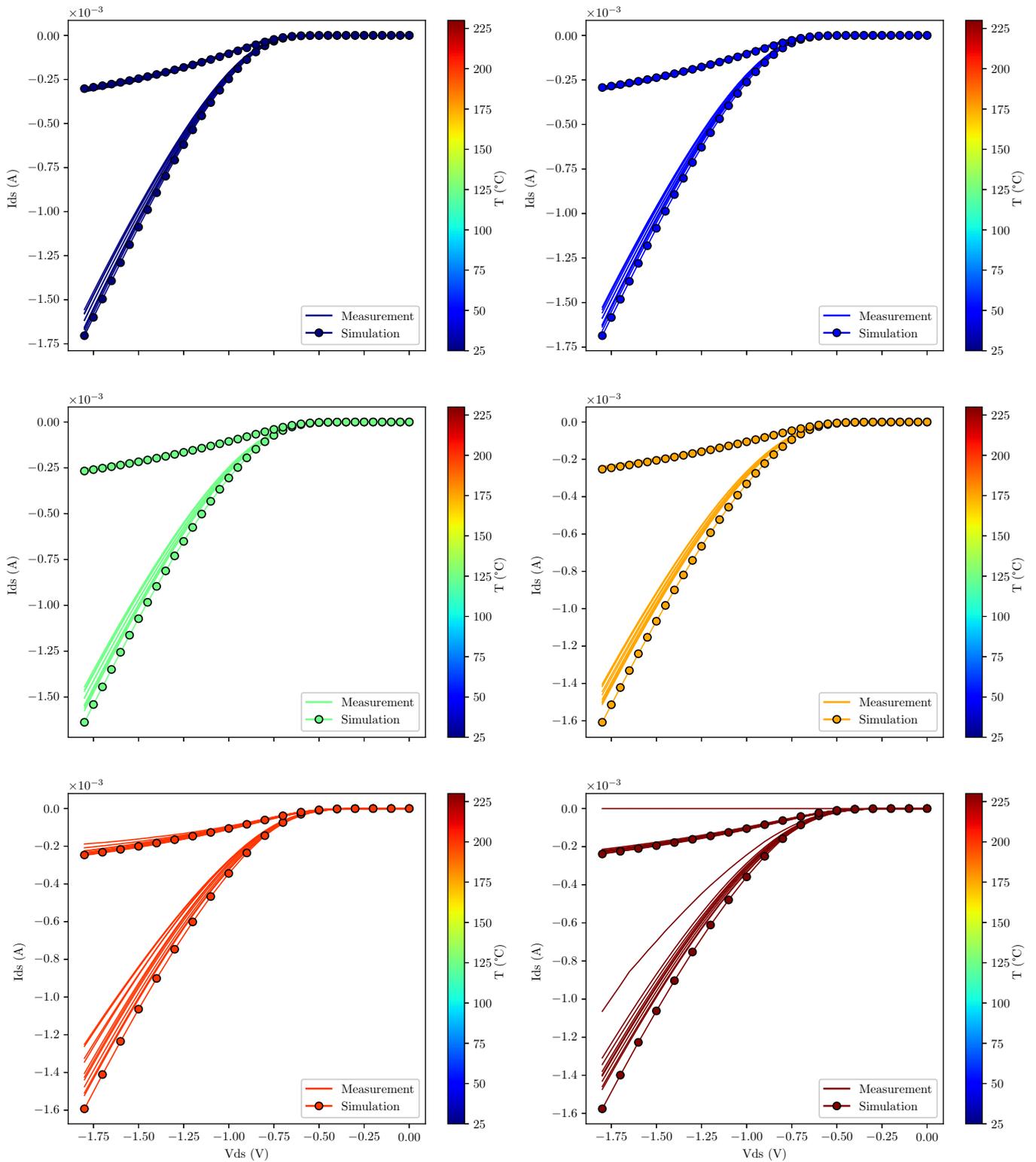


Figure 19: $I_{ds} - V_{gs}$ curves of 1.8V pMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures. Values of V_{ds} are -0.1V and -1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

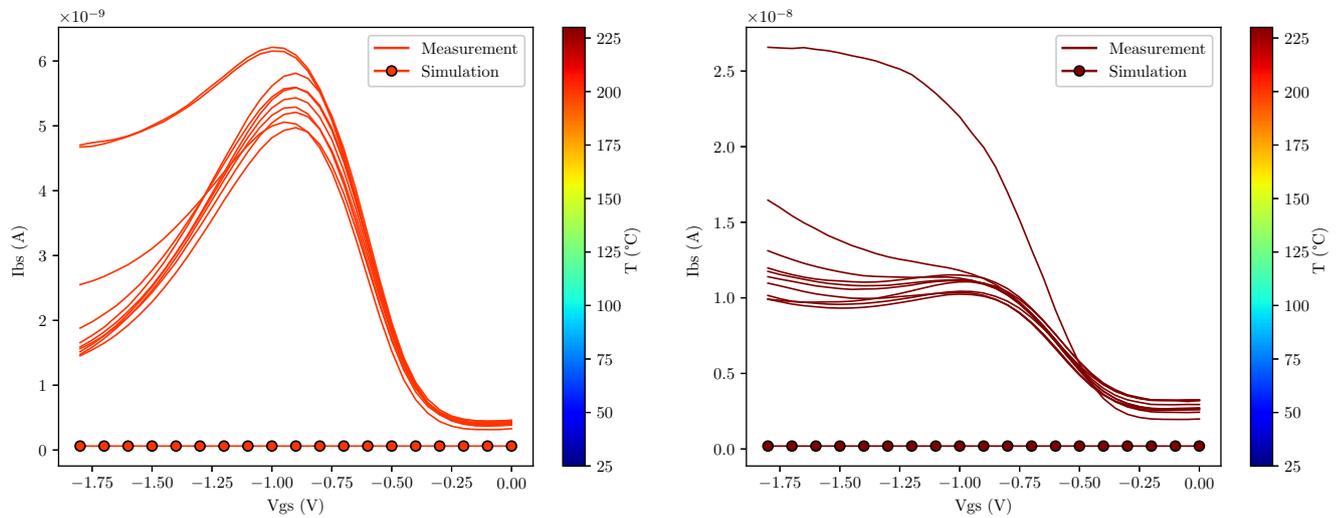


Figure 20: $I_{bs} - V_{gs}$ curves of 1.8V pMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures and $V_{ds}=-1.8\text{V}$. The color indicates the according temperature.

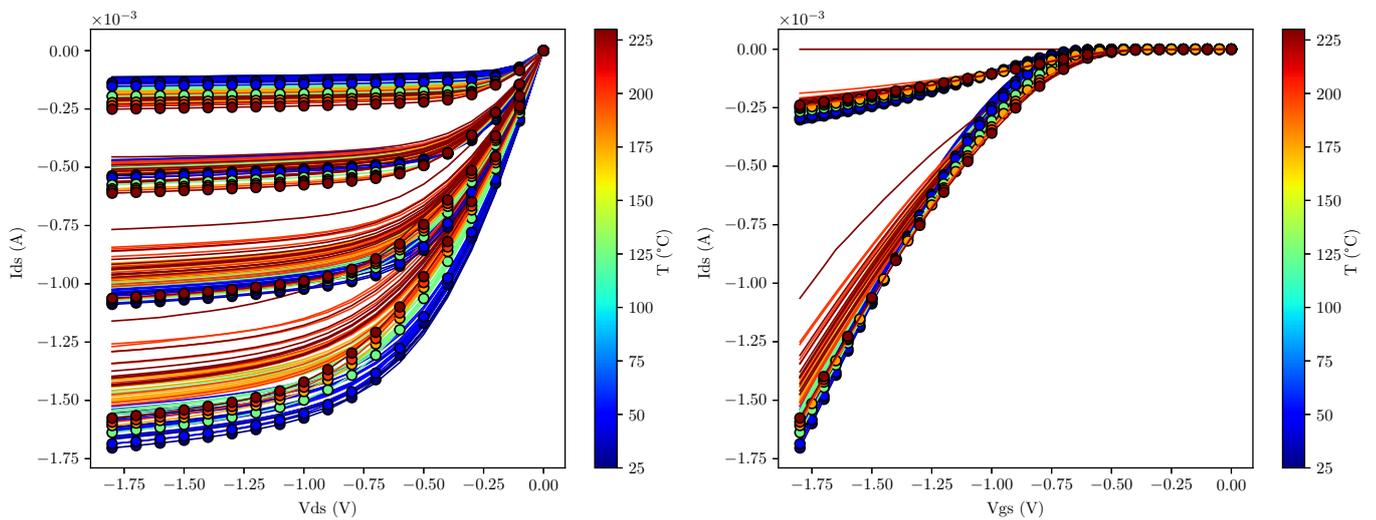


Figure 21: Comparisons of measurements (circle marks) and simulations (solid lines) of 1.8V pMOS ($W/L=10/0.18\mu\text{m}$) at different temperatures. The color indicates the according temperature.

1.8V pMOS_ W/L = 10 μ m/0.5 μ m

1.8V pMOS_10 μ m/0.5 μ m												
	T $^{\circ}$ C	Simula- tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device #10
VTHcc (V)	25 $^{\circ}$ C	-0.71	-0.69	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70
	50 $^{\circ}$ C	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70	-0.70
	125 $^{\circ}$ C	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60
	175 $^{\circ}$ C	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55
	200 $^{\circ}$ C	-0.52	-0.52	-0.51	-0.51	-0.52	-0.52	-0.52	-0.51	-0.52	-0.52	-0.51
	230 $^{\circ}$ C	-0.51	-0.51	-0.50	-0.51	-0.51	-0.51	-0.51	-0.51	-0.51	-0.51	-0.51
IDlin (mA)	25 $^{\circ}$ C	-0.09	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10
	50 $^{\circ}$ C	-0.09	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10
	125 $^{\circ}$ C	-0.08	-0.08	-0.09	-0.09	-0.09	-0.08	-0.09	-0.08	-0.09	-0.09	-0.09
	175 $^{\circ}$ C	-0.07	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08
	200 $^{\circ}$ C	-0.07	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.08	-0.07	-0.07	-0.07
	230 $^{\circ}$ C	-0.07	-0.07	-0.07	-0.07	-0.07	-0.07	-0.07	-0.07	-0.07	-0.07	-0.07
IDSat (mA)	25 $^{\circ}$ C	-0.43	-0.47	-0.48	-0.48	-0.48	-0.47	-0.48	-0.47	-0.47	-0.47	-0.49
	50 $^{\circ}$ C	-0.42	-0.46	-0.47	-0.46	-0.46	-0.46	-0.46	-0.46	-0.46	-0.46	-0.47
	125 $^{\circ}$ C	-0.41	-0.42	-0.43	-0.43	-0.43	-0.42	-0.43	-0.42	-0.42	-0.42	-0.44
	175 $^{\circ}$ C	-0.40	-0.41	-0.42	-0.41	-0.41	-0.40	-0.41	-0.40	-0.40	-0.40	-0.41
	200 $^{\circ}$ C	-0.40	-0.40	-0.40	-0.41	-0.39	-0.41	-0.39	-0.39	-0.37	-0.38	-0.38
	230 $^{\circ}$ C	-0.40	-0.38	-0.39	-0.40	-0.38	-0.40	-0.38	-0.37	-0.38	-0.38	-0.35

Table 16: Key figures of merit of the MOSFETs extracted from I-V curves.

1.8V pMOS_10 μ m/0.5 μ m												
	T $^{\circ}$ C	Simula- tion	Device #1	Device# 2	Device# 3	Device# 4	Device #5	Device #6	Device# 7	Device #8	Device #9	Device #10
 I_{bmax} (nA) @ V_{ds}=-1.8V	200 $^{\circ}$ C	0.24	1	1	1	1	1	1	1	2	2	1
	230 $^{\circ}$ C	0.41	8	8	7	4	4	4	7	5	6	23

Table 17: Body currents of MOSFETs extracted from I_{bs} - V_{gs} curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
ID _{lin} (mA)	25°C	-0.10	-0.10	-0.10	0	0.0 %	10.0 %
	50°C	-0.10	-0.10	-0.10	0	0.0 %	10.0 %
	125°C	-0.09	-0.08	-0.087	-0.0042	4.8 %	8.0 %
	175°C	-0.08	-0.08	-0.08	0	0.0 %	12.5 %
	200°C	-0.08	-0.07	-0.08	0.0017	2.2 %	12.5 %
	230°C	-0.07	-0.07	-0.07	0.0011	1.5 %	0 %
ID _{sat} (mA)	25°C	-0.49	-0.47	-0.476	0.006	1.3 %	9.7 %
	50°C	-0.47	-0.46	-0.462	0.0032	0.7 %	9.1 %
	125°C	-0.44	-0.42	-0.426	0.006	1.4 %	3.8 %
	175°C	-0.42	-0.40	-0.407	0.0056	1.4 %	1.7 %
	200°C	-0.41	-0.37	-0.39	0.011	2.7 %	2.6 %
	230°C	-0.40	-0.35	-0.38	0.0079	2.1 %	5.0 %

Table 18: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value.

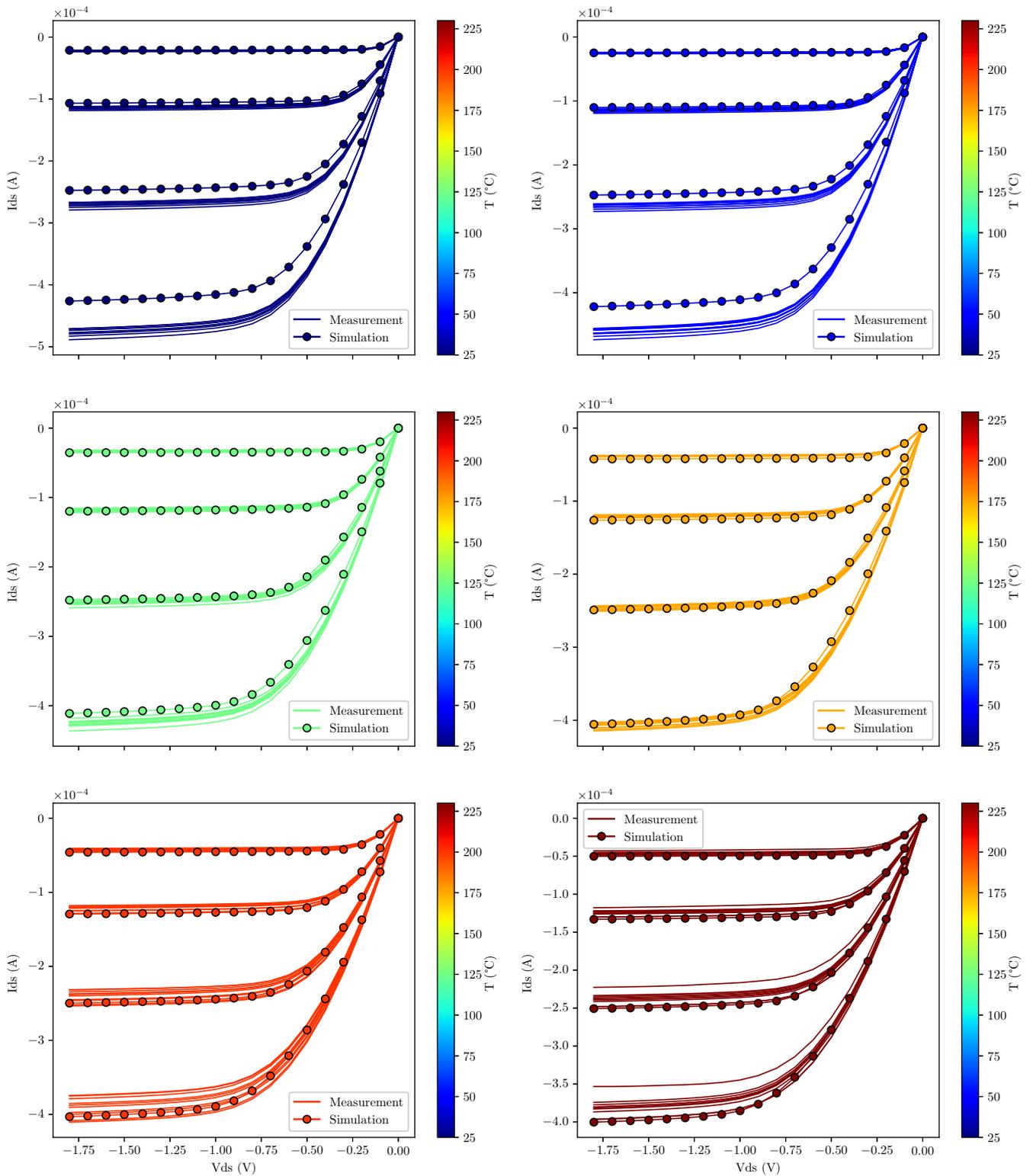


Figure 22: $I_{ds} - V_{ds}$ curves of 1.8V pMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures. The values of V_{gs} are -0.9V, -1.2V, -1.5V, -1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

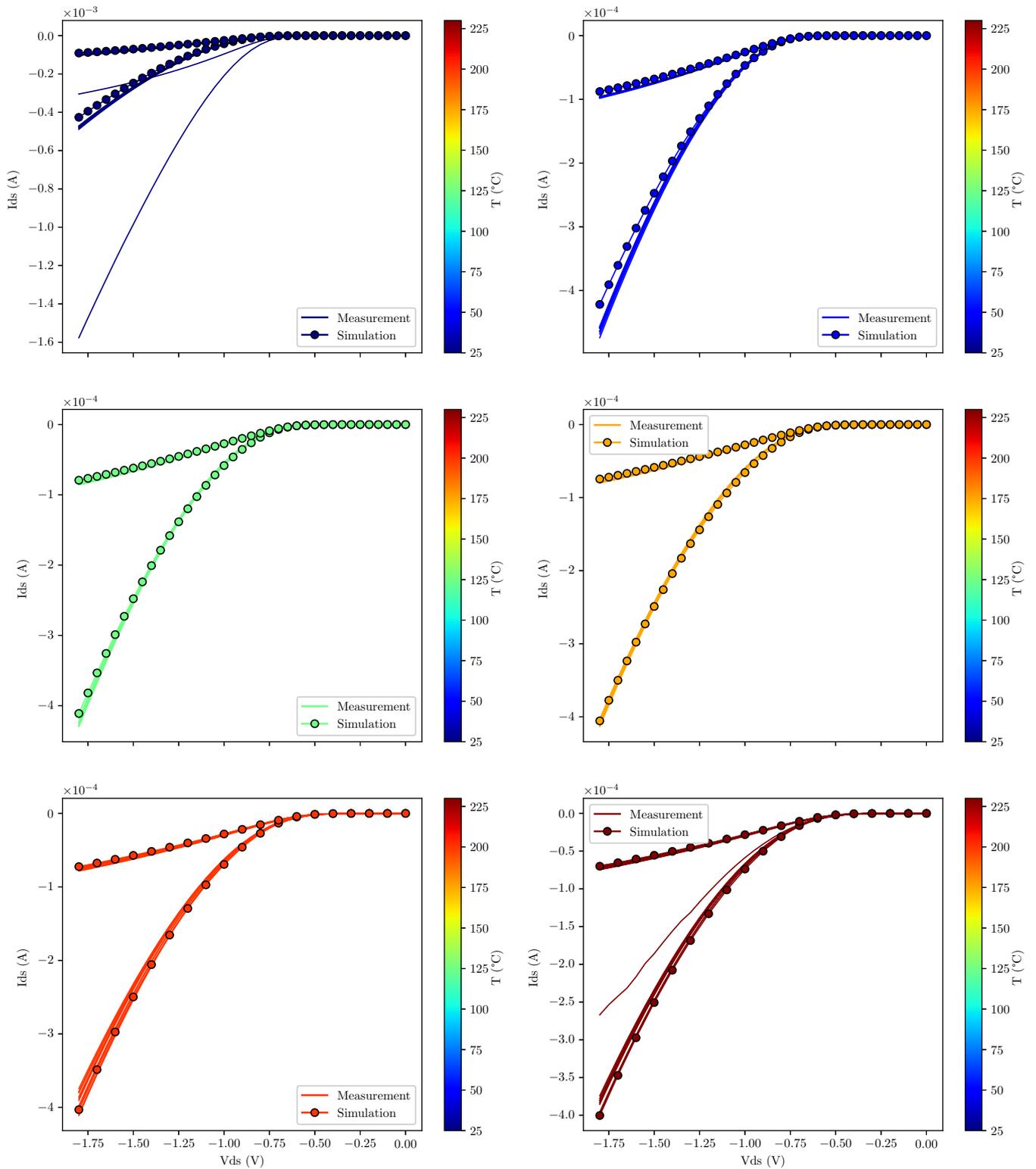


Figure 23: $I_{sd} - V_{sg}$ curves of 1.8V pMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures. Values of V_{ds} are -0.1V and -1.8V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

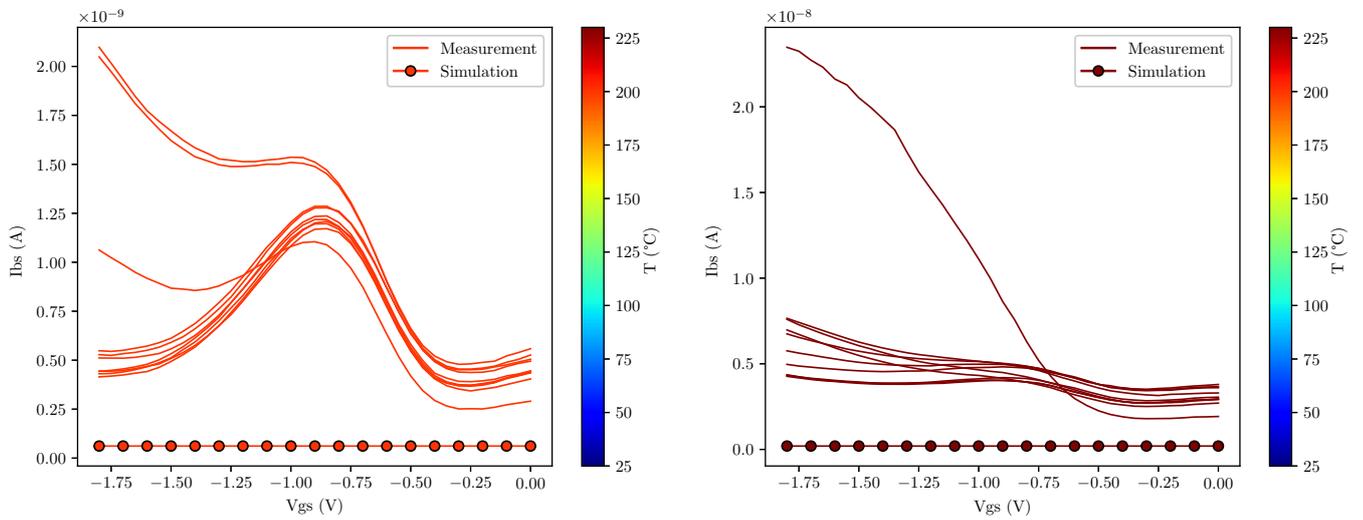


Figure 24: $I_{bs} - V_{gs}$ curves of 1.8V pMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures and $V_{ds}=-1.8\text{V}$. The color indicates the according temperature.

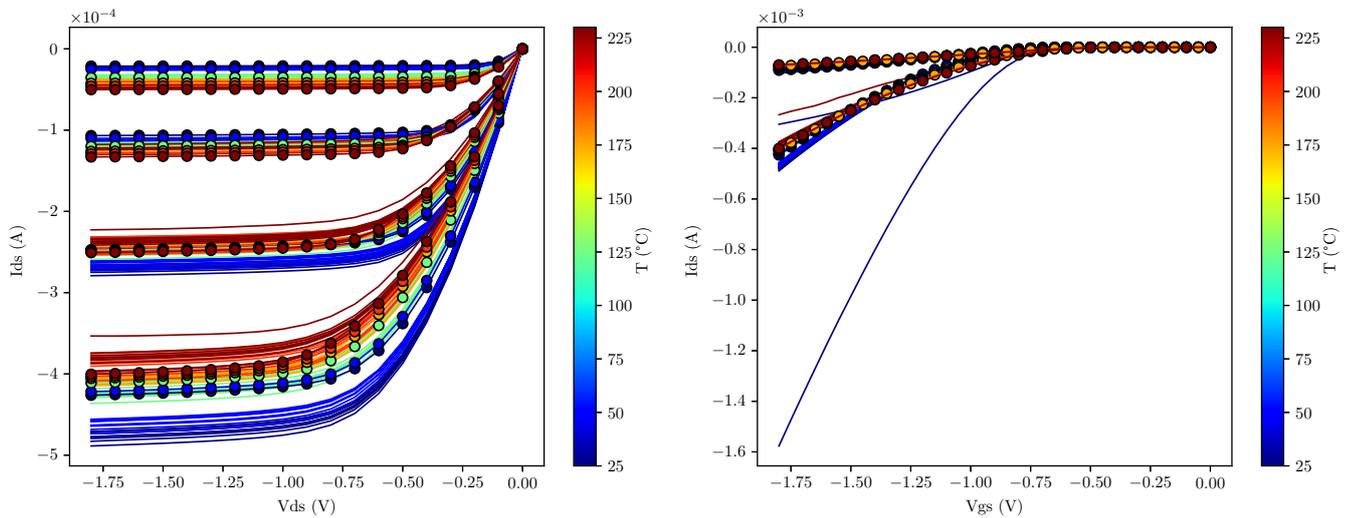


Figure 25: Comparisons of measurements (circle marks) and simulations (solid lines) of 1.8V pMOS ($W/L=10/0.35\mu\text{m}$) at different temperatures. The color indicates the according temperature.

3.3V pMOS_ W/L = 10 μ m/0.3 μ m

3.3V pMOS_10 μ m/0.3 μ m												
	T $^{\circ}$ C	Simula- tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device #10
VTHcc (V)	25 $^{\circ}$ C	-0.63	-0.65	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64	-0.64
	50 $^{\circ}$ C	-0.59	-0.59	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60	-0.60
	125 $^{\circ}$ C	-0.51	-0.50	-0.51	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50	-0.50
	175 $^{\circ}$ C	-0.45	-0.44	-0.44	-0.44	-0.44	-0.44	-0.44	-0.44	-0.44	-0.44	-0.44
	200 $^{\circ}$ C	-0.44	-0.44	-0.44	-0.43	-0.44	-0.44	-0.44	-0.44	-0.44	-0.43	-0.44
	230 $^{\circ}$ C	-0.42	-0.38	-0.39	-0.38	-0.38	-0.38	-0.38	-0.38	-0.38	-0.38	-0.38
IDlin (mA)	25 $^{\circ}$ C	-0.27	-0.29	-0.27	-0.27	-0.27	-0.26	-0.27	-0.26	-0.27	-0.27	-0.27
	50 $^{\circ}$ C	-0.25	-0.25	-0.26	-0.26	-0.26	-0.25	-0.26	-0.25	-0.26	-0.26	-0.26
	125 $^{\circ}$ C	-0.23	-0.22	-0.22	-0.22	-0.22	-0.22	-0.22	-0.22	-0.22	-0.22	-0.22
	175 $^{\circ}$ C	-0.21	-0.20	-0.20	-0.20	-0.20	-0.20	-0.20	-0.20	-0.20	-0.20	-0.20
	200 $^{\circ}$ C	-0.21	-0.20	-0.20	-0.21	-0.20	-0.20	-0.20	-0.20	-0.20	-0.20	-0.19
	230 $^{\circ}$ C	-0.19	-0.19	-0.19	-0.19	-0.19	-0.19	-0.18	-0.19	-0.19	-0.19	-0.19
IDSat (mA)	25 $^{\circ}$ C	-3.16	-3.06	-3.09	-3.15	-3.12	-3.09	-3.15	-3.05	-3.15	-3.16	-3.15
	50 $^{\circ}$ C	-3.05	-2.98	-3.00	-3.06	-3.02	-2.99	-3.06	-2.96	-3.06	-3.07	-3.08
	125 $^{\circ}$ C	-2.79	-2.72	-2.73	-2.80	-2.77	-2.74	-2.80	-2.70	-2.80	-2.82	-2.82
	175 $^{\circ}$ C	-2.66	-2.57	-2.58	-2.64	-2.61	-2.59	-2.65	-2.55	-2.63	-2.65	-2.66
	200 $^{\circ}$ C	-2.61	-2.44	-2.52	-2.52	-2.50	-2.50	-2.49	-2.41	-2.50	-2.32	-2.42
	230 $^{\circ}$ C	-2.54	-2.30	-2.39	-2.39	-2.39	-2.39	-2.39	-2.29	-2.40	-2.37	-2.22

Table 19: Key figures of merit of the MOSFETs extracted from I-V curves.

3.3V pMOS_10 μ m/0.3 μ m												
	T $^{\circ}$ C	Simula- tion	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device#8	Device#9	Device #10
I _{bmax} (nA) @ V _{ds} =-3.3V	200 $^{\circ}$ C	392	689	701	712	705	707	693	683	2415200	673	680
	230 $^{\circ}$ C	378	702	716	723	724	725	710	698	1966800	728	576

Table 20: Body currents of MOSFETs extracted from I_{bs} - V_{gs} curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
IDlin (mA)	25°C	-0.29	-0.26	-0.27	0.004	1.5 %	0.0 %
	50°C	-0.26	-0.25	-0.257	0.0042	1.6 %	2.7 %
	125°C	-0.22	-0.22	-0.22	0	0.0 %	4.5 %
	175°C	-0.20	-0.20	-0.20	0	0.0 %	5.0 %
	200°C	-0.21	-0.19	-0.20	0.0048	2.4 %	5.0 %
	230°C	-0.19	-0.13	-0.18	0.0104	5.7 %	5.5 %
IDsat (mA)	25°C	-3.16	-3.05	-3.117	0.0356	1.1 %	1.4 %
	50°C	-3.08	-2.96	-3.028	0.038	1.3 %	0.7 %
	125°C	-2.82	-2.70	-2.77	0.038	1.4 %	0.7 %
	175°C	-2.66	-2.55	-2.613	0.033	1.3 %	1.8 %
	200°C	-2.52	-2.32	-2.46	0.0530	2.1 %	6.1 %
	230°C	-2.40	-2.22	-2.35	0.050	2.1 %	8.1 %

Table 21: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value.

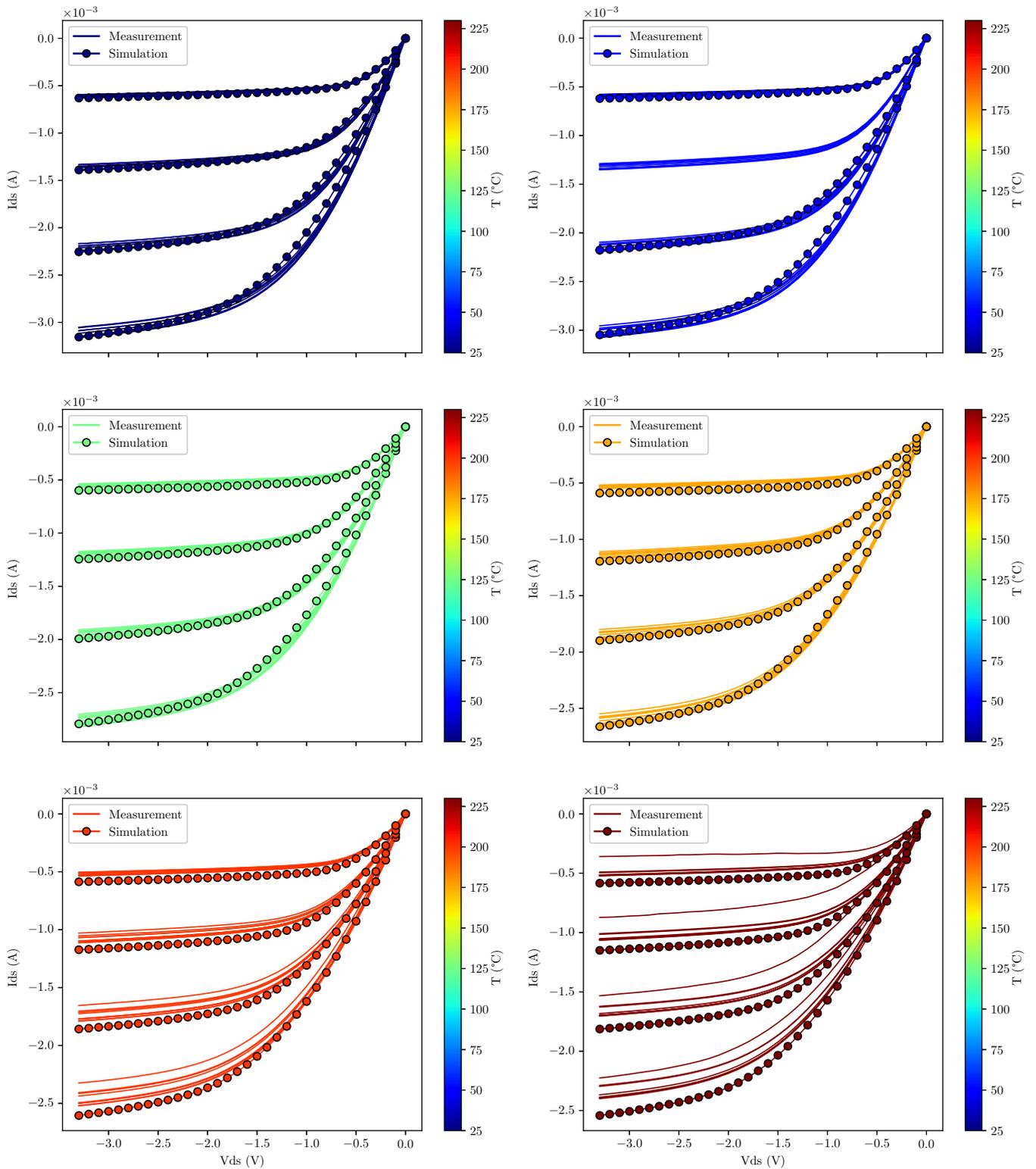


Figure 26: $I_{ds} - V_{ds}$ curves of 3.3V pMOS ($W/L=10/0.3\mu\text{m}$) at different temperatures. The values of V_{gs} are -1.5V, -2.1V, -2.7V, -3.3V, respectively. The color indicates the corresponding temperature. x-axis of all figures are in the same scale

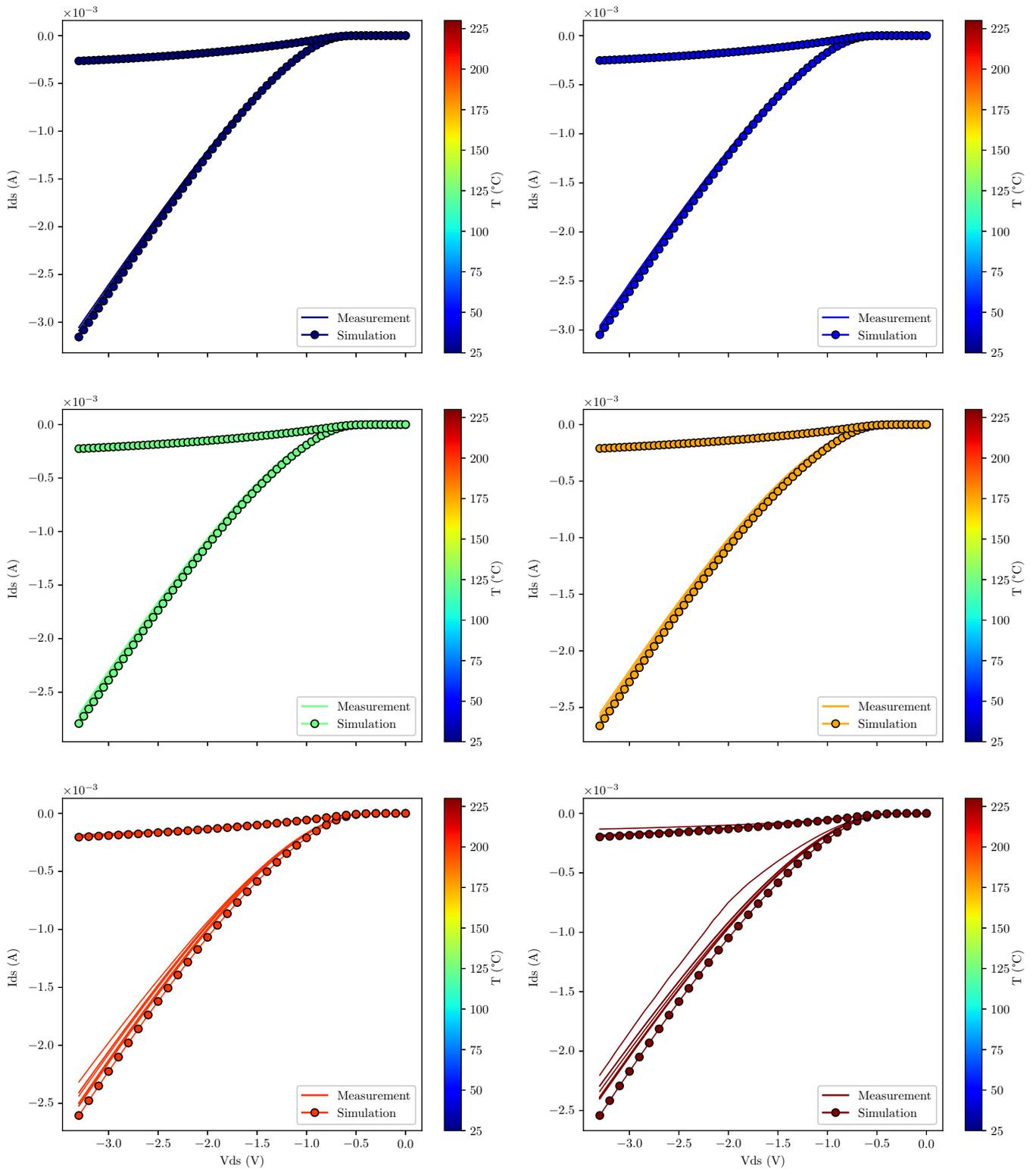


Figure 27: $I_{ds}-V_{gs}$ curves of 3.3V pMOS ($W/L=10/0.3\mu\text{m}$) at different temperatures. Values of V_{ds} are -0.1V and -3.3V , respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

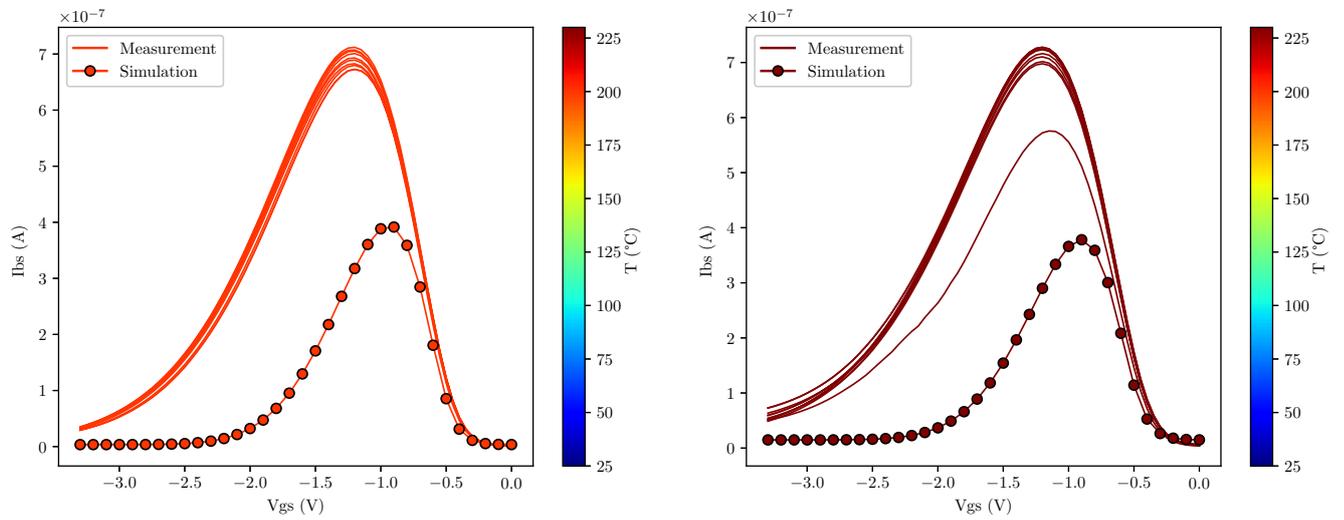


Figure 28: $I_{bs} - V_{gs}$ curves of 3.3V pMOS ($W/L=10/0.3\mu\text{m}$) at different temperatures and $V_{ds}=-3.3\text{V}$. The color indicates the according temperature.

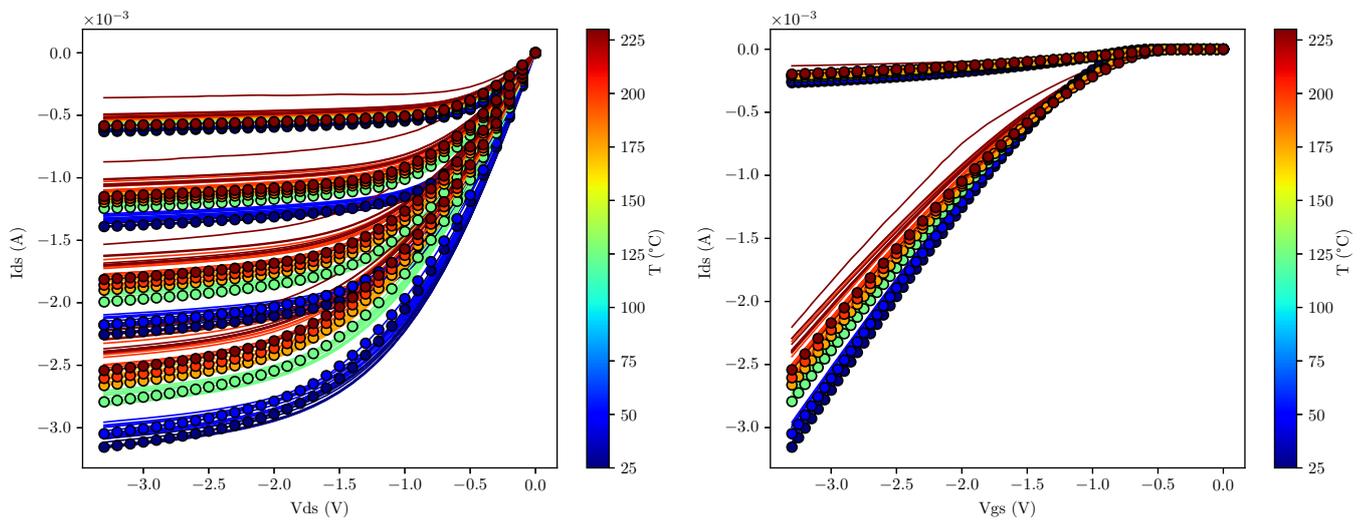


Figure 29: Comparisons of measurements (circle marks) and simulations (solid lines) of 3.3V pMOS ($W/L=10/0.3\mu\text{m}$) at different temperatures. The color indicates the according temperature.

3.3V pMOS_ W/L = 10 μ m/0.6 μ m

3.3V pMOS_10 μ m/0.6 μ m												
	T°C	Simulation	Device #1	Device #2	Device #3	Device #4	Device #5	Device #6	Device #7	Device #8	Device #9	Device #10
V _{THcc} (V)	25°C	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65
	50°C	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65	-0.65
	125°C	-0.56	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55	-0.55
	175°C	-0.51	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5
	200°C	-0.51	-0.46	-0.47	-0.47	-0.46	-0.46	-0.47	-0.47	-0.47	-0.47	-0.47
	230°C	-0.48	-0.44	-0.44	-0.44	-0.44	-0.44	-0.44	-0.45	-0.44	-0.44	-0.44
I _{Dlin} (mA)	25°C	-0.13	-0.14	-0.13	-0.13	-0.13	-0.13	-0.13	-0.13	-0.13	-0.13	-0.13
	50°C	-0.12	-0.13	-0.12	-0.13	-0.13	-0.12	-0.13	-0.12	-0.13	-0.13	-0.13
	125°C	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11	-0.11
	175°C	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10
	200°C	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.10	-0.09	-0.10
	230°C	-0.09	-0.09	-0.09	-0.09	-0.09	-0.09	-0.09	-0.09	-0.09	-0.09	-0.09
I _{Dsat} (mA)	25°C	-1.44	-1.55	-1.56	-1.57	-1.57	-1.55	-1.58	-1.55	-1.57	-1.58	-1.57
	50°C	-1.38	-1.49	-1.48	-1.50	-1.50	-1.49	-1.51	-1.48	-1.50	-1.51	-1.51
	125°C	-1.24	-1.31	-1.31	-1.32	-1.32	-1.31	-1.33	-1.31	-1.33	-1.33	-1.33
	175°C	-1.17	-1.21	-1.22	-1.22	-1.23	-1.21	-1.23	-1.21	-1.22	-1.23	-1.23
	200°C	-1.14	-1.13	-1.14	-1.14	-1.15	-1.14	-1.14	-1.12	-1.13	-1.10	-1.13
	230°C	-1.11	-1.06	-1.08	-1.08	-1.09	-1.08	-1.08	-1.06	-1.08	-1.07	-1.04

Table 22: Key figures of merit of the MOSFETs extracted from I-V curves.

3.3V pMOS_10 μ m/0.3 μ m												
	T°C	Simulation	Device #1	Device #2	Device# 3	Device #4	Device #5	Device #6	Device #7	Device# 8	Device #9	Device #10
I _{bmax} (nA) @ V _{ds} =-3.3V	200 °C	336	215	216	216	216	220	215	216	1120460	213	211
	230 °C	324	226	224	225	225	228	223	225	895800	228	218

Table 23: Body currents of MOSFETs extracted from I_{bs} - V_{gs} curves.

		Min #1-10	Max #1-10	Average Value #1-10	Average Deviation #1-10	% deviation #1-10	% difference of Simulation compared to Average Value
IDlin (mA)	25°C	-0.14	-0.13	-0.131	0.0018	1.4 %	0.8 %
	50°C	-0.13	-0.12	-0.127	0.0042	3.3 %	5.5 %
	125°C	-0.11	-0.11	-0.11	0	0.0 %	0.0 %
	175°C	-0.10	-0.10	-0.10	0	0.0 %	0.0 %
	200°C	-0.10	-0.09	-0.10	0.0009	1.0 %	0.0 %
	230°C	-0.09	-0.09	-0.09	0.0009	1.0 %	0.0 %
IDsat (mA)	25°C	-1.58	-1.55	-1.565	0.01	0.6 %	8.0 %
	50°C	-1.51	-1.48	-1.497	0.0096	0.6 %	7.8 %
	125°C	-1.33	-1.31	-1.32	0.008	0.6 %	6.0 %
	175°C	-1.23	-1.21	-1.221	0.0072	0.6 %	4.2 %
	200°C	-1.15	-1.10	-1.13	0.0099	0.9 %	0.9 %
	230°C	-1.09	-1.04	-1.07	0.0114	1.1 %	3.7 %

Table 24: Statistical analysis of linear and saturation current.

Note:

- Average Value is the average (arithmetic mean) of a set of numbers.
- Average Deviation is the average of the difference of a set of numbers from their Average Value.
- % deviation is the average percentage that a data point differs from the Average Value.

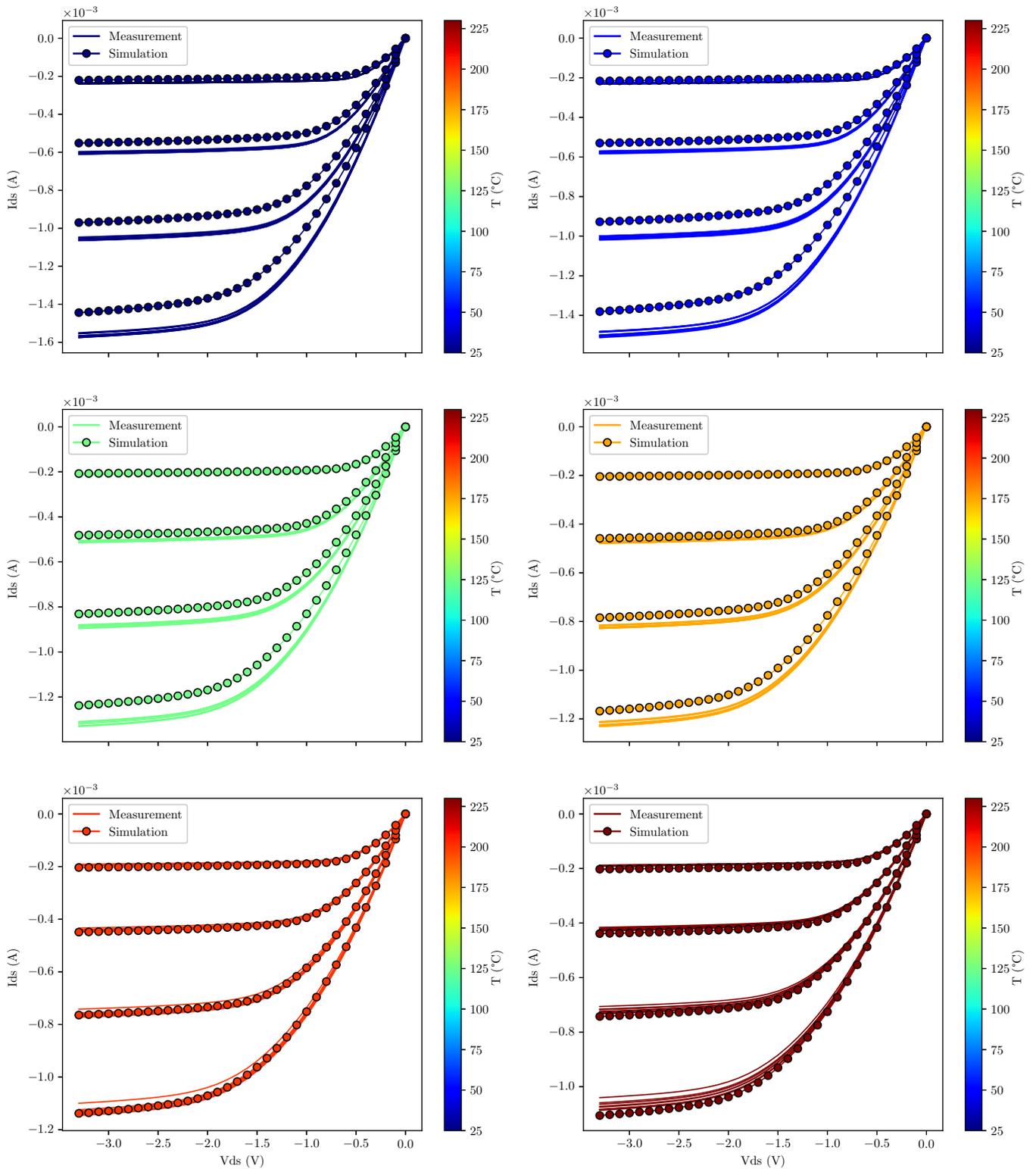


Figure 30: $I_{ds} - V_{ds}$ curves of 3.3V pMOS ($W/L=10/0.6\mu\text{m}$) at different temperatures. The values of V_{gs} are -1.5V, -2.1V, -2.7V, -3.3V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

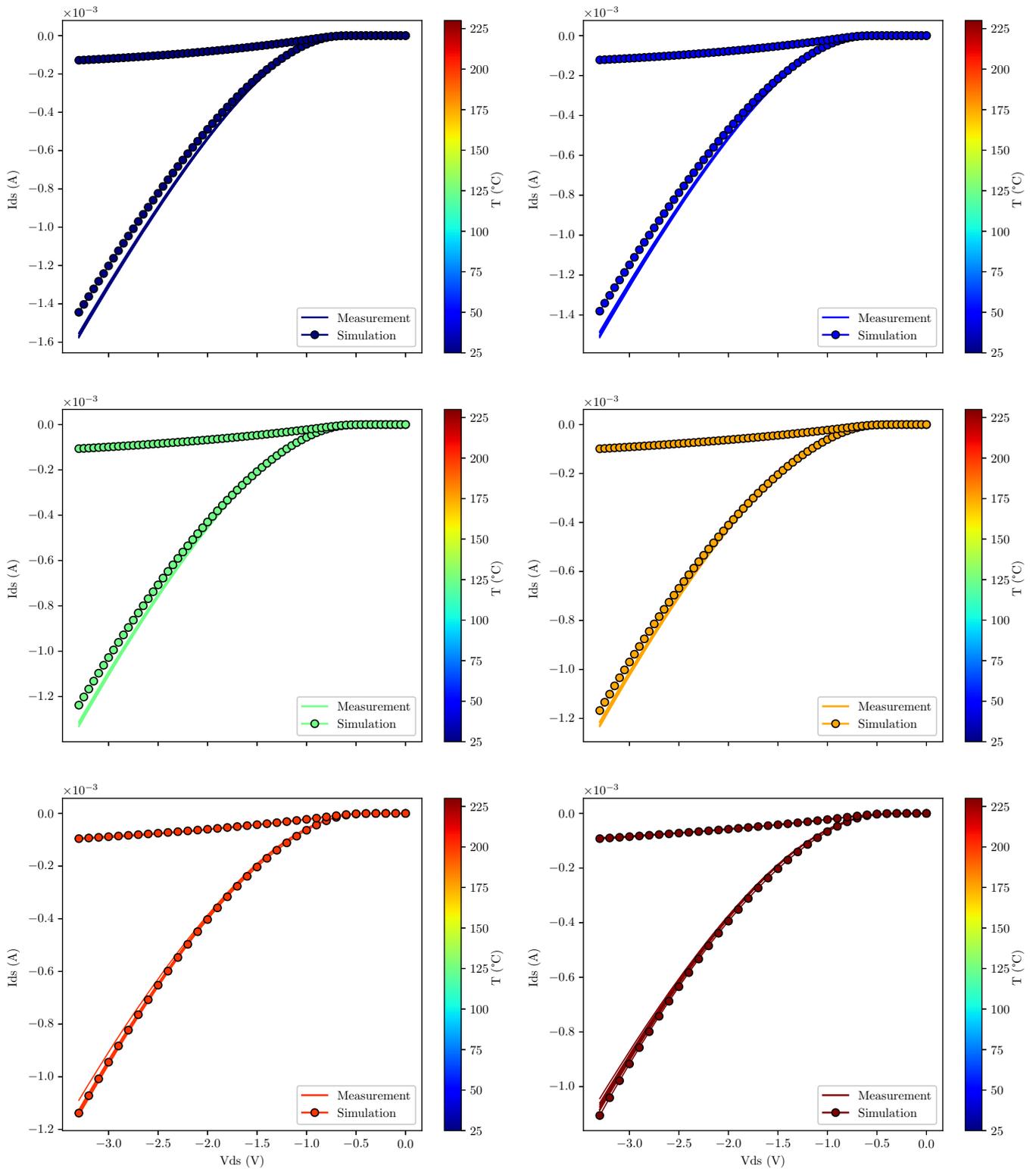


Figure 31: $I_{ds}-V_{gs}$ curves of 3.3V pMOS ($W/L=10/0.6\mu m$) at different temperatures. Values of V_{ds} are -0.1V and -3.3V, respectively. The color indicates the according temperature. x-axis of all figures are in the same scale

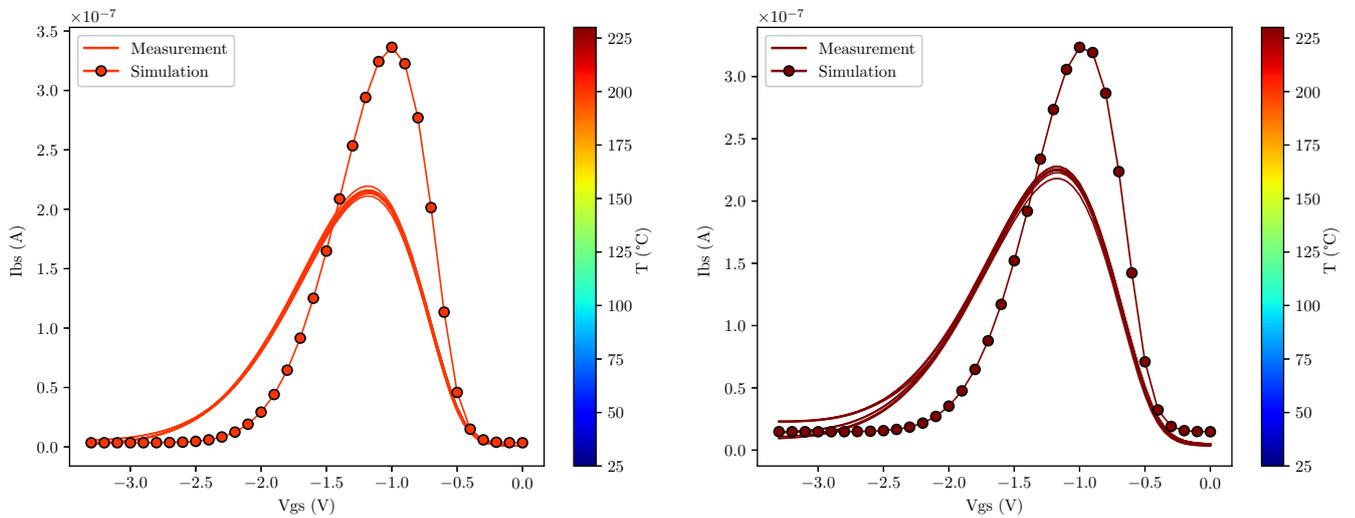


Figure 32: $I_{bs} - V_{gs}$ curves of 3.3V pMOS ($W/L=10/0.6\mu\text{m}$) at different temperatures and $V_{ds}=-3.3\text{V}$. The color indicates the according temperature.

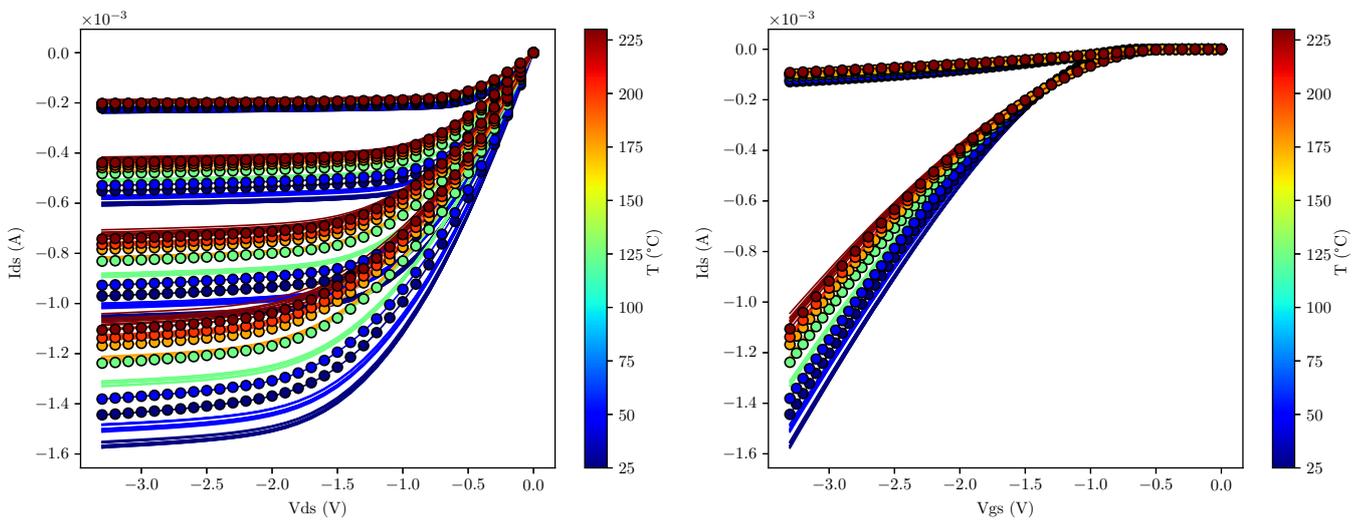


Figure 33: Comparisons of measurements (circle marks) and simulations (solid lines) of 3.3V pMOS ($W/L=10/0.6\mu\text{m}$) at different temperatures. The color indicates the according temperature.

Summary

Device	W/L	$T^{\circ}\text{C} \leq 175^{\circ}\text{C}$	$200 \leq T^{\circ}\text{C} \leq 230^{\circ}\text{C}$
1.8V nMOS	10 μm / 0.18 μm	- Process deviation $\leq 3.8\%$ - Simulation difference $\leq 10.4\%$	- Process deviation $\leq 12.2\%$ (*) - Simulation difference $\leq 19.4\%$
	10 μm / 0.5 μm	- Process deviation $\leq 1.4\%$ - Simulation difference $\leq 8.4\%$	- Process deviation $\leq 11.3\%$ (*) Simulation difference $\leq 14.8\%$
3.3V nMOS	10 μm / 0.35 μm	- Process deviation $\leq 1.4\%$ - Simulation difference $\leq 11.4\%$	- Process deviation $\leq 11.7\%$ (*) - Simulation difference $\leq 23.1\%$
	10 μm / 0.5 μm	- Process deviation $\leq 1.8\%$ - Simulation difference $\leq 9.4\%$	- Process deviation $\leq 4.85\%$ - Simulation difference $\leq 14.8\%$
1.8V pMOS	10 μm / 0.18 μm	- Process deviation $\leq 2.6\%$ - Simulation difference $\leq 10.3\%$	- Process deviation $\leq 20.0\%$ (*) - Simulation difference $\leq 20.0\%$
	10 μm / 0.5 μm	- Process deviation $\leq 4.8\%$ - Simulation difference $\leq 12.5\%$	- Process deviation $\leq 2.7\%$ - Simulation difference $\leq 12.5\%$
3.3V pMOS	10 μm / 0.3 μm	- Process deviation $\leq 1.5\%$ - Simulation difference $\leq 5\%$	- Process deviation $\leq 5.7\%$ - Simulation difference $\leq 8.1\%$
	10 μm / 0.6 μm	- Process deviation $\leq 3.3\%$ - Simulation difference $\leq 8\%$	- Process deviation $\leq 1.1\%$ - Simulation difference $\leq 3.7\%$

(*) Result deviations were caused by measurement set-up issues. They do not reflect the real process deviation.

Appendix B

C code integrated CHE and DAHC model for 1.8V nMOS transistors is presented hereafter. The C code for NBTI model for 1.8V and 3.3V pMOS transistors are 80% similar to the one below and it has been explained in Chapter 5, therefore, it is not necessary to include here.

```
1 // file nmosYen.h
2
3 #ifndef _NMOSYENDEF_H_
4 #define _NMOSYENDEF_H_
5
6 typedef struct nmosYen {
7     /* user defined model goes here */
8     double n;
9     double nl;
10    double nh;
11    double alpha;
12    double Cl;
13    double Ch;
14    double Ea;
15    double KB;
16    double m;
17    double rel_vth0;
18    int agelevel;
19 } NMOSYEN;
20
21 /* Defined the Spectre native reliability
22 * analysis data type. This data structure
23 * is only used by Spectre. */
24 static URI_Param uriModelParams[] = {
25     {"n", uriRealType},
26     {"nl", uriRealType},
27     {"nh", uriRealType},
```

```

28     { "alpha", uriRealType },
29     { "Cl", uriRealType },
30     { "Ch", uriRealType },
31     { "Ea", uriRealType },
32     { "KB", uriRealType },
33     { "m", uriRealType },
34     { "rel_vth0", uriRealType },
35 };
36
37
38 /* variables passed among uri routines */
39
40 typedef struct nmosYenSharedInstState {
41     /* instance parameters related to geometry */
42     double mult;
43     double l;
44     double w;
45     char devName[1024];
46     char modName[1024];
47 } NMOSYENSHAREDINSTSTATE;
48
49 typedef struct nmosYenInstState {
50     /* instance parameters related to bias */
51     double totaldeg;
52     double agerate;
53     double deltaD;
54 } NMOSYENINSTSTATE;
55
56 #endif
57
58 // file nmosYen.c
59
60 #include "uri.h"
61 #include "nmosYen.h"
62 #include <string.h>
63 #include <stdlib.h>

```

```

64 #include <stdio.h>
65 #include <math.h>
66
67 /*
68  * this function set up the reliability parameters needed and the default
69  * values for the reliability parameters
70  * returns 0 if successful
71  */
72 int nmosYenSetupModel( URI_Model *model, const char *const modelType,
73                       const int isDebug )
74 {
75     NMOSYEN *mymodel = ( NMOSYEN * )model;
76     mymodel->n = 0.0; /* n */
77     mymodel->n1 = 0.0; /* n */
78     mymodel->nh = 0.0; /* n */
79     mymodel->alpha = 0.0; /* n */
80     mymodel->C1 = 0.0; /* n */
81     mymodel->Ch = 0.0; /* n */
82     mymodel->Ea = 0.0; /* n */
83     mymodel->KB = 0.0; /* n */
84     mymodel->m = 0.0; /* n */
85     mymodel->rel_vth0 = 0.0; /* n */
86     mymodel->agelevel = -1;
87     if ( isDebug ) {
88         printf( "nmosYenSetupModel done\n" );
89     }
90     return 0;
91 }
92
93 /*
94  * this function assigns the model parameter values from the model card
95  * returns 0 if successful
96  */
97 int nmosYenAddParam( URI_Model *model, const char *const name,
98                    const double value, const char *strvalue, const int
isDebug )

```

```

99 {
100     NMOSYEN *mymodel = ( NMOSYEN * )model;
101     if ( isDebug ) {
102         printf( "nmosYenAddParam ... name %s, value:%f ", name, value );
103     }
104     if ( strcasecmp( name, "NL" ) == 0 ) {
105         mymodel->nl = value;
106         if ( isDebug ) {
107             printf( " parameter nl=%f for low temperature assigned\n",
mymodel->nl );
108         }
109         return 0;
110     } if ( strcasecmp( name, "NH" ) == 0 ) {
111         mymodel->nh = value;
112         if ( isDebug ) {
113             printf( " parameter nh=%f for high temperature assigned\n",
mymodel->nh);
114         }
115         return 0;
116     } else if ( strcasecmp( name, "ALPHA" ) == 0 ) {
117         mymodel->alpha = value;
118         if ( isDebug ) {
119             printf( " parameter alpha=%f assigned\n", mymodel->alpha );
120         }
121         return 0;
122     } else if ( strcasecmp( name, "CL" ) == 0 ) {
123         mymodel->Cl = value;
124         if ( isDebug ) {
125             printf( " parameter Cl=%f for low temperature assigned\n",
mymodel->Cl);
126         }
127         return 0;
128     } else if ( strcasecmp( name, "CH" ) == 0 ) {
129         mymodel->Ch = value;
130         if ( isDebug ) {

```

```

131         printf( " parameter Ch=%f for high temperature assigned\n",
mymodel->Ch );
132     }
133     return 0;
134 } else if ( strcasecmp( name, "M" ) == 0 ) {
135     mymodel->m = value;
136     if ( isDebug ) {
137         printf( " parameter m=%f assigned\n", mymodel->m );
138     }
139     return 0;
140 } else if ( strcasecmp( name, "EA" ) == 0 ) {
141     mymodel->Ea = value;
142     if ( isDebug ) {
143         printf( " parameter Ea=%f assigned\n", mymodel->Ea);
144     }
145     return 0;
146 } else if ( strcasecmp( name, "KB" ) == 0 ) {
147     mymodel->KB = value;
148     if ( isDebug ) {
149         printf( " parameter KB=%f assigned\n", mymodel->KB);
150     }
151     return 0;
152 } else if ( strcasecmp( name, "REL_VTH0" ) == 0 ) {
153     mymodel->rel_vth0 = value;
154     if ( isDebug ) {
155         printf( " parameter rel_vth0=%f assigned\n", mymodel->
rel_vth0);
156     }
157     return 0;
158 } else if ( strcasecmp( name, "AGELEVEL" ) == 0 ) {
159     mymodel->agelevel = ( int )( value + 0.5 );
160     if ( isDebug ) {
161         printf( " parameter AGELEVEL=%f assigned\n", mymodel->
agelevel );
162     }
163     return 0;

```

```

164     }
165     if ( isDebug ) {
166         printf( "failed\n" );
167     }
168     return 1;
169 }
170
171 int nmosYenInitAllParams( URI_Model *model, const URI_Env *const env,
172     const int isDebug, URI_sharedInstState *st1 )
173 {
174     NMOSYEN *mymodel = ( NMOSYEN * )model;
175
176     double T = env->temp;
177     if(T>=150)
178         mymodel->n = mymodel->nh;
179     else
180         mymodel->n = mymodel->n1;
181     printf("Temperature is %f, take n = %f\n", T, mymodel->n);
182 }
183 /* This function is used to add vector model parameters into URI model.
184 * Currently no vector parameter is needed. Keep the function for
185 * compability
186 */
187 int nmosYenAddVectorParam( URI_Model *model, const char *const name,
188     const double *value,
189     const int size, const int isDebug )
190 {
191     int i = 0;
192     NMOSYEN *mymodel = ( NMOSYEN * )model;
193     if ( isDebug ) {
194         printf( "nmosYenAddVectorParam ... No vector parameter is needed
195         .\n" );
196     }
197     return 0;
198 }

```

```

196 /*
197  * This function is used to free the memoery allocated to save vector
198  * parameters if exist.
199  * */
200 int nmosYenDeleteModel( URI_Model *model,  URI_sharedInstState *st1 ,
201                        URI_InstState *st2 ,
202                        const int isDebug )
203 {
204     NMOSYEN *mymodel = ( NMOSYEN * )model;
205     if ( isDebug ) {
206         printf( "nmosYenDeleteModel ...\\n" );
207     }
208     return 0;
209 }
210
211 /*
212  * this function calculates the age rate value
213  * returns age rate value if successful
214  */
215 double nmosYenCalcA( URI_Model *model, const URI_Var *const uriVar ,
216                    const URI_Env *const env, const int isDebug ,
217                    URI_sharedInstState *st1, URI_InstState *st2 )
218 {
219     NMOSYEN *mymodel = ( NMOSYEN * )model;
220     URI_MosVar *uriMosVar = ( URI_MosVar * )uriVar;
221     NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2;
222     NMOSYENSHAREDINSTSTATE *s1 = ( NMOSYENSHAREDINSTSTATE * )st1;
223     double ageRate = 0.0;
224     float vgs = uriMosVar->vgs;
225     float vds = uriMosVar->vds;
226     float vth = uriMosVar->von;
227     float w = uriMosVar->weff;
228     float l = uriMosVar->leff;
229
230     double Cl = mymodel->Cl;
231     double Ch = mymodel->Ch;

```

```

230 double n = mymodel->n;
231 double Ea = mymodel->Ea;
232 double KB = mymodel->KB;
233 double m = mymodel->m;
234 double alpha = mymodel->alpha;
235 double T = env->temp + 273.15;
236 double C=0.0;
237
238 if( fabs(vgs) < vth)
239 {
240     ageRate = 0;
241     if(isDebug)
242         printf("mosfet is in cutoff mode, agerate is set to 0 vgs = %
243 f vth=%.15f for %s (%s)\n", vgs, vth, s1->devName, s1->modName);
244 }
245 else
246 {
247     if(T >= (150+273.15))
248         C=Ch*exp(-Ea/(KB*T));
249     else
250         C = Cl;
251     ageRate = C * pow(w/l, m) * exp(-alpha/fabs(vds));
252     ageRate = pow(ageRate, 1/n);
253     if(isDebug)
254         printf("Yen: agerate is %.15f vgs = %f vth=%.15f for %s (%s),
255 w=%.15f, l=%.15f, C=%.15f vds=%.15f\n", ageRate, vgs, vth, s1->
256 devName, s1->modName,w, l, C, vds );
257 }
258
259 if (ageRate < 0.0) abort();
260 s2->agerate = ageRate;
261 return ageRate;
262 }
263 /*

```

```

263  * this function calculates the delta degradation
264  * returns delta degradation if successful
265  */
266  double nmosYenCalcDeltaD( URI_Model *model, const URI_Var *const uriVar ,
267                          const int isDebug, URI_sharedInstState *st1 ,
268                          URI_InstState *st2 ,
269                          const URI_Env *const env )
270  {
271      NMOSYEN *mymodel = ( NMOSYEN * )model;
272      NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2;
273      URI_MosVar *uriMosVar = ( URI_MosVar * )uriVar;
274      NMOSYENSHAREDINSTSTATE *s1 = ( NMOSYENSHAREDINSTSTATE * )st1;
275
276      double deltaD = s2->deltaD;
277      double n = mymodel->n;
278      double ageRate = s2->agerate;
279
280      if( ageRate > 0.0)
281      {
282          double tmpDeg = s2->agerate * uriMosVar->dt;
283          deltaD = pow( pow( deltaD , 1.0 / n ) + tmpDeg , n );
284          s2->deltaD = deltaD;
285      }
286
287      if ( isDebug ) {
288          printf( "Yen nmosYenCalcDeltaD done for %s (%s), deltaD=%.15f,
289          ageRate=%.18f\n" ,s1->devName, s1->modName, deltaD , ageRate);
290      }
291
292      return deltaD;
293  }
294
295  /*
296  * this function calculates the total age value up to the simulation time
297  * returns the total age value
298  */

```

```

296 double nmosYenCalcDeltaAge( URI_Model *model, const URI_Var *const uriVar
    ,
297                                     const int isDebug, URI_sharedInstState *st1 ,
    URI_InstState *st2 ,
298                                     const URI_Env *const env )
299 {
300     NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2 ;
301     URI_MosVar *uriMosVar = ( URI_MosVar * )uriVar ;
302
303     if ( isDebug ) {
304         printf( "dt = %f nmosYenCalcDeltaAge done. No need to calculate
    delta age \n", uriMosVar->dt );
305     }
306     return 0;
307 }
308
309 /*
310 * this function calculates the final age value for the times specified
311 * with .age.
312 * returns the final total age value
313 */
314 double nmosYenCalcAge( URI_Model *model, const double futuretime ,
315                       const int isDebug, URI_sharedInstState *st1 ,
    URI_InstState *st2 ,
316                       const URI_Env *const env )
317 {
318     NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2 ;
319     NMOSYENSHAREDINSTSTATE *s1 = ( NMOSYENSHAREDINSTSTATE * )st1 ;
320     NMOSYEN *mymodel = ( NMOSYEN * )model ;
321
322     if ( isDebug ) {
323         printf( "Starting CalcAge(): ( dev: %s; mod: %s ). No need to
    calculate Age\n", s1->devName, s1->modName );
324     }
325     return 0;
326 }

```

```

327
328 /*
329  * this function calculates the final degradation value for the times
330  * specified with .age.
331  * returns the final degradation value
332  */
333 double nmosYenCalcDegradation( URI_Model *model, const URI_Var *const
    uriVar ,
334                               const double futuretime , const int isDebug
    ,
335                               URI_sharedInstState *st1 , URI_InstState *
    st2 ,
336                               const URI_Env *const env )
337 {
338     NMOSYEN *mymodel = ( NMOSYEN * )model;
339     NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2;
340     NMOSYENSHAREDINSTSTATE *s1 = ( NMOSYENSHAREDINSTSTATE * )st1;
341     double deg;
342
343     if ( isDebug ) {
344         printf( "Starting CalcDegradation(): ( dev: %s; mod: %s )\n", s1
    ->devName , s1->modName );
345     }
346
347     deg = s2->deltaD * pow( futuretime / ( env->tStop - env->tStart ) ,
    mymodel->n );
348     if ( isDebug ) {
349         printf( "nmosYenCalcDegradation done, deltaD=%.15f, sim time %.15
    f, deg=%f, futuretime %f, n=%f \n", s2->deltaD ,(env->tStop - env->
    tStart), deg , futuretime , mymodel->n);
350     }
351     s2->totaldeg = deg;
352     return deg;
353 }
354
355 /*

```

```

356 * this function calculates the final lifetime value for degradation
357 * criterion specified in .degrad statement
358 * Please note that this degradation criterion is not the degradation in
    percentage.
359 * It's the degradattion at which we want to calculate lifetime
360 * returns the final lifetime value
361 */
362 double nmosYenCalcLifetime( URI_Model *model, const double age,
363                             const double degAtLifetime, const int isDebug
    ,
364                             URI_sharedInstState *st1, URI_InstState *st2,
365                             const URI_Env *const env )
366 {
367     NMOSYEN *mymodel = ( NMOSYEN * )model;
368     NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2;
369     NMOSYENSHAREDINSTSTATE *s1 = ( NMOSYENSHAREDINSTSTATE * )st1;
370     double lt;
371
372     if ( isDebug ) {
373         printf( "Starting CalcLifeTime(): ( dev: %s; mod: %s )\n", s1->
    devName, s1->modName );
374     }
375
376     lt = ( env->tStop - env->tStart ) * pow( degAtLifetime / s2->deltaD,
    1 / mymodel->n );
377     if ( isDebug ) {
378         printf( "nmosYenCalcLifetime done. Lifetime is %f\n", lt);
379     }
380     return lt;
381 }
382
383 /*
384 * this function returns the degraded spice parameter value
385 *
386 */
387 double nmosYenScaleParam( URI_Model *model, const double age,

```

```

388         const char *const name, const double value ,
const int isDebug ,
389         const URI_Var *const uriVar , const
URI_sharedInstState *const st1 ,
390         const URI_Env *const env , const URI_InstState *
const st2 )
391 {
392     NMOSYEN *mymodel = ( NMOSYEN * )model;
393     NMOSYENSHAREDINSTSTATE *s1 = ( NMOSYENSHAREDINSTSTATE * )st1;
394
395     if ( !strcasecmp( name, "VTH0" ) ) {
396         NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2;
397         double vthdeg = s2->totaldeg;
398         double sign;
399         if(value < 0.0) sign = -1;
400         else sign = 1;
401         double degraded = value + sign* vthdeg;
402         printf( "Beginning with vth0 %.15f, deg=%f ending value %.15f,
defined para %.15f Starting ScaleParam(): %s ( dev: %s; mod: %s )\n",
value , vthdeg , degraded , mymodel->rel_vth0 , name , s1->devName , s1->
modName );
403         if(fabs(value - mymodel->rel_vth0) > fabs(0.00001*mymodel->
rel_vth0))
404             {
405                 printf("You have change the size of nmos/pmos, please
readapte the value of rel_vth0 , provied value %.15f, it should be %.15
f\n", mymodel->rel_vth0 , value);
406                 abort();
407             }
408         return degraded;
409     } else {
410         return value;
411     }
412 }
413
414 /*

```

```

415 * this function adds all instance parameters into URI states , such as l,
      w, m.
416 * NOTE: All MOS device parameters can be added into URI states with this
      func.
417 *      but for external users , the argu "name" must be the same as the
      param
418 *      name in device definition , such as ad, as, w, l ...
419 */
420 int nmosYenAddInstParam( URI_Model *model, URI_sharedInstState *st1,
      URI_InstState *st2, const char *const name, const double value, const
      char *strvalue )
421 {
422     NMOSYENSHAREDINSTSTATE *s1 = ( NMOSYENSHAREDINSTSTATE * )st1;
423     // NMOSYENINSTSTATE *s2 = ( NMOSYENINSTSTATE * )st2;
424     if ( s1 != 0 ) {
425         if ( strcmp( name, "l" ) == 0 ) {
426             s1->l = value;
427             return 0;
428         } else if ( strcmp( name, "w" ) == 0 ) {
429             s1->w = value;
430             return 0;
431         } else if ( strcmp( name, "mult" ) == 0 ) {
432             s1->mult = value;
433             return 0;
434         } else if ( strcmp( name, "device_name" ) == 0 ) {
435             strcpy( s1->devName, strvalue );
436         } else if ( strcmp( name, "model_name" ) == 0 ) {
437             strcpy( s1->modName, strvalue );
438         }
439         // TODO: add other instance parameters , such as ad, as ...
440     }
441     return 1;
442 }
443
444 static NMOSYEN nmosYenMod;
445

```

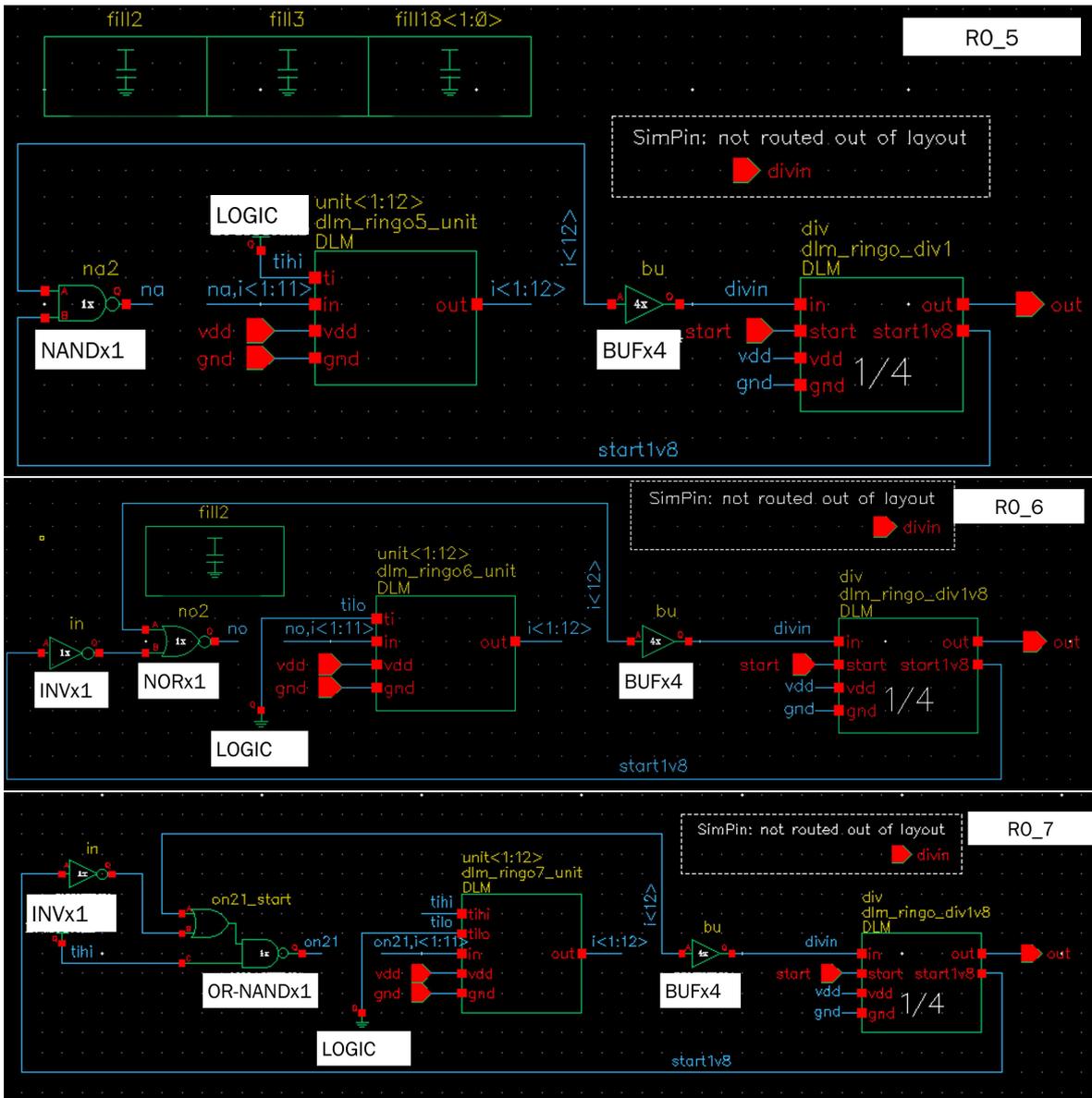
```

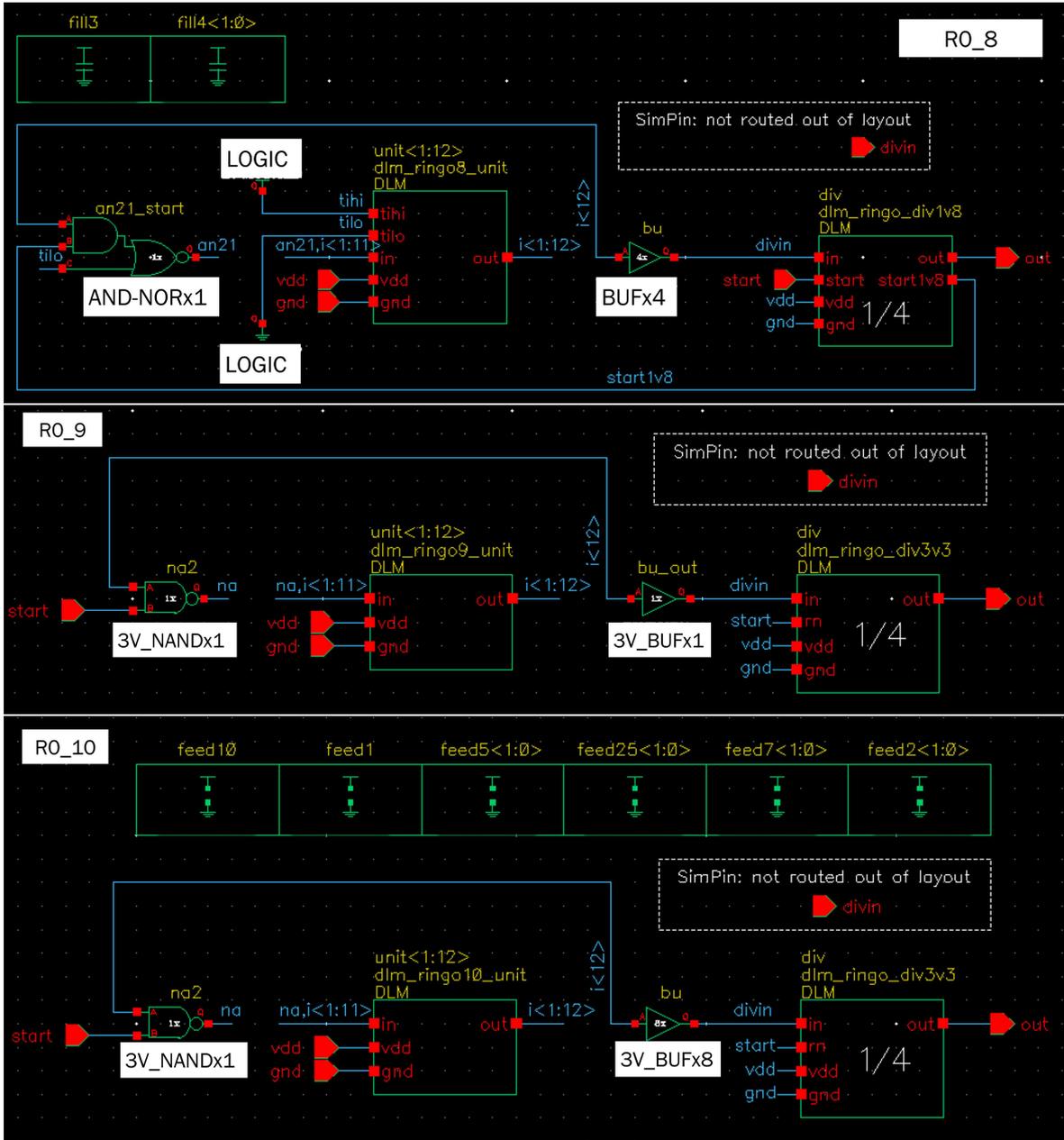
446 static URI_ModelDef nmosYenModDef = {
447     ( URI_Model * ) &nmosYenMod ,
448     104 ,
449     sizeof( NMOSYEN ) ,
450     uriModelParams ,
451     sizeof( uriModelParams ) / sizeof( uriModelParams[0] ) ,
452     nmosYenSetupModel ,
453     nmosYenAddParam ,
454     nmosYenInitAllParams , // nmosYenInitAllParams
455     nmosYenCalcA ,
456     nmosYenCalcDegradation ,
457     nmosYenCalcLifetime ,
458     nmosYenScaleParam ,
459     nmosYenCalcAge ,
460     nmosYenCalcDeltaD ,
461     nmosYenCalcDeltaAge ,
462     nmosYenAddVectorParam ,
463     nmosYenDeleteModel ,
464     nmosYenAddInstParam ,
465     NULL, // nmosYenCopyInstState ,
466     NULL, // nmosYenGetModelParam ,
467     NULL, // nmosYenGetModelVectorParam ,
468     NULL, // nmosYenGetInstParam ,
469     NULL, // nmosYenGetInstVectorParam ,
470     sizeof( NMOSYENSHAREDINSTSTATE ) ,
471     sizeof( NMOSYENINSTSTATE ) ,
472 };
473
474 URI_ModelDef *nmosYenDefPtr = &nmosYenModDef;

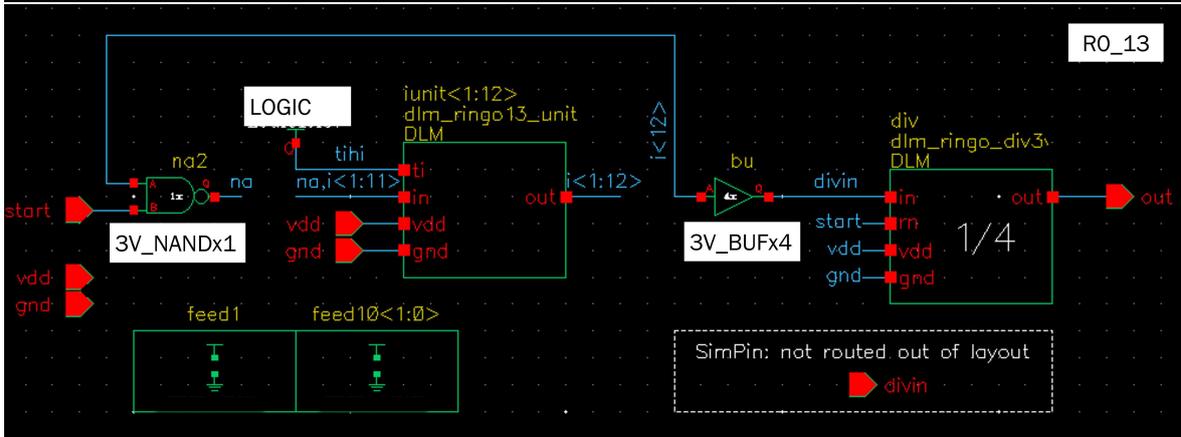
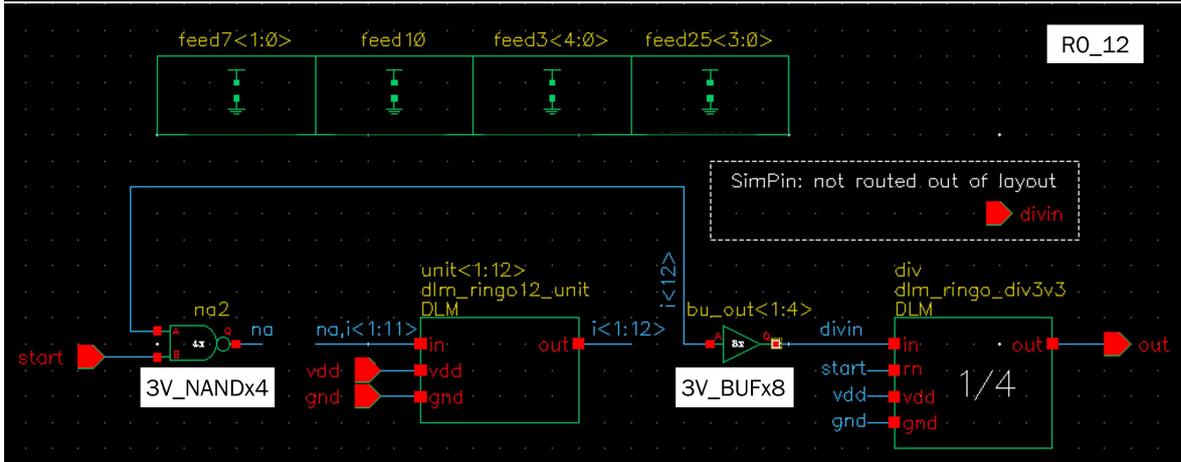
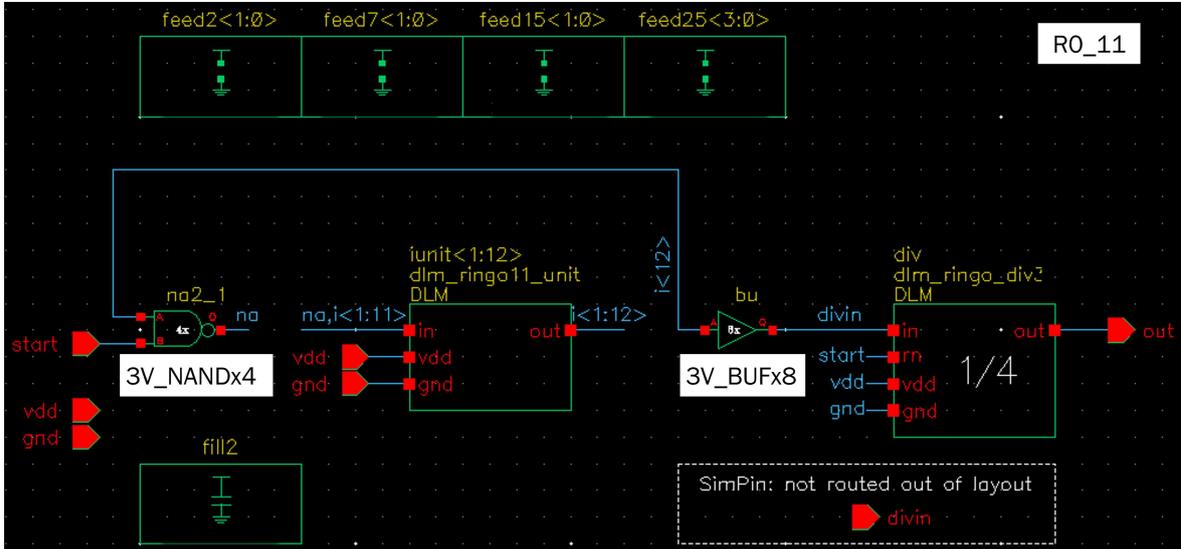
```

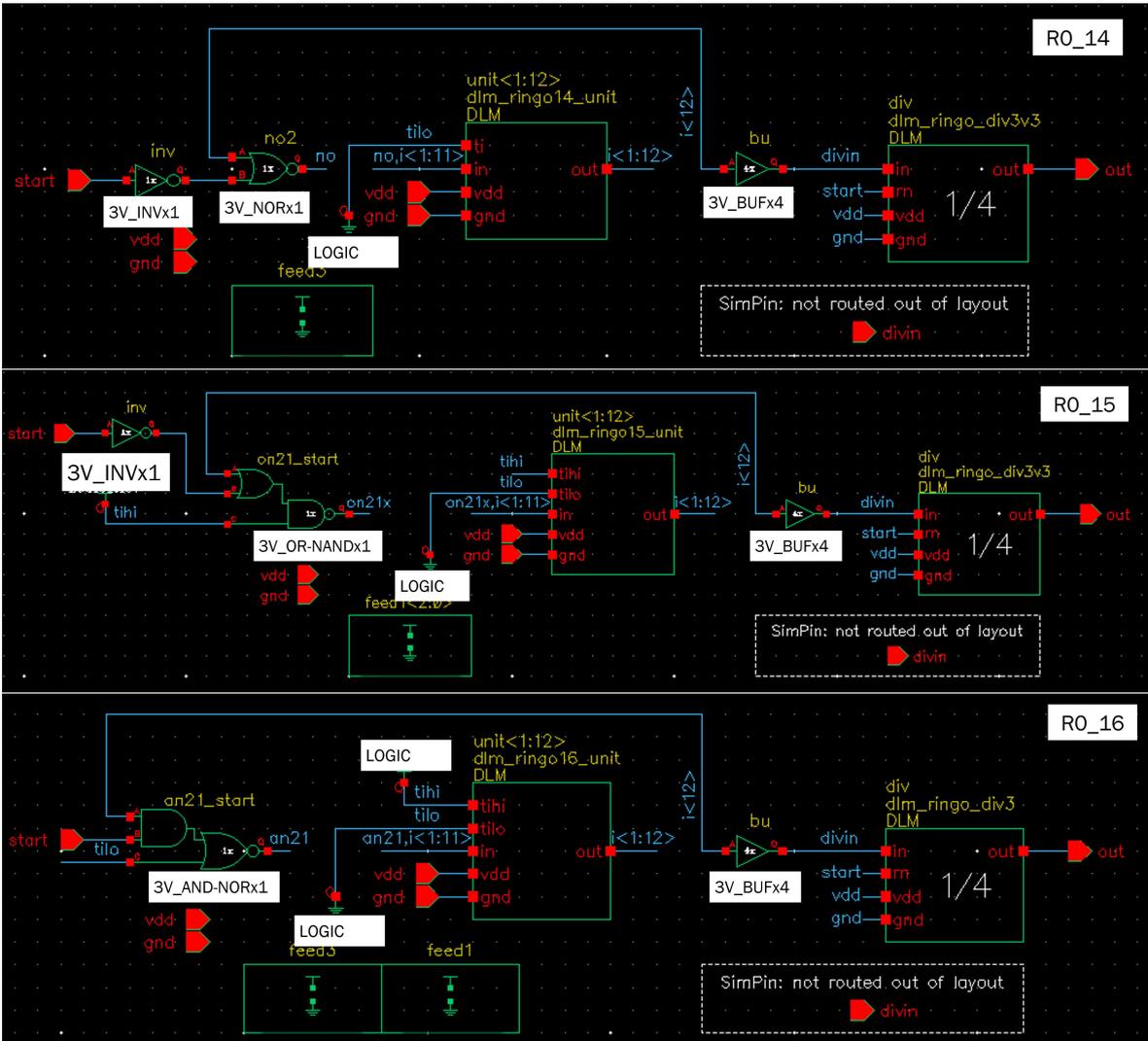
Appendix C

The schematics of RO_2 to RO_16 are listed hereafter:









Author Publication List

International conferences

1. **Yen Tran**, Toshihiro Nomura, Mohamed Salim Cherchali, Claire Tassin, Yann Deval, Cristell Maneux, “**Bias Temperature Instability Characterization and Modeling for 0.18um CMOS Under Extreme Thermal Stress Conditions**”; SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME, 2021, pp. 1-4.
2. **Yen Tran**, Toshihiro Nomura, Mohamed Salim Cherchali, Claire Tassin, Yann Deval, Cristell Maneux, “**Reliability Investigation of 0.18um CMOS for Oilfield Applications**”; SMACD / PRIME 2021; International Conference on SMACD and 16th Conference on PRIME, 2021, pp. 1-4.
3. **Yen Tran**, Toshihiro Nomura, Mohamed Salim Cherchali, Claire Tassin, Yann Deval, Cristell Maneux, “**0.18um CMOS Ring Oscillator: NBTI and HCI Investigation**”; International Conference on Analog VLSI Circuits (AVIC), Bordeaux, October 18-20, 2021.
4. **Yen Tran**, Toshihiro Nomura, Mohamed Salim Cherchali, Claire Tassin, Yann Deval, Cristell Maneux, “**Investigation of 0.18um CMOS Sensitivity to BTI and HCI Mechanisms under Extreme Thermal Stress Conditions**”; Asian Test Symposium (ATS), Japan, virtual event, November 22-24, 2021.
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