

# AC-DC converter based on piezoelectric material and adiabatic power Transfer

Mustapha Touhami

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### THÈSE

Pour obtenir le grade de



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## Convertisseur AC-DC piézoélectrique à transfert de puissance adiabatique

## AC-DC converter based on piezoelectric material and adiabatic power Transfer

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#### Invités :

"A mes parents..."

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"Louange à Allâh par Lequel les bonnes choses se réalisent".

« الحمد لله الذي بنعمته تتم الصالحات »

### Abstract

oday, the demand for electronic devices continues to increase with the requirements for miniaturization. Most of the volume of the power supply are occupied by the passive components. Therefore, one of the major challenges consists of reducing the size of these passives' components. Conventional solutions based on magnetic components tend to be limited by the physical properties of ferromagnetic materials. Small scale integration is thus stopped by these intrinsic limitations, which makes it difficult to achieve high efficiency and high power density power supplies.

A new mechanism has been developed recently based on piezoelectric resonators. The mechanism consists of transforming an input electrical energy into a mechanical energy before restoring it to an electrical load with the right voltage. The piezoelectric materials are widely used for sensing (accelerometer, force sensor ...), harvesting energy (vibration, deformation), or actuating (sonar, ultrasonic cleaner, scanning microscope). These materials offers several advantages, such as can be integrated while achieving small scale, and offering high quality factor and electromechanical coupling factor, enabling high power density and high efficiency operation. Also, they have an LC-resonator behavior, which enables their use in resonant converters. Nevertheless, their usage in power converters should be investigated for a better utilization.

Therefore, in the first part of this thesis, we studied the conversion mechanism, that alternates between connected voltage stage for charge transfer and open circuit stage for soft changing of the voltage level across the piezoelectric resonator (PR) and performing soft-switching, reducing losses and EMI interference. A generic model of six-stages based switching sequence is developed, this model estimates the timing of each stage and the amplitude of the current related to the amplitude of the vibration. Furthermore, we propose a dc-dc converter based on PR targeting high-to-low voltage and low power applications (up to 100 W), suitable for grid to load power supply. Indeed, the proposed topology enables high step-down voltage conversion and minimizes the stored energy in the PR.

In the second part, we propose a design of the DC-DC converter based on PR, with an actual circuit for an input voltage up to 250 V and an output voltage up to 125 V. This converter achieved an output power up to 50 W with an efficiency of 93 % for radial mode vibration at frequency near 90 kHz, and an output power up to 175 W for thickness mode vibration at a

frequency of 1 MHz. Experimental waveforms are exhibited, which show how the conversion cycle evolves through the various operating conditions.

After that, we have focused on the development of a first control strategy for closed-loop operation for such a conversion principle. The control strategy enables load regulation, while achieving the conversion cycle, the soft switching operation, soft-charging and phase/frequency control for the synchronization with the mechanical vibration of the PR. The control strategy is then implemented in a Field Programmable Gate Arrays (FPGA) with the development of a suited control circuit, for a high step-down DC-DC converter. An actual prototype was designed for input voltage up to 120 V and output voltage < 48 V. The implemented control demonstrates good performances in terms of response time (less than 2 ms) and the voltage overshoot not exceeds 10 % of the output voltage.

At the end of this manuscript, we investigate on piezoelectric materials suited for power converters based on piezoelectric resonators. The investigation aims the increasing of the operating frequency, reducing the spurious modes interference, achieving high quality and electromechanical factors and mechanical mounting by using lithium niobate (LNO). Then, a fabricated LNO based PR is presented, with an actual circuit for an operating frequency up to 7 MHz. The proposed circuit covers a power range of 2-32 W with an input to output voltage of 60 to 20 V. This part is presented in **APPENDIX A**.

Then, we finish by presenting our perspectives and main challenges that can be investigated in the future, and the potential opportunities of power conversion based on piezoelectric resonators.

### Résumé

ujourd'hui, la demande de dispositifs électroniques continue d'augmenter avec des exigences de miniaturisation et de réduction de la taille des alimentations. La majeure partie du volume des alimentations est généralement occupée par les composants passifs. Par conséquent, l'un des principaux défis consiste à réduire la taille de ces composants passifs. Les solutions conventionnelles basées sur les composants magnétiques ont tendance à être limitées par les propriétés physiques des matériaux ferromagnétiques. Leur miniaturisation est donc freinée par ces limitations intrinsèques, ce qui rend difficile la réalisation d'alimentations à haut rendement et à haute densité de puissance.

Un nouveau mécanisme a été développé récemment, basé sur des résonateurs piézoélectriques (ou piézo-résonateurs PR). Ce mécanisme consiste à transformer l'énergie électrique prélevée à une source en énergie mécanique stockée dans un résonateur mécanique avant de la restituer sous forme électrique à une charge sous la tension souhaitée. Les matériaux piézoélectriques sont largement utilisés pour les applications telles que la mesure (accéléromètre, capteur de pression...), des systèmes de récupération d'énergie (vibratoire, déformation mécanique...), des actionneurs électromécaniques (sonar, nettoyeur ultra-son, injecteur...). Ces matériaux offrent plusieurs avantages, tels que la réduction de volume ou encore la possibilité d'intégration. Par ailleurs, leur facteur de qualité élevé et leur facteur de couplage électromécanique élevé permettent d'atteindre une densité de puissance élevée et un fonctionnement à haut rendement. Ces matériaux peuvent se comporter comme des résonateurs LC, permettant ainsi leur utilisation dans les convertisseurs résonants. Néanmoins, leur utilisation dans les convertisseurs de puissance doit donc être investiguée pour une meilleure utilisation.

Dans la première partie de cette thèse, nous avons étudié le mécanisme de conversion, qui alterne entre une phase à tension constante pour échanger des charges électriques et une phase à circuit ouvert pour changer le niveau de tension du PR de manière douce et ainsi effectuer des commutations à zéro de tension. Ce fonctionnement permet la conversion de puissance avec de faibles pertes et de faibles interférences électromagnétiques. Un modèle générique pour un cycle de conversion contenant six phases est développé, ce modèle permet d'estimer la durée de chaque phase ainsi que l'amplitude du courant qui est l'image de l'amplitude des vibrations du résonateur. Nous proposons également un convertisseur continu-continu basé sur le PR visant une application pour une conversion de haute vers basse tension et une puissance faible (jusqu'à 100 W), cette structure est adaptée pour les appareils s'alimentant à partir du réseau domestique. En effet, la topologie proposée permet une conversion à fort abaissement de tension et une minimisation de l'énergie stockée dans le PR.

Dans la deuxième partie, nous proposons la conception d'un convertisseur continu-continu basé sur le PR, conçu et réalisé pour une tension d'entrée allant jusqu'à 250 V et une tension de sortie allant jusqu'à 125 V. Ce convertisseur a atteint une puissance de sortie de 50 W avec un rendement de 93 % pour un mode vibration radial à une fréquence proche de 90 kHz, et une puissance de sortie de 175 W en mode de vibration d'épaisseur à une fréquence de 1 MHz. Des formes d'onde expérimentales sont présentées, qui montrent comment le cycle de conversion évolue en fonction des différentes conditions de fonctionnement.

Par la suite, nous nous sommes concentrés sur le développement d'une première stratégie de contrôle pour un fonctionnement en boucle fermée pour ce nouveau principe de conversion. La stratégie de contrôle permet la régulation de la tension de sortie, tout en réalisant le cycle de conversion, des commutations douces et le contrôle de phase/fréquence pour la synchronisation du cycle de pilotage avec la vibration mécanique du PR. La stratégie de contrôle est implémentée dans un Field Programmable Gate Arrays (FPGA), constituant le circuit de contrôle adapté pour un convertisseur DC-DC fortement abaisseur. Un prototype a été conçu pour une tension d'entrée allant jusqu'à 120 V et une tension de sortie < 48 V. Le contrôle implémenté a montré de bonnes performances en termes de temps de réponse (moins de 2 ms) et de dépassement de tension n'excédant pas 10 % de la tension de sortie.

Dans une dernière étape de la thèse, nous avons investigué les matériaux piézoélectriques dédiés aux convertisseurs de puissance basés sur des résonateurs piézoélectriques. L'étude visait l'augmentation de la fréquence en utilisant du Niobate de Lithium (LNO) afin de : -réduire les modes parasites perturbant le bon fonctionnement du résonateur, -atteindre un facteur qualité et un fort couplage électromécanique, -améliorer le montage mécanique et la connexion électrique avec le circuit électronique. Par la suite, nous avons fabriqué un PR à base de LNO en salle blanche, avec un circuit dédié pour une fréquence de fonctionnement allant jusqu'à 7 MHz. Le circuit proposé a pu être validé sur une plage de puissance de 2 - 32 W avec une tension d'entrée de 60 V et une tension de sortie de 20 V. Cette partie est présentée dans l'APPENDIX A.

Nous terminons ce manuscrit en présentant nos perspective et les principaux défis qui peuvent être étudiés, ainsi que les opportunités potentielles de la conversion d'énergie basée sur les résonateurs piézoélectriques.

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## List of symbols

С	Motional capacitance in the electrical equivalent circuit.
$C_P$	Static capacitance in the equivalent circuit.
D	Diameter.
<i>d</i> <sub>33</sub>	Piezoelectric coefficient where the polarization face the electrodes
$f_{ar}$	The ani resonant frequency in the equivalent circuit.
fr	The resonant frequency in the equivalent circuit.
G	The conversion gain between the input and the output voltage.
Ι	The amplitude of the current in the motional branch in the equivalent circuit.
Iout	The average value of the output current.
i	The current of the equivalent circuit.
<b>i</b> <sub>in</sub>	The input current.
iout	The input current
$i_P$	The current out of the resonator.
k	Electromechanical coupling factor.
<i>k</i> 31	Electromechanical coupling factor, where the polarization is normal to the electrode.
<i>k</i> 33	<i>Electromechanical coupling factor, where the polarization is orthogonal to the electrode.</i>
L	Dynamic inductance in the equivalent circuit.
$N_P$	Constant frequency for a disk in radial mode vibration.
$N_t$	Constant frequency for a disk in thickness mode vibration.
m	Mass of the material in kg.
$\vec{P}$	Polarization vector.
Pout	The mean output power.
PR	Piezoelectric Resonator.
PT	Piezoelectric Transformer.
Q	The quality factor.
$R_P$	The motional resistance illustrating the dumping losses.
th	Thickness of the material.
VC	Variable capacitance.
Vin	The input voltage of an electrical source.
Vout	The output voltage.
$V_P$	The voltage across the piezoelectric resonator.

- *Y<sup>D</sup> Elastic modulus at constant displacement.*
- *Y<sup>E</sup>* Elastic modulus at constant electric field.
- $\rho$  Density of the material kg/m<sup>3</sup>.
- $\varepsilon_0$  Electric constant.
- $\varepsilon_{33}^{s}$  Permittivity at constant strain where the polarization is longitudinal to the electrode.
- $\omega$  Radial frequency rad/s.

## Chapter I: Introduction

*Abstract*: This chapter is the introduction of this dissertation, where the scope and the objectives of this thesis are presented.

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### I.1 Scope

The scope of this dissertation is to expose the research that has been conducted during this PhD project. This project was carried out at CEA-Leti (Carnot's Institutes) and SATIE laboratory, and supported by French *Agence Nationale de la Recherche* (ANR) and via Carnot Funding. This research has been mostly published as journal/conference papers and patents, [APPENDIX B].

### I.2 Background and motivations

Nowadays, all electronics need to be powered by grid-connected supplies or batteries. These electronic devices operate at various voltage amplitude, frequency and power. Therefore, power converters are required to change the power source's waveform and to adapt it to the electronic devices need, as illustrated in **Figure 1.1**. Thus, these converters become unavoidable in our daily life. Certainly, the demand of power converters is constantly growing, which is providing a serious economic challenge. Indeed, according to the report of Market Sand Markets in Global Power Converters in 2022, the market of only dc-dc converters is estimated to grow by USD 7.7 billion between 2021 and 2026 all over the world [1]. This growth is due to the increase of the power consumption in industrial automation (industry 4.0), telecommunication, aerospace industry, electric vehicle ...etc., and the constant demand in cleaner energy as renewable energy.



Figure I.1. Power converter Schematic.

Among the large family of power converters, we can classify two categories: the direct transfer converters and the indirect ones. The basic operating of these lasts, which are considered in this

work, consists of taking electrical energy from the source and to store it temporally in a passive component. Then, this stored energy is transferred to the load. The electrical energy can be stored in electromagnetic, electrostatic or mechanical energy form. As the source and the load can be found in different forms (AC current, DC current), designing power converter is a serious process. Indeed, the design process consists of well selecting the topology of the converter, the semiconductors and the passive components..., as illustrated by **Figure 1.2**. Moreover, that should fit the requirement in terms of power, efficiency, size reduction and cost. Considering that, the design process becomes complex and tough as it depends on multiple parameters, as illustrated in **Figure 1.2**. Therefore, the major challenge of the design is to provide a compact converter that ensures high efficiency (i.e., low heat sink) and load constraints (i.e., power, voltage, frequency).



Figure I.2. Power converter: design requirements.

Commercially, the most used power converters are based on electromagnetic energy conversion. These converters use inductors or transformers in order to operate as step-up or step-down converters, or as isolated converters. They can operate with high efficiency and high power. However, the magnetic components have parasitic effects increasing losses like copper losses, hysteresis and Eddy Current losses in magnetics, limiting the operating frequency and the energy stored by cycle due to materials and provide poor efficiency with size reduction [2]-[5]. Also, inductors radiate since the electromagnetic field is not completely enclosed in the material. Therefore, miniaturization of the converter becomes limited by the magnetic components, as they take a significant part of the volume of the converter and their performances decline with size reduction [5]. Some researchers have investigated on size reduction of magnetic components by increasing the switching frequency and/or on using improved magnetic materials [2], [5], but the power density of magnetic components based converters remains limited by their materials' fundamental physical limits [5].

The capacitors used as energy storage in power electronics can easily be integrated into monolithic structures, which can be assembled in parallel or series from small cells to fit the requirements in terms of power and voltage [6], [7]. Moreover, the switched capacitance converters (SCCs) can achieve high-power density for low-power applications (less than 1W), which could be 100–1000 times greater than magnetic converters [6]. However, their efficiency drops significantly for variable gain. Furthermore, it needs to operate at variable switching frequency for maintaining high efficiency with load variations (i.e., variable output power) [7].

Piezoelectric transformers (PTs) were used to replace the magnetic transformers of high step-up power converters and low power, especially for cold cathode fluorescent back light (CCFL) to overcome the drawbacks of the magnetic solutions, [8]-[13]. PTs-based power converters are compact and low profile suited for integration in thin devices like cell phone. However, their efficiency, without additional inductor in order to achieve ZVS operation, is quite poor, or it needs a specific condition for ZVS operation [14]-[15]. Ultimately, the market of the backlight was widely replaced by led lightning. Thus, the commercial breakthrough has still to show up with the current market demand. Hence, the investigation on alternative mechanism of conversion should be conducted to offer new perspectives in power electronics. Therefore, this dissertation deals with indirect power conversion based on piezoelectric resonators, since these materials can achieve high power density and efficiency compared to magnetic and electrostatic devices [16]. Indeed, the advantage of the piezoelectric components are listed below:

- Reducing EMI problems:
  - o no magnetic field generation by the storage element as long as it is mechanical.

- o it is immune to electromagnetic interference EMI.
- Soft switching operation avoiding fast electric field variations.
- High quality factor (low losses): potential high efficiency.
- High mechanical energy storage capability: potential of high power density conversion.
- Low cost, thanks to the simple build-up and manufacturing.
- Low profile and planar shape.
- Integration on silicon with controlled process such as quartz oscillator.
- Inherent electrical insulation.
- Possibility to achieve complex geometries such as Tubes, disks, plates, focal bowls...

As reveled by the title, our main objective is to develop an uninsulated power converter for AC to DC voltage conversion and low power applications (between 10 to100 W) by using piezoelectric components in order to miniaturize the power supply. The structure of AC to DC converter can be composed of multiple conversion stages (i.e., rectifier stage, isolated dc-dc, PFC, etc....) which depends on the power level, voltage, insulation requirement, etc....[17]. Still, most of AC-DC converters contains a regulated DC-DC power stage in order to deliver the energy at a constant voltage level to the output load. In domestic and housing applications, this DC-DC stage is a high-to-low voltage converter; hence, we focus on a high ratio DC-DC power converter in this dissertation. This converter will use a piezoelectric resonator as the main transient energy storage.

### I.3 Thesis objectives

The main objective of this thesis is to investigate a new mechanism of power conversion that uses an alternative to the conventional magnetic power storage. The conversion mechanism that we focus on is based on mechanical energy storage. Indeed, the piezoelectric properties enable to store electrical energy as mechanical one through the reverse effect of the piezoelectricity, and to restitute this energy as electrical form thanks to the direct effect. Therefore, the objectives of thesis can be summarized by:

- Identifying the topology of the piezo DC-DC converter and the related conversion cycle.
- Providing an analytical model.
- Developing an actual prototype for experimental verification.
- Providing and developing a control strategy for regulating the output voltage.

• Implanting the control strategy.

#### I.4 Thesis structure and content

This dissertation is structured as follow:

#### Chapter II:

In this chapter, we present an overview of the state of the art of the piezoelectricity and power converters based on piezoelectric components. The recent progress are also presented.

### **Chapter III:**

This chapter presents the power conversion using a piezoelectric resonator as storage element. A generic representation of the power conversion is established, and a relative generic model is provided. We also present the most relevant topologies and conversion cycles. A comparison between the conversion cycles are made considering step-down converters. Therefore, we identify the relevant converter topology and cycle that we will use for our applications.

### Chapter IV:

In this chapter, we propose a design and gives the constraints of our converter. Then, we present our experimental setup. Afterward, experimental results are exhibited over various operating points. The influence of the voltage, frequency and power are stated.

#### Chapter V:

This chapter shows a generic control strategy of conversion cycle based on piezoelectric resonator. Therefore, this strategy is applied on our topology. Simulation under MATLAB-Simulink is carried out, which validates the operation of the developed control strategy. An experimental prototype is built in order to validate the control. Therefore, we present the experimental results to fulfil the validation process.

#### Chapter VI:

This chapter concludes our work and present the major challenges and perspectives of piezobased power converters.

## Chapter II: Overview and State of Art

**Abstract**: This chapter gives the state of the art and overview of the piezo-based power converters. Also, this chapter illustrates the recent improvements and progress of such converters, and the major challenges that we should deal with.

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### II.1 Introduction

The goal of this chapter is to give the state of art of the piezoelectricity through its history and applications with a particular attention on the power conversion using piezoelectric components, in which we explain the mechanism of the conversion through an example of implementation. In addition, a synthesis of the main papers in the literature dealing with our topic are cited and classified by subjects.

### II.2 The piezoelectricity: history and applications

In 1880, the French physicists Curie Brothers discover the piezoelectricity [18]. The piezoelectricity consists of generating electricity from a pressure. Therefore, the piezoelectricity is the interaction between the mechanical and electrical states in the piezoelectric material providing thus an electromechanical coupling. Resulting from that, two effects of the piezoelectricity are defined:

<u>The direct effect:</u> it is the result of a displacement of electrical charge when a mechanical force is applied.

<u>The reverse effect:</u> Lippman in 1881 demonstrated the reverse effect. The reverse effect is the result of a mechanical strain when an electrical field is applied. In literature, the mechanical strain is very small, for instance: the lead zirconate titane (PZT) material provides a mechanical strain around 0.1 %. The low mechanical strain can be very useful for achieving



Figure II.1. (a) Direct effect, (b) Reverse effect of piezoelectricity.

a precise positioning (for example: microscopy) or for providing large forces (for example: inkjet printing or fuel injectors).

The first use of the piezoelectric materials were in sonar systems in submarines during the 1920s, which consists of using these materials as transducers. Then, the use of piezoelectric devices has been diversified in various applications such as actuation, sensing, filtering (Bulk or Surface Acoustic Wave filter (B/SAW)), energy harvesting applications. Piezoelectric devices are widely used in industry, medical equipment, military and telecommunication. By the increase in the use of piezoelectric devices, their performances and the fabrication process have been widely developed and improved like PZT ceramics.



Figure II.2. Field of application of the piezoelectric devices.

The usage of the piezoelectric materials in power converters comes in the late of 1950s, when C. Rosen has invented the first piezoelectric transformer (PT) (*called the Rosen-type after the inventor*) [19], and then PT-based power converter [20]. Therefore, with the progress in the piezoelectric material, many researches have been conducted in this domain. To replace the magnetics based converters, the piezoelectric based converters were a commercial achievement but only for high step-up voltage conversion and low power (< 5 W) applications. Indeed, the usage of PT-based converters to supply LCD display with CCFL back-light has succeeded. However, the Back-lighting was rapidly replaced by Led lighting which is supplied with low voltage. Even if the PT-based converters, a major challenge remains in developing them for high-to-low voltage or low-voltage conversion and power up to 100 W, in order to meet the growing demand in the switched-mode power supply (SMPS) and low-voltage converters.

In the last decade, the piezoelectric resonators (PRs) were firstly used in switched capacitor converters as replacement for the capacitors [21]-[23], the PRs can provide a higher quality factor and also get benefit from the natural inductive behavior in order the converter to operate with ZVS conditions. However, the voltage gain remains to be fixed to 2 (in step-up conversion), which requires using cascade converters for having another conversion gain. In addition, these converters inherit the same drawbacks as the switched capacitor converters in terms of voltage regulation and low efficiency with load variation [6]-[7]. With the recent developments in PR-based converters [24], a new potential field has emerged that consists of using a single PR as storage component in power converters without requiring transformer or additional inductors in the conversion systems. Moreover, it enables employing the PR component in step-up and step-down topologies. Subsequently, several research studies have emerged [25]-[29] that investigate on power converters based on PR. They exhibit the performances of the PR-based converters in several use cases. Until now, we have identified three major research teams on using PRs in power electronics: CEA-Leti, MIT and Sandford University.

### II.3 Piezo-based power converters

#### II.3.1 Mechanical Energy Conversion

The first use of the mechanical energy in order to store transiently the electric energy as replacement for the magnetic was made by J. M. Noworolski et S. R. Sanders [30]. Basically, J. M. Noworolski was motivated by the fact that twice energy can be stored in the Silicon as

mechanical energy compared to magnetic energy in the same volume. In their research, they have used a variable capacitance (VC) to transfer electric energy to a mechanical form. The operating principle of their converter consists in using multiple cycles of pumping energy from the input source to the mechanical resonator at the resonance frequency of the VC, then, once the energy stored in the VC reaches the desired value, a boosting cycle is applied to transfer the energy stored to the load. Even if the integration of the converter was achieved, its efficiency was low, because during the pumping stage (i.e., the pumping stage consists of charging and discharging the capacitance to increase the displacement of the free electrode), hard switching was applied to discharge the capacitance when the energy of the capacitance is at its maximum value. This leads to high power losses. In addition, the converter is limited only to boost conversion.

In 2017, **G. Despesse and B. Pollet** have submitted the first patent on power converter based on piezoelectric resonator that describes a new mechanism of energy conversion [31]. The power converter based on piezoelectric resonator (PR) was firstly inspired from the research made by S. **Ghandour, G. Despesse and S. Basrour** during their research work in integration of power converters as MEMS using a VC [32]. The initially developed power converter is based on using a variable capacitance where by construction one electrode is recessed and the other one is on free movement. That can be modeled by a motion of mass on spring system, as shown in **Figure II.3**.



Figure II.3. (a) Mechanical structure of the VC, (b) Resonant electrostatic model of the VC [32].

The VC-based converter topology shown in Figure II.4 operates as an electro-mechanical transducer during the resonant regime, enabling by that to get benefits from the quality factor of the VC. Indeed, during a period of resonance, the VC is connected successively to {V<sub>e</sub>, V<sub>e</sub>+V<sub>s</sub>, V<sub>s</sub>} to exchange charge between the input source and/or the output voltage. Also, between each voltage level, the VC is disconnected in order to change the voltage across the VC following the equation:  $Q = V * C_{var} = V * \varepsilon_0 * Area/th$  (the thickness (*th*) is variable as one of the electrodes of the VC is on free movement, as shown in Figure II.3. This enables to close-on the switches with ZVS operation. The presented converter in [32] illustrates an efficiency up to 80 % in simulation for a step-up converter from 10 V to 20 V with a power of the order of mW for a VC having an area of 1 cm<sup>2</sup>.



Figure II.4. The topology of the converter based on VC [32].

The advantage of such a converter is that the fabrication process of the VC is compatible with the current process in silicon industry enabling to integrate the power converters, even though some difficulties had been noted for the fabrication of the free electrode requiring some developments. However, the VC should be permanently polarized, and if the zero voltage crossing is occurred, the VC should be re-polarized which provides a major issue. Also, the power density (W/cm<sup>2</sup>) shown of this converter remains low, less than 10 mW/cm<sup>2</sup> (considering only the area of VC).

Therefore, to overcome these limitations, B. Pollet *&.al.* [31] have started the investigation on the use of the piezoelectric components instead of the electrostatic devices. In both cases, energy is stored in a mechanical form, but in the piezoelectric case, the energy transfer between

electrical and mechanical domains is done by using the piezoelectric properties and not any more by using electrostatic actuation/regeneration. This enables a significant increase in power level that can be exchanged between the mechanical and electrical domain at each cycle thanks to high electromechanical coupling factor of the recent piezoelectric materials ( $k^2 > 0.3$ ). Furthermore, the storage and transduction mechanism are merged, removing the need of adding air-gap, electrodes, and guidance/spring. Finally, the power density is significantly increased, about a factor 1000 (Watt range scale obtained for piezoelectric materials compared to mW range per centimeter scale for the VC).

In addition, the piezoelectric materials are extensively developed as MEMS components in actuator or in sensing applications[33]-[35], which make them suitable for integration and miniaturization.

### II.3.2 Example of implementation of PR-based DC-DC converter

Figure II.5 shows the topology of the DC-DC converter that has been used for validation in [36]. The circuit is composed of three switches  $\{k_{in}, k_{out}, k_3\}$  and a PR that has been modeled for its motional part by a sinusoidal current source (assumed near the resonant frequency) in parallel with the intrinsic capacitance of C<sub>P</sub>. This circuit enables connecting the PR with the input source V<sub>in</sub>, the output load V<sub>out</sub> and Zero voltage (short-circuit).



Figure II.5. Topology of a dc-dc converter using PR as storage component.

During operation near the resonant frequency, the PR is successively connected to  $V_{in}$ , 0V,  $V_{out}$  during stages 1, 3 and 5 respectively, as shown in Figure II.6. Connecting the PR to the
sources enables to transfer energy from the electrical source to the mechanical resonator, while when the PR is connected to load (stage 5) the PR transfers the stored energy to the load in electrical form. The short-circuit is performed in stage 3 to balance the charge between the stored and transferred one. For ZVS operating, the PR is disconnected between each constant voltage stage (stage 2, 4 and 6) in order to let charging/discharging  $C_P$ , thus changing the voltage V<sub>p</sub> across the PR (as shown in Figure II.6). The energy and charge balances can be written by (the values are algebraic):

$$\begin{cases} Energy: V_{in}Q_{in} + 0VQ_3 + Q_{out}V_{out} = 0\\ Charge: Q_{in} + Q_3 + Q_{out} = 0 \end{cases}$$
(II.3.1)

Where,  $Q_{in}$  is the charge taken from the input source, while  $Q_{out}$  is the charge transferred to the load.  $Q_3$  is the charge evacuated during the stage 3 (short-circuit), used for balancing the total charge of the PR while energy exchanged during stages 1 and 5 are balanced.

Therefore, the conversion gain can be deduced by (II.3.2). As stated in (II.3.2), the conversion gain is just the ratio between the charge stored in the PR and the one transferred to load.

$$\frac{V_{out}}{V_{in}} = \frac{Q_{in}}{|Q_{out}|} = 1 - \frac{Q_3}{|Q_{out}|} \le 1$$
(II.3.2)



Figure II.6. Waveforms of the step-down conversion cycle 20-10 V [36].

This operating principle enables to operate with energy balance, making as consequence a sustainable oscillation. The charge balance clamps the amplitude of the voltage across  $V_{P.}$  Therefore, the losses are mainly depending on the quality factor of the materials (damping effect) that may be low as the PR may achieve a high quality factor (> 1000 for PZT), and also on conduction losses of the switches (no switching losses). Assuming this operation, the converter may achieve a high efficiency and a high power density, as demonstrated in [36]. Thus, this operation can be extended in numerous conversion cycles and topologies, depending on the power conversion requirements and implementation.

# II.4 Piezo-based power converters: projects and applications

In this part, we have identified the recent scientific articles or patents on the development of power converters based PR that give an overview of the state of the art illustrating the various topics and application targets. Therefore, through the recent research projects, we can summarized the 3 main research related topics as follow:

## II.4.1 Topology of power converters based on PR

The integration of the PR as a storage component in DC-DC converter leads to question about the best topology, the conversion cycle, the number of switches...etc., based on how the PR is used. In [24]-[28], the authors enumerate the main topologies for step-up, step-down, high step-down/high step down converters. Also, isolated PRs-based converters have been developed in [36].

In [36], the DC-DC converter presented operates as step-up ( $0 < V_{out} < V_{in}$ ) or step-down ( $0 < V_{in} < V_{out}$ ) conversion. In this topology (Figure II.5), the PR stores the energy taken from the input source, and then transfers it to the output load. Figure II.7 shows the prototype that has been used for experimental verification of power conversion based on PR. Also, it has been the first prototype used for experimental verification. This prototype exhibits a high efficiency (>90 %) for an input voltage 10 V, an output voltage range 15-30 V, and an output power up to 1.5 W. This topology operates a wide voltage range conversion, but all the energy transferred to the load is stored in the PR, which increases the constraints on the PR.



Figure II.7. Picture of circuit, [36].



Figure II.8. Efficiency Vs Output Power, for Vin=10 V, and Vout=15, 20, 25, 30 V, [36].

The authors of [27] presented a step-down dc-dc converter based on a PR. This topology is composed of four switches. The switching sequence of the proposed converter uses  $\{V_{in}-V_{out}, 0V, V_{out}\}$ , therefore, a part of the energy is transferred directly to the load during the stage  $V_{in}-V_{out}$ , while a second part is stored in the PR and then transferred during the stage  $V_{out}$ .

It enables to reduce the energy stored in the PR, and then, it enables to reduce the size of the PR. However, the voltage conversion ratio is limited to  $(V_{in}/2 < V_{out} < V_{in})$ .



(b)



Figure II.9. (a) Converter topology, (b) picture of the prototype, [27].

**Figure II.10** shows the efficiency of this converter as a function of the output power, for an output voltage of 40 V and a conversion ratio up to 0.47. In this figure, the measured efficiency is higher than 90 % for power level up to 10 W. As exhibited, a peak efficiency of 98 % is reached at 2 W for a conversion gain of 0.47.

All these results give encouragement for developing PR based dc-dc converters, which motivates our researches in exploring the numerous topologies and conversion cycles that get the best advantage of the PR.



Figure II.10. Efficiency Vs Output power, for Vout=40 V and Vout/Vin=0.2 to 0.47 [27].

# II.4.2 Close-loop Control

The control of a such dc-dc converters that employs PR reveals to be more complex than the classical solutions in magnetics based converters. Indeed, the control should take into consideration the conversion cycle, variable frequency, soft switching/charging and load regulation. In [25], authors have developed a control strategy that takes into consideration the previous issues for a step-up converter with low voltage conversion 10-20 V and power of 0.5 W for the switching sequence  $\{V_{in}, 0, V_{out}\}$ .



Figure II.11. Structure of control step-up converter based on PR for 10-20 V, [36].

Also, during my PhD, the MIT [37] has implemented a control law in a microcontroller for a step-down converter for a voltage conversion 30 -10 V and a power of < 1 W, the control shows good performances in terms of transient response and load regulation (response time is about 14.8 ms to reach 2 % of the output voltage set point). In [38], we have developed and implemented a first control law for such a conversion mechanism. It has been used for high-to-low voltage converter for a 120 V input voltage and an output voltage of < 48 V and power up to 16 W. This control strategy shows a response time for load regulation less than 2 ms, it can be used for any switching sequence, and will be detailed chapter V.

Also, it reveals that spurious modes can show-up at high frequency operation which limits the operating power range (i.e., variable frequency), [25]-[29]. Therefore, fixed frequency control can be used by using burst mode as proposed by Stanford University [39]. It consists of using power conversion cycles to transfer the energy to load followed by Zero Voltage cycles to cut-off the power transfer. The ratio between the number of conversion cycles and zero voltage cycles gives the mean power. Since, the PR can achieve a high quality factor (i.e., the operating frequency is near the resonance), the losses in the PR remains lower compared to magnetic converters. Nevertheless, the efficiency is lower than the optimal control developed in [25], [37]-[38]. In addition, frequency should be, in any cases, regulated as the resonant frequency of the material depends on the temperature.

## II.4.3 Piezoelectric materials

Piezoelectric components are anisotropic materials such as ceramics produced by powder metallurgy process (PZT), and crystals (Lithium Niobate) fabricated by crystal growth process. Therefore, their performances are highly depending on their physical properties (i.e., strain, Elastic and dielectric constants), the shape, the mutual orientation of driving electric field and acoustic wave propagation direction [40]. All these considerations should be taken into account for choosing the best material enabling high power density and high efficiency. In harvesting applications, the figure of merit (FOM) is given by the product of the quality factor Q (inverse of loss rate), and the electromechanical coupling factor  $k^2$  (see its definition in (II.4.1)). This same FOM is also applicable for PR based power converters to maximize the efficiency (cf. Pollet's thesis [36]). It is a simple approach for classifying the piezoelectric materials in terms of efficiency.

$$k^{2} = \frac{Electrical \ energy \ converted \ to \ mechnical \ form}{input \ Electrical \ energy}$$
(II.4.1)

In Figure II.12 [41], we have plotted the efficiency as a function of the product  $Qk^2$  for the conversion cycle presented in [26], considering hard PZT and Lithium Niobate from several manufacturers. This figure illustrates disparities of the materials, and show the efficiency that may be achieved. However, this FOM is not sufficient, as it does not give an indication on the material that can achieve the highest power density. In [42], a FOM (FOM<sub>ADP</sub>) based on calculation of the power density (W/cm<sup>2</sup>) is proposed. The main PZT materials are then placed on a 2D graph showing the area power density as a function of loss ratio (i.e.,  $k^2Q$ ), giving the



Figure II.12.Efficiency Vs  $k^2Q$  (thickness mode vibration), [41], APPENDIX A.

physical limits of the materials, as illustrated in Figure II.13. But overall, all these FOMs give only indications for choosing the best material. To determine the power density limit, it lacks of data verified and the measurement setups or technics to determine the properties of the materials are not specified and/or normalized for all the manufacturers.

The paper [29] and our paper [41] introduced the use of LNO materials for power converters, with a specific focus on the sizing of the piezoelectric resonator. These articles show the impact of the geometry, size and mounting on the performances of the resonator and the spurious modes disturbances. They well illustrate the influence of the geometry, the dimensions and the mechanical mounting on the reduction of the spurious modes through experimental results and actual prototypes.



Figure II.13. Hard PZT materials comparison: FOM<sub>APD</sub> (Areal Power Density) Vs FOM<sub>M</sub> (*loss ratio* P<sub>out</sub>/P<sub>loss</sub>), [42].

# II.5 State of the art synthesis

We have summarized the relevant references in **TABLE II.1**, and sorted by subject and by research team. Some references deal with multiple subjects, so, they are cited in multiple cases. The references in red color are prior to this thesis work, while all other researches appeared simultaneously to this work.

From this table we can deduce the effort that was invested by each team. For the Stanford team, they were the first to use the LNO in dc-dc converter based on PR in order to operate at high frequency. Also, to deal spurious modes, burst modulation was implemented in open loop. In addition, they have put their interest in very high frequency converters by using the LNO-resonator as filter for cancelation of the second harmonic in  $\Phi 2$  inverter and output filter for the class E structure.

For the MIT team, they were the second team working on piezo-based converter after CEA-Leti. They started by exploring the converters based on PR, then, they have extended the conversion principle to PT-based converters, for high voltage and low power applications. In addition, they have put their interest for establishing figures of merit for selecting the PZT- materials that can provide a high efficiency and a high power density. Also, design and optimization of piezo components are subject of their work.

As illustrated in the table, in CEA-leti, we have put our interest on exploring the possibilities of the piezo-based converters. Numerous patents and papers have been submitted/accepted dealing with DC-DC converters based on PRs for isolated and non-isolated structures before and during this thesis. Also, developing control strategy is investigated with the scope of developing actual porotypes for validation. In addition, we investigate on design and fabrication of piezoelectric resonators through internal collaboration with the different departments. To sum up, several subjects are aimed to investigate on the opportunities of piezoelectric in power conversion.

TABLE II.1.Relevant references arranged by subjects and research teams									
	Subject	MIT	Stanford						
	PR-based converters: Non- Isolated	[ <b>24], [25]</b> , [26], [28], [ <b>31</b> ]	[27]						
Topology	PRs-based converters: Isolated	[ <b>31</b> ], [Patent 3- [Patent 6]							
	PT-based converters		[43]						
Control Methods	Variable frequency control (optimal control)	[36], [38], [Patent 2]	[37]						
	Fixed frequency control: reactive energy	[Patent 2]							
	Burst modulation	[Patent 2]		[39]					
Materials	Design and fabrication	[41]	[48]	[29]					
	Materials and limits	[41]	[42]	[29]					
	"Augmented Piezo"	[Patent 2]	[48]						
VHF-filter	Φ2 inverter: L-Piezo Class (suppression of the second harmonic)	[45], [49]		[46]					
	Output Filter : Class E			[47]					

#### II.6 Conclusion

So far, energy conversion based on using mechanical storage components such as piezoelectric resonators remains new and poorly studied at the beginning of this thesis project. Up to now, few cases are explored and investigated, while numerous variants of power converters based on piezoelectric resonators are still to be investigated and developed for a better use of the piezoelectric materials.

In this thesis project, we aim to develop a power converter that uses a piezoelectric resonator as a storage component for high-to-low voltage conversion and low power applications, while minimizing the energy stored in the material, which allows the miniaturization of the power converter. In addition, the conversion mechanism is not well developed and clarified in the literature, thus, during the thesis we have made efforts to properly detail the operating principle and provide a generic model to build a conversion cycle based on six switching stages.

The control of such a converter is not yet addressed in the scientific literature. Conventional control is not sufficient for a PR-based converter, as it requires frequency control, soft charging, soft switching, and load regulation at the same time while keeping the control synchronized with the motion of the PR, for high efficiency operation. Furthermore, there are no papers (to our knowledge) demonstrating the feasible implementation of control law on a PR-based converter prior to this thesis [24]. Therefore, during this thesis project, we aim to develop a control strategy and design a control circuit for a step-down DC-DC converter for high-to-low voltage conversion. The implementation will be developed with a real control circuit for the experimental proof.

In addition, we have conducted research on increasing the operating frequency using alternative materials such as Lithium Niobate which was not explored at the beginning of the thesis. This material can provide a high quality factor and a high electromechanical coupling factor, and have low permittivity, which makes it suitable for high frequency operation. Therefore, we have provided a design on LNO-based PR for high frequency operation with achieving high quality and coupling factors. Moreover, the proposed design takes into consideration the reduction of the spurious modes' disruption.

# Chapter III: Piezoelectric resonator based power converter

**Abstract**: In this chapter, we start by presenting the operating principle of piezo-based dcdc converters. Then, we propose a generic analytical model for steady-state operation. Also, we enumerate the conversion cycles and the topologies. Furthermore, a simulation is presented to verify the operating principle. Finally, we propose a method to compare the conversion cycles. We conclude the chapter with a discussion and analysis.

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#### III.1 Introduction

The piezoelectric resonator (PR) in power conversion operates by using the both piezoelectricity effects. Over a single conversion period, the PR works as a piezoelectric actuator to store the electrical energy in mechanical form, and as a piezoelectric transducer to transfer the mechanical energy in electrical energy to supply the load. A PR is composed of a piezoelectric ceramic plate or crystal with two electrodes on each side; it can operate in thickness vibration mode or longitudinal vibration mode.

To replace the inductive behavior of inductor in power converter, the PR operates in the inductive region of its impedance (i.e., between the resonant and anti-resonant frequencies). Compare to a L-C resonator (Q < 50), PR benefits of a high quality factor of the ceramic, such as PZT (Q > 1000). However, due to the physical behavior of the PR and the need for operating near the resonance frequency, the conversion mechanism and the approach should be adapted to the PR based DC-DC energy converter. This chapter first presents the equivalent circuit model of PR, the main operating principle and the conversion cycle of piezo-based power conversion. Then, the conversion cycle is derived for any switching sequences. Therefore, this chapter presents an analytical model based on energy approach by taking as example a switching sequence adapted for high-to-low voltage applications. The electrical waveforms and the power conversion efficiency are performed by simulation in order to illustrate and to assess the operating principle.

# **III.2** Operating Principle

#### III.2.1 Equivalent circuit model of PR

Piezo-materials behave like dielectrics but also like active materials able to convert electrical energy into mechanical energy and vice-versa. Therefore, an equivalent circuit can represent both effects. The two electrodes, in relation with the dielectric property of the plate acts as a natural capacitance (or called blocked capacitance) named  $C_P$  while an *L*-*C*-*R*<sub>P</sub> series electrical circuit models the electro-mechanical property of the PR close to the resonance. Figure III.2.a shows the equivalent circuit based on Butterworth-Van Dyke (BVD) model.



Figure III.1. PR's: (a) electrical model based on Butterworth-Van Dyke (BVD) model [50], (b) impedance plot.

L represents the mass of the PR; C the compliance and  $R_P$  the resistance that models the mechanical losses. TABLE III.1 illustrates the electrical model with the related mechanical model. Therefore, L-C circuit part models the mechanical storage behavior.

TABLE III.1. Electrical circuit and the corresponding mechanical circuit.									
Electrical system	Voltage	Current	Charge Electrical resistance Inductance Ca						
	V	Ι	q	$R_P$	L	С			
Mechanical system	Force	Velocity	Displacement	Mechanical resistance	Mass	Compliance			
	F	v	и	r	т	S			

The Figure II.1b shows the impedance of the PR between the resonant frequency  $f_r$  (L-C) (and the anti-resonant frequency  $f_{ar}$  (L-(C//C<sub>P</sub>))

Once the PR is placed in the converter, we define two operating configurations: one where the PR is connected to a constant voltage source/load named **connected stage** and a second configuration where the PR is placed in open-circuit (isolated) named **open-circuit stage**. **Figure III.2** shows these both configurations of the PR, where:

(a) <u>Connected stage</u>: during this stage, the piezo can take electric charge from the input voltage (source) or/and transfer charges to the output voltage (load). In addition, a short-circuit (*Zero voltage*) can be applied to balance charges over a period. Therefore, for connected stage operation, the PR is considered as an AC current source.

(b) <u>Open-circuit stage</u>: this stage allows charging or discharging the capacitance  $C_P$  (depending on the sign of current *i* in the *L*-*C*-*R*) as shown in Figure III.2b, which makes

change the voltage across the PR ( $V_P$ ) and the voltage across the switches. Equation (III.2.1) gives the evolution of the voltage  $V_P$  during this stage, as a function of the current *i*. During this stage, the PR behaves like an AC voltage source.



Figure III.2. PR's electrical connections: (a) Connected stage, (b) open-circuit stage.

$$V_P(t) = -\frac{1}{C_P} \int i(t) dt \qquad (\text{III.2.1})$$

Yet, the PR operates between the resonant and the anti-resonant frequency, the current i in *L*-*C* branch can be approximated by a sinusoidal AC current source thanks to the high quality factor of the ceramics like PZT, then the current i is given by:

$$i(t) = I \cdot \sin \omega t \tag{III.2.2}$$

Where, *I* is the amplitude of current *i* in *LCR* branch, and  $\omega = 2\pi f$  is the pulsation and *f* the operating frequency.

## **III.2.2** Operational principle

As in a conventional energy converter, the energy is taken from the input source, stored temporarily in a passive component before being transferred to the load, with changing the type of the energy. Therefore, by using a PR as a storage element, it should at least being connected to two voltage levels named  $V_a$  and  $V_b$ ; where  $V_a$  and  $V_b$  can be the input or the output voltages or composed of input and output voltages combinations. In addition, open-circuit is used to let the voltage level of  $V_P$  evolves ( $V_a \rightarrow V_b$  or  $V_b \rightarrow V_a$ ) in order to turn-on switches in ZVS mode. By ensuring the energy balance, the amplitude of *i* is constant, leading to a sustained oscillation. With charge balance, the voltage  $V_P$  is capped between a minimum and maximum value throughout of a period of conversion. Equations (III.2.3) and (III.2.4) give the energy and

charge balance over a single period of conversion, where  $Q_a$  and  $Q_b$  are the charges exchanged under  $V_a$  and  $V_b$  respectively and taken as algebraic values. To sum up, the operating principle is based on:

- Energy balance.
- Charge balance.
- Zero voltage Switching thanks to soft-charging.

$$Q_a = Q_b \tag{III.2.3}$$

$$V_a Q_a = V_b Q_b \tag{III.2.4}$$

Considering (III.2.3) and (III.2.4), it induces to  $V_a = V_b$ . In this case, the possible values for the voltages couples {V<sub>a</sub>, V<sub>b</sub>} are limited to:

- $\{V_{in}-V_{out}, V_{out}\}$  : where  $V_{in}=2V_{out}$ .
- $\{V_{in}, V_{out}-V_{in}\}$ : where  $V_{in}=\frac{1}{2}V_{out}$ .
- $\{V_{in}-V_{out}, 0\}$ : where  $V_{in}=V_{out}$ .
- $\{V_{in}, V_{out}\}$ : where  $V_{in}=V_{out}$ .

Therefore, a third connected stage named  $V_c$  is required to operate with a variable voltage conversion gain. This stage allows balancing the PR's charge and energy independently. So, we can construct a conversion cycle where we define the voltages { $V_a$ ,  $V_b$ ,  $V_c$ } as follow:

- Each voltage level is defined during only a single polarity of the current *i* which means that no reactive energy is exchanged with the PR.
- The constant voltage stages V<sub>a</sub> and V<sub>b</sub> are defined to occur on opposite polarities of the current *i*.
- The voltage level  $V_c$  is defined after  $V_a$  occur and at the same current *i* polarity as  $V_a$ , as shown in Figure III.3. It results thus that  $Q_a$  and  $Q_c$  have the same polarity.

Then, the energy and charge balance become:

$$Q_a + Q_b + Q_c = 0 \tag{III.2.5}$$

$$V_a Q_a + V_b Q_b + Q_c V_c = 0 \tag{III.2.6}$$

We can remove  $Q_b$  in (III.2.6) by using (III.2.5), the energy balance can be re-written by:

$$(V_a - V_b)Q_a = (V_b - V_c)Q_c$$
 (III.2.7)

The equation (III.2.7) states that if  $V_a > V_b$  then  $V_b > V_c$ , and if  $V_a < V_b$  then  $V_b < V_c$ , because  $Q_a$  and  $Q_c$  have the same polarity by definition. In case of  $V_a > V_b$ , we obtain the following classification:  $V_c < V_b < V_a$ . Since  $V_a > V_c$ , the current *i* should be positive in the half period where  $V_a$  and  $V_c$  are located, because we need to discharge the capacitance  $C_P$  (according to (III.2.1)) for going from  $V_a$  to  $V_c$  during the open-stage between  $V_a$  and  $V_c$ , as shown in **Figure III.3**a. In the second case with  $V_a < V_b$ , the classification becomes  $V_a < V_b < V_c$ . Since  $V_a < V_c$  in this case, the current *i* should be negative in the half period where  $V_a$  and  $V_c$  are located to charge the capacitance  $C_P$  and thus going from  $V_a$  to  $V_c$  during the open-stage between  $V_a$  and  $V_c$ , as illustrated **Figure III.3**b. These two cases are represented in **Figure III.4**.



Figure III.3. Conversion cycle for: (a) V<sub>c</sub><V<sub>b</sub><V<sub>a</sub>, (b) V<sub>a</sub><V<sub>b</sub><V<sub>c</sub>

From these two cases,  $V_b$  is always defined between  $V_a$  and  $V_c$ . In order to unify both cases, we can define a positive  $\beta Q_b V_b$  energy flow during the  $V_b$  stage by introducing a coefficient  $\beta$  depending on the  $Q_b$ 's charge sign. Hence, there are two cases for  $\beta$ :

- A positive power flow is <u>taken</u> under V<sub>b</sub> stage: β=1 for V<sub>c</sub><V<sub>b</sub><V<sub>a</sub> ⇔ βV<sub>c</sub>< βV<sub>b</sub>< βV<sub>a</sub>.
- *A positive power flow is <u>supplied</u> from V<sub>b</sub> stage:* β=-1 for V<sub>a</sub><V<sub>b</sub><V<sub>c</sub> ⇔ βV<sub>c</sub>< βV<sub>b</sub>< βV<sub>a</sub>.

These two configurations can be merged into a single representation, where the voltage  $V_P$  and the current *i* are multiplied by the factor  $\beta$  leading to a unique classification:  $\beta V_c < \beta V_b < \beta V_a$ . The resulting classification enables to merge all possible cycles in a single conversion cycle representation and to obtain a generic model regarding only the power flow and voltage levels.

The Figure III.4 shows the generic conversion cycle. The extremum voltage  $V_{zvst3}$  (respectively  $V_{zvst6}$ ) is sometime required between  $V_b$  and  $V_a$  (respectively  $V_b$  and  $V_c$ ) to ensure the ZVS conditions when one terminal of the PR is floating, it is occurring during the inversion of the polarity of the current *i*. Therefore, for a given voltage levels triplet {V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub>}, we construct a conversion cycle by firstly identifying the median voltage  $V_\beta$  of {V<sub>1</sub>, V<sub>2</sub>, V<sub>3</sub>}, and then the parameter  $\beta$  that gives the power flow sign that depends on the charge transfer sign from  $V_\beta$  by:

$$\begin{cases} V_{\beta} = \text{median}\{V_1, V_2, V_3\} \\ \beta = -\text{sign}\left(Q_{V_{\beta}}\right) \end{cases}$$
(III.2.8)

Once  $\beta$  is known, {V<sub>a</sub>, V<sub>b</sub>, V<sub>c</sub>} can then be identified by:

$$\begin{cases} \beta V_a = \max\{\beta V_1, \beta V_2, \beta V_3\} \\ \beta V_b = \operatorname{median}\{\beta V_1, \beta V_2, \beta V_3\} \\ \beta V_c = \min\{\beta V_1, \beta V_2, \beta V_3\} \end{cases}$$
(III.2.9)

Therefore, this cycle shown in Figure III.4 is composed of 3-constant voltage stages and 3open-circuit stages.



Figure III.4. Generic conversion cycle.

The electrical connections to the constant voltage values are illustrated in Figure III.5, where the LC branch is modeled by a sinusoidal current source. Thus, the operating cycle is divided in six-stages as follows:

**t**<sub>0</sub>-**t**<sub>1</sub>: All switches are OFF during this stage, the resonant current  $\beta$  *i* charges the capacitance  $C_P$  (considering the sign of current in Figure III.4), so, the voltage  $\beta V_P$  goes from  $\beta V_c$  to  $\beta V_b$ .

**t**<sub>1</sub>-**t**<sub>2</sub>: The PR is connected to  $\beta V_b$ . So, the PR exchanges electric charge under  $\beta V_b$ :  $Q_b$ .

**t2-t3**: Again, all switches are OFF and PR is isolated. The voltage  $\beta V_P$  goes from  $\beta V_b$  to  $\beta V_{zvst3}$  by discharging the capacitance  $C_P$  with current  $\beta i$ , since  $\beta i$  is negative.

t3-t3':  $\beta i$  becomes positive and the capacitance  $C_P$  is being discharged. The voltage  $\beta V_P$  goes from  $\beta V_{zvst3}$  to  $\beta V_a$ . This stage is needed in some cases to turn-on switches with zero voltage switching-on. However, if  $\beta V_a = \beta V_{zvst3}$ , then this stage in not required. As, we consider the general case, this stage is taken into account for the following analysis.

t3'-t4: PR is connected to  $\beta V_a$ , and exchanges a charge  $Q_a$ .

**t**<sub>4</sub>–**t**<sub>5</sub>: The PR is isolated, and the current  $\beta i$  discharges the capacitance  $C_{P_i}$  so, the voltage  $\beta V_P$  decreases from  $\beta V_a$  to reach the voltage  $\beta V_c$  at t=t<sub>5</sub>.

**t**5–**t**5': The PR is connected to  $\beta V_{c}$ , and  $Q_{c}$  is the electric charge exchanged between the PR and  $\beta V_{c}$ . This stage ends to let the voltage go from  $\beta V_{c}$  to  $\beta V_{zvst6}$ .

t5'-t6: During this stage, the PR is isolated, and the voltage  $\beta V_P$  decreases from  $\beta V_c$  to reach  $\beta V_{zvst6}$  at t=t6. This stage ends when the current *i* changes of sign at the end of period.



Figure III.5. (a) Connected stage, (b) Open-circuit stage.

This cycle is repeated at the PR's oscillation frequency. In some cases, as proposed by [39], the cycle can be applied only on a few periods, during the other periods the piezoelectric being short-circuited. This enables to reduce the output power level without reducing too much the power per cycle, reducing the operating frequency shift. The high quality factor being sufficient to keep the mechanical oscillation amplitude between two effective cycles.

# III.2.3 Energy approach

The conversion principle of the piezo-based power converter is based on a balance of energy and charge over each period of conversion in steady-state operation. Therefore, for the generic conversion cycle, Equation (III.2.10) gives the charge balance and equation (III.2.10) gives the energy balance without considering the losses in the PR and the switches. Thus, the conversion cycle can be represented in a diagram  $V_P vs Q$ , where the open-circuit stage operates with constant charge (Q=constant), while connected stage operates at constant voltage ( $V_P$ =constant).

$$Q_a + Q_b + Q_c = 0 \tag{III.2.10}$$

$$\beta V_a Q_a + \beta V_b Q_b + \beta Q_c V_c = 0 \tag{III.2.11}$$

Figure III.6 illustrates  $V_P$  vs Q for the switching sequence illustrated in Figure III.4. As shown, the diagram alternates between constant voltage (horizontal displacement) and constant charge stage (vertical displacement). From this diagram, the charge exchanged during each connected stage are deduced by (III.2.12)-(III.2.14), and the energy exchanged during each constant voltage stage is represented by the area under the curve. The cycle is closed, which means that the charge are balanced. The global energy exchanged during one cycle is the area surrounded, the area surrounded in one direction is positive and the area surrounded in the opposite direction is negative. Here, the positive area in orange is equal to the negative area in blue and purple, meaning a zero global energy exchange respecting thus the energy balance.



Figure III.6.  $V_P$  vs Q diagram.

This representation makes it easy to visualize and to understand the energy and charge transfer over a period of conversion in steady state operation.

$$Q_a = q_4 - q_{3'} \tag{III.2.12}$$

$$Q_b = q_2 - q_1$$
 (III.2.13)

$$Q_c = q_{5'} - q_5 \tag{III.2.14}$$

# III.3 Steady state analytical model

In this part, we propose an analytical model to calculate the time-duration of each stage and to find the amplitude of current I for any six-switching sequences to fit the requirements in terms of the output power, and also to establish the control laws by identifying the key parameters to control. The current amplitude I is a main sizing parameter for the PR. That amplitude depends on the switching sequences, so, having I as a function of the switching sequence and the operating conditions (V<sub>in</sub>, V<sub>out</sub> and P<sub>out</sub>) allows to design the PR. To do so, we propose a method to evaluate I over the various switching sequences and operating points.

#### III.3.1 Charge transfer

For simplification, *i* is considered as a sinusoidal waveform. This approximation will be validated in the simulation part. The charge exchanged during each constant voltage stage is estimated by integrating the current *i* (III.2.2), as given in (III.3.1)-(III.3.3), where  $\gamma_i = \cos \omega t_i$ . Thus, the charge depends only on the time duration of the connected stage and the amplitude of *I*.

$$Q_a = \beta \frac{I}{\omega} (\gamma_4 - \gamma_{3\prime}) \tag{III.3.1}$$

$$Q_b = \beta \frac{I}{\omega} (\gamma_2 - \gamma_1) \tag{III.3.2}$$

$$Q_c = \beta \frac{I}{\omega} (\gamma_{5'} - \gamma_5) \tag{III.3.3}$$

These expressions give the charge exchanged during each connected stage. So, assuming the charge balance during steady state operation (no accumulation of charge), one can find a relation between the instants  $\{t_{0..., t_{6}}\}$ , as is given by (III.3.4).

$$(\gamma_4 - \gamma_{3'}) + (\gamma_2 - \gamma_1) + (\gamma_{5'} - \gamma_5) = 0$$
(III.3.4)

In addition, during open-stage, as the voltage  $V_P$  is evolving by charging and discharging the capacitance  $C_P$ , the electric charge required for each open stage is determined by ( $C_P \Delta U$ ), as given in (III.3.5)-(III.3.9).

$$\beta(V_b - V_{zvst6})C_P = \beta \frac{I}{\omega}(\gamma_1 - \gamma_0)$$
(III.3.5)

$$\beta(V_{zvst3} - V_b)C_P = \beta \frac{I}{\omega}(\gamma_3 - \gamma_2)$$
(III.3.6)

$$\beta(V_a - V_{zvst3})C_P = \beta \frac{I}{\omega}(\gamma_{3\prime} - \gamma_3)$$
(III.3.7)

$$\beta(V_c - V_a)C_P = \beta \frac{I}{\omega}(\gamma_5 - \gamma_4)$$
(III.3.8)

$$\beta(V_{zvst6} - V_c)C_P = \beta \frac{I}{\omega}(\gamma_5, -\gamma_6)$$
(III.3.9)

Assuming that the voltage  $\beta V_P$  is capped between its minimum (i.e.,  $\beta V_{zvst6}$ ) and maximum (i.e.,  $\beta V_{zvst3}$ ) values, the sum of charge (III.3.5) to (III.3.6) gives the charge required to go from minimum to maximum amplitude of  $V_P$ :  $\beta (V_{zvst3} - V_{zvst6})C_P$ , while the sum of (III.3.7) to (III.3.9) gives the charge required to go from maximum to minimum amplitude of  $V_P$ :  $\beta (V_{zvst6} - V_{zvst3})C_P$ . Consequently, the amplitude of the circulating current  $I_{circulating}$  required to charge and discharge the capacitance  $C_P$  is then deduced by (III.3.10). This part of the current is required only for charging and discharging the capacitance  $C_P$  without any power transfer to load, and it is directly proportional to the  $C_P\omega$  (i.e., inverse of the impedance  $C_P$ ) value and the voltage excursion.

$$I_{circulating} = \frac{\beta(V_{zvst3} - V_{zvst6})}{2} C_P \omega$$
(III.3.10)

#### III.3.2 Energy transfer

As mentioned before, the PR operates with energy balance leading to sustained oscillation. Equation (III.2.11) illustrates the energy balance without including the losses of PR. By considering the electric model of PR, its losses (i.e., estimated by  $1/2R_PI^2$ ) can be integrated in the energy balance equation as shown in (III.3.11).

$$\beta V_a Q_a + \beta V_b Q_b + \beta V_c Q_c = \frac{1}{2} R_P I^2 T$$
(III.3.11)

By using charge balance, we deduce a relation between each charge stage:

$$Q_b = AQ_a + B \tag{III.3.12}$$

$$Q_c = -(1+A)Q_a - B$$
 (III.3.13)

Where A and B are:

$$A = \frac{V_c - V_a}{V_b - V_c}, \quad B = \frac{R_P I^2 T}{2\beta (V_b - V_c)}$$
(III.3.14)

By including equations (III.3.1)-(III.3.3) in (III.3.11), one can obtain a second relation between the instants  $\{t_0..., t_6\}$  as shown in (III.3.15). The energy balance is mainly linked to time-duration of each constant voltage stage and to the voltage levels. This expression is simple, and can be simpler if one voltage level is equal to 0, and moreover simplified by removing losses.

$$V_a(\gamma_4 - \gamma_{3'}) + V_b(\gamma_2 - \gamma_1) + V_c(\gamma_{5'} - \gamma_5) = \frac{\pi R_P I}{\beta}$$
(III.3.15)

#### III.3.3 Load current

To determine the current flowing to the output load, we consider a constant output voltage without ripple. Therefore, the mean output current  $I_{out}$  is determined by summing the charges exchanged during each constant voltage stage where  $V_{out}$  is involved. As said before, the voltage levels { $V_a$ ,  $V_b$ ,  $V_c$ } can be the input voltage/the output voltage or a linear combination of the input and the output voltage, or 0V. Thus, by considering a general case, we introduce three parameters named ( $\alpha_a$ ,  $\alpha_b$ ,  $\alpha_c$ ) for each voltage level respectively { $V_a$ ,  $V_b$ ,  $V_c$ }, so,  $\alpha_a$  (respectively  $\alpha_b$ ,  $\alpha_c$ ) is defined regarding to  $V_a$  (respectively  $V_b$ ,  $V_c$ ) by:

$$\begin{cases} \alpha_{a} = -1 \text{ if } V_{a} \text{ contains } (-V_{out}) \\ \alpha_{a} = +1 \text{ if } V_{a} \text{ contains } (+V_{out}) \\ \alpha_{a} = 0 \text{ otherwise} \end{cases}$$
(III.3.16)

Then, the load current is calculated by using (III.3.17). This expression shows that the average current transferred to the load is highly depending on the switching sequences. Indeed,

for the switching sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  charges are transferred to the load during all the three connected stage minimizing the amplitude of *I* compared to  $I_{out}$ .

For the switching sequence ( $V_{in}$ , Zero,  $V_{out}$ ), the charge transfer to the load occurs only during one stage which inducing a higher current amplitude I at same output current compared to the previous switching sequence.

$$I_{out} = \frac{P_{out}}{V_{out}} = -\frac{(\alpha_a Q_a + \alpha_b Q_b + \alpha_c Q_c)}{T}$$
(III.3.17)

This expression can be reworded as a function of  $Q_a$ , as shown in (III.3.18). The expression (III.3.18) states that the current  $I_{out}$  is mainly depending on  $Q_a$  which itself depends on the time duration of  $[t_3', t_4]$ . The transition time  $t_3'$  is the instant where  $V_p$  is equal to  $V_a$  and it cannot be changed, the stage duration is then only controlled by  $t_4$  which is free to move. Equation (III.3.18) reveals that the degree of freedom is reduced to one parameter (in general case,  $t_4$  is chosen to manage the output power), and the other instants { $t_0, t_1, t_2, t_3, t_3', t_5, t_5', t_6$ } are deduced directly to ensure ZVS, soft charging, energy and charge balance. Therefore, Equation (III.3.18) gives a way to control the output (current or voltage).

$$I_{out} = -\left((\alpha_a - \alpha_c) + (\alpha_b - \alpha_c)A\right)\frac{Q_a}{T} - \frac{B}{T}(\alpha_b - \alpha_c)$$
(III.3.18)

For a lossless PR (i.e.,  $R_P=0$ , so, B=0), the equation (III.3.18) can be simplified by:

$$I_{out} = -\left((\alpha_a - \alpha_c) + (\alpha_b - \alpha_c)A\right)\frac{Q_a}{T}$$
(III.3.19)

#### III.3.4 Estimation of the amplitude of the current *i*

As mentioned in charge transfer section, the current *I* is determined by the one needed to charge and discharge the capacitance  $C_P$  (III.3.10) and by the one required to supply the output load (III.3.18) which depends on the switching sequence and the load. By combining the previous equations (III.3.4)-(III.3.9) with (III.3.19) and considering lossless PR (i.e., B=0) for reaching a readable equation, one deduces the amplitude of the current *I* which is given by (III.3.20). This expression is applicable to all switching sequences, and takes into account the PR's proprieties and the operating points ( $V_{in}$ ,  $V_{out}$ ,  $I_{out}$ ).

$$I = \frac{\beta \pi}{(\alpha_b - \alpha_c) + (\alpha_a - \alpha_c)A_0} I_{out} + I_{circulating} = I_{useful} + I_{circulating}$$
(III.3.20)

where 
$$A_0 = \frac{V_c - V_b}{V_a - V_c}$$
,  $I_{circulating} = \frac{\beta(V_{ZVSt3} - V_{ZVSt6})}{2} C_P \omega$ .

 $I_{circulating}$  is the amplitude of the current required to charge and discharge the capacitance  $C_P$ , this amplitude is required even with no load.  $I_{useful}$  is the amplitude of the current required to provide the load current  $I_{out}$ , its amplitude is proportional to  $I_{out}$  and depends on the switching sequences. Regarding to the charge transfer utilization *K*-factor<sup>1</sup> defined in [27], we can express the *K*-factor as a function of our parameters, as given by (III.3.21).

$$K = \frac{(\alpha_a + \alpha_b) - (\alpha_c - \alpha_a)A_0}{2\beta}$$
(III.3.21)

Once the amplitude of the current *I* is determined as a function of the operating conditions, the conversion cycle can be plotted by estimating the transition time between each stage  $\{t_0 = \arccos\left(\frac{\gamma_0}{\omega}\right), \dots t_6 = \arccos\left(\frac{\gamma_6}{\omega}\right)\}$  by using (III.3.22)-(III.3.30). These equations show that the instants are mainly linked to the operating conditions  $\{V_{in}, V_{out}, P_{out}, f \text{ and } C_p\}$ . For cycles defined under charge and energy balance conditions, and for conversion cycle based on six stages, the output load is regulated by acting on the instant  $t_4 = \arccos\left(\frac{\gamma_4}{\omega}\right)$  because this instant controls the charge  $Q_a$  while the others instants are determined to ensure the ZVS operation and soft charging of C<sub>P</sub>. Therefore, the equation (III.3.27) can be used as a transfer function to manage the output current through  $t_4$ , this equation can be used for any switching sequence.

$$\gamma_0 = 1 \tag{III.3.22}$$

$$\gamma_1 = \beta (V_b - V_{ZVSt6}) \frac{\beta I}{C_P \omega} + \gamma_0$$
(III.3.23)

$$\gamma_2 = \beta (V_b - V_{ZVSt3}) \frac{\beta I}{C_P \omega} + \gamma_3$$
(III.3.24)

$$\gamma_3 = -1 \tag{III.3.25}$$

<sup>&</sup>lt;sup>1</sup> The *K*-factor in [27], quantifies the charge transfer delivered to the output load. Also, the *K*-factor indicates how efficiently is used the PR. This factor is mainly depending on the switching sequences and  $V_{in}$  and  $V_{out}$ .

$$\gamma'_{3} = \beta (V_{ZVSt3} - V_{a}) \frac{\beta I}{C_{P}\omega} + \gamma_{3}$$
(III.3.26)

$$\gamma_4 = 1 + \frac{2\pi}{(B_0 - A_0)(\alpha_a - \alpha_b)} \frac{I_{out}}{\beta I} - \beta (V_c - V_a) \frac{C_P \omega}{\beta I}$$
(III.3.27)

$$\gamma_{5} = 1 + \frac{2\pi}{(B_{0} - A_{0})(\alpha_{a} - \alpha_{b})} \frac{I_{out}}{\beta I}$$
(III.3.28)

$$\gamma'_{5} = \beta (V_{c} - V_{ZVSt6}) \frac{\beta I}{C_{P} \omega}$$
(III.3.29)

$$\gamma_6 = 1 \tag{III.3.30}$$

Where  $B_0 = \frac{a_c - \alpha_a}{\alpha_a + \alpha_b}$ .

From the proposed model, one can first determine the current *I* from (III.3.20), and then deduces the instants  $t_0$  to  $t_6$  on the cycle thanks to equations (III.3.22) to (III.3.30). Furthermore, the relation between  $t_4$  and  $I_{out}$  helps to determine the loop to regulate the output voltage.

## III.4 Converter topologies and conversion cycles

### **III.4.1** Switching Sequences Implementation

As mentioned before, the voltages  $V_a$ ,  $V_b$  and  $V_c$  can be zero (a short-circuit), the input voltage, the output voltage, a combination of them, with a positive or negative polarity ( $V_i$ =+/- $V_{in}$ +/- $V_{out}$  or Zero). Therefore, starting from these various combinations, we can enumerate the conversion cycles, where some of them are mentioned and/or explored in [24]-[28]. For example, for a given 3-voltage levels triplet { $V_{in}$ - $V_{out}$ ,  $V_{out}$ , 0V} [27], which operates as step-down converter, we can have  $V_{out}$ >  $V_{in}$ - $V_{out}$  or  $V_{out}$ Vin- $V_{out}$  or  $V_{out}$ >  $V_{in}$ - $V_{out}$ , the voltage level  $V_{in}$ - $V_{out}$  is the median voltage, so, a positive power flow is provided from this voltage leading to a factor  $\beta$  equals to -1. Thus, we can identify the voltages { $V_a$ ,  $V_b$ ,  $V_c$ } by using (III.2.9) as below:

$$\begin{cases}
-V_a = \max\{-(V_{in} - V_{out}), -V_{out}, 0\} = 0 \\
-V_b = \max\{-(V_{in} - V_{out}), -V_{out}, 0\} = -(V_{in} - V_{out}) \\
-V_c = \min\{-(V_{in} - V_{out}), -V_{out}, 0\} = -V_{out}
\end{cases}$$
(III.4.1)

Also, the amplitude of the current is immediately determined from (III.3.20) as follows:

$$I = \pi \frac{V_{out}}{V_{in}} I_{out} + \frac{V_{in}C_P\omega}{2} = I_{useful} + I_{circulating}$$
(III.4.2)

Where,  $\alpha_a = 0, \alpha_b = -1, \alpha_c = +1, \beta = -1, K = \frac{V_{in}}{2V_{out}}$ .

In case of  $V_{in}$ - $V_{out}$  > $V_{out}$ ,  $V_{out}$  is then the median voltage, so, a positive power flow is taken under this connected stage leading to  $\beta$  equals to 1. Then, the voltages { $V_a$ ,  $V_b$ ,  $V_c$ } are determined as:

$$\begin{cases} V_{a} = \max\{V_{in} - V_{out}, -V_{out}, 0\} = V_{in} - V_{out} \\ V_{b} = \max\{V_{in} - V_{out}, V_{out}, 0\} = V_{out} \\ V_{c} = \min\{V_{in} - V_{out}, V_{out}, 0\} = 0 \end{cases}$$
(III.4.3)

The amplitude of current *I* is then deduced:

$$I = \pi \frac{V_{in}}{V_{in} - V_{out}} I_{out} + \frac{V_{in}C_P\omega}{2} = I_{useful} + I_{circulating}$$
(III.4.4)

Where, 
$$\alpha_a = -1$$
,  $\alpha_b = +1$ ,  $\alpha_c = 0$ ,  $\beta = +1$ ,  $K = \frac{V_{in}}{2(V_{in} - V_{out})}$ .

TABLE III.2 shows the various possible switching sequences {V<sub>a</sub>, V<sub>b</sub>, V<sub>c</sub>} with a valid classification sequence {V<sub>a</sub>, V<sub>b</sub>, V<sub>c</sub>}, with the corresponding parameters { $\beta$ ,  $\alpha_a$ ,  $\alpha_b$ ,  $\alpha_c$ } for each switching sequence. The following switching sequences shown in TABLE III.2 do not take into account the number of required switches or the need or not of bidirectional switches. In addition, the expression of the current *I* is given for each conversion cycle, which is separated into the circulating current and the current needed to achieve the output current. After choosing

the switching sequence fitting a need, the topology of the piezo-based dc-dc converter can be built to ensure the switching sequence.

TABLE III.2. Switching Sequences and Current Expressions. The topologies(a)-(i) are shown														
in Figure III.8.														
Voltages triplet	Topology	Va	$V_b$	V <sub>c</sub>	V <sub>ZVS_t3</sub>	V <sub>ZVS_t6</sub>	β	α <sub>a</sub>	α <sub>b</sub>	α <sub>c</sub>	K	$g = \frac{V_{out}}{V_{in}}$	I <sub>useful</sub>	$I_{circulating}$
VinsVout, 0	(c), (a),(h)	V <sub>in</sub>	V <sub>out</sub>	0	V <sub>in</sub>	0	1	0	1	0	$\frac{1}{2}$	<i>g</i> < 1	<i>g</i> < 1	$\frac{V_{in} C_p \omega}{2}$
	(b),(d),(i)	0	V <sub>in</sub>	V <sub>out</sub>	0	V <sub>out</sub>	-1	0	0	1	$\frac{1}{2g}$	<i>g</i> > 1	$\pi g I_{out}$	$\frac{V_{out} C_p \omega}{2}$
V <sub>in</sub> ,-V <sub>out</sub> , 0	(e)	V <sub>in</sub>	0	-V <sub>out</sub>	V <sub>in</sub>	-V <sub>out</sub>	1	0	0	-1	$\frac{1}{2}$	any	πI <sub>out</sub>	$\frac{(V_{in}+V_{out}) C_p \omega}{2}$
Via-Vant Vant 0	(a)	V <sub>in</sub> - V <sub>out</sub>	V <sub>out</sub>	0	V <sub>in</sub>	0	1	-1	1	0	$\frac{1}{2(1-g)}$	$g < \frac{1}{2}$	$\pi(1-g)I_{out}$	$\frac{V_{in} C_p \omega}{2}$
V in- V out, V out, U	(a)	0	V <sub>in</sub> - V <sub>out</sub>	V <sub>out</sub>	V <sub>in</sub>	V <sub>out</sub>	-1	0	-1	1	$\frac{1}{2g}$	$\frac{1}{2} < g$ < 1	$\pi g I_{out}$	$\frac{V_{in} C_p \omega}{2}$
Vin-Vout, Vout, - Vout	(Figure III.9)	V <sub>in</sub> - V <sub>out</sub>	V <sub>out</sub>	-V <sub>out</sub>	V <sub>in</sub>	-V <sub>out</sub>	1	-1	1	-1	1	$g < \frac{1}{2}$	$\frac{\pi}{2}I_{out}$	$\frac{(V_{in}+V_{out}) C_p \omega}{2}$
	(Figure III.9)	-V <sub>out</sub>	V <sub>in</sub> - V <sub>out</sub>	V <sub>out</sub>	-V <sub>out</sub>	V <sub>in</sub>	-1	-1	-1	1	$\frac{1}{2g}$	$\frac{1}{2} < g$ < 1	$\pi g I_{out}$	$\frac{(V_{in}+V_{out}) C_p \omega}{2}$
Vin,-Vout, Vout	(Figure III.9)	V <sub>in</sub>	V <sub>out</sub>	$-V_{out}$	V <sub>in</sub>	-V <sub>out</sub>	1	0	1	-1	$\frac{1}{(1+g)}$	<i>g</i> < 1	$\frac{\pi}{2}(1+g)I_{out}$	$\frac{(V_{in}+V_{out}) C_p \omega}{2}$
V <sub>in</sub> , V <sub>out</sub> , V <sub>in</sub> -V <sub>out</sub>	(a)	V <sub>in</sub>	V <sub>out</sub>	V <sub>in</sub> - V <sub>out</sub>	V <sub>in</sub>	0	1	0	1	-1	$\frac{1}{2g}$	$\frac{1}{2} < g$ < 1	$\pi g I_{out}$	$\frac{V_{in} C_p \omega}{2}$
V <sub>in</sub> -V <sub>out</sub> , 0, -V <sub>out</sub>	(c),(e),(f)	V <sub>in</sub> - V <sub>out</sub>	0	$-V_{out}$	V <sub>in</sub>	-V <sub>out</sub>	1	-1	0	-1	$\frac{1}{2}$	<i>g</i> < 1	$\pi I_{out}$	$\frac{(V_{in}+V_{out}) C_p \omega}{2}$
V <sub>out</sub> , V <sub>in</sub> , V <sub>out</sub> -V <sub>ir</sub>	(d)	V <sub>out</sub> - V <sub>in</sub>	V <sub>in</sub>	V <sub>out</sub>	0	V <sub>out</sub>	-1	1	0	1	$\frac{1}{2}$	1 < g < 2	$\pi I_{out}$	$\frac{V_{out} C_p \omega}{2}$
$V_{in}, V_{out}$ - $V_{in}$ 0	(d)	V <sub>in</sub>	V <sub>out</sub> - V <sub>in</sub>	0	$V_{in}$ + $V_{out}$	0	1	0	1	0	$\frac{1}{2}$	1 < g < 2	$\pi I_{out}$	$\frac{(V_{in}+V_{out}) C_p \omega}{2}$
	(d)	0	V <sub>in</sub>	V <sub>out</sub> - V <sub>in</sub>	0	$V_{in}$ + $V_{out}$	-1	0	0	1	$\frac{g-1}{2}$	<i>g</i> > 2	$\frac{\pi}{(g-1)}I_{out}$	$\frac{(V_{in}+V_{out}) C_p \omega}{2}$
V <sub>in</sub> ,V <sub>in</sub> -V <sub>out</sub> , 0	(b),(e),(g)	V <sub>in</sub>	0	V <sub>in</sub> - V <sub>out</sub>	V <sub>in</sub>	V <sub>in</sub> - V <sub>out</sub>	1	0	0	-1	<u>g</u> 2	<i>g</i> > 1	$\frac{\pi}{g}I_{out}$	$\frac{V_{out} C_p \omega}{2}$

Actually, the current amplitude I gives the key element of physical constraints for the PR and the switches. Indeed, at a specific frequency in its inductive behavioral, the PR has a current limitation per square centimeter, and then, for minimizing the piezoelectric material volume, we have to minimize the current amplitude I for a given output current value. Also, the amplitude I can be used to compare the converter topologies and conversion cycles. Indeed, at the same current amplitude I, the output current can be higher by maximizing K-factor. The maximum value for the *K*-factor is 1. K=I means that  $I = \frac{\pi}{2}I_{out}$  (omitting the circulating current) which corresponds to the average value of a rectified sine wave. It is obtained while the switching sequence ensures multiple connections with the output load during each constant voltage stages. It is for example the sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$ . This switching sequence operates with a gain ratio lower than 0.5. At the opposite, the K-factor is lower (i.e., high amplitude of the current I) for a switching sequence like  $\{V_{in}, -V_{out}, 0\}$ , where a half of the period is connected to zero without any power transfer. However, this switching sequence can operate at any gain ratio. Therefore, regarding the operating conditions and the need of the power/voltage and the conversion ratio, the switching sequence should be carefully selected to minimize I, but also to minimize the switch number and the voltages they have to sustain.

Figure III.7 shows some examples of switching sequences for step-down converters and step-up converters. For instance, the conversion cycle (A) shown in Figure III.7 is suitable for low gain ratio conversion  $2V_{out} < V_{in}$ , and it enables a direct energy transfer thanks to the stage  $V_a=V_{in}-V_{out}$  allowing by that to reduce the energy stored in the PR.



Figure III.7. Examples of switching sequences.

#### III.4.2 Piezo-Based dc-dc Converters: converter sequences

As illustrated in the previous paragraph, the PR can be driven by a large number of switching sequences. In [27]-[36], various topologies are enumerated and/or explored based on using a single PR. For a conversion cycle based on six stages (3-connected stages, 3-open circuit stages), the switching sequence can be driven with a minimum number of switches of:

- 4- switches if both ends of PR are floating, as shown in Figure III.5a
- 3-switches if one terminal of the PR is connected to V<sub>in</sub>, or V<sub>out</sub> or grounded, but it requires at least one bidirectional-blocking switch to avoid the short-circuit of the source/load or direct connection of the source and the load.

The **Figure III.8** shows the converter topologies, which are composed of four switches {S1...S4} and a single PR, as shown **Figure III.8a-e**, or a bidirectional-blocking switch and two unidirectional-blocking switches {S1...S3}, as shown in **Figure III.8f-i**. In case of the topologies with an unidirectional switch, a diode in series with unidirectional switch can be used as a replacement. Also, for some switching sequences, two active switches can be replaced by diodes, as their conduction stage depends on the polarity of the PR's current *i*.

Considering the number of switches employed, the possible switching sequences are summarized in nine-switching sequences. **TABLE III.2** shows the switching sequences related to the converter topologies. By reducing the number of switches, the implementation of the switching sequences is easier [27]. However, besides the number of switches, this approach does not take into consideration how the PR is used, but only minimizing the number of the switches.















(e)



(g)

(h)

(i)



Figure III.8. Converter Topologies based on four switches [27], [36].

Figure III.9 shows the topology derived from the topology shown in Figure III.8h, which ensures the switching sequence  $\{V_{in}, 0, V_{out}\}$  with g=V<sub>out</sub>/V<sub>in</sub> < 1. The derived topology allows to modify the previous switching sequence into  $\{V_{in}, V_{out}, V_{out}\}$ , but it needs two additional switches S4 and S5. By increasing the number of connections with the load, this switching sequence reduces the current I and then the energy stored in the PR and it maximize the charge transfer.



Figure III.9. The proposed topology [28].

The topology shown in **Figure III.9** is not limited to provide the sequence  $\{V_{in}, V_{in}-V_{out}, V_{out}, V_{out}\}$ , but it enables also various other switching sequences that are mentioned in **TABLE III.2**. Therefore, regarding the operating conditions shown in **TABLE III.2**, these switching sequences can be applied in consequence. Also, for operation as step-up dc-dc converter g>1, S1 should be replaced by a bidirectional switch, which allows that the converter can operate as buck-boost converter.

TABLE III.3. Examples of Switching Sequences Used with the Proposed Topology.									
	Conditions	V <sub>in</sub>	$V_{in}$ - $V_{out}$	-V <sub>out</sub>	Zero	V <sub>out</sub>			
Mode 1	Any	i>0		i>0	i <0				
Mode 2	$2V_{out} < V_{in}$		i >0	i >0		i <0			
Mode 3	$V_{out} < V_{in}$	i>0			i >0	i <0			
Mode 4	V <sub>out</sub> <v<sub>in</v<sub>	i>0		i >0		i <0			
Mode 5	$2V_{out} < V_{in}$		i>0		i >0	i <0			
Mode 6	$2V_{out} > V_{in}$		i>0		i <0	i <0			
Mode 7	$V_{out} < V_{in} < 2V_{out}$	i>0	i>0			i <0			

#### III.4.3 Example of implementation of a switching sequence

Figure III.10a shows the steady-state operation of the dc-dc converter based on the PR for the topology shown in Figure III.9 and for the switching sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$ . As noted before, the current in the LCR branch is assumed sinusoidal, since the PR operates in the inductive region and has a high quality factor.



Figure III.10. Key waveforms of the dc-dc converter for the switching sequence  $\{V_{in} - V_{out}, V_{out}, -V_{out}\}$ : (a) ideal switching sequence, (b) switching sequence with soft variation on  $V_{p^+}$  and  $V_{p^-}$  to reduce switching losses.

Therefore, the switching sequence has six stages of operation, as shown on Figure III.10a. In this figure, the waveform of  $V_P$ ,  $V_{P^+}$  (right leg of the PR) and  $V_{P^-}$  (left leg of the PR) are displayed over a period of conversion, so, the following description gives the operation for each stage:

[t<sub>0</sub>, t<sub>1</sub>] All switches are turned OFF during this stage as shown in Figure III.11d, and the voltage across  $C_P$  increases by charging the capacitance  $C_P$  since the current *i* is negative (III.2.1).  $V_P$  goes from  $-V_{out}$  to  $V_{out}$ , as shown in Figure III.10a.

[ $t_1$ ,  $t_2$ ] The switches S2, S3 and S5 are turned ON, and the voltage  $V_P$  is equal to  $V_{out}$ , as shown in Figure III.11b. During this stage, the PR transfers charges to the load. This stage ends by turning OFF S2.

 $[t_2, t_3]$  The PR is in open-circuit stage, and voltage  $V_P$  increases from  $V_{out}$  to  $V_{in}$ - $V_{out}$ .

[ $t_3$ ,  $t_4$ ] The switches S1 and S4 are turned ON, and the PR is connected between the input and the output voltage (Figure III.11d). During this stage, the PR stores the electrical energy as mechanical inertia. This stage ends by turning OFF S1 at t= $t_4$ . The instant  $t_4$  enables to control the energy balance in the PR.

[t<sub>4</sub>, t<sub>5</sub>] All switches are turned OFF, and the PR is isolated. Since the current *i* is positive, the voltage  $V_P$  decreases by discharging the capacitance  $C_P$ , therefore,  $V_P$  goes from  $V_{in}$ - $V_{out}$  to - $V_{out}$ .

 $[t_5, t_6]$  The switches S4 and S6 are turned ON as illustrated in Figure III.11f, and the PR is connected to load. A part of the stored charge in the PR is transferred to the load. This stage ends when the current *i* becomes negative.

This switching mode operation described above does not consider the parasitic capacitances of the switches. Indeed, when  $V_P = V_{out}$  at t=t<sub>2</sub>, it means that  $V_{P+}=V_{out}$  and  $V_{P-}=0$  and the current *i* is negative. Still *i* <0, the voltage  $V_{P+}$  increases while  $V_P$ . decreases, however,  $V_P$  can go below 0V, as  $V_P$  is capped to 0V by the reverse diode of S5, so,  $V_P=V_{P+}$  increases until to reach  $V_{in}-V_{out}$  at t=t<sub>3</sub>, as shown in **Figure III.10a**. Consequently, the drain-source voltage of S1 is equal to  $V_{in}-(V_{in}-V_{out})=V_{out}$ , the turn-on of S1 thus is not accomplished with ZVS operation, the same case goes for S4 which the drain-source is equal to  $V_{out}$ . To overcome this issue, we let the voltage  $V_P=V_{P+}$  reaching  $V_{in}$ , enabling this to turn-on S1 with ZVS at t=t<sub>3</sub>. At that time, *i* becomes positive,  $V_P$  decreases to reach  $V_{in}-V_{out}$ , as  $V_P$  increases to reach  $V_{out}$  in order to turn-on S4 with ZVS while  $V_{P+}$  remains fixed to  $V_{in}$  thanks to on-state of S1.

Hence, the stage [t<sub>2</sub>, t<sub>3</sub>] is divided into the following stages:

[t<sub>2</sub>, t<sub>3</sub>] The PR is isolated, and the voltage  $V_P$  increases as the current *i* is negative. Since, voltage  $V_{P-}$  is equal to 0 and  $V_{P+}$  increases from  $V_{out}$  to  $V_{in}$  in order to turn on S1 in ZVS mode at t=t<sub>3</sub>, as shown in Figure III.10b. This stage ends when the current *i* becomes positive.

[t<sub>3</sub>, t<sub>3</sub>'] The PR is also isolated, but the current *i* is positive. So, voltage  $V_P$  goes from  $V_{in}$  to  $V_{in}$ - $V_{out}$ , since  $V_{P+}$  is clamped to  $V_{in}$  thanks to S1 closed state, the voltage  $V_{P-}$  increases from 0 V to  $V_{out}$ . This stage ends by turning on S4 at t=t<sub>3</sub>' in ZVS mode (Figure III.10b).


Figure III.11. Circuit configurations.

The presented study for building a conversion cycle stage by stage can be conducted for any switching sequence, enabling to determine the control law of the switches. Nonetheless, in practice, we should consider the parasitic capacitance of the switches, in order to determine the need or not for the peaks  $V_{zvst3}$  and/or  $V_{zvst6}$ .

### III.5 Simulation to validate the operating principle

To check the switching sequence and the waveforms for the switching sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  during the steady-state operation, we have performed a simulation in LTSpice. In this simulation, we have used a spice model of the switches S1 to S6 (HEMT model: GaN 6650508B from GaNSystem) and the BVD model parameters for the PR are shown in TABLE III.4. In addition, the load is modeled by a voltage source aiming to obtain a steady state operation after a few periods, i.e., a short transient-mode. Figure III.12 shows the circuit used to validate the simulation with active switches.

TABLE III.4. PR's circuit C-213 from Fuji								
Parameter $R_P$ $C_P$ $C$ $L$ $f_r$ $f_{ar}$								
Value	0.4Ω	8.4nF	2.9nF	1.1mH	89kHz	104kHz		



Figure III.12. Simulation circuit.

Figure III.13 shows the voltage waveforms of the PR ( $V_p$  and its terminals  $V_{p+}$  and  $V_{p-}$ ) and the current *i* in the LCR branch, the simulation is done for a 120 V to 40 V step-down conversion and for an output power of 5 W. The steady state is reached after 10 periods. The computed instants {t<sub>0</sub>...t<sub>6</sub>} are firstly calculated from equations (III.3.22)-(III.3.30) and for an operating frequency of 98 kHz, which are tuned in the simulation since the proposed model did not consider the parasitic capacitances of switches in the calculation of the instants. As shown in Figure III.13, the illustrated waveforms matches the theoretical waveforms presented in Figure III.10b. Indeed, the simulation waveforms exhibit the connected stages and the opencircuit stages, and the switching sequence transition times {t<sub>0</sub>...t<sub>6</sub>} are depicted. Also, the sinusoidal waveform approximation of the current *i* established previously is verified by the simulation. The waveforms reveal that the ZVS of S2 is not achieved due to the parasitic capacitance of S3 (or D2), however, we propose a solution to overcome that limitation detailed in APPENDIX C. The amplitude of the current *I* measured in the simulation is equal to 0.657 A, while by using the equation (III.3.18) the amplitude of *I* is equal to 0.633 A. Therefore, the model accuracy is better than 5% for the estimation of *I*. This accuracy can be improved by including the parasitic capacitances and the conduction losses  $R_{dson}I_{eff}^2$  in the model of the PR; i.e., the capacitance  $C_P$  becomes  $C_P+C_{eq}$ , where  $C_{eq}$  is the equivalent capacitance of all the switches [27], the same method can be used for  $R_P$  by including  $R_{dson}$ .



Figure III.13. Simulated waveforms in the time domain for the switching sequence :  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}: V_{in} = 120 \text{ V}, V_{out} = 40 \text{ V}, P_{out} = 5 \text{ W} \text{ and } \eta = 99.1 \text{ \%}.$ 

#### III.6 Efficiency estimation

As shown by equation (III.3.20), the amplitude of current *i* is highly depending on the switching sequence, leading to an efficiency dependency. Equation (III.6.1) gives the expression to estimate the efficiency considering only the losses in the material  $P_{PR}$  due to the

damping effect, in order to select the appropriate switching sequence and the converter topology in order to minimize the energy stored in the material as first approach (while omitting the losses of the switches, number of the switches and their electrical constraints). Therefore, as we are considering a step-down converter AC-Grid (230/110 VAC) to load (<100V) applications, we have selected a six switching sequences from those listed in TABLE III.2 enabling a gain ratio conversion lower than 0.5. Some switching sequences are modified to consider the soft switching operation by considering the reached extremums  $V_{zvst3}$  and  $V_{zvst6}$ , for a fair comparison.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{1}{1 + \frac{P_{PR}}{P_{out}}} = \frac{1}{1 + \frac{0.5R_P l^2}{P_{out}}}$$
(III.6.1)

**Figure III.14** shows the evolution of the efficiency as a function of the output power for g = 0.083, 0.25 and 0.5 for input voltage of 120 V and for topologies adapted to these gain values enumerated in **TABLE III.2**. In this figure, we note that for low gain, the switching sequence { $V_{in}$ - $V_{out}$ ,  $V_{out}$ , - $V_{out}$ } offers the highest efficiency over the output power range compared to the other switching sequences, since this stage sequence yields a maximum of connected stage to the load, reducing the amplitude of current I and then reducing the losses.



(a): g=0.083



(b): g=0.25



(c): g=0.5

Figure III.14. Efficiency Vs Output Power for input voltage of 120 V and: (a): g = 0.083, (b) g = 0.25 and (c): g = 0.5.

By increasing the gain ratio toward 0.5 through Figure III.14a to Figure III.14b, the switching sequence  $\{V_{in}-V_{out}, 0, V_{out}\}$  becomes more competitive to  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$ . Indeed, current I is a sum of a part  $I_{useful}$  proportional to the output current and a part  $I_{circulating}$ needed for charging/discharging the capacitance  $C_P$  that depends on the voltage excursion of  $V_P$ . So, for the switching sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  the peak to peak voltage excursion is  $V_{in}+V_{out}$  and for the switching sequence  $\{V_{in}-V_{out}, 0, V_{out}\}$  the voltage excursion is  $V_{in}$ . The circulating current  $I_{circulating}$  is then higher for the sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  and the difference becomes significant while  $g=V_{out}/V_{in}$  increases. At the same time  $I_{useful}$  for the case  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  is lower than the one for the case  $\{V_{in}-V_{out}, 0_t, V_{out}\}$  while the gain is lower than 0.5. As illustrated in Figure III.14c, for a gain of 0.5 (the threshold value for Iuseful between the both sequences), the switching sequence  $\{V_{in}-V_{out}, 0, V_{out}\}$  offers the highest efficiency over all the power range, but the switching sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  remains competitive by increasing the output power, when current Icirculation becomes neglected compared to Iout. The stage Vin-Vout allows a direct energy transfer to load while storing energy in the PR, this stage helps to maximize the efficiency. On the other side, the zero voltage stage deteriorates the efficiency, because during this stage no energy is exchanged with the load or the source. Hence, for a better utilization of the PR it is preferable:

- avoiding the Zero-Voltage stage.
- using multiple connected stages with the output.

These criteria can be used to select the switching sequence that holds a better utilization of the PR, enabling to reduce the constraint in terms of size of the material while maintaining a high efficiency and a high power density.

In the **Figure III.15**, we have plotted the efficiency as a function of the gain ratio. This figure illustrates that the conversion cycle  $\{V_{in}-V_{out}, V_{out t}, -V_{out}\}$  offers the highest efficiency compared to the other switching sequences, while at the opposite  $\{V_{in}, -V_{out}, 0\}$  gives the worst case. The switching sequence  $\{V_{in}-V_{out}, -V_{out}, 0\}$  gives the same efficiency evolution as  $\{V_{in}, 0, V_{out}\}$ , since this switching sequence is just offsetting by  $V_{out}$  regarding to  $\{V_{in}, 0, V_{out}\}$ . The difference between the two previous cycles is that  $\{V_{in}-V_{out}, -V_{out}, 0\}$  has a peak-to-peak voltage of  $V_{in}+V_{out}$  to ensure the ZVS condition while  $\{V_{in}, 0, V_{out}\}$  has just  $V_{in}$ , leading to a higher  $I_{circulating}$ .



Figure III.15. Efficiency Vs Gain for  $P_{out} = 15$  W and  $V_{in} = 120$  V.

#### III.7 Analysis and discussion

A large number of conversion cycles are possible for six-stages operations. However, few of them are interesting for a better use of the PR in terms of efficiency and power density. Indeed, using the estimation of the efficiency and the current amplitude of the resonator gives a guideline to determine the appropriate switching sequence and then deducing the converter topology. In addition, the presented analysis provides an evaluation of the operation of the step-down dc-dc converters based on PR, which leads to select the converter with high efficiency and power density.

The current amplitude determined previously can be found by computing the derivative equations of the current/voltage  $\{i, V_p, V_c\}$  numerically as demonstrated in [27], with additional assumptions to obtain the exact steady state. This method is tedious, *as it should be computed by using 18 variables* and required appropriate initial conditions to reach the same behavior of the efficiency/current as previously with slightly higher accuracy [27]. A numerical model is presented in [44], this model firstly considers a sinusoidal current waveform *i*, and then uses Fourier transforms of V<sub>P</sub> to evaluate an induced equivalent capacitance placed in parallel to  $C_P$ . It enables to find the operating frequency and the current amplitude *I* and the angular transition times. The main advantage of this model is to find the operating frequency, to reduce transient

time simulation and to evaluate harmonic spectrum generated by the switching sequence. However, this approach requires a complex model and calculations, and the convergence time/accuracy depends on the calculation step number. Therefore, the approach here gives a fast solution to evaluate the efficiency, with simplified and readable equations. In addition, the proposed generic analytical model makes it easier to select the cycle, the topology, to identify the key parameters for the PR and to define the general structure of the closed-loop to regulate the output power/voltage.

Hence, a generic implementation of the control for six switching sequence can be built with the same method and can be used for any switching sequence regardless of the topology of the converter.

#### III.8 Summary of the chapter

In this chapter the operating principle of the dc-dc converter based on PR is fully detailed and explained, as well as the most relevant conversion cycles and topologies. A generic model is described, enabling to determine the current amplitude, the time duration of each stage and the efficiency for each switching sequence. A simulation based on a Spice model validates the operating principle while exhibiting a high efficiency. In addition, an efficient conversion cycle was identified for a high-to-low voltage conversion ratio. This one will be used for the rest of this thesis.

# Chapter IV: The piezoelectric-based DC-DC step-down converter: experimental validation

Abstract: This chapter is aimed to demonstrate experimentally the operating principle of the DC-DC converter based on a piezoelectric resonator. An actual prototype is designed to operate at various voltage and power levels demonstrating high efficiency operation. Parallelization of the PRs is investigated for a scalable power conversion. In addition, high frequency operation is shown using the thickness mode, which enables a high power level conversion up to 175 W. We conclude with discussion and the presentation of some challenges to overcome.

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#### IV.1 Introduction

The switching sequences based on dc-dc converters that employs PR as storage element were validated in a prior work [24] for various operating conditions in terms of voltage and power applications. As we are aiming for high-to-low voltage conversion, we have selected the conversion cycle by respecting the following criteria:

- > Low voltage gain ratio:  $g = \frac{V_{out}}{V_{in}} < 0.5$ .
- Minimum number of stages in the switching sequence: 6 stages.
- Maximizing energy transfer to the output load by maximizing the number of connections with the output load: {ex: V<sub>in</sub>-V<sub>out</sub>, V<sub>out</sub>, -V<sub>out</sub>}.

Therefore, considering these criteria, we have selected the switching sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  which is studied in details in this chapter. Figure IV.1a illustrates the selected conversion cycle based on six stages, while the Figure IV.1b shows the topology used to apply this switching sequence.

The proposed design considers the voltage and current constraints on the switches and PR . From the proposed design, a prototype has been built to validate the operating principle through the waveforms at various operating conditions. The efficiency and power density are measured. In addition, various vibrations modes are investigated, with various operating frequencies. The effect of spurious modes on the operation is studied and quantified by spectrum analysis.



Figure IV.1. (a) The conversion cycle  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$ , (b) the proposed dc-dc topology.

## IV.2 Piezoelectric Resonator: Electrical Equivalent Circuit and Design considerations

For a disc shape resonator (Figure IV.2), the converter can operate for the main vibration modes: radial mode and thickness mode. For the PZT material, the polarization is normal to the electrodes of the resonator. The radial mode is defined when the driving electric field is perpendicular to the displacement, and the thickness mode when the electric field is parallel to the displacement.



Figure IV.2. (a) Radial mode vibration (b) thickness mode vibration.

The equivalent electrical circuit model has been modeled in prior work [35], [50], BVD circuit. The equivalent model is composed of L-C-R<sub>P</sub> series branch that represents the motional behavior of the resonator for a vibration mode, in parallel with the capacitance named C<sub>P</sub>.

The equivalent circuits are shown in Figure IV.3. For the thickness mode, the induced capacitance  $-C_P$  in the motional branch is due to that the driving field is parallel to the displacement. It results from the coupling between the driving electric field and the one induced.



Figure IV.3. Equivalent BVD circuit for: (a) Radial mode vibration (b) thickness mode vibration, [35].

Therefore, we propose now to determine the electrical parameters of the BVDM equivalent electrical model from the material properties in radial and thickness mode.

(a) Radial mode (lateral mode) :  $(\vec{E} \perp \vec{D})$ 

For the radial mode, the model parameters are determined by the equations (IV.2.1) to (IV.2.5), [35]. These equations result from solving the fundamental equations of the piezoelectricity, which are well detailed in literature [35]. The resonant frequency can be determined by the diameter D and the resonant constant frequency in radial mode  $N_P$  (Hz.m) which depends on the physical proprieties of the material, and given by the manufacturers.

$$C_P = \frac{\varepsilon_{33}^S \pi D^2}{4th}$$
(IV.2.1)

$$C = \frac{8k_p^2}{\pi^2} C_P \tag{IV.2.2}$$

$$f_r = \frac{N_P}{D} \tag{IV.2.3}$$

$$L = \frac{1}{4\pi^2 f_r^2 C} \tag{IV.2.4}$$

$$R_P = \frac{2\pi f_r L}{Q} \tag{IV.2.5}$$

Where,  $\varepsilon_{33}^{S}$  is the clamped primitivity, as it is determined by assuming blocked-electrodes and can be measured at high frequency above 15 MHz as suggested by [38].

In the literature [18], [35], the capacitance *C* is also defined by  $k_{eff}^2 C_P$  for this vibration mode, where  $k_{eff}^2$  is the effective coupling factor and determined by:

$$k_{eff}^2 = \frac{f_{ar}^2 - f_r^2}{f_{ar}^2}$$
(IV.2.6)

Thus, using this simplified model, one can determine the electrical model by using the geometry parameters of the PR, the diameter D, the thickness *th*, and the physical proprieties of the material Q,  $k_p$ ,  $\varepsilon_{33}^S$  and N<sub>P</sub> which are generally given by the manufacturers.

## (b) Thickness mode: $(\vec{E} \parallel \vec{D})$

In thickness vibration mode, the equivalent circuit parameters are determined by (IV.2.7)-(IV.2.11), [35]. Also, the resonant frequency in this mode is determined as a function of the thickness *th* of the resonator and the constant frequency in thickness mode of the material named  $N_t$  (Hz.m).

$$C_P = \frac{\varepsilon_{33}^S \pi D^2}{4th} \tag{IV.2.7}$$

$$C' = \frac{8k_t^2}{\pi^2 - 8k_t^2} C_P$$
(IV.2.8)

$$L = \frac{1}{4\pi^2 f_r^2 C} \tag{IV.2.9}$$

$$R_P = \frac{2\pi f_r L}{Q} \tag{IV.2.10}$$

$$f_r = \frac{N_t}{th} \tag{IV.2.11}$$

The previous models described only the fundamental resonant mode regarding to the driving electric field. So, to fully describe the resonator behavior, an extra LCR branch should be added in parallel with  $C_P$  for each vibration modes. However, for a first approximation, we will use only the fundamental mode to design the resonator.

As shown in the previous part, the BVDM model is mainly linked to the physical proprieties and the geometry of the PR. For a simplified design, we have designed a resonator by ensuring the following conditions:

• High  $k^2Q$ 

In the prior work [18], the PR is selected for its high figure of merit  $k^2Q$ . Indeed, having high quality factor means low power loss due to low damping effect in the material, while a high coupling factor ensures a high electromechanical energy conversion ratio and then a high part of the energy mechanically stored can be exchanged at each cycle. Therefore, it is interesting to choose a ceramic with high  $k^2Q$ . Regarding the datasheet of the supplier, we have selected the PZT C213 from Fuji ceramics which exhibits the highest  $k^2Q$  (ex: Q=2500,  $k_P$ =58%) value [41].

• Insulation

As we are aiming to use the PR for high-to-low voltage power converter, the PR should withstand the maximum voltage applied. For most PZT based ceramics, the maximal electric field is between 1 kV/mm and 1.5 kV/mm (assumed), so, by considering the worst case of 1 kV/mm and a maximum voltage applied of 750 V ( $2V_{acmax}=2 \times 350 \text{ V}$ ), the thickness of the PR is then equal to 0.75 mm. The thickness could be higher but it leads to a lower power density [36].

Operating frequency

As mentioned previously, the PR operates between its series and parallel frequency (inductive region). Also, for the radial mode operation, the series resonant frequency is determined by its diameter. So, for operating frequency around 90 kHz, the diameter is calculated by using (IV.2.3), and equal to 25 mm considering C-213 material.

Therefore, considering the previous assumptions, the PR is sized and the equivalent circuit parameters are summarized in TABLE III.4.

TABLE IV.1. BVDM model parameters of the PR in radial mode from Fuji Ceramics C-213.									
	d	th	$C_P^*$	С	L	R	Q	$k_P$	fr
calculated	25mm	0.75mm	8.6nF	2.85nF	1.1mH	0.242Ω	2500	58%	90kHz
measured	25mm	0.75mm	8.4nF	2.9nF	1.1mH	0.5 <b>Ω*</b> *	1500	52%	89.5kHz
$C_P^*$ : the capacitance $C_P$ determined is not the "clamped" capacitance. As the capacitance $C_P$ is measured by using an impedance analyzer. So, this capacitance is obtained by applying a constant amplitude AC electric field that induces a displacement arising. The "clamped" capacitance $C_P$ can be measured at high frequency out of the resonance >15 MHz, but the measurement becomes highly sensitive to the setup.									

**Figure IV.4b** shows the impedance of the PR measured by using the impedance analyzer Wayne Kerr 6500B. As we operate in radial mode, the electrical contact may disturb the resonance. So, to reduce the impact of the electric connections, we have used the setup shown in **Figure IV.4a**. This setup does not require the soldering (avoiding heat soldering) and the connections are taken at the center of the resonator, at the neutral axe. As shown, we have used a spring contact from the top with a low pressure applied to not disturb the electric model.



Figure IV.4. (a) Setup for the measurement, (b) Experimental impedance of the PR.

#### IV.3 Circuit Design

To validate the operating principle and to quantify the performances of the dc-dc converter based on PR, an actual circuit is proposed in this part. The switches S3 to S6 shown in **Figure IV.1b** operate as a synchronous rectifier which are suited for reducing the losses. So, these switches can be replaced by diodes. **Figure IV.5** shows the converter topology where the switches S3 to S6 are replaced by D1 to D4. This topology enables reducing the number of controlled switches, which simplifies the experimental verification, as only two command signals are required but that degrades the efficiency.



Figure IV.5. The converter topology.

Considering the topology shown in Figure IV.5 and the voltage waveforms of  $V_P$ ,  $V_{P+}$  and  $V_P$ - illustrated in Figure IV.6, we deduce the voltage constraint on the switches. In addition, as we aim to quantify the losses in the material for exhibiting its performances, the switches are selected with minimum conduction losses (on state resistance  $\langle R_P \rangle$ ). The TABLE IV.2 summarizes the electrical constrains on the switches.



Figure IV.6. Simulated waveforms in time-domain:  $V_{in}$ =120V and  $V_{out}$ =48V.

TABLE IV.2. Electrical constraints of switches.						
Component	Losses					
S1 and S2	$V_{in}$	$R_{dson} < 100 m \Omega$				
D4 and D3	V <sub>out</sub>	$V_{\rm f} {<} 500 {\rm mV}$				
D1 and D2	V <sub>in</sub>	$V_{\rm f}$ < 500mV				

Therefore, we have built the prototype shown in Figure IV.7. The 10 x 5 cm board is fabricated with a two layers  $35\mu m$  PCB. The switches S1 and S2 are GaN high electron mobility transistors (HEMT) from GaN System, and D1-D4 are ultra-fast diodes.



Figure IV.7. Photograph of the prototype.

The part components are shown in **TABLE IV.3**. The transistors are controlled by isolated gate drivers, where each gate driver is supplied by an isolated power supply that enables having +6V for on state and -3 V for off state on the gate. The PR is connected at its neutral axe by using SMD contract ( $R_{smd} = 40 \text{ m}\Omega$ ) at the bottom and spring contact ( $R_{spring\_contact} = 40 \text{ m}\Omega$ ) at the top of the PR, the mechanical connections of PR are similar to the one used during the characterization, thus having the same behavior.

TABLE IV.3. Key part components.						
Component	Ref	Voltage/ current	Electrical characteristics			
S1 and S2	GaN 66508B	650 V, 30 A	$R_{dson} = 50 \text{ m}\Omega @T=25 \degree C$			
D4 and D3	US1G	400 V, 1 A	$V_{f} = 485 \text{mV} @T = 25 \text{ °C}$			
D1 and D2	US1G	400 V, 1 A.	$V_{\rm f} = 485 {\rm mV}$ @ T = 25 °C			
Gate driver	SI8721	$V_{GS} = +6 \text{ V}/-3 \text{ V}$	$Rg_{on/off} = 10 \Omega$			

#### IV.4 Experimental results

In this part, we illustrate the performances of the piezo based dc-dc converter through various voltage and power conditions. Also, parallelization of PRs is investigated for increasing the power. In addition, we employ the thickness mode operation for high frequency operation 1MHz, while the current density is measured over 3-PRs (three different diameters) at the same frequency operation (thickness = 2 mm). The setup used for the measurement is shown in **Figure IV.8**. The duty cycles of S1 and S2 are generated by using the signal generator AFG 3011C. These duty cycles are pre-calculated (by using the analytical model shown in the previous chapter) at the central frequency, and then tuned while varying the frequency between the resonant and anti-resonant frequency. As illustrated in **Figure IV.8**, the efficiency is measured between the output and the input by using two-power analyzers HMC8015, without taking into consideration the power consumption of the gate drivers that was estimated at 0.5 W @ 100kHz.



Figure IV.8. Setup used for the experimental validation.

#### **IV.4.1** Waveforms

In this part, we exhibit the waveforms through various operating points, showing how the stages evolved by varying the input voltage, the output voltage and the power.

#### a. Constant Load.

Figure IV.9 validates the operating principle of the dc-dc converter based on PR presented in the previous chapter. Indeed, Figure IV.9a-c illustrates the waveforms evolution of the voltage { $V_p$ ,  $V_{p+}$ ,  $V_{p-}$ } and the current  $i_P$ , for an input voltage  $V_{in} = 100$ , 150 and 200 V, a constant output voltage  $V_{out} = 48$  V and a power  $P_{out} = 10$  W.

These waveforms illustrate the evolution of the conversion cycle for various input voltages. It shows that the converter can operate on a wide range of input voltage from 100 V (2 x  $V_{out}$ ) up to 200 V (4 x  $V_{out}$ ). As a result, such a converter can be placed next to a 110  $V_{RMS}$  AC rectifier for instance with a large voltage range capability which reduces the need for a large input filtering capacitor.

As shown on Figure IV.9a, for a gain ratio approaching  $V_{out}/V_{in}=0.5$ , the stage  $V_{in}-V_{out}$  equals the stage when  $V_p = V_{out}$ . So, the charge stored during stage  $V_{in}-V_{out}$  is equal to the charge transferred to load during the stage  $V_{out}$ . Therefore, in this case, the third stage  $V_p = -V_{out}$  is not required, and the conversion cycle operates with only two connected stages.

However, by decreasing the gain ratio, the stage  $V_{in}$ - $V_{out}$  becomes higher than the stage  $V_{out}$ , so, in this case, the third stage  $V_p$ = - $V_{out}$  is needed for balancing the charge. In addition, the third stage's time duration increased by decreasing the gain ratio, as illustrated throughout the **Figure IV.9b** to **Figure IV.9c**. Furthermore, we note that the time duration of the connected stage decreases by increasing the input voltage, while the open-stage duration increases. Indeed, the voltage needs to go from  $V_{in}$  to - $V_{out}$  before going back to  $V_{out}$ . So, by increasing  $V_{in}$ , the time duration of open-stages increases to let  $V_P$  evolving by charging and discharging the capacitance  $C_P$ .



(a):  $V_{in} = 100 \text{ V}$ ,  $V_{out} = 48 \text{ V}$ ,  $P_{out} = 10 \text{ W}$ , f = 92.17 kHz,  $\eta = 95.5\%$ .

(b):  $V_{in}$ =150 V,  $V_{out}$ =48 V,  $P_{out}$ =10 W, f=96.74 kHz,  $\eta$ =92.6%.



Figure IV.9. Experimental waveforms in the time-domain for  $V_{out} = 48$  V,  $P_{out} = 10$  W and input voltage: (a)  $V_{in} = 100$  V, (b)  $V_{in} = 150$  V, (c)  $V_{in} = 200$  V.

#### b. Fixed voltages: Vin and Vout

Figure IV.10 shows the evolution of  $V_p$ ,  $V_{p^+}$ ,  $V_{p^-}$  and  $i_p$  while the input voltage  $V_{in} = 200$  V and the output voltage  $V_{out} = 66.7$  V (G = 0.3). The output power varies from 6 to 16 W (Figure IV.10a to Figure IV.10c).

For a low power (Figure IV.10a), the amplitude of current *I* is low, and the time duration of the connected stage is low, as the charge exchanged is low. However, by increasing the output power up to 16 W (Figure IV.10a to Figure IV.10c), the time duration of connected stage increases and the current amplitude increases as well. In this case, the charge transfer is high.

The amplitude of current *I* at  $P_{out} = 16$  W estimated by the waveforms shown in Figure IV.10c is about 0.85 A, and by using (IV.4.1) solved at the same condition, the amplitude of the current obtained is 0.728 A. This calculated value is lower than the experimental one, which is expected as the losses are not taken into consideration in (IV.4.1), and the circulating current  $I_{circulating}$  does not include the parasitic capacitance of the switches (C<sub>P</sub> + C<sub>oss</sub>), which should lead to a higher  $I_{circulating}$ . By including losses and the parasitic capacitance C<sub>oss</sub> in the model, a better accuracy of the current can be given.

$$I = I_{utile} + I_{circulating} = \frac{\pi P_{out}}{2V_{out}} + \frac{V_{in} + V_{out}}{2}C_P\omega$$
(IV.4.1)

Therefore, regarding how the waveforms evolved at various loads, as it is depending on time duration of the connected stage and the open stage, a control law can be deduced for ensuring the energy and charge balance. In addition, we note that the frequency decreases from 100.08 kHz to 96.56 kHz, while the output power increases. This frequency variation should be taken into account in the control law; for low power, the frequency operation is approaching the anti-resonant frequency of the PR, and by increasing the output power toward the full power, the operating frequency decreased up to the series resonant frequency.



(a):  $V_{in}$ =200 V,  $V_{out}$ =66.7 V,  $P_{out}$ =6 W, f=100.08 kHz,  $\eta$ =92.6%

(b):  $V_{in} = 200 \text{ V}, V_{out} = 66.7 \text{ V}, P_{out} = 10 \text{ W}, f = 98.54 \text{ kHz}, \eta = 94.08\%$ .





Figure IV.10. Experimental waveforms in time-domain for  $V_{in} = 200 \text{ V}$ ,  $V_{out} = 66.7 \text{ V}$  and for output power: (a)  $P_{out} = 6 \text{ W}$ , (b)  $P_{out} = 10 \text{ W}$ , (c)  $P_{out} = 16 \text{ W}$ .

The experimental waveforms are in good agreement with the theoretical waveforms, also, the influence of the timing as function of the power and voltage on the conversion cycle enables to determine thereafter the control strategy for a close-loop control.

#### IV.4.2 Frequency operation

Figure IV.11 shows the output power as a function of the frequency over various gain values. This figure illustrates how frequency evolves with the power. We note that the tendency is the same for each gain ratio, and the curves are shifted down for lower gain. While, the PR operates in free oscillation, the operating frequency evolves regarding the operating condition in terms of voltage and power.

As mentionned in the previous section, the amplitude of the oscillation increases when the frequency is approaching the resonant frequency, leading to high power transfer. At the opposite, when the frequency is near the anti-resonant frequency, the amplitude of the oscillation decreases and the power decreases as well.

Indeed, for low power operation, the time duration of open stages is preponderant, which means that the frequency is defined by L-(C//C<sub>P</sub>) for major part of conversion cycle. Although, by increasing the power conversion, the time duration of connected stage becomes preponderant leading to operating frequency near the resonant frequency defined by L-C.



Figure IV.11. Output Power vs Frequency, for  $V_{in} = 150$  V and G=0.4, 0.33, 0.25 and 0.1667.

Figure IV.12 illustrates the evolution of frequency as a function of the voltage gain for output voltage  $V_{out} = 48$  V. As shown, by increasing the gain, the operating frequency decreases leading to high amplitude of *I* for a constant load (P<sub>out</sub> and V<sub>out</sub> are constants). Indeed, by increasing the gap between the input and output voltages, the amplitude of the current *I*<sub>circulating</sub> required to charge/discharge C<sub>P</sub> increases as well (IV.4.2). So, the proportion of open-circuit time increases and making the frequency approaching the anti-resonant frequency.

$$I_{circulating} = \frac{(V_{in} + V_{out}) * C_P \omega}{2}$$
(IV.4.2)

Also, in the case of increasing the output power from  $P_{out} = 2$  to 10 W, the frequency decreases, as in this case the time-duration of the connected stage increases and the conversion cycle operates under the resonant frequency L-C.

Furthermore, as shown in Figure IV.12, for some cases the frequency is lower for low gain than for high gain at the same output power, as in these cases spurious mode are excited, leading to increase losses. Therefore, to satisfy the output power, the conversion cycle operates at lower frequency closer to the resonant frequency to compensate losses by increasing *I*.



Figure IV.12. Gain Vs Frequency for  $P_{out} = 2$  to 10 W.

#### IV.4.3 Efficiency

In this part, the efficiency of the converter is evaluated experimentally. The measurements take into account the losses of the PR and of the switches; the power supply of the gate drivers is omitted since the power supply is not optimized. However, we have measured its value to 1.1W@5Vdc.

Figure IV.13 to Figure IV.15 show the efficiency as a function of the output power over various gain levels for g < 0.5. The efficiency of the converter increases with the gain ratio and the input voltage (IV.4.3), even though the circulating current increases because it remains very low compared to the useful current. This leads to an efficiency which is mainly related to the current.

$$I = \frac{\pi}{2} \frac{P_{out}}{gV_{in}} + V_{in} \frac{(1+g) * C_P \omega}{2}$$
(IV.4.3)

Indeed, for the same current  $I_{out}$  ( $\frac{P_{out}}{V_{out}}$ ), higher power and efficiency are obtained by increasing the output voltage, since the power losses of the switches and the PR remains constant ( $P_{loss} \alpha I^2$ ). Also, at the same efficiency, higher output power is obtained which also validates that the efficiency is mainly depending on the current (omitting dielectric losses).



Figure IV.13. Efficiency vs output power for gain G = 0.48 and for different input voltages.



Figure IV.14. Efficiency vs output power for gain G = 0.33 and for different input voltages.



Figure IV.15. Efficiency vs output power for gain G = 0.167 and for different input voltages.

Figure IV.16 illustrates the evolution of the efficiency as a function of the power, for an output voltage of 48 V, for various gain ratios. As shown, by decreasing the gain (i.e., increasing the input voltage in this case) while maintaining the output voltage constant, the efficiency decreases, as the part of the circulating current  $I_{circulating}$  increases with (V<sub>in</sub>+V<sub>out</sub>) leading to higher amplitude of the current *I* at same output power, leading to increase the loss by  $I^2$ .



Figure IV.16. Efficiency Vs. Output power for  $V_{out} = 48$  V.

#### **IV.4.4** Loss Distribution

In Figure IV.17, we have estimated the losses of each power components for  $V_{in} = 250$  V, g = 0.33 and  $P_{out} = 25$  W using the experimental results , while comparing this estimation with the analytical model and simulation.



Figure IV.17. Loss distribution for:  $V_{in} = 250$  V, g = 0.33 and  $P_{out} = 25$  W  $\pm$  10 %.

For the analytical model, the conduction losses of the switches S1 and S2 are obtained by computing  $0.5R_{dson}I_{Seff}^2$  with  $I_{Seff}$  the RMS current flowing through the switch. Regarding to diodes, their conduction losses are determined by computing  $I_DV_f$ , where  $I_D$  is the mean current flowing through the diode and  $V_f$  the forward voltage. Furthermore, for the experimental results, the losses are calculated by using the experimental waveforms.

However, the PR loss are deduced by subtracting the losses of semiconductors from the total losses, since we do not have fully access to the current i (as we can measure i only during conduction stage).

For the simulation results, the losses are obtained directly from Spice model for each power components.

As shown in **Figure IV.17**, the estimated losses obtained from analytical model and simulation match with the experimental losses with a good accuracy for the semiconductor components. However, the PR provides higher losses in experimental results due to spurious modes excitation, which induces a significant amplitude increase of current *I* in the PR. Also, the effect of the spurious modes increases the losses in the semiconductors, however, as the losses in the switches are low the effect of spurious modes is barely noticeable.

Figure IV.18 shows the thermal image of the prototype at full amplitude of current I ( $I \approx 1$  A), where the hottest areas show the components having the highest losses. This thermal image is obtained after we have blacked the circuit for having emissivity near 1, and then inserted in box at room temperature and without cooling.

As shown, the diodes and the PR provide the major losses of the prototype. A peak temperature of 58.8 °C is achieved at the center of the PR, as all the current of the PR is flowing at the center of the PR through the electric contacts, as shown in **Figure IV.7**. Also, this thermal image is a good illustration of the distribution of the losses and going in the direction of the loss estimation in each component of **Figure IV.17** 



Figure IV.18. Thermal image of the prototype at V<sub>in</sub>=250 V, g=0.33 and P<sub>out</sub>= 25 W  $\pm$  10 % and  $I \approx 1$  A,  $\Delta T = 28 \ ^{\circ}C$ .

#### IV.4.5 Parallelization of PRs

In this part, we have used 3-PRs connected in parallel in order to increase the output power and to illustrate the scaling of power with the global piezoelectric area. The PRs have the same geometry: a disk shape with a diameter of 25 mm and a thickness of 0.75mm. TABLE IV.4 shows the equivalent model parameters of each PR. A deviation of the resonant frequencies can be noted.

TABLE IV.4. Equivalent model of 3-PRs in radial mode vibration.								
Parameters	L	С	R <sub>P</sub>	CP	fr			
PR1	1.1 mH	2.9 nF	0.548 Ω	8.4nF±10%	89.1kHz			
PR2	1.1 mH	2.824 nF	0.506 Ω	8.35nF±10%	90.01KHz			
PR3	1.1 mH	2.925 nF	0.501 Ω	8.38nF±10%	88.72kHz			

**Figure IV.19** shows the waveforms of the voltage across PRs and the currents flowing through the PRs. As expected, higher output power is achieved by increasing the number of PR and then the global piezoelectric area of the PR. A power of 25 W is reached by using 2 PRs, since by using a single PR only 16 W is reached.

However, as the PRs have not the same resonant frequency, the amplitude of the current induced in each resonator is different, as both resonators are excited at the same operating frequency. As shown in Figure IV.19, PR1 has a lower resonant frequency than PR2. Then, at same operating frequency, PR2 is closer to its resonant frequency than PR1 and it induces higher current amplitude in PR1 than in PR2. Also, to equilibrate the voltage between both resonators placed in parallel, a circulating current during open-stage between PR1 and PR2 is induced.



Figure IV.19. Experimental waveforms of 2-PR for: Vin=120V, Vout=48V and Pout=25 W.

In addition, Figure IV.20 shows the case of using 3-PRs that enables to reach an output power of 38 W. This figure also shows a circulating current between resonators during open stage. Thus, parallelizing the PRs is an easy way to increase the output power, but, since the resonators are not perfectly identical, it induces a current circulation during open stage between the PRs.



Figure IV.20. Experimental waveforms of 3-PR for: Vin=120V, Vout=48V and Pout=38 W.

In Figure IV.21, we have plotted the efficiency as a function of the output power for 1-PR to 3-PRs. As illustrated, by increasing the number of resonators, the output power increases. However, at the same output power, the efficiency falls since there is a current exchange between PRs to balance the voltages between resonators leading to increase the losses by  $I^2$ . Also, as we have 3-PRs, the equivalent parallel capacitance becomes three times higher  $3C_P$ , so, the circulating current increases as well.



Figure IV.21. Efficiency Vs. Output power for V<sub>in</sub>=120 V and V<sub>out</sub>= 48 V.

#### IV.4.6 Thickness mode operation

TABLE IV.5 shows the BVD equivalent circuit in thickness mode vibration of three PRs having various diameters (12, 25 and 40 mm). The PRs are selected in order to operate at the same resonant frequency, which is 1 MHz. Therefore, the thickness is deduced by using (IV.2.11) and it is equal to 2 mm. The various diameters are to evaluate the dependency of the power with the piezoelectric material area.

	TABLE IV.5. BVD circuit of 3-PRs in thickness mode vibration for C-213.									
	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$								k <sub>t</sub> (%)	
PR1	12	2	133	0.17	0.775	7.4	1.04	200	42.7	
PR2	25	2	34	0.735	3.3	0.39	1.049	500	43	
PR3	40	2	11.7	2.01	8.44	0.5	1.038	300	45	

However, due to spurious modes, the inductive region is highly disturbed, which limits the operating frequency range, as shown in Figure IV.22. Therefore, the experimental results are provided near the resonant frequency where the output power is higher.



Figure IV.22. Impedance plot in inductive region for the resonator with D=25mm and Th=2mm.

Also, for the biggest power values (> 50 W), measurements are taken within few minutes, before thermal stability, as the temperature may reach 100°C which causes a depolarization of the resonator, since, the Curie temperature is near 320°C and the supplier recommends not exceeding 1/3 of curie temperature. In addition, the BVD model depending on the temperature, the duty cycles should be adjusted consequently. The results are provided in open loop operation.

**Figure IV.23** shows the waveforms of the PR1's voltage and current in the thickness mode vibration. As illustrated, the switching sequence used is { $V_{in}-V_{out}$ ,  $V_{out}$ ,  $-V_{out}$ }, the soft charging stages and the connected stages at 1 MHz operation appear clearly. The current amplitude is estimated to 1.41 A by using (IV.4.4), where the useful current is 0.785 A and the circulating current part is 0.633 A. This current amplitude of *I*=1.41 A reached near the resonant frequency, is close to the maximum current reachable with this material (C-213) @ 1MHz, it corresponds to a current density of 1.2 A/cm<sup>2</sup>. The circulating current *I*<sub>circulating</sub> increases linearly with frequency, as shown in I.4.2. At high frequency operation, this part becomes significant, limiting the useful current *I*<sub>useful</sub> part and then the output current.

$$I = \frac{\pi}{2}I_{out} + \frac{V_{in} + V_{out}}{2}C_P\omega = I_{useful} + I_{circulating}$$
(IV.4.4)



Figure IV.23. Experimental voltage and current waveforms of PR1 for:  $V_{in}=200$  V,  $V_{out}=60$  V, f=1.086 MHz and  $P_{out}=30$  W±10%.

Figure IV.24 shows the experimentals waveforms for PR2 and PR3 at the same operating frequency @1.086 MHz. As shown, the amplitude of the current increases by increasing the diameter of the resonator. Indeed, an amplitude of 5.3 A is obtained for D =25 mm while 10.5 A is reached for a disk of diameter D = 40 mm at the same operating conditions.





Figure IV.24. Experimental voltage and current waveforms for PR2 and PR3  $V_{in} = 200 V$ ,  $V_{out} = 60 V$ , f = 1.086 MHz: (a)  $P_{out} = 100 W \pm 10\%$  (b)  $P_{out} = 138 W \pm 10\%$ .

In Figure IV.25, the efficiency is plotted as a function of the output power for the three resonators cited in TABLE IV.5. Due to spurious modes in the inductive region, the operating frequency range is limited, which is focused mainly close to the resonant frequency. Therefore, the lower power operation cannot be achieved.

As illustrated Figure IV.25, the efficiency is lower (< 85%) than expected (> 94%), since the experimental quality factor is damaged by the damping induced by the electrical connection shown in Figure IV.7. The experimental quality factor is about 500 while the theoretical value given by the datasheet C-213 is 2500.



Figure IV.25. Efficiency Vs. Output power for Vin=200 V and Vout=60 V.

Futhermore, at this operating frequency, the circulating current becomes significant  $(\frac{V_{in}+V_{out}}{2}C_P\omega)$ , which increases considerably the current amplitude *I* and then the losses  $(0.5R_p.I^2)$ . For instance, the circulationg current to charge/discharge the capacitance C<sub>P</sub> of PR3 is of 6.9 A for input-output voltage of 200-60 V. Nevertheless, a higher ouput power is reacheable at higher frequency, an output power of 175 W was reached, with an efficiency of 80 %. An improvement of the electrical contacts should be carried out to increase the quality factor of the setup.

In conclusion, in thickness mode, the thickness defines the operating frequency while the surface defines the maximal current amplitude value *I*, the maximal current density being about
1.2A/cm<sup>2</sup>. The piezoelectric material surface should be well-sized compare to the need in terms of output current  $I_{out}$ . A downsizing inducing an over heat and an oversizing inducing a bigger capacitance  $C_p$  and then a higher circulating current inducing extra loss.

# IV.4.1 Thickness Vs radial mode vibration

In this part, we compare the thickness mode with the radial mode vibration by considering the same resonator. For that, we have taken a PR with D = 25 mm and th = 2 mm, the equivalent model for each vibration mode are shown in TABLE IV.6.

TABLE IV.6. BVD circuit of a PR with D = $25$ mm and th = $2$ mm.							
Vibration mode	L	С	$R_P$	$C_P$	fr	Q	k
Radial	2.7mH	1.19nF	1.087 <b>Ω</b>	3.3nF	88.8kHz	1387	0.51
Thickness	32µН	0.72nF	0.2049Ω	3.3nF	1.051MHz	1026	0.42

This comparison aims to determine the maximum reachable current density for each resonant mode, at same operating conditions  $V_{in}$  and  $V_{out}$ . Also, for achieving these current densities, the operating frequency for each vibration mode is selected to be near the resonant frequency. Indeed, **Figure IV.26** shows the measured waveforms for the radial and thickness modes, for an input-output voltage of 200-60 V.

For the radial mode at f = 91 kHz, we have measured an output power of 22 W, and an estimated current density of 0.2 A/cm<sup>2</sup> in the PR. For thickness mode that operates at 1 MHz, the output power measured is 100 W and a current density about 1 A/cm<sup>2</sup>. From these results, increasing the frequency by a factor 10, the power and current density are increased by a factor 5.

It can be noted that for the waveforms measured in radial mode, the time-duration of the connected stages is dominant compared to the open circuit stages used for charging/discharging  $C_P$ . One can deduce that the useful current amplitude is higher than the circulating current.

However, for the thickness mode, as shown in Figure IV.26, the time-duration of connected stage is lower than the open-circuit, and the current is pulsed during the connected stages. The amplitude of the circulating is at least comparable to the useful current.



(a): 
$$V_{in} = 200 V$$
,  $V_{out} = 60 V$ ,  $f = 91 kHz$ ,  $P_{out} = 22 W$ ,  $\eta = 90 \%$ 

(b) :  $V_{in} = 200 V$ ,  $V_{out} = 60 V$ , f = 1.08 MHz,  $P_{out} = 100 W \eta = 90 \%$ 



Figure IV.26.Waveform of voltage and current of PR near resonant frequency for: (a) radial mode, (b) thickness mode.

In TABLE IV.7, we have estimated  $I_{circulating}$ ,  $I_{useful}$  and I by using (IV.4.3) for the radial and thickness mode. As shown, by increasing the frequency, the circulating current becomes significant, which is increasing the amplitude I. Also, as  $I_{circulating}$  is only used for charging/discharging  $C_P$ , this amplitude induces losses even without load. So, having a high  $I_{circulating}$  reduces the efficiency, especially at low power operations. Thus, the design of the PR should consider the ratio between  $I_{circulating}$  and  $I_{useful}$ . A simple solution for keeping a high efficiency operation over wide power range consists of parallelizing the PRs as a function of power segments.

TABLE IV.7. Current Vs Frequency: $V_{in}=200 \text{ V}$ , $V_{out}=60 \text{ V}$ and $C_P=3.3 \text{ nF}$ .				
Value	Radial mode F = 91  kHz	Thickness mode $F = 1.08$ MHz		
$I_{circulating} = \frac{(V_{in} + V_{out})2\pi f C_p}{2}$	0.273 A	2.73 A		
$I_{useful} = \frac{\pi}{2} I_{out}$	0.6 A	2.62 A		
Ι	0.9 A	5.4 A		

#### IV.5 Inductor Vs. PR

In this part, we propose a simple comparison between an inductor L (magnetic energy) and a PR having the same inductive value L between its resonant and anti-resonant frequencies. Therefore, we compare the energy stored per unit volume between the mechanical ( $E_{PR}$ ) and magnetic storage ( $E_L$ ).

To do so, we have taken as an example a PR with diameter of 25 mm and thickness of 0.75 mm. In addition, we take the amplitude of the ac current for PR (I=1 A determined experimentally) and a resonant frequency around 100 kHz. This PR provides:

$$L = 1.1 \text{ mH}, E_{PR} = \frac{1}{2} L I_{PR}^2 = 0.55 \text{ mJ} \text{ and Volume} = 0.368 \text{ cm}^3, R_P = 0.5 \Omega$$

Hence, we come up with a commercial inductor referenced by MSS1210-105KED (we try our best to keep the volume of L as low as possible while having a high Q factor) that gives the same energy stored and same inductance value L:

$$L = 1 mH$$
,  $E_L = \frac{1}{2} L I_L^2 = 0.5 \text{ mJ}$  and Volume = 1.513 cm3,  $R_{dc} = 0.906 \Omega$ 

The PR volume is about four times smaller than that of the inductor and power losses are lower thanks to its higher quality factor. In addition, PR offers a planar shape easier for implementation in thin devices (th = 0.75 mm). Still, at this frequency, the inductor remains competitive compared to PR.

However, by using thickness mode vibration at 1 MHz, and considering a PR with D=25mm and th=2mm used in part IV.4.1, it sustains an amplitude of current of 5.6 A and:

$$L = 32 \ \mu H$$
,  $E_{PR} = \frac{1}{2} L I_{PR}^2 = 0.466 \text{ mJ}$  and Volume = 0.98 cm<sup>3</sup>,  $R_P = 0.2 \Omega$ 

At this operating frequency, it is hard to find a commercial inductance with a comparable energy stored and volume. Nevertheless, by taking for instance, the inductor ref. 33330C (Q=3.5@1MHz) sustaining an ac current of  $I_L = 4.2 A$ , and:

$$L = 33 \ \mu H$$
,  $E_L = \frac{1}{2} L I_L^2 = 0.29 \text{ mJ}$  and Volume = 14.6 cm<sup>3</sup>,  $R_{dc} = 0.04 \ \Omega$ 

As shown, this inductor is able to store less energy, and its volume is more than 10 times bigger while having a poor quality factor of Q = 3.5 (compared to PR Q > 1000). Thus, by increasing the frequency, the miniaturization of the inductors becomes difficult, since we have to take into account winding losses, cores losses and size limitations [3], while in counterpart the miniaturization of the PR is easier;

# IV.6 Summary and discussion

This Chapter has shown the experimental validation of the operating principle of our power converter based on PR. The BVD model of the PR is presented as a function of the physical and geometrical parameters for radial and thickness vibration modes. The presented models enable to design a PR as a function of the desired parameters such as frequency, input/output voltages and output current.

Then, we have designed a dc-dc prototype with our proposed converter topology for a conversion gain  $V_{out}/V_{in} < 0.5$ . The experimental voltage and current waveforms have been presented at various operating points. These waveforms have shown the reliance of the operating conditions with the time-duration of each stage of the conversion cycle. Indeed, for high power rate, the time-duration of the connected stages is preponderant, while the time

duration of the open stages becomes preponderant at low power rate. This reliance appears again in the output power vs. operating frequency relation.

The presented power converter performs a high efficiency, which illustrates the potential of this PR based converter. Indeed, this power converter exhibits an efficiency higher than 85 % over a wide range of power and voltage. Also, a peak output power of 50 W is reached for input-output voltage of 250-117 V with an efficiency up to 94 %. Moreover, a higher efficiency is expected by using a synchronous rectifier, as the main losses of the semiconductors are located in the diodes. However, the challenging part of synchronous rectifier is the control, which should be optimized to ensure ZVS operation.

A potential of increasing the output power is investigated by employing several parallel PRs or by increasing the operating frequency. Indeed, the use of parallel resonators is an easy way to increase the output power. However, a small dispersion between resonators parameters induces a circulating current between resonators to balance the voltages; this circulating current increases the losses, limiting thus the scaling of the output power and reducing the efficiency. Operating at a higher frequency of 1 MHz has been demonstrated, it exhibits a higher output power, and a higher current and power density.

Indeed, at 1MHz operation, an output power exceeding 100 W was reached for a PR volume of 0.98 cm<sup>3</sup>, with an efficiency up to 80 %. However, a cooling system is required for long-term operation, since a temperature of 100°C is reached. Furthermore, the mechanical and electrical contact should be considered to reduce the electrical resistance of the connection and to reduce the impact on the mechanical vibrations (damping). Furthermore, we have shown the capability to increase the output power by increasing the area of the resonator.

Avoiding spurious modes remains a serious challenge for designing the PR. As illustrated, the spurious modes provide additional losses: additional high frequency current flows through the switches and some of energy is stored in another mechanical mode and is ultimately dissipated.

# Chapter V: Design and implementation of a control strategy for a piezo-based DC-DC converter

**Abstract**: the aim of the chapter is to design a control strategy for a DC-DC converter based on PR. The different issues for this control are enumerated and exposed for operating with energy and charge balance. Thus, we have proposed a control strategy that has been verified by simulation. Also, an actual circuit has been designed to check the operating of the control in transient and steady-state. Experimental results are exhibited that validated the control strategy.

# Content

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# V.1 Introduction

As demonstrated in previous chapter, DC-DC converter based on piezoelectric resonator enable high efficiency and high power density without using any magnetic components. Therefore, one challenge of such converter is the control, while using simple and low cost components. To our knowledge, the control of such converter remains poorly developed and little studied [24]. In order to be attractive for commercial applications by using a low-cost electronics solution increases the challenge.

Indeed, the conversion cycle using a PR as a storage element operates with six-switching stages, alternating open-circuit stages and constant voltage stages, which is simple but requires a control to ensure:

- Zero voltage switching and soft charging,
- Energy and charge balance,
- Output voltage regulation.

Those criteria make the operation efficient, as it reduces the switching losses while it ensures the output voltage regulation. Therefore, considering these constraints and the need of managing 6 stages, the control becomes difficult as a whole.

Generally, the objective of the control when designing a dc-dc power converter is to regulate the output voltage to a desired constant value. Nevertheless, for a high efficiency operation, the control must ensure the zero-voltage switching of the semiconductors and, in addition in our case, the energy and charge balance, which is more difficult.

In this chapter, we present the design and the implementation of a cost effective control of a PR based DC-DC converter. This control is valid for any switching sequences. The control strategy is validated experimentally.

# V.2 Issues of control

**Figure IV.5** shows the generic conversion cycle, while we identify the key elements of the control. In this figure, we described the optimal control that minimizes the amplitude of the current *i*. This control ensures:

- ZVS,
- Soft charging,

- Load regulation,
- Synchronization with the mechanical movement (zero current crossing detection).



Figure V.1. Generic conversion cycle.

#### V.2.1 ZVS operation

The switching losses are proportional to the frequency, the square of the voltage  $\Delta V$  across the switches before closing, the capacitance of the transistor C<sub>oss</sub>, as given by (V.2.1). The frequency *f* can be selected in order to reduce the volume of passive components. Indeed, increasing the frequency allows to reduce the stored energy per cycle (i.e.,  $E_{cycle}=P/f$ ), that reduces the volume of the passive components. The C<sub>oss</sub> value depends on the technology of transistor (IGBT, MOSFET, HEMT), which is designed regarding the operating conditions *V*, *f* and *P* and the cost. Therefore, minimizing the switching losses can be done by minimizing the voltage across the switches named  $\Delta V$  just before closing the switch (i.e.,  $P_{sw} \alpha \Delta V^2$ ).

$$P_{sw} = \frac{1}{2}C_{oss} * \Delta V^2 * f$$
 (V.2.1)

In Figure V.2, we have illustrated an example of turning ON the switch(es) to achieve the connected stage ( $V_P = V_b$ ) at  $t = t_1$ . In the first case (a): the switch (es) is/are closed after the voltage  $\beta V_P$  crosses the voltage level  $\beta V_b$  since  $t_1 > t_{1opt}$  (too late). In the second case (b): the switch(es) is/are closed before the voltage  $\beta V_P$  reaches the voltage level  $\beta V_b$  as  $t_1 < t_{1opt}$  (too early). In both cases, the turning-ON of the switch(es) provides switching losses. In addition, supplementary losses are provided by the parallel capacitance of the PR (C<sub>P</sub>) which is significantly larger than a switch C<sub>oss</sub> parasitic capacitance (at least 10 times).



Figure V.2. No ZVS operation: (a)  $t_1 > t_{1opt}$ , (b)  $t_1 < t_{1opt}$ .

# V.2.2 Soft charging

In our conversion cycle, the soft charging of  $C_p$  allows to change the  $V_P$  voltage between two successive connected voltage stages in order to achieve ZVS at the next closing of a switch, for instance between stage  $V_P = V_b$  and  $V_P = V_a$ , and between  $V_P = V_c$  and  $V_P = V_b$ . Therefore, the instant t<sub>2</sub> (respectively t<sub>5</sub>') is determined regarding the open stage duration between  $V_b$  and  $V_a$ (respectively  $V_c$  and  $V_b$ ). At same time, t<sub>2</sub> (respectively t<sub>5</sub>') defines the end of the connected stage  $V_b$  (respectively  $V_c$ ). Figure V.3 shows the waveform of voltage  $V_P$  during the open stage between  $V_b$  and  $V_a$ , where the soft charging is not ensured leading to two cases:

- (a)  $t_2 > t_{2opt}$ : in this case the time duration for charging the capacitance  $C_P$  is not sufficient to reach  $V_{zvst3}$  at t=t<sub>3</sub> (at the zero crossing of the current) to ensure the ZVS at t<sub>3</sub>.
- (b) t<sub>2</sub> < t<sub>2opt</sub>: in this case, the ZVS operation is possible, however, the voltage V<sub>P</sub> exceed V<sub>zvst3</sub> or it is clamped to V<sub>zvst3</sub> depending if the switch is closed in ZVS on the first or second V<sub>P</sub> crossing the V<sub>zvst3</sub> voltage value (i.e., while V<sub>P</sub> increases or decreases). In any case, it increases the circulating current. In case of V<sub>P</sub> is briefly clamped to V<sub>zvst3</sub>, it can induce a reverse power flow (reactive power). For the case of the switching sequence {V<sub>in</sub>-V<sub>out</sub>, V<sub>out</sub>, -V<sub>out</sub>}, voltage V<sub>P</sub> is clamped to V<sub>in</sub> + V<sub>f</sub> (V<sub>f</sub>: forward voltage of the intrinsic diode of S<sub>1</sub>). Therefore, if t<sub>2</sub> < t<sub>2opt</sub>, V<sub>p</sub> reaches V<sub>in</sub> +V<sub>f</sub> before t<sub>3</sub>, a part of the stored energy of the PR is then restored to the input source since during this stage the current *i* is negative, as illustrated in Figure V.4. As consequence, the PR operates at higher current amplitude, compare to the optimal case, inducing extra losses.



Figure V.3. Soft charging between  $[t_2, t_3]$ : (a)  $t_2 > t_{2opt}$ , (b)  $t_2 < t_{2opt}$ .

In both cases, the operating conversion is not optimal, since it induces a higher amplitude of current *I* if  $t_2 < t_{2opt}$  leading to higher losses and implying to oversize the PR to achieve the requirements of the conversion, or higher switching losses if  $t_2 > t_{2opt}$ . Therefore, we need to control  $t_2$  in order to let V<sub>P</sub> reaching V<sub>zvst3</sub> in  $t_3$  maximizing by that the efficiency and the power density.



Figure V.4. Reverse power flow during the stage  $V_{in}+V_f$  for  $t_2 < t_{2opt.}$ 

# V.2.3 Synchronization with the current i

As mentioned previously, the operating frequency depends on the load: at high output power, the operating frequency gets closer to the resonant frequency; at lower power, the operating frequency approaches the anti-resonant frequency, as illustrated in Figure V.5. Thus, the control should take into consideration the fact that the frequency moves. In addition, the phase of current i should be known, as the switching sequences are implemented regarding the polarity of i as shown previously. Thus, the phase and the frequency should be determined/measured to implement the control, which acts like a vector control of a rotational electrical machine. In the above section, we present a few methods to measure the phase and frequency of the resonator.



Figure V.5. Power Vs frequency.

# V.2.4 Load control

Equation (III.3.19) gives a direct relation between the output current (or power) and the charge exchange during the connected stage  $[t_3', t_4]$ . Actually, this equation states that the output power is directly depending on the charge exchanged  $Q_a$ . For that reason, we take  $t_4$  as the parameter to control the output current/power. Indeed, increasing the time-duration  $[t_3', t_4]$  increases the charge exchanged with the PR and then the charge transferred to the load. At the opposite, decreasing this time duration decreases the charge transferred to the load.

$$I_{out} = \frac{P_{out}}{V_{out}} = \alpha \frac{Q_a}{T}$$
(V.2.2)

Where  $\alpha = -\left((\alpha_a - \alpha_c) + (\alpha_b - \alpha_c)\frac{V_c - V_a}{V_b - V_c}\right)$  is a constant and depends only on the switching sequence,  $\alpha_a$  takes +1 or -1 if V<sub>a</sub> contains +V<sub>out</sub> or -V<sub>out</sub> respectively, otherwise 0, the same goes for  $\alpha_b$ ,  $\alpha_c$  related to V<sub>b</sub> and V<sub>c</sub>.

#### V.3 Design of the control strategy

The main idea to implement the control is based on sensing the voltage of the PR,  $V_{in}$  and  $V_{out}$  at specific instants of the conversion cycle, then, we use these measurements for achieving the soft-switching, ZVS and load regulation. The information tied to these conditions are processed digitally and implemented in a state machine in order to generate the PWMs synchronized with the mechanical movement thanks to a zero current crossing detection of  $i_p$ .



Figure V.6. Converter circuit.

In this section, we propose to design a control strategy by considering the switching sequence  $\{V_{in}-V_{out}, V_{out}, -V_{out}\}$  with the topology proposed in the previous chapter. In the control design, we consider -the soft charging, -ZVS conditions, -synchronization with *i* -and load regulation. Figure V.6 shows the conversion structure and the key waveforms in steady state operation. Thus, only S1 and S2 are driven. So, for an easy implementation, we consider a passive rectification with diodes, as the losses in the diodes are neglected at high voltage operation.

The connected stages are:

•  $V_P = V_{in} - V_{out}$ : S1 and D4 are turned on during [t<sub>3</sub>', t<sub>4</sub>],

- $V_P = -V_{out}$ : D1 and D4 are 'on' naturally during [t<sub>5</sub>, t<sub>6</sub>],
- $V_P = V_{out}$ : D3, S2 and D2 are in conduction stage during [t<sub>1</sub>, t<sub>2</sub>].

The following design of the converter and the feedback regulation are made for an input voltage of 120 V and an output voltage < 48 V, and output power up to 20 W.



Figure V.7. Waveforms in time-domain for  $V_{in} = 120$  V and  $V_{out} = 48$  V.

# V.3.1 Synchronization with PR's deformation

As the conversion cycle is composed of connected stages and open-circuit stages, current *i* can be measured directly only during the connected stages configurations. Therefore, current *i* cannot be sensed all over the resonant period, which makes it difficult to measure its phase and frequency. So, to determine these quantities, we can use one of the methods shown in TABLE V.1. The advantages and drawbacks of each method are enumerated. Note: the phase and

frequency can be deduced from a simple zero current crossing without requiring the full current waveform.



In the case of the switching sequence illustrated in Figure IV.6, we note that  $V_{P}$ - is equal to  $V_{out}$  when *i* is positive (i.e., the diode D<sub>3</sub> is turning-off), and negative when  $V_{P}$ - is equal to zero (i.e., the diode D<sub>3</sub> is turning-on). So, we can use the conduction state of D<sub>3</sub> to determine the current zero crossing and then the phase of current *i*. Therefore, a single threshold

comparator monitoring the diode voltage can be used to determine the beginning of the resonant period at  $t = t_3$ , as shown in Figure V.7. Figure V.8 shows the voltage  $V_{sync}$  of the zero-crossing comparator. This implementation is simple but it introduces a delay due to the comparator switching time and the filtering. This can be corrected by including a well-tuned compensation in the drive. Then, we can use a PLL to drive the successive operations. The switching sequence and PWM are then implemented starting from the instant  $t = t_3$ .



Figure V.8. Theoretical waveforms of the comparator used for phase/frequency tracking.

The frequency is then determined by counting the number of clock cycles ( $f=f_{clk}/n_{cycle}$ ). Where,  $f_{clk}$  is the clock reference of the control circuit.

# V.3.2 ZVS

The turning-on of S1 is achieved at the beginning of the period, when the voltage  $V_{P}$ + is approaching  $V_{in}$  (i.e.,  $V_{ds}(S1) = V_{in} - V_{P+} \approx 0V$ ), which is trigged on the rising edge of  $V_{sync}$  at t= t<sub>3</sub>, as shown in **Figure V.9**. For S2, the turning-on is achieved when drain-source voltage of S2 is reaching 0V, when  $V_{P}$ + reaches  $V_{out}$  and  $V_{P}$ - reaches 0V (falling-edge of  $V_{sync}$  at t = t<sub>1</sub>), as shown in **Figure V.9**. Therefore,  $V_{sync}$  can trig both ZVS turning-on of S1 and S2, respectively at t<sub>3</sub> and t<sub>1</sub>, as illustrated in **Figure V.9**. Indeed, the rising-edge of  $V_{sync}$  is used to turn-on S1, and the falling-edge is used to turn-on S2 at the starting of the connected stage  $V_P=V_{P+}-V_{P-}=V_{out}$ .



Figure V.9. Theoretical waveforms for ZVS control of S1/S2.

#### V.3.3 Soft charging

The time duration of the stage  $V_P = V_{out}$  is controlled by turning off S2 at t =t<sub>2</sub>. This instant t<sub>2</sub> is used to regulate the charge balance. This means that the instant t = t<sub>2</sub> should be controlled by a closed loop in order to let  $V_P$  reach the voltage level  $V_{in}$  at the half of the resonant period. Indeed, if the instant t<sub>2</sub> > t<sub>2opt</sub>, then  $V_P$  cannot reach  $V_{in}$  at t<sub>3</sub> and S1 cannot be turned-on with ZVS condition. In other hand, if t<sub>2</sub> < t<sub>2opt</sub>, then  $V_P$  reaches  $V_{in}$  before t<sub>3</sub>, so S1 can be turned-on with ZVS at t = t<sub>3</sub>. However, the reverse diode of S1 is turned-on and a part of the stored energy in the resonant or is restored to the input source through the reverse diode of S1 and D4. In both cases, the efficiency of the converter is reduced. Therefore, to regulate the t<sub>2</sub> value, we can use a simple comparator to compare voltage  $V_{P+}$  with  $V_{in}$ . In this case, we use  $V_{P+}$  as it is the image of  $V_P$ , since  $V_{P+}$  is referenced to the ground, avoiding a differential measurement of  $V_P$ . The result of the comparison at t = t<sub>3</sub> is then used to increase or decrease t<sub>2</sub> for the next resonant period.



Figure V.10. Schematic diagram for the comparator at t=t<sub>3</sub>.

$$\begin{cases} if V_{P+} > (V_{in} - V_{offset}) at t = t_3 \rightarrow t_2((n+1)T) = t_2(nT) + \Delta t \\ if V_{P+} < (V_{in} - V_{offset}) at t = t_3 \rightarrow t_2((n+1)T) = t_2(nT) - \Delta t \end{cases}$$
(V.3.1)

 $V_{offset}$  is the precision of the controller, and should be as small as possible since the switching losses of S1 are depending on this value (i.e.,  $P_{sw}(S1)=1/2C_{iss}V_{offset}^2f$ ), as illustrated in Figure V.11.  $\Delta t$  is the incremental step of t<sub>2</sub>. The implementation of this regulation is simple but it can take several periods to converge depending on  $\Delta t$  value.



Figure V.11. Operating principle of the regulation of  $t_2$ : (a)  $t_2 < t_{2opt}$ , (b)  $t_2 > t_{2opt}$ .

# V.3.4 Output voltage regulation

As illustrated in equation (V.2.2), the output power is mainly linked to the stored energy in the PR during the stage  $V_P=V_a$  (= $V_{in}-V_{out}$  in this case), which is the time duration of [t<sub>3</sub>',t<sub>4</sub>]. From the generic representation, the instant t<sub>4</sub> for the switching sequence { $V_a=V_{in}-V_{out}$ ,  $V_b=V_{out}$ ,  $V_c=-V_{out}$ } is written as a function of the electrical parameters (for lossless resonator:  $R_P=0$ ):

$$\cos \omega t_4 = 1 - \frac{4V_{out}}{V_{in}} + \frac{V_{out}C_P\omega}{I} \left(1 + \frac{2V_{out}}{V_{in}}\right)$$
(V.3.2)

The output load is modeled as a resistor  $R_L$  in parallel with an output capacitance  $C_{out}$  as illustrated in Figure V.12. We consider that  $C_{out}$  is sufficiently high for filtering the high frequency current ripple on the output voltage, and  $R_L$  is depending on the desirable output power. Therefore, by using (V.3.2), equation (V.3.3) can be rewritten as a function of  $V_{out}$  by removing *I*.

$$I = \frac{\pi}{2} \frac{V_{out}}{R_L} + \frac{C_P \omega V_{out}}{2} \left(1 + \frac{V_{in}}{V_{out}}\right)$$
(V.3.3)



Figure V.12. Output load model.

Thus, equation (V.3.4) gives the relation between t<sub>4</sub> and V<sub>out</sub>: this expression can be linearized around an operating point for small variations around initial point 0 (by using Taylor series development at first order), where  $t_4 = t_{4_0} + \Delta t_4$  and  $v_{out} = V_{out_0} + \Delta V_{out}$ .

$$\cos \omega t_4 = 1 - \frac{4V_{out}}{V_{in}} + \frac{2\left(1 + 2\frac{V_{out}}{V_{in}}\right)}{1 + \pi C_P \omega / R_L + V_{in} / V_{out}}$$
(V.3.4)

Therefore, by linearizing the equation (V.3.4), one can obtain a relation between  $\Delta t_4$  and  $\Delta V_{out}$  (using Taylor development 1<sup>st</sup> order):

$$-\omega \Delta t_4 * \sin \omega t_{4_0} = -4 \frac{\Delta V_{out}}{V_{in}} + \frac{4 \frac{\Delta V_{out}}{V_{in}}}{1 + \pi C_P \omega / R_L + V_{in} / V_{out0}}$$
(V.3.5)

Then, we deduce the static transfer function H(s) by  $\frac{\Delta V_{out}}{\Delta t_4}$  for a desired operating point. This gain gives a slew rate of the variation of the V<sub>out</sub> when a small change of t<sub>4</sub> occurs, and it is expressed in V/s.

$$\frac{\Delta V_{out}}{\Delta t_4} = \omega \sin \omega t_{4_0} \left( 1 + \frac{1}{\frac{\pi C_P \omega}{R_L} + \frac{V_{in}}{V_{out_0}}} \right)$$

Then, a PI controller can be designed to minimize the transient duration while respecting a maximum overshoot value on the output voltage. Thus, the objective of controlling t<sub>4</sub> is to regulate the output voltage to a constant voltage set point.

# V.4 Simulation with MATLAB

According to the previous assumption, we have used MATLAB-Simulink to implement the control strategy and to check the accuracy and stability of the control. In this simulation, we have used the converter topology and the switching sequence shown in Figure IV.6. Indeed, Figure V.13 shows the dc-dc converter and the PR's model by using the toolbox of Simulink SimScape, the output load used is modeled by a  $(R_L//C_{out})$  circuit. The key electrical parameters are shown in TABLE V.2.



Figure V.13. Converter topology by using toolbox SimScape.

TABLE V.2. Key parameters.			
Parameter	Value		
L	1.1 mH		
R <sub>P</sub>	0.6 Ω		
С	2.9 nF		
CP	8.9 nF		
R <sub>dson</sub>	100 mΩ		
V <sub>f</sub>	0.7 V		
Cout	10 µF		
f	[ <i>f</i> <sub><i>r</i></sub> , <i>f</i> <sub><i>ar</i></sub> ]=[90 kHz, 105 kHz]		
Vin	120 V		
Vout	48 V		

Therefore, considering the previously described control blocks of operating functions (ZVS, soft-charging, synchronization with the movement and load regulation), we have designed each regulation block as follows:

• Load regulation

As mentioned in the previous part, the output voltage is regulated thanks to a feed-back loop on the value of  $t_4$ . In our implementation, we use a PI type corrector in the feed-back loop to stabilize the output voltage. Thus, we have calculated the PI corrector for an overshoot not exceeding 10% and a time response about 1 ms, which is 100 times the resonant period (around 10  $\mu$ s).



Figure V.14. Loop control of the output voltage:  $V_{out ref} = 48 V$ .

• Soft-charging

The soft-charging during the stage  $[t_2, t_3]$  is controlled by  $t_2$  in order to reach  $V_{in}$  at  $t_3$ . Thus, equation (V.3.1) can be implemented as illustrated in Figure V.15, so, the variation of  $t_2$  is achieved through the comparison between  $V_{P+}$  and  $V_{in}$  sampled at  $t_3$  each period. The correction of  $t_2$  is done by steps of  $\pm 10$  ns, which is 1/1000 of the resonant period.



Figure V.15. Soft-charging control for t<sub>2</sub>.

• Synchronization

In simulation, we have access to the current in the RLC branch. Thus, we use the polarity of the motional current to measure the frequency and the phase of the resonator in order to



Figure V.16. Close-loop control in Simulink: green-block for  $V_{out}$  control, yellow-block for soft-charging t=t<sub>2</sub> and bleu-block for the synchronization with the current *i*.

synchronize the PWM of S1 and S2 with the current, at each period. Figure V.16 shows the implemented blocks in Simulink, where each control loop is identified by its inputs and outputs.

# V.5 Simulation Results

Once each block has been designed as illustrated in the previous section, we have implemented the control strategy for an input-output voltage of 120 - 48 V and an output power of 10 W. Figure V.16 shows the close-loop control implemented in Simulink. The pink block contains the DC-DC converter shown Figure V.13, the blue block enables the synchronization with the current *I*, the yellow-block contains the regulation of the soft charging by controlling t<sub>2</sub> and which generates the pulse of S2, the green-block is the block for regulation of the output voltage to it set point through t<sub>4</sub>.

Figure V.17 shows the simulated waveforms during the transient mode. It shows a good regulation of the output voltage to 48 V, with an overshoot not exceeding 7 V. At the beginning, we can observe a delay of 0.58 ms during which the output voltage is close to 6 V. This delay is due to the saturation of the control's parameters. This delay can be avoided by using initial conditions close to the steady state operation. During the transient mode, the amplitude of current *i* is not sufficiently high to charge and discharge the capacitance C<sub>P</sub>, since the extrema of V<sub>P</sub> (low value -V<sub>out</sub>) is not reached, no stage V<sub>P</sub> = -V<sub>out</sub> is visible as observed in Figure V.17. Therefore, to increase the current amplitude *i*, and then the mechanical oscillation amplitude, the PR takes higher energy from the input source than the energy transferred to the output load. So, the conversion cycle operates with a positive energy balance during this regime to increase the mechanical energy and so the current *i* amplitude and at the end the output power. Once, the amplitude of the current becomes significant, the resonator transfers energy to the load and the output voltage increases. Thus, the output voltage reaches the set value 48 V, and the converter operates with energy and charge balance, leading to a constant amplitude of the current in the LCR branch.



Figure V.17. Simulated waveforms during transient-response for :  $V_{in}$ =120 V,  $V_{out}$ = 48 V and  $P_{out}$ =10 W.

Figure V.18 displays the waveforms of the converter during the steady-state operation. Clearly, the  $V_P$  voltage waveform shows that the conversion cycle of our topology fits to the theoretical prediction, where the connected and the open-circuit stages can be observed. The mean value of the output voltage is 48 V, the peak-to-peak value of the output voltage ripple is 180 mV.



Figure V.18. Steady-state waveforms for : V<sub>in</sub>=120 V, V<sub>out</sub>=48 V and P<sub>out</sub>=10 W.

# V.1 Implementation of the control strategy

The control of the dc-dc power converters generally requires a Logic Core that enables to implement the functional algorithms: possible hardware solutions are based on Microcontroller or FPGA. In our case, we have selected a FPGA, as this solution can easily guarantee in one hand a sufficiently flexible development, and in other hand, it can satisfy all the major constraints in terms of timing generation. In addition, it offers the possibility to develop an optimized circuit (low-cost dedicated circuit) such as an ASIC. Figure V.19 depicts the

conception flow in order to generate the configuration file of the FPGA starting from the proposed control algorithm. This enables fast prototyping and implementation.



Figure V.19. Conception flow.

Once, we have validated the simulation of the control strategy, we have instantiated the functional blocks as schematic design, as illustrated in Figure V.20. Indeed, the feedback control is depicted as schematic blocks that shows each control loop parameters. Then, we have programmed the functions using VHDL language. This representation makes it easy to visualize the interactions between the different parameters and enables a fast debugging phase.



Figure V.20. Schematic block of the feedback control in ISE-Xilinx.

# V.2 Circuit design and considerations

In this section, we describe the circuit that we designed for experiments. Beforehand, we list the control parameters with the measurements awaited in order to identify the resources as illustrated in **TABLE V.3**. Then, we deduce the structure of the control circuit as shown in **Figure V.21**. In this case, we have selected the FPGA SPARTAN 3 to implement the control strategy, this FPGA is oversized for our application but it offers the possibility to implement a non-optimized program that may need supplementary resources. In addition, it can operate with a clocking up to 312.5 MHz, allowing a high precision PWM with a step of 3.2 ns.

TABLE V.3. Control parameters.				
Parameters	Resources	Requirements		
t <sub>0</sub>				
t1	Natural conduction D4			
t <sub>2</sub> : soft-charging	Comparator $V_{P^+}$ with $V_{in}$	Bandwidth : >10 MHz		
t <sub>3</sub> : Phase/frequency	Comparator: V <sub>D3</sub>	Bandwidth : >10 MHz		
t <sub>4</sub> : load regulation	ADC : V <sub>out</sub>	Sampling : > 50 KHz		
t5	Natural conduction D1 and D4			
t <sub>6</sub>	2*t <sub>3</sub>			



Figure V.21: Simplified synoptic of the control circuit.

**Figure V.22** shows the circuit with the proposed control schematic. It illustrates an overview of the control strategy. The various measurements used for generating the PWMs are illustrated. A state machine implemented in FPGA is used for generating the PWMs regarding to the timing of the conversion cyle.



Figure V.22: PR-based DC-DC circuit with the proposed control.

**Figure V.23** shows the designed circuits to validate the control feedback. The voltages are sensed by using a voltage divider. These measurements are filtered through first order RC filters to reduce the sensing noise. Also, buffer amplifiers are used for impedance matching. In addition, we used digital isolator ADUM1201 and isolated ADC AMC1204 in order to isolate the control circuit from the power converter. This reduces the EMI noise in the control circuit and it protects the circuit and the users. The sampling of the output voltage is achieved at 78 kHz with a resolution on 14 bits. The PWMs S1 and S2 are generated by the FPGA after calculating the duty cycles, and then transmitted to the isolated gate drivers SI8271. We measured on this board a power consumption of 1 W at 5 V voltage supply that includes also the power supply of the gate drivers operating at 100 kHz. This circuit is designed for a frequency operation around 100 kHz and an output dc-current of 1 A, the selected transistors are STD5NM50T4 for S1-S2 and the diodes are US1G for D1 to D4 in this prototype.



Figure V.23: Picture of the prototype circuits.

# V.3 Experimental verification

The objective of this part is to validate the control strategy of the proposed dc-dc power converter: the transient response and the steady-state operation. Also, the robustness of the control to load variations is also tested. **Figure V.24** shows the setup used to validate the control strategy. The input voltage is generated by a dc source, while the output voltage is emulated by the load resistor  $R_L$  of 230  $\Omega$  for an output power of 10 W at  $V_{out} = 48$  V. Moreover, parallel resistors are added to emulate load variations by connecting and disconnecting them. The input and the output powers are measured to determine the efficiency of the converter. The FPGA is programmed by using ISE 14.1 with JTAG connector.



Figure V.24: Experimental Setup.

# V.3.1 Start-up and Transient response

To illustrate the transient performances, we have fixed the input voltage to 120 V while  $R_L$  is set to 230  $\Omega$ , and  $V_{out}$  to 0 V as  $C_{out}$  is discharged. Then, we have turned on the control circuit. At the beginning, the PWMs are not synchronized with the vibration of the PR (i.e., the current in the LCR branch) and the frequency of the PWMs is initialized to 95 kHz, and the operating frequency range is limited between the resonant and anti-resonant frequencies. This transition enables to increase the output voltage up to 5 V, where, at this threshold voltage, the comparator at t<sub>3</sub> (the center of the resonant period) is activated. Indeed, the comparator at t<sub>3</sub> operates by comparing the voltage V<sub>P</sub>- with zero voltage as shown in **Figure V.8**. So, to measure the phase and the frequency of *I*, we need a minimum amplitude of V<sub>P</sub>-, which is obtained when V<sub>out</sub> reaches 5 V in our case. Once, V<sub>out</sub> is higher than 5 V, the PWMs become synchronized with current *i* and their time durations become regulated to control the output voltage to the voltage set point. When the set point is reached, the converter operates in steady-state with charge and energy balanced over a full period. **Figure V.25** shows the experimental transient response. As explained before, this transient mode is divided into two phases:

• Starting: unregulated phase

This phase operates in open-loop (unsynchronized phase), where the PWMs are fixed to their initial values and the frequency is set to 95 kHz. As shown in Figure V.25, the waveform of current  $i_P$  reveals high ripples, as the switches are not turned on synchronized with the conversion cycle, they are not operated with ZVS. This phase takes 0.4 ms, for the output voltage to reach the threshold value.

• Transient response: regulated phase

During this phase, the regulation is turned-on, which allows to control the switches synchronized with the current. This makes the power transfer more effective. Consequently, the output voltage increases to reach the set value. As shown in **Figure V.25**, the output voltage increases with a slew rate up to 70 V/ms before reaching a peak value of 56 V, which means an overshoot of 8 V. In addition, we have measured a setting time of 1.2 ms for a band error of  $\pm$  5 V around the voltage set point. The steady-state operation is reached after 3 ms, where the output voltage is stabilized to its 48 V set point. Thus, this validates the operating of the control strategy.



Figure V.25: Transient response for:  $V_{in}$ =120 V,  $V_{out}$ =48 V and P=10 W.

#### V.3.2 Steady state operation

Figure V.26 shows the experimental waveforms measured during the steady state operation, for an input-output voltage of 120-48 V. The waveform of  $V_P$  illustrates the six-stages conversion cycle, confirming a proper operating of the control. However, small oscillations of the peak value of  $V_P$  can be observed at t<sub>3</sub>. These oscillations are due to the control of the instant t<sub>2</sub>. Indeed, as stated before, t<sub>2</sub> depends on how accurately is  $V_{P+}$  measured at t<sub>3</sub>. Nevertheless, these oscillations remains low (~ 10V) compared to the input voltage (120 V). Overall, the control strategy has been able to regulate the output voltage to its reference value.



Figure V.26: Steady-state regime for: Vin=120 V, Vout=48 V and P=10 W.

#### V.3.3 Load variations

Once we have validated the transient response during the turning-on of the control strategy and the steady-state operation, we have proceeded to check if the control is able to follow an output voltage set point after a load change. Figure V.27 and Figure V.28 show the dynamic response to load variations.

In Figure V.27, we have instantly changed the load  $R_L$  from 329  $\Omega$  to 177  $\Omega$ . Thus, the output power increases from 7 W to 13 W. As shown, before the load variation, the power converter operates under energy balance  $E_{in1} = E_{out1}(+E_{loss})$  at an output power about 7 W, which is noted by a constant amplitude of the current (sustainable regime). When a variation on the load is applied, the energy balance is not conserved, as the amplitude of the current *i* is not sufficient to maintain the output voltage to its set point, i.e. to reach the output power requirement.



Figure V.27: Dynamic response for a power step from 7 W to 13 W.

Therefore, during this transient regime, the input energy is higher than the output one  $E_{inl} > E_{outl}(+E_{loss})$  at each resonant period, which increases the current *i* amplitude. Once, it reaches a sufficiently high value, the resonator can store sufficient energy to transfer the right power level to the output load. Therefore, a new energy balance  $E_{in2} = E_{out2}(+E_{loss})$  is established for the output power of 13 W, which leads to a constant amplitude of *i* (sustainable regime). This transient takes about 2 ms, enabling to regulate the output voltage with an overshoot not exceeding 10 V. This test validates the operating of the control strategy while the output power changes.

In Figure V.28, we have performed a load variation by increasing  $R_L$  from 177  $\Omega$  to 329  $\Omega$ , in order to check if the control strategy is able to regulate the output voltage while the output power decreases. As shown, the output voltage is regulated after almost 3.5 ms. However, we can observe a current overshoots on *i<sub>P</sub>*, since S1 is not turned with ZVS. Indeed, these overshoots are due to the regulation of t<sub>2</sub> that needs to be adjusted to ensure the soft charging of V<sub>P</sub> to reach V<sub>in</sub> at t<sub>3</sub>, making it possible to turn-on S1 with ZVS. As shown, the ZVS of S1 is regulated after almost 7 ms.



Figure V.28: Dynamic response for a power step from 13 W to 7 W.

Overall, the implemented control strategy enables to regulate the output voltage even when load variations occur.

#### V.3.4 Efficiency

**Figure V.29** illustrates the efficiency of the converter as a function of the output power over various gain levels. It should be noted that the driving power (estimated to 1 W) is not considered in the efficiency calculation since the control board is overdesigned. As illustrated,
the converter exhibits a good efficiency over the various operating points, higher than 90 % for most of the cases. In addition, it demonstrates the capability of the control strategy to operate at various gain levels.



Figure V.29: Efficiency vs Output Power.

### V.4 Analyze and discussion

The proposed control strategy was able to regulate the output voltage at various operating conditions as demonstrated previously. Nevertheless, it should be noted that this control is sensitive to voltage measurement accuracy, which is needed for the control loop. Indeed, the sensing interface of the voltage is depending on the voltage divider and the pre-amplification and amplification stages, which should be well designed and calibrated. Also, the control of dc-dc converter based on PR reveals to be more complex than the classical ones which operate at fixed frequency and with only two stages for most of them (one PWM having only two values and dead time). Indeed, to control a PR based converter, it requires frequency and phase tracking, two ZVS detection, a soft-charging regulation, and a load regulation. However, the implementation shows the feasibility of controlling such a converter by using comparators and simple control loops and low-cost controller while exhibiting a quite high performance in terms of response time and overshoot. Moreover, the experimental behavior was observed very close to the simulated one. High efficiency (higher than 90%) was obtained at various gain levels and

power operating points for high to low voltage conversions. These satisfactory results give encouragements for further works on this new conversion principle.

### V.5 Summary of the chapter

In this chapter, we have developed and designed a control strategy of a step-down dc-dc converter based on PR that operates on a six-stages conversion cycle. Energy balance, soft charging and ZVS were all considered in the development of the control law. The control strategy was firstly verified by simulation in transient and steady-state regimes. Then, we have designed the power and the control circuits for experimental checking for an input voltage of 120 V, an output voltage < 48V and an output power up to 16 W. The control strategy was synthetized by using VHDL language and then implemented in a FPGA. The experimental results have demonstrated the feasibility to regulate the output voltage of the dc-dc converter while ensuring the six-stages conversion cycle. Indeed, the control loop is able to regulate the converter in order to follow the output voltage set point at the starting of operation (transient regime), steady-state operation and when load variations are applied.

This chapter was published in the EPE2020 conference, [38] entitled: Implementation of Control Strategy for Step-down DC-DC Converter Based on Piezoelectric Resonator, and presented in a talk. This published paper discusses the closed-loop control of a DC-DC converter based on a piezoelectric resonator, which demonstrates experimentally the first implementation of a control for this type of converter.

# Chapter VI: Conclusion

**Abstract**: This chapter summarizes the various investigation subjects that have been conducted in this thesis, and the main results are presented. In addition, we present the future challenges and opportunities for the piezo-based power conversion in aims of miniaturization and integration of power converters.

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### VI.1 Conclusions

In this thesis, we focused on the development of novel PR-based power converters for high to low voltage and low power applications. Replacing the L-C resonant circuit in quasi-resonant or resonant DC-DC converters with PRs reduces the number of components. In addition, PRs offer a low-profile design and a high power density, which facilitates their miniaturization and integration. They can also offer low losses and high electromechanical coupling factor. However, due to the electrical model and peculiarities of piezoelectric resonators, we need to adapt the power conversion mechanism and the conversion cycle, in order to exploit the performances of these materials.

The interest of using piezoelectric material is demonstrated. The mechanism of the conversion is explained with a method of construction for any conversion cycle using sixswitching stages alternating between constant voltage stage and open circuit stage. The conversion cycle consists of taking energy from the input source, storing it as mechanical energy in a piezo material, then, transferring that energy in electrical form to the load. Therefore, during this cycle, the energy and charge are balanced, resulting in a sustained oscillation and low power loss. A generic analytical model was also presented to predict the timing of each stage and the amplitude of the current in the motional branch. The expression of the current enables a better understanding of the impact of the switching sequence, the properties of the material and the electric parameters of the converter like the input voltage, the output voltage and the load. Also, it enables a fast sizing of the power switches. A comparison between the various conversion switching sequences was conducted in order to identify the appropriate one for our application. This comparison was achieved over various operating conditions, and stated which switching sequence can minimize the constraints on the material and maximize efficiency as well. An actual prototype was built for experimental verification. The experimental measurements exhibit a high efficiency and high power density, as for instance: a 100 W output power for a volume of PR of 1 cm<sup>3</sup> and an input to output voltage of 200 V-60 V was achieved in steady state (180 W in transient pic power).

A control strategy was developed which can be used for any switching sequence for any DC-DC converter based on PR, enabling energy/charge balance, soft-switching and soft-charging. A control strategy was designed and implemented by considering our selected switching sequence and topology. The control was validated in simulation (SIMULINK). Then, we have designed an actual circuit and the control laws were implemented in FPGA. The control

strategy exhibits a good performance in terms of transient time response (less 2 ms) and load perturbation rejection.

To sum up, the power conversion based on piezoelectric components gives a good promise in power electronics which aiming for the miniaturization, the integration on silicon, the high efficiency and the high power density. Nevertheless, several research subjects require more investigations and explorations for maturing this conversion technique.

### VI.2 Perspectives and future challenges

The recent advancements have shown serious opportunities for further research in PR based power converters and in potential applications, as well as high voltage conversion or low voltage for integrated power supply. It requires supplementary investigation and optimization, which are presented below:

Design and optimization of the PR materials for discrete as well as integrated applications is needed, for a better exploitation of their performances. Indeed, as the PRs are not extensively employed in power converters, the guideline of designing the PR is lacking. This guideline design should take into consideration the mechanical mounting, the fabrication process, reducing the effect of spurious modes, electrical connection (bonding, silver glue...) and the heat sink. Also, optimization considering an additional mass connected mechanically to the PR for a higher power density should be investigated as it may offer a bigger energy density by just adding an inert mass [48]. Also, this guideline must be combined with the circuit design as the IC.

Further explorations in power converters, conversion cycles and control is needed, in order to cover all the possibilities of using PRs as storage components. In the end, we should be able to meet all the needs of power converters..

It is also possible to design multi-port converters (several inputs and/or outputs) that share the same piezoelectric resonator [31]. Therefore, the control and the power management can be developed as consequence. Also, using more than six-switching sequence enables to store additional energy in the PR or in mass (by exciting the material at a higher amplitude of oscillation than needful) and then transfer it immediately to the load when necessary [Patent 2], reducing by that way the time response of the system.

Moreover, isolated magnetic-(and less) power converters were investigated in this thesis but not presented as it is subject of patents. To conclude, the piezo-based power conversion may become one of the most important breakthroughs in power electronics for miniaturization and integration of power converters.

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# APPENDIX

# **APPENDIX A: Piezoelectric materials**

## Piezoelectric Materials for the DC-DC Converters Based on Piezoelectric Resonators

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Abstract—This paper presents a generic representation of the six switching sequences dc-dc converters based on piezoelectric resonator. In addition, the estimation of current density and voltage limitations of lead zirconate titanate and lithium niobate resonators are given. A comparison between these piezoelectric materials is carried out. Then, we propose a lithium niobate-based piezoelectric resonator design that reduces spurious modes, while providing a quality factor of 3700 and an electromechanical coupling factor of 25.5 Experimental results demonstrate the operating principle for input-output voltage of 60-20 V around 6 MHz for a wide power range 2-32 W. A peak efficiency of 93.6 % is obtained at 16 W. A power density of 128 W/cm<sup>3</sup> for the designed resonator is reached for input-output voltage of 60-20 V.

Keywords—Piezoelectric resonator, DC-DC converter, soft switching, power converters, Lithium Niobate, inductorless power converter.

#### I. INTRODUCTION

Nowadays, the main challenge for miniaturization and integration of power converters is reducing the volume of the passive components, such as the capacitors and the inductors contained wherein. To this end, increasing the frequency enables reducing the energy converted by cycle, which allows downsizing the passives elements [1]. While, semi-conductors (GaN HEMT) offer a possibility to increase the switching frequency regarding to conventional MOSFET, reducing the volume of inductors becomes difficult by maintaining low losses and their integrations is not compatible with the actual process [2-3]. Power converters based on capacitances ensure high power density and high efficiency compared to magnetic converters, and their integration is possible. However, their efficiency decreases for a variable gain operation [4-5].

To overcome these limitations, one potential solution consists of using piezoelectric components as a replacement for the inductors and the capacitances [6]-[16]. Piezoelectric components use the converse piezoelectric effect to convert electric energy to mechanical form and the direct effect allows converting mechanical energy to electrical one. So, employing both effects enables using the piezoelectric element as electrical-mechanical-electrical transducer. Also, the piezoelectric ceramics provide an inductive behavior between their series and parallel frequency, which enables zero voltage switching (ZVS) and soft charging operations [17]-[24]. In [17]-[24], the operating principle based on

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piezoelectric resonators (PR) was explored and validated experimentally for high and low voltage conversion and low power levels (<200 W). These first results show a promising future for the piezo-based power converters.

Some PZT ceramics were selected for their high quality factor (Q) and their high electromechanical coupling factor (k) [17]-[19], [20], [26]. However, the PZT materials have a high dielectric constant ( $\varepsilon_{33}^S/\varepsilon_0 = 1500$ ) which induces a high intrinsic capacitance. As a result, the current needed to charge and discharge this capacitance over a cycle becomes higher with increasing the operating frequency [19]. In [25], Lithium Niobate (LNO) was introduced as an alternative to the PZT. This material provides a lower dielectric  $(\varepsilon_{33}^S/\varepsilon_0 =$ 30) and a higher quality factor than PZT, while it exhibits an electromechanical coupling factor similar to the PZT ceramics. Fig. 1 shows the figures of merit  $k^2Q$  for some piezoelectric materials, where, the efficiency is plotted as a function of  $k^2Q$ , considering the switching sequence presented in [20-21], and taking into account only losses due to the damping effect of the PR. The data are collected from the datasheet of the suppliers. As shown, LNO exhibits the highest  $k^2Q$  and efficiency, making it a promising alternative to PZT. The aim of this paper is to present a comparison between PZT and LNO in terms of current density and voltages operation, and presents a design of a PR based on LNO.

This paper is organized as follow: in section II, we present a generic model of dc-dc converters based on PRs for conversion cycle with six switching stages (can be also used for four switching sequences). An example of the switching sequence is given to verify the generic model. In section III, we propose an estimation of the current density as a function of frequency with the operating voltage limits. A comparison



Fig. 1. Figure Of Merits of Piezoelectric Materials.



Fig. 2. (a) Butterworth Van-Dyke equivalent circuit (BVD) [27], (b) Geometry of the PR.

between PZT ceramics and LNO is proposed in terms of current density and voltage. Then, we propose a design of PR based on LNO that enables to reduce the spurious modes. In section IV, experimental results are shown to verify the performance of the dc-dc converter based on LNO resonator.

#### II. THE OPERATING PRINCIPLE

#### A. Generic conversion cycle and model

The piezoelectric resonator (PR) can be modeled using the Butterworth Van-Dyke equivalent circuit (BVD), shown in Fig. 2a. This model is composed of a LCR<sub>P</sub> branch that expresses a mechanical behavior of the PR, in parallel with a capacitance  $C_P$ . Within the inductive region, located between the resonant frequency (LC) and anti-resonant frequency  $(L(C//C_P))$ , the current *i* in the LCR<sub>P</sub> branch can be assumed sinusoidal thanks to the high quality factor of the piezoelectric materials. Therefore, the conversion cycle is composed of six stages, which alternate between connected stage (V<sub>P</sub> = constant) and open-circuit stage ( $i_p = 0$ ), for operation with variable conversion gain  $V_{out}/V_{in}$  [17-25]. The connected stage allows exchanging the PR's charge with the source and/or load or zero voltage (short-circuit). The opencircuit stage enables changing the voltage level of the PR by using the soft charging/discharging of the capacitance  $C_P$  in order to turn-on the switches in ZVS mode. So, we consider a six stages conversion cycle, composed of three connected stages and three open circuit stages; where the connected stages operate at three voltage levels named  $V_a$ ,  $V_b$  and  $V_c$ . These voltages can be the input voltage, the output voltage, zero voltage or a combination of the input and the output voltage. Then, we define three voltage levels  $\{V_a, V_b, V_c\}$ , where:

- The voltage level V<sub>a</sub> and V<sub>b</sub> are defined at each polarity of the current *i*.
- The voltage level V<sub>c</sub> is defined at the same polarity of the current *i* as V<sub>a</sub>, which results that Q<sub>a</sub> and Q<sub>c</sub> have the same polarity (the same sign).
- Each voltage level stage is defined during only a single polarity of the current *i*.

From these considerations, the charge and energy balance (for lossless conversion cycle) write by:

$$Q_a + Q_b + Q_c = 0 \tag{1}$$

$$Q_a V_a + Q_b V_b + Q_c V_c = 0 \tag{2}$$

By suppressing  $Q_b$  in (2) by using (1), we obtain:

$$(V_a - V_b)Q_a = (V_b - V_c)Q_c$$
(3)

In case  $V_a > V_b$ ,  $V_b > V_c$  is induced because  $Q_a$  and  $Q_c$  have by definition the same polarity, leading to the classification of:  $V_a > V_b > V_c$ . As  $V_a > V_c$ , the current *i* should be positive in the half period where  $V_a$  and  $V_c$  are located, because we need to discharge the capacitance  $C_P$  to go from  $V_a$  to  $V_c$  during the open circuit stage between  $V_a$  and  $V_c$ . In the case where  $V_a < V_b$ ,  $V_b < V_c$ , so, we obtain the classification of the voltages as:  $V_a < V_b < V_c$ , and the current *i* should be negative, since we need to charge the capacitance  $C_P$  during the open stage between  $V_a$  and  $V_c$ . Therefore, we can state a *positive power flow* regarding to  $V_b$  by considering:

- (a) A positive power flow is taken under  $V_b$ , in this case, we introduce the factor  $\beta$  that is equal to 1 for the classification:  $V_c < V_b < V_a$ .
- (b) A positive power flow is provided from  $V_b$ , in this case, we define the factor  $\beta$  equal to -1 for the classification:  $V_a < V_b < V_c$ .

These two configurations can be merged into a single representation by using the factor  $\beta$  that is multiplied by the voltage  $V_P$  and the current *i*, which is leading to a single classification  $\beta V_c < \beta V_b < \beta V_a$ . Fig. 3 shows the steady-state generic conversion cycle, with  $V_P$  the voltage across the piezoelectric and *i* the current. The voltage extremum  $V_{zvst3}$  (respectively  $V_{zvst6}$ ) is required between the connected stage  $V_a$  and  $V_b$  (respectively between  $V_b$  and  $V_c$ ) to ensure the ZVS conditions, when one ends of the PR is floating. If yields that, for a given voltage levels triplet { $V_1$ ,  $V_2$ ,  $V_3$ }, the construction of a conversion cycle needs firstly to identify the median voltage of { $V_1$ ,  $V_2$ ,  $V_3$ }, named  $V_\beta$ , and the parameter  $\beta$  that determines the power flow as follow:

$$\begin{cases} V_{\beta} = \text{median}\{V_1, V_2, V_3\} \\ \beta = -\text{sign}(Q_{V_{\beta}}) \end{cases}$$
(4)

Once  $\beta$  is known,  $V_a$ ,  $V_b$  and  $V_c$  are then immediately identified by:

$$\begin{cases} \beta V_a = \max\{\beta V_1, \beta V_2, \beta V_3\}\\ \beta V_b = \operatorname{median}\{\beta V_1, \beta V_2, \beta V_3\}\\ \beta V_c = \min\{\beta V_1, \beta V_2, \beta V_3\} \end{cases}$$
(5)

The amplitude I of the current in the motional branch of the resonator is given as a function of the switching sequences:

$$I = \frac{\beta \pi}{(\alpha_b - \alpha_c) + (\alpha_a - \alpha_c)A_0} I_{out} + I_{circul}$$
  
=  $I_{useful} + I_{circul}$  (6)

where  $A_0 = \frac{v_c - v_b}{v_a - v_c}$ , and  $I_{circul} = \frac{\beta(v_{ZVSt3} - v_{ZVSt6})}{2} C_P \omega$ .  $I_{circul}$  is the amplitude of the circulating current required to charge and discharge the capacitance  $C_P$  over a period, this amplitude of current is required even with no load.  $I_{useful}$  is the amplitude of the current required to supply the output load, which depends on the switching sequence and the load  $I_{out}$ . The parameter  $\alpha_a$  (respectively  $\alpha_b$ ,  $\alpha_c$ ) is defined regarding to V<sub>a</sub> (respectively V<sub>b</sub>, V<sub>c</sub>) by :

$$\begin{cases} \alpha_{a} = -1, & \text{if } V_{a} \text{ contains } (-V_{out}) \\ \alpha_{a} = +1, & \text{if } V_{a} \text{ contains } (+V_{out}) \\ \alpha_{a} = 0, & \text{otherwise} \end{cases}$$
(7)

The amplitude I is the key parameter for the design of the PR in order to fit the requirements in terms of power and inputoutput voltages. The charge factor K in [20], can be expressed by:

$$K = \frac{(\alpha_b - \alpha_c) + (\alpha_a - \alpha_c)A_0}{2\beta} \tag{8}$$

The current amplitude *I* and the *K*-factor expressions can be validated through the examples explored in [17], [19-20]. The output current is written as a function of the switching sequence by:

$$I_{out} = \frac{P_{out}}{V_{out}} = -\left( (\alpha_a - \alpha_c) + (\alpha_b - \alpha_c) \frac{V_c - V_a}{V_b - V_c} \right) \frac{Q_a}{T}$$
(9)

where  $Q_a = \beta \frac{I}{\omega} (\cos(\omega t'_3) - \cos(\omega t_4)).$ 

The output current is directly proportional to  $Q_a$ , which depends on the  $\beta V_a$  stage duration [t<sub>3</sub>', t<sub>4</sub>], as shown in Fig. 3. Finally, by controlling  $t_4$ , we can regulate the output current value, as illustrated in [21]. Therefore, the presented generic conversion cycle enables to:

- Give a single representation of the conversion cycle.
- Identify the unique switching sequence for a given voltage levels regarding to the conversion cycle.
- Achieve a fast calculation of the estimated current *I* and *I*<sub>out</sub>.
- Give the feasible conversion gain ratio.

#### B. Example of implementation of switching sequence

To verify the presented generic model, we can take as an example a step-down dc-dc converter ( $V_{in}>V_{out}$ ) that operates at these three voltage levels { $V_{in}-V_{out}$ ,  $V_{out}$ , 0}, which is explored in [20]. Therefore,  $V_{\beta}$  can be equal to  $V_{in}-V_{out}$  or  $V_{out}$ . In case of  $V_{out} > V_{in}-V_{out}$ , then  $V_{\beta}$  is equal to  $V_{in}-V_{out}$ . Therefore, a positive charge is supplied to the PR under  $V_{\beta}$ , so, the sign of  $Q_{\nu\beta}$  is positive which leads to  $\beta = -1$ . Hence, { $V_a, V_b, V_c$ } are deduced as below:

$$\begin{cases} \beta V_a = \max\{-(V_{in} - V_{out}), -V_{out}, 0\} = 0\\ \beta V_b = \max\{-(V_{in} - V_{out}), -V_{out}, 0\} = -(V_{in} - V_{out})\\ \beta V_c = \min\{-(V_{in} - V_{out}), -V_{out}, 0\} = -V_{out} \end{cases}$$
(10)

The amplitude of the current is in this case:

$$I = \pi \frac{v_{out}}{v_{in}} I_{out} + \frac{v_{in}}{2} C_P \omega = I_{useful} + I_{circul}$$
(11)

where  $\alpha_a = 0$ ,  $\alpha_b = -1$ ,  $\alpha_c = 1$ .

In case of  $V_{out} < V_{in}$ - $V_{out}$ ,  $V_{\beta}$  is equal to  $V_{out}$ . Therefore, a positive charge is taken from the PR. As a result, the sign of  $Q_{P\beta}$  should be negative leading to  $\beta = 1$ . Thus, the triplet {V<sub>a</sub>, V<sub>b</sub>, V<sub>c</sub>} are defined as follow:

$$\begin{cases} \beta V_a = \max\{V_{in} - V_{out}, V_{out}, 0\} = V_{in} - V_{out} \\ \beta V_b = \operatorname{median}\{V_{in} - V_{out}, V_{out}, 0\} = V_{out} \\ \beta V_c = \min\{(V_{in} - V_{out}), V_{out}, 0\} = 0 \end{cases}$$
(12)



#### Fig. 3. Generic conversion cycle.

In this case, the amplitude *I* is then deduced directly as:

$$I = \pi \left( 1 - \frac{v_{out}}{v_{in}} \right) I_{out} + \frac{v_{in}}{2} C_P \omega = I_{useful} + I_{circul}$$
(13)

where  $\alpha_a = -1$ ,  $\alpha_b = 1$ ,  $\alpha_c = 0$ .

The presented generic conversion cycle can be validated as well through the enumerated switching sequences shown in [19-24].

#### III. LITHIUM NIOBATE PR: DESIGN AND FABRICATION

#### A. PR model

The electrical parameters of the PR based on the BVD circuit (see Fig. 2a) are linked to the physical properties and geometry of the PR. Equations (14)-(17) give the electrical parameters as a function of the physical properties and geometry for an ideal rectangular plate and a disk operating in thickness extensional vibration mode [28], as shown in Fig. 2b. The BVD model can be determined as a function of the resonator proprieties and the designed geometry: the area A=ab (or  $\pi D^2/4$  for disk shape) and the thickness *th* of the PR:

$$C_P = \varepsilon_{33}^S * \frac{A}{th} = \varepsilon_{33}^T (1 - k_{33}^2) \frac{A}{th}$$
(14)

$$C = \frac{8k_{33}^2 C_P}{\pi^2 - 8k_{33}^2} \tag{15}$$

$$L = \frac{th^2 \rho}{8 \, C_P k_{33}^2 Y_{33}^D} \tag{16}$$

$$R_P = \frac{2\pi L f_r}{o} \tag{17}$$

where  $k^2_{33}$  is the electromechanical factor, Q is the quality factor of the material and illustrates the mechanical losses.  $\rho$ is the density of the material in kg/m<sup>3</sup>, and  $Y_{33}^{D}(N/m^{2})$  is the Young's modulus of the material at constant stress. The equivalent impedance of the PR ( $Z_{PR}$ ) is then given by (18):

$$Z_{PR}(f) = \frac{1}{i2\pi f C_P} \frac{R_P + i2\pi L f \left(1 - \left(\frac{f_T}{f}\right)^2\right)}{R_P + i2\pi L f \left(1 - \left(\frac{f_R}{f}\right)^2\right)}$$
(18)

where  $f_r$  is the resonant (series) frequency and  $f_{ar}$  is the antiresonant (parallel) frequency [17].



Fig. 4. The evolution of the current density as a function of the frequency for PZT and LNO.

#### B. Density of the current and limitations

As demonstrated in [19], [29], the amplitude of the current *I* is mainly related to the area of the PR in thickness extensional mode which is therefore the key element for designing the PR. However, this current density j(f) is given for a fixed operating frequency. By using the experimental results in [19], the current density can be empirically estimated by (19) for PZT ceramics:

$$j(f) = j_0 * 10^{0.7 \log_{10} \frac{f}{f_0}}$$
(19)

where  $j_0 = 1 A/cm^2$  at  $f_0 = 1 MHz$  for the PZT C-213 from Fuji Ceramics. This expression states that the current density scales by a factor five per frequency decade. Assuming that the current density of LNO + 36° Y-cut evolves according to the same law, Fig. 4 shows the evaluation of the current density as a function of the frequency. For the LNO, we consider the current density of  $j_0 = 1 A/cm^2$  at 6 MHz that was reached in [25]. Consequently, the LNO provides a lower current density than PZT at same frequency. Assuming the current density expression (19), we can then derive the expression of the maximum voltage applied  $U_{max}(f)$  on the PR when all the amplitude of I is used to charge and discharge the capacitance  $C_P$  (i.e.,  $I=I_{circul}$ ), and when the operating frequency is near to the anti-resonant frequency (open circuit operation). Therefore, the voltage  $U_{max}(f)$  gives an upper limit of using the PR as function of f even without load, where  $U_{max}$ decreases linearly with l/f (i.e.,  $U_{max} \alpha 1/f$  as  $j \alpha f$ ).

$$U_{max}(f = f_{ar}) = \frac{I(f_{ar})}{2\pi C_p f_{ar}} = \frac{j(f_{ar})}{2\pi f_{ar}^2 \gamma}$$
(20)

where  $\gamma = \varepsilon_{33}^{S} \sqrt{4\rho/Y_{33}^{D}}$ , as  $Y_{33}^{D} = 4\rho f_{ar}^{2} th^{2}$ , [28].

However, for an output load, the current  $I_{useful}$  is not zero (i.e.,  $I_{useful}$  is the amplitude of the current required to supply the load). It depends on the output load, as seen in (6). So, we need to reduce  $I_{circul}$  (i.e.,  $I_{circul}$  is the amplitude of the current required to charge and discharge the  $C_P$  over a period), because I is constant as it is determined by the physical proprieties and the geometry of the PR. Thus, to reduce  $I_{circul}$ , we can reduce the voltage applied on the PR, (6). Therefore, we define  $U_{min}(f)$  that gives the minimum circulating

 
 TABLE I. Comparative between LNO and PZT at the same current density.

	Nt (MHz.mm)	c(mm)	fo (MHz)	$j_0(A/cm^2)$
LNO+36°Y-cut	3.3	0.5	6.6	~1
PZT (C-213)	2	2	1	~1

current while  $I_{useful}$  is maximized, which leads to an operating frequency that is taken slightly higher than the resonant frequency, because if  $f=f_r$ ,  $Z_{PR}$  is then equal to  $R_P$ . Consequently, the PR is only resistive and no energy is transferred to load. Therefore, we define a phase shift  $\delta_{PR}$  caused by the mechanical losses near  $f_r$ , while the PR still inductive, which is given by (21), obtained from the impedance  $Z_{PR}$ .

$$\delta_{PR} = \pi - \tan^{-1} \frac{2\pi l f \left(1 - \left(\frac{l_T}{f}\right)^2\right)}{R_P} + \tan^{-1} \frac{2\pi l f \left(1 - \left(\frac{l_T}{f}\right)^2\right)}{R_P}$$
(21)

For a high quality factor material (i.e.,  $-2\pi lf(1 - (f_{ar}/f)^2) \gg R_P$ ), the equation (21) can be simplified into a function of Q and  $\lambda = \frac{f}{f_r}$  assuming  $\lambda > 1$ :

$$\tan \delta_{PR} = \frac{1}{\varrho \lambda \left(1 - \left(\frac{1}{\lambda}\right)^2\right)}$$
(22)

By imposing a phase shift (loss rate tan  $\delta_{PR}$ ), we can deduce  $\lambda$  by solving the following equation:

$$\lambda^{2} - (Q \tan \delta_{PR})^{-1} \ \lambda - 1 = 0$$
 (23)

Once  $\lambda$  is known, we determine  $U_{min}$  by computing:

$$U_{min}(\lambda f_r) = I(\lambda f_r) Z_{PR}(\lambda f_r)$$
(24)

In Fig. 5, we have plotted the maximum voltage  $U_{max}$  on the PR when the maximum current I that the piezoelectric can sustain is only a circulating current, and the minimum voltage  $U_{min}$  that enable to reach that same maximum current I. That last one operating voltage minimizes the circulating current while maximizing the useful current. This plot is done for the PZT C-213 operating in thickness mode, considering a quality factor of 2000 and a loss rate of 2 %. The filled area corresponds to the operating area where the physical maximum current density is reachable and not exceeded. Indeed, for a given frequency, increasing the voltage increases the circulating current while the useful current decreases as the current amplitude I is constant for a given frequency, since I depends only on the material's proprieties. Also, the filled area decreases with the quality factor and increases with increasing the loss rate. This plot can be crossed with the dielectric strength of the material (i.e.,  $U=E_{bd}N_t/f$ , where Nt is the frequency thickness constant of the piezoelectric ceramic). As shown, when increasing the frequency, the voltage decreases, what limits the operating points in terms of voltage (for instance: at 10 MHz, U=[0.5 V, 25 V]), limiting the downsizing of the PR, due to the high dielectric constant of PZT. Therefore, using LNO with a lower dielectric constant, a higher quality factor and electromechanical coupling factor could be an alternative at higher frequency and high voltage operation. Indeed, as shown in Fig. 6, the LNO voltage operating range is shifted in higher voltage than the PZT (for instance, at 10 MHz, U= [14 V, 258 V]), which illustrates a good potential of



Fig. 5. Voltage limits for PZT C-213, with Q = 2000 and  $\tan \delta_{PR} = 2 \%$ .

utilization at high operating frequency (>1 MHz) for usual < 600 V voltage operating range.

To sum up, these plots enable to design a PR regarding to operating conditions  $\{P, f \text{ and } V\}$ , by considering a distribution between the circulating current  $(f, V, C_P)$  and the useful current  $(P \text{ or } I_{out})$ .

#### C. Lithium Niobate resonator: Design and fabrication

Lithium niobate is an anisotropic material [30]. Therefore, the piezoelectric constant ( $d_{33}$  in C/N) and the dielectric constant of the material depend on the orientation of the piezoelectric crystal, as illustrated in [31]. In this work, we have selected lithium niobate +36°Y-cut plates (promoting a quasi-extensional vibration mode) because it offers a good compromise between obtaining a high piezoelectric electromechanical coupling and a low dielectric constant (i.e., low  $C_P$  leading to low  $I_{circul}$ ). Also, we aim to fabricate a PR for a low voltage operation (< 100 V) and exhibiting a resonant frequency around 6 MHz. The PR is fabricated from a double-side polished 4 inch commercial black-LNO +36°Ycut wafer with a thickness of 0.5 mm  $\pm$  20µm (black wafers allow reducing the pyroelectric effect of the material during the fabrication process), from the supplier Yamaju Ceramics. On both sides of the wafer, 2 µm-thick aluminum electrodes were deposited by evaporation and then patterned by wet etching. Fig. 7 shows the fabricated wafer after wafer dicing, with two resonator shapes. Deported electrodes are used at the top and bottom of each samples for the electrical contacts with the PCB board, in order to reduce the impact of the mechanical fixtures on the PR's mechanical behavior. The two types of devices have the same active area, which is  $\sim 5 \text{ cm}^2$ .

#### D. Impedance plot

Fig. 8 shows the impedance of the PRs obtained by using an impedance analyzer. For the measurement, the PRs have been mounted on PCB as shown in Fig. 9a. The electrical contacts are made by using wire bonding at the top and bottom of the deported electrodes. In addition, the measured impedances of the PRs are compared to the theoretical model (the fundamental mode) that is plotted in dashed curves, revealing a good agreement with the fabricated prototypes. However, as shown in the Fig. 8a, the rectangular PR exhibits spurious modes within the inductive region due to lateral vibration modes, which create a discontinuity in terms of the



Fig. 6. Voltage limits comparison between PZT C-213 in cyan color and for LNO +36°Y-cut in gold color, for Q=2000 and tan  $\delta_{PR} = 2$ %.



Fig. 7. Fabricated wafer LNO +36°Y-cut.

parameters	Calculated	Measured
$\varepsilon_{33}^S/\varepsilon_0$	36.64	37.4
C <sub>P</sub>	315pF	325pF*
С	72.2pF	84.5pF
L	8.75µH	7.6µH
R <sub>P</sub>	33mΩ	80 mΩ**
$f_r$	6.3MHz	6.281MHz
f <sub>ar</sub>	7.03MHz	7.1MHz
$k_t^{2***}$	0.24	0.255
Q	104****	3700
k <sup>2</sup> 0	2400	955

<sup>\*</sup> C<sub>P</sub>=325 pF is measured at outside of the resonant frequency 3fr around 18 MHz. The measurement of C<sub>P</sub> is provided with an accuracy of +/-10%.\*\*R<sub>P</sub> is measured at the series frequency f<sub>n</sub>\*\*\*k<sub>i</sub> is the coupling factor for disk shape resonator for thickness mode and taken insteade of k<sub>3,k</sub>\*\*\*\*Q is not given by the supplier, so we have approximated Q by Q=10<sup>µ</sup>/f<sub>n</sub> [30].



Fig. 8. PR's impedance between its resonance and anti-resonance for: (a) disk with D=25mm and th=0.521mm, (b) Rectangular with a=20mm, b=25mm and th=0.521mm.

operating points as the power is depending on the frequency [24]-[25]. Nevertheless, these spurious modes can be attenuated by using a disk shape PR. Indeed, in Fig. 8b, the disk shape resonator exhibits a lower spurious mode content in the inductive region.

From the plotted impedance and using (25)-(28), we have extracted the equivalent electrical circuit for the disk resonator, as shown in TABLE II. Indeed, TABLE II shows a good accuracy between the equivalent electrical model parameters obtained from the theoretical equations and from the experimental impedance. The designed PR provides a high quality factor of 3700 and a high coupling of 25.5 %, which gives  $k^2Q$  of 955.

$$k_{33}^2 = \frac{\pi}{2} \frac{f_r}{f_{ar}} \cot\left(\frac{\pi}{2} \frac{f_r}{f_{ar}}\right) \tag{25}$$

$$C = \frac{8k_{33}^2 C_P}{\pi^2 - 8k_{33}^2} \tag{26}$$

$$L = \frac{1}{4\pi^2 C f_r^2}$$
(27)

$$Q = \frac{2\pi L f_r}{R_p} \tag{28}$$



Fig. 9. Photograph of the mounted PR on PCB phi-board (a), and of the circuit board (b).



Fig. 10. Circuit topology.

#### IV. EXPERIMENTAL RESULTS

In this part, we have integrated the fabricated PR into a dcdc converter. The prototype is described and experimental results are exhibited to validate the operation of LNO based PR in dc-dc converters.

#### A. Topology and setup

The topology of the dc-dc step-down converter is presented in [19], and shown in Fig. 10. In this paper, we focus on the switching sequence presented in section II.B and [20]. Therefore, only S1, S2, S4 and S5 are used to operate with the switching sequence  $\{V_{in}-V_{out}, 0, V_{out}\}$ . Fig. 9 presents the mounted PR on PCB phi-board and the main circuit board. The circuit is based on two layers of copper of 1 oz and a size of 11x9 cm<sup>2</sup>. The GS66504B was taken for the switches with the gate driver SI8271. The switches are driven by  $V_{GS}$ =+5 V/-2 V. The equivalent model of the PR is

shown in TABLE II. The PWMs are generated by a PLL clock implemented on FPGA (XC7A35TICSG324) with a precision of 1 % of the resonant period, so, the angular stages are conserved while the frequency is tuned. The timings are pre-calculated by using the analytical model presented in [19], [24] and solved at the center frequency between resonant and anti-resonant frequency, and then tuned to ensure soft switching and soft charging.



Fig. 11. Experimental waveforms of PR'voltage at differents power levels for switching sequence  $\{V_{in}$ - $V_{out}$ , 0,  $V_{out}$ .



Fig. 12. Efficiency Vs. Output Power:  $V_{\text{in}}{=}60~V$  and  $V_{\text{out}}{=}20~V.$ 

#### B. Waveforms

As mentioned before, we use the switching sequence {V<sub>in</sub>-V<sub>out</sub>, 0, V<sub>out</sub>}, whose theoretical waveforms are shown in [20], [25], with the corresponding timing  $\{t_0...t_6\}$  shown in Fig. 3. Fig. 11 shows the evolution of the experimental waveforms of the voltage across the PR at different power levels, and for an input voltage of 60 V and a gain ratio of 1/3.  $V_{P+}$  and  $V_{P-}$  are the voltages at the ends of the PR (as shown in Fig. 10), and  $V_P$  is the voltage across the PR determined by  $V_{P-}$   $V_{P+}$  –  $V_{P-}$ . As shown in Fig. 11, voltage oscillations can be observed due to the parasitic inductance in series with the PR. These oscillations can be reduced by optimizing the routing on the PCB. By increasing the power, the frequency decreases and the timing of the connected stages increases while the open stages decrease. Indeed, for  $P_{out} = 4$  W, the connected stages time-duration is very low as the amplitude of current I is low. However, by increasing the output power, the time duration of open stages decreases as I increases, which enables changing voltage levels briefly. As illustrated in Fig. 12, the PR can operate at low ( $P_{out} = 2 \text{ W}$ ) and high power ( $P_{out} = 32$  W), which gives a wide range of operating power. Indeed, for the PR based on LNO that has been used in [25], the minimum output power was 18 W, as the designed PR in this case provided spurious modes in the inductive region, limiting the operating power range.

#### C. Efficiency

Fig. 12 shows the efficiency as function of the output power for a wide power range of [2-32 W] for input-output voltages of 60-20 V. As illustrated, the power converter shows a good efficiency, with a peak efficiency of 93.6 % reached for 16 W. The efficiency is lower than expected, due to losses induced by turning-on the switches, which are not being turned on exactly with a ZVS mode. Indeed, the timing control has a precision of 1 % of the period deriving from a PLL clock of 600 MHz, for an operating frequency around 6 MHz. This precision is however not enough to ensure a perfect ZVS mode and soft charging. Furthermore, the voltage oscillations make it difficult to turn-on the switches with ZVS mode. Yet, the efficiency is higher than 85 % over a wide power range and expected higher with an optimized control.

#### V. CONCLUSION

In this paper, we have presented a generic model of the dcdc converters based on piezoelectric resonators. Then, we have proposed an estimation of the current density and operating voltage limits of PZT and LNO. A design of PR based on LNO is proposed, achieving a quality factor of 3700 and a coupling factor of 25.5 %. In addition, the proposed design enables to reduce spurious modes which allows to operate on a wide output power range. The designed PR enables to operate for an output power range of 2-32 W for input-output voltage of 60-20 V. A peak efficiency of 93.6 % is achieved for an output power of 16 W. As demonstrated, the LNO enables operation at higher frequency and/or higher voltage compare to the PZT material while ensuring high coupling and quality factors. Also, the designed PR provides a power density of 128 W/cm<sup>2</sup> for 60-20 V input-output operation. The study of this material will be deepened in future work to reach its limits.

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# APPENDIX B : List of the contributions

This appendix contains the publications/patents made during this PhD project:

# Journal

### Regular

**M. Touhami**, G. Despesse and F. Costa, "A New Topology of DC–DC Converter Based on Piezoelectric Resonator," in *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6986-7000, June 2022, doi: 10.1109/TPEL.2022.3142997.

### Letter

L. d. A. Pereira, A. Morel, **M. Touhami**, T. Lamorelle, G. Despesse and G. Pillonnet, "Operating Frequency Prediction of Piezoelectric DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2508-2512, March 2022, doi: 10.1109/TPEL.2021.3115182.

# Conference

M. Touhami et al., "Piezoelectric Materials for the DC-DC Converters Based on Piezoelectric Resonators," 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), 2021, pp. 1-8, doi: 10.1109/COMPEL52922.2021.9645999.

**M. Touhami**, G. Despesse and F. Costa, "A New Topology of DC-DC Converter Based On Piezoelectric Resonator," *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1-7, doi: 10.1109/COMPEL49091.2020.9265767.

**M. Touhami**, G. Despesse, F. Costa and B. Pollet, "Implementation of Control Strategy for Step-down DC-DC Converter Based on Piezoelectric Resonator," *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. 1-9, doi: 10.23919/EPE20ECCEEurope43536.2020.9215910.

B. Pollet, M. Touhami, G. Despesse and F. Costa, "Effects of Disc-Shaped Piezoelectric Size Reduction on Resonant Inductorless DC-DC Converter," 2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII *(TRANSDUCERS & EUROSENSORS XXXIII)*, 2019, pp. 1423-1426, doi: 10.1109/TRANSDUCERS.2019.8808328.

**Mustapha Touhami**, Ghislain Despesse, Lucas de Araujo Pereira, Adrien Morel, Théo Lamorelle, et al. "Effect of Operating Frequency On Piezo-Based DC-DC Converter. 10th National Days on Energy Harvesting and Storage", Jun 2021, Grenoble, France. ff10.1109/OJPEL.2021.306702ff. ffhal-03258910f.

Lucas de Araujo Pereira, Adrien Morel, **Mustapha Touhami**, Théo Lamorelle, Ghislain Despesse, et al. "Prédiction de la dynamique d'un convertisseur DC-DC piézoélectrique". 10th National Days on Energy Harvesting and Storage, Jun 2021, Grenoble, France. ffhal-03258911f.

**Mustapha Touhami**, Benjamin Pollet, Ghislain Despesse, François Costa. "A new DC-DC piezoelectric Converter". *9 th National Days on Energy Harvesting and Storage (JNRSE)*, May 2019, Blois, France.

## Patent

[Patent 1] G. Despesse, **M. Touhami**, A. Morel, G. Pillonnet, "Electronic device and method for controlling an electric energy converter comprising a piezoelectric element, related electronic system for electric energy conversion", US - BET 22P0256 – APE.

[Patent 2] G. Despesse, **M. Touhami**, "Convertisseur DC/DC piézoélectrique adiabatique avec gestion d'un stockage tampon "

[Patent 3] G. Despesse, **M. Touhami,** V. Breton, "Convertisseur d'énergie électrique avec élément(s) piézoélectrique(s) et circuit(s) d'aide à la commutation, système électronique de conversion d'énergie électrique associé".

[Patent 4] G. Despesse, **M. Touhami**, V. Breton, "Système de conversion d'énergie électrique avec ensemble(s) piézoélectrique(s) et transformateur électrique".

[Patent 5] G. Despesse, **M. Touhami,** V. Breton, "Convertisseur d'énergie électrique avec au moins un couple d'ensembles piézoélectriques et au moins un interrupteur complémentaire de connexion directe entre eux, système de conversion et procédé de pilotage associés"

[Patent 6] G. Despesse, **M. Touhami,** V. Breton, "Dispositif électronique et procédé de pilotage sans mode commun d'un convertisseur d'énergie électrique comportant deux éléments piézoélectriques, système électronique de conversion d'énergie électrique associé".

# APPENDIX C : ZVS operation of S2

Given the parasite capacitance of the diode/transistor in series with S2, the operation with ZVS of S2 is limited by this capacitance, since it remains charged during the first stage and the voltage across S2 is not zero, as shown by:



Simulated waveforms of drain-source voltage of S2 (No ZVS of S2) and  $V_P$  for  $V_{in} \!\!=\!\! 120 \text{ V and } V_{out} \!\!=\!\! 48 \text{ V}.$ 

However, by using a diode between the source of S2 and the ground, named  $D_{opt}$  (as illustrated below), the parasitic capacitance of D2/transistor can be discharged, and the transistor S2 can be turned on with ZVS when the voltage  $V_P$  reaches  $V_{out}$ , at the beginning of stage 2.



Circuit of the converter with an additional diode D<sub>opt</sub> for ZVS operation of S2.



Simulated waveforms of drain-source voltage of S2 (ZVS of S2) and  $V_P$  for  $V_{in}{=}120~V$  and  $V_{out}{=}48~V.$