Ultra-low power high data-rate transmitter for body-coupled communication in 28 nmFD-SOI CMOS

Guillaume Tochou

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Ultra-low power high data-rate transmitter for body-coupled communication in 28 nm FD-SOI CMOS

Transmetteur très faible consommation et haut-débit pour les communications couplées au corps humain en 28 nm FD-SOI

Préparée en collaboration avec :

STMicroelectronics, Crolles, France
Le laboratoire IEMN, Lille, France
Le laboratoire BWRC, Berkeley, USA

Présentée et soutenue publiquement par :

Guillaume TOCHOU

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Jury

M. Yann DEVAL,	Université de Bordeaux	Président du Jury
M. Sylvain BOURDEL,	Université Grenoble Alpes	Rapporteur
M. Jerald YOO,	National University of Singapore	Rapporteur
Mme Patricia DESGREYS,	Telecom Paris	Examinatrice
Mme Rabia TUGCE YAZICIGIL,	Boston University	Examinatrice
M. Antoine FRAPPÉ,	Junia, Université de Lille	Invité
M. Jan RABAEY,	University of California, Berkeley	Co-Encadrant
Mme Andreia CATHELIN,	STMicroelectronics	Co-Directrice de Thèse
M. Andreas KAISER,	Junia, Université de Lille	Directeur de Thèse

A mes Grands Parents,

« *Science is not only a disciple of reason but, also, one of romance and passion.* »

Stephen Hawking

Abstract

This PhD research work was realized in the framework of *the Human Intranet* project. The Human Intranet aims to interconnect various kinds of sensors and actuators on the human body for wellness and medical applications. Common RF-based solutions such as Bluetooth or Ultra-Wideband suffer from the body shadowing effect degrading the quality and reliability of the channel. As an alternative, body-coupled communication, where the human body is used as the medium of propagation, has been studied. Human body communications require transceivers with flexible data rate, comfortable wearability, low-power consumption, high body coverage, and robustness. This thesis presents a fully digital pulse-based transmitter for capacitive body-coupled communications (c-BCC) in 28 nm Fully Depleted Silicon on Insulator (FD-SOI) CMOS. The transmitter is operating at 450 MHz where surface wave propagation is the dominant mechanism of c-BCC, offering a larger bandwidth with a more stable channel than c-BCC with electro-quasi static communication. The heavily duty-cycled transmitter uses a 90 MHz free-running pseudo-differential ring oscillator and edge-combiners to generate OOK Gaussian-shaped pulses through a switched-capacitor power amplifier (SCPA). Wide range forward body-biasing, specific to FD-SOI technology, allows frequency tuning and adaptive efficiency optimization as a function of data rate. The proposed transmitter consumes 17 to 116 μW for flexible data rates from 0.1 to 45 Mb/s (170 pJ/b down to 2.58 pJ/b) with up to 18 % system efficiency under 0.5 V supply voltage. This work also presents design principles and methodology of body-biased, ultra-low voltage SCPA in 28 nm FD-SOI CMOS, and design considerations for ultra-low power receivers.

Résumé

Ce travail de recherche doctorale a été réalisé dans le cadre du projet *Human Intranet*. Le concept d'Human Intranet vise à interconnecter différents types de capteurs et d'actionneurs sur le corps humain pour des applications médicales et bien-être. Les solutions RF connues, telles que le Bluetooth ou l'Ultra-Wideband, subissent l'effet d'ombre du corps, qui dégrade la qualité et la fiabilité du canal de communication. Comme alternative, la communication couplée au corps humain, où le corps humain est utilisé comme moyen de propagation, a été étudiée. Les communications couplées au corps humain nécessitent des émetteurs-récepteurs avec un débit de données flexible, une expérience utilisateur confortable, une faible consommation d'énergie, une couverture de communication élevée et une grande robustesse. Cette thèse présente un émetteur entièrement numérique à base d'impulsions, pour les communications couplées au corps humains capacitives (c-BCC), en technologie 28 nm Fully Depleted Silicon on Insulator (FD-SOI) CMOS. L'émetteur fonctionne à 450 MHz où la propagation par ondes de surface est le mécanisme dominant, offrant une plus grande largeur de bande avec un canal de communication plus stable que pour une communication c-BCC quasi-static. L'émetteur à rapport-cyclique élevé utilise un oscillateur en anneau pseudo-différentiel de 90 MHz en boucle ouverte et des combinateurs de fronts pour générer des impulsions modulées en OOK de forme gaussienne à travers un amplificateur de puissance à capacités commutées (SCPA). La large plage de tension de polarisation du substrat, offerte par la technologie FD-SOI, permet de régler la fréquence d'utilisation et d'optimiser l'efficacité en fonction du débit de données. L'émetteur proposé consomme de 17 à 116 µW pour des débits de données flexibles de 0,1 à 45 Mb/s (170 pJ/b à 2,58 pJ/b) avec une efficacité système allant jusqu'à 18 % pour une tension d'alimentation de 0,5 V. Ce travail présente également une méthodologie pour la conception de SCPA à ultra-basse tension en 28 nm FD-SOI CMOS, ainsi que des considérations de conception pour les récepteurs à ultra-basse consommation.

Acknowledgement

During these last three years, I had the chance to receive great help and support from many people, who definitely made my Ph.D. journey a stunning experience. With this few words, I would like to express my genuine gratitude to all these people.

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A sincere thank you to Florence Alberti, from Junia ISEN, for taking care of administrative issues and especially for hanging on the phone 1h30 with Air France for me to come back to France in March 2020.

I also thank all my Grenoblois and Phelma friends, the list is way too long to name you all but I am sure you will recognize yourselves. With a special shout out to team "Jean-Jacques" and team "Belle".

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Introduction

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1.1 Research Context and The Human Intranet Concept

1.1.1 Research Context

This manuscript is the result of a CIFRE PhD program from a collaboration between STMicroelectronics, Crolles, France, the University of Lille, France, and the Berkeley Wireless Research Center (BWRC), University of California, Berkeley, California, USA. This thesis is part of an ambitious research project called *The Human Intranet*, which was first proposed in 2015 by Professor Jan Rabaey from UC Berkeley [1].

1.1.2 The Human Intranet Concept

The world is becoming an increasingly connected place and the Internet of Things (IoT) is definitely happening as we speak. A part of the IoT is dedicated to Body Area Network (BAN), to connect devices on and around the human body. Such a network is finding applications in wearables and implantable devices for wellness and health purposes. For example, sensors such as : hearing-aid, Continuous Glucose Monitoring (CGM), Electrocardiography (ECG), oximeter, Electromyography (EMG), Brain-Machine Interface (BMI), among many others. Today's BAN often relies on the smartphone, placed at the center of a star network with a required connection to the outside where all data is processed in the cloud. Smartwatches have now been widely adopted by the general public for fitness, wellness, and healthcare reasons, and they represent the overwhelming majority of wearables in the current market. Latest smartwatch releases are now able to embed several features such as electrical heart sensors for ECG and blood oxygen sensors for oximetry. The number of sensors in smartwatches is expected to increase in the future. However this is again a solution where all the functionalities are centralized in one device worn at one static location of the human body.

The Human Intranet differentiates by proposing a less centralized, more distributed, more dynamic and self-sufficient network. In a more long-term view, such a network could possibly become a way to augment ourselves to cope with a quick-changing environment. The Human Intranet includes many advanced research topics, which can be divided in three main categories : Sensing/Actuating, Computing, and Networking. Sensing and actuating focus on the development of sensors to detect physiological signals from the human body, such as heartbeat detection, glucose sensing, oximetry, neuronal activity, and so forth. It also includes the development of actuators such as robotic prostheses. Computing, focuses on data processing and embedded intelligence [2]. It includes research on Artificial Intelligence (AI) and computing at the edge. Networking, focuses on connecting numerous on-body devices to one another. It includes the design of transceiver but also the definition of Media Access Control (MAC) protocols and upper layers [3]. At all levels, it is

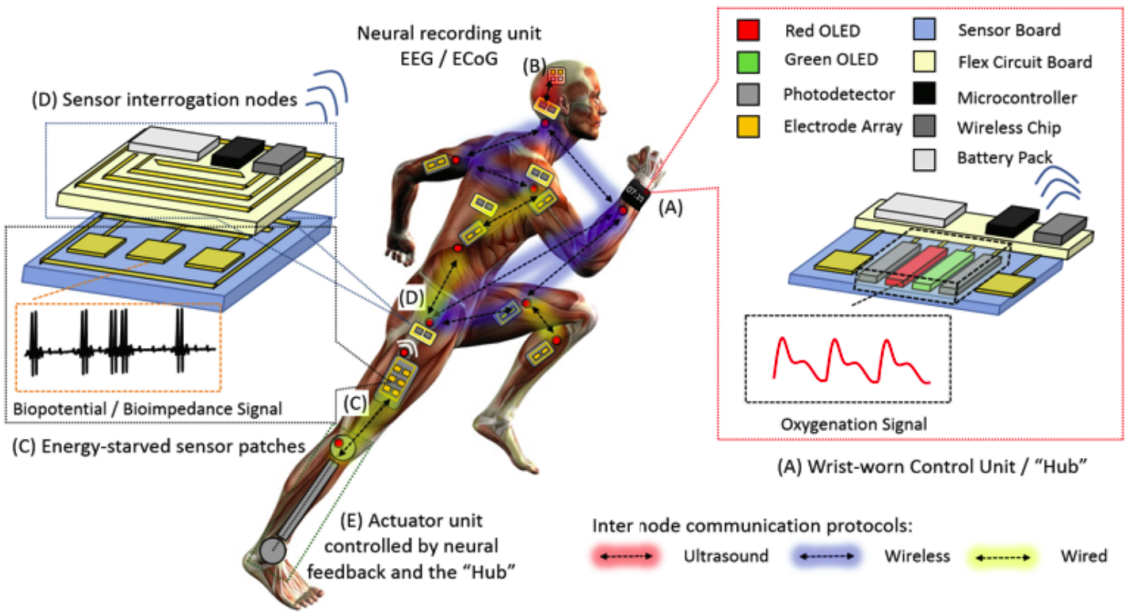


FIGURE 1.1 – Illustration example of the Human Intranet (Taken from Rabaey [1]).

important to note that privacy, security, and safety cannot be neglected at any cost [4].

This work focuses on the Networking research topic of the Human Intranet project and more specifically on the design of wireless transceivers.

1.2 Requirements for the Human Intranet Transceivers

Enabling the Human Intranet requires an energy-efficient network interconnecting multiple sensors and actuators on the human body featuring a diverse and broad range of data rates. For a "user-friendly" experience the devices need to have a small form factor for comfortable wearability. To avoid battery replacement or allow battery-less devices, the power consumption has to be as low as possible for a long-term operating life. It is also required to reach "long-range" (at the human body scale) communication to minimize the use of repeaters that would degrade the wearability and power consumption of the network. Finally, the network requires a robust communication scheme when undergoing changing environments and motions. To summarize, 5 requirements can be highlighted for the Human Intranet transceivers :

— **Flexible Data rate**

— **Wearability/Form Factor**

— **Power Consumption/Energy Efficiency**

— **Range/Body Coverage**

— **Robustness**

Signal	Sampling Rate [Hz]	Resolution [bit]	Data Generation Rate [bit/s]
Temperature	0.2-2	12	2.4-24
Chemicals	10	12	120
Heart Rate	10	12	120
Biometric Z	10-20	12	120-240
Respiration Rate	20	12	240
Oxymetry	60	12	1440
ECG	220-250	12	1440-3000
Motion (/axis)	220-250	12	1440-3000
Neural Recording (/channel)	10k-30k	12	120k-360k

TABLE 1.1 – Table of Data Generation Rates for different types of sensors [6].

1.2.1 Flexible Data Rate

A list of potential sensors that could be used on the human body is given in Table 1.1. The required communication data rate for these sensors has to be at least equal to their data generation rate. Thus, the network has to be able to communicate from a few bit/s for a temperature sensor, up to tens of Mb/s for a Neural Recording sensor with a high number of channels. Furthermore, we can identify two families of devices. The first one generates less than a few thousand of bit/s (from temperature to ECG sensors), where the second family lies in motion and neural recording systems which can generate more than tens of Mb/s depending on the number of channels or axis (up to 23 Mb/s for a 64 channel neural recording sensor) [5].

1.2.2 Wearability/Form Factor

The network on the human body has to remain near-invisible for the user which requires very small devices. Typically, antennas for Radio-Frequency (RF) transceivers can be constraining for small form factor. The other bulkiest parts are batteries and crystal oscillators. Hence it is desirable to use coin batteries or battery-less devices which constrains even more the power consumption. Finally, avoiding the use of a bulky crystal oscillator constrains timing and synchronization between nodes and makes traditional Phase-Locked Loop (PLL) with precise frequency reference unusable.

1.2.3 Power Consumption/Energy Efficiency

Low power consumption is probably the most challenging requirement of the Human Intranet. As stated before, low power consumption and energy-efficiency are mandatory to reach long-term operating life and to avoid bulky batteries. Furthermore, conventional RF transmitter architectures using Power Amplifier (PA)/Low Noise Amplifier (LNA), mixers, and PLL consume too much energy. With such analog architectures, the PA is no longer the most power-hungry block, as the

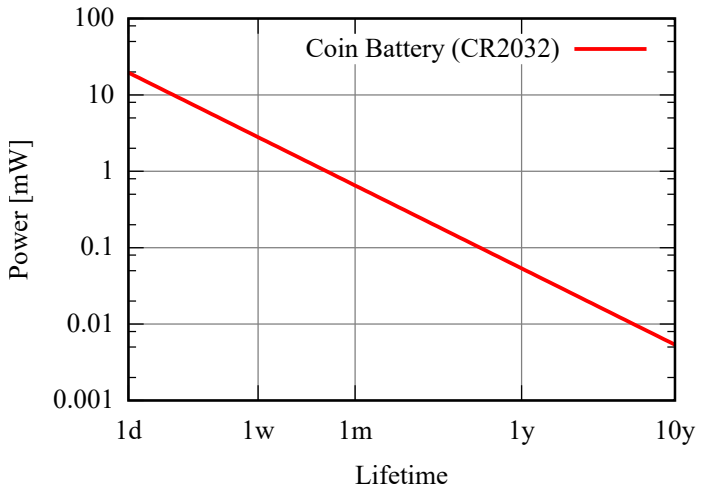


FIGURE 1.2 – Coin Battery Lifetime vs Device Power Consumption

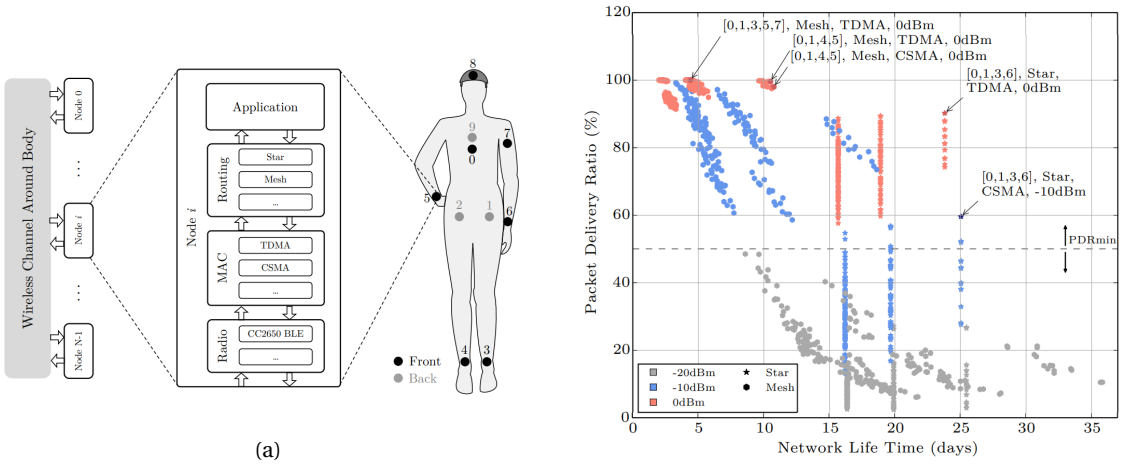
output power is typically below 0 dBm [7]. Hence, the PLL typically becomes the most power-consuming part of the transceiver (> 1 mW) [8]. Moreover, PLLs are typically always-on because of slow start-up time making duty-cycling difficult. PAs with high efficiency at low output power are still desirable. It is then mandatory to imagine new transceiver architectures. An interesting metric to evaluate the efficiency of a transceiver is the *energy-efficiency* which translates the required energy to transmit/receive a single bit. As shown in Figure 1.2 a single node has to consume less than 100 µW to be able to operate for more than a year without any battery replacement. Moreover, to be able to operate battery-less sensors, with state of the art energy harvesters, devices typically require to consume less than 100 µW (Table 1.2).

1.2.4 Range/Body Coverage

Full body coverage is mandatory to be able to communicate from any part of the human body. Although the human body rarely exceeds 2 meters, which corresponds to a short distance compared to what RF radios are capable of, full-body coverage remains challenging without using high output power (at the transmitter) and high sensitivity (at the receiver) and hence increased power consumption. Moreover, the *body shadowing effect* is an additional constraint for front-to-back

Energy Sources	Power Density
Ambient Light (outdoors)	100 mW/cm^2
Human Sweat	1 mW/cm^2
Ambient Light (indoors)	100 $\mu W/cm^2$
Thermal (Human)	60 $\mu W/cm^2$
Vibrations (Human Motion)	4 $\mu W/cm^3$
Ambient RF	1 $\mu W/cm^2$

TABLE 1.2 – Comparison of energy sources [9, 10]



(a) (b)

FIGURE 1.3 – (a) Scenario for the Human Intranet simulation, (b) Simulation results (Taken from Moin et al. [11]).

communication as the human body can "block" the RF signal, significantly degrading the channel.

1.2.5 Robustness

The human body is constantly moving or changing posture, which makes the surrounding environment always changing. When running or walking, for example, two nodes can switch between line-of-sight communication to shadowed communication within a few seconds. It is then essential for the network to be able to cope with the unstable channel caused by the change of environment and postures.

1.3 Network Architecture

Moin et al. [11] have proposed a simulation platform of a Human Intranet network in a realistic scenario (Fig. 1.3a). This publication simulates two network topologies : star and mesh, and for two MAC protocols : Carrier-Sense Multiple Access (CSMA) and Time Division Multiple Access (TDMA) . Two metrics are considered : Packet Delivery Ratio (PDR) and the network lifetime, representing the power consumption of the network. The take-away results from this work is that a star topology allows for a longer network lifetime at the cost of a degraded PDR. In another hand a mesh topology allows to reach higher PDR but at the cost of shorter network lifetime (Fig. 1.3b). Considering those results in network topologies and the wide diversity of devices and requirements from Table 1.1 a mesh of star topology has been proposed by Solt et al. [6], Benarrouch [12] (Fig. 1.4). The network is divided in two categories : *Hubs* and *Leaves*.

— *Hubs* are nodes made for devices generating a high amount of data, requiring high traffic

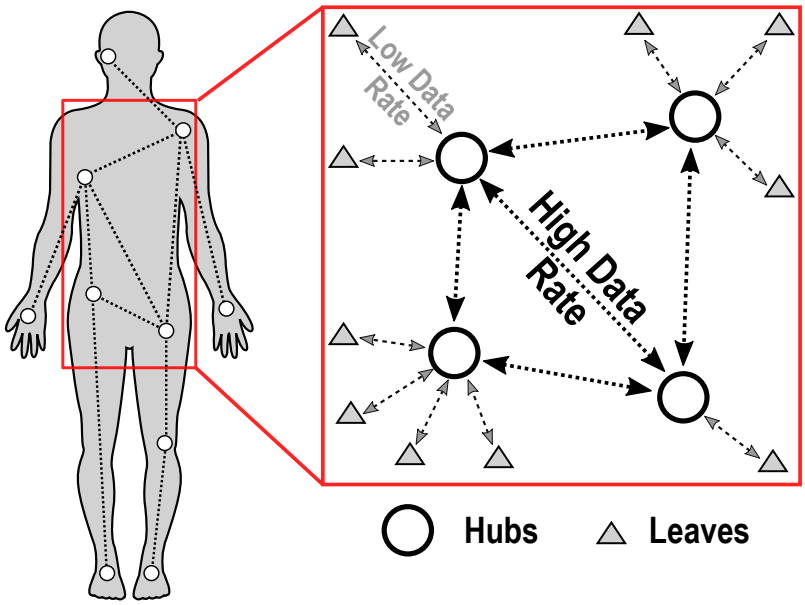


FIGURE 1.4 – The Human Intranet Network [6, 12]

with high data rate communication and low latency. A non-exhaustive list of devices in this category can be : BMI with neural recording/stimulation, motion sensors such as EMG, and actuators (e.g. prostheses). The Hubs are interconnected in a mesh topology as they are meant for more critical applications and hence require a high communication reliability. They are also meant to embed more processing capabilities for a distributed intelligence in the network.

— *Leaves*, in another hand, are made for devices generating a low amount of data requiring lower traffic with lower data rate and tolerating higher latency. They are more energy-constrained as they are expected to be battery-less or to avoid any battery replacement/recharging. A non-exhaustive list of devices in this category can be : temperature, ECG, chemicals, or oximetry sensors. The leaves are connected in a star topology with a Hub as the central node as they are more constrained by the power consumption.

1.4 Thesis Purpose and Main Contributions

1.4.1 Thesis Objective

The main purpose of this thesis is to propose a new ultra-low power transmitter which fulfils all the requirements of the Human Intranet as stated just before. To do so, the existing technologies and communication options need to be explored through a state of the art study at both the channel and physical implementation levels. After identifying the strengths and weaknesses of the existing propositions, the goal is to propose a new and innovative solution to improve the

state of the art of human body communication. The final goal is to design the transmitter in the 28 nm Fully Depleted Silicon On Insulator (FD-SOI) Complementary Metal-Oxide-Semiconductor (CMOS) technology to take advantage of its ultra-low power features such as the wide range body-biasing.

1.4.2 Main Contributions

The main contributions of this thesis work are listed below :

— **Physical Layer & Transceivers Review.** The state of the art of on-body and around-body communications has been surveyed at both the channel and physical implementation levels. Following this comparative survey, a capacitive body coupled communication with surface wave as the dominant propagation mechanism has been designated as an interesting and little explored solution.

— **Transmitter for Surface Wave Capacitive Body Coupled Communication.** As the surface wave propagation has been explored only at the channel level so far, this work proposes the first transmitter using this communication mechanism. The proposed transmitter also defines a new architecture for pulse-based communication with edge-combiners embedded in a switched-capacitor power amplifier for frequency multiplication.

— **Proof of concept prototype and demonstration.** The prototype of the transmitter has proven the concept with electrical measurement results at par or better than the state of the art. It also demonstrated an on-body communication with an of the shelf receiver.

— **Body-Biased Switched Capacitor Circuits.** The body-biasing feature of the 28 nm FD-SOI technology has been extensively used in the proposed transmitter. The contribution and novelty of this work is the optimization of the switched-capacitor power amplifier by using forward body-biasing on the switches to reduce the ON-resistance while limiting their width, to reduce the dynamic power consumption. This work proposes new models for drain and system efficiency for body-biased switched-capacitor power amplifiers. It also introduces a preliminary simulation study of passive-mixers exploiting the same principle.

1.4.3 List of Publications

This PhD work has led to 4 publications in conference and journal venues :

— F. Solt, R. Benarrouch, G. Tochou, O. Facklam, A. Frappé, A. Cathelin, A. Kaiser, J. Rabaey, **"Energy Efficient Heartbeat-Based MAC Protocol for WBAN Employing Body Coupled Communication,"** *IEEE Access*, vol. 8, pp. 182966-182983, 2020.

Abstract : *Wireless Body Area Networks (WBANs) are a fast-growing field fueled by the number of wearable devices developed for countless applications appearing on the market. To enable communication between a variety of those devices, the IEEE 802.15.6 standard was established. However, this standard has some intrinsic limitations in addressing the heterogeneity of the network nodes in terms of activity, data rates (from less than bit/s to multiple Mb/s), energy availability, form factor, and location on, around or inside the body. To address these concerns, an alternative model is proposed that could serve as an extension of the IEEE 802.15.6 Standard. At its core is an adaptive and low-overhead synchronization scheme based on heartbeat sensing. This forms the base for a TDMA-based (Time Division Multiple Access) Media Access Control (MAC) protocol dedicated to multi-tier networks. While this effort focuses specifically on Capacitive Body-Coupled Communication (C-BCC), other physical layers can be easily incorporated as well. Based on these premises, this paper compares various random-access slot allocation approaches to accommodate the multiple data rates matching the system requirements, while incorporating a duty-cycling strategy anchored by heartbeat detection. This work proposes a novel, flexible, and robust solution, making use of heartbeat synchronization and addressing the corresponding challenges. It efficiently interconnects multiple device types over a wide range of data rates and targets a mesh of stars topology. At the cost of an increased communication latency, the proposed protocol outperforms the IEEE 802.15.4 MAC standard in terms of energy-efficiency by a factor of at least 12x in a realistic scenario.*

— G. Tochou, R. Benarrouch, D. Gaidioz, A. Cathelin, A. Frappé, A. Kaiser, J. Rabaey **"A Fully-Digital 0.1-to-27 Mb/s ULV 450 MHz Transmitter with sub-100 μW Power Consumption for Body-Coupled Communication in 28 nm FD-SOI CMOS,"** *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2021, *(Awarded Best Industry Paper, Ranked* 1^{st}*)*

Abstract : *A 0.5 V fully-digital 450 MHz transmitter for surface wave capacitive body-coupled communications is realized in 28 nm FD-SOI CMOS and consumes 17 to 76* μW *for data rates from 0.1 to 27 Mb/s with up to 14 % system efficiency. The heavily duty-cycled transmitter uses a 90 MHz free-running oscillator and edge combiners to generate OOK Gaussian-shaped pulses through a switched-capacitor PA. Body-biasing allows frequency tuning and adaptive efficiency optimization as a function of data rate.*

— G. Tochou, A. Cathelin, A. Frappé, A. Kaiser, J. Rabaey **"Impact of Forward Body-Biasing on Ultra-Low Voltage Switched-Capacitor RF Power Amplifier in 28 nm FD-SOI,"** *IEEE Transactions on Circuits and Systems II : Express Briefs*, vol. 69, no. 1, pp. 50-54, Jan. 2022.

Abstract : *The Switched-Capacitor Power Amplifier (SCPA) has become a key enabler for mo-*

dern wireless communication because of its high efficiency, high linearity, and high integrability.This paper discusses the impact of the extended Forward Body-Biasing (FBB) feature in 28 nm FD-SOI technology on Ultra-Low Voltage (ULV) SCPA. A new model of the Drain Efficiency (DE) and System Efficiency (SE) including body-biasing and drivers power consumption is introduced and validated with SpectreRF simulations. FBB on the SCPA improves by up to 14 % and 67 % the SE and transistors area, respectively, compared to a nominally body-biased SCPA under 0.5 V supply voltage at 2.4 GHz, while improving linearity and enhancing PVT variations.

— G. Tochou, R. Benarrouch, D. Gaidioz, A. Cathelin, A. Frappé, A. Kaiser, J. Rabaey **"A Sub-100 μW 0.1-to-27 Mb/s Pulse-based Digital Transmitter for the Human Intranet in 28 nm FD-SOI CMOS,"** *IEEE Journal of Solid-State Circuits*. IEEE, May 2022.

Abstract : *Human body communications require energy-efficient transceivers to connect diverse devices on the human body for wellness and medical applications. This paper presents a fully digital pulse-based transmitter (TX) for capacitive body-coupled communications (c-BCC) in 28 nm FD-SOI CMOS. The transmitter is operating at 450 MHz where surface wave (SW) propagation is the dominant mechanism of capacitive body coupled communication (c-BCC), offering a larger bandwidth with a more stable channel. The heavily duty-cycled transmitter uses a 90 MHz free-running oscillator and edge combiners to generate OOK Gaussian-shaped pulses through a switched-capacitor PA. Wide range forward body-biasing (FBB), specific to FD-SOI technology, allows frequency tuning and adaptive efficiency optimization as a function of data rate. The proposed transmitter consumes 17 to 76 μW for flexible data rates from 0.1 to 27 Mb/s (170 pJ/b down to 2.8 pJ/b) with up to 14 % system efficiency under 0.5 V supply voltage.*

1.5 Manuscript Structure

The manuscript is organized in seven Chapters. This chapter has introduced the concept of the Human Intranet with its associated challenges and research interests.

Chapter 2 presents the state of the art of wireless communications around the human body. It includes a study of the literature for common RF-based solutions, ultrasound, and body coupled communication mechanisms : magnetic, galvanic, and capacitive. All these options are evaluated and compared at the channel characterization level and at the integrated circuit design level.

Chapter 3 describes some system considerations for the design of the transmitter. According to the state of the art investigation, the physical layer is defined : frequency of operation, modulation, bandwidth, data rate, output power, and power consumption. This gives the specifications of the

transmitter.

Chapter 4 presents the design of the transmitter. Following the system specifications, a design of an ultra-low power, ultra-low voltage, and high data rate pulse-based transmitter in 28 nm FD-SOI technology is proposed. The chapter details the design techniques, the measurement results, an on-body demonstration and a comparison with the state of the art.

Chapter 5 presents the design methodology for ultra-low voltage switched-capacitor in FD-SOI technology. The chapter introduces a model of the drain and system efficiency for a body-biased switched-capacitor power amplifier. It also presents the impact of forward body-biasing on the linearity of the power amplifier.

Chapter 6 introduces some design considerations for the receiver. It includes a quick state of the art overview of low power receivers for ultra-wideband and narrow band wake-up receivers, and presents a preliminary study of the impact of forward body-biasing on passive mixers.

Finally, Chapter 7 concludes this manuscript summarizing the thesis work and introduces some ideas for future work.

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Chapter 2

State of the Art

Contents

This Chapter presents the proposed techniques and hardware implementations in the state of the art to communicate efficiently on the human body and how they comply with the Human Intranet requirements.

2.1 RF Transmitters

2.1.1 Bluetooth Low-Energy

Bluetooth Low-Energy (BLE) is the most commonly used radio technology for wearables and personal IoT. This is probably the first strength of BLE. It is a widely used standard making the nodes easily compatible with a broad range of existing devices. The proposed Transmitter (TX) in [1] is one of the most energy and power-efficient BLE implementation with the smallest form-factor of the state of the art. This solution proposes an architecture based on a power oscillator with a printed inductive loop antenna and an on-chip digitally switched-capacitor array forming a high-Q resonator. This allows reducing the power consumption compared to a typical architecture with PLL+PA which typically drives up the power consumption to more than 3 mW. A sub-0.5 mW BLE transmitter has been achieved in [2] using such an architecture by using an All-Digital PLL (ADPLL) and a switched-capacitor digital PA. However, this comes at the cost of degraded performances in terms of frequency deviation and phase noise, due to the low-power ring-oscillator.

Designing power-efficient PA at low output power (< 0 dBm) is challenging. A transformer-boost power oscillator (Fig. 2.1a) is proposed to remove the PA from the front-end. It also allows to reach a very low level of phase noise (− 118.5 dB/Hz @ 1MHz offset) and low-frequency deviation (< 10 kHz) resulting in a low FSK modulation error (< 2.1 %). Finally, a compact ADPLL (Fig. 2.1a) realizes fast center frequency settling (< 15 μs), operates only during frequency settling, and is powered off when transmitting. This avoids the use of power-consuming, always-on, PLL.

This implementation achieves an overall power consumption of 606 µW for a − 8.4 dBm output

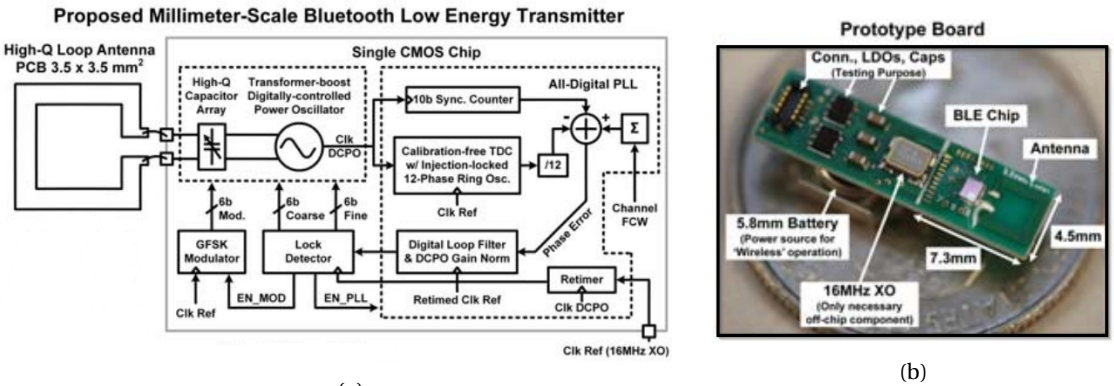


FIGURE 2.1 – (a) Example of BLE transmitter and (b) prototype board (Taken from Shi et al. [1])

power (23.6 % power efficiency) in a $4.5 \times 18.6\ mm^2$ fully self-contained board. The power oscillator consumes 88.2 % of the power with 28 % efficiency. The only external component necessary is the 16 MHz crystal oscillator. It is observable in Figure 2.1b that such crystal oscillator is the major area consumer, and its power consumption is not taken into account into the reported overall power consumption, although its power consumption is typically between 30 to 100 µW [3, 4].

If such implementation is pushing the limit of power consumption and form-factor, it still does not meet all the requirements for an efficient Human Intranet network. First, the data-rate of BLE is fixed and limited to 1 Mb/s (up to 2 Mb/s in the latest standard version), which is not compliant with a lot of sensors/actuators applications and lacks flexibility. Secondly, *body shadowing* effect will degrade significantly the link budget. For line-of-sight communication, BLE is capable of communicating around 10 meters (8 meters is reported in [1], with − 8.4 dBm output power and the printed antenna and an off-the-shelf Bluetooth receiver). However, for an on-body or around-body communication, the human body absorbs the signal and degrades the path loss (Fig. 2.2), e.g. for a torso to back communication. Then, to overcome such effect, it would require to : increase the output power of the transmitter, improve the sensitivity of the receiver, use a larger gain antenna, or use repeaters. Such solutions would inevitably increase the power consumption or downgrade the wearability of the sensors.

To demonstrate this issue, Fort et al. [6] realized near torso measurement and a statistical model for communication in the 915 MHz and 2.45 GHz Industrial, Scientific and Medical (ISM) bands associated with Zigbee and Bluetooth. It is observable in Figure 2.3 that the path loss for around-body communication is exceeding 70 dB beyond a 25 cm distance at 2.4 GHz. Where for a line-of-sight communication the path loss can be modeled as :

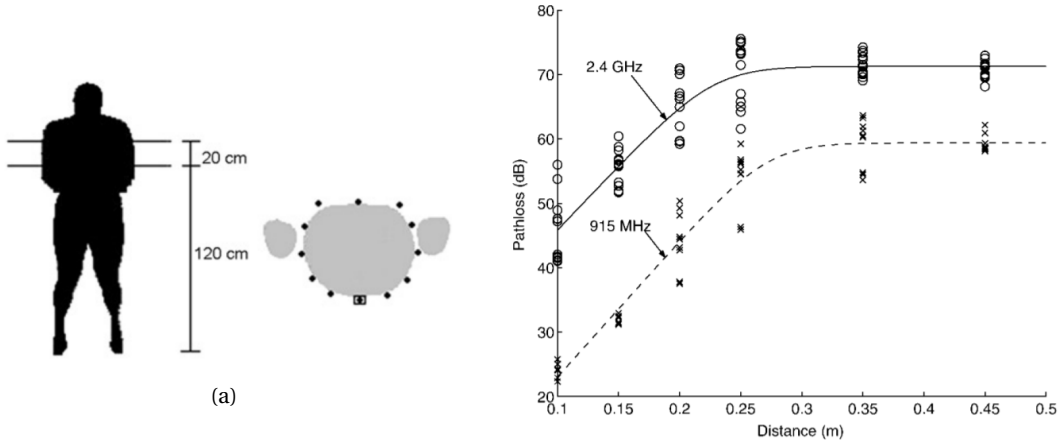
$$\mathrm{PL}_{(d\mathrm{B})} = 20 \cdot log_{10}\left(\frac{4 \cdot \pi \cdot d \cdot f}{c}\right) \tag{2.1}$$

Where d is the distance between the receiver and the transmitter, f is the frequency and c is the

(a) (b)

FIGURE 2.2 – Illustration of body shadowing on wireless transmission between sensors : (a) Line-of-sight, successful transmission ; (b) body shadowing that affects transmission (Taken from Januszkiewicz [5])

speed of light. Then, for a 2.4 GHz frequency at 50 cm the path would correspond to roughly 35 dB path loss. And a 70 dB path loss would correspond to a 30 meters line-of-sight communication.



(a) (b)

FIGURE 2.3 – (a) Measurement locations around the body (b) Measured pathloss for ISM around the body (Taken from Fort et al. [6])

2.1.2 Ultra-Wide Band

Another solution using RF propagation is widely studied for BAN : Ultra-Wide Band (UWB). This technology has the advantage to be able to reach high data rates and to be very energy-efficient. The principles of UWB lie in pulse-based communication. Each bit is transmitted by a short-time pulse allowing bit-level duty cycling for reduced power consumption, especially at low data rates. A communication is considered UWB when the bandwidth of the signal is more than 500 MHz or when the fractional bandwidth is more than 20 %. To use such large bandwidth, UWB usually operates in the 3-10 GHz frequency band. Simple modulations are mainly used such as On Off Keying (OOK), Pulse Position Modulation (PPM) and Binary Phase Shift Keying (BPSK). OOK and PPM allow for the use of non-coherent receivers which reduces the constraints and power consumption by using PLL-free architecture.

G. de Streel et al. [7] proposed a UWB transmitter compliant with the IEEE 802.15.4a standard specifying defines the operation of UWB wireless personal area networks (WPANs). It uses FD-SOI technology permitting low threshold voltage (V_t) through Forward Body Biasing (FBB) and hence ultra-low voltage operation at 0.55 V. FBB also enhances Process Voltage Temperature (PVT) variations, tunes the carrier frequency (f_c) and output power. The architecture is based on a free-running, body-biased controlled, ring oscillator and a current Digital to Analog Converter (DAC) acting as a power amplifier permitting a digital Gaussian pulse shaping (Fig. 2.4). The transmitter is aggressively duty-cycled for high energy-efficiency where both the oscillator and PA are enabled only while the burst pulse is emitted.

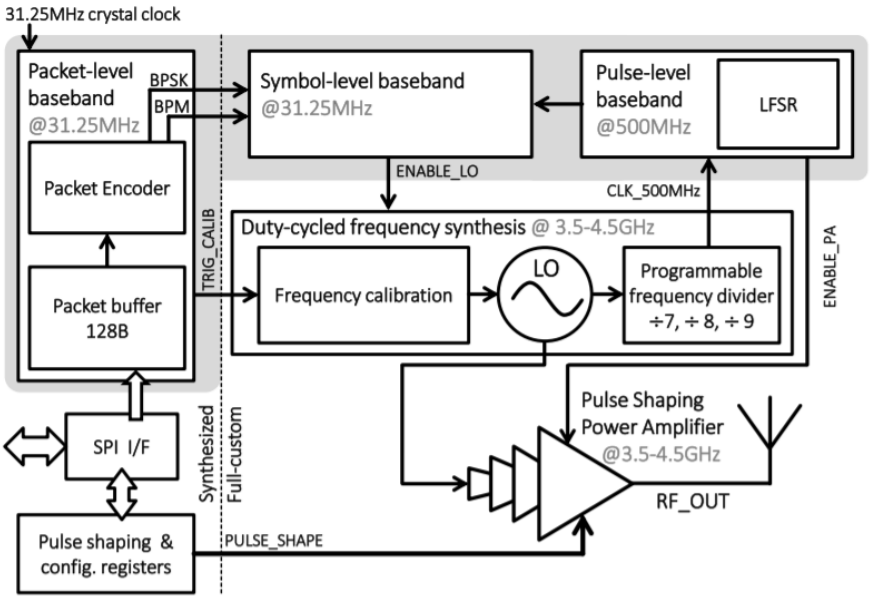


FIGURE 2.4 – Example of an UWB transmitter proposed by de Streel et al. [7]

The transmitter (TX core only) reaches a best-in-class energy-efficiency of 14 pJ/b at the maximum data rate (dictated by the IEEE 802.15.4a standard) of 27 Mb/s for a -20 dBm output power. At the lowest data rate of 100 kb/s the transmitter consumes 100 µW corresponding to a 950 pJ/b energy-efficiency. Including the fully System-on-Chip (SoC) power the transmitter consumes 650 µW at the maximum data rate.

Free-running Ring Oscillator

LC-based oscillators can offer good jitter performances but at the cost of high power, large area, and large settling time. To avoid these drawbacks, previous low-power TX relied on duty-cycled Ring-Oscillator (RO). However this solution suffers from higher jitter compared to LC-based solutions. A differential RO is used as they have better jitter performances compared to inverter-based, single-ended RO and enables simple BPSK modulation. They further improve the jitter by optimizing the oscillator with FBB-based frequency tuning, avoiding current starving in the LO. FBB is used to control the threshold voltage and, hence, the delay of the RO elements and to tune the carrier frequency to the selected channel. Moreover, it uses a differential multiple-pass RO based on feed-forward loops. The seven-stage architecture improves both the switching speed as well as the noise performance thanks to its fast transitions. The body-biased controlled oscillator consumes 180 µW when operating at 4.5 GHz featuring -102 dBc/Hz phase noise at 30-MHz offset, corresponding to a 17 ps jitter for a 32 ns runtime.

Pulse Shaped Digital Power Amplifier

One of the major constraints in UWB is compliance with Federal Communication Commission (FCC) regulations. The emitted power of a UWB transmitter must not exceed -41 dBm/MHz in the 3.1 – 10.6 GHz band, limiting the output power of UWB transmitters. The most constraining is the notch in the 960 MHz – 1.6 GHz band (GPS band) where the out-of-band emission power should not exceed -75.3 dBm/MHz [8] (Fig. 2.5). Hence, when emitting in the 3.1 – 10.6 GHz band the sidelobes of the emitted spectrum are to be carefully engineered to avoid any violation of the FCC regulation. G. de Streel et al. [7] proposed a pulse shaping technique allowing to attenuate the side-lobs. To do so, a Gaussian pulse shaping is applied thanks to a digital power amplifier and two ring counters clocked by the two differentials phases of the RO reproducing a $2 \times f_c$ sampling rate, enabling the PA slices depending on the digitally configured pulse shaping.

SoC Integration

This solution is very complete as it describes a full SoC implementation. Power management is done with a 1.2 to 0.55 V DC-DC converter and the body-bias voltages of +/- 1.8 V are generated on-chip using DACs and charge pumps. The only required external component is a 31.25 MHz frequency reference for periodic calibration of the RO frequency.

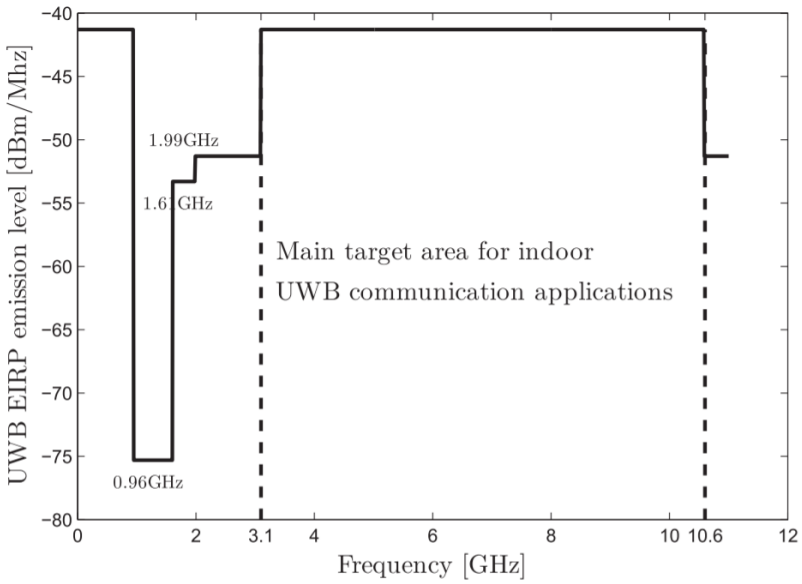
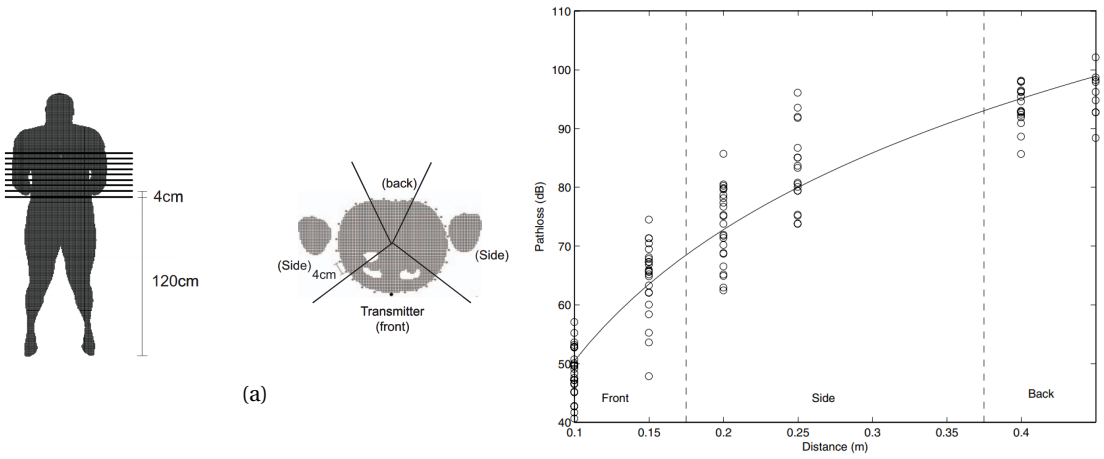


FIGURE 2.5 – UWB spectral mask (Taken from Yajnanarayana et al. [8])

If UWB resolves the data-rate issue compared to BLE, it still suffers from the body shadowing effect described earlier. Fort et al. [9] modeled and measured the path loss for a UWB communication around the human body (Fig. 2.6). With similar scenarios as [6] (Fig. 2.6a), the path loss is measured around the torso at different distances. The path loss is roughly equal to 100 dB for a 50 cm distance (torso to back). We can observe that the path loss is more important than the path

loss for ISM bands (Fig. 2.3b) mainly because of the higher carrier frequency and multipath. Furthermore, it is more challenging to reach high sensitivity for UWB receivers because of their large bandwidth and the output power of the transmitters is limited by the FCC regulations, reducing the link budget.



(a) (b)

FIGURE 2.6 – (a) Measurement locations around the body (b) Measured pathloss for UWB around the body (Taken from Fort et al. [9])

2.2 In-body Ultrasound

As the human body is mostly composed of water, ultrasounds propagate easily in the human body. Hence this communication technique has been recently studied for human body communication. However, the channel suffers from multipath caused by the reflections of the heterogeneous medium composed of muscle, bone, and skin material [10]. Furthermore, similarly to

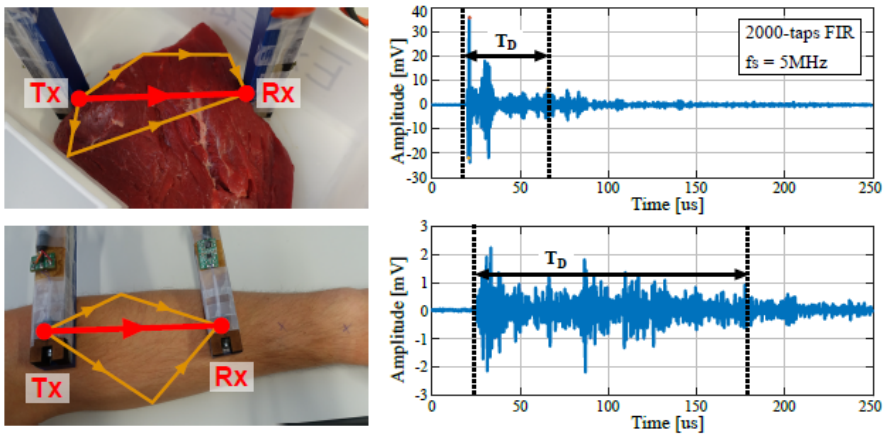


FIGURE 2.7 – Characterization of realistic in-body finite impulse responses (FIRs). Left : pictures of the two different channel types with illustration of the main and secondary propagation paths (respectively red and orange lines). Right : corresponding FIR of both channel types, with highlighting of the multipath delay spread TD (Taken from Bos et al. [10])

electromagnetic communication, losses increase with the frequency which limits the central frequency of the transducers to ~10 MHz. This frequency limitation inherently restrains the bandwidth and hence the communication data rate [10].

An ultra-low-power transceiver implementation with a low data rate has been presented in [11]. Although this design was more meant for in-water or over-the-air communication rather than for intra-body communication, it gives an idea of the achievable power consumption and energy-efficiency of an on-chip ultrasound transceiver. It achieves a total power consumption of 51.18µW (50µW for the TX and 1.18µW for the Receiver (RX)) when communicating at 1 kb/s. This corresponds to a total energy-efficiency of 51.18 nJ/b. This energy-efficiency could be improved by reducing the important TX power consumption when adapted to intra-body communication where the targeted distances are smaller, although more sensitive to multipath. Ultrasound remains a good communication option for short-range implants (under-skin) to on-body (on-skin) communication with a low data rate.

2.3 Body-Coupled Communication

To overcome the *body shadowing* effect, a recently studied alternative solution is Body-Coupled Communication (BCC). This solution proposes to use the human body as a communication channel instead of free-space. Three different mechanisms have been mainly studied so far in BCC [12] (Fig. 2.8) :

— Magnetic Body-Coupled Communication (m-BCC)

— Galvanic Body-Coupled Communication (g-BCC)

— Capacitive Body-Coupled Communication (c-BCC)

In the following subsections, the three mechanisms principles, and challenges will be described and different physical implementation examples for each mechanism will be presented.

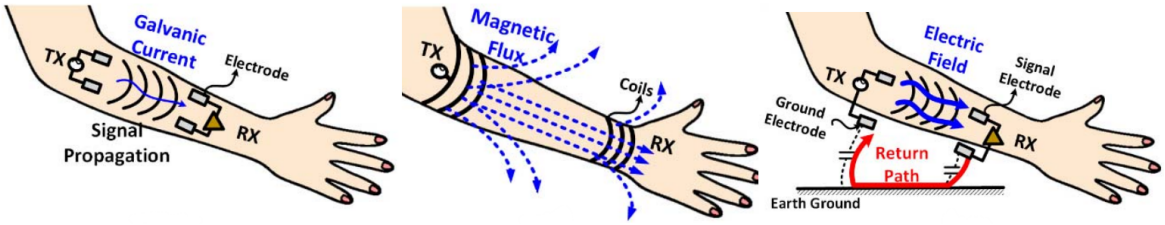
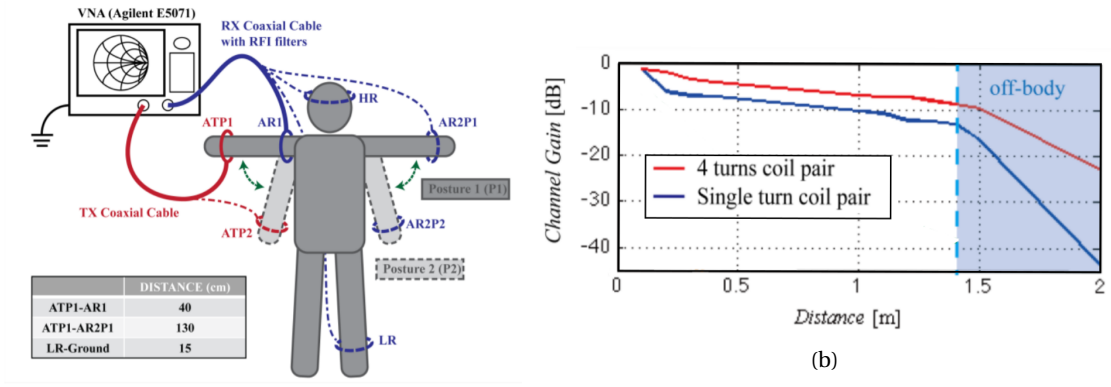


FIGURE 2.8 – BCC mechanisms : Galvanic, Magnetic Resonance and Capacitive coupling (from left to rigth). (Taken from Yoo [12])



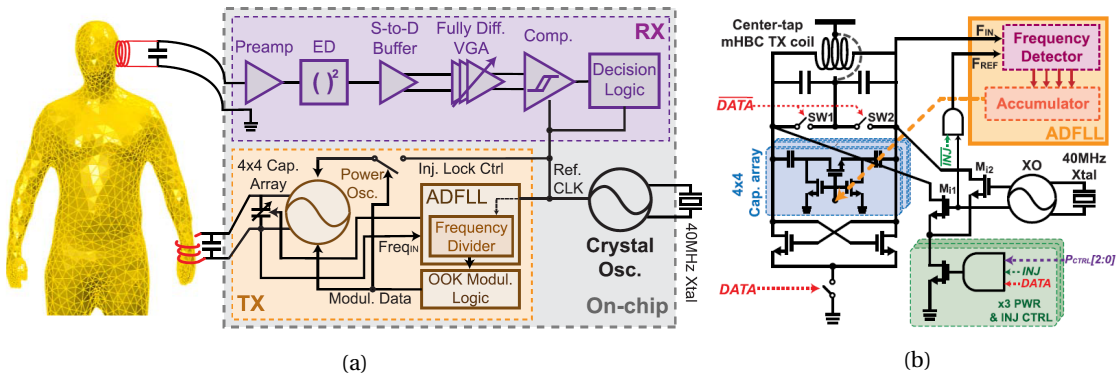
(a) (b)

FIGURE 2.9 – (a) Measurement setup (b) Path loss measurement for magnetic BCC (Taken from Park and Mercier [13])

2.3.1 Magnetic Body-Coupled Communication

Magnetic-BCC uses resonant coils wrapped around body limbs to communicate through a magnetic field. Magnetic fields travel with low loss through biological tissue, as the human body is magnetically inert [13] (Fig. 2.9). Hence, if the magnetic resonance is kept constant, magnetic coupling reaches low path loss with all body coverage. However, coils wrapped around the body are not easily wearable. For example, having a coil around the head or the torso is not convenient. Furthermore maintaining magnetic resonance is sensitive to motion artifacts. It remains a good communication option if both the receiver and transmitter are on the same limb with light coils.

Park and Mercier [15] proposed a transceiver using m-BCC, for wrist-to-ear communication targeting audio application (Fig. 2.10a). The transmitter uses a power oscillator to generate the 40 MHz carrier frequency using the coil as the resonator. The transceiver aims to communicate at 5 Mb/s using OOK modulation. With a high-Q resonator (around 50) the data rate is typically limited to less than 1 Mb/s. To increase the data rate, two transistors SW1 and SW2 (Fig. 2.10b) are used to shunt the inductor current during transmissions of logic '0's. When transmitting lo-



(a) (b)

FIGURE 2.10 – (a) Example of magnetic BCC transceiver architecture (b) Transmitter schematic (Taken from Park and Mercier [14])

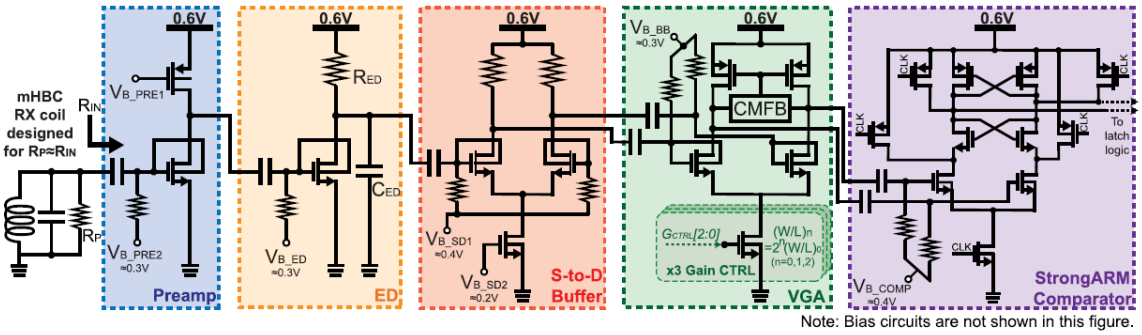


FIGURE 2.11 – Example of receiver schematic for magnetic BCC (Taken from Park and Mercier [14])

gic '1's, Mi1 and Mi2 are used as injection transistors to rapidly start-up oscillations (Fig. 2.10b). Injection locking is used with an external crystal at 40 MHz for fast kick-start with an All Digital Frequency Locked Loop (ADFLL) for synchronous injection. The ADFLL also allows enhancing frequency matching between TX and RX.

On the receiver side, an envelop detector principle is used. It comprises 5 different blocs (Fig. 2.11) : a common-source based pre-amplifier, an envelop detector, a single to differential buffer, a Variable Gain Amplifier (VGA), and finally a comparator. Such non-coherent receiver architecture allows reaching low power consumption.

As a performance summary, the TX consumes 35.8 µW, including the 17.2 µW crystal oscillator power consumption, at -24.8 dBm output power. At -56 dBm sensitivity, the RX consumes 23.5 µW (also including the crystal oscillator power). This corresponds to a 7.2 pJ/bit and 4.7 pJ/bit energy-efficiency at 5 Mb/s, for the transmitter and receiver, respectively.

2.3.2 Galvanic Body-Coupled Communication

The second option for BCC is galvanic coupling. This communication scheme uses two electrodes on both the transmitter and the receiver. The principle is based on a differential signal creating a galvanic current propagating through the skin. The galvanic coupling has the advantage to be very robust to environment changes due to a very stable channel. However, it suffers from strong path loss beyond a few centimeters [16]. As observable in Figure 2.12, the path loss is around 60 dB for a communication distance of 15 cm for a frequency of operation of 100 kHz. Furthermore, such a low frequency of operation limits the usable bandwidth. Thus, this makes g-BCC a good candidate for implant (under-skin) to on-body (on-skin) communications but makes full-body coverage communication unachievable.

Jeon et al. [17] proposed a transceiver for an implant to on-skin communication. To be able to communicate at a high data rate, this implementation proposes to use a termination at the receiver of 100 Ω parallel to the body impedance. This termination allows to flatten the chan-

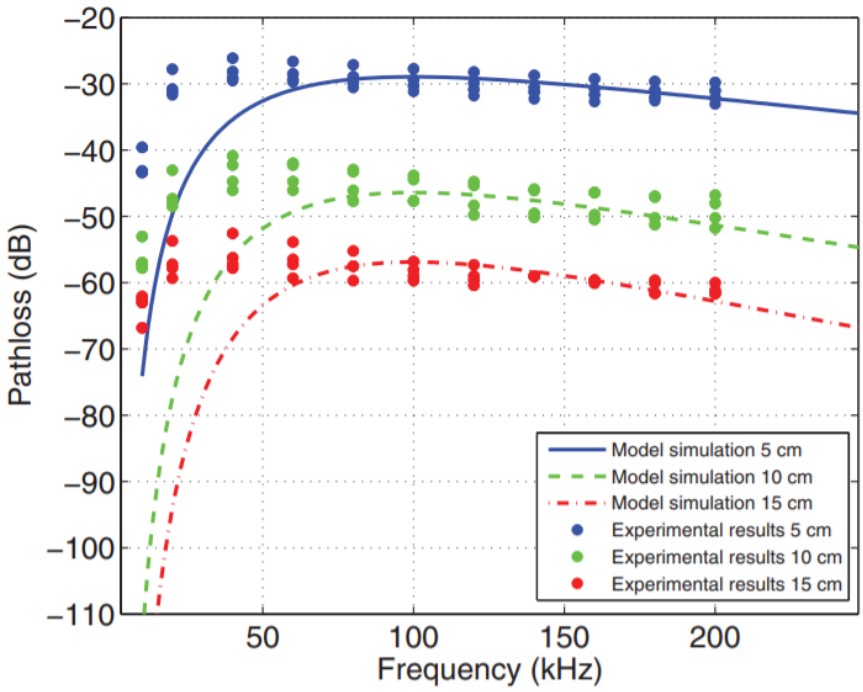
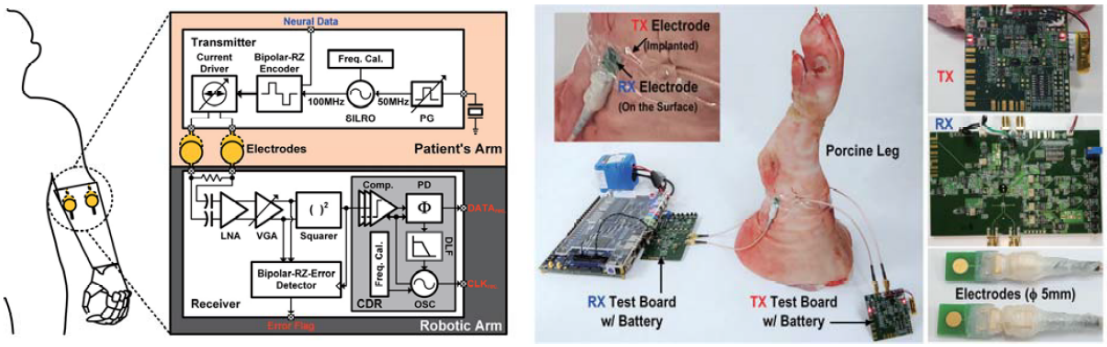


FIGURE 2.12 – Path loss for galvanic body coupled communication (Taken from Callejon et al. [16])

nel response and hence to increase the bandwidth and data rate. The transmitter is based on a direct-baseband transmission, where a subharmonic injection-locked ring oscillator generates the 100 MHz clock from the 50 MHz external crystal. The data is then simply modulated through a bi-polar encoding and buffered to the electrodes using a current driver.

The receiver is based on an analog front end and a clock and data recovery in the digital domain. To filter low-frequency signals including biosignals, the input of the receiver is AC-coupled. Then the received signal is amplified through an LNA and VGA before being squared. The clock and data recovery are then made in the digital domain.

The transceiver achieves a power consumption of 0.475 mW and 2.68 mW for the transmitter



(a) (b)

FIGURE 2.13 – (a) Example of galvanic BCC transceiver (b) In-vitro demonstration set-up (Taken from Jeon et al. [17])

and receiver, respectively, at a 100 Mb/s data rate. The communication is demonstrated with an in-vitro experiment on a porcine leg with the TX electrodes implanted (Fig. 2.13b) with a 10^{-9} Bit Error Rate (BER).

2.3.3 Capacitive Body-Coupled Communication

Capacitive body coupled communication has first been introduced by Zimmerman [18] in 1996. The principle is based on one electrode in contact with the skin at the TX and RX side, with a floating electrode on each side acting as groundselectrodes. The signal propagates along the body as an electric field. The return path is formed by the ground and air environment creating a capacitive coupling between the transmitter and the receiver (Fig. 2.8).

Bae et al. [19] proposed an extensive study on the signal propagation mechanism of capacitive BCC. By deriving Maxwell's equations and considering the on-body electrode as an infinitesimal dipole (Fig. 2.14), the magnitude of the electric field along the human body (z axis) can be expressed as :

$$| \mathrm{E}_z | = 2 \, | \, k \cdot \mathrm{S} \cdot \frac{1}{r} + i \cdot \frac{1}{r^2} - \frac{1}{k} \cdot \frac{1}{r^3} \, | \tag{2.2}$$

Where k is the wavenumber, S is a term that depends on the frequency and the dielectric properties of the conducting surface, and r is the distance from the source. Three parts can be identified. The first term in $1/r$ corresponds to the far-field propagation in combination with attenuation factor S, which corresponds to a surface wave propagation. The second and third term, in $1/r^2$ and $1/r^3$, corresponds to reactive radiation (i.e. induction field) and electro quasi-static coupling (i.e. near-field coupling), respectively.

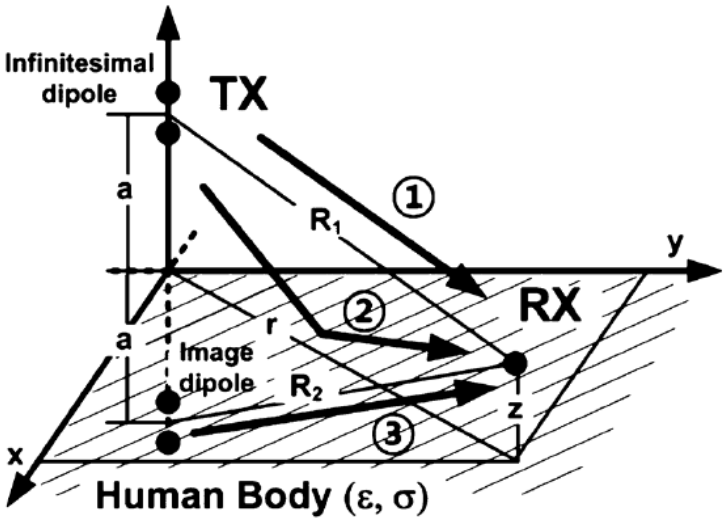
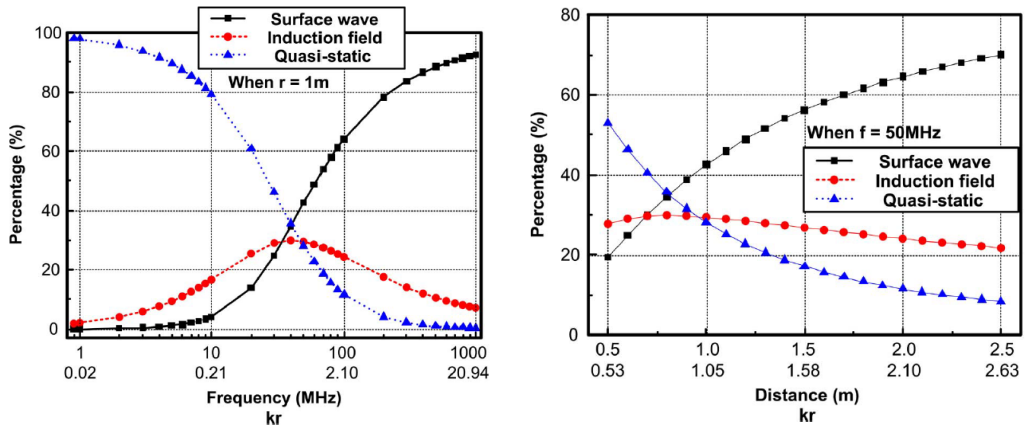


FIGURE 2.14 – Electric field from dipole and its geometry on the human body (Taken from Bae et al. [19])

Hence, the dominant propagation mechanism in capacitive body coupled communication depends on two parameters : frequency (wavenumber k) and distance (r). For a higher frequency and/or longer distance the dominant propagation mechanism is the surface wave propagation. On the other hand, the closer the receiver will be from the source or the smaller the frequency becomes, the quasi-static coupling will become the dominant mechanism (Fig. 2.15).

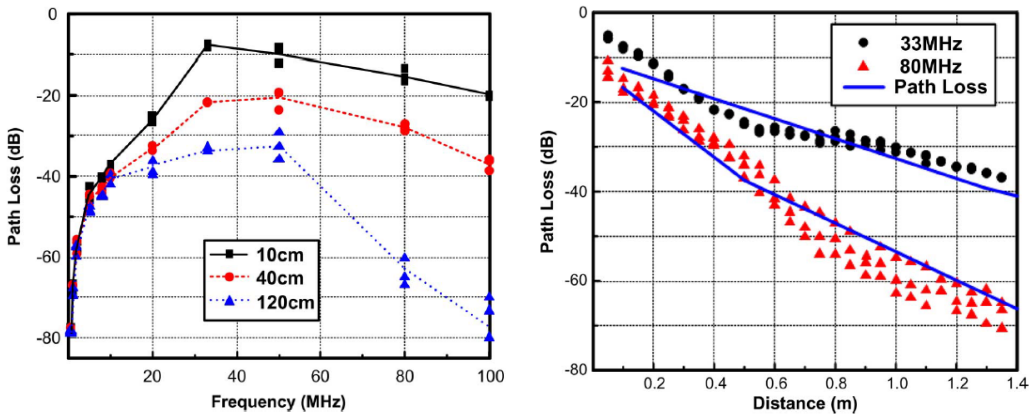
Bae et al. [19] also proposed to study the path loss of capacitive BCC from 1 to 100 MHz (Fig. 2.16). Capacitive body coupled communication with a frequency of operation below 100 MHz offers low path loss for a distance up to 1.5 m. However, because of the important influence of the return path on the channel, the communication can become very unstable with changing environment and motion.

In another hand, Thielens et al. [20] and Benarrouch et al. [21] proposed to study the channel of the capacitive body coupled communication where the surface wave is the dominant mechanism of propagation in the 400-500 MHz band. Indeed, being able to use higher frequency will result in a larger usable bandwidth which will allow for an increase of the data rate of the communication. Furthermore using surface wave propagation is less dependent on the return path by nature. Measuring the channel of capacitive body coupled communication is challenging. As the channel response is highly dependable on the return path, the direct use of a Vectorial Network Analyzer (VNA) is not possible. This is because the ground electrodes of the receiver and the transmitter will be directly connected to the measurement equipment and hence idealize the channel behavior. In Bae et al. [19], baluns are used to isolate the ground electrodes from the measurement equipment to avoid such an effect. Though a balun can conveniently separate TX and RX from the ground and each other, it can be coupled to the ground with a capacitance of approximately 2 pF, which is more heavily coupled than real environment [19]. To overcome this issue, and to



(a) (b)

FIGURE 2.15 – Contribution ratio of each mechanism in terms (a) frequency and (b) distance (Taken from Bae et al. [19])



(a) (b)

FIGURE 2.16 – Path Loss vs (a) frequency and (b) distance (Taken from Bae et al. [19])

be closer to what a real on-body communication will give, the measurement method in [20, 21] used a battery-powered transmitter and receiver where the transmit output power is set to 0 dBm and the Received Signal Strength Indicator (RSSI) is taken at the receiver to calculate the path loss. Hence in [21] a model of the channel path loss is proposed in the 400-500 MHz and validate with simulation and measurements.

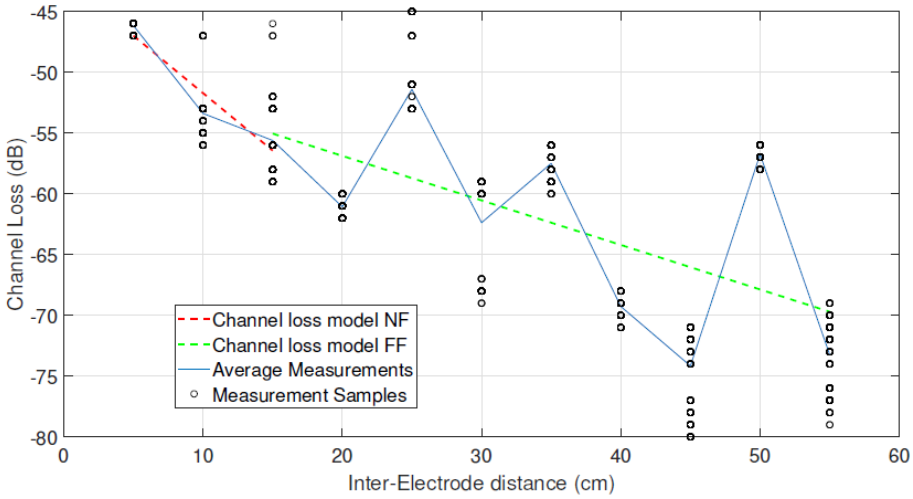
The channel can be modeled with a near-field model for a distance up to 15 cm and with a far-field model for further distance. The path loss in the near field (0.79 - 2.1 dB/cm) is higher than in the far-field (0.19 - 0.45 dB/cm) (Fig. 2.17a). Furthermore, as observable in Figure 2.17a the channel response remains very flat over the 420-510 MHz frequency band.

Many transceiver implementations have been proposed in the state of the art using capacitive body coupled communication [22–29]. All of them use the Electro Quasi-Static (EQS) propagation mechanism with a frequency below 150 MHz. Cho et al. [23], Zhao et al. [29] proposed transceivers compliant with the IEEE 802.15.6 standard section dedicated to human body communication. In this standard section, the frequency of operation is defined at 21 MHz with a 3 dB bandwidth of 5.25 MHz. Such low frequency of operation and bandwidth limits significantly the maximum achievable data rate to a few Mb/s. Maity et al. [24], Lee et al. [28] proposed transceivers with direct-baseband communication with up to 30 Mb/s and 150 Mb/s. Such solutions allow for the use of simple buffers at the transmitter side and defer the complexity at the receiver. Although both solutions report high energy-efficiency below 20 pJ/b, the reported power consumption does not take into account the clock generation power consumption which will be the most power-consuming part.

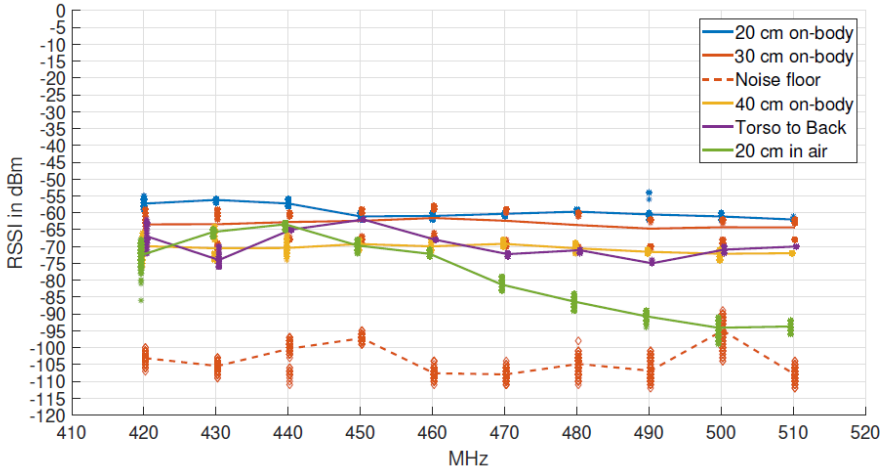
Cho et al. [22] proposed a dual-transceiver being able to communicate efficiently at both high (80 Mb/s) and low data rates (100 kb/s) (Fig. 2.18). The high data rate transceiver uses a dual-band communication with BPSK modulation in the 20-60 MHz and 140-180 MHz bands to avoid

FM-band interferences (80-100 MHz). The transmitter is based on a Wien-bridge oscillator with an integer-1 PLL generating the 160 MHz frequency. A 40 MHz crystal external oscillator directly generates the second frequency band and serves as a reference for the PLL. The two signals at 160 MHz and 40 MHz are summed after being modulated and transferred to a driver (Fig. 2.18c). The receiver uses a common source LNA and a dual-path Costas shared-loop which allows to reduces area and power consumption compared to two different receivers for each band without hardware sharing (Fig. 2.18d). The low data rate transceiver operates at 13.56 MHz frequency. The data is transmitted directly in baseband through a programmable inverter-based driver in OOK modulation. The receiver is based on a super-regenerative architecture with an RC-oscillator which consumes less power and area than a typical LC-oscillator (Fig. 2.18b).

To summarize the performances. The high data rate transmitter consumes 2.6 mW at 80 Mb/s (32.5 pJ/b) with a 79 pJ/b receiver (6.3 mW). For the 100 kb/s low data rate transceiver the trans-



(a)



(b)

FIGURE 2.17 – (a) Path Loss model and measurements at 450 MHz and (b) Measured RSSI (path loss) in the 420-510 MHz band (Taken from Benarrouch et al. [21])

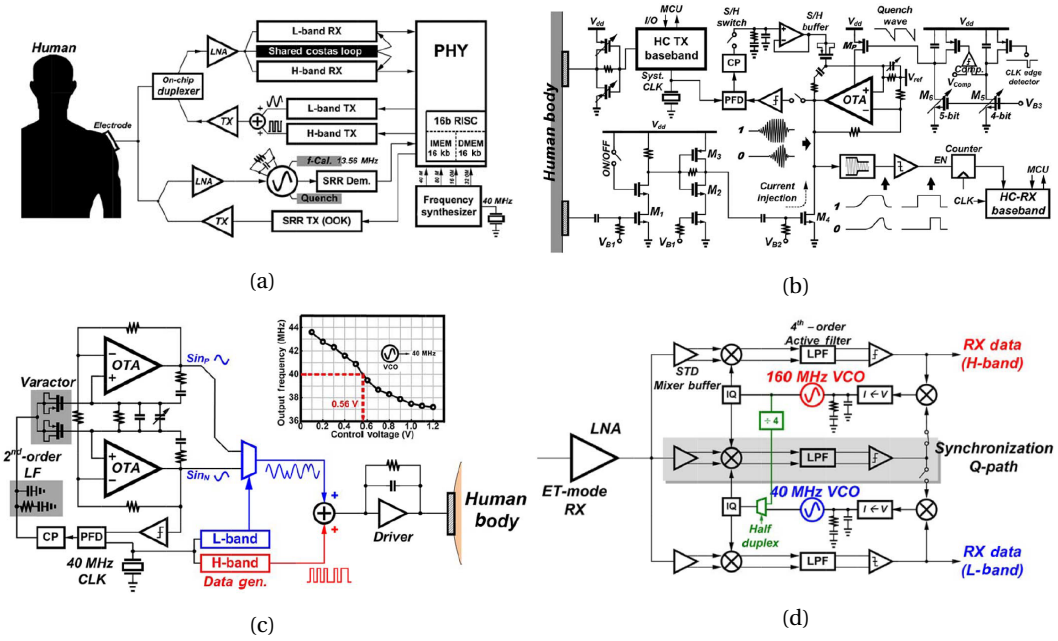


FIGURE 2.18 – (a) Overall transceivers architectures (b) 100 kb/s transceiver (c) Dual-band 80 Mb/s TX (d) Dual-band 80 Mb/s RX (Taken from Cho et al. [22])

mitter and receiver draws 21 µW (210 pJ/b) and 42.5 µW (425 pJ/b) from the power supply, respectively.

2.4 Comparison and Preferred Solution

The comparison of the different presented communication technology is summarized in Table 2.1. And a visual comparison of the existing implementations for the different presented technologies is observable in Figure 2.19. If UWB allows reaching much higher data rates than BLE with more flexibility and energy-efficiency, it still suffers from the body shadowing effect inherent to RF-based solutions, significantly degrading the channel for around-body communication. Furthermore, the antenna form factor can be a real challenge to make the nodes wearables with acceptable gain.

To overcome such issues body-coupled communication has been studied. Magnetic body cou-

Techno	BLE	UWB	Ultrasound	m-BCC	g-BCC	c-BCC eqs	c-BCC sw
Data Rate	1-2 Mb/s	0.1-1000 Mb/s	<1 Mb/s	Up to 5 Mb/s	Up to 100 Mb/s	Up to 150 Mb/s	>100MHz (available BW)
Form Factor	Narrowband Antennas	Wideband Antennas	Transducers	Around-limbs coils	2 electrodes on-skin	1 electrode on-skin	1 electrode on-skin
Energy-Efficiency order	~1 nJ/b	~10 to 1000 pJ/b (high and low data rate)	10-100 nJ/b	~10 pJ/b	~10 pJ/b	~10 pJ/b	To be defined
Range/ Body Coverage	~10 m (line of sight)	<10 m (line of Sight)	~10 cm intra-body	>2 m on-body	<15 cm on-body	>1.5 m on-body	Potentially up to 50 cm
Robustness	Sensitive to Body Shadowing	Sensitive to Body Shadowing	Sensitive to Multipath	Sensitive to coils resonance and motions	Very Stable	Sensitive to environment changes	Mildly sensitive to environment changes

TABLE 2.1 – Comparison of communication candidates for the Human Intranet

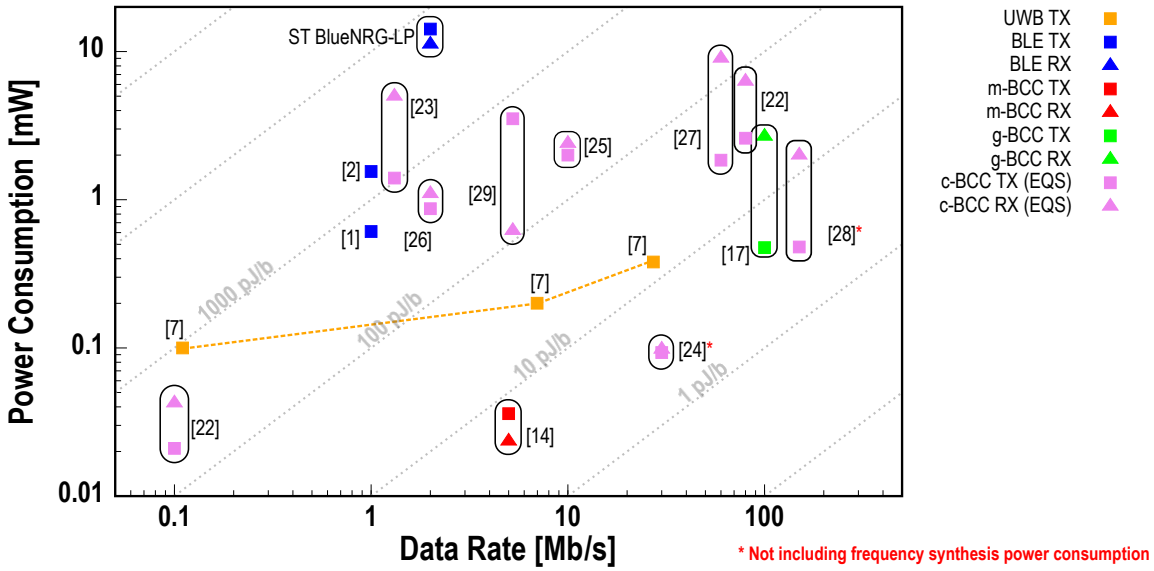


FIGURE 2.19 – State of the art comparison of TRX (power consumption vs data rate)

pled mechanism offers the best path loss per unit of distance. However, the usage of coils limits the wearability to arms and legs, as wearing coils around the head or torso is not convenient. Furthermore, the trade-off between pathloss, coils Q-factor, and bandwidth limits the data rate to a few Mb/s. Secondly, galvanic body coupled communication offers a very stable channel but with strong path loss beyond a few centimeters, making it merely usable for implants to on-skin communication. Finally capacitive coupling mechanism allows long-range communication with only 1 electrode per transmitter/receiver attached to the human body with high data rate capability. Hence, this makes capacitive coupling the best candidate for the Human Intranet network. However, using capacitive coupling in the quasi-static mode brings a limited bandwidth and unstable channel due to the return path dependencies.

The surface wave propagation mechanism has been further studied to increase the bandwidth availability and to be less sensitive to the return path. If the path loss appears to be much higher in the 400-500 MHz band (Fig. 2.17b) than EQS propagation (Fig. 2.16), it is mainly due to the insertion loss of the electrodes. Hence, by matching the capacitive electrodes to the TX impedance, the path loss could be significantly improved. Additionally, surface wave propagation offers the same loss per distance (19-45 dB/m [21]) as c-BCC EQS (38 dB/m[19]) with a larger available bandwidth Hence a capacitive BCC in the 400-500 MHz band using surface wave as the dominant mechanism appears to be the best solution to investigate to meet all the requirements of the Human Intranet.

2.5 Conclusion

The state of the art for body area network uses different communication technologies. Among common RF-based technology BLE does not meet the data rate requirements and UWB suffers

from body shadowing effect, degrading the path loss and making the communication unstable. Body coupled communication has been proposed to overcome the body shadowing effect by using the human body as the propagation medium. Three BCC mechanisms have been studied with transceivers implementations : magnetic, galvanic, and capacitive. Magnetic BCC offers a low path loss but requires bulky on-body coils. Galvanic BCC does not enable communication beyond 15 cm and is only applicable for implant to on-skin communication. Capacitive coupling, offers the smaller form-factor with only one attached electrode on-body, while offering a low-path loss channel. However the state of the at is focusing on quasi-static coupling where the frequency is below 200 MHz, which limits the available bandwidth and is sensitive to environment changes because of the important impact of the return path on the channel.

To overcome these challenges, the surface wave propagation mechanism has been further studied to increase the bandwidth availability and to be less sensitive to the return path. This comes at the cost of a slightly higher path loss than quasi-static coupling but still allows long-range on-body communication up to 50 cm. However, no hardware implementations have been proposed yet to confirm those statements. Hence, the main goal of this thesis is to further explore capacitive body-coupled communication with surface wave propagation by proposing a transmitter physical implementation.

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Chapter 3

System Specifications and Hardware Considerations

Contents

3.1 Pulse-based Communication

According to the channel studies in the 400 − 500 MHz band for c-BCC [1, 2], pulse-based communication allows for wide bandwidth > 100 MHz and more channel stability under motion and changing environment. Taking advantage of the wide available bandwidth, the TX is inspired by UWB principles with the use of pulse-based communication with simple modulation such as OOK or BPSK . Pulse-based communication can handle aggressive duty-cycling allowing for low power consumption and the ability to reach high data-rates.

3.1.1 Bandwidth Data rate Trade-off

From the analysis in [3], the trade-off between Bandwidth (BW) and maximum data rate is defined. The temporal expression of a pulse centered at the frequency f_c with a Gaussian envelope can be written as :

$$p(t) = \mathrm{A}\exp\left(-\frac{t^2}{2\sigma^2}\right)\cos(2\pi f_c t) \tag{3.1}$$

where A is the maximum amplitude of the pulse and σ the standard deviation of the Gaussian envelope. In the frequency domain, the single side-band Fourier transform of (3.1) gives :

$$\mathrm{P}^+(f) = \mathrm{A}\sqrt{\pi}\sigma\exp\left(-\frac{(2\pi\sigma(f-f_c))^2}{2}\right) \tag{3.2}$$

The trade-off between the pulse width (T_p =∼ 6σ), and hence the maximum Pulse Repetition Frequency (PRF) (PRF =∼ 1/6σ), and the BW at −10 dBc is given by solving :

$$10\log_{10}\left(\frac{|\mathrm{P}^+(f)|^2}{|\mathrm{P}^+(f_c)|^2}\right)\Big|_{f=f_c\pm\mathrm{BW}/2} = -10\ d\mathrm{B} \tag{3.3}$$

Which gives the following relationship between BW and PRF :

$$\mathrm{BW(PRF)} = \frac{\sqrt{-\ln(0.1)}\cdot 6\cdot\mathrm{PRF}}{\pi} \approx 3\mathrm{PRF} \tag{3.4}$$

This function is plotted in Figure 3.1. As a compromise between the available bandwidth and the maximum achievable data rate, the chosen bandwidth is 150 MHz, which corresponds to a ∼20 ns pulse. For a 1 bit per pulse modulation like OOK and BPSK , this corresponds to a maximum theoretically achievable data rate of ∼50 Mb/s. Equations 3.1 and 3.2 are represented in Figure 3.2 for a 20 ns pulse centered at 450 MHz.

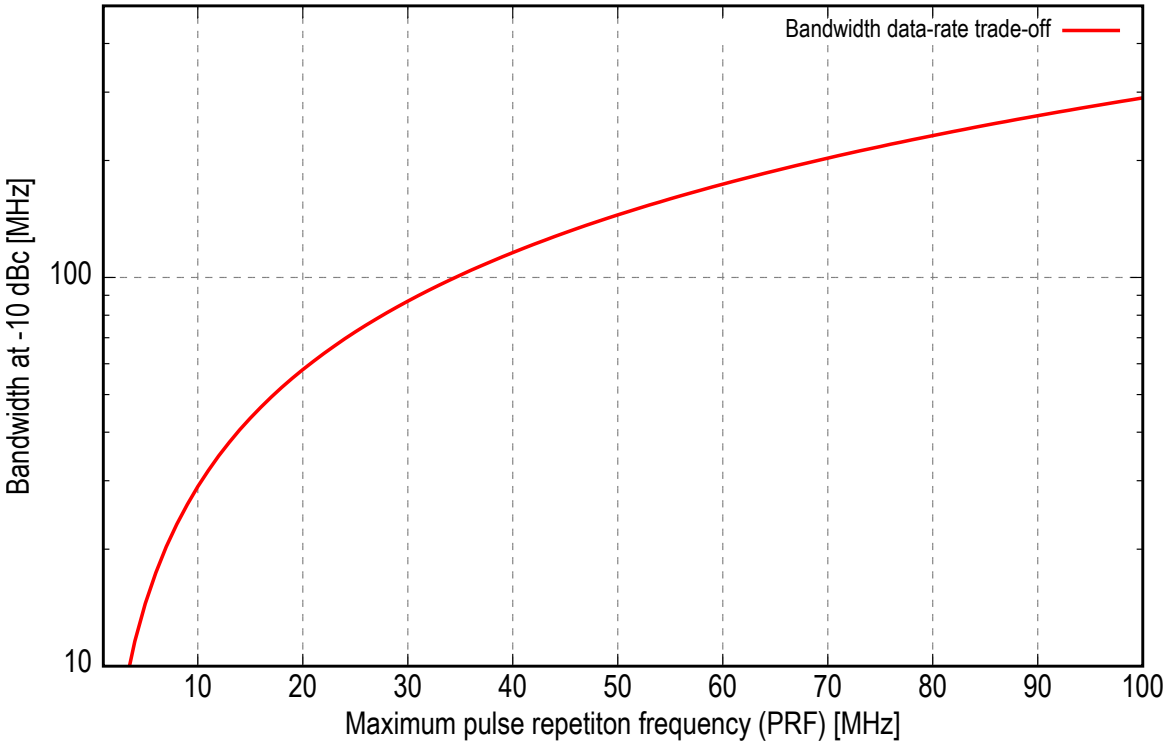

FIGURE 3.1 – Maximum pulse repetition frequency (i.e. maximum data-rate) versus bandwidth trade-off.

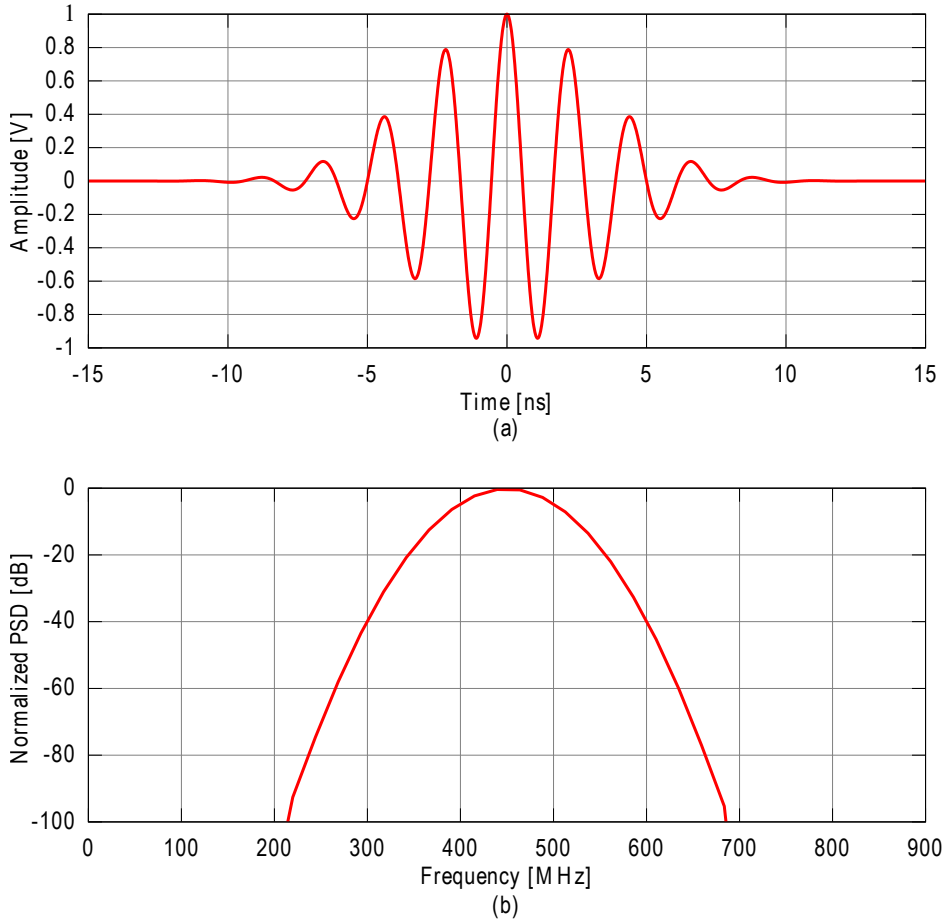

FIGURE 3.2 – (a) Pulse in time domain (b) Pulse in frequency domain.

3.1.2 Pulse Shaping

The chosen frequency is not covered by the IEEE 802.15.6 standard for c-BCC communication, hence there is no specific spectrum mask to fulfill. However, as the fractional bandwidth is more than 20 % we can consider the signal as an UWB signal, which should respect FCC regulation [4]. Although the emitted signal would be mainly confined to the body, the signal will partially radiate because of the *body antenna effect*, where the human body operates as an antenna radiating the signal power into the air [5]. The impact of the body antenna effect has not been measured yet for frequencies higher than 150 MHz, but this effect is expected to increase with frequency. Hence, it is desirable to limit out-of-band emissions, for example, in the GPS band (960−1610 MHz), where the radiated power density should be below −75.3 dBm/MHz [4].

3.2 Link Budget

The derived channel loss model is presented in (3.5), and the measured parameters at 450 MHz are enumerated in Table 3.1 [1, 2]. From the channel characterisation we know that the channel loss is up to 70 dB at 50 cm. This value will be used when computing the complete link budget.

$$\mathrm{L} = \begin{cases} \mathrm{L}_0 & d = d_0 \\ \mathrm{L}_0 + \alpha_0 (d - d_0) & d_0 < d < d_1 \\ \mathrm{L}_1 + \alpha_1 (d - d_1) & d_1 < d \end{cases} \tag{3.5}$$

Frequency [MHz]	L_0	α_0	L_1	α_1	σ [dB]
450	-47	-0.95	-55	-0.37	6.5

TABLE 3.1 – Channel loss model parameters

σ is the standard deviation of the measurement compared to the theoretical fit, explained by the non-homogeneity of the human body. L_0 is the loss for the shortest distance recorded at d_0 =5 cm (i.e. insertion loss). L_1 represents the loss at d_1 = 15 cm, transition distance between the EQS and Surface Wave (SW) regimes.

Considering the network architecture presented in Figure 1.4, the type and amount of data exchanged from Table 1.1, the channel characterization results from [1, 2], and the pulse-based communication centered on 450 MHz, the hub-to-hub communication data rate is set to the maximum possible rate of 50 Mb/s. The leaf-to-hub link is however set to 100 kb/s. The receiver sensitivity S is calculated in (3.6) as a function of the integrated thermal noise N_{th} over the bandwidth of consideration (see (3.8)) .

$$\mathrm{S} = \mathrm{N}_{th} + \mathrm{NF} + \mathrm{SNR}_{req} \tag{3.6}$$

Where NF is the receiver noise figure and SNR_{req} is the required signal-to-noise ratio expressed in (3.7) as a function of the desired data rate DR.

$$SNR_{req} = \frac{E_b}{N_0} + 10 \cdot \log_{10}\left(\frac{DR}{BW}\right) \tag{3.7}$$

$$N_{th} = 10 \cdot \log_{10}(K \cdot T \cdot 10^3) + 10 \cdot \log_{10}(BW) \tag{3.8}$$

For a usual noise figure of NF = 6 dB, a bandwidth of BW = 150 MHz, a ratio E_b/N_0 = 14 dB and a data rate of DR=100 kb/s and DR = 50 Mb/s, the sensitivity becomes respectively :

$$S_{100kb/s} = -104dBm \tag{3.9}$$

$$S_{50Mb/s} = -77dBm \tag{3.10}$$

In terms of geometry, the leaf-hub distance is limited to 15 cm, which means from equation 3.5, that the signal attenuation is not greater than 55 dB. Given a receiver sensitivity of −104 dBm and a 3 dB margin, the minimal output power the leaf transmitter should radiate is about −46 dBm. The inter-hub range is set to 50 cm (about an adult arm length) allowing a large coverage of the human body. Applying the same calculation, the hub transmitter output power should be around −4 dBm for a 50 Mb/s data rate. Again, the link budget could be improved by reducing the insertion loss (L_0) with adapted electrodes, which would relax the required output power of the transmitter and/or the required sensitivity of the receiver.

3.3 Energy efficiency

For a CMOS digital intensive, low-power transmitter, the power consumption is defined as the general formula for the dissipated power losses in a digital circuit [6] :

$$P_{diss} \approx \alpha(C_L + C_{SC}).V_{DD}^2.f + (I_{DC} + I_{Leak}).V_{DD} \tag{3.11}$$

Where α is the activity factor, also called duty-cycle factor, C_L is the load capacitance, C_{SC} is the short-circuit capacitance modelling the short-circuit dissipated power, V_{DD} is the supply voltage, f is the operating frequency, I_{DC} is the static current and I_{Leak} is the leakage current. Thus, $\alpha(C_L+C_{SC}).V_{DD}^2.f$ corresponds to the dynamic dissipated power ($P_{diss,dyn}$), while $(I_{DC}+I_{Leak}).V_{DD}$ corresponds to the static power dissipated ($P_{diss,stat}$). Then, for a duty-cycled transmitter, when $\alpha \rightarrow 1$, the power consumption is dominated by the dynamic dissipated power. Whereas, when $\alpha \ll 1$ the static dissipated power dominates. Therefore, for an aggressively duty cycle transmitter,

the leakage plays a major role in the energy and system efficiency of the transmitter.

The average power consumption to transmit one pulse is illustrated in Figure 3.3 and is expressed as :

$$\bar{\mathrm{P}} = \frac{1}{\mathrm{T}_b}\int_0^{\mathrm{T}b} p(t)dt = \frac{1}{\mathrm{T}_b}[\mathrm{T}_p \cdot \mathrm{P}_{diss,pulse} + (\mathrm{T}_b - \mathrm{T}_p) \cdot \mathrm{P}_{diss,stat}] \tag{3.12}$$

$\mathrm{P}_{diss,pulse}$ represents the total dissipated power to transmit one pulse for $\alpha = 1$:

$$\mathrm{P}_{diss,pulse} = \mathrm{P}_{diss,stat} + \mathrm{P}_{diss,dyn} + \mathrm{P}_{out,peak} \tag{3.13}$$

We then express two factors, the activity factor α and the leakage ratio β :

$$\alpha = \mathrm{T}_p/\mathrm{T}_b \tag{3.14}$$

$$\beta = \mathrm{P}_{diss,stat}/\mathrm{P}_{diss,pulse} \tag{3.15}$$

We also express the peak system efficiency (SE_{peak}) of the transmitter for $\alpha = 1$:

$$\mathrm{SE}_{peak} = \mathrm{P}_{out,peak}/\mathrm{P}_{diss,pulse} \tag{3.16}$$

Finally, we express the energy-efficiency, i.e. the required energy to transmit one bit of data, as

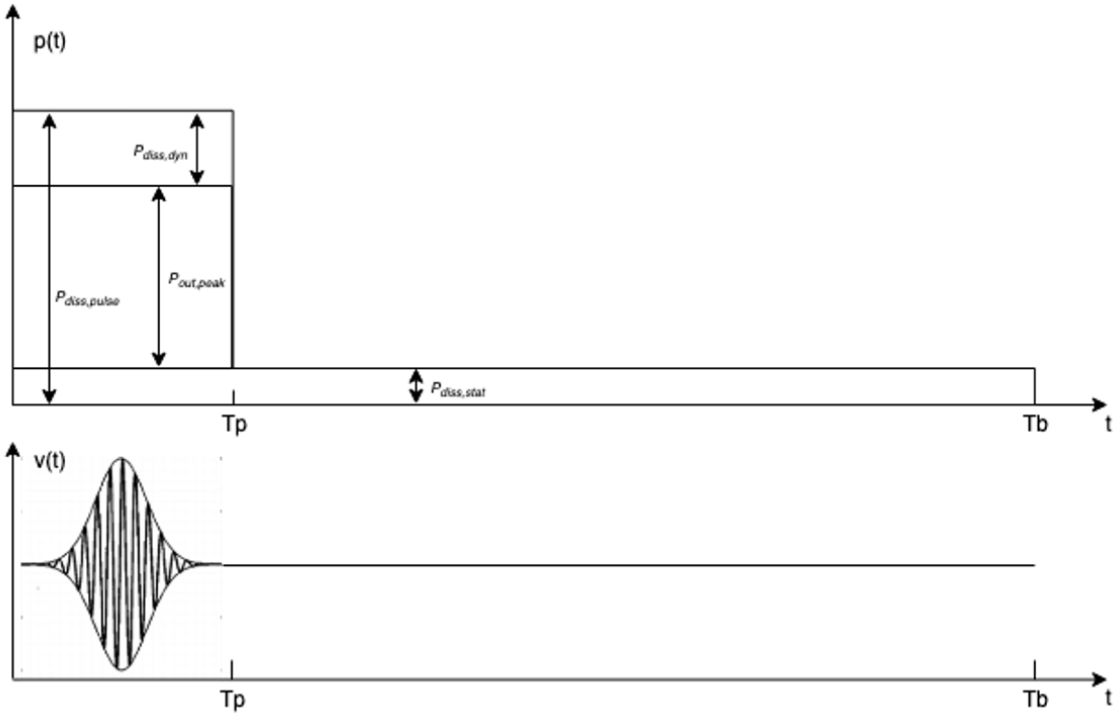

FIGURE 3.3 – Illustration of a transmitted pulse and its power consumption over time

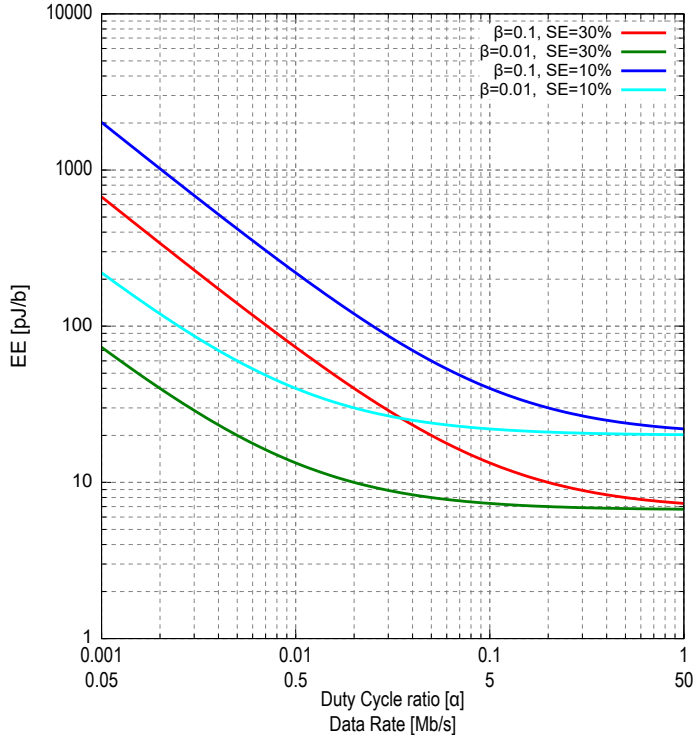

FIGURE 3.4 – Energy Efficiency as a function of the duty cycle ratio α (and equivalent Data Rate for T_p = 20 ns) for different values of leakage ratio (β) and system efficiency (SE) ($P_{out,peak} = -10\ dBm$).

a function of the duty cycle ratio, the leakage ratio, and the system efficiency of the transmitter.

$$EE \cong T_p \cdot \frac{P_{out,peak}}{SE_{peak}} \cdot (1 + \beta/\alpha) \tag{3.17}$$

The energy-efficiency is plotted in Figure 3.4 for 30 % peak system efficiency with 10 % and 1 % leakage ratio and for 10 % peak system efficiency with 10 % and 1 % leakage ratio (for T_p=20 ns and P_{out}= −10 dBm). We can observe that at high data rates, the system efficiency of the transmitter is the parameter to optimize for an energy-efficient transmitter. This means that dynamic power losses should be reduced. In another hand, when transmitting at low data-rates, the leakage current is the main parameter to be optimized. Hence, for design considerations of an energy-efficient pulse-based transmitter, it is required to design power amplifier with high system efficiency (i.e., reduced dynamic losses) for high data rate communications and ultra-low leakage current for low data rate communications.

3.4 Safety Regulations

Besides spectrum regulation, Electric and Magnetic Fields (EMF) exposure of the human body is limited by international regulations. Here, we will consider international guidelines from the International Commission on Non-Ionizing Radiation Protection (ICNIRP), but local regulations can

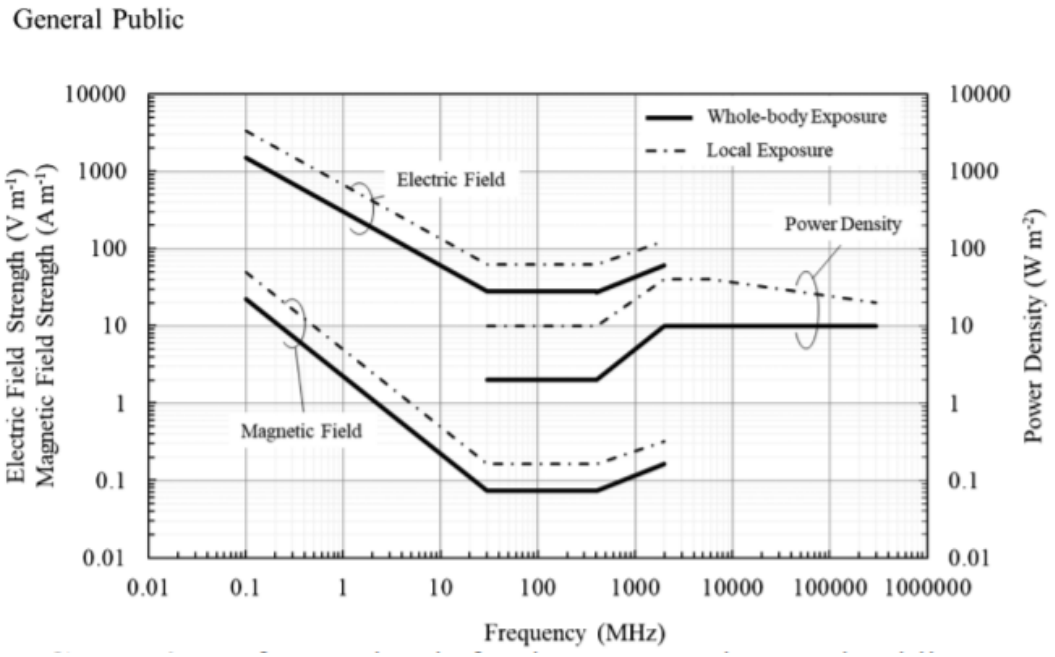

FIGURE 3.5 – Reference levels for time averaged general public exposures of ≥ 6 min, to electromagnetic fields from 100 kHz to 300 GHz (unperturbed rms values)

apply (e.g., FCC for the United States). According to [7], the whole-body exposure for the general public is limited to 2 W/m² at 400 MHz and local exposure is limited to 10 W/m², for time average exposure ≥ 6 minutes (Fig. 3.5). Furthermore, the whole-body average Specific energy Absorption Rate (SAR) restriction for the general public is 0.08 W/kg, averaged over 30 min [7]. Hence, considering a transmitter with an output power below 0 dBm (1 mW), the radiated power is much below the exposure limit.

3.5 Conclusion

This chapter describes the system specifications for the transmitter and receiver for a surface wave c-BCC channel at 450 MHz. First, the trade-off between bandwidth and maximum data-rate has been defined for a pulse-based communication. This trade-off allowed to derive the transmitter as emitting 20 ns pulses for a 150 MHz bandwidth allowing to reach a theoretical maximum data rate of 50 Mb/s. Then, considering the channel model proposed by [1, 2] we defined the link budget of the communication, allowing to define the required sensitivity of the receiver and the output power of the transmitter. Some design considerations have been presented highlighting the importance of leakage current reduction for low data rate communications and system efficiency enhancement for high data-rate communications. Finally, regulations at the spectrum and health levels have been considered to propose a safe and regulatory compliant solution.

3.6 References

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Chapter 4

Proposed transmitter : A fully-digital, pulse-based transmitter with flexible data-rate and ultra-low power consumption

Contents

4.1 28 nm FD-SOI Technology

Advanced CMOS technology allows for compact integration of analog, digital and mixed circuits on a single SoC with low-voltage supply and hence low-power consumption. In bulk technology, the body-bias voltage is directly applied on the parasitic diodes formed between diffusion and substrate. FBB in bulk technology is limited to +300 mV, due to the diffusion to substrate junction leakage. The FD-SOI technology offers some advantages compared to the conventional bulk CMOS technology. A buried oxide layer, called the BOX, isolates the transistor from the substrate. This BOX allows for leakage reduction and extends the range of the possible substrate voltage called body-biasing, or back gate biasing. Regular Voltage Threshold (RVT) devices use a conventional well configuration (Fig. 4.1.b). Low Voltage Threshold (LVT) architecture (Fig. 4.1.a) uses a reversed configuration with respect to bulk technology. This technology is known as flip-well technology. In this configuration, NMOS transistors are fabricated on an N-Well and PMOS transistors are fabricated on P-Well. This approach is possible only in FD-SOI technology, as it provides complete dielectric isolation to the device. The body is connected with dedicated supplies, such as VBBN for NMOS and VBBP for PMOS. In the 28 nm FD-SOI technology, the body factor is ~85 mV/V for the thin oxide devices and the body voltage variation can range up to +/- 3 V [1] (Fig. 4.1.c). The wide range of body-biasing for both LVT and RVT devices allows for threshold voltage control which eases the trade-off between high performances and low leakage current, as well as allowing low voltage operation. Hence, the 28 nm FD-SOI technology is particularly suitable for low-power applications.

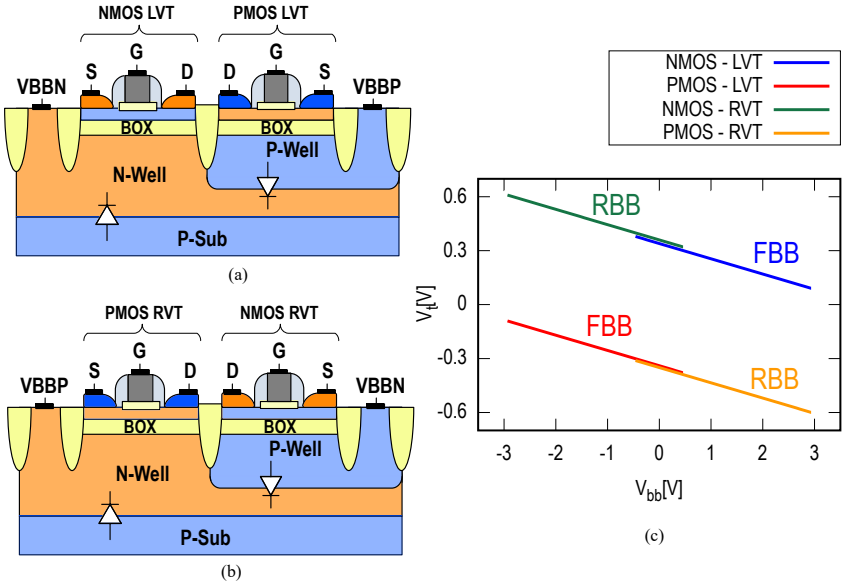


FIGURE 4.1 – (Cross section of 28 nm FD-SOI CMOS transistors : (a) LVT transistors and (b) RVT transistors. (c) Threshold voltage (V_t) versus the body-bias voltage for RVT and LVT.

4.2 Transmitter Architecture

The proposed transmitter is based on a digital intensive architecture. A digital transmitter benefits from technology scaling and allows for smaller area, lower power consumption and higher configurability, compared to an analog architecture. Digital power amplifiers reach high power added efficiency as CMOS inverters are very efficient amplifiers that require no bias current or large inductances [2]. In terms of frequency generation, CMOS inverter-based ring-oscillators have shown ultra-low power capabilities compared to typical LC oscillators. As stated in Chapter 3, the power consumption of a digital pulse-based transmitter is dominated by dynamic power consumption when operating at high pulse repetition rate where the power dissipation is proportional to fCV_{DD}^2. Hence, ultra-low voltage operation is desirable as dividing by 2 the supply voltage divides by 4 the dynamic power dissipation. For lower data rate operations, ultra-low voltage supply also allows for low static power dissipation as it is equal to $I_{leak}V_{DD}$ with body-biasing allowing to control the leakage current. As the 28 nm FD-SOI technology offers low-voltage threshold transistors, which can further be controlled through body-biasing, we target a supply voltage operation at 0.5 V. To further reduce the dynamic power consumption, it is also desirable to massively operate the transmitter at low frequency such as in [3, 4]. Hence, the proposed architecture is based on a low-frequency ring oscillator with edge-combiners embedded in a digital power amplifier performing the frequency multiplication at the very end of the transmitter. Moreover, a digital architecture is used, it also allows digital pulse shaping permitting to easily configure the pulse shape, and enhance out-of-band emissions.

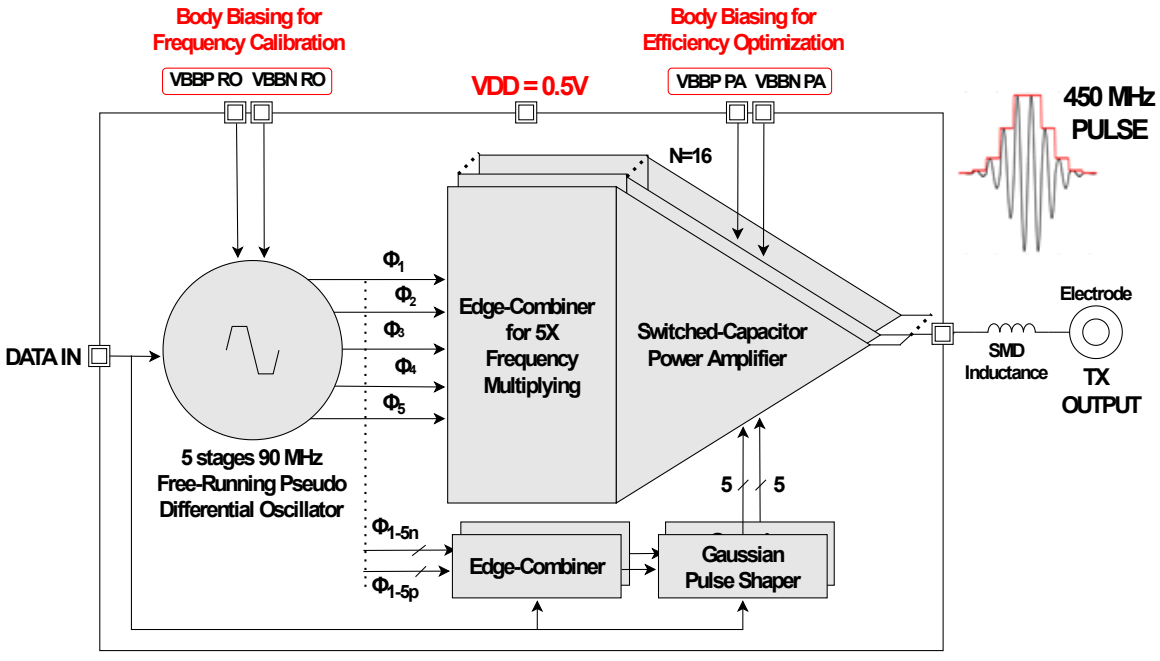


FIGURE 4.2 – Proposed architecture of the c-BCC SW TX

The proposed TX circuit (Fig. 4.2) is composed of a free-running Pseudo-Differential Ring Oscillator (PD-RO) at 90 MHz feeding a Switched-Capacitor Power Amplifier (SCPA) with embedded Edge-Combiner (EC), in order to reach the 450 MHz central frequency. The overall TX is data-enabled (OOK modulation), which means it only runs during the pulse duration, saving power at low data-rates. Short pulses combined with non-coherent OOK modulation accept the use of an unlocked frequency reference and enable instant startup and aggressive duty-cycling. A low-frequency oscillator with frequency multiplication in the power amplifier allows for reduced dynamic power consumption as the circuit is massively low-frequency operated. Digital pulse-shaping is also introduced for spectral efficiency limiting out-of-band emissions. To enable BPSK modulation, a multiplexer array is introduced between the PD-RO and the Edge-Combiner Switched-Capacitor Power Amplifier (EC-SCPA). Hence, to transmit a BPSK modulated signal, the oscillator receives a pulse-width modulated "clock", and the input data is from the phase selection of the multiplexer array, selecting one of the two differential outputs of the PD-RO to create a phase-modulated signal. Regarding electrode impedance matching, Benarrouch [5] have simulated and measured the electrode impedance when attached on-body in the frequency band of 400−500 MHz (Fig. 4.3). As observable in Figure 4.3, the real part of the electrode impedance in 400−500 MHz band is roughly equal to 20 Ω and the imaginary part equals to −50 Ω. However, the transmitter has been designed for a 50 Ω load for measurement purposes. In a complete solution, specific electrodes matched to the desired impedance should be designed.

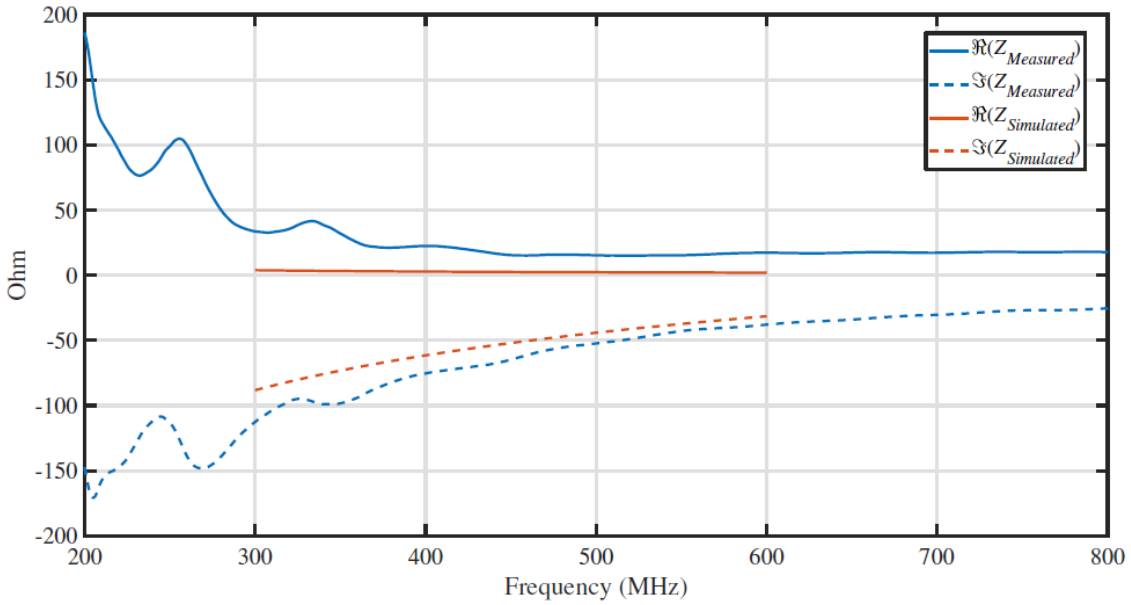


FIGURE 4.3 – Electrode impedance simulated vs. measured with a VNA (Taken from Benarrouch [5])

The body-biasing feature of the 28 nm FD-SOI technology is used in mainly three aspects in the proposed circuit. First, it enables low threshold voltage allowing ultra-low voltage operation down to 0.5 V for ultra-low power consumption. Secondly, it allows for frequency calibration and PVT compensation on the oscillator, by tuning the threshold voltage of the inverters in the ring oscillator. Thirdly, it enables power amplifier efficiency optimization by reducing the ON-resistance of the transistors while limiting parasitic capacitances.

4.3 Transmitter Design

4.3.1 Pseudo-Differential Ring Oscillator

Ring-oscillators have recently become a low-power alternative to a typical LC oscillator. ROs offer 1) smaller area by avoiding the use of integrated inductance, 2) the ability to easily take out several phases, 3) lower power consumption, at the cost of degraded phase noise, compared to LC oscillators. A single-ended ring-oscillator is composed of an odd number of inverters where the last inverter is looped back to the first, producing a stable oscillation. The frequency of oscillation is determined by :

$$f = \frac{1}{2\mathrm{N}t_d} \tag{4.1}$$

Where N is the number of inverters in the loop and t_d is the propagation delay of a single inverter. To produce a differential signal, an alternative architecture uses differential inverting amplifiers. Such architecture usually consumes more power than single-ended ROs. Another solution to produce a differential output from the oscillator is to use a pseudo-differential architecture. A pseudo-differential architecture is composed of two single-ended ring oscillator loops mounted in a pseudo-differential topology with inverter-based latch locking between each stage. The pseudo-differential architecture consumes less power compared to a differential architecture.

A design methodology of pseudo-differential ring oscillators was presented in [6]. The take-away idea is that doubling the size of the inverters in the loops, for a constant oscillating frequency, doubles the power consumption and improves by 3 dB the phase noise (Table 4.1). Given the low-frequency oscillator with relaxed phase noise requirements, and thanks to the simple modulations used, the oscillator can reach ultra-low power.

According to jitter theory, in free-running ring oscillator, for a short runtime, white noise is the dominant noise source in free-running oscillators, and jitter increases as the square root of the run-time [7]. The accumulated rms jitter as a function of run-time T_p is given by :

$$\Delta t_j(\mathrm{T}_p) = \frac{\sqrt{2\mathscr{L}(f_0)}f_0}{f_c}\sqrt{\mathrm{T}_p} \tag{4.2}$$

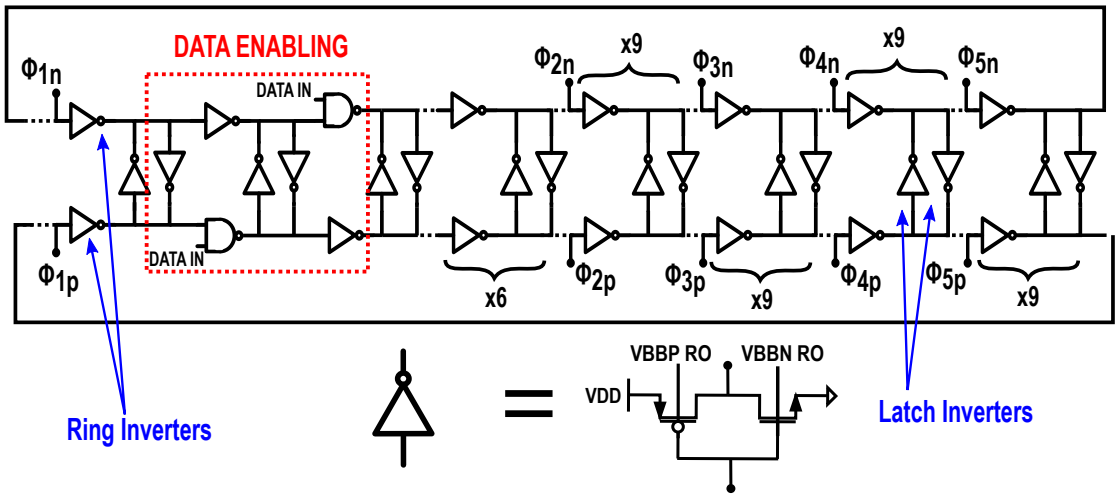


FIGURE 4.4 – 90 MHz Pseudo-differential Ring-Oscillator (PD-RO) schematic.

Where $\mathscr{L}(f_0)$ is the phase noise at f_0, f_0 being the frequency offset from f_c the central frequency. For a free-running oscillator the frequency offset should be taken where white noise is the dominant source of noise, i.e. where the slope of the phase noise is equal to -20 dB/decade. For an OOK modulation, phase noise is not a constraint as it does not use the phase information to demodulate the data. According to the analysis in [8], for a BPSK modulation scheme, we can set the maximum phase noise allowable to $\pi/4$, which corresponds to a maximum total accumulated time jitter of $\Delta t_j = 278\ ps$ after $T_p = 22.22\ ns$ pulse duration at $f_c = 450\text{MH}z$. Which means that the phase noise should not be higher than $-78\ d\text{Bc/H}z$ to be able to demodulate BPSK modulation. Such a relaxed phase noise requirement allows for the use of an unlocked ultra-low power oscillator.

The PD-RO circuit is represented in Figure 4.4. The 90 MHz frequency is chosen as two periods correspond to 22.22 ns which is the specified pulse width. An oscillator at 450 MHz will consume 5X more power at equivalent phase noise because of the dynamic power dissipation proportional to $f\text{CV}^2$. The oscillator is based on a 45 stages pseudo-differential architecture. 5 phases are taken

W_P Ring Inverter W_N Ring Inverter [µm]	W_P Latch W_N Latch [µm]	Power Consumption [µW]	Phase Noise @ 1 MHz [dBc/Hz]
1.5 0.5	0.75 0.25	11	-105
3 1	750 0.25	22	-108
6 2	1.5 0.5	44	-111

TABLE 4.1 – Simulation of 3 designs of pseudo differential ring oscillator for f=110 MHz (considering 20% post-layout loss), Vdd=0.5 V and L=46 nm, with 28 nm FD-SOI technology

every 9 stages from both the negative and positive loops to perform frequency multiplication. The positive feedback enables fast current transitions with sharp edges as required for the edge combination. A NAND gate inside each loop duty-cycles the oscillator according to the input data and allows instant start-up. As the PD-RO is turned-off between each pulse by the introduced NAND gates, there is no long-term drift of the oscillator.

4.3.2 Edge-Combiner Switched Capacitor Power Amplifier

Following the oscillator, the signal needs to be frequency-multiplied and amplified. For the amplification, a SCPA architecture is used [9]. The SCPA is a Class-D PA that has been very popular recently as it allows to design high performance transmitters with high-order complex modulation, watt-level output power, beamforming, among others [10]. As well, it has also been demonstrated to be very well suited for ultra-low power communications [3, 11, 12], and allows for high integrability, digital configuration, and high efficiency.

The efficiency of a switching mode power amplifier strongly depends upon the ON-resistance (r_{on}) of the switches in the output inverters. The usual technique to reduce r_{on} is to increase the width of the transistors. However, this leads to an increase of the parasitic capacitance, increasing the dynamic power consumption and hence degrading the efficiency of the power amplifier. The forward body-biasing knob, specific to FD-SOI technology, is used to lower the threshold voltage of the transistors, reducing r_{on} at the low 0.5 V supply voltage, limiting their size and parasitic capacitance which improves the efficiency of the power amplifier as well as saving area. The principles and design methodology are described in detail in Chapter 5. By using the simulation-validated

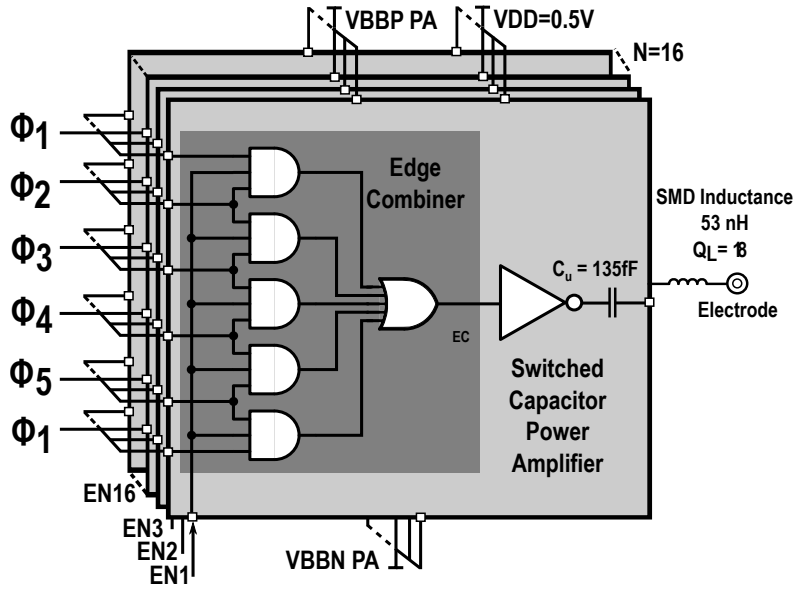


FIGURE 4.5 – Schematic of the EC-SCPA

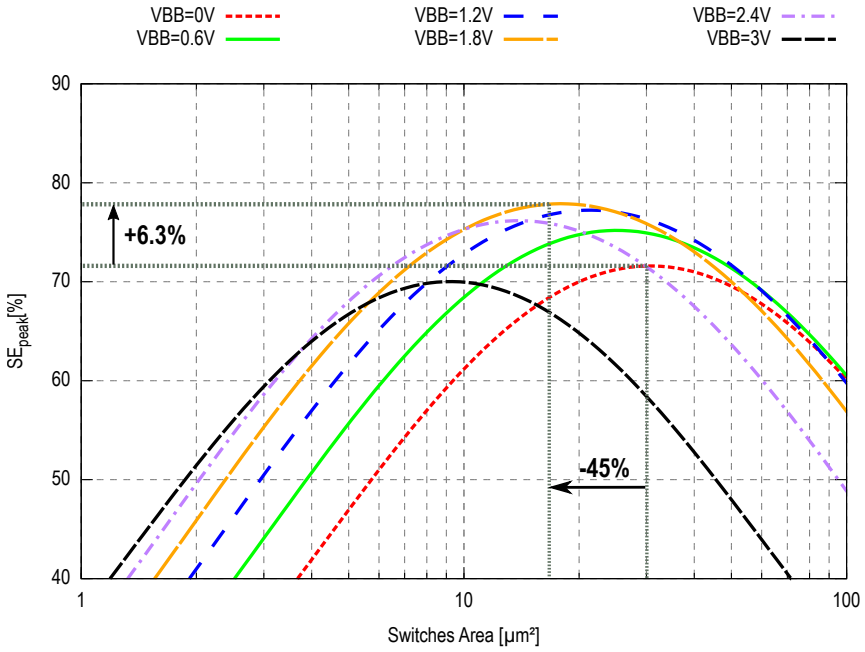


FIGURE 4.6 – Model of the peak system efficiency (SE) of a SCPA at 450 MHz for different body-biasing values (Switches Area for an optimal load of 50Ω).

model proposed in the next chapter, it is shown in Figure 4.6 that a forward body-biased SCPA improves by 6 % the peak system efficiency (SE_{peak}) of the power amplifier while reducing by 45 % the switches area at 450 MHz. The output inverters are sized for an optimal body-biasing of ~1.8 V according to the results in Figure 4.6. For further area saving the unit capacitances C_u in each slice are MOM capacitances stacked on top of the inverters. An external inductance is used in a 0402 package to form a wideband LC bandpass filter centered at 450 MHz. From SCPA theory [9], for an ideal peak output power of 0 dBm and a supply voltage of 0.5 V, the optimal load is equal to 50 Ω which avoids the use of lossy matching network.

As presented in Figure 4.8 the EC are performing frequency multiplication by 5 to reach the 450 MHz central emission frequency. In each SCPA slice, an edge combiner multiplies the PD-RO frequency by using the 5 phases of the 90 MHz oscillator. In practice, the conceptual AND and OR

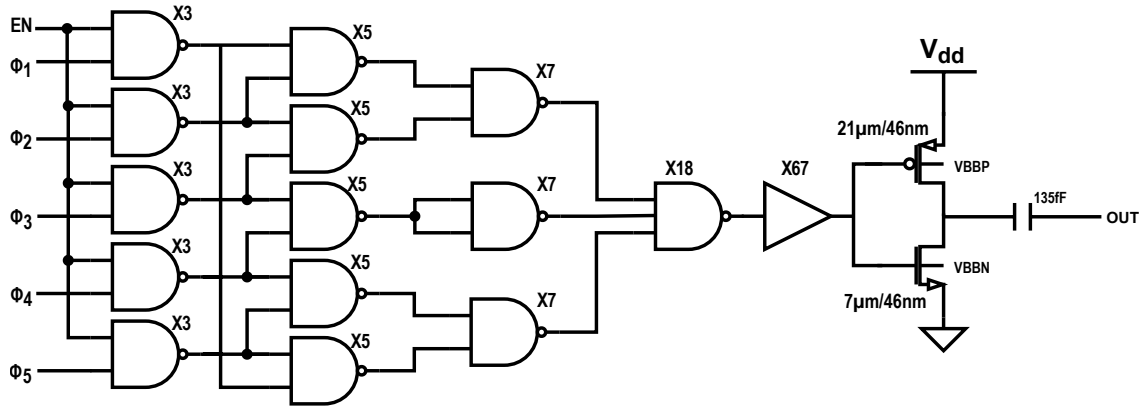


FIGURE 4.7 – Detailed schematic of a EC-SCPA slice

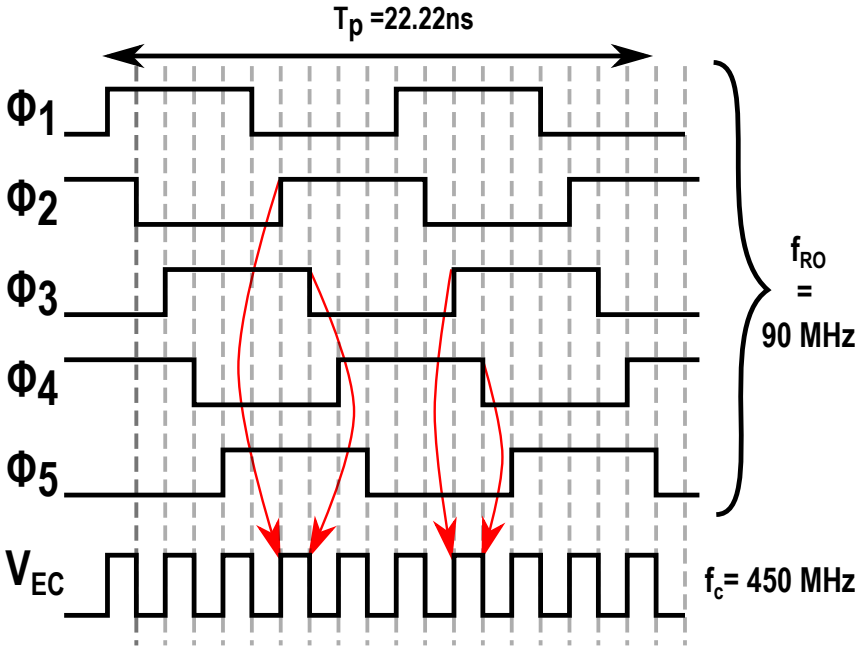


FIGURE 4.8 – Timing diagram of the EC

gates shown in Figure 4.5 are implemented in NAND logic (Fig. 4.7) for fast switching, limiting the introduced jitter by the edge-combiners. Also, as observable in Figure 4.7, a buffer is inserted after the edge-combiner to drive the output inverter with a tapering factor of ~3.5. All NAND gates and buffers are implemented with standard cells with a poly-biasing (i.e. gate length extension) of 16 nm for manufacturing robustness and to limit the leakage impact. As observable in Figure 4.9,

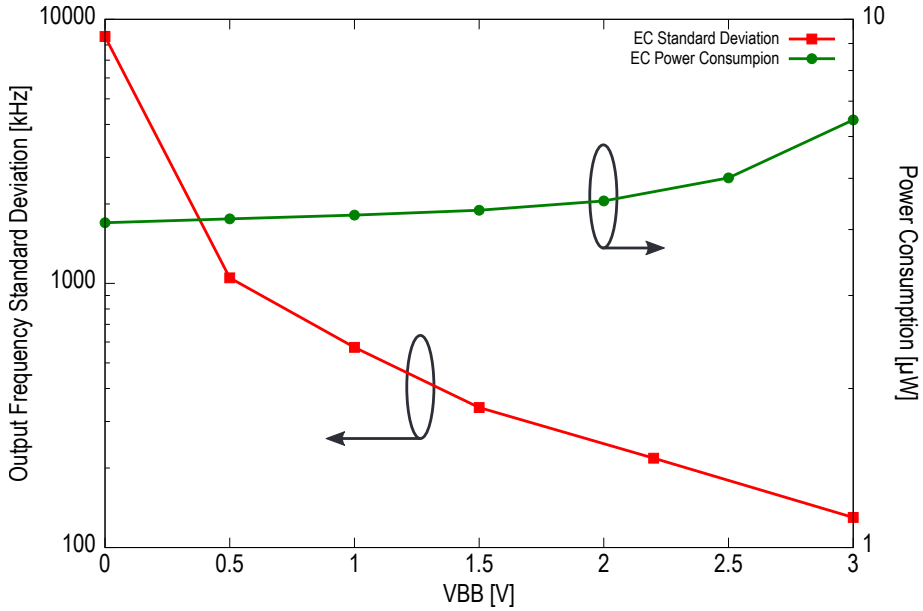


FIGURE 4.9 – Standard Deviation (obtained with process and mismatch Monte-Carlo simulations of the Edge-Combiner for 1000 iterations, with the oscillator at the input considered body-bias calibrated) (red) and power consumption (green) of an EC as a function of the body-bias voltage VBB

the edge-combiners provide robust frequency-multiplication thanks to body-biasing. As observable in Figure 4.9, applying a ~1.8 V body-biasing on the edge-combiners allows to reduce by 40X the standard deviation of process and mismatch variations compared to a nominally body-biased edge-combiner with little overhead of their power consumption. This effect is explained by the threshold voltage reduction offered by FBB , making the switching of the NAND gates sharper and hence reducing timing errors. As ~1.8 V approaches the optimal body-biasing to apply on the SCPA (Fig. 4.6), the ECs are body-biased with the same voltage as the SCPA.

Having the edge combiner distributed in each of the 16 slices allows to have the 450 MHz frequency only at the very final inverter of each slice, allowing a massively low-frequency operated circuit. It also relaxes the constraints on buffers and 'clock' tree distribution, with the multiplication performed only in the activated slices.

4.3.3 Pulse Shaper

The pulse shape has an important impact on the frequency response of the transmitter. With a rectangular pulse shaping (i.e. no pulse shaping) important sidelobe emissions are observable which cause out-of-band interferences and degrade spectral efficiency. Gaussian pulse shaping has already been demonstrated to be very efficient to limit out-of-band spectral emissions [8, 13].

It is shown that an ideal Gaussian pulse shaping at $2f_c$ sampling frequency removes the sidelobes emissions at $2f_c$, limiting out-of-band emissions. Hence, a near-Gaussian pulse shaping, as shown in Figure 4.11, with a sampling frequency of $2f_c$ is implemented. In Figure 4.10 the schematic of the implemented pulse-shaper is presented. A dual 5-bit Johnson ring counter driven by complementary clocks provides the enable (ENx) signals. As observable in Figure 4.11 the ring counters allows for successive activation of a given number of slices forming the near-Gaussian

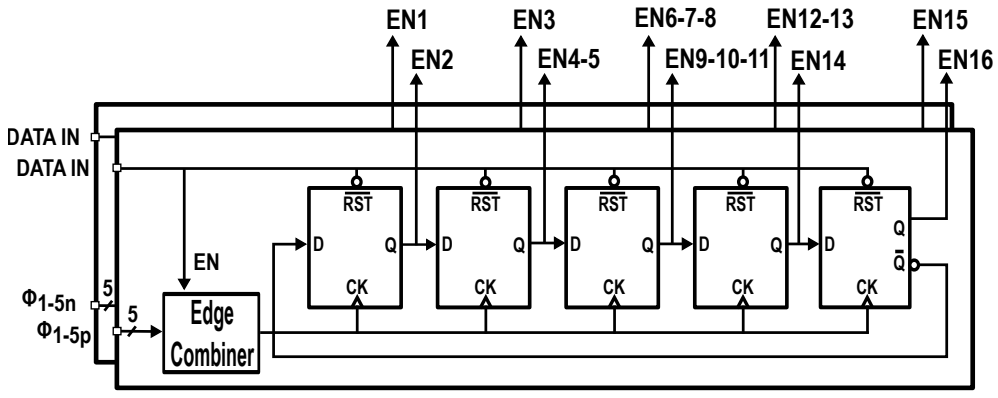


FIGURE 4.10 – Schematic of the digital pulse shaper

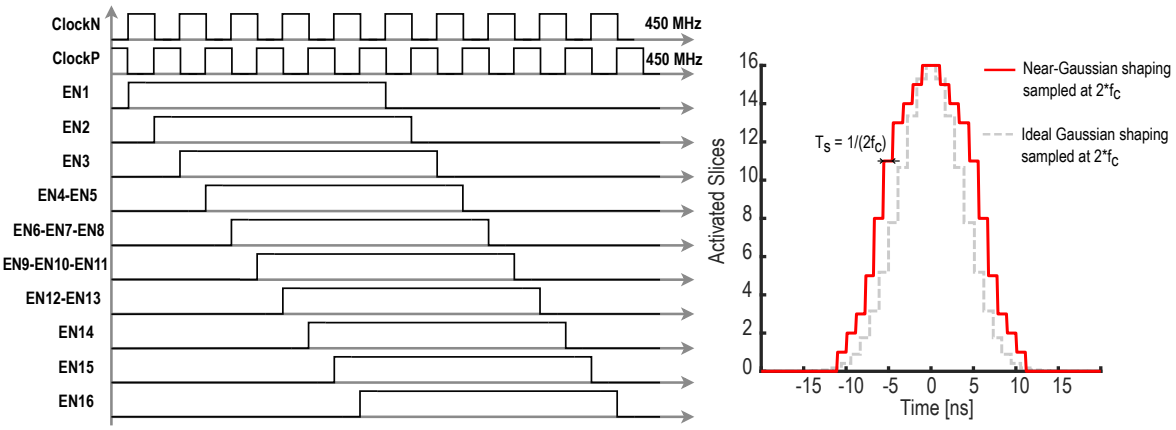


FIGURE 4.11 – Timing diagram of the pulse shaper and Gaussian pulse envelop generated by the pulse shaper

shape.

To reach a thinner control of the amplitude resolution, the number of slices in the EC-SCPA could be increased at the cost of an increased complexity. The number of 16 slices has been chosen as a trade-off between complexity and near-Gaussian approximation.

The complementary 450 MHz clocks are generated by two identical edge combiners from respectively the positive and negative phases of the 90 MHz PD-RO (ϕ_{1-5n}, ϕ_{1-5p}). The $2f_c$ frequency is then easily generated without power consumption overhead by using the complementary clocks, thanks to the pseudo-differential architecture of the oscillator. Similarly as the edge-combiners the flip-flops are implemented with standard cells with a poly-biasing of 16 nm for

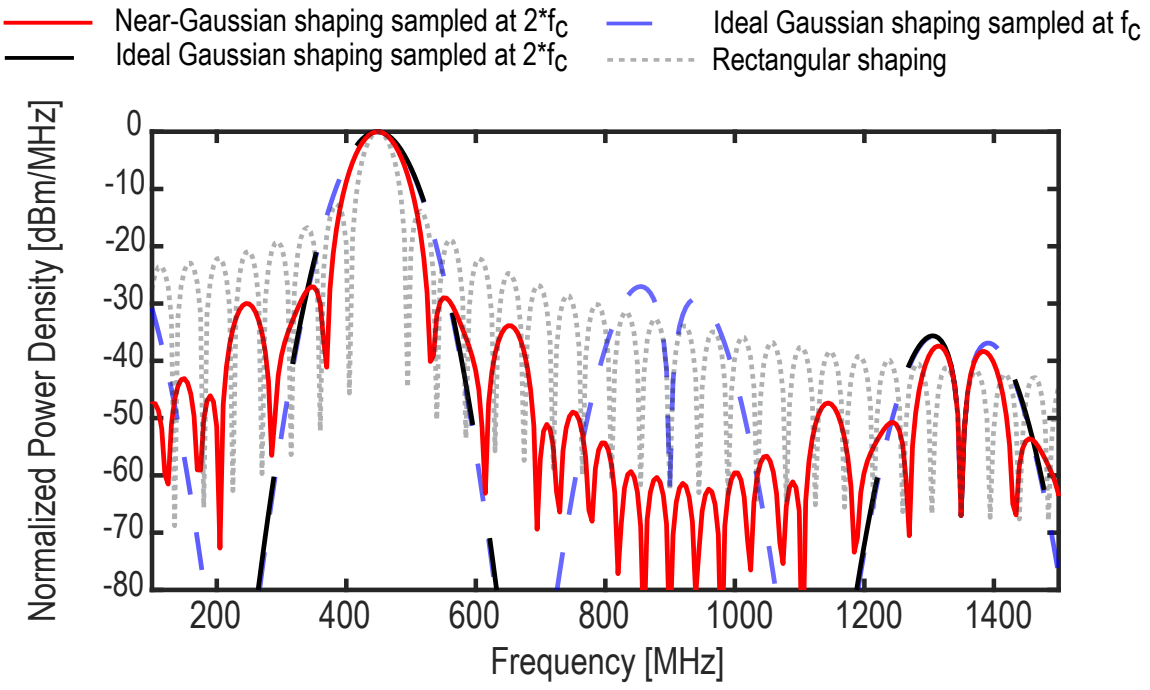


FIGURE 4.12 – Impact of pulse shaping waveform on the frequency response

manufacturing robustness and to limit the leakage impact.

Figure 4.12 compares ideal Gaussian pulse shaping with sampling frequencies equal to f_c and $2f_c$. The frequency response of the near-Gaussian pulse shaping implemented is observable in Figure 4.12, and shows that it limits out-of-band emissions at $2f_c$ frequency and improves spectral efficiency.

4.4 Measurement Results

The designed transmitter has been implemented on a 1x1 mm² die. The active area of the TX occupies 0.0418 mm². Beside the TX, a replica of the PD-RO and of the SCPA (without edge-combining) are placed on the die for test purposes (Fig. 4.13). The chip is packaged in a WFLGA-48 packaging and a Printed Circuit Board (PCB) is designed for measurements. For voltage supply, low-dropout voltage regulators (LP38511 from Texas Instruments) are placed on PCB to convert the 3 V battery voltage to the 0.5 V targeted supply while limiting power supply noise. The body-bias voltages are generated from external power supplies. In a fully practical implementation, a body-bias generator should be integrated on-chip to generate the body-biasing voltages on chip [14].

4.4.1 Pseudo Differential Ring Oscillator

The measurements of the PD-RO are realized by using the isolated oscillator placed on-chip for test purpose. The low-frequency PD-RO consumes 11 µW when running at 90 MHz. As presented in Figure 4.14a, the oscillator frequency fine-tuning is obtained via body-biasing through a one-time calibration (around VBB_{RO} = 0.5 V), and allows to compensate PVT variations between different devices. The measured phase noise of the oscillator in the −20 dB/decade slope the equivalent accumulated jitter can be calculated. In Figure 4.14b the measured phase noise of the PD-RO is presented. In the −20 dB/decade region we measure a phase of −90 dBc/Hz at 1 MHz offset. From the phase noise measurement the accumulated jitter is calculated with equation 4.3.1. This

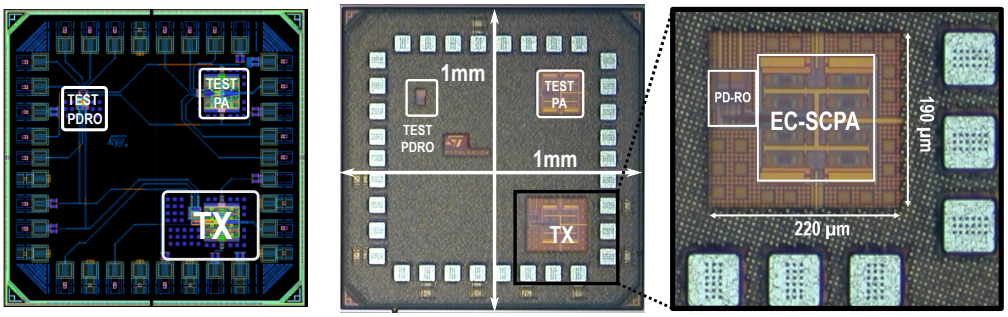
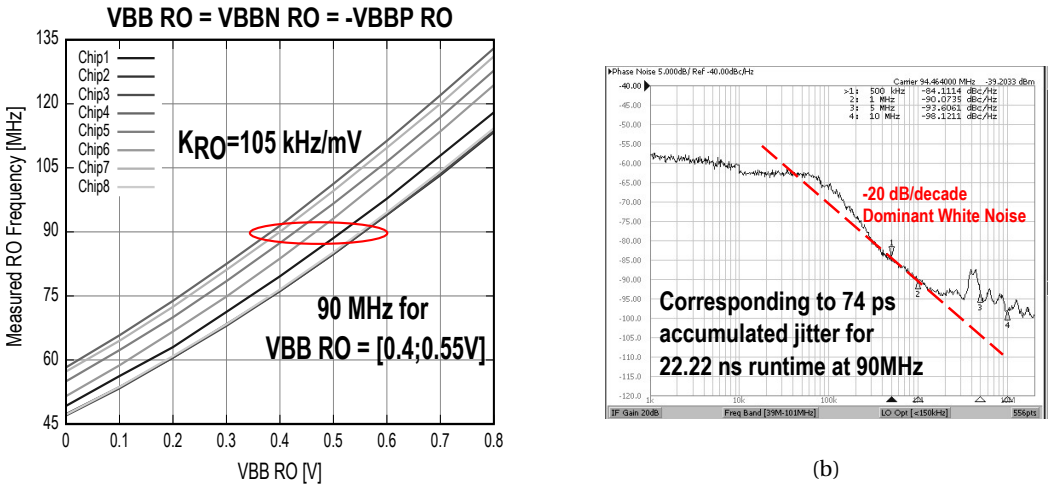


FIGURE 4.13 – Layout picture and die photograph



(a) (b)

FIGURE 4.14 – (a) Measured PD-RO Frequency vs body-bias voltage for 8 devices (b) PD-RO phase noise measurement (the plateau from 1 kHz to 100 kHz is due to the internal PLL of the measurement equipment locking)

corresponds to an accumulated jitter of 74 ps when running for a 22.22 ns duration.

4.4.2 Achievable Data Rate, System Efficiency and Power Consumption

The proposed transmitter reaches a maximum achievable data rate of 27 Mb/s. The output power and system efficiency of the TX is measured on several devices at the maximum data-rate (for Hub-to-Hub communication) and at a low data-rate of 100 kb/s (for Leaves to Hub communication). In Figure 4.15 the output power and system efficiency (at low and high data-rates) is plotted versus the applied body-biasing voltages on the power amplifier. It shows that for a measured −19.7 dBm output power at the maximum data rate of 27 Mb/s, the EC-SCPA reaches an optimal operating point at VBB_{PA} = 2.2 V where the system efficiency is maximum reaching 14 %. An optimal body-biasing point exists as FBB allows to decrease the ON-resistance, while on the other hand, it increases the current leakage. Hence, the optimal bias corresponds to the point where the leakage power consumption becomes predominant. The body-biasing voltage can be adapted to reach the best system efficiency for a given data-rate, or to compensate PVT variations, through one-time calibration. The TX consumes 76 µW at 27 Mb/s, which corresponds to an energy-efficiency of 2.8 pJ/b, for an overall 14 % system efficiency at −19.7 dBm average output power. For the lowest data-rate (100 kb/s), the TX consumes 17 µW with 2.44 % system efficiency, translating into an energy-efficiency of 170 pJ/b for a −33.8 dBm average output power. The power breakdown of the transmitter is plotted versus the data-rate in Figure 4.16. The PD-RO is the dominating power consumer for a data-rate up to 2 Mb/s because of its static power dissipation. At higher data-rate the EC-SCPA becomes the largest power-consuming part of the TX.

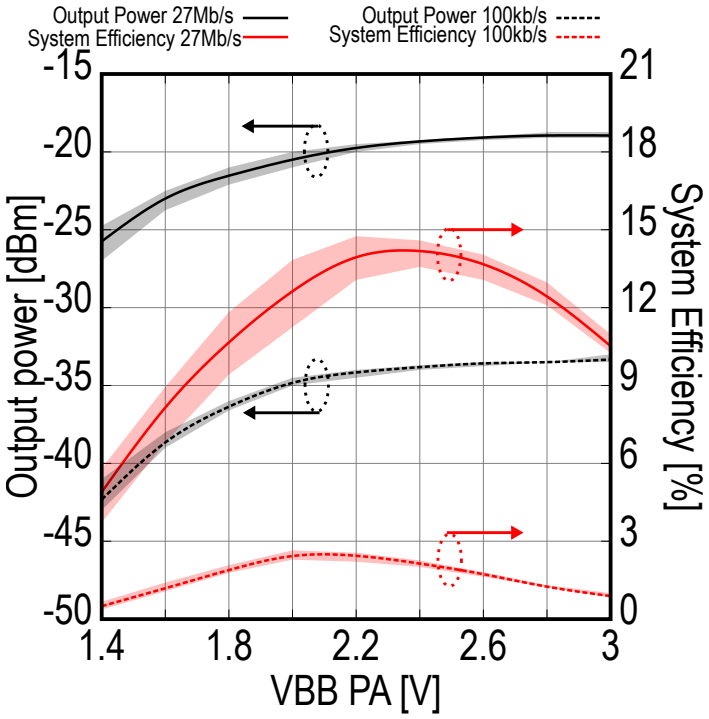


FIGURE 4.15 – Average output power and System Efficiency versus body-biasing voltage for different data-rate (Lines represent the average measured values and the shaded curves represent the boundaries of minimum of maximum measured values on several devices)

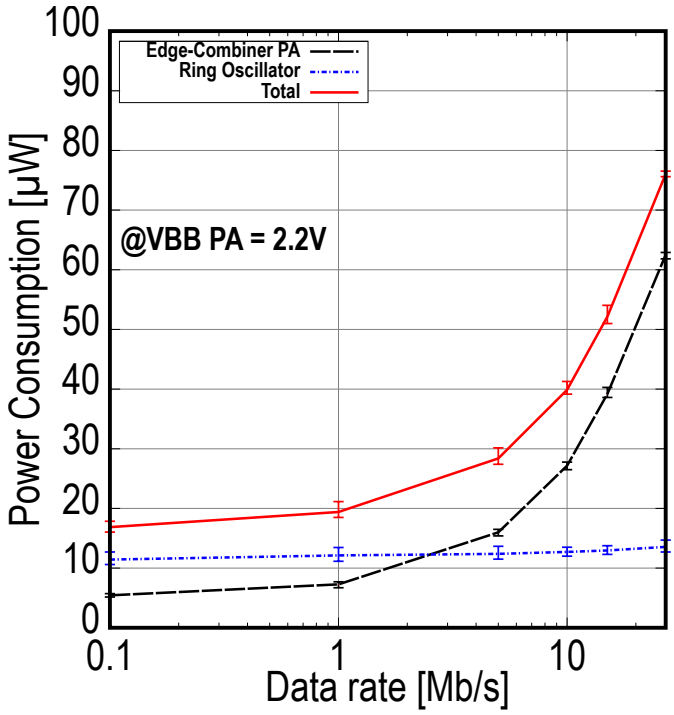


FIGURE 4.16 – Power Breakdown of the TX at VBBPA = +/-2.2 V versus data-rate (error bars represent the boundaries of minimum of maximum measured values)

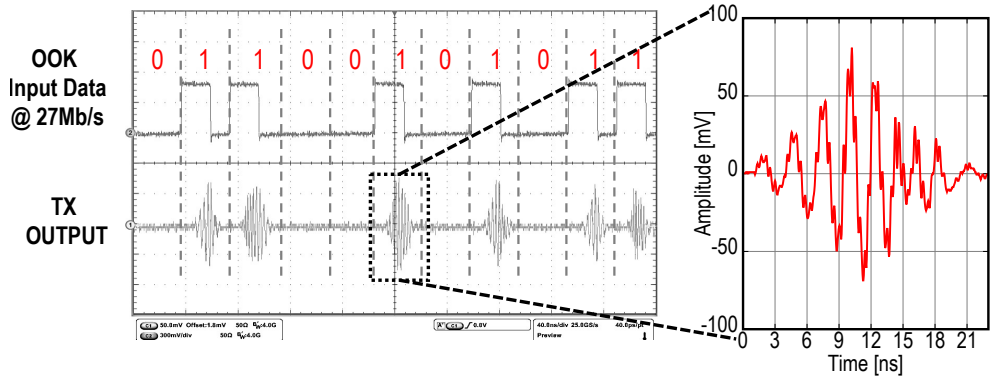
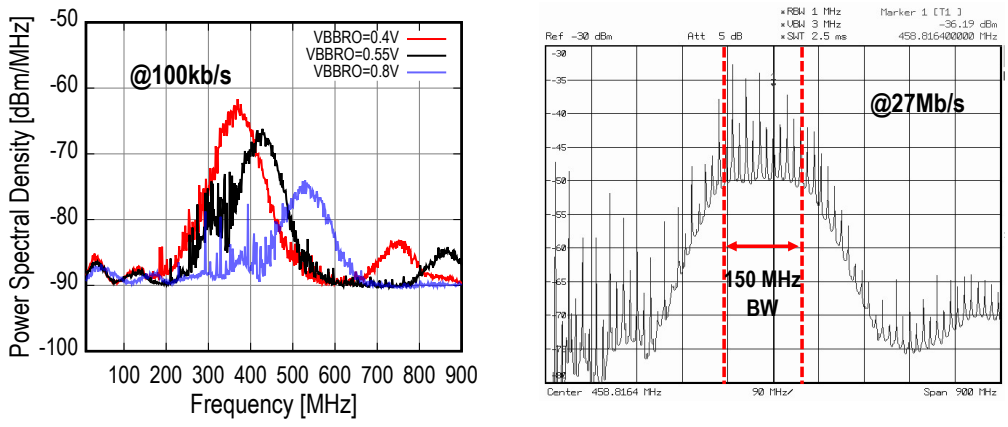


FIGURE 4.17 – Timing response of the TX at the maximum data rate of 27 Mb/s.

4.4.3 Time and Frequency Response

The pulses reach a peak-to-peak amplitude of ~150 mV (Fig. 4.17). The pulses amplitude remains constant at any data rate, which automatically scales the average output power with data rate. Figure 4.18a and Figure 4.18b show the OOK modulated output signal in the time and frequency domains for the low and high data-rates, 100 kb/s and 27 Mb/s, respectively. These measurements highlight the large signal bandwidth and the effect of the pulse shaping. It also shows how the body-biasing voltage on the PD-RO allows for central frequency tuning. We can notice in Figure 4.18b spurs spaced by 27 MHz which corresponds to the pulse repetition rate. However, the frequency response is better at $f_c \approx 350$ MHz ($VBB_{RO} = 0.4$ V) as observable in Figure 4.18. This is due to a slight mismatch of the LC filter at the output, because of parasitics. A slight change of the LC bandpass could result in a performance improvement in terms of output power and efficiency at 450 MHz.



(a) (b)

FIGURE 4.18 – (a) Frequency response for different body-bias voltage on the ring oscillator at 100 kb/s (b) Measured spectrum response at 27 Mb/s

4.4.4 Measurement results of a second chip version

The previously presented measurements were performed on a chip that included a routing mistake in the pulse-shaper, making the pulse shaping slightly asymmetric and limiting the maximum achievable data rate. In a second version of the transmitter, this routing mistake was corrected. Furthermore, a control signal has been added to enable and disable the pulse shaping, allowing to observe the impact of pulse shaping on the frequency response.

We can observe in Figure 4.19 the input and output of the transmitter at the maximum data rate of 45 Mb/s. This corresponds to the theoretically maximum achievable data rate, as the pulse duration is 22.22 ns. At this data rate the transmitter achieves a power consumption of 116.3 µW which translates into an energy efficiency of 2.58 pJ/b, with an optimal body-biasing of 2.2 V. At this optimal body-biasing, the transmitter delivers -17.3 dBm output power, corresponding to a 18 % system efficiency.

In Figure 4.20, we observe the impact of pulse shaping on the frequency response of the transmitter. It is clear that a rectangular shaping, i.e. no shaping (Fig. 4.20a) contains much more sidelobes emissions compared to a Gaussian shaped pulse (Fig. 4.20b), confirming what was expected by the theory explained previously.

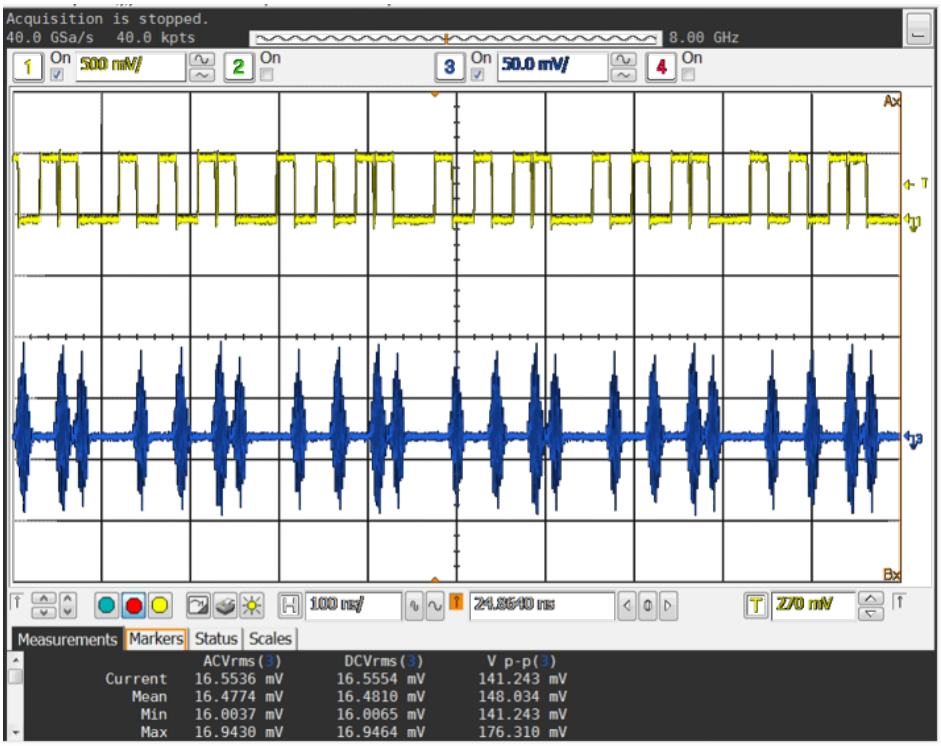
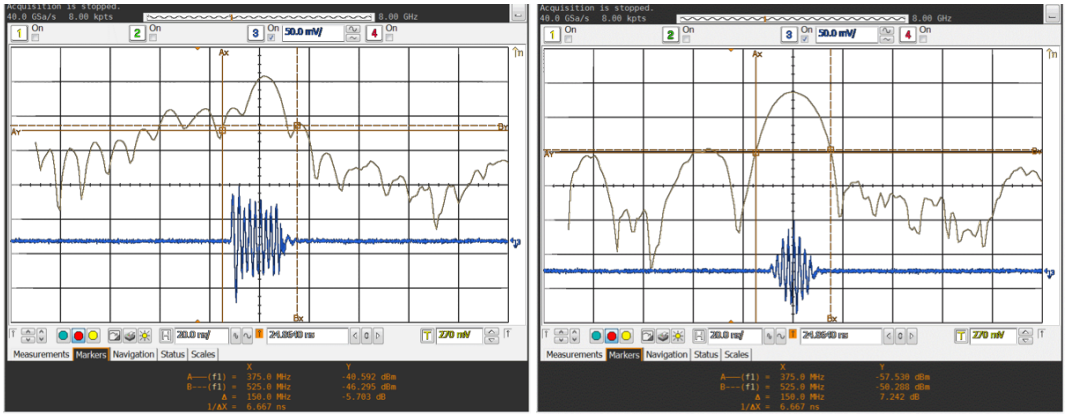


FIGURE 4.19 – Timing response of the TX at the maximum data rate of 45 Mb/s



(a) (b)

FIGURE 4.20 – Frequency and timing response of (a) a rectangular shaped (i.e. no shaping) pulse and (b) a Gaussian shaped pulse.

4.4.5 On-Body Demonstration

Finally, as a proof of concept, a demonstration of the signal propagation on the human body is performed with the measurement set-up described in Figure 4.21. On-body measurements are challenging for c-BCC because the ground planes must be considered carefully [15]. The transmitter is battery powered to avoid earth-grounded supply but the PCB-ground remains large and the amplifier at the RX side has an earth-grounded power supply. Although using SW as the dominant propagation mechanism limits the impact of the return path by nature, it should still be noted that such a setup is not fully representative of a communication between on-battery wearable devices with small ground planes. The signal propagation is demonstrated in two scenarios. The first scenario (in red in Figure 4.22 and in Figure 4.23 in picture) demonstrates a communication along the arm where the two electrodes are in line-of-sight with a distance up to 50 cm.

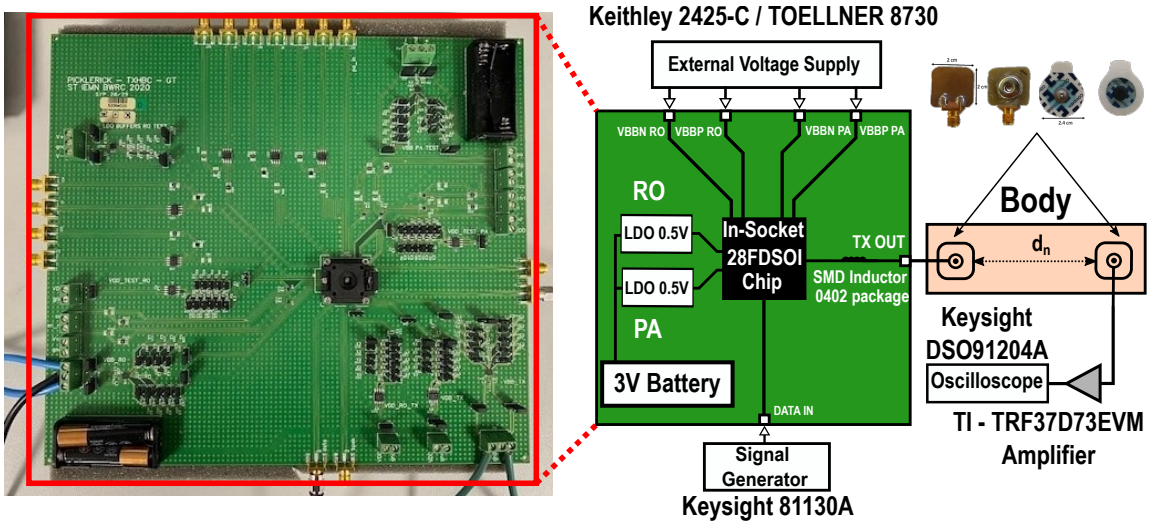


FIGURE 4.21 – Set-up for on-body demonstration

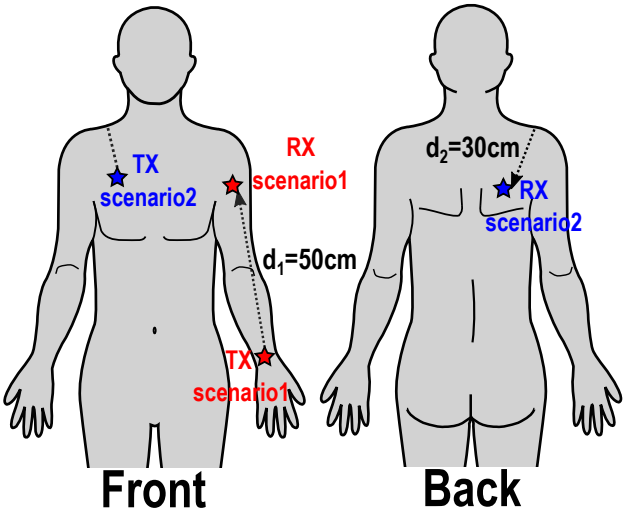


FIGURE 4.22 – Scenarios for on-body demonstration

In the second scenario (in blue in Figure 4.22), one electrode is placed on the pectoral while the second is placed on the shoulder blade (Fig. 4.23). In this scenario, the electrodes are non-line-of-sight and spaced from each other at a distance of 30 cm (following the path along the body). This second scenario helps to demonstrate the capabilities of body coupled communication when undergoing the body shadowing effect. A 4 cm² electrode (similar to the one used in [16]) is wired to the output of the battery-powered TX and attached to the body. As a receiver, a TRF37D73EVM amplifier from Texas Instruments, offering a 20 dB gain with 3.5 dB NF, is attached to a second electrode with the same dimensions. The signal is then observed and recorded on a digital oscillo-

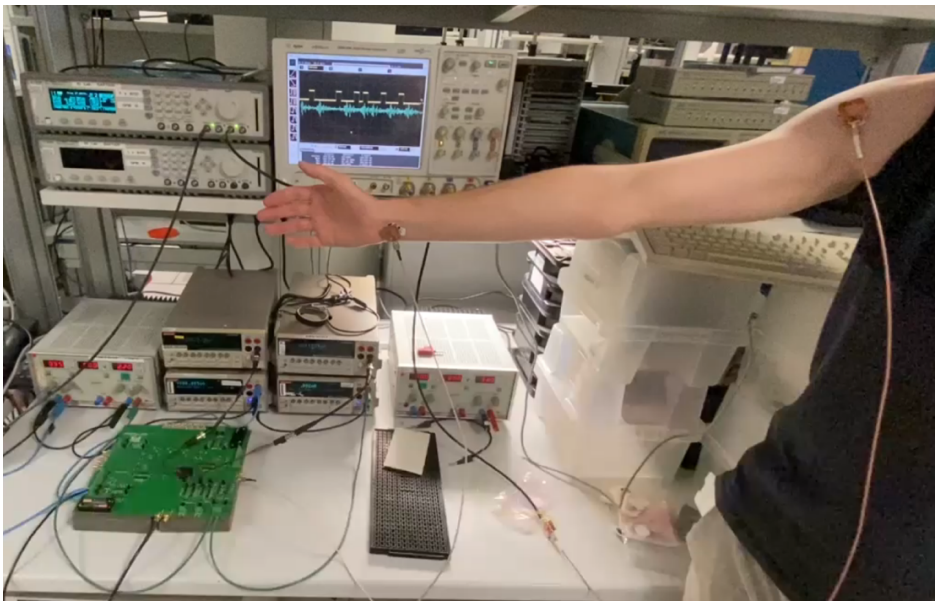


FIGURE 4.23 – Picture of the body-coupled demonstration on the arm

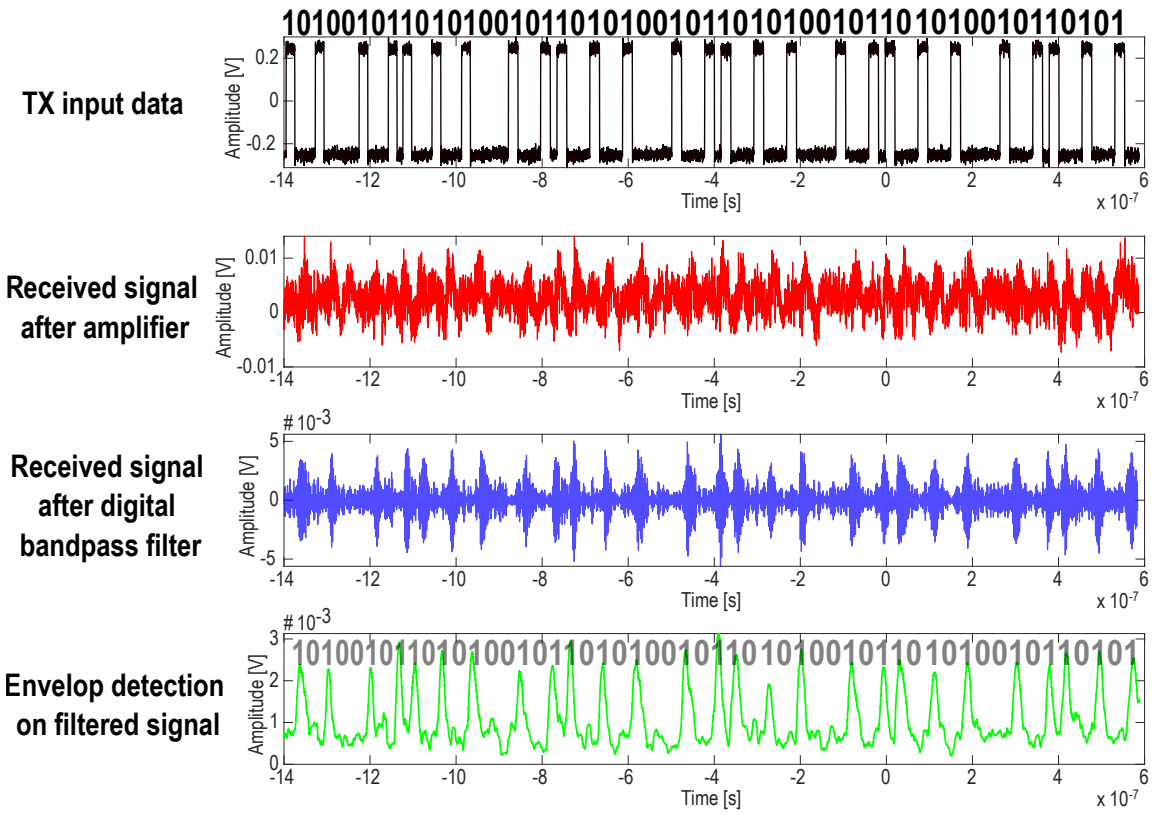


FIGURE 4.24 – Signal processing on the measured received signal for the pectoral to shoulder scenario

scope from Keysight (DSO91204A). In Figure 4.24 post-measurement signal processing is applied on the measured received signal. After applying a digital band-pass filter and envelope detection, the data can be easily retrieved. This shows that simple filtering, envelope detection and a comparator would allow to receive and demodulate the data. Furthermore, it is notable that when the electrodes are not attached to the body (air propagation) the signal is merely observable over a few centimeters. This demonstrates that the mechanism of propagation is truly body-coupled and not because of the electrodes acting as antennas with over-the-air propagation. A video of the full demonstration is available at [17].

4.4.6 State of the Art Comparison

The TX performances are summarized in Table 4.2 and compared with the most recent state of the art for BAN transmitters. For a visual comparison of the TX performances, the total power consumption is plotted versus the data-rate and compared with state of the art TXs in Figure 4.25. The power consumption of the surface-wave transmitter is at par or better than the state-of-the-art over the full range of data-rates. When compared to UWB TX, this work shows a ~5X improvement in energy-efficiency at both high and low data-rates for similar output power [8] without

suffering from the body shadowing effect. Compared to m-BCC [18] the TX achieves a 20 % reduction in power consumption at equal data-rate (5 Mb/s) with similar output power. With respect to a c-BCC (EQS) TX [19], this SW solution improves the energy-efficiency by 11X and 1.2X, for high and low data-rates, respectively over the state-of-the-art. In comparison with [20], this work offers a wider range of operating data-rate and a higher maximum achievable data-rate with equivalent energy-efficiency order. [21] also reports a 30 Mb/s transmitter with similar energy-efficiency (~3 pJ/b) but does not take into account the power consumption of the clock generation, which can easily be predominant in such low power circuits. Similarly, [22] reaches a very high data-rate up to 150 Mb/s with 3.5 pJ/b energy-efficiency but does not take into account the power consumption of the frequency synthesis. Finally, [23] also reports a very high data-rate up to 80 Mb/s but at the cost of a 22X higher power consumption. The key techniques to reach state of the art energy-efficiency are : 1) ultra-low voltage operation enabled by body-biasing 2) pulse-based communication for high duty-cycling 3) massively low-frequency operated architecture to reduce dynamic power consumption.

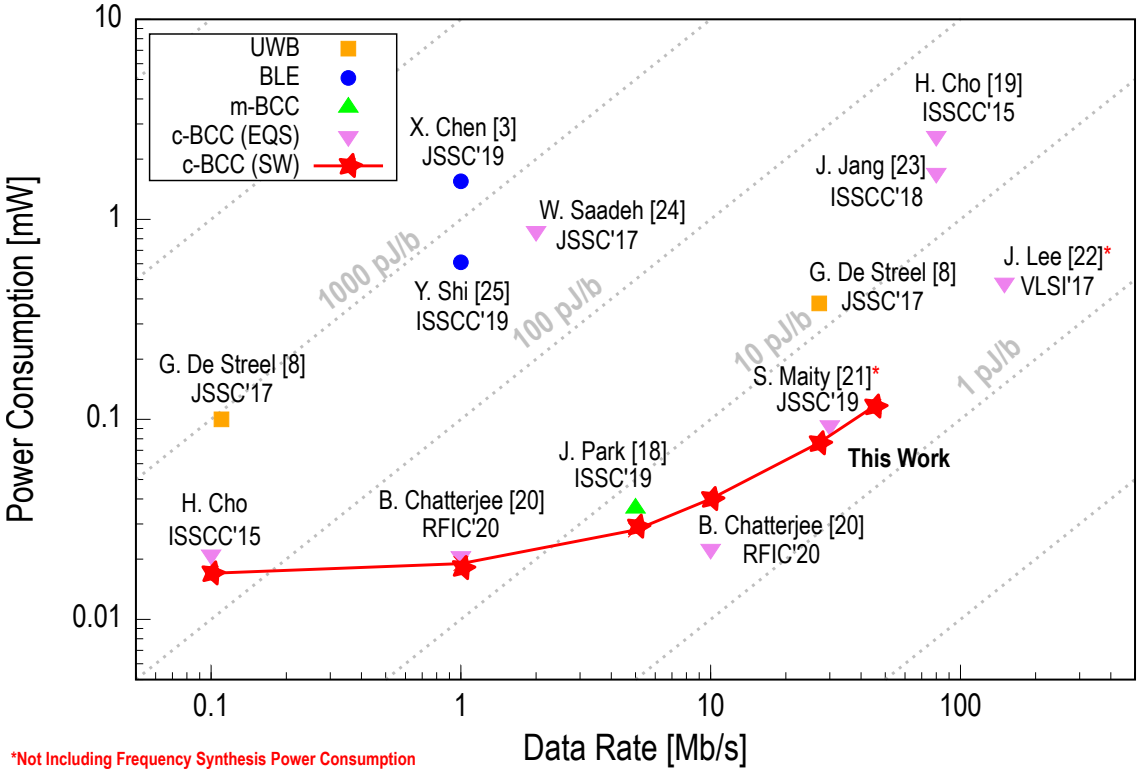


FIGURE 4.25 – TX State of the Art Comparison

TABLE 4.2 – State of the art comparison for BAN TX

	This Work		H. Cho [19] JSSC'15		J. Lee [22] VLSI' 17	W. Saadeh [24] JSSC' 17	J. Jang [23] JSSC' 19	S. Maity [21] JSSC'19	B. Chatterjee [20] RFIC' 20		J. Park [18] JSSC'19	G. De Streel [8] JSSC'17		X. Chen [3] JSSC' 19	Y. Shi [25] ISSCC' 19
Radio Technology	**C-BCC (SW)**		C-BCC (EQS)		C-BCC (EQS)	C-BCC (EQS)	C-BCC (EQS)	C-BCC (EQS)	C-BCC (EQS) IEEE 802.15.6		M-BCC	UWB IEEE 802.15.4a		BLE	BLE
Process Technology	**28nm FD-SOI**		65nm		65nm	65nm	65nm	65nm	65nm		65nm	28nm FD-SOI		40nm	65nm
Carrier Frequency [MHz]	**350 - 550**		13.56	20 - 60 140 - 180	Baseband <100MHz	20 - 120	20 - 60 100 - 180	Baseband <100MHz	22.27		40	3500 - 4500		2400	2400
Supply Voltage [V]	**0.5**		1.2	1	Not Reported	1.1	1	1	0.7		0.6	0.55		0.6	1.2
Data rate [Mb/s]	**0.1**	**45**	0.1	80	100	2	80	30	1	10	5	0.11	27	1	1
Modulation	**OOK**		OOK	BPSK	Decision Feedback Equalization	P-OFDM BPSK	QPSK BPSK	NRZ	OOK		OOK	BPM/BPSK		GFSK	GFSK
TX Power Consumption [µW]	**17**	**116.3**	21	2600	350*	870	1700	93*	20.6	22.4	37	100	380	490	610
TX Energy per bit [pJ/b]	**170**	**2.58**	210	32.5	3.5	435	22	3.1	20.6	2.24	7.2	950	14	490	610
Output Power [dBm]	**-33.8**	**-17.3**	Not Reported		Not Reported	Not Reported	Not Reported	Not Reported	Not Reported		-24.8	-20		-19	-8.4
TX System Efficiency [%]	**2.44**	**18**	Not Reported		Not Reported	Not Reported	Not Reported	Not Reported	Not Reported		17.8	2.6		2.6	23.6
Area [mm²]	**0.0418**		0.1672	5.76	0.00348	0.54	1.3	0.02	0.117		0.0204	0.095		0.0166	0.494

* Note : Not including frequency synthesis power consumption

4.5 Conclusion

A 0.5 V 28 nm FD-SOI CMOS ultra-low voltage transmitter with flexible data-rate (100 kb/s to 45 Mb/s) and using capacitive body-coupled communication with surface wave propagation is presented. The highly duty-cycled transmitter with pulse-based communication uses a low frequency, body-bias controlled oscillator and a switched-mode power amplifier with embedded frequency multiplier, Gaussian pulse shaping, and body-bias efficiency optimization. The one-time calibration, through body-biasing, of the PD-RO and the EC-SCPA is made externally. In future work, a complete SoC implementation with an integrated body-bias generator [14] and periodic calibration with an on-chip reference should be designed. Such additional parts will surely add power consumption overhead to the transmitter. However, integrated body-biasing would also enable duty-cycled body-biasing, meaning that the body-biasing would be duty-cycled by the input data like the rest of the transmitter. Hence, it will decrease the static power consumption due to leakage currents.

When compared to body-coupled transmitter state of the art, the proposed TX solution shows better flexibility as addressing a wider operation data-rate, while staying at par or better in terms of energy-efficiency. Moreover, the surface wave body-coupled link has been successfully demonstrated on-body using an off-the-shelf receiver. Future work will focus on the integration of an on-chip periodic calibration loop, on-chip body-biasing generation, electrode design with emerging flexible electronics, the design of a receiver to demonstrate a full data transfer on-body, and implementation of the MAC protocol [26] for a full demonstration of the Human Intranet network [27].

4.6 References

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Chapter 5

Power Efficient Design of Switched-Capacitor Power Amplifier with Forward Body-Biasing

Contents

5.1 Switched Capacitor Power Amplifier

The SCPA is composed of an array of M capacitances C_u and switches (Fig. 5.1). A switch slice is designed with a CMOS inverter driven by a buffer chain and enabled by a NAND gate. The phase and frequency information is carried through the Local Oscillator (LO). A given number of slices m of the array is enabled dynamically by a digital code-word $a = \{a_1, a_2, ..., a_M\}$ controlling the envelope amplitude of the output signal. Hence, the ideal output power in continuous wave is given by [1] :

$$P_{out,id} = \frac{2}{\pi^2}\left(\frac{m}{M}\right)^2 \frac{V_{dd}^2}{R_L} \tag{5.1}$$

Where V_{dd} is the supply voltage and R_L is the load. For an ideal SCPA, the only source of loss comes from the dynamic power required to charge and discharge the capacitance array [1]. The Drain Efficiency (DE) is defined as the ratio of the output power to the power drawn from the supply by the switches. The switches are CMOS inverters where the PMOS is connecting the output to V_{dd}, while the NMOS is in OFF-state, for half a period, and the NMOS is connecting the output to the ground, while the PMOS is in OFF-state, during the other half of the period. The ideal peak DE is 100 % and the ideal DE at power back-off (i.e., $m < M$) is defined as [1] :

$$\eta_{id} = \frac{P_{out,id}}{P_{out,id} + \frac{m(M-m)}{M^2} C V_{dd}^2 f_c} = \frac{4m^2}{4m^2 + \frac{\pi m(M-m)}{Q_L}} \tag{5.2}$$

$$Q_L = \frac{1}{2\pi \cdot f_c \cdot C \cdot R_L} \tag{5.3}$$

Where C is equal to the sum of the unit capacitances C_u, f_c is the operating frequency, and Q_L is the loaded quality factor.

The first source of loss in a SCPA is due to the ON-resistance r_{on} of the MOSFETs. The common technique to reduce losses is to increase their widths to reduce r_{on}. However, careful optimization of the MOSFETs' width is required as it linearly increases the parasitic capacitance C_p making the dynamic losses predominant [2]. It has been shown [3], that the use of FBB lowers

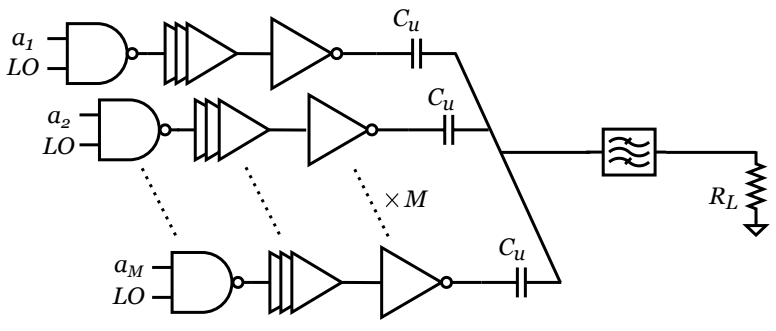


FIGURE 5.1 – SCPA Schematic

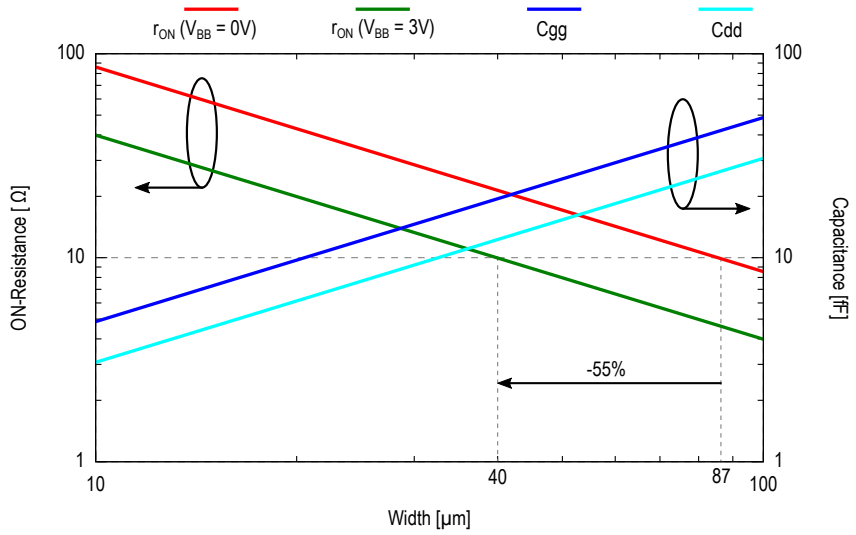


FIGURE 5.2 – Associated ON-resistance, C_{gg} and C_{dd} for a LVT NMOS transistor versus transistor width (L=30 nm)

the ON-resistance of the MOSFETs and positions the FD-SOI technology as a great candidate for switched-capacitor circuits. The proposed idea is to use the forward body-biasing feature of the 28 nm FD-SOI technology to reduce r_{on} while limiting the parasitic capacitances. We can observe in Figure 5.2 the ON-resistance, the total input capacitance C_{gg} and total output capacitance C_{dd} for a LVT NMOS transistor (L = 30 nm), for the minimum and maximum body-biasing voltage (0 and 3 V). Figure 5.2 shows that FBB of 3 V allows to reduce by 55 % the width of the transistor for the same r_{on} value. Hence, this directly translate by a 55 % reduction of the input and output capacitances, as they are linearly proportional to the width of the transistor. Thus, reducing the dynamic power consumption. However, FBB exponentially increases the leakage of the MOSFETs when they are in OFF-state. Then, it exists an optimal point of operation where FBB allows to re-

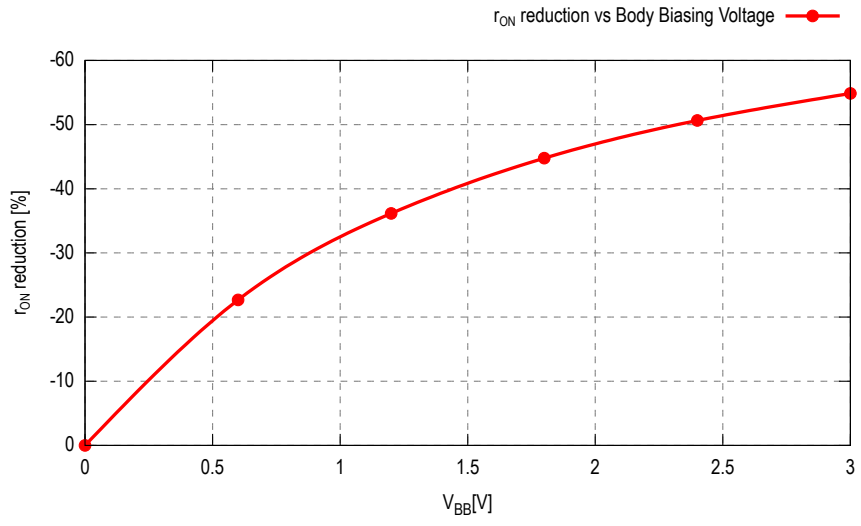


FIGURE 5.3 – ON-resistance reduction versus forward body-biasing voltage (V_{BB}) on LVT NMOS (L = 30 nm)

duce the dynamic power consumption due to the parasitic capacitance while limiting the leakage power consumption. Figure 5.3 shows the r_{on} reduction percentage as a function of the body-bias voltage. The following sections propose drain and system efficiency models to help find the optimal operation point.

5.2 Drain Efficiency Model

The equivalent model of a SCPA is represented in Figure 5.4. The Drain Efficiency can be written as :

$$\eta = \frac{P_{out}}{P_{out} + P_{sc} + P_{diss} + P_{dyn} + P_{leak}} \tag{5.4}$$

Where P_{diss} is the dissipated power in r_{on}, P_{dyn} is the dynamic power dissipated due to C_p, the parasitic capacitance, and P_{leak} is the static dissipated power due to the current leakage. P_{sc} corresponds to the dynamic power required to charge and discharge the capacitance array at Power Back-Off (PBO) and is equal to [1] :

$$P_{sc} = f_c \cdot V_{dd}^2 \cdot \frac{m(M-m)}{M^2} \cdot C \tag{5.5}$$

The calculations of these three sources of losses, including the body-bias parameter, are detailed in the following sub-sections.

5.2.1 Losses due to ON-Resistance

The ON-resistance lowers the output power as it acts as a voltage divider and dissipates power :

$$P_{out} = \frac{2}{R_L}\left(\frac{m}{M}\right)^2 \left(\frac{V_{dd}}{\pi}\frac{R_L}{R_L + r_{on}}\right)^2 \tag{5.6}$$

$$P_{diss} = \frac{2}{r_{on}}\left(\frac{m}{M}\right)^2 \left(\frac{V_{dd}}{\pi}\frac{r_{on}}{R_L + r_{on}}\right)^2 \tag{5.7}$$

Where the equivalent r_{on} model, with body-bias parameter is :

$$r_{on} = \frac{L}{W \cdot K \cdot [V_{dd} - (|V_{T0}| - \gamma|V_{bb}|)] \cdot M} \tag{5.8}$$

Where V_{T0}, the nominal threshold voltage, γ, the body factor, and K (typically equal to $\mu_{eff}C_{ox}$) are all technology parameters. L and W are the length and the width of the transistors, respectively, and V_{bb} is the body-biasing voltage. Thus, to reduce the ON-resistance we can increase the switches' width and/or the body voltage. In the 28 nm FD-SOI technology, the body factor is ~85 mV/V for the thin oxide LVT devices and the body voltage variation can range up to +/- 3 V [4] allowing to

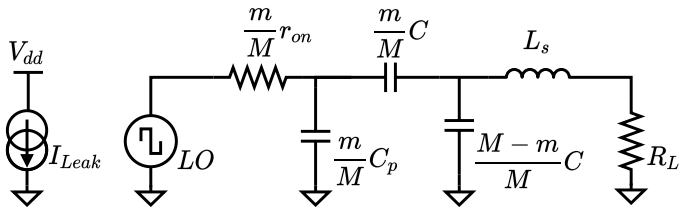


FIGURE 5.4 – Equivalent circuit model of the SCPA including ON-resistance, parasitic capacitance, and leakage

reduce the threshold voltage and hence the r_{on}. As a rule of thumb, PMOS width to NMOS width ratio has to be sized such as $r_{on,p} \approx r_{on,n}$ to minimize the losses [1].

5.2.2 Dynamic Power Dissipation in switches

Dynamic dissipated power in the switches is due to the power required to charge and discharge the parasitic capacitance C_p of the MOSFETs. The dynamic power consumption is expressed by :

$$P_{dyn} = \left(\frac{m}{M}\right) \cdot f_c \cdot C_p \cdot V_{dd}^2 \cdot k_{sc} \tag{5.9}$$

Where the factor k_{sc} represents the short-circuit current loss. Typically, k_{sc} is inferior to 1.1 (ideally equal to 1) for equal rise/fall transition times [5]. The total parasitic capacitance C_p is linearly proportional to the width of the switches and is equal to $C_p = b \cdot W \cdot M$ where b is a technology parameter.

5.2.3 Static Power Dissipation in switches

Static power dissipation is mainly due to the subthreshold leakage and Drain-Induced Barrier Lowering (DIBL) leakage when the transistors are in OFF-state [6]. The leakage power dissipation is expressed as :

$$P_{leak} = V_{dd} \cdot I_{leak} \tag{5.10}$$

$$I_{leak} = 2 \cdot n \cdot K \frac{W}{L} U_{th}^2 \exp\left(\frac{-V_{T0} + \gamma V_{bb} + \lambda V_{dd}}{n U_{th}}\right) \cdot M \tag{5.11}$$

Where n is the subthreshold slope factor, λ is the DIBL factor and are technology parameters. U_{th} is the thermal voltage (kT/q).

5.3 System Efficiency Model

A more relevant metric to evaluate the efficiency of a SCPA is the System Efficiency (SE), which takes into account all the power drawn from the supply by all the external circuitry required to operate the PA : the digital logic, clock tree distribution and driving buffers [7]. However, we define

here the SE as the metric solely taking into account the dissipated power in drivers in addition to the power dissipated in the switches. The buffer chains required to drive the large input capacitance of the switches are the most consuming part in the external circuitry [1]. Furthermore, only the drivers power dissipation is directly dependent on the switch sizing.

$$\mathrm{SE} = \frac{\mathrm{P}_{out}}{\mathrm{P}_{out} + \mathrm{P}_{sc} + \mathrm{P}_{diss} + \mathrm{P}_{dyn} + \mathrm{P}_{leak} + \mathrm{P}_{dr}} \tag{5.12}$$

$$\mathrm{P}_{dr} = \left(\frac{m}{\mathrm{M}}\right) \cdot f_c \cdot \mathrm{C}_{dr} \cdot \mathrm{V}_{dd}^2 \cdot k_{sc} + \mathrm{I}_{leak,dr} \cdot \mathrm{V}_{dd} \tag{5.13}$$

To calculate the power consumption of the drivers, we need to estimate the equivalent drivers' capacitance C_{dr} and their total leakage current. By using the analysis in [8] we can easily calculate the total capacitance in the tapered buffers :

$$\mathrm{C}_{dr} = (\mathrm{F}^{\mathrm{N}} - 1) \cdot \frac{\mathrm{F}\mathrm{C}_x + \mathrm{C}_y}{\mathrm{F} - 1} \cdot \mathrm{M} \tag{5.14}$$

Where F is the tapering factor of the buffer chain, C_x is the input capacitance of a minimum size inverter, C_y is the output capacitance of a minimum size inverter. N is the number of inverter in the driver chain and is defined as $\mathrm{N} = ln(\mathrm{C}_{sw}/\mathrm{C}_x)/ln(\mathrm{F})$. Where C_{sw} is the input capacitance of a switch. By analogy, we can also calculate the total leakage current in the driver chains.

$$\mathrm{I}_{leak,dr} = \mathrm{I}_0 \cdot \frac{\mathrm{F}^{\mathrm{N}} - 1}{\mathrm{F} - 1} \tag{5.15}$$

Where I_0 is the reference current leakage in a minimum size inverter which can be calculated using (5.11).

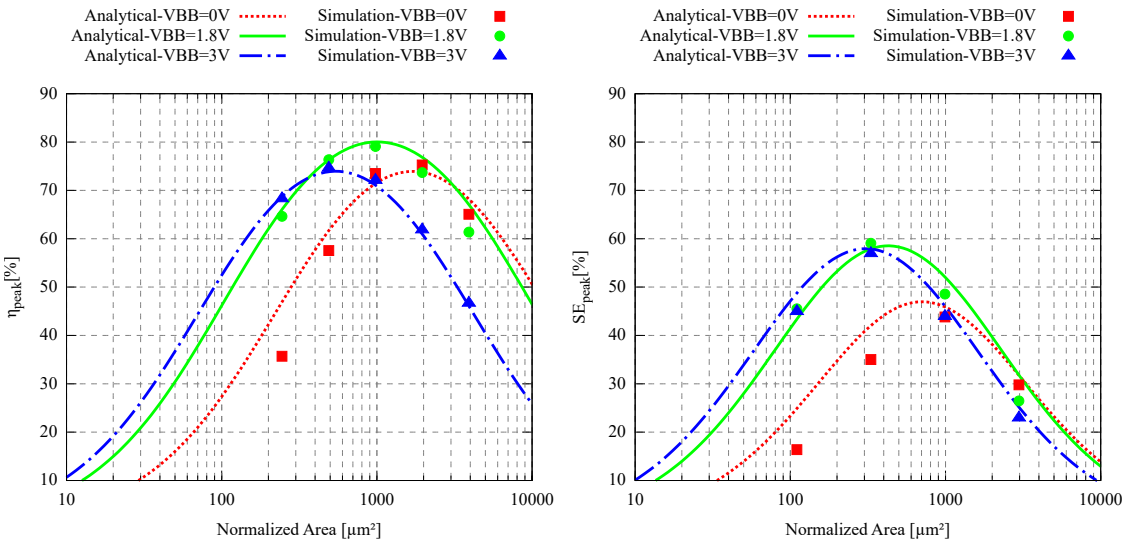
5.4 Simulation Validation

To compare and validate the DE and SE analytical models, simulations are performed with *SpectreRF* using the transistor models of the 28 nm FD-SOI technology from *STMicroelectronics*. The simulations and analytical models are compared for a 2.4 GHz frequency, 0.5 V supply voltage. To limit the leakage impact, the lengths of the transistors are slightly increased by 15 % through poly-biasing of $\mathrm{L}_{min} + 4\ nm$ [9]. For the DE simulations, the drivers are considered ideal, consuming zero power and with the same sizing as the switches (i.e. tapering factor of 1). The NMOS transistors are body-biased with voltages spanning from 0 to 3 V, and the PMOS transistors from 0 down to −3 V, respectively. The body-bias voltages are applied symmetrically (i.e. $\mathrm{V}_{bb} = \mathrm{V}_{bb,\mathrm{NMOS}} = -\mathrm{V}_{bb,\mathrm{PMOS}}$), and homogeneously in both drivers and switches. As the optimal sizing of the PA depends on the R_L value (smaller R_L requires a proportionally larger switches

area), and as R_L is defined by the required output power, we define the normalized area as the switch area for R_L = 1 Ω. In practice, the value of the load is defined by the peak output power targeted by the application. The scaling of R_L to 50 Ω can be achieved with a matching network which is not considered here. Since the scope of this work is to study the efficiency of the active part of a body-biased SCPA, the capacitances C_u and the inductance L_s are considered being ideal and defined for Q_L = 3. For the SE simulations, a standard tapering factor of 3 is chosen in the driver chain.

We can observe in Figure 5.5 the analytical models proposed in this chapter compared to the simulations, with good matching for the peak DE and peak SE (i.e. m = M). By sweeping the value of the FBB voltages in the model, we reach the optimal body-biasing at +/- 1.8 V, where we obtain a 5 % improvement in DE with a significant 50 % area reduction. A stronger body-biasing annihilates any efficiency improvement as the leakage power dissipation becomes predominant (Fig. 5.5a). The reduction in switch area allows to reduce the number of buffers required in the driver chain and thus shows an improvement of 14 % of the SE with a 67 % improvement of the switch area at an optimal body-biasing of +/- 1.8 V (Fig. 5.5b).

We observe in Figure 5.6 the SE at PBO. Here we consider two different designs : the first one (Design A) is the one sized for an optimized peak SE without body-biasing (normalized area of ~ 1000 μm^2 in Figure 5.5.b) and the second one (Design B) is sized for an optimized peak SE when body-biased at V_{bb} = 1.8 and 3 V (normalized area of ~ 330 μm^2 in Figure 5.5b). At – 6 dB PBO a body-biased SCPA at +/- 1.8 V still shows a 10 % improvement compared to a non-body-biased SCPA. With a body-biasing of +/- 3 V the SE decreases more rapidly with PBO, caused by a more



(a) (b)

FIGURE 5.5 – (a) Peak DE and (b) peak SE versus normalized switch area : simulated results compared to the analytical model for different body-biasing voltage

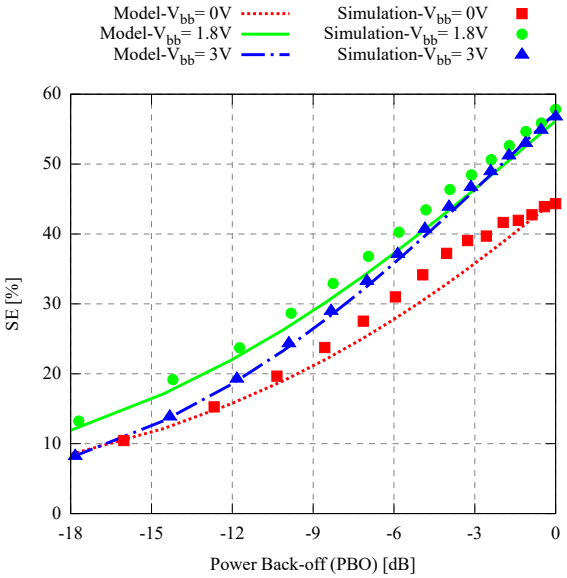


FIGURE 5.6 – Simulated SE compared to the analytical model of SE versus Power Back-Off. V_{bb} = 0 V is on Design A, V_{bb} = 1.8 V and V_{bb} = 3 V on Design B

important leakage power consumption. Furthermore, FBB also allows to compensate PVT variations. As observable in Figure 5.7 the optimal body-bias voltage depends on the process corner. An integrated body-bias generator such as [10] could dynamically tune the body-bias voltage for optimal operation under PVT variations, making the design more robust [4].

It is expected to see more impact of the FBB at higher frequencies as it allows to reduce the parasitic capacitance of the switches, reducing the frequency-dependent dynamic power dissipation, and shall benefit from the high transition frequency f_T of the FD-SOI technologies (~ 300 GHz [4]) for ultra low-power design up to 30 GHz [7, 11].

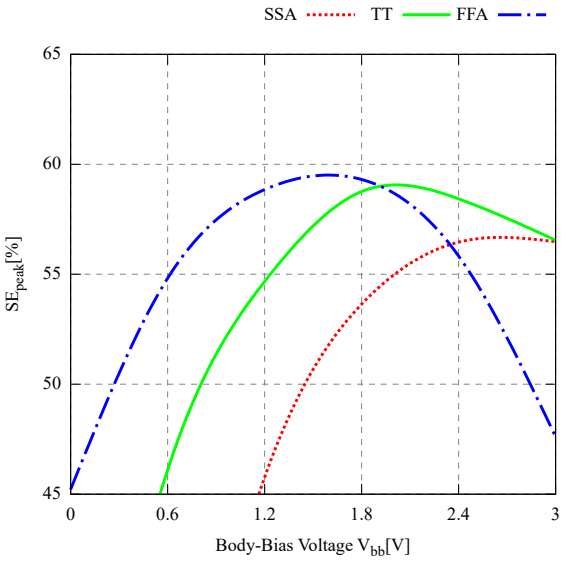
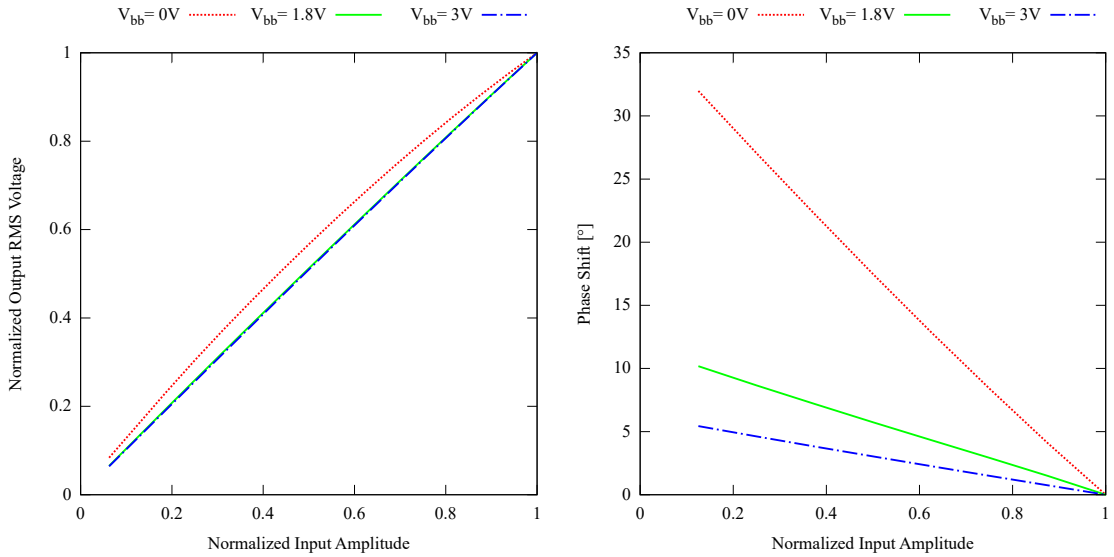


FIGURE 5.7 – Simulated Corners peak System Efficiency versus Body-Bias Voltage (on Design B)



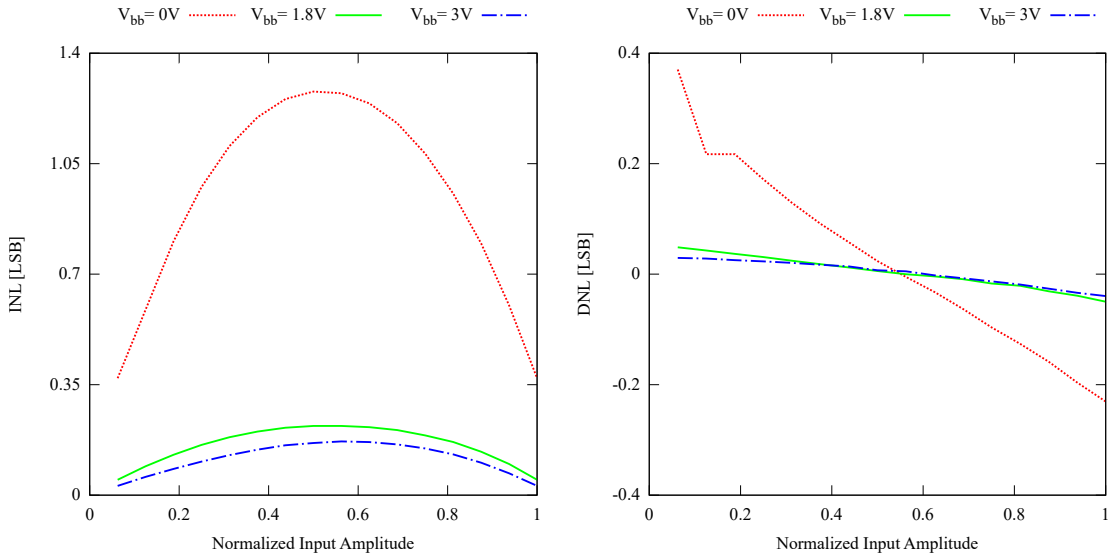
(a) (b)

FIGURE 5.8 – Simulated (a) AM–AM and (b) AM–PM distortion. V_{bb} = 0 V is on Design A, V_{bb} = 1.8 V and V_{bb} = 3 V on Design B

5.5 Impact on Linearity

In this section, we study the impact of Forward Body-Biasing on the linearity by using the simulation results. We consider again the two designs : Design A (sized at normalized area of ~ 1000 μm^2 in Figure 5.5b for V_{bb} = 0 V) and Design B (sized at normalized area of ~ 330 μm^2 in Figure 5.5b for V_{bb} = 1.8 and 3 V).

Linearity can be studied by simulating the AM–AM and AM–PM distortions. Two other interesting metrics are Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) as SCPA are



(a) (b)

FIGURE 5.9 – Simulated (a) INL and (b) DNL. V_{bb} = 0 V is on Design A, V_{bb} = 1.8 V and V_{bb} = 3 V on Design B

basically RF-DACs. Nonlinear distortion is mainly due to two effects in SCPAs : (1) non-zero switching times (2) source impedance variations, r_s, depending on the input amplitude code and the parasitics (r_{on}, C_p) [1, 12, 13]. FBB has a positive impact on those two effects. It mainly allows to dramatically increase the switching speed of the inverters [4]. As demonstrated in the previous section, it also allows to obtain a more compact design and thus to reduce even more the ON-resistance and C_p parasitics. Hence, it reduces the AM–AM distortion and divides by 3 to 5 the maximum AM–PM phase shift distortion for V_{bb} = 1.8 V and V_{bb} = 3 V, respectively (Fig. 5.8). This is also observable in the INL/DNL metrics (Fig. 5.9) where FBB permits to drastically reduce the error conversions.

5.6 Conclusion

This section demonstrates that forward body-biasing of low-voltage SCPA in FD-SOI technology reduces the ON-resistance of the switches, while limiting the increase of the parasitic capacitance. This allows the reduction of the switch area by 67 % and improves by 14 % the SE at 2.4 GHz. It is also shown that forward body-biasing allows for a more robust design by selecting the optimal body-bias voltage depending on process corner variations. Ultimately, it is highlighted how forward body-biasing can improve the linearity of SCPAs. Using FBB in FD-SOI technology adds a tuning knob for optimizing the design for energy-efficient, compact, robust and linear Ultra-Low Voltage (ULV) SCPA.

5.7 References

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Chapter 6

Design Considerations for the Receiver

Contents

After building the transmitter, the receiver needs to be designed to demonstrate a full communication link. In this chapter, we will redefine the receiver specifications according to the transmitter's results, explore low-power receivers state-of-the-art, and give some design considerations, opening opportunities for future work.

6.1 Receiver Specifications

The receiver specifications have been defined in Chapter 3. Following the results of the transmitter we can update these specifications. At 100 kb/s the transmitter delivers −33.8 dBm of output power. As the communication distance in the low-data rate mode is meant to be around 15 cm, where the path loss is estimated around 55 dB, it relaxes the sensitivity constraint to −92 dBm (considering a 3dB margin). In another hand the maximum achievable data-rate was measured at 27 Mb/s with −20 dBm output power. If we still consider a noise figure of NF = 6 dB, a bandwidth of BW = 150 MHz and a ratio E_b/N_0 = 14 dB, the sensitivity becomes −80 dBm at 27 Mb/s. Considering a −20 dBm output power at the transmitter and the channel model this corresponds to a communication distance of 30 cm. Hence the Noise Figure (NF) cannot be relaxed and should be equal or less than 6 dB. In terms of power consumption, we would like the receiver to be in the same order of energy-efficiency as the transmitter, meaning sub-200 pJ/b at low-data rate and sub-20 pJ/b for the highest data rate.

It is also important to note that the receiver might be sensitive to narrow-band in-band interferences. Indeed, there is the ISM band at 433 MHz and the Medical Implantable Communication System (MICS) at 402-405 MHz. Hence, the receiver needs to be designed with in-band interference rejection.

6.2 Low-power receivers state of the art

6.2.1 UWB receivers

Many implementations of UWB receivers have been proposed in the state of the art. We focus on implementations proposing non-coherent demodulation with crystal-less reference [1–7]. Most of the implementations propose the use of Envelope/Energy Detection (ED). [1–5] or peak voltage detection [7], as it allows to demodulate the OOK modulated data without the use of a PLL or a mixer, saving power. However, ED-based receivers suffer from poor sensitivity and do not tolerate interferences. The sensitivity issue can be overcome by using a LNA but at the cost of an important power consumption overhead [4, 5]. Gambini et al. [6] has proposed a dual-mode receiver, where a low-power mode is based on a ED architecture and a mixer-first architecture is used

in the second mode to improve performances when the link quality is degraded.

6.2.2 Wake-up receivers

In terms of ultra-low power receivers, Wake-Up Receiver (Wu-RX) have been extensively studied recently. This type of receiver is used as an alternative to duty-cycled radio to avoid idle listening power consumption from the main radio. The wake-up radio is designed for ultra-low power consumption, and turn the main radio on when a wake-up signal is received, saving the overall stand-by power consumption of the receiver. They usually operate at very low data-rate for sensitivity and low-power reasons. Although the specifications of Wu-RX are quite different to main radio RX, we can inspire from the low-power design concepts they are using [8]. To save power, some Wu-RX are reaching sub-µW power by using envelope/energy detection, which again suffers from poor sensitivity because of their large noise bandwidth. The sensitivity can be improved by ~20 dB by using a impedance transformer with a high quality factor at the front-end, providing passive gain and filtering [8–10]. If ED architectures in Wu-RX reach extremely low-power, they also are limited to extremely low data rate. Most ED are using rectifiers with a high number of stages, which requires long charging time, limiting the data rate to a few hundreds of bit per seconds[9, 10]. An alternative to ED-first receivers is the mixer-first architecture. Mixer-first architecture can achieve better sensitivity performances than ED-first architecture at the cost of a higher power consumption [11, 12], but still achieving sub-100 µW power consumption. The dominant power consuming part in the passive mixer-first RX is the LO and its drivers. In order to reduce the LO power consumption, the conventional LC oscillator can be replaced with a RO as in [11]. Furthermore, [11, 12] use an *Uncertain-IF* architecture. This architecture allows for the use of an unlocked LO, avoiding the use of a power consuming PLL. The "uncertainty" of the down-converted frequency is then further compensated by an IF-amplifier with an increased bandwidth.

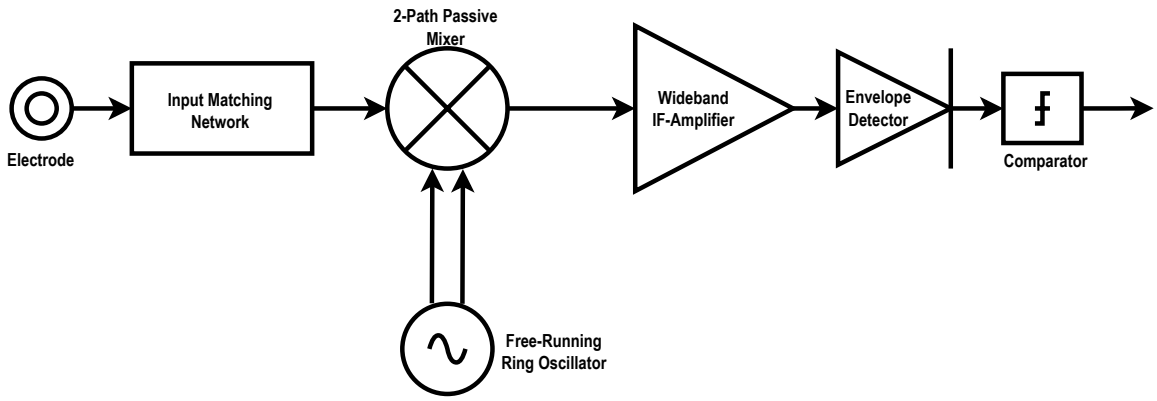

FIGURE 6.1 – Example of a Uncertain-IF RX Architecture

6.3 Receiver Architecture

Following the receiver specifications and the state of the art study we decide to explore the mixer-first architecture with uncertain-IF downconversion such as in [11, 12]. However, these implementations have been proposed for narrow-band communication and must be adapted to pulse-based wideband communication.

6.3.1 2-path passive mixer

As we consider an OOK demodulation, which does not require quadrature-phase demodulation, a 2-Path Passive Mixer (2-PPM) is considered similarly as in [12] (Fig. 6.2). In Figure 6.2, R_s represents the source impedance of the antenna/electrode, R_{sw} represents the ON-resistance of the switches, and $R_{IF}C_{IF}$ is the baseband low-pass filter load. Following the analysis in [12], a 2-PPM can be approximated by a Linear Time Invariant (LTI) model as in Figure 6.3. The virtual shunt resistance R_{sh} models the baseband energy radiated back to the input path due to the backward mixing with the LO signal. Considering the LTI model, the effective input impedance presented by the 2-PPM at the fundamental LO component equals $R_{sw} + (R_{sh}||R_{IF})$. Hence, impedance matching to the input source ($Z_{in}(\omega_{LO}) = R_s$) is provided for a specific value of R_{IF} , which is labeled $R_{IF,match}$ [12].

A 2-PPM architecture saves power, as it limits the number of switches and avoids the use of frequency dividers, compared to a N-PPM (with N ≥ 4) architecture, at the cost of no image-rejection and higher noise factor. A passive mixer behaves as a switched-capacitor circuit. Hence, the ON-resistance should be minimized to reduce losses and improve the noise performance. As usual in switched-capacitor circuits, the most common technique is to increase the width of the switches

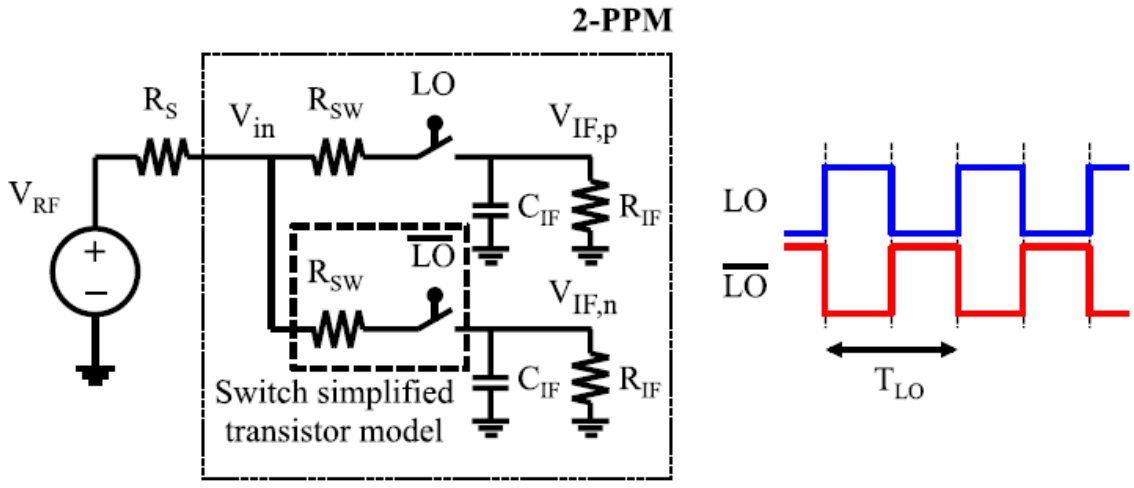

FIGURE 6.2 – Simplified single-to-differential 2-path passive mixer model (Taken from Salazar et al. [12]).

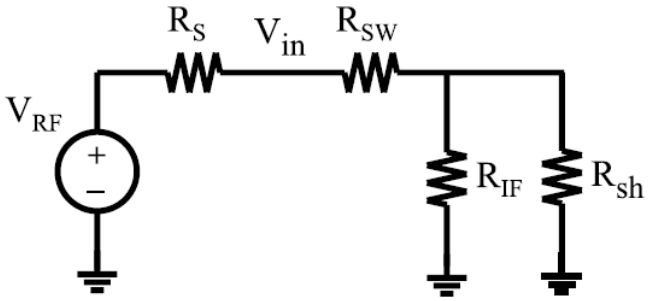

FIGURE 6.3 – Two-path passive mixer linear time invariant equivalent model (Taken from Salazar et al. [12]).

to reduce the ON-resistance to a minimum. However, increasing the width of the transistors increases the load capacitance of the LO drivers, which increases their power consumption. As similarly as for the SCPA, we propose a preliminary study on the impact of FBB on passive mixers to save power.

As presented in the previous chapter, applying a body-biasing voltage on a transistor can reduce its width by up to 55 % for a constant ON-resistance. Hence, we simulate a 2-PPM for different switches sizing within the full body-bias range (such as the ON-resistance remains constant) to observe what is the impact on the single-to-differential DC voltage conversion gain (A_{v_0}) and the NF of the passive mixer. The simulation results are presented in Figure 6.4. We can observe that the width reduction through body-bias actually degrades the gain and noise performance of the mixer.

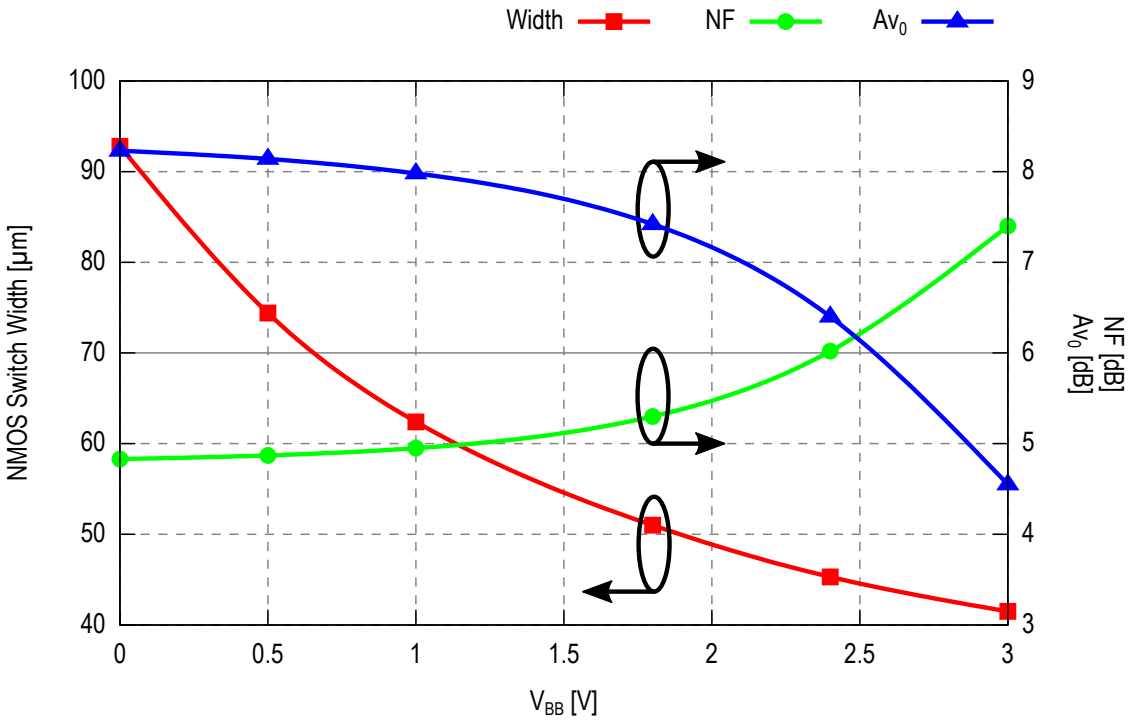

FIGURE 6.4 – NMOS switches width, voltage conversion gain, and noise factor versus body-biasing voltage, for R_{sw} = 9.5 Ω constant, $R_{IF} = R_{IF,match}$ and R_s = 50 Ω at 450 MHz.

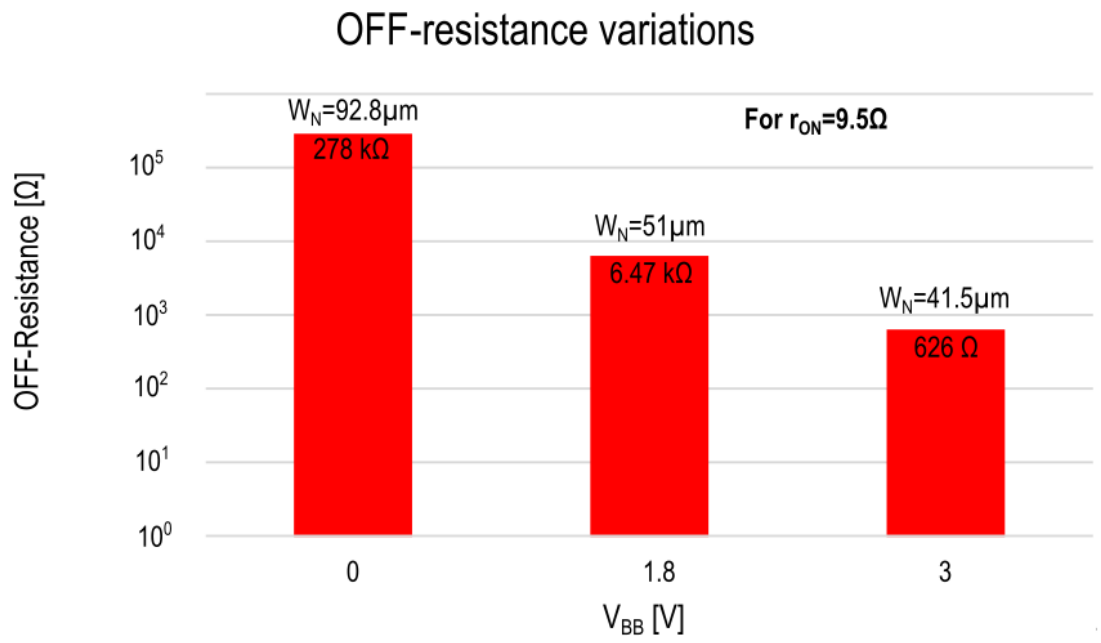

FIGURE 6.5 – OFF-resistance for 3 transistors sizing with 3 different body-bias such as their ON-resistance are equal to 9.5 Ω.

Which can be surprising, as the models described in [12] of both the voltage conversion gain and the noise factor are given as a function of R_{sw}, R_s, and R_{IF}, which are kept constant. To further investigate the reasons of such performances degradation, we investigate the OFF-resistance of the switches. Indeed, applying forward body-biasing on the transistors reduces the ON-resistance but also reduces the OFF-resistance of the switches if the bias is static.

To verify this hypothesis, the 2-PPM is simulated again with a dynamic body-biasing which is in phase with the LO. This means that the body-biasing is applied only when the switches are ON. In this case, the noise factor and voltage conversion gain remain constant, confirming that the performances degradation is due to the OFF-resistance of the switches. As observable in Figure 6.5 the OFF-resistance of the switches when the body-bias voltage is 0, 1.8 and 3 V and when all are sized for a ON-resistance of 9.5 Ω (defined as the minimum switch resistance for matching according to [12]). We observe that for a body-bias of 3 V the OFF-resistance is reduced by more than 2 order of magnitude as down to 626 Ω. Such a low value of the OFF-resistance inherently changes the input impedance, degrading the voltage conversion gain and noise factor of the passive mixer. To fully understand the impact of the OFF-resistance on the passive mixer, the 2-PPM model presented in [12] should be updated. This will be further investigated in future works.

Altogether, we can still notice in Figure 6.4, that for a static 1.8 V forward body-bias voltage, the width of switches can be reduced by 45 % while merely degrading the gain and NF performances by less than 1 dB. Hence, we can reduce by 45 % the power consumption of the LO drivers at the cost of less than 1 dB of performances degradation.

6.4 Conclusion

This chapter introduced some design considerations for the design of a pulse-based receiver to perform a full-link communication with the proposed transmitter. After updating the specifications according to the transmitter results, we explored the state of the art in UWB receiver and wake-up receivers. From the specifications and the state of the art study, we concluded that a passive mixer-first with uncertain-IF architecture is worth exploring for low-power consumption with both low and high data rates. Then, a preliminary study of a body-biased passive mixer has been proposed. As it has already been demonstrated, the body-bias feature of the 28 nm FD-SOI technology allows area and dynamic power consumption reduction in switched-capacitor circuits. This principle was applied to the passive-mixer to study its impact on the gain and noise factor. We concluded that, although body-biasing allows to reduce the size of the switches, it degrades the noise and gain performance of the mixer, because of the drastic reduction of the OFF-resistance. However, keeping the body-biasing voltage at around 1.8 V, would allow a 45 % reduction of the LO driver power consumption, while limiting the performance degradation to less than 1 dB for both the noise factor and the voltage conversion gain. We could also consider the implementation of a dynamic body-biasing in phase with the LO, but it should be investigated if the power overhead is not overcoming the gain in the LO driver power consumption. Overall, this chapter provides some food for thoughts for future work on the design of the receiver.

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Chapter 7

Conclusion and Future Work

Contents

7.1 Conclusion

This research work has been focusing on the design of an ultra-low power transmitter with a flexible data rate for the Human Intranet. The concept of the Human Intranet has been introduced with their associated challenges and opportunities. While the Human Intranet contains various research topics in computing, biosensing and networking, this work has been focusing on the design of a wireless transceiver to efficiently interconnect various sensors and actuators on the human body, for medical and wellness applications. Five requirements have been highlighted to answer these challenges : a flexible data rate, a small form factor for comfortable wearability, low-power consumption for energy-efficiency, long-range communication for good body coverage, and robustness.

Considering these challenges, the state of the art of the communication options around the human body has been extensively studied at both the channel and transceiver design levels. Most common RF-based solutions such as Bluetooth or UWB suffer from the body shadowing effect and hence undergo strong path loss, as well as channel instability and inconvenient antenna form factor. As an alternative, BCC has been recently studied to overcome the body shadowing effect by using the human body as the channel itself. Three main BCC mechanisms have been considered from today's literature : magnetic BCC, galvanic BCC and capacitive BCC [1]. Magnetic BCC offers low path loss but suffers from bulky magnetic coils that can not be worn easily on every part of the human body. Galvanic BCC offers a very stable channel against motion and environment changes, offering a robust communication, but undergoes a strong path loss, drastically limiting the communication distance to a few centimeters. Capacitive BCC, on another hand, offers a low path loss channel with only one on-body electrode, but suffers from environment variations because of the strong dependencies of the capacitive return path. More specifically, the proposed transceivers in the state of the art for capacitive BCC are operating in the electro quasi-static mode, where the frequency of operation is below 200 MHz. Previous work has proposed a channel model with measurements for the use of capacitive BCC with a frequency of operation up to 500 MHz, where surface wave propagation becomes predominant [2]. Increasing the frequency of operation enables a larger bandwidth of communication, allowing to reach higher data rates. It is also expected to be less sensitive to the environment variations as the surface wave component is less sensitive to the return path by nature. Numerous transceiver designs have been proposed using capacitive BCC with electro quasi-static communication. However, no implementation has been proposed yet for capacitive BCC using surface wave propagation as the dominant mechanism.

Hence, this thesis work proposed the first design of a transmitter for capacitive BCC with surface wave propagation in the 400−500 MHz band. The proposed transmitter is based on UWB principles as they have already shown excellent energy-efficiency thanks to their ability to be

highly duty-cycled. First, a system study was presented with the trade-off between maximum achievable data rate and bandwidth for a pulse-based communication. The system specifications have also been presented for the transmitter and the receiver according to the channel model at 450 MHz [2]. According to these system specifications, a design of a fully-digital, pulse-based transmitter with OOK modulation has been presented. The transmitter is based on an unlocked oscillator with immediate start-up for aggressive data duty-cycling. The oscillator is based on a pseudo-differential ring oscillator running at 90 MHz. The pseudo-differential ring oscillator allows for ultra-low power consumption and sharp edges. The low frequency is then multiplied by 5 through edge-combiners that are embedded in a switched-capacitor power amplifier. Furthermore, a digital pulse shaping feature is included to reduce out-of-of-band interferences and for spectral efficiency. Thanks to the 28 nm FD-SOI technology, the efficiency of the power amplifier is improved. The body-biasing feature of the FD-SOI technology allows for ON-resistance reduction, which is the main sources of loss in switched-capacitor circuits. By using body-biasing on the output switches, the power amplifier can be designed with smaller switches, reducing the parasitic capacitance and hence reducing the dynamic power losses. This principle has been presented with a simulation-validated model of the impact of forward body-biasing on switched-capacitor power amplifiers. And provides a design methodology for the design of switched-capacitor power amplifiers in FD-SOI technology. It has been demonstrated that forward body-biasing allows for area reduction, system efficiency improvement and linearity improvement. This has been published in the IEEE TCAS-II journal [3].

The measurements of the transmitter demonstrated that it consumes 17 to 116 μW for flexible data rates from 0.1 to 45 Mb/s (170 pJ/b down to 2.58 pJ/b) with up to 18 % system efficiency under 0.5 V supply voltage. An on-body demonstration has also been performed. By using a wideband low-noise amplifier as a receiver, the received signal was able to be processed and demodulated. It was demonstrated for a distance up to 50 cm line of sight on the arm and up to 30 cm for a non line of sight communication with a pectoral to shoulder blade link. The proposed transmitter is the first transmitter employing surface wave propagation for capacitive BCC , and its performances are at par or better than the state of the art. The transmitter design along with measurement results and demonstration have been presented during the IEEE RFIC 2021 conference [4], with an extended paper published in the IEEE Journal of Solid State Circuits of May 2022 [5].

Finally, following the results of the transmitter, some design considerations have been presented for the receiver. The passive mixer-first architecture has been defined as worth studying. Furthermore, as a passive mixer is a switched-capacitor circuit, the body-biasing principle used for the power amplifier could be reused for power consumption reduction of the receiver.

7.2 Future Work

In this section, we describe the future work needed to improve the presented work and push further the development of the Human Intranet network.

To improve the proposed solution, some functionality should be included on-chip to achieve a complete SoC solution. First, the frequency calibration of the oscillator is made externally as of now. For a complete solution, periodic calibration should be included on-chip to fully compensate PVT variations. As we want to avoid bulky crystal references, an on-chip frequency reference should be designed with a calibration loop that could tune the oscillator's frequency periodically. Secondly, a body-bias generator should be designed to generate the required body-bias voltages on-chip such as in [6, 7]. This will allow the on-chip calibration of the oscillator and the power amplifier. Furthermore, it could also allow for body-bias duty-cycling, reducing the static power consumption of the transmitter. Thirdly, power management should also be included on-chip such as a DC-DC converter similarly as in [6]. Last but not the least, more work is needed on the design of efficient electrodes with impedance matching, which is challenging. For the design of electrodes, flexible and fabric electronics are fields of research gaining attention for comfortable wearability [8].

As described in Chapter 6, the receiver needs to be designed to realise a full communication link on the human body. The Uncertain-IF architecture with passive mixer first has been identified as an option worthwhile to be studied. It has been identified that body-biasing could enable low power consumption in passive mixers. The analysis of body-biased passive mixers should be push further to fully understand its impact on the gain and noise performances. Other blocks in the receiver should also be studied and designed, such as IF-amplifiers.

Finally, the ultimate goal is to include the previous work that has been realised in the upper layers. Previous work [9], has proposed a heartbeat-based synchronisation as an alternative to duty-cycling and wake-up radios. Hence, a heartbeat detector should be designed and integrated to the designed transceiver for node synchronisation. Furthermore, a MAC protocol [10], based on the heartbeat synchronisation, has been proposed. Hence, after the design of the receiver, the heartbeat detector, and the electrodes, a complete demonstration of the Human Intranet network could be performed with several wearable nodes on the human body.

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Annexe A

Acronymes

2-PPM 2-Path Passive Mixer. 88–90

ADFLL All Digital Frequency Locked Loop. 24

ADPLL All-Digital PLL. 16

AI Artificial Intelligence. 2

BAN Body Area Network. 2, 18, 65

BCC Body-Coupled Communication. 22–24, 26, 27, 31, 32, 96, 97

BER Bit Error Rate. 26

BLE Bluetooth Low-Energy. 16, 17, 20, 30, 31

BMI Brain-Machine Interface. 2, 7

BPSK Binary Phase Shift Keying. 18, 19, 28, 38, 50, 52

BW Bandwidth. 38

c-BCC Capacitive Body-Coupled Communication. 22, 38, 40, 44, 63, 66

CGM Continuous Glucose Monitoring. 2

CMOS Complementary Metal-Oxide-Semiconductor. 8–10, 41, 48, 49, 74

CSMA Carrier-Sense Multiple Access. 6

DAC Digital to Analog Converter. 18, 20, 82

DE Drain Efficiency. 74, 78, 79

DIBL Drain-Induced Barrier Lowering. 77

DNL Differential Non-Linearity. 81, 82

EC Edge-Combiner. 50, 54, 56

ECG Electrocardiography. 2, 4, 7

EC-SCPA Edge-Combiner Switched-Capacitor Power Amplifier. 50, 57, 59, 68

ED Envelope/Energy Detection. 86, 87

EMF Electric and Magnetic Fields. 43

EMG Electromyography. 2, 7

EQS Electro Quasi-Static. 28, 31, 40, 66

FBB Forward Body Biasing. 18, 19, 48, 56, 59, 74, 75, 79, 80, 82, 89

FCC Federal Communication Commission. 20, 21, 40, 44

FD-SOI Fully Depleted Silicon On Insulator. 8–11, 18, 48, 49, 51, 53, 68, 75, 76, 78, 80, 82, 91, 97

g-BCC Galvanic Body-Coupled Communication. 22, 24

INL Integral Non-Linearity. 81, 82

IoT Internet of Things. 2, 16

ISM Industrial, Scientific and Medical. 17, 21, 86

LNA Low Noise Amplifier. 4, 25, 29, 86

LO Local Oscillator. 74, 87–91

LTI Linear Time Invariant. 88

LVT Low Voltage Threshold. 48, 75, 76

MAC Media Access Control. 2, 6

m-BCC Magnetic Body-Coupled Communication. 22, 23, 66

MICS Medical Implantable Communication System. 86

NF Noise Figure. 86, 89, 90

OOK On Off Keying. 18, 23, 29, 38, 50, 52, 61, 86, 88, 97

PA Power Amplifier. 4, 5, 16, 18, 20, 53, 78

PBO Power Back-Off. 76, 79

PCB Printed Circuit Board. 58, 63

PDR Packet Delivery Ratio. 6

PD-RO Pseudo-Differential Ring Oscillator. 50, 52–54, 57–59, 61, 68

PLL Phase-Locked Loop. 4, 5, 16, 18, 29, 86, 87, I

PPM Pulse Position Modulation. 18

PRF Pulse Repetition Frequency. 38

PVT Process Voltage Temperature. 18, 51, 58, 59, 80, 98

RF Radio-Frequency. 4–6, 10, 31, 82, 96

RO Ring-Oscillator. 19, 20, 51, 87

RSSI Received Signal Strength Indicator. 28

RVT Regular Voltage Threshold. 48

RX Receiver. 22, 24, 26, 27, 63, 87

SAR Specific energy Absorption Rate. 44

SCPA Switched-Capacitor Power Amplifier. 50, 53, 54, 56, 58, 74, 76, 77, 79, 81, 82, 89

SE System Efficiency. 77–79, 82

SoC System-on-Chip. 19, 20, 48, 68, 98

SW Surface Wave. 40, 63, 66

TDMA Time Division Multiple Access. 6

TX Transmitter. 16, 19, 22, 24, 26, 27, 31, 38, 50, 58, 59, 64–66, 68

ULV Ultra-Low Voltage. 82

UWB Ultra-Wide Band. 18, 20, 21, 30, 31, 38, 40, 65, 91, 96

VGA Variable Gain Amplifier. 24, 25

VNA Vectorial Network Analyzer. 27

Wu-RX Wake-Up Receiver. 87