



HAL
open science

Design and implementation of high efficiency power amplifiers for 5G Applications

Joe Bachi

► **To cite this version:**

Joe Bachi. Design and implementation of high efficiency power amplifiers for 5G Applications. Micro and nanotechnologies/Microelectronics. Institut Polytechnique de Paris, 2022. English. NNT : 2022IPPAT039 . tel-03911284

HAL Id: tel-03911284

<https://theses.hal.science/tel-03911284v1>

Submitted on 22 Dec 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Design and Implementation of High Efficiency Power Amplifiers for 5G Applications

Thèse de doctorat de l'Institut Polytechnique de Paris
préparée à Télécom Paris

École doctorale n°626 École Doctorale de l'Institut Polytechnique de Paris (ED IPP)
Spécialité de doctorat : Electronique et Optoélectronique

Thèse présentée et soutenue à Palaiseau, le 28/11/2022, par

Joe BACHI

Composition du Jury :

Sylvain BOURDEL <i>Professeur, Grenoble INP</i>	<i>Président</i>
Nathalie DELTIMPLE <i>Professeure, Bordeaux INP</i>	<i>Rapporteur</i>
Alain PEDEN <i>Professeur, IMT Atlantique</i>	<i>Rapporteur</i>
Jean-Christophe COUSIN <i>Maître de Conférences, Télécom Paris</i>	<i>Examineur</i>
Patricia DESGREYS <i>Professeure, Télécom Paris</i>	<i>Directrice de thèse</i>
Alexandre GIRY <i>Docteur, CEA-LETI</i>	<i>Co-Encadrant</i>
Ayssar SERHAN <i>Docteur, CEA-LETI</i>	<i>Invité</i>
Dang-Kiên Germain PHAM <i>Maître de Conférences, Télécom Paris</i>	<i>Invité</i>

To my parents, Emile & Najah

Acknowledgments

After four years of hard work, I am happy to have produced this manuscript. This however would not have been possible without the support, guidance, and assistance that were provided to me by a lot of different people both in professional and personal circles. It really does take a village!

First and foremost, I would like to thank my advisors starting with my thesis director Pr. Patricia Desgreys whose comments and insight proved invaluable to producing a scientific document of this scale. I am also grateful to my advisor Dr. Alexandre Giry for always encouraging me to aim higher and believing in my potential. A special thanks to Dr. Germain Pham whose methodical and rigorous scientific approach was only surpassed by his caring and aimable nature. Finally, words fail to do justice to the recognition deserved by Dr. Ayssar Serhan who never skipped an opportunity to provide his full support and commitment to this project.

I would also like to thank Pr. Sylvain Bourdel, Pr. Nathalie Deltimple, Pr. Alain Peden, and Dr. Jean-Christophe Cousin for accepting to be part of the jury and taking the time to review my work.

Thank you to the members of the LAIR laboratory at CEA-Leti for making me feel welcomed during my three-year stay, with a special mention to Dr. Dominique Morche who was always available to help out the PhD students. I am especially grateful to the members of the PA/FEM team Dr. Pascal Reynier and M. Damien Parat for their continuous support and assistance.

During this PhD, I was able to meet other aspiring PhD students, interns, and researchers, who became some of my closest friends. Etienne, Mathilde, Abdess, Saad, Jorge, Ghita, Naci, Aicha, Lucien, Nouheila, Léa, and Mohammed, thank you all for your friendship, support, and all the fun activities, coffee, and drinks, I wish you all good luck on your respective journeys.

None of this would have been possible without the love, support, and sage advice of parents, Emile and Najah, and my amazing sisters Jessy and Christelle. I am blessed to have had you all by my side.

Last but certainly not least, I would like to thank my best friend, fiancé, and future wife, Julia for being my constant support system and helping me get through the low phases.

Table of Contents

Acknowledgments	i
Table of Contents	ii
List of Figures	v
List of Tables	xii
Glossary of Abbreviations	xiii
Chapter 1. Introduction.....	1
1 Evolution of Mobile Communication Standards	3
2 5G System Specifications	4
3 RF Front-End Architectures.....	6
4 Thesis Objectives	8
Chapter 2. Power Amplifier Basics	11
1 RF Power Amplifiers	13
1.1 Output Power.....	13
1.2 Efficiency	14
1.3 Gain	14
1.4 Linearity	15
1.5 Bandwidth	17
2 PA Operation	18
2.1 Linear Class PAs	20
2.2 Class-E PA	24
2.3 Back-Off Operation.....	27
3 Load Modulated PA Architectures	30
3.1 Outphasing PA Architecture	32
3.2 Doherty PA Architecture.....	35
4 Conclusion	39
Chapter 3. Load Modulated Power Amplifier Combiner Design	41
1 Outphasing PA Combiners	43
1.1 Reactive Compensation.....	45
1.2 Delay-Line Compensation.....	47
1.3 Driving Mode	48
1.4 Outphasing Combiner Analysis.....	49
1.4.1 Unified Outphasing Combiner Design Methodology	54
2 Doherty PA Combiners.....	57
2.1 DPA Combiner Analysis	58
2.1.1 Reactive Compensation Current Combiner for DPA Operation.....	61
3 Conclusion	66

Chapter 4.	SOI-CMOS Class-E Doherty PA	67
1	Doherty PA Design	69
1.1	Power Stage Design	70
1.1.1	Impedance Matching	72
1.1.2	PA Stability	74
1.2	Driver Stage Design	76
1.3	Inter-Stage Matching Network Design	77
1.4	Two-Stage DPA Line-Up and Simulation	78
2	Integration Technology	83
2.1	SOI-CMOS Technology	83
2.1.1	Inductors	84
2.1.2	Capacitors	85
2.1.3	Power Device	87
2.2	Package Substrate Technology	88
2.3	PCB Technology	90
3	Circuit Implementation and Measurement	91
3.1	Layout	91
3.2	Validation	94
3.3	CW and LTE Performance	96
4	Conclusion	99
Chapter 5.	Towards an Outphasing PA Transmitter System	101
1	Outphasing PA Design	103
1.1	Class-B OPA	103
1.1.1	Outphasing Angle Boundary Condition	104
1.2	Class-E OPA	106
1.2.1	Offset Transmission Lines	107
1.2.2	Load-Pull Contours Rotation	108
2	DPD System Level Analysis	112
2.1	Look-Up Table Approach	112
2.2	Modelling-Based Approaches	114
2.2.1	In-SCS DPD Architecture	115
3	PA Modelling	117
4	Conclusion	119
	Conclusion & Future Work	121
	List of Publications	123
	References	124

List of Appendices	131
Appendix A. Active Device Modelling	132
Appendix B. Two-Port Networks	134
B.1. Transmission Lines	135
B.1.1. Quarter-Wave Transmission Line.....	135
B.1.2. Half-Wave Transmission Line	136
B.1.3. Cascading Transmission Lines	136
B.1.4. Lumped Element Equivalent Model	137
B.1.5. Differential to Single-Ended Transformation	137
B.2. Dual Networks	138
B.2.1. Note on the direction of active sources in dual networks	139
Appendix C. Complex Load OPA Combiner Design	140
C.1. OTL-Based OEPA Design.....	140
C.2. Generalized Solution.....	144
Résumé de la Thèse	147

List of Figures

Figure 1.1 – Power envelope snippet in the time domain showing the peak and average power levels.....	5
Figure 1.2 – (a) Simulated PDF of different mobile communication standards. (b) CCDF of different carrier waveforms plotted against PAPR [9].	5
Figure 1.3 – Simplified RF FEM block diagram.....	6
Figure 1.4 – 4G/5G RF front-end for smartphones [13].	7
Figure 2.1 – Generic power amplifier schematic with power and impedance representation..	13
Figure 2.2 – Gain compression showing the 1dB power level and the saturation power.	14
Figure 2.3 – Example of a simulated PA’s (a) AMAM and (b) AMPM response with respect to output power.....	15
Figure 2.4 – Two-tone PA test showing power spectrum of the input signal and output signal with the fundamental, harmonics, third order (IMD3) and second order (IMD2) intermodulation components.....	16
Figure 2.5 – (a) PA output spectrum showing Main channel and high, low adjacent channels, (b) IQ plot showing original and emitted symbols with error vector.....	16
Figure 2.6 – Measured PAE and Psat over frequency [14].	17
Figure 2.7 – Generic power amplifier schematic.	18
Figure 2.8 – (a) DC sweep transistor schematic. (b) Normalized Id-Vg characteristic representing drain current vs gate voltage. (c) Normalized Id-Vd characteristic representing drain current vs drain voltage for different gate voltages with knee region.....	18
Figure 2.9 – (a) Ideal large-signal transistor model (b) Large-signal transistor model with linear parasitic elements.	19
Figure 2.10 – (a) Linear-class PA schematic. (b) Transistor characteristic with the bias voltage point for different classes.	20
Figure 2.11 – Examples of Class-A (red) and Class-B (blue). $V_T = 0$ for simplicity.....	20
Figure 2.12 – Drain current (a) harmonics amplitude and (b) harmonic ratio for different conduction angle values.	22
Figure 2.13 – (a)PA drain efficiency and (b) power gain for different conduction angles.	23
Figure 2.14 – (a) Ideal class-E PA with shunt capacitance. (b) Square-wave input voltage V_{in}	24
Figure 2.15 – (a) Drain Voltage-Current phase difference at different harmonics (b) Drain voltage and current time domain waveforms.	25
Figure 2.16 – (a) Class-E PA drain efficiency and output power as a function of duty cycle (b) Single-tone sinewave driven Class-E PA drain efficiency and output power as a function of input voltage amplitude.	27
Figure 2.17 – (a)Probability distribution functions of different communication standards versus back-off power level. (b)Class-A PA load-line for different RF power levels showing drain voltage and current waveforms.	27

Figure 2.18 – (a) PA drain efficiency and (b) power gain versus normalized output power for class-A, class-AB, and class-B PA simulations. 28

Figure 2.19 – Class-E PA simulation results showing (a) drain efficiency and (b) normalized power gain versus normalized output power. 29

Figure 2.20 – Supply modulation on a class-A PA. 29

Figure 2.21 – Load modulation on class-A PA loadlines and drain I-V curves. 30

Figure 2.22 – Class-E PA with varying load Z_L for load-pull simulation. 31

Figure 2.23 – Smith Charts normalized to R with optimal performance load line in black showing: (a) Output power contours (b) Drain efficiency contours. For impedance values located on the optimal performance load line: (c) Drain efficiency versus output power, (d) Drain voltage and current amplitudes. 31

Figure 2.24 – (a) Outphasing PA block diagram, (b) Complex-plane, input signal decomposition 32

Figure 2.25 – (a) Isolating Wilkinson combiner based OPA and (b) its associated efficiency profile with respect to back-off output power level. (c) Classic Chireix non-isolating combiner based OPA with (d) possible efficiency profiles that can be achieved depending on the combiner design values. 33

Figure 2.26 – OPA Chireix combiner simulation showing normalized PA load (a) conductance and (b) susceptance versus output power. 34

Figure 2.27 – Classic DPA power stage and output combiner schematic. 35

Figure 2.28 – Normalized Main and Auxiliary (a) current (b) voltage (c) parallel load resistance versus linear output power. (d) Normalized DPA efficiency versus normalized output back-off in dB. The dashed line marks the BO critical operation point separating low power and Doherty regions. 36

Figure 2.29 – Examples of published DPA designs using (a) LCL combiner [43] and (b) LC combiner [42]. 37

Figure 3.1 – Differential Outphasing voltage combiner. 43

Figure 3.2 – (a) Normalized load conductance, (b) Normalized load susceptance. 44

Figure 3.3 – (a) Normalized efficiency, (b) OPA efficiency and load susceptance with respect to normalized output power (OBO). 45

Figure 3.4 – (a) Differential voltage combiner with reactive compensation, (b) Load susceptance versus Outphasing angle for different compensation angle values. 45

Figure 3.5 – (a) Efficiency with respect to Outphasing angle, (b) Efficiency with respect to output power back-off (OBO). 46

Figure 3.6 – Single-ended (a) voltage combiner, (b) current combiner with reactive compensation. 46

Figure 3.7 – (a) Differential voltage combiner, (b) Single-ended voltage combiner with delay-line compensation. 47

Figure 3.8 – (a) Single-ended (a) current combiner with delay-line compensation, (b) current combiner with simplified lumped equivalent of delay-line compensation. 47

Figure 3.9 – (a) Voltage combiner and (b) Current combiner with reactive compensation, (c) Voltage combiner and (d) Current combiner with delay-line compensation. Without negative signs at sources.	48
Figure 3.10 – Cascaded two-port representation of the RCC combiner and its equivalent simplified form to be used for analysis.	49
Figure 3.11 – (a) Normalized Conductance and (b) Susceptance. (c) Normalized load admittance trajectories. (d) Efficiency with respect to output power for different values of θc	51
Figure 3.12 – (a) Input current amplitude evolution with respect to θ for different values of θc , (b) Normalized input impedances, (c) Normalized load conductance, (d) Efficiency with respect to output power.....	52
Figure 3.13 – (a) Maximum Outphasing angle θ_{stop} with respect to compensation angle variation. (b) Efficiency with respect to output power.....	53
Figure 3.14 – (a) Reactive compensation voltage combiner (RCV) (b) Reactive compensation current combiner (RCC) (c) Delay-line compensation voltage combiner (DCV) (d) Delay-line compensation current combiner (DCC).....	54
Figure 3.15 – (a) Normalized load conductance and (b) Efficiency with respect to output power for different targeted OBO in voltage-mode operation.	56
Figure 3.16 – (a) Normalized current amplitude and (b) load conductance for different values of OBO in current-mode operation.....	56
Figure 3.17 – Simplified current-mode representation of the DPA architecture.	57
Figure 3.18 – (a) Lossy two-port representation of the black-box method, (b) Lossless three-port representation of the black-box method.....	57
Figure 3.19 – Cascaded two-port network representation of the reactive compensation current combiner for DPA operation.	58
Figure 3.20 – Cascaded two-port network representation of the reactive compensation current combiner for DPA operation.	61
Figure 3.21 – Maximum theoretical back-off value ζ_{max} with respect to ϕ	63
Figure 3.22 – Main and auxiliary normalized (a) current amplitude, (b) voltage amplitude, (c) parallel load resistance, and (d) impedance for different values of ϕ at $\zeta = 5dB$	64
Figure 3.23 – DPA combiner efficiency versus normalized output power for (a) different values of ϕ at $\zeta = 5dB$ and (b) different levels of ζ at $\phi = -90^\circ$	65
Figure 4.1 – Two-stage DPA block diagram.....	69
Figure 4.2 – (a) Reactive compensation current combiner, (b) Class-E power cell schematic.	70
Figure 4.3 – Schematic of the class-E DPA power stage with combiner.....	71
Figure 4.4 – 1dB step power contours and 5% step efficiency contours with load modulation trajectory seen at (a) main branch at peak, (b) main branch at back-off, (c) auxiliary branch at peak. (d) DPA stage efficiency and gain versus output power.....	71
Figure 4.5 – Comparison of DPA (a) gain and (b) efficiency versus output power in the case of linear and efficient operation modes.	72

Figure 4.6 – (a) Low Pass-High Pass (LPHP) matching network, (b) High Pass-Low Pass (HPLP) matching network, (c) Low Pass-Low Pass (LPLP) matching network, (d) High Pass-High Pass (HPHP) matching network..... 73

Figure 4.7 – (a) PAE and (b) Power gain performance versus output power for different IMN architectures. 73

Figure 4.8 – (a) Dual-input DPA reflection coefficients, (b) Input and output impedance extraction..... 74

Figure 4.9 – Real part of the input and output impedances of (a) Main and (b) Auxiliary branch PAs..... 75

Figure 4.10 – (a) Real part of the input and output impedances of the auxiliary branch PA after tuning. (b) Simulated DPA efficiency and gain versus output power achieved after tuning... 75

Figure 4.11 – Single-stage dual-input DPA schematic with input and output matching networks. 76

Figure 4.12 – (a) Cascode topology schematic and (b) Driver stage equivalent model. 76

Figure 4.13 – ISMN sub-circuit components..... 77

Figure 4.14 – (a) Conventional lumped-element Wilkinson divider, (b) Modified Wilkinson lumped-element divider 78

Figure 4.15 – Tuned single-input two-stage DPA schematic. 78

Figure 4.16 – (a) Reflection coefficients, (b) Transmission coefficient. 79

Figure 4.17 – (a) Driver stage performance, (b) Main and auxiliary branch performance..... 79

Figure 4.18 – (a) Real power stage load modulation, (b) driver stage load modulation..... 80

Figure 4.19 – (a) Simulated power stage PAE and gain versus output power. (b) power stage AMAM and AMPM distortions. 80

Figure 4.20 – (a) Power and driver stage AMAM distortion, (b) Two-stage DPA AMAM and AMPM distortion. 80

Figure 4.21 – (a) Two-stage DPA line-up performance, (b) Insertion loss of the matching stages. 81

Figure 4.22 – Simulated (a) PAE and (b) gain profiles at different frequencies. 81

Figure 4.23 – Simulated (a) Peak and 6dB Back-Off PAE and (b) Output power and gain with respect to operating frequency. 82

Figure 4.24 – Assembly technology stack-up..... 83

Figure 4.25 – RF-SOI technology M4TCTA stack showing metals on the left and vias on the right. 83

Figure 4.26 – Custom inductor with (a) High quality factor, (b) High compacity. 84

Figure 4.27 – Custom inductor with (a) High quality factor, (b) High inductance in a compact size. 84

Figure 4.28 – EM simulation results of the series auxiliary inductor $Ls|Aux$ and the LC tank bias inductor $LBias$ showing (a) inductance value and (b) quality factor with respect to frequency..... 85

Figure 4.29 – 3D representation of (a) 3 metal layers MOM capacitor, (b) MIM capacitor. .. 85

Figure 4.30 – Quality factor at 2.5GHz and self-resonance frequency simulated for 1pF using DK (a) MOM capacitor model, (b) MIM capacitor model.	86
Figure 4.31 – (a) 2D layout view of the elementary MIM capacitor cell with top and bottom pins on the metal4u layer, (b) 3D view of the access structure with the external top and bottom pins marked in purple, and the internal connection pins to the unitary capacitor cells marked in orange.	87
Figure 4.32 – (a) Capacitance and (b) Q-factor of the equivalent capacitor using 4 parallel capacitors with the DK model only (red) and EM model of the access+capacitor DK model (blue).....	87
Figure 4.33 – (a)2D layout view of the 8mm LDMOS PA cell, (b) 3D layout of the power stage with copper pillars.	88
Figure 4.34 – μ PCB laminate stack showing metals on the left and vias on the right.	88
Figure 4.35 – (a) 3D view of the supply inductor layout, (b) Inductance and Q-factor of the EM model.	89
Figure 4.36 – (a) 3D view of the CPWG line implemented on Cu1 layer with a ground plane on Cu2, (b) S-parameters of the EM model.	89
Figure 4.37 – PCB technology stack showing metals on the left and vias on the right.	90
Figure 4.38 – Tuned single-input two-stage DPA schematic.....	91
Figure 4.39 – RFpro 3D view of the integrated IC inductors.....	91
Figure 4.40 – (a) 2D layout view of the IC chip with black boxes outlining the main, auxiliary, and driver cells. (b) 2D layout view of the μ PCB package.	92
Figure 4.41 – 3D RFpro view of the full-stack for EM simulation.	92
Figure 4.42 – IC die and laminate package photograph.	93
Figure 4.43 – (a) Fabricated PCB with mounted IC and package (b) PCB access lines test structure.	93
Figure 4.44 – Measurement and model comparison of (a) S11 magnitude, (b) S11 phase, (c) S21 magnitude, (d) S21 phase.	94
Figure 4.45 – PA measurement setup.....	94
Figure 4.46 – (a) Driver and (b)Power stage DC drain current comparison between measurements and EM model.	95
Figure 4.47 – (a) PAE, DE and (b) power gain comparison between measurements and simulation.	95
Figure 4.48 – (a) Reflection and (b) transmission coefficient comparison between measurements and simulation.....	96
Figure 4.49 – (a) PAE and gain profiles at different operating frequencies. (b) Extracted power, efficiency and gain at different operating frequencies in CW mode.....	96
Figure 4.50 – (a) PAE and E-UTRA ACLR versus P_{out} measured at 2.3GHz using 10MHz LTE QPSK 50RB uplink signal with memoryless DPD and (b) Output Spectrum.	97
Figure 4.51 – (a) AMAM and AMPM and (b) output constellation measured at 2.3GHz using 10MHz LTE QPSK 50RB uplink signal.	97

Figure 4.52 – (a) Measured PAE and G_p versus P_{out} and (b) PAE and P_{out} extracted for ACLR=-35dBc at different frequencies using 10MHz LTE QPSK 50RB uplink signal. 98

Figure 5.1 – Generic OPA block schematic showing its three main components. 103

Figure 5.2 – (a) Ideal transistor model (b) Simplified OBPA with reactive compensation voltage combiner..... 103

Figure 5.3 – (a) Complex plane representation of normalized drain and gate voltages (b) Normalized admittance magnitude for different compensation angle values..... 104

Figure 5.4 – (a) Output power and (b) efficiency evolution for ideal voltage-mode (dashed black) and the proposed OBPA design (red). 106

Figure 5.5 – Ideal switch-based $q=1$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with classic Outphasing load modulation schemes overlaid in black. 107

Figure 5.6 – Two-port representation of the Outphasing combiner with offset transmission lines. 107

Figure 5.7 – Ideal switch-based $q=1$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with rotated OTL Outphasing load modulation schemes overlaid in black. 107

Figure 5.8 – Ideal switch-based $q=1.3$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with classic Outphasing load modulation schemes overlaid in black. 108

Figure 5.9 – (a) Reactive compensation combiner schematic, (b) Class-E power cell schematic with red arrow marking complex load modulation plane. 109

Figure 5.10 – Load-pull contours at $P_{avs}|dBm = 23.5dBm$ (a) Power contours, (b) PAE contours..... 109

Figure 5.11 – Load-pull contours at $P_{avs}|dBm = 13dBm$ (a) Power contours, (b) PAE contours..... 110

Figure 5.12 – Dual input OEPA schematic..... 110

Figure 5.13 – Possible (a) PAE and (b) power gain performance versus output power for different values of θ in OPA operation for $q = 1.3$. Potentially unstable points are shown in grey..... 111

Figure 5.14 – Conventional (signal) diagram of an OPA. 112

Figure 5.15 – PAE and gain profiles versus output power extracted from the OEPA simulation using (a) maximum PAE criterion, and (b) constant gain value $G_p = 12dB$ criterion..... 113

Figure 5.16 – Signal representation of LUT approach for dual input OPA..... 113

Figure 5.17 – LUT-based DPD integrated in OTX system..... 113

Figure 5.18 – Equivalent baseband signal diagram of the conventional OPA. 114

Figure 5.19 – SISO basedband OPA model representation. 115

Figure 5.20 – SISO basedband DPD model representation. 115

Figure 5.21 – OTX diagram showing how the post-inverse can be used as a pre-inverse. ... 116

Figure 5.22 – Pre-inverse configuration of the In-SCS DPD architecture..... 116

Figure 5.23 – Associated post-inverse configuration of the proposed In-SCS DPD architecture.	116
Figure 5.24 – PA behavioural modelling flow chart.	118
Figure A.1 – Two-port network representation	132
Figure B.1 – Two-port network representation	134
Figure B.2 – (a)Transmission Line representation as a two-port network, (b) Transmission line terminated in a load Z_L	135
Figure B.3 – Transmission Line representation as a two-port network	136
Figure B.4 – (a) Differential power combining topology, (b) Equivalent common-mode power combiner	137
Figure B.5 – (a) Differential power combining topology, (b) Equivalent single-ended power combiner	137
Figure B.6 – Examples of dual circuits with (a) Voltage sources and (b) Current sources ...	139
Figure C.1 – Generic Outphasing load modulation combiner with offset transmission lines	140
Figure C.2 – Ideal switch-based $q=1$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with rotated OTL Outphasing load modulation schemes overlaid in black.	141
Figure C.3 – (a) Effect of ϕ on the direction of the load modulation trajectories (b) Effect of θc on the opening of the load modulation trajectories and the distance between the intersections	142
Figure C.4 – Ideal OTL-based OEPA schematic	143
Figure C.5 – (a) OEPA load modulation trajectories (b) Efficiency versus output power of the OEPA.....	144
Figure C.6 – Output power evolution for ideal voltage-mode (dashed black) and the proposed OBPA design (red)	144
Figure C.7 – Simplified schematic of the generalized combiner design circuit.....	145
Figure C.8 – (a) Complex load modulation trajectories referenced at 50Ω (b) Complex load modulation trajectories referenced at $Z\alpha^*$	145

List of Tables

Table 1.1 – Classification of the different 5G NR frequency bands and their main target application.....	4
Table 2.1 - K-set design equations for $0.6 \leq q \leq 1.65$	25
Table 2.2 – State of the art sub-6 GHz Outphasing PAs.....	34
Table 2.3 – State of the art sub-6 GHz Doherty PAs.....	37
Table 3.1 – Combiner design expressions.	55
Table 4.1 – DPA target performance	69
Table 4.2 – Linear DPA drive profile.	72
Table 4.3 – Modified DPA drive profile.....	75
Table 4.4 – MOM and MIM specs comparison.	85
Table 4.5 – Comparison with the state-of-the-art LTE Doherty PAs.	98
Table B.1 – Common component ABCD matrices.....	134
Table B.2 – Dual networks of elementary components	138
Table C.1 – Combiner Component Design Values for OTL-based combiners	142

Glossary of Abbreviations

1G	First Generation Mobile Communication Standard
2D	Two dimensional
2G	Second Generation Mobile Communication Standard
3D	Three dimensional
3G	Third Generation Mobile Communication Standard
4G	Fourth Generation Mobile Communication Standard
5G	Fifth Generation Mobile Communication Standard
5G NR	5G New Radio
5G NSA	5G Non-Standalone
5G SA	5G Standalone
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADS	Agilent Design System
AMAM	Amplitude Modulation to Amplitude Modulation
AMPM	Amplitude Modulation to Phase Modulation
BEOL	Back End of Line
BO	Back-Off
BPSK	Binary Phase-Shift Keying
BS	Base Station
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CG	Common Gate
CMB	Combiner Stage
CMOS	Complementary MOS
CPWG	Coplanar Waveguide
CS	Common Source
Cu	Copper
CuP	Copper Pillars
CW	Continuous Wave
DC	Direct Current

DCC	Delay-Line Compensation Current (combiner)
DCV	Delay-Line Compensation Voltage (combiner)
DDR	Dynamic Deviation Reduction
DE	Drain Efficiency
DK	Design Kit
DL	Downlink
DPA	Doherty Power Amplifier
DPD	Digital Predistortion
DRV	Driver Stage
EER	Envelope Elimination and Restoration
EM	Electromagnetic
eMBB	Enhanced Mobile Broadband
ET	Envelope Tracking
E-UTRA	Evolved Universal Terrestrial Radio Access
EVM	Error Vector Magnitude
FDMA	Frequency Division Multiple Access
FEM	Front End Module
GaAs	Gallium Arsenide
GMP	Generalized Memory Polynomial
GSM	Global System for Mobile Communications
GPS	Global Positioning System
HCD	Hybrid Chireix-Doherty
HR	Harmonic Ratio
IC	Integrated Circuit
ILA	Indirect Learning Architecture
IMD	Intermodulation product
IMN	Input Matching Network
IoT	Internet of Things
ISMN	Inter-Stage Matching Network
LDMOS	Laterally-Diffused MOS
LINC	Linear Amplification using Non Linear Components
LNA	Low Noise Amplifier

LTE	Long Term Evolution
LTE-A	LTE-Advanced
LUT	Look-Up Table
MIM	Metal-Insulator-Metal
MIMO	Multiple Input Multiple Output
MISO	Multiple Input Single Output
mMIMO	Massive MIMO
mMTC	Massive Machine Type Communication
mmW	Millimetre-Wave
MOM	Metal-Oxyde-Metal
MOS	Metal Oxide Semiconductor
MP	Memory Polynomial
NMOS	N-type MOS
OBPA	Class-B OPA
OBO	Output Back-Off
OEPA	Class-E OPA
OFDMA	Orthogonal Frequency Division Multiple Access
OMN	Output Matching Network
OPA	Outphasing Power Amplifier
OTL	Offset Transmission Line
OTX	Outphasing Transmitter System
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PCB	Printed Circuit Board
PDF	Probability Density Function
POM	Polar Outphasing Modulator
PWR	Power Stage
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase-Shift Keying
RCC	Reactive Compensation Current (combiner)
RCV	Reactive Compensation Voltage (combiner)

RF	Radio Frequency
RX	Receiver
SCS	Signal Component Separator
SiGe	Silicon Germanium
SISO	Single Input Single Output
SMA	Subminiature version A
SMD	Surface Mounted Device
SOI	Silicon on Insulator
SP	Scatter Parameters
SRF	Self-Resonance Frequency
TDMA	Time Division Multiple Access
TX	Transmitter
UMTS	Universal Mobile Telecommunications System
UE	User Equipment
UL	Uplink
uRLLC	Ultra-Reliable and Low Latency Communication
VNA	Vector Network Analyzer
VGA	Variable Gain Amplifier
VoIP	Voice over Internet Protocol
WiFi	Wireless Fidelity
WiMAX	Worldwide Interoperability Microwave Access

Chapter 1. Introduction

1	Evolution of Mobile Communication Standards.....	3
2	5G System Specifications.....	4
3	RF Front-End Architectures	6
4	Thesis Objectives	8

Cellular communications have become an integral part of everyday life. Since the rise of smartphones in 2007, demand for higher data-rates and increased network capacity has exponentially grown which has fuelled the research and development of new communication standards. As of 2018, the groundwork has been laid out for the next step in mobile communication, the 5G standard. However, each new technology brings new challenges. This first chapter outlines the context of 5G development and the requirements it imposes from a circuit design point of view. These criteria are used to define the current needs and subsequently the objectives of the following thesis.

1 Evolution of Mobile Communication Standards

Cellular communications have come a long way since the deployment of the first-generation standards (1G) in 1984. Back then, wireless communication was achieved through analog frequency modulation known as Frequency Division Multiple Access (FDMA). Each user would be allocated a frequency band of 30KHz on a carrier frequency around 500MHz. Moreover, the different existing standards were incompatible [1].

The rise of the number of users quickly led to a saturation of the radio-frequency (RF) spectrum which served as the motivation for creating the second generation of communication standards (2G). This effort was initially led by the Conference of European Post and Telecommunication Administrations (CEPT) which founded the coordinating group Groupe Spécial Mobile (GSM) to oversee European cellular radio development. However, as time went on, GSM's aspirations became much more far-reaching and its acronym now stood for Global System for Mobile Communications. This new standard was the world's first digital cellular system, opening up the possibilities for improvement upon the 1G system. Thanks to its use of digital signals, which can be clearly defined in time, Time Division Multiple Access (TDMA) was made possible. As a result, several channels can be multiplexed onto a single carrier with a bandwidth of 200KHz with the two main frequency bands being 900MHz and 1800MHz [2].

The advent of the 2000s saw the arrival of the third generation (3G) of communication standards which focused on providing internet services such as video streaming and email exchange. This was done through the Universal Mobile Telecommunications System (UMTS) based on Code Division Multiple Access (CDMA) which further improved spectral efficiency. While UMTS was not the standard to bring internet connectivity (that distinction goes to the EDGE standard which can be considered as an evolution of the 2G GSM standard; a 2.5G), it did greatly improve data-rates from 384Kbit/s to 1.92Mbit/s. Furthermore, additional bands were allocated for 3G use in the 900-2600MHz range with channel bandwidths of 3.84MHz [3].

The introduction and rise in popularity of smartphones in the 2010s fuelled the demand for increased data-rates which could accommodate Voice-over Internet Protocol (VoIP) applications such as video-calls and live streaming. The International Telecommunications Union (ITU) therefore set the technical specifications of the next mobile standard evolution, the fourth generation (4G), one of which were data-rates of 100Mbit/s and 1Gbit/s for moving and stationary users respectively as well as channel bandwidths between 5 and 20MHz. Two main standards are considered 4G-compliant: The first is the Worldwide Interoperability for Microwave Access (WiMAX), and the second more popular one is the Long-Term Evolution Advanced (LTE-A). It should be noted that while the precursor to LTE-A, the LTE was commercialized as a 4G service, it did not in fact fulfil the data-rate requirement and as a result cannot be considered a 4G standard. Both WiMAX and LTE-A were based on Orthogonal Frequency Division Multiple Access (OFDMA) air interface which improves on the FDMA by using multiple narrowband sub-carriers which are mutually orthogonal, thereby preventing interference between them [4], [5].

Finally, the fifth generation (5G) evolution of mobile standards has three main objectives: The first is enhanced Mobile Broadband (eMBB) which serves as an extension to 4G services, allowing for higher data-rates (up to 10Gbit/s) and better coverage in urban settings through the use of massive Multiple Input Multiple Output (mMIMO) protocols. The second objective is ultra-Reliable and Low Latency Communication (uRLLC) which allows for the evolution of

certain services such as autonomous self-driving cars and remote surgery where high speed communication is essential. The last objective is massive Machine Type Communication (mMTC) which will provide connectivity between smart objects and sensors; namely the Internet of Things (IoT) [6], [7].

As this work primarily deals with 5G applications, the next section will focus on 5G system specifications.

2 5G System Specifications

The 5G New Radio (5G NR) standard was first introduced in 2018 with the publication of Release 15 by the Third Generation Partnership Project (3GPP). The launch of this new standard would be done in two phases: Phase 1 refers to the deployment of the 5G Non-Standalone (5G NSA) mode which relies on existing LTE infrastructure and is mainly concerned with eMBB applications. As a result, this deployment mode, which began in 2020 uses much of the same frequency bands as LTE referred to as Frequency Range 1 (FR1) which are spread between 450MHz and 6GHz.

Phase 2 will see the deployment of the 5G Standalone (5G SA) mode which cater to eMBB as well as uRLLC and mMTC applications. This second mode will require an update of current cellular infrastructure and extend into millimetre-wave (mmW) frequencies between 24GHz and 52GHz also referred to as FR2 [8].

The different 5G NR frequency bands can therefore be grouped in four main categories as shown in Table 1.1 below.

Table 1.1 – Classification of the different 5G NR frequency bands and their main target application.

5G Band Group	Carrier Frequencies	Current standards	Best suited 5G application
Low Bands	<1GHz	2G/3G/4G/IoT	mMTC, eMBB
Middle Bands	1 – 2.7GHz	2G/3G/4G	eMBB
High Bands	3 – 6GHz	LTE-A	eMBB, uRLLC
Ultra-High Bands	24.25 – 52GHz	-	eMBB, localised uRLLC

The 5G air interface is based on OFDMA variants such as CP-OFDMA and DFT-s-OFDM. This allows the system to allocate time and frequency slots dynamically depending on the needs of each user. To this end, 5G can operate at different channel bandwidth depending on the frequency band in use. Low, middle, and high bands can have a channel bandwidth between 3.84MHz and 100MHz, while the very high bands can go up to 400MHz. Moreover, different modulation schemes can be used to code binary digital data onto the carrier frequency signals; these include phase modulation schemes such as QPSK and $\pi/2$ -BPSK as well as amplitude and phase modulation schemes such as 16, 64, and 256-QAM.

The flexibility provided by the new 5G NR standard comes at the cost of signal complexity. One of the ways of assessing this complexity is by examining the signal's Peak to Average Power Ratio (PAPR) which can be calculated using the equation from (1.1).

$$PAPR = 10 \cdot \log_{10} \left(\frac{P_{peak} |P=0.01\%}{P_{avg}} \right) \quad (1.1)$$

The PAPR is commonly expressed in decibels (dB) and represents the ratio of the peak power, defined as the power level with a probability of 0.01%, and the average signal power. These two power levels are shown in Figure 1.1.

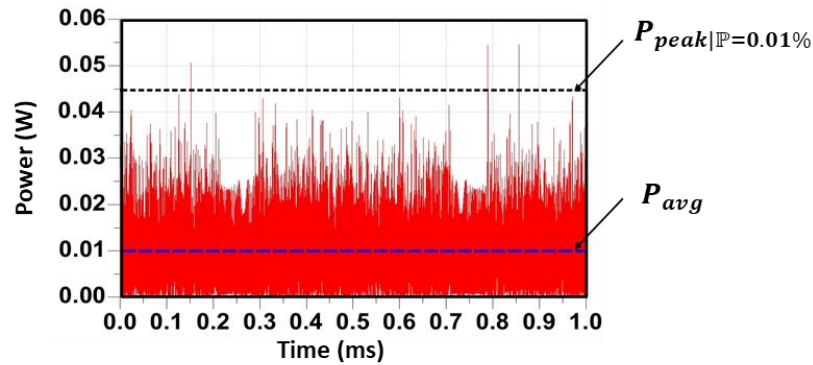


Figure 1.1 – Power envelope snippet in the time domain showing the peak and average power levels.

A more thorough approach for calculating the PAPR is possible when looking at the signals from a statistical perspective.

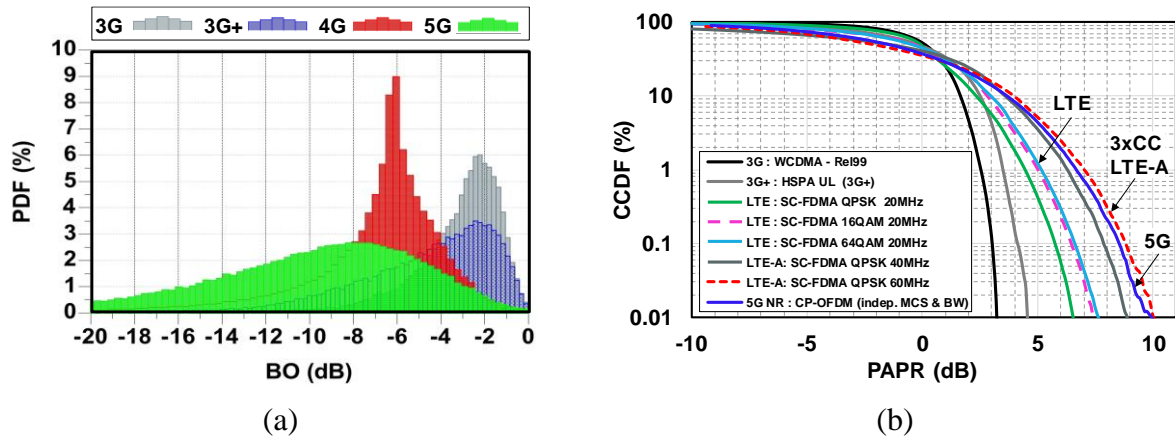


Figure 1.2 – (a) Simulated PDF of different mobile communication standards. (b) CCDF of different carrier waveforms plotted against PAPR [9].

Figure 1.2(a) shows the Probability Density Function (PDF) of different signals with respect to the power back-off level (BO). In other words, it gives the probability of a waveform to have a power value that is x dB lower than the peak power of the signal. As can be seen, the BO level with the highest concentration decreases with every new standard, meaning that the signal will have a lower mean power but require a larger dynamic range in order to reach its peak. The PDF function can be used in order to calculate the Complementary Cumulative Distribution Function (CCDF) as shown in (1.2).

$$CCDF(PAPR) = 1 - \int_{P_{min}}^{PAPR+P_{avg}} PDF(x) dx \quad (1.2)$$

In this form, it is possible to determine the probability of the signal achieving a given PAPR level. The PAPR of the signal is defined as the value for which the CCDF is 0.01%. Figure 1.2(b) plots the CCDF functions of different waveforms and shows once again that the PAPR increases when going from 4G to 5G signals.

3 RF Front-End Architectures

In a typical cellular communication scenario between two mobile terminals, each referred to as User Equipment (UE), are connected via one or more intermediaries known as the Base Stations (BS). Ever since the introduction of 2G, the connection between UE and BS has been dictated by two sub-protocols of the communication standard in use.

The first protocol, Uplink (UL), refers to a communication from the UE to the BS. In 5G NR, this protocol typically uses Cyclic Prefix OFDM (CP-OFDM) and Discrete Fourier Transform spread OFDM (DFT-s-OFDM) air interfaces as well as Single-Carrier FDMA (SC-FDMA) [10]–[12]. The maximum power transmitted by a UE is typically capped at 23dBm.

In the case of BS to UE communication, i.e. Downlink (DL), the CP-OFDMA is used. Depending on the application (rural/urban) different types of coverage cells are used with maximum power levels up to 50dBm.

In both BS and UE terminals, communication is achieved through the RF transceiver which allows for the wireless transmission and reception of modulated signals. Figure 1.3 shows the basic structure of the RF Front-End Module (FEM). In a UL scenario, the MoDem, short for Modulator/Demodulator, encodes binary data into a baseband signal which is then upconverted to RF and fed into the transmitter (TX) chain of the Front-End Module. There, the signal is amplified by the Power Amplifier (PA) before being sent through a filter in order to remove unwanted out-of-band emissions before finally being sent to the antenna. When in DL, the signal is captured by the antenna and filtered before being amplified by the Low Noise Amplifier (LNA) in the receiver (RX) and then downconverted before decoding in the MoDem.

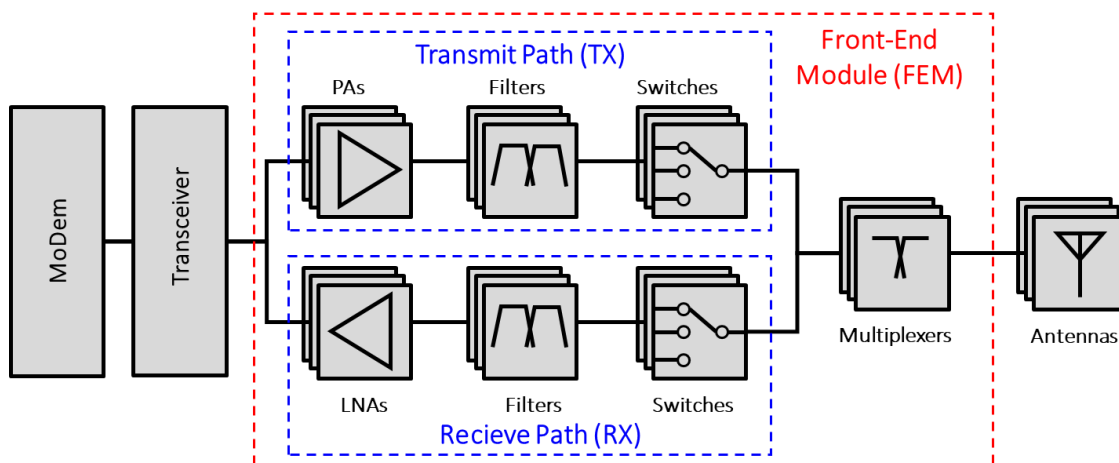


Figure 1.3 – Simplified RF FEM block diagram.

Depending on the operating frequency of the transmitted or received signal, different filters are selected by the switches. Meanwhile the multiplexers act as filters between the different antennas and TX/RX branches.

Over the years, the FEM architecture has become more and more complex in an effort to accommodate different frequency bands and communication standards so as to offer seamless and backwards compatible operation to worldwide users. Today, smartphone FEMs are expected to address 2G, 3G, 4G and 5G standards as well as other standards such as Bluetooth, WiFi, and GPS. An example of a modern FEM architecture taken from [13] is provided in Figure 1.4.

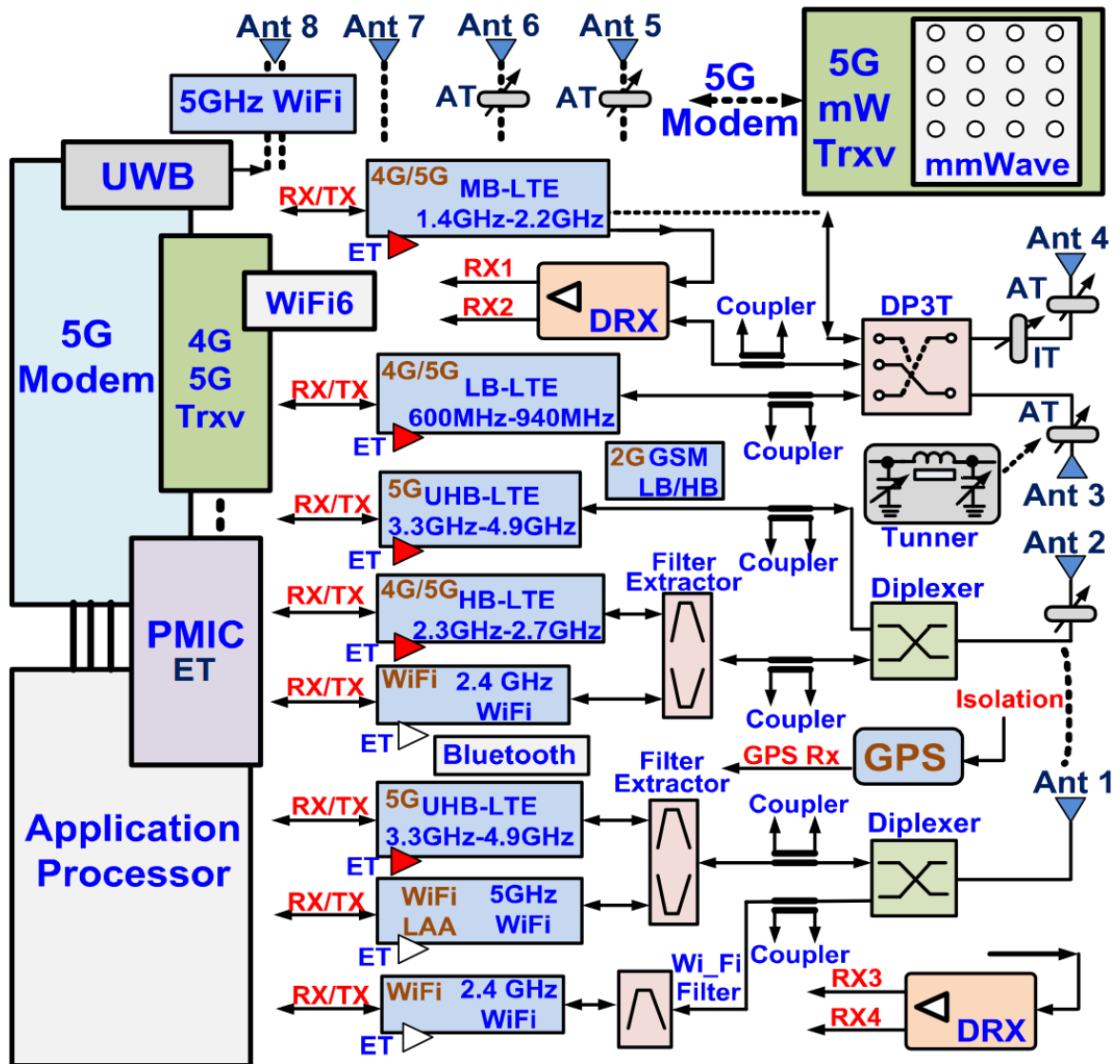


Figure 1.4 – 4G/5G RF front-end for smartphones [13].

Within the different FEM components, the PA can be singled out as the most critical. That is because a PA's power consumption represents more than half of the total FEM consumption. As a result, the efficiency of the PA is directly linked to battery consumption and thermal dissipation in a smartphone. Moreover, the performance of the PA can greatly affect the quality of communication as transmitted signals can become distorted when amplified thus making them unreadable at reception.

4 Thesis Objectives

PA efficiency plays a crucial role since improving it would lead to an increase in battery life and decrease in heat dissipation. Component integration is another vital characteristic. That is because today's phone must be compliant with many different standards and frequency bands, which leads to an increase in the number of required components within the FEM. Integration therefore becomes essential in keeping mobile form factors from becoming too cumbersome. Finally, PAPR is increasing with every new standard, meaning that the next generation of PAs must be able to operate efficiently at high back-off level.

The different components of the FEM are typically implemented using different technologies. While switches are typically made using RF-SOI, most LNA and PA blocs are built using SiGe and GaAs respectively. However, recent years have seen an increase in the use of RF-SOI for LNA and PA implementation. RF-SOI has the potential to address high output power levels (in the range of 30 to 36dBm), while providing high efficiency operation. This technology is therefore chosen for the implementation of the proposed PA architecture thereby opening the door to full FEM integration in the future.

This work will focus on finding an innovative design of high efficiency power amplifiers for 5G applications using combiner analysis and then validate it through circuit implementation and measurement. However, given the wide scope of such a topic, the study will focus on two load modulation PA architectures: Doherty and Outphasing. The PAs are to be used in mobile applications and as a result will be implemented using a 130nm RF-SOI process with a supply voltage of 3.4V. The target operation band is the 5G Mid Band, with a primary focus on bands n40 and n41 of the 5G NR FR1. As a result, the PAs must be designed to operate between 2.3GHz and 2.7GHz. Finally, the PA must be capable of delivering a peak output power of 33dBm and operate at an average efficiency higher than 40% at -35dBc of E-UTRA ACLR.

This PhD work is the result of a joint collaboration between the LAIR and LTCI laboratories of CEA-Leti and Télécom Paris respectively. The following manuscript is organized into five chapters as outlined below:

Chapter 1 presented the context and motivations of the thesis work by recounting evolution of modern mobile communication standards. The new challenges of the 5G standard were explored and their impact on the mobile RF front-end architecture were assessed.

Chapter 2 introduces the basics of PA operation and performance metrics. Classic operation modes are explored before moving on to high efficiency architectures such as load modulation which includes Doherty and Outphasing.

Chapter 3 focuses on load modulated power combiner design. Outphasing combiners are examined first and a new unified analysis and design methodology is presented. Next, an analysis method for Doherty combiners is proposed. The novel analysis provides a way to determine the maximum back-off power level at which Doherty operation can be achieved. Moreover, it gives the current evolution profiles required at the combiner inputs for ideal Doherty operation.

Chapter 4 focuses on the design and implementation of a two-stage Doherty PA. The designed PA is simulated and optimized using load-pull analysis. The different packaging technologies are then showcased before moving on to circuit implementation. Finally, realized DPA circuit

is measured and shown to be capable of similar performance to the current state-of-the-art PAs, thus validating the combiner analysis and design method from the previous chapter.

Chapter 5 explores the Outphasing PA architecture and proposes a design for a class-E OPA. The dual input OEPA is then analysed from a system perspective in an effort to integrate the digital predistortion bloc (DPD) directly into the OPA. A model-based DPD architecture is then formalized. Efforts were also made to create a PA behavioural model to be used in the DPD architecture.

Chapter 2. Power Amplifier Basics

1	RF Power Amplifiers	13
	1.1 Output Power	13
	1.2 Efficiency.....	14
	1.3 Gain	14
	1.4 Linearity.....	15
	1.5 Bandwidth.....	17
2	PA Operation.....	18
	2.1 Linear Class PAs.....	20
	2.2 Class-E PA.....	24
	2.3 Back-Off Operation	27
3	Load Modulated PA Architectures.....	30
	3.1 Outphasing PA Architecture.....	32
	3.2 Doherty PA Architecture	35
4	Conclusion.....	39

Power amplifiers (PA) have the most impact on the mobile front-end module (FEM) since they dissipate the most power and as a result are responsible for most of the heating issues. In order to better understand the challenges and compromises required for PA design, this chapter introduces the main evaluation criteria used to benchmark and compare PA performance.

The basics of PA operation are then explained starting with transistor characterization and sizing. Next, traditional linear classes are analysed, followed by the switch-mode class-E.

Finally, load modulation architectures are introduced as a solution to enhance the PA efficiency at back-off power levels. Outphasing and Doherty PA architectures are briefly discussed and shown to be good candidates for LTE and 5G applications.

1 RF Power Amplifiers

When it comes to RF power amplifiers (PA), there are five main performance indicators:

- Output power
- Efficiency
- Gain
- Linearity
- Bandwidth

The schematic in Figure 2.1 shows a generic, simplified power amplifier circuit.

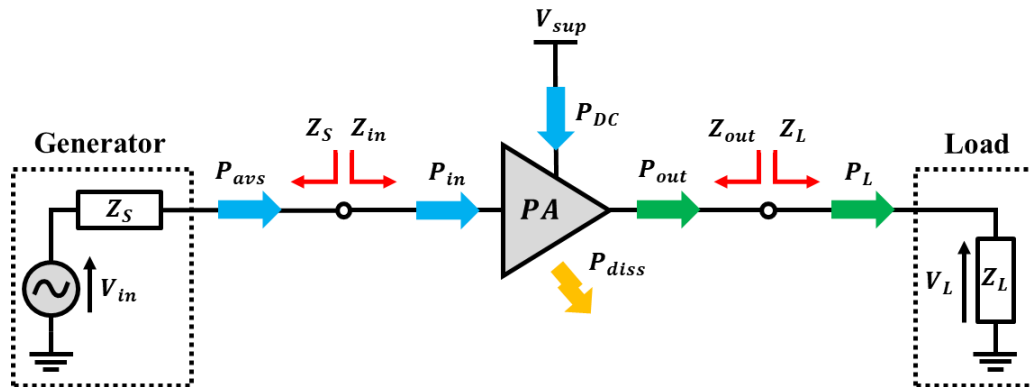


Figure 2.1 – Generic power amplifier schematic with power and impedance representation.

The power provided by the generator is referred to as the available source power P_{avs} . Maximum power transfer refers to the case where all of the available power is delivered to the PA, i.e. $P_{in} = P_{avs}$. This occurs when the impedances Z_S and Z_{in} are conjugately matched ($Z_S = Z_{in}^*$). DC power (P_{DC}) is pulled from the supply voltage source (V_{sup}) and converted into RF output power (P_{out}). A portion of the pulled DC power, is lost through heat dissipation within the PA (P_{diss}).

1.1 Output Power

Maximum power transfer from the PA output to the load is achieved when $Z_L = Z_{out}^*$ leading to $P_{out} = P_L$. The load power P_L can be calculated through:

$$P_L = \frac{1}{2} \cdot |V_L|^2 \cdot \Re \left[\frac{1}{Z_L} \right] \quad (2.1)$$

Using the power conservation principle, the output power can be expressed as:

$$P_{out} = P_{in} + P_{DC} - P_{diss} \quad (2.2)$$

1.2 Efficiency

The efficiency of PA can be assessed using different metrics. The first is the drain efficiency defined as the DC-to-RF conversion ratio between the output power and the DC power. It can be calculated using (2.3).

$$DE = \eta = \frac{P_{out}}{P_{DC}} \quad (2.3)$$

The second efficiency indicator is the power added efficiency (PAE), expressed in (2.4) below.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \quad (2.4)$$

1.3 Gain

PA gain can be calculated in two different ways. The power gain G_p is the ratio between the output and input powers as shown in (2.5).

$$G_p = \frac{P_{out}}{P_{in}} \quad (2.5)$$

Meanwhile, the transducer gain is defined as the ratio between the output power and the available source power:

$$G_t = \frac{P_{out}}{P_{avs}} \quad (2.6)$$

In practical applications, a PA cannot maintain a constant gain (G_p or G_t) across the overall power range due to many different limiting factors. As a result, the PA gain decreases when approaching the saturation output power P_{sat} . The P_{1dB} power level is used to indicate the output power value for which the gain drops by 1dB as can be seen in Figure 2.2. This gain compression, leads to the distortion of the input signal at high power levels thereby affecting the linearity of the PA which is defined and discussed as follows.

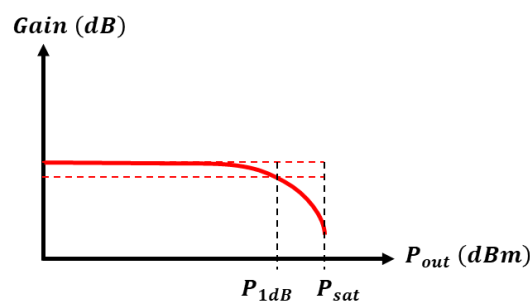


Figure 2.2 – Gain compression showing the 1dB power level and the saturation power.

1.4 Linearity

Linearity allows to quantify the amount of distortion of the amplified output signal with respect to the original input signal. There are many ways to assess to the linearity of a PA, the most practical of which are detailed below.

When a PA approaches saturation, its gain value starts to compress leading to a distortion of the output signal. The signal distortion can be characterized in terms of amplitude distortion (AMAM), which is caused by the nonlinearity of the transistor’s transconductance g_m , as well as phase distortion (AMPM), which is mainly due to the nonlinearity of the transistor’s parasitic capacitors. These effects are shown in the PA simulation results of Figure 2.3. The AMAM distortion represents the gain compression of the PA whereas the AMPM is indicative of the phase deviation at output. These distortions are most impactful at peak power, where the PA is in compression and have very little effect at low power levels.

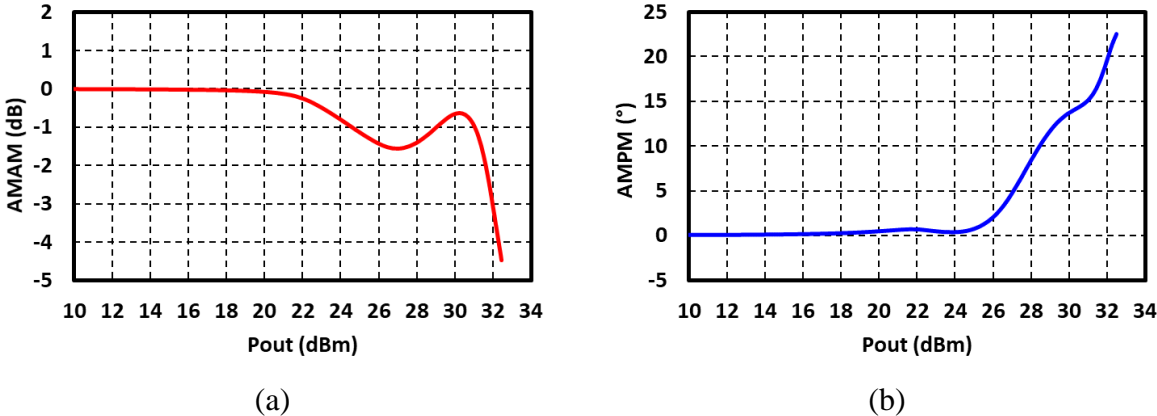


Figure 2.3 – Example of a simulated PA’s (a) AMAM and (b) AMPM response with respect to output power.

Distortion can also be assessed using the dual tone test where a two-tone input signal composed of two carrier frequencies f_1 and f_2 is injected into the PA input. In addition to the original two-tone frequencies, the output signal contains their respective harmonics and intermodulation products as can be seen in Figure 2.4. While all of the aforementioned elements contribute to the effective distortion of the signal, the most significant impact comes from the third and fifth order intermodulation products (IMD3, IMD5) which are very close to the fundamental tones. Higher order odd intermodulation products can also be considered but are generally too low to have a significant effect.

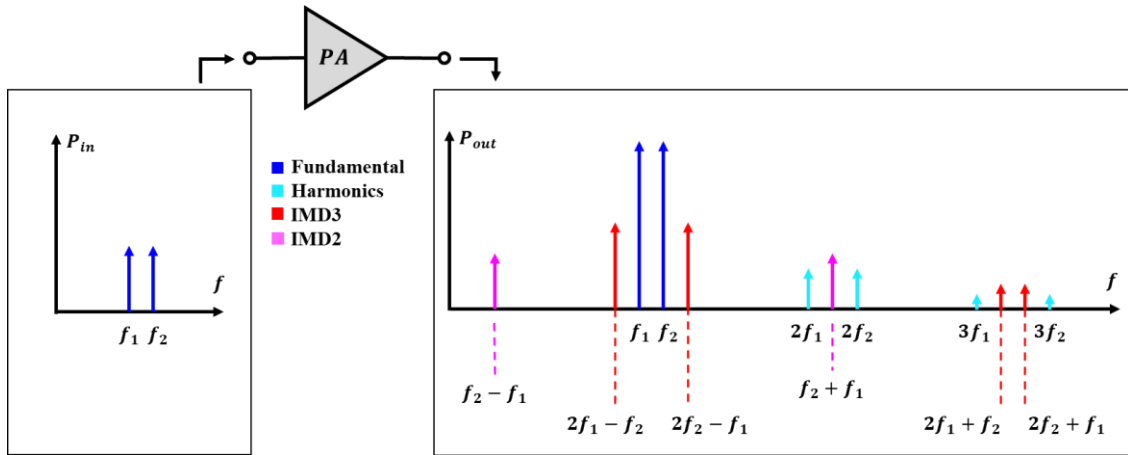


Figure 2.4 – Two-tone PA test showing power spectrum of the input signal and output signal with the fundamental, harmonics, third order (IMD3) and second order (IMD2) intermodulation components.

In the case of complex modulated signals, two metrics are generally used. The first is the adjacent channel leakage or power ratio (ACLR or ACPR) commonly expressed in *dBc*. ACLR is an out-of-band type of distortion, as it represents the amount of power that is leaked from the main channel into the upper and lower adjacent channels as seen in Figure 2.5(a).

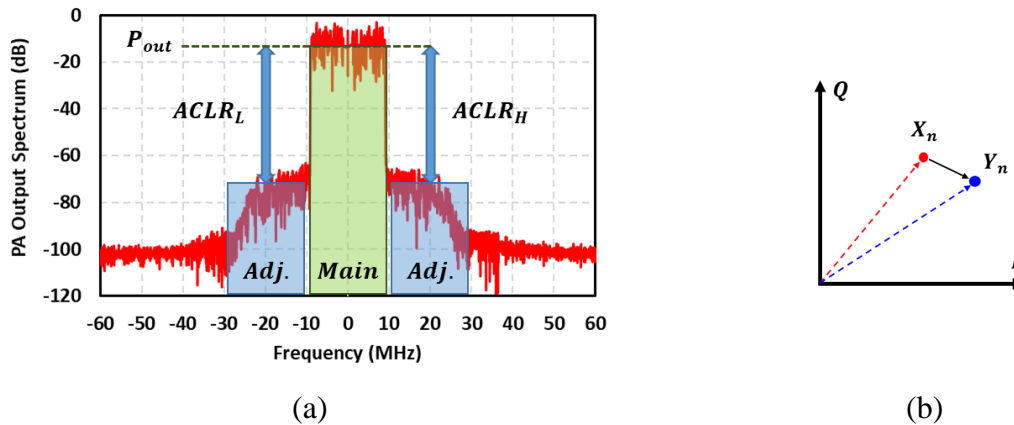


Figure 2.5 – (a) PA output spectrum showing Main channel and high, low adjacent channels, (b) IQ plot showing original and emitted symbols with error vector.

The second metric is the error vector magnitude (EVM) which represents the in-band distortion. It measures the magnitude between the original symbol X_n and the transmitted symbol Y_n .

EVM can be calculated using (2.7).

$$EVM = \frac{\sum_{n=1}^M |Y_n - X_n|^2}{\sum_{n=1}^M |X_n|^2} \quad (2.7)$$

1.5 Bandwidth

Finally, a PA is designed to provide optimal performance around a centre frequency f_0 . The bandwidth of a PA represents the frequency range $[f_{min}; f_{max}]$, for which the above-mentioned performance indicators can be maintained below a given variation threshold. The bandwidth is generally expressed in terms of the fractional bandwidth (FBW) using (2.8).

$$FBW = \frac{f_{max} - f_{min}}{f_0} \tag{2.8}$$

An example is provided in Figure 2.6 which shows the measured PAE and Psat achieved in [14] over a range of frequencies. In their paper, the authors note that the saturated power, peak PAE and back-off PAE remain higher than 32dBm, 50%, and 40% respectively between 1.9GHz and 2.7GHz, thereby resulting in a fractional bandwidth of 34.7%.

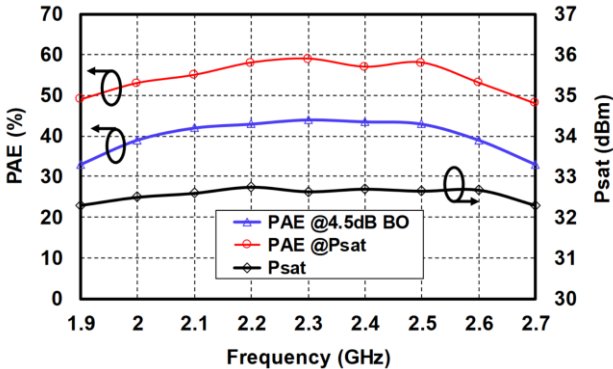


Figure 2.6 – Measured PAE and Psat over frequency [14].

2 PA Operation

Depending on their mode of operation, power amplifiers can be grouped into two main categories. The first is the traditional linear PAs which includes class-A, B, AB, and C where the output power is directly linked to the input power. The second category is the switch-mode PAs (Class-D, E) where the output power is dictated by the supply voltage and duty cycle of the input signal. In most cases, a PA circuit can be broken down into the generic diagram of Figure 2.7 where the PA consists of a transistor connected to matching and harmonic control networks that perform impedance transformation and waveform shaping.

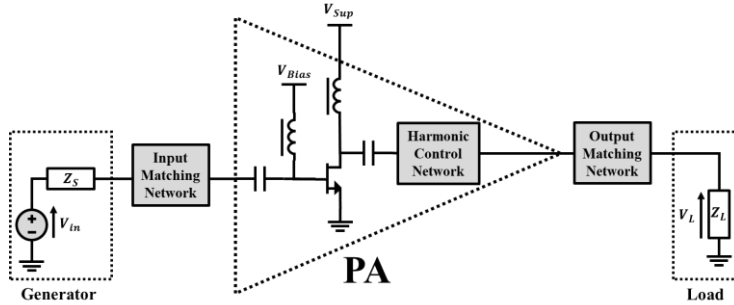


Figure 2.7 – Generic power amplifier schematic.

The choice of a transistor technology sets the maximum allowed gate (V_{GSmax}) and drain (V_{DSmax}) voltages. In order to correctly use the transistor, it must first be characterized and its different parameters extracted. First, a transistor is defined by its DC IV characteristics which can be extracted by sweeping the DC bias and supply voltages as shown in Figure 2.8(a).

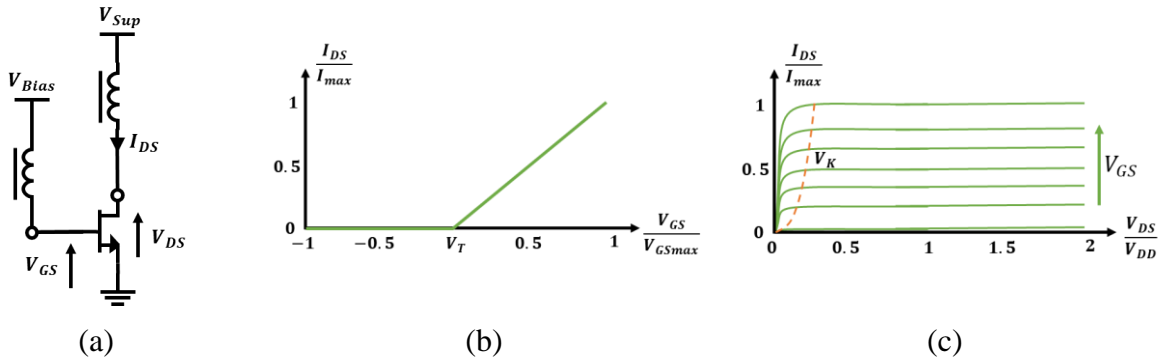


Figure 2.8 – (a) DC sweep transistor schematic. (b) Normalized Id-Vg characteristic representing drain current vs gate voltage. (c) Normalized Id-Vd characteristic representing drain current vs drain voltage for different gate voltages with knee region.

The Id-Vg characteristic is obtained by plotting the drain current value I_{DS} against the gate voltage V_{GS} . Figure 2.8(b) shows a simplified linear approximation of the Id-Vg characteristic of an ideal transistor which will be used instead of the conventional quadratic form. Drain current is generated when the gate bias voltage exceeds a certain threshold voltage V_T . Maximum drain current I_{max} is achieved when the gate voltage is maximum ($V_G = V_{GSmax}$). The slope of the line between these two values determines the ideal transconductance g_m .

When designing a PA, the maximum drain current I_{max} is set by the class of operation and the targeted output power. The transistor gate width can then be estimated using (2.9), where

$J_{sat|dev}$ refers to the current density of the PA device (maximum current for 1mm of transistor gate width).

$$w_t = \frac{I_{max}}{J_{sat|dev}} \tag{2.9}$$

The Id-Vd characteristic plots the drain current I_{DS} against the drain voltage V_{DS} for different gate voltage V_{GS} . The curves show two regions of operation: an ohmic region where the drain current increases with respect to the drain voltage, and a saturation region where the transistor delivers a constant current regardless of the drain voltage. The transition between these two regions is delimited by the knee voltage denoted V_K and indicated by the dashed line in Figure 2.8(c).

An ideal MOS transistor can be represented by a voltage-controlled current source as shown in Figure 2.9(a). The behaviour of real transistors is much more complex but it can be generally approximated using the equivalent model given in Figure 2.9(b) [15]. The different parameters of this model can be extracted using *Appendix A*.

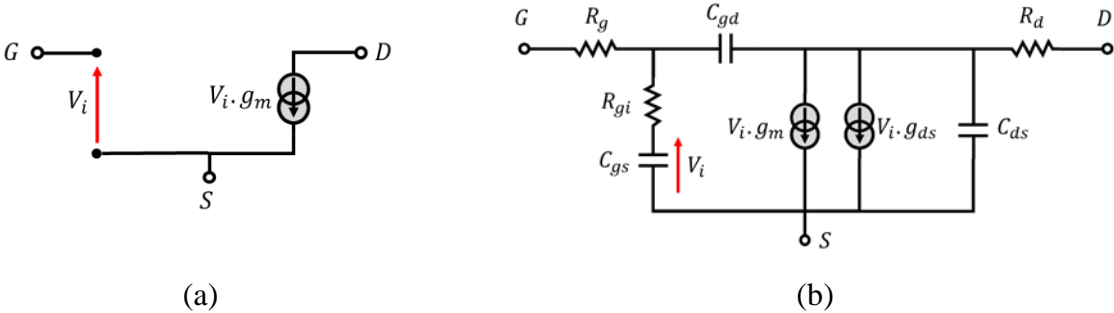


Figure 2.9 – (a) Ideal large-signal transistor model (b) Large-signal transistor model with linear parasitic elements.

2.1 Linear Class PAs

The aim of this section is to provide a general description of the linear operating classes (Class-A/AB/B/C) that have been covered extensively in numerous previous works such as [16].

Figure 2.10(a) shows the generic schematic of a linear class PA. Coupling capacitors are used at the input and output of the transistor in order to prevent DC signals flowing to the ground. At the output, an LC tank tuned at f_0 shorts out all of the harmonic components leaving only a pure sinewave at the load R_L . The transistor supply is fixed at V_{DD} and the PA class of operation is determined by the bias voltage $V_{GS|0}$ as illustrated in Figure 2.10(b).

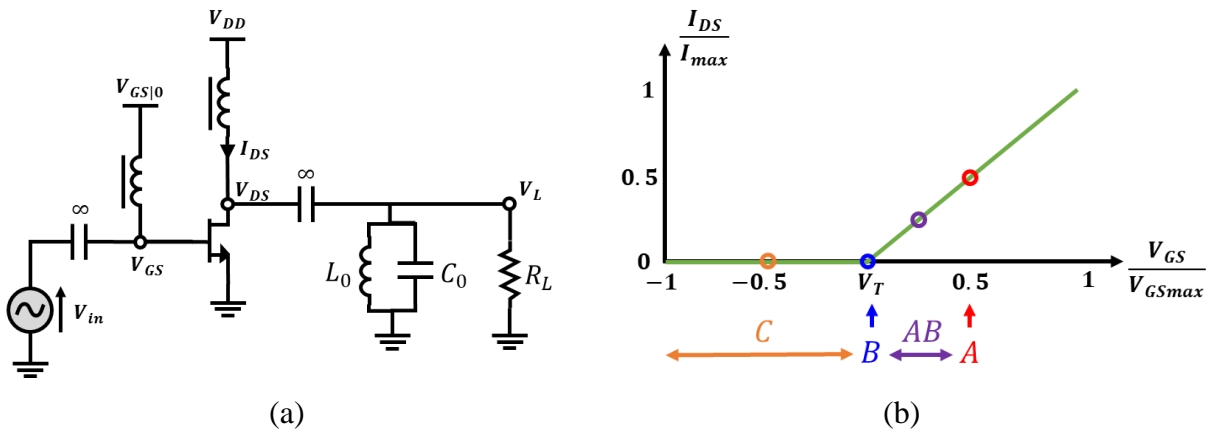


Figure 2.10 – (a) Linear-class PA schematic. (b) Transistor characteristic with the bias voltage point for different classes.

Figure 2.11 shows how the IV characteristics can be used to determine linear PA operation in the case of class-A (red curves) and class-B (blue curves).

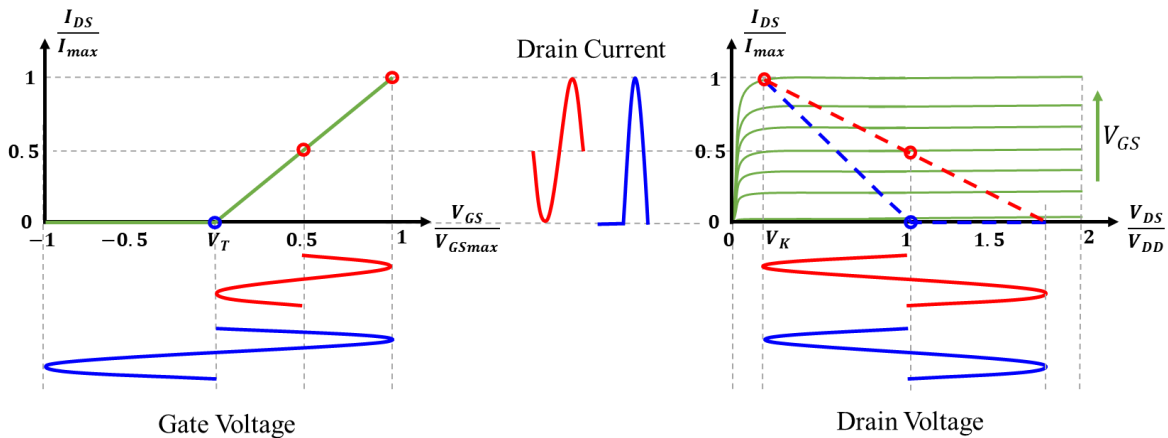


Figure 2.11 – Examples of Class-A (red) and Class-B (blue). $V_T = 0$ for simplicity.

In class-A, the PA is biased at:

$$V_{GS|A0} = \frac{V_{GSmax} - V_T}{2} \tag{2.10}$$

The gate voltage is a combination of the DC component and the amplitude of the fundamental frequency of the RF voltage input $V_{GS|A1}$.

$$v_{GS|A}(t) = V_{GS|A1} \cdot \sin(\omega_0 t) + V_{GS|A0} \quad (2.11)$$

$$V_{GS|A1} = \frac{V_{GSmax} - V_T}{2} \quad (2.12)$$

The gate voltage excursion is entirely within the conduction range of the transistor characteristic, and as a result, the drain current waveform is a sinewave with a DC component as shown in (2.13).

$$i_{DS|A}(t) = -\frac{I_{max}}{2} \cdot \sin(\omega_0 t) + \frac{I_{max}}{2} \quad (2.13)$$

$$I_{DS|A0} = \frac{I_{max}}{2} \quad (2.14)$$

Class-A has a conduction angle $\psi = 2\pi$ (i.e. a full period) since the drain current sinewave is not truncated.

Moving to the Id-Vd characteristic two operating points can be defined, the first is the maximum operating point ($V_K; I_{max}$). As the DC supply voltage is set to V_{DD} , the second operating point is ($V_{DD}; I_{DS|A0}$). These two points define the load line (shown in dashed red in Figure 2.11) whose slope can be used to calculate the optimal resistance value $R_{opt|A}$, such that

$$R_{opt|A} = -\frac{\Delta V_{DS}}{\Delta I_{DS}} = \frac{V_{max}}{I_{max}} \quad (2.15)$$

$$V_{max} = 2 \cdot (V_{DD} - V_K) \quad (2.16)$$

The drain voltage is obtained by projecting the drain current curve onto the load line and results in the equation in (2.17).

$$v_{DS|A}(t) = -V_{DS|A1} \cdot \sin(\omega_0 t) + V_{DD} \quad (2.17)$$

$$V_{DS|A1} = V_{DD} - V_K \quad (2.18)$$

Finally, the load voltage is a pure sinewave without a DC component since DC is blocked by the coupling capacitor.

$$v_{L|A}(t) = -V_{DS|A1} \cdot \sin(\omega_0 t) \quad (2.19)$$

Class-AB, B, and C modes are slightly different as they have lower conduction angles. Below an example is given using class-B, starting with the gate voltage:

$$v_{GS|B}(t) = V_{GS|B1} \cdot \sin(\omega_0 t) + V_T \quad (2.20)$$

$$V_{GS|B1} = 2 \cdot V_{GS|A1} \quad (2.21)$$

As the transistor is biased at the threshold voltage V_T , only half of the sinewave is amplified and the drain current (seen in blue in Figure 2.11) is a truncated half-sine. Class-B has a conduction angle $\psi = \pi$. Projecting the drain current onto the load line results in the same drain voltage as class-A operation.

$$v_{DS|B}(t) = v_{DS|A}(t) \quad (2.22)$$

Output power P_{out} is defined as the real (active) RF power delivered to the load. At the fundamental frequency, the load R_L is purely resistive, and the drain voltage swing is $V_{DS|A1}$. Therefore, P_{out} can be expressed as:

$$P_{out} = \frac{1}{2} \cdot (V_{DD} - V_K) \cdot I_{DS|1} \quad (2.23)$$

Since the drain current isn't always a pure sinewave, its fundamental component amplitude $I_{DS|1}$ must be extracted using the Fourier series. This is done by expressing the drain current as:

$$i_{DS}(t) = I_{DS|0} + \sum_{n=1}^{\infty} I_{DS|n} \cdot \cos(n \cdot \theta) \quad (2.24)$$

The first five harmonic amplitudes along with the DC component are shown for different conduction angles in Figure 2.12(a).[16]

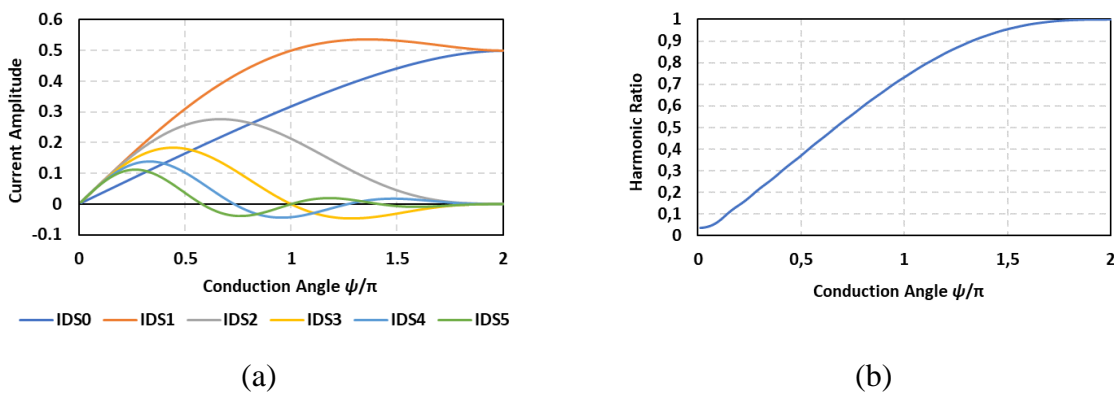


Figure 2.12 – Drain current (a) harmonics amplitude and (b) harmonic ratio for different conduction angle values.

For a given I_{max} , the fundamental current amplitude is the same for both class-A and class-B meaning that they have the same maximum output power P_{out} . $I_{DS|1}$ reaches its maximum when in class-AB, and goes to zero in deep class-C.

Class-A is said to be the most linear, as its output current (and voltage) contain no harmonic components. Meanwhile, class-C is seen as the least linear due to the high number of current harmonics. This result is represented in Figure 2.12(b) through the harmonic ratio defined as the ratio of fundamental current amplitude to the sum of all harmonics as shown below.

$$HR = \frac{I_{DS|1}}{\sum_{n=2}^{\infty} I_{DS|n}} \quad (2.25)$$

The drain efficiency of the PA is the ratio of P_{out} to the DC power P_{DC} calculated using:

$$P_{DC} = V_{DD} \cdot I_{DS|0} \quad (2.26)$$

The drain current expression is therefore:

$$DE = \frac{1}{2} \cdot \frac{(V_{DD} - V_K)}{V_{DD}} \cdot \frac{I_{DS|1}}{I_{DS|0}} \quad (2.27)$$

In an ideal case where $V_K = 0$, the drain efficiency is determined solely by the ratio of the fundamental current to the DC current, both of which can be extracted from Figure 2.12(a). The efficiency goes from a theoretical 100% in deep class-C to 50% in class-A as shown in Figure 2.13(a).

In (2.21), it was shown that the input voltage amplitude in class-B is twice that of class-A for the same drain voltage (2.22). Therefore, the class-B power gain G_p is four times less than that of class-A (i.e. $-6dB$). This is proven in the simulation results shown in Figure 2.13(b) where power gain drops rapidly when going from class-A to class-C.

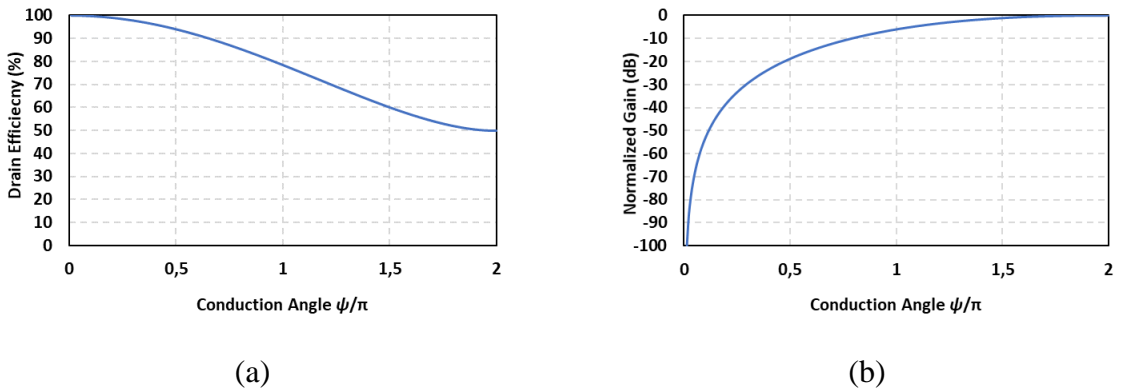


Figure 2.13 – (a) PA drain efficiency and (b) power gain for different conduction angles.

In conclusion, linear class PAs showcase one of the fundamental challenges of PA design. There is always a trade-off between efficiency, linearity, and output power or gain. 100% efficiency can theoretically be obtained when operating in deep class-C, but the resulting PA would have no gain and therefore be unable to provide any power to the load. In order to tackle this issue,

other PA modes of operation were developed, among which Class-E operation considered in our work and will therefore be explained next.

2.2 Class-E PA

The class-E PA first proposed by the Sokals in 1975 [17] is illustrated in Figure 2.14(a).

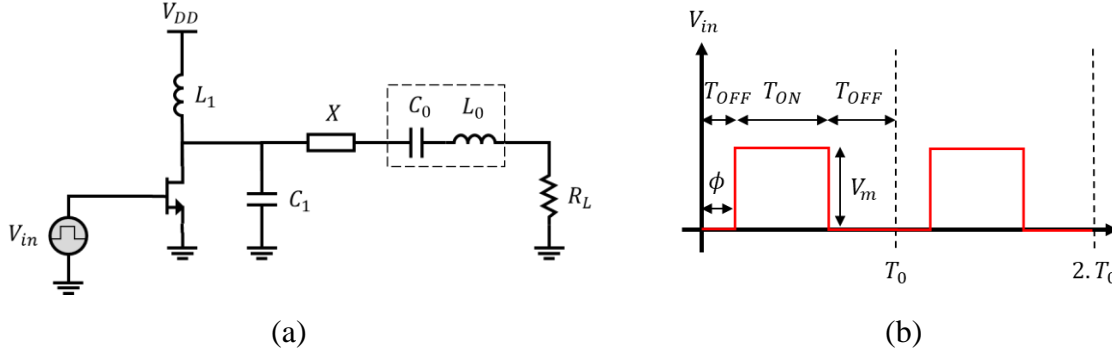


Figure 2.14 – (a) Ideal class-E PA with shunt capacitance. (b) Square-wave input voltage V_{in} .

Switch-mode operation consists in driving the transistor with a pulsed signal creating two possible states; i.e. ON and OFF. Output waveform shaping is then achieved at the drain plane using a matching network composed of L_1 , C_1 and X in order to ensure high efficiency. Finally, a series LC resonator (L_0 and C_0) is used to filter the output signal and obtain a sinusoidal output voltage at the load.

Class-E operation is of itself a very complex subject. Extensive work on class-E PA design exists in the current literature such as [18]. In this section, only the basics of class-E operation are presented and will be used as a basis for the power cell design in later chapters.

The driving voltage V_{in} , shown in Figure 2.14(b), is a pulsed wave defined by its period T_0 , phase delay ϕ , voltage amplitude V_m and duty cycle d which is calculated through (2.28)

$$d = \frac{T_{ON}}{T_0} \quad (2.28)$$

For optimal class-E operation, the following conditions need to be respected:

- Zero Voltage Switching condition (ZVS): the drain voltage value is zero at the turn-on and turn-off switching times.
- Zero Slope Switching condition (ZSS): the slope of the drain voltage is zero at the turn-on switching time.

These conditions ensure that the drain voltage and current waveforms are orthogonal for the different harmonics as illustrated in Figure 2.15(a). As a result, there is no overlap between the two waveforms in the time-domain as shown in Figure 2.15(b). Therefore, no power is dissipated, meaning that optimal class-E operation can theoretically achieve 100% of drain efficiency.

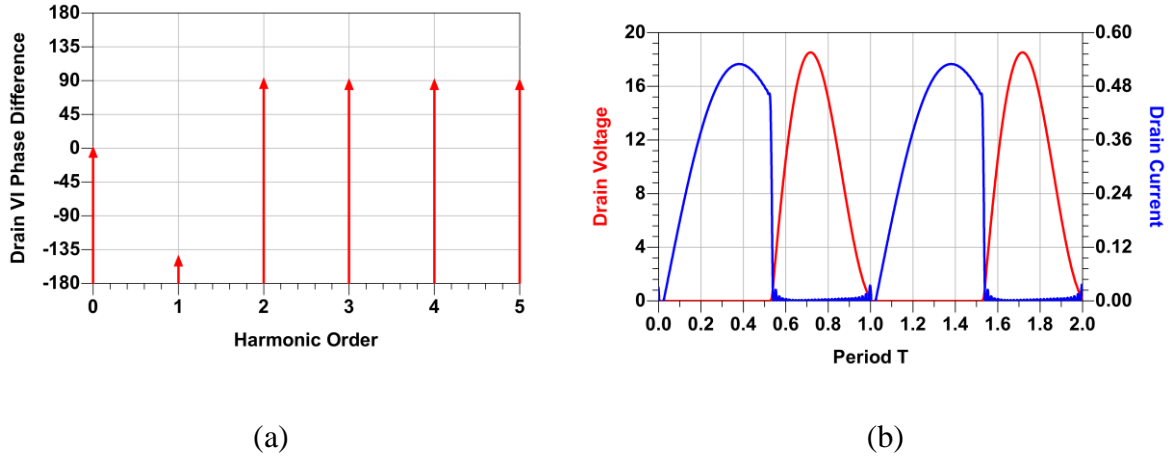


Figure 2.15 – (a) Drain Voltage-Current phase difference at different harmonics (b) Drain voltage and current time domain waveforms.

Throughout the years, there have been numerous works detailing the design of class-E PAs while taking into account different non-ideal factors such as on-state resistance and finite supply inductance [19]–[22]. The most practical Class-E PA design method is introduced in [23]. It uses a set of four parameters referred to as the K-set parameters. For a duty cycle of 50%, the K-set parameters can be approximated using polynomial equations depending on the harmonic factor q defined as:

$$q = \frac{1}{\omega_0 \cdot \sqrt{L_1 \cdot C_1}} \quad (2.29)$$

Where ω_0 represents the angular frequency relating to the design frequency f_0 . Depending on the desired q value, the four K-set parameters can be computed using the equations given in Table 2.1 below.

Table 2.1 - K-set design equations for $0.6 \leq q \leq 1.65$.

K-set Parameter	$0.6 \leq q \leq 1$	$1 < q \leq 1.65$
K_L	$44.93q^2 - 94.32q + 52.46$	$8.085q^2 - 24.53q + 19.23$
K_C	$0.426q^2 - 0.379q + 0.3$	$-6.97q^3 + 25.93q^2 - 31.071q + 12.48$
K_P	$0.74q^2 - 0.6q + 0.76$	$-11.9q^3 + 42.753q^2 - 49.63q + 19.7$
K_X	$-0.73q^2 - 0.411q + 1.03$	$-2.9q^3 + 8.8q^2 - 10.2q + 5.02$

These parameters can then be used to calculate the output network components for a targeted output power P_{OUT} , supply voltage V_{DD} , and frequency f_0 as shown in the following equations.

$$R_L = K_P \cdot \frac{V_{DD}^2}{P_{OUT}} \quad (2.30)$$

$$L_1 = K_L \cdot \frac{R_L}{\omega_0} \quad (2.31)$$

$$C_1 = K_C \cdot \frac{1}{R_L \cdot \omega_0} \quad (2.32)$$

$$X = K_X \cdot R_L \quad (2.33)$$

Finally, the series resonator elements are designed using the loaded quality factor Q_L .

$$L_0 = Q_L \cdot \frac{R_L}{\omega_0} \quad (2.34)$$

$$C_0 = \frac{1}{L_0 \cdot \omega_0^2} \quad (2.35)$$

For q lower than 0.6, the equations introduced in [24] for class-E PA with ideal choke inductance can be used. Finally, higher values of q (>1.65) are not covered as they lead to physically impractical component values. q can therefore be seen as a design variable in the class-E design space and can be chosen depending on the circuit implementation requirements (such as the value of L_1) or as a means of performance optimization for a given application.

The previous design equations result in optimal class-E performance at $d = 0.5$, which corresponds to maximum output power and efficiency. By sweeping the duty cycle, the efficiency and output power profiles can be extracted as shown on Figure 2.16(a). It can be concluded that optimal performance is not strictly limited to $d = 0.5$, as the PA seems to hold high power and efficiency for the range $d \in [0.4; 0.55]$. Beyond this level, the PA is able to provide more power, though at a lower efficiency. This result can be mathematically predicted by using the analysis in [25], which looks at the effects of circuit variations on the ideal Class-E operation.

One of the challenges of ideal class-E operation is generating square-wave inputs with sufficiently small rise and fall times, as well as low duty cycle signals. Moreover, a square-wave signal requires a high order of harmonics and can lead to spectral spreading issues when attempting to linearize the PA using predistortion techniques. Luckily, pseudo-class-E operation is possible using a sinewave input. In [18], the authors show how a class-E PA can be driven using a single tone sinewave signal without resulting in significant performance degradation. This is showcased in Figure 2.16(b) where an ideal class-E PA circuit simulated with a sinewave input signal (and an equivalent duty cycle of 0.5) results in near ideal drain efficiency value at peak power.

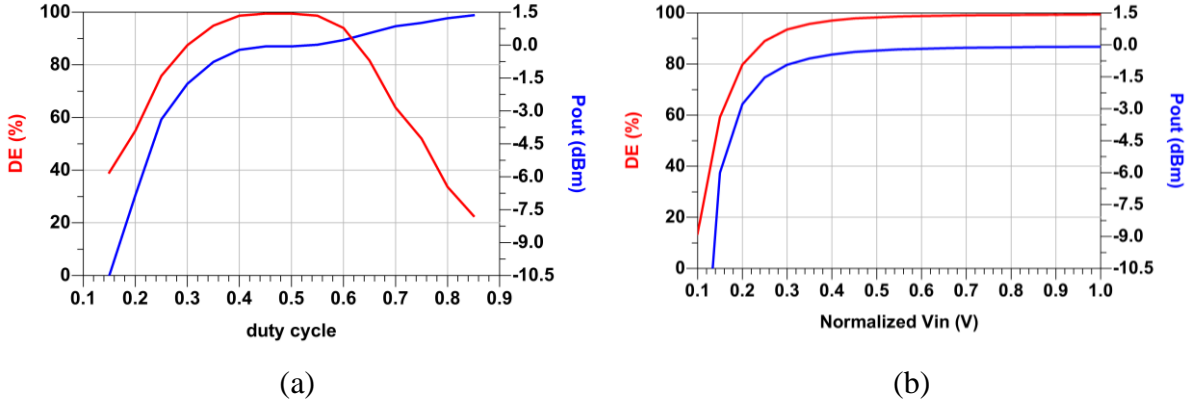


Figure 2.16 – (a) Class-E PA drain efficiency and output power as a function of duty cycle (b) Single-tone sinewave driven Class-E PA drain efficiency and output power as a function of input voltage amplitude.

Class-E can therefore provide a theoretical peak efficiency of 100% when operated with adequate input drive signal. However, peak efficiency is only achieved at peak output power as can be seen in Figure 2.16. Given that a PA operates over a range of output power values, it is important to consider its performance not only at peak power but also at back-off.

2.3 Back-Off Operation

So far, all of the analysis was conducted at peak output power. However, a PA seldom operates at peak power and instead operates most of the time in power back-off (BO) as can be seen in the PDF functions of Figure 2.17(a). In Figure 2.17(b), an example is given using the class-A loadline.

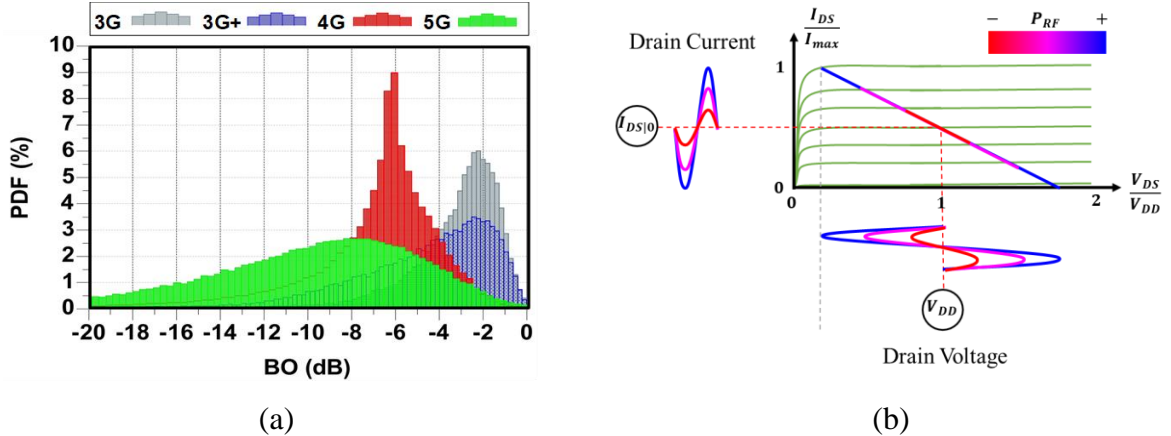


Figure 2.17 – (a) Probability distribution functions of different communication standards versus back-off power level. (b) Class-A PA load-line for different RF power levels showing drain voltage and current waveforms.

For different output power levels P_{RF} , the drain voltage and current waveforms sweep a different interval of the loadline. It is important to note however that the DC drain voltage and current, V_{DD} and $I_{DS|0}$ respectively, remain constant for all values of P_{RF} . This means that DC power P_{DC} is constant thus leading to a drop in drain efficiency (DE) at back-off. Figure 2.18(a) shows the evolution of DE with respect to the normalized output power referred to as output power back-off (OBO) and calculated using (2.36).

$$OBO = P_{out|dBm} - \max(P_{out|dBm}) \quad (2.36)$$

The simulation results show an exponential decrease in efficiency for all linear classes. Consequently, the linear PA classes present a low average efficiency when amplifying modulated signals such as LTE or 5G whose PDF shows a concentration at $OBO = -7dB$.

Figure 2.18(b) shows the normalized power gain values for different PA linear classes. In the case of class-AB operation, the power gain is the same as that of class-A in low power, but decreases in high power. The reason for this gain drop is the class-AB bias point: Class-A and class-B are biased to conduct 100% and 50% of the input signal respectively regardless of the signal amplitude. On the other hand, the conduction angle of class-AB is defined for maximum input voltage. That is because in class-AB, signals whose amplitudes are less than V_{GS10} are not truncated and therefore resemble class-A. However, input signals whose amplitude exceeds V_{GS10} are progressively truncated leading to a behaviour that's closer to class-B. As a result, class-AB starts off at the same gain as class-A before decreasing at higher power and approaching the gain of class-B. Meanwhile, class-C exhibits the opposite behaviour as its gain increases relatively to the effective conduction angle at the given OBO.

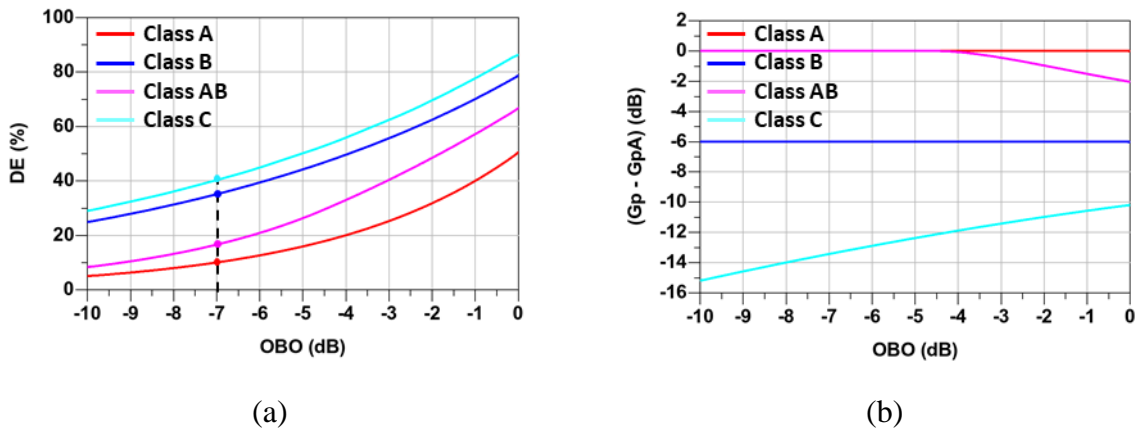


Figure 2.18 – (a) PA drain efficiency and (b) power gain versus normalized output power for class-A, class-AB, and class-B PA simulations.

In Class-E, much like the previously discussed linear class PAs, efficiency decreases at back-off as seen in Figure 2.19(a). Similarly, the gain value, plotted in Figure 2.19(b), also shows degradation when the PA is operated at back-off.

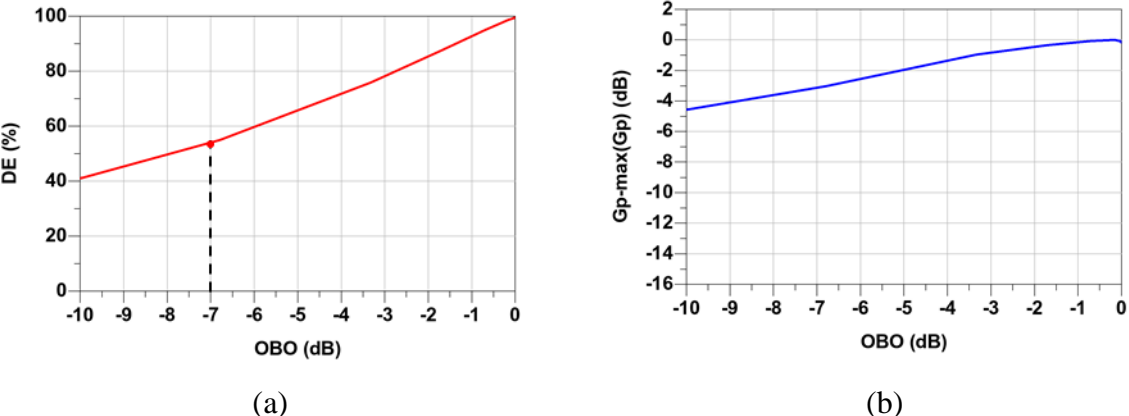


Figure 2.19 – Class-E PA simulation results showing (a) drain efficiency and (b) normalized power gain versus normalized output power.

In conclusion, both linear classes and Class-E PAs present the same efficiency degradation in back-off. Throughout the years, different PA architectures have been developed to improve efficiency in back-off. Most of these architectures can be grouped into two main categories.

The first category relates to supply modulation PA architectures such as envelope tracking (ET) [26] and envelope elimination and restoration (EER) [27]. The idea is to adapt the DC supply voltage V_{DD} to the required output power thereby reducing DC power dissipation at lower output power levels as shown in Figure 2.20. The downside of this method is that it requires an additional device (supply modulator) to dynamically change the supply voltage accordingly. This can be especially difficult to achieve for wideband modulated signals as it requires complex analog control circuitry with additional power consumption.

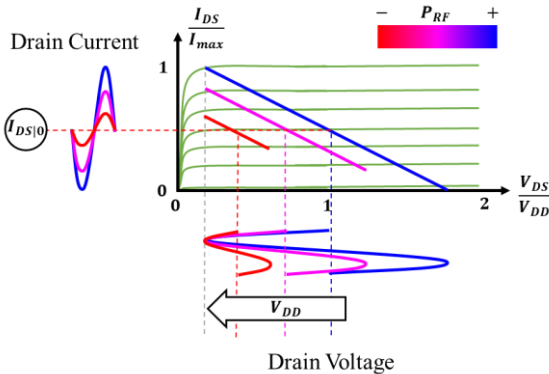


Figure 2.20 – Supply modulation on a class-A PA.

The second category relates to load modulation PA architectures that will be discussed in the next section.

3 Load Modulated PA Architectures

Active load modulation is achieved when two or more amplifiers inject a current into the same load which leads to a variation of the impedance perceived at each branch [28]. Figure 2.21 shows how load modulation can be used to increase efficiency as changing the slope of the transistor loadline results in a decrease of the DC drain current $I_{DS|0}$ which also leads to a decrease in DC power at lower output power levels.

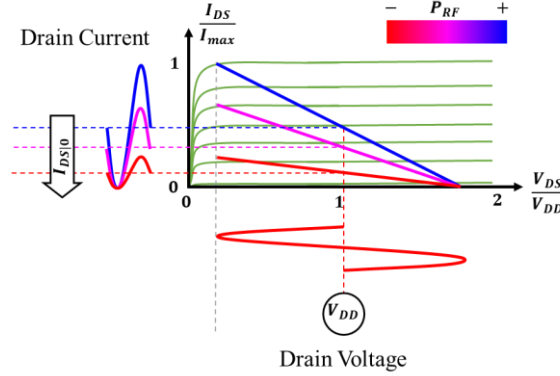


Figure 2.21 – Load modulation on class-A PA loadlines and drain I-V curves.

Throughout the years, different load modulation architectures have been proposed, with Doherty and Outphasing as the most common ones. In this section, the principle of operation of both architectures will be exposed.

Load modulation can increase a PA's efficiency at BO by changing the load impedance seen at the drain of the transistor in order to keep the PA operating at peak efficiency. First, the optimal load impedance needs to be determined as a function of output power.

In the case of linear class PAs, the optimal load R_{opt} is inversely proportional to the output power P_{out} as given by (2.37).

$$R_{opt} = \frac{V_{max}}{I_{max}} = \frac{(V_{DD} - V_K)^2}{P_{out}} \quad (2.37)$$

Class-E on the other hand, requires more effort. Unlike linear classes, class-E operation requires a complex optimal load impedance in order to achieve optimum performance. The value of the load impedance $Z_{L|CS}$ at the internal current plane of the transistor can be calculated using the equations from [29] presented below in the case of $d = 0.5$ and $q \rightarrow 0$.

$$Z_{L|CS}(n, \omega) = \begin{cases} (1.52 + j \cdot 1.11) \cdot R & n = 1 \\ -j \cdot \frac{5.45}{n} \cdot R & n > 1 \end{cases} \quad (2.38)$$

$$R = 0.58 \cdot \frac{V_{DD}^2}{P_{OUT}} \quad (2.39)$$

This expression, while useful in some cases, remains rather restrictive as it only applies to a specific value of d and q . Moreover, this equation provides the complex load impedance at the

internal current plane of the transistor without any indication for the output matching network elements. It is therefore more practical to design the class-E PA at peak power, and then perform a load-pull simulation by varying the complex load impedance Z_L as shown in Figure 2.22.

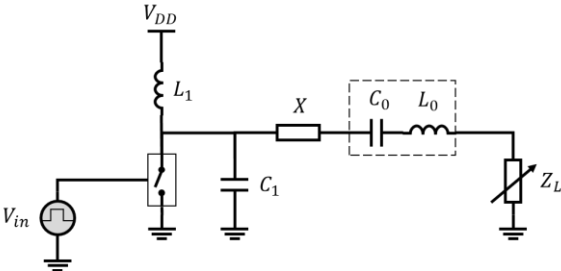


Figure 2.22 – Class-E PA with varying load Z_L for load-pull simulation.

While this simulation can be run for any value of q and d , only the case of $q = 1$ and $d = 0.5$ will be presented as an example.

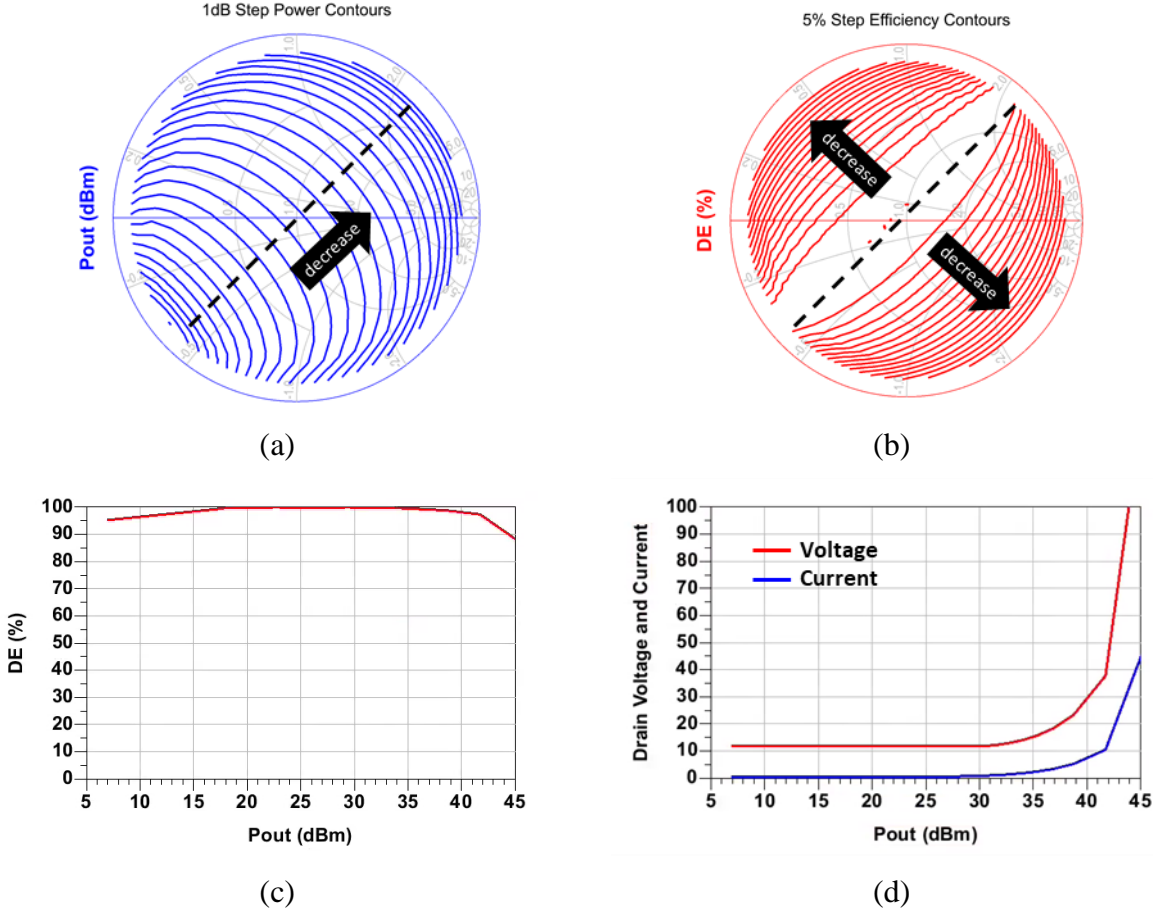


Figure 2.23 – Smith Charts normalized to R with optimal performance load line in black showing: (a) Output power contours (b) Drain efficiency contours. For impedance values located on the optimal performance load line: (c) Drain efficiency versus output power, (d) Drain voltage and current amplitudes.

The load-pull contours in Figure 2.23(a) and Figure 2.23(b), show the effect of load variation on the output power and efficiency respectively. It can be seen that maximum efficiency can be achieved for a range of load impedances located on the black dashed line, going through the centre of the smith chart. That same line goes through the different power contours, meaning that a Class-E PA can address different power levels while maintaining maximum efficiency. Figure 2.23(c) illustrates this finding, by plotting the efficiency against the output power for

load impedances located on the optimal performance load line (black dashed line seen on the smith charts). It is important though to keep in mind that this load-pull simulation is based on an ideal switch class-E PA. In reality, the achievable power range will be much more limited as the performance shown above would require extremely high DC voltage and current as shown in Figure 2.23(d).

Having determined the optimal load impedance as a function of output power, the next sections will present two of the main load modulation PA architectures which are capable of providing dynamic load modulation in order to increase efficiency at back off.

3.1 Outphasing PA Architecture

The Outphasing PA (OPA) was first proposed by Henry Chireix in his paper in 1935 [30]. In an ideal OPA architecture, such as the one in Figure 2.24(a), the input signal $S_{in}(t)$ is split by a Signal Component Separator (SCS) into two signals with constant amplitude, $S'_1(t)$ and $S'_2(t)$ with a phase shift of $+\theta$ and $-\theta$ respectively.

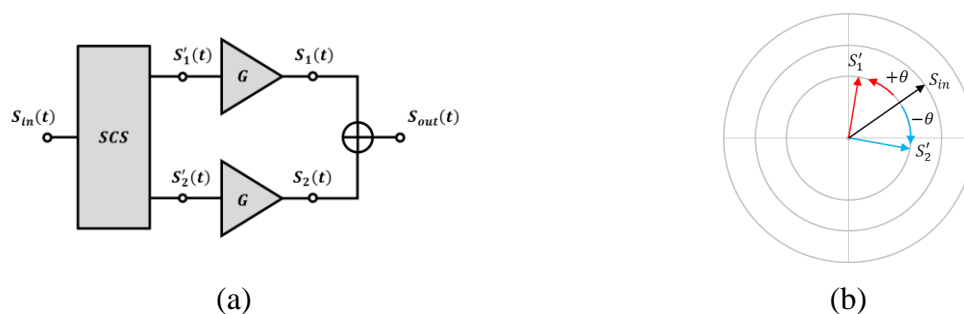


Figure 2.24 – (a) Outphasing PA block diagram, (b) Complex-plane, input signal decomposition

Given an input signal $S_{in}(t)$, with an amplitude modulation $E(t)$ and a phase modulation $\phi(t)$ expressed in phasor form:

$$S_{in}(t) = E(t) \cdot e^{j\phi(t)} \quad (2.40)$$

The input signal $S_{in}(t)$ is split into two constant envelope signals $S'_1(t)$ and $S'_2(t)$ as shown in Figure 2.24(b).

$$S_{in}(t) = S'_1(t) + S'_2(t) \quad (2.41)$$

$$S'_{1,2}(t) = \frac{\max[E(t)]}{2} \cdot e^{j[\phi(t) \pm \theta(t)]} \quad (2.42)$$

Where $\theta(t)$ represents the Outphasing angle and is calculated using:

$$\theta(t) = \cos^{-1} \left(\frac{E(t)}{\max[E(t)]} \right) \quad (2.43)$$

The signals $S'_1(t)$ and $S'_2(t)$ have constant envelopes and can therefore be used to operate the two PA branches at saturation, ensuring that amplification is achieved at peak efficiency. Finally, the output signal $S_{out}(t)$ can be obtained by adding the amplified signals.

$$\begin{aligned}
 S_{out}(t) &= S_1(t) + S_2(t) \\
 &= G \cdot S_{in}(t)
 \end{aligned}
 \tag{2.44}$$

Depending on the type of combiner, different OPA efficiency profiles can be achieved. In the case of an isolating structure, such as the Wilkinson combiner of Figure 2.25(a), the main focus is on the linearity which comes at the cost of the efficiency at back-off. This is because the output power is controlled by dissipating the excess power in the isolating resistor, which results in high loss at low power levels [31]–[33] and therefore low efficiency as seen in Figure 2.25(b). This method is usually referred to as LInear amplification using Non-linear Components (LINC) as coined by Cox [34] and does not involve load modulation due to the isolating combiner. On the other hand, non-isolating combiners, such as the classic Chireix combiner shown in Figure 2.25(c), allow for active load modulation and subsequently high efficiency at back-off as illustrated in Figure 2.25(d). These types of combiners will be the focus of this thesis since efficiency is highly critical in mobile applications.

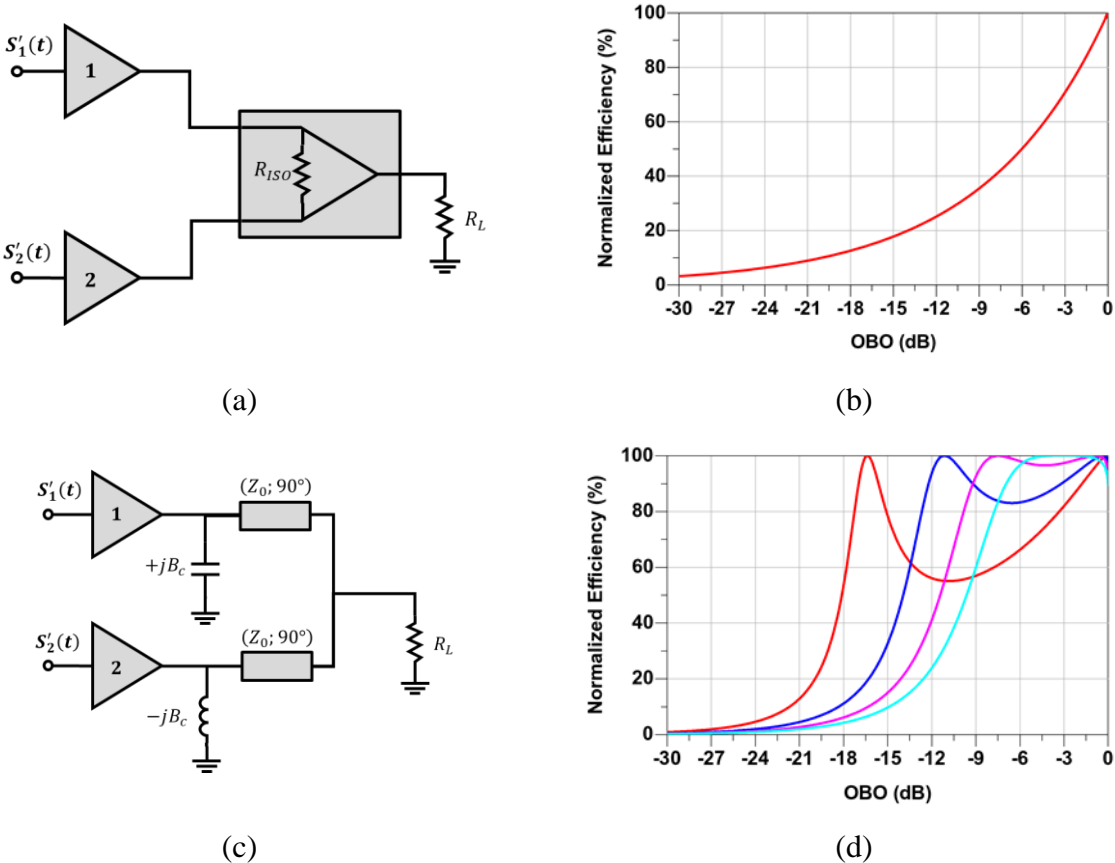


Figure 2.25 – (a) Isolating Wilkinson combiner based OPA and (b) its associated efficiency profile with respect to back-off output power level. (c) Classic Chireix non-isolating combiner based OPA with (d) possible efficiency profiles that can be achieved depending on the combiner design values.

Outphasing load modulated combiners, such as the classic Chireix combiner of Figure 2.25©, lead to load impedance variation in both paths. Each amplifier sees a complex load which can

be represented by its conductance (real part of the admittance) and susceptance (imaginary part of the admittance) as shown in Figure 2.26(a) and (b) respectively.

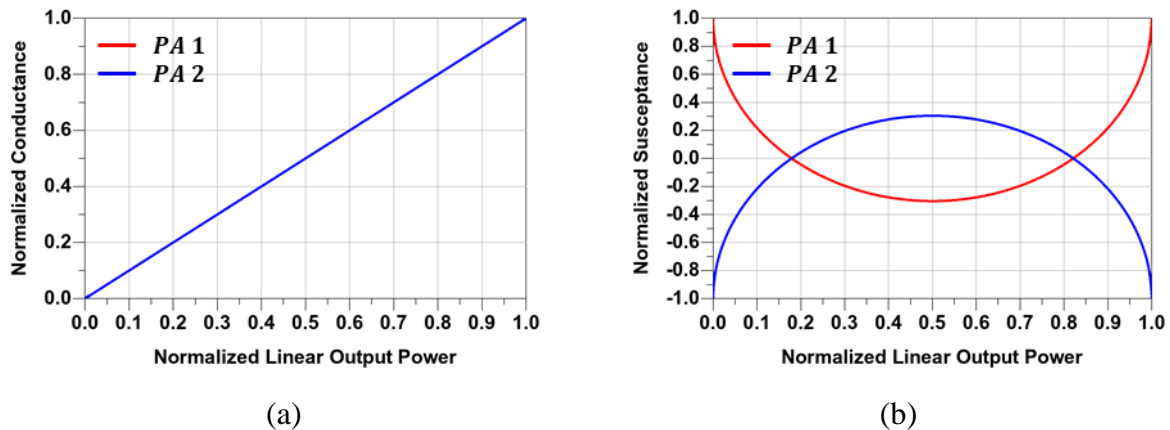


Figure 2.26 – OPA Chireix combiner simulation showing normalized PA load (a) conductance and (b) susceptance versus output power.

The efficiency peaks occur when the load is purely real. The peak efficiency at back-off can therefore be controlled through the combiner design.

This PhD work focuses on integrated sub-6 GHz power amplifiers. Therefore, OPA realizations respecting these criteria are selected and compiled in Table 2.2.

Table 2.2 – State of the art sub-6 GHz Outphasing PAs.

		[35]	[36]	[37]	[38]
	Power Cell Class	D	E	E	E
	CMOS Technology (nm)	28	65	45	130
	Supply (V)	3.6	1.25	2.4	2.8
CW	Freq. (GHz)	1.7	1.8	2.4	1.85
	P_{sat} (dBm)	29.7	20.1	29.5	20.7
	PAE @ P_{sat} (%)	34.7*	60.7	46.7*	36.9
	OBO (dB)	-	12	6	6
	PAE @ OBO (%)	-	21	21.16*	20
Modulated LTE	Modulation	64QAM	64QAM	64QAM	-
	BW (MHz)	20	20	10	10
	ACLR (dBc)	-37.6	-22	-50.4	-31.6
	Pout (dBm)	23.1	13.1	22.3	24.7
	PAE (%)	15.3*	33.6	21*	20.8
	DPD Linearization	No	Yes	Yes	Yes

*DE value used instead of PAE

In practice, it would seem that the high efficiency OPA operation is not easily achieved as evidenced by the efficiency measurements presented in the state of the art. All of the OPAs use high efficiency power cells in either class-E or class-D, but somehow fail to provide high efficiency values both in continuous wave (CW) and modulated LTE signal measurements. Moreover, none of the OPAs are capable of delivering an output power higher than 30dBm.

This work will therefore explore the OPA architecture in an attempt to design a high efficiency integrated OPA capable of delivering 33dBm of output power.

3.2 Doherty PA Architecture

The Doherty Power Amplifier (DPA) was first proposed by William H. Doherty in 1936 as a way to increase the efficiency of the first broadcasting transmitters [39]. A Doherty PA is usually implemented by a combination of a *Main* or *Carrier* amplifier, and an *Auxiliary* or *Peaking* amplifier. The idea is to modulate the load seen by the Main amplifier by injecting a current from an Auxiliary amplifier, in order to provide optimal efficiency at a given back-off [40].

Figure 2.27 shows the classic configuration of a DPA, which consists of a Main and Auxiliary amplifier combined via an impedance inverter with a characteristic impedance Z_T at the output of the Main amplifier, and connected to a common load R_L .

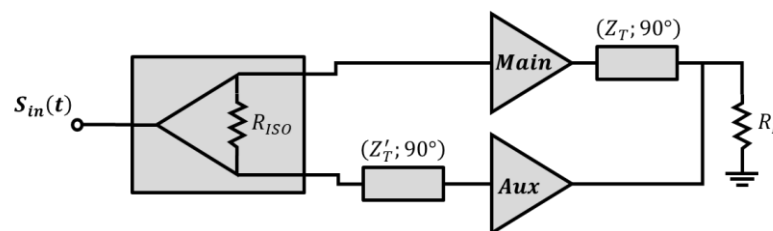


Figure 2.27 – Classic DPA power stage and output combiner schematic.

The DPA behaviour can be broken into two operating regions:

- In the low power region, only the Main amplifier is active and delivers power to the load. This mode of operation extends until the main amplifier reaches saturation. The output power level corresponding to the main saturation point is referred to as output back-off (OBO).
- Beyond this point, the Auxiliary amplifier starts contributing by injecting current into the common load R_L . This region is known as the Doherty region and is characterized by a decrease of the load impedance seen by the Main amplifier due to load modulation [41].

This behaviour can be seen in Figure 2.28(a) where the Auxiliary current is null in the low power region and starts to rise after the dashed line indicating the beginning of the Doherty region. Meanwhile, the Main PA provides current in both regions but reaches voltage saturation at the start of the Doherty region and remains saturated as shown in Figure 2.28(b).

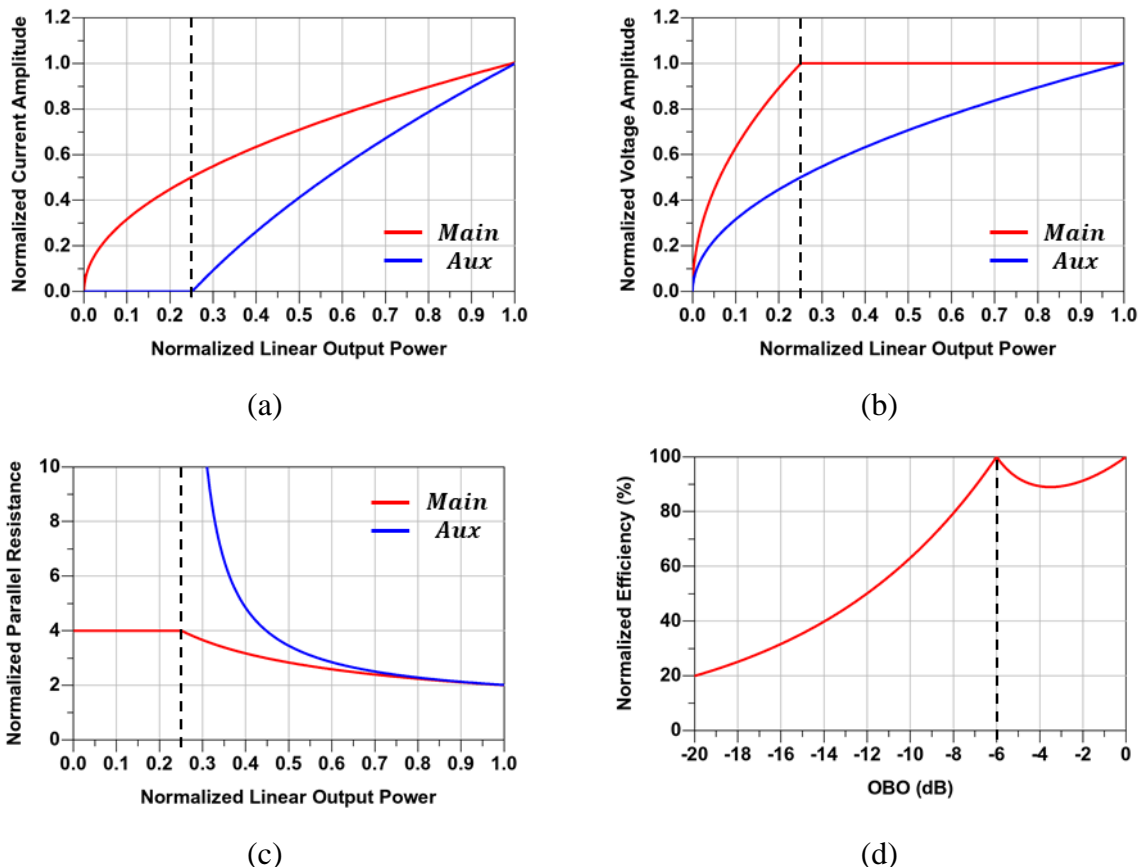


Figure 2.28 – Normalized Main and Auxiliary (a) current (b) voltage (c) parallel load resistance versus linear output power. (d) Normalized DPA efficiency versus normalized output back-off in dB. The dashed line marks the BO critical operation point separating low power and Doherty regions.

The effect of load modulation can be observed in Figure 2.28(c) where the load seen by each branch is represented by the normalized parallel resistance. In the low power region, the Main branch load resistance is constant at $4 R_L$. When the Auxiliary starts conducting current, both the Main and Auxiliary branch load resistances are dynamically changed and become $2 R_L$ at peak power.

Finally, the DPA efficiency profile is presented in Figure 2.28(d) and shows two peaks. The first, at -6dB , occurs when the Main amplifier is operating alone and reaches saturation. The second peak is seen at peak power where both Main and Auxiliary PA operate at saturation. As with OPA operation, different BO values can be addressed with Doherty operation depending on the design of the combiner and drive profile.

Table 2.3 summarizes the main performance achieved in published DPA works within the sub-6 GHz range for mobile applications using both CW and modulated LTE signals. These DPAs all use a lumped pi-network version (LCL) of the classic quarter-wave transmission line combiner with the exception of [42] which uses a more compact LC combiner as shown in Figure 2.29(a) and (b) respectively. The combiner from [42] is of particular interest to this study as its compact structure makes it more suitable for integration. However, the authors of this paper were only able to achieve 3dB back-off when using the LC combiner.

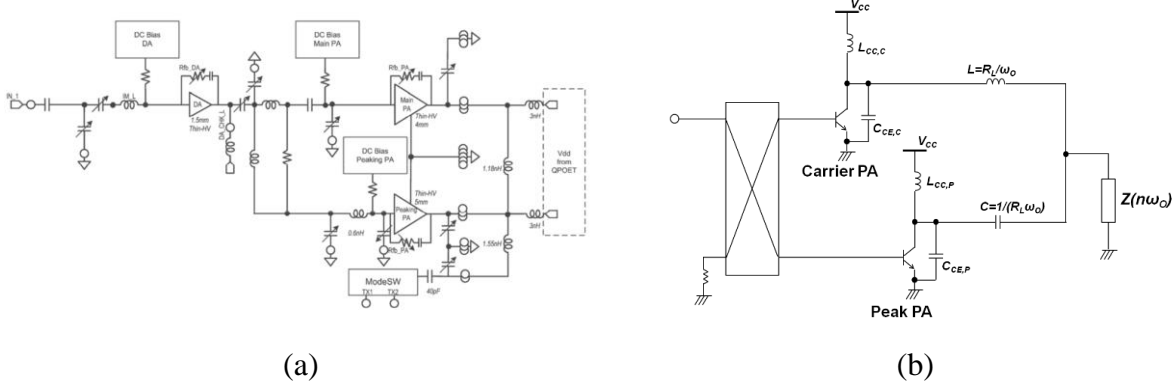


Figure 2.29 – Examples of published DPA designs using (a) LCL combiner [43] and (b) LC combiner [42].

Moreover, the PAs from Table 2.3 use linear class power cells, with the Main and Auxiliary biased in class-AB and class-C respectively. As a result, the peak PAE is between 45% and 59%, while the PAE at 6dB of back-off is between 30% and 40%. It would therefore be interesting to explore the possibility of increasing PA efficiency, both at peak and back-off through the use of class-E power cells along with a compact combiner capable of higher back-off operation.

Table 2.3 – State of the art sub-6 GHz Doherty PAs.

		[42]	[44]	[43]	[45]
	Class (Main/Aux)	AB/C	AB/C	AB/C	AB/C
	Combiner Type	LC	CLC	CLC	CLC
	Technology	InGaP	SOI	SOI	SOI
	Supply (V)	3.4	3.4	3.4	3.4
CW	Freq. (GHz)	2.5	2.5	1.95	2.3
	P _{sat} (dBm)	30	32.7	30.5	32.8
	PAE @ P _{sat} (%)	45	57	52	59
	OBO (dB)	4	6	5	6
	PAE @ OBO (%)	40	40	47	40
Modulated	Modulation	QPSK	QPSK	-	QPSK
	BW (MHz)/RB	10/50	10/12	20/-	10/50
	Band (GHz)		1.9-2.7	1.55-2.3	1.9-2.7
	ACLR (dBc)		-35	-30	-35
	Pout min/max (dBm)		28		28
	PAE min.max (%)		35/45		35/44
	DPD Linearization	Yes	No	Yes	No

In conclusion, load-modulated PA architectures are capable of high efficiency operation at back-off. The peak back-off efficiency is mainly determined by the combiner design. As a result, optimizing the combiner is of utmost importance, and will therefore be the subject of the following chapter.

4 Conclusion

In this chapter, the different metrics used to evaluate PA performance are introduced. By evaluating output power, efficiency, gain, linearity and bandwidth, the PA can be compared to other PAs.

Next, the fundamentals of PA operation were laid out starting with transistor characteristics which can be used to determine the required device size as well as the parasitic effects to be taken into account. The linear class mode of operation was then detailed, showing the inherent compromise between efficiency, gain and linearity when moving from class-A to class-C. While a PA in deep class-C can theoretically achieve 100% efficiency, it has no gain and as result it cannot be used in practice. This issue can be solved with the use of switch-mode PAs, and more specifically class-E. This class of operation is theoretically capable of achieving 100% efficiency. This however, comes at the cost of linearity. Looking at back-off operation, both the linear classes and class-E suffer from an exponential drop in efficiency when the PA operates below its peak value. Given that modern communication standards require 7 to 10 dB OBO operation, more complex PA architectures are needed.

Load modulated PAs allow for high efficiency operation in back-off by dynamically changing the load impedance seen by the amplifier. Optimal impedance required to ensure peak efficiency operation at different OBO are determined for linear classes as well as class-E. The two main load modulation PA architectures are then presented. Outphasing and Doherty operation are briefly exposed and shown to be good candidates for LTE and 5G applications.

Chapter 3. Load Modulated Power Amplifier Combiner Design

1	Outphasing PA Combiners.....	43
1.1	Reactive Compensation	45
1.2	Delay-Line Compensation	47
1.3	Driving Mode.....	48
1.4	Outphasing Combiner Analysis	49
2	Doherty PA Combiners	57
2.1	DPA Combiner Analysis	58
3	Conclusion.....	66

High efficiency load modulated PA architectures rely on a dedicated output combiner to achieve peak efficiency at back-off. This chapter provides an in-depth theoretical analysis of different combiner designs for Outphasing (OPA) and Doherty (DPA) PA architectures.

First, this work attempts to structure the various possible Outphasing combiners and driving modes into a homogenous unified design approach, showing that all of the combiners in the literature can be traced back to the same circuit originally proposed by Henry Chireix. To the author's best knowledge, this is the first instance of a unified, comparative Outphasing analysis and design methodology that takes into account all the different combiner architectures and driving modes.

Next, combiners for Doherty PA are explored. Existing DPA combiner synthesis and analysis methods present a limitation where the ideal DPA current/voltage conditions are only respected at the start and end of the Doherty operation range but not throughout. This issue is addressed and resolved with the introduction of a new generic combiner analysis method that can provide optimized DPA operation for a variety of input conditions.

1 Outphasing PA Combiners

Throughout the years many different Outphasing implementations have been put forward. The main difference between the proposed architectures tends to be the combiner design. All existing Outphasing PA architectures can be viewed as variations and sometimes generalisations of the original combiner design and can be classified into different categories, which will be detailed in the sections below.

In his original paper, Henry Chireix defines the Outphasing circuit as:

“Dividing the amplifier [...] into two parts, each including one or several tubes according to the power required and each part having its own output circuit while the load circuit is differentially coupled to both.”

Using this definition, Chireix’s Outphasing system can be represented as seen in Figure 3.1, by two voltage sources, V_1 and V_2 , with a constant amplitude V_{max} and conjugate phases $\pm\theta$ as described in (3.1), connected to a series resistor R .

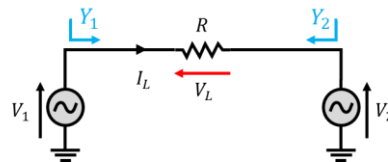


Figure 3.1 – Differential Outphasing voltage combiner.

$$V_{1,2} = V_{max} \cdot e^{j\pm\theta} \quad (3.1)$$

The load voltage V_L is then calculated using mesh analysis as shown in (3.2).

$$\begin{aligned} V_L &= V_1 - V_2 \\ &= 2 \cdot V_{max} \cdot \sin(\theta) \cdot e^{j\frac{\pi}{2}} \end{aligned} \quad (3.2)$$

The amplitude of V_L is therefore controlled through the Outphasing angle θ , which is contained within the $[0^\circ; 90^\circ]$ interval.

The admittances Y_1 and Y_2 seen by each source respectively can be calculated through:

$$\begin{aligned} Y_{1,2} &= \pm \frac{I_L}{V_{1,2}} \\ &= \frac{1}{R} \cdot [2 \cdot \sin^2(\theta) \pm j \cdot \sin(2 \cdot \theta)] \end{aligned} \quad (3.3)$$

Using the result from the equation above, we can determine that the load admittances are complex conjugates of each other. This is of course due to the symmetry of the design with the initial voltage sources also being complex conjugates of one another.

The load admittance can be expressed in terms of conductance G_0 and susceptance B_0 as shown below. Plotting these values yields Figure 3.2(a) and Figure 3.2(b) respectively.

$$Y_1 = Y_2^* = G_0 + j \cdot B_0 \quad (3.4)$$

$$G_0 = \Re[Y_1] = \frac{2}{R} \cdot \sin^2(\theta) \quad (3.5)$$

$$B_0 = \Im[Y_1] = \frac{1}{R} \cdot \sin(2 \cdot \theta) \quad (3.6)$$

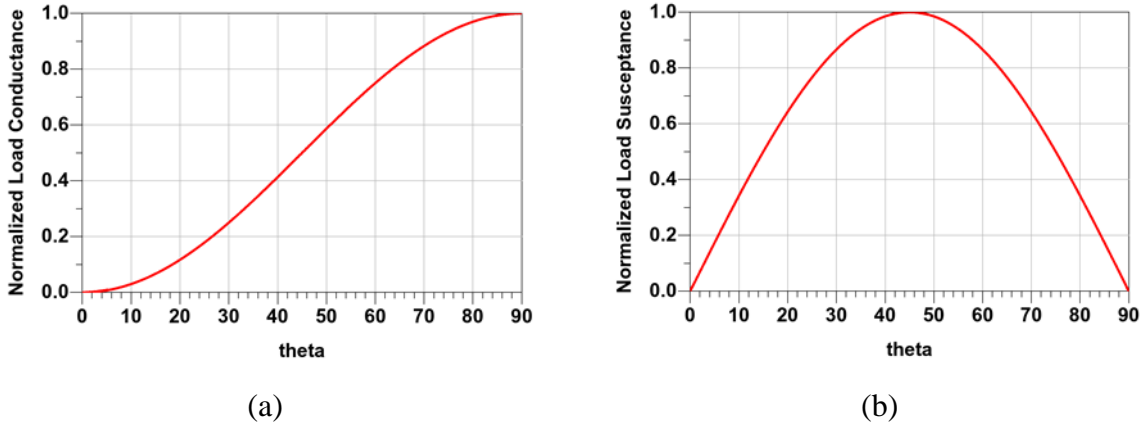


Figure 3.2 – (a) Normalized load conductance, (b) Normalized load susceptance.

The RF output power delivered to the load can therefore be calculated through:

$$P_{out}(\theta) = V_{max}^2 \cdot G_0(\theta) \quad (3.7)$$

Finally, assuming that the ideal power cells are operating in a linear mode such as Class-B, the efficiency of the Outphasing system can be calculated using (3.8) [46].

$$\eta = \eta_{max} \cdot \frac{G_0}{|Y_{1,2}|} \quad (3.8)$$

Where η_{max} is the maximum theoretical efficiency for a given operating class. Figure 3.3(a) plots the normalized efficiency versus the Outphasing angle θ . Plotting the efficiency with respect to the output power shows that the efficiency decreases exponentially with the power level. The reason behind this drop is the increase in load susceptance B_0 seen by each branch as seen in Figure 3.3(b).

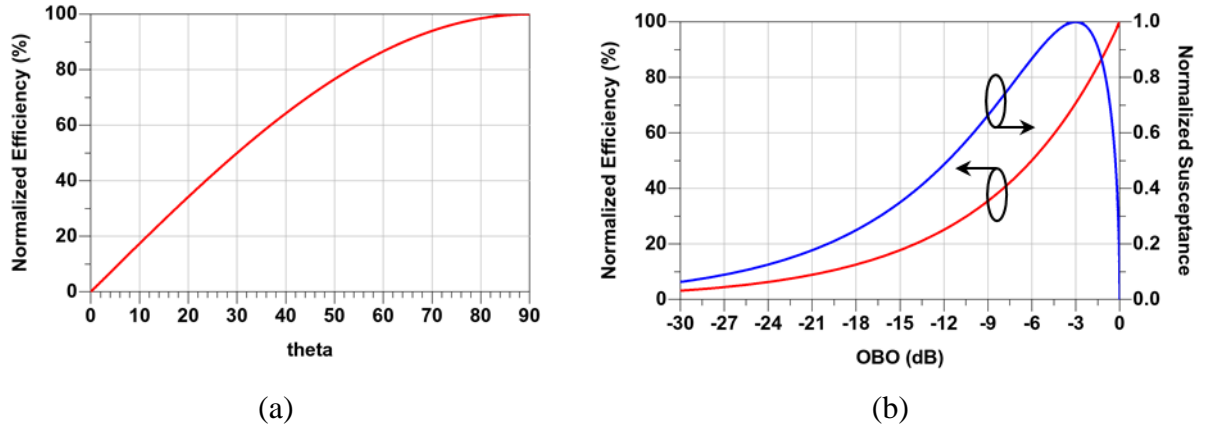


Figure 3.3 – (a) Normalized efficiency, (b) OPA efficiency and load susceptance with respect to normalized output power (OBO).

In order to achieve higher efficiency at power back-off, the imaginary part of the admittances $Y_{1,2}$ must be compensated (cancelled) for a given power level (and therefore for a given Outphasing angle). Reactive compensation and delay-line compensation are the two methods that can be used and are detailed in the following sections.

1.1 Reactive Compensation

Reactive compensation, as proposed by Chireix, consists of adding a shunt susceptance B_c to each branch of the circuit as seen in Figure 3.4(a).

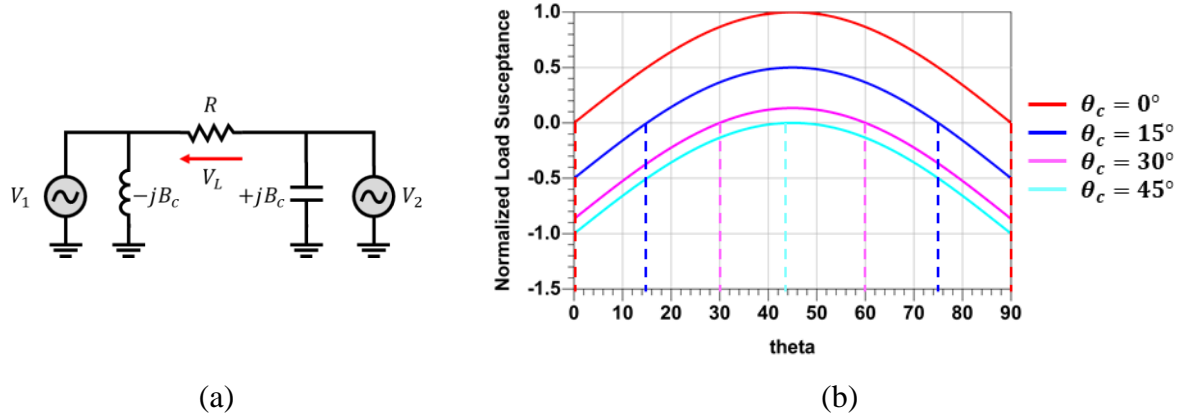


Figure 3.4 – (a) Differential voltage combiner with reactive compensation, (b) Load susceptance versus Outphasing angle for different compensation angle values.

The susceptance value is calculated using (3.9) where θ_c is the compensation angle at which the reactive part of the load is cancelled (Figure 3.4(b)).

$$B_c = \frac{1}{R} \cdot \sin(2 \cdot \theta_c) \quad (3.9)$$

The admittances seen by each branch, $Y'_{1,2}$ are then expressed as:

$$Y'_{1,2} = G_0 \pm j.(B_0 - B_c) \quad (3.10)$$

Given that B_0 is symmetrical with respect to $\theta = 45^\circ$, the compensation angle can take any value within the range $[0^\circ; 45^\circ]$. The susceptance is cancelled for two root values of θ as shown in (3.11).

$$B_0 - B_c = 0 \text{ for } \theta \in \{\theta_c; 90^\circ - \theta_c\} \quad (3.11)$$

Using (3.8) with the admittance value from (3.10), yields the plot in Figure 3.5(a).

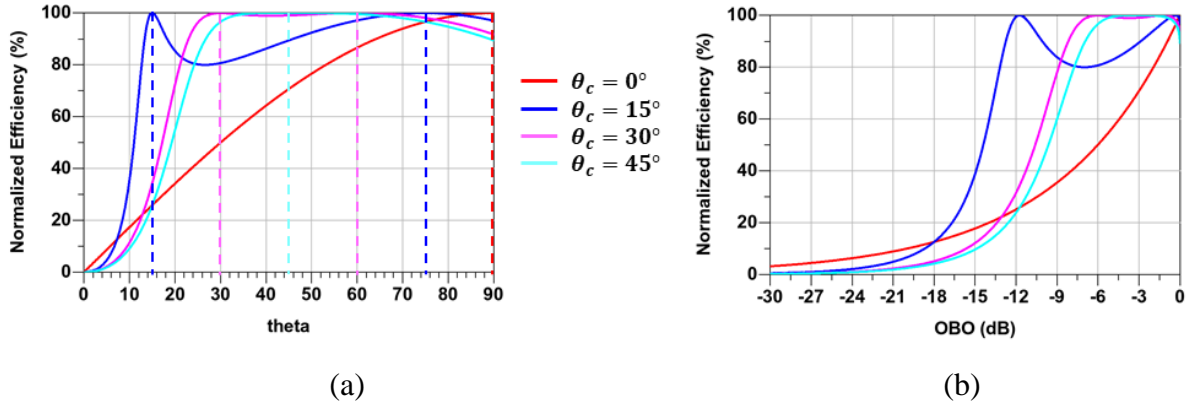


Figure 3.5 – (a) Efficiency with respect to Outphasing angle, (b) Efficiency with respect to output power back-off (OBO).

With the exception of $\theta_c = \{0^\circ; 45^\circ\}$, the efficiency profile shows two peaks as seen in Figure 3.5(a). The position of the peaks with respect to the output power back-off (OBO), can be determined using (3.12). This effect can be observed by plotting the efficiency against the output power as in Figure 3.5(b).

$$OBO_{dB}|_{Peak \eta} = \begin{cases} -20 \cdot \log[\sin(\theta_c)] \\ -20 \cdot \log[\cos(\theta_c)] \end{cases} \quad (3.12)$$

However, given that the first OBO_{dB} value is relatively close to the peak power, only the second expression is considered when referencing the back-off.

In most practical cases, the output of the combiner is connected to a grounded load. Therefore, a single ended version of the combiner is needed. By applying the differential to single-ended transformation highlighted in Appendix B section B.1.5, the circuit in Figure 3.4(a) becomes that of Figure 3.6(a).

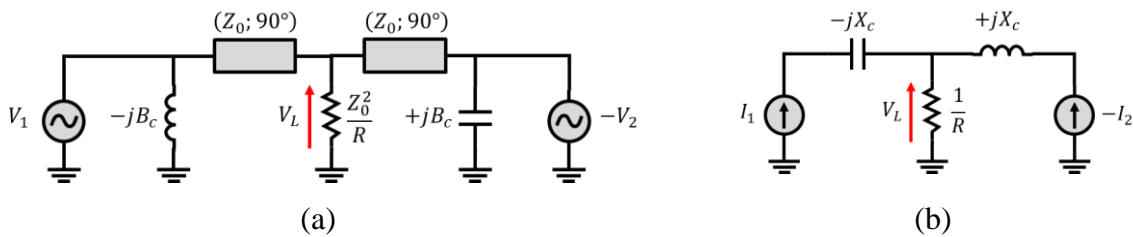


Figure 3.6 – Single-ended (a) voltage combiner, (b) current combiner with reactive compensation.

Moreover, a dual structure of the original differential combiner can be obtained by applying the circuit duality transformation detailed in *Appendix B section 0B.2* which results in the circuit of Figure 3.6(b) where $X_c = B_c$. Due to the duality transformation, the voltage sources become current sources, and therefore the combiner of Figure 3.6(b) is considered as a current combiner.

1.2 Delay-Line Compensation

The second type of compensation is the phase compensation which uses delay lines to achieve the same result as the classic Chireix reactive compensation. This method is preferred in high frequency and high power circuits where transmission lines can be easily implemented [47]–[49]. Figure 3.7(a) shows the differential voltage combiner circuit with the asymmetric transmission lines as compensation elements. Its single-ended equivalent, obtained through the differential to single ended transformation of *Appendix B section B.1.5*, is shown in Figure 3.7(b).

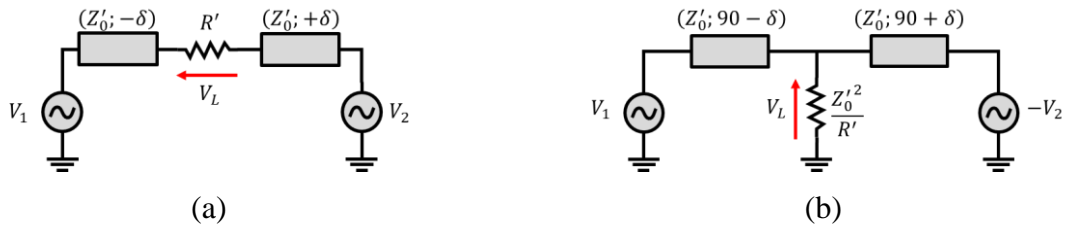


Figure 3.7 – (a) Differential voltage combiner, (b) Single-ended voltage combiner with delay-line compensation.

Once again, the dual circuit of Figure 3.7(a) can be obtained through the duality transform and results in the current combiners in Figure 3.8(a). The circuit in Figure 3.8(a) can be further simplified by replacing the transmission lines with their respective π -network lumped element models (*Appendix B section B.1.4*) and then resonating out the shunt reactive elements at the output node resulting in the combiner of Figure 3.8(b).

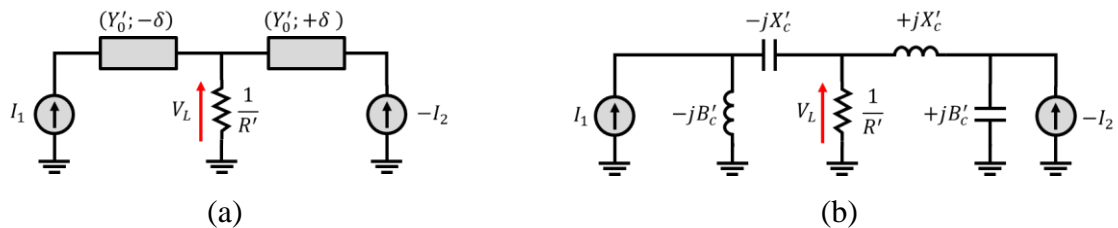


Figure 3.8 – (a) Single-ended (a) current combiner with delay-line compensation, (b) current combiner with simplified lumped equivalent of delay-line compensation.

In this section, the relation between the different Outphasing combiners has been explored, starting with the classical Chireix differential voltage combiner with reactive compensation. As previously discussed, single-ended combiners are generally preferred as the PA is usually connected to a grounded load.

Moreover, the single-ended architectures present a 180° phase shift (negative sign) of the second voltage/current source. This can be compensated by switching the compensations elements on the left and right of the load resistance. The resulting forms are shown in Figure 3.9 below.

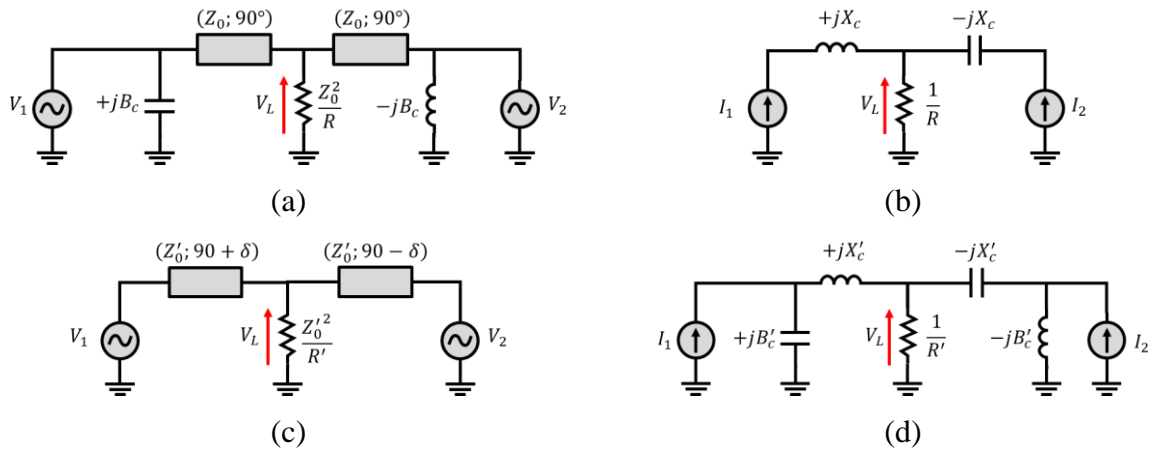


Figure 3.9 – (a) Voltage combiner and (b) Current combiner with reactive compensation, (c) Voltage combiner and (d) Current combiner with delay-line compensation. Without negative signs at sources.

These four OPA combiners represent the main architectures for both current and voltage combiners. In early OPA implementations, the classic single-ended Chireix voltage combiner of Figure 3.9(a), which can be classified as Reactive Compensation Voltage combiner (RCV) was the architecture of choice.

The emergence of higher frequency PAs led to the popularization of the Delay-line Compensation Voltage combiner (DCV) seen in Figure 3.9(c) as it doesn't require the use of discrete elements for reactive compensation which is directly achieved by changing the length of the transmission lines. Meanwhile, the Reactive Compensation Current combiner (RCC) shown in Figure 3.9(b) was favoured in applications requiring high integration as it is the most compact of the OPA combiner architectures.

Finally, the Delay-line Compensation Current combiner (DCC) of Figure 3.9(d) was to the author's best knowledge not showcased in any published works. This combiner architecture offers no clear advantage over the other three combiners as its lumped form is not as compact as the RCC combiner, and its transmission line form requires longer lines than the DCV combiner which might in part explain its absence from the literature. Its form was derived in this section through the duality transformation to complete the set. With the four main combiner architectures clearly defined, the driving mode must be considered next.

1.3 Driving Mode

The different combiner circuit variations presented so far include both voltage and current combiners obtained through the duality transformation. This shows that the Outphasing can be applied to either voltage sources (voltage-mode Outphasing) or current sources (current-mode Outphasing) and it can therefore be assumed that these two modes of operation can be used with any Outphasing combiner structure.

In voltage-mode, the phase control is applied to the input voltages as was described in (3.1). Similarly, in current-mode, the phase control is applied to the input currents as in (3.13) [50].

$$I_{1,2} = I_m \cdot e^{j\pm\theta} \quad (3.13)$$

The voltage and current sources used at the combiner inputs thus far represent the transistors of the OPA power cells. In order to maximise the PA's efficiency, the transistors must be saturated, and as a result, the amplitude of the input voltages $V_{1,2}$ is fixed at V_{max} . While this condition is achieved directly in voltage-mode using an ideal voltage source, a specific current drive is needed in current-mode as expressed through (3.14), where I_m is the current amplitude and $Z_{CM}(\theta)$ is the input impedance of the combiner.

$$I_m = \frac{V_{max}}{|Z_{CM}(\theta)|} \quad (3.14)$$

Since the input impedance of the combiner depends on the selected architecture, a novel Outphasing combiner analysis method is proposed in the following section.

1.4 Outphasing Combiner Analysis

In this section, a novel generalized Outphasing combiner analysis is described. The first step consists in calculating the input admittances of the combiner circuit. This can be easily achieved by representing the combiner as a cascade of two-port networks and calculating the equivalent ABCD matrix of the circuit. An example is provided in Figure 3.10 using the RCC combiner.

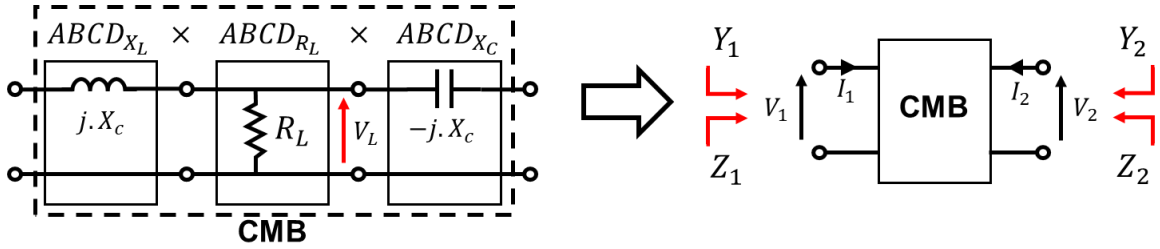


Figure 3.10 – Cascaded two-port representation of the RCC combiner and its equivalent simplified form to be used for analysis.

Using the equivalent generic combiner matrix, the following equation can be defined:

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \times \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \quad (3.15)$$

The input admittance expression is therefore:

$$Y_1 = \left(C - \frac{A \cdot D}{B} \right) \cdot \frac{V_2}{V_1} + \frac{D}{B} \quad (3.16)$$

The input voltages are complex conjugates as stated in (3.1), and the network is composed of passive elements and therefore reciprocal so $AD - BC = 1$. Therefore, the input admittance can be simplified and rewritten as in (3.17) below.

$$Y_1 = \frac{1}{B} \cdot (D - e^{-j \cdot 2 \cdot \theta}) \quad (3.17)$$

The input admittance Y_2 is the complex conjugate of Y_1 and can be found using (3.18).

$$Y_2 = \frac{1}{B} \cdot (A - e^{j.2.\theta}) \quad (3.18)$$

Finally, the conjugate input impedances Z_1 and Z_2 , can be calculated using the equations below.

$$Z_1 = \frac{1}{C} \cdot (A + e^{-j.2.\theta}) \quad (3.19)$$

$$Z_2 = \frac{1}{C} \cdot (D + e^{j.2.\theta}) \quad (3.20)$$

The RCC is the most compact of the proposed combiner architectures, and is therefore well suited for the integration requirements of our work. As a result, this combiner architecture will be used in the following sections to better illustrate the merits of the proposed analysis and design method which can be applied to any different combiner architecture.

The ABCD matrix of the RCC combiner can be expressed as in (3.21).

$$ABCD = \frac{1}{R_L} \cdot \begin{pmatrix} R_L + j \cdot X_c & X_c^2 \\ 1 & R_L - j \cdot X_c \end{pmatrix} \quad (3.21)$$

The series reactive elements of the combiner must cancel out the imaginary part of the complex impedance seen at the inputs of the combiner for a given compensation angle θ_c . This can be achieved by calculating the reactive components using (3.22).

$$X_c = R_L \cdot \sin(2 \cdot \theta_c) \quad (3.22)$$

In voltage-mode operation, the input admittance calculated through (3.17) can be expressed as:

$$Y_{1|VM} = \frac{1}{R_L \cdot \sin^2(2 \cdot \theta_c)} \cdot [2 \cdot \sin^2(\theta) + j \cdot (\sin(2 \cdot \theta) - \sin(2 \cdot \theta_c))] \quad (3.23)$$

Figure 3.11(a) and Figure 3.11(b) show the evolution of the quadrature components of the input admittance $Y_{1|VM}$ as a function of the Outphasing angle for different compensation angles while Figure 3.11(c) shows the evolution of the input admittances normalized with respect to the load R_L . Unlike the classic Chireix combiner, the conductance value G is dependent on the compensation angle θ_c . Consequently, different values of θ_c result in different output power levels (calculated using (3.7)). This is showcased in Figure 3.11(d) where the efficiency η , calculated using (3.8) and (3.23), is plotted against the output power. This effect can complicate the combiner design process, as the output power must be adapted to each compensation value.

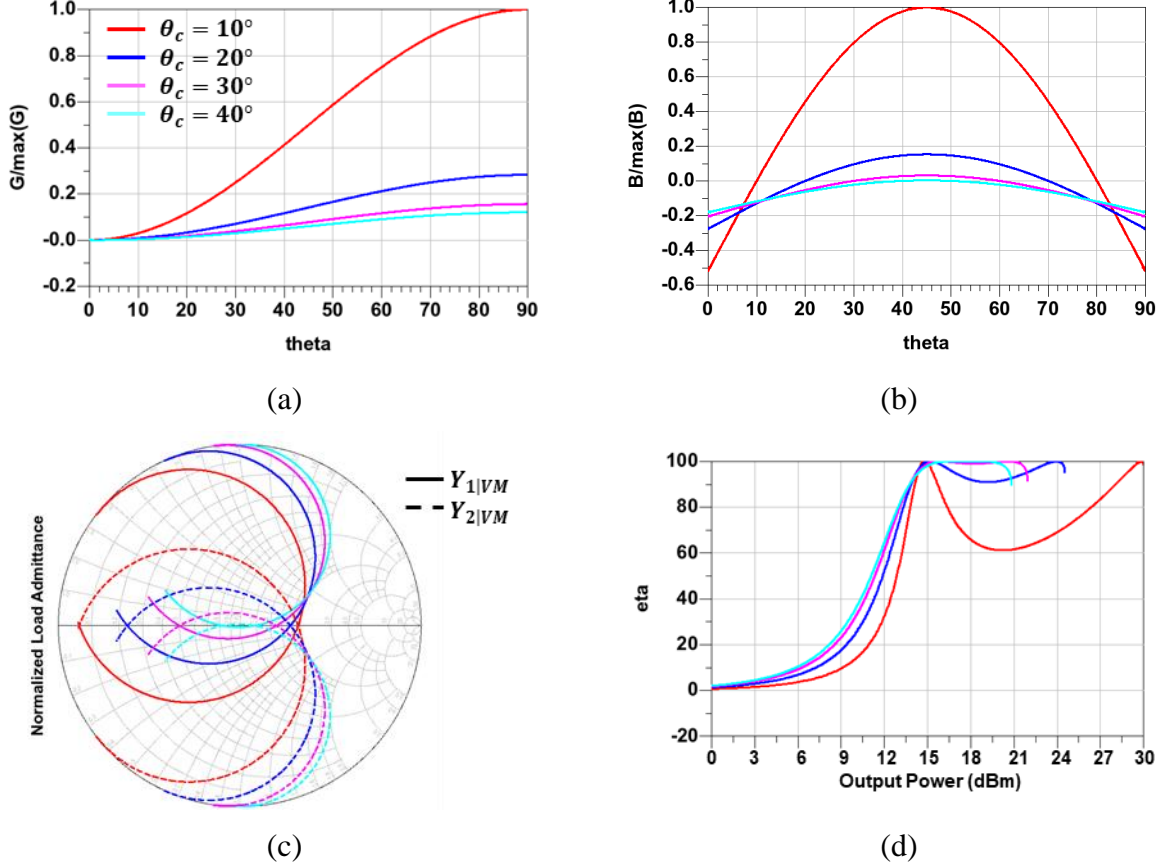


Figure 3.11 – (a) Normalized Conductance and (b) Susceptance. (c) Normalized load admittance trajectories. (d) Efficiency with respect to output power for different values of θ_c

However, a solution is provided in the proposed design method that will be discussed in *section 1.4.1*. Finally, the load voltage is obtained by the expression in (3.24).

$$V_{L|VM} = \frac{2 \cdot V_{max}}{\sin(2 \cdot \theta_c)} \cdot \sin(\theta) \quad (3.24)$$

As pointed out in *section 1.3*, in the case of current-mode operation, the impedance is better suited than the admittance. It can be calculated using (3.25).

$$\mathbf{Z}_{1|CM} = R_L \cdot [2 \cdot \cos^2(\theta) - j \cdot (\sin(2 \cdot \theta) - \sin(2 \cdot \theta_c))] \quad (3.25)$$

The input current amplitude I_m is then determined through (3.25) and (3.14) and results in the plot of Figure 3.12(a). The load modulation trajectories of the input impedances, normalized with respect to the load resistance value R_L , can be seen in Figure 3.12(b). The output power, as defined in (3.7) can be calculated using the load conductance which can be found using (3.26) and is plotted in Figure 3.12(c). Once again, the maximum value of the conductance, and consequently the output power, is seen to be dependent on the compensation angle θ_c . Furthermore, the maximum conductance (or power) no longer occurs at $\theta = 90^\circ$ but instead is also dependent on θ_c .

$$G = \Re \left[\frac{1}{Z_{CM}} \right] \quad (3.26)$$

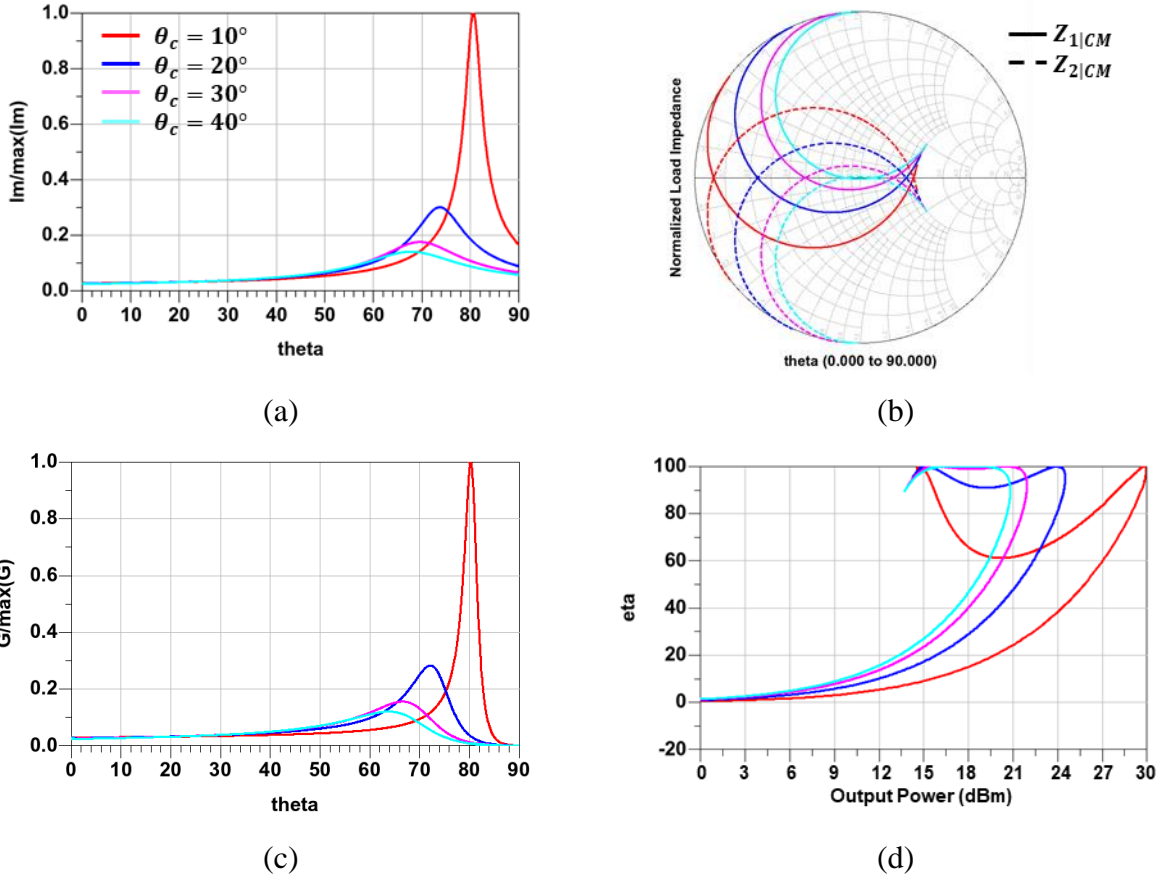


Figure 3.12 – (a) Input current amplitude evolution with respect to θ for different values of θ_c , (b) Normalized input impedances, (c) Normalized load conductance, (d) Efficiency with respect to output power.

The efficiency can be calculated using (3.8) which can be transformed into (3.27) and used to plot the profiles of Figure 3.12(d).

$$\eta = \eta_{max} \cdot \frac{\Re[Z_{CM}]}{|Z_{CM}|} \quad (3.27)$$

The efficiency profiles here differ from those in voltage-mode operation and seem to be phase-shifted. This is because of the variation of the input current amplitude I_m and can be solved by changing the Outphasing angle variation interval from $[0^\circ; 90^\circ]$ to $[90^\circ; \theta_{stop}]$ where θ_{stop} is the Outphasing angle that corresponds to the maximum conductance (or power) and can be calculated using (3.28).

$$\theta_{stop} = -j \cdot \ln \left(\frac{\sqrt{1 + e^{j.8.\theta_c} - 18. e^{j.4.\theta_c}}}{4. e^{j.2.\theta_c} + e^{j.4.\theta_c} - 1} \right) \quad (3.28)$$

Figure 3.13(a) plots the evolution of θ_{stop} with respect to θ_c . Plotting the efficiency using the new Outphasing angle interval, results in Figure 3.13(b) which shows the same evolutions as the voltage-mode operation of Figure 3.11(d).

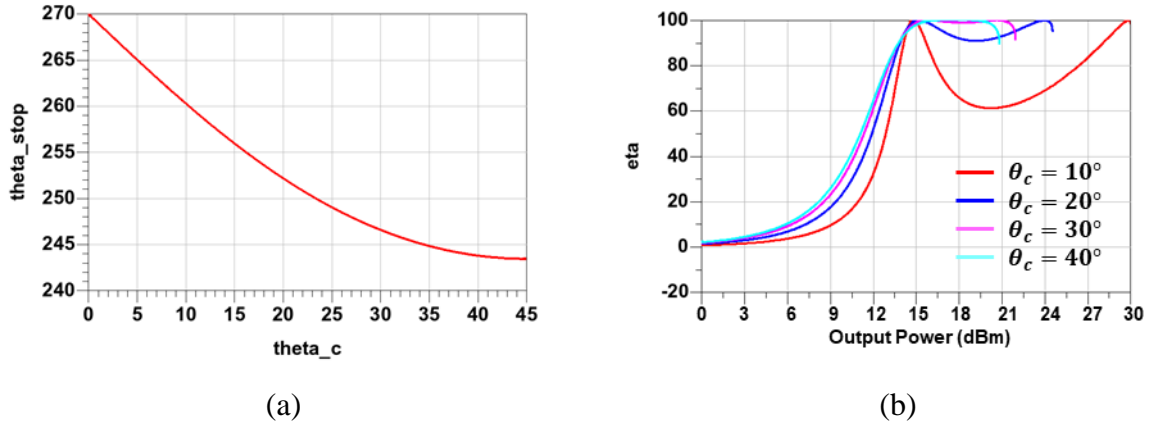


Figure 3.13 – (a) Maximum Outphasing angle θ_{stop} with respect to compensation angle variation. (b) Efficiency with respect to output power.

Finally, the current-mode expression of the load voltage is determined by:

$$V_{L|CM} = -2 \cdot I_0 \cdot R_L \cdot \cos(\theta) \quad (3.29)$$

It can be noticed that in current-mode, the phase variation interval is greater than the one required for voltage-mode operation. Moreover, the OPA becomes extremely sensitive to phase variation at higher power (as can be concluded by examining the slopes of the different curves in Figure 3.12 (c)). Due to these challenges, voltage-mode operation is generally privileged as it provides the same efficiency characteristics but without sensitivity issues.

The reactive compensation current combiner has the particularity of being the most compact of the studied structures. As a result, it is an attractive option for integrated circuits where occupied area must be minimized [51], [52]. However, this architecture presents a peak power that is dependent on the compensation angle both in voltage and current-mode. This can be troublesome when designing a combiner, as the peak power is usually taken as a starting point for the PA design process. The next paragraph shows how this issue can be circumvented by presenting a unified design method.

1.4.1 Unified Outphasing Combiner Design Methodology

In this section, a novel Outphasing combiner design method is discussed. The main interest of the presented method lies in the formalization of the different design approaches existing in the literature. It provides a unified framework which covers all four combiners seen so far and presented again in Figure 3.14 below.

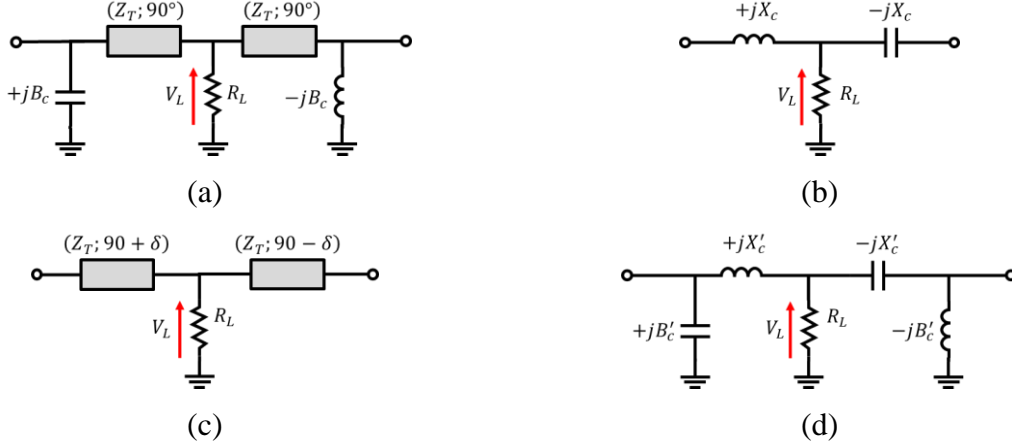


Figure 3.14 – (a) Reactive compensation voltage combiner (RCV) (b) Reactive compensation current combiner (RCC) (c) Delay-line compensation voltage combiner (DCV) (d) Delay-line compensation current combiner (DCC).

Important parameters in PA design are the saturated power P_{max} (PA total output power), the maximum output voltage swing V_0 , and the output power back-off level OBO (expressed in dB). First, the optimal load resistance R_{opt} and compensation angle θ_c are calculated using

$$R_{opt} = \frac{2 \cdot V_0^2}{P_{max}} \quad (3.30)$$

$$\theta_c = \sin^{-1} \left(10^{-\frac{OBO}{20}} \right) \quad (3.31)$$

One of the main problems revealed by the RCC combiner analysis in the previous section was the dependence of the maximum output power on the compensation angle. This issue is expressed in (3.32) which states that for any compensation angle value θ_c , the maximum conductance (and therefore power) must be equal to a constant k . In order to simplify the subsequent design process, the value of k is set as the maximum conductance for $\theta_c = \frac{\pi}{4}$.

Moreover, the input susceptance must be equal to zero when $\theta = \theta_c$ as expressed in (3.33).

$$\max \left[\Re \left[\mathbf{Y} \left(\theta, \theta_c = \frac{\pi}{4} \right) \right] \right] = k \quad (3.32)$$

$$\Im[\mathbf{Y}(\theta = \theta_c)] = 0 \quad (3.33)$$

Solving the system for the conditions above leads to the design equations in Table 3.1. The first condition gives the appropriate load impedance expression for the different combiner

architectures depending on the targeted compensation angle or back-off efficiency. Meanwhile, the second condition results in the expressions for the reactive compensation elements.

Table 3.1 – Combiner design expressions.

	Reactive Compensation Voltage Combiner	Delay-Line Compensation Voltage Combiner	Reactive Compensation Current Combiner	Delay-Line Compensation Current Combiner
R_L	$\frac{R_{opt}}{2}$	$\frac{R_{opt}}{4 \cdot \cos^2(\theta_c)}$	$\frac{R_{opt}}{\sin^2(2 \cdot \theta_c)}$	$\frac{R_{opt}}{4 \cdot \sin^2(\theta_c)}$
Z_T	$R_L \cdot \sqrt{2}$	$2 \cdot R_L$	–	$2 \cdot R_L$
X_c	–	–	$R_L \cdot \sin(2 \cdot \theta_c)$	$2 \cdot R_L \cdot \sin(\theta_c)$
B_c	$\frac{\sin(2 \cdot \theta_c)}{2 \cdot R_L}$	–	–	$\frac{1 - \cos(\theta_c)}{2 \cdot R_L \cdot \sin(\theta_c)}$

The delay-line mismatch δ of Figure 3.14(c) (and the transmission-line form of Figure 3.14(d)), can be calculated using (3.34) which shows that when Z_T is set to the value given in Table 3.1, δ becomes equal to θ_c .

$$\begin{aligned} \delta &= \frac{1}{2} \cdot \sin^{-1} \left(\frac{2 \cdot R_L}{Z_T} \cdot \sin(2 \cdot \theta_c) \right) \\ &= \theta_c \end{aligned} \quad (3.34)$$

In voltage-mode operation, the voltage combiners have the same admittance expression shown in (3.35), as do the current combiners whose admittance is calculated in (3.36).

$$Y_{1|VM|VC} = \frac{1}{R_{opt}} \cdot [2 \cdot \cos^2(\theta) - j \cdot (\sin(2 \cdot \theta) - \sin(2 \cdot \theta_c))] \quad (3.35)$$

$$Y_{1|VM|CC} = \frac{1}{R_{opt}} \cdot [2 \cdot \sin^2(\theta) + j \cdot (\sin(2 \cdot \theta) - \sin(2 \cdot \theta_c))] \quad (3.36)$$

The admittance equations show that the conductance of both the voltage combiners and current combiners is no longer dependent on the compensation angle θ_c .

To better illustrate this, an RCC combiner is designed to provide a peak output power of 33dBm ($P_{max} = 2W$) for different values of output back-off. The simulation results in Figure 3.15 show that the conductance is not affected by the choice of OBO.

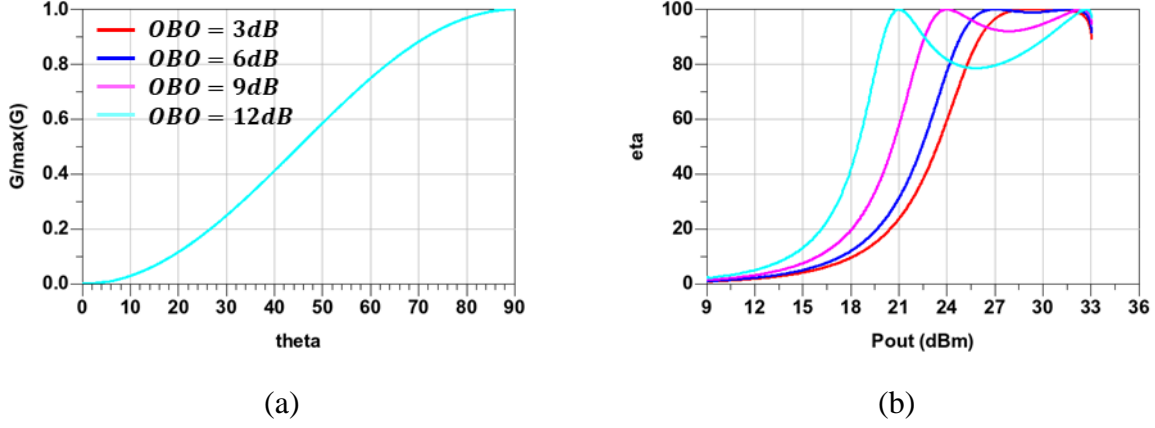


Figure 3.15 – (a) Normalized load conductance and (b) Efficiency with respect to output power for different targeted OBO in voltage-mode operation.

The proposed design method is also applicable to current-mode operation. The input impedances can be derived and simplified to (3.37) and (3.38) for voltage and current combiners respectively.

$$\mathbf{Z}_{1|CM|VC} = \frac{R_{opt}}{\sin^2(2\theta_c)} \cdot [2 \cdot \sin^2(\theta) + j \cdot (\sin(2\theta) - \sin(2\theta_c))] \quad (3.37)$$

$$\mathbf{Z}_{1|CM|CC} = \frac{R_{opt}}{\sin^2(2\theta_c)} \cdot [2 \cdot \cos^2(\theta) - j \cdot (\sin(2\theta) - \sin(2\theta_c))] \quad (3.38)$$

The designed RCC combiner is now simulated in current-mode using the correct Outphasing angle interval for each OBO value. The normalized input current amplitude is shown in Figure 3.16(a). The load conductance, plotted in Figure 3.16(b) reveals that the maximum conductance G is the same for all plots. Finally, current-mode operation results in the same efficiency curves as Figure 3.15(b).

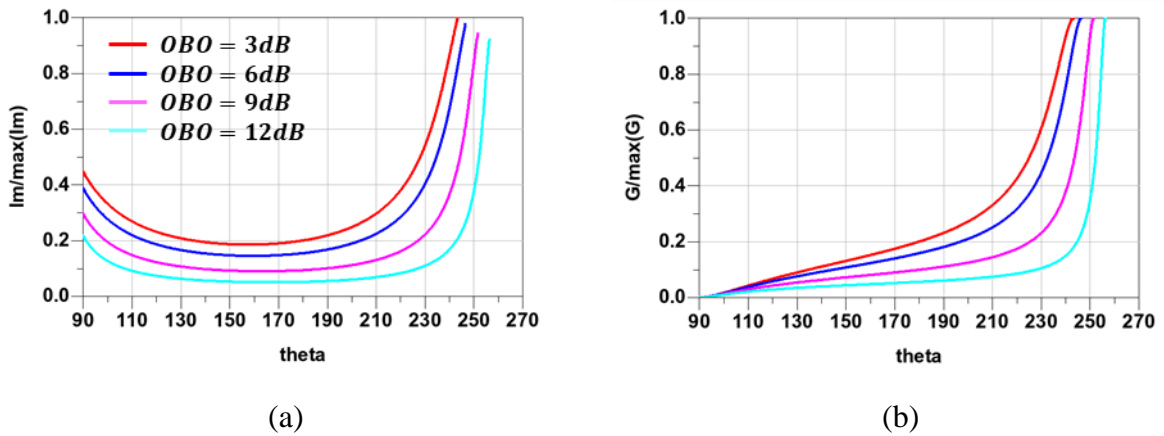


Figure 3.16 – (a) Normalized current amplitude and (b) load conductance for different values of OBO in current-mode operation.

The proposed design methodology results in an OPA design that delivers the targeted output power, regardless of the compensation angle and mode of operation for all four combiners. The choice of combiner architecture then depends on the targeted application, the different architectures providing the same load modulation for a given mode of operation.

2 Doherty PA Combiners

The Doherty PA (DPA) is the most prevalent load modulation architecture in the literature. Indeed, since its inception in 1936 and re-emergence in the late 80s, the DPA architecture has evolved significantly while keeping its core principle: Amplification is achieved by using two amplifiers. In the low power region, the main amplifier operates alone until its saturation at the back-off (BO) point. Beyond that point, the auxiliary amplifier starts injecting current into the same load thus increasing the overall output power until it reaches the peak point. This second phase is referred to as the Doherty region. Of the aforementioned DPA evolutions, the power combiner was originally designed using an impedance inverter transmission line on the main amplifier branch connected to the auxiliary branch and load impedance as shown in Figure 3.17.

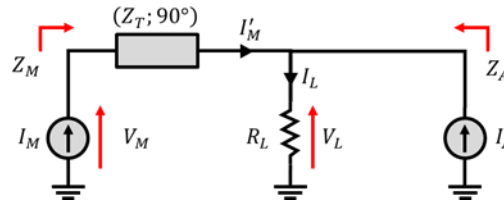


Figure 3.17 – Simplified current-mode representation of the DPA architecture.

Today, using the work done by Özen in [53], a DPA power combiner architecture can be synthesized using a set of initial boundary conditions on the two critical operating points that define Doherty operation (i.e. Peak and BO). In this approach, the drain current and voltage of the two branches are set at peak power and back-off, and then used to determine the required two-port Z-matrix (Figure 3.18(a)) satisfying these conditions by solving the equation in (3.39).

$$\begin{pmatrix} V_{1|Peak} & V_{1|BO} \\ V_{2|Peak} & V_{2|BO} \end{pmatrix} = (Z) \times \begin{pmatrix} I_{1|Peak} & I_{1|BO} \\ I_{2|Peak} & I_{2|BO} \end{pmatrix} \quad (3.39)$$

Once determined, the Z-matrix is used to synthesize the combiner after transformation into a lossless 3-port network connected to a resistive load R_L as shown in Figure 3.18(b).

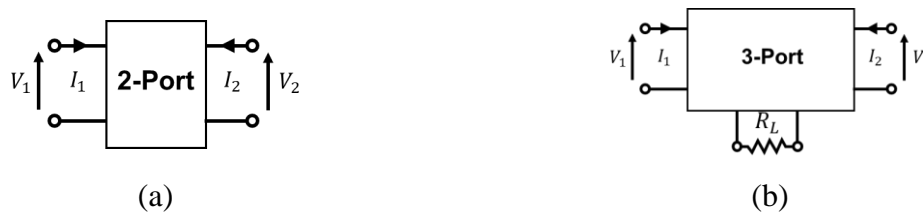


Figure 3.18 – (a) Lossy two-port representation of the black-box method, (b) Lossless three-port representation of the black-box method.

This solution was complemented by other works [54], [55] which propose a load modulation continuum theory that positions Doherty and Outphasing as part of a larger set of solutions, defined by their boundary conditions on the Peak and BO operation points.

The work presented in [56] takes this a step further by proposing a generalized Doherty-Outphasing continuum where DPA and OPA operation are but singular cases of a larger design space, defined by their boundary conditions. This allows additional degrees of freedom, as more variables are introduced into the design space, leading to the *Hybrid Chireix Doherty* (HCD) operation.

This approach, while advantageous in many aspects, does however present a setback. As the synthesis of the combiner is determined solely by the two aforementioned operation points, there is no guarantee that the main branch will maintain constant voltage in-between these states. Consequently, the overall output power and efficiency can drop in some cases while respecting the Doherty conditions at the peak and BO points.

This problem extends to the analysis approach for combiner design as well. In [57], the authors analyse a compact combiner architecture and determine that it can be used for DPA operation at 3dB back-off. The analysis is conducted only on the two critical points and as a result, the main branch voltage decreases between the BO and peak points (Doherty-like operation instead of Doherty).

In the following section, a new combiner analysis method for DPA design, capable of respecting the current and voltage requirements throughout the entire Doherty region, is presented. The current and voltage conditions between the Peak and BO powers are taken into account and the optimal current driving profiles are derived. This method is then used on the compact L-C combiner to demonstrate that with an optimized drive profile, this combiner can operate up to 7.2dB back-off unlike in [57] where Doherty operation is achieved over 3dB back-off.

2.1 DPA Combiner Analysis

Using the classic impedance inverter-based DPA as a reference, a set of four conditions can be defined for ideal DPA operation.

- i. In low power region, the Auxiliary PA does not contribute to the overall output power.
- ii. The main PA is saturated all over the Doherty region
- iii. The auxiliary amplifier reaches its saturation when the peak overall output power is achieved.
- iv. In the Doherty region, the power combination of the two paths is additive. In addition, the power per branch is required to be strictly incremental.

As in [53], the critical operation points are defined as the peak output power ($P_{O|P}$) and the back-off output power ($P_{O|B}$). The ratio between the two power levels is the peak to back-off power ratio and is denoted using ζ .

$$\zeta = \frac{P_{O|P}}{P_{O|B}} \quad (3.40)$$

These conditions are then tested against a given combiner architecture in order to verify its compatibility with Doherty operation and derive optimized current profiles.

The DPA combiner can be represented a cascade of two-port networks and represented using its equivalent ABCD matrix.

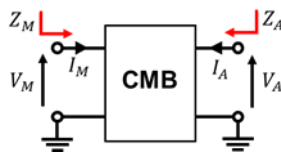


Figure 3.19 – Cascaded two-port network representation of the reactive compensation current combiner for DPA operation.

Using the schematic of Figure 3.19, the current and voltage relations can be expressed as follows:

$$\begin{pmatrix} V_M \\ I_M \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \times \begin{pmatrix} V_A \\ -I_A \end{pmatrix} \quad (3.41)$$

The complex auxiliary to main current ratio is represented using amplitude γ_I and phase ϕ .

$$\frac{I_A}{I_M} = \left| \frac{I_A}{I_M} \right| \cdot e^{j\phi} = \gamma_I \cdot e^{j\phi} \quad (3.42)$$

The main and auxiliary input impedances can therefore be derived:

$$Z_M = \frac{1}{C} \cdot (A + \gamma_I \cdot e^{j\phi}) \quad (3.43)$$

$$Z_A = \frac{1}{C} \cdot \left(D + \frac{1}{\gamma_I} \cdot e^{-j\phi} \right) \quad (3.44)$$

As stated in condition (i), the auxiliary provides no current at $P_{O|B}$ (i.e., $I_{A|B} = 0$) and therefore, only the main branch contributes to the overall output power.

$$P_{O|B} = \frac{1}{2} \cdot \Re[Z_{M|B}] \cdot I_{M|B}^2 \quad (3.45)$$

Where $Z_{M|B}$ is the main input impedance at $P_{O|B}$ defined by:

$$Z_{M|B} = \frac{A}{C} \quad (3.46)$$

The main current amplitude at back-off $I_{M|B}$ can therefore be calculated as follows:

$$I_{M|B} = \sqrt{\frac{2 \cdot P_{O|B}}{\zeta \cdot \Re[Z_{M|B}]}} \quad (3.47)$$

At peak output power, both branches contribute to the overall output power. This can be expressed using (3.48).

$$P_{O|P} = \frac{1}{2} \cdot (\Re[Z_{M|P}] \cdot I_{M|P}^2 + \Re[Z_{A|P}] \cdot I_{A|P}^2) \quad (3.48)$$

Condition (ii) states that the main voltage amplitude must remain constant throughout the Doherty region. In other words, this condition is only considered at the peak and back-off points which can result in unwanted behaviour within the Doherty region. The key difference between the proposed method and the standard approach [55], [56], is the verification of this voltage condition throughout the Doherty region using the expressions below:

$$\text{for } P \in [P_{O|B}; P_{O|P}], \quad |V_M| = |Z_M \cdot I_M| = |Z_{M|B}| \cdot I_{M|B} \quad (3.49)$$

$$= |Z_{M|P}| \cdot I_{M|P} \quad (3.50)$$

Starting with (3.48), $P_{O|P}$ is replaced with its equivalent expression derived from (3.47). The same is done for $I_{M|B}$ using (3.49) and (3.50) which results in the equation below.

$$\frac{\Re[Z_{M|B}]}{|Z_{M|B}|^2} \cdot \zeta \cdot |Z_{M|P}|^2 - \Re[Z_{M|P}] - \Re[Z_{A|P}] \cdot \gamma_{I|P}^2 = 0 \quad (3.51)$$

As can be seen in (3.43) and (3.44), both $Z_{M|P}$ and $Z_{A|P}$ are functions of $\gamma_{I|P}$, meaning that (3.51) can be rewritten as a quadratic function of $\gamma_{I|P}$ with real coefficients:

$$a(\zeta, \phi) \cdot \gamma_{I|P}^2 + b(\zeta, \phi) \cdot \gamma_{I|P} + c(\zeta, \phi) = 0 \quad (3.52)$$

$\gamma_{I|P}$ is the ratio of two amplitudes, and as a result its value must be both positive and real. For a given value of ϕ , the discriminant of (3.52), Δ_γ , is positive for a range of ζ values, the highest of which, ζ_{max} , represents the maximum theoretical back-off achievable in DPA operation using the chosen combiner architecture and current phase difference ϕ .

$$\gamma_{I|P} = \frac{-b(\zeta, \phi) \pm \sqrt{\Delta_\gamma}}{a(\zeta, \phi)} \quad (3.53)$$

Once ζ is set, the root values of $\gamma_{I|P}$ can be calculated and subsequently used to determine $I_{A|P}$ using (3.49) and (3.50):

$$I_{A|P} = \frac{|Z_{M|B}|}{|Z_{M|P}|} \cdot I_{M|B} \cdot \gamma_{I|P} \quad (3.54)$$

The main current amplitude at peak is calculated using

$$I_{M|P} = \frac{I_{A|P}}{\gamma_{I|P}} \quad (3.55)$$

With the current values calculated at both peak and back-off power levels, the trajectory between these points must be determined. The auxiliary current is null in the low power region and starts to increase in the Doherty region. Assuming a linear evolution of the current amplitude, its drive profile can be defined as:

$$I_A = \begin{cases} 0 & \text{for } 0 \leq \alpha \leq \alpha_b \\ I_{A|P} \cdot \frac{(\alpha - \alpha_b)}{1 - \alpha_b} \cdot e^{j\phi} & \text{for } \alpha_b \leq \alpha \leq 1 \end{cases} \quad (3.56)$$

Where α and α_b are normalized power values defined as:

$$\alpha = \sqrt{\frac{P_O}{P_{O|P}}} \quad (3.57)$$

$$\alpha_b = \sqrt{\frac{1}{\zeta}} \quad (3.58)$$

In the low power region, the main current can be assumed to follow a linear increase as well, however, throughout the Doherty region, the voltage condition must be kept, and as a result, the evolution of the main current must be derived from (3.49) by rewriting it as a function of $|I_A|$ and $|I_M|$ and solving for $|I_M|$. The main input drive profile can therefore be written as:

$$I_M = \begin{cases} I_{M|B} \cdot \frac{\alpha}{\alpha_b} & \text{for } 0 \leq \alpha \leq \alpha_b \\ f(|I_A|) & \text{for } \alpha_b \leq \alpha \leq 1 \end{cases} \quad (3.59)$$

Using the voltage condition, it is possible to extract the drive profile for the main current amplitude in the Doherty region. To the authors' best knowledge, this type of approach has not yet been attempted in the literature, as the drive profile is usually assumed to keep its linear evolution.

Ideal Doherty operation is achieved when all of the previously listed conditions are met. Conditions (i) and (ii) are used to derive the current profiles and as a result are considered validated. Meanwhile, condition (iii) is satisfied when:

$$|V_{A|P}| = \max[|V_A|] \quad (3.60)$$

Finally, condition (iv) which requires the power combination to be additive is verified if the total output power P_O is always increasing with respect to input power.

This new analysis method is now used to evaluate the reactive compensation current combiner, which was selected for OPA operation for its compact size.

2.1.1 Reactive Compensation Current Combiner for DPA Operation

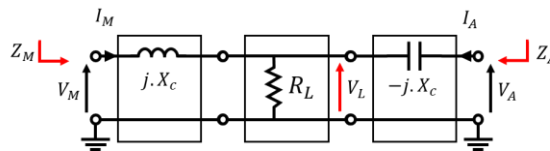


Figure 3.20 – Cascaded two-port network representation of the reactive compensation current combiner for DPA operation.

The compact combiner architecture used in [42], [57] is a special case of the reactive compensation current combiner (RCC) used for Outphasing operation with a compensation angle $\theta_c = 45^\circ$. The reactive component values can therefore be calculated using (3.22) resulting in:

$$X_c = R_L \quad (3.61)$$

Going back to the equivalent ABCD matrix given in (3.21), the input impedances can be found using (3.43) and (3.44) as shown below.

$$\mathbf{Z}_M = R_L + j \cdot R_L + R_L \cdot \gamma_I \cdot e^{j\phi} \quad (3.62)$$

$$\mathbf{Z}_A = R_L - j \cdot R_L + \frac{R_L}{\gamma_I} \cdot e^{-j\phi} \quad (3.63)$$

The main branch current amplitude at back-off, whose expression is given in (3.47), becomes:

$$I_{M|B} = \sqrt{\frac{2 \cdot P_{O|P}}{\zeta \cdot R_L}} \quad (3.64)$$

The second order polynomial coefficients of (3.52) are calculated below:

$$a(\zeta, \phi) = \frac{\zeta}{2} - 1 \quad (3.65)$$

$$b(\zeta, \phi) = \zeta \cdot \sin \phi + (\zeta - 2) \cdot \cos \phi \quad (3.66)$$

$$c(\zeta, \phi) = \zeta - 1 \quad (3.67)$$

Using the discriminant condition shown in (3.68), the maximum theoretical back-off ζ_{max} can be determined for different values of ϕ through (3.69).

$$\Delta_\gamma = \zeta^2 \cdot (\sin(2 \cdot \phi) - 1) - 2 \cdot \zeta \cdot (2 \cdot \cos^2 \phi + \sin(2 \cdot \phi) - 3) - 4 \cdot \sin^2 \phi \geq 0 \quad (3.68)$$

$$\zeta_{max} = \frac{\sqrt{2} \cdot \sin\left(2 \cdot \phi + \frac{\pi}{4}\right) - 2 - \sqrt{3 - 2 \cdot \sqrt{2} \cdot \sin\left(2 \cdot \phi + \frac{\pi}{4}\right)}}{\sin(2 \cdot \phi) - 1} \quad (3.69)$$

For a given value of ϕ , the achievable back-off levels are bounded by ζ_{max} . However, this does not guarantee that all the back-off levels $\zeta < \zeta_{max}$ are achievable, as there are other conditions that must be satisfied as well.

The $\gamma_{I|P}$ roots extracted from (3.52) can be calculated using (3.70)

$$\gamma_{I|P} = \frac{-\zeta \cdot \sin \phi - (\zeta - 2) \cdot \cos \phi \pm \sqrt{\Delta_\gamma}}{\zeta - 2} \quad (3.70)$$

As γ_{IP} is the ratio of two amplitudes, only real, positive roots are retained. This restricts the possible values of ϕ to the range of $[-90^\circ; 0^\circ]$.

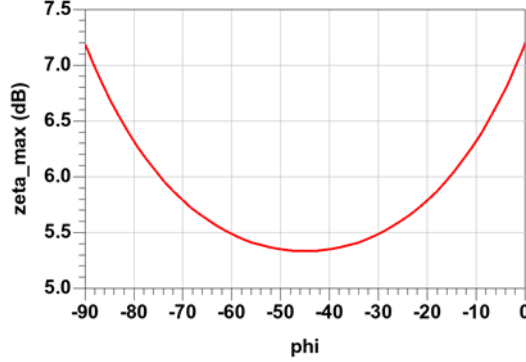


Figure 3.21 – Maximum theoretical back-off value ζ_{max} with respect to ϕ .

Figure 3.21 plots the values of ζ_{max} with respect to ϕ . The compact RCC combiner is shown to be capable of a maximum back-off value $\zeta_{max} = 7.12dB$ when $\phi = \{-90^\circ; 0^\circ\}$. The peak auxiliary current amplitude can now be calculated using (3.54) which results in (3.71).

$$I_{A|P} = I_{M|B} \cdot \gamma_{IP} \cdot \sqrt{\frac{2}{\gamma_{IP}^2 + 2 \cdot \gamma_{IP} \cdot (\sin \phi + \cos \phi) + 2}} \quad (3.71)$$

Finally, as previously stated, the main current amplitude in the Doherty region can be expressed by solving (3.49) which results in the expression below.

$$|I_M| = \frac{-|I_A| \cdot (\sin \phi + \cos \phi) \pm \sqrt{|I_A|^2 \cdot (\sin(2 \cdot \phi) - 1) + 4 \cdot I_{M|B}^2}}{2} \quad (3.72)$$

Each of the two roots found in (3.72) corresponds to one of the two roots of γ_{IP} that were previously calculated. Only the $|I_M|$ expression (and corresponding γ_{IP} root) that results in real positive value for any $\alpha \in [\alpha_b; 1]$ is retained.

Using this method, it can be shown that the compact combiner can operate under Doherty conditions for different back-off levels as well as phase difference values. The plots of Figure 3.22(a) show the main and auxiliary input current profiles required to achieve a back-off of $\zeta = 5dB$ for different values of phase offset ϕ . The main voltage amplitude is seen to remain constant throughout the Doherty region in Figure 3.22(b). Lastly, the load modulation seen by each branch can be visualized in Figure 3.22(c) and Figure 3.22(d).

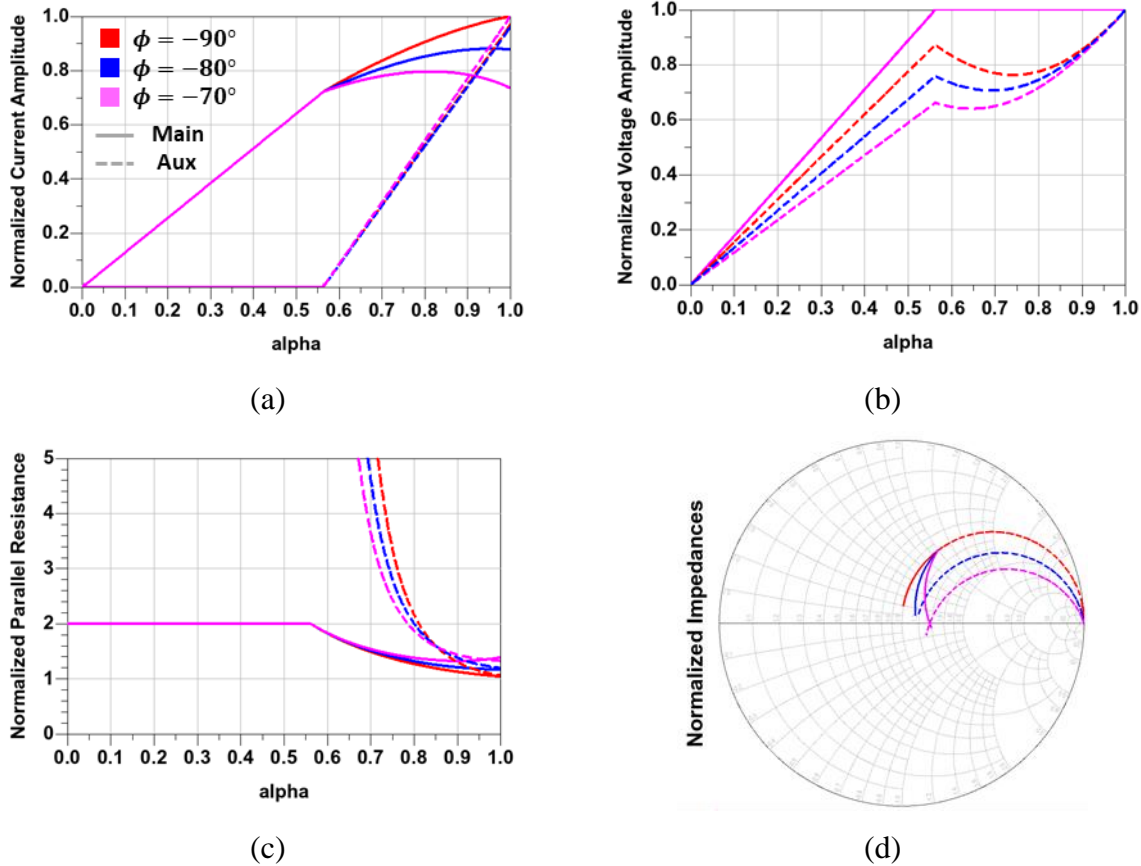


Figure 3.22 – Main and auxiliary normalized (a) current amplitude, (b) voltage amplitude, (c) parallel load resistance, and (d) impedance for different values of ϕ at $\zeta = 5\text{dB}$.

Finally, the efficiency of the DPA combiner must be analysed. The ideal efficiency of the DPA circuit using the selected combiner can be calculated through:

$$\eta = \eta_M \cdot \eta_A \cdot \frac{P_M + P_A}{P_M \cdot \eta_A + P_A \cdot \eta_M} \quad (3.73)$$

Where P_M and P_A represent the output power contribution of the main and auxiliary branches respectively, and are calculated using (3.74), while η_M and η_A represent the power efficiency of each branch and can be found using (3.75).

$$P_k = \frac{1}{2} \cdot \Re[\mathbf{Z}_k] \cdot |\mathbf{I}_k|^2 \quad (3.74)$$

$$\eta_k = \eta_{\max|k} \cdot \frac{|\mathbf{V}_k|}{\max[|\mathbf{V}_k|]} \quad (3.75)$$

$\eta_{\max|k}$ is the maximum theoretical efficiency value for the class of operation of each power cell. The DPA efficiency is plotted against the normalized output power expressed in dB in Figure 3.23(a) for the different values of ϕ used above. It can be seen that all three plots respect the 5dB back-off and present two efficiency peaks. Moreover, the efficiency curve obtained when $\phi = -90^\circ$ results in the highest average efficiency and should therefore be favoured.

Using this value of ϕ , the combiner can be operated at different levels of back-off going up to 7dB as shown in Figure 3.23(b).

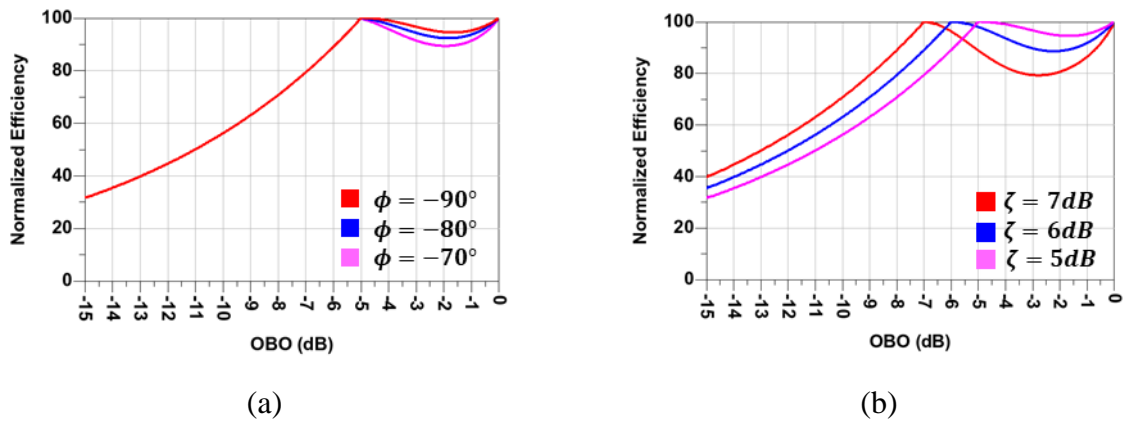


Figure 3.23 – DPA combiner efficiency versus normalized output power for (a) different values of ϕ at $\zeta = 5\text{dB}$ and (b) different levels of ζ at $\phi = -90^\circ$.

Through this study, it can be determined that the compact combiner is capable of ideal Doherty operation with back-off levels up to 7dB. Furthermore, its compactness makes it the ideal choice for an integrated DPA design.

3 Conclusion

In this chapter, the main load modulation PA architectures for back-off efficiency enhancement were discussed and analysed. The Outphasing PA architecture is first explored through the classic Chireix combiner. It is shown that most of the Outphasing combiners used today can be obtained by applying circuit transformations to the original Chireix combiner. Through these transformations, a new combiner is proposed, completing the set of dual voltage and current combiners. Both voltage and current-mode Outphasing are explained and shown to be compatible with all of the analysed voltage and current combiners. With the exception of the classic Chireix combiner, all the other combiners have a peak output power that is dependent on the targeted output back-off level. A new design method is proposed which unifies the combiner design for both voltage and current mode operation and ensures a given peak power regardless of the targeted back-off level.

Next a set of Doherty PA operation conditions were proposed and used as the basis of a new combiner analysis method. Current combiner synthesis and analysis methods focus solely on the two bordering points of the Doherty region (Peak and BO) which in consequence puts no conditions on the operation points in-between these two and can result in unwanted behaviour. The proposed method takes into account the entirety of the Doherty region and ensures that the current and voltage conditions are respected at all points of operation. Using this approach, the compact combiner used in [57] is proven to be capable of Doherty operation with up to 7dB of back-off (up to 4dB from the initial analysis of the authors).

The compact reactive compensation current combiner architecture is found to be the ideal choice for PA integration, given its limited number of components and compatibility with both OPA and DPA operation.

Chapter 4. SOI-CMOS Class-E Doherty PA

1	Doherty PA Design	69
1.1	Power Stage Design	70
1.2	Driver Stage Design.....	76
1.3	Inter-Stage Matching Network Design	77
1.4	Two-Stage DPA Line-Up and Simulation	78
2	Integration Technology	83
2.1	SOI-CMOS Technology	83
2.2	Package Substrate Technology	88
2.3	PCB Technology	90
3	Circuit Implementation and Measurement	91
3.1	Layout	91
3.2	Validation.....	94
3.3	CW and LTE Performance	96
4	Conclusion.....	99

Load modulated PA architectures have two major features: the combiner which was discussed at length in the previous chapter and the power stage. For high efficiency PA operation in back-off, an optimal load impedance must be presented to the PA devices as a function of the output power. Moreover, the transistors must be correctly biased and driven so as to maintain stable, high efficiency operation.

In order to validate the newly proposed DPA combiner analysis technique, a SOI-CMOS class-E Doherty power amplifier is designed, fabricated and measured.

First, the design process begins with the DPA power stage design considering the compact LC combiner. The power stage is then integrated into a two-stage DPA design which is tuned until the desired performance is achieved.

Next, the different integration technologies considered in this work are exposed. The SOI-CMOS, package and circuit board technologies are presented along with their main characteristics.

Finally, the proposed circuit is implemented and fabricated before being tested with both continuous wave (CW) and modulated LTE signals.

1 Doherty PA Design

This section details the design process of the proposed two-stage class-E Doherty PA used to validate the proposed combiner design analysis.

The PA targets mobile applications, and as a result, the supply voltage is limited to $3.4V$. The design frequency is set to $2.5GHz$ to target the mid-band. The target DPA circuit performance is summed up in Table 4.1 below.

Table 4.1 – DPA target performance

CW	Peak Power	33 dBm
	Gain	24 dB
	Peak PAE	>50%
	PAE at 6dB BO	>42%
Modulated Signal	Standard	LTE
	Signal Bandwidth	10 MHz
	Modulation	QPSK LTE
	Average PAE	>40%
	ACLR	<-35 dBc

A typical two-stage DPA architecture is shown in Figure 4.1. It consists in two active blocks, namely the power stage (PWR) and the driver stage (DRV), along with three matching networks at the output (OMN), input (IMN), and inter-stage (ISMN). Since a Doherty architecture is considered, a power divider (integrated in the ISMN) and a power combiner (CMB) are also considered.

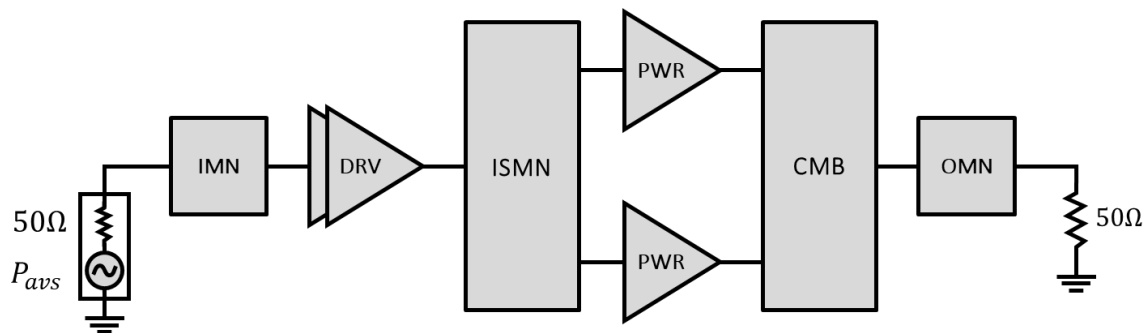


Figure 4.1 – Two-stage DPA block diagram.

The first stage (driver) of the PA is followed by a power divider, which offers the best compromise between efficiency and linearity as demonstrated in [58].

The DPA design process is split into two steps. First, a single-stage dual-input Doherty PA consisting of the PWR, CMB, and OMN stages is designed. Once the power stage is optimized in terms of efficiency and output power, the driver stage and ISMN are added and the overall two-stage DPA is tuned to provide optimized performance.

1.1 Power Stage Design

The compact reactive compensation current combiner architecture studied in *Chapter 3 section 2.1.1*, is selected and designed to provide an overall output power of 33dBm. The values of the combiner elements are shown in Figure 4.2(a). Next, the class-E power cells are designed. An electrical LDMOS transistor model is used and the class-E PA is designed using the K-set method presented in *Chapter 2 section 2.3*. Due to the ON-resistance of the transistor, the PA cell must be oversized by a factor of two. The class-E PA is designed at $f_0 = 2.5\text{GHz}$, with a supply voltage of $V_{DD} = 3.4\text{V}$, and a target peak power $P_{sat} = 33\text{dBm}$ considering the q factor as a free design variable.

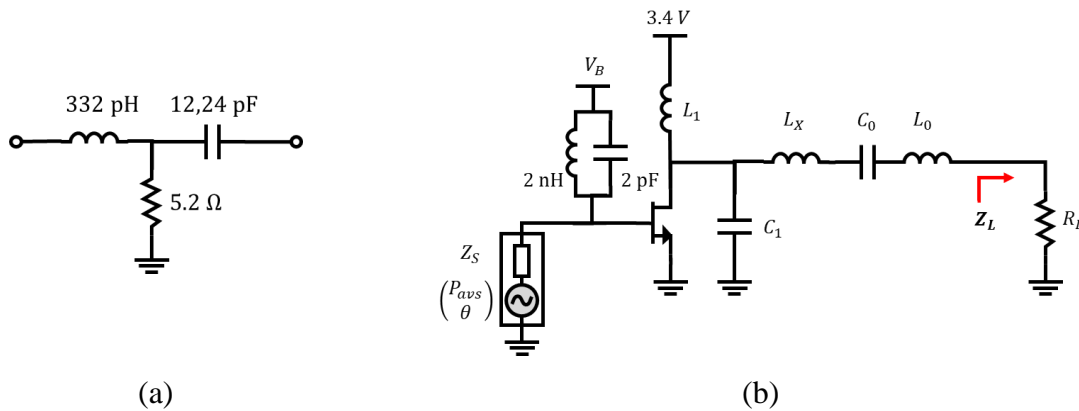


Figure 4.2 – (a) Reactive compensation current combiner, (b) Class-E power cell schematic.

As shown in Figure 4.2(b), a single-tone input signal is chosen instead of the typical square-wave and a parallel LC tank tuned to f_0 is used as a biasing circuit at the gate of the transistor. The value of the bias voltage is different for each of the two power cells, so as to achieve Main/Auxiliary Doherty behaviour. The quality factors of the capacitors and inductors are $Q_C = 90$ and $Q_L = 40$ respectively.

The source impedance Z_s is first conjugately matched to the input impedance of the transistor, and then tuned in order to optimize efficiency and output power.

The choice of q is determined through load pull simulations: The main and auxiliary class-E PA power cells are biased to $V_{B|1} = 0.8\text{V}$ and $V_{B|2} = 0.25\text{V}$ respectively. Each PA cell is then simulated in a load pull bench by varying the load Z_L , and the power and efficiency contours are extracted at the desired peak and back-off operation points. Using the proposed combiner analysis technique, the load impedance seen by the main and auxiliary cells can be calculated and overlaid on the smith chart contours in order to compute the DPA performance at peak and back-off power. This procedure is repeated until an optimal q value (in terms of peak and back-off efficiency) is found.

In the case of the proposed DPA, $q = 1$ and results in the schematic of Figure 4.3 where the reactive elements of the combiner are merged with the class-E series LC resonators, leading to a more compact circuit. At the inputs, both a power and phase difference, ΔP and $\Delta \theta$ respectively, are introduced. These two design variables are used to further optimize the DPA performance.

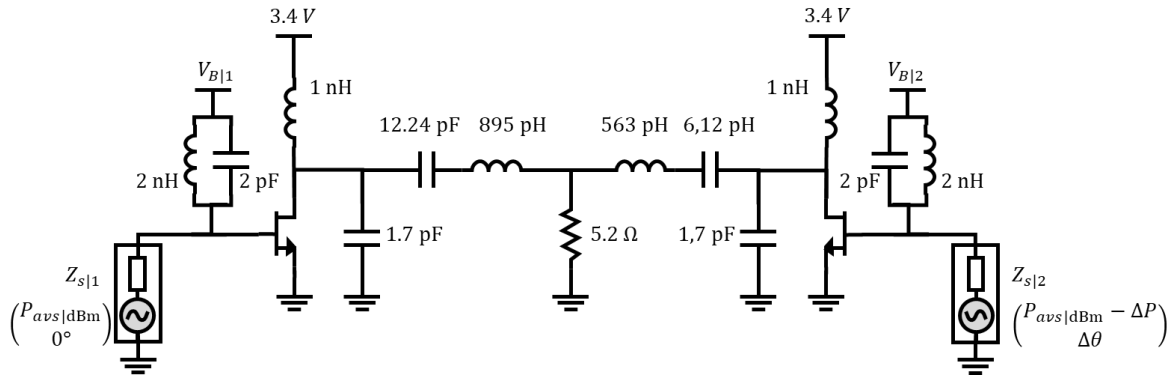


Figure 4.3 – Schematic of the class-E DPA power stage with combiner.

Figure 4.4(a) and (b) show the load pull contours of the main class-E power cell with the load modulation trajectory seen by the main branch at peak and back-off powers respectively. The same is done for the auxiliary branch in Figure 4.4(c) at the peak operation point (since the auxiliary is off at back-off). Drain efficiency of the DPA stage is around 71.6% at 32.3dBm output power (calculated using (3.73) and the values from Figure 4.4(a) and (c)) and 60% at 26.5dBm output power (Figure 4.4(b)). These results are validated in Figure 4.4(d) which shows the efficiency and gain profiles of the simulated DPA stage from Figure 4.3.

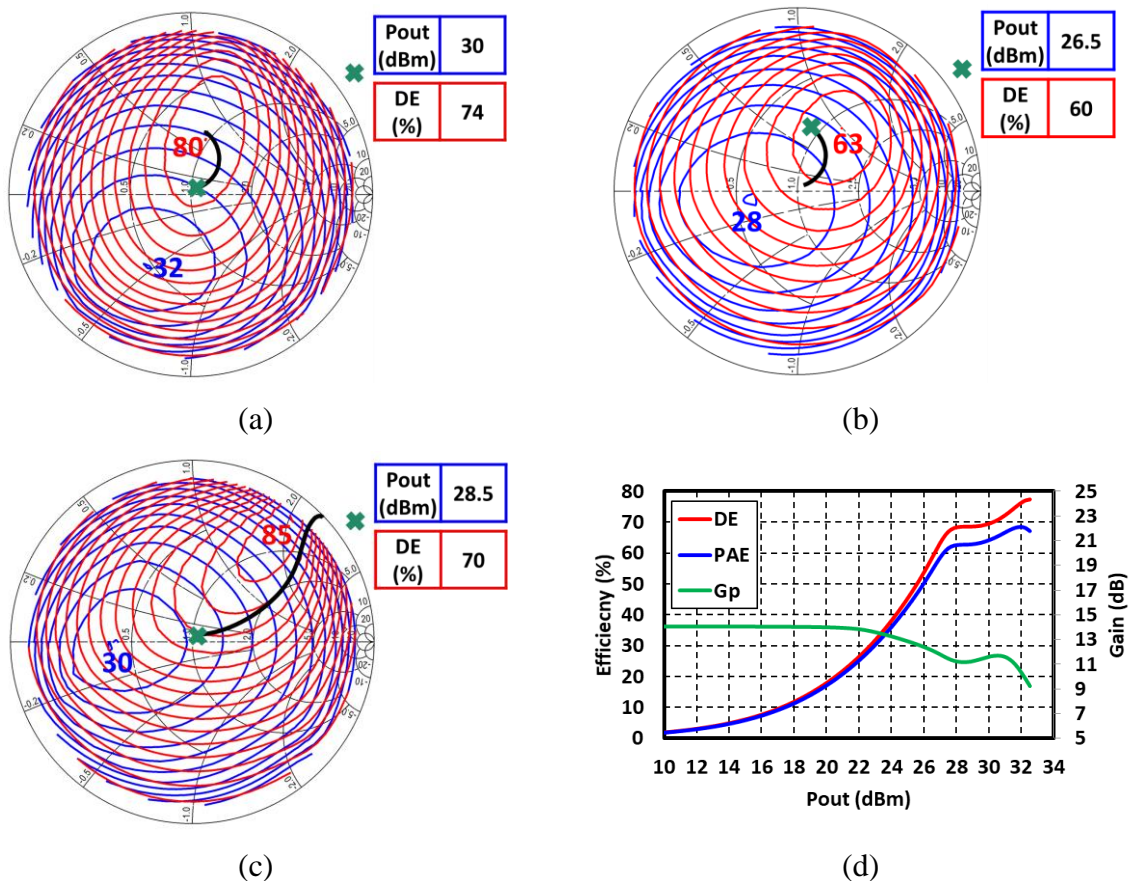


Figure 4.4 – 1dB step power contours and 5% step efficiency contours with load modulation trajectory seen at (a) main branch at peak, (b) main branch at back-off, (c) auxiliary branch at peak. (d) DPA stage efficiency and gain versus output power.

The DPA stage is optimized in terms of efficiency, but the gain profile shows a 3dB drop at high power which negatively impacts the linearity. In order to achieve more linear

characteristics, the auxiliary bias voltage is increased, and the DPA stage is operated using the design parameters listed in Table 4.2.

Table 4.2 – Linear DPA drive profile.

$V_{B 1}$	$V_{B 2}$	$Z_{S 1}$	$Z_{S 2}$	ΔP	$\Delta\theta$
0.82V	0.45V	$1.95 + j.025 \Omega$	$0.7 + j.2.8 \Omega$	2.5dB	25°

Figure 4.5(a) shows the simulated gain compression characteristic improvement between the previous (efficient mode) and the new settings (linear mode). However, this improvement in terms of linearity comes at the expense of efficiency in back-off throughout the Doherty region. As can be seen in Figure 4.5(b), the peak efficiency remains around 72% and 63% of DE and PAE respectively for 32dBm of output power. At 27dBm of output power, there is a noticeable difference since the efficiency drops to 52% and 47% of DE and PAE respectively. Nonetheless, the simulation results of the linear mode DPA are promising.

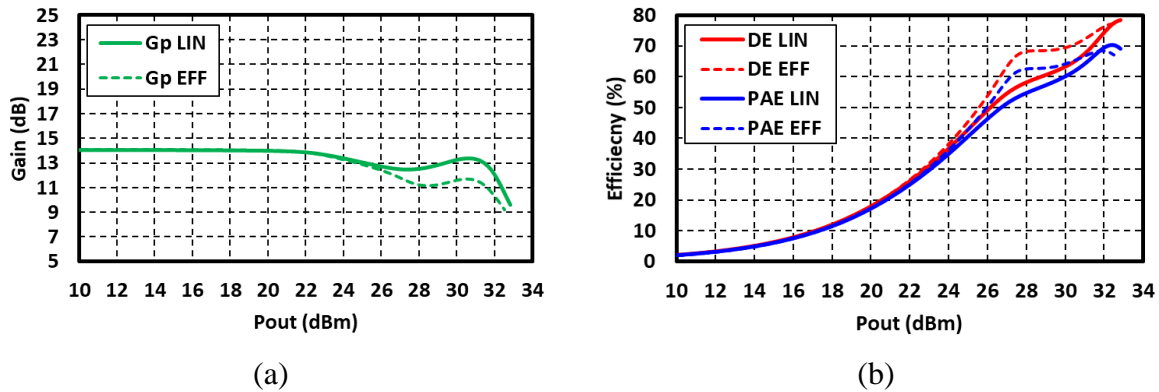


Figure 4.5 – Comparison of DPA (a) gain and (b) efficiency versus output power in the case of linear and efficient operation modes.

Having determined the baseline performance with optimal input and load impedances, the next step is to match the circuit to 50Ω using matching networks.

1.1.1 Impedance Matching

The impedance transformation ratios are first calculated and used to determine the optimal order of the required matching networks through the equation below [59]:

$$n_{opt} \rightarrow \ln \left[\sqrt{\frac{|Z_1|}{|Z_2|} - 1} \right] \tag{4.1}$$

Using the equation from (4.1), it is determined that a two-stage matching network is optimal at both inputs and at the output.

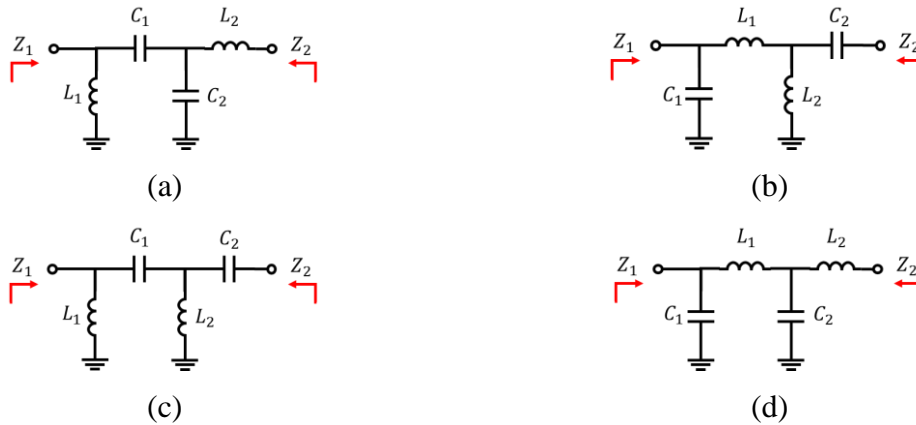


Figure 4.6 – (a) Low Pass-High Pass (LPHP) matching network, (b) High Pass-Low Pass (HPLP) matching network, (c) Low Pass-Low Pass (LPLP) matching network, (d) High Pass-High Pass (HPHP) matching network.

Four possible matching network configurations were evaluated, observing from right to left:

- Low Pass-High Pass (LPHP) in Figure 4.6(a)
- High Pass-Low Pass (HPLP) in Figure 4.6(b)
- Low Pass-Low Pass (LPLP) in Figure 4.6(c)
- High Pass-High Pass (HPHP) in Figure 4.6(d)

The same type of network is used for both inputs so as to minimize loss and phase mismatch between the two branches. Each of the four networks is then simulated with optimized input drive parameters ΔP and $\Delta \theta$ and the simulation results are plotted in Figure 4.7.

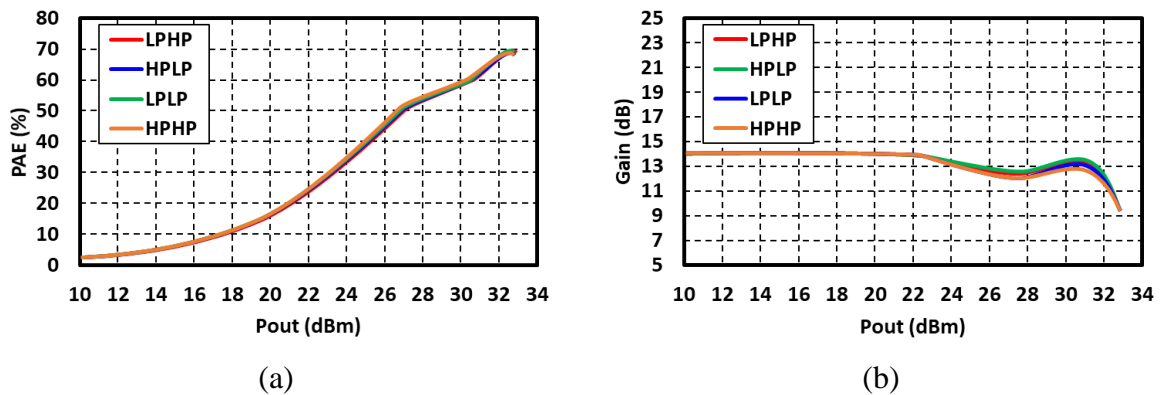


Figure 4.7 – (a) PAE and (b) Power gain performance versus output power for different IMN architectures.

As the four architectures are relatively equivalent in terms of overall PA performance, other criteria are taken into account:

The HPHP architecture is excluded since it has no series capacitor which would require the addition of an additional decoupling capacitor at the input in order to block the DC voltage.

The LPHP architecture is the best suited since its series inductance at the gate input would provide easier layout integration by allowing routing the capacitors away from the gate without having to add parasitic inductance. The output matching network is also implemented as a LPHP architecture for the same reasons.

The selected IMNs are designed to transform the 50Ω reference impedance to the optimal source impedance Z_{sopt} at the design frequency f_0 . The impedance seen at the harmonics depends on the choice of the architecture and can affect PA stability and performance.

1.1.2 PA Stability

A first stability check is realized by simulating the input (S11, S22) and output (S33) reflection coefficients of the dual-input DPA as defined in Figure 4.8(a).

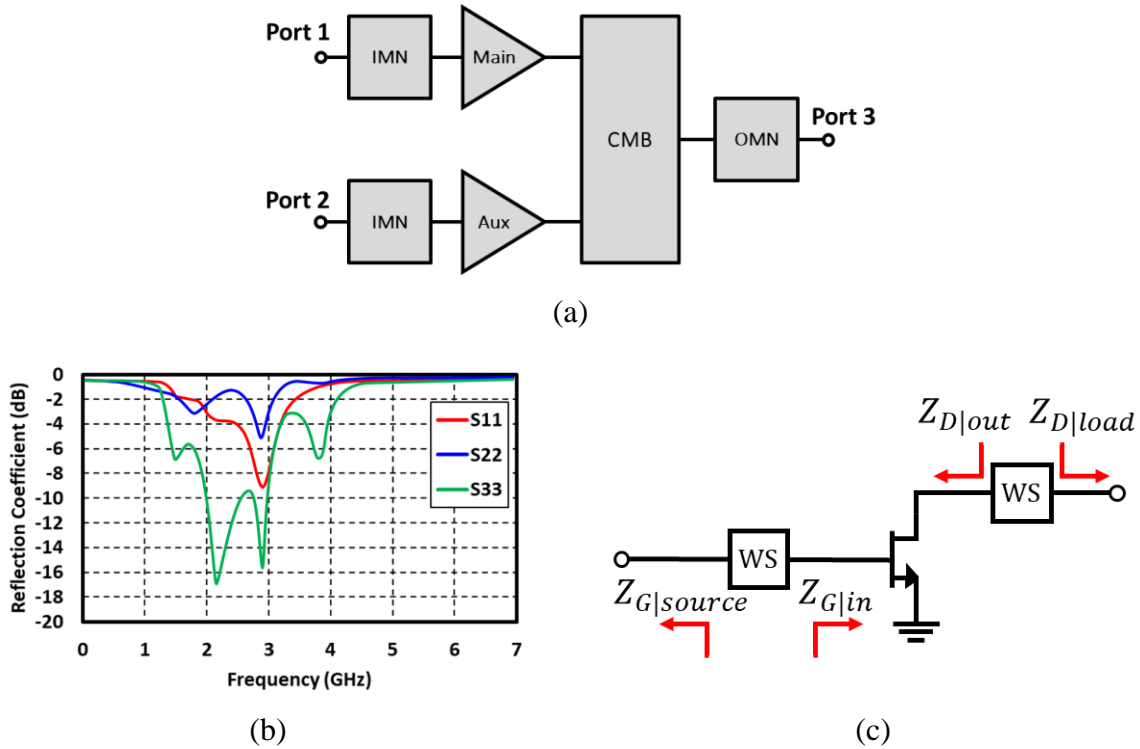


Figure 4.8 – (a) Dual-input DPA reflection coefficients, (b) Input and output impedance extraction.

Figure 4.8(b) shows that the reflection coefficients are negative for all frequencies indicating no signs of potential instability both in and out of the operation frequency band. This first test however, is only relative to small-signal behaviour and gives no information about the PA stability when operating at high power. Driving point admittance is therefore used to test large-signal stability at the gate and drain of the transistors [60]. This test looks at the input and output impedances Z_{in} and Z_{out} respectively using the *WS_Probe* in ADS design environment, as shown in Figure 4.8(c). A PA is considered unconditionally stable, when the real parts of Z_{in} and Z_{out} are positive for any power level. The input and output resistances of each PA branch are plotted against the overall output power in Figure 4.9.

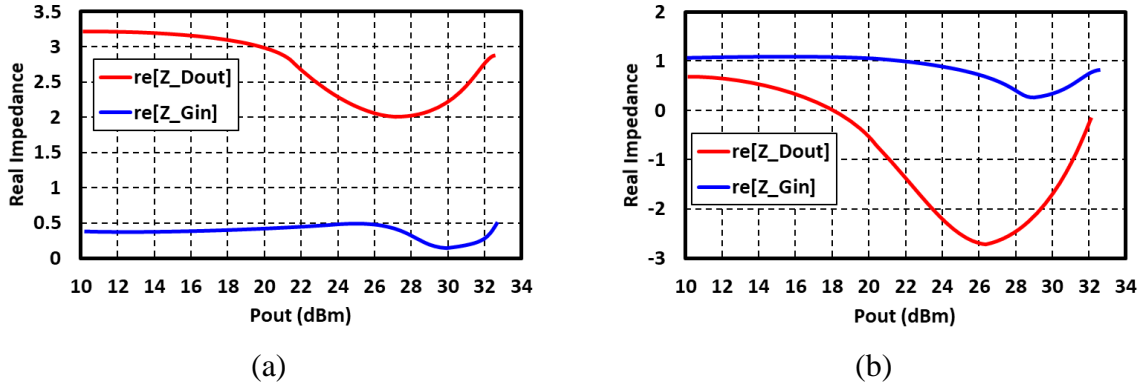


Figure 4.9 – Real part of the input and output impedances of (a) Main and (b) Auxiliary branch PAs.

All the resistances are positive with the exception of the output resistance of the auxiliary branch when operating in the Doherty region. The negative value is an indication of a possible instability, and should therefore be eliminated by tuning the value of impedance $Z_{s|2}$.

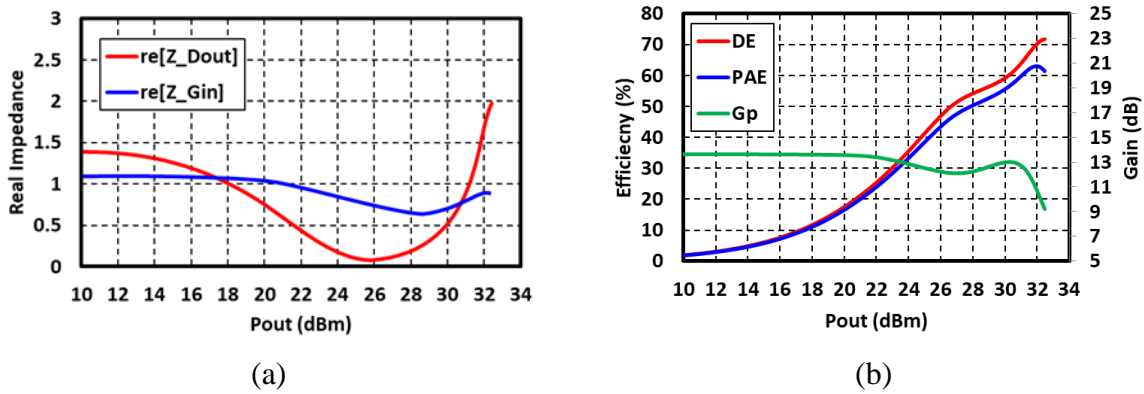


Figure 4.10 – (a) Real part of the input and output impedances of the auxiliary branch PA after tuning. (b) Simulated DPA efficiency and gain versus output power achieved after tuning.

For an input impedance $Z_{s|2} = 2.15 + j.2.02 \Omega$ (and optimized drive conditions) the output impedance $Z_{out|2}$ becomes positive for all power levels at f_0 as shown in Figure 4.10(a). The modified DPA drive profile is indicated in Table 4.3 and results in the efficiency characteristics shown in Figure 4.10(b). The DPA delivers up to 33dBm of output power with a peak PAE of 62%. At 27dBm, the PAE value drops to 40%. The power gain profile is mostly flat around 13dB.

Table 4.3 – Modified DPA drive profile.

$V_{B 1}$	$V_{B 2}$	$Z_{s 1}$	$Z_{s 2}$	ΔP	$\Delta\theta$
0.82V	0.45V	$1.95 + j.025 \Omega$	$2.15 + j.2.02 \Omega$	2.5dB	25°

The final dual-input DPA stage schematic is given in Figure 4.11 below. In order to boost the gain, a driver stage is then considered as detailed in the next section.

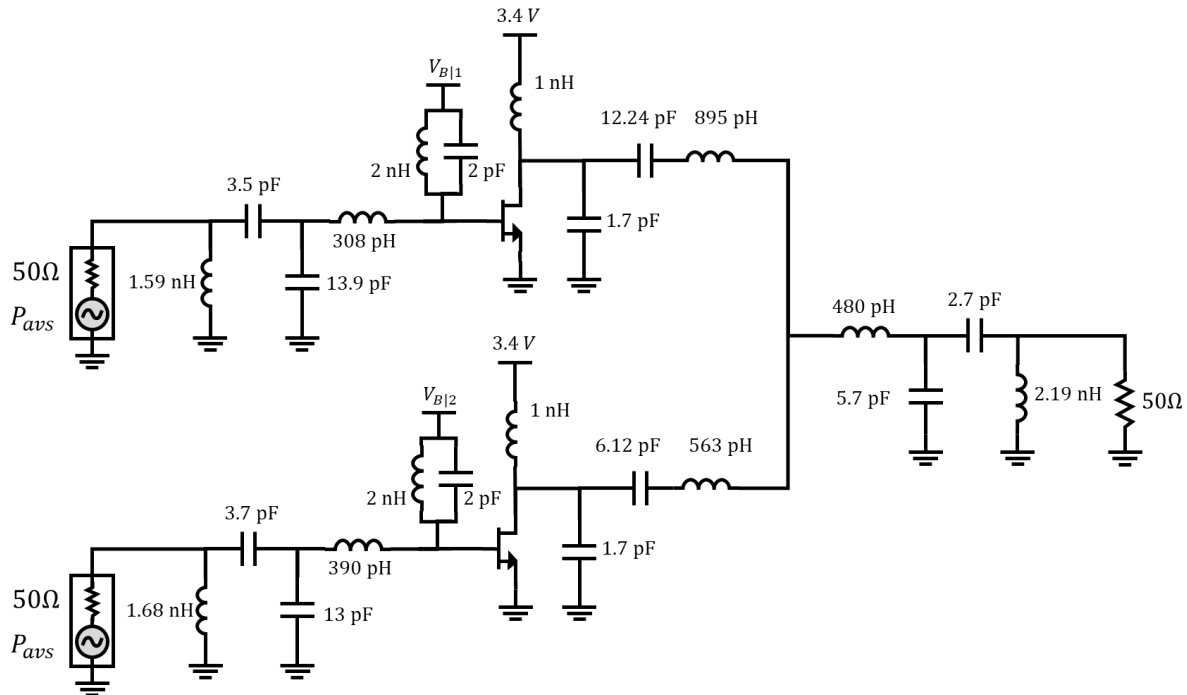


Figure 4.11 – Single-stage dual-input DPA schematic with input and output matching networks.

1.2 Driver Stage Design

A driver is typically used to increase the overall gain of the PA. Its transistor and class of operation can be different from the power stage, but must nonetheless be compatible. Class-E stages are usually preceded by class-D stages capable of supplying the required square-wave voltage. However, in the proposed power stage design, class-E power cells driven by a sine wave are considered, and it is then possible to operate the driver stage in linear class-AB. As a result, the overall PA linearity can be maintained without degrading the overall efficiency [18].

A cascode topology is selected for the driver cells in order to handle high voltage swings while providing high gain. An LDMOS transistor is used in common gate configuration (CG) in series with a body-contacted NMOS transistor in common source configuration (CS) as shown in Figure 4.12(a). As for the power stage, an electromagnetic (EM) extraction is performed and results in the transistor model of Figure 4.12(b).

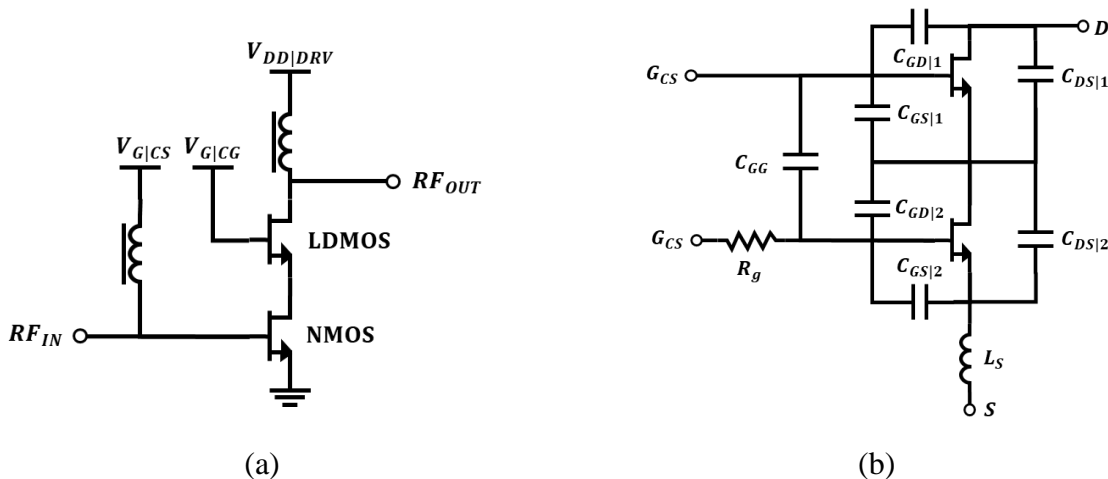


Figure 4.12 – (a) Cascode topology schematic and (b) Driver stage equivalent model.

The required driver stage output power and efficiency can be estimated by calculating the power budget of the overall two-stage PA line-up. For an output power of 33 dBm, the driver stage must provide 26 dBm of output power (in order to account for loss). The overall PA efficiency can be expressed in terms of efficiency and gain of the driver and power stages as well as insertion loss of the inter-stage network using (4.2).

$$\frac{1}{PAE_{Tot}} = \left(\frac{1}{\eta_{PWR}} + \frac{1}{\eta_{DRV} \cdot IL_{IS} \cdot G_{P|PWR}} \right) \cdot \left(1 - \frac{1}{G_{P|DRV} \cdot G_{P|PWR} \cdot IL_{IS}} \right) \quad (4.2)$$

Based on the power stage performance, the required driver efficiency and power gain can be calculated for a given overall PAE. However, the driver performance is subject to change once placed into the two-stage PA because the load modulation at the drains of the power stage leads to load modulation of the driver through the gate-drain capacitors C_{gd} of the power stage and the inter-stage network. The driver stage must then be tuned from the initial design step, in order to take into account the impact of this effect.

1.3 Inter-Stage Matching Network Design

The inter-stage matching network plays a crucial role. It must provide adequate source impedances $Z_{s|1,2}$ to the power stage, ensure correct phase difference and provide correct load impedance $Z_{L|DRV}$ to the driver stage.

In Figure 4.13, the different ISMN components are shown. The matching networks MN1 and MN2 are designed to provide the required source impedances. By using a high-pass architecture for MN1 and a low-pass architecture for MN2, a 90° phase shift is introduced. However, as seen in *section 1.1*, the dual-input DPA requires a phase difference $\Delta\theta \neq 90^\circ$. The correct phase shift is therefore achieved by adding a high-pass circuit MN3.

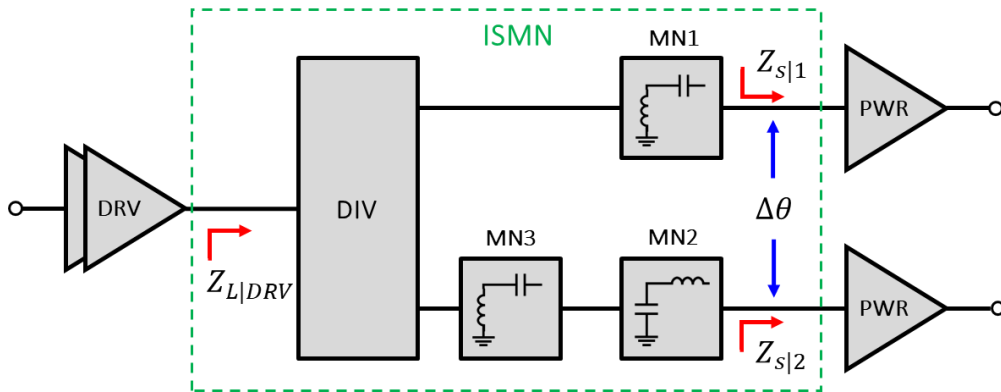


Figure 4.13 – ISMN sub-circuit components.

The power divider is implemented using a Wilkinson divider. The conventional lumped-element Wilkinson [61] is shown in Figure 4.14(a). This architecture includes two series inductors and thus is prone to high insertion loss since inductors generally present a limited quality factor. In [62], the authors propose a modified version of the lumped-element power divider, shown in Figure 4.14(b). An AC coupling capacitor C_{CP} is added at the input of the divider in order to block the DC voltage from the driver stage supply.

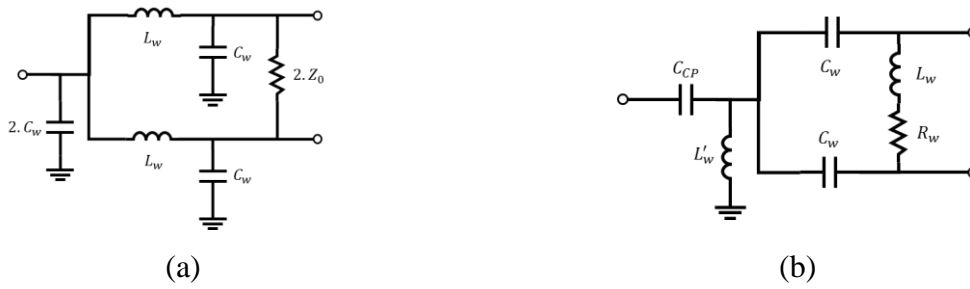


Figure 4.14 – (a) Conventional lumped-element Wilkinson divider, (b) Modified Wilkinson lumped-element divider

The divider exhibits vertical symmetry, therefore the component values can be calculated using even/odd mode analysis [63].

The methods described in this section give a starting point for the ISMN design. However, the component values must be tuned once all the blocks are placed in the two-stage PA line-up in order to take into account the impedance changes brought on by the load modulation.

1.4 Two-Stage DPA Line-Up and Simulation

The different two-stage PA sub-blocks are put together, and the full two-stage DPA circuit is simulated and tuned in order to get optimal results. The schematic of Figure 4.15 shows the different component values after tuning.

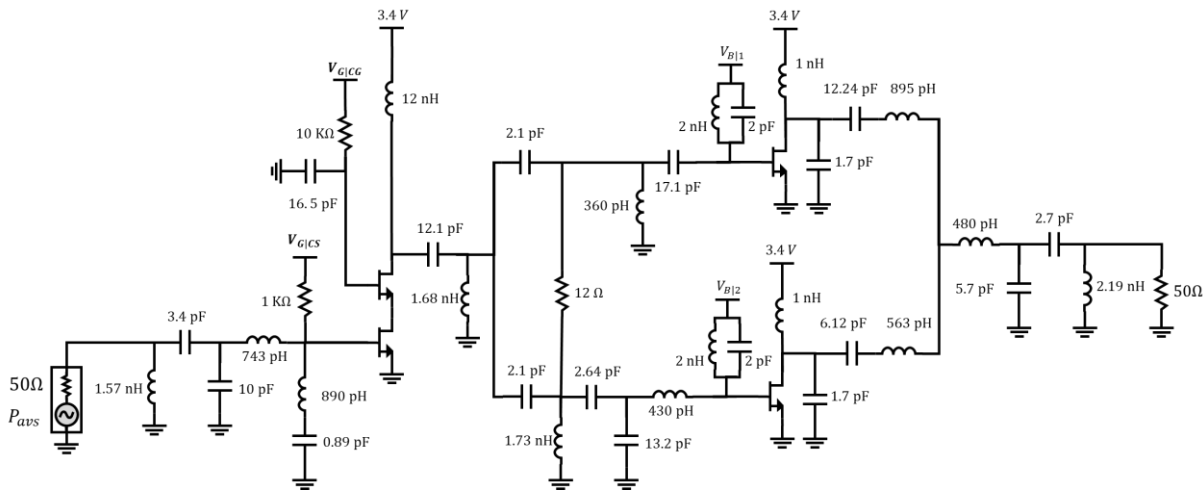


Figure 4.15 – Tuned single-input two-stage DPA schematic.

A second order LPHP architecture is used for both the IMN and OMN stages. A series LC shunt resonator is added to the IMN network in order to provide low input impedance at the second harmonic for improved linearity. The reactive compensation current combiner is merged with the class-E power cell matching networks, and the ISMN provides the optimal source impedance to the power stage. As with the dual-input DPA, the stability and bandwidth of the circuit is checked using S-parameter simulations as shown in Figure 4.16.

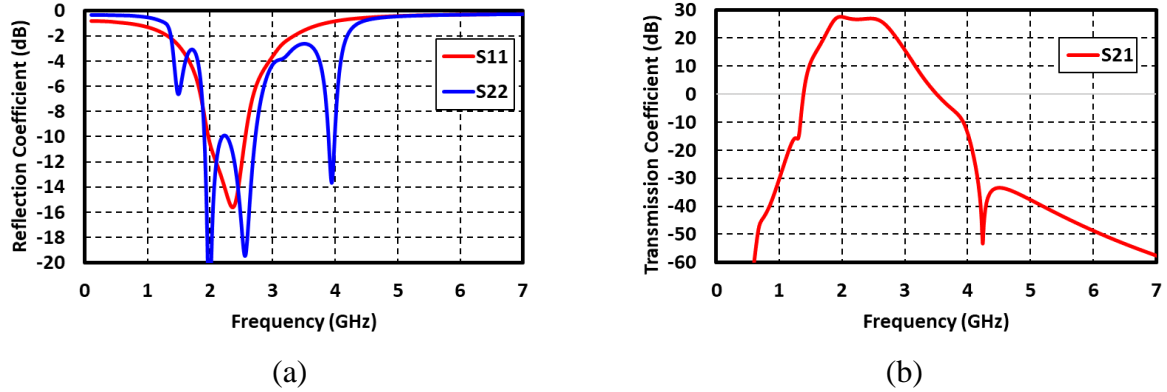


Figure 4.16 – (a) Reflection coefficients, (b) Transmission coefficient.

Good input and output are achieved as shown by S_{11} and S_{22} respectively. The input reflection coefficient remains below -10dB between 2.1 and 2.9GHz. Meanwhile, the output reflection coefficient goes down to -34dB between 2 and 2.9GHz and goes up to -10dB within this band. The transmission coefficient S_{21} shows that the small-signal gain is 25dB and remains close to this value between 2 and 2.8GHz.

Next, CW simulations are performed on the two-stage DPA, and the performance of the driver and power stages is analysed.

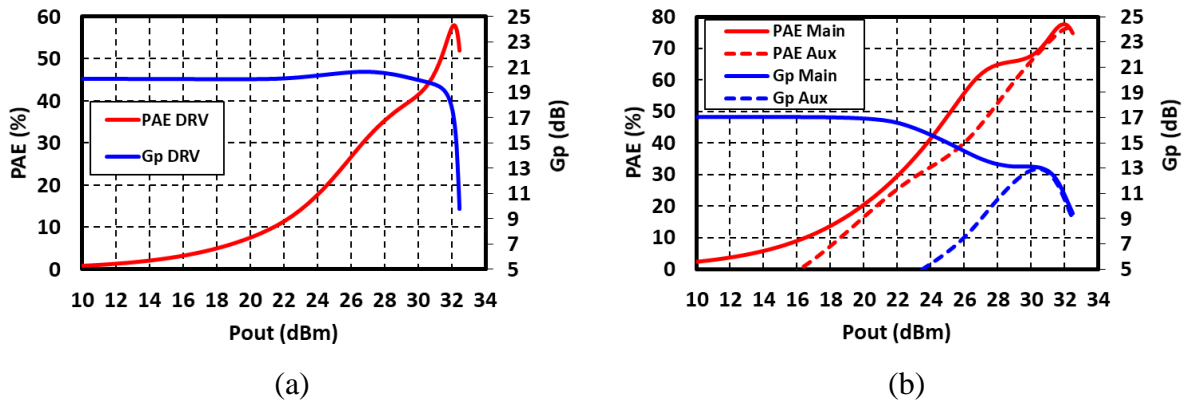


Figure 4.17 – (a) Driver stage performance, (b) Main and auxiliary branch performance.

Figure 4.17(a) shows the PAE and gain of the driver stage. The output power is 26dBm with a peak PAE of 58% at its drain. The performance of the main and auxiliary branches of the power stage are plotted in Figure 4.17(b) and show Doherty-like behaviour, with the auxiliary branch providing the necessary load modulation to push the main into higher power levels while keeping its high efficiency. The load modulation can be seen clearly in Figure 4.18(a) where the parallel resistances of the two power stage branches are plotted. As mentioned before, this modulation impacts the driver stage as well. The parallel load resistance and equivalent inductance of the driver change around 21dBm of output power.

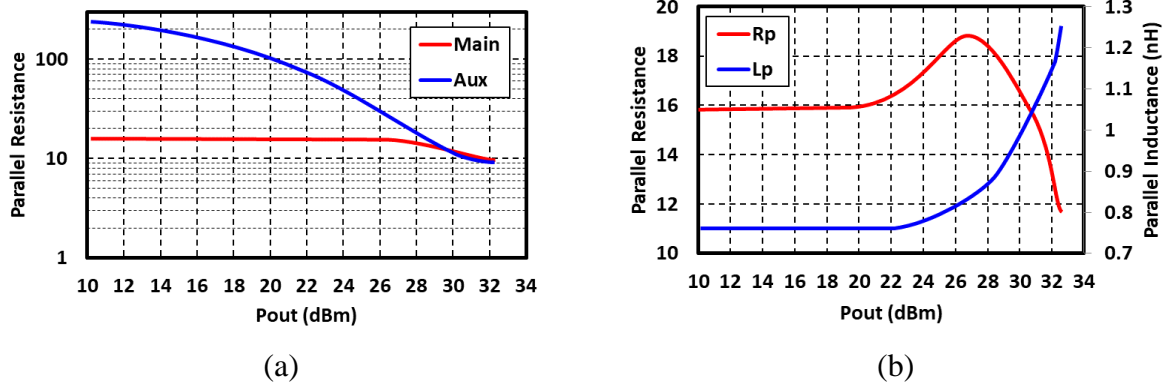


Figure 4.18 – (a) Real power stage load modulation, (b) driver stage load modulation.

The performance of the power stage with the two combined branches is shown in Figure 4.19(a). A peak PAE of 77% at 33dBm of output power is achieved with a small-signal gain of 15dB which drops to 13dB in the Doherty region. The phase difference at the input of the two branches is plotted in Figure 4.19(b) and shows the same evolution as that of the single-stage DPA from section 1.1.

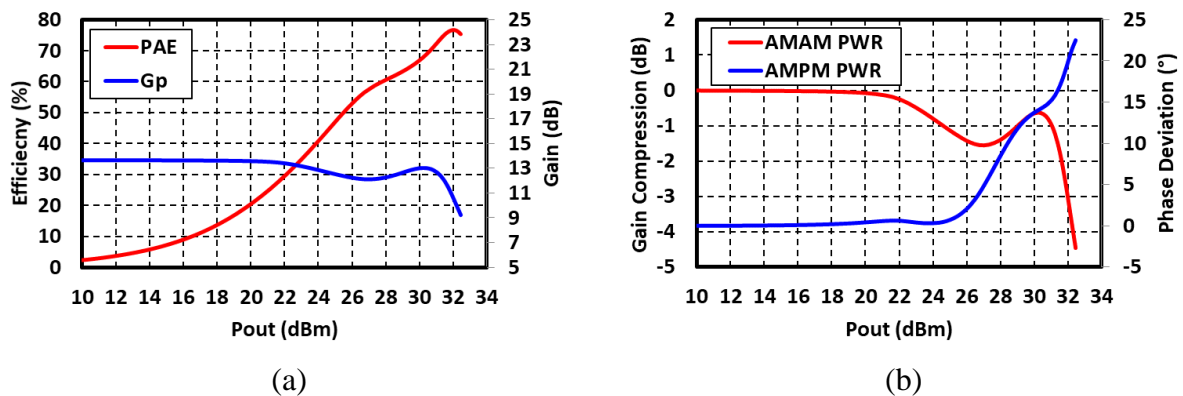


Figure 4.19 – (a) Simulated power stage PAE and gain versus output power. (b) power stage AMAM and AMPM distortions.

The gain compression shown in Figure 4.19(a) translates to AMAM distortion which affects the overall linearity. However, with proper tuning, the driver stage can be used to linearize the overall AMAM. This can be done by compensating the power stage AMAM with that of the DRV stage as illustrated in Figure 4.20(a). As a result, an overall flat AMAM can be achieved as shown in Figure 4.20(b). The overall AMPM distortion is also plotted and remains below 2° of variation before the PA saturates which is a satisfactory result.

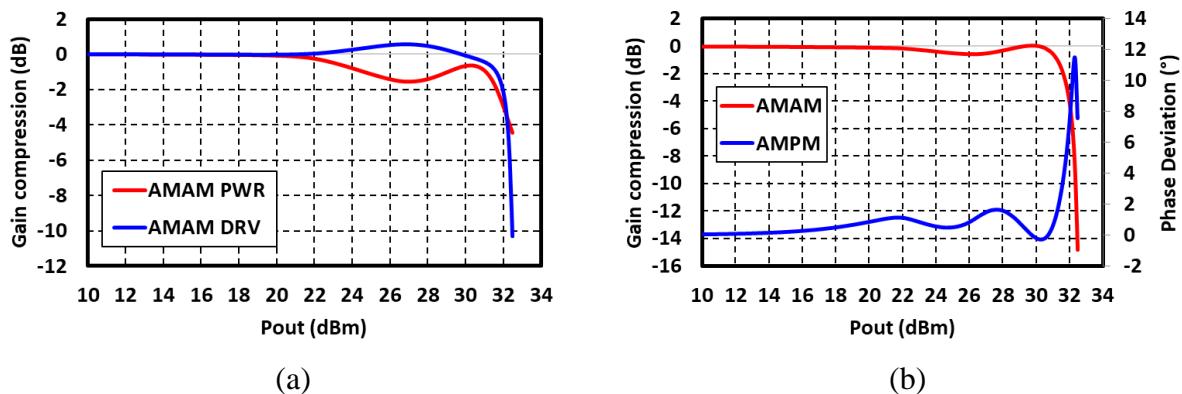


Figure 4.20 – (a) Power and driver stage AMAM distortion, (b) Two-stage DPA AMAM and AMPM distortion.

Finally, the two-stage DPA performance is plotted in Figure 4.21(a). The DPA achieves 57% of PAE at 32dBm of output power with a flat gain of 26.5dB. At 27dBm of output power (5dB back-off), the PA operates with an efficiency of 40%. The final delivered power is slightly lower than the targeted output of 33dBm. The insertion loss of the three matching networks are plotted in Figure 4.21(b) and show that the loss is mainly dominated by the ISMN stage.

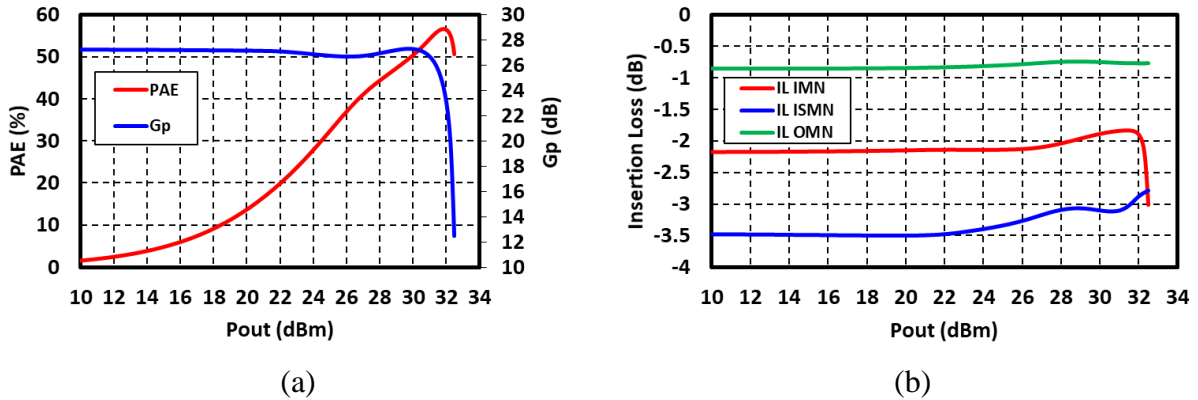


Figure 4.21 – (a) Two-stage DPA line-up performance, (b) Insertion loss of the matching stages.

Finally, the two-stage DPA is tested at different frequencies with the gate biases adjusted each time for optimal performance. Figure 4.22(a) shows that peak output power is higher than 30dBm with a peak PAE higher than 45%. The gain shown in Figure 4.22(b) is higher than 26.5dB except at 2.7GHz, as predicted by the S_{21} in Figure 4.16(b).

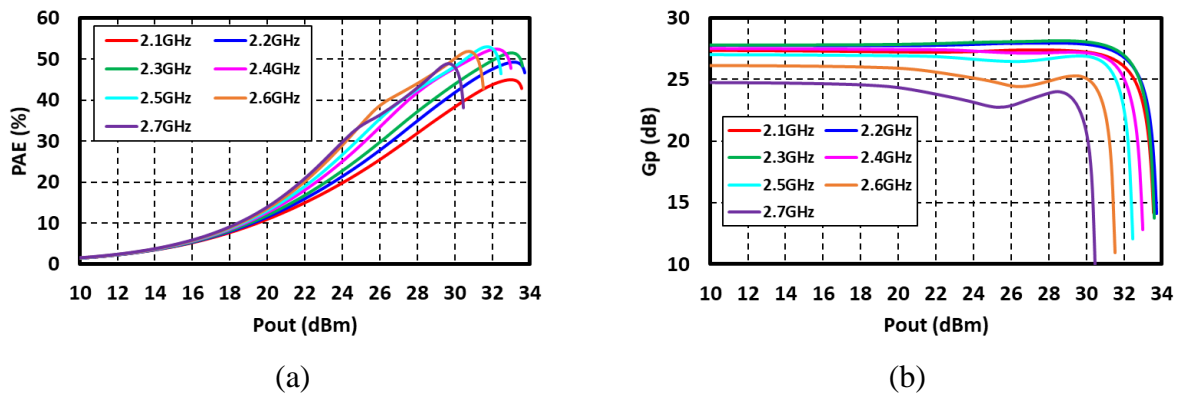


Figure 4.22 – Simulated (a) PAE and (b) gain profiles at different frequencies.

The peak and 6dB back-off PAE are extracted and plotted in Figure 4.23(a). The FBW is taken as the bandwidth corresponding to a $\leq 10\%$ change in peak PAE. Using this definition, the FBW is 16%.

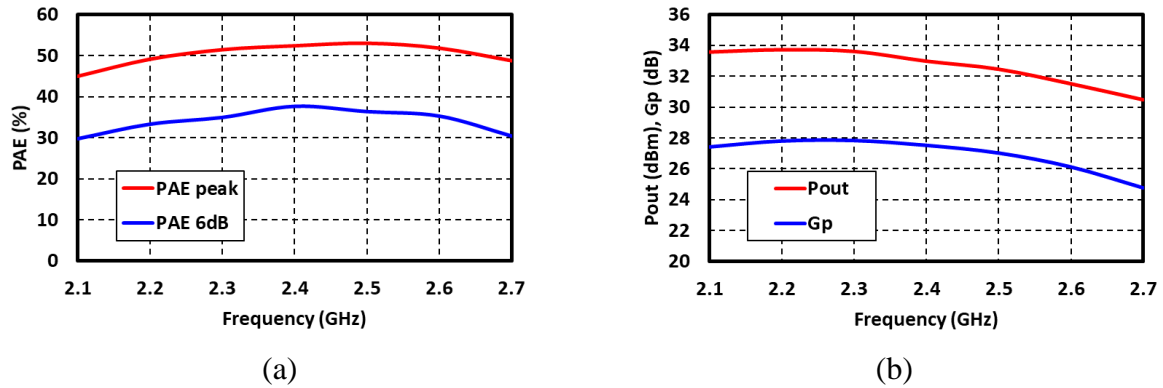


Figure 4.23 – Simulated (a) Peak and 6dB Back-Off PAE and (b) Output power and gain with respect to operating frequency.

Finally, the two-stage DPA provides more than 30.5dBm of output power and 25dB of gain within the 2.1-2.7 GHz frequency band.

This first section detailed the design methodology of the proposed two-stage class-E DPA. A dual-input DPA, used as the power stage, was first designed, matched to 50Ω , evaluated for stability, and tuned to provide optimal performance. The gain of this single-stage DPA was then boosted with the addition of a driver stage. A cascode topology was chosen for the driver cell and its performance in terms of output power, efficiency and gain was determined. The driver and power stages were connected through the inter-stage network which provides the required impedance levels to both the driver and the power stage. Finally, the two-stage DPA line-up was optimized through tuning. Carefully controlling the AMAM and AMPM distortion of the driver allows for compensating the power stage distortion, resulting in a linear two-stage Class-E PA.

After the design of the two-stage class-E DPA, the following step is the implementation. This requires a knowledge of the characteristics of the different implementation and packaging technologies. The next section will expose the main features of these technologies.

2 Integration Technology

The implementation of the final two-stage DPA design from the previous section (Figure 4.15), is performed using SOI-CMOS technology. The integrated circuit (IC), is then flip-chipped onto the packaging substrate technology using copper pillars (CuP) as can be seen in Figure 4.24. This solution offers an advantage over the classic solder bumps in terms of both minimum spacing (and therefore compactness) as well as thermal conductivity. The dimensions of the CuP are chosen after careful consideration of the thermal conductivity, electro-migration, and grounding constraints.

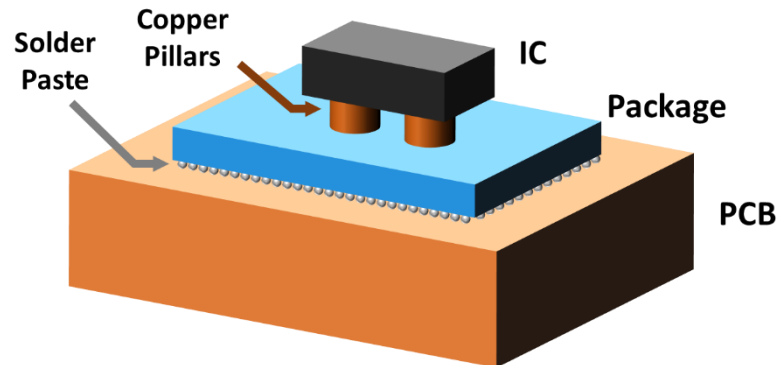


Figure 4.24 – Assembly technology stack-up.

The choice of the packaging technology is determined by the diameter and minimum spacing between the copper pillars. As detailed in [64], a laminate solution is chosen to accommodate large CuP capable of handling high currents. The IC and package must be co-designed simultaneously so as to take into account the different constraints and parasitic effects and therefore increase the circuit performance. The following sections detail characteristics of the selected technologies and the circuit implementation.

2.1 SOI-CMOS Technology

A 130nm RF-SOI technology from ST Microelectronics was selected for the implementation of the integrated circuit. This technology offers different back end of line (BEOL) options. In this design the M4TCTA option was chosen as it provides higher quality factor and current rating for the integrated inductors. Figure 4.25 shows a simplified stack-up of the selected technology. The different metal layers are listed on the left, while the vias are indicated on the right. The dielectrics in between the metals are represented in grey, and the die passivation in yellow.

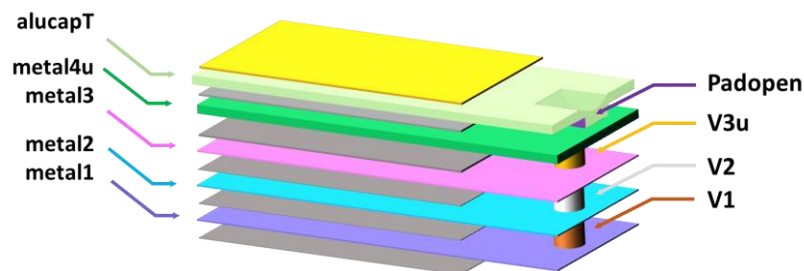


Figure 4.25 – RF-SOI technology M4TCTA stack showing metals on the left and vias on the right.

2.1.1 Inductors

The design kit (DK) of the chosen technology includes high current and high quality factor inductors. However, two types of compact custom inductors were used in order to optimize overall chip size. Figure 4.26(a) shows a first type of custom inductors designed for high-Q values. This is achieved by stacking different metal layers, which increases the cross-sectional area and therefore the conductivity of the structure. On the other hand, the inductor with high inductance value shown in Figure 4.26(b) is achieved by using multiple turns on different metallization levels [65].



Figure 4.26 – Custom inductor with (a) High quality factor, (b) High compactness.

Two examples of integrated inductors used in the circuit layout are presented below. The first inductor, the ISMN auxiliary series inductor $L_{S|Aux}$, illustrated in Figure 4.27(a), uses alucapT and metal4u layers in order to get a single loop with access lines for connection to the other components.

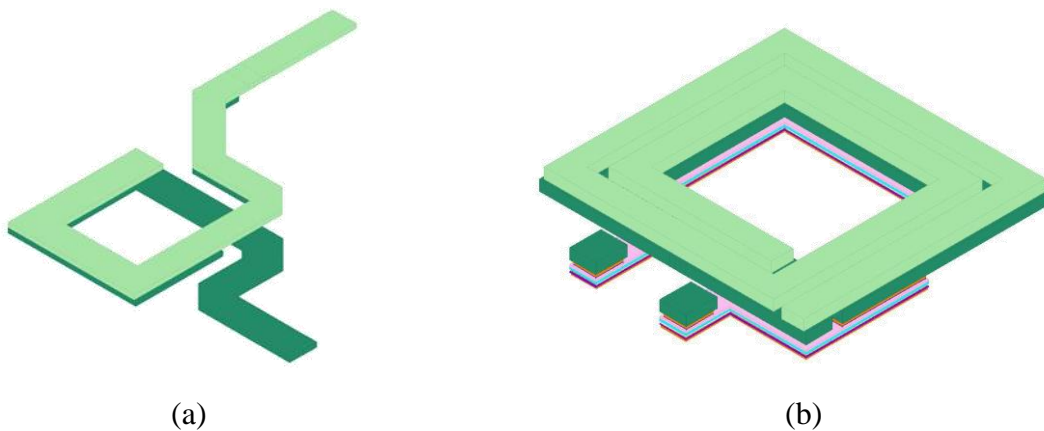


Figure 4.27 – Custom inductor with (a) High quality factor, (b) High inductance in a compact size.

The EM simulation results provided in Figure 4.28, show that the inductor has a value of 413pH with a quality factor of 17. Figure 4.27(b) shows the compact LC tank bias inductor. This inductor achieves a high inductance value of 2nH by effectively having 5 turns on different metal layers: 4 turns are made using the top two metal layers (alucapT and metal4u) which are thick and therefore provide adequate conductance. The final turn must therefore be made on the thinner metal3 layer, which would result in significant degradation of the quality factor. This is solved by stacking metal layers 1 to 3 as suggested above in order to increase effective conductivity.

This results in a compact integrated inductor with high inductance and a quality factor of 9.5 as shown in Figure 4.28. The self-resonance frequency (SRF) is 18GHz and is due to the parasitic capacitance between the different turns.

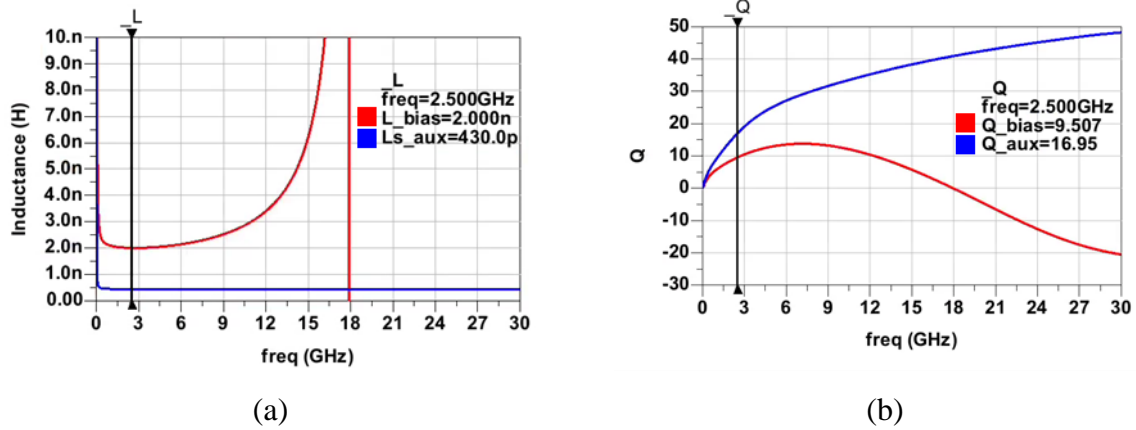


Figure 4.28 – EM simulation results of the series auxiliary inductor $L_{s|Aux}$ and the LC tank bias inductor L_{Bias} showing (a) inductance value and (b) quality factor with respect to frequency.

All the inductors of the two-stage DPA circuit in Figure 4.15 are integrated in the IC with the exception of those in the OMN and the three supply inductors since the supply and OMN inductors must handle high currents.

2.1.2 Capacitors

The DK offers two types of capacitors, Metal-Oxide-Metal (MOM) and Metal-Insulator-Metal (MIM). The MOM capacitor, represented in Figure 4.29(a) uses an interdigital capacitor structure on metals 3, 2, and 1 (with metal1 having twice as many fingers and half the finger width and spacing). The different layers are connected together using vias on the sides which make up the two access ports. The MIM capacitor is shown in Figure 4.29(b) and requires two additional layers to the standard BEOL stack (the metal and insulator layers seen on the left). The ports of the capacitor are located on the metal4u layer and connected through V3u vias. The choice of capacitor architecture depends on the component’s place in the circuit as they each offer their own advantages and drawbacks.

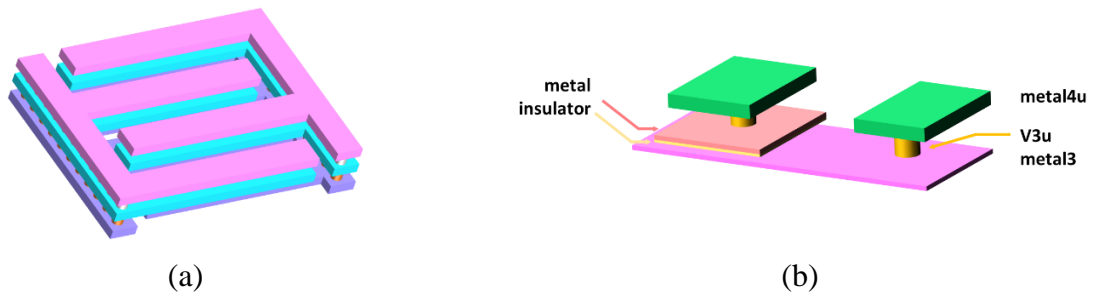


Figure 4.29 – 3D representation of (a) 3 metal layers MOM capacitor, (b) MIM capacitor.

The comparison in Table 4.4 shows that MIM capacitors have a higher integration density (4.4 times more compact), whereas MOMs can handle higher voltages and as such are more suited to power stages.

Table 4.4 – MOM and MIM specs comparison.

	MOM	MIM
Density	0.45 pF/mm ²	2 pF/mm ²
Qualification Voltage	25 V	5.5 V

The Q-factor and SRF of the capacitor are two other key metrics to consider. Both depend on the form factor of the capacitor: the number of fingers for a MOM, and the width for a MIM. Figure 4.30 shows the evolution of the Q-factor at 2.5GHz and the SRF for 1pF of a capacitance when the design parameters of the MOM and MIM capacitors are swept.

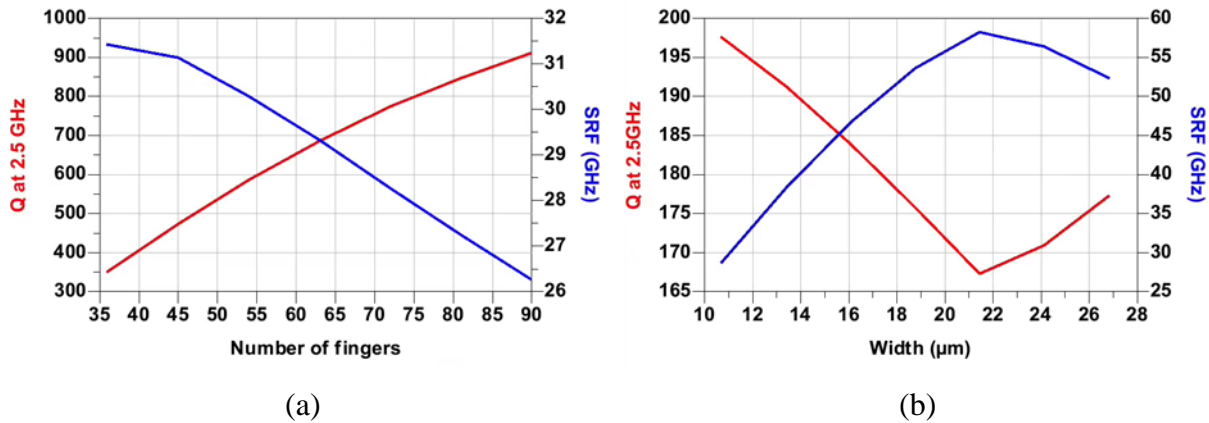


Figure 4.30 – Quality factor at 2.5GHz and self-resonance frequency simulated for 1pF using DK (a) MOM capacitor model, (b) MIM capacitor model.

MOM capacitors have a much higher quality factor than MIMs. However, given that both architectures present intrinsic Q-factors exceeding 150, the distinction is not very significant. During implementation, the SRF must be evaluated once the access structures are added as it could affect the capacitance value at the centre frequency.

The models provided by the DK have two main limitations: they are less accurate for high capacitance value, and they do not take into account the access structures needed to connect the capacitors to other components of the circuit.

The first limitation is overcome by placing multiple small capacitors in a parallel configuration, connected together using an access structure, in order to get the desired capacitance value.

The impact of the access structures can be taken into account by EM simulation and creating a capacitor model which contains the DK model in addition to the EM model of the access structure. This method is applicable to both MIM and MOM structures and is illustrated using the example of the IMN shunt capacitor (Figure 4.15). Given its position in the IMN, the capacitor is not subject to high voltage swings, and as a result can be implemented using a MIM.

The capacitor has a relatively large capacitance of 10pF and is therefore implemented by dividing it into 4 elementary capacitors of 2.5pF each. Figure 4.31(a) shows a 2D layout view of the elementary capacitor cell with Top and Bottom pins on the metal4u layer. The capacitors are connected together using an access structure on the metal4u and alucapT layers as shown in Figure 4.31(b).

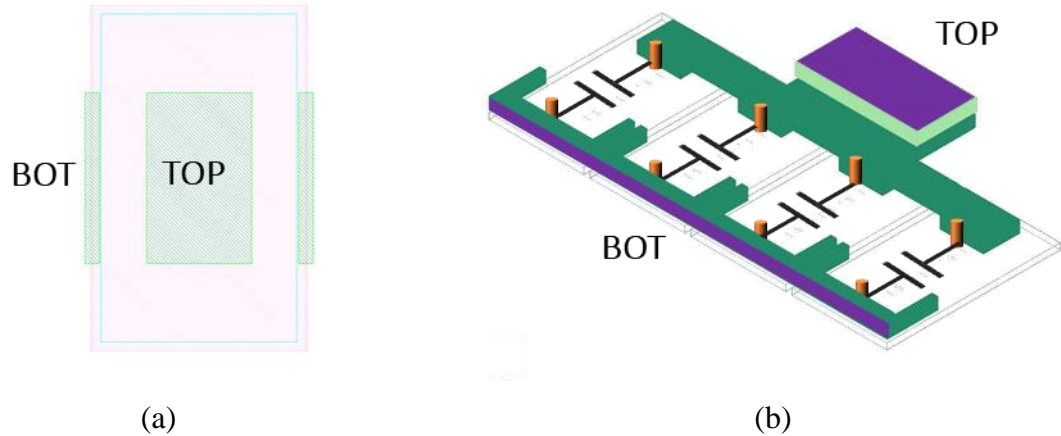


Figure 4.31 – (a) 2D layout view of the elementary MIM capacitor cell with top and bottom pins on the metal4u layer, (b) 3D view of the access structure with the external top and bottom pins marked in purple, and the internal connection pins to the unitary capacitor cells marked in orange.

The EM results of Figure 4.32 illustrate the effects of the additional access. When simulating the four capacitor DK models in parallel, the capacitance and Q-factor at 2.5GHz are 10pF and 153 respectively. The addition of the access structure has a significant effect on the SRF, lowering it from 32 to 15.5GHz. A second, but smaller resonance, can also be observed at 26GHz which is due to a parasitic capacitance between the metal plates. The Q-factor also decreases to 105 when considering the access. The value of the elementary capacitor is changed from 2.5pF to 2.44pF in order to fine tune the equivalent capacitance at 2.5GHz.

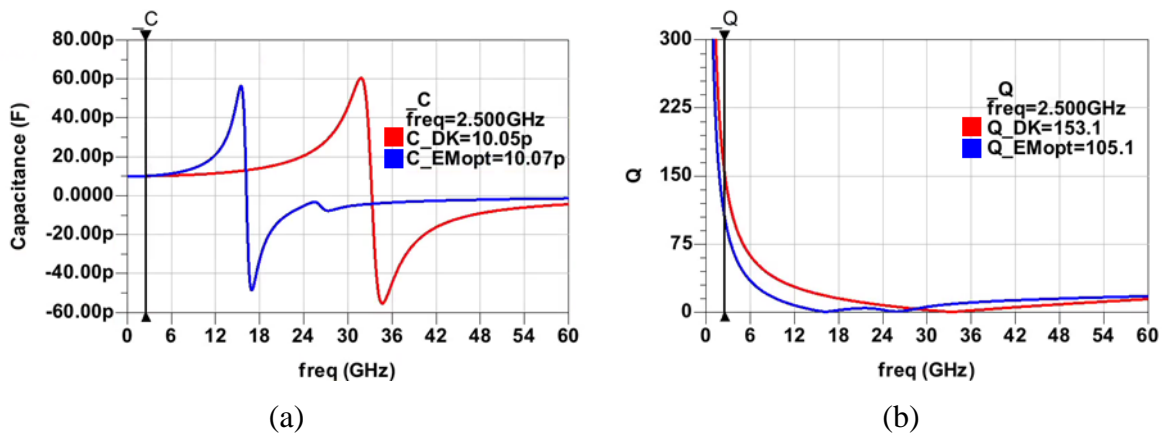


Figure 4.32 – (a) Capacitance and (b) Q-factor of the equivalent capacitor using 4 parallel capacitors with the DK model only (red) and EM model of the access+capacitor DK model (blue).

2.1.3 Power Device

The power device is the core of the PA circuit and special care must be taken during implementation. The elementary cell uses a LDMOS transistor with a gate length of 0.3 μ m. CC extraction and EM simulations are used to determine the parasitic elements of the electrical model. The main and auxiliary transistors of the power stage have a gate width of 8mm. They are made up of 8 transistors of 1mm, each consisting of two 0.5mm elementary cells as shown in Figure 4.33(a). The Drain and Source access are made using comb structures on the top alucapT and metal4u layers. The gate access is made using a tapered architecture of stacked metal1 and metal2 to ensure uniform distribution of the input signal to the different branches.

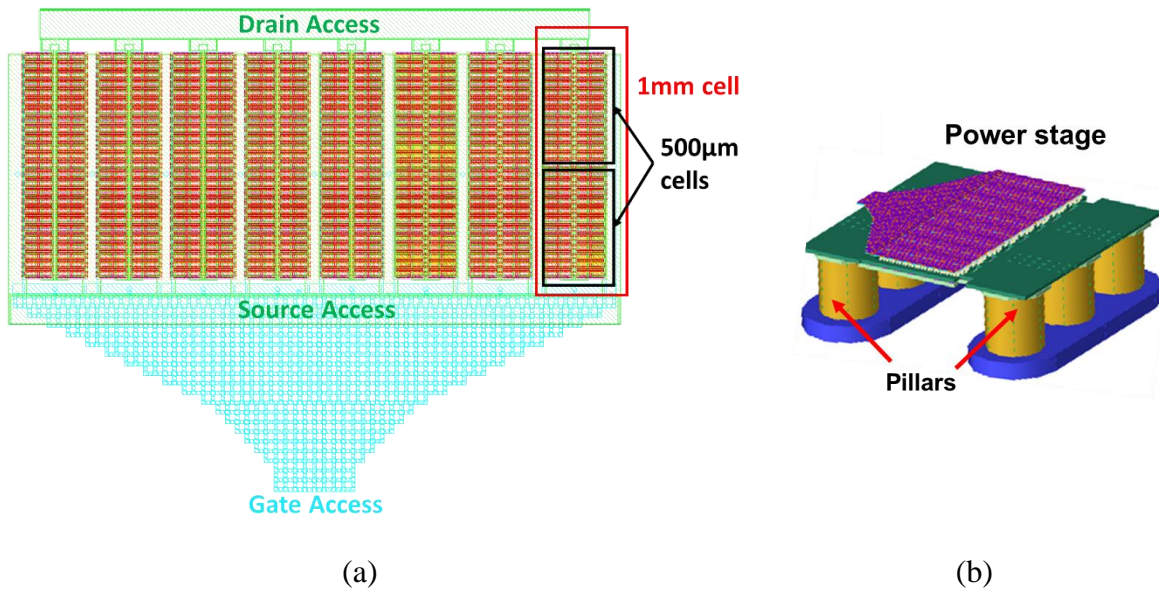


Figure 4.33 – (a) 2D layout view of the 8mm LDMOS PA cell, (b) 3D layout of the power stage with copper pillars.

As mentioned before, copper pillars (CuP) are used to connect the PA to the package substrate as shown in Figure 4.33(b). The choice of pillar diameter and length are mainly dictated by the maximum drain current and source inductance of the PA cell. In the proposed two-stage DPA, three copper pillars with 70µm of diameter and height are required for the drain and source connections.

2.2 Package Substrate Technology

Due to the copper pillar dimensions and spacing, a laminate package technology must be used. The selected laminate is a four-metal layer micro Printed Circuit Board (µPCB) as shown in Figure 4.34.

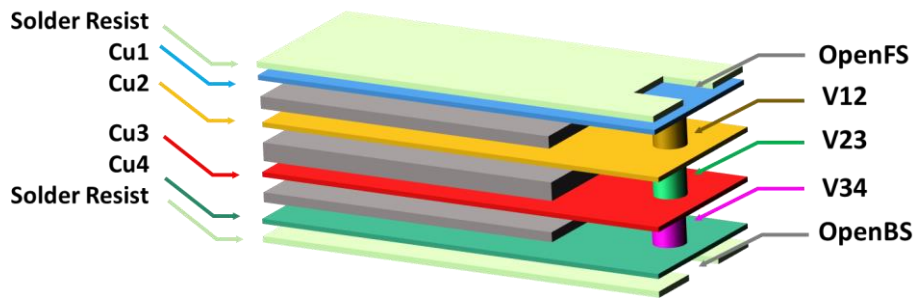


Figure 4.34 – µPCB laminate stack showing metals on the left and vias on the right.

The top and bottom sides of the stack are covered with an isolating solder resist film and negative layers (OpenFS and OpenBS) are used to get access to metals 1 and 4. Vias are used to connect the different metal layers. The metal layers are made of copper and have a thickness of 15µm which results in an increased current density when compared to the metals layers of the IC technology (the thickest SOI metal layer is 4µm).

Inductors can be made using metal traces much like those on SOI technology. The key difference is the achievable quality factor as shown in Figure 4.35 with the example of a supply

inductor. This inductor, uses layers Cu1 and Cu2 and has an inductance value of 1nH and a quality factor of 54 at the design frequency f_0 .

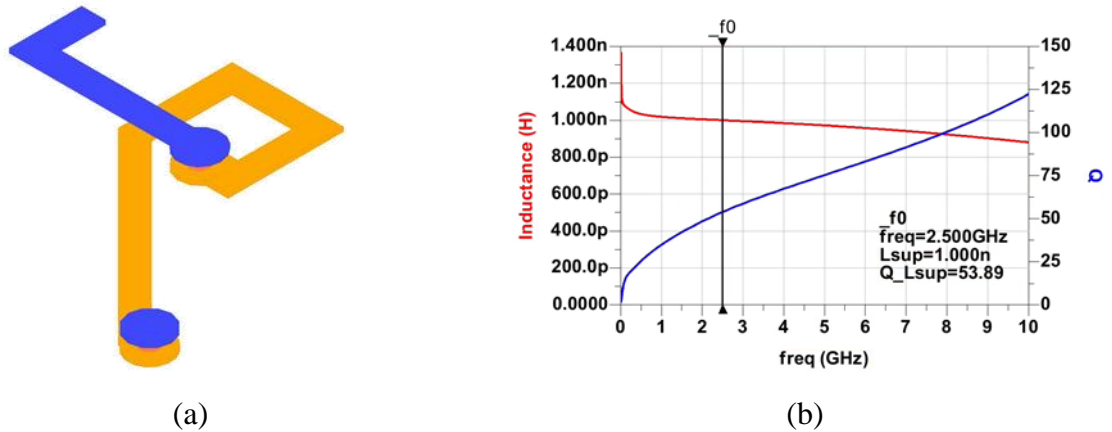


Figure 4.35 – (a) 3D view of the supply inductor layout, (b) Inductance and Q -factor of the EM model.

The inductors of the μ PCB must then be simulated together with the inductors of the IC in order to take into account the coupling effects. The inductors are then tuned until the desired values are achieved.

Capacitors can be placed on the laminate substrate using surface mounted devices (SMD). SMDs can also be used for large inductors which would take up a larger space if implemented directly on the μ PCB. Another advantage of the SMDs is their high quality factor and the ability to perform tuning during the measurement phase by swapping them for other values.

Finally, transmission lines can be used for routing purposes, ensuring 50Ω impedance if needed. They are implemented using coplanar waveguides (CPWG) designed using the *LineCalc* tool from ADS. An example is shown in Figure 4.36(a) where the transmission line is made using a Cu1 trace with a ground plane on Cu2 and the surrounding Cu1 connected through vias. The extracted EM model is simulated with 50Ω terminations and the results are illustrated in Figure 4.36(b). The transmission line shows excellent matching at 2.5GHz with $S_{11} = -35\text{dB}$ and very limited loss ($S_{21} = -0.02\text{dB}$).

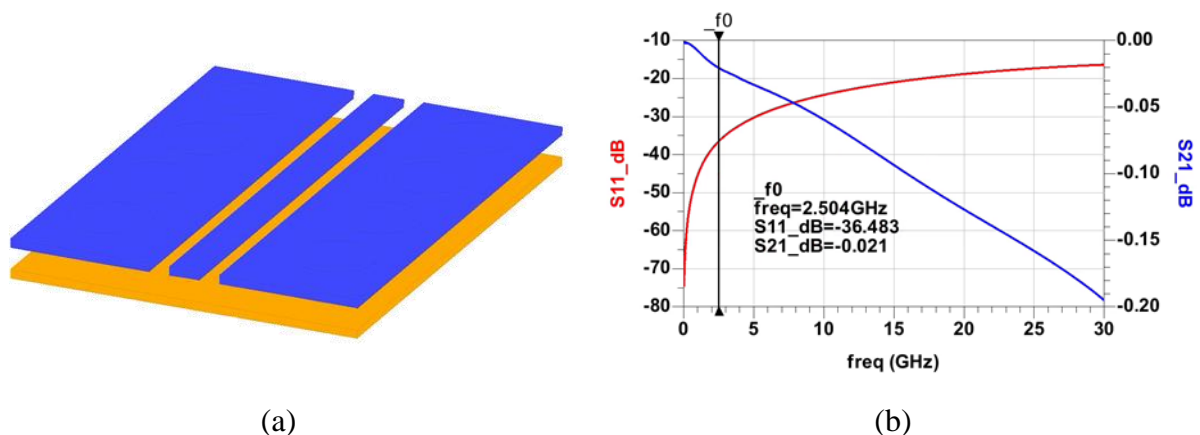


Figure 4.36 – (a) 3D view of the CPWG line implemented on Cu1 layer with a ground plane on Cu2, (b) S -parameters of the EM model.

2.3 PCB Technology

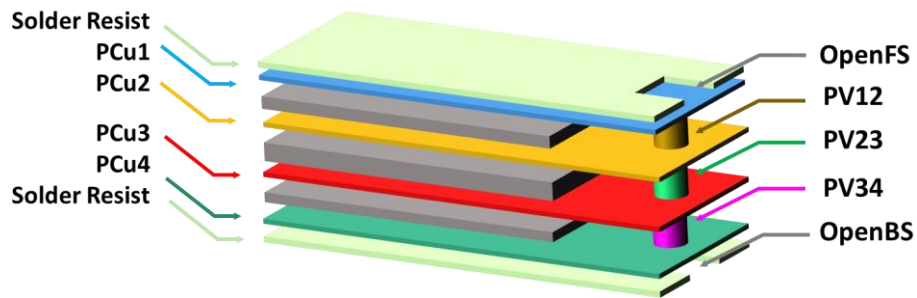


Figure 4.37 – PCB technology stack showing metals on the left and vias on the right.

A printed circuit board (PCB) is used to characterize the module by adding RF and DC connectors which allow direct connections to the lab equipment. The module is soldered on the PCB using a solder paste and the module ports are then connected to the I/O interface. RF ports are routed to the SMA connectors using 50Ω transmission lines. DC ports with high current are routed using wide metal traces in order to minimize resistive losses.

SMD components such as decoupling capacitors are placed on the PCB. Moreover, a radiator is added on the back-side of the PCB in order to provide a heat sink and improve thermal dissipation during PA measurements.

Finally, the ground reference of the module is provided by the PCu4 layer of the PCB shown in Figure 4.37. It is therefore important to include the PCB layers when performing EM simulations so as to take into account the parasitic ground inductance and get more precise results between simulation and measurement.

3 Circuit Implementation and Measurement

With the two-stage class-E DPA circuit design finalized, and the different implementation technologies presented, the final steps are circuit implementation, validation, and measurement.

3.1 Layout

Having detailed the characteristics of the different implementation technologies, a floor-plan must be elaborated in order to determine on which technology the different components will be implemented. While full integration is desirable, the limited inductor quality factors offered by the IC technology complicate this task. This is especially true for series components such as the class-E matching network inductors whose losses greatly impact the PA efficiency. As a result, the output network is implemented on the package as shown in Figure 4.38. The circuit ground reference is set on the bottom layer of the PCB (PCu4), and 50Ω access lines are added at the input and output of the DPA.

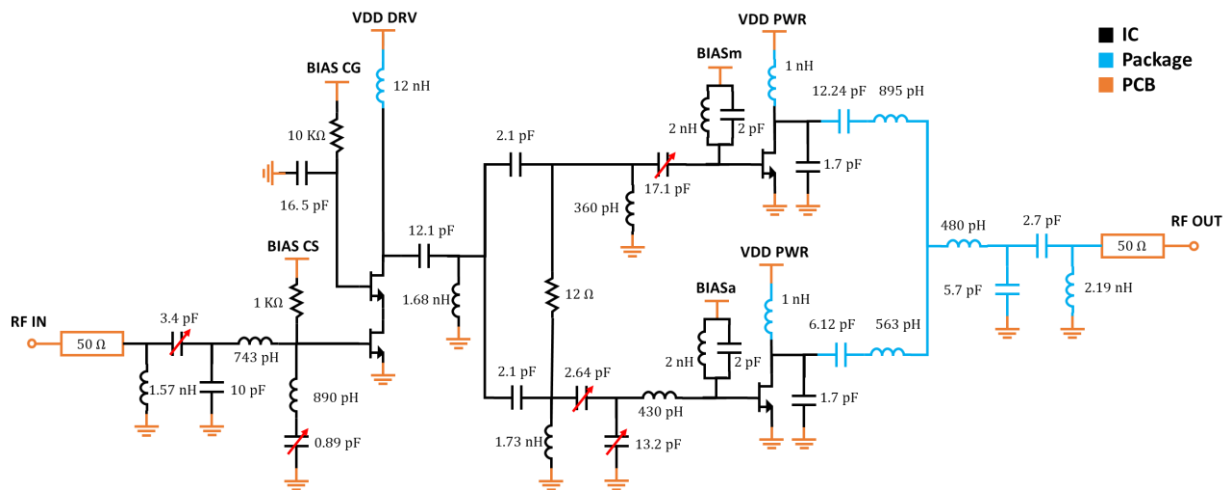


Figure 4.38 – Tuned single-input two-stage DPA schematic.

The IC level is implemented first. Inductors are first drawn and simulated individually using EM simulation before being simulated all together in order to account for electromagnetic coupling as illustrated in Figure 4.39. The inductors are then tuned so as to provide the required value.

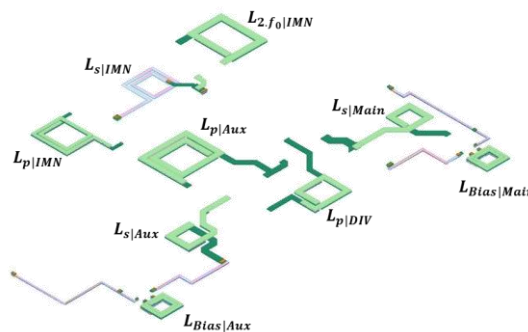


Figure 4.39 – RFpro 3D view of the integrated IC inductors

Capacitors are implemented using the MIM and MOM structures discussed earlier and reconfigurable capacitors (marked with a red arrow in Figure 4.38) are used in order to provide an additional degree of freedom during measurements. Digital and analog blocks are added to the IC chip in order to control the switched capacitors using a computer interface.

Figure 4.40(a) shows the 2D layout of the IC chip where the main, auxiliary and driver cells are connected to the network networks. The digital control part can be seen in the lower left corner of the chip. The μ PCB package design is shown in Figure 4.40(b).

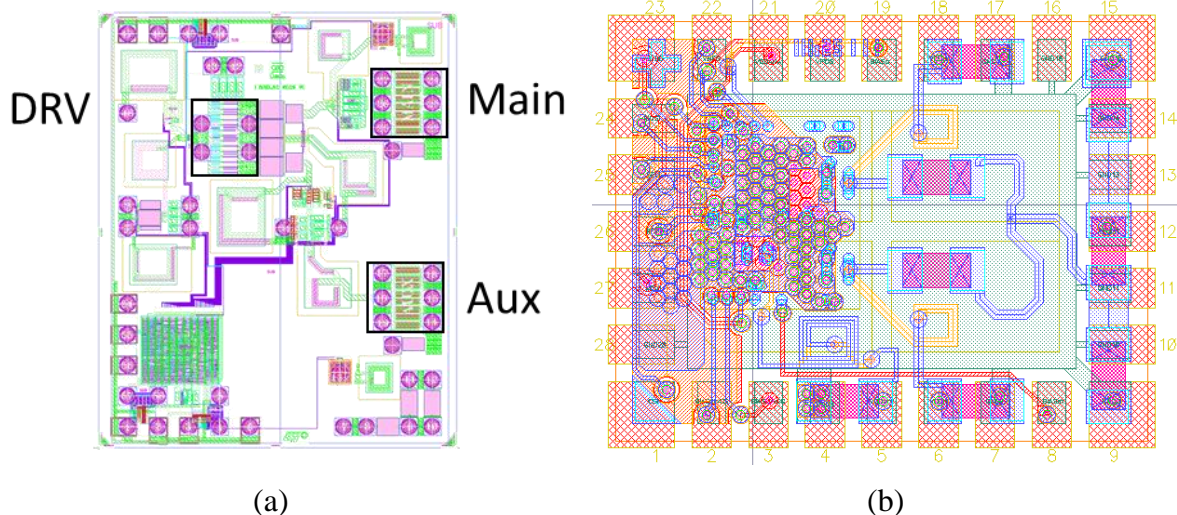


Figure 4.40 – (a) 2D layout view of the IC chip with black boxes outlining the main, auxiliary, and driver cells. (b) 2D layout view of the μ PCB package.

The capacitors as well as the parallel inductor of the OMN are implemented using SMD components. Supply inductors are realized using a combination of Cu1 and Cu2 layers. The ground plane beneath the IC is filled with vias in order to provide a direct short path to the PCB ground reference. This is done so as to minimize resistive losses in the source connections of the transistors as well as to avoid return loops between two ground paths. A final EM simulation is performed with the overall stack-up as shown in Figure 4.41. Once validated, the circuit can be sent to fabrication.

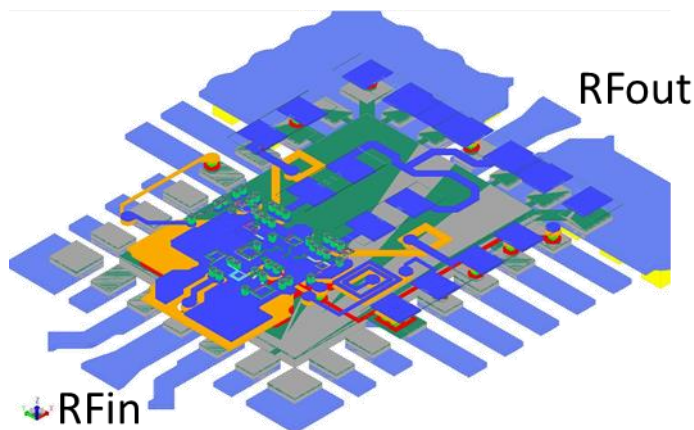


Figure 4.41 – 3D RFpro view of the full-stack for EM simulation.

Figure 4.42 shows the fabricated IC and laminate package. Due to the μ PCB fabrication process, over-etching was observed when examining the laminate. The inductor lines are 20%

thinner than the initial design which causes a shift in inductance and an increase in loss. In order to take into account the effects of this variation, the EM layout view of the package was modified. A new EM model is then extracted for subsequent comparisons between measurement and simulations.

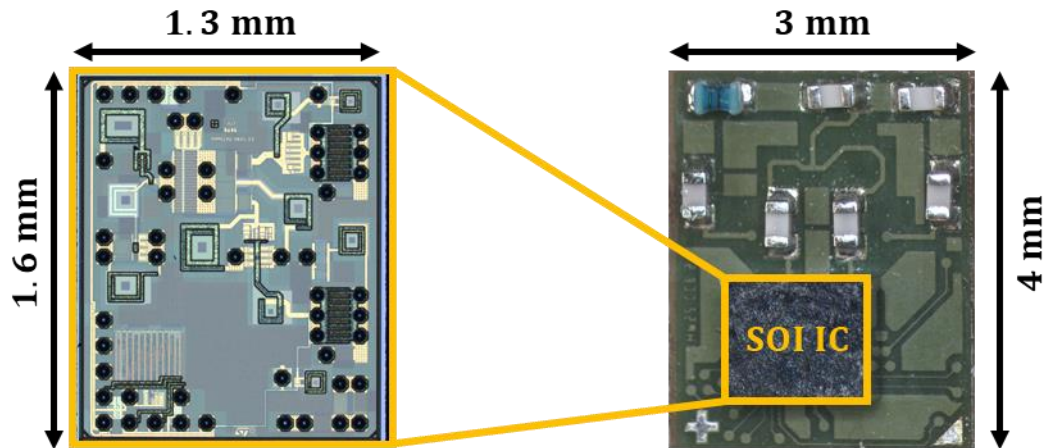


Figure 4.42 – IC die and laminate package photograph.

The IC and package are mounted onto the PCB shown in Figure 4.43(a). The board contains the RF input and output 50Ω access lines, as well as the DC supply lines and the digital circuit interface.

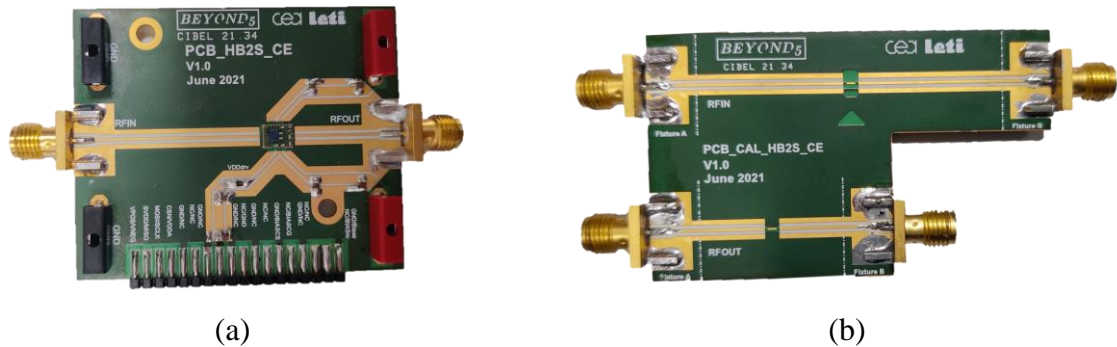


Figure 4.43 – (a) Fabricated PCB with mounted IC and package (b) PCB access lines test structure.

The 50Ω transmission lines are first validated using the test structure shown in Figure 4.43(b). Both the RF_{in} and RF_{out} lines are mirrored and connected to each other in the middle. Using a vector network analyzer (VNA), the S-parameters can be measured at the two ends of each line.

The reflection (S₁₁) and transmission (S₂₁) coefficients are extracted and used to create a more realistic transmission line model so that the EM simulation better fits with the measurements. The plots in Figure 4.44 show the measurement results along with the developed line model.

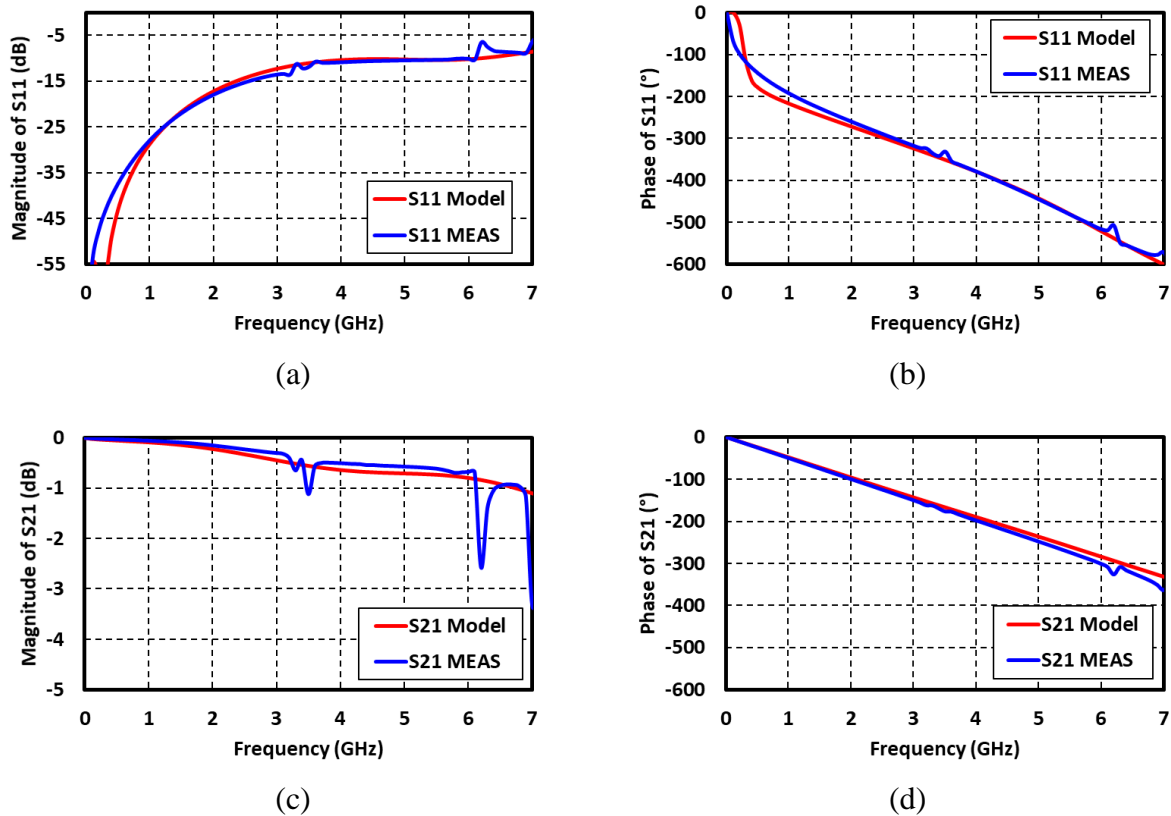


Figure 4.44 – Measurement and model comparison of (a) S11 magnitude, (b) S11 phase, (c) S21 magnitude, (d) S21 phase.

Thanks to these preliminary tests, a new more accurate retro-simulation EM model can be used to validate the performance of the fabricated circuit as will be shown below.

3.2 Validation

The circuit is placed in the measurement setup shown in Figure 4.45.

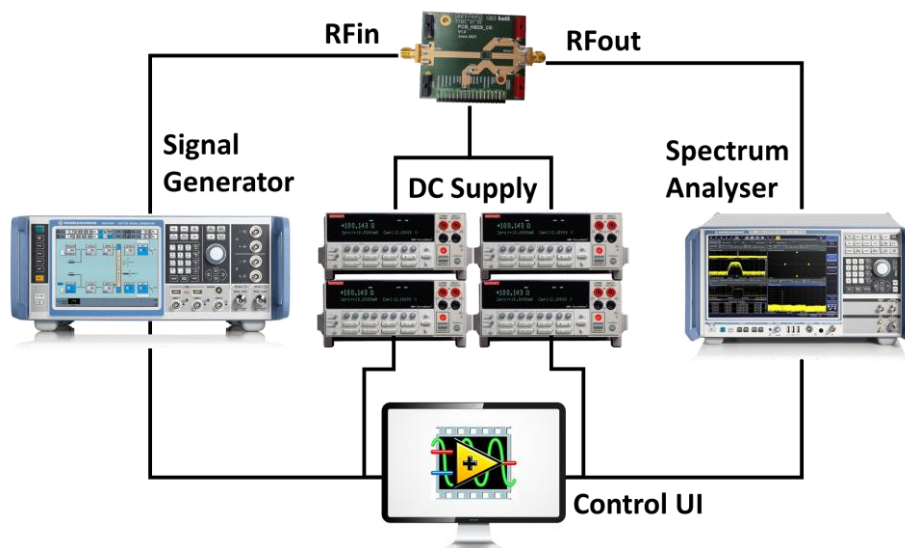


Figure 4.45 – PA measurement setup.

The signal generator is connected to the RF input while the spectrum analyzer is connected to the RF output. DC supplies are used to bias the PA as well as supply the digital interface. A

user interface (UI) control system is set up using LabVIEW in order to control the different equipment and extract measurement results.

First, the transistor is biased without an RF signal and the DC supply currents are plotted for both the driver and power stages. Gate bias voltages are tuned until the current consumption matches the PA model. Next, the input power is swept and the DC current evolution profiles are plotted and compared to the PA model as shown in Figure 4.46.

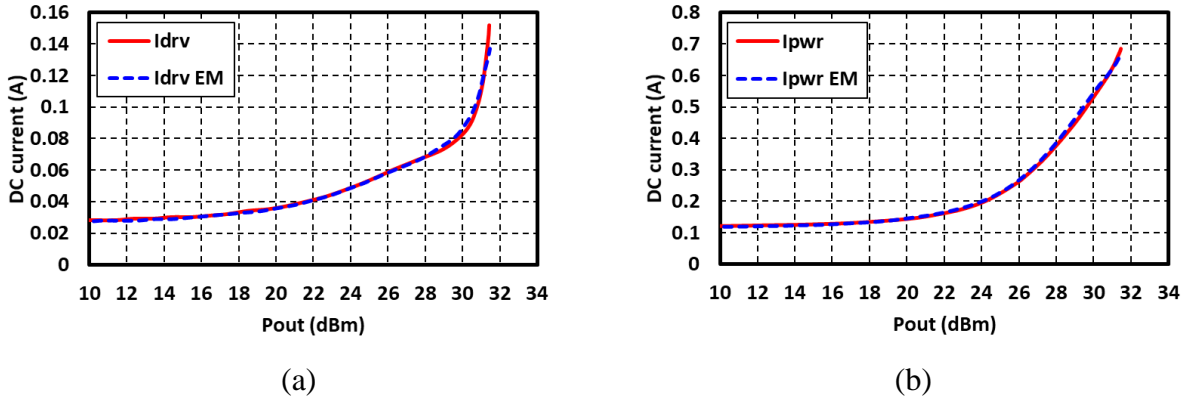


Figure 4.46 – (a) Driver and (b) Power stage DC drain current comparison between measurements and EM model.

Both driver and power measured DC currents show the same evolution as the PA model. The efficiency and gain profiles are examined next as shown in Figure 4.47(a) and (b) respectively.

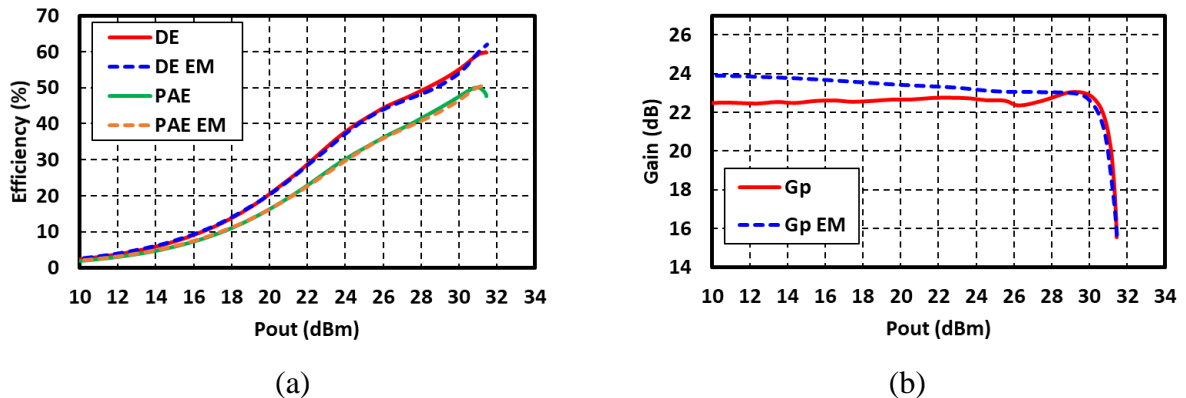


Figure 4.47 – (a) PAE, DE and (b) power gain comparison between measurements and simulation.

Once again, measurement results are very similar to the PA model. At 2.5GHz, the measured two-stage class-E DPA achieves a peak PAE of 50% at 31dBm of output power and 35% at 6dB of back-off. Meanwhile, the small-signal power gain is 22.5dB.

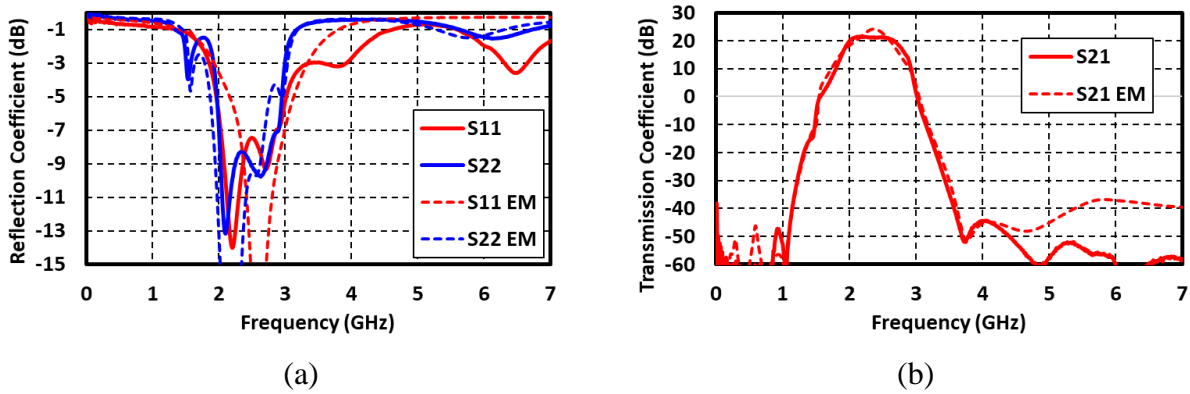


Figure 4.48 – (a) Reflection and (b) transmission coefficient comparison between measurements and simulation.

A final validation is done using the S-parameters. The plots in Figure 4.48 show the comparison between the simulated and measured S-parameters.

3.3 CW and LTE Performance

The two-stage class-E DPA is then measured from 2.1GHz to 2.5GHz using a CW input signal. For each frequency, the interstage capacitors are reconfigured so as to obtain a flat gain with a good back-off efficiency as shown in Figure 4.49(a).

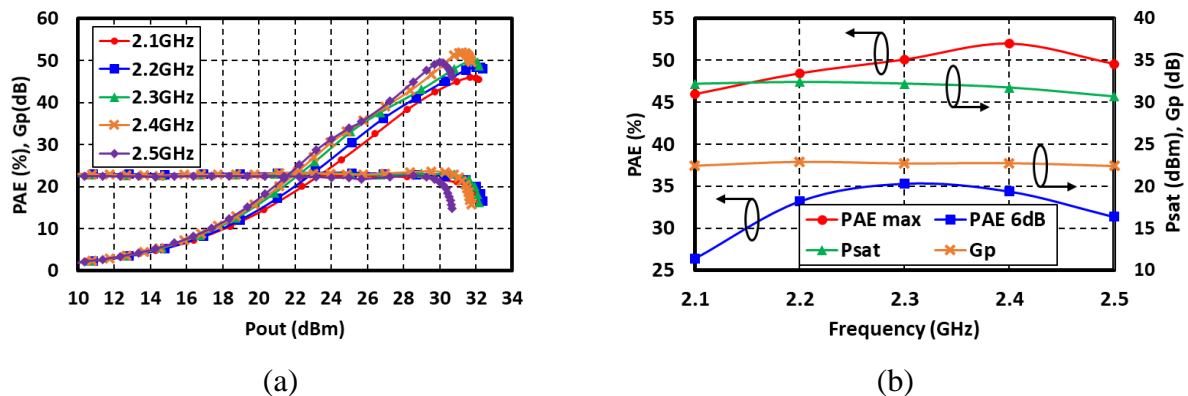


Figure 4.49 – (a) PAE and gain profiles at different operating frequencies. (b) Extracted power, efficiency and gain at different operating frequencies in CW mode.

The PA maintains higher than 31dBm of saturated output power (P_{sat}), and a peak PAE higher than 48% with relatively constant power gain over 17% of a fractional bandwidth around 2.3GHz as can be seen in Figure 4.49(b). Moreover, at 6dB BO, the measured PAE is higher than 36% at 2.3GHz.

Next, the PA is measured using a 10MHz LTE QPSK 50RB uplink signal (6.2dB of PAPR) on a 2.3GHz carrier while applying an instrument-based 7th order polynomial memory-less DPD. As shown in Figure 4.50(a), the PA achieves an E-UTRA ACLR of -35dBc for 28dBm of average output power with 43% of average PAE. This result is further illustrated Figure 4.50(b) which shows the output spectrum.

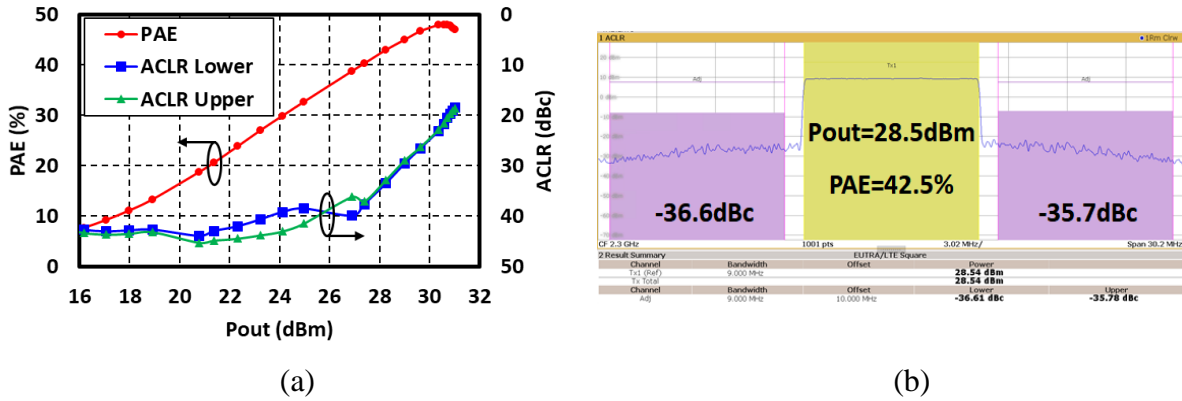
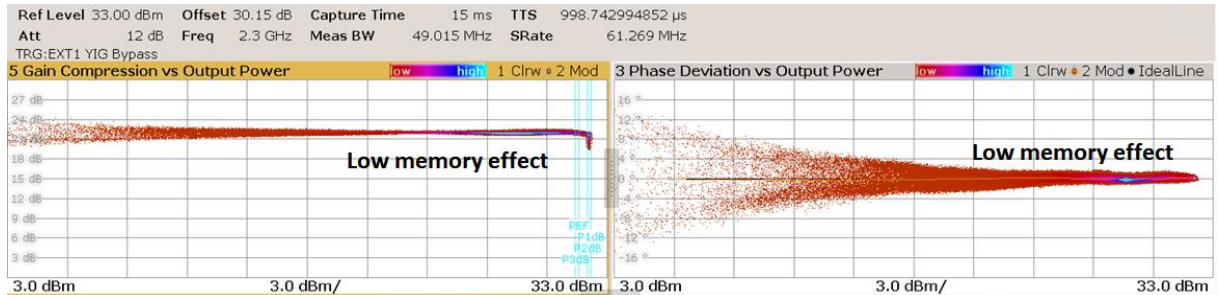
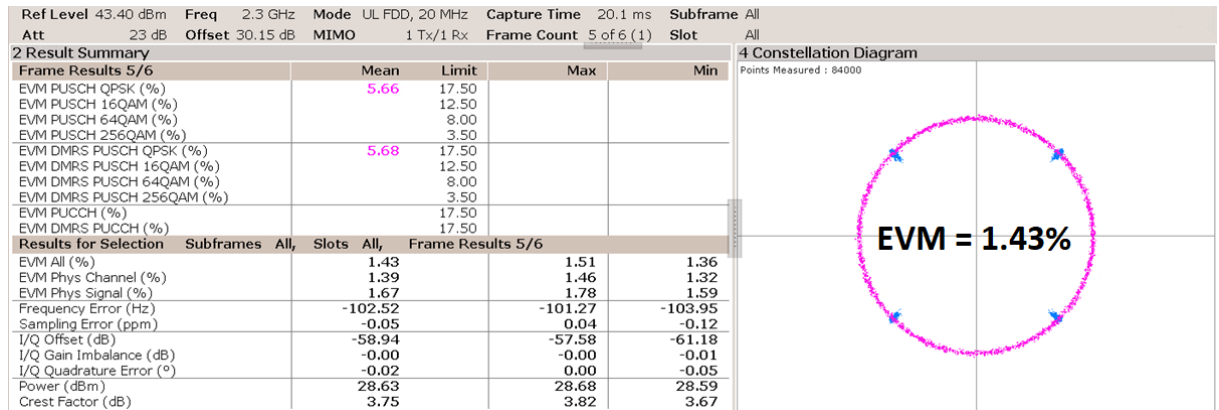


Figure 4.50 – (a) PAE and E-UTRA ACLR versus P_{out} measured at 2.3GHz using 10MHz LTE QPSK 50RB uplink signal with memoryless DPD and (b) Output Spectrum.

The flatness of the measured AMAM and AMPM characteristics of Figure 4.51(a) show that the DPA is linear and exhibits low memory effect. The in-band distortion is assessed using the EVM results of Figure 4.51(b). The QPSK constellation is clearly visible and the PA achieves a satisfying EVM level of 1.43%.



(a)



(b)

Figure 4.51 – (a) AMAM and AMPM and (b) output constellation measured at 2.3GHz using 10MHz LTE QPSK 50RB uplink signal.

Finally, the DPA performance with modulated signal is measured at different carrier frequencies ranging between 2.1 and 2.5GHz. Figure 4.52(a) shows that using the correct bias and capacitor states, a flat gain profile can be achieved for the different operating frequencies. The PAE curves are tightly grouped within a 10% variation interval.

In Figure 4.52(b) the PAE and output power are extracted at $ACLR = -35\text{dB}$ for the different carrier frequencies. The PAE is centred around 2.3GHz with a 17% fractional bandwidth while the output power decreases at higher frequency.

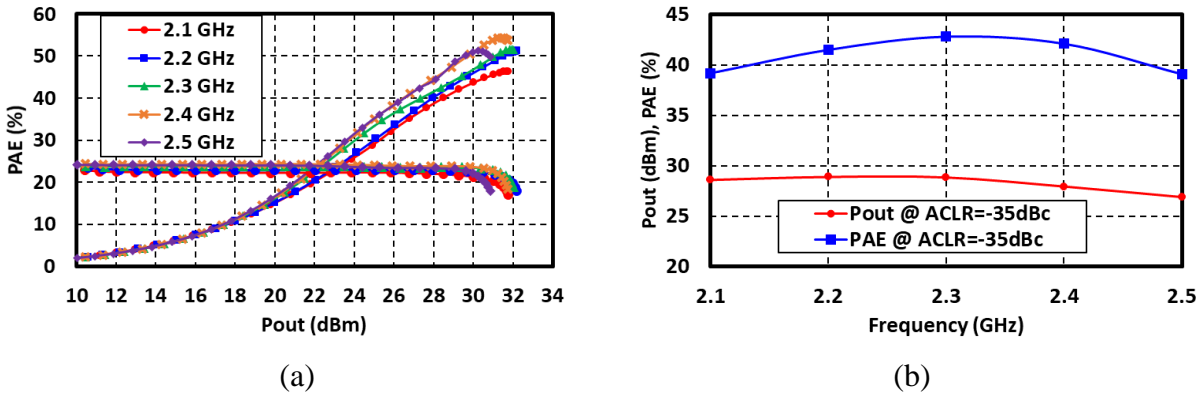


Figure 4.52 – (a) Measured PAE and G_p versus P_{out} and (b) PAE and P_{out} extracted for $ACLR=-35\text{dBc}$ at different frequencies using 10MHz LTE QPSK 50RB uplink signal.

The measurement results are compared to published LTE Doherty PAs in Table 4.5. Comparison to another LC combiner-based DPA architecture [42] shows that the proposed Class-E DPA circuit achieves higher efficiency operation both at peak and 6dB back-off. Furthermore, this work is capable of similar performance as other inverter-based, CLC combiner DPAs [43]–[45].

Table 4.5 – Comparison with the state-of-the-art LTE Doherty PAs.

		This Work	[42]	[44]	[43]	[45]
	Class (Main/Aux)	E/E	AB/C	AB/C	AB/C	AB/C
	Combiner Type	LC	LC	CLC	CLC	CLC
	Technology	SOI	InGaP	SOI	SOI	SOI
	Supply (V)	3.4	3.4	3.4	3.4	3.4
CW	Freq. (GHz)	2.3	2.5	2.5	1.95	2.3
	P_{sat} (dBm)	32	30	32.7	30.5	32.8
	PAE @ P_{sat} (%)	51	45	57	52	59
	PAE @ 6dB (%)	36	33	40	37	40
Modulated	Modulation	QPSK	QPSK	QPSK	-	QPSK
	BW (MHz)/RB	10/50	10/50	10/12	20/-	10/50
	Band (GHz)	2.1-2.5	-	1.9-2.7	1.55-2.3	1.9-2.7
	ACLR (dBc)	-35	-	-35	-30	-35
	P_{out} min/max (dBm)	26.9/28.9	-	28	-	28
	PAE min.max (%)	39.1/42.8	-	35/45	-	35/44
	DPD Linearization	Yes	Yes	No	Yes	No

4 Conclusion

In this chapter, a two-stage class-E Doherty PA was designed, fabricated, and measured in order to validate the Doherty combiner analysis method presented in Chapter 3.

The DPA power stage was designed first using the compact LC combiner. Class-E load pull power and efficiency contours were used to determine the ideal Class-E matching network q -factor. This was done by superposing the DPA load modulation trajectory with the Class-E PA load pull results obtained for different q values at peak and back-off operation points for the main and auxiliary amplifiers. Optimal performance was found for $q = 1$. The power stage was then matched to 50Ω terminations and checked for stability issues using the S-Parameters and the driving point admittance method. Next, a driver stage was added to the power stage and both blocks were connected through the inter-stage matching network. The final two-stage circuit design was tuned so as to present optimal performance.

The different levels of implementation technology were detailed. 130nm RFSOI was chosen for the IC which was to be mounted onto the package using copper pillars. Given the required CuP dimensions, a four-layer laminate μ PCB was selected as the packaging technology.

The designed elements of the DPA circuit are implemented onto the different technologies. The implemented circuit is then simulated using electromagnetic (EM) simulations in order to obtain more accurate results. The fabricated circuit is measured and validated by comparing its measured DC, SP, and CW results with those of the EM simulation model. Due to a fabrication process issue, the centre frequency is shifted downwards from 2.5GHz to 2.3GHz, and additional loss is introduced to the OMN stage. At 2.3GHz, the DPA saturation power is 32dBm and the peak PAE is 51%. At 6dB of back-off, the PA maintains a high efficiency of 36%.

Modulated signals measurements were done using a 10 MHz LTE signal with DPD. At 2.3GHz, the DPA delivers an output power of 28dBm with 43% of PAE for an ACLR level of -35dBc. Comparison with other published works shows that the DPA performance is in line with the state of the art, further validating the approach.

Chapter 5. Towards an Outphasing PA Transmitter System

1	Outphasing PA Design	103
1.1	Class-B OPA.....	103
1.2	Class-E OPA	106
2	DPD System Level Analysis	112
2.1	Look-Up Table Approach.....	112
2.2	Modelling-Based Approaches.....	114
3	PA Modelling	117
4	Conclusion.....	119

The Outphasing architecture can be regarded as the runner-up in terms of high efficiency load modulation PAs. While not nearly as popular as Doherty, this architecture is nonetheless a mainstay in all major PA publications. This is in part due to Outphasing's potential to become a major player in the age of digitalized FEMs. This chapter offers a look into the design and system analysis aspects of an Outphasing-based transmitter (OTX) integrating digital pre-distortion (DPD) directly into the SCS architecture.

In the following, the basics of OPA design will be discussed. Driving signal constraints and optimal operating conditions will be detailed in the case of both class-B and class-E OPAs.

Next, a general look into integrated DPD solutions is presented. This is done through a focus on the OTX system formalization required for advanced DPD analysis leading to a DPD architecture proposition referred to as In-SCS DPD.

Finally, some notes are given on the PA modelling efforts conducted within the time constraints of this work.

1 Outphasing PA Design

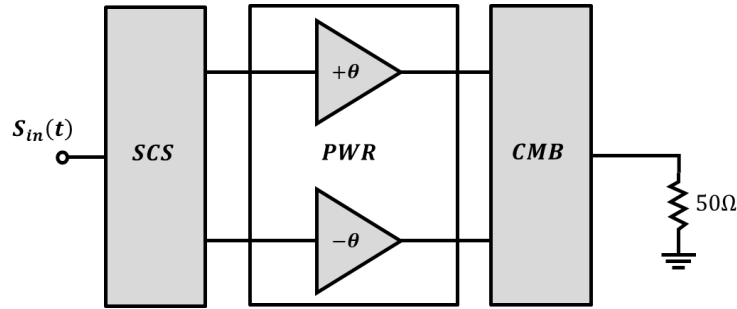


Figure 5.1 – Generic OPA block schematic showing its three main components.

A basic OPA system, such as the one seen in Figure 5.1, consists of three major components: The signal component separator (SCS), the power stage (PWR) comprising of the two PA cells/branches, and finally the combiner (CMB). Chapter 3 offered an in-depth analysis of OPA combiners, highlighting the required conditions to be respected for optimal Outphasing behaviour, and subsequently, high efficiency performance. In this section, the power stage design and operation are examined. Although there are many works detailing the design of RF and mmW Outphasing PAs, few actually give information about the driving signals required for their operation. A first study is conducted on a classic class-B OPA in order to understand some of the driving signal constraints. This is then followed up by a more complex modified class-E OPA design capable of providing superior performance.

1.1 Class-B OPA

When it comes to class-B OPA (OBPA), the required driving signals are not straightforwardly obtained. The architecture calls for the transistors to be treated as voltage sources, meaning that they must be at saturation point. However, due to load modulation, the driving voltage required to keep the transistors in saturation mode changes with every new load impedance value. The expression of the driving voltage can be obtained by first studying the OBPA behaviour.

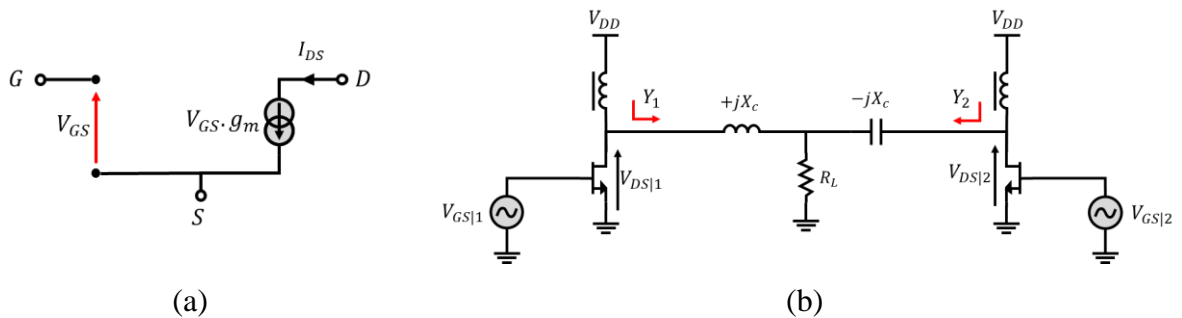


Figure 5.2 – (a) Ideal transistor model (b) Simplified OBPA with reactive compensation voltage combiner.

An ideal large-signal transistor model with linear transconductance g_m , Figure 5.2(a), is considered. In order to simplify the analysis, the following basic drain current equation will be used with V_{GSmax} as the maximum allowed gate voltage:

$$I_{DS}(t) = \begin{cases} 0 & V_{GS}(t) < 0 \\ g_m \cdot V_{GS}(t) & 0 \leq V_{GS}(t) \leq V_{GSmax} \end{cases} \quad (5.1)$$

As shown in [66], the driving voltage must be modulated in order to follow the variations of the perceived load and keep the transistor at saturation point. As a result, the gate voltage can be expressed as follows:

$$V_{GS|1,2}(t) = Y_{1,2} \cdot R_L \cdot V_{GSmax} \cdot e^{\pm j \cdot \theta(t)} \quad (5.2)$$

In the equation above, $Y_{1,2}$ refers to the voltage-mode admittance of the corresponding combiner circuit as shown in Figure 5.2(b). The normalized values of the gate and drain voltages are represented in the complex plane in Figure 5.3(a). Here it can be seen that while the gate inputs vary in both amplitude and phase, the voltages on the drain are of constant amplitude and only vary in phase by a factor of $\pm\theta$, thus fulfilling the Outphasing conditions at the inputs of the combiner.

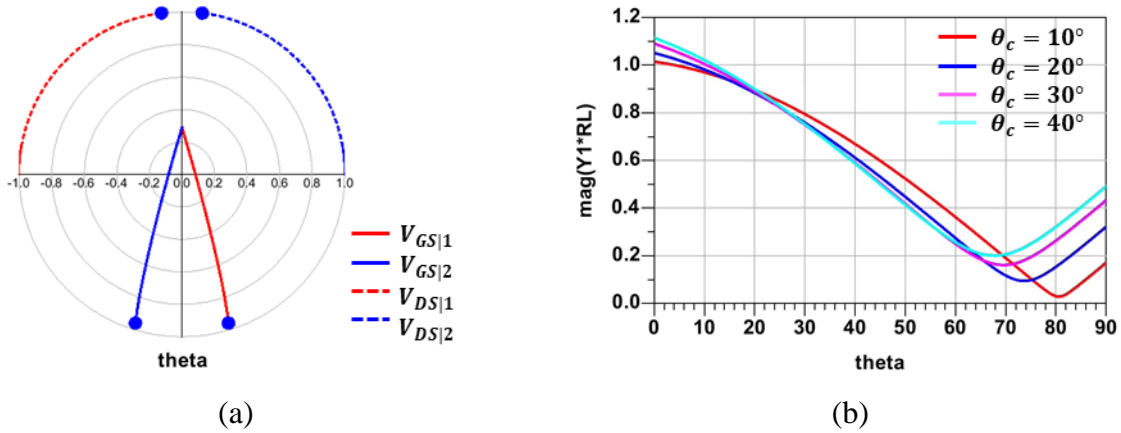


Figure 5.3 – (a) Complex plane representation of normalized drain and gate voltages (b) Normalized admittance magnitude for different compensation angle values.

When looking at the normalized amplitude of the input gate voltage in Figure 5.3(b), it can be seen that for low values of θ , it exceeds the maximum gate voltage V_{GSmax} . Therefore, the Outphasing angle cannot be swept from 0° , but instead from a starting threshold angle θ_s . This threshold angle, which varies depending on the compensation angle θ_c , is normally found using an empirical approach and was never defined analytically. The following section shows the analytical boundary condition that was calculated for improved OBPA design and resulted in a published work [67].

1.1.1 Outphasing Angle Boundary Condition

In order to keep the gate voltage from exceeding the V_{GSmax} value, the condition in (5.3) must be satisfied.

$$Y_{1,2}(\theta_s) \cdot R_L = 1 \quad (5.3)$$

In the case of a reactive compensation voltage combiner, the threshold angle is defined as:

$$\theta_s(\text{rad}) = \frac{1}{2} \cdot \arg \left(\frac{2 \cdot \overline{B}_c \sqrt{2 - \overline{B}_c^2} + j \cdot (2 \cdot \overline{B}_c^2 - 1)}{2 \cdot \overline{B}_c - j} \right) \quad (5.4)$$

$$\overline{B}_c = \frac{\sin(2 \cdot \theta_c)}{2} \quad (5.5)$$

By introducing this new boundary condition, the maximum allowed gate voltage is respected. However, this leads to a decrease in the maximum power delivered per branch since:

$$P_{OUT} = \frac{V_{max}^2}{2 \cdot R_L} \cdot \cos^2(\theta) \quad (5.6)$$

Under normal operation conditions, the maximum power is achieved for $\theta = 0$ and the PA is designed for this output value. When considering the threshold angle, the maximum deliverable power by the OBPA becomes:

$$P_{max} = \frac{V_{max}^2}{2 \cdot R_L} \cdot \cos^2(\theta_s) \quad (5.7)$$

Each branch is supposed to supply half of the total output power, therefore, in order to correctly size the power cells, a new maximum power per branch value is used.

$$P_{branchmax} = \frac{P_{max}}{2} \cdot \frac{1}{\cos^2(\theta_s)} \quad (5.8)$$

The optimal resistance value R_{max} can then be calculated using (5.9).

$$R_{max} = \frac{V_{max}^2}{2 \cdot P_{branchmax}} \quad (5.9)$$

Using this technique allows the design of an OBPA capable of supplying the required amount of power at θ_s without the risk of damaging the transistors by overdriving the gates. Figure 5.4(a) shows the case of an OBPA designed to deliver 2W output power. In the ideal voltage-mode, the maximum delivered power, corresponding to θ_s is slightly lower than the desired 2W, whereas the proposed design delivers this maximum power value at $\theta = \theta_s$.

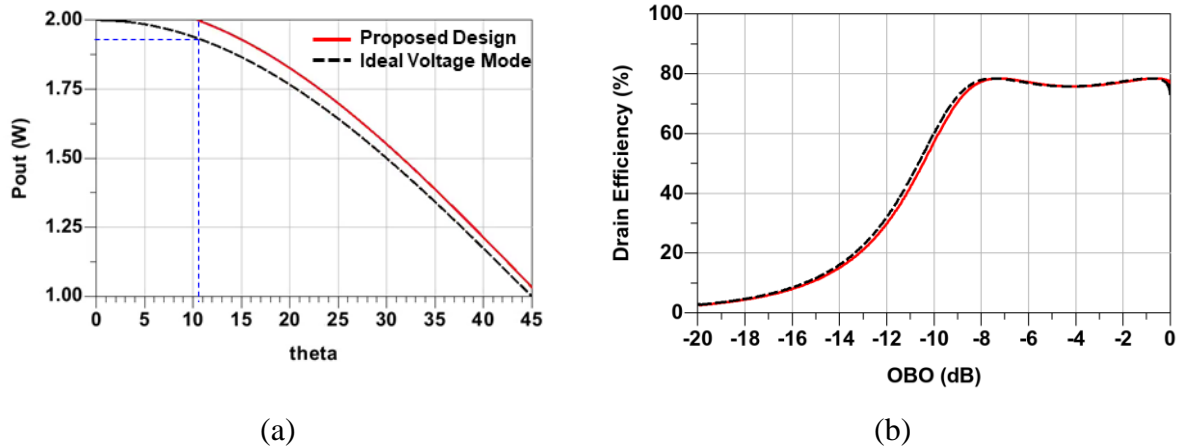


Figure 5.4 – (a) Output power and (b) efficiency evolution for ideal voltage-mode (dashed black) and the proposed OBPA design (red).

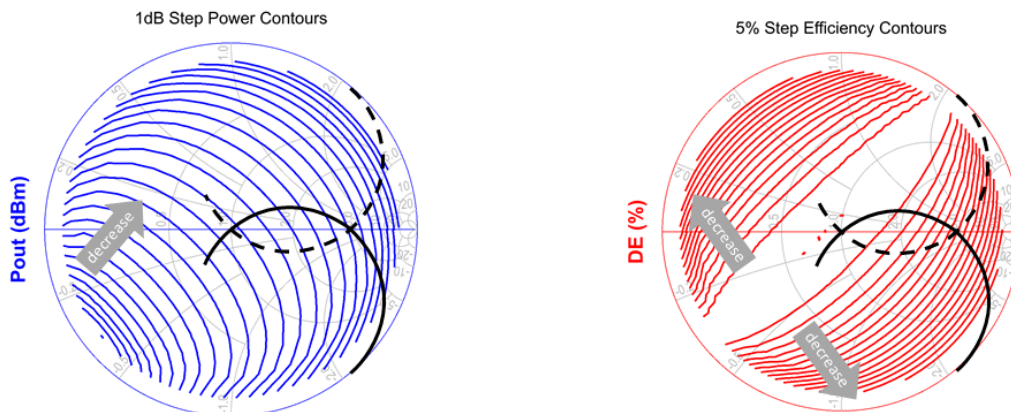
Finally, a consequence of this design method is the slight shift of the expected efficiency peaks with respect to output back-off level, as they are no longer defined as in (3.12), and are now calculated using (5.10) and can be observed in Figure 5.4(b).

$$OBO_{dB} = \begin{cases} -20 \cdot \log \left(\frac{\sin \theta_c}{\cos \theta_s} \right) \\ -20 \cdot \log \left(\frac{\cos \theta_c}{\cos \theta_s} \right) \end{cases} \quad (5.10)$$

Linear class power cells were heavily used during the early days of OPA design, but have since fallen in popularity and given way to switch-mode and continuous classes of operation. Class-E in particular has shown lots of promise when it comes to load modulated PA design, and will be explored next.

1.2 Class-E OPA

Using class-E power cells for OPA design comes with its own set of challenges. As seen in *Chapter 2 section 2.2*, class-E PAs require complex load impedances in order to keep optimal operation conditions at back-off. This however, is incompatible with the OPA combiner analysis conducted in *Chapter 3 section 1* where it is shown that the load impedances are purely resistive at the peak and back-off operation points.



(a) (b)

Figure 5.5 – Ideal switch-based $q=1$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with classic Outphasing load modulation schemes overlaid in black.

There are however, ways to overcome this apparent incompatibility, two of which will be discussed in the following subsections.

1.2.1 Offset Transmission Lines

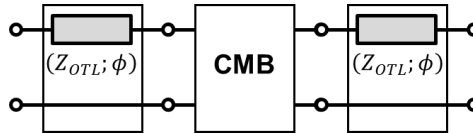


Figure 5.6 – Two-port representation of the Outphasing combiner with offset transmission lines.

The first method of adapting OPA load modulation to Class-E operation was proposed by Raab in [68] and [69] and involves adding offset transmission lines at the inputs of the Outphasing combiner as shown in Figure 5.6. In a typical Outphasing load modulation, the impedance trajectories intersect at two points on the real axis as shown in Figure 5.5. For the designed OPA to present two efficiency peaks, the two load trajectories must intersect on the optimal performance axis as in Figure 5.7.

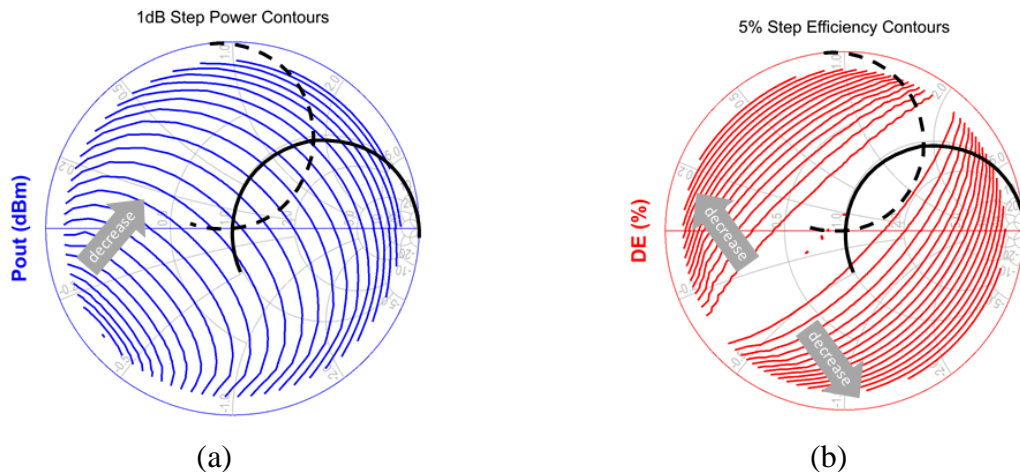


Figure 5.7 – Ideal switch-based $q=1$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with rotated OTL Outphasing load modulation schemes overlaid in black.

Such a result was achieved by Beltran and Raab who proposed the use of offset transmission lines at the inputs of a delay line compensation voltage combiner [68] as well as a transformer-based variation of the reactive compensation voltage combiner [69]. While their works show the possibility of producing such load modulation schemes, they give no indication on the driving signals or the drain voltage/current that would be required. An analysis was therefore conducted in order to determine the required driving conditions for any generic OPA-compatible combiner. The details of this study are provided in *Appendix C* which shows how to design an OPA combiner for any target peak and back-off impedance values.

The main drawback of this method is its reliance on transmission line structures which are impractical from a circuit integration point of view, especially when dealing with sub-6 GHz frequencies. Moreover, the addition of these extra components will inevitably lead to more loss

in the output stage since integrated components have low quality factors as demonstrated in Chapter 4 section 2.1.1.

1.2.2 Load-Pull Contours Rotation

Another possible solution to the class-E load modulation problem is to rotate the load-pull contours themselves instead of rotating the load modulation trajectories. This technique was first proposed by Ghahremani in [70], and relies on tuning the duty cycle d and resonance factor q of the class-E PA in order to optimize its efficiency over the required range of output power.

In [36], the authors show that class-E PA load-pull contours can be rotated clockwise by increasing the value of the resonance factor q . The duty cycle d was shown to have the opposite effect, and therefore a number of different combinations of these two design factors could result in the same rotation of the contours. This property could be used to the designer’s advantage in order to rotate the optimal performance load line and place it in on the real axis. In doing so, there would be no need to modify the Outphasing combiners to intersect at complex values as the optimal performance would require real impedance at both peak and back-off output power levels.

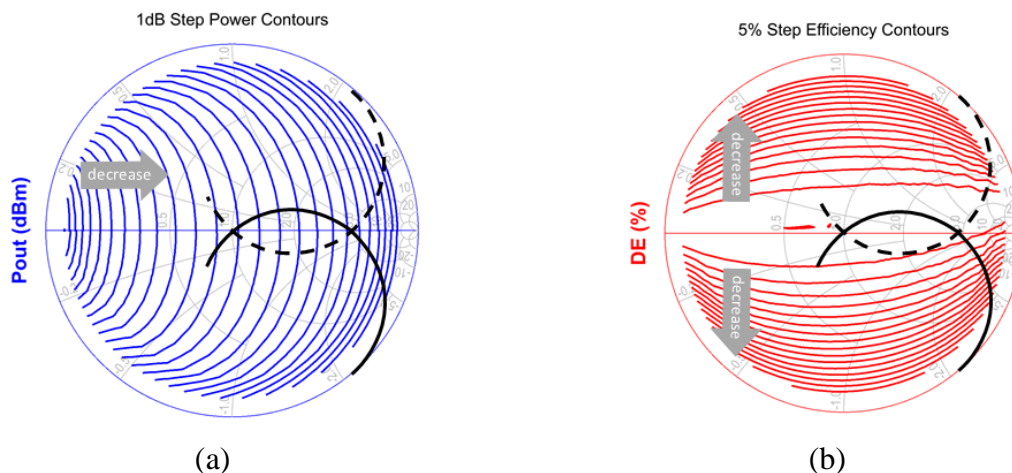


Figure 5.8 – Ideal switch-based $q=1.3$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with classic Outphasing load modulation schemes overlaid in black.

The contours in Figure 5.8(a) and (b) show the power and efficiency contour rotations when q is increased to 1.3 with $d = 0.36$. The load modulation intersections now lie on the high efficiency contours while having different output power values which results in the target OPA performance.

The load-pull contours rotation method for class-E load modulation is more desirable from an integration point of view, as it requires less elements making it a more compact solution that is less likely to experience power loss. However, real transistor operation is much more complicated, as there are switching losses, switching delays, and capacitive and inductive parasitic components to be taken into account.

To better illustrate these issues, a dual input class-E OPA (OEPA) is designed and simulated, using non-ideal transistor models capable of giving more accurate results. The OEPA is designed with the following input variables:

- Transistor type 130nm RF-SOI LDMOS
- Centre frequency $f_0 = 2.5GHz$

- Supply voltage $V_{DD} = 3.4V$
- Maximum output Power $P_{max} = 33dBm$

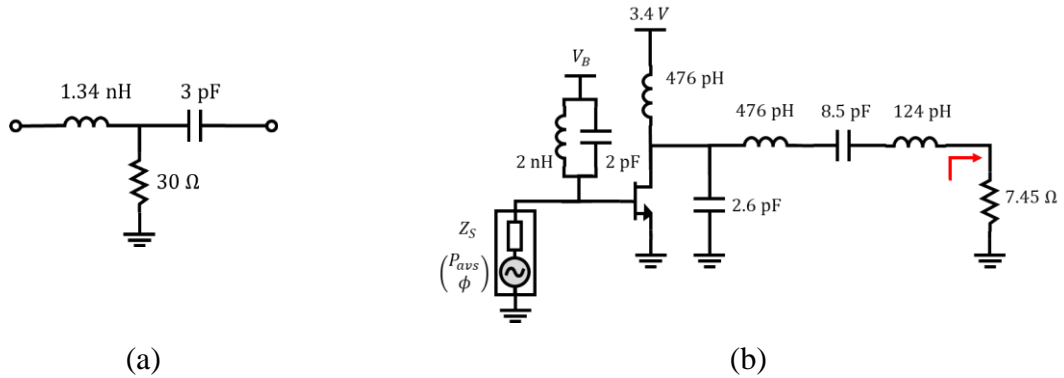


Figure 5.9–(a) Reactive compensation combiner schematic, (b) Class-E power cell schematic with red arrow marking complex load modulation plane.

The RCC combiner circuit shown in Figure 5.9(a) is chosen once again, this time with a compensation angle value of $\theta_c = 22.5^\circ$ in order to achieve high back-off OPA operation. As per the load-pull contours rotation technique, the class-E power cells are designed with a resonance factor $q = 1.3$. The resulting class-E PA schematic from Figure 5.9(b) is placed in a load pull simulation where the complex value of the load presented after the red arrow is swept and the PA’s output power and PAE contours are plotted. In the ideal class-E switch simulations, only the complex load Z_L was swept and the input driving signal was kept constant. Here however, as a single-tone input class-E is used, the power $P_{avs|dBm}$ is also swept, and as a result, each set of contours corresponds to a single input power value. Therefore, if we are to estimate the performance of the class-E power cell in an Outphasing configuration, the load pull contours must be checked at both maximum output power as well as the OBO. Figure 5.10 shows the output power and PAE contours for $P_{avs|dBm} = 23.5dBm$. The ideal Outphasing load modulation trajectories corresponding to the combiner of Figure 5.9(a) are overlaid in black. The first efficiency peak, which occurs near the maximum power value is indicated by the green cross and shows that each branch can provide an output power of 30dBm with $PAE \approx 68\%$.

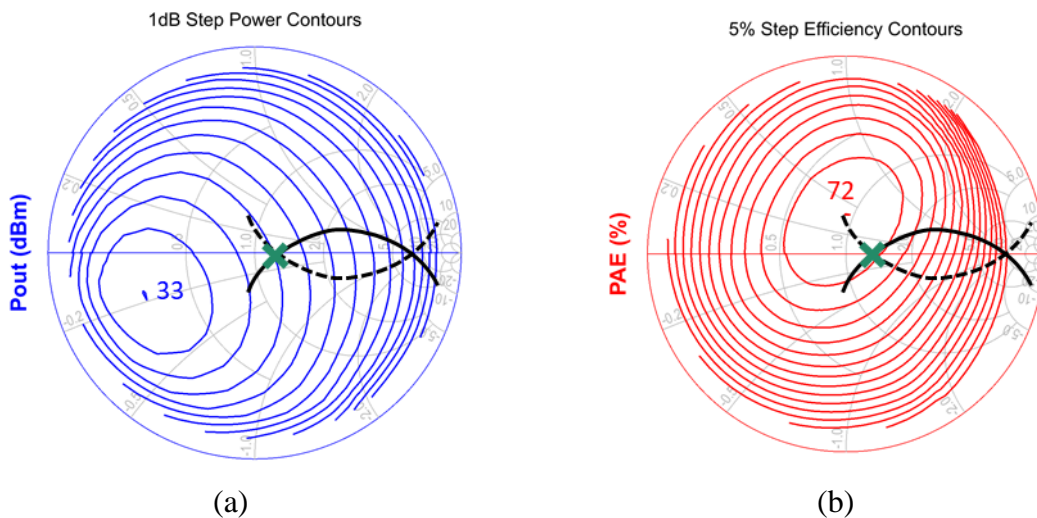


Figure 5.10 – Load-pull contours at $P_{avs|dBm} = 23.5dBm$ (a) Power contours, (b) PAE contours.

For an input power $P_{avs|dBm} = 13dBm$, the OPA is assumed to be at its second efficiency peak. The corresponding power cell load pull contours are plotted Figure 5.11 and once again overlaid with the same load modulation trajectories. This time, the green cross indicates the location of the second efficiency peak, and shows that each power cell provides 21dBm of output power with $PAE \approx 41\%$.

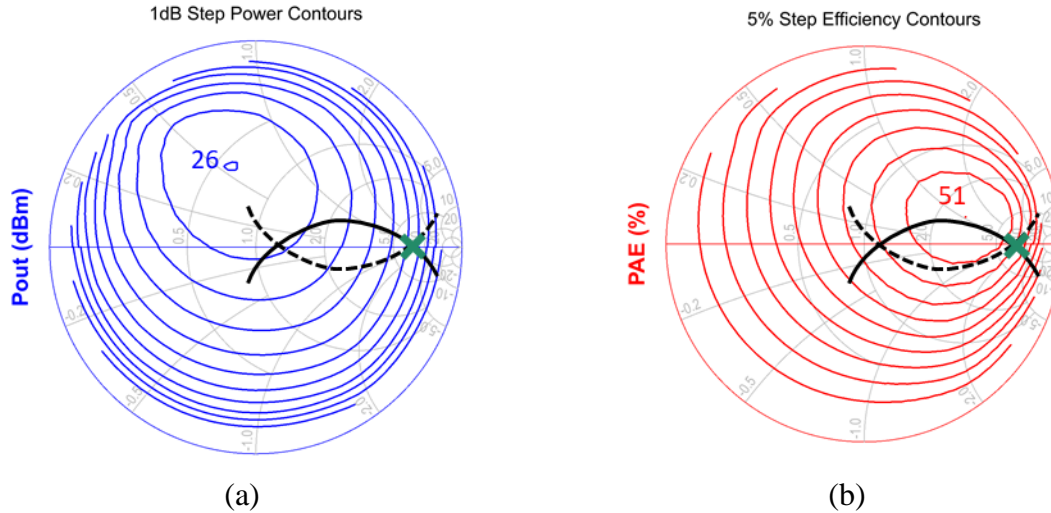


Figure 5.11 – Load-pull contours at $P_{avs|dBm} = 13dBm$ (a) Power contours, (b) PAE contours.

Given these encouraging load-pull results, the OEPA circuit can therefore be designed using the previously selected combiner and power cell. The inductor and capacitor of the combiner can be merged with the series elements of the class-E power cells giving the dual input circuit of Figure 5.12.

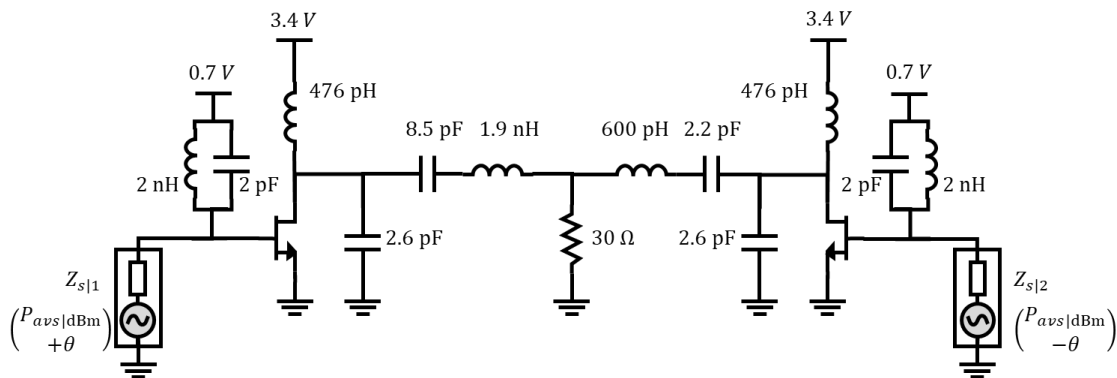


Figure 5.12 – Dual input OEPA schematic.

The above circuit is simulated by sweeping the input power and phase difference between the two branches resulting in the scatter plots of Figure 5.13. Each dot represents a $(P_{avs|dBm}; \theta)$ couple value. Stable operation points are coloured red while potentially unstable points are shown in grey.

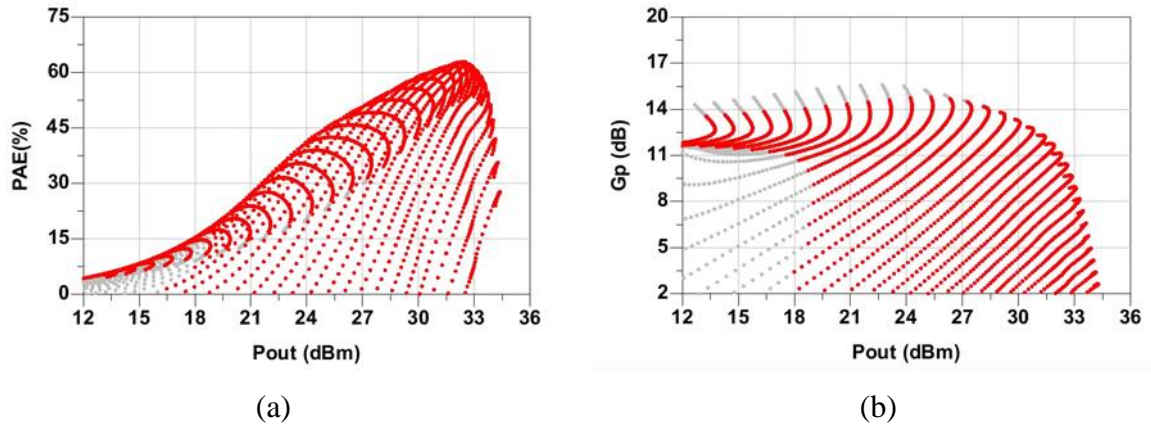


Figure 5.13 – Possible (a) PAE and (b) power gain performance versus output power for different values of θ in OPA operation for $q = 1.3$. Potentially unstable points are shown in grey.

Looking at the envelope of the PAE points, for an output power level of 33dBm (corresponding to two 30dBm power cells) the efficiency value is 65%. At 24dBm, this value becomes 48% which is aligned with the load pull simulation estimations. The associated gain profile can be obtained by extracting the operating points corresponding to the maximum efficiency envelope from the power gain scatter plot as shown in Figure 5.13(b). Looking back at these scatter plots, it can be seen that the high efficiency profile is only one of many possible configurations, as different points of operation can be chosen in order to better suit the desired application. More importantly, the choice of operation points could be used as a way to ensure linear PA operation and as a result fulfil the same function of a predistortion circuit block. This will be further explored in *section 2.1*.

With that in mind, the next section will take a look at the OPA from a systems perspective and provide the formalism for integrating digital predistortion (DPD) directly into the Outphasing transmitter system (OTX).

2 DPD System Level Analysis

In order to propose a DPD model as relevant as possible for the OPA, it is necessary to study in detail its architecture from a signal point of view in order to propose an adequate PA model. Figure 5.14 shows the conventional block diagram of an OPA from a signal processing perspective.

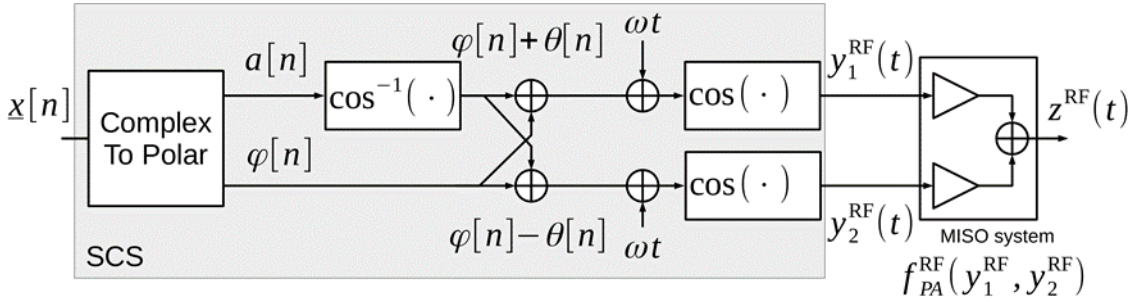


Figure 5.14 – Conventional (signal) diagram of an OPA.

It exhibits the sampled complex baseband signal $x[n]$ (obtained from the original IQ signals modulation), its conversion into polar coordinates ($a[n]$ and $\varphi[n]$) and the conversion of the amplitude into an Outphasing angle $\theta[n]$. The combination of the baseband phase $\varphi[n]$ and the Outphasing angle $\theta[n]$ is a baseband representation of the signal. Addition of the carrier phase ωt and the cosine modulation represent a frequency transposition to RF domain. The RF signals $y_1^{\text{RF}}(t)$ and $y_2^{\text{RF}}(t)$ are constant amplitude and modulate the transistors in Outphasing manner. The OPA power and combiner stages are represented by the multiple input single output (MISO) system. Their behaviour can be described by the function $f_{PA}^{\text{RF}}(y_1^{\text{RF}}, y_2^{\text{RF}})$ which performs the amplification and reconstruction of the modulated RF signals resulting in the final amplified output signal $z^{\text{RF}}(t)$.

The block that converts the baseband complex signal to the two outphased constant amplitude signals is usually called the *signal component separator* (SCS). The material implementation of an SCS bloc is out of the scope of this work. The SCS description is therefore limited to a signal processing perspective. The main reasons behind this decision are the fact that SCS blocs are designed for a specific PA implementation and thus limiting reusability. Furthermore, the SCS function itself is composed of very non-linear signal processing elements which makes its implementation challenging [71], [72].

With the OPA system clearly defined, linearization methods can be more easily discussed and formalized, starting with the look-up table (LUT) approach.

2.1 Look-Up Table Approach

This first approach is based on an exhaustive characterization of the operating configurations in CW mode. Using the designed dual input OPA schematic from Figure 5.12, one can sweep the Outphasing and power values of the sinusoids and extract from these CW simulations the PAE and gain performance of the system as was done in Figure 5.13.

By defining a selection criterion based on the PAE, the gain and/or P_{out} , it is therefore possible to define a trajectory in these point clouds, where each point is defined by a very precise couple $\{P_{avs}, \theta\}$. For example, Figure 5.15(a) results from the selection of points which maximize the

PAE for a given value of P_{out} . The associated gain profile resulting from this selection is plotted in blue and shows a 3dB dip at high power. Similarly, the selection criterion can be instead based on the gain profile in an attempt to keep it at a constant value and thereby decreasing AMAM distortion. This results in the performance profiles of Figure 5.15(b), where it can be seen that the gain value is kept at 12dB until the eventual gain collapse at the saturation power level.

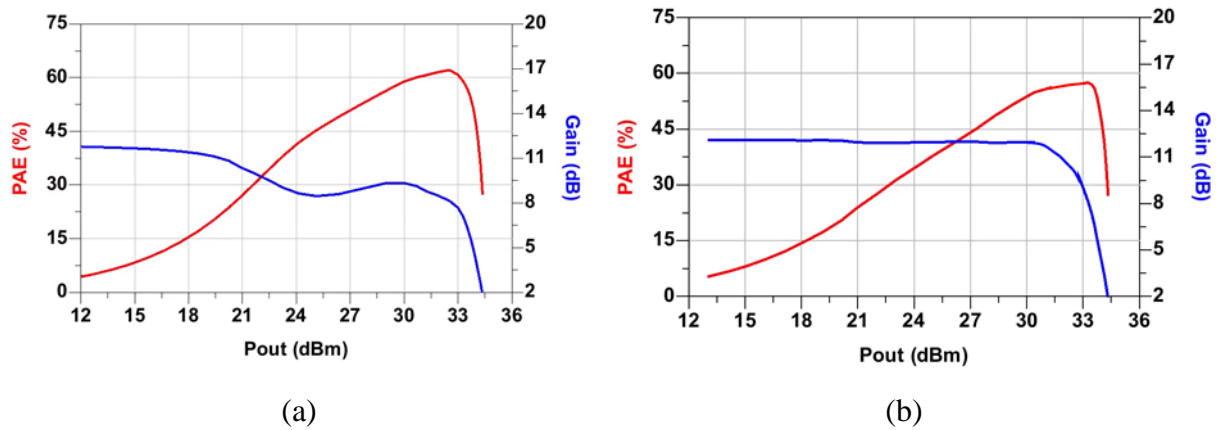


Figure 5.15 – PAE and gain profiles versus output power extracted from the OEPA simulation using (a) maximum PAE criterion, and (b) constant gain value $G_p = 12\text{dB}$ criterion.

It can therefore be deduced that by defining a list of values of couples $\{P_{avs}, \theta\}$ a predistortion LUT can be formed as shown in Figure 5.16.

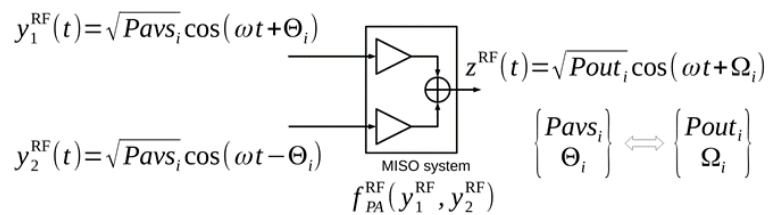


Figure 5.16 – Signal representation of LUT approach for dual input OPA.

This mode of operation can be assimilated into the original OPA block diagram of Figure 5.14 as described in the diagram of Figure 5.17 below.

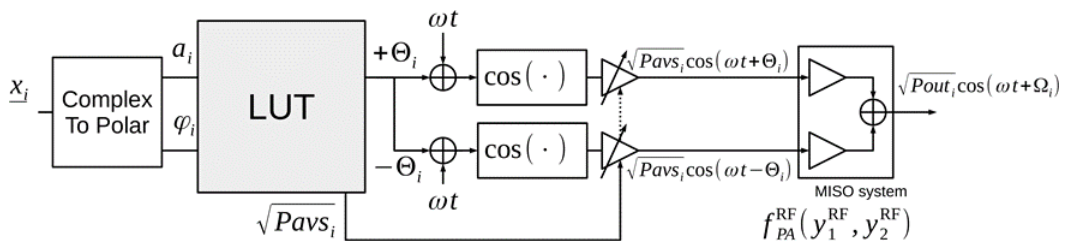


Figure 5.17 – LUT-based DPD integrated in OTX system.

The most notable change from the conventional SCS architecture is the inclusion of amplitude modulation at the two inputs of the power stage which is done through the addition of a variable gain amplifier (VGA) to each branch. This can be justified by the fact that the power cells experience load modulation and as a result, their inputs must also be modulated in order to maintain the transistors at saturation as was shown in *section 1.1*.

Finally, it is important to note that while not discussed here, phase characterization of the OPA is also important and can be used as a criterion for selecting $\{P_{avs}, \theta\}$ couples that minimize both AMAM and AMPM distortions while providing high efficiency operation.

This LUT-based approach, while practical for assessing the potential linearity of an OTX system is, at least in this simplified form, not very suitable for modern modulations containing heavy amplitude and phase modulation. A more consistent approach is the so called behavioral models which are showcased in the next section.

2.2 Modelling-Based Approaches

Digital predistortion and PA modeling are two closely related research areas. Indeed, to linearize an amplifier, it is essential to understand its nonlinear behavior. We therefore use behavioral models in the field of DPD. We will explain the classical strategy of PA behavioral modeling for DPD and then, we will present the methodology that we have implemented and the results obtained.

Looking back at the block diagram of Figure 5.14, the MISO system representing the dual input OPA can be described by a function f_{PA}^{RF} which uses the two input signals $y_i^{RF}(t)$ to model the output signal $z^{RF}(t)$. It can be assumed that this non-linear function is, a priori, with real coefficients because y_i^{RF} and z^{RF} are real-valued signals. However, instead of determining f_{PA}^{RF} directly, the conventional approach is to instead determine the baseband model denoted f_{PA} . Introductory elements of baseband modelling are further developed in *section 3* of this chapter.

The interest of baseband modeling is that the sampling frequency to represent the signal (and the system) is much lower than in the case where the carrier must also be sampled. This has the consequence that baseband simulations are extremely faster than RF simulations, where the carrier signal must be taken into account. Of course, this modeling comes at the price of a loss of information (the harmonics); but this loss of information will in practice be negligible. The PA and DPD models used in this work are therefore baseband and complex-valued.

The block diagram of Figure 5.14 requires an adjustment to be compatible with a baseband modelling of the PA and the resulting baseband block diagram is shown in Figure 5.18.

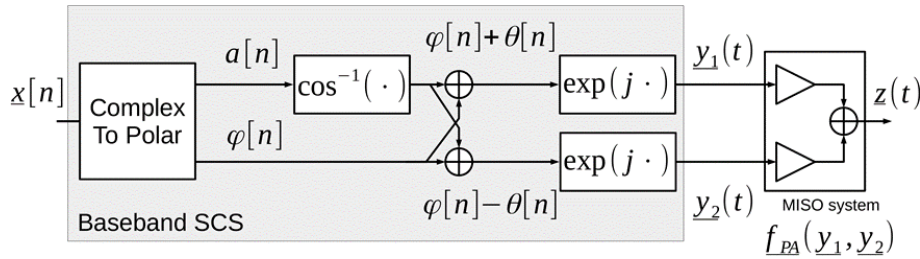


Figure 5.18 – Equivalent baseband signal diagram of the conventional OPA.

The validity of this representation is proven by the equation below.

$$y_i^{RF}(t) = \Re \{ \underline{y}_i(t) e^{j\omega t} \} \quad (5.11)$$

The inputs and outputs of the function f_{PA} are complex-valued, leading to the assumption that it has complex-valued coefficients too.

The simplest approach to DPD system modelling, is to ignore the PA circuit structure. Only the baseband signal $\underline{x}[n]$ at the input of the SCS and the sampled output of the PA $\underline{z}[n]$ are considered, as shown in Figure 5.19.

In this modelling case, all the classic DPD techniques apply straightforwardly since a classic DPD structure can be recognized as shown in Figure 5.20; the system is therefore expressed using only single input single output (SISO) functions. Instrument-based DPD using a signal generator with a feedback loop can therefore be used.

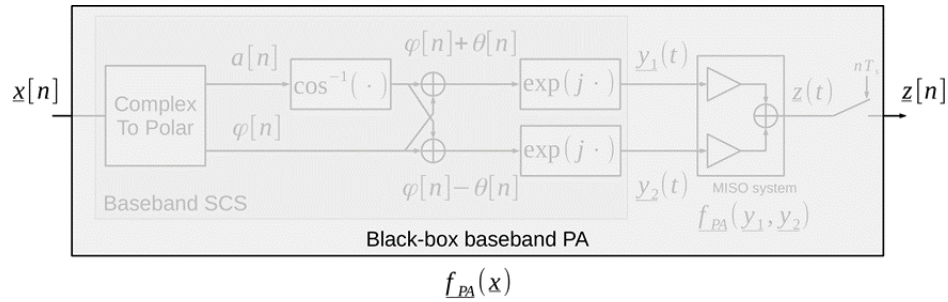


Figure 5.19 – SISO basedband OPA model representation.

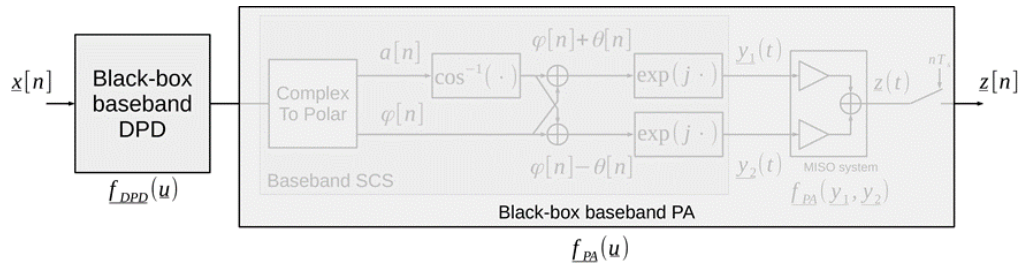


Figure 5.20 – SISO basedband DPD model representation.

This approach, while being the easiest to implement has the drawback of giving little to no information on how to optimize the OTX. Given that it is SISO-based, it is impossible to tell if the system distortion is a result of the combination mismatch, the amplification stage, or even the signal decomposition.

The DPD of OPAs is a research topic with very strong potential from a modeling and signal processing point of view. This is because the architecture can be modeled at different levels of abstraction; each level of abstraction offering multiple research options. One of the most difficult parts of this work was to understand how to integrate the DPD block into the SCS block and to formulate the identification problem in the usual DPD formalism. This understanding has resulted in the definition of a promising DPD architecture for OPAs.

2.2.1 In-SCS DPD Architecture

The operation of the proposed architecture is based on that of indirect learning DPD architecture (ILA) [73]. The subject of DPD based on ILA being very vast, only one essential point of this technique will be retained: when the input and output signals of the system to linearize are known, and the system is modeled by a *linear-in-parameters* model, the calculation of the DPD comes down to a simple matrix inversion.

The main theory of indirect learning relies on the fact that, for a given nonlinear system, its post-inverse works quite well as a pre-inverse. Figure 5.21 illustrates the two possible configurations in the case of a MIMO modeling of the OPA. However, it should be noted that

this modeling could be difficult to implement from the hardware point of view. Indeed, to calculate the post-inverse, it is necessary to know the signals \underline{z}_1 and \underline{z}_2 at the output of each PA and the sampling of these signals could greatly disturb the load modulations and the recombination of the signals. A more interesting solution would be to integrate the DPD directly into the SCS block, thereby leveraging the inherent digital friendliness of the OTX.

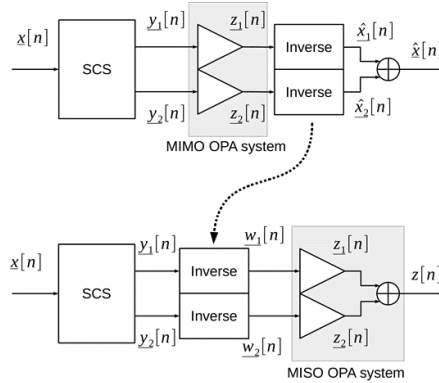


Figure 5.21 – OTX diagram showing how the post-inverse can be used as a pre-inverse.

This can be achieved by decomposing the SCS block into two main parts as shown in Figure 5.22: a $\mathbb{C}2\text{Pol}$ block which separates the complex baseband signal into its two components (modulus and angle) and a *Polar Outphasing (phase) modulator* (POM) which calculates the modulation angles and generates the associated baseband signals. The pre-inverse block can now be inserted inside the SCS between the $\mathbb{C}2\text{Pol}$ block and the POM block.

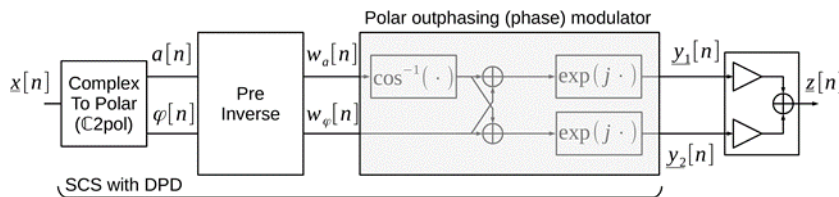


Figure 5.22 – Pre-inverse configuration of the In-SCS DPD architecture.

Although this structuring of the DPD is very natural, there remains an important element to specify: the positioning of the associated post-inverse, required for the calculation of the pre-inverse. Figure 5.23 shows how the post-inverse can be extracted, by taking the complex output $\underline{z}[n]$ of the PA and generating the required amplitude and phase $\hat{a}[n]$ and $\hat{\phi}[n]$ respectively which are considered equal to $a[n]$ and $\phi[n]$ in the context of ILA DPD; in this case, the inverse function is MIMO.

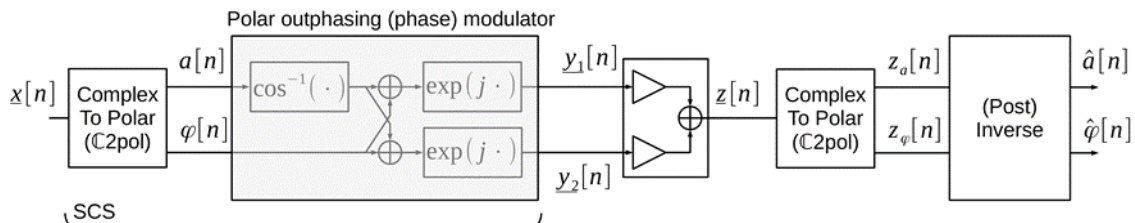


Figure 5.23 – Associated post-inverse configuration of the proposed In-SCS DPD architecture.

Through this formal presentation of the DPD problem, the integration and identification of the DPD in the SCS block of the OPA becomes feasible. With the DPD system architecture determined, the final piece required for full OTX system simulations is the actual PA model.

3 PA Modelling

Modeling amplifiers requires understanding what behavior amplifiers exhibit and the cause of that behavior. We summarize briefly the main points here but encourage the reader to refer to Ghannouchi's book [74] for an in-depth presentation and analysis.

The objective of the behavioral modeling of the amplifier is to find the equation which links the input signal RF_{IN} and the output signal RF_{OUT} . Amplifier characterization analysis have highlighted three main categories of distortion:

- static non-linearities (mainly due to the DC characteristics of the transistor)
- short-term memory effects (attributed to frequency responses of matching networks and parasitic elements of the transistor)
- long-term memory effects (attributed for example to effects in the semiconductor (trapping effects) and to transistor temperature variations)

To obtain good quality linearization, it is necessary to compensate for these different effects. The main challenge of behavioral modeling is to find models that are precise but of low computational complexity in order to guarantee “easy” use.

One of the essential points of the behavioral modeling of amplifiers is to assume that the signal is band-limited. The case of interest consists in neglecting the harmonics of the RF signal and considering only the signal around the fundamental of the carrier. And more precisely, the original idea is that a real narrow-band RF signal centered around a frequency F_c can be completely represented by an equivalent (complex-valued) signal centered at DC. If we denote $u_{RF}(t)$ the narrowband RF (“bandpass”) signal, we obtain its complex equivalent in baseband (lowpass) $u_{BB}(t)$ by the following equations:

$$\begin{aligned}
 u_{RF}(t) &= A(t)\cos(\omega_c t + \varphi(t)) \\
 &= \Re\{A(t)e^{j(\omega_c t + \varphi(t))}\} \\
 &= \Re\{u_{BB}(t)e^{j\omega_c t}\}
 \end{aligned} \tag{5.12}$$

Where

$$u_{BB}(t) = A(t)e^{j\varphi(t)}, \tag{5.13}$$

and $A(t)$ and $\varphi(t)$ represent the amplitude and phase modulation signals; ω_c is the angular frequency of the RF carrier.

The conventional approach to extract a baseband PA model consists in characterizing it with a modulated signal. The measurement of the (baseband) input and output waveforms are then used to build a so-called “black box” model (a mathematical expression) whose sole purpose is to predict the value of the output samples. The model is usually constructed using a chosen type of model structure such as memory polynomials (MP), generalized memory polynomials (GMP), or dynamic deviation reduction (DDR) to name a few. The ability to model the output is evaluated by exhaustively testing different values of memory depth and orders of non-

linearity which can be referred to as the model dimension. The algorithm flow chart in Figure 5.24 from [75] details this methodology.

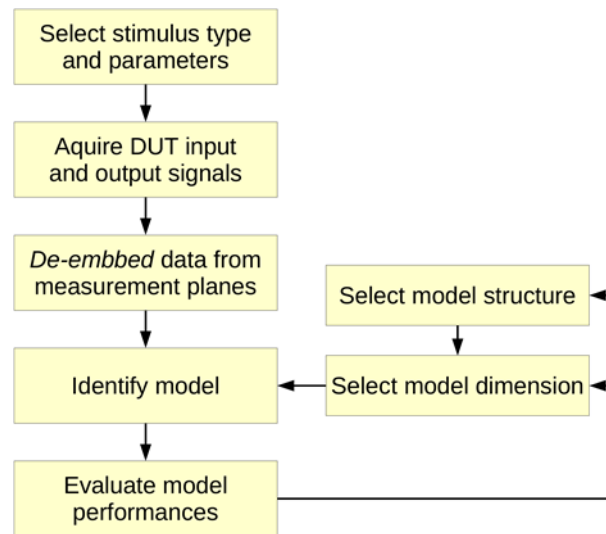


Figure 5.24 – PA behavioural modelling flow chart.

Within the framework of this work, for reasons of simplicity and time constraint, the model which is planned to be used is the memory polynomial (MP) whose expression is:

$$y[n] = \sum_k \sum_m a_{km} \cdot x[n - m] \cdot |x[n - m]|^{2k} \quad (5.14)$$

The choice of this model is motivated by the following practical and scientific considerations:

- we already have a robust and fast implementation of the model on Matlab,
- the notoriety of the model makes it a mandatory model,
- we will use a more advanced model when we have demonstrated the MP model limitations in our specific case

As noted earlier, PA modelling requires extensive measurement data. Unfortunately, due to time restrictions and supply chain disruptions, an OPA based IC could not be made available on time.

One of the possible fallback options, was to use the ADS design model and simulate the OPA with the different required input signals. However, this solution proved to be harder to implement than initially thought. The reason behind this lies in the fact that PA modelling requires modulated signals which must then be mathematically transformed as they would be by the SCS block. Attempting to accomplish this in the ADS environment would require considerable time and resources. Nonetheless a potential solution which utilizes Matlab and ADS was proposed but is pending experimental validation.

4 Conclusion

In this chapter, the Outphasing load modulation PA architecture was explored. A first study was conducted using an ideal transistor model in a class-B OPA architecture with a reactive compensation voltage combiner (LC combiner). This was then followed by a class-E OEPA implementation that introduced two different forms of optimization: The first, built on the work done by Beltran and Raab, uses offset transmission lines in order to provide the PA with the required complex load at OBO. The second, put forth by Ghahermani, uses the design parameters of the class-E power to rotate the power and efficiency load-pull contours and therefore make the optimal back-off impedance real.

Next, a dual-input load modulated class-E OPA was designed using an LDMOS electrical model to provide 33dBm of output power at $f_0 = 2.5GHz$. The OEPA was simulated with different input power levels as well as branch phase mismatch $\pm\theta$. This extra degree of freedom was then leveraged to better control the operation of the OPA, providing a rudimentary method for increasing linearity through predistortion.

In order to better understand and analyse the system requirements of an Outphasing-based transmitter (OTX), a system level analysis was conducted. The SCS, OPA, and DPD blocks were represented and studied from a signal processing perspective, leading to two DPD architecture propositions. The first is the look-up table (LUT) based approach: it uses extensive CW characterization of the RF OPA circuit in order to build an LUT of input power and phase values which satisfy a predetermined performance criterion such as high efficiency operation, or high linearity. The second architecture is more advanced and relies on the PA's behavioural model. This method, referred to as In-SCS DPD is based on the indirect learning DPD architecture and determines a post-inverse block of the OPA MISO system in order to use it as a pre-inverse and thus linearize the OTX system.

Finally, the PA modelling process is briefly exposed and a memory polynomial (MP) type model is chosen as the starting point. Building the PA model requires extensive measurements using modulated signals. Unfortunately, an OPA IC couldn't be realized within the time constraints of this work. This section therefore serves as the foundation for future work on OTX systems.

Although very theoretical, the work carried out and presented in this chapter constitutes an essential foundation for the integration of the DPD in the OPA architecture. We have formalized the problem of the DPD in-SCS which makes it possible to easily calculate the inverse using a matrix inversion; these theoretical developments are, to the author's best knowledge, not present in any of the current literature on the subject.

Conclusion & Future Work

This work presented the context and evolution of cellular communication standards which, in their fifth generation, require more complex PA architecture in order to operate efficiently.

The first chapter serves as an introduction to the context and challenges of modern mobile communication technology. 5G requirements are explored and their impact on the RF front end architectures is revealed. Among the FEM elements, the PA is identified as a key component for efficiency optimization.

The second chapter introduced the basics of PA operation and assessment tools such as output power, efficiency, gain, linearity and bandwidth. The fundamental performance trade-off between efficiency, linearity and gain was shown through the use of classic PA operation modes such as Class-A, AB, B, and C PAs as well as the switch-mode class-E. These architectures also suffered from a sharp decrease in efficiency when the PA is operated at back-off; a requirement in 5G applications. Load modulation-based PA architectures, namely Doherty and Outphasing, are chosen as viable solutions for the efficiency problem.

In the third chapter, the focus was put on the combiner stage of both OPA and DPA architectures. Starting with the OPA combiner analysis, it was shown that most of the Outphasing combiners used today can be obtained by applying circuit transformations to the original Chireix combiner. Their modes of operation are analysed and then grouped in one unified OPA combiner design methodology which ensures a constant peak power regardless of the back-off level. Next, the DPA operation conditions were extracted and used to define a new DPA combiner analysis method. Unlike existing approaches, the proposed method ensures that the main transistor remains in saturation throughout the Doherty region. Using this approach, the compact L-C combiner is proven to be capable of ideal Doherty operation with up to 7dB of peak efficiency back-off. The L-C combiner is therefore shown to be compatible with both OPA and DPA applications.

Chapter 4 details the design of a two-stage class-E DPA using the compact L-C combiner. The power stage is designed and optimized for DPA operation through the use of load pull analysis. It is then used to simulate a two-stage DPA with high efficiency at back-off. The finalized circuit is implemented using RF-SOI technology and flip-chipped onto a μ PCB laminate. Multi-technology EM simulations are then used to validate the implemented design. In CW mode, the measured DPA circuit achieves a saturation power of 32dBm with a peak PAE of 51% when operated at 2.3GHz. At 6dB of back-off, the PA maintains a high efficiency of 36%. Modulated signal measurements with 10MHz LTE signal and a 2.3GHz carrier show an average power of 28dBm with 43% PAE at -35dBc of ACLR. These results are in line with other published works and serve to validate the combiner design method that was proposed in Chapter 3.

Finally, Chapter 5 explored the OPA architecture, starting with the classic class-B implementation. This was followed by a class-E OPA design that used the contour rotation method in order to optimize back-off efficiency. This design was then studied from a system perspective in order to find an improved method of linearization. Two approaches were studied starting with the LUT-based method which provided rudimentary linearization through amplitude and phase control within the SCS. Next a more complex behavioural model-based approach was considered. This led to the formalization of a new In-SCS DPD architecture.

However, given the various constraints, an OPA circuit could not be fabricated in time, which led to the use of a fallback involving an MP PA model. Validation of the model is still ongoing.

The main contributions of this work can be summed up as follows:

- Unified Outphasing combiner design and analysis methodology that is compatible with both voltage and current-mode Outphasing operation.
- Doherty combiner analysis methodology that can be used to determine the maximum achievable BO efficiency level and provide required current profile for maintaining ideal DPA operation.
- Validation of the proposed DPA combiner analysis method through the design and implementation of a two-stage class-E DPA circuit in RF-SOI technology published in [76].
- Analytical boundary condition on Outphasing angle for OPA operation published in [67].
- OPA combiner design method capable of providing set target complex impedances at peak and BO, allowing for more flexible power cell designs.
- In-SCS DPD architecture proposal for linear OPA operation.

The findings of this thesis also serve to directly set up possible future research directions. The analytical study done on both Outphasing and Doherty-type power combiners can be extended to include other types of load modulation-based architectures as well as hybrid operation modes within the Doherty-Outphasing continuum.

Moreover, this work merely scratched the surface of the increasingly popular class-E PA. Further understanding of the subtleties of the class-E design space and operation have the potential to greatly improve the performance of the architectures that use it.

Additionally, different design approaches such as asymmetrical PA designs and hybrid operation modes that utilize both load and supply modulation can provide a way of achieving higher average efficiency for 5G NR signals.

Finally, the work done on DPD system analysis sets the foundation for the integration of DPD within the digital friendly OPA architecture. Future works must focus on the validation of the basic MP PA model before assessing the need for more complex behavioural models. Once the model is ready, it can be used within the proposed In-SCS DPD architecture and optimized to provide the best trade-off between efficiency and linearity. This would lead to a more in-depth analysis of SCS/OPA co-design which is missing from the literature.

List of Publications

The work conducted in this thesis has resulted in the following scientific communications and publications:

Journal Article

- J. Bachi et al., “A Novel Approach for Doherty PA Design using a Compact L-C Combiner,” *IEEE Trans. Circuits Syst. II Express Briefs*, pp. 1–1, 2022, doi: 10.1109/TCSII.2022.3185174.

Conferences

- J. Bachi et al., “A Novel Approach for Doherty PA Design Using a Compact L-C Combiner,” *IEEE International Symposium on Integrated Circuits and Systems (ISICAS)*, Oct 2022, Bordeaux, France.
- J. Bachi, A. Serhan, D. G. Pham, P. Desgreys, and A. Giry, “New Analytical Boundary Condition for Optimized Outphasing PA Design,” in *2019 17th IEEE International New Circuits and Systems Conference (NEWCAS)*, Jun. 2019, pp. 1–4. doi: 10.1109/NEWCAS44328.2019.8961239.
- J. Bachi, A. Serhan, D. G. Pham, P. Desgreys, and A. Giry, “Nouvelle Approche de Dimensionnement d’un Amplificateur de Puissance de Type Outphasing,” *21èmes Journées Nationales Micro-Ondes (JNM)*, May 2019, Caen, France.

References

- [1] D. J. Goodman, "Trends in cellular and cordless communications," *IEEE Commun. Mag.*, vol. 29, no. 6, pp. 31–40, Jun. 1991, doi: 10.1109/35.79400.
- [2] R. Dettmer, "GSM-European cellular goes digital," *IEE Rev.*, vol. 37, no. 7, pp. 253–257, Jul. 1991, doi: 10.1049/ir:19910114.
- [3] F. Hillebrand, "The creation of standards for global mobile communication: GSM and UMTS standardization from 1982 to 2000," *IEEE Wirel. Commun.*, vol. 20, no. 5, pp. 24–33, Oct. 2013, doi: 10.1109/MWC.2013.6664470.
- [4] B. A. Bjerke, "LTE-advanced and the evolution of LTE deployments," *IEEE Wirel. Commun.*, vol. 18, no. 5, pp. 4–5, Oct. 2011, doi: 10.1109/MWC.2011.6056684.
- [5] S. Chen, S. Sun, Y. Wang, G. Xiao, and R. Tamrakar, "A comprehensive survey of TDD-based mobile communication systems from TD-SCDMA 3G to TD-LTE(A) 4G and 5G directions," *China Commun.*, vol. 12, no. 2, pp. 40–60, Feb. 2015, doi: 10.1109/CC.2015.7084401.
- [6] M. Agiwal, A. Roy, and N. Saxena, "Next Generation 5G Wireless Networks: A Comprehensive Survey," *IEEE Commun. Surv. Tutor.*, vol. 18, no. 3, Art. no. 3, thirdquarter 2016, doi: 10.1109/COMST.2016.2532458.
- [7] J. G. Andrews *et al.*, "What Will 5G Be?," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 6, Art. no. 6, Jun. 2014, doi: 10.1109/JSAC.2014.2328098.
- [8] G. Liu, Y. Huang, Z. Chen, L. Liu, Q. Wang, and N. Li, "5G Deployment: Standalone vs. Non-Standalone from the Operator Perspective," *IEEE Commun. Mag.*, vol. 58, no. 11, pp. 83–89, Nov. 2020, doi: 10.1109/MCOM.001.2000230.
- [9] GTI, "GTI 5G Device RF Component Research Report," 2018. Accessed: Aug. 15, 2022. [Online]. Available: <https://docplayer.net/83222040-Gti-5g-device-rf-component-research-report.html>
- [10] P. Banelli, S. Buzzi, G. Colavolpe, A. Modenini, F. Rusek, and A. Ugolini, "Modulation Formats and Waveforms for 5G Networks: Who Will Be the Heir of OFDM?: An overview of alternative modulation schemes for improved spectral efficiency," *IEEE Signal Process. Mag.*, vol. 31, no. 6, pp. 80–93, Nov. 2014, doi: 10.1109/MSP.2014.2337391.
- [11] G. Berardinelli, K. I. Pedersen, T. B. Sorensen, and P. Mogensen, "Generalized DFT-Spread-OFDM as 5G Waveform," *IEEE Commun. Mag.*, vol. 54, no. 11, pp. 99–105, Nov. 2016, doi: 10.1109/MCOM.2016.1600313CM.
- [12] J. Yli-Kaakinen *et al.*, "Frequency-Domain Signal Processing for Spectrally-Enhanced CP-OFDM Waveforms in 5G New Radio," *IEEE Trans. Wirel. Commun.*, vol. 20, no. 10, pp. 6867–6883, Oct. 2021, doi: 10.1109/TWC.2021.3077762.
- [13] F. Balteanu *et al.*, "Multiple Transmitter Coexistence for 5G RF Front End Modules," in *2021 51st European Microwave Conference (EuMC)*, Apr. 2022, pp. 180–183. doi: 10.23919/EuMC50147.2022.9784253.

-
- [14] A. Giry, A. Serhan, D. Parat, and P. Reynier, "Linear Power Amplifiers for Sub-6GHz Mobile Applications: Progress and Trends," in *2020 18th IEEE International New Circuits and Systems Conference (NEWCAS)*, Jun. 2020, pp. 226–229. doi: 10.1109/NEWCAS49341.2020.9159835.
- [15] A. Siligaris, "Modélisation grand signal de MOSFET en hyperfréquences: application à l'étude des non linéarités des filières SOI," PhD Thesis, University of Lille 1, Lille, France, 2004. Accessed: Oct. 26, 2021. [Online]. Available: <https://www.theses.fr/2004LIL10091>
- [16] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA, USA: Artech House, 2006.
- [17] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun. 1975, doi: 10.1109/JSSC.1975.1050582.
- [18] A. Grebennikov and N. O. Sokal, *Switchmode RF Power Amplifiers*. Newnes, 2007.
- [19] R. Zulinski and J. Steadman, "Class E Power Amplifiers and Frequency Multipliers with finite DC-Feed Inductance," *IEEE Trans. Circuits Syst.*, vol. 34, no. 9, pp. 1074–1087, Sep. 1987, doi: 10.1109/TCS.1987.1086268.
- [20] C. P. Avratoglou, N. C. Voulgaris, and F. I. Ioannidou, "Analysis and design of a generalized class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. 36, no. 8, pp. 1068–1079, Aug. 1989, doi: 10.1109/31.192415.
- [21] M. Acar, A. J. Annema, and B. Nauta, "Analytical Design Equations for Class-E Power Amplifiers with Finite DC-Feed Inductance and Switch On-Resistance," in *2007 IEEE International Symposium on Circuits and Systems*, May 2007, pp. 2818–2821. doi: 10.1109/ISCAS.2007.378758.
- [22] M. Kreißig and F. Ellinger, "Extended analysis of idealized class-E operation with finite DC-feed inductance and preservation of zero volt switching at variable load," in *2017 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Jun. 2017, pp. 1–4. doi: 10.1109/SMACD.2017.7981613.
- [23] M. Acar, A. J. Annema, and B. Nauta, "Generalized Design Equations for Class-E Power Amplifiers with Finite DC Feed Inductance," in *2006 European Microwave Conference*, Sep. 2006, pp. 1308–1311. doi: 10.1109/EUMC.2006.281237.
- [24] F. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. 24, no. 12, pp. 725–735, Dec. 1977, doi: 10.1109/TCS.1977.1084296.
- [25] F. H. Raab, "Effects of circuit variations on the class E tuned power amplifier," *IEEE J. Solid-State Circuits*, vol. 13, no. 2, pp. 239–247, Apr. 1978, doi: 10.1109/JSSC.1978.1051026.
- [26] J.-S. Paek *et al.*, "Efficient RF-PA Two-Chip Supply Modulator Architecture for 4G LTE and 5G NR Dual-Connectivity RF Front End," *IEEE J. Solid-State Circuits*, vol. 57, no. 4, pp. 1075–1089, Apr. 2022, doi: 10.1109/JSSC.2022.3144771.

- [27] X. Liu, H. Zhang, P. K. T. Mok, and H. C. Luong, "A Multi-Loop-Controlled AC-Coupling Supply Modulator With a Mode-Switching CMOS PA in an EER System With Envelope Shaping," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1553–1563, Jun. 2019, doi: 10.1109/JSSC.2019.2892555.
- [28] X. A. Nghiem, J. Guan, and R. Negra, "Broadband Sequential Power Amplifier With Doherty-Type Active Load Modulation," *IEEE Trans. Microw. Theory Tech.*, vol. 63, no. 9, pp. 2821–2832, Sep. 2015, doi: 10.1109/TMTT.2015.2456901.
- [29] F. H. Raab, "Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 8, pp. 1462–1468, Aug. 2001, doi: 10.1109/22.939927.
- [30] H. Chireix, "High Power Outphasing Modulation," *Proc. Inst. Radio Eng.*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935, doi: 10.1109/JRPROC.1935.227299.
- [31] K. D. Holzer, W. Yuan, and J. S. Walling, "Wideband Techniques for Outphasing Power Amplifiers," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 65, no. 9, pp. 2715–2725, Sep. 2018, doi: 10.1109/TCSI.2018.2800041.
- [32] G. Poitau, A. Birafane, and A. Kouki, "Experimental characterization of LINC outphasing combiners' efficiency and linearity," in *Proceedings. 2004 IEEE Radio and Wireless Conference (IEEE Cat. No.04TH8746)*, Sep. 2004, pp. 87–90. doi: 10.1109/RAWCON.2004.1389078.
- [33] Z. Abou-Chahine, T. Felgentreff, G. Fischer, and R. Weigel, "Efficiency analysis of the asymmetric 2-level outphasing PA with Rayleigh enveloped signals," in *2012 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications*, Jan. 2012, pp. 85–88. doi: 10.1109/PAWR.2012.6174930.
- [34] D. Cox, "Linear Amplification with Nonlinear Components," *IEEE Trans. Commun.*, vol. 22, no. 12, pp. 1942–1945, Dec. 1974, doi: 10.1109/TCOM.1974.1092141.
- [35] M. Martelius *et al.*, "A Class-D Tri-Phasing CMOS Power Amplifier With an Extended Marchand-Balun Power Combiner," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 3, Art. no. 3, Mar. 2020, doi: 10.1109/TMTT.2019.2952771.
- [36] A. Ghahremani, A. Annema, and B. Nauta, "Outphasing Class-E Power Amplifiers: From Theory to Back-Off Efficiency Improvement," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1374–1386, May 2018, doi: 10.1109/JSSC.2017.2787759.
- [37] A. Banerjee, R. Hezar, L. Ding, and B. Haroun, "A 29.5 dBm Class-E Outphasing RF Power Amplifier With Efficiency and Output Power Enhancement Circuits in 45nm CMOS," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 64, no. 8, Art. no. 8, Aug. 2017, doi: 10.1109/TCSI.2017.2695243.
- [38] S. Shim and S. Pamarti, "A 1.85GHz CMOS power amplifier with zero-voltage-switching contour-based outphasing control to improve back-off efficiency," in *2015 IEEE MTT-S International Microwave Symposium*, May 2015, pp. 1–4. doi: 10.1109/MWSYM.2015.7166962.
- [39] W. H. Doherty, "A new high-efficiency power amplifier for modulated waves," *Bell Syst. Tech. J.*, vol. 15, no. 3, pp. 469–475, Jul. 1936, doi: 10.1002/j.1538-7305.1936.tb03563.x.

- [40] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The Doherty Power Amplifier," *Int. J. Microw. Opt. Technol.*, vol. 5, no. 6, Nov. 2010, Accessed: May 26, 2020. [Online]. Available: <https://www.ijmot.com/ijmot/uploaded/qtpzmelcujf.pdf>
- [41] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The AB-C Doherty power amplifier. Part I: Theory," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 19, no. 3, pp. 293–306, 2009, doi: 10.1002/mmce.20350.
- [42] K. Takenaka, T. Sato, H. Matsumoto, M. Kawashima, and N. Nakajima, "New compact Doherty power amplifier design for handset applications," in *2017 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Jan. 2017, pp. 81–83. doi: 10.1109/PAWR.2017.7875579.
- [43] P. Draxler and J. Hur, "A multi-band CMOS Doherty PA with tunable matching network," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Jun. 2017, pp. 944–946. doi: 10.1109/MWSYM.2017.8058742.
- [44] A. Serhan *et al.*, "A Broadband High-Efficiency SOI-CMOS PA Module for LTE/LTE-A Handset Applications," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2019, pp. 299–302. doi: 10.1109/RFIC.2019.8701727.
- [45] A. Serhan *et al.*, "A Reconfigurable SOI CMOS Doherty Power Amplifier Module for Broadband LTE High-Power User Equipment Applications," in *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Aug. 2020, pp. 79–82. doi: 10.1109/RFIC49505.2020.9218305.
- [46] S. Moloudi and A. A. Abidi, "The Outphasing RF Power Amplifier: A Comprehensive Analysis and a Class-B CMOS Realization," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1357–1369, Jun. 2013, doi: 10.1109/JSSC.2013.2252522.
- [47] W. Gerhard and R. Knoechel, "Novel transmission line combiner for highly efficient outphasing RF power amplifiers," in *2007 European Microwave Conference*, Oct. 2007, pp. 1433–1436. doi: 10.1109/EUMC.2007.4405474.
- [48] A. Bogusz, J. Lees, R. Quaglia, G. Watkins, and S. C. Cripps, "Practical Load Compensation Networks in Chireix Outphasing Amplifiers Using Offset Transmission Lines," in *2018 48th European Microwave Conference (EuMC)*, Sep. 2018, pp. 17–20. doi: 10.23919/EuMC.2018.8541517.
- [49] T. W. Barton, A. S. Jurkov, P. H. Pednekar, and D. J. Perreault, "Multi-Way Lossless Outphasing System Based on an All-Transmission-Line Combiner," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 4, pp. 1313–1326, Apr. 2016, doi: 10.1109/TMTT.2016.2531691.
- [50] L. C. Nunes, F. M. Barradas, D. R. Barros, P. M. Cabral, and J. C. Pedro, "Current Mode Outphasing Power Amplifier," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Jun. 2019, pp. 1160–1163. doi: 10.1109/MWSYM.2019.8701026.
- [51] S. Lee and S. Nam, "A CMOS Outphasing Power Amplifier With Integrated Single-Ended Chireix Combiner," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 57, no. 6, pp. 411–415, Jun. 2010, doi: 10.1109/TCSII.2010.2048353.
- [52] K. Ning, Y. Fang, N. Hosseinzadeh, and J. F. Buckwalter, "A 30-GHz CMOS SOI Outphasing Power Amplifier With Current Mode Combining for High Backoff

- Efficiency and Constant Envelope Operation,” *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1411–1421, May 2020, doi: 10.1109/JSSC.2019.2949255.
- [53] M. Özen, M. van der Heijden, M. Acar, R. Jos, and C. Fager, “A Generalized Combiner Synthesis Technique for Class-E Outphasing Transmitters,” *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 64, no. 5, pp. 1126–1139, May 2017, doi: 10.1109/TCSI.2016.2636155.
- [54] A. Yamaoka, T. M. Hone, and K. Yamaguchi, “70 % Efficient Dual-Input Doherty-Outphasing Power Amplifier for Large PAPR Signals,” in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Jun. 2019, pp. 556–559.
- [55] A. R. Qureshi, M. Acar, J. Qureshi, R. Wesson, and L. C. N. de Vreede, “A 112W GaN dual input Doherty-Outphasing Power Amplifier,” in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, May 2016, pp. 1–4. doi: 10.1109/MWSYM.2016.7540194.
- [56] C. Liang, P. Roblin, Y. Hahn, Z. Popovic, and H. Chang, “Novel Outphasing Power Amplifiers Designed With an Analytic Generalized Doherty–Chireix Continuum Theory,” *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 66, no. 8, pp. 2935–2948, Aug. 2019, doi: 10.1109/TCSI.2019.2910471.
- [57] K. Takenaka, T. Sato, H. Matsumoto, M. Kawashima, and N. Nakajima, “Novel broadband Doherty power amplifier design for multiband handset applications,” in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Jun. 2017, pp. 778–781. doi: 10.1109/MWSYM.2017.8058693.
- [58] P. Saad, Z. Asghari, C. Fager, and H. Mashad Nemati, “Driver Topologies for RF Doherty Power Amplifiers,” *IEEE Microw. Wirel. Compon. Lett.*, vol. 27, no. 1, pp. 67–69, Jan. 2017, doi: 10.1109/LMWC.2016.2629977.
- [59] Y. Han and D. J. Perreault, “Analysis and Design of High Efficiency Matching Networks,” *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1484–1491, Sep. 2006, doi: 10.1109/TPEL.2006.882083.
- [60] M. Bakshi, V. Sule, and M. Shojaei Baghini, “Systems Theory Approach to Stabilization of Multiport Networks,” *J. Control Syst. Eng.*, vol. 5, pp. 48–63, Dec. 2017, doi: 10.18005/JCSE0501005.
- [61] H. S. Nagi, “Miniature lumped element 180°/spl deg/ Wilkinson divider,” in *IEEE MTT-S International Microwave Symposium Digest, 2003*, Jun. 2003, vol. 1, pp. 55–58 vol.1. doi: 10.1109/MWSYM.2003.1210882.
- [62] T. Kawai, I. Ohta, and A. Enokihara, “Design method of lumped-element dual-band Wilkinson power dividers based on frequency transformation,” in *2010 Asia-Pacific Microwave Conference*, Dec. 2010, pp. 710–713.
- [63] T. Kawai, H. Mizuno, I. Ohta, and A. Enokihara, “Lumped-element quadrature wilkinson power divider,” in *2009 Asia Pacific Microwave Conference*, Dec. 2009, pp. 1012–1015. doi: 10.1109/APMC.2009.5384352.
- [64] M. S. Boutayeb, “Architecture et conception d’un amplificateur de puissance large-bande pour des applications 4G/5G,” These de doctorat, Université Grenoble Alpes,

2020. Accessed: Nov. 30, 2021. [Online]. Available: <http://www.theses.fr/2020GRALT055>
- [65] G. Tant, “Etude et intégration en SOI d’amplificateurs de puissance reconfigurables pour applications multi-modes multi-bandes,” These de doctorat, Université Grenoble Alpes (ComUE), 2015. Accessed: Nov. 30, 2021. [Online]. Available: <https://www.theses.fr/2015GREAT101>
- [66] D. A. Calvillo-Cortes and L. C. N. de Vreede, “Analysis of pure- and mixed-mode class-B outphasing amplifiers,” in *2014 IEEE 5th Latin American Symposium on Circuits and Systems*, Feb. 2014, pp. 1–4. doi: 10.1109/LASCAS.2014.6820271.
- [67] J. Bachi, A. Serhan, D. G. Pham, P. Desgreys, and A. Giry, “New Analytical Boundary Condition for Optimized Outphasing PA Design,” in *2019 17th IEEE International New Circuits and Systems Conference (NEWCAS)*, Jun. 2019, pp. 1–4. doi: 10.1109/NEWCAS44328.2019.8961239.
- [68] R. A. Beltran and F. H. Raab, “Simplified analysis and design of outphasing transmitters using class-E power amplifiers,” in *2015 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, Jan. 2015, pp. 1–3. doi: 10.1109/PAWR.2015.7139197.
- [69] R. Beltran, F. H. Raab, and A. Velazquez, “HF outphasing transmitter using class-E power amplifiers,” in *2009 IEEE MTT-S International Microwave Symposium Digest*, Jun. 2009, pp. 757–760. doi: 10.1109/MWSYM.2009.5165807.
- [70] A. Ghahremani, A. Annema, and B. Nauta, “A 20dBm outphasing class E PA with high efficiency at power back-off in 65nm CMOS technology,” in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2017, pp. 340–343. doi: 10.1109/RFIC.2017.7969087.
- [71] J. Lemberg *et al.*, “A 1.5–1.9-GHz All-Digital Tri-Phasing Transmitter With an Integrated Multilevel Class-D Power Amplifier Achieving 100-MHz RF Bandwidth,” *IEEE J. Solid-State Circuits*, vol. 54, no. 6, Art. no. 6, Jun. 2019, doi: 10.1109/JSSC.2019.2902753.
- [72] M. Kosunen *et al.*, “13.5 A 0.35-to-2.6GHz multilevel outphasing transmitter with a digital interpolating phase modulator enabling up to 400MHz instantaneous bandwidth,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2017, pp. 224–225. doi: 10.1109/ISSCC.2017.7870342.
- [73] G. Baudoin, O. Venard, and D.-K. Pham, “Digital predistortion,” in *Digitally Enhanced Mixed Signal Systems*, Institution of Engineering and Technology, 2019, pp. 65–123. doi: 10.1049/PBCS040E_ch3.
- [74] F. M. Ghannouchi, O. Hammi, and M. Helouai, *Behavioral Modeling and Predistortion of Wideband Wireless Transmitters* / Wiley. Wiley, 2015. Accessed: Aug. 10, 2022. [Online]. Available: <https://www.wiley.com/engb/Behavioral+Modeling+and+Predistortion+of+Wideband+Wireless+Transmitters-p-9781118406274>
- [75] S. A. Bassam, M. Helouai, and F. M. Ghannouchi, “2-D Digital Predistortion (2-D-DPD) Architecture for Concurrent Dual-Band Transmitters,” *IEEE Trans. Microw.*

- Theory Tech.*, vol. 59, no. 10, pp. 2547–2553, Oct. 2011, doi: 10.1109/TMTT.2011.2163802.
- [76] J. Bachi *et al.*, “A Novel Approach for Doherty PA Design using a Compact L-C Combiner,” *IEEE Trans. Circuits Syst. II Express Briefs*, pp. 1–1, 2022, doi: 10.1109/TCSII.2022.3185174.
- [77] F. Zarate-Rincon, G. Álvarez-Botero, R. Torres-Torres, and R. Murphy Arteaga, “Extraction Methodology of the Substrate Parasitic Network of an RF-MOSFET with Separate Substrate DC Connection,” Feb. 2012.
- [78] D. M. Pozar, “Microwave Network Analysis,” in *Microwave engineering*, 4th ed., Hoboken, NJ: Wiley, 2012, pp. 165–227.
- [79] D. M. Pozar, “Transmission Line Theory,” in *Microwave engineering*, 4th ed., Hoboken, NJ: Wiley, 2012, pp. 48–94.
- [80] J. Hong and M. J. Lancaster, “Network Analysis,” in *Microstrip Filters for RF/Microwave Applications*, 2nd ed., Wiley–Blackwell, pp. 7–28.

List of Appendices

Appendix A.	Active Device Modelling	132
Appendix B.	Two-Port Networks.....	134
B.1.	Transmission Lines	135
B.1.1.	Quarter-Wave Transmission Line	135
B.1.2.	Half-Wave Transmission Line	136
B.1.3.	Cascading Transmission Lines	136
B.1.4.	Lumped Element Equivalent Model.....	137
B.1.5.	Differential to Single-Ended Transformation.....	137
B.2.	Dual Networks.....	138
B.2.1.	Note on the direction of active sources.....	139
Appendix C.	Complex Load OPA Combiner Design	140
C.1.	OTL-Based OEPA Design	140
C.2.	Generalized Solution	144

Appendix A. Active Device Modelling

The intrinsic capacitive and resistive elements of a transistor are assumed to be linear. The large-signal transistor model of Figure A.1(a) is considered, with ideal capacitors and resistances.

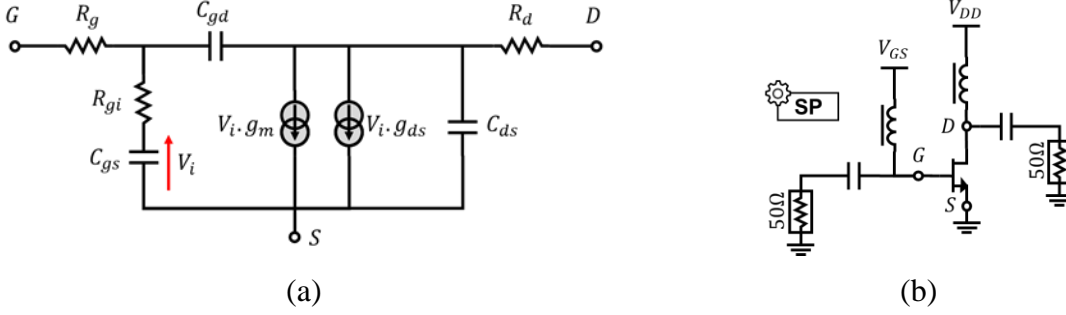


Figure A.1 – Two-port network representation

In order to extract the values of the model parasitic components, the device is placed in a common source configuration like the one in Figure A.1(b) and its small-signal S-Parameters are extracted. The values of the capacitors are calculated using the equations below [15].

$$C_{gd} = -\frac{\Im[Y_{21}]}{\omega} \quad (A.15)$$

$$C_{gs} = -\frac{\Im[Y_{11}]}{\omega} - C_{gd} \quad (A.16)$$

$$C_{ds} = -\frac{\Im[Y_{22}]}{\omega} - C_{gd} \quad (A.17)$$

The gate resistance R_g is extracted using the equation in (A.18) for $V_{GS} = 0$. [77]

$$R_g = \left(\frac{\Re[Y_{11}]}{(\Im[Y_{11}])^2} \right) \Big|_{V_{GS}=0} \quad (A.18)$$

The remaining parameters can be calculated using the equations below:

$$R_{gi} = \frac{1}{C_{gs} \cdot \omega} \cdot \left(\frac{\Re[Y_{11}] + \Re[Y_{12}]}{\Im[Y_{11}] + \Im[Y_{12}]} \right) \quad (A.19)$$

$$g_{ds} = (\Re[Y_{22}])|_{\omega \rightarrow 0} \quad (A.20)$$

$$R_d = \left(\Re[Z_{22} - Z_{12}] - \frac{1}{2 \cdot K \cdot (V_{GS} - V_{TH})} \right) \Big|_{V_{DS} \rightarrow 0; V_{GS} = V_{GSmax}} \quad (A.21)$$

Finally, the value of the transconductance g_m can be verified through (A.22).

$$g_m = (\Re[Y_{21}])|_{\omega=0} \quad (\text{A.22})$$

Appendix B. Two-Port Networks

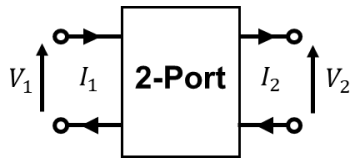


Figure B.1 – Two-port network representation

A two-port network [78], shown in Figure B.1, is a representation of a sub-circuit with two pairs of terminals and can be defined by different types of matrices such as:

- Impedance parameter matrix Z
- Admittance parameter matrix Y
- Transmission or Chain or ABCD parameter matrix

The ABCD parameter matrix is constructed using the expressions in (B.1).

$$ABCD = \begin{pmatrix} \left. \frac{V_1}{V_2} \right|_{I_2=0} & \left. \frac{V_1}{I_2} \right|_{V_2=0} \\ \left. \frac{I_1}{V_2} \right|_{I_2=0} & \left. \frac{I_1}{I_2} \right|_{V_2=0} \end{pmatrix} \quad (B.1)$$

An important property of ABCD parameters is the ability to calculate the equivalent ABCD matrix of a cascade of multiple two-port networks by multiplying their individual ABCD matrices.

$$ABCD_{Eq} = \prod_i ABCD_i \quad (B.2)$$

A list of ABCD matrices for common elementary components is provided in Table B.1.

Table B.1 – Common component ABCD matrices

Network Type	Symbol	ABCD Matrix
Series Element		$ABCD_Z = \begin{pmatrix} 1 & Z \\ 0 & 1 \end{pmatrix}$
Shunt Element		$ABCD_Y = \begin{pmatrix} 1 & 0 \\ Y & 1 \end{pmatrix}$
Transmission Line		$ABCD_{TL} = \begin{pmatrix} \cos(\theta) & j \cdot Z \cdot \sin(\theta) \\ j \cdot Z^{-1} \cdot \sin(\theta) & \cos(\theta) \end{pmatrix}$
Transformer		$ABCD_{TF} = \begin{pmatrix} N & 0 \\ 0 & N^{-1} \end{pmatrix}$

B.1. Transmission Lines



Figure B.2 – (a) Transmission Line representation as a two-port network, (b) Transmission line terminated in a load Z_L

A lossless transmission line is defined by its characteristic impedance Z and its electrical length θ for a given frequency f_0 . When terminated with a load Z_L its input impedance Z_{in} is calculated through [79]:

$$Z_{in} = Z \cdot \frac{Z_L + j \cdot Z \cdot \tan(\theta)}{Z + j \cdot Z_L \cdot \tan(\theta)} \quad (B.3)$$

Using (B.3) it can be shown that if the characteristic impedance Z of the transmission line is of the same value as the load, then the input impedance Z_{in} becomes equal to the load impedance Z_L .

B.1.1. Quarter-Wave Transmission Line

For $\theta = 90^\circ$, the transmission line is referred to as a quarter-wave line and its ABCD matrix is simplified to

$$ABCD_{\frac{\lambda}{4}} = \begin{pmatrix} 0 & j \cdot Z \\ j \cdot Z^{-1} & 0 \end{pmatrix} \quad (B.4)$$

Moreover, its input impedance becomes:

$$Z_{in} = \frac{Z^2}{Z_L} \quad (B.5)$$

In the equation above, it can be seen that the input impedance Z_{in} is inversely proportional to the load impedance Z_L . As a result, the quarter-wave transmission line is considered as an impedance inverter.

Finally, its corresponding impedance matrix is shown in (B.6) and leads to the expression in (B.7)

$$Z_{\frac{\lambda}{4}} = \begin{pmatrix} 0 & -j \cdot Z \\ -j \cdot Z & 0 \end{pmatrix} \quad (B.6)$$

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} j \cdot Z \cdot I_2 \\ -j \cdot Z \cdot I_1 \end{pmatrix} \quad (B.7)$$

B.1.2. Half-Wave Transmission Line

When the electrical length θ is equal to 180° , the transmission line is referred to as a half-wave line. Its ABCD matrix becomes:

$$ABCD_{\frac{\lambda}{2}} = \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix} = -\mathbb{I}_2 \quad (B.8)$$

The ABCD matrix of the half-wave line is the opposite of the 2×2 identity matrix \mathbb{I}_2 . As a result, it can be moved freely within a cascaded system without affecting its overall behaviour. Furthermore, it can be removed entirely from the system, by replacing its with a negative sign on any of the input or output voltages or currents. This property is better illustrated in Figure B.3 where all four topologies result in the same equivalent circuit.

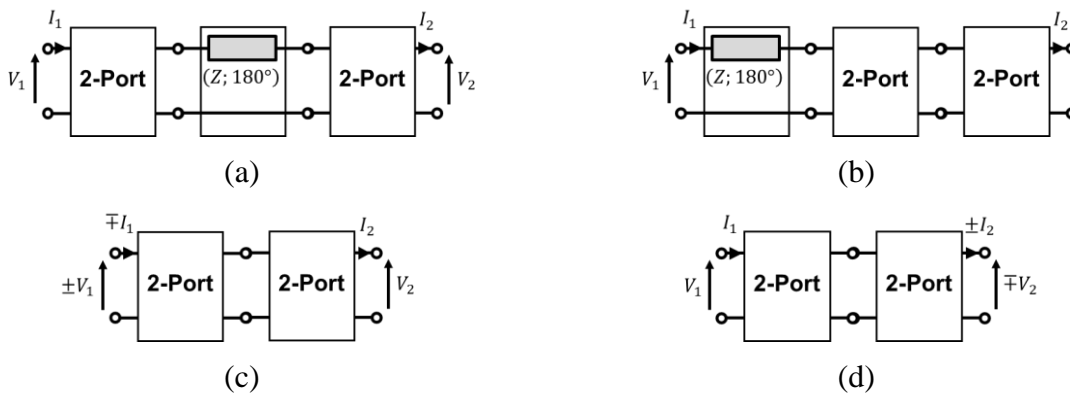


Figure B.3 – Transmission Line representation as a two-port network

B.1.3. Cascading Transmission Lines

Cascaded transmission lines having the same characteristic impedance Z and different electrical lengths θ_i can be represented by a single transmission line of characteristic impedance Z and an electrical length equal to the sum of the lengths of the individual lines. This can be proven by multiplying the ABCD matrices of the individual lines

$$ABCD(Z; \theta) = \prod_i ABCD(Z; \theta_i) = ABCD\left(Z; \sum_i \theta_i\right) \quad (B.9)$$

As a result, in a cascaded topology, two half-wave transmission lines anywhere in the circuit can be summed up together to produce a full-wave line, whose ABCD matrix is the identity matrix \mathbb{I}_2 , and removed from the system.

$$ABCD_{\lambda} = ABCD_{\frac{\lambda}{2}} \cdot ABCD_{\frac{\lambda}{2}} = \mathbb{I}_2 \quad (B.10)$$

B.1.4. Lumped Element Equivalent Model

A lossless transmission line of characteristic impedance Z and electrical length θ can be modelled at a given frequency f_0 using a π -network like the one shown in Figure B.4(a).

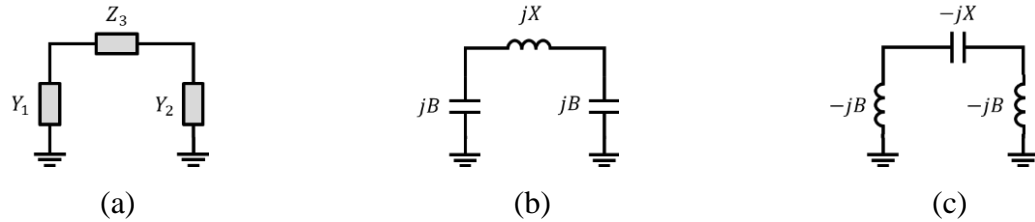


Figure B.4 – (a) Differential power combining topology, (b) Equivalent common-mode power combiner

Depending on the value of θ , two possible cases ensue:

- For $\theta \in [0^\circ; 180^\circ]$, the equivalent model is that of Figure B.4(b).
- For $\theta \in [0^\circ; -180^\circ]$, the equivalent model is that of Figure B.4(c).

In either case, the values of the series reactance X and the shunt susceptance B can be obtained by equating the ABCD matrices of the transmission line and the π -network. The result is shown below in (B.11) and (B.12)

$$X = Z \cdot |\sin(\theta)| \quad (B.11)$$

$$B = \frac{1 - \cos(\theta)}{X} \quad (B.12)$$

B.1.5. Differential to Single-Ended Transformation

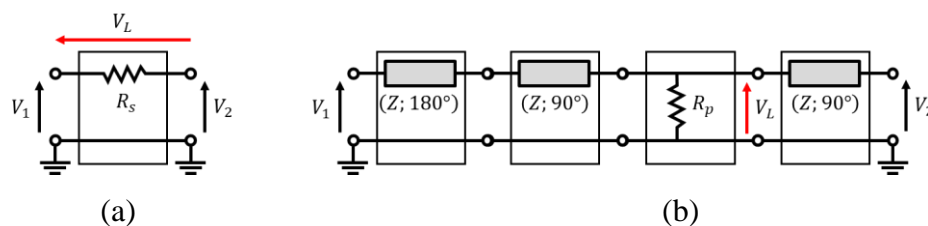


Figure B.5 – (a) Differential power combining topology, (b) Equivalent single-ended power combiner

A differential power combiner topology, as seen in Figure B.5.(a) can be transformed into an equivalent single-ended topology, Figure B.5(b), using transmission lines. The value of the resulting parallel resistance R_p can be obtained by comparing the ABCD-parameter matrices of the two topologies:

$$ABCD_{Dif} = \begin{pmatrix} 1 & R_s \\ 0 & 1 \end{pmatrix} \quad (B.13)$$

$$ABCD_{SE} = ABCD_{\frac{\lambda}{2}} \cdot ABCD_{\frac{\lambda}{4}} \cdot ABCD_{R_p} \cdot ABCD_{\frac{\lambda}{4}} = \begin{pmatrix} 1 & \frac{Z^2}{R_p} \\ 0 & 1 \end{pmatrix} \quad (B.14)$$

$$R_p = \frac{Z^2}{R_s} \quad (B.15)$$

B.2. Dual Networks

In electronic network analysis, two networks N and N' are said to be dual if the Z-matrix of the first, Z and the Y-matrix of the second, Y' respect the following conditions [80]:

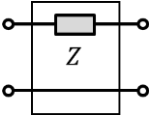
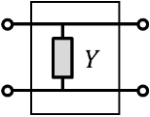
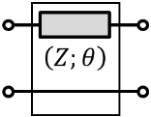
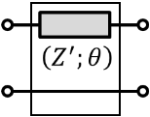
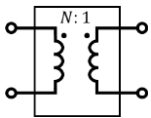
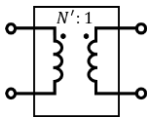
$$\begin{cases} z_{ii} = y'_{jj} \\ z_{ij} = -y'_{ij} \quad (i \neq j) \end{cases} \quad (B.16)$$

In the case of two-port networks, the duality condition can be expressed in terms of ABCD parameters by comparing the ABCD parameters of the dual networks N and N' .

$$\mathcal{D} \begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} D & C \\ B & A \end{pmatrix} \quad (B.17)$$

Applying this duality transformation to the elementary components of Table B.1, results in the dual networks presented in Table B.2.

Table B.2 – Dual networks of elementary components

Original Network	Dual Network	Parameters
		$Z = Y$
		$Z' = \frac{1}{Z}$
		$N' = \frac{1}{N}$

B.2.1. Note on the direction of active sources in dual networks

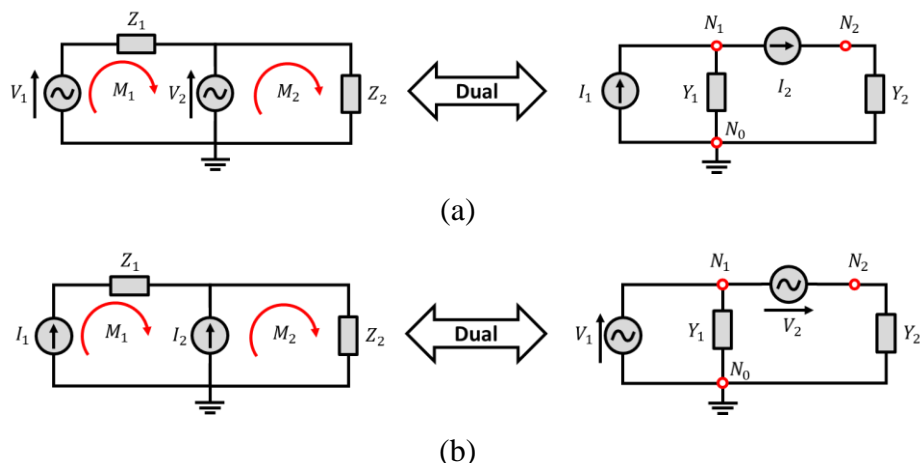


Figure B.6 – Examples of dual circuits with (a) Voltage sources and (b) Current sources

In order to determine the dual of a given circuit, a single direction is applied to each of its meshes. Then, every mesh M_i is replaced by a node N_i , and a ground node N_0 is added. The circuit elements are then transformed individually: An element contained in a single mesh M_i , is replaced by its dual form between nodes N_i and N_0 , whereas an element contained between two meshes M_i and M_j is replaced by its dual form between nodes N_i and N_j . In the case of an active source with an arrow pointing in the same direction as the mesh M_i , its dual source will point towards the node N_i as shown in Figure B.6.

Appendix C. Complex Load OPA Combiner Design

One of the main setbacks of classic outphasing combiners, is the fact that the two intersections of the load modulation trajectories seen by each branch only occur at purely real impedances (purely resistive). This is an issue for some PAs such as class-E, which require a real impedance at peak power and a complex one at back-off. In [68] and [69] the authors propose a solution to this problem by introducing offset transmission lines to the combiner inputs. These works however do not give the voltage or current profiles required to achieve ideal outphasing behaviour when using the OTLs. The following sections provide a detailed analytical study of the OTL method for class-E OPA behaviour as well as a generalized variant capable of providing complex impedances both at peak and back-off.

C.1. OTL-Based OEPA Design

A typical load modulation-based OPA combiner is represented as a two-port network (CMB) and is cascaded between two identical offset transmission lines as represented in Figure C.1.

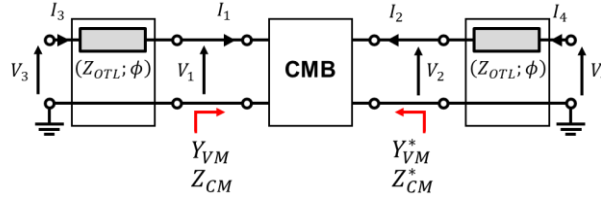


Figure C.1 – Generic Outphasing load modulation combiner with offset transmission lines

Assuming ideal Outphasing operation at ports 1 and 2 ($V_{1,2}$ defined as in (3.1)) of the core combiner, the input voltages $V_{3,4}$ can be calculated by solving the system in (C.1).

$$\begin{pmatrix} V_{3,4} \\ I_{3,4} \end{pmatrix} = \begin{pmatrix} \cos(\phi) & j \cdot Z_{OTL} \cdot \sin(\phi) \\ j \cdot \frac{1}{Z_{OTL}} \cdot \sin(\phi) & \cos(\phi) \end{pmatrix} \times \begin{pmatrix} V_{1,2} \\ I_{1,2} \end{pmatrix} \quad (C.1)$$

In voltage-mode operation, the input signal must therefore be:

$$V_{3,4} = (\cos(\phi) + j \cdot Z_{OTL} \cdot \sin(\phi) \cdot Y_{VM|1,2}) \cdot V_{1,2} \quad (C.2)$$

Where $Y_{VM|1,2}$ represents the core combiner voltage-mode admittance. The current-mode operation inputs $I_{1,2}$, defined in (3.13), can also be calculated and result in the equations of (C.3) where $Z_{CM|1,2}$ is the core combiner input impedance in current-mode operation.

$$I_{3,4} = \left(\cos(\phi) + j \cdot \frac{1}{Z_{OTL}} \cdot \sin(\phi) \cdot Z_{CM|1,2} \right) \cdot I_{1,2} \quad (C.3)$$

With the voltage and current expressions clearly defined at the inputs of the new OTL-based combiner, a design method is required to control the size and position of the impedance trajectories. In the following paragraph, a new method is outlined for the design of an OTL-based OEPA using two impedance values.

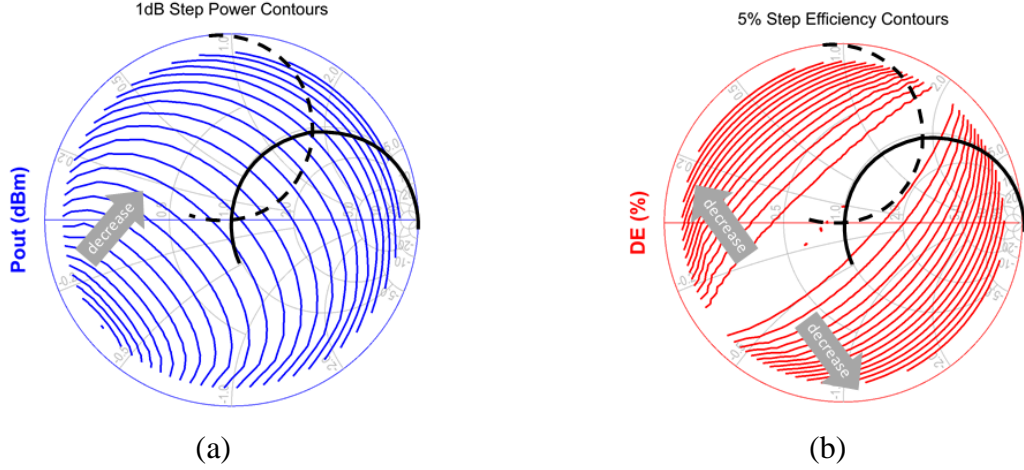


Figure C.2 – Ideal switch-based $q=1$ class-E PA load-pull contours showing (a) output power and (b) efficiency contours with rotated OTL Outphasing load modulation schemes overlaid in black.

A class-E PA delivers the required output power when the load $Z_L = R$. This resistance value will be referred to as the peak resistance R_{opt} and used to normalize the Smith chart. The load trajectories in Figure C.2 must intersect at the centre of the Smith chart, therefore the characteristic impedance of the offset transmission lines is set as:

$$Z_{OTL} = R_{opt} = R \quad (C.4)$$

The first intersection of the load trajectories is therefore at the value R_{max} . This condition is expressed in equation form in (C.5) for both voltage combiners or current combiners.

$$\begin{cases} \Re[Y_{VM|VC}]|_{\theta=\theta_c} = R_{opt} \\ \Re[Y_{VM|CC}]|_{\theta=90^\circ-\theta_c} = R_{opt} \end{cases} \quad (C.5)$$

Solving the equations above leads to the expression for the load resistance R_L to be used in the core combiner design. Recalling the combiner design methodology presented in *Chapter 3 section 1.4.1*, the value of the elements of the core combiner stage can be determined for the different combiner types using the updated Table C.. This ensures that for all acceptable values of θ_c and ϕ , the value of the first intersection impedance (and therefore the associated power level) is always the same.

Table C.1 – Combiner Component Design Values for OTL-based combiners

	Reactive Compensation Voltage Combiner	Delay-Line Compensation Voltage Combiner	Reactive Compensation Current Combiner	Delay-Line Compensation Current Combiner
R_L	$R_{opt} \cdot \cos^2(\theta_c)$	$\frac{R_{opt}}{2}$	$\frac{R_{opt}}{2 \cdot \sin^2(\theta_c)}$	$\frac{R_{opt}}{2 \cdot \tan^2(\theta_c)}$
Z_T	$R_L \cdot \sqrt{2}$	$2 \cdot R_L$	–	–
X_c	–	–	$R_L \cdot \sin(2 \cdot \theta_c)$	$2 \cdot R_L \cdot \sin(\theta_c)$
B_c	$\frac{\sin(2 \cdot \theta_c)}{2 \cdot R_L}$	–	–	$\frac{1 - \cos(\theta_c)}{2 \cdot R_L \cdot \sin(\theta_c)}$

The next step is to determine the desired location for the second load trajectory intersection. A complex impedance Z_{BO} is chosen as the back-off impedance value either through calculation, or by using the load-pull contours to determine the desired power back-off and efficiency. The back-off reflection coefficient Γ_{BO} is then defined as:

$$\Gamma_{BO} = \frac{Z_{BO} - R_{opt}}{Z_{BO} + R_{opt}} \quad (C.6)$$

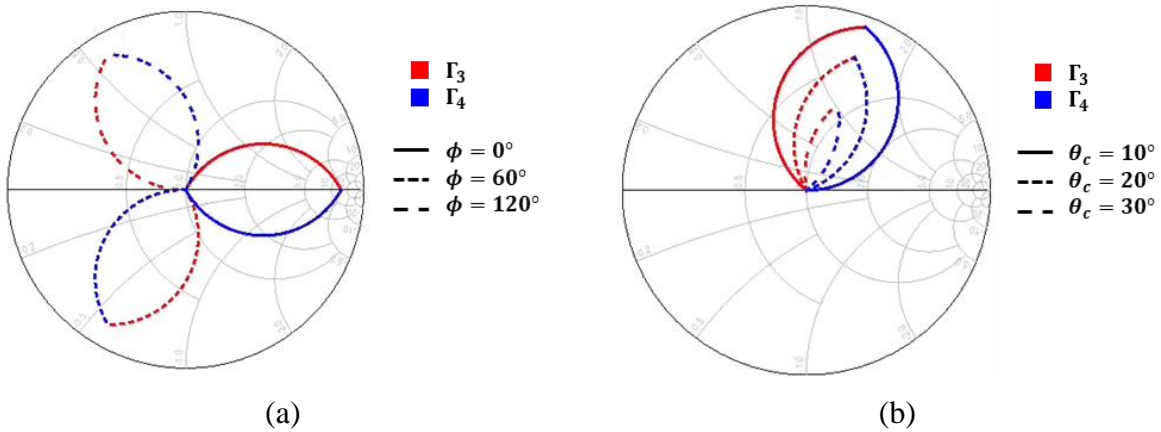


Figure C.3 – (a) Effect of ϕ on the direction of the load modulation trajectories (b) Effect of θ_c on the opening of the load modulation trajectories and the distance between the intersections

The OTL electrical length ϕ is responsible for the rotation of the load trajectories, as seen in Figure C.3(a) where the range of the Outphasing angle θ is kept restrained to $[\theta_c; 90^\circ - \theta_c]$ for clarity. The value of ϕ can be calculated for a given Γ_{BO} using (C.7).

$$\phi = 180^\circ - \frac{\arg[\Gamma_{BO}]}{2} \quad (C.7)$$

The second intersection, is also determined by the magnitude of the reflection coefficient, which depending on the type of the combiner leads to one of the equations in (C.8). The compensation angle θ_c is the remaining degree of freedom and its value would therefore directly set the distance between the two points of intersection on the Smith chart as seen in Figure C.3(b).

$$\begin{cases} \Re[Y_{VM|VC}]|_{\theta=90^\circ-\theta_c} = |\Gamma_{BO}| \\ \Re[Y_{VM|CC}]|_{\theta=\theta_c} = |\Gamma_{BO}| \end{cases} \quad (C.8)$$

Solving either of the equations in the system above leads to the value of the compensation angle θ_c which is expressed in (C.9).

$$\theta_c = \cos^{-1} \left(\sqrt{\frac{|\Gamma_{BO}| + 1}{2}} \right) \quad (C.9)$$

The described technique results in a OPA combiner suitable for class-E operation, with the impedance at Z_L being R for peak power, and Z_{BO} for back-off.

To better illustrate this method, an ideal OTL-based OEPA circuit is designed with the following input parameters:

- Design frequency $f_0 = 2.5 \text{ GHz}$
- Supply voltage $V_{DD} = 3.4 \text{ V}$
- Peak power $P_{max} = 33 \text{ dBm}$
- Back-off level impedance $Z_{BO} = 7 + j.20$
- Loaded quality factor of the class-E series resonator $Q_L = 5$

A reactive compensation current combiner is chosen as the core OPA combiner. Using the previously detailed design methods results in the OEPA circuit shown in Figure C.4 below.

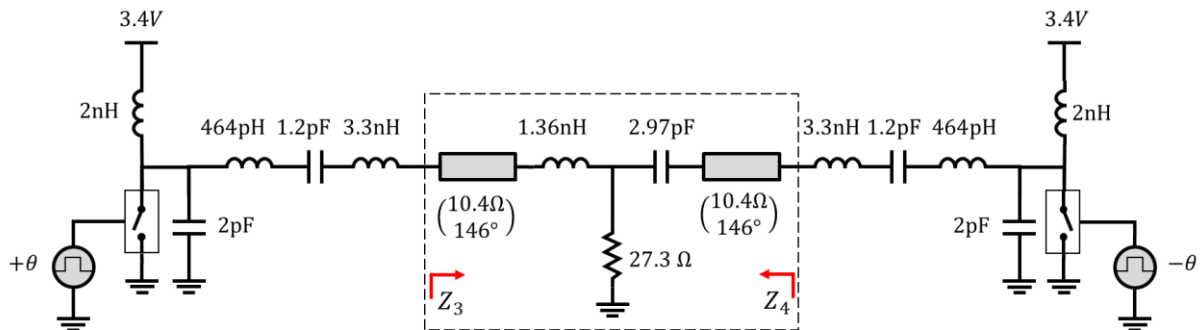


Figure C.4 – Ideal OTL-based OEPA schematic

The transistors are considered to be ideal switches with a saturation resistance of $1 \text{ m}\Omega$ added for convergence. The driving signals are square-wave pulses with a duty cycle d and phase delay $\pm\theta$. The ideal drive profiles are very non-linear and would require different duty cycle and phase difference values for each branch as pointed out in [69].

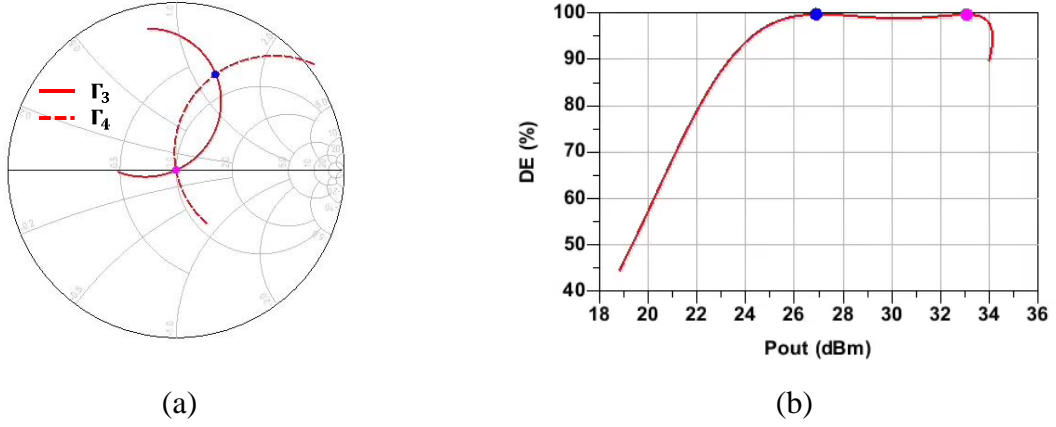


Figure C.5 – (a) OEPA load modulation trajectories (b) Efficiency versus output power of the OEPA

A simpler drive profile was considered by applying the same duty cycle $d = 0.54$ and a phase shift $\pm\theta$ to the two OEPA branches. This mode of operation results in the load modulation trajectories shown in Figure C.5(a) where the intersections occur at the normalized centre of the smith chart (magenta dot, $R_{opt} = 10.4 \Omega$) and at the chosen back-off impedance Z_{BO} (blue dot). The efficiency of the OEPA is plotted against its power output in Figure C.5(b), and shows that the intersections seen on the Smith chart correspond to maximum efficiency points ($DE = 100\%$) corresponding to $33dBm$ and $27dBm$ of output power.

This method can be generalized for any type of PA operation requiring complex impedances at both peak and back-off operation (i.e. Class-J).

C.2. Generalized Solution

It is possible to generalize the OTL-based combiner method, mainly adapted for Class-E operation, to any operation mode requiring complex impedances both at peak and back-off. This can be done by adding a reactive element X to the combiner stage as shown in Figure C..

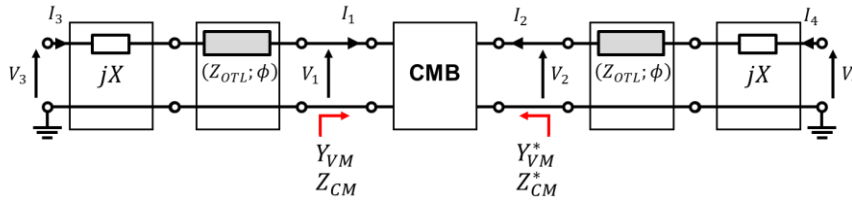


Figure C.6 – Output power evolution for ideal voltage-mode (dashed black) and the proposed OBPA design (red)

The modified combiner stage can be expressed as an ABCD matrix system which is then used to derive the required input voltages as in (C.10). The input currents equation are themselves unchanged and the results from (C.3) can be used here.

$$\mathbf{V}_{3,4} = \left(\cos(\phi) - \frac{X}{R_{opt}} \sin(\phi) + j \cdot (R_{opt} \cdot \sin(\phi) + X \cdot \cos(\phi)) \cdot \mathbf{Y}_{VM|1,2} \right) \cdot \mathbf{V}_{1,2} \quad (C.10)$$

These inputs voltages relate to the drain of the transistors as shown in Figure C.7. For correct Outphasing operation; the gate voltages $V_{GS|3,4}$ must be tuned in order to ensure the correct waveforms at the drains of the transistors.

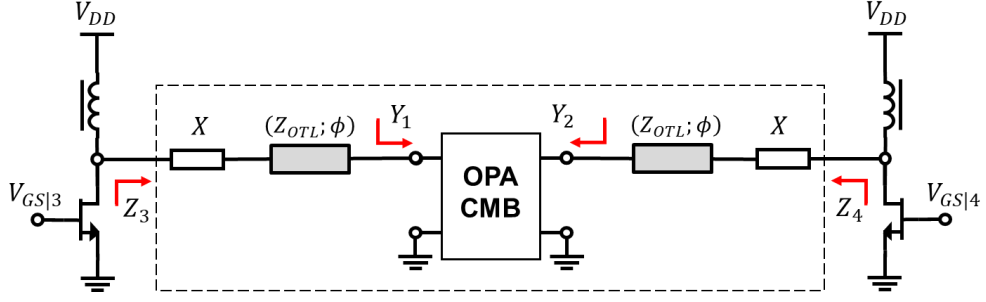


Figure C.7 – Simplified schematic of the generalized combiner design circuit

The amplifier is assumed to operate under optimal conditions when the drain impedance is defined as follows:

$$\mathbf{Z}_{3,4} = \begin{cases} \mathbf{Z}_\alpha & \text{at } P_{max} \\ \mathbf{Z}_\beta & \text{at } OBO \end{cases} \quad (C.11)$$

The method described in the previous section can still be used to calculate the values of R_L , θ_C , Z_{OTL} , and ϕ . The input variables R_{opt} , \mathbf{Z}_{BO} , and X are set using the following equations.

$$X = \Im[\mathbf{Z}_\alpha] \quad (C.12)$$

$$R_{opt} = \Re[\mathbf{Z}_\alpha] \quad (C.13)$$

$$\mathbf{Z}_{BO} = \Re[\mathbf{Z}_\beta] + j \cdot (\Im[\mathbf{Z}_\beta] - X) \quad (C.14)$$

Finally, the designed combiner, when driven correctly, leads to the trajectories in Figure C.8(a), which intersect at \mathbf{Z}_α and \mathbf{Z}_β . The representation of the trajectories can be improved by normalizing the Smith chart to \mathbf{Z}_α^* , as was done in Figure C.8(b).

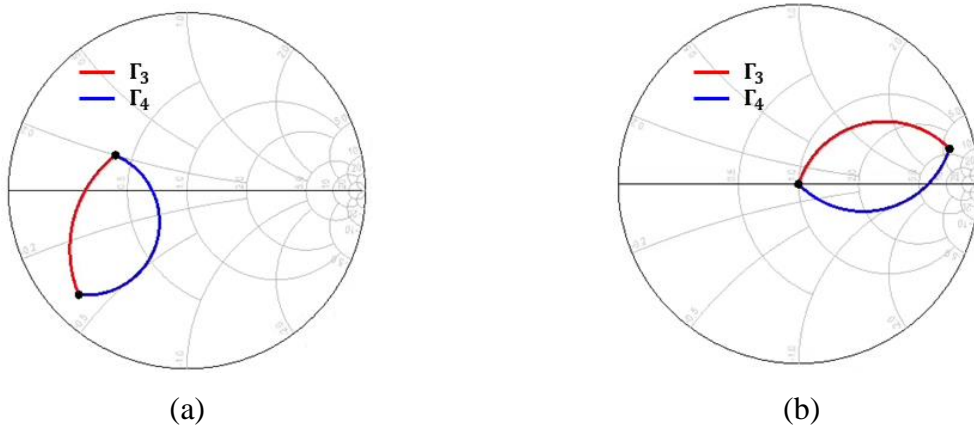


Figure C.8 – (a) Complex load modulation trajectories referenced at 50Ω (b) Complex load modulation trajectories referenced at \mathbf{Z}_α^*

Résumé de la Thèse

Les normes de communication mobile sont en constante évolution. Chaque nouvelle génération apporte davantage de fonctionnalités et d'améliorations des performances. Cela se fait toutefois au prix d'exigences plus strictes en termes de largeur de bande du signal, de linéarité et de nombre de bandes prises en charge, pour n'en citer que quelques-unes. Par conséquent, les architectures frontales de radiofréquence sont devenues plus complexes. L'amplificateur de puissance joue un rôle essentiel dans la chaîne d'émission, car il est responsable de la plus grande consommation d'énergie du module frontal. De plus, sa linéarité affecte directement la qualité du signal transmis. Ce travail aborde donc la conception et l'intégration d'un amplificateur de puissance à haut rendement pour les applications 5G.

L'une des particularités des nouveaux signaux 5G, est leur rapport élevé entre la puissance de crête et la puissance moyenne (entre 7 et 10dB). Cela signifie que l'amplificateur de puissance doit fonctionner la plupart du temps en retrait de puissance (back-off). Cela crée un problème pour les amplificateurs de puissance typiques tels que les classes A, AB, B et C et la classe E, car ils ont tous une faible efficacité au back-off. Cependant, les architectures d'amplificateur de puissance à modulation de charge, telles que Doherty et Outphasing, présentent une efficacité élevée à la fois à la puissance de crête et aux niveaux de back-off, ce qui les rends parfait pour les applications 5G.

En mode Outphasing, un signal modulé est divisé en deux signaux à enveloppe constante avec un déphasage relatif de 2θ . Chaque signal est ensuite amplifié séparément avant d'être recombinaé et injecté dans la même charge de sortie. En conséquence, l'impédance de charge vue par chaque branche est modulée, et devient purement réelle à la puissance de crête et de back-off. Cela conduit à son tour à deux pics de rendement aux niveaux de puissance susmentionnés.

Par ailleurs, un amplificateur de puissance Doherty typique est composé d'un amplificateur principal dit Main et d'un amplificateur auxiliaire dit Auxiliary, tous deux connectés à une seule charge par le biais du circuit combinateur. Pour les faibles niveaux de puissance, seul l'amplificateur Main est actif. Lorsque l'amplificateur Main atteint la saturation, l'amplificateur Auxiliary entre en jeu, injectant du courant dans la charge commune, modulant ainsi l'impédance de charge vue par l'amplificateur Main. Par conséquent, l'amplificateur de puissance Doherty présente deux pics d'efficacité : le premier se produit lorsque l'amplificateur Main sature au moment du back-off, et le second se produit au moment du pic de puissance, lorsque l'amplificateur Main et l'amplificateur Auxiliary atteignent tous deux la saturation.

Dans les architectures Doherty et Outphasing, l'étage de combinaison joue un rôle crucial dans la performance globale de l'amplificateur de puissance. Par conséquent, ce travail se concentre sur l'analyse et la compréhension du fonctionnement des combineurs afin de proposer des méthodologies de conception optimisées. Tous les combineurs Outphasing existants sont dérivés de la même architecture initialement proposée par Chireix et sont regroupés en deux catégories : les combineurs à compensation réactive et les combineurs à compensation par ligne à retard. En outre, les deux modes de commande Outphasing sont expliqués et il est démontré qu'ils sont compatibles avec les deux catégories de combineurs. Enfin, une nouvelle méthodologie unifiée de conception des combineurs Outphasing est proposée.

De même, une nouvelle méthode d'analyse est proposée pour les combineurs Doherty. Les méthodes existantes se contentent de vérifier les conditions Doherty aux niveaux de crête et de back-off, sans tenir compte de ce qui peut se passer entre ces deux points. La méthode proposée résout ce problème et garantit que les conditions idéales Doherty sont respectées dans toute la

région de Doherty. En outre, cette technique donne le back-off maximal réalisable pour une architecture de combineur donnée ainsi que les profils de courant d'entrée nécessaires pour l'atteindre. À titre d'exemple, le combineur LC compact de [57] est analysé et montre qu'il est capable de fonctionner avec un back-off de 7dB alors que les auteurs de l'article original n'étaient capables d'atteindre que 3dB de back-off.

La méthodologie d'analyse du combineur DPA proposée est ensuite validée par la conception, la mise en œuvre et la mesure d'un DPA de classe E utilisant le combineur LC compact. L'étage de puissance du DPA a été conçu en premier. Des simulations de type load-pull de la classe E sont utilisées pour générer les contours de puissance et d'efficacité des deux cellules de puissance. Les paramètres optimaux du réseau d'adaptation de classe E sont ensuite déterminés en superposant les trajectoires de modulation de la charge du combineur LC aux contours de load-pull. L'étage de puissance est ensuite adapté à des terminaisons 50Ω et vérifié pour les problèmes de stabilité à l'aide des paramètres S et de la méthode d'admittance du point de drive. Ensuite, un étage driver est ajouté à l'étage de puissance et les deux blocs sont connectés à travers le réseau d'adaptation inter-étages. La conception finale du circuit à deux étages est réglée de manière à présenter des performances optimales. La technologie RFSOI 130 nm est choisie pour le circuit intégré qui devait être monté sur le boîtier à l'aide de piliers en cuivre. Compte tenu des dimensions requises du CuP, un μ PCB laminé à quatre couches est choisi comme technologie de packaging.

Les éléments conçus du circuit DPA sont implémentés sur les différentes technologies. Le circuit implémenté est ensuite simulé à l'aide de simulations électromagnétiques (EM) afin d'obtenir des résultats plus précis. Le circuit fabriqué est mesuré et validé en comparant ses résultats mesurés en DC, SP et CW avec ceux du modèle de simulation EM. En raison d'un problème de processus de fabrication, la fréquence centrale est décalée vers le bas de 2,5 GHz à 2,3 GHz, et des pertes supplémentaires sont introduites dans l'étage OMN. A 2,3GHz, la puissance de saturation du DPA est de 32dBm et le PAE de pointe est de 51%. A 6dB de back-off, le PA maintient une efficacité élevée de 36%.

Les mesures des signaux modulés sont effectuées en utilisant un signal LTE de 10 MHz avec DPD. A 2.3GHz, le DPA délivre une puissance de sortie de 28dBm avec 43% de PAE pour un niveau d'ACLR de -35dBc. La comparaison avec d'autres travaux publiés montre que les performances du DPA sont conformes à l'état de l'art, ce qui valide davantage l'approche.

L'architecture du PA à modulation de charge outphasing est explorée. Une première étude est menée en utilisant un modèle de transistor idéal dans une architecture OPA de classe B avec un combineur de tension de compensation réactive (LC combiner). Elle est ensuite suivie d'une mise en œuvre d'un OPA de classe E qui introduit deux formes différentes d'optimisation : La première, basée sur le travail effectué par Beltran et Raab, utilise des lignes de transmission décalées afin de fournir au PA la charge complexe requise à OBO. La seconde, proposée par Ghahermani, utilise les paramètres de conception de la puissance de classe E pour faire pivoter les contours de la puissance et de l'efficacité du load-pull et ainsi rendre réelle l'impédance de back-off optimale. Un OPA de classe E à modulation de charge à deux entrées est ensuite conçu à l'aide d'un modèle électrique LDMOS pour fournir une puissance de sortie de 33 dBm à $f_0 = 2.5GHz$. L'OEPA est simulé avec différents niveaux de puissance d'entrée ainsi qu'un déphasage de branche $\pm\theta$.

Afin de mieux comprendre et d'analyser les exigences du système d'un émetteur outphasing (OTX), une analyse au niveau du système a été réalisée. Les blocs SCS, OPA et DPD ont été représentés et étudiés du point de vue du traitement du signal, ce qui a conduit à deux propositions d'architecture DPD. La première est l'approche basée sur une DPD tabulée (LUT):

elle utilise une caractérisation CW extensive du circuit OPA RF afin de construire une LUT de valeurs de puissance et de phase d'entrée qui satisfait un critère de performance prédéterminé tel qu'un fonctionnement à haut rendement ou une linéarité élevée. La deuxième architecture est plus avancée et s'appuie sur le modèle comportemental du PA. Cette méthode, appelée DPD In-SCS, est basée sur l'architecture DPD à apprentissage indirect et détermine un bloc post-inverse du système OPA MISO afin de l'utiliser comme pré-inverse et ainsi linéariser le système OTX.

Enfin, le processus de modélisation du PA est brièvement exposé et un modèle de type polynôme à mémoire (MP) est choisi comme point de départ. La construction du modèle PA nécessite de nombreuses mesures à l'aide de signaux modulés. Malheureusement, un circuit intégré OPA n'a pas pu être réalisé dans les contraintes de temps de ce travail. Cette section finale sert donc de base aux travaux futurs sur les systèmes OTX.

Titre : Conception et implémentation d'architectures d'amplificateurs de puissance à haute efficacité pour des applications 5G.

Mots clés : 5G ; Amplificateur de puissance ; SOI ; Outphasing ; Doherty

Résumé : La complexité croissante des schémas de modulation due à l'évolution des normes de communication mobile a conduit à des signaux à fort rapport puissance de crête/puissance moyenne (PAPR). En conséquence, les architectures traditionnelles d'amplificateurs de puissance (PA) linéaires ne sont plus adaptées car elles présentent un faible rendement moyen lorsqu'elles fonctionnent avec de tels signaux. Une des solutions possibles à ce problème est l'utilisation d'architectures basées sur la modulation de charge qui sont capables de fournir un rendement moyen plus élevé. Ce travail se concentre sur l'analyse, la conception et la mise en œuvre des deux principales architectures à modulation de charge : Outphasing (OPA) et Doherty (DPA). L'architecture Outphasing est étudiée sous ses différentes formes et une nouvelle méthode de conception unifiée est proposée pour les combineurs OPA. Une seconde analyse est menée sur les combineurs DPA, aboutissant à une nouvelle méthode d'analyse capable de déterminer le back-off maximal réalisable par une architecture de combineur donnée en mode Doherty. Contrairement aux travaux existants, la méthode proposée détermine également les courants d'attaque requis aux entrées du combineur pour maintenir des conditions idéales de Doherty dans toute la région de Doherty. Afin de valider cette technique, un DPA en classe E à deux étages avec un

combineur LC compact est conçu et implémenté en utilisant la technologie RF-SOI en 130nm. Les performances mesurées sont en ligne avec l'état de l'art puisque le PA atteint un PAE maximum de 51% à une puissance de sortie de 32dBm sous une tension d'alimentation de 3,4V à 2,3GHz en mode CW. De 2,1 GHz à 2,5 GHz, le PA présente une puissance de sortie moyenne et un PAE supérieur à 26,9 dBm et 39% respectivement à -35 dBc E-UTRA ACLR lors de l'utilisation d'un signal de liaison montante LTE 10MHz-50RB QPSK avec prédistorsion digitale (DPD) sans mémoire. À 2,3GHz, le PA atteint un Pout linéaire et un PAE de 28,85 dBm et 42,8% respectivement. Ensuite, une analyse de système est effectuée sur le système émetteur Outphasing (OTX) qui contient à la fois l'OPA RF ainsi que l'interface de traitement du signal et l'interface analogique connue sous le nom de séparateur de composantes signal (SCS). La conception et le fonctionnement de l'OPA en classe B et en classe E sont étudiés, ce qui aboutit à la conception d'un OPA de classe E à double entrée. Différentes architectures de DPD sont étudiées, notamment la DPD tabulée (look-up table) et les architectures basées sur la modélisation comportementale. Enfin, une architecture DPD IN-SCS est proposée comme une nouvelle solution potentielle permettant l'intégration du bloc DPD dans le SCS, fournissant une base pour de futures recherches.

Title : Design and Implementation of High Efficiency Power Amplifiers for 5G Applications.

Keywords : 5G ; Power Amplifier ; SOI ; Outphasing ; Doherty

Abstract: The increasing complexity of modulation schemes brought on by the evolution of mobile communication standards has led to high peak to average power ratio (PAPR) signals. As a result, traditional linear power amplifier (PA) architectures are no longer suitable as they exhibit low average efficiency when operating with such signals. One of the possible solutions to this issue is load modulation-based architectures which are capable of providing higher average efficiency. This work focuses on the analysis, design, and implementation of the two main load modulation architectures: Outphasing (OPA) and Doherty (DPA). The Outphasing architecture is studied under its different forms and a new unified design method is proposed for OPA combiners. A second analysis is conducted on DPA combiners, resulting in a new analysis method capable of determining the maximum back-off achievable by a given combiner architecture in Doherty mode. Unlike existing works, the proposed method also determines the required driving currents at the inputs of the combiner to maintain ideal Doherty conditions throughout the Doherty region.

In order to validate this technique, a two-stage class-E DPA with compact LC combiner is designed and implemented using 130nm RF-SOI. Measured performance is in-line with the state of the art as the PA achieves a peak PAE of 51% at 32dBm output power under 3.4V supply voltage at 2.3GHz in CW mode. From 2.1GHz to 2.5GHz, the PA shows an average output power and PAE higher than 26.9dBm and 39% respectively at -35dBc E-UTRA ACLR when using a 10MHz-50RB QPSK LTE uplink signal with memoryless digital predistortion (DPD). At 2.3GHz, the PA achieves a linear Pout and PAE of 28.85dBm and 42.8% respectively. Next, a system analysis is performed on the Outphasing transmitter system (OTX) which contains both the RF OPA as well as the signal processing interface and analog interface known as the signal component separator (SCS). The design and operation of OPA in both class-B and class-E is studied resulting in a dual-input class-E OPA design. Different DPD architectures are studied including the look-up table DPD and the behavioural modelling-based architectures. Finally, an IN-SCS DPD architecture is put forward as a potential novel solution allowing the integration of the DPD block into the SCS providing a basis for future research.