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Analyse des mécanismes de pollution d'une alimentation à découpage sur des fonctions analogiques embarquées sur un même " Système sur Puce " et développement de techniques de minimisation du bruit de l'alimentation à découpage

Eric Feltrin

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Analyse des mécanismes de pollution d'une alimentation à découpage sur des fonctions analogiques embarquées sur un même « Système sur Puce » et développement de techniques de minimisation du bruit de l'alimentation à découpage.

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Abstract

The micro-controller market is undergoing changes and is expected to grow quickly promoted by the Internet-of-Things (IoT) development. Calculation capability, connectivity, analog performances and power efficiency are key enablers.

Power management unit is co-integrated with the micro-controller so that only few off-chip passive components are necessary. The embedded power management unit must deliver the micro-controller input voltage along with the power demand which increases with the computation capability. The chosen architecture has to optimize the efficiency in high and low power mode but without impacting analog performance of sensitive IPs (Intellectual Property).

The active part of an inductive buck converter is integrated but some switching noise is observed that severely impact analog IPs.

The objective of this work is the analysis of the noise generation from the power stage and its propagation in the System-on-Chip (SoC).

The generation model is constituted of a RLC equivalent circuits in each state of the power stage. The R, L and C expressions are detailed depending on physical parasitic components. These models permit to understand noise mechanisms and to give an estimation of the noise amplitude and frequency resonance. The models show the degrees of freedom to manage the noise signature.

The whole system, i.e. the electronic board, the package and the chip, is modeled to extract the system-level propagation path between the buck converter and sensitive IPs.

These models are verified by measurement on a test vehicle.

Finally three solutions are presented to reduce the buck converter noise impact: two changes in the power stage architecture to reduce noise generation and one modification of the top routing of the power delivery network to improve isolation between parts of the circuit regarding noise susceptibility.

The thesis contributes an original methodology to build the missing models at system-level regarding noise generation and propagation from the switching power supply. Knowledge has been acquired, experimentally verified and supported by the design of a demonstrator (to be tested).

Résumé

Le marché des microcontrôleurs est en pleine mutation et devrait croître propulsé par le développement de l'Internet des objets. La puissance de calcul, la connectivité, les performances des périphériques et l'efficacité énergétique sont les facteurs clés de ce développement.

Le module de gestion de l'alimentation est entièrement intégré au sein même du microcontrôleur lui permettant de fonctionner avec uniquement quelques composants passifs. Ce module doit assurer le maintien de la tension d'alimentation indépendamment de la consommation du microcontrôleur qui augmente avec la puissance de calcul. L'architecture choisie doit également optimiser le rendement selon la consommation du microcontrôleur sans impacter le fonctionnement de blocs sensibles.

L'intégration de l'étage de puissance d'une alimentation à découpage engendre du bruit de commutation ayant un impact sur les fonctions analogiques du circuit.

L'objectif de ce travail est l'analyse de la génération du bruit par l'étage de puissance et sa propagation au sein du circuit complexe.

Le modèle de génération du bruit est constitué de circuits RLC équivalents. Les expressions des R , L et du C sont exprimées dans chaque état de l'étage de puissance en fonction des composants parasites du système. Ces modèles permettent de comprendre le mécanisme de génération du bruit et de donner une estimation de l'amplitude et de la fréquence des résonances.

L'ensemble du système c'est-à-dire le circuit, le boîtier et la carte électroniques, est modélisé pour extraire les chemins de propagation entre l'alimentation à découpage et les cellules sensibles du système.

Ces modèles sont vérifiés en mesurant un circuit de test.

Finalement trois solutions sont proposées pour réduire l'impact du bruit de l'alimentation à découpage : deux changements dans l'architecture de l'étage de puissance pour réduire la génération du bruit et une modification des interconnexions globales du circuit pour améliorer l'isolation entre les différentes parties du système.

Cette thèse présente une méthodologie originale pour construire un modèle au niveau système de la génération et de la propagation du bruit de commutation. Les connaissances acquises ont été vérifiées expérimentalement et appuyées par la conception d'un démonstrateur (qui doit être testé).

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List of Acronyms

ADC	: Analog to Digital Converter
BEM	: Boundary Element Method
CCM	: Continuous Current Mode
CPSW	: Core-less Planar Spiral Windings
CWS	: Coupling Wave Solution
DC/DC	: Direct Current to Direct Current conversion
DNW	: Deep NW, buried below NW
EMC	: ElectroMagnetic Compatibility
ENOB	: Effective Number Of Bit
FEM	: Finite Element Method
FFA	: Fast PMOS Fast NMOS Analog corner
FFT	: Fast Fourier Transform
IC	: Integrated Circuit
I/O	: Input/Output
IoT	: Internet of Things
IP	: Intellectual Property
LDO	: Low Drop Output
MoM	: Method of Moment
MOSFET	: Metal Oxide Semi-conductor Field Effect Transistor
NMOS	: Negative MOSFET, drain and source are NW
NW	: Negative implanted Well
PCB	: Printed Circuit Board
PDN	: Power distribution Network
PMOS	: Positive MOSFET, drain and source are PW
PW	: Positive implanted Well
RF	: Radio Frequency
SAR	: Successive Approximation Register
SMPS	: Switched Mode Power Supply
SoC	: System on Chip
SSA	: Slow PMOS Slow NMOS Analog corner
STM32	: 32 bits STMicroelectronics micro-controller
TQFP	: Thin Quad Flat Package
VNA	: Vector Network Analyzer
WLCSP	: Wafer Level Chip Scale Package

1 Introduction

Micro-controllers are microelectronic circuits in which all computing components are integrated. The instructions are stored in a non-volatile memory and only the power supply is needed for operation. The interface with outside environment is ensured by programmable Input/Output peripherals (I/Os): digital, analog, power or even RF pins.

The micro-controller market is undergoing changes and is expected to grow quickly promoted by the Internet-of-Things (IoT) development. The portion of IoT applications in the micro-controller market is presented in Figure 1.1 [1]. The IoT purposes to give an identifier to every physical devices including everyday sensors, tools, cars or even living entities. It will allow communication between themselves by extending Internet to (nearly) everything.

1.1 What are the challenges?

IoT requires smarter devices (consumer electronic), power efficiency for low power mode management (wearable, smart-phone and tablet), connectivity (automotive, metering) and compact designs (more functionality in the same volume, standalone chip).

From these concerns, the differentiation relies on three parameters: the computation capability, the power efficiency and the analog functionality.

The micro-controller computation capability which is often proportional to the clock processor frequency, has grown significantly over the last ten years (from $50MHz$ to $400MHz$) and NXP introduced a dual core micro-controller in 2012. The power consumption decreases (from $300\mu A/MHz$ to $40\mu A/MHz$), an ultra low power mode was introduced with less than $200nA$ consumption and in 2012, Microchip moved from LDO to SMPS to reduce the consumption by half. Analog functionality was improved: high resolution (16 bits) Analog to Digital Converter (ADC) and RF transmitters (Bluetooth, WiFi, Zigbee) were embedded with the micro-controller. Power management (active part) is integrated so the micro-controller can operate with only few off-chip passive components. Some demonstrators integrate even the capacitors and inductors inside the package [6]. This technology is not yet used as a mainstream in micro-controller circuits due to surface and cost restriction.

The main challenges of the power management unit are:

- to deliver the output power demand, which increases with computation capability;

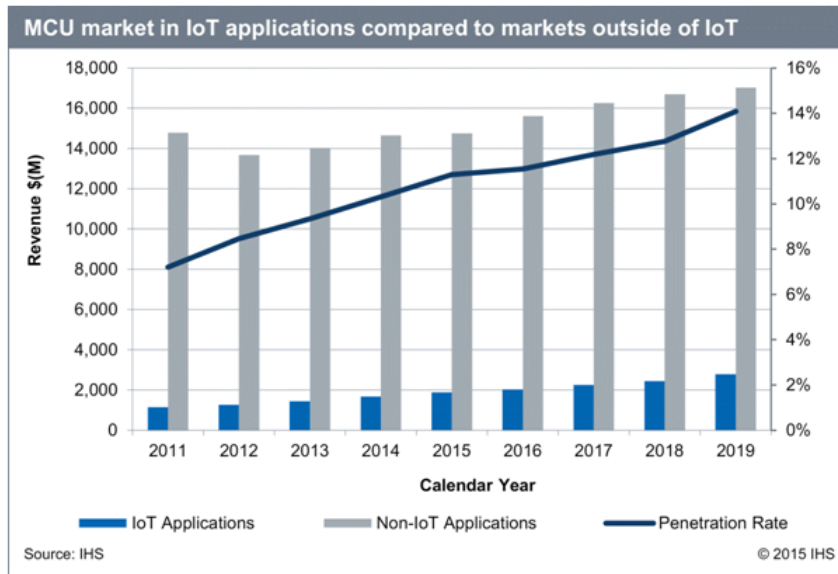


Figure 1.1 – IoT impact on micro-controller market - IHS 2015 [1]

- to optimize efficiency in high and low power modes;
- to not degrade analog performances of sensitive IPs.

The power management architecture must be chosen wisely to satisfy these requirements.

1.2 Why using a SMPS?

The IC power module supplies the computation core with adapted voltage levels. In this case, the input voltage from 1.6V to 3.6V is stepped down to 1.2V at the output. The power module must remain efficient and reliable for any voltage in this range.

Three structures may be considered: Low-Drop-Out (LDO) regulators, capacitive and inductive Switched Mode Power Supplies (SMPS). When used to step down the input voltage, the SMPS structure is called a buck converter. This denomination will be used in the rest of the report. The operation, advantages, and drawbacks of each architecture are further described in the following section.

1.2.1 Low-Drop-Out (LDO) regulators

The LDO structural schematic is presented in Figure 1.2a. The output capacitor C_{out} is filled with charge to a desired voltage ($V_{out} = \frac{Q_{out}}{C_{out}}$). The charging current is modified depending on current demand I_{out} to maintain V_{out} . In a CMOS process the variable current source is made of a PMOS whose gate potential is adjusted to obtain the desired I_{out} [7].

The input power is $P_{in} = V_{in}(I_{out} + I_{ldo})$ with I_{ldo} the current consumption in the regulation loop. As this current is negligible versus I_{out} ($\frac{I_{ldo}}{I_{out}} \approx 1000$), P_{in} is approximated to $V_{in}I_{out}$. The output power is $P_{out} = V_{out}I_{out}$ so the

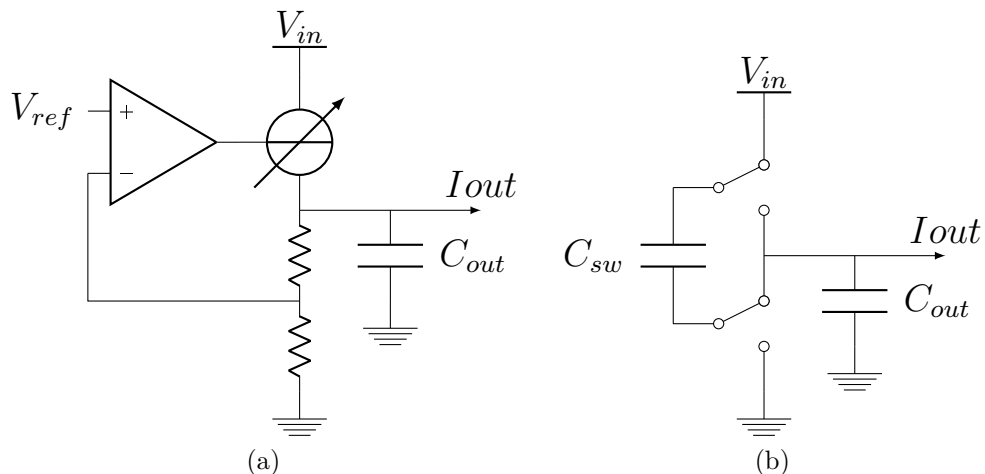


Figure 1.2 – Structural schematic of a LDO (a) and a capacitive buck converter (b)

theoretical efficiency is $\eta_{th} = \frac{P_{out}}{P_{in}} = \frac{V_{out}}{V_{in}}$ and in our case $\eta_{th} \in [0.33, 0.75]$ [8]. In practice, the efficiency is degraded by the package impedance, the PMOS r_{dson} and other parasitic impedances.

The pros of the structure are its "simplicity", the fast transient response (adjustable with the amplifier specification) and the low noise contribution (no switching). The main con is the efficiency, less than 33% in the worst case, causing performance degradation in low power mode but also creating thermal issue in high power mode, due to the large amount of energy dissipated in the main (P)MOSFET.

1.2.2 Capacitive step-down converter

The capacitive step-down converter structural schematic is presented in Figure 1.2b. The output capacitor C_{out} is filled with charge during each period. A smaller capacitor C_{sw} is charged at potential $V_{in} - V_{out}$ and then is connected between output and ground to transfer charge to the output capacitor C_{out} . The injected charge decrease when V_{out} grows. In steady state, the net charge transfer is balanced and $V_{in} - V_{out} = V_{out} - 0 \implies V_{out} = \frac{V_{in}}{2}$ [9].

The efficiency of the structure is impacted by the ESR of the capacitance and R_{on} of the switches, that depend on design parameters and parasitic impedances. For integer ratios of output to input voltages, the structure has a good efficiency and could be integrated in some process technologies (with high capacitor density available). Literature reports capacitive buck converter structure with efficiency around 80% [9]. The efficiency is degraded in low power mode but some techniques, like frequency scaling, permit to keep a descent efficiency in this case (switching losses reduction) [10].

In the present case, the value of the maximum output current implies large capacitors to be integrated (few μF), needing a large silicon area incompatible with cost constraints. The output voltage is a fraction of the input voltage and cannot be fixed independently. In the case of a drop in the input voltage (for

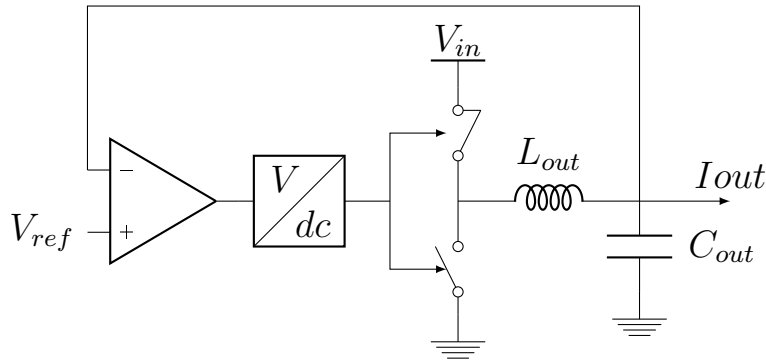


Figure 1.3 – Structural schematic of an inductive buck converter

example battery discharge), the output voltage will follow this drop preventing the satisfying operation of the system. To solve this issue the capacitive structure regulates at higher voltage and increases resistive losses to achieve the desired voltage. This degrades the efficiency as presented in [11]. Moreover the growth in number of required output voltage levels implies a larger number of switches and capacitors, negatively affecting the efficiency of the system and requiring the use of many I/Os (two for each capacitors). Another con, along with external passive components is that the switching activity in package parasitic impedance is noisy.

1.2.3 Inductive buck converter

The inductive buck converter structural schematic is presented in Figure 1.3. The current flowing through the inductor L_{out} is regulated to charge the output capacitor C_{out} to the desired voltage. When the high-side switch is closed, the current increases as $L_{out} \frac{dI_{out}}{dt} = V_{in} - V_{out}$ whereas when the low-side switch is closed, the current decreases as $L_{out} \frac{dI_{out}}{dt} = -V_{out}$. By duty cycle (α) adjustment, the current is regulated to charge the capacitor to V_{ref} and to match the output current I_{out} demand. The adjustment methods are various (voltage, current or hysteretic mode) and well described in the literature [12].

The efficiency of the structure is similar to the capacitive one. The switching losses, R_{dson} , and parasitic impedances are responsible for efficiency degradation. To keep a descent efficiency in low power mode, pulse skipping techniques are used. Instead of injecting systematically a small amount of energy, a minimum is injected once and the system waits for this energy to be consumed, "skipping pulses", before re-injection. This reduces switching frequency and so switching losses [13]. Some literature efficiency results are presented in Table 1.1.

A buck converter with a state of the art architecture can achieve efficiency above 90% in the studied range. In the structure in [15], the passive devices are on interposer inside the same package. The efficiency for an output voltage of 1.2V is above 80% for current larger than 100mA. This topology is however expensive and not realistic for mass market product for now. When the buck converter is integrated in a micro-controller, the efficiency is still above 80%

1.3. What is noisy in a buck converter?

Reference	V_{in} (V)	V_{out} (V)	I_{out} (mA)	Efficiency
O. Trescases [14]	2.7	1.8	1 – 1000	82% – 91%
F. Neveu [15]	3.6	1.2 – 2.4	0 – 300	up to 91.5%
C. H. Huang [16]	3 – 3.6	1 – 1.8	1 – 500	90% – 97%
Microchip SAM4L [17]	2 – 3.6	1.7	5 – 50	82% – 95%

Table 1.1 – Partial state of the art of inductive buck converter efficiency

Architecture	LDO	Capacitive	Inductive
Pros	<ul style="list-style-type: none">• simplicity• fast transient• low noise		<ul style="list-style-type: none">• efficiency
Cons	<ul style="list-style-type: none">• bad efficiency	<ul style="list-style-type: none">• I/Os number• bad efficiency• switching noise	<ul style="list-style-type: none">• switching noise• complexity

Table 1.2 – Power management structure pros and cons for micro-controller context

(Microchip SAM4L [17]).

The pro of inductive buck converter architecture is the satisfying efficiency but the cons are the switching activity which generates noise at the board level and inside the chip (interacting with micro-controller and other IPs) and the relatively complex structure which has an impact on the power management area.

The pros and cons of each architecture are summarized in Table 1.2.

STMicroelectronics chooses to integrate an inductive switch power module inside the most recent STM32 micro-controller as only two passive components are required off-chip for a large range of voltage ratios. The high-side switch is a PMOS and the low-side switch is a NMOS. To improve transient response, asynchronous feedback has been added to the system increasing its complexity [18]. The area of the SMPS structure, larger than the one of a LDO, is small compared to the whole IC surface. A major con remains: the switching noise. This noise could negatively impact performance of the sensitive analog IPs of the micro-controller. The micro-controller context is presented in Figure 1.4. The noise pollutes analog IPs by two main paths: by power supply pairs connected on PCB or directly on-chip by substrate crosstalk.

A study on noise generation and its impact is needed to guarantee a satisfying operation of the sensitive analog blocks in micro-controller.

1.3 What is noisy in a buck converter?

1.3.1 Noise mechanism

Independent on the the feed-back control method, the power stage of a buck converter is quite identical: a PMOS and a NMOS [12]. The control

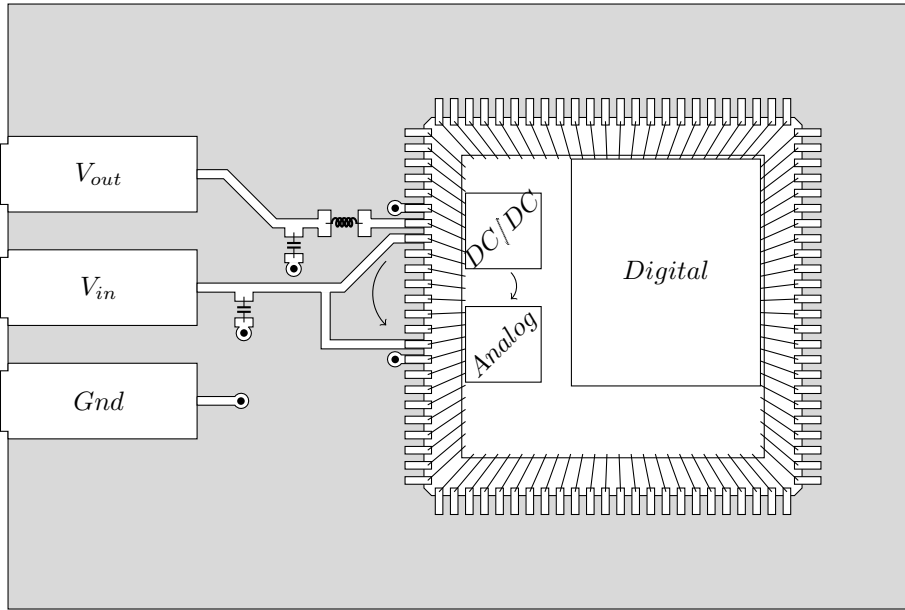


Figure 1.4 – Buck converter inside the micro-controller

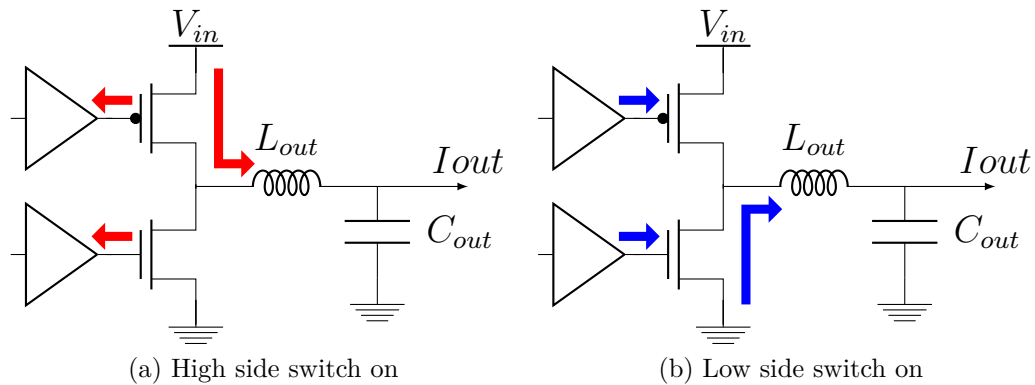


Figure 1.5 – Buck converter current paths

loop turns on and off the two switches alternatively. To improve efficiency, the on-resistance of the MOSFET, R_{dson} must be reduced and the switching be as fast as possible. To have low R_{dson} and to tolerate a high current level, MOSFET widths are large. Consequently the gate capacitors are big and need powerful drivers to switch quickly resulting in a large inrush current during gate charging. Moreover the inductor current, I_{Lout} switches between PMOS and NMOS channel. All these current variations presented in Figure 1.5, stimulate the parasitic resonant network also called the Power Delivery Network (PDN). The consequent fluctuations of the supply voltage level, called switching noise, are presented in Figure 1.6.

1.3. What is noisy in a buck converter?

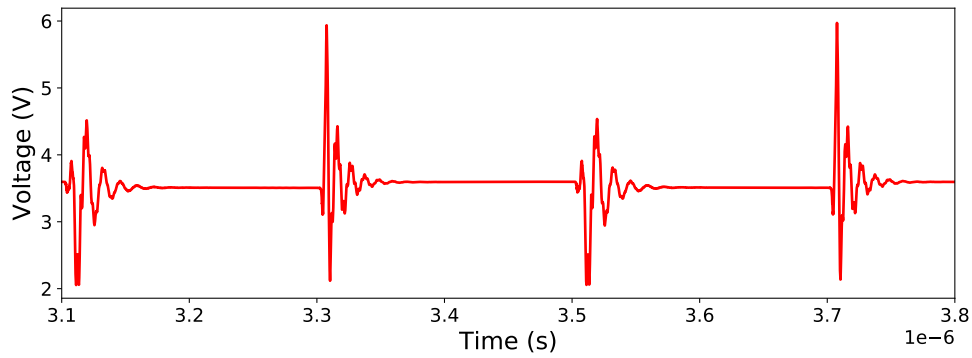


Figure 1.6 – Example of fluctuations of the buck converter input voltage

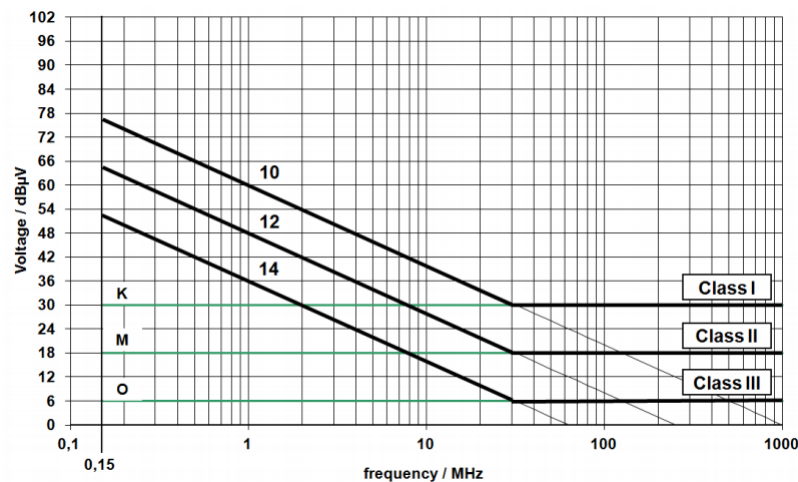


Figure 1.7 – Limit line set 1Ω emission test method for global pins [2]

1.3.2 Noise on PCB

Standards have been fixed for ElectroMagnetic Compatibility (EMC) between Integrated Circuits (IC). The emission measurement procedure are described in IEC-61967 [19] and immunity in IEC-62132 [20]. For measurement of conducted emission through the power supply, the 1Ω probe method is used. A 1Ω resistor is placed on ground path with 49Ω connected to the measurement equipment (50Ω adapted). The pattern of emission classification is illustrated in Figure 1.7 from ZVEI - Generic IC EMC Test Specification report [2].

This measurement setup is difficult to transpose to the IC context. First 1Ω on ground path is too high for power range of micro-controller: $0.5mA$ through 1Ω creates a drop of $0.5V$ which is significant considering the voltage range [$1.6V$, $3.6V$]. The resistor value may be adapted to 0.1Ω with 49.9Ω integrated resistors. A second issue is the distributed aspect of the Power Distribution Network (PDN) and of the substrate junctions. It is not possible to place resistors crossed by all emitted current from the SMPS.

A lot of studies have been made about PCB PDN analysis and design of passive [21] or active [22] filters to reject noise generated by the SMPS in power supply interconnections. Even some optimization algorithms have been

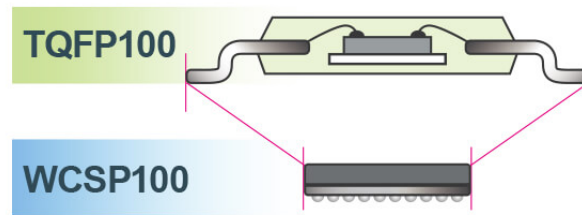


Figure 1.8 – TQFP and WL-CSP size comparison

reported [23].

In case of EMC inside a chip, the PDN filter needs passive components with large values, which are difficult to integrate. In [24], the filter is implemented on PCB using Coreless Planar Spiral Windings (CPSW). To filter the noise emitted by a $1MHz$ SMPS operation, the inductor diameter is $40mm$ which could not be integrated but is efficient to reduce PCB pollution between different signals, power and ground pins of the chip.

1.3.3 Technology dependency

Change in technology implies variations in power MOSFET characteristics. There are changes in oxide thickness and doping profiles which influence gate and junction capacitances. To support the supply voltage ($V_{dd_{max}} = 3.6V$), the gate oxide thickness has a minimum value which limits channel length scale down. Moreover a small R_{dson} is needed to keep the power efficiency value so the change in current paths of I_{Lout} does not depend on technology.

The parasitic impedances of the package have an important role in noise switching level of the buck converter. A Wafer-Level Chip-Scale Package (WL-CSP) where solder balls are connected to chip without bonding presents a very low parasitic impedance (less than $1nH$ inductance) compared to Thin Quad Flat Package (TQFP) with long bonding ($\sim 10nH$ for a TQFP100 and a $16mm^2$ die). For micro-controller market where the chip is used in many different packages, the worst situation has to be taken into account: the TQFP will be the vehicle package considered in the study.

1.3.4 System solutions

Solutions of spreading or scattering the spectrum of the input and output of the buck converter have been investigated to reduce the noise at the system level. The noise spectrum is constituted of harmonics of the switching frequency, f_{sw} . An FFT of the supply voltage obtained by simulation is presented in Figure 1.9. Spreading these harmonics should permit to highly reduce the noise maximum magnitude.

A first solution is a random phase shifting of the high-side switch conduction phase as presented in [25]. Another solution is to use a $\Sigma\Delta$ converter on the error signal to shape the noise outside the operating bandwidth [26]. A last proposed solution uses frequency hopping as described in [3]: the SMPS

1.3. What is noisy in a buck converter?

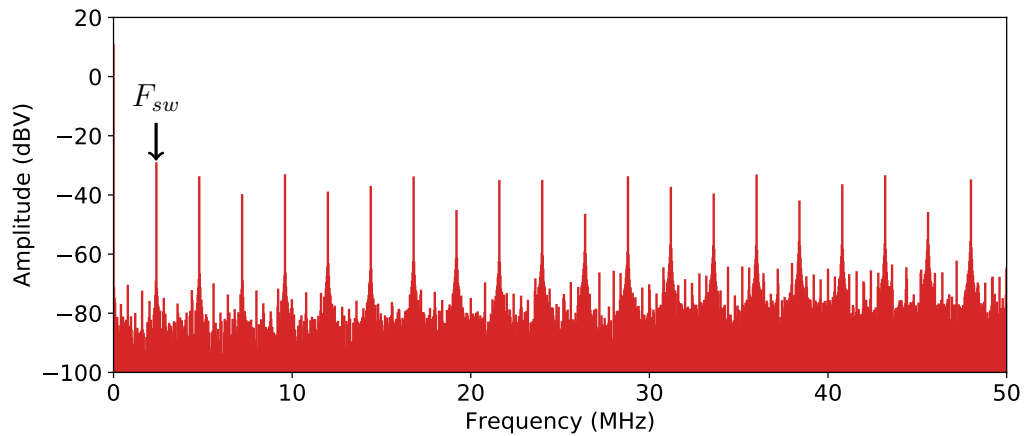


Figure 1.9 – Example of frequency spectrum of simulated buck converter supply voltage

	[25]	[26]	[3]
Peak reduction	$-30.6dB$	$-35dB$	$-32dB$
Noise floor increase	$7dB$	$20dB$	$6dB$

Table 1.3 – Noise reduction technique comparison

switches between two or more frequency to cancel noise resonance. These complex solutions are not described here but the performances in terms of noise reduction are compared in Table 1.3.

These three solutions are efficient to reduce the magnitude of switching frequency rays (more than $30dB$ reduction) but spreading the noise energy produces a noise floor rise (more than $6dB$ increase) as presented in the spectrum of solution in [3] in Figure 1.10.

The performances of IPs sensitive to maximum spurious amplitude may be improved by these techniques but performances of IPs sensitive to noise floor level may be degraded. In practice to reduce the noise emitted from switching (decrease overshoot amplitude and ringing duration), the lever is to reduce the gate driver speed what has the counterpart to increase switching losses. Dealing with noise amplitude inside a micro-controller seems to be a trade-off with efficiency. A clear understanding of noise mechanisms is needed to size the system wisely.

In conclusion, there are two differentiators in micro-controller market: power efficiency and analog performances so introducing SMPS is adapted to respond to the first but is in contradiction with the second. In consequence, it is essential to manage this noise to permit a safe operation of the sensitive IPs inside the micro-controller. To achieve this, three questions have to be answered: How much noise is propagated to the victims? What are the levers to manage the noise? What noise level is admissible on the victims? As in all engineering approach, one must acquire knowledge before thinking of actions. Particularly EMC is sensitive to intruding probes, so most of the knowledge must be built on virtual prototyping, what means models. Models should be validated to

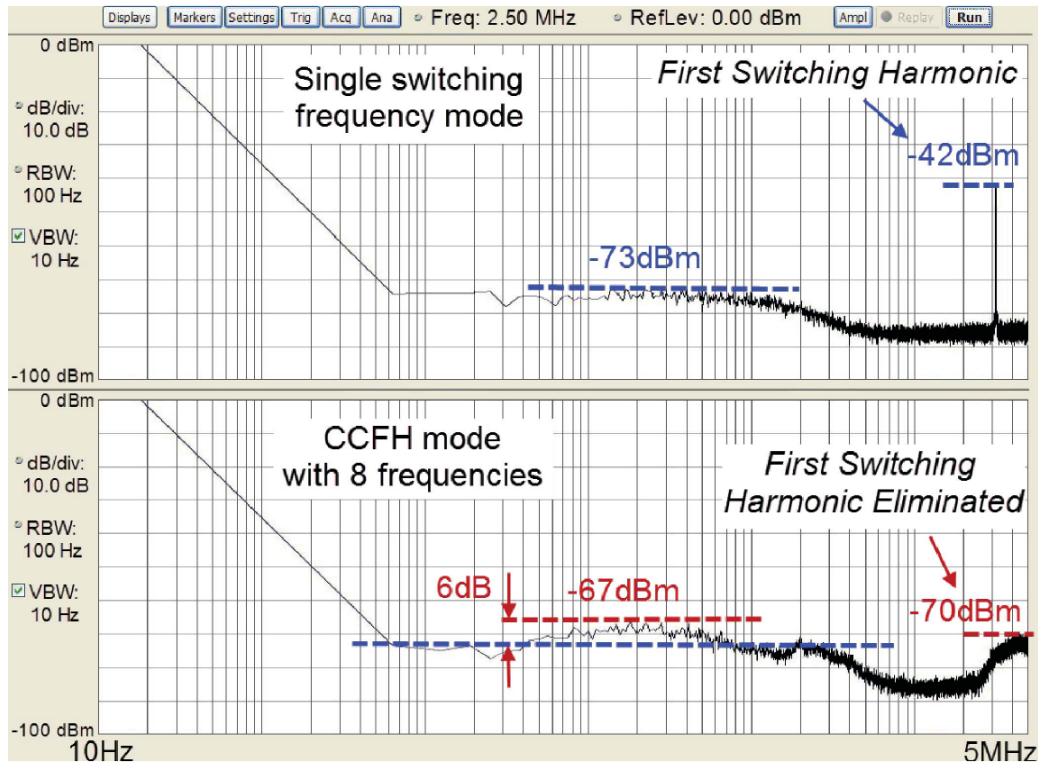


Figure 1.10 – Spectrum with frequency hopping solution [3]

some extent as well.

The susceptibility of the victims is highly dependent of the type and the architecture of the victim. Giving a general answer is not possible and the best person to give the answer about what is admissible must be the IP designer himself. But the noise shape and its propagation to the victim have to be determined to permit him to evaluate the impact on the performances of his IP.



It is the objective of this thesis:

To analyze the pollution mechanisms of the buck converter on sensitive analog IPs integrated in a SoC and to develop minimization techniques of the buck converter noise.

The second chapter presents the methodology used to analyze the noise to achieve this goal, then the buck converter architecture, the environment: the package and the PCB models is detailed. Finally the ADC measurement results show the impact of the buck converter on a sensitive IP and the measurement setups of the noise at source and victim pins are described.

The third chapter explains noise signature and details models of emission due to each transitions of the power stage of the buck converter depending on system parameters. Then propagation model of noise inside the chip and its environment is presented with an analysis of the main propagation path at different frequency values. Each model is validated by comparison with

1.3. What is noisy in a buck converter?

simulation and measurement results.

The fourth chapter presents solutions to reduce noise amplitude by modifying the power stage architecture to change the transition behavior. It also presents a solution to increase the propagation path impedance by top level routing modifications.

A final chapter gives conclusion and draws perspectives.

2 Environment and measurement setup

The noise generation and propagation throughout the chip is analyzed with respect to a vehicle circuit. A DC/DC, a bandgap voltage source operating as a voltage reference and an Analog-to-Digital Converter (ADC) are integrated inside a chip using a 40nm flash technology by STMicroelectronics. The environment and the measurement setup are described in the following sections.

2.1 Hardware environment

The vehicle circuit in Figure 2.6 is detailed in terms of IP blocks and interconnection parasitic components prior to measurement.

2.1.1 The DC/DC converter

The integrated DC/DC is an inductive buck converter with an input voltage range of $[1.6V, 3.6V]$. The output voltage is regulated to $V_{ref} = 1.2V$. The current load on the output is in the range $[0A, 0.6A]$.

The implemented architecture is based on a voltage control loop at fixed frequency, $F_{clk} = 2.4MHz$. The high-side and low-side switches are a PMOS and a NMOS respectively. The study is focused on the Continuous Conduction Mode (CCM), the high power mode where the output current can reach its maximum value of $0.6A$. Other operating modes are implemented but the hard switching of the power stage exists in each of them so the main part of this work can hopefully be transposed to other modes. The implemented architecture is presented in Figure 2.1.

The time waveforms in the voltage control loop in CCM are represented in Figure 2.2. These waveforms are extracted from Spice simulation of the system.

The output voltage, V_{out} , is compared to the reference, V_{ref} . The difference is integrated (ε) and compared to a saw-tooth signal at the switching frequency, to convert the error (ε) into a duty cycle (α). If the output voltage V_{out} drops, the error (ε) increases to enlarge the PMOS conduction duration, rising the inductor current I_{lx} and vice versa. A dead-time between PMOS and NMOS gate drivers is added to avoid cross-conduction.

The decoupling capacitor value at the input is $C_{dec} = 4.4\mu F$ and the output filter component values are $L_{out} = 2.2\mu H$ and $C_{out} = 4.4\mu F$.

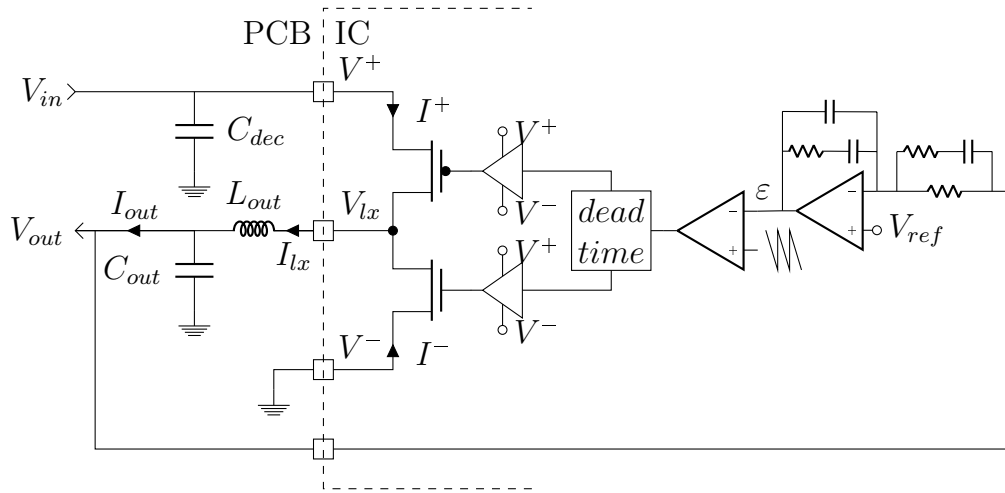


Figure 2.1 – Buck converter architecture

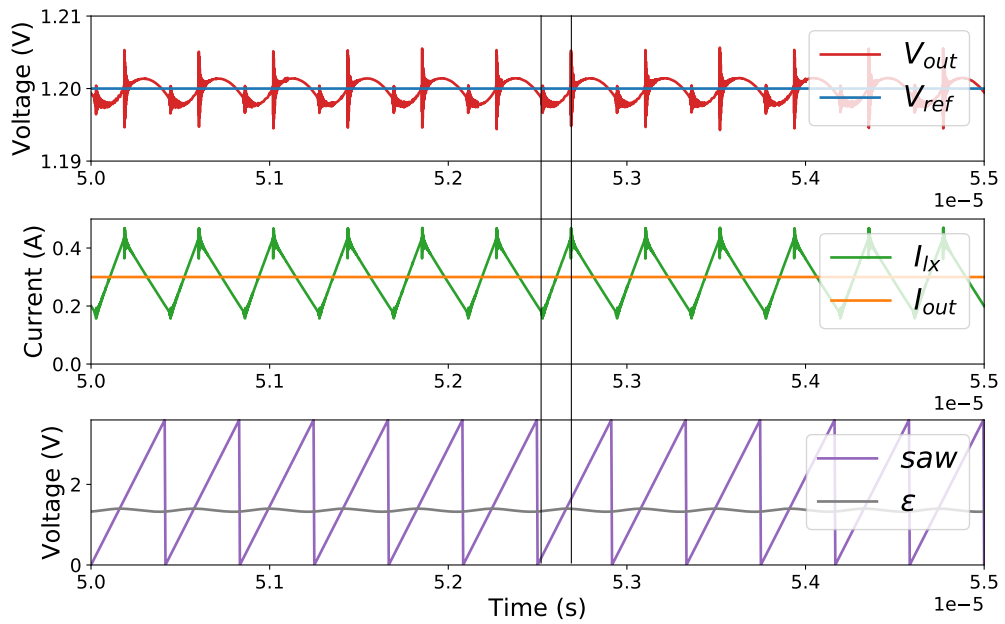


Figure 2.2 – Main simulated waveforms in the circuit in Figure 2.1

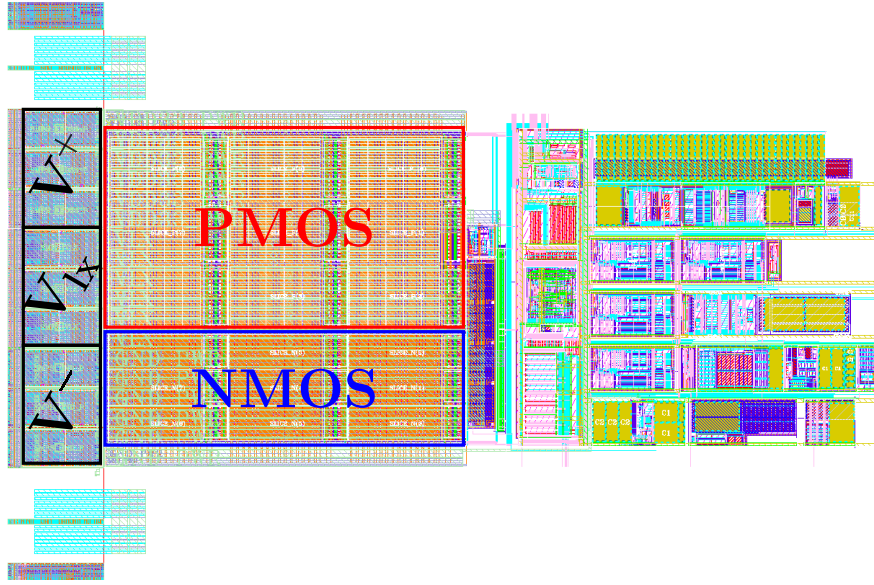


Figure 2.3 – Buck converter layout

To secure the regulation in the worst case ($V_{in} = 1.6V$ and $I_{out} = 0.6A$) and for efficiency requirement, the R_{on} of the power MOSFETs is set approximately to $50m\Omega$. Power MOSFETs' widths are large to obtain the latter value: for PMOS, $W \times L = 8cm \times 0.44\mu m$ and for NMOS, $W \times L = 3cm \times 0.55\mu m$ in CMOS $40nm$ technology. The resulting size of the power stage is $450\mu m \times 450\mu m$. A layout view is presented in Figure 2.3.

Two ranges are considered to analyze the frequency spectrum: SMPS functional bandwidth below $10MHz$ and resonant frequencies above. In the latter range, $Z_{Lout} > 100\Omega$ and $Z_{Cdec} < 5m\Omega$. In consequence, V_{lx} is considered as a high impedance node and V^+ is shorted to the DC input voltage. The original schematic and its equivalent above $10MHz$ are presented in Figure 2.4.

The waveforms of three main currents in the power stage: I^+ , I^- and I_{lx} are given in Figure 2.5a. I_{lx} is a triangular signal with a slope of $\frac{V_{in}-V_{out}}{L}$ and $\frac{-V_{out}}{L}$.

$$\begin{aligned} \Delta I_{lx} &= \alpha T \frac{V_{in} - V_{out}}{L} \\ &= \frac{T}{L} V_{out} \left(1 - \frac{V_{out}}{V_{in}}\right) \end{aligned} \quad (2.1)$$

where $\alpha = \frac{V_{out}}{V_{in}}$ is the duty cycle and T the buck converter switching period.

$$\begin{aligned} I_{lx} &= I^+ + I^- = I_{out} - \frac{1}{2} \Delta I_{lx} \text{ when PMOS is turned-on} \\ I_{lx} &= I^+ + I^- = I_{out} + \frac{1}{2} \Delta I_{lx} \text{ when NMOS is turned-on} \end{aligned} \quad (2.2)$$

In the resonant frequency range (above $10MHz$), V_{lx} node is considered at high impedance. Only the current between power supply pins have to be taken

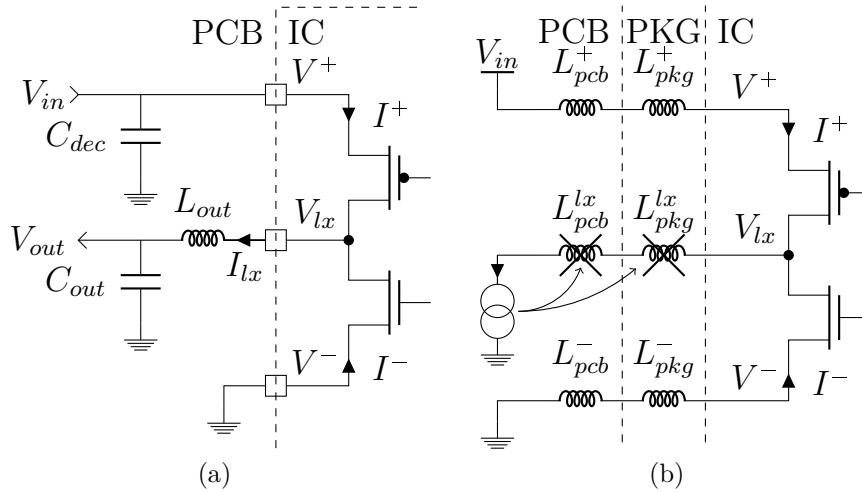


Figure 2.4 – Power stage functional schematic (a) and resonant schematic (b)

into account:

$$\begin{aligned} \frac{dI_{lx}}{dt} &= \frac{dI^+}{dt} + \frac{dI^-}{dt} \approx 0 \\ \frac{dI^+}{dt} &= -\frac{dI^-}{dt} \end{aligned} \quad (2.3)$$

The current I^+ is composed of I_{lx} multiply by a square signal at $F_{clk} = 2.4MHz$ with a duty cycle of $\frac{V_{out}}{V_{in}}$. A ringing signal is superimposed to the functional waveform as presented in Figure 2.5b.

The study is focused on the analysis of the I^+ current especially on the ringing signal: the resonance frequency, the amplitude and finally the spectrum envelop. A precise analysis of the environment of the buck converter is needed to correctly understand the influence of the parasitic impedances. The chip, the package and the PCB are presented in sections 2.1.2 and 2.1.3.

2.1.2 The chip and the package

The circuit is fabricated using the CMOS 40nm technology. The silicon substrate resistivity is $10\Omega.cm$. The chip size is $4mm \times 4mm$.

The circuit was designed and fabricated by STMicroelectronics to test the functionality of IPs which will be integrated in a STM32 product.

The circuit is composed of:

- a Low Drop Out regulator (LDO), the usual DC/DC converter of the micro-controller,
- a buck converter (Buck) with multiple mode to ensure the power integrity and a good efficiency in every working conditions,
- a "Reset-block" (RB), whose functionality is to monitor the start-up and the parameters of a micro-controller (supply voltage level, temperature, etc.),
- a JTAG interface to control the inputs of the tested IPs from outside the chip,

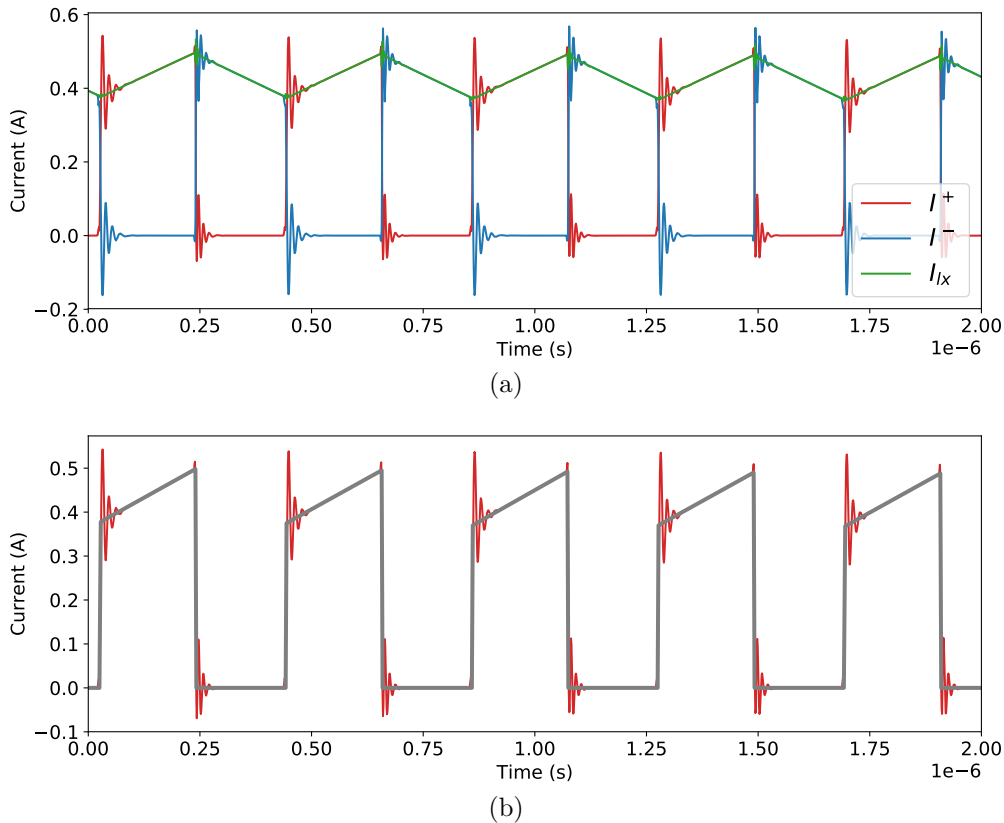


Figure 2.5 – Simulated waveforms of main currents in CCM

- a digital load (DIG) to emulate the consumption of the future microcontroller cortex at the output of the SMPS,
- a 14-bit SAR Analog-to-Digital Converter (ADC) is also integrated in a version of the test vehicle.

The LDO and the digital load are unused and turned-off. The buck converter is only used in CCM as presented in section 2.1.1. Only the voltage reference of the "Reset-block" is monitored as a victim of buck converter noise. ADC measurements require a special setup so they are done with a more complex PCB than the one presented below (section 2.1.3).

A picture of the circuit is presented in Figure 2.6a.

The package is a TQFP100 represented in Figure 2.6b. The three power pins V^+ , V_{Lx} and V^- are highlighted.

The package modeling and the estimation of parasitic impedances are well described in literature for example in [27]. The goal of this section is to apply the latter work to the present case to obtain a formula linking physical dimensions to the parasitic inductances. Finally the theoretical values are compared to the values given by a RLCG netlist of the package parasitic impedances extracted using ANSYS Q3D from the 3D package description. From [27], a simplified formula of the self- and mutual inductance of L_{pkg} in Figure 2.4b is

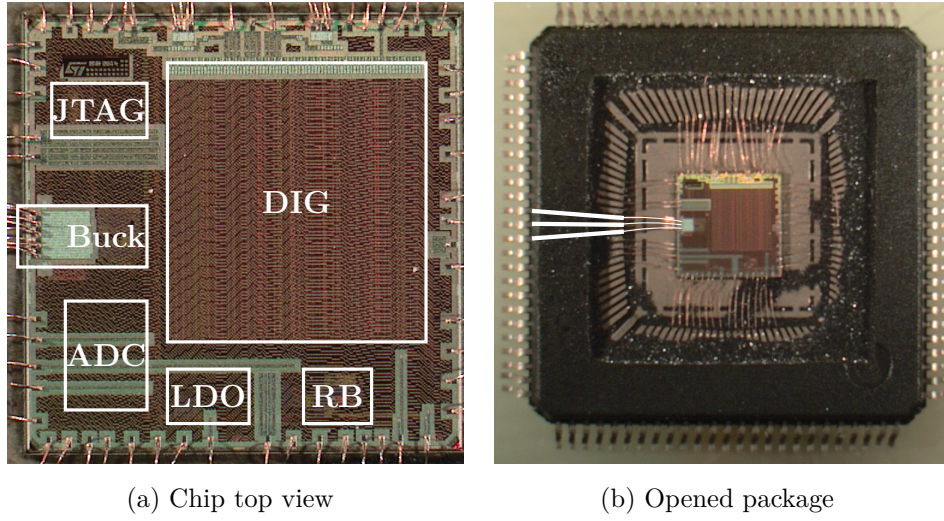


Figure 2.6 – Binocular microscope pictures

presented in (2.4).

$$\begin{aligned}
 L &= \frac{\mu_0 l}{2\pi} \left(\ln\left(\frac{4l}{p}\right) + \frac{1}{2} \right) \\
 M &= \frac{\mu_0 l}{2\pi} \left(\ln\left(\frac{2l}{d}\right) - 1 \right)
 \end{aligned} \tag{2.4}$$

where l is the wire length, p the wire perimeter and d wire spacing.

The latter equation is applied to the parasitic inductances in the power supply path: L_+ and L_- package inductances between respectively V_{in}/V^+ and V^-/gnd (see Figure 2.4b) and the inductive coupling coefficient, M .

$$\begin{aligned}
 \Delta V &= V^+ - V^- \\
 &= \left(V_{in} - L_{pkg}^+ \frac{dI^+}{dt} - M \frac{dI^-}{dt} \right) - \left(0 - L_{pkg}^- \frac{dI^-}{dt} - M \frac{dI^+}{dt} \right) \\
 &= V_{in} - (L_{pkg}^+ + L_{pkg}^- - 2M) \frac{dI^+}{dt}
 \end{aligned} \tag{2.5}$$

L_{pkg} represents the total parasitic inductance along the power loop due to the package (V_{DD} and ground interconnections). Injecting (2.4) in (2.5) and assuming $L_{pkg}^+ \approx L_{pkg}^-$:

$$L_{pkg} = 2L - 2M = \frac{\mu_0 l}{\pi} \ln\left(\frac{1.2d}{p}\right) \tag{2.6}$$

The comparison of RLCG extracted netlist from ANSYS Q3D with expression (2.6), presented in Table 2.1, shows an error of $\sim 10\%$ in total loop estimation. Considering the accuracy of wire length measurement (l , d , p), (2.6) gives an estimation of the main loop inductor. Moreover (2.6) shows a logarithmic dependency on the distance d between lead frame and the wire perimeter p , which has to be taken into account in Input/Output pads placement.

	L_{pkg}^+	L_{pkg}^-	L_{pkg}^{lx}	$K_{pkg}^{+/-}$	$K_{pkg}^{+/lx}$	L_{pkg}
Extracted	4.53nH	4.51nH	4.48nH	0.42	0.59	5.21nH
Calculated	4.57nH	4.57nH	4.57nH	0.37	0.52	5.74nH
Error	0.88%	1.32%	1.99%	-12.7%	-12.6%	9.68%

with $M_{1/2} = K_{1/2}\sqrt{L_1L_2}$

Table 2.1 – Calculated and extracted values of the parameters of the model of parasitic inductances in Figure 2.4b

Another parasitic impedance to take into account is the package resistance. The theoretical formula is $R = \frac{\rho l}{s}$ with ρ the resistivity, l the length and s the section area. The extracted value from the RLCG model is $R_{pkg} = 61.3m\Omega$ per package pin.

2.1.3 The PCB

The PCB for micro-controller application is designed by customers so it is difficult to add constraints especially if they are expensive. A test vehicle PCB is a dual-side substrate with tracks in copper, $35\mu m$ thick and a FR4 substrate with a thickness of $1.5mm$ (standard inexpensive PCB).

Some advices about external component placement are available as explained in [28]. The main constraint is the surface of the current loop. To reduce it, decoupling capacitors have to be implemented as close as possible to power pins with vias directly under capacitor pads. The layout for the buck converter external components is presented in Figure 2.7. The loop between the supply voltage pin and the ground pin of the chip is represented in red for the top layer and blue for the ground plane.

The PCB has to be modeled precisely to understand noise generation and propagation throughout the system. Parasitic impedances of external components and PCB have to be extracted.

There are shunt resistors R_{shunt} of 0.1Ω on power supply path and on output path to monitor I^+ and I_{lx} respectively. As the studied bandwidth is $1GHz$, the shunt could not be considered as only resistive. The resistor is characterized with a Vector Network Analyzer (VNA) to extract its parasitic impedance.

As the resistor value is small compared to characteristic impedance of the VNA input ($0.1\Omega \ll 50\Omega$), the shunt is connected in parallel at input to optimize the accuracy of the measurement ($0.1\Omega // 50\Omega \approx 0.1\Omega$). The methodology is described in [29]. This work explains the necessity to measure impedance using S_{21} parameter to decrease the measurement error. The formula to calculate impedance Z_{shunt} from S_{21} parameter is given by (2.7).

$$Z_{shunt} = \frac{Z_0 S_{21}}{2(1 - S_{21})} \quad (2.7)$$

where $Z_0 = 50\Omega$ is the characteristic impedance.

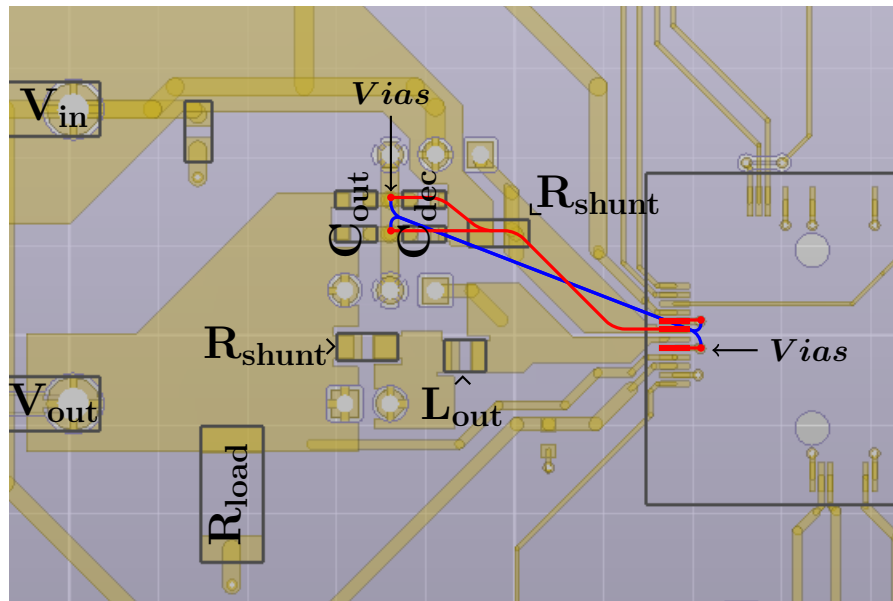


Figure 2.7 – PCB layout for buck converter external components using a TQFP package

The shunt is soldered on a dedicated PCB. The bench is presented in Figure 2.8. A similar PCB provides a short, open, thru and 50Ω configuration (SMD $50\Omega \pm 1\%$ on $0 - 1GHz$ bandwidth) to de-embed the PCB impedance from the measurement. The resulting waveform is presented in Figure 2.9.

At low frequency, the real part of the impedance is $105m\Omega$. Above $40MHz$, the real part increases due to the skin effect ($1.35 \times 10^{-17} f^2$). The imaginary part increases proportionally to frequency due to a parasitic inductance of $2.55nH$. The total impedance is expressed as (2.8).

$$Z_{shunt}(\Omega) = 0.105 + 3.42 \times 10^{-19} \omega^2 + j2.55 \times 10^{-9} \omega \quad (2.8)$$

Other external components are provided by Murata Manufacturing Co., Ltd.. Component references are LQM2MPN2R2NG0L for L_{out} and CAP SMD 0603 X7S 2200000PF 6.3V 20% for C_{dec} and C_{out} (double devices to achieve the $4.4\mu F$). The company provides accurate models of parasitic impedances permitting to model the capacitor by a RLC in series and the inductor by a RLC in parallel.

All these component models are instantiated in a solver to extract S parameters of the PCB. The solver is ANSYS Siwave, based on the Boundary Element Method (BEM) called also the Method-of-Moment (MoM). This algorithm is optimized for stack systems like a PCB or an IC. It has to respect two criteria: plane layers and a substrate surface large compared to its thickness. This method is faster than Finite Element Method (FEM) because electromagnetic equations are solved at boundaries only in contrary to the entire substrate for FEM.

Pins are placed on:

- the buck converter Inputs/Outputs (IOs): V_{ddP} , gnd_P and V_{lx}

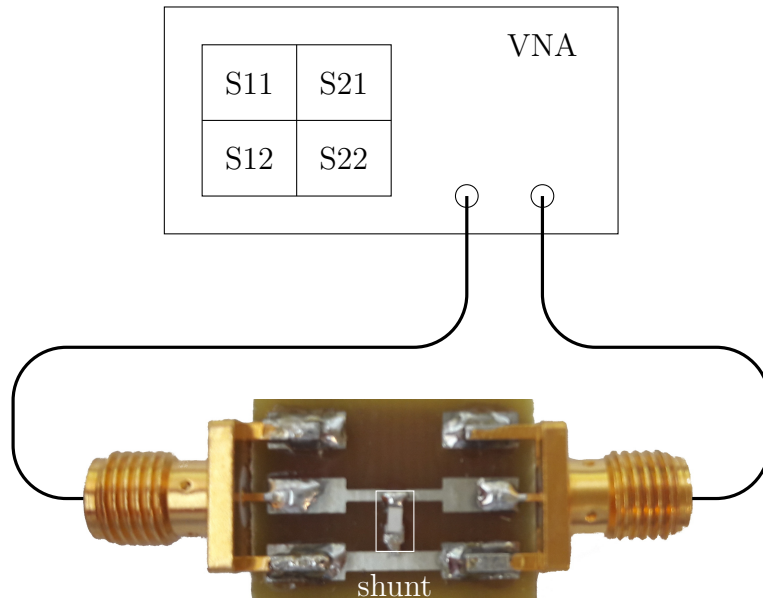


Figure 2.8 – Measurement bench for the shunt resistor Vishay WSL0805R1000F

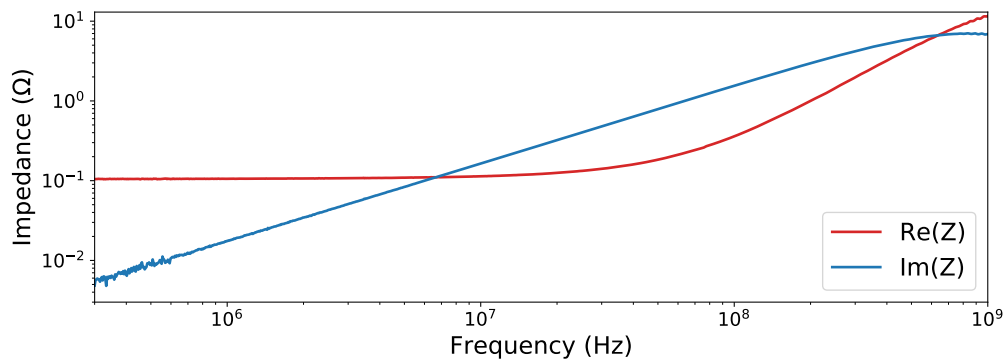


Figure 2.9 – Real and imaginary part of the measured shunt resistor impedance

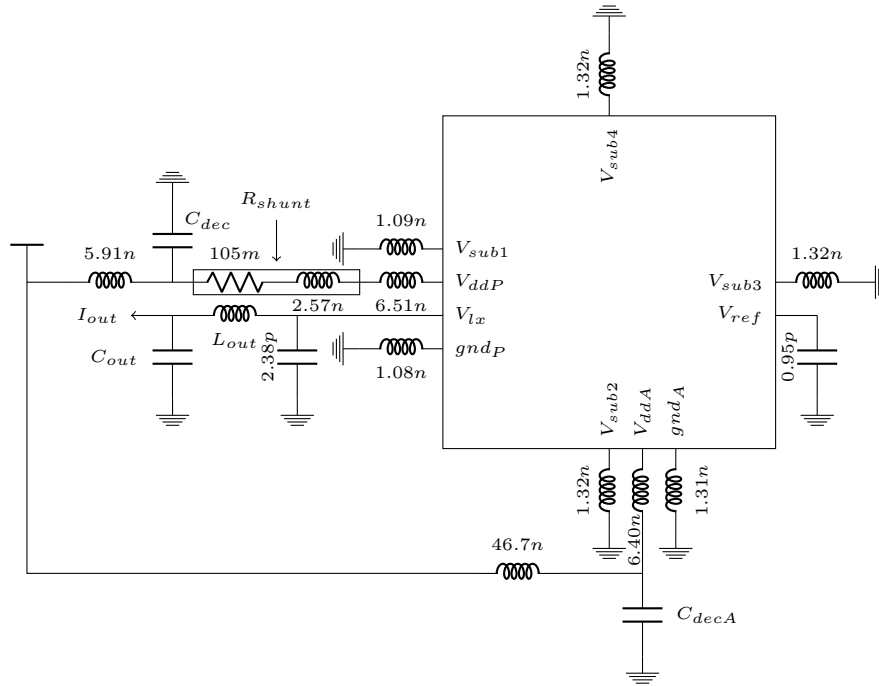


Figure 2.10 – Schematic of the parasitic impedances from the PCB

- the victim I/Os: V_{ddA} , gnd_A and V_{ref}
- the substrate I/Os: V_{sub1} to V_{sub4}
- the V_{ref} probing point: V_{refPCB}



Why include V_{lx} in PCB extraction? It has been proved in section 2.1.1 that V_{lx} can be considered in high impedance due to the large value of the output inductor. Even though V_{lx} output interconnections do not contribute to noise generation, it is important to include V_{lx} for propagation issue. The fast variations of the output node of the power stage pollute the ground plane through the parasitic capacitance.

There are two main recommendations about port reference placement. The current going into the pin, goes out from the reference. Consequently the port reference has to be placed on current return path to stimulate the same impedance as in the physical circuit. The port size (distance between pin and reference) has to be small compared to wavelength, λ . For the analyzed bandwidth (0 to 1GHz), $\lambda = 30cm$.

In the power stage, above 10MHz, the current is flowing between V^+ and V^- as presented in section 2.1.1. There is also some parasitic current in substrate pins that will be presented in chapter 3. The current paths between those pins are represented in Figure 2.7. In consequence, the port references are located in the ground plane under pins to respect the recommendations.

Parasitic impedances of the PCB are extracted from S-parameter model for simulation purpose as presented in Figure 2.10.

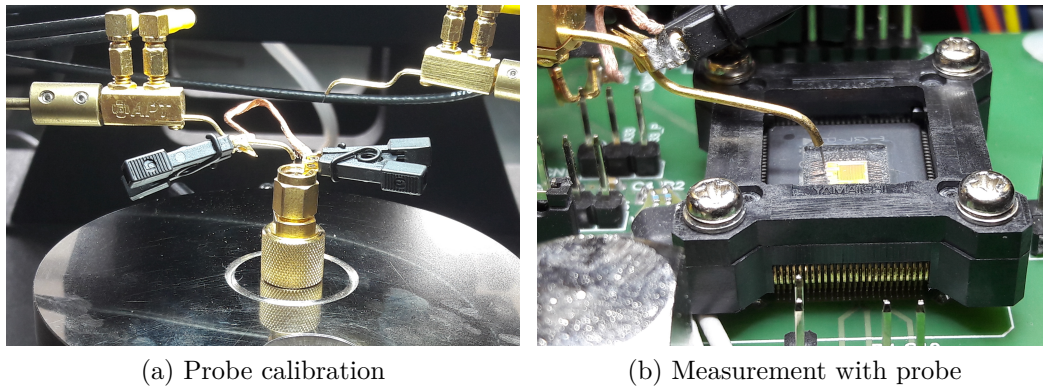


Figure 2.11 – VNA measurement setup

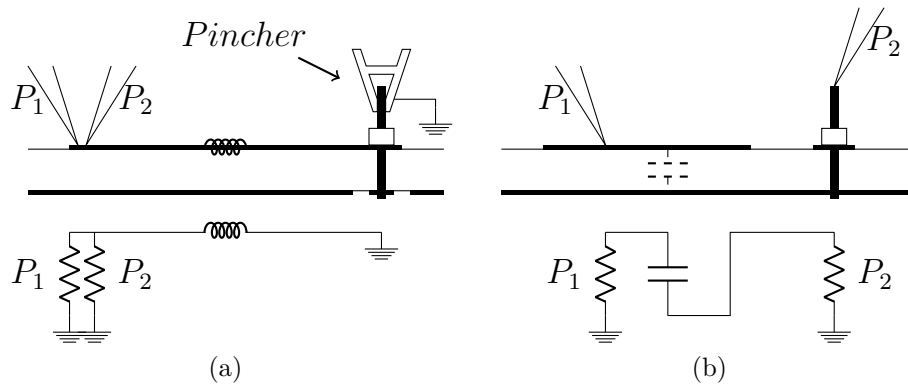
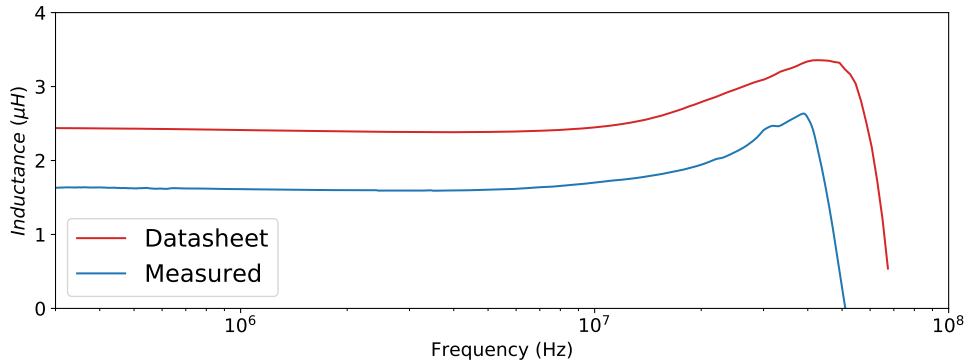
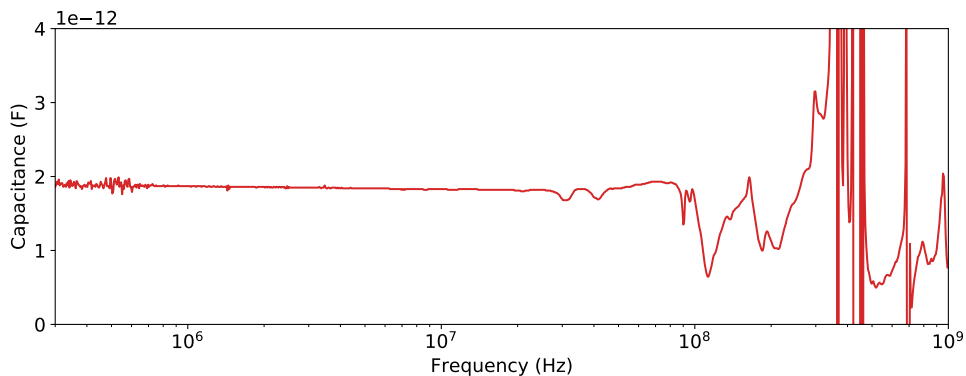


Figure 2.12 – Probe position for the evaluation of parasitic inductance (a) and parasitic capacitor (b)

Measurements are performed using micro-probe connected to a Vector Network Analyzer (VNA) to verify parasitic impedance values: $300kHz - 1GHz$ bandwidth with the VNA Keysight N5232A 300kHz-20GHz. Interconnection impedances are de-embedded using a calibration set. The probe is put down on the core of the 50Ω load, open or short configuration. Two clips are soldered at the wire extremities to connect the ground. The setup is presented in Figure 2.11a. The *thru* configuration is achieved by putting down the two probes as close as possible on a PCB copper track and by connecting the reference of the two probes.

Large impedances in comparison to $Z_0 = 50\Omega$ have to be in series with port impedance and small impedance in parallel as explained in [29]. The calibration is better at low frequency (under $100MHz$). In this bandwidth, capacitor impedances are large and inductance ones are small. In consequence, depending on expected parasitic impedance, the probes have to be placed as presented in Figure 2.12.

The setup, the calibration and the calculation are tested on genuine impedances as L_{out} . The comparison between manufacturer and experimental inductances are presented in Figure 2.13. There is an offset in DC inductance value: $1.6\mu H$

Figure 2.13 – Frequency response of the inductance L_{out} Figure 2.14 – Experimental parasitic capacitor between V_{ref} and ground plane

measured for a $2.2\mu H$ inductor but this variation is in the range given by Murata ($\pm 30\%$). The inductance profile is respected (same cut-off frequency).

Another verification is to measure the reflection parameter S_{11} , probes up. An error in calibration of the probe appears: a capacitor of $0.7pF$ remains after calibration. This capacitor is in parallel with the 50Ω port resistance. However the port impedance is not modified below $100MHz$ (less than 2% error).

The S parameters are measured at the output of the voltage reference pin. The parasitic capacitor is calculated from S parameter waveforms to obtain the results presented in Figure 2.14. In the range $[300kHz, 70MHz]$, the parasitic capacitor is estimated to $1.8pF$. It can be noticed that the waveform is noisy above the range $70MHz$. Above $200MHz$ the waveform deviates: this is not due to noisy measurement but to non-capacitive behavior of the parasitic impedance.

Main parasitic impedances of the circuit are presented in Table 2.2. C_{lx} measurement is inaccurate because at low frequency the impedances are dominated by L_{out} impedance. The capacitive behavior appears at higher frequency ($60MHz$) but is noisy. A version of the PCB with chip socket is used to permit measurement without chip impedance but the two inductance values contain the socket parasitic inductance. Even if all the measurements and the model do not fit accurately for every parasitic impedance, the order of magnitude is respected. The models presented in the chapter 3 are based on values extracted from S parameter model here.

	L_{out}	C_{ref}	C_{lx}	L_{pcb}^-	L_{pcb}^+
Extracted	$2.2\mu H$	$0.95pF$	$2.38pF$	$1.09nH$	$9.08nH$
Measured	$1.6\mu H$	$1.8pF$	$6pF$	$10nH^*$	$15nH^*$

Table 2.2 – Extracted and measured values of main parasitic components



The accuracy of these measurements may be improved with measurements without any external component, especially for C_{lx} without L_{out} and for the parasitic inductances without socket.



Finally the total inductance of the buck converter supply loop is

$$L_{tot} = L_{pcb} + L_{pkg} = 9.08n + 1.09n + 5.21n = 15.38nH \quad (2.11)$$

And the total resistance of the package and PCB path up to the decoupling capacitor is

$$R_{ext} = R_{shunt} + 2 \times R_{bonding} = 105m + 2 \times 61.3m = 228m\Omega \quad (2.12)$$

The hardware environment has been described. It is time to take a look at buck converter noise measurement setups which will permit to validate models presented in chapter 3.

2.2 Measurement setup

The setup is presented for three different measurements: the preliminary measurements on ADC whose performance degradations motivated this work; measurements on the buck converter to confirm noise source models; measurements on a reference voltage output to evaluate noise propagation.

2.2.1 Analog-to-Digital Converter (ADC)

The preliminary analysis is realized on the version of the test-vehicle with an ADC. The architecture of the ADC is Successive Approximation Register (SAR) with a resolution of 14 bits. The ADC is supplied under $3.6V$ and operates at $36MHz$ corresponding to $3.6Msps$ (Mega sample per second). The measurement presented below are performed in single-ended mode.

Figure 2.15 presents the loss of accuracy of the ADC as function of the current load on the buck converter output. The loss of accuracy is represented by the Effective Number Of Bits (ENOB). At $0.6A$ load current the resolution falls by $1.5bits$.

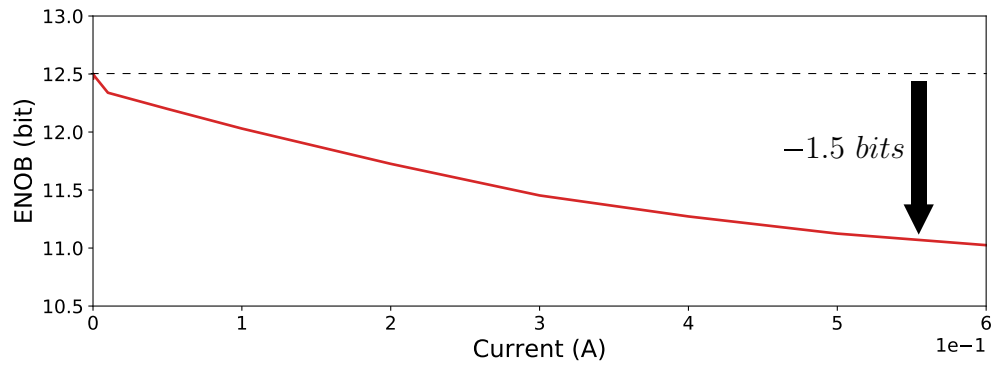


Figure 2.15 – ADC ENOB versus buck converter current load

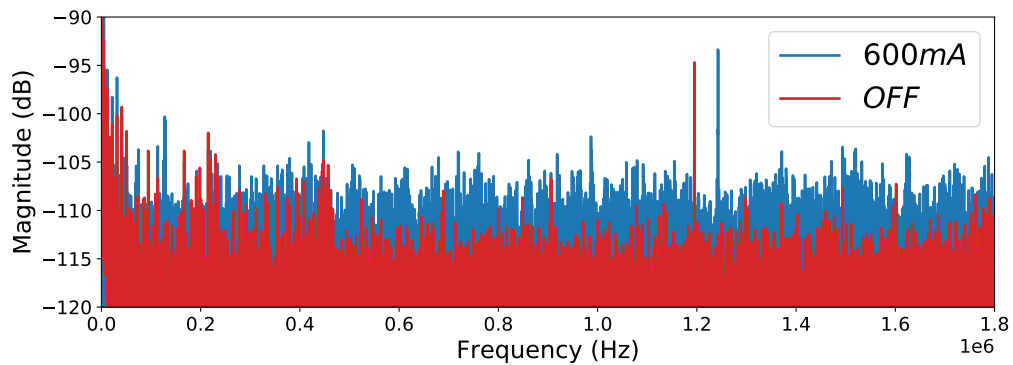


Figure 2.16 – Fast Fourier Transform of ADC output

The spectrum of the ADC output is plotted in Figure 2.16 with the buck converter turned off compared to $600mA$ load current. The noise floor is increased by $5dB$ but there is no resonant frequency. The noise is approximately white. The mechanism of the buck converter noise generation and propagation is masked by the aliasing due to ADC sampling.

Analysis of noise signature of the buck converter and its impact on the system requires to separate source, propagation and victim perturbations. For the source part, major noise contribution is included in I^+ signal (or I^-) as previously explained in package presentation (see 2.3). Consequently monitoring this current gives an image of noise generation.

The study of the noise propagation includes PCB, package and substrate crosstalk. A software tool, CWS *WaveIntegrity* presented in section 3.6, is used to discriminate each path. A victim cell is used as a probe. Measurements on victim pins are used to fit simulations and measurements. A static cell is selected to make the interpretation and the calculation easier and more accurate (no non-linear transfer functions). Consequently in the rest of the work, the victim is a voltage reference, constituted by a bandgap whose output voltage is buffered. This structure is static (DC function) consequently the perturbation on the output can be calculated using small-signal AC response around the operating point.

The study of the susceptibility to switching noise of the buck converter is not part of the present work. Measurements on ADC are used only as a

quantifier of noise pollution.

2.2.2 Buck converter input current

Two methods can be used to measure I^+ current. First a current probe is implemented. The magnetic field generated by a bond wire is sensed by the probe to have an image of the current. This method is accurate and valid in a large bandwidth (for example Tektronix CT6 probe has $200\mu A$ resolution and $2GHz$ bandwidth). The main cons of this probing approach are the parasitic inductance due to the probe ($3nH$) and the setup. Indeed the PCB has to be modified to add a wire on power net going through the probe. This modification adds a parasitic inductance which is difficult to characterize.

Measurements with a shunt is used to minimize system modification. This method "only" adds a small resistor on the power path. This component has to be small enough to reduce its impact on the system (efficiency and switching speed degradation) but large enough for accurate measurements. The chosen value is 0.1Ω with 1% tolerance (Vishay WSL0805R1000F).

Voltage across the shunt resistor is monitored by differential probe 1134A connected to the oscilloscope DSO-S 104A $1GHz$ from Keysight with sample rate of $20Gs/sec$. Then the current is calculated using the non-ideal impedance detailed in section 2.1.3. The results are presented in section 3.2.

2.2.3 Propagation paths

It is difficult to separate propagation paths especially the substrate crosstalk. So two kinds of measurements are performed to verify the model. The output of the voltage reference is sensed directly using an oscilloscope DSO-S 104A $1GHz$ with an active probe N2795A $1GHz$ to validate global perturbations. Then the paths between the buck converter and the voltage reference are measured with the VNA to consolidate results obtained by simulation. The setup of these measurements is the same as the ones presented in 2.1.3.

A first overview of the noise spectrum on the voltage reference is presented in Figure 2.17. There are three parts. The objective of the next chapter is to understand the generation and the propagation path for each part of this noise spectrum.

Measurement setup have been presented to verify source model by I^+ monitoring, propagation paths impedance by voltage reference measurements and VNA PCB characterization. In the next chapter, model construction will be detailed and compared to the experimental results.

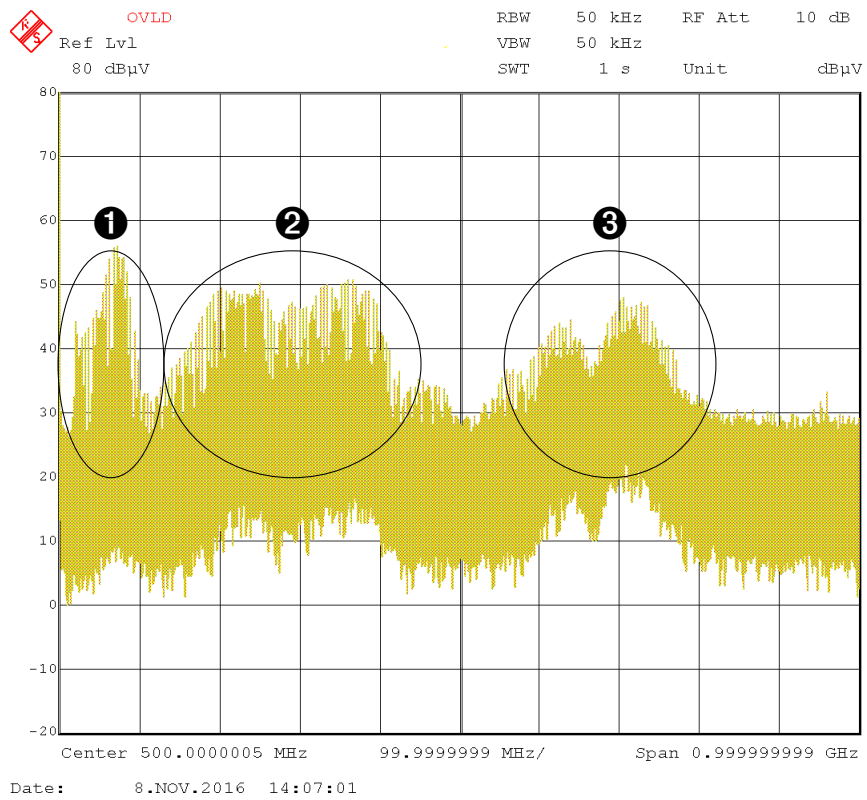


Figure 2.17 – Noise spectrum on the voltage reference

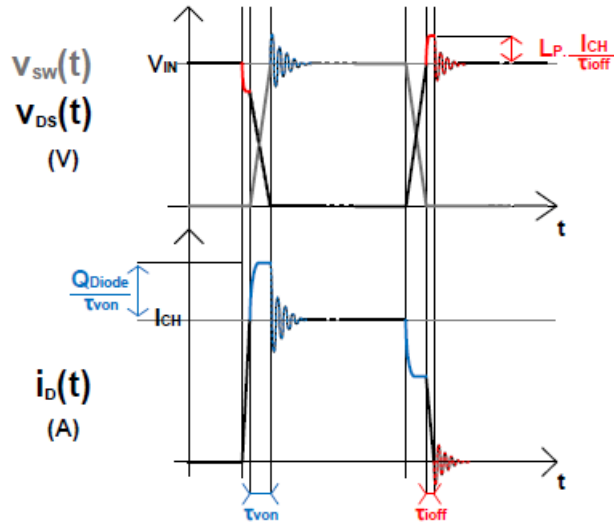


Figure 3.2 – Transition waveforms of the buck converter in [4]

These transitions stimulate the parasitic network which resonates at

$$f_r = \frac{\sqrt{1 - \zeta^2}}{2\pi\sqrt{LC}} \approx \frac{1}{2\pi\sqrt{LC}} \text{ with } \zeta = \frac{1}{2}R\sqrt{\frac{C}{L}} \quad (3.1)$$

Based on this analysis, the equations of power stage ringing are calculated. The spectrum envelope is obtained by a FFT on the time signal.

$$\begin{aligned} H_{on}(f) &= \frac{Q_{Diode}}{\tau_{von}} \frac{2F_{clk}\sqrt{L_P C_{Diode}}\sqrt{1 - \zeta^2}}{\sqrt{4\pi^2 R_{Pon}^2 C_{Diode}^2 f^2 + (1 - 4\pi^2 L_P C_{Diode} f^2)^2}} \\ H_{off}(f) &= \frac{I_{CH}}{\tau_{ioff}} \frac{2F_{clk} L_P C_{DS}}{\sqrt{4\pi^2 R_{Poff}^2 C_{DS}^2 f^2 + (1 - 4\pi^2 L_P C_{DS} f^2)^2}} \end{aligned} \quad (3.2)$$

where τ_{von} is the rising time of V_{SW} and τ_{ioff} the falling time of I_D .

The frequency response of a trapezoidal signal is added to the noise contribution [33] to obtain the full spectrum response.

This buck converter topology used commercial components (NMOS smartmos8mv from Freescale and diode MBR540T3G) so parameters of the MOSFET could not be freely adjusted. In consequence the study does not detailed R, L and C equations. Moreover some formula give an expression for each parameter but in practice these parameters are extracted from spice simulation and measurements.

In the studied case, the topology is different: one supply for drivers and the power stage is constituted of PMOS and NMOS switches. Consequently the transient phenomena are different and so the noise amplitude at the resonant frequency. Moreover a detail about RLC component is needed to understand how to deal with physical parameters of the power MOSFET to be compatible with buck converter noise emission requirements.

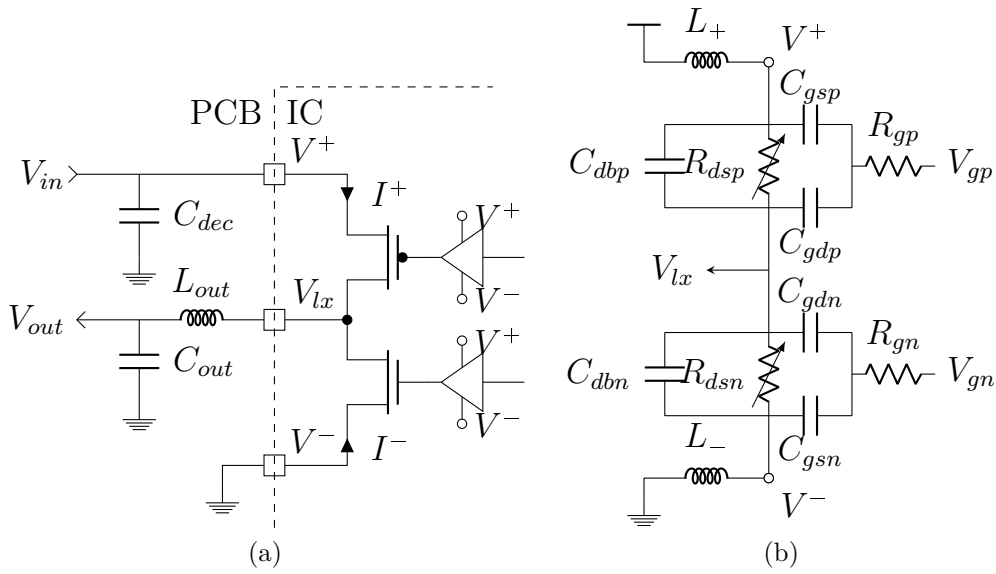


Figure 3.3 – Power stage structure (a) and its equivalent schematic (b)

The power stage considered here is presented in Figure 3.3a. It can be in three different states: conduction of PMOS, P_{ON} state; conduction of NMOS, N_{ON} state; non-overlapping phase, OFF state. A specific resonant frequency corresponds to each state and the transitions between those states stimulate the parasitic network.



The objective of noise understanding in terms of frequency and amplitude is achieved by simplification of the parasitic network as a simple RLC. The R, L, C and the initial conditions are defined by parasitic components' combination to reproduce the stimulation of the network during the transitions.

The time response of the RLC network is a solution of (3.3),

$$\frac{d^2 I}{dt^2} + \frac{R}{L} \frac{dI}{dt} + \frac{1}{LC} I = 0 \quad (3.3)$$

The general solution to (3.3) is,

$$I(t) = (A \cos(\omega_r t) + B \sin(\omega_r t)) e^{-\lambda t} \quad (3.4)$$

with $\omega_r = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$ and $\lambda = \frac{R}{2L}$

In the following subsections, the parasitic impedances of the system in each state are analyzed to determine R, L, C and then the stimulations during each transition between those states to determine A, B expressions for each transition.

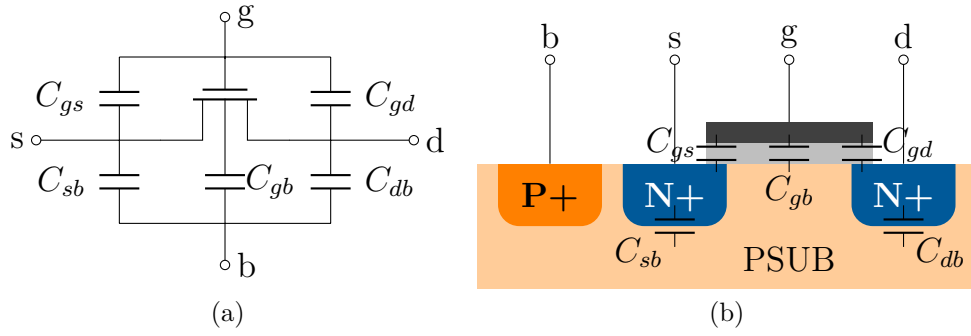


Figure 3.4 – Parasitic capacitances of a MOSFET: (a) schematic and (b) cross-section

3.1.1 Network of parasitic components

Each state is studied separately to determine the parasitic network. The analysis of these states requires modeling of the MOSFET parasitic components. When the MOSFET is on, it works in deep triode region, $V_{ds} \ll V_{gs} - V_{th}$ with V_{th} threshold voltage. In this case, $V_{ds} \sim mV$ whereas $V_{gs} - V_{th} \in [1V, 3V]$ depending on input voltage V_{in} . So the channel resistance is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \quad (3.5)$$

Where μ_n is the electron mobility, C_{ox} the gate oxide capacitance per unit area, W the width and L the length of the channel [34]. The hole mobility of PMOS is less than half the electron mobility in NMOS ($\mu_n \approx 2.5\mu_p$). So the PMOS width W_p is increased to achieve a similar R_{on} : $W_p = 81mm$ and $W_n = 33mm$. Extracted from spice simulation, the channel resistances are, $R_{onn} \in [59m\Omega, 98m\Omega]$ for NMOS and $R_{onp} \in [57m\Omega, 122m\Omega]$ for PMOS.

MOSFET parasitic capacitances are represented in Figure 3.4.

The gate-source C_{gs} and the gate-drain C_{gd} are due to overlaps of the gate on respectively source and drain wells. Moreover gate to channel capacitance is added when MOSFET is on. In off region, $C_{gs,d} = WC_{ov}$ and in triode region, $C_{gs,d} = WC_{ov} + WLC_{ox}$. The gate-bulk C_{gb} capacitance decreases when the MOSFET is turned on due to channel capacitance added in series with oxide capacitance (/ in Table 3.1). Finally drain-bulk C_{db} and source-bulk C_{sb} are due to junction capacitance [34, p. 30]. All these components are directly proportional to physical dimensions so the PMOS capacitances are bigger than NMOS ones due to a larger width.

Capacitances' values are presented in Table 3.1. In the power stage configuration, source and bulk are connected to V^+ or to V^- for PMOS and NMOS respectively so C_{sb} is shorted and C_{gs} , C_{gb} are in parallel so only four capacitances are taken into account: C_{db} , C_{gd} , C_{gs} and C_{gb} . Moreover when the MOSFET is on, source and drain are shorted and so is C_{db} (X in Table 3.1).

		$C_{gs}(pF)$	$C_{gd}(pF)$	$C_{gb}(pF)$	$C_{db}(pF)$	$R_g(\Omega)$
PMOS	$V_{sg} = V_{in}$	100.2 – 102.9	100.2 – 102.9	/	X	6.09 – 3.32
	$V_{sg} = 0$	41.9	<u>25.9 –</u> <u>21.9</u>	34.9	15.3	5.56 – 2.43
NMOS	$V_{gs} = V_{in}$	50.7 – 52.0	50.7 – 52.0	/	X	15.7 – 6.89
	$V_{gs} = 0$	14.2	9.1 – 8.1	16.8	6.3	6.03 – 3.28

Table 3.1 – Parasitic components of the power stage

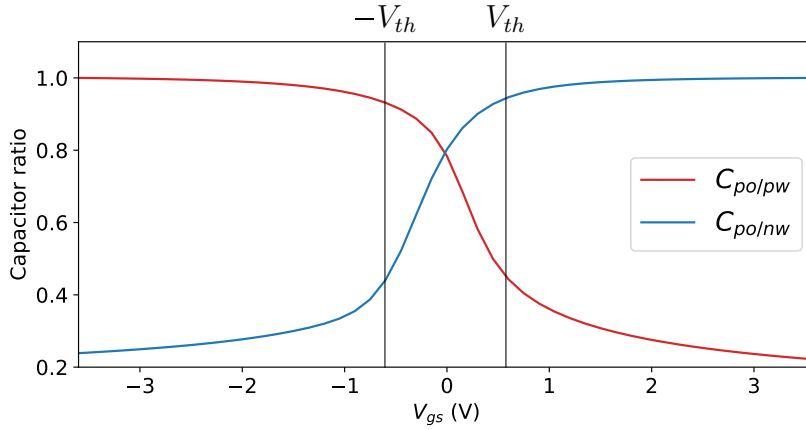


Figure 3.5 – MOSFET capacitor variation due to applied voltage



There is a difference between C_{gd} and C_{gs} in off mode. In N_{on} state, the PMOS drain is connected to V^- so $V_{gd} = V^+ - V^- \approx V_{in}$ whereas $V_{gs} = 0V$. As gate capacitances are CMOS capacitances, their values decrease when the voltage difference increases [35, p. 217] so $C_{gd} < C_{gs}$. Due to this voltage dependency, two values are presented when the applied voltage is V_{in} on a CMOS capacitor: one for 1.6V and the other for 3.6V. The capacitor value variation is presented for a PMOS ($C_{po/pw}$) and a NMOS ($C_{po/nw}$) in Figure 3.5.

Parasitic components will replace the MOSFET in the global power stage equivalent schematic in Figure 3.3b.

The package and the PCB tracks are represented by the equivalent inductances with coupling coefficients according to (2.11) in chapter 2.

Gate driver buffers are represented by their output resistor R_{gp} , R_{gn} connected to V^+ or to V^- respectively: $V_{gp}, V_{gn} \in \{V^+, V^-\}$. Depending on these voltages, the channel resistance of the MOSFET can be a high impedance or R_{on} . Comparing R_{on} values (few $m\Omega$) to R_{gp} , R_{gn} (few Ω , Table 3.1), the ON-state MOSFET channel resistance is neglected. Finally $R_{dsp}, R_{dsn} \in \{0, \infty\}$ (see

3.1. Noise generation - The power stage

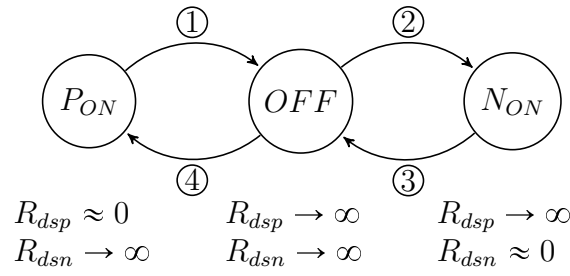


Figure 3.6 – Power stage transitions and drain-to-source resistance

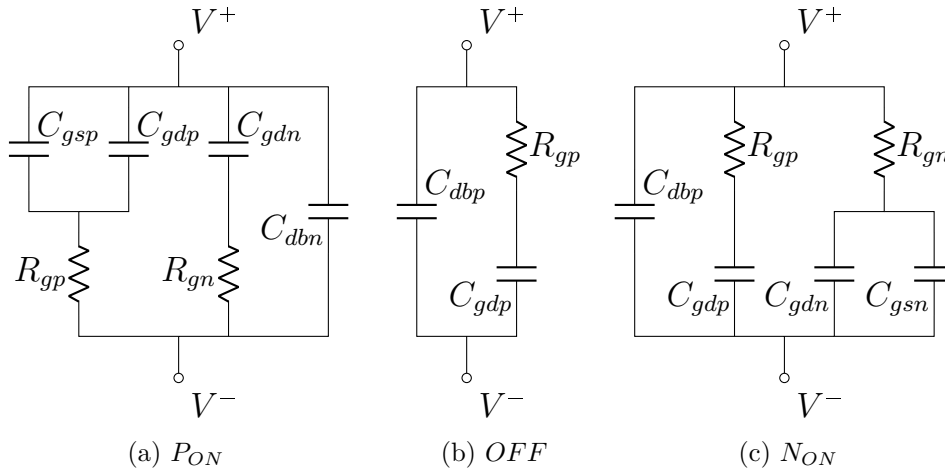


Figure 3.7 – Equivalent networks in P_{ON} (a), OFF (b) and N_{ON} (c)

Figure 3.6).

The RC equivalent schematic in each state is represented in Figure 3.7.

In Table 3.1, parasitic capacitors of the equivalent network are in bold type and color red for P_{on} , blue for N_{on} and underlined for OFF state.

! A capacitor $C_d=18.6\text{pF}$ between V^+ and V^- must be added in parallel to the equivalent network due to the parasitic body diode (junction of NWell and DeepNWell with isolated PWell).

The network is simplified to a simple RLC using the formula demonstrated in annex A to associate parallel RC: $R = \frac{\sum R_n C_n^2}{(\sum C_n)^2}$ and $C = \sum C_n$. An hypothesis is made to use these formula: all resonant frequencies are below 200MHz , to guarantee that all $(RC\omega)^2 < 0.1 \ll 1$. This assumption will be confirmed by numerical applications and measurements.

Parasitic components in P_{on} state:

$$R_{P_{on}} = \frac{R_{gp}(C_{gdp} + C_{gsp})^2 + R_{gn}C_{gdn}^2}{(C_{gdp} + C_{gsp} + C_{gdn} + C_{dbn} + C_d)^2} \quad (3.6)$$

$$C_{P_{on}} = C_{gdp} + C_{gsp} + C_{gdn} + C_{dbn} + C_d$$

Parasitic components in OFF state:

$$R_{off} = \frac{R_{gp}C_{gdp}^2}{(C_{gdp} + C_{dbp} + C_d)^2} \quad (3.7)$$

$$C_{off} = C_{gdp} + C_{dbp} + C_d$$

Parasitic components in N_{on} state:

$$R_{N_{on}} = \frac{R_{gp}C_{gdp}^2 + R_{gn}(C_{gdn} + C_{gsn})^2}{(C_{gdp} + C_{dbp} + C_{gdn} + C_{gsn} + C_d)^2} \quad (3.8)$$

$$C_{N_{on}} = C_{gdp} + C_{dbp} + C_{gdn} + C_{gsn} + C_d$$

In OFF state, only few capacitances are involved in the resonant frequency network. Moreover in the off-mode, MOSFET capacitances are smaller than in on-mode. The parasitic capacitances of the driver buffer chain become significant and must be considered in the calculation procedure. To model the gate buffers' parasitic impedances, two RC networks are added in parallel, R_{bufp} , C_{bufp} and R_{bufn} , C_{bufn} . Finally the RC equivalent network in OFF state can be expressed as,

$$R_{off} = \frac{R_{gp}C_{gdp}^2 + R_{bufp}C_{bufp}^2 + R_{bufn}C_{bufn}^2}{(C_{gdp} + C_{dbp} + C_d + C_{bufp} + C_{bufn})^2} \quad (3.9)$$

$$C_{off} = C_{gdp} + C_{dbp} + C_d + C_{bufp} + C_{bufn}$$

Based on these RLC networks, the next objective is to determine the stimulation, i.e. the initial condition after the switching transition. To achieve this goal, an analysis of each transition is needed.

3.1.2 Transition analysis

The network stimulations are due to the current variations in parasitic inductances. These current variations are created by two phenomena:

1. Charging and discharging of the parasitic capacitances present in the equivalent MOSFET schematic in Figure 3.4,
2. Output current path change from $V_{in} \rightarrow V_{lx}$ to $gnd \rightarrow V_{lx}$ and vice versa.

Transitions are numbered ① to ④ as presented in Figure 3.6.

During every transitions, gate potentials change so the first phenomenon must be evaluated for each transition. The output current path changes only

during PMOS turn-on (transition ④) or turn-off (transition ①) because NMOS and body diode (of the NMOS) are connected to V^- .

i

In $40nm$ technology, the MOSFET threshold is smaller than the diode junction threshold, $V_{th-mos} = 0.55V < 0.85V = V_{th-junction}$. Consequently when the power stage is *OFF*, $V_{lx} = V_d$ activates the NMOS (biased as a diode $V_g = V_s$) before the body junction diode. The current flows through the channel instead of the junction: $V_d + V_{th-junction} > V_g = V_b = V^- > V_d + V_{th-mos}$. For the following explanation, the diode symbol is used and V_{th} corresponds to MOSFET threshold.

Each transition is detailed in the following paragraphs. The charging and discharging paths of the parasitic capacitances are represented in Figure 3.8. The currents from V^+ in red, the currents from V^- in blue and the charge recombination in green. Time waveforms are given in Figure 3.9 where gray areas represent capacitors' charging.

PMOS turning-off ①: The PMOS gate starts charging, reducing R_{on} . Parasitic capacitances of the MOSFET supply the output current instead of the PMOS channel. As these capacitances are mainly connected to V^+ , the current path does not change during the discharge. Then when V_{lx} reaches $-V_{th}$, the current path changes quickly from V^+ (parasitic capacitors) to V^- (NMOS diode). This path change stimulates the parasitic network.

NMOS turning-on ②: The NMOS gate starts charging. Parasitic capacitances inject charge from V^+ to the output, reducing the current in the NMOS channel. Once the capacitors are charged, the current goes again through NMOS channel. This charging current on V^+ stimulates the parasitic network.

NMOS turning-off ③: The switching mechanism is similar to NMOS turning-on but the NMOS parasitic capacitors are shorted. When shorted these capacitors do not generate any current inrush. Finally the only small current inrush is due to V_{lx} increase from $V^- - V_{th}$ to V^- on PMOS capacitors.

PMOS turning-on ④: The PMOS gate is discharged of a threshold voltage V_{th} . As the PMOS is on, the current path changes from NMOS to PMOS channel. After the current through the diode reaches zero, V_{lx} starts rising to V^+ then the PMOS gate is discharged to V^- . Current path change stimulates the network but the current overshoot is hidden by the current demand for parasitic capacitor charging. The overshoot is created by current inrush for capacitor charging.

For each of these transitions, the equivalent circuit response is calculated with initial conditions chosen according to the stimulation phenomenon (discharged capacitances or current step in the parasitic inductance). Example of application for $V_{in} = 3.6V$ and $I_{out} = 0.3A$ is given for each transition. After

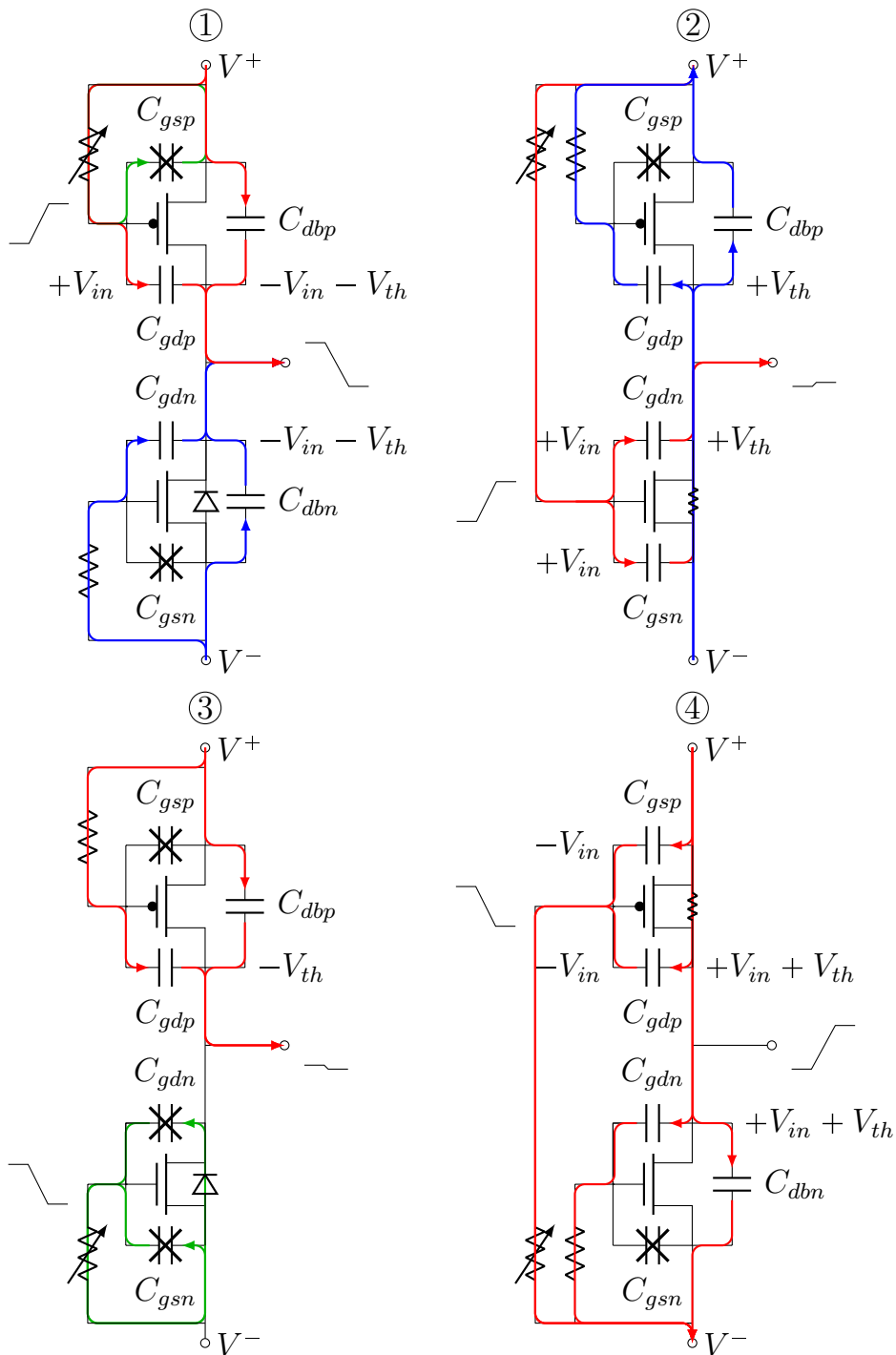


Figure 3.8 – Details of charge injection paths during each transition

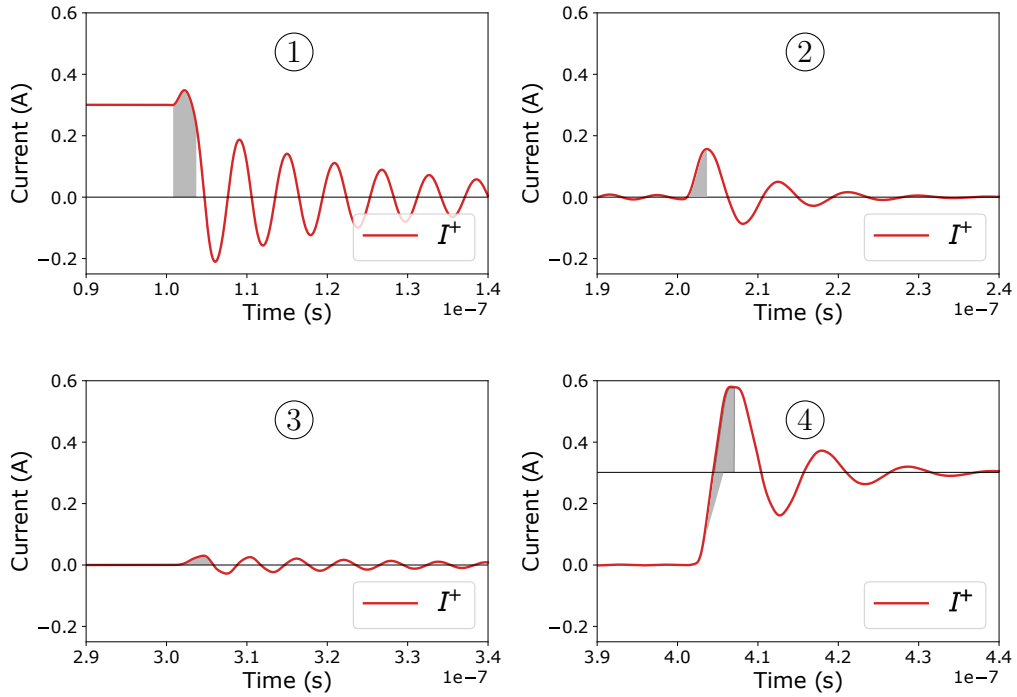


Figure 3.9 – Simulated waveforms of I^+ during transition ①, ②, ③ and ④

the model presentation, the models are compared to experimental results in different operating condition.

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In the equivalent schematic L_+ and L_- are merged for simplification to an inductor L_{tot} calculated in (2.11). The differential voltage across this equivalent inductance is $\Delta V = V^+ - V^-$. Current fluctuations remain identical.

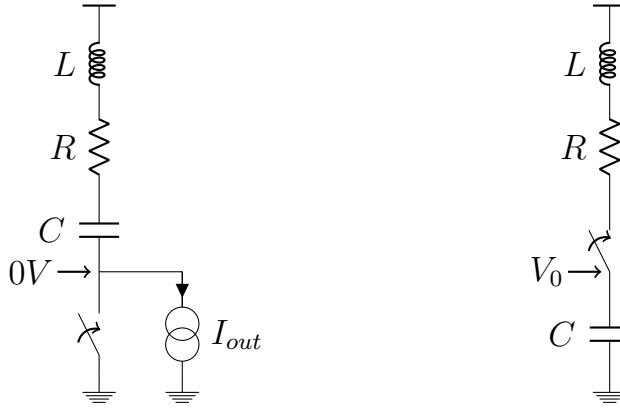
3.1.3 PMOS turning-off ①

During the PMOS turning-off, I_{out} drop in the parasitic inductance of the power paths stimulates the equivalent network of the power stage described in Figure 3.7b.

The turning-off of the PMOS ① can be modeled by a RLC network with a current source as presented in Figure 3.10a. Modeling the diode activation implies an ideal switch closing, shorting the current source. To take into account the threshold voltage of the diode, the supply voltage should be increased to $V_{in} + V_{th}$ but this potential does not need to be involved in the following calculation.

The current function is given by (3.4), where $R = R_{off}$, $C = C_{off}$ (3.9) and $L = L_{tot}$ (2.11). A and B are determined using initial conditions, in this case:

- I is continuous due to inductance continuity constraint so $I(0^+) =$



(a) PMOS turning-off - diode activation (b) NMOS turning-on - gate charging

Figure 3.10 – Equivalent schematics during transitions

$$I(0^-) = I_{out}.$$

- $V_C(0^+) = V_C(0^-)$ due to capacitor continuity constraint. V_R , the voltage across resistance, is proportional to I which is continuous. Consequently, the voltage across RC is continuous. $V_C^-(0^-) = 0V = V_C^-(0^+)$ (diode) so the voltage across the inductance is continuous, what implies $\frac{dI}{dt}(0^+) = \frac{dI}{dt}(0^-) = \frac{dI_{out}}{dt} = 0$.

Using these initial conditions in (3.4), $A = I_{out}$ and $B = \frac{\lambda I_{out}}{\omega_r}$.

$$I_1(t) = I_{out}(\cos(\omega_r t) + \frac{\lambda}{\omega_r} \sin(\omega_r t))e^{-\lambda t} \quad (3.10)$$

This function reaches its minimum at $t = \frac{\pi}{\omega_r}$, $I_{min} = -I_{out}e^{-\lambda\pi/\omega_r}$.

3.1.4 NMOS turning-on ②

During the NMOS turning-on, the current I_{out} continues to flow through the ground interconnection. Current inrush is due to NMOS gate charging and does not depend on current load I_{out} , so the more convenient current value is chosen: $I_{out} = 0A$. Capacitor charging stimulates the RLC parasitic network where $R = R_{Non}$, $C = C_{Non}$ (3.8) and $L = L_{tot}$ (2.11).

The corresponding model for NMOS turning-on (phase ②) is represented in Figure 3.10b. The ideal switch represents the NMOS buffer switching to V_{in} .

V_0 value is calculated as a ratio of the charge demand and the total capacitance of the parasitic network,

$$V_0 = V_{in} - \frac{\Delta Q_2}{C_{Non}} \quad (3.11)$$

The charge demand on V^+ to refill gate capacitances represented in Figure 3.8 is given by (3.12),

$$\begin{aligned} \Delta Q_2 &= -V_{th}C_{dbp} - V_{th}C_{gdp} + (V_{in} - V_{th})C_{gdn} + V_{in}C_{gsn} \\ &= V_{in}(C_{gdn} + C_{gsn}) - V_{th}(C_{dbp} + C_{gdp} + C_{gdn}) \end{aligned} \quad (3.12)$$

A and B are calculated using (3.4) with initial conditions:

- I is continuous due to inductance current continuity constraint so $I(0^+) = I(0^-) = 0$.
- $L \frac{dI}{dt}(0^+) = V_{in} - RI(0^+) - V_C(0^+) = V_{in} - V_0 = \frac{\Delta Q_2}{C_{Non}}$ due to capacitor voltage continuity constraint.

The current response during transition is then:

$$I_2(t) = \frac{\Delta Q_2}{LC\omega_r} \sin(\omega_r t) e^{-\lambda t} \quad (3.13)$$

The maximum of that function is reached at $t = \frac{1}{\omega_r} \arctan(\frac{\omega_r}{\lambda})$ and is equal to $I_{max} = \frac{\Delta Q_2}{LC\omega_r} \frac{1}{\sqrt{1+(\frac{\lambda}{\omega_r})^2}} e^{-\frac{\lambda}{\omega_r} \arctan(\frac{\omega_r}{\lambda})}$ with $\sin(\arctan(x)) = \frac{x}{\sqrt{1+x^2}}$.

3.1.5 NMOS turning-off ③

The phenomena involved during this transition are similar to the ones during the transition ②: the output current I_{out} continues to flow through ground interconnection. But the gate capacitors of the NMOS are shorted so the charge demand is highly reduced:

$$\Delta Q_3 = V_{th}(C_{dbp} + C_{gdp}) \quad (3.14)$$

As a result, the overshoot and so the noise contribution is relatively low compared to the other transitions as illustrated in Figure 3.9. For our study this transition is considered noiseless.

3.1.6 PMOS turning-on ④

During this transition, the PMOS gate is discharged to ground and the output current I_{out} swaps from the ground interconnections to the supply interconnections. The two phenomena described previously for transitions ① and ② are involved.

The transition charge paths are presented in Figure 3.8. The total transferred charge is expressed as

$$\begin{aligned} \Delta Q_4 &= -\Delta V_{gp} C_{gsp} + (\Delta V_{lx} - \Delta V_{gp}) C_{gdp} + \Delta V_{lx} C_{gdn} + \Delta V_{lx} C_{dbn} \\ &= V_{in}(C_{gsp} + 2C_{gdp} + C_{gdn} + C_{dbn}) + V_{th}(C_{gdp} + C_{gdn} + C_{dbn}) \end{aligned} \quad (3.15)$$

Unfortunately the calculation could not be done directly as for ② due to the sequence transition.

PMOS turning-on can be split in four phases presented in Figure 3.11a: the charging of V_{sgp} to threshold (A), the increase in current through PMOS channel I_{dsp} (B), the rise of V_{lx} to V^+ (C) and finally the charging of V_{sgp} from threshold to V^+ (D).

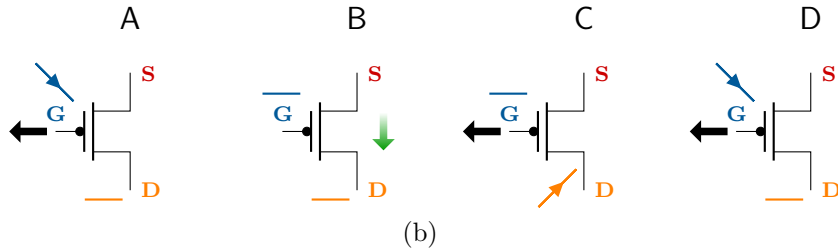
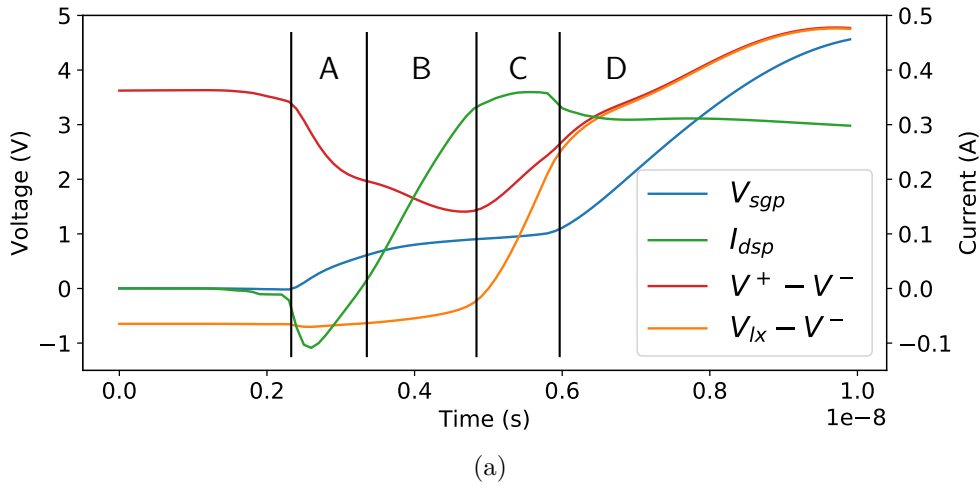


Figure 3.11 – Simulated waveforms during transition ④

i

The phase (C) is called "Miller plateau" in literature [36] because V_{sgp} is approximately flat during this period. The node V_{lx} injects charge on the gate of the MOSFET maintaining the gate potential value. In the present case, the Miller plateau is extended to phase (B). This change is due to the driver integration with the power MOSFET. The variations of the current going inside the chip are limited by package parasitic inductance. In consequence, the current goes through the channel and no current discharges the gate during this phase. The current and voltage variation are represented in Figure 3.11b.

The latter phase (D) absorbs the overshoot created by the previous phase, so at end the overshoot is due to charge transfer during the increase of V_{sgp} to V_{in} . Consequently the ringing does not depend on output current level.

The charge variation during the phase D is expressed as,

$$\begin{aligned} \Delta Q_4 &= (-\Delta V_{gp} - V_{th})(C_{gsp} + C_{gdp}) + (V_{in} - \Delta V)(C_{gdn} + C_{dbn} + C_d) \\ &= (V_{in} - V_{th})(C_{gsp} + C_{gdp}) + (V_{in} - \Delta V)(C_{gdn} + C_{dbn} + C_d) \end{aligned} \quad (3.16)$$

There are fluctuations on the supply voltage due to the previous phase: the V_{lx} node increases to V^+ . These fluctuations are taken into account in the term $(V_{in} - \Delta V)(C_{gdn} + C_{dbn} + C_d)$ with $\Delta V = V^+ - V^-$. The voltage variation

is expressed using charge transfer calculation as:

$$V_{in} - \Delta V = L \frac{dI}{dt}(0^-) = \frac{\Delta Q_i}{C_{Pon}} \quad (3.17)$$

$$\Delta Q_i = (C_{gdn} + C_{dbn} + C_{gdp})V_{in} + (C_{gdn-i} + C_{dbn-i} + C_{gdp-i})V_{th} \quad (3.18)$$

The extension X_{-i} is added to considered capacitor values of the previous state (*OFF*) to take into account the change in capacitor values depending on the voltage difference applied to it.

The current function is calculated with a similar method as (3.13),

$$I_4(t) = I_{out} + \frac{\Delta Q_4}{LC\omega_r} \sin(\omega_r t) e^{-\lambda t} \quad (3.19)$$

The maximum of that function is reached at $t = \frac{1}{\omega_r} \arctan \frac{\lambda}{\omega_r}$ and is equal to $I_{max} = I_{out} + \frac{\Delta Q_4}{LC\omega_r} \frac{1}{\sqrt{1+(\frac{\lambda}{\omega_r})^2}} e^{-\frac{\lambda}{\omega_r} \arctan(\frac{\omega_r}{\lambda})}$.

The current waveforms during each transition were detailed. From these equations the frequency response is calculated. The models of transition are confronted to simulation and measurement.

3.2 Model validation

The equations of the models' responses are compared to Spice simulations and measurement results for,

$$\begin{aligned} V_{in} &\in \{1.6, 2.1, 2.6, 3.1, 3.6\}V \\ I_{out} &\in \{0, 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.4, 0.5, 0.6\}A \end{aligned} \quad (3.20)$$

The models are verified in two different ways. First, time equation of each transition is compared with spice simulation waveforms without the feedback loop. It permits to study transitions one at a time and with the exact I_{lx} current sink by an ideal source. Second, the system is studied with its feedback loop. Transitions ① and ②, ③ and ④ are respectively associated with dead-time duration. That permits comparisons with spice simulations and measurement results of the buck converter in operation.

The simulation setup of the first test bench is presented in Figure 3.12. PMOS and NMOS gates are driven separately with large time spacing between each transition to analyze the current ringing in each state (damping, resonance frequency). The MOSFET models are provided by STMicroelectronics Design Kit (DK). Parasitic resistors and capacitors of the routing are merged to speed up the simulation. The package model provided by STMicroelectronics package team was obtained by Q3D extraction in a Spice netlist format. Finally the PCB is modeled by a S-parameter file by ANSYS Siwave. Spice parasitic components are used to permit time simulations of the system. The values of these components are adjusted to fit frequency response of the S-parameter model.

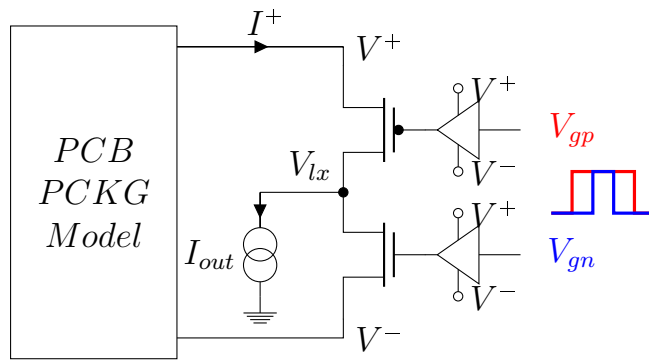


Figure 3.12 – Spice simulation bench with arbitrary large dead-time (feedback loop is not considered)

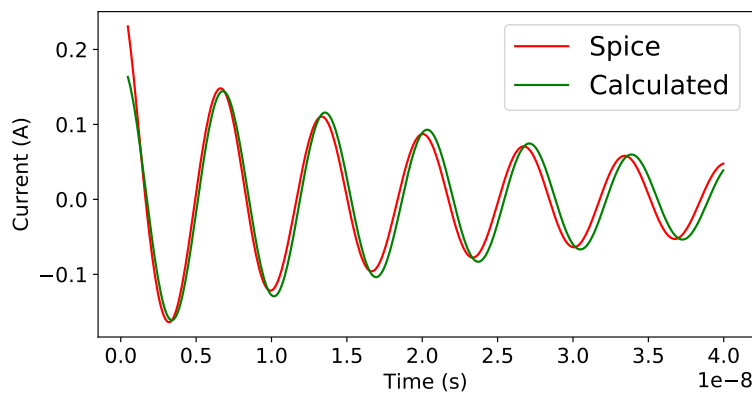


Figure 3.13 – One calculated waveform compared to the corresponding spice simulation for $V_{in} = 3.6V$ and $I_{out} = 0.3A$

The solution is calculated using parameters of the implemented MOSFETs. The equations of the model are superposed to spice simulation of the buck converter to verify the theory. For example, the calculated waveforms are represented in green in Figure 3.13 with the spice simulated waveforms in red during transition ① for $V_{in} = 3.6V$ and $I_{out} = 0.3A$.

The questions are: how far is the model from the solution? How big is the error on R, L, C parameters? The best RLC matching in Spice simulation waveforms is extracted by optimization procedure. The values are compared with theory to estimate the accuracy of the model.

The optimization procedure minimized the error between theory and spice simulation. This error is $\sqrt{\sum \varepsilon^2}$ with ε the difference between theory and spice waveforms for each point (sampling period is set to $T_s = 100ps$). The error is calculated for a range of L and C around the theoretical solution. The results is presented in Figure 3.14a for $V_{in} = 3.6V$ and $I_{out} = 0.3A$: a 3D graph with L and C in (x, y) axis and the error in z axis. The calculated solution is represented by a blue cross and the red line represents the set of fitted solutions.

The set of fitted solutions is represented in Figure 3.14b. There is a solution for every inductance (receptively capacitance) values. L is determined by the

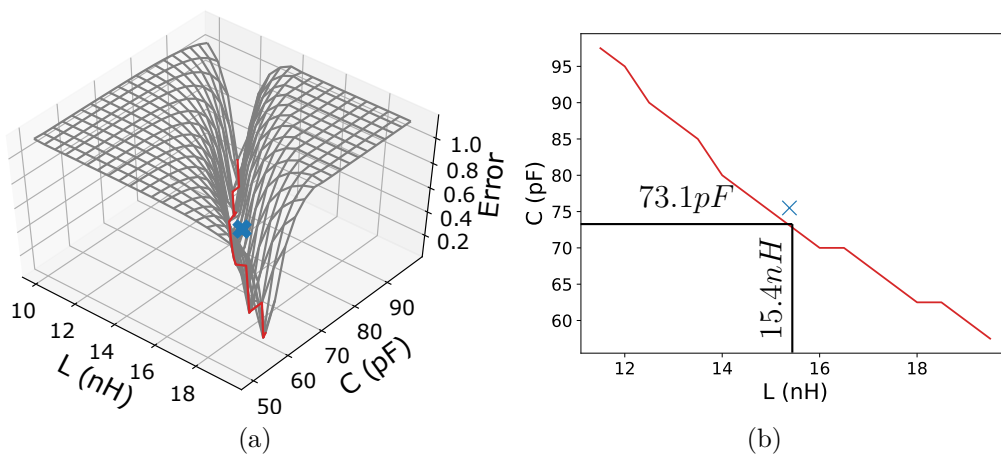


Figure 3.14 – Fitting error for transition ①, $V_{in} = 3.6V$ and $I_{out} = 0.3A$

extraction described in chapter 2. Its value is constant whatever the input parameters (V_{in} or I_{out}) and the state of the power stage. In consequence, the value of L is set to the calculated value ($15.4nH$) and the other parameters are optimized to fit the spice simulation waveform.

The R , C and the initial conditions obtained by fitting are compared with the calculated values for every operating conditions (3.20). The results for transition ① are presented in Figure 3.15 and discuss below.

PMOS turning-off ①

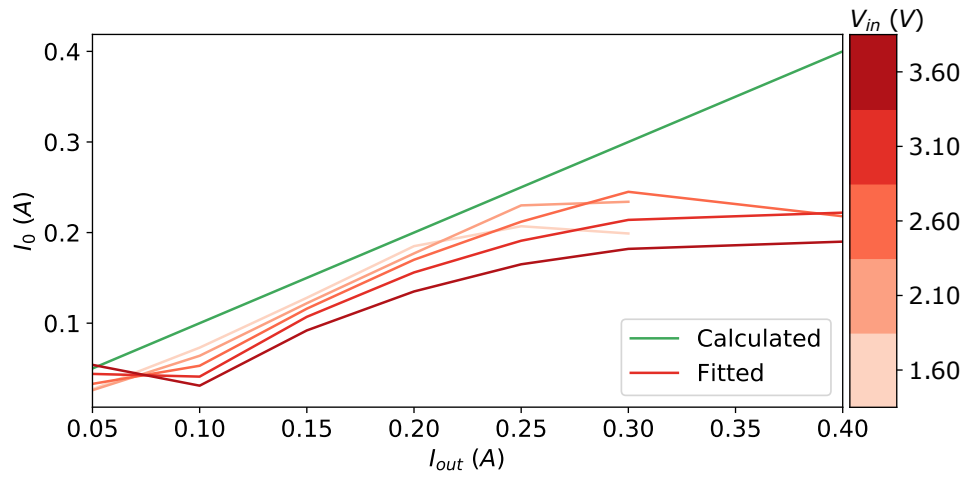
In Figure 3.15a, the initial current in the parasitic RLC is represented. In theory, the initial current I_0 is equal to I_{out} in green. It can be noticed that the maximum current is not $0.6A$ but $0.3A$ or $0.4A$ depending on input voltage V_{in} . At larger current, the results could not be extracted due to convergence issues in the spice simulation.

The initial condition is proportional to output current between $0.1A$ and $0.25A$. At larger current, the initial condition reaches a saturation level. This saturation seems to be linked to the non-convergence of the spice simulation. At smaller current, the stimulation of the change in current path from PMOS to NMOS is masked by the charging of MOSFET capacitances.

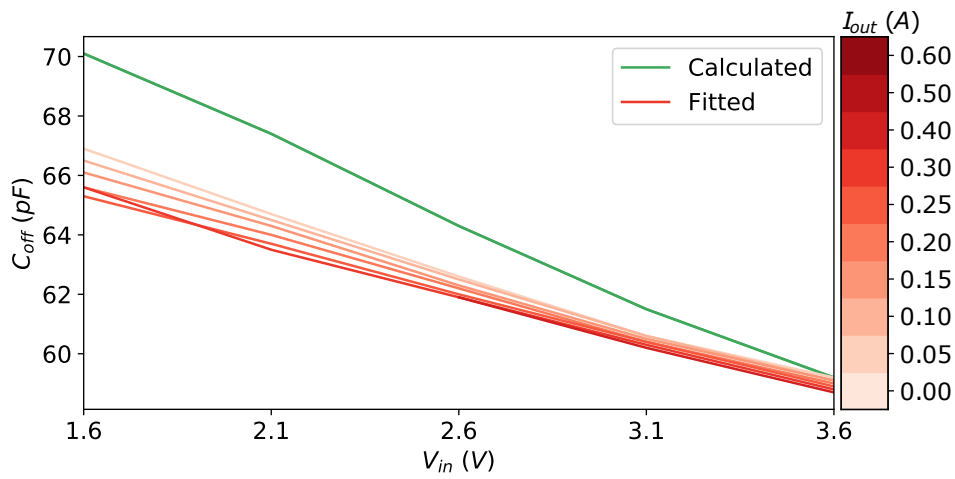
Finally, the current slope is different from what theory predicts and this shift depends on V_{in} value. This shift is due to MOSFET capacitance charging. In Figure 3.8, a part of the current goes from the ground to the output to discharge capacitance C_{gdn} and C_{dbn} of the NMOS. So only a part of the output current remains in supply path what reduces the current path swap at the closing of the PMOS channel. The injected charge variation depends on V_{in} as (3.21).

$$\Delta Q = (C_{gdn} + C_{dbn})(V_{in} - V_{th}) \quad (3.21)$$

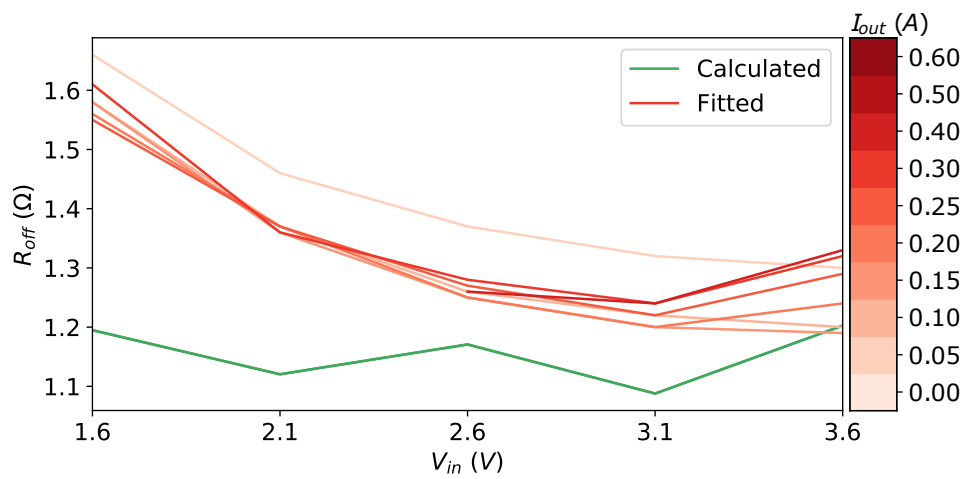
The capacitance value is correlated between simulation and calculation with a maximum error of 6% (see Figure 3.15b). The error on resistance estimation is larger (30%) due to the difficulty to estimate R_{buf} (see (3.9)).



(a)



(b)



(c)

Figure 3.15 – PMOS turning-off ①: I_0 (a), C_{off} (b), R_{off} (c)

V_{in} (V)	1.6	2.1	2.6	3.1	3.6
ΔQ_{2th} (pC)	110	165	225	277	335
ΔQ_{2ext} (pC)	109	164	219	273	327

Table 3.2 – Comparison of charge variations during transition ②: modeling and circuit simulation

The results for transition ② are presented in Figure 3.16.

NMOS turning-on ②

From Figure 3.16a, there are two remarks. First, all the fitted points V_0 (red) are identical independently of the output current except for $I_{out} = 0A$. In that case V_{lx} node is not discharged by the output current in *OFF* state. In consequence, the charge variation is increased resulting in smaller V_0 . Second, the calculated V_0 is shifted from spice-simulation values. The reason of this shift is presented in Figure 3.17.

The buffers turning-on the NMOS gate do not switch instantly from ground to supply connection. The resistance of the buffers goes down during the beginning of the gate charging to reach its final value. During this phase, the RLC model does not describe accurately the charge transfer. Even if the total charge transfer corresponds to theory (error inferior to 3%, see Table 3.2), the differences between the system simulation and the RLC model create an error on initial condition values.

The R and C are estimated with a maximum error of 7%.

The results for transition ④ are presented in Figure 3.18.

PMOS turning-on ④

In Figure 3.18a, the initial voltage condition V_0 depends on output current what does not appear in ΔQ_4 expression in (3.16). ΔQ_4 depends on V_{th} of the PMOS but the Miller plateau is not flat: $V_{sg} \neq V_{th}$ as represented in Figure 3.11. V_{sg} reaches V_{th} value before the current starts rising in PMOS channel. In consequence, if the current is large, it take time to switch and V_{sg} across the PMOS increases. At the end of the current switch, $I_{out} = 0A$, $V_{sg} = 0.75V$ whereas $I_{out} = 0.6A$, $V_{sg} = 1.15V$ in simulation. V_0 value is represented with respect of these two values in Figure 3.18a. The extracted value is within the interval evaluated by analytical analysis.

The R and C are estimated with a maximum error of 5%.

Current measurement

The simulation results are compared with measurement results to verify that the behavior of the system is in-line with the model. The current overshoot and the resonant frequency are compared in the same operating conditions as presented in (3.20).

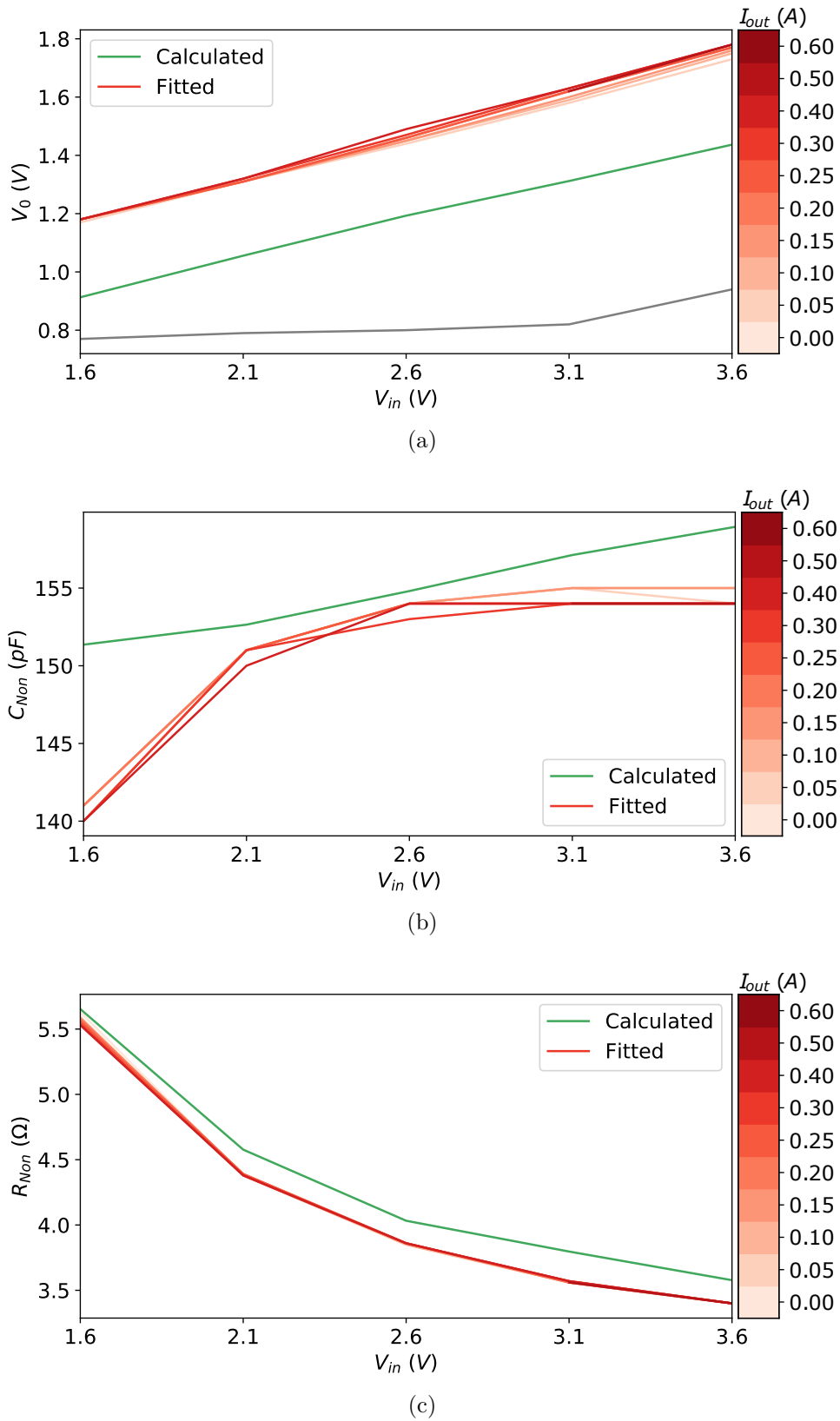


Figure 3.16 – NMOS turning-on ②: V_0 (a), C_{Non} (b), R_{Non} (c)

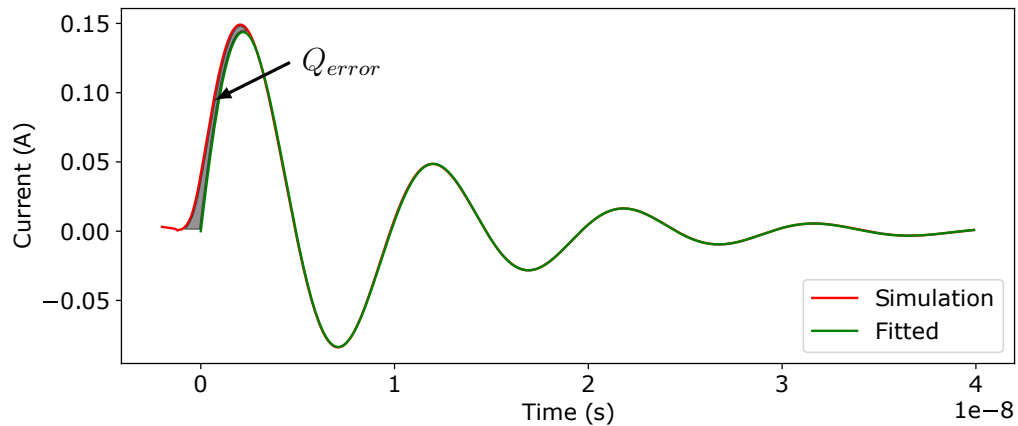


Figure 3.17 – Fitting error during transition ②

On the test vehicle, the buck converter is in action, so the transitions ① and ②, ③ and ④ are associated respectively with dead-time durations. In consequence, *OFF* state time is short so the measurement of the resonant frequency in this state is not possible. Another consequence is that the overshoot contributions of each state are overlapped. But the overshoot during the transition ③ is smaller and could be neglected in practice as presented in section 3.1.5 so the overshoot during the transition ④ can be measured.

The resonant frequency of P_{ON} and N_{ON} states and the overshoot measurement of the transition ④ are presented in Figure 3.19.

In Figure 3.19a, the resonant frequency extracted from the simulation is superior to measurement. This phenomenon is probably due to a larger capacitance on silicon than in the model: for example, due to the parasitic capacitances of the connection grid of the MOSFETs. This assumption is reinforced by the second result in Figure 3.19b: with a larger gate capacitance, the parasitic is less influential.

In Figure 3.19c, the overshoot amplitude is over-estimated but the linear dependency with V_{in} is confirmed.

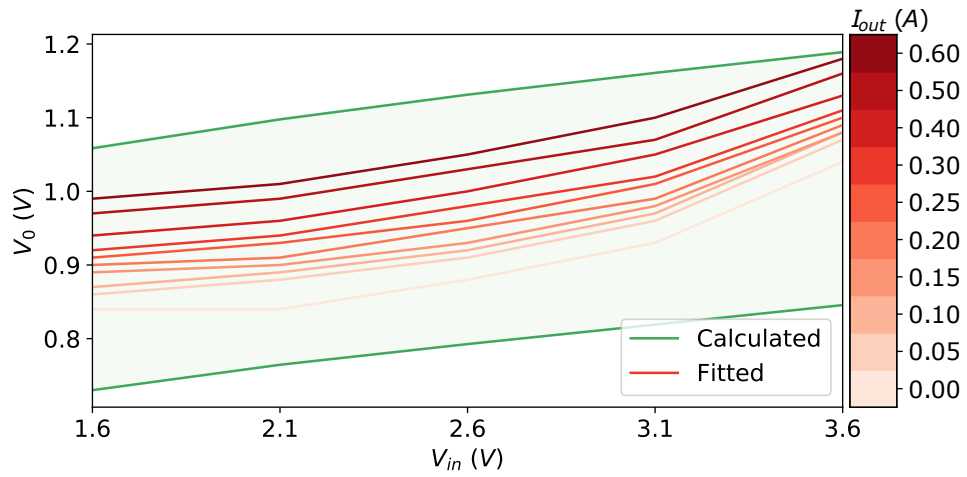
3.3 Frequency response

The frequency spectrum of current I^+ is calculated, to be compared then with results in [4] presented in section 3.1. Moreover these expressions are important to understand phenomena in propagation analysis in section 3.6.

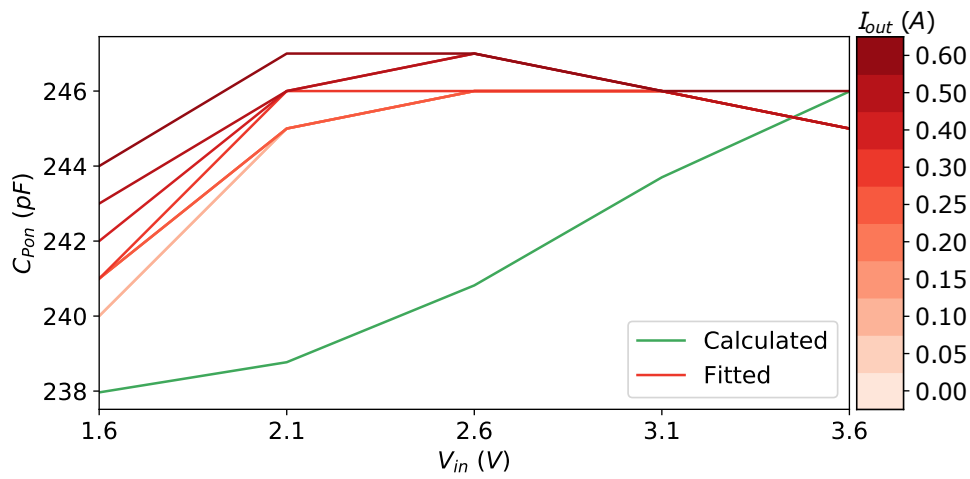
The input current I^+ is decomposed in three parts:

1. a square signal,
2. a saw-tooth signal,
3. a noise signal, composed of the contributions presented in the subsections 3.1.3 to 3.1.6.

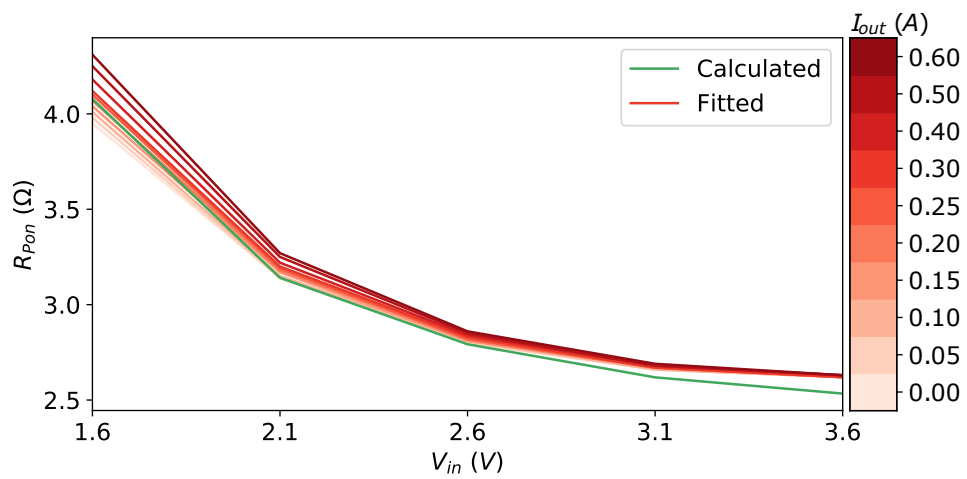
This decomposition is presented in Figure 3.20.



(a)



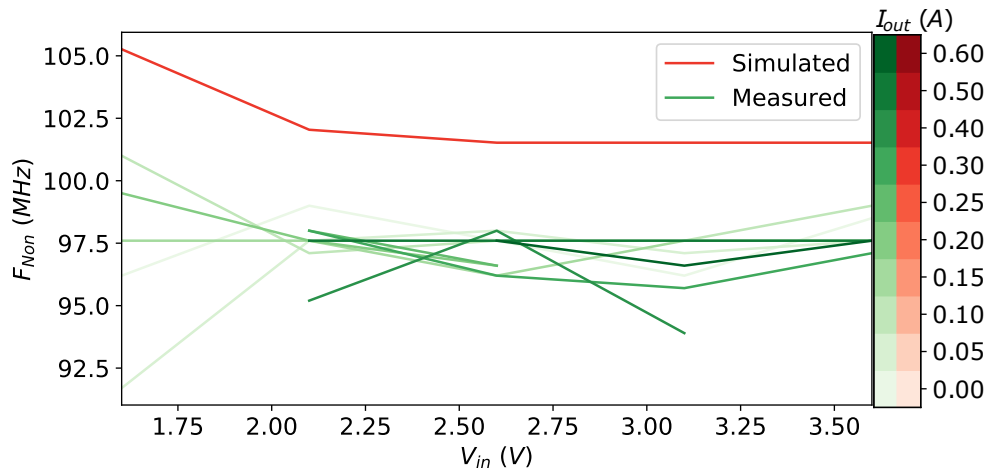
(b)



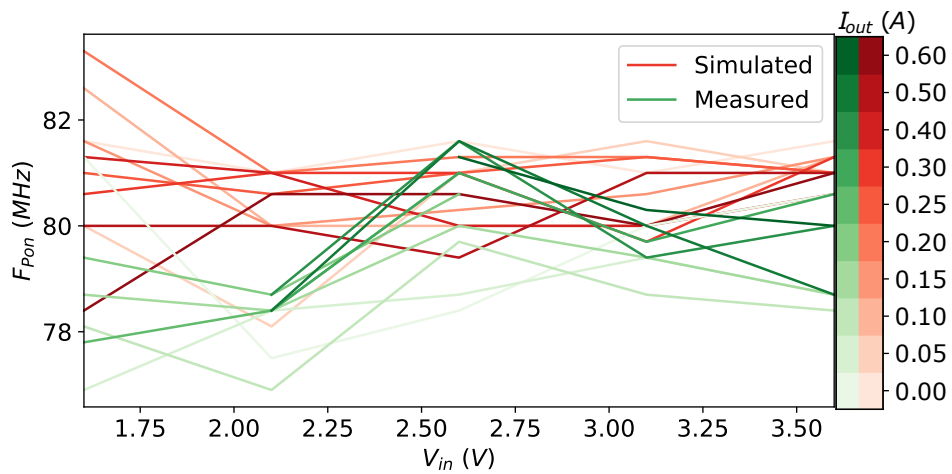
(c)

Figure 3.18 – PMOS turning-on ④: V_0 (a), C_{Pon} (b), R_{Pon} (c)

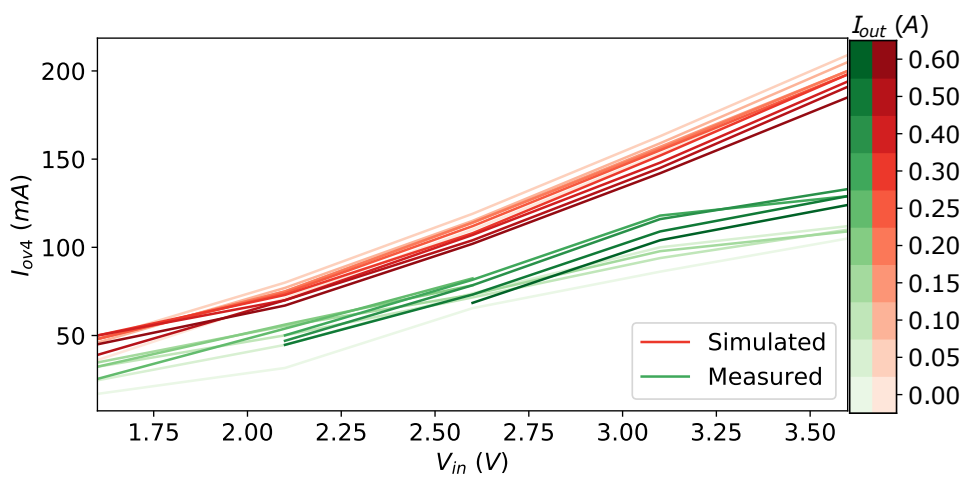
3.3. Frequency response



(a)

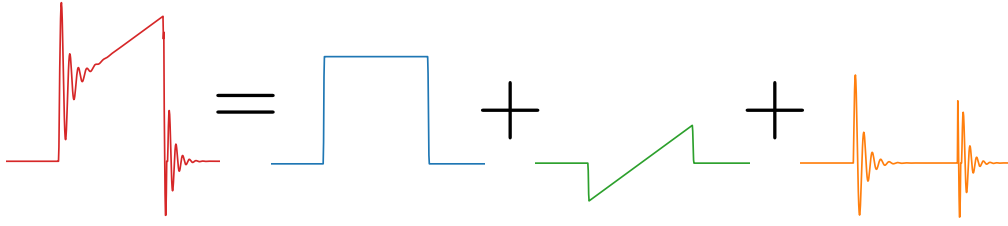


(b)



(c)

Figure 3.19 – Simulations and measurements comparison: P_{ON} (a) and N_{ON} (b) resonant frequencies and overshoot amplitude of transition ④ (c)


 Figure 3.20 – I^+ current decomposition

The spectrum envelop of the square signal with non-ideal rising (resp falling) edge is calculated in [33] and the same approach is applied to the saw-tooth signal (annex C). The result is presented in (3.22).

$$\begin{aligned}
 I_{sqr}(\omega) &= \frac{4I_{out}F_{clk}}{\omega} \sin\left(\frac{\alpha\omega}{2F_{clk}}\right) \\
 I_{saw}(\omega) &= \frac{2\Delta I_{lx}F_{clk}}{\omega} \left(-\cos\left(\frac{\alpha\omega}{2F_{clk}}\right) + \frac{2F_{clk}}{\alpha\omega} \sin\left(\frac{\alpha\omega}{2F_{clk}}\right)\right)
 \end{aligned} \quad (3.22)$$

with α the duty cycle and ΔI_{lx} the current ripple defined in (2.1).

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Using the theory presented in [33], the ideal square (resp. the saw-tooth) signal has to be multiplied by $\text{sinc}(\omega\tau_{on}/2) + \text{sinc}(\omega\tau_{off}/2)$ to obtain the real spectrum envelop with τ_{on} and τ_{off} the rising and falling edge duration. τ_{on} and τ_{off} could be obtained using time equation differentiation when current I^+ reaches 0A in respectively PMOS turning on ④ and PMOS turning off ① transitions (see section 3.1.6 and 3.1.3).

The real noise equation has to be calculated before calculating the frequency response. The duration between PMOS turning-off ① and NMOS turning-on ② is small compared to the period duration. In consequence, the spectrum contribution from transition ① is neglected but the initial condition of the transition ② is modified. The initial current is not 0A as presented in section 3.1.4 but equals to $I_{1f} = I_1(\delta t)$ with δt the dead time duration between transitions ① and ②. Finally the current is given by (3.23),

$$I_2 = (I_{1f} \cos(\omega_r t) + \frac{1}{\omega_r} \left(\frac{\Delta Q_2}{LC} - \lambda I_{1f}\right) \sin(\omega_r t)) e^{-\lambda t} \quad (3.23)$$

The Fourier transform of the noise signal permits to obtain the spectrum envelope. The formula demonstrations are detailed in annex D. The theoretical

frequency response of ① is expressed in (3.24) to be compared with [4].

$$\begin{aligned}
I_1(\omega) &= 2F_{clk}I_{out} \frac{2\lambda + j\omega}{(\lambda + j\omega)^2 + \omega_r^2} \\
I_2(\omega) &= \frac{2F_{clk}}{(\lambda + j\omega)^2 + \omega_r^2} \left(\frac{\Delta Q_2}{LC} + I_{1f}j\omega \right) \\
I_4(\omega) &= \frac{2F_{clk}}{(\lambda + j\omega)^2 + \omega_r^2} \frac{\Delta Q_4}{LC}
\end{aligned} \tag{3.24}$$

At the resonant frequency f_r ($\omega = \omega_r$), the magnitudes are,

$$\begin{aligned}
|I_{1r}| &= \frac{2F_{clk}I_{out}}{\lambda} \frac{\sqrt{4\lambda^2 + \omega_r^2}}{\sqrt{\lambda^2 + 4\omega_r^2}} \\
|I_{2r}| &= \frac{2F_{clk}}{\sqrt{\lambda^2 + 4\omega_r^2}} \sqrt{\left(\frac{\Delta Q_2}{\lambda LC} \right)^2 + I_{1f}^2\omega^2} \\
|I_{4r}| &= \frac{2F_{clk}}{\sqrt{\lambda^2 + 4\omega_r^2}} \frac{\Delta Q_4}{\lambda LC}
\end{aligned} \tag{3.25}$$

The spectrum envelop of PMOS turning-on ④ and turning-off ① can be compared with results in [4] presented in section 3.1. In both studies, the envelop related to transition ④ is dependent of charge variation and the envelop related to transition ① depends on output current I_{out} . A main difference is the presence of τ_{on} and τ_{off} . The formulas are directly linked to system parasitic components and dimensions permitting to understand levers that the designer may play with to control the noise emission.

The envelop is multiplied by the Dirac comb $\text{III}_{F_{clk}} = \sum_n \delta(\omega - 2\pi n F_{clk})$ to obtain the frequency spectrum as presented in annex D. Finally the spectrum is $(I_{env}(2\pi n F_{clk}))_{n \in \mathbb{N}}$.

Another mechanism generates noise at higher frequency: the substrate coupling.

3.4 Effect of substrate coupling

The power MOSFETs are isolated to avoid direct injection of charge from the SMPS noisy switching activity into the substrate. This isolation is realized by adding a Deep N-Well layer below the power MOSFETs as presented in Figure 3.21. The junction between the substrate and the DNW layer can be modeled with a capacitor [37].

In consequence a new RLC is involved during switching with R, the substrate resistance, L the package and PCB parasitic inductance and C, the junction capacitor. The equivalent schematic is presented in Figure 3.22.

Z_{PS} represent the impedance of the parasitic network of the power stage describe in section 3.1. Due to the difference in capacitor values ($C_{+/-} \gg C_{+/-sub} = C_j$), the two resonances can be studied separately. $C_{+/-}$ can be neglected in

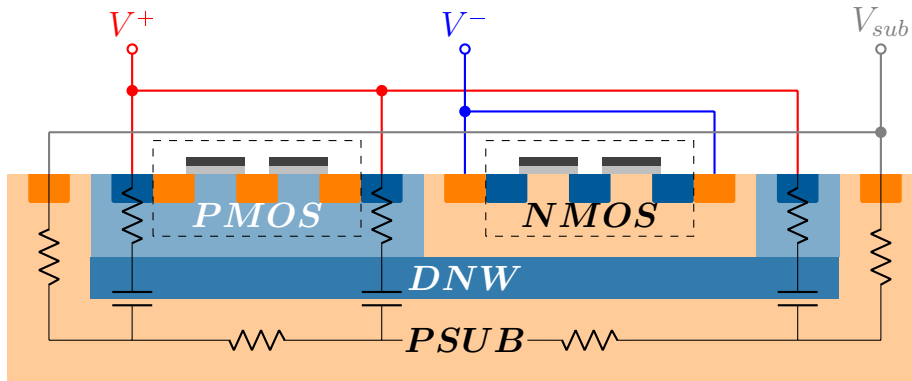


Figure 3.21 – Power stage cross-section

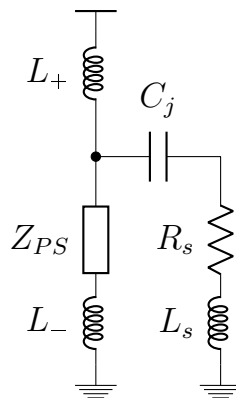


Figure 3.22 – Substrate resonant network

V_{in} (V)	1.6	2.1	2.6	3.1	3.6
f_s calculated (MHz)	637	658	676	692	706
f_s extracted (MHz)	590	605	616	627	632

Table 3.3 – Comparison f_s for theory and extraction

comparison to the substrate DNW junction capacitor and other impedance at substrate resonant frequency ($\sim 500MHz$). In consequence, $Z_{PS} \approx R_{+/-}$.

Using formula detailed in appendix B, the total inductance and resistance are calculated. Considering $(\frac{\omega}{\omega_l})^2 \gg 1$ at resonance with $\omega_l = \frac{R_{+/-}}{L_- - M}$ it comes:

$$R = R_s + \frac{R_{+/-}(L_+ - M)^2}{(L_+ + L_- - 2M)^2}, \quad L = L_s + \frac{L_+L_- - M^2}{L_+ + L_- - 2M}, \quad C = C_j \quad (3.26)$$

With L_+ , L_- and L_s the parasitic inductances on supply, ground and substrate biasing paths respectively. M the coupling coefficient between L_+ and L_- . R_s is the substrate equivalent resistance between junctions and metal contacts.

This RLC network is stimulated by the voltage variation on V^+ due to switching activity. The initial voltage variation could be obtained by multiplying the derived function of the current flowing from V^+ to V^- with the inductance on supply paths, L_+ . It may be complicated to validate and to use this result in practice due to the low amplitude of the voltage variation compared to the situation at the main resonant frequency. However the substrate resonance is important in terms of noise due to its higher frequency (impact on RF) and the path to analog could be at low impedance (propagation paths will be presented in the next section 3.6).

The resonance frequency linked to the junction capacitance with the substrate are presented in Table 3.3.

There is an error of 10% on the estimation of the substrate resonance frequency to be compared to an error of 20% on L or on C_j values.

3.5 Wrap-up on noise generation

What to retain from these models?

1. There are three resonance frequencies in the form $f_r = \frac{1}{2\pi\sqrt{LC}}$: two due to PCB and package power loop inductance, $L_{tot} = L_+ + L_- - 2M$ and the capacitance presented in (3.27):

$$\begin{aligned} C_{Pon} &\approx C_{gdp} + C_{gsp} \\ C_{Non} &\approx C_{gdp} + C_{dbp} + C_{gdn} + C_{gsn} \end{aligned} \quad (3.27)$$

And another resonance frequency is due to $L = L_s + L_+ // L_-$ (L_s substrate bias parasitic inductance) and the junction capacitance C_j between NW and DNW layers connected to V^+ with the substrate connected to PCB ground.

2. There are four transitions: when PMOS and NMOS are turning-on, overshoots are due to current inrush to charge parasitic capacitance. They are proportional to V_{in} and to $C_{gn/p}$ so to the power MOSFET width $W_{n/p}$. PMOS turn-off undershoot due current path switching is function of I_{out} . And finally NMOS turn-off does not contribute to noise significantly.

The voltage overshoots can be limited by reducing the gate buffer strength to slow down the gate charging of the MOSFETs or the current drop in PMOS channel. The charge demand during transition ② and ④ and the current switching speed during transition ① lead to solutions presented in chapter 4.



The resonance frequency are due to PMOS and NMOS C_g with the package L_{pkg} .

The transition overshoots are due to:

1. PMOS turning-off ① $\propto I_{out}$
2. NMOS and PMOS turning-on ②, ④ $\propto V_{in}$
3. NMOS turning-off ③ ~ 0

3.6 Noise propagation - PCB and chip paths

Now that the source of noise, the power stage switching and the associated resonance frequencies are described, the objective is to understand how the noise is propagating to the victim IP. There are two steps to reach that objective. First the entire system is modeled and compared to measurement to verify that no path has been forgotten. Second the parameters of the model are modified to evaluate which of the propagation paths are predominant.

The system is represented in Figure 3.23. There are the noise source, the DC/DC buck converter and the victim, i.e. an analog IP sharing the same silicon substrate as the buck converter. The chip is inside a TQFP100 package (worst case of parasitic impedance) and finally the pins of the circuit are interconnected on PCB.

As presented in sections 2.1.2 and 2.1.3, the package is modeled by an RLCG spice netlist extracted using *Ansys Q3D* simulator and the PCB S-parameter file (.snp) is extracted using *Ansys Siwave*.

A final point needs to be resolved: how to model the substrate and the internal chip propagation?

3.6.1 Chip modeling

The chip model has to include substrate and interconnections, to model the entire chip with reasonable time and resource consumption. Five solutions have been investigated:

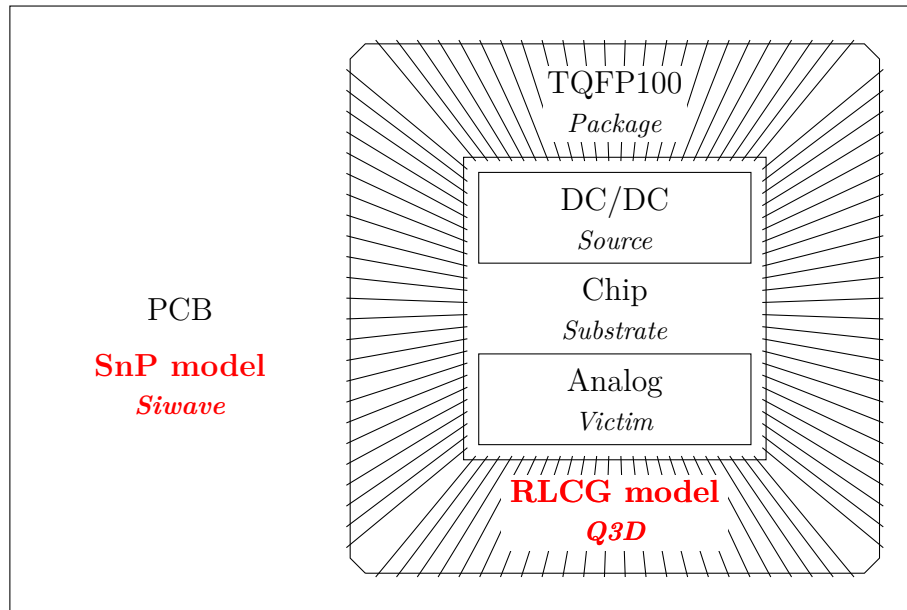


Figure 3.23 – Structure of the system and modeling methods

1. Spice simulations: simple setup (already exist for IP simulation) but do not include substrate and interconnections
2. Spice simulations including layout RC extraction: the interconnections are extracted from layout view to include parasitic Resistances and Capacitances. The simulation bench is easy to setup and includes interconnections but it does not take into account the substrate. Moreover the extraction generates millions of resistances and capacitors. The simulation is not convergent with all these components.
3. Spice simulations using EPFL models [38]: the substrate is modeled with lumped devices, an extraction of parasitic components of the substrate. Each junction is represented by a diode and distance between junctions by a resistor depending on substrate resistivity. The components are modified into 4-port devices (instead of dipole devices) to take into account propagation of minority carriers. The simulation includes substrate but not the interconnections (obtained by RC extraction). Moreover the setup has to be adapted to the CMOS technology and no commercial solution ready to use was existing at the time of the study.
4. FEM/BEM solver: 3D solver resolving electromagnetic equations in the entire chip. These simulators are really accurate to model physical systems but the accuracy comes with a huge complexity. In the studied system there are a lot of different elements. In consequence these solvers are not adapted to our problem: the simulations would spend days or even weeks to calculate the noise propagation if convergence is obtained.
5. Coupling Wave Solution [39]: an optimized BEM solver using model for IP of the chip, reducing the complexity of the system. Moreover this software suite was already under evaluation at STMicroelectronics allowing to quickly obtain the first results.

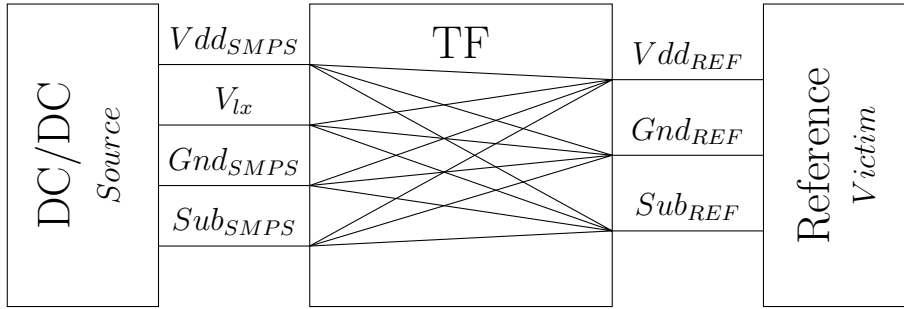


Figure 3.24 – Structure of CWS bench

The chosen solution is CWS software suite [39]. The next section presents the modeling procedure and its application to the studied system.

3.6.2 CWS setup

The structure of CWS bench is presented in 3.24.

The noise generation is modeled by spice Piece-Wise Linear (PWL) sources. On which pins? Which type (Voltage or current source)? There are six pins to and from the power stage: Vdd_{SMPS} , Gnd_{SMPS} , Sub_{SMPS} , V_{lx} , Cmd_{PMOS} and Cmd_{NMOS} . The last two signals are connected to the gate of the first stage of the driver so they can be considered at high impedance. Vdd_{SMPS} , Gnd_{SMPS} and Sub_{SMPS} are voltage supply pins. As voltage input, they are modeled by PWL current sources. And finally V_{lx} as an output voltage is a PWL voltage source. These sources are extracted from Spice time simulation of the system with the environment presented in chapter 2. Then the spectrum of these signals are calculated using FFT with $f_{sample} = 1.6384GHz$ and $T_{acq} = 3T_{clkSMPS} = 1.25\mu s$.



How the FFT parameters have been selected? The FFT make the input signal T_{acq} -periodic with T_{acq} the time acquisition length. Two solutions are possible to achieve a correct result. First if the signal is periodic, the acquisition have to contain a integer number of signal period, M . Second windowing methods can be used [40]. In the present case, the signal is T_{clk} -periodic so the first method is used. Then the FFT algorithm are optimized for $N = 2^n$, $n \in \mathbb{N}$ with N the number of samples. Moreover if N is a multiple of M , the same samples appear at each period so time acquisition length can be reduced by $hcf(M, N)$. The constraints are presented in Figure 3.25.

Finally the chosen numbers are $M = 3$ & $N = 2048 = 2^{11}$ so $f_{max} = \frac{1}{2}f_{sample} = \frac{N}{2T_{acq}} = 819.2MHz > f_{sub}$ and $hcf(M, N) = 1$. $M = 3$ has been selected to sample the noise floor ($M > 1$) to verify the quality of the FFT calculation. Moreover $M = 3$ gives a round number of nanosecond for $T_{acq} = MT_{clk} = 1.25\mu s$.

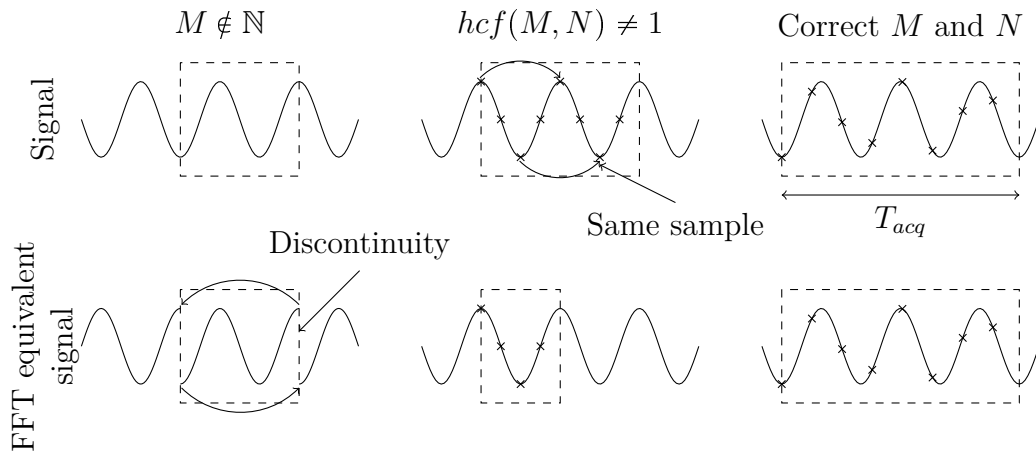


Figure 3.25 – Illustration of FFT constraints

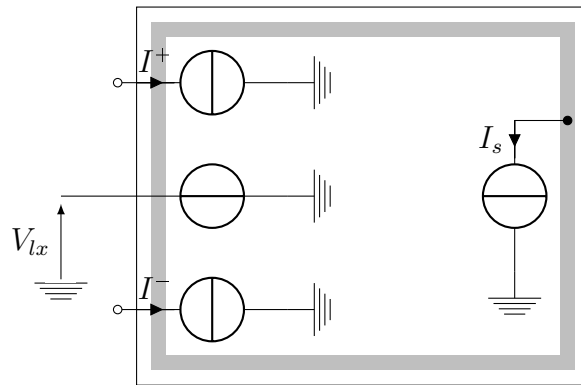


Figure 3.26 – Structure of the source model: the buck converter

The model of the buck converter is represented in Figure 3.26.

The victim pins to be taken into account differ from one IP to another but for the voltage reference studied in this section there are three pins: $V_{dd_{REF}}$, Gnd_{REF} and Sub_{REF} . A S-parameter model of the victim is extracted from Spice harmonic simulation with linear step of $800KHz$ and a maximum frequency of $1.6384GHz$.

The layout is simplified to reduce the overall simulation time: all cells and the Inputs/Outputs (I/Os) not connected to source or victim cells are removed and fillers are replaced by metal connection in the I/O ring. Fillers are non-functional cells implemented to fill unused space of the chip. The objective of these cells is to ensure continuity of power rails and substrate biasing.

The CWS software *WaveIntegrity* uses the process parameters, the layout, the RLCG model of the package and the S-parameter model of the PCB.

The voltage reference is a static structure (DC function). In consequence, the perturbation on the output is calculated using small-signal AC response of the propagated noise. Finally the output signal is transformed into a time signal using iFFT and the results are compared with measurement results.

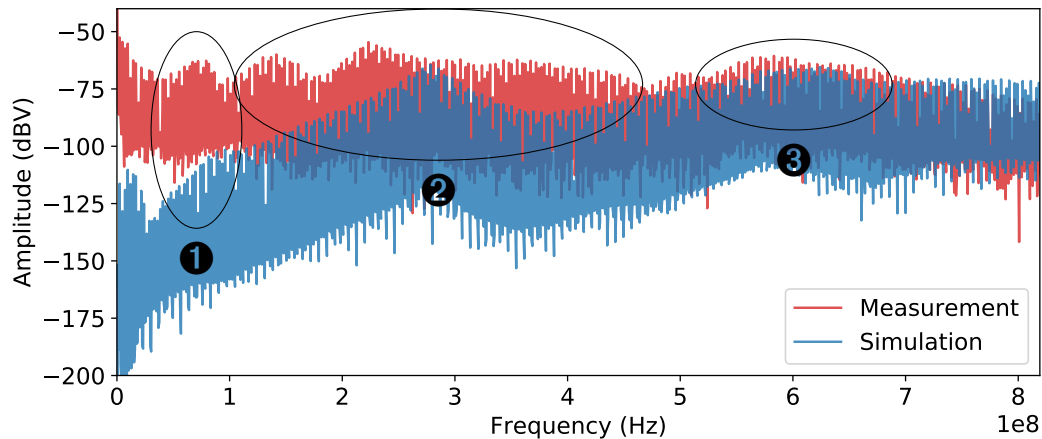


Figure 3.27 – Simulated and measured waveforms comparison on the voltage reference output with $V_{in} = 3.6V$ and $I_{out} = 0.3A$

3.6.3 Measurement vs simulation

The comparison between measured and simulated waveforms in frequency domain for $V_{in} = 3.6V$ and $I_{out} = 0.3A$ is presented in Figure 3.27.

There are three parts in measured frequency spectrum:

- ❶ $f \sim 80MHz$: the resonance of gate capacitances with package inductances presented in section 3.1.1,
- ❷ $100MHz < f < 500MHz$: the harmonics of the current spectrum described in (3.22),
- ❸ $f \sim 600MHz$: the resonance of junction capacitances between Deep NWell and substrate with package inductances presented in section 3.4.

In terms of frequency, the part ❸ is well discriminated. The intermediate resonance frequencies ❷ are merged into one contribution at higher frequency.

In terms of amplitude, there is a "high-pass filter" effect in simulation results rejecting the low frequency contribution (❶ and ❷). But the estimation of part ❸ amplitudes is correct.

The global propagation model was described. The next subsection analyzes the different noise propagation paths and discuss two limitations.

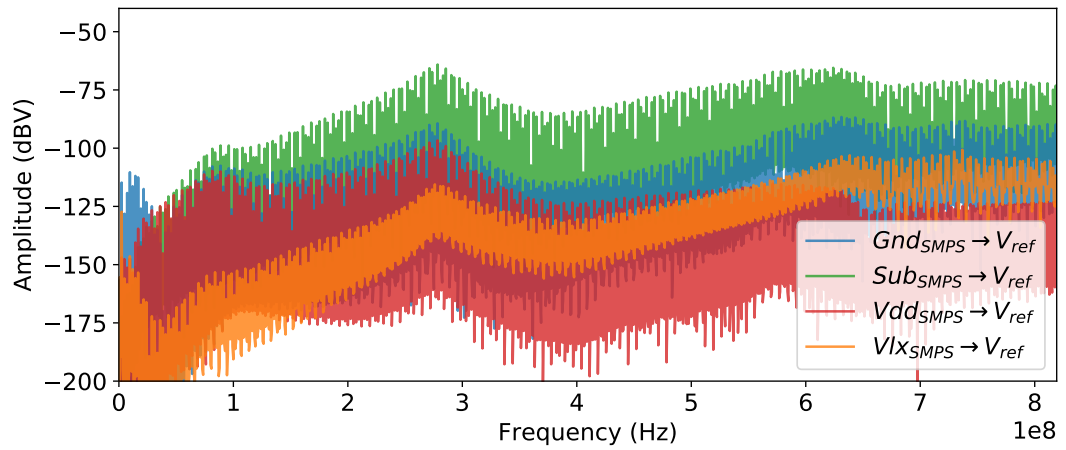
3.6.4 Propagation path analysis

Spectra in Figure 3.28a represent the contributions of aggressors' ports to the victim output port.

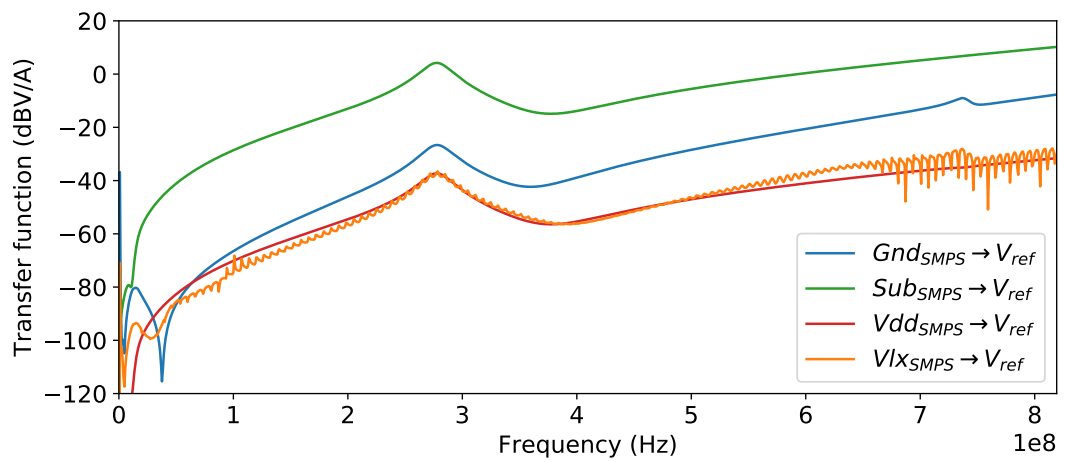
The main contributor at low frequency is the GND_{SMPS} node but above $50MHz$ the noise amplitude is due to Sub_{SMPS} . The peak at low frequency ($\sim 20MHz$) is due to internal resonance frequency of the buffer at the output of the voltage reference.

The theory presented in section 3.1 shows that the principal noise generator is the I^+ (or I^-) current but at the victim inputs the main contributor is the substrate. The transfer functions are presented in Figure 3.28b to understand this difference.

3.6. Noise propagation - PCB and chip paths



(a)



(b)

Figure 3.28 – Noise contributions and transfer functions from buck converter pins to voltage reference output

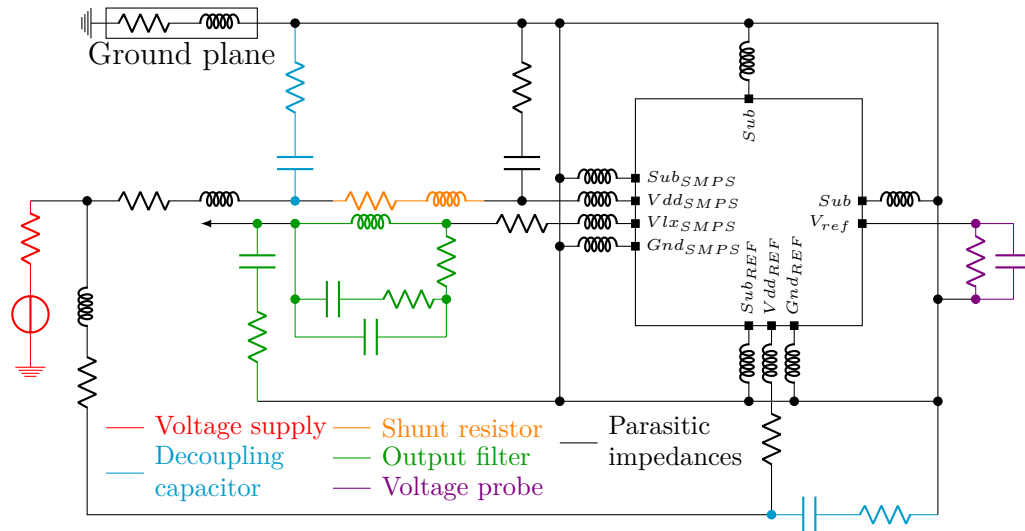


Figure 3.29 – Equivalent schematic of the PCB

Transfer functions are expressed in V/A but the Vlx_{SMPS} noise is represented by a voltage source. The voltage source is applied to the parasitic network and the current coming from this source is then used as a noise stimulator.

There is a resonance frequency in the transfer functions at $300MHz$ and the substrate transfer function is $40dB$ higher than the others. The parasitic impedances are modified to analyze the variation in transfer functions and to determine which noise path is preponderant between the source and the victim.

It is difficult to analyze and to modify the PCB model in S-parameter format. In consequence, a model of the PCB in lumped components is fitted with the S-parameter models. The equivalent schematic is represented in Figure 3.29.

First all external components are represented by a manufacturer model. Then a R and a L are added to model line parasitic impedances and a L to model a parasitic inductor of a via. Finally all the schematic is fitted with S-parameter model. A parasitic capacitor is needed on Vdd_{SMPS} before the shunt to fit with S-parameter results. The transfer functions of S-parameter model (SNP) in dotted line and the schematic model (SCH) in continuous line are compared in Figure 3.30.

Below $50MHz$, there is some differences in Gnd_{SMPS} Transfer function what changes the response in low frequency spectrum. The Vlx_{SMPS} transfer function is also modified and in a larger bandwidth ($-10dB$ at $100MHz$) but its contribution to noise is not significant so it has not an impact on accuracy of the model.

Now the model can be modified to evaluate the influence of schematic components on noise propagation paths and determine the characteristics of these paths.

3.6. Noise propagation - PCB and chip paths

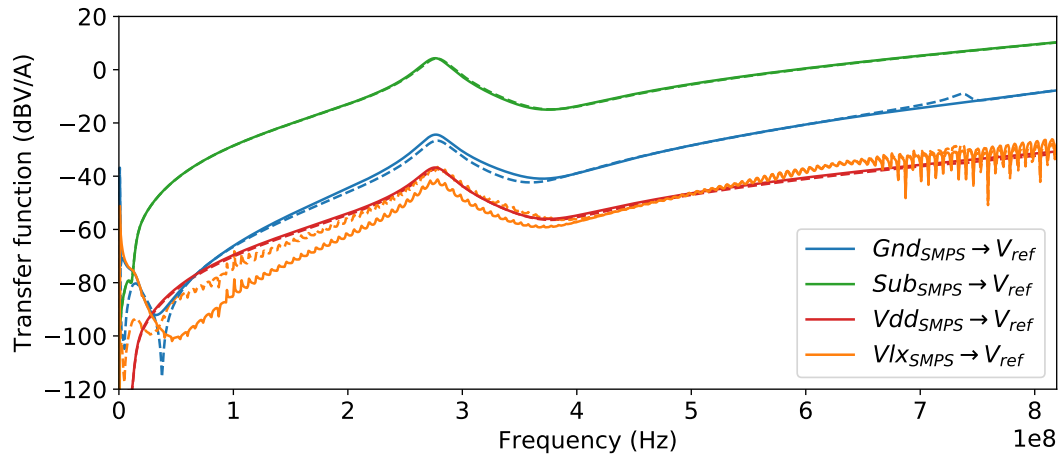


Figure 3.30 – Transfer function comparison between S-parameter model (dashed line) and lumped model (continuous line) of the PCB

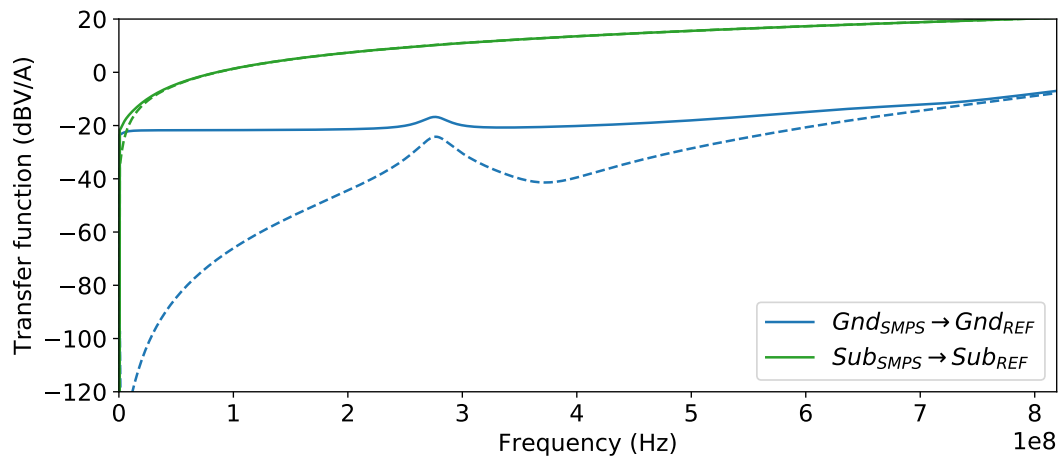


Figure 3.31 – Influence of 0.1Ω resistance in ground connection on transfer functions (dashed lines represent previous results)

Is the substrate pollution due mainly to PCB or on-chip interconnections? A 0.1Ω resistance is added in the ground path (boxed impedance in Figure 3.29). The variation of transfer function is presented in Figure 3.31.

The transfer function from Sub_{SMPS} to Sub_{REF} does not change significantly in comparison to initial configuration whereas the transfer function from Gnd_{SMPS} to Gnd_{REF} increases of $40dB$ at the buck converter resonance frequency ($\sim 80MHz$) and of $10dB$ at the substrate resonance frequency. The path between source and victim are symbolized in the schematic in Figure 3.32.

The substrate noise propagation is not impacted by change in resistance connection to ground on PCB so the major part of noise is propagating to the victim by on-chip paths in opposition to ground noise propagates through PCB interconnections to the victim. This is due to metal interconnections on chip of the substrate all over the circuit. The layout net view is presented in Figure 3.33.

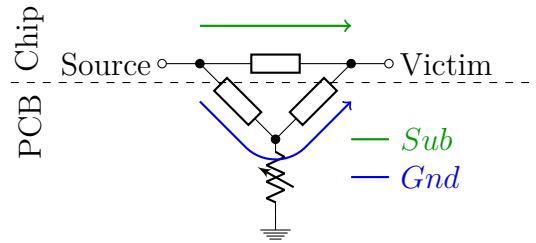


Figure 3.32 – Substrate and ground paths

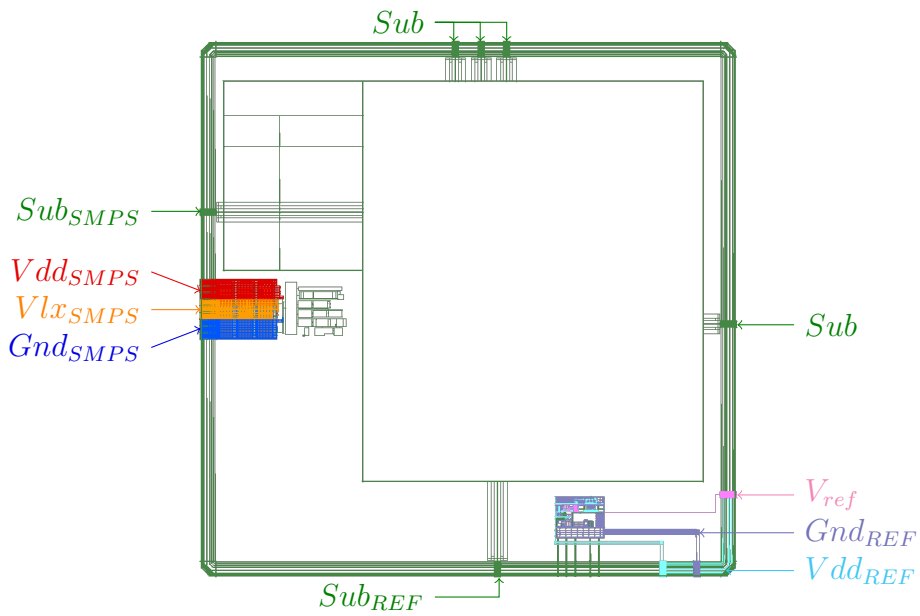


Figure 3.33 – On-chip nets representation

The substrate net is represented in green. This net is connected to the entire chip by the I/O ring and the substrate biasing interconnections. In consequence the path between noise source and victim is in low impedance.



The substrate noise is not propagated to the victim through direct substrate cross-talk but by biasing contacts interconnected all around the chip.

Where does the path resonance at 300MHz come from? A parasitic inductor is added on pins of the IC to find which ones influence this resonance.

An increase in parasitic inductances in the reference supply path reduces the paths resonance frequency. The on-chip parasitic capacitor between Vdd_{REF} and Gnd_{REF} resonates with package and track inductances. The difference between simulation and measurement is due to the simplification of the integrated circuit. The layout was simplified to reduce simulation time: all cells and the Inputs/Outputs (I/Os) not connected to source or victim cells are removed and fillers are replaced by metal connection in the I/O ring. These simplifications change resonances of the propagation paths.

How to correct the "high pass filter" issue in Figure 3.27? Adding a resistor on ground plane connection increases the low frequency spectrum and even the contribution of the buck converter resonance frequency (see Figure 3.31). In consequence, adding parasitic impedance in ground plane should correct the "high pass filter" issue.

Adding a resistor also increases the DC and very low frequency spectrum and the natural resonance of the voltage reference becomes preponderant. Finally an inductor is added: at low frequency the inductor impedance is small and at high frequency noise is already propagating on-chip so a change in PCB impedance does not have impact on this frequency range. The spectrum obtained with an inductor of $0.5nH$ is compared to measurement and the model without any inductor in Figure 3.34.

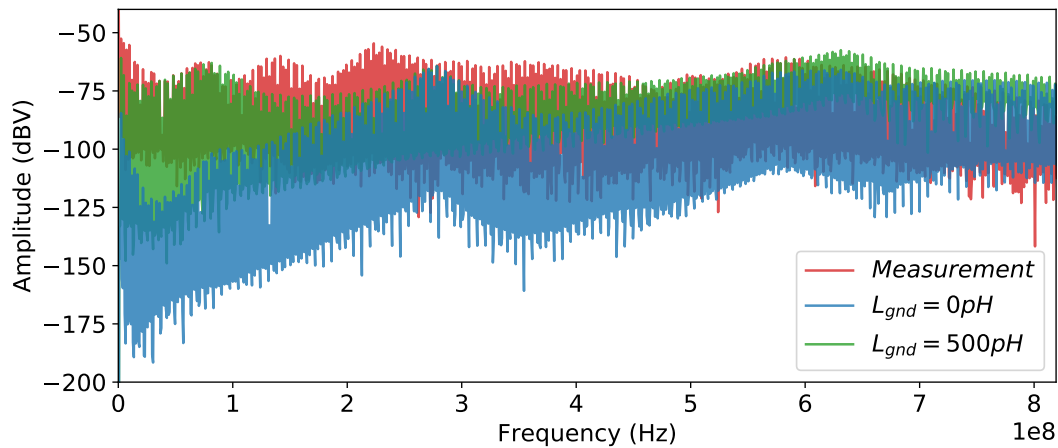


Figure 3.34 – Voltage reference spectrum comparison between model with or without $0.5nH$ added and measurement

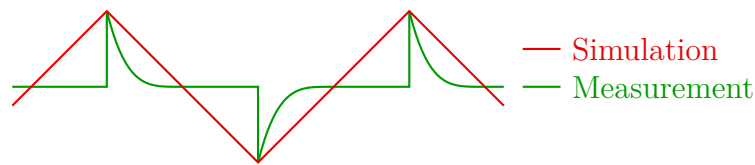


Figure 3.35 – Low frequency pattern: simulation versus measurement



The baseband part of the PCB impedance is not described accurately by the S-parameters and the equivalent schematic in Figure 3.29 because the spectrum has a resolution of $0.8MHz$. Moreover the supply cables are not included in the S-parameter extraction, in consequence there is no resonance between the input capacitance and the parasitic inductance of the cable. Finally the DC supply impedance has to be described by a more complex model than a simple resistor. For all these reasons, parasitic impedances have to be added on the supply path, i.e. models have to be corrected.

A resistor of 0.1Ω could be added in series with the inductance of the ground plane to be aligned with measured baseband spectrum. However in time domain, the resistor value change only the amplitude of the saw-tooth signal represented in Figure 3.35 but does not fit with the actual low frequency signal of the measurement. This part of the spectrum and this part of the PCB are not the main area of this study so the model is finally limited to a simple R and L.

The "high pass filter" issue is solved but the contributions of different paths to noise change as presented in Figure 3.36.

Vdd_{SMPS} and Gnd_{SMPS} are the main noise contributors. A change in PCB impedance affects PCB noise paths. In consequence, the substrate is less influenced by this change than supply and ground paths. Moreover all port of the

3.6. Noise propagation - PCB and chip paths

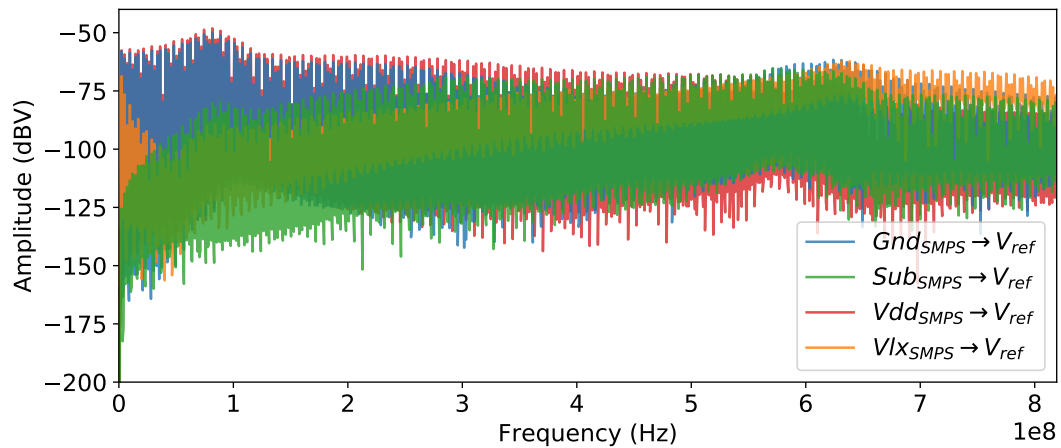


Figure 3.36 – Noise contributions from buck converter pins to voltage reference output with an added $0.5nH$ parasitic inductance

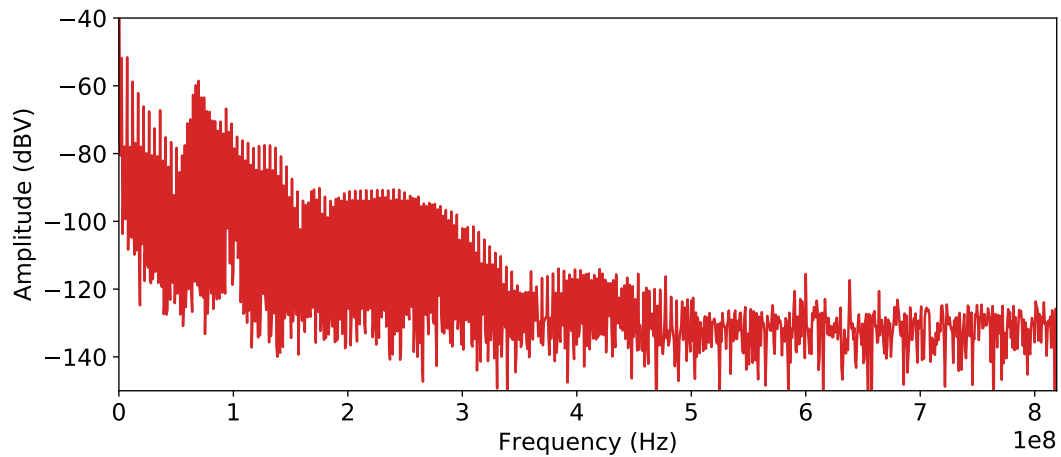


Figure 3.37 – Voltage reference spectrum with buck converter off and clock signal on V_{lx} to emulate the buck operation

buck converter contribute to the resonance amplitude at $\sim 600MHz$.

The spectrum modification and its correlation with measurement show the limitations of the S-parameter extracted model with respect to ground plane imperfections.

A measurement is done to verify the propagation of $V_{lx_{SMPs}}$ throughout the system. The chip is operating with the reference voltage activated but the buck converter is off. The inductor of the buck converter L_{out} is disconnected. A clock signal is applied on V_{lx} node to stimulate the parasitic network. The reference voltage spectrum is presented in Figure 3.37.

The spectrum is significant with a maximum voltage amplitude of $-60dB$ at $70MHz$. The edge slopes and the impedances are different from the true $V_{lx_{SMPs}}$ stimulation so this contribution cannot be simply added. The noise is propagating to the reference voltage through the ground plane so it shows again the limitations of S-parameter models in describing the ground plane impedance.

This propagation model is verified for operating conditions in (3.20). As the

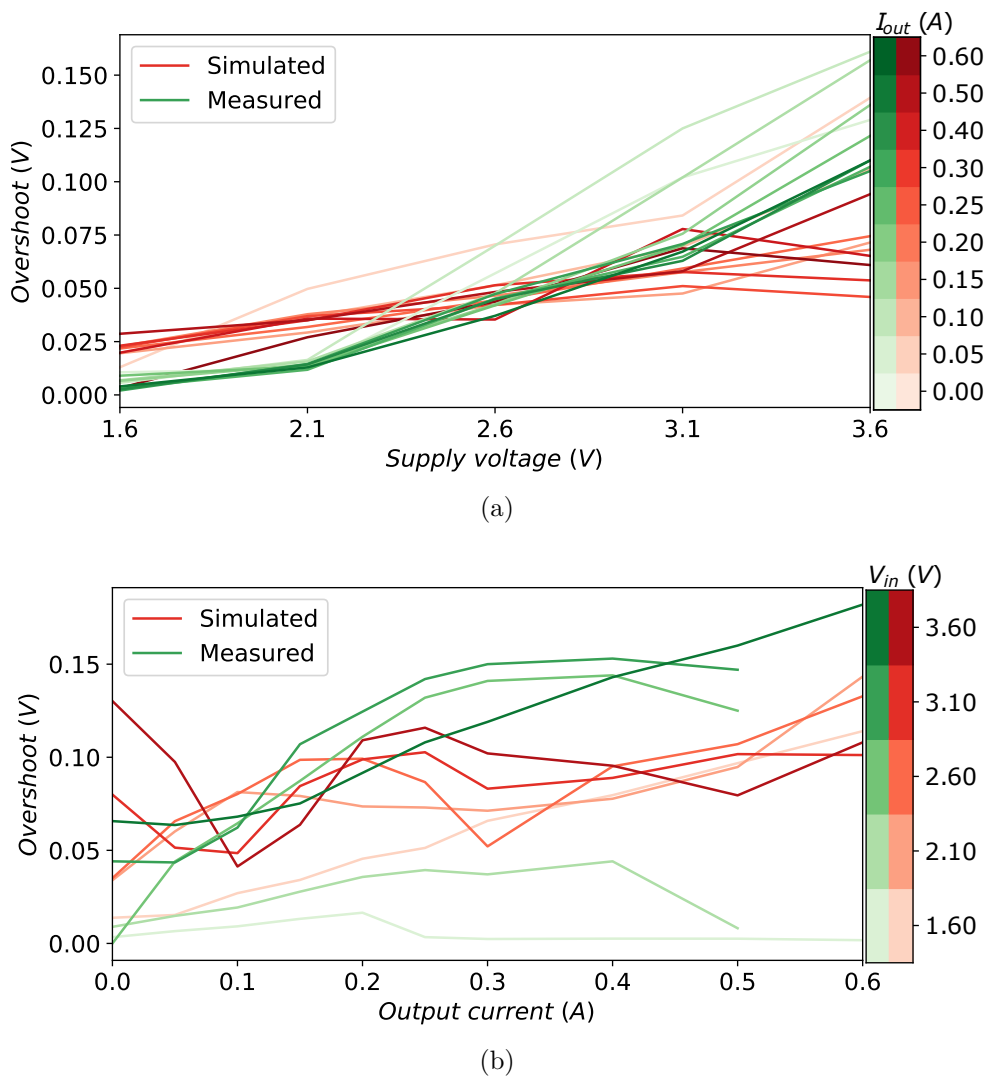


Figure 3.38 – Amplitude comparison on the voltage reference output between measurement and simulation results due to PMOS turning-on (a) or NMOS-turning-on (b)

resonance frequencies do not largely fluctuate, only the amplitudes of the time overshoots are extracted. The comparison between measurement and simulation results is presented in Figure 3.38. Color variations represent the different output currents $I_{out} \in [0A, 0.6A]$ in Figure 3.38a and the different supply voltages $V_{in} \in [1.6V, 3.6V]$ in Figure 3.38b.

In the results of Figure 3.38a, the overshoots depend on voltage supply V_{in} level. This dependency is in-line with the theoretical analysis of PMOS turning-on ④ (see section 3.1.6).

In measurement results of Figure 3.38b, the overshoots are proportional to the output current I_{out} level. For 1.6V and 2.1V supply voltage levels (the two waveforms in light green), the overshoot decreases for an output current above 0.2A and 0.4A respectively. It is due to the large duty cycle: the input current I^+ does not reach 0A because the *OFF* phase is too short.

In simulation results and at $I_{out} = 0A$, the overshoots depend on the supply voltage V_{in} and at higher current, the overshoots become proportional to I_{out} level.

In measurement as in simulation, the dependency is unclear due to superposition of PMOS turning-off ① and NMOS turning-on ② contributions to noise level: one depends on the output current and the other on the supply voltage.

Finally the measurement results are in correlation with the simulation results in a first perspective.

3.6.5 Propagation synthesis

The measured spectrum is composed of **three different resonance frequencies**. One, described in section 3.1, is due to the **buck converter emission** ($\sim 100MHz$). Another presented in section 3.4, is due to **junction capacitance** of NWell and Deep NWell of the buck converter power MOSFET with the substrate ($\sim 600MHz$). And finally resonance frequencies appear between those two, added by the **propagation environment**. Indeed the parasitic impedances along propagation paths are susceptible to resonate to noise stimulation. The identification of these parasitic impedances is not part of the study. An analysis may be difficult due to the large number of elements to consider. However there are two preponderant paths: on-chip and PCB propagation.

At **low frequency** (below $\sim 400MHz$) the noise is mainly propagating through **PCB supply connection and ground plane**. The S parameter extraction using ground plane as reference underestimates the propagation of noise through the ground plane. Other port configurations have been tested. Port reference connected to the absolute ground or to the ground connection of the board for example. Due to the physical size of the port (distance between pin and reference), the obtained S-parameter models were not passive what does not correspond to reality of the PCB.

At **high frequency** (above $\sim 400MHz$) the noise is propagating through **on-chip interconnections** and especially through I/O ring. The metal layers are low resistive and the package parasitic inductances at that frequency are high impedance avoiding the noise to reach the ground plane. The analysis has been realized using CWS software suite, *WaveIntegrity*, to build a global propagation model. The results show the importance of accurate source and victim models but a simple model of the interconnections is enough to describe the propagation. The substrate biasing all around the chip does not significantly change the transfer function between the source and the victim pins. This is due to the high resistive of the substrate in this technology ($10\Omega.cm$): noise does not propagate through long distance inside the substrate.



There are three kinds of resonance frequencies:

1. $\sim 100MHz$: buck converter emission
2. $\sim 600MHz$: buck converter substrate coupling
3. $200MHz - 500MHz$: propagation paths impedance

There are two main propagation paths: PCB supply and ground for low frequency range (below $400MHz$) and on-chip interconnections for higher frequency range.

The next chapter presents solutions or improvement to the present system to reduce noise emission and noise propagation throughout the system.

4 Solution implementation

In the previous chapter, the noise generation, parasitic simulation and ringing analysis, and the noise propagation has been exposed. The objective of this chapter is to answer each point exposed previously.

Each of the following sections presents a solution to decrease noise impact on the victim. There is a solution for the two stimulation phenomena, the current path change developed in section 4.1, the gate charging inrush current developed 4.2. Then a modification of the chip top routing is considered in order to decrease noise propagation in section 4.3. Finally other investigations are presented in section 4.4.

4.1 Smooth current switching

The solution is working on PMOS turning-off transition ①. As explained in section 3.1.3, the transition undershoot is dependent of output current of the buck converter I_{out} . A precise description of what happen before the current switching is needed to explain the solution. After that the solution mechanism is described and how it is implemented in the test vehicle. Finally the characterization of the solution is presented.

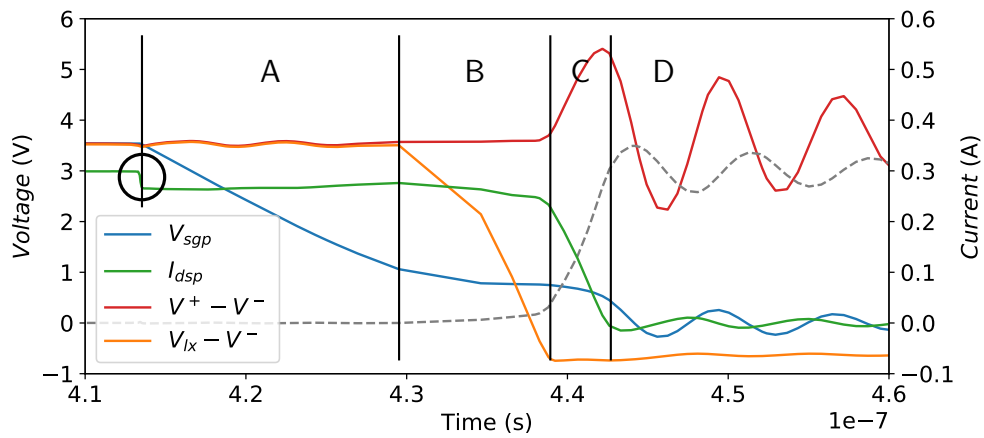
4.1.1 Switching behavior

The switching behavior depends on gate buffers strength. The situations of small and large buffers ($W_{large} = 15W_{slow}$) are presented in Figure 4.1 and Figure 4.2 respectively.

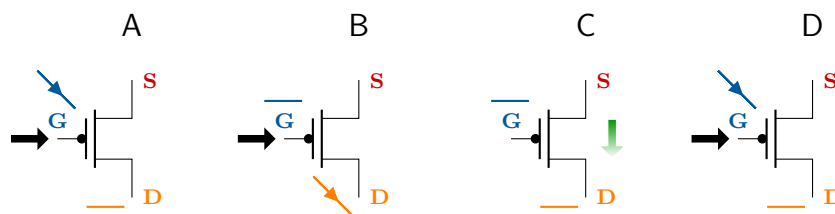
In case of small buffers, the transition ① can sliced in four phases: (A) the gate is charged to $V^+ - V_{th}$ ($V_{sgp} = V_{th}$), (B) the V_{lx} is discharged from V^+ to $V^- - V_{th}$ then (C) the current is switched to NMOS body diode and finally (D) the gate is charged to V^+ ($V_{sgp} = 0$).

During the phase (A) and (B), the current due to the charge and the discharge of the parasitic capacitor I_C flows to the output. In consequence, the current going through the PMOS channel $I_{PMOS} = I_{out} - I_C$ is reduced. The reduction is circled in Figure 4.1a.

In Figure 4.2a, the gate buffers are larger. In consequence, the current of the capacitor discharge provides the entire output current demand, $I_C = I_{out}$. Finally no current remains in PMOS channel, $I_{PMOS} = I_{out} - I_C = 0A$. The path of the I_C is represented in Figure 4.2b.

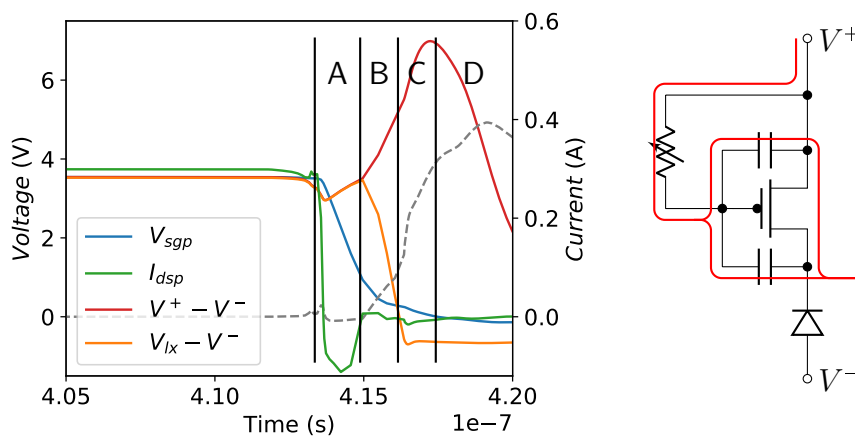


(a)

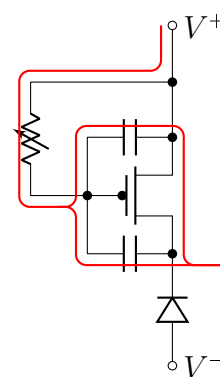


(b)

Figure 4.1 – Simulation results of PMOS turning-off for small buffers



(a)



(b)

Figure 4.2 – Simulation results of PMOS turning-off for large buffers (a) and schematic of current path in the power stage during A, B and C phases (b)

In Figure 4.1 and Figure 4.2, two important differences between the configurations (small buffers and large buffers) can be noticed:

1. the noise generation: an overshoot of the supply voltage $V^+ - V^-$ of $3.4V$ with large buffers in opposite to $1.8V$ with the small buffers,
2. the switching time: in case of small buffers the switching time is equal to $40ns$ versus only $4ns$ for the fast buffer configuration.

The fluctuation of the supply voltage is an issue in term of noise but also in term of stress of the MOSFET. The MOSFET of the STMicroelectronics $40nm$ technology are degraded by frequent over-voltage on their terminals. When PMOS is turned-off its gate and its source are at V^+ and its drain is at $V^- - V_{th}$ so in case of large buffer configuration the voltage difference is $7.5V$.

The switching time impacts the power losses during the transition but also the maximum duty cycle the system can reach. For a buck converter with a switching frequency of $F_{clk} = 2.4MHz$, a switching time of $40ns$ consumes 10% of the period duration in only one of the four transitions. In consequence, the driver sizing is a deal between switching speed and overshoot generation.

The solution exposed in the next section, tries to take advantage of the two configurations.

4.1.2 Solution mechanism

The current in NMOS I_{dsn} is represented in dashed gray line in Figure 4.1 and 4.2. During I_{dsn} rise, the current I^- in the parasitic ground inductance L^- increases in contrary to I^+ . The supply voltage $V^+ - V^-$ fluctuates due to the current switching slope as presented in (4.1). The equation is detailed in section 2.1.2.

$$V^+ - V^- = V_{in} - (L^+ - L^-) \frac{dI^+}{dt} \quad (4.1)$$

The objective is to control the slope of the current switching. In case of slow buffers, part of the current remains in PMOS channel during the transition. So the current slope can be modified by controlling the PMOS gate voltage. The proposed solution is to reduce buffer speed during the change of the current path.

The V_{lx} signal is used as a trigger to reduce buffer speed because V_{lx} voltage drops before that the current switches (see Figure 4.3). Then the buffer is turned-on when no current remains in PMOS channel to finish the transition properly.

The solution mechanism has been exposed, the implementation at MOSFET level can be detailed.

4.1.3 Solution implementation

The schematic of the implemented solution is presented in Figure 4.4. The two large MOSFETs represent the power MOSFETs. The signals Cmd_N and Cmd_P are generated by the system control which is not represented here. There is a dead-time between these two signals to avoid cross-conduction of

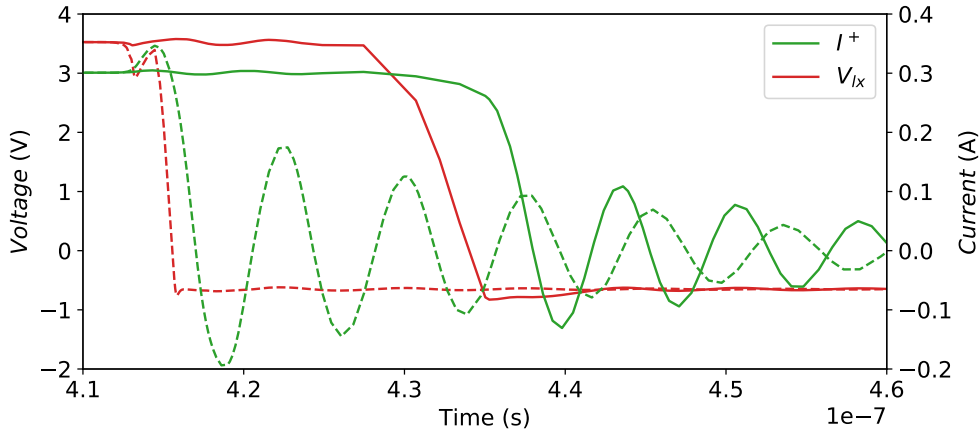


Figure 4.3 – Comparison of I^+ and V_{lx} falls for small buffers (solid lines) and large buffers (dashed lines)

the power MOSFETs. The signals are buffered to control the gate of the power MOSFETs.

The last stage of the buffer of the PMOS gate is represented separately by M_3 and M_4 . M_3 is a small MOSFET which represents the slow buffer configuration. M_3 can be shorted by M_2 , a larger MOSFET, in fast buffer configuration ($\frac{W_{M2}}{W_{M3}} = 50$ with $W_{M2} = 117\mu m$). The gate of M_2 is equal to $smooth = Cmd_P \cdot (V_{lx} + Gate_P)$. The "or-nand" gate is customized to be large enough to drive M_2 gate. The "or-nand" gate is instantiated at the end of the buffer chain to react quickly to V_{lx} drop (no propagation delay).

Finally M_1 is a small copy of the power PMOS. When $Gate_P$ goes over $V^+ - V_{th}$, M_1 channel conduction is stopped and the resistor R pulls-up the $Gate_{sense}$ signal.

A time chart is represented in Figure 4.5.

During transition ①, Cmd_N is set to V^- and Cmd_P is switched from V^- to V^+ . $Gate_P$ initially at V^- starts rising driven by M_2 and M_3 (fast buffer configuration). When $Gate_P$ approaches $V^+ - V_{th}$, V_{lx} drops from V^+ to $V^- - V_{th}$. The drop turns-off M_2 ($smooth$ signal at V^+) and the gate charging slows down. The current I_{out} is switched from PMOS channel to NMOS body diode in slow buffer configuration. When the PMOS channel is opened, $Gate_{sense}$ signal rises to V^+ and turns-on M_2 to finish the transition properly.

The implementation of the solution has been detailed, the simulation and the characterization can be presented.

4.1.4 Simulation results

The simulation results of the system for $V_{in} = 3.6V$ and $I_{out} = 0.3A$ with and without the proposed solution are represented in Figure 4.6.

The undershoot is reduced of $178mA$ and the switching duration is increased of $3.7ns$.

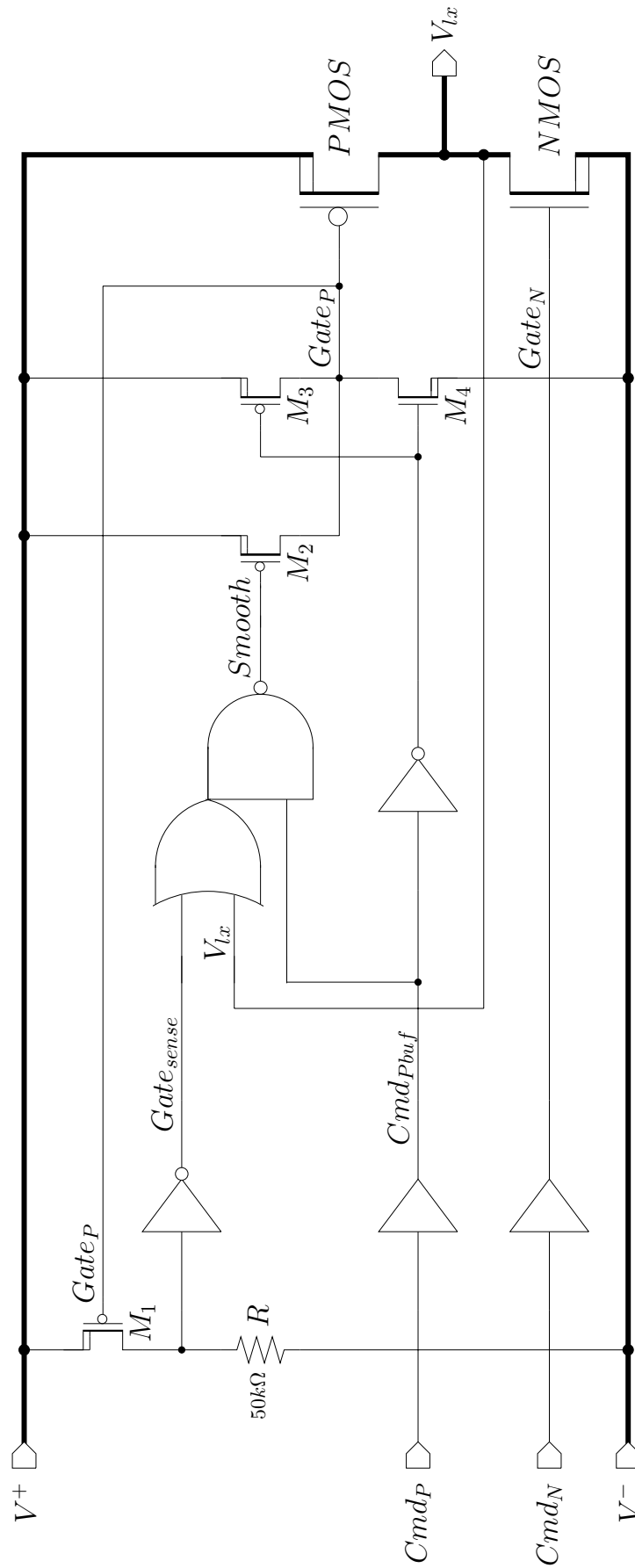


Figure 4.4 – Schematic of the smooth current switching solution

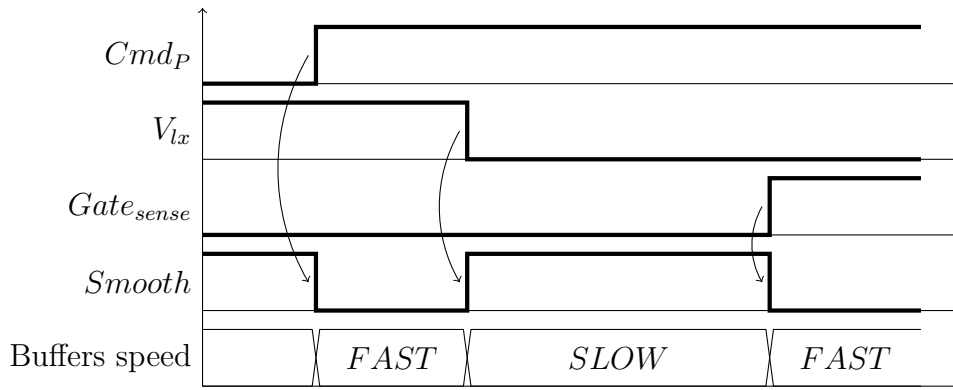


Figure 4.5 – Time chart of the signals of the smooth current switching solution

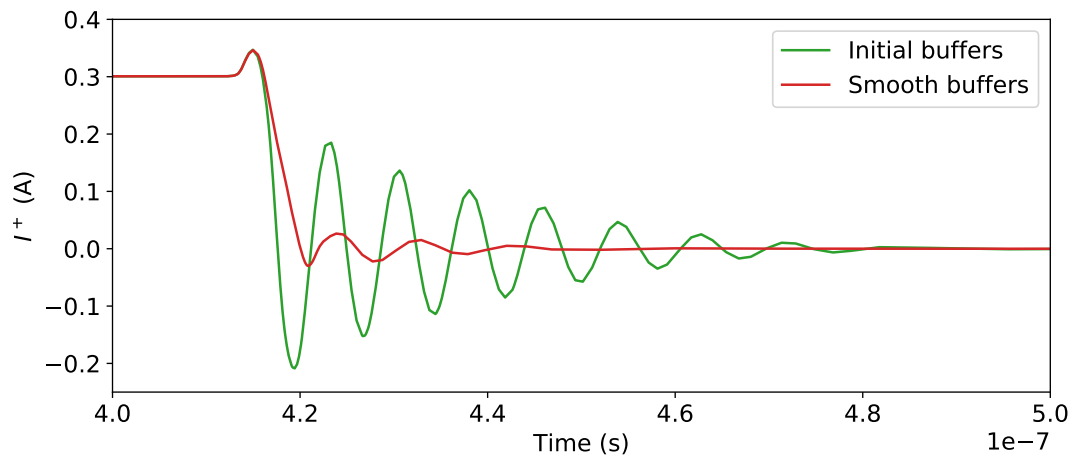


Figure 4.6 – Comparison of I^+ current at PMOS turning-off ① for $V_{in} = 3.6V$ and $I_{out} = 0.3A$ between initial buffers (red) and smooth buffers (green)

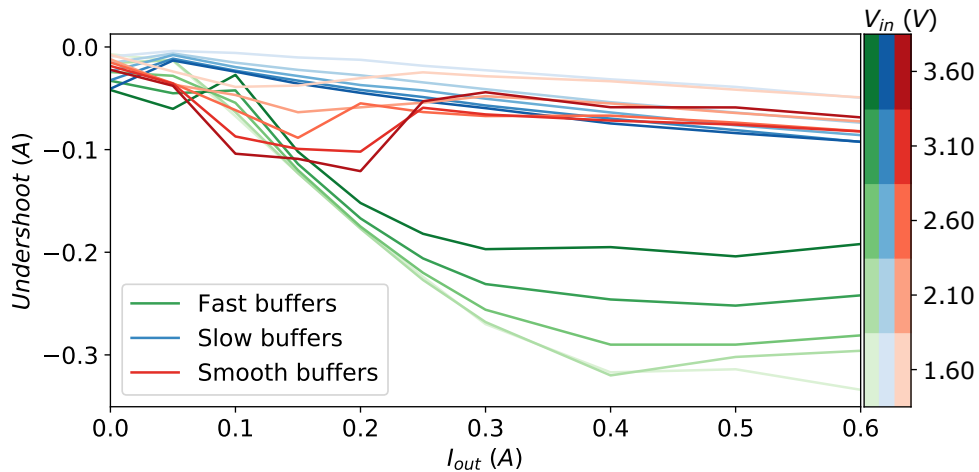


Figure 4.7 – Comparison of I^+ current undershoot between initial buffers (green), slow buffers (blue) and smooth buffers (red)

Is the solution working in any use case? The undershoot and the switching time are extracted from time simulation of the system for,

$$\begin{aligned} V_{in} &\in \{1.6, 2.1, 2.6, 3.1, 3.6\}V \\ I_{out} &\in \{0, 0.05, 0.1, 0.15, 0.2, 0.25, 0.3, 0.4, 0.5, 0.6\}A \end{aligned} \quad (4.2)$$

The results are presented in Figure 4.7 and Figure 4.7 for fast, slow and smooth buffer configuration. The fast buffers corresponds to the initial configuration of the test vehicle i.e. M_2 is used to switched the gate to V^+ . The slow buffers corresponds to the smooth time of the solution i.e. only M_3 is used.

The maximum value of the undershoot is decreased of $159mA$ between the fast buffer configuration and the smooth buffer configuration but at an output current of $I_{out} = 0.1A$, the solution is noisier than the fast buffer configuration. Above $I_{out} = 0.25A$, the undershoot of the smooth solution is reduced to a similar level than the slow buffer configuration.

The maximum value of the switching time is increased of $19.7ns$ between the fast buffer configuration and the smooth buffer configuration. Whereas in slow buffer configuration the switching time is $107.6ns$ slower than the fast buffer configuration. The switching time of the solution represents 6% whereas the switching time of the slow buffer 27% of the period length $\frac{1}{F_{clk}} = \frac{1}{2.4e6} \approx 417ns$.

Why the solution does not work at $I_{out} = 0.1A$? The time simulation results of the system for $V_{in} = 3.6V$ and $I_{out} = 0.1A$ is presented in Figure 4.9.

The large buffers are switched-off during a very short time (less than $1ns$). This glitch creates a current demand of the buffer what increases I^+ oscillations.

A delay is added on $Gate_{sense}$ signal to enlarge the time duration of the slow buffer configuration. The results for a delay of $\{0ns, 2ns, 5ns\}$ are presented in Figure 4.10. For clarity reasons, the surface between the best case and the worst case in term of supply voltage level has been colorized.

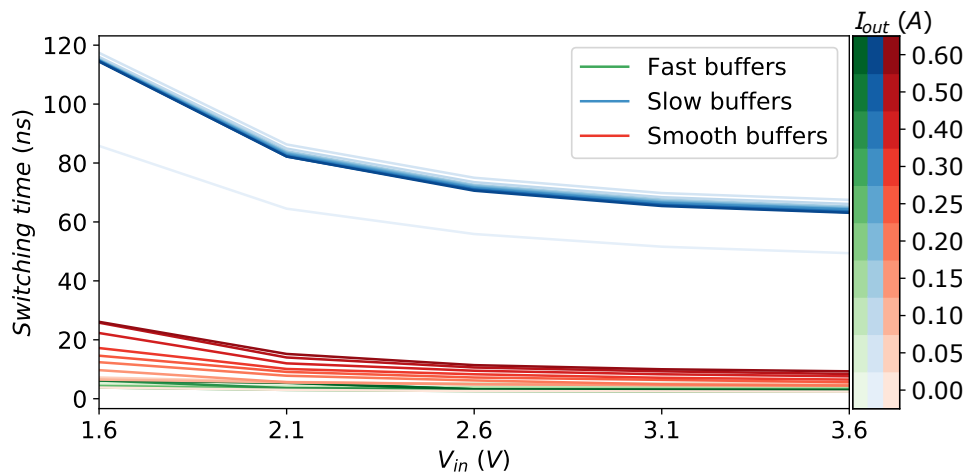


Figure 4.8 – Comparison of I^+ current switching time between initial buffers (green), slow buffers (blue) and smooth buffers (red)

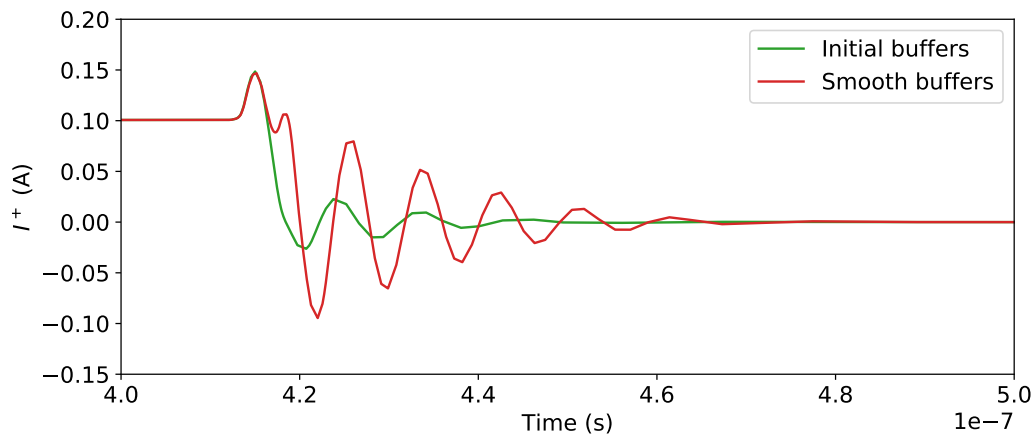


Figure 4.9 – Comparison of I^+ current at PMOS turning-off ① for $V_{in} = 3.6V$ and $I_{out} = 0.1A$ between initial buffers (red) and smooth buffers (green)

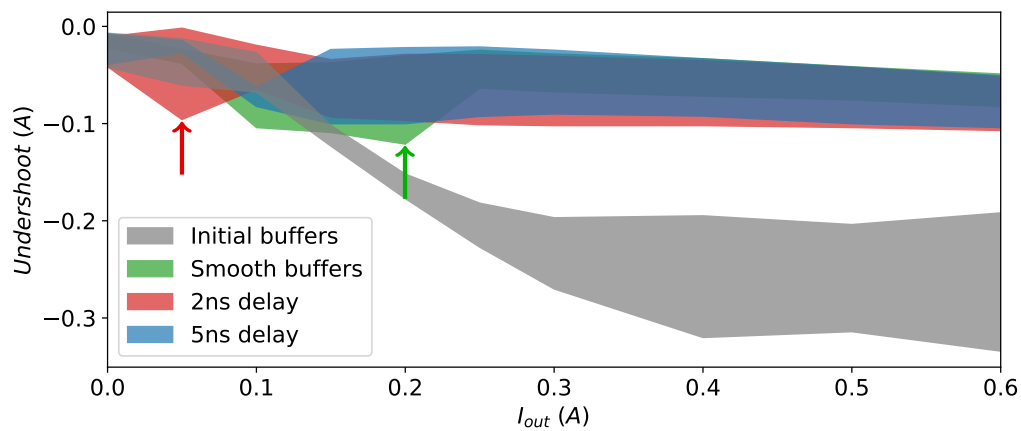


Figure 4.10 – Comparison of I^+ current undershoot between different delays on $Gate_{sense}$ signal

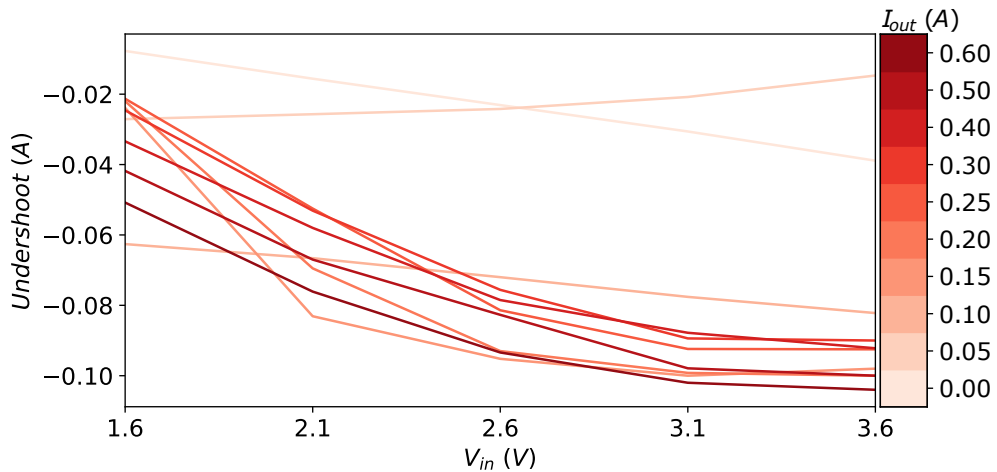


Figure 4.11 – Undershoot variation of I^+ current versus V_{in} (with $5ns$ delay)

The maximum undershoot is reduced and moved to lower current when the delay is increased. With a delay of $5ns$, the undershoot is identical to the initial buffer configuration at output low current (below $0.1A$) and the undershoot is largely reduced at high output current.

This work-around seems to solve the issue at $0.1A$ at a price of an increase in the switching time of $5ns$.

With the solution the undershoot is proportional to V_{in} as presented in Figure 4.11. At low I_{out} ($0A$ and $0.05A$), the extracted undershoot dependency is unclear. The undershoots are impacted by the charge injection of the MOSFET switching. A mechanism similar to PMOS and NMOS turning-on ② and ④.

In consequence, the noise of transition ① becomes dependent of V_{in} as the noise of transition ②. The combination of the two transitions is not exposed here but can be good improvement to cancel noise ringing of one transition with the noise ringing of the second.

The delay on $Gate_{sense}$ signal can be done by adding a capacitor in parallel of R in the schematic of Figure 4.4.

The delay is large in comparison with the time between V_{lx} drop and the $Gate_{sense}$ rising. A simple delay on V_{lx} node should replace the delayed $Gate_{sense}$ signal. This improvement is not tested in the current work but may simplify the structure of the solution.

How do the switching losses vary? The simulation results of the energy losses in PMOS turning-off are presented in Figure 4.12.

The gate discharging is done in fast mode (see Figure 4.5) so at low output current $I_{out} < 0.2A$, the switching losses are equivalent to fast buffer configuration. The current switch from PMOS to NMOS channel is done in slow mode so the switching losses rises in the same way as the slow buffer configuration.

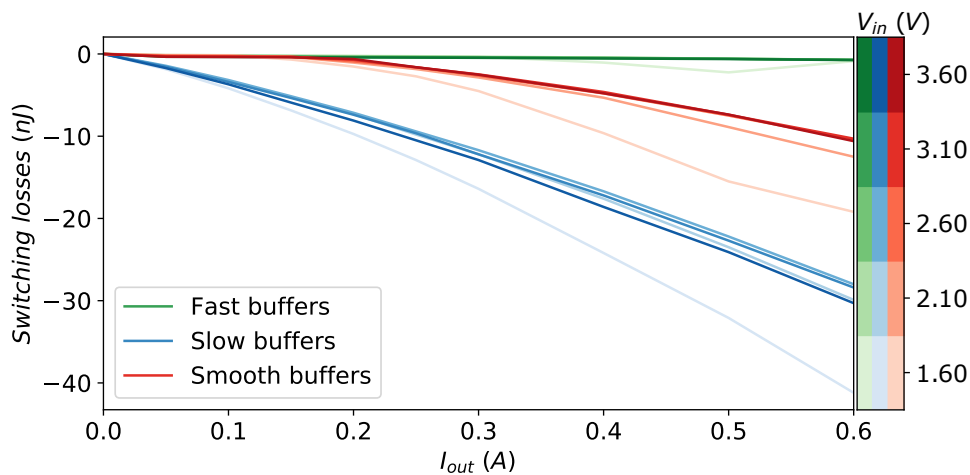


Figure 4.12 – Comparison of switching losses between initial buffers (green), slow buffers (blue) and smooth buffers (red)

Does the process and the temperature variability impact performances? The solution is tested in different "corners". For temperature, the considering range is $T \in [-40^{\circ}\text{C}, 125^{\circ}\text{C}]$ and the two considering process corners are *FFA* and *SSA*. The maximum undershoot is recorded and compared to the results of Figure 4.10. The added delay is not actually implemented at MOSFET level, in consequence the process variation does not impact the delay length. The results are presented in Figure 4.13.



The "corners" represents possible variations of the process and of the temperature. A simulation is done in every "corners" which means for the temperature that each simulation are done at $T = -40^{\circ}\text{C}$ and at $T = 125^{\circ}\text{C}$. The two considering process corners are *FFA* and *SSA* which mean *Fast PMOS Fast NMOS Analog* and *Slow PMOS Slow NMOS Analog*. Due to the large production volume, the circuits are designed to match the specification even with these tiny variations. In analog design, the variations can largely impact characteristic of a circuit.

The process and the temperature variations do not impact significantly the performance of the circuit.

This solution (without delay) was implemented in test vehicle similar to the circuit used for characterization of the models in chapter 3. The chip was processed in STMicroelectronics Crolles site. The circuit is under debugging.

4.2 Injection from a capacitor

The second proposed solution is focused on PMOS turning-on ④. As explained in section 3.1.6, the overshoot is due to current inrush during gate discharge so the overshoot depends on V_{in} . To understand the solution mech-

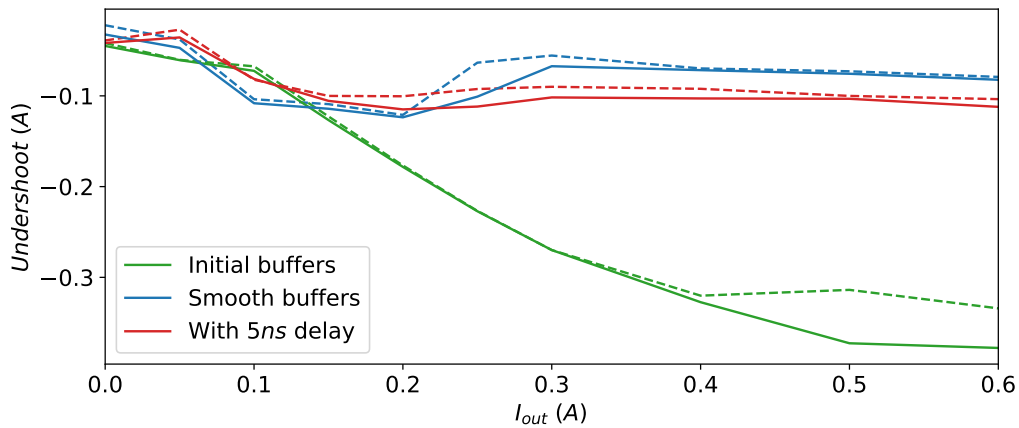


Figure 4.13 – Comparison of I^+ current undershoot between initial buffers (green), smooth buffers (blue) and with $5ns$ delay (red) in worst case (solid line) versus typical case (dashed line) in term of process variation, temperature and current

anism a brief wrap-up on this transition is important.

4.2.1 Switching behavior

The simulation results of the PMOS turning-on ④ are presented in Figure 4.14.

The transition is composed of four phases: the PMOS gate is discharged to $V^+ - V_{th}$ ($V_{sgp} = V_{th}$) (A), then the current rises in the PMOS channel up to I_{out} (B), after that no current flows through NMOS body diode so the V_{lx} increases to V^+ and finally the gate is discharged to V^- (D).

The latter phase (D) generates a current inrush to charge the gate capacitance creating an overshoot on I^+ .

4.2.2 Solution mechanism

The objective is to create a charge tank on-chip which supplies gate during switching and refill slowly during the rest of the period.

A first solution is to add decoupling capacitor on-chip but to be efficient this capacitor has to be large in comparison to the PMOS gate capacitance. Due to the large size of the PMOS, its gate capacitance is $\sim 200pF$. A capacitor significantly larger than $200pF$ requires a large silicon area which is costly.



The MOS capacitor density is three times the gate capacitance density of MOSFET in the $40nm$ technology. For a MOSFET with a surface S and a gate capacitance C_g , a MOS capacitor of $\frac{1}{3}S$ is needed to achieve the same capacitance value C_g . Other capacitance structures with a higher density exist but are not available in this technology.

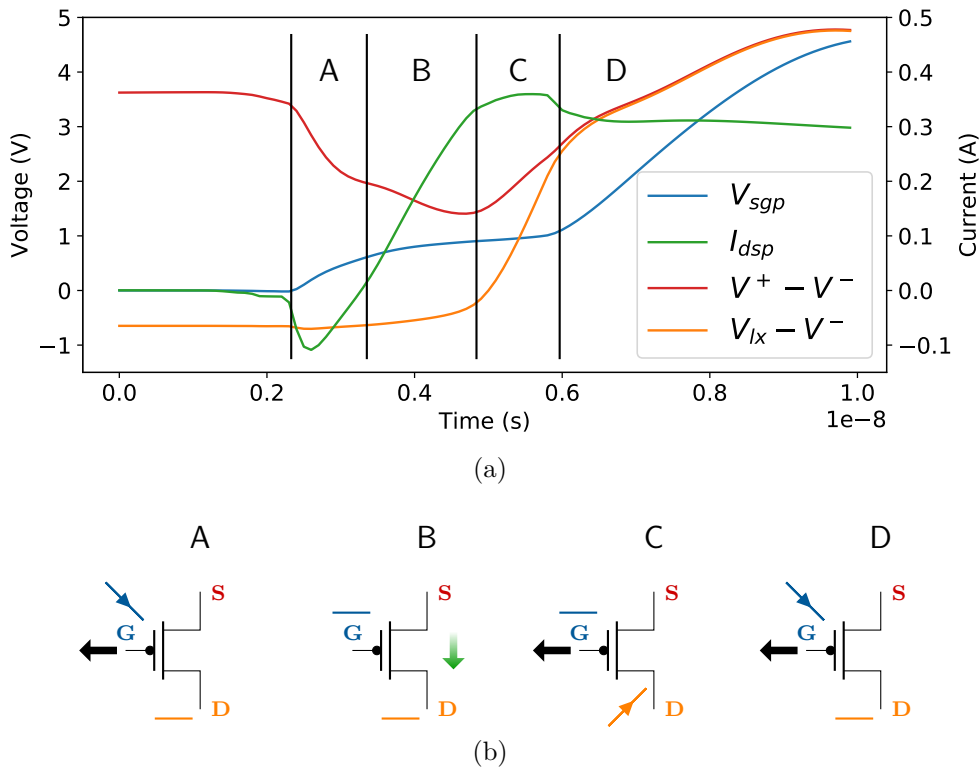


Figure 4.14 – Simulation results for PMOS turning-on ④

A second solution is a switched-capacitor structure. The capacitor is discharged on gate during the transition and refills slowly during the rest of the period as presented in Figure 4.15. The buffer discharges PMOS gate of V_{th} and V_{ix} increases to V^+ (Figure 4.15a). Charges are injected on gate (Figure 4.15b). The buffers finish to discharge the gate and the refill of the capacitor is starting slowly (Figure 4.15c).

The charge in the PMOS Q_{MOS} and in the switched-capacitor Q_{SC} are,

$$Q_{MOS} = 2C_g(V^+ - (V^+ - V_{th})) = 2C_gV_{th} \quad (4.3)$$

$$Q_{SC} = C_i(V^+ - V^-) \quad (4.4)$$

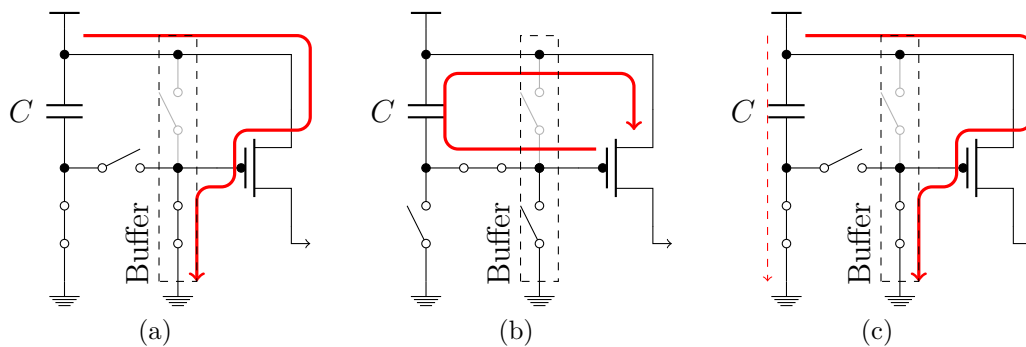


Figure 4.15 – Outline schematics of the switched-capacitor structure

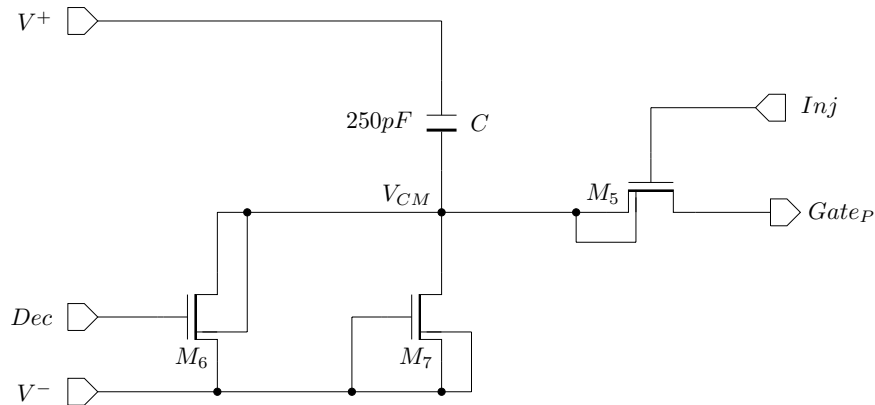


Figure 4.16 – Schematic of the charge injection solution

At the end of the injection phase, the charge is dispatched between each capacitance so V_{sgp} is,

$$V_{sgp} = \frac{Q_{MOS} + Q_{SC}}{2C_g + C_i} = \frac{2C_g V_{th} + C_i(V^+ - V^-)}{2C_g + C_i} \quad (4.5)$$

In consequence with a switched-capacitor $C_i = 2C_g \approx 200pF$, the gate voltage $V_{sgp} = \frac{1}{2}(V_{th} + V^+ - V^-)$. So half of the charge needed for the switching has been injected.

During the injection the gate and the switch-capacitor are disconnected from the supply. There is no current inrush to refill quickly the switch-capacitor. Then this capacitor is reconnected to the supply by a large resistor to reduce current inrush. The solution may be considered as a variable damping resistor on a decoupling capacitor: when the system needs charge the resistance is low to respond quickly to the demand but to refill the capacitor, the resistance is bigger to limit the current demand.

4.2.3 Solution implementation

The schematic of the solution is represented in Figure 4.16.

A time chart of the two signal Dec and Inj is represented in Figure 4.17.

The signal Dec is turned-off with Cmd_P to avoid capacitor discharging due to supply variation before the injection. The buffer discharged gate to $V^+ - V_{th}$ (A) and the current switches to PMOS channel (B) and then the V_{lx} rises to V^+ (C) at this moment the buffer is turned-off and the capacitor is connected to the gate during $T_{inj} = 3ns$ (determined empirically by simulation).

The large fluctuation of the voltage supply activates the MOSFET M_6 . The capacitor is partially discharged during phases (B) and (C). In consequence, just few charge is actually injected and the solution does not reduce noise level more than a simple decoupling capacitor with the same size than switched-capacitor. But during the test of the solution a side-effect canceling the ringing has been observed. Finally the solution is centered on this side-effect presented in Figure 4.18.

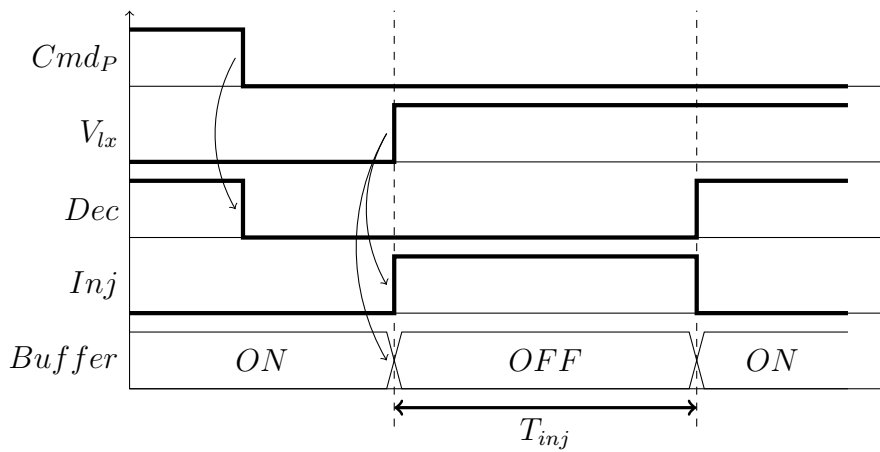


Figure 4.17 – Time chart of the signals of the switched-capacitor solution

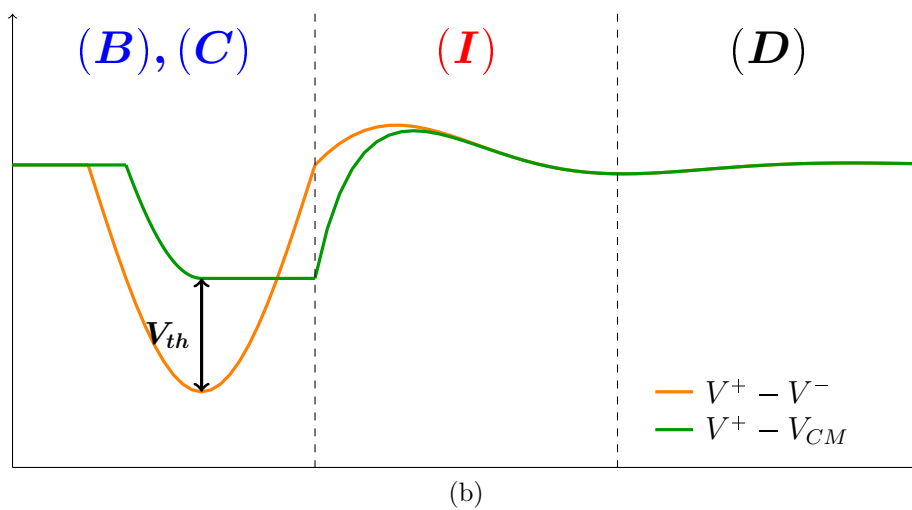
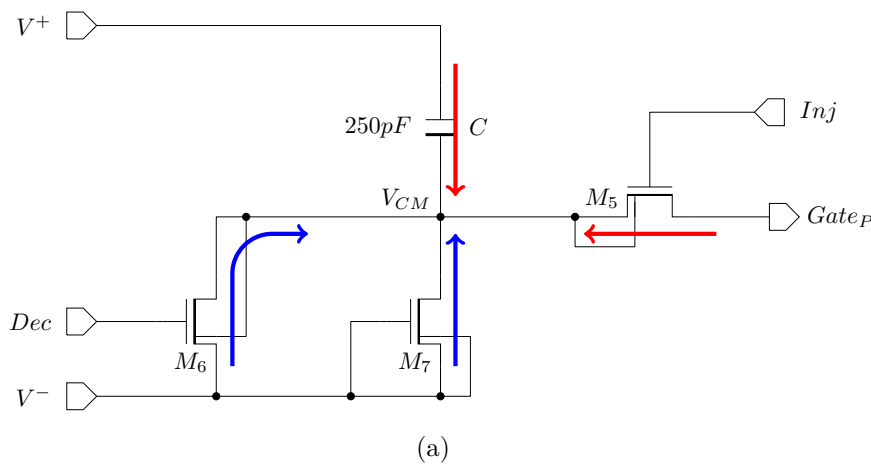


Figure 4.18 – Schematic of the charge injection solution (a) and ringing cancellation explanation (b)

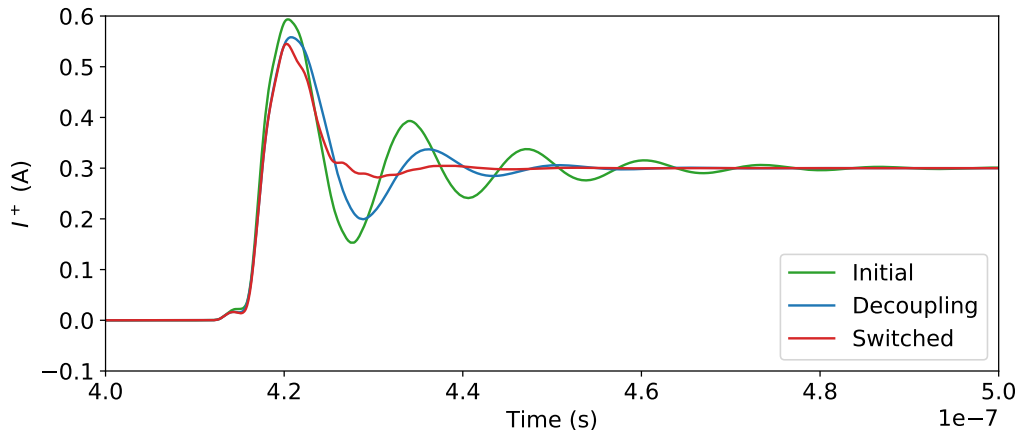


Figure 4.19 – Comparison of time simulation results of I^+ current between initial buffers (red), with a decoupling capacitors (blue) and with switched-capacitor structure (green) for $V_{in} = 3.6V$ and $I_{out} = 0.3A$

At Cmd_P falls, the signal Dec is set to V^- so the two MOSFETs M_6 and M_7 work as diode (with threshold voltage of V_{th}). The PMOS gate is discharging by the buffer. Due to supply voltage fluctuations, the capacitor C is discharged during phase (B) and (C) (arrows in blue). Then on V_{lx} rise, the buffer is turned-off but the signals Dec and Inj are turned-on for a fixed time ($3ns$). This phase is called (I) in the Figure 4.18. The excess of charge due to the current inrush is used to refill the capacitor C and to discharge PMOS gate (arrows in red). The charge demand in phase with current overshoot absorbs the excess and cancels the ringing. Finally the buffer is turned-on and the signal Inj is turned-off to finish to discharge the PMOS gate (D).

This new solution is presented, but needs to be confirmed by a characterization. The next section exposes the simulation results.

4.2.4 Simulation results

The time simulation results for $V_{in} = 3.6V$ and $I_{out} = 0.3A$ are presented in Figure 4.19.

The overshoot with the switched-capacitor structure is similar to the overshoot with just the decoupling capacitor but the oscillations are canceled. The system is tested in variable operating conditions of the equation (4.2). The results in term of overshoot is presented in Figure 4.20a. The undershoot is extracted in the different conditions to illustrate the ringing cancellation. The extraction results are presented in Figure 4.20b.

The overshoot is not significantly reduced by the solution in comparison to the initial buffers configuration and the decoupling capacitor. This overshoot is proportional to V_{in} as presented in section 4.2.1.

The ringing cancellation is working in every current condition except for $I_{out} = 0A$ where the extracted overshoot is similar to the buffers with a decoupling capacitor configuration. Especially at $V_{in} = 3.6V$, the ringing is reduced by 78% compared to the initial buffers and by 72% compared to the buffers

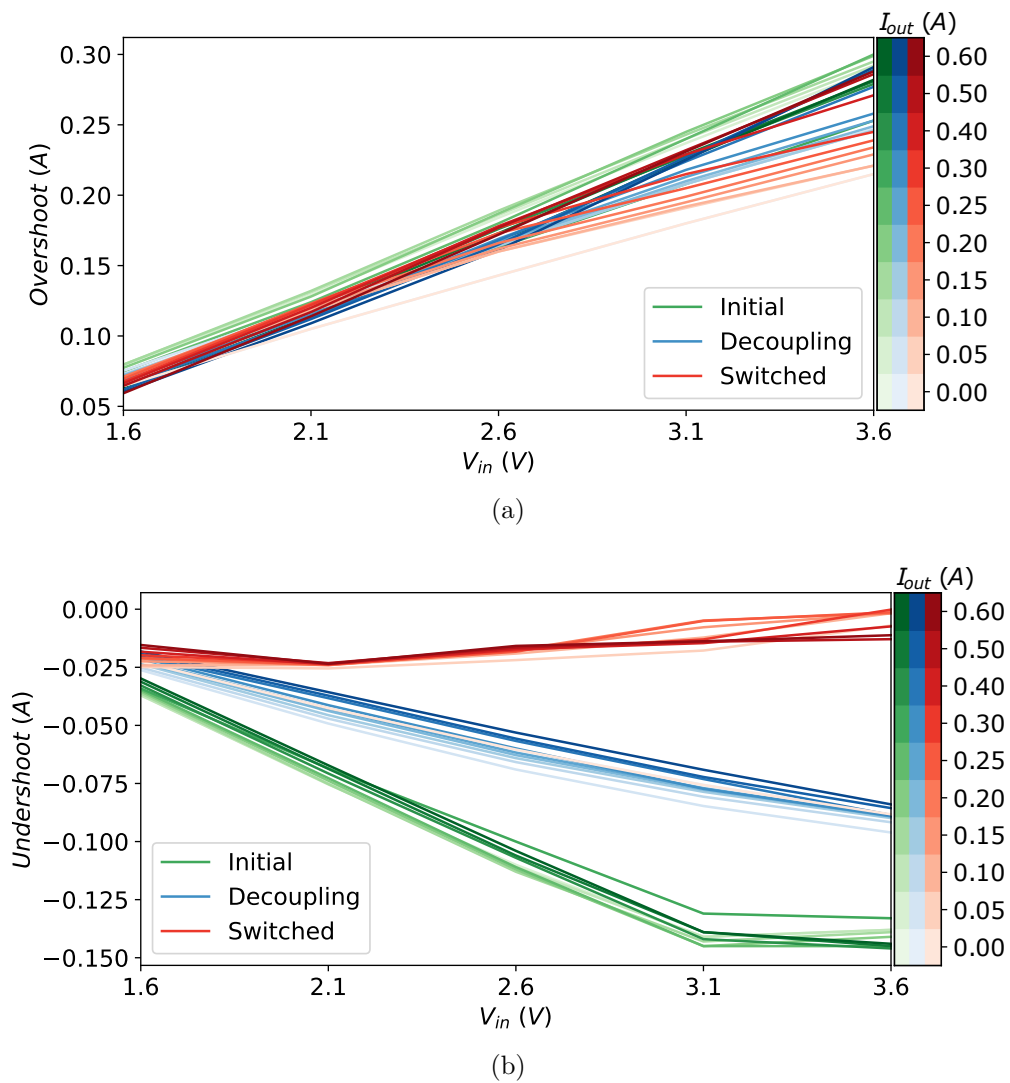


Figure 4.20 – Comparison of I^+ current overshoot (a) and undershoot (b) during PMOS turning-on ④ between initial buffers (red), with a decoupling capacitors (blue) and with switched-capacitor structure (green)

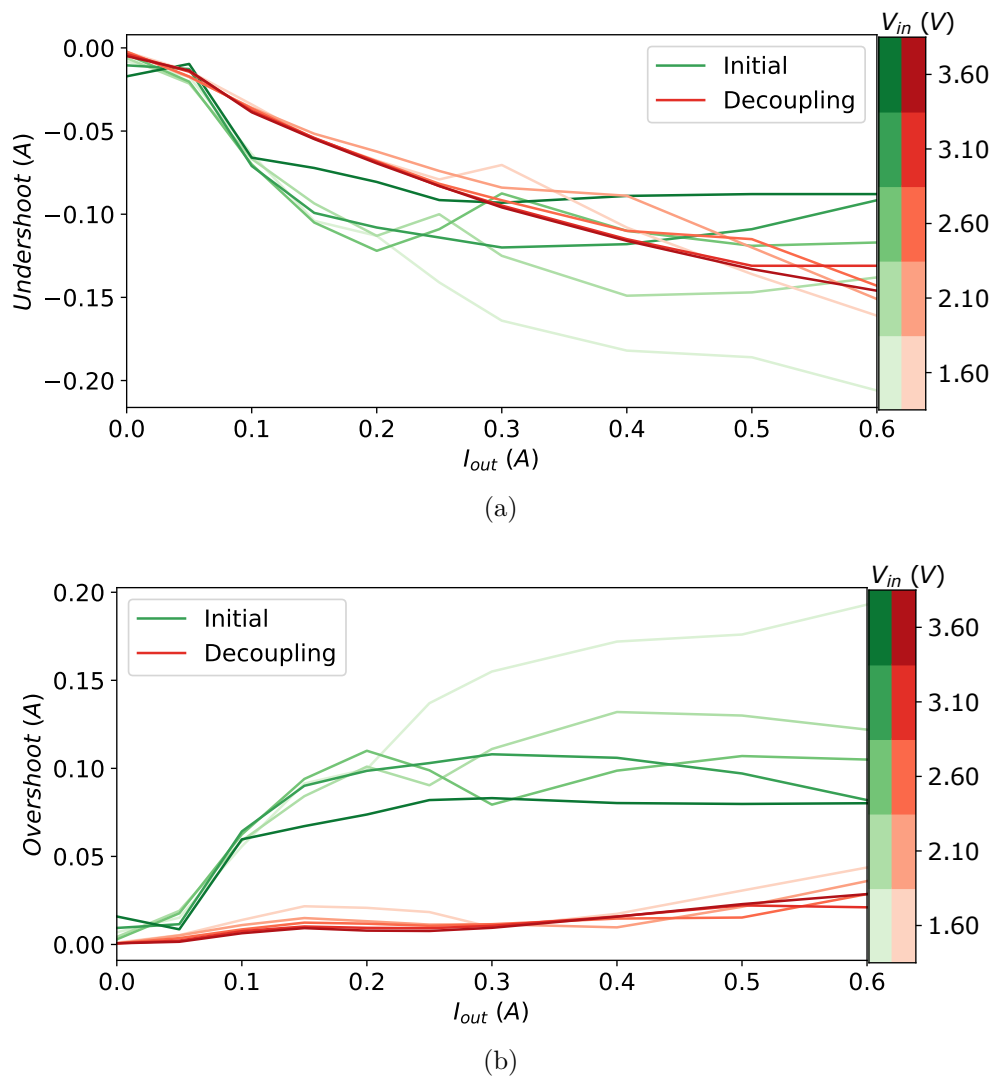


Figure 4.21 – Comparison of I^+ current undershoot (a) and overshoot (b) during PMOS turning-off ① between initial buffers (red), with a decoupling capacitors (green)

with a decoupling capacitor.

The present system works as a decoupling capacitor during the other transitions. The decoupling capacitance reduces significantly the noise of PMOS turning-off ①. This improvement is presented in Figure 4.21. The undershoot is not really impacted due to the damping resistor in series with the decoupling capacitor limiting the speed of the capacitor discharge but the attenuation of the ringing is increased. The damping resistor is chosen to minimize impedance of the supply network. Its value is fixed to 10Ω .

In term of power efficiency, only the ringing is impacted by the solution: the transition behavior is similar to initial buffer. The simulation results extraction present a variation of 1% on the switching losses (plus or minus depending on the case) what does not impact significantly the efficiency.

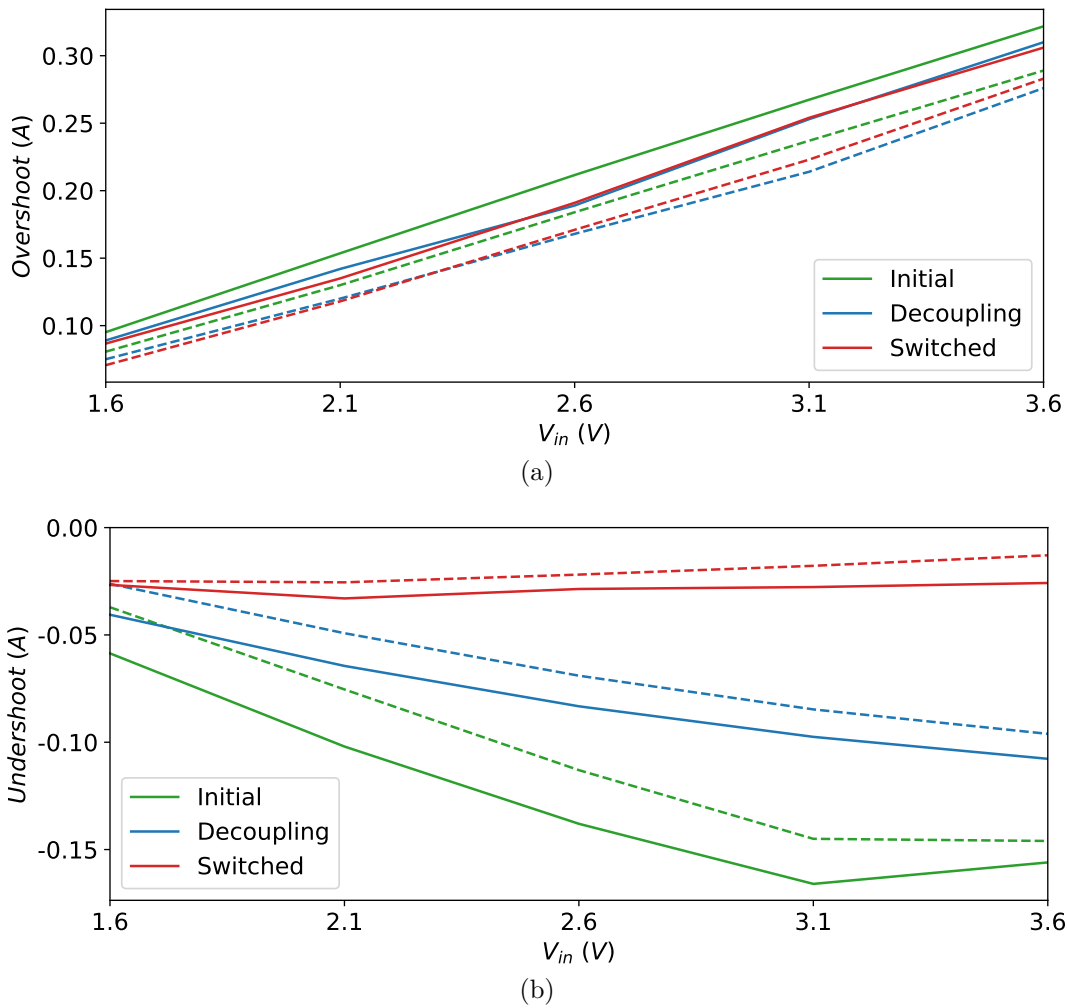


Figure 4.22 – Comparison of I^+ current overshoot (a) and undershoot (b) during PMOS turning-on ④ in worst case (solid line) versus typical case (dashed line) in term of process variation, temperature and current (except 0A)

Impact of the process and the temperature variability

The solution is tested at a temperature of $T = -40^\circ\text{C}$ and $T = 125^\circ\text{C}$ and in corners FFA and SSA but also C_{min} and C_{max} to evaluate the impact of the switched capacitor variation. The maximum overshoot and undershoot are recorded and compared to the results of Figure 4.20. The delay T_{inj} is not actually implemented at MOSFET level, in consequence the process variation does not impact the delay length. The results are presented in Figure 4.22.

The undershoots are impacted by the process and temperature variation but relatively to the initial buffers and to the configuration with decoupling capacitor, the performances are not degraded.

The solution reduced efficiently the current ringing and could be applied to other transitions especially to NMOS turning-on ② whose behavior is similar to PMOS turning-on ④.

Solutions to reduce noise emission has been exposed, the next section solution work on on-chip propagation paths.

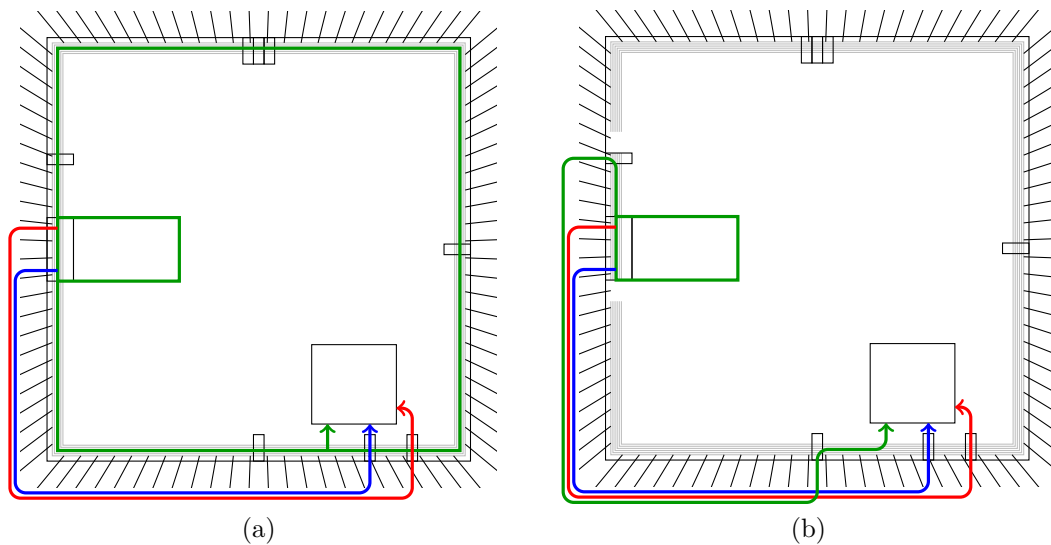


Figure 4.23 – Top view of the chip with continuous (a) and discontinuous (b) I/O ring

4.3 Reduction of internal paths

The objective of the solution is to reduce on-chip propagation paths. The path impedance between the source and the victim must be higher than the impedance to the PCB ground plane to evacuate noise outside the chip through the ground instead of polluting the victim.

4.3.1 Solution mechanism

As exposed in section 3.6.4, the main on-chip propagation path is the I/O ring. A top view of the chip with the propagation paths is presented in Figure 4.23. The red and the blue arrow represents the propagation of noise through supply and ground interconnections. These two paths are external: the noise is going through the PCB to reach the victim cell. The green path is interconnected all around the chip by the I/O ring to bias the substrate. The propagation of substrate noise is facilitated by these metal interconnections.

The natural solution is to cut the I/O ring near the source of noise to isolate that part of the substrate biasing network from the rest of the circuit. Well, by isolating the buck converter substrate, the biasing is not guaranteed so the voltage may be locally different and the junction with the substrate may be activated. In consequence, a dedicated pin for buck converter substrate biasing is needed. The solution is represented in Figure 4.23b.

The solution has been implemented in layout. The circuit simulation results are presented in the next section.

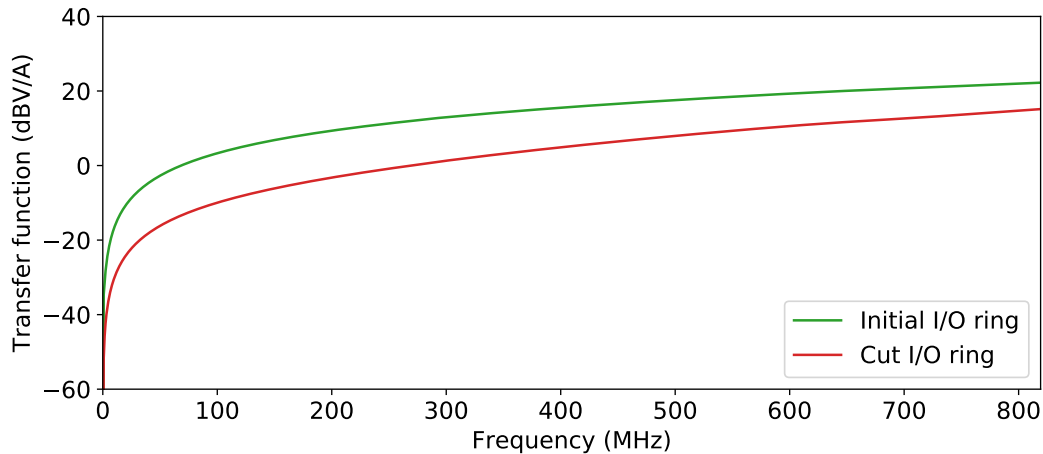


Figure 4.24 – Transfer function between substrate pins of the buck converter and the voltage reference w/o I/O ring cut

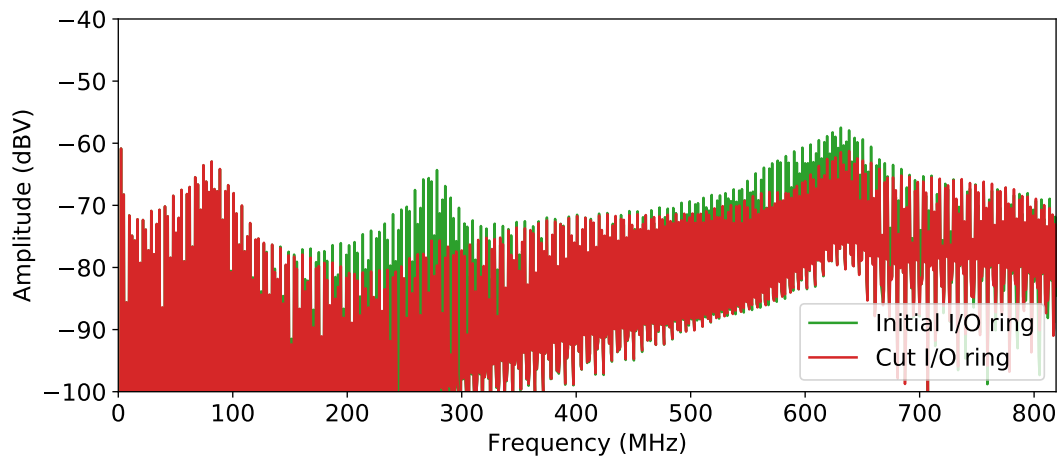


Figure 4.25 – Simulation results of noise amplitude on the voltage reference w/o I/O ring cut

4.3.2 Simulation results

The simulation has been done using *WaveIntegrity* tool from CWS. The setup of the simulation is detailed in section 3.6.

The comparison between the transfer function from substrate pin of the buck converter (the source) to the substrate pin of the voltage reference (the victim) with I/O ring and with the cut proposed in Figure 4.23b is presented in Figure 4.24.

The cut in the I/O ring reduces the transfer function between the two substrate pins. At substrate resonance frequency ($\sim 640MHz$), the transfer function is reduced of $-8.5dB$. The noise spectrum of the voltage reference output is presented in Figure 4.25.

The noise amplitude at the path resonance frequency ($278MHz$) almost disappeared ($-15.3dB$). The noise amplitude at the substrate resonance frequency is reduced of $-3.9dB$. The amplitude at the gate resonance frequency ($94MHz$) does not change. Moreover the noise floor remains the same.

The noise at low frequency is propagating through the PCB so a change on-chip does not affect the noise contribution. At higher frequency, the PCB connection impedances are larger (parasitic inductance) and the noise is propagating on-chip so the transfer function reduction due to the cut in I/O ring is more effective.

The solution of internal transfer function reduction has been exposed, a last solution is investigated in the next section.

4.4 Other investigation

Solutions exist at PCB level to filter noise but, in the micro-controller context, only advices on components placement can be given to the customer. Lots of studies have been made about PCB filtering and presented in literature. An overview of the state of the art is given in section 1.3.2.

System solutions are also possible especially different dithering methods to reduce the amplitude of buck converter frequency harmonics. These solutions do not reduce noise energy but spread it in the entire spectrum. This study is focused on the root causes of the noise generation and to reduce its energy so no investigation has been done on the subject. These topics are connected and a study of spreading solution may be an interesting development. Some references about spreading techniques are proposed in section 1.3.4.

A last solution is experimented. The objective is to cancel ringing of the I^+ current. The solution is based on results exposed in [5].

Two inductances are printed on a PCB, one in power loop and the other one in gate-drive. The article presents the impact of the mutual inductance between these two inductors on switching noise.

What are the main differences between the environments of the studies?

4.4.1 Context differences

The power range: the supply voltage is $500V$ and the output current is $20A$ so a power of $10kW$ in comparison to the present work with a maximum output power of $3.6V \times 0.6A = 2.16W$.

The main inductor: the main inductor of [5] is printed on PCB and its value is $255nH$ in comparison to the present work where the inductor is due the package interconnections with a lower value $5.21nH$.

The power stage architecture: the schematic of the power stage of [5] is presented in Figure 4.26.

The switching noise reduction is studied during NMOS turning-off. The gate is discharging, in consequence the channel resistance increases and V_{ds} rises to $E_{in} + V_{th-diode}$. At this time, the current source I_{out} is shorted by the diode and no current is flowing through the NMOS channel and L_{main} .

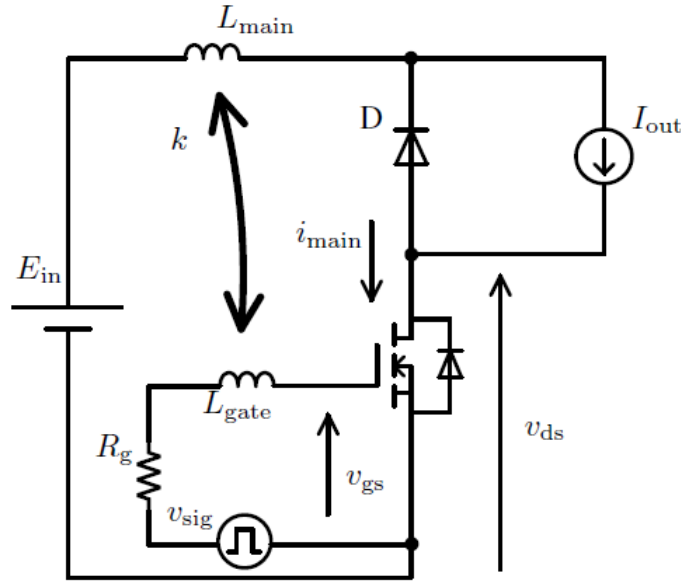


Figure 4.26 – Power stage schematic of [5]

There is a MOSFET turning-off with a change in current path what corresponds to the PMOS turning-off in the present work.

So is it possible to adapt the solution to a low power case ($2.16W \ll 10kW$), to PMOS turning-off and to tiny inductance ($5.21nH \ll 255nH$)?

The schematic, adapted to the present work, is presented in Figure 4.27.

The two large MOSFETs represent the power stage, the triangle symbolizes buffer chain. The mutual inductance is considered between L_G^- and L^- and between L_G^+ and L^+ . The inductance values are simplified for the proof of concept simulations. $L_G^{+-} = \frac{1}{4}L^{+-}$ to respect the ratio of [5].

The solution actually reduces noise, the Figure 4.28 presents the mechanism responsible of ringing attenuation. The four inductances are merged into two, one on the gate, the other one on supply path, for readability. The NMOS buffers are considered to V^- during the transition so the NMOS works as a diode.

The resonant network is composed of two loops with different resonance frequencies. During the switching, the loops are stimulated by different phenomena: I_{out} switching from PMOS channel to NMOS body diode for $L^{+/-}$ and PMOS buffer switching from V^- to V^+ for $L_G^{+/-}$. Depending on the phase difference between oscillations the current ringing can be canceled as presented in Figure 4.29.

The solution is limited by its dependency to parasitic parameters of the power stage. These parameters are dependent of the operating conditions V_{dd} and I_{out} levels. In [5], the operating conditions are fixed: $V_{dd} = 500V$, $I_{out} = 20A$. In consequence, the inductance value can be adjusted to reduce noise in that special context. In the micro-controller environment, the V_{dd} can be freely set to any value in the range $[1.6V, 3.6V]$. Moreover I_{out} at switching time depends on output load especially on digital activity of the micro-controller.

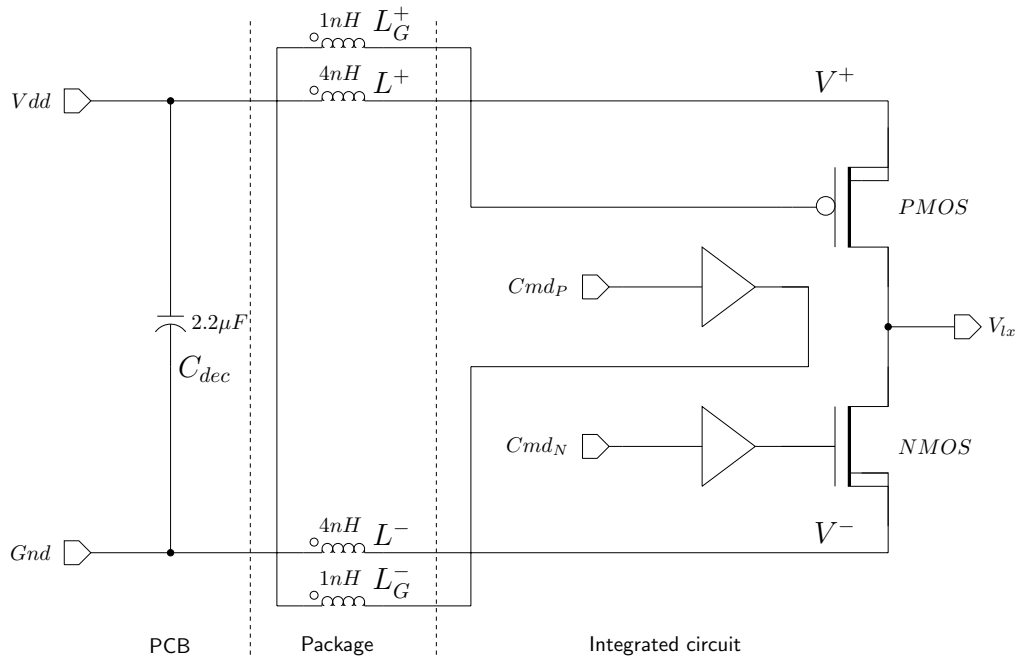


Figure 4.27 – Schematic of the inductive coupling solution

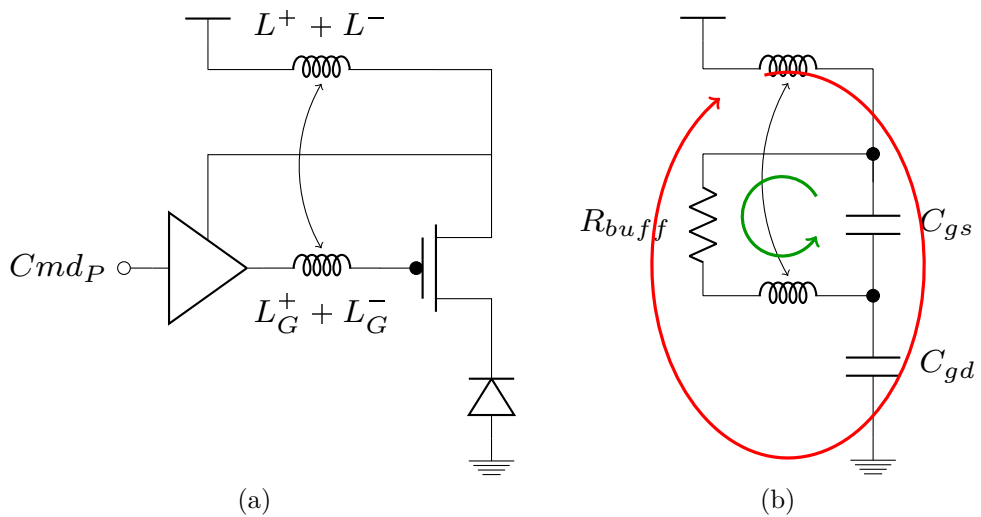


Figure 4.28 – Equivalent schematics of the inductive coupling solution

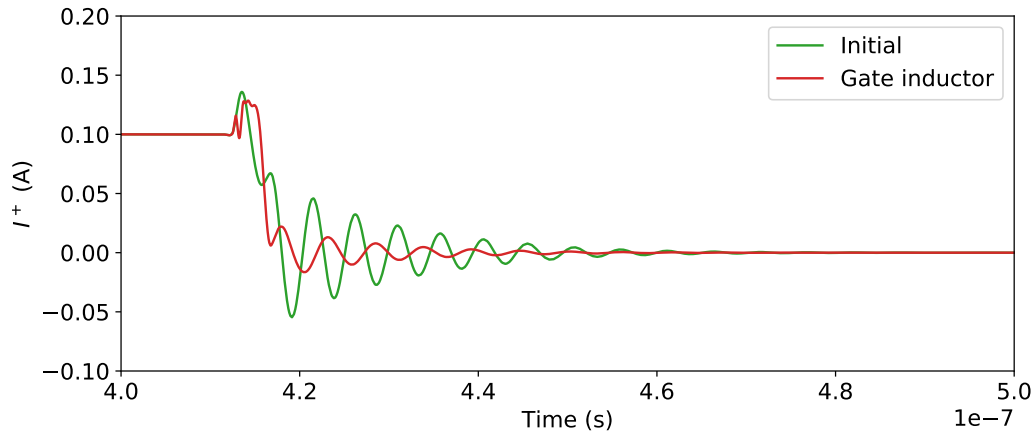


Figure 4.29 – Comparison of time simulation results of I^+ between initial buffers (red) and with gate inductor (green) for $V_{dd} = 3.6V$, $I_{out} = 0.3A$ and $K = 0.5$

Finally the solution cannot be used in the present environment.

The solution may be interesting for a system with fixed supply voltage and a Pulse Frequency Modulation (PFM) control loop. In this configuration, the output current of the power stage always switches at same value.



The Pulse Frequency Modulation (PFM) is a special regulation method. The system always injects identical pulses to charge the output capacitance. The output voltage is regulated by adjusting the frequency of the pulse emission [41].

4.5 Wrap-up of solutions

Three solutions are proposed:

1. To reduce I_{out} switching slope with a variable buffer strength: at PMOS turning-off ①, the gate is discharged with large buffers but the current is switched with small buffers. The noise amplitude is equivalent to the slow buffer configuration but the switching time is largely reduced (about 80% in the present configuration).
2. To reduce charge injection of gate capacitor with a switched-capacitor: the capacitor absorbs the excess of charge due to the ringing of the PMOS turning-on ④. The overshoot is not modified by the solution but the following undershoot is reduced of 70% versus a simple decoupling capacitor and by 80% versus the initial configuration. The decoupling capacitor also reduces the overshoot of PMOS turning-off ①. The solution mechanism could be applied to other transitions especially NMOS turning-on ②.
3. To reduce the propagation of the substrate noise by splitting the I/O ring in two parts, one for the sources and one for the victims. A dedi-

cated substrate biasing for the buck converter reduces the amplitude of the substrate resonance frequency by $-3.9dB$. It also reduces propagation paths resonance.



Finally the solution constraints can be summarized by:

1. small surface - longer switching time - only for PMOS turning-off ①,
2. large surface ($250pF$ capacitor) - same switching time - all the transitions,
3. possibly more I/Os to substrate biasing - reduce substrate crosstalk - high frequency noise.

5 Conclusion

Synthesis

The objective of this work was to analyze the pollution mechanism of a buck converter on sensitive analog IPs integrated in a SoC and to develop minimization techniques to reduce the buck converter noise.

The objective was split in three parts: first to analyze noise generated by the power stage of the buck converter, then to understand by which paths the noise was propagating to the victim and finally based on these results, to implement solutions reducing the generation or the propagation of the noise.

To analyze switching noise of the buck converter means to determine the noise resonance frequency, the noise amplitude and to link these two values to parameters of the buck converter. The power stage and its environment were simplified to a simple RLC. The R, L and C were determined by the parasitic network extraction in each state of the buck converter and the initial conditions of these equivalent schematics were determined by an analysis of the transitions between the states.

The R was mainly due to buffer strength, the L was located in the package and PCB supply and ground interconnections and finally the C was composed of gate capacitances of the two power MOSFETs.

There were four transitions: the PMOS and NMOS turning-on whose overshoots were due to the discharging and charging of the power MOSFET gate capacitances and depended on voltage supply level, the PMOS turning-off whose undershoot was due to current switching from PMOS channel to NMOS channel and depended on output current level and finally the NMOS turning-off whose contribution was negligible in comparison to the contributions of the other transitions.

Another resonance frequency was pointed out: the junction capacitance between buck converter supply and the substrate biasing resonates with the parasitic inductance of the package and the PCB. This parasitic network was stimulated by fluctuations of the supply voltage of the buck converter.

The propagation understanding was achieved in two steps. First the whole system (the entire integrated circuit, the package and the PCB) was modeled using CWS software suite, *WaveIntegrity* and compared with measurements to verify and correct the model. Then the environment of the buck converter was modified in simulation to understand the contribution weight of the different propagation paths.

At low frequency (below $\sim 400MHz$), the noise was mainly propagating

through PCB supply connection and ground plane. The S parameter extraction using ground plane as reference underestimated the propagation of noise through the ground plane. The model was corrected by adding an impedance on the ground plane connection to ideal ground.

At high frequency (above $\sim 400MHz$), the noise was propagating through on-chip interconnections. Due to the high resistivity of the substrate in the technology, noise did not propagate through long distance inside the substrate but was propagating through the I/O ring. The metal layers were low resistive and the package parasitic inductances at that frequency were high impedance avoiding the noise to be evacuated through the ground plane.

Finally solutions to reduce noise impact were investigated. First solutions to decrease noise generation were presented. The buffer strength reduction decreased the noise generated by power MOSFET switching but at a cost of a larger switching time. A solution with a variable buffer strength was experimented permitting to switch the gate voltage quickly but to smooth the current switching from PMOS to NMOS channel. The switching time is reduced in comparison to the small buffer configuration but with an equivalent undershoot amplitude.

Another solution was to add a decoupling capacitor but this solution was limited by surface constraint and the capacitor was not large compared the charge demand of gate capacitance at transitions. A solution permitted to cancel noise ringing. The decoupling capacitor refill was time shifted to absorb the excess of charge due to oscillation of the parasitic network.

A last solution was presented: to reduce the propagation paths. The PCB power distribution network could be optimized but in the micro-controller context, the PCB is designed by the customer so the investigations were focused on internal propagation paths. The presented solution is to have two different biasing networks of the substrate. Due to the high resistivity of the substrate the noise was evacuated through the PCB instead of the internal paths which reduced the impact of this noise on the victim.

Perspectives

A test vehicle has been designed and send to foundry with the buck converter, a voltage reference and an ADC. First an open-loop configuration has been implemented to separate transitions, especially PMOS turning-off from NMOS turning-on in order to complete the model validation. Second the solutions presented before have been implemented. The measurements of the circuit will permit to verify the efficiency of the noise reduction solutions and indirectly models.

In a future work, the link between buck converter parameters and the increase in the noise floor at the ADC output should be investigated. The result will be dependent of ADC architecture.

The solutions proposed in this work could be improved: the variable buffer strength should be adapted to the victim susceptibility and the solution of ringing canceling could be adapted to other transitions (only for PMOS turning-on

in this work). Other solutions may be investigated especially at system level for example by dithering the buck converter switching frequency.

This work answers the objective exposed previously: to analyze the noise generation and its propagation throughout the system and to proposed solutions reducing this noise.

Only few studies are reported on the topic in the specific context of SMPS embedding and surely no link between the design parameters and the noise level due to the buck converter activity. The present work contributed to answer this absence by proposing a model to estimate noise generation and its propagation depending on system parameters.

The first solution (variable buffer strength) had already been integrated inside one of the STMicroelectronics micro-controllers for reliability problem. By limiting the undershoot, the stress of the power MOSFET is reduced.

Moreover the noise generation of embedded SMPSs on-chip with a micro-controller is a major issue in future products that target more accurate analog IPs and on-chip RF transmitters. The present work gives keys to answer this industrial concern and the proposed solutions may be a marker to differentiate STMicroelectronics micro-controller from the competition.

A Parallel RC association - Equivalent impedance

The development proves by recurrence that if $\forall k \in \llbracket 0, n \rrbracket$, $(\frac{\omega}{\omega_k})^2 \ll 1$ with $\omega_k = \frac{1}{R_k C_k}$, the equivalent impedance of the network in Figure A.1 may be approximated as:

$$Z_n = Re_n + Im_n = \frac{\sum_n R_n C_n^2}{(\sum_n C_n)^2} + \frac{1}{j\omega \sum_n C_n} \quad (\text{A.1})$$

So $Re_{eqn} = \frac{\sum_n R_n C_n^2}{(\sum_n C_n)^2}$ and $C_{eqn} = \sum_n C_n$.

For $n = 0$, $Z_0 = R_0 + \frac{1}{j\omega C_0}$ (series impedances).

For $n = 1$,

$$Z_1 = (R_0 + \frac{1}{j\omega C_0}) // (R_1 + \frac{1}{j\omega C_1})$$

$$Re_1 = \frac{R_0 C_0^2 + R_1 C_1^2 + R_0 R_1 (R_0 + R_1) C_0^2 C_1^2 \omega^2}{(C_0 + C_1)^2 + (R_0 + R_1)^2 C_0^2 C_1^2 \omega^2}$$

$$Im_1 = \frac{1}{j\omega} \frac{C_0 + C_1 + (R_0 C_0 + R_1 C_1)(R_0 + R_1) C_0 C_1 \omega^2}{(C_0 + C_1)^2 + (R_0 + R_1)^2 C_0^2 C_1^2 \omega^2}$$

If $(\frac{\omega}{\omega_0})^2 \ll 1, (\frac{\omega}{\omega_1})^2 \ll 1$,

$$Z_1 = Re_1 + Im_1 \approx \frac{R_0 C_0^2 + R_1 C_1^2}{(C_0 + C_1)^2} + \frac{1}{j\omega (C_0 + C_1)} \quad (\text{A.2})$$

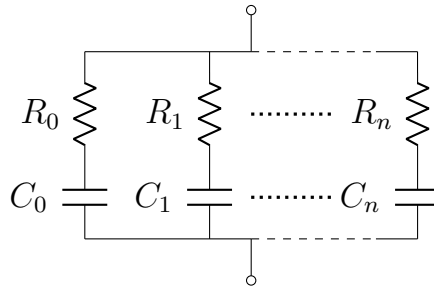


Figure A.1 – RC parallel association

Appendix A. Parallel RC association - Equivalent impedance

If the proposition is proven for n , then at $n + 1$,

$$Z_{n+1} = (R_{eqn} + \frac{1}{j\omega C_{eqn}}) // (R_{n+1} + \frac{1}{j\omega C_{n+1}})$$

but $(\frac{\omega}{\omega_{eqn}})^2 = (R_{eqn} C_{eqn} \omega)^2 = (\frac{\sum C_n}{\sum C_n} \omega)^2 \leq \max_n^2(\frac{\omega}{\omega_n}) \ll 1$ and $\frac{\omega}{\omega_{n+1}} \ll 1$

(A.2) applies, and

$$\begin{aligned} Z_{n+1} &= \frac{\frac{\sum R_n C_n^2}{(\sum C_n)^2} (\sum C_n)^2 + R_{n+1} C_{n+1}^2}{(\sum C_n + C_{n+1})^2} + \frac{1}{j\omega (\sum C_n + C_{n+1})} \\ &= \frac{\sum_{n+1} R_{n+1} C_{n+1}^2}{(\sum_{n+1} C_{n+1})^2} + \frac{1}{j\omega \sum_{n+1} C_{n+1}} \end{aligned}$$

The result is verified for $n + 1$ and concludes the recurrence.

B Parallel coupled RL association - Equivalent impedance

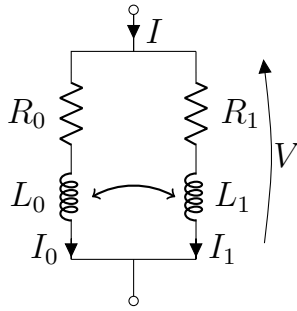


Figure B.1 – RL parallel association

The time equation of the network in Figure B.1 is given by,

$$\begin{aligned} V &= R_0 I_0 + L_0 \frac{dI_0}{dt} + M \frac{dI_1}{dt} \\ V &= R_1 I_1 + L_1 \frac{dI_1}{dt} + M \frac{dI_0}{dt} \\ I &= I_0 + I_1 \end{aligned}$$

In Laplace domain, the impedance is,

$$Z = \frac{(R_0 + j\omega L_0)(R_1 + j\omega L_1) + \omega^2 M^2}{R_0 + R_1 + j\omega(L_0 + L_1 + 2M)}$$

From this equation, the real and imaginary part are expressed as

$$\begin{aligned} Re &= \frac{R_0 R_1 (R_0 + R_1) + \omega^2 (R_0 (L_1 - M)^2 + R_1 (L_0 - M)^2)}{(R_0 + R_1)^2 + \omega^2 (L_0 + L_1 - 2M)^2} \\ Im &= j\omega \frac{L_0 R_1^2 + L_1 R_0^2 + 2M R_0 R_1 - (L_0 + L_1 - 2M)(L_0 L_1 - M^2)}{(R_0 + R_1)^2 + \omega^2 (L_0 + L_1 - 2M)^2} \end{aligned} \quad (B.1)$$

Considering the assumption $(\frac{\omega}{\omega_0})^2 \ll 1, (\frac{\omega}{\omega_1})^2 \ll 1$ with $\omega = \frac{R}{L-M}$,

$$Z = \frac{R_0 (L_1 - M)^2 + R_1 (L_0 - M)^2}{(L_0 + L_1 - 2M)^2} + j\omega \frac{L_0 L_1 - M^2}{L_0 + L_1 - 2M} \quad (B.2)$$

$$\text{So } R_{eq} = \frac{R_0 (L_1 - M)^2 + R_1 (L_0 - M)^2}{(L_0 + L_1 - 2M)^2} \text{ and } L_{eq} = \frac{L_0 L_1 - M^2}{L_0 + L_1 - 2M}.$$

C Spectrum envelop of the partial sawtooth signal

The function in Figure C.1 is periodic with respect to T , so the development in Fourier series is used to determine the spectrum envelop. This is an odd function so $(a_n)_{n \in \mathbb{N}} = 0$ and,

$$\begin{aligned}
 \forall n \in \mathbb{N}^*, b_n &= \frac{4}{T} \int_0^{\frac{T}{2}} f(t) \sin(2\pi n \frac{t}{T}) dt = \frac{4}{T} \int_0^{\frac{\alpha T}{2}} \frac{2A}{\alpha T} t \sin(2\pi n \frac{t}{T}) dt \\
 &= \frac{4A}{\alpha T^2} \left(\left[-t \frac{\cos(2\pi n \frac{t}{T})}{\frac{2\pi n}{T}} \right]_0^{\frac{\alpha T}{2}} + \int_0^{\frac{\alpha T}{2}} \frac{\cos(2\pi n \frac{t}{T})}{\frac{2\pi n}{T}} dt \right) \\
 &= \frac{2A}{n\pi\alpha T} \left(-\frac{\alpha T}{2} \cos(\pi n \alpha) + \left[\frac{T}{2\pi n} \sin(2\pi n \frac{t}{T}) \right]_0^{\frac{\alpha T}{2}} \right) \\
 &= \frac{A}{n\pi} \left(-\cos(\pi n \alpha) + \frac{1}{\pi n \alpha} \sin(\pi n \alpha) \right)
 \end{aligned} \tag{C.1}$$

The time signal is equal to $f(t) = \sum_n b_n \sin(2\pi n \frac{t}{T})$. In consequence, $\forall n \in \mathbb{N}^*, F(2\pi n \frac{1}{T}) = b_n$. Finally the envelop is,

$$\begin{aligned}
 F(\omega) &= \frac{2A}{\omega T} \left(-\cos(\alpha \omega \frac{T}{2}) + \frac{2}{\alpha \omega T} \sin(\alpha \omega \frac{T}{2}) \right) \\
 &= \frac{2AF_{clk}}{\omega} \left(-\cos\left(\frac{\alpha \omega}{2F_{clk}}\right) + \frac{2F_{clk}}{\alpha \omega} \sin\left(\frac{\alpha \omega}{2F_{clk}}\right) \right)
 \end{aligned} \tag{C.2}$$

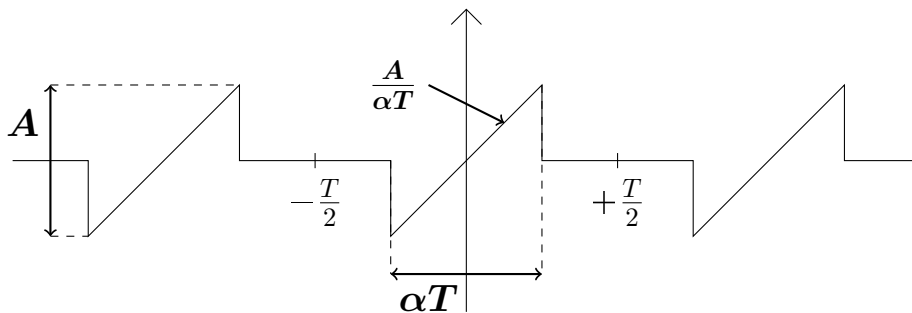


Figure C.1 – Partial sawtooth signal

D Fourier transform of time response of a RLC resonator

The time response of a RLC resonator is,

$$\forall t \in \mathbb{R}^+, I(t) = (A \cos(\omega_r t) + B \sin(\omega_r t)) e^{-\lambda t}$$

$$\text{with } \omega_r = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \text{ and } \lambda = \frac{R}{2L}$$

This signal is composed of $I_{\cos} : t \mapsto \cos(\omega_r t) e^{-\lambda t}$ and $I_{\sin} : t \mapsto \sin(\omega_r t) e^{-\lambda t}$. The Fourier transforms of these two functions are,

$$\begin{aligned} I_{\cos}(\omega) &= \int_{-\infty}^{+\infty} e^{-j\omega t} I_{\cos}(t) u(t) dt = \int_0^{+\infty} e^{-(\lambda+j\omega)t} \cos(\omega_r t) dt \\ &= \frac{1}{2} \left(\int_0^{+\infty} e^{-(\lambda+j(\omega-\omega_r))t} dt + \int_0^{+\infty} e^{-(\lambda+j(\omega+\omega_r))t} dt \right) \\ &= \frac{1}{2} \left(\frac{-[e^{-(\lambda+j(\omega-\omega_r))t}]_0^{+\infty}}{\lambda+j(\omega-\omega_r)} + \frac{-[e^{-(\lambda+j(\omega+\omega_r))t}]_0^{+\infty}}{\lambda+j(\omega+\omega_r)} \right) \\ &= \frac{1}{2} \frac{\lambda+j(\omega+\omega_r) + \lambda+j(\omega-\omega_r)}{(\lambda+j(\omega-\omega_r))(\lambda+j(\omega+\omega_r))} = \frac{\lambda+j\omega}{(\lambda+j\omega)^2 + \omega_r^2} \end{aligned} \quad (\text{D.1})$$

$$I_{\sin}(\omega) = \frac{\omega_r}{(\lambda+j\omega)^2 + \omega_r^2} \quad (\text{D.2})$$

From these results the Fourier transform of $I(t)$ is,

$$I(\omega) = \frac{A(\lambda+j\omega) + B\omega_r}{(\lambda+j\omega)^2 + \omega_r^2} \quad (\text{D.3})$$

The resonance occurs at each period of the buck converter so the time signal is made periodic using a convolution with a Dirac comb $\text{III}_{\frac{1}{F_{clk}}} = \sum_n \delta(t - \frac{n}{F_{clk}})$. The Fourier transform of the whole function is,

$$I(t) * \text{III}_{\frac{1}{F_{clk}}} \implies I(\omega) F_{clk} \text{III}_{F_{clk}} = F_{clk} \sum_n I(2\pi n F_{clk}) \quad (\text{D.4})$$

Considering the positive spectrum, the result is multiply by 2. Finally the spectrum envelop is,

$$I(\omega) = 2F_{clk} \frac{A(\lambda+j\omega) + B\omega_r}{(\lambda+j\omega)^2 + \omega_r^2} \quad (\text{D.5})$$

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1 Introduction

Les microcontrôleurs sont des circuits microélectroniques dans lesquels tous les composants informatiques sont intégrés. Les instructions sont stockées dans une mémoire non volatile et seule l'alimentation électrique est nécessaire au fonctionnement. L'interface avec l'environnement extérieur est assurée par des périphériques d'entrée/sortie (E/S) programmables : numériques, analogiques, de puissance ou encore RF.

Le marché des microcontrôleurs est en pleine mutation et devrait croître rapidement grâce au développement de l'Internet des Objets (IdO). La part des applications IdO sur le marché des microcontrôleurs est présentée à la figure 1.1. [1]. L'IdO a pour but de donner un identifiant à tous les dispositifs physiques, y compris les capteurs de tous les jours, les outils, les voitures ou même les entités vivantes. Il permettra la communication entre eux en étendant Internet à (presque) tout.

1.1 Quels sont les enjeux ?

L'IoT cible les appareils plus intelligents (électronique domestique), économes en énergie pour la gestion des modes à faible consommation (portable, téléphone intelligent et tablette), connectés (automobile, comptage) et compacts (plus de fonctionnalités dans le même volume, puce autonome).

A partir de ces préoccupations, la différenciation repose sur trois paramètres : la capacité de calcul, l'efficacité énergétique et la fonctionnalité analogique.

La capacité de calcul des microcontrôleurs augmente considérablement (de $50MHz$ à $400MHz$ au cours des dix dernières années et NXP a introduit un microcontrôleur double cœur en 2012). L'efficacité augmente (la consommation passe de $300\mu A/MHz$ à $40\mu A/MHz$, introduction du mode ultra basse consommation avec une consommation inférieure à $200nA$ et en 2012, Microchip passe de LDO à SMPS pour réduire de moitié la consommation). La fonctionnalité analogique a été améliorée : la haute résolution (16 bits) du convertisseur analogique-numérique (ADC) et des émetteurs RF (Bluetooth, WiFi, Zigbee) ont été intégrés au microcontrôleur. La gestion de l'alimentation (partie active) est intégrée afin que le microcontrôleur puisse fonctionner avec seulement quelques composants passifs hors puce. Certains démonstrateurs intègrent même les condensateurs et les inductances à l'intérieur du boîtier [3]. Cette technologie n'est pas encore utilisée comme courant dominant dans les

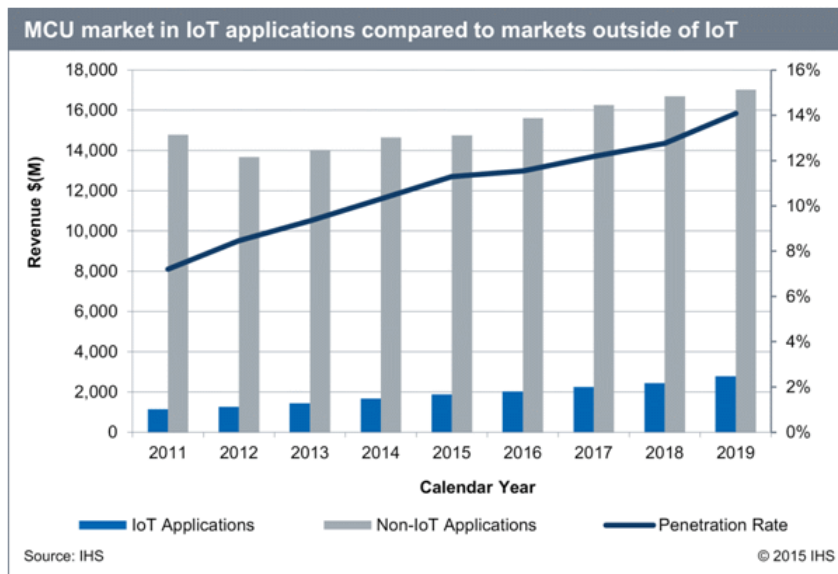


FIGURE 1.1 – Impact de l’IdO sur le marché des microcontrôleurs - IHS 2015 [1]

circuits de microcontrôleurs en raison des restrictions de surface et de coût.

Les principaux enjeux des modules de gestion de l’énergie sont :

- fournir la puissance de sortie nécessaire
- optimiser le rendement énergétique dans les différents modes de fonctionnement,
- ne pas dégrader les performances du reste du circuit.

L’architecture doit être choisie avec soin pour répondre à ces enjeux.

1.2 Pourquoi un SMPS ?

Le module de puissance intégré est chargé d’alimenter le coeur de calcul avec un niveau de tension adapté. Ici le régulateur abaisse la tension d’entrée de 1,6V à 3,6V à 1,2V en sortie. Le module de puissance doit rester efficace et fiable pour toute tension dans cette plage.

Trois structures sont envisagées : un régulateur LDO (Low-Drop-Out) ou une alimentation à découpage (SMPS) capacitive ou inductive. Lorsqu’elle est utilisée pour abaisser la tension d’entrée, le SMPS est appelé convertisseur buck. Cette dénomination sera utilisée dans le reste du rapport. Le fonctionnement et les avantages et inconvénients de chaque architecture sont détaillés dans la section suivante.

1.2.1 Low-Drop-Out - LDO

Les avantages de cette structure sont sa "simplicité", la réponse transitoire rapide et la faible contribution au bruit (pas de commutation). Le principal inconvénient est le faible rendement, inférieure à 33% dans le pire des cas, causant une dégradation des performances en mode basse consommation mais

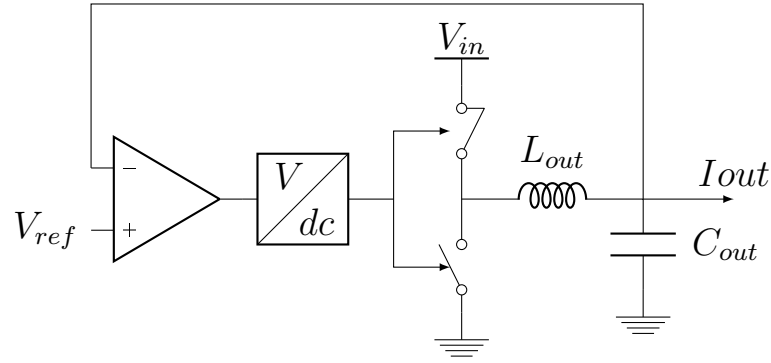


FIGURE 1.2 – Schéma structurel d'un convertisseur inductif buck

créant également un problème thermique dans les modes utilisant toute la puissance de calcul en raison de la grande quantité d'énergie dissipée.

1.2.2 Convertisseur capacitif buck

La tension de sortie est une fraction de la tension d'entrée et ne peut être fixée indépendamment. Dans ces conditions le rendement est bon (autour de 80%) mais en cas de chute de la tension d'entrée (par exemple décharge de batterie), la tension de sortie suivra cette chute empêchant le bon fonctionnement du système. Pour résoudre ce problème, la structure capacitive se règle à une tension plus élevée et augmente les pertes résistives pour atteindre la tension souhaitée. Cela dégrade l'efficacité telle que présentée dans [4]. De plus, l'augmentation du nombre de niveaux de tension de sortie requis implique un plus grand nombre de commutateurs et de condensateurs, ce qui affecte l'efficacité du système et nécessite l'utilisation de plusieurs E/S (deux pour chaque condensateur). Un autre inconvénient, dus aux composants passifs externes, les commutations au travers l'impédance parasite du boîtier génèrent du bruit.

1.2.3 Convertisseur inductif buck

Le schéma structurel du convertisseur inductif buck est présenté dans la figure 1.2. Le courant traversant l'inductance L_{out} est régulé pour charger le condensateur de sortie C_{out} à la tension souhaitée. Lorsque le commutateur haut est fermé, le courant augmente de $L_{out} \frac{dI_{out}}{dt} = V_{in} - V_{out}$ alors que lorsque le commutateur bas est fermé, le courant diminue de $L_{out} \frac{dI_{out}}{dt} = V_{out}$. Par ajustement du rapport cyclique (α), le courant est régulé pour charger le condensateur à V_{ref} et pour fournir le courant de sortie I_{out} demandé. Les méthodes de régulation sont diverses (tension, courant ou mode hystérétique) et bien décrites dans la littérature [5].

Le rendement de la structure est similaire à celle de la structure capacitive. Les pertes de commutation, R_{dson} , et les impédances parasites sont responsables de la dégradation du rendement. Pour le maintenir correcte en mode basse puissance, des techniques de saut d'impulsions sont utilisées. Au lieu d'injecter systématiquement une petite quantité d'énergie, un minimum d'énergie

Reference	V_{in} (V)	V_{out} (V)	I_{out} (mA)	Efficiency
O. Trescases [7]	2.7	1.8	1 – 1000	82% – 91%
F. Neveu [8]	3.6	1.2 – 2.4	0 – 300	up to 91.5%
C. H. Huang [9]	3 – 3.6	1 – 1.8	1 – 500	90% – 97%
Microchip SAM4L [10]	2 – 3.6	1.7	5 – 50	82% – 95%

TABLE 1.1 – Partial state of the art of inductive buck converter efficiency

Architecture	LDO	Capacitive	Inductive
Pros	<ul style="list-style-type: none"> • simplicity • fast transient • low noise 		<ul style="list-style-type: none"> • efficiency
Cons	<ul style="list-style-type: none"> • bad efficiency 	<ul style="list-style-type: none"> • I/Os number • bad efficiency • switching noise 	<ul style="list-style-type: none"> • switching noise • complexity

TABLE 1.2 – Avantages et inconvénients des structures de puissance dans le contexte des microcontrôleurs

est injecté une seule fois et le système attend que cette énergie soit consommée, "sautant des impulsions", avant la réinjection. Cela réduit la fréquence de commutation et donc les pertes de commutation [6]. Certains rendements de la littérature sont présentés dans le tableau 1.1.

Un convertisseur buck avec une architecture à l'état de l'art peut atteindre un rendement supérieur à 90% dans la gamme étudiée. Dans la structure de [8], les dispositifs passifs sont embarqués dans le même boîtier. Le rendement pour une tension de sortie de 1,2V est supérieur à 80% pour un courant supérieur à 100mA. Cependant cette topologie est aujourd'hui coûteuse et donc peu réaliste pour une production en grande série. Lorsque le convertisseur buck est intégré dans un microcontrôleur, le rendement est toujours supérieure à 80% (Microchip SAM4L [10]).

L'avantage de l'architecture de convertisseur inductif est le haut rendement mais les inconvénients sont le bruit généré par les commutations au niveau de la carte et à l'intérieur de la puce (interaction avec le microcontrôleur et autres IP) et une structure relativement complexe utilisant une large surface de silicium.

Les avantages et les inconvénients de chaque architecture sont résumés dans le tableau 1.2.

STMicroelectronics a choisi d'intégrer un module de puissance inductif à l'intérieur du dernier microcontrôleur STM32 car seuls deux composants passifs sont nécessaires pour une large gamme de tension. Le commutateur haut est un PMOS et le commutateur bas est un NMOS. Pour améliorer la réponse transitoire, une rétroaction asynchrone a été ajoutée au système, augmentant un peu plus sa complexité [11]. La surface de la structure SMPS, plus grande que celle d'un LDO, est petite par rapport à la surface totale du CI. Un inconvénient majeur demeure : le bruit de commutation. Ce bruit pourrait avoir un

1.3. Qu'est-ce qui est bruyant dans une alimentation à découpage ?

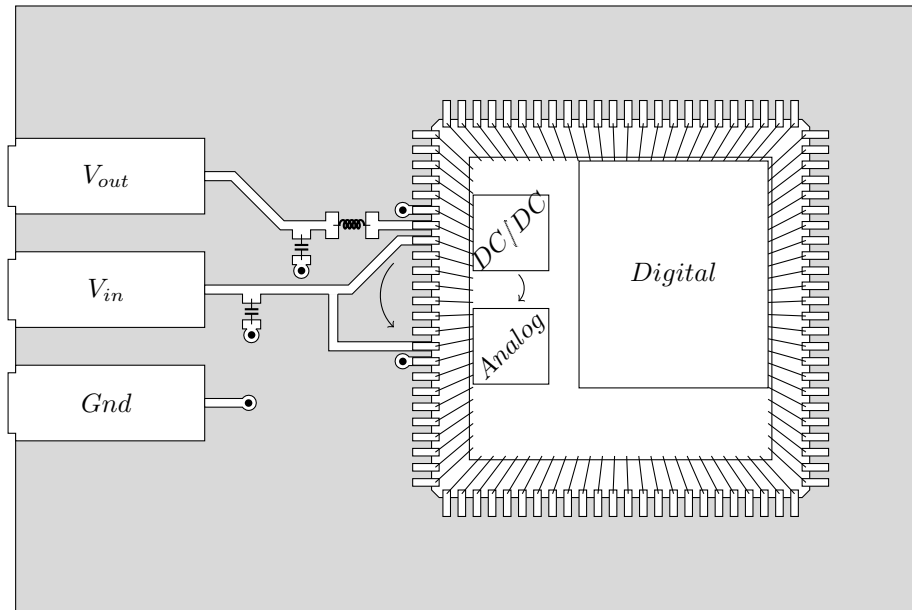


FIGURE 1.3 – Buck converter inside the micro-controller

impact sur les performances des IP analogiques sensibles du microcontrôleur. Le contexte du microcontrôleur est présenté dans la figure 1.3. Le bruit pollue les IP analogiques par deux voies principales : par paires d'alimentations connectées sur PCB ou directement sur puce par le substrat.

Une étude de la génération de bruit et de son impact est nécessaire pour garantir un fonctionnement satisfaisant des blocs analogiques sensibles du microcontrôleur.

1.3 Qu'est-ce qui est bruyant dans une alimentation à découpage ?

Quelle que soit la méthode de contrôle de la rétroaction, l'étage de puissance d'un convertisseur Buck est assez similaire : un PMOS et un NMOS [5]. La boucle de régulation active et désactive alternativement les deux interrupteurs. Pour améliorer le rendement, la résistance du MOSFET, R_{dson} doit être faible et la commutation doit être aussi rapide que possible. Pour avoir une faible R_{dson} et tolérer un niveau de courant élevé, les MOSFETs sont larges. Par conséquent, les capacités de grille sont larges et ont besoin d'un contrôle puissant pour commuter rapidement, ce qui entraîne un appel de courant important pendant la charge des grilles. De plus, le courant dans l'inductance I_{Lout} passe du canal du PMOS au canal du NMOS. Toutes ces variations de courant présentées dans la figure 1.4, stimulent les impédances parasites également appelé réseau de distribution de puissance (PDN). Les larges fluctuations du niveau de tension d'alimentation, appelées bruit de commutation, sont présentées sur la figure 1.5.

En conclusion, il existe deux différenciateurs sur le marché des microcontrô-

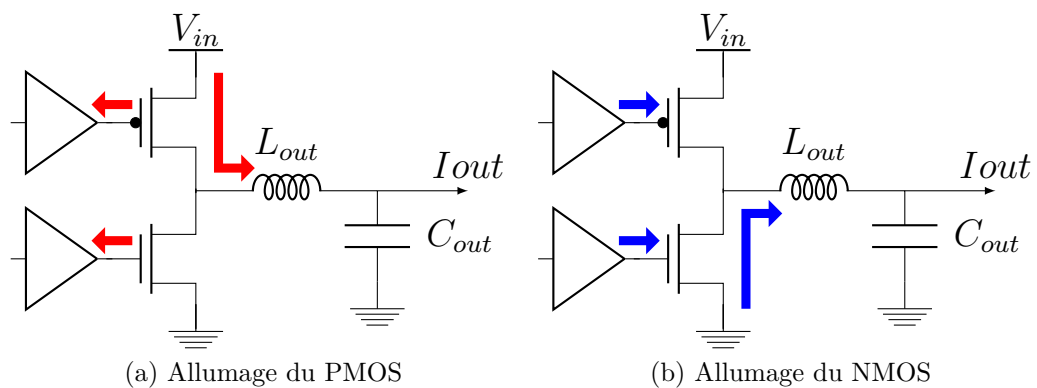


FIGURE 1.4 – Chemin de courant dans le convertisseur buck

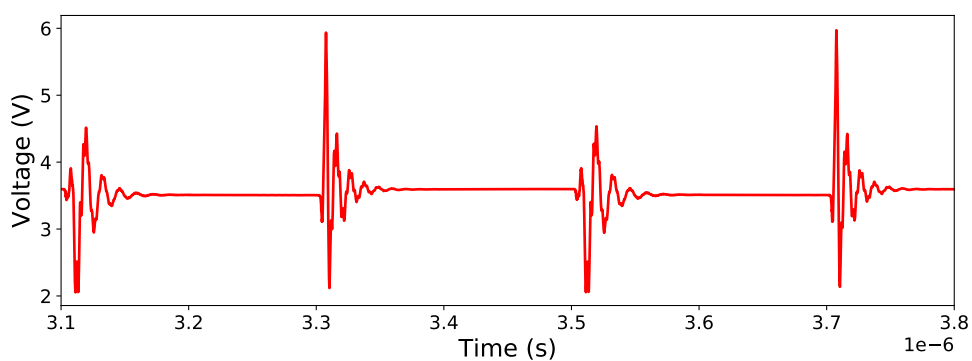


FIGURE 1.5 – Exemple de fluctuations de la tension d'entrée d'un convertisseur buck

1.3. Qu'est-ce qui est bruyant dans une alimentation à découpage ?

leurs : le rendement et les performances analogiques. L'introduction du SMPS est adaptée pour répondre au premier mais est en contradiction avec le second. Par conséquent, il est essentiel de gérer ce bruit pour permettre un bon fonctionnement des IP sensibles à l'intérieur du microcontrôleur. Pour y parvenir, il faut répondre à trois questions : Quelle quantité de bruit se propage aux victimes ? Quels sont les leviers pour contrôler le bruit ? Quel est le niveau de bruit admissible sur les victimes ? Comme dans toute approche d'ingénierie, une étude préalable est nécessaire avant de réfléchir aux actions. La CEM est particulièrement sensible aux sondes intrusives, de sorte que la plupart des connaissances doivent être construites sur la simulation, ce qui implique des modèles. Ces modèles doivent également être validés.

La susceptibilité des victimes dépend fortement du type et de l'architecture de la victime. Répondre de manière générale n'est pas possible et la meilleure personne pour répondre sur ce qui est admissible doit être le concepteur de l'IP lui-même. Mais la forme du bruit et sa propagation vers la victime doivent être déterminées pour lui permettre d'évaluer l'impact sur les performances de son IP.



L'objectif de cette thèse est donc :

Analyser les mécanismes de pollution d'un convertisseur buck sur des IP analogiques sensibles intégrées dans un SoC et développer des techniques de minimisation du bruit de ce convertisseur.

Le deuxième chapitre explique la signature du bruit et détaille les modèles d'émission dus à chaque transition de l'étage de puissance du convertisseur buck en fonction des paramètres du système. Ensuite, le chapitre suivant présente le modèle de propagation du bruit à l'intérieur de la puce et de son environnement en analysant les principaux chemins de propagation pour différentes plages de fréquence. Chaque modèle est validé par comparaison avec les résultats de simulation et de mesure.

Le troisième chapitre présente des solutions pour réduire l'amplitude du bruit en modifiant l'architecture de l'étage de puissance ce qui modifie le comportement des transitions. Il présente également une solution pour augmenter l'impédance d'un chemin de propagation par des modifications de routage de haut niveau.

Un dernier chapitre conclut et dessine des perspectives.

2 Modélisation du bruit

2.1 La source de bruit - l'étage de puissance

L'étage de puissance est présenté en figure 2.1a. Il peut être dans trois états différents : conduction de PMOS, l'état P_{ON} ; conduction de NMOS, l'état N_{ON} ; phase non-superposition, l'état OFF . Une fréquence de résonance spécifique correspond à chaque état et les transitions entre ces états stimulent le réseau parasite.



Pour comprendre la composition du bruit en termes de fréquence et d'amplitude, le réseau parasite est simplifié en un simple RLC. Les conditions R, L, C et les conditions initiales sont définies par la combinaison de composants parasites pour reproduire la stimulation du réseau pendant les transitions.

La réponse temporelle du réseau RLC est une solution de (2.1),

$$\frac{d^2 I}{dt^2} + \frac{R}{L} \frac{dI}{dt} + \frac{1}{LC} I = 0 \quad (2.1)$$

La solution générale de (2.1) est de la forme,

$$I(t) = (A \cos(\omega_r t) + B \sin(\omega_r t)) e^{-\lambda t} \quad (2.2)$$

with $\omega_r = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$ and $\lambda = \frac{R}{2L}$

Dans les sous-sections suivantes, les impédances parasites du système dans chaque état sont analysées pour déterminer R, L, C, puis les stimulations pendant chaque transition entre ces états pour déterminer les expressions A, B pour chaque transition..

2.1.1 Réseau de composants parasites

Chaque état est étudié séparément pour déterminer le réseau parasite. Les composants parasites remplaceront le MOSFET dans le schéma de l'étage de puissance global équivalent de la figure 2.1b.

Le package et les pistes du PCB sont représentés par les inductances équivalentes $L = L_+ + L_-$.

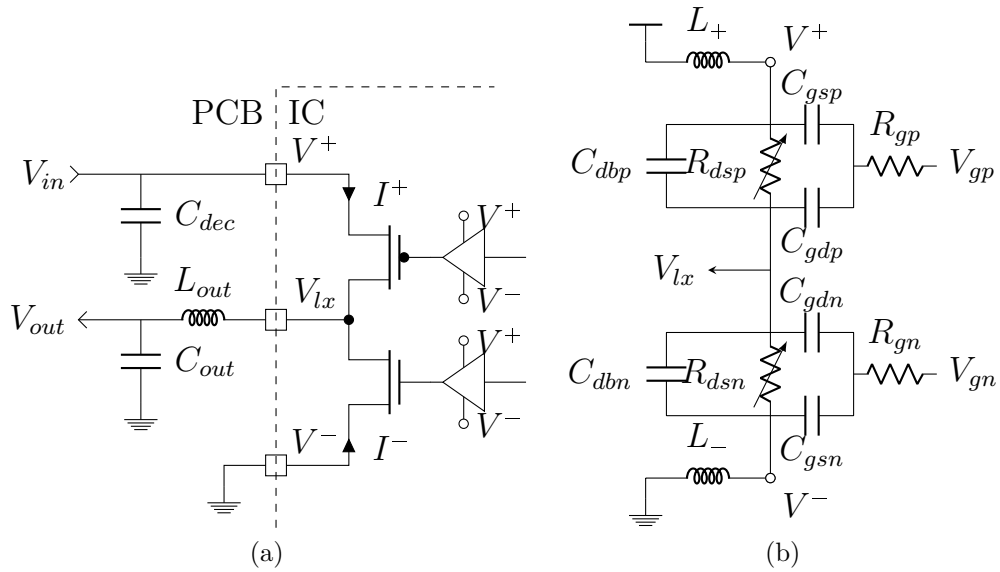


FIGURE 2.1 – Structure de l'étage de puissance (a) et son réseau équivalent (b)

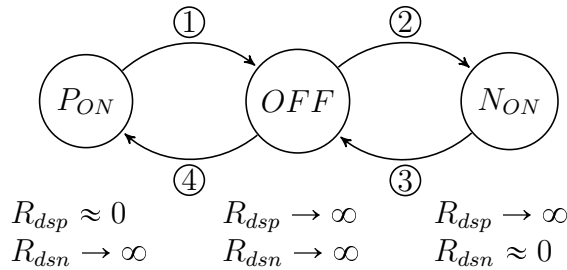


FIGURE 2.2 – Transitions de l'étage de puissance avec la valeur de resistance drain-source correspondante

Les contrôles de grille sont représentés par leur résistance de sortie R_{gp} , R_{gn} connecté respectivement à V^+ et V^- : $V_{gp}, V_{gn} \in \{V^+, V^-\}$. Depending on these voltages, the channel resistance of the MOSFET can be a high impedance or R_{on} . Comparing R_{on} values (few $m\Omega$) to R_{gp} , R_{gn} (few Ω), the ON-state MOSFET channel resistance is neglected. Finally $R_{dsp}, R_{dsn} \in \{0, \infty\}$ (see figure 2.2). En fonction de ces tensions, la résistance de canal du MOSFET peut être une impédance élevée ou R_{on} . En comparant les valeurs de R_{on} (quelques $m\Omega$) au R_{gp} , R_{gn} (quelques Ω), la résistance du canal MOSFET à l'état ON est négligée. Finalement $R_{dsp}, R_{dsn} \in \{0, \infty\}$ (voir figure 2.2).

Le schéma RC équivalent de chaque état est représenté dans la figure 2.3.

Le réseau est simplifié à un simple RLC à l'aide de la formule : $R = \frac{\sum R_n C_n^2}{\sum C_n}$ and $C = \sum C_n$. Une hypothèse est faite pour utiliser ces formules : toutes les fréquences de résonance sont inférieures à $200MHz$, pour garantir que tous les $(RC\omega)^2 < 0.1 \ll 1$. Cette hypothèse est confirmée par des applications numériques et des mesures.

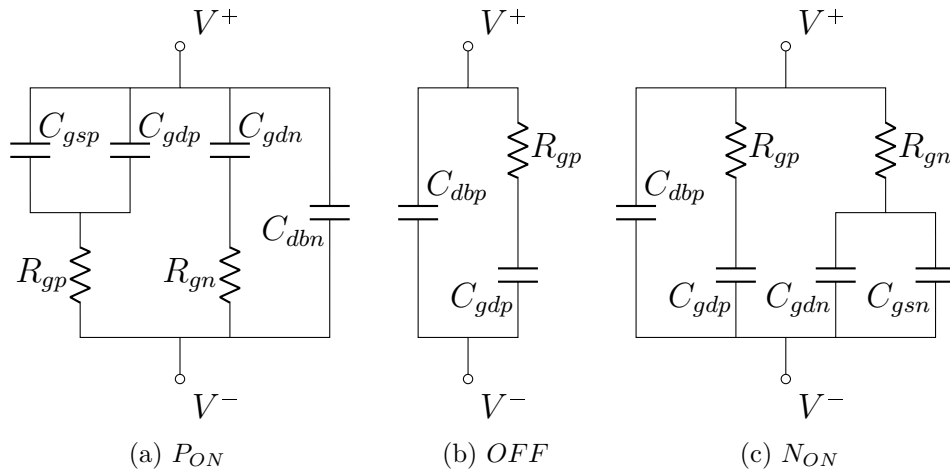


FIGURE 2.3 – Schémas équivalents dans les états P_{ON} (a), OFF (b) et N_{ON} (c)

Composants parasites dans l'état P_{on} :

$$R_{P_{on}} = \frac{R_{gp}(C_{gdp} + C_{gsp})^2 + R_{gn}C_{gdn}^2}{(C_{gdp} + C_{gsp} + C_{gdn} + C_{dbn} + C_d)^2} \quad (2.3)$$

$$C_{P_{on}} = C_{gdp} + C_{gsp} + C_{gdn} + C_{dbn} + C_d$$

Composants parasites dans l'état OFF :

$$R_{off} = \frac{R_{gp}C_{gdp}^2}{(C_{gdp} + C_{dbp} + C_d)^2} \quad (2.4)$$

$$C_{off} = C_{gdp} + C_{dbp} + C_d$$

Composants parasites dans l'état N_{on} :

$$R_{N_{on}} = \frac{R_{gp}C_{gdp}^2 + R_{gn}(C_{gdn} + C_{gsn})^2}{(C_{gdp} + C_{dbp} + C_{gdn} + C_{gsn} + C_d)^2} \quad (2.5)$$

$$C_{N_{on}} = C_{gdp} + C_{dbp} + C_{gdn} + C_{gsn} + C_d$$

Dans l'état OFF , seules quelques capacités sont impliquées dans le calcul de la fréquence de résonance. De plus, à l'état ouvert, les capacités MOSFET sont plus faibles qu'à l'état fermé. Les capacités parasites de contrôle de grille deviennent significatives et doivent être prises en compte dans les calculs. Pour modéliser les impédances parasites du contrôle de grille, deux réseaux RC sont ajoutés en parallèle, R_{bufp} , C_{bufp} et R_{bufn} , C_{bufn} . Finalement, le réseau RC équivalent dans l'état OFF peut être exprimé sous la forme,

$$R_{off} = \frac{R_{gp}C_{gdp}^2 + R_{bufp}C_{bufp}^2 + R_{bufn}C_{bufn}^2}{(C_{gdp} + C_{dbp} + C_d + C_{bufp} + C_{bufn})^2} \quad (2.6)$$

$$C_{off} = C_{gdp} + C_{dbp} + C_d + C_{bufp} + C_{bufn}$$

Sur la base de ces réseaux RLC, l'objectif suivant est de déterminer la stimulation, c'est-à-dire la condition initiale après la commutation. Pour atteindre cet objectif, une analyse de chaque transition est nécessaire.

2.1.2 Analyse des transitions

Les stimulations du réseau sont dues aux variations de courant dans les inductances parasites. Ces variations de courant dues à deux phénomènes :

1. La charge et la décharge des capacités parasites des MOSFET,
2. Le changement du chemin d'écoulement du courant de $V_{in} \rightarrow V_{lx}$ à $gnd \rightarrow V_{lx}$ et inversement.

Les transitions sont numérotées de ① à ④ comme présenté dans la figure 2.2.

Lors de chaque transition, les potentiels de grille changent. Par conséquent le premier phénomène doit donc être évalué pour chaque transition. Le chemin du courant de sortie ne change que lors de l'allumage (transition ④) ou de l'extinction (transition ①) du PMOS parce que le NMOS et la diode (du NMOS) sont connectés à V^- .

Chaque transition est détaillée dans les paragraphes suivants. Les chemins de charge et de décharge des capacités parasites sont représentés sur la figure 2.4. Les courants de V^+ en rouge, les courants de V^- en bleu et la recombinaison de charge en vert. Les courbes temporelles sont données dans la figure 2.5 où les zones grises représentent la charge des capacités.

Arrêt du PMOS ① : La grille du PMOS commence à se charger, réduisant le R_{on} . Le courant de sortie s'écoule au travers des capacités parasites du MOSFET au lieu du canal PMOS. Comme ces capacités sont principalement connectées à V^+ , le chemin de courant ne change pas pendant la décharge. Lorsque V_{lx} atteint $-V_{th}$, le chemin de courant passe rapidement de V^+ (capacités parasites) à V^- (diode NMOS). Ce changement brutal stimule le réseau parasite.

Allumage du NMOS ② : La grille du NMOS commence à se charger. Les capacités parasites injectent des charges de V^+ vers la sortie, réduisant ainsi le courant dans le canal du NMOS. Une fois les condensateurs chargés, le courant repasse par le canal du NMOS. Ce courant de charge sur V^+ stimule le réseau parasite.

Arrêt du NMOS ③ : Le déroulement est similaire à celui de l'allumage du NMOS, mais les capacités parasites du NMOS court-circuitée. Ces capacités ne génèrent donc pas d'appel de courant. Seul petit appel de courant est dû à l'augmentation de V_{lx} de $V^- - V_{th}$ à V^- sur les capacités parasites du PMOS.

Allumage du PMOS ④ : La grille du PMOS est déchargée d'une tension de seuil V_{th} . Lorsque le PMOS est activé, le chemin actuel passe du canal du NMOS au canal du PMOS. Lorsque le courant traversant la diode atteint zéro, V_{lx} commence à monter à V^+ puis la grille du PMOS

est déchargée à V^- . Le changement de chemin de courant stimule le réseau mais le dépassement du courant est masqué par la demande de charge des capacités parasites. Le dépassement est donc lié à l'appel de courant dû à la charge des capacités.

Pour chacune des transitions, la réponse du circuit équivalente est calculée avec des conditions initiales choisies en fonction du phénomène de stimulation (capacités déchargées ou variations de courant dans les inductances parasites). Un exemple d'application pour $V_{in} = 3.6V$ et $I_{out} = 0.3A$ est donné pour chaque transition.

2.1.3 Arrêt du PMOS ①

Lors de l'extinction du PMOS, la chute de I_{out} dans l'inductance parasite du PDN stimule le réseau équivalent de l'étage de puissance décrit dans la figure 2.3b.

L'extension du PMOS ① peut être modélisée par un réseau RLC avec une source de courant comme présenté dans la figure 2.6a. L'activation de la diode est modélisée par la fermeture d'un interrupteur idéal, court-circuitant la source de courant. Pour tenir compte de la tension de seuil de la diode, la tension d'alimentation doit être augmentée à $V_{in} + V_{th}$ mais ce potentiel n'est pas impliqué dans le calcul suivant.

La forme du courant est donné par la fonction (2.2), où $R = R_{off}$, $C = C_{off}$ (2.6) et $L = L_+ + L_-$. A et B sont déterminées grâce aux conditions initiales, ici :

- I est continue due à la continuité du courant dans une inductance donc $I(0^+) = I(0^-) = I_{out}$.
- $V_C(0^+) = V_C(0^-)$ car le potentiel au borne d'une capacité est continue. V_R , la tension à travers la résistance, est proportionnelle à I qui est continue. Par conséquent, la tension à travers RC est continue. $V_C^-(0^-) = 0V = V_C^-(0^+)$ (diode) donc la tension à travers l'inductance est continue, ce qui implique $\frac{dI}{dt}(0^+) = \frac{dI}{dt}(0^-) = \frac{dI_{out}}{dt} = 0$.

En utilisant les conditions initiales (2.2), $A = I_{out}$ et $B = \frac{\lambda I_{out}}{\omega_r}$.

$$I_1(t) = I_{out}(\cos(\omega_r t) + \frac{\lambda}{\omega_r} \sin(\omega_r t))e^{-\lambda t} \quad (2.7)$$

Cette fonction atteint son maximum à $t = \frac{\pi}{\omega_r}$, $I_{min} = -I_{out}e^{-\lambda\pi/\omega_r}$.

2.1.4 Allumage du NMOS ②

Lors de l'allumage du NMOS, le I_{out} actuel continue de circuler à travers l'interconnexion de masse. L'appel de courant est dû à la charge de la porte NMOS et ne dépend donc pas du courant de charge I_{out} , donc le courant choisi est $I_{out} = 0A$ pour faciliter l'analyse. La charge des capacités stimule le réseau parasite RLC où $R = R_{Non}$, $C = C_{Non}$ (2.5) et $L = L_+ + L_-$.

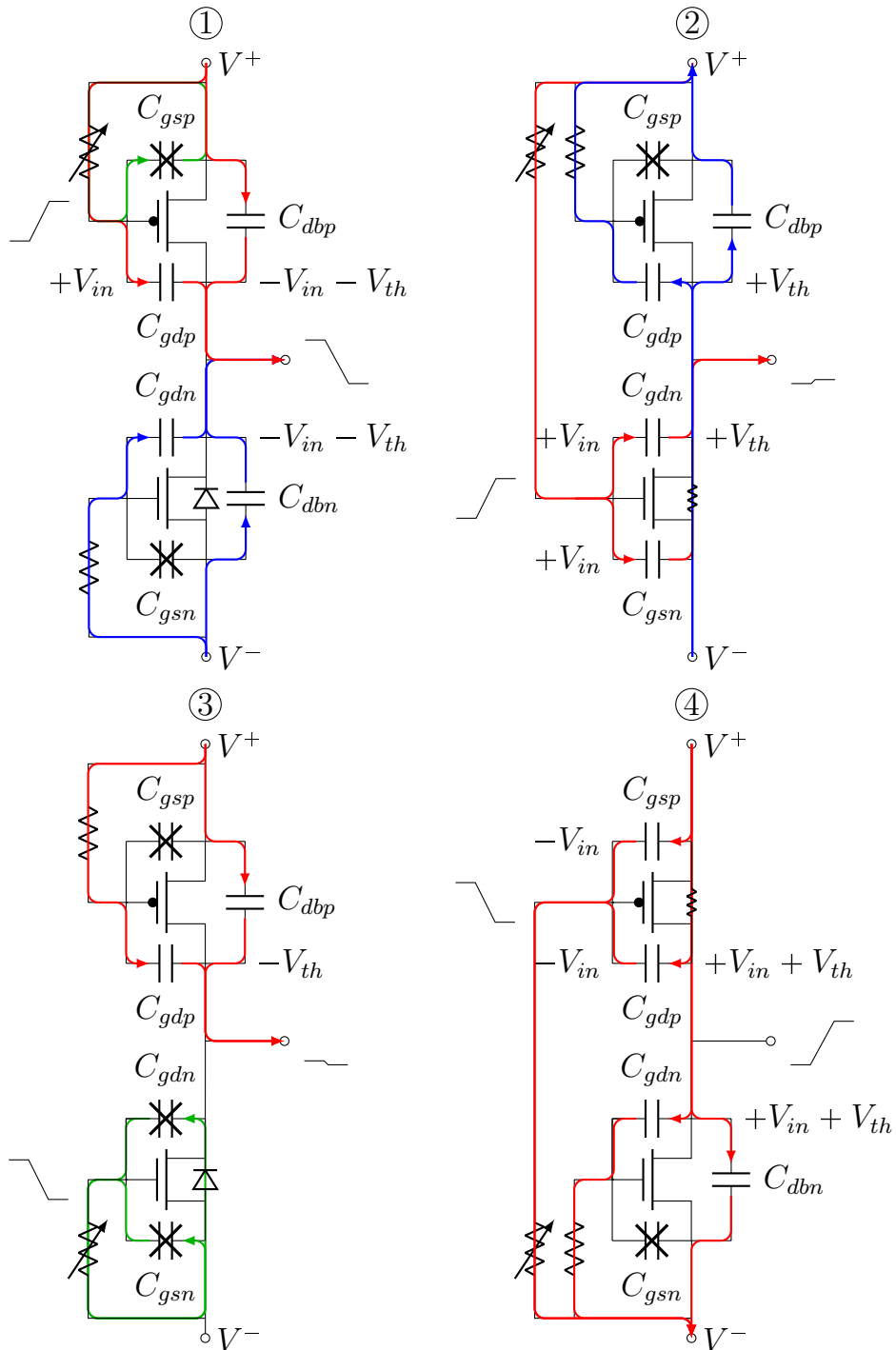


FIGURE 2.4 – Détails de l'injection de charge pour chaque transition

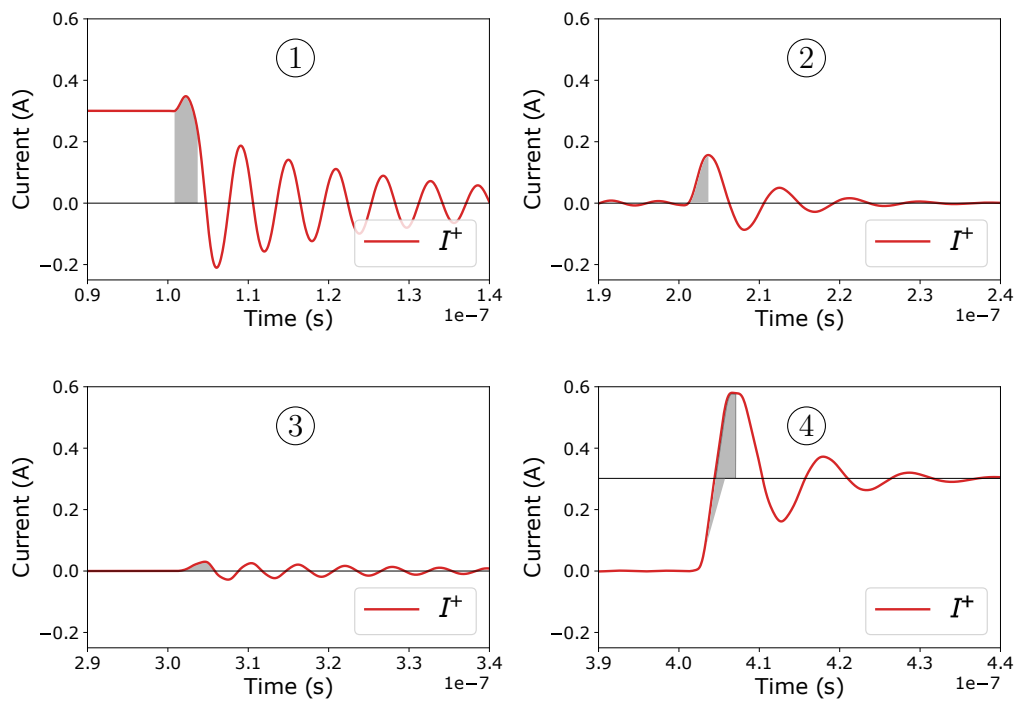
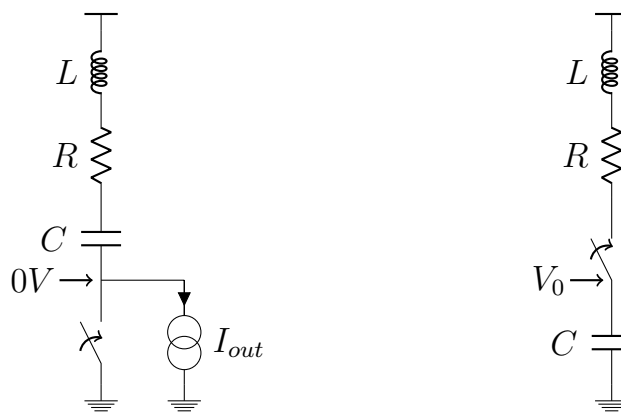


FIGURE 2.5 – Courbes de I^+ pendant les transitions ①, ②, ③ et ④ obtenues par simulation



(a) PMOS turning-off - diode activation (b) NMOS turning-on - gate charging

FIGURE 2.6 – Schéma équivalent durant les différentes transitions

2.1. La source de bruit - l'étage de puissance

Le modèle correspondant pour l'allumage de NMOS (phase ②) est représenté sur la figure 2.6b. L'interrupteur idéal représente le passage de la commande du NMOS à V_{in} .

V_0 est calculée par un ratio entre la demande de charges et la capacité totale du réseau parasite,

$$V_0 = V_{in} - \frac{\Delta Q_2}{C_{Non}} \quad (2.8)$$

La demande de charge sur V^+ pour recharger les capacités de grille représentées dans la figure 2.4 est donnée par (2.9),

$$\begin{aligned} \Delta Q_2 &= -V_{th}C_{dbp} - V_{th}C_{gdp} + (V_{in} - V_{th})C_{gdn} + V_{in}C_{gsn} \\ &= V_{in}(C_{gdn} + C_{gsn}) - V_{th}(C_{dbp} + C_{gdp} + C_{gdn}) \end{aligned} \quad (2.9)$$

A et B sont calculées grâce à (2.2) avec les conditions initiales suivantes :

- I est continu par continuité du courant dans une inductance, de sorte que $I(0^+) = I(0^-) = 0$.
- $L \frac{dI}{dt}(0^+) = V_{in} - RI(0^+) - V_C(0^+) = V_{in} - V_0 = \frac{\Delta Q_2}{C_{Non}}$ est continue par continuité de la tension aux bornes d'un condensateur.

La réponse ne courant durant la transition est donc :

$$I_2(t) = \frac{\Delta Q_2}{LC\omega_r} \sin(\omega_r t) e^{-\lambda t} \quad (2.10)$$

Le maximum de la fonction est atteint à $t = \frac{1}{\omega_r} \arctan(\frac{\omega_r}{\lambda})$ et vaut $I_{max} = \frac{\Delta Q_2}{LC\omega_r} \frac{1}{\sqrt{1+(\frac{\lambda}{\omega_r})^2}} e^{-\frac{\lambda}{\omega_r} \arctan(\frac{\omega_r}{\lambda})}$ avec $\sin(\arctan(x)) = \frac{x}{\sqrt{1+x^2}}$.

2.1.5 Arrêt du NMOS ③

Les phénomènes impliqués pendant cette transition sont similaires à ceux de la transition ② : le courant de sortie I_{out} continue à circuler à travers l'interconnexion de masse. Mais les capacités de grille du NMOS sont court-circuitées, de sorte que la demande de charge est fortement réduite :

$$\Delta Q_3 = V_{th}(C_{dbp} + C_{gdp}) \quad (2.11)$$

En conséquence, le dépassement et donc la contribution du bruit est relativement faible par rapport aux autres transitions comme l'illustre la figure 2.5. Pour notre étude, le bruit de cette transition est négligé.

2.1.6 Allumage du PMOS ④

Pendant cette transition, la grille du PMOS est déchargée à la masse et le courant de sortie I_{out} passe de l'interconnexion de masse à l'interconnexion d'alimentation. Les deux phénomènes décrits précédemment pour les transitions ① et ② sont impliqués.

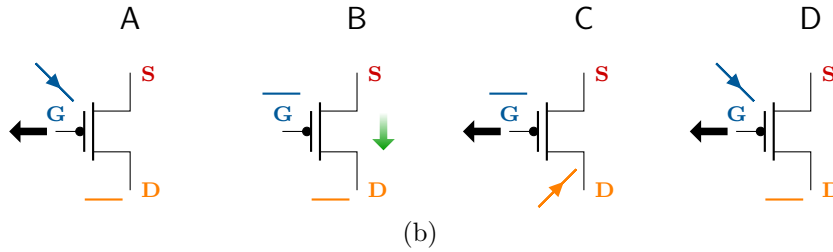
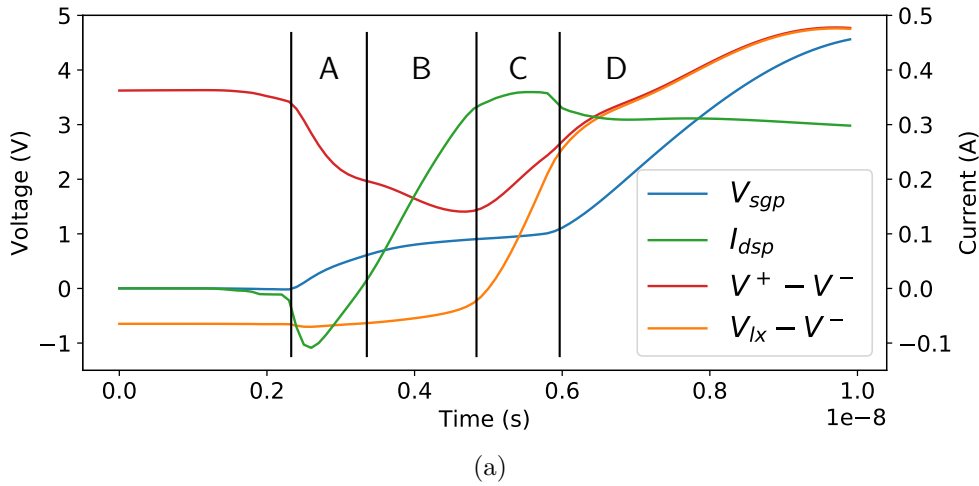


FIGURE 2.7 – Courbes simulées de la transition ④

La propagation des charges à la transition est présentée dans la figure 2.4. La charge totale transférée est exprimée comme suit,

$$\begin{aligned} \Delta Q_4 &= -\Delta V_{gp} C_{gsp} + (\Delta V_{lx} - \Delta V_{gp}) C_{gdp} + \Delta V_{lx} C_{gdn} + \Delta V_{lx} C_{dbn} \\ &= V_{in} (C_{gsp} + 2C_{gdp} + C_{gdn} + C_{dbn}) + V_{th} (C_{gdp} + C_{gdn} + C_{dbn}) \end{aligned} \quad (2.12)$$

Malheureusement, le calcul ne peut pas être fait directement comme pour ② à cause du déroulement de la transition.

La mise sous tension du PMOS peut être divisée en quatre phases présentées dans la figure 2.7a : la charge de V_{sgp} au seuil (A), l'augmentation du courant par le canal PMOS I_{dsp} (B), la hausse de V_{lx} à V^+ (C) et enfin la charge de V_{sgp} du seuil à V^+ (D).

Cette dernière phase (D) absorbe le dépassement créé par la phase précédente, de sorte qu'à la fin, le dépassement est dû au transfert de charge pendant la charge de V_{sgp} à V_{in} . Par conséquent, la stimulation ne dépend pas du niveau de courant de sortie.

La variation des charges au cours de la phase D est exprimée par,

$$\begin{aligned} \Delta Q_4 &= (-\Delta V_{gp} - V_{th})(C_{gsp} + C_{gdp}) + (V_{in} - \Delta V)(C_{gdn} + C_{dbn} + C_d) \\ &= (V_{in} - V_{th})(C_{gsp} + C_{gdp}) + (V_{in} - \Delta V)(C_{gdn} + C_{dbn} + C_d) \end{aligned} \quad (2.13)$$

Il y a des fluctuations sur la tension d'alimentation dues à la phase précédente : la charge du nœud V_{lx} à V^+ . Ces fluctuations sont prises en compte dans le terme $(V_{in} - \Delta V)(C_{gdn} + C_{dbn} + C_d)$ avec $\Delta V = V^+ - V^-$. La variation

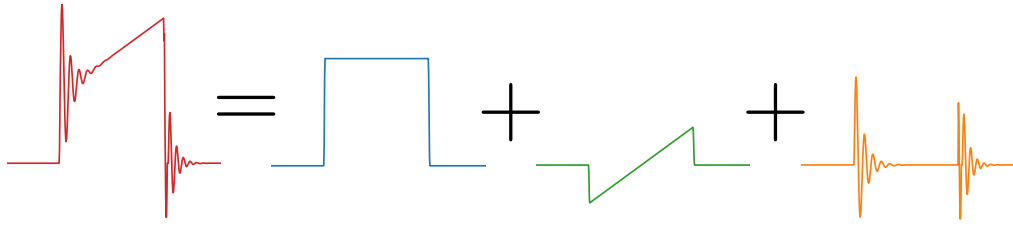


FIGURE 2.8 – Décomposition du courant I^+

de tension est exprimée en utilisant le transfert de charge :

$$V_{in} - \Delta V = L \frac{dI}{dt}(0^-) = \frac{\Delta Q_i}{C_{Pon}} \quad (2.14)$$

$$\Delta Q_i = (C_{gdn} + C_{dbn} + C_{gdp})V_{in} + (C_{gdn-i} + C_{dbn-i} + C_{gdp-i})V_{th} \quad (2.15)$$

L'extension X_{-i} est ajoutée à la valeur des capacités considérées à l'état précédent (*OFF*) pour prendre en compte le changement de capacités en fonction de la différence de tension qui leur sont appliquées.

La réponse du courant est calculée avec une méthode similaire (2.10),

$$I_4(t) = I_{out} + \frac{\Delta Q_4}{LC\omega_r} \sin(\omega_r t) e^{-\lambda t} \quad (2.16)$$

Le maximum de cette fonction est atteint à $t = \frac{1}{\omega_r} \arctan \frac{\lambda}{\omega_r}$ et vaut $I_{max} = I_{out} + \frac{\Delta Q_4}{LC\omega_r} \frac{1}{\sqrt{1+(\frac{\lambda}{\omega_r})^2}} e^{-\frac{\lambda}{\omega_r} \arctan(\frac{\omega_r}{\lambda})}$.

Les réponses temporelles du courant pendant chaque transition ont été détaillées. La réponse en fréquence est calculée à partir de ces équations. Puis les modèles de transition seront confrontés à la simulation et à la mesure.

2.2 Réponse fréquentielle

Le spectre de fréquence du courant I^+ est important pour comprendre les phénomènes intervenant dans l'analyse de la propagation (section 2.5).

Le courant d'entrée I^+ se décompose en trois parties :

1. un signal carré,
2. un signal en dents-de-scie,
3. un signal de bruit, composé des contributions présentées précédemment (sous-sections 2.1.3 à 2.1.6).

Cette décomposition est présentée dans la figure 2.8.

L'enveloppe spectrale du signal carré avec front montant (ou descendant) non idéal est calculée dans [14], la même approche est appliquée au signal en

dents de scie. Le résultat est présenté dans (2.17).

$$\begin{aligned} I_{sqr}(\omega) &= \frac{4I_{out}F_{clk}}{\omega} \sin\left(\frac{\alpha\omega}{2F_{clk}}\right) \\ I_{saw}(\omega) &= \frac{2\Delta I_x F_{clk}}{\omega} \left(-\cos\left(\frac{\alpha\omega}{2F_{clk}}\right) + \frac{2F_{clk}}{\alpha\omega} \sin\left(\frac{\alpha\omega}{2F_{clk}}\right)\right) \end{aligned} \quad (2.17)$$

with α the duty cycle and ΔI_x the current ripple.

L'équation du bruit réel doit être calculée avant de calculer la réponse en fréquence. La durée entre l'extinction de PMOS ① et l'allumage de NMOS ② est faible par rapport à la durée de la période. En conséquence, la contribution spectrale de la transition ① est négligée mais la condition initiale de la transition ② est modifiée. Le courant initial n'est pas 0A comme présenté dans la section 2.1.4 mais est égal à $I_{1f} = I_1(\delta t)$ avec δt le temps mort entre les transitions ① et ②. Enfin le courant est donné par (2.18),

$$I_2 = (I_{1f} \cos(\omega_r t) + \frac{1}{\omega_r} \left(\frac{\Delta Q_2}{LC} - \lambda I_{1f}\right) \sin(\omega_r t)) e^{-\lambda t} \quad (2.18)$$

La transformée de Fourier du signal de bruit permet d'obtenir l'enveloppe spectrale.

$$\begin{aligned} I_2(\omega) &= \frac{2F_{clk}}{(\lambda + j\omega)^2 + \omega_r^2} \left(\frac{\Delta Q_2}{LC} + I_{1f} j\omega\right) \\ I_4(\omega) &= \frac{2F_{clk}}{(\lambda + j\omega)^2 + \omega_r^2} \frac{\Delta Q_4}{LC} \end{aligned} \quad (2.19)$$

À la fréquence de résonance f_r ($\omega = \omega_r$), les amplitudes sont,

$$\begin{aligned} |I_{2r}| &= \frac{2F_{clk}}{\sqrt{\lambda^2 + 4\omega_r^2}} \sqrt{\left(\frac{\Delta Q_2}{\lambda LC}\right)^2 + I_{1f}^2 \omega^2} \\ |I_{4r}| &= \frac{2F_{clk}}{\sqrt{\lambda^2 + 4\omega_r^2}} \frac{\Delta Q_4}{\lambda LC} \end{aligned} \quad (2.20)$$

L'enveloppe est multipliée par un peigne de Dirac $\text{III}_{F_{clk}} = \sum_n \delta(\omega - 2\pi n F_{clk})$ pour obtenir le spectre réel. Les spectre est donc $(I_{env}(2\pi n F_{clk}))_{n \in \mathbb{N}}$.

Un autre mécanisme génère du bruit à plus haute fréquence : le couplage par le substrat.

2.3 Couplage substrat

Les MOSFET de puissance sont isolés pour éviter l'injection directe des charges dues aux commutations du SMPS dans le substrat. Cette isolation est réalisée en ajoutant une couche Deep N-Well sous les MOSFET de puissance comme présenté dans la figure 2.9. La jonction entre le substrat et la couche DNW peut être modélisée avec un condensateur.

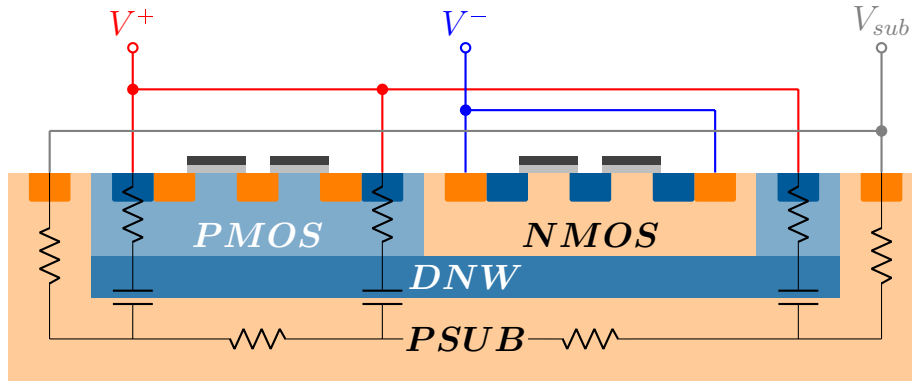


FIGURE 2.9 – Power stage cross-section

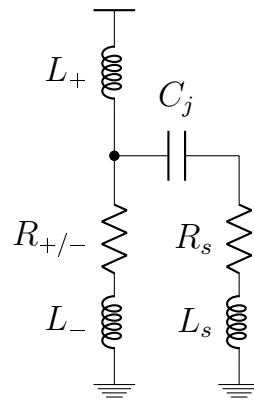


FIGURE 2.10 – Schéma des composants liés à la résonance avec le substrat

En conséquence, un nouveau RLC est impliqué lors de la commutation avec R, la résistance du substrat, L le boîtier et l'inductance parasite du PCB et C, la capacité de jonction. En raison de la différence des valeurs des capacités ($C_{+/-} \gg C_{+/-sub} = C_j$), les deux résonances peuvent être étudiées séparément. $C_{+/-}$ peut être négligé par rapport au condensateur de jonction DNW du substrat et aux autres impédances à la fréquence de résonance du substrat ($\sim 500MHz$). Le schéma équivalent est présenté dans la figure 2.10.

En considérant $(\frac{\omega}{\omega_l})^2 \gg 1$ à la fréquence de résonance avec $\omega_l = \frac{R_{+/-}}{L_-}$, on obtient :

$$R = R_s + \frac{R_{+/-}(L_+)^2}{(L_+ + L_-)^2}, \quad L = L_s + \frac{L_+L_-}{L_+ + L_-}, \quad C = C_j \quad (2.21)$$

Avec L_+ , L_- et L_s les inductances parasites sur les connexions à l'alimentation, à la masse et au substrat respectivement. R_s est la résistance équivalente du substrat entre les jonctions et les contacts métalliques.

Ce réseau RLC est stimulé par la variation de tension sur V^+ due aux commutations. La variation initiale de tension peut être obtenue en multipliant la dérivée du courant circulant de V^+ à V^- par l'inductance de la connexion à l'alimentation, L_+ . Il peut être compliqué de valider et d'utiliser ce résultat dans la pratique en raison de la faible amplitude de la variation de tension par rapport à la fréquence de résonance principale. Cependant, la résonance

du substrat est importante en termes de bruit en raison de sa fréquence plus élevée (impact sur les RF) et dont le chemin vers l'analogique pourrait être à faible impédance (les chemins de propagation seront présentés dans la section suivante 2.5).

2.4 Résumé de la génération du bruit

Que retenir de ce chapitre ?

1. Il y a trois fréquences de résonance sous la forme $f_r = \frac{1}{2\pi\sqrt{LC}}$: deux dues à l'inductance de la boucle de puissance du PCB et du boîtier, $L_+ + L_-$ et la capacité présentée dans (2.22) :

$$\begin{aligned} C_{Pon} &\approx C_{gdp} + C_{gsp} \\ C_{Non} &\approx C_{gdp} + C_{dbp} + C_{gdn} + C_{gsn} \end{aligned} \quad (2.22)$$

Et une autre fréquence de résonance est due à $L = L_s + L_+ // L_-$ (L_s inductance parasite de polarisation du substrat) et à la capacité de jonction C_j entre les couches NW et DNW reliées à V^+ avec le substrat relié à la masse PCB.

2. Il y a quatre transitions : lorsque PMOS et NMOS s'allument, les dépassements sont dus à l'appel de courant pour charger les capacités parasites. Ils sont proportionnels à V_{in} et à $C_{gn/p}$ donc à la largeur du MOSFET de puissance $W_{n/p}$. Le dépassement dû à la commutation du chemin de courant lors de l'arrêt du PMOS est fonction de I_{out} . Enfin, l'extinction du NMOS ne contribue pas de manière significative au bruit.

Les dépassements peuvent être limités en réduisant la force de la commande de grille et ainsi ralentir la charge des MOSFETs ou la chute de courant dans le canal PMOS. Cependant des solutions pour réduire le bruit sans changer la vitesse de commutation sont présentées dans le chapitre 3.

2.5 Propagation du bruit

Maintenant que la source du bruit, la commutation de l'étage de puissance et les fréquences de résonance associées ont été décrites, l'objectif est de comprendre comment ce bruit se propage jusqu'à l'IP victime.

Le spectre mesuré à la sortie victime est composé de **trois fréquences de résonance différentes**. L'une, décrite dans la section 2.1, est due au **au convertisseur buck** ($\sim 100MHz$). Un autre présenté dans la section 2.3, est dû à **capacité de jonction** NWell, Deep NWell du convertisseur MOSFET avec le substrat ($\sim 600MHz$). Et enfin, les fréquences de résonance apparaissent entre les deux sont ajoutées par **l'environnement de propagation**. En effet, les impédances parasites le long des chemins de propagation sont susceptibles de résonner avec stimulation du bruit. L'identification de ces impédances parasites ne fait pas partie de l'étude. Une analyse peut s'avérer difficile

en raison du grand nombre d'éléments à prendre en compte. Cependant, il y a deux voies prépondérantes : la propagation sur puce et la propagation sur circuit imprimé.

En **basse fréquence** (en-dessous de $\sim 400MHz$) le bruit se propage principalement à travers **des connexions PCB de l'alimentation et du plan de masse**. L'extraction du paramètre S en utilisant le plan de masse comme référence sous-estime la propagation du bruit dans ce plan de masse. D'autres configurations de ports ont été testées. Référence de port connectée à la masse absolue ou à la masse de la carte par exemple. En raison de la taille physique des ports (distance entre la broche et la référence), les modèles de paramètres S obtenus n'étaient pas passifs ce qui ne correspond pas à la réalité du PCB.

À **haute fréquence** (au-dessus de $\sim 400MHz$) le bruit se propage à travers **les interconnexions sur silicium** et surtout à travers l'anneau E/S. Les couches métalliques sont peu résistives et les inductances parasites du boîtier à cette fréquence sont haute impédance, ce qui empêche l'écoulement du bruit vers le plan de masse. L'analyse a été réalisée à l'aide de la suite logicielle CWS, *WaveIntegrity*, pour construire un modèle de propagation global. Les résultats montrent l'importance des modèles de source et de victime, mais un simple modèle des interconnexions suffit pour décrire la propagation. La polarisation du substrat tout autour de la puce ne modifie pas de manière significative la fonction de transfert entre la source et les broches de la victime. Ceci est dû à la haute résistivité du substrat dans cette technologie ($10\Omega.cm$) : le bruit ne se propage pas sur de longues distances à l'intérieur du substrat.

Le chapitre suivant présente des solutions ou des améliorations à apporter au système actuel pour réduire les émissions et la propagation du bruit dans l'ensemble du système.

3 Solution implementation

Dans le chapitre précédent, la génération de bruit, ainsi que la propagation du bruit ont été exposées. L'objectif de ce chapitre est de répondre à chaque point exposé précédemment.

Chacune des sections suivantes présente une solution pour réduire l'impact du bruit sur la victime. Il existe une solution pour les deux phénomènes de stimulation, le changement de chemin du courant développé dans la section 3.1, l'appel de courant pour charger les grilles développé 3.2. Enfin, une modification du routage des niveaux de métaux supérieures de la puce est envisagée afin de réduire la propagation du bruit dans la section 3.3.

3.1 Commutation douce du courant

La solution fonctionne sur la transition d'arrêt de PMOS ①. Comme expliqué dans la section 2.1.3, le dépassement de cette transition dépend du courant de sortie du convertisseur, I_{out} . Une description précise de ce qui se passe avant la commutation du courant est nécessaire pour comprendre la solution. Ensuite, le mécanisme de la solution est décrit et ainsi que son implémentation dans le véhicule d'essai.

3.1.1 Description de la commutation

Le comportement durant la commutation dépend de la résistance du contrôle de grille. Les situations de faible et de fort contrôles ($W_{large} = 15W_{slow}$) sont présentées dans les figures 3.1 et 3.2 respectivement.

Dans le cas de faible contrôle, la transition ① se découpe en quatre phases : (A) la grille est chargée à $V^+ - V_{th}$ ($V_{sgp} = V_{th}$), (B) le V_{lx} est déchargé de V^+ à $V^- - V_{th}$ puis (C) le courant est transféré vers la diode du NMOS et enfin (D) la grille est chargée à V^+ ($V_{sgp} = 0$).

Pendant la phase (A) et (B), le courant dû à la charge et à la décharge des capacités parasites I_C circule vers la sortie. En conséquence, le courant passant par le canal PMOS $I_{PMOS} = I_{out} - I_C$ est réduit. La réduction est encerclée sur la figure 3.1a.

Dans la figure 3.2a, le contrôle de grille est plus fort. En conséquence, le courant de décharge des capacités fournit la demande totale de courant de sortie, $I_C = I_{out}$. Il ne reste donc aucun courant dans le canal PMOS, $I_{PMOS} = I_{out} - I_C = 0A$. Le chemin du I_C est représenté dans la figure 3.2b.

3.1. Commutation douce du courant

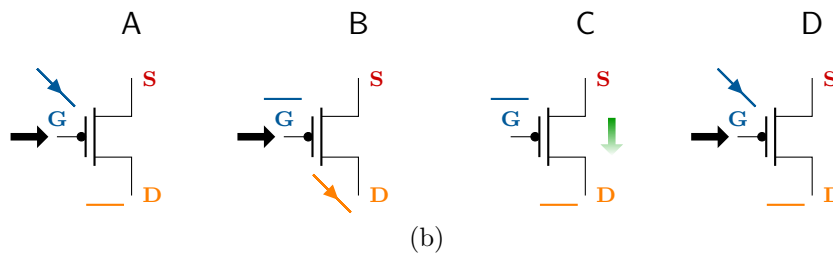
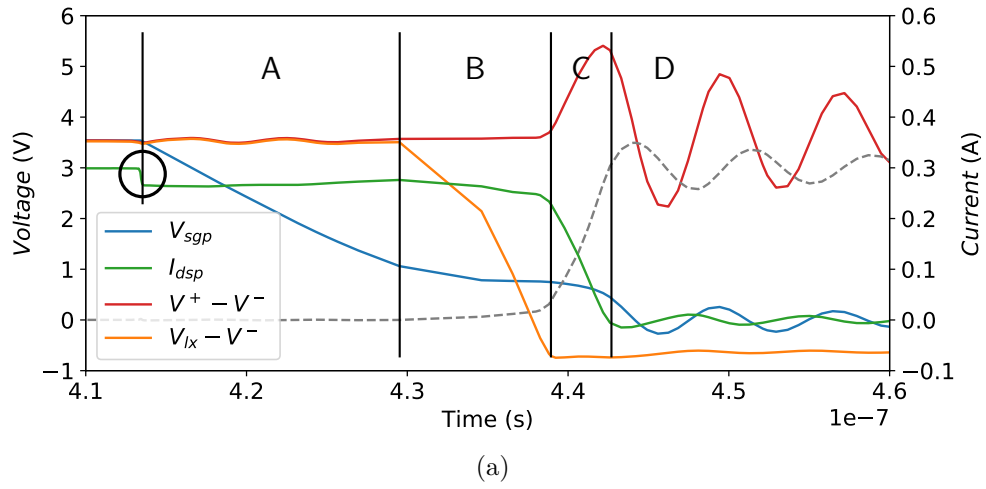


FIGURE 3.1 – Résultats de simulation de l'arrêt du PMOS (faible contrôle)

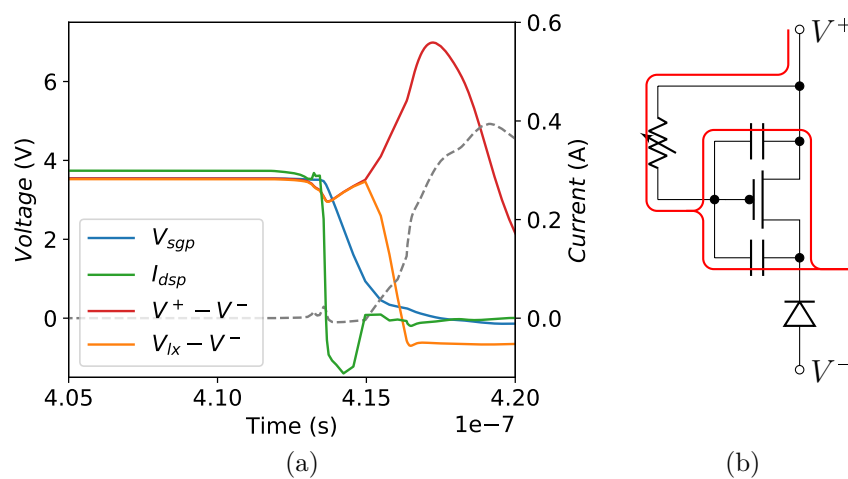


FIGURE 3.2 – Résultats de simulation de l'arrêt du PMOS (fort contrôle) (a) et schéma de l'écoulement des charges dans l'étage de puissance (b)

Dans les figures 3.1 et 3.2, deux différences importantes entre les configurations (faible et fort contrôle) peuvent être observées :

1. l'amplitude du bruit : un dépassement de la tension d'alimentation $V^+ - V^-$ de 3,4V avec un contrôle fort en opposition à 1,8V avec un contrôle faible,
2. le temps de commutation : dans le cas d'un contrôle faible, le temps de commutation est égal à 40ns contre seulement 4ns pour la configuration de fort contrôle.

La fluctuation de la tension d'alimentation est un problème en termes de bruit mais aussi en termes de fiabilité du MOSFET. Les MOSFET de la technologie STMicroelectronics 40nm sont dégradés par des surtensions sur leurs terminaux. Lorsque PMOS est éteint, sa grille et sa source sont à V^+ et son drain est à $V^- - V_{th}$, donc dans le cas d'un contrôle fort, la différence de tension atteint 7,5V.

Le temps de commutation a un impact sur les pertes de puissance pendant la transition mais aussi sur le rapport cyclique maximum que le système peut atteindre. Pour un convertisseur buck avec une fréquence de commutation de $F_{clk} = 2.4MHz$, un temps de commutation de 40ns consomme 10% de la durée de la période dans seulement une des quatre transitions. Par conséquent, le dimensionnement du contrôle de grille est un compromis entre la vitesse de commutation et le dépassement.

La solution exposée dans la section suivante, tente de tirer parti des deux configurations.

3.1.2 Mécanisme de la solution

Le courant du NMOS I_{dsn} est représenté par une ligne pointillé grise dans les figures 3.1 et 3.2. Lors d'une augmentation de I_{dsn} , le courant I^- de l'inductance parasite de masse L^- augmente (au détriment de I^+). La tension d'alimentation $V^+ - V^-$ fluctue en fonction de la pente de ce courant présentée dans (3.1).

$$V^+ - V^- = V_{in} - (L^+ - L^-) \frac{dI^+}{dt} \quad (3.1)$$

L'objectif est de contrôler la pente du courant lors de la commutation. En cas de contrôle lents, une partie du courant reste dans le canal PMOS pendant la transition. La pente du courant peut donc être modifiée en contrôlant la tension de grille du PMOS. La solution proposée est de réduire la vitesse du contrôle de grille pendant le changement du chemin de courant.

Le signal V_{lx} est utilisé comme déclencheur pour réduire changer de configuration car la tension V_{lx} chute avant que le courant ne commute (voir figure 3.3). Ensuite, le contrôle rapide est réactivé lorsqu'il ne reste plus de courant dans le canal du PMOS pour finir la transition.

Le mécanisme de la solution a été exposé, l'implémentation au niveau MOSFET peut être détaillée.

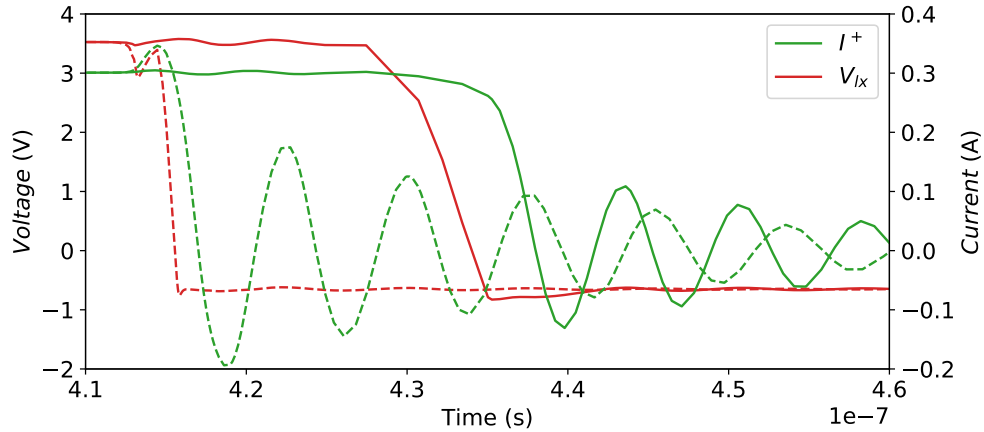


FIGURE 3.3 – Comparaison des commutations de I^+ et V_{lx} avec un contrôle faible (lignes continues) et un contrôle fort (lignes discontinues)

3.1.3 Implémentation de la solution

Le schéma de la solution implémentée est présenté figure 3.4. Les deux gros MOSFET représentent les MOSFET de puissance. Les signaux Cmd_N et Cmd_P sont générés par la commande système qui n'est pas représentée ici. Il y a un temps mort entre ces deux signaux pour éviter le court-circuit des MOSFET de puissance. Les signaux passent par une chaîne d'inverseur pour contrôler la porte des MOSFET de puissance.

La dernière étape du contrôle de la grille du PMOS est représentée séparément par M_3 et M_4 . M_3 est un petit MOSFET qui représente la configuration contrôle lent. M_3 peut être court-circuité par M_2 , un MOSFET plus large, en configuration contrôle rapide ($\frac{W_{M2}}{W_{M3}} = 50$ avec $W_{M2} = 117\mu m$). La grille de M_2 est égale à $smooth = Cmd_P \cdot (V_{lx} + Gate_P)$. La porte "or-nand" est personnalisée pour être assez forte pour contrôler la grille de M_2 . La porte "or-nand" est instanciée à la fin de la chaîne contrôle pour réagir sans délai de propagation à la baisse de V_{lx} .

Enfin M_1 est une petite copie du PMOS de puissance. Lorsque $Gate_P$ dépasse $V^+ - V_{th}$, la conduction du canal M_1 est arrêtée et la résistance R fait commuter le signal $Gate_{sense}$ à V^+ .

Un chronogramme est présenté figure 3.5.

Pendant la transition ①, Cmd_N est à V^- et Cmd_P passe de V^- à V^+ . $Gate_P$ commence initialement à V^- , puis augmente contrôlé par M_2 et M_3 (configuration rapide). Lorsque $Gate_P$ approche $V^+ - V_{th}$, V_{lx} passe de V^+ à $V^- - V_{th}$. Le drop éteint M_2 (signal $smooth$ à V^+) et la charge de la grille ralentit. Le courant I_{out} passe du canal du PMOS à la diode du NMOS en configuration lente. Lorsque le canal du PMOS est ouvert, le signal $Gate_{sense}$ monte à V^+ et active M_2 pour finir la transition.

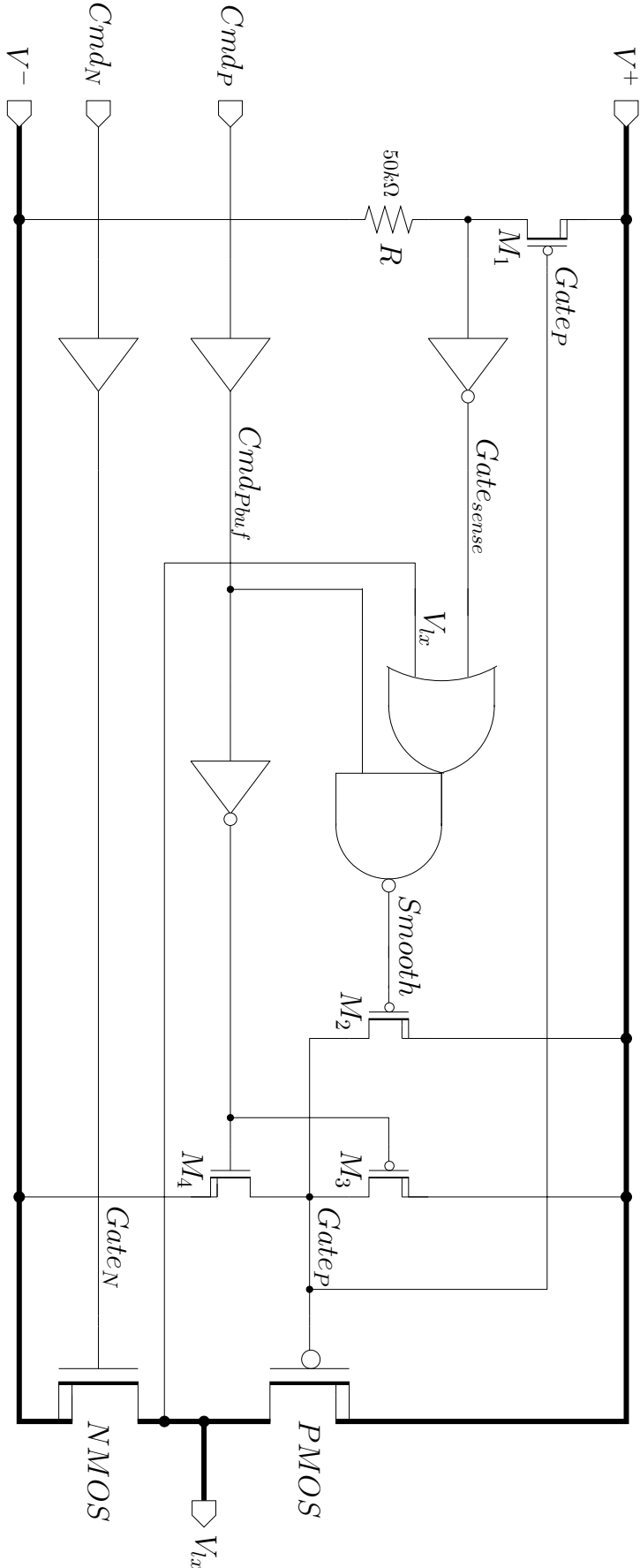


FIGURE 3.4 – Schéma de la solution de commutation douce

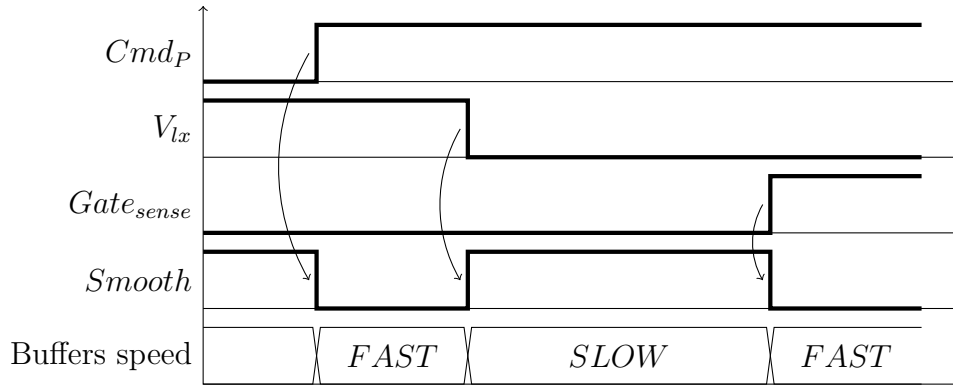


FIGURE 3.5 – Chronogramme des signaux de contrôle de la solution de commutation douce

3.2 Injection de charges par capacité commuté

La deuxième solution proposée est centrée sur l’activation du PMOS ④. Comme expliqué dans la section 2.1.6, le dépassement est dû à l’appel de courant pour décharger la grille, le dépassement dépend donc de V_{in} . Pour comprendre le mécanisme de la solution, il est important de faire un bref rappel sur cette transition.

3.2.1 Description de la commutation

Des résultats de simulation de l’allumage du PMOS ④ sont présentés figure 3.6.

La transition est composée de quatre phases : la grille du PMOS est déchargée à $V^+ - V_{th}$ ($V_{sgp} = V_{th}$) (A), puis le courant augmente dans le canal du PMOS jusqu’à I_{out} (B), ensuite puisqu’aucun courant ne traverse la diode corps NMOS, le V_{Lx} augmente à V^+ et enfin la grille est déchargée à V^- (D).

Cette dernière phase (D) génère un courant d’appel pour charger la capacité de la porte en créant un dépassement sur I^+ .

3.2.2 Mécanisme de la solution

L’objectif est de créer un réservoir de charge sur puce qui alimente la grille lors de la commutation et se recharge lentement pendant le reste de la période.

Une première solution consiste à ajouter une capacité de découplage sur puce, mais pour être efficace, cette capacité doit être large par rapport à la capacité de grille du PMOS. En raison de la grande taille du PMOS, sa capacité de grille est de $\sim 200pF$. Un condensateur nettement supérieur à $200pF$ nécessiterait une grande surface de silicium, ce qui est coûteux.

Une deuxième solution est une structure à capacité commutée. La capacité se décharge sur la grille pendant la transition et se recharge lentement pendant le reste de la période comme présenté dans la figure 3.7. Le contrôle de grille du PMOS la décharge de V_{th} et V_{Lx} augmente à V^+ (figure 3.7a). Les charges

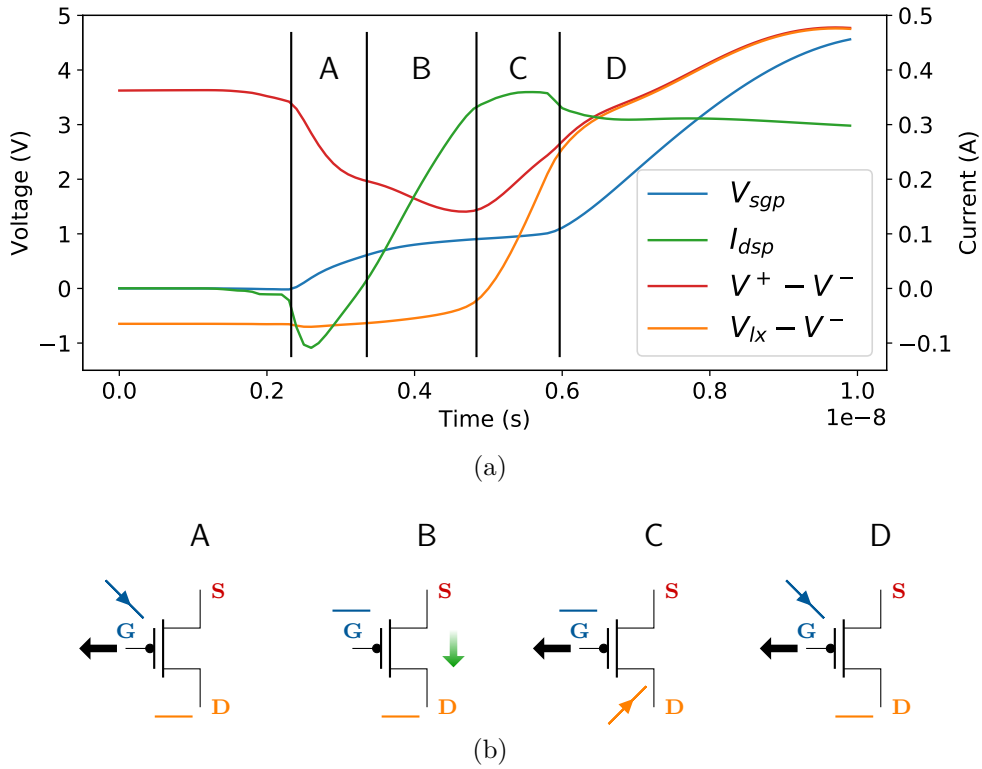


FIGURE 3.6 – Résultats de simulation de l’allumage du PMOS ④

sont injectées sur la grille (figure 3.7b). Le contrôle termine la décharge à V^- (figure 3.7c).

Les charges dans le PMOS Q_{MOS} et dans la capacité commuté Q_{SC} sont,

$$Q_{MOS} = 2C_g(V^+ - (V^+ - V_{th})) = 2C_gV_{th} \quad (3.2)$$

$$Q_{SC} = C_i(V^+ - V^-) \quad (3.3)$$

À la fin de la phase d’injection, les charges sont réparties entre toutes les capacités donc V_{sgp} vaut,

$$V_{sgp} = \frac{Q_{MOS} + Q_{SC}}{2C_g + C_i} = \frac{2C_gV_{th} + C_i(V^+ - V^-)}{2C_g + C_i} \quad (3.4)$$

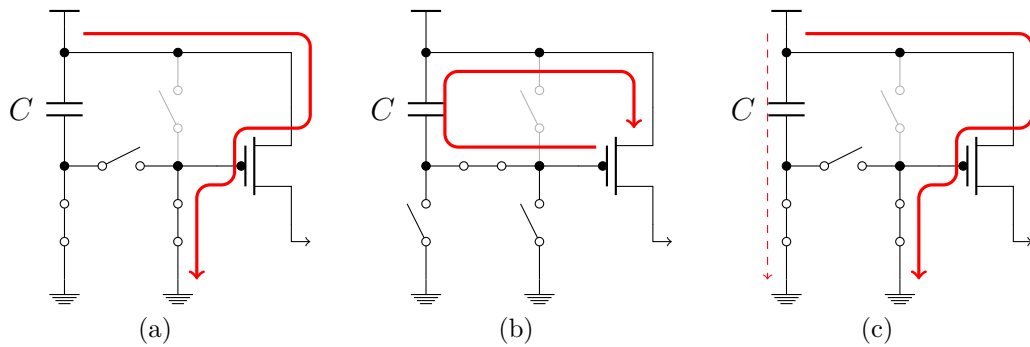


FIGURE 3.7 – Schéma de principe de la structure à capacité commuté

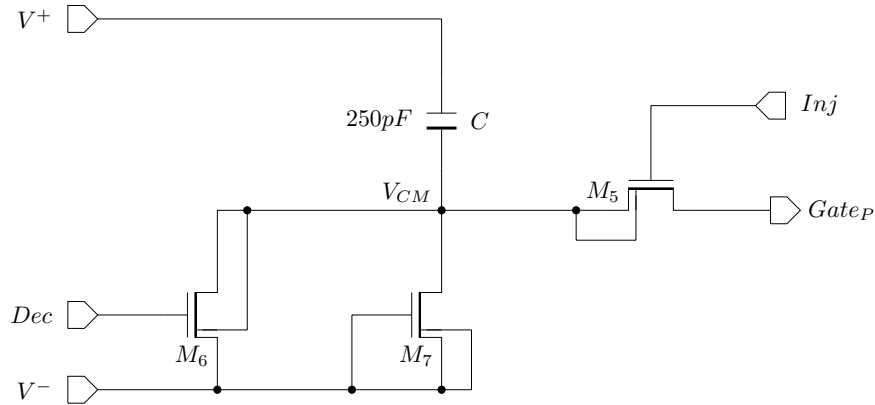


FIGURE 3.8 – Schéma de la solution à capacité commutée

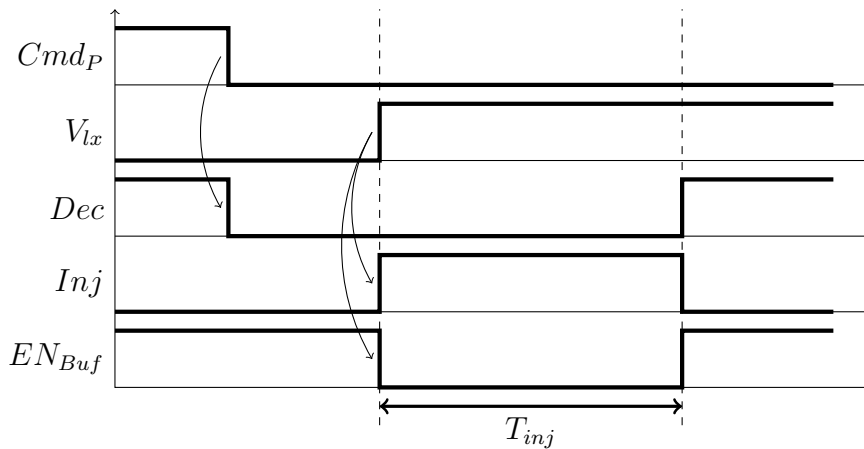


FIGURE 3.9 – Chronogramme des signaux de la solution à capacité commutée

En conséquence avec une capacité commutée $C_i = 2C_g \approx 200pF$, la tension de grille $V_{sgp} = \frac{1}{2}(V_{th} + V^+ - V^-)$. La moitié de la charge nécessaire à la commutation a donc été injectée.

Pendant l'injection, la grille et la capacité commutée sont déconnectées de l'alimentation. Il n'y a pas d'appel de courant pour recharger rapidement la capacité commutée. Cette capacité est ensuite reconnectée à l'alimentation par une grande résistance pour réduire l'appel de courant. La solution peut être considérée comme une résistance d'amortissement variable sur une capacité de découplage : lorsque le système a besoin de charges, la résistance est faible pour répondre rapidement à la demande mais la résistance est plus importante pour recharger la capacité afin de limiter la demande en courant.

3.2.3 Implémentation de la solution

Le schéma de la solution est représenté figure 3.8.

Un chronogramme des deux signaux Dec et Inj est représenté figure 3.9.

Le signal Dec est désactivé avec Cmd_P pour éviter la décharge du condensateur due à la variation d'alimentation avant l'injection. La grille est déchargée à $V^+ - V_{th}$ (A) et le courant passe au canal PMOS (B) puis le V_{lx} monte à V^+

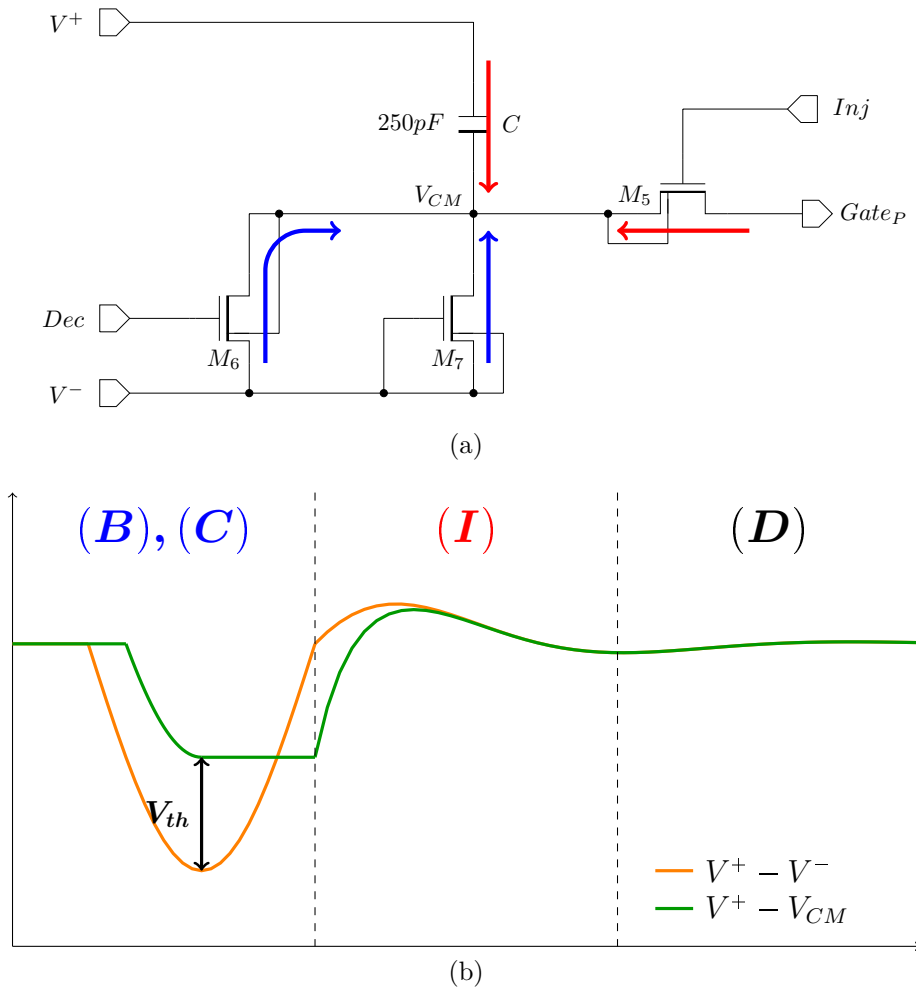


FIGURE 3.10 – Schéma de la solution d’injection de charge (a) et explication de l’annulation des oscillations (b)

(C) à ce moment le contrôle de grille est désactivé et la capacité est connectée à la grille pendant $T_{inj} = 3ns$ (réglé par simulation).

La grande fluctuation de la tension d’alimentation active le MOSFET M_6 . La capacité est partiellement déchargée pendant les phases (B) et (C). Par conséquent, peu de charges sont effectivement injectées et la solution ne réduit pas le niveau de bruit plus qu’une simple capacité de découplage de la même taille. Mais pendant le test de la solution, un effet secondaire annulant les oscillations a été observé. En conséquence, la solution est centrée sur cet effet secondaire présenté dans la figure 3.10.

Lorsque C_{mdP} chute, le signal Dec est à V^- , de sorte que les deux MOSFET M_6 et M_7 fonctionnent comme des diodes (avec une tension de seuil de V_{th}). En raison des fluctuations de la tension d’alimentation, la capacité C est déchargée pendant les phases (B) et (C) (flèches bleues). Lorsque V_{lx} monte, le contrôle est désactivé mais les signaux Dec et Inj sont activés pour un temps fixe ($3ns$). La phase (I) dans la figure 3.10. L’excédent de charges dû à l’appel de courant est utilisé pour recharger la capacité C et pour décharger la

grille du PMOS (flèches rouges). La demande de charge de la capacité absorbe l'excès dû au dépassement du courant et annule l'oscillation. Enfin, le contrôle est réactivé et le signal Inj désactivé pour terminer de décharger la grille du PMOS (D).

Les solutions pour réduire l'émission de bruit ont été exposées, la prochaine section travaille sur les chemins de propagation au sein de la puce.

3.3 Réduction de la propagation interne

L'objectif de cette solution est la réduction des chemins de propagation sur puce. L'impédance du chemin entre la source et la victime doit être supérieure à l'impédance du chemin vers le plan de masse du circuit imprimé pour évacuer le bruit à l'extérieur de la puce par la masse au lieu de polluer la victime.

Le principal chemin de propagation sur la puce est l'anneau d'E/S. Une vue globale de la puce avec les chemins de propagation est présentée dans la figure 3.11. Les flèches rouge et bleue représentent la propagation du bruit à travers les interconnexions d'alimentation et de masse. Ces deux voies sont externes : le bruit passe à travers le PCB pour atteindre la cellule victime. Le chemin vert est interconnecté tout autour de la puce par l'anneau d'E/S pour polariser le substrat. La propagation du bruit par le substrat est facilitée par ces interconnexions métalliques.

La solution naturelle est de couper l'anneau d'E/S près de la source de bruit pour isoler cette partie du réseau de polarisation du substrat du reste du circuit. En isolant le substrat du convertisseur buck, la polarisation n'est pas garantie, donc la tension peut varier localement et la jonction avec le substrat peut être activée. Par conséquent, une E/S dédiée à la polarisation du substrat du convertisseur buck est nécessaire. La solution est représentée dans la figure 3.11b.

Les solutions investiguées au cours de cette thèse ont été décrites. Le prochain chapitre dresse un bilan de ce travail et propose des pistes de développement pour les futures recherches sur le sujet.

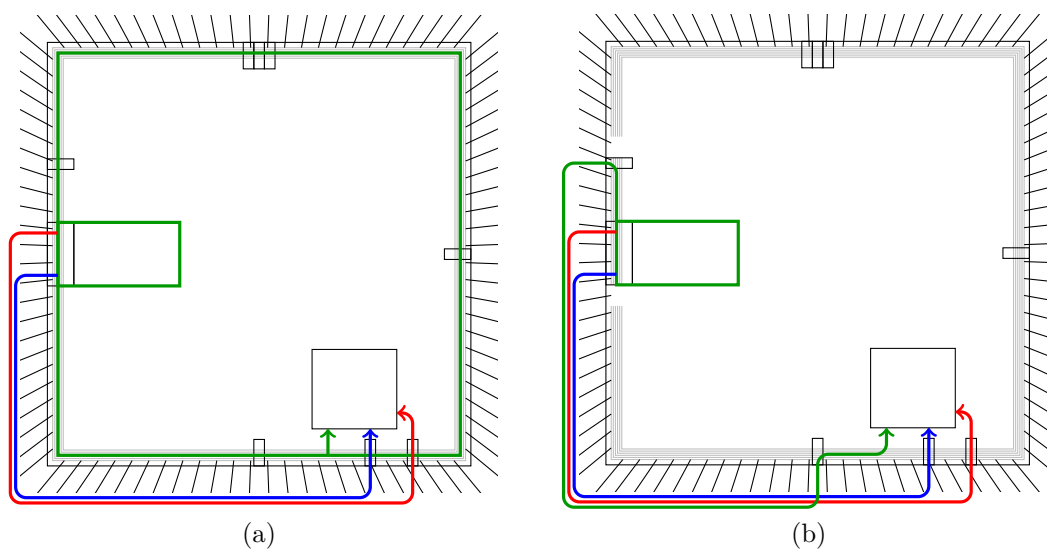


FIGURE 3.11 – Vue globale du circuit avec un anneau d'E/S continue (a) ou discontinue (b)

4 Conclusion

Synthèse

L'objectif de ce travail était d'analyser le mécanisme de pollution d'un convertisseur DC/DC sur des IP analogiques sensibles intégrées dans un SoC et de développer des techniques de minimisation pour réduire le bruit du convertisseur de buck.

L'objectif a été divisé en trois parties : d'abord l'analyse du bruit généré par l'étage de puissance du convertisseur, puis l'étude des chemins de propagation vers la victime et enfin, sur la base de ces résultats, mettre en œuvre des solutions réduisant la génération ou la propagation de ce bruit.

Analyser le bruit de commutation du convertisseur signifie déterminer la fréquence de résonance du bruit, l'amplitude du bruit et relier ces deux valeurs aux paramètres du convertisseur. L'étage de puissance et son environnement ont été simplifiés à un simple réseau RLC. Le R, le L et le C ont été déterminés par l'extraction du réseau parasite dans chaque état du convertisseur buck et les conditions initiales de ces schémas équivalents ont été déterminées par une analyse des transitions entre les états.

Le R était principalement dû à la force du tampon, le L était situé dans le boîtier et dans les interconnexions d'alimentation et de mise à la terre des circuits imprimés, et enfin le C était composé des capacités de grille des deux MOSFET de puissance.

Il y a eu quatre transitions : la mise sous tension des PMOS et des NMOS dont les dépassements étaient dus à la décharge et à la charge des capacités de la porte MOSFET de puissance et dépendaient du niveau de tension d'alimentation, la mise hors tension des PMOS dont le dépassement était dû au passage du courant du canal PMOS au canal NMOS et dépendant du niveau du courant de sortie et enfin la mise hors tension des NMOS dont la contribution était négligeable en comparaison des contributions des autres transitions.

Une autre fréquence de résonance a été signalée : la capacité de jonction entre l'alimentation du convertisseur Buck et la polarisation du substrat résonne avec l'inductance parasite du boîtier et du PCB. Ce réseau parasite a été stimulé par les fluctuations de la tension d'alimentation du convertisseur Buck.

La compréhension de la propagation s'est faite en deux étapes. Tout d'abord, l'ensemble du système (l'ensemble du circuit intégré, le boîtier et le circuit imprimé) a été modélisé à l'aide de la suite logicielle CWS, *WaveIntegrity* et comparé aux mesures pour vérifier et corriger le modèle. Ensuite, l'environne-

ment du convertisseur de buck a été modifié en simulation pour comprendre le poids de contribution des différentes voies de propagation.

A basse fréquence (moins de $\sim 400MHz$), le bruit se propageait principalement à travers la connexion d'alimentation PCB et le plan de masse. L'extraction du paramètre S à partir du plan de masse comme référence a sous-estimé la propagation du bruit dans le plan de masse. Le modèle a été corrigé en ajoutant une impédance sur la connexion du plan de masse à la masse idéale.

A haute fréquence (au-dessus de $\sim 400MHz$), le bruit se propageait à travers les interconnexions sur puce. En raison de la résistivité élevée du substrat dans la technologie, le bruit ne se propageait pas sur de longues distances à l'intérieur du substrat, mais par l'anneau E/S. Les couches métalliques étaient peu résistives et les inductances parasites du colis à cette fréquence étaient de haute impédance, ce qui permettait d'éviter le bruit à évacuer par le plan de masse.

Enfin, des solutions pour réduire l'impact sonore ont été étudiées. Les premières solutions pour réduire la génération de bruit ont été présentées. La réduction de l'intensité du tampon a réduit le bruit généré par la commutation MOSFET de puissance, mais au prix d'un temps de commutation plus long. Une solution avec une force de tampon variable a été expérimentée permettant de commuter rapidement la tension de grille mais de lisser le passage du courant du canal PMOS au canal NMOS. Le temps de commutation est réduit par rapport à la petite configuration du tampon, mais avec une amplitude de prise de vue inférieure équivalente.

Une autre solution était d'ajouter un condensateur de découplage mais cette solution était limitée par la contrainte de surface et le condensateur n'était pas très important comparé à la demande de charge de la capacité de grille aux transitions. Une solution permettant d'annuler les sonneries. La recharge du condensateur de découplage a été décalée dans le temps pour absorber l'excès de charge dû à l'oscillation du réseau parasite.

Une dernière solution a été présentée : réduire les voies de propagation. Le réseau de distribution d'énergie des circuits imprimés pourrait être optimisé, mais dans le contexte des microcontrôleurs, le circuit imprimé est conçu par le client de sorte que les recherches se sont concentrées sur les voies de propagation internes. La solution présentée est d'avoir deux réseaux de polarisation différents du substrat. En raison de la haute résistivité du substrat, le bruit a été évacué par le circuit imprimé au lieu des voies internes, ce qui a réduit l'impact de ce bruit sur la victime.

Perspectives

Un circuit de test a été conçu et envoyé en fabrication avec le convertisseur Buck, une référence de tension et un ADC. Tout d'abord, une configuration en boucle ouverte a été mise en œuvre pour séparer les transitions, en particulier l'arrêt de PMOS de l'allumage de NMOS afin de terminer la validation du modèle. Deuxièmement, les solutions présentées précédemment ont été mises en

œuvre. Les mesures du circuit permettront de vérifier l'efficacité des solutions de réduction du bruit et indirectement des modèles.

Dans un travail futur, le lien entre les paramètres du convertisseur et l'augmentation du plancher de bruit à la sortie de l'ADC pourrait être étudié. Le résultat dépendra de l'architecture ADC choisie.

Les solutions proposées dans ce travail pourraient être améliorées : le contrôle de grille à vitesse variable doit être adaptée à la susceptibilité au bruit de la victime et la solution d'annulation des oscillations pourrait être adaptée aux autres transitions (uniquement faite pour l'activation de PMOS dans ce travail). D'autres solutions peuvent être étudiées, notamment au niveau du système, par exemple en faisant de l'étalement spectral sur fréquence de commutation du convertisseur Buck.

Les travaux exposés dans ce manuscrit répondent à l'objectif exposé précédemment : analyser la génération de bruit et sa propagation dans le système et proposer des solutions pour réduire ce bruit.

Seules quelques études ont été rapportées sur le sujet dans le contexte spécifique de l'intégration SMPS et ne propose aucun lien entre les paramètres de conception et le niveau de bruit dû à l'activité de convertisseur de buck. Ces travaux ont contribué à répondre à cette absence en proposant un modèle d'estimation de la génération et de la propagation du bruit en fonction des paramètres du système.

La première solution (commande de grille variable) a déjà été intégrée dans l'un des microcontrôleurs de STMicroelectronics pour répondre à un problème de fiabilité. En limitant le dépassement, le stress des MOSFETs de puissance est réduit.

De plus, la génération de bruit des SMPS intégrés au sein d'un microcontrôleur est un enjeu majeur pour les futurs produits qui embarqueront des IP analogiques plus précise ainsi que des émetteurs RF. Ces travaux donnent les clés pour répondre à cette problématique industrielle et les solutions proposées peuvent être un marqueur permettant à STMicroelectronics de se différencier sur le marché des microcontrôleurs.

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AUTORISATION DE SOUTENANCE

Vu les dispositions de l'arrêté du 25 mai 2016,

Vu la demande du directeur de thèse

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Ecole doctorale ELECTRONIQUE, ELECTROTECHNIQUE, AUTOMATIQUE

Fait à Ecully, le 29 mars 2019

P/Le directeur de l'E.C.L.
La directrice des Etudes

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