Design of millimeter-wave receivers for embedded automotive radars

Hugo Vallée

université de BORDEAUX

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Présentée par
Hugo Vallée

Dirigée par le *Professeur Thierry Taris*, Bordeaux INP

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Laboratoire d'Intégration du Matériau au Système Bordeaux, France
NXP Semiconducteurs, Toulouse, France

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Conception de récepteurs millimétriques pour des applications radars automobiles embarqués

Design of millimeter-Wave Receivers for Embedded Automotive Radars

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Après avis de :

M. Sylvain BOURDEL	Professeur	Grenoble INP	Rapporteur
M. Domenico ZITO	Professeur	Aarhus University	Rapporteur

Devant la commission d'examen formée de :

M. Jean-Baptiste BEGUERET	Professeur	Université de Bordeaux	Président
M. Xavier HOURS	Ingénieur	NXP Semiconductors	Examinateur
M. Christophe LANDEZ	Ingénieur	NXP Semiconductors	Examinateur
M. Gilles MONTORIOL	Docteur	NXP Semiconductors	Invité co-encadrant
M. Thierry TARIS	Professeur	Bordeaux INP	Directeur de thèse

Résumé

Conception de récepteurs aux fréquences millimétriques pour des applications radars automobiles embarqués

Depuis plusieurs années, l'industrie automobile multiplient les systèmes d'aide à la conduite dans l'objectif d'améliorer l'autonomie des véhicules. Pour cela, chaque véhicule intègre un panel de capteurs de plus en plus étoffé. Le radar 80GHz embarqué présente alors des avantages multiples : immunité aux conditions extérieures, mesure simultanée de la distance et la vitesse... Ainsi, l'industrie du semiconducteur se trouve face à deux défis : réduire le coût des puces et améliorer leurs performances. Cela passe par l'utilisation de technologie CMOS avancées et, par l'amélioration des principaux facteurs de mérite du radar comme la puissance de sortie de son transmetteur, le bruit de phase de son oscillateur local et le facteur de bruit de son récepteur. L'objectif de cette thèse est de proposer des architectures et topologies susceptibles d'améliorer significativement les performances d'une récepteur radar.

Dans ce cadre, le récepteur radar est soumis à deux contraintes qui peuvent être contradictoires. Placé derrière le pare-chocs, le module radar est affecté par la réflexion du signal transmis. Face au risque d'apparition de non linéarités, donc de fausses cibles, de fortes contraintes sont exigées en termes de point de compression. De l'autre côté, pour réduire le facteur de bruit globale du récepteur, il y a besoin de maximiser le gain et minimiser le facteur de bruit de sa partie millimétrique. Pour répondre à cela, cette thèse propose plusieurs pistes.

Le premier axe est centré sur les techniques de conception de circuits millimétriques. D'un côté, il s'agit de réduire la consommation des circuits au travers d'étages complémentaires et l'opération en moyenne inversion. De l'autre côté, il s'agit d'implémenter des techniques d'annulation de bruit. Ces techniques permettent simultanément de travailler sur de larges bandes passantes et d'améliorer les performances en bruit. Cela a amené au développement d'une topologie dite « complémentaire à couplage transversale capacitif ».

Le second axe de ce travail se concentre sur les techniques de mélange. Les mélanges actifs présentent un bon compromis entre gain, linéarité et facteur de bruit mais également un bruit en 1/f élevé, malgré l'implémentation de techniques pour le réduire. Ces topologies peuvent adresser des applications de RADAR courte portée mais pas longue portée. Les mélangeurs passifs présentent de meilleures performances en bruit mais sont plus contraignants en termes de linéarités. Pour cela, cette thèse propose d'implémenter un mélangeur en courant à 80GHz pour améliorer simultanément les performances en bruit et linéarité, capable d'adresser des applications RADAR longue portée.

Mots clés : radar, amplificateur à faible bruit, mélangeurs, millimétrique, radiofréquence,

Abstract

Design of millimeter-Wave Receivers for Embedded Automotive Radars

Since few years, automotive industry implements more and more advanced driven assistance systems to improve safety and autonomy of vehicles. To achieve high autonomy level, each vehicle may include more and more sensors. The embedded 80GHz radar presents many advantages for car manufacturers: great immunity to outdoor conditions, real-time measurement of distance and velocity... To face such requirements, semiconductor industry has to simultaneously reduce cost and improve radar performances. It requires first to use advanced CMOS technologies (40nm, 28nm and smaller nodes). However, the main figures of merit should be improved such as the output power of the transmitter, the phase noise of the local oscillator and the noise figure of the receiver. The objective of this thesis is to propose new architectures and topologies able to improve the radar receiver performances.

In an automotive context, the radar receiver face two main issues. Mounted behind the bumper, the radar module is impacted by the reflection of the transmitted signal. It may cause non linearities in the demodulation chain thus creating false targets. For this reason, the level of linearity is high, especially regarding the compression point and the limited front end (FE) gain. The improvement of the RADAR sensitivity requires both to maximize the FE gain and to minimize the noise figure (NF) of the receiver front-end. To face such contradictory specifications about the FE gain, this thesis works on more advanced design techniques and topologies.

In this thesis, a specific focus is proposed on two design techniques. First, the circuits are designed to improve their efficiency (g_m/I_D) by operating in the moderate inversion region which contributes to reduce the power consumption. Secondly, the common-gate based noise cancelling technique is explored at 80GHz. This topology achieves simultaneously a wideband behavior and a low noise figure. It leads to develop a topology called "complementary capacitor cross-coupled" which achieves high RF performance at a reduced power consumption with respect to the operating frequency.

Besides this thesis studies various mixing approach to determine the best suited for radar applications. First, considering its interesting performance trade-off in BICMOS technology implementations, active mixers are explored. Whereas the level of 1/f can allow for short range operations, it is too large for long range RADAR. To address this issue, passive mixers are then studied. They achieve better noise performances but severely impact the linearity performances. To overcome this drawback, an 80GHz current mode mixer featuring noise and linearity improvement is developed.

Keywords: radar, low noise amplifier, mixer, millimeter-Wave, radiofrequency

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Contents

Chapter 1. 77GHz Embedded Automotive Radar

Since few decades, automotive industry moves to safer and autonomous cars. In this way, car manufacturers integrate more and more advanced driver assistance systems to monitor car vicinity. In this chapter, some generalities of radar markets are first proposed, specific focus is then proposed on modern modulations for automotive radar. The third section details the constraints and specifications of a 77GHz radar receiver. Finally, some specific points are opened in the last section.

I. Radars in automated vehicles

Since few years, Automotive industry is hugely working on safer and more autonomous vehicles. The main trend of vehicle automation is presented in section 1 while the constraints on automotive radar are detailed in section 2. Finally, a quick description of the different automotive radars is proposed in section 3.

1. Introduction to automated vehicles

This section proposes a brief overview of automated vehicle and draws the context where automotive radars take place. First, a top-level outline of automation levels is first proposed. To reach vehicles to the highest level, different sensors are proposed with their own advantages and drawbacks as presented in section b. Finally, section c details the different architectures of sensor data fusion.

a. Automated vehicles trends

The next decades will present many challenges for automotive industries. First, safety is a major concern as 1 million people died each year in road crash due to human error [1]. Besides, traffic congestion becomes an issue for many cities and will cost more than 4 billion dollars to the western economies between 2013 and 2030 [2]. According European Commission, transportation represents 25% of all European CO_2 emissions [3] while environmental issues lead to change our mobility and reduced greenhouse gas emissions. To face those challenges, Automated Vehicles *(AV)* are a promising solution [4]. A more efficient driving should reduce both the risk of accident and the traffic congestion. Besides, safer vehicles allow car

manufacturers to reduce the physical protections and, finally, their weight which is highly correlated to CO_2 emissions. Finally, AV open up to new mobility paradigms.

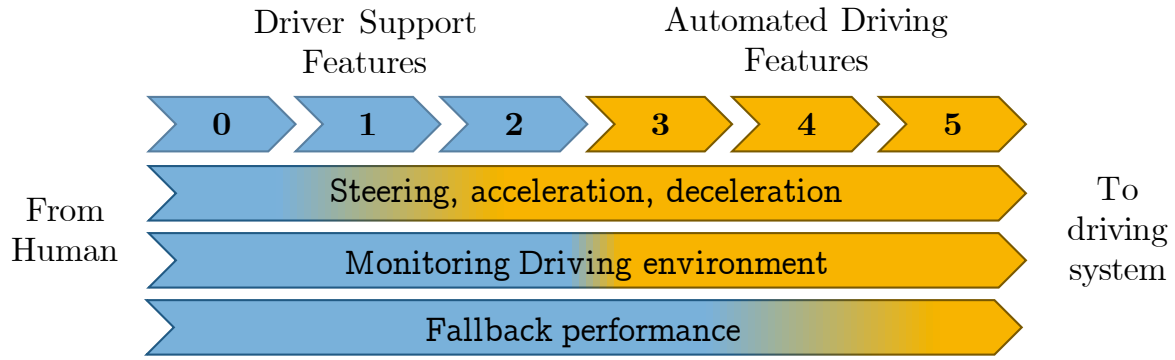


Figure 1 – Levels of Driving Automation defined by SAE J3016

The Society of Automotive Engineers proposes a classification of automation levels for vehicles from 0 to 5 [5]. A quick description is proposed:

- Level 0 – No automation: Human driver performs all the *dynamic driving tasks*, safety features only provide warning or momentary assistance such as *Automatic Emergency Breaking*, *Blind Spot* or *Lane Departure* warning,
- Level 1 – Driver assistance: Human still drive and monitor the environment but features proposes assistance for basic driving nodes like *cruise control* or *lane centering*,
- Level 2 – Partial automation: The car can drive in some driving modes, but human driver must constantly monitor the environment and be ready to take control,
- Level 3 – Conditional automation: Automated system can drive under limited conditions (ex. *Traffic jam chauffer*) but human must drive when feature requests,
- Level 4 – High automation: The automated driving system performs all driving task in many driving circumstances,
- Level 5 – Full automation: Automation system can drive anywhere in all condition using only its own systems.

b. Sensors in automated vehicles

To reach to SAE level 5, autonomous cars manufacturers require a continuous and ubiquitous monitoring of the car environment. To address this purpose different technologies are proposed. The most popular, reported in Table 1, are: lidar, radar and secure vehicle-to-environment communication *(V2X)*. Since these technologies provide a unique and different benefit, they are not concurrent but complementary [6].

Table 1 – Comparison of the proposed sensors for automated driving

Technology	Lidar	Radar	Camera	Secure V2X
Range	Up to 200m	Up to 300m	±	+
Distance Estimation	Time of Flight	Time of Flight	Indirect	Indirect
Velocity Estimation	Indirect	Direct	Indirect	Indirect
Angular Separation	$< 0.25°$	$\approx 3°$	Megapixels	Indirect
Outdoor conditions	Limited for weather, Good for night	Through all weathers, night...	Very limited	Through all weathers, night...
Colour pattern	Intensity only	No	Yes	No
Best for	Simultaneous Localization and Mapping	Reliable in all weather, speed measurement	Object classification, sign reading	Safe connection to X (Traffic Lights, cars...)

Lidar technology uses a pulsed laser to illuminate the target and to measure the reflected pulses to evaluate the distance. Achieving high accuracy, Lidar is used to make a digital map of the car environment. Nevertheless, lidar is not yet industrialized with concurrent technologies: solid-state lidar, MEMS mirrors, optical phase arrays... and remains expensive, up to more than ten thousand euros.

Radar systems use the reflection of Electro-Magnetic *(EM)* waves on objects to determine its distance, velocity and angle. Thanks to its great immunity to outdoors conditions (luminosity, rain...) and its high detection range, radar is a key element for detecting objects. To replace Lidar solutions for 3D cloud mapping, Imaging Radars *(IR)* are a promising solution. Implementing a Multiple-Input Multiple-Output architecture, IR provide an angular resolution lower than 1°. Even it's not as performant as lidar as illustrated in Figure 2, IR has a very competitive cost.

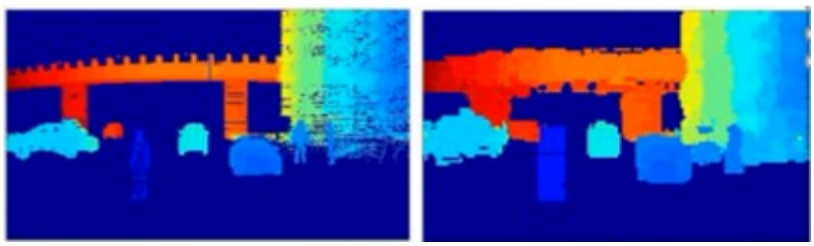


Figure 2 – Cloud map of car environment with Lidar and high-resolution radar [14]

The automotive CMOS image camera is a crucial sensor for automated driving. Thanks to its high megapixel resolution and the colour information, cameras are extremely superior for object recognition and classification, lane tracking, signalization analysis... Very different from consumer electronics, CMOS automotive image sensors have specific needs such as a high dynamic range, an improved sensitivity, a lower resolution, a faster response time.

In addition to other sensors, V2X can also help to automated driving by connecting the car to nearby infrastructure (traffic lights...), vehicles or pedestrians. With the exchange of data on vehicle position, traffic signal, accidents or congestions, autonomous cars can anticipate the situation and make relevant choice.

c. Sensor data fusion

As presented in section b, each sensor technology has pro and cons. Hence a fully autonomous car requires combining the data of various sensors to improve the perception of the environment, and to improve the relevance of decision. Since few years, various systems of sensor data fusion are proposed [7].

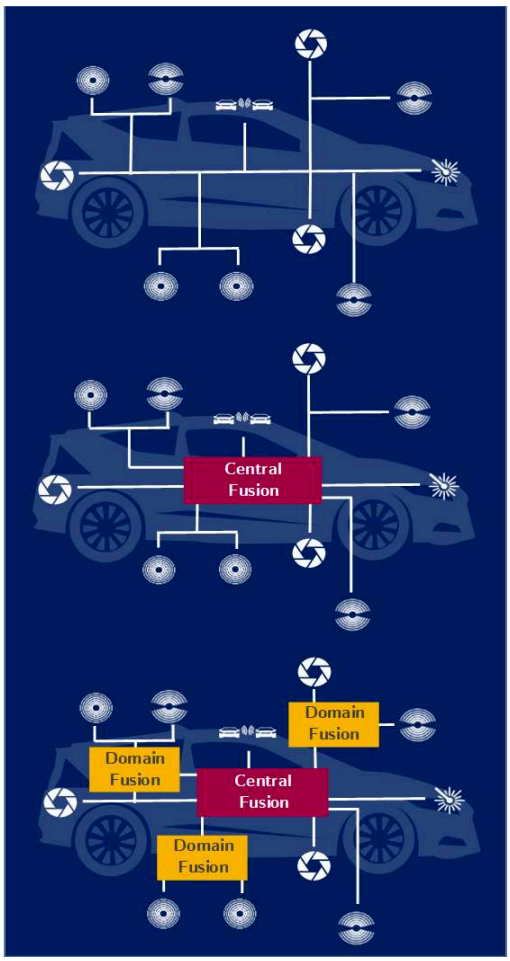


Figure 3 – Data fusion possible topologies [7]

On *Distributed Fusion*, data fusion and decision process are done locally at sensor module level with all the data of the other sensors. This option has several disadvantages: high complexity of sensors, expensive data processing for each sensor, low level of interoperability.

On *Centralized Fusion*, all raw data of naive sensor are processed in a central server which also made the decision. This solution has many advantages: cheaper and simplified sensors, very accurate fusion... On the other hand, centralized fusion requires a high interoperability, a very efficient central unit and an extended bandwidth for raw data.

An intermediate solution can be found in *Hybrid Fusion* which allows both smart sensing with local data processing and central fusion. It allows for partitioning of resource effort between sensor and the central server. It reduces the cost of data distribution and maintain a good fusion accuracy.

The two last fusion models are in competition. Historic car manufacturers like Volkswagen or Renault-Nissan choose the hybrid fusion scenario which offers a good trade-off between flexibility, adaptability, complexity and cost. On the other hand, new "*Californian*" car manufacturers like Tesla or Weymo work on centralized fusion exploiting to its high accuracy. This situation brings to the development of adaptable sensors featuring high sensoring performances and data processing resources.

2. Automotive radar overview

As discussed in the previous section, automotive radar is one of the critical sensors for automotive safety and automation. This section exposes the main expectations of automotive radar, its characteristics and the different user cases.

a. Radar system

Radar systems were developed in the early '40 for military aeronautics and then become popular for civilian applications. As explained in 1.b, the radar is based on the emission of an electromagnetic signal with a specific signature. When the signal illuminates an obstacle, it's reflected to a receiver module which detects and computes the signal. The radar receiver can determine the time of flight and the signature modification to measure the distance to the target, its speed and even its position relative to the sensor.

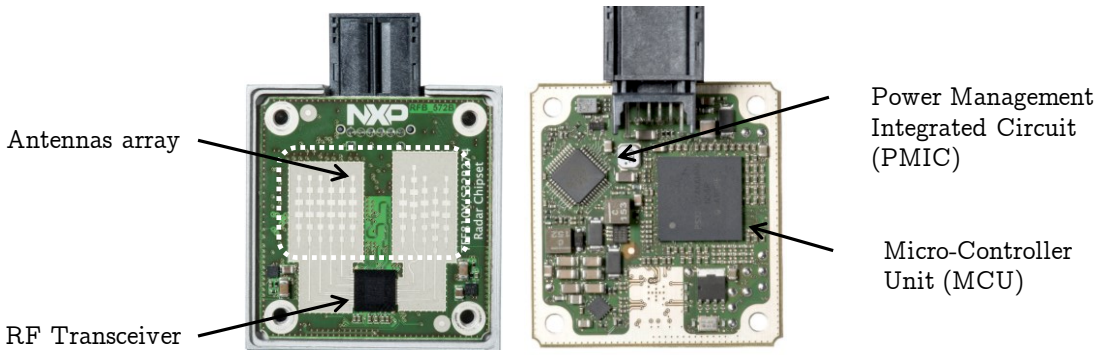


Figure 4 – Example of Radar board with a Transceiver (a), Antennas (b), PMIC (c) and MCU (d)

A complete radar module is presented in Figure 4. As isolation between transmission and emission is a critical point, a bistatic architecture is chosen with two antennas arrays as we can see on the Figure 4.b. The RF transceiver is integrated in a single chip (Figure 4.a), a detailed description of this chip is proposed in III. The two other components of a radar module are the Power Management Integrated Circuit (*PMIC*) and the Microcontroller Unit *(MCU),* respectively Figure 4.c and Figure 4.d. The second one assures the digital signal processing and is integrated in the RF Transceiver chip for the new radar generations.

b. Expectations of automotive radar

To maintain a high level of sensing, car manufacturers define several specifications linked to the *maximum range*, the *resolution* range, the velocity and the angular measurement. The measurement accuracy is obviously important for the determination of the target distance and velocity. Besides, the ability to recognize *target signature*, throughout its radar cross section, is critical for classification. If two targets are closed, the *object separation* is a critical parameter to distinguish one target from another. Besides the ability to echo detection is critical

in the case where target echo is masked by unexpected large signals such as interferers, large echoes, jamming...

Additionally to RF performances, the radar is supposed to be used over several decades of years in very different conditions such as desert, mountain roads... Hence the robustness and the reliability are also important metrics in the development of radar modules.

c. Spectral occupation

In radar applications, frequency is a key parameter since it contributes to the performance, field of use and form factor. The increase of the operating frequency, and bandwidth as well, improves the skills. For this reason, industry has pushed up to operate automotive radar in millimeter Waves frequency band. In this domain, H_2O and O_2 absorption has a strong impact on atmospheric attenuation, as illustrated in Figure 5. Since the attenuation is critical for the application, radar band are positioned in low absorption frequency band such as 24GHz and 76 to 81GHz.

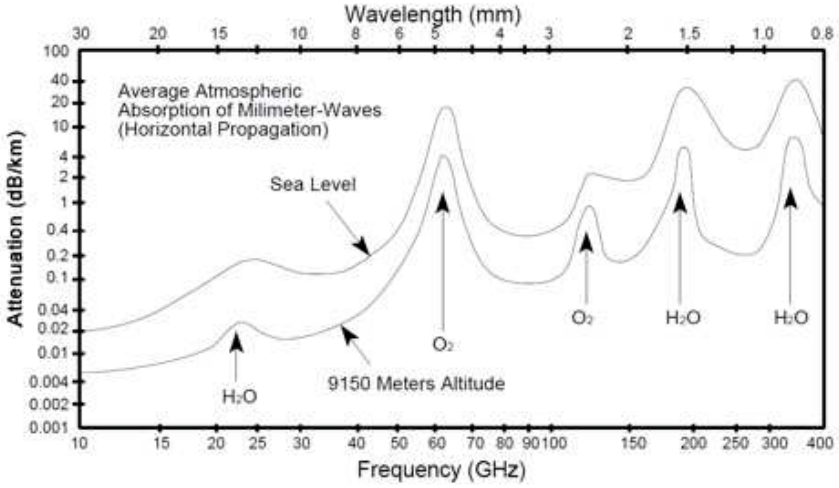


Figure 5 – Atmospheric attenuation in mm-Waves domain [8]

d. Automotive Radar Standards

In European Union, the European Telecommunications Standards Institute oversees the standardization of telecommunication industry. The ETSI defines the European Standards noted *EN* in link with International Telecommunication Union and national administrative authorities. These standards are only related to spectral occupation and level of emissions/receptions of RF signals. For automotive radar, the different European standards are proposed in Table 2 and based on measurement techniques which are defined in ETSI EN 303 396 [9]. All metrics are related to transmitted/received RF signals of the overall radar module, including antennas. This metrics are given for in-band signals, signals closed to RF band called "out of band" and for spurious in remote-band.

Table 2 – ETSI Automotive Radar standards from [10], [11] and [12]

Standards	*Band*	*EN 302 858*	*EN 301 091*	*EN 302 264*
Frequency (GHz)	/	24.05-24.5	76-77	77-81
Mean Power (dBm)	in-band	/	50	-3 dBm/MHz
Peak Power (dBm)	in-band	20	55	55
Unwanted emissions (dBm EIRP)	out-of-band	10	0	-30
	Spurious	-30	-30	-30
Emissions (dBm EIRP)	Spurious	-47	-47	-47
Signals handling at 10m (dBm EIRP)	in-band	0	10	10
	out-of-band	10	20	20
	remote-band	10	20	20

3. Radar applications in automated vehicles

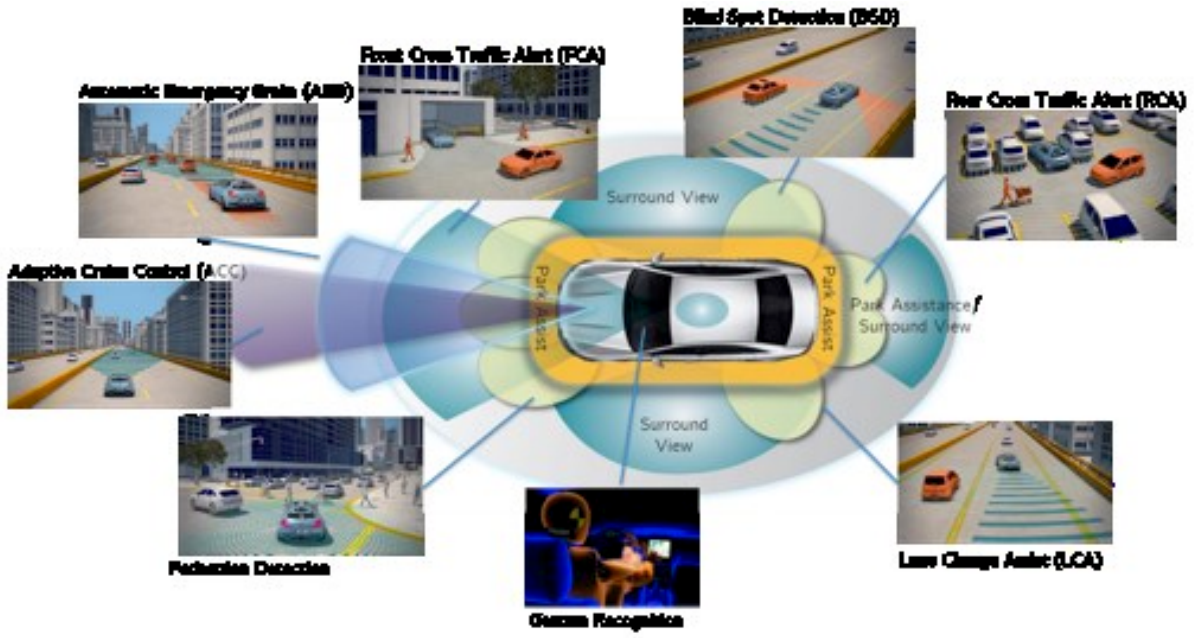


Figure 6 – Radar applications in automated vehicle

The flexibility and the reliability of radar technology are attractive for a large scope of detection scenarios as illustrated in Figure 6. In practice, three kinds of radar modules are exploited in the automotive industry: Long Range Radar *(LRR)*, Medium Range Radar *(MRR)* and Short-Range Radar *(SRR)*. Their specifications are reported in Table 3 and further discussed in the next sub-sections.

Table 3 – Typical LRR, MRR and SRR specifications [13]

Radar type	LRR	MRR	SRR
R Range (m)	10 to 250m	1 to 100m	0.15 to 30 m
ΔR Range resolution (m)	0.5m	0.5m	0.1m
δR Range accuracy (m)	0.1m	0.1m	0.02m
Δv Velocity resolution (m/s)	0.6m/s	0.6m/s	0.6m/s
δv Velocity accuracy (m/s)	0.1m/s	0.1m/s	0.1m/s
ϕ_{max} 3dB beamwidth in azimuth (°)	15°	40°	80°
$\delta\phi$ Azimuth angular resolution (°)	0.1°	0.5°	1°
ϑ_{max} 3dB beamwidth in elevation (°)	5°	5°	10°

a. Short Range Radar (SRR)

Shorts range radars are designed to monitor the car vicinity and detect targets within 80 meters. Thanks to the use of numerous SRR, it's possible to create a 360° safety cocoon around the car with several applications such as surround view, pedestrian detection, park assist or side impact detection. To address these various applications, SRR has a high azimuth aperture angle, up to 90°, and need a high spatial resolution to detect simultaneously several targets. However, as autonomous cars are supposed to used more than ten radar modules, the power consumption and the price of SSR modules are critical.

b. Medium Range Radar (MRR)

Many applications such as blind spot detection, rear or forward cross traffic alert or autonomous emergency braking needs medium range radar with a higher detection range up to 160-m but a lower angular aperture. MRR performances represents a trade-off between SRR and LRR ones.

c. Long Range Radar (LRR)

Long range radars need to detect long distant targets up to 300 meters. The applications such as lane change assist, adaptive cruise control need a very narrow field of view with a small horizontal angle, around 5°, with strong constraints on object separation or angular resolution. For instance, a 0.1° accuracy is needed for spatial resolution. Due to these constraints, radar transmitter is supposed to generate a signal with a high effective isotropic radiated power (*EIRP*) whereas the receiver is expected to achieve a high sensitivity. This metric denotes the ratio between signal power and noise power and it's a key parameter to define RF performances of a radar system.

II. FMCW Modulation Basics

The radar industry develops many modulations: pulsed radar, continuous wave, FSK modulation... Frequency Modulated Continuous Wave (FMCW) modulation is still dominant in ADAS. This technique is based on "chirps", a continuous signal whose frequency varies linearly with time, which gives to FMCW some advantages:

- Easy generation of the transmitted signal,
- Simultaneous measurement of target distance and velocity with a good resolution,
- Simple baseband for signal processing at few MHz,
- Low peak power constraint compared to pulsed radar.

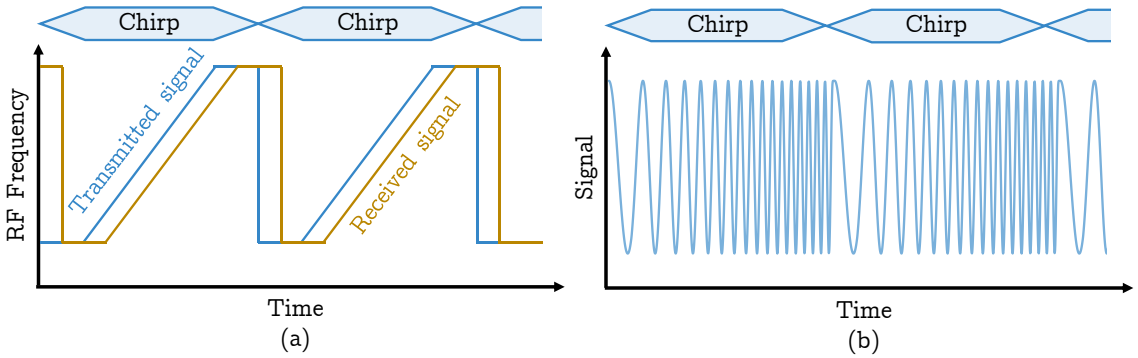


Figure 7 – FMCW modulation among time in frequency domain (a) and signal for transmitted signal (b)

Widely used for automotive radar, the saw tooth pattern modulation is illustrated in Figure 7.a. When the chirp transmitted signal illuminates an object, it creates a reflected attenuated signal at radar receiver input with some propagation delay. An illustration of signal variation in time domain is also proposed in Figure 7.b. This section details the measurement techniques for the estimation of the distance and the velocity of a target in an FMCW radar system. The main trends in FMCW signal characteristics for modern ADAS applications and their impact on Receiver characteristics are further discussed.

1. Distance measurement

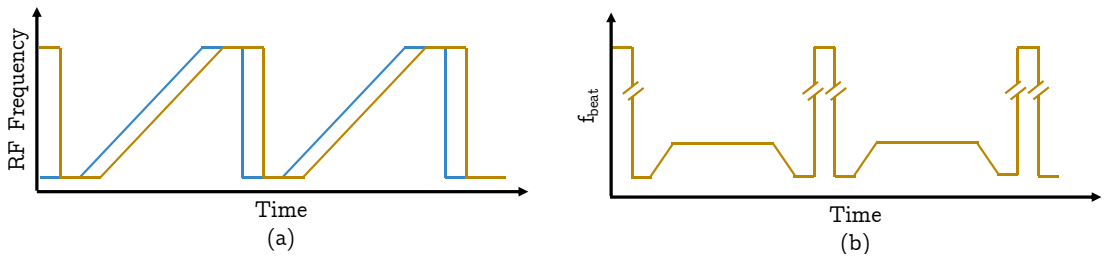


Figure 8 – FMCW modulation for Automotive Radar regarding the (a) RF Frequency and (b) the frequency difference f_{beat}

For all radars, the time of flight of the signal measures the target distance and, with FMCW modulation, is easy to relate to signal characteristics. Illustrated in Figure 8, the distance between the target and the radar module is equivalent to the measurement of frequency difference between emission and reception.

Equation 1 – Range (R) measurement for Linear FMCW radar

$$R = \frac{C}{2}\Delta t \xleftrightarrow{For\ Linear\ FMCW} R = \frac{C}{2}\frac{T_{chirp}}{BW_{chirp}} f_{beat}$$

The Table 4 details the link between distance measurement performances key indicators and the signal characteristics. In modern ADAS applications, radars are expected to measure distant target with a high resolution and a good accuracy. For instance, a modern radar must be able to identity pedestrians over a long range and possibly close to a larger vehicle.

Table 4 – Target distance measurement performances (SNR: Signal-Noise-Ratio)

Performance parameter	Equation	Conditions
Maximum range	$R_{max} = \frac{C}{2}\frac{T_{chirp}}{BW_{chirp}} f_{beat,max}$	Depending on maximal $f_{beat,max}$ measurement
Range resolution	$\Delta R = \frac{c}{2\,BW_{chirp}}$	As $\Delta f = \frac{2\,\Delta R\,BW_{chirp}}{c\,T_{chirp}}$ and $\Delta f \approx \frac{1}{T_{chirp}}$
Range accuracy	$\delta R = \frac{c}{3.6\,BW_{chirp}\sqrt{2\,SNR}}$	Fraction of range resolution depending of SNR

Two major trends exist to improve the performance of the measured distance. First, RF chirp bandwidth is increased to improve range resolution and accuracy. For instance, a 1GHz bandwidth achieve a resolution of 15cm, a 4GHz bandwidth improves it to 4cm. Modern fast chirp modulation leads to reduce chirp time thus increases the maximum measurable frequency difference (f_{beat}). In consequence, RF wideband receivers with higher baseband Intermediate Frequency (*IF*) are needed.

2. Velocity measurement

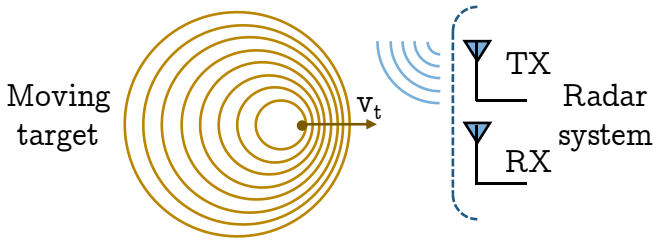


Figure 9 – Example of Doppler effect

When the receiver and the target, which is considered as a wave source, are in motion, the Doppler effect corresponds to an alteration of the received signal frequency. When the target approaches (or recedes) from the radar, each successive emitted wave travels further (or farther) before impacts the car and be reflected to radar receiver as presented in Figure 9. Due to this effect, the wave distance decreases (or increases) and is interpreted as an increase (or a decrease) of the measured frequency. One of the key advantages of automotive radar is the measurement of target velocity thanks to the Doppler effect. This section details the velocity measurement techniques in FMCW Radar and especially the recent change due to recent evolution to fast chirp modulation.

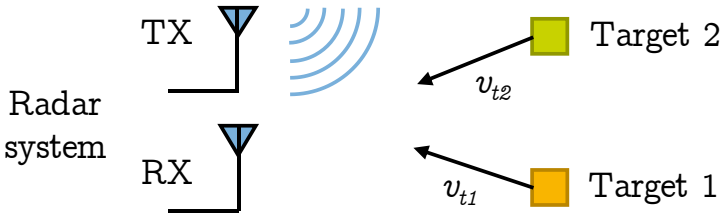


Figure 10 – Two targets situation

In slow chirp measurement with a chirp duration of 1ms, the velocity measurement is performed with a triangular signal. The frequency difference between emission and reception is shifted by the Doppler frequency f_D. However, in a situation with multiple targets illustrated by the Figure 10, slow chirp FMCW has a problem of ambiguity as shown Figure 11. For the resolution, four crossing points of range and velocity are measured. It induces the presence of two ghost targets. In consequences, slow chirp FMCW modulation is no longer preferred for modern ADAS radars.

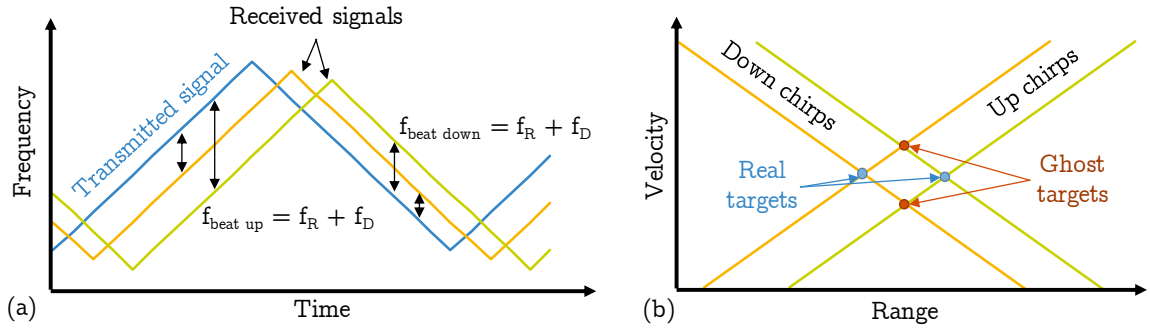


Figure 11 – Slow chirp FMCW modulation in a case with multiples targets for (a) transmitted and received signals and (b) velocity and range system resolution

Due to this ambiguity, modern ADAS applications prefer fast chirp FMCW modulation where the emission is done with a frame of N chirps with small duration of few microseconds. This measurement method enables an accurate estimation of distance and velocity without ambiguity as presented in Figure 12.

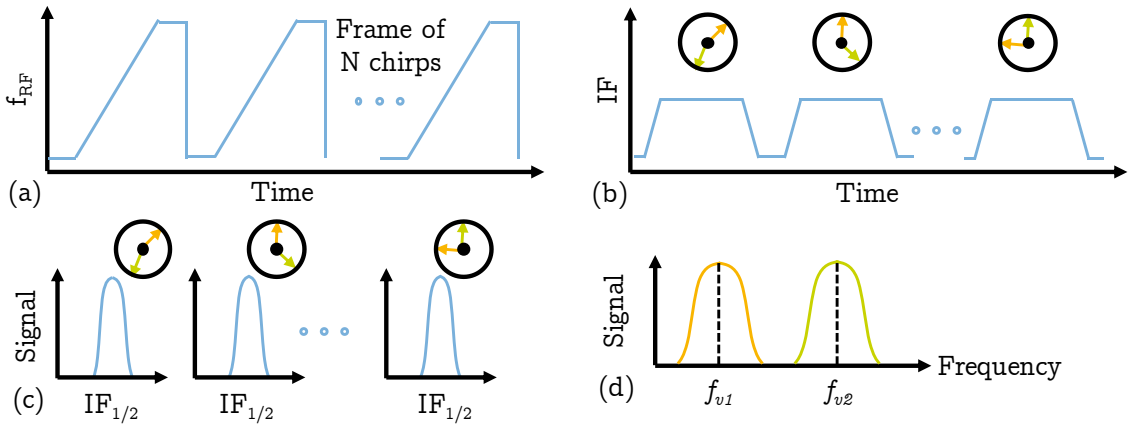


Figure 12 – FMCW processing flow of received signal with the (a) RF signal; downconverted to (b) baseband signal; and its (c) interpretation by a 1st FFT to determine the range; and (c) a velocity estimation thanks to a second Doppler FFT

In fast chirp modulation, the Doppler frequency is neglectable in front of the distance measurement frequency. Therefore, the range calculation is made with a first Fast Fourier Transform *(FTT)* on the downconverted signal to calculate f_{beat}. The phase of the received signal embeds the Doppler frequency information. Thanks to a second FFT, it's possible to calculate the target velocity with the phase difference between two chirps.

Equation 2 – Measurement of velocity with a fast chirp modulation

$$s(t) = f(f_{beat}t + \Delta\phi_r) \text{ with } \Delta\phi_r = \frac{4\,\pi\,v\,T_{chirp}}{\lambda}$$

To avoid any ambiguity between equidistant objects with different velocities, the fast FMCW uses a frame of N chirps. Each chirp has a different phase embedding the phase information of each target. A second FFT, called Doppler-FFT, is made on this N-system and separate the contributions of each objects. It allows the measurement of their velocity without ambiguity as expressed in Equation 3.

Equation 3 – Velocity measurement at Doppler FFT output

$$v_i = \frac{\lambda\, f_{v\,i}}{2\, T_{chirp}}$$

The Table 5 presents the performance assumptions on velocity measurement for modern ADAS. As fast targets should be detected, the chirp time should be small enough. In the same time, an important frame time, corresponding to numerous chirps, is done to maintain a good velocity resolution and a better accuracy.

Table 5 – Velocity measurement performances

Performance	Equation	Conditions
Maximum velocity	$v_{max} = \frac{\lambda}{4\,T_{chirp}}$	Unambiguous measurement for $\|\Delta\phi\| < \pi$
Velocity resolution	$\Delta v = \frac{\lambda}{2\,T_{chirp}\,N}$	Unambiguous measurement for $\Delta\omega > \frac{2\pi}{N}$
Velocity accuracy	$\delta v = \frac{\lambda}{3.6\,T_{chirp}\,N\,\sqrt{SNR}}$	Fraction of velocity resolution depending in SNR

3. Conclusion

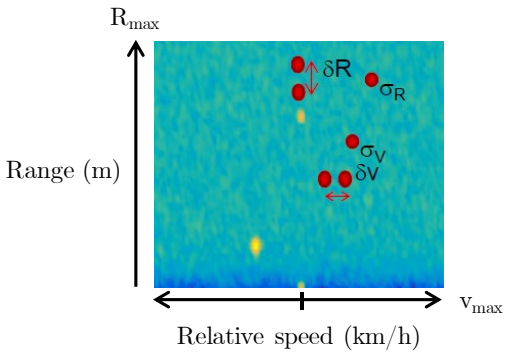


Figure 13 – 2-D image of car vicinity in a situation with multiple targets and the ley parameters of radar performance expecting the angular ones [14]

In conclusion, modern ADAS applications are now moving to fast chirp FMCW modulation which allows non-ambiguous measurement of distance and velocity of different targets in the same environment. This resolution is performed by an important digital processing and can propose a 2D image of the car environment as shown in Figure 13. To maintain a high unambiguous velocity measurement, a chirp duration between 20 and 50µs is mandatory. Increasing the range resolution is also critical for vehicle automation as discussed in section 2.b. This trend leads to increase the RF bandwidth as illustrated in Figure 14.

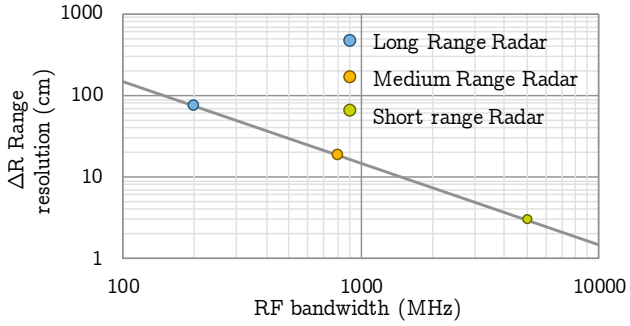


Figure 14 – Improving the range resolution regarding the RF bandwidth;

Considering the characteristics of the various radars exposed in the Table 3, the Figure 15 proposes the maximum archivable range regarding the f_{beat} frequency. In the range of ten microseconds, and for distant target, f_{beat} increase up to 40MHz. These trends make more challenging the analog signal processing in baseband sections and lead to faster RF bandwidth.

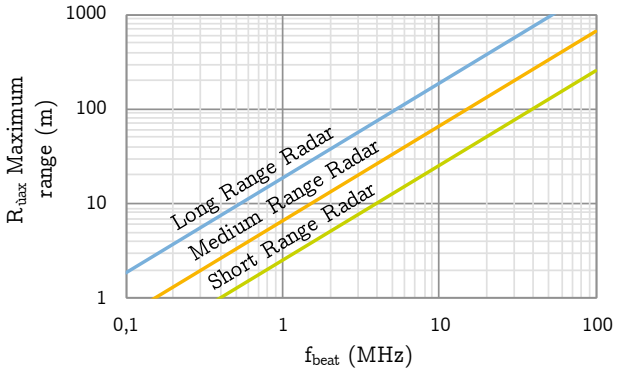


Figure 15 – Maximum range regarding the beat frequency

III. 77 GHz FMCW Radar IC

A high-level description or radar module is first presented in this section. The RF metrics are then discussed with respect to the radar performances. A radar module is presented in Figure 16. It includes some digital or analog parts such as digital controller, memory, sensors, power management; but also, the RF Front-End (*RFFE*) with the Phase-Locked Loop generating the Local Oscillator (*LO*), the transmitter (*TX*) and the Receiver (*RX*). This one is composed with a RF Demodulator (*DEMOD*) and an analog-to-digital converter (*ADC*).

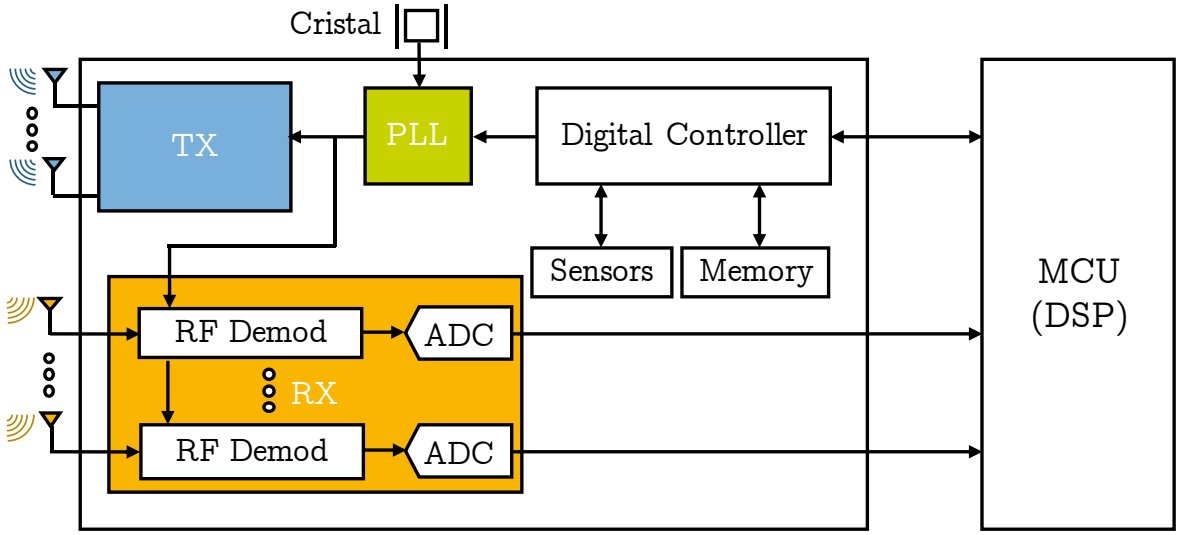


Figure 16 – Architecture of automotive radar module [17]

The transmitted signal is generated by a Phase-Locked Loop which features chirp linearity and phase noise which directly impacts the object separation [15]- [16]. As illustrated in Figure 17, considering 15dB SNR, the object separation cannot be resolved if the phase noise is too high (Figure 17.(b)). Indeed, the maximum range of detection is determined by the radiated power as illustrated in Equation 5. As consequences, the TX is expected to yield a high output power P_{TX}, +12dBm at least, which is challenging regarding the operating frequency, the technology capabilities and reliability issues.

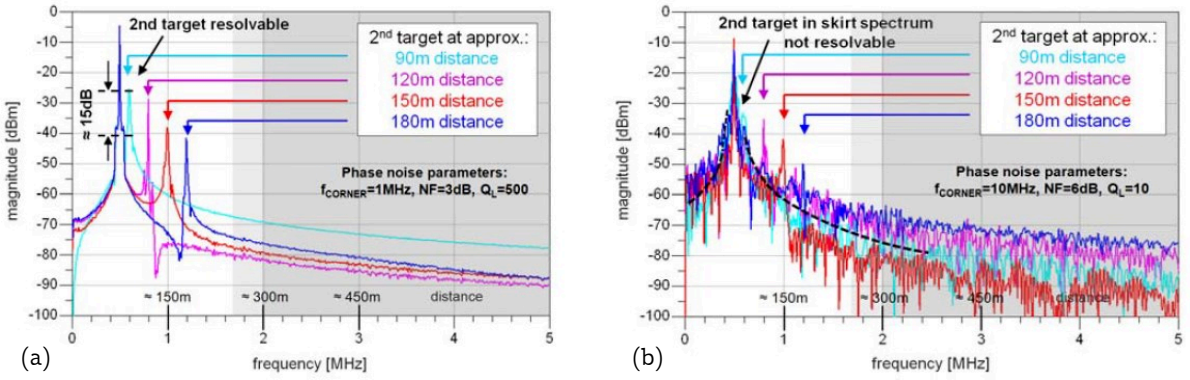


Figure 17 – Simulation of the influence of phase noise on target signal quality when a distant target approaching to a 75m object considering a LO with: (a) a low phase noise; (b) a high phase noise [15]

The third critical block for the RF Transceiver is the RX section featuring the RF Demodulator which downconverts the RF signal and formats the baseband signal for the ADC. The Analog-to-Digital Converter (*ADC*) transforms the analog signal into digital data which are further processed by the Micro Processor Unit. A detailed description of the RF Demodulator is proposed in the section 1.b. In this chain, the RF downconverter is critical, and this section focus on its main specifications: gain, noise and linearity. In the following sections, the terms downconverter and RX-RFFE will be used as equivalent.

1. Noise in automotive radar [17]

As shown in Figure 5, atmospheric losses are negligible at 77GHz and the losses are mainly due to natural dispersion of the EM wave. The purpose here is to determine the maximum range due to the signal treatment. Three phenomena are then considered: the propagation of radar signal considering radar module characteristics, the noise distribution overall the demodulation chain, the de-sensitization of the receiver due to cross-talk between transmission and reception.

a. Maximum range regarding the demodulator NF

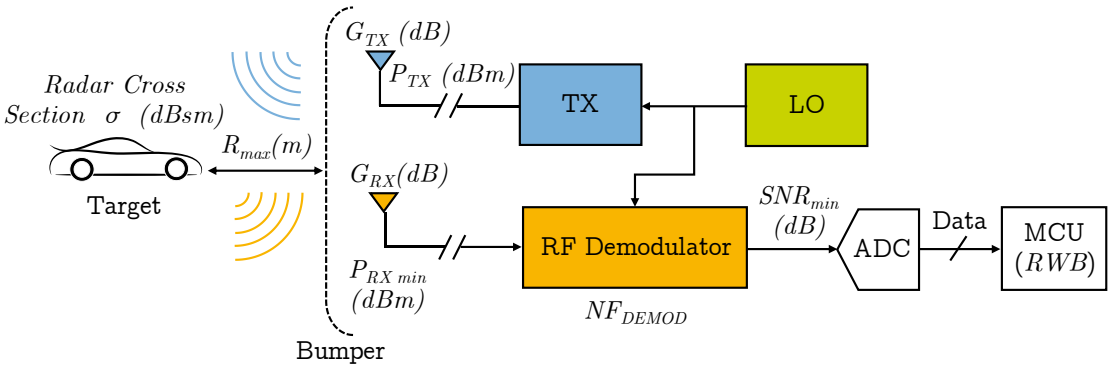


Figure 18 – Schematic of radar signal attenuation in use case

An illustration of the radar emission/reception is proposed in Figure 18. As expressed in section 3, the Radar standards define the transmitted power noted P_{TX}, including the TX output power, the number of transmitters, the PCB losses, and the transmission antenna gain G_{TX}. The antenna gains are calculated thanks to antenna characteristics (Table 3) and gain formula from [18]. On the other hand, the receiver needs a minimum input power called sensitivity noted $P_{RX,min}$, to properly process the signal. The Equation 4 links the maximum achievable range to these parameters.

Equation 4 – Radar maximum achievable range

$$R_{max}(m) = \left(\frac{P_{TX}G_{TX}G_{RX}\lambda^2\sigma}{(4\pi)^3 P_{RX,min}}\right)^{0.25}$$

The Radar Cross Section σ, expressed in m^2 or dBsm [$dB(m^2)$], represents the target signature and depends on the target size, its physical properties and its shape. In Table 6, some common targets radar cross sections are proposed:

Table 6 – Common radar cross section for specific targets [19]

Target Type	σ (dBsm)
Pedestrian	-10
Bike	7
Car	Maximum {10 log (Range (m)) + 5; 20}
Truck	Maximum {20 log (Range (m)) + 5; 45}

The MCU performs an FFT of the data with a resolution (RBW) as illustrated in Figure 18. To execute this signal processing, a minimum Signal-on-Noise Ratio (SNR_{min}) is required at ADC input. The SNR_{min} is linked to $P_{RX,min}$ by the Equation 5 which defines the receiver

sensitivity from noise floor at -174dBm accounting the noise contribution of the RF demodulator represented by its noise figure NF_{DEMOD}.

Equation 5 – Sensitivity definition for a receiver

$$P_{RX,min}(dBm) = -174dBm + NF_{DEMOD}(dB) + 10\log(RBW) + SNR_{min}(dB)$$

Considering these two equations, a top-level specification on the maximum range define the maximal NF of the RF demodulator as proposed in Figure 19. In short range use case, a 20 dB NF_{DEMOD} is expected to target at 80m. In long range use case, the maximal measurable distance should be higher than 200 meters, such feature leads a NF_{DEMOD} at 17dB. These noise specifications may appear as relaxed, but it should consider the noise distribution overall the all demodulator chain and the NF de-sensitization. These two elements are discussed is the following sections.

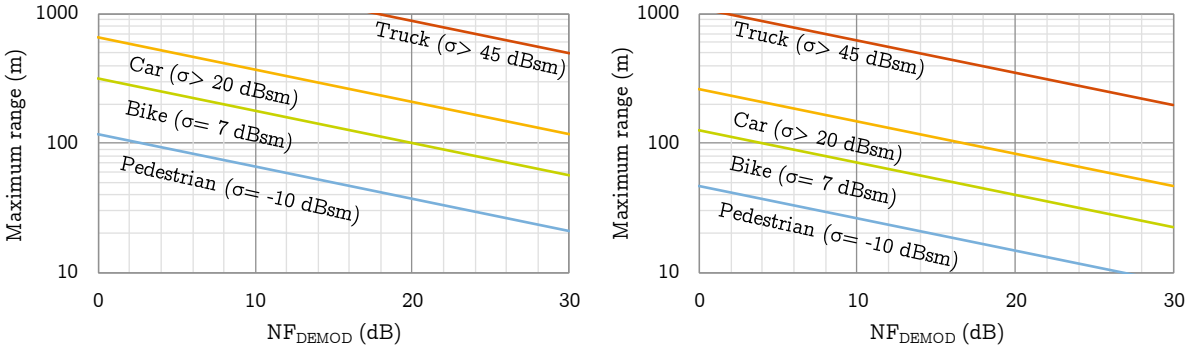
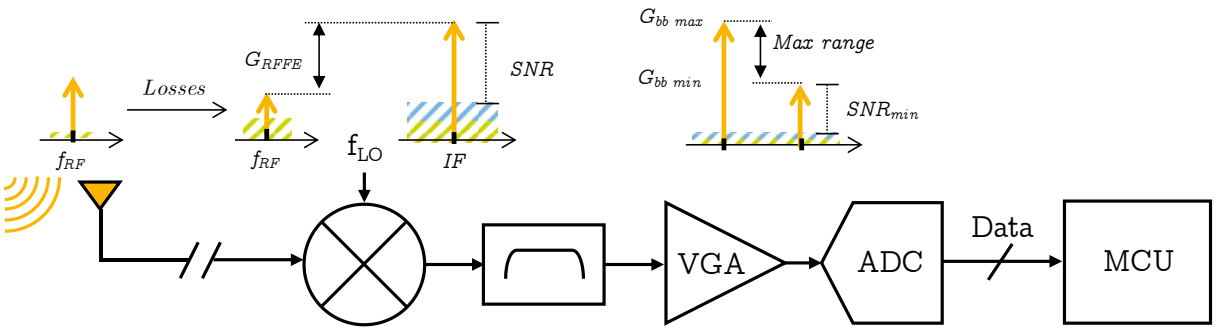


Figure 19 – Maximum achievable range of various targets regarding the RF demodulator NF for (a) long range radar and (b) short range radar

b. Noise distribution on RF demodulator chain



PCB & Interface	RX-RFFE	HPF-VGA$_1$	HPF-VGA$_2$	Sub-systems
-2dB	15dB	22dB	10dB	Gain
2dB	12dB	10nV/√Hz	50nV/√Hz	Noise

Figure 20 – Signal processing and noise distribution throughout the RF demodulator

The Figure 20 proposes an illustration of the overall architecture of the RF demodulator. The interconnection of the antennas to the IC, the PCB routing and the interface directly impacts the noise performance due to losses which are estimated to 2dB. The RX-RFFE downconverts the RF signal to baseband domain from 1 to 40MHz. Analog filtering eliminates out-of-band jammers, and the Variable Gain Amplifier (VGA) improves the dynamic range of the signal at ADC input. The Figure 20 also presents an evaluation of the noise contribution and gain of the different blocks. Based on the Friis formula for a cascaded chain of blocks, from Equation 6, the noise factor F_{DEMOD} can be derived.

Equation 6 – Friis formula for the RF demodulator considering noiseless filter

$$F_{DEMOD} = F_{RX-RFFE+PCB} + \frac{(e_{n,VGA1})^2}{k_B T\, Z_S\, (G_{PCB} + G_{RX-RFFE})} + \frac{(e_{n,VGA2})^2}{k_B T\, Z_S\, (G_{PCB} + G_{RX-RFFE} + G_{VGA1})}$$

The Figure 21 presents the noise performance of RF demodulator regarding the gain and noise figure of the RX-RFFE, considering the baseband characteristics exposed in the Figure 20. Conventional downconverters have a noise figure from 10 to 16dB in the worst case. Considering this typical value, the impact of RX-RFFE gain is critical. According to Figure 21, $G_{RX\text{-}RFFE}$, should exceed 10dB to significantly moderate the noise contribution of baseband circuit to NF_{DEMOD}. In the following analysis, a gain of 12.5dB will be considered.

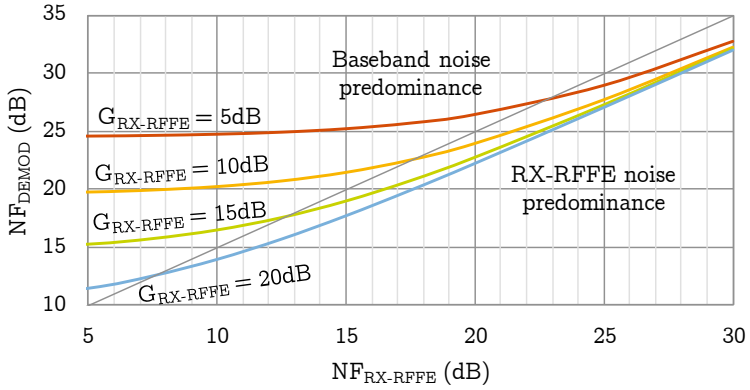


Figure 21 – RF Demodulator noise performance regarding RX-RFFE characteristics

c. Noise figure de-sensitization

Considering the reflecting effect of a bumper and the coupling through the PCB, the isolation between TX and RX is estimated at 35dB. The lack of isolation creates a jammer P_{jammer} at RX input defined by the Equation 7.

Equation 7 – Jammer due to lack of isolation

$$P_{jammer}(dBm) = P_{out}(dBm) - Isolation\ (dB)$$

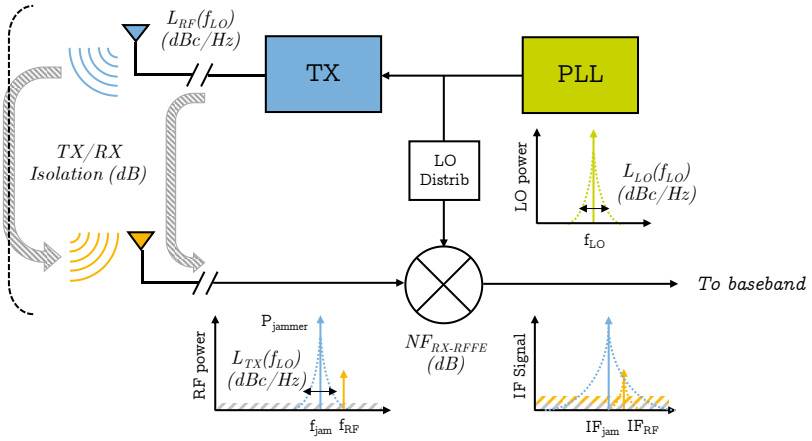


Figure 22 – NF de-sensitization phenomenon due to uncorrelated phase noise and isolation

Due to the different paths between the LO distribution to RX and TX, uncorrelated phase noise appears between both paths. This phase noise is evaluated to -144dBc/Hz. Hence, the downconverter jammer presents an important noise skirt modeled by a noise source e_{degrad} defined in Equation 8.

Equation 8 – Noise degradation due to de-sensitization

$$e^2_{degrad}(mW/Hz) = P_{jammer}(mW) \cdot (10^{L_{TX}(dBc/Hz)} + 10^{L_{LO}(dBc/Hz)})$$

This additional noise source can significantly degrade the noise figure of the downconverter as illustrated in Figure 23.(a). This expansion of noise figure is particularly important for low noise RX-RFFE but reduced as the NF increases. Considering a 12dB noise figure, this degradation is limited to 2dB for a +12dB output power, which is equivalent to one TX enable, but it rises to almost 5dB if four TX are on (P_{TX} = +18dBm). This noise de-sensitization phenomena must be considered evaluating the overall performance of the radar in receiver mode. Nevertheless, as shown in Figure 23(b), the increase of the transmitted power P_{TX} remains a possible solution to improve the radar range.

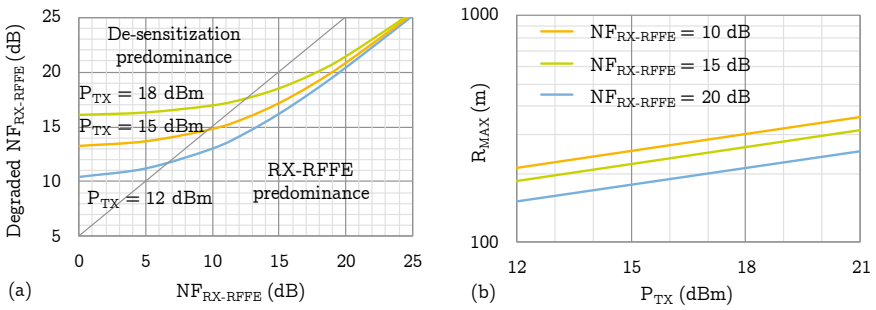


Figure 23 – Effect of de-sensitization on (a) Noise figures for various transmitted powers; (b) Maximum achievable range regarding the transmitted power for various $NF_{RX\text{-}RFFE}$

c. Conclusion on noise specifications

The proposed analysis allows to define a specification of the maximum detection range with an associate NF for the RF demodulator. The overall noise budget must account for distributed contributions such as PCB losses, IC interface, the RF Front End and the baseband circuits. The RFFE de-sensitization due to the lack of isolation between TX and RX and the uncorrelated phase noise in the LO distribution must be also considered. Accounting for these noise phenomena, we determine the maximum achievable range regarding the RX-RFFE noise figure for the short- and long-range use cases as illustrated in Figure 24.

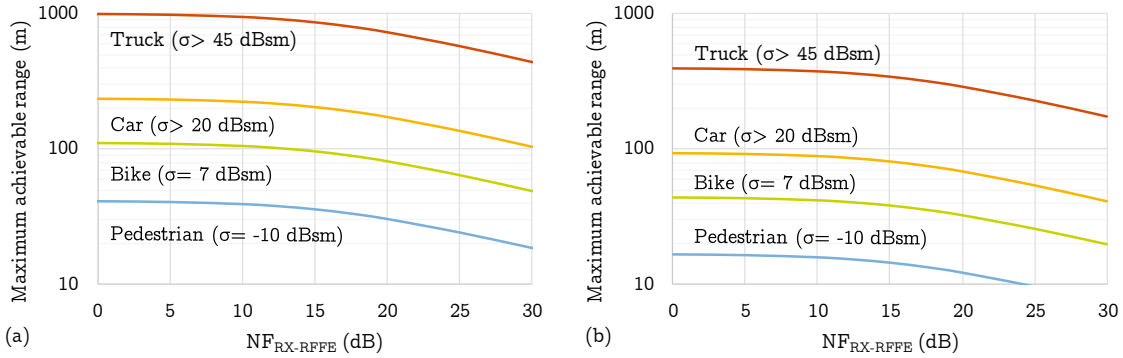


Figure 24 – Maximum range regarding the RFFE noise figure for various targets for (a) long range applications; (b) short range applications

The downconverter noise figure is a key indicator of the radar performance. To address long range or even imaging radars use cases, the RX RF Front-End may achieve a 12dB noise figure at 150°C in the worst case. For short range use cases, the noise specification is relaxed to 15dB.

1. Linearity in Automotive Radar [20]

For an ideal Front-End, the output signal is a linear image of the input signal. Unfortunately, the downconverter introduces some distortions which corrupt the original signal. These non-linearities are further discussed in this section.

a. In-band linearity (ICP1)

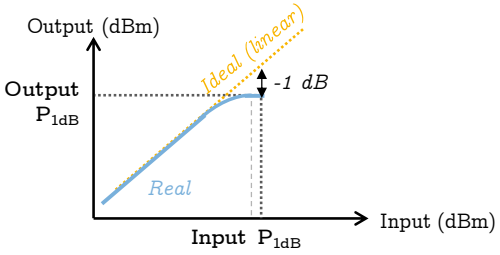


Figure 25 – 1dB compression point definition

Equation 9 – In band compression point specification

$$inband\ P_{1dB}(dBm) = \ OP_{max} - \ G_{RX} \ \approx \ -20\ dBm$$

Any RX-RFFE behaves linearly up to a level of input power which drives then the system in saturation as illustrated in Figure 25. Entering the non-linear mode, the received signal is corrupted and the information cannot be retrieved. The linear region is defined by the -1dB compression point (*CP1*) which can be referred at the input (ICP1) or at the output. In automotive radar, the in-band compression point, due to target reflection, is defined by the Equation 9 considering the total gain of the Receiver chain. In our case, we consider it around -20dBm in the worst case.

b. Intermodulation (IIP3)

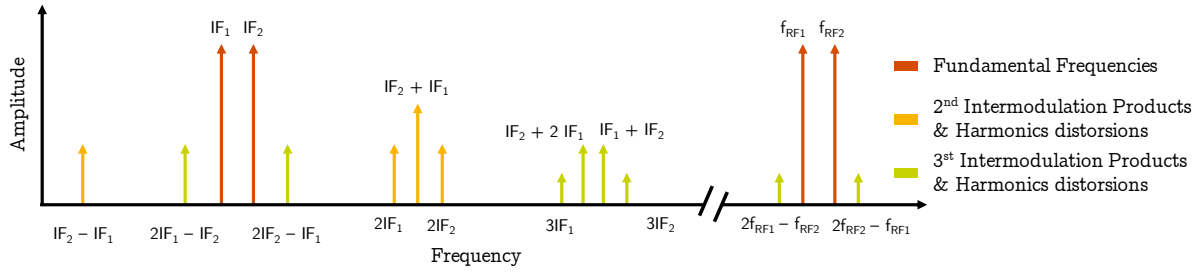


Figure 26 – Intermodulations & distorsions products in real downconverter

Most of the time, several targets are present in the radar scope. It leads to several in-band signal with different frequencies at RX input, i.e. at fundamental frequencies f_{RF1} and f_{RF2}. A linear receiver is supposed to process and to transfer signal at these two harmonics only. A real receiver will be affected by a mixing effect. It leads to create in-band intermodulation products as illustrated in Figure 26, i.e. 2nd and 3st intermodulation productions (IP2 & IIP3) and 2nd and 3st harmonic distortions. Most of them are filtered out by the system but the third order intermodulation, $2f_1$-f_2 and $2f_2$-f_1, are located in the radar bandwidth. These harmonics can be interpreted as spurs and leads to identify ghost targets.

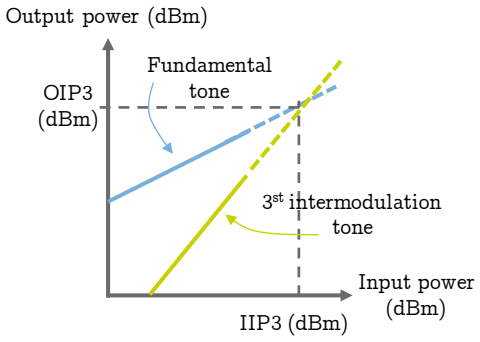


Figure 27 – IIP3 definition

The third order intercept point (*IP3*) is a figure-of-merit which evaluate this intermodulation. The IP3 is a hypothetical point at which the power of the third order harmonic rise to the fundamental harmonic power. This parameter can be referred at the input (*IIP3*) or at the output. The in-band IIP3 specification is expressed in Equation 10 considering the RX chain gain and is estimated at -26dBm.

Equation 10 – In band IIP3 specification

$$Inband\ IIP3\ (dBm) = 16 - G_{RX} \approx -26\ dBm$$

c. Bumper impact on linearity (ICP1)

According equations Equation 9 and Equation 10, the intrinsic specifications for in-band linearity of a radar RX are not tough. However, these two equations don't consider the environment of radar in the car. As radars antennas are mounted behind bumpers, the transmitted signal may be reflected by the bumper to the radar receiver. Intensive researches investigate the development of invisible bumpers, so far the reflection is limited to -20dB over the entire 76-81GHz band as shown in Figure 28.

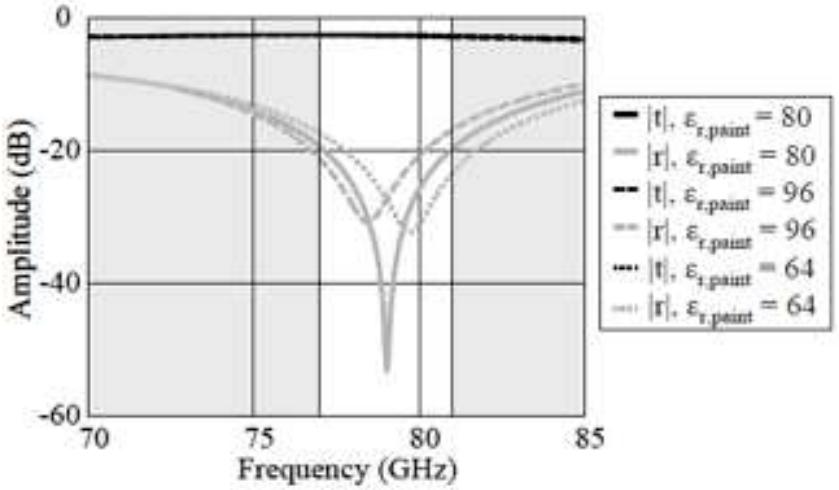


Figure 28 – Transmission and reflection through a bumper with metallic paint [21]

Due to the bumper proximity, a high power reflected signal is presented at the receiver input with a very small frequency shifting, evaluated at 10kHz around the transmitted frequency. Unfortunately, this signal can't be filtered out as illustrated in Figure 29. The bumper blocker is further downconverted and processed in baseband.

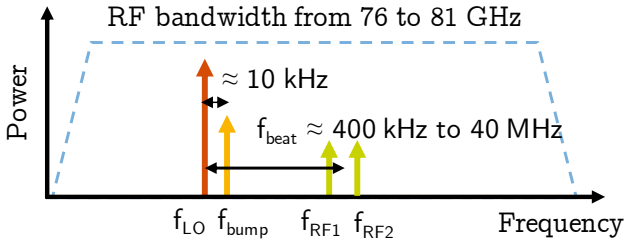


Figure 29 – Spectrum at Front-End input

The presence of the in-band blocker, located at f_{bump} as illustrated in Figure 29, is an important issue for downconverter linearity. First, the LNA should not be placed in saturation mode. Besides, if one or two tones are present at the input, important intermodulation products will be created as illustrated in Figure 30. These spurs can be considered as targets by the MCU. The ghost targets are obviously a major issue in automated vehicles. To handle this major issue, the 1dB compression point specification is revised to -5dBm.

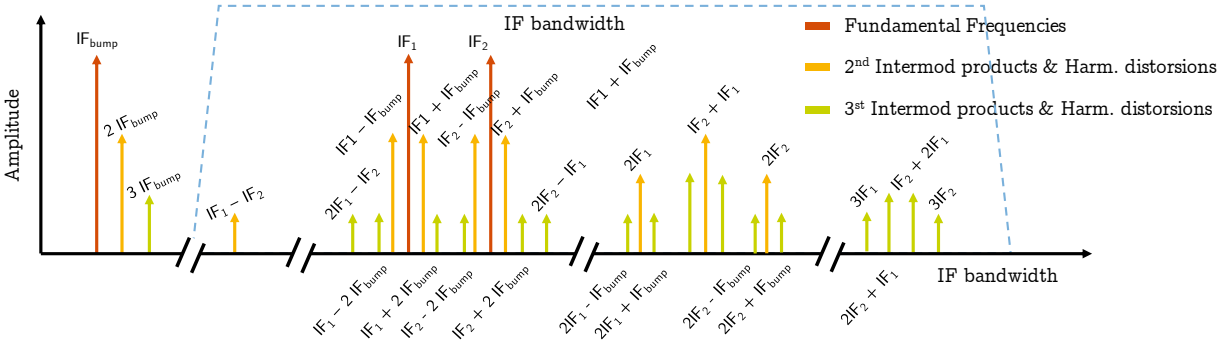


Figure 30 – IF spectrum with intermodulations due to bumper

2. Conclusion

Radar IC is a complex system with some specific constraints related to the application and its environment. At commercial stage, four key specifications are critical regarding the competitor in semiconductor industry: the form factor (price, size and consumption), the transmitted output power, the PLL phase noise and the Noise Figure of the RX chain. More specifically the development of the downconversion part of a radar module would address some challenges to be competitive. One is related to the linearity due to the close location of the bumpers. Beside the sensitivity of the radar requires not only a low NF but also a large conversion gain. These two characteristics would be improved with a reduced impact on the overall power consumption. The Table 7 sums up some of the important specifications of a radar RX-RFFE.

Table 7 – Specifications of receiver RF front-dnd

Specifications	Min	Typ	Max
RF bandwidth (GHz)	76		81
IF bandwidth (MHz)	1	/	40
Noise figure (dB)			
For LRR			15
For SRR			17
ICP1 (dBm)	-5		
Passband ICP1 (dBm)	-20		
IIP3 (dBm)		-26	
LO-to-RF Isolation (dB)			-35
Objectives	Min	Typ	Max
Conversion Gain (dB)		10	
Power consumption (mW)		20	

IV. Considerations on receiver RFFE for automotive radar

As discussed in previous section, the RX specifications are challenging and as consequences, the receiver is a critical block for automotive radar. This section focusses on the selection of the technology for the next generation radar, which will have an impact on RX-RFFE possible architecture.

1. RF CMOS opportunities

Automotive radars were originally designed in III-V GaAs technologies. As shown in Table 8, they presented good performances in terms of gain, cut-off frequency or temperature behavior which are critical for 77GHz radar applications. Nevertheless, III-V technologies are expensive and do not offer a large scale of integration for digital processing. For these reasons, III-V technologies were reserved for luxurious car with an implementation based on discrete components, whereas semiconductor industry is moving to Silicon technologies for mass market products.

The two historic market leaders (NXP and Infineon) have selected BiCMOS technology on Silicium-Germanium substrate for their products thanks to their good trade-off between integration level and RF performances. As shown in Figure 31, BiCMOS technologies can achieve high transition frequencies with good performances. Nevertheless, modern ADAS do

not only require good RF performances but also a high level of integration and a low-cost production. On one hand, as discussed in 1.c, digital functions are included in radar chip and semiconductor manufacturers are considering the integration of the MCU and radar transceiver. On the other hand, as expressed in 3, radar modules are about to be massively deployed in modern cars, so the price of radar IC become critical.

Table 8 – Comparison of integrated technologies

Technology	CMOS	BiCMOS (SiGe)	III-V (GaAs)
Transition frequency	Medium	High	Very High
Breakdown voltage	Low	Medium	High
Power gain	Medium	High	Very High
Temperature behavior	Poor	Good	Good
Integration level	Very High	Medium	Very Low
Cost	Low	Medium	High

These trends push the semiconductor industry is moving to consider CMOS technologies for the implement of the next generations of radar modules. As illustrated in Figure 31, recent advanced RF CMOS technologies are now compatible with 77GHz radar constraints, especially regarding the transition frequency which exceeds 300GHz for technology nodes below 50 nm. The circuits proposed in this manuscript are developed in a 28nm CMOS process. The technology back end is illustrated in Figure 32. The three tick upper metal layers (AP, M8, M7) are used for RF routing. The six thin lower metal layers (M1 to M6) are basically used for digital blocks.

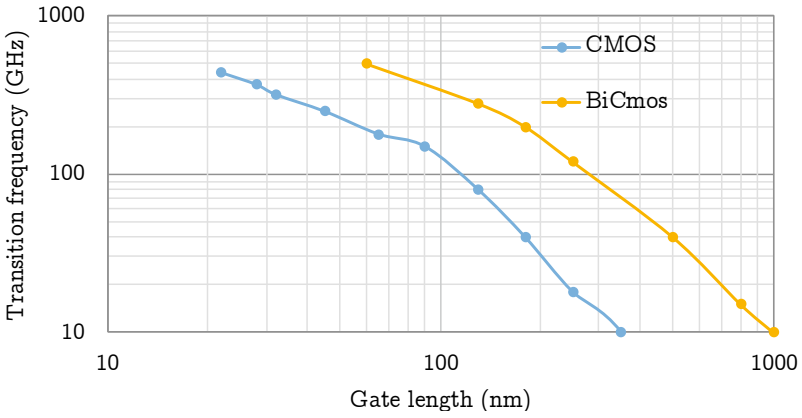


Figure 31 – Transition frequencies of CMOS & BiCMOS technologies

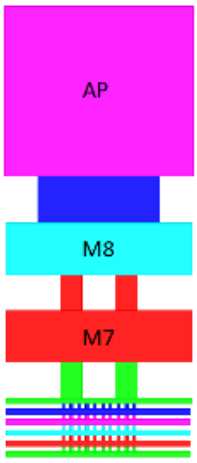


Figure 32 – 28nm CMOS technology back-end

2. mmW Front-End architecture

a. RFFE Basics

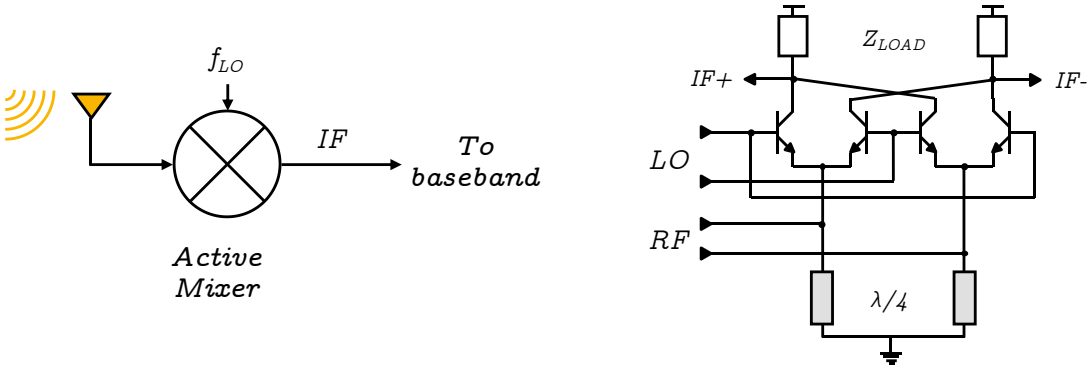


Figure 33 – Radar mmW Front End in 180 BiCMOS technology [17]

The core of the downconverter is the mixer. Active topologies, based on Gilbert cell, presented in Figure 33, are usually exploited in BiCMOS receiver architecture. This topology exhibits a good trade-off between conversion gain (typ. 17dB) and the compression point (-5dBm) with moderate Noise Figure (typ. 13dB). In terms of integration the input matching performed with quarter wave line require a significant silicon area.

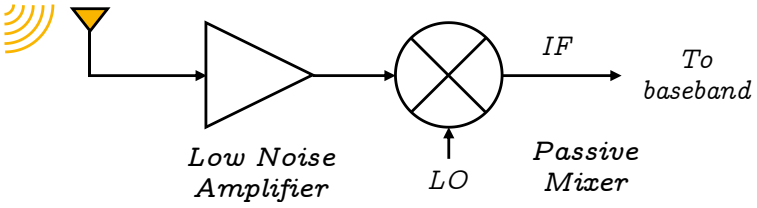


Figure 34 – Radar mmW typical architecture

Many CMOS Receivers do not use active mixer due to flicker noise contribution. In such a case, the receiver features a Low Noise Amplifier (*LNA*), a passive mixer and, eventually, a low noise baseband amplifier. The large voltage gain of the LNA is supposed to hide the noise of the following stage as expressed in Friis formula (Equation 11).

Equation 11 – Friis formula on noise

$$F_{RX} = F_{LNA} + \frac{F_{mixer} - 1}{G_{LNA}} + \frac{F_{baseband} - 1}{G_{LNA} G_{mixer}} + \cdots + \frac{F_n - 1}{G_1 \ldots G_n}$$

Nevertheless, a high gain LNA compromises the linearity of the system. This issue is illustrated in Equation 12. To reduce the degradation of the receiver linearity (*IP3*) due to cascaded stages, the linearity of the second stage $IP3_{\text{mixer}}$ would be G_{LNA} time larger than $IP3_{LNA}$, the $IP3_{baseband}$ would be ($G_{LNA} \cdot G_{mixer}$) time larger than $IP3_{LNA}$ and so on. Any increase in G_{LNA} requires the same improvement in the IP3 of the following stages. To keep the IP3 of a radar receiver at a high level, the voltage gain of the *LNA* is reduced which degrades the noise figure according Equation 11. Hence the design of the LNA is led by a tradeoff between linearity and NF performance.

Equation 12 – Cascaded IIP3 formula

$$\frac{1}{IIP3_{RX}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \cdots + \frac{G_1 \ldots G_{n-1}}{IIP3_n}$$

Frequency down-converters based on active and passive mixers are further investigated in this work.

b. RF signal processing

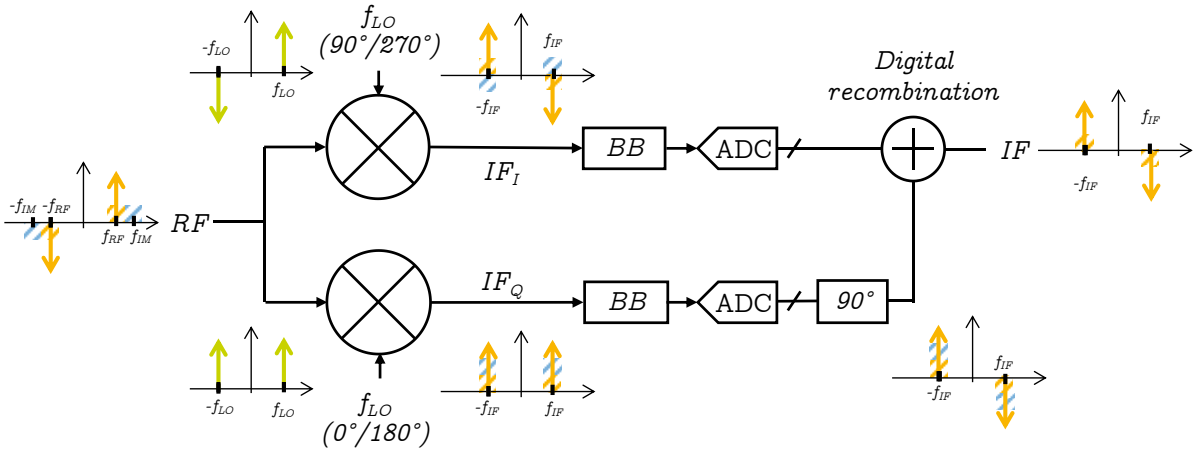


Figure 35 – IQ downconverter

A large majority of recent radars use a frequency down conversion based on in-phase signal processing as illustrated in Figure 34. This strategy is mainly motivated by a lower complexity and a reduced cost due to an implementation for baseband analog [14]. As discussed in section 1, the evolution of radar module specifications requires an overall improvement of RF performances. To address this challenge, a better RF signal processing is required. To leverage such challenge a complex (or I-Q) mixer is investigated in radar receivers. This kind of architecture presents in Figure 35, is based on a parallel processing, in-phase and in-quadrature, in the down conversion operation to cancel out the image contribution f_{IM} of the RF signal f_{RF}. I-Q downconversion improves in theory the Noise Figure by 3dB. Indeed, a real receiver downconverts the noise at image frequency, the image band foldback is cancelled with a I-Q configuration. In practice, the benefit is limited due to signal loss in the I-Q imbalance due to the implementation. Inherent to the image cancellation the I-Q signal processing also mitigates the intermodulation occurring in RFFE and improve "bumper rejection" and interference tolerance. This feature can be exploited for better safety monitoring. Besides, it mitigates the noise degradation due to TX/RX crosstalk.

3. Conclusion

The overall trend to integrate all the digital blocks with the RF transceiver leads to select highly integrated CMOS technologies for the next generation of radar. New receiver architectures are investigated to address the challenging specifications inherent to radar modules. Various RX implementations (passive or active, voltage and current mixing) will be discussed throughout this manuscript using noise cancelling approach for simultaneously wideband behavior and noise performances.

V. Thesis outline

Due to the development of automotive full automation, new generations of 77GHz radar require both a high level of digital integration and a low-cost development which leads to the selection of advanced 28nm RF CMOS technology. Bearing in mind the general specifications of power consumption, form factor or PVT robustness, the radar module presented at Figure 36 has four critical specifications: PLL phase noise, PLL linearity, TX output power and the RX noise figure. This work focusses on the design of downconverters which are critical for noise specifications.

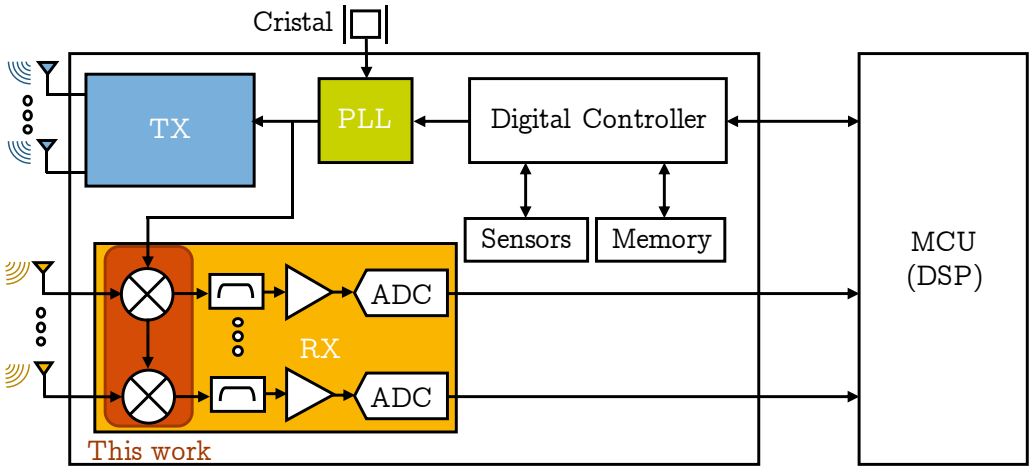


Figure 36 – The RX-RFFE in the radar module

Various downconverter architectures can be proposed to address the stringent radar specifications. Considering these various architectures, circuits techniques such as noise cancelling can be proposed to strengthen robustness to PVT variations and maintain good noise performances.

Table 9 – Specifications of receiver RF front-end

Specifications	Min.	Typ.	Max.
RF bandwidth (GHz)	76		81
IF bandwidth (MHz)	1	/	40
Noise figure (dB) for LRR			15
ICP1 (dBm)	-5		
Passband ICP1 (dBm)	-20		
IIP3 (dBm)		-26	
LO-to-RF Isolation (dB)			-35
Objectives	Min.	Typ.	Max.
Conversion Gain (dB)		10	
Power consumption (mW)		20	

The Chapter 2 presents active mixers in 28nm CMOS based on noise cancelling architecture. Due to large *1/f* noise in advanced RF CMOS, specific flicker noise reduction techniques are implemented in millimeter-Wave domain. Two active mixers were designed: a proof of concept for RF band and an application-oriented downconverter at 77GHz.

The Chapter 3 introduces various Low Noise Amplifiers which use noise cancelling approach with a differential architecture and leads to the development of a complementary capacitor cross coupled amplifier. Several implementations are proposed: the first on is a proof

of concept for RF multistandard applications and the others are application-oriented LNAs at 77GHz.

The Chapter 4 describes two Receivers using the proposed complementary capacitor cross coupled LNA. This chapter presents two downconversion architectures with either voltage mode mixer either a current mode mixer to compare their respective performances regarding the specifications.

The Chapter 5 draws the conclusions of this thesis and introduces the future works in Radar Automotive RX field.

The proposed research is realized in partnership with Bordeaux IMS Lab and NXP Semiconductors focusing on the design of downconverter adapted to the constraints of 77GHz Embedded Automotive Radar.

Chapter 2. 77-GHz Noise-cancelling active downconverter

Previously, in Chapter I, the system analysis brings up challenging specifications on RX front-end such as low noise and high linearity. Therefore, conventional architectures featuring Gilbert active mixer or common-source LNA combined with passive mixers are no longer sufficient to address the specifications presented in Table 9, especially in advanced RF CMOS technologies. Hence advanced circuit techniques are required to address these requirements.

This chapter proposes to study the application of noise cancelling downconversion to 77-GHz Radars. Active mixers are considered due to their good trade-off between gain, noise figure and linearity. Furthermore, downconverter based on noise cancelling architecture achieve wideband operation and overall high performances.

The first section proposes an introduction to noise cancelling topologies and their implementation. An RF demonstrator applying noise cancelling and low power techniques for IoT applications is proposed and measured in section II. To address automotive radar specifications, a noise cancelling mixer is proposed in section III with specific solutions to overcome CMOS flicker noise limitations. The measurement results are also reported. Finally, the section IV draws the conclusion about the downconverter regarding the state-of-art and the applications.

I. Noise cancelling principle

In order to address 5GHz band, a wideband design can enhance the robustness to PVT corners and the performance flatness over frequency. For multi-band and multi-standards communications receivers, a noise cancelling architecture is an emerging solution to perform both wide bandwidth and high RF requirements. This work proposes to export this topology to millimeter-wave domain, first the principle of noise cancellation is introduced.

In this section, the limitation of conventional noise matching approach is first outlined and then the overall principle of noise cancellation is explained. Furthermore, the conditions to build a common-gate based noise cancelling circuits are detailed and the advantages of this architecture are discussed.

1. Why noise cancelling is interesting?

a. Limitation of noise matched structures

According Chapter I.3, noise performance is a key metric for RF RX front-ends. For an RF device, the noise factor is expressed in Equation 13 considering the Lange invariant (N), the noise optimal impedance ($Z_{opt}=R_{opt}+jX_{opt}$) and the minimal noise factor (NF_{min}). To lower the noise factor (F) to the minimum noise factor (F_{min}), the noise impedance of the device (Z_{opt}) must be equal to the source noise impedance (Z_S)

Equation 13 – Noise factor regarding the noise parameters [22]

$$F = F_{min} + \frac{N}{R_s R_{opt}} \left| Z_{opt} - Z_s \right|^2$$

Nevertheless, this impedance Z_{opt} can be slightly different from the impedance which allows for a maximum of power transfer -i.e. power matching- as illustrated in Figure 37. This divergence between power and noise matching can lead to a poor trade-off and important variations over wideband operations or under PVT conditions.

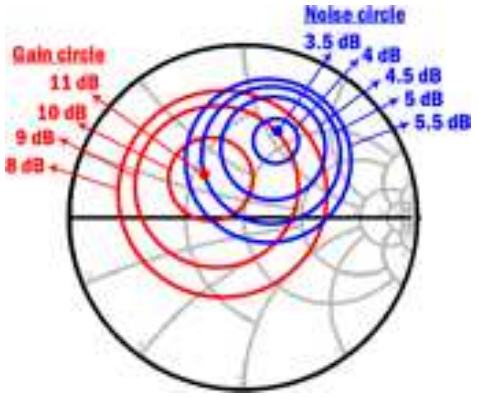


Figure 37 – Example of 94-GHz BiCMOS LNA noise and gain circle in Smith chart [23]

To achieve those matching requirements, two approaches are used with resonant or non-resonant matching. The former solution is based on a combination of passive elements resonating out the input impedance of the circuit to achieve a high level of noise (or power) matching at a given frequency. If it offers better RF performances, this topology is unfortunately narrowband and sensitive to PVT variations. The second approach avoids the use of resonant inductive elements and prefers wideband networks such as resistors, shunt feedback or common-gate structures. These topologies are intrinsically wideband, and some specific configurations can be controlled by biasing, allowing for some PVT compensations, at the cost of moderate gain and noise performances.

As detailed in Chapter I.3.1, automotive radar receivers have stringent specifications regarding the noise figure, directly linked to the achievable range, the bandwidth which must cover 76 to 81GHz to target short-range applications, and the robustness to PVT variations, up to a temperature of 150°C. To fulfill these conditions, a noise canceling topology can be interesting.

b. Noise cancellation principle

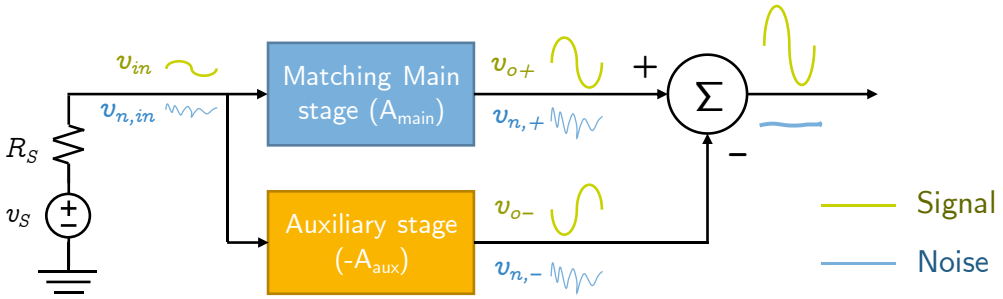


Figure 38 – Noise cancelling principle

The principle of noise cancelling architecture can be illustrated by the block diagram proposed in Figure 38 [24]. The main stage (A_{main}) achieves the impedance matching and determines the gain performance. Its noise is modeled by a noise source at its input ($v_{n,in}$). This stage is usually a wideband circuit with a poor noise performance. On the other hand, the auxiliary stage (-A_{aux}) assures the voltage sensing and performs the noise cancellation of the main stage. A combination is necessary to perform the effective cancellation of the noise. The key of noise cancelling principle is to identify the two circuit nodes where the signal is in-phase (respectively in-opposition) but noise is opposite (respectively in phase).

Considering only the main path of the block diagram in Figure 38, the input and output nodes have anti-phase noise voltages ($v_{n,in}$ and respectively $v_{n,+}$) and in-phase signal voltage ($v_{s,in}$ and respectively v_{o+}). The auxiliary stage uses a voltage sensing to pick up the signal and the noise voltage. By designing an auxiliary stage with a similar transfer function -i.e. $|A_{main}| = |A_{aux}|$ with opposite phase-, it's then possible to have at its output an opposite-phase signal and an in-phase noise with respect to the main path. By combining the output nodes of each path, signals are constructive throughout the adder whereas noise contributions are destructive and will be removed at the output. Inherent to the noise cancellation operation, the input signal experiences an increase of the voltage dynamic by a factor 2. This feature contributes to theoretically improve the voltage gain by +6 dBv.

The aforementioned noise cancelation process only concerns the white noise sources located in the main stage. Hence the noise of the auxiliary path holds, as well as non-white noise sources of the main stage, and the noise figure of a noise canceling circuit is not null.

However, the technique of noise canceling significantly relaxes the trade-off between input matching, noise and gain performances.

2. Common-gate based noise cancelling

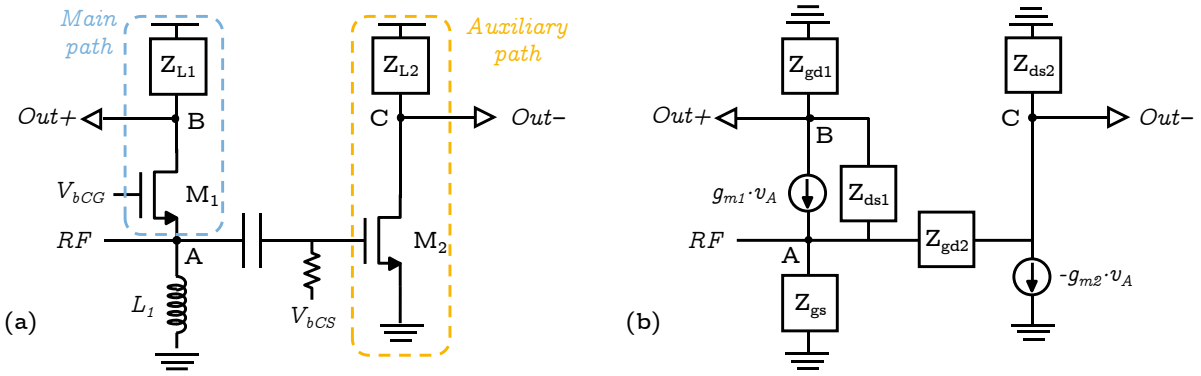


Figure 39 – Common-gate based noise cancelling LNA in (a) schematic; and (b) small signal model

Noise cancelling architectures have been widely investigated for the two last decades [25] one of the most popular topology is the common-gate based noise cancelling amplifier [26]. This architecture is illustrated by the Figure 39(a). A common-gate amplifier (M_1) acts as the main path and offers inherent wideband operation regarding the gain and the input matching but suffers from poor noise figure. The auxiliary path is composed with a common source stage (M_2) which senses the input voltage and achieves better noise performance. Another advantage of this architecture is to perform a single input to balanced output operation thus avoiding the use of an external balun which would introduce additional losses and noise. To account for parasites at the output node, the load is usually modeled by a low pass filter as presented in Equation 14. This section describes the conditions to perform simultaneous impedance matching, output balancing, noise cancellation and distortion cancellation.

Equation 14 – Amplifier load in common-gate path (i=1) and common source path (i=2)

$$Y_{Li} = 1/(R_{Li} + {}^{1}/_{j\omega C_{Li}})$$

The small signal equivalent circuit of the noise cancelling LNA is shown in Figure 39(b). The admittances at nodes A, B and C are proposed in Equation 15 considering the transistors M_1 and M_2 and the passive elements. For sake of clarity, the imaginary parts of admittances are neglected.

Equation 15 – Equations of small signal model impedances

$$Y_{ds1} = {}^{1}/_{Z_{ds1}} = g_{ds1} + j\omega C_{ds1} \approx {}^{1}/_{r_{ds1}}$$

$$Y_{dg1} = {}^{1}/_{Z_{dg1}} = \frac{1}{R_{L1}} + j\omega \cdot (C_{dg1} + C_{L1}) \approx {}^{1}/_{R_{L1}}$$

$$Y_{ds2} = {}^{1}/_{Z_{ds2}} = \frac{1}{R_{L2}} + g_{ds2} + j\omega(C_{ds2} + C_{L2}) \approx \frac{R_{L2} \cdot r_{ds2}}{R_{L2} + r_{ds2}}$$

$$Y_{dg2} = {}^{1}/_{Z_{dg2}} = j\omega C_{dg2} \approx 0$$

$$Y_{gs} = {}^{1}/_{Z_{gs}} = j\omega(C_{gs1} + C_{gs2}) - \frac{j}{\omega L_1} \approx 0$$

a. Impedance matching

Equation 16 – Common gate impedance

$$Z_{in,CG} = \frac{Z_{ds1} + Z_{dg1}}{1 + g_{m,CG} Z_{ds1}} = \frac{r_{ds1} + R_{L1}}{1 + g_{m,CG} r_{ds1}} \approx \frac{1}{g_{m,CG}}$$

The Equation 16 proposes an expression of the common-gate input impedance ($Z_{in,CG}$). Considering a high drain source impedance regarding the load and neglecting parasitic capacitances, the input impedance can be approximated to the transconductance inverse. Then a wideband real impedance can be achieved as long as reactive elements are negligible.

Equation 17 – Condition for impedance matching

$$g_{m,CG} = \frac{1}{R_s}$$

b. Gain balance

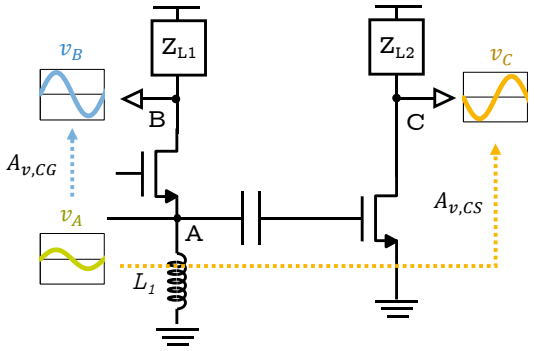


Figure 40 – Signal in common-gate based amplifier

Considering a power source connected at node A, the input signal is amplified by the main path and inverted in the auxiliary path. This single-to-differential topology acts as an active balun but imbalance between paths should be avoided. This section details the condition to prevent from imbalance.

Equation 18 – Gain over the main path

$$A_{v,CG} = \frac{v_B}{v_A} = \frac{1 + g_{m1}Z_{ds1}}{1 + {Z_{ds1}}/{Z_{dg1}}} = \frac{1 + g_{m1}r_{ds1}}{1 + {r_{ds1}}/{R_{L1}}} = g_{m,CG} \cdot R_{CG} = \frac{R_{CG}}{R_S}$$

For the common-gate path, the voltage gain ($A_{v,CG}$) is described by Equation 18. Considering a drain-source resistor significantly higher than the load resistor, the main path gain is determined by the transconductance ($g_{m,CG}$) and the output load (R_{CG}). Due to the input matching condition expressed in Equation 17, the gain is then defined by the ratio between load resistor (R_{CG}) and source impedance (R_S). To have a balanced operation, the voltage gain in the common source path should be equal to the gain of common-gate path. It leads to the second design condition described in Equation 19.

Equation 19 – Condition on path gains

$$A_{v,CG} = A_{v,CS} \Leftrightarrow g_{m,CG} \cdot R_{CG} = g_{m,CS} \cdot R_{CS}$$

Considering that the two previous conditions are fulfilled, the voltage gain (A_V) is then expressed in Equation 20. Compared to a conventional architecture with a balun and a differential common source or common gate amplifier, the noise cancelling amplifier acts as an active balun-amplifier and performs a double voltage gain at same power consumption.

Equation 20 – Voltage gain of the amplifier

$$A_v = 2 \cdot g_{m,CG} \cdot R_{CG} = \frac{2 \cdot R_{CG}}{R_S}$$

c. Noise cancellation

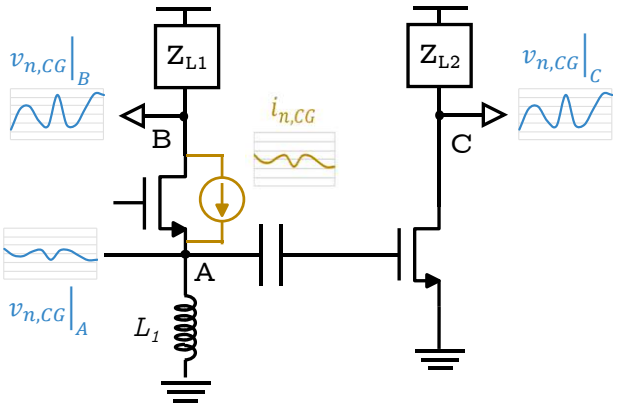


Figure 41 – Common-gate noise in a noise cancelling LNA

The Figure 41 illustrates the noise cancellation mechanism in a low noise amplifier. The thermal noise current generated by M_1 (i_n) generates correlated anti-phase noise voltages at the input A ($v_{n,A}$) and the output B ($v_{n,B}$) expressed in Equation 21. These expressions include a

factor equals to the voltage division between the input resistance and the source resistance. It is ½ under perfect input matching conditions.

Equation 21 – Noise generated at the main path output and amplifier input

$$v_{n,A} = \frac{R_{in,CG}}{R_{in,CG} + R_S} \cdot i_n \cdot R_S$$

$$v_{n,B} = -\frac{R_{in,CG}}{R_{in,CG} + R_S} \cdot i_n \cdot R_{CG}$$

The input noise voltage is then sensed by the auxiliary path at node A and amplified by the common-source path. The noise voltage ($v_{n,C}$) at auxiliary output, node C, is expressed in Equation 22. If input matching (Equation 17) and balanced operation (Equation 19) conditions are completed, the output noise voltage in B and C, originally generated by the common-gate noise current, are in-phase and equals as illustrated in Figure 41. Hence the thermal noise of M_{CG} is cancelled out.

Equation 22 – Voltage noise at C output

$$v_{n,C} = -A_{v,CS} \cdot v_{n,A} = -g_{m,CS} \cdot R_{CS} \frac{R_{in,CG}}{R_{in,CG} + R_S} \cdot i_n \cdot R_S$$

$$v_{n,C} = -g_{m,CG} \cdot R_{CG} \frac{R_{in,CG}}{R_{in,CG} + R_S} \cdot i_n \cdot R_S = v_{n,B}$$

d. Distortion cancellation

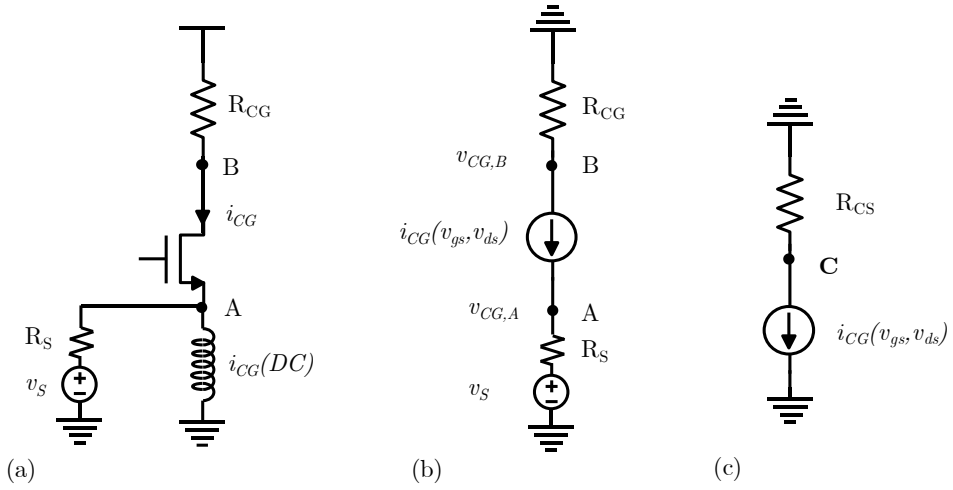


Figure 42 – (a) Schematic of the common-gate path; (b) Small signal equivalent model of the common gate path; (c) Small signal equivalent model of the common-source path

Simultaneously to noise, weak non-linearities of the matched common-gate device are also cancelled. Considering a high impedance for choke L_1 inductor, the common gate path (Figure 42(a)) is equivalent to the circuit illustrated in Figure 42(b). Considering weakly

nonlinearties, the source signal (v_s) creates a nonlinear current in common gate path (i_{CG}) which is converted into voltage at the input A ($v_{CG,A}$). This voltage is decomposed in a Taylor series as detailed in Equation 20.

Equation 23 – Voltage at the input with its decomposition in a linear and unwanted nonlinear term

$$v_{CG,A} = \sum_{n=1}^{+\infty} a_n v_s^n = a_1 v_s + \sum_{n=2}^{+\infty} a_n v_s^n = a_1 v_s + v_{NL}$$

Considering the expression of the approximated gain of both paths detailed in section b, the output voltages of CG and CS stages are expressed in Equation 24. When the difference of output voltages is performed, the nonlinear terms is then cancelled, and only linear terms remain. It leads to improve the linearity of the amplifier for weak non linearities of common-gate path. Still the non-linearities of the CS path remains like was the noise contribution.

Equation 24 – Voltages at the output (nodes B & C) due to nonlinear behavior

$$v_{CG,B} = i_{cg} \cdot R_{CG} = \frac{v_s - v_{CG,A}}{R_S} \cdot R_{CG} = \left((1 - a_1) \cdot v_S - v_{NL}\right) \cdot \frac{R_{CG}}{R_S}$$

$$v_{CS,C} = -v_{CG,A} \cdot \frac{R_{CG}}{R_S} = -(a_1 \cdot v_s + v_{NL}) \cdot \frac{R_{CG}}{R_S}$$

e. Conclusion

In this section, a brief analysis of common-gate based noise cancelling amplifier is proposed. In this topology, a common-gate amplifier acts as a main path while the auxiliary path uses a common-source for cancelation. A wideband real input impedance can be achieved by adjusting common-gate transconductance. Besides, to maintain a balanced operation the signal must experience the same conversion gain in each path. Considering these two design conditions, the channel noise current generated by the common-gate transistor is then cancelled at the output.

In literature, this topology presents several advantages. First, a wideband behavior is assured thanks to the common-gate amplifier as expected from a non-resonant matching. Simultaneously, the noise of this path is cancelled by the auxiliary path, and the noise figure can be reduced with specific design of the CS path. Besides, this architecture offers an inherent single-to-differential behavior which could lead in some cases to superior performances with respect to fully differential amplifier solutions with balun.

II. RF Noise Cancelling Blixer

Until few years, the emergence of Internet of Things (IoT) leads to change paradigms on connectivity and mobility. The development of multiple sensor platforms and the

improvement of their connectivity induce major evolutions in application fields such as: smart cities, transportation, infrastructure, healthcare or industry. In order to integrate more and more sensors in wireless local networks, multiples standards are proposed: Bluetooth, ZigBee, Wi-Fi Ha-Low [27].

To address the challenge of interoperability in IoT deployment, low power multi-standard radios are mandatory. Substantial efforts are dedicated to reduce the cost and the form factor by minimizing the number of off-chip devices, and by increasing the silicon integration. Besides the constrain on the form factor drastically limits the power supply capability of the devices. As consequences, the power efficiency is of utmost importance in the development of Radio modules. In the transmitter part, this issue is addressed by the class of operation of the power amplifier. In the receiver (Rx) part, all the functions featuring the RF front end are concerned, and among the most critical ones is the frequency down-conversion.

Previously, in section I, the principle of noise cancelling applied to amplifier is detailed and literature shows competitive performances. Combining an active mixer with a noise cancelling transconductance amplifier, "Blixer" topology can achieve very high performances over a wide bandwidth [28]. Originally proposed for software-defined wideband radio receivers, mixer-first architectures using noise cancelling principle can perform low noise figure and high linearity as requested by the multiple standards of the RF band. In this section, a Blixer is proposed to address low power IoT market with specific techniques to reduce the power consumption.

1. Noise cancelling applied to mixer

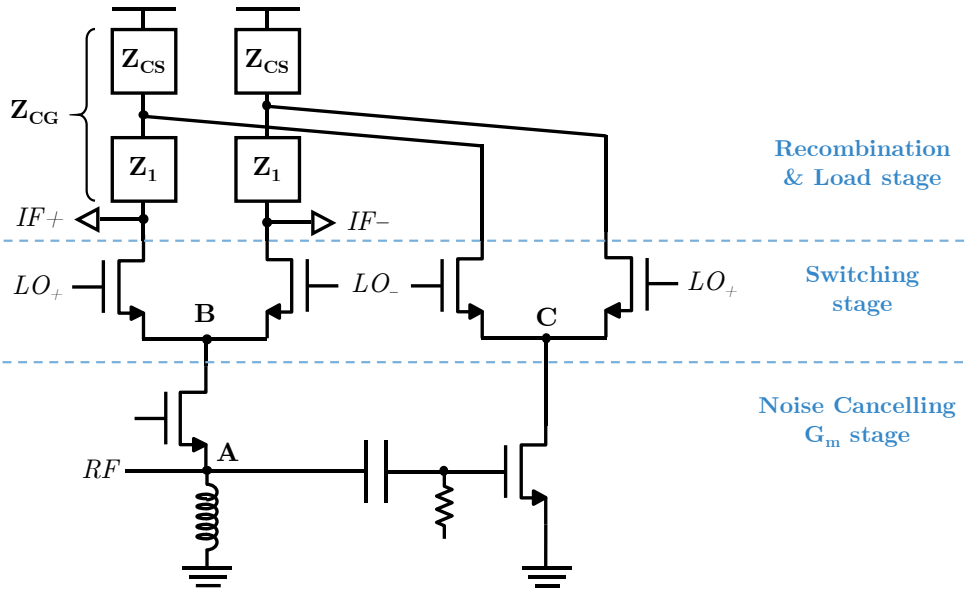


Figure 43 – Basic topology of blixer

The Blixer was originally released in [28] and merge a noise cancelling balun-LNA with a current commutating mixer. The basic topology featuring three different stages is depicted in Figure 43. The input *transconductor* is based on a noise cancelling architecture and cascoded with a *switching quadrature stage* which performs the mixing operation. As NMOS pairs are periodically switched on and off, the input impedance of mixing stage is low enough to validate the matching condition. The currents delivered by the CG and CS transistors flow to the switches and are downconverted to an Intermediate Frequency. The *baseband stage* performs the proper recombination of IF signals to maintain balanced operation and to achieve the thermal noise cancelation of CG stage.

a. Noise cancellation in a mixer

In the Blixer topology, the condition to design a noise cancelling architecture are similar to amplifier ones. Considering a low impedance at nodes B and C; the input impedance is then dominated by the common-gate transconductance as exposed in Equation 17. As the RF signal is alternatively switched to IF+ and IF-, the baseband load stage is modified to maintain the condition exposed in Equation 19. In Figure 44, LO switches are alternatively turned ON and OFF. For common source path, the signal downconverted voltage at switch drains is sensed through a potential divider composed by Z_1 load and the switch output impedance. When the switch is OFF, its impedance can be considered infinite. It leads to sense the output voltage can through the Z_1 load to IF. Otherwise, the cancellation of the noise current of common-gate transistor is performed in a similar way.

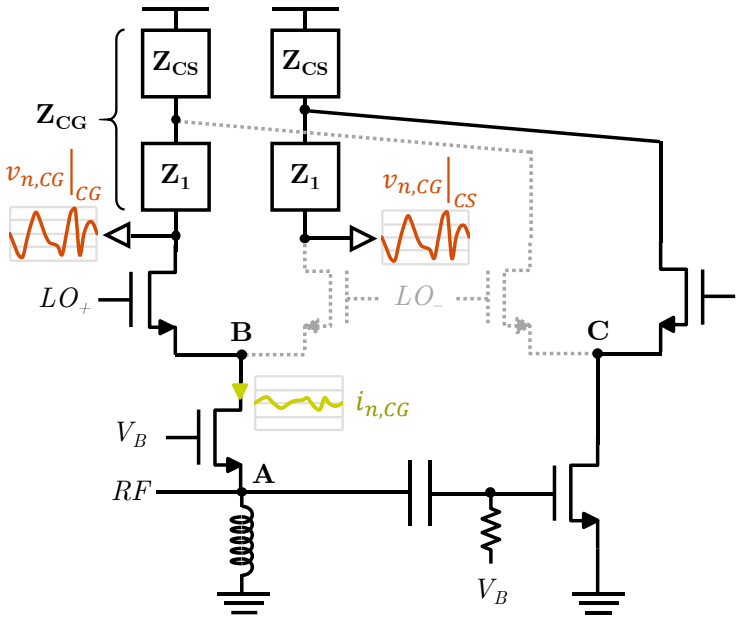


Figure 44 – Noise cancellation in mixer

b. Attractive properties of Blixer

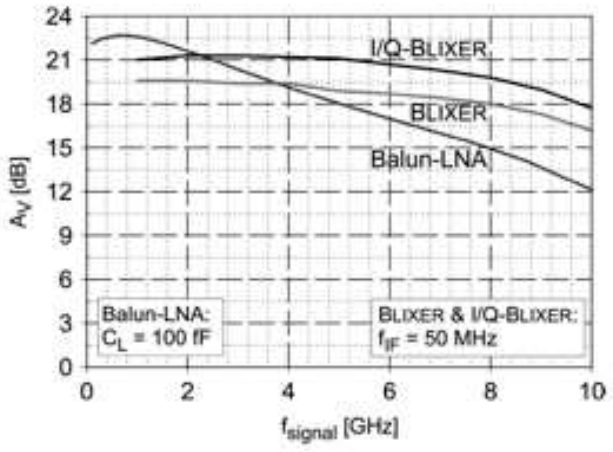


Figure 45 – Gain over RF band for the noise cancelling LNA, basic Blixer and I/Q-Blixer [28]

In advanced RF CMOS technologies, Blixer topology exhibits interesting properties compared to noise cancelling LNA architectures. First the bandwidth is significantly higher in a mBixer than an amplifier as illustrated in Figure 45 [28]. Whereas noise cancelling amplifier should maintain a sufficient impedance at its output to achieve good performances, blixer has only low impedance RF nodes. Dominated by switch ON resistance, the tail impedance is relatively low and is less impacted by the parasitic capacitances.

As discussed previously, the blixer performs noise cancellation in the baseband stage. According to Figure 44, both CG and CS paths contribute equally to both IF± outputs which requires a symmetrical design of the baseband stage. These two considerations lead to improve the quality of the output signal balance.

As exposed in section I.2.d, noise cancelling architectures also cancel third order distortions generated by the common gate transistor. As mixing stage is assumed linear in hard-switched operations and passive loads do not introduce distortions, the only source of non-linearities arises from the common source transistor.

2. Noise figure improvement

According to section c, if the conditions for input matching (Equation 17) and balanced operation (Equation 19) are completed, the thermal noise of common gate transistor is cancelled. Therefore, common source noise becomes the main contributor of thermal noise. The spectral power density of noise of the common-source transistor is expressed in Equation 25(a).

Equation 25 – (a) Noise contribution of common source transistor; (b) Noise contribution with the topological factor (n) in common source sizing

$$(a)\ \frac{\overline{v_{n,CS}{}^2}}{\Delta f} = \frac{2}{\pi}\gamma kT g_{m,CS} R_{CS}{}^2 \quad ; \quad (b)\ \frac{\overline{v_{n,CS}{}^2}}{\Delta f} = \frac{2}{\pi}\gamma kT \frac{g_{m,CG} R_{CG}{}^2}{n}$$

To reduce the contribution of the auxiliary path in the noise figure (Equation 25(b)), the transconductance $g_{m,CS}$ is increased by a factor n compared to the transconductance $g_{m,CG}$ (Equation 26). The transconductance unbalance is compensated by a proper sizing of the resistive load, to maintain the balun operation at IF port.

Equation 26 – Noise reduction relation of common source transistor

$$g_{m,CS} = n \cdot g_{m,CG} \; ; R_{CS} = \frac{R_{CG}}{n}$$

This technique leads to a substantial reduction of the noise figure illustrated in Figure 46. Increasing the common source transconductance $g_{m,CS}$ by a factor 3 improves the noise figure by 2-dB. However, it also doubles the power consumption of the mixer which is not suited for low power purpose. This issue is further addressed in the section 3.

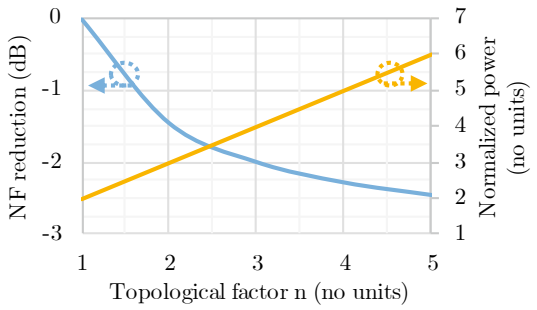


Figure 46 – Impact of topological factor (n) on NF (dB) and normalized power (no units)

3. Low power improvement

As discussed in the introduction of section II, the power consumption is critical for IoT applications. To address low power requirements, specific techniques are proposed to reduce the current with a moderate impact on RF performances. This section details three implemented techniques with an improvement of auxiliary path circuits, a design in moderate inversion region for all transistors and the use of impedance matching to reduce the overall power consumption.

a. Auxiliary path improvement

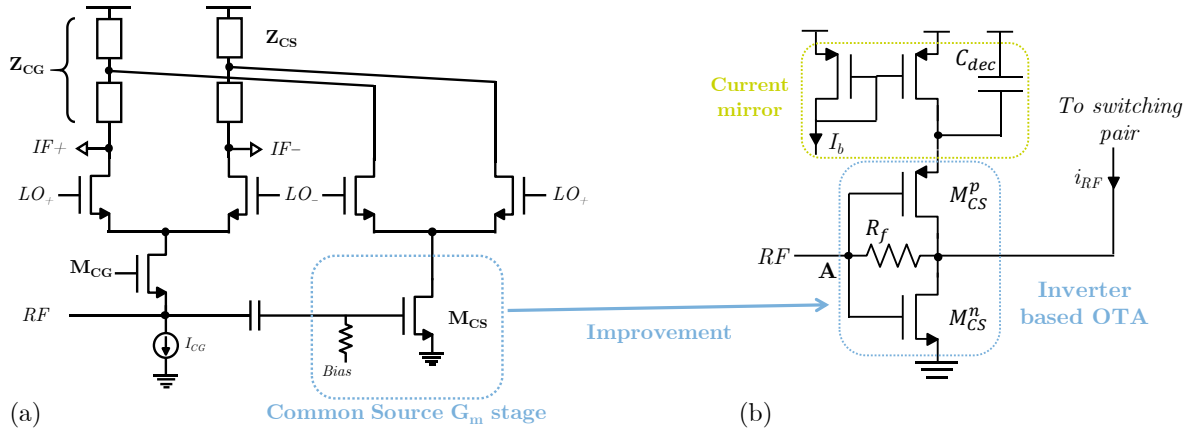


Figure 47 – (a) Schematic of noise cancelling mixer; (b) Auxiliary path transconductance improvement with a current-reuse OTA

As previously discussed, a large transconductance for M_{CS} leads to a large DC current, and to increase accordingly the supply voltage to maintain respectively the transistor of the transconductance stage in saturation mode and the LO stage in hard-switching operation. In this section, a circuit technique on the auxiliary path is investigated to reduce the overall power consumption. The architecture proposed in Figure 47(b) exploits an inverter based OTA in the common source path to boost the transconductance $g_{m,CS}$, according Equation 13, and to improve the current efficiency. The transconductor is steered by a PMOS current mirror biased with I_b.

Equation 27 – Transconductance of the auxiliary path

$$g_{m,CS}^{aux} = g_{m,CS}^{n} + g_{m,CS}^{p} - \frac{1}{R_f} \approx g_{m,CS}^{n} + g_{m,CS}^{p} \text{ for } R_f \gg g_{m,CS}^{n} + g_{m,CS}^{p}$$

Since the same current is reused in $M_{2\text{-}n}$ and $M_{2\text{-}p}$, the power efficiency (g_m/I_D) of the CFS stage is significantly improved. Besides the inverter-based transconductance stage is designed to have no DC current flowing through the switching pairs which allows to reduce the nominal supply voltage, and the overall power consumption as well.

b. Design in moderate inversion

To work out the best trade-off between RF performance and current efficiency, the MOS devices are biased at the maximum of $g_m.f_T/I_D$ [29]. This figure of merit represents the current efficiency at high frequency of a MOS transistor. It is drawn for 28-nm NMOS devices in Figure 48. In weak inversion region, a very high current efficiency is achieved but the transition frequency is too low to target RF applications. In strong inversion region, transistors present high f_T but suffer from a poor efficiency. The $g_m.f_T/I_D$ is maximum in the region of

moderate inversion, known as sub-threshold operation. It's the best trade-off for RF performance regarding the current efficiency. Each path of the transconductor stage is biased by a current mirror to properly operate the transistors in the moderate inversion region.

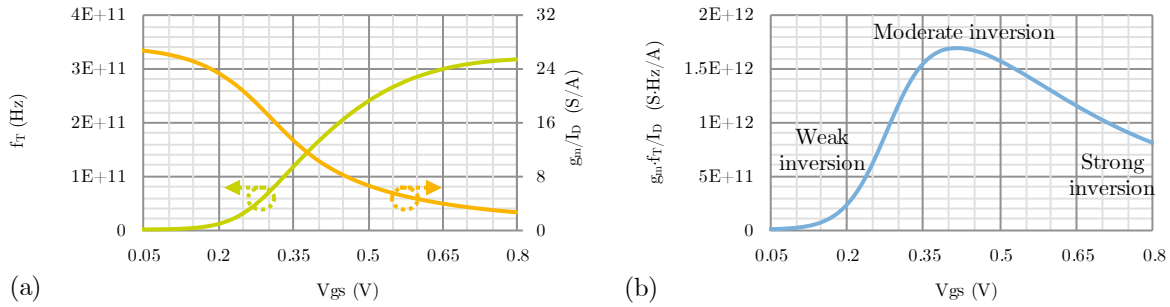


Figure 48 – Different FoM of 28-nm transistor regarding V_{gs}: (a). f_T & g_m/I_D; (b). $g_m.fT/ID$

c. Impedance matching

To account for mismatch and the frequency dependence of impedance at high frequency, the input/output matching is evaluated through the return loss S_{ii}. For active circuits, it is admitted the input matching is satisfactory if the level of S_{11} is lower than -10 dB. This condition is exploited in the proposed mixer to further reduce the power consumption.

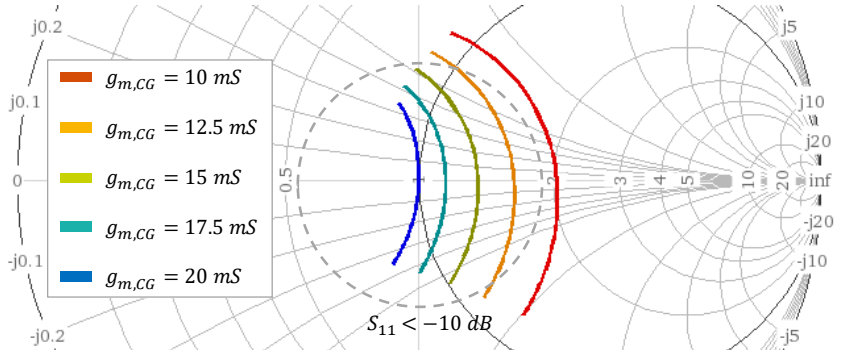


Figure 49 – Input matching (S11) between 1-GHz and 6-GHz for various $g_{m,CS}$ values and a source resistance Rs = 50-Ω

According Equation 17, the input impedance of the proposed mixer is mainly controlled by the common-gate transconductance ($g_{m,CG}$). In Figure 49, the input return loss S_{11} of the mixer is reported on a Smith chart from 1 to 6-GHz for various $g_{m,CG}$. The corresponding power consumption is reported in Figure 50. To complete the input matching conditions (S_{11}<-10dB), the arc is expected to be in the dotted circle in Figure 49. A very low S_{11} is achieved when $g_{m,CS}=1/R_S$=20-mS, blue curve, which implies a power consumption of 7-mW, Figure 50. Interestingly, the power consumption can be reduced by a factor of three with a $g_{m,CS}$ of 15m-S, while maintaining the input matching conditions. This trade-off between the power consumption and the input matching is further exploited in this mixer.

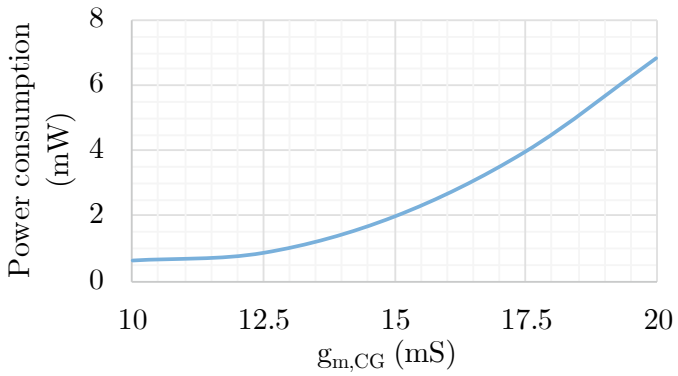


Figure 50 – Power consumption regarding the $g_{m,CG}$

4. Performances of implemented RF-Blixer

A simplified schematic of the downconverter is proposed in Figure 51. Based on a noise cancelling topology, it includes the different improvements presented in sections 2 and 3. The circuit is implemented in 28-nm CMOS bulk technology and the chip micrograph is shown in Figure 52. The mixer occupies a silicon area of only 0.04-mm², including the input inductor L_{IN} which is also used as an ESD protection. This section details the measurement results and presents post layout simulations regarding PVT variations. For these simulations, industrial operation temperature is considered with variations from -20°C up to 85°C while a 3% variation of supply voltage is estimated.

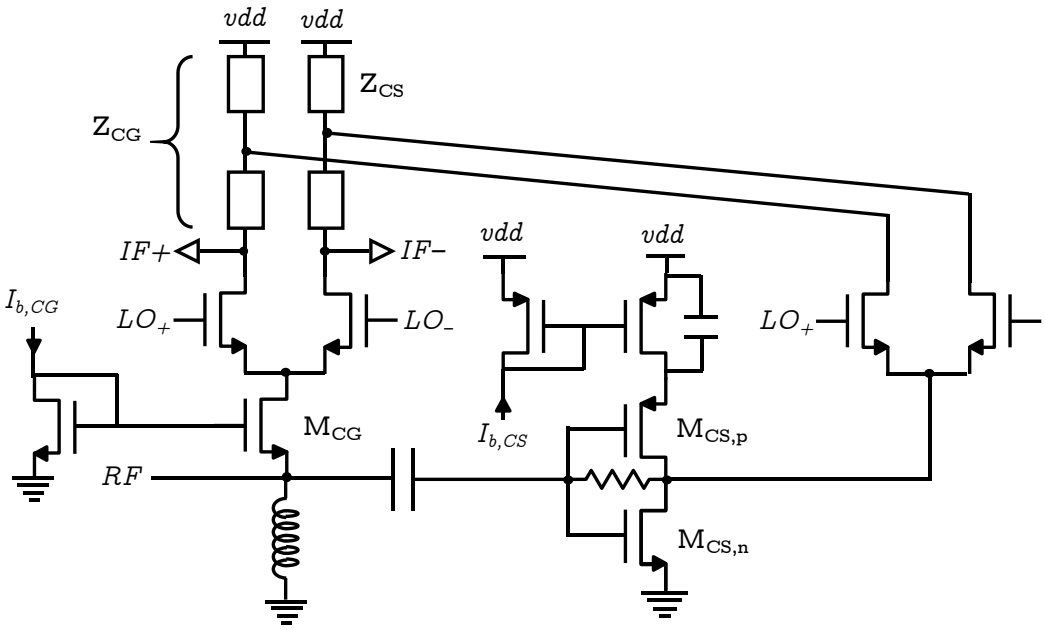


Figure 51 – Schematic of proposed mixer

To address the different trade-offs, two modes of operation are defined. The *"nominal mode"* is set with a $g_{m,CG}$ of 17.5-mS under a supply voltage of 1.2-V. This mode proposes the

best RF performances for a moderate power consumption of 4-mW. In the *"power saving mode"*, the $g_{m,CG}$ is 15-mS, the power consumption is reduced to 2-mW and the supply voltage is 0.9V. All the post layout simulations are proposed for the "*nominal mode*".

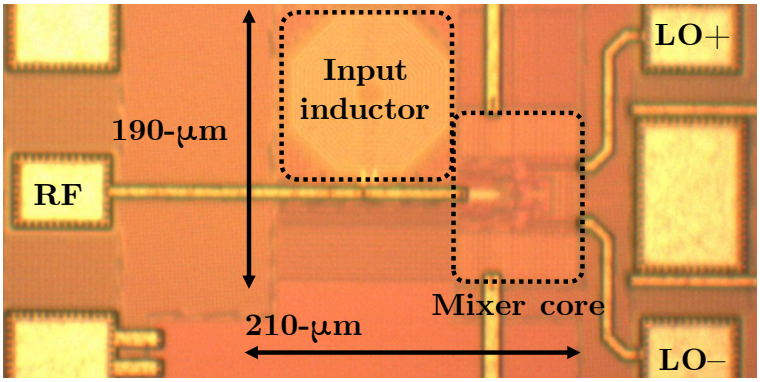


Figure 52 – Micrograph of the implemented downconverter

(1) Input matching

The measurement of the input return loss, Figure 53(a), shows that S_{11} is lower than -10dB from 800MHz to 6GHz, and it is not really affected by the mode of operation. A bandwidth of almost one decade is achieved which demonstrates the capability of common gate configuration to ensure a wideband input matching operation. Post layout simulations in PVT corners shows an important variation of input matching (Figure 53(b)). As the circuit operates in weak inversion region, the definition of the CG transconductance is highly impacted by the variation of threshold voltage and leads to limited matching in slow corner. However, the PVT spread can be reduced by adjusting the current in the CG path, Figure 53, during the test of the chip.

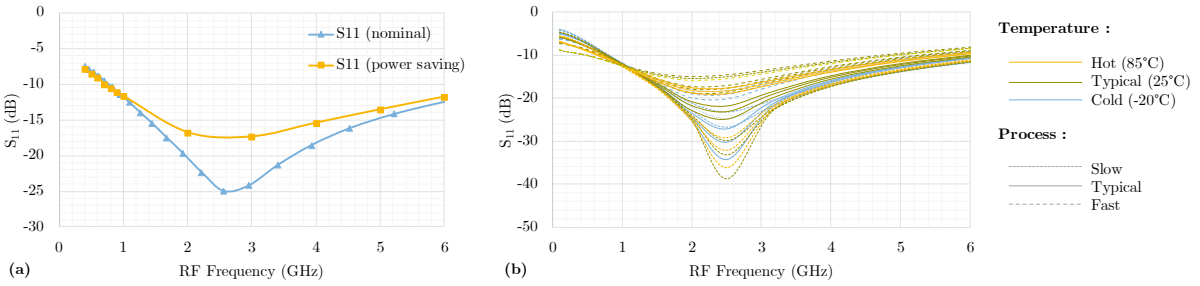


Figure 53 – Input matching: (a) for measurement in both modes; (b) for post-layout simulations in PVT variations for nominal modes

(2) Conversion gain

The measured conversion gain, Figure 54(a), is maximum at 2GHz and reaches 15dB in nominal mode. In power saving mode the reduced transconductance decreases the conversion gain to 11dB. The -3dB bandwidth covers more than a decade in the two modes, with respectively 0.5-7GHz in nominal mode, and 0.5-6GHz in. power saving mode. In post layout

simulations, Figure 54(b), the gain presents an important variation regarding process from 12dB to 19dB. The measured IIP3, Figure 54(a), is almost constant between 1 and 4GHz in both modes with a typical value of 0dBm.

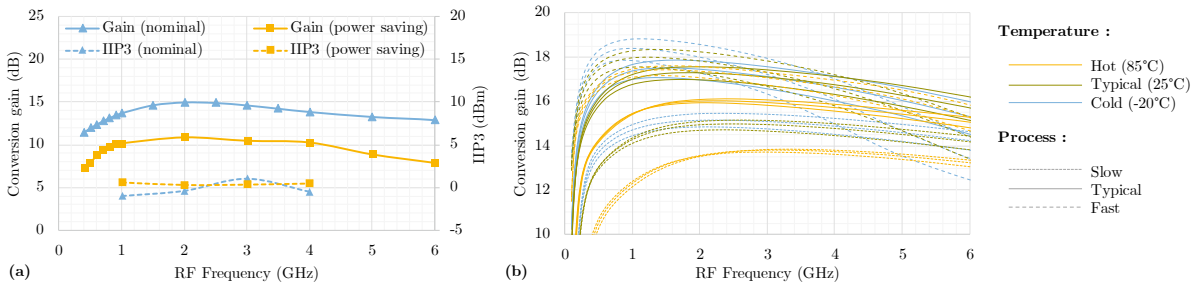


Figure 54 – (a) Conversion gain and IIP3 in measurement for both modes; (b) Conversion gain in post layout simulations in PVT for nominal mode

(3) Noise figure

Figure 55(a) reports the single side band noise figure (NF_{ssb}) versus the RF frequency at 10MHz IF. The noise cancelation is originally designed for nominal mode operation, the minimum NF_{ssb} is 6dB at 2GHz and does not exceed 8dB from 1GHz to 6GHz. In power saving mode, the minimum NF_{ssb} increases to 7dB at 2GHz. However, the frequency response is not as flat as in nominal mode since the NF_{ssb} reaches 13dB at 6GHz. Interestingly, the measured NF is 2dB lower than post-layout simulations. The measurements of the NF have been performed over different chips and many times. Two combined reasons are suspected for this discrepancy. The simulation of noise cancelling by the simulator could be miss evaluated. The transistor gate resistor is large in advanced silicon technology, typically below 65nm. The exact value of PMOS gate in the CS stage can significantly impact the NF. This phenomenon has already been experienced with a current re-use LNA in another 28nm process. Besides, the NF also presents an important variation up to 14dB especially at slow corner in post layout simulations (Figure 55(b)).

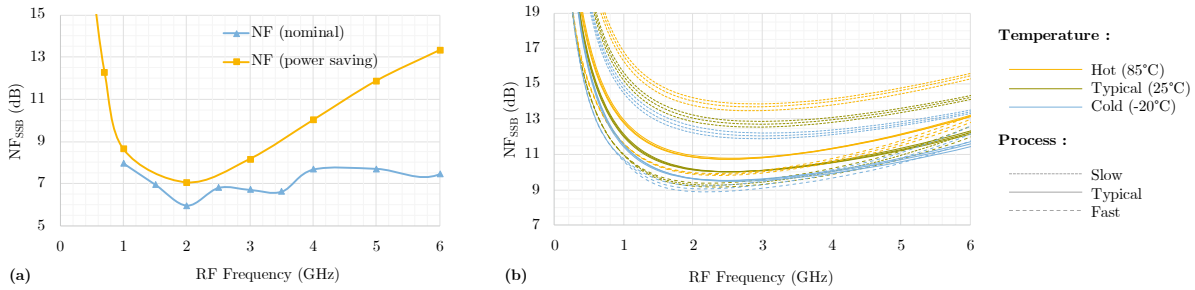


Figure 55 – Single side band NF (a) in measurement for both modes; (b) in post layout simulations with PVT variations for nominal mode

5. Conclusion

The Table 10 shows a comparison between the proposed mixer and some works of the state of the art. The proposed design presents competitive RF performances with an interesting trade-off between the die area and the power consumption. First, the bandwidth is significantly higher than most of the others low power downconverters. Some references, [30], [31] and [32], include a baseband analog chain with a large gain feature to compensate for the mixer losses. Besides, the proposed mixer achieves a low noise figure, close to the best performance of the referenced works which are I/Q architectures. The silicon footprint is the smallest with [9]. Some references such as [30] and [33] are designed to achieve very low power but suffer from a dramatically reduced bandwidth. The proposed mixer covers a large bandwidth at a moderate power consumption.

This first RF mixer dedicated to IOT applications demonstrates the inherent wideband behavior and active balun operation of a noise canceling architecture. It further allows to experiment some circuit techniques applied to frequency down conversion: the reduction of the NF in a noise cancelation topology by beta factor balancing, the improvement of the current efficiency in a transconductance stage throughout current reuse and transistor biasing. Some of these techniques will be further exploited to implement mm-Wave circuits when it is possible.

Table 10 – State of the art of low power downconverters (NF_{DSB}, $^{+}$ including baseband, ** including pads)*

Parameter	[28]	[30]	[31]	[32]	[33]	[34]	This work	
CMOS tech (nm)	65	28	28	65	65	65	28	
Architecture	Active IQ-mixer	LNTA IQ-mixer +BB	LNTA IQ-mixer +BB	Active IQ-mixer +BB	LNTA I-mixer	Active I-mixer	Active I-mixer	
VDD (V)	1.2	0.9	1.8	0.6	0.6	1.2	0.9	1.2
Bandwidth (GHz)	0.8-7	0.6	0.8	1.3	0.8	1-10	0.8-4	0.8-6
Conv. gain (dB)	18	53.3^{+}	43.4^{+}	57^{+}	22.8	12.8	10	15
NF (dB)	5.5*	6.5*	7.5*	8.5*	8	7.5*	7	6.2
IIP3 (dBm)	-3	-8	6	-6	-21	-5	0.5	-1
Power (mW)	16	0.35	4.3	1.7	0.064	5	2	4
Area (mm^2)	0.01**	0.1	0.22	0.24	0.22	0.01	0.04	

III. 77GHz Noise Cancelling Mixer

In BiCMOS technologies, RF Front-End usually features active mixers due to their interesting trade-off between gain, noise figure and linearity. As discussed in Chapter I.1.2.2, a -5dBm compression point is critical for rear target measurement while a high conversion gain, typically higher than 10dB, is necessary to reduce the noise contribution of baseband chain.

This section explores the architecture of active mixer for 77GHz downconverter in RF-CMOS technologies.

As radar may work in diverse environments, the downconverter may have enough robustness to process corners, to operate over a large range of temperature and to support a variation of its supply voltage of +/- 5%. According section II, the noise cancelling topology based on common gate presents inherent wideband operation and, for this reason, a better immunity to PVT variations. Some techniques, such as the beta factor and the current-reuse OTA, implemented in the RF demonstrator cannot be exploited at millimeter-Wave due to the large parasitic capacitances at critical nodes. However, the biasing of transistors in moderate inversion is considered when it is possible.

The issue of 1/f noise in CMOS technologies is first explored for active mixers and some techniques to reduce its impact are investigated. The second part proposes to model the noise cancelling mixer topology for millimeter-Wave applications. Finally, the implementation of a noise cancelling mixer with flicker noise reduction at 77GHz is proposed with post-layout simulations in PVT corners and measurement results in typical case.

1. Flicker noise in CMOS active mixers

For many years, the flicker noise is identified as one of the main issues of CMOS active mixers [35]. A lot of work has investigated on it in order to reduce its impact on mixer performance. This sub-section first details the generation of 1/f noise in a switching pair throughout direct and indirect mechanisms. Then, it explores the different techniques to reduce it and discusses their interest in the millimeter-Wave domain. Finally, the last part focuses on the techniques exploited in the implemented mixer.

a. Flicker noise in CMOS switching pair

Equation 28 – Gate-referred flicker noise voltage where K_F is a process parameter, C_{ox} is the oxide capacitance, W and L are the width and length of the transistor and f the operating frequency

$$V_n(f) = \frac{K_f}{W\,L\,C_{ox}} \cdot \frac{1}{f}$$

In MOS transistors, flicker noise originates from electron tunneling through traps in the oxide to the gate causing fluctuations through carrier number and mobility, and consequently drain current flickering. The gate-referred noise voltage (Equation 28) increases with the reduction of operating frequency. In 28nm RF CMOS technology, it becomes predominant below 10-MHz which corresponds to the low-end of radar IF bandwidth. As radar solutions use thinner CMOS technologies to increase digital integration and transition frequency, flicker noise tends to increase.

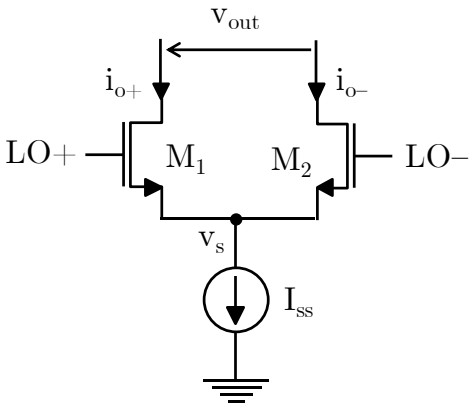


Figure 56 – Switching pair considered in the flicker noise analysis

In active mixers, the flicker noise impacts the noise performance during the switching event through a direct and an indirect mechanism. In this section, the mixer analysis is simplified to a switching pair cascoded on top of a current source modeling the RF transconductance stage as illustrated in Figure 56. As the noise of the transistors are uncorrelated, they can be superposed in the following analysis.

(1) Direct mechanism due to LO sine waveform

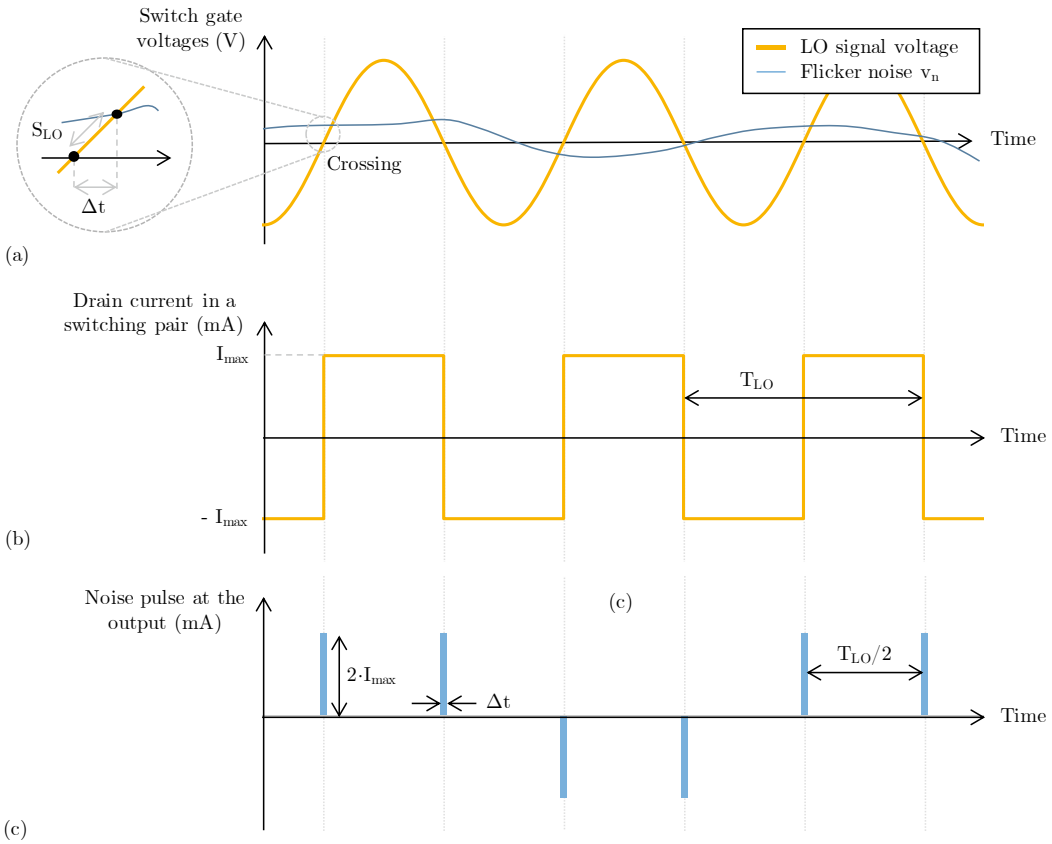


Figure 57 – Signals in a switching pair: (a) LO± at switch input / gates; mixer output current composed with (b) a square-wave output currents (mA) and (c) noise pulse train at the output

The direct mechanism is linked to the finite slope of LO sine waveform, Figure 57 (a). Even if we assume a sharp transition during the switching event, which would be very optimistic in millimeter-Wave domain, the noise voltage V_n modulates the drain current during the LO± crossing as illustrated in Figure 57(a). As consequences, the switching event shifts by a (very) small-time amount Δt which depends on the LO slope (S_{LO}) and the flicker noise (V_n). At the mixer output, it causes a pulse train of random width (Δt) with a fixed amplitude of $2 \cdot I_{max}$ at twice the operating frequency, Figure 57(c), superimposed to the square wave form of the drain current, Figure 57(b).

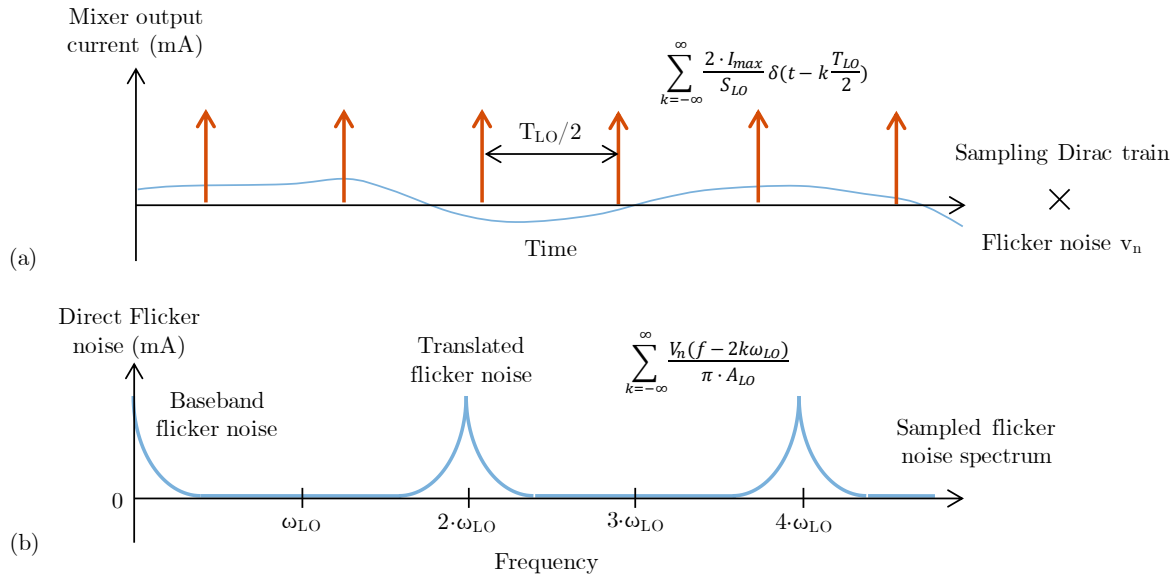


Figure 58 – Mixer output direct flicker noise current (a) Time model of the noise pulse train with a sampling Dirac comb and the v_n flicker noise; (b) Frequency model of the noise pulse train

As Δt is significantly lower than the operating frequency, this noisy pulse train is then modeled as a noiseless Dirac comb sampling the long-time variant flicker noise (V_n) as illustrated in Figure 58(a). In frequency domain, the sampling of the noise signal is considered as the convolution of a $2 \cdot \omega_{LO}$ Dirac comb with the flicker noise spectrum thanks to Fourier transformation. Illustrated in Figure 58(b), the output flicker noise spectrum shows the frequency shift of the flicker noise at multiple harmonics of $2 \cdot f_{LO}$. The high frequency terms do not impact the downconverter performance but the baseband flicker noise current $i_{n,direct}$ degrades the IF signal. Equation 29 describes this noise current induced by flicker noise direct mechanism.

Equation 29 – Flicker noise current in a switching cell due to direct mechanism (For a sine-wave LO: $S_{LO} \cdot T_{LO}$ is equivalent to $4\pi \cdot A_{LO}$ with A_{LO} the amplitude of the LO signal)

$$i_{n,direct}(f) = \frac{2}{T_{LO}} \cdot 2I_{max} \cdot \Delta t = \frac{2}{T_{LO}} \cdot 2I_{max} \cdot \frac{V_n(f)}{S_{LO}} = \frac{4\, I_{max}}{S_{LO} T_{LO}} \cdot V_n(f) = \frac{1}{\pi} \cdot \frac{I_{max}}{A_{LO}} \cdot V_n(f)$$

(2) Indirect mechanism due to LO sine waveform

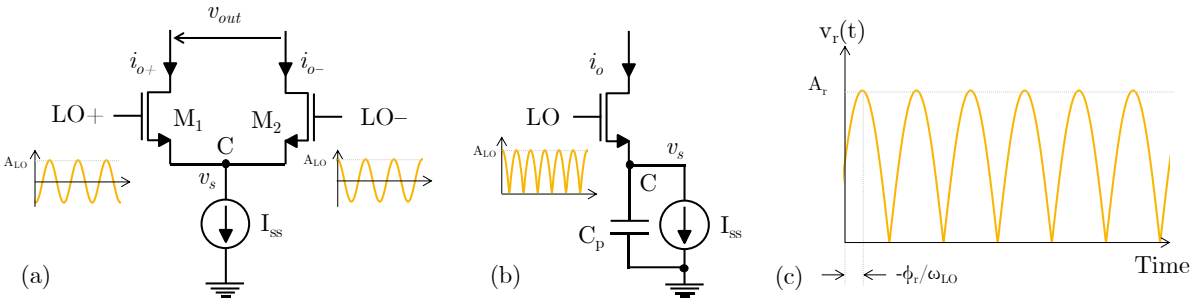


Figure 59 – (a) Switching pair with LO sine waveform; (b) Source follower model with a rectified LO sine waveform; (c) Rectified sinewave linked to LO waveform.

The generation of flicker noise is also due to parasitic capacitance at the switch tail node. Depending of LO frequency, this mechanism leads to significant noise emission in millimeter-Wave domain. The overall principle of this noise generation is illustrated in Figure 59(a), the LO switch transistors are modeled as a source follower continuously connected to the tail (node C) when it is ON.

Equation 30 – Amplitude of tail voltage rectified sinewave

$$A_r = A_{LO} \cdot \frac{g_{ms}}{\sqrt{g_{ms}^2 + \left(C_p \omega_{LO}\right)^2}}$$

When a sinewave LO is applied to the gate of a switching transistor, it is transferred to the source node C when the transistor is ON. As the differential pair is driven by anti-phase voltage sources, the voltage waveform at node C is modeled as a rectified sine-wave, Figure 59(b). The amplitude A_r and the phase ϕ_r, relative to the LO signal, of the rectified sine-wave are expressed respectively in Equation 30 and Equation 31.

Equation 31 – Phase difference between LO and tail voltages

$$\phi_r = \arctan\left(\frac{C_p \omega_{LO}}{g_{ms}}\right)$$

The rectified sine waveform is then downconverted by the switching cell. The LO sine waveform leads to a noisy mixing operation due to direct mechanism. It creates a flicker noise current at the mixer output evaluated to Equation 32.

Equation 32 – Flicker noise current due to LO waveform and tail capacitance

$$i_{o,n} = \frac{4}{T_{LO}} \cdot \int_{-\frac{\Delta t}{2}}^{\frac{\Delta t}{2}} C_p \frac{d\, V_r(t)}{dt}\, dt \Leftrightarrow i_{o,n}(f) = -\frac{C_p \omega_{LO}}{\pi} \cdot V_n(f) \cdot \frac{g_{ms}^2}{g_{ms}^2 + \left(C_p \omega_{LO}\right)^2}$$

(3) Indirect mechanism due to gate noise

The analysis of the two previous mechanisms of flicker noise generation suggests that a square-wave LO waveform would avoid the generation of flicker noise in an active mixer. Unfortunately, the indirect mechanism keeps on generating flicker noise due to the source follower behavior even with a square-wave drive. For this analysis, the signal at switches input can be decomposed on the superposition of the flicker noise voltage and the LO waveform which can be sinus or square wave. Without loss of generality, the Figure 60(a) features a LO square waveform on M_1 and M_2 transistors and a flicker noise voltage. These noise voltages are fully uncorrelated, the flicker noise of the overall switching cell is associated to M_1 transistor without loss of generality.

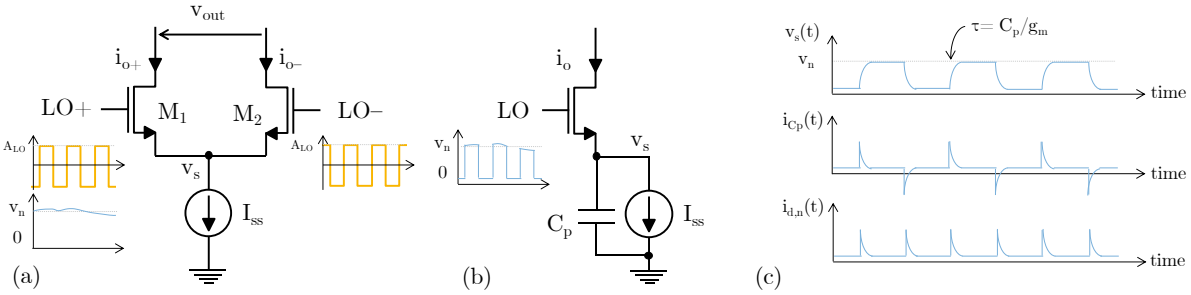


Figure 60 – (a) Switching pair with LO sine waveform and the vn gate noise; (b) Source follower model with modelized noise during ON state; (c) Tail voltage and currents due to vn noise

This generation mechanism is represented in Figure 60(b). The switching transistor acts as source follower during its ON state. The square wave modulated by the noise voltage v_n is transferred to the switch tail, charging and discharge the parasitic capacitance C_p. The time response of this RC load generates a current noise $i_{n,Cp}$ represented in Figure 60(c). Extending the analysis to the differential pair, the generated output noise current $i_{n,o}$ exhibits harmonics at $N^*(2\cdot f_{LO})$ with a baseband contribution represented by Equation 33.

Equation 33 – Flicker noise current due tail capacitance and v_n gate noise voltage

$$i_{n,o} = \frac{2}{T_{LO}} \int_0^{T_{LO}/2} i_{C_p}(t)dt = \frac{2}{T_{LO}} \int_0^{T_{LO}/2} C_p \frac{d\,V_s(t)}{dt} dt \Leftrightarrow i_{o,n}(f) = \frac{C_p \omega_{LO}}{\pi} \cdot V_n(f)$$

(4) Conclusion on flicker noise

As presented in this section, the flicker noise is generated by three different mechanisms due to the LO waveform and the parasitic capacitance in the RF signal path. For long channel CMOS devices, the indirect mechanism is negligible, but it becomes predominant for millimeter-Wave applications in advanced RF-CMOS.

Based on the previous analysis, a solution to reduce the generation of flicker noise is to reduce the width of noise pulse which requires to increase the LO slope and the power consumption of the LO generation circuit. Another solution is to design larger switches, this approach reduces the operating frequency of the mixer due to the increase of parasitics. The reduction of flicker noise at high frequency calls for circuit techniques.

b. Flicker noise reduction techniques

To overcome the issue of mixer noise at low IF, several techniques have been proposed in the literature to reduce the generation of flicker noise. This section proposes an overview of these techniques and discusses their interest in millimeter-Wave domain.

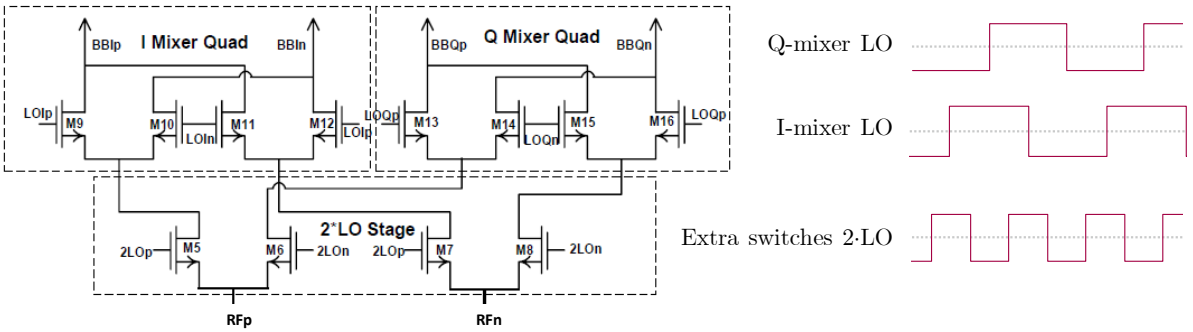


Figure 61 – Quadrature active mixer with a 2·f_{LO} extra-switches [36]

As the flicker noise is generated during switching event, using extra-switches driven at $2f_{LO}$ are used [36] to prevent DC current to flow in the mixing pair during switching event as shown in Figure 61. This technique significantly reduces the noise figure by 10dB at 10kHz as reported in [36] but suffers from complex LO generation at twice the LO frequency which is not realistic in millimeter-Wave.

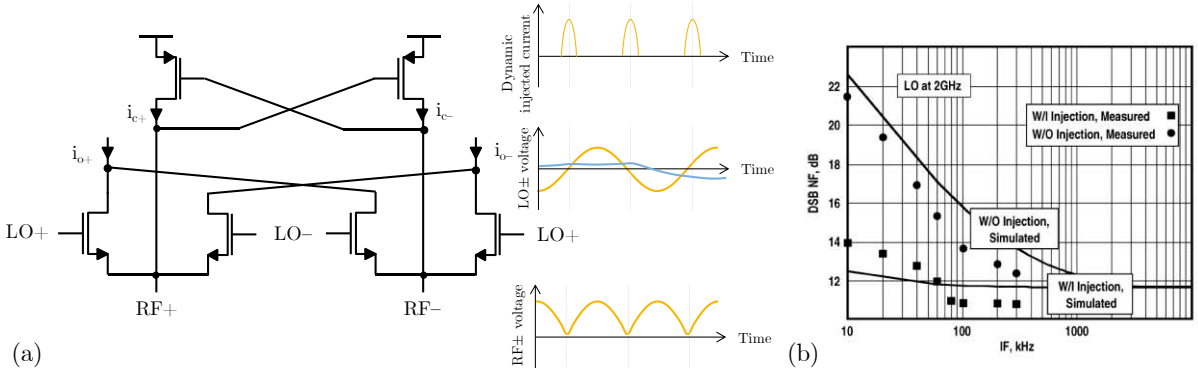


Figure 62 – (a) Dynamic current injection in active mixer with signals waveforms; (b) Measurement results of NF_{DSB} (dB) regarding intermediate frequency (Hz) at 2GHz with and without noise reduction technique [37]

One popular technique, featured in [37] (Figure 62(a)), proposes a dynamic current injection with a PMOS cross coupled pair which injects current during switching event to avoid bias current to flow through switches during switching event. This technique is efficient to

suppress flicker noise leakage in mixer and allows a significant reduction of noise frequency corner as reported in Figure 62(b) but it is reported to reduce the conversion gain. Again, the cross coupled pair drives a dynamic injected current at twice the LO frequency which is not suitable for 77GHz applications.

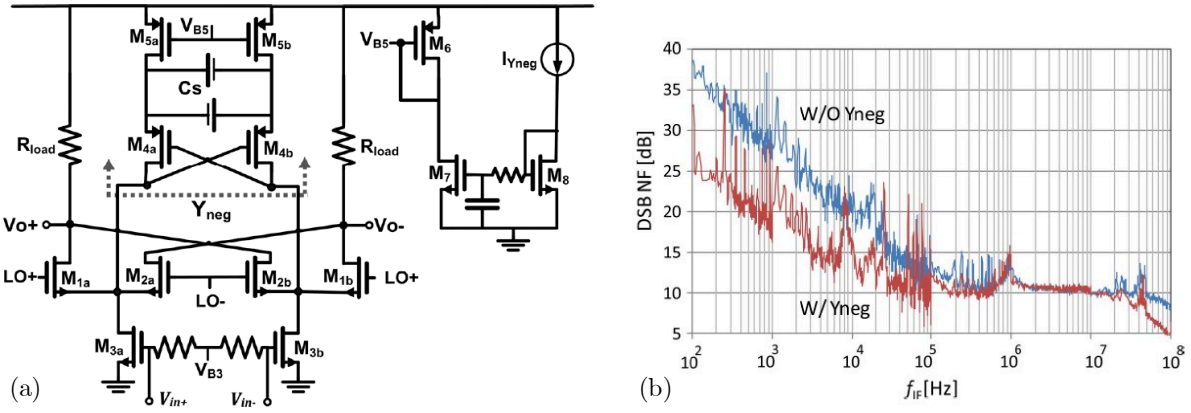


Figure 63 – (a) Schematic of an active mixer with a negative impedance; (b) Measurement results of NF_{DSB} (dB) regarding intermediate frequency (Hz) at 0.9GHz with and without noise reduction technique

A promising technique uses the generation of negative impedance at switches tail [38]. By properly sizing a cross coupled pair with a capacitive source degeneration, it's possible to significantly reduce the flicker noise leakage, Figure 63(b), as well as the third order intermodulation as shown. Nevertheless, this technique is very sensitive to parasitics extraction and has not been proved at higher frequencies than a few gigahertz.

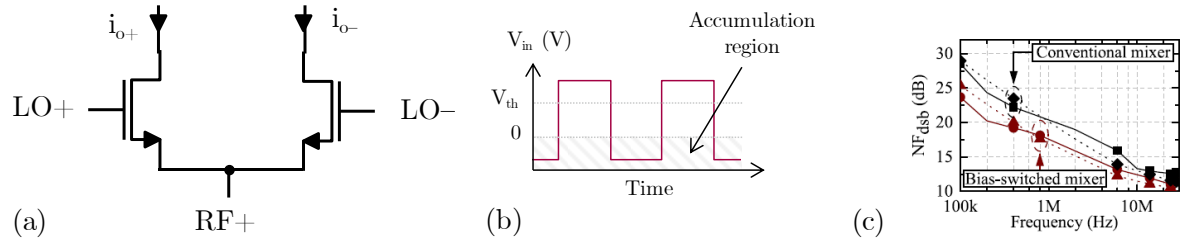


Figure 64 – (a) Switching pair with (b) LO square waveform with OFF state in accumulation generation; (c) Measurement result of NF_{dsb} (dB) regarding Intermediate Frequency (Hz) at 60GHz with and without noise reduction technique

As shown in Figure 64, the direct and part of the indirect flicker noise due to LO sine-wave form can be reduced by driving the switching transistor with a square-wave LO signal. This approach is investigated in [39]. The author also proposes to bias the switches between strong inversion and accumulation region to reduce v_n. This technique, implemented at 60GHz in [40], reduces the NF at 1MHz by 5dB with an extra 10mW in the power consumption.

c. Proposed flicker noise reduction

The most efficient techniques dedicated to reduce the flicker noise cannot be exploited in millimeter-Wave domain due to a frequency limitation. Besides, the solutions should present enough robustness regarding parasitics and PVT variations due to the targeted application. To address this purpose, we propose to combine two approaches, implemented here for the first time in mm-Wave domain: a *current bleeding biasing* and a *resonating tank*. These techniques, proposed in [41] for the RF domain, decrease the flicker noise generated by both direct and indirect mechanism.

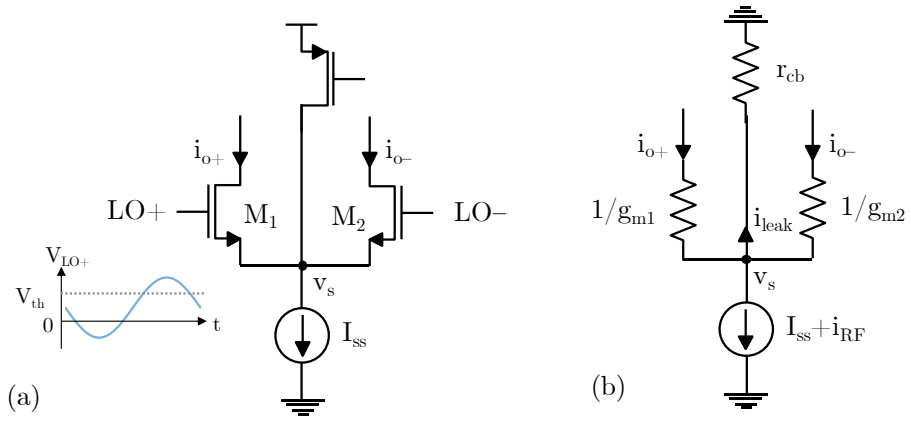


Figure 65 – Switching pair with a current bleeding in (a) schematic; (b) model

The contribution of the direct mechanism can be reduced if the DC component of the current flowing in the switching transistors is reduced, represented by I_{max} in Equation 29. In current bleeding approach, a current source is stacked on top of the G_m stage branch, PMOS transistor Figure 65(a), to make independent the tuning of the bias current of LO and RF stages. The main drawback of this technique is the introduction of a resistor at the switch tail modeled by r_{cb} in Figure 65(b). According Equation 34 the resistor r_{cb} derives a part of i_{RF} which is no longer commutated by the LO stage, hence the conversion gain of the mixer is reduced.

Equation 34 – Current in LO switches

$$i_{LO}(t) = \frac{r_{cb}\,(g_{m1}(t) - g_{m2}(t))}{r_{cb}(g_{m1}(t) + g_{m2}(t)) + 1} \cdot i_{RF}(t)$$

As the bias gate voltage of the LO switching pair is controlled by the average DC voltage of $V_{LO\pm}$, the LO switching pair operates in accumulation region as shown Figure 65(a), in order to reduce the flicker noise voltage. The hypothesis, developed in [39], is the traps occupancy memory is erased in the accumulation region.

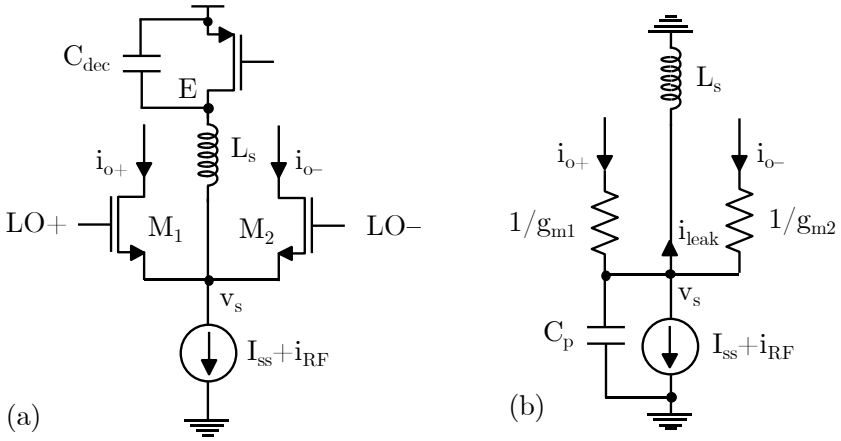


Figure 66 – Switching pair with current bleeding and resonating inductor in (a) schematic; (b) model

If a current bleeding helps to reduce flicker noise generated by direct mechanism, at the cost of gain reduction, the tail parasitic capacitance still generates 1/f noise. To compensate for it, a resonating inductor can be introduced at the tail, Figure 66(a). Considering that node E is AC grounded, it prevents RF leakage to the current bleeding. Furthermore, it reduces the impact of the indirect mechanism presented in sections III.1a(2) and III.1.a(3). The parasitic capacitors at the switch tail, modeled by a capacitor C_p, are resonated out by the inductor L_s at the operating frequency. Operating in millimeter-Wave range, the inductor value is low and the associated silicon footprint remains small.

Equation 35 – Input impedance of the switches pair

$$Z_{in,swi} = \frac{1}{g_{m1}} || \frac{1}{g_{m2}} || \frac{1}{j\omega C_p} || \left(j\omega L_s + r_{cb} || \frac{1}{j\omega C_{dec}}\right)$$

The input impedance of the switching pair is derived in Equation 35. As the architecture of the proposed mixer is not fully symmetrical, the AC ground is assured by a decoupling capacitor. The input impedance can then be reduced to the terms linked to the switch transconductances. At node C, the post layout simulations, Figure 67, show a cancellation of the imaginary part while the real part remains stable and close to a low value of 40Ω from 76 to 81GHz.

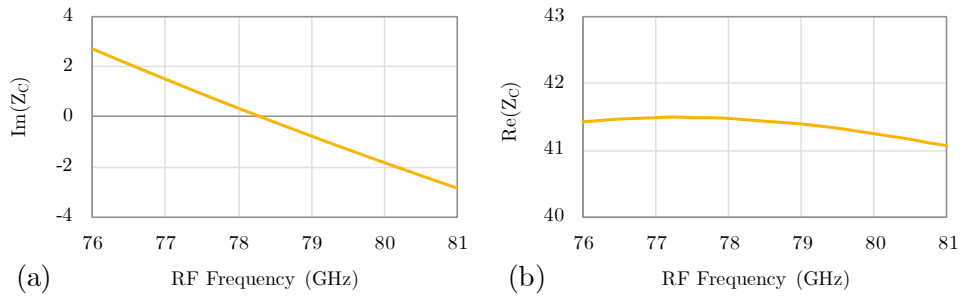


Figure 67 – (a) Imaginary part and (b) real part of tail impedance over the 76 to 81GHz band

As illustrated in Figure 68, the combination of the two proposed techniques improves the NF by a factor of 2 (-3dB) in the flicker noise region which decreases from 22dB to 19dB at 1MHz. The corner frequency is also reduced by a factor 2 from almost 9MHz to 4MHz. In section II, a downconverter is designed using this topology of switching cell implementing the proposed flicker noise reduction techniques.

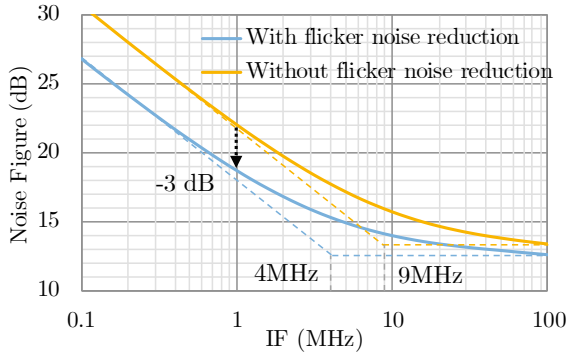


Figure 68 – Noise figure regarding the intermediate frequency for the mixer with and without the flicker noise reduction techniques (post-layout simulation)

2. mmW noise cancelling mixer model

The previous sub-sections focused on a critical characteristic of active mixers with respect to the application: the flicker noise. The present one investigates the AC modeling of the proposed noise canceling mixer in order to complete the analytic derivations of: the conversion gain, the input impedance and the noise figure. A simplified schematic of the mixer is shown in Figure 69(a). The transconductance (G_m) stage is based on an asymmetric active balun combining a common gate (CG) branch (M_1) and a common source (CS) branch (M_2). This configuration allows for both a cancelation of the drain thermal noise of the CG path at the IF output, and a wideband operation. The circuit also implements the flicker noise reduction technique presented in section II.

a. Impedance matching

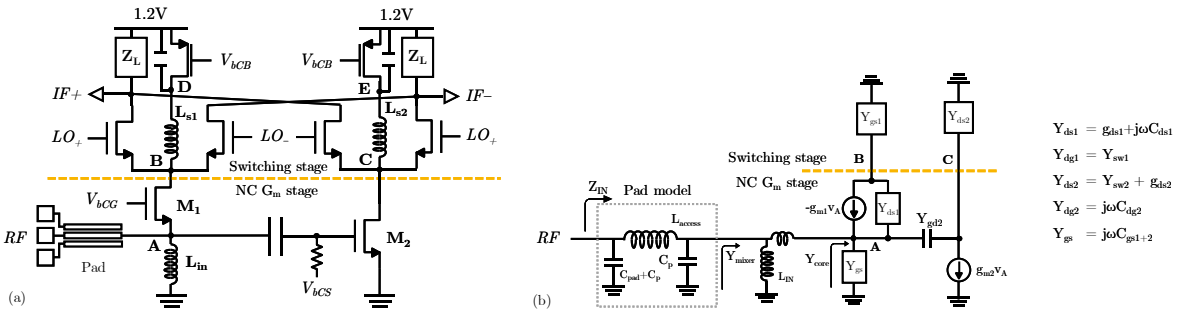


Figure 69 – (a). The schematic of the proposed downconverter (b). A model of the noise cancelling transconductance stage and the access to the mixer

A small signal equivalent model of the transconductance stage is presented in Figure 69(b). The transconductance core is composed of an auxiliary path with a CS transistor (M_2) and a main path with a CG transistor (M_1). The core input admittance Y_{core} is derived in Equation 36.

Equation 36 – Admittance of mixer core without access and input inductor

$$Y_{core} = Y_{CG} + Y_{CS} = j\omega(C_{gs1} + C_{gs2}) + \frac{1 + g_{m1}Z_{ds1}}{Z_{ds1} + Z_B} + \frac{1 + g_{m2}Z_C}{Z_C + Z_{dg2}}$$

In section III.1.c, the impedance at node C (Z_C) is assumed real at the operating frequency and closed to 40Ω. As the drain-to-gate impedance is significantly higher (C_{gd2} = 2.7fF), the impedance of common source path is dominated by the gate-to-source capacitance (C_{gs2}). For common-gate path, the impedance at node B is also closed to 50Ω. Then the CG path input impedance is mainly controlled by g_{m1} and impacted by the gate-to-source capacitance (C_{gs1}). The core input admittance is then simplified to Equation 37.

Equation 37 – Simplified admittance of mixer core

$$Y_{core} = j\omega(C_{gs1} + C_{gs2}) + g_{m1}$$

Considering this core impedance, the inductor L_{IN} is sized for input matching accounting for the pad model. Figure 70 proposes a representation on Smith chart of the different impedances considered in Figure 69(b). To ensure an input return loss, S_{11} lower than -10dB, the input impedance Z_{in} must be located inside the dashed circle over the frequency band. The model of the circuit, presented on Equation 36, shown in Figure 69 leads to a similar input matching (green S_{11}).

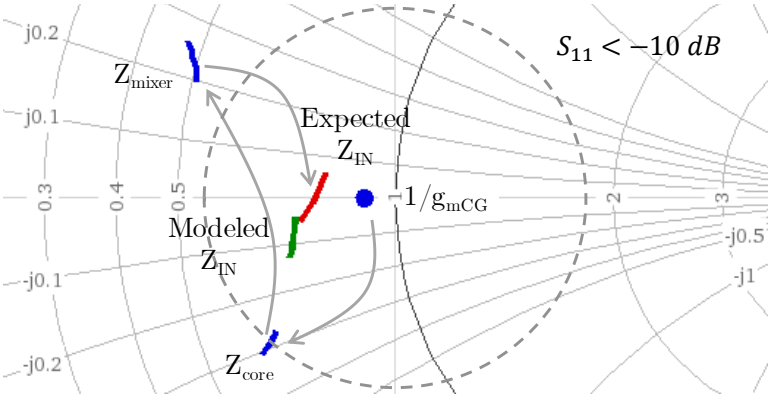


Figure 70 – Smith chart of the input impedance from core impedance to measured impedance on pad on 76 to 81GHz band

b. Conversion gain

As discussed in the introduction, the noise contribution of the baseband signal processing depends on the gain of the RFFE. As no LNA is used before the mixer, the conversion gain of the proposed downconverter is critical for the radar performance. Besides, due to the mixer asymmetry, the imbalance between the common-gate and the common source path should be considered. The equivalent transconductance from the mixer input to the switching stage for each path is expressed in Equation 38 for the CG and CS path. Due to the noise cancelling configuration, the transconductance of each path is slightly different.

Equation 38 – Expression of transconductances on each path

$$G_{mCG} = \frac{g_{m1} + Y_{ds1}}{1 + Y_{ds1}/Y_{dg1}} \approx \frac{g_{m1} + g_{ds1}}{1 + \frac{g_{ds1}}{Y_{swi1}}};\ G_{mCS} = \frac{\left(1 - g_{m2}\, Z_{dg2}\right) \cdot \left(Y_{swi2} + Y_{ds2}\right)}{1 + Z_{dg2} \cdot \left(Y_{swi2} + Y_{ds2}\right)}$$

To study the impact of this imbalance on the downconverter functionality, an analysis of the common-mode is performed. Post layout simulations shows that this imbalance does not affect the mixer performance as the common mode signal is fifty times lower than the differential IF signal.

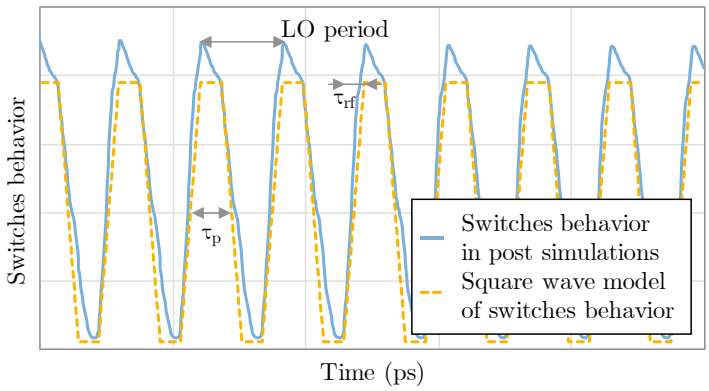


Figure 71 – Time domain behavior of mixing switches in post layout simulation (solid line) and square wave model (dashed line)

As exposed in section III.1.a, the finite slope of LO waveform generates indirect flicker noise during switching events, it also degrades the mixing operation as illustrated in Fig. 71 (solid curve). To account for the non-instantaneous switching operation, a square wave model featuring a finite slope is used, Fig. 9 (dashed curve). In the conversion gain expression, derived in (39), the square wave model is represented by the term within the brackets. More specifically the sinus cardinal accounts for trapezoid waveform through τ_p and τ_{rf} which respectively stand for the pulse width and for the rise and fall times. The inherent single-to-differential conversion performed by the transductor stage architecture leads to consider the equivalent transconductance of each path, G_{mCG} and G_{mCS}, in the mixer conversion gain.

Equation 39 – Expression of overall gain

$$G_v = (G_{mCG} + G_{mCS}) \cdot R_L \cdot \{\frac{2\pi\,\tau_p}{T_{LO}} sinc\left(\frac{\pi\,\tau_p}{T_{LO}}\right) \cdot sinc\left(\frac{\pi\,\tau_{rf}}{T_{LO}}\right)\}$$

c. Noise

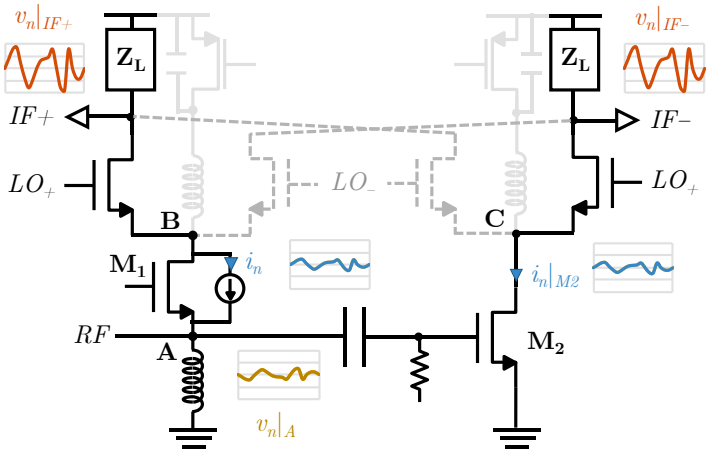


Figure 72 – Noise cancelling principle in mixers during a LO cycle

The noise cancelling topology is based on two parallel stages: a *common-gate path* which ensures a wideband input matching as described in section III.A. and a *common source path* which features the inherent balun behavior. This configuration of the transconductance stage also performs the cancelation of the thermal noise of the common gate transistor under input matching and output signal balance conditions

The Fig. 10. proposes an illustration of the noise cancelling principle during an LO_+ phase. The common gate transistor (M_1) generates a thermal channel noise current (i_n) which induces a noise voltage at the mixer input (node A). This noise is then converted into an in-phase current in the auxiliary path by the common source transistor. The spectral power density of noise for each path is expressed in (10) and (11).

Equation 40 – Noise current of common gate transistor in both path

$$\frac{\overline{\iota_{n|CG}{}^2}}{\Delta f} = 4kT\gamma \cdot g_{m1}; \frac{\overline{\iota_{n|CS}{}^2}}{\Delta f} = 4kT\gamma \cdot g_{m1} \cdot (R_S^2 \cdot g_{m2})^2$$

Under the conditions of input matching and signal balance, the thermal noise currents (10) and (11) are equal and in phase. As the switching and load stages are symmetrical, the transfer function is similar for each path and the downconversion operation does not affect the processing of noise cancellation. Depending on LO± phase, the current is only alternatively downconverted to IF±.

In practice, the thermal noise of M_1 cannot be fully canceled [22] in the millimeter-wave domain due to the phase imbalance induced by the different parasitics attached to each path. The Table 11 proposes an overall summary of the mixer noise sources at an IF of 10MHz. Post-layout simulations show a thermal noise contribution of the common-gate transistor which is 2.5 times lower than the common source.

Table 11 – Noise summary of the proposed noise cancelling mixer at high intermediate frequency

Noise source	Noise type	Value (V^2/Hz)	%
Switches	Thermal	$16.4 \cdot 10^{-18}$	16.4
	Resistive	$4.9 \cdot 10^{-18}$	5
Common Source transistor	Thermal	$13.2 \cdot 10^{-18}$	12.4
	Resistive	$5.6 \cdot 10^{-18}$	5.7
Common-gate transistor	Thermal	$5.1 \cdot 10^{-18}$	5.2
	Resistive	$1.4 \cdot 10^{-18}$	1.4
Load	Resistive	$13.2 \cdot 10^{-18}$	13.4
RF Port	Resistive	$10.4 \cdot 10^{-18}$	10.6

3. Measurement and simulations

This section studies the performance of the proposed mixer for automotive applications accounting for the input matching, the conversion gain, the linearity and the noise figure. Measurements have been done in typical case but discussions regarding PVT variations are proposed based on post-layout simulations before and after a calibration procedure.

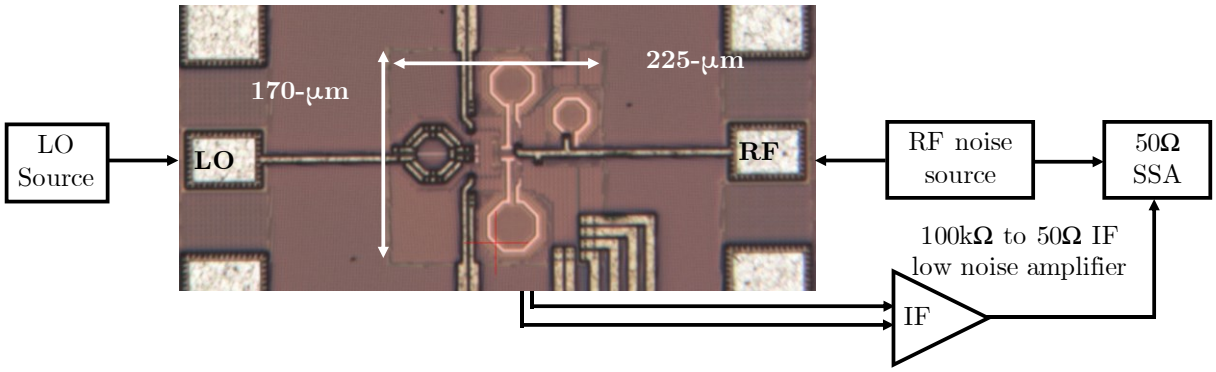


Figure 73 – Chip micrograph with measurement setup by Y method

The Figure 73 shows the chip micrograph of the proposed mixer implemented in 28nm CMOS bulk technology. The silicon footprint including the local oscillator balun is only $0.04mm^2$. During this study, the nominal supply voltage is 1.5V and the LO power is fixed to +3dBm. The overall power consumption is measured at 16mW in typical case. For measurement, as the following stage is supposed to be a VGA with a high input impedance, an

off-chip IF buffer is used for measurement purpose as shown in Figure 73. It presents a high impedance at the mixer output and can drive a 50Ω output impedance. The buffer contribution is de-embedded from the presented measurement results.

To improve block performances, a calibration is emulated on downconverter. Its purpose is to measure the downconverter noise figure and, during specific times, to modify the bias currents of mixer to reduce the noise figure. For each figure of merit, the impact of this noise calibration is evaluated.

Post-layout simulations show a minor impact of supply voltage variation on the radar performances, less than 5% of variation compared to nominal conditions. For a sake of clarity, its impact is not reported on the presented figures.

(1) Input matching

The mixer exhibits a wideband input matching in post layout simulations, Figure 74(a), from 68 to 83GHz corresponding to a 20% bandwidth of the central frequency. The variation on return loss and central frequency, is mainly due to process variations which impact the common gate transconductance through the threshold voltage and the process parameters. This mixer achieves a sufficient matching on the radar band (76-81GHz). The calibration doesn't significantly impact the matching of the proposed mixer (Figure 74(b)). The measured S_{11} (Figure 74(c)) is higher than expected due to an underestimation of input pad parasitics. Some re-simulations have been down and show a similar behavior.

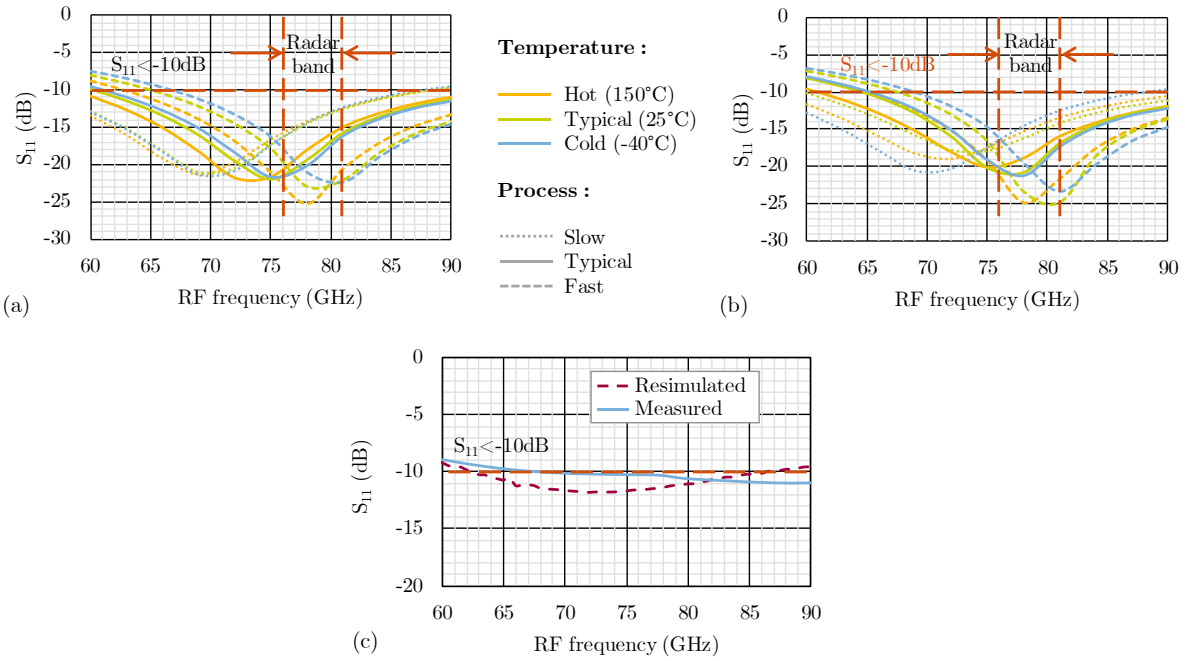


Figure 74 – (a) PVT post-layout simulations of return loss; (b) PVT post layout simulations of return loss after calibration; (c) Measurement result and re-simulated result of return loss

(2) Conversion gain

In Figure 75(a), the conversion gain is proposed in PVT post-layout simulations. The nominal conversion gain presents an average value of 14.6dB with a variation of ±2dB over the 60-90GHz band. Thanks to a common-gate based topology, a wide -3dB bandwidth is achieved from 72-90GHz. In the 76-81GHz radar band, a nominal gain of 13.8dB is achieved with a ±2dB variation on PVT and a reduced ripple of ±0.5dB over the selected band. Temperature is the main contributor to the PVT variation. The noise calibration significantly impacts the conversion gain regarding PVT of ±3.5dB, Figure 75(b). It leads to a minimum gain reduced to 9.3dB which is below the target. In Figure 75(c), the average conversion gain is measured in typical case at 12.5dB with a gain ripple of 0.6dB from 76 to 81GHz band. These values are closed to the re-simulated results.

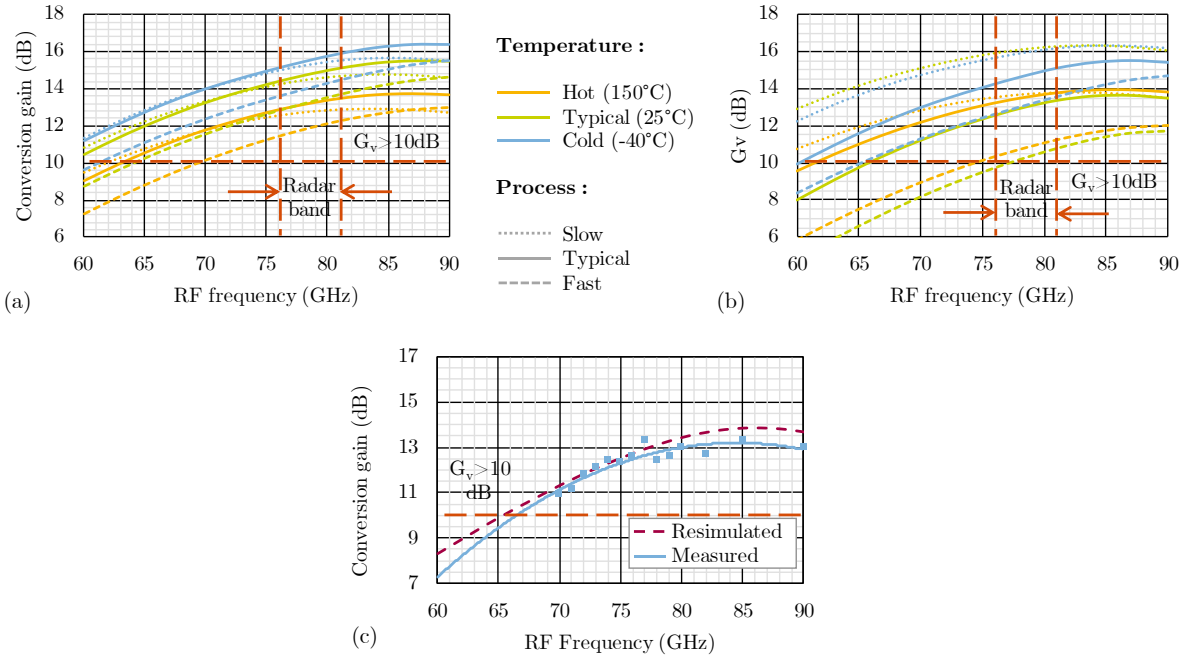


Figure 75 – (a) PVT post-layout simulation of conversion gain; (b) PVT post layout simulations of conversion gain after calibration; (c) Measurement result and re-simulated result of conversion gain

(3) Input compression point

The -1dB input referred compression point, Figure 76(a), exceeds -5dBm over the entire 60-90GHz band. After calibration, Figure 76(b), the 1dB compression point presents an important variation on the specified band down to -7dBm. This value may be compatible with radar applications. Measurements in typical case, Figure 76(c), show similar results with a -4dBm compression point. This value is almost +1dB higher than the specification which makes it suitable to handle jammers due to bumper reflections and Tx-to-Rx limited isolation.

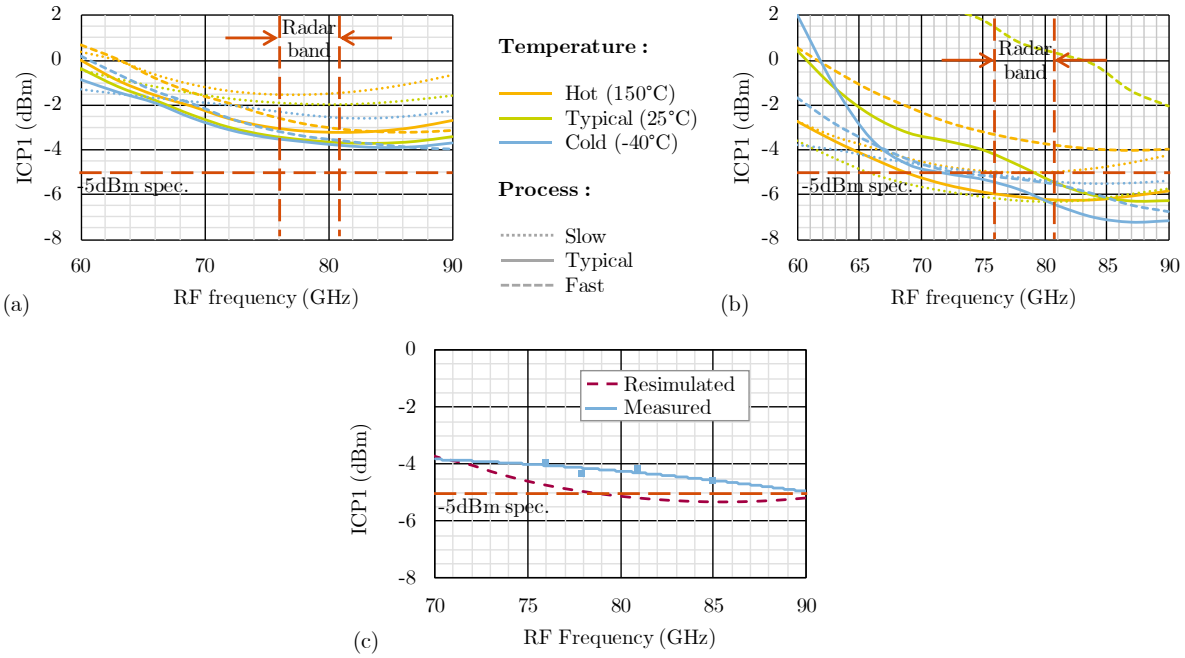


Figure 76 – (a) PVT post-layout simulation of ICP1; (b) PVT post layout simulations of ICP1 after calibration; (c) Measurement result and re-simulated result of ICP1

(4) Noise figure

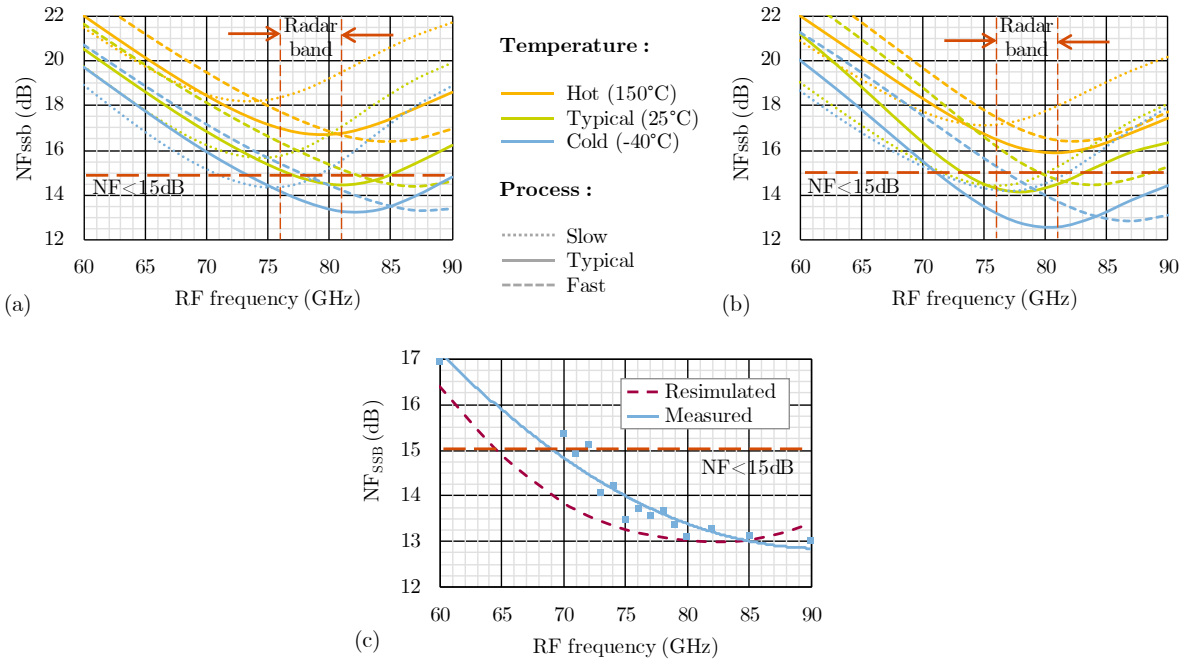


Figure 77 – (a) PVT post-layout simulation of NF_{SSB} at 10MHz IF; (b) PVT post layout simulations of NF_{SSB} at 10MHz IF after calibration; (c) Measurement result and re-simulated result of NF_{SSB} at 10MHz IF

For noise characterization, two aspects are considered: the NF variation over the RF band at a fixed IF frequency, Figure 77, and the NF variation over the IF band at a fixed RF

frequency, Figure 78. For noise measurement at a fixed 10MHz IF, post layout simulations show an important variation of NF regarding temperature. The minimal noise figure frequency also varies regarding the process corners. It leads to a maximal noise figure of 19.5dB which is very high regarding the specification. The calibration leads to significantly reduce the spread of minimal noise figure regarding corners. It allows to reduce maximal NF by 1.5dB on the radar band. On typical measurements, the NF remains below 14dB limit over the entire radar band. Re-simulated post layout simulations show similar values with a small frequency shift.

As discussed in previous sections, active mixer presents an important flicker noise at low intermediate frequencies. In post layout simulations, noise corner significantly changes with temperature and process corners. Calibration permits a reduction of maximal noise but do not affect flicker noise generation. In measurement, the noise figure increases to 20dB as the IF is reduced to 1MHz. This low IF range corresponds to the flicker noise region, upper bounded by the corner frequency measured at 4MHz.

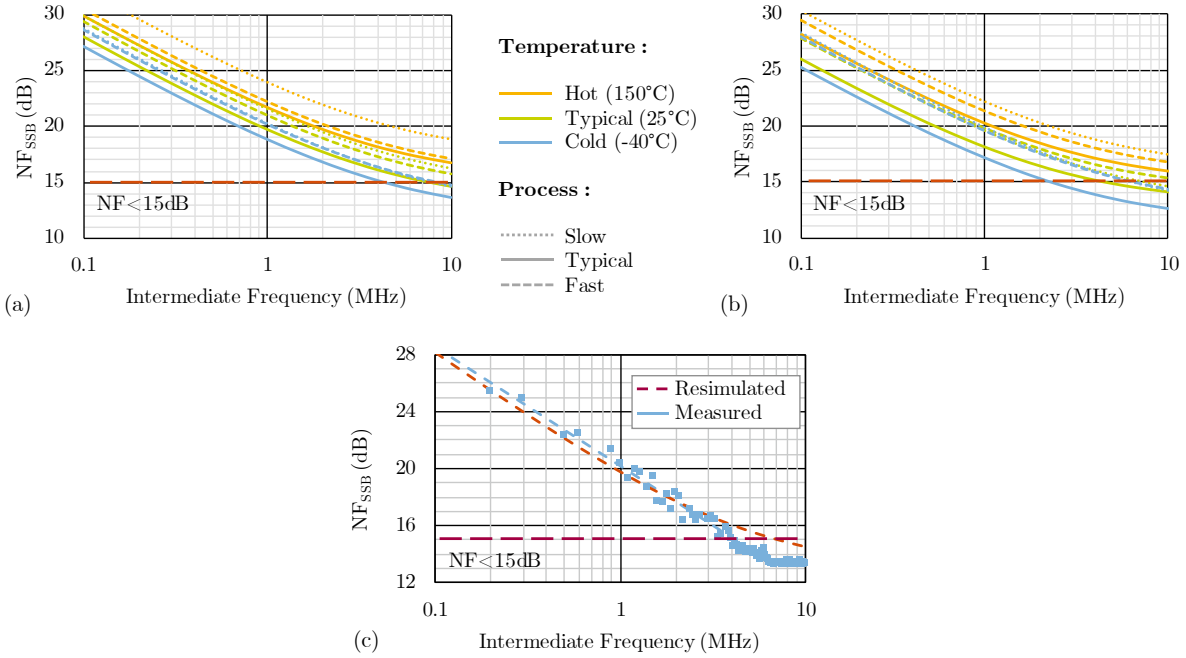


Figure 78 – (a) PVT post-layout simulation of NF_{SSB} (dB) versus IF at f_{RF} = 78.5GHz; (b) PVT post layout simulations of NF_{SSB} (dB) versus IF at f_{RF} = 78.5GHz; (c) Measurement result and re-simulated result of NF_{SSB} (dB) versus IF at f_{RF} = 78.5GHz

4. Conclusion on 77GHz mixer

As introduced in Chapter 1.1.3, many applications are proposed for automotive radar from short range up to long range detection. This section proposes a comparison to the start of the art of millimeter-Wave receivers and draws a conclusion regarding the performance of the proposed downconverter for the different automotive radar applications.

Equation 41 – Figures of merit for downconverters

$$FOMI = \frac{G_c\,(lin)\cdot P_{1dB}(mW)}{P(mW)\cdot (F(lin)-1)} \quad ; \quad FOMII = \frac{G_c\,(lin)\cdot P_{1dB}(mW)}{P(mW)\cdot (F(lin)-1)\cdot Area(mm^2)}$$

The Table 12 reports the performance of some millimeter-wave mixers of the state of the art with their FOM defined in (41). The two receivers presented in [42] and [43] exhibit a good RF performances but a large power consumption due to the bipolar technology for the first one and the architecture, with a LNA and a passive mixer, for the second one. The two active CMOS mixers in [44] and [45] presents an interesting trade-off between the overall performance and the power consumption. However, the NF is only evaluated in the thermal noise region at high IF, which is not relevant for the targeted application. The paper [46] proposes a 77GHz active mixer with some measurement at an IF of 1MHz but suffers from a high NF and a poor gain. The circuit proposed in [40] demonstrates a flicker noise reduction technique based on LO signal waveform shaping. It achieves a good noise performance at 60GHz but presents a low conversion gain with respect to the power consumption. The proposed mixer achieves a good performance trade-off compared to the state of the art. Besides it exhibits the smallest silicon area.

Table 12 – State of the art of millimeter-wave mixers (: Including pads; **: Including pads and baseband) for typical measurements*

Parameters	[42]	[43]	[44]	[45]	[46]	[40]	This work
Conditions	25	25	25	25	25	25	25
Results	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.
Mixer architecture	Active	LNA + Passive	Active	Active	Active	Active	Active
Tech (nm)	SiGe Bip.	CMOS 40	CMOS 65	CMOS 65	CMOS 65	CMOS 28	CMOS 28
VDD (V)	3.3	1.1 / 1.8	1.2	1	1.2	0.9	1.6
Frequency (GHz)	77	77	60	77	77	60	77
Bandwidth (GHz)	25	/	9	28	/	25	30
Conv. gain (dB)	21.5	30.8	14	9.5	6.8	2	12.5
NF(dB) @1MHz	10.8	9	/	/	21	18	20
NF(dB) @10MHz			12	9.2	/	10.6	13
ICP_1 (dBm)	-5	-22.3	-10	-3.8	-7	-4	-2.5
Power (mW)	70	142**	13.2	15	3	11.7	16
Area (mm^2)	0.53*	0.8**	0.68	0.27	0.47*	0.23	0.04
FOMI	0.005	0.0007	0.003	0.011	0.001	0.004	0.008
FOMII	0.009	0.0008	0.004	0.042	0.003	0.018	0.02

Regarding the Table 9 of front-end specifications, the present active downconverter is not suitable for long range applications. The Figure 77 shows that the noise figure remains roughly stable regarding the RF frequency for a high IF which is compatible with short range application. Nevertheless, it is sensitive to the intermediate frequency which is correlated to the target distance. As reported in Figure 15, low part of the IF spectrum corresponds to the

closed targets. For those ones, the noise specification is relaxed since the input signal-to-noise ratio (SNR) is large. The Figure 79 proposes an evaluation of the achievable distance for a short-range radar module considering the analysis proposed in Chapter I.3.1. The grey line corresponds to the maximum measurable distance for various type of target. For large size targets, such as cars, it is possible to detect them up to 80-meters. For smaller targets, such as bikes and pedestrians, the RFFE limits the achievable range to respectively 40 meters and 15 meters. Hence the proposed downconverter can be exploited for a short-range use case.

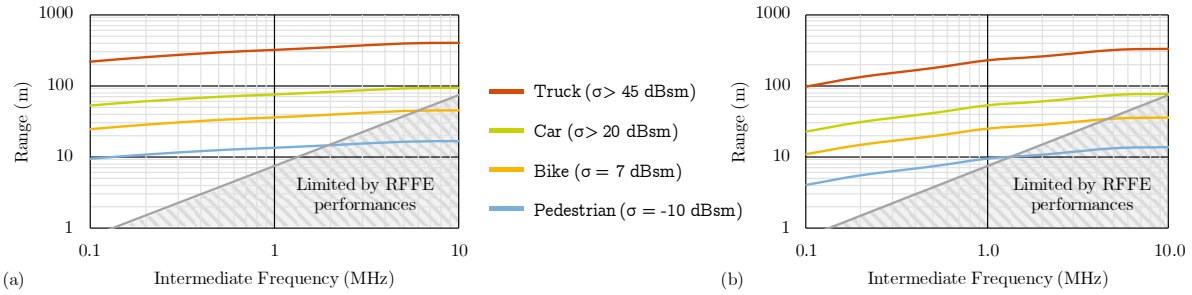


Figure 79 – Maximum achievable range (m) for various targets versus the intermediate frequency IF (MHz) at RF frequency of 78.5GHz for (a) measurement results; (b) worst case in post-layout simulations

In this section, a 28-nm RF CMOS active mixer suitable for short-range radar applications is proposed. The architecture is based on a common gate noise cancelling transconductance stage which achieves a wideband input matching (65 to 85 GHz). To improve the noise performance at low IF, in the flicker noise region, two techniques are implemented: current bleeding and resonating inductor. The measured NF is 20dB at 1MHz and 13dB at 10MHz. The conversion gain is 12.5dB with less than 0.6dB ripple in the targeted 76-81GHz band. To handle jammers generated by bumper reflections, the linearity of the RX RFFE is important, and the circuit achieves an ICP1 of -2.5dBm. This circuit presents a reduced silicon area (0.04mm^2) and a moderate power consumption (16mW).

IV. Conclusion on noise cancelling mixer

Regarding the RX-RFFE specifications developed in Table 9, this chapter proposes the development of a 77GHz radar downconverter. Considering the requirement of high linearity and gain, an active real mixing is preferred. The topology is based on a noise canceling architecture which achieves a large voltage gain with balun operation and a good linearity, in terms of compression and intermodulation. The wideband behavior of a noise canceling configuration contributes to improve the circuit robustness to PVT variations.

In order to validate the concept of noise canceling in frequency conversion, as well as various circuit techniques dedicated to improve the performances, a first demonstrator

dedicated to IOT applications, namely RF blixer is developed and implemented in 28nm CMOS. The circuit exhibits competitive performance, reported in Table 13, regarding the state of the art.

The RF mixer allows to demonstrate at circuit level: the concept of noise cancelation in mixer implementation, the reduction of the NF through path imbalance (beta factor), the improvement of the current efficiency in a transconductance stage with a current reuse configuration; and at device level: the biasing of MOS transistor in moderate inversion region to improve the figure of merit $g_m.f_T/I_D$ which represents the current efficiency accounting for frequency performance

Table 13 – Measurement results of noise cancelling mixer for RF and millimeter-Wave applications

Parameters	RF Mixer	mmW Mixer
Frequency (GHz)	0.4-6	76-81
Conversion gain (dB)	15	12.5
NF (dB) at 1MHz	6.2	20
NF (dB) at 10MHz		13
Linearity (dBm)	-1 (IIP_3)	-2.5 (ICP_1)
Power (mW)	4	16
Area (mm^2)	0.04	0.04

Some of the techniques experimented in the design of the RF mixer are then exported, when it is possible, in the implementation of the mm-Waves mixer. Notably the architecture exploits the same noise canceling configuration based on a common gate path and a common source path. Complementary approaches, specific to the application, are developed to reduce the flicker noise. After a comprehensive analysis of flicker noise generation in frequency down conversion process, two techniques are proposed to reduce the noise figure at low IF :

- *at circuit level* - the configuration of current bleeding to reduce the DC component in the LO switching stage and a parallel inductor to cancel parasitic capacitances
- *at device level* - the biasing of LO transistors in sub-threshold region to reduce the noise voltage at the gate

The proposed downconverter, implemented in 28nm CMOS technology, achieves a wideband matching, a high gain for a moderate noise figure as reported in Table 13. Likewise the RF mixer, the mm-Waves mixer compares favorably with the state-of-art. It achieves among the best trade-off between performances accounting for the power consumption, and the silicon footprint.

The analysis of radar RFFE performance featuring such active mixer figures out this solution can address short range radar applications. However, for a long-range radar module, it seems difficult for an active downconverter to achieve enough low noise figure to target the most distant targets.

Chapter 3. 77-GHz low noise amplifier

In Chapter I, stringent specifications are determined for RX-RFFE, especially regarding noise and linearity. Chapter II demonstrates the limitations of active downconverters to address long-range radar requirements, especially at low intermediate frequency (IF). To improve the performance at low IF we further investigate the development of an RX-RFFE combining a Low Noise Amplifier (LNA) and a passive mixer. This chapter focuses on the design of low noise amplifiers in advanced RF-CMOS featuring common-gate based noise-cancelling.

The first section proposes to define the LNA specifications considering the different elements featuring the RX-RFFE. A single-to-differential noise-cancelling amplifier is proposed and simulated in section II. A new architecture called "complementary capacitor-cross-coupled amplifier" is introduced in section III. This LNA improves the overall current efficiency and the noise performance compared to conventional topologies. Finally, the section IV draws the conclusion about the proposed LNAs regarding the state-of-art.

I. Introduction to conventional RF architecture

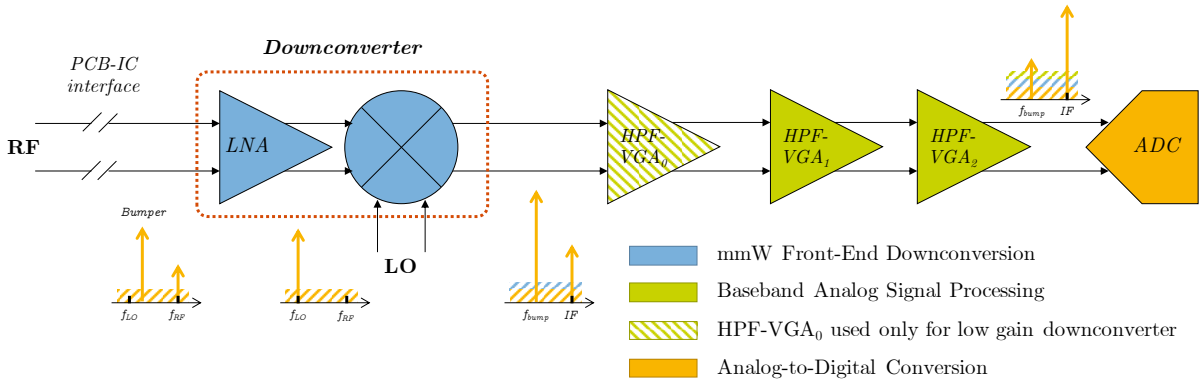


Figure 80 – Radar RX-RFFE typical architecture

Conventional RF-CMOS receivers do not usually exploit active mixer architectures due to their large flicker noise contribution. They rather feature a Low Noise Amplifier (*LNA*), a passive mixer and a baseband demodulation chain. For radar applications, the baseband analog often uses two variable gain amplifiers and high pass filters (VGA-$HPF_{1/2}$) as illustrated in Figure 80. Due to the low gain of the millimeter-Wave front-end, a low noise VGA-HPF (VGA-HPF_0) can be added following the mixer. The characteristics of the building blocks are reported in Table 14. Some additional 2dB losses accounting for PCB to IC interfaces are further considered. This section derives the LNA specifications in terms of voltage gain, noise figure and linearity.

Table 14 – Overview of the main FoM of the considered blocks in the demodulation chain

Parameters		Mixer	VGA_0 (low noise) & HPF_0	VGA_1 & HPF_1	VGA_2 & HPF_2
Gain (dB)		-4	10	22	10
NF (dB)		8	/	/	/
Noise (nV/√Hz)		/	3	10	50
Linearity	@20kHz	+5 dBm	0.57 V_{RMS}	0.57 V_{RMS}	/
	@10MHz		0.14 V_{RMS}	0.45 V_{RMS}	/

1. LNA specification: Noise Figure

The main purpose of a LNA is to increase the level of the desired RF signal with a minimum degradation on its Signal-to-Noise Ratio. Considering the noise distribution on the demodulation chain expressed by Friis formula (Equation 42), the RF characteristics of the LNA are predominant for the overall noise performance. A large gain (G_{LNA}) is supposed to hide the noise contribution of the following stage, and a reduced noise figure (F_{LNA}) should lower the overall RX-RFFE noise figure.

Equation 42 – Friis formula on noise

$$F_{RX} = F_{LNA} + \frac{F_{mixer} - 1}{G_{LNA}} + \frac{e_{VGA0}^2}{4kT \cdot R_S \cdot G_{LNA} \cdot G_{mixer}} + \frac{e_{VGA1}^2}{4kT \cdot R_S \cdot \prod_{LNA}^{VGA0} G} + \frac{e_{VGA2}^2}{4kT \cdot R_S \cdot \prod_{LNA}^{VGA1} G}$$

Considering the noise contributions and the gain of each stage, Figure 81 proposes an application of the Friis formula for the calculation of the demodulation chain NF depending on the LNA RF specifications. To achieve long range requirements, the noise figure of the overall RX-RFFE should not exceed 15dB. To address this constraint, and considering the characteristics reported in Table 14 for the RX-RFFE, the LNA would achieves more than 10dB of gain, and a NF below 7dB.

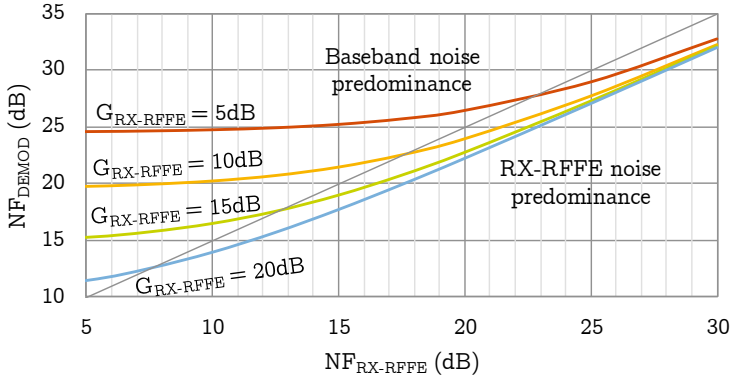


Figure 81 – Noise figure of the overall chain regarding the noise figure and the gain of the LNA

2. LNA specification: Linearity

The previous section highlights any increase of the LNA gain reduces the noise contribution of the following stage. Unfortunately, a high gain LNA can compromise the linearity of the system. This issue is illustrated in Equation 43. To reduce the degradation of the receiver linearity (*ICP1*) due to cascaded stages, the linearity of the second stage $ICP1_{mixer}$ must be G_{LNA} time larger than $ICP1_{LNA}$, the $ICP1_{baseband}$ should be ($G_{LNA} \cdot G_{mixer}$) time larger than $ICP1_{LNA}$ and so on. As consequences, any increase in G_{LNA} implies the same improvement of CP1, and IP3 since the analysis holds for inter-modulations, in the following stages. Hence this trend can lead to very high values of linearity specifications for the base-band section.

Equation 43 – Cascaded IIP3 formula

$$\frac{1}{ICP1_{RX}} = \frac{1}{ICP1_{LNA}} + \frac{G_{LNA}}{ICP1_{mixer}} + \frac{G_{LNA}G_{mixer}}{ICP1_{BBLNA}} + \cdots + \frac{G_1 \ldots G_{n-1}}{ICP1_n}$$

To keep the input 1dB compression point of a radar receiver at -5dBm, the gain of the LNA should not be too large. In the Chapter I, the ICP1 of the RX-RFFE is specified to -5dBm due to bumper reflections. Considering an optimistic compression point of +5dBm for a passive mixer, the gain of the LNA should not exceed 10dB to address the system specification in terms of signal compression.

3. Conclusion on LNA Specifications

Hence the design of the LNA is led by a tradeoff between the linearity and the NF performance. To achieve a high ICP1 at system level, the gain of the *LNA* should be reduced, according Equation 43, which degrades the overall noise figure according Equation 42. Table 15 sums up the LNA specifications in terms of noise figure, linearity and gain accounting for the RX-RFFE characteristics reported in Table 9 to address long range radar (LRR) applications.

Table 15 – Targeted performances for suitable LNA for radar applications

Objectives	Min.	Typ.	Max.
Noise figure (dB) for LRR			7
ICP1 (dBm) – *For bumper management*	-5		
IIP3 (dBm) – *For signal intermodulation*		-26	
Voltage Gain (dB)		10	
Power consumption (mW)		10	

Table 16 presents an overview of the State of art of millimeter-Wave LNAs. These circuits usually feature several stages with conventional architectures such as common-source or common-gate topologies. Depending of the context, various trade-offs can be targeted. On one hand, some proposed LNAs [47] [48] optimize the NF of the first stage, then cascading a large gain stage limiting the overall linearity. One the other hand, some circuits [49] [50] achieve a high value of 1dB compression point by cascading 3 to 4 low gain stages thus degrading the NF performance. The nominal value of such NF, typically between 5.7 to 6.6 dB, does exhibit enough margin with our NF_{LNA} specification, 7dB, to withstand PVT variations of advanced CMOS nodes. The 3-stage LNA proposed in [51] achieves good RF performances regarding gain, noise and linearity but it requires a very high-power consumption due to the number of cascaded stages. The 1-stage implementation [51] achieves a low noise figure, a high linearity with a limited power consumption, but a too low gain to ensure a RX-RFFE NF of 15dB.

Table 16 – State of the art of 80GHz LNA for automotive radar applications (Power gain)*

Parameters	[47]	[48]	[49]	[50]	[51]	[51]
Conditions	25	25	25	25	25	25
Results	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.
Number of stages	2	2	3	4	3	1
Tech. (nm)	CMOS 28nm	CMOS 28nm	CMOS 45nm	CMOS 90nm	CMOS 65nm	CMOS 65nm
VDD (V)	0.9	2	1.4	1.2	1	1
Frequency (GHz)	80	60	95	80	80	80
Bandwidth (GHz)	12	15	23	23	14	14
Gain (dB)	16.5*	13.8*	10.7*	7.6*	7.2*	2.1*
NF (dB)	5.2	4	6	6.6	5.7	4.5
ICP1 (dBm)	-15.5	-12.5	-3.2	-7	-3.75	0
Power (mW)	26	24	52	11.3	70	22
Area (mm^2)	0.14	0.38	0.32	0.59	0.99	0.33

The various CMOS low noise amplifiers proposed in Table 16 do not address the specifications of a modern 77GHz radars presented in Table 9. Technically the cascade of several stages is not a solution as it is difficult to achieve simultaneously a low noise figure and a high 1dB compression point at a moderate power consumption. On the other hand, a single stage LNA based on a basic common source, or common gate, configuration does not achieve enough gain. New LNA architectures are required to address our purpose.

II. Single-balanced noise-cancelling LNA

In Chapter II, the common-gate based noise-cancelling topology for mixer is studied. It presents interesting performances regarding the bandwidth, the noise figure and the linearity. As discussed in Chapter 2.III, active mixers cannot perform low noise figure, especially at low

IF. Nevertheless, the noise-cancelling principle has been widely investigated for RF amplification [26]. This section proposes to exploit this technique for the implementation of a 77-GHz low noise amplifier.

In this section, the conditions to design a common-gate-based noise-cancelling amplifier are first reminded. Finally, the architecture is discussed throughout post-layout simulations.

1. Noise-cancelling LNA modelling

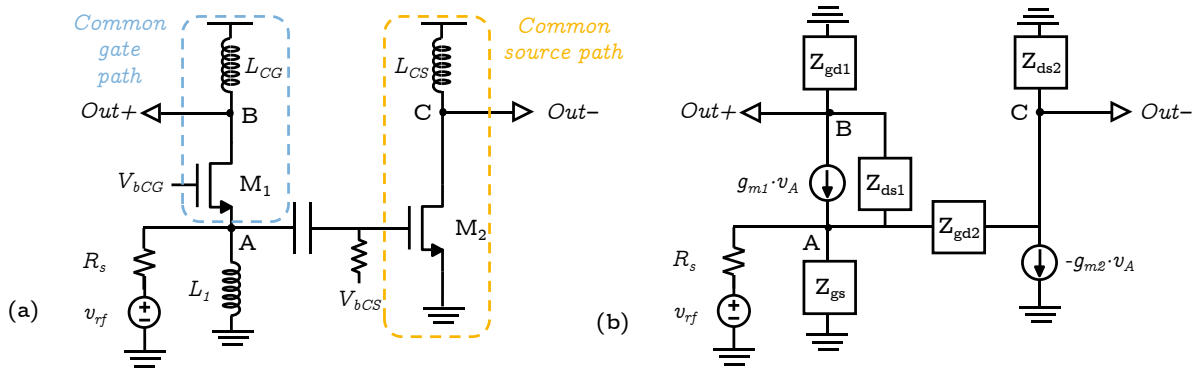


Figure 82 – Common-gate-based noise-cancelling amplifier in (a) schematic with m matching condition & (b) in schematic with gain imbalance condition

As discussed in section II.1.2, noise-cancelling architectures based on common-gate (CG), Figure 82(a), require some conditions to perform the cancellation of the noise of the main path CG stage [26]. The first condition to achieve noise cancellation is to match the CG stage to the source impedance Rs according Equation 44. As common-gate transconductance term is predominant in the input impedance, the matching band is wider than architectures based on a common-source (CS) configuration.

Equation 44 – Condition for impedance matching

$$g_{m,CG} = \frac{1}{R_s}$$

The second condition is to balance the gain in each path. Indeed, the architecture has an inherent asymmetry since the main path is a CG configuration and the auxiliary path is a CS configuration, Figure 82(a). To cancel the thermal noise of the main path, each path is expected to achieve the same gain, which leads to the condition edited in Equation 45.

Equation 45 – Condition on path gains

$$A_{v,CG} = A_{v,CS} \Leftrightarrow g_{m,CG} \cdot R_{CG} = g_{m,CS} \cdot R_{CS}$$

If the two conditions are completed, the common-gate noise current creates two in-phase equal voltages at the outputs which cancel out by virtue of differential signal processing.

This section will discuss about the efficiency of this noise-cancelation technique in mm-waves context regarding the input matching, the gain and the noise. To perform this analysis, the model presented in Figure 82(b) is considered, where M_1 stands for the common-gate transistor and M_2 for the common-source one. For sake of readibility, some preliminary equations are defined in Equation 46.

Equation 46 – Preliminary equations on noise-cancelling amplifier model

$$Y_{ds1} = g_{ds1} + j\omega C_{ds1}\ ; \qquad Y_{dg1} = j\omega C_{dg1} + Y_{CG}\ ;$$
$$Y_{ds2} = g_{ds2} + j\omega C_{ds2} + Y_{CS}\ ; \qquad Y_{dg2} = j\omega C_{dg2}$$
$$Y_{gs} = j\omega\left(C_{gs1} + C_{gs2} + C_{pL_1}\right) + \frac{1}{j\omega L_1}$$

a) Input Matching

As detailed in Chapter 2.III.2, the input matching is dominated by the common-gate transistor. Nevertheless, in millimeter-wave, the parasitics as well as the common-source stage cannot be neglected. For this analysis, two paths are first considered, and an overall input impedance is then calculated. In Equation 16, the input impedance of the main path is expressed. We note if we neglect the capacitive contributions and output conductance in Equation 47, we find the conditions defined in Equation 17.

Equation 47 – Common-gate impedance

$$Z_{in,CG} = \frac{Z_{ds1} + Z_{dg1}}{1 + g_{m,CG}Z_{ds1}} = \frac{g_{ds1} + j\omega\left(C_{ds1} + C_{dg1}\right) + Y_{CG}}{\left(g_{m,CG} + g_{ds1} + j\omega C_{ds1}\right)\cdot\left(j\omega C_{dg1} + Y_{CG}\right)}$$

For the auxiliary path, the expression of common-source amplifier input impedance is expressed in Equation 48.

Equation 48 – Common-source impedance

$$Z_{in,CS} = \frac{Z_{ds2} + Z_{dg2}}{1 + g_{m,CS}Z_{ds2}} = \frac{g_{ds2} + j\omega\left(C_{ds2} + C_{dg2}\right) + Y_{CS}}{\left(g_{m,CS} + g_{ds2} + Y_{CS} + j\omega C_{ds2}\right)\cdot j\omega C_{dg2}}$$

Combining Equation 47 and Equation 48, the overall input impedance of the noise-cancelling amplifier is expressed in Equation 49. It includes the gate-source capacitances of M_1 and M_2, and the input parallel inductor L_1, Figure 82(a), modeled by Z_{gs} in Figure 82 (b). With a proper sizing of such devices, it is possible to cancel the imaginary part of Zin and to match a source impedance Rs.

Equation 49 – Overall input impedance of a common-gate-based noise-cancelling amplifier

$$Z_{in} = \frac{1}{\frac{1+g_{m2}Z_{ds2}}{Z_{gd2}+Z_{ds2}} + \frac{1+g_{m1}Z_{ds1}}{Z_{ds1}+Z_{dg1}} + j\left(\omega(C_{gs1}+C_{gs2}) - \frac{1}{\omega L_1}\right)}$$

b) Conversion gain

As discussed in the introduction, the gain balance between the two paths is important to perform the cancellation of the common-gate noise and to ensure the integrity of the signal. Equation 50 presents the conversion gain for each path. The gain balance, in terms of phase and amplitude, is tuned by adjusting the output loads Z_{dg1} and Z_{ds2} through L_{CG} and L_{CS} respectively.

Equation 50 – Definition of conversion gain in each path

$$A_{vCS} = \frac{v_{ds2}}{v_{gs2}} = \frac{1-g_{m2}Z_{dg2}}{1+{Z_{dg2}}/{Z_{ds2}}} \;\; ; \;\; A_{vCG} = \frac{v_{dg1}}{v_{sg1}} = \frac{1+g_{m1}Z_{ds1}}{1+{Z_{ds1}}/{Z_{dg1}}}$$

c) Noise figure

As introduced in Chapter II, the noise contribution of the main path, i.e. the common-gate stage, can be cancelled, at least significantly reduced. To achieve the cancelation of the thermal noise contribution of common-gate transistor M_{CS}, the common-gate and common-source paths must be balanced. In millimeter-Wave, the balance between both paths is difficult to ensure due to the impact of parasitics. As consequences, the contribution of the CG thermal noise is not completely cancelled but still significantly reduced compared to the CS noise contribution.

2. Post-layout simulations

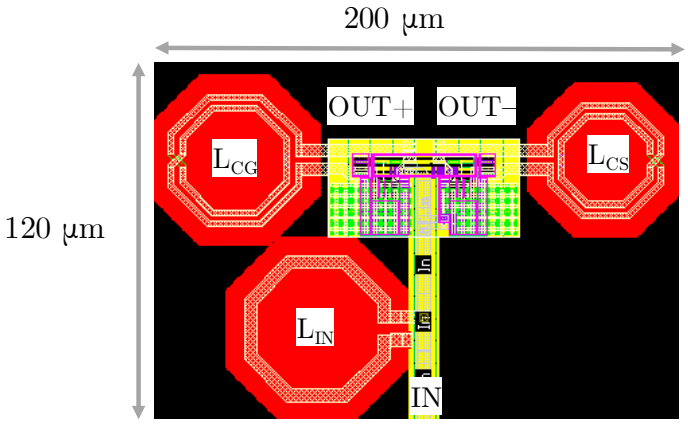


Figure 83 – Layout of the proposed noise-cancelling LNA

Based on the analysis proposed in the previous section, a noise-cancelling low noise amplifier has been designed and implemented in 28nm CMOS bulk. For some reasons related to the performance, further discussed at the end of the Chapter 1.III.1, this LNA has not been manufactured and only post-layout simulations are proposed in PVT. Figure 83 shows the layout of the circuit, the silicon footprint is 0.024mm^2. The nominal supply voltage is 0.6V and the overall power consumption is 4.6mW. As the LNA is not very sensitive to supply voltage variations, the simulation results for different supply voltages are reported for graphical readability.

(1) Input matching

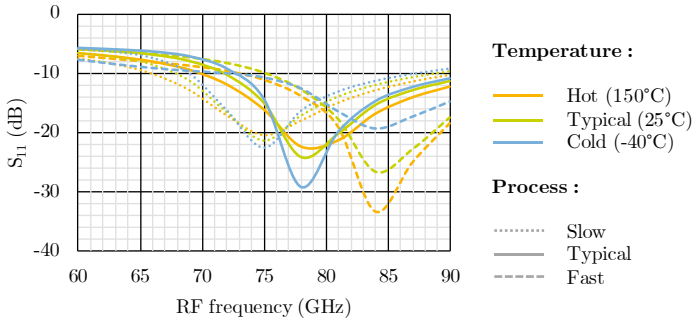


Figure 84 – PT post-layout simulation of return loss (S_{11})

In post-layout simulations, Figure 84, a wideband input matching is ensured with at least a 20% bandwidth from central frequency. The variation of the central frequency of the matching bandwidth is mainly due to process. As the noise-cancelling LNA input impedance is dominated by the common-gate transconductance, the variation of the threshold voltage or the process parameter can significantly impact the input impedance. A -10dB return loss is ensured over the 76-81GHz band.

(2) Conversion gain and linearity

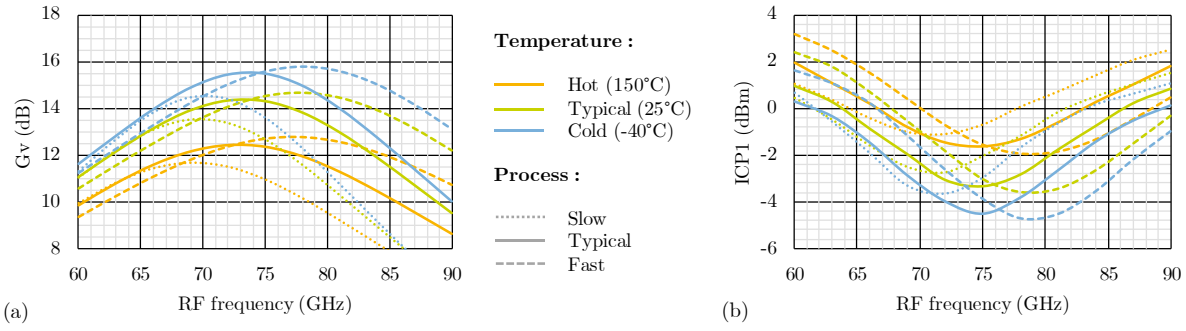


Figure 85 – PT post-layout simulation of: (a) conversion gain (Gv), 1dB compression point (ICP1)

In Figure 85(a), the conversion gain is simulated in post-layout extraction with temperature and process variations. The frequency for maximum gain mainly depends on the process whereas the maximum conversion gain is more dependent to the temperature. The conversion gain varies between 10dB in the hot worst case and 16dB in the cold best case. For the linearity, shown in Figure 85(b), the input compression point presents an important variation from -5dBm to +1dBm. Interestingly the specification of -5dBm is still addressed even for the largest conversion gain. Under these conditions the linearity would be limited by the passive mixer.

(3) Noise figure

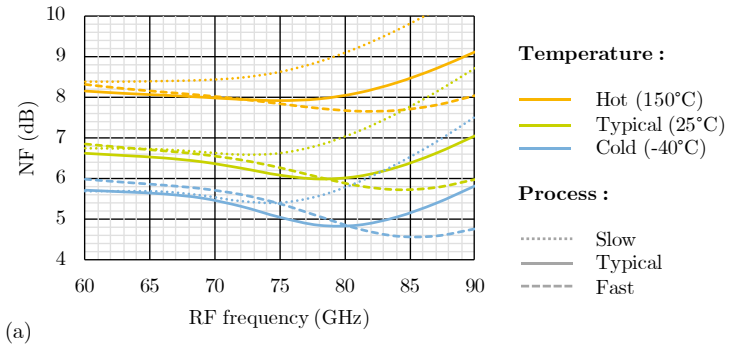


Figure 86 – PT post-layout simulation of NF

In Figure 86, the post-layout simulations of the noise figure are proposed with temperature and process variations. The nominal noise figure in typical case is about 6dB in the targeted band. The NF exhibits an important variation due to temperature, up to +3dB in hot case. Such high value of NF limits the complete RFFE performance and does not respect the specifications for long range radar.

(4) Balance

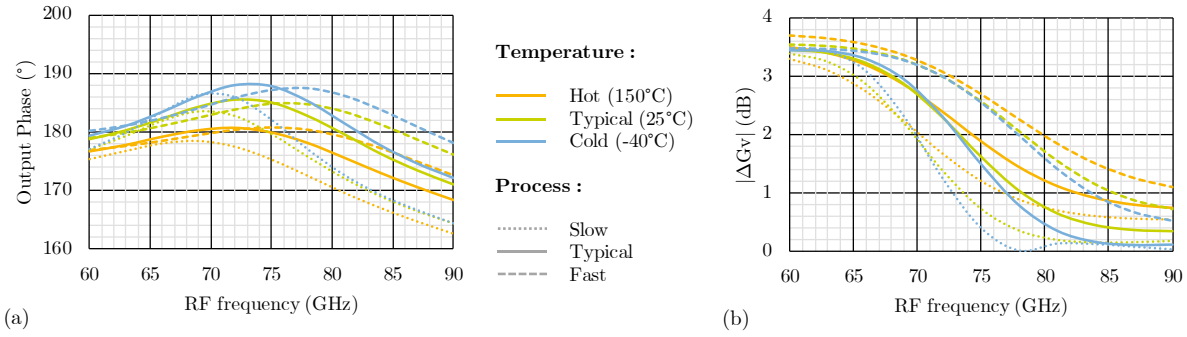


Figure 87 – PT post-layout simulation of imbalance between paths considering: (a) output phase; (b) gain imbalance

The common-gate-based noise-cancelling architectures achieves an inherent single-to-differential behavior but, due to the amplifier asymmetry, the balance between both paths must be controlled. In Figure 87(a), the relative phase of the output signal is represented, it fluctuates from 170 to 190°. In Figure 87(b), the gain imbalance between CG and CS paths is reported. It is below 1dB for slow and typical process variations from 77GHz to 90GHz. However, it goes up to 2dB for fast corners 76GHz. The important variation of phase and amplitude imbalance inherent to the asymmetrical architecture of the LNA can be an issue for the RX-RFFE performances.

3. Single Balanced LNA and down converter performances

Introduced in [26], the common-gate based noise-cancelling architecture significantly improves the RF performances, summarized in Table 17, with a limited DC power consumption. In comparison to the literature, referenced in Table 16, this 1-stage LNA achieves a high linearity with an ICP1 of -5dBm at a reduced power consumption of 4.6mW. The typical noise figure is closed to 6dB, degraded to 9dB in worst case of PVT. According to Chapter 2.I.1, the noise-cancelling topology does not achieve lower NF than conventional common-source architectures but performs a good trade-off between RF performances and a wideband input matching.

Table 17 – Performances of the proposed LNA and a downconverter using this LNA with a voltage-mode mixer including typical case at 25°C and worst case in PVT

Parameters	LNA (Typical)	LNA (Worst)	RX (Typical)	RX (Worst)
Gain (dB)	14	8.7	9.6	6.3
Noise figure (dB)	6	9.4	11.4	13.7
ICP1 (dBm)	-5	-4.5	-3.4	-5.5
Power consumption (mW) / VDD (V)	4.6 / 0.6V	< 5 / 0.6V	< 5 / 0.6V	< 5 / 0.6V

To discuss the performance of the LNA at system level, the Table 17 reports an evaluation of a downconverter based on the proposed noise-cancelling LNA combined with a real passive mixer in voltage mode. The analysis and the performances of the voltage mixer are further developed in the Chapter IV. Due to the passive mixer topology, the proposed downconverter presents a typical conversion gain of 9.6dB reduced to 6.3dB in worst case of PVT. Under this worst-case condition, the overall noise figure, 13.7dB, exceeds the specification as well as the linearity with a ICP1 of -5.5dBm.

Even if this noise-cancelling amplifier exhibits interesting nominal performances, it has not been selected for fabrication due to some limitations in terms of:

a) Noise Figure and Gain, especially for worst case PVT corners

b) Sensitivity of balanced operation to PVT corners, inherent to the asymmetry of the architecture

c) Acceptable but limited linearity when associated with a voltage mode mixer.

III. Complementary capacitor-cross-coupled amplifier

In the previous sections, the advantage of noise-cancelling approach in terms of bandwidth, gain and noise figure is illustrated with the implementation of common-gate based LNA. The investigations also point out the sensitivity of such architecture to achieve a balanced operation due to the inherent asymmetry of the topology combining two independent and different paths, and performing a single to differential operation. To address this issue a fully differential architecture would be preferred.

First, several LNAs featuring noise-cancelling techniques are discussed. The second part introduces a novel topology called "complementary capacitor-cross-coupled amplifier". Finally, the design and the implementation of this proposed LNA at 80GHz is developed and illustrated with post-layout simulations in PVT variations.

1. Introduction to differential noise-cancelling

The architecture of the noise canceling LNA developed in the previous section performs a single input to differential output operation through two independent paths based on a CG configuration and a CS configuration respectively. First, a fully differential topology is studied based on the same noise-cancelling architecture. A capacitor-cross-coupled technique is further investigated in millimeter-Wave domain to improve the current efficiency.

a. Fully differential noise-cancelling LNA

Considering that the main problem of the noise-cancelling amplifier is the imbalance between the common-source and common gate paths, we consider a differential implementation, Figure 88, to address it. The topology proposed in Figure 88 is technically a pseudo-differential circuit since the transistor sources are not tied to a current source. The reason is the parasitics of the current source has more drawbacks than benefits on circuit performances at mmWaves. For sake of simplicity we will further use the word differential instead of pseudo-differential for mmWaves circuits. The conditions for noise cancellation are the same as the ones described for the single balanced topology of section II considering a 100Ω input impedance. The input/output transformers are exploited as two folds: a) to isolate the circuit bias from

input/output nodes b) to resonate out the parasitics. Beside the coupling effect of transformers contribute to reduce the generation of even harmonics, including common mode, and to improve balanced operation inherent to a differential implementation.

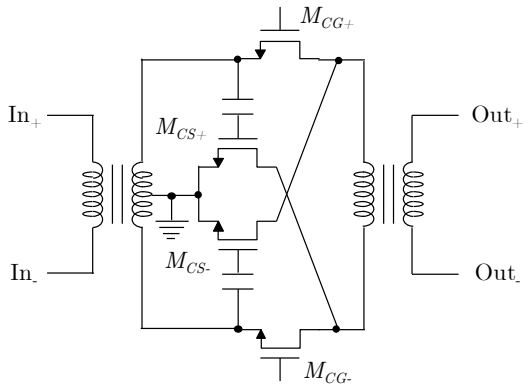


Figure 88 – Differential noise-cancelling amplifier with input and output transformers (biasing not shown)

The circuit presented in Figure 88 is simulated at schematic level, for typical and worst cases. The simulation results reported in Table 18 figure out the nominal performances could address the specifications, but the worst case of PVT corners do not. These results are consistence with the investigations proposed in section II, only the balanced operation is improved by this differential implementation.

Table 18 – Schematic simulation in typical and hot case for automotive radar applications

Parameters	LNA (Typical)	LNA (worst case)
Conversion Gain (dB)	9.5	7.5
Noise figure (dB)	5.5	6.7
ICP1 (dBm)	-5	-5
Power consumption (mW) / VDD (V)	<5 / 0.6V	<5 / 0.6V

b. Capacitor-cross-coupled LNA

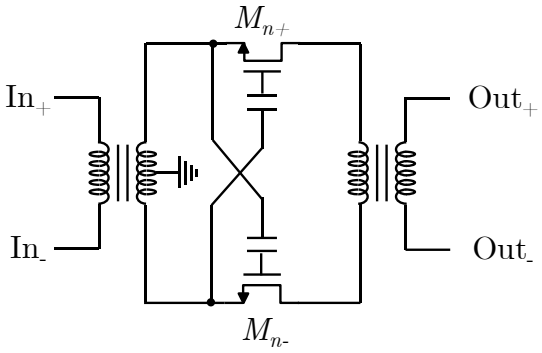


Figure 89 – Capacitor-cross-coupled amplifier with input and output transformer (biasing not shown)

The performances of a CG based amplifier can be improved by the capacitor-cross-coupled technique, proposed in [52], presented in Figure 89. The idea is to merge the common-source and common-gate paths by virtue of the differential implementation. In Figure 90(a), the concept is illustrated for the AC signal path: the input signal v_{in+} is applied on M_{n+} source and M_{n-} gate, it leads to generate opposite-phase RF signals at the amplifier output. The input signal v_{in-} applied on M_{n-} source and M_{n+} gate experiences the same operation. This symmetrical, but opposite phase, operation virtually doubles the transconductance, and only a 10mS transconductance is necessary to matching a 100**Ω** input impedance. It leads then to a reduction of the current consumption by a factor of 4.

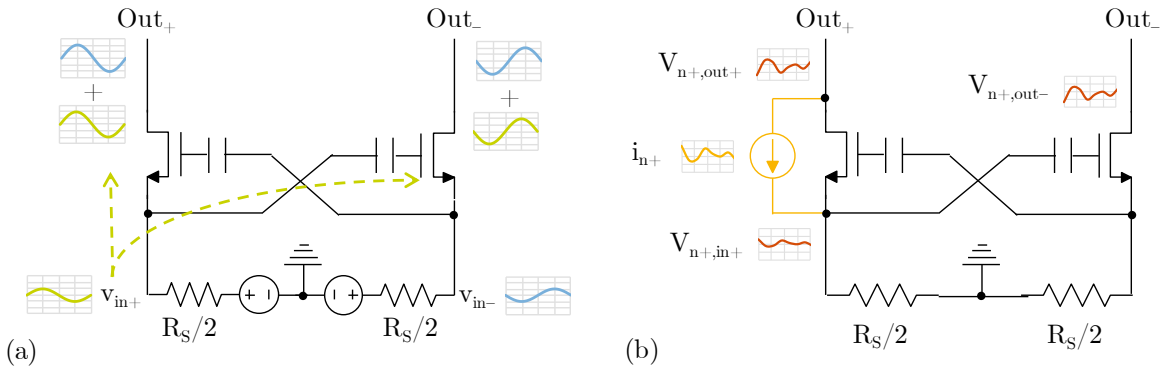


Figure 90 – (a) RF signal and gain in cross coupled topology; (b) Noise cancellation in a cross coupled topology for the M_{n+} noise

Interestingly the noise cancelation inherent to the CG capacitive cross-coupled topology of Figure 90 was originally not noticed. But if we consider the schematic of Figure 90(b) for noise analysis, we observe the noise generated by M_{n+} transistor creates two anti-phase voltages at Out+ and In+ nodes. The noise voltage $v_{n+|in+}$ is then inversed and amplified by the common-source transistor. As for noise-cancelling, these two anti-phase noise voltages can be, at least, partially canceled by virtue of differential signal processing.

The circuit presented in Figure 90 is simulated at schematic level, for typical and worst case. The simulation results reported in Table 19 figure out the nominal performances could address the specifications, but the worst case of PVT corners do not.

Table 19 – Schematic simulation in typical and hot case for automotive radar applications

Parameters	LNA (Typical)	LNA (worst case)
Conversion Gain (dB)	8.7	6.5
Noise figure (dB)	5.3	6.8
ICP1 (dBm)	-5.2	-5.6
Power consumption (mW) / VDD (V)	<4 / 0.6V	<4 / 0.6V

2. Principle of C4 LNA

The section II demonstrates the interest of noise-cancelling technique in common-gate based architectures for the implementation of LNA in mm-Waves domain. It also highlights the limitations due to the inherent asymmetry of the original architecture. A fully differential implementation has been discussed in section III.1 to reduce the sensitivity of the balanced operation to PVT corners. A capacitive cross coupled arrangement of the differential architecture has been also considered to improve the current efficiency. This section focuses on a novel version of the capacitive cross coupled namely complementary *capacitor-cross-coupled amplifier*.

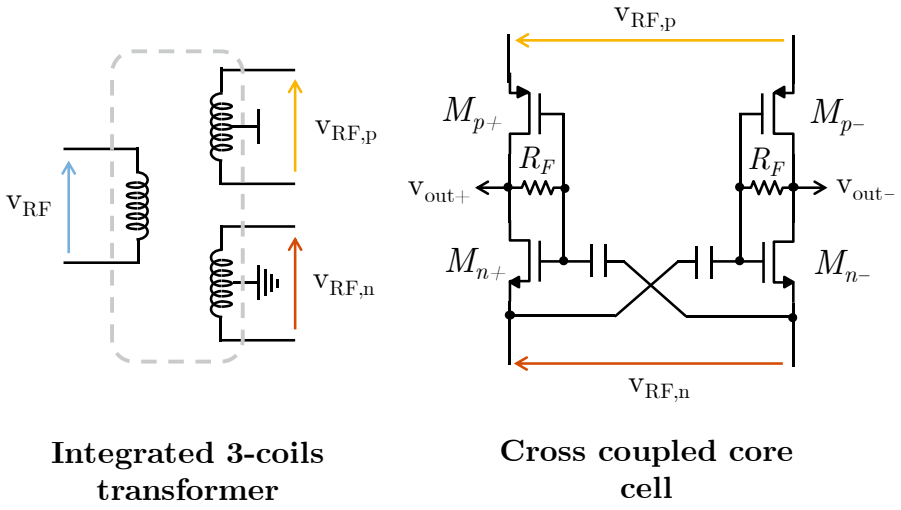


Figure 91 – Complementary capacitor-cross-coupled amplifier with an input transformer

To improve the conventional cross coupling architecture, an amplifier is proposed in Figure 91. The circuit uses a transformer with one primary coil and two secondary coils which splits (almost) equally the input RF voltage on the Pmos and Nmos transistor sources of the cross-coupled core cell. This cell features a current-reused amplifier to improve the current efficiency. As proposed for a conventional cross coupled topology, the RF input voltage is applied on the source and, simultaneously, on the gate of the opposite transistor as shown in Figure 91. It allows to increase the transconductance of each transistor by a factor of 4. This amplifier works as a transimpedance amplifier (TIA) when loaded by a low to moderate impedance. Operating as a TIA the compression point is improved since the linearity of the amplifier is not first limited by the output voltage headroom.

To ensure the transistors operate in saturation region, the current-reused amplifier is self-biased by a feedback resistor (R_F). The following subsections detail the analysis of the input matching, the transconductance and the noise figure.

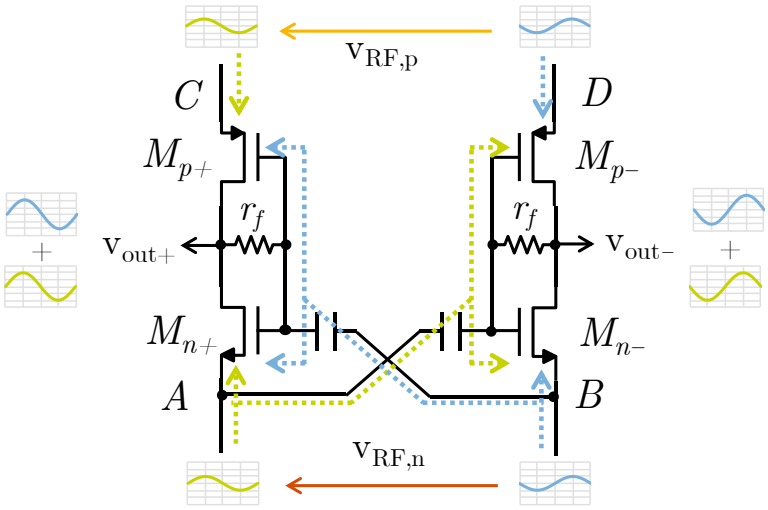


Figure 92 – Gain and RF signal in the cross coupled cell

a. Modelling of the three-coil transformer

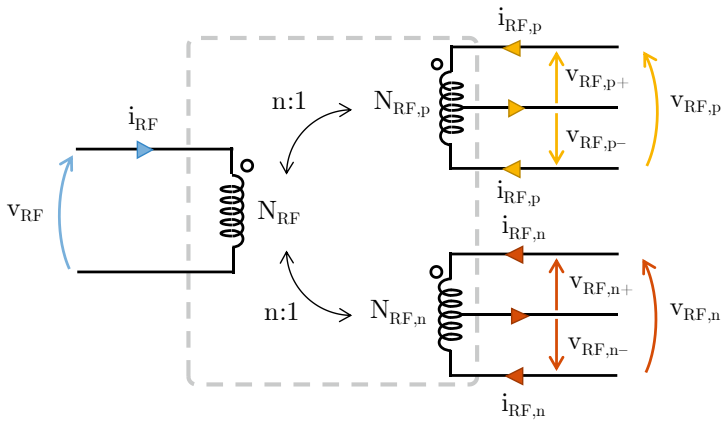


Figure 93 – Modelling of the transformer with one primary and two secondary coils

As described in Figure 93, a three-winding integrated transformer is used for the proposed topology. This section proposes a basic model of this transformer, necessary to describe the mechanism of input matching and gain boosting, as well as the thermal noise canceling. Based on Figure 93, the basic equations of this transformer are proposed in Equation 51 for the voltage and the current transfer.

Equation 51 – Basic equations of the three coils transformer

$$\frac{V_{RF,p}}{V_{RF}} = \frac{N_{RF,p}}{N_{RF}} = 1/n \;;\; \frac{V_{RF,n}}{V_{RF}} = \frac{N_{RF,n}}{N_{RF}} = 1/n \;;\; \frac{V_{RF,n}}{V_{RF,p}} = \frac{N_{RF,n}}{N_{RF,p}} = 1$$

$$I_{RF} = 2 \cdot I_{RF,p} \cdot \frac{N_{RF,p}}{N_{RF}} = 2 \cdot I_{RF,n} \cdot \frac{N_{RF,n}}{N_{RF}}$$

Considering these basic equations, Equation 52 proposes a calculation of the impedance shown at secondary outputs and the associated voltages. As both secondary coils are identical, a transforming ratio (n) is considered between primary and secondary windings. This ratio may be considered for the sizing of the amplifier.

Equation 52 – Impedance and voltage at the secondary outputs considering a transforming ratio n

$$Z_{S1/2} = 2 \cdot \frac{Z_p}{n^2} \quad ; \quad V_{S1/2} = V_p \cdot \frac{1}{n}$$

The back-end of the 28nm CMOS technology, illustrated in Figure 32, includes two thick copper layers (M7, M8) and a very thick aluminum (AP) layer which are exploited to implement the transformer as follows: the primary winding is laid out in AP layer and the two secondary windings are drawn in M7 and M8 layers. Figure 94 shows the layout of the transformer, its footprint is 62µm x 72µm.

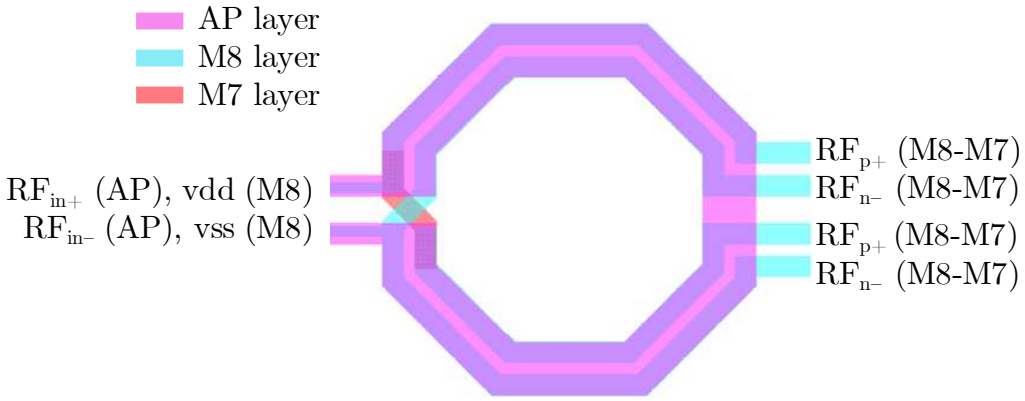


Figure 94 – Layout of the proposed transformer

b. Modelling of C4 LNA

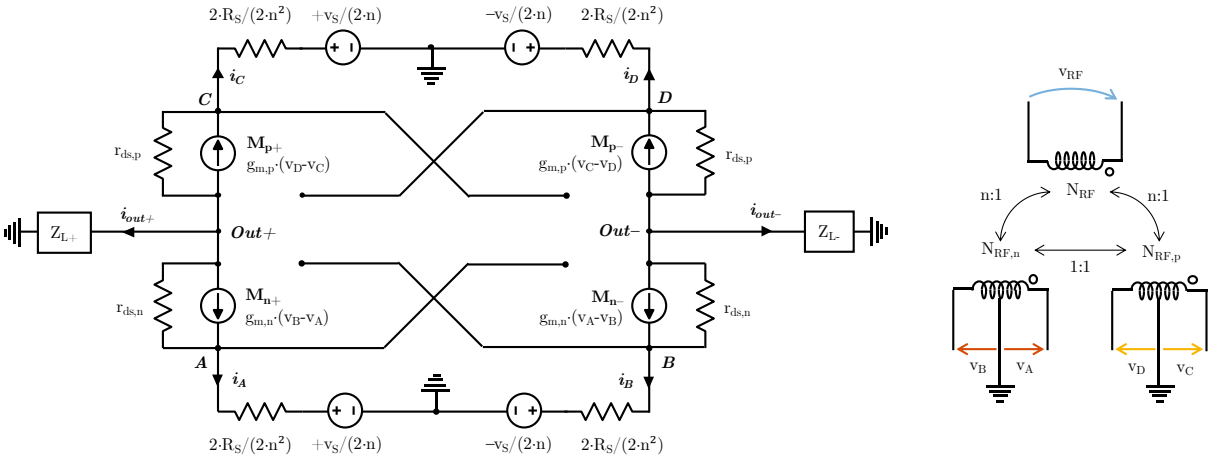


Figure 95 – Modelling on the C4 LNA

This section focuses on the modelling of the gain and the input matching of the C4 transconductance amplifier. For this analysis, a small signal equivalent model is proposed in Figure 95. For the sake of clarity, capacitive and inductive elements are neglected. As the PMOS and NMOS stages are symmetrical, their characteristics are assumed equivalent.

(1) Impedance matching

To achieve the matching of the complete amplifier, the three-winding transformer should be matched at the input port and at the output port. The analysis focuses on the NMOS stage, and duplicated to the entire architecture by virtue of the complementary, and symmetrical, configuration of the topology. Equation 53 proposes an expression for the input impedance of AB stage, including the output impedance Z_L. A final expression, excluding the capacitive and inductive elements, is proposed. If the amplifier is used in transconductor mode, the output resistance $r_{ds,n}$ of the transistor can be considered significantly higher than the output load $Z_{L\pm}$. The input impedance is then dominated by the transconductance of the transistor.

Equation 53 – Expression of AB input impedance

$$Z_{in,AB} = \frac{v_A - v_B}{i_A - i_B} = \frac{v_{A,Out+} - v_{B,Out-}}{i_A - i_B} + Z_{L\pm} = \frac{r_{ds} + Z_{L\pm}}{1 + 2g_m \cdot r_{ds}} \approx \frac{1}{2 \cdot g_m}$$

Considering the expression of the input impedance of the amplifier core and the transformer output impedance, a matching condition is then expressed in Equation 54. To achieve this matching, the transconductance of the transistor must be adjusted to the transformer coil ratio. However, the current consumption increases accordingly.

Equation 54 – Matching condition on g_m expression

$$Z_{in,AB} = \frac{R_S}{n^2} = \frac{1}{2 \cdot g_m} \Leftrightarrow g_m = \frac{n^2}{2R_S}$$

(2) Amplifier transconductance

Equation 55 proposes an expression of the output current depending of the differential input voltage. If we assume a lossless transformer, the input RF power is fully transmitted through the transformer to the amplifier core.

Equation 55 – Output current expression

$$i_{out} = i_A - i_B + i_C - i_D = \frac{2g_m + g_{ds}}{1 + g_{ds} \cdot Z_L} \cdot (V_B - V_A + V_D - V_C)$$

$$\text{with } V_A - V_B = V_C - V_D = \frac{R_S}{2n^2} \cdot i_{out} + \frac{v_S}{n}$$

With the expression of the output current Equation 55, it is possible to determine the overall transconductance of the amplifier ($G_{m,LNA}$) proposed in Equation 56.

Equation 56 – Expression of the LNA transconductance

$$G_{m,LNA} = \frac{i_{out}}{v_S} = \frac{\frac{2}{n} \cdot \frac{2g_m + g_{ds}}{1 + Z_{L\pm}/r_{ds}}}{1 + \frac{R_S}{n^2} \cdot \frac{2g_m + g_{ds}}{1 + Z_{L\pm}/r_{ds}}} \Rightarrow G_{m,LNA} \approx \frac{4g_m}{n\left(1 + \frac{2R_S g_m}{n^2}\right)} = n/R_S$$

If the amplifier is exploited in a transconductance mode we can assume: $r_{ds} >> Z_{L\pm}$ and $g_m >> g_{ds}$. Hence the transconductance is simplified to Equation 56 under matching conditions, defined in Equation 54. Interestingly the transimpedance gain ($G_{m,LNA}$) becomes proportional to the transformer ratio n.

Equation 57 – Simplified transconductor gain under input matching conditions

$$G_{m,LNA} \approx \frac{4g_m}{n\left(1 + \frac{2R_S g_m}{n^2}\right)} = n/R_S$$

c. Noise analysis of C4 LNA

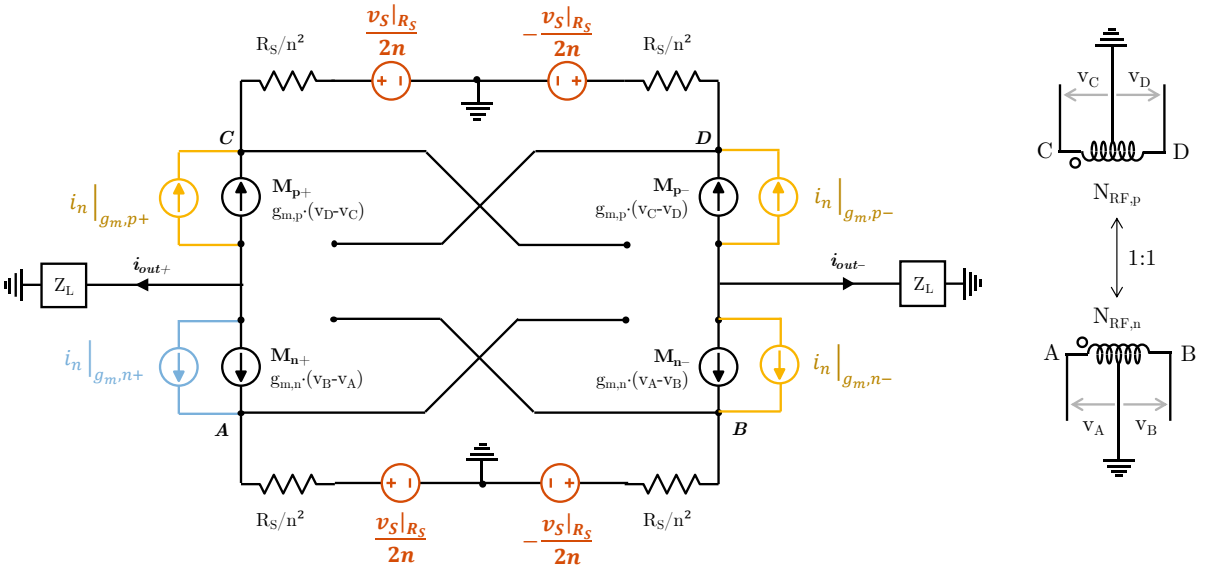


Figure 96 – Noise modelling of the C4 LNA

Figure 96 illustrates the main source of noise of the proposed amplifier used in transconductor mode, only the drain thermal noise of MOS devices is first considered. Indeed, bias resistor R_F is large, typically more than 10K, and can be neglected. Besides the sick metal

level, M7, M8 and AP exploited to implement the 3-coil transformer, together with the small foot print of the device at mm-Waves, contribute to achieve a low value of the winding sheet resistance. In this simplified analysis, two main sources of noise are considered. First, the noise contribution of amplification transistors, detailed for the M_{n+} transistor. Secondly, the noise of the source modelled by noise sources and resistors seen through the input transformer.

(1) Transistors noise

Considering the noise of one transistor, for instance M_{n+}, the thermal noise current ($i_{n+}|_{n+}$) generates a noise voltage at node A ($v_A|_{n+}$), and through, the input transformer, a noise voltage at node B ($v_B|_{n+}$). Due to the transformer configuration, the differential noise voltage between A and B ($v_A|_{n+} - v_B|_{n+}$) is also applied to the input of the complementary stage (M_{p+}, M_{p-}) as $v_C|_{,n+} - v_D|_{n+}$. It leads to the overall expression given in Equation 58.

Equation 58 – Noise output current expression of the M_1 transistor

$$i_{out}|_{n+} = \left(i_{n+} - i_{n-} + i_{p+} - i_{p-}\right)|_{n+} = 2g_m(V_B|_{n+} - V_A|_{n+} + V_D|_{n+} - V_C|_{n+}) + i_{n+}|_{n+}$$
$$\text{with } V_A|_{n+} - V_B|_{n+} = V_C|_{n+} - V_D|_{n+} = i_{out}|_{n+} \cdot \frac{R_S}{2n^2}$$

From Equation 58, we can derive the output current noise ($i_{out}|_{n+}$) due to M_{n+} noise, Equation 59. Interestingly this output noise current ($i_{out}|_{n+}$) is half of the M_{n+} noise current ($i_{n+}|_{n+}$). The C4 LNA performs a partial noise cancelation of the MOS thermal drain noise under input matching conditions.

Equation 59 – Final expression of the output current of one transistor noise

$$i_{out}|_{n+} = \frac{i_{n+}|_{n+}}{1 + \frac{4g_m R_S}{2n^2}} = \frac{i_{n+}|_{n+}}{2}$$

(2) Source noise

Equation 60 – Noise output current expression of the source (R_S) noise

$$i_{out}|_{R_S} = \left(i_{n+} - i_{n-} + i_{p+} - i_{p-}\right)|_{R_S} = 2g_m\left(V_B|_{R_S} - V_A|_{R_S} + V_D|_{R_S} - V_C|_{R_S}\right)$$
$$\text{with } V_A|_{R_S} - V_B|_{R_S} = V_C|_{R_S} - V_D|_{R_S} = i_{out}|_{R_S} \cdot \frac{R_S}{2n^2} + \frac{v_S|_{R_S}}{n}$$

The noise generated by the source is transferred to the amplifier core through the transformer. Equation 60 proposes an expression of the output current depending of the input voltages. Under input matching conditions, it can be simplified to Equation 61.

Equation 61 – Final expression of the output current of the source (R_S) noise

$$i_{out}|_{R_S} = \frac{4\, g_m v_S|_{R_S}}{1 + \frac{2 g_m R_S}{n^2}} = \frac{n}{R_S} \cdot v_S|_{R_S}$$

(3) Noise factor

The two expressions of noise contribution Equation 59 and 61 are used to define the C4 LNA noise factor F. Considering the matching conditions on transistor transconductance sizing, the noise factor does not depend on the topological factor (n) which makes this topology very interesting for the noise to power consumption trade-off. The minimum theoretical achievable noise figure is 1.25dB for a typical γ of 2/3. It is a reduction by a factor of 2.45 with respect to the theoretical NF of a conventional common-gate differential amplifier. This improvement corresponds to the partial noise-cancelling illustrated in Equation 61. In practice, the NF is larger accounting for all the sources neglected in this simplified noise analysis of the C4 LNA.

Equation 62 – Noise factor expression and

$$F = 1 + \frac{4\overline{i_{out}|_{n+}}^2}{\overline{i_{out}|_{R_S}}^2} = 1 + \frac{\frac{4}{4}\overline{i_n|_{n+}}^2}{\left(\frac{n}{R_S}\right)^2 \cdot \overline{v_S|_{R_S}}^2} = 1 + \frac{4kT \cdot \gamma \cdot g_m \cdot R_S}{4 \cdot 4kT \cdot n^2} = 1 + \frac{\gamma}{2}$$

d. C4 amplifier design trade-off

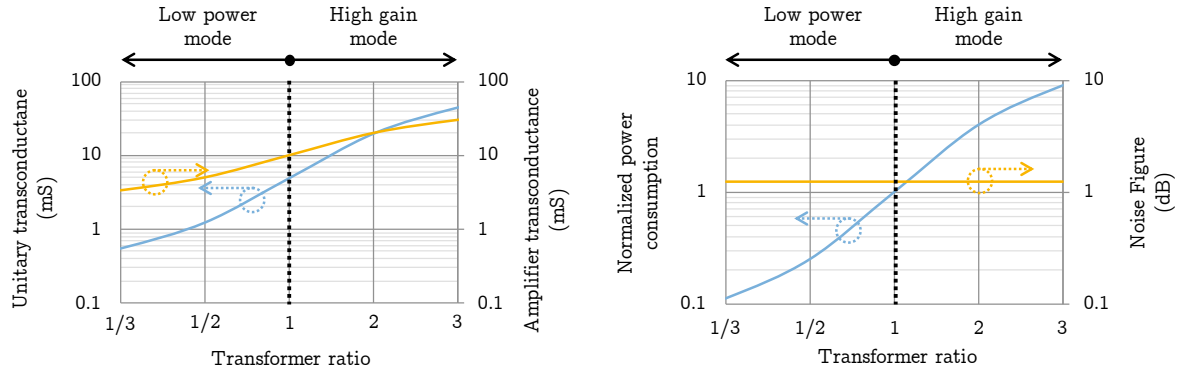


Figure 97 – Impact of transformer ratio on the figure of merit of the proposed amplifier

Considering the requirement of matching operation, the proposed architecture still have a degree of freedom on the selection of the transformer ration impacting both the power consumption and the transconductance values. The Figure 97 shows the evolution of the various parameters regarding the transformer ratio value. It leads to define two modes of operation can be defined, a low power mode and a high gain mode. For low power operations, the first mode uses the transformer as a voltage elevator transformer leading to undersize the unitary transconductance and the overall current consumption. The overall transconductance value is

less impacted leading to an improvement of the overall efficiency. For improving the RF performance, the second mode of operation artificially increases the unitary transconductance by reducing the voltage sweep at transformer output. It leads to increase the overall amplifier transconductance and the power consumption improving the overall RF performance. Interestingly, the noise figure is not impacted by the transformer ratio sizing.

3. Implemented mmWave C4 LNA

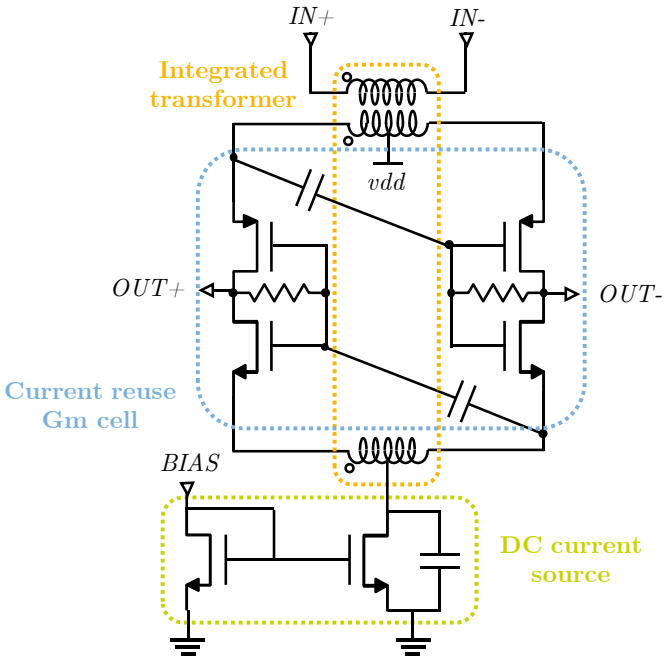


Figure 98 – Schematic of the implemented C4 LNA

A C4 LNA dedicated to 77GHz automotive radar applications has been implemented in 28nm RF-CMOS technology. The circuit is not yet measured but post-layout simulations are reported in this section with process and temperature variations. The noise calibration procedure is not performed on the C4 LNA only, but it is further proposed for a complete downconverter in Chapter IV. Figure 98 reports the schematic of the implemented C4 LNA which includes the input three-winding transformer, the amplifier core and a current source used for the bias control.

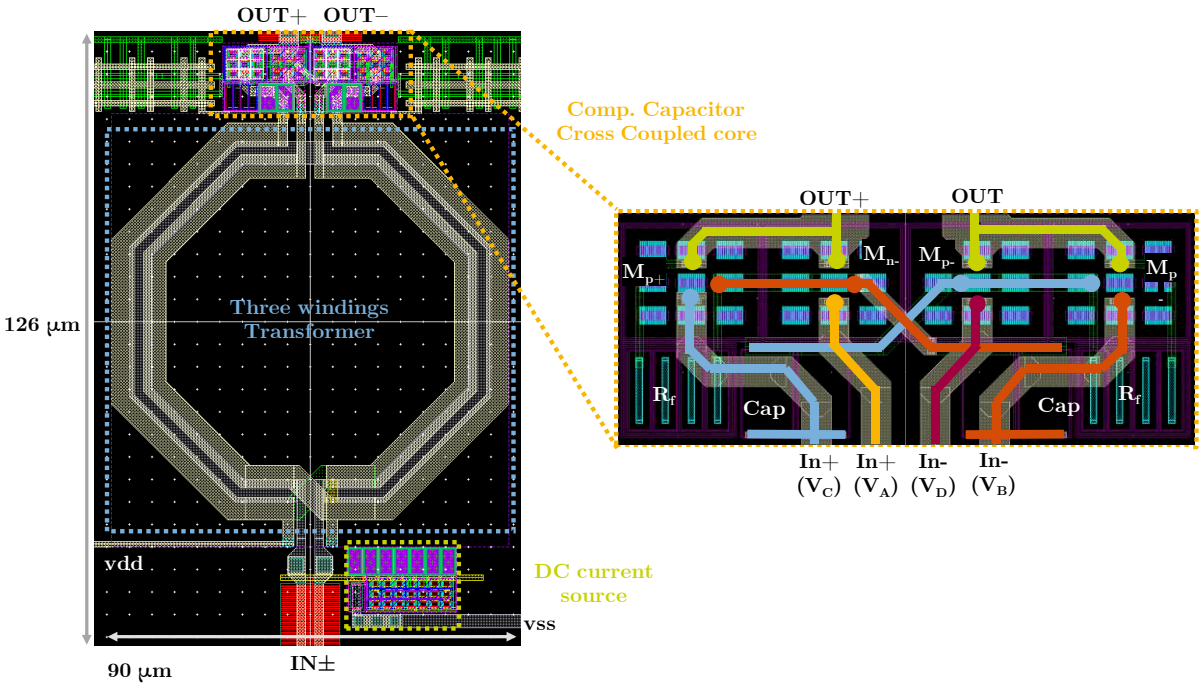


Figure 99 – Layout of the implemented C4 LNA with focus on the amplifier core

As illustrated in Figure 99, the layout of the amplifier is very compact, with a silicon footprint of 0.011mm^2 for an input transformer with a turn ratio of 1. As consequences, the transconductance of each transistor is adjusted to 5mS with a drain current of 2 mA, which corresponds to half of the current required to bias a conventional cross coupling topology. The nominal supply voltage and power consumption of the overall C4 LNA are 1.5V and 6mW respectively. Post-layout simulations show a minor impact of the supply voltage variation on the radar performances, less than 5% compared to nominal conditions. For the sake of clarity, it is not reported on the results presented herein after.

(1) Impedance matching

The proposed C4 LNA exhibits a wideband behavior in post layout simulations, as shown in Figure 100. A more than 15GHz bandwidth is achieved, and a great immunity to PVT variations is observed. This return loss is fully compatible with 77GHz radar applications.

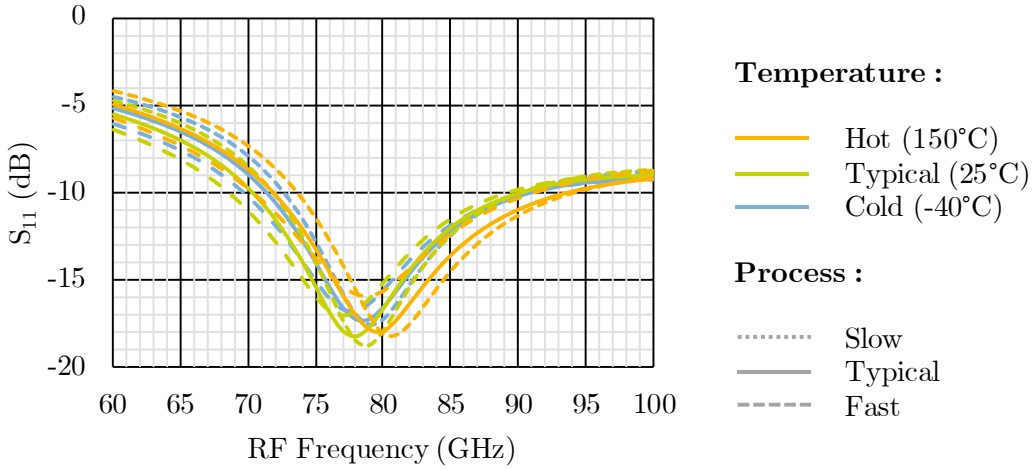


Figure 100 – Post layout simulations in temperature and process corner for return loss (S_{11})

(2) Gain & linearity

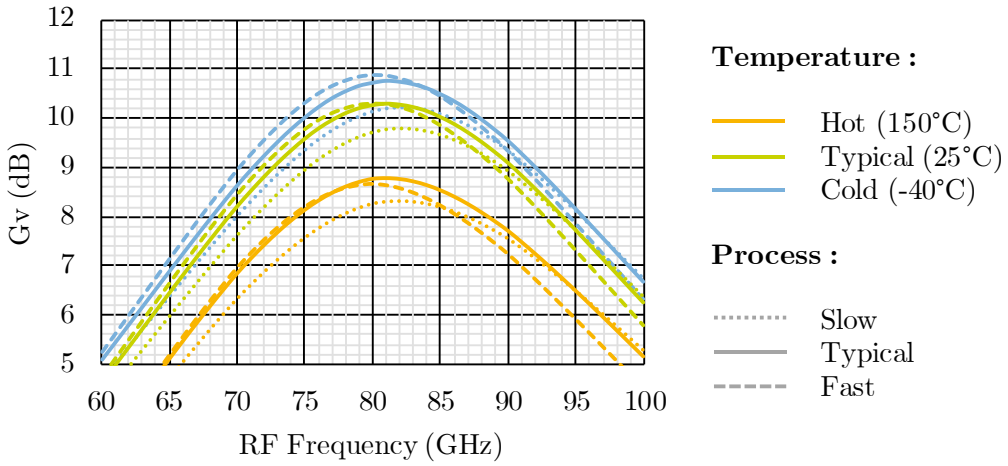


Figure 101 – Post layout simulations in temperature and process corner for conversion gain (Gv)

The post-layout simulations with temperature and process variations, Figure 101, show that the amplifier achieves a 10dB conversion gain in a typical case. In comparison to other presented topologies, the central frequency in PVT presents a small variation below 5GHz while the 3dB bandwidth is around 20GHz for each case corresponding to a 25% ratio between the bandwidth and the central frequency. On the other hand, the variation of the voltage gain is limited to 2.5dB, between 8.3dB and 10.9dB. Illustrated in Figure 102, the 1dB compression point is typically around -2.5dBm with small variations of ±0.5dB. This high linearity is fully compatible with the specification for radar applications.

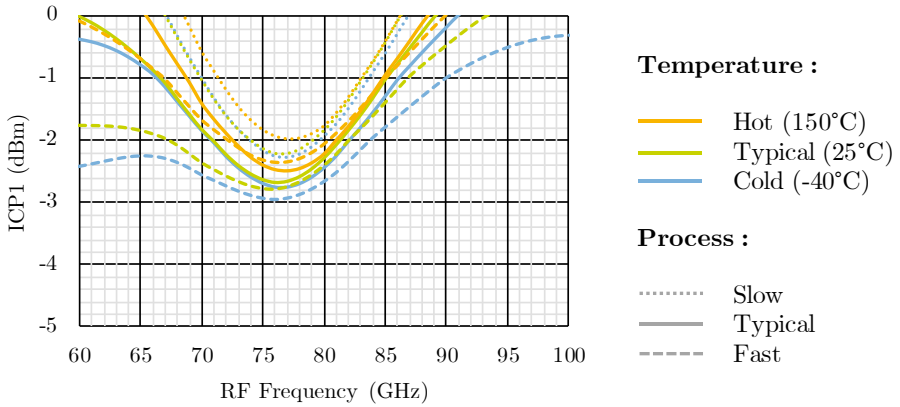


Figure 102 – Post layout simulations in temperature and process corner for 1dB compression point (ICP1)

(3) Noise figure

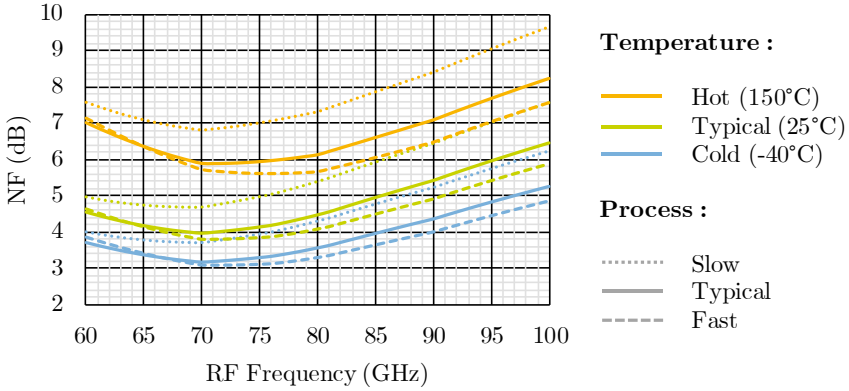


Figure 103 – Post layout simulations in temperature and process corner for Noise Figure (NF)

The noise figure is studied in Figure 103 in post-layout simulation with temperature and process variations. The nominal noise figure in typical case is 4.5dB in the targeted radar band. It is a good performance with respect to the operating frequency, 77GHz, and the power consumption, 6mW. Nevertheless, we observe a variation of +3dB in the hot case. This maximal noise figure is 2dB lower than the conventional noise-cancelling architectures and is compatible with long range radar specifications.

4. C4 LNA Conclusion

As discussed in section II, the basic architecture of common gate noise canceling LNA suffers from imbalance between paths generating common-mode. This drawback can significantly corrupt the signal processing in a zero IF demodulation chain such as automotive RADAR receivers. A fully differential implementation can address this issue at the cost of a doubled power consumption to achieve the same level of performance in terms of gain and noise figure. To improve the current efficiency, a complementary current reuse configuration is

proposed in a capacitor-cross-coupled arrangement. This new differential architecture of common gate noise canceling LNA, namely C4 LNA, is implemented in 28nm CMOS technology. The proposed C4 LNA achieves a low noise figure with typical value of 4.2dB at 77GHz, a gain of 10.8dB and a power consumption of only 4.2mW under 1.5V supply voltage. The complementary configuration coupled with a large voltage headroom allows for a high linearity with an ICP1 of -3dBm in worst case corners.

Table 20 – Performances of the proposed LNA and a downconverter using this LNA with a voltage-mode mixer including typical case at 25°C and worst case in PVT

Parameters	LNA (Typical)	LNA (Worst)	RX (Typical)	RX (Worst)
Conversion Gain (dB)	10.8	8.2	11.5	10
Noise figure (dB)	4.2	7.2	9.4	12
ICP1 (dBm)	-2.5	-3	-9	-9
Power consumption (mW) / VDD (V)	4.2 / 1.5V	< 5 / 1.5V	< 5 / 1.5V	< 5 / 1.5V

To discuss the performance of the LNA at system level, the Table 20 reports an evaluation of a downconverter based on the proposed C4 LNA combined with a passive mixer in voltage mode. A current mode passive mixer would be better suited since the C4 topology is of transconductance amplifier type. However, for a fair comparison with the downconverter proposed in section II, the same mixer, further developed in Chapter IV, is exploited. The proposed downconverter presents a typical conversion gain of 11.5dB reduced to 10dB in worst case which is more than 3 dB higher than the downconverter of section II. The noise figure is now limited to 12dB in the worst case, it was 13.7dB for the previous downconverter. The downconverter linearity cannot be fairly compared due to the voltage operation of the mixer. Due to the advantages shown by the C4 LNA, this topology has been selected to build a RX-RFFE compatible with long range radar applications.

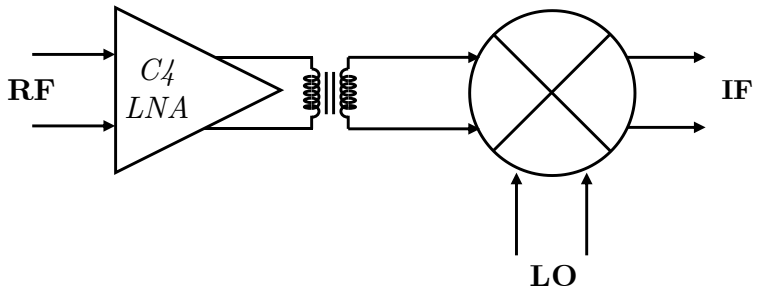


Figure 104 – RX including C4 LNA with voltage mode mixer

IV. Conclusion

Considering the specifications for long range radar presented in Table 9 of Chapter I, Chapter II highlights the limitations of active mixer-first downconverters and leads us to consider the combination of a low noise amplifier and a passive mixer. This Chapter III focuses on the design of the low noise amplifier. The interest of common-gate based noise cancelling configuration has been previously demonstrated. It is further considered, and combined with circuit techniques, to implement a new LNA architecture, named C4 LNA, in a 28nm RFCMOS technology at 77GHz.

First, a single-to-differential noise-cancelling amplifier is designed and evaluated through post-layout simulations. This topology achieves interesting RF performances regarding gain, linearity and power consumption but its noise figure is still too high to address the specifications. Besides the imbalance inherent to the architecture is not suited for RADAR demodulation processing. Thereafter, a differential complementary capacitor-cross-coupled amplifier topology is proposed. This architecture, implemented in millimeter-Wave, achieves a low noise figure and a high linearity for a limited power consumption but its gain is inferior compared to conventional noise-cancelling topologies.

Equation 63 – Figures of merit defined (a) with RF charateristics and power consumption; (b) with the previous ones added silicon area

$$FOMI = \frac{G_p \cdot ICP1}{(F-1) \cdot P_{DC}} \quad ; \quad FOMII = \frac{G_p \cdot ICP1}{(F-1) \cdot P_{DC} \cdot Area}$$

Table 21 presents the performances of the two proposed topologies in post layout simulations and a state of the art of millimeter-Wave LNAs. To compare the circuits two figures of merit are proposed: FOMI, Equation 63(a), only accounts for gain, NF, linearity and power consumption, and FOMII, Equation 63(b), which includes the silicon foot print. As discussed previously, conventional common-source amplifiers [5] cannot simultaneously achieve low noise, high linearity and enough gain with a low power consumption. Regarding multi-stages LNA, the two proposed circuits compares favorably in terms of noise figure, linearity and DC consumption, they exhibit a larger FOMI compared to other works. This trade-off is further increased considering the silicon area as illustrated with FOMII. Indeed, FOMII does not exceed 0.2 for the circuits of the state of the art, it is 5.3 for the NC LNA and 10.3 for the C4 LNA.

The impact of the LNA performance on a downconverter has been also estimated. The two proposed LNA are combined with a voltage-mode passive mixer. The best combination with respect to the gain and noise figure, is the one based on the C4 LNA. For this reason, the next chapter investigates the development, and implementation, of a down converter with a

C4 LNA, a passive mixer and a base band amplifier to address 77GHz long range RADAR applications.

Table 21 – State of the art of 80GHz LNA for automotive radar applications compared to post-layout simulations of the designed LNA in typical case (Power gain; $^{+}$Voltage gain)*

Parameters	[48]	[49]	[50]	[51]	NC LNA	C4 LNA
Tech. (nm)	CMOS 28nm	CMOS 45nm	CMOS 90nm	CMOS 65nm	CMOS 28nm	CMOS 28nm
Number of stages	2	3	4	1	1	1
Bandwidth (GHz)	57-72	87-110	72-95	72-86	73-90	71-90
Gain (dB)	13.8*	10.7*	7.6*	2.1*	14^{+}	10.8^{+}
NF (dB)	4	6	6.6	4.5	6	4.2
ICP1 (dBm)	-12.5	-3.2	-7	0	-5	-3
Power (mW) / VDD (V)	24 / 0.9V	52 / 2V	11.3 / 1.2V	22 / 1.2V	5 / 0.6V	4.6 / 1.5V
Area (mm^2)	0.38	0.32	0.59	0.33*	0.01	0.01
FOMI	0.008	0.011	0.012	0.032	0.053	0.12
FOMII	0.02	0.033	0.02	0.096	5.3	10.3

Chapter 4. 77-GHz Downconverter

Considering the tough requirements defined for RX-RFFE in Chapter I, the second Chapter demonstrates the limitations of active mixer topology, especially for the long-range radar case. Therefore, a downconverter featuring low noise amplifier and a passive mixer is preferred. The Chapter III studies several topologies of low noise amplifiers, and more specifically a Complementary Capacitor Cross Coupled (C4) amplifier. This LNA architecture exhibits a good tradeoff between RF performance, silicon footprint and DC power consumption. This Chapter focuses on the design of a downconverter with a comparison between voltage and current mode downconversion.

The first section reminds the modelling of passive mixers in order to understand the difference between voltage and current mode operation. In the section II, a voltage-mode downconverter is implemented, and a current-mode downconverter is proposed in section III. The two circuits have been fabricated but are not yet measured. Finally, the section IV makes a comparison between the two topologies and draws the conclusion of the selected RX-RFFE regarding the state-of-the-art and the application.

I. Introduction to CMOS passive mixer modelling

Since few years [53], RF receivers are supposed to target multi-standards applications and must fulfill challenging requirements such as wide bandwidth, high linearity and low noise. Addressing these specifications imply to reconsider passive mixers for frequency downconversion. For radar applications, the Chapter II highlights the limitation of active mixer topologies in terms of flicker noise in advanced RFCMOS technologies. To address this issue, a passive approach is now considered. Different architectures can be proposed operating in current or voltage mode. This section investigates passive mixer modeling to draw the conditions of such operation.

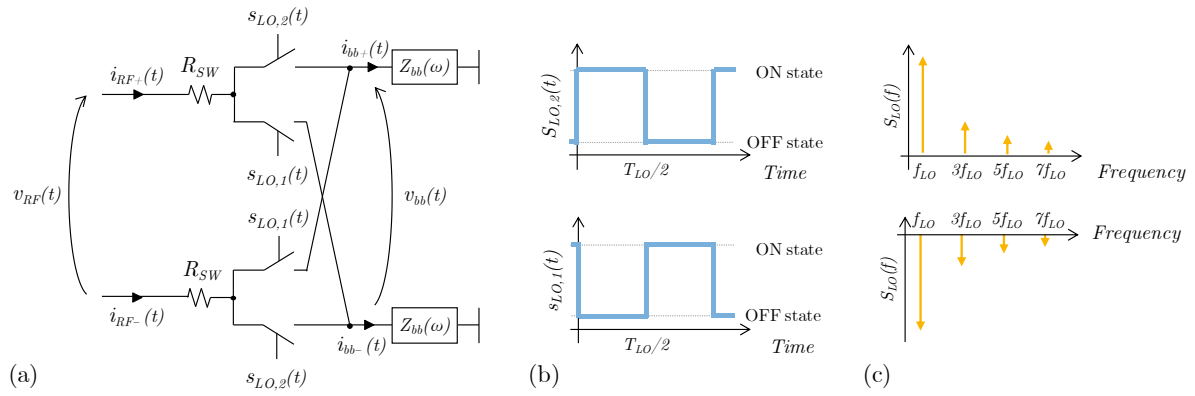


Figure 105 – (a) Mixer core model with baseband impedance; LO switches behavior in time domain (b) and frequency domain (c)

The LNA is modeled as an ideal current source driving the passive mixing quadrature cell, Figure 105(a). In current and voltage mixing cases, this RF input current, $i_{RF}(t)$, is mixed by the local oscillator ($s_{LO,k}$) by switching transistors featuring a series resistor (R_{SW}). The main difference between voltage and current mode operation comes from the baseband load (z_{bb}) which is high for voltage mode mixer (VGA) and low for current mode mixer (TIA). The LO waveform is depicted in Equation 64 with respectively a time domain representation, $s_{LO,k}(t)$, and a spectrum domain representation, $S_{LO,k}(\omega)$, proposed in Figure 105(b) and (c). For a square waveform, the even harmonics are null while the odd harmonics are equal to $a_n = {}^{4}/_{\pi n}$.

Equation 64 – Switch behavior expression in time and frequency domain for in-phase (k=2) and opposite-phase (k=1) LO signal

$$s_{LO,k}(t) = \sum_{n=-\infty}^{+\infty} (-1)^k \cdot a_n \cdot e^{jn\omega_{LO}t} \Leftrightarrow S_{LO,k}(\omega) = \sum_{n=-\infty}^{+\infty} (-1)^k \cdot a_n \cdot \delta(\omega - n\omega_{LO})$$

(1) Baseband IF current and voltage

Equation 65 – Baseband current expression for differential mixer in time and frequency domains

$$i_{bb}(t) = \Big(S_{LO,2}(t) - S_{LO,1}(t)\Big) \cdot i_{RF}(t) \Leftrightarrow I_{bb}(\omega) = \frac{1}{\pi} \sum_{n=-\infty}^{+\infty} a_n \cdot \delta(\omega - n\omega_{LO}) * I_{RF}(\omega)$$

$$I_{bb}(\omega) = \frac{1}{\pi} \sum_{n=-\infty}^{+\infty} a_n \cdot I_{RF}(\omega - n\omega_{LO}) \xrightarrow[LO]{Square} I_{bb}(\omega_{IF}) = \frac{4}{\pi} \sum_{n=-\infty}^{+\infty} \frac{1}{2n+1} \cdot I_{RF}(\omega - (2n+1)\omega_{LO})$$

Since the mixer is differential, at least two transistors are connected to the baseband section in each phase of LO signal, Equation 65 proposes an expression of the output current in the time domain, $i_{bb}(t)$. In frequency domain, it corresponds to the convolution product between the input RF current and the Dirac comb, leading to downconvert the RF current at

each harmonic of LO. Considering a square waveform, the baseband current only contains odd harmonics. The baseband voltage v_{bb} is then derived in Equation 66.

Equation 66 – Baseband voltage expression for differential mixer in time and frequency domains

$$v_{bb}(t) = i_{bb}(t) * z_{bb}(t) = \Leftrightarrow V_{bb}(\omega) = \sum_{n=-\infty}^{+\infty} a_n \cdot I_{RF}(\omega - n\omega_{LO}) \cdot Z_{bb}(\omega)$$
$$\xrightarrow[LO]{Square} V_{bb}(\omega_{IF}) = \sum_{n=-\infty}^{+\infty} \frac{1}{2n+1} \cdot I_{RF}(\omega_{IF} - (2n+1)\omega_{LO}) \cdot Z_{bb}(\omega_{IF})$$

(2) Input RF voltage

Equation 67 – Input RF voltage expression in time and frequency domain

$$v_{RF}(t) = 2R_{SW} \cdot i_{RF}(t) + \Big(s_{LO,2}(t) - s_{LO,1}(t)\Big) \cdot v_{bb}(t)$$
$$V_{RF}(\omega) = 2R_{SW} \cdot I_{RF}(\omega) + \frac{1}{2\pi}\Big(S_{LO,2}(\omega) - S_{LO,1}(\omega)\Big) * V_{bb}(\omega)$$

To understand the difference between current and voltage mode operation, the input RF voltage (v_{RF}) is derived in Equation 67. If we consider the input signal only includes components at the RF frequency, the input RF voltage is simplified to Equation 68.

Equation 68 – Input RF voltage expression frequency domain

$$V_{RF}(\omega) = 2R_{SW} \cdot I_{RF}(\omega) + \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} a_m \cdot a_n \cdot I_{RF}(\omega - (m+n)\omega_{LO}) \cdot Z_{bb}(\omega - m\omega_{LO})$$
$$V_{RF}(\omega_{RF}) = I_{RF}(\omega_{RF}) \cdot \left(2R_{SW} \cdot + \sum_{m=-\infty}^{+\infty} |a_m|^2 \cdot Z_{bb}(\omega_{RF} - m\omega_{LO})\right)$$

(3) Input RF impedance

Equation 69 – Input RF impedance expression and approximation in frequency domain

$$z_{RF}(\omega_{RF}) = 2R_{SW} + \sum_{n=-\infty}^{+\infty} |a_m|^2 \cdot Z_{bb}(\omega_{RF} - m\omega_{LO})$$
$$z_{RF}(\omega_{RF}) \approx 2R_{SW} + |a_0|^2 \cdot Z_{BB}(\omega_{RF}) + |a_1|^2 \cdot (Z_{bb}(\omega_{RF} - \omega_{LO}) + Z_{bb}(\omega_{RF} + \omega_{LO}))$$

Combining Equation 67 and 68, the input RF impedance Z_{RF} is derived in Equation 69. The baseband impedance Z_{BB} is translated at RF frequency by virtue of LO switching. Fortunately, the sum can be reduced, with a good approximation, to the two first terms, a_0 and a_1.

II. Voltage mode downconverter

In this section, the architecture of a downconverter featuring a low noise amplifier based on a C4 amplifier and a fully differential passive mixer is first presented. The post-layout simulations of this front-end are then presented and discussed. Finally, a conclusion is proposed regarding the automotive radar application.

1. Demodulation chain

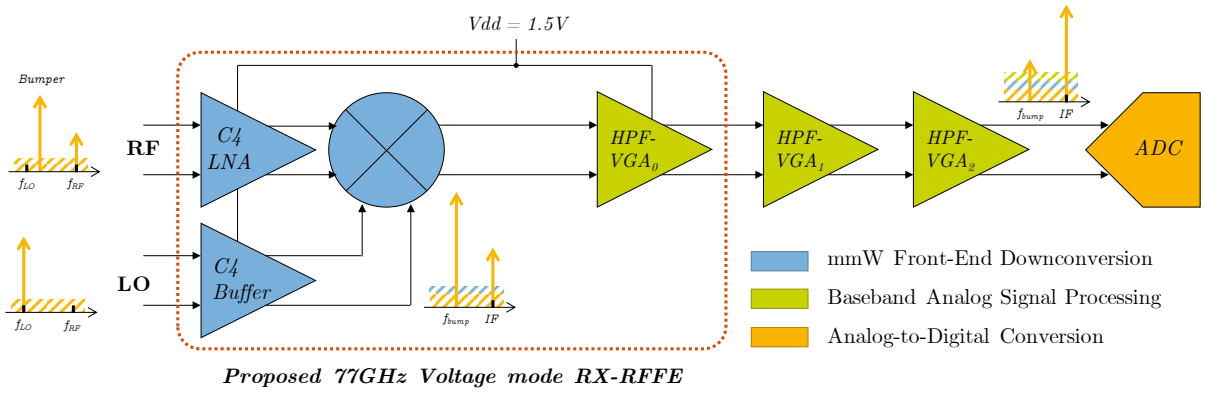


Figure 106 – Proposed Voltage-mode RX-RFFE in a complete demodulation chain

The proposed voltage-mode downconverter (RX-RFFE) is presented in Figure 106, featuring a millimeter-Wave front end in blue, and a baseband analog section in green. The RX-RFFE is supposed to downconvert the millimeter-Wave signal with minimal impacts on linearity and SNR. The analog chain processes the baseband IF signal by filtering the bumper jammer and by increasing the voltage level. The first section details the analog signal processing, especially for the first high pass filter and the variable gain amplifier ($HPF\text{-}VGA_0$). The second section studies the behavior of the voltage mode mixer and the implementation of the RF amplifiers.

a. Baseband analog signal processing

Before the analog to digital conversion by the ADC block, the radar signal is expected to present a large dynamic range with a high SNR and, obviously, no jammer susceptible to corrupt the digital signal processing. As detailed in Chapter I, the trade-off between gain, noise and linearity performance is tough in the demodulation chain. For this reason, the constraints on the analog chain are discussed, and the design of the first baseband stages, a high pass filter (HPF) and a low noise baseband amplifier (VGA_0), is detailed.

Due to the bumper reflection of the transmitted signal, typically around -5dBm, the linearity of the complete chain is critical since this jammer cannot be filtered in the RF domain.

To address a high level of linearity (CP1), the RX-RFFE usually presents a poor gain, typically around 10dB. In baseband, this jammer results in a $0.6V_{rms}$ signal at only 20kHz, which is far below the IF signal band. Hence the jammer signal is attenuated by several high-pass filters, with a cutoff frequency of typically 400kHz, distributed in the base-band section. The filters allow to relax the ICP1 specification to -20dBm, $140mV_{rms}$, in the IF band -i.e. from 2 MHz to 40MHz.

Table 22 – Performances of the baseband analog blocks HPF-VGA

Parameters		HPF-VGA$_0$	HPF-VGA1	HPF-VGA2
Conv. gain (dB)		10	22	10
Noise (V/√Hz)		3	10	50
ICP1 (V_{rms})	@20kHz	0.57	0.57	/
	@10MHz	0.14	0.45	/

To properly process the signal, a dynamic range of 20 dB is needed with specific constraints on linearity. Due to this trade-off, the two cascaded VGA usually presents a high noise contribution as reported in Table 22. Thereby, a third low noise HPF-VGA (HPF-VGA$_0$) is added before HPF-VGA$_1$ and HPF-VGA$_2$. As described in Table 22, it is designed to minimize the impact on analog chain noise with a reduced noise contribution of 3nV/√Hz and a moderate gain of 10dB.

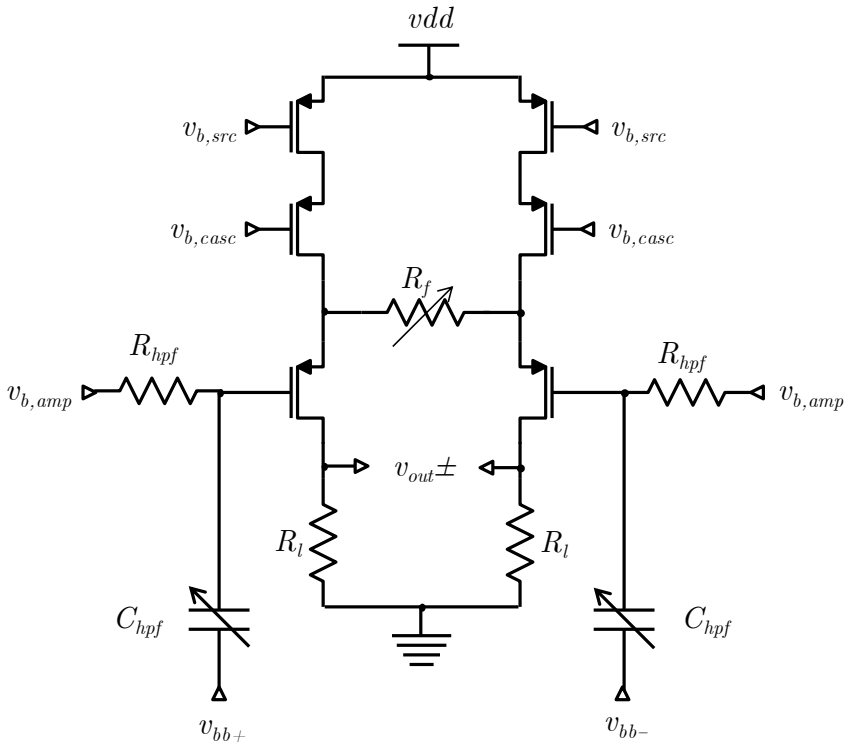


Figure 107 – Schematic of a Variable gain amplifier including high-pass filter

Figure 107 proposes the schematic of the cascaded high-pass filter with the baseband low noise amplifier VGA$_0$. The first order high pass filter features a 15pF capacitor (C_{hpf}) and a resistor (R_{hpf}) of 24.4kΩ, also used for gate biasing. For the baseband amplifier, a PMOS amplification (M_p) is selected to minimize the amplifier noise, the channel length is closed to 600nm to reduce the flicker noise contribution. For the DC current sources, a cascode approach is preferred to maximize the output impedance and recopy. The gain of the amplifier is set by the ratio between the load resistor (R_L) and the feedback resistor (R_f). This feedback resistor is tunable to adjust the gain considering the various use cases. The amplifier consumes 5.7mW with a 1.5V supply voltage.

The HPF-VGA$_0$ is simulated in schematic and has not been implemented in the test vehicle. In Figure 108(a), a flat-band 10 dB gain is achieved from 2 to 100MHz, with an attenuation of 15dB at 20kHz. The bumper blocker is located at a frequency typically below 50kHz, the amplifier exhibits in this low band a high compression point, above +1.8V$_{rms}$, Figure 108(b). This performance allows the baseband section to address the overall linearity specification. Regarding the noise performance, Figure 108(c), a typical noise of 2nV/√Hz is achieved in the IF band, rising to 3 nV/√Hz in the worst hot case. The noise corner frequency of the proposed amplifier remains below 1MHz which does not impact the SNR of the IF signal.

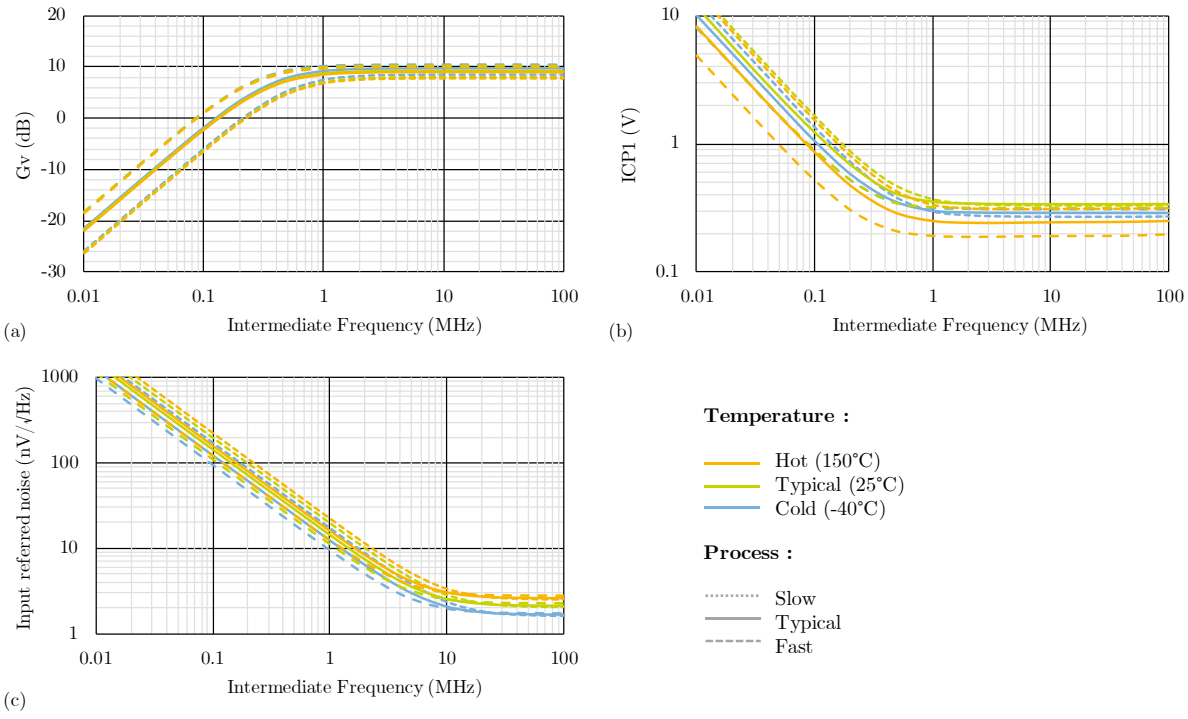


Figure 108 – Simulations of the baseband amplifier with (a) conversion gain in dB; (b) compression point in V; (c) input referred noise (nV/√Hz)

b. Millimeter-Wave Voltage-mode Front-End

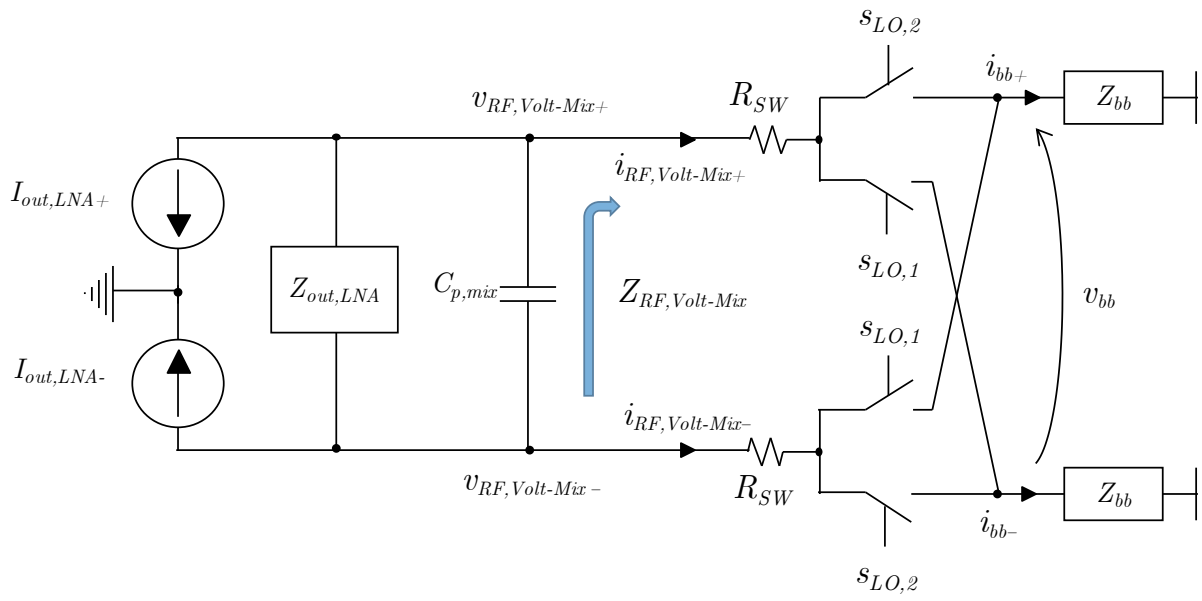


Figure 109 – Modelling of voltage mode mixing including a low noise amplifier output

Considering the analog demodulation chain detailed in the previous section, we now focus on the millimeter-Wave front end with the mixer centered model proposed in Figure 109. The amplifier HPF-VGA$_0$ presents a high input impedance Z_{bb} at the IF port, at the input RF port the LNA is modeled by a current source with an impedance $Z_{out,LNA}$. According Equation 69, the input impedance of the mixer is dominated by the up-conversion of the baseband impedance Z_{bb} which can be simplified to Equation 70. Due to parasitic capacitances ($C_{p,mix}$), not considered in the mixer modelling proposed in the section I, the input impedance of the voltage mode mixer is modified. To compensate for it a transformer, which also acts as DC block, is used to transfer the RF signal from the LNA to the mixer.

Equation 70 – Approximation of input RF impedance of voltage mode mixer

$$Z_{RF,Volt-Mix}(\omega_{RF}) \approx |a_1|^2 \cdot \left(Z_{bb}(\omega_{RF} - \omega_{LO}) + Z_{bb}(\omega_{RF} + \omega_{LO})\right) \;//\; \frac{1}{jC_{p,mix}\omega_{RF}}$$

As long as the input impedance of the mixer and the output impedance of the LNA are real and almost equivalent, the transmission loss of the RF signal from the LNA to the mixer can be determined by $Z_{RF,volt-mix}$ and $Z_{out,LNA}$, Equation 71. Hence the ratio between $Z_{out,LNA}$ and $Z_{RF,Volt-Mix}$ affects the conversion gain and, consequently, the linearity of the mixer. If the mixer input voltage is to large, or the output impedance of the LNA is to low, the non-linearities of the mixer will affect the 1dB compression point.

Equation 71 – Input RF voltage and current in the mixer considering an output load for LNA

$$I_{RF,Volt-Mix}(\omega_{RF}) = \frac{I_{out,LNA}(\omega_{RF})}{1 + \frac{|a_1|^2 \cdot \left(Z_{bb}(\omega_{RF} - \omega_{LO}) + Z_{bb}(\omega_{RF} + \omega_{LO})\right)}{Z_{out,LNA}(\omega_{RF})}}$$

$$V_{RF,Volt-Mix}(\omega_{RF}) = I_{out,LNA}(\omega_{RF}) \cdot (Z_{out,LNA}(\omega_{RF}) \;//\; Z_{RF,Volt-Mix}(\omega_{RF}))$$

The development of the LNA is based on the C4 topology presented in the Chapter 3.III. It is designed to simultaneously achieve a sufficient linearity, ICP1, to handle bumper reflection, to perform a low noise figure and a sufficient gain to attenuate the noise contribution of the following stages. The gain of the LNA would still be limited to avoid the mixer saturation.

To drive the mixer a buffer stage is added on the LO path to hard switch the transistors. This buffer is based on C4 topology designed to achieve more than 8dB voltage gain, and a low output impedance. This LO driver is supplied by a 1.5 V and consumes 13mW, considering a 0dBm input LO power.

2. Post layout simulations

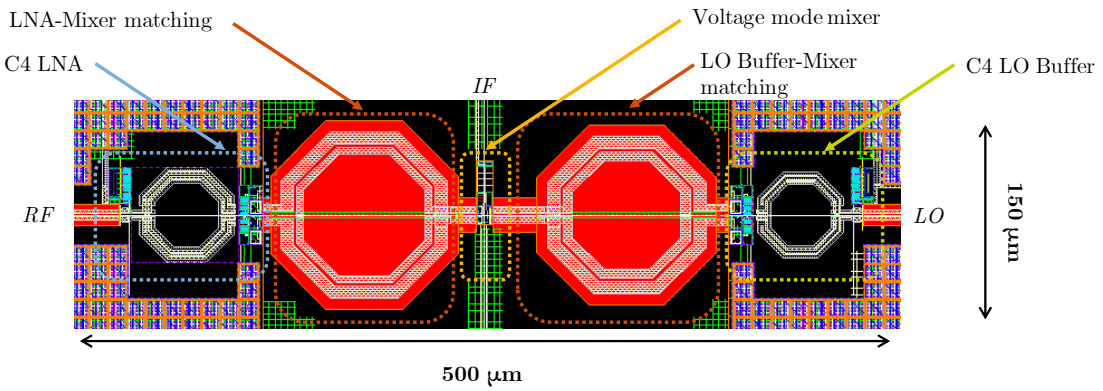


Figure 110 – Layout of the millimeter-Wave front-end of the proposed voltage-mode downconverter

Based on the analysis of the previous section, a complete RX-RFFE has been designed in 28nm CMOS technology. The millimeter-Wave part has been implemented but is not yet measured, for this reason only post-layout simulations are reported herein after. These results include the process and temperature variations to which the circuit is the most sensitive, the voltage supply variations have been also evaluated but they have a minor impact on the performance. As discussed previously, baseband blocks are included in schematic to the simulation. Figure 110 presents the layout of the millimeter-Wave part of the circuit, the silicon footprint is only 0.06mm^2. The overall footprint is estimated 0.09mm^2 including baseband. The nominal voltage is set to 1.5V for all blocks and leads to an overall DC consumption of 18mW including the LO buffer.

(1) Input matching

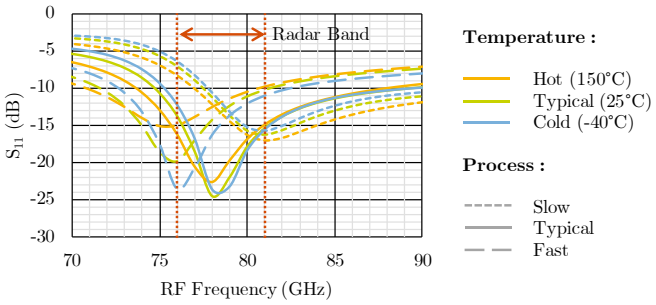


Figure 111 – Input matching (S11) in dB in process and temperature variations

Over the RADAR band the input matching, Figure 111, achieves a return loss lower than -8dB in any case. However, we observe an important variation of the central frequency of the return loss leading to a moderate robustness to PVT variations. This issue is due to both the impact of the mixer impedance on the LNA input impedance, discussed in section 2, and the sensitivity of the transformer and the LNA input to parasitics.

(2) Conversion gain

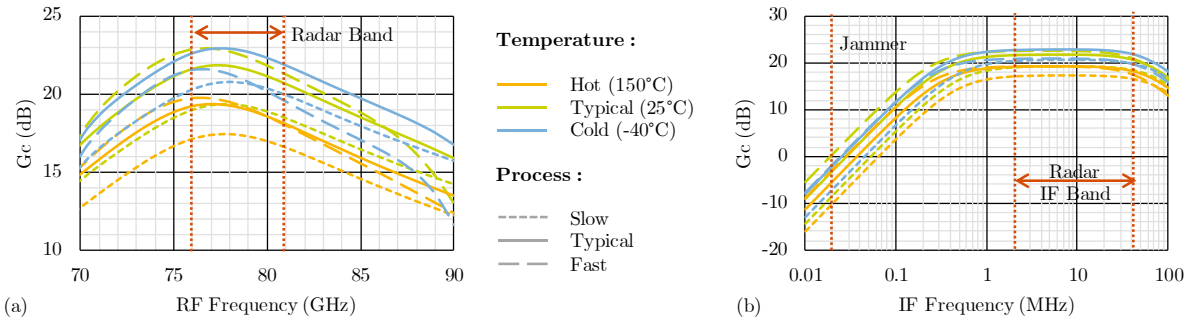


Figure 112 – Conversion gain (Gc) in dB in process and temperature variations: (a) in RF band (76-81GHz) for a 10MHz IF; (b) in IF band (10kHz-100MHz) for a 78.5GHz

The post-layout simulations of conversion gain are proposed in process and temperature corners. This voltage-based down-converter reaches a high conversion gain with a nominal gain of 22dB, Figure 112(a), which is sufficient to reduce the noise impact of the baseband analog blocks. Thanks to the common-gate based topology, a wide -3dB bandwidth is achieved, from 73 to 84GHz, with a ripple of only -1dB in the radar band. Still the process and temperature corners leads to important variations on conversion gain, it is reduced to 16dB in the worst case. Nevertheless, it does not impact the functionality of the downconverter regarding the application. Regarding the IF band from 2MHz to 40MHz, the conversion gain is almost flat in any case as shown in Figure 112(b). At 20kHz, the bumper reflected jammer is not amplified by the downconverter and would not disturb the signal processing.

(3) Noise figure

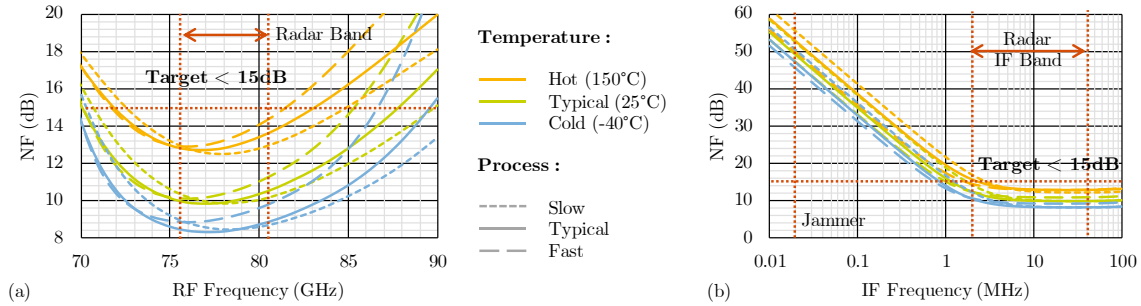


Figure 113 – Noise figure (NF) in dB in process and temperature variations: (a) in RF band (76-81GHz) for a 10MHz IF; (b) in IF band (10kHz-100MHz) for a 78.5GHz

For noise characterization, the down-converter is first simulated, Figure 113(a), at a fixed IF with the RF frequency ranging from 70 to 90GHz. In typical case, the RFFE achieves a nominal NF of 10dB. The temperature has an important impact on the minimal noise figure with a ±3dB variation. For the second kind of simulations the RF frequency is fixed to 78.5GHz, the middle of the RADAR band, and the IF band is swept by varying the LO frequency. The Noise Figure, Figure 113(b), is almost flat on the signal bandwidth from 2MHz to 40MHz. In conclusion, the downconverter noise figure is suitable for long range radar applications.

(4) Linearity

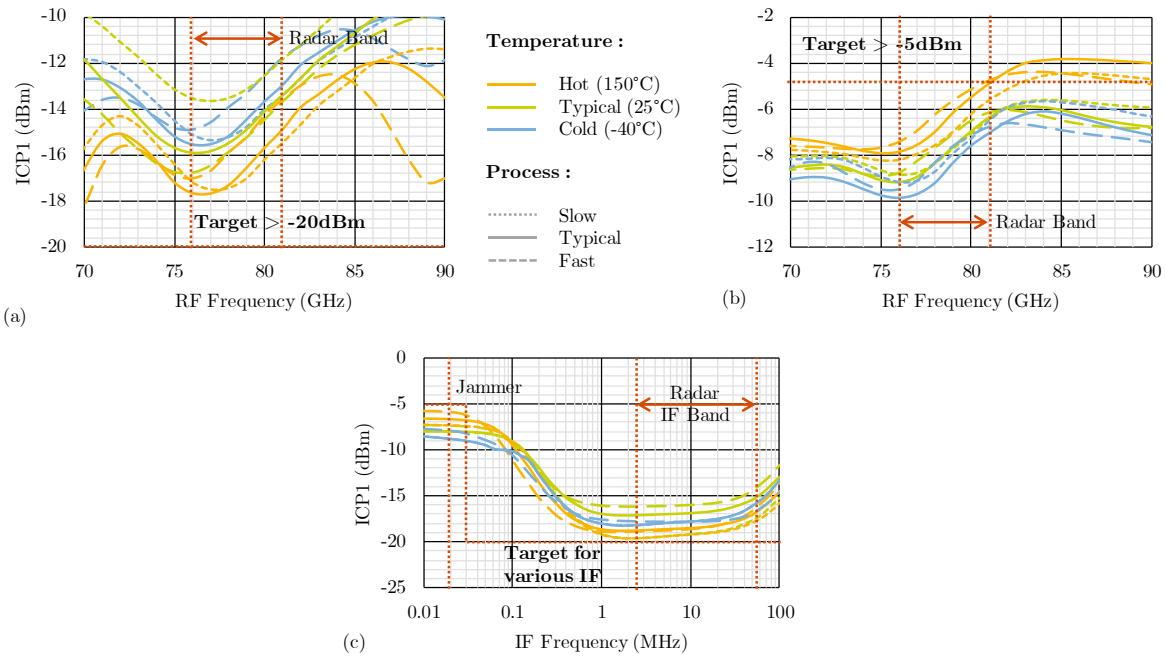


Figure 114 – 1dB compression point (ICP1) in dBm in process and temperature variations: (a) in RF band (76-81GHz) for a 10MHz IF; (b) in RF band (76-81GHz) for a 20kHz band; (c) in IF band (10kHz-100MHz) for a 78.5GHz

For linearity, two cases are considered for the specifications defined in Chapter I. The first one concerns the impact of the targets, corresponding to an IF of 2MHz to 40MHz, the ICP1 specification is fixed to -20dBm. In Figure 114(a), the simulations of the ICP1 shows a linearity higher than -18dBm which is compatible with the specification. The second case is for the bumper reflection, corresponding to a low IF of typically 20kHz and a specification of -5dBm, Figure 114(b). The ICP1 is below -5dBm with a minimum of value close to -10dBm at the lower bound of the RADAR band. This performance is not compatible with the automotive radar use cases. Regarding the IF frequency, in Figure 114(c), the linearity in the target IF band is sufficient over the 2MHz to 40MHz bandwidth.

3. Conclusion

This last chapter investigates on the development of an RX Front-End for automotive radar for LRR solutions capable of managing blockers due to bumper reflection, and minimizing noise to extend the radar range. Hence the downconverter must achieve simultaneously a low noise figure, a high linearity (ICP1) and a large conversion gain. A voltage-mode downconverter is first proposed. Its mm-Waves section features a single stage LNA and a passive mixer. The LNA is based on a complementary capacitor cross-coupled topology to maximize the trade-off between the noise performance, the linearity and the power consumption. The passive mixer

operates in voltage-mode to down-convert the RF voltage to baseband. The first stage of the baseband section, combining a high-pass filter and a base-band low noise amplifier, is also designed. The topology of the base-band VGA is a PMOS pseudo-differential pair to reduce the noise contribution, with a resistive degeneration to improve the linearity.

Table 23 – Simulations of Voltage-mode RX in typical, best and worst cases

Parameters		Specification	RX (Typical)	RX (Hot/Slow)	RX (Cold/Fast)
VDD (V)		/	1.5	1.5	1.5
Bandwidth (GHz)		76-81	75-89	77-90	73-82
Conv. Gain (dB)	@IF=10MHz	> 15	20.3	15.5	22
Noise figure (dB)	@IF=1MHz	/	16	21	14
	@IF=10MHz	< 15	10.1	15	8.1
ICP1 (dBm)	@IF=20kHz	> -20	-9.1	-7.1	-9.8
	@IF=10MHz	> -5	-15.2	-13.6	-17.6
Area (mm^2)		/	0.09	0.09	0.09
Power consumption (mW)		/	18	18	18

The performances of the RX-RFFE are summarized in Table 23. This front end achieves a noise figure below 14dB and a conversion gain higher than 15.5dB in any case. These performances are included in the system model presented in chapter I to evaluate the RADAR performance, the TX section combines two transmitters achieving a +15dBm overall output power. Considering various target types, the proposed downconverter achieves a proper detection distance of more than 50 meters for pedestrians, 100 meters for bikes, 200 meters for cars and 1 km for trucks which is compatible with a long-range application. Nevertheless, voltage-mode mixing involves two limitations. First, the high real input impedance of the mixer is significantly impacted by parasitic capacitances leading to a reduced, and sliding, bandwidth in PVT corners. Secondly, the voltage mixing operation significantly impacts the linearity of the overall demodulator, leading to an ICP1 below -5dBm which is not compatible with radar specifications. The next section focuses on the RFFE design to address this issue.

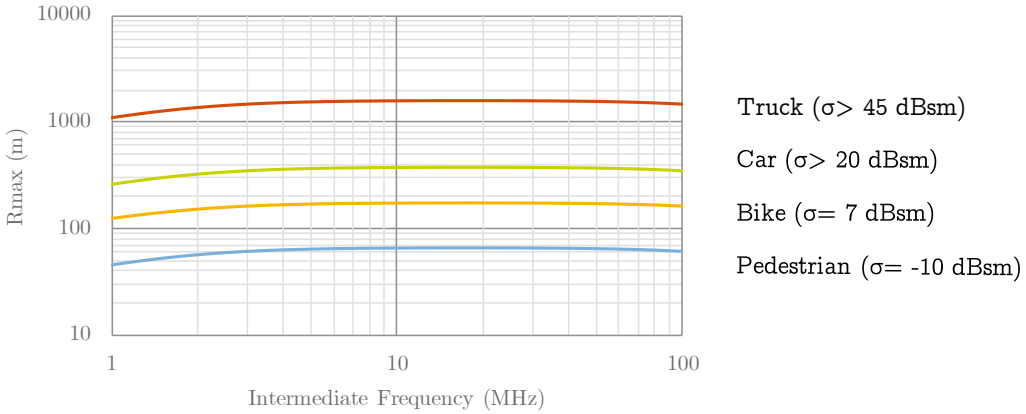


Figure 115 – Maximal range regarding the Intermediate Frequency for various targets in the worst case

III. Current mode downconverter

Regarding the inherent limitations of voltage mode mixer to implement a highly linear low noise RX-RFFE, a current mode mixer is identified as a promising solution. Driving lower impedance, the current mode operation exhibits reduced voltage swing preventing from transistor clipping, and extended bandwidth. In this section, the demodulation chain featuring a current-mode mixer is presented with details on each block, then the post-layout simulations are proposed for this RX-RFFE. The performances are finally discussed at system level with respect to SRR and LRR applications.

1. Demodulation chain

Presented in Figure 116, the current-mode downconverter features an RF section in blue and an analog section in green. The constraints on each part are similar to the voltage mode RX-RFFE. In a first section, a discussion between current and voltage analog processing is proposed leading to the design of the TransImpedance Amplifier (*TIA*). Some analysis is then proposed for the current-mode millimeter-Wave front-end which downconverts the radar signal with a limited impact on the radar linearity while maintaining a high SNR.

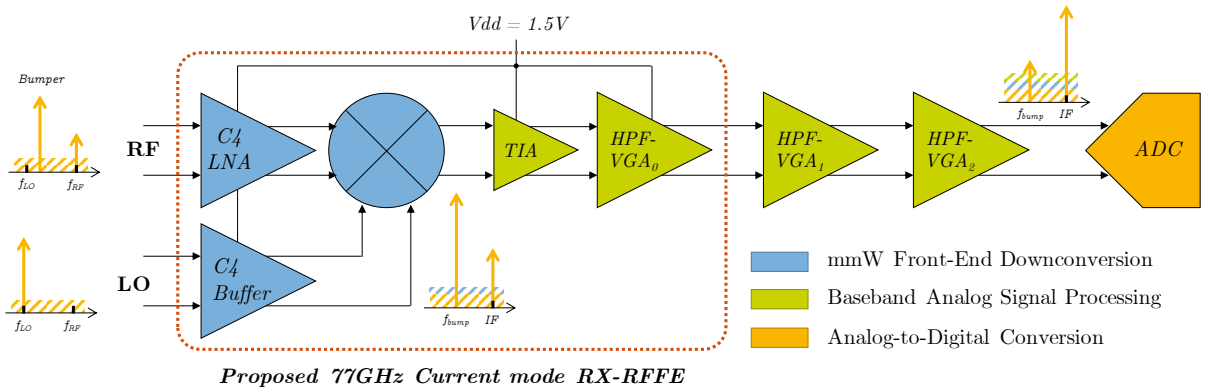


Figure 116 – Proposed Current-mode downconverter in a complete demodulation chain

a. Baseband analog signal processing

Usually, in digital communications, current mode architectures require current mode amplifiers and ADC baseband signal processing. Involving low impedance, both the bandwidth and the linearity improve. As consequences, the filtering of low frequency blockers necessitates to significantly increase the capacitor value to maintain the cut-off frequency with a lower impedance. For this reason, voltage mode analog blocks are still preferred and the HPF-VGA, presented in section II.1.a, are reused. Still a TIA is necessary to convert the IF baseband current to voltage at the output of the mixer.

As the filtering of the bumper blocker is performed in the following VGAs, the TIA must achieve a high linearity. Besides the TIA is cascaded with the conventional baseband analog processing, its noise contribution should be reduced to avoid an increase of the overall noise figure. This trade-off between noise and linearity is critical in the implementation of the current-mode downconverter.

The TIA, Figure 117, is based on a common-gate topology. If the output impedance of the current source is assumed high, the input impedance is then dominated by the common-gate transconductance and is closed to $2/g_{m,CG}$. The input current is then converted in a voltage through the load resistor (Rl) which determines the overall transconductance value. A 450Ω resistor is selected to maximize the conversion gain of the overall front-end. To achieve an overall ICP1 of -5dBm for the entire RX-RFFE, the voltage swing allowed across the load resistor and the common-gate transistor would be at least 600mV. The DC current source is then sized to maintain the linearity and the input impedance of the circuit. The TIA consumes 4mW with a supply voltage of 1.5V.

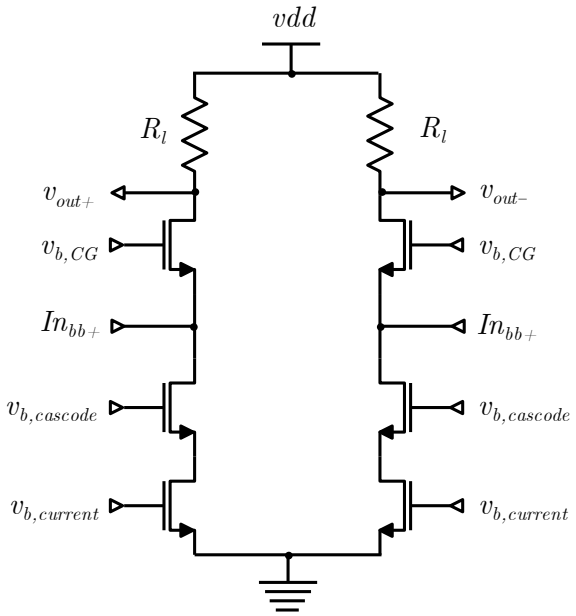


Figure 117 – Schematic of a Trans Impedance Amplifier

The performances of the TIA are simulated in schematic and presented in Figure 118. The transimpedance gain, Figure 118(a), presents a nominal value close to 450Ω and exhibits a +/- 15% variations to the process corners, which can be compensated on chip. The 1dB compression point, Figure 118(b), is higher than 3.5mA which addresses the system specifications. Finally, the input referred noise, Figure 118(c), is below 1nV/√Hz over the IF bandwidth, this performance does not affect the overall RFFE noise figure.

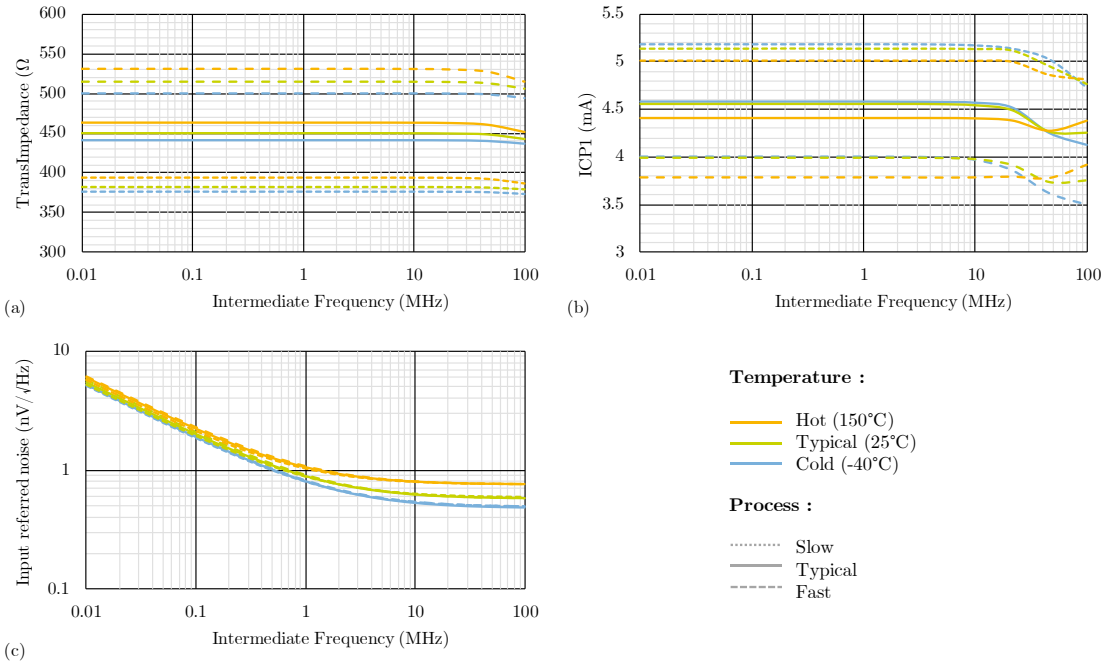


Figure 118 – Simulations of the baseband TIA with (a) TransImpedance in Ω; (b) 1dB compression point in mA; (c) input referred noise (nV/√Hz)

b. Millimeter-Wave Current mode front-end

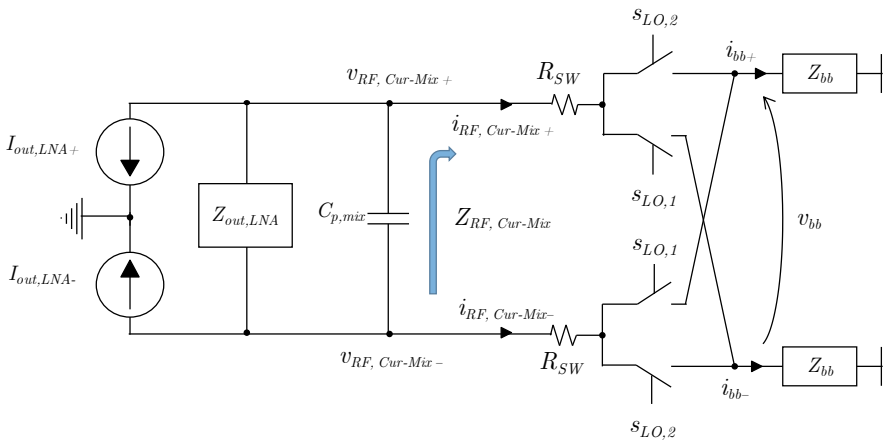


Figure 119 – Modelling of current mode mixing including a low noise amplifier output

A mixer centered model of the mm-Waves RX-RFFE (downconverter) is proposed in Figure 119. Since the modeling of the mixing operation is the same for voltage or current mode, we directly provide the final expression in this sub-section.

The input impedance of the mixer, $Z_{RF,cur\text{-}Mix}$, is given in Equation 72. It is dominated by the switch on resistance R_{sw} since the TIA exhibits a low Z_{bb} input resistance. As the input impedance of the mixer is low, the current mode operation is less sensitive to parasitic capacitances ($C_{p,mix}$) and the output impedance of the LNTA ($Z_{out,LNA}$). It allows for a larger bandwidth. A transformer is still implemented to ensure the transfer of the RF signal from the LNA to the current mixer with DC blocking.

Equation 72 – Approximation of input RF impedance of current mode mixer

$$Z_{RF,Cur-Mix}(\omega_{RF}) \approx 2R_{sw} + |a_1|^2 \cdot \left(Z_{bb}(\omega_{RF} - \omega_{LO}) + Z_{bb}(\omega_{RF} + \omega_{LO})\right)$$

If we assume the low noise (transconductance) amplifier exhibits a large output impedance $Z_{out,LNA}$ compared to $Z_{RF,Cur\text{-}Mix}$, most of the current $I_{out,LNA}$ flows into the mixer which maximizes the signal transfer. Interestingly the RF voltage swing $V_{RF,Cur\text{-}Mix}$ remains small due to the low value of $Z_{RF,Cur\text{-}Mix}$, thus the downconverter linearity is larger in the current mode than in the voltage mode. To drive the mixer the same buffer stage implemented in the voltage mode mixer is added on the LO path.

Equation 73 – Input RF voltage and current in the mixer considering an output load for LNA

$$I_{RF,Cur-Mix}(\omega_{RF}) = \frac{I_{out,LNA}(\omega_{RF}) \times Z_{out,LNA}}{\left[2R_{sw} + |a_1|^2 \cdot \left(Z_{bb}(\omega_{RF} - \omega_{LO}) + Z_{bb}(\omega_{RF} + \omega_{LO})\right)\right] + Z_{out,LNA}}$$

$$V_{RF,Cur-Mix}(\omega_{RF}) \approx I_{out,LNA}(\omega_{RF}) \cdot Z_{RF,Volt-Mix}(\omega_{RF})$$

2. Post-layout simulations

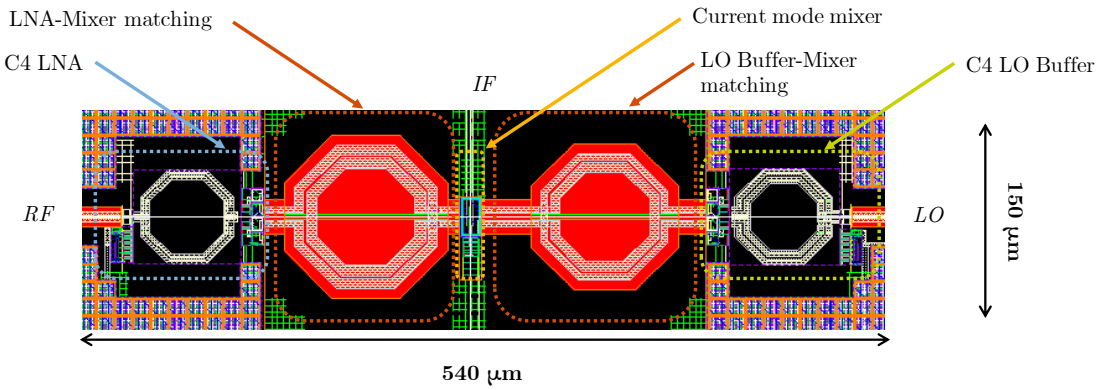


Figure 120 – Layout of the millimeter-Wave front-end of the proposed current-mode downconverter

A receiver front-end featuring the architecture proposed in Figure 116 has been implemented in 28nm CMOS technology. As the measurements have not been performed, only the post-layout simulations are proposed including process and temperature corners. As discussed previously, baseband blocks are included in schematic to the simulation. The layout of the millimeter-Wave front-end is shown in Figure 120, the silicon footprint is 0.08mm². If we including the analog TIA and the HPF-VGA$_0$, the overall area is estimated 0.14mm². The DC consumption is limited to 23mW for a supply voltage of 1.5V including the LO buffer.

(1) Input matching

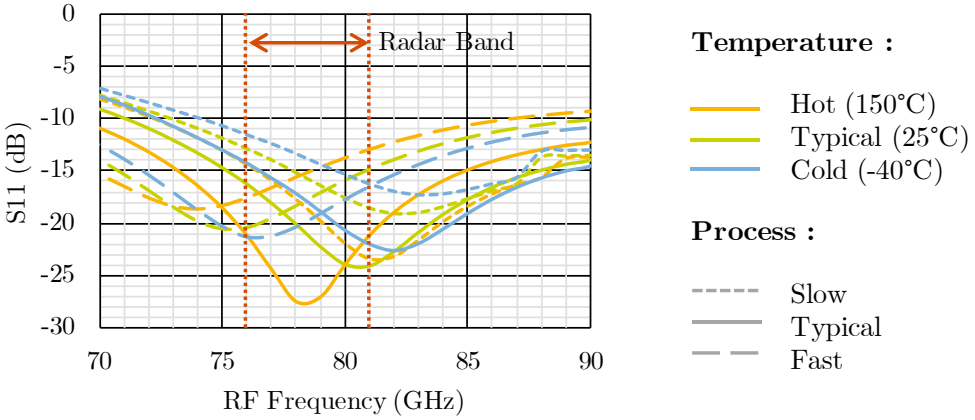


Figure 121 – Input matching (S11) in dB in process and temperature variations

The downconverter exhibits a wideband input matching as shown in Figure 121. As discussed previously, the current-mode mixer presents a low impedance over a large bandwidth with a reduced sensitivity to parasitic capacitances. Due to this low impedance, the input impedance of the RX-RFFE is dominated by the equivalent transconductance of the C4 LNA controlled by a current source. The current steering of the input impedance allows for a better

immunity to PVT variations as illustrated in Figure 121. The Rx-RFFE achieves a wideband input matching in any case of process and temperature corners, and a return loss lower than -12dB in the RADAR Band.

(2) Conversion gain

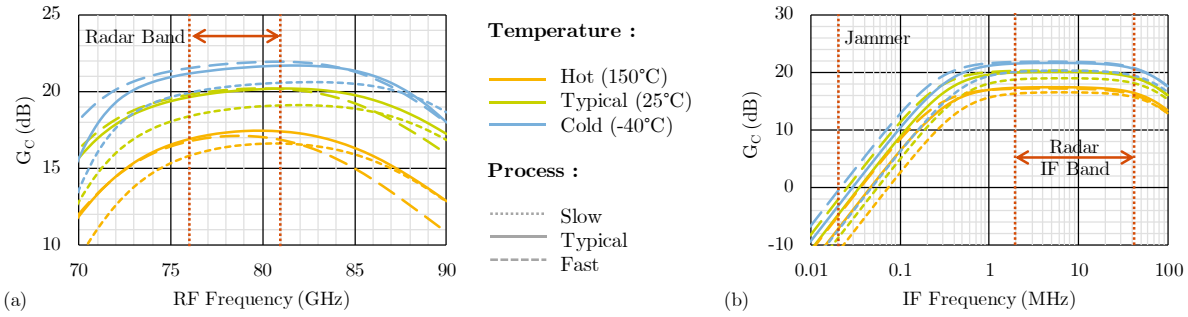


Figure 122 – Conversion gain (Gc) in dB in process and temperature variations: (a) in RF band (76-81GHz) for a 10MHz IF; (b) in IF band (10kHz-100MHz) for a 78.5GHz

Regarding RF frequency, Figure 122(a), the conversion gain exhibits a high nominal value, close to 20dB, with a ±4dB variation in corners. Compared to the voltage-mode front-end, it is flatter over the radar band with a ripple of only 0.5dB instead of 1dB. In typical case, the -3dB bandwidth covers from 73 to 90 GHz. Regarding the intermediate frequency, Figure 122(b), the front-end presents a flat conversion gain in the IF band, with a good rejection of the bumper blocker at 20kHz. As expected, the conversion gain presents a large bandwidth with an interesting immunity to corner variations.

(3) Noise Figure

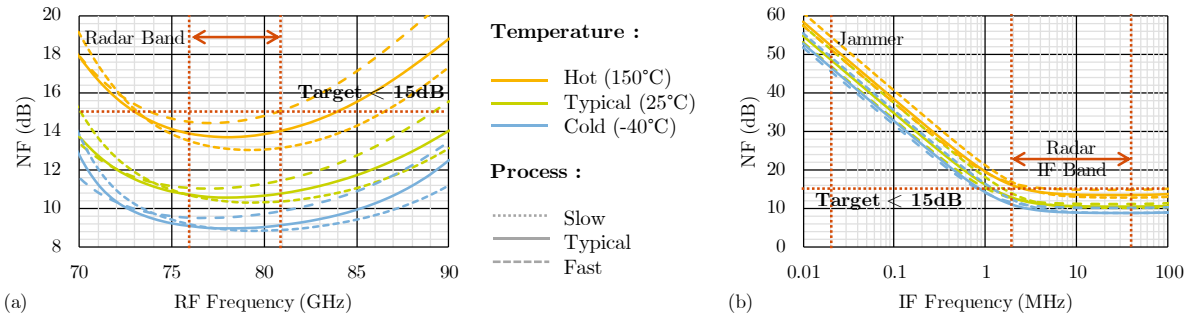


Figure 123 – Noise figure (NF) in dB in process and temperature variations: (a) in RF band (76-81GHz) for a 10MHz IF; (b) in IF band (10kHz-100MHz) for a 78.5GHz

In Figure 123, the post-layout simulations of the noise figure are proposed with process and temperature variations. The noise figure, Figure 123(a), exhibits a typical value of 11dB with a significant variation of respectively +3.5dB and -2 dB, in the hot case and in the cold case. Interestingly it presents a limited rippled of +0.5dB over the RADAR band. In the 2-

40MHz IF band, Figure 123(b), the noise figure is almost flat. Compared to the voltage mode down-converter, the current mode operation achieves a slightly higher noise figure (+0.5dB) due to the noise contribution of the base-band TransImpedance Amplifier.

(4) Linearity

In Figure 124(a), the compression point is presented in the RF band with a fixed IF of 2MHz. It is higher than -18dBm in any case thus addressing the specification. For the bumper jammer case the ICP1 is simulated at a fixed IF of 20kHz, Figure 124(b), it is above the specification of -5dBm in any case. Regarding the IF band, Figure 124(c), the compression point is stable over the IF band.

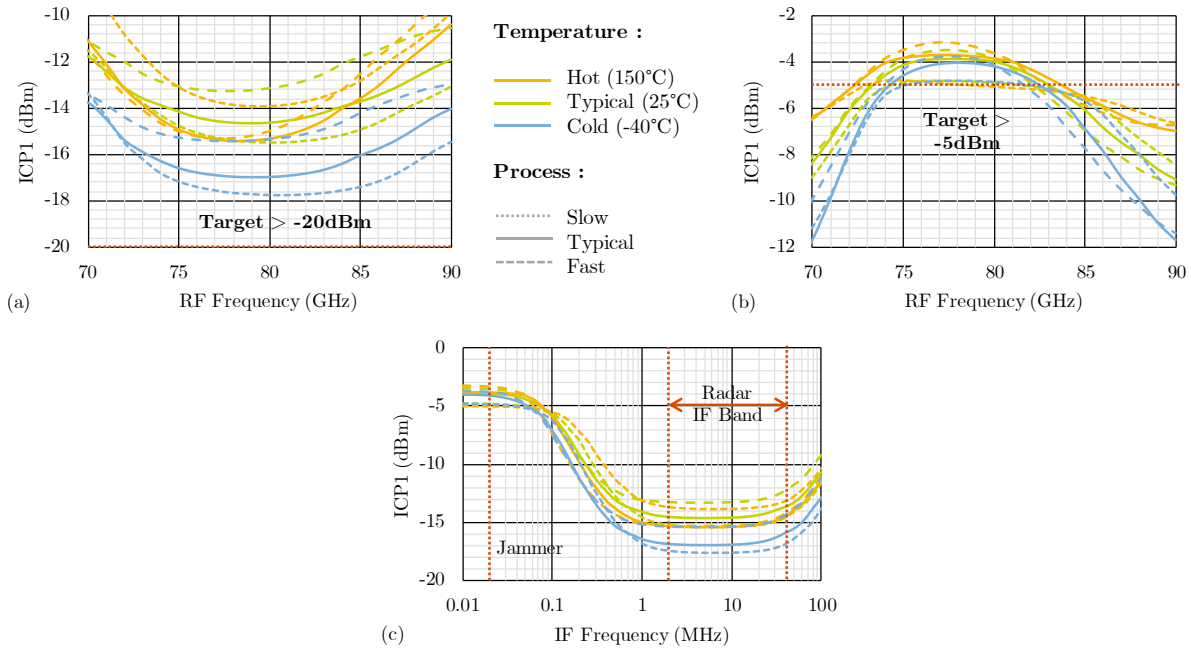


Figure 124 – 1dB compression point (ICP1) in dBm in process and temperature variations: (a) in RF band (76-81GHz) for a 10MHz IF; (b) in RF band (76-81GHz) for a 20kHz band; (c) in IF band (10kHz-100MHz) for a 78.5GHz

3. Conclusion

In this section, a RX Front-End based on current-mode mixing is proposed. The millimeter-Wave part uses two C4 amplifiers for low noise transconductance amplification and LO buffering. The current-mode mixer downconverts the RF signal with a high linearity. In the analog section, two stages are also implemented; a TransImpedance Amplifier to convert the baseband current into voltage, and a HPF-VGA$_0$ to filter the 20kHz jammer and to increase the dynamic of the signal.

Table 24 – Simulations of Current-mode RX in typical, best and worst cases

Parameters		Specification	RX (Typical)	RX (Hot/Slow)	RX (Cold/Fast)
VDD (V)		/	1.5	1.5	1.5
Bandwidth (GHz)		76-81	71-90	72-90	70-90
Conv. Gain (dB)	@IF=10MHz	> 15	20	16	22
Noise figure (dB)	@IF=1MHz	/	16.5	20	14
	@IF=10MHz	< 15	11	15.5	9
ICP1 (dBm)	@IF=20kHz	> -20	-4	-3	-5
	@IF=10MHz	> -5	-15	-15	-18
Area (mm^2)		/	0.12	0.12	0.12
Power consumption (mW)		/	23	23	23

The performance of the current mode RX-RFFE are summarized in Table 23. This front end achieves a noise figure below 15.5dB, a conversion gain higher than 15.5dB and an ICP1 above -5dBm in any case. These performances are included in the system model presented in chapter I to evaluate the RADAR performance, the TX section combines two transmitters achieving a +15dBm overall output power. Considering various target types, the current-mode and voltage mode downconverters achieve equivalent performance compatible with long-range detection as presented in Figure 125. Unlike the voltage mode RX-RFFE the current mode RX-RFFE is capable of handling bumper reflection by addressing the linearity specification. It is also important to note the current-mode RX-RFFE achieves robustness to PVT variations and a larger bandwidth.

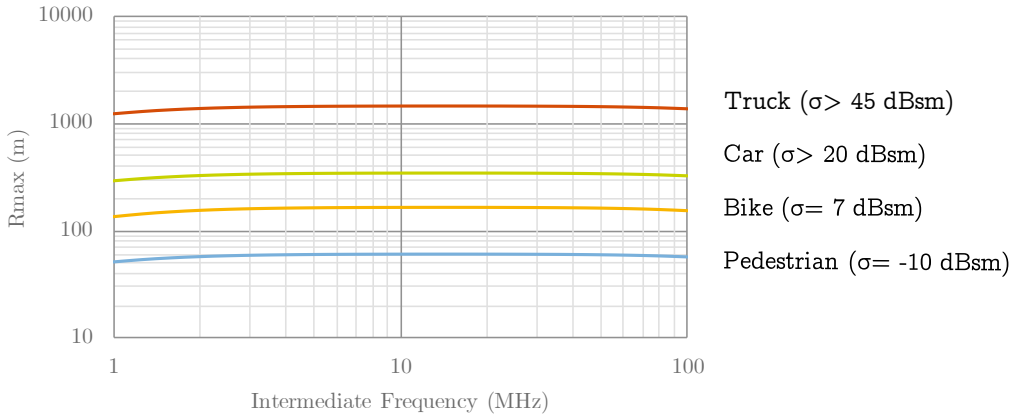


Figure 125 – Maximal range regarding the Intermediate Frequency for various targets in the worst case

IV. Conclusion

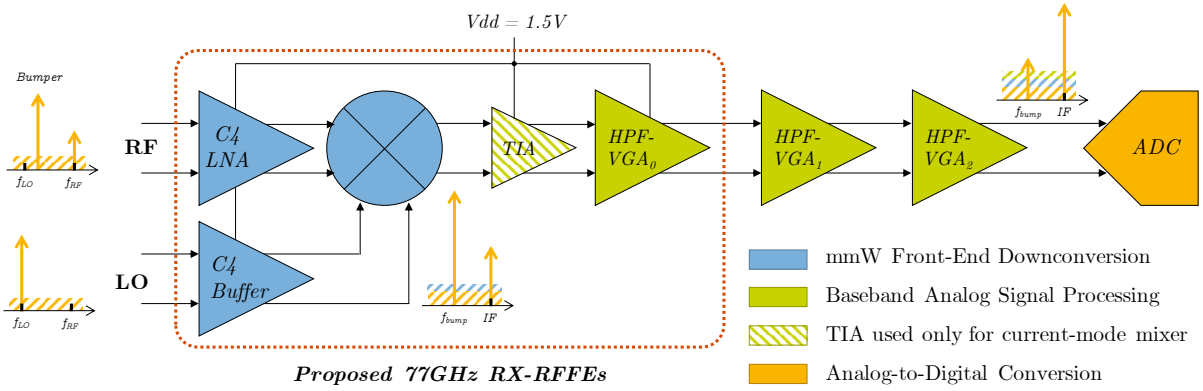


Figure 126 – Proposed downconverters in a complete RX-RFFE including a baseband TIA used only in current-mode downconverters

Considering the various radar use cases, the system analysis proposed in Chapter I brings two main constraints on RX-RFFE. First, the presence of the radar antennas behind the bumper leads to an important reflection of transmitted signal thus affecting the receiver linearity. This situation requires a high linearity with a -1dB compression point above -5dBm. Long range radars also need to minimize the noise contribution of the complete demodulation chain to perform a high level of detection. Considering the typical noise values of baseband blocks, detailed in Table 25, and characteristics of ADC, the RX Front End must present a high conversion gain, typically higher than 15dB, and a low noise figure, below 16dB. These tough requirements lead us to investigate on new architectures.

Table 25 – Summary of performance requirements for the various blocks of the demodulation chain

Parameters		mmW Front-End (including HPF-VGA0 if needed)	VGA1 & HPF1	VGA2 & HPF2
Gain (dB)		10	22	10
NF (dB)		15	/	/
Noise (nV/√Hz)		/	10	50
ICP1	@20kHz	-5 dBm	0.57 V_{RMS}	/
	@10MHz	-20 dBm	0.45 V_{RMS}	/

For the low noise amplifier stage, the Chapter III highlights the advantages of the Complementary Capacitor Cross-Coupled topology. Due to the constraints on linearity, the LNA features only a single stage but differential topology. This C4 architecture achieves a good trade-off between performance and power consumption. In the worst case of PVT corners, the noise figure remains below 7dB and the ICP1 exceeds -5dBm, which makes it compatible with radar specifications.

The present Chapter focuses on the design of an RX-RFFE based on passive-mixer combined with a C4-LNA at 77GHz. A comparison between voltage and current mode downconversion is performed, Figure 126. The critical building blocks of the base-band section are also designed and implemented. The two RX-RFFE include high-pass filters (HPF) and VGAs to filter out jammers induced by bumper reflections, and to match the signal dynamic. In the current-mode downconverter, a TransImpedance Amplifier is also developed to convert the baseband current into voltage further processed by HPF-VGA blocks.

Equation 74 – Figures of merit defined

$$FOMI = \frac{G_C \cdot ICP1_{20kHz}}{(F-1) \cdot P_{DC}} \quad ; \quad FOMII = \frac{G_C \cdot ICP1_{20kHz}}{(F-1) \cdot P_{DC} \cdot Area}$$

The post-layout simulations, for typical case, of the two developed downconverters are summarized in Table 26 and compared to the state-of-the-art. Two figures of merit are proposed to compare these circuits: FOMI only accounts for noise, gain, linearity and power consumption, and FOMII includes the silicon footprint. The two proposed circuits present an interesting trade-off between noise and compression point. The current mode RX-RFFE achieves the best FOMI. With a moderate constrain on linearity, conventional architectures achieve lower noise figure and a large conversion gain. Regarding FOMII, the proposed circuits compares favorably with the state-of-the-art except [54] which has a reduced silicon footprint.

Table 26 – State of the art of millimeter-Wave RX Front-End compared to post-layout simulations of the designed RX Front-End for automotive radar applications in typical case (including pads)*

Parameters		[43]	[55]	[56]	[54]	This work (Voltage)	This work (Current)
Results		Meas.	Meas.	Meas.	Meas.	Post-layout sim.	Post-layout sim.
Tech. (nm)		CMOS 40 nm	CMOS 65nm	CMOS 40nm	CMOS 45nm	CMOS 28nm	CMOS 28nm
VDD (V)		1.1	1	1.1	1.1	1.5	1.5
Frequency (GHz)		77	77	60	60	77	77
Bandwidth (GHz)		/	5	10	9	14	19
Gain (dB)		30.8	11	30	26	20.3	20
NF (dB)	@1MHz	/	/	/	/	16	16.5
	@10MHz	9	8	5.5	6	10.1	13.1
ICP1 (dBm)	@20kHz	-22.3	-15	-31	-22.5	-9.1	-5
	@10MHz					-15	-15.5
Power (mW)		143	22	35	21	18	23
Area (mm^2)		0.8*	0.231	0.7*	0.023	0.09	0.12
FOMI		0.0002	0.001	0.0003	0.002	0.008	0.012
FOMII		0.0003	0.004	0.0004	0.078	0.085	0.01

Chapter 5. Conclusion

To allow for full autonomy vehicles -i.e. a SAE level of 5- many sensors must be embedded from camera to lidar through RADAR systems. In this panel, radars present many advantages: a simultaneous measurement of distance and velocity, a high range and a high immunity to outdoor conditions. This flexibility allows various use cases from short range radars which create a safety cocoon around the car, to long range radars which allow an adaptive cruise control. Since few years, radars are based on fast chirp FMCW facilitating an unambiguous measurement of distance and velocity. Improving radar performances leads to two major trends for the receivers. First, the radar RF bandwidth increases to few gigahertz to improve the resolution. Secondly, the demodulated IF signal bandwidth also enlarges from 1MHz up to 40MHz. The development of the automotive radar market leads to select technologies capable of good RF performances, a high level of integration and a low production cost. Due to these considerations, a 28nm RF-CMOS technology is selected for this work.

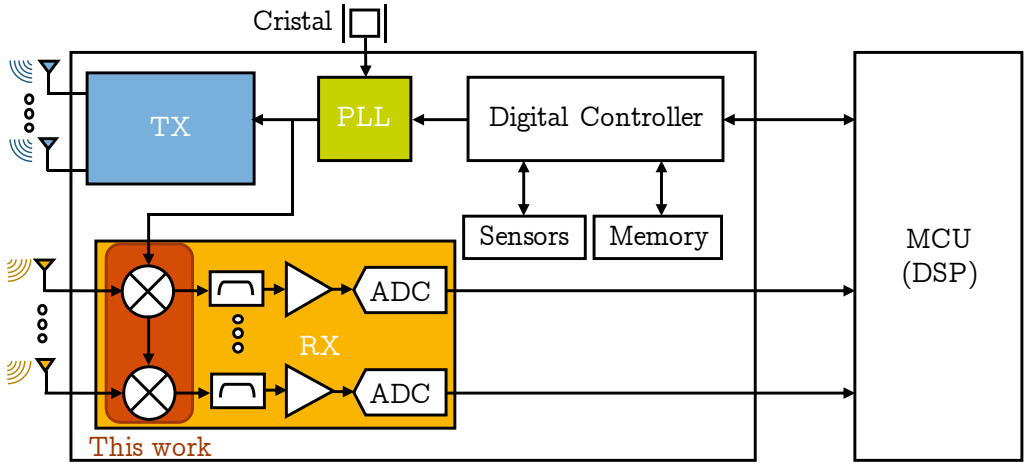


Figure 127 – RX-RFFE in a complete radar module

A high-level representation of a radar module is shown at Figure 127, including the micro controller unit (MCU). The RF Front-End features a PLL generating the LO signal, a transmitter (TX) and a receiver (RX). Obviously, the radars have general constrains on the power consumption, the form factor or the PVT robustness but also four critical RF specifications: PLL phase noise, PLL linearity, TX output power and the RX noise figure. This work focusses on the design of downconverters which is a critical block of RX modules. The specifications on noise of RX RF Front-End are determined considering three phenomenon: the radar equation which links the full-demodulator noise figure to the maximal range with various parameters such as antenna gain, output transmitted power and target characteristics; the

noise distribution over the demodulator chain featuring the downconverter and the analog blocks; and finally the de-sensitization of a received signal due the phase noise of the local oscillator and the lack of isolation between TX and RX. All these considerations, discussed in Chapter I of this manuscript, lead to define the specifications of the receiver module reported in Table 27.

Table 27 – Specifications of receiver RF front-end

Specifications	Min.	Typ.	Max.
RF bandwidth (GHz)	76		81
IF bandwidth (MHz)	1	/	40
Noise figure (dB) for LRR			15
Out-of-band ICP1 (dBm)	-5		
Passband ICP1 (dBm)	-20		
IIP3 (dBm)		-26	
Objectives	Min.	Typ.	Max.
Conversion Gain (dB)		10	
Power consumption (mW)		20	

Overall Contributions

To address these tough requirements in advanced RF CMOS technologies, modern receivers investigate architectures and design techniques altogether. In this thesis, a focus is proposed on two circuit techniques.

First, the circuits are designed to improve their efficiency (g_m/I_D) and to reduce their power consumption while maintaining the RF performances. To achieve a better efficiency, complementary current-reuse structures are preferred and transistors are biased in moderate inversion region when possible.

Secondly, the noise cancelling architecture is exploited to achieve a wideband behavior and to provide a low noise figure. Popular in the RF domain, this technique has never been experienced so far at millimeter-Waves. It is first exploited for the implementation of active mixers featuring additional techniques to reduce the flicker noise as shown Figure 128(a),. The concept of noise canceling is further exploited in an original design, Figure 128(b), using a capacitive cross-coupling in a complementary arrangement to achieve a power efficient LNA, namely C4 LNA.

At system level, the RF signal processing is discussed, and investigated, in this work throughout the mixing mode -i.e. current mode and voltage mode-. The two approaches are considered and evaluated for the implementation of a 77GHz RX-RFFE dedicated to LLR. The development of the Rx-RFFE involves the design of the base-band section.

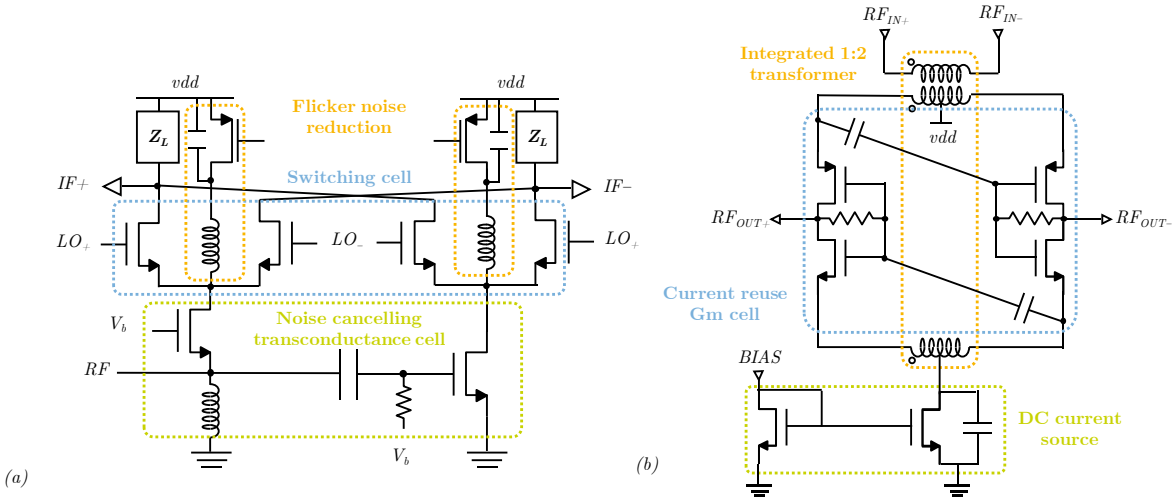


Figure 128 – Schematic of low noise amplifier using (a) common-gate based noise cancelling topology; (b) complementary capacitor cross coupled topology

Achievements

Table 28 – Summary of the performances of the RF noise cancelling demonstrator and the millimeter-Wave low noise amplifier designed in this thesis

Parameters	RF noise cancelling mixer		mmW noise cancelling LNA		mmW C4 LNA	
Operating temperature	25	85	25	150	25	150
Results	Meas.	Post-layout sim.	Post-layout sim.		Post-layout sim.	
Mixer topology	Passive		Passive		Passive	
Tech. (nm)	CMOS 28nm		CMOS 28nm		CMOS 28nm	
VDD (V)	1.2		0.6		1.5	
Frequency (GHz)	2.4		77		77	
Bandwidth (GHz)	5	5	16	16	15	15
Gain (dB)	15	14	14	8.7	10.8	8.2
NF (dB)	6.2	14	6	9.4	4.2	7.2
ICP1 (dBm)	-1	-1	-5	-4.5	-2.5	-3
Power (mW)	4	4	4.6	5	4.2	5
Area (mm^2)	0.04	0.04	0.024	0.024	0.011	0.011
FOMI	0.35	0.041	0.12	0.025	0.28	0.061
FOMII	8.8	1.0	4.8	1.0	25	5.3

Active mixing is first considered for its interesting trade-off between gain, noise and linearity. The noise cancelling is first demonstrated in an RF mixer whose performances are presented in Table 28. To reduce the impact of a large flicker noise, specific techniques are implemented in the mm-Waves version. Presented in Table 29, the 77GHz active mixer performing noise cancelation achieves in typical case a high gain, 12.5dB, a high linearity (ICP1), -2.5dBm and a moderate noise figure of 13dB. Considering PVT variations for automotive, the minimal gain is closed to 11dB, the linearity is higher than -7dBm while noise figure is below 18dB. Even with flicker noise reduction techniques, the noise figure is degraded by 8dB between 10MHz and 1MHz. This active down-converter demonstrates adequate performances for short range RADAR applications, but not enough low NF and linearity for a long-range use case as illustrated in Table 29. To address this issue a combination of a passive mixer with a LNA is further reconsidered in the following work.

Table 29 – Summary of the performances of the millimeter-Wave downconverter designed in this thesis

Parameters		mmW voltage mode downconverter with C4 LNA		mmW current mode downconverter with C4 LNTA		mmW noise cancelling active mixer	
Conditions		25	150	25	150	25	150
Results		Post-layout sim.		Post-layout sim.		Meas.	Post-layout sim.
Tech. (nm)		CMOS 28nm		CMOS 28nm		CMOS 28nm	
VDD (V)		1.5		1.5		1.5	
Frequency (GHz)		77		77		77	
Bandwidth (GHz)		14	13	19	18	30	30
Gain (dB)		20.3	15.5	20	16	13	12
NF (dB)	@1MHz	16	21	16.5	20	20	22
	@10MHz	10.1	15	11	15.5	13.5	16
ICP1 (dBm)	@20kHz	-9.1	-7.1	-4	-3	-2.5	-4
	@10MHz	-15.2	-13.6	-14	-16		
Power (mW)		18	18	23	23	16	16
Area (mm^2)		0.09	0.09	0.12	0.12	0.04	0.04
FOMI		0.008	0.003	0.015	0.004	0.007	0.003
FOMII		0.085	0.031	0.015	0.033	0.18	0.064

To address the linearity specification, a single stage LNA is preferred. Various arrangements of differential noise canceling LNA are evaluated, leading to the proposed C4-LNA which performances are summarized in Table 28. This topology designed at 77GHz compares favorably with the state of the art, especially in terms of performance to current trade-off. Passive mixing techniques is further investigated, with a comparison between voltage

and current mode downconverter. Figure 129 presents a complete RX-RFFE with a millimeter-Wave Front-End and a baseband analog chain, including three stages of high-pass filters and VGA. The designed voltage mode mixer achieves a low noise figure, below 14dB in the worst case, a high gain, above 15dB but it suffers from a poor linearity, ICP_1 below -7dBm. On the other hand, the current-mode downconverter presents a better trade-off between noise and linearity. Due to the high pass filtering, the baseband analog remains in voltage-mode and requires a TransImpedance Amplifier just after the mixer stage. The introduction of such additional block degrades the noise performance, +1dB, compared to voltage-mode down-converter. However, the current mode operation allows for an improved linearity since the ICP1 exceeds -5dBm. These results should be confirmed by the measurements of the manufactured circuits.

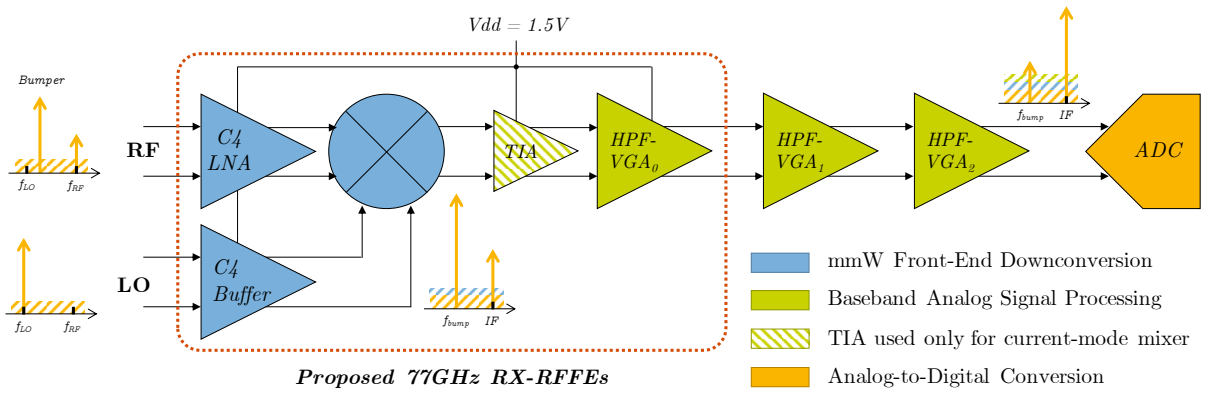


Figure 129 – Architecture of the proposed downconverter including a TIA if the mixer works in current-mode

Regarding the state-of-the-art of millimeter-Wave downconverter, shown in Table 30, the proposed downconverters present an interesting trade-off. Historical Silicium-Germanium BICMOS technologies offers high RF performances as reported by [42] at the cost of a high power consumption and a large silicon area. Active mixers usually present, as [45], a better trade-off between RF performances and power consumption but suffers from high flicker noise which is not easy to eliminate. On the other hand, downconverters featuring passive mixers, such as [54] - [56], have a poor trade-off between gain, noise and linearity. Most of the referenced downconverter cannot achieve simultaneously a high linearity to manage bumper reflection, a low noise and a high gain to maximize the radar range.

Table 30 – State of the art of millimeter-Wave downconverters

Parameters		[42]	[45]	[55]	[43]	[56]	[54]
Results		Meas.	Meas.	Meas.	Meas.	Meas.	Meas.
Mixer topology		Active	Active	Passive	Passive	Passive	Passive
Tech. (nm)		SiGe Bip.	CMOS 65nm	CMOS 65nm	CMOS 40nm	CMOS 40nm	CMOS 45nm
VDD (V)		3.3	1	1	1.1	1.1	1.1
Frequency (GHz)		77	77	77	77	60	60
Bandwidth (GHz)		15	28	5	/	10	9
Gain (dB)		21.5	9.5	11	30.8	30	26
NF (dB)	@1MHz	/	/	10	8	/	/
	@10MHz	10.8	9.2	9		5.5	6
ICP1 (dBm)	@20kHz	-5	-3.8	-22.3	-15	-31	-22.5
	@10MHz						
Power (mW)		70	15	143	143	35	21
Area (mm^2)		0.53*	0.27	0.231	0.8	0.7	0.023
FOMI		0.005	0.011	0.001	0.0002	0.0003	0.002
FOMII		0.009	0.042	0.004	0.0003	0.0004	0.08

Regarding these state-of-the art, the proposed circuits presents significant improvements regarding RF performances. Even if flicker noise reduction techniques have been implemented, the active mixing topologies cannot fulfill long range radar specifications due to their high level of flicker noise. Finally, passive mixing topologies present an interesting trade-off but requires advanced design techniques to improve the trade-off between linearity and noise. In this work, noise cancelling techniques have been experienced in millimeter-Wave to improve the RF performances of low noise amplifier with significant benefits, and the current-mode mixing operation demonstrates adequate performances.

The research and work done for this thesis can be pursued by:

a) improving the noise cancelling techniques for the development of 77GHz downconverters either at circuit level (LNA...) or architecture level
b) investigating I/Q architectures and maybe multi-phase mixing
c) the exploration of new frequency bands for emerging ADAS applications.

Dissemination

Journal

H. Vallée, T. Taris, T. Mesnard, G. Montoriol, X. Hours, *A 77-GHz Automotive Radar Downconverter with Noise Cancellation and Flicker Noise reduction in 28nm CMOS*, Transactions on Circuits and Systems II (submitted)

International Conferences

H. Vallée, T. Taris, T. Mesnard, G. Montoriol, X. Hours, *A 1-9 GHz wideband downconverter with noise cancellation and Gm-boosted transconductance cell*, IEEE International Conference on Electronics Circuits and Systems (ICECS), Bordeaux, 2018

H. Vallée, T. Taris, T. Mesnard, G. Montoriol, *A 0.8-6GHz Wideband Mixer with Noise Cancellation for Low Power Applications*, IEEE International Conference on Electronics Circuits and Systems (ICECS), Virtual, 2020

National Conferences

H. Vallée, T. Taris, T. Mesnard, G. Montoriol, X. Hours, *Un mélangeur large bande à annulation de bruit et cellule de transconductance de classe AB*, XXIe Journées Nationales Microondes (JNM), Caen, 2019

H. Vallée, T. Taris, T. Mesnard, G. Montoriol, X. Hours, *Un amplificateur à faible bruit à annulation de bruit à 77GHz pour radar automobile embarqué*, XXIe Journées Nationales Microondes (JNM), Caen, 2019

Bibliography

[1] European Commission, "Autonomous cars: a big opportunity for European industry," Brussels, 2017.

[2] CEPR, "The future economic and environmental costs of gridlock in 2030," London, 2014.

[3] Eurostat, "Greenhouse gas emission statistics - emission inventories," 2019.

[4] Policy Department Structural and Cohesion Policies, "Research for TRAN Committee - Self piloted cars: the future of road transport ?," European Parliament, 2016.

[5] Society of Automotive Engineers, "SAE International Releases Updated Visual Chart for Its "Levels of Driving Automation" Standard for Self-Driving Vehicles," Society of Automotive Engineers, 11 December 2018. [Online]. Available: https://www.sae.org/news/press-room/2018/12/sae-international-releases-updated-visual-chart-for-its-%E2%80%9Clevels-of-driving-automation%E2%80%9D-standard-for-self-driving-vehicles.

[6] P. Morgan, *NXP ADAS Sensors Light the Way for Autonomous Driving,* NXP Semiconductors, 2018.

[7] D. Salle, *Architecture of an autonomous vehicle,* Toulouse: NXP Semiconductors, 2018.

[8] M. M. Sayed, "Millimeter wave tests and instrumentation," in *ARFTG Conference*, Long Beach, 2005.

[9] European Telecommunications Standards Institute, "Short Range Devices; Measurement Techniques for Automotive and Surveillance Radar Equipment," Sophia-Antipolis, France, 2016.

[10] European Telecommunications Standards Institute, "EN 301 091," Sopha-Antipolis, 2016.

[11] European Telecommunications Standards Institute, "EN 302 264," Sophia-Antipolis, 2016.

[12] European Telecommunications Standards Institute, "ETSI EN 302 858," Sophia-Antipolis, 2016.

[13] J. Hasch, E. Topak, R. Schnabel, T. Zwick, R. Weigel and C. Waldschmidt, "Millimeter-Wave Technology for Automotive Radar Sensors in the 77 GHz Frequency Band," *IEEE*

TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, vol. 60, no. 3, pp. 845-860, 2012.

[14] K. Ramasubramanian, "Using a complex-baseband architecture in FMCW radar systems," Texas Instruments, Dallas, 2017.

[15] D. Dhar, P. van Zeljl, D. Milosevic, H. Gao and A. van Roermer, " Modeling and analysis of the effects of PLL phase noise on FMCW radar performance," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, 2017.

[16] M. Dudek, I. Nasr, D. W. R. Kissinger and G. Fischer, "The Impact of Phase Noise Parameters on Target Signal Detection in FMCW-radar system simulations for automotive applications," in *IEEE CIE International Conference on Radar*, Chengdu, 2011.

[17] C.-E. Souria, Conception d'interfaces boitiers innovantes pour le radar automobile 77-GHz. Application à la conception otpimisée d'une chaine de réception radar en boitier, Toulouse: Université Toulouse 3 Paul Sabatier, 2017.

[18] Internation Telecommunication Union, "Reference radiuation patterns of omnidirectional, sectoral and other antennas in point-to-multipoint systems for use in sharing studies in the frequency range from 1GHz to about 70GHz," Internation Telecommunication Union, Geneva, 2012.

[19] C. Kärnfelt, A. Péden, A. Bazzi, G. El Haj Shhadé, M. Abbas and T. Chonavel, "77 GHz ACC Radar Simulation Platform," in *9th International Conference on Intelligent Transport Systems Telecommunications*, Lille, 2009.

[20] C. Pavao Moreira, "Automotive Radar Transceivers," NXP Semiconductor, Toulouse, 2018.

[21] H.-L. Blöecher, M. Andres, C. Fischer, A. Sailer, M. Goppelt and J. Dickmann, "Impact of system parameter selection on radar sensor performance in autoimotive applications," *Advances in Radio Science,* vol. 10, pp. 33-37, 2012.

[22] L. Belostotski, "No Noise is Good Noise," *IEEE Microwave Magazine,* pp. 28-40, 2016.

[23] S. Afroz, H. Kim and K.-J. Koh, "Power-Efficient W-Band (92–98 GHz) Phased-Array Transmit and Receive Elements With Quadrature-Hybrid-Based Passive Phase Interpolator," *IEEE Journal of Solid-State Circuits,* vol. 53, no. 6, pp. 1678-1693, 2018.

[24] I. Das and N. Nallam, "Noise Cancelation? Explained!," *IEEE Microwave Magazine,* pp. 100-109, 2017.

[25] F. Bruccoleri, E. Klumperink and B. Nauta, "Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling," *IEEE Journal of Solid-State Circuits,* vol. 39, no. 2, pp. 275-282, 2004.

[26] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts and B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," *IEEE Journal of Solide-State Circuits,* vol. 34, no. 6, 2008.

[27] A. Apsel, "A Simple Guide to Low-Power Wireless Technologies," *IEEE Solid-State Circuits Magazine,* vol. 10, no. 4, pp. 16-23, 2018.

[28] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts and B. Nauta, "The Blixer, a Wideband balun-LNA-I/Q-Mixer Topology," *IEEE Journal of Solide-State Circuits,* vol. 43, no. 12, pp. 2706-2715, 2008.

[29] C. Enz, F. Chicco and A. Pezzotta, "Nanoscale MOSFET Modeling: Part 2: Using the Inversion Coefficient as the Primary Design Parameter," *IEEE Solid-State Circuits Magazine,* vol. 9, no. 4, pp. 73-81, 2017.

[30] E. Kargaran, B. Guo, D. Manstretta and R. Castello, "A Sub-1-V, 350-μW, 6.5-dB Integrated NF Low-IF Receiver Front-End for IoT in 28-nm CMOS," *IEEE Solid-State Circuits Letters,* vol. 2, no. 4, pp. 29-32, 2019.

[31] M. Ramella, I. Fabiano, D. Manstretta and R. Castello, "A SAW-Less 2.4-GHz Receiver Front-End With 2.4-mA Battery Current for SoC Coexistence," *IEEE Journal of Solid State Circuits,* vol. 52, no. 9, pp. 2292-2305, 2017.

[32] Z. Lin, P.-I. Mak and R. P. Martins, "A 2.4 GHz ZigBee Receiver Exploiting an RF-to-BB-Current-Reuse Blixer + Hybrid Filter Topology in 65 nm CMOS," *IEEE Journal of Solid State Circuits,* vol. 49, no. 6, pp. 1333-1344, 2014.

[33] A. Dissanayake, H.-G. Seok, O.-Y. Jung, S.-K. Han and S.-G. Lee, "A 64 μW, 23 dB Gain, 8 dB NF, 2.4 GHz RF Front-end for Ultra-Low Power Internet-of-Things Transceivers," in *IEEE Radio Frequency Integrated Circuits Symposium*, Honolulu, 2017.

[34] S. K. Hampel, O. Schmitz, M. Tiebout and I. Rolfes, " Inductorless Low-Voltage and Low-Power Wideband Mixer for Multistandard Receivers," *IEEE Transactions on Microwave Theory and Techniques ,* vol. 58, no. 5, pp. 1384 - 1390, 2010 .

[35] H. Darabi and A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model," *IEEE Journal of Solid State Circuits (JSSC),* vol. 35, no. 1, pp. 15-25, 2000.

[36] R. Pullela, T. Sowlatti and D. Rozenblit, "Low Flicker-Noise Quadrature Mixer Topology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, 2006.

[37] H. Darabi and J. Chiu, "A Noise Cancellation Technique in Active RF-CMOS Mixers," *IEEE Journal of Solid-State Circuit (JSSC°,* vol. 40, no. 12, pp. 2628-2632, 2005.

[38] W. Cheng, A. J. Annema, G. J. M. Wienk and B. Nauta, "A Flicker Noise/IM3 Cancellation Technique for Active Mixer Using Negative Impedance," *IEEE Journal of Solid-State Circuits,* vol. 48, no. 10, pp. 2390-2402, 2013.

[39] E. Klumperink, S. Gierkink, A. van der Wel and B. Nauta, "Reducing MOSFET 1/f Noise and Power Consumption by Switched Biasing," *IEEE Journal of Solid-State Circuits,* vol. 35, no. 7, pp. 994-1001, 2000.

[40] R. Ciocoveanu, R. Weigel, A. Hagelauer and V. Issakov, "Modified Gilbert-Cell Mixer With an LO Waveform Shaper and Switched Gate-Biasing for 1/f Noise Reduction in 28-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 2, no. 4, pp. 1688-1692, 2019.

[41] J. Park, C.-H. Lee, B.-S. Kim and J. Laskar, "Design and Analysis of Low Flicker-Noise CMOS Mixers for Direct-Conversion Receivers," *IEEE Transactions On Microwave Theory and Techniques (TMTT),* vol. 54, no. 12, pp. 4372-4380, 2006.

[42] S. Yang, H. Forstner, G. Haider, H. Kainmueller, K. Aufinger, L. Maurer and R. Hagelauer, "A low noise, high gain, highly linear mixer for 77 GHz automotive radar applications in SiGe:C bipolar technology," in *European Solid-State Circuits Conference (ESSCIRC)*, Athens, 2009.

[43] T. Murakami, N. Hasegawa, Y. Utagawa, T. Arai and S. Yamaura, "A 9 dB Noise Figure Fully Integrated 79 GHz Automotive Radar Receiver in 40 nm CMOS Technology," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Boston, 2019.

[44] J. Shi, L. Li and T. J. Cui, "A 60-GHz broadband Gilbert-cell down conversion mixer in a 65-nm CMOS," in *IEEE International Conference of Electron Devices and Solid-state Circuits*, Hong Kong, 2013.

[45] Z. Liu, J. Dong, Z. Chen, Z. Jiang, P. Liu, Y. Wu, C. Zhao and K. Kang, "A 62-90 GHz High Linearity and Low Noise CMOS Mixer Using Transformer-Coupling Cascode Topology," *IEEE Access,* vol. 6, pp. 19338-19344, 2018.

[46] S.-K. Kim, C. Cui, G. Huang, S. Kim and B.-S. Kim, "A 77 GHz Low LO Power Mixer With a Split Self-Driven Switching Cell in 65 nm CMOS Technology," *IEEE Microwave and Wireless Components Letters,* vol. 22, no. 9, pp. 480-482, 2012.

[47] A. Medra, D. Guermandi, K. Vaesen, S. Brebels, A. Bourdoux, W. Van Thilo, P. Wambacq and V. Giannini, "An 80 GHz Low-Noise Amplifier Resilient to the TX

Spillover in Phase-Modulated Continuous-Wave Radars," *IEEE Journal of Solid State Circuit,* vol. 51, no. 5, 2016.

[48] D. Fritsche, G. Tretter, C. Carta and F. Ellinger, "Millimeter-Wave Low-Noise Amplifier Design in 28-nm Low-Power Digital CMOS," *IEEE Transactions on Microwave Theory and Techniques,* vol. 63, no. 6, 2015.

[49] B. Cetinoneri, Y. A. Atesal, A. Fung and G. M. Rebeiz, "W-Band Amplifiers With 6-dB Noise Figure and Milliwatt-Level 170–200-GHz Doublers in 45-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques,* vol. 60, no. 3, 2012.

[50] C.-Y. Huang and J. Y.-C. Kiu, "62–92 GHz low-noise transformer-coupled LNA in 90-nm CMOS," *ELECTRONICS LETTERS,* vol. 54, no. 10, pp. 634-636, 2018.

[51] B. Martineau, A. Cathelin, F. Danneville, A. Kaiser, G. Dambrine, S. Lepilliet, F. Gianesello and D. Belot, "80 GHz Low Noise Amplifiers in 65nm CMOS SOI," in *ESSCIRC 2007 - 33rd European Solid-State Circuits Conference*, Munich, 2007.

[52] W. Zhuo, X. Li, S. Shekhar, E. S. H. K., J. Pineda de GFyvez, D. J. Allstot and E. Sanchez-Sinencio, "A Capacitor Cross-Coupled Common-Gate Low-Noise Amplifier," *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS,* vol. 52, no. 12, pp. 875-879, 2005.

[53] A. Liscidini, "Fundamentals of Modern RF Wireless Receivers," *IEEE Solid State Circuits Magazine,* vol. 7, no. 2, pp. 39-48, 2018.

[54] J. Borremans, K. Raczkowski and P. Wambacq, " A digitally controlled compact 57-to-66GHz front-end in 45nm digital CMOS," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, San Francisco, 2009.

[55] Z. Duan, D. Pan, Y. Wang, B. Liao, Y. Dai and F. Lin, " A 76-81GHz High-linearity CMOS Receiver Front-end for Automotive Radar," in *IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, Beijing, 2018.

[56] V. Vidojkovic, G. Mangraviti, K. Khalaf, V. Szortyka, K. Vaesen, W. Van Thillo, B. Parvais, M. Libois, S. Thijs, J. R. Long, C. Soens and P. Wambacq, "A low-power 57-to-66GHz transceiver in 40nm LP CMOS with −17dB EVM at 7Gb/s," in *IEEE International Solid-State Circuits Conference*, San Francisco, 2012.

Résumé / Abstract

Depuis plusieurs années, l'industrie automobile multiplient les systèmes d'aide à la conduite pour rendre les véhicules plus autonomes. Le radar 80GHz embarqué est un capteur aux nombreux avantages. Ainsi, l'industrie se trouve face à deux défis : réduire le coût des puces et améliorer leurs performances. L'objectif de cette thèse est de proposer des architectures et topologies susceptibles d'améliorer significativement les performances d'une récepteur radar dans nœuds technologiques CMOS avancés. Dans ce cadre, le récepteur radar est soumis à deux contraintes qui peuvent être contradictoires : un fort signal d'entrée amenant de fortes contraintes de linéarité et le besoin d'un récepteur optimisé en gain et en bruit pour améliorer sa portée.

Le premier axe est centré sur les techniques de conception. D'un côté, il s'agit de réduire la consommation des circuits au travers d'opération en moyenne inversion. De l'autre côté, il s'agit d'implémenter des techniques d'annulation de bruit. Ces techniques permettent de travailler sur de larges bandes passantes et d'améliorer les performances en bruit.

Le second axe de ce travail se concentre sur les techniques de mélange. Les mélanges actifs présentent un bon compromis entre de performances mais un bruit en 1/f élevé. Les mélangeurs passifs présentent alors un meilleur compromis. Pour cela, cette thèse propose d'implémenter un mélangeur en courant à 80GHz pour améliorer simultanément les performances en bruit et linéarité.

Mots clés : radar, millimétrique, amplificateur, faible bruit, mélangeurs, récepteur

Since few years, automotive industry implements more and more advanced driven assistance systems to improve safety and autonomy of vehicles. The embedded 80GHz radar is a sensor with many advantages. To face such requirements, semiconductor industry has to simultaneously reduce cost and improve radar performances. The objective of this thesis is to propose new architectures and topologies able to improve the radar receiver performances in advanced CMOS nodes. In an automotive context, the radar receiver face two main issues: a high-power input signal induces constraints on linearity, reduced noise figure and high gain to achieve a wider range.

In this thesis, a specific focus is proposed on two design techniques. First, the circuits are designed to reduce the power consumption by operating in the moderate inversion region. Secondly, the common-gate based noise cancelling technique has been implemented at 80GHz, achieving simultaneously a wideband behavior and a low noise figure.

Besides this thesis studies various mixing approach to determine the best suited for radar applications. First, active mixers achieve good performance trade-off but suffer from high flicker noise. To address this issue, passive mixers are then studied, achieving better trade-off. To overcome this drawback, an 80GHz current mode mixer featuring noise and linearity improvement is developed.

Keywords: radar, millimeter-Wave, low noise, amplifier, mixer, receiver