Design Tools for Millimeter Wave Ultra Wideband Distributed Amplifiers

Mohamad El Chaar

Mohamad El Chaar. Design Tools for Millimeter Wave Ultra Wideband Distributed Amplifiers. Micro and nanotechnologies/Microelectronics. Université Grenoble Alpes [2020-..], 2022. English. NNT : 2022GRALT067 . tel-03936695

HAL Id: tel-03936695

https://theses.hal.science/tel-03936695v1

Submitted on 12 Jan 2023

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ GRENOBLE ALPES

École doctorale : EEATS - Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)
Spécialité : Nano électronique et Nano technologies
Unité de recherche : Techniques de l'Informatique et de la Microélectronique pour l'Architecture des systèmes intégrés

Outils de conception pour l'amplification distribuée ultra large bande aux fréquences millimétriques

Design Tools for Millimeter Wave Ultra Wideband Distributed Amplifiers

Présentée par :

Mohamad EL CHAAR

Direction de thèse :

Florence PODEVIN Enseignante-Chercheure, Université Grenoble Alpes	Directrice de thèse
Sylvain BOURDEL Enseignant-chercheur Grenoble INP, Université Grenoble Alpes	Co-directeur de thèse
Manuel José BARRAGAN ASIAN Chargé de Recherche, CNRS	Co-directeur de thèse

Rapporteurs :

FRANK ELLINGER
PROFESSEUR DES UNIVERSITES, Technische Universität Dresden, Faculty of Electrical and Computer Engineering
Thierry PARRA
PROFESSEUR DES UNIVERSITES, Université de Toulouse III Paul Sabatier

Thèse soutenue publiquement le **29 septembre 2022**, devant le jury composé de :

Florence PODEVIN PROFESSEUR DES UNIVERSITES, Université Grenoble Alpes	Directrice de thèse
Sylvain BOURDEL PROFESSEUR DES UNIVERSITES, Université Grenoble Alpes	Co-directeur de thèse
Philippe BENECH PROFESSEUR DES UNIVERSITES, Université Grenoble Alpes	Président
FRANK ELLINGER PROFESSEUR DES UNIVERSITES, Technische Universität Dresden, Faculty of Electrical and Computer Engineering	Rapporteur
Thierry PARRA PROFESSEUR DES UNIVERSITES, Université de Toulouse III Paul Sabatier	Rapporteur
Jean-Yves DUPUY DOCTEUR EN SCIENCES, THALES DMS FRANCE SAS	Examinateur

Invités :

Philippe CATHELIN
INGENIEUR, STMicroelectronics
Antonio A. L. DE SOUZA
PROFESSEUR ASSOCIE, Federal University of Paraíba

Pour les amis, la famille et la France… Santé!

For Friends, Family and France… Cheers!

“Vacation?... What is this?... Never heard of it…”

A PhD candidate in mm-wave IC design

Abstract

Over the last few years, both data center and network traffic increased by several folds (more than six-fold, as stated by CISCO Systems, Inc.) and are still experiencing an ongoing growth. This demand for higher capacity while meeting with higher end-to-end quality service projects a continuous need for improvements in spectral efficiency enhancement techniques; however, a given spectrum band has its limit of volume it can support before reaching saturation levels. This pushes research efforts towards finding other solutions and a promising one is by exploiting the uncrowded millimeter-wave (mm-wave) spectrum through arranging more bandwidth. Signal amplification is one of the most basic and prevalent circuit function in modern RF- and microwave- systems. On the topic of wideband operation, distributed amplifier (DA) has proved to be a suitable and promising candidate with its ultra-wideband (UWB) performance. Meanwhile, the design of integrated circuit (IC) in mm-wave spectrum is becoming a challenging process due to the unavoidable parasitic that affect circuit performance and complicate design process. The reliability of the conventional design techniques through deriving mathematical equations, a simple and direct design process commonly used at low frequencies, starts to diminish. Another proposed design technique is by combining advanced-scripting languages with a proper physical model; this will lead to a smart and efficient technique of designing mm-wave IC DAs through a process referred as computer-automated design (CAutoD) process. In this thesis, in particular, we propose for DAs an original ABCD-parameter based chain matrix model, a well-known formalism originating from the passive RF-circuit domain, in addition to a CAutoD methodology built upon it. Following this design technique is considered complete to a much greater extent, since the model gives flexibility in controlling a wider range of correlated design parameters. It is also considered reliable, a crucial criterion for mm-wave design, since the model does not apply simplification or neglect parasitic effects. It is simple, since the designer does not have to deal with the tiny effects (parasitic) that affect DA behavior and, finally, it is considered versatile, since it does not impose restrictions on the design component topologies the designer might be interested to use. Our end-goal is to offer the mm-wave designer a different and interesting technique in which the outcome of the suggested CAutoD process is a set of 3D graphical design exploration (DSE) plots. Designers then can explore different feasible solutions and choose the best design that meet their multiple performance objectives. Its benefit here is demonstrated by exploring the design space of DAs with BWs ≥ 80 GHz where STMicroelectronics (ST) 55-nm CMOS technology process is used, reporting 216 feasible DA options to explore from. Two global optimum DAs amplifying frequencies up to 100 GHz were then implemented as circuit prototypes: a single stage DA with 6.01 GHz/mW of measured gain-bandwidth product over DC consumption ($\mathrm{GBP/P_{DC}}$) and a 17.5 THz GBP cascaded DA with 71.96 GHz/mW of $\mathrm{GBP/P_{DC}}$, being the highest figure of merits, to the authors' knowledge.

Contents

Chapter 1

General Introduction

The aim of this first chapter is to overview the reader on the subject of this thesis work that is wideband amplification in the millimeter-wave (mm-wave) frequency band (30 GHz-300 GHz). This high frequency band attracts strong interest for its uncrowded characteristic and opportunity to produce high date rate systems such that significant efforts are being dedicated to overcome the challenges faced when designing high-end mm-wave circuits. In particular, integrated circuit (IC) amplifier is a popular topic of study between the research community that is undergoing continuous improvement to break the limits on high frequency of operation, especially when the wideband criterion is targeted from a few GHz to hundred GHz and above. The need for such criterion has lead researcher towards distributed amplification as a promising candidate that offers such great capability and hence a critical circuit to adequately design. This topic also gains widespread interest especially when using complementary metal–oxide–semiconductor (CMOS) technology process for its attractive low-cost, high-volume production features and its ability of high frequency operation with continued device scaling. Nevertheless, a crucial challenge encountered is the lack of appropriate and accurate design techniques at such band where the simple analytical-based approaches, traditionally applied at low frequency spectrum, begin to fail and therefore advocate for a revaluation of design techniques.

The following sections outlines our context starting from a general overview on analog signal amplification and ending by stating our needs for an automated circuit design approach when dealing with mm-wave operating frequencies. Distributed amplification, which is the heart of this work, will be considered in Chapter 2, devoted specifically to introducing wideband amplifiers.

1.1 Analog Signal Amplification

Signal amplification is one of the most basic and prevalent circuit functions in modern RF and microwave systems. Amplifier block is found as a first component of any receiver front-end circuitry, on which overall receiver performance depends, as well as the last component of any transmitter front-end circuitry, on which a reliable transmission depends. In addition, an amplifier can be considered for implementation as an intermediate block in a complete system to compensate for any signal degradation encountered through intra-stages circuitry.

Those applications share one common goal and it is magnifying a weak signal for further RF-treatment or digital signal processing. From the literature, it is clear that the amplifier design subject and application in fully integrated systems dates back to the early 21th century. Demonstrative implementation inside receivers and transmitters front-ends, and even transceivers have been reported using Si CMOS [1]-[3], SiGe BiCMOS [4]-[7] and various III-V technologies such as GaAs and InP [8]-[10], to mention but a few. Those show its widespread interest between RF- and microwave- research community for performance exploration and improvement. While the demos of those systems can be considered old dated, but their added contribution to the community and value stays the same till this day. Their concept can be re-used in recent years for their originality and enhanced by benefiting from the advancement of semiconductor technologies towards smaller nodes for the purpose of operating at higher frequencies [11]-[13].

1.2 Move Towards Low-Cost Production: CMOS Technology as a Solution

To meet today needs of the consumer marketplace and the radio chipset to be practical for very large-scale production, the cost, size, and power consumption of any circuit solution has to be significantly below what is being achieved today using compound semiconductor technology. Traditionally, analog radio front-end ICs, especially the ones operating at high frequencies, have been designed using III-V compound technologies which have superior performance compared to SiGe BiCMOS and Si CMOS technologies due to their higher electron mobility [14], [15].

Still, a CMOS implementation promises higher levels of integration and reduced cost. ICs implemented using CMOS technology directly benefit from the higher speed limit of the scaled technology [16] and with continued device scaling, enable circuit blocks to operate at ever-increasing frequencies.

Typical telecommunication applications require not only transceiver and sensing hardware, but also digital circuity to process the acquired data. Silicon CMOS technologies are good candidates for the integration of such systems. These technologies are being considered particularly attractive for their potential of integration with intermediate frequency (IF) and baseband digital signal processing (DSP) functions, together with high performance analog frontends, enabling true systems-on-chip (SoC).

1.3 Move Towards High-Frequency Band: Millimeter-Wave Band as a Solution

Over the last few years, both data center and network traffic increased by several folds, and are still experiencing an ongoing growth at an unsustainable rate [17]. This increasing demand for higher capacity while meeting with the demand for high end-to-end quality service projects a continuous need for improvements in spectral efficiency enhancement techniques, particularly if the medium has to be shared with many users and interchanged data.

However, a given spectrum band has a limit for the volume of data it can support. Improving its throughput using bandwidth portioning and spectral aggregation techniques has already been exhausted, leading to their evolvement arguably providing insignificant enhancements to the recent spectrum bands since the latter have already reached their saturation level due to being over-packed. This pushes us to search for other solutions and one promising alternative is by arranging more bandwidth. The availability of uncrowded spectrum in the millimeter band to exploit from makes it possible to accommodate future significant increase in network traffic and producing multi-gigabit per second data accesses. This motivated research attempts to overcome the limitation on high frequency of operation through advancement in semiconductor technology process, such as technology scaling, for instance, and in the continuous proposal of innovative analog circuits. For what concerns the latter, it necessitates the development of advanced circuit topologies and suitable design techniques capable of meeting with the marketplace requirements. Therefore, mm-wave ICs is gaining a growing interest and receiving focus from recent activities by the research and development (R&D) department of both private and public sectors.

1.4 Move Towards High-Frequency Band: Issues Encountered

Operating at millimeter-wave spectrum, however, is seeing continuous efforts in system design to satisfy the demand for high-speed applications.

Generally speaking, synthesizing analog ICs in the high frequency spectrum subjects one to performance degradation cause by reduced quality of passive components and increase in parasitic that impact the highest operating frequency one could reach. Technological-wise speaking, and in this particular case, the attractive low-cost CMOS processes experience high sheet resistance, strict metal density rules and lossy silicon substrate that makes it challenging to achieve high-end mm-wave CMOS circuits.

In terms of design process, designing at mm-wave renders the conventional analytical-equation based design techniques difficult to be applied. The simplicity offered by them starts to diminish since more behavior-dominant parasitic elements comes into role and become difficult to neglect. Since simplicity is desirable in any design process, approximation is adopted, inaccuracy in design parameter sizing increases and hence dependency on electronic computer-aided design (CAD) softwares grows, such as Keysight Advanced Design System (ADS) or Cadence Virtuoso software. Since the demand of wireless and wireline communication is at high pace, the optimum design of any IC component becomes major part.

1.5 Move Towards High-Frequency Band: CAutoD Technique as a Solution

To meet the ever-growing demand of quality and competitiveness, iterative physical prototyping is now often replaced by automated prototyping. The introduction of artificial intelligence (AI) algorithms into the design process realizes an intelligent and automatic design, and consequently considerable time and effort could be saved. Meanwhile, designers will not have the concern that whether a specific topology can meet the design specification or whether another parameters set exists that corresponds to better performance.

However, before any code scripting can be performed or any proposal of algorithms and design methodologies can be possible, developing a suitable physical model that can properly simulate a given circuit behavior is considered an essential first step to this process. This model is required to be complete and accurate, besides offering the designer the possibility to have control over all design variables. Having control over all analog-circuit components equates to having the option to propose several design methodologies meeting multiple design objectives such as maximized output, highest speed, and cost-effectiveness, and identifying multiple figures of merit. It also equates to obtaining a design solution considered more of a global optimum solution than a local optimum solution. In addition, an important metric when proposing a design model is simplicity. When speaking of mm-wave IC design, especially, the less the designer has to deal with the plethora of tiny parasitic effects, the easier and time-efficient his design task is considered.

Combining both circuit design-model and the widespread of advance scripting languages will lead to a smart and efficient way of designing mm-wave ICs, which is commonly referred to CAutoD process. Such process will give the designer the ability to virtually explore a complete circuit before it is implemented for production.

1.6 Thesis Objectives

After demonstrating the big-picture of this thesis work, one can conclude that the theme of this manuscript will be about IC amplifier design, implemented using low-cost CMOS technology, with amplification bandwidth extending into the mm-wave frequency range. In addition, it emphasizes on the need for a simple design process based on computer automation, from proposing a versatile and complete physical model, and appropriate methodology to achieve a desired performance criterion by the analog designer. Combining both is required to provide optimum sizing-values for the circuit design parameters.

Among wide bandwidth amplifiers, our focus will be laid specifically on distributed amplifiers with the following report organization.

1.7 Organization of the Report

The remaining of this manuscript is organized as follows.

In Chapter 2, a specific introduction on wide bandwidth amplifiers is provided. Here, insights on the future trend towards operating at millimeter-wave are first discussed followed by a more particular discussion on distributed amplifier device as a promising solution to overcome the upper limit on frequency.

In Chapter 3, an overview of existing design techniques for distributed amplifiers and their limitations for mm-wave usage are described. An original matrix-based design model, based on four-port chain $ABCD$-parameter, is then proposed as a reliable and accurate model for this specific active circuit design to reach full CAutoD process.

In Chapter 4, a loss-compensated distributed amplifier, a topology for mitigating the high losses issue of mm-wave frequencies, is described. Based on its concept and using the proposed model of Chapter 3, an algorithmic design methodology is presented that maximizes bandwidth for a given passband flatness. Its outcome is a set of 3D design space exploration (DSE) plots that enables to explore a wide range of possible distributed amplifier solutions.

In Chapter 5, from the resulting DSE plots of Chapter 4, a global optimum 100-GHz bandwidth CMOS-based distributed amplifier is chosen and implemented for on-wafer characterization.

In Chapter 6, a THz gain-bandwidth cascaded CMOS-based distributed amplifier, with the same upper operating frequency of 100 GHz, is presented.

In the previous three chapters, the 55-nm CMOS process provided by STMicroelectronics (ST) was adopted for both illustration, and design exploration and implementations.

Finally, Chapter 7 provides a summary and general conclusion for the work presented in this manuscript.

Chapter 2

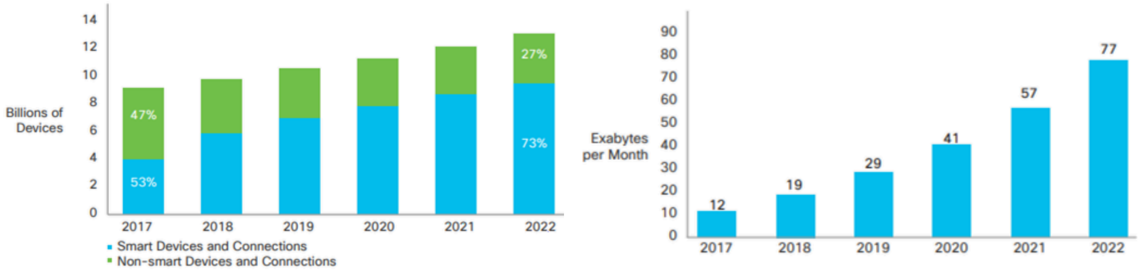
Introduction to Wideband Amplifiers – Distributed Amplifier for mm-Wave Access

In this chapter, a particular discussion is devoted on amplifiers capable of extending their operating frequency deep in the mm-wave band and proving distributed amplification as a unique solution with ultra-wide bandwidth performance from a few gigahertz until hundredth of gigahertz.

This chapter is structured as follows. Section 2.1 explains the motivation behind recent trend followed by analog designers towards realizing ICs in mm-wave band. It also sheds light on broadband amplification as an indispensable component of high demand in the near future. Section 2.2 examines several amplifier circuit topologies proposed in the literature to overcome the limitation on bandwidth, and demonstrates distributed amplification as a promising candidate for ultra-wide bandwidth. Section 2.3 focuses on the history, principle of operation, and technology versatility of distributed amplifiers. Here, a state-of-the-art table in different technology processes is provided for performance tradeoff comparison. Finally, Section 2.4 concludes this chapter and sets the tasks that will be covered in the following chapters.

2.1 Future Trends for Millimeter-Wave Applications

The RF spectrum is a finite resource to be shared by all network devices in the world. As years progress, the number of connected devices and data traffic is increasing at a significant rate, as illustrated in Figure 2.1. Those statistical graphics are provided by Cisco corporation [17] and demonstrate, via Figure 2.1(a), that by the year 2022 the overall amount of connected devices will reach 12.3 billion units, a 43% growth from 8.6 billion devices in 2017. In addition, via Figure 2.1(b), the overall mobile data traffic is expected to grow to 77 exabytes (10^9 gigabytes) per month by 2022, a seven-fold increase over 2017. Both statistics point to a no nearby deceleration in the amount of circulating information, on the contrary, they indicate a continuous surge in telecommunication in the upcoming years.



(a) (b)

Figure 2.1: Global (a) growth of connected devices and (b) mobile data traffic in exabyte (10^9 gigabytes) per month, from 2017 to 2022. [17]

Usually, the frequency spectrum is divided into several differently sized small-portions in order to accommodate the multi RF-applications. A demonstrative example of such radio spectrum partitioning, adopted by the United States [18], is illustrated in Figure 2.2. Oversharing of the spectrum, however, can lead to unintentional interference. This can happen between signals through overlapping of a given carrier sideband with upper and/or lower sidebands of adjacent carriers, and interference that occurs when frequencies shift slightly. In either case, they make it difficult or near impossible for receivers to pick out the correct signal. This unintentional interference mostly occurs because generating and treating an RF-signal is an imperfect process. Figure 2.2 can also serve as a visual proof for demonstrating the congestion we reached in recent frequency spectrum due to oversharing. Indeed, the common range spanning from few KHz to 30 GHz is over-populated and it is becoming progressively difficult to open room for future devices and applications, and a bottleneck for the support of the many attractive but bandwidth-demanding services of the coming multimedia society.

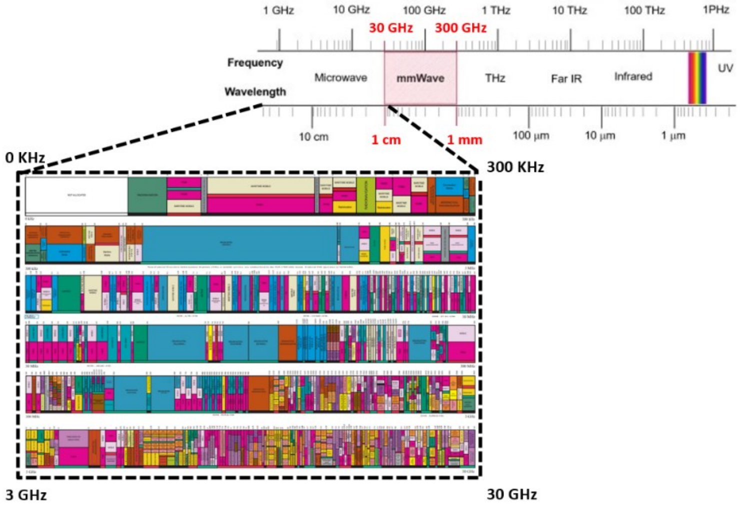


Figure 2.2: Radio spectrum demonstrating frequency allocations adopted by the United States. [18]

One common way used to alleviate this issue is by increasing the spectral efficiency, unit of measurement defined by (bits/sec)/Hz. This can be achieved through signal multiplexing techniques; for instance, through orthogonal frequency-division multiplexing (OFDM). Such ways, however, are starting to reach saturation levels in recent years [19], as shown in Figure 2.3, where capacity growth is slowing down and unable to keep up with the continuous increase in services demand. Due to occurring congestion in the frequency spectrum below 30 GHz, we reached a period in time where trying to push few bits of extra information in just a single Hertz of frequency component is becoming significantly challenging. Figure 2.3 also gives an early intuition that recent years advancement in radio resources management techniques is slowing down in demonstrating a notable improvement compared to the previous years; therefore, advocating the need to look for other solutions for the years to come.

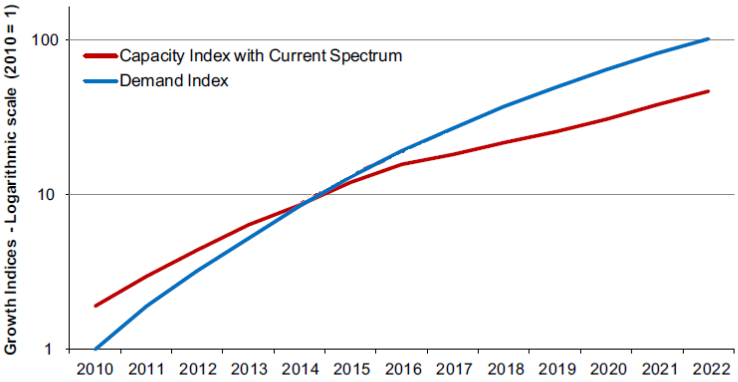


Figure 2.3: Comparing data capacity growth to demand growth. [19]

By referring back to Figure 2.2, one could perceive another promising solution and it is exploring the mm-wave band, i.e., beyond 30 GHz, to arrange more bandwidth. As formalized in the Shannon-Hartley theorem, enlarging bandwidths does indeed comply with obtaining higher channel capacity. In theory, there is an unlimited amount of unexploited bandwidth available in the 300 GHz frequency spectrum. It has motivated many research contributions on mm-wave electronics for wireless communication in general and broadband implementation in particular. Indeed, the sufficient broadband spectrum that exists there has sparked interest in a variety of potential applications, such short-range high data-rate wireless personal area networks (WPANs), wireless local area networks (WLANs) with extraordinary capacity, and wireless uncompressed digital-video transmission. This also allows for a variety of applications including gigabit/s point-to-point links, wireless docking for portable devices, and vehicular radar. Millimeter-wave systems find also place in the field of bio-medical devices. Today, imaging devices are largely confined to health-centers and large hospitals. The dynamics of patient-health provider interaction will radically change if these diagnostic tools are available by patient's side rather than at long distances. Examples include large-array low-power ultrasonic imagers and lab-on-chip devices for rapid detection of pathogens or sequencing of DNA [20]-[22]. Diagnostic medical imaging is another application that can greatly benefit from large capacity offered by such spectrum. Even in wireline communication, wireline backbones, such as fiber optic communication systems, with data rates of over 100 Gb/s per channel will be required in the near future and for those ultra-broadband systems with a minimum required bandwidth of 50 GHz are key components in such systems [23]. Therefore, the 30 GHz-300 GHz spectrum spanning about 55 GHz of contiguous bandwidth is identified as the most suitable candidate to accommodate the ever increase of circulating data deduced. It is also appearing as a promising solution for the support of all kinds of bandwidth-demanding services and applications that run at fiber speeds and beyond.

In fact, significant efforts in the development of ICs with frequencies extending into the mm-wave spectrum is already being observed. In parallel, silicon technology is being considered as an attractive design tool for the cost-reduction and miniaturization offered by it. Those efforts can be noticed from the available state-of-the-art research work [24]-[29], [30]-[36], to give example of few, which highlights the trend being adopted in pushing the limit of high frequency operation and in enlarging bandwidth performance. Through those available researches, diverse circuit techniques are being proposed besides their corresponding design theory and while offering the design tools and methodologies necessary to replicate such performance characteristics.

In this thesis, efforts were concentrated on broadband mm-wave amplification, in particular on a minimum of 50 GHz bandwidth to support future 100 Gb/s capacity and higher. This is elaborated more in the next section (Section 2.2) where several amplifier topologies, each with its own bandwidth limit, are listed and briefly described, where the most promising one is a distributed structure.

2.2 Amplifier Circuit Topologies with Wide Bandwidth Characteristic

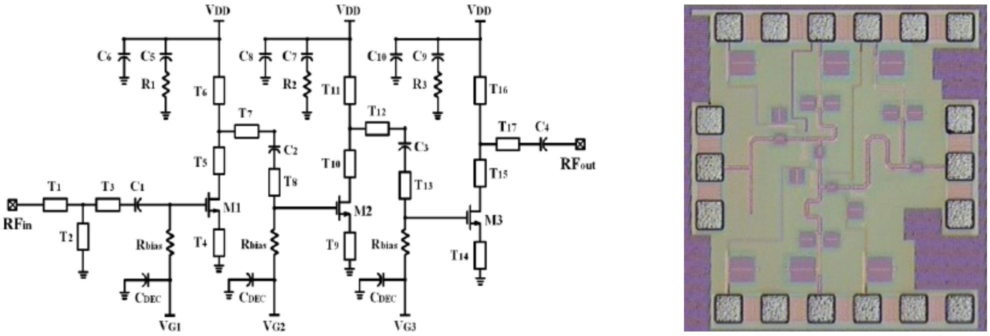
As telecommunication technology proceeds, expectations from an amplifier increase with it. Today’s telecommunication systems require wideband, efficient and high gain amplifiers. Depending on the application, requirements on an amplifier change. Obtaining high-gain and wideband systems has been one of the main areas of focus in wireless and wireline technologies. In RF and microwave amplifiers, transistors are employed as the main component; however, physical constraints of transistors put an upper limit to the gain and bandwidth of a practical amplifier. This fact is observed as gain-bandwidth product (GBP) which stays constant for an amplifier design. For these reasons, special consideration must be given to the problem of designing wide bandwidth amplifiers. Researchers have come up with some topologies to overcome the limitation on bandwidth. Some of those common approaches are listed below; note in each case that an improvement in BW is achieved at the expense of complexity, i.e., more correlated design variables to take into consideration, an added challenge when searching for optimum performance.

2.2.1 Small-to-Large Bandwidth Amplifiers Topologies

The topic of integrated amplifiers is not considered as a newborn research topic. For that, the literature demonstrates plenty of circuit prototypes implemented in several process nodes and each with different performance improvement objectives. In this section, concentration is put solely on the ones with bandwidth improvement as objective. Those topologies are listed starting by the one that offers the smallest bandwidth and ending by the topology that offers the largest one. For each case, a single optimum design example is given. A short description for each design is given accompanied by frequency behavior examination through S-parameter analysis.

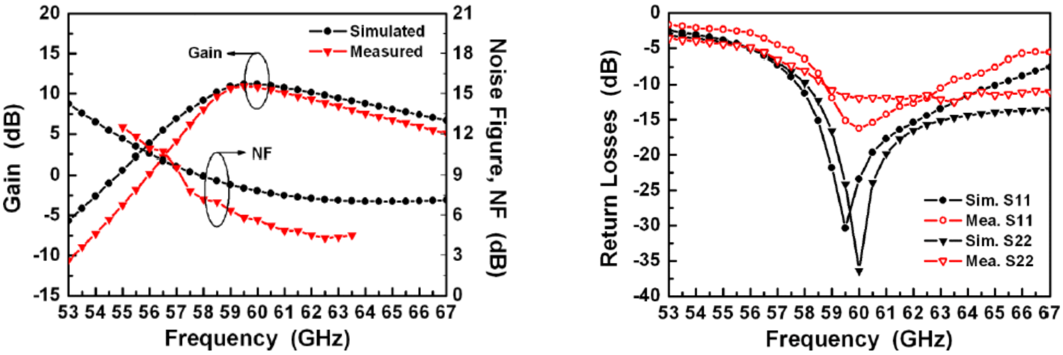
2.2.1.1 Single-Transistor Amplifier Topology [24]

We begin this listing by what could be arguably considered as the simplest topology one could synthesize and it involves using a single transistor as Gm-cell. It is considered of importance to demonstrate what one could obtain as frequency behavior when using just a simple transistor biased in the active region in order to support the efforts towards more complex topologies. It will also serve as a performance benchmark for the topologies coming after. [24] demonstrates such amplifier through a prototype implemented in 90-nm CMOS technology. Figure 2.4(a) and Figure 2.4(b) illustrate the circuit schematic and microphotograph, respectively. This amplifier is synthesized as a three-stage amplifier connected in series in order to increase its gain in the given bandwidth: a sign of weak amplification provided by just a single transistor. From Figure 2.5(a), the fabricated amplifier exhibits 10.8 dB of gain with 5 GHz of 3-dB bandwidth around 60 GHz, i.e., 8.3% of fractional bandwidth (FBW). The total power consumption is only 5.5 mW from a 1-V power supply. From Figure 2.5(b), both input and output return losses, S_{11} and S_{22}, respectively, exhibit narrowband behavior with values better than -15 dB at 60-GHz center of frequency.



(a) (b)

Figure 2.4: Single-transistor amplifier topology. (a) Schematic circuit diagram. (b) Microphotograph. [24]

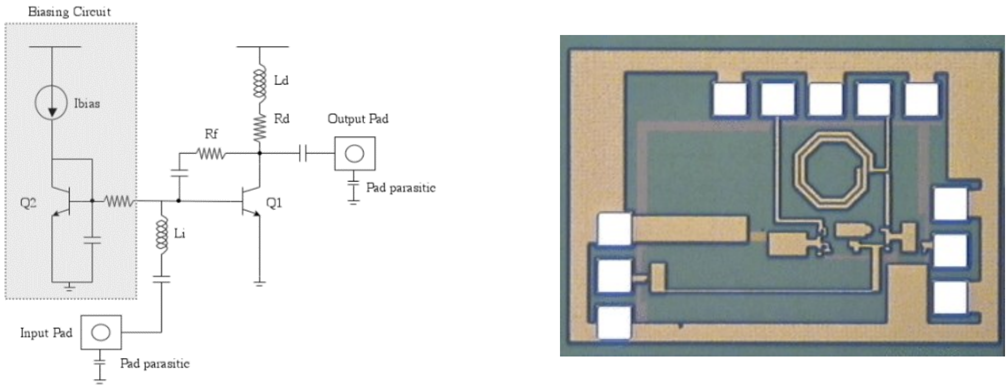


(a) (b)

Figure 2.5: Simulated and measured S-parameters versus frequency. (a) Insertion gain. (b) Input and output return losses. [24]

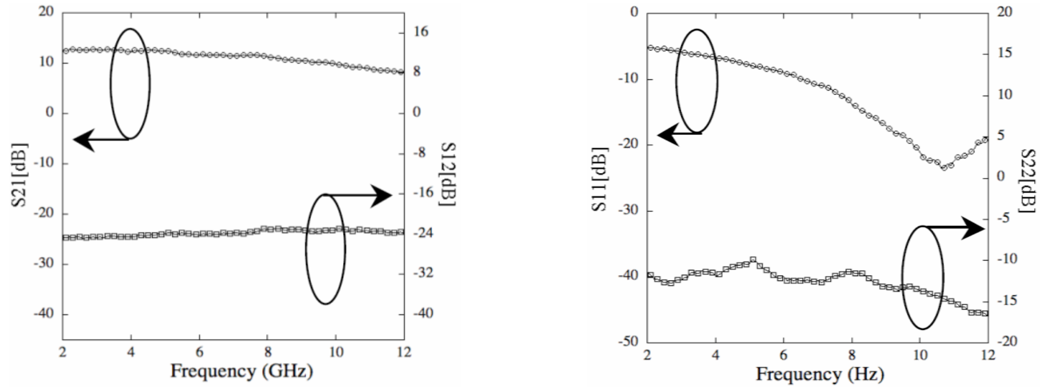
2.2.1.2 Resistive-Feedback Amplifier Topology [25]

The first suggested topology for obtaining wide bandwidth amplification is through resistive-feedback configuration [25]. Figure 2.6(a) illustrates the schematic view of this topology. The resistive shunt-feedback provides wideband input matching. Its bandwidth is dominated by the RC time constant at the input/output node. Figure 2.6(b) shows the implemented microphotograph using 0.18-µm SiGe BiCMOS process. The measured *S*-parameters are plotted in Figure 2.7. From Figure 2.7(a), a gain of 13 dB with 3-dB bandwidth of 10 GHz is obtained, i.e., more than 100% of FBW. While FBW here does seem interesting at first; however, one should note that as we increase in frequency, the inherent parasitic of the transistor start to affect the shunt matching provided by the resistive feedback. This makes it challenging to maintain wideband matching at mm-wave spectrum and support the efforts for more complex topologies. The fabricated amplifier consumes 4 mA from a 2.4-V power supply. From Figure 2.7(b), the input and output return losses are below -5 dB and -10 dB, respectively, within the declared passband. Through this topology, bandwidth enlargement is possible compared to the single-transistor amplifier topology [24] discussed at the beginning of this section.



(a) (b)

Figure 2.6: Resistive-feedback amplifier topology. (a) Schematic circuit diagram. (b) Microphotograph.[25]

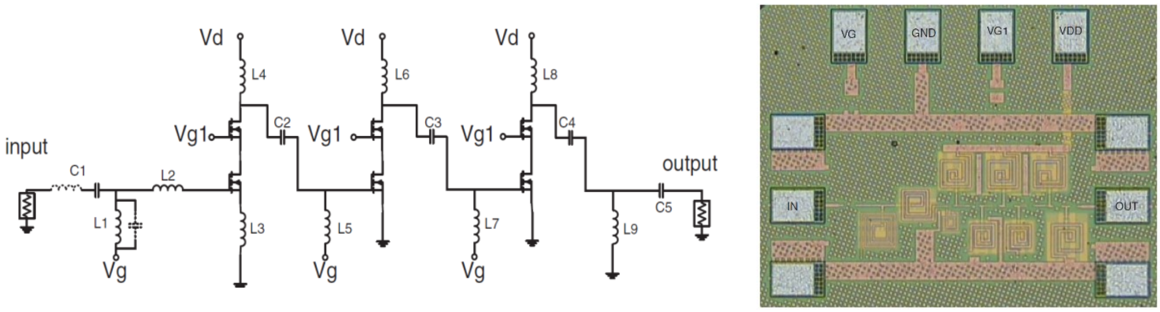


(a) (b)

Figure 2.7: Measured *S*-parameters versus frequency. (a) Insertion gain and reverse isolation. (b) Input and output return losses. [25]

2.2.1.3 Cascode Amplifier Topology [26]

Since design interest is focused on the mm-wave frequency region, parasitic capacitance becomes difficult to neglect. The most unfavorable capacitance that causes gain and bandwidth degradation a single transistor experiences is the input-to-output overlap parasitic, leading to a parasitic Miller capacitance. Arguably, the most widely used technique to mitigate it is by using a conventional cascode topology, where two transistors configuration is used at its simplest form. [26] demonstrates such cascode cell designed at 60 GHz and implemented with a 90-nm CMOS process. Its circuit topology and microphotograph are shown in Figure 2.8(a) and Figure 2.8(b), respectively. Its frequency response through *S*-parameters characterization is demonstrated in Figure 2.9. The amplifier exhibits 14 dB gain with a 3-dB bandwidth of 23 GHz around 60 GHz at 32-mW of total power consumption, i.e. 38.3% of FBW. The input and output return losses are below -8 dB within the declared passband region. Through this topology, a near five-fold fractional bandwidth enlargement is possible compared to the single-transistor amplifier topology [24] discussed at the beginning of this section.



(a) (b)

Figure 2.8: Cascode amplifier topology. (a) Schematic circuit diagram. (b) Microphotograph. [26]

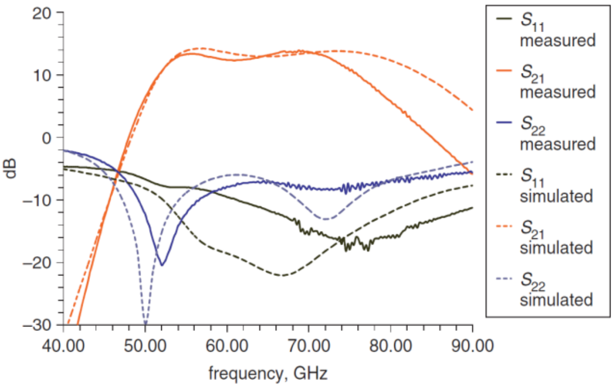
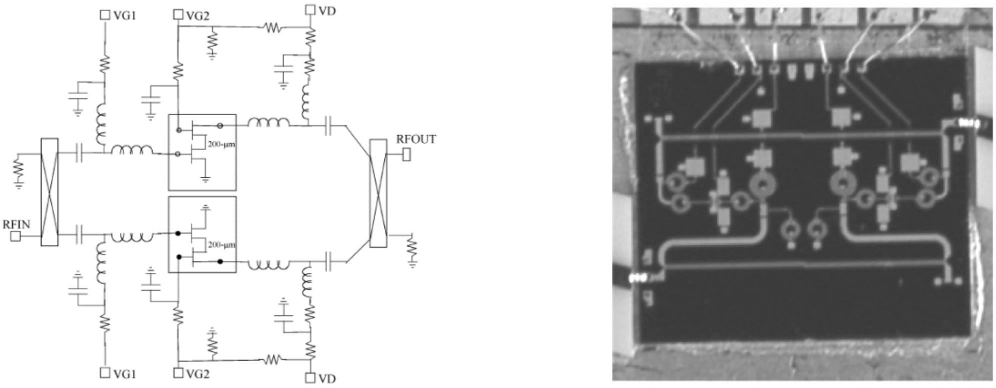


Figure 2.9: Simulated and measured *S*-parameters versus frequency. [26]

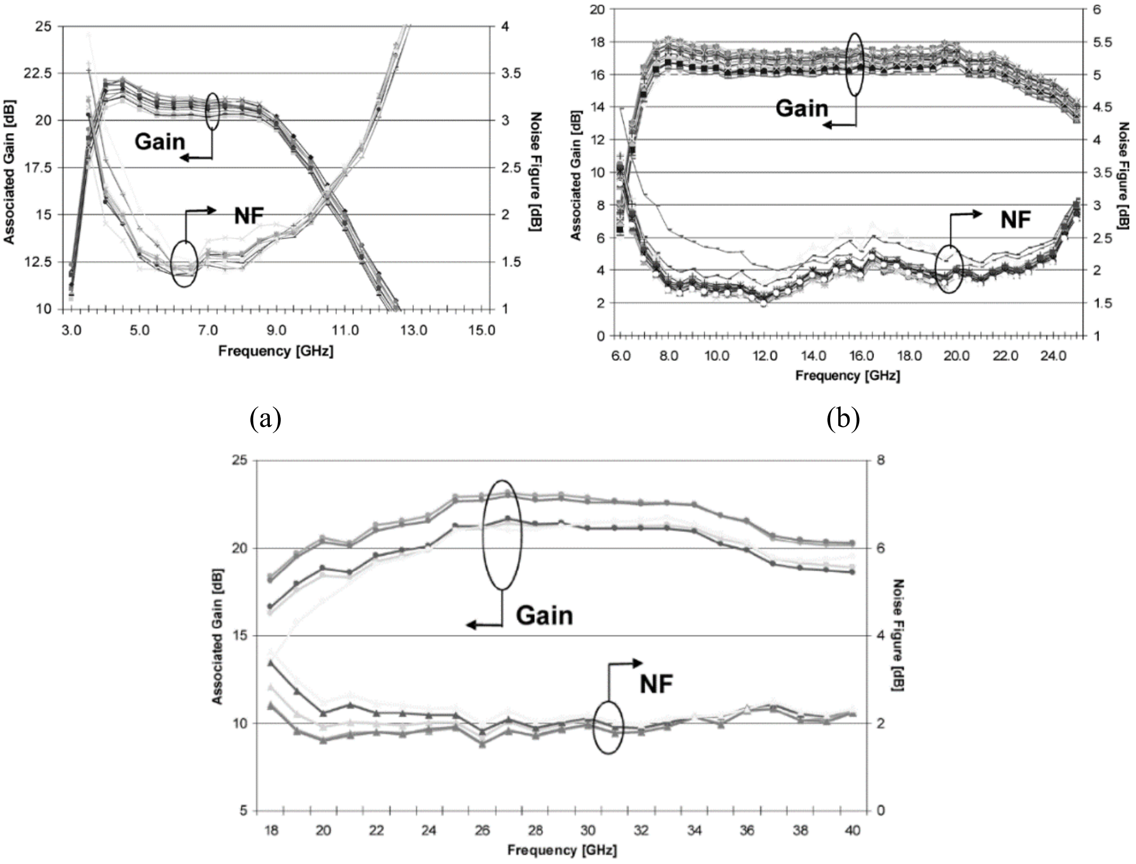
2.2.1.4 Balanced Amplifier Topology [27]

A common issue between microwave transistors is that they typically are not well matched to 50 Ω (a common standard reference-impedance). In the case of previous amplifiers topologies, matching networks where used. While matching network provides good input and output matching over the desired frequency bandwidth; however, it gives maximum gain only over a relatively narrow bandwidth. The balanced amplifier circuit solves this problem by using two 90-degree couplers to cancel input and output reflections from two identical amplifiers. [27] demonstrates such topology through a family of balanced amplifiers developed to cover an operating range of 4-40 GHz and implemented in a 0.1-µm pseudomorphic InGaAs/AlGaAs/GaAs HEMT production process. Schematic circuit diagram of only one design is presented here in Figure 2.10(a) with its respective microphotograph in Figure 2.10(b). The first 90° hybrid coupler divides the input signal into two equal-amplitude components, with a 90◦ phase difference, which drive the two amplifiers. The second coupler recombines the amplifier outputs. Because of the phasing properties of the hybrid coupler, reflections from the amplifier inputs cancel at the input to the hybrid, resulting in an improved impedance match; a similar effect occurs at the output of the balanced amplifier. [27] targeted three designs with different frequency bands including 4-9 GHz, 9-20 GHz, and 20-40 GHz, as illustrated in Figure 2.11. The two first designs demonstrate the excellent qualities of balanced amplifiers in terms of matching characteristics, while proving higher FBW than previously discussed designs, 77% and 76% for the 4-9 GH and 9-20 GHz cases, respectively, with a maximum of -15 dB of return loss for the 4-9 GHz and -17 dB for the 9-20 GHz. The 20-40 GHz also proves an extended bandwidth but return loss is not provided; nonetheless, its FBW extends up to 66.7%. Through the two first topologies, a nine-fold fractional bandwidth enlargement is possible compared to the single-transistor amplifier topology [24] discussed at the beginning of this section. The third topology shows an eight-fold improvement.



(a) (b)

Figure 2.10: Balanced amplifier topology. (a) Schematic circuit diagram. (b) Microphotograph. [27]



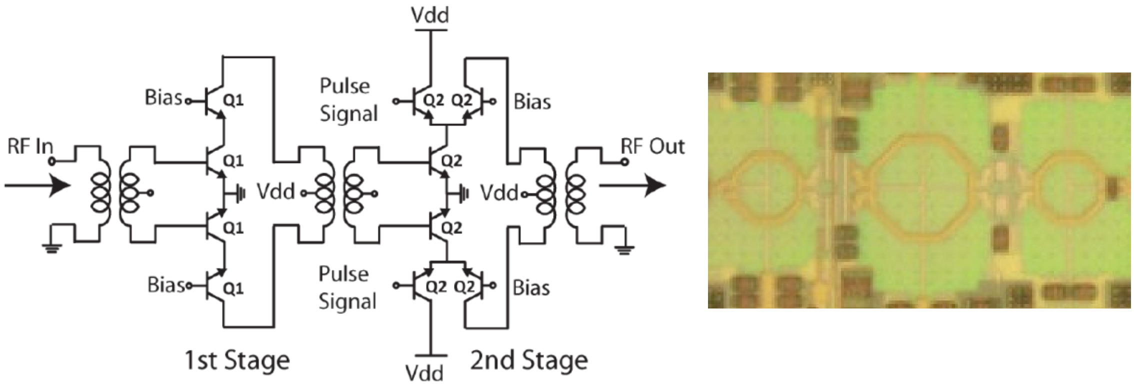
(a) (b)

(c)

Figure 2.11: Measured insertion gain responses of (a) 4-9 GHz, (b) 9-20 GHz and (c) 20-40 GHz balance-topology amplifier. [27]

2.2.1.5 Transformer-Coupled Amplifier Topology [28]

Similar to the balanced amplifier concept, the transformer-coupled topology aims at providing a wide bandwidth input- and output- matched impedances. Instead of using a 90-degree coupler, the following topology proposes the usage of transformers for input and output matching. Through them, they can simultaneously perform impedance transformation and differential-to-single-ended conversion. [28] demonstrates such circuit realized in a 0.13-µm SiGe BiCMOS process at 60 GHz with two coupled loop inductors as transformers. Circuit schematic is shown in Figure 2.12(a) with its microphotograph shown in Figure 2.12(b). Performance characterization of the amplifier against frequency is illustrated in Figure 2.13. A 3-dB bandwidth of 56 GHz, from 34 to 90 GHz, i.e. 90% of FBW, is obtained with gain of 12.25 dB while consuming a total P_{DC} of 270 mW. Matching is poorer than 6 dB in the lower band from 34 to 50 GHz. By reducing requirements to a reasonable matching better than 6 dB, the passband reduces within 50 to 90 GHz, i.e. still 57% of FBW that is almost seven-fold the one of the reference single transistor. Nonetheless, by relaxing the constraints on matching characteristic and on the basis of solely the stated amplification-passband 3-dB bandwidth (56 GHz), through this topology almost eleven-fold bandwidth enlargement is possible compared to the single-transistor amplifier topology [24] discussed at the beginning of this section.



(a) (b)

Figure 2.12: Transformer-coupled amplifier topology. (a) Schematic circuit diagram. (b) Microphotograph. [28]

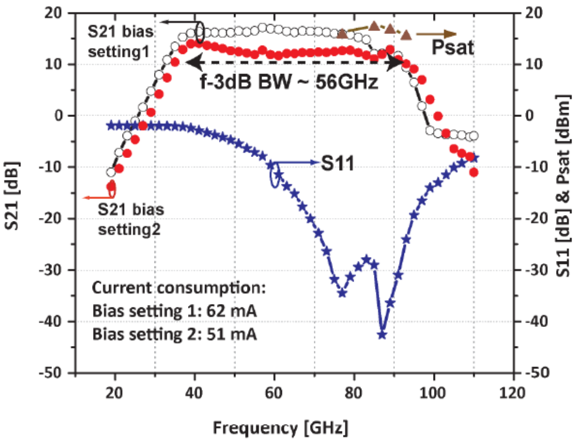
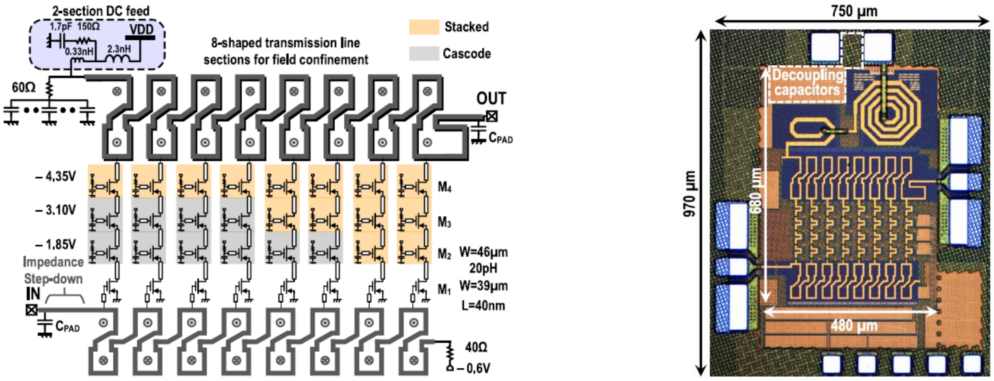


Figure 2.13: Measured S-parameters versus frequency. [28]

2.2.1.6 Distributed Amplifier Topology [29]

We end this listing by mentioning the topology that offers the widest bandwidth. Ultra-wide bandwidth characteristic is possible with distributed amplifier topology. As a short overview, with more in-depth details on its principle of operation provided in Section 2.3, the DA achieves its large bandwidth trough connecting pair of inductive-type segments at both the input and output ports of Gm-cell. Since the Gm-cell experiences input and output parasitic capacitance at high frequencies, the latter combined with inductive-type segments create what is called artificial transmission line (TL). Those artificial lines provide wide bandwidth matching which makes broadband amplification possible. Meanwhile the high gain of the DA results from the cumulative gains of those small Gm-cells. As a demonstrative example, [29] illustrated the performance capability of a 100-GHz DA, centered around 50 GHz from 4 to 104 GHz, i.e. 200% of FBW, implemented in a 45-nm CMOS SOI process. The meaning of center operating frequency loses somewhat sense with this architecture that can be seen as an accumulation of small sections of Gm-cells, each one showing an extended cut-off frequency due to inductive-type segments. In spite of that, its cut-off frequency can be adjusted through its design parameters, such as transistor size, and thus justifying the possibility to mention here the 50 GHz center frequency. Figure 2.14(a) and Figure 2.14(b) represent both its schematic diagram and fabricated circuit, respectively. From Figure 2.15, the amplifier attains 16 dB of gain while being powered from a 5-V supply. Through this topology, a twenty-two-fold bandwidth enlargement is possible compared to the single-transistor amplifier topology [24] discussed at the beginning of this section.



(a) (b)

Figure 2.14: Distributed amplifier topology. (a) Schematic circuit diagram. (b) Microphotograph. [29]

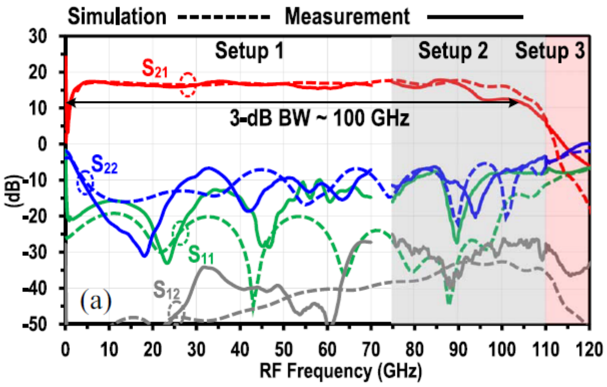


Figure 2.15: Measured S-parameter versus frequency. [29]

2.2.2 Table-of-Comparison for Performances Analysis

The six amplifier topologies that were presented in subsection 2.2.1 are summarized in Table 2.1. The purpose of this table is to review their performance tradeoffs and highlight, as a matter of course, why, in the context of RF spectrum enlargement towards mm-waves, the suitable topology is distributed amplification that will be the subject of further study in this manuscript. Since overcoming the upper limit on the gain and bandwidth of a practical amplifier is the motivation behind the proposal of such designs, the accent is put here on Gain-Bandwidth product (GBP) criterion. Special consideration on minimum bandwidth of 50 GHz is taken into account as it is important for future 100 Gb/s and beyond applications, as discussed previously in Section 2.1.

TABLE 2.1: PERFORMANCE COMPARISON BETWEEN WIDE BANDWIDTH AMPLIFIER TOPOLOGIES.

Ref.	**Amplifier Topology**	**Gain (dB)**	**Bandwidth (GHz)**	**P_{DC} (mW)**	**Chip Area (mm^2)**	**GBP (GHz)**
[24]	Single Transistor (Cascaded)	10.8	5	5.5	0.39	17
[25]	Resistive-feedback	13	10	9.6	0.88	45
[26]	Cascode	14	23	32	0.22	115
[27]	Balanced	20	5	187.5	12.16	50
		17	11	187.5	12.16	78
		22	20	187.5	8.6	252
[28]	Transformer-Coupled	12.25	56	270	0.15	229
[29]	Distributed	16	100	N/A	0.73	640

The first three topologies: single-transistor [24], resistive-feedback [25] and cascode [26] amplifiers are the one which present relatively simple design process compared to the remaining topologies, since they involve few components to deal with. They even show attractive low P_{DC} suited for low power consumption applications. However, they do not meet the required minimum bandwidth of 50 GHz and provide the lowest GBP merit, and hence were disregarded. Balanced amplifier topology [27] could demonstrate possible potentials in reaching this bandwidth requirement when pushed towards higher frequencies and it also shows flexibility in its GBP where one can obtain different BWs using the same topology. However, its design necessitates the implementation of two Gm-cells devices, as illustrated in Figure 2.10(a), hence twice the DC power, but with an overall delivered gain equal to that of a single Gm-cell device.

Both transformer-coupled amplifier [28] and distributed amplifier [29] topologies fulfill the minimum bandwidth requirement. However, as explained in Section 2.1 and illustrated by Figure 2.1, the number of connected devices and data traffic, in other words, data network, is constantly increasing and with no sign of stopping in the future. At one moment in the future, even larger bandwidths will be of need. Hence, a good research practice would be to anticipate the future and be prepared for the system demand. For that reason, distributed amplifier is chosen as topic of further discussion since it is the only topology that presents potential ultra-wide bandwidth performance reaching deep into the millimeter-wave spectrum. It also coincides with continuous advancement in technology nodes where smaller nodes are reaching higher frequency limits. It is worth also adding from a practical point of view, that the transformer-coupled amplifier presents inability to start amplifying from very low frequencies, if needed, compared to distributed amplifier. A requirement for fiber optic communications. This lack of ability to amplify starting from DC-level is because in the former topology, the input signal is being fed through a transformer to the input of the transistor, as shown in Figure 2.12(a), compared to being feed through a transmission line segment as in the case of a DA, as shown in Figure 2.14(a).

As a conclusion and on those bases, the remaining of this chapter is dedicated into describing the DA circuit topology and analyzing its basic principle of operation and performances.

2.3 What is a Distributed Amplifier?

In Section 2.1, a serious issue of congestion in the lower side of the radio spectrum due to over-sharing was identified. It highlighted the efforts taken by analog designers in moving towards the unexplored millimeter band as a promising solution to respond to the consumer marketplace for high-speed applications and possibility, by expanding the allocation bandwidth, to accommodate further increase in data traffic. Several proposed amplifier topologies for enlarging bandwidth were discussed in Section 2.2 and demonstrated the trend adopted in continuously trying to push the upper frequency limit. Since DA presented the potentials of achieving the largest bandwidth, suitable for today and future needs, this section is dedicated to elaborate more on the subject. For a systematic presentation, it is divided into four subsections. It starts by presenting the history and interest of DA design since 1936. Then, it introduces its structure and principle of operation. The intention here is to give the reader a first step towards understanding how a DA usually functions and what controls its behavior. Several DAs implemented in different IC technology processes are also provided that demonstrate its widespread popularity between research community for performance exploration. Finally, a state-of-the-art table summarizing all IC DAs in different technology processes is presented and discussed.

2.3.1 Walk Through History

The potential of distributed amplification for obtaining gains over wide frequency bands has long been recognized. Historically, distributed amplifier is an ancient concept appearing in the 20th century. It was first explored by British inventor William S. Percival with vacuum tubes to compensate for the parasitic capacitance of electrodes. He later was the first to deposit a single patent on this topic in 1936 [37], shown in Figure 2.16, but without any exhaustive explanation or any trace of further discussion of this idea in the literature.

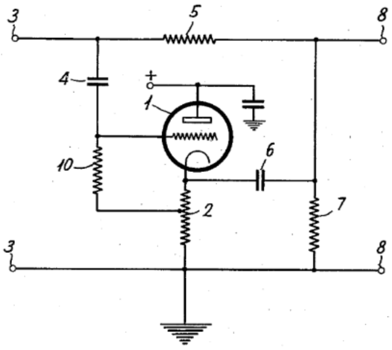


Figure 2.16: Thermionic valve circuit - William S. Percival's 1936 patent. [37]

The work became renown with the publication of [38] in 1948, where both Ginzton, Hewlett, Jasberg and Noe, based on the concept disclosed by William Percival, discovered that by appropriate distribution of vacuum tubes along artificial transmission lines, it is possible to obtain amplification over much greater bandwidths than would be possible with ordinary circuits. Their objective at that time was to find a practical solution for extremely broadband "video" amplifiers which have flat frequency response from low audio frequencies to frequencies as high as several hundred Megahertz. Due to technology limitation at their generation, practical limitations of electron tubes prevented them to reach frequencies up to 1000 MHz. Nevertheless, [38] was considered the first published research work to present the principle in wide-band amplifier design and hence the term "distributed amplifier" was born. Figure. 2.17 illustrates the general principle of distributed amplification using vacuum tubes as amplification elements presented by [38], which later was adopted and still being adopted in recent research work.

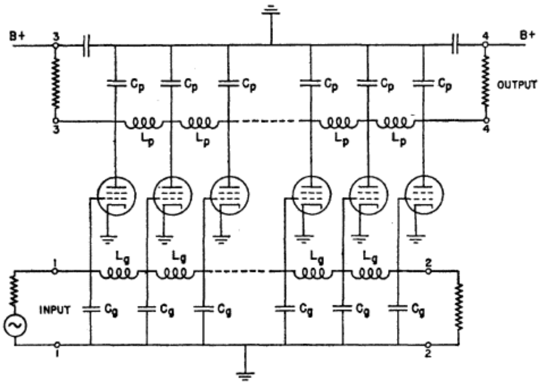


Figure 2.17: First schematic diagram of distributed amplifier using vacuum tubes from 1948. [38]

Implementation using solid-state devices followed with early demonstration presented by [39] in 1969, where an attempt was made in implementing a distributed amplifier with 2 GHz bandwidth using MESFET technology.

In 1982, [40] was published introducing a new concept of treating the DA as a continuous-structure model. It provided the required analytical approach to represent a DA gain behavior with respect to frequency and the design tools necessary to size one. In [40], the design concept was enhanced and made suitable for implementing amplifiers with several gigahertz of bandwidth. They demonstrated their idea through a practical example where they realized a DA that covers 1-13 GHz using 1-µm GaAs FET technology.

Even in the early 21st century, this concept is still being widely adopted between authors, such as [30]-[36], while synthesizing DAs at multi-gigahertz frequencies.

2.3.2 Structure and Basic Principle of Operation

Figure 2.18 illustrates the configuration of a conventional distributed amplifier. The core of a DA design consists of what is commonly referred to as a unit cell. A unit cell is composed of a Gm-cell connected to a set of four inductive-type segments, depicted here as having an inductance value of $L_I/2$ and $L_O/2$, on both its respective input and output sides. A set of N unit cells are connected together until a desired overall level of amplification is reached within a given passband. Since every Gm-cell is loading each inductive side by its own inherent output and input complex impedances, the overall upper and lower sides of DA are referred to, in this manuscript, as output- and input- loaded lines, respectively.

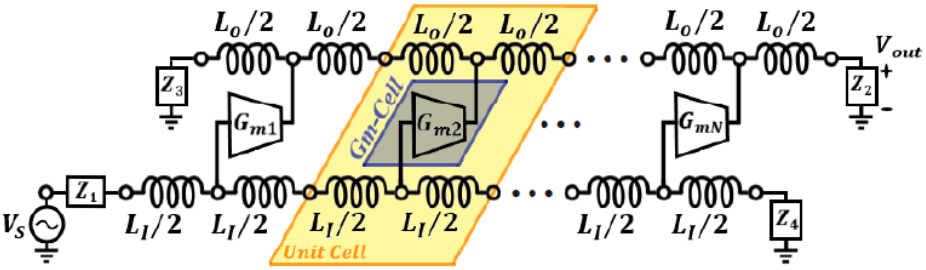


Figure 2.18: Conventional distributed amplifier made of N unit cells.

An RF signal (V_S) applied at the input end of the loaded input line travels towards the right side, where it is absorbed by the terminating load impedance Z_4 at the opposite end. As it travels down, each Gm-cell samples a portion of the signal at different phase and amplitude, and then transfer it to the output line through its own transconductance. Due to the non-ideality of those Gm-cells, a small portion of both signals is wasted through dissipation caused by the cells resistive loads distributed along the input and output lines.

If the phase delay of the signal at the output-loaded line is identical to the phase delay of the input-loaded line, then the signals on the former line add constructively. The addition will be in phase only for the forward-traveling signal. There is also a backward traveling wave component on the output line, but the individual contributions to this wave will not be in phase, and therefore they at least partially cancel. Any signal which travels backward and is not completely cancelled by the out-of-phase additions, will be absorbed by the termination output impedance, represented by Z_3 in Figure 2.18.

The basic principle behind distributed amplification is the absorption of the bandwidth limiting parasitic capacitances of Gm-cell into artificial transmission lines, which allows high bandwidths. In this approach, the added inductive-type segments combined with the parasitic capacitances are forming artificial TLs on each sides of the DA. The artificial lines will result in high cut-off frequencies, which will determine the new gain-bandwidth behavior of the desired amplifier. For a more in-depth explanation of this statement, the next discussion is dedicated to presenting the mathematical aspect behind the DA concept.

However, beforehand, for a clearer and more realistic analysis, the following modifications are carried out. First, the DA is split into two halves, as shown in Figure 2.19. The lower side represents the input loaded line and the upper side represents the output-loaded line. Second, since by the end of this manuscript a FET-based DA will be implemented as a circuit prototype for on-wafer characterization, it is considered suitable to adopt here, in the theoretical part, a FET-based Gm-cell and represent its behavior by its AC-equivalent lumped model. A unilateral assumption is used for its electrical model for the purpose of simplifying the derivation for a better interpretation of the concept. Finally, since in practice the ideal lumped inductors, $L_I/2$ and $L_O/2$, are typically implemented each as physical microstrip, they are replaced here by microstrip transmission (µ-TL) segments of length $l_g/2$ and $l_d/2$, respectively.

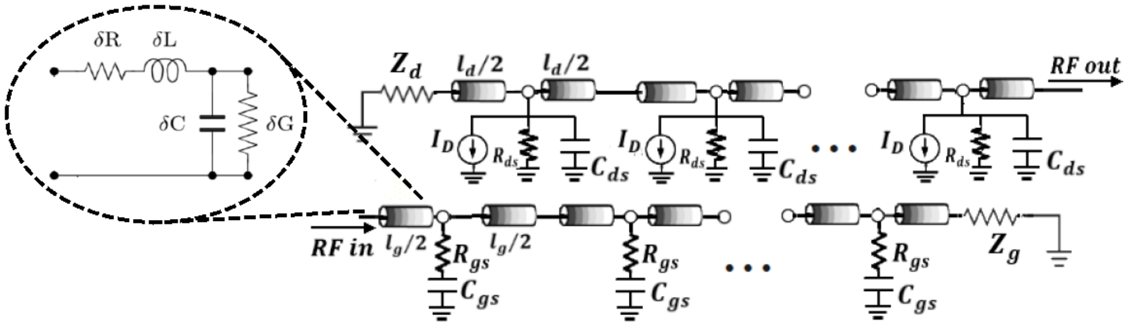


Figure 2.19: Simplified equivalent-circuit representation of a FET-based distributed amplifier.

Referring to Figure. 2.19, both R_{gs}, C_{gs}, R_{ds}, C_{ds} and I_D are the small-signal intrinsic elements of the FET transistor, and δR, δL, δC and δG are the per-unit-length series resistance (Ω/m), series inductance (H/m), shunt capacitance (C/m) and shunt conductance (S/m) of the lumped-element equivalent circuit of the μ-TL segment.

The combination of the distributed FET parasitic with the segments creates the artificial transmission lines. The input (gate) and output (drain) loaded-lines are represented by their effective series inductance-per-unit-length δL_g and δL_d, respectively, of their own segments. Their effective shunt capacitance-per-unit-length is a result of a merge between the parasitic capacitances from the FETs and segments, i.e., $(\delta C_g + C_{gs}/l_g)$ and $(\delta C_d + C_{ds}/l_d)$, respectively. What remains as resistive lumped elements act as per-unit-length series and shunt losses for those equivalent transmission lines.

The previous assumption of equivalent lines is only valid when the spacing between the FETs, i.e., l_g and l_d, is very small compared to the wavelength of operation (2.1).

$$l_g\big|_{max} \; and \; l_d|_{max} << \lambda_{guided} = \frac{c}{\sqrt{\varepsilon_{eff}} \cdot f_{operation}} \tag{2.1}$$

If this condition is satisfied, both lower and upper lines can be approximated each as continuous structure, referred to as artificial gate and drain lines, since FETs are used. Their characteristic impedances and propagation constants are deduced to be (2.2), (2.3) and (2.4), (2.5), respectively, [56].

$$Zc_g \approx \sqrt{\frac{\delta L_g}{\delta C_g + {C_{gs}}/{l_g}}} \tag{2.2}$$

$$Zc_d \approx \sqrt{\frac{\delta L_d}{\delta C_d + {C_{ds}}/{l_d}}} \tag{2.3}$$

$$\gamma_g = \alpha_g + j\beta_g \approx \left(\frac{\delta R_g}{2} \sqrt{\frac{\delta C_g}{\delta L_g}} + \frac{\omega^2 R_{gs} C_{gs}^2 Z c_g}{2 l_g} \right) + j\omega \sqrt{\delta L_g \left(\delta C_g + {C_{gs}}/{l_g} \right)} \tag{2.4}$$

$$\gamma_d = \alpha_d + j\beta_d \approx \left(\frac{\delta R_d}{2} \sqrt{\frac{\delta C_d}{\delta L_d}} + \frac{Z c_d}{2 R_{ds} l_d} \right) + j\omega \sqrt{\delta C_d \left(\delta C_d + {C_{ds}}/{l_d} \right)} \tag{2.5}$$

By preserving what was declared as initial condition in (2.1) for short length segments between Gm-cells, the gain expression for an N-cell DA circuit can be derived as follows.

For an incident source voltage, V_S, the voltage on the gate-to-source capacitance of the n^th FET, V_{C_n}, can be written as (2.6) for a phase reference from the first transistor.

$$V_{C_n} = V_S e^{-(n-1)\gamma_g l_g} \left(\frac{1}{1 + j\omega R_{gs} C_{gs}} \right) \tag{2.6}$$

The factor in parentheses in (2.6) accounts for the voltage division between R_{gs} and C_{gs}. For small node FET parameters, $(\omega R_{gs} C_{gs}) << 1$; therefore, this factor can be approximated as unity over the passband of the amplifier.

The output current on the drain line can be found by recognizing that each voltage-controlled current-source contributes to waves of the form $(-1/2) I_{D_n} e^{\pm \gamma_d x}$ in each direction when perfect matching is assumed from both sides of each node. Since the transconductance of a given Gm-cell is given, by definition, as $I_{D_n} = g_{m_n} V_{C_n}$, the total output current at the N^{th} terminal of the drain line is found to be (2.7), [56].

$$\begin{aligned} I_o &= -\frac{1}{2} \sum_{n=1}^{N} I_{dn} e^{-(N-n)\gamma_d l_d} \\ &= -\frac{1}{2} g_m V_S e^{-N\gamma_d l_d} e^{+\gamma_g l_g} \sum_{n=1}^{N} e^{-n(\gamma_g l_g - \gamma_d l_d)} \end{aligned} \tag{2.7}$$

Using the geometric series summation formula given by (2.8), allows (2.7) to be simplified as (2.9).

$$\sum_{n=1}^{N} x^n = \frac{x^{N+1} - x}{x - 1} \tag{2.8}$$

$$I_o = -\frac{g_m V_S}{2} \frac{e^{\gamma_d l_d}\left(e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}\right)}{e^{-(\gamma_g l_g - \gamma_d l_d)} - 1} \\ = -\frac{g_m V_S}{2} \frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}} \tag{2.9}$$

For a matched input and output ports, i.e., $Zc_g = Z_{in} = \mathrm{Z}_4$ and $Zc_d = Z_{out} = \mathrm{Z}_3$, the amplifier gain can be calculated as (2.10), [56].

$$Gain = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2}|I_o|^2 Zc_d}{\frac{1}{2}|V_S|^2 / Zc_g} \\ = \frac{g_m^2 Zc_g Zc_d}{4} \left| \frac{e^{-N\gamma_g l_g} - e^{-N\gamma_d l_d}}{e^{-\gamma_g l_g} - e^{-\gamma_d l_d}} \right|^2 \tag{2.10}$$

As mentioned previously, if the phase velocity of the signal at the drain line is identical to the one of the gate line, then the output signals on the drain line add constructively. The addition will be in-phase only for the forward traveling signal. Referring to equation (2.7), the terms in the summation will add only when $\beta_g l_g = \beta_d l_d$, i.e., the phase delays on the gate and drain lines are synchronized.

Applying the synchronization condition of $\beta_g l_g = \beta_d l_d$ allows equation (2.10) to be further simplified to (2.11), [56].

$$Gain = \frac{g_m^2 Zc_g Zc_d}{4} \frac{\left(e^{-N\alpha_g l_g} - e^{-N\alpha_d l_d}\right)^2}{\left(e^{-\alpha_g l_g} - e^{-\alpha_d l_d}\right)^2} \tag{2.11}$$

For an ideal case where the DA losses are neglected, the gain equation (2.11) can be reduced to (2.12)

$$Gain = \frac{g_m^2 Zc_g Zc_d N^2}{4} \tag{2.12}$$

Several interesting aspects of the distributed amplifier can be deduced from the gain expression of (2.11) and (2.12), as follows. From Equation (2.11), for a lossless distributed amplifier, the gain increase as N^2. When loss is present, Equation (2.11) specify that gain approaches zero as N tends to infinity. This behavior is explained by the fact that the input voltage on the input-loaded line decays exponentially. The same applies for the output-loaded line. Thus, the FET at the end of the amplifier receive no input signal.

Those imply that, for a given set of transistor parameters, there will be an optimum value of N that maximizes the gain of the amplifier. This can be found by differentiating (2.11) with respect to N and setting the result to zero to obtain (2.13).

$$N_{opt} = \frac{ln\left(\alpha_g l_g / \alpha_d l_d\right)}{\alpha_g l_g - \alpha_d l_d} \tag{2.13}$$

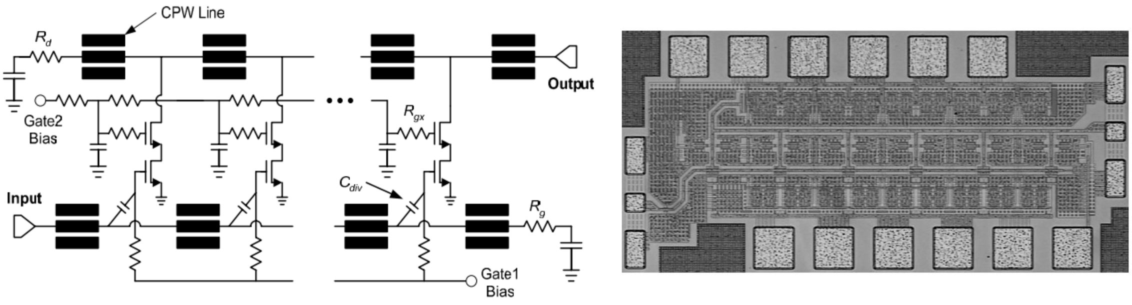
This result (2.13) depends on the frequency, the Gm-cell parameters and the line lengths through the attenuation constants given in (2.4) and (2.5).

2.3.3 Performance Demonstration through Different Technologies and Topologies

Distributed amplification topic received popularity between amplifier-research community as being a promising candidate for breaking restrictions on upper frequency limit. Owing to that, a noticeable amount of research work was made public demonstrating the versatility of DA in different IC technology processes from Si, SiGe and compound III-V technologies, such as InP and InGaAs. The common objective between those works, as was also stated by the authors, was presenting the possible performances from gain, bandwidth and P_{DC} one is capable of reaching through each technology. In this section, a handful of design examples that illustrates optimum performance in each technology is provided. Those designs are sorted out on the basis of their GBP achievements before their electrical performance are finally summarized in a state-of-the-art table for tradeoffs comparison in subsection 2.3.4. Only single stage DAs are duly presented herein for state-of-the-art relevance, excluding any cascaded DA configurations where achievable gains are inherently higher. Nonetheless, the later are introduced in Table 2.2 and their interest is justified with the discussion that follows it.

2.3.3.1 A 4-91 GHz Bandwidth Distributed Amplifier in 90-nm Si CMOS [30]

This article presents the design of a CMOS-based DA implemented in silicon 90-nm process node. This technology is benchmarked at f_t = 160 GHz and f_{max} = 142 GHz. The DA is synthesized with six unit-cells. Figure 2.20(a) illustrates its circuit diagram and Figure 2.20(b) its microphotograph for on-wafer characterization. The fabricated circuit occupies a chip area of 0.6 × 1.2 mm^2 including pads. The conventional cascode topology with a two-transistor configuration was adopted for the Gm-cell and coplanar waveguide (CPW) was used for realizing inductive-type segments instead of conventional microstrip lines. Authors explain that with their back-end technology, they could guarantee lower losses at high frequency using CPW topology.



(a) (b)

Figure 2.20: Six unit-cells 90-nm Si CMOS-based distributed amplifier. (a) Schematic diagram. (b) Microphotograph. [30]

Referring to Figure 2.21, the measured S-parameters performance against frequency is shown. Their six-unit cell DA achieves a peak gain of 7.4 dB with a 3-dB bandwidth of 80 GHz. This results in a GBP of 190 GHz. The amplifier consumes 120 mW from a 2.4-V power supply. The measured output and input return losses across the 3-dB bandwidth reaches a maximum of -10 dB. The reverse isolation is better than -20 dB for the whole passband region.

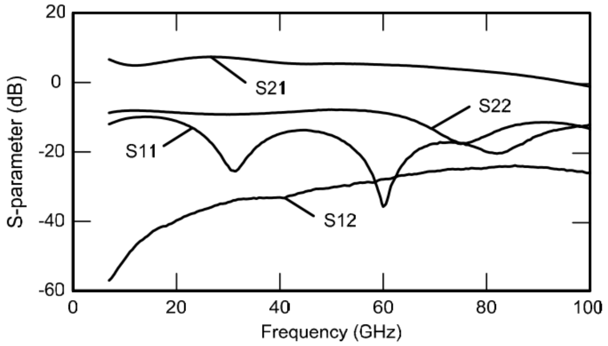
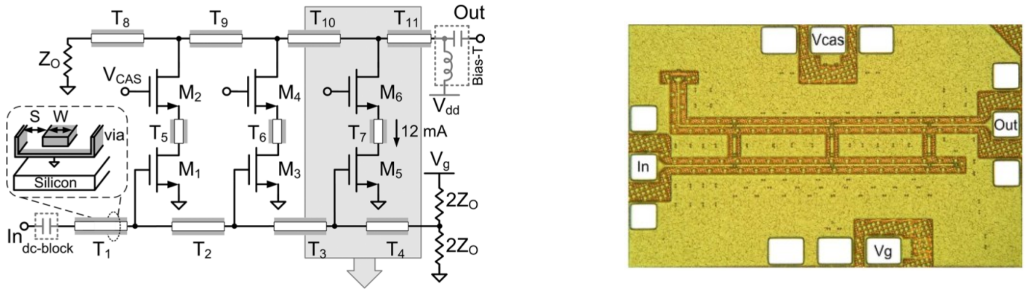


Figure 2.21: Measured S-parameters of the 90-nm Si CMOS-based distributed amplifier. [30]

2.3.3.2 A 92-GHz Bandwidth Distributed Amplifier in 45-nm SOI CMOS [31]

This article presents the design of a CMOS-based DA implemented in silicon-on-insulator (SOI) 45-nm process node. This technology is benchmarked at f_t = 350 GHz and f_{max} = 300 GHz. The DA is synthesized with three unit cells. Figure 2.22(a) shows the schematic diagram of the device and Figure 2.22(b) shows its microphotograph for on-wafer characterization. The fabricated circuit occupies a chip area of 0.5 × 0.8 mm^2 including pads. The Gm-cell adopted is based on a cascode topology with a two-transistor configuration and the inductive-type segments are conventional microstrip lines.



(a) (b)

Figure 2.22: Three unit-cells 45-nm SOI-based distributed amplifier. (a) Schematic diagram. (b) Microphotograph. [31]

Referring to Figure 2.23, the measured S-parameters against frequency are plotted along with the simulated results. The amplifier achieves a 3-dB bandwidth of 92 GHz and a gain of 9 dB with a gain-ripple of ±1.5 dB inside the passband region. This offers an overall gain-bandwidth of 259 GHz. The amplifier consumes 73.5 mW from a 1.2 V supply. The measured input return loss across the entire 3-dB bandwidth is better than -10 dB, but remains better than -15 dB below 70 GHz. The measured output return losses across the 3-

dB bandwidth is less than -6 dB but remains better than -10 dB below 84 GHz. The reverse isolation is -15 dB at 88 GHz and better than -20 dB below 70 GHz.

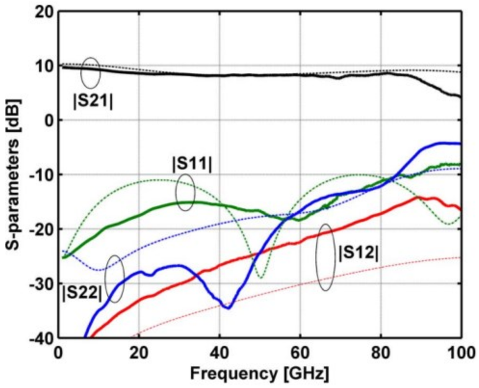
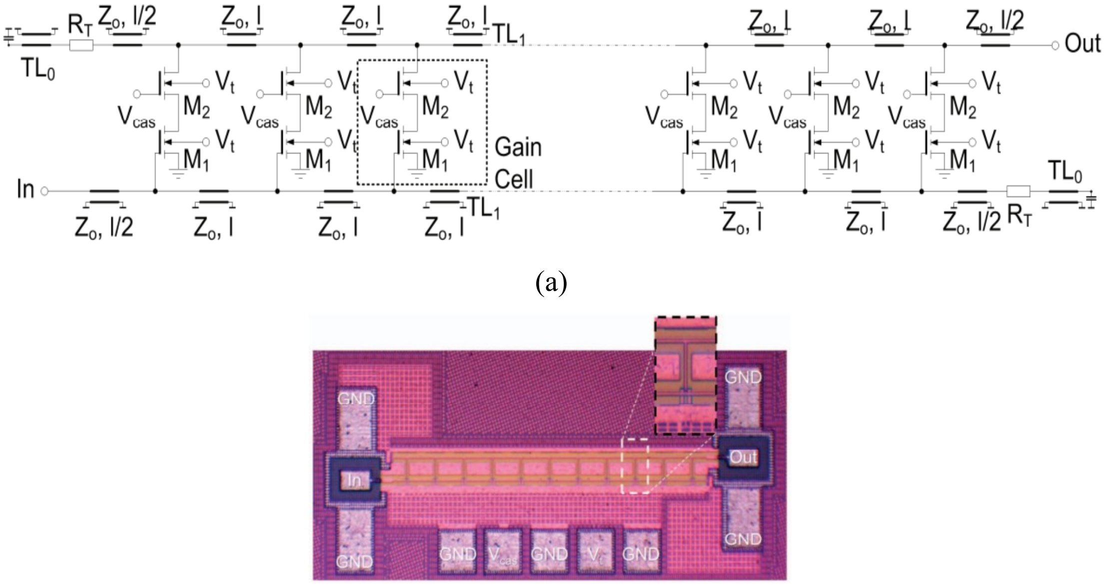


Figure 2.23: Measured (solid lines) and simulated (dotted lines) S-parameters of the 90-nm Si CMOS-based distributed amplifier. [31]

2.3.3.3 A 110-GHz Bandwidth Distributed Amplifier in 22-nm FD-SOI CMOS [32]

This article presents the design of a CMOS-based DA implemented in fully-depleted silicon-on-insulator (FD-SOI) 22-nm process node. This technology is benchmarked at f_{max} = 396 GHz (authors did not provide value for f_t). The DA is synthesized using eleven unit cells. Figure 2.24(a) shows the schematic diagram of the device and Figure 2.24(b) shows its microphotograph for on-wafer characterization. The chip occupies an area of 0.38 × 1 mm^2 including the pads. The Gm-cell adopted is based on a cascode topology with a two-transistor configuration and the inductive-type segments are conventional microstrip lines.



(a)

(b)

Figure 2.24: Eleven unit-cells 22-nm FD-SOI-based distributed amplifier. (a) Schematic diagram. (b) Microphotograph. [32]

Referring to Figure 2.25, the measured S-parameters against frequency are plotted along with the simulated results. The amplifier achieves a 3-dB bandwidth of 110 GHz and a gain of 8.5 dB. This offers an overall gain-bandwidth of 292 GHz. The amplifier consumes 80 mW from a 2-V supply. The magnitude of the input and output return losses are both better than -15 dB for the whole amplifier bandwidth.

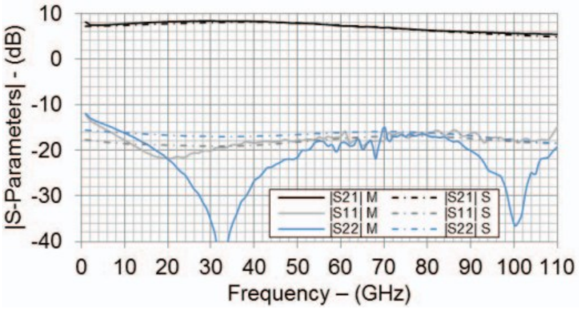
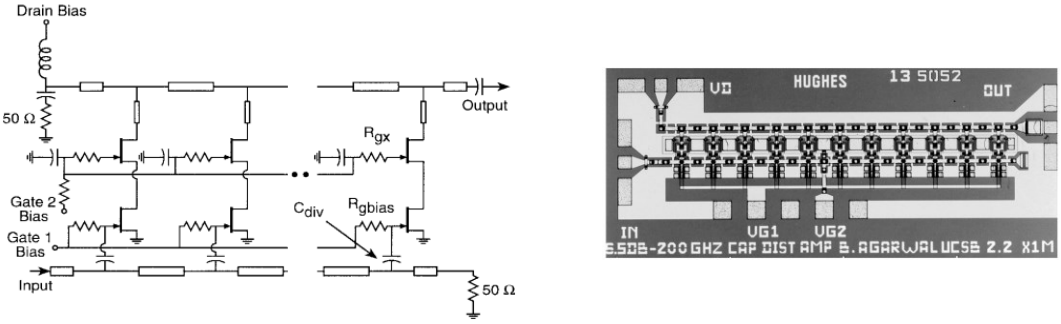


Figure 2.25: Simulated and measured S-parameters of 22-nm FD-SOI-based distributed amplifier. [32]

2.3.3.4 A 112-GHz, 157-GHz, and 180-GHz Bandwidth Distributed Amplifier in 100-nm InP HEMT [33]

This article presents the design of a high-electron-mobility transistor (HEMT)-based DA implemented in 100-nm gate length InGaAs/InAlAs technology. This technology is benchmarked at f_t = 160 GHz and f_{max} = 300 GHz. It demonstrates the capability of such technology by synthesizing three DAs with different bandwidths: A 1-112 GHz, 1-157 GHz, and a third amplifier with 5-dB gain and a 180-GHz high-frequency cutoff. Figure 2.26(a) shows the schematic circuit diagram of the DA. The cascode topology with a two-transistor configuration and conventional μ-TL line for the inductive segments were adopted as unit-cell Gm-cell. Figure 2.26(b) shows the microphotograph of the fabricated chip of 1-157 GHz DA. It consists of eleven unit cells and the die size is about 1 × 2.2 mm^2 including pads.

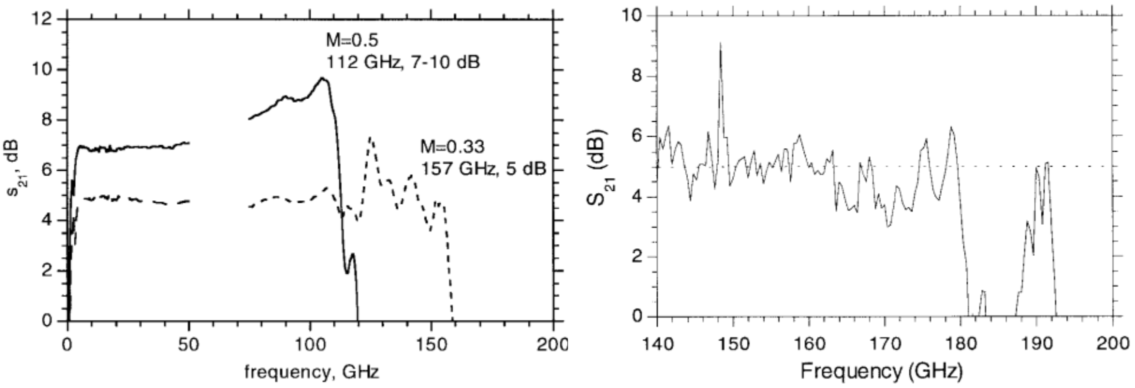


(a) (b)

Figure 2.26: Eleven unit-cells 100-nm InP-based distributed amplifier. (a) Schematic diagram. (b) Microphotograph of the 1-157-GHz version. [33]

Referring to Figure 2.27, measured insertion gain (S_{21}) for all three DAs against frequency are plotted. From Figure 2.27(a), the 1-112 GHz and 1-157 GHz DAs provide

7 dB and 5 dB of gain, respectively. The third DA, with 180 GHz cutoff frequency provides 5 dB of gain as shown in Figure 2.27(b). Those offer an overall gain-bandwidth of 248 GHz, 277 GHz and 320 GHz, respectively. The authors did not provide data for power consumptions.

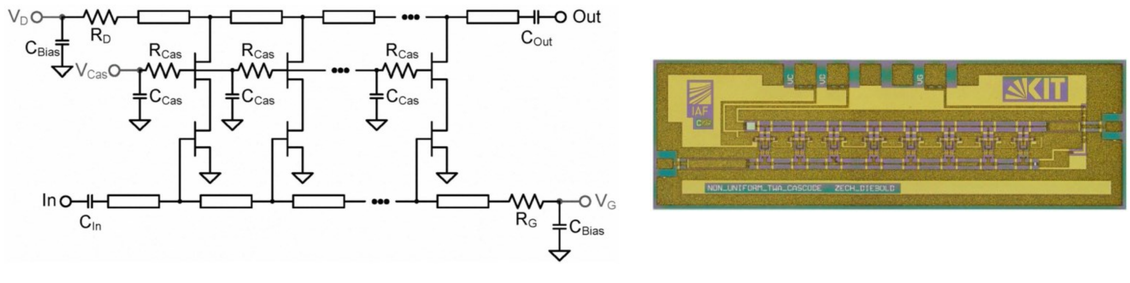


(a) (b)

Figure 2.27: Measured insertion gain of (a) 1-112 GHz and 1-157 GHz, and (b) 180 GHz 100-nm InP-based distributed amplifiers.[33]

2.3.3.5 A 105-GHz Bandwidth Distributed Amplifier in 50-nm InGaAs mHEMT [34]

This article presents the design of a metamorphic HEMT-based DA implemented in 50-nm InGaAs technology. This technology is benchmarked at f_t = 380 GHz and f_{max} = 500 GHz. The DA fabricated consists of eight unit cells. Figure 2.28(a) illustrates the schematic circuit diagram. The Gm-cell adopted was based on cascode topology with a two-transistor configuration and conventional μ-TL line was used for the inductive-type segments. Figure 2.28(b) illustrates the microphotograph of the implemented DA. The die size is 0.75 × 2.25 mm^2.



(a) (b)

Figure 2.28: Eight unit-cells 50-nm InGaAs-based distributed amplifier. (a) Schematic diagram. (b) Microphotograph. [34]

Referring to Figure 2.29, the measured S-parameters against frequency are plotted. The DA covers a 3-dB bandwidth of 110 GHz with 11 dB of gain while consuming a total of 450 mW from a 6-V supply voltage. This leads to a GBP of 373 GHz. The passband region experiences a gain-ripple of around ±1 dB from 5 GHz to 110 GHz. The gain peak, in the frequency range from 2 GHz to 5 GHz, is caused by the inductive feed of the DC bias voltages used for on-wafer measurements. The input return loss is below -10 dB from 10

GHz up to 110 GHz with a maximum of -5 dB for frequencies below 10 GHz. The output return loss is below - 7.5 dB from 5 GHz up to 100 GHz.

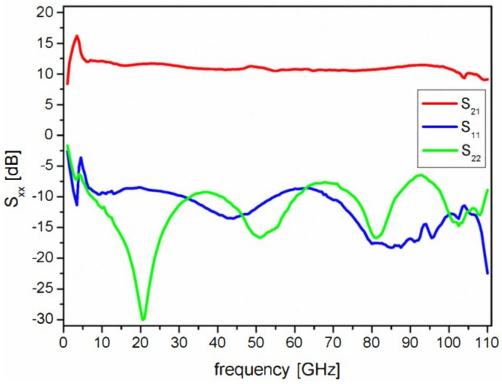
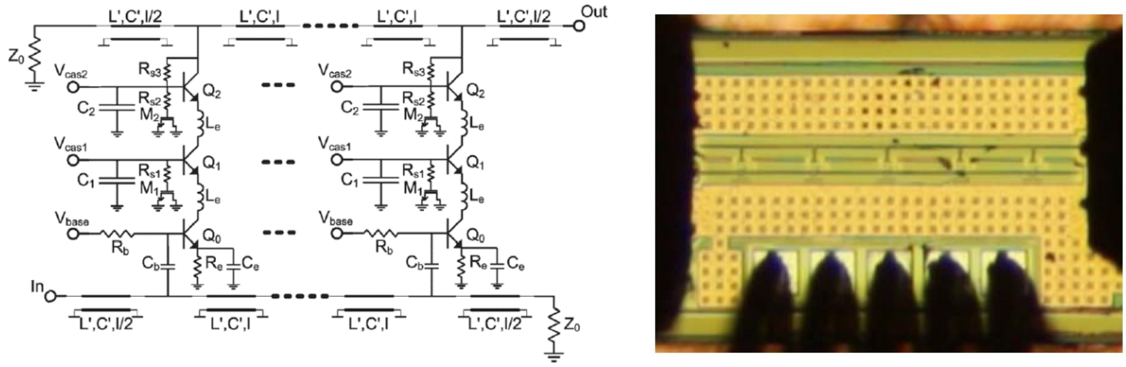


Figure 2.29: Measured S-parameters of 50-nm InGaAs-based distributed amplifier. [34]

2.3.3.6 A 170 GHz Bandwidth Distributed Amplifier in 130-nm SiGe HBT [35]

This article presents the design of a HBT-based DA implemented in 130-nm SiGe-BiCMOS technology. This technology is benchmarked at f_t = 300 GHz and f_{max} = 500 GHz. The DA fabricated consists of five unit cells and the Gm-cell adopted is based on cascode topology with a three-transistor configuration to increase voltage swing and hence output power. Slow-wave μ-TL line topology was used for the inductive-type segments to reduce lines length. The cascode is designed to compensate the transmission-line-losses at high frequencies in order to extend the bandwidth as well as the GBP. Figure 2.30(a) and Figure 2.30(b) illustrate the schematic circuit diagram and the microphotograph of the implemented DA. The chip occupies an area of 0.85 × 0.45 mm^2 including pads.



(a) (b)

Figure 2.30: Five unit-cells 130-nm SiGe-based distributed amplifier. (a) Schematic diagram. (b) Microphotograph. [35]

Referring to Figure 2.31, the simulated and measured S-parameters against frequency are plotted. The amplifier provides a gain of 10 dB up to a 3-dB bandwidth of 170 GHz. It consumes a total of 108 mW FoM a 3.6-V supply. This leads to a GBP of 537 GHz. The passband region experiences a gain-ripple of ±2 dB. The input return loss is below -20 dB up to 100 GHz and then it increases with frequency reaching a maximum of -5 dB at 170 GHz. The output return loss is below -20 dB up to a higher frequency of around 140 GHz and then it starts to increase reaching a maximum of -5 dB at 170 GHz.

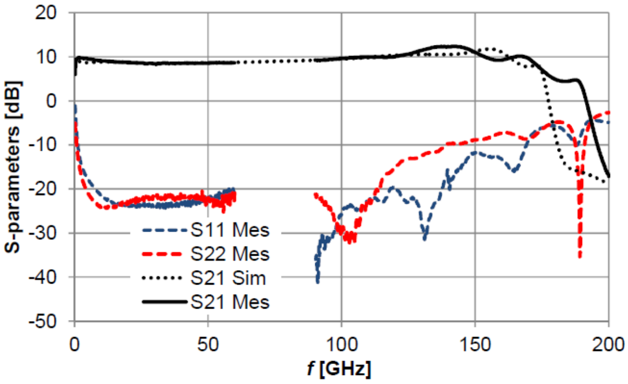
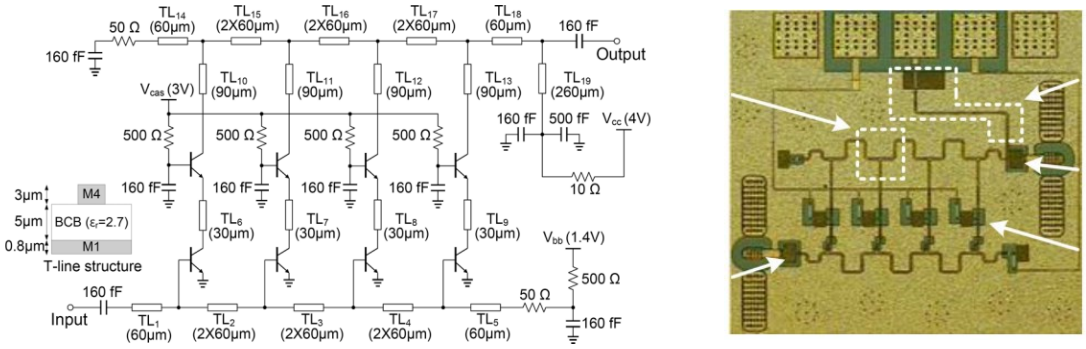


Figure 2.31: Simulated and measured S-parameters of 130-nm SiGe-based distributed amplifier. [35]

2.3.3.7 A 40-222 GHz Bandwidth Distributed Amplifier in 250-nm InP HBT [36]

This article presents the design of an HBT-based DA implemented in 250-nm indium phosphide (InP) technology. This technology is benchmarked at $f_t \geq 375$ GHz and $f_{max} \geq 650$ GHz. The fabricated DA consists of four unit cells and the Gm-cell adopted is based on cascode topology with a two-transistor configuration with conventional µ-TL topology for the inductive segments. Figure 2.32(a) and Figure 2.32(b) illustrate the schematic circuit diagram and the microphotograph of the implemented DA. The chip occupies an area of 0.546 × 0.602 mm^2 including pads.



(a) (b)

Figure 2.32: Four unit-cells 250-nm InP-based distributed amplifier (a) schematic diagram and (b) microphotograph. [36]

Referring to Figure 2.33, the measured S-parameters against frequency with simulation results superimposed are plotted. The amplifier provides a nominal gain of 10 dB with 3-dB bandwidth extending from 40 GHz to 222 GHz, resulting in the highest 3-dB bandwidth of 182 GHz reported thus far. It should be reminded that bandwidth is considered here and not upper operating cutoff-frequency. The passband region experiences a gain-ripple of ±2 dB. The circuit consumes a total of 105 mW FoM a 4-V supply. This leads to a GBP of 575

GHz. The input return loss is below -10 dB from 40 GHz up to 22 GHz. The output return loss is below -10 dB from 90 GHz to 210 GHz. The authors state that the degradation in output return loss below 90 GHz is attributed to the on-chip dc bias network.

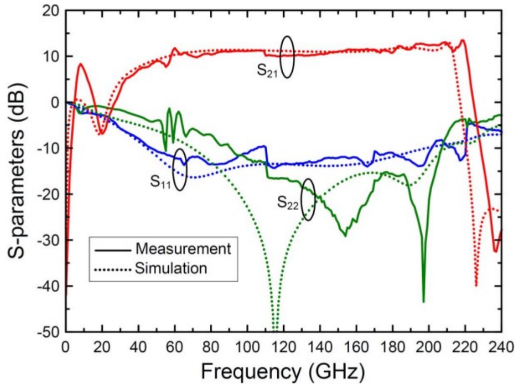


Figure 2.33: Simulated and measured S-parameters of 250-nm InP-based distributed amplifier. [36]

2.3.4 State-of-the-Art Table on Distributed Amplifiers

Previously described distributed amplifiers, with extra ones reported for their relevance with this thesis work, are listed in the state-of-the-art table, Table 2.2. The purpose of this table is to summarize the design tradeoffs between integrated technologies when addressing the subject of UWB amplification using DAs. In addition, it will serve us as a reference for later benchmarking when characterizing our own fabricated circuit prototypes.

It is true that the GBP is an appropriate figure-of-merit (FoM) to evaluate the level of improvement offered by a given proposal when pushing the limitation on gain and bandwidth, as demonstrated in Section 2.2; however, the amount of delivered gain per milliwatt of consumption is also an important merit to consider for low-power applications. To account for this design tradeoff and ease of comparison, we define the following new figure of merit (2.14):

$$FoM_1 = \frac{GBP}{P_{DC}} = \frac{Gain \cdot Bandwidth}{P_{DC}} \quad (GHz/mW) \tag{2.14}$$

Surface area could also be of particular interest for some analog designers and distributed amplifier are not far from reserving relatively larger on-chip area compared to other amplifier topologies as an expense for its wider bandwidth. To highlight the area efficiency, we also define the following figure of merit (2.15):

$$\begin{aligned} FoM_2 &= \frac{GBP}{P_{DC} \cdot Area} \\ &= \frac{Gain \cdot Bandwidth}{P_{DC} \cdot Area} \quad (GHz/(mW \cdot mm^2)) \end{aligned} \tag{2.15}$$

In this thesis, our emphasis is placed on (2.14). We believe that area reserved by an amplifier, or any integrated circuit in a general context, is highly dependent on the process technology node, where smaller nodes tend to be more efficient in occupied area than larger nodes. In addition, it depends on the design rule restrictions that accompanies a given process, where nodes having stringent density rules can lead to large area than less restrictive nodes. We also believe that the amount of surface area occupied is ultimately influenced by the end-objective of the designer circuit prototype; it depends on what design characteristic the designer opted his efforts on and providing improving for the research community.

Table 2.2 compares results from state-of-the-art FET- and HBT- based DAs. HBT-based DAs, [35], [36], [48], [49], have been reported to provide larger bandwidths, beyond 100 GHz, thereby contributing to a much higher GBP merit. This is due to HBTs impressive cutoff frequencies [14], [15] compared to their cheaper CMOS counterparts. In addition, due to the bipolar transistor capability in providing much higher transconductance, bipolar-based DAs provide much higher gain for relatively similar P_{DC}, in the hundreds milliwatt, to the other technology processes. This can explain their higher GBP/P_{DC} merit. In terms of surface area reservation, they also present higher $GBP/(P_{DC} \cdot Area)$ merit. This is also due to its advantageous transconductance. For instance, for a similar gain of around 10 dB, [35] implemented a five unit-cells HBT-based DA while [44] implemented a nine unit-cells CMOS-based DA.

Analyzing the design tradeoffs between FET-based DAs, III-V technologies [33], [34], [46], [47] offer superior GBP merit than silicon semiconductor technologies. This is due to their high electron mobility, but at the expense of much larger P_{DC}, which is why they present low GBP/P_{DC} merit and, hence, could be considered as not appropriate for applications where low power consumption is critical.

Analyzing the performances of the CMOS-based DAs, using the cheap silicon technology, such as in [30], [31], [44], [45], they do offer comparable gain with bandwidths reaching above 70 GHz. In order to boost their relative low gain and obtain much higher GBP/P_{DC} performance, [41] and [42] demonstrate the technique of cascading multiple single-stage DAs. This technique helps in rising the GBP merit; for example, for the same 90-nm process node, [42] demonstrates an excess of two-fold improvement in their cascaded DA circuit compared to[30] that implemented just a single-stage DA circuit.

A final observation worth highlighting is that all of the mentioned state-of-the-art DAs here have adopted a cascode topology for their Gm-cell when synthesizing their unit cell. This is even perceptible through the schematic diagrams of each research work discussed in previous subsection 2.3.3, where the most common configuration is a cascode made of two transistors. This could advocate the easiness that follows from implementing a cascode topology where the purpose of adding the upper transistor is to mitigate the Miller effect that results from the input-to-output overlap capacitance of the lower transistor. It also advocates for its capability in being a suitable solution to provide gain for mm-wave signals. For this reason, cascode Gm-cell topology will be adopted later when implementing our proper DA circuits, which also would give a fair comparison to the already published state-of-the-art ones.

TABLE 2.2: STATE-OF-THE-ART PERFORMANCES COMPARISON FOR DISTRIBUTED AMPLIFIERS

Ref.	Process Techno.	Gain (dB)	Ripple[£] (dB)	BW[&] (GHz)	Supply (V)	P_{DC} (mW)	GBP (GHz)	$\boldsymbol{\frac{GBP}{P_{DC}}}$ $\boldsymbol{\left(\frac{GHz}{mW}\right)}$	Total Area (mm^2)	$\frac{\text{GBP}}{P_{DC} \cdot \text{Area}}$ $\left(\frac{\text{GHz}}{\text{mW} \cdot \text{mm}^2}\right)$
[30]	90-nm Si CMOS	7.4	-3[%]	80	2.4*	120	188	1.57	0.72	2.18
[41]	90-nm Si CMOS	7[@]	+9[%],-3	70	N/A	122	157	1.29	0.72	1.8
[42]	90-nm digital CMOS	14[@]	±1.5[%]	73.5	1.2*	84	368	4.38	1.72	2.54
[43]	40-nm digital CMOS	15[$]	+5[%],-3	80	(1, 1.7)**	90	450	5	0.31	16.13
[44]	120-nm SOI CMOS	11	±1.2	85	2.5*	210	302	1.44	1.28	1.13
[45]	120-nm SOI CMOS	7.8	±1.3	82	2.6*	130	201	1.55	1.05	1.47
[31]	45-nm SOI CMOS	9	±1.5[%]	92	1.2*	73.5	259	3.52	0.45	7.82
[32]	22-nm FD-SOI CMOS	8.5	-3[%]	110	2*	80	292	3.66	0.38	9.63
[46]	130-nm InP HEMT	14.5[#]	±0.7	94	3*	N/A	499	N/A	2.75	N/A
[33]	100-nm InP HEMT	7	+2.5[%]	111	N/A	N/A	248	N/A	2.2	N/A
[47]	70-nm InP HEMT	21[@]	±3[%]	80	2**	300	898	3	2.47	1.21
[34]	50-nm InGaAs mHEMT	11	±1	105	6*	450	373	0.83	1.69	0.5
[48]	250-nm InP HBT	12.8	+7[%],-2[%]	180	N/A	110	724	6.58	0.32	20.57
[36]	250-nm InP HBT	10	-3	182	4*	105	575	5.47	0.33	16.57
[35]	130-nm SiGe HBT	10	±2[%]	170	3.6*	108	537	5	0.38	13.16
[49]	130-nm SiGe HBT	24[@]	+2.5[%],-1[%]	95	N/A	247	1506	6.09	0.65	9.37

N/A = not available.

[&]BWs are reported as declared by authors. [£]Ripple limits is determined within the authors declared BW for their reported gain.

[%]Estimated from plots [@]Cascaded Multi-stage DA (CMSDA) [$]Cascaded single-stage DA (CSSDA) [#]Flip-Chip DA

[*]Biased using external bias-tee [**]Biased using integrated bias-tee

2.4 Conclusion

This chapter stressed on the importance and the necessity of providing large bandwidth amplifiers in present time due to its rise in value and need in the upcoming future for higher spectrum capacity and data rates reasons. Several amplifier topologies from small to large bandwidth performance were presented, but the choice of study at the end was placed on distributed amplifier device as it showed to be the only design solution that can provide interesting ultra-wide amplification bandwidth. This mainly due to its capability provide impedance matching over an extremely wide frequency range by creating artificial transmission lines through distribution of Gm-cells between inductive-type segments. Its history, principle and technology-process versatility were also presented. From equation (2.11), design complexity was detected where design variables from number of unit cells and dimensions of both Gm-cell and inductive-type segments are correlated, and need to be studied simultaneously to meet multiple design objectives to find the best design.

On that basis, the following tasks are set to be covered in the next chapters of this thesis manuscript:

- Propose a DA model suited for mm-wave application that is considered complete when it comes to describing frequency behaviors, such as gain response, for instance, by taking into account the whole design parameters the conventional DA can be made synthesized from.
- Propose a design methodology, based on our DA model, that demonstrates optimum sizing of DA design parameters that will then assist us in choosing the highest GBP/P_{DC} metric (2.14), a desirable criterion for low-consumption application.
- Finally, validate the proposed design process through on-wafer characterization of both a single-stage and cascaded stages CMOS-based DAs.

In the next chapter, Chapter 3, we begin by discussing the already existing design techniques for DAs and discussing our own newly proposed model.

Chapter 3

Proposition of a Novel Model to Design DAs: the Four-Port Chain (ABCD) Model

In the previous chapter, the topic of DA was introduced. Both its principle of operation and performance abilities with different technology processes were investigated. In this chapter, its design process is discussed. The commonly used techniques are described first, followed by introducing a new design model for DAs that assists in successful realization of CAutoD process and offering a different approach of designing using scripting methods.

This chapter is structured as follows. Section 3.1 starts by stating the requirements for what a proposed physical model is believed to fulfil in order for it to be considered complete and general, suitable for mm-wave IC design. Section 3.2 reviews already existing techniques, from models and methods, suggested for distributed amplifier design. Section 3.3 goes through the limitations those techniques impose, in particular when dealing with operating frequencies reaching into the millimeter spectrum. Section 3.4 introduces a novel matrix-based design model using Chain ($ABCD$) parameters. Finally, Section 3.5 summarizes and concludes this chapter.

3.1 Introduction

For the realization procedure of an IC, an initial step to consider beforehand is the design approach; i.e., how a given circuit will be sized to reach the required performance before being sent to the final stage of fabrication and measurement-based characterization. For a mm-wave IC, the design process starts by having a corresponding physical model, will it be by deriving analytical model or through graphical interface using CAD software, that relates the circuit design variables to its performance characteristics. This aids the designer to have a better understanding on how the circuit works and determining which parameters plays what role on the circuit behavior. For instance, since the discussion is dedicate for DA device, referring to Figure 2.18 the recurrent variables in its design are the number of unit cells (N) and Gm-cell size; by proposing a given type of physical model that relates to its S-parameters, the performance of the DA can be analyzed and used for designing one. The latter parameters set is highlighted since it is popularly used in microwave engineering to describe the electrical behavior against frequency and useful in determining the electrical properties of the circuit at hand such as gain, bandwidth and ports mismatch level.

A detailed inspection of different design techniques that can be used in DA design has been conducted and subsequent Section 3.2 is dedicated to reviewing them. During this inspection process, we took note of criteria we wanted to satisfy as a whole through our own proposed design technique and we listed them here. We deduced that the degree of usability of a design model can be determined through:

- First, how complete it is. This is defined by the amount of variables the model takes into consideration and influences its ability in producing optimum design end-results; when the model is constructed from the complete set of design parameters the circuit is made from, its suggested performance starts to be defined as a global optimum solution rather than a local one. In addition, those amounts of variables influence the number of possible design methodologies a designer produces from it to satisfy different desired performance merits.
- Second, its versatility. A model can be considered general when it can easily be exchanged between technology processes, in addition to having the ability to be adopted to several proposed topologies. That is to say, if a designer is interested in using a different component topology from the one used when producing a given tool, the model should be able to be adapt to the designer needs.
- Third, its complexity. Since this thesis theme is about mm-wave circuits, more parasitic element comes into role and have a dominant impact on the circuit frequency behavior. The attempts to take into account all tiny effects in order for it to be considered accurate to simulate a circuit behavior lead to an excessive complication of the model. This can be observed, for instance, when attempting to derive an analytical-equation based model that represent the frequency behavior for the IC under study through representing first all of its components with their respective complete AC equivalent network.
- Finally, its reliability in simulating the circuit behavior. Again, this is crucial since we are dealing with millimeter IC design; simplifying through neglecting those parasitic elements degrades the overall accuracy of the proposed model, devaluating all results of circuit analysis and thereby rendering it unsuitable for higher frequencies usage.

The target in this thesis is set to take into account those criteria and propose a complete model, without any approximation, for mm-wave DA design. Its main purpose is to be used in scripting-based design technique and successful implementation of computer automation to render the design process simple and fast. Our end-goal is to offer the designer a different and interesting technique (other than conventional analytical approaches) in which the outcome of the suggested CAutoD process is a set of 3D graphical design exploration plots (DSE) plots. Designers then can explore through them different possible solutions and choose the best design that meet their multiple performance objectives.

3.2 Existing Distributed Amplifier Design Techniques

Several design techniques already exists in the literature and usually each proposal comes as an improvement for precedent works. While they are useful for preliminary sizing, they were deduced to be not complete. Each proposed model is based on certain assumptions that makes its outcome correct within design limitations. In addition, they demonstrate a compromise between reliability, complexity and completeness. Simplicity was deduced to be the most preferable through approximation and elements neglecting, which leads to a less reliable model and, thereby, lower optimum performance distant from being considered a global solution choice. This section starts by presenting the most common approach in representing a DA [40], since 1982, and progress through the available improvements until recent day's technique is discussed, in which designers rely more often on CAD tools. In the next section, Section 3.3, their limitations are discussed.

3.2.1 Artificial-Line Based Model [40]

The first physical model proposed for DAs dates back to 1982. It is still being referenced by recent publications [29], [31], [33], [42], [47], [58], [59], while explaining the concept of a DA. It is a set of mathematical equations derived from portraying the input and output loaded lines as artificial lines. Due to this assumption, they refer to their DA as a traveling-wave amplifier. This concept was already described in details in Chapter 2 (Section 2.3) with equation (2.11) derived to model the DA gain behavior with respect to frequency. It was derived while assuming the µ-TL-type segments a unit cell is made from as an equivalent lumped-element circuit with the intrinsic per-unit-length parasitic quantities, i.e. $RLCG$-lumped circuit. In addition, it considers the influence of transistor through its unilateral AC equivalent circuit. To prove the validity of their model, the authors in [40] implemented a $1-$ 13-GHz distributed amplifier using 0.1-mm GaAs process node. Figure 3.1 illustrates the S-parameter results versus frequency through on-wafer characterization. Indeed, their proposed mathematical gain-model is shown to fit their measured DA gain up to 12 GHz.

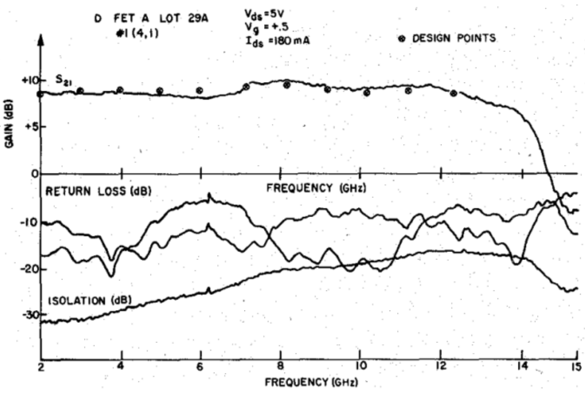
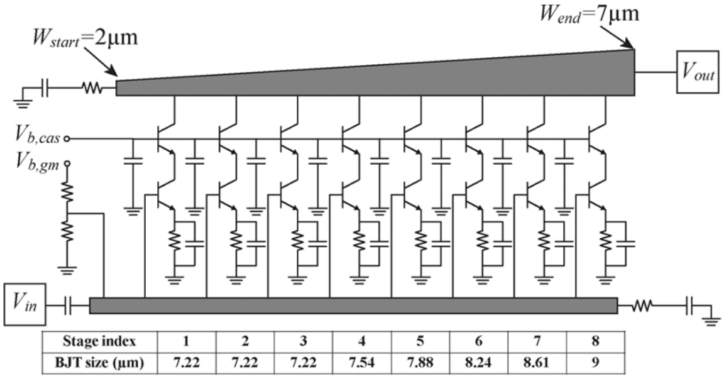


Figure 3.1: Experimental performance of a 0.1-mm GaAs node distributed amplifier at 2–14 GHz frequency range. [40]

3.2.2 Stage-Scaling Based Model [51]

Due to the assumption of artificial lines and identical transistor dimension across all unit cells, the conventional model introduced first is limited only to uniform DAs design. [51] demonstrated a modified version of this analytical-based model where each unit cell is now considered independent and, hence, its own μ-TL-type segments and Gm-cell can be sized differently. Their main objective was to offer a methodology to enhance the power added efficiency (PAE) of DAs. This was achieved through a stage-scaling technique for the output-loaded line to utilize more voltage swing while reducing the total current consumption. The design technique and analysis provided by [51] are derived for bipolar-based DAs, but can as well be adapted to FET-based DAs. In a stage-scaled DA, the loaded collector-line impedance and the transistor size are scaled simultaneously from unit cell to another. Figure 3.2 illustrates such design example implemented by [51]. Both collector-line TL width and cascode transistors sizes are increasing as they approach the last unit cell. It is noticeable for this particular example that the first three stages of the amplifier are not scaled; based on the authors, this is due to the highest T-line impedance achievable on-chip which is restricted by the minimum metal width rule of their process technology. In addition, the base-line TL width is kept the same since negligible current is being consumed and hence no significant enhancement in the PAE of the DA.



Stage index	1	2	3	4	5	6	7	8
BJT size (μm)	7.22	7.22	7.22	7.54	7.88	8.24	8.61	9

Figure 3.2: Schematic diagram of the stage-scaled distributed amplifier. [51]

The wave propagation constant, derived by [51], describing the output-loaded line is given by (3.1a). It is noticeable how the scaling process is achieved through introducing the design term $\eta_{c,i}$ (3.1b); where i^{th} is the position of the unit cell. It is defined as the ratio between the intrinsic and loaded collector-line characteristic impedance, denoted by $Z_{C0,i}$ (3.1c) and $Z_{C,i}$ (3.1d), respectively. The terms R_{cl}, C_{cl} and L_{cl} represent the equivalent $RLCG$-element circuit of the μ-TL-type segments, and C_{out} and G_{out} represent the output complex impedance of the Gm-cell device used.

$$\gamma_{c,i} = \alpha_{c,i} + j\beta_{c,i} \tag{3.1a}$$

$$= \frac{1}{2l_{c,i}}\left(\frac{\eta_{c,i}}{\eta_{c,i}^{2}-1}\nu_{c,i}R_{cl,i}C_{out}k^{N-i} + Z_{c,i}G_{out}k^{N-i}\right)$$

$$+ j\omega\sqrt{L_{d,i}\left(C_{cl,i}+\frac{C_{out,i}}{l_{c,i}}\right)}$$

$$\eta_{c,i} = \frac{Z_{c0,i}}{Z_{c,i}} \tag{3.1b}$$

$$Z_{c0,i} = \sqrt{\frac{R_{cl,i}+j\omega L_{cl,i}}{G_{cl,i}+j\omega C_{cl,i}}} \approx \sqrt{\frac{L_{cl,i}}{C_{cl,i}}} \tag{3.1c}$$

$$Z_{c,i} \approx \sqrt{\frac{L_{cl,i}}{C_{cl,i} + {C_{out,i}}/{l_{c,i}}}} \tag{3.1d}$$

Assuming phase synchronization between output and input lines, i.e., $\beta_c l_c = \beta_b l_b$, the total output voltage swing arriving at the load is found to be (3.2). The terms Z_L and I_c are the impedance and DC-current of the last unit cell. The term "k" is the scaling factor for both the transistor size and the dc-bias current between two adjacent unit cells in the direction from the output to the input. The term "z" is the scaling factor of the loaded collector-line impedance seen by the Gm-cell between two adjacent unit cells in the same direction.

$$V_{out} = \sum_{n=1}^{N}\frac{1}{2}I_c Z_L (k^2 z)^{\frac{N-n}{2}} exp\left(-\sum_{i=n}^{N}\alpha_{c,i}l_{c,i}\right) \tag{3.2}$$

Indeed, through the suggestion of (3.2), higher degree of design freedom is possible since more variables are available and each unit cell is treated independently. This also results in the ability to explore a broader range of performance solutions compared to [40].

3.2.3 Distributed-Line Based Model [52]

The physical model provided by [52] comes as an improvement for both [40] and [51] models. Contrary to traditional ways of treating the unit-cell µ-TL-type segments as equivalent $RLCG$-lumped circuit, [52] treats each segment as a real microstrip line with its own distributed effect. Through this change, propagation and mismatch impact between inter-cells are now taken into considered. This provides an extra degree of accuracy when performing preliminary sizing, since a more realistic representation of the TL losses is now considered. In addition, [52] treats the distributed amplifier as a discrete set of cells connected together, contrary to the continuous artificial line concept of [40] and [51]. This treatment is considered a more realistic approach, since in practice the Gm-cells induce amplification at specific discrete positions (nodes) between the input to output loaded-line; therefore, it will lead to a more reliable representation of the DA amplification response.

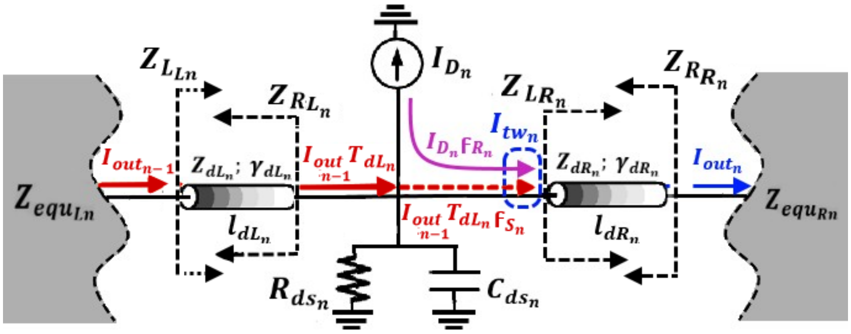


Figure 3.3: Equivalent circuit of the output loaded-line side of the nth unit cell. [52]

Figure 3.3 illustrates the equivalent AC model of the output loaded-line side of a single unit cell made from a FET-based Gm-cell. The output port of the Gm-cell is depicted by a voltage-controlled current source with a complex parallel RC-impedance denoted by R_{ds_n} and C_{ds_n}. The Gm-cell is connected in the middle of two μ-TLs-type segments denoted by subscripts 'L', for left side, and 'R', for right side. The influence of the preceding and subsequent unit cells is taken into consideration in this illustration, as they will affect the total output current generated by the unit cell under study. The latter is done as follows. Equivalent impedances Z_{equL_n} and Z_{equR_n} model all the unit-cells seen on the left and right sides, respectively, of the n^{th} unit cell under study. Current $I_{out_{n-1}}$, flowing from the left side, represents the total current wave generated by the preceding cells traveling towards the right side. Impedance $Z_{L_{Ln}}$ represents the input impedance seen by the μ-TL-type segment ($Z_{d_{Ln}}$,$\gamma_{d_{Ln}}$) on its left side towards its right side while being loaded on its right side by impedance $Z_{L_{Rn}}$ in parallel with output impedance of the Gm-cell (R_{ds_n}, C_{ds_n}). Impedance $Z_{L_{Rn}}$ represents the input impedance seen by the μ-TL-type segment ($Z_{d_{Rn}}$, $\gamma_{d_{Rn}}$) on its left side towards its right side while being loaded on its right side by Z_{equR_n}. Impedance $Z_{R_{Rn}}$ represents the input impedance seen by the μ-TL-type segment ($Z_{d_{Rn}}$,$\gamma_{d_{Rn}}$) on its right side towards its left side while being loaded on its left side by impedance $Z_{R_{Ln}}$ in parallel with output impedance of the Gm-cell (R_{ds_n}, C_{ds_n}). Impedance $Z_{R_{Ln}}$ represents the input impedance seen by the μ-TL-type segment ($Z_{d_{Ln}}$, $\gamma_{d_{Ln}}$) on its right side towards its left side while being loaded on its left side by Z_{equL_n}.

Based on this configuration and applying Kirchhoff's laws and microwave TL theory, the total current wave traveling towards the right side of the nth Gm-cell, I_{tw_n}, is expressed as (3.3);

$$I_{tw_n} = -I_{D_n}\mathsf{F}_{R_n} + I_{out_{n-1}}\mathsf{F}_{S_n}T_{dL_n} \tag{3.3}$$

where F_{R_n} represents how much current generated by the nth current source, I_{D_n}, is incident on the right TL, and is calculated from (3.4);

$$\mathsf{F}_{R_n} = \frac{Z_{R_{Ln}}R_{ds_n}}{(1 + j\omega R_{ds_n}C_{ds_n})Z_{R_{Ln}}Z_{L_{Rn}} + (Z_{R_{Ln}} + Z_{L_{Rn}})R_{ds_n}} \tag{3.4}$$

and f_{S_n} represents the splitting current factor between the right part of the n$^{\text{th}}$ Gm-cell, just before the right TL (Z_{dR_n}, γ_{dR_n}), and the dissipated part in the transistor drain impedance, as given by (3.5);

$$\mathrm{f}_{S_n} = \frac{R_{ds_n}}{\left(1 + j\omega R_{ds_n} C_{ds_n}\right) Z_{L_{Rn}} + R_{ds_n}} \tag{3.5}$$

Finally, the term T_{dL_n} is the n$^{\text{th}}$ left µ-TL-type segment (Z_{dL_n},γ_{dL_n}) transmission coefficient which takes into account the multiple reflections that occur at its boundaries. T_{dL_n} can be calculated using (3.6a) on the basis of Figure 3.3;

$$T_{dL_n} = \frac{\left(1 + \Gamma_{in_{dLn}}\right)\left(1 + \Gamma_{out_{dLn}}\right) e^{-\gamma_{d_{Ln}} l_{d_{Ln}}}}{1 + \Gamma_{in_{dLn}} \Gamma_{out_{dLn}} e^{-2\gamma_{d_{Ln}} l_{d_{Ln}}}} \tag{3.6a}$$

$$\Gamma_{in_{dLn}} = \frac{Z_{L_{Ln}} - Z_{d_{Ln}}}{Z_{L_{Ln}} + Z_{d_{Ln}}} \tag{3.6b}$$

$$\Gamma_{out_{dLn}} = \frac{Z_{d_{Ln}} - Z_{R_{Ln}}}{Z_{d_{Ln}} + Z_{R_{Ln}}} \tag{3.6c}$$

In order to determine the amount of current that a given n$^{\text{th}}$ unit-cell transmits to the entire right-side unit cells, represented by an equivalent impedance Z_{equR_n} in Figure 3.3, the transmission coefficient of the right µ-TL-type segment (Z_{dR_n}, γ_{dR_n}) is introduced to the input current expressed in (3.3), and hence the total output current comes to (3.7);

$$\begin{aligned} I_{out_n} &= I_{tw_n} T_{dR_n} \\ &= -I_{D_n} \mathrm{f}_{R_n} T_{dR_n} + I_{out_{n-1}} \mathrm{f}_{S_n} T_{dL_n} T_{dR_n} \end{aligned} \tag{3.7}$$

where the transmission coefficient T_{dR_n} stands for the n^{th} right µ-TL-type segment (Z_{dR_n}, γ_{dR_n}) and is calculated using (3.8a);

$$T_{dR_n} = \frac{\left(1 + \Gamma_{indR_n}\right)\left(1 + \Gamma_{outdR_n}\right) e^{-\gamma_{dR_n} l_{dR_n}}}{1 + \Gamma_{indR_n} \Gamma_{outdR_n} e^{-2\gamma_{dR_n} l_{dR_n}}} \tag{3.8a}$$

$$\Gamma_{in_{dRn}} = \frac{Z_{L_{Rn}} - Z_{d_{Rn}}}{Z_{L_{Rn}} + Z_{d_{Rn}}} \tag{3.8b}$$

$$\Gamma_{out_{dRn}} = \frac{Z_{d_{Rn}} - Z_{R_{Rn}}}{Z_{d_{Rn}} + Z_{R_{Rn}}} \tag{3.8c}$$

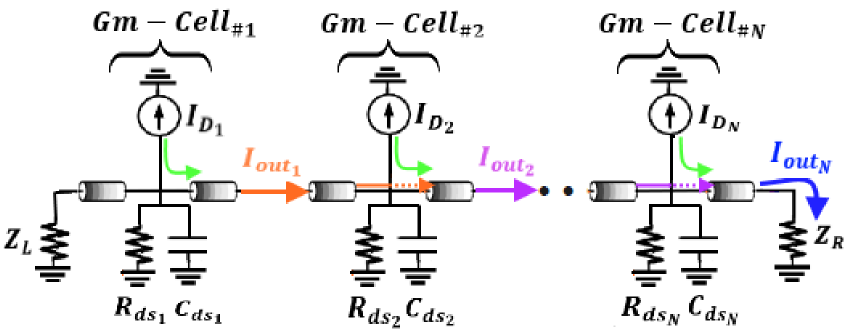


Figure 3.4: Distributed amplifier output loaded-line equivalent circuit representation. [52]

Figure 3.4 demonstrates the case where N unit cells are distributed. By developing (3.7), a non-closed-form model for the total output current generated from the output loaded-line of the DA is expressed in (3.9). The term $\delta_{\langle i,n\rangle}$ represents the "Kronecker" delta.

$$I_{out} = \sum_{n=1}^{N} -I_{D_n}\left[\prod_{i=n}^{N}\left(T_{dR_i}\mathsf{F}_{R_i}\right)^{\delta_{\langle i,n\rangle}}\left(\mathsf{F}_{S_i}T_{dL_i}T_{dR_i}\right)^{1-\delta_{\langle i,n\rangle}}\right] \tag{3.9}$$

For the gate line analysis, a similar approach to that of the drain line analysis was applied. Based on Figure 3.5, the gate side of the Gm-cell is depicted as an equivalent impedance of series resistor and capacitor, denoted R_g and C_{gs}, respectively. One can perceive that the input loaded-line is similar to a transmission line periodically loaded by N complex series RC-impedances.

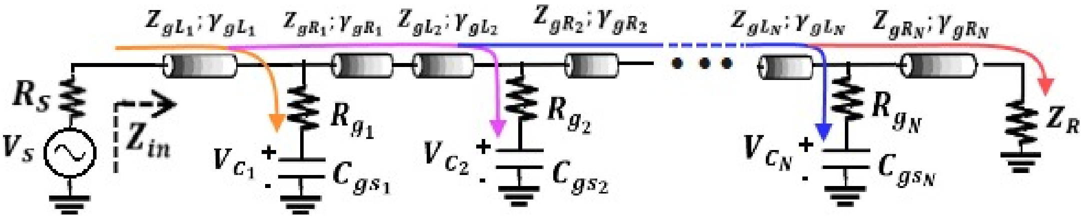


Figure 3.5: Distributed amplifier input loaded-line equivalent circuit representation. [52]

Based on this configuration, the approach was focused on determining the voltage V_{C_n} at each gate-source capacitor C_{gs_n} for the n^{th} unit-cell when a given voltage source V_S is applied (V_{C_n} is the control voltage of the controlled current source I_{D_n} in Figure 3.3). This resulted in the non-uniform capacitor voltage-expression (3.10).

$$V_{C_n} = V_S\left(\frac{Z_{in}}{Z_{in}+R_S}\right)\left(\frac{1}{1+j\omega R_{g_n}C_{gs_n}}\right)\prod_{i=1}^{n}\left[T_{gL_i}T_{gR_i}^{1-\delta_{\langle i,n\rangle}}\right] \tag{3.10}$$

where Z_{in} is the input impedance of the whole DA and R_S is the internal resistance of the signal source. The term T_{gL_i} (T_{gR_i}) is the transmission coefficient of the µ-TL-type segment (Z_{gLn},γ_{gLn}) ((Z_{gRn},γ_{gRn})) which is determined by using the same equations as (3.6a) ((3.8a) respectively) with the boundary reflection coefficients given in (3.11). The same description given to the output-loaded line segments input-impedances ($Z_{L_{Ln}}$, $Z_{R_{Ln}}$, $Z_{L_{Rn}}$,

$Z_{R_{Rn}}$) can be applied to input-loaded line segments input-impedances, the only difference lies in the Gm-cell inherent impedances where previously, for the output side, we were dealing with (R_{ds_n}, C_{ds_n}) in parallel and here, for the input side, we are dealing with (R_{g_n}, C_{gs_n}) in series.

$$\Gamma_{in_{gLn}} = -\frac{Z_{L_{Ln}} - Z_{g_{Ln}}}{Z_{L_{Ln}} + Z_{g_{Ln}}};\ \Gamma_{out_{gLn}} = -\frac{Z_{g_{Ln}} - Z_{R_{Ln}}}{Z_{g_{Ln}} + Z_{R_{Ln}}} \tag{3.11a}$$

$$\Gamma_{in_{gRn}} = -\frac{Z_{L_{Rn}} - Z_{g_{Rn}}}{Z_{L_{Rn}} + Z_{g_{Rn}}};\ \Gamma_{out_{gRn}} = -\frac{Z_{g_{Rn}} - Z_{R_{Rn}}}{Z_{g_{Rn}} + Z_{R_{Rn}}} \tag{3.11b}$$

The parameter linking the output loaded-line, modeled by (3.9), and the input loaded-line, modeled by (3.10), is the transconductance (g_m) of the nth Gm-cell topology used which relates its output current (I_{D_n}) to its input control voltage (V_{C_n}) as given by (3.12).

$$I_{D_n} = g_{m_n} V_{C_n} \tag{3.12}$$

Using equations (3.9), (3.10) and (3.12), the designer can now evaluate more accurately the impact of each design parameter the distributed amplifier is made from, as well as treat each unit cell separately and arrive at the end of the design process to an optimum and more realistic performance.

3.2.4 Artificial Neural Network Based Model

Another modeling technique worth mentioning is through artificial neural network. Since in mm-wave spectrum more elements for representing a certain behavior have to be taken into consideration, the process of deriving equations is shortened through machine learning.

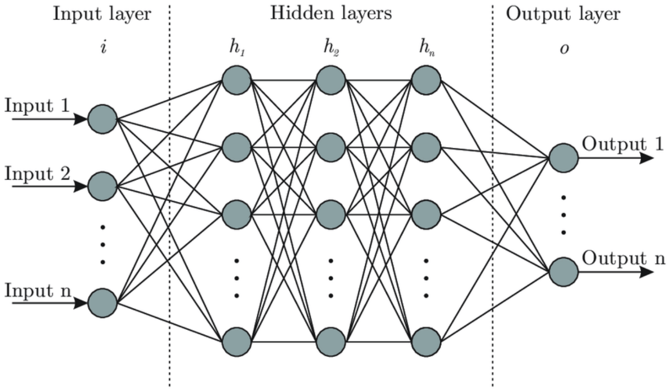
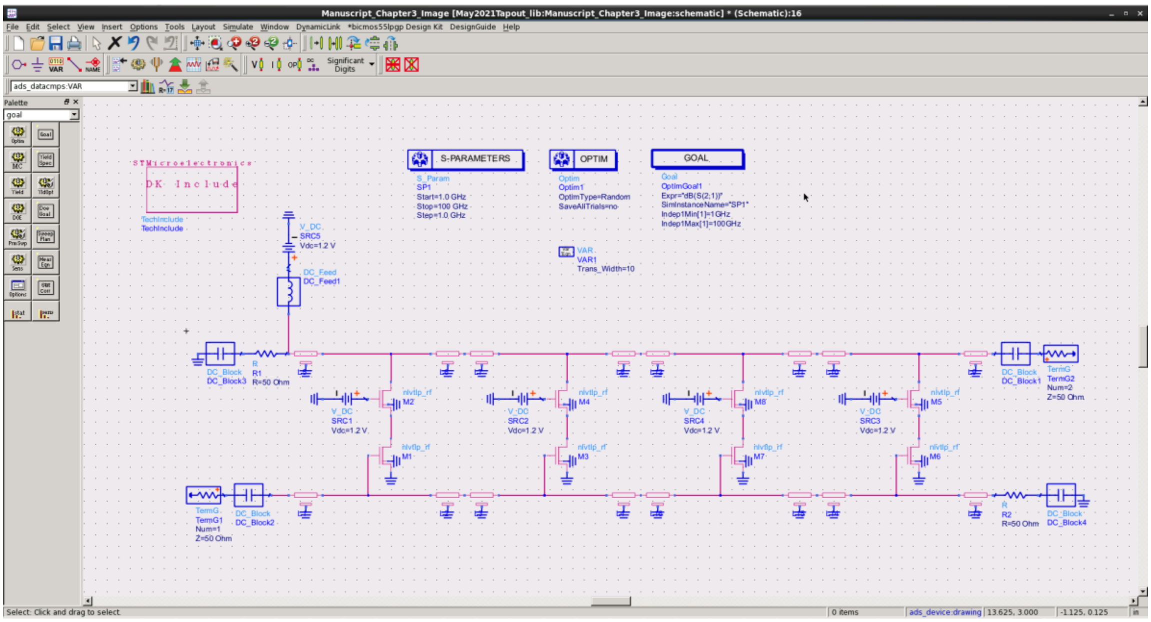


Figure 3.6: Simplified representation of an artificial neural network

Artificial neural network is one topology of machine learning that identifies the relationship (function) between a given set of data and already known outcomes. It does this through artificial intelligence algorithms where they tune its function constants until they find the parameter sets that best matches the training set, i.e., already observed input and output data. Figure 3.6 illustrates an example of a simplified neural network structure. It is made of three layers. The left most side represents its input layer, it is made of a total of i input pins where design parameter set are fed. The right most side represents the output layer, it is made of a total of n output pins; this depends on what the designer is interested in providing as design characteristics. The middle layer is composed of a two-dimensional array of neurons, which are the function constants that will be optimized. After the training stage, the neural network can be used to predict possible characteristic outcomes from a new different input dataset within the possibility of the pre-trained set. Such machine-learning modeling technique has been demonstrated in [53]-[55], for instance, for modeling power-amplifier behaviors. Compared to previously mentioned mathematical equation-based modeling techniques, by using neural network technique there is no need for the designer to be concerned with any tiny effects that impact circuit behavior. Thereby, arguably it could be considered as a simple and fast technique to use during a circuit design process, since it can be considered similar to a multi-variable curve fitting approach. However, it should be highlighted the importance of the pre-training process step needed to make the neural network work. For instance, when dealing with the DA circuit, as a beforehand step the designer needs to simulate several already designed N unit-cells DAs and use those simulations results for the neural network model training (fitting) process. This means that when the model becomes ready to be used again in a new design task, its prediction relies on how adequately the pre-training circuits set were designed. For us, we are interested in providing a design model that discovers the optimum performance (first criterion, Section 3.1).

3.2.5 Widespread Design Technique: Through CAD Software

The final design technique that could be considered the most preferable and reliable way for DAs, or any electronic circuit in a general context, is through a computer-aided design (CAD) software. Traditionally, circuits are first assembled on a graphical user interface by picking the required components from the design library. Then, a set of desired performance goals are defined and the circuit variables intended to be tuned are enumerated. Through the usage of iterative optimization functionality, the CAD software configures automatically those variables through several iterations until the declared goals are fulfilled or closely achieved. This technique is proven to be the most accurate procedure one can have, since no assumption is made, and the closest one in simulating circuit behavior to real-life measured behavior. Several CAD tools exists, but for RF/Microwave integrated circuit design the most famous ones are Keysight ADS and Cadence Virtuoso softwares. Both tools provide fully-custom integrated design environment to designers of RF electronic products such as mobile phones, wireless networks, satellite communications, radar systems, and high-speed data links. They support every step of the design cycle from schematic entry, layout, design rule checking (DRC), frequency-domain and time-domain circuit simulation, and sometimes electromagnetic field simulation, allowing the designer to fully characterize and optimize an RF design without changing CAD platforms. Figure 3.7 provides a demonstrative example of a DA circuit synthesized on ADS software schematic where the transistor sizes are defined as a single variable, and random optimization is being applied until designer-defined gain (S_{21}) goal is reached.


Manuscript_Chapter3_Image [May2021Tapout_lib:Manuscript_Chapter3_Image:schematic] * (Schematic):16

S_Param
SP1
Start=1.0 GHz
Stop=100 GHz
Step=1.0 GHz

Optim
Optim1
OptimType=Random
SaveAllTrials=no

Goal
OptimGoal1
Expr="dB(S(2;1))"
SimInstanceName="SP1"
Indep1Min[1]=1GHz
Indep1Max[1]=100GHz

VAR
VAR1
Trans_Width=10

Figure 3.7: ADS schematic view of a distributed amplifier being optimized to satisfy a defined gain response goal.

3.3 Design Limitations when Operating in mm-Wave Band

Five different techniques where mentioned for DA design. From mathematical-based approaches, to artificial intelligence-based techniques and through schematic-level design environments using CAD tools. However, a set of limitations have been detected for each technique and are described as follows.

First, neglecting the inter-stage propagation, where spacing between individual Gm-cells is assumed small compared with the wavelength of operation (λ_o). This is observed in the first model (subsection 3.2.1) and second model (subsection 3.2.2) through their artificial line assumption. While valid for low frequency of operation, it neglects the transmission line theory for the implemented physical TL spacing that takes effect especially when dealing with DAs extending into the mm-wave region.

Second, neglecting the fact that the Gm-cells embedded between the two lines induce amplification at discrete positions rather than the assumed continuous manner. A limitation also observed in the first two models discussed in Section 3.2.

This pair of limits lead to constraining design formulas usability, and hence the DSE reliability, to only synthesizing DAs that require TL spacing between consecutive Gm-cells with electrical length $(\beta l) \ll \pi/2$, or synthesizing DAs that amplify signals with long wavelengths, in other words DA with smaller bandwidth [56].

Both assumptions were fixed through (3.9) model (Subsection 3.2.3) where [52] re-derived DA physical equation while keeping each TL segment as a real physical µ-TL with its distributed effect. However, even with this improvement, until now both [40], [51], [52], suggested models are still considered as approximate representation of the DA behavior since they are produced based on the assumption of a unilateral two-port AC equivalent model for transistor. This leads to the third design limitation caused by assuming a simple Gm-cell model. The central element of a DA is its Gm-cell; as operating frequencies increase, amplifier designers can no longer benefit from transistor unilateral approximation where Miller effect starts to have a dominant impact. This assumption leads to discrepancy in predicting its behavior, and hence that of the DA, and results in suboptimal Gm-cell sizing. The arguably widely adopted way for improving reverse isolation, as observed in Chapter 2 (subsection 2.3.3) where DAs in different technology processes are presented, is by implementing a conventional cascode configuration. Even then, modeling the DA equivalent circuit becomes complicated since the high-frequency equivalent circuit for a single transistor biased in active region becomes large with a plethora of parameters [57]. It becomes more complicated for a cascode Gm-cell since it involves stacking a minimum of two transistors, rendering analytical expressions based design processes for mm-wave DAs quite cumbersome. This is without considering transistor non-quasi-static behavior that appears when operating deep into mm-wave spectrum. Furthermore, in bulk technology, the transistor is a four-terminal device in which the substrate influence can no longer be disregarded.

Fourth limit, and this is more specific for neural-network based modeling approach, is using a design model constructed from a beforehand step of function fitting to a series of already observed data. While this approach does simplify the derivation process, where one is no longer subjected to the hustle to derive equations and taking into account all tiny effects; however, the degree of optimum performance it predicts for a design characteristic is bounded within how well designed the pre-training circuit set were when used during the fitting pre-process. Another limit for the same modeling approach is its reliability being bounded within the same training data set used in the fitting pre-process. Beyond this set, its predicted outcome becomes more of an extrapolation with a greater degree of uncertainty. For example, when speaking about DA design, if the pre-training data included a set of DAs designed up to N_{max} unit cells, using the model for $N > N_{max}$ has a higher risk of producing meaningless results. Therefore, making the neural network technique more of a statistical modeling technique than previously mentioned ones.

Fifth limit would be neglecting losses that become important at high frequencies and the need for loss-compensated DA topologies. Even if distributed amplification is a promising technique to push the limit of gain-bandwidth-product (GBP) [47], [58], [59], however, with conventional cascode as Gm-cell, it is difficult to achieve these potentially wideband characteristics because the resistive losses in the loaded lines are large at high frequencies. Different techniques of loss-compensation cascodes were suggested, as in [50], [60]. This highlights the various topologies that can be adopted and the approach considered in enhancing the cascode topology, in which extra components are being added to enable the DA to reach wider BWs thereby maximizing its GBP. This undoubtedly adds a new dimension of complexity for mm-wave DA design, pushing DA designers even more towards CAD software.

The sixth and final limit, and it is specific to using graphical schematic environment of CAD tools, concerns the fact that some design variables are not allowed to be automated by their optimization algorithm and hence it relies on the designer to manually do it. For the case of DA design, semiconductor foundries provide for a given process technology a broad range of transistor sizes to explore from. Determining the optimal transistor size to use with the optimal number of Gm-cells (N_{opt}) in order to maximize DA gain for a desired BW could be considered tricky. For instance, for CAD tools where circuit design is possible only via drawing on schematic diagram, the designer will be obligated to manually manipulate the number of unit cells for each component modification performed on the DA. Designing through CAD software schematic environment is therefore the most accurate technique available, but a time-cost consuming one indeed. It could be argued that with recent progress of CAD tools in extending the capability of their design environment, where they start to offer scripting environment possibilities such as application extension language (AEL) in Keysight ADS and OCEAN language in Cadence Virtuoso, that the design of the DA can be automated. While similar can be said when using, for instance, MathWorks MATLAB computing environment, a scripting language will not be able to achieve DA design automation without having first at-hand a proper physical model. A model that takes into account the complete set of DA variables, including and most importantly its variable N as a free variable.

All of those limits, therefore, highlight that the success in the automated design of an IC DA depends crucially on first the appropriate choice of the device model. They emphasize on the need for proposing a new complete and reliable DA model that accommodates any suggested Gm-cell topology and that provides systematic design approaches with less dependence on CAD proprietary optimization tools. This is covered in next Section 3.4.

3.4 Proposed Solution: Chain Matrix (ABCD) Based Design Model [73]

After listing both the milestones and limitations in available distributed amplifier design techniques, in this section an original matrix-based technique is introduced. This model is based on $ABCD$-parameters and it was proposed for the purpose of providing a more direct way of designing mm-wave distributed amplifiers without imposing restrictions on the designer search for optimum design solution. Compared to the previous models, we concentrate on providing a model that deals with the criteria listed in Section 3.1: Optimum performance by taking into account the complete set of design parameters the conventional DA can be made from, and versatility, complexity and reliability with focus on accurate representation of the DA mm-wave behavior.

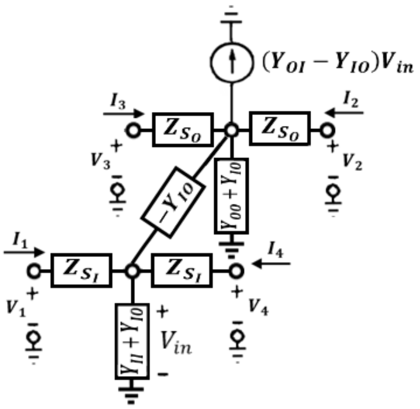


Figure 3.8: Four-port equivalent network for a unit cell.

Referring to Figure 3.8, the Gm-cell can be represented symbolically by its equivalent two-port admittance network. Its self-admittance impacts on the input and output loaded-lines are represented by $Y_{II} + Y_{IO}$ and $Y_{OO} + Y_{IO}$, respectively, where (I) subfix refers to input of Gm-Cell and where (O) subfix refers to input of Gm-Cell. Because any Gm-cell also introduces two different kinds of coupling, leakage from output to input node and amplification from its input to output node, their effect are represented here as two different admittances where Y_{IO} admittance is for the former type of coupling and Y_{OI} admittance is for the latter type. The choice for such a Gm-cell representation was made to keep the proposed unit cell model (and hence the DA model) suitable for any two-port Gm-cell topology the designer decides to use. In addition, all inductors in Figure 2.18 were replaced by a general two-port series impedance networks, depicted as Z_{S_I} and Z_{S_O} for input and output side, respectively, for the intention of obtaining a general unit cell model and for the ease it provides when interchanging DA inductive-type segments topology, as will be presented shortly.

From Figure 3.8, one can now observe that when designing a DA, one is dealing at its core with a four-port network unit cell. Because a DA is defined by cascading this four-port network N times, an $ABCD$-type matrix (3.13), adapted to a four-port representation, is therefore a suitable choice to characterize a single unit cell.

$$\begin{bmatrix} V_1 \\ I_1 \\ V_3 \\ I_3 \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} A_{14} & B_{14} \\ C_{14} & D_{14} \end{bmatrix} & \begin{bmatrix} A_{12} & B_{12} \\ C_{12} & D_{12} \end{bmatrix} \\ \begin{bmatrix} A_{34} & B_{34} \\ C_{34} & D_{34} \end{bmatrix} & \begin{bmatrix} A_{32} & B_{32} \\ C_{32} & D_{32} \end{bmatrix} \end{bmatrix} \begin{bmatrix} V_4 \\ -I_4 \\ V_2 \\ -I_2 \end{bmatrix} \tag{3.13}$$

The left side of the equality sign represents the input side of the four-port unit cell and the right-most matrix represents its output side. The negative sign of both I_2 and I_4 arises to make the output current of one cascaded unit cell equal to the input current of the adjacent one. When speaking of the whole DA, illustrated in Figure 2.18, its $ABCD$-matrix model is represented by (3.14); thereby, it becomes a matter of multiplying the matrix of each unit cell together in the same order the DA network is drawn, i.e., left to right.

$$\begin{bmatrix} V_1 \\ I_1 \\ V_3 \\ I_3 \end{bmatrix} = \prod_{n=1}^{N} \begin{bmatrix} \begin{bmatrix} A_{14} & B_{14} \\ C_{14} & D_{14} \end{bmatrix} & \begin{bmatrix} A_{12} & B_{12} \\ C_{12} & D_{12} \end{bmatrix} \\ \begin{bmatrix} A_{34} & B_{34} \\ C_{34} & D_{34} \end{bmatrix} & \begin{bmatrix} A_{32} & B_{32} \\ C_{32} & D_{32} \end{bmatrix} \end{bmatrix}_n \begin{bmatrix} V_4 \\ -I_4 \\ V_2 \\ -I_2 \end{bmatrix}_n \tag{3.14}$$

In order to solve either equation (3.13) or (3.14), it is necessary to identify the boundary conditions at each terminal side of the four-port network. By proper application of Kirchhoff's voltage law at each port, they are found to be (3.15):

$$\begin{gathered} V_S = Z_1 I_1 + V_1 \\ 0 = Z_2 I_2 + V_2 \\ 0 = Z_3 I_3 + V_3 \\ 0 = Z_4 I_4 + V_4 \end{gathered} \tag{3.15}$$

Here it is assumed the case where only port 1 is stimulated by a microwave signal (Figure 2.18) and all other ports are terminated by a shunted load: Z_2, Z_3 and Z_4. Depending on the choice of Gm-cell topology and type of inductive-type segments used, it will be a lumped impedance or a physical TL. Both equations (3.13) and (3.14) can be used to design any DA that follows the conventional cascading topology of Figure 2.18.

By taking the case of series lumped impedance as a first approach for the inductive-type segments, with admittance representation for Gm-cell, the factorized $ABCD$-matrix describing the network of Figure 3.8 is found to be the one of (3.16).

$$\begin{bmatrix} V_1 \\ I_1 \\ V_3 \\ I_3 \end{bmatrix} = \begin{bmatrix} 1 & Z_{S_I} & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & Z_{S_O} \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ Y_{II} & 1 & Y_{IO} & 0 \\ 0 & 0 & 1 & 0 \\ Y_{OI} & 0 & Y_{OO} & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_{S_I} & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & Z_{S_O} \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_4 \\ -I_4 \\ V_2 \\ -I_2 \end{bmatrix} \tag{3.16}$$

By further inspecting matrix (3.16), one can note the similarity between its structure and that of Figure 3.8 from which it can be concluded that a DA unit-cell is constructed from three four-port networks cascaded together. At the right side of the equal sign, the leftmost and rightmost 4x4 matrices represent each the $ABCD$-matrix of the parallel series-lumped impedances network on the left and right side of the Gm-cell, respectively, and the middle 4x4 matrix, containing the Y-parameters, represents the four-port $ABCD$-matrix of the Gm-cell topology used. Further inspection of (3.16) also reveals the value of such a representation, both leftmost and rightmost 4x4 matrices are made from smaller submatrices that represents the $ABCD$-parameters of the individual input and output segments the unit cell is made from. This demonstrates the simplicity and flexibility in using the proposed model: DA designers now only have to replace those $ABCD$-submatrices with any other $ABCD$-submatrices representing a unit-cell input and output segments topology of their choice. For demonstration, replacing the lumped inductors used in Figure 3.8 with physical TLs transforms equation (3.16) into equation (3.17); where the input-side series μ-TL segments are represented by $(Z_{c,S_I}, \gamma_{S_I})$ with length $(l_{S_I}/2)$ each and the output-side series μ-TL segments are represented by $(Z_{c,S_O}, \gamma_{S_O})$ with length $(l_{S_O}/2)$ each. This also applies for the middle Gm-cell matrix; the designer can choose any Gm-cell topology he desires and apply it to the DA model since it is represented in its general form (Y-parameter). This is contrary to the conventional ways where they are restricted to a unilateral assumption of a single transistor Gm-cell. A demonstrative example will be provided in Chapter 4 where a method for accurately representing the frequency behavior of a cascode topology as a scalable parameter with respect to transistor size and integrating it with (3.16) or (3.17) is given.

$$\begin{bmatrix} V_1 \\ I_1 \\ V_3 \\ I_3 \end{bmatrix} = \begin{bmatrix} cosh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right) & Z_{c,S_I}\, sinh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right) & 0 & 0 \\ sinh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right)/Z_{c,S_I} & cosh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right) & 0 & 0 \\ 0 & 0 & cosh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right) & Z_{c,S_O}\, sinh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right) \\ 0 & 0 & sinh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right)/Z_{c,S_O} & cosh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right) \end{bmatrix}$$

$$\bullet \begin{bmatrix} 1 & 0 & 0 & 0 \\ Y_{II} & 1 & Y_{IO} & 0 \\ 0 & 0 & 1 & 0 \\ Y_{OI} & 0 & Y_{OO} & 1 \end{bmatrix} \bullet \tag{3.17}$$

$$\begin{bmatrix} cosh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right) & Z_{c,S_I}\, sinh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right) & 0 & 0 \\ sinh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right)/Z_{c,S_I} & cosh\left(\gamma_{S_I}\frac{l_{S_I}}{2}\right) & 0 & 0 \\ 0 & 0 & cosh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right) & Z_{c,S_O}\, sinh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right) \\ 0 & 0 & sinh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right)/Z_{c,S_O} & cosh\left(\gamma_{S_O}\frac{l_{S_O}}{2}\right) \end{bmatrix} \begin{bmatrix} V_4 \\ -I_4 \\ V_2 \\ -I_2 \end{bmatrix}$$

In order to obtain the terminal behavior of the DA, the proposed 4x4 $ABCD$-matrix model is first converted into a 2x2 $ABCD$-matrix characterizing a two-port network in terms of input and output ports. In the proposed conventional DA design topology, shown in Figure 2.18, both ports 3 and 4 are terminated by matching impedances Z_3 and Z_4, respectively, to absorb backward-signals and prevent reflections back to the main loaded output and input lines, respectively, as early stated in Chapter 2 (subsection 2.3.2). Interest, thus, falls on both ports 1 and 2, as input and output ports, respectively, leading to the required design matrix (3.18).

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{3.18}$$

Applying the previously listed boundary conditions of (3.15), the required $ABCD$-parameters were deduced to be the ones of (3.19):

$$A = \frac{-(Z_3C_{32} + A_{32})\left(A_{14} + \frac{B_{14}}{Z_4}\right)}{\Delta} + A_{12} \tag{3.19a}$$

$$B = \frac{-(Z_3D_{32} + B_{32})\left(A_{14} + \frac{B_{14}}{Z_4}\right)}{\Delta} + B_{12} \tag{3.19b}$$

$$C = \frac{-(Z_3C_{32} + A_{32})\left(C_{14} + \frac{D_{14}}{Z_4}\right)}{\Delta} + C_{12} \tag{3.19c}$$

$$D = \frac{-(Z_3 D_{32} + B_{32})\left(C_{14} + \frac{D_{14}}{Z_4}\right)}{\Delta} + D_{12} \tag{3.19d}$$

where

$$\Delta = \left(A_{34} + \frac{B_{34}}{Z_4}\right) + Z_3\left(C_{34} + \frac{D_{34}}{Z_4}\right) \tag{3.19e}$$

The two-port network $ABCD$-parameters is now easily convertible into any other two-port network parameters, such as impedance, admittance or power scattering matrix. For the case at hand, where characterizing the behavior of the DA at terminals 1 and 2 is desired, S-parameter conversion [56] is used. For ease of referencing when implementing the design methodology, they are rewritten hereafter (3.20). S_{21} represents DA insertion gain, S_{12} its reverse isolation, and S_{11} and S_{22} represent reflection coefficients seen at the input and output ports, respectively. Z_0 denotes the characteristic impedance reference (usually 50 Ω) for ports 1 and 2.

$$S_{11} = \frac{A + \frac{B}{Z_0} - CZ_0 - D}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{3.20a}$$

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{3.20b}$$

$$S_{12} = \frac{2(AD - BC)}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{3.20c}$$

$$S_{22} = \frac{-A + \frac{B}{Z_0} - CZ_0 + D}{A + \frac{B}{Z_0} + CZ_0 + D} \tag{3.20d}$$

3.5 Conclusion

This chapter discussed the available models in the literature and techniques used to design a DA. Each approach presented its own improvement in terms of added parameters for a more flexible design and targeting to represent the DA behavior more accurately. The most complete and accurate design technique of course being through CAD software, such as ADS or Cadence tools, in which the full technology design kit is available from the manufacturing company. In spite of those, limitations exist and were discussed in this chapter, and they can be summarized as follows. When it comes to designing DAs, the designer has one of three options:

1) Proceeding with the mathematical approaches where the designer can directly see the relation between parameters and hence determine directly the optimal set for a design goal. However, this is at the expense of being restricted towards low operating frequencies, in other words designing DA with smaller bandwidths, since assumptions and simplification through neglecting parameters are more often performed to derive them.

2) Using machine learning, such as artificial neural network, or curve fitting techniques where the designer does not have to deal with the tiny effect (plethora of parasitic) that affect the DA behavior or even how it is made, i.e., the DA will be treated as a black box. However, its output prediction during the design process relies on a large set of pre-designed DAs used in the function fitting (pre-training) process and, also, its optimum performance relies on how adequately they were designed, as already described in Section 3.3 (fourth limit).

3) Relying on CAD tool, either on its schematic diagram environment or scripting environment. For the former case, some parameters such as N are not readily accessible to optimize and consequently the design process becomes a manual and iterative process that relies on intuition. It is also a tedious one if elements to enhance the DA response are being considered to be modified each time because this pushes the designer to redo the performance investigation manually over and over again from scratch, i.e., starting from $N = 1$, per element modification. Furthermore, when the goal changes for the same topology, even with the experience from the previous design, relatively large simulation works are still not avoidable. For the latter case of exploiting CAD scripting capability, if available by the CAD tool, while it could become possible in this scenario to automate and hence made easier. But, first and most importantly is having at disposal a proper physical model: a (simple) model that considers the entire set of design parameters (complete), gives flexibility in choosing DA components topologies (versatile) and accurate in the simulation outcome it provides the designer (reliable).

As a proposed solution, a novel matrix-based model was proposed for both unit cell and DA based on Chain ($ABCD$) parameters. No approximation was performed since both the µ-TL-type segments and Gm-cell were represented by their complete $ABCD$ parameters. It also presents versatility where the model was provided with no assumption of any kind on neither the topology of Gm-cell nor segments used. This is contrary to what is done in the conventional approaches where a simple unilateral AC-equivalent model was always assumed for the transistor. The latter is considered to be not the case in practice since the designer could be interested in adopting other Gm-cell topologies, such as a cascode Gm-cell as was concluded in Chapter 2 (subsection 2.3.3).

In the next chapter, the potential of this model is presented through a scripting a CAutoD methodology example where it is used to explore the different possible CMOS DAs the 55-nm ST technology can provide.

Chapter 4

Model Application – Computer Automated Design for Loss-Compensated Distributed Amplifier

In the last chapter, a four-port matrix-based model using $ABCD$-parameters was proposed for DA design. It was considered to be complete since no assumption was made, and versatile since no limitations was imposed on it, neither on the topology of Gm-cell nor on the µ-TL segments. In this chapter, the proposed model is used to explore different CMOS-based DA solutions the 55-nm ST technology could produce.

This chapter is structured as follows. Section 4.1 starts by introducing the concept of loss-compensated DA. A topology proposed in the nineties [50] and still commonly used for its simplicity in reducing the high-losses issue in millimeter frequencies and expanding the passband. Based on it and with the use of the proposed DA model (Eq. 3.17), Section 4.2 suggests a systematic algorithmic methodology for realizing a CAutoD process that maximizes the DA bandwidth for a given passband-gain-ripple specification. Section 4.3 discusses this process outcome where a set of 3D DSE plots are obtained that enable one to examine the tradeoffs between gain, bandwidth and power consumption, and the size and number of Gm-cells, and arrive at the optimum desired design. Finally, Section 4.4 summarizes and concludes this chapter.

4.1 Loss-Compensated Distributed Amplifier

While the conventional DA is capable of providing us wideband amplification through wideband matching, by dealing with the input- and output- parasitic capacitance of the Gm-cell through connecting inductive-type segments, as already analytically analyzed in Chapter 2 (Section 2.3); however, resistive-type losses remain unmanageable by it and become important at high frequencies that they can no longer be neglected. Those latter losses impact on the gain become more evident at mm-wave frequency that they influence the flatness of the DA passband.

Loss-compensated DA topologies are thus proposed, and even a necessity, when it comes to mm-wave application. Loss-compensation is achieved by adding extra components to the DA device, such as inductors [50] or extra transistors [60], which provides the designer with additional tuning knobs to control the resistive-type losses of the DA. In this work, interest was set on [50] for their interesting idea of making use of the already implemented unit cell Gm-cell contrary to [60] which requires to distribute additional N transistors along each loaded-lines of the DA.

A graphical study of [50] technique influence on both input- and output- loaded lines is carried out first in subsection 4.1.2. Then, an analytical analysis is provided in subsection 4.13. Finally, in subsection 4.1.4, a method for modeling the loss-compensated cascode Gm-cell topology and implementing it in a numerical computing environment, such as MathWorks MATLAB, is demonstrated.

4.1.1 Overview of Publication

The idea of a loss-compensated DA dates back to year 1996. It was first proposed by [50] as a technique to mitigate losses for both the gate and drain loaded-lines. Indeed, from (2.4) and (2.5), the gate-line attenuation constant (α_g) and drain-line attenuation constant (α_d) are dominated by the Gm-cell input and output resistance, R_i and R_{ds}, respectively, as well as microstrip segments resistive part, represented by δR_g and δR_d, respectively. The proposed technique comes as an improvement for the conventional cascode device, in which two additional inductors, L_g and L_{ds}, are added, as illustrated in Figure 4.1. The new loss-compensation circuit improves the high frequency performance of the amplifier device and, when speaking of the whole DA, it makes the gain-bandwidth product larger than that of conventional ones.

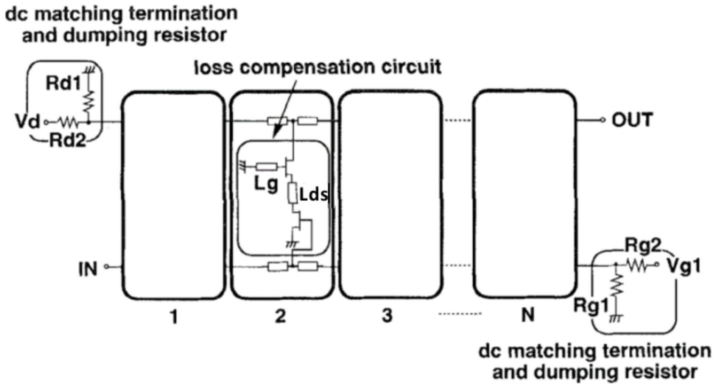


Figure 4.1: Schematic circuit of the proposed loss-compensated distributed amplifier. [50]

To prove their suggested enhancement, [50] realized two DAs using 0.1-μm InAlAs/InGaAs/InP HEMT technology with 50-GHz and 90-GHz bandwidth each. The 50-GHz DA is made from eight unit cells and delivers 16 dB of gain, as shown in Figure 4.2, while the 90-GHz DA is made from six unit cells and delivers a gain of 10 dB, as shown in Figure 4.3. Indeed, this technique is showing its capability in granting the possibility to amplify frequencies above 30 GHz, i.e. compensating losses inside the mm-wave spectrum and producing high gain level similar to the lower side of the frequency spectrum.

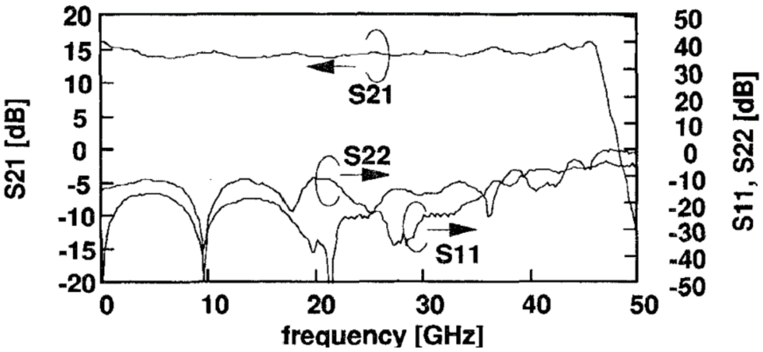


Figure 4.2: Measured S-parameters of the loss-compensated DA IC with eight unit-cells. [50]

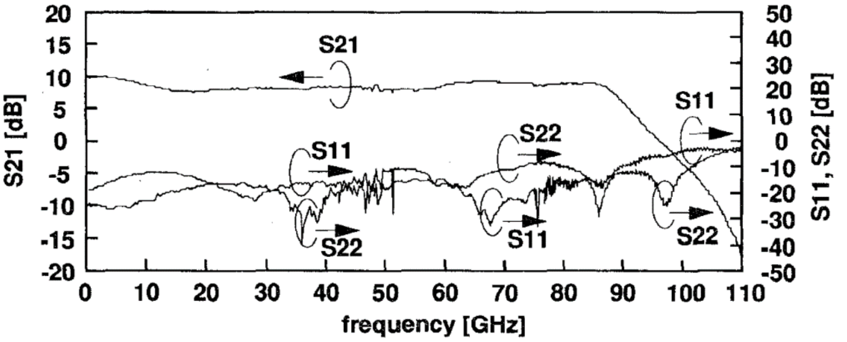


Figure 4.3: Measured S-parameters of the loss-compensated DA IC with six unit-cells. [50]

4.1.2 Loss-Compensation Technique: Graphical Analysis

Due to the increasing losses on both gate and drain lines with increase of frequency, the DA does not experience a flat gain response inside its passband. This is demonstrated in Figure 4.4, where attenuation constants α_g and α_d are plotted. For relevant insight, the losses plotted here represent the ones of the 100-GHz DA designed in Chapter 5 which is synthesized using the conventional two-transistor cascode for Gm-cell topology without the compensation inductors L_g and L_{ds}. One can note that the total losses ($\alpha_{total} = \alpha_g + \alpha_d$) at 100 GHz is about 14-fold higher than the total losses at the lower end of the spectrum. This emphasizes that when speaking about the overall gain behavior with respect to frequency, the upper-end of the conventional (non-compensated) DA passband tends to be lower than the lower-end of its passband.

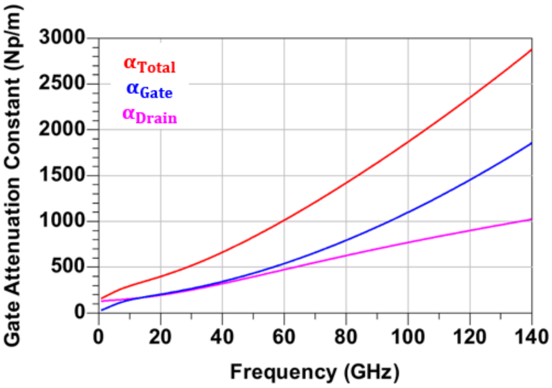
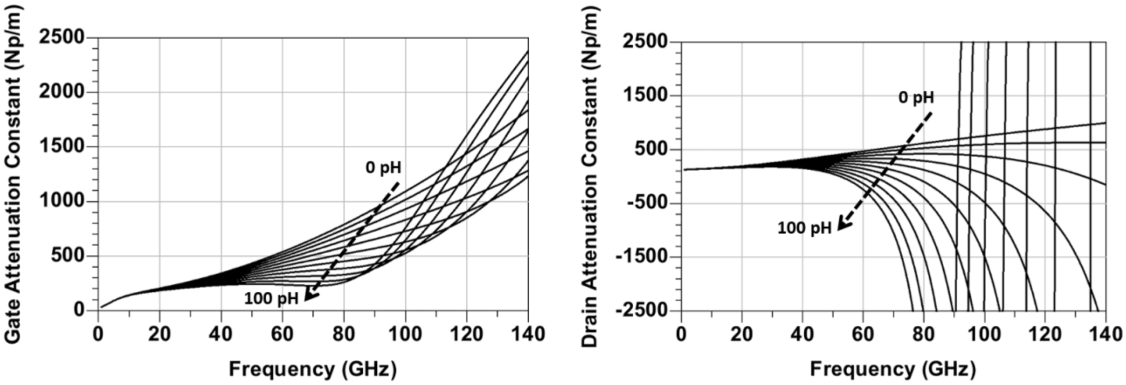


Figure 4.4: Attenuation constants of the conventional DA without loss-compensation technique.

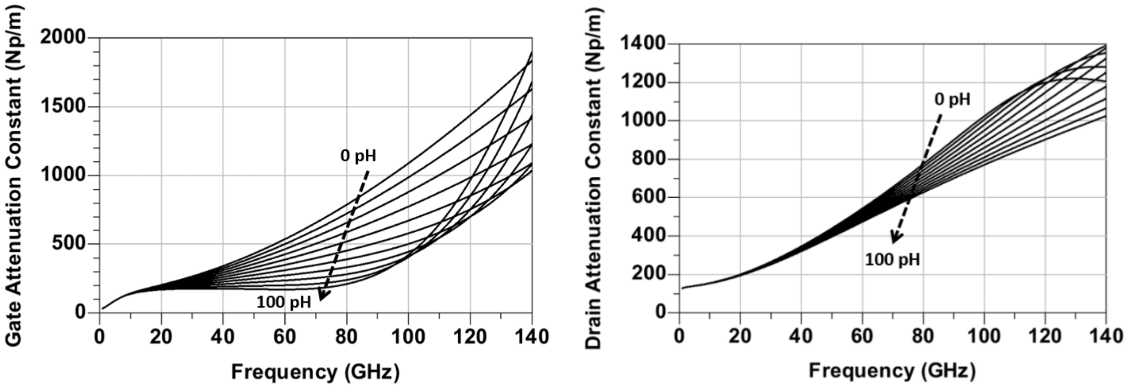
To comprehend the impact of the compensation inductors, L_g and L_{ds}, on both attenuation constants α_g and α_d, they are first studied here visually by increasing each independently and plotting the latter constants behaviors with respect to frequency.



(a) (b)

Figure 4.5: Influence of loss-compensating inductor L_g on (a) gate-line attenuation constant (α_g) and (b) drain-line attenuation constant (α_d).

Referring to Figure 4.5, the inductor L_g has a noticeable influence on the mm-wave frequencies above 60 GHz with a dominant role on the attenuation constant α_d. As L_g increases, the losses on both the gate and drain loaded-lines decrease up to a certain frequency limit as attenuation constants above this limit begin to experience a rapid increase. Thereby, one can deduce that an excessive L_g value can reduce the cut-off frequency of both lines. For the attenuation constant α_d, inductor L_g is also observed to cause negative value if excessively increased. The reason for this will be demonstrated in the upcoming subsection 4.1.3, which deals with the analytical side of this analysis. Nonetheless, as a short explanation here, this is the result behind [50] proposed idea where they regulate the real part of the cascode Gm-cell output impedance through introducing a tunable negative term in it. Doing so provides the designer with the ability to have control over the magnitude of the DA attenuation constant with respect to frequency. A negative attenuation constant, thereby, represents an over-compensation of the overall losses. However, deliberately compensating losses more than what is needed to be removed while one end-objective is to maintain a flat gain across a given BW is usually something not performed when designing wideband devices. In other words, one would not remove resistive losses excessively more than would be required to be removed at a given frequency with respect to another, if by the end the intention is to have a proper flat-wideband response for the amplifier device-under-test. This will be our case here, for instance, where the DA will be designed in a way that the magnitude of the DA total losses at high frequency will be made on the same level as the losses at low frequencies, and not over-compensated, in order to have a proper flat passband response. This will be made clearer when discussing Figure 4.7 next and will be further elaborated on when speaking of the loss-compensated DA design concept in Section 4.2.



(a) (b)

Figure 4.6: Influence of loss-compensating inductor L_{ds} on (a) gate-line attenuation constant (α_g) and drain-line attenuation constant (α_d).

From Figure 4.6, inductor L_{ds} allows the reduction of the losses on the gate loaded line. It is also observed to have an impact on its cut-off frequency where α_g is decreasing up to a certain frequency limit and above this limit the loss starts to increase again rapidly. Thereby, one can deduce that an excessive L_{ds} value can reduce the cut-off frequency of the gate line. For the drain line, inductor L_{ds} is observed to have relatively weak influence on α_d compared to what was observed in the other plots.

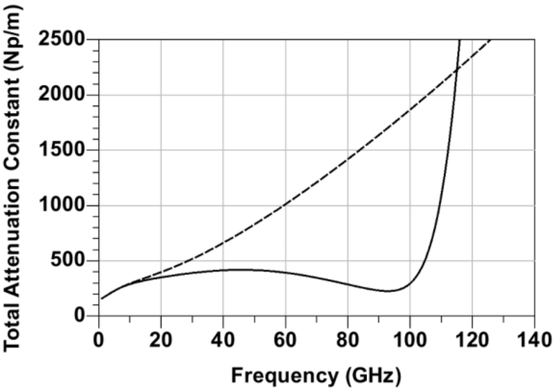
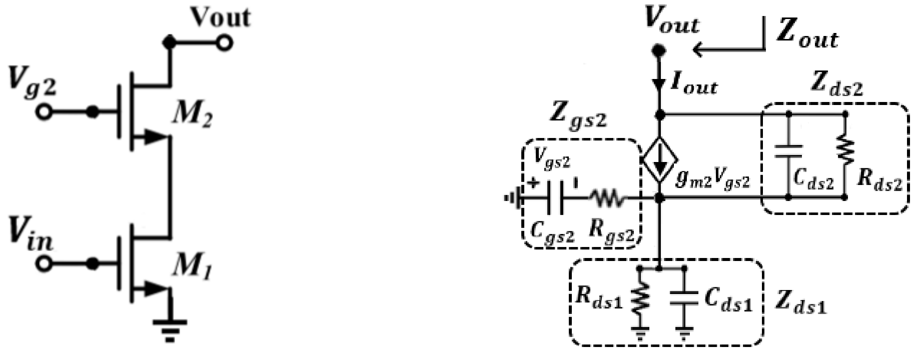


Figure 4.7: Total attenuation constant (α_{Total}) behavior with and without loss-compensation technique.

When combing both compensation inductors, the overall losses (α_{total}) needs to be adjusted such that the losses at the (targeted) upper-end of the passband is on the same level as the losses on its lower-end, as illustrated in Figure 4.7. This will result in the DA experiencing a relatively flat wide amplification passband. It is being considered as relatively flat since at the midband around 50 GHz, peak loss is observed to occur. This will translate into a drop of gain in the middle of the DA passband. Increasing either L_g or L_{ds} to flatten it even more would be difficult, since, as discussed previously, they have an influence on the cut-off frequency of both gate and drain line, i.e., increasing L_g or L_{ds} excessively will lead to shrinkage of the DA bandwidth. On that basis, one can conclude that by using this loss-compensation topology a trade-off exists between the bandwidth and midband gain-drop level, in other words gain-ripple. It is up to the designer to choose between either having a DA that demonstrates wide bandwidth but with a notable midband gain-drop or having a DA with a flat response but at the expense of a smaller bandwidth. In this work, for instance, flatness was given priority when designing single stage DAs where its midband was restricted within 1 dB of gain-drop. A common passband characteristic adopted by similar work when referring to the single stage-stage DAs mentioned in the state-of-the-art Table 2.2 (Chapter 2). .

4.1.3 Loss-Compensation Technique: Analytical Analysis

Previously, the impact of loss-compensation inductors is investigated graphically. Here, mathematically speaking, inductors L_g and L_{ds} are found to compensate the losses through resonance with the intrinsic capacitance of the cascode cell: Inductor L_g with the gate-to-source capacitance (C_{gs2}) coming from transistor M2 and inductor L_{ds} with the drain-to-source capacitance (C_{ds1}) coming from transistor M1. The following are proven as follows.



(a) (b)

Figure 4.8: Non-loss compensated cascode gm-cell: (a) symbolic representation and (b) simplified AC-equivalent circuit.

From the non-compensated cascode equivalent intrinsic circuit of Figure 4.8, its output impedance is represented by (4.1). Subscripts 1 and 2, respectively, indicate the commons-source (CS) transistor M1 and common-gate (CG) transistor M2.

$$Z_{out} = Z_{ds2} + \frac{Z_{ds1}}{Z_{ds1} + Z_{gs2}}\left(Z_{gs2} + \frac{Z_{ds2} \cdot gm_2}{j\omega C_{gs2}}\right) \tag{4.1}$$

Since transistor M2 drain-source intrinsic resistor (R_{ds_2}) is larger than its gate-source intrinsic resistor (R_{gs_2}), this leads to $Mag(Z_{ds}) \gg Mag(Z_{gs})$; thereby, the impedance coefficient ratio $Z_{ds1}/(Z_{ds1} + Z_{gs2}) \approx 1$. Hence, (4.1) can be reduced to (4.2).

$$Z_{out} = Z_{ds2} + Z_{gs2} + \frac{Z_{ds2} \cdot gm_2}{j\omega C_{gs2}} \tag{4.2}$$

Since the real part of impedances Z_{ds2}, Z_{gs2} and $(Z_{ds2} \cdot g_{m2})/(j \cdot \omega \cdot C_{gs2})$ are (4.3a), (4.3b) and (4.3c), respectively, the real part of the output impedance of the cascode, seen by the drain loaded-line, is deduced to be (4.3d).

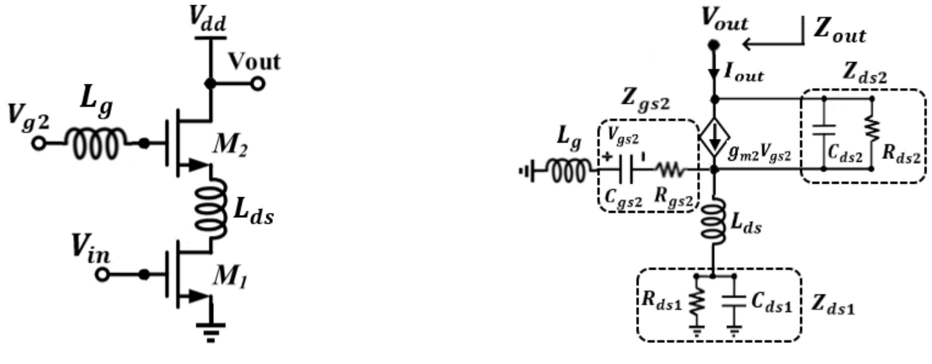
$$Re(Z_{ds2}) = Re\left(\frac{R_{ds2}}{1 + j\omega R_{ds2} C_{ds2}}\right) = \frac{R_{ds2}}{1 + \omega^2 R_{ds2}^2 C_{ds2}^2} \tag{4.3a}$$

$$Re(Z_{gs2}) = Re\left(R_{gs2} - \frac{j}{\omega C_{gs2}}\right) = R_{gs2} \tag{4.3b}$$

$$Re\left(-j\frac{Z_{ds2} \cdot gm_2}{\omega C_{gs2}}\right) = -\frac{gm_2 \cdot R_{ds2}^2 \cdot C_{ds2}}{C_{gs2}(1 + \omega^2 R_{ds2}^2 C_{ds2}^2)} \tag{4.3c}$$

$$Re(Z_{out}) = R_{gs2} + \frac{R_{ds2}}{1 + \omega^2 R_{ds2}^2 C_{ds2}^2}\left(1 - \frac{gm_2 \cdot C_{ds2} \cdot R_{ds2}}{C_{gs2}}\right) \tag{4.3d}$$

Indeed, from (4.3d) one can note that by using just the simple conventional cascode Gm-cell the resistive losses cannot be reduced as they only depend on the intrinsic parameters of the cascode. It is also clear that the second term between parenthesis $((gm_2 \cdot C_{ds2} \cdot R_{ds2})/C_{gs2})$ operates as a negative term and contributes in decreasing the real part of the output impedance that causes the loss on the drain line. However, circuit designers cannot control this negative term effect freely because it depends solely on the parameters of the transistors which can have unfavorable degradation on the overall gain of the DA. That is why external components are proposed by [50] to be added, in this case extra inductors L_g and L_{ds}, in order to have more flexible control over $\mathrm{Re}(Z_{out})$ with significant change on its value, as demonstrated hereafter.



(a) (b)

Figure 4.9: Loss compensated cascode gm-cell: (a) symbolic representation and (b) simplified AC-equivalent model.

Referring to Figure 4.9, L_g and L_{ds} are added to see how they influence the behavior of $Re(Z_{out})$. The former inductor is considered through its impedance $Z_{L_g} = j\omega L_g$ in series with $Z_{gs2} = R_{gs2} + 1/j\omega C_{gs2}$ and the latter inductor is considered through its impedance $Z_{L_{ds}} = j\omega L_{ds}$ in series with Z_{ds1} (C_{ds1} in parallel with R_{ds1}). This results in (4.1) becoming (4.4).

$$Z_{out} =$$

$$Z_{ds2} + \frac{(Z_{ds1} + j\omega L_{ds})}{(Z_{ds1} + j\omega L_{ds}) + \left(Z_{gs2} + j\omega L_g\right)} \left\{ \left(Z_{gs2} + j\omega L_g\right) + \frac{Z_{ds2} \cdot gm_2}{j\omega C_{gs2}} \right\} \tag{4.4}$$

Now it is clear how the compensation takes place through resonances: Z_{ds} interacts with Z_{ds1} and Z_g interacts with Z_{gs2}, where both together contribute into reducing the frequency impact on the degrading part of Z_{out}. Through (4.5a) it is found that inductor L_{ds} resonates specifically with the parasitic capacitor C_{ds1} and through (4.5b) inductor L_g resonates specifically with the parasitic capacitor C_{gs2}.

$$Z_{ds1} + j\omega L_{ds} = \frac{R_{ds1}}{1 + j\omega R_{ds1} C_{ds1}} + j\omega L_{ds} \tag{4.5a}$$

$$Z_{gs2} + j\omega L_g = R_{gs2} + \frac{1}{1 + j\omega C_{gs2}} + j\omega L_g \tag{4.5b}$$

The analysis demonstrated up to now, while insightful for explaining how the compensation inductors influence the losses on gate and drain loaded-lines, it is considered approximate and not fully suited for practical usage when designing in the mm-wave spectrum. Adding more elements for more accurate depiction will cause the information to be lost, since more parasitic will be intertwined, and will result in a more complicated design process since each parasitic needs to be extracted for different transistor sizes. For that reason, the next subsection deals with the modeling aspect of loss-compensated cascode by introducing a simple matrix-based method for implementing the complete Gm-cell topology on a coding software such as MathWorks MATLAB.

4.1.4 Implementing Loss-Compensated Cascode Gm-Cell in a Numerical Computing Environment

Compared to conventional ways of using AC equivalent circuit to derive parametric expressions to replicate the cascode Gm-cell frequency behavior for use in circuit design, the method presented hereafter treats the adopted loss-compensated cascode as a matrix-based model.

This method is considered an important step since in either DA model (3.14) or (3.17), the Gm-cell is represented in its general form through the middle $ABCD$-matrix. In addition, this method will allow the inductors to be implemented as tuning knobs, a necessary step if full computer automation is needed. Since no approximation for simplification purposes is carried out, this method benefits from the complete and accurate representation of cascode behavior, hence of DA behavior. It also benefits from ease of scalability where a collection of matrices can be extracted for several transistor sizes and then depending on the desired cascode size the corresponding transistors matrices are used.

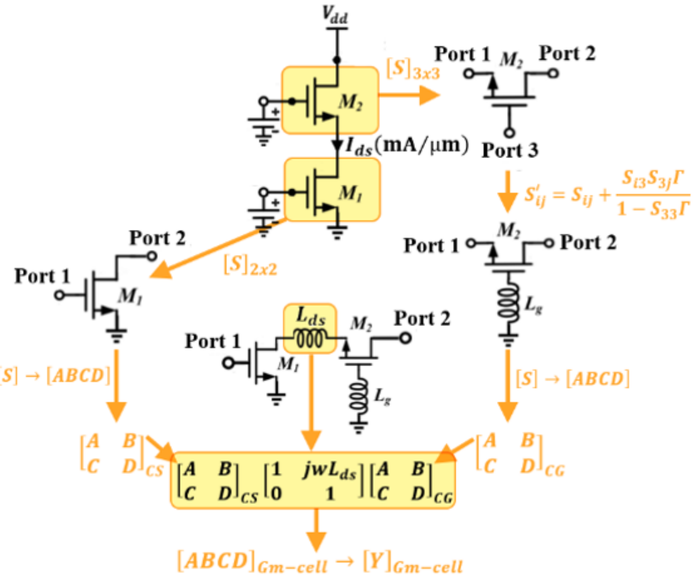


Figure 4.10: Flow diagram for converting the loss-compensated cascode Gm-cell into a Y-matrix representation.

This implementation method is illustrated in Figure 4.10 as a flow diagram. When the designer has biased his cascode cell to the desired operating point, a collection of both CS and CG transistor S-parameter matrices are extracted first for the envisaged sizes and frequency range during DA design process. Since CS transistor in standalone has its gate pin as input port, drain pin as output port and source pin grounded, its corresponding S-parameters will be a two-port matrix extraction. Since CG transistor in standalone has its source pin as input port, drain pin as output port and gate pin as a third port eventually connected to a shunt inductor L_g, its corresponding S-parameters will be a three-port matrix extraction.

Next step involves converting CG transistor three port S-matrix into a two-port matrix form. This can be done by using (4.6a), where Γ represents the reflection coefficient between the added inductor L_g and the reference characteristic impedance (Z_0) the CG three-port S-parameters was extracted with (4.6b). In case µ-TL topology is used to implement inductor L_g, (4.6c) is a suitable option where Z_C, $\gamma_{TL_{Lg}}$ and $l_{TL_{Lg}}$ are the characteristic impedance, propagation constant and length of this inductor.

$$S'_{ij} = S_{ij} + \frac{S_{i3}S_{i3}\Gamma}{1 - S_{33}\Gamma};\ (i,j) \in (1,2) \tag{4.6a}$$

where

$$\Gamma = \frac{j\omega L_g - Z_0}{j\omega L_g + Z_0} \tag{4.6b}$$

$$\Gamma = \frac{Z_c\, tanh(\gamma_{TL_{Lg}} l_{TL_{Lg}}) - Z_0}{Z_c\, tanh(\gamma_{TL_{Lg}} l_{TL_{Lg}}) + Z_0} \tag{4.6c}$$

Afterwards, both CS and CG two-port S-parameters matrices are converted into an $ABCD$-matrix format using the conversion provided by [2] and multiplied with $ABCD$-matrix of the series inductor L_{ds}, as shown in (4.7a). In case μ-TL topology is used to implement inductor L_{ds}, (4.7b) is a suitable option where Z_C, $\gamma_{TL_{Lds}}$ and $l_{TL_{Lds}}$ are the characteristic impedance, propagation constant and length of this μ-TL (TL_{Lds}).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Cascode} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CS} \begin{bmatrix} 1 & j\omega L_{ds} \\ 0 & 1 \end{bmatrix}_{L_{ds}} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CG} \tag{4.7a}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{Cascode} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CS} \begin{bmatrix} cosh\left(\gamma_{TL_{Lds}} \frac{l_{TL_{Lds}}}{2}\right) & Z_c\, sinh\left(\gamma_{TL_{Lds}} \frac{l_{TL_{Lds}}}{2}\right) \\ sinh\left(\gamma_{TL_{Lds}} \frac{l_{TL_{Lds}}}{2}\right)/Z_c & cosh\left(\gamma_{TL_{Lds}} \frac{l_{TL_{Lds}}}{2}\right) \end{bmatrix}_{TL_{Lds}} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{CG} \tag{4.7b}$$

Finally, the obtained two-port $ABCD$-matrix describing the proposed Gm-cell amplifier is converted to a two-port Y-matrix from using [56] and now can be joined with proposed DA $ABCD$-models, (3.14) or (3.17), by filling up their middle $ABCD$-matrix with the adequate Y_{ij} parameters. Due to no simplification performed on the transistors and the possibility to represent the complete cascode Gm-cell through (4.7b), DA designers can now benefit from high reliability in accurate behavior representation, one of the desired criterion highlighted in Chapter 3 (Section 3.1). In addition, designers can benefit by using to proposed design methodologies that produce accurate DA sizing outcome, as will be presented later on when speaking of our own algorithmic DA design methodology.

4.2 Loss-Compensated Distributed Amplifier CAutoD Process

Before discussing the offered loss-compensated DA algorithmic design methodology, the design concept of the loss-compensated cascode Gm-cell [50] adopted as a technique that can be used in extending the DA bandwidth while providing control over its mid-band flatness is first examined. Using the proposed cascode Y-matrix based model, (4.7a) or (4.7b), in conjunction with the DA $ABCD$-model (3.14), the influence of inductors L_g and L_{ds} on DA S_{21} response is first investigated.

4.2.1 Distributed Amplifier Bandwidth Extension and Flattening Concept

The DA under study is the one implemented and measured in Chapter 5, whose design parameters were obtained from the design methodology of the upcoming subsection 4.2.2. Those parameters are only summarized here as follows. The DA consists of five unit cells ($N = 5$), where the unit cell is modeled using (3.17) and its inductive-type segments are implemented as μ-TLs using the thickest copper metal available in the BEOL of ST 55-nm used process with 131 μm in length. The middle $ABCD$-matrix of (3.17) is filled up with the Y-parameters of the two-port admittance of the loss-compensated cascode consisting made from 31-μm CS nMOS, M1, and 62-μm CG nMOS, M2, biased at a current density of 0.16 mA per CS micrometer width (0.16 mA/μm). During this concept analysis, both L_g

and L_{ds} were left as ideal components, (4.6b) and (4.7a), and used as tuning knobs. The DA is intended to cover a bandwidth of 100 GHz.

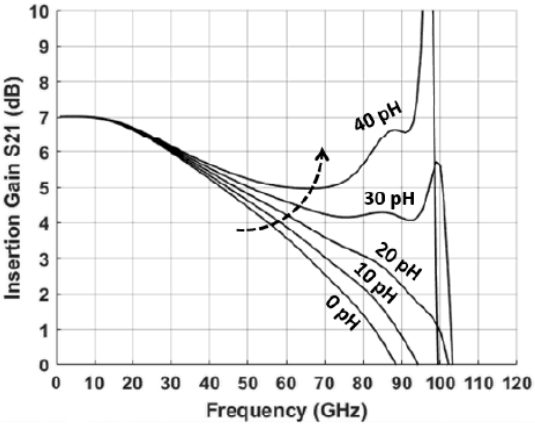


Figure 4.11: S_{21} response versus frequency when $L_{ds} = 0$ pH and L_g increases.

Referring to Figure 4.11, for the given N and cascode size, the DA gain is determined by its gain level at lower of spectrum – here, it is 7.1 dB. When L_g and L_{ds} are set to zero, one can observe the gradual decrease in gain with respect to frequency. The cause of this is related to the high losses both physical μ-TLs and cascode Gm-cell itself experience at mm-wave frequencies, as illustrated in Figure 4.4. By shorting L_{ds}, i.e., L_{ds} = 0 pH, increasing L_g rises gain at a certain high frequency component. Indeed, inductor L_g is extending the DA BW, enabling it to reach higher frequencies—in this case 100 GHz—by compensating for losses at those frequencies, as demonstrated in Figure 4.5.

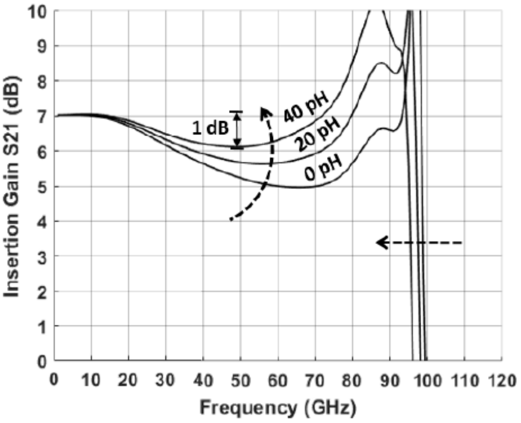


Figure 4.12: S_{21} response versus frequency when L_{ds} increases and L_g =40 pH.

Regardless of the achievable extension, however, Figure 4.11 highlights an undesirable behavior between lower and upper passband limits: the mid-band exhibits a gradual gain roll-off. This is due to L_g being a loss-compensating technique with a major impact on the magnitude of the attenuation constant α_g at frequencies above 60 GHz, as was deduced from Figure 4.5, and insignificant impact on the lower spectrum. To solve this issue causing midband gain drop, the addition of L_{ds} is required. By maintaining L_g at the value that peaks DA gain at the higher-end of the spectrum to the same level of gain as the lower-end of the spectrum, in this case 40 pH, increasing L_{ds} leads to lifting the mid-band gain drop, as illustrated in Figure 4.12—here, it is desired to have 1-dB mid-band gain drop. Therefore, to summarize up to now, one can conclude the following: Inductor L_g mainly influences upper-end peaking while inductor L_{ds} plays its main role on mid-band, but unfortunately not exclusively.

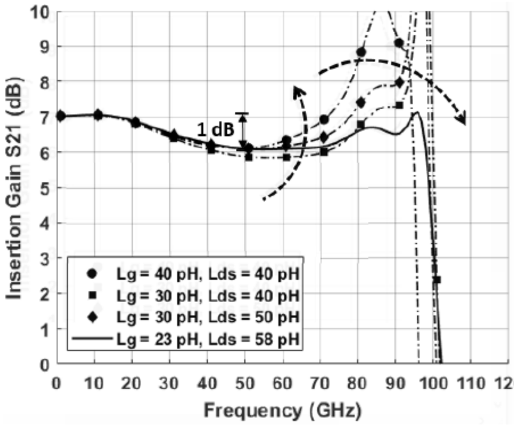


Figure 4.13: S_{21} response versus frequency when L_{ds} and L_g are tuned to maintain simultaneously the extended bandwidth of 100 GHz and 1-dB mid-band gain drop at 50 GHz.

Figure 4.12 also highlights an undesirable behavior: increasing L_{ds} has an influence on the level of peaking produced from L_g where it increases it even further and on the position of its gain-peaking frequency where it shifts it towards lower spectrum. To fix it, L_g and L_{ds} must simultaneously be decreased and increased, respectively, to maintain the desired mid-band drop (1-dB) while conserving the acquired high frequency component (100 GHz), as demonstrated in Figure 4.13. Indeed, it is observed that through the usage of L_g and L_{ds}, one can extend the BW while flattening the passband gain-ripple

4.2.2 Algorithmic Design Methodology

A step-by-step algorithmic DA design methodology is proposed based on the design concept discussed previously. This methodology uses both DA $ABCD$-model (3.14) with the unit cell model (3.17), where the physical μ-TL topology is used for the inductive-type segments, and the presented loss-compensated cascode Gm-cell with its matrix implementation method presented in subsection 4.1.4. For the latter, its inductors L_g and L_{ds} are implemented as physical μ-TL and thereby (4.6c) and (4.7b), respectively, will be used during the design process.

The purpose of this methodology is to explore all loss-compensated DAs a given technology process can provide at a given biasing point, by maximizing bandwidth for various combinations of transistor widths and number of unit cells while satisfying a specified passband flatness. It is therefore noted that the initiating point for such method is the designer's choice of bias point beforehand, what follows will be automated and the end outcome will be 3D DSE plots to pick DA solutions from.

The design methodology is summarized as a flowchart in Figure 4.14 and its systematic steps are presented hereafter. The DSE plots outcome of this methodology are discussed in the next Section 4.3. Since 55-nm ST process node is used at the end for fabrication, its process design kit (PDK) is used throughout the design steps for illustration. For the numerical computing environment, in our case MathWorks MATLAB software is used. It should be noted that technology components, such as μ-TL and transistors, were first simulated on Keysight ADS software, since PDK is available on it by semiconductor foundry and, as a second step, their S-parameters were exported into MATLAB to perform the required conversions and matrix manipulations.

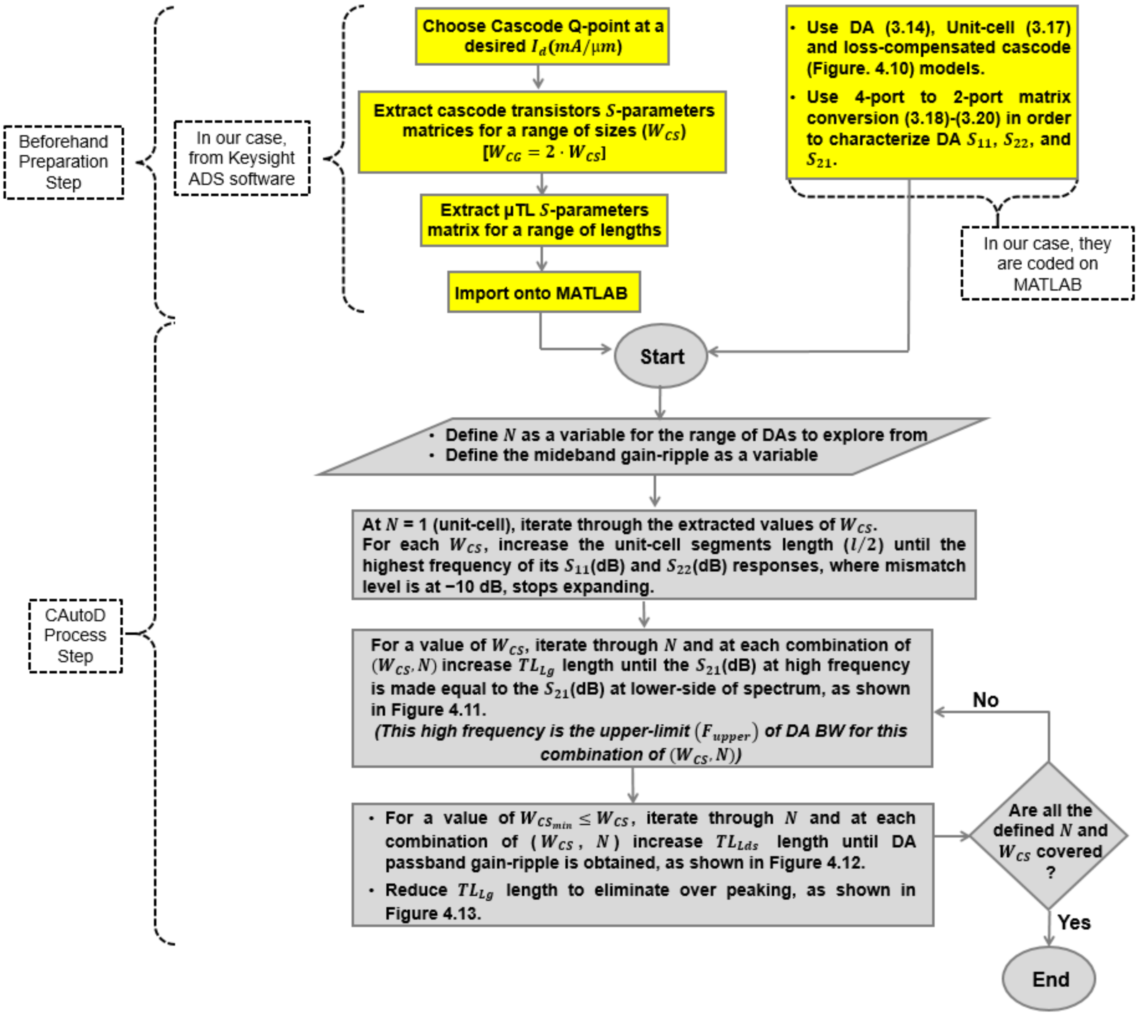


Figure 4.14: Flowchart presenting our DA CAutoD procedure using proposed DA and loss-compensated cascode models.

Step 1) Extract the S-parameters for a range of PDK μ-TL lengths at a given thickness and width. They will be used to model the unit-cell segments as well as TL_{Lg} (4.6c) and TL_{Lds} (4.7b). Choosing the thickest μ-TL in technology BEOL offers the lowest losses versus frequency, since it will have the lowest sheet resistance, and hence aids DA gain response. For eight-metal version of 55-nm CMOS process, it is the ultra-thick metal M8. For what concerns the width, in this metal layer, the minimum width allowed is 0.6 μm, but to comply with the DC-current handling limits expressed on the Design Rule Manual (DRM), we decided to adopt a width of 1 μm. We also decided to apply the same 1 μm width for all μ-TLs with the aim of having later on a simpler design implementation process where all the lines will share the same width. After that, the two-port S-parameters are extracted for length ranging from 10 μm up to 400 μm from ADS. Since chain $(ABCD)$

model is used for both unit-cell and cascode models, the μ-TL characteristic impedance (Z_C) and propagation constant (γ) can be obtained using (4.8) when needed, where conversion between two-port S-parameters to $ABCD$-parameters is done on MATLAB.

$$Z_C = \sqrt{\frac{A \cdot B}{C \cdot D}} \tag{4.8a}$$

$$\gamma = \frac{1}{l} cosh^{-1}\left(\frac{A + D}{2}\right)\sqrt{\frac{A \cdot B}{C \cdot D}} \tag{4.8b}$$

Step 2) At a desired drain current per unit gate width ($I_d(A/width)$), extract the S-parameter matrices of both nMOS CS and CG FETs separately for a range of different channel widths, as explained in Figure 4.10, in order to link the loss-compensated cascode as a two-port Y-matrix with the DA model (3.17). Here, the CG FET, M2, channel width is set to be twice the size of the CS FET, M1, in order to have similar magnitude for the cascode Gm-cell input and output capacitive-type reactance. From that, the unit-cell μ-TL segments can be set equal in length, i.e., $l_{S_I}/2 = l_{S_I}/2 = l/2$, inside (3.17) which will aid us later in having a simpler layout implementation process. Those two design choices were taken in order to equate the loaded input- and output-lines phase delays; a necessity for producing constructive interference on the output line, as was discussed in the basic operation section of a DA in Chapter 2.

In this thesis, the cascode bias was desired to be biased at 0.16 mA per CS micrometer width (0.16 mA/μm) at V_{DD}=1.2 V (nominal value of technology). While this choice of current density does not represent the full capability of ST 55-nm CMOS (f_t = 160 GHz/f_{max} = 246 GHz at $I_d(A/width)$ = 0.22 mA/μm): our choice of current density is to nearly maximize g_m while being consumption-efficient since our end goal is concerned about a metric of GBP over P_{DC}. On that basis and as a first step, the CS and CG FETs were inserted as separate standalone devices on ADS schematics from the technology PDK library and their drain current per unit gate width was set to our 0.16 mA/μm choice. As a second step, a sweep for a desired range of widths is performed; in this work, their width was varied for a range of 14 μm≤ W_{CS} ≤ 40 μm and, hence, 28 μm≤ W_{CG} ≤ 80 μm, and their respective S-parameters were extracted. It should be reminded that for the CS FET it will be a two-port matrix extraction and for the CG FET it will be a three-port matrix extraction, as already described in Figure 4.10. Wider widths are possible, but were disregarded in being mentioned in this discussion. This is because during the time of proposal and testing of this methodology, W_{CS} > 40 μm were observed to offer DAs with BWs ≤ 80 GHz, as will be proven in Section 4.3 (Figure 4.16); thereby, of no interest for us to highlight them here and in the remaining of this manuscript. In addition, DAs with W_{CS} < 14 μm required TL_{Lds} μ-TLs with lengths above our set design limit (400 μm) extracted in Step 1) and hence did not converge, and, for us, were disregarded since they are solutions with excessively large on-wafer areas.

After this step, the DA model (3.17) is now ready with its tunable μ-TLs lengths (unit-cells segments, TL_{Lg} and TL_{Lds}), transistors width and N knobs to perform automated design for a defined matching and passband flatness levels.

Step 3) By fixing the number of unit cells of DA to one in (3.14), i.e. $N = 1$, iterate through each W_{CS} and increase the µ-TL segments length ($l/2$) until the input- and output-ports reflection coefficient bandwidth stops expanding at a defined targeted maximum level. In (3.20), Z_0 is set to 50 Ω that represents the impedance of both RF probes for the measurement setup. In our case, the maximum acceptable mismatch level defined for a single unit cell input and output ports is set at $S_{11max} = S_{22max} = -10$ dB. The scripted methodology at each transistor width is set to increase $l/2$ until the far-end frequency of S_{11} and S_{22} bandwidth where mismatch level is at −10 dB stops expanding.

Step 4) For a given value of W_{CS}, iterate through N and for each combination of (W_{CS}, N) detect the length of TL_{Lg} that increases gain at the rightmost side of the frequency spectrum to attain same level of gain of that at the lower-end of the DA passband. The lower-end passband frequency is usually determined by the AC-grounded capacitor used in series with termination resistors R_3 and R_4 when implementing the loaded-lines termination loads Z_3 and Z_4. Both R_3 and R_4 were set as ideal 50-Ω resistors since it is desired here to design DAs at $Z_0 = 50$ Ω, as stated in Step 3. As a first approach during the design process and before starting the layouting process of making the choice of AC-ground topology to synthesis, the capacitors were considered here as a perfect GND connection (i.e. $Z_3 = R_3$ and $Z_4 = R_4$). This is observed to provide equal gain over all frequencies ≤ 10 GHz and with a flat shape, as visible from Figure 4.11. Since it is commonly known that moving higher in frequency benefits IC designers from implementing components of reduced on-chip area, we decided to go with 10 GHz as the lower-corner frequency (F_{lower}) of the DA passband. The latter choice will benefit us later on during layout implementation with synthesizing small AC-grounded capacitor for R_3 and R_4 compared to if F_{lower} of 1 GHz was to be picked, for instance. Accordingly, for a given (W_{CS}, N), the µ-TL TL_{Lg} length is increased until a certain high frequency component gain becomes on the same gain level as at 10 GHz (see Figure 4.11). The frequency at which this peaking first occurs is considered the DA upper-corner frequency (F_{upper}).

Step 5) For a given value of W_{CS}, iterate through N and for each combination of (W_{CS}, N) detect the length of TL_{Lds} in order to flatten passband for a desired mid-band gain drop. In this manuscript, the desired mid-band gain drop variable was assigned to a value of 1 dB and the mid-band frequency is determined by $(F_{upper} + F_{lower})/2$; accordingly, for a given W_{CS} and N, the length of TL_{Lds} is increased until the gain at mid-band is made 1 dB less than gain at F_{lower} (see Figure 4.12). As mentioned in subsection 4.2.1, TL_{Lds} has an influence on gain peaking established by TL_{Lg} and vice-versa. The proposed way to counteract it is just to script the algorithm to reduce TL_{Lg} in order to maintain gain at F_{upper} on the same level as gain at F_{lower} while increasing TL_{Lds} to maintain mid-band gain drop limited to 1 dB with respect to gain at F_{lower} (see Figure 4.13).

Step 6) Repeat Steps 4) to 5) for all combinations of W_{CS} extracted in Step 2) with the desired range of unit cells. In this manuscript, we extracted 27 transistor widths ($14\ \mu\text{m} \leq W_{CS} \leq 40\ \mu\text{m}$) and explored DA configurations made of $2 \leq N \leq 9$. For $N > 9$, BWs ≤ 80 GHz were obtained and hence were disregarded. This results in the automated DA design program in producing 216 feasible loss-compensated DAs solutions.

Step 7) Final step includes evaluating for each design option, in this case 216 solutions, its power consumption (P_{DC}). This can be accounted for by using (4.9) where $I_d(A/width) = 0.16\ mA/\mu m$ at $V_{DD} = 1.2\ V$ (defined in Step 2).

$$P_{DC} \cong N \cdot V_{DD} \cdot I_d \cdot W_{CS} \tag{4.9}$$

4.3 3D Design Space Exploration Plots: Parameters and Variables

When successfully implementing the proposed design methodology, the DA designer will end up with an outcome of six DSE plots. Each 3D plot illustrates a given characteristic against transistor size on x-axis and number of unit cells (N) on the y-axis. Subsection 4.3.1 covers the three DSE plots that represent parameter of interest from gain, bandwidth and P_{DC}. Subsection 4.3.2 covers the remaining DSE plots that represent the required design-variables from μ-TL segments length and compensation μ-TL-type inductors TL_{Lg} and TL_{Lds} lengths.

4.3.1 DA Design Parameters: Gain, Bandwidth and P_{DC}

Figure 4.15 illustrates the variation of DA gain against W_{CS} and N. One can observe that when either of those two parameters increase, the overall DA gain increases.

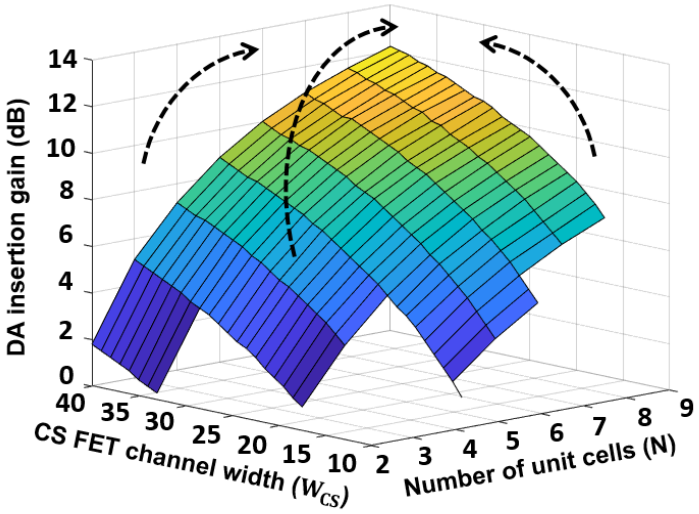


Figure 4.15: 3D DSE plot showing possible DA gain with respect to W_{CS} and N.

This is in agreement with is in agreement with (2.11) where the gain expression is proportional to transconductance term (g_m). The transconductance parameter is defined by the transistor width. Having larger width equates to having higher g_m, hence higher gain. This plot also is in agreement with (2.12) where DA gain is clearly defined with the number of unit cells.

Thereby, one can conclude that the small transconductance provided by narrow transistor can be compensated by adding more unit cells to achieve higher gain and this is also equivalent to realizing a DA with big transistors and fewer number of unit cells.

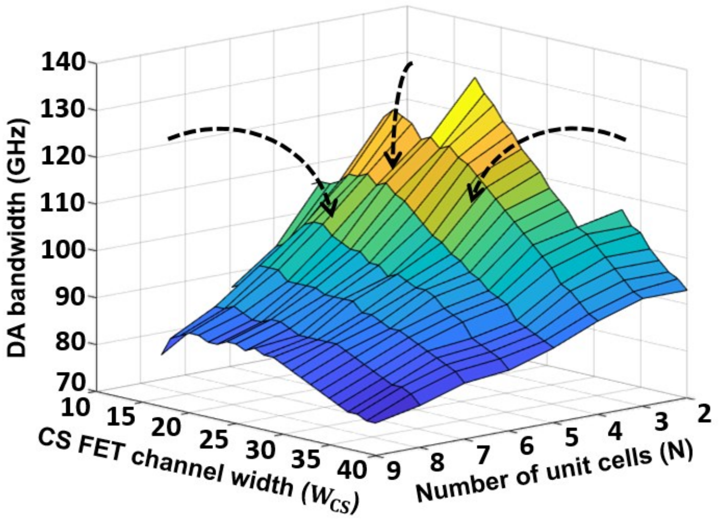


Figure 4.16: 3D DSE plot showing possible DA 1-dB bandwidths with respect to W_{CS} and N.

Figure 4.16 illustrates the variation of DA bandwidth against W_{CS} and N. It highlights that for each N there is a maximum BW attainable that is wider for smaller W_{CS} sizes; however, until a certain limit where even smaller sizes lead to smaller BWs. This could be explained by the inability of smaller transistors from providing enough gain to compensate for important losses at high mm-wave regions. Therefore, this pushed both TL_{Lg} and TL_{Lds} to be increased even more to elevate the gain at F_{upper} towards the same level of gain at F_{lower} while maintaining the 1-dB mid-band gain drop constraint. As already discussed in Section 4.1 (subsection 4.1.2), this leads to shrinkage of BW where excessive increase of either compensation inductors leads to shift of loaded-lines cut-off frequencies towards lower frequencies.

Decreasing N while also decreasing W_{CS} can permit operation at wider BWs but at the expense of lower gain, as shown by Figure 4.15. Therefore, the first parameter to choose from would be the bandwidth required for the DA to cover and, then, as a second step, to choose the desired gain level from the available options obtained for that specific bandwidth.

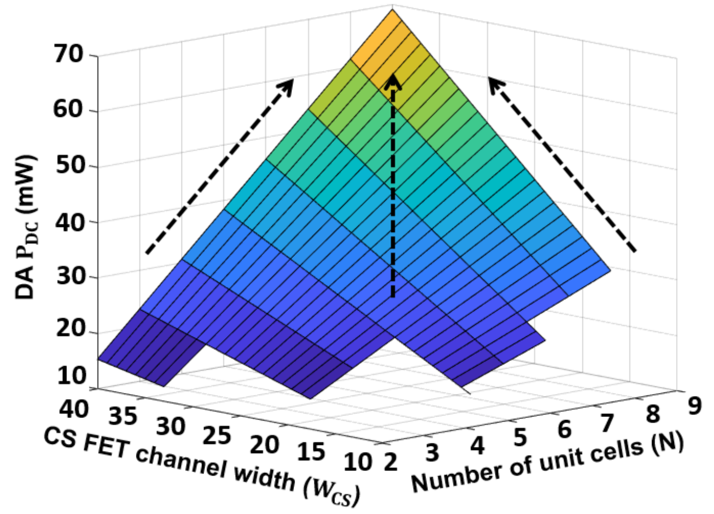


Figure 4.17: 3D DSE plot showing possible DA P_{DC} with respect to W_{CS} and N.

Figure 4.17 illustrates the variation of DA power consumption against W_{CS} and N. It shows that a DA constituting of more Gm-cells, i.e., larger N, leads to higher P_{DC}. The same applies for having a DA made from larger transistors. The highest consumption, hence, would be the design in which the DA is synthesized with both big transistors and large N at the same time. One reason for this design point could be for delivering larger gain. For instance, from Figure 4.17, choosing a DA made from $N = 9$ with $W_{CS} =$ 40 µm leads to 70 mW of power consumption but with a high gain close to 12 dB; however, from Figure 4.16, this choice would restrict the design to a passband of only 80 GHz.

As a conclusion, from those three figures, one can conclude that a compromise between those three parameters (gain, bandwidth and P_{DC}) exists and the choice would depend on the designer application orientation. Having an amplifier that delivers high gain will equates to having a smaller bandwidth and higher P_{DC} and vice-versa. In this work, major interest is laid on the bandwidth as a first choice. This will be further elaborated on in Chapter 5 where a 100-GHz BW DA is needed for on-wafer characterization, and then, as a second step, the choice was made to have high gain with low P_{DC}.

4.3.2 DA Design Parameters: Synthesizing a Unit-cell

In this section, the design parameters needed to obtain the performance characteristics covered previously are presented. The loss-compensated unit cell in discussion is synthesized from µ-TL segments and a cascode Gm-cell with loss compensation inductors implemented as µ-TL (TL_{Lg} and TL_{Lds}). Its electrical schematic is presented in Figure 4.18. Those parameters (length of segments, TL_{Lg} and TL_{Lds}) are plotted independently with respect to W_{CS} and N, as shown in Figure 4.19 and Figure 4.20.

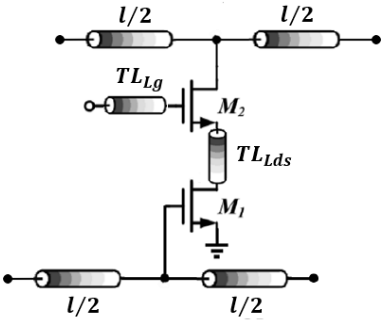


Figure 4.18: Schematics of DA unit cell with loss-compensated cascode Gm-cell.

Figure 4.19 presents the length needed for µ-TL segments ($l/2$) needed for obtaining a DA with reference impedance (Z_0) around 50 Ohms. It is noticeable that when the size of transistor increases, the length of segments increases. It is interesting to note the linear dependence of segments length against W_{CS}. This is consistent with loaded lines characteristic impedance equation (2.2) and (2.4) discussed in Chapter 2, which states that inductance of segments must increase when the Gm-cell input and output capacitances are increased in order to maintain a required DA characteristic impedance. We remind here that the length of the µ-TL segments is determined by setting N =1, what explains a 2D plot.

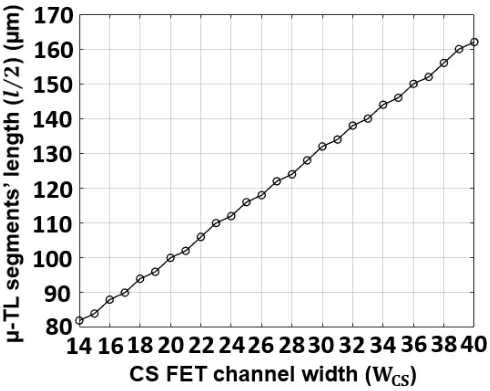
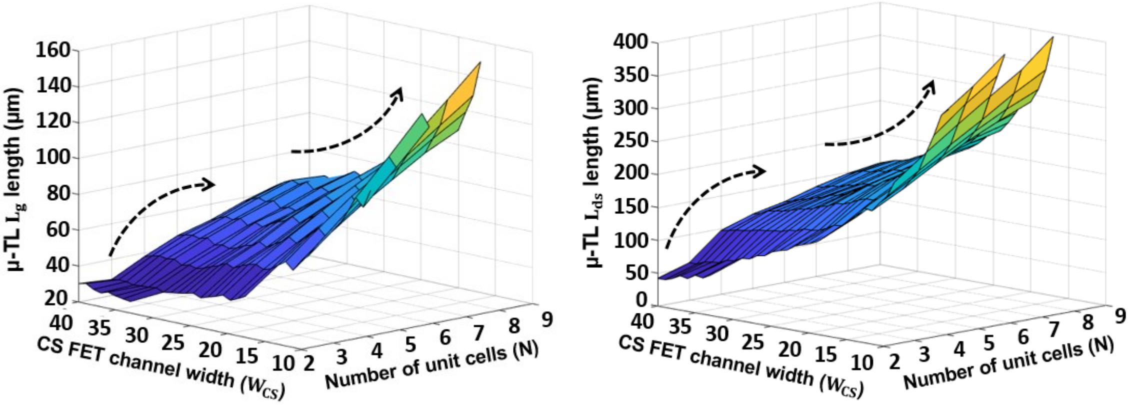


Figure 4.19: DA 2D DSE plot showing μ-TL segments lengths to achieve widest matching BW for $\|S_{11max}\| = \|S_{22max}\| = -10$ dB

For the compensation inductors TL_{Lg} and TL_{Lds}, referring to Figure 4.20, one can note that larger inductances are needed for DAs built using either smaller transistor sizes or larger number of unit cells. This is due to the small transistor incapability in providing sufficient gain, in other words transconductance, to mitigate the losses at high frequency. This becomes even more drastic when N increases, since total losses of gate and drain are defined by $N(\alpha_g l_g)$ and $N(\alpha_d l_d)$, as shown in (2.11).



(a) (b)

Figure 4.20: 3D DSE plot showing possible lengths for (a) shunt μ-TL (TL_{Lg}) and (b) series μ-TL (TL_{Lds}), with respect to W_{CS} and N.

4.4 Conclusion

This chapter started by introducing the idea of loss-compensation for DAs where it showed to be a promising topology for extending and flattening the passband response. The necessary graphical and mathematical analysis of its function was provided. It was shown to influence the passband response through regulating both the input (gate) and output (drain) loaded-line losses (Figure 4.7). In addition, a technique for modeling this cascode device in a matrix-form and use it in MATLAB was demonstrated that enables a complete representation of the cascode device (Figure 4.10) and designing one through scripting.

Based on this concept and using the $ABCD$-matrix model provided in Chapter 3, a step-by-step algorithmic methodology was provided for the designer to implement in any scripting language he desires and explore the possible DA design solutions a given technology node can offer. For demonstration, in this work, the 55-nm CMOS ST process was used and 216 possible feasible DAs with BW ≥ 80 GHz were resulted to explore from.

Owing to this design process, graphical plots were produced that presented in an interesting 3D view the behavior of gain (Figure 4.15), bandwidth (Figure 4.16) and P_{DC} (Figure 4.17) with respect to both the transistor size and number of unit-cells used. Using them, the designers can now study and analyze the correlation between each design parameter and arrive at the optimum design point, as also demonstrated through Figure 4.19 for choice of μ-TL segments length and Figure 4.20 for choice of compensating inductor TL_{Lg} and TL_{Lds}.

In the next chapter, this DSE plots were used to choose a 100-GHz CMOS DA that offers the highest FoM of $GBP/P_{DC}$for implementation and on-wafer characterization.

Chapter 5

100-GHz Single Stage CMOS Distributed Amplifier

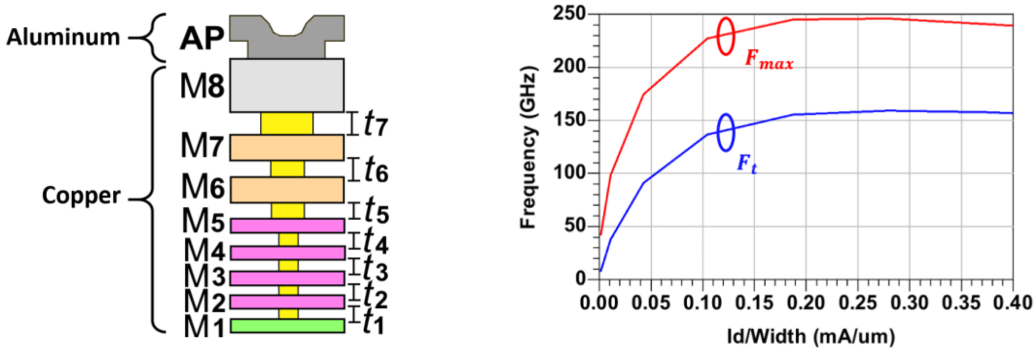
In the last chapter, using both the DA (3.14) matrix-based model with its unit-cell (3.17) representation, a systematic algorithmic methodology was proposed. Its aim is to explore, through scripting computer-automated algorithms, the possible amplifier gains and bandwidths obtainable from a given process node for any desired range of N and transistor size (W_{CS}). A design process was determined to be challenging to perform especially when using CAD tools in which N has to be manipulated manually. For demonstration, the 55-nm ST technology was used and the methodology was coded to automatically size CMOS-based DAs for a range of $2 \leq N \leq 9$ and 14 μm$\leq W_{CS} \leq 40$ μm. A total of 216 feasible solutions were obtained with design space solutions covering 80 GHz ≤ BW ≤ 130 GHz and ≈0 dB ≤ $\text{Gain} \leq 12$ dB. In this chapter, focus is put on DA solutions that amplify up to 100 GHz and choosing the one that demonstrates global optimum GBP/P_{DC} merit for on-wafer implementation and characterization.

This chapter is structured as follows. Section 5.1 starts by describing the 55-nm ST technology process used. Section 5.2 covers the circuit design part. It demonstrates how the obtained 3D DSE plots from Chapter 4 were used to pinpoint the global optimum 100-GHz DA that satisfies our defined FoM criterion. Section 5.3 covers the circuit implementation part of the latter DA. Here, a new stacked parallel plate shunt capacitor [61] with high quality factor at mm-waves and high self-resonance frequency (SRF) reaching 368 GHz is introduced. Section 5.4 discusses the experimental results of the fabricated DA circuit. A comparison with the performance of the state-of-the-art CMOS DAs, from Chapter 2, is presented in Section 5.5. Finally, Section 5.6 concludes and summarizes this chapter.

.

5.1 STMicroelectronics 55-nm Node Process Technology

The technology process adopted in this work is introduced first since it will aid in providing a better visualization for when discussing integrated components and circuit realization. In this work, the eight-metal version of the 55-nm ST process is used.



(a) (b)

Figure 5.1: (a) Simplified cross-section of metal stack and (b) transistor F_t and F_{max} as a function of drain current per unit gate width for nMOSFET available with ST eight-metal version 55-nm process.

As illustrated in Figure 5.1, this process uses copper metallization with eight metal layer backend and aluminum metallization with the top-most metal later (AP) used for pads probing. Its back end of line (BEOL) is composed of one ultra-thick top metal layer (M8) on top of two thick metals (M7 and M6), in order to sustain high current densities and to reduce sheet resistance for high-quality passive circuit design in Analog/RF applications. Beneath them, five thin lower layers (M5-M2 and M1) are available for dense interconnections and contact with silicon devices. Under optimal bias conditions, nMOS transistors offer a unity-gain cutoff frequency (f_t) and maximum power-gain cutoff frequency (f_{max}) of 160 GHz and 246 GHz, respectively, suited for mm-wave applications.

5.2 100-GHz Single-Stage CMOS DA: Circuit Design

This section concentrates on explaining how we chose the optimum values for N and W_{CS} to design a CMOS-based DA with high GBP/P_{DC} merit. For this optimum design point, it also demonstrates how we determined the required dimensions for the inductive-type segments and the loss-compensation inductors, TL_{Lg} and TL_{Lds}, to synthesize its unit cell.

At the beginning of this manuscript, we stated our interest for DAs that cover a minimum BW of 50 GHz for the opportunity to offer futuristic 100 Gb/s and above data-rates systems. In order to benefit from meaningful results for performance analysis with already available works and gain better perspective on the DA model capabilities, our choice is designated on bandwidth performance similar to the evaluated DAs from the literature presented in Chapter 2. It is noticeable that related works on silicon-based DA provided amplification up to around 100 GHz. Therefore, for a fair comparison, we decided to implement an amplifier device with similar passband. It should be noted that even higher

BWs are possible for realization using 55-nm process, reaching as high as 130 GHz as indicated by Figure 4.16, but were ignored in the scope of model validation.

To determine the possible options for such BW criterion, the first step is to sort the available solutions from Figure 4.16 for an upper-corner frequency of 100 GHz. Since the available solutions do not present exact values of 100 GHz but around it, we decided to relax our search margin with a spread of ±2 GHz, i.e. we picked DA solutions that present 98 GHz $\leq$ BW $\leq$ 102 GHz. This led us to obtain a narrower DSE range of 35 possible options to choose from instead of the 216 options, as shown in Figure 5.2, with their respective gain and the required values of N and W_{CS}.

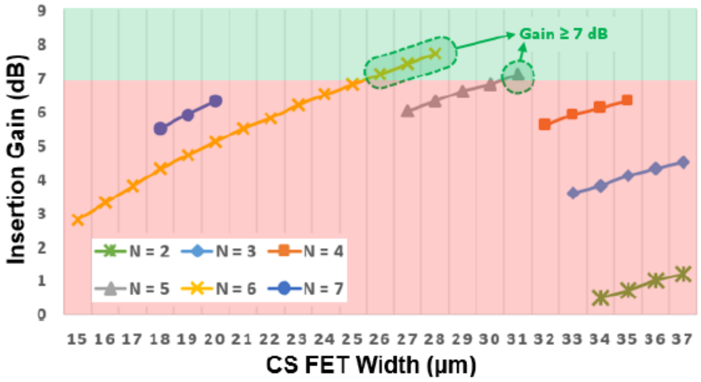


Figure 5.2: Insertion gain of thirty-five DA design options, with respect to N and W_{CS}, that offer 98 GHz $\leq BW \leq$ 102 GHz.

As a second step, from this new set of 35 solutions, we analyze how DC efficient is each DA option when delivering its own insertion gain. This can be performed through Figure 5.3, where GBP/P_{DC} performance for each of the 35 DAs is plotted with the required values of N and W_{CS}. It is visible, in our case, that this performance varies between 7.2 GHz/mW and 8.4 GHz/mW, with the relatively lowest values being for the DA options delivering higher gain.

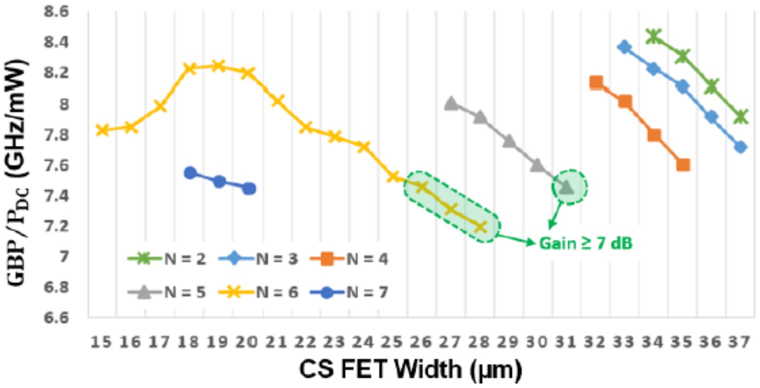


Figure 5.3: GBP/P_{DC} merit of thirty-five DA design options, with respect to N and W_{CS}, that offer 98 GHz $\leq BW \leq$ 102 GHz.

From here, the final step now depends on the application purpose of the DA; either the most P_{DC}-efficient DA with degradation in gain or the highest gain with a degradation in P_{DC}. Since our interest by the end of this thesis work is to publish our research efforts in order to assist in future mm-wave DA designs, our search was focused towards DAs that demonstrate comparable gain to the already published single-stage CMOS DAs; this is in order to highlight the added value from using our design technique. Doing so leads us to an even more restricted range and from it, we chose the DA that offers high GBP/P_{DC} merit.

Referring back to the sate-of-the-art Table 2.2, the minimum gain published for single-stage CMOS DA is 7 dB; consequently, from Figure 5.2, our options were restricted to only four options (highlighted in green): a six unit-cells DA with 26 µm ≤ W_{CS} ≤ 28 µm and a five unit-cell DA with W_{CS} =31 µm. Since it was of our interest here to also implement a P_{DC}-efficient amplifier, choice was directed on DAs offering high GBP/P_{DC} between those four options; thereby, from Figure 5.3, our choice is now limited to either choosing a DA with $N = 6$ and $W_{CS} = 26$ µm or a DA with $N = 5$ and $W_{CS} = 31$ µm, respectively, where both offer ≈7.4 GHz/mW of GBP/P_{DC}.

To choose from those two options, we opted for the DA with the smallest core area. This requires pre-knowledge of how the DA will be implemented. In this work, all inductors are implemented as conventional microstrip lines; by referring to Figure 4.18, it is clear that TL_{Lds} has a dominant role in defining the physical height of the unit cell and hence of the DA. Thereby, from the DSE plot in Figure 4.20(b), that gives the required lengths for TL_{Lds}, it was deduced that the five unit-cells DA option offers 31% less core area than its six unit-cells counterpart since its loss-compensation inductors are smaller in value.

As a result, the DA solution made from $N = 5$ unit-cells with $W_{CS} = 31$ µm is determined to be our global optimum choice for circuit implementation and on-wafer characterization. Figure 5.4 shows the loss-compensated DA preliminary schematic diagram with its design parameters summarized in Table 5.1 and its design characteristics in Table 5.2. This DA will provide a simulated gain of 7 dB up to 100 GHz with a P_{DC} of 30 mW. It is composed of five loss-compensated cascode Gm-cells, placed at a distance of $2 \cdot (l/2)$ from each other; where the unit-cell segment length $(l/2)$ is 131 µm. Transistor M1 is set to 31 μm width and M2 twice that, i.e. 62 μm. To compensate the high losses at 100 GHz while maintaining 1-dB of midband gain drop, a TL_{Lg} and TL_{Lds} of 43 µm and 129 µm, respectively, are needed as indicated by Figure 4.20. To prevent voltage drop across the termination resistors R_3 and R_4 when biasing the DA, the latter are AC-grounded through bypass capacitors C_S. In addition, TL_{Lg} is AC-grounded through a capacitor C_g.

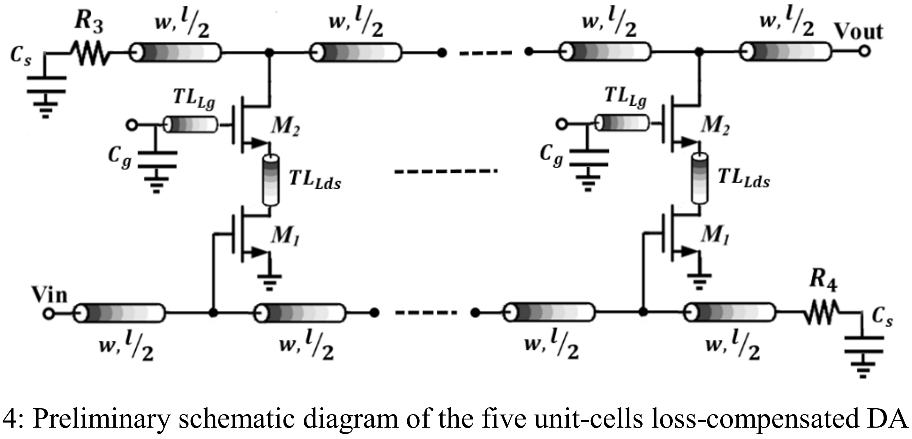


Figure 5.4: Preliminary schematic diagram of the five unit-cells loss-compensated DA (biasing not shown). Both C_s and C_g are shunt capacitors to insure AC ground connections.

TABLE 5.1: SINGLE-STAGE DA DESIGN PARAMETERS DETERMINED FROM CAUTOD PROCESS

N	M1 (µm)	M2 (µm)	TL Segments $(l/2)$ (µm)	$\mathrm{TL_{Lg}}$ (µm)	$\mathrm{TL_{Lds}}$ (µm)
5	31	62	131	43	129

TABLE 5.2: SINGLE-STAGE DA PRELIMINARY DESIGN CHARACTERISTICS

Gain (dB)	Bandwidth (GHz)	$\mathrm{P_{DC}}$ (mW)	Gain Ripple (dB)	GBP (GHz)	$\mathrm{GBP/P_{DC}}$ (GHz/mW)
7	Up to 100	30	±1	224	7.46

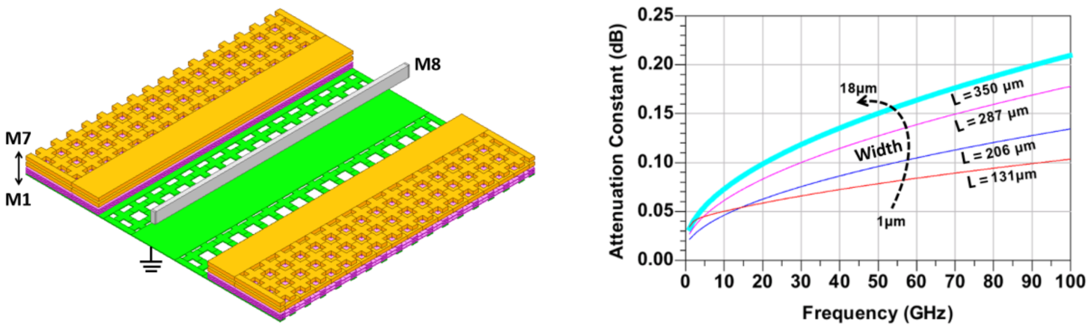
It is worth highlighting how the circuit design process was simple, fast and direct. Owing to our matrix-based DA model (3.14), with its unit-cell model (3.17), and the possibility it offers for automating N and W_{CS} through MATLAB, analog designers can just directly pick their optimum design point in an interesting graphical way for any FoM they please. There is no need to change N manually and run optimization for each time a design parameter is modified in order to search for possible improvement in performance. In the next Section 5.3, the layout aspect is covered and Section 5.4 covers the experimental results of the on-wafer measurements.

5.3 100-GHz Single-Stage CMOS DA: Circuit Implementation

This section discusses the layout implementation side of the previously chosen circuit. In subsection 5.3.1, the microstrip line topology used for implementing all type of inductors making the DA from unit-cell segments, TL_{Lg} and TL_{Lds} is presented. In subsection 5.3.2, a new high quality stacked parallel plate shunt-capacitor, used to implement C_S and C_g, is introduced. In subsection 5.3.3, the MOS transistor interconnection that are used when implementing are presented. Finally, subsection 5.3.4 is devoted to presenting the final implemented layouts of both unit-cell and DA with their own on-chip microphotographs.

5.3.1 Microstrip Transmission Line

For the TL, we have taken advantage of the accurate and flexible models that are provided in the PDK since they are based on pre-measurements from the semiconductor foundry. Its topology is presented in 3D view in Figure 5.5(a). Metal 1 (M1, in green) is the ground floor, metals 2 to 7 (M2 to M7) are used for complying with the local density rules and are connected to the ground while metal 8 (M8) is the signal strip.



(a) (b)

Figure 5.5: (a) Isometric 3D view of the microstrip line. (b) Its attenuation constant when implementing a 76-pH inductor for different width and length.

Figure 5.5(b) illustrates the attenuation constant (α_{TL}) of the TL with respect to frequency for different widths ranging from 1 μm to 18 μm (limit imposed from PDK). For a fixed inductance of 76 pH, which represent the needed value to synthesize the unit cells segments, it is noticeable that the smaller the width, the lower α_{TL}. It might seem that any μ-TL configuration has negligible loss impact; however, it must be noted that a DA is made of two inductive segments cascaded N times, as evident in Figure 2.18. This means that the input microwave signal will propagate through a total of 2×N physical segments, in other words it will experience 2·N times the losses, on both the loaded input and output lines of the DA. Therefore, having the smallest width for TL can benefit from having the smallest length that aid in reducing surface area of the DA when implemented and it contributes in lowering the overall losses of the DA.

Since the 5-unit cells DA that we chose consumes 30 mW from a 1.2-V supply (25 mA), and on the bases of the DC-current handling limits expressed on the Design Rule Manual (DRM), we adopted for a width of 1 μm. We also decided to apply the same 1 μm width for all μ-TLs with the aim of having later on a simpler design implementation process where all the lines will share the same width.

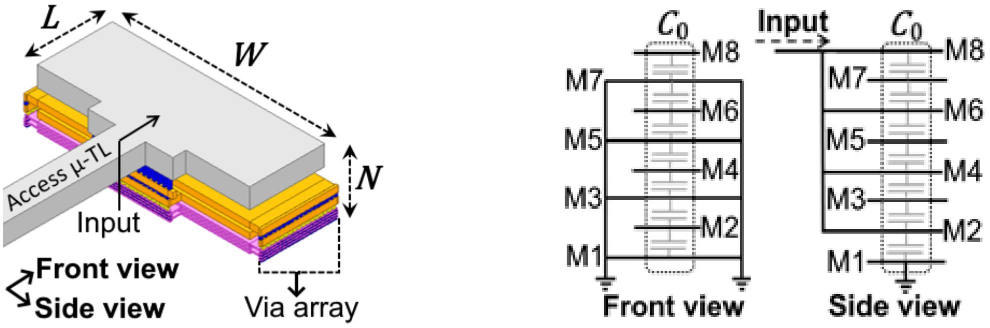
5.3.2 High Quality and SRF Stacked Parallel Plate Shunt Capacitor [61]

A common issue when synthesizing circuits at mm-wave is having at hand suitable passive components that demonstrate high quality (Q) factor. As made clear from the capacitor Q-factor formula ($Q = 1/(\omega \cdot R \cdot C)$ for $\omega < (2 \cdot \pi \cdot SRF)$; where ω is the angular frequency, R is the equivalent parasitic resistor, C is the equivalent parasitic resistor and SRF is the self-resonance frequency), its Q-value is constantly experiencing decrease with increase of operating frequency, thereby highlighting, in a general context, that capacitors may become a bottleneck for high performance mm-wave ICs. In this work, referring to Figure 5.4, capacitors C_S and C_g are used to provide DC decoupling and AC grounding for the termination resistors and inductor TL_{Lg}, respectively.

As a solution, we proposed an on-chip passive stacked parallel plate shunt-capacitor (SPP-SC) [61], constructed without additional process steps and with focus on mm-wave performance. To prove its mm-wave performances, the proposed SPP-SC is compared with other state-of-the-art capacitor topologies found in the literature in addition to a woven-type MOM capacitor already available in the 55-nm ST process design kit.

5.3.2.1 Stacked Parallel Plate Shunt Capacitor

Figure 5.6(a) depicts the physical structure of a 300-fF SPP-SC synthesized within existing masks using the 8-metal version of 55-nm process and Figure 5.6(b) illustrates a symbolic view of its concept on how the process BEOL stack is used.



(a) (b)

Figure 5.6: 300-fF SPP-SC (a) 3D isometric view, and (b) symbolic front and side views of its topology.

The odd metal plates are linked together by a stack of via array placed on each side of the capacitor distributed in the longitudinal direction; this is to lower the resistive and inductive parasitic, where path towards ground for current density is shorter. It also contributes in confining the electric field within the plates, which contributes to the increase of capacitance and prevent coupling with adjacent components. The even metal plates are linked together from the front by a stack of via array and the stack is considered as the access side. The multi-plate structure offers several parallel paths, thus minimizing AC current density and lowering even more the aforementioned parasitic. Both via and structure configurations give rise to a capacitor with an overall high Q and SRF merits, as will be demonstrated when discussing its on-wafer measurements.

$$C_0 \cong \varepsilon_0 \cdot W \cdot L \cdot \sum_{n=1}^{SF-1} \frac{\varepsilon_{r_n}}{t_n} = W \cdot L \cdot C_d \qquad (5.1)$$

From Figure 5.6(b), design equation (5.1) can be deduced and used as a first approach, before layout implementation, to size the required the design variables: physical dimensions (L x W) and stacking factor (SF), to obtain a desired intrinsic capacitance (C_0) value. The term SF is the number of metal plates desired and made available from a given technology node. Terms ε_{r_n} and t_n are the relative permittivity and thickness of each dielectric layer, respectively, and ε_0 is the permittivity of free space. From (5.1), the benefit of the proposed topology can also be perceived: as SF increases with process node advancement, higher capacitance density per unit area (C_d) is expected.

Referring to the state-of-the-art work on high-frequency passive capacitors [62]-[66], similar works presented capacitors on the order of 300 fF at most. On that bases, and since by the end our main objective is to compare with what already exists by fixing a parameter and showing the added values, the capacitance C_0 in (1) is set to 300 fF. To demonstrate the proposed capacitor performance, the 300-fF SPP-SC is designed as follows. The entire metal stack of 55-nm node, i.e. $SF = 8$, is used to maximize to total C_d ($\approx 0.91\ \mathrm{fF/\mu m^2}$)

for smaller dimensions and, also, to lower parasitic. Referring to Figure 5.6, reducing W contributes to lower capacitor self-resistance, since GND connections from each side will be closer to the capacitor input; however, since the metal layers of our capacitor share equal dimensions, we were restricted by our Design-Rule-Manual (DRM) rules of the stringent thin-metal layers (M1-M5) length (L). Thereby, L is restricted up to 10.8 µm, what led to a wider width (W) of 30.6 µm, accepted by the DRM, in order to preserve C_0 at 300 fF, (1). Figure 5.7 illustrates the microphotograph of final capacitor for on-wafer measurements.

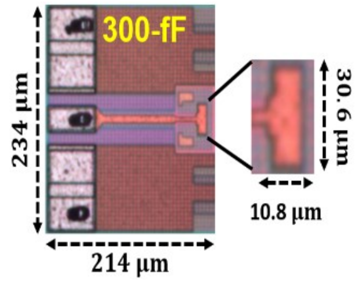
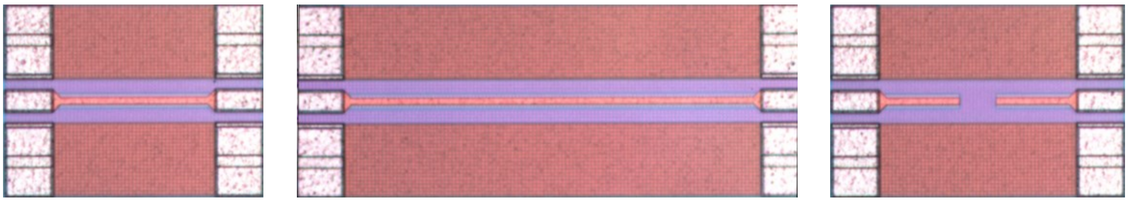


Figure 5.7: Microphotograph of the fabricated 300-fF SPP-SC.

5.3.2.1 On-wafer Characterization and Simulation Results

The S-parameters of the capacitor was measured via on-wafer probing using Anritsu 2-port VectorStar ME7838D VNA setup. Conventional Thru-Reflect-Line (TRL) calibration method [67], with a 630-µm line and an open reflect, was then applied. The microphotographs of the TRL structures are shown in Figure 5.8.



(a) (b) (c)

Figure 5.8: Microphotograph of the fabricated Thru-Line-Reflect calibration kit.

The de-embedded capacitor can be represented as the electrical equivalent model illustrated in Figure 5.9; where R_0, L_0 and C_0 are the intrinsic resistance, inductance and capacitance, respectively, and C_{eff} is an effective capacitance that represents L_0 in series with C_0.

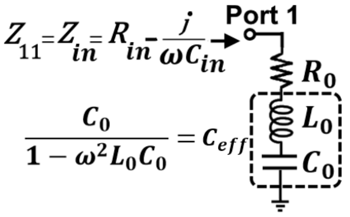


Figure 5.9: SPP-SC equivalent electrical model. (R_0, L_0, C_0) represents intrinsic lumped-elements of the capacitor and (R_{in}, C_{in}) represents the measured input-impedance.

To characterize those elements, S- to Z-parameter conversion is first performed [56]. Intrinsic resistor R_0 is determined from the measured capacitor equivalent input-series resistance (R_{in}), (5.2a). Intrinsic capacitance C_0 (5.2b) is determined from the measured capacitor equivalent input series-capacitance (C_{in}) using (5.2c) and the intrinsic inductance L_0 is determined from (5.2d) where $\omega|_{Q=0}$ is the angular frequency at SRF since $\Im\text{m}\{Z_{11}\}|_{Q=0} = 0$.

$$R_{in}(\omega) = \Re e\{Z_{11}\} \tag{5.2a}$$

$$C_0 = C_{in}|_{\omega\approx 0} \tag{5.2b}$$

$$C_{in}(\omega) = C_{eff}(\omega) = -\frac{1}{\omega \cdot \Im m\{Z_{11}\}} \tag{5.2c}$$

$$L_0 = \frac{1}{\left(\omega|_{Q=0}\right)^2 \cdot C_0} \tag{5.2d}$$

$$Q(\omega) = -\frac{\Im m\{Z_{11}\}}{\Re e\{Z_{11}\}} \tag{5.2e}$$

Figure 5.10 illustrates the measured and simulated RLC-elements against frequency for the implemented 300-fF SPP-SC. The capacitor experience a relatively constant R_{in} against frequency with a measured average magnitude of 0.37 Ω. The increase of resistance at frequencies below 6 GHz is attributed to the lower limit of TRL defined by the 630-μm line. Since R_{in} is shown here to have a flat variation in the measurements frequency range, it can safely be considered as a lumped R_0. The slight difference in extracted resistance between EM simulation and measurement results could be attributed to limitation in our equipment to accurately quantify very low losses. The proposed topology provides a relatively constant value of C_{in} within the frequency range considered, signifying that the SRF are all beyond our measurement limit (100 GHz). Measured intrinsic capacitances C_0 of 285 fF is obtained for the calculated 300-fF. The slight difference between what was calculated (5.1) and measured could be due to process variation in dielectric layers permittivity (ε_r).

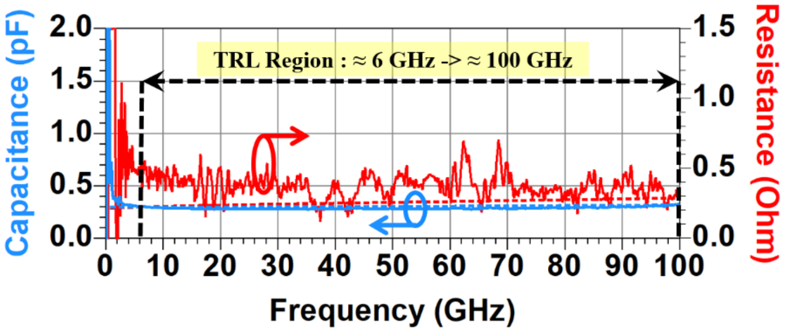


Figure 5.10: Measured and HFSS EM-simulated equivalent input series-resistance (R_{in}) and capacitance (C_{in}) of de-embedded 300-fF SPP-SC. (Solid line: Measured. Dashed line: EM Simulated)

The measured Q-factor is plotted in Figure 5.11 using $Q(\omega)$ from (5.2e). Q-value of 14.7 is obtained at 100 GHz. It must be noted that the drop of Q-value here is dominated by the increase of frequency rather than resistance, since from Figure 5.10 it is clear that R_{in}, at any given frequency, remains almost the same. The proposed capacitor also contributes to a high SRF merit, as demonstrated in Figure 5.11, where measured Q-factor is extrapolated using MathWorks MATLAB and SRF is then extracted at frequency in which $Q = 0$ (since $\Im\mathrm{m}\{Z_{11}\}|_{Q=0} = 0$). The 300-fF capacitor is estimated to reach an SRF of 368 GHz.

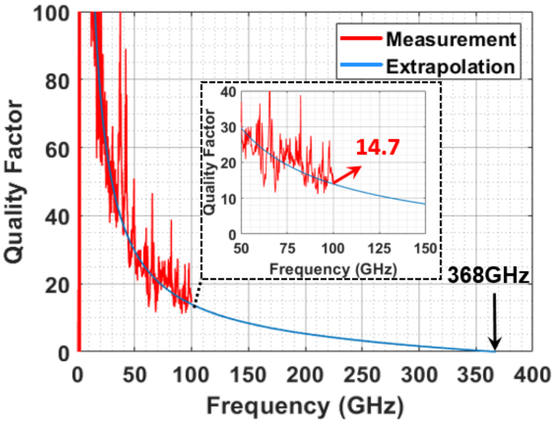


Figure 5.11: Estimated SRF for 300-fF SPP-SC capacitor, extracted at $Q = 0$ through extrapolating the measured Q-factor.

Using those values, L_0 is then obtained using (5.2d) and summarized within Table 5.3 with the other intrinsic elements modeling the SPP-SC in addition to the values extracted from EM simulation. A slight difference in the extracted values of L_0 exists between measurement and simulation. This is due to the measured L_0 being determined from an extrapolation of a measured Q-factor with evident distortion caused by the measured low-value resistance fluctuation against frequency, as illustrated in Figure 5.10.

TABLE 5.3: EXTRACTED INTRINSIC LUMPED ELEMENTS OF 300-fF SPP-SC.

Capacitor	**R_0 (Ω)**		**C_0 (fF)**		**L_0 (pH)**	
	Meas.	**EM Sim.**	**Meas.**	**EM Sim.**	**Meas.**	**EM Sim.**
300-fF	0.37	0.25	285	298	0.66	0.55

Figure 5.12 (next page) compares de-embedded to both lumped modeled (Figure 5.9) and EM simulated S_{11} parameters for all 300-fF SPP-SC. A very good agreement is obtained. This indicates how accurate the proposed physical model is up to 100 GHz.

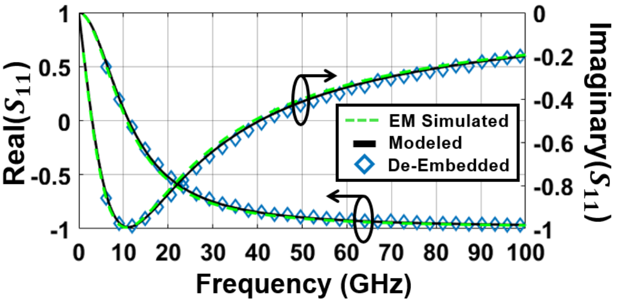


Figure 5.12: Equivalent electrical model validation through S_{11} parameter plot of 300-fF

5.3.2.2 Performance Comparison with State-Of-the-Art Capacitor Topologies

After introducing the capacitor topology with its on-wafer performance, a comparison with state-of-the-art capacitors is performed here. As part of AC-grounded components, radial stub [62] is used for its ease of design but reserves large chip area. Slow-wave stub [63] is proposed that benefits from length reduction; however, wider footprint is required resulting in comparable area. Metal-Insulator-Metal (MIM) capacitor is one topology that can offer high capacitance density due to its special high-k dielectric layer but suffers from high dielectric losses at mm-waves. In [64], a 120-fF MIM capacitor demonstrated a Q-value of 3.8 at 100 GHz. Also, the majority of low-cost CMOS technologies lack MIM capacitor options. Metal-Oxide-Metal (MOM) capacitor is an alternative option that uses existing metals in the process backend-of-line (BEOL) but experiences lower Q-values due to its structure consisted of narrow thin metal wires. For instance, a 129-fF woven-structure MOM capacitor provides a Q-value below 3.2 at 100 GHz, [65]. In [66], for a common multi-stack interdigital capacitor, the same value of 120-fF provided a Q-value of 2.5 at 100 GHz. In addition, MOM capacitors experience a rapid SRF reduction when higher capacitance value is desired which could be attributed to the substantial increase in its parasitic-inductance caused by its wire-type topology. It is also worth mentioning the simulation efforts where they require large processing resources since condensed meshing process is required for their closely spaced wires when optimizing ICs in full 3D-EM simulators. Other approaches referred to as active capacitors such as implementing gate oxide capacitors [64] exist to improve Q-factor and area-efficiency, but they need a DC bias and are strongly process and temperature dependent.

TABLE 5.4: PERFORMANCE COMPARISON BETWEEN WIDE BANDWIDTH AMPLIFIER TOPOLOGIES.

Ref.	Topology	Process Node	Stack Layers	C_0 (fF)	SRF (GHz)	$Q^{\&\%}$	Area (mm^2)	C_d ($fF/\mu m^2$)
[62]	Stub	65-nm	9	348	150	N/A	10053	0.035
[64]	MIM	65-nm	7	120	194	3.8	N/A	N/A
[65]	MOM	45-nm	7	129	160	< 3.2$^{£}$	129$^{\#}$	1
[65]	MOM	45-nm	7	215	110	0.5	196$^{\#}$	1.1
[66]	MOM	45-nm	11	120	140	2.5	32$^{\#}$	3.75
[66]	MOM	45-nm	11	350	75	< 0*	92$^{\#}$	3.8
This Work	**SPP**	**55-nm**	**8**	**285**	**368**	**14.7**	**331**	**0.86**

N/A = not available. $^{\%}$Estimated from plots. $^{£}$Estimated from Q-value provided at 60 GHz. $^{\#}$Estimated from fF/μm^2.
$^{\&}$Determined at 100 GHz. *Due to SRF being below 100 GHz.

Table 5.4 compares the measured capacitor performance with results from state-of-the-art capacitors. To the authors' knowledge, this work demonstrated a capacitor that offers the highest SRF and Q merits while providing large capacitance values for mm-wave frequency range. In terms of occupied area, it is true that the SPP capacitors reserved larger area between the stated ones [64]-[66], but this is attributed to the characterized SPP in this work having larger C_0. For the case of [66] 350-fF capacitor compared to the 285-fF SPP, the former presented compact area which is largely related to [66] using an 11-metal version of a 45-nm node compared to the 8-metal version of a larger 55-nm node used in this work and, also, at the expense of a lower SRF.

As a conclusion, measurements showed attractive performance from excellent quality factor and high SRF, making it suitable for analog systems operating until 100 GHz and possibly even up to 368 GHz, proving eligibility for both broadband and high data-rate ICs.

5.3.2.3 Performance Comparison with 55-nm Woven-Structure MOM Capacitor

In the design kit of the technology at hand, a common woven-structure MOM capacitor is available for usage as a parameterized cell (PCell). Figure 5.13 illustrates its topology where it makes use of existing metals (M2-M4) in the process BEOL.

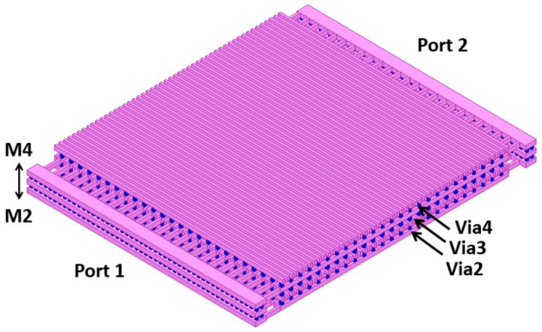
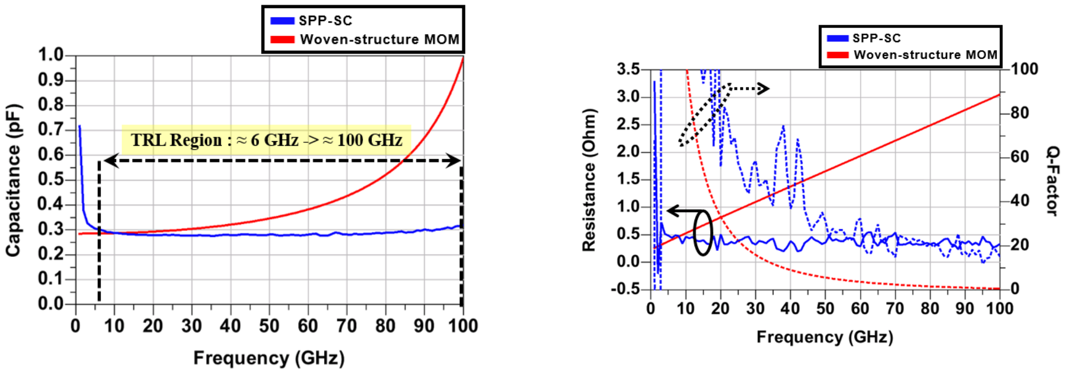


Figure 5.13: Cross section of a Metal 2/Metal 4 woven-structure MOM capacitor in 55-nm PDK

To justify even further the need for our proposed SPP-SC topology, a comparison with the mm-wave performance of this PCell MOM capacitor is also performed. For a fair comparison, the value of 300-fF capacitance was fixed for both topologies, and both resistance, capacitance variation against frequency and quality factors were plotted in Figure 5.14. The 300-fF PDK woven-structure MOM capacitor reserved area of 30.6 µm × 6.23 µm, a lower area relative to the SPP capacitor due to the woven-structure topology providing higher capacitance density per area (1.5 $\mathrm{fF}/\mu m^2$)



(a) (b)

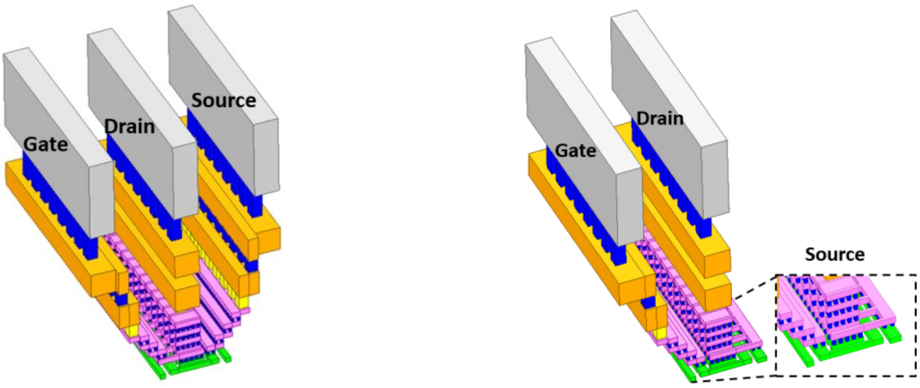
Figure 5.14: Measured (a) equivalent input capacitance, and (b) equivalent input resistance and Q-factor for 300-fF SPP-SC and woven-structure MOM capacitor in 55-nm process.

From Figure 5.14(a), for the same capacitance value of 300-fF, the SPP-SC demonstrated flat capacitance variation against frequency, which signify an SRF well above 100 GHz (close to 368 GHz as determined from Figure 5.11), whereas the woven-structure PDK MOM demonstrates a rapid increase in capacitance which signify its SRF is close to 100 GHz. From Figure 5.14(b), the SPP-SC delivers a self-resistance much lower than that of the PDK MOM capacitor and hence a much desirable quality factor at millimeter wave regions. At 100 GHz, the former capacitor has 0.33 Ω of self-resistance and $Q = 14.7$, whereas the latter capacitor has 3.1 Ω of self-resistance and $Q = 0.53$.

Through this analysis, we validated even more the efforts taken to propose a different capacitor than the already available ones for the purpose of gaining better overall performance when designing our 100-GHz DA and any mm-wave ICs in a general context.

5.3.3 MOS Transistor Interconnection

The transistor connection is crucial in mm-wave design. In order to reduce the resistive losses that can load the DA and hence degrade its passband, we have adopted the topology illustrated in Figure 5.15 during layout implementation. The CG-FET uses the one of Figure 5.15(a) where gate-, drain- and source- pins are accessed through M8, and the CS-FET uses the same one (Figure 5.15(b)), but with source-pin directly shorted to GND plane.



(a) (b)

Figure 5.15: Isometric 3D view of the interconnection used. (a) CG-FET. (b) CS-FET.

5.3.4 Standalone Unit-Cell Layout and Microphotograph

A single unit cell is implemented as a standalone device for the purpose of validating the proposed model (3.17) frequency behavior with measurements through S-parameters characterization.

Referring to the design parameters determined in Section 5.2 (Table 5.2) and the electrical schematic provide in Figure 5.4, and using both the microstrip line topology, the proposed SPP capacitor topology for implementing C_g as a decoupling capacitor and the transistor interconnection introduced in subsection 5.3.1, 5.3.2 and 5.3.3, respectively, the unit cell can be synthesized as shown in Figure 5.16. Due to the high SRF and quality factor of a single SPP-SC capacitor, as was determined in Figure 5.10, we were able to provide a strong AC-ground at the upper end of the 43-µm TL_{Lg} facing the DC-input side and with SRF well above 100 GHz. Figure 5.17 illustrates the microphotograph of this unit cell as a standalone circuit. Extra DC pads were attached on top for biasing gate-pin of the CG transistor (M2) through external power supply. For the drain pin of transistor M2 and gate pin of transistor M1, biasing is provided through the RF-pads by the probes of the VNA.

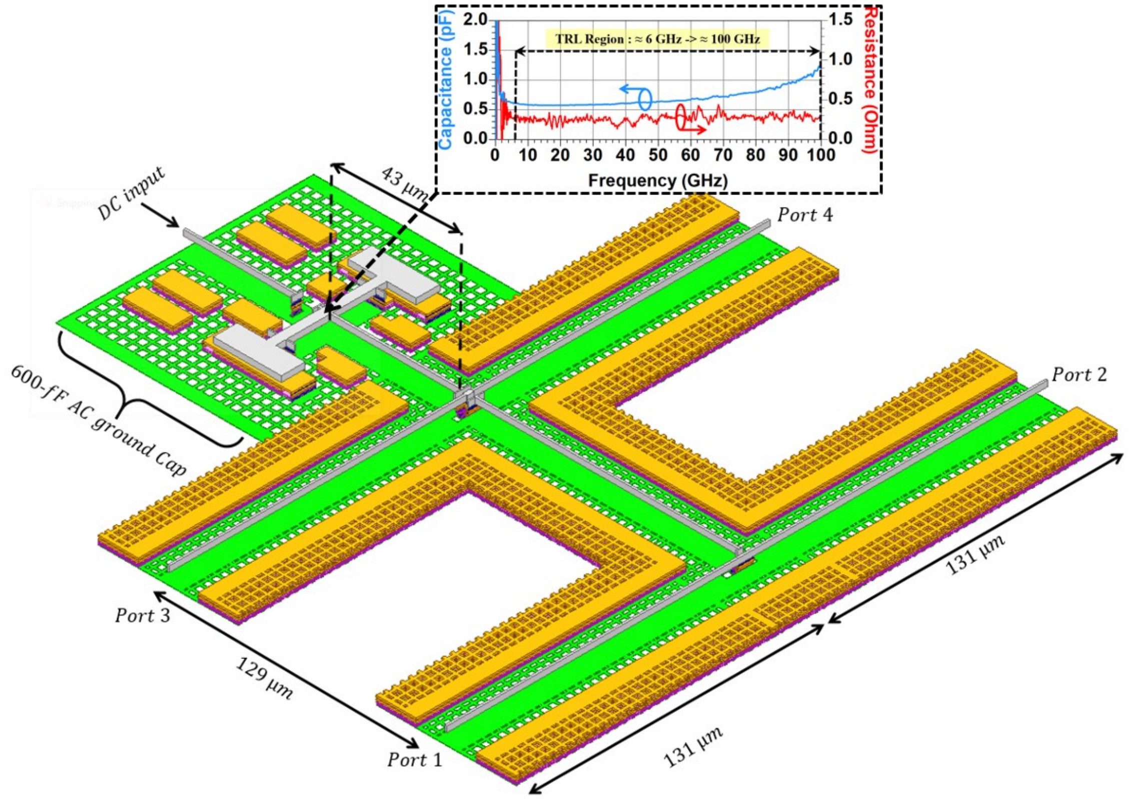


Figure 5.16: Isometric 3D representation of a single unit cell with loss-compensated cascode as Gm-cell attached to a 600-fF AC grounded SPP capacitor C_g.

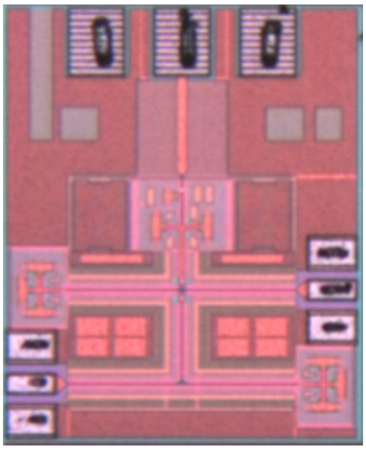


Figure 5.17: Microphotograph of the fabricated standalone unit cell in 55-nm process for on-wafer characterization.

5.3.5 100-GHz Single-Stage DA: Layout and Microphotograph

In order to achieve the targeted 7 dB of gain up to 100 GHz, we need to connect five replicas of the same unit cell, Figure 5.4, together as suggested by the design method. Figure 5.18 (next page) presents the final electrical schematic diagram of our loss-compensated CMOS-based DA. Table 5.5 summarizes all of its design parameters values used during layout implementation. All µ-TL were implemented using thickest metal available in technology, M8, with same width of 1 µm, as explained in subsection 5.3.1. The µ-TL segments are done with length $l/2$ of 131 µm. Both TL_{Lg} and TL_{Lds} are implemented with length of 43 µm and 129 µm, respectively. Both termination impedances Z_3 and Z_4 are realized as series RC loads. Both R_3 and R_4 are implemented using technology component as N+ silicided polysilicon resistors, and were AC-grounded through a 1-pF bypass SPP capacitor (C_S for both C_3 and C_4) to have a DA passband starting from 10 GHz; as was already stated in Chapter 4 design algorithm (Step 4), we decided to go with the highest F_{lower} of 10 GHz instead of 1 GHz, for instance, since they showed equal gain; but choosing higher frequency will benefit us from having a bypass capacitor with a small on-chip area, hence smaller DA. After finishing the design layout implementation and before sending to fabrication, one last simulation (as a validation step) was performed on ADS schematic to make sure that everything is in order. R_3 and R_4 had to be refine hand-tuned to 53.5 Ω to slightly readjust the passband midband gain drop to be precisely at 1-dB limit. This step is not always necessary and can vary from one designer to another. But, it could be considered as a possible quick solution when slight re-adjustment is required at the end-stage before sending to fabrication instead of, for instance, increasing TL_{Lds} that will affect the height of the DA (even if TL_{Lds} was slightly increased) and forces the designer to redo the synthetization process once more followed by DRC/GAG validation procedure.

TABLE. 5.5: DA CIRCUIT DESIGN PARAMETERS FOR LAYOUT IMPLEMENTATION

N	M1 (µm)	M2 (µm)	TL Segments ($l/2$) (µm)	TL_{Lg} (µm)	TL_{Lds} (µm)	R_3 (Ω)	R_4 (Ω)
5	31	62	131	43	129	53.5	53.5

Supply voltages for the gate pin of each M1 FET and the drain pin of each M2 FET are provided through RF-probes by the measurement setup. The gate pins of M2 FETs are biased together by an external bench power supply delivered from G-DC-G pads and through resistor-type RF-chokes (R_g) implemented using high-resistivity polysilicon resistor of 10-kΩ. This is possible since we are dealing with FET and hence there is no impact on overall P_{DC}. A 600-fF decoupling SPP capacitor (C_g) was added on L_g terminal pin facing the DC pads for AC-grounding.

Finally, GSG-type RF-pads with 50-µm pitch are connected to DA input and output ports. Both the final DA layout view and microphotograph are shown in Figure 5.19 and Figure 5.20, respectively. The DA presents a core are of 0.52 mm^2 and total area of 0.83 mm^2 including pads.

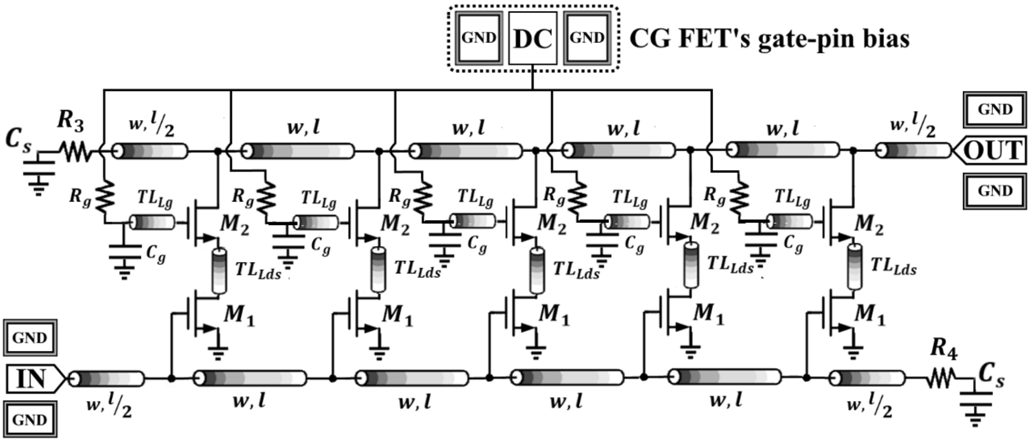


Figure 5.18: Circuit schematic of the 5 unit-cells 100-GHz CMOS-based DA.

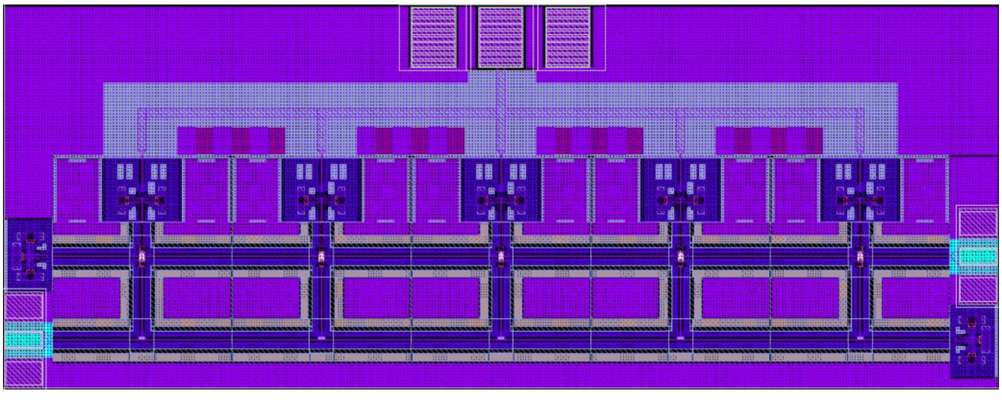


Figure 5.19: Layout view of the implemented 5 unit-cells 100-GHz CMOS-based DA.

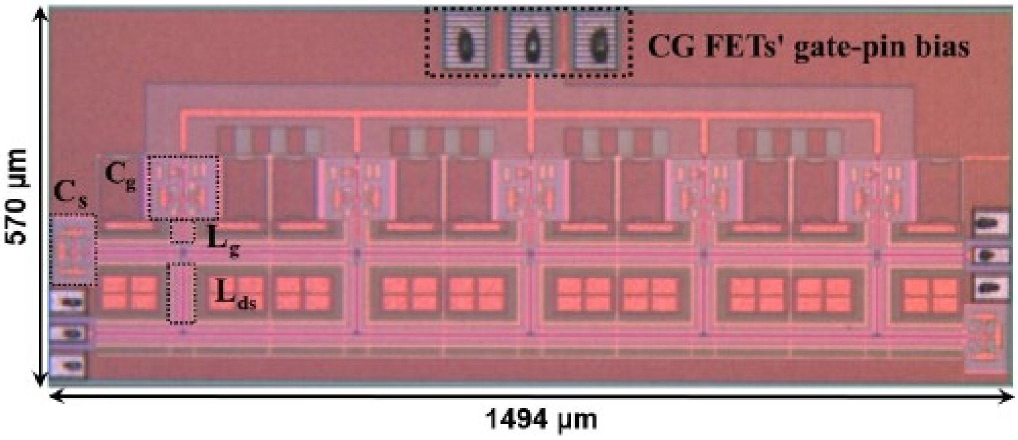


Figure 5.20: Microphotograph of the fabricated 5 unit-cells 100-GHz CMOS-based DA in 55-nm process for on-wafer characterization.

5.4 100-GHz Single-Stage CMOS DA: Experimental Results

In this section, simulation and measurement results of the amplifier device are presented and compared. The measurement setup is first introduced in subsection 5.4.1. The S-parameters analysis of both the unit-cell and DA are discussed in subsection 5.4.2. In subsection 5.4.3, a performance analysis of the implemented DA is carried out. Here, stability and group delay analysis are presented in addition to power capabilities analysis from 1-dB gain compression point (P1dB), saturation power ($\mathrm{P_{sat}}$) and third order intercept point (IP3). Finally, a comparison with state-of-the-art CMOS DAs is carried out in Section 5.5.

5.4.1 Vector Network Analyzer Description

All S-parameters measurements are performed via on-wafer probing using the VNA setup shown in Figure 5.21.

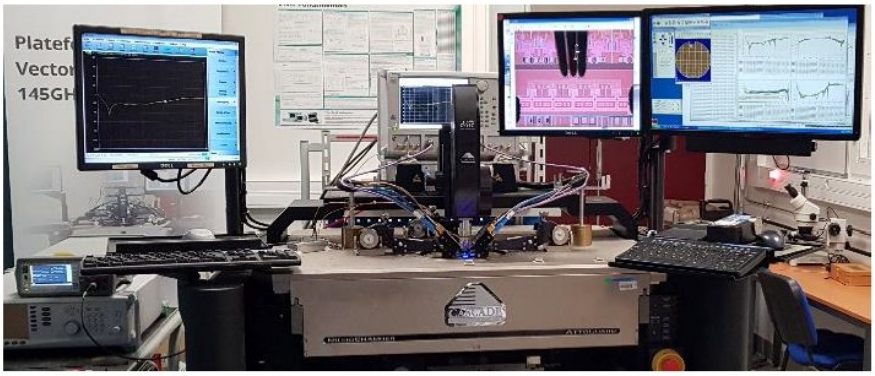
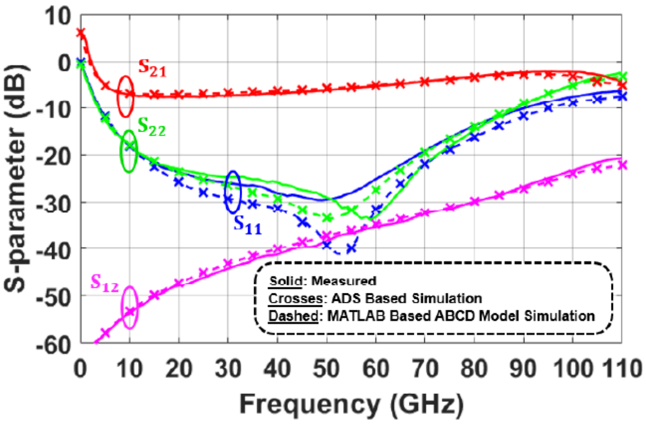


Figure 5.21: Bias-tee simulated and measured isolation (S_{21}) versus frequency between DC- and RF- ports.

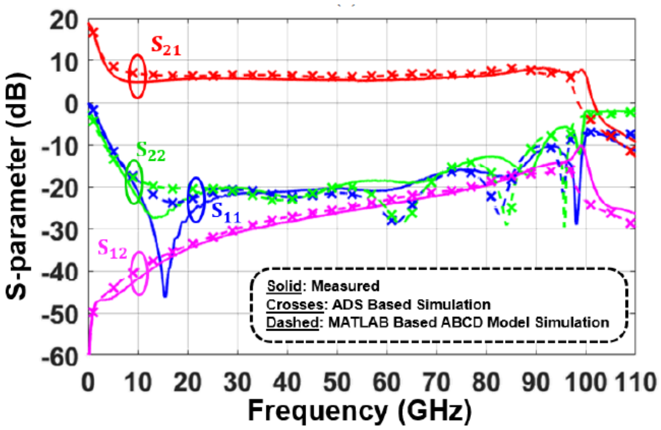
This setup consists of an Anritsu 2-port VectorStar ME7838D mm-wave system available with the MS4640B series Vector Network Analyzer (VNA) and the 3739C test set to control two MA25300A mm-wave modules, each connected to Cascade Microtech Infinity GSG 50-µm pitch probes. Both MS4640B and 3739C devices cover frequencies < 54 GHz then transition towards MA25300A modules occurs to cover ranges above 54 GHz. For biasing, two external bench power supplies are used, Keysight B2901A to bias the gate pins of cascode CG FETs and Keysight B2902A to provide bias along the loaded gate- and drain-line of the DA through RF probes. VNA calibration using line-reflect-reflect-match (LRRM) technique was performed before measurements to remove probing RF impact.

5.4.2 S-parameters Analysis: Unit-Cell and DA Model Validation

Figure 5.22(a) and Figure 5.22(b) compare the S-parameter results versus frequency obtained from MATLAB-based $ABCD$-model simulation, (3.14) with (3.17), to both ADS-based simulation and measurement of a single unit-cell and DA, respectively. Great agreement is obtained between ADS and $ABCD$-model results. This indicates how reliable the proposed model is when used as design tool, this support the forth criterion. Unit-cell pads were de-embedded from measurements but the DA pads were not for a better representation of the latter behavior when used as standalone IC in real-world applications.



(a)



(b)

Figure 5.22: S-parameters simulation and measurement results versus frequency. (a) Single unit cell. (b) DA.

Biased at V_{DD} =1.2 V, the unit cell consumed an overall measured current of 5 mA and the DA consumed 25 mA—same consumptions when calculated during design process using (4.9). This resulted in a measured P_{DC} of 6 mW and 30 mW, respectively. The DA achieves an average insertion gain S_{21} of 6.7 dB. A peak gain of 8 dB is observed at 91 GHz resulting in an in-band ripple of ±1.3 dB when referenced to mid-band gain and, hence, a coverage range from F_{lower} of 16.7 GHz up to an F_{upper} of 100 GHz. This gives an amplified passband BW of 83.3 GHz and leads to a GBP of 180 GHz. The slight difference (3.3 GHz) at the upper side of the frequency spectrum, where the measured DA reaches higher frequencies compared to the simulated one, could be attributed to a slight overestimation of the parasitic the transistors used are made from. The increase of gain at frequencies < 10 GHz is attributed to the small bypass capacitor (C_S) used to cover down to 10 GHz (a decision we made in Step 4 of our design methodology in subsection 4.2.2). This can be improved by either using larger C_S (MIM capacitors in this case could be considered for their larger capacitance density) or shorting both R_3 and R_4 directly to GND as illustrated in Figure 4.1. The latter option will offer a DA with a flat gain starting from DC level, but at the expense of higher P_{DC} since DC-current will pass through those resistors (caused by the DC-voltage bias along the output loaded-line for R_3 and along the input loaded-line for R_4). The dip in gain between F_{lower} and 10 GHz is caused by an overestimation of loaded-lines termination resistances during implementation. Both input and output matching levels, S_{11} and S_{22}, respectively, are better than -10 dB starting from 4.35 GHz. The amplifier maintains input matching up to 100 GHz while the output matching remains < -10 dB up to 91.6 GHz with a slight dip back at 99 GHz. The reverse isolation S_{12} is less than -50 dB below 1 GHz and reaches a maximum of -10 dB at 100 GHz. The overall good agreement between simulation and measurement results validates the design process.

5.4.3 Implemented DA Performance Analysis

After demonstrating the benefits this matrix-based model offers from ease and direct design process, and the reliability it provides where good agreement was obtained between simulations and measurements, focus here is placed on analyzing the performance of the fabricated 100-GHz CMOS-based DA. Both group-delay, stability and large-signal performance analysis is performed hereafter. It should be pointed out that those three design characteristics were not part of the CAutoD algorithm presented in Chapter 4 and what is demonstrated in this subsection is just an illustration of what we would obtain if we decided to go with a DA design process that focuses solely on extending and flattening passband. The same three analysis were not applied to the standalone unit-cell since from Figure 5.22(a) this device does not provide amplification and hence it has no interest for practical usage.

5.4.3.1 Group Delay Performance Analysis

Figure 5.23 shows the DA group-delay behavior besides its S_{21} phase. Inside its passband ranging from F_{lower} of 16.7 GHz to an F_{upper}100 GHz, determined previously, the group delay experiences a measured ±5 ps variation up to 80 GHz and then increases quickly as it approaches the upper side 100 GHz. This is because amplifier S_{21} phase is linear against frequency until 80 GHz and becomes non-linear as it approaches passband steep roll-off at higher frequency end.

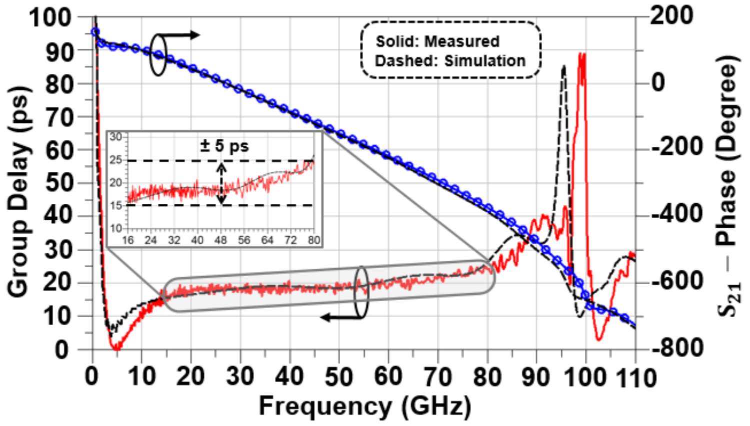


Figure 5.23: Group delay simulation and measurement results versus frequency. Simulations were performed on ADS software

5.4.3.2 Stability Performance Analysis

The DA k- and $|\Delta|$-factor derived from measurements and compared to simulation can be seen in Figure 5.24. The DA is unconditionally stable for the whole measured passband except at frequency of 100 GHz where it becomes conditionally stable with $k = 0.85$. This decline is attributed to a higher measured S_{12} reaching an utmost of -10 dB compared to -17 dB in simulation and a wider S_{21}-passband. This led to a higher $|S_{12}S_{21}|$ product which causes k-factor to degrade since $k = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2)/(2|S_{12}S_{21}|)$ [20].

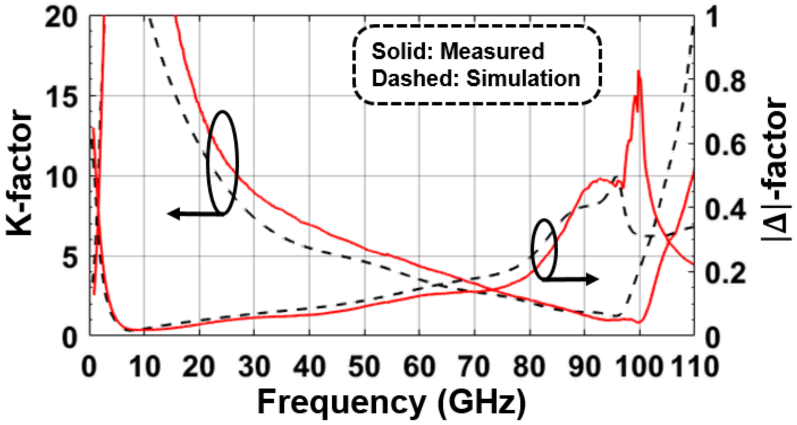


Figure 5.24: DA k- and $|\Delta|$-factor versus frequency. Simulations were performed on ADS software.

5.4.3.3 Large-Signal Performance Analysis

While the main scope of this thesis is to come up with a different and new design technique for mm-wave DAs, the large signal performance are worth mentioning to gasp the performance of the UWB amplifier device. The following analysis is presented hereafter where the power delivery capability of the former device is analyzed. Due to limitation in our measurement equipment, the provided data in Figure 5.25 and Figure 5.26 are simulation-based results.

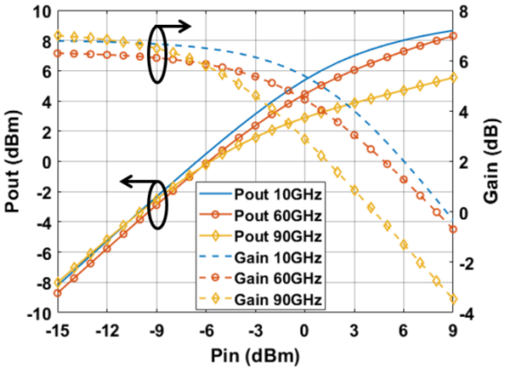


Figure 5.25: Simulated output power and gain at 10 GHz, 60 GHz and 90 GHz

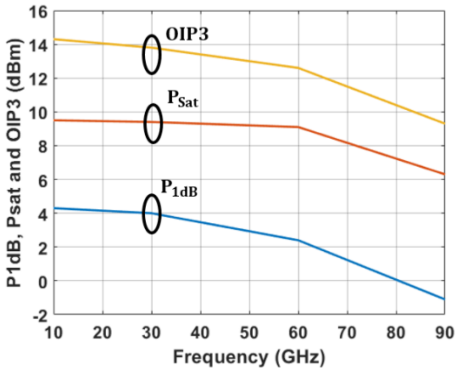


Figure 5.26: Simulated $\mathrm{P_{1dB}}$, $\mathrm{P_{sat}}$ and OIP3 as a function of frequency

Figure 5.25 shows the simulated output power and gain as a function of input power at 10 GHz, 60 GHz and 90 GHz. The maximum output power at the three frequencies is 9.5 dBm, 9.1 dBm and 6.3 dBm, respectively. At 10 GHz and 60 GHz, the gain exhibits similar behavior while at 90 GHz, the gain is compressed slightly earlier. Figure 5.26 shows the simulated OP1dB, $\mathrm{P_{sat}}$and IP3 as a function of frequency. The average $\mathrm{P_{1dB}}$, $\mathrm{P_{sat}}$ and OIP3 over the entire frequency band are 2.4 dBm, 8.6 dBm and 12.5 dBm, respectively. The maximum $\mathrm{P_{sat}}$ of 9.5 dBm and OIP3 of 14.3 dBm were achieved at frequencies below 40 GHz.

TABLE 5.6: DA SIMULATED AND MEASURED OP_{1dB} ESULTS

	Frequency (GHz)			
$\mathrm{OP_{1dB}}$	10	30	60	90
Simulation (dBm)	4.3	4	2.4	-1.1
Measurement (dBm)	4.6	3.4	2	-1.6

Table 5.6 compares the simulated $\mathrm{P_{1dB}}$ results to the ones we were able to measure at 10 GHz, 30 GHz, 60 GHz and 90 GHz. Both OIP3 and $\mathrm{P_{sat}}$ measurements were not possible to provide due to lack of coupler equipment to send two tones to perform the former measurement and the incapability of our VNA in providing more than 0 dBm for the latter

measurement. One can note that measured results are well correlated with simulation and are considered acceptable performance for such a CMOS-based small-signal distributed amplifier.

5.5 Comparison with State-of-the-Art CMOS-Based DAs Performances

In Chapter 2, state-of-the-art DA performances in different process nodes and technologies was introduced. It was concluded that indeed HBT-based DA can outperform FET-based DAs due to the HBT superiority in providing higher transconductance. Since this is commonly known and for a fair comparison, here our characterized DA is compared to only CMOS-based DAs. Table 5.7 summarizes our measured results to the other start-of-the-art silicon DAs.

TABLE 5.7: STATE-OF-THE-ART PERFORMANCE COMPARISON FOR CMOS-BASED DISTRIBUTED AMPLIFIERS

Ref.	Process Techno.	Gain (dB)	Ripple$^{£}$ (dB)	BW$^{\&}$ (GHz)	Supply (V)	P_{DC} (mW)	GBP (GHz)	$\boldsymbol{\frac{GBP}{P_{DC}}}$ $\boldsymbol{\left(\frac{GHz}{mW}\right)}$	Total Area (mm^2)	$\frac{\mathrm{GBP}}{P_{DC}\cdot \mathrm{Area}}$ $\left(\frac{\mathrm{GHz}}{\mathrm{mW}\cdot \mathrm{mm}^2}\right)$
[30]	90-nm Si CMOS	7.4	-3$^{\%}$	80	2.4*	120	188	**1.57**	0.72	2.18
[41]	90-nm Si CMOS	7$^{@}$	+9$^{\%}$,-3	70	N/A	122	157	**1.29**	0.72	1.8
[42]	90-nm digital CMOS	14$^{@}$	±1.5$^{\%}$	73.5	1.2*	84	368	**4.38**	1.72	2.54
[43]	40-nm digital CMOS	15$^{\$}$	+5$^{\%}$,-3	80	(1, 1.7)**	90	450	**5**	0.31	16.13
[44]	120-nm SOI CMOS	11	±1.2	85	2.5*	210	302	**1.44**	1.28	1.13
[45]	120-nm SOI CMOS	7.8	±1.3	82	2.6*	130	201	**1.55**	1.05	1.47
[31]	45-nm SOI CMOS	9	±1.5$^{\%}$	92	1.2*	73.5	259	**3.52**	0.45	7.82
[32]	22-nm FD-SOI CMOS	8.5	-3$^{\%}$	110	2*	80	292	**3.66**	0.38	9.63
This Work	**55-nm Si CMOS**	**6.7**	**±1.3**	**83.32**	**1.2***	**30**	**180**	**6.01**	**0.83**	**7.24**

N/A = not available.

$^{\&}$BWs are reported as declared by authors. $^{£}$Ripple limits is determined within the authors declared BW for their reported gain.

$^{\%}$Estimated from plots $^{@}$Cascaded Multi-stage DA (CMSDA) $^{\$}$Cascaded single-stage DA (CSSDA)

*Biased using external bias-tee **Biased using integrated bias-tee

This work demonstrates comparable gain while being the most power-efficient DA. As a result, this work reports the highest $\mathrm{GBP}/\mathrm{P_{DC}}$ figure of merit for single-stage CMOS DA of 6.01 GHz/mW, to the authors' knowledge. It is true that our presented DA does not provide the highest GBP between the stated CMOS DAs; for instance, [43] provides a GBP of 450 GHz. However, one can benefit from our low P_{DC} to cascade three of our DA stage until [43] $\mathrm{P_{DC}}$ of 90 mW is reached. This would lead to a higher GBP of 843 GHz and, hence, a $\mathrm{GBP}/\mathrm{P_{DC}}$ of 9.37 GHz/mW; highlighting once more, that thanks to our model and algorithmic scripted method, we were able to squeeze out the last drop of possible performance improvement from each design parameter when design the single stage DA. It is true that cascading leads to increase in total area; however, in this case, layout improvements such as pads rearrangement would have been considered. In addition, it is worth mentioning the contribution a smaller technology node (e.g. 40-nm [43] and 22-nm [32]) can bring in area reduction compared to the 55-nm adopted in this work, which could explain their higher $\mathrm{GBP}/(\mathrm{P_{DC}} \cdot \mathrm{Area})$ merit.

5.6 Conclusion

In this chapter, the $ABCD$-model was put to practice where it was used to realize a 100-GHz single-stage loss-compensated CMOS DA using ST 55-nm CMOS technology. Both the circuit design and layout implementation aspects of the design process were covered. It showed how we were able to directly determine the optimum number of unit cells and transistor size, besides other design parameters, needed to satisfy our desired FoM of high GBP/P_{DC} with reasonable gain. It demonstrated how the design process can be rendered simple and fast by using the proposed methodology and scripting, and interesting through 3D-DSE plots.

During the design process, a lack of high-quality capacitor suitable for mm-wave design was detected. As a solution, a viable passive capacitor topology is demonstrated and characterized. An accurate design equation (5.1) is also provided with at most 5% of discrepancy with the characterization performed. Measurements showed attractive performance from excellent quality factor and high SRF, making it suitable for analog systems operating until 100 GHz and possibly even up to 368 GHz, proving eligibility for both broadband and high data-rate ICs. Furthermore, it is fabricated without extra mask costs (unlike MIM capacitor) and easy to simulate in a time-efficient manner in full 3D-EM simulators if compared to MOM capacitor, since it does not involve a mesh of closely spaced thin metal wires. Finally, it is a promising topology in advanced technology nodes since higher capacitance density is expected with metal stack increment.

When comparing overall behavior of the unit-cell and DA, Figure 5.21, to both ADS-based simulation and measurements, good agreement was obtained validating therefore the accuracy of the model. In addition, when compared to the state-of-the-art CMOS DAs (Table 5.7), optimum GBP/P_{DC} performance was obtained owing to the capability of the proposed model in presenting the complete DA and taking all of its design parameters into consideration during the automated sizing. Joining the latter two criteria contributes to maximizing the performance that could possibly come from each design parameter.

Chapter 6

THz Gain-Bandwidth Product 100-GHz Cascaded CMOS Distributed Amplifier

In the last chapter, a demonstration on how we can use the proposed model to realize a single-stage DA with high GBP/P_{DC} characteristic was presented. There, both circuit design and implementation sides of the design process were covered. In addition, performance analysis and comparison with state-of-the-art CMOS-based DAs was performed where ours demonstrated better overall performance. In this chapter, the model is reused in combination with device cascading technique to demonstrate its potentiality in realizing a CMOS-based DA with the highest THz GBP characteristic possible when compared to the literature.

This chapter is structured as follows. Section 6.1 covers the circuit design part of the design process from determining the new set of required design variables ($l/2$, N, W_{CS}, TL_{Lg} and TL_{Lds}) in addition to a new design variable (M) which defines the cascading factor. Section 6.2 covers the design implementation part of the design process. Here, a new integrated inductive bias-tee [68] is presented that offers wideband characteristic. Section 6.3 discusses the simulated results of the implemented cascaded DA. A comparison with the performances of state-of-the-art DAs in different technologies and process nodes is presented in Section 6.4. Finally, Section 6.5 concludes and summarizes this chapter.

6.1 THz GBP Cascaded CMOS DA: Circuit Design

From the state-of-the-art presented in Table 2.2 (Chapter 2), and reminded in Section 6.4 of this chapter, the idea of cascading DA was introduced by [41], [42], [47], [49], as a technique to obtain higher overall gain covering the large passband where the gain of a single-stage N-unit cells DA is multiplied by the number of cascaded stages (M). In [69], an analytical-based study was provided that demonstrates a trade-off between N and M to reach a certain gain while being P_{DC}-efficient. Herein, we decide to make use from the outcome of our previously described algorithmic methodology to choose new set of adequate design-variables sizes in order to have the optimum GBP per single stage. This proposition will aid in maximizing the cascaded DA overall GBP, which in return will have advantageous influence on having a much higher overall GBP/P_{DC} merit.

The circuit design part for a 100-GHz bandwidth criterion was already covered in Chapter 5 (Section 5.2). It was determined that 35 DA options were only able to satisfy such criterion, from the whole 216 DAs design space of Figure 4.11, with their respective optimum values for N and W_{CS}.

Since our aim here is to show that maximizing GBP is possible through our model, we decided to pick the optimum design option that offers the highest gain. Referring to Figure 5.2, the DA with $N = 6$ and $W_{CS} = 28$ µm offers gain of 7.7 dB over 100 GHz of passband, higher compared to the previous option of $N = 5$ and $W_{CS} = 31$µm (7 dB). Of course, from Figure 5.3, it is visible that the former option offers relatively lower GBP/P_{DC} than the latter due to its higher P_{DC} (32.3 mW instead of 30 mW, determined from Figure 4.17). However, when cascading the DAs, the higher gain will benefit us from having a much higher overall GBP and therefore will lead to an even greater GBP/P_{DC} performance, as will be proven here shortly after.

For the chosen design option of $N = 6$ and $W_{CS} = 28$ µm, the segments length $(l/2)$ was determined to be 125 µm from Figure 4.19 and the values of its loss-compensating µ-TL-type inductors, TL_{L_g} and $TL_{L_{ds}}$, are found to be 54 µm and 155 µm from Figure 4.20(a) and Figure 4.20(b), respectively.

It should be highlighted how the re-design process was easy and determining the required design variables was immediate without any re-calculation of any kind. This would have not been the case if the previously methods mentioned in Chapter 3 (Section 3.2) were used nor would it have been the case if CAD tools that only offers schematic design environment where change of FoM is followed by re-doing the manual exchange of N from the scratch and consequently followed by a re-optimization process per exchange.

What remains is determining the number of cascaded stages (M) needed. From state-of-the-art Table 2.2, it is noticeable between cascaded DAs that the commonly adopted gain ripple is ±3 dB over the passband. For this reason, we can benefit from our 1-dB restriction imposed during our design process, as was already specified in the algorithmic design methodology (Step 5), and cascade the single-stage DA six times, i.e., set $M = 6$. This will lead to a preliminary simulated gain of 46.2 dB ±3 dB. For a 100-GHz passband, this will result in a GBP of 20.42 THz. Of course, P_{DC} will also be 6-fold higher, but when calculating the overall GBP/P_{DC} of the cascaded DA, one will obtain 105.5 GHz/mW; proving the previous statement, that cascading does indeed increase GBP/P_{DC} merit. Such value is determined to be the highest between the recorded values in the literature, based on state-of-the-art Table 2.2. Those design parameters in order to implement such cascaded DA are summarized in Table 6.1 with the design characteristics in Table 6.2.

Next Section 6.2 covers the layout implementation of the cascaded DA.

TABLE 6.1: CASCADED DA DESIGN PARAMETERS DETERMINED FROM CAUTOD PROCESS

M	N	M1 (μm)	M2 (μm)	TL Segments ($l/2$) (μm)	$\mathrm{TL_{Lg}}$ (μm)	$\mathrm{TL_{Lds}}$ (μm)
6	6	28	56	125	54	155

TABLE 6.2: CASCADED DA PRELIMINARY DESIGN CHARACTERISTICS

Gain (dB)	Bandwidth (GHz)	$\mathrm{P_{DC}}$ (mW)	Gain Ripple (dB)	GBP (THz)	$\mathrm{GBP/P_{DC}}$ (GHz/mW)
46.2	Up to 100	193.54	±3	20.42	105.5

6.2 THz GBP Cascaded CMOS DA: Circuit Implementation

This section discusses the layout implementation part of the previously chosen circuit. Since we will implement a DA circuit similar to the one implemented in Chapter 5, but just with different values for N and W_{CS}, both discussions on microstrip line topology and shunt SPP capacitor topology were already covered in Section 5.3 and are not re-written here. Only the extra difference is highlighted where the output loaded-line of the DA here is biased through a newly proposed integrated wideband bias-tee whereas the former DA of Chapter 5 was biased from the external VNA through its RF-probes.

6.2.1 Integrated Wideband Millimeter-Wave Bias-Tee [68]

In a general context, realizing wideband active ICs is accompanied with additional design efforts to produce suitable components used to synthesize them, mainly ones capable of providing wideband characteristic. For instance, in Chapter 5 an issue with having high Q-factor and SRF shunt capacitor components, suited for the mm-wave band, was detected and was resolved by proposing our own SPP topology. Another challenge encountered is when the wideband IC is required to be synthesized with its own bias tee. This requires the implementation of a compact, low power-overhead and wideband RF-choke. For the case at hands, for instance, the bias-tee has to be able to provide RF-choke capability covering frequencies reaching the highest operating frequency of the DA, i.e., 100 GHz. This is considered challenging since parasitic at high frequency become dominant and can disrupt the performance of the bias tee and, consequently, have negative influence on the behavior of the device itself.

6.2.1.1 Already Existing Techniques for Realizing Wideband Bias-Tees

There already exists traditional techniques to realize a bias-tee and they are summarized as follows. The most common technique to realize a wideband and compact biasing network is by using integrated resistive elements as RF-chokes [50]. With this approach, a series resistance is used between power-supply equipment and on-wafer device to inhibit RF signals from leaking outwards and any possible interaction between both two. This approach also benefits from allowing the lower-corner frequency of the IC to extend downwards to DC levels (0 Hz). However, this approach is not suitable when DC power efficiency is important since it causes a voltage drop across the resistor and thus V_{dd} must be increased to preserve the same operating point of the biased circuit. External bias-tees with large inductance are commonly used, such as in [31], [45] and [70], to mitigate this issue owing to their attractive low DC-resistance while providing high reactance that chokes RF signal. This technique, however, requires the use of a bulky and expensive off-chip inductor not suited for fully integrated systems. Embedding a large spiral inductor as part of the design to avoid cost penalty, such as in [71], is suited for relatively small operational bandwidths where they can be positioned below SRF [72], but this integrated solution may become problematic when dealing with several tens of gigahertz bandwidth. This is due to the parasitic elements having larger influence at high frequencies and hence affecting the behavior of the wideband bias-tee. Most often, this happens to the bias-tee SRF where the overall parasitic can alter it and subsequently alter the passband behavior of the device being designed. Shifting this SRF outside such wide passband by reducing those parasitic is considered challenging especially when the intended circuit to be biased operates up to 100 GHz.

As a solution, a compact fully integrated bias-tee with low DC-overhead and wideband performance is proposed. Compared to conventional approach where bias-tees, the ones that use inductor components as RF-choke, are designed to reduce the overall parasitic and push their SRF outside the device passband, i.e., above the highest operating frequency of the biased device, here the bias-tee is designed by taking advantage of the parasitic capacitance and pushing its SRF below the passband of the biased device.

For the sake of simplicity in demonstrating the proposed bias-tee idea, its design concept and process are first introduced followed, as a second step, by a practical example where a 100-GHz bandwidth standalone bias-tee is implemented and its simulation versus measurement is discussed.

6.2.1.2 Proposed Wideband Bias-Tee: Design Concept

Figure 6.1 illustrates the complete biasing network configuration. The left side represents the DC-power supply, the right side represents the intended RF-circuit to be biased and the middle network represents the lumped-element circuit of the proposed bias-tee. The bias-tee here is a two-port RF network, with port-1 towards DC-power supply side and port-2 towards the RF-circuit side. When compared to the practical implementation in Figure 6.6 where each single-stage DA is biased from its output-loaded line, it is noticeable that the termination resistance R and DC-decoupling capacitance C (R_3 and C_3, respectively, on Figure 6.6) are considered as part of the bias-tee.

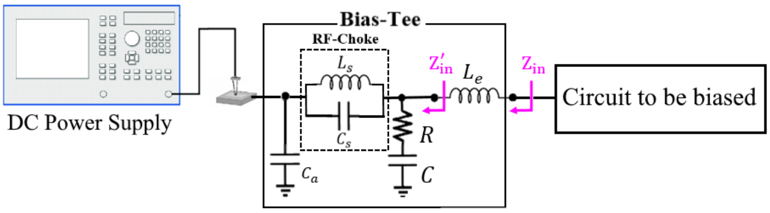


Figure 6.1: Lumped model representation of the proposed bias-tee topology

Conventionally, the bias-tee reactance-type RF-choke is designed such that its SRF is pushed above the biased circuit highest operating frequency (F_{upper}) while providing sufficiently high inductive reactance across its passband. This is usually achieved by optimizing the structure on the basis of L_S while attempting to diminish RF-choke parasitic C_S. Our proposed way, however, takes advantage of the SRF instead of suffering from it. This is done by making use of RF-choke parasitic capacitance C_S and considering it now as a design parameter while pushing bias-tee overall resonance frequency below the biased circuit lower-corner frequency (F_{lower}). For this reason, the bias-tee of the proposed approach could be viewed as having a "capacitive-reactance RF-choke", i.e. the passband of the device is operating in the capacitive region established by C_S. Referring to Figure 6.1, shunt capacitor C_a is added as a filtering capacitor to protect the integrated mm-wave circuit against any perturbation that comes from DC power supply and its wiring. In practice, off-chip capacitors are also implemented all along the DC-path and probe coming from external power supply. In addition, large on-wafer integrated capacitors are also added at pad-level to enhance protection. Those have no effect on bias-tee as long as C_a acts as a perfect AC-ground in the DA frequency range of interest. Capacitors C_a and C own parasitic are not considered herein, being negligible as compared to L_S-C_S tank elements and would be, for instance, if the SPP capacitor introduced in Chapter 5 (Section 5.3) is used. Finally, the purpose of adding L_e, a small value inductor, is to remove excess imaginary part of the bias tee input impedance seen by the device being biased. This will be better explained when discussing equation (6.5).

In a first approach, L_S and C_S are being considered as independent parallel components. Equation (6.1) demonstrates the impedance of the LC-tank. Emphasis was put intentionally here on the parasitic capacitance C_S as a design parameter, instead of L_S, as it is noticeable how capacitor C_S can be benefited from to create high impedance RF-choke. Later on, when dealing with the practical example of designing a 100-GHz bandwidth bias-tee for the DA, an empirical relationship between both is provided as an example that designers can adopt to choose adequately the RF-choke parameters.

$$Z_{tank}(\omega) = \frac{-j}{\omega C_S \left(1 - \left(\frac{\omega_{tank}}{\omega}\right)^2\right)} \tag{6.1a}$$

$$\omega_{tank} = \frac{1}{\sqrt{L_S C_S}} \tag{6.1b}$$

By ignoring L_e at first, and if C_a is chosen large enough to be safely assumed as an AC-connection to ground for the whole passband, the bias-tee equivalent input impedance is derived first from Z'_{in} in (6.2).

$$Re\{Z'_{in}(\omega)\} = R'_{in}(\omega) = R\frac{C^2}{\Delta} \tag{6.2a}$$

$$Im\{Z'_{in}(\omega)\} = X'_{in}(\omega) = -\frac{1}{\omega} \cdot \frac{C + \rho C_s + \omega^2 \rho C_s C^2 R^2}{\Delta} \tag{6.2b}$$

$$\rho = 1 - \left(\frac{\omega_{tank}}{\omega}\right)^2 \tag{6.2c}$$

$$\Delta = (C + \rho C_s)^2 + (\omega \rho C C_s R)^2 \tag{6.2d}$$

Impedance Z'_{in} is in the form of $R'_{in} \pm \mathrm{j}|X'_{in}|$. For matching purpose, $|X'_{in}|$ should be reduced as much as possible while R'_{in} be made as close as possible to the real part of the output impedance of the device being biased—in this case, to the single-stage DA. Up to this point, an additional relationship for C_S and L_S is necessary to pursue the proposed bias-tee design; it can be obtained through practical implementation considerations, as done next.

6.2.1.3 100-GHz Bandwidth Bias-Tee: Circuit Design Process

The design process of our wideband bias-tee, suitable for the DA discussed in Section 6.1, will be covered here. Beforehand, this process requires pre-knowledge of the bandwidth lower-limit of the device tackled. In our case, we will target by the end of this chapter a DA that will start amplifying from an F_{lower} of 5 GHz until an F_{upper} of 100 GHz. The RF-choke used is a microstrip spiral inductor realized using the eighth metal layer of ST 55-nm technology. It is chosen here since it is widely known to offer an equivalent parallel L_S-C_S tank at high frequency without the need to add explicitly extra lumped components. However, for this choice, C_S becomes a parameter correlated to L_S and, thereby, requires as a first step to be modeled analytically. Figure 6.2 gives the simulated f_{tank} and DC self-resistance of the spiral inductor metallic winding —this will be referred back to when discussing measurement results—, using ANSYS' HFSS, as a function of its self-inductance L_S.

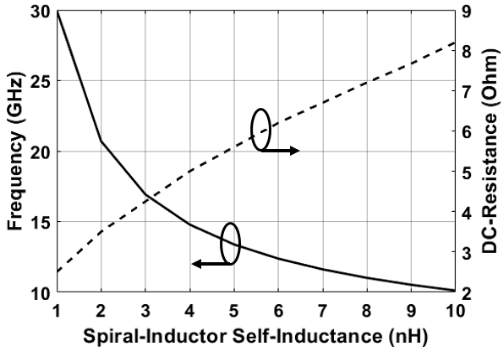


Figure 6.2: Plot of L_S-C_S tank f_{tank} frequency and its DC self-resistance against different values of self-inductance (L_S).

By curve fitting the collected f_{tank} to L_S, an empirical expression is formulated in (6.3).

$$f_{tank} = \frac{\omega_{tank}}{2\pi} = 3.778 \cdot 10^4 \cdot L_{S(H)}^{-0.6479} + 4.355 \cdot 10^9 \tag{6.3}$$

The design parameter C_S can be represented analytically as (6.4).

$$C_S = \frac{1}{((2\pi \cdot f_{tank})^2 \cdot L_S)} \tag{6.4}$$

Equation (6.3) is optional, but simplifies the design task by relating C_S to any implemented spiral design through its f_{tank}. Another possible way could be to execute multiple 3D EM simulations and extract C_S for each spiral inductor winding turns. This will result in discrete values for C_S instead of continuous ones as provided by the use of equations (6.3) and (6.4).

After having modeled the L_S-C_S tank, the bias-tee circuit design can now begin as follows. As stated previously, the proposed idea for wideband performance is to place the resonance frequency of the overall bias-tee ($f_{res_{Bias-Tee}}$) at most at the targeted F_{lower} of the device. Since we will deal with an F_{lower} of 5 GHz, both C_a and C are set to 2 pF to insure enough AC-ground while not reserving too much area when being implemented as close as possible to the DA stage. Resistance R is set to 50 Ω that represents the DA R_3 termination resistor, as already mentioned at the beginning of this subsection. By sweeping L_S from 1-nH up to 10-nH, the input reactance against frequency can thus be calculated from equation (6.2b) and for each L_S-value, $f_{res_{Bias-Tee}}$ corresponds to when $X'_{in}\left(\omega_{res_{Bias-Tee}}\right) = 0\ \Omega$. Figure 6.3 summarizes those values of $f_{res_{Bias-Tee}}$ with respect to L_S. One can observe that a minimum of 5.6 nH is needed for a resonance frequency of the bias-tee below 5 GHz. We decide to choose a slightly higher 6-nH inductance to be cautious against process variation.

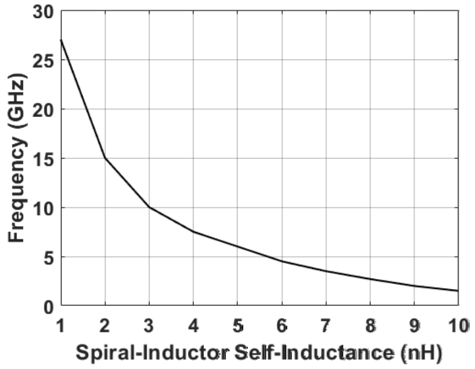


Figure 6.3: Plot of bias-tee overall resonance frequency against different values of self-inductance (L_S).

Figure 6.4 shows the bias-tee X'_{in} variation with respect to frequency. Above 5 GHz, X'_{in} is acting as a negative reactance for $L_S \geq 5.6$ nH proving, therefore, when used with the DA later on, that its passband will experience an equivalent capacitive behavior with small magnitude. In order to obtain wideband low input reactance up to the intended F_{upper}, for better port matching purposes, and since the negative part of the reactance is quite small, it can be compensated at higher frequencies by simply adding a low-value inductor, L_e. By doing so, one arrives at the complete bias-tee of Figure 6.1, providing an input impedance Z_{in}, described by equation (6.5).

$$Z_{in} = Z'_{in} + j\omega L_e = R'_{in} \approx R \tag{6.5}$$

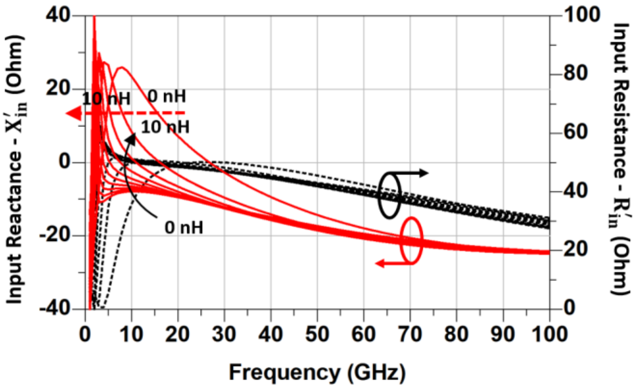


Figure 6.4: Bias-tee equivalent input reactance (X'_{in}) versus frequency for different values of L_S.

The effective input resistance R'_{in} is observed to decrease against frequency as a consequence of using C_S, as indicated by (6.2a) and (6.2d). A deducible solution would be to increase R so that the average of R_{in} becomes 50 Ω. However, based on the refine hand-tuning performed at the end of the design process with the previous single-stage DA implemented in Chapter 5, the resistor R was left here untouched until the end process before sending the cascaded DA to fabrication. Table 6.3 summarizes the required design parameter determined previously and needed to implement such bias-tee suitable to cover the passband of a DA amplifying from 5-GHz up to 100 GHz. In the next part of this subsection, simulation and measurements of the implemented bias-tee as a standalone device are presented.

TABLE 6.3: 100-GHZ BANDWIDTH INDUCTIVE BIAS-TEE DESIGN PARAMETERS

L_S (nH)	**C_S (fF)**	**C_a (pF)**	**C (pF)**	**L_e (pH)**
6	27.6	2	2	39

6.2.1.4 100-GHz Bandwidth Bias-Tee: Simulation vs Measurement Results

Figure 6.5 illustrates a 3D view of the implemented bias-tee that represents the electrical model of Figure 6.1. The L_S-C_S tank with L_S of 6 nH and C_S of 27.6 fF was implemented as a microstrip spiral inductor covering a surface area of 82 µm x 82 µm with the minimum spacing allowed by the DRM of 0.6 µm between metallic windings to conserve area. The 39-pH inductor L_e is implemented using µ-TL of 50-µm in length. Both 2-pF shunt capacitors, C_a and C, where implemented using SPP-topology introduced in Chapter 5 [61] since this high-quality capacitor topology demonstrated to be the most suitable for such applications at mm-wave band

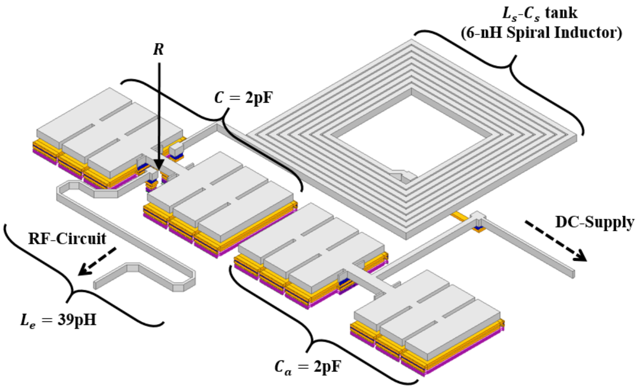


Figure 6.5: 3D isometric view of the implemented 100-GHz bandwidth bias-tee.

Figure 6.6 compares the simulated and de-embedded measured results. The simulation was performed on ANSYS 3D EM simulator HFSS. The discrepancy at frequencies below 6 GHz is attributed to the lower limit of TRL defined by the 630-µm line (Figure 5.8). A slight shift exits at lower frequencies, which could be caused by a slightly higher inductance than the anticipated L_S of 6 nH. In overall, great agreement is obtained between both results validating the design process and concept. The proposed bias-tee is capable of delivering an RF-choke bandwidth of around 100 GHz since isolation between DC- and RF- port is ≤ -20 dB up to 100 GHz (the intended F_{upper} of the DA). As additional note, referring back to Figure 6.2, the price of such a bias-tee is a small DC resistance of about 6.3 Ω. It is considered an attractive property for such a wideband performance since it will lead to a smaller DC-power overhead compared to using a resistor-based bias-tee, for instance, that provides similar wideband performance but for a much higher DC-power overhead.

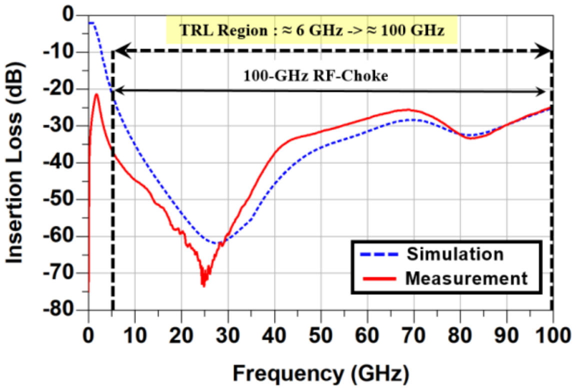


Figure 6.6: Bias-tee simulated and measured isolation (S_{21}) versus frequency between DC- and RF- ports.

Up to now, the new bias-tee topology was discussed and its design concept was validated through measuring a 100-GHz standalone device version of it. In the next subsection, the layout implementation of single stage DA, of Section 6.1, with such bias-tee is presented.

6.2.2 100-GHz Single-Stage DA: Layout and Microphotograph

All the needed components to implement the six unit-cells single-stage DA piece of the complete cascaded DA are now available. Figure 6.7 presents the final electrical schematic diagram of our loss-compensated single-stage 6-unit cells CMOS-based DA of 7.7-dB amplification and Figure 6.8 its microphotograph. Table 6.4 summarizes all of its design parameters. All TL are implemented using thickest metal available in technology, M8, with same width of 1 µm, as explained in Chapter 5, subsection 5.3.1. The µ-TL segments are done with length $l/2$ of 125 µm. Both TL_{Lg} and TL_{Lds} are implemented with length of 54 µm and 155 µm, respectively. Both termination impedances Z_3 and Z_4 are realized as series RC loads. Both R_3 and R_4 are implemented using technology component as N+ silicided polysilicon resistors, and were AC-grounded through a 2-pF bypass SPP capacitor (both C_3 and C_4) which will lead to a DA passband starting from 5 GHz while being compact in area.

TABLE 6.4: SINGLE-STAGE DA CIRCUIT DESIGN PARAMETERS FOR LAYOUT IMPLEMENTATION

N	M1 (µm)	M2 (µm)	TL Segments ($l/2$) (µm)	$\mathrm{TL_{Lg}}$ (µm)	$\mathrm{TL_{Lds}}$ (µm)
6	28	56	125	54	155

Supply voltage for the drain pin of each M2 FET is provided through the newly proposed integrated bias-tee topology (Figure 6.5) connected to the output loaded-line of the single-stage DA. The biasing of all gate pins is provided through resistive RF-choke implemented using high-resistivity polysilicon resistor (R_g) of 10-kΩ. This is possible since we are dealing with FET and hence there is no impact on overall P_{DC}. A 600-fF decoupling SPP capacitor (C_g) was added on each L_g terminal pin facing the DC pads for AC-grounding.

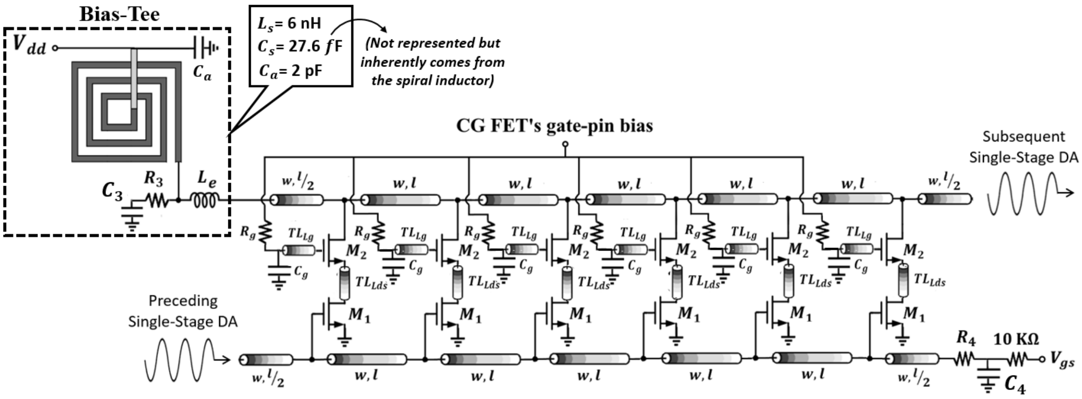


Figure 6.7: Circuit schematic of the 6 unit-cells 100-GHz CMOS-based DA with integrated bias-tee.

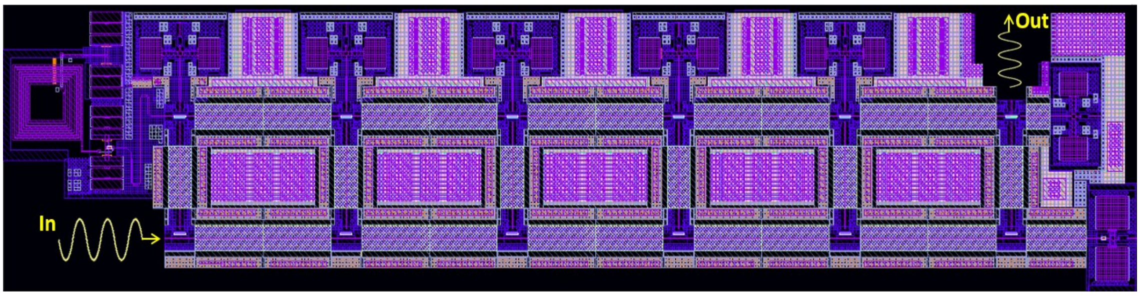


Figure 6.8: Layout view of the implemented 6 unit-cells 100-GHz CMOS-based DA with integrated bias-tee.

6.2.3 Six-Stage Cascaded 100-GHz DA Layout and Microphotograph

The final design step remaining is to realize the cascaded DA. In order to obtain 46.2 dB of gain, the single-stage DA of Figure 6.8 is cascaded six times ($M = 6$). Figure 6.9 demonstrates the final layout of the implemented cascaded DA.

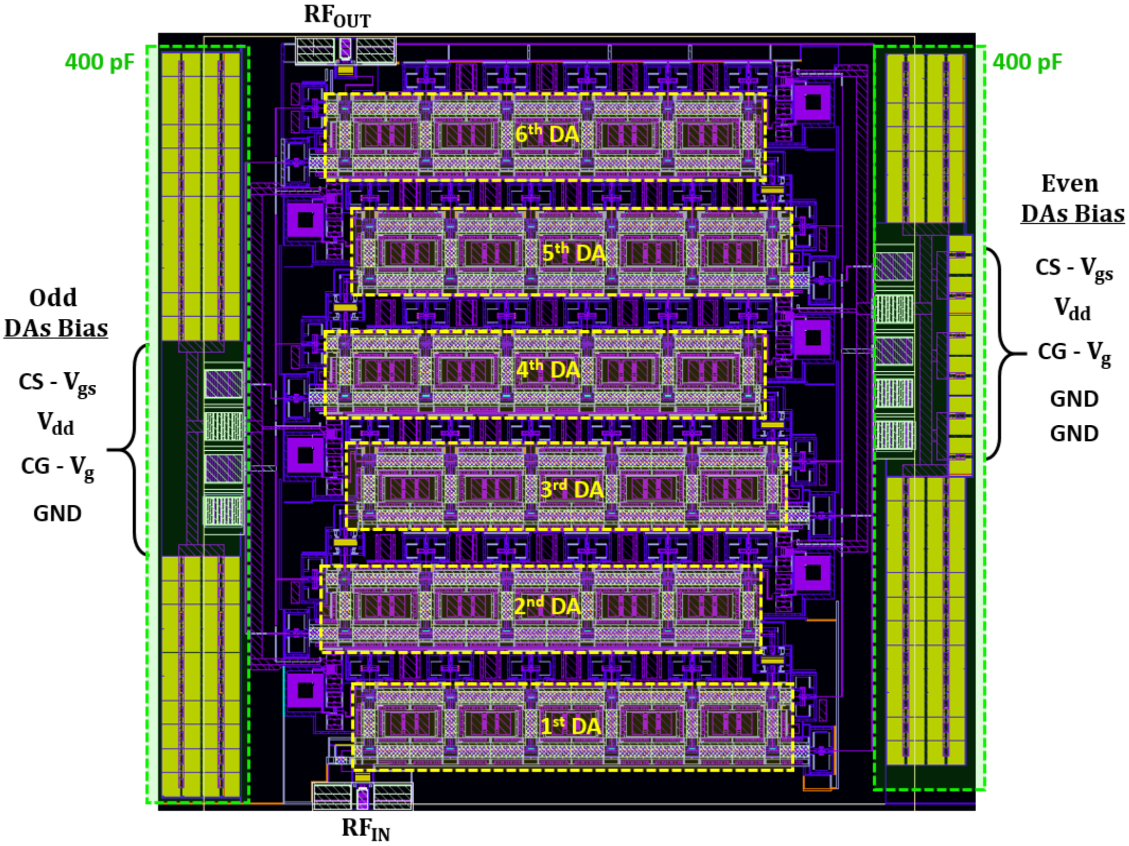


Figure 6.9: Layout view of the implemented 6-stage cascaded 100-GHz CMOS-based DA.

The core area of the DA is 2.3 mm^2 and the total area is 3.5 mm^2 including pads. To prevent biasing interference between consecutive DAs where the drain-line of a preceding DA is connected to the gate-line of the subsequent DA, a 2-pF MOM capacitor was added in series as a DC-decoupling capacitor. Series DC-decoupling capacitors were also added at both the input and output sides of the cascaded DA to prevent any influence from VNA RF-probes on the biasing point of both first and sixth single-stage DAs, respectively. Due to high gain delivered by the integrated amplifier, any influence from the outside word —in this case external biasing equipment— can interfere with the behavior of the DA and could render it unstable. For that reason, 400-pF AC-grounded capacitor was added on each side of the DA on DC-pad that provides V_{dd} to filter any incoming low-frequency noise. Woven-structure MOM capacitors, already available in the PDK, were used for both roles (DC-decoupling and AC-grounding on DC-pads) due to its capability in providing high capacitance density per unit area, hence considered advantageous for not wasting additional silicon area. Finally, GSG-type pads with 50-µm pitch are connected to the cascaded DA input and output RF-ports. After finishing the design layout implementation and before sending to fabrication, one last simulation (as a validation step) was performed on ADS schematic to make sure that everything is in order. Termination resistor R_3 was hand-tuned to 57 Ω while taking into consideration the resistive drop caused by the implemented bias-tee (Figure 6.4) and fixing any slight imperfection in midband gain-drop to preserve precisely the 3-dB limit. Concerning resistor R_4, it was left at 53.5 Ω since this part is similar to the one used in the implementation of single-stage DA of Chapter 5 without a bias-tee.

In the next Section 6.3, the performance analysis of the presented cascaded CMOS-based DA is discussed.

6.3 THz GBP Cascaded CMOS DA: Simulation Results

In this section, simulation results of the amplifier device are presented. Measurements were not possible to provide at that time due to silicon wafer still being in the fabrication stage. The S-parameter analysis of the cascaded DA are first discussed. Then, performance analysis is performed from stability and group delay analysis. Regarding power capability analysis from $\mathrm{P_{1dB}}$, $\mathrm{P_{sat}}$ and IP3, they are not possible to simulate due to insufficient processing resources when performing large-signal harmonic balance simulation on ADS of such a DA with great deal of non-linear components. A comparison with state-of-the-art DAs is performed in the next Section 6.4.

6.3.1 S-parameter Analysis

Figure 6.10 illustrates the simulated S-parameter results versus frequency for the cascaded DA. While the design process was performed using the simulation capability of our $ABCD$-model on MATLAB, however, the final simulation of the complete cascaded DA device is performed on ADS software. This is due to some design blocks, such as bias-tee, being added as touchstone files (.s2p) whereas our DA model does not possess such functionality.

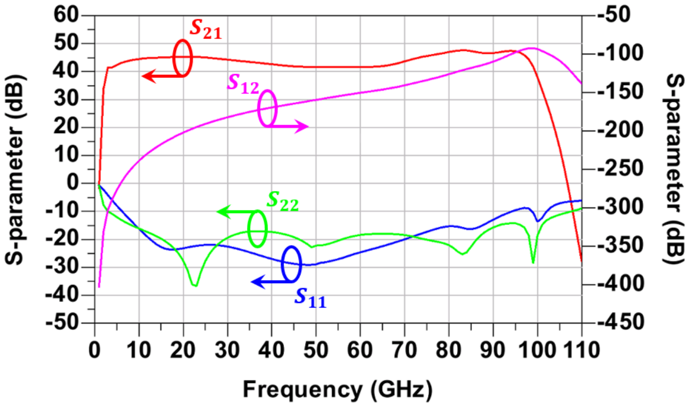


Figure 6.10: S-parameter simulation results versus frequency of cascaded DA.

Biased at V_{dd} =1.5 V instead of 1.2 V, to compensate for the bias-tee self-resistance, each single-stage DA consumes 27 mA and the overall cascaded DA consumes a total of 162 mA. This results in a P_{DC} of 40.5 mW and 243 mW, respectively. The DA achieves an average insertion gain S_{21} of 45.3 dB with in-band ripple of ±3 dB and, hence, a coverage range from F_{lower} of 5 GHz up to an F_{upper} of 100 GHz. This gives an amplified passband BW of 95 GHz and leads to a GBP of 17.5 THz. Due to bias-tee power overhead and the

DA starting from 5 GHz instead of DC-level, the new GBP/P_{DC} merit is found to be 71.96 GHz/mW. Both input and output matching levels, S_{11} and S_{22}, respectively, are better than -10 dB starting from 5 GHz up to 100 GHz. The reverse isolation S_{12} reaches a maximum of -93 dB at 100 GHz. This high isolation can be explained from using cascode topology as Gm-cell for the unit cells and since we are cascading single-stage DAs M-times, the overall reverse isolation is also multiplied by the number of cascaded stages the same way as the overall gain is.

6.3.2 Group Delay Performance Analysis

Figure 6.11 shows the DA group-delay behavior besides its S_{21} phase. The group delay experiences a flat variation inside passband up to 70 GHz and then increases quickly as it approaches F_{upper} of 100 GHz (the cut-off frequency of the DA where sharp roll-off occurs). This is because amplifier S_{21} phase is linear against frequency until 70 GHz and becomes non-linear as it approaches passband steep roll-off at higher frequency end.

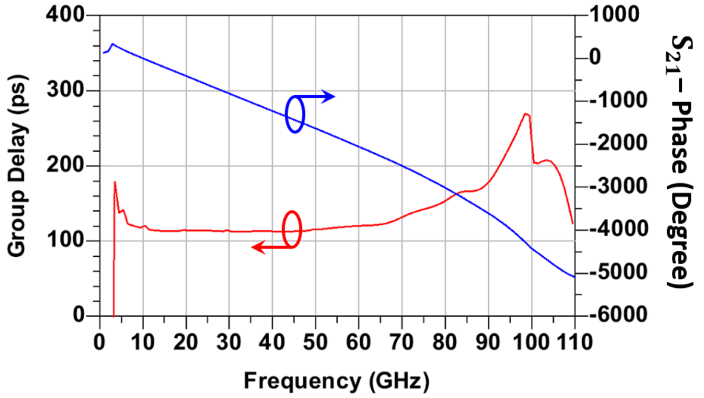


Figure 6.11: S-parameter simulation results versus frequency of cascaded DA.

6.3.3 Stability Performance Analysis

The cascaded DA k- and $|\Delta|$-factor derived from simulation can be seen in Figure 6.12.

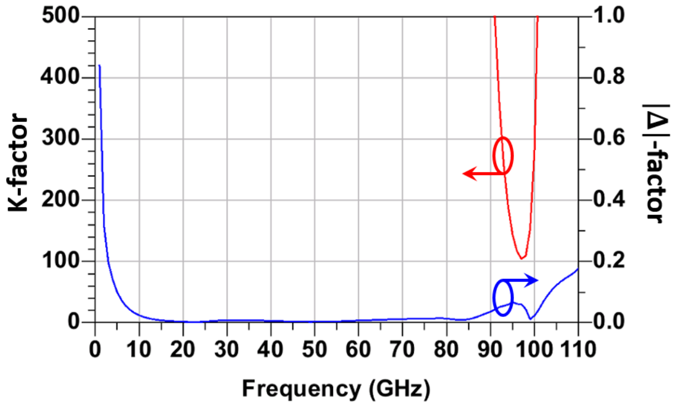


Figure 6.12: DA k- and $|\Delta|$-factor versus frequency. Simulations were performed on ADS software.

It is unconditionally stable for the whole passband. This DA demonstrates k-values ≥ 100 and $|\Delta|$-values ≤ 0.1. This high stability is attributed to the device S_{12} being interestingly very low, as illustrated in Figure 6.10, compared to single-stage DA of Chapter 5 (Figure 5.21(a)). The decline of both k- and $|\Delta|$-factors as frequency increases is due to the same reason of S_{12} increasing until -93 dB at 100 GHz.

6.4 Comparison with State-of-the-Art DAs Performances

In Chapter 2, a comparison between state-of-the-art DA performances in different process nodes and technologies was introduced. In order to highlight that it is possible using CMOS technologies to obtain high gains with UWB performances reaching frequencies as high as 100 GHz, since the former is usually considered as a weak technology due to its low transconductance, the characterized cascaded DA is mentioned with all the different DAs of Table 2.2. This performance comparison is summarized in Table 6.5 (next page).

It is observed that for a comparable bandwidth, our DA demonstrated to offer the highest gain recorded while being power efficient, hence possessing the highest GBP/P_{DC} between the stated DAs. In addition, even though our cascaded DA reserves a relatively higher total area of 3.5 mm^2; however, a comparison between all $GBP/(P_{DC} \cdot Area)$ values shows that our DA contributed to the highest one. This indicates an efficient usage of per silicon area to deliver the stated 45.3 dB of gain and re-validates once more the ability our model can give us in squeezing the most from each deign component the DA is made from to maximize the latter gain performance.

Through this performance comparison, we can conclude that while it is true what is said that CMOS technology do provide low transconductance compared to the other mentioned process technologies; however, with adequate and proper choice of optimum design parameters provided thanks to our model, CMOS technologies can be aided even more in proving their abilities in mm-wave circuit design applications.

TABLE 6.5: STATE-OF-THE-ART PERFORMANCES COMPARISON FOR DISTRIBUTED AMPLIFIERS

Ref.	Process Techno.	Gain (dB)	Ripple$^{£}$ (dB)	BW$^{\&}$ (GHz)	Supply (V)	P_{DC} (mW)	GBP (GHz)	$\frac{\boldsymbol{GBP}}{\boldsymbol{P_{DC}}}\left(\frac{\boldsymbol{GHz}}{\boldsymbol{mW}}\right)$	Total Area (mm2)	$\frac{\text{GBP}}{\text{P}_{\text{DC}} \cdot \text{Area}}\left(\frac{\text{GHz}}{\text{mW} \cdot \text{mm}^2}\right)$
[30]	90-nm Si CMOS	7.4	-3$^{\%}$	80	2.4*	120	188	1.57	0.72	2.18
[41]	90-nm Si CMOS	7$^{@}$	+9$^{\%}$,-3	70	N/A	122	157	1.29	0.72	1.8
[42]	90-nm digital CMOS	14$^{@}$	±1.5$^{\%}$	73.5	1.2*	84	368	4.38	1.72	2.54
[43]	40-nm digital CMOS	15$^{\$}$	+5$^{\%}$,-3	80	(1, 1.7)**	90	450	5	0.31	16.13
[44]	120-nm SOI CMOS	11	±1.2	85	2.5*	210	302	1.44	1.28	1.13
[45]	120-nm SOI CMOS	7.8	±1.3	82	2.6*	130	201	1.55	1.05	1.47
[31]	45-nm SOI CMOS	9	±1.5$^{\%}$	92	1.2*	73.5	259	3.52	0.45	7.82
[32]	22-nm FD-SOI CMOS	8.5	-3$^{\%}$	110	2*	80	292	3.66	0.38	9.63
[46]	130-nm InP HEMT	14.5$^{\#}$	±0.7	94	3*	N/A	499	N/A	2.75	N/A
[33]	100-nm InP HEMT	7	+2.5$^{\%}$	111	N/A	N/A	248	N/A	2.2	N/A
[47]	70-nm InP HEMT	21$^{@}$	±3$^{\%}$	80	2**	300	898	3	2.47	1.21
[34]	50-nm InGaAs mHEMT	11	±1	105	6*	450	373	0.83	1.69	0.5
[48]	250-nm InP HBT	12.8	+7$^{\%}$,-2$^{\%}$	180	N/A	110	724	6.58	0.32	20.57
[36]	250-nm InP HBT	10	-3	182	4*	105	575	5.47	0.33	16.57
[35]	130-nm SiGe HBT	10	±2$^{\%}$	170	3.6*	108	537	5	0.38	13.16
[49]	130-nm SiGe HBT	24$^{@}$	+2.5$^{\%}$,-1$^{\%}$	95	N/A	247	1506	6.09	0.65	9.37
This Work$^{\$}$	**55-nm Si CMOS**	**45.3**	**±3**	**95**	**1.5****	**243**	**17487**	**71.96**	**3.5**	**20.56**

N/A = not available.

$^{\&}$BWs are reported as declared by authors. $^{£}$Ripple limits is determined within the authors declared BW for their reported gain

$^{\%}$Estimated from plots $^{@}$Cascaded Multi-stage DA (CMSDA) $^{\$}$Cascaded single-stage DA (CSSDA) $^{\#}$Flip-Chip DA

$^{\$}$Simulated performances

*Biased using external bias-tee **Biased using integrated bias-tee

6.5 Conclusion

Through this chapter, a 45.3-dB cascaded DA using ST 55-nm CMOS technology was introduced. Results demonstrated the highest GBP and GBP/P_{DC} characteristics of 17.5 THz and 71.96 GHz/mW, respectively. The highest recorded FoMs in the literatures. Owing to the proposed $ABCD$-matrix based model and through the provided design methodology in Chapter 4, the optimum design parameters were able to be determined in order to provide the highest gain per DA-stage possible while being power efficient.

Throughout this chapter, a bias-tee topology with UWB performance was also introduced where it is based on a newly proposed technique for pushing the resonance below the lower-end of the wide passband compared to the traditional way of pushing it towards the higher-end of the wide passband. The latter becomes quite difficult especially if we are speaking about futuristic BWs ≥ 100GHz. Our proposed bias-tee showed to be efficient in power-consumption where it demonstrated lower power-overhead compared to resistive-based bias-tee and simpler in designing compared to the conventional inductive-based bias-tee since parasitic capacitance was part of the design instead of a component suffering from it. As a proof-of-concept, the proposed topology was designed for the intended DA and was characterized as a standalone device, which showed its capability in providing RF-choke functionality reaching 100 GHz of bandwidth.

Chapter 7

General Conclusion

In this thesis, we contributed in improving the design process of mm-wave distributed amplifier in integrated circuits. We did so by focusing on various aspects of its design requirements as follows. 1) Proposing a reliable and versatile design model that represents the distributed amplifier complete frequency behavior, offering the possibility for scripting-based design technique. 2) Providing an algorithmic methodology that can be used in the framework of automated designing to explore the wide space of possible distributed amplifier solutions a given process technology can offer. In addition, 3) proposing integrated passive components specifically designed to address the issue of wideband AC-grounding and device biasing. Our efforts have been validated by using STMicroelectronics 55-nm process as a technology to explore from and discover the feasible CMOS DAs and, by the end, arrive at implementing a single-stage and cascaded CMOS DA options that amplify frequencies up to 100 GHz and demonstrate global optimum performances.

First, different DA design techniques were investigated from mathematical-based approaches, to artificial intelligence-based techniques such as neural-network and through schematic-level design environments using CAD tools; however, each technique presented its own weakness. It ranged from the assumption of a continuous loaded-lines structure, which restricts the highest frequency of operation where the model can still be considered valid. The assumption of a simple unilateral Gm-cell AC equivalent circuit, where in reality a more complex representation is needed when dealing with high frequencies since parasitic become dominant. In addition, when speaking especially of mm-wave frequency bands, loss-compensated Gm-cells become necessary to be adopted in order to mitigate the parasitic losses and provide amplification at those bands, but they introduce extra design variables. This complicates the circuit design process where more variables, besides the one of the DA, needs to be taken into consideration. Depending on the Gm-cell topology chosen by the designer, those variables can change between one DA to another which highlights, therefore, the need for a general DA model. The most preferred design technique is often determined to be through CAD environments, such as Keysight ADS or Virtuoso Cadence software. For CAD environments where only schematics diagram simulation is provided, the DA is drawn first and as a second step, optimization is applied until a specific performance goal is achieved. This technique lacks the capability to optimize the number of unit-cells (N) which falls on the designer task to manually do it and, consequently, perform re-optimization per N changement. Since the DA structure has several degrees of freedom, a large volume of simulation work is necessary for a specific topology and goal, hence affecting the simplicity of such design process. For CAD environments where scripting capabilities are provided, this optimization process can be made easier through automation, however, of course, whatever the scripting language used, this requires first having at hand a proper physical model. On those basis, a matrix-based design model based on $ABCD$ parameters, famously used in describing passive circuitry, was introduced that does not employ restrictions on any kind of design parameter, that considers a complete and general Gm-cell representation, and that offers the possibility to consider all design parameters as possible tunable variables, including N. Efforts were dedicated on providing a model for successful implementation of CAutoD process for DAs through scripting.

Secondly and as a practical example, the basic principle-of-operation of a loss-compensated DA was presented as a topology that can aid in the possibility to extend the amplification passband response deep into the mm-wave frequency range. Based on its concept, a systematic algorithmic methodology, with the help of the $ABCD$-based model, was offered that maximizes passband for any combination of unit cells and transistor size. As a result, its outcome was 3D DSE plots that offer the designer an interesting graphical overview of the possible tradeoffs between all the design characteristics of interest (in this case gain, bandwidth and $\mathrm{P_{DC}}$). Our CAutoD method also provided the optimal and accurate dimensions needed for design parameters set such as transistor width, N, TL segments length, and, in this particular case of loss-compensated cascode, the inductive-type elements L_g and L_{ds}, to synthesize the suitable design option.

Finally, two CMOS-based DAs using ST 55-nm process were designed and implemented for on-wafer characterization. The first amplifier was a single-stage 100-GHz bandwidth DA that demonstrated high GBP/P_{DC} that served for model validation purposes. The second amplifier was a cascaded 100-GHz bandwidth DA that demonstrated 17.5 THz GBP and 71.96 GHz/mW GBP/P_{DC} merits, the highest recorded characteristics compared to the state-of-the-art literature. During the design process, two new design components were introduced that can contribute in synthesizing high quality and broadband mm-wave ICs. The first component was an AC-ground capacitor that offers the highest SRF- and Q-merit while providing large capacitance values at high frequency range. For instance, for a 300-fF capacitance, an SRF of 368 GHz and Q-value of 14.7 at 100 GHz were obtained. The second component being a new bias-tee topology based on the idea of benefiting from the parasitic and pushing below its SRF below the lower-end operating frequency of the DA. The latter demonstrated promising wideband performance reaching 100 GHz.

Through our work, we prevision that by the usage of our model and method we could assist analog designers in their future design process where it facilitates the alternation between layout- and design- stages where more focus can be dedicated on layout and the challenges it brings to mm-wave circuitry, and proposing enhanced components, as was done here. In addition, to give the opportunity to discover the optimality a given technology node can yield, and explore and suggest enhancements that can break the limits and further advance the performance of future mm-wave distributed amplifiers.

Publications

<u>Journals:</u>

[**Published**] M. El-Chaar, L.Vincent, J. -D. Arnould, A. A. L. de Souza, S. Bourdel and F. Podevin, "Accurate Design Method for Millimeter Wave Distributed Amplifier based on Four-Port Chain (ABCD) Matrix Model," in *IEEE Transactions on Circuits and Systems I: Regular Pape*rs, vol. 69, no. 11, pp. 4510-4523, Nov. 2022.

[**Published**] M. El-Chaar, F. Podevin, S. Bourdel, A. A. L. de Souza and J. -D. Arnould, "Integrated Stacked Parallel Plate Shunt Capacitor for Millimeter-Wave Systems in Low-Cost Highly Integrated CMOS Technologies," in *IEEE Solid-State Circuits Letters*, vol. 5, pp. 114-117, 2022.

<u>Conferences with acts:</u>

M. EL Chaar, A. L. de Souza, M. Barragan, F. Podevin and S. Bourdel, "A Non-Closed-Form Mathematical Model for Uniform and Non-Uniform Distributed Amplifiers," *2020 IEEE MTT-S International Conference on Microwaves for Intelligent Mobility (ICMIM)*, 2020, pp. 1-4,

M. E. Chaar, A. L. de Souza, M. Barragan, F. Podevin, S. Bourdel and J. -D. Arnould, "Integrated Wideband Millimeter-Wave Bias-Tee – Application to Distributed Amplifier Biasing," *2021 19th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2021, pp. 1-4,

I. Alaji, T. C. Mouvand, M. El-Chaar, A. Lisboa-de-Souza, F. Podevin and S. Bourdel, "Cascaded tunable distributed amplifiers for serial optical links: Some design rules," *2020 18th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2020, pp. 234-237,

M. El-Chaar, F. Podevin, S. Bourdel, A. Lisboa-de-Souza, J.-D. Arnould "Méthode de conception d'amplificateurs distribués millimétriques basée sur la matrice chaîne (ABCD) 4 ports ", », *22èmes Journées Nationales Microondes*, Limoges, 7-10 juin 2022.

<u>Seminar, worshops:</u>

M. El-Chaar, A. de Souza, F. Podevin, S. Bourdel, J.-D. and M. Barragan, "Distributed Amplifier: Application to future means of communication in the field of millimeter-wave frequencies", *Journée Scientifique du Pole PEM*, Grenoble, France, 21 octobre 2021.

Bibliography

[1] D. Alldred, B. Cousins, and S. P. Voinigescu, “A 1.2 V, 60 GHz radio receiver with on-chip transformers and inductors in 90 nm CMOS,” in Proc. IEEE Compound Semiconductor Integrated Circuits Symp., Nov. 2006, pp. 51–54.

[2] B. Razavi, "A 60GHz direct-conversion CMOS receiver," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005., 2005, pp. 400-606 Vol. 1

[3] Razavi, "A 60-GHz CMOS receiver front-end," in *IEEE Journal of Solid-State Circuits*, vol. 41, no. 1, pp. 17-22, Jan. 2006,

[4] Q. Gordon, T. Yao and S. P. Voinigescu, "65-GHz receiver in SiGe BiCMOS using monolithic inductors and transformers," *Digest of Papers. 2006 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2006, pp. 4 pp.-,

[5] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema and B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 156-167, Jan. 2005,

[6] C. H. Wang, Y. H. Cho, C. S. Lin, H. Wang, C. H. Chen, D. C. Niu, J. Yeh, C. Y. Lee, and J. Chern, “A 60 GHz transmitter with integrated antenna in 0.18 m SiGe BiCMOS technology,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 186–187.

[7] B. Floyd, S. Reynolds, U. Pfeiffer, T. Beukema, J. Grzyb, and C. Haymes, “A silicon 60 GHz receiver and transmitter chipset for broadband communications,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 649–658.

[8] S. Gunnarsson, C. Karnfelt, H. Zirath, R. Kozhuharov, D. Kuylenstierna, A. Alping, and C. Fager, “Highly integrated 60 GHz transmitter and receiver MMICs in a GaAs pHEMT technology,” in *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2174–2186, Nov. 2005.

[9] M. Siddiqui et al., “GaAs components for 60 GHz wireless communication applications,” presented at the GaAs Mantech Conf., San Diego,CA, Apr. 2002.

[10] H. Zirath, T. Masuda, R. Kozhuharov, and M. Ferndahl, “Development of 60 GHz front-end circuits for a high-data-rate communication system,” IEEE J. Solid-State Circuits, vol. 39, no. 10, pp. 1640–1649, Oct. 2004.

[11] O. Memioglu, Y. Zhao and B. Razavi, "A 300GHz 52mW CMOS Receiver with On-Chip LO Generation," *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, 2022, pp. 1-3,

[12] S. Hara *et al.*, "A 416-mW 32-Gb/s 300-GHz CMOS receiver," *2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 2017, pp. 65-67.

[13] K. Takano et al., "17.9 A 105Gb/s 300GHz CMOS transmitter," 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2017, pp. 308-309.

[14] J. Hacker et al., "THz MMICs based on InP HBT Technology," 2010 IEEE MTT-S International Microwave Symposium, 2010, pp. 1126-1129.

[15] J. Rieh, B. Jagannathan, H. Chen, K. T. Schonenberg, D. Angell, A. Chinthakindi, J. Florkey, F. Golan, D. Greenberg, S.-J Jeng, M. Khater, F. Pagette, C. Schnabel, P. Smith, A. Stricker, K. Vaed, R. Volant, D. Ahlgren, “SiGe HBTs with cut-off frequency of 350 GHz”, Digest of 2002 International Electron Devices Meeting (IEDM '02), pp. 771-774, 2002

[16] International Technology Roadmap for Semiconductors, 2007, see http://public.itrs.net/

[17] Cisco, “Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2017-2022” Cisco Visual Netw. Index, San Jose, CA, USA, White Paper, Feb. 2019.

[18] National Telecommunications and Informatio Administration, "United States Frequency Allocations: The Radio Spectrum Chart" United States Department of Commerce, Jan. 2016.

[19] Richard N. Clarke, Expanding mobile wireless capacity: The challenges presented by technology and economics, Telecommunications Policy, Volume 38, Issues 8–9, 2014, Pages 693-708.

[20] P. Liu, K. Skucha, M. Megens, and B. Boser, “A CMOS Hall-effect sensor for the characterization and detection of magnetic nanoparticles for biomedical applications,” *IEEE Trans. Magn.*, vol. 47, no. 10, pp. 3449–3451, 2011.

[21] B. Jang, P. Cao, A. Chevalier, A. Ellington, and A. Hassibi, “A CMOS fluorescent-based biosensor microarray,” in IEEE ISSCC Dig. Tech. Papers, 2009, pp. 436–437.

[22] D. Di Carlo, L. Y. Wu, and L. P. Lee, “Dynamic single cell culture array,” Lab Chip, vol. 6, pp. 1445–1449, 2006.

[23] Gustav Veith, Eugen Lach, Karsten Schuh, 100 Gigabit-per-second: Ultra-high transmission bitrate for next generation optical transport networks, Comptes Rendus Physique, Volume 9, Issues 9–10, 2008, Pages 1002-1011, ISSN 1631-0705.

[24] Chun-Lin Ko, Chieh-Pin Chang, Chien-Nan Kuo, Da-Chiang Chang and Ying-Zong Juang, "A 1-V 60 GHz CMOS low noise amplifier with low loss microstrip lines," Proceedings of Technical Program of 2012 VLSI Design, Automation and Test, 2012, pp. 1-4.

[25] Y. Park, C. . -H. Lee, J. D. Cressler, J. Laskar and A. Joseph, "A very low power SiGe LNA for UWB application*,"* IEEE MTT-S International Microwave Symposium Digest, 2005*.,* 2005, pp. 1041-1044.

[26] Sananes, R.; Socher, E.: '52–75 GHz wideband low-noise amplifier in 90 nm CMOS technology', Electronics Letters, 2012, 48, (2), p. 71-72,

[27] W. R. Deal, M. Biedenbender, P. Liu, J. Uyeda, M. Siddiqui and R. Lai, "Design and Analysis of Broadband Dual-Gate Balanced Low-Noise Amplifiers," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2107-2115, Oct. 2007

[28] A. Arbabian *et al*., "A 90GHz-carrier 30GHz-bandwidth hybrid switching transmitter with integrated antenna," *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 2010, pp. 420-421

[29] O. El-Aassar and G. M. Rebeiz, "A Compact pMOS Stacked-SOI Distributed Power Amplifier With Over 100-GHz Bandwidth and Up to 22-dBm Saturated Output Power," in *IEEE Solid-State Circuits Letters*, vol. 2, no. 2, pp. 9-12, Feb. 2019.

[30] Ren-Chieh Liu, To-Po Wang, Liang-Hung Lu, Huei Wang, Sung-Hsiung Wang and Chih-Ping Chao, "An 80GHz travelling-wave amplifier in a 90nm CMOS technology," *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005*, San Francisco, CA, USA, 2005, pp. 154-590 Vol. 1.

[31] J. Kim and J. F. Buckwalter, "A 92 GHz Bandwidth Distributed Amplifier in a 45 nm SOI CMOS Technology," in *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 6, pp. 329-331, June 2011.

[32] P. V. Testa, D. Fritsche, S. Schumann, W. Finger, C. Carta and F. Ellinger, "110 GHz travelling-wave amplifier in 22 nm FD-SOI CMOS," *2017 IEEE Asia Pacific Microwave Conference (APMC)*, Kuala Lumpur, Malaysia, 2017, pp. 406-409.

[33] B. Agarwal et al., "112-GHz, 157-GHz, and 180-GHz InP HEMT traveling-wave amplifiers," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2553-2559, Dec. 1998.

[34] C. Zech et al., "An ultra-broadband low-noise traveling-wave amplifier based on 50nm InGaAs mHEMT technology," 2012 The 7th German Microwave Conference, Ilmenau, Germany, 2012, pp. 1-4.

[35] P. V. Testa, G. Belfiore, D. Fritsche, C. Carta and F. Ellinger, "170 GHz SiGe-BiCMOS Loss-Compensated Distributed Amplifier," *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2014, pp. 1-4.

[36] S. Yoon, I. Lee, M. Urteaga, M. Kim and S. Jeon, "A Fully-Integrated 40–222 GHz InP HBT Distributed Amplifier," in *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 7, pp. 460-462, July 2014.

[37] W. S. Percival, “Thermionic Valve Circuits,” British Patent Specification no. 460,562, Jul. 24 1936.

[38] E. L. Ginzton, W. R. Hewlett, J. H. Jasberg and J. D. Noe, "Distributed Amplification," in Proceedings of the IRE, vol. 36, no. 8, pp. 956-969, Aug. 1948.

[39] W. Jutzi, "A MESFET distributed amplifier with 2 GHz bandwidth," in Proceedings of the IEEE, vol. 57, no. 6, pp. 1195-1196, June 1969.

[40] Y. Ayasli, R. L. Mozzi, J. L. Vorhaus, L. D. Reynolds and R. A. Pucel, "A Monolithic GaAs 1-13-GHz Traveling-Wave Amplifier," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 30, no. 7, pp. 976-981, Jul. 1982.

[41] Ming-Da Tsai, Huei Wang, Jui-Feng Kuan and Chih-Sheng Chang, "A 70GHz cascaded multi-stage distributed amplifier in 90nm CMOS technology," *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, San Francisco, CA, USA, 2005, pp. 402-606 Vol. 1.

[42] A. Arbabian and A. M. Niknejad, "A tapered cascaded multi-stage distributed amplifier with 370GHz GBW in 90nm CMOS," *2008 IEEE Radio Frequency Integrated Circuits Symposium*, Atlanta, GA, USA, 2008, pp. 57-60.

[43] Po-Han Chen, Kuang-Sheng Yeh, Jui-Chih Kao and H. Wang, "A high performance DC-80 GHz distributed amplifier in 40-nm CMOS digital process," *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, Tampa, FL, USA, 2014, pp. 1-3.

[44] Jonghae Kim et al., "A 12dBm 320GHz GBW distributed amplifier in a 0.12/spl mu/m SOI CMOS," *2004 IEEE International Solid-State Circuits Conference* (IEEE Cat. No.04CH37519), San Francisco, CA, USA, 2004, pp. 478-540 Vol.1.

[45] J. Plouchart et al., "A 4-91-GHz traveling-wave amplifier in a standard 0.12-/spl mu/m SOI CMOS microprocessor technology," in *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1455-1461, Sept. 2004.

[46] S. Masuda, T. Takahashi and K. Joshin, "An over-110-GHz InP HEMT flip-chip distributed baseband amplifier with inverted microstrip line structure for optical transmission system," in *IEEE Journal of Solid-State Circuits*, vol. 38, no. 9, pp. 1479-1484, Sept. 2003.

[47] Y. Li, W. -L. Goh and Y. -Z. Xiong, "A 2 to 92 GHz distributed amplifier using 70-nm InP HEMTs," 2015 *IEEE International Wireless Symposium (IWS 2015)*, Shenzhen, China, 2015, pp. 1-4.

[48] K. Eriksson, I. Darwazeh and H. Zirath, "InP DHBT Distributed Amplifiers With Up to 235-GHz Bandwidth," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1334-1341, April 2015.

[49] A. Arbabian, S. Callender, S. Kang, M. Rangwala and A. M. Niknejad, "A 94 GHz mm-Wave-to-Baseband Pulsed-Radar Transceiver with Applications in Imaging and Gesture Recognition," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 1055-1071, April 2013

[50] S. Kimura, Y. Imai, Y. Umeda and T. Enoki, "Loss-compensated distributed baseband amplifier IC's for optical transmission systems," *in IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 10, pp. 1688-1693, Oct. 1996.

[51] J. Chen and A. M. Niknejad, "Design and Analysis of a Stage-Scaled Distributed Power Amplifier," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1274-1283, May 2011.

[52] M. EL Chaar, A. L. de Souza, M. Barragan, F. Podevin and S. Bourdel, "A Non-Closed-Form Mathematical Model for Uniform and Non-Uniform Distributed Amplifiers," *2020 IEEE MTT-S International Conference on Microwaves for Intelligent Mobility (ICMIM)*, 2020, pp. 1-4.

[53] Danh Luongvinh and Youngwoo Kwon, "Behavioral modeling of power amplifiers using fully recurrent neural networks," *IEEE MTT-S International Microwave Symposium Digest, 2005.*, 2005, pp. 1979-1982

[54] Taijun Liu, S. Boumaiza and F. M. Ghannouchi, "Dynamic behavioral modeling of 3G power amplifiers using real-valued time-delay neural networks," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 3, pp. 1025-1033, March 2004

[55] Ali Reza Zirak and Sobhan Roshani, “Design and Modeling of RF Power Amplifiers with Radial Basis Function Artificial Neural Networks” *International Journal of Advanced Computer Science and Applications* (ijacsa), 7(6), 2016.

[56] D. M. Pozar, Microwave Engineering, 4th ed. Hoboken, NJ, USA: Wiley, 1998.

[57] Y. Tsividis, Operation and modeling of the MOS transistor, 2nd ed. New York; Oxford: Oxford University Press, 1999.

[58] O. El-Aassar and G. M. Rebeiz, "A DC-to-108-GHz CMOS SOI Distributed Power Amplifier and Modulator Driver Leveraging Multi-Drive Complementary Stacked Cells," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3437-3451, Dec. 2019.

[59] O. El-Aassar and G. M. Rebeiz, "A Cascaded Multi-Drive Stacked-SOI Distributed Power Amplifier With 23.5 dBm Peak Output Power and Over 4.5-THz GBW," in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 7, pp. 3111-3119, July 2020.

[60] K. Moez and M. Elmasry, "A New Loss Compensation Technique for CMOS Distributed Amplifiers," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 3, pp. 185-189, March 2009

[61] M. El-Chaar, F. Podevin, S. Bourdel, A. A. L. de Souza and J. -D. Arnould, "Integrated Stacked Parallel Plate Shunt Capacitor for Millimeter-Wave Systems in Low-Cost Highly Integrated CMOS Technologies," in *IEEE Solid-State Circuits Letters*, vol. 5, pp. 114-117, 2022.

[62] M. Seo, B. Jagannathan, J. Pekarik, and M. J. W. Rodwell, “A 150 GHz Amplifier With 8 dB Gain and +6 dBm Psat in Digital 65 nm CMOS Using Dummy-Prefilled Microstrip Lines,” in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3410–3421, Dec. 2009

[63] A.-L. Franc, E. Pistono, D. Gloria, and P. Ferrari, "High-performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Band-pass Filters," in *IEEE Trans. on Electron Device*, vol. 59, no.5, pp. 1219-1226, May 2012

[64] A. Ghadiri and K. Moez, "High-Quality-Factor Active Capacitors for Millimeter-Wave Applications," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 12, pp. 3710-3718, Dec. 2012

[65] T. Quémerais, L. Moquillon, P. Benech, J. Fournier and S. Pruvost, "CMOS 45-nm 3D metal-oxide-metal capacitors for millimeter wave applications," *Microwave and Optical Technology Letters*, vol. 53, no. 7, pp. 1476-1478, Apr. 2011

[66] J. Shi, K. Kang, Y. Z. Xiong, J. Brinkhoff, F. Lin and X. Yuan, "Millimeter-Wave Passives in 45-nm Digital CMOS," *in IEEE Electron Device Letters*, vol. 31, no. 10, pp. 1080-1082, Oct. 2010

[67] G. F. Engen and C. A. Hoer, "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, no. 12, pp. 987-993, Dec. 1979

[68] M. E. Chaar, A. L. de Souza, M. Barragan, F. Podevin, S. Bourdel and J. -D. Arnould, "Integrated Wideband Millimeter-Wave Bias-Tee – Application to Distributed Amplifier Biasing," *2021 19th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2021, pp. 1-4

[69] I.Alaji, T. Capelli Mouvand, M. El-Chaar, A. Lisboa-de-Souza, S. Bourdel, F. Podevin, "Cascaded tunable distributed amplifiers for serial optical links: some design rules," Proc. 18th IEEE Int. New Circuits and Systems Conf. (NEWCAS), Montreal, Canada, June 16-19 2020, remote conference

[70] F. Ellinger, "60-GHz SOI CMOS traveling-wave amplifier with NF below 3.8 dB from 0.1 to 40 GHz," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 553-558, Feb. 2005.

[71] T. Huang, Y. Lin, J. Cheng, J. Kao, T. Huang and H. Wang, "A high-gain low-noise distributed amplifier with low DC power in 0.18-μm CMOS for vital sign detection radar," *2015 IEEE MTT-S International Microwave Symposium*, Phoenix, AZ, 2015, pp. 1-3

[72] V. Pulijala and S. Azeemuddin, "Spiral inductors for V-band wireless ICs," *2011 IEEE Applied Electromagnetics Conference (AEMC)*, Kolkata, 2011, pp. 1-4.

[73] M. El-Chaar, L. Vincent, J. -D. Arnould, A. A. L. de Souza, S. Bourdel and F. Podevin, "Accurate Design Method for Millimeter Wave Distributed Amplifier Based on Four-Port Chain (ABCD) Matrix Model," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 11, pp. 4510-4523, Nov. 2022.