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# Low power, high-reliability class-C voltage-controlled oscillator for space application in 28 nm FD-SOI technology

Ayoub Ait Ihda

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Ayoub Ait Ihda. Low power, high-reliability class-C voltage-controlled oscillator for space application in 28 nm FD-SOI technology. Electronics. Université de Bordeaux, 2022. English. NNT : 2022BORD0442 . tel-04011169

**HAL Id: tel-04011169**

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THÈSE PRÉSENTÉE  
POUR OBTENIR LE GRADE DE  
**DOCTEUR DE**  
**L'UNIVERSITÉ DE BORDEAUX**

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR  
SPÉCIALITÉ ÉLECTRONIQUE

Par Ayoub AIT IHDA

**Low power, high-reliability class-C voltage-controlled  
oscillator for space application in 28 nm FD-SOI technology**

Sous la direction de : Yann Deval

Soutenue le 16/12/2022

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# Oscillateur commandé en tension de classe C à faible puissance et haute fiabilité pour application spatiale en technologie FD-SOI 28 nm

Des milliers de satellites orbitent autour de la terre et fournissent à des milliards de personnes des informations météorologiques, des communications, des émissions et des informations de navigation. Les services par satellite sont tellement omniprésents et essentiels dans notre vie que l'utilisation des satellites dans notre vie quotidienne est souvent devenue "invisible". Le nombre de satellites lancés dans l'espace augmente chaque année, annonçant une nouvelle course à l'espace. Cette nouvelle ère spatiale encourage la transition des technologies traditionnelles de semi-conducteurs utilisées dans l'espace, qui sont en retard sur l'état de l'art, vers les derniers nœuds technologiques qui offrent de hautes performances à faible coût, comme la technologie CMOS FD-SOI de 28 nm.

Outre des performances spectrales élevées pour les communications à large bande, les émetteurs-récepteurs de satellites doivent être très fiables et consommer peu d'énergie, l'électricité étant une denrée rare dans l'espace. L'oscillateur commandé en tension (VCO) est l'un des blocs de circuit les plus importants dans les émetteurs-récepteurs de satellite en termes de dissipation de puissance et de performance globale. Le travail de thèse se concentre sur la conception d'une nouvelle topologie VCO pour la communication par satellite avec un compromis équilibré entre la fiabilité, le bruit de phase, la consommation d'énergie et la plage d'accord.

**Mots clés :** Oscillateur commandé en tension, FD-SOI, fiabilité, réglage du bruit de phase, oscillateur sans varactor, classe C, polarisation de la grille arrière.

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## Low power, high-reliability class-C voltage-controlled oscillator for space application in 28 nm FD-SOI technology

Thousands of satellites orbits around the earth providing billions of people with meteorological and weather information, communications, broadcasting, and navigational information. Satellite services become so omnipresent and essential in our life that the use of satellites in our daily life has often become "invisible". The number of satellites launched into space is increasing every year, heralding a new space race. This new space era encourages the transition from traditional semiconductor technologies used in space, which lag behind the state of the art, to the latest technology nodes that offer high performance at low cost such as 28 nm FD-SOI CMOS technology.

In addition to high spectral performance for broadband communications, satellite transceivers must have high reliability and low power consumption, as electricity is a rare commodity in space. Voltage Controlled Oscillator (VCO) is one of the most important circuit blocks in satellite transceivers in terms of power dissipation and overall performance. The thesis work focuses on the design of a new VCO topology for satellite communication with a balanced trade-off between phase noise, reliability, power consumption, and tuning range.

**Keywords:** Voltage-Controlled Oscillator, FD-SOI, Reliability, Phase Noise Tuning, Varactor-less Oscillator, Class-C, Body-Biasing.

---

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# Acknowledgments

First of all, I would like to express my deep gratitude to my supervisors, Yann DEVAL, Hervé LAPUYADE, and François RIVET for their invaluable guidance, encouragement, and support throughout this thesis. Without their expertise and unwavering belief in my abilities, this thesis would not have been possible.

I would also like to thank all members of the jury Christian ENZ, Gilles JACQUEMOD, Stephane ROCHETTE, Matthieu GASTALDI, Jean-Louis CAZAUX who accepted to be part of my defense's jury. An additional special thanks to Eric Kerherve who accepted to be the president of my jury

I am also indebted to CNES and Thales Alenia Space for providing the financial support that made this research possible.

I would like to thank Magali for her assistance and support throughout the measurement process. Thank you for going above and beyond to ensure the success of the measurements.

I would like to thank Justine for her help, kindness, and support in the writing process.

I am also grateful to my colleagues and friends in the IMS laboratory who have provided me with support and motivation throughout this journey. In particular, I would like to thank Manuel, Benjamin, Andres, Gwennaël, Issam, Marwane, and Mohamed Amine for their valuable contributions and for always being there to listen and offer encouragement.

Finally, I want to extend a heartfelt thank you to my family, especially my parents, Amina and Mbarek, for their constant love and support. Their constant encouragement, guidance, and belief in my abilities have been a constant source of motivation and inspiration throughout my life. I am deeply grateful for everything they have done for me and couldn't have made it this far without their love and support. +•|[[[ξO+

In conclusion, I would like to acknowledge the support and encouragement of my friends, who have been a constant source of inspiration and support throughout this process. Thank you all for your encouragement, patience, and understanding.

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# Introduction

Thousands of satellites orbit around the earth providing billions of people with meteorological and weather information, communications, broadcasting, and navigational information. Satellite services become so omnipresent and essential in our life to the extent that the use of satellites in our daily life has often become "invisible". The number of satellites launched into space is increasing every year, heralding a new space race, not between governments this time, but between companies. New Space is the term used to describe this new era of the space industry, which is characterized by a desire to democratize access to space through affordable rocket launches and cost-effective satellites. This vision encourages the transition from traditional semiconductor technologies used in space, which lag behind the state of the art, to the latest technology nodes that offer high performance at low cost such as 28 nm FD-SOI CMOS technology.

Satellite communication services are expected to develop more high data rate communications. There are two main reasons for this: 1) the growing demand for streaming media instead of traditional broadcasting media and 2) the motivation to have global coverage, even in isolated areas. The ways to increase data rate are 1) by increasing the bandwidth via moving to higher communication frequencies, such as mm-wave frequencies, or 2) by using advanced modulation techniques to increase the transmitted data, such as Orthogonal Frequency-Division Multiplexing (OFDM), which requires stringent phase noise. In addition to high spectral performance for broadband communications, satellite transceivers must have high reliability and low power consumption, as electricity is a rare commodity in space. Voltage Controlled Oscillator (VCO) is one of the most important circuit blocks in satellite transceivers in terms of power dissipation and overall performance. The thesis work focuses on the design of a VCO for satellite communication aiming at the following goals:

- Development of a new VCO topology in 28nm FD-SOI with an optimal trade-off between reliability, low power, low phase noise, and wide tuning range for millimeter-wave and Ku-band frequencies targeting high data rate satellite communications.
- Explore 28nm FD-SOI CMOS technology for space applications and demonstrate its unique capabilities using the body-biasing feature in the proposed VCO topology.

This manuscript is composed of five chapters. The first chapter outlines the context of this work and presents the main limitations and trade-offs in oscillator design. The main oscillator topologies are presented and compared.

The second chapter presents the 28 nm FD-SOI CMOS technology and introduces the proposed oscillator based on a transformer resonator and a class C topology. The reliability problems of harmonic oscillators are discussed and a solution for the long-term reliability of the proposed oscillator is presented. The chapter provides a theoretical analysis of the phase noise of the proposed oscillator.

The third chapter describes the design methodology used to implement the proposed VCO topology in mm-wave and Ku band frequencies. The challenges and target specifications are presented for each VCO.

The fourth chapter presents the measurement results and proof of concept of the proposed VCO in mm-wave and Ku-band frequencies. The performance of the two designed VCOs is compared with the state-of-the-art.

The last chapter provides a general conclusion of the thesis work and presents the research perspectives of the proposed VCO topology.

# Chapter 1:

## Overview of satellite communication to harmonic oscillators

*Satellite communication is an essential asset in our modern communication systems that required reliable and high-speed transceivers to meet the increasing demand for data rate in the consumer market. The first part of this chapter presents the history, financial prospects, and challenges of satellite communication. The second part of the chapter provides an overview of harmonic oscillators, presenting the basics of oscillators and phase noise theory, highlighting the main trade-offs in oscillator design, and comparing the main oscillator topologies.*

### 1. Satellite communications: then and now

The concept of satellite communications was introduced in 1945 in an article by Arthur C. Clarke in *Wireless World* magazine. [1]. Clarke described the fundamentals behind the deployment of manned satellites into specific orbit (later known as a geostationary orbit GEO or “Clarke Belt”) to relay radio signals. A satellite in Clarke’s Orbit covers 44% of the earth’s surface. Hence, with only 3 satellites, with inter-satellite communication, the entire globe communication is covered as shown in Figure 1-1. Moreover, thanks to the stationarity of the satellites relative to the earth, ground antennas are simpler to build, and signals sent to the earth are received 24 hours a day without interruption. Thereby increasing the ease of communication.

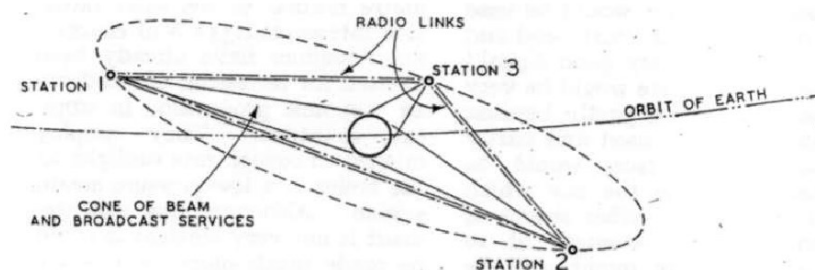


Figure 1-1: Arthur C. Clarke’s sketch describing the coverage of the entire world with three satellites [1].

Clarke thought that the satellite required a human presence to replace the radio tubes because the radio tubes of the time had a very short life. So he did not try to patent the idea of a geosynchronous communication satellite. Little did he know that a few years later, Bell Laboratories would announce the invention of the transistor in 1947. This revolutionary invention and the integrated circuits that followed it took satellite communications from science fiction to a possible reality. These devices not only brought reliable satellite technology to life but also enabled the creation of high-speed electronic computers that do the calculations to accurately deploy a satellite in orbit.

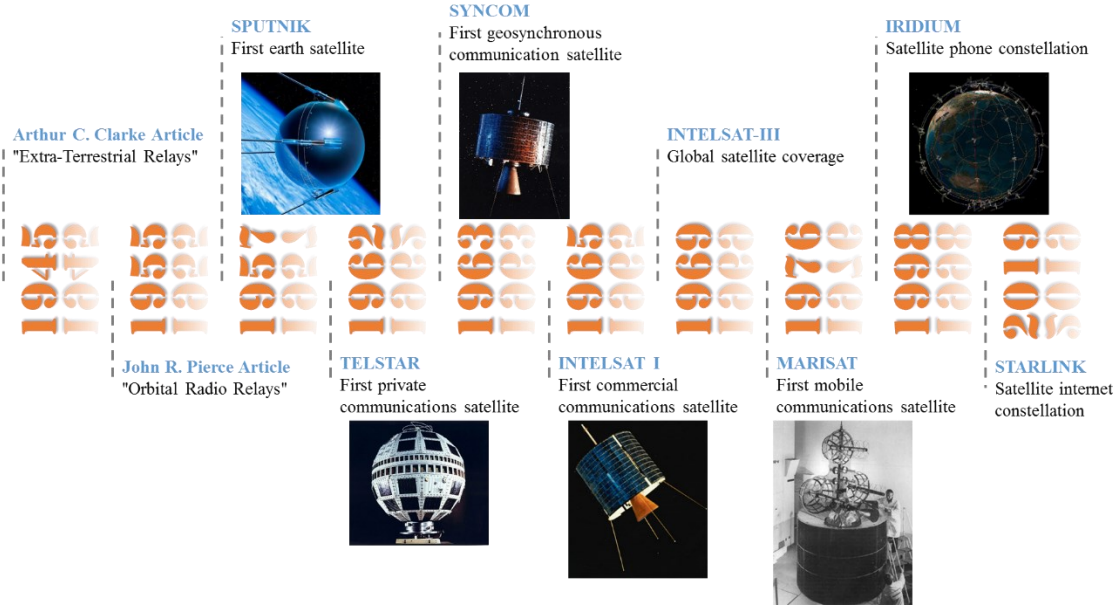


Figure 1-2: A selective communications satellite timeline [2].

Figure 1-2 shows a timeline with a selective communications satellite timeline. The idea of satellite communications became a reality with the launch of the first artificial satellite by the Soviet Union in 1957. Sputnik, a silver orb the size of a bullet, orbited the earth every 96 minutes, sending beeps to earth through an onboard radio transmitter. This achievement triggered the space race between the United States and the Soviet Union, which permitted the quick development of the space sector. In 1962, NASA launched the world's first privately funded communications satellite, TELSTAR, which transmitted the first live transatlantic broadcast between Europe and the United States. The year 1963 saw the launch of the first geosynchronous satellite, SYNCOM, which was used in 1964 to broadcast the Tokyo Olympic Games for the first time. Communication Satellite Corporation (COMSAT) launched Early Bird (Intelsat I) in 1965, the first commercial communication satellite placed in geosynchronous orbit. Its successor, INTELSAT-III series launched in 1969, achieved



global coverage on which the first moon landing was broadcast to 600 million viewers worldwide. At the end of the twentieth century, the space industry developed more specialized satellites that eclipsed the previous ones. Starting in 1976 with the launch of the first communication system to provide mobile services, MARISAT. With the emergence of new technologies such as cell phones, the internet, and the Internet of Things (IoT), global communications have grown exponentially. Hundreds of sophisticated low earth orbit (LEO) satellite constellations have been deployed, providing high-speed, low-latency digital communications and global coverage in even the most remote areas of the world. From the Iridium 66 satellites that provide pole-to-pole phone coverage, launched in 1998, to Starlink which promises to provide low-cost internet to isolated locations with a mega-constellation of 12,000 satellites.

The rapid development of satellite communications is due to its financial prospects. John R. Pierce was one of the pioneers to highlight the economic potential of satellites, in his 1954 speech and 1955 article, where he demonstrated the potential superiority of satellite communication capacity over the first transatlantic telephone cable (TAT-1), which could carry 36 simultaneous telephone calls for \$30-50 million, compared to an estimated 1,000 simultaneous telephone calls by satellite. Pierce wondered if a satellite would be worth a billion dollars. Nowadays, thousands of applications satellites orbits around the earth providing over a billion people with meteorological and weather information, communications, broadcasting, and navigational information. Satellite services have become so ubiquitous that they have become almost commonplace in the space of half a century. To the extent that the use of satellites in our daily life has often become "invisible". Figure 1-3 shows the number of operational satellites by mission type in recent years. The number of satellites increases by 252% in the 10 years between 2010 and 2020. The market for satellite applications will continue to grow rapidly and diversify for many years to come, as the space industry enters a new chapter called the "New Space", characterized by a desire to democratize access to space through more affordable launches (reusable rockets, carpooling) and satellites (small satellites). In 2020, satellite services realized more than \$117 billion in revenue. If we include the costs of the launch industry, satellite manufacturing, and ground equipment, the annual revenues of the satellite industry reach \$271 billion, representing 74% of the global space economy (see Figure 1-4). The satellite industry is a global industry that has been growing steadily for several decades, even in times of global recession. John R. Pierce's prediction was right, it would be worth a billion dollars.

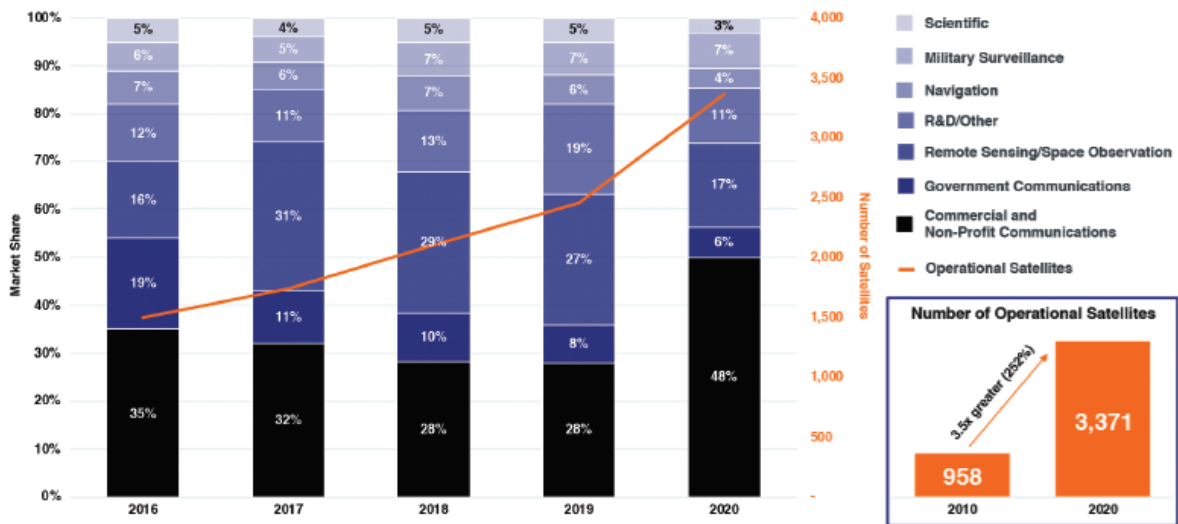


Figure 1-3: The number of operational satellites by mission type between 2016 and 2020 [3].

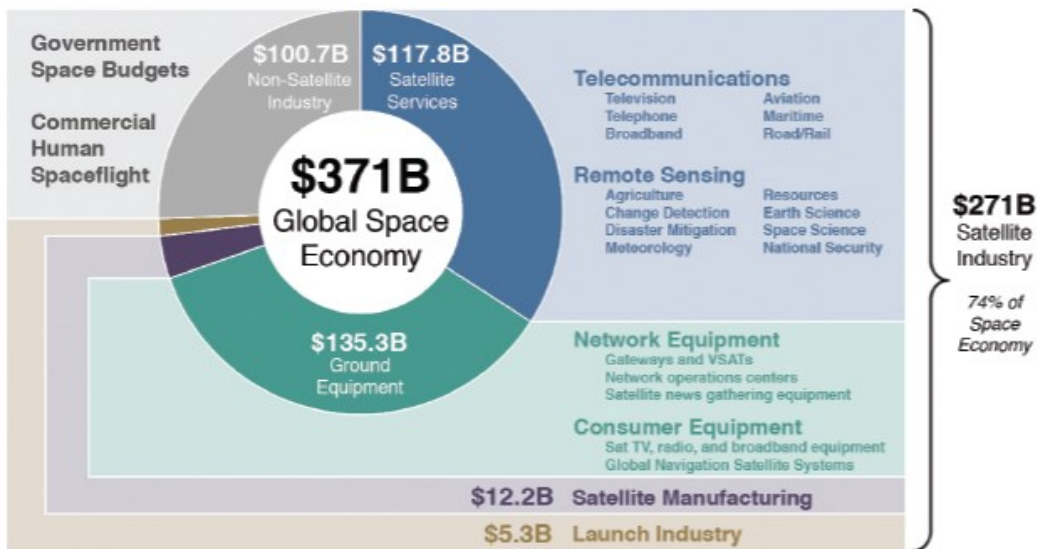


Figure 1-4: 2020 satellite industry revenues worldwide in billions of U.S. dollars [3].

## 2. Electronic circuits in space

TELSTAR was the first satellite to transmit a transatlantic broadcast in space and the first victim of an electronic failure caused by radiation. Four months after the launch of TELSTAR in 1962, it ceased to function. The problem was linked to a transistor failure due to radiation caused by a nuclear weapon explosion test at a high altitude that took place the day before Telstar's launch. Other satellites have been lost for the same reason - radiation. Since then, the effects of radiation and its mitigation in electronics have become a top priority for the space industry. The construction of satellites requires astronomical costs that reach hundreds of millions of dollars. Therefore, no tolerance is accepted for electronic failure in such systems.

Satellites are so essential to the functioning of the modern world (weather forecasting, navigation ...) that their loss would have catastrophic consequences.

Radiation affects satellite electronics in two main ways: total ionizing dose (TID) and single event effects (SEE). Exposure of the device to radiation in space leads to an accumulation of charges in the device. This results in a progressive deterioration of the device's performance over time. The total accumulated dose is a function of time and altitude and is quantified by the TID measured in units of kilorads (krad). For instance, an unshielded satellite in GEO could absorb a TID of over 20 Megarad (Mrad) in one year. In contrast, the same satellite in LEO would absorb only about 100 krad in a year.

SEE is an instantaneous phenomenon triggered by a strike from a highly energetic particle. The collision can result in data disruption or a complete device latch-up. SEEs are divided into soft errors and hard errors. Soft errors are non-destructive and disappear after a reboot, while hard errors are irreversible and result in system malfunction or, worse, loss of the entire circuit.

For radiation mitigation, the space sector traditionally relied on radiation-hardened by design circuits. Hardened chips are implemented in custom semiconductors. In the past, the government and the military led the development of new semiconductor manufacturing processes, as they were the main customers of the semiconductor industry. Today, the semiconductor industry has shifted its focus to the consumer electronics market (cell phones, IoT, gaming...), thus radiation-hardened technologies used for space applications are often far from state-of-the-art. Moreover, radiation-hardened devices are expensive as they are required to undergo rigorous testing.

Traditional space players, such as NASA, ESA, and Roscomos, are committed to a high level of mission reliability and safety and therefore use high-value radiation-hardened products. While the "New Space" actors (startups and smaller companies) are more interested in the democratization of space with affordable satellites, they therefore creatively employ unconventional components, and design techniques to cut costs. Nowadays small satellites for LEO missions are designed by commercial-off-the-shelf (COTS) integrated circuits with plastic packaging rather than the hermetically sealed ceramic packaging preferred in spacecraft, to cut costs. Along with their low price, these components bring the benefits of ultra-submicron microelectronics (higher integration, faster processing, and lower power consumption) to the space industry. However, the use of COTS products significantly

increases the risks of the mission. In brief, COTS sacrifices reliability for a low price, unlike radiation-hardened products that provide a high level of reliability for a considerable cost. Radiation-tolerant devices by reputation offer the best of both worlds. These devices are radiation tolerant by design and implemented in a qualified process such as silicon-on-insulator technologies. This eliminates some testing and selection costs. For example, SEE sensitivity testing does not need to be repeated on every batch because it is technology-dependent.

### 3. High-speed communications

The demand for high data rates continues to grow. This increase is driven by the rapid growth of streaming media over broadcast media, and gaming (especially in this covid pandemic), in addition to entertainment, other applications also require high-speed communications, such as telemedicine that can bring low-cost health care to remote areas. High-speed communication is carried out through two main channels: wireless and wireline connections. Wireless communication is primarily used for mobile telephony and broadband data communications like Wi-Fi. Wireline communication is provided by networks such as the local area network (LAN) and the wide-area network (WAN). Wired communication is primary data communication technology thanks to its ability to support high-speed communications.

Wireline broadband communication is limited to certain areas because it requires an existing infrastructure. For extended coverage, wireless communication is the answer. With the standardization of 5th generation (5G) mobile technology a new term emerge called Non-Terrestrial Network (NTN), which refers to communication systems via satellites, unmanned aerial systems (UAV), and high altitude platforms (HAPs). The idea is to incorporate these systems into 5G as a complement to terrestrial systems to provide global coverage, even in isolated areas, with high data rates and low latency (see Figure 1-5).

There are two main ways to increase the communication data rate: 1) increasing the channel capacity, which is equivalent to widening the radio bandwidth, and 2) using advanced modulation and coding techniques. Moving to higher frequency provides wide bandwidth, thus operators are interested in shifting from the congested RF bands to millimeter waver bands such as Ka and V-band. However, high frequency faces some challenges related to the environment like rain fading and large transmission loss. On the other hand, modulation techniques increased the data rate such as Orthogonal Frequency Division Multiplexing

(OFDM) used in 4G, WI-FI, and now in 5G. The principle of OFDM is based on the division of data into several orthogonal subcarriers, transmitted in parallel. OFDM systems are sensitive to the phase noise of the local oscillator, so they require strict specifications from the transceiver, especially the oscillator, not only in terms of phase noise but also in terms of power consumption and reliability, a fortiori when it is intended for a space application.

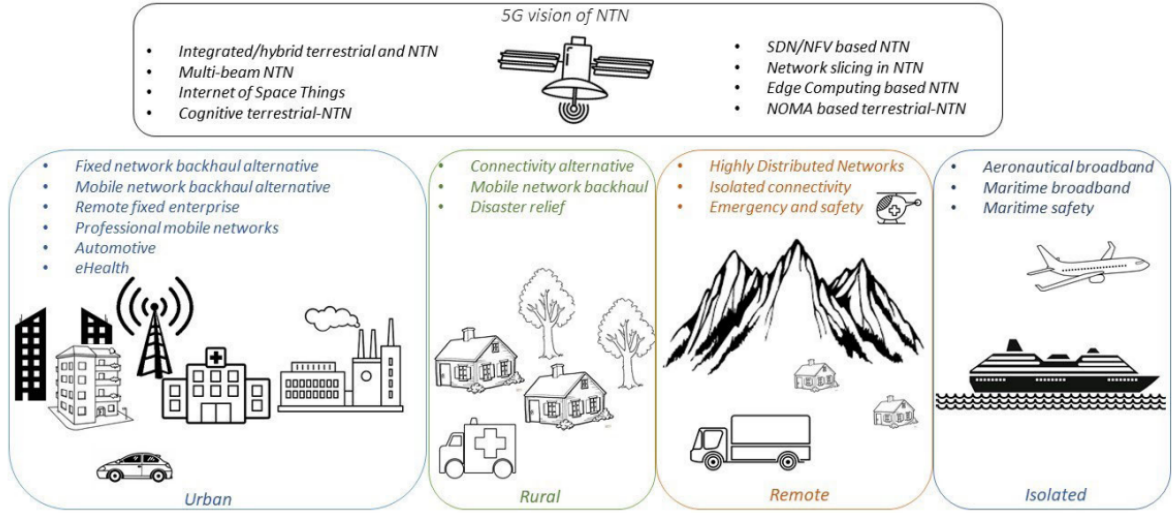


Figure 1-5: The NTN in the 5G ecosystem [4].

#### 4. Oscillators

Oscillators are autonomous systems that produce time information. For example, a pendulum, when displaced from its resting position, swings back and forth for a certain period of time. The motion of the pendulum results from the conversion of potential energy into kinetic energy and vice versa. However, the oscillation stops due to air resistance and hinge friction that converts some of the pendulum’s energy into heat with each cycle. The oscillation will be sustained if we give the pendulum an impulse at each period to replenish the losses.

The LC oscillator is shown in Figure 1-6 works in the same way as the pendulum. A charged capacitor in an LC tank discharges into the inductor, converting electrical energy into magnetic energy. When the capacitor is empty, the inductor maintains the current flow in the circuit by charging the capacitor in the opposite direction. Thus, the magnetic energy is converted back into electrical energy. The exchange of energy in the LC tank produces a periodic signal. This signal, like the pendulum, dwindles with time until it stops due to the series resistance of the capacitor, the inductor, and the wires. To maintain the oscillation,

active device A is connected to the LC resonator to compensate for the energy lost due to the circuit imperfections.

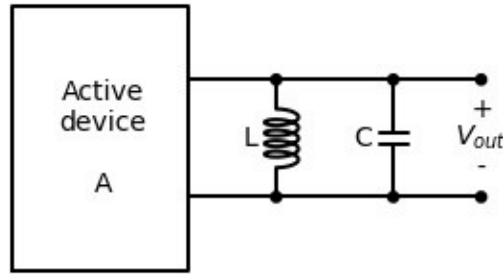


Figure 1-6: LC oscillator model.

“Amplifiers oscillate, and oscillators amplify” this common saying among RF circuit designers implies that a poorly designed amplifier may turn into an oscillator and vice versa. In fact, in 1912, Armstrong noticed the appearance of parasitic high-frequency signals while experimenting with his regenerative circuit (positive feedback amplifier). It turned out that the amplifier was oscillating. Armstrong increased the feedback until the amplifier was unstable and thud he invented the first electronic oscillator.

In 1921, Barkhasuen stated that for a positive feedback system, oscillation occurs when the loop gain has a phase shift of zero and a magnitude of unity. Figure 1-7 shows the feedback model of an oscillator. The amplifier  $A$  compensates for the resonator  $\beta(j\omega)$  losses at a given frequency  $\omega_0$ . The amplitude and phase conditions for a sustained oscillation, known as the Barkhausen criterion, are:

$$|A\beta(j\omega)| = 1 \quad \text{Eq 1.1}$$

$$\arg A\beta(j\omega) = 0 \quad \text{Eq 1.2}$$

The resonator provides a  $360^\circ$  phase shift at the resonance frequency  $\omega_0$ . The signal returns itself after a cycle around the loop provided that the loop gain is unity. In reality, the oscillation starts from noise. The noise is amplified with  $|A\beta(j\omega)| > 1$  and the resonator selects only the signal at the frequency  $\omega_0$  defined by Eq (1.2). The oscillation builds up exponentially at  $\omega_0$  until the amplifier’s non-linearity saturation reduces the loop gain and limits the amplitude growth. At the steady-state, the loop reaches the sustained oscillation condition  $A\beta(\omega_0) = 1$ . Thus, the amplitude is defined by the circuit non-linear saturation and the oscillation frequency is obtained from Eq (1.2).

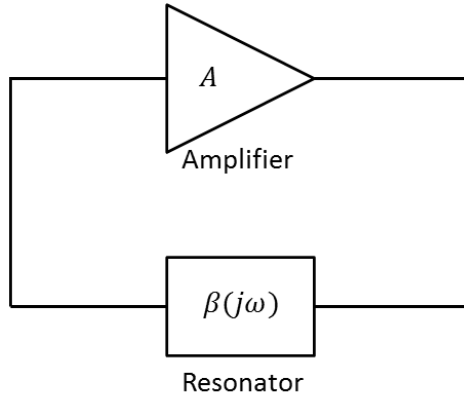


Figure 1-7: Oscillator feedback model.

## 5. Phase noise

An ideal oscillator generates a sinusoidal signal with a single frequency component, as depicted in Figure 1-8.a. The zero-crossing of such signal occurs regularly at  $nT/2$ , where  $n$  is the  $n$ -th zero crossing. On the other hand, A real oscillator is prone to its intrinsic noise that causes fluctuations in amplitude and phase. Such a noisy signal is expressed as follows:

$$V(t) = V_0[1 + \alpha(t)] \cos(\omega_0 t + \phi(t)) \quad \text{Eq 1.3}$$

where  $V_0$  is the amplitude,  $\omega_0$  is the oscillation frequency,  $\alpha(t)$  describes the amplitude fluctuation and  $\phi(t)$  denotes phase fluctuation. The saturation of the oscillator at steady-state suppresses amplitude noise, hence only the phase noise matters in oscillators. Phase perturbations cause the zero-crossing instant to drift randomly from its nominal value, this drift is referred to as jitter. The deviation of the zero-crossing of the signal results in a random change in the instantaneous frequency, consequently the signal energy is spread at the vicinity of the center frequency. The spectrum of the oscillator's output signal exhibits bandwidth broadening, as shown in Figure 1-8.b. Intuitively, the more one moves away from the center frequency of the signal, the more the signal strength fades, as the oscillator tends to hold the oscillation at the center frequency. This explains the skirted shape of the oscillator's spectrum.

The spectral purity of the oscillator is measured by the phase noise which is defined by IEEE standards as [5]:

$$\mathcal{L}(f) = \frac{S_\phi(f)}{2} \quad \text{Eq 1.4}$$

where  $S_{\phi}(f)$  is the one-sided power spectral density of the random phase fluctuation  $\phi(t)$ . In practice,  $\mathcal{L}(f)$  is expressed as  $10 \log_{10}[\mathcal{L}(f)]$  and is given in dBc/Hz. This latter stands for dB below the carrier in a 1 Hz bandwidth.

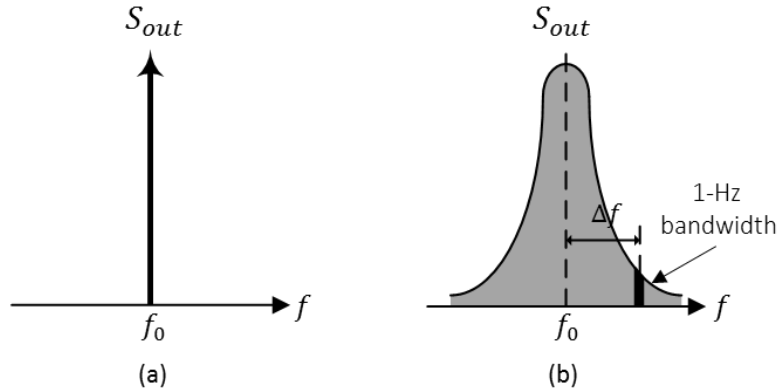


Figure 1-8: Frequency response of (a) an ideal oscillator, (b) a real oscillator.

The oscillator phase noise is a major bottleneck in wireless communication systems. In a receiver, the shape of the local oscillator skirt converts the adjacent interfering signal with the wanted signal, as shown in Figure 1-9. This results in an overlap of the spectrum of the interfering signal with the signal of interest, which corrupts the detection. Thus, the communications system, due to phase noise, becomes very sensitive to neighboring interfering signals. In a transmitter, the strong output signal with the skirt spectrum hides the adjacent weak signal that needs to be detected, which again corrupts the detection (cf. Figure 1-10).

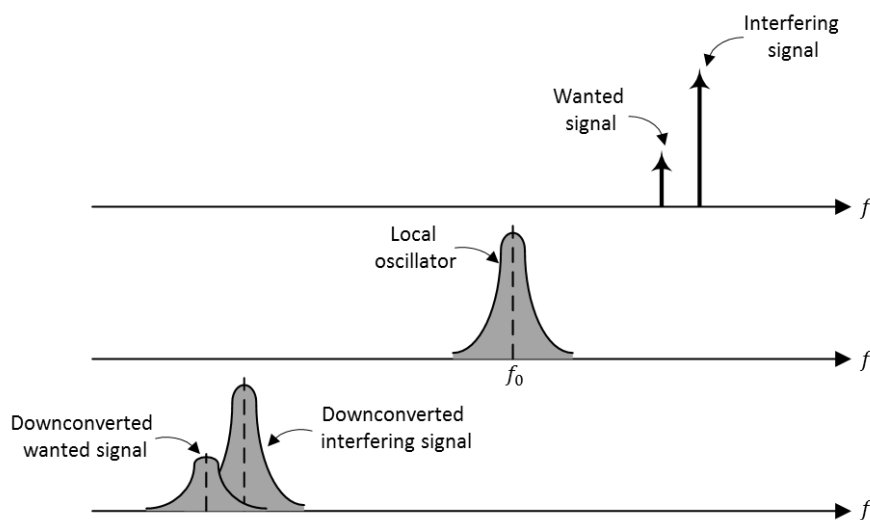


Figure 1-9: Effect of phase noise on a receiver.



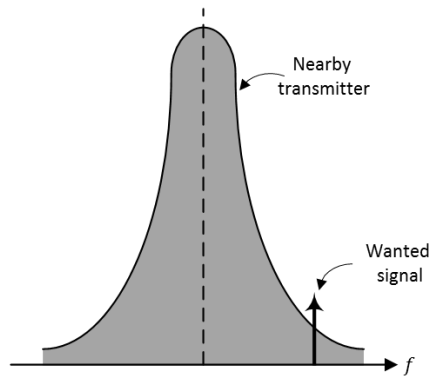


Figure 1-10: Effect of phase noise on a transmitter.

Stringent requirements were placed on the oscillator phase noise to meet communication standards. In the North American Digital Cellular (NADC) IS-54 system, the phase noise must be -115 dBc/Hz at an offset of 60 kHz from the carrier. To design an oscillator with such low phase noise, designers must have a good understanding of phase noise mechanisms and patterns.

### 5.1. Phase noise model

The spectrum of the phase noise of the oscillator is modeled by the power-law spectral densities. The experimentally observed random phase fluctuation can be represented as follows:

$$S_{\phi} = \sum_{i=-4}^0 b_i f^i \quad \text{Eq 1.5}$$

Figure 1-11 depicts the power-law spectrum. Distinct noise regions are observed and in each region, the power spectral density of the noise has a dependence on  $1 / f^n$ , where  $n$  is between 0 and 4. Sometimes higher slope regions add to the power-law spectra such as  $1/f^5$  noise observed experimentally in some oscillators. In practice, not all oscillators display all the regions, one or more regions disappear because the cross-over frequency (frequency at which the power density changes the slope) is out of order.

Each region is named [5] as follows: the first is called white noise,  $f^0$ , the second is flicker noise,  $f^{-1}$ , then white frequency,  $f^{-2}$ , followed by the flicker frequency,  $f^{-3}$ , and random walk frequency,  $f^{-4}$ . Oscillators incorporate all of these noise processes, whereas two-port devices have only the white and flicker noise.

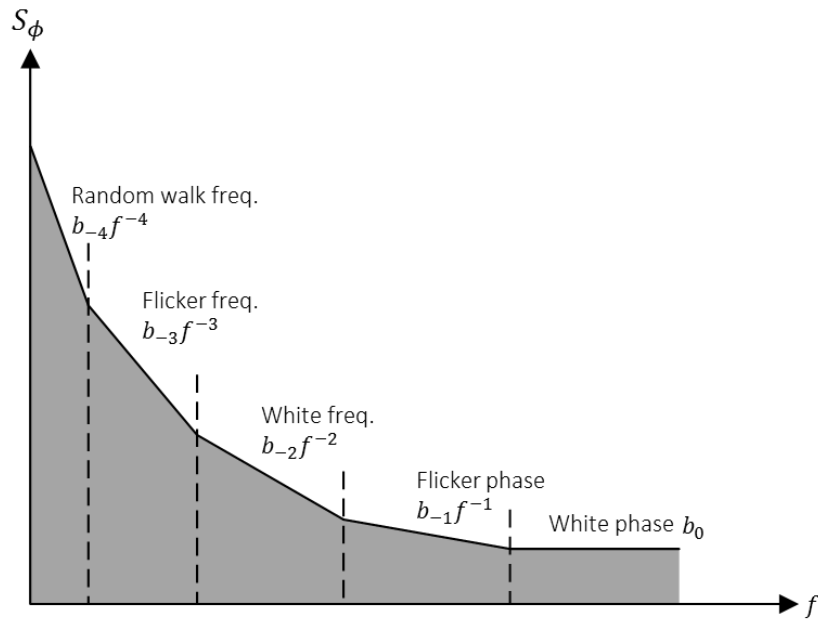


Figure 1-11: Power-law spectrum.

### 5.1.1. Leeson model

The power law describes the shape of the oscillator's phase noise spectrum but does not give any insight into the physical process behind such noise characteristics. In 1966, Leeson proposed a heuristic model that describes the generation of phase noise in oscillators [6]. Leeson builds his model (cf. Figure 1-12) on 4 assumptions: 1) the amplifier is assumed noiseless; 2) the resonator acts as a bandpass filter and selects the oscillating frequency; 3) the noise source  $\psi$  englobes all noise sources in the oscillator; 4) the amplifier noise is quenched by amplifier saturation, thus only phase noise remains [7].

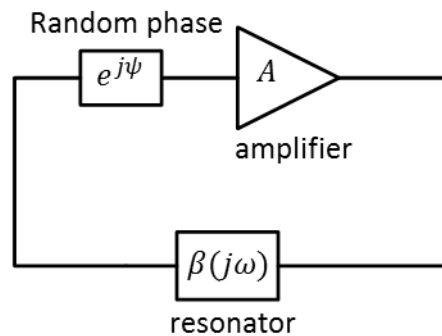


Figure 1-12: Oscillator model with the phase noise of the amplifier and all other components modeled as random phase  $\psi$ .

Under these assumptions, the oscillator is considered a first-order filter with a perfect integrator and a cutoff frequency  $f_L$  called Leeson frequency (cf. Figure 1-13) [8]:

$$S_{\phi} = \left(1 + \frac{f_L^2}{f^2}\right) S_{\psi} \quad \text{Eq 1.6}$$

where  $S_{\psi}$  is the power spectral density of the amplifier noise,  $f_L = f_0 / 2Q_T$ ,  $f_0$  is the center frequency,  $Q_T$  is the loaded quality factor. The phase noise from the internal components of the oscillator is multiplied by  $1/f^2$  to appear as frequency noise in the oscillator, as shown in Figure 1-13. This mechanism is known as the Leeson effect. The oscillator flicker noise is upconverted to flicker frequency noise  $f^{-3}$  and the white noise becomes white frequency noise  $f^{-2}$  in the passband of the oscillator (cf. Figure 1-14).

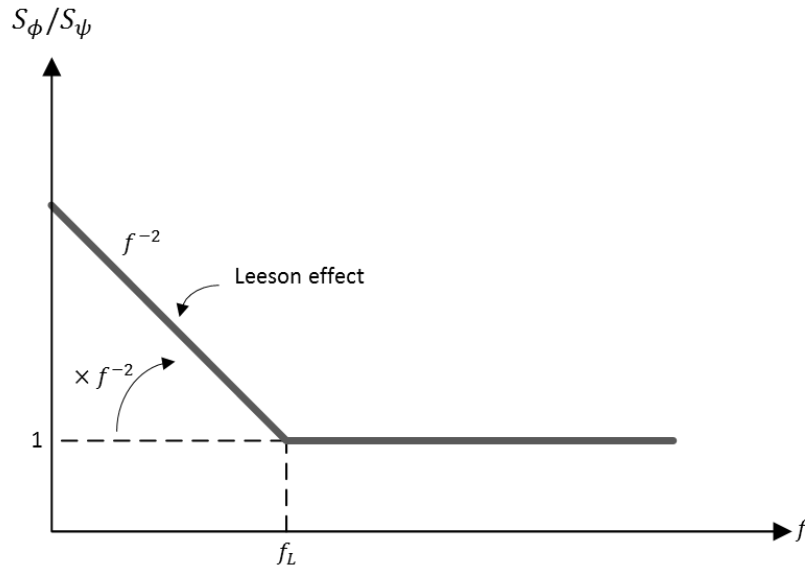


Figure 1-13: The Leeson effect phase transfer function  $S_{\phi}/S_{\psi}$ .

The mathematical expression of the Leeson model is [6]:

$$\mathcal{L}(\Delta f) = \frac{2Fk_bT}{P_{RF}} \left(1 + \left(\frac{f_0}{2Q_T\Delta f}\right)^2\right) \quad \text{Eq 1.7}$$

where  $F$  is an empirical parameter (called device excess noise number),  $k_b$  is Boltzmann's constant,  $T$  is the absolute temperature,  $P_{RF}$  is the power of the oscillating signal, and  $\Delta f$  is the offset frequency from the carrier. The equation gives the phase noise as the ratio of thermal noise power to signal power, multiplied by the resonator bandwidth correction factor  $\left(1 + \left(\frac{f_0}{2Q_T\Delta f}\right)^2\right)$ . To account for the generation of  $f^{-1}$  and  $f^{-3}$  noise, another term was added to the original equation:

$$\mathcal{L}(\Delta f) = \frac{2Fk_bT}{P_{RF}} \left(1 + \left(\frac{f_0}{2Q_T\Delta f}\right)^2\right) \left(1 + \frac{f_c}{\Delta f}\right) \quad \text{Eq 1.8}$$

where  $f_c$  is the corner frequency between  $f^{-2}$  and  $f^{-3}$  noise region.

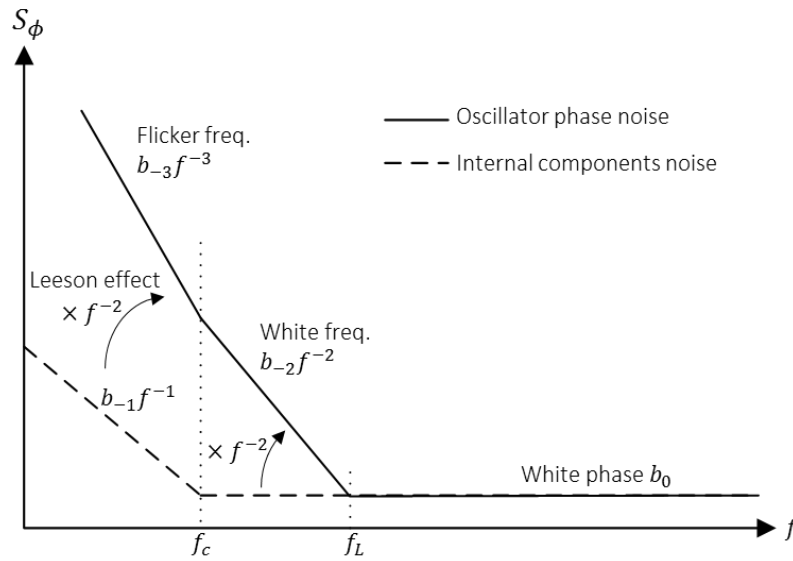


Figure 1-14: Conversion of device noise to oscillator's phase noise.

Leeson's model, although simple to follow, has serious limitations. The factor  $F$  accounts for the discrepancy between the noise level predicted by Eq (1.8) and the measured one. This empirical parameter cannot be determined a priori. Moreover, the measurements showed that  $f_c$  is unequal to  $1/f$  noise corner as asserted by the model. Thus,  $f_c$  is also an empirical fitting parameter.

### 5.1.2. Hajimiri and Lee model

The noise undergoes multiple frequency transformations to appear as phase noise in oscillators. Leeson's linear time-invariant model explains the up-conversion of near DC noise to phase noise, but it does not address the down-conversion of noise around harmonics frequencies to close-in phase noise. Hajimiri and Lee [9] abandon the time-invariant model for a linear time-variant model to include these high-order conversion mechanisms.

In Hajimiri and Lee's theory, phase noise generation is determined by the instant at which the noise impulse is injected into the circuit. The noise injected at the peak of the oscillating signal produces amplitude modulation with no effect on phase, as depicted in Figure 1-15.a. In contrast, noise injected at the zero-crossing of the signal causes phase noise with no effect on amplitude, as shown in Figure 1-15.b. If noise is injected between these two instances, it causes both amplitude and phase noise. This sensitivity of phase noise to the time of noise injection is quantified by a function called Impulse Sensitivity Function (ISF). The ISF

function has its maximum at the zero-crossing of the oscillator signal and its minimum at the peak of the signal. Figure 1-16 shows the ISF of a harmonic oscillator. The oscillator phase response to a noise impulse is [9]:

$$h_{\phi}(t, \tau) = \frac{\Gamma(\omega_0 t)}{q_{max}} u(t - \tau) \quad \text{Eq 1.9}$$

where  $\Gamma$  is the impulsive sensitivity function,  $q_{max} = CV_0$  is the maximum displacement across the tank capacitor,  $C$  is the tank capacitance,  $V_0$  is the amplitude of the oscillation signal,  $t$  is the observation time and  $\tau$  is the time of the excitation.

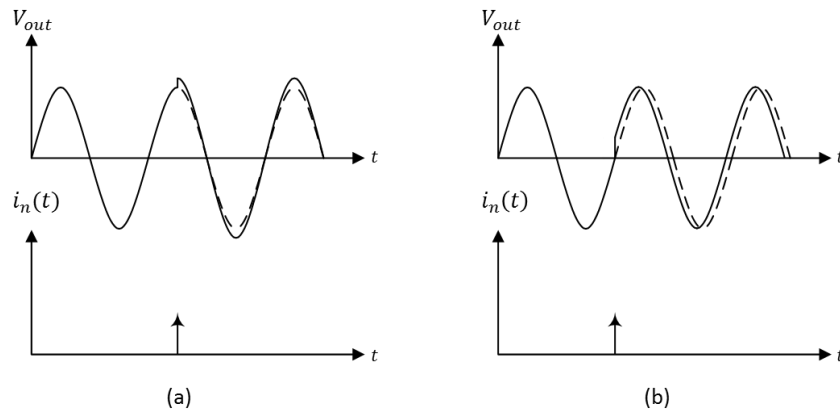


Figure 1-15: (a) Effect of impulse injection at peak of the waveform, (b) effect of impulse injection at zero crossing of waveform.

The random phase fluctuation, added into the carrier's phase, is obtained by convolving the current noise source and the ISF as:

$$\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^t \Gamma(\omega_0 t) i(\tau) d\tau \quad \text{Eq 1.10}$$

where  $i(\tau)$  is the noise current injected in the oscillator. The ISF is a periodic function, hence it can be expressed as a Fourier series. Thus, Eq (1.10) becomes:

$$\phi(t) = \frac{1}{q_{max}} \left[ c_0 \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0 \tau) d\tau \right] \quad \text{Eq 1.11}$$

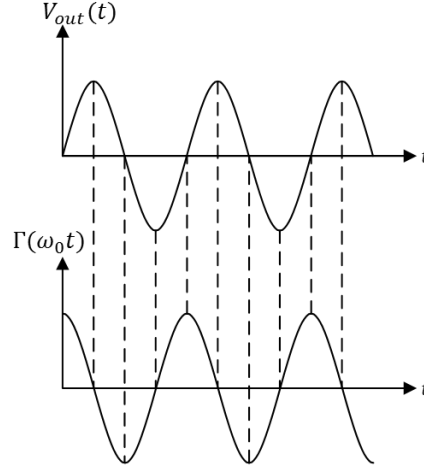


Figure 1-16: ISF waveform of an oscillator with a sinusoidal output.

where  $c_n$  are coefficients of the Fourier series. The first term with  $c_0$  coefficient designates noise that is up-converted from the baseband, while the second term represents the contribution of noise near harmonic frequencies down-converted to the oscillator phase noise. The phase noise spectral density at an offset frequency  $\Delta\omega$  from the carrier can be expressed as [9]:

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left( \frac{\Gamma_{rms}^2}{C^2 V_0^2} \cdot \frac{\overline{i_n^2} / \Delta f}{2\Delta\omega^2} \right) \quad \text{Eq 1.12}$$

where  $\overline{i_n^2}$  is the power spectral density of the white noise current and  $\Gamma_{rms}$  is the effective impulsive sensitivity function. The LC-tank losses are represented by  $R_p = Q_T / (\omega_0 C)$ . The general phase noise expression becomes:

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left[ \frac{\overline{i_n^2} / \Delta f}{P_{RF}} R_p \cdot \Gamma_{rms}^2 \cdot \left( \frac{\omega_0}{2Q_T \Delta\omega} \right)^2 \right] \quad \text{Eq 1.13}$$

where  $P_{RF} = V_0^2 / (2R_p)$  is the signal power. The upconversion of flicker noise to  $1/f^3$  phase noise is expressed as:

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left( \frac{\frac{\overline{i_n^2}}{\Delta f} c_0^2}{8q_{max}^2 \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right) \quad \text{Eq 1.14}$$

where  $\omega_{1/f}$  is the  $1/f$  corner frequency.

## 5.2. Phase noise trade-offs

Analog circuit design is about choosing the right trade-off between circuit parameters across different topologies, oscillators are no exceptions. This section presents the different parameters that trade-off with the oscillator phase noise.

### 5.2.1. Noise Sources

The spectral purity of the oscillator output waveform depends on the intrinsic noise generated within the oscillator. Generally, in a conventional LC oscillator, there are three main contributors to phase noise, as shown in Figure 1-17, which are the cross-coupled switching transistors  $M_1$  and  $M_2$ , the tail current source, and the thermal noise associated with the loss in the LC resonator.

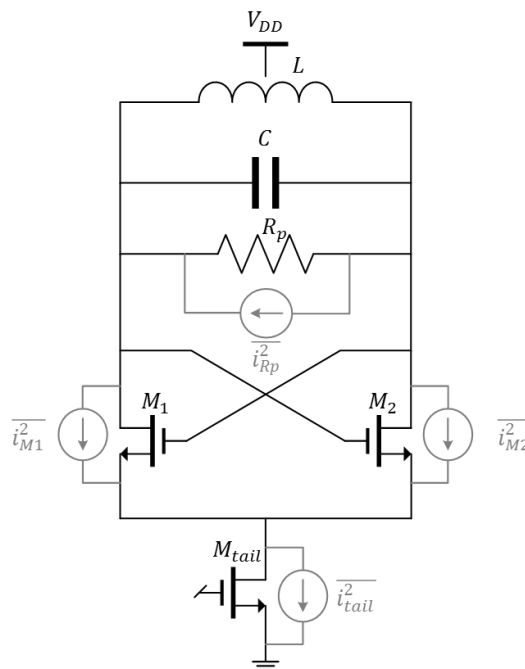


Figure 1-17: Noise sources in a cross-coupled LC oscillator.

#### Resonator noise

The energy loss in the LC tank, represented by the parallel resistance  $R_p$ , induces a thermal noise current, with a power density  $\overline{i_{Rp}^2}$ :

$$\overline{i_{Rp}^2} = 4k_B T \frac{1}{R_p} \Delta f \quad \text{Eq 1.15}$$

For a differential harmonic oscillator with a sinusoidal output, the ISF of the resonator noise is a sinusoid in quadrature with the tank voltage giving  $\Gamma_{rms}^2 = 1/8$  [10]. The phase noise generated by the thermal noise from  $R_p$  according to Eq (1.12) is:

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left( \frac{k_B T}{4V_0^2 C^2 R_p \Delta\omega^2} \right) = 10 \cdot \log \left[ \frac{k_B T}{4V_0^2} \cdot R_p \cdot \left( \frac{\omega_0}{Q_T \Delta\omega} \right)^2 \right] \quad \text{Eq 1.16}$$

The resonator's thermal noise contribution can be reduced by using passive elements with a high-quality factor  $Q$ . However, the maximum achievable  $Q_T$  is mainly determined by the characteristics of the technology and can only be slightly improved through design or layout techniques.

### Tail current noise

The noise at the tail transistor is translated up and down in frequency due to the switching of the commutations transistors. These transistors act as a self-balanced mixer that upconverts tail noise at  $\Delta\omega$  to  $\omega_0 \pm \Delta\omega$  and downconverts noise at  $2\omega_0 \pm \Delta\omega$  to  $\omega_0 \pm \Delta\omega$ . From these two transformations, only the downconverted noise at  $2\omega_0 \pm \Delta\omega$  causes phase fluctuation the other causes just amplitude fluctuation [11]. The phase noise from the tail current is expressed as:

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left[ \frac{2k_B T}{V_0^2 C^2 \Delta\omega^2} \cdot \Gamma_{tail,rms}^2 \cdot \gamma \cdot g_{m,tail} \right] \quad \text{Eq 1.17}$$

where  $\gamma$  is the noise factor of a transistor and  $g_{m,tail}$  is the transconductance of the tail transistor. The tail current provides a high impedance path when the transistor enters the triode region which prevents them from loading the tank. However, the overdrive voltage of the current tail transistor limits the oscillation output voltage which impacts the phase noise.

### Differential pair noise

The active device in the oscillator compensates for the losses in the LC tank by transferring the DC power supply to the resonator via periodical current pulses. In the process, the active device injects noise into the tank. This noise contribution inherits the periodicity of the active device, yielding a cyclostationarity noise. The expression of the effective ISF incorporates this cyclostationarity behavior [9]:

$$\Gamma_{eff}(\omega t) = \Gamma(\omega t) \alpha(\omega t) \quad \text{Eq 1.18}$$

where  $\alpha$  is the Noise Modulating Function (NMF) that represents the modulation of noise (cyclostationarity). The expression for the phase noise generated by the switches is:



$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left[ \frac{2k_B T}{V_0^2 C^2 \Delta\omega^2} \cdot \Gamma_{\text{eff,rms}}^2 \cdot \gamma \cdot \frac{g_m}{\lambda} \right] \quad \text{Eq 1.19}$$

where  $\gamma$  is the noise factor of the transistor and  $\lambda$  is the voltage gain between the tank and the switching transistors. The differential pair phase noise can be improved by increasing the gain  $\lambda$  or by reducing the effective ISF  $\Gamma_{\text{eff}}$ . This latter is reduced if the switching transistors turn on only during the short period where the oscillator is less sensitive to phase noise as indicated by the ISF. Thus, less noise will be converted to phase noise.

### 5.2.2. Power consumption

Consider the cross-coupled oscillator shown in Figure 1.18.a. The tail transistor  $M_{\text{tail}}$  sets the bias current  $I_{\text{bias}}$ . The transistors  $M_1$  and  $M_2$  compensate for the tank losses by injecting current into the tank. The resonator with reasonable quality factor  $Q$  filters all the current harmonics except the fundamental  $I_1$ . At the resonance frequency, the oscillator impedance is  $R_p$  since the L and C compensate for each other, thus the oscillator amplitude at  $\omega_0$  can be expressed by:

$$V_0 = \beta I_{\text{bias}} R_p \quad \text{Eq 1.20}$$

where

$$I_1 = \beta I_{\text{bias}} \quad \text{Eq 1.21}$$

and  $\beta$  is the current efficiency.

The amplitude affects the phase noise as emphasized in Eq (1.12). The phase noise is reduced by a slope of -20 dB/dec with an increase in  $V_0$ . On the other hand,  $V_0$  is linearly related to the bias current  $I_{\text{bias}}$ , as shown in Eq (1.20). Hence, an increase in the oscillator power consumption will improve the phase noise.

The reduction in phase noise is not indefinitely proportional to the power consumption. The linear growth of amplitude with bias current in equation (1.20) is valid only when the transistors are in saturation. For larger amplitude, the transistors are pushed into the triode region, which limits the value of the amplitude. Hence, LC oscillators exhibit two modes of operation, namely the current-limited region (M1 and M2 operate in saturation) and the voltage-limited region (M1 and M2 enter in the triode region), as shown in Figure 1-18.b. In the voltage-limited region, when the transistors enter the triode region, the parasitic tail capacitance  $C_{\text{tail}}$  adds its low-quality factor to the tank reducing the overall quality factor  $Q_T$ , as result the output phase noise increases. Therefore, for optimum phase noise, the oscillator

amplitude should be at the boundary between the current-limited and the voltage-limited regions.

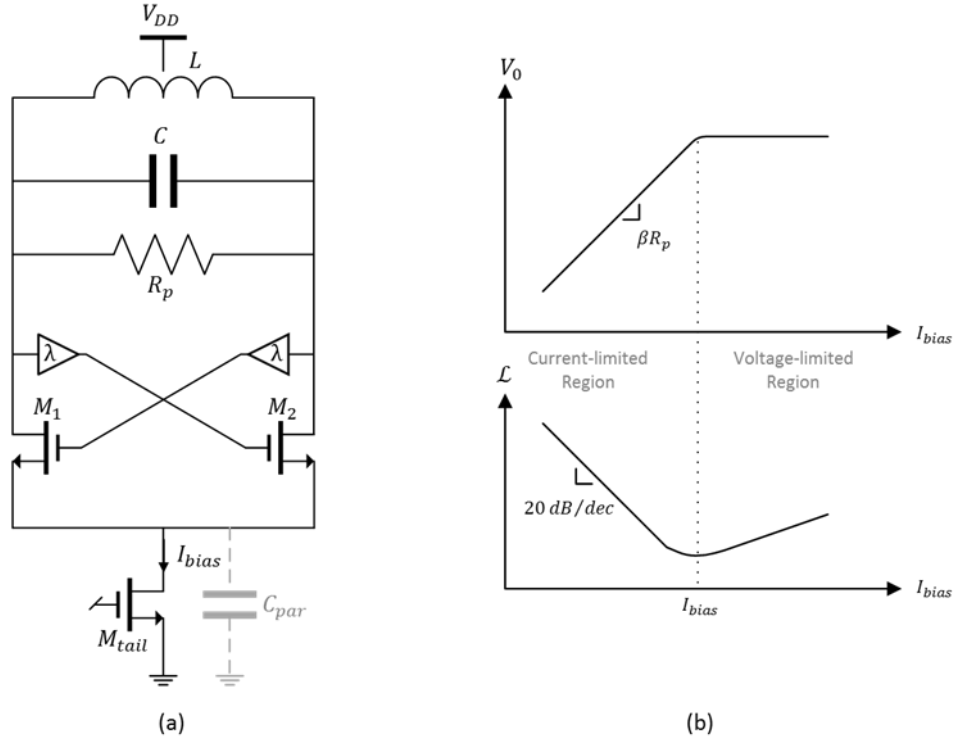


Figure 1-18: (a) Cross-coupled oscillator topology, (b) amplitude and phase noise of the oscillator in current-limited and voltage-limited regions.

In the current-limited region, the phase noise trades off with power consumption. This trade-off is evaluated in the oscillator by a Figure of Merit (FoM) defined as:

$$FoM = -\mathcal{L}(\Delta\omega) + 20 \log_{10} \left( \frac{\omega_0}{\Delta\omega} \right) - 10 \log_{10} P_{DC,mW} \quad \text{Eq 1.22}$$

Replacing Eq (1.13) in Eq (1.22),  $FoM$  becomes:

$$FoM = 10 \log_{10} \left[ \frac{2 \cdot Q_T^2 \cdot \eta_p}{R_p \sum \bar{i}_n^2 / \Delta f \cdot \Gamma_{n,rms}^2} \right] \quad \text{Eq 1.23}$$

where  $\eta_p$  is the power efficiency defined as:

$$\eta_p = \frac{P_{RF}}{P_{DC}} = \frac{I_{RF} V_{RF}}{I_{DC} V_{DC}} = \eta_I \eta_V \quad \text{Eq 1.24}$$

where  $P_{DC}$  is the DC power,  $P_{RF}$  is the RF power,  $I_{RF}$  and  $V_{RF}$  are the rms values of the fundamental components of current and voltage in the oscillator,  $V_{DC}$  and  $I_{DC}$  are the supply voltage and current. According to Eq (1.23)  $FoM$  is improved in three ways:

- Maximizing the tank quality factor  $Q_T$ , 6 dB of improvement for every doubling of it,

- Increasing the power transfer efficiency  $\eta_p$  from DC-to-RF, 3dB for every doubling of it,
- Reducing the oscillator ISF.

### 5.2.3. Frequency Tuning

Conventionally, a wide Frequency Tuning Range (FTR) in the oscillator is achieved by combining switching capacitors for coarse tuning and varactors for fine-tuning. The former covers the tuning range with discrete points by connecting/disconnecting fixed capacitors through a switching transistor, as shown in Figure 1-19. The varactors for fine-tuning connect the discrete points to provide continuous tuning on the FTR.

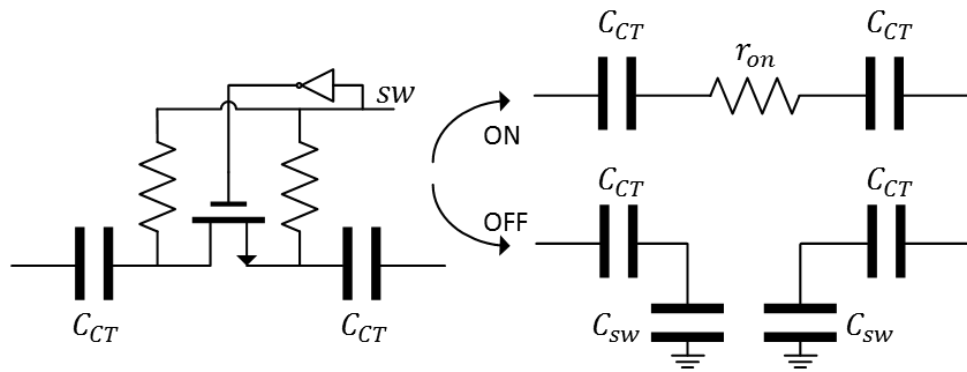


Figure 1-19: Switch capacitor model in ON and OFF state.

The minimum oscillation frequency is reached when all switches in the capacitor bank are turned on. The parasitic capacitance  $C_{p,AD}$  from the active device is also added up to the capacitor-bank capacitance  $C_{CT}$  and reduces the oscillation frequency.

$$f_{min} = \frac{1}{2\pi} \frac{1}{\sqrt{L(C_{CT} + C_{p,AD})}} \quad \text{Eq 1.25}$$

The switch capacitor quality factor  $Q_c$  is determined by the on-resistance  $r_{on}$  of the transistors:

$$Q_c = \frac{1}{\omega_0 C r_{on}} \quad \text{Eq 1.26}$$

where  $r_{on}$  can be expressed as:

$$r_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{th})} = \frac{r_{on,\mu m}}{W} \quad \text{Eq 1.27}$$

with

$$r_{on,\mu m} = \frac{L}{\mu_n C_{ox}(V_{gs} - V_{th})} \quad \text{Eq 1.28}$$

where,  $\mu_n$  is the mobility of the carrier,  $C_{ox}$  is the oxide capacitance,  $W$  is the width of the transistor,  $L$  is the length of the transistor,  $V_{gs}$  is the gate to source voltage, and  $V_{th}$  is the threshold voltage. Replacing Eq (1.27) in Eq (1.26) the capacitor quality factor becomes:

$$Q_c = \frac{W}{\omega_0 C r_{on,\mu m}} \quad \text{Eq 1.29}$$

The quality factor of the resonator is a parallel combination of the inductor quality factor  $Q_L$  and the capacitor-bank quality factor  $Q_c$ :

$$Q_T = \frac{Q_L Q_c}{Q_L + Q_c} \quad \text{Eq 1.30}$$

On the other hand, the maximum oscillation frequency is reached when all the switches of the capacitor bank are turned off. The tank capacitance, in this case, is composed of the active device's parasitic capacitance  $C_{p,AD}$  and the off-state capacitance  $C_{off}$  of the capacitor bank.

$$f_{max} = \frac{1}{2\pi} \frac{1}{\sqrt{L(C_{off} + C_{p,AD})}} \quad \text{Eq 1.31}$$

where

$$C_{off} = \frac{C_{CT} \cdot C_{sw}}{2C_{CT} + C_{sw}} \quad \text{Eq 1.32}$$

The on-resistance of the transistors in the capacitor-bank lowers the quality factor of the tank  $Q_T$ , thus degrading the phase noise. This effect is mitigated using large transistors as implied by Eq (1.29). In contrast, the parasitic capacitance of the transistor increases with its sized  $C_{sw} \propto W$ , thus reducing the maximum oscillation frequency as pointed out by Eq (1.31) and Eq (1.32). Consequently, the frequency tuning range trades off with the phase noise, i.e. capacitor bank quality factor  $Q_c$ .

Varactors also degrade the phase noise because they introduce AM-to-FM noise [12]. At millimeter frequencies, the quality factor of varactors is so low that it becomes the dominant quality factor compared to the inductor. Therefore, it is preferable to reduce the varactor capacitance and compensate for it with the switching capacitors.

The above discussion elucidates the trade-off between the oscillator phase noise and frequency tuning. This trade-off is evaluated in the oscillator by a tuning range-based figure of merit  $FOM_T$ , which is defined as:

$$FoM_T = -\mathcal{L}(\Delta\omega) + 20 \log_{10} \left( \frac{\omega_0}{\Delta\omega} \right) + 20 \log_{10} \left[ \frac{FTR(\%)}{10} \right] - 10 \log_{10} P_{DC,mW} \quad \text{Eq 1.33}$$

## 6. Oscillator topologies

The previous section presented the trade-offs between the oscillator parameters. These trade-offs are set by the oscillator topology. Thus, it is interesting to compare different oscillator topologies to determine the one with the better performance balance. The following subsections describe the common oscillator architectures. These oscillators are classified as power amplifiers.

### 6.1. Class-B

The class-B LC-tank oscillator (cf. Figure 1-20.a) is the most common implementation of harmonic oscillators due to its simplicity, relaxed start-up, and relatively good phase noise. The differential pair, composed of  $M_1$  and  $M_2$ , creates a negative resistance that compensates for the resonator losses modeled as  $R_p$ . The tail transistor  $M_{tail}$  sets the bias current of the oscillator  $I_{bias}$ . The latter flows through each switching transistor for a half period, producing a square wave current at their drain, as shown in Figure 1-20.b. The oscillation amplitude, as stated by Eq (1.20), is the product of the fundamental harmonic current  $I_1$  and the resonator impedance at the oscillation frequency  $R_p$ :

$$A_{class-B} = I_1 R_p = \frac{2}{\pi} I_{bias} R_p \quad \text{Eq 1.34}$$

The tail transistor operates in the saturated region presenting ideally a high impedance to the sources of  $M_1$  and  $M_2$ . This high impedance prevents the switching transistor from injecting noise and loading the tank when they enter the triode region near the amplitude peak. However, at the current transition,  $M_1$  and  $M_2$  work differentially presenting a virtual ground (low impedance) to their common source. Thus, the active device injects noise only at this moment, which unfortunately coincides with the ISF extremum, as depicted in Figure 1.20.b.

Moreover, the parasitic capacitor  $C_{par}$  of  $M_{tail}$  presents an RF path to the ground, distorting the current, and degrading the resonator quality factor when the transistors enter the triode region [13]. The oscillator current efficiency  $\eta_I$  is limited at  $\sqrt{2}/\pi$  to the square shape of the current and is even lower when the switching transistors enter the triode region. The voltage drop  $V_{ds,tail}$  that keeps  $M_{tail}$  in saturation, reduces the voltage efficiency  $\eta_V$ .

Increasing the width of  $M_{tail}$  improves  $\eta_I$  but also increases the transistor's transconductance, and consequently its noise injection into the tank Eq (1.17). Those effects degrade the theoretical ideal phase noise performance of the cross-coupled oscillator in a real implementation [13].

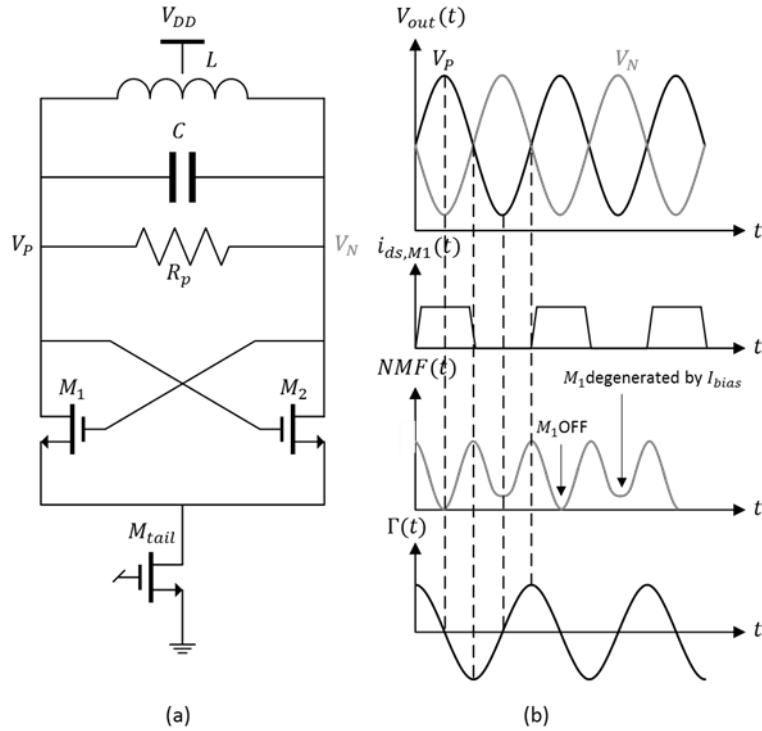


Figure 1-20: (a) Class-B oscillator topology, (b) differential output voltages, drain current of  $M_1$ ,  $i_{ds,M1}$ , noise modulating function (NMF) of  $M_1$  and ISF of  $M_1$ ,  $\Gamma$ .

The class-B can be improved by adding a noise tail filter (cf. Figure 1-21.a) as proposed in [14]. As discussed in section 5.2.1 only noise at  $2\omega_0$  in the tail current source contributes to phase noise. The inductor resonates with a parasitic capacitance at twice the oscillation frequency  $2\omega_0$ , thus filtering the tail current source noise. The tail inductor allows the oscillation amplitude to fall below the ground voltage, hence improving the voltage efficiency  $\eta_V$ . However, this technique requires an additional LC tank whose resonance frequency must be tuned with the oscillation frequency along the frequency tuning range. This increases the complexity and the area of the circuit.

The current efficiency can be improved by ac-coupling the switching transistors to the tank, as shown in Figure 1-21.b. The RC filter allows the bias voltage  $V_{bias}$  to be set lower than  $V_{DD}$ . This approach prevents  $M_1$  and  $M_2$  from entering the deep triode region. The

current efficiency  $\eta_I$  can be larger than  $\sqrt{2}/\pi$  because of the effect of the parasitic capacitance  $C_{par}$  that push the transistors in class-C partially [13].

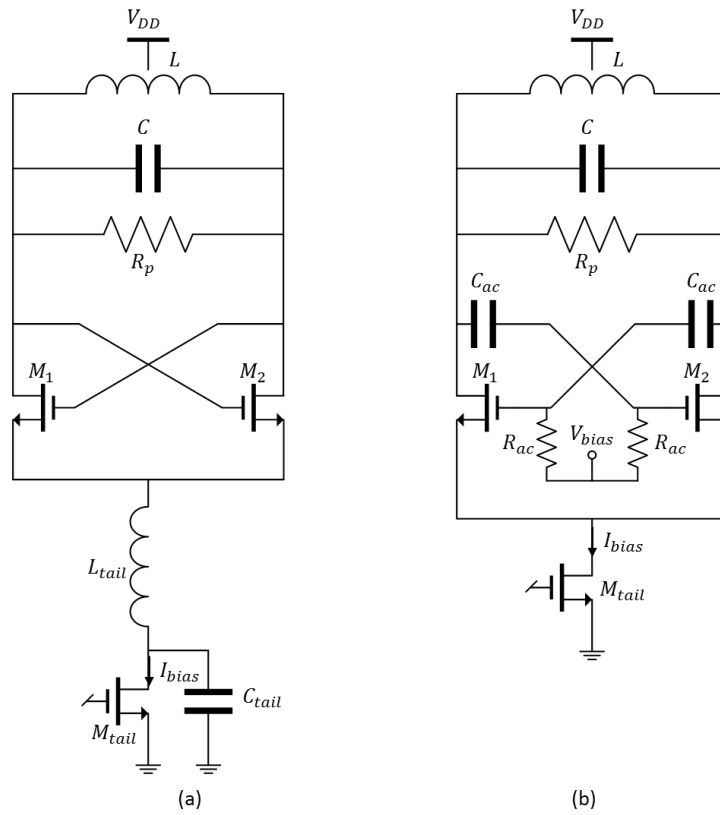


Figure 1-21: (a) Class-B oscillator with the tail filter, (b) class-B oscillator with ac-coupling.

## 6.2. Class-C

The class-C oscillator (cf. Figure 1-22.a) evolved from the combination of the class-B oscillator and the Colpitts differential oscillator [15]. The tail capacitor  $C_{tail}$  suppresses the sensitivity of the common source node to parasitic capacitance. In steady-state,  $C_{tail}$  increases the common source voltage, pushing the switching transistors to operate in a class-C, which produces a narrow and high drain current pulse (cf. Figure 1-22.b). The fundamental harmonic of the pulse current wave is larger than that of a square wave current. Thus, a class-C oscillator exhibits a better DC-to-RF power conversion than a class-B oscillator. The amplitude of the oscillation is expressed as [10]:

$$A_{class-c} = I_{bias} \left( 1 - \frac{\phi^2}{14} \right) R_p \quad \text{Eq 1.35}$$

with  $\Phi$  the half conduction angle. Considering that the class-B oscillator and the class-C oscillator have the same noise level, the phase noise ratio between the two topologies is expressed according to Eq (1.13) as:

$$\Delta\mathcal{L}(\Delta\omega) = 10 \log \left[ \left( \frac{A_{class-C}}{A_{class-B}} \right)^2 \right] \quad \text{Eq 1.36}$$

$$\Delta\mathcal{L}(\Delta\omega) = 10 \log \left[ \left( \frac{I_{bias} \left( 1 - \frac{1}{14} \Phi^2 \right) R_p}{\frac{2}{\pi} I_{bias} R_p} \right)^2 \right] \quad \text{Eq 1.37}$$

For  $\Phi = \pi/2$ , the class-c oscillator improves the phase noise by 2.2 dB compared to the class-B oscillator thanks to its higher efficiency. Class-C oscillator further improves the phase noise since the current source noise is filtered by the tail capacitor. Moreover, the pulse-like current peaks when the resonator is less sensitive to perturbation (cf. Figure 1-22.b). Therefore, the full potential of noise cyclostationarity is exploited to reduce the active device phase noise contribution.

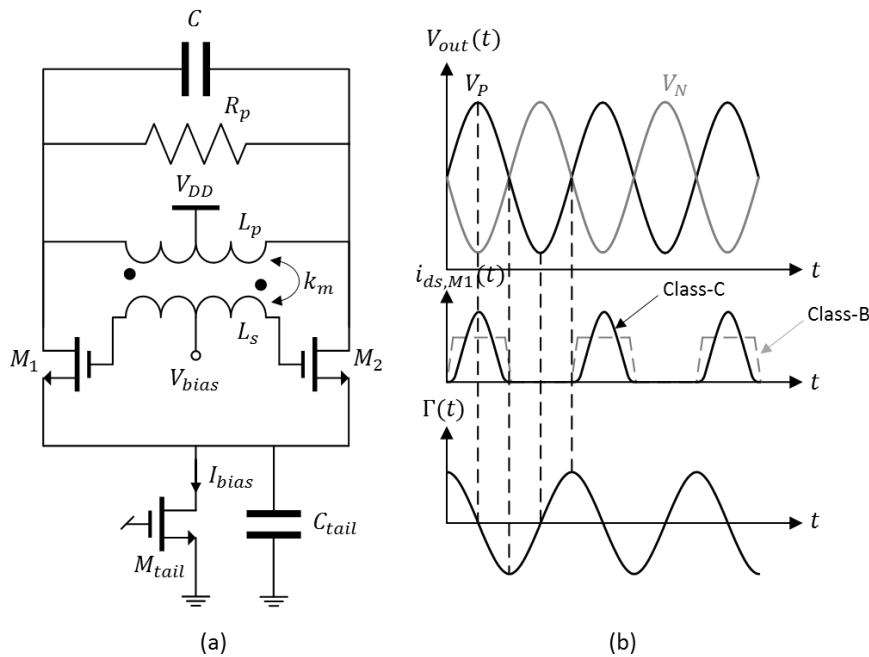


Figure 1-22: (a) Class-C oscillator topology, (b) differential output voltages, drain current of  $M_1$ ,  $i_{ds,M1}$ , and ISF of  $M_1$ ,  $\Gamma$ .

The class-C oscillator owes its good performance to the tail capacitor but also its limitations. The resonator becomes sensitive to the large capacitor loading when  $M_1$  and  $M_2$  enter the triode region, degrading the phase noise. Decreasing the DC voltage at the gate of  $M_1$  and  $M_2$  mitigates this effect. A transformer is used in Figure 1-22.a to decouple the DC



input of the switching transistor from its output, and allow the gate of  $M_1$  and  $M_2$  to be biased with a lower voltage than  $V_{DD}$ . The maximum usable oscillation amplitude  $A_{max}$  is defined as the amplitude where  $M_1$  and  $M_2$  are in the vicinity of the triode region [15]:

$$A_{Class-c} < A_{max} = \frac{V_{DD} - V_{od}}{1 + \lambda} \quad \text{Eq 1.38}$$

where  $\lambda$  is the transformer voltage gain,  $V_{od}$  is the overdrive voltage of  $M_{tail}$ ,  $V_{DD}$  is the supply voltage, and  $V_{bias}$  is the gate bias voltage of  $M_1$  and  $M_2$ . For  $\lambda = 1$  and  $V_{bias}$  close to  $V_{th}$ , the maximum voltage swing of a class-C oscillator is limited to  $V_{DD}/2$ . For a short-channel transistor, the limit is higher since a smaller drain voltage is needed to keep the transistor saturated [15]. The maximum voltage of the class-B oscillator is  $V_{DD} - V_{od}$ , with  $V_{od}$  being the overdrive voltage of the tail current. Hence, both oscillators achieve the same voltage swing (since  $V_{od}$  tends to be large to reduce the current source noise [13]). Nevertheless, the class-C oscillator is more efficient, which allows it to achieve a better FoM.

The start-up of class-C oscillators trades off with the maximum oscillation voltage. For robust and quick oscillation,  $V_{bias}$  should be set to  $V_{DD}$  but for a large oscillation swing  $V_{bias}$  should be small as Eq (1.38) implies. This trade-off is solved by dynamically adjusting  $V_{bias}$  (high at start-up and low in steady-state) through a feedback control [13], [16]–[18] or by using a hybrid topology between class-B and class-C oscillators [19].

### 6.3. Class-F

The square wave proved to have a special ISF [9]. The ISF is zero over the entire period, except when the signal goes from low to high value or vice versa. As a consequence, the noise has a smaller time window to be converted to phase noise. Class-F oscillators enforce a pseudo square wave by injecting a third harmonic into the fundamental oscillation (cf. Figure 1-23.b). This is done by introducing another impedance peak at  $3\omega_0$  to prevent the filtering of the third harmonic's drain current. M. Babaie *et al.* [20] use a transformer-based resonator that resonates at the fundamental frequency  $\omega_0$  and at the third harmonic  $3\omega_0$  (cf. Figure 1-23.a). The oscillating signal is expressed as:

$$V(t) = V_{p1} \sin(\omega_0 t) + V_{p3} \sin(3\omega_0 t + \Delta\phi) \quad \text{Eq 1.39}$$

The ISF RMS of the waveform such as Eq (1.39) is estimated for  $-\pi/8 < \Delta\phi < \pi/8$  by [20]:

$$\Gamma_{rms}^2 = \frac{1}{2} \frac{1 + 9\xi^2}{(1 + 3\xi)^2} \quad \text{Eq 1.40}$$

where  $\xi = V_{p3} / V_{p1}$  is the ratio between the third-to-first harmonic oscillation voltage. For  $\xi = 1/3$ ,  $\Gamma_{rms}^2$  reaches its minimum value, resulting in a 3 dB improvement in phase noise compared to other traditional oscillators. The sharper transition of the output signal leads the switching transistor to dissipate power for a smaller time window. Hence, the oscillator power efficiency is improved with the *FOM*.

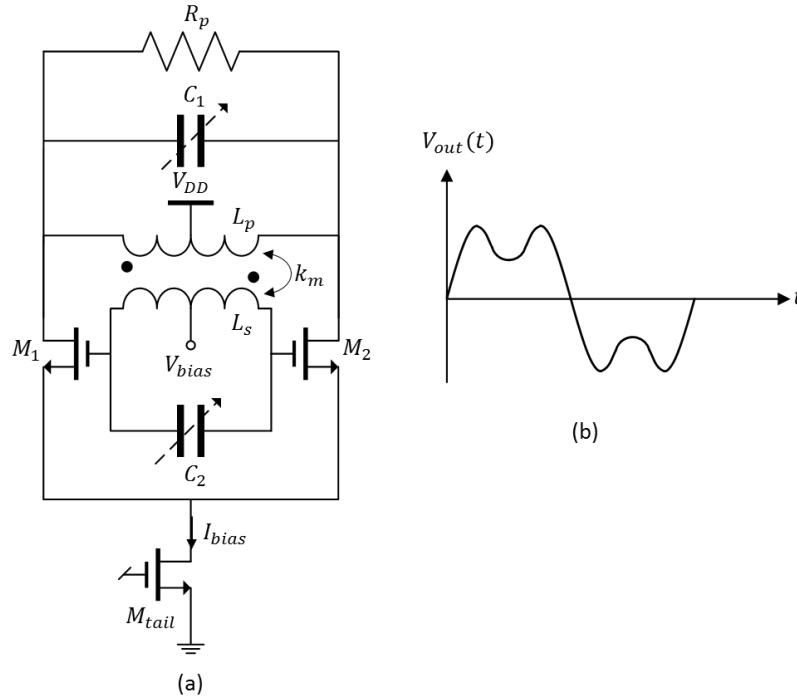


Figure 1-23: (a) Class-F oscillator topology, (b) output voltage waveform.

Other harmonics can be injected into the tank in a class-F to reshape the output signal. M. Shahmohammadi et al [21] proposed a class-F oscillator with an auxiliary resonance at 2<sup>nd</sup> harmonic  $2\omega_0$ . The oscillator exhibits a waveform with symmetric rise and fall time, as the 2<sup>nd</sup> harmonic of the current flows in a resistive path rather than the capacitive path. The signal symmetry reduces the DC coefficient of the ISF  $c_0$ , which attenuates the up conversion of flicker noise to  $1/f^3$  noise. Class-F oscillators with multiple harmonics have been also proposed [22], [23].

#### 6.4. Topologies comparison

The resonator quality factor  $Q_T$  has an important impact on the phase noise, and it is uniquely related to the process technology. The topology of the oscillator has a small to no

impact on the quality factor. Thus, to fairly compare oscillator topologies [24] proposed a figure of merit, called Excess Noise Factor (ENF), that excludes the quality factor and considers only topology-related parameters. The excess noise factor is defined as:

$$ENF = FOM_{Max} - FOM \quad \text{Eq 1.41}$$

where  $FOM_{max}$  is the thermodynamic limit associated with the noise and power dissipation of the unloaded tank.  $FOM_{max}$  is defined from Eq (1.23) assuming 100% power efficiency, noiseless tank and transistors, and no other noise contribution:

$$FOM_{Max} = 10 \log \left[ \frac{2 \cdot 10^{-3} Q_T^2}{k_B T} \right] = 173.8 \text{ dBc/Hz} + 10 \log(2Q_T^2) \quad \text{Eq 1.42}$$

Placing Eq (1.23) and Eq (1.42) in Eq (1.41) gives:

$$ENF = FOM_{Max} - FOM = 10 \log \left[ \frac{2(\Gamma_{Rp,rms}^2 + \Gamma_{M,rms}^2 \gamma)}{\eta_P} \right] \quad \text{Eq 1.43}$$

where  $\gamma$  is the transistor noise factor. The ENF defines the distance from the ultimate limit. To approach the highest achievable FoM, an oscillator topology should maximize power efficiency and reduce the ISF. Table 1-1 presents a comparison of the oscillator topologies with their corresponding ENF [24]. From the table, the class-B oscillator with tail filter and class-C oscillator stand out among other topologies to be more performant.

The main difference between the class-B and class-C oscillators is their efficiency. The class-C oscillator achieves the same phase noise level with 36% power saving compared to the class-B oscillator. The special ISF of class C improves the phase noise compare to class B. Moreover, the tail capacitance filters out the tail noise source in class-C. However, class-C trades off between robust start-up and high amplitude, requiring additional circuitry to deal with this trade-off. On the other hand, class-B oscillators have an inherited robust start-up and simple implementation. The tail filter class-B is one of the topologies with the highest  $FOM$  [24]. This performance is paid with an increase in chip area and high complexity for tail tank tuning. Class-F oscillators modified the output waveforms to manipulate the ISF. This results in low noise conversion to phase noise. Moreover, the sharp transition of class-F improves power efficiency. Nevertheless, The phase noise improvement in the class-F oscillator requires that the quality factor at the third harmonic  $Q_3$  is superior to the fundamental quality factor  $Q_1$  [24], a condition difficult to achieve which limits the use of class-F oscillators in real-life applications.

Oscillator type	$\eta_{I,max}$	$\eta_{V,max}$	$\eta_{p,max}$	$ENF_{min}$
Class-B	$\sqrt{2}/\pi$	$\sqrt{2}\left(1 - \frac{V_B}{V_{DD}}\right)$	$\frac{2}{\pi}\left(1 - \frac{V_B}{V_{DD}}\right)$	$\sim 10dB$
Class-B AC-Bias	$\sqrt{2}/\pi$	$\sqrt{2}\left(1 - \frac{V_B}{V_{DD}}\right)$	$\frac{2}{\pi}\left(1 - \frac{V_B}{V_{DD}}\right)$	$\sim 8.5dB$
Class-B AC-Bias LC-Filter	$\sqrt{2}/\pi$	$\frac{\pi}{\sqrt{2}}\left(1 - \frac{V_B}{V_{DD}}\right)$	$1 - \frac{V_B}{V_{DD}}$	$\sim 4.5dB$
Class-C	$1/2$	$1/\sqrt{2}$	$1/2$	$\sim 6dB$
Class-F	$\sqrt{2}/\pi$	$\frac{4\sqrt{2}}{\pi}\left(1 - \frac{V_B}{V_{DD}}\right)$	$\frac{8}{\pi^2}\left(1 - \frac{V_B}{V_{DD}}\right)$	$\sim 8.5dB$

Table 1-1: Efficiency comparison of oscillator topologies [24].

## 7. Conclusion

Satellite communications play a major role in the deployment of data services such as the internet and TV broadcasting throughout the world, even in remote areas. The new space democratizes access to space, which gives rise to new applications and financial opportunities. However, it also brings new challenges to transceiver design, especially to oscillators that must have high phase noise performance with low power and high reliability.

Harmonic oscillator performance is determined by its phase noise. This latter trade-off with power consumption, frequency tuning, and noise sources. In general cases, a high  $FoM$  is achieved by maximizing the resonator quality factor  $Q_T$  and the signal power, i.e, increasing the oscillating signal amplitude. The maximum achievable  $Q_T$  for passive components is mainly determined by technology limitations and can only be slightly improved by design or layout techniques. High amplitude can be achieved by increasing the current transfer efficiency from DC-to-RF. In addition to these two factors, the ISF proposed by Hajimiri and Lee's model can guide the choice of the oscillator topology for minimum phase noise.

The main oscillator's topologies were presented. Class-B with tail filter and class-C exhibit the highest  $FoM$ . However, class-B with a tail filter occupies more area and needs additional tuning for the tail tank. On the other hand, class C suffers from a trade-off between the amplitude and the start-up that limits its advantage. For our design, we selected the class-C topology due to its superior FoM and reduce complexity compared to the class-B with tail filter.

In the next chapter, we present our proposed class-C oscillator topology that comes as an evolution from the basic topology to our own with an in-depth discussion of phase noise and the reliability issues and mitigation techniques. The 28 nm FD-SOI CMOS technology used in this work is also presented.

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## Chapter 2:

# Transformer-coupled Class-C Oscillator with Long-Term Reliability and Adjustable Phase Noise

*This chapter introduces an overview of the 28 nm FD-SOI technology and presents the proposed oscillator topology based on the high oscillation class C oscillator and the transformer resonator. The reliability issues encountered in an LC oscillator are discussed and a proposed solution is given to improve the reliability of the circuit. The phase noise and transconductance of the proposed oscillator are analyzed theoretically and verified by simulation.*

### 1. 28 nm FD-SOI technology overview

Shrinking the transistor size is the dominant trend in the semiconductor industry, following Moore's law. However, at low nodes, such as 28nm, the CMOS bulk transistor encounters many bottlenecks that limit its performance. Two main mechanisms reduce drastically bulk device performance: leakage current, and variability [1]. As the bulk transistor is downsized, the channel is reduced, hence the control of the gate exercised over the channel region is reduced too, resulting in an unwanted leakage current flow even if the transistor is off. On the other hand, the channel formation is also subjected to the influence of drain voltage through drain-gate capacitance. At a low node, this capacitance becomes so important, that the drain terminal controls the channel formation alongside the gate terminal. With a drain connected to a high potential voltage, electrons flow and the channel starts to conduct, increasing the leakage current. The current leakage is mitigated in bulk CMOS by placing the source and drain terminals on doped silicon. Increasing the doping concentration reduces leakage current however the variability in the circuit increases.

These difficulties lead the semiconductor industry toward fully depleted architecture such as Fully Depleted Silicon on Insulator (FD-SOI) CMOS and Fin-FET CMOS devices. The latter exhibits a high-speed switching transistor suitable for digital applications, but its large parasitic capacitance limits its use in RF applications. In contrast, FD-SOI has lower parasitic capacitance and high-speed transistors compared to bulk technology. Thus, it is possible to



integrate both high-speed digital and RF components to take advantage of system-on-chip (SOC) integration and thus reduce the production costs of complex systems [2].

In this work, we used the 28 nm FD-SOI technology from ST Microelectronics. This section presents an overview of this technology.

### 1.1. Active devices

The 28 nm FD-SOI keeps the fundamental geometry of the transistor. An insulator layer of buried oxide was inserted under the channel as shown in Figure 2-1. The thin silicon layer (7 nm) enables the silicon under the transistor gate to be fully depleted of charges; therefore, it eliminates the random dopants fluctuation. By that, it decreases the variability and increases the matching between short-channel devices. The technology with very thin buried oxide is called Ultra-Thin Body and Buried Oxide (UTBB) [1].

The isolation of the channel by the buried oxide confines the electrons flowing from the source to the drain, as shown in Figure 2-2. Hence, it reduces the leakage current from the channel to the substrate. Moreover, the transistor benefit from total latch-up immunity.

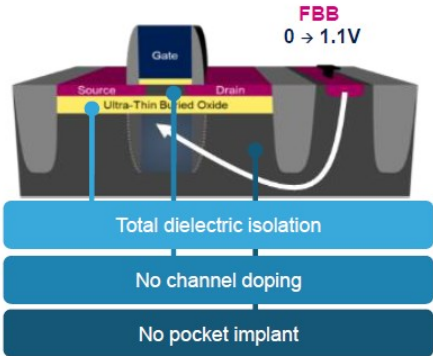


Figure 2-1: Cross-section of an UTBB FD-SOI transistor.

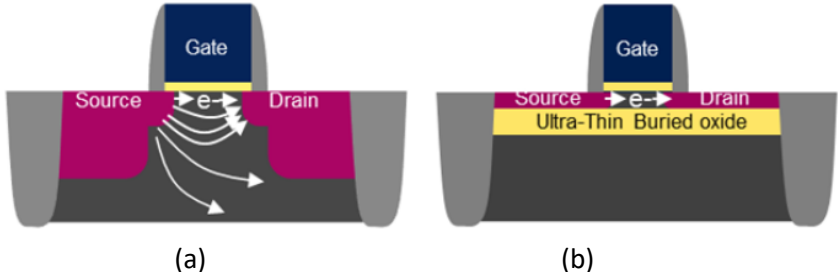


Figure 2-2: Electron flow (a) bulk technology (b) FD-SOI technology.

The 28 nm FD-SOI technology exhibits higher analog performances compared to its equivalent 28 nm LP bulk from ST Microelectronics. The FD-SOI has a smaller effective channel length compared to the bulk technology. Thus, the electrons' path flow is shorter

resulting in a faster transistor. Moreover, the current in FD-SOI is higher by a factor of 1.3-1.4 than that of bulk transistors [1]. Figures 2-3 and 2-4 present a comparison between 28 nm FD-SOI and 28 LP bulk analog performances. In Figure 2-3, the FD-SOI outperforms its bulk counterparts in terms of analog gain ( $g_m/g_{ds}$ ) and threshold voltage  $V_{th}$  matching parameter. Furthermore, FD-SOI transistors have lower parasitic capacitance and higher  $G_m$  for a given current compared to bulk technology (cf. Figure 2-4). Hence, FD-SOI achieves a higher gain-bandwidth product.

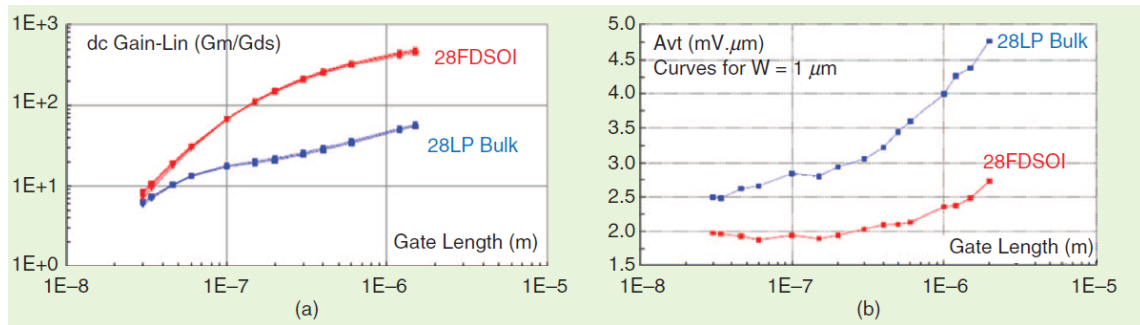


Figure 2-3: Comparison between 28-nm FD-SOI technology (red) and 28-nm LP bulk (blue) in (a) Analog gain ( $G_m/G_{ds}$ ) and (b) matching parameter ( $A_{vt}$ ) [3].

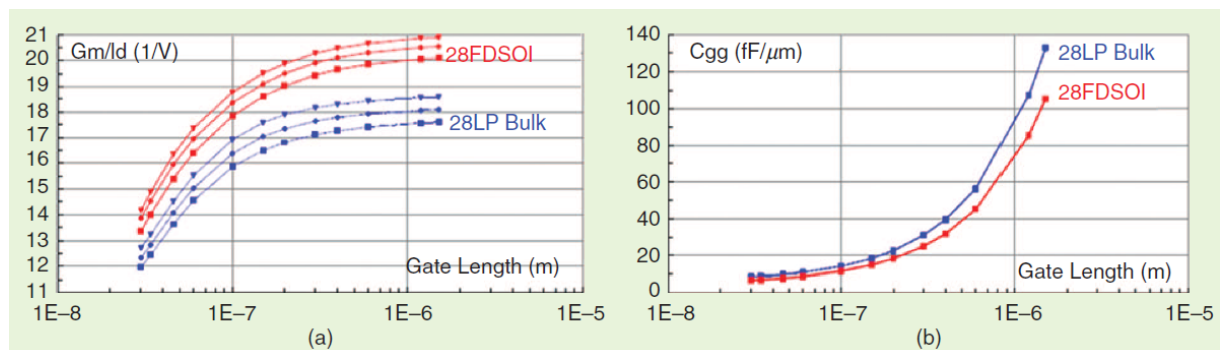


Figure 2-4: Comparison between 28-nm FD-SOI technology (red) and 28-nm LP bulk (blue) in (a) transconductance over drain current ( $G_m/I_d$ ) and (b) total gate capacitance ( $C_{gg}$ ) [3].

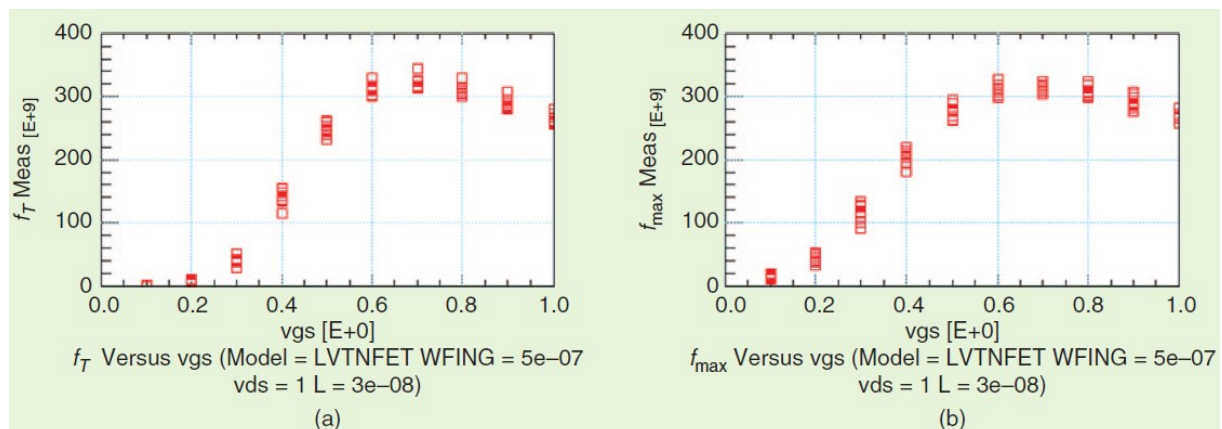


Figure 2-5:  $f_T$  and  $f_{max}$  of LVT NMOS  $0.5 \mu m/30 nm$  in 28-nm FD-SOI CMOS [3].

The 28 nm FD-SOI technology exhibits interesting RF and mmW features. For example, low  $V_T$  (LVT) NMOS transistors (Front-End-of-Line (FEOL) plus Metall contact) yield a transition frequency ( $f_T$ ) and a maximum frequency ( $f_{max}$ ) superior to 300 GHz, as shown in Figure 2-5 [3].

The transistors in 28 nm FD-SOI have two “flavors”: regular  $V_T$  (RVT) and low  $V_T$  (LVT). Figure 2-6 shows the two types of transistors. In RVT configuration, NMOS and PMOS transistors are implemented on a PWell and an NWell, respectively, as the regular implementation in bulk technology. In contrast, the LVT configuration, also called flip-well, place NMOS transistors on an NWell body, and PMOS on a PWell body. The technology also proposed transistors with thin and thick gate oxide.

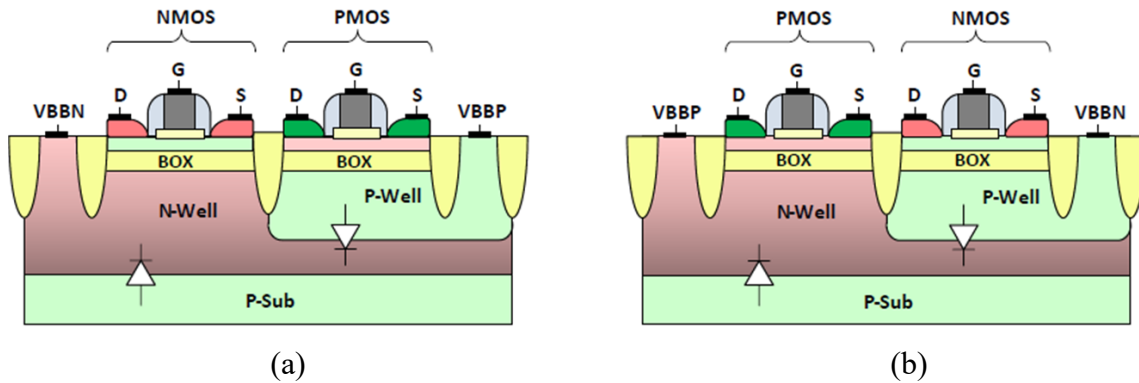


Figure 2-6: 28-nm UTBB FD-SOI CMOS transistors: (a) RVT transistors and (b) LVT transistors.

## 1.2. Body biasing

The flagship feature of the 28 nm FD-SOI technology is the wide body-biasing voltage range ( $-3 V < V_{BB} < 3 V$ ). The body biasing feature exists already in bulk CMOS however, its range is limited due to the junction diodes between the source/drain and the substrate. The typical voltage range for body biasing in bulk CMOS is  $0 < V_{BB} < 0.3 V$ . The buried oxide in FD-SOI technology suppresses the junction diodes of the source/drain to the substrate, which allows a large body biasing compared to bulk CMOS. The limiting factor in FD-SOI is the parasitic diodes between the deep NWell to substrate for NMOS and PWell to deep N-well for PMOS. These diodes turn on at a voltage of 3V (modulus) [2].

There are two types of body biasing: Forward Body Biasing (FBB) and Reverse Body Biasing (RBB). The forward and reverse bias ranges depend on the doping of the well in which the transistor is placed (i.e. transistor flavor). The FBB reduces the threshold

voltage  $V_{th}$ , while RBB increases  $V_{th}$ . Figure 3-7 sum-up the biasing configuration for each transistor flavor.

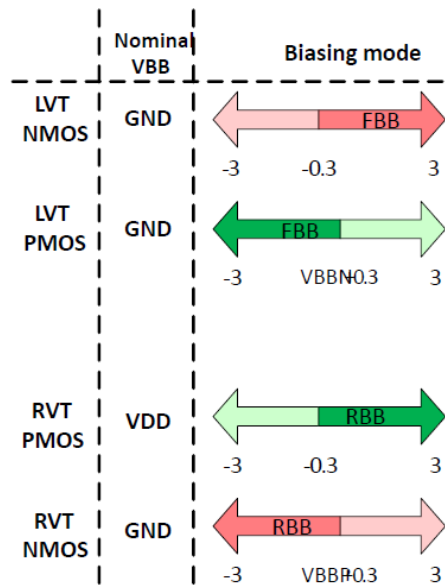


Figure 2-7: 28nm FD-SOI CMOS technology transistors body biasing mode, limits, and nominal voltage.

The 28 nm FD-SOI transistors have a large threshold voltage  $V_{th}$  variation (250 mV) compared to 28 nm LP bulk transistor (15 mV). Figure 2-8 depicts  $V_{th}$  variation in function of the body biasing for RVT and LVT transistor in 28 nm FD-SOI. The current leakage and transistor speed depend on the threshold voltage  $V_{th}$ . A low  $V_{th}$  increases the device speed but increases also the leakage current and vice versa. Thus, different  $V_{th}$  can be exploited to optimize the circuit for speed or low power according to the application.

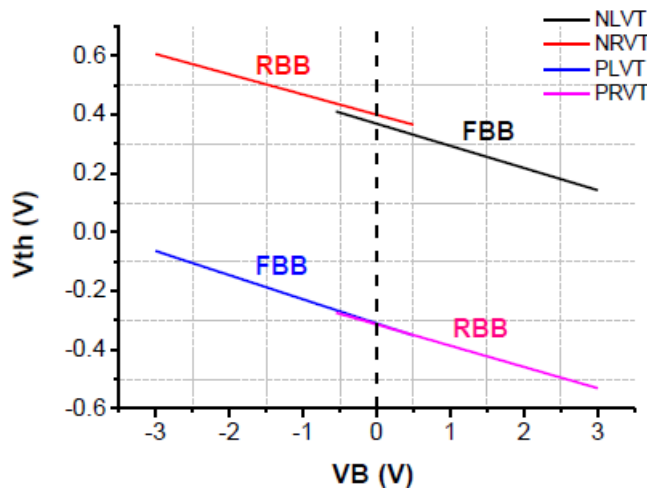


Figure 2-8:  $V_{th}$  variation range in function of body-biasing voltage for RVT and LVT devices in 28nm FD-SOI technology.

### 1.3. Back-End-Of-Line (BEOL)

The RF performances of a technology do not depend only on the transistors but also on the BEOL process and the quality factor of passive elements. The integration of high-quality passive elements such as inductors requires a higher number and thicker metal layers. The 28 nm FD-SOI technology has two BEOL: 8 metal layers (8ML) and 10 metal layers (10ML). The metal construction of 8ML BEOL is detailed as follows:

- 6 thin copper metal layers (M1 to M6).
- 2 thick copper metal layers (IA and IB).
- A thick aluminum metal layer (LB).

The thin metal layers are used only for digital routing. On the other hand, thick metal layers are suitable for high-frequency applications due to their low resistivity. The SOI allows the use of high resistive substrate which reduces the RF losses and crosstalk as was demonstrated in [4]. Thus, the passive elements like the inductors have an improved quality factor due to the high resistive substrate in SOI. The 10ML BEOL has two additional intermediate thick metal layers (B1 and B2), which are located between M6 and IA.

In this work, the circuits were designed on 8ML BEOL 28 nm FD-SOI technology. The 8ML BEOL structure is presented in Figure 2-9.

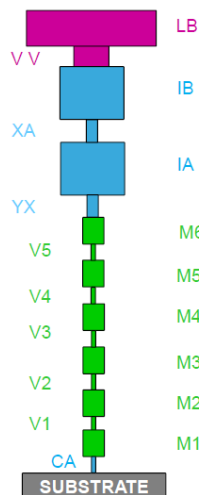


Figure 2-9: 8 metal layers back-end-of-line of 28nm FD-SOI technology.

### 1.4. Self-heating and radiation effects on 28nm FD-SOI

As the devices downsized, the current and power densities increase causing self-heating. The latter increases the transistor's temperature, resulting in an altered analog performance of

the device, such as threshold voltage shift, reduced mobility, and current degradation. Self-heating affects FD-SOI more than bulk CMOS [5]. The thin silicon film in 28 nm FD-SOI has lower thermal properties than bulk silicon. Moreover, the buried oxide reduces the Joule heat removal from the device channel to the substrate. Although the thermal effects are stronger in FD-SOI, it still outperforms bulk technology in a wide frequency range in terms of RF performances [5].

In space applications, the circuits are subject to cryogenic temperatures. In these temperatures, 28 nm FD-SOI transistors show an improvement in transconductance ( $g_m$ ), drain current  $I_d$ , and current gain cut-off frequency ( $f_T$ ). Figure 2-10 shows  $f_T$  and  $f_{max}$  as a function of the gate length at 300 K and 77 K for  $V_{ds} = 0.6 V$ . The technology exhibits  $f_t \sim 240$  GHz and  $f_{max} \sim 135$  GHz in the shortest device at 300 K with further improvement up to  $f_t \sim 323$  GHz and  $f_{max} \sim 150$  GHz at 77 K, proving the advantage of this technology for RF circuits in space applications [6].

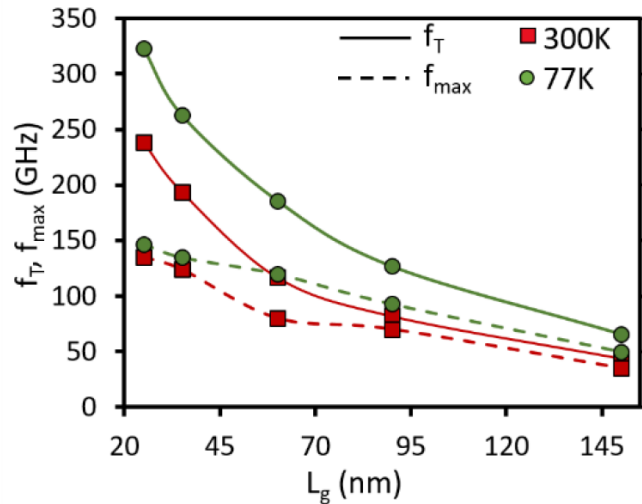


Figure 2-10:  $f_T$  and  $f_{max}$  in function of transistor length  $L_g$  for 77 K and 300 K in saturation at low- $V_{ds}$  ( $V_{ds} = 0.6 V$ ) and at  $V_{gs}$  that corresponds to maximum  $g_m$  [6].

In a space environment, high-energy radiation causes the charges to be stuck in the insulating oxides of the device. These trapped charges will produce electrical degradation that manifests in MOSFET devices as a negative threshold voltage shift, a subthreshold slope weakening, and an increase in leakage currents. Studies [7], [8] show that 28 nm FD-SOI is more resilient against radiation effects than bulk technology. The SOI reduces single-event effects by two orders compared to the bulk technology [7]. Moreover, 28 nm FD-SOI technology also performs well when exposed to an irradiative environment for a long term (up to 1 Mrad(Si)) [7]. However, some studies [7], [9]–[11] have outlined the fact that positive

charges are trapped in the thick oxide box due to radiation, which changes the electrical characteristics of the device. This electrical variation impact is limited with the use of thin oxide BOX [12], such as the 25 nm thickness used in the ST 28 nm FD-SOI technology. These advantages qualify 28 nm FD-SOI for space applications.

## 2. From high swing class-C oscillator to a class-C oscillator with long-term reliability and adjustable phase noise

In this section, we introduce the high-swing class-C oscillator which is the heart of our proposed topology. Then, we describe the transformer-based resonator operation with an analysis of the effect of transformer gain voltage on phase noise. We discuss the reliability issues encountered by an oscillator, before introducing the cascode oscillator that alleviates some of these issues. Finally, we present our proposed oscillator with a thorough analysis of its phase noise.

### 2.1. High swing class-C oscillator

Power efficiency optimization is the main factor to approach the maximum  $FoM$  for an oscillator as shown in Eq (1.43). The class-C oscillator has a higher current efficiency than the class-B oscillator due to the current in a pulse wave shape. However, the voltage efficiency is similar in both topologies. The output oscillation swing, for both topologies, is limited by two mechanisms: switching transistors entering the triode region at high voltage swings, and the overdrive voltage of the tail current sink. Figure 2-11 shows a high swing class-C oscillator proposed in [13]. This topology omits the current sink, which expands the voltage swing compared to the simple class-C. As a result, the voltage efficiency is improved.

The oscillation frequency is selected by a transformer-based resonator. The active device is composed of the transistors  $M_1$  and  $M_2$  compensate the losses of the resonator. These transistors operate in class C mode, which means that they have a conduction angle of less than  $180^\circ$ . The conduction angles of  $M_1$  and  $M_2$  is reduced by lowering their DC gate voltage. Thanks to the transformer, the DC gate voltage of  $M_1$  and  $M_2$  is isolated from  $V_{DD}$ , which allows it to be polarized with a lower voltage. The control circuit generates the bias voltage  $V_{ctrl}$  that bias the gates of  $M_1$  and  $M_2$ . The control circuit function as follow:  $M_1$  and  $M_2$  mirror the current flowing in the oscillator by a factor  $1/N$  where  $N$  is the mirror ratio. This current is then compared to the referential current  $I_{ref}$ . The difference between the two currents is integrated and converted by the capacitor  $C_b$  to a control voltage  $V_{ctrl}$ . This voltage

is fed to the gate of the switching transistors  $M_1$  and  $M_2$  to close the feedback loop. If the oscillator current image in the control circuit exceeds  $I_{ref}$ ,  $V_{ctrl}$  decreases to reduce the oscillator current. Inversely, when  $I_{ref}$  exceeds the mirrored current, more current flows in the capacitor  $C_b$ , consequently  $V_{ctrl}$  becomes larger and in return increases the current in the oscillator.

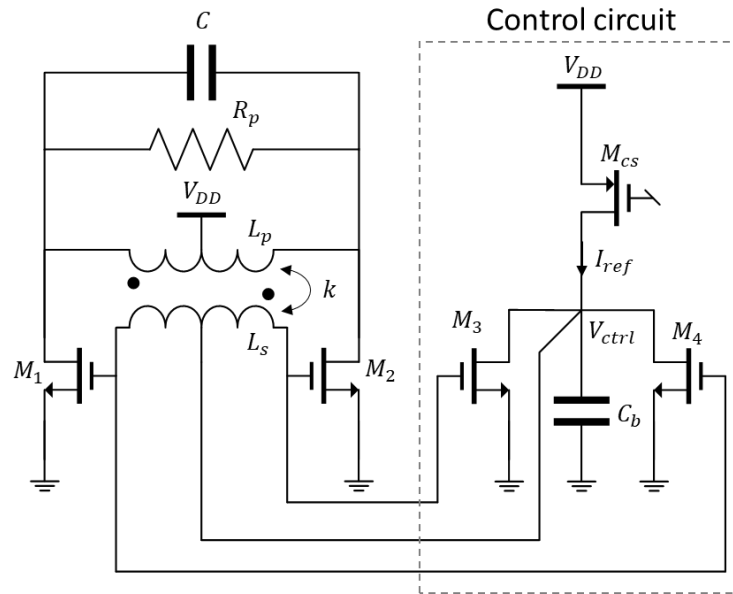


Figure 2-11: High swing class-C oscillator [13].

Another key role of the control circuit is to ensure a robust start-up. At the start-up, the secondary coil of the transformer  $L_s$  is shorted, thus  $M_3$  and  $M_4$  are diode-connected in DC, and they mirror  $I_{ref}$  with a ratio of  $N$  to  $M_1$  and  $M_2$ . As result,  $V_{ctrl}$  is set at a high voltage and the oscillation starts quickly providing that the current is sufficient to meet the Barkhausen criterion. In steady-state, the oscillator current stabilizes at  $NI_{ref}$  and the  $V_{ctrl}$  decreases to a lower voltage. The current  $I_{ref}$  control both the power consumption and the oscillation amplitude of the oscillator. Therefore, the control circuit solves the trade-off between robust start-up and maximum amplitude.

The output swing of the high-swing class-C oscillator reaches theoretically  $2V_{DD}$ . Although increasing the oscillation amplitude reduces the phase noise, at a certain threshold voltage -where the transistors enter the triode region - the amplitude has the opposite effect on phase noise as explained in chapter 1 section 5.2.2. Thus, the optimal maximum oscillation amplitude is reached when the switching transistors are at the edge of the triode region. Therefore, the maximum amplitude is defined when  $V_{gd1,2} = V_{th}$  by:



$$V_{gd} = V_g - V_d = (V_{ctrl} + \beta A_{max}) - (V_{DD} - A_{max}) = V_{th}$$

$$\Rightarrow A_{max} = \frac{V_{DD} - V_{ctrl} + V_{th}}{A_v + 1} \quad \text{Eq 2.1}$$

where  $A_v$  is the voltage gain of the transformer.  $V_{ctrl}$  value depends on the transistors size and the reference current  $I_{ref}$ .  $V_{ctrl}$  can be set as low as an overdrive by properly sizing the transistors  $M_3$  and  $M_4$ . Comparing Eq (2.1) and Eq (1.38) the maximum amplitude is improved in the high-swing class-C compared to the conventional class-C by  $V_{th}/(1 + A_v)$ . Therefore, the power voltage efficiency (i.e. power efficiency) in high swing class-C is higher. Furthermore, the absence of the tail current sink improves the phase noise. We select this topology as the base for our oscillator topology due to its high voltage efficiency.

### 2.1.1. Transformer-based resonator

Figure 2-12 presents the transformer-based resonator. The transformer consists of two inductance coils  $L_p$  and  $L_s$ , that are magnetically coupled with a coupling coefficient  $k$ . The capacitors  $C_p$  and  $C_s$  load the primary and the secondary coils of the transformer respectively. The series resistances  $R_{sp}$  and  $R_{ss}$  represent the losses of the coils. The transformer is described by the following impedance matrix:

$$Z_m = \begin{bmatrix} R_{sp} + j\omega L_p & j\omega k \sqrt{L_p L_s} \\ j\omega k \sqrt{L_p L_s} & R_{ss} + j\omega L_s \end{bmatrix} \quad \text{Eq 2.2}$$

The two-port transformer-based resonator impedance matrix is given by [14]:

$$Z = \frac{1}{1 - \omega^2 C_s C_p \det Z_m + j\omega (C_p Z_{m11} + C_s Z_{m22})} \cdot \begin{bmatrix} Z_{m11} + j\omega C_s \det Z_m & Z_{m12} \\ Z_{m12} & Z_{m22} + j\omega C_p \det Z_m \end{bmatrix} \quad \text{Eq 2.3}$$

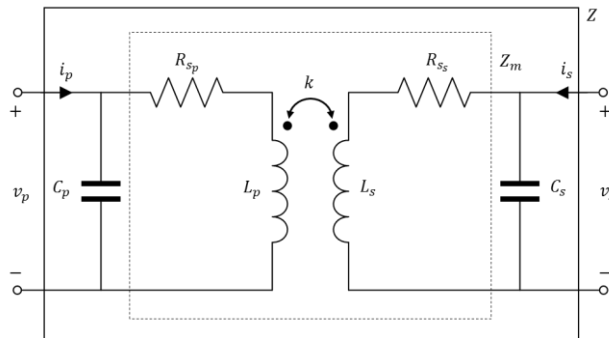


Figure 2-12: Transformer-based resonator.

The transformer can be used as a resonator in two configurations: one port or two port configuration as illustrated in Figure 2-13. In one-port configuration (cf. Figure 2-13.a), a negative conductance  $-G_m$  is connected to one port, to compensate for the resonator losses. In the two-port configuration (cf. Figure 2-13.b), a transconductor in a feedback loop compensates for the resonator's losses. The two-port configuration was used in the high swing class-C oscillator and our topology because it's immune to multi-resonance as we will discuss later. Therefore, we will consider only the two-port configuration. The start-up condition for a two-port configuration is expressed as [14]:

$$1 + G_m \Re\{Z_{12}\} < 0 \quad \text{Eq 2.4}$$

$$\Im\{Z_{12}\} = 0 \quad \text{Eq 2.5}$$

Eq (2.5) gives two possible resonance frequencies  $\omega_L$  and  $\omega_H$ . These two resonance frequencies are expressed as [14]:

$$\omega_{L,H}^2 = \frac{1 + \xi \mp \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{2(1 - k^2)} \omega_s^2 \quad \text{Eq 2.6}$$

where  $\omega_p^2 = 1 / (L_p C_p)$ ,  $\omega_s^2 = 1 / (L_s C_s)$ ,  $k$  is the coefficient of the magnetic coupling and  $\xi = (\omega_p / \omega_s)^2$ .

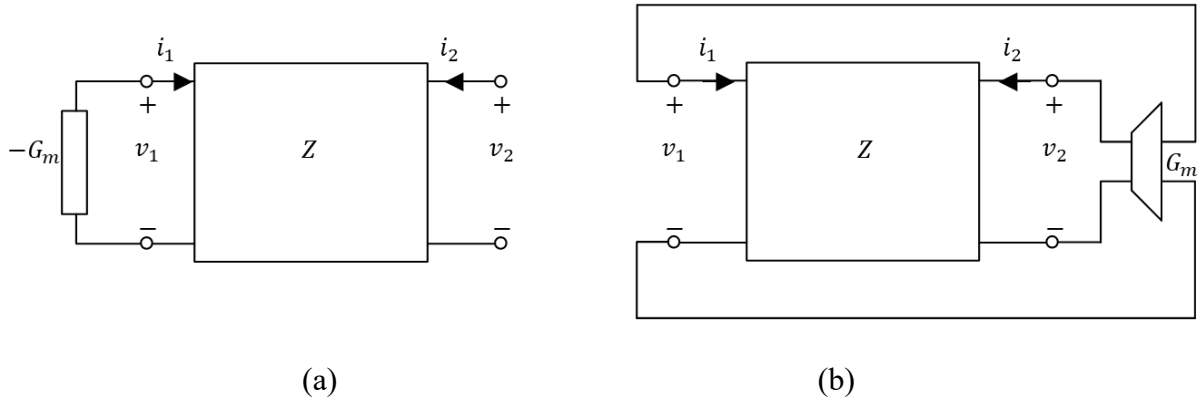


Figure 2-13: (a) One-port oscillator. (b) Two-port oscillator.

With two resonance frequencies, the risk of multi-resonance arises. In the two-port configuration, the feedback loop selects one oscillation frequency from the two possible frequencies. Eq (2.4) derives the transconductance required to start and maintain the oscillation as:

$$G_m = -G_{tank} = \frac{\omega}{\omega_s} \cdot \frac{\left[ \left( \frac{\omega}{\omega_p} \right)^2 - 1 \right] \frac{1}{Q_s} + \left[ \left( \frac{\omega}{\omega_s} \right)^2 - 1 \right] \frac{1}{\xi Q_p}}{\omega_s k \sqrt{L_p L_s}} \quad \text{Eq 2.7}$$

What stands out from the equation is the dependence of the transconductance's sign on the resonance frequencies  $\omega_L$  and  $\omega_H$ . Knowing that  $\omega_L < \{\omega_p, \omega_p\} < \omega_H$ ,  $G_m$  is negative for  $\omega = \omega_L$  and in contrast for  $\omega = \omega_H$   $G_m$  is positive. This result can be interpreted as follow, a positive feedback loop generates oscillation at  $\omega_L$ , and a negative feedback loop generates oscillation at  $\omega_H$ . Thus, the two-port configuration is immune to multi-oscillation behavior.

The quality factor of the resonator is related to the resonance frequency selected. Therefore, the choice between  $\omega_L$  and  $\omega_H$  is determined by analyzing their corresponding resonator quality factor. The quality factor of the transformer-based resonator is expressed as follows [15], [16]

$$Q = \frac{\omega_{L,H}}{2} \left| \frac{d}{d\omega} \ln Z_{12} \right| \quad \text{Eq 2.8}$$

giving

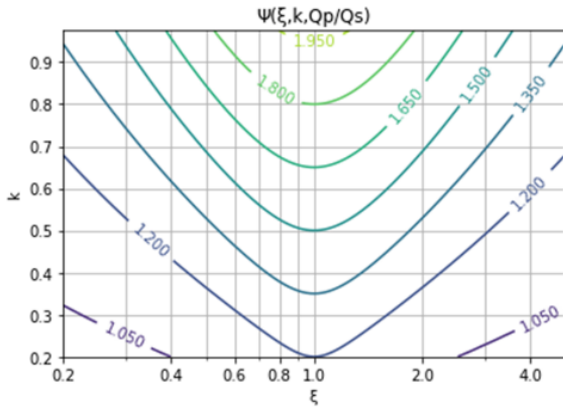
$$Q \approx Q_p \frac{[4\Omega_{L,H}^4(1-k^2) - \Omega_{L,H}^2(1+\xi)][\Omega_{L,H}^2(1-k^2) - 1]}{\xi \left[ \Omega_{L,H}^4 \left( 1 + \frac{Q_p}{Q_s} k^2 \right) - 2\Omega_{L,H}^2 + 1 \right]} \quad \text{Eq 2.9}$$

$$Q = Q_p \cdot \Psi(\xi, k, Q_p/Q_s) \quad \text{Eq 2.10}$$

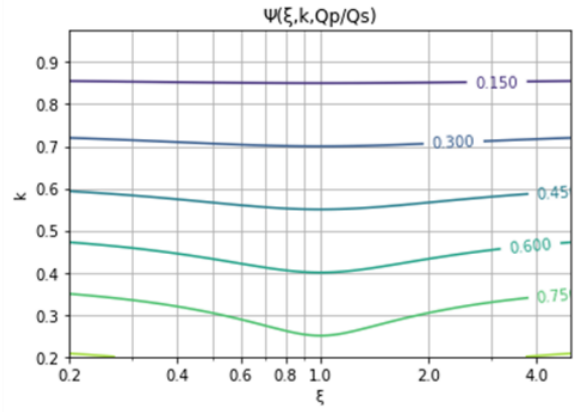
where  $Q_p$  and  $Q_s$  are the quality factor of the primary and secondary winding, respectively and

$$\Omega_{L,H}^2 = \frac{1 + \xi \mp \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{2(1 - k^2)} \quad \text{Eq 2.11}$$

The resonator quality factor depends on the magnetic coupling factor  $k$ ,  $\xi$ , and the quality factor  $Q_s$  and  $Q_p$ . Figures 2-14, 2-15, and 2-16 depict the function  $\Psi(\xi, k, Q_p/Q_s)$  for the low and high frequency  $\omega_L$  and  $\omega_H$  respectively for different values of  $Q_p/Q_s$ . In all three cases, the quality factor in  $\omega_L$  is higher than in  $\omega_H$ . Also, the magnetic coupling factor  $k$  has an opposite effect on the two resonance frequencies. In  $\omega_L$ , the resonator quality factor increases as the magnetic coupling  $k$  increases, while in  $\omega_H$  the quality factor decreases as  $k$  increases. As for  $\xi$ , its optimal value depends on the ratio  $Q_p/Q_s$ . When  $Q_p = Q_s$ ,  $Q$  is maximized for  $\xi = 1$  over all values of  $k$ , as shown in Figure 2-14. In the case where  $Q_p < Q_s$ ,  $Q$  is maximized for  $\xi > 1$ , as shown in Figure 2-15 for  $Q_p/Q_s = 1/2$ . In contrast, for  $Q_p > Q_s$ , the maximum  $Q$  is reached for  $\xi < 1$ , as depicted in Figure 2-16 for  $Q_p/Q_s = 2$ . In general,  $Q$  is maximized if the resonant frequency  $\omega_s$  or  $\omega_p$  of the winding with the lowest quality factor is pushed high.

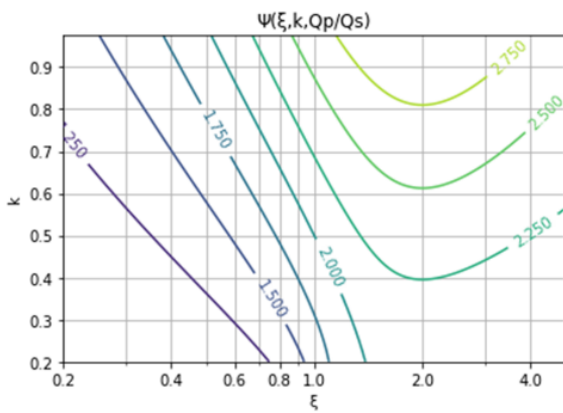


(a)

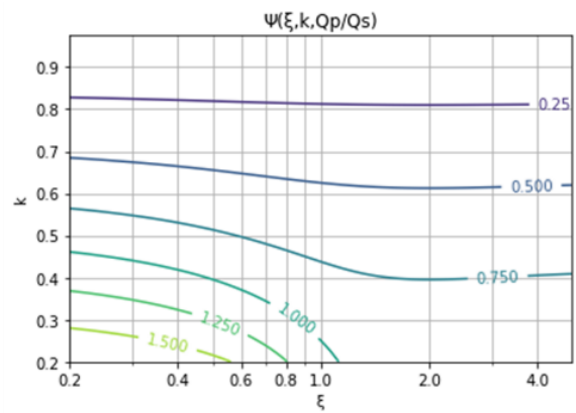


(b)

Figure 2-14:  $\Psi(\xi, k, Q_p/Q_s)$  in the case of  $Q_p = Q_s$  for (a)  $\omega_L$  and (b)  $\omega_H$

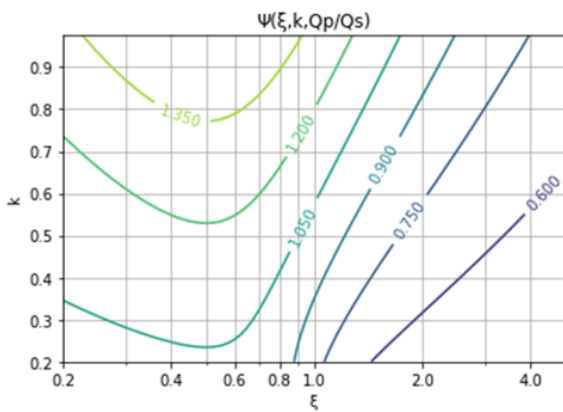


(a)

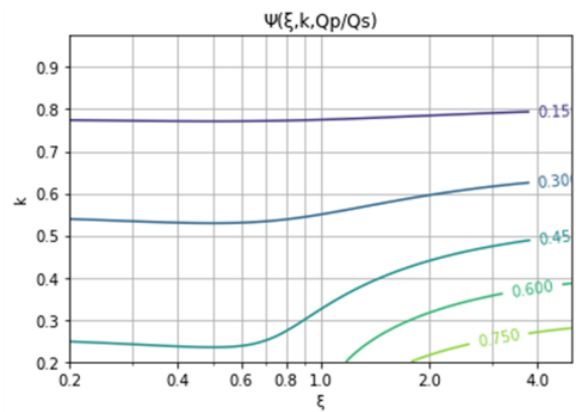


(b)

Figure 2-15:  $\Psi(\xi, k, Q_p/Q_s)$  in the case of  $Q_p < Q_s$  for (a)  $\omega_L$  and (b)  $\omega_H$



(a)



(b)

Figure 2-16:  $\Psi(\xi, k, Q_p/Q_s)$  in the case of  $Q_p > Q_s$  for (a)  $\omega_L$  and (b)  $\omega_H$

The transformer-based resonator reduces the noise of the active device by introducing a gain voltage  $A_v$  between the tank and the active devices, as shown in Eq (1.19). However, increasing the voltage gain causes the switching transistors to enter earlier in the triode region

due to the larger swing. Therefore, the maximum amplitude is reduced (cf. Eq (2.1)). Consequently, the voltage efficiency trades off with noise reduction. The following paragraphs present an analysis of the optimal voltage gain  $A_v$  that considers this trade-off.

In a class-C VCO, the current in switching transistors has a pulse shape, so the fundamental harmonic in the current tank is approximately equal to the bias current. Hence, the power efficiency  $\eta_p = \eta_v / \sqrt{2}$  since  $\eta_I \approx 1/\sqrt{2}$ . With a reasonable assumption of  $\Gamma_{rms}^2 \approx 1/2$  [17], [18] Eq (1.43) gives:

$$ENF = 10 \log \left[ \frac{1 + \frac{\gamma}{A_v}}{\eta_p} \right] = 10 \log \left[ \frac{1 + \frac{\gamma}{A_v}}{\eta_v / \sqrt{2}} \right] \text{ with } \eta_v = \frac{V_{RF}}{V_{DC}} = \frac{A_{max}}{V_{DD}} \quad \text{Eq 2.12}$$

Replacing  $A_{max}$  by Eq (2.1) gives:

$$ENF = 10 \log \left[ \frac{\sqrt{2} V_{DD} (A_v + 1) \left(1 + \frac{\gamma}{A_v}\right)}{A_v (V_{DD} - V_{ctrl} + V_{th})} \right] \quad \text{Eq 2.13}$$

The  $ENF$  has a minimum for  $A_v$  that is calculated as follows:

$$\begin{aligned} \frac{dENF}{dA_v} = 0 &\Rightarrow \frac{10}{\ln(10)} \frac{A_v^2 - \gamma}{A_v + A_v(\gamma + 1) + A_v} = 0 \\ &\Rightarrow \begin{cases} A_v^2 - \gamma = 0 \\ A_v > 0 \end{cases} \Rightarrow A_v = \sqrt{\gamma} \end{aligned} \quad \text{Eq 2.14}$$

The optimal voltage gain value  $A_v = \sqrt{\gamma}$  gives the minimum  $ENF$  (i.e maximum  $FoM$ ). On the other hand, the excess noise  $\gamma$  is superior to 1 for transistors with a length below 1.7  $\mu\text{m}$ . In [19], excess thermal noise is measured around 2.2 for 0.25  $\mu\text{m}$  MOSFETs based on the hydrodynamic formulation. Thus, for  $\gamma = 2.2$  the optimum gain voltage is equal to  $A_v \approx 1.48$ .

### 2.1.2. Reliability issues

The oscillation voltage swing is centered at  $V_{DD}$ , thus it exceeds the nominal supply voltage. This voltage applies a large electric field on the gate oxide, which causes reliability issues. The quest for high swing voltage in oscillators must take into account the reliability issues that arise.

There are four main mechanisms responsible for circuit unreliability [20]: Negative Bias Temperature Instability (NBTI), Hot Carrier Injection (HCI), Time-dependent dielectric

breakdown (TDDB), and electromigration. NBTI occurs when a negative voltage is applied to the transistor's gate-source voltage  $V_{gs}$ . NBTI induces a threshold voltage shift and degradation on carrier mobility. This phenomenon affect PMOS transistors in particular, as NMOS transistors are off at a negative  $V_{gs}$  [21]. Thus, NMOS transistors are preferred for long-operating time applications like satellite communications. Electromigration is the displacement of atoms in a conductor due to a high current density. This causes empty regions (open circuit) and regions with crowded atoms that can create a short circuit with the adjacent metal line. Electromigration is the main cause of interconnect failure and is avoided by widening the connection with a high current and increasing the number of the via. HCI and TDDB are related to the electrical fields applied across the transistor. These two mechanisms are the main limitations of the maximum amplitude.

The HCI occurs when a large lateral electrical field (drain to source) gives high kinetic energy to the carriers until they become "hot". Some "lucky" ones among these hot carriers gain sufficient energy to overcome the silicon-oxide barrier and get trapped in the insulator. These defects degrade the carrier mobility and shift the transistor threshold voltage. The effects of HCI accumulate over the life of the circuit, causing circuit aging and irreversible degradations that may lead to circuit failure. In RF circuits, such as oscillators, the  $G_m$  must be oversized to account for the HCI degradation over time. Increasing the  $G_m$ , increases also the noise, as shown in eq (2.49). The "lucky electron" model quantifies the HCI effects as the number of generated interface states  $\Delta N_{IT}$  [20]:

$$\Delta N_{IT} = C_1 \left[ \frac{I_{DS}}{W} \exp\left(-\frac{\phi_{IT,e}}{q\lambda_e E_{lat}}\right) T_{str} \right]^n \quad \text{Eq 2.15}$$

where  $C_1$  and  $n$  are process-dependent constants,  $W$  is the transistor width,  $I_{ds}$  is the drain-source current,  $E_{lat}$  is the peak lateral field at the drain,  $T_{str}$  is the stress time,  $\lambda_e$  is the hot-electron mean-free path, and  $\phi_{IT,e}$  is the critical energy for electrons to create an interface trap. The most important parameter in eq (2.15) is  $E_{lat}$ . The latter is expressed in [22] as:

$$E_{lat} = \frac{V_{ds} - V_{dsat}}{\sqrt{3}t_{tox}x_j} \quad \text{Eq 2.16}$$

where  $V_{ds}$  is the drain-source voltage of the transistor,  $V_{dsat}$  is the potential at the pinch-off,  $t_{ox}$  is the gate oxide thickness and  $x_j$  is the drain-junction depth. From Eq (2.15) and Eq (2.16), we deduce that  $V_{ds}$  is a significant contributory factor to the development of HCI ( $\Delta N_{IT} \propto 1 / V_{ds}$ ). Therefore, high swing voltage worsens the HCI effects.

Oxide breakdown occurs when a conduction path is formed through the gate oxide, leading the gate oxide to lose its insulating properties. At a high electrical field, impact ionization, anode hole injection, and trap creation phenomena generate defects in random positions inside the oxide until a percolation path is formed that results in the gate oxide breakdown. At a low electric field, the oxide slowly wears out over time until it breaks down. This is called time-dependent dielectric breakdown (TDDB). The breakdown is a stochastic phenomenon described by the Weibull probability distribution as:

$$F = 1 - e^{-(T_{BD}/\eta)^\beta} \quad \text{Eq 2.17}$$

where  $F$  is cumulative failure probability and  $T_{BD}$  is a random variable for time-to-breakdown,  $\beta$  is Weibull slope and  $\eta$  is the characteristic  $T_{BD}$  at  $F = 63\%$ . Both  $\beta$  and  $\eta$  are experimental parameters. Maricau et al [20] show that the breakdown of thin oxides (< 5nm of thickness) follows a power-law voltage dependence rather than an exponential dependence. The breakdown time in this model is expressed as:

$$T_{BD} \propto V_{gs}^{n(T)} \quad \text{Eq 2.18}$$

where  $n(T)$  is the voltage acceleration factor, which varies with the temperature  $T$ . TDDB depends on the stress time and the voltage across the gate. High voltage and longer time exposure cause defects.

In summary, the high swing class-C exhibits a high voltage efficiency and good noise performance compared to a simple class-C. The transformer-based resonator with a step-up transformer improves the oscillator performances for a voltage gain  $\beta \approx 1,5$ . However, the large voltage swing leads to oscillator reliability issues such as HCI and TDDB. Thus, the amplitude (and by dependence on the phase noise) trades off with reliability. In the next section, we will introduce our proposed oscillator that tackles the reliability issues in the high swing class-C oscillator.

## 2.2. A class-C oscillator with long-term reliability and adjustable phase noise.

### 2.2.1. Cascode class-C oscillator

In advanced CMOS technologies, circuit reliability needs to be ensured through circuit design, by taking into account the impact of a failure at the circuit level, especially for space applications such as satellite communications.

In oscillators, HCI and TDDB are the critical failure mechanisms [23], [24]. As explained earlier, these phenomena depend on the electrical field applied to the transistors (i.e. the oscillation amplitude). Thus, by reducing the electric field stress we can improve the oscillator's reliability. On the other hand, D. Chang et al [25] show that the reliability hotspot in the LC oscillator is the tail transistor. Indeed, a reduction of the tail current leads to a decrease in the amplitude, and thus a degradation of the phase noise. In high swing class-C (cf. Figure 2-11), the transistors  $M_1$  and  $M_2$  regulate the oscillator current through the control circuit. As consequence, the performances of high swing class-C oscillator are sensitive to  $M_1$  and  $M_2$  degradation.

Figure 2-17 presents a high-swing class-C oscillator with an active cascode device. The cascode structure splits the lateral electric field stress into two transistors. As a result, it mitigates the generation of hot carriers. Moreover, the TDDB of FD-SOI transistors is also improved in the cascode structure. Measurement data [26] show that the TDDB, in short-channel NMOS FD-SOI transistors, is degraded with an increased drain voltage  $V_d$ . Thus, reducing the  $V_{ds}$  voltage reduces the electrical field stress on the oxide of  $M_1$  and  $M_2$  transistors, improving the TDDB. Furthermore, the use of NMOS transistors immunizes the circuit against the NBTI as it mainly affects PMOS transistors.

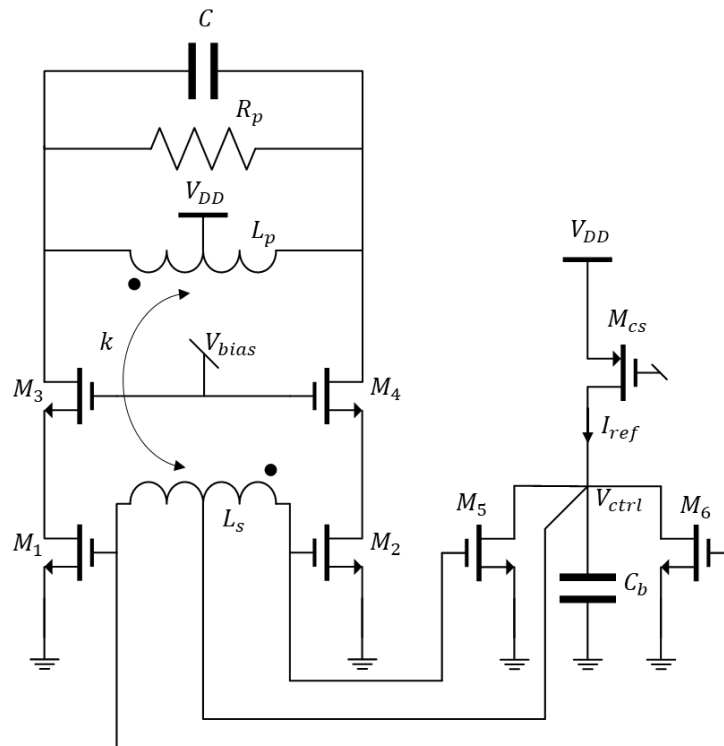


Figure 2-17: Cascode high swing class-C oscillator.



### 2.2.2. Gm boost class-C oscillator

Figure 2-18 shows the proposed oscillator with improved transconductance. The local capacitive feedback loop increases the transconductance of the oscillator compared to the cascode topology without increasing the power consumption. Therefore, the proposed circuit alleviates the start-up condition and increases power efficiency.

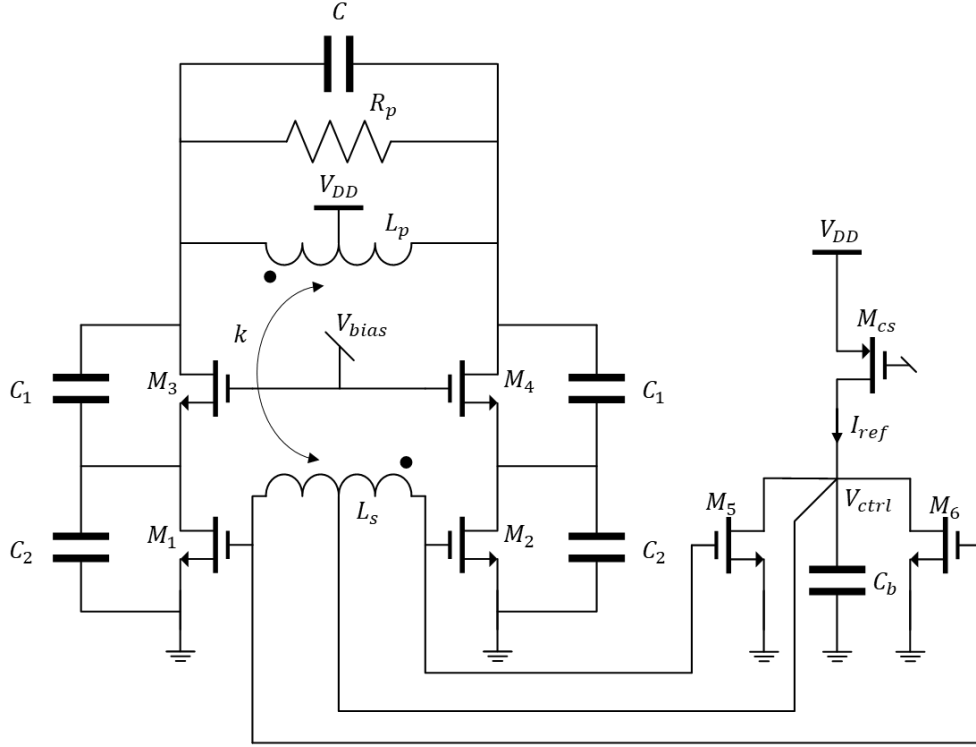


Figure 2-18: Proposed class-C oscillator.

The proposed oscillator is a hybrid topology between Colpitts and Armstrong oscillators. The oscillator is composed of two Colpitts pseudo-differential oscillators synchronized by the transformer magnetic coupling (characteristic of Armstrong oscillators). Thus, the capacitors introduce local feedback, related to each pseudo-oscillator, and the transformer ensures the main feedback loop of the oscillator. Figure 2-19 shows the small-signal model of the active device, where the transistors are biased into saturation and the channel length modulation is neglected besides the body effect. The input admittance is expressed as:

$$Y_{in}(s) = \frac{1}{2} \frac{C_2 C_1 s^2 - g_{m2} g_{m4} A_v - g_{m2} C_1 A_v s}{g_{m4} + (C_1 + C_2) s} \quad \text{Eq 2.19}$$

where  $g_{m2}$  and  $g_{m4}$  are respectively the transconductance of  $M_2$  and  $M_4$ ,  $A_v$  is the transformer voltage gain, and  $s$  is the Laplace variable.

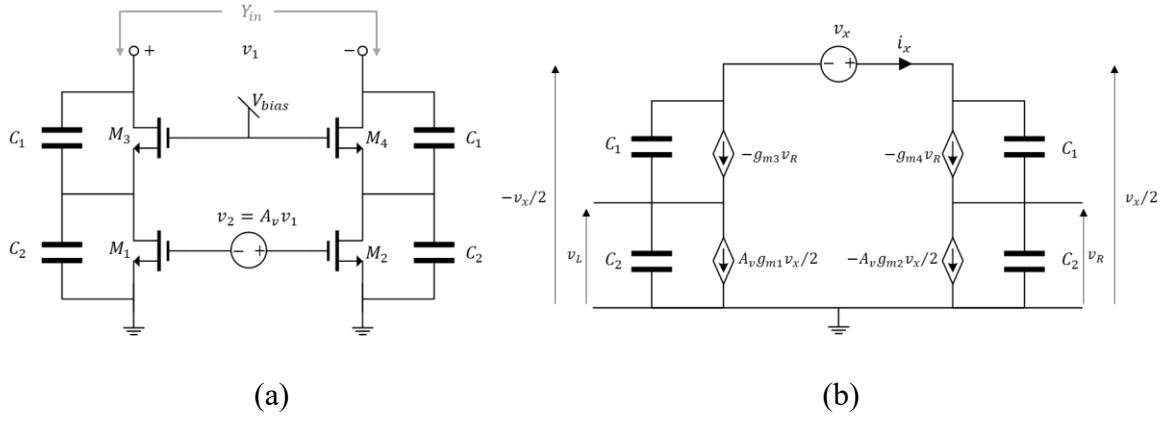


Figure 2-19: (a) The active device of the proposed oscillator. (b) The small-signal equivalent of the active device.

Since the tank is connected in shunt to the active device, an equivalent shunt conductance and shunt reactance model for the active device is convenient for analysis. Figure 2-20 shows the equivalent shunt model for the proposed active device. The conductance (i.e. transconductance) and capacitance of the active device are derived as:

$$G_{m,ADp}(\omega) = -\frac{g_{m2}}{2} \frac{\alpha C_1 C_2 \omega^2 + A_v C_1 (C_2 + C_1) + g_{m4}^2 A_v}{g_{m4}^2 + \omega^2 (C_1 + C_2)^2} \quad \text{Eq 2.20}$$

$$C_{eq}(\omega) = \frac{C_2 \omega^2 C_1 (C_1 + C_2) + g_{m2} g_{m4} A_v}{g_{m4}^2 + \omega^2 (C_1 + C_2)^2} \quad \text{Eq 2.21}$$

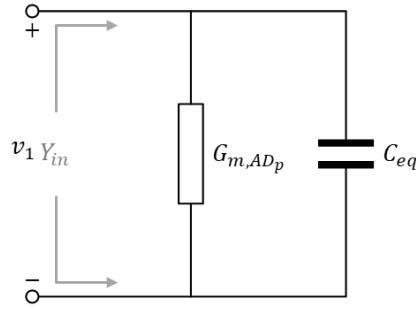


Figure 2-20: Shunt model of the active device.

where  $\alpha = g_{m4}/g_{m2}$ . For comparison the transconductance of the simple and cascode high swing class-C can be derived as:

$$G_{m,ADs} = -\frac{g_{m2}}{2} \quad \text{Eq 2.22}$$

Comparing the two transconductances in Eq (2.20) and Eq (2.22), the gm-boost is achieved only if:

$$\alpha > \frac{C_1 + C_2}{C_1} = 1/n \quad \text{Eq 2.23}$$

This condition guides the design of transistors  $M_3$  and  $M_4$  and the ratio between the capacitance  $C_1$  and  $C_2$ .

### 2.3. Phase noise

For heuristic analysis of phase noise in the oscillator, we can evaluate the effects of noise sources at zero crossing. Since the oscillator is more sensitive to noise at zero crossing as stated in the model of Hajimiri and Lee [18]. The transistors are in equilibrium at zero crossing. The transistor  $M_3$  is degenerated by  $M_1$  at his source, thus only a fragment of  $M_3$  noise is fed to the tank. On the other hand, when the differential voltage  $V_1$  is near to its minimum,  $M1$  enters the triode region canceling the degeneration advantage. At this instant, the noise injection occurs when the ISF is zero or close to zero, thanks to the class-C operation. Therefore, the noise contribution of the added cascode transistors  $M_3$  and  $M_4$  can be neglected thanks to the degeneration and class-C operation mode.

The capacitors  $C_1$  and  $C_2$  play a role in the resultant phase noise of the oscillator. The capacitor  $C_2$  presents a low-impedance path for the  $M_1$  noise to the ground i.e. filtered  $M_1$  noise, as shown in Figure 2-21.a. However, for  $M_3$  noise the capacitance presents a low impedance to the ground, thus more  $M_3$  noise reaches the tank. Similarly,  $C_1$  filters the noise of  $M_3$  (cf. Figure 2-21.b), reducing its contribution to phase noise. The ratio between the noise current discharged by the capacitor in the tank and the noise current filtered is expressed in [27] as:

$$\frac{I_{c_2}}{I_{fltr}} = \frac{\omega_0 C_2}{g_{m_{31}}} \quad \text{Eq 2.24}$$

A low capacitor value and/or high transconductance mitigate the degradation of phase noise caused by the capacitors  $C_1$  and  $C_2$ .

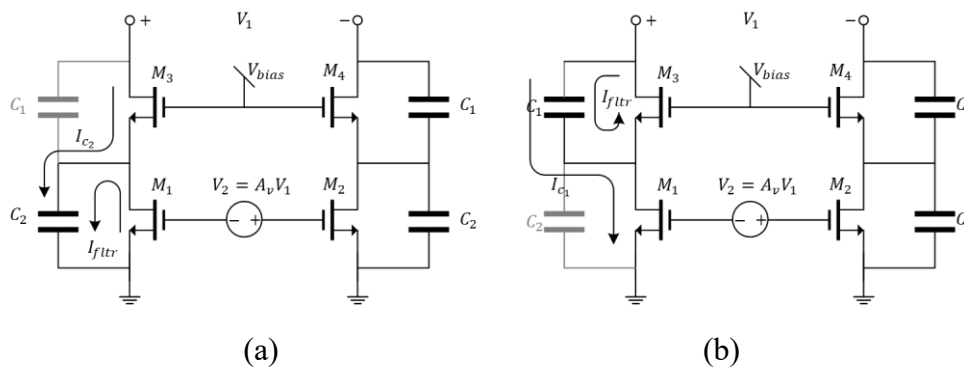


Figure 2-21: Active device noise current path with (a)  $C_2$  and (b)  $C_1$ .

The main noise sources in the proposed oscillator are the thermal noise of the resonator and the thermal and flicker noise of the active device. The control circuit noise is filtered by the large capacitor  $C_b$ , thus it can be neglected for this analysis. The total phase noise in  $1/f^2$  the region is expressed according to Eq (1.12) as:

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left[ \frac{\Gamma_{rms,tank}^2 \overline{l_{n,tank}^2} + \Gamma_{rms,AD}^2 \overline{l_{n,AD}^2}}{2A^2 C^2 \Delta\omega^2} \right] \quad \text{Eq 2.25}$$

The noise contribution of the oscillator components to the phase noise is determined through the ISF [18]. For the transformer-based resonator, considering a sine wave voltage  $V_{tank} = A_0 \cos(\omega_0 t)$ , the ISF is defined as [27]:

$$\Gamma_T = -\sin(\omega_0 t) \quad \text{Eq 2.26}$$

Figure 2-22 shows the ISF expression in Eq (2.26) compared to the simulated ISF of the tank  $\Gamma_T$ . Both curves have roughly the same trend and shape. However, the simulated ISF covers more area than the derived ISF. This difference can be explained by the fact that the output signal of the proposed oscillator is not a perfect sine wave. Despite this difference Eq (2.26) is still a relatively good approximation of the tank ISF.

For the active device, the derivation of the ISF is based on the analysis in [17], [27], where the active device ISF is expressed as a function of the tank ISF. The transformer-based resonator can be simplified to an LC model for phase noise analysis [16] as shown in Figure 2-23. The parameter of the equivalent LC model is expressed as [16]:

$$L_{eq} = \frac{\Omega_L^2(1 - k^2) - 1}{\Omega_L^4 \frac{1 - k^2}{\xi} - 1} L_p \quad \text{Eq 2.27}$$

$$C_{eq} = \frac{1}{\omega_L^2 L_{eq}} \quad \text{Eq 2.28}$$

$$R_{eq} = R_{pp} \frac{\xi k \cdot A_v}{-\Omega_L^4 \left(1 + \frac{Q_p}{Q_s}\right) + \Omega_L^2 \left(1 + \frac{Q_p}{Q_s} \xi\right)} \quad \text{Eq 2.29}$$

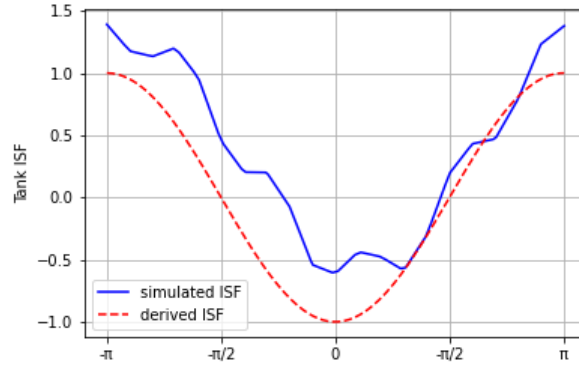


Figure 2-22: The simulated and derived tank ISF.

where  $A_v = \sqrt{L_s / L_p}$  and  $R_{p_p} = R_{sp} Q_p^2$  is the parallel resistance of the primary inductance  $L_p$ .

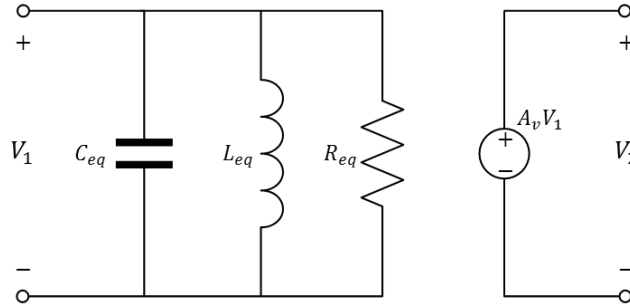


Figure 2-23: The simplified LC model of the transformer-based resonator.

The ISF of a device is defined as the excess phase generated by a specified current impulse injected into the same node as the current noise source of the device. Thus, by definition tank's ISF  $\Gamma_T$  is calculated by injecting a current impulse of area  $\Delta Q$  in parallel to the tank as shown in Figure 2-24.a. This current impulse loads the tank capacitance  $C_{eq}$  and generates a voltage

$$\Delta V_{tank} = \frac{\Delta Q}{C_{eq}} \quad \text{Eq 2.30}$$

The excessive phase caused by the current impulse is related to  $\Delta V_{tank}$ , thus  $\Gamma_T$  is linked to  $\Delta V_{tank}$ .

Similarly to the tank, the ISF of the lower transistor  $M_1$  is calculated by injecting a current impulse with a total charge of  $\Delta Q$ , as shown in Figure 2-24.b. The transistor  $M_1$  ( $M_2$  respectively) and  $M_3$  ( $M_4$  respectively) conduct simultaneously, thus a portion of the injected charge  $\Delta Q_1$  flows through  $M_3$  and generates a voltage  $\Delta V_{n1}$  across the tank capacitance  $C_{eq}$ . The other part of the charge  $\Delta Q_{n2} = \Delta Q - \Delta Q_{n1}$  is reflected by the high impedance presented

by the cascode transistor  $M_3$ . As a result, only  $\Delta Q_1$  contributes to phase noise. The ISF  $\Gamma_{ADb}$  of  $M_1$  is proportional to  $\Delta V_{n1} / \Delta V_{tank}$  based on the linearity of Hajimiri and Lee's model. The voltage  $\Delta V_1$  is given as:

$$\Delta V_{n1} = \frac{\Delta Q_1}{2C_{eq}} \approx \frac{g_{m,M_3}(g_{m,M_3} + g_{m,M_1}) + \omega^2 C_1(C_1 + C_2)}{(g_{m,M_3} + g_{m,M_1})^2 + \omega^2(C_1 + C_2)^2} \frac{\Delta V_{tank}}{2} \quad \text{Eq 2.31}$$

Thus, the ISF of the transistor  $M_1$  is derived as :

$$\Gamma_{ADB} = \frac{g_{m,M_3}(g_{m,M_3} + g_{m,M_1}) + \omega^2 C_1(C_1 + C_2)}{(g_{m,M_3} + g_{m,M_1})^2 + \omega^2(C_1 + C_2)^2} \frac{\Gamma_T}{2} \quad \text{Eq 2.32}$$

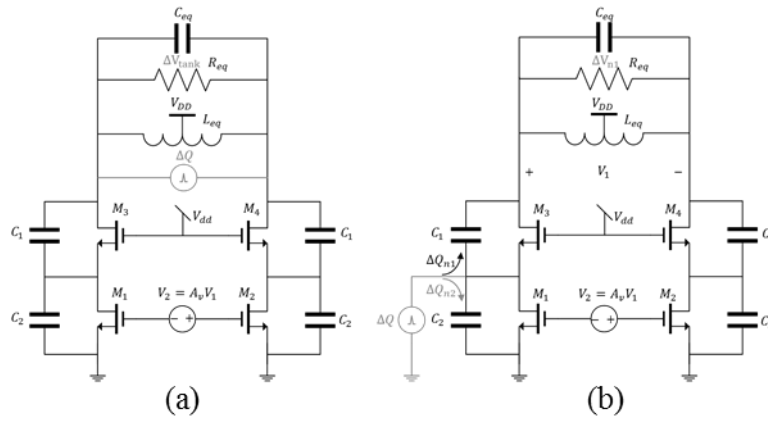


Figure 2-24: Circuit model of ISF calculation for (a) the tank and (b) the lower transistor in the active device.

Figure 2-25 shows the derived ISF in Eq (2.31) and Eq (2.32) compared to the simulated ISF. The calculated ISF of the lower transistor matches the simulated ISF. The phase noise can be estimated theoretically considering only the noise contribution of the lower transistor. The cascode transistor acts only as a buffer for the lower transistor that generates the current pulse to compensate for the losses of the tank. Thus, the lower transistor is the main contributor to the active device noise. The upper transistor also contributes to the noise of the active device but with a small part thanks to degeneration effects compared to the lower transistor, so we can neglect its contribution to simplify the analysis. Figure 2-26 compares the simulated phase noise to the empirical phase noise at  $1/f^2$  calculated from Eq (2.25). The theoretical phase noise gives a good approximation to the real phase noise in  $1/f^2$  region.

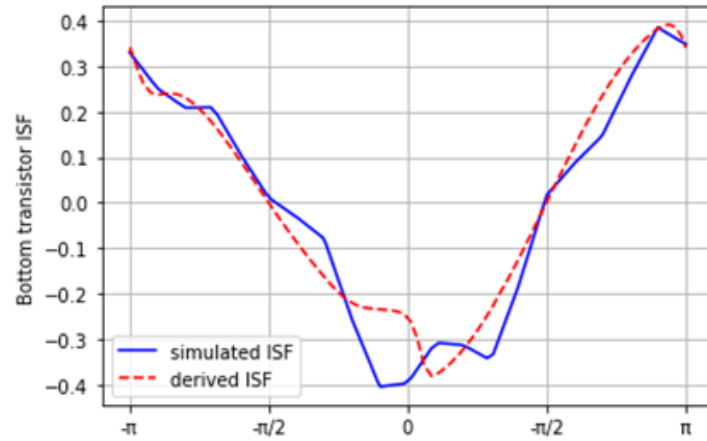


Figure 2-25: The simulated and derived ISF of the lower transistor  $M_1$ .

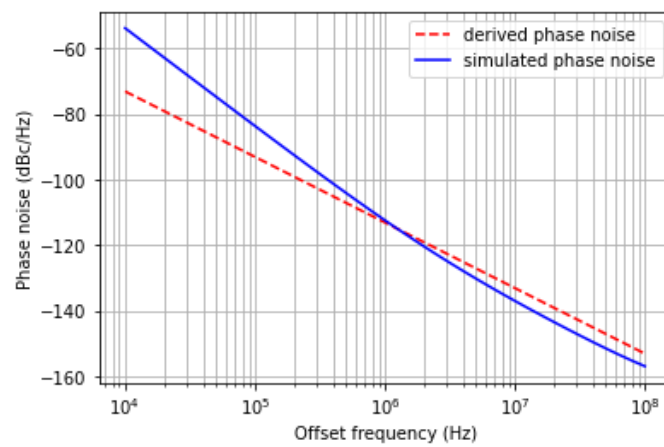


Figure 2-26: The simulated and derived phase noise of the proposed oscillator.

To investigate the effects of the added capacitors on phase noise, we compare the phase noise of the cascode class-C oscillator with that of the proposed oscillator. Figure 2-27 shows the circuit configurations used for simulation and the simulated phase noise of the cascode class-C oscillator and the proposed oscillator. The same transformer ( $L_p = 500 \text{ pH}$ ,  $L_s = 400 \text{ pH}$ ,  $Q_p = 13$ ,  $Q_s = 10$  and  $k = 0.83$ ) is used for the two setups. The phase noise simulation was performed at the optimal oscillation amplitude for both oscillators, thus the power consumption differs for each oscillator. It is 5.72 mW for the proposed oscillator and 6.27 mW for the cascode oscillator. The local feedback - introduced by the capacitors  $C_1$  and  $C_2$  - improves the phase noise by 1 dB and reduces the power consumption by 0.5 mW. Table 2-1 summarizes the noise contribution of each component in the oscillator at 1 MHz offset for the two oscillators. The noise contribution of the active device in the proposed oscillator is reduced compared to the cascode structure. This is thanks to the filtering action of the capacitors. Moreover, the gm boost with a passive element increases the oscillation amplitude with reduced power consumption. Note that the lower transistors are the major

contributor in the oscillator as well as in the active device which confirms our assumption in phase noise calculation.

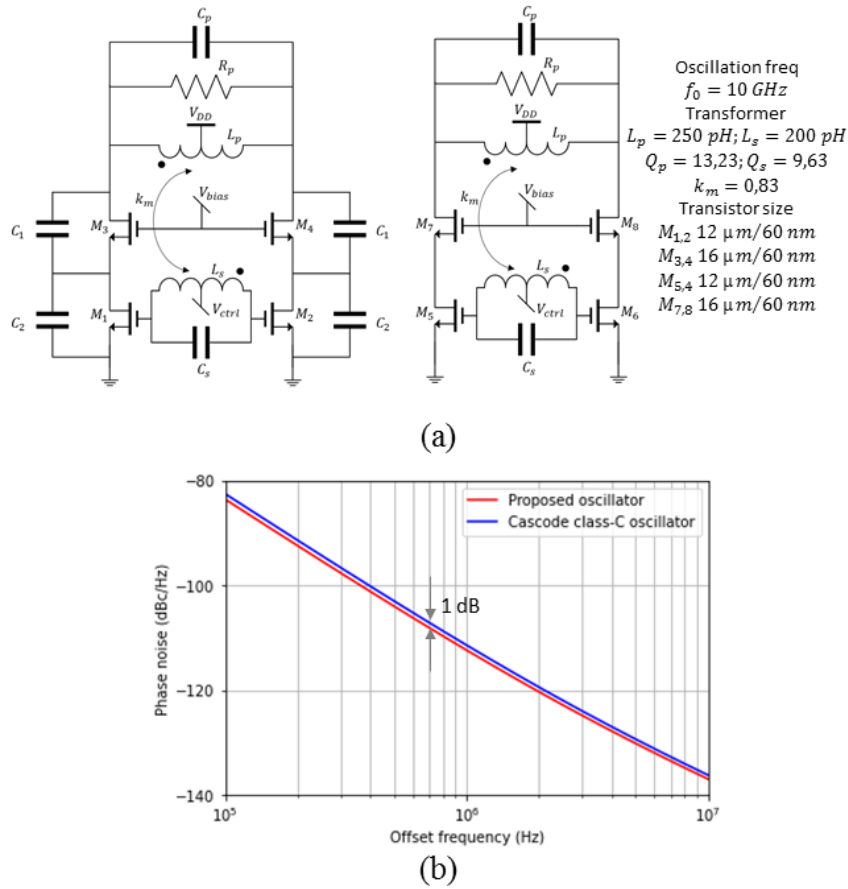


Figure 2-27: (a) The set-up configuration (b) The phase noise simulation of the proposed oscillator and the cascode class-C oscillator.

Noise sources	Cascode class-C oscillator		Proposed class-C oscillator	
	Value	%	Value	%
<b>Resonator</b>	$4.32 \times 10^{-13} \text{ V}^2/\text{Hz}$	12%	$4.57 \times 10^{-13} \text{ V}^2/\text{Hz}$	14%
<b>Lower transistors</b>	$2.61 \times 10^{-12} \text{ V}^2/\text{Hz}$	72%	$2.34 \times 10^{-12} \text{ V}^2/\text{Hz}$	72%
<b>Upper transistors</b>	$2.27 \times 10^{-13} \text{ V}^2/\text{Hz}$	6%	$3.03 \times 10^{-13} \text{ V}^2/\text{Hz}$	9%
<b>Control circuit</b>	$3.63 \times 10^{-13} \text{ V}^2/\text{Hz}$	10%	$1.45 \times 10^{-13} \text{ V}^2/\text{Hz}$	4%
<b>Total</b>	$3.64 \times 10^{-12} \text{ V}^2/\text{Hz}$	100%	$3.25 \times 10^{-12} \text{ V}^2/\text{Hz}$	100%
<b>Phase noise at 1 MHz</b>	-111.45 dBc/Hz		-112.4 dBc/Hz	
<b>Power consumption</b>	6.27 mW		5.72 mW	
<b>FoM at 1MHz</b>	183.47		184.82	
<b>Differential amplitude</b>	1.01 V		1.07 V	

Table 2-2: Comparison of noise contribution at 10 GHz between the cascode class-C and the proposed class-C.



### 2.3.1. Phase noise tuning

As discussed earlier, phase noise is highly dependent on the amplitude, doubling the amplitude reduces the phase noise by 6 dB. Thus, varying the amplitude allows the oscillator's phase noise to be adjusted. On the other hand, the amplitude is set by the drain current of  $M_1$  and  $M_2$ , which can be expressed as:

$$I_{ds,M_{1,2}}(\omega t) = \frac{\mu_e C_{ox} W}{2} [V_{ctrl} + A_v V_0 \cos(\omega t) - V_{th}]^2 \quad \text{Eq 2.33}$$

where  $\mu_e$  is the electron mobility,  $C_{ox}$  is the gate oxide capacitance per unit area,  $W$  is the width of the transistor and  $L$  is the length of the transistor,  $A_v$  is the transformer's voltage gain,  $V_0$  is the oscillation amplitude and  $V_{th}$  is the threshold voltage. The control circuit regulates the current drain of  $M_1$  and  $M_2$ , through the feedback signal  $V_{ctrl}$ . These drain currents can be also controlled by the threshold voltage  $V_{th}$ . The back-gate of the 28 nm FD-SOI transistors offers a wide tuning range of the threshold voltage (cf Figure 2-8). Thus, the drain current, as well as the amplitude, is controlled by the back-gate of  $M_1$  and  $M_2$ . The variation of the amplitude over the back-gate voltage induces a variation in phase noise. Hence, the back-gate voltage of the 28 nm FD-SOI transistor can tune the phase noise of the oscillator.

Figure 2-28 shows the phase noise and power consumption as a function of the back-gate voltage  $V_{bulk}$ . The phase noise is reduced by 10.48 dB for 1 V variation of  $V_{bulk}$ , while the power consumption increased by 1.27 mW. The body biasing adjusts the performance of the oscillator. This capability can be used in satellite communications since satellite-to-earth and satellite-satellite communications do not require the same phase noise constraints. In satellite-to-earth communications, the oscillator must have a high spectral purity due to the long-distance and atmosphere attenuation. While satellite-to-satellite communication experiences less harsh conditions in the vacuum, thus it demands a more relaxed phase noise. Adjusting the RF circuit performance between those two types of communication optimizes the power consumption and, in the long term, reduces the stress on the circuit, as the oscillator alternates between tight and relaxed conditions. Moreover, performance drifts due to radiation and temperature can be adjusted over the life of the oscillator, increasing its robustness and the operational lifetime of the circuit.

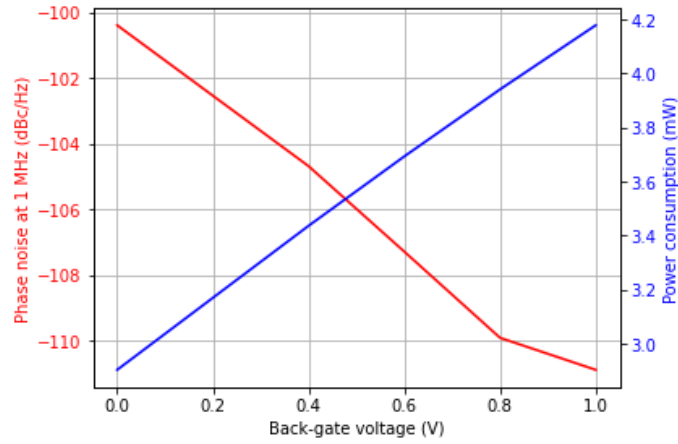


Figure 2-28: Phase noise at 1 MHz and power consumption as a function of the back-gate voltage of  $M_1$  and  $M_2$ .

### 3. Conclusion

Our proposed oscillator comes as an evolution from the high-swing class-C oscillator. The cascode structure of the active device mitigates the reliability issues in oscillators such as HCI and TDDDB, thus ensuring the long-term reliability of the circuit. The local feedback added by the capacitors improves the transconductance, power efficiency, and phase noise of the oscillators. The simulation shows a 1 dB improvement in phase noise with a power-saving of 0.5 mW thanks to the local feedback loop. We also demonstrated that the 28 nm FD-SOI back-gate can tune the phase noise and the power consumption over a wide range. This feature can be used to optimize power consumption by adjusting the oscillator performance according to the application or to correct the performance variation caused by aging or radiation.

In the next chapter, we will present the implementation of the proposed topology for the two oscillation frequencies 10 GHz and 40 GHz. The design flow and methodology in 28 nm FD-SOI technology will be discussed.

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## Chapter 3:

### Circuit Design

*This chapter describes the design strategy followed to implement the proposed Class C oscillator topology in 10 and 40 GHz oscillation frequencies. The chapter begins with an overview of the VCOs schematics and the challenges corresponding to each VCO before presenting the adopted design flow. For each block of the VCOs, we detail the design methodology of the implementation, starting with the transformer to the output buffers. Finally, we present the implementation of the VCOs in the chip.*

#### 1. Introduction

Our proposed topology, detailed in the previous chapter, provides three main advantages:

- Low power due to the high efficiency of the class-C structure.
- Improved reliability against HCI thanks to the cascode structure of the active device.
- Adaptive phase noise using the back gate voltage of the active device transistors.

Two prototype oscillators have been designed to evaluate the proposed topology. One at an oscillation frequency of 10 GHz, a band frequently used in space communications, to test the topology capability and phase noise adaptability. The second oscillator is implemented in a 40 GHz oscillation frequency to evaluate the topology at mm-wave frequencies where wide bandwidths are available for high-speed communication. Although the two VCOs share the same topology, the design challenges and target performance are different. In the following subsection, we detail the design challenges and schematic of each VCO.

##### 1.1. 10 GHz VCO

Analog design is a matter of finding the right trade-off between all the performances. In the case of oscillators, four main parameters - phase noise, power consumption, reliability, and tuning range - counterbalance each other, as shown in Figure 3-1. Our main driver/challenge in the design of the 10 GHz oscillator is to achieve a good balance between

all these parameters through the topology, but also to provide dynamic tuning to modify the trade-off to optimize the performance for the targeted applications. This last characteristic is part of the new doctrine of the so-called smart satellites that have onboard processing allowing them to adapt to the environment for an optimal link.

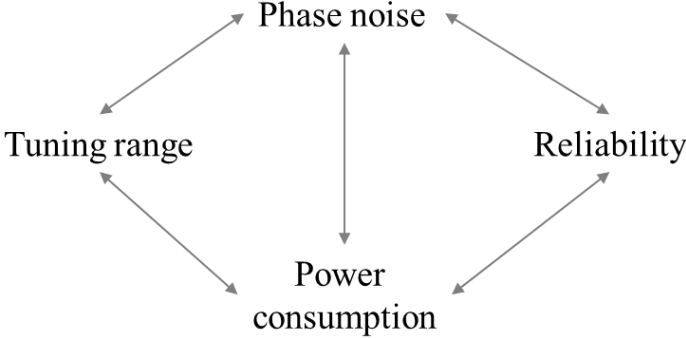


Figure 3-1: Trade-offs between oscillator parameters.

Figure 3-2 shows the 10 GHz VCO schematic and layout sketch. The VCO is frequency tuned by two 4-binary weighted switching capacitors for coarse tuning and varactors for fine and continuous tuning. One is connected to the transformer primary and the other to the transformer secondary. The back-gates of transistors  $M_1$  and  $M_2$  are used to adjust the phase noise and power consumption. This will allow the oscillator to be optimized for multiple applications.

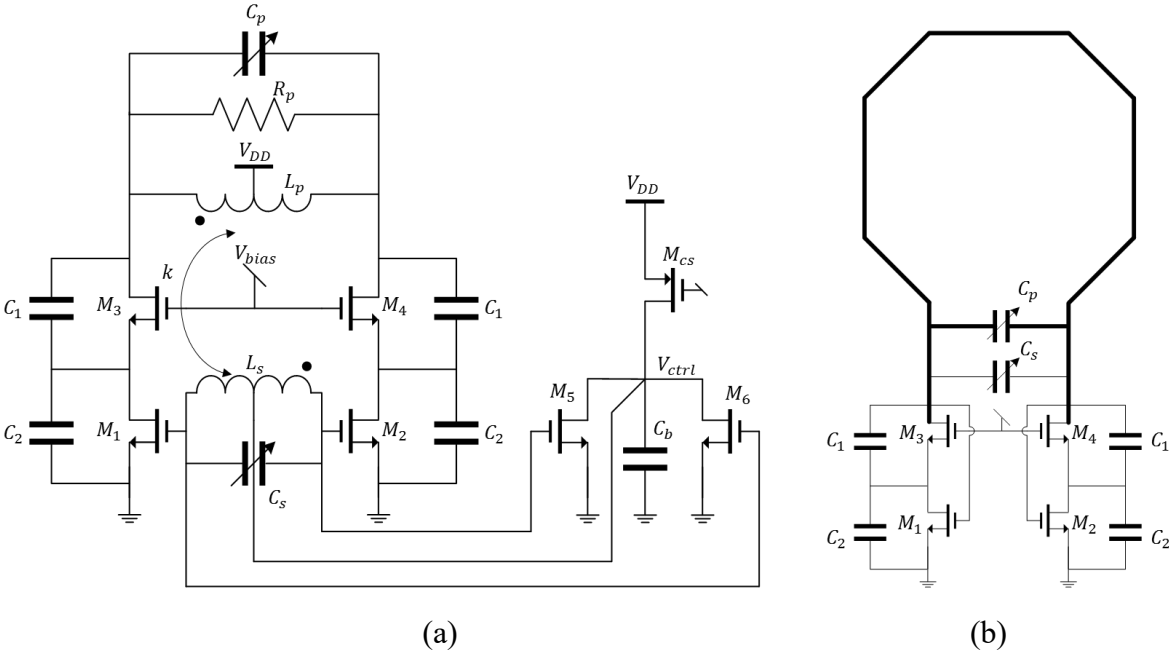


Figure 3-2: 10 GHz VCO (a) schematic and (b) layout sketch.

## 1.2. 40 GHz VCO

Achieving a wide Frequency Tuning Range (FTR) and low phase noise is the main challenge in Millimeter-Wave (mmW) VCO. On one hand, as the frequency increases, the lumped oscillator resonator shrinks, increasing the ratio of parasitic capacitance to the total resonator capacitance, which limits the tuning range. Moreover, the parasitic capacitance of the active device significantly reduces the tuning range of the VCO. On the other hand, at mm-wave frequencies, the varactor has a low-quality factor becoming the dominant factor in the resonator. For instance, a 7.5  $\mu\text{m}$  wide MOS varactor in 28 nm FD-SOI technology has a quality factor of 13.41 at 40 GHz.

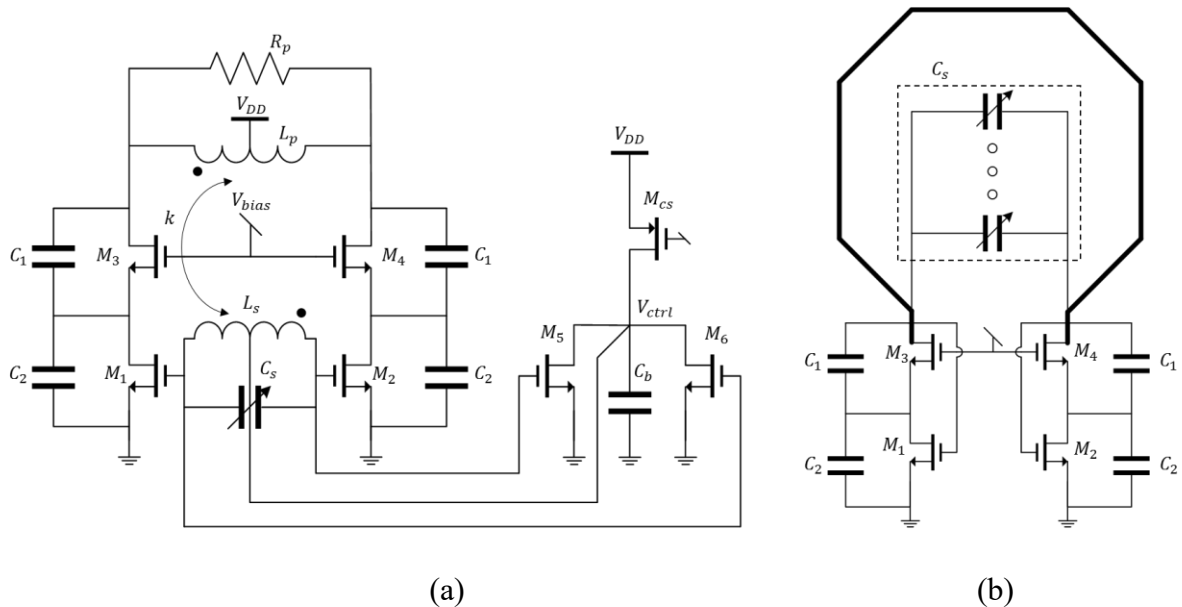


Figure 3-3: 40 GHz VCO (a) schematic and (b) layout sketch.

The main focus of the 40 GHz VCO design is to ensure a wide tuning range while maintaining low phase noise and low power consumption. Figure 3-3 shows the schematic and the layout sketch of the 40 GHz VCO. Frequency tuning is provided by a 6-bit differential switched capacitor bank and the parasitic capacitance of  $M_3$  and  $M_4$  controlled through the back-gate voltage. The first 5 bits control binary-weighted switching elementary capacitors, the 6<sup>th</sup> bit controls a bank of 8 elementary capacitors. In this topology, we omitted the low-quality factor varactors and replace them with the parasitic capacitance of the transistors  $M_3$  and  $M_4$  transistor. Thanks to the wide-body biasing voltage of the 28 nm FD-SOI, the parasitic capacitance of  $M_3$  and  $M_4$  can be adjusted and therefore, guarantee continuous tuning. In this topology, we exploit the parasitic capacitance to our advantage and at the same time avoid the low-quality factor varactor. The capacitor bank was placed inside



the transformer (cf. Figure 3-2.b) to reduce the routing wires and their parasitic inductance that limit the FTR.

## 2. Design flow

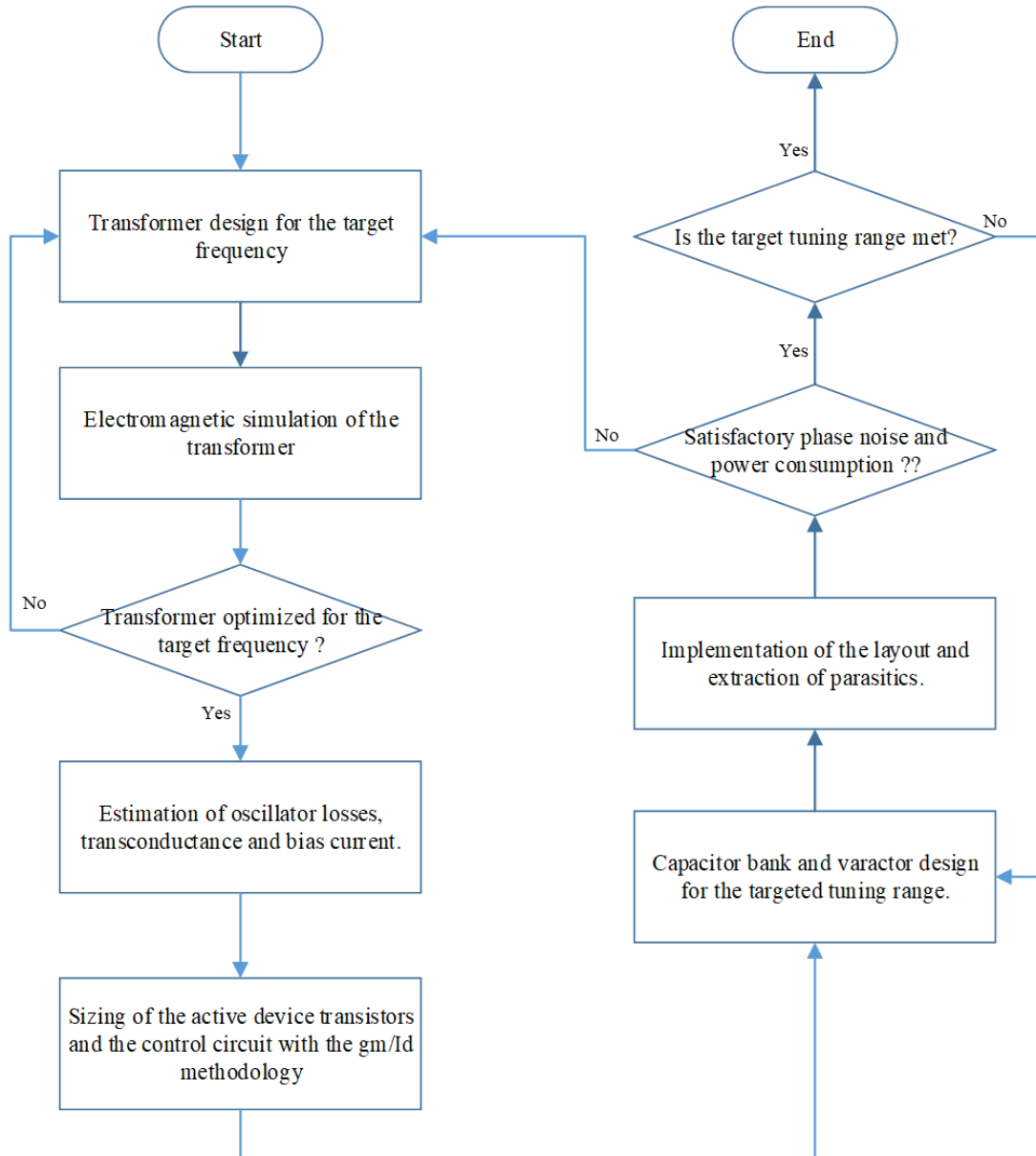


Figure 3-4: Design flow

Figure 3-4 summarizes the design flow followed in the design of the two VCOs. The first step of the design is the selection of the optimal transformer dimensions for the target frequency by iterative sizing of the transformer. The transformer is evaluated by its magnetic coupling coefficient, coil quality factor, and self-resonance frequency. After the transformer is designed, the resonator losses can be estimated assuming that the transformer is the main source of losses in the tank. From the estimated losses, we can derive the transconductance

needed to compensate for the losses in the tank, and calculate the bias current to obtain the maximal oscillation amplitude. The active device and control circuit transistors are sized using the gm/Id methodology and based on estimates of transconductance and bias current. These derived transistors' dimensions serve as a starting point to optimize the size of the transistors through iterative simulations. After that, we design the capacitor banks and size the varactors to cover the targeted frequency tuning range. When all the components are sized we implement the VCO layout to extract the parasitics and re-evaluate the VCO performance taking these parasitics into account. The lead wires that connect the transformer to the capacitor and the active device were included and simulated in the electromagnetic model of the transformer, everything else is extracted through cadence extraction software. The purpose of this step is to readjust the transformer and the transistors to account for the losses in the layout. The frequency shifts due to parasitic inductances and capacitances are corrected by resizing the capacitor bank and the varactors.

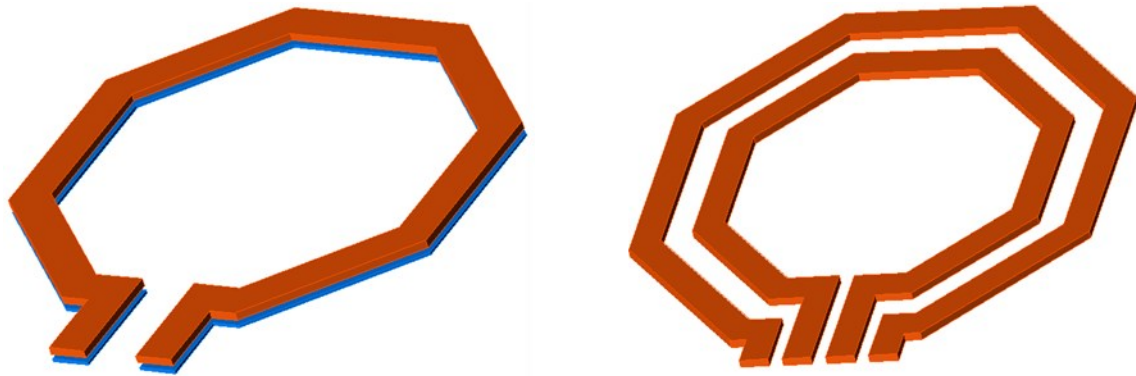
### 3. Transformer design

The transformer is usually not included in the technology design kit, which is the case for 28 nm FD-SOI. The designer must design and characterize the transformer through EM simulations. The design process is iterative and time-consuming, which limits the use of the transformer in integrated circuits. To accelerate the design process, we created a parameterized cell (PCell) of the transformer.

The monolithic transformer is commonly implemented as an interleaved or stacked transformer (cf. Figure 3-4). Each topology has its pros and cons. In the interleaved structure the coils are implemented in the same metal layer, so they have similar electrical characteristics and a good quality factor. However, the magnetic coupling is weak. In contrast, the stacked transformer has a better magnetic coupling (close to 0.9), but its windings are implemented in different metal layers, which results in different electrical characteristics for each coil.

Two PCells were designed, one for the interleaved transformer and the other for the stacked transformer. The 28nm FD-SOI has three thick and six thin metal layers (cf. Figure 2-9). The coils of the interleaved transformer were implemented both in the top metal layer (LB). In the stacked transformer, the primary was implemented in the top metal layer (LB) and the secondary in the second layer (IB). Both topologies were evaluated with the PCells for different sizes. The transformers were compared according to the following parameters:

- The self-resonance frequency of the primary and the secondary.
- The quality factor of the primary and the secondary at the targeted frequency.
- The inductance of the primary and the secondary at the targeted frequency.
- The magnetic coupling at the targeted frequency.



(a)

(b)

Figure 3-5: (a) Stacked transformer; (b) Interleaved transformer.

For the transformer design, the self-resonance frequency should, as a rule of thumb, be 3 times the operating frequency. The transformer is sized to maximize the quality factor and the magnetic coupling around the targeted frequency. For the value of the inductance, it is preferred to choose a low value because it improves the phase noise. The phase noise expression in Eq (1.13) can be rewritten with  $R_p = L \cdot Q_T \cdot \omega_0$  as:

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left[ \frac{\overline{i_n^2} / \Delta f}{P_{RF}} \cdot \left( \frac{L}{Q_T} \right) \cdot \Gamma_{rms}^2 \cdot \frac{\omega_0^3}{4\Delta\omega^2} \right] \quad \text{Eq 3.1}$$

Thus, according to Eq (3.1), reducing the inductance  $L$  improves the phase noise. However, the parallel resistance  $R_p$  is also reduced and with it, the amplitude, so more current must be injected into the oscillator to keep the same amplitude. As a result, the phase noise trades off with the power consumption.

The following subsection details the transformer design for each VCO. In the 40 GHz VCO subsection, we discuss the difference between the interleaved and the stacked transformer.

### 3.1. Transformer design: 40 GHz VCO

To design the 40 GHz VCO, different transformer sizes of both topologies (stacked and interleaved) were designed with the PCells and simulated with Momentum. This subsection compares the two topologies based on the evaluation parameter stated above.

### 3.1.1. Self-resonance frequency

The parasitic capacitance of the substrate resonates with the transformer coils at a frequency called the self-resonant frequency defined as:

$$f_{self\_res} = \frac{1}{2\pi\sqrt{L_{coil}C_{substrate}}} \quad \text{Eq 3.2}$$

Above this frequency, the transformer windings behave like a capacitive element. The transformer must therefore operate below its self-resonance frequency. As a rule of thumb, the self-resonance frequency should be three times the operating frequency. Thus, for a 40 GHz VCO, the transformer's self-resonant frequency must be 120 GHz or higher for both coils.

Figures 3-6 and 3-7 show the self-resonance frequencies of simulated interleaved and stacked transformers, respectively. In both structures, the self-resonant frequency decreases with larger inductance, which is expected since the area of the coils increases with inductance and with it the substrate parasitic capacitance. Therefore, the self-resonant frequency decreases with a large inner diameter and a large coil width. The maximum inductance is limited by the self-resonance frequency.

The self-resonant frequency of the primary coil differs from that of the secondary coil in the interleaved transformer (cf. Figure 3-6) because the secondary (the outer coil) has a larger diameter than the primary (the inner coil). Thus, the parasitic capacitance and the inductance of the secondary are larger than that of the primary. In the stacked transformer, the self-resonant frequency of the secondary is close to that of the primary (cf. Figure 3-7) because both coils have the same diameter. The slight difference between their values is due to the secondary being closer to the substrate than the primary.

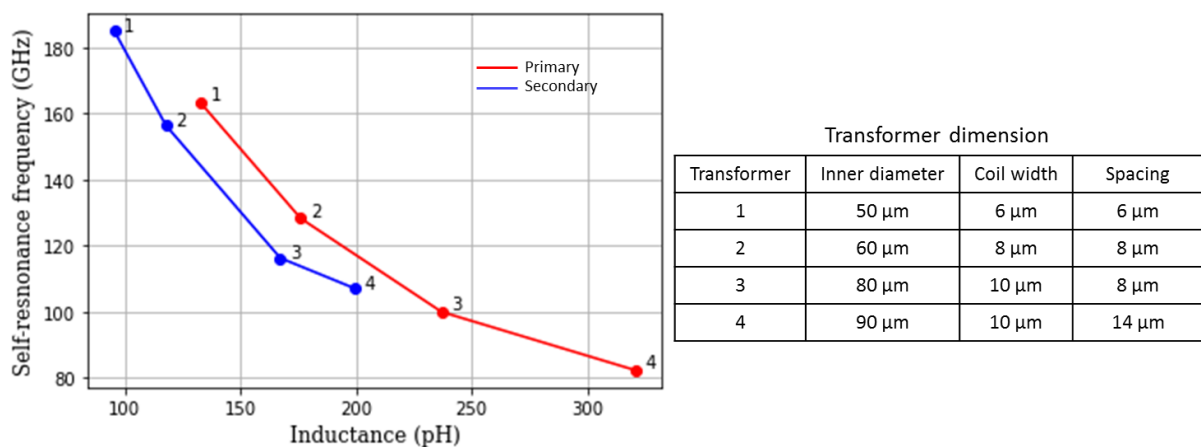


Figure 3-6: self-resonance frequency in the simulated interleaved transformers.

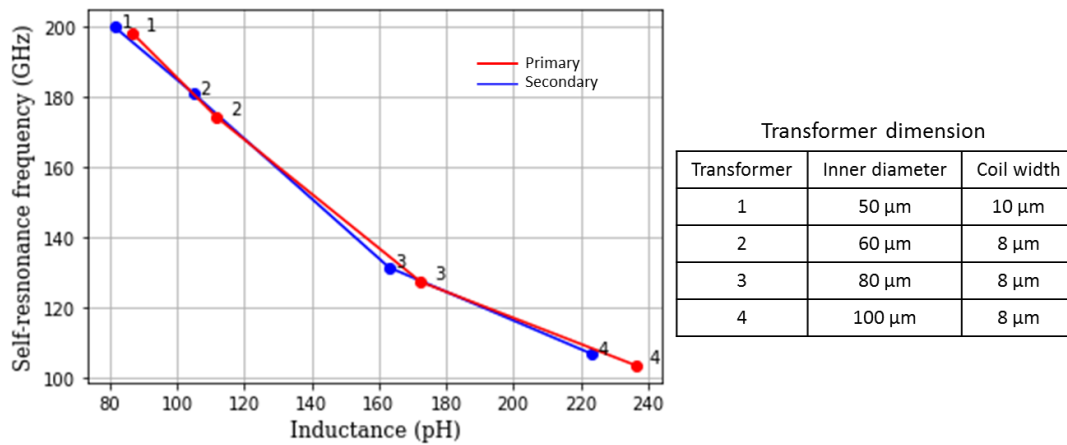


Figure 3-7: self-resonance frequency in the simulated stacked transformers.

In theory, the stacked transformer should have the worst self-resonance frequency since the secondary coil is closer to the substrate, but the compactness of its topology results in a smaller area compared to the interleaved structure, thus the capacitive coupling with the substrate is lower, making it more suitable for high frequency uses.

### 3.1.2. Quality factor and magnetic coupling

Here we consider only the transformer that meets the self-resonant frequency criterion ( $> 120$  GHz). Figures 3-8 and 3-9 show the quality factor and magnetic coupling of the interleaved and stacked transformer, respectively. In the interleaved transformer, the quality factor of the secondary and primary are relatively close with a difference of 1 to 2. This small difference is explained by the fact that the secondary coil is larger than the primary coil, and thus has a higher series resistance. In the stacked transformer, the secondary and primary are implemented in different metal layers and their quality factors are therefore different. The primary coil of the interleaved transformer and the stacked transformer achieve the same quality factor for the same diameter, but the secondary coil of the stacked transformer is considerably lower than that of the interleaved transformer. However, the magnetic coupling of the stacked transformer is twice as high as that of the interleaved transformer. In summary, the stacked transformer has a compact area and good magnetic coupling. While the interleaved transformer has a better-quality factor per coil but occupies a large area and has a weak magnetic coupling.

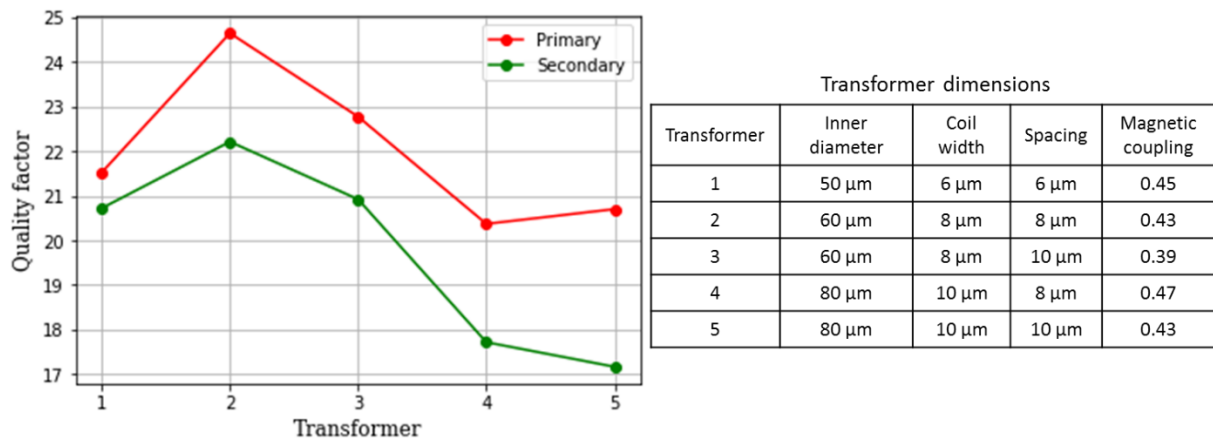


Figure 3-8: Coils quality factor and magnetic coupling coefficient in the simulated interleaved transformers.

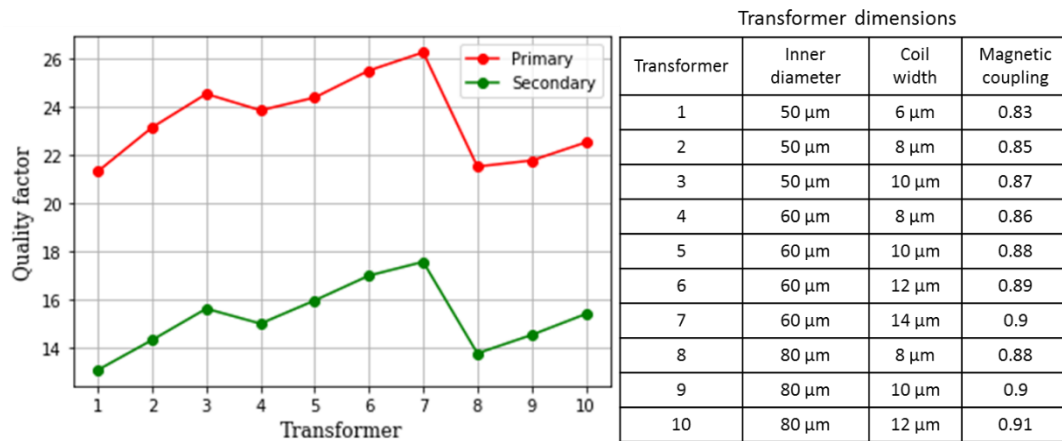


Figure 3-9: Coils quality factor and magnetic coupling coefficient in the simulated stacked transformers.

The quality factor increases with the width of the coil as the resistivity decreases (cf. Figure 3-9). On the other hand, as the transformer gets longer, the resistivity of the coil increases, and thus the quality factor decreases. However, in Figure 3-8, the opposite is observed, the quality factor increases when the transformer goes from a diameter of 50  $\mu\text{m}$  to 60  $\mu\text{m}$ . This is because, at a higher frequency, losses are not only caused by the series resistance of the coil but other mechanisms are added such as the skin effect and the proximity effect. Proximity effects become more important in small diameter coils, so by increasing the diameter, losses are reduced and thus explain the increase in quality factor observed with larger coils. As a design rule, the transformer is designed with a diameter greater than 50  $\mu\text{m}$  to limit proximity effects [1].

The resonator quality factor is expressed in Eq (2.8), it takes into account the individual quality factor of each coil but also the transformer magnetic coupling. Figure 3-10 shows the

resonator quality factor of the interleaved and stacked transformer at 40 GHz with  $\xi = 1$ . What stands out in this figure is the clear superiority of the quality factor of the stacked transformer over the interleaved transformer. The high magnetic coupling in the stacked transformer improves the overall quality factor despite the high losses in the secondary coil compared to the interleaved transformer. Therefore, we choose the stacked structure for transformer design in the 40 and 10 GHz VCOs.

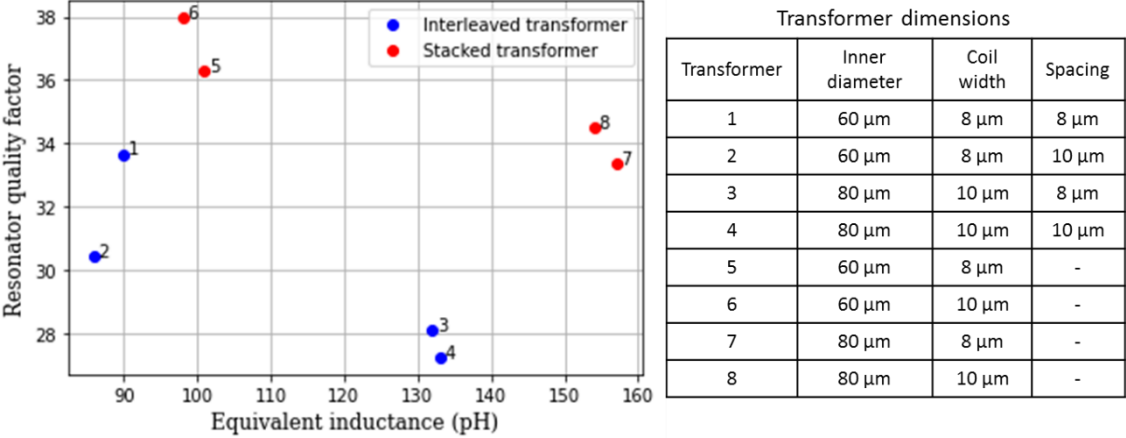


Figure 3-10: Comparison of the resonator quality factor of the stacked and interleaved transformers.

The secondary winding of the transformer is connected to a capacitor bank for coarse tuning in the 40 GHz VCO. The routing wire between the transformer and the capacitor bank adds parasitic inductance that limits the tuning range. To improve the tuning range, we implement the capacitor bank inside the transformer to reduce the routing wire. Figure 3-11 shows the designed transformer and its simulation model with parasitics. The horseshoe shape of the transformer allows the integration of the capacitor bank inside the transformer. The presence of metal layers inside the transformer impacts its performance. Thus, to evaluate the impact of the capacitor bank on the transformer, we created a model of the transformer with the metal layers of the switching capacitor inside the transformer as shown in Figure 3-11.b. Table 3-1 compares the performances issued from the electromagnetic simulation of the transformer with and without the capacitor bank inside and the equivalent inductor of the transformer (From Eq (2.26)). The equivalent inductance was designed by stacking two metal layers LB and IB. The resonator quality factors in the table are calculated with Eq (2.8).

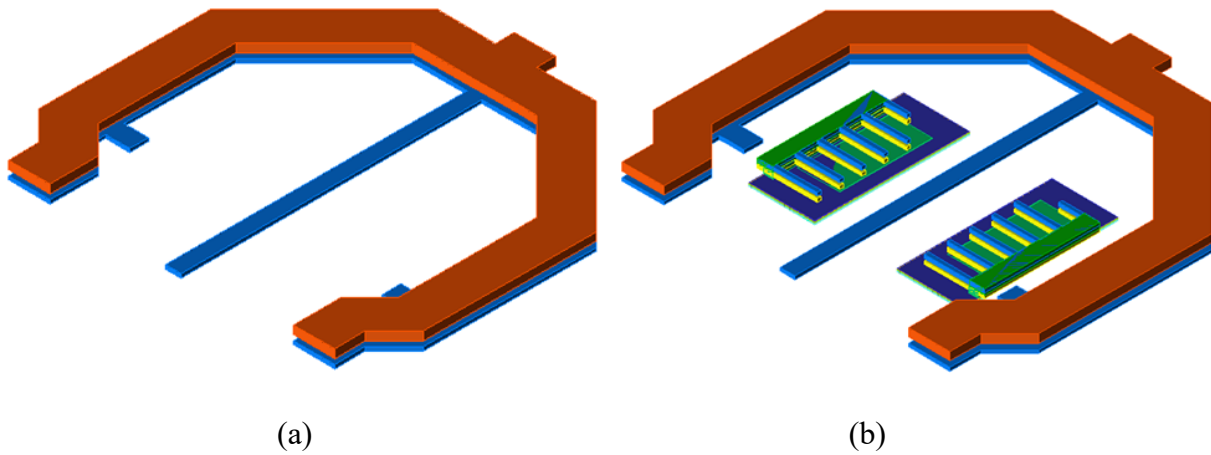


Figure 3-11: (a) The design Horseshoe-shaped stacked transformer (b) The transformer with capacitor bank model inside it.

		Transformer	Transformer with parasitic	Equivalent inductor
<b>Inductance</b>	<b>Primary</b>	111 pH	108 pH	94.8 pH
	<b>Secondary</b>	93.5 pH	90.3 pH	
<b>Magnetic coupling coefficient</b>		0.83	0.83	-
<b>Resonator Quality factor</b>		37	33.5	33

Table 3-1: Comparison between the transformer with and without the capacitor model, and its equivalent inductance.

The capacitor bank inside the transformer reduces the resonator quality factor by 9.5%, which corresponds to 1 dB of phase noise degradation according to Eq (1.13). The extended tuning range comes at the cost of a slight phase noise degradation. What is remarkable in the table is that the transformer resonator quality factor is higher than that of the inductance. Even with the parasitic inside the transformer, the resonator quality factor of the transformer is comparable with a slight advantage over the one of the inductor. The high resonator quality factor of the stacked transformer over the inductance can be explained through the classical quality factor definition, which is:

$$Q = 2 \times \pi \frac{\text{energy stored}}{\text{energy dissipated per cycle}} \quad \text{Eq 3.3}$$

The stacked transformer stores energy by the magnetic coupling between its coils in addition to the energy stored in inductors like the simple inductor. The transformer, hence, stores more energy than the inductor, resulting in a higher resonator quality factor. A note of caution is due here since the transformer might dissipate more energy than the inductor. Thus, the transformer has an improved resonator quality factor than the inductor only if the stored



magnetic energy added is greater than the dissipated energy introduced by the secondary coil. The energy loss is related to the metal thickness, if the technology disposes of multiple thick metal layers, as in the case in the 28 nm FD-SOI, the stacked transformer might outperform the inductor. For an interleaved transformer, it has been shown in [2] that the interleaved transformer exhibits a similar quality factor as the inductor subject to the same area constraint. In summary, the BEOL of the technology is the main factor that determines whether or not the stacked transformer will have a better quality factor than the inductor.

### 3.2. Transformer design: 10 GHz VCO

The 10 GHz transformer is designed in a stacked structure that has been previously shown to be better than the interleaved structure. The transformer was designed through an iterative process to find the optimal sizing at 10 GHz. Table 3-2 compares the designed transformer with its equivalent inductance at 10 GHz. Here again, we reiterate the same result as for the transformer at 40 GHz, that the stacked transformer has a better quality factor than a single inductance in the 28 nm FD-SOI technology. In other words, a transformer-based oscillator achieves a lower phase noise than an equivalent inductance-based oscillator.

		<b>Transformer</b>	<b>Transformer with routing wires</b>	<b>Equivalent inductor</b>
<b>Inductance</b>	<b>Primary</b>	268 pH	492 pH	241 pH
	<b>Secondary</b>	274 pH	398 pH	
<b>Magnetic coupling coefficient</b>		0.85	0.82	-
<b>Resonator Quality factor</b>		24.3	19.35	18.87

Table 3-2: Comparison between the transformer with and without routing wires, and its equivalent inductance.

The 10 GHz VCO resonator is composed of the transformer connected to two capacitor banks, one at the secondary and one at the primary as shown in Figure 3-2. The wires connecting the transformer and the capacitor banks introduce parasitics that must be taken into account in the modeling of the transformer. Hence, these wires are included in the EM model of the transformer. Figure 3-12 shows the transformer design and its model with the routing wires. The characteristics of the transformer with the lead wires are shown in Table 3-2. The inductance has increased significantly, which impacts the tuning range of the VCO, however, at 10 GHz frequency, there is a comfortable margin for tuning capacitance to adjust the tuning range for the targeted interval, unlike at the 40 GHz frequency. The quality

factor has decreased by a factor of 20 % but it is still higher than that of an inductance-based resonator.

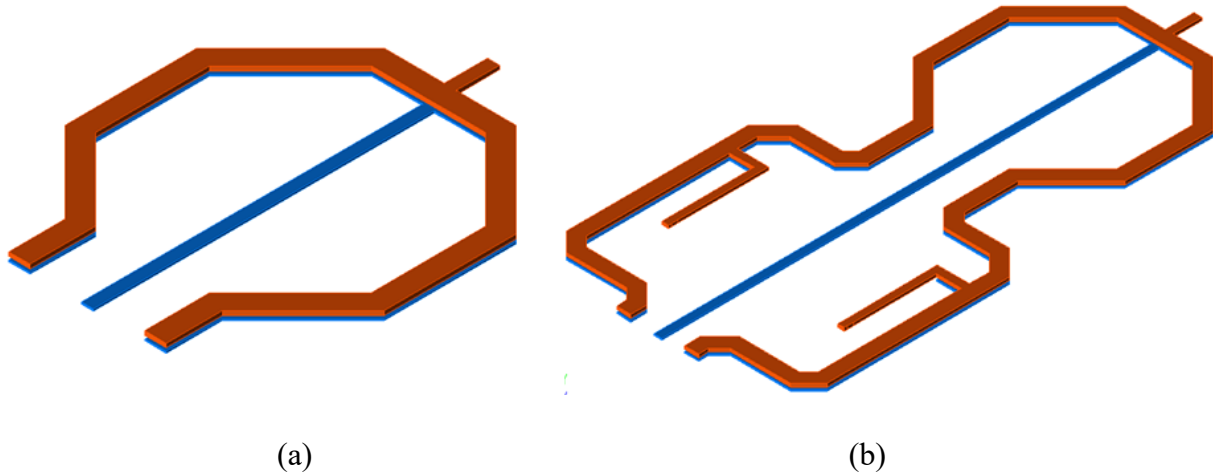


Figure 3-12: (a) The design 10 GHz VCO transformer and (b) the transformer model with the routing wires.

### 3.3. Conclusion

This section has shown that the stacked transformer outperforms the interleaved transformer and single inductance in terms of quality factor. Therefore, we have implemented a stacked transformer in the 10 and 40 GHz VCO. The design procedure is mainly based on repetitive sizing and electromagnetic simulation until an optimal size is found. In the 40 GHz VCO, we designed a horseshoe-shaped transformer in which the capacitor bank will be placed inside to minimize the wire parasitic inductance.

In section 2.1.1 in chapter 2, we discussed the phase noise improvement that a step-up transformer with a voltage gain of 1.48 can provide. Implementing such voltage gain in a stacked transformer misaligns the primary and the secondary coils, which significantly reduces the magnetic coupling. Thus, the quality factor is drastically reduced and the phase noise degradation due to the quality factor is more important than the step-up transformer improvement. As a result, we kept the voltage gain at 1 to improve the magnetic coupling with aligned coils.

## 4. Active device and control circuit design

The active device generates the required transconductance to compensate for the losses in the resonator. Thus, the design of the active device must start with the estimation of the losses

in the resonator. For the oscillation to start, the transconductance  $G_m$  of the active device and the losses in the tank must satisfy the equations below:

$$G_m = k_{osc} G_{tank} \quad \text{Eq 3.4}$$

where  $G_{tank}$  is the tank conductance and  $k_{osc}$  is a design constant chosen greater than 1 to guarantee the oscillations. With the transformer characteristics extracted from EM simulation and Eq (2.6), we can estimate  $G_{tank}$ . Figure 3-13 shows the tank conductance in 10 GHz VCO over a 20% tuning range. The resonator conductance is frequency-dependent, varying by 18% between the highest and lowest value. This also implies an amplitude variation over the tuning range with a fixed bias current. For the transconductance design, we consider the worst-case in terms of losses which is at the minimum frequency.

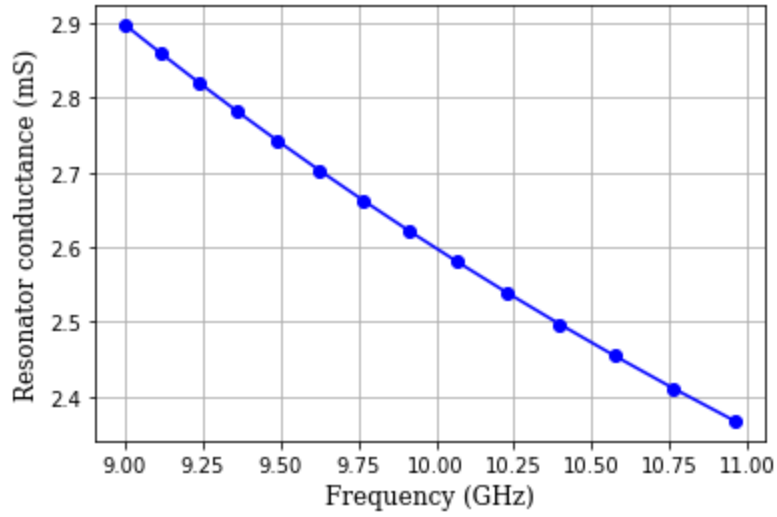


Figure 3-13: The conductance of the 10 GHz VCO resonator over a 20% tuning range.

The reference current  $I_{ref}$  (cf. Figures 3-1 and 3-2) defines the oscillator core current and by implication the oscillation amplitude.  $I_{ref}$  is chosen to obtain the maximum oscillation amplitude. This maximum amplitude can be estimated from Eq (2.1), assuming  $V_{ctrl} = V_{th}$  which is valid with good sizing of the transistors, the maximum amplitude is estimated as  $A_{max} = 0.5 \text{ mV}$ . The oscillator core current  $I_{osc}$  can be calculated from Eq (1.35) as:

$$I_{osc} = \frac{A_{max} G_{tank}}{1 - \frac{\phi^2}{14}} \quad \text{Eq 3.5}$$

The reference current is related to  $I_{osc}$  by the mirror ratio  $N$  between  $M_{1,2}$  and  $M_{5,6}$ :

$$I_{ref} = \frac{I_{osc}}{N} \quad \text{Eq 3.6}$$

To size the transistors we used  $g_m/I_d$  methodology [3]. This methodology relies on empirical data extracted from spice simulations to size the transistors. The  $g_m/I_d$  methodology provides a sizing procedure over all the inversion regions (strong, moderate, and weak inversion). The  $g_m/I_d$  characterization extracted from the transistor is independent of the width of the transistor but depends on the length. To achieve a high transition frequency, we set the length of the transistor to 60 nm, which is the smallest recommended length for RF/analog circuits. Figure 3-14 shows the transistors drain current normalized to the transistor width ( $I_d/W$ ) and the transition frequency  $f_t$  as a function of  $g_m/I_d$ . Generally, the transistor is considered in a strong inversion region when  $g_m/I_d < 8$ , in a weak inversion region when  $g_m/I_d < 20$ , and in a moderate inversion region when  $8 \leq g_m/I_d \leq 20$ .

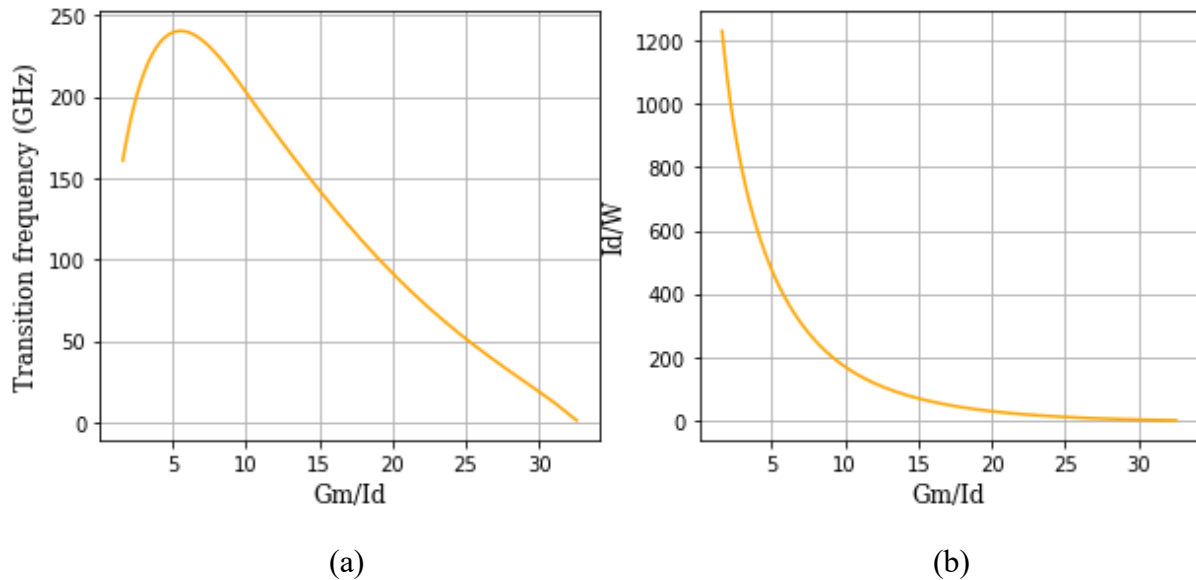


Figure 3-14: The transistor (a) transition frequency, and (b) drain current normalized to the transistor width of the transistor as a function of  $g_m/I_d$

The design of the transistor in  $g_m/I_d$  is straightforward. A  $g_m/I_d$  ratio is selected in function of the circuit specification and the desired inversion region. Then, from Figure 3-14.a, we extract the  $I_d/w$  that correspond to the selected  $g_m/I_d$ , and by defining the drain current  $I_d$  we obtain the transistor width. In our case, the transistors in the active device are sized to yield a transconductance that satisfies Eq (3.4). With Eq (2.19) and Eq (2.22), we evaluate the  $g_m/I_d$  ratios that meet the specification of the start-up condition. The upper limit for the  $g_m/I_d$  ratio is set by  $f_t$ , as the transistor should have at least a  $f_t$  two times higher than the operation frequency, and in Figure 3-14.b the  $f_t$  decreases with an increasing  $g_m/I_d$ . We preferred the moderate inversion region because it has the best tradeoff between power consumption and gain. The drain current of the transistor can be deduced from Eq (3.5).

Therefore, with the selected  $g_m/I_d$  and the defined drain current  $I_d$  we can determine the transistor width from Figure 3-14.a.

In layout, the width of the transistor is fragmented into several fingers, to decrease the value of the gate resistance. As a result, the gate thermal noise is reduced which improve slightly the phase noise. For the drain and source accesses, we adopted a staircase structure (cf. Figure 3-15) to reduce the parasitic capacitance and improve the  $f_{max}$  by 20% compared to the classical layout method [4].

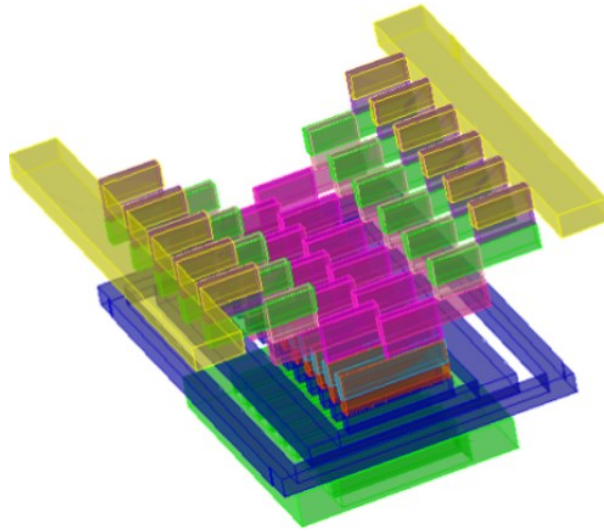


Figure 3-15: transistor layout with staircase accesses [4].

The transistors in the control circuit are sized to mirror the  $I_{ref}$  into the core oscillator with a mirror ratio  $N$ , which is defined as :

$$N = \frac{W_{1,2}}{W_{5,6}} \quad \text{Eq 3.7}$$

where  $W_{1,2}$  is the width of  $M_1$  and  $M_2$  and  $W_{5,6}$  is the width of  $M_5$  and  $M_6$ . If  $N$  is high, the value of  $I_{ref}$  will be low and thus the control circuit will have a reduced power consumption. However, the oscillation starts slowly as the low current  $I_{ref}$  will take some time to charge the capacitor  $C_b$ . In contrast, with a low  $N$  value, the current  $I_{ref}$  is higher, resulting in a faster charge of the capacitor  $C_b$  and a quick start of the oscillation. But the drawback is the increased power consumption in the control circuit. The  $N$  value was chosen between these two cases for a better compromise. The value of the integrator capacitor  $C_b$  must be high to filter the control circuit noise with an upper limit of  $2C_{eq}$  to avoid the squegging effect [5].

## 4.1. Conclusion

In this section, we have explained the transistor sizing strategy based on the  $g_m/I_d$  methodology and the circuit specifications. The methodology gives a starting point for transistor dimensions that are refined by Spice simulations to obtain optimal values.

# 5. Frequency tuning

## 5.1. 10 GHz VCO

The target frequency tuning range was 20%, which corresponds to a maximum-to-minimum capacitance ratio  $C_{max}/C_{min} = 1.44$ . The frequency control bloc combines switch capacitors for a digital control (i.e. coarse tuning) and a varactor for fine-tuning. Figure 3-16 shows the resonator of the 10 GHz VCO and the structure of the switching capacitors. The transformer-based resonator can be simplified to an LC resonator as discussed in chapter 2. The equivalent inductance and capacitance can be further simplified for  $\xi = 1$ , which is our design case. Eq (2.26) and Eq (2.27) become in this case:

$$L_{eq} = \frac{1+k}{2} L_p \quad \text{Eq 3.8}$$

$$C_{eq} = 2C_p \quad \text{Eq 3.9}$$

The equivalent inductance is  $L_{eq} = 455 \text{ pH}$  for the transformer shown in Figure 3-12.b. The equivalent capacitance must switch between  $460 \text{ fF}$  for the maximum frequency  $f_{max}$  and  $687 \text{ fF}$  for the minimum frequency  $f_{min}$ . Therefore, we can deduce the maximum and minimum values of  $C_p$  using Eq (3.9) and conclude those of  $C_s$  from  $\xi$ . The capacitor bank is divided into 15 equal units of 4-bit binary-weighted capacitors, as shown in Figure 3-16. The same capacitor bank designed for the primary is duplicated for the secondary, and both capacitor banks share the same 4-bit control signal  $V_{ctr}$ . This configuration is adopted to maintain the same capacity variation in the primary and secondary tank, to meet the design constraint  $\xi = 1$  throughout the tuning range.

As discussed in Chapter 1, Section 5.2.3, the quality factor of the capacitor bank is inversely proportional to the drain-source resistance  $R_{on}$  of the switching transistor. A wide switching transistor has a small  $R_{on}$ , which improves the quality factor, but the wide transistor has a larger parasitic capacitance that limits the tuning range. The switching transistor is designed to achieve the best compromise between quality factor and tuning range. The quality

factor in the worst case (all switches are ON) of primary and secondary quality factors are 58 and 73.5 respectively.

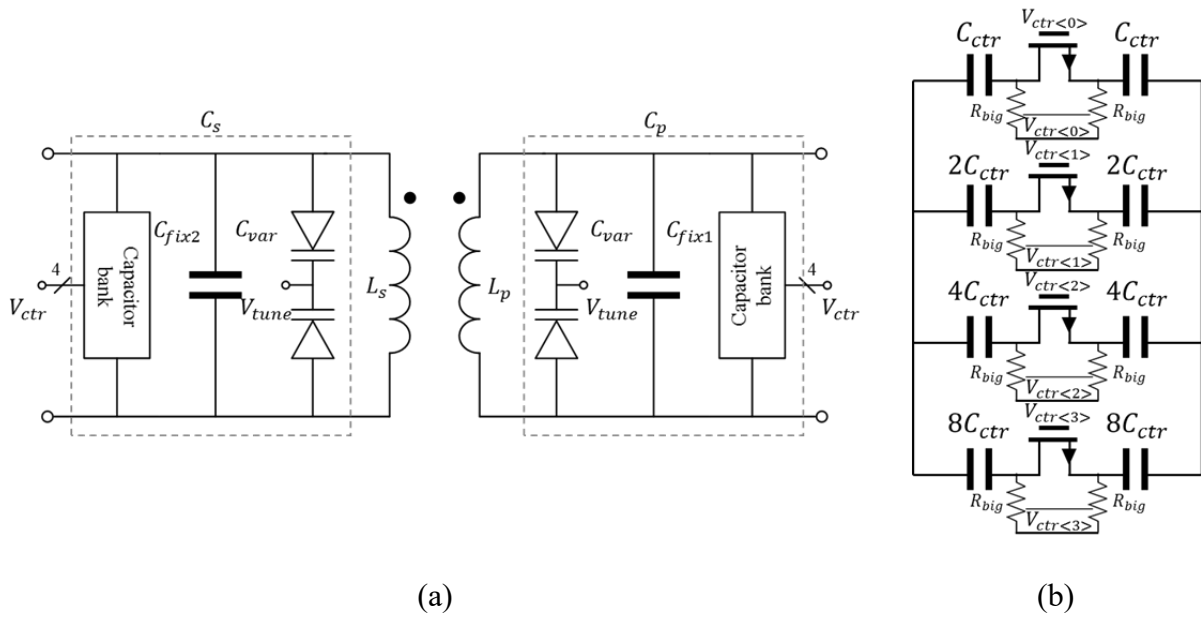


Figure 3-16: (a) The resonator model of the 10 GHz VCO (b) The 4-bit capacitor bank structure.

The varactor  $C_{var}$  was designed to cover the frequency range between two successive digital control words in the capacitor bank. Similar to the switch transistor, the tuning range of the MOS-based varactor trades with the quality factor. Indeed, a longer channel in the varactor reduces the relative contribution of the gate-drain and gate-source overlap capacitances, widening the tuning range but lowering the quality factor. The frequency interval between two successive bit words in the coarse tuning was chosen to optimize the varactor value. As with the capacitor bank, the same varactor was implemented in the primary and secondary, and both varactors share the same control voltage  $V_{var}$ . Figure 3-17 shows the post-layout simulation of the 10 GHz VCO frequency tuning range. The frequency band of each digital control word overlaps with that of the next word, ensuring continuity of tuning without blind spots. The frequency control unit covers a frequency range of 11.5 GHz to 9.14 GHz, giving a tuning range of 22.83%.

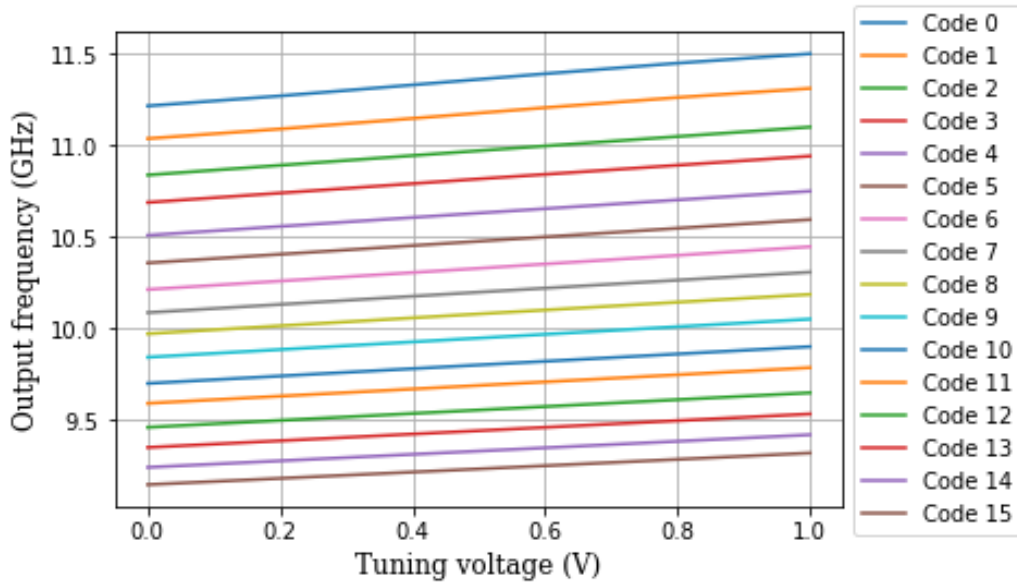


Figure 3-17: Output frequency according to the 10 GHz VCO 4-bit capacitor-bank control code.

Biasing the back gate of the transistors changes their parasitic capacitance, which affects the frequency. Figure 3-18 shows the frequency variation as a function of the back gate voltage variation of  $M_1$  and  $M_2$ . With a 1 V change in the back-gate voltage, the frequency is shifted by 30 MHz, which is about 14% of the tuning range of the varactor at that frequency. Thus, the back gate bias has a relatively small impact on the frequency tuning and can be rectified by the varactor.

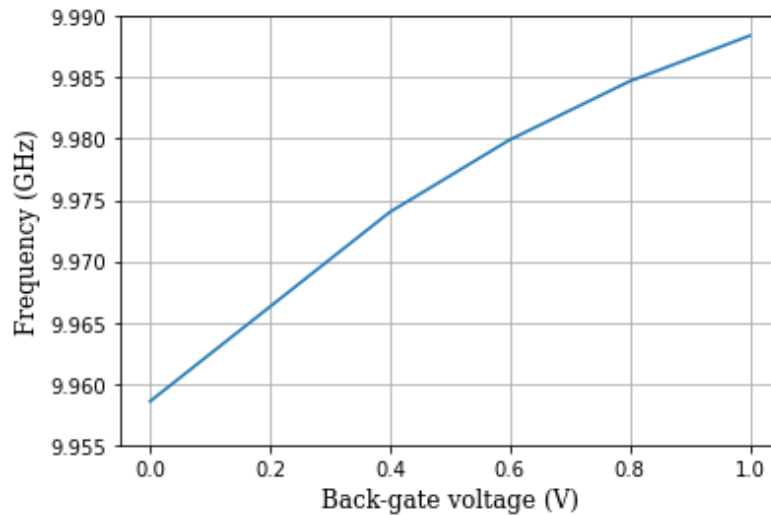


Figure 3-18: Output frequency variations according to the back-gate voltage.

## 5.2. 40 GHz VCO

At 40 GHz, parasitic elements from the layout have a significant impact on the tuning range because they are in the same order of magnitude as the resonator components.



Moreover, active device transistors introduce a parasitic capacitance to the tank that limits further the tuning range. On the other hand, the varactor at 40 GHz has a low-quality factor that increases considerably the phase noise. For instance, a MOS varactor of 7.5  $\mu\text{m}$  width has a quality factor of 13.41 at 40 GHz, which is lower than the transformer quality factor of 33.5.

We propose a varactor-less frequency control unit that uses the parasitic capacitance of the active device for fine-tuning through the back-gate biasing. Figure 3-19 shows the resonator of the 40 GHz VCO. A 6-bit capacitor bank is connected to the secondary to perform coarse frequency tuning. This capacitor bank is placed inside the transformer (cf. Figure 3-11.b) to reduce the parasitic inductance of wires, enlarging the tuning range. The capacitor bank was designed so that the frequency transition between two successive digital words is as small as possible to relax the constraint on fine-tuning. The capacitor bank is divided into 78 equal units, of which 62 units are organized into 5-bit binary-weighted groups, and the remaining 16 capacitor units are controlled by the 6<sup>th</sup> bit. The limited space inside the transformer was the reason for not implementing a 6-bit weighted binary switching capacitor. There was only room for an additional 16-unit capacitor for the most significant bit (MSB).

The parasitic capacitance of the transistors in the active device can be adjusted by their back-gate voltage in the same way as the varactors by their gate voltage. Thus, these transistors with their back-gate can be used to connect the discrete frequency points of the digital tuning. One or both transistor pairs  $M_1/M_2$  and  $M_3/M_4$  can be used with the body biasing to fine-tune the frequency. However,  $M_1$  and  $M_2$  mirror the current from the control circuit. So, varying their back-gate voltage will change the oscillator current, resulting in a variation in the VCO performance. On the other hand,  $M_3$  and  $M_4$  are only cascode transistors, so they have a lower impact on the VCO performances if their back-gate voltage is modified. Therefore, only the back gates of  $M_3$  and  $M_4$  are used for frequency tuning. Both transistors were properly sized to cover the frequency range between two subsequent coarse tuning points to ensure the continuity of frequency tuning.

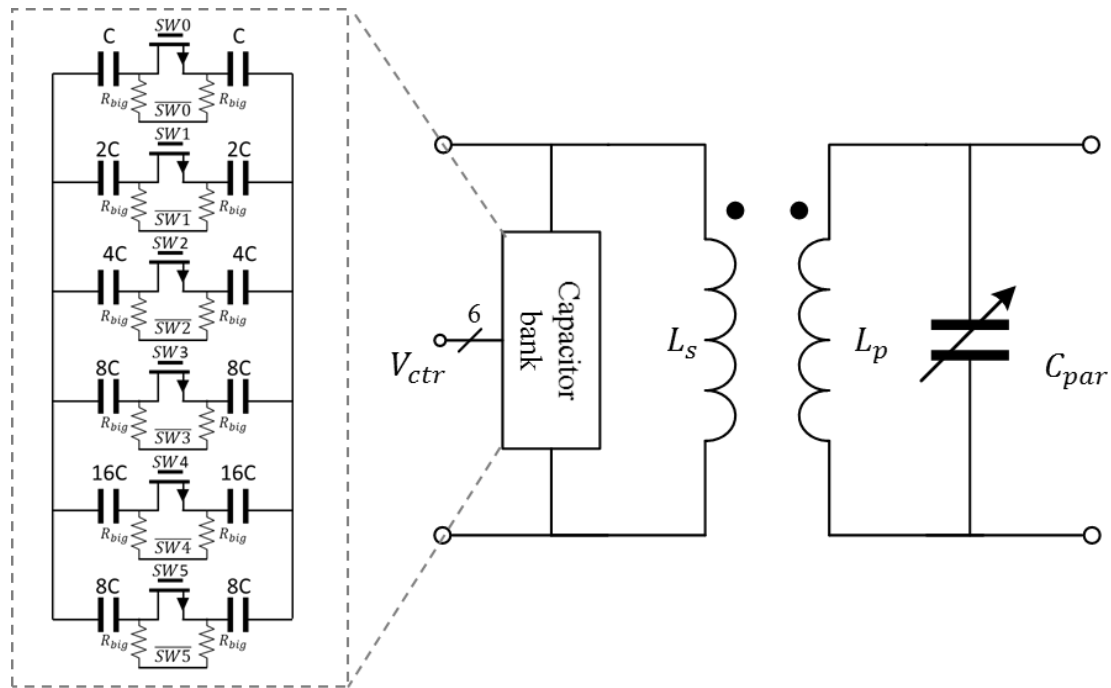


Figure 3-19: 40 GHz VCO resonator with the 6-bit capacitor bank.

Figure 3-20 shows the post-layout simulation of the frequency tuning for all possible capacitor bank configurations. The VCO covers the frequency range between 42.17 GHz and 36.3 GHz with a tuning range of 15%. The frequency band of each digital control word overlaps without any blind spots. The cluster of curves around the 40 GHz in the figure is due to some repeated configurations induce by the 6<sup>th</sup> bit.

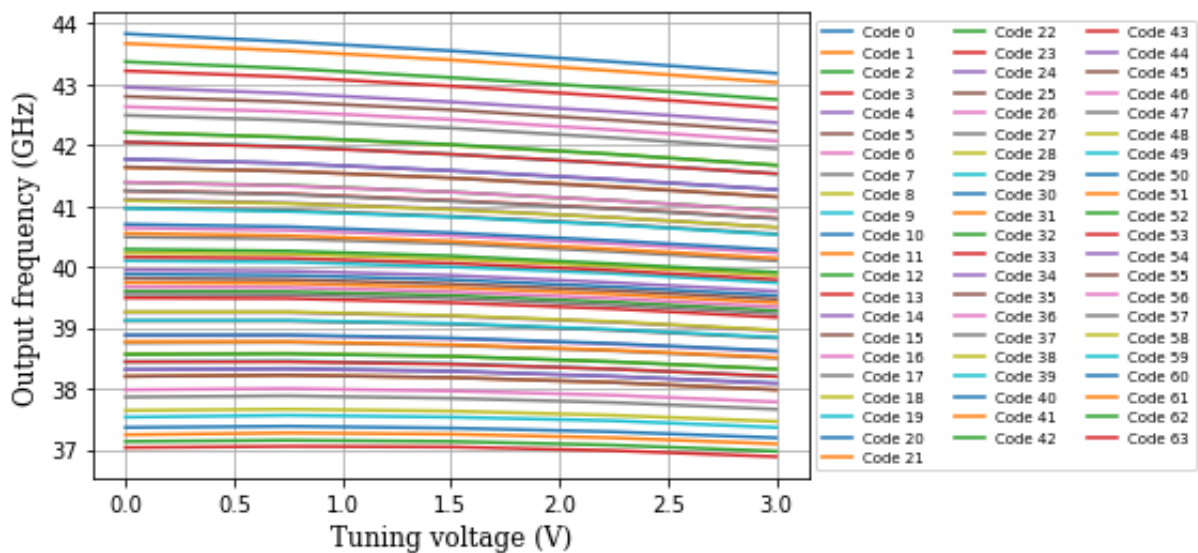


Figure 3-20: Output frequency according to the 40 GHz VCO 4-bit capacitor-bank control code.

## 6. Output buffer

### 6.1. 10 GHz VCO

To drive the output measuring instruments, we implemented an output buffer shown in Figure 3-21. The output buffer consists of a sequence of inverters where the inverter size increments after each stage. The first inverter has a small size to reduce its impact on the tuning range. The feedback resistor in the first stage centers the DC voltage at  $V_{DD}/2$  so that the inverters are sensitive to input variations.

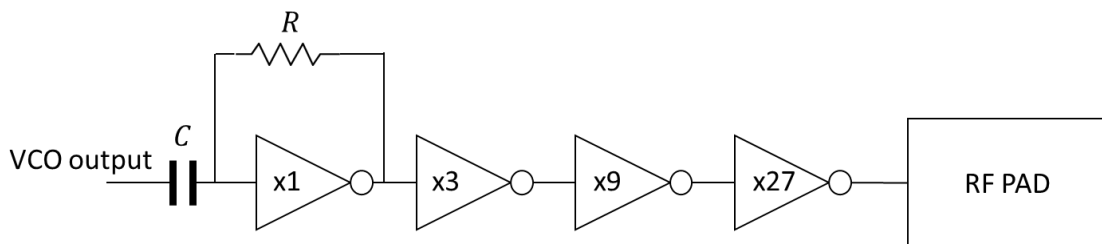


Figure 3-21: 10 GHz VCO output buffer: tapered inverter chain.

### 6.2. 40 GHz VCO

The inverter buffer was unsuitable for the 40 GHz VCO because the PMOS transistors fail to keep up with a 40 GHz signal transition. Therefore, we used a common source amplifier with an inductive load shown in Figure 3-22. The input RC filter blocks the DC voltage from the VCO and allows the bias voltage of the transistor gate to be set with an external voltage  $V_{bias}$ . The coupling capacitor has an impact on the tuning range of the VCO, so it is designed to be as small as possible. The inductance  $L_{ind}$  was sized to match a  $50 \Omega$  load at the output, and the transistor was designed to drive a  $50 \Omega$  load.

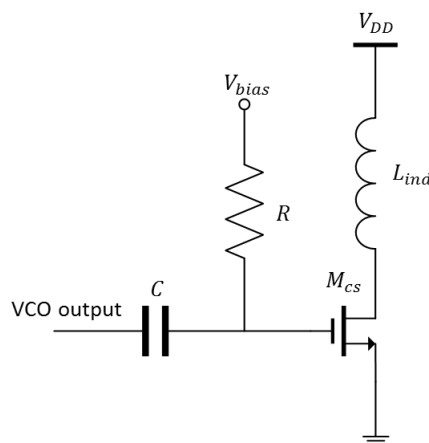


Figure 3-22: 40 GHz VCO output buffer: common source amplifier with an inductive load.

## 7. Layout implementation

This section describes the implementation of the 10 and 40 GHz VCOs in layout. We start with the implementation of the 10 GHz VCO, then we tackle the 40 GHz VCO and finally we present the full layout of the chip.

### 7.1. 10 GHz VCO

Figure 3-23 shows the implementation of the 10 GHz VCO. The active device, capacitor bank, and transformer were aligned on a horizontal axis for a symmetrical layout and an identical path for the differential signals. Thick metal layers have been preferred for routing wherever possible, to reduce ohmic losses, especially for critical connections such as the connection between the active device and the transformer. The capacitor bank was placed near the transformer to minimize wire connections and thus reduce the wire parasitics that limit the tuning range. The external digital control signals of the capacitor bank are buffered via an input inverter buffer. The 10 GHz VCO core occupies an area of  $180\ \mu\text{m} \times 460\ \mu\text{m}$ .

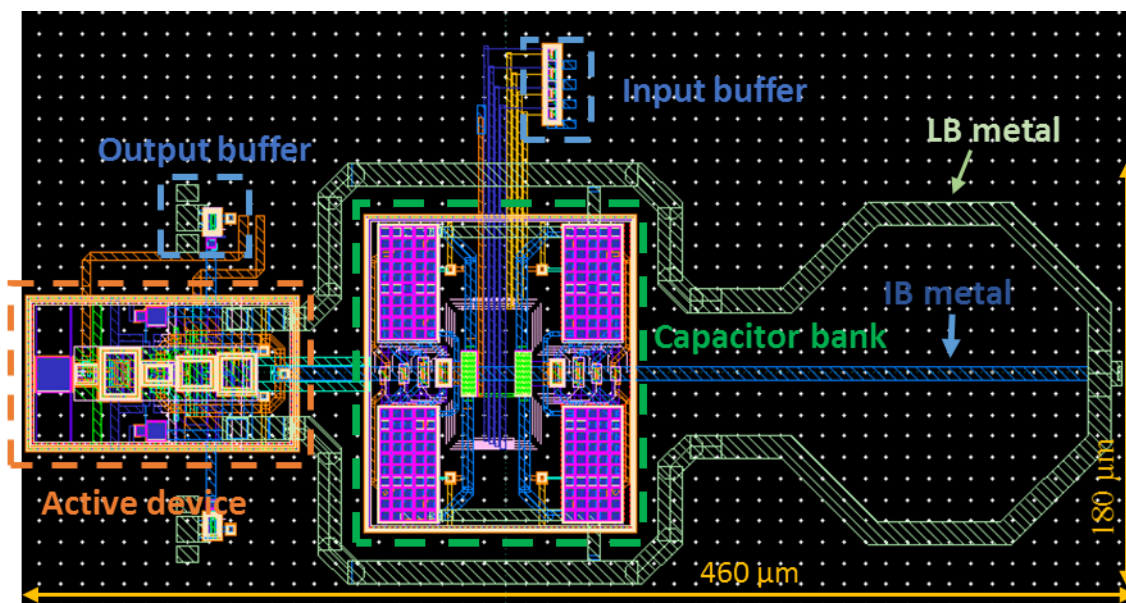


Figure 3-23: Layout of the 10 GHz VCO core.

Figure 3-24 shows the complete layout of the 10 GHz VCO. The supply voltage and the ground were distributed around the chip with a mesh structure to reduce the series resistance, respect the densities rules, and provide a decoupling capacitor to stabilize the value of  $V_{DD}$ . The supply voltage is connected to the center tap of the primary with a trapezoid shape to guide and smooth the current flow. The transformer was placed on an undoped substrate to reduce eddy current losses, the red marker shows the undoped Pwell area in the figure. The

pad ring was designed for a QFN 48 pin package, it includes decoupling capacitors for DC pads and ESD protection for all pads.

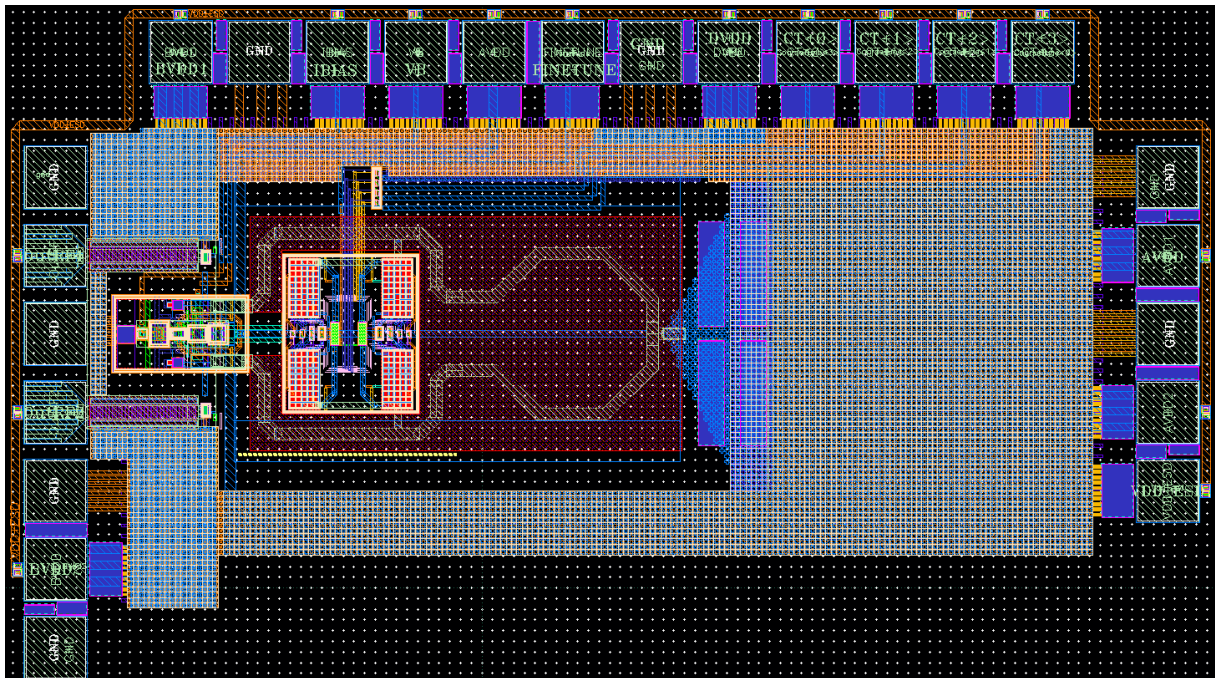


Figure 3-24: Layout of the complete layout of the 10 GHz VCO with pad ring.

### 7.1.1. capacitor bank

Figure 3-25 shows the implementation of the capacitor bank. An elementary capacitor is duplicated to build the binary-weighted switching capacitors and the fixed capacitor. The use of the same capacitor unit improves the matching and symmetry of the layout. Dummy capacitors were added to surround the useful capacitors to reduce process variation and increase matching between capacitors. The width of the switching transistors doubles at each stage, as do the switching capacitors, to scale the cutoff capacitance of the transistors with the switching capacitors for uniform capacitance change between digital control words. The digital control signals of the primary and secondary capacitor banks are combined to form a mutual control signal. The frequency control unit is surrounded by two guard rings, the inside connected to the ground and the outside connected to the supply voltage  $V_{DD}$ . These guard rings create a reverse bias diode that prevents the frequency control circuit from injecting or receiving noise from other components through substrate coupling.

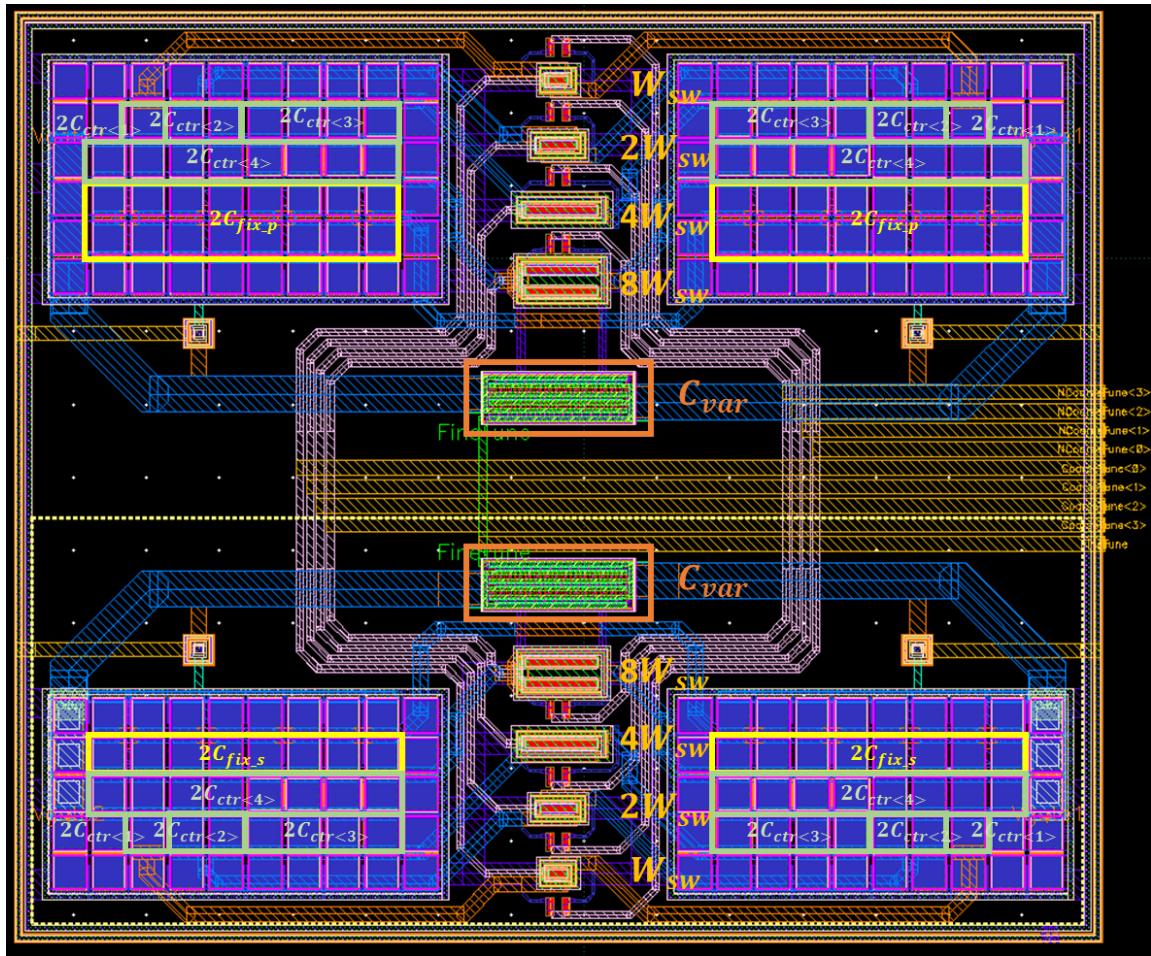


Figure 3-25: Capacitor bank layout.

### 7.1.2. Active device

Figure 3-26 shows the active device and the control circuit implementation. The transistor blocks were placed successively in a chain order to obtain a symmetrical arrangement on the vertical axis. Figure 3-27 highlights the group of transistors to match the layout. The transistors  $M_5$  and  $M_6$  should be matched with  $M_1$  and  $M_2$  for an accurate current mirroring. However, the back-gate voltage of  $M_1$  and  $M_2$  varies with an external voltage, while the back-gate voltage of  $M_5$  and  $M_6$  is connected to the ground. Therefore, the pair of transistors  $M_{1,2}$  and  $M_{5,6}$  must be placed in a separate well and thus cannot be matched in the same structure. The inaccuracy resulting from the mismatch between  $M_{1,2}$  and  $M_{5,6}$  can be adjusted in measurement through the reference current which is also an external signal. For matching, the transistors were placed in a common centroid structure wrapped with a dummy transistor. The active device and each transistor structure were surrounded by a double guard ring to protect the circuit against substrate noise coupling.

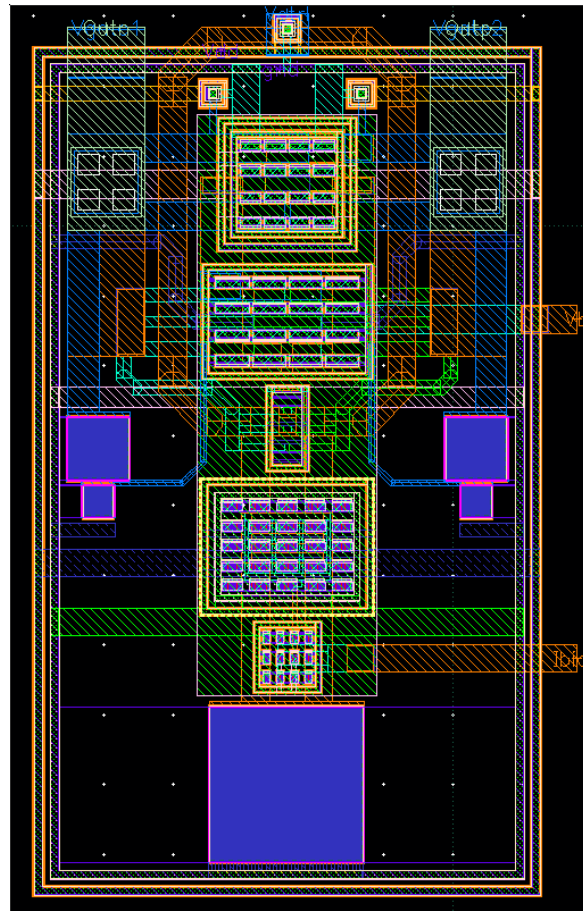


Figure 3-26: Layout of the active device.

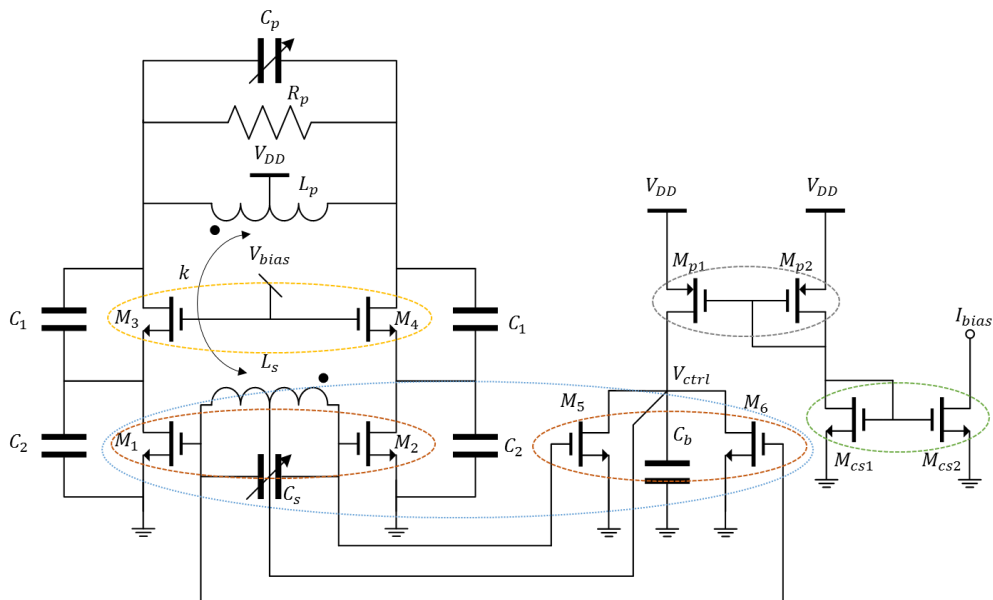


Figure 3-27: Schematic of a 10 GHz VCO with highlights on the transistors to be matched in the circuit.

## 7.2. 40 GHz VCO

Figure 3-28 shows the implementation of the 40 GHz VCO. The capacitor bank was placed inside the transformer to reduce the lead wires and improve the frequency tuning range, as discussed earlier. The use of a smaller inductor allows larger capacitances and has lower substrate capacitance due to the smaller area. A single-turn structure eliminates interwinding capacitance. The implementation of the capacitor bank and the active device in 40 GHz VCO is similar to that of the 10 GHz VCO, but it is more compact to reduce the routing wires. The VCO layout has a horizontal axis symmetry and occupies a compact area of  $15.7 \mu\text{m}^2$ .

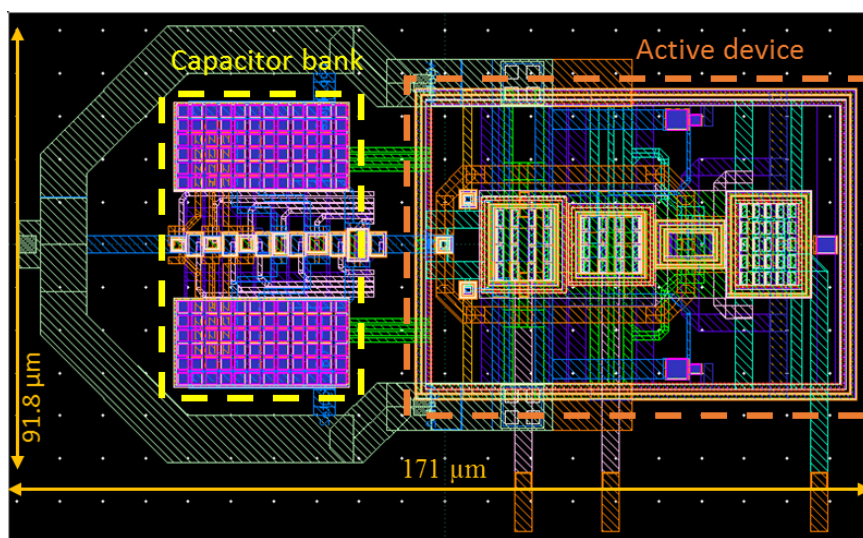


Figure 3-28: The layout of the 40 GHz VCO.

Figure 3-29 shows the complete layout of the 40 GHz VCO. The VCO was placed as close as possible to the RF output pad to shorten the connections. The pad ring differs from the one used in 10 GHz because it was designed for measurement under a probe station. This VCO was not packaged because, at the 40 GHz frequency, the wire bond must be short for the RF outputs, which cannot be done in a QFN package. The supply voltage and the ground are distributed in a mesh structure as the 10 GHz VCO. The circuit includes a Serial Peripheral Interface (SPI) to program the capacitor bank.

## 7.3. Full chip

The complete circuit with both oscillators occupies an area of  $1.13 \text{ mm}^2$  on silicon. The chip is divided between the 10 GHz and the 40 GHz VCO as shown in Figure 3-30. The 40 GHz makes the most of the area as the pads need to be large and have a certain distance for the measurement probe to be placed correctly. The supply voltage and the ground mesh fulfill



the density requirements around the VCOs, within the circuits the metal dummies were placed manually. Thick metal layers were used for leads from the circuits to the pads to minimize the resistance of these long wires.

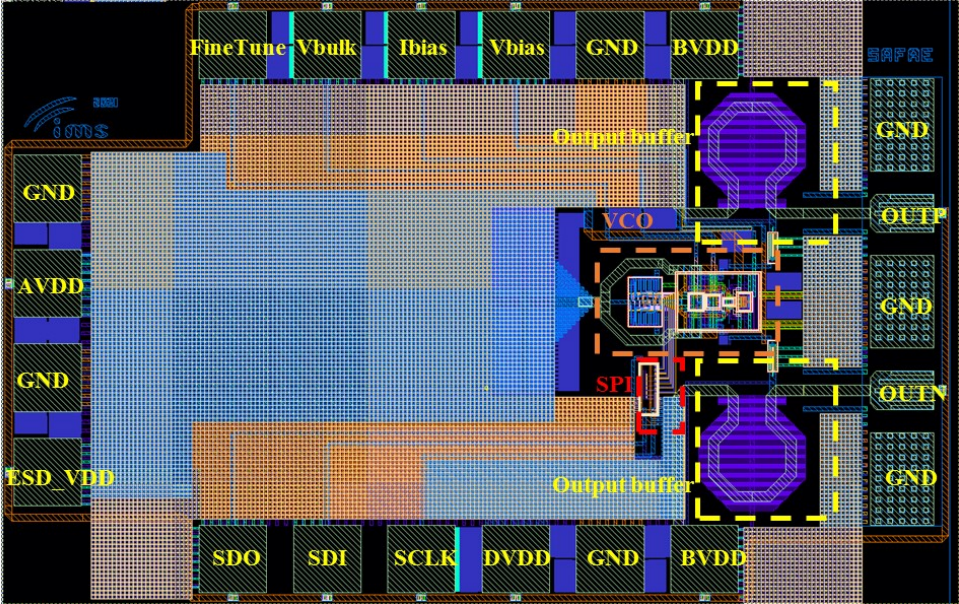


Figure 3-29: Layout of the complete layout of the 40 GHz VCO with pad ring.

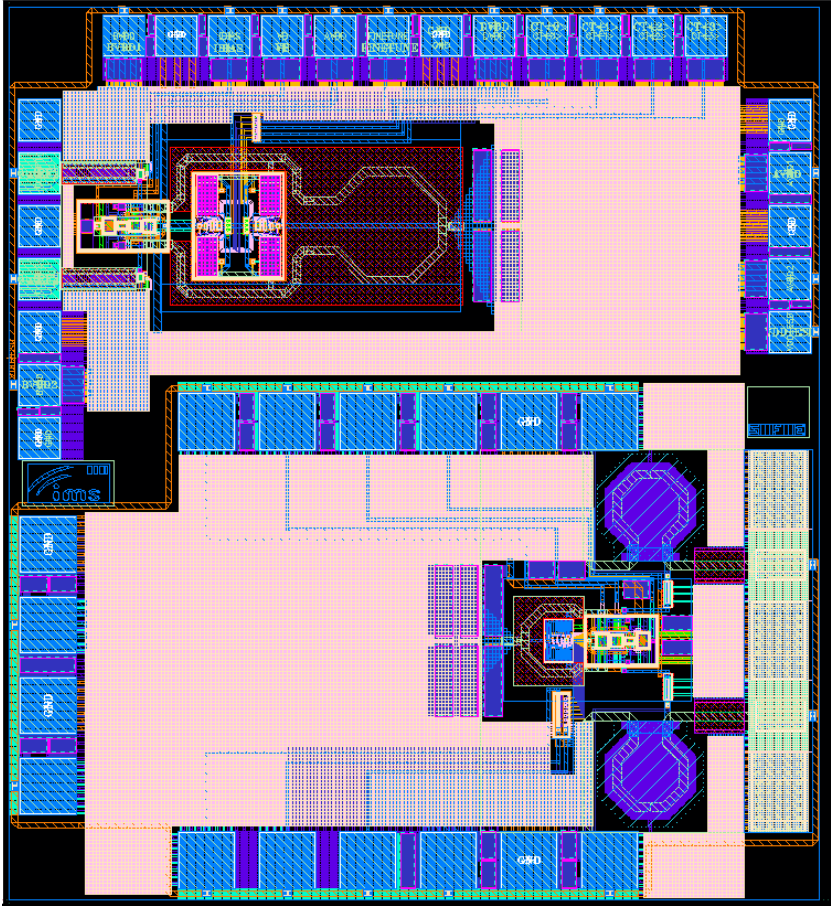


Figure 3-30: The complete layout of the implemented chip.

## 8. Conclusion

In this chapter, we presented the design strategy followed to implement the 10 and 40 GHz VCO in the 28 nm FD-SOI technology. We discussed thoroughly the difference between the interleaved transformer and the stacked transformer and concluded that in 28 nm FD-SOI the stacked transformer has a better resonator quality factor even compared to an inductor. We have detailed the design of the active device, starting from the definition of the specification to the sizing of the transistors with the gm/Id methodology.

The frequency tuning circuit design was presented for each VCO. The 40 GHz VCO uses a varactor-less frequency control unit that exploits the parasitic capacitance of the transistors and their back gate terminal to perform fine-tuning. This technique avoids the use of a poor-quality varactor and exploits the parasitic capacitance of the active device which, in other designs, is a burden for frequency tuning. The capacitor bank in the 40 GHz VCO was placed inside the horseshoe-shaped transformer to reduce the lead wire parasitics that limit the tuning range.

The following chapter presents and discusses the measurement results of the designed VCOs at 10 and 40 GHz.

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## Chapter 4:

### Measurement results

*Two tape-out were made on the proposed class-C VCO presented in chapter 2 during this thesis. This chapter presents and discusses the measurement results of the two prototypes. First, we discuss the experimental results of the first prototype which contains two 10 GHz VCOs and present the conclusions drawn from this first run.*

*Then, we present the measurement results of the second prototype that contains 10 GHz and 40 GHz VCOs that have been presented in chapter 3. For each VCO, the measurement configuration and results are presented with a complete characterization of its performance and a comparison with state-of-the-art oscillators.*

#### 1. 1<sup>st</sup> prototype: 10 GHz VCO

The proposed VCO discussed in Chapter 2 is implemented in the first prototype. Two versions of the proposed oscillators (cf. Figure 4-1) at 10 GHz have been implemented. Both oscillators share the same core oscillator, only their control circuit differs. The control circuit mirror the reference current  $I_{ref}$  to the core oscillator with a mirror ratio equal to the width proportion between  $M_3/M_4$  and  $M_1/M_2$ . For an accurate current mirroring  $M_3/M_4$  and  $M_2/M_1$  must have the same drain-to-source voltage. In Figure 4-1.b, transistors  $M_7$  and  $M_8$  were added to mimic the core oscillator structure, to have a similar drain-to-source voltage in  $M_3/M_4$  and  $M_2/M_1$ . The second oscillator (Figure 4-1.a) is implemented without the transistors  $M_7$  and  $M_8$  to be a reference. The back gate of transistors  $M_1$  and  $M_2$  is used to tune the phase noise and the power consumption in both oscillators.

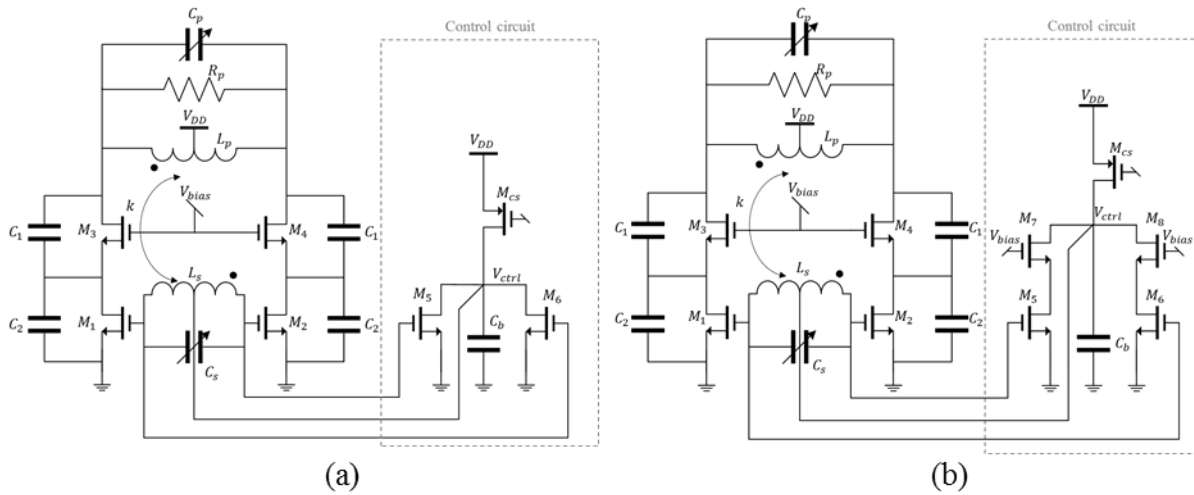


Figure 4-1: Proposed 10 GHz VCO with (a) the simple control circuit, and (b) the improved control circuit.

### 1.1. Measurement setup

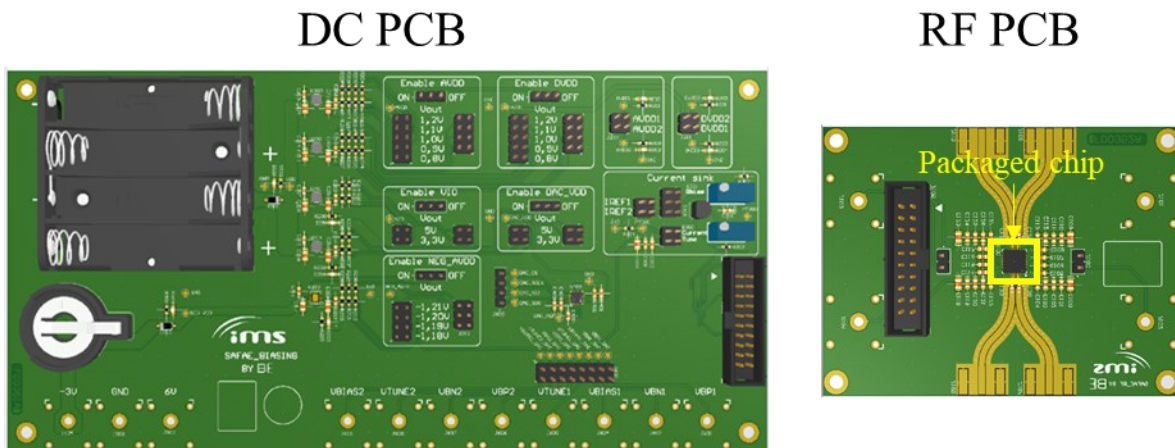


Figure 4-2: Printed circuit boards of the first prototype.

The circuit was packaged in a 32 pins Quad Flat No-leads (QFN) package. The packaged chips were mounted on an RF PCB, as shown in Figure 4-2. The supply and control voltages are generated by another PCB referred to as DC PCB in Figure 4-2. The supply voltages were generated by low noise LDO and the control signals with a built-in DAC. The control signals can be also set through external voltage supplies. The DC PCB can be alimeted directly by a voltage supply or with batteries. The latter presents a much cleaner supply voltage in contrast to the voltage supply that can inject noise coming from devices connected to the same electrical network.

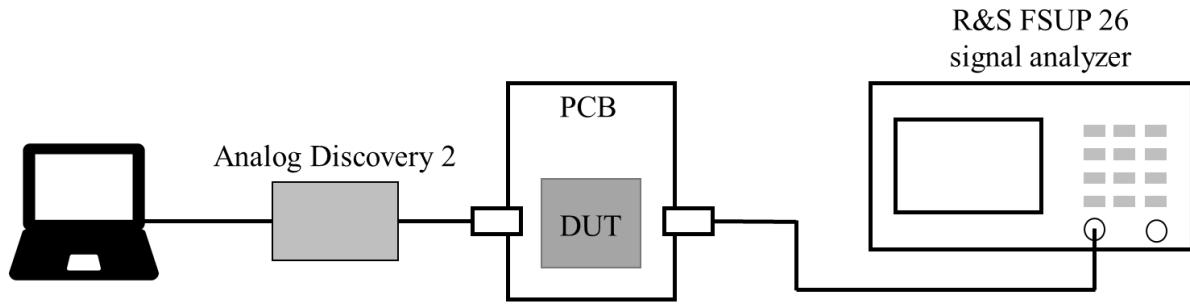


Figure 4-3: Measurement setup.

Figure 4-3 shows the measurement setup. The spectrum and phase noise of the circuit output signal was measured by Rohde & Schwarz FSUP 26 signal source analyzer. The control signals (body-biasing voltage, frequency tuning voltage ...) are programmed into the DAC by Digilent's Analog discovery 2 FPGA board. The circuits were also measured under the probe station using the DC PCB and the same signal source analyzer.

## 1.2. Measurement results

Figure 4-4 illustrates the die microphotograph. The circuit is laid down on a 0.9 mm<sup>2</sup> area where each VCO occupies a 0.04 mm<sup>2</sup> area. The following paragraph presents the measurement results of VCO with the improved control circuit (Figure 4-1.b) in a packaged chip.

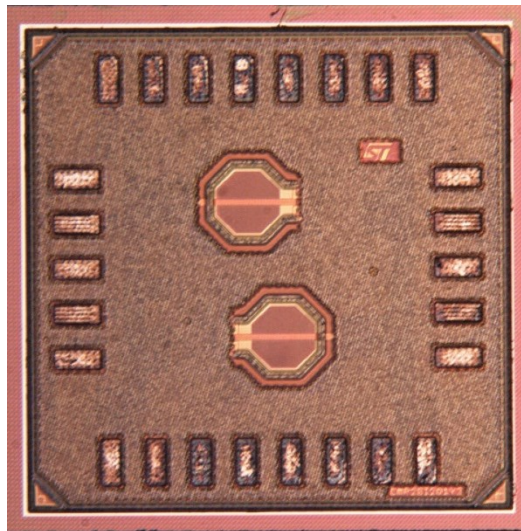


Figure 4-4: Microphotograph of first prototype 10 GHz VCO.

The power consumption of the oscillator is regulated by an external current  $I_{ref}$ . Figure 4-5 shows the evolution of the oscillator power consumption with  $I_{ref}$  under a supply voltage of 1 V. The oscillator power consumption increases proportionally with  $I_{ref}$ . The

Change in back-gate voltage ( $V_{bulk}$ ) from 0 to 1 V causes a jump in power consumption. This dependence of power consumption on the body biasing is illustrated in Figure 4-6 where the power consumption is traced as a function of the back-gate voltage for a fixed  $I_{ref}$ . The back-gate voltage in the proposed oscillator tunes the power consumption over a range of 0.65 mW.

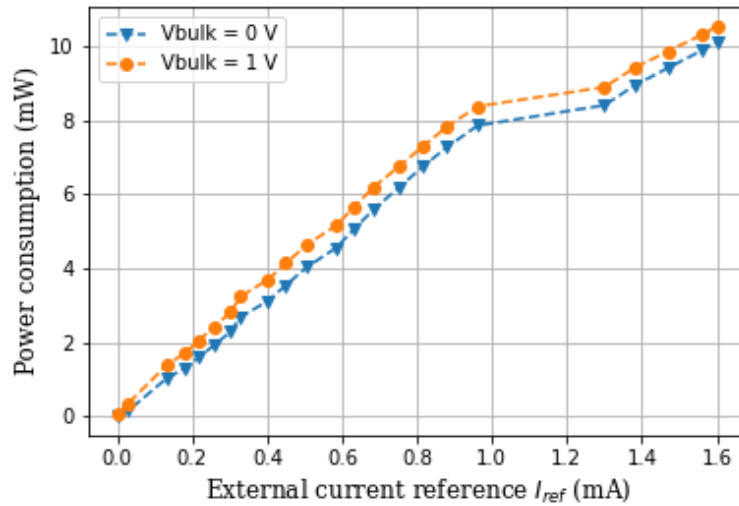


Figure 4-5: Power consumption as a function of the external current reference  $I_{ref}$ .

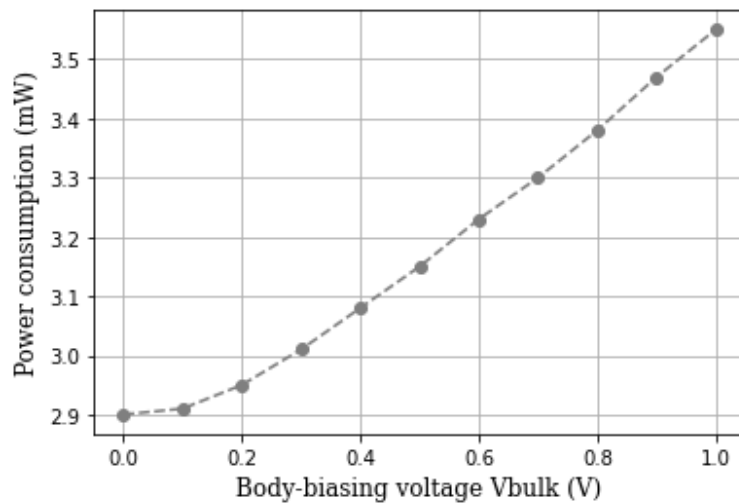


Figure 4-6: Power consumption as a function of the back-gate voltage  $V_{bulk}$ .

Figure 4-7 shows the output spectrum of the oscillator. The spectrum shows an oscillation at 2 GHz well below the expected frequency of 10 GHz. This oscillation at 2 GHz persists when the oscillator is turned off, while the output buffer is still active. This result suggests that the output buffer is the source of the observed oscillation. To suppress this parasitic oscillation, the supply voltage of the output buffer (BVDD) is set to 0.8 V to reduce its gain. Figure 4-8 shows the output spectrum with a reduced BVDD. Although the 2 GHz buffer

oscillation is suppressed, the oscillator does not oscillate even with an increased power supply and/or current reference.

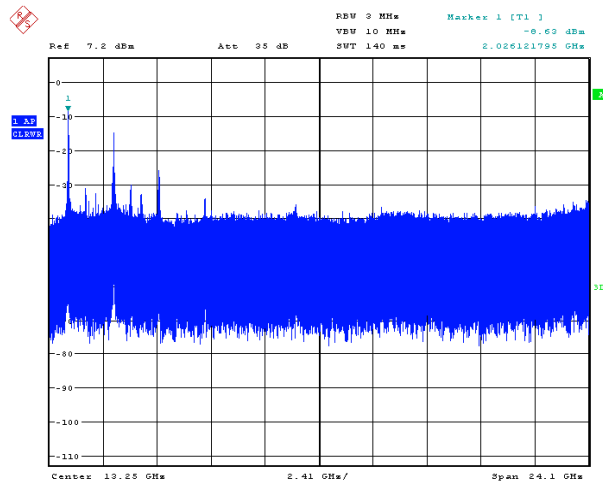


Figure 4-7: Output spectrum of the oscillator.

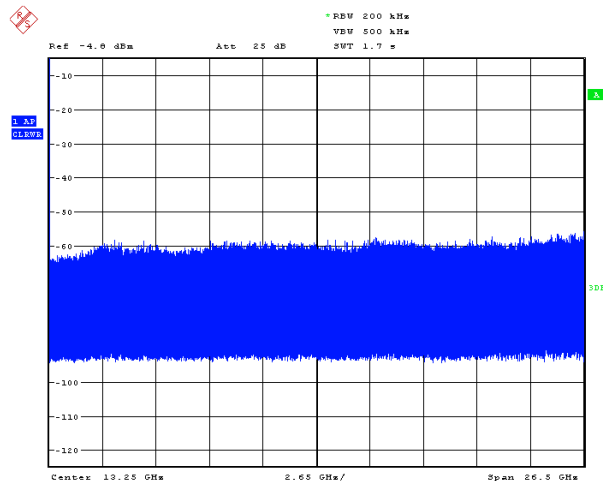


Figure 4-8: Output spectrum of the oscillator with output buffers under a supply voltage of 0.8 V.

### 1.3. Discussion

The non-oscillation of the oscillator results from a violation of one of the Barkhausen criteria. The oscillator tank contains a transformer and capacitors that provide a  $180^\circ$  phase shift. The active device is wired to have negative feedback with the tank. Thus, the positive feedback requirement is satisfied. Therefore, the non-oscillation can be linked to the violation of the second condition which is a loop gain superior to one.

To study the origin of the losses excess, we conducted a series of simulations. Starting from an ideal topology to the implanted oscillator. Among the many simulations performed,



three simulation configurations that are most significant to our analysis are presented below. The analysis focused only on whether the oscillator oscillates or not.

1. First configuration: the transformer block is connected by an ideal wire with the rest of the circuit. The oscillator in this configuration oscillates. Thus, from this simulation, the connections between the active device and the transformer are suspected to be the source of the oscillator failure.
2. Second configuration: the parasites of the wires are extracted with Cadence's layout extraction and included in the simulation. The oscillator also oscillates in this configuration in contradiction with the measurement results of the real circuit.
3. Third simulation: the connection wires are modeled with the transformer using an electromagnetic simulation. The oscillator does not oscillate which is in line with the measurement results of the real circuit.

These simulations point out two things:

1. The losses in the wire connections are the cause of the oscillator failure.
2. Cadence's layout extraction estimates are inaccurate for high frequency.

In the post-layout simulations performed before the tape-out, we relied on Cadence's layout extraction simulation to model the wire parasitics. As a result, the losses were underestimated which leads to the oscillator failure during measurement. The discrepancy between the electromagnetic model and the extracted model could be attributed to high-frequency losses, such as the skin effect, which may not be modeled in the extraction tool.

### 1.3.1. Losses in wire connections

Figure 4-9 shows the layout of the oscillator. The active device was placed close to the transformer. The idea was to make a compact layout to reduce the length of the access wire to the transformer. However, in this structure, the lines intersect, which forces the use of different metal layers. The drains of  $M_{5,6}$  were connected to the transformer primary through a thick metal layer IB (cf. Figure 2-9). But for the gates of  $M_{1,2}$  thin metal layers were used as the transistor gate does not conduct any current.

Previous simulations have shown that the lead wires should be simulated electromagnetically and considered as a part of the transformer. Table 4-1 shows a comparison between a transformer with lead wires and a transformer alone. The quality factor of the transformer decreases when the leads are connected, especially the quality factor of the

secondary. The thickness of the metal layer  $M_6$  and  $M_5$  used to connect the secondary to the active device, is about  $100\ \mu\text{m}$ . They, therefore, have a high resistivity which impacts the quality factor of the transformer. The quality factor of the resonator also depends on the magnetic coupling. The latter also degrades because the primary and secondary connection wires are not aligned. The two degradations (quality factor and magnetic coupling) decrease the quality factor of the resonator from 17.32 to 5.85. As a result, the oscillator has more losses which leads to a loop gain lower than one.

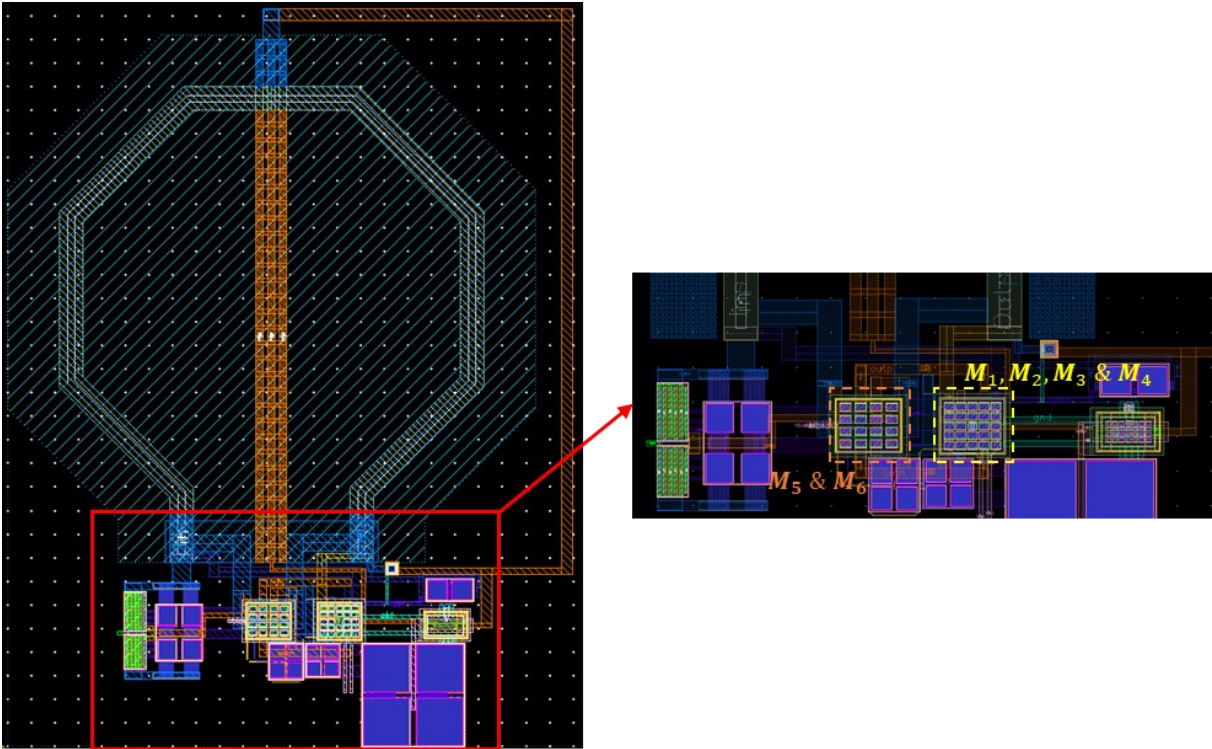


Figure 4-9: View of the oscillator layout with a zoom into the active device implementation.

Transformer		Stand-alone Transformer	Transformer with access wires
Primary quality factor	Half inductance Qp 1	17.37	10.31
	Half inductance Qp 2	17.38	10.30
Secondary quality factor	Half inductance Qs 1	7.51	1.71
	Half inductance Qs 1	7.52	3.58
Magnetic coupling		0.65	0.41
Resonator quality factor		17.32	<b>5.85</b>

Table 4-1: Performances comparison between the transformer with wire connections and the transformer alone.

### 1.3.2. Output buffer oscillations

Figure 4-10 shows the schematic of the output buffer. The feedback system in the first inverter centers the input signal at  $V_{DD}/2$ . In the absence of an input signal, the buffer's output should be at  $V_{DD}/2$  ideally. However, the supply voltage  $V_{DD}$  experiences small variations. The decoupling capacitors and the parasitic inductances in the wires create an LC tank (cf. Figure 4-11) that causes the supply voltage to oscillate [1]. The oscillation frequency is expressed as:

$$\omega = \frac{1}{\sqrt{2L_{wire}C_{decoupling}}} \quad \text{Eq 4.1}$$

These perturbations of  $V_{DD}$  cause the DC voltage  $V_{DD}/2$  to vary in the first inverter stage. The following inverters amplify these variations since the inverters have a steep voltage characteristic around their midpoint ( $V_{DD}/2$ ), and thus they are sensitive to small variations. As a consequence, the buffer outputs a periodic signal with a frequency equal to the supply voltage perturbations, instead of a DC voltage at  $V_{DD}/2$  in the ideal case. These parasitic oscillations disappear if the buffer is driven by a large input signal. This is because the magnitude variation of  $V_{DD}$  are neglected compared to the input signal amplitude.

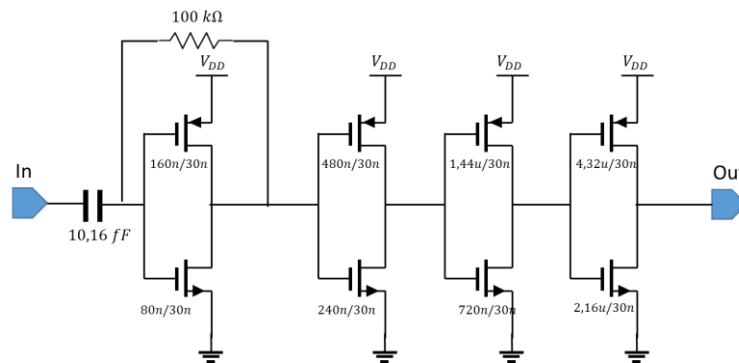


Figure 4-10: Output buffer schematic.

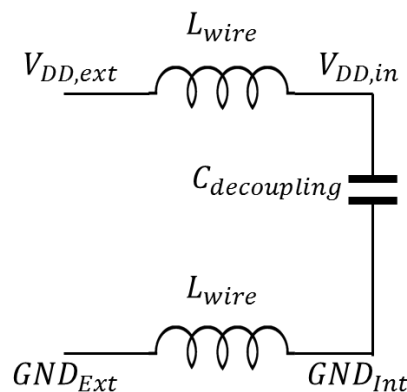


Figure 4-11: Model of the chip supply voltage and ground connections.

## 1.4. Conclusion

The measurement results verified the tunability of the power consumption by the back gate. However, the phase noise tuning could not be tested as the oscillator fail to oscillate. The two main causes of the non-oscillation are: 1) the wire losses from the use of thin metal layers; 2) Low magnetic coupling caused by the asymmetric layout. Moreover, Cadence's layout extraction inaccuracy in high-frequency miss guides us to underestimate the losses during the conception.

Although the first circuit did not function as expected, it allowed us to thoroughly examine the technology and draw up the following conclusions for the second prototype:

- All critical connections must be wired by thick metals; thin metals use is limited to digital circuits.
- Connection wires should be simulated with the transformer apart from it for accurate estimation of losses in the tank.
- Adoption of a symmetrical structure of the layout to improve the magnetic coupling of the transformer.
- Insertion of a resistor in series with the decoupling capacitor to eliminate parasitic oscillation by increasing the damping factor.

## 2. 2<sup>nd</sup> prototype: 10 GHz VCO

### 2.1. Measurement setup

The second prototype of the 10 GHz VCO was placed in a 48-pin QFN package. Figure 4-12 shows the entire microphotograph of the second prototype. The DC PCB from the first prototype is reused for the second chip to provide power and control voltages. The packaged chips were mounted on a new PCB with a socket, as shown in Figure 4-13, that allows different circuits to be tested without having to solder them to the PCB.

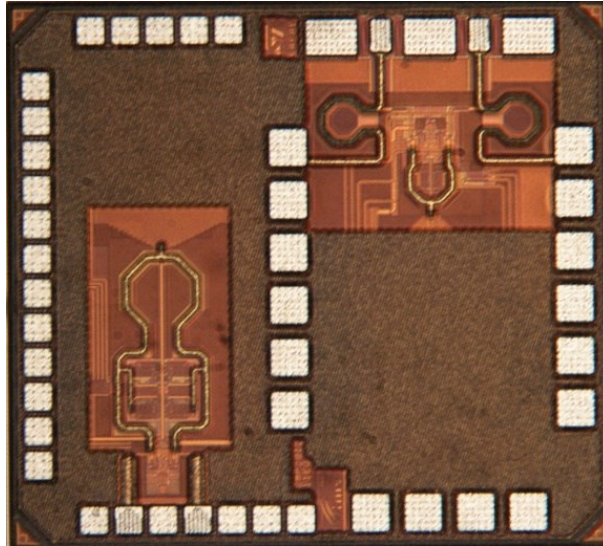


Figure 4-12: Microphotograph of the second prototype chip.

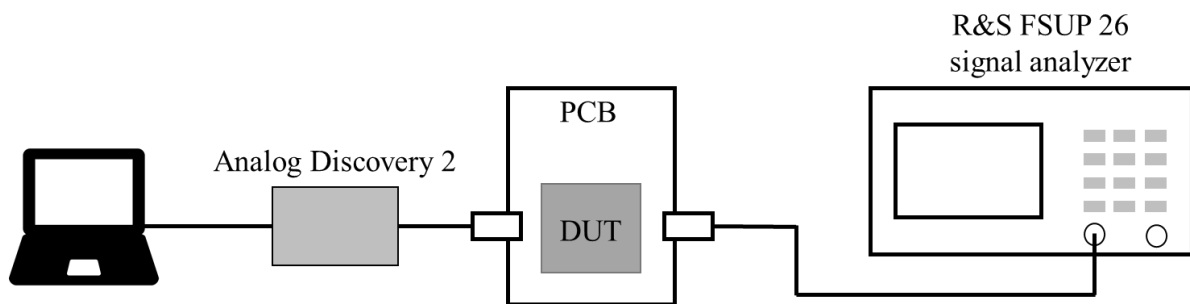
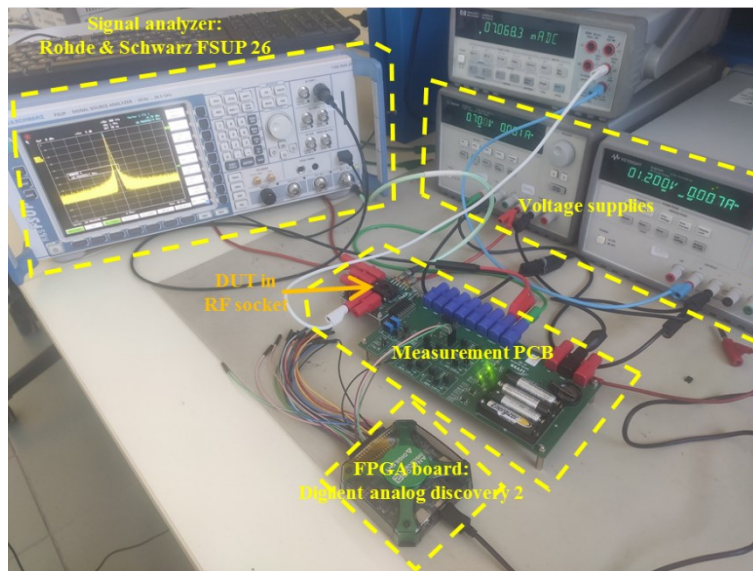


Figure 4-13: Measurement setup.

Figure 4-13 shows the measurement setup. The measurement setup is similar to the previous prototype. Rohde & Schwarz FSUP 26 signal source analyzer was used to measure the spectrum and phase noise of the VCO. The control signals (body-biasing voltage, frequency tuning voltage ...) are programmed into the DAC by Digilent's Analog discovery 2

FPGA. The control signals can be also set through external voltage supplies with the DC PCB.

## 2.2. Measurement results

Figure 4-14 shows the microphotograph of the second prototype 10 GHz VCO. The circuit is implemented in 8-metal 28 nm FD-SOI CMOS technology from STMicroelectronics. The oscillator core occupies an area of  $160\ \mu\text{m} \times 460\ \mu\text{m}$ . Figure 4-15 shows the VCO output spectrum at 11.73 GHz with an output power of -5.03 dBm.

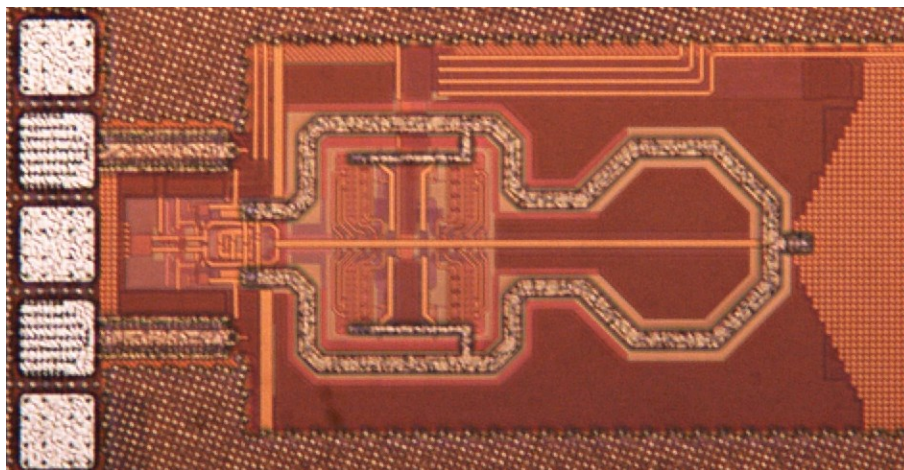


Figure 4-14: Microphotograph of the second prototype 10 GHz VCO.

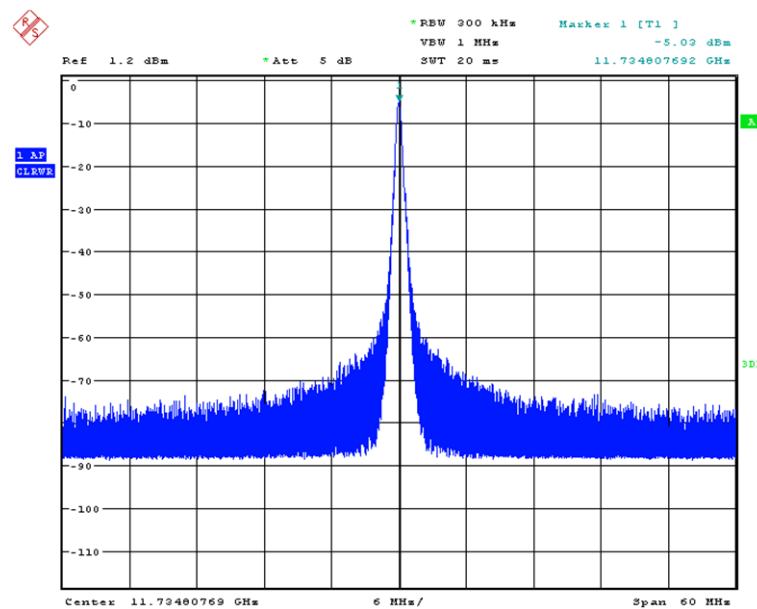


Figure 4-15: Output spectrum of the 10 GHz VCO.

Figure 4-16 shows the phase noise measured at 11.68 GHz frequency. The VCO exhibits a phase noise of -111.83 dBc/Hz and -133.81 dBc/Hz at 1-MHz and 10-MHz offset respectively, with a power consumption of 4.88 mW under a 1 V supply. The simulated and

calculated  $1/f^2$  phase noise matches the measured phase noise which validates the phase noise analysis presented in chapter 2.

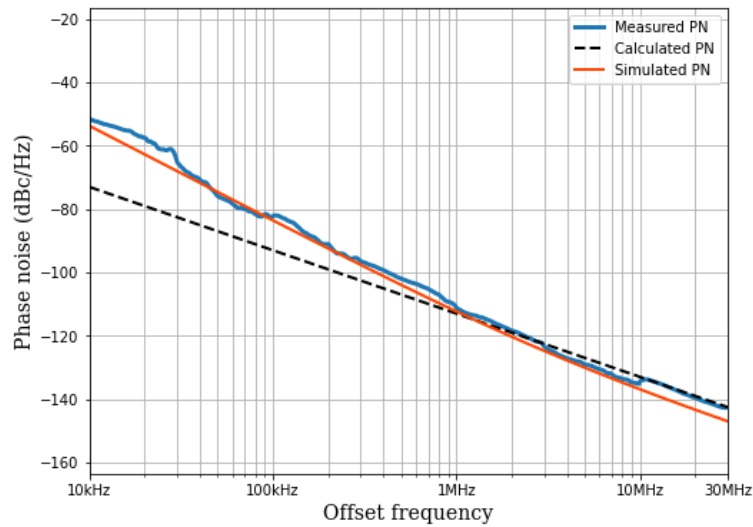


Figure 4-16: Measured phase noise of the VCO at 11.73 GHz carrier frequency.

The phase noise of the proposed VCO is adjustable by the back gate voltage of the switching transistors. Figure 4-17 shows the phase noise and power consumption as a function of back-gate voltage. The phase noise varies by 4 dB at 1 MHz offset with a 1 V change in the back gate, while the power consumption varies by 0.84 mW over the same range.

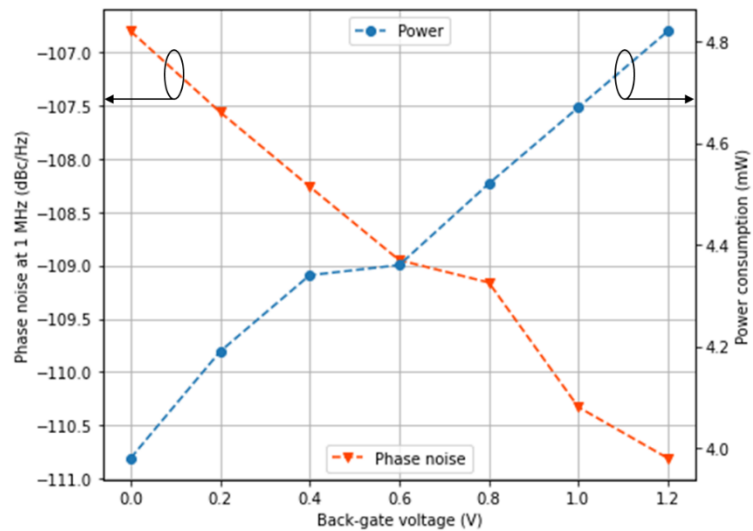


Figure 4-17: Phase noise and power consumption as a function of the back-gate voltage.

The VCO operates from 9.95 GHz to 11.73 GHz giving a tuning range of 17.82% centered around 10.84 GHz. Figure 4-18 shows the output frequency of the VCO sweeping the capacitor bank from 0 to 7 binary code. The frequency bands overlap, ensuring continuous frequency tuning without blind spots. The measured frequency tuning range is only half of

that simulated because the VCO does not oscillate with the 4<sup>th</sup> switching capacitor being activated. A possible explanation for this could be that the losses introduced by the last switching transistors are higher than what the active device can compensate for.

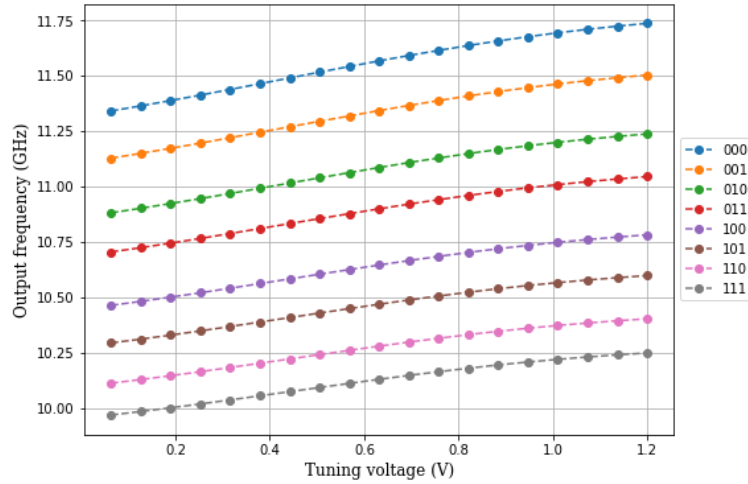


Figure 4-18: VCO frequency tuning range.

Figure 4-19 shows the phase noise of the VCO at 1 MHz offset over the frequency tuning range. We observe a significant variation in phase noise ( $\sim 3$  dBc/Hz) between the low and high frequencies of the tuning range with fixed power consumption. This variation is caused by the variation of the amplitude over the tuning range. As explained in section 3 chapter 3, the conductance of the resonator is frequency-dependent and since the amplitude is the product of the fundamental harmonic of the current and the inverse of the conductance Eq (1.20), the amplitude is also frequency-dependent.

From Figure 3-13, the conductance of the resonator decreases with the frequency tuning range, therefore with fixed power consumption, the amplitude increases with the frequency tuning range. To obtain a fixed amplitude and thus a fixed phase noise over the tuning range, the current must vary to counterbalance the frequency-dependent conductance variation. Using the back-gate of the switching transistors in the proposed VCO, we can adjust the phase noise over 4 dB range with 1.2 V (cf. Figure 4-17). Assuming linear variation of phase noise over frequency, we increment the back-gate voltage by 80 mV with each binary code in the capacitor bank. The phase noise variation is reduced from 2.86 dB to 0.5 dB with body biasing (cf. Figure 4-19), while the power consumption increases.



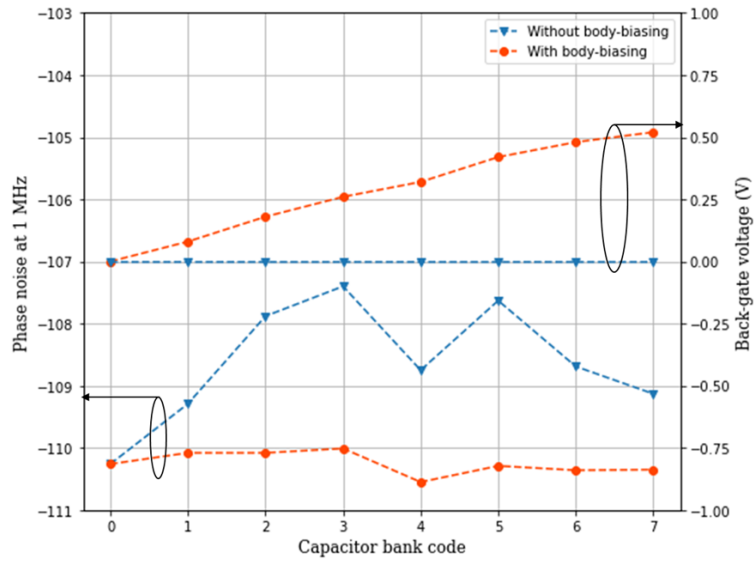


Figure 4-19: VCO phase noise over the frequency tuning range.

Thanks to the socket 5 dies were measured in the same configuration to evaluate the circuit variability. Figure 4-21 shows the circuit variability in terms of phase noise, power consumption, and output frequency for  $V_{DD} = 1 V$ , all switching capacitors are OFF and  $V_{tune} = 1.2 V$ . The circuit variation in terms of phase noise is only 0.5%, power consumption is less than 3.5% and the output frequency is only 0.24%. This demonstrates a low variability feature of the VCO architectures. However, with a small number of samples, it is important to keep in mind that these variability results are not precise but vaguely show the variability of the circuit.

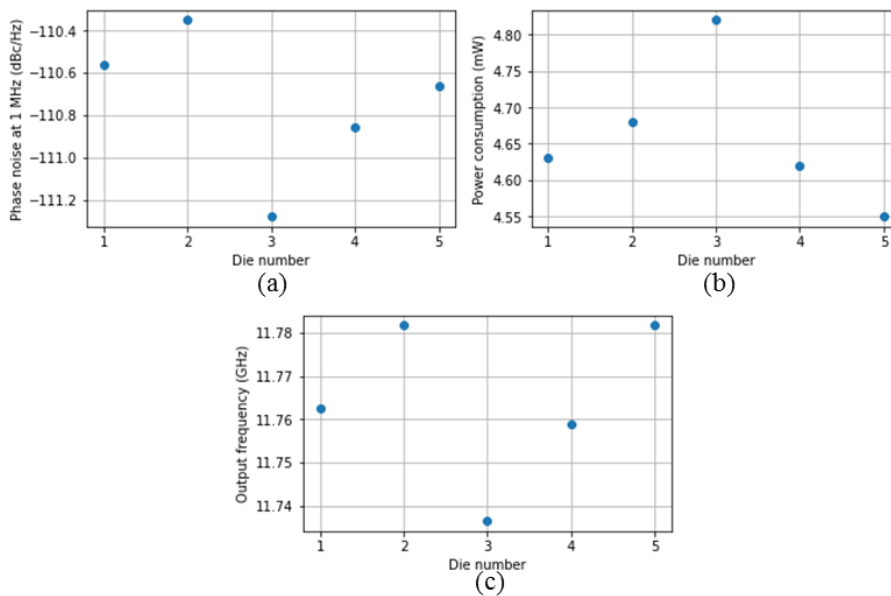


Figure 4-20: Circuit variability in terms of (a) phase noise at 1 MHz, (b) power consumption, and (c) oscillation frequency.

### 2.3. Comparison with the state-of-the-art

Table 4-2 summarizes the performance of the proposed 10 GHz VCO and compares it to state-of-the-art VCOs with FoM in Eq (1.22) as well as FoM including the tuning range FoM<sub>T</sub> in Eq (1.33).

References	This work	[2]	[3]	[4]	[5]
<b>CMOS Technology</b>	<b>28 nm FD-SOI</b>	120 nm SiGe BiCMOS	40 nm	65 nm	90 nm
<b>Frequency (GHz)</b>	<b>9.95 – 11.73</b>	9.9 – 12.45	11.74 – 12.63	7.76 – 8.62	9.5 – 11.7
<b>Tuning range (%)</b>	<b>17.82</b>	23	7.3	10.5	10.6
<b>Power (mW)</b>	<b>4.88</b>	54 - 110	13.23	10.6 – 12.3	13.3
<b>Phase noise at 1 MHz (dBc/Hz)</b>	<b>-111.83</b>	-119 - -122	-120.2	-120.8	-117.2
<b>FoM at 1 MHz</b>	<b>186.33</b>	181 – 183	190.5	188.4	185.4
<b>FoM<sub>T</sub> at 1 MHz</b>	<b>191.35</b>	188 – 190	187.8	188.82	185.9
<b>Area (mm<sup>2</sup>)</b>	<b>0.0736</b>	0.8*	0.04	0.38	0.2

\*Including the pads

Table 4-2: Comparison with state-of-the-art VCOs.

The proposed VCO achieves one of the highest FoM and FoM<sub>T</sub>, and the lowest power consumption compared to the previous work. The considerably low phase noise in [2-5] is achieved by enforcing a 3<sup>rd</sup> harmonic and/or a 2<sup>nd</sup> harmonic which distorts the output signal into a pseudo-square signal with consequent power consumption and large surface area. The power consumption of the proposed VCO is about half of the lowest power consumption of comparable VCOs, this is due to the high efficiency of the class-C topology and the local capacitive feedback network. In addition to the good performance of the proposed VCO, the cascode structure ensures the long-term reliability of the circuit, making it more suitable for space applications. Moreover, the back-gate phase noise tuning ensures a near-constant phase noise over the entire tuning frequency range with a variation of less than 0.5 dB.

### 3. 2<sup>nd</sup> prototype: 40 GHz VCO

#### 3.1. Measurement setup

Figure 4-22 shows the microphotograph of the proposed varactor-less class-C 40 GHz VCO implemented in 28 nm FD-SOI technology from ST Microelectronics. The VCO core occupies an area of 92  $\mu\text{m}$  x 172  $\mu\text{m}$ . The circuit includes a Serial Peripheral Interface (SPI) to program the capacitor bank, and an output buffer to drive the 50  $\Omega$  load of the measurement instrument and to isolate the circuit.

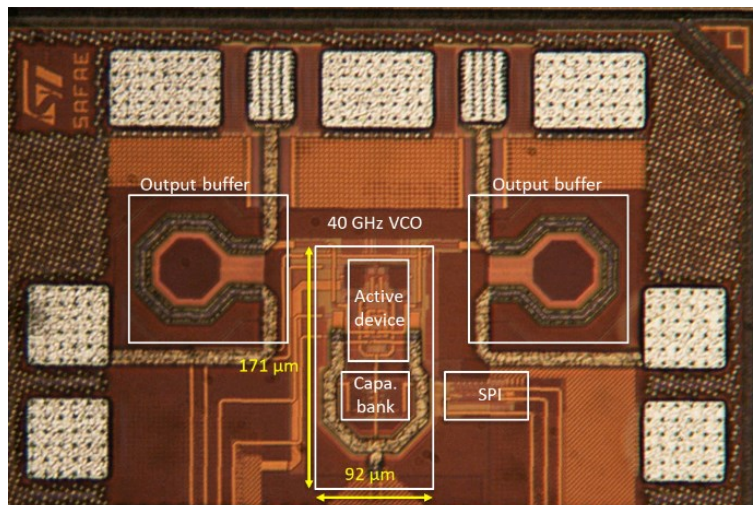


Figure 4-21: Microphotograph of the 40 GHz VCO.

Figure 4-23 shows the measurement setup under the probe station. The SPI is configured with an Analog discovery 2 FPGA board while the DC pins are biased by external supply voltages. The output spectrum and phase noise are measured with Rohde & Schwarz FSUP 26 signal source analyzer using an external mixer for measurements above 24 GHz.

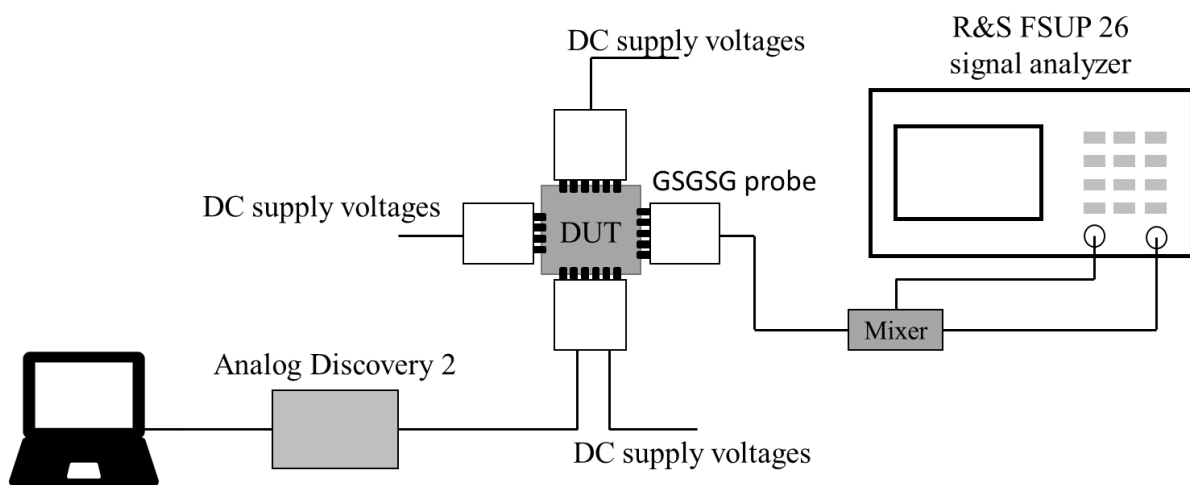


Figure 4-22: Measurement setup.

### 3.2. Measurement results

Figure 4-24 shows the output spectrum at 35.61 GHz with an output power of -6.7 dBm. The VCO consumes 7.3 mW under 1 V supply voltage.

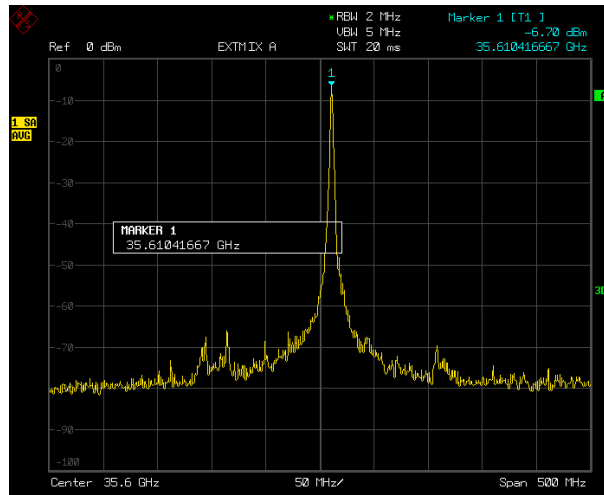


Figure 4-23: VCO output spectrum.

Figure 4-25 shows the simulated and measured frequency tuning range. The VCO covers a tuning range from 35.58 GHz to 42.36 GHz by sweeping the capacitor bank code from 0 to 39, resulting in an FTR of 17.1%. The circuit lead wires were EM-simulated with Momentum, thus parasitic elements were adequately estimated resulting in a good agreement between simulation and measurement results. The observed discrepancy in the tuning range at binary code 31 could be attributed to the additional 6th switching capacitor in the capacitor bank that is not binary weighted with the other 5 switching capacitors, causing a larger discrepancy when activated.

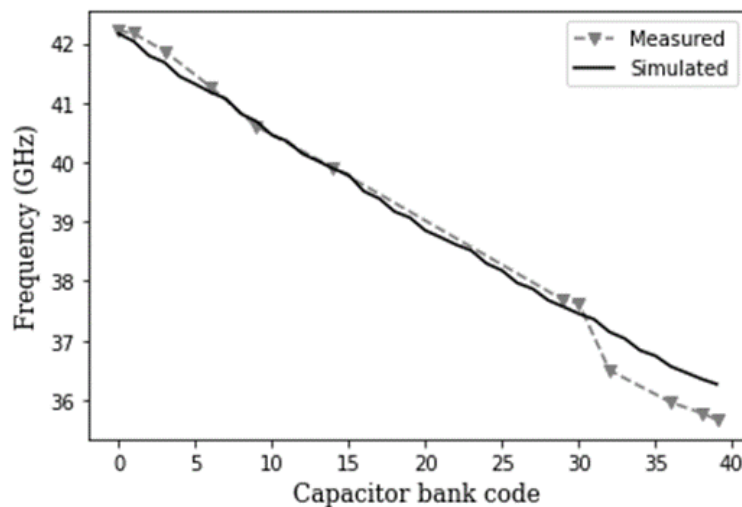


Figure 4-24: The measured and simulated tuning range of the designed VCO.

DC probes were used to program the SPI block. These probes contain an integrated decoupling capacitor. During the measurement, we noticed that the SPI clock signal is affected by this decoupling capacitor, which causes the SPI to malfunction. Therefore, we could only access a part of the binary codes of the capacitor bank.

Figure 4-26 depicts the frequency shift as a function of the back-gate voltage. The fine-tuning range varies between each capacitor bank code. This variation is due to the changes in the impedance of the resonator over the frequency tuning range, resulting in a change in amplitude, which in turn changes the bias of the transistor. Therefore, the parasitic capacitance changes from one code to another. The average frequency shift is around 140 MHz. However, in some configurations, the frequency shift is less than 100 MHz which might create some frequency gaps.

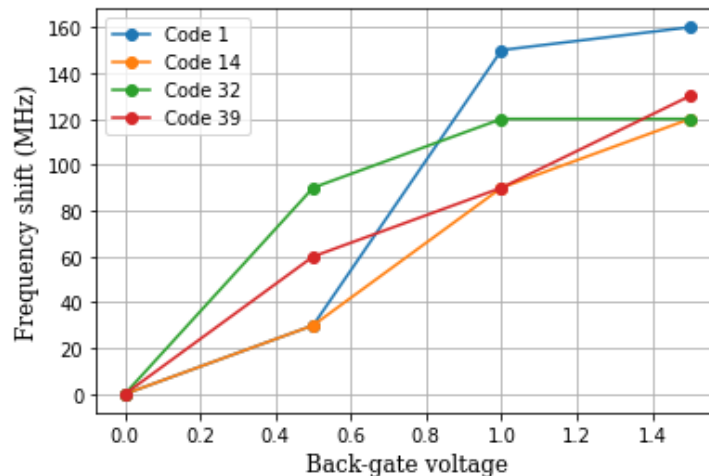


Figure 4-25: Measured frequency shift for four capacitor bank codes (0, 14, 32, and 39) as a function of the back-gate voltage.

Contrary to expectations, the frequency tuning by the back-gate is limited to 1.5 V, not 3 V as in the simulation. Above 1.5 V the frequency decreases instead of increasing or staying at the same value. This inconsistency may be due to the transistor models not being developed to accommodate this type of application with the back gate. Despite these promising results, frequency tuning through the back-gate must be limited to a 50 MHz frequency range for robust tuning.

The phase noise of a free-running VCO is very sensitive to external source noise. Figure 4-27 depicts the measured phase noise. The observed bump is due to the spectral signature of the measuring equipment and other equipment connected to the power grid. These low-frequency noises are converted by the oscillator to the carrier frequency. By disconnecting some unnecessary equipment, the observed bump in the phase noise is reduced.

The VCO achieved a phase noise of -88.33 dBc/Hz at 1 MHz and -112.84 dBc/Hz at 10 MHz offset from 35.58 GHz carrier frequency.

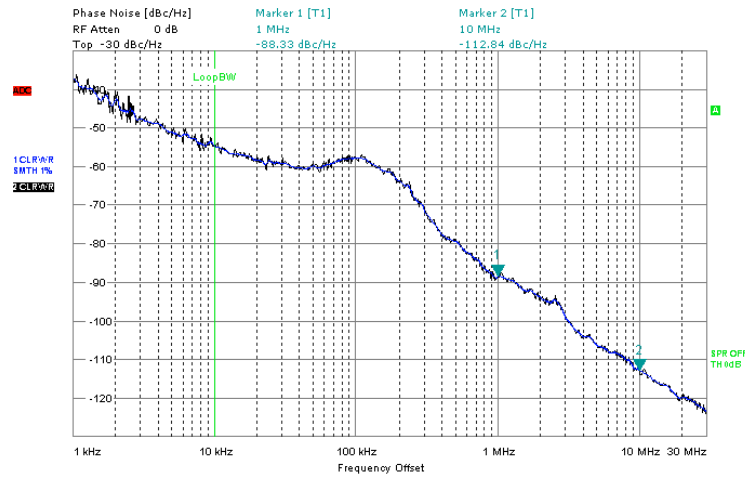


Figure 4-26: Measured PN at 35.58 GHz with a power consumption of 7.3 mW.

### 3.3. Comparison with the state-of-the-art

Table 4-3 compares the proposed varactor-less 40 GHz VCO to the other state-of-the-art 40 GHz VCOs. The VCOs are compared with the  $FoM$  expressed in Eq (1.22) as well as  $FoM$  including the tuning range  $FoM_T$  expressed in Eq (1.33).

References	This work	[6]	[7]	[8]	[9]	[10]
<b>CMOS Technology</b>	28 nm FD-SOI	90 nm	65 nm	130 nm	40 nm	130 nm
<b>Frequency range (GHz)</b>	35.6 – 42.3	37.6 – 43.4	55.1 – 70.4	39.6 – 41.8	31.8 – 40.8	34.5 – 45.4
<b>Tuning range (%)</b>	17.1	14	15.3	5.4	24.8	27
<b>Power (mW)</b>	7.3	19	21.5	28.84	20	12
<b>PN @ 1MHz (dBc/Hz)</b>	-88.33	-89	-92.2	-94.8	-93.5	-95
<b>FoM @ 1MHz</b>	170.72	168.9	174.86	172.1	172.5	176.25
<b>FoM<sub>T</sub> @ 1MHz</b>	175.38	172.1	178.56	166.8	180.4	184.9
<b>Area (mm<sup>2</sup>)</b>	0.015	0.075	0.0075	0.018	-	0.03
<b>Tuning mechanism</b>	Body-biasing / switching capacitor	Variable inductor	Switching transmission line	Varactor	Single inductor/ varactor	Switching varactor/ negative capacitance

Table 4-3: Comparison with the state-of-the-art VCOs.

The proposed VCO has the best-in-class power consumption compared to [6-10], thanks to the removal of the high-loss varactors. This low power consumption ensures a lower operating temperature. This lower operating temperature increases the meantime before the failure of the circuit, which is critical when it comes to satellite payloads. Also, the proposed VCO exhibits a notable tuning range for a varactor-less architecture. The here proposed VCO provides long-term reliability through HCI reduction with the cascode structure. While this feature is mandatory for satellite applications, the addition of cascode transistors increases the circuit noise sources. Together with the low power consumption, it directly impacts the VCO phase noise, as can be seen in Figure 4-27 and Table 4-3. However, the global PN is still in line with satellite communication requirements, and the proposed VCO reaches state-of-the-art figures of merit regardless of the trade-off that has been done to ensure long-term reliability to the circuit.

## 4. Conclusion

This chapter summarizes the measurement results of the thesis work. The first prototype of 10 GHz VCO was presented, although it did not work as expected, it allowed us to study in-depth the topology and its implementation to improve the second prototype. The second prototype 10 GHz VCO presents a good compromise between all performances, with one of the highest  $FoM_T$  and a competitive  $FoM$ . The proposed VCO exhibits a phase noise of -111.83 dBc/Hz at a frequency offset of 1 MHz from an 11.73 GHz carrier. The phase noise variation over the tuning range is reduced to 0.5 dB through body biasing. The VCO provides a frequency range of 9.95 GHz to 11.73 GHz, resulting in a 17.8% tuning range covered by a 3-bit control word and analog control voltage tuning the varactors. The frequency bands overlap, providing a continuous frequency tuning range, allowing direct use in a phase-locked loop. Thanks to the efficiency of the class-C topology, the oscillator has one of the lowest power consumption, consuming only 4.88 mW at a supply voltage of 1V. These performances, along with the long-term reliability provided by the cascode structure, respond to the requirements of high-speed communications in satellite communications.

In the third section, we have presented a 40 GHz varactor-less class-C VCO in 28 nm FD-SOI technology. The VCO topology exploits the bias of the transistor body to fine-tune the frequency avoiding low-quality factor varactors. The measured tuning range is 17.1%, centered around 38.95 GHz. The circuit features also an active device in cascode structure that improves the reliability of the circuit against HCI and TDDDB and increases the lifetime of

the circuit. The VCO exhibits a phase noise of -88.33 dBc/Hz at an offset frequency of 1 MHz and -112.84 dBc/Hz at 10 MHz from a carrier frequency of 35.58 GHz. The power consumption of the 40 GHz VCO is also one of the lowest compared to previous work, with 7.3 mW draws from a 1 V supply. The resulting FoM and FoM<sub>T</sub> are 170.72 dBc/Hz and 175.38 dBc/Hz respectively, in line with the state-of-the-art VCOs.

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## Chapter 5:

### Conclusion and perspectives

#### 1. Conclusion

Satellite communications play an essential role in providing broadband communications on a global scale, even in remote areas. The new space age aims to democratize access to space through affordable launches and satellites, leading to new applications and financial opportunities. This is driving the space industry to explore new avenues, such as CMOS technologies, that can help reduce costs and improve performance. However, the design of satellite transceivers presents challenges related to reliability, power consumption, and phase noise.

In this thesis, we present a new VCO topology that meets the requirements of high data rate satellite communications in the mm-wave and Ku-band frequencies. In the first chapter, we analyzed the mechanisms of phase noise in harmonic oscillators and its tradeoffs with power consumption, frequency tuning, and noise sources. We evaluated these tradeoffs in different oscillator topologies and selected the most efficient topology, which is the high swing class-C topology.

In chapter 2, we studied the high swing class-C topology and the reliability issues present in LC oscillators, then we presented a custom VCO topology in 28 nm FD-SOI technology that enhanced the oscillator reliability against HCI and TDDDB with a cascode active device. The proposed topology includes local capacitor feedback to improve the oscillator transconductance, power efficiency, and phase noise. The body biasing, a specificity of FD-SOI technology, was exploited to fine-tune the frequency of the mm-wave VCO and adjust the phase noise of the Ku-band VCO. We provide a depth study of the phase noise and transconductance of the proposed topology.

Chapter 3 presents the design methodology followed to implement the proposed oscillator in 10 and 40 GHz carrier frequencies. We compared the interleaved transformer and the stacked transformer. The stacked structure in 28 nm FD-SOI technology emerged as the transformer implementation with the highest resonator quality factor. We detailed the sizing of the transistors in the active device following the gm/Id methodology. The varactor-less

mm-wave oscillator topology was presented with the horseshoe-shaped transformer to maximize the tuning range.

Chapter 4 presents the measurement results of the thesis. The 10 GHz VCO exhibits an excellent trade-off between all performances, achieving one of the highest  $FoM_T$  of 191.35 dBc/Hz and a competitive  $FoM$  of 186.33 dBc/Hz. The VCO prototype demonstrates phase noise tuning by body biasing, which is employed herein to reduce the phase noise variation over the tuning range to less than 0.6 dB. These performances, along with the long-term reliability provided by the cascode structure, respond to the requirements of high-speed communications in satellite communications. Despite its limitations, measurement results from the 40 GHz VCO validate the frequency fine-tuning concept by the back gate. The millimeter-wave oscillator achieved one of the lowest power consumptions with 7.3 mW drawn from a 1 V supply and has a phase noise of -88 dBc/Hz at 1 MHz.

## 2. Perspectives

The results of this thesis work validate the proposed topology of a class C VCO with a good performance trade-off, long-term reliability, and adjustable phase noise. Yet, there is still room for improvement of the topology in terms of phase noise and radiation hardening. Some suggestions for improvement of the proposed topology are:

- **Hybrid topology between class-F and class-C for low phase noise.**

The transformer-based resonator of the topology can be fully exploited to lower the phase noise by adopting a class-F<sub>2,3</sub> topology. Figure 5-1 shows the suggested hybrid class-F/C VCO. The same configuration is kept only the capacitor bank needs to be adjusted to create a common mode resonance at the 2<sup>nd</sup> harmonic and 3<sup>rd</sup> differential harmonic resonance with the second resonance frequency of the transformer-based resonator. Common mode resonance improves the  $1/f^3$  phase noise because it creates a resistive low path for the 2<sup>nd</sup> harmonic current to flow instead of the capacitive path that creates close-up phase noise according to the Groszkowski effect [1]. The 3<sup>rd</sup> harmonic distorts the signal into a square pseudo-signal with a tweaked ISF that converts less noise into phase noise, as outlined in Chapter 1 section 6.3.

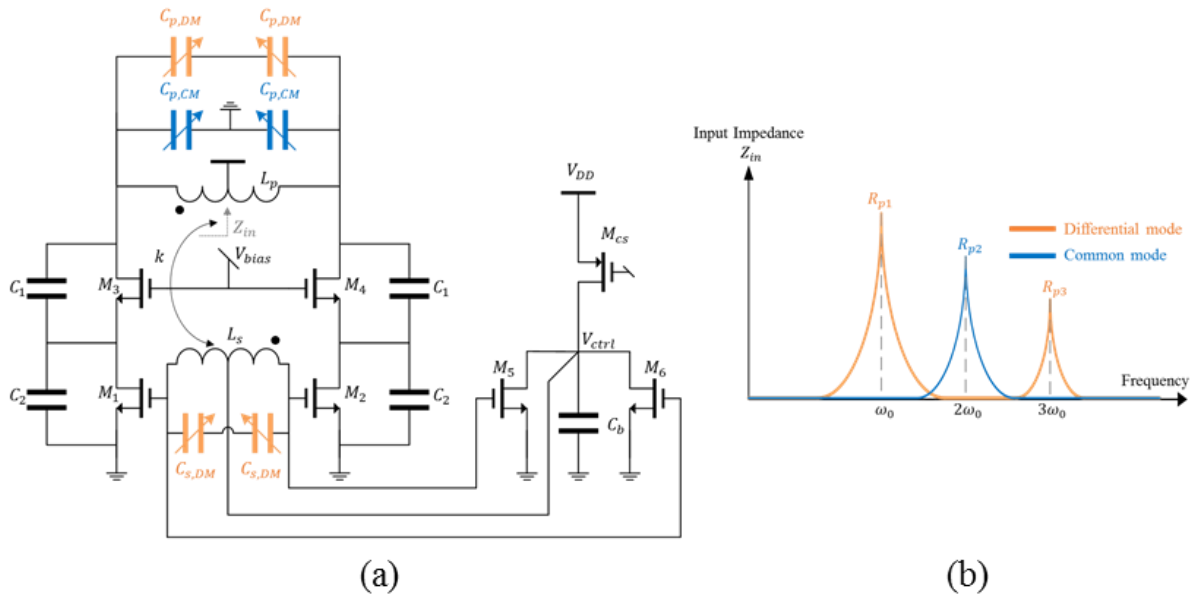


Figure 5-1: (a) The proposed hybrid class-F/C (b) Input resonator impedance.

- **Radiation hardening and application adjustability.**

The demonstrated feature of phase noise adjustability through body biasing suggests several courses of action. One could be radiation hardening against Total Ionization Dose (TID). FD-SOI has demonstrated its merits against single-event effects (SEE). However, radiation-induced positive charge trapping in the thick oxide box remains a problem, even with a thin layer. These positive charges induce always a negative shift of the threshold voltage in the transistors, which will result in the case of an oscillator in a variation of the current and thus a degradation of the phase noise performance. With body biasing, the threshold shift can be corrected to nullify the impact of TID. In fact, [2] demonstrates full attenuation of 50 krad irradiation with a back-gate bias voltage of -3 V on an NMOS transistor. Figure 5-2 shows a proposed topology to cancel irradiation effects with a feedback loop.

In the VCO topology, LVT transistors are replaced by RVT transistors to use a negative gate voltage. The peak detector retrieves the amplitude of the oscillation which is then sent to a voltage comparator that evaluates the amplitude against a reference voltage  $V_{ref}$ . The output of the comparator is fed back to the back gate of transistors  $M_1$  and  $M_2$  through a low pass filter to reduce noise. The control loop will correct any performance drift caused by the TID and thus harden the circuit against radiation. LVT transistors can also be used, but in this case, the circuit must be designed with a back gate voltage of 3 V, so that the feedback loop compensates for the threshold shift by decreasing the back gate voltage. Furthermore, the

reference voltage determines the performance of the oscillator, so with at least two values of  $V_{ref}$  we can adjust the oscillator performances. One  $V_{ref}$  to determine the optimal phase noise performance of the oscillator and the other to reduce power consumption. This adjustment allows for optimizing the performance of the oscillator according to the application. For instance, satellite-to-earth communication requires a carrier frequency with high spectral purity, since the communication is established over long distances and experiences different attenuation mechanisms in the atmosphere (absorption, refraction, polarization...). By contrast, inter-satellite communication operates in the cosmic void and relatively short distances. Thus, it tolerates a much higher phase noise from the VCO. Dynamic control over the oscillator phase noise optimizes communication in terms of power efficiency.

Further research could also be conducted to determine the effectiveness of the circuit reliability against an irradiated environment.

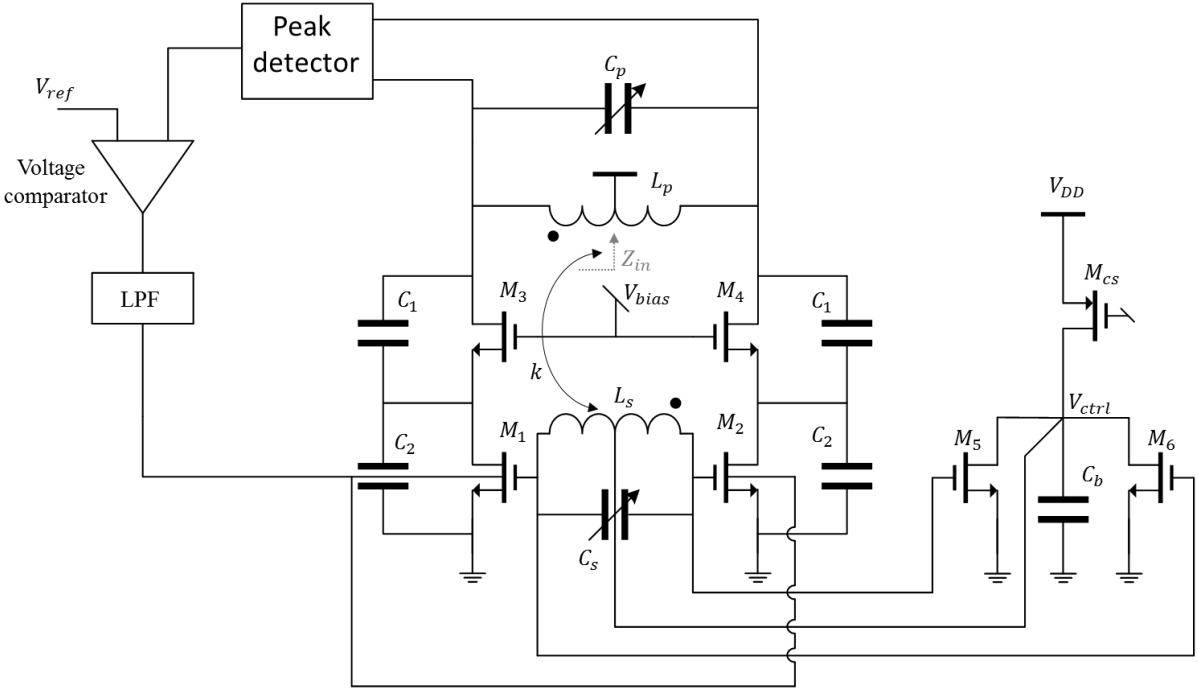


Figure 5-2: Proposed VCO with radiation hardening feedback loop.

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# List of publications

## International conference

Yann Deval, Andreia Cathelin, Raphaël Guillaume, Ayoub Ait Ihda, Herve Lapuyade , Francois Rivet, “Benefits of an FD-SOI Feature: Optimal Power Budget of Wireless Links through Phase Noise Tuning”, *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 2019.

Ayoub Ait Ihda, Yann Deval, Hervé Lapuyade, François Rivet, Matthieu Gastaldi, Stephane Rochette, “A 40 GHz Varactor-less Class-C VCO with 17.1% Tuning Range and Long-Term Reliability in 28nm FD-SOI for Satellite Communications” *The 29th IEEE International Conference on Electronics Circuits and Systems (ICECS)*, Oct 2022, Glasgow, United Kingdom.

Ayoub Ait Ihda, Yann Deval, Hervé Lapuyade, François Rivet, Matthieu Gastaldi, Stephane Rochette, “A 40 GHz Varactor-less Class-C VCO with 17.1% Tuning Range and Long-Term Reliability in 28nm FD-SOI for Satellite Communications” *International Conference on Analog VLSI Circuits (AVIC)*, Nov 2022, Hiroshima, Japan.

## National conference

Ayoub Ait Ihda, Yann Deval, Hervé Lapuyade, François Rivet, Matthieu Gastaldi, Stephane Rochette, “Oscillateur en classe C à 10 GHz, à faible bruit et large plage d’accord en fréquence, avec une fiabilité à long terme et un réglage du bruit de phase par la grille arrière”, *Journées Nationales Microondes (JNM 2022)*, 2022.