Phase Change Memory (PCM) for High Density Storage Class Memory (SCM) Applications

Giusy Lama

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Mémoires à Changement de Phase (PCM) pour les applications de Mémoire de Classe de Stockage (SCM) à haute densité

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Présentée par :

Giusy LAMA

Direction de thèse :

Véronique SOUSA Ingénieur HDR, CEA LETI	Directrice de thèse
Gabriele NAVARRO Ingénieur docteur, CEA LETI	Co-encadrant de thèse

Rapporteurs :

Luca LARCHER
PROFESSEUR, Université de Modene
Abdelkader SOUIFI
PROFESSEUR DES UNIVERSITES, INSA Lyon

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Véronique SOUSA INGENIEUR HDR, CEA LETI	Directrice de thèse
Ahmad BSIESY PROFESSEUR DES UNIVERSITES, Université Grenoble Alpes	Président
Luca LARCHER PROFESSEUR, Université de Modene	Rapporteur
Abdelkader SOUIFI PROFESSEUR DES UNIVERSITES, INSA Lyon	Rapporteur
Philippe BOIVIN INGENIEUR DOCTEUR, STMicroelectronics	Examinateur

Invités :

Innocenzo TORTORELLI
INGENIEUR, Micron
Gabriele NAVARRO
INGENIEUR DOCTEUR, CEA LETI

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Abstract - Résumé

TITLE: Phase-Change Memory (PCM) targeting high density Storage Class Memory (SCM) applications

Abstract:

The amount of data generated is increasing exponentially in the last years and is expected to reach 175 Zettabytes by 2025 [1]. This data explosion is pushing memory technologies to their performance and density limits. The access and writing speed of storage memory has emerged as the primary bottleneck of modern systems due the growing speed of data elaboration. The current memory hierarchy consists of a top layer, closest to the processor, which is faster and expensive, and by a bottom layer, that is more dense but slower. Storage Class Memory (SCM) was created to reduce the performance and cost barriers between storage and memory, in particular between DRAM and NAND Flash. PCMs are considered the best candidate for SCM thanks to the good scalability, the high endurance, fast switching time and multilevel cell capability [2]. Material engineering becomes essential to meet the demand for low cost, high programming speed and endurance of SCM applications. In particular, it necessitates the investigation of novel alloys capable of rapid crystallization while maintaining the material stability during the multiple transitions between the amorphous and crystalline phases that occur during the device lifetime. The objective of this thesis is the investigation of innovative phase-change materials to target SCM applications, understanding the failure mechanisms and which parameters can limit the reliability of the device.

Speciality: Nanoelectronics and Nanotechnology

Key Words: Phase-Change Memory, Storage Class Memory, reliability, phase-change materials.

Thesis work prepared at: CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France.

TITRE: Mémoires à Changement de Phase (PCM) pour les applications de Mémoire de Classe de Stockage (SCM) à haute densité

Résumé:

La quantité de données générées augmente de façon exponentielle ces dernières années et devrait atteindre 175 Zettabytes d'ici 2025 [1]. Cette explosion des données pousse les technologies de mémoire à leurs limites de performance et de densité. La vitesse d'accès et d'écriture de la mémoire de stockage est devenue le principal goulot d'étranglement des systèmes modernes en raison de la vitesse croissante d'élaboration des données.

La hiérarchie mémoire actuelle est constituée d'une couche supérieure, la plus proche du processeur, plus rapide et coûteuse, et d'une couche inférieure, plus dense mais plus

lente. La mémoire de classe de stockage (SCM) a été créée pour réduire les barrières de performances et de coûts entre le stockage et la mémoire, en particulier entre la DRAM et la NAND Flash.

Les PCM sont considérés comme les meilleurs candidats pour le SCM grâce à leur bonne scalabilité, leur haute endurance, leur temps de commutation rapide et leur capacité multi-niveaux [2].

L'ingénierie des matériaux devient essentielle pour répondre à la demande de faible coût, de vitesse de programmation élevée et d'endurance des applications SCM. En particulier, cela nécessite l'étude de nouveaux alliages capables de cristalliser rapidement tout en maintenant la stabilité du matériau lors des multiples transitions entre les phases amorphe et cristalline qui se produisent pendant la durée de vie du dispositif.

L'objectif de cette thèse est l'étude de matériaux innovants à changement de phase pour cibler les applications SCM, en comprenant les mécanismes de défaillance et quels paramètres peuvent limiter la fiabilité du dispositif.

Spécialité: Nano Électroniques et Nano Technologies

Mots Clés: mémoires à changement de phase, Mémoire de Classe de Stockage, fiabilité, matériaux à changement de phase.

Thèse préparée au sein du:

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[1] David Reinsel-John Gantz-John Rydning, J Reinsel, and J Gantz. The digitization of the world from edge to core. Framingham: International Data Corporation, 2018.

[2] Scott W Fong, Christopher M Neumann, and H-S Philip Wong. Phase-change memory-towards a storage-class memory. IEEE Transactions on Electron Devices, 64(11):4374?4385, 2017.

List of Acronyms

Acronym	Designation
1R	One Resistor
1T1C	One-Transistor One-Capacitor
1T1R	One-Transistor-One-Resistor
AIST	$Ag_4In_3Sb_{67}Te_{26}$
ALD	Atomic Layer Deposition
BEOL	Back-End-of-Line
C2C	cycle-to-cycle
D2D	device-to-device
DRAM	Dynamic Random Access Memory
FeRAM	Ferroelectric Random Access Memory
GST	GeSbTe
HDD	Hard Disk Driver
IPCM	Interfacial Phase Change Memory
I-V	Current-Voltage curve
MIEC	Mixed Ionic-Electron Conduction
MIM	Metal-Insulator-Metal
MIT	Metal-Insulator Transition
MIT	Metal-Insulator Transition
MLC	Multilevel Cell Capability
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MRAM	Magnetic Random Access Memory
M-SCM	Memory-type Storage Class Memory
MTJ	Magnetic Tunneling Junction
NDR	Negative Differential Resistance
NVM	Non-Volatile Memories
OTS	Ovonic Threshold Swith
PCM	Phase Change Memory
PMem	Persistent Memory
PV	Program and Verify
PVD	Physical Vapor Deposition
R-I	Resistance-Current curve
RRAM	Resistive Random Access Memory
R-T	Resistivity-Temperature curve
SCM	Storage Class Memory
SL PCM	Superlattice Phase Change Memory
SRAM	Static Random Access Memory
S-SCM	Storage-type Storage Class Memory
STT-RAM	Spin-Transfer Torque Magnetic Random Access Memory

TEM	Transmission Electron Microscopy
TMR	Tunnel Magneto-Resistance
V-XPoint	Vertical Cross-Point
XPoint	Cross-Point
XRD	X-Ray Diffraction

Introduction

Our digital society is based on data. The word *data* was used for the first time in English in the 1640s with the meaning of "fact given or granted". In the XVIIs, data was employed by the scientific community to indicate experimental or tangible events. In the world of information technology, for the first time *data* was reported as "transmittable and storable information by which computer operations are performed" in 1946 [1]. Raw data is unidentifiable as information, for this reason we collect, measure, clean, analyze, share or transfer data: the information achieved from these operations consents to generate knowledge. In order to ensure this process, the data must be stored on physical media. The first means found for data collection is the Ishango Bone from the Upper Paleolithic, where some scratches in the bone were used as raw data [2]. Later, with the birth of writing, tablets, papyri and finally, books became the new form of mass storage. The birth of internet and of search engines in the 1990s determined the last revolution ensuring data access to anyone in possession of a computer.
Today the internet users are 4.95 billions [3], a huge number, constantly growing, linked to an ever-increasing flow of data supported by smart connected devices, artificial intelligence and internet of things. Indeed, the amount of data generated is increasing exponentially in the last years and is expected to reach 175 Zettabytes by 2025 (Fig. 3) [4]. Data have been presented as the new oil of the digital economy [5], since companies are exploiting data to be more competitive, more productive and to create new markets capable of reaching every place in the world. Data centers play an important role in ensuring access to internet data at any time. However, the energy efficiency of data centers is an issue, since they consume a considerable amount of power even when are unused in the idle state (Fig. 1) [6].

Energy is not consumed only by smart devices, but also by the system that diffuses the contents. Behind the video and music on demand, social networks or shopping websites, huge data centers need to be powered. For example, a Microsoft data center could consume 48 MW, that is enough power for 40000 homes [8]. The sector of Information and Communication Technology (ICT) is predicted to consume 20 % of the global electricity demand by 2030. Data centers will require a large slice of this electricity [9], presenting a considerable carbon footprint (Fig. 2).
The main consumers in a data center are CPU and memory [10], where dynamic random access memory (DRAM) is a building block. The interfaces used to access the memory array and provide bits off the chip are responsible for the power consumption in the DRAM system [11]. On the other side, access to storage Hard Disk Drivers (HDD) requires energy, which could be saved using Solid State Drivers (SSD) based on NAND Flash. Indeed, SSDs do not have moving parts and exhibit higher speed

and density than HDD [12]. However, the charge storage mechanism of NAND makes difficult the scaling of this technology, since, as the number of electrons stored in the floating gate is reduced, the loss of just one electron can cause significant reliability issues.
Therefore, the current memory hierarchy is composed on the top by SRAM and DRAM, that require frequent access and, thus, are fast and have a high endurance, and on the bottom by SSD and HDD, that feature a low cost, but low speed and endurance. The speed gap between DRAM and SSD is about 3 orders of magnitude, while the gap in areal density (i.e. cost) is around 2 orders of magnitude. In this context, the traditional memory hierarchy must be modified.
Storage Class Memory introduces a new level in the traditional memory hierarchy to fill the gap in performance and cost between DRAM and SSD. Storage Class Memory (SCM) concept was concretized by the commercialization of Intel and Micron 3D XPoint in 2015, that, however, in July 2022 has ceased the production. In fact, in the storage market, there are already several mature lower cost devices, although Intel 3D XPoint provided superior performance, the high price held back its success. 3D XPoint exploits Phase Change Memories (PCM), that are considered the best candidate for SCM thanks to the good scalability, the high endurance, faster switching time compared to NAND and the multilevel cell capability (Fig. 4) [7]. However, the end of 3D XPoint production demonstrates that there are still certain barriers preventing PCM memory from becoming mainstream mainly due to the high cost linked to the commercialization of a technology that is new compared to NAND Flash.
Material engineering becomes essential to meet the demand for low cost, high programming speed and endurance of SCM applications. In particular, it necessitates the investigation of novel alloys capable of rapid crystallization while maintaining the material stability during the multiple transitions between the amorphous and crystalline phases that occur during the device lifetime.

The objective of this thesis is the development of innovative phase-change materials to target SCM applications, understanding the failure mechanisms and which parameters can limit the reliability of the device.

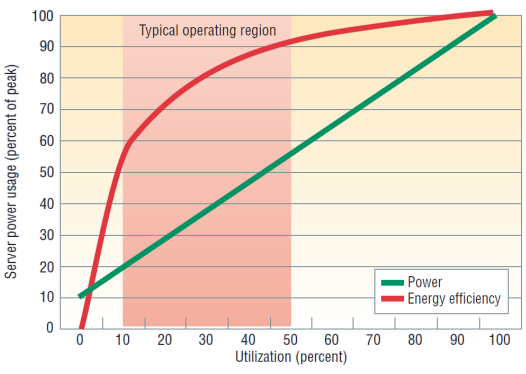

Fig. 1. Power usage and energy efficiency in a server [6].

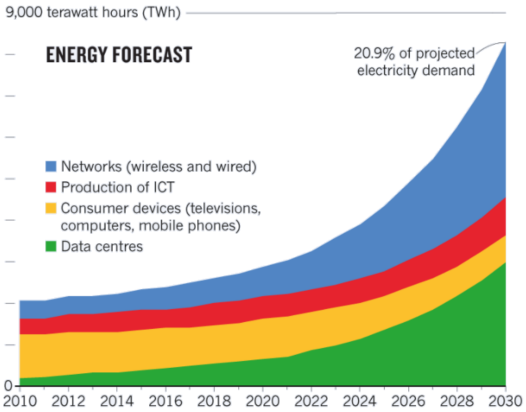

Fig. 2. Energy required by the ICT sector [9].

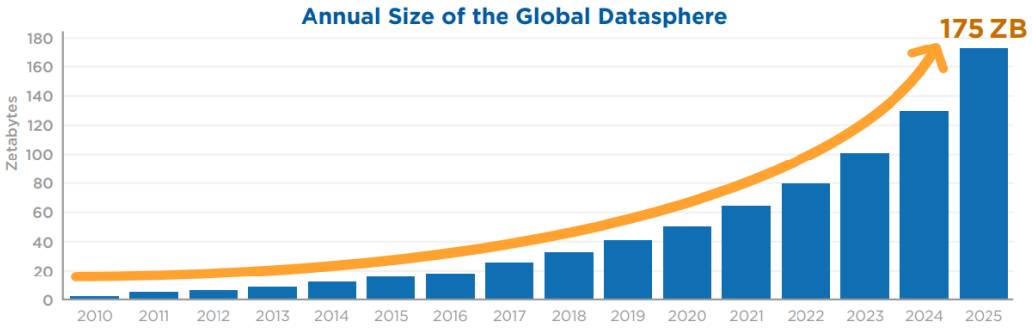

Fig. 3. Annual global datasphere trend [4].

In the first chapter, we focus on SCM comparing the emerging non-volatile memories (NVM) in terms of the main features for SCM, i.e. scalability, 3D integration, multilevel cell capability, latency and endurance. Moreover, 3D architecture and selector are discussed.
In the second chapter, PCM working principle is described. Then, we examine PCM reliability issues and how they can be overcame thanks to material engineering.
In the third chapter, we compare the performances of GeTe and GeSbTe (GST) based PCMs for SCM focusing on programming speed and material properties evolution during the programming cycles, and we investigate the impact of the pulse energy on endurance. Additionally, we demonstrate that Si doping in GST enhances MLC capacity and retention in PCM devices.
In the fourth chapter, we analyze different Sb-rich GST multilayers obtained by alternating layer deposition of GST and Sb targets, reporting that the best multilayer stack developed exhibits a reduced device-to-device variability with respect to bulk equivalent PCM devices. In the fifth chapter, we explore novel PCMs based on TiTe/GST bi-layer stack that guarantee high speed, high endurance and MLC capability. Then,

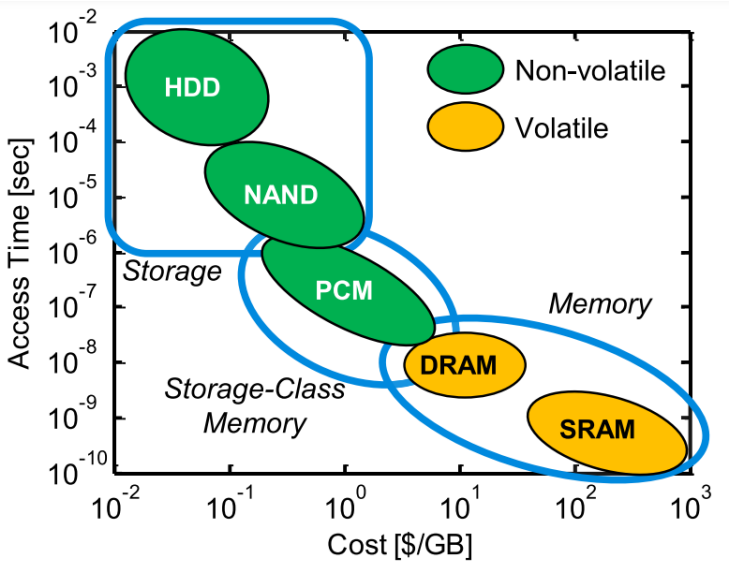

Fig. 4. Access time of various memories as a function of the cost. The space between NAND flash and DRAM in the memory hierarchy can be filled by PCM [7].

we investigate GaSb-based PCM demonstrating that C doping aids in reducing segregation, that naturally happens in off-stoichiometric GaSb.
In the conclusions, we summarize the key findings of this work and offer some perspectives for further research on PCM towards SCM applications or even SRAM/DRAM partial or total replacement in the future of the memory hierarchy.

Chapter 1

Storage Class Memory and emerging Non Volatile Memories

The two basic components of a computer are the processor and memory. The processor retrieves data from the memory, elaborates it, and then sends it back to the memory. However, the processor speed is increasing more quickly than the memory speed, and even though the processor is extremely fast, the system speed will be affected by the memory bandwidth if the memory cannot send data at that rate. This is called the Memory Wall [14]. The memory hierarchy was created in order to address this issue. We are referring to a Von Neumann architecture, where the computation part and the memorization part are separated.
The memory hierarchy is represented as a pyramid: the top layer is the one closest to the processor, which is faster but more expensive and less dense compared to the bottom layers (Fig. 1.1). The different levels are [13]:

1. the internal memory, constituted by the CPU registers.
2. the cache, usually organized with a further hierarchy of multiple levels L1, L2 and L3, where L1 contains the data with high frequency access since it is closer to CPU. Cache is made by static random access memory (SRAM).
3. the main memory, made by DRAM.
4. the hard disk and SSD.

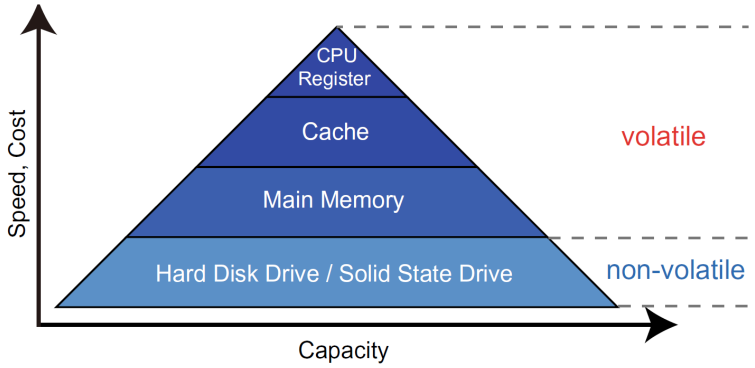

Fig. 1.1. The classical memory hierarchy in a Von Neumann architecture [13].

The first three levels consist of volatile memories, which must be powered to hold data, the fourth level includes non-volatile memories (NVMs) which retain data even when the power is turned off. In the last years, Flash memories have become the dominant NVM devices for mobile electronics [15]. In the next sections, we describe what are the problems related to SRAM, DRAM and Flash memory, why the memory hierarchy should be reorganized and what are the candidates for this revolution.

SRAM, DRAM and NAND limits

SRAM stores the information, i.e. the bit, in a node of a cross-coupled inverter, while other two transistors are used for write and read operations. Hence, a SRAM consists of six transistors in total, as shown in Fig. 1.2 (a). DRAM is composed by a transistor that modifies the charge of a capacitor as shown in Fig. 1.2 (b). It is clear that DRAM is less expensive and denser that SRAM, since the DRAM cell is smaller; on the other hand SRAM is faster than DRAM. However, both are volatile memories that need to be constantly powered to hold data and, therefore, consume a significant amount of power.
Flash memories are based on a charge storage mechanism, such as DRAM and SRAM, although are distinguished by non-volatility. A Flash memory cell is a floating-gate metal-oxide-semiconductor field-effect transistor (MOSFET), which is basically a MOSFET with two gates (Fig. 1.3). The stored data is represented by the charge trapped in the floating gate that changes the threshold voltage of the device. NAND and NOR are two types of Flash architectures. The NAND cells are connected in series, while the NOR Flashes are in parallel, meaning that each cell is connected to ground and to the line to access it. NANDs are more diffuse today in stand-alone systems since they are denser than NORs due to the fewer connection lines. However, Flash has reached its scaling limits due to interference between adjacent cells, retention issues and high variability between devices, which impacts the multilevel cell capability when the floating gate is reduced [16]. In addition, Flash features a poor endurance of 10^4-10^5 [17], requires an erase operation before the writing, long access time (25 µs) and erasing time (2 ms) due to the block-based architecture [18].

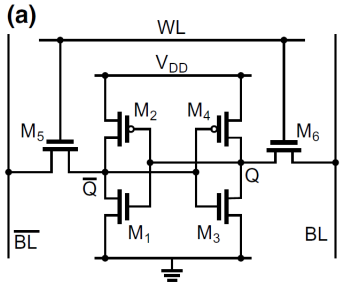

Fig. 1.2. Schematic of SRAM (a) and DRAM (b)cells [13].

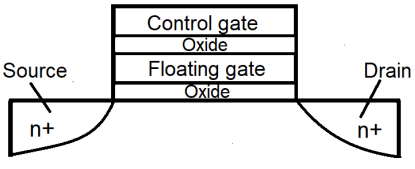

Fig. 1.3. Schematic of a Flash memory cell.

Storage Class Memory

In the previous section, we have seen that, in the memory hierarchy, the volatile part, also called memory, is characterized by high speed, low density and high cost; the non-volatile part, also called storage, features instead high density, low cost and low speed. This creates a bottleneck in the traditional memory hierarchy. Storage Class Memory (SCM) has the aim to reduce the boundaries in performances and cost between storage and memory. Therefore, SCM should combines performances of DRAM and SSD, preserving speed and endurance higher than NAND Flash and, at the same time, density and cost better than DRAM. In synthesis, the main requirements of SCM are non-volatility, short access and programming time, high endurance and low cost per bit [17]. Low cost per bit means high density, which can be provided by three dimensional (3D) integration and multiple bits per cell. The non-volatility ensures a low power consumption compared to DRAM that requires constantly the refresh. SCM does not have the task to simply replace NAND Flash or DRAM, it is a complementary level of the memory hierarchy and might be used for caching or tiering [19]. The position of SCM in the memory hierarchy is showed in Fig. 1.4. We can distinguish two types of SCM:

- **Memory-type SCM (M-SCM)** that shows characteristics closer to DRAM keeping a lower cost and power than DRAM. Speed and endurance are critical in this case: read/write speed must be less than 200 ns and endurance must be higher than 10^9. The data retention can be moderate.

- **Storage-type SCM (S-SCM)** that is closer to NAND Flash features. In this case, density and cost are important and must be comparable with NAND Flash. Although speed and endurance are not crucial for S-SCM, they must be higher than NAND Flash. Moreover, S-SCM must be truly non-volatile [20].

The target specifications for the two types of SCM are showed in the table 1.1 next to HDD, NAND Flash and DRAM characteristics.

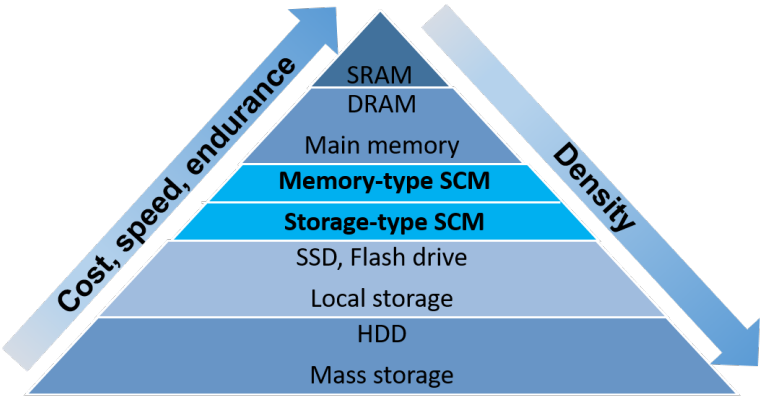

Fig. 1.4. The new memory hierarchy with SCM.

Table 1.1. Target specifications for SCM [20].

Parameter	Benchmark			Target	
	HDD	NAND flash	DRAM	Memory-type SCM	Storage-type SCM
Read/write latency	3–10 ms	~100 µs (block erase ~1 ms)	<100 ns	<200 ns	1–5 µs
Endurance (cycles)	Unlimited	10^3–10^5	Unlimited	$>10^9$	$>10^6$
Retention	>10 yr	~10 yr	64 ms	>5 d	~10 yr
ON power (W/GB)	0.003–0.05	~0.01–0.04	0.4	<0.4	<0.10
Standby power	~52–69% of ON power	<10% ON power	~25% ON power	<5% ON power	<5% ON power
Areal density	$\sim10^{11}$ bit/cm^2	$\sim10^{11}$ bit/cm^2	$\sim10^9$ bit/cm^2	$>10^{10}$ bit/cm^2	$>10^{10}$ bit/cm^2
Cost (US$/GB)	~0.1–1.0	2	10	<10	<3–4

1.1 Emerging memories for SCM

In this section, we are going to discuss about the different emerging NVMs that can be possible candidates for SCM and, then, have a place in the memory hierarchy.

1.1.1 FeRAM

A ferroelectric random access memory (FeRAM) exploits a ferroelectric material, which belongs to a class of crystals that can be polarized in two opposite directions (positive and negative) by the application of an electric field [21]. The two most common structures of FeRAM are the ferroelectric field effect transistor (FeFET) and the capacitor-like one-transistor one-capacitor (1T1C) cell. FeFET is similar to a floating-gate MOSFET cell, where a ferroelectric stack replaces the floating gate. In this structure the ferroelectric polarization modifies the threshold voltage of the transistor and the cell is programmed through the application of a positive or a negative voltage on the gate. However, the write operation in FeFET degrades the endurance due to charge trapping effects and defects generation. In the 1T1C cell, a capacitor composed of a ferroelectric material interposed between two metal electrodes is integrated at the drain of a transistor that acts as a selector. A positive write pulse is applied to sense the polarization state, if the polarization is negative, a large transient current can be detected. However, since this operation is disruptive and the cell must be rewritten, a high endurance of about 10^{14} is required [22, 23]. FeRAM is a good alternative to DRAM due to its high speed and low voltage operation, however due to its difficulties with 3D scaling and integration, FeRAMs cannot be considered good options for SCM [18, 20]. Nevertheless, FeRAMs have gained interest after the discovery of the ferroelectricity of hafnium dioxide thanks to its CMOS compatibility and scalability [24].

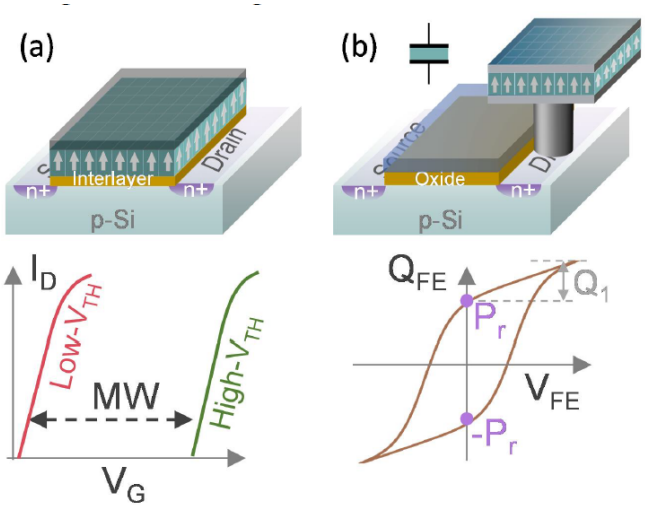

Fig. 1.5. (a) Structure of FeFET and ID-VG characteristics of two VTH states. (b) Capacitor based FeRAM and QFE-VFE hysteresis loop [22].

1.1.2 STT-RAM

Spin-transfer torque magnetic random access memory (STT-RAM) is the replacement of magnetic random access memory (MRAM). Both store the information in a magnetic tunneling junction (MTJ), which consists of three elements: a reference layer with a fixed ferromagnetic orientation; a free layer, whose magnetic orientation can be modified, and a tunnel barrier that is a dielectric sandwiched between the two magnetic layers. The storage is possible thanks to the tunnel magneto-resistance (TMR) effect according to which only electrons with the same spin orientation of the second layer can tunnel it. Therefore, the resistance is lower when the two ferromagnetic layers have the same magnetic orientation and is higher when they have opposite orientation [25]. Free layer orientation is obtained differently in MRAM and STT-RAM. In MRAM, memory switching is achieved by an external field, generated by a current passing through two orthogonal metal lines. In STT-RAM, the direction of the current passing through the MJT causes the orientation of the free layer, exploiting the spin-transfer torque effect. Two major issues of MRAM were resolved by STT-RAM: the scalability (since in MRAM the current does not scale with the cell size, resulting in significant energy consumption) and a problem called "half-select", which is an intentional switching of the cells above or below the selected cell due to the magnetic field created. Due to the absence of the additional metallic wires required by MRAM, STT-RAM presents also a simpler and smaller cell compared to MRAM [25].
Since atoms are not moved and only the magnetization is rotated during the write operation, the endurance of STT-RAM can be higher than 10^{12}. However, dielectric breakdown of the tunnel barrier can limit the endurance, if high voltages are applied [26, 27]. STT-MRAM is considered a promising candidate in low-level cache since it shows lower leakage power and smaller cell size than SRAM and higher write endurance than any NVMs. The main issue of STT-RAM is the high writing energy to achieve faster write speed [28]. To minimize write energy and latency, a reduction in data retention has been proposed. By decreasing the free layer area of the MJT, the write current decreases reducing write latency and write energy, nevertheless, the data retention time is

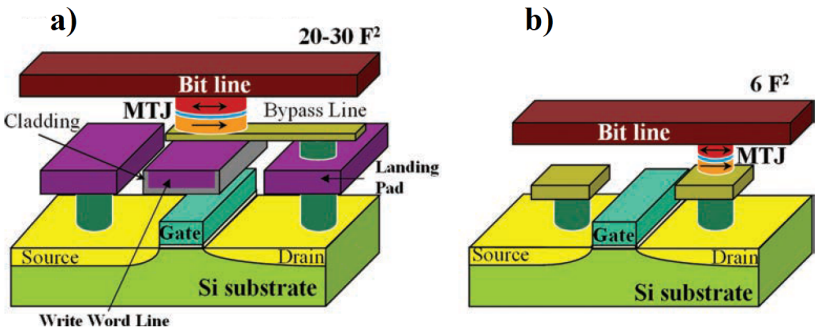

Fig. 1.6. (a) A Conventional MRAM cell. (b) A STT-RAM cell. [25]

reduced from 10 years to several ms or µs and, to prevent data loss, a refresh operation is required [29].

1.1.3 RRAM

A resistive random access memory (RRAM) is characterized by a basic structure called metal-insulator-metal (MIM) that consists of an oxide sandwiched between two metal electrodes (Fig. 1.7a). A reversible resistive switching can bring the insulator to the conductive state by applying a voltage pulse, which causes a large modification in the device resistance. Post-fabrication the resistance of the RRAM cell is high and requires an operation called electroforming, based on the application of a high voltage stress to reduce the resistance of the device. A memory selector is used, since the current flowing through the cell must be limited by a compliance current to avoid the electrical breakdown of the cell. The switching behavior depends on the MIM materials and can be classified as unipolar or bipolar: in the unipolar (or nonpolar) switching, the transition from one resistive state to the other depends only on the amplitude of the voltage; on the contrary, in the bipolar switching it depends on the voltage polarity (Fig. 1.7b-c). The voltage application leads to the formation of a conductive filament in the insulator during the transition to the low resistive state (SET) or to the rupture of the filament during the transition to the high resistive state (RESET) [30].
Hafnium oxide (HfO_x) is one of the most mature RRAM materials explored that is usually used with TiN electrodes to achieve a bipolar switching. HfO_x based RRAM

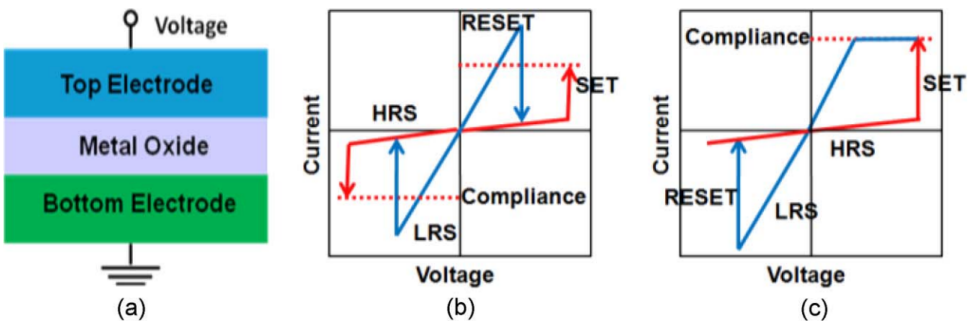

Fig. 1.7. (a) Schematic of RRAM MIM structure and schematic of I-V curves for (b) unipolar and (c) bipolar switching [30].

shows high speed operation (<10 ns), large ON/OFF ratio (>100), good endurance (>10^6 cycles) and multilevel storage [31]. Instead, RRAM with TaO_x (tantalum oxide) is recognized for the endurance higher than 10^{12} cycles [32].
RRAM has attracted interest for the low energy operation, the low cost, the fast write operation and the good scalability. However, the main limits of RRAM are the temporal (cycle-to-cycle) and spatial (device-to-device) variability of the programmed resistance due to the stochastic formation and rupture of the conductive filament in the oxide [33].

1.1.4 PCM

Phase-change memory (PCM) is a dual terminal memory that exploits the property of phase-change materials to reversibly switch from an amorphous to a crystalline phase. In a PCM device, this transition is obtained by Joule heating through electrical pulses. The crystalline phase is characterized by a low resistivity, while the amorphous phase features a high resistivity. The large resistive contrast between the two phases exceeds 2-3 orders of magnitude and makes the PCMs suitable for multilevel storage. The multilevel capability can be limited by the resistance drift that can be mitigate through material engineering or error correction metrics and architectures [34–36].
PCM high maturity is demonstrated by its manufacturability and reliability in 28 nm technology node for automotive applications [37] and by its commercialization in SCM market, thanks to 3D XPoint technology [38]. Indeed, the excellent scalability, fast read and write time, good endurance and multilevel cell make PCM a good candidate for SCM [7].
PCM will be better described and analyzed in the next chapter.

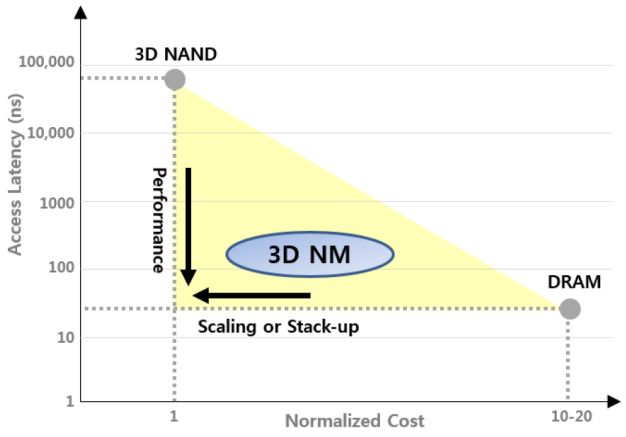

Fig. 1.8. Position of 3D cross-point memory compared with DRAM and 3D NAND in terms of latency and normalized cost [39].

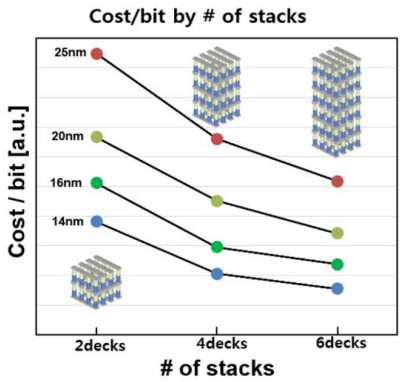

Fig. 1.9. Calculated cost per bit of 3D cross-point memory for scaling and vertical stack-up. [39].

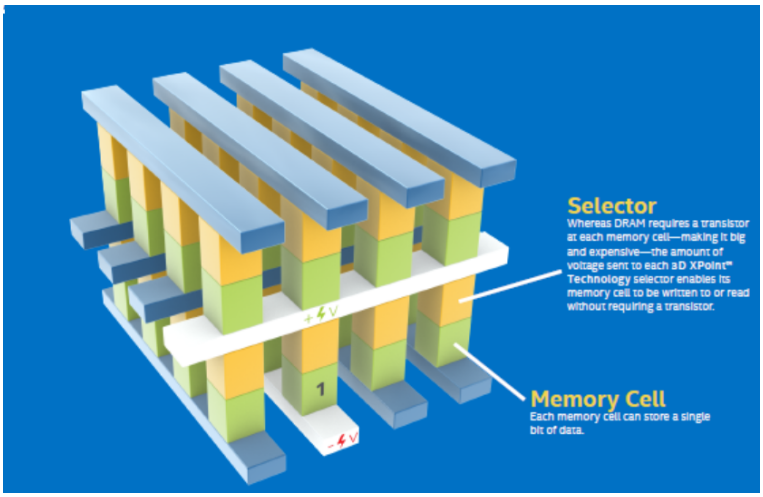

Fig. 1.10. Intel and Micron 3D XPoint technology.

1.2 The cross-point architecture: towards a 3D BEOL memory

3D integration is fundamental for boosting the memory density and reducing the cost of SCM architectures. New 3D memory technologies must collocate between DRAM, that is expensive and fast, and NAND Flash, that is cheap but slow, hence should exhibit low latency and cost effectiveness, as indicated in Fig. 1.8. Fig. 1.9 shows how the cost is reduced from both lateral and vertical scaling, assuming that the peripheral circuit is placed completely under the cell array. Without this condition, the number of die per wafer cannot increase [39].
In 2003, the first 3D cross-point (XPoint) memory technology of 512 Mb with 8 layers of vertically stacked memory cells was developed [40, 41]. The memory cell is a poly-silicon based SiO_2 anti-fuse, situated at the intersection between perpendicular word-line and bit-line, which is only programmable once.
A stackable 3D cross-point based on PCM and on an Ovonic Threshold Swith (OTS) selector has been demonstrated in 2009 [42]. Robust isolation of individual PCM cells is ensured by the high resistive amorphous selector. PCMs with OTS are fully stackable over CMOS circuits and the compatibility of PCM with metallization schemes makes feasible the superimposition of multiple layers of cross-point memory arrays. 3D XPoint memory technology was commercialized in 2015. It is 1000 times faster than NAND, 10 times denser than conventional DRAM memory and presents 1000 times greater endurance than NAND. Cells can be addressed individually ensuring faster read and write operations. Therefore, data can be stored close to the processor and accessed at speeds previously impossible for non-volatile storage [43]. The first generation of 3D XPoint memory technology is capable of storing 128 Gb in a die, the second generation has doubled the capacity and future scaling will continue to increase the capacity reducing the cost per bit, while material tuning and circuit design optimization will decrease latency [44].
3D XPoint is exploited in two Intel technologies: Intel Optane Persistent Memory (PMem) and Intel Optane SSDs. Intel Optane PMem is a valid alternative to DRAM

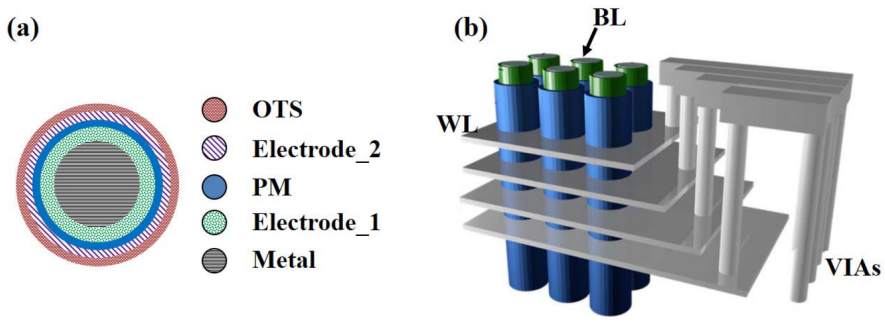

Fig. 1.11. Vertical cross-point architecture. a) Cross section of the bit-line pillar. b) Schematic of the overall vertical cross-point architecture [46].

delivering high capacity at a low cost for rapid data processing, introducing a new category in the memory hierarchy between memory and storage. Intel Optane PMem has two operating modes: Memory Mode and App Direct Mode. In Memory Mode, the amount of volatile memory visible to the operating system is extended without application changes. The CPU uses the DRAM as cache and the Optane persistent memory as addressable main memory, providing larger memory capacity and lower cost than DRAM. In App Direct Mode, the operating system sees Intel Optane PMem and DRAM as two separate entities, and software and application can talk directly to Intel Optane PMem that can act like an SSD with higher endurance and better bandwidth compared to NAND [45]. On the other hand, Intel Optane SSDs consists of a new storage tier between Intel Optane PMem and NAND SSDs. It provides low latency for database applications that require frequent high-speed caching.

However, in 3D XPoint, it is challenging to increase the number of stacked layers, since the amount of lithography and process steps increases linearly with the number of stacked layers, reducing the cost effectiveness of this architecture.
A new proposed architecture is the Vertical XPoint (V-XPoint) that mimics the highly mature 3D NAND fabrication [47]. In V-XPoint, word-line and bit-line are arranged in the lateral and in the vertical directions, as indicated in Fig. 1.11. This structure allows reducing the number of patterning steps, improving the cost effectiveness. V-XPoint requires Atomic Layer Deposition (ALD) to ensure conformal film growth over the 3D structure and the research on ALD selectors is still at the beginning [46].

3D cross-point challenges

In order to achieve a high density in 3D cross-point architectures, word-line and bit-line must be scaled at the same rate as the selector and the memory cell. As Cu wires scale down to a width comparable to the mean free path of Cu, the wire resistivity increases. The resistivity increase can cause degraded write/read margins, reduced speed and substantial energy dissipation of wires. This is a limit on the array size increasing. Possible solutions to overcome the Cu limits may be the use of wires with better conductivity and scalability, such as graphene or carbon nanotubes or memory arrays with smaller partition size [48].
In a cross-point architecture, a half-selected scheme is commonly used, in which the cells along the same word-line and bit-line of the selected cell are biased by a voltage

V/2, in contrast to the selected cell biased at the voltage V. The applied voltage can enable an excessive leakage in the half-selected cells causing sneak paths [49]. Sneak paths are undesired paths for current that act as an unknown parallel resistance to the selected cell resistance narrowing the noise margin and reducing the maximum size of the cross-point array [50]. The choice of an access device with a low leakage current is fundamental to reduce the sneak paths.

1.3 3D cross-point selectors

In a cross-point architecture, the read and write operations must take place in the desired memory cell avoiding disturbing any other cell. In this context, the selector comes to play.
The features that a selector should have are listed below [49, 51]:

1. **Two-terminal structure** to not occupy an extra area in the array and ensure the minimal cell size. For this reason, transistors as selectors must be avoided.

2. **High ON-state current density** on the order of several MA/cm^2 to provide enough current to program and erase the memory cell.

3. **High non-linearity**, namely the OFF state leakage current must be as low as possible to prevent the leakage through the unselected cells and the associated power consumption. If this condition is satisfied, the maximum array block size can be increased.

4. **Process compatibility with 3D multilayer stacking**: the materials of the selector must be CMOS compatible and the selector must be compatible with the Back-End-of-Line (BEOL) fabrication process to enable the stacking of multiple layers of cross-point arrays. To be compatible with the BEOL, the maximum thermal budget during the fabrication must not exceed 400 °C and the access device must remain functional after 2 hours at 400 °C.

5. **Voltage compatibility with the memory element** to ensure read and write operations in the selected memory cell and low leakage in the unselected cells. Furthermore, the voltage should be compatible with device-to-device variations and changes in the operating temperature.

6. **Speed, endurance and variability of the access device should be better than those of the memory element** to not limit memory chip performance and reliability.

Furthermore, STT-RAM and bipolar RRAM require the current to flow in opposite directions for the programming and erasing operations, in this case, the selector must guarantee bipolar operation.

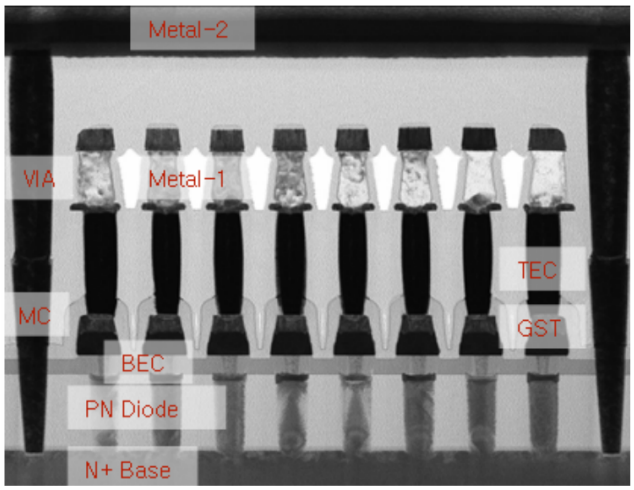

Fig. 1.12. Vertical view of a 512 Mb PRAM array with PN diode selectors [52].

Si-based selectors

PN diodes are able to provide enough current for the switching operation of a memory cell minimizing the off-current and ensuring cell area efficiency.
For example, functionality of a 512 Mb PCM array was demonstrated using a vertical PN diode as selector (Fig. 1.12) [52]. A poly-Si diode was used in a cross-point with PCMs showing low off-current of 100 A/cm^2 and high on-current of 8 MA/cm^2 that can support PCM programming operation [53]. Also a n+/p/n+ vertical junction showed bipolar operation and high switching speed, furthermore the on-voltage can be tuned modifying the p-region doping and its length [54]. However, a temperature of 700 °C is required for fabrication making it incompatible with BEOL fabrication process. This is a limit of all Si-based selectors where the dopant activation needs higher temperature not suitable for 400 °C BEOL process and 3D stacking of multiple layers [51].

Oxide-based diodes

Oxide-based diodes have been proposed as alternative to Si-based diodes since they can be fabricated at BEOL compatible temperatures.
Binary oxide diodes consisting of NiO as p-type semiconductor and TiO_2 as n-type semiconductor have been fabricated below 300 °C combined with oxide-RRAM cells, showing a proper functionality [55]. However, this NiO/TiO_2 diode can provide a maximum current density of 10^3A/cm^2. P-CuO_x/n-$InZnO_x$ showed an increased current density of over 10^4A/cm^2 and can be easily fabricated at room temperatures [56], although the current density is still not enough high for 3D cross-point architectures.
A Ni/TiO_2/Ni bipolar nonlinear selector has been reported in [57]. It was fabricated by sputtering at 200 °C in series with oxide-RRAM. The Schottky emission over the Ni/TiO_2 barrier allows achieving highly nonlinear characteristics with an ON/OFF ration of six orders of magnitude between 0 and ±2 V. Furthermore, Ni/TiO_2/Ni demonstrated capable to provide a current density of 10^5A/cm^2 and to be fabricated at room temperature in a 8×8 cross-bar array [58].

Mixed Ionic-Electron Conduction (MIEC) selectors

Mixed Ionic-Electron Conduction (MIEC) materials conduct both ions and electrons (or holes) and typically contain a large amount of Cu. The Schottky barrier at the MIEC-electrode interfaces suppresses the current flow at low bias. As the bias increases, copper ions and vacancies shift leading to an exponential increase of the current [59]. Selectors based on MIEC materials can be fabricated at BEOL compatible temperature, are scalable, can conduct high currents (>50 MA/cm^2) and provide a large ON/OFF ratio (>10^7). This makes MIEC selector interesting for multiple stacking in PCM cross-point arrays [60].
MIEC-based access devices have been integrated with PCM, demonstrating to enable RESET operations at currents higher than 200 μA in <15 ns. The devices are still functional if scaled down to a thickness of 11 nm and to <30 nm in lateral size. Despite a leakage increase as the thickness is reduced to 6 nm, the voltage margin improves when the lateral sizes are reduced [61]. Furthermore, large 512 kb arrays with 100% yield have been realized co-integrating PCM and MIEC selectors exhibiting large currents (>200 μA), low leakage (<10 pA) and high voltage margin (1.5 V) [62]. Scaling is also beneficial for endurance, indeed an improved endurance in thinner MIEC selectors integrated with PCM has been shown. Endurance can reach 10^8 cycles using 150 μA as programming current, but higher currents reduce cycling endurance leading to earlier failures [63].

Metal-Insulator transition (MIT) selectors

Some oxides, such as VO_2, have a metal-insulator transition (MIT) property that can be exploited using these materials as access devices. VO_2 devices show fast switching speed (<20 ns) and high current densities (>10^6A/cm^2) [64]. Although VO_2 exhibits an excellent MIT characteristic, its transition temperature of 67 °C [65] makes it unsuitable for applications that need higher operating temperatures [49]. On the contrary, NbO_2 remains stable up to 160 °C. Fast switching speed (22 ns), excellent scalability down to 10 nm and high ON current (>2MA/cm^2) were observed in NbO_2-based access devices [66]. However, the leakage current in half-selected and unselected devices is still high, due to the low band-gap of MIT materials [49, 51].

Ovonic Threshold Switch (OTS) selectors

OTS selectors enabled the commercialization of Intel and Micron 3D XPoint. OTS are based on amorphous chalcogenide materials capable of switching to the crystalline phase reversibly and volatilely. As the voltage across the OTS exceeds a threshold voltage (V_{TH}), the device switches to the conductive state and, as the current is reduced below a certain value defined as holding current, the OTS switches back to the highly resistive state [67].
The high ON current, the high selectivity and the compatibility with the BEOL make OTS suitable for 3D integration with PCM [68]. The current-voltage (I-V) characteristic of a RESET PCM integrated vertically with an OTS is illustrated in Fig. 1.13: V_{TH} is equal to the sum of the OTS V_{TH} and PCM V_{TH}, since OTS and PCM are connected in series [42]. When the PCM is in the crystalline phase, V_{TH} is that of

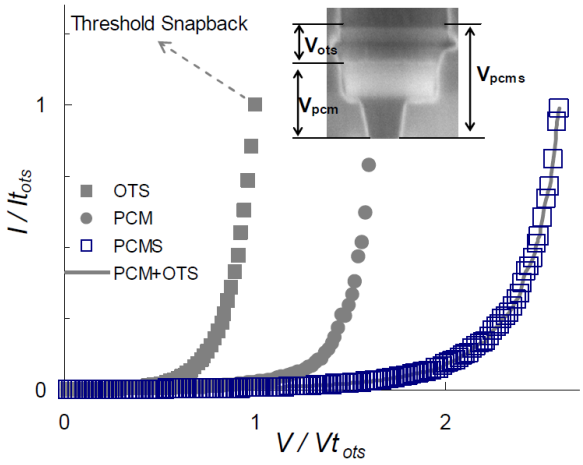

Fig. 1.13. I-V characteristic of an OTS, a PCM and an OTS+PCM. The PCM was programmed in the RESET state [42].

the OTS. Hence, this threshold voltage mechanism allows distinguishing the different resistive states of the PCM.
OTS performance depends on the chalcogenide material used. AsTeGeSi shows an ON current higher than 11 MA/cm^2 and an endurance higher than 10^8 [69]. Nevertheless, Te-based OTSs exhibit a selectivity lower than 10^4 that is insufficient for achieving dense PCM arrays [68]. An OTS based on binary B-Te alloy exhibits high ON/OFF current ratio grater than 10^5, low operating voltage, low leakage, fast switching speed, endurance up to 10^8 cycles and a high ON current of 55 MA/cm^2 [70]. Also GeSe OTS showed high drive current of 23 MA/cm^2, endurance grater than 10^8 and tunable turn-on voltage [71]. SET and RESET operations have been demonstrated in AsSeGe selector integrated with PCM. The selector can deliver 7.9 MA/cm^2 and fast speed (10 ns). Moreover, an excellent cycling endurance of 10^{12} is achieved in AsSeGe OTS+PCM [72].

	FeRAM	**STT-RAM**	**RRAM**	**PCM**
Scalability	Limited	Limited	Promising	Promising
Multilevel cell	Limited	Limited	Medium	Good
3D Integration	Limited	Medium	Good	Good
Write Speed	High	High	Medium	Medium
Write Power	Medium	Medium	Medium	High
Retention	Medium	Good	Medium	Good
Endurance	Good	Good	Limited	Medium
Variability	Low	High	High	Medium

Table 1.2. Comparison of emerging NVM technologies for SCM. Adapted from [20]

1.4 Summary of the chapter

In this chapter, we discuss the challenges of the traditional memory hierarchy and how they can be overcome by SCM, which goal is to reduce the gap in performances and cost between storage and memory.
Scalability, 3D integration, multilevel cell capability are characteristics required by memory devices to satisfy the high density requirements of SCM applications. Other key features of SCM are low fabrication costs, long data retention, low latency, low power consumption, high endurance and low variability. A comparison of emerging NVMs in terms of these attributes is shown in Table 1.2.
Despite low power and low latency, FeRAM is not indicated for SCM applications due to the poor MLC capability, difficulties in scaling and 3D integration.
Among the described emerging NVM, STT-RAM features the highest endurance. However, maintaining long data retention while achieving competitive speed, endurance, and scalability is challenging.
RRAMs offer the benefit of a simple structure with correlate low cost, however variability and endurance must be improved verifying if aggressive scaling can be supported.
PCM is the most mature among emerging NVM since the multilevel cell capability and good scalability can increase the device density. Latency and endurance can be further improved thanks to material engineering. Power efficiency efforts are ongoing to reduce the power consumption of these memories. For its features and maturity, PCM can be considered the best candidate for SCM.
Indeed, PCM was exploited by Intel and Micron 3D XPoint memory, which is faster than NAND, denser than regular DRAM memory, and offers more endurance than NAND. Moreover, individual cell access provide faster read and write operations.
Read and write operations in a 3D XPoint memory can be realized without disturbing other memory cells thanks to a selector. Different types of selector for 3D architectures have been discussed in this chapter
Si-based selectors require for the fabrication high temperatures incompatible with BEOL process and 3D vertical stacking. However, although oxide-based diodes are compatible with the BEOL fabrication, they can not provide sufficient current density for PCM programming. MIEC selectors offer BEOL compatible temperatures, high ON/OFF ratio, high ON currents and low leakage, however high drive currents reduce the endurance. Among MIT selectors, NbO_2 ensures higher operating temperatures than VO_2 and high ON currents, nevertheless the leakage current is not sufficiently low. The high ON current, high ON/OFF ratio and great endurance of OTS make it suitable for 3D integration with PCM, as confirmed also by the choice to use OTS and PCM in 3D XPoint technology. The research is still active to improve OTS endurance and reduce leakage through material engineering.

Chapter 2

Phase-Change Memory

In the late 1960s, Ovshinsky discovered a rapid and reversible transition between a highly resistive and a conductive state enabled by electric field in chalcogenide materials [67]. In the '70s, it was proposed to exploit this reversible switching in NVM devices [73, 74]. However, the first PCM devices were characterized by high energy consumption due to high programming currents and low speed that prevented their commercialization for long time [75]. After almost three decades, the interest in phase-change technology was renewed: GeSbTe alloys were exploited in optical recording media [76], since these alloys can be switched using laser pulses of short duration. The feasibility of PCM with low energy consumption, high speed and high endurance was demonstrated at the beginning of the second millennium [77, 78]. Read and write operations in memory array are ensured by a selector that must be coupled with the memory cell. BJT was proposed as selector in a 8 Mb array integrated in a 180 nm CMOS process to get high density [79]. Since MOSFET selectors occupy a large area, they cannot be exploited for high density standalone applications, though they can be integrated with few masks into CMOS technology reducing the costs and making them suitable for embedded applications [80]. In 2009, the first 128 Mb array based on a 90 nm PCM technology was commercialized to meet NOR Flash replacement requirements [81]. Finally, a 1 Gb PCM cell array with BJT selector based on a 45 nm technology node was developed [82]. At the beginning, PCM development was focused on replacing NOR Flash in cellular phones [75]. This bet turned out wrong, since with smart-phones NAND Flash architecture became dominant due to the high storage capacity demand. PCM prototypes were also realized for SSDs showing improvements in read latency and bandwidth [83]. However, the product was never introduced since density and cost were not still competitive with NAND Flash. Recently PCM entered both embedded and stand alone market. Indeed, ST Microelectronic developed a highly scaled 28 nm embedded PCM that meets automotive reliability criteria [84]. Concerning standalone market, PCM is included in 3D XPoint that has achieved high volume production concretizing the concept of SCM [44].
In recent years, research is working to improve PCM performance on two main fronts [75]:

1. by a scalable cell architecture to minimize the programming current. In fact, PCM working mechanism is based on the ability to convert the current across the device in temperature, but most of the heat generated is lost in the surrounding

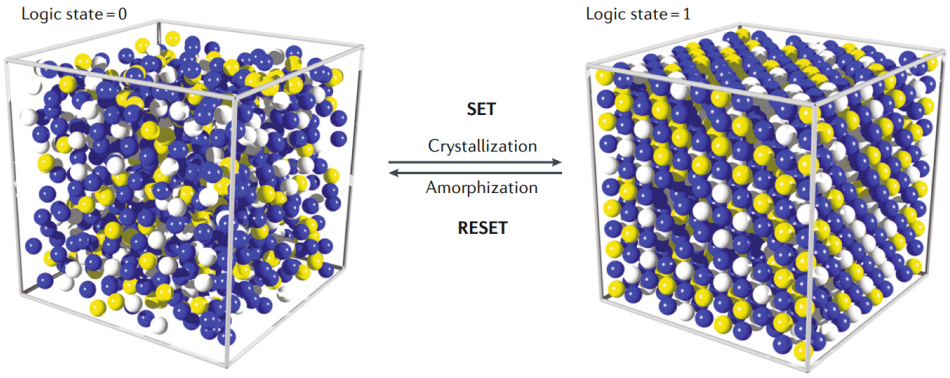

Fig. 2.1. Phase-change transition consequent to SET and RESET operations [85].

structure. Therefore, a thermally optimized cell is able to reduce significantly the programming current.

2. by material engineering to tailor PCM properties accordingly to the target applications.

These two subjects will be better discussed later in this chapter.

Brief history of phase-change materials for PCM

The first chalcogenide proposed by Ovshinsky was $Ge_{10}Si_{12}As_{30}Te_{48}$, but the low speed and low endurance limited its utilization [67]. In the late 1980s, GeTe and GeSbTe compounds in the GeTe-Sb_2Te_3 tie line, such as $Ge_2Sb_2Te_5$ and $Ge_1Sb_2Te_4$, became popular in optical storage thanks to their fast crystallization. Then, also doped Sb and Sb_2Te compounds were developed for optical applications, in particular $Ag_4In_3Sb_{67}Te_{26}$ (AIST) was widely used [85].
In the 2000s, the interest for PCMs was renewed and GeSbTe compounds, in particular $Ge_2Sb_2Te_5$, were selected to be integrated in PCM devices thanks to the good cyclability and improved programming speed [85]. However, to make PCM competitive with DRAM and NAND Flash memory technologies, research efforts are required to find the best phase-change materials.

2.1 PCM working principle

PCM is a dual terminal resistive memory that exploits the electrical properties of some chalcogenide materials, which are alloys consisting at least of one chemical element in the VI group of the periodic table [87]. These alloys can switch reversibly from an amorphous phase to a crystalline phase: the low-resistance crystalline phase is referred as SET state, while the high-resistance amorphous phase as RESET state (Fig. 2.1). In phase-change materials, this transition occurs thanks to a temperature increase that can be induced optically, like in optical disks, or electrically, like in PCM. After the BEOL fabrication process at 400 °C, the PCM is in the crystalline phase. To bring the cell to the amorphous phase, the temperature must increase above the melting point

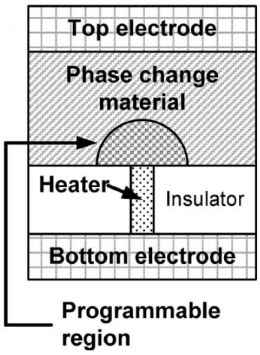

Fig. 2.2. Schematic of a conventional PCM cell, usually referred as mushroom cell [86].

of the phase-change material and then the cell must be quenched rapidly to preserve the disorder typical of the amorphous phase. For the SET operation, the cell must be kept above the crystallization temperature for a time period long enough to crystallize it. Fig. 2.2 shows a typical PCM cell, consisting of a top and a bottom electrode, through which the electrical current flows, the phase change material and the heater, where the heat is generated thanks to Joule effect. The length and the intensity of the program pulse control the local temperature. A short and sufficiently intense program pulse enables the RESET operation. However, the falling edge of the pulse must be fast enough to make effective the RESET operation, otherwise a re-crystallization can be induced. Indeed, the length of the falling edge slows the cooling, favoring the organization of the material in the ordered crystalline phase.

The current-voltage (I-V) curve of a PCM is reported in Fig. 2.3. At low field, crystalline and amorphous phases exhibit a large resistance contrast, in this part of the curve read operation is performed. SET and RESET programming regions can be reached increasing the bias above the switching threshold voltage (V_{TH}), so that the currents is able to heat the programming region of the cell causing the phase-change [88]. The resistance behavior at different bias is shown in Fig. 2.4. At low currents, the cell resistance state remains the same (READ region). If a device is programmed in

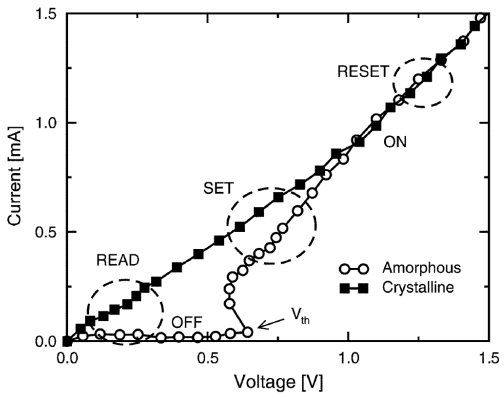

Fig. 2.3. Experimental I-V characteristic of a GST based PCM in the amorphous/RESET and in the crystalline/SET state [88].

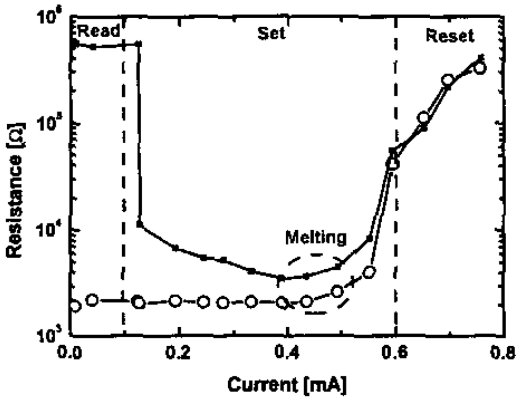

Fig. 2.4. Experimental resistance-current curve of GST PCM programmed in both SET and RESET state [89].

the high resistive state, the resistance drops at higher currents (SET region) and starts to rise when the current is higher enough to generate a rapid cooling of the melted material [89].

2.2 Crystallization behavior of phase-change materials

Information about the crystallization behavior of a phase-change material can be extracted from the resistivity as a function of temperature (R-T) characteristic. As shown in Fig. 2.5, amorphous film exhibits a high resistivity that decreases as the temperature increases. The drop in resistivity corresponds to the crystallization temperature that depends on the material. GST shows a more gradual transition to the crystalline phase compared to AIST, in particular GST features two transitions: one from the amorphous to the face-centered cubic phase at 154 °C and the other one from the fcc to the trigonal phase at 348 °C [90]. On the contrary, AIST shows a single steep transition from the amorphous to the trigonal phase.
Crystallization of phase-change materials can be either nucleation-driven or growth-driven (Fig. 2.6). For nucleation-driven materials, crystallization occurs through the stochastic formation of crystalline nuclei an their growth [85]. In this case, the crystallization time does not depend on the size of the amorphous mark and the crystallized region is poly-crystalline with grains of different size and orientations.
For growth-driven materials, crystallization starts at the interface between the amorphous mark and the crystalline surrounding creating a single crystallite. The nucleation time is so long that the nucleation of crystalline seeds does not occur during the rapid growth process. In this case, the crystallization time increases as the amorphous size increases [85, 91].

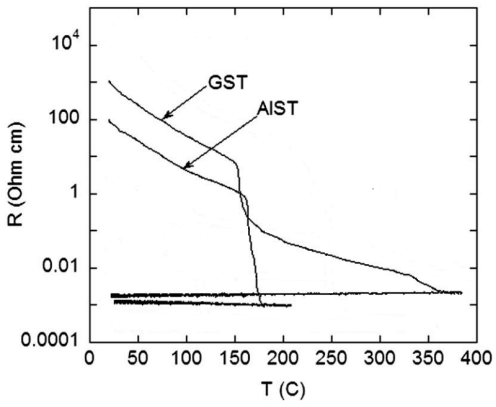

Fig. 2.5. Resistivity as a function of temperature in GST and AIST. Adapted from [90].

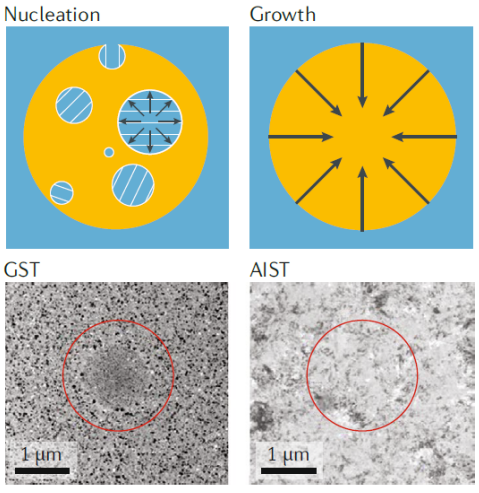

Fig. 2.6. Above: schematic of nucleation and growth driven crystallization. Below: Transmission electron microscope (TEM) images showing the crystallized region marked by a red circle in GST and AIST that exhibit respectively a nucleation driven and a growth driven crystallization [85].

Transmission electron microscopy (TEM) analysis evidence that AIST is a growth-driven material, while GST is nucleation-driven [85]. This can explain the different transition from amorphous to crystalline phase in GST and AIST observable in the R-T curve. However, studying the crystallization behavior of phase-change materials, it must be remembered that the nucleation time of a melted-quenched material is half that of an as-deposited material, since in a melted-quenched material atomically ordered clusters already exist reducing the nucleation barrier [91].

2.3 Conduction in the crystalline and in the amorphous phase

Investigations on the properties of the band structure can be realized by optical and electrical characterization on thin material films.
Hard x-ray photoemission spectroscopy (HXPES) is an experimental technique to determine the density of states in the valence band. Commonly, in the crystalline phase the valence band edge is closer to the Fermi level compared to the amorphous phase, since the crystalline phase is highly conductive. In amorphous GST, the band gap is about 0.8 eV, suggesting that it behaves as an intrinsic semiconductor with the Fermi level in the mid gap. In the crystalline fcc GST, the Fermi level situated close to the valence band and the narrow band gap indicates a quasi-metallic conduction. The schematic band structures of crystalline and amorphous phase is represented in Fig. 2.7. Distorted bonds, dangling bonds, wrong bonds (e.g., Ge-Ge bonds in GST) in the amorphous phase constitute defects that result in a large density of localized states in the forbidden gap [93].
Moreover, electrical resistivity measurements as a function of temperature provide information about the band structure. In Fig. 2.5, at temperatures below the crystallization temperature, the resistivity decrease is due to the temperature activation of

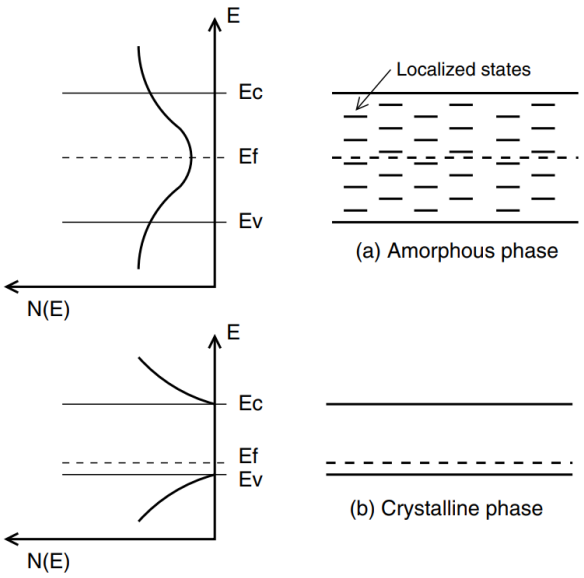

Fig. 2.7. Schematic band diagrams and density of states of amorphous (top) and crystalline (bottom).

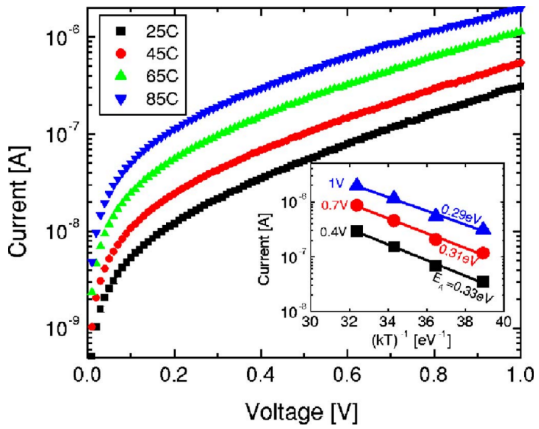

Fig. 2.8. I-V characteristics for a RESET PCM at increasing temperatures. Inset: Arrhenius plot of the current measured at three values of voltage [92].

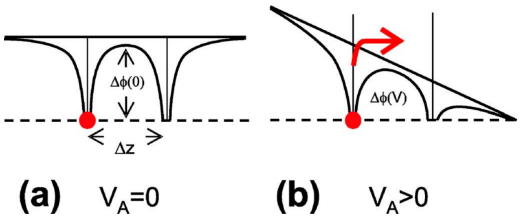

Fig. 2.9. Schematic for the trap-limited conduction mechanism with electrons confined by potential barriers at zero bias (a) and after voltage application (b) [92].

transport deriving from thermal generation of carriers from the valence band to the conduction bands of the amorphous semiconductor. The activation energy corresponding to the energy difference between the Fermi level and the valence band, equal to half of the band gap for the amorphous phase, can be estimated from the Arrhenius plot [93]. In the crystalline phase, the smaller slope, that results in a lower activation energy of conduction, indicates a more favorable conduction compared to the amorphous phase.

Although thin films investigations provide basic knowledge of the phase-change material, electrical characterization of PCM devices offers more insights on the conduction mechanisms. Fig. 2.8 shows the subthreshold I-V characteristic performed at different temperatures in a GST PCM device programmed in the RESET state. At small voltages below 0.3 V the curve exhibits a linear behavior, while at higher voltages an exponential regime is observed. As the temperature increase, the large activation energy of conduction of the amorphous material causes a strongly increase of the current. The current values were plotted as a function of 1/kT for different voltages in the inset of Fig. 2.8 showing an activation energy of conduction that decreases as the voltage increases. This behavior is observed in materials with a trap-limited conduction and is commonly described as Poole-Frenkel mechanism. According to this mechanism, the conduction is due to electrons thermally emitted hopping between traps. As indicated in Fig. 2.9, the application of an electric field lowers the potential barriers. Since the electron emission depends exponentially on the barrier height, the current I can be written as [92]:

$$I \propto e^{\frac{\Delta\Phi(0)-qV_A\Delta z/(2u_a)}{kT}} \tag{2.1}$$

where $\Delta\Phi(0)$ is the barrier height at zero bias, q is the elementary charge, V_A is the applied voltage, Δz is the average distance between two traps, u_a is the thickness of the amorphous material, k is the Boltzmann constant and T is the temperature. Whereas the standard Poole-Frankel model predicts an exponential dependence of I on the square root of the voltage, in eq. 2.1 an approximation valid for small intertrap distance was utilized, assuming that the maximum of the potential barrier lies in the

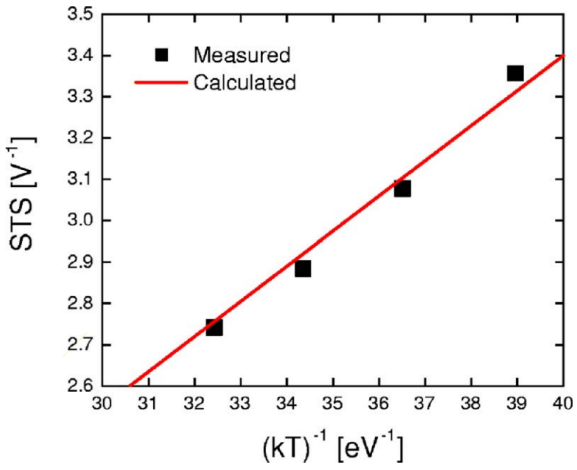

Fig. 2.10. STS as a function of 1/kT [92].

middle between two traps [92].
The subthreshold slope (STS) in the exponential regime can be extracted from eq. 2.1:

$$STS = \frac{\partial log I}{\partial V} = \frac{q}{kT}\frac{\Delta z}{2u_a} \tag{2.2}$$

Therefore, STS values can be obtained from the subthreshold I-V characteristic (Fig. 2.8) in the high voltage region. The slope of Fig. 2.2, representing the STS as a function of 1/kT, is useful to calculate $\Delta z/2u_a$, i.e. the intertrap distance normalized to the amorphous layer thickness, that allows estimating the degree of disorder in the amorphous phase-change material, or rather, if u_a is known, the intertrap distance Δz.

2.4 The threshold switching

The threshold switching is a critical feature of phase-change materials that arises from a bistable negative differential resistance (NDR) in which two distinct currents can be achieved at a given voltage [93]. Without this mechanism PCM would not be a viable technology, because in the high resistive state extremely high power would be necessary to heat the cell over the crystallization temperature. The threshold switching is reversible since removing the voltage quickly, the cell returns to the high resistance state without memory switching. Memory switching occurs only if the voltage pulse is long enough to organize the material in the crystalline phase bringing the cell in the low-resistance state.
The origin of threshold switching is still debated and has been explained by different models. At the beginning, a thermal model was proposed where the switching phenomenon was due to the thermal breakdown of the amorphous film. As the temperatures rises for Joule effect, the thermal runaway improves the electrical conductivity locally and causes a thermal generation of electrical carriers [94].
In an electronic model, the threshold switching was attributed to a carrier generation mechanism driven by electric field [95].

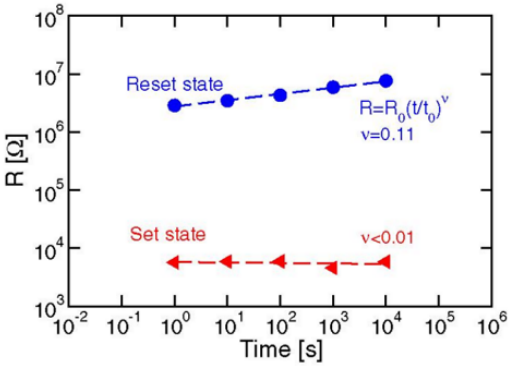

Fig. 2.11. Resistance as a function of time measured in $Ge_2Sb_2Te_5$ showing the drift phenomena [98].

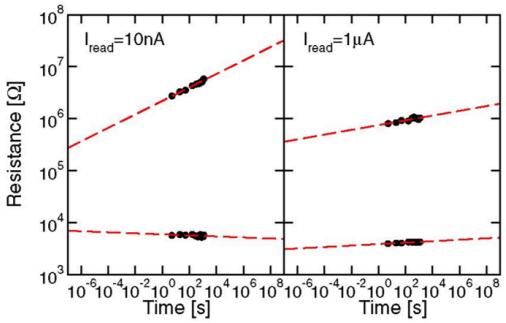

Fig. 2.12. Resistance drift for two different read currents [98].

Another electronic model explains the threshold switching with an energy gain of electrons for hopping among traps at high electric field that results in a non-equilibrium configuration of bands with inhomogeneous electric field [96].
In the field-induced nucleation model, the threshold switching is due to a nucleation of a long conductive cylinder. The electric field increase facilitates the nucleation of additional particles making the cylinder longer. However, the conductive embryo disappears if the field is removed too quickly, otherwise the embryo will reach a stable size ensuring the memory switching to the low resitive state [97].
Threshold switching is critical for PCM operation and performances. Indeed, the threshold voltage establishes the voltage ranges for the read and write operations and, if the PCM is integrated with an OTS selector, it defines the ON/OFF ratio.

2.5 Resistance drift

Resistance drift indicates the increase of the programmed resistance over time due to a structural relaxation of the material, which affects the electrical conduction and the atomic arrangement.
Drift is represented in Fig. 2.3 for both RESET and SET state: SET resistance is stable, while RESET resistance increases according to the following power law:

$$R = R_0(\frac{t}{t_0})^v \tag{2.3}$$

where R is the resistance, t the time, R_0 and t_0 are constants. Although the only state affected by drift is RESET in GST, there are some materials, like Ge-rich GST, where the SET state shows a remarkable drift due to a crystalline disordered phase [99].
Structural relaxation occurs in a disordered phase, where defects of the liquid phase remain in the material after quenching, annihilating these defects. For example, structural relaxation results in fixing dangling bond or wrong bonds. The high temperature accelerates this relaxation process, leading to an increase of the resistance, the STS and the threshold voltage over time [100]. The increase of STS is due to an increase in the average distance between traps linked to the defect annihilation. Moreover, the defect

reduction results in band gap increase, widening the barrier for electrical conduction and leading the increase of the resistance and higher threshold voltage.
The increase of the RESET resistance widens the resistance window and is problematic for multilevel programming, but is not a reliability issue for single level programming, although the increase of the threshold voltage can make difficult the SET operation.
Read and program algorithms can be adopted to mitigate the drift. Indeed, the increase of the read current or of the read voltage leads to a decrease of the resistance drift [101] (Fig. 2.12). Moreover, the material and the device architecture can be engineered in order to reduce the drift. For example, a confined PCM cell with a metallic surfactant layer demonstrates to stabilize the drift, since the metallic layer provides an alternative conductive path during read operations making the cell immune to amorphous instabilities [102].

2.6 PCM architectures

The choice of the ideal cell structure is determined by many factors such as the density of the cell and its scalability, the power consumption and the number of masks required by the cell integration [103]. PCM cell structures can be distinguished in self-heating cells, in which the heat is generated inside the phase-change material, and heater-based cells where the heater element generates the heating.

The mushroom cell

A conventional heater-based cell structure is the mushroom cell, where a cylindrical heater made typically with TiN is in contact with a thin film of phase-change material. Since the phase-change material is on top of a flat surface, it can be deposited using a standard physical vapor deposition (PVD) technique. In order to provide thermal insulation during the programming operations, the thermal conductivity must be low enough, while the electrical conductivity must be high enough to avoid adding series resistance. Furthermore, the electrode materials must not chemically interact withe the phase-change material and must be able to withstand the high temperatures during the RESET programming. In the mushroom cell, the RESET current depends on many factors, such as the dimensions, electrical and thermal properties of the bottom electrode, the thermal properties of the material that surrounds the bottom electrode and the thermal properties and thickness of the phase-change material [104].

The μtrench structure

The μtrench cell is based on a heater element. In this structure, the contact area between the heater and the phase-change material is defined by the intersection of a thin vertical heater and a trench in which the chalcogenide material is deposited. This expedient allows to keep low programming currents of 600 μA maintaining a compact vertical integration demonstrated using a pnp-BJT selector. Furthermore, endurance of 10^{11} cycles and data retention of 10 years at 110 °C have been shown [79].
The difficulty of obtaining a completely flat surface between the phase-change material and the vertical heater is the main issue of the μtrench cell [103]. The lithographic

alignment requirements of this architecture may influence the multi-megabit array integration and its yield. A self-aligned patterning method to simplify the integration process and to reduce the fabrication costs has been developed. Therefore, a 128 Mb array has been fabricated in a 90 nm CMOS process using a self-aligned patterning method showing a decreased programming currents of 300 μA [105].

The "wall" structure

In comparison to the μtrench architecture, the "wall" cell offers better lithographic alignment tolerances while maintaining good programming current controllability and simplifying the storage element process integration since it allows to save one critical mask [82]. The "wall" cell is constituted by a vertical heater, above which the chalcogenide material is directly deposited.
In this architecture, heat is generated inside the heater element by Joule effect, and then transmitted to the chalcogenide via the contact area interface. Thermal efficiency is determined by geometric parameters, such as heater width, height and thickness, and by physical parameters, such as the heater thermal conductivity. In general, as the heater resistance increases, efficiency decreases. However, as resistance is increased by reducing the heater's width , efficiency deterioration is negligible since also the melted chalcogenide volume scales down. Moreover, physical qualities of the chalcogenide materials can have an impact on thermal efficiency [106].
"Wall" manufacturability was proven in a 1 Gb product based on a 45 nm technology node that features a low programming current of 200 μA.
In this manuscript, most of the PCM reliability studies were performed on "wall" PCM devices.

The bridge structure

In the bridge device, a narrow dielectric layer separates the two metallic electrodes connected by an ultra-thin chalcogenide on the top surface of the insulator. A bridge device implemented with GeSb showed a RESET current lower than 100 μA, a cross sectional area of 60 nm^2 on a 3 nm thin film [107].
However, the main drawback of this cell is its lateral extension that prevents the minimum pitch design typical of vertical structures for high density applications. Nevertheless, the tight control of the chalcogenide thickness, the planar surface for the chalcogenide deposition and its simplicity, make the bridge cell usable for applications requiring less density [103].

The confined structure

In this architecture, the phase-change material is deposited in a small hole on the sidewall of a dielectric material. Since the wall hole can be very narrow, atomic layer deposition and chemical vapor deposition are preferred, while standard physical vapor deposition is not recommended [79, 108].
In a confined cell, the RESET programming current is reduced since the heat is generates within the phase-change material that is surrounded by oxide, improving the

thermal efficiency. However, after RESET operation, all the phase-change material is fully amorphous and does not contain any crystal seeds. Hence, the SET operation requires the crystal nucleation, reducing consequently the speed of confined device compared to a conventional heater-based PCM [109].
The highest endurance of 2×10^{12} was achieved in a confined Sb-rich GST PCM with a metallic layer interposed between the insulator and the phase-change material [110] and an excellent cell scalability to sub-20nm technology was demonstrated [111]. Furthermore, this cell architecture is 3D compatible and it has been used in 3D XPoint product.

2.7 PCM reliability

A reliable memory device should be functional maintaining its performances (e.g., speed, power consumption) for its whole life and should retain data at the ambient temperature for a certain period of time according to its specifications. In PCMs, we can distinguish two main failure causes: the temperature seen by the device and the modification of the composition in the active region over time. The working temperature could be responsible of the re-crystallization of the amorphous phase, or to the structural relaxation of the amorphous phase, leading the drift phenomenon. These two mechanisms have an impact on the data retention of the device. Furthermore, the unwanted increase of temperature in a cell due to the programming of a neighbor cell, named thermal cross talk, can modify the state of the interested cell. The second main failure cause, correlated to the electrical stress during programming, limits the endurance, generating modification in the phase-change composition. This will be discussed more in detail in the following.

2.7.1 Endurance and failure mechanisms

The endurance of a PCM is the maximum number of SET and REST cycles that the device can perform reliably, indicating how many times the memory can be written. For S-SCM, endurance is a critical parameter and must be higher than 10^9, while for M-SCM 10^6 cycles are enough.
We are mainly interested to the intrinsic failure mechanisms that occur within the phase-change material rather than the extrinsic mechanisms, usually due to the integration. During the write operation, the device experiences high temperature and high current densities that can lead to atomic migration. The two failure modes of a PCM are stuck RESET, where the cell remains in the RESET state and is no long able to switch into the SET state, and stuck SET, where the cell cannot switch into the RESET state. The stuck RESET is correlated to void formation [113], otherwise stuck SET is due to a change of the composition in the active region. However, both fails are linked to atomic migration. The atomic migration can be explained thanks to the incongruent melting. In the case of $Ge_2Sb_2Te_5$, from the pseudobinary phase diagram, we can observe that $Ge_2Sb_2Te_5$ is melted as a single phase above 650 °C, but between 630 and 650 °C generates a Sb, Te-rich liquid phase and a Ge-rich solid phase (Fig. 2.13a) [112]. The phase change materials are subjected to the maximum thermal budget during the melt-quench process, which happens during RESET operation. The

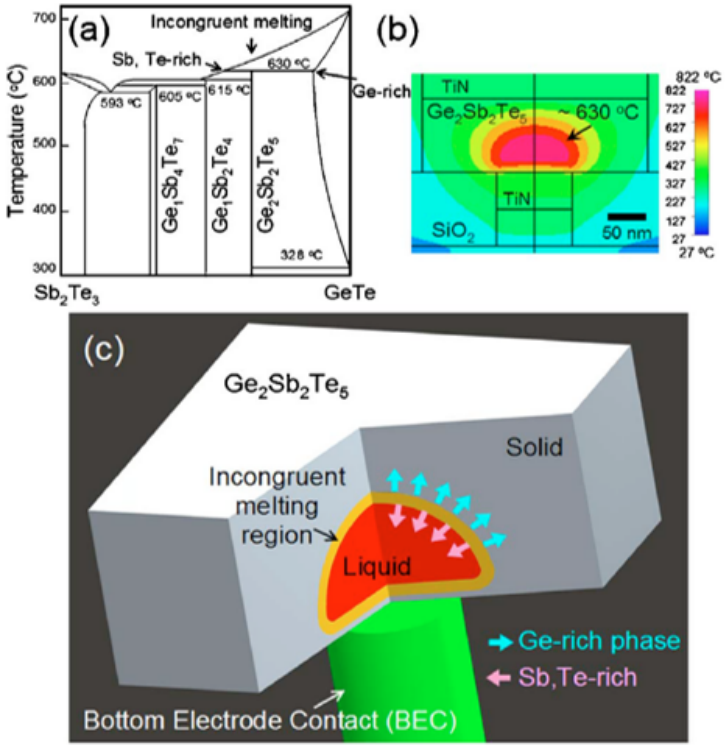

Fig. 2.13. a) The pseudobinary phase diagram between Sb_2Te_3 and GeTe for the analysis of the real PRAM device. b) The temperature profile simulation during the RESET operation. c) The phase separation model during the RESET operation. [112].

incongruent melting zone is expected to appear around the central melting region, as indicated in Fig. 2.13c [112].

Another process named crystallization-induced segregation can explain the variations in stoichiometry seen during cycling [114]. This phenomenon happens when a slow crystallizing phase-change material rearranges forming a local stoichiometry capable of fast crystallization. The crystal growth reinforces the preferred stoichiometry and can segregate elements in a PCM device. Then, the crystallization process strengthens this stoichiometry at the expense of the elements not required for it [114].

It has been demonstrated that the stuck SET failure is reversible since can be recovered by inverting the RESET voltage polarity, confirming that the electric field contributes on endurance degradation with an electromigration process [115]. Hence, voltage polarity change when the RESET resistance goes under a certain value could be exploited to extend the lifetime of the PCM.

The switching between amorphous and crystalline phases is another source of stress in the PCM during endurance, because crystallization increases the density of the material, while amorphization leads a volume increase. The difference in density obtained for $Ge_2Sb_2Te_5$ is about 6% [116]. This volumetric expansions and compressions can modify the SET and RESET resistances, especially during the first life cycles of the device, [117] and creates some voids in the material. However, during all the usable life of the PCM, we can observe variations of resistances, threshold voltage and crystallization temperature that are correlated to decomposition of the active region due to electromigration [117].

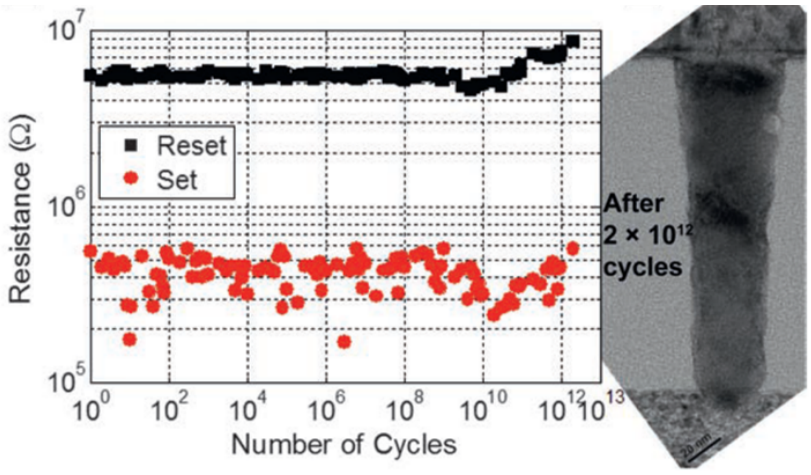

Fig. 2.14. Endurance of 2×10^{12} exhibited by the confined PCM with a metallic liner. The TEM image on the right shows the void-free cell after 2×10^{12} cycles [110].

The RESET pulse has a remarkable impact on endurance, because a power law relationship has been demonstrated experimentally between the endurance capability and the writing energy [118, 119]. The SET pulses seems to do not affect the endurance degradation, that, instead, is correlated to the RESET pulse. However, it has been demonstrated that the cycling capability depends little on the RESET current amplitude but strongly on the RESET pulse width [115]. This means that the time under melt degrades more the endurance than the high temperatures reached increasing the current.
In order to reduce elemental segregation, the cell geometry can be designed symmetrically to maintain the composition at the center of the structure, as in the case of the confined structure [120]. Furthermore, the confined PCM exploits a metallic liner to eliminate voids by Joule heating [119], since it has been found that high temperature heals the voids generated by the density difference between crystalline and amorphous phase [121]. The confined structure with metallic liner allows to achieve the maximum endurance of 2×10^{12} (Fig. 2.14) [110].

2.7.2 Data retention

Data retention fails in a PCM are due to a modification of the programmed resistance over time. While the crystalline phase is stable, the amorphous phase represents the main concern for data retention since it can evolve over time for two main reasons: resistance drift and crystallization of the amorphous phase. As showed in Fig. 4.7, at high temperature, initially RESET resistance can increase over time due to the resistance drift widening the resistance window. This not represents an issue during single level cell programming, but can be a problem during multilevel cell operations. After a certain time, the RESET resistance starts decreasing and, if it goes below a certain value for which it is no longer distinguishable from the SET resistance, gives rise to a data loss.
The failures time of data retention can vary among cells due to device-to-device structure differences and to the randomness of the crystallization process. Fig. 2.16 il-

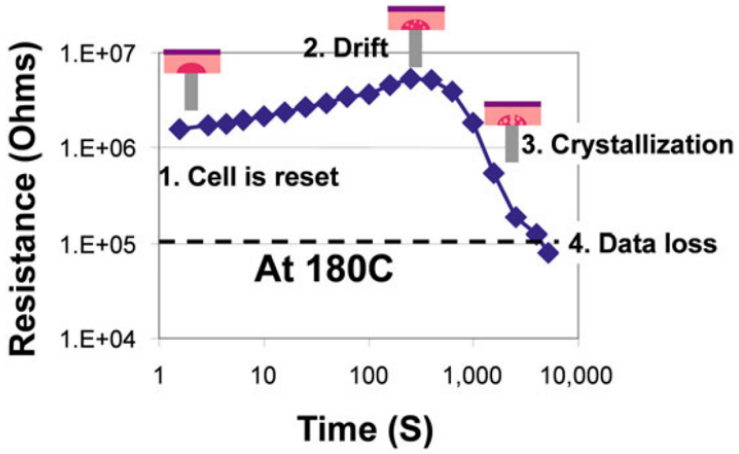

Fig. 2.15. Evolution of a RESET resistance over time at elevated temperature [122].

lustrates the resistance distributions for 512kb RESET devices after bake [123]. A considerable variation in crystallization time among the cells can be observed. It has been found that the early fails are related to the arrangement of the nucleation sites within the amorphous matrix, as represented in Fig. 2.17. Nucleation sites are present in all cells after the RESET operation and the configuration of these sites can change at each RESET programming. In some cases, the nucleation sites growing can form easily a crystalline percolation path giving rise to an early data retention fail. These early fails can be suppressed with an optimized RESET programming algorithm [123]. Although high data retention temperature are not a SCM requirement, in the last years the interest towards applications that require data retention at high temperature, such as automotive, is increased. Indeed, for automotive, data retention specification is 125 °C for 10 years. Other applications can demand to program the PCM before the soldering operation, that rises the temperature above 250 °C for few minutes. Regarding the qualifications of integrated circuits, PCMs must retain data at 90 °C for 1000 h according the JESD47I standard.
Since the low crystallization temperature (about 150 °C) of GST does not allow to meet

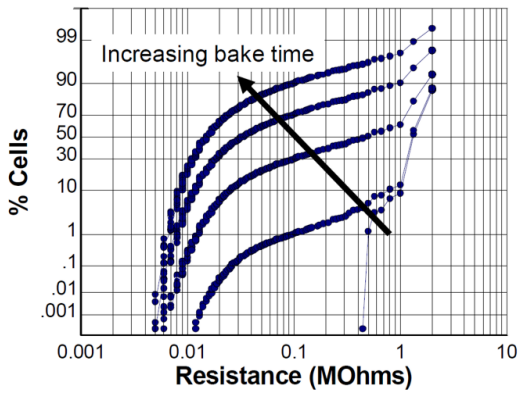

Fig. 2.16. RESET resistance distributions achieved increasing the bake time [123].

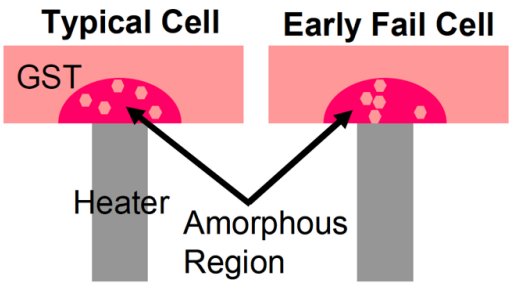

Fig. 2.17. Schematic showing the nucleation sites configuration on a typical RESET cell and on early fail cell [123].

automotive e applications, two main solutions have been investigated to improve data retention in PCM: varying the chalcogenide stoichiometry or doping the chalcogenide with other elements. For example, Ge-rich GST has been demonstrated able to ensure integrity of RESET state after soldering thermal profile and at 150 °C for 10 years enabling automotive applications. In this composition, a compromise must be done with the SET programming speed that results quite reduced compared to $Ge_2Sb_2Te_5$ [124].

2.7.3 Multilevel cell reliability

Multilevel cell capability (MLC) in PCM, enabled by the large resistivity contrast between amorphous and crystalline state, is an important feature to reduce the cost per bit and to make PCM competitive with NAND Flash.
In addition to the high ON/OFF contrast, a gradual transition from SET to RESET state is linked to a robuster MLC. Intermediate states in PCM can be obtained applying pulses with increasing amplitude to a device programmed in the SET state increasing the thickness of the amorphous volume, as shown in Fig. 2.18 until the RESET state is reached.
For multilevel programming, two conventional approaches can be distinguished: programming begins with a RESET pulse and then pulses with incremental amplitude progressively crystallize the cell or programming starts with a SET pulse and pulses with incremental amplitude are used to increase the amorphous thickness [127].
However, MLC in PCMs is challenging due to the resistance drift, cell variability and circuit noise during write and read operations [125]. Drift, which broads the resistance distributions over time, is accelerated by temperature compromising the stability and the reliability of the intermediate resistances at high temperature. Furthermore, the cell variability in a memory array can affect MLC. Structural variations of the cell critical dimensions deriving from the fabrication process translate in electrical variations during the device operation, thus same electrical pulses can result in different resistance values. The most used approach to reduce programming variability is the employment of iterative program and verify techniques, where a sequence of pulses are

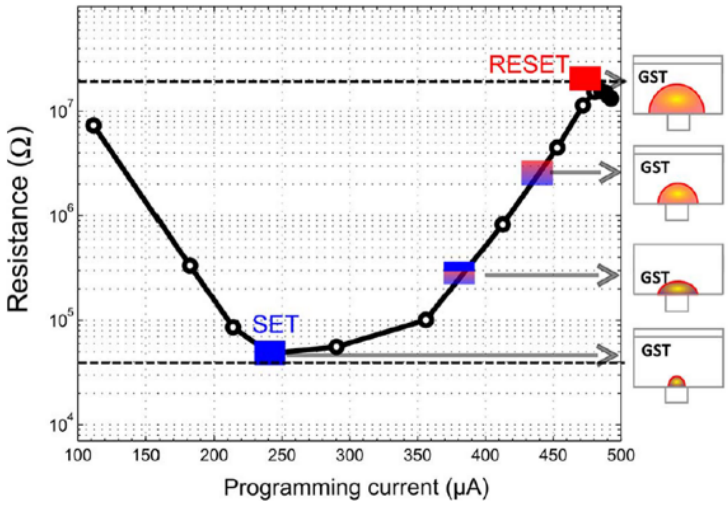

Fig. 2.18. RI curve with the associated intermediate states [125].

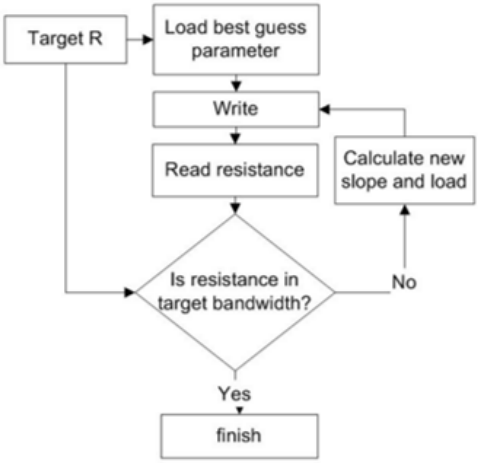

Fig. 2.19. Program and verify algorithm with the adjustement of the pulse slope to achieve 16 intermediate states [126].

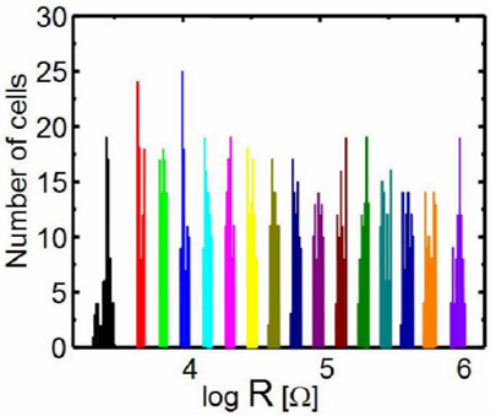

Fig. 2.20. 10×10 array programmed into 16 levels [126].

applied, then the programmed resistance is verified following a loop until the target resistance is reached. Another factor that must be considered for MLC is the intra-cell variability rising from repeated programming cycles. Indeed, SET/RESET cycling induces atomic migration modifying the thermal profile of the cell and thus the electrical pulse necessary to reach the target resistance value. Moreover, data retention for MLC is critical since intermediate states can crystallize faster than RESET states. Indeed a decrease of retention time has been found as the programming voltage decreases wrt the voltage to obtain the fully RESET, while a higher programming voltage is correlated to a better data retention [128].
In addition to the program and verify algorithms, MLC in PCM can be improved engineering the device structure or the phase-change material. For example, a more gradual transition between RESET and SET state can be achieved by N doping in $Ge_2Sb_2Te_5$ [126] and, in the next chapter, we are going to show that an improved MLC is obtained by Si doping. Stable intermediate states are demonstrated in PCM obtained by stacking $Ge_2Sb_2Te_5$, a tungsten layer and a Si-doped $Ge_2Sb_2Te_5$ layer [129]. The best result about MLC in PCM consists of 16 distinct levels achieved using an algorithm, where the amplitude and the slope of the programming pulse trailing edge is carefully chosen based on the resistance achieved in the previous programming iteration, making 4 bits/cell possible in PCM [126] (Fig. 2.19 and Fig. 2.20).

2.7.4 Scaling effects on PCM reliability

Moore's law, affirming that the number of transistors in an integrated circuit doubles every 18 months, is a keystone of electronic and a goal of every silicon-based device, including NVMs, such as PCM. In fact, technological scaling allows to obtain more compact and more performing devices, making scalability one of the main characteristics of PCMs.
In order to determine if PCM is a viable future technology, it is very important to understand how the scaling affects PCM performances and reliability, such as thermal

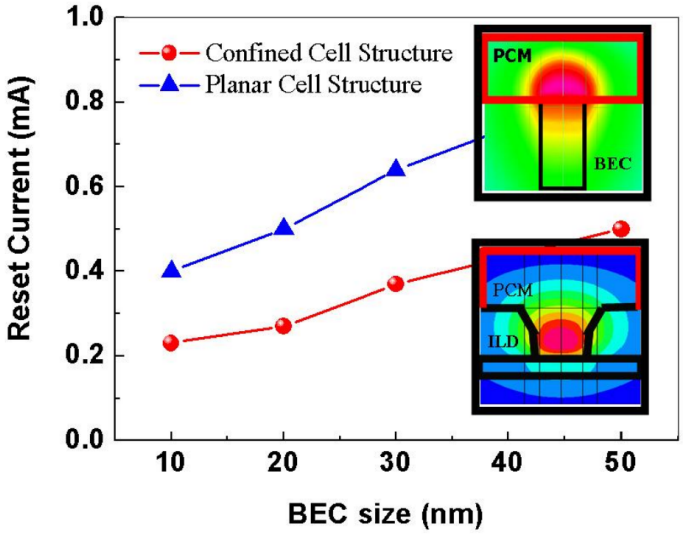

Fig. 2.21. Comparison of RESET current between confined and planar mushroom cell architectures as a function of contact diameter [130].

stability, crystallization speed, programming power, etc.
As the film thickness decreases below 10 nm, it was found that the crystallization temperature increases for GST, N-doped GST, $Ge_{15}Sb_{85}$, Sb_2Te Ag and In-doped Sb_2Te; the increase depends on the material and may reach 200 °C [131]. However, the crystallization behavior of thin phase-change materials is significantly influenced by the encapsulating layer. Indeed, a decrease of the crystallization temperature as the film thickness decreases was observed using metallic interfaces [132], that can produce metal-induced crystallization.
Also the speed can be affected in a different way depending on the phase-change material and the encapsulation. For example, it was observed that, as the film thickness reduces, the crystallization speed decreases in GST and increases in AIST [133].
Moreover, a reduction of the melting temperature was found in thin films [134, 135]. A lower melting point means a reduced power and current required by RESET operation, which is favorable for device performance. In addiction to the film thickness, the cell architecture plays an important role in determining the reduction of the RESET current as shown if Fig. 2.21 [130]. The active volume in a PCM is determined by the electrodes size, therefore a reduction of the RESET current is expected as the electrode contact size decreases [53].
Another significant PCM parameter is the resistivity. When the film thickness is decreased, the electrical resistance for thin films increases slightly for both SET and RESET [136]. Higher resistances result in a greater voltage drop across the material, which can lower switching currents and be advantageous for scaling.
The threshold voltage saturates at 0.8 and 0.6 V for GeTe and Sb_2Te_3 devices if the amorphous volume of the nanowire is reduced. The existence of a minimum V_{th} makes possible to miniaturize PCM to nanoscale scale without unintentionally losing data during reading [137].
In synthesis, phase change materials have highly advantageous scaling behavior; indeed, smaller PCM cells shows better performances than larger cells in terms of programming

currents and powers. Furthermore, the increase of the crystallization temperature for smaller film thickness may improve PCM thermal stability.

2.8 Material engineering in PCM

In PCMs the performances, such as power consumption, programming speed, data retention, programming voltages, are strongly influenced by the the phase-change material used, as indicated in Table 2.1. For example, a low melting temperature consents to reduce the RESET current and a low thermal conductivity of the phase-change material allows to heat efficiently reaching easily the melting point. The crystallization temperature is correlated to the data retention, while the crystallization speed determines the SET pulse duration. Therefore, material engineering is a relevant approach to achieve the desired performances in a PCM device.
Material engineering can be realized mainly by:

- stoichiometry tuning;
- doping the chalcogenide with another element;
- multilayer configuration depositing layers of different materials.

2.8.1 Reference PCM materials : GST and GeTe

The two most studied PCM compounds are $Ge_2Sb_2Te_5$ and GeTe which are both stoichiometric compounds capable of melting without any modification to the composition. $Ge_2Sb_2Te_5$ was first used for optical discs, taking advantage of the strong optical contrast between the crystalline and the amorphous phases. In late 1990s, $Ge_2Sb_2Te_5$ was employed also in PCM devices, exploiting its strong electrical contrast. This material demonstrated a resistance window of two orders of magnitude, the capability to crystallize with pulses of 100 ns and 10 years of data retention at 110 °C [140].
GeTe is a phase change material that can switch at rates comparable to DRAM in 1 ns for both SET and RESET operations [141]. It was demonstrated that as the RESET resistance decreased, the SET process accelerated revealing that GeTe exhibits

Phase change material parameter	**Influence on PCM device performance**
Crystallization temperature and thermal stability of the amorphous phase	Data retention and archival lifetime
Melting temperature	RESET power
Resistivity in amorphous and crystalline phases	ON/OFF ratio
Threshold voltage	SET voltage and reading voltage
Thermal conductivity in both phases	SET and RESET power
Crystallization speed	SET pulse duration, data rate

Table 2.1. Phase change material parameters and the device performances correlated. Adapted from [138].

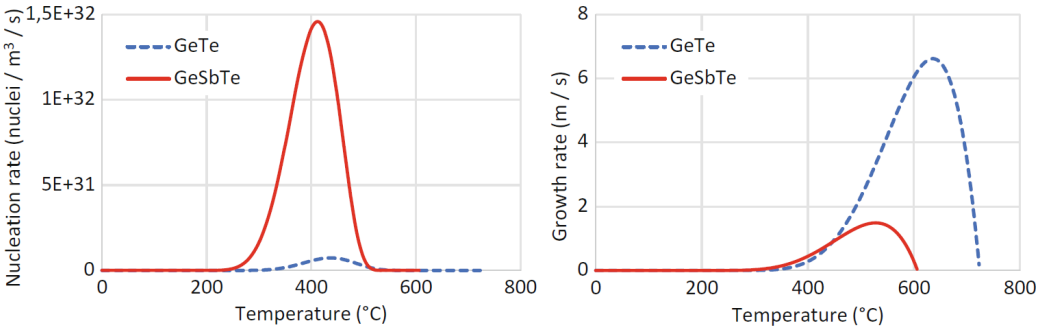

Fig. 2.22. Nucleation and growth rates comparisons in GST and GeTe [139].

growth-dominated recrystallization related to the size of the amorphous area [141]. Indeed, it was found that GeTe has a high growth rate, while GST presents a high nucleation rate and a low growth rate, as shown in Fig. 2.22, thus GST is referred as a nucleation-dominated material [139].
A further difference between the two materials is represented by the R vs T curve: the two step resistance drops in GST is due to the transition from amorphous phase to the crystalline cubic rock salt structure and finally to the hexagonal structure [142], while GeTe shows a single step transition from amorphous to the rhombohedral structure [143].
Stoichiometric GeTe exhibits a high crystallization temperature of 180 °C compared to GST (150 °C), while the activation energy of crystallization of GeTe is slightly lower. Comparing the R-I characteristics of both materials, GeTe shows a higher resistance window of 3 orders of magnitude compared to GST, however, the RESET programming current is similar in both compositions [139].
However, TEM analyses in GST based PCMs revealed that thermal interdiffusion of Sb and Te can generate a nonstoichiometric composition in the active region that is Sb-rich and Te-deficient. This can be due to the moderate temperature gradient in the inactive region between top electrode and active region or to the interdiffusion of Ti from the electrode to GST that interacts with Te leading to the alteration of the pristine GST composition [144]. According to the crystallization induced-segregation theory, the thermal induced motion and elemental segregation at temperatures below the melting point is due to material rearrangement within a fluid and poorly-crystallizing phase-change material that forms a local stoichiometry capable of rapid crystallization, such as Sb-rich GST [114]. Instead, GeTe exhibits a mass density increase of about 9% during crystallization [143] that can cause void formations during programming cycling.
The instability of GST and GeTe based PCMs during endurance makes them not suitable for SCM and pushed the research interest toward innovative phase-change materials for PCM devices.

2.8.2 Doping effects in phase-change materials

In order to improve the data retention of the RESET state, to increase the resistivity of PCM materials and to reduce the programming current, the slight element doping

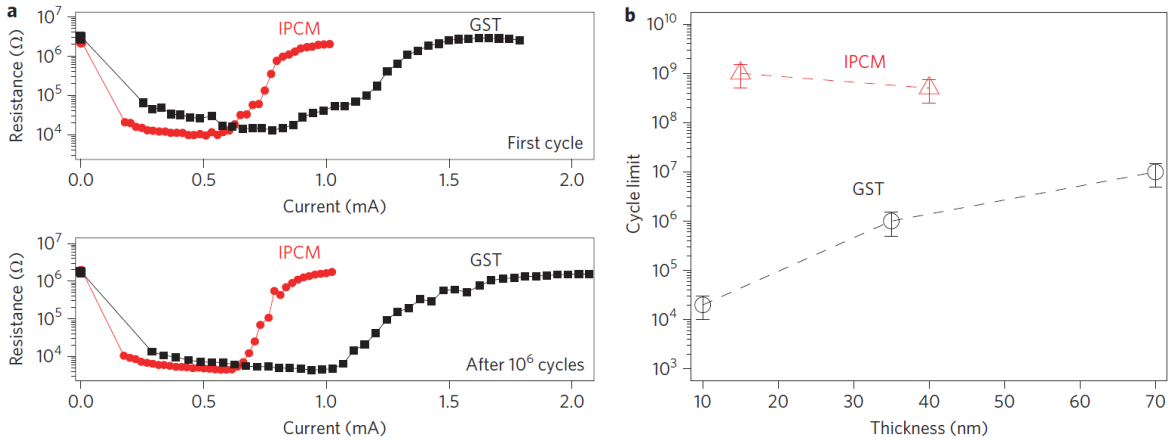

Fig. 2.23. a) R-I characteristic of IPCM devices. b) Maximum number of endurance cycles as a function of phase-change material thickness [149]

of phase-change materials was introduced.
C doping is extensively studied for its many benefits. Indeed, despite a reduction of the resistance window, C doping of GST allows to reduce the RESET current up to about 50%. C introduction in GST decreases the thermal conductivity contributing to the reduction of the programming current [145]. Another benefit of C doping is the improved thermal stability, due to a higher crystallization temperature compared to undoped GST [146].
Another doping element analyzed in literature is N. N-doped GeTe demonstrated an improved data retention with respect to GeTe up to 154 °C for 10 years. The stabilization of the amorphous phase is considered linked to the formation of amorphous GeN agglomerates. N-doped GeTe shows a higher SET speed than GeTe and RESET current similar to GeTe [147].
A current of 100 µA was reached thanks O doping in GST with an archival lifetime of 10 years at 100 °C: the formation of GeO in GST film gives rise to thermal efficiency during RESET operation [148].
Therefore, in most cases, adding dopants to the chalcogenide material improves thermal stability by increasing the crystallization temperature thanks to the creation of separate phases that retard the crystallization process.
In the next chapter, we are going to discuss about the benefits of Si doping in GST.

2.8.3 Multilayer PCM

Multilayer PCM, also called superlattice PCM (SL PCM) or interfacial PCMs (IPCM), was developed in 2011 to reduce the power consumption in PCMs [149]. It consists of the superposition of layers in which different materials alternate, such as GeTe and Sb_2Te_3.
R-I characteristics of SL made by GeTe and Sb_2Te_3 and of conventional GST illustrates that the resistance window is similar in both PCMs, however the RESET current and voltage are reduced of 50% in SL devices (Fig. 2.23a), decreasing considerably the power consumption [149]. As shown in Fig. 2.23b, in SL GST the endurance is higher compared to GST. Furthermore, in GST the endurance decreases as the material

thickness is reduced, while in SL GST it remains high also for the lowest thickness of 15 nm [149]. Therefore, the great potential of SL PCM is also due to the better endurance compared to conventional GST devices. However, the switching mechanism behind the reduced programming current in SL PCM is still under discussion.
The suggested switching methods may be split into two groups:

- the typical phase transition, i.e. partial melting;
- novel phase transition mechanisms without melting, i.e. order-to-order transition or stacking-fault motion induced metal-insulator transition (MIT) due to the flipping of Ge or Sb respectively [150].

The order-to-order transition between SET and RESET state is the first mechanism proposed by Simpson [149]. However, the high energy calculated for Ge atoms flipping is too high to be feasible [151] and this model does not take into account the Ge/Sb intermixing that was observed in TEM images [152].
In 2017, a new mechanism based on metal-insulator switching achieved by stacking-fault motions was proposed [153]. This mechanism shows a lower energy barrier than order-to-order transition. The Sb flipping can break the local stoichiometry, thus, it works also in the Ge/Sb intermixed system. However, the reversibility of the process is still unclear [150].
Furthermore, the low power consumption can be explained by low thermal conductivity of SL GST due to the phonon scattering at the interfaces. Indeed, the thermal conductivity decreases as the the number of interfaces increases [154]. Therefore, as the thermal conductivity decreases, the thermal energies operate in a small area close to the interfaces generating a partial melting in this limited region. Moreover, the interface between the electrode and SL GST can provoke phonon scattering lowering the thermal conductivity and the unmelted material can act as seed for crystal growth [150].
Since the atomic structure of SL PCMs could vary in different devices for atomic intermixing, stacking faults and layer thickness, the switching mechanism can change from one device to another. The advantage of SL materials is the possibility to have many knobs to optimize them, such as searching for innovative materials or for proper substrates, tuning the number of layers and the layer thickness or improving the crystal quality [150].

2.9 Summary of the chapter

PCM working principle is based on a reversible switching between amorphous and crystalline phases that modifies the resistivity of the phase-change material.
Reliability of PCM devices may be impacted mainly by the device working temperature or by the electrical stress during programming that limit the data retention and the endurance respectively. Resistance can evolve over time for resistance drift and crystallization of the amorphous phase. Endurance failure can be due to void formation in the phase-change material, atomic migration, density change between the two phases or to crystallization-induced segregation, that leads towards a material with higher crystallization speed.

PCM exhibits a favorable scaling behavior, since scaling allows reducing the programming power and increase the crystallization temperature improving the data retention. Material engineering is fundamental to boost PCM performances, such as power consumption, data retention and crystallization speed. Indeed, doping can improve the thermal stability and multilayer deposition of different materials can reduce the programming current enhancing the endurance capability.

Chapter 3

GeSbTe and GeTe based PCMs

Material and stoichiometry engineering in PCM is considered the main factor for boosting the device performances. Materials along the GeTe-Sb_2Te_3 tie line were identified for their high programming speed and represent possible candidates for M-SCM applications. Indeed, a high speed of 1 ns has been showed in GeTe based PCM [141]. However, in addition to the speed, a high endurance and the stability of the material along cycling must be taken into account to know if the material is suitable for SCM. On the other side, S-SCM must provide high density at a low cost, preserving, however, endurance and speed higher than NAND Flash. Hence, for S-SCM, multilevel cell (MLC) represents a key solution, since it both ensures high density and does not affect the process costs.
In this chapter, after introducing Sb_2Te_3 doped with Ge, we compare GeTe and αGST based PCM performances to target the specifications of M-SCM applications, focusing on programming speed, material properties evolution triggered during the programming cycles and we investigate how the pulse energy affects the endurance.
Furthermore, we show the suitability of αGST alloy for S-SCM thanks to Si doping which leads an improved MLC capability and retention in PCM devices.

3.1 Material and electrical characterization

In this section, we are going to talk about the material characterization and about the devices, the experimental setup and the testing protocols used during electrical characterization.

3.1.1 Material characterization

Measuring the resistivity as a function of an external temperature is one of the first stages towards characterizing a phase-change material. This measurement allows us to determine the crystallization temperature of the material, to understand the nature of crystallization that can be growth-dominated or nucleation-dominated and to know the activation energy of crystallization.
The resistivity (ρ) can be monitored using the four-probes method, where the probes are placed on a straight line at the same distance from each other (Fig. 3.1). A constant and known electric current (I) is applied on the two outermost probes and the voltage drop (V) on the sample resistance is measured trough the two inner probes [156]. The sample thickness (t) should be less than the distance between probes, that in our case is ∼1 mm, while the sample thickness is 50 nm or 100 nm. The material is placed on top of an insulated layer of SiO_2. The resistivity ρ can be calculated by this formula [156]:

$$\rho = \frac{\pi t}{ln(2)} \frac{V}{I} \tag{3.1}$$

The crystallization temperature increases as the heating rate increases since crystallization is a thermally activated process. Exploiting this dependence, the activation energy of crystallization (E_a) can be estimated through the Kissinger's formula:

$$ln(\frac{dT}{dt} \frac{1}{T_c^2}) \propto \frac{-E_a}{k_b T_c} \tag{3.2}$$

where $\frac{dT}{dt}$ is the heating rate, T_c is the crystallization temperature and k_b is the Boltzmann constant. E_a can be easily extracted from the slope of $ln(\frac{dT}{dt})$ versus $1/T_c$.
Another material analysis used in this work is the X-ray diffraction (XRD) that exploits the diffraction pattern created by atomic scattering of X-ray to reveal the crystalline

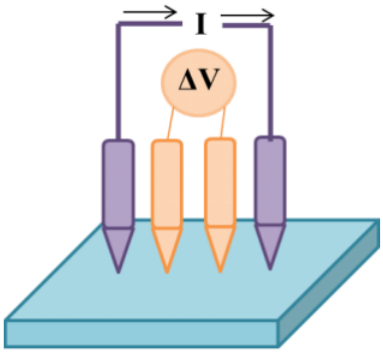

Fig. 3.1. Schematic of four-probes technique [155].

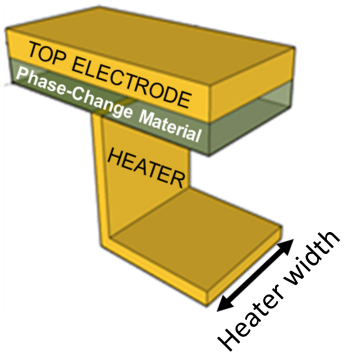

Fig. 3.2. Schematic of a "wall" PCM device.

structure of materials. Amorphous materials do not create any discernible peaks in the diffraction pattern because they lack the periodicity with long-range order. Diffraction patterns consist of a well-defined, narrow and sharp peaks. The position of a diffraction peak depends on the size and shape of the unit cell of the crystalline phase [157].

3.1.2 Electrical characterization

The devices

The PCM devices analyzed in this work were integrated in the Back-End-Of-Lines (BEOL) fabrication of the LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology with a wafer diameter of 200 mm. The majority of the devices studied features a state-of-the-art "wall" structure, while devices with a confined structure will be also treated at the end of the fifth chapter. "Wall" is a heater-based architecture, where the heater is a vertical thin wall and the calchogenide material is deposited above. On the contrary, the confined structure does not have the heater element and is based on self-heating. In this cell, the thermal efficiency is improved since the phase-change material is deposited in a limited area surrounded by oxide.
The "wall" devices were fabricated with different heater widths (40 nm, 50 nm, 80 nm, 100 nm, 200 nm, 300 nm), the phase-change material thickness is 50 nm and the top electrode consists of TiN. A schematic of a "wall" PCM device is reported in Fig. 3.2.
The devices were tested in three configurations:

1. single device (1R), with no selector co-integrated;

2. one-transistor-one-resistor (1T1R) device that is a PCM cell in series with a NMOS transistor connected trough the transistor drain. The transistor is used to control the current flowing trough the PCM cell and features a width of 6700 nm and a length of 500 nm.

3. 4kb arrays (Fig. 3.3) consisting of 256 Bit Lines (BL) and 16 Word Line (WL), for a total of 4096 1T1R devices to perform statistical analysis.

Experimental setup

In PCMs, the cell resistance is the main parameter to measure since represents the memory state. The programming occurs applying voltage pulses, whose rise, width and fall time can be tuned (Fig. 3.4).
The main parameters extracted for a basic electrical characterization are:

- RESET resistance: the maximum resistance of a PCM in the amorphous phase;
- SET resistance: the resistance of a PCM in the crystalline phase;
- Resistance Window: logarithmic difference between the RESET resistance and the SET resistance;
- RESET current: current to bring the resistance from the SET state to a value corresponding to 90% of the resistance window;
- SET current: current needed to program the cell in the SET state;
- threshold voltage (V_{TH}): voltage at which threshold switching occurs.

Different measurements setup were used for single 1R devices and for 1T1R and 4kb devices, which will be described below.

1R setup

We employed an Agilent 81110A pulse/pattern generator to apply the voltage on the device. The length of the voltage pulse can be tuned from 2 ns to 200 ms while the voltage can go from 100 mV to 10 V. A digitizing oscilloscope Tektronix TDS 744A was used to detect the signal and acquire the waveform during the voltage application. The PCM resistance and the current flowing trough the PCM device can be extracted thanks a Agilent 4156C parameter analyzer. A load resistance, tunable between 100 Ω

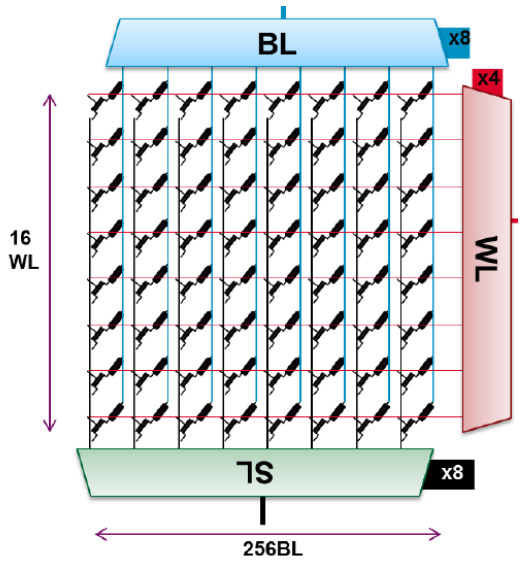

Fig. 3.3. Schematic of a 4kb array.

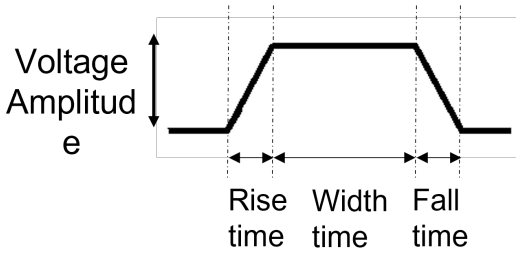

Fig. 3.4. Example of a voltage pulse used to program our PCM devices.

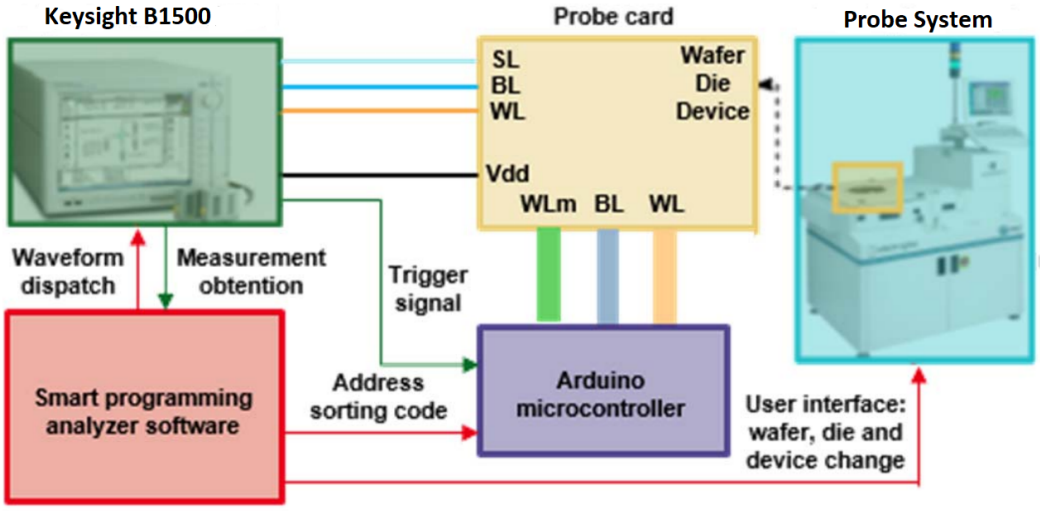

Fig. 3.5. Experimental setup to characterize 4kb arrays. Adapted from [158].

and 10 kΩ, is connected externally in series with the PCM cell in order to limit the current and to measure the current flowing trough the PCM device monitoring the voltage dropping on it.
A Cascade Microtech (12000-5378) probe system with a hot chuck system allows to raise the temperatures during the programming and measurement.

1T1R and 4kb array setup

The load resistance was not utilized in 1T1R devices and matrices due to the presence of the transistor that allows tuning the current. The programming pulse was applied between the drain and the source of the transistor, while source and bulk are short circuited. In a 4kb array, bit-line and source-line are respectively connected to the top electrode and to the transistor source. The array word-line is connected to the transistor gate and allows to regulate the programming current. The electrical setup is divided into two parts: an analogical part to measure the cell resistance and a digital addressing part based on an Arduino microcontroller for the cell selection (Fig. 3.5). In the analogical side, a parameter analyzer Keysight B1500 is used to apply single pulses or train of pulses and to read the current/voltage. Furthermore, the 4kb characterization needs a Keithley 230 Programmable Voltage as VDD power supply; in our case the

voltage was fixed at 4.5 V, corresponding to the maximum voltage applicable for the array programming. Once the measures or the programming have been completed, a trigger signal is sent to the microcontroller which changes the address. A probe card connects the following test pads: 8 pads to address the 256 BLs, 4 pads to address the 16 WLs, 5 analog plugs for bit-lines, word-lines and source-lines, VDD and ground. SMA connectors and a ground plate on the top of the card are necessary to ensure that the analog signal is correctly sent. The measurement time has two components: the first one is the addressing time that is a small contribution to the total measurement time, the second one is the time to write or read. The time to programming the cell resistance can be selected and optimized, however, the read duration represents the major constraint in the measurement time to perform a large amount of operations [158]. In this work, the read operations were performed at a low voltage of 0.1 V.
200 mm Cascade Microtech (12000-5378) probe system was employed to automatically move the probe needles.

3.1.3 The testing protocols

The electrical characterization occurs applying single voltage pulses or train of pulses. The length and the shape of the pulses as well as the voltage amplitude must be chosen carefully according to the type of phase-change material.
Resistance-current (R-I) and current-voltage (I-V) characteristics can be obtained with the staircase up/down sequence that is the preliminary test performed on a PCM consisting on the application of a train of pulses with the same shape and with increasing or decreasing amplitude respectively (Fig. 3.6). In the staircase test, we select rise and fall time with the same duration of 10 ns, while width time is 300 ns. Usually the PCM devices are in the SET state after fabrication and with the first staircase up the cell reaches the RESET state. The subsequent staircase down brings the PCM to a SET state which usually has a resistance lower than that achieved with a single pulse, due to the cumulative effect of the staircase train pulses on the crystallization. Then, the memory is returned to the RESET state with another staircase up that can be exploited to find the RESET current calculated as the current needed to bring the cell to the 90% of the resistance window. The last staircase up applied allows to calculate the threshold voltage.
From R-I and I-V characteristics we can extrapolate the RESET pulse to program the

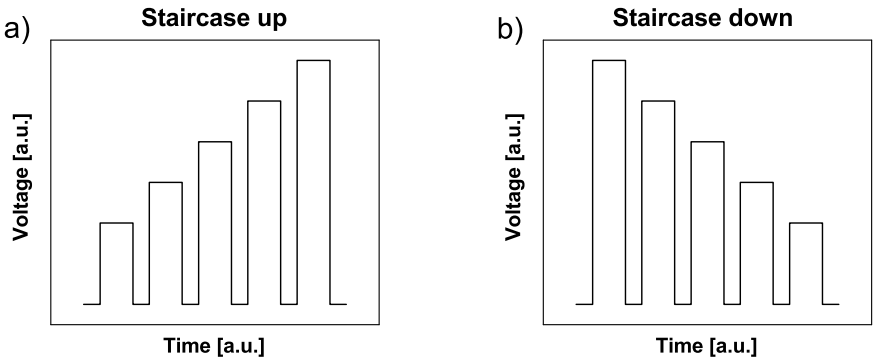

Fig. 3.6. Simplified example of a staircase up (a) and of a staircase (down).

PCM in the high resistive state. The SET pulse can be extracted approximately from the R-I characteristic or applying a staircase up sequence with a RESET pulse before each element of the staircase to verify which is the voltage necessary to obtain the lower resistance. The RESET pulse features a short width time, rise and fall time of 10 ns, while the SET pulse usually has a longer fall time, except for some fast materials that we will analyze in this thesis.

Quasi-static programming

Quasi-static measurements were realized in 1R devices with the same setup described previously. A ramped DC voltage is used to obtain the subthreshold I-V curve of the device, that illustrates the type of conduction in the phase-change material. The conduction is ohmic in the case of a fully crystallized material or can be described by a Poole or Poole-Frenkel law in case of an amorphous material. From the subthreshold I-V characteristic, the STS slope can be extracted from the exponential region in order to provide additional information about the material conduction. STS is defined by the eq. 2.2.

SET speed

Once the SET and RESET voltages are known, the minimum SET pulse time must be found, since the SET programming time is longer than the RESET time (in the order of 20-30 ns) and must comply with SCM specifications. First, the minimum SET fall time is evaluated applying a RESET pulse followed by a SET pulse of 300 ns width time and variable fall time (from 10 ns to 100 µs logarithmically spaced). If the PCM can be programmed into the SET state with 10 ns fall time, we evaluate also the minimum SET width time, fixing the SET fall time at 10 ns and modifying the width time from 20/30 ns to 300 ns, each time reprogramming the device into the RESET state, as in the previous fall time test.
In single devices, a SET carthography can be achieved varying both fall/width time and SET voltage, each time reprogramming the device in the RESET state in order to get the evolution of the measured resistance as a function of both the programming current and pulse time.

Endurance

The endurance test is a sequence of SET and RESET pulses to determine the lifetime of the device that is critical for SCM. Hence, the endurance can be defined as the number of SET/RESET cycles before a failure, that could be a reduction of a resistance window or a stuck SET/RESET.
SET and RESET resistance are read after a certain amount of cycles logarithmically spaced to reduce the testing time. In order to further decrease the number of endurance cycles, we accelerated the degradation of the PCM device applying long SET and RESET pulses and, hence, delivering high energy to the PCM. This strategy allows to perform the endurance test on more devices with reasonable test times to have statistical results.

A test protocol, described in the next chapter, was realized to extrapolate the maximum endurance achievable with the minimum programming time, by performing endurance with different SET and RESET width times.
The endurance test with logarithmically spaced reading does not allow to catch all the resistance variations along the SET/RESET cycling. For this reason, we performed hundreds cycles reading the SET/RESET resistances after each cycle to evaluate the cycle-to-cycle variability before and after an endurance stress.
Furthermore, during cycling, the PCM behavior can be monitored measuring the R-I characteristic, the STS, or evaluating the SET speed and the data retention.

Data retention

The stability of the programmed state over time is evaluated trough data retention measurements at high temperature (>100 °C). In this thesis, data retention has been performed programming a 4kb array in a certain resistance, baking the wafer at a chosen temperature for a specific period of time, and then reading the resistance at room temperature. The stability in time of the programmed states is significant for S-SCM.

Multilevel programming

Multilevel cell capability is another main feature of SCM since consents to increase the device density reducing the technology cost. Between SET and RESET resistance, there are many resistance levels programmable, however, it is not obvious to find the right pulse to obtain a reproducible intermediate resistance with low variability among the whole matrix. First, we need to verify if the intermediate resistive states with low variability can be achieved preprogramming the array in the SET state or the RESET state. In our work, the intermediate states were obtained by controlling the programming current through the addressing transistor, tuning its gate voltage. Then, the right

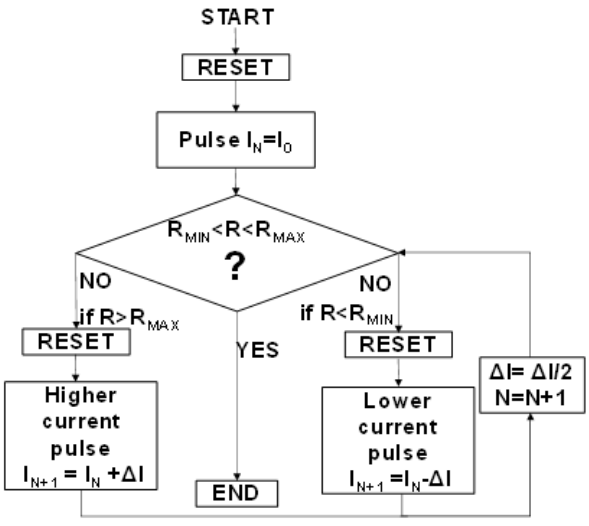

Fig. 3.7. Schematic of the PV algorithm used in our work.

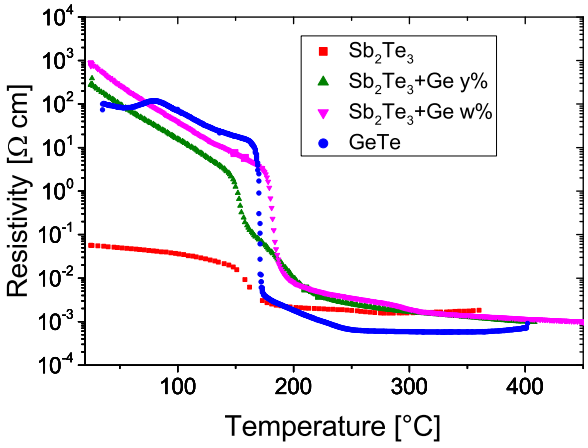

Fig. 3.8. Resistivity of as-deposited Sb_2Te_3, Sb_2Te_3+Ge y%, Sb_2Te_3+Ge w% and GeTe as a function of temperature measured at a rate of 10 °C/min.

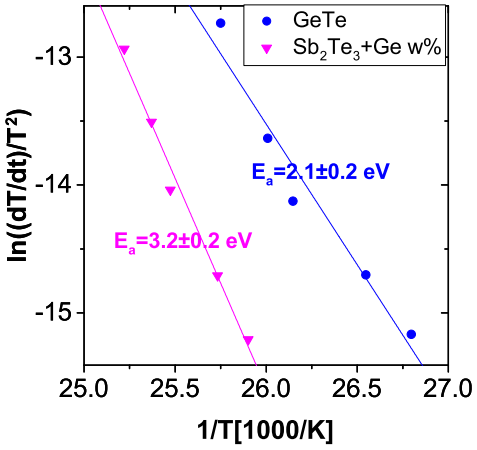

Fig. 3.9. Kissinger plot of GeTe and Sb_2Te_3+Ge w% for activation energy extraction.

pulse time must be found doing attempts with programming pulses of different width or fall times.
A program and verify approach was used for Si-doped GST preprogramming the array in the RESET state, then the programming current is updated at each iteration depending on whether the resistances obtained are lower or higher than the target range. The protocol used is shown in Fig. 3.7.

3.2 Sb_2Te_3+Ge

Sb_2Te_3 could be a PCM material meeting high switching speed required by SCM due to its growth-dominated crystallization [159]. Additionally, Sb_2Te_3 features a low melting temperature, which is helpful in reducing the RESET programming current and the energy consumption. However, the low crystallization temperature of amorphous Sb_2Te_3 limits remarkably the data retention of PCM devices based on this composition. An effective way to increase the thermal stability is doping Sb_2Te_3 with elements such as Ag, In, As, Se or Ge [160]. In particular, Ge can provide amorphous stability increasing the crystallization temperature, since it enters Sb/Te lattice substituting Sb or Te and bonding with Te [160].

Sb_2Te_3 and Sb_2Te_3 doped with two different percentages of Ge (w>y, w∼15) were compared with GeTe measuring the resistivity in temperature of as-deposited full sheet samples (Fig. 3.8). The resistivity of as-deposited Sb_2Te_3 film is very low likely because has partly crystallized due to its low crystallization temperature (85 °C) [161]. When a small amount of Ge is added into Sb_2Te_3, the thermal stability is improved. Indeed, Ge dopant leads to higher resistivity at all annealing temperatures and to a higher crystallization temperature compared to un-doped Sb_2Te_3. GeTe and Sb_2Te_3+Ge w% have almost similar crystallization temperature, but GeTe activation energy of crystallization is ∼1eV lower than Sb_2Te_3+Ge w%, indicating a better thermal stability for Sb_2Te_3+Ge w%.

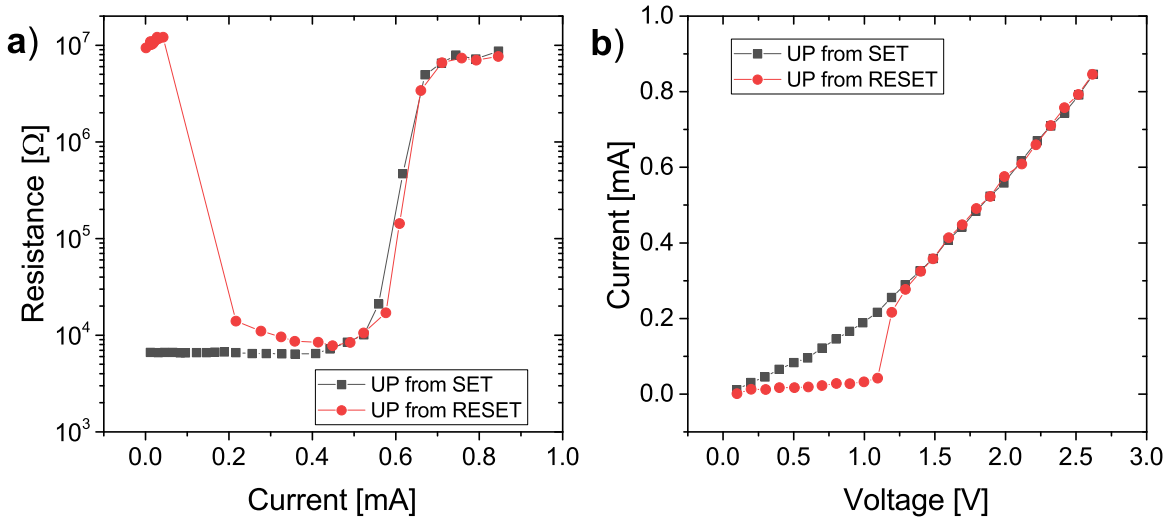

Fig. 3.10. R-I (a) and I-V (b) characteristics of a Sb_2Te_3+Ge w% PCM device with a heater width of 100 nm.

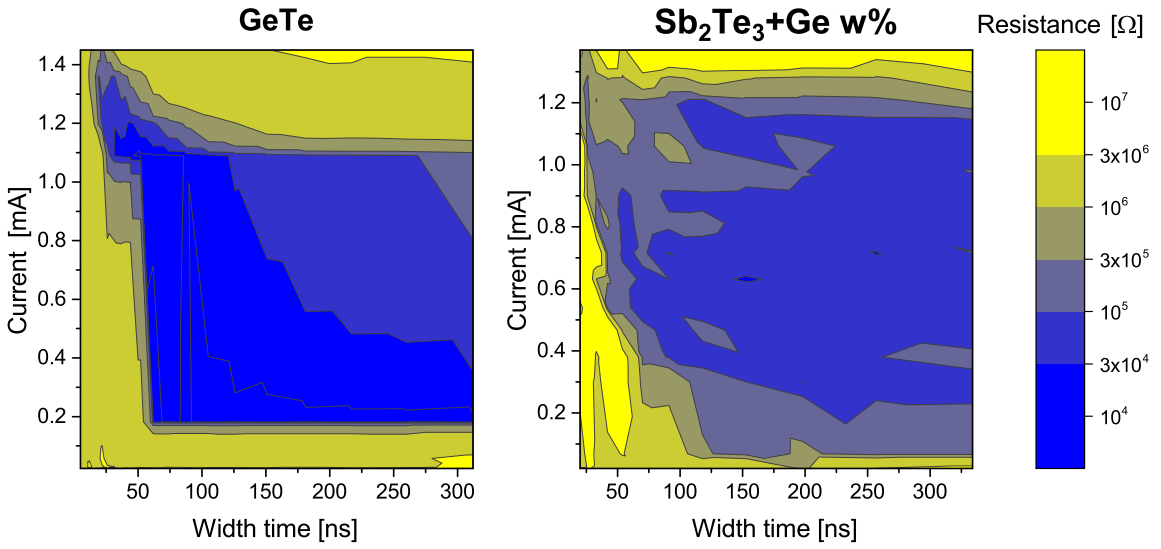

Fig. 3.11. SET programming cartographies. Resistance is represented as a function of the pulse width time and of the pulse current for both GeTe and Sb_2Te_3+Ge w% based PCM.

Fig. 3.10 shows the R-I and the I-V characteristics of a Sb_2Te_3+Ge w% PCM device. In Fig. 3.10a we can observe a high resistance window of 3 orders of magnitude and a steep transition from the RESET state to the SET state typical of a fast PCM material. This PCM device exhibits a threshold voltage of ∼1 V as shown in Fig. 3.10b.
The speed cartographies of GeTe and Sb_2Te_3+Ge w% in Fig. 3.10 evidence that both are very fast materials, switchable into SET state with ∼50 ns width time and 5 ns fall time. However, we did not perform statistical analysis of Sb_2Te_3+Ge w% devices, since the Sb_2Te_3+Ge w% array performances were strongly impacted by substrate adhesion problems, typical of Sb_2Te_3 based layers [162].

3.3 GeTe and GeSbTe based Phase Change Memory

GeTe and αGST, that is a composition close in stoichiometry to $Ge_1Sb_2Te_4$, are both phase change materials characterized by a high SET speed [141, 163]. However, in order to address SCM applications, such as 3D XPoint technology, low programming variability at array level and stability of the phase change material along endurance are fundamental to ensure the reliability in high density memory arrays. In this section, we compare αGST and GeTe mainly in terms of the most important specification for SCM, i.e. speed and endurance, highlighting the evolution of the material properties during cycling.

GeTe and GeSbTe compositions developed and analyzed are highlighted in the Ge-Sb-Te ternary diagram of Fig. 3.12. Resistivity of as-deposited amorphous full sheet layers as a function of temperature (R-T), reported in Fig. 3.13, was measured by four-probe technique heating the sample at a rate of 17 °C/min. The inset of Fig. 3.13 shows the activation energy of crystallization calculated by Kissinger method in both materials. The drop in resistivity after 150 °C corresponds to the transition from the amorphous to the crystalline state. The crystallization temperature of GeTe is higher wrt αGST, however the crystallization dynamic is different in the two layers as the activation energy of the crystallization is higher in αGST. Indeed, the two materials show different crystallization mechanisms. The crystallization involves nuclei formation in the amorphous matrix and successive nuclei growth. A material is growth dominated if the crystallization happens thanks to the fast growth of few crystal nuclei, leading to a steep amorphous to crystalline transition in the R-T plot as observed in GeTe [141]. On the other hand, a material is nucleation dominated if crystallization relies on the high nucleation rate rather than on the growth rate, which on the contrary is low. This is the case of αGST, which exhibits a nucleation dominated crystalliza-

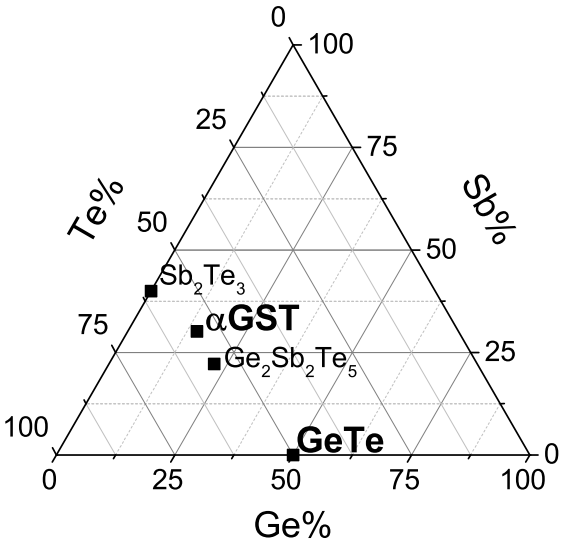

Fig. 3.12. Ge-Sb-Te ternary diagram highlighting the PCM materials analyzed in this work: GeTe and αGST.

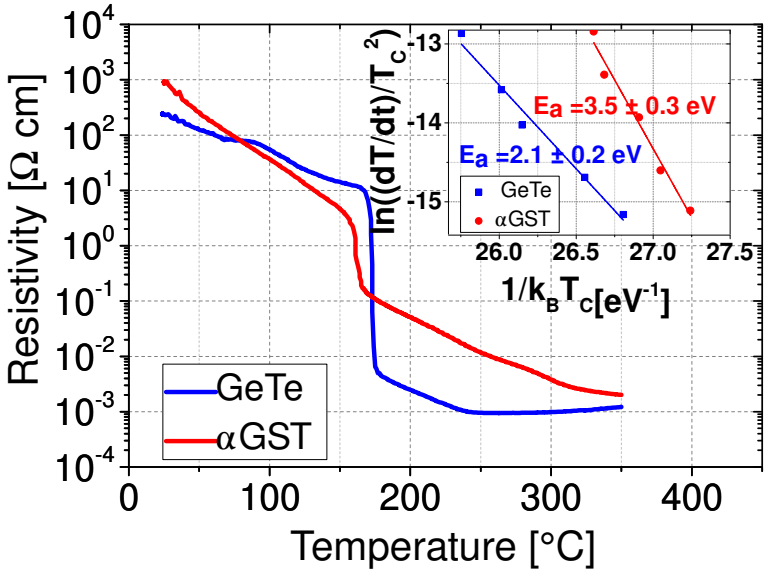

Fig. 3.13. Resistivity of as-deposited amorphous GeTe and αGST as a function of the temperature. Inset: Kissinger plot for Activation Energy of crystallization (E_a is the slope of the Kissinger plot) extraction.

tion [91], also highlighted by a more gradual reduction of the resistivity (i.e. grain growth) in the R-T plot. Anyway, the resistivity evolution of GeTe must be analyzed also in the light of a faster aging of GeTe layer after air exposure wrt αGST due to the the method used to measure the resistivity, which can result in a partial air exposure of the GeTe material in the area of contact between the probes and the material.
GeTe and αGST were integrated in state of the art "wall" PCM devices into the Back End of Line (BEOL) of the fabrication of LETI MAD based on 130 nm CMOS technology. To accomplish statistical analysis, the measurements were performed in 4kb arrays consisting of 1T1R devices with a heater width of 100 nm.
RESET and SET preliminary distributions in 4kb arrays are achieved with optimized current pulses (Fig. 3.14). SET operation in this case is performed with a single long pulse (width time of 300 ns and fall time of 100 µs) in order to reach the minimum resistance value achievable in the devices under investigation. Only single pulse programming approach was considered in our tests, without any program verify strategy. The high resistance window of about two orders of magnitude is verified for both materials. However, the GeTe SET state shows a higher variability wrt αGST.

3.3.1 Speed analysis

We evaluated the programming speed in 4kb arrays analyzing the SET speed, since SET operation (involving the material crystallization) is known to be slower wrt RESET operation in PCM. SET pulses with incremental width and optimized current amplitude were applied, before each SET pulse the devices were programmed into the RESET state (Fig. 3.15). GeTe shows capability of 50 ns SET time, despite a high variability within the 4kb array mainly due to a part of the population remaining in the RESET state. In αGST, SET operation can be obtained only with pulses higher than 100 ns. However, low resistance variability is obtained for 100 ns pulse duration in

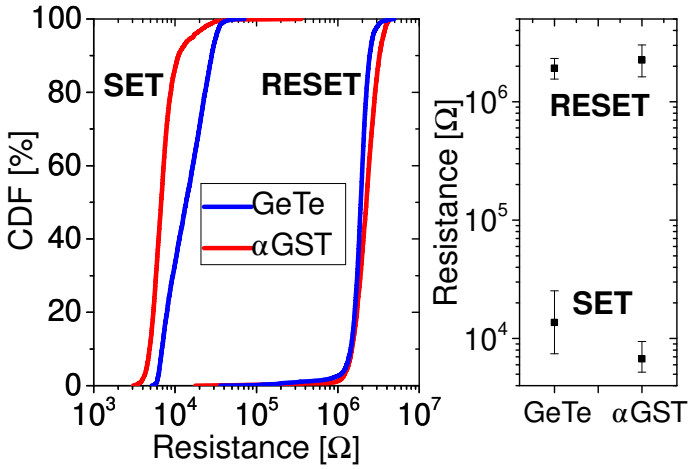

Fig. 3.14. Cumulative distributions of RESET and SET resistances for GeTe and αGST 4kb PCM arrays. On the right, the median and the standard deviation of the distributions are summarized, obtained with optimized RESET and SET pulses.

both materials (Fig. 3.15b). Nevertheless, it should be noticed that the maximum speed achieved is limited by the measurement setup used for arrays, indeed a switching speed of 1 ns was already demonstrated for SET and RESET in GeTe single devices [141]. Therefore, our speed results should be considered for statistical material comparison more than minimum absolute SET pulse duration. The benefit of the pulse fall time increase is more evident in αGST where a constant decrease of the SET resistance is achieved down to less than 10 kΩ (Fig. 3.16a). Moreover, αGST shows the capability of an even more reliable SET state wrt GeTe thanks to pulse fall time increasing, demonstrated by the considerable reduction of resistances variability (Fig. 3.16b). We think that it could be related to the different crystalline nature of the two materials. αGST has different crystalline phases and morphologies, and the degree of crystallinity can be easily tuned with a consequent large resistivity variation, whereas GeTe presents a single amorphous to crystalline phase transition. Moreover, the higher vacancies density in the crystalline lattice of cubic αGST favors a higher crystal reorganization wrt GeTe [164, 165].

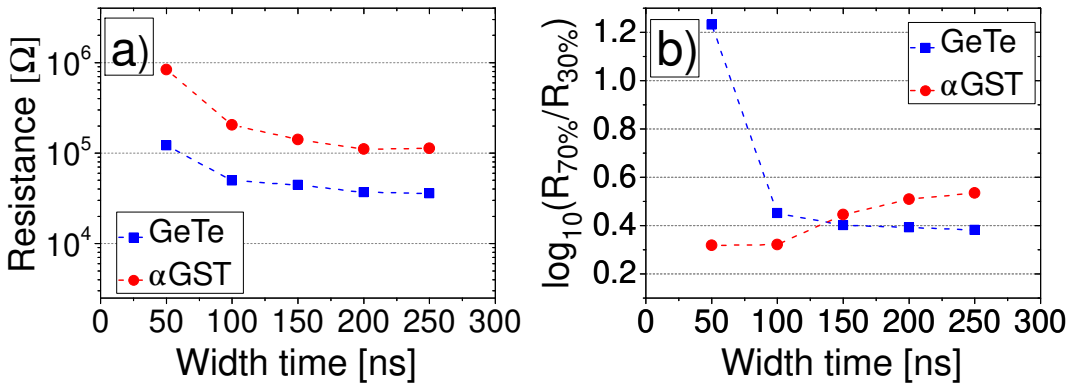

Fig. 3.15. SET programming speed tests performed in 4kb PCM arrays with constant pulse fall time (10 ns) and increasing pulse width: evolution of the median of the resistance values (a) and of the resistance spread (b) are reported.

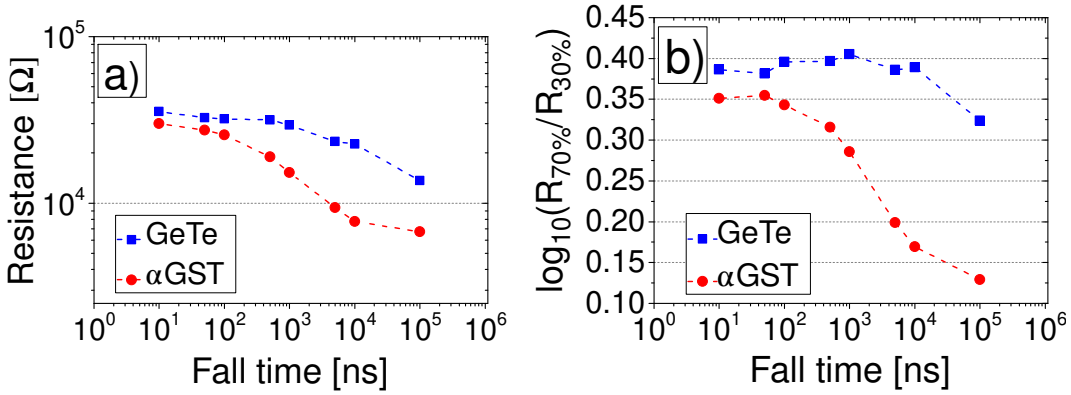

Fig. 3.16. SET programming speed tests performed in 4kb PCM arrays with constant pulse width (300 ns) and increasing pulse fall time: evolution of the median of the resistance values (a) and of the resistance spread (b) are reported.

3.3.2 Data retention analysis

We performed retention tests on RESET state to compare the amorphous phase stability in both materials. We annealed at 100 °C the 4kb arrays programmed in the RESET state after different number of cycles up to 10^4 cycles (Fig. 3.17). GeTe shows a higher stability wrt αGST even after 10^4 cycles, according to previous results reported about GeTe compared to standard $Ge_2Sb_2Te_5$ [166]. The higher nucleation rate at 100 °C in αGST [91] leads to the higher probability of the appearance of nuclei wrt GeTe, with the consequent decrease of the RESET resistance. Nevertheless, αGST shows an interesting retention improvement after cycling, together with a reduced variability. This improvement of data retention could be attributed to an evolution of the material along cycling. As previously reported for standard $Ge_2Sb_2Te_5$ [167], the material could undergo a stoichiometry evolution in the active volume due to a progressive increase of Sb concentration [144], leading to a higher immunity to recrystallization of the cor-

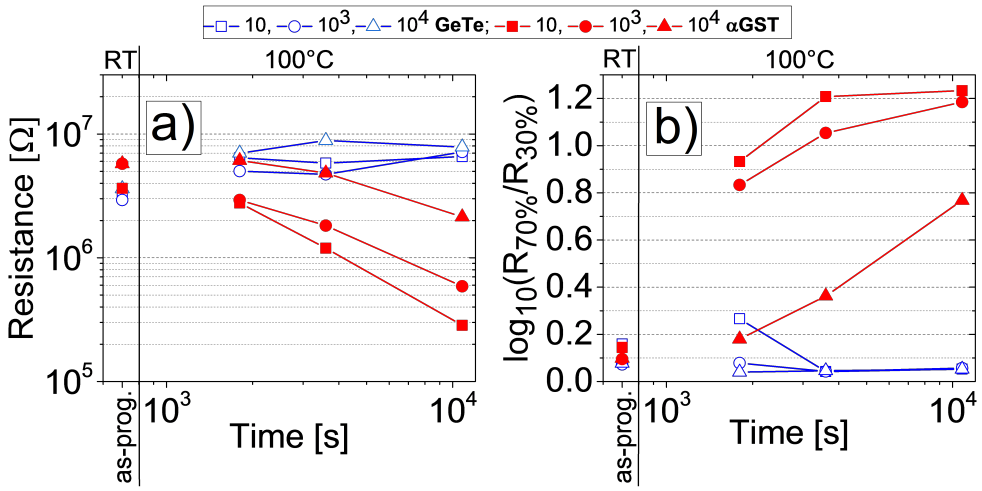

Fig. 3.17. RESET state retention at 100 °C for GeTe and αGST. RESET resistance in 4kb arrays, median (a) and variability (b), are reported after programming (as-prog.) at room temperature (RT), their evolution in time post an 100 °C anneal performed after 10 cycles, 10^3 cycles (in 1000 devices) and 10^4 cycles (in 100 devices) is reported.

respondent amorphous phase, indeed the crystallization temperature of Sb rich αGST reported in [168] is 205 °C that is much higher than that of αGST shown in Fig. 3.13.

3.3.3 Endurance

In order to compare the impact of cycling in GeTe and αGST, we accelerated the degradation phenomena applying a sequence of long SET and RESET pulses (i.e. width time 10 μs). In Fig. 3.18 the RESET and SET resistance states evolution are reported for both materials as a function of the cumulative energy applied on the devices along cycling (E). GeTe, despite a stable resistance window, shows a fast degradation of both programming states after about 0.3 mJ (i.e. 10^4 cycles). On the contrary, αGST preserves a reliable programming even after more than 1 mJ (i.e. more than 10^5 cycles). To understand the material evolution ongoing, we analyzed the change of the subthreshold conductivity of the amorphous phase along cycling for both materials. In the subthreshold regime, the electrical transport in our materials is well described by a Poole conduction ($\ln(I/V) \propto V$) [169], which is linked to the presence of a high trap sites density (i.e. short trap to trap distance Δz), as can be seen in Fig. 3.19a. The subthreshold slope evolution (defined as STS = $d\ln(I)/dV$ in the subthreshold regime) is correlated with the trap density as shown in eq. 2.2. The STS calculated for both materials along cycling is reported as a function of E in Fig. 3.19b. We observe a decrease of STS in both materials with a similar power law trend:

$$STS \propto E^{-\lambda} \tag{3.3}$$

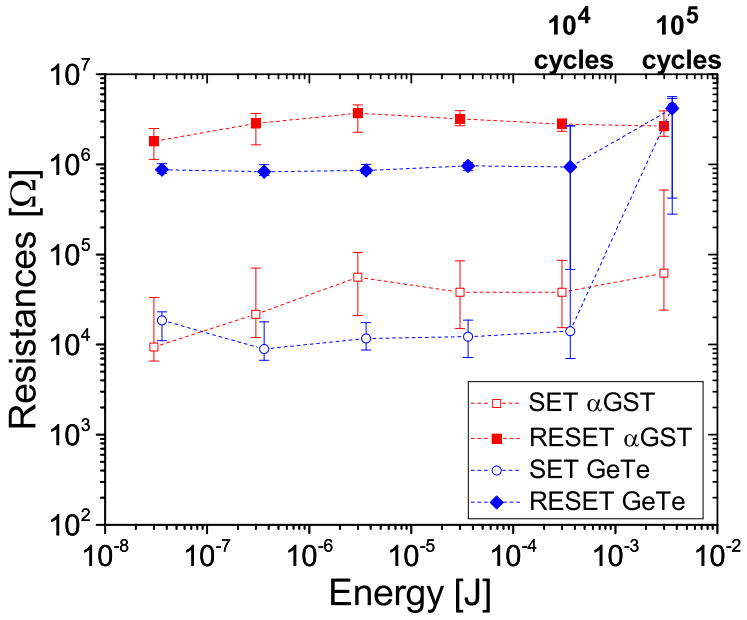

Fig. 3.18. Endurance performed on GeTe and αGST with long RESET and SET pulses (10 μs). Evolution of SET and RESET resistances are reported as a function of cumulative pulses energy (E) in 70 devices. Median, 16th and the 84th percentile (that correspond to one standard deviation σ) of resistances have been represented.

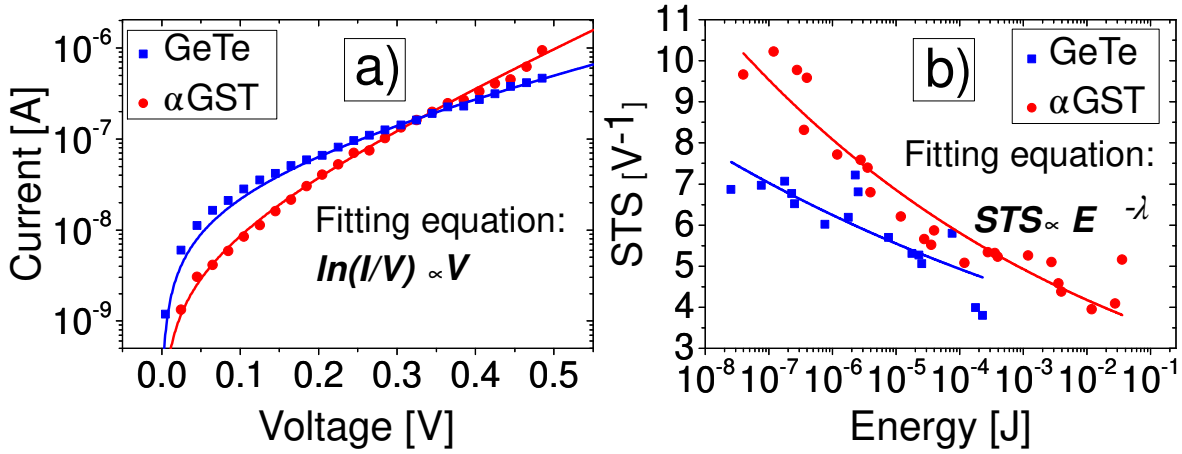

Fig. 3.19. a) Subthreshold characteristics of RESET devices before cycling. b) STS evolution as a function of the cumulative pulse energy along cycling (E), described by a power law (λ coefficient is material dependent).

To be noticed that a variation of STS is not directly reflected by a resistance evolution (e.g. Fig. 3.18) since reading operations are performed at low electric fields, while the STS is extracted at higher electric fields.
A higher STS in αGST is an evidence of a lower density of defect sites wrt GeTe [170]. Moreover, the decrease of STS along cycling confirms a material evolution that is not necessarily a precursor of endurance degradation. This is supported by the fact that αGST shows perfect SET and RESET operations even after reaching same STS values at which GeTe shows programming failure. This evolution is driven by the high tem-

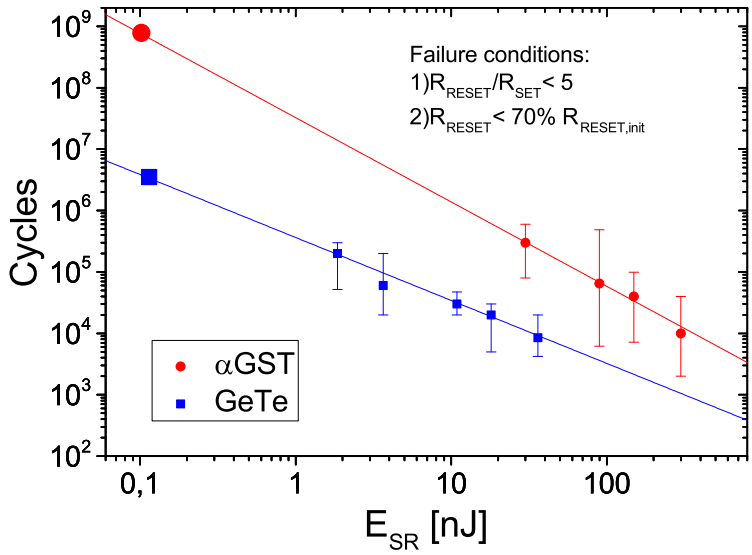

Fig. 3.20. Cycles number achieved for different SET+RESET pulses energy E_{SR} (i.e. increasing SET+RESET pulse duration) and extrapolation at 0.1 pJ. Each test was performed on a population of 70 devices. Median, 16th and the 84th percentile (corresponding to one standard deviation σ) of number of cycles are represented.

perature gradient achieved in the device during the programming, which can contribute to the stoichiometry change and atomic displacement in the active volume of the cell. These results confirm what is already observed in retention measurements. While a Sb enrichment is not detrimental for the switching properties of the device, as certified by record endurance of 2×10^{12} cycles achieved in segregated Sb rich alloys [110], a slight segregation or stoichiometry evolution in GeTe could lead to the degradation of its switching properties [171].
Finally, PCM endurance capability was evaluated performing several endurance tests using different sets of RESET+SET pulses with increasing total energy E_{SR} (Fig. 3.20), in order to take advantage of the power law correlation between the number of cycles (N_{cycles}) and the pulse energy [118]:

$$N_{cycles} \propto E_{SR}^{-C} \tag{3.4}$$

with C a material dependent coefficient. N_{cycles} is the number of cycles obtained before the failure conditions, which take into account both a reduction of the resistance window and a reduction of the RESET resistance. This relationship indicates that the lifetime of the device depends on the energy (i.e. duration) of the single programming pulse. Indeed, longer pulses could involve phenomena such as materials inter diffusion or electromigration, accelerated in a stationary regime that submits the device to a high temperature gradient and localized high electric field. In our endurance test the pulse energy was modified through the variation of the width time of SET and RESET pulses. Considering a minimum energy of 0.1 nJ for single reliable SET+RESET operation (compatible with our previous speed tests), we extrapolated the total number of cycles achievable. We can observe a higher endurance capability in αGST wrt GeTe, reaching about 10^9 cycles for the device size considered. This result can be attributed to the lower density change during phase transition in GeSbTe materials wrt GeTe [172], which could delay the material degradation and void formations.

3.4 Si-doped GeSbTe

In this section, we investigate Si doping in αGSTphase change material to target SCM applications. Si doping benefits on writing current reduction and data retention have been studied in standard GeSbTe alloys [173–176]. We report here for the first time a statistical study of the Si effects on the crystallization dynamic in αGST alloy and its direct link to an improved MLC capability of the PCM devices. Si addition allows to easily tune the crystallization degree in PCM cells, achieving an extremely low variability of the intermediate resistance states. TEM analysis are used to support our findings. Therefore, we demonstrate at statistical level more reliable MLC operations in Si doped αGST 4kb arrays already using a simple double pulse programming protocol. Finally, αGST represents a promising candidate for SCM, since it addresses both M-SCM and S-SCM when the Si content is finely tuned.

αGST and Si-doped αGST with two different Si concentrations, called αGST+Si1 and αGST+Si2, with respectively lower and higher Si percentage, were integrated in state of the art “wall” PCM into the BEOL of the fabrication of LETI MAD based on

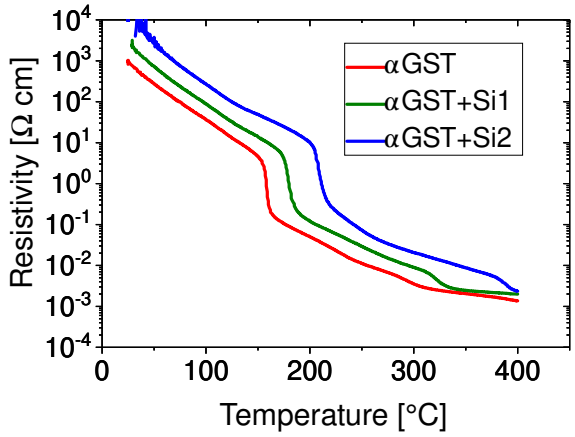

Fig. 3.21. Resistivity of as-deposited αGST, αGST+Si1, αGST+Si2 as a function of temperature measured at a rate of 10 °C/min.

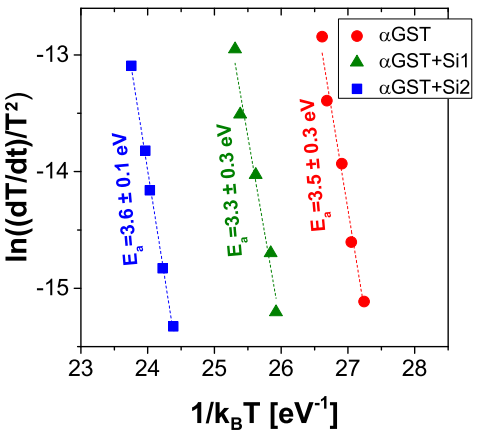

Fig. 3.22. Kissinger plot of αGST and Si-doped αGST for activation energy extraction.

130 nm CMOS technology. For statistical analysis, the measurements were performed on 4kb arrays of 1T1R devices with a heater width of 100 nm.

3.4.1 Si doping effects in PCM devices

The resistivity as a function of temperature of as-deposited amorphous layers is reported in Fig. 3.21. Both the resistivity and the crystallization temperature increase as the Si content increases. It is likely associated to the localization of Si at the grain boundaries, which inhibits the grain growth, retarding the crystallization process [173]. Fig. 3.22 shows the activation energy of crystallization (E_a) calculated by Kissinger method. The crystallization dynamic is similar in the three materials, since E_a, is almost the same in αGST, αGST+Si1 and αGST+Si2. XRD measurements were realized after annealing of αGST and αGST+Si2 samples at 250 °C and 450 °C (Fig. 3.23). At 250 °C same peaks typical of cubic phase appear in both materials. The cubic to hexagonal transition occurs at 450 °C for both materials but in αGST we observe the presence of supplementary peaks wrt Si-doped αGST, linked to a higher degree of crystalline order.
The R-I curves (Fig. 3.24) are obtained by pre-programming a 4kb array in the low resistive state (i.e., crystalline phase) and applying pulses with incremental intensity for each one of the compositions under study. The R-I curves show that the RESET current decreases in Si doped devices with a lower variability demonstrated for the devices doped with the higher Si content. As reported in literature, the RESET current reduction could be associated to the melting temperature lowering with Si content [175] or to a separate Si rich phase that acts as micro heater in the film boosting Joule effect [176].

However, the Si doping leads to a lower crystallization (i.e., SET) speed, as shown in Fig. 3.25. By increasing the fall time, a more reliable SET state with a low variability is achieved in both αGST and αGST+Si2. Nevertheless, a longer fall time is required in Si doped devices to reach the same SET resistance of αGST.
In amorphous chalcogenide materials, the subthreshold conduction is characterized by

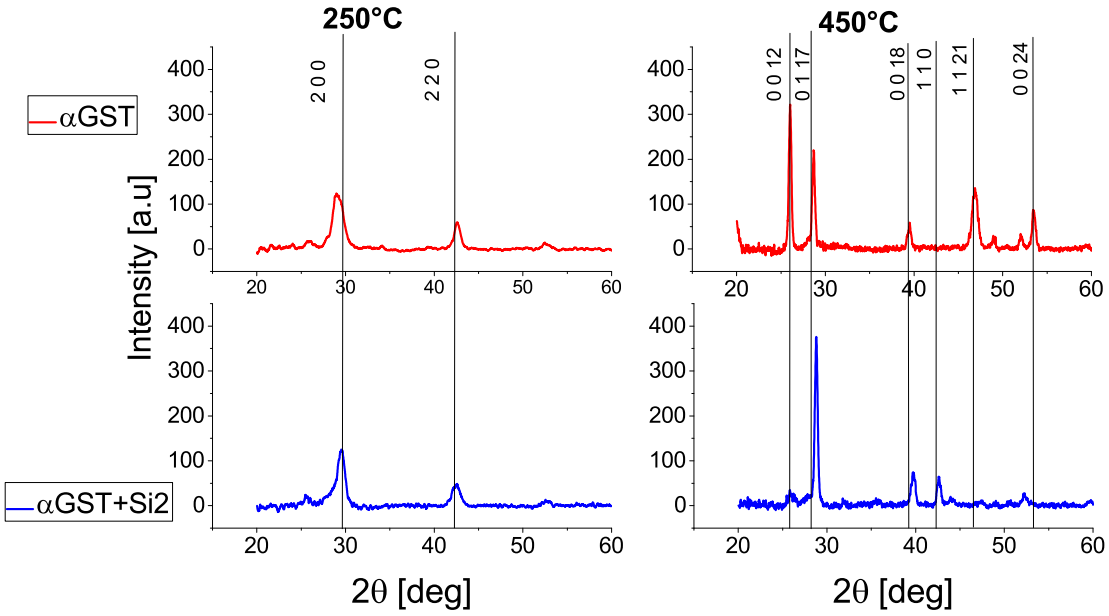

Fig. 3.23. XRD measurements of αGST and αGST+Si2 samples annealed at 250 °C and 450 °C.

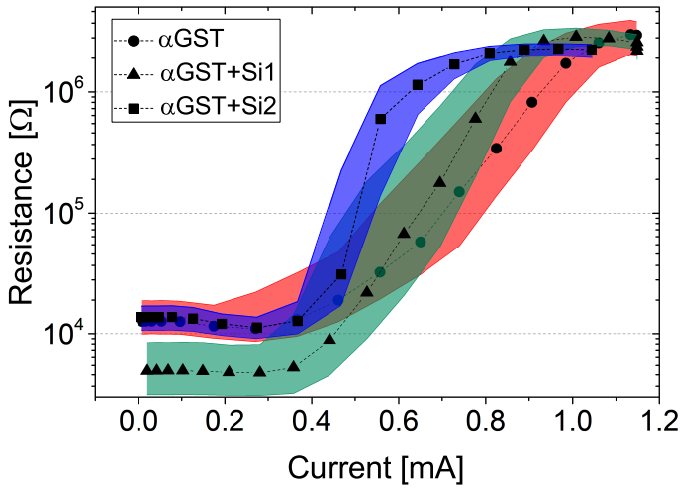

Fig. 3.24. R-I characteristics for αGST, αGST+Si1, αGST+Si2 based PCMs: median, 16th and 84th percentiles (corresponding to 1σ) of the resistance values obtained in 4kb arrays are represented by the shadowed boundaries.

a trap-limited transport. The subthreshold slope is a meaningful parameter, which is linked to the trap density as indicated in the equation 2.2. STS measured in devices programmed in RESET state (i.e., amorphous phase) is reported as a function of $(kT)^{-1}$(Fig. 3.26). It evidences that in αGST the conduction depends considerably on the temperature, whereas STS remains constant with temperature in Si doped αGST. This suggests that the trap-to-trap distance Δz is higher in αGST than in αGST+Si and it indicates that the Si doping is responsible for the higher number of defects in the active material, which gives rise to an amorphous structure with a higher disorder and more stable against crystallization.

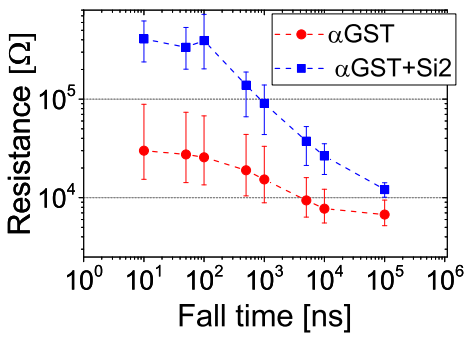

Fig. 3.25. SET programming speed test performed in 4kb arrays with constant pulse width (300 ns) and increasing pulse fall time: median, 16th and 84th percentiles of the resistance values are represented.

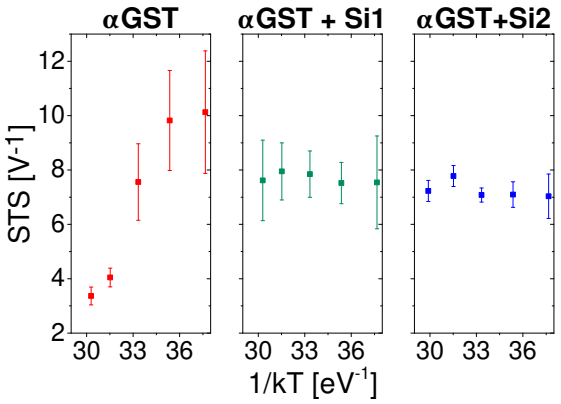

Fig. 3.26. Subthreshold slope (STS) calculated at different temperatures (4 devices for each composition) is represented as a function of $(kT)^{-1}$.

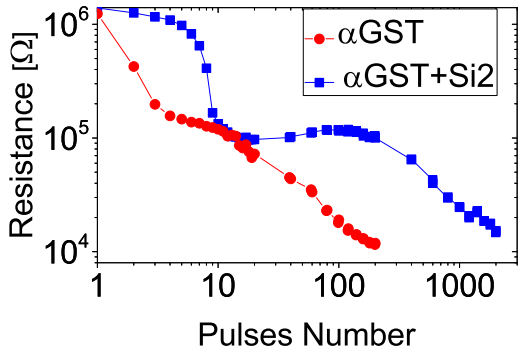

Fig. 3.27. Resistance achieved in αGST and αGST+Si2 devices, starting from a RESET state, applying consecutively a sequence of short pulses with 10 ns rise/fall time and 20 ns width time.

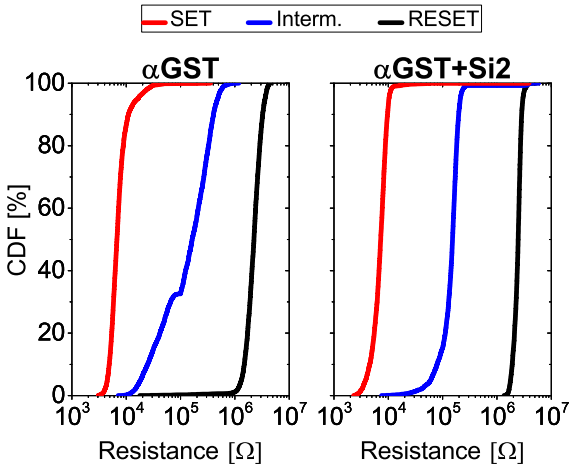

Fig. 3.28. Cumulative distributions of resistances measured in αGST and αGST+Si2 4kb arrays. The intermediate state is achieved with a current of 0.2 mA and a pulse width time of 1 µs.

We analyzed the crystallization process applying a series of short pulses (20 ns) in αGST and αGST+Si2 devices pre-programmed in RESET state (Fig. 3.27). As expected, a gradual crystallization is observed in αGST. On the contrary, αGST+Si2 resistance decreases and stabilizes at about 10^5 Ω, and only after applying about hundred pulses the resistance starts to decrease again down to the same αGST SET resistance. Therefore, Si retards the crystallization process and brings the advantage of a reliable intermediate state. This behavior is statistically confirmed in 4kb array using a single squared pulse of ∼1 µs, which allows obtaining an intermediate state of about 10^5 Ω with low variability (Fig. 3.28); diversely, in undoped αGST the variability achieved with the same pulse shape is higher than αGST+Si2.

Transmission Electron Microscopy (TEM) images of αGST+Si2 devices programmed

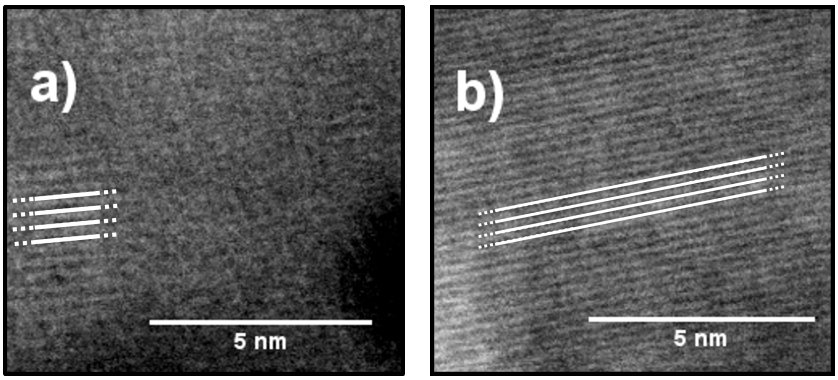

Fig. 3.29. TEM images performed in the active region of two αGST+Si2 devices programmed respectively in the intermediate state (a) and in the SET state (b).

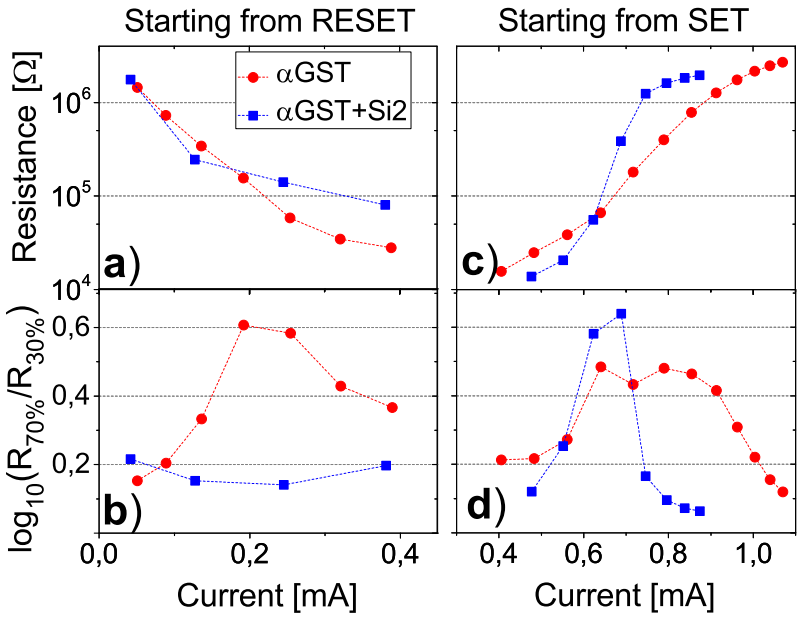

Fig. 3.30. Intermediate states achieved starting from RESET state (a,b) with 1 µs square pulses and from SET state (c,d) with 300 ns square pulses. Median (a,c) and variability (b,d) of the resistances in 4kb arrays are represented.

in the intermediate state previously described (Fig. 3.29a) and in SET state (Fig. 3.29b) evidence that the SET state features a long range crystalline structure, whereas the intermediate state contains localized crystalline grains embedded in an amorphous matrix.

3.4.2 MLC analysis in Si-doped PCM

In order to define the best protocol to achieve multiple resistive states, we applied programming pulses of different durations and amplitudes, by bringing the memory in the RESET state (Fig. 3.30a-b, Fig. 3.31) or SET state (Fig. 3.30c-d) before each one of the applied pulse. In αGST, the variability is higher for each test realized:

the variability with a "bell shape" indicates that, unlike the intermediate states, only RESET and SET state show a low variability.

The application of pulses with incremental intensity on the crystalline material is not effective for MLC programming in both compositions (Fig. 3.30 c-d). On the contrary, starting from RESET, all the resistance states programmed with a 1 µs width time in αGST+Si2 exhibit a low variability (Fig. 3.30b). Fig. 3.31a-b shows that, even if the devices were pre-programmed in RESET state, the intermediate states are not achievable using a short pulse of 300 ns, because αGST+Si2 fails to crystallize properly. A fine control of the median resistance (Fig. 3.31c) with low variability (Fig. 3.31d) of the programmed resistance is obtained only tuning the pulse fall time (i.e., up to 10 µs). Therefore, reliable MLC operations in αGST+Si2 can be obtained if the crystallization dynamics is controlled during cell programming, namely starting from the RESET state.

In order to verify the reliability along cycling of the intermediate states in αGST+Si2, we performed endurance tests with different pulse durations (Fig. 3.32), since the endurance is strongly correlated to the pulse energy. A long RESET pulse of 300 ns, leads to an early degradation of both SET and intermediate states, with a probable Si migration outside of the active region of the device, while a low energy 30 ns RESET pulse allows to reach 10^5 cycles with no degradation of the programmed states (i.e., SET, RESET and intermediate state). Fig. 3.33 shows the evolution of SET, RESET and intermediate state distributions obtained using pulses of 300 ns width time. At the beginning the three states are well distinguishable, but after 10^5 cycles the distributions are more dispersed and the intermediate state starts overlapping with the SET state. Indeed, long pulses involve higher energies that can induce material degradation phenomena such as electromigration or elements interdiffusion [118, 177]. Exploiting this

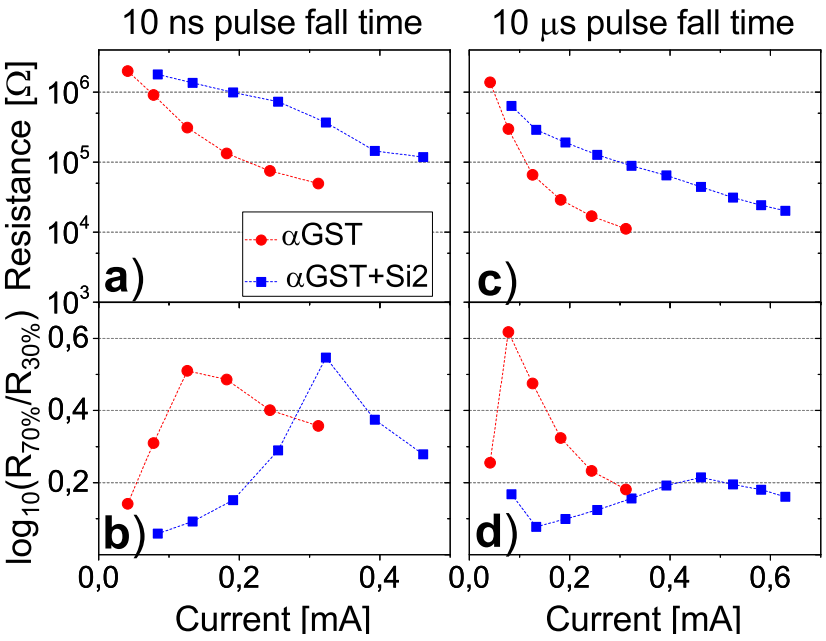

Fig. 3.31. Intermediate states achieved starting from RESET (a,b) with 10 ns pulse fall time (a,b) and 10 µs pulse fall time (c,d), the width time is 300 ns for both. Median (a,c) and variability (b,d) of the resistances in 4kb arrays are represented.

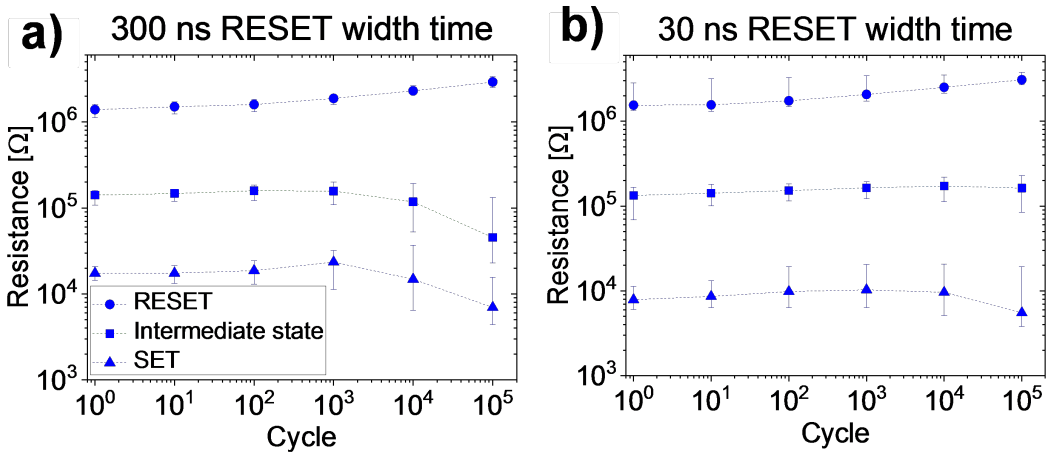

Fig. 3.32. Endurance test performed in αGST+Si2 applying a RESET pulse with a width time of 300 ns (a) and 30 ns (b) on a population of about 100 devices.

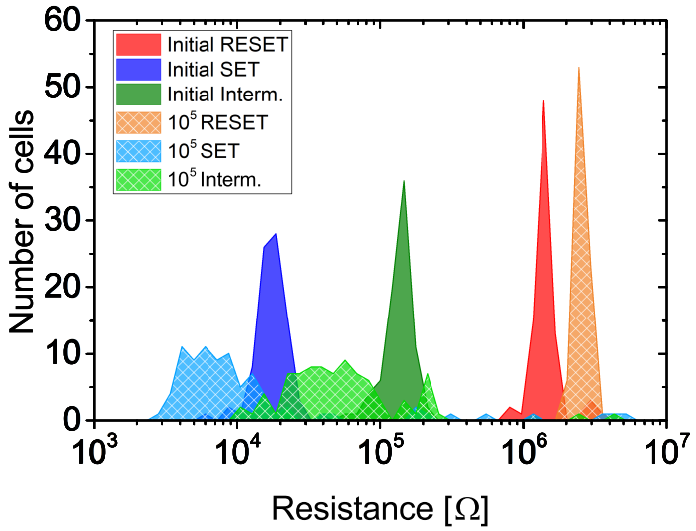

Fig. 3.33. SET, RESET and intermediate state distributions before cycling and after 10^5 cycles in αGST+Si2.

feature, endurance tests with different SET/RESET pulses durations (i.e., energies) were realized to extrapolate the maximum endurance achievable with the minimum programming time (Fig. 3.34) that is 100 ns in αGST [178]. The failure conditions used to calculate the number of cycles take into account a reduction of the RESET resistance and of the reading window, moreover we added for αGST+Si2 the condition on the degradation of the SET state, which is correlated to the loss of the intermediate state, as reported in Fig. 3.32a. Indeed, the endurance in αGST+Si2 could be higher than 10^8, but the reduction of SET resistance at about 10^6 cycles is correlated to the loss of MLC behavior, as shown in Fig. 3.35. Therefore, the extrapolated endurance is higher in αGST (close to 10^9 cycles) than in αGST+Si2 (higher than 10^6 cycles), considering standard SET and RESET operations for αGST and reliable MLC operations for αGST+Si2.

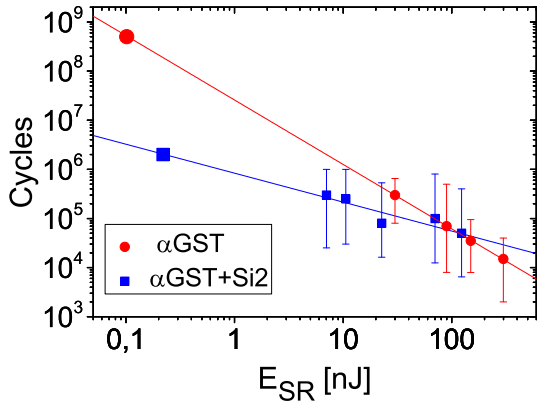

Fig. 3.34. Number of cycles achieved for different SET+RESET pulses duration (i.e., energy) in αGST and αGST+Si2 devices allowing to extrapolate a higher endurance in αGST. Each condition was applied on a population of about 40 devices. Median and 1σ are represented.

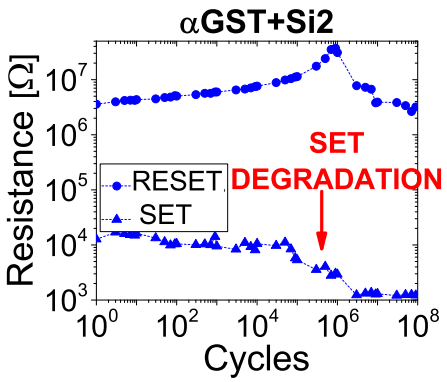

Fig. 3.35. Endurance test performed on a αGST+Si2 device.

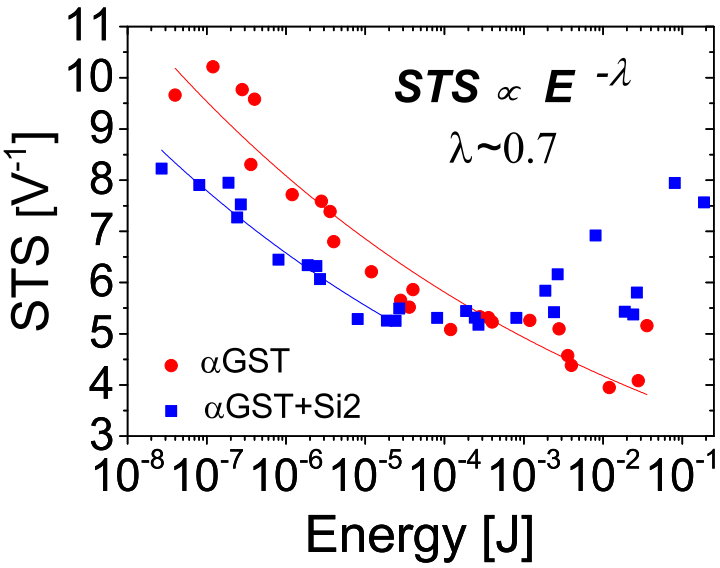

Fig. 3.36. STS evolution along cycling. Energy is the sum of SET and RESET energies multiplied by the number of cycles. Same STS dynamic is observed in both materials (i.e. same λ).

In order to investigate the origin of endurance evolution in αGST+Si2, we studied the change of STS during cycling, being STS inversely proportional to the trap-to-trap density (Fig. 3.36). In both αGST and αGST+Si the STS decreases along cycling with the same trend (i.e. same dynamic and same power coefficient) indicating an increasing of trap density, and as previously observed a likely Sb enrichment in the active volume of the device [178]. However, STS starts from a lower value in αGST+Si, linked to an anticipated atomic diffusion. Indeed, TEM/EDX analyses on devices before and after cycling (Fig. 3.37) show that Sb enrichment and Ge/Te depletion in the active region

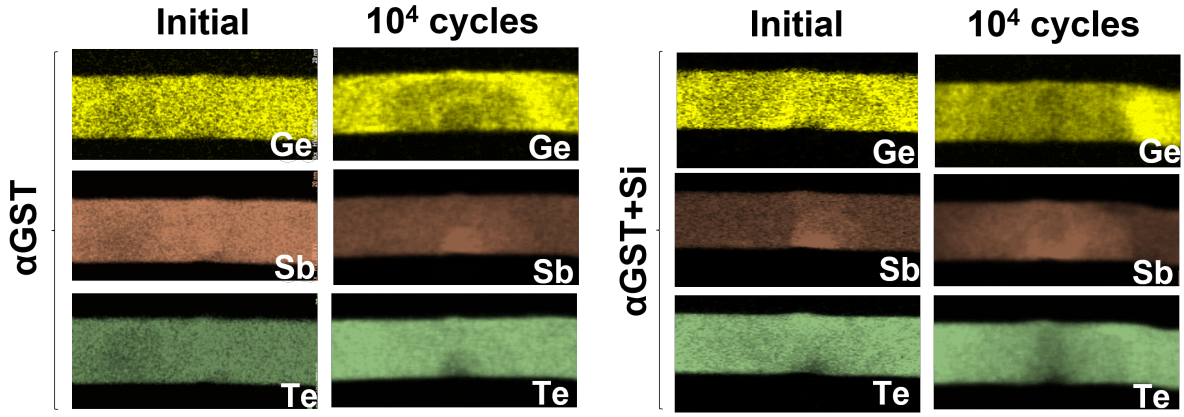

Fig. 3.37. TEM/EDX analyses of αGST and Si doped αGST devices before and after cycling.

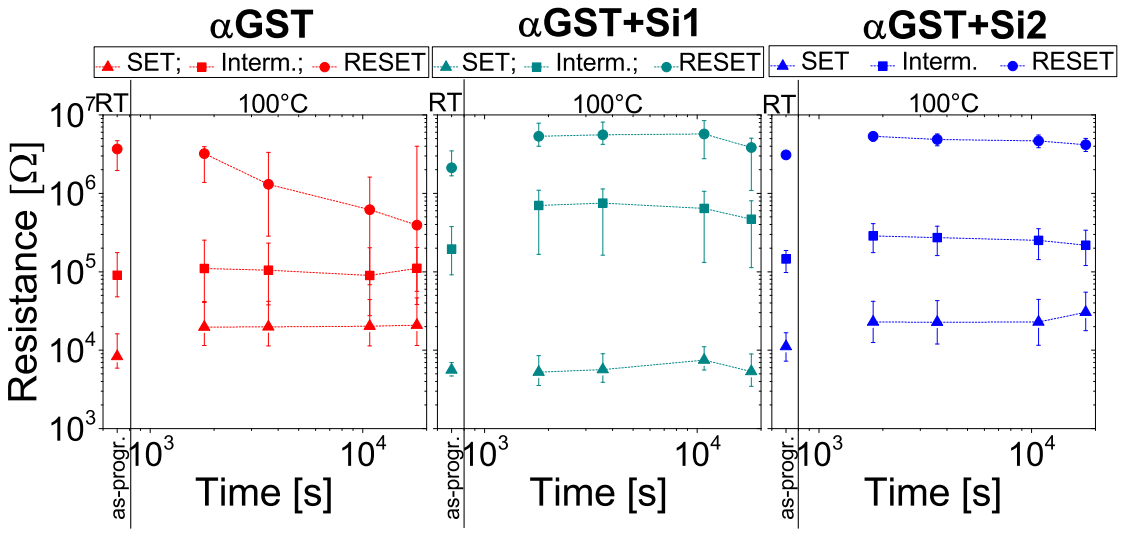

Fig. 3.38. Data retention at 100 °C of SET, RESET and an intermediate state for the three compositions measured in 4kb arrays. Median and 1σ are reported after programming (as. progr.) at room temperature (RT) and along time after annealing at 100 °C.

are already present in αGST+Si before cycling. Si is embedded in the active region, playing a role in retarding the ordering of the crystalline structure (as seen in XRD results). Si mainly substitutes Sb atoms in the crystalline lattice [179] but at the same time it is lighter than Sb. This enhances the Sb elemental diffusion that naturally happens in αGST, leading the system towards the same features of αGST (i.e. high cyclability but loss of MLC reliability).

Furthermore, Si addition in αGST improves the RESET and the intermediate state retention at 100 °C, as illustrated in Fig. 3.38, due to the higher crystallization temperature of Si-doped αGST (Fig. 3.21). Indeed, RESET resistance of αGST decreases at 100 °C increasing the annealing time leading to an overlap of the intermediate state with SET and RESET state; on the contrary, the three states are distinguishable in αGST+Si2 even after a 5h annealing at 100 °C. The impact of the Si addition is demonstrated by the intermediate behavior of αGST+Si1 with respect to the other

two compositions. To summarize, the resistances programmed at room temperature significantly evolve after annealing in αGST and slightly in αGST+Si1 devices, while in αGST+Si2 they remain stable at 100 °C.
In order to take advantage of the improved MLC capability of our devices, a multilevel iterative program and verify (PV) protocol was applied. In this protocol, the programming current (I_N) is updated at each iteration depending on whether the resistances obtained are lower or higher than the target range (Fig. 3.39). The devices are pre-programmed in the RESET state since MLC operation is more reliable starting from the amorphous phase, as shown in Fig. 3.30 and Fig. 3.31. We implemented a single iteration of this protocol in αGST and αGST+Si2 for two target ranges properly chosen between SET and RESET resistances reported in Fig. 3.39b-c. Already using only a double pulse operation (i.e., RESET pulse plus programming pulse), the percentage of devices in the 4kb array reaching the target resistance range is higher in αGST+Si2 than in αGST for both ranges. A second step of this protocol allows even enhancing the MLC programming yield, obtaining only 68% and 71.3% for αGST and 93.3% and 91.2% for αGST+Si2 as final percentages of devices reaching the desired resistance ranges. Therefore, a single PV iteration is not sufficient for αGST to reach the same αGST+Si2 yield, confirming the high suitability of αGST+Si2 for MLC operations.

3.5 Summary of the chapter

In this chapter, we perform a reliability analysis on materials along the GeTe-Sb_2Te_3 tie line, recognized for the high switching speed, focusing on Sb_2Te_3 doped with Ge, GeTe, αGST and Si-doped αGST to target SCM applications.

First, we introduce Sb_2Te_3 doped with Ge that shows a high resistance window of 3 orders of magnitude and a high SET speed. However, Sb_2Te_3+Ge performances were

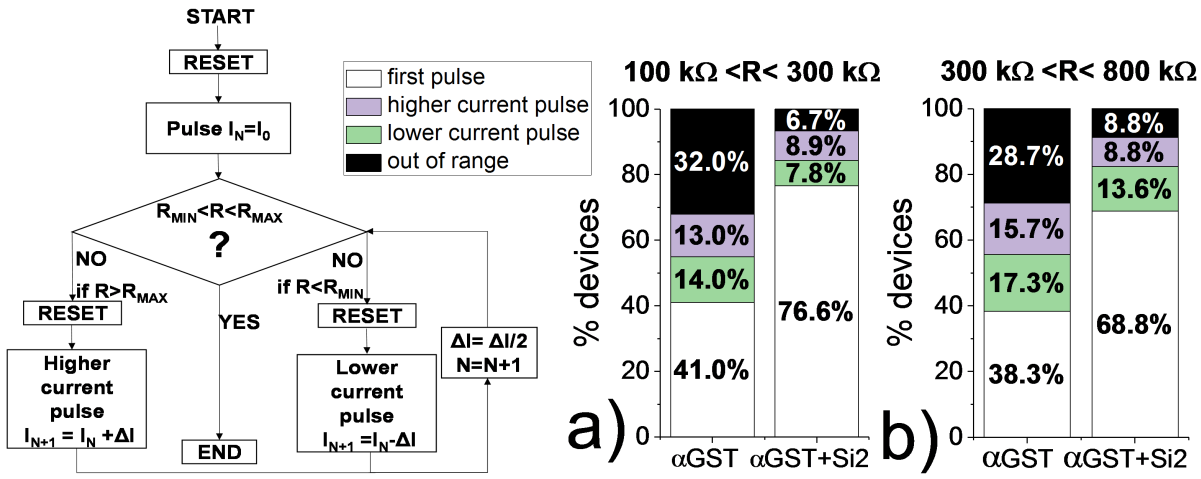

Fig. 3.39. Program and Verify (PV) protocol used to get intermediate resistive states in αGST and αGST+Si2 4kb arrays. The target intermediate resistance range is reported above the graphs a) and b). In white, the percentage of the devices getting the target after the first programming pulse, in purple and in green the devices getting the target after a single step of PV and in black those remaining out of the range.

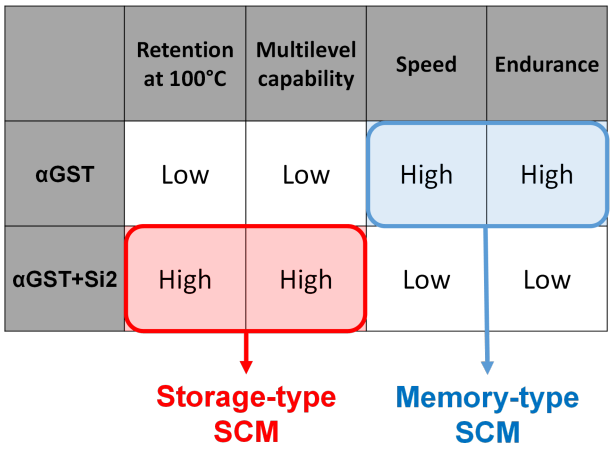

Fig. 3.40. Summary of the features achieved in αGST and αGST+Si2 based PCM devices, showing the possibility to target both S-SCM and M-SCM specifications.

affected by some adhesion problems, typical of Sb_2Te_3 layers.

We analyzed programming reliability of GeTe and αGST based 4kb PCM arrays targeting SCM. High programming speed is ensured in both materials, showing the possibility of a lower SET variability in αGST by pulse fall time control. We provided evidences of the materials evolution during programming operations, thanks to retention and subthreshold conduction measurements along cycling, and by endurance tests we showed how such evolution is more detrimental for GeTe than for αGST. Endurance tests highlighted the dependency of the total cycles number on the single pulse duration. Finally, thanks to this correlation, endurance up to more than 10^9 cycles is extrapolated for αGST, proving its suitability for SCM applications.

Then, we investigate the effects of Si-doping in αGST. We study the crystallization process by electrical tests and TEM analysis, revealing that, in addition to a RESET current reduction, Si retards the crystallization process, without affecting the programming yield. Si-doped devices demonstrate a high reliability of the intermediate states programming, shown statistically in 4kb arrays, already using simple double-pulse operations. Data retention at 100 °C and endurance up to more than 10^6 cycles confirm the high stability of the achieved intermediate states in Si-doped αGST. However, at high number of cycles the MLC capability is reduced, due to an Sb enrichment in the active region shown by STS evolution and TEM/EDX analyses.
Finally, MLC operations tested with a single iteration of an optimized PV protocol, demonstrate a higher yield in αGST+Si2 ($> 90\%$) with respect to αGST (about 70%). These results demonstrate the suitability of αGST alloy for M-SCM applications, thanks to its high speed and high endurance, and for S-SCM thanks to the improved MLC capability and retention obtained by an optimized Si doping (Fig. 3.40).

Chapter 4

Sb-rich GST

Among the several developed alloys, Sb-rich GST is recognized for its high programming speed [180] (i.e. SET time in the ns range) and for its high endurance of 2×10^{12} [110]. In particular, these features make Sb-rich PCMs suitable for SCM to bridge the large gap in performances and cost between DRAM main memory and solid mass storage [17]. In recent years, another technique was explored to customize the performances of PCM that consists in the alternation of layers of different alloys (i.e. multilayered structure), such as GeTe and Sb_2Te_3 in a superlattice configuration [149] or $Ge_2Sb_2Te_5$ and Sb [181]. The main achievement obtained with this solution is the low power consumption, likely attributed to the enhanced thermal properties of the stack [182, 183]. However, a comparison between Sb-rich GST multilayer and equivalent bulk materials and the statistical analysis of the performances and electrical parameters of PCM devices based on multilayers are still missing.
In the next sections, different Sb-rich GST multilayers obtained by alternating layer deposition of GST and Sb targets are compared to bulk equivalent materials obtained by standard co-sputtering. First, material samples are investigated by four probe method to evaluate the resistivity in temperature and by Raman spectroscopy for structural analysis. Therefore, thanks to electrical characterization, we study the performances of the different stacks once integrated in 4kb arrays based on PCM devices featuring a "wall" structure. In particular, we analyzed and compared at statistical level the programming current density, the programming speed and the data retention at high temperature in the different materials. Finally, we focus on the endurance performance of the best multilayer stack developed, reporting about the highly reduced device-to-device (D2D) and cycle-to-cycle (C2C) variability with respect to bulk equivalent PCM devices. The results are supported as well by TEM and EDX analyses.
At the end of the chapter, we analyze briefly confined Sb-rich devices that show functionality contrary to GST devices, with the advantage of a low power consumption compared to standard "wall" PCMs.

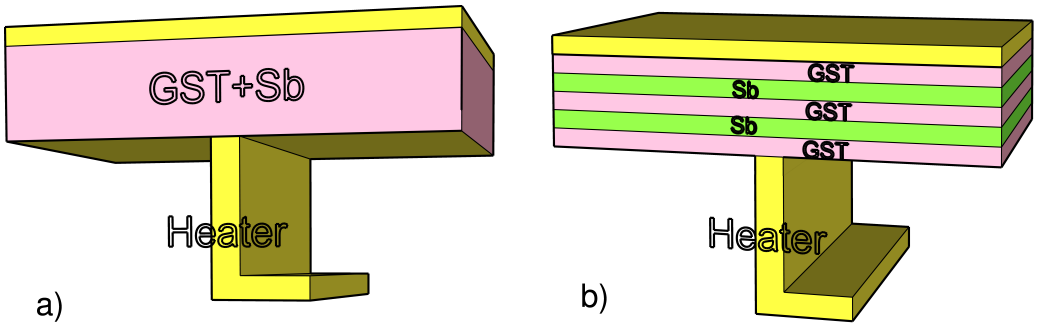

Fig. 4.1. Simplified representation of our "Wall" PCM device, based on a heater element that represents the bottom electrode, in bulk (a) and in multilayer configuration (b).

4.1 Multilayered Sb-rich GeSbTe PCM

Sb-rich GST multilayer stacks were deposited alternating GST and Sb layers, tuning the layer thicknesses down to about 3 nm, and targeting two different stacks respectively with low and high total Sb content (i.e. low and high Sb thickness), both with a total amount of Sb in the range between 40 at.% and 70 at.%. In the following, we will refer to the two different developed multilayer stacks as ML1 (for the one with low Sb content) and ML2 (for the one with high Sb content). The corresponding standard bulk layers with equivalent global stoichiometry of the two multilayers will be addressed as GST+Sb1 and GST+Sb2 respectively. N-doping was as well introduced in ML1 stack in order to observe the possible improvements thanks to N introduction compatibly with what previously reported [184]. This last stack will be addressed as ML1+N.

4.1.1 Materials analysis

Resistivity-vs-Temperature

Sb-rich GST exhibits a growth-dominated crystallization mechanism, in which the crystallization is due to a fast crystal growth at the amorphous/crystalline interfaces [159]. Fig. 4.2a-b reports the resistivity as a function of temperature (R-T) measured by four probes method in as-deposited materials. At the beginning, the materials are in the high resistive amorphous phase and at 200 °C the resistivity remarkably decreases due to the transition to the crystalline phase. The crystallization temperatures of the multilayers (ML1, ML2 and ML1+N) are slightly lower than the corresponding bulk ones (GST+Sb1 and GST+Sb2) (Fig. 4.2c-d), likely due to the heterogeneity induced by the several interfaces intrinsic of the multilayered structure. This is confirmed by the fact that amorphous multilayers present a lower amorphous resistivity with respect to the equivalent bulk layers, due to the presence in their stack of highly conductive Sb layers reducing their total resistivity. Increasing the temperature, we observe an increase in resistivity before the crystallization step, likely related to the intermixing of GST and Sb layers that gives rise to an homogeneous phase. The resistivity curve evidences in each material a one-step transition from amorphous to hexagonal phase, typical of Sb-rich GST [180], contrarily to other nucleation-dominated alloys such as $Ge_2Sb_2Te_5$, in which crystallization occurs more gradually and with intermediate phases from amorphous to cubic and finally to hexagonal phase [142]. Indeed,

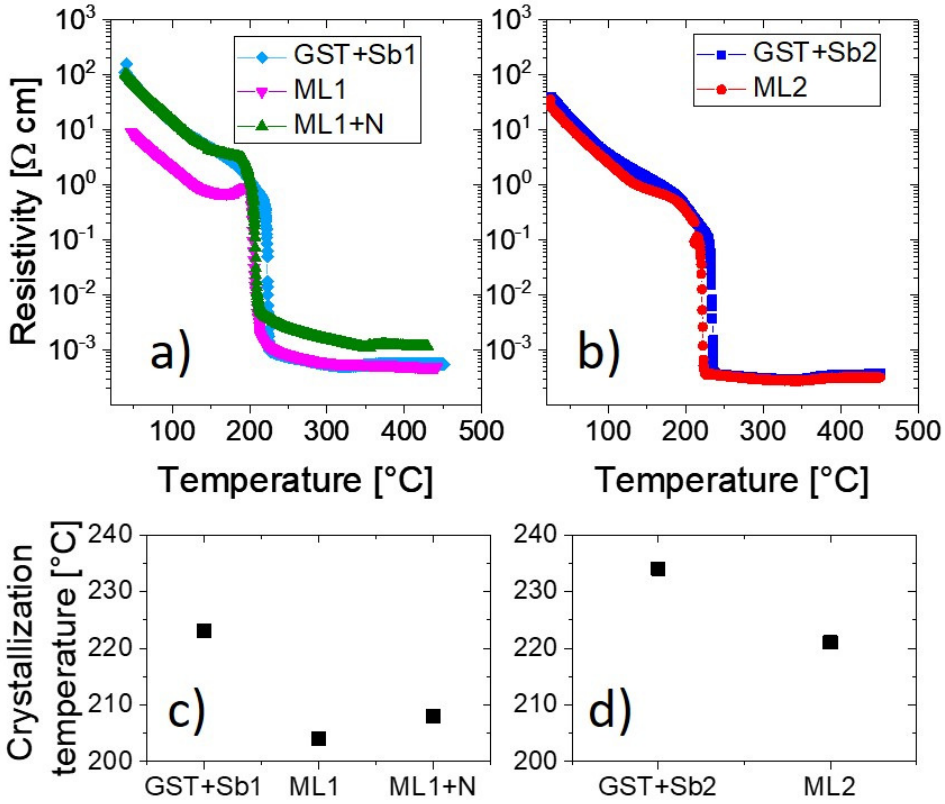

Fig. 4.2. Resistivity of as-deposited materials analyzed as a function of the temperature, measured during a ramp up of 10 °C/min (a-b) and their crystallization temperature (c-d).

cubic phase requires a large amount of vacancies, that in Sb-rich samples are filled by Sb, inhibiting the formation of the cubic phase and leading to a crystallization possible only towards an hexagonal phase [185].

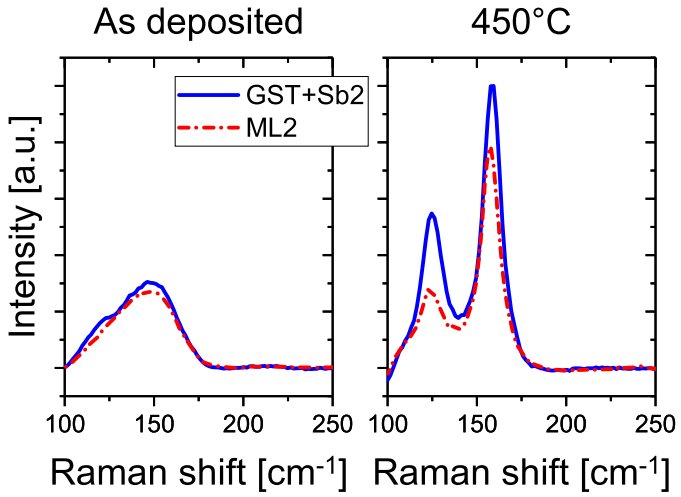

Fig. 4.3. Raman spectra obtained for GST+Sb2 and ML2 as-deposited (amorphous) and after annealing at 450 °C (crystalline).

Raman spectroscopy

The high similarity between bulk and multilayered stacks is evidenced also by Raman spectra of amorphous and crystallized samples reported in Fig. 4.3 for GST+Sb2 and ML2. The sharp peaks of both samples annealed at 450 °C indicate a high crystalline degree in both samples. The peak positions have analogies with the ones found for other GST phases (e.g. $Ge_2Sb_2Te_5$ [186]). The peak at 125 cm^{-1} can be associated to $GeTe_{4-n}Ge_n$(n=1,2) tetrahedral groups, the most intense peak at 158 cm^{-1} can be attributed to the vibration modes of SbTe based groups and to Sb-Sb bonds [186]. The low intensity of the first peak compared to the second is linked to the low presence of Ge atoms in the Sb-rich GST crystallized phase. Slight differences in stoichiometry and Ge incorporation in the obtained crystalline phases after annealing, could be taken into account to explain the difference in the ratio between the two peaks intensities (i.e. different ratio between the two types of bonds).
In summary, from R-T and Raman analyses we can observe the strong similarity of the crystallization dynamics between bulk and multilayered equivalent systems.

4.1.2 Electrical Characterization

The developed bulk and multilayers have been integrated in "wall" PCM devices with a heater thickness of 10 nm and a width going from 40 nm up to 100 nm, into the BEOL of LETI MAD based on 130 nm CMOS technology. Electrical measurements were performed on 4kb arrays for statistical analysis.

Programming characteristics

RESET current was measured pre-programming the devices in the SET state and applying a sequence of pulses with incremental voltage (i.e. AC based protocol). Fig. 4.4 reports the resistance as a function of the current measured during the pulses applica-

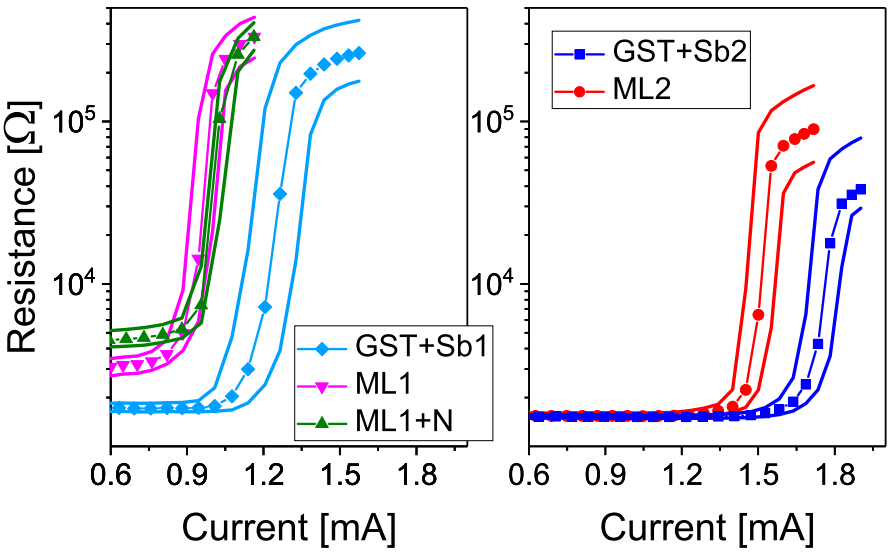

Fig. 4.4. Resistance as a function of current in 4kb arrays of PCM devices with a heater width of 100 nm. Median and corresponding 1σ standard deviation for the 4kb devices are represented.

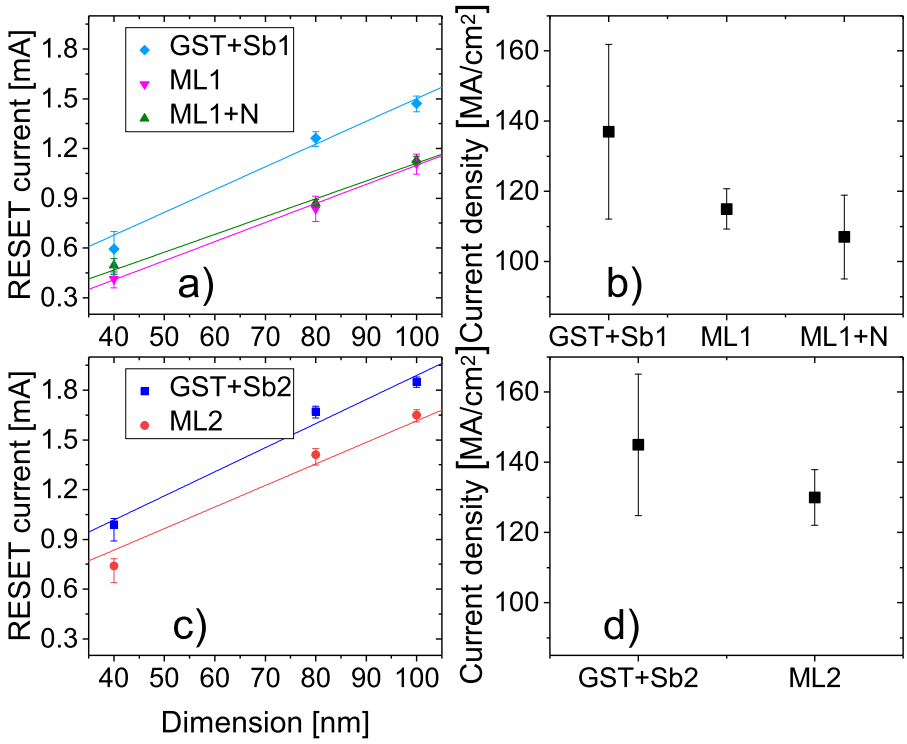

Fig. 4.5. RESET current measured in 4kb arrays for different heater dimensions. Median values and standard deviation are represented (a,c). RESET current density was extracted from the interpolation of the data in a and c for each composition (b,d). The current density variability is due to the fitting error on the slope calculation from the graph (a,c).

tion in 4kb arrays. We observe a general reduction of the RESET current in multilayer devices compared to the corresponding bulk devices. Considering the devices with low Sb content we observe a low RESET (at high current) resistance variability for both ML1 and ML1+N. The SET variability is extremely low for both high Sb content stacks (GST+Sb2 and ML2), however ML2 presents the highest RESET resistance value and then the highest resistance window with respect to the equivalent bulk GST+Sb2. RESET current was measured for three different heater sizes in 4kb arrays (Fig. 4.5a,c) in order to extract the RESET current density (J_R) for each composition (Fig. 4.5b,d). Multilayer devices present a lower J_R compared to the corresponding bulk ones, statistically confirming a lower power consumption of multilayer Sb-rich GST PCMs. Furthermore, the multilayer deposition suppresses the random growth of crystalline grains typical of bulk materials, as shown by the lower current density variability of multilayer PCMs in Fig. 4.5b,d. This is particularly evident in devices featuring small dimensions.

Programming speed analysis

The SET speed was evaluated pre-programming the 4kb arrays in the RESET state and applying SET pulses with variable duration from 30 ns up to 300 ns (Fig. 4.6). All the compositions can be programmed in the SET state with a pulse of 300 ns. The highest speed is observed in compositions with the highest Sb content, GST+Sb2 and

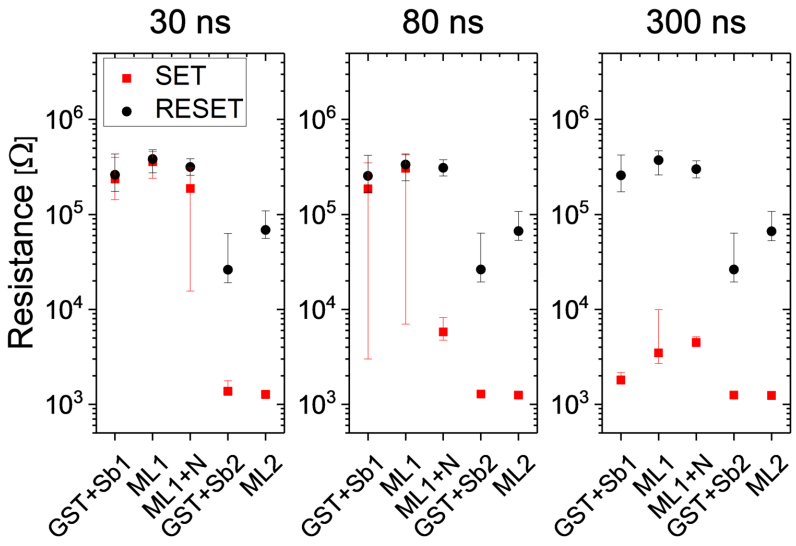

Fig. 4.6. Resistance achieved with a SET pulse of 30, 80 and 300 ns (respectively from left to right) for each stack analyzed. The starting RESET state resistance is reported as well for each test.

ML2, that are capable to crystallize in 30 ns. This is line with the growth-dominated crystallization mechanism in Sb-rich alloys that feature a high growth rate with a one-step phase-change transition from amorphous to hexagonal phase as observed in R-T measurements (Fig. 4.2). ML1+N is the only composition with low Sb content capable of SET programming in 80 ns. Indeed, Ge tends to bond with N [187] and GeN features could enhance the Sb enrichment in the active region, leading to a material with a faster growth rate. In the following, the analyses will focus on such PCMs featuring high programming speed, nominally ML1+N, GST+Sb2 and ML2.

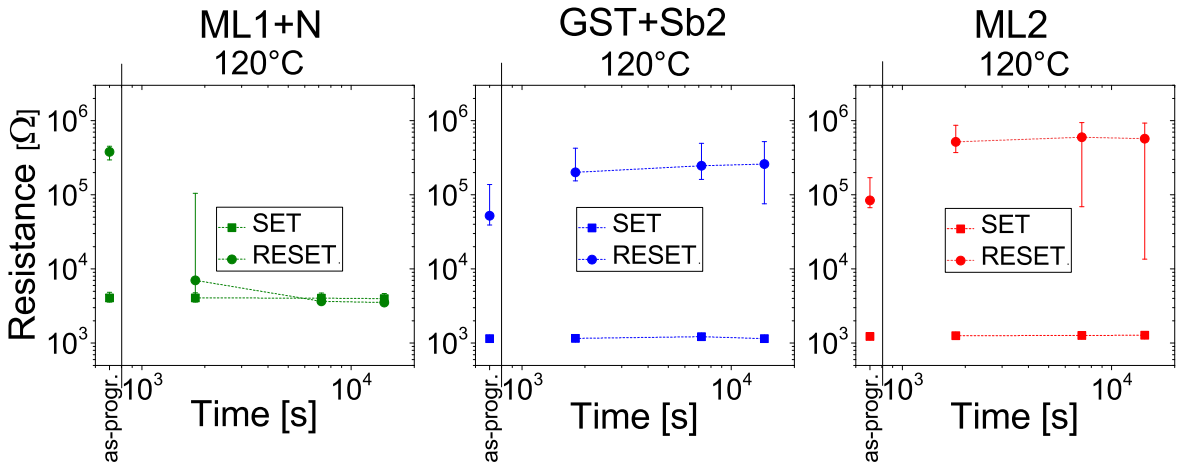

Fig. 4.7. Data retention evaluated at 120 °C for the SET and the RESET states for ML1+N, GST+Sb2 and ML2 in 4kb arrays. We report the starting SET and RESET distributions (as.-progr.) and after different annealing times up to 4 hours.

Data retention

The data retention at 120 °C of SET and RESET states was investigated in ML1+N, GST+Sb2 and ML2 (Fig. 4.7). Amorphous ML1+N crystallizes already after 30 min at 120 °C. On the contrary, in GST+Sb2 and ML2 the RESET resistance exhibits only a drift towards higher resistance values after 30 minutes annealing. After 4 hours annealing we start to observe an initiation of the crystallization of some devices in both materials. The SET state is extremely stable without exhibiting any resistance drift or variability increasing in each composition analyzed. The improved retention observed in high Sb content layers, is likely related to the low nucleation rate featured by this materials at low temperatures [180].

Endurance analysis

The RESET current has been measured along cycling until 10^5 cycles realized with pulses with a duration of 10 µs for SET and RESET operations (i.e. long pulses are used to accelerate material degradation phenomena) and the results are reported in Fig. 4.8. The RESET current measured in Fig. 4.4, reduced in ML2 with respect to GST+Sb2, appears stable along cycling in both materials. Indeed, in TEM/EDX analyses performed on ML2 devices we demonstrate that the elemental distribution remains uniform in the active region of the cell even after cycling (Fig. 4.9), without elemental or phase segregation appearing, similarly to what observed already for bulk highly Sb-rich GST [180].

Contrarily to ML2 and GST+Sb2, ML1+N shows a degradation of the programming characteristics (i.e. increasing RESET current) and a reduction of RESET resistance already after 10^2 cycles (Fig. 4.8b). In order to explore the origin of the different endurance performance, we measured the threshold voltage for ML1+N (V_{th}) and we compared it to the one of GST+Sb2 and ML2 (Fig. 4.10). V_{th} is the voltage necessary to achieve the switching event in the amorphous phase of the material [101]. We observe an increased V_{th} (of almost 100%) in ML1+N with respect to high Sb content compositions. The higher V_{th} in ML1+N is in line with the higher resistivity of the

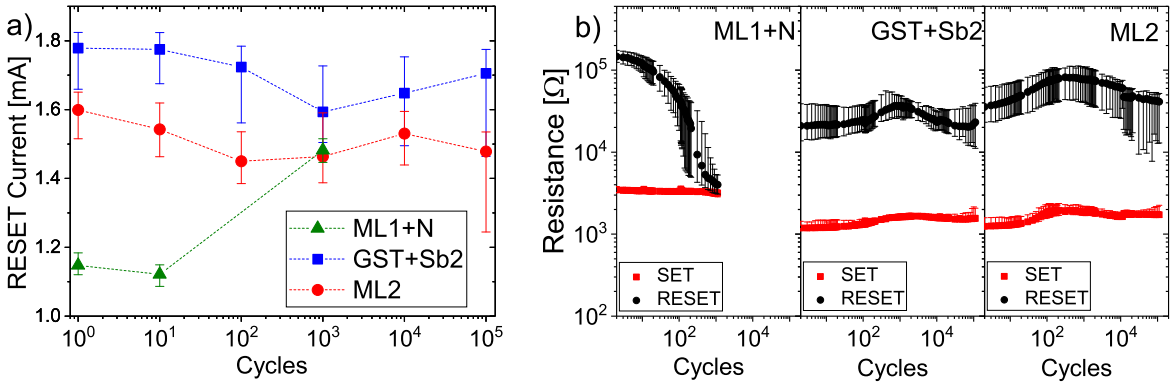

Fig. 4.8. a) RESET current evolution along endurance. Pulses of 10 µs width time were used to accelerate the degradation phenomena during cycling. b) SET and RESET resistance as a function of cycles number. For both graphs, median values and the standard deviation for populations of 100 devices are represented.

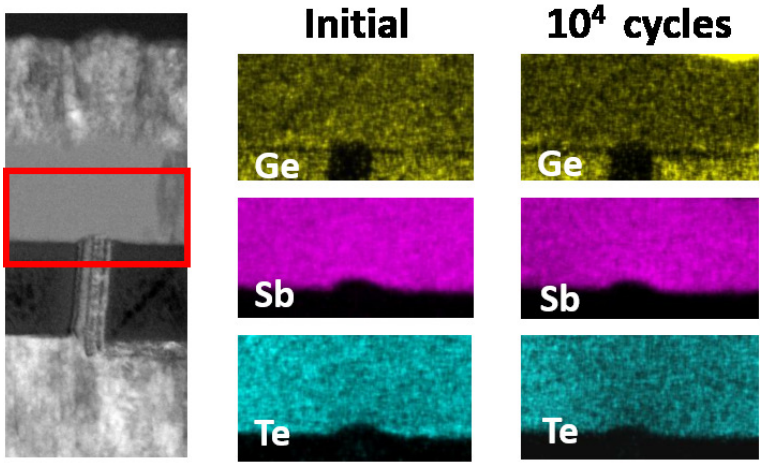

Fig. 4.9. TEM/EDX analyses performed on the active region of a ML2 PCM device before and after 10^4 cycles.

RESET state observed in Fig. 4.6, being V_{th} proportional to the mobility gap [96]. A higher threshold voltage is responsible for a higher stress in the device during the switching event, leading to a likely accelerated degradation of the material properties (i.e. elemental or/and phase segregation) [188].

The endurance has been further studied in GST+Sb2 and ML2, that demonstrated from previous tests the best performances. SET/RESET cycling was executed applying pulses with a duration of 200 µs and overloading the RESET current measured in Fig. 4.4 and Fig. 4.5 in order to evaluate the sensitivity of the devices to the programming current variations. The results are reported in Fig. 4.11. ML2 can be programmed with a higher current overload (more than 20%) than GST+Sb2 without affecting the maximum endurance.

C2C and D2D variability were statistically analyzed in 4kb arrays before and after endurance tests (Fig. 4.12). The SET variability is extremely low in both materials, as expected from the high crystal growth speed and the high crystalline homogeneity in Sb-rich alloys. The RESET state of GST+Sb2 presents a large tail towards low

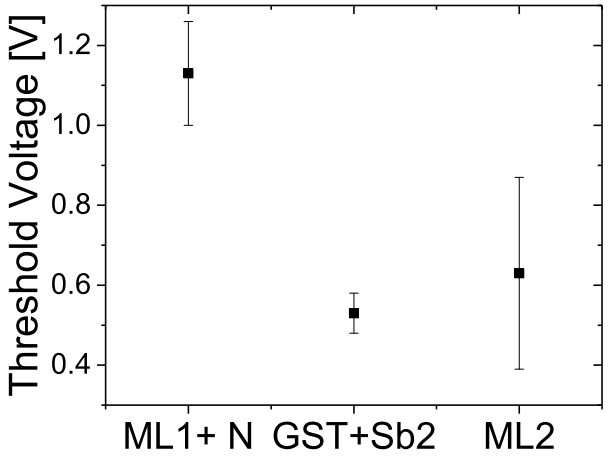

Fig. 4.10. Threshold voltage measured in 4kb arrays for ML1+N, GST+Sb2 and ML2.

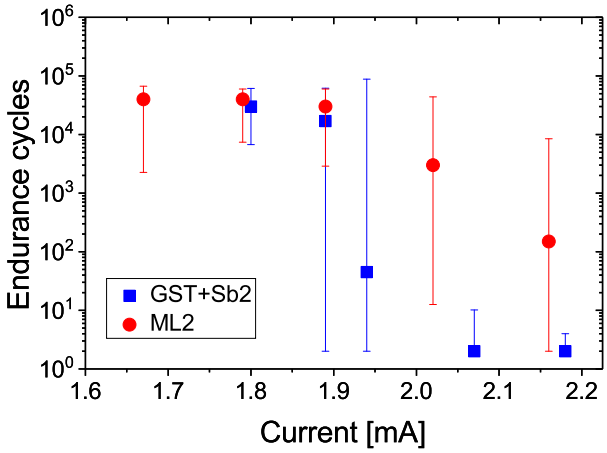

Fig. 4.11. Number of endurance cycles achieved applying RESET pulses with different current in GST+Sb2 and ML2 4kb arrays. The endurance test has been executed with pulses with a duration of 200 µsto increase the stress during programming and to speed up the test sequence. We report the median values and one standard deviation.

resistance values with a high C2C variability (Fig. 4.12a). Such tail is present since the beginning of the life of the devices, and their resistance becomes more and more variable along cycling (Fig. 4.12b). On the contrary, ML2 features a very high stability of the RESET resistance values, with a low C2C and D2D variability before and after accelerated endurance test. This demonstrates the interest of multilayer in providing at the out of the fabrication an important reduction of the D2D electrical parameters variability.

4.1.3 Discussions

Multilayer deposition in Sb-rich GST alloys shows its advantage in an improved layer quality demonstrated first of all by a reduction of the device-to-device variability since the out-of-fabrication (Fig. 4.12). This is achieved despite the intermixing of the Sb and GST layers composing the multilayer stacks happening already at temperatures close to 200 °C (Fig. 4.2), and likely to happen during the BEOL of the fabrication at even higher thermal budget (i.e. several hours at 400 °C). Indeed, the intermixing is not itself a problem, on the contrary it is favoring the crystallization of the layer (and even orienting it), as demonstrated by the reduced crystallization temperature observed in multilayers with respect to equivalent bulk layers in R-T measurements. We think that the reduction of the stochasticity of the crystalline grains size and orientation is the key for a reduced variability in the final devices, still preserving the advantageous properties of the target stoichiometry. High SET speed in tens of ns range (Fig. 4.6), data retention (Fig. 4.7), and endurance performances (Fig. 4.8) show the good alignment between multilayer ML2 and bulk equivalent GST+Sb2, thanks to the matched composition obtained in the active volume of the device. Even the high compositional stability after cycling, previously observed in Sb-rich GST, is confirmed for multilayer (i.e. ML2 in Fig. 4.9). We think that this is directly linked to a reduced impact of the switching operation in high Sb content materials thanks to the reduced switching voltage V_{th} (Fig. 4.10).

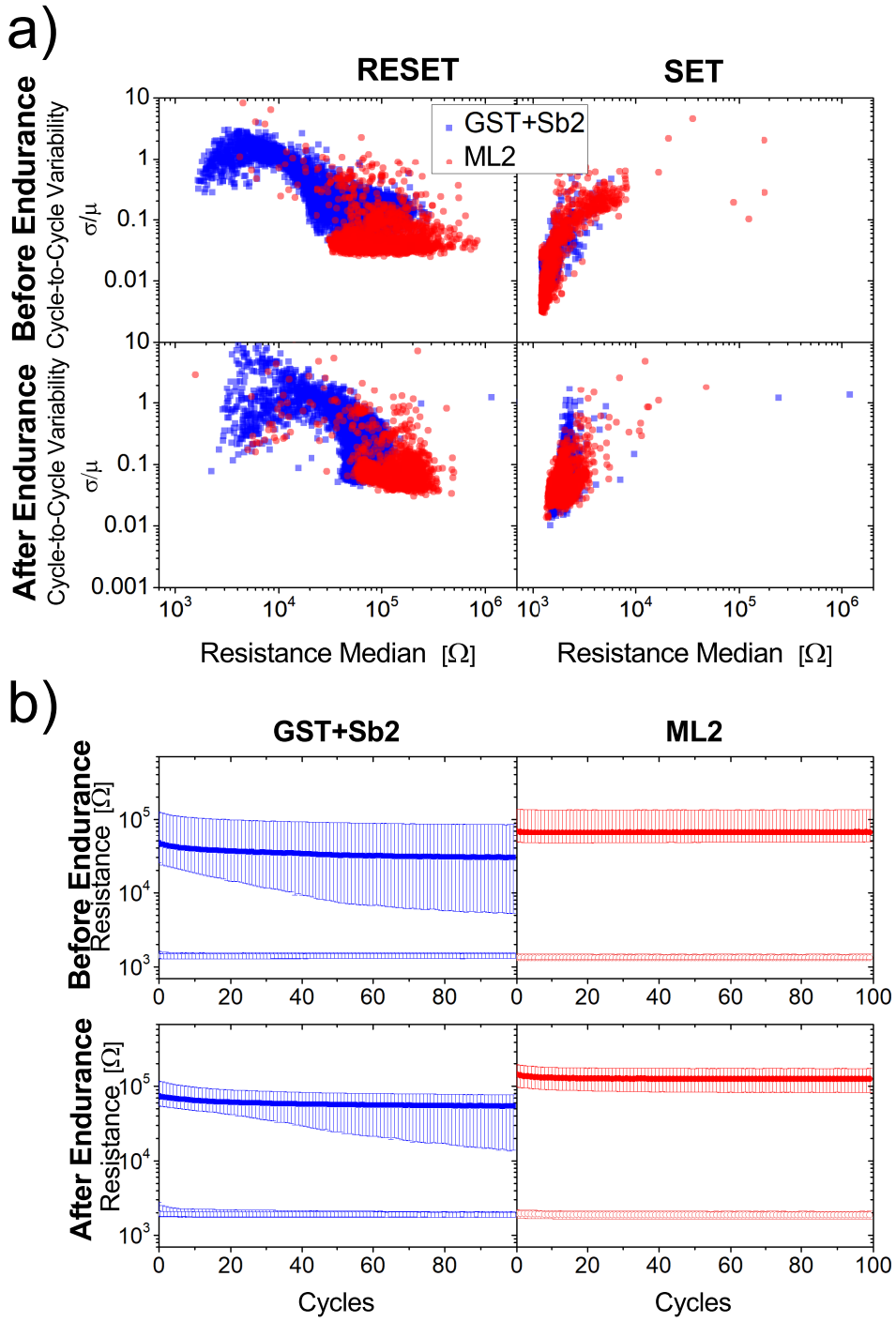

Fig. 4.12. Variability of the SET and RESET states evaluated along 100 programming cycles (SET/RESET pulses of 50 ns) in 4kb arrays, before and after a sequence of 10^3 cycles (performed with 10 µs SET/RESET pulses for an accelerated aging of the devices). a) cycle-to-cycle: each point in the graphs represents the variance of the resistance value (for both RESET and SET state) of a single device normalized with respect to its median resistance along 100 cycles. b) device-to-device: median and standard deviation for the 4kb devices resistance values along the 100 cycles.

While the optimal speed and endurance performances of Sb-rich GST alloys are preserved in multilayer stacks, in these latter we observed in general a reduction of the RESET programming current statistically demonstrated in 4kb arrays (Fig. 4.4 and Fig. 4.5). This reduction is confirmed even after array cycling (Fig. 4.8). It could be likely related to the higher in-plane thermal conductivity expected in multilayers due to a more uniform and oriented crystalline morphology. Such property is beneficial for the reaching of a uniform temperature distribution over the heater, reducing the programming current needed to achieve the complete amorphization of the phase-change material [189]. In addition, multilayer Sb-rich GST revealed a lower sensitivity to current overload (Fig. 4.11), and it could be as well due to the enhanced thermal conductivity of the layer, better dissipating the overheating that such overload could generate. This is fundamental to reduce the sensitivity of the PCM devices to variations of the controlled programming current caused by parameters related to the design/layout of the array.

Finally, Sb-rich GST multilayers enable a high reduction of the device-to-device variability that is intrinsic of the uncontrolled crystallization of bulk PCM layers happening during the fabrication process. This result enables high yield in high density memory arrays and nm scaled devices, targeting SCM applications and next generation of PCM for DRAM replacement.

4.2 Sb-rich confined PCM

In addition to the "wall" structure, we characterized also the confined PCM cell, where the phase-change material is deposited on the sidewall of the structure connecting the bottom and the top electrode, which is essentially a structure without the heater element (Fig. 4.13a).

The interest for Sb-rich GST confined PCMs was given by previous works showing that, in these devices, fast SET operation of 30 ns, low RESET programming current of 80 μA, good scalability sub-20 nm [111] and the highest endurance of 2×10^{12} were achieved [110].

First, confined PCMs based on $Ge_2Sb_2Te_5$ were tested. After fabrication, the devices are in the crystalline phase with a resistance lower than 10^4 (Fig. 4.13b). Applying a staircase up sequence, the material switches to the amorphous phase, but the $Ge_2Sb_2Te_5$ devices were not able to reach again the SET state. On the contrary, devices based on GST+Sb show functionality achieving easily the SET state, as represented in Fig. 4.13 (c) and (d). In fact, in a confined cell the SET operation is more difficult compared to a "wall" PCM since all the phase-change volume is amorphized after the RESET operation and does not contain any crystalline seeds which would facilitate and speed up the SET operation. The high crystallization rate typical of Sb-rich GST allows to easily obtain the transition to the SET state, proving to be suitable for confined architecture compared to $Ge_2Sb_2Te_5$.

The hysteresis among the obtained R-I curves, in particular on GST+Sb1 device, is probably due to the absence of a selector to better control the programming current. Indeed, the confined structure is quite delicate since the high current density in the small phase-change material volume can induce atomic migration [190].

In the confined architecture, a remarkable RESET current reduction was obtained

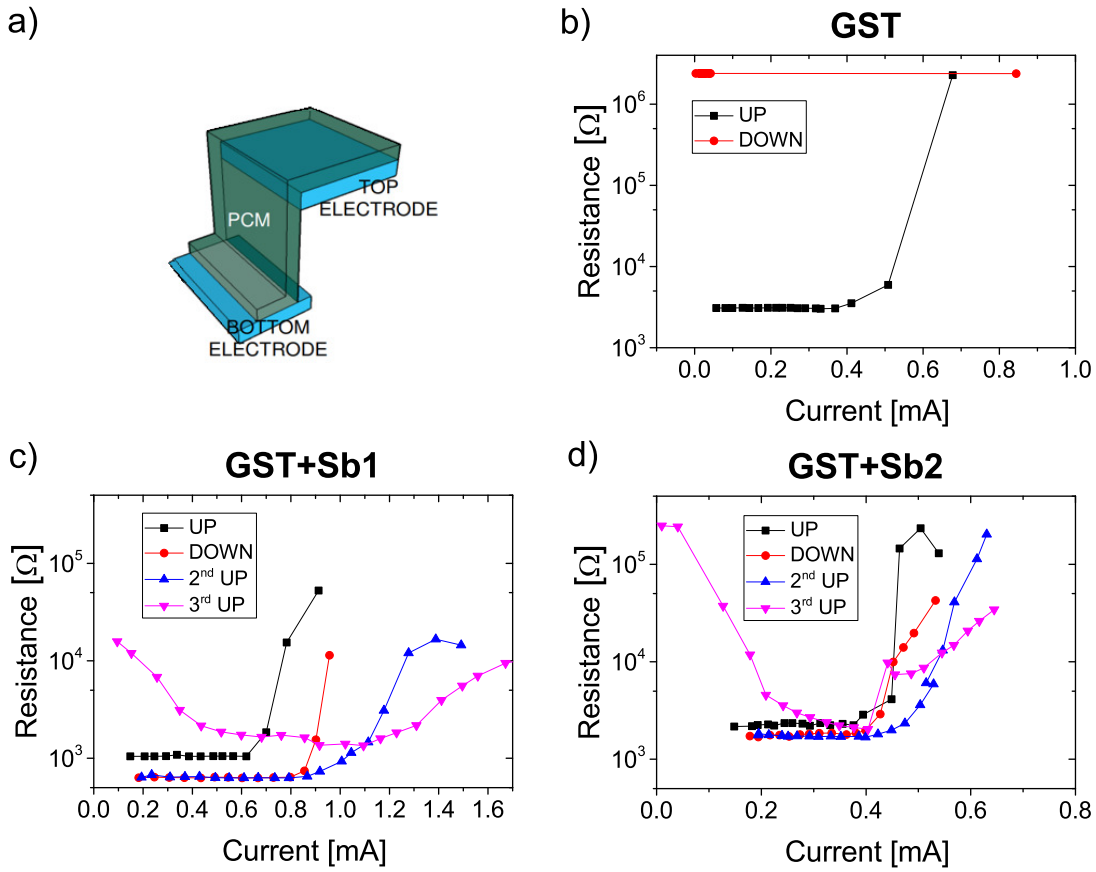

Fig. 4.13. a)Schematic of the confined architecture used in this work. R-I characteristics of $Ge_2Sb_2Te_5$ (b), GST+Sb1 (c), GST+Sb2 (d) confined PCM devices.

compared to a standard "wall" PCM: in particular, in GST+Sb2 device we achieved about 4 times of current reduction.
We did not go more in depth in the analysis of confined Sb-rich GST PCMs, since we had only available single 1R devices and the current must be well controlled and limited through a selector to not lead early atomic migration. However, our analysis confirmed that Sb-rich is more adapted to be integrated in a confined architecture than a standard $Ge_2Sb_2Te_5$, and since the confined cell is 3D compatible would be interesting to investigate 3D confined Sb-rich PCMs.

4.3 Summary of the chapter

Sb-rich GeSbTe based PCMs were studied in the last years for their high switching speed to target SCM applications. In this chapter, we show the advantages of an engineered multilayered Sb-rich GeSbTe stack compared to standard bulk reference materials. The studied multilayer-based PCM devices feature a lower programming current with respect to the equivalent bulk ones even after array cycling, preserving a high programming speed. Furthermore, multilayered Sb-rich GeSbTe brings better endurance performances for a wide programming current range and extremely reduced C2C and D2D variability along cycling verified in 4kb PCM arrays. Despite the layers

intermixing after the BEOL thermal budget, we believe that the multilayer fabrication is responsible of a reduction of the stochasticity of the crystalline grains size and orientation leading a variability reduction. Furthermore, multilayer Sb-rich GST showed a decreased sensitivity to current overload, that is essential in order to mitigate the variations in the controlled programming current brought by the fabrication process. These results confirm the improved yield and reliability obtained thanks to multilayered PCM solution.
Moreover, Sb-rich GST results particularly suitable for the confined architecture, since its high crystallization rate allows to easily switch to the SET state, although the phase change volume is completely amorphous and no crystalline seeds are present. The interest towards confined structure is due to its 3D architectures compatibility and the low power consumption compared to “wall” PCM.

Chapter 5

Innovative phase-change materials

In this chapter, we investigate innovative PCM based on TiTe/GST bi-layer stack and GaSb devices.
Sb-rich GST, analyzed in the previous chapter, has been recognized as a suitable phase-change material for SCM thanks to its ns range programming time and a record endurance of 2×10^{12} [110]. However, these materials present a really steep SET-to-RESET characteristic, which prevents the possibility of achieving intermediate states with low variability i.e. MLC. For this reason, it would be interesting to explore other PCM materials that ensure high speed and MLC capability at the same time.
TiTe and $Ge_2Sb_2Te_5$ bi-layer (TiTe/GST) stack, analyzed in the next section, shows low D2D already at the out-of-fabrication thanks to a TiTe layer that features low resistivity and high stability in temperature. An initialization step drives a reliable intermixing of TiTe and GST. We explore the SET speed, the MLC capability, drift in temperature and in time as well as C2C variability in 4kb arrays, making a comparison with standard GST based PCM. Finally, we analyze the behavior of TiTe/GST devices before and after endurance stress highlighting an extremely low variability of the resistance states even after cycling and we present an application that exploits TiTe/GST properties.
Then, we analyze GaSb based PCMs, showing that off-stoichiometric GaSb tends to segregate into GaSb and Sb. However, C doping helps reduce segregation, improve yield and reduce D2D variability.

5.1 TiTe/GST Bi-Layer

$TiTe/Sb_2Te_3$ stack has been presented as a PCM material with reduced compositional and structural variability with also good speed and cyclability [191], however it requires a huge stability of the multilayer structure that could result difficult along cycling.
In order to ensure stability against BEOL fabrication process thermal budget, we engineered the thin TiTe layer integrated in our PCM devices. For this purpose, we deposited three TiTe layers with different percentages of Ti ranging from ∼10 at.% to ∼50 at.% (addressed as Ti x, y, z% with x<y<z) and we measured at room temperature the resistivity of TiTe layers before and after annealing at 450 °C by four-probe method (Fig. 5.1). The resistivity of TiTe layer decreases as the Ti content increases due to its metallic nature. The layer with Ti z% maintains a resistivity similar to the initial one after being annealed, showing a higher stability compared to the layers with less Ti content. For this reason, we selected Ti_zTe_{100-z} as thin layer to be co-integrated with a GST layer in "wall" PCM devices, as described in the inset of Fig. 5.2 (this PCM will be addressed as TiTe/GST in the following). We performed electrical characterization on 4kb arrays consisting of PCM devices with a heater width of 100 nm integrated into the BEOL of LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology.

5.1.1 TiTe/GST Programming Characteristics

Resistance of as-fabricated devices is reported in Fig. 5.1 showing an extremely low dispersion in TiTe/GST with respect to GST. Such low resistance variability is ensured by the low resistive Ti_zTe_{100-z} layer, which offers a good temperature stability against fabrication process thermal budget. This is confirmed by TEM/EDX analyses of Fig. 5.3 illustrating that the TiTe layer remains intact after the fabrication, while in a programmed TiTe/GST the TiTe layer is no longer visible in the active region due to the intermixing of TiTe with GST.
The R-I curve in Fig. 5.4a evidences that as-fabricated TiTe/GST devices need an ini-

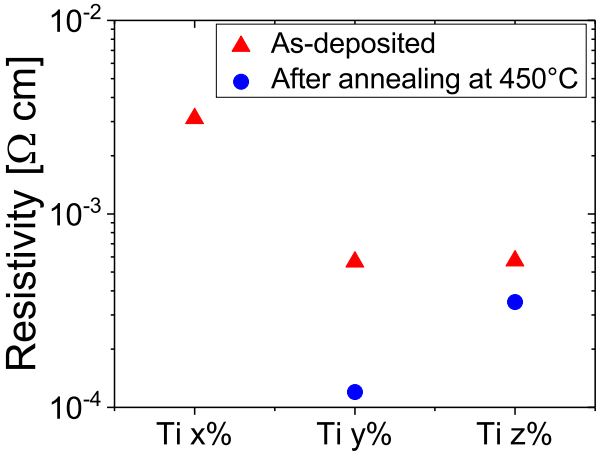

Fig. 5.1. Resistivity of TiTe samples with three different percentages of Ti (x, y and z with x<y<z) measured at room temperature before and after annealing at 450 °C. The resistivity after annealing of the layer with Ti x % is not reported since the layer resulted degraded after the test.

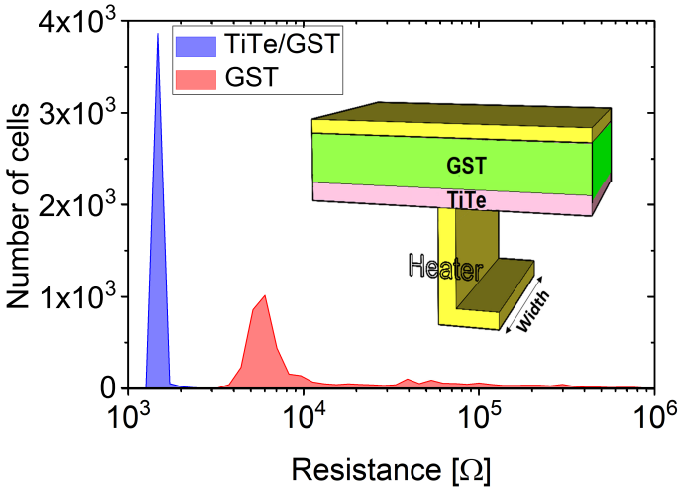

Fig. 5.2. As-fabricated resistance distributions of TiTe/GST and GST 4kb arrays. Inset: simplified scheme of the studied "Wall" PCM device based on TiTe/GST bi-layer stack.

tialization step to give rise to the intermixing of TiTe with GST in the active region. Such initialization effect is also highlighted by current-voltage (I-V) measurements in Fig. 5.4b: as-fabricated TiTe/GST devices exhibit an ohmic behavior, while after the initialization and the first programming in the SET state, the I-V characteristic changes showing an exponential behavior. Resistance-Current (R-I) curve of TiTe/GST devices after initialization shows an extremely low variability and more gradual SET-to-RESET transition with respect to GST, despite a reduced resistance window.

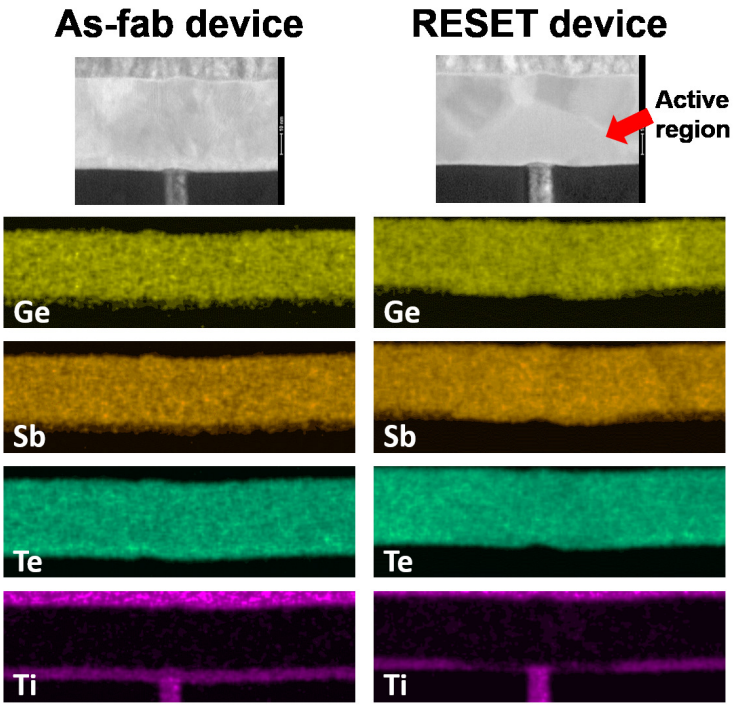

Fig. 5.3. TEM/EDX analyses performed on as-fabricated TiTe/GST device (left column) and on a device programmed in the RESET state after initialization (right column).

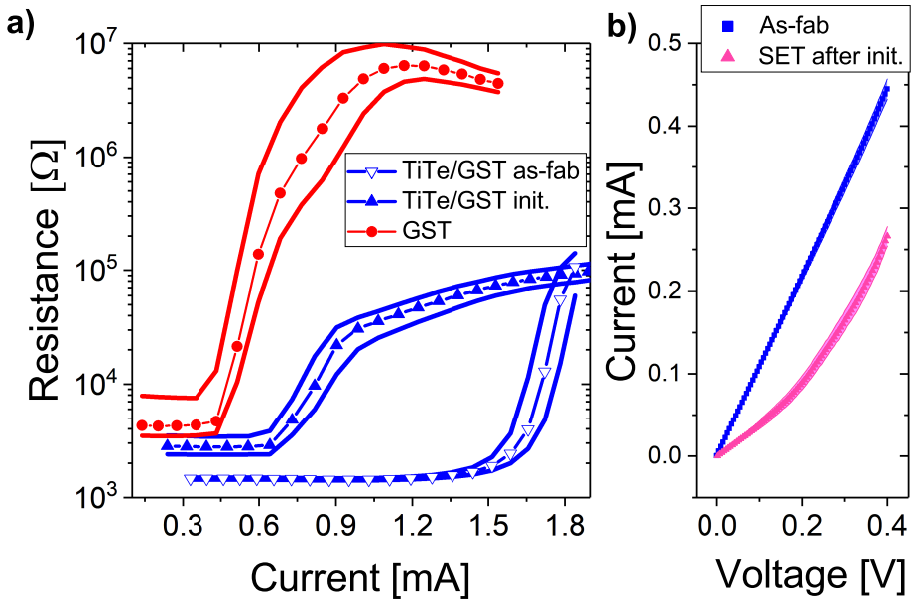

Fig. 5.4. a) Resistance as a function of current measured in 4kb array for GST and TiTe/GST devices starting in the SET state. We represent median values and 1σ intervals, and in particular before (as-fab) and after initialization (init.) for TiTe/GST. b) Current-Voltage (I-V) characteristics of five TiTe/GST PCM devices as-fabricated (as-fab) and after initialization in the SET state (SET after-init.).

The SET speed is evaluated in (Fig. 5.5) indicating that GST needs pulses longer than 1 µs to obtain a reliable SET state, whereas in TiTe/GST the SET operation is achievable using pulses with a short fall time lower than 10 ns.
MLC capability is analyzed in Fig. 5.6a, which reports the resistances obtained applying pulses of increasing intensity in arrays programmed in the SET state before each

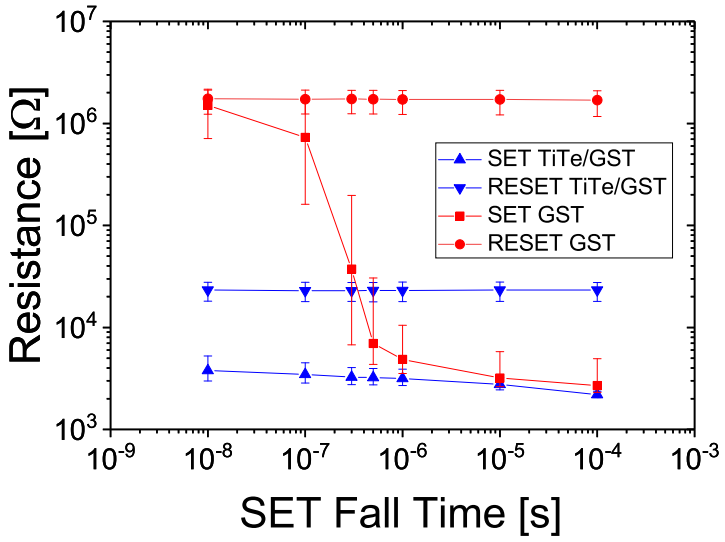

Fig. 5.5. SET speed test performed on TiTe/GST and GST 4kb arrays. Data are obtained applying a SET pulse with optimized current, 300 ns width time and incremental fall time on arrays pre-programmed in RESET state before each SET pulse. RESET state resistance is reported as well.

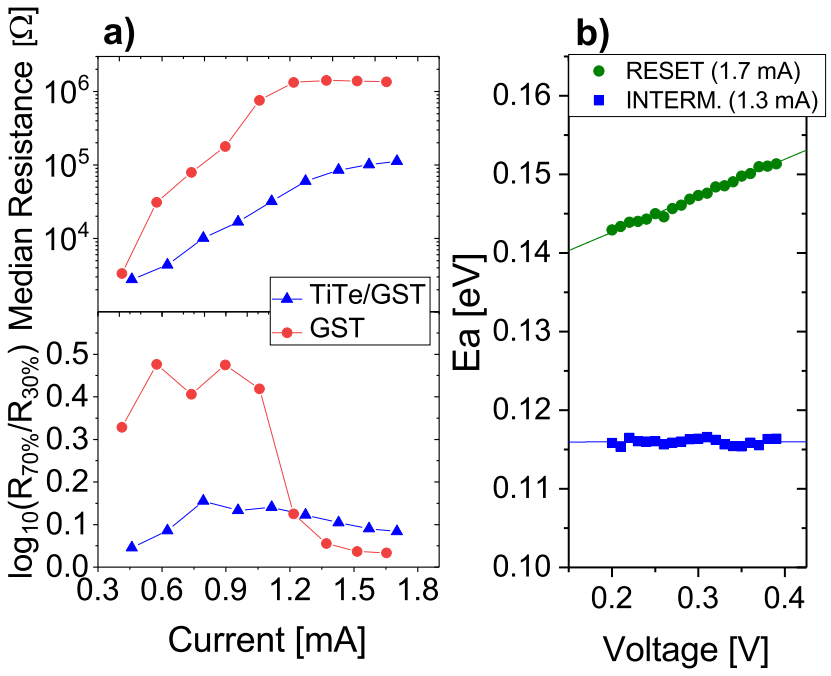

Fig. 5.6. a) Intermediate states obtained in GST and TiTe/GST applying 300 ns squared pulses with increasing current intensity pre-programming the array in the SET state before each pulse. Median (above) and variability (below) of the resistances in 4kb arrays are represented. The variability was calculated as the ratio between the 70th and the 30th percentile of the 4kb resistances. b) Activation energy of the conduction measured from I-V characteristics of TiTe/GST (not reported), for RESET state and an intermediate state, following the model from [92].

pulse. GST shows a higher variability, except for the RESET state. On the contrary, a low variability of all the programmed states is confirmed in TiTe/GST. The activation energy of conduction (E_a) of the RESET state and of an intermediate state in TiTe/GST is measured from subthreshold I-V realized at different temperatures (Fig. 5.6b) according to [92]. In common phase-change materials, such as GST, the amorphous phase shows a trap-limited transport described by Poole-Frenkel mechanism, where E_a decreases with increasing voltage [92]. In the case of TiTe/GST, E_a is not dependent on the voltage for the intermediate state and it increases with voltage for the RESET state. Moreover, TiTe/GST presents a low E_a ($\sim$ 0.1 eV i.e. small energy gap) compared to GST (0.37 eV) [92]. These results evidence a different conduction mechanism in RESET TiTe/GST that appears more close to a metallic behavior, with the presence of defects that generates scattering, increasing E_a value as the electric field increases.

5.1.2 Data Retention

Data retention in our PCM devices was investigated comparing the resistance states values before and after an annealing at 100 °C for 3 hours. The resistance drift is quantified for each device of the array in Fig. 5.7. SET state drifts more in TiTe/GST than in GST devices, likely due to the presence of defects in the crystalline matrix of the material related to Ti inclusion. GST intermediate state shows a large spread in the behavior of the devices after annealing, that is suppressed in TiTe/GST. The

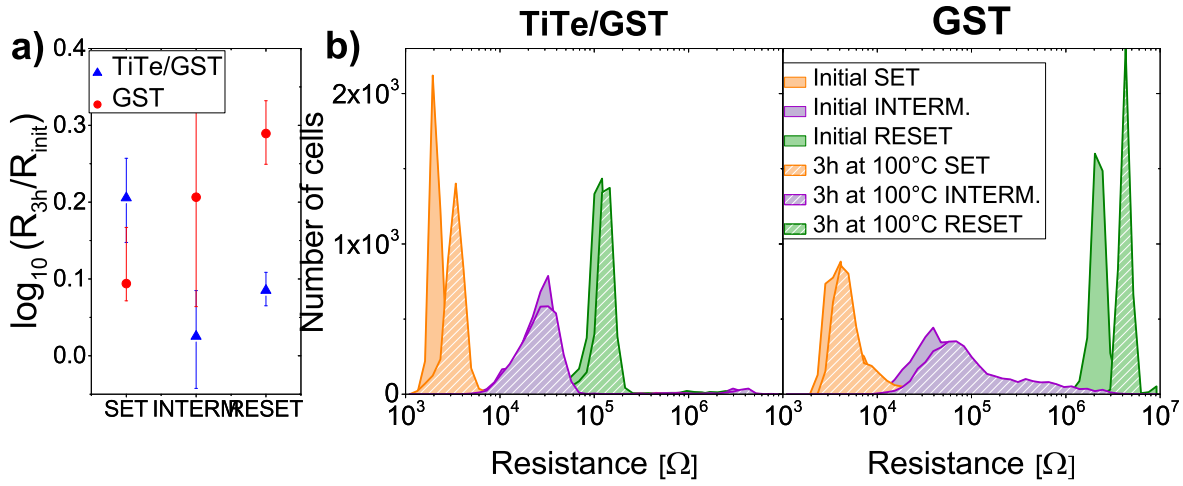

Fig. 5.7. Data retention evaluated after annealing at 100 °C for the SET, intermediate and RESET states in TiTe/GST and GST 4kb arrays. a) The resistance drift is quantified as the ratio between the resistance measured after a 3 hours annealing and the initial resistance. Median values and variability are represented. b) Resistance distributions of the three states before and after 3 hours annealing at 100 °C.

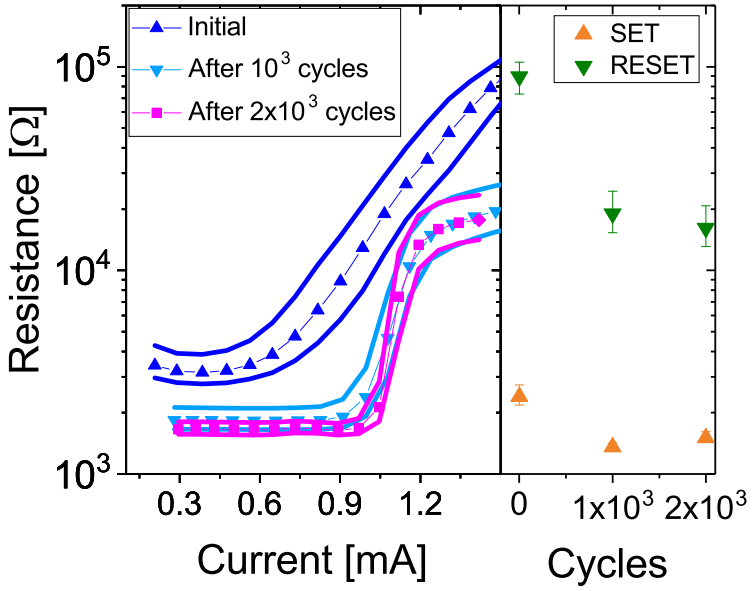

Fig. 5.8. Left: R-I characteristic at the beginning of the devices life and after endurance for TiTe/GST. Right: 4kb TiTe/GST SET and RESET resistances evolution along cycles performed with pulses of 10 µs to accelerate and evidence the evolution.

RESET state is also more stable in TiTe/GST with respect to GST. We think that the (almost) metallic behavior of amorphous TiTe/GST observed in previous E_a analyses contributes to the improved stability in this material.

5.1.3 Endurance

In order to analyze the behavior of TiTe/GST during cycling, R-I curves and SET and RESET resistances before and after endurance stress are reported in Fig. 5.8. The

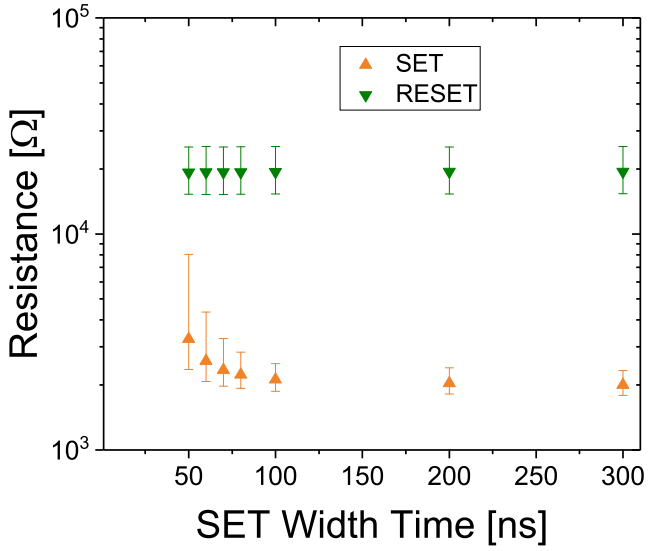

Fig. 5.9. SET speed test realized in TiTe/GST 4kb array after endurance test performed in Fig. 5.8b, using SET pulses with increasing width time and short constant fall time of 10 ns.

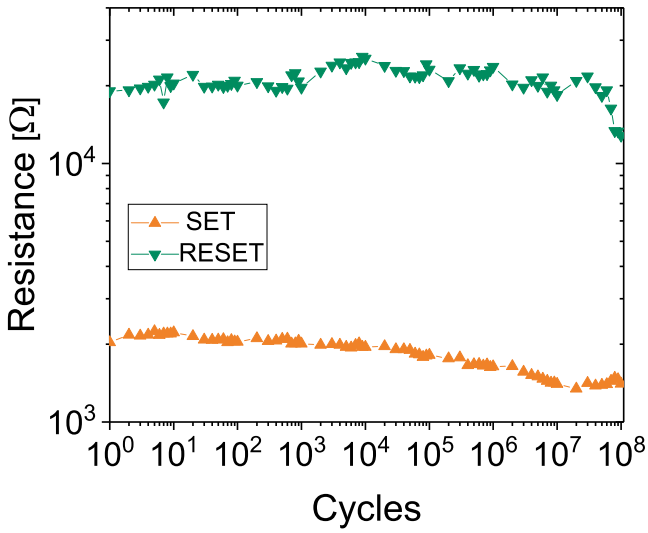

Fig. 5.10. Endurance evaluated in a TiTe/GST device with optimized SET and RESET pulses (width time = 50 ns, rise/fall time = 10 ns).

cycles were executed with long pulses of 10 µs for accelerated aging. After 10^3 cycles, the R-I curve evolves and SET and RESET resistances decrease. Additional 10^3 cycles, applied with the same protocol, highlight that this evolution is not detrimental and the devices achieve an extremely stable behavior. Indeed, we realized that the composition achieved in the active region of the PCM features unique stability properties. Fig. 5.9 shows the programming SET time kept in tens of ns range and an endurance higher than 10^8 cycles without the use of any smart programming protocol (Fig. 5.10). The devices were still perfectly functional after all the stresses applied. The C2C and D2D variability in TiTe/GST 4kb arrays along 100 cycles were evaluated for SET, intermediate and RESET state before and after the endurance stress (Fig. 5.11). The three

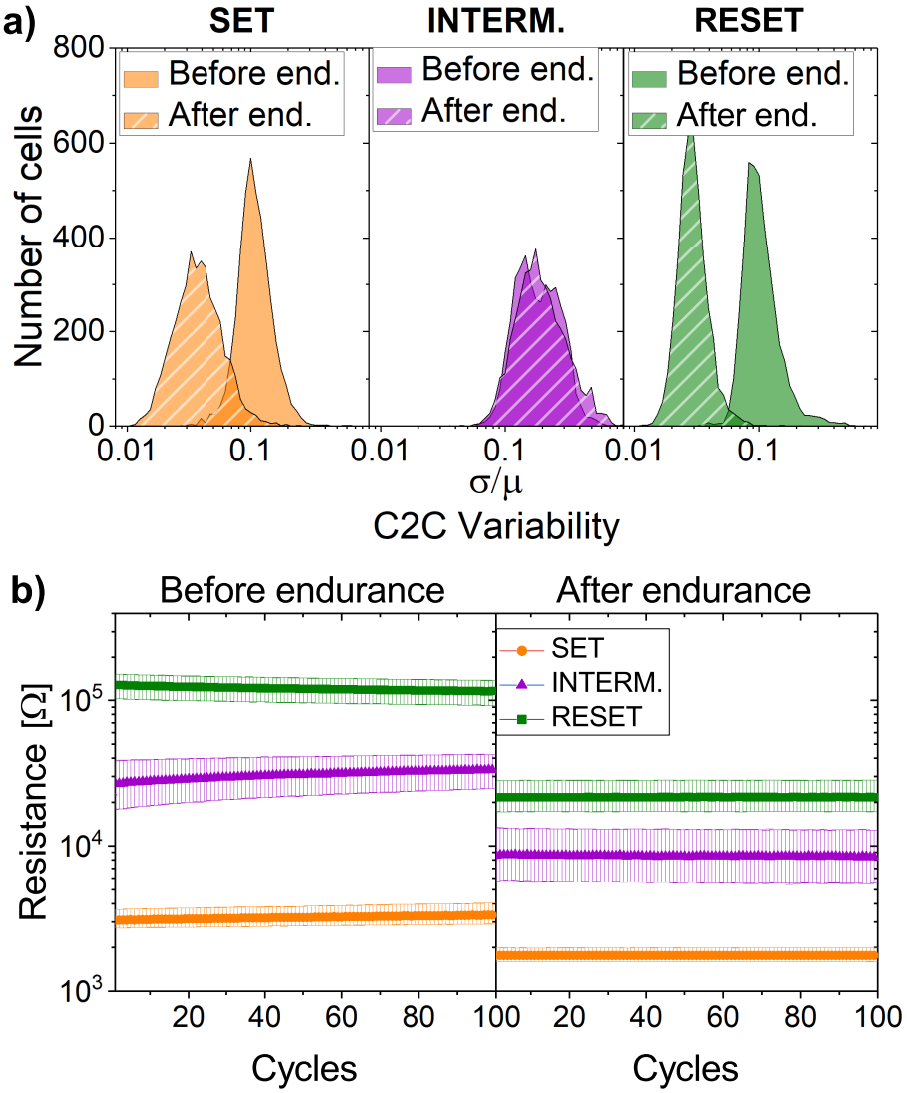

Fig. 5.11. Variability of SET, RESET and intermediate states evaluated along 100 programming cycles (SET/RESET pulses of 50 ns) in TiTe/GST 4kb arrays, before and after an endurance test compatible with the one performed in Fig. 5.8. a) C2C variability distributions: for each device in the array the C2C variability was calculated as the ratio between the standard deviation of the resistance value and its median resistance along 100 cycles. b) D2D variability: median and standard deviation for the 4kb resistance values along the 100 cycles.

states modify their resistance values after cycling, as shown in Fig. 5.11b, compatibly with previous results. Nevertheless, the three states are still perfectly achievable and distinguishable and the C2C variability of SET and RESET states is even reduced after cycling (Fig. 5.11a). Further analyses are ongoing to reveal the nature of this new composition featuring such striking stability and endurance performances.

5.1.4 Applications

In the previous sections, we have seen that TiTe/GST PCM needs an initialization step at higher current compared to its standard RESET current to intermix TiTe and GST. This feature can be used for encryption applications. After deposition, the TiTe/GST

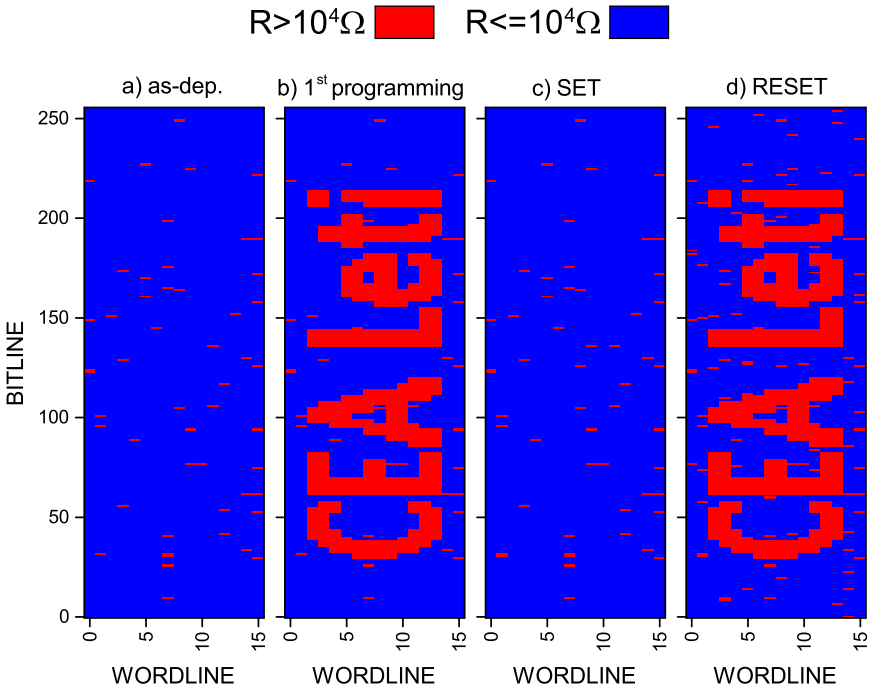

Fig. 5.12. Example of a 4kb array programming that can be exploited for encryption applications (in the array used, the few random high resistance cells are defective and not programmable).

array resistance is low due to the presence of the TiTe layer: we are going to call this state INIT(Fig. 5.12a). On the array, we can choose to initialize just a part of the array in the RESET state for the encryption operation (Fig. 5.12b). Applying a SET pulse on the whole array (Fig. 5.12c) and then a RESET pulse (Fig. 5.12d), just the devices previously initialized will switch into the RESET state, exploiting the fact that the initializing pulse amplitude is higher compared to the RESET pulse amplitude. We can apply an encryption rule programming the desired devices in the SET or the RESET state and, at the end, we are going to have an array consisting of three state: INIT, SET and RESET. In binary, the reading of the INIT and SET states are identical, they can be represented by "1", on the contrary, the RESET state is "0". Only the knowledge of the encryption rule can be used to trace the correct nature of the "1", that could be equal to INIT (non-useful bit) or SET (useful bit).
The benefit of this approach is its simplicity, since no extra circuitry is required and the initialization voltage is equivalent to that of a RESET operation.

5.2 GaSb based PCMs

GaSb is a phase-change material mainly used in optical devices and characterized by a high amorphous stability and by a rapid crystallization, linked to its growth-dominated crystallization [192]. Thanks to these features, it could be an interesting PCM material also for SCM applications. However, only few works concern the study of GaSb based PCMs. In $Ga_{14}Sb_{86}$ PCMs, SET and RESET operations have been performed with pulses as short as 20 ns and endurance until 3.2×10^5 [193]. A further improvement

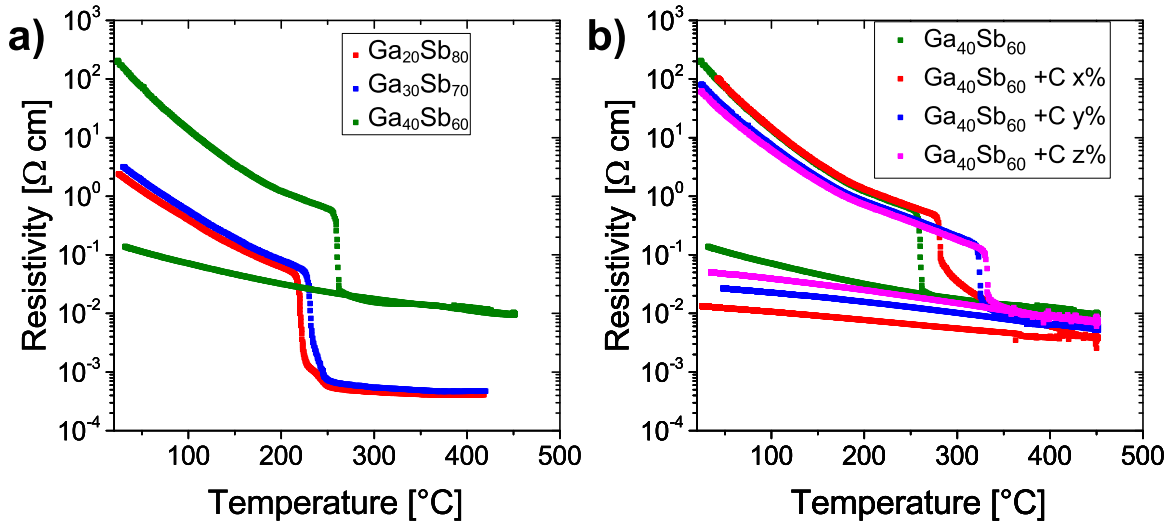

Fig. 5.13. Resistivity of as-deposited materials analyzed as a function of the temperature, measured during a ramp up of 10 °C/min comparing GaSb with three different percentage of Ga and Sb (a) and $Ga_{40}Sb_{60}$ doped with three different amount of C (b).

	$Ga_{40}Sb_{60}$	**$Ga_{40}Sb_{60}$+C x%**	**$Ga_{40}Sb_{60}$+C y%**	**$Ga_{40}Sb_{60}$+C z%**
Initial V_{th} [V]	1.0±0.1	0.9±0.3	1.6±0.1	1.8±0.6
SET Resistance [kΩ]	3±1	1.7±2.2	1.1±0.2	3.6±4.4
RESET Resistance [kΩ]	30±19	73±35	33±10	58±26
RESET Current [mA]	1±0.1	1.5±0.1	1.6±0.1	1.7±0.2

Table 5.1. Comparison of C-doped $Ga_{40}Sb_{60}$ PCMs. The data are calculated on 5 devices per composition.

on amorphous stability, while maintaining a fast switching capability, has been shown in Si-doped $Ga_{19}Sb_{81}$ [194].

In order to better investigate GaSb properties varying the atomic percentages, we analyzed $Ga_{40}Sb_{60}$, $Ga_{30}Sb_{70}$ and $Ga_{20}Sb_{80}$ PCM single devices. Resistivity measurements on full sheet samples showed that the crystallization temperature of $Ga_{40}Sb_{60}$ is about 260 °C, but increasing the amount of Sb, the crystallization temperature decreases, as well as the resistivity of the amorphous and crystalline phases (Fig. 5.13a). The steep transition from the amorphous to the crystalline phase indicates a growth-dominated crystallization mechanism. Furthermore, $Ga_{40}Sb_{60}$ was doped by three different atomic percentages of carbon, named x, y, z with x < y < z. The crystallization temperature, which is almost equal in $Ga_{40}Sb_{60}$+C y% and $Ga_{40}Sb_{60}$+C z%, increases further adding C, while the amorphous-crystalline transition remains steep excepting for the composition with less C content (Fig. 5.13b).
After the material characterization, we analyzed 1R devices. $Ga_{30}Sb_{70}$ devices exhibit a high device-to-device variability, whereas $Ga_{20}Sb_{80}$ devices are not functional, mainly due to high susceptibility to phase segregation of Sb-rich GaSb into Sb and stoichiometric GaSb [195]. Among $Ga_{40}Sb_{60}$ devices tested, approximately 50% showed functionality. Moreover, N-doped $Ga_{40}Sb_{60}$ PCMs were tested, but were not able to switch

reliably between SET and RESET state. On the contrary, all C-doped devices tested functioned. $Ga_{40}Sb_{60}$+C devices need an initialization step with the overcoming of a threshold voltage, which increases as the C content increases, as indicated in Table 5.1. Indeed, $Ga_{40}Sb_{60}$+C y% and $Ga_{40}Sb_{60}$+C z% devices shows a high initial resistance of

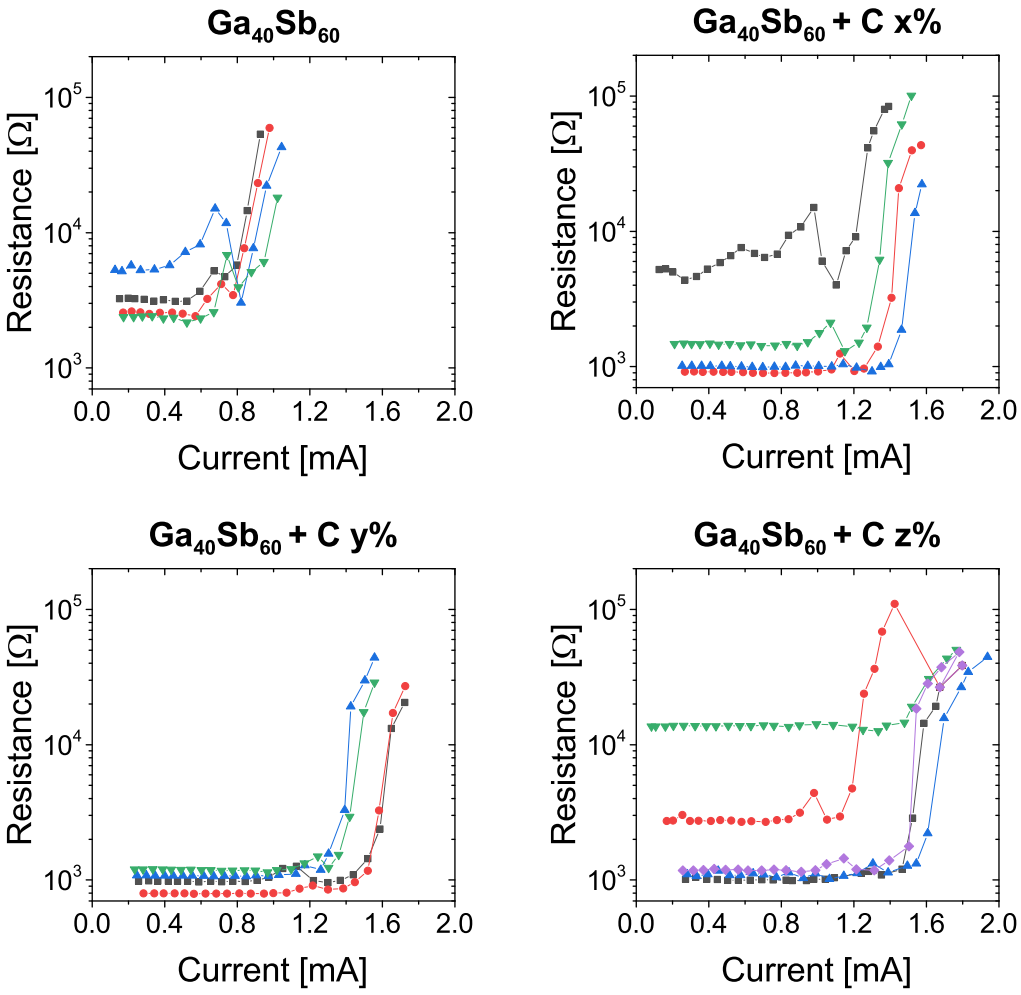

Fig. 5.14. R-I characteristic achieved in $Ga_{40}Sb_{60}$ and C- doped$Ga_{40}Sb_{60}$ with a staircase up in 5 devices for each composition.

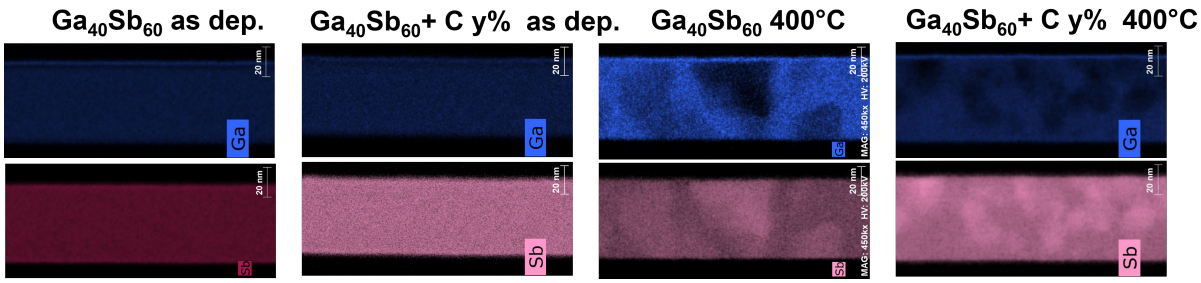

Fig. 5.15. TEM analysis performed on as-deposited full sheet samples and annealed at 400 °C for $Ga_{40}Sb_{60}$ and $Ga_{40}Sb_{60}$+C x%.

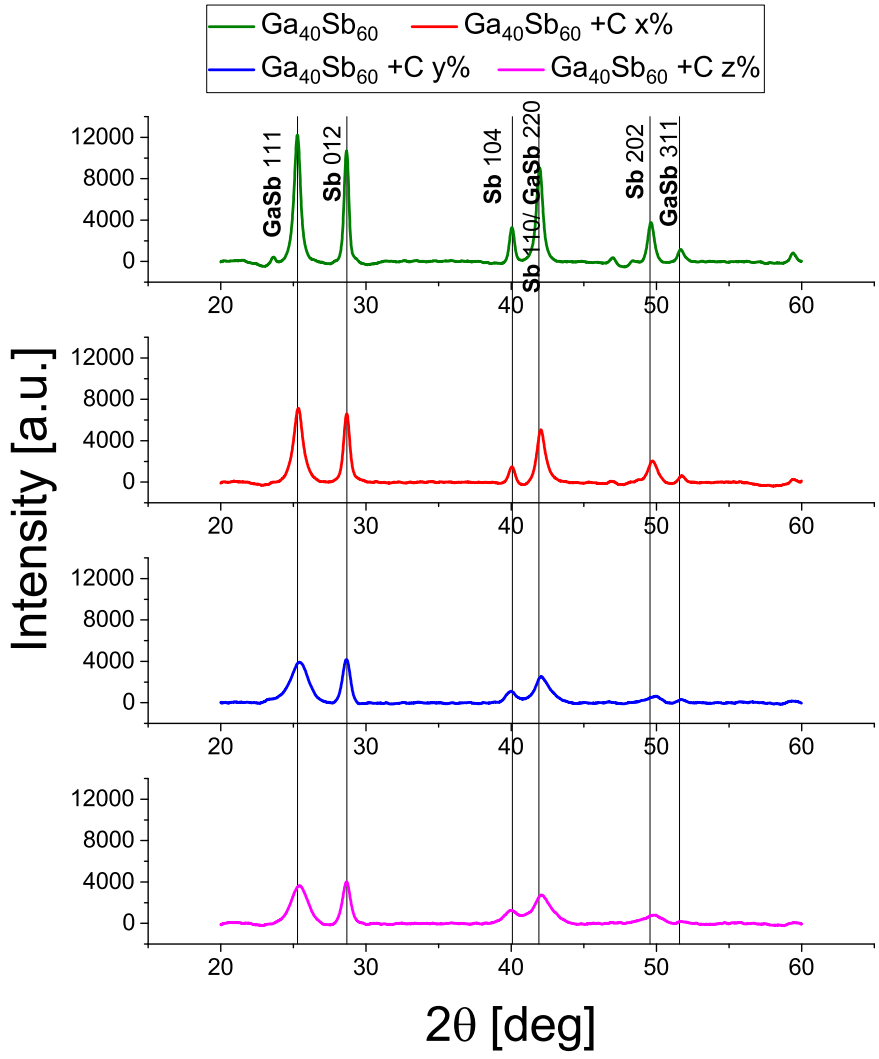

Fig. 5.16. XRD measurements of $Ga_{40}Sb_{60}$ and C-doped $Ga_{40}Sb_{60}$ samples annealed at 400 °C.

about 10^6 Ω, while $Ga_{40}Sb_{60}$+C x% exhibits a variable initial resistance from 10^3 Ω to 10^7 Ω. Moreover, the RESET current increases as the C content increases. R-I characteristics in Fig. 5.14 show a high device-to-device variability in $Ga_{40}Sb_{60}$+C x% and $Ga_{40}Sb_{60}$+C z% PCMs, while undoped $Ga_{40}Sb_{60}$ and $Ga_{40}Sb_{60}$+C y% devices tested have an uniform behavior. In order to better investigate these two compositions, TEM analysis were performed on full-sheet samples (Fig. 5.15), showing the presence of Sb enriched grains in both undoped and C-doped $Ga_{40}Sb_{60}$. However, the elemental segregation is more pronounced in the undoped $Ga_{40}Sb_{60}$, justifying the fact that a higher yield has been demonstrated in $Ga_{40}Sb_{60}$+C y% PCMs, contrary to $Ga_{40}Sb_{60}$ where only about 50% of tested devices were functional. Therefore, $Ga_{40}Sb_{60}$ doped with the intermediate amount of C is the most interesting composition since this particular amount of C helps in reducing the phase segregation typical of off-stoichiometric GaSb, evidenced also by XRD analysis, which indicate the coexistence of rhombohedral Sb and cubic GaSb phases on samples annealed at 400 °C (Fig. 5.16).
The crystallization temperature higher than 300 °C, the enhanced yield, the high crys-

tallization rate related to the growth-dominated crystallization make $Ga_{40}Sb_{60}$+C y% a potential candidate for S-SCM applications. In order to support this hypothesis, endurance and speed analysis at statistical level should be realized.

5.3 Summary of the chapter

We investigate through electrical characterization an innovative PCM device based on a TiTe/GST bi-layer stack. The TiTe layer was engineered to be stable after the fabrication process, as demonstrated by the low variable resistance distributions of as-fabricated 4kb devices and by TEM/EDX analyses. The first programming into the high resistive state gives rise to a new alloy made by GST and TiTe, that showed improved performances with respect to GST, such as higher speed and intermediate states featuring lower variability. Endurance up to more 10^8 cycles was demonstrated, nevertheless a modification of R-I characteristic and a reduction of SET and RESET resistances were found after aging. The obtained new alloy revealed striking stability along cycling, showing high SET speed and reduced C2C variability even in MLC mode. This new alloy, obtained from our TiTe/GST investigation, holds great promise for targeting DRAM-like performances for SCM applications. The initialization step required by TiTe/GST PCM to intermix TiTe and GST was exploited to describe an encryption application.
$Ga_{40}Sb_{60}$, $Ga_{30}Sb_{70}$ and $Ga_{20}Sb_{80}$ single devices were analyzed, however, the more the composition moves away from the stoichiometric $Ga_{50}Sb_{50}$, the worse the functioning gets. $Ga_{40}Sb_{60}$ was also studied doped by C, showing a low device-to-device variability, since C doping allows limiting phase segregation, typical of off-stoichiometric GaSb, and thus improving functionality, as demonstrated by TEM analysis.

Conclusions

Experts predict that the total amount of data in the world will reach 175 Zettabytes by the year 2025. This data explosion is pushing memory technologies to their performance and density limits. The access and writing speed of storage memory has emerged as the primary bottleneck of modern systems, particularly servers, due the growing speed of data elaboration.
The current memory hierarchy consists of a top layer, closest to the processor, which is faster and expensive, and by a bottom layer, that is more dense but slower. Storage Class Memory (SCM) was created to lessen the performance and cost barriers between storage and memory, in particular between DRAM and NAND Flash.
Therefore, non-volatility, quick access and programming times, high endurance, and low cost per bit are the essential objectives of SCM. The combination of multiple bits per cell with 3D integration can provide high density at low cost per bit, while non-volatility guarantees low power consumption compared to DRAM, which constantly needs to be refreshed.
Two types of SCM can be distinguished. Memory-type SCM (M-SCM), which is closer to DRAM while using less power at a cheaper cost than DRAM : in this case, read/write speed and endurance are crucial. Storage-type SCM (S-SCM) has properties more similar to NAND Flash, thus, cost and data retention are important, maintaining speed and endurance higher than NAND Flash.
Among emerging non-volatile memories (NVM), phase-change memory (PCM) exhibits characteristics that are appropriate for SCMs, such as scalability, multilevel cell (MLC) capability, high endurance and good speed.
PCM is a dual terminal resistive memory, whose working mechanism is based on the reversible switch from amorphous to crystalline phase by electrical pulses that generate Joule heating. The high-resistance amorphous phase is known as the RESET state, while the low-resistance crystalline phase is known as the SET state.
The introduction of 3D XPoint technology for SCM, which exploits PCMs, illustrates the great maturity of PCM. However, 3D XPoint ended its production in 2022, mainly due to the high cost of this technology which is still not competitive with NAND Flash.

Material engineering is essential to meet nanosecond programming, high endurance and low cost requirements of SCM applications. The purpose of this work is to investigate novel families of chalcogenide materials for SCM able to crystallize quickly while maintaining the material stability over repeated programming. Stoichiometry tuning, element doping and multilayer deposition of different materials are the three methods through which material engineering is addressed in this work.
State of the art “wall” PCM single devices and 4kb arrays were used for the majority

of our PCM reliability analysis.
In the third chapter, we investigate PCMs based on materials along GeTe-Sb_2Te_3 tie line, known for the high crystallization speed. First, we analyze GeTe and αGST based PCMs focusing on programming speed and endurance evolution. Both GeTe and αGST guarantee a high programming speed with pulse widths of around 100 ns. During programming cycling, αGST demonstrates an interesting increase in retention combined with decreased variability, attributable to a material evolution during cycling, that is confirmed also by the reduction of STS along cycling with a similar power law in both materials. In order to compare the effects of programming cycling in GeTe and αGST, material degradation was accelerated through long SET and RESET pulses. GeTe exhibits an anticipated deterioration of both programming states than αGST. Moreover, PCM endurance capabilities were evaluated by a series of endurance tests employing various sets of RESET/SET pulses with increasing programming times, to take advantage of the power law relationship between the number of cycles and the pulse energy. In fact, longer pulses may involve phenomena like accelerated interdiffusion of materials or electromigration when the device is subjected to high temperature gradient and a concentrated high electric field. This correlation allows to estimate an endurance up to over 10^9 cycles for αGST, demonstrating that it is more suitable for SCM applications than GeTe.
Then, we studied the effects of Si doping in αGST. Si doped devices exhibit a lower programming current and a reduced variability in 4kb arrays, despite a lower crystallization speed. Indeed, Si retards the crystallization allowing to better control the crystallization dynamic and to obtain reliable MLC operations. The high stability of the intermediate states in Si-doped αGST is confirmed by data retention at 100 °C and endurance up to more than 10^6 cycles. An iterative program and verify (PV) approach was implemented in order to benefit from the enhanced MLC capabilities of our devices. A single loop of this optimized PV procedure was used to evaluate MLC operations, which show a better yield in αGST+Si compared to αGST. However, at high number of cycles the MLC capability is reduced, although the endurance in αGST+Si could be higher than 10^8 for standard SET and RESET operations: the loss of MLC behavior is due to a Sb enrichment in the active region demonstrated by STS reduction during cycling and TEM/EDX analysis.
In the fourth chapter, we show the benefits of an engineered multilayered Sb-rich GST stack over conventional bulk reference materials. In multilayer stacks, we observe a decrease in the RESET programming current, that is maintained even after array cycling. It could be due to a higher thermal conductivity linked to a more uniform crystalline morphology of the multilayer structure, that makes homogeneous the temperature distribution over the heater, reducing the current necessary to amorphize the material. High SET speed in tens of ns range, data retention performances and high compositional stability after cycling are preserved in the multilayer PCM analyzed. Multilayer deposition in Sb-rich GST alloys brings an enhanced layer quality, evident in a decrease of device-to-device variability since the out-of-fabrication. This is accomplished despite the Sb and GST layers intermixing presumably occurred during the BEOL of the fabrication at a high thermal budget. The intermixing is not an issue, since helps in reducing the stochasticity of the crystalline grains size and orientation, thus, decreasing the variability at array level. Furthermore, low susceptibility to current overload

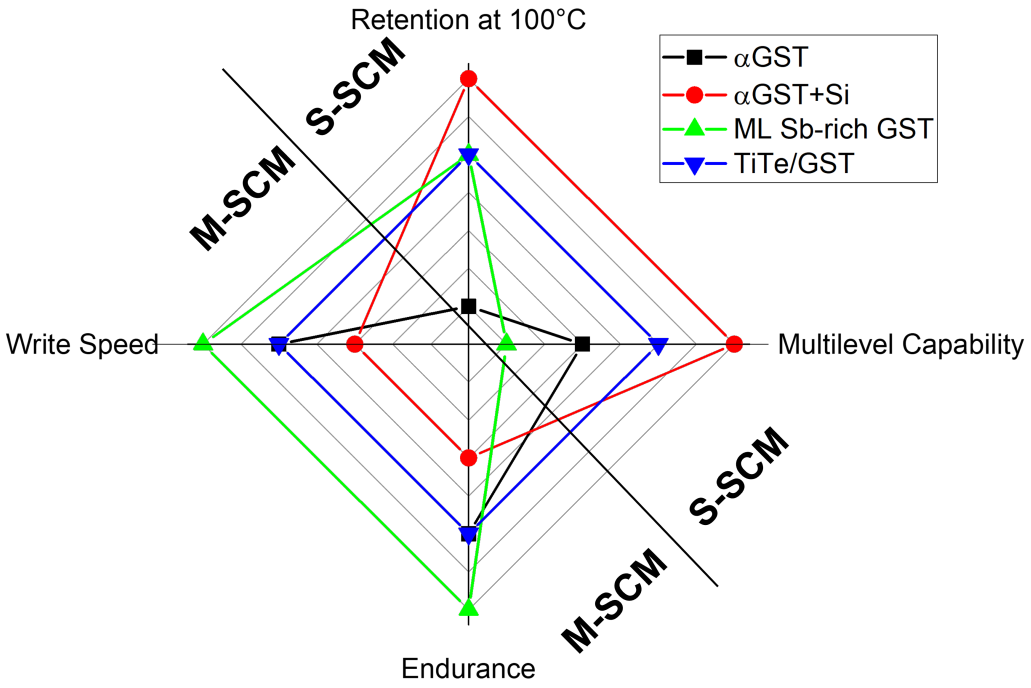

Fig. 5.17. Comparison of the main PCMs analyzed in this work. Good data retention and MLC capability are features required by S-SCM, while high endurance and high write speed are required by M-SCM.

was reported in multilayer PCM compared to bulk PCM, that allows to mitigate the variations linked to the array architecture and layout.
Additionally, we characterize Sb-rich confined single devices, which are interesting for 3D compatibility and low power consumption. Sb-rich GST exhibits suitability for this architecture due to its rapid crystallization rate, which enables a transition to the SET state even when the phase change volume is entirely amorphous and no crystalline seeds are present.
We investigate an innovative TiTe and GST bi-layer (TiTe/GST) stack, that exhibits a low device-to-device variability at the out-of-fabrication. A novel alloy consisting of GST and TiTe intermixing is created after the first programming into the high resistive state. This alloy shows an improved MLC capability and a higher SET speed than standard GST. We analyze the behavior of TiTe/GST after cycling discovering that, although endurance can be up to more than 10^8, aging modifies the R-I characteristic and reduces SET and RESET resistances. The novel alloy obtained after aging demonstrates endurance stability, a SET programming time of 60 ns, and minimized cycle-to-cycle variability.
Furthermore, we analyze GaSb-based PCM demonstrating that C doping aids in improving yield, lowering device-to-device variability, and reducing segregation typical of off-stoichiometric GaSb.

Fig. 5.17 presents an overview of the main PCMs investigated in this work. Among the materials analyzed, both multilayer and bulk Sb-rich GST are characterized by the highest SET speed with a latency of 30 ns that, together with a remarkable com-

positional stability after aging, make them more suitable for M-SCM. Also αGST alloy demonstrates suitability for M-SCM applications thanks to the good programming speed and the high endurance, while the improved MLC capability and retention obtained by an optimized Si doping in αGST, make αGST+Si suitable for S-SCM. TiTe/GST exhibits features appropriate for both S-SCM and M-SCM, but we need to specify that the initial intermixed TiTe/GST is characterized by a good MLC capability and, thus, could be used for S-SCM, while after endurance cycling, the resistance window is reduced and the SET speed is improved, making this composition more suitable for M-SCM.
A further analysis could be realized to validate the properties of these materials on more scaled architectures, in order to reduce the cost and increase the density of the final PCM product.
The excellent speed and endurance of Sb-rich GST, together with its functionality in confined architecture, that is 3D compatible, make interesting the investigation of 3D confined Sb-rich PCMs towards high-density applications.
A statistical investigation can be also worthwhile in C-doped GaSb thanks to the promising data retention, crystallization rate and yield.
In addiction to the density, the second factor that can make PCM for SCM mainstream is the wafer cost, which can be reduced running the technology in high volume. This could be realized if the stand alone memory production is accompanied by the technology use in embedded systems.
Machine learning, artificial intelligence applications and other systems that must quickly react to rapid load variations, will necessitate SCM, since DRAM employment requires high cost and high energy consumption. A new interconnect standard, Compute Express Link (CXL) was ideated to help data centers to handle more efficiently high data load maintaining data coherence between processor and memory and creating shared pools of SCMs across host and device [196]. CXP would increase bandwidth and memory capacity enabling lower latencies.
Therefore, SCM future is promising and PCMs are probably going to contribute to it.

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