Characterization and Modeling of FD-SOI Qubit MOS devices down to deep cryogenic temperatures for quantum computing applications

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préparée au sein du **CEA-LETI**
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Characterization and Modeling of FD-SOI Qubit MOS devices down to deep cryogenic temperatures for quantum computing applications

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Abstract

A massive production of qubits will be necessary for the future quantum processors. However, these qubits, to be functional, usually must be cooled down to a few tens of mK. Measuring the physical properties of qubits at these very low temperatures is currently done on individual devices, and requires a lot of time, typically a few days per qubit. The preselection of qubit devices potentially functional from the physical and technological parameters measured at $T = 300K$ and down to $T = 4.2K$, using faster measurements and compatible with a quasi-industrial approach, remains a challenge.

The goal of this thesis is to characterize, from room down to deep cryogenic temperatures, LETI qubit devices in transistor – like regime and to develop compact models, valid in a wide temperature range, that permit the extraction of the main devices' parameters. Both the models and the characterization methods developed can be used to select potentially functional quantum bits devices.

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Chapter 1: Quantum computing at industrial level

1.1 INTRODUCTION

The need of quantum computers to simulate quantum mechanics was firstly foreseen by Richard Feynman in the early ‘80s [1]. In the following years, the development of quantum algorithms not necessarily related to quantum mechanics, such as the factoring algorithm by Peter Shor [2] and the searching algorithm by Lov Grover [3] [4], unveiled the possibility of using quantum computers in a broader spectrum of domains, ranging from information security to finance [5]. Indeed, quantum computers provide a speed – up over classical ones just in solving exponentially growing problems, such as proteins’ simulations. A quantum computer runs the same algorithm several times over again, and the final output corresponds to the most likely solution of the several runs. Twenty years ago, quantum computing aroused the interest of many industrial actors, such as the Canadian company D – Wave System [6], and the U.S. companies IBM [7], Google [8] and Intel [9].

In most cases, the industrial and commercial R&D efforts are focused on solid – state quantum bits (qubits) implementations. In general, solid – state qubits can be split in two categories: superconducting Josephson junctions [10] [11] and spin qubits in silicon [12] [13], which are in principle compatible with the CMOS technology used for the room temperature control read – out electronics. Indeed, increasing the dimensions of the quantum processors, the number of interconnections required to address individually each qubit becomes very soon intractable. The quantum chip is placed usually at the bottom of a dilution refrigerator, cooled down to few mK. The interconnections pass from this environment to the $4.2\ K$ stage all the way to outside [14]. One of the most envisaged solutions for the cable connections management is to bring the front – end electronics close to the $4.2\ K$ stage [15] [16] [17] [18], and ultimately to co – integrate it on the quantum chip.

This Chapter introduces briefly the concept of quantum bit and its main technological implementations, with a specific focus on silicon quantum bits. Moreover, the Si qubit industrial technology state – of – art is presented. In this context, the LETI technology is discussed in details, showing the main devices' architectures. Finally, once that the technological perspectives are given, the motivations and goals of this work will be clarified and the main points of the thesis will be outlined.

1.2 QUANTUM BITS

A quantum bit is an elementary unit of quantum information, and it is the quantum-computing counterpart of the classical bit in a conventional computer. In general, a quantum bit is a two – level quantum - mechanical system [19] and, contrary to a classical bit that can have just two values, it can be both in the ground and excited state at the same time (see Fig.(1.2.1)) [14].

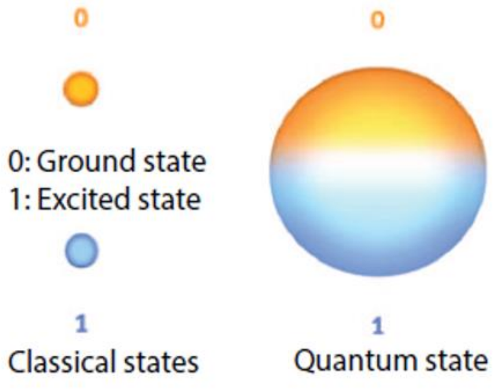

Figure 1.2.1 Abstract representation of a classical and quantum two – level system. Image taken from [14].

Some examples of physical systems that can be exploited as quantum bits are the electron or nuclear spins, and two different polarizations of a photon.

Quantum computers rely on two quantum – mechanical properties of qubits, which are the quantum superposition and the quantum entanglement. The first property is a fundamental principle of quantum mechanics and affirms that two or more quantum states can be added, and the results will be another quantum state. Taking as reference Fig.(1.2.1), if the system has two basis states $|0\rangle$ and $|1\rangle$, a generic state can be expressed as $|\psi\rangle = \alpha_1|0\rangle + \alpha_2|1\rangle$, where α_1 and α_2 are complex coefficients. When the quantum – mechanical system is measured, the outcome can be either "0", with probability $|\alpha_1|^2$, or "1", with probability $|\alpha_2|^2$.

The second property is the quantum entanglement, which was first introduced by Albert Einstein [20]. If two qubits are entangled, a correlation exists between them. More specifically, if a qubit is in a particular state, the other qubit has to be in another specific state, defined by the first one. An example of entangled system concerns two electrons' spins: if the first electron has a spin – up, the second one has to have a spin – down.

1.3 QUBIT IMPLEMENTATION

The theoretical physicist David DiVincenzo introduced a list of requisites that quantum bits should respect. These are called usually "DiVincenzo criteria", and are the following [21]:

- A physical scalable system
- Ability to initialize the state of the qubits
- Coherence time longer than the gate operation time
- A universal set of quantum gates
- A qubit – specific measurement capability

In the following, we are going to review the main qubit technological implementations, highlighting if they meet, at least partially, the above criteria or not.

1.3.1 **Nuclear Magnetic Resonance Qubits**

Nuclear Magnetic Resonance (NMR) qubits exploit the spin of atomic nuclei [22], and an example of implementation of Shor's algorithm was demonstrated using this technology [23]. Even if NMR qubits meet the DiVincenzo criterion for what concern coherence time, their main drawback regards the scalability.

1.3.2 **Ion Traps**

Quantum computers based on ion traps consist of linear strings of ions confined in a high electromagnetic field. Long coherence times have been proved [24], as well as good scalability [25].

1.3.3 **Superconducting qubits**

Superconducting qubit is the technology chosen by Google [11] and IBM. It consists of a Josephson junction coupled to a microwave resonator for the control read

– out. In LC circuit made of non – superconducting metals, the energy levels of the quantum harmonic oscillator are equally spaced, and therefore it is impossible to distinguish between transitions from the ground and the first excited state and transitions from other two higher orders excited states. The Josephson junction introduces a non-linearity thanks to which the energy levels are no more equally spaced. In such a system, one can recognize excitations between ground and first excited state.

1.3.4 Nitrogen vacancies in Diamond

Nitrogen vacancies (NV centers) in diamond consist of defects in diamond crystals. Their fabrication process is quite hard to control if compared to other technologies, such as superconducting or silicon qubits. On the other side, it is easy to couple them with photons, paving the way to the accomplishment of quantum networks [26].

1.3.5 Silicon Qubits

Semiconductor qubits were initially developed on III – V heterostructures, such as $GaAs/AlGaAs$ [27]. The firs electron spin quantum bit in Si was realized by a group of the University of New South Wales in Sydney in 2012 [12]. Since then, many university research groups started to develop their own silicon quantum bits, and many technological advancements were achieved, such as higher operating temperatures (above 1K) [28] [29], longer spin coherence times (up to several milliseconds) [30], and gate fidelities well above 99% [31]. Among the several possible architectures, some aroused particular interest, especially from ICTs companies, thank to their compatibility with CMOS technology. Indeed, as previously mentioned, one of the main pros of Si qubits, is the possibility of easily interfacing the quantum processor with the front – end classical electronics. The first CMOS compatible qubit was demonstrated by a group of CEA – LETI in 2016 [32]. The benefit of such architecture was twofold: from one side there was the compatibility with CMOS control read – out electronics; on the other hand, FD – SOI nanowire technology was exploited for the design and fabrication of such a qubit, and this paved the way to the possibility of recycling the expertise matured from transistor manufacturing to achieve qubit mass production. Indeed, future quantum computers will require thousands or even millions of quantum bits, in order to implement quantum error correction codes, fundamental for their correct functioning [14]. Before going through the state – of – the – art of the industrial platforms for quantum bits production, let us briefly describe how a single and double quantum dot work, since they are the basic structures of many architectures that we are going to introduce below.

1.3.6 Single and Double Quantum Dots

In this section, we will go through a brief description of the fundamentals physical principles that govern a single and double quantum dot. In both cases, we will consider an abstract scheme of such structures and not a specific architecture. For a detailed treatment of single and double quantum dots, the reader can refer to [33] and [34].

A quantum dot is a three terminal device (Fig.(1.3.1) [33]). It consists of a conductive island, coupled to two terminals, the "source" and the "drain", which allows electrons to flow. The third terminal is capacitive coupled to the island, and can be used as a gate electrode.

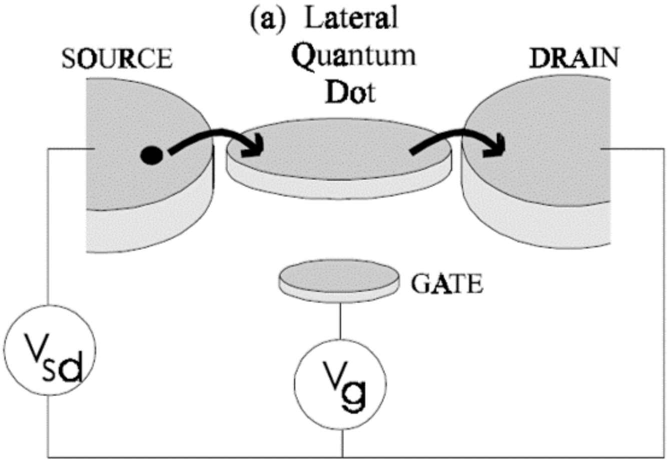

Figure 1.3.1 Schematic of a quantum dot. Figure taken from [32]

If the conductive island, i.e. the dot, is not coupled to source and drain, no electrons can flow through, and the number of charges inside the dot is constant. By coupling the island to the electrodes, an extra electron can be added to the dot only if enough energy is provided to overcome the Coulomb repulsion among electrons. This phenomenon is called "Coulomb blockade" [33] [34].

The energy landscape of a quantum dot resembles that of an atom and, for this reason, they are often referred to as "artificial atoms". Indeed, carriers are confined in all the three dimensions, and the energy levels are quantized. In order to be able to resolve these levels, $\Delta E \gg k_B T$ [33], being ΔE the energy difference between two levels in the dot, k_B is the Boltzmann constant and T the temperature in Kelvin. The previous condition partly justifies the cryogenic temperature operation of quantum dots and Si spin quantum bits. The other motivation for the low temperature-working requirement resides in the minimization of electrons' thermal energy: the charging energy, that is, the energy needed to add one electron to the dot, must be smaller than the thermal energy [33]. If it is not the case, electrons can flow freely through the dot, because the energy to overcome Coulomb repulsion is fully provided by temperature.

If a single quantum dot can be thought as an "artificial atom", a double quantum dot can be regarded as an "artificial molecule" (Fig.(1.3.2) [34]).

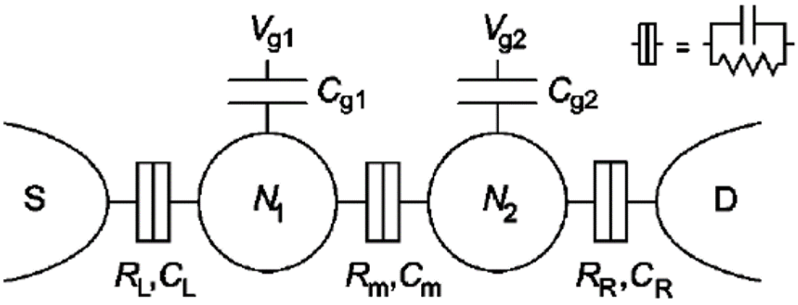

Figure 1.3.2 Schematic of a double quantum dot. Figure taken from [33]

In the structure sketched in Fig.(1.3.2), besides the coupling between dots and electrodes, there is a coupling also between dots. Depending on the strength of the inter – dot coupling, we can have two situations: if the dots are weakly coupled (Fig.(1.3.3), left side), the electrons are localized in individual dots; in case of strong coupling (Fig.(1.3.3), right side), instead, the electrons are delocalized over the entire structure. Double quantum dots are usually exploited in quantum computing experiments using one dot for manipulation and the other dot for measurement,

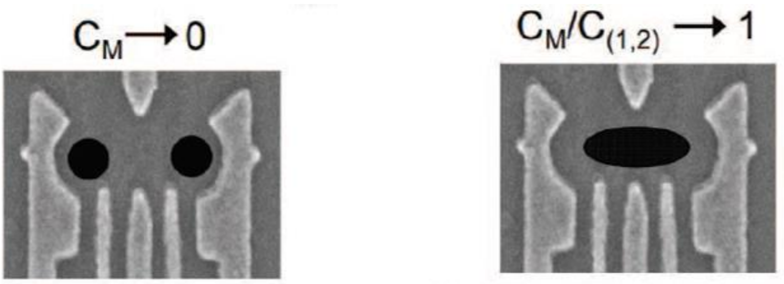

Figure 1.3.3 Weakly (left) and strongly (right) coupled quantum dots.
Figure taken from [14]

typically performed through gate reflectometry [35]. It is worth to point out that, in many Si spin qubits, holes instead of electrons are used. In order to understand why, it is crucial to remember that a magnetic moment is associated to the spin of an electron (hole). To interact with the spin, therefore, a magnetic field is required. This can be obtained in two ways: implementing a micro magnet in the device, or pushing an oscillating current through a wire that, in turn, will generate a magnetic field. Both solutions are not very scalable. A third alternative is using directly a MOS gate that, of course, cannot generate a magnetic field able to interact directly with the particle's spin. A requirement to achieve coupling between the gate electric field and the carrier spin, is using a material with strong spin – orbit coupling. In silicon, this is achieved just by holes [36].

1.4 INDUSTRIAL CMOS COMPATIBLE QUANTUM BITS

As previously mentioned, quantum computing left the shores of academic research and landed in ICTs industry. This was eased by the introduction of qubit architectures compatible with CMOS technology (Fig.(1.4.1) and Fig.(1.4.2)) [32] [37] [38].

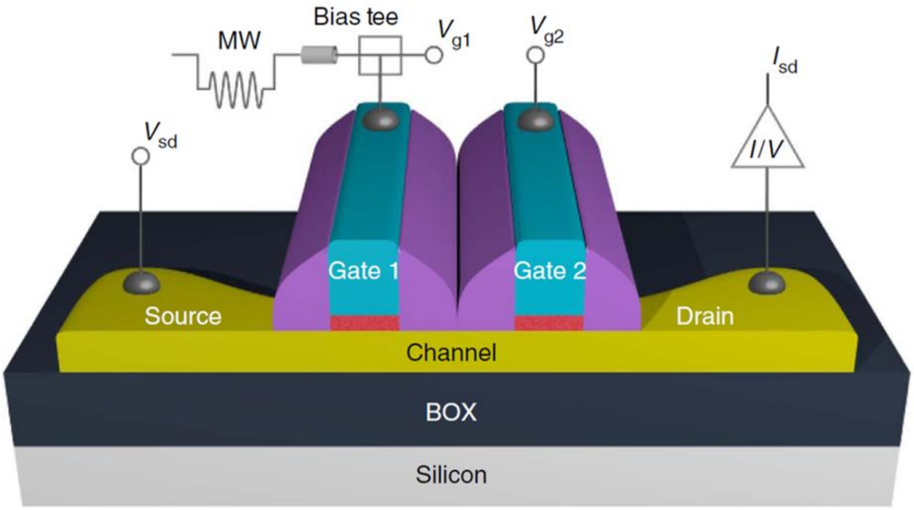

Figure 1.4.1 Cross section of double gate LETI qubit device. Image taken from [32]

Both the implementations shown in Fig.(1.4.1) and Fig.(1.4.2) consist of a double quantum dot structure and relies on FD – SOI technology. More specifically, LETI qubit is based on Si FD – SOI nanowires, therefore it is a 3D structure, whereas the one proposed in [38] is a planar device realized starting from 22nm FD – SOI technology from Global Foundries [39]. Similarly to CEA – LETI, also Intel decided

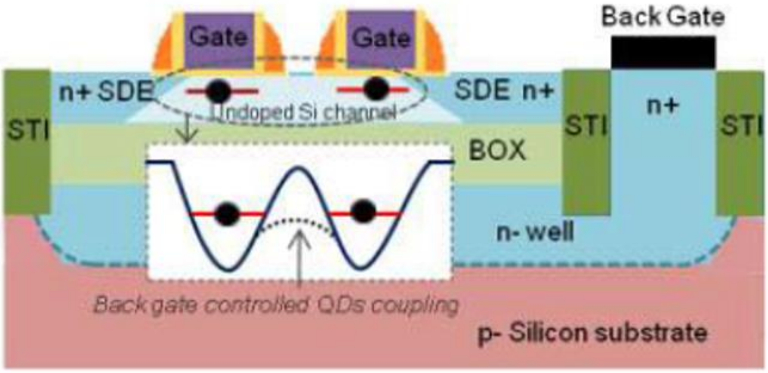

Figure 1.4.2 Qubit based on 22nm FD – SOI technology. Taken from [38]

to design its devices exploiting a 3D structure (Fig.(1.4.3)), consisting of two parallel Si fins, one that hosts the qubits and the other one that hosts the sensing dots [40]. In Fig.(1.4.3), it is also shown the industrial process flow used to fabricate the qubit devices. As already mentioned, the advantage of these MOS – based architectures is twofold: on one side, they allow to exploit the expertise in semiconductor manufacturing, facilitating a high volume qubit production. On the other side, these devices, when they do not operate at temperatures lower than 1K with extremely low bias voltages, behave essentially as transistors, enabling the exploitation of fast characterization techniques for devices' screening. In particular, the ultimate goal is developing a process flow where potentially functioning qubits are selected through room temperature measurements. Indeed, characterizations at 300 K are faster and easier than cryogenic ones, even if 300 mm wafer probers able to work at temperatures around 1K have been developed recently [41] [42] [43]. In order to link the room temperature transistor behavior with the cryogenic quantum dot and quantum bit one, it is necessary to understand how the device physics, as well as the main physical parameters, changes with temperature. A first step consists in linking the room and cryogenic temperature transistor behavior and selecting the figures of merit able to describe well the device physics at both temperatures. Afterwards, one can study and model the transition from classic to quantum regime at $T < 4.2\ K$ [44] [45]. Indeed, characterization and modeling of MOS – like structures from $T = 300\ K$ down to $T = 4.2\ K$ gained a renewed interest both because of the classical control read – out electronics that have to operate at cryogenic temperature, and also because it is a necessary step to enable fast characterization protocols for qubit manufacturing. This is the approach adopted by some companies, like Intel [40] [41] [46], and research centers, like IMEC [47] and CEA – LETI [37] [48].

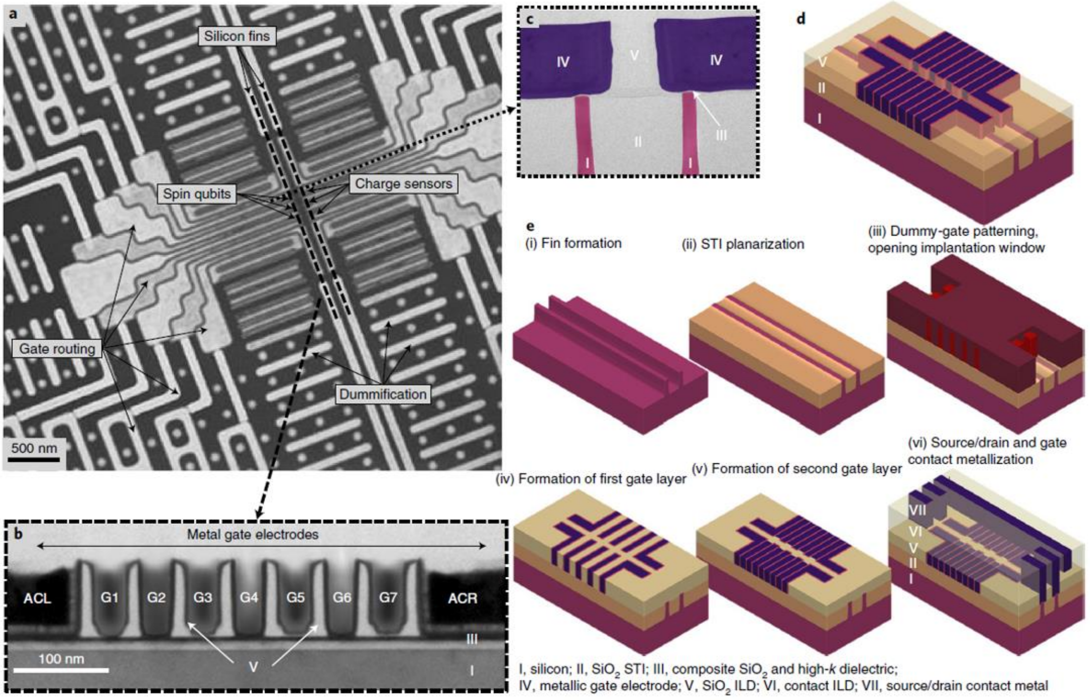

Figure 1.4.3 Industrially fabricated quantum dot devices from Intel [40].

1.5 LETI QUBIT TECHNOLOGY

LETI qubit devices can be categorized into two groups: “pump” and “split – gate” devices. Both are fabricated starting from CEA – LETI FD – SOI NanoWire (NW) process flow [37] [48]. NWs are fabricated from 300mm SOI wafer, with 145 nm of buried oxide thickness and a variable Si film thickness, ranging from $t_{Si} = 8\ nm$ to $t_{Si} = 18\ nm$. The active area is defined by etching and MESA isolation. The gate, composed of 6nm of thermally grown SiO_2 and 5nm of TiN metal layer, wraps around the Si NW. High – k dielectrics, usually introduced in MOSFET gate stack process, were avoided because of their trapping issues [49].

In “split – gate” devices, a single gate is split into two “face – to – face” devices (Fig.(1.5.1), bottom), permitting an independent electrostatic control of the two dots located underneath each corner. “Pump” devices, instead, consist of nanowires with several gates placed in series (Fig.(1.5.1), top). The simplest structure, that has only two gates (Fig.(1.4.1)), uses one gate for spin manipulation and the other one for the read – out [32]. Both the architectures can contemplate multiple gates in series and, in the case of “split – gate” devices, this translates in having two rows of dots, similarly to Intel quantum bits shown in Fig.(1.4.3).

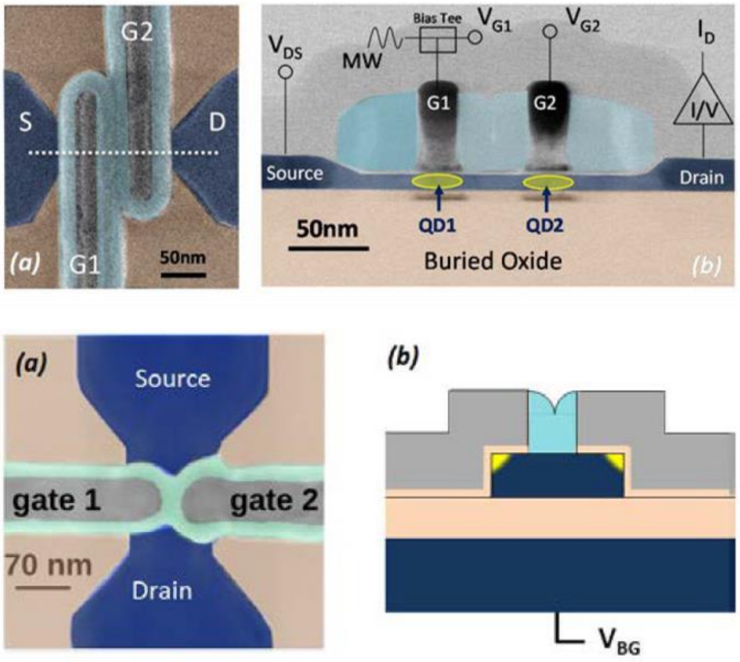

Figure 1.5.1 (Top) “Pump” device with two gates in series and (bottom) face – to – face device. Taken from [48]

In this thesis, we focus on the characterization of “pump” devices, with a number of gates ranging from one to five. Multiple gates structures, e.g. four – gates devices (Fig.(1.5.2)), have shown to be functional qubit as well. Indeed, normally only one gate is exploited for spin manipulation, whereas the others are used as carriers reservoirs or for the read – out [50].

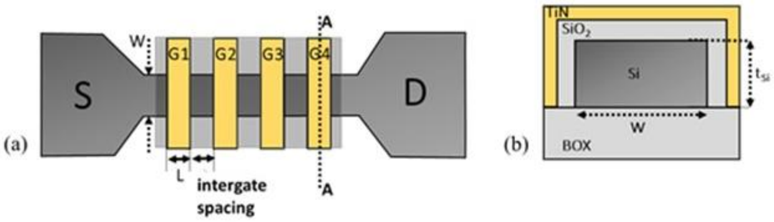

Figure 1.5.2 (a) 4G device top – view schematic. (b) AA cross - section

From Fig.(1.5.1) and Fig.(1.5.2) it is clear that, if all the gates are biased at a voltage high enough to invert the channel, the “pump” devices are basically transistors. In all the characterizations shown in this work, we distinguished between the “active gate” where the voltage is swept and that effectively controls the drain current, and the “external gates”, biased at a fixed potential in order to invert the portion of channel not controlled by the active one.

Devices are characterized normally in liner regime ($V_D = 50\ mV$), and it is worth pointing out that, at this voltage, they maintain a transistor – like behavior down to $T = 4.2\ K$.

1.6 THESIS MOTIVATION AND OUTLINE

As previously mentioned, in order to facilitate the development of industrial quantum bits, fast characterization methods for devices’ screening must be developed accordingly. In particular, it turned out to be fundamental to exploit the transistor – like behavior of such Si qubits to link the room temperature to the quantum dot behavior. The goal of this thesis is to characterize, from room down to deep cryogenic temperatures, LETI qubit devices in transistor – like regime and to develop compact models, valid in a wide temperature range, that permit the extraction of the main devices’ parameters. Both the models and the characterization methods developed can be used to select potentially functional quantum bits devices. Moreover, the understanding of the device physics at a transistor level can provide a better comprehension of the quantum dot and quantum bit behavior. Indeed, for example, low field mobility turned out to have a crucial role for selecting the gates that can be devoted to carrier’s spin manipulation and those that can be used as carrier reservoirs. It is worth to point out that, many of the compact models developed in this work can be used also for classical cryogenic MOSFETs.

The second chapter is dedicated to the development of TCAD tools able to simulate the device physics from room down to cryogenic temperature. An analytical approximation of the Fermi – Dirac function with 3D density of states is introduced, thanks to which it is possible to calculate the carrier density in a given structure. The simulation model developed can be applied both to a classical MOSFET and to a qubit device. Simulating the electrostatics and the transport is essential to understand some experimental data, such as the non linear $I_D(V_D)$ at small biases and cryogenic temperature. Moreover, it is demonstrated that, below $T \leq 20\ K,$ the electrostatics of the device does not change significantly.

The third chapter is focused on compact modeling. Two kind of compact models are discussed: those based on the Maxwell – Boltzmann statistics, like the Lambert –

W function, and those that relies on the Fermi – Dirac one. They were shown to be effective down to deep cryogenic temperatures and to be able to extract reliable values of the main device parameters. Moreover, it is proposed an explanation of the origin of the zero temperature coefficient in MOSFETs, which is corroborated by some simulations, performed using the model developed in the second chapter. Furthermore, one-dimensional confinement is demonstrated to be responsible of some features observed in strong inversion. Finally, subthreshold current oscillations are modeled qualitatively and explained using the percolation transport theory.

The fourth chapter is dedicated to devices' characterization from $T = 300\ K$ down to $T = 4.2\ K$. First, a large area FD – SOI device is characterized, and the main experimental quantities are shown at different temperatures, such as capacitance, drain current and mobility curves. We test the validity of the models previously introduced by fitting the experimental data and by extracting the main figures of merit. After having benchmarked both the technology and the compact models on a wide area standard device, we characterize a five – gate pump device. In this context, we introduce an ad – hoc compact model, based on the Lambert – W function, for the extraction of the main device's parameters. Low field mobility turns out to be a critical parameter to select gates that could be used efficiently as quantum dots. Finally, we discuss the impact of high V_D on the multi – gate devices at cryogenic temperature.

Chapter 5 is devoted to the static and dynamic variability of four – gates pump devices. First, static variability, or matching, at room temperature is discussed. Indeed, matching studies are essential for technological benchmarking. In this context, gates of the same device are compared. Both the electrical and the statistical analysis are then modeled using the Lambert – W function method. Afterwards, dynamic variability, or noise characterization, is performed. In this case, two devices are selected and tested both at $T = 300\ K$ and $T = 10\ K$. Both flicker and random telegraph noise are present in the devices. The $1/f$ noise was shown to be caused by carrier number and mobility fluctuations. Finally, the same Lambert – based model developed for the static variability is applied to noise curves, and its validity is proven at both temperatures.

Chapter 2: TCAD Simulations at Cryogenic Temperature

2.1 INTRODUCTION

TCAD modeling plays a fundamental role in the semiconductor industry, facilitating transistors mass production by providing support both in the device design and in the experiments interpretation. Quantum computing, in order to evolve from a basic research field to an industrial technology, must rely on an equivalent background of modeling expertise and tools. Indeed, if quantum bits mostly lean on non-commercial tools [51], CMOS devices, that are essential for the control read-out electronics [52], are lacking from effective TCAD modeling at deep cryogenic temperatures, i.e. $T < 77\ K$, even if, recently, efforts were made in simulating an nMOSFET down to 5 K [53].

In this chapter, the focus is on the TCAD modeling of FD-SOI devices down to deep cryogenic temperatures. First, in section 2.2, the physical models used in the simulations are shown, with particular emphasis on the choice of the carrier statistics to represent the system. An example of what is possible to achieve with the models previously described is presented in section 2.3, where a single gate FD-SOI device is considered as test structure, whose dimensions are inspired by the LETI qubit technology [32] [48]. In this context, the effects of channel length reduction, i.e. short channel effects (SCE), are investigated at both room and deep cryogenic temperatures, as well as the impact of high drain biases on the device performances. Afterwards, the simulations are extended to multi-gate devices, which are more interesting in a quantum computing perspective, since they will be effectively exploited as quantum bits.

2.1.1 FlexPDE

FlexPDE was used in this thesis (at http://www.pdesolutions.com/). It is a partial differential equation solver, that allowed us to simulate both the electrostatics and the transport in several n-type FD-SOI structures down to deep cryogenic temperatures using an analytical approximation of the Fermi-Dirac integral with 3D density of states (DOS) and even down to zero kelvin using the metallic statistics.

2.2 TCAD MODELING DESCRIPTION

The device electrostatics is simulated solving the Poisson's equation

$$\boldsymbol{\nabla} \cdot (\epsilon \nabla V) = \rho \tag{2.2.1}$$

where ϵ is the material permittivity, V is the electrostatic potential and $\rho = q(n - p)$ is the total charge density, n is the electron density and p is the hole density. Transport is obtained by coupling eq.(2.2.1) with the current continuity equation in stationary conditions for an n-type FD-SOI, given by

$$\boldsymbol{\nabla} \cdot \left(n\mu_{eff} \nabla V_n\right) = 0 \tag{2.2.2}$$

where μ_{eff} is the effective carrier mobility and V_n is the quasi-Fermi potential for electrons. It is worth to point out that eq.(2.2.2) also holds for holes.

The carrier density in eq.(2.2.1) and eq.(2.2.2) is not known and it is generally given by:

$$n = \int_{E_C}^{\infty} N(E) f(E) dE \tag{2.2.3}$$

where E_C is the bottom of the conduction band, $N(E)$ is the density of states (DOS) and $f(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{k_B T}\right)}$ is the Fermi-Dirac function, where E_F is the Fermi level, k_B is the Boltzmann constant and T is the temperature. The solution of eq.(2.2.3) depends on the DOS chosen to describe the system, that, in turn, is related to the dimensionality of the system itself. The solutions and the approximations used in our model are described in details in the next paragraphs.

Once the electrostatics and the quasi-Fermi potential together with the carrier density are known for a given gate voltage V_G and drain bias V_D, it is possible to calculate the main device's electrical characteristics. It can be useful to mention that the gate-to-channel capacitance $C_{gc} = \frac{dQ_{inv}}{dV_G}$, is computed from the total device energy ΔW_e as [54] [55]

$$C_{gc} = \frac{2\Delta W_e}{\Delta V_G^2} \tag{2.2.4}$$

Eq.(2.2.4) was shown to provide a more precise evaluation of the capacitance [54]. Moreover, from [54]

$$\Delta W_e = \int_{Device} \frac{\epsilon \Delta E^2 + \Delta\rho\Delta V}{2} dv \tag{2.2.5}$$

where ΔE is the local field variation, ΔV is the local potential change, $\Delta\rho$ is the local charge density difference for gate voltage varying from V_G to $V_G + dV_G$. The first term in the integral in eq.(2.2.5) corresponds to the electric field energy, whereas the second term is the work done on the system by bringing charge from infinity. Furthermore, eq.(2.2.5) allows computing the energy in every device region (see Fig. 2.3.1), permitting the calculation of the different contributions to the total capacitance.

Concerning the drain current I_D, it is computed within the gradual channel approximation (GCA) as [56]

$$I_D = \frac{W}{L}\int_0^{V_D} \mu_{eff} Q_i dV_n \tag{2.2.6}$$

where $Q_i = q \cdot n$ is the inversion charge. Different effective mobility laws can be implemented, enabling the simulations of different transport phenomena, as shown in the next chapters.

Finally, the quantum confinement effect at the $Si - SiO_2$ interfaces is accounted for using the Hansch correction [57]:

$$n_{QM} = n \cdot \left(1 - \exp\left(-\frac{y^2}{\lambda_{TH}^2}\right)\right) \tag{2.2.7}$$

where n_{QM} is the carrier density accounted for the quantum mechanical correction, n is the classical carrier density, whose expression will be given explicitly in the next paragraph, y is the vertical position inside the channel and $\lambda_{TH}^2 = \hbar^2/2mk_BT$ is the thermal wavelength, $\hbar$ is the reduced Planck's constant and m the electron effective mass.

2.2.1 Carrier statistics

In the simulations, 3D DOS are used, at both room and cryogenic temperatures. Indeed, even though the inversion channel can be well approximated to a 2D system at cryogenic temperature, the DOS must account for the dimensionality of the simulated structure. In this way, eq.(2.2.3) reads [56]

$$n = N_C(T)\frac{2}{\sqrt{\pi}}F_{\frac{1}{2}}(u) \tag{2.2.8}$$

where $N_C(T) = 2 \cdot 10^{19} \cdot \left(\frac{T}{300}\right)^{\frac{3}{2}}$ is the 3D effective density of states, and

$$F_{\frac{1}{2}}(u) = \int_{E_C}^{\infty} \frac{E^{\frac{1}{2}}}{1 + \exp(E - u)} dE \tag{2.2.9}$$

is the Fermi-Dirac integral of order $1/2$, and $u = (E_F - E_C)/k_B T$. In the following, we will distinguish two cases: non-degenerate and degenerate semiconductors.

Non-degenerate case – Room temperature

In non-degenerate semiconductors, the Fermi level is several $k_B T$ below the conduction band edge E_C and eq.(2.2.8) can be approximated with the Maxwell-Boltzmann (M-B) statistics:

$$n = N_C(T) \cdot \exp\left(-\frac{E_C - E_F}{k_B T}\right) \tag{2.2.10}$$

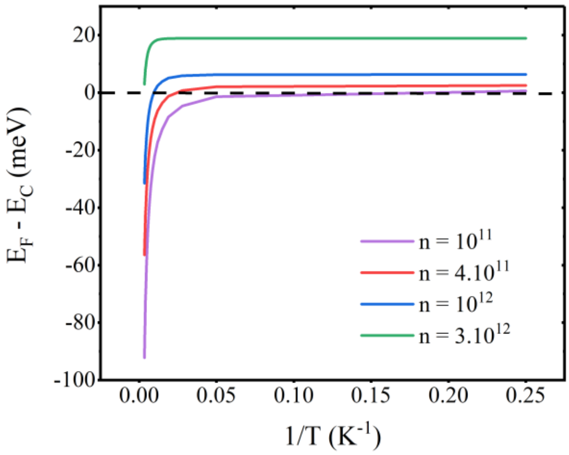

Figure 2.2.1 Variations of the Fermi level with the inverse of temperature

In bulk MOSFETs, E_F, and therefore the eventual semiconductor degeneracy, is controlled by the substrate doping concentration: if its level is smaller than N_C, the semiconductor is non-degenerate [56]. In the case of FD-SOI, the semiconductor is intrinsic, and then it is non-degenerate by definition. The Fermi level, however, is not only governed by the substrate doping and gate voltage, but also by temperature.

In Fig.(2.2.1) the Fermi level variation with temperature is plotted for different electron densities in the inversion layer (see also [58]). As can be observed, the

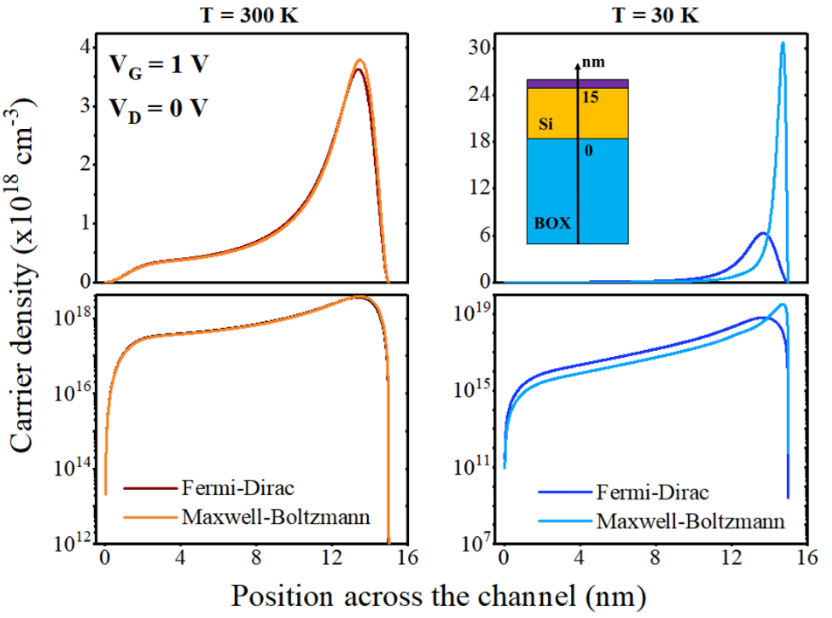

Figure 2.2.2 Comparison between carrier densities calculated with M-B and F-D statistics across the device channel, both at $T = 300\ K$ (a)-(c) and at $T = 30\ K$ (b)-(d).

inversion layer degenerates at smaller electron densities as the temperature is lowered. It is important to underline that, in FD-SOI, the effect of cryogenic temperatures is to degenerate the inversion layer, not the entire semiconductor, which is non-degenerate by definition. The same argument can be used to discuss the effect of high gate voltages, as can be inferred by Fig.(2.2.1).

Degenerate case – Cryogenic temperature

As previously demonstrated, at cryogenic temperature the inversion layer becomes degenerate and the Maxwell – Boltzmann statistics is not valid anymore. Indeed, by comparing the carrier density distribution across the Si channel calculated with F-D and M-B, it is possible to observe that they are in good agreement at room temperature, whereas M-B greatly overestimates the carrier confinement at the $Si - SiO_2$ interface at $T = 30\ K$ (Fig 2.2.2).

From these considerations it is evident that one must rely on eq.(2.2.8) for simulations at cryogenic temperatures. Since the Fermi-Dirac integral (eq.(2.2.9)) has no analytical solution, an analytical approximation was used [59] [60]:

$$F_{app}(u) = \frac{\sqrt{\pi}}{2} \ln\left(1 + \exp\left(2\frac{u}{3}\right)\right)^{\frac{3}{2}} \left(1.2 + 0.2 \tanh\left(\frac{u}{3}\right)\right) \tag{2.2.11}$$

Note that this simple approximation for $F_{\frac{1}{2}}$ provides less than 10% of error with u varying between -15 and $+15$ as shown in Fig. 2.2.3. The error on the charge density is lower, since eq.(2.2.11) must be calculated for all the Fermi level values across the channel, i.e. it is function of the channel cross-section position. The charge $Q_{inv}(x, y)$ such obtained is then integrated over the channel to get the total Q_{inv}.

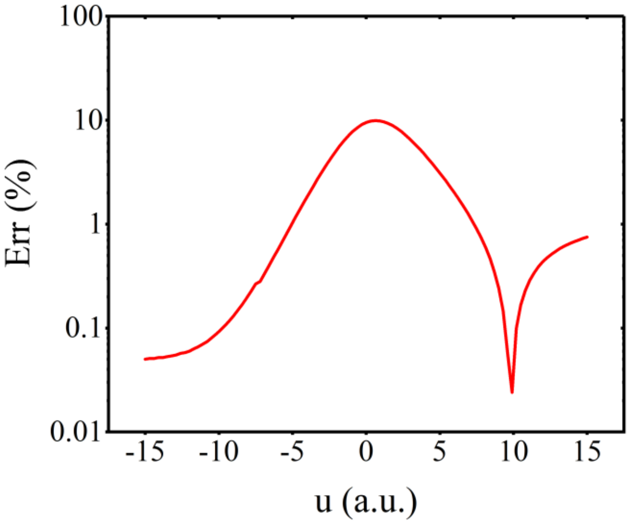

Figure 2.2.3 Percentage error between $F_{\frac{1}{2}}$ and F_{app} versus u

The results at deep cryogenic temperatures are also compared to those obtained using the fully degenerate metallic statistics, i.e. the zero temperature approximation (ZTA) [59]:

$$n_{deg}(E_F, T) = N_C(T) \cdot \frac{2}{\sqrt{\pi}} \left(\frac{2}{3} \left(\frac{E_F}{k_B T} \right)^{\frac{3}{2}} \right) \tag{2.2.12}$$

2.3 FD-SOI SINGLE GATE DEVICE

In Fig.(2.3.1).(b) is sketched the structure that we simulated, whose dimensions are reported in Table (2.3.1). They are inspired by the LETI qubit technology [32].

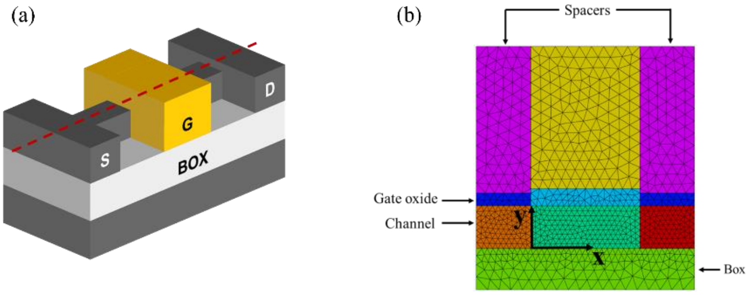

Figure 2.3.1 (a) 3D sketch of LETI qubit technology and (b) simulated cross-section

Parameter	Dimension
Silicon thickness (t_{Si})	15 nm
Buried oxide thickness (t_{BOX})	145 nm
SiO_2 oxide thickness	6 nm
Channel length (L)	40 nm
Si_3N_4 Spacer length	20 nm
Channel width (W)	75 nm

Table 2.3.1 Device dimensions

In the simulations, in order to improve the mesh, we reduce t_{BOX}, and we increased by the same factor the oxide permittivity, in order to keep the buried oxide capacitance constant. In order to take into account the influence of source and drain, that are not explicitly considered here, the built-in potential calculated with degenerate statistics (eq.(2.2.12)) $V_{bi} = V_0 + \left(3\sqrt{\pi}\frac{N_D}{4N_{cc0}}\right)^{\frac{3}{2}}$ is imposed as boundary condition, where V_0 is the intrinsic Fermi potential, N_D is the source/drain doping concentration and $N_{cc0} = 2 \cdot 10^{19}/(k_B \cdot 300)^{\frac{3}{2}}\ (eV^{\frac{3}{2}}/cm^3)$ a constant.

Device Electrostatics

In Fig.(2.3.2) are reported the carrier density distributions across the channel as function of temperature, both in linear (Fig.(2.3.2).(a)) and logarithmic (Fig.(2.3.2).(b)) scale. The gate voltage is set to $V_G = 2\,V$, for which the channel is fully inverted, and the drain bias to $V_D = 0\,V$.

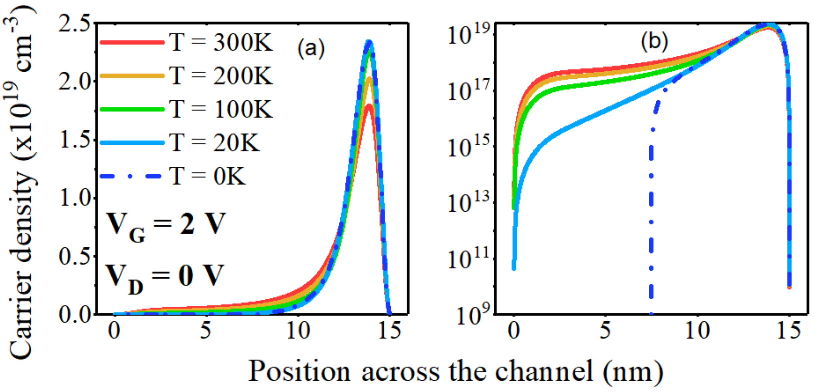

Figure 2.3.2 Simulated carrier density across the channel in linear (a) and logarithmic scale (b).

Lowering down the temperature, the carriers are more confined at the $Si-SiO_2$ interface, since the inversion layer becomes more and more degenerate.

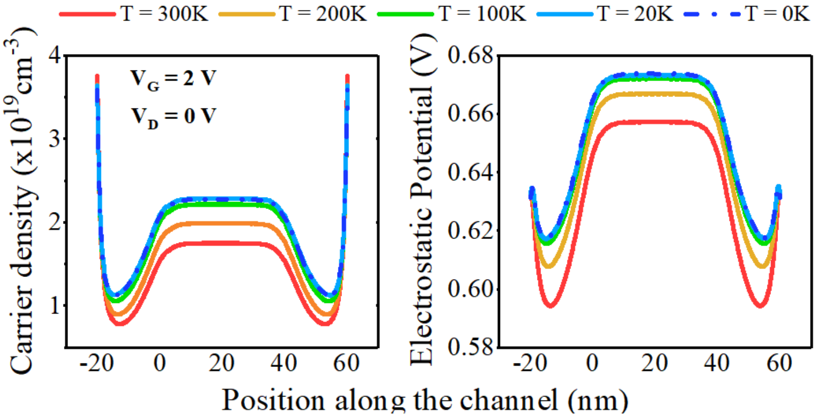

Figure 2.3.3 Carrier density (a) and electrostatic potential (b) along the channel

It is worth to point out that the zero temperature approximation follows the same trend as the curve simulated at $T = 20\ K$ until the middle of the channel, where it suddenly drops to zero. It is possible to plot the carrier density and the electrostatic potential also along the channel (Fig.(2.3.3)). From Fig.(2.3.2) and Fig.(2.3.3) it is possible to conclude that ZTA well reproduces the devices electrostatics at $T \leq 20\ K$. The gate-to-channel capacitance $C_{gc}(V_G)$, calculated with eqs.(2.2.4)-(2.2.5), is plotted in Fig.(2.3.4).(a), at different temperatures.

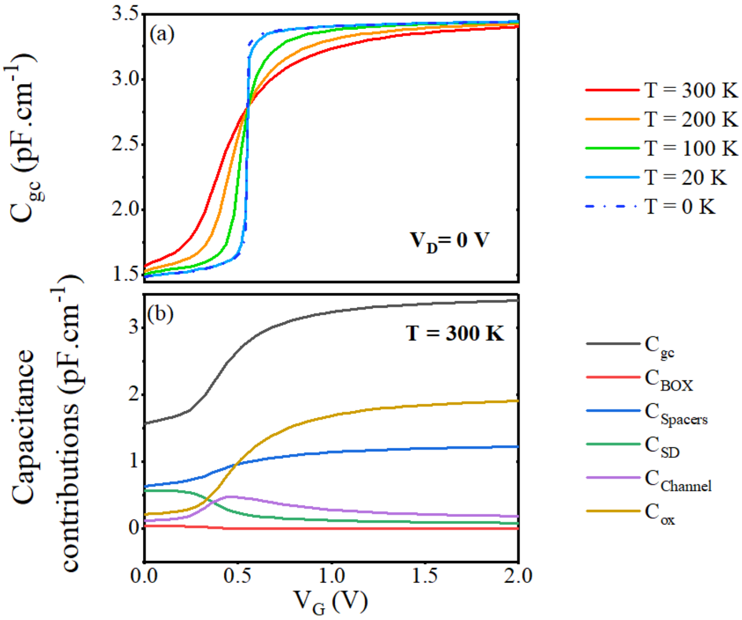

Figure 2.3.4 (a) Simulated gate-to-channel C_{gc} versus V_G for different temperatures. (b) Contributions to the total $C_{gc}(V_G)$.

As observed experimentally [61], the capacitance slope in weak and moderate inversion regions becomes steeper as the temperature is lowered down, due to the temperature evolution of the Fermi-Dirac statistics. Moreover, all the curves cross in a single point, the so-called "zero temperature coefficient (ZTC)" point. Its origin will be discussed in details in the next chapter. In Fig.(2.3.4).(b) are plotted the different contributions to $C_{gc}(V_G)$ at $T = 300\,K$, and they are schematized, for the sake of clarity, in Fig.(2.3.5). Here the spacer region comprehends both the Si_3N_4 and the SiO_2 layers (see Fig.(2.3.1)). The finite value of the gate-to-channel capacitance at $V_G = 0$ is mainly caused by the high values of $C_{Spacers}$ and C_{SD} (Fig.(2.3.3).(b)). Indeed, the spacers are thick and made of Si_3N_4, whose permittivity is $\epsilon_{Si_3N_4} = 7$, and the fringing field through these regions is large. Moreover, the small dimensions of the device enhance their impact (the so-called "short channel effects"). Interestingly, once the inversion layer starts to form, the total capacitance C_{gc} is mainly given by the sum of the gate oxide capacitance C_{ox} and the spacer capacitance $C_{Spacers}$, whereas the channel capacitance decreases, since the channel charges are screened out by the inversion layer. It is worth to point out that the large contribution of $C_{Spacers}$ in strong inversion results again from the short channel effects.

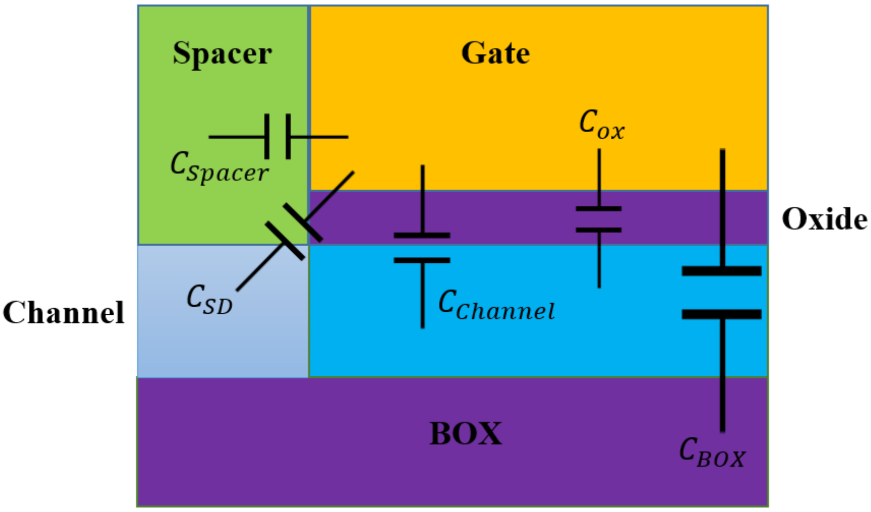

Figure 2.3.5 Schematic of a MOSFET source side with represented the different capacitances contributions

The impact of parasitic capacitances, and short channel effects in general, are mitigated at cryogenic temperature, especially in subthreshold regime (Fig.(2.3.4).(a) and Fig.(2.3.6)), as it will be discussed in the next section.

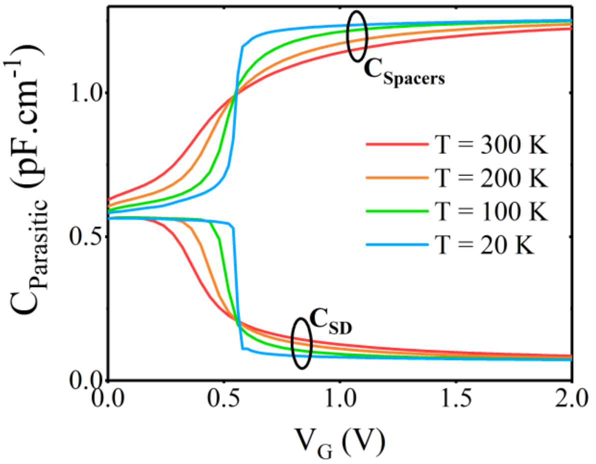

Figure 2.3.6 Parasitic capacitances at different temperatures.

Device Transport

In Fig.(2.3.7) drain current characteristics $I_D(V_G)$ with different mobility laws are reported, both at room and deep cryogenic temperature. In Fig.(2.3.7).(a), a constant low field mobility value equal to $\mu_0 = 100\ \frac{cm^2}{V.s}$ is used, whereas in Fig.(2.3.7).(b) the impact of both vertical and horizontal electric field is considered, according to [62]:

$$\mu = \frac{\mu_0}{1 + \frac{E_y}{E_{cy}} + \frac{E_x}{E_{cx}}} \tag{2.3.1}$$

where E_y and E_x are the electric field along y and x, respectively; E_{cy} and E_{cx} are the critical fields along y and x, respectively.

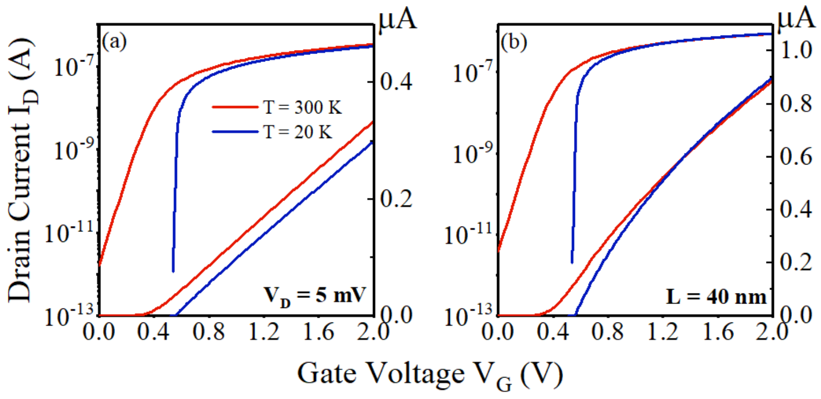

Figure 2.3.7 Simulated $I_D(V_G)$ with constant (a) and field-dependent mobility (b)

The simulations well reproduce the experimental behaviors typically observed at cryogenic temperatures [63]: increase of both the subthreshold swing SS and threshold voltage V_{th}. It is worth pointing out that the saturation of the subthreshold slope is not accounted for here, since no band tails were included in the density of states [64]. Therefore, the simulated SS corresponds to the ideal one. Moreover, I_{ON} does not increase at low temperature, and this is a consequence of the fact that the low field mobility was set to a fixed value, constant in temperature. The low field mobility temperature evolution can be taken in into account through the Mathienssen equation [65]:

$$\mu_0 = \left(\frac{T}{300 \cdot \mu_{ph}} + \frac{300}{T \cdot \mu_C} + \frac{1}{\mu_{nd}} \right)^{-1} \tag{2.3.2}$$

where μ_{ph}, μ_C and μ_{nd} are the phonon, Coulomb and neutral defects scattering mechanisms, respectively. The calibration of these parameters is based on the values found for a different technology in [65], with the sole scope of illustrate that it is possible to reproduce, at least semi-quantitatively, the experimental results. The values chosen reproduce the behavior of a small channel device, whose transport is limited by neutral defects scattering, as known to be for devices whose channel length is smaller than $L_G \leq 100\ nm$ [65] [66] [67] [68]. In the case of LETI qubit devices, as it will be shown, the transport at low temperatures is quite different from that of commercial MOSFETs. In Fig.(2.3.8) are shown the $I_D(V_G)$ characteristics from $T = 300\ K$ down to $T = 20\ K$, in linear regime. As it can be observed, the I_{ON} increases lowering down the temperature, and a ZTC is present, as well as in the $C_{gc}(V_G)$.

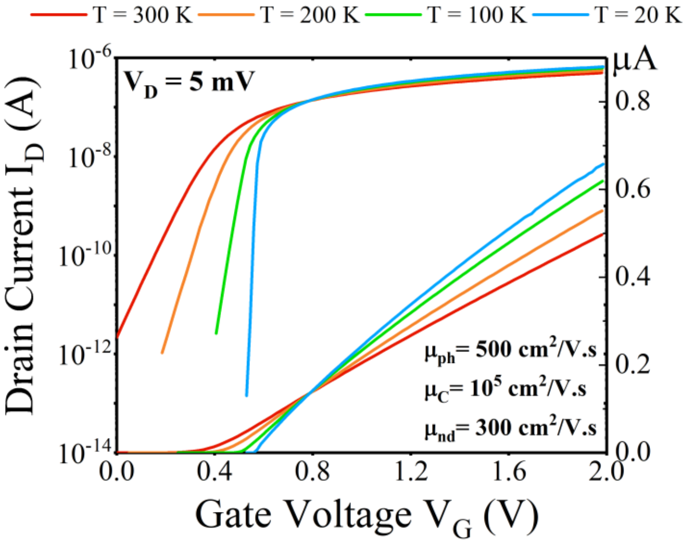

Figure 2.3.8 Simulated $I_D(V_G)$ with temperature dependent mobility.

2.3.1 Short Channel Effects

Short channel effects, previously mentioned, can be investigated more deeply, both at room and at cryogenic temperature. In Fig.(2.3.9) is shown the electrostatic potential for various L_G, in strong inversion regime, at both $T = 300\ K$ and $T = 20\ K$. As can be seen, the temperature does not affect the effects of channel reduction, at least when the channel is fully inverted.

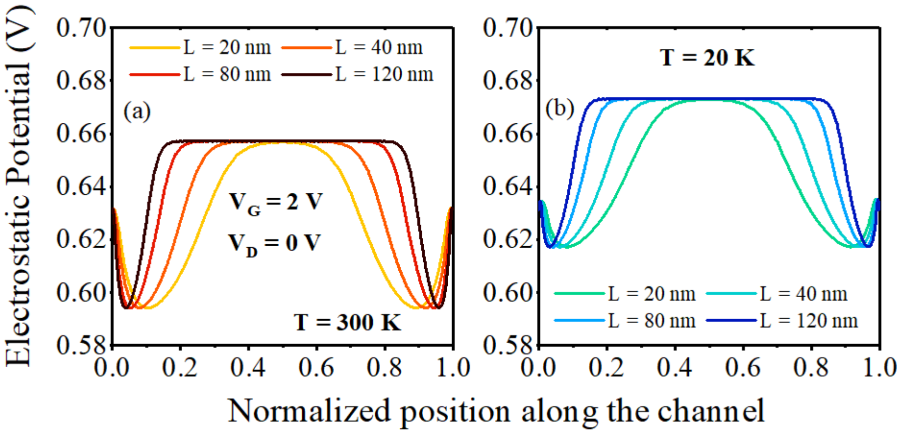

Figure 2.3.9 Electrostatic potential for different channel lengths L_G at (a) $T = 300\ K$ and (b) $T = 20\ K$

Indeed, from Fig.(2.3.10), it is possible to infer that the temperature impact on SCE is dramatic in subthreshold regime. Thanks to the steepness of the subthreshold slope, the off current I_{off} is strongly reduced.

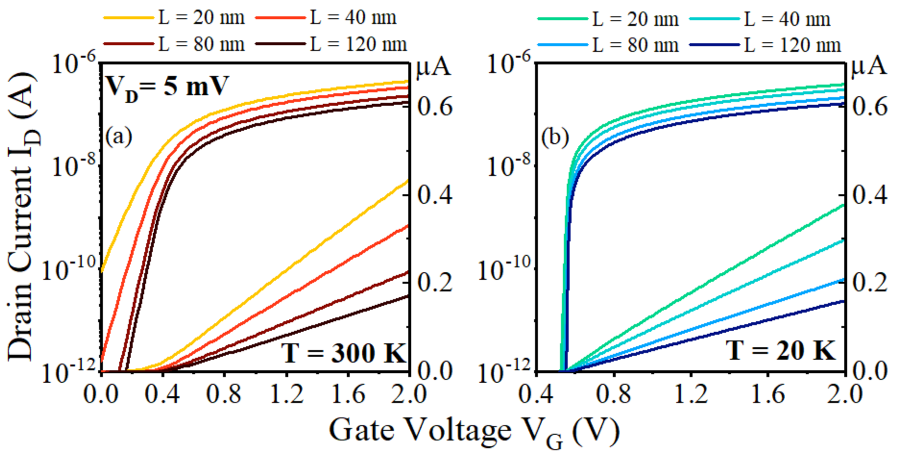

Figure 2.3.10 Simulated $I_D(V_G)$ for different L_G at $T = 300\ K$ (a) and $T = 20\ K$ (b).

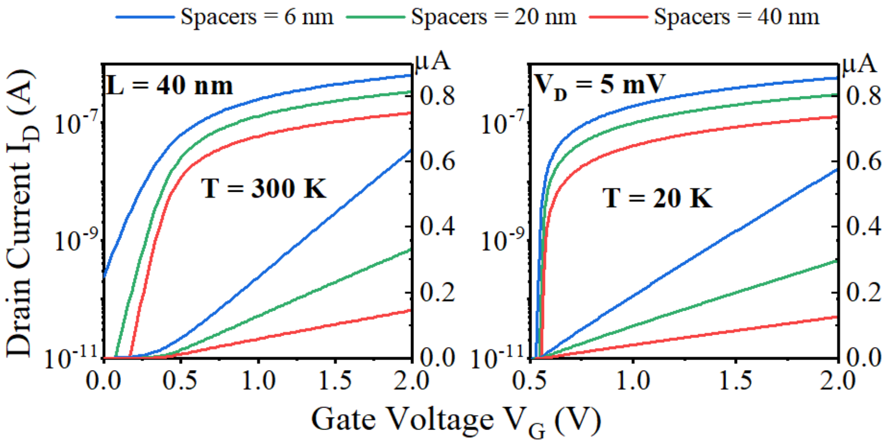

Figure 2.3.11 Simulated $I_D(V_G)$ for different L_{SD} at $T = 300\ K$ and $T = 20\ K$ (b)

It is also possible to explore the influence of the spacers' length and its temperature dependency. As can be seen in Fig.(2.3.11) the device performance above threshold are worsen as the spacers' length increases, because of their higher resistive contribution to the total current, both at low and high temperatures.

2.3.2 High Drain Bias

In the previous paragraph, some $I_D(V_G)$ characteristics in linear regime were presented. We now consider the impact of temperature on transport outside the linear regime.

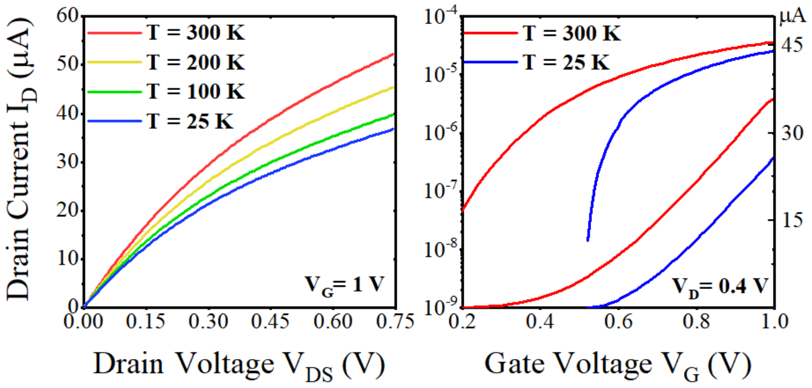

Figure 2.3.12 $I_D(V_D)$ for different T and (b) $I_D(V_G)$ at $V_D = 0.4\ V$

In Fig.(2.3.12).(a) several $I_D(V_D)$ characteristics at various temperatures are plotted. The channel is completely inverted, since $V_G = 1\ V$. Below $V_D = 0.15\ V$ the device is in linear regime, no matter the temperature. Moreover, it should be mentioned that a constant value for μ_0 was used, and this explains the current decrease against temperature. The current increase in saturation is due to SCE, and DIBL in particular [69].

In Fig.(2.3.12).(b) is sketched an example of $I_D(V_G)$ in saturation regime. Both V_{th} and SS increase at cryogenic temperature, as well as for the linear operation case.

2.4 FDSOI MULTI GATE DEVICES

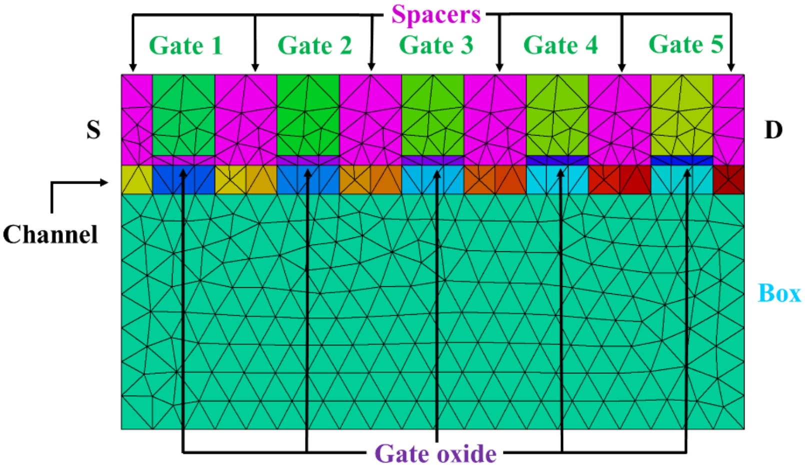

Figure 2.4.1 Example of five-gate MOS based qubit device structure used in simulations.

The model previously described is applied to LETI qubit devices. In Fig.(2.4.1) is sketched an example of multi-gate device used in simulations. It consists of five gates placed in series (5G) and separated by Si_3N_4 spacers, whose length is nominally equal to the gate one. In simulations, in order to improve the mesh, we reduce t_{BOX}, and we increased by the same factor the oxide permittivity, in order to keep the buried oxide capacitance constant. Device dimensions are the same of those reported in Table.(2.3.1). It is worth to point out that the electrostatic considerations for the 5G hold no matter the number of gates placed in series. In the future, we will consider structures from two up to five gates, and the analysis developed here can still be applied without loss on generality. In Fig.(2.4.2) are shown both the carrier density (a) and the electrostatic potential (b) along the channel, in strong inversion and from $T = 300\ K$ to $T = 0\ K$. Despite the thick spacers, the channel, at high V_G, is completely inverted, no matter the operating temperature. For what concerns the carrier density across the channel, the considerations made in the previous paragraphs are still valid, since the cross section of the 5G device is identical to that of a standard FD-SOI.

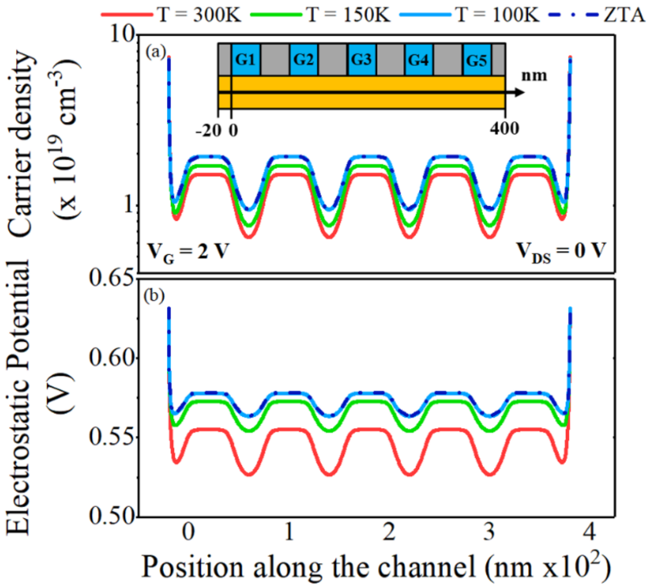

Figure 2.4.2 Carrier density (a) and electrostatic potential (b) along the channel

In Fig.(2.4.3) are reported the $I_D(V_G)$ characteristics in linear regime ($V_D = 5\ mV$) of gates 1 (a) and 3 (b) (see Fig.(2.4.1)), from $T = 300\ K$ to $T = 20\ K$. The simulations were performed emulating the experimental measurement: the potential was fixed on the so called "external gates" to $V_{G,ext} = 2\ V$, while the potential of the active one was swept from $V_G = 0\ V$ to $V_G = 2\ V$. In this way, the current is controlled only by the active gate, i.e. gate 1 in Fig.(2.4.3).(a). Eq.(2.3.2) was used to compute the low field mobility, and eq.(2.3.1) was also implemented to take into account the impact of longitudinal and transversal field. The mobility scattering contributions were calibrated using the experimental values found for this technology [60] [70], as it will be discussed in Chapter 4. In general, gates closer to source and drain suffer a larger impact of neutral defects scattering, and the current increase at low temperature is

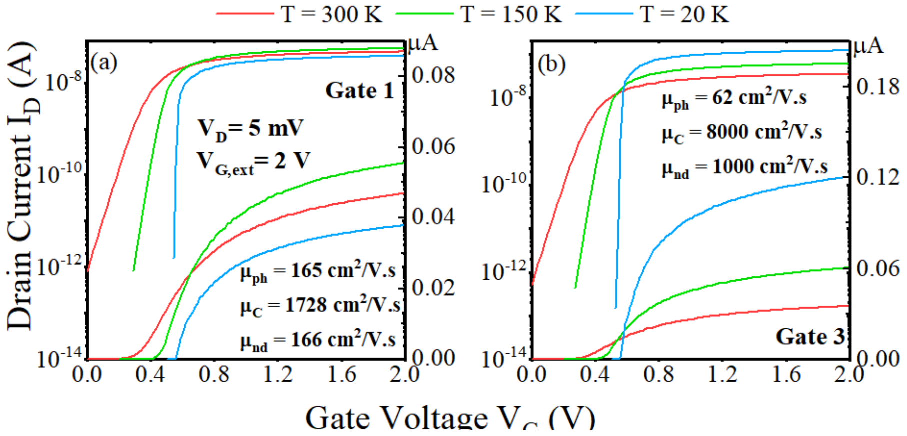

Figure 2.4.3 $I_D(V_G)$ for gate 1 (a) and gate 3, with different mobility scattering parameters

attenuated with respect to the inner gate, where phonons scattering dominates [70]. Indeed, at $T = 20\ K$ and for gate 1, $I_D(V_G)$ is lower than at $T = 300\ K$. Moreover, it is interesting to observe that the ZTC is wiped out in both the outer and inner gate case. This is likely due to the mobility temperature law, which does not vary as $\mu_0 \sim 1/T$, as explained in the next chapter.

2.5 CONCLUSION

In this chapter, we demonstrated the feasibility of performing TCAD simulations of FD-SOI devices down to deep cryogenic temperatures and even at zero Kelvin. In order to do so, an analytical approximation of the Fermi-Dirac integral was introduced, as well as the metallic degenerate statistics valid at zero Kelvin. Initially, a single gate device was considered as test structure. It was shown a general improvement of the device performance at cryogenic temperature, such as an increase of the low field mobility and a global reduction of the short channel effects. Furthermore, the capability of performing simulations at high drain bias voltages was proved. Finally, a more advance qubit structure was simulated, using the method and the equations previously introduced.

In conclusion, we proposed a TCAD model valid at deep cryogenic temperatures, which can be exploited to simulate both commercial FD-SOI devices and qubit-like structures.

Chapter 3: Device Compact Modelling

3.1 INTRODUCTION

Quantum computing promises a boost in computational performances, making it an appealing technology for many research fields. In the last twenty years, many efforts have been devoted in developing solid-state quantum bits, and more recently, the fabrication of spin qubits based on Silicon-On-Insulator (SOI) CMOS platform has been demonstrated [32] [48] [37]. Their interest mainly relies on the possibility of recycling the expertise in transistor manufacturing into large-scale qubit technology. Moreover, silicon quantum bits pave the way to the possibility to integrate the control CMOS – based electronics on the quantum processor itself [18]. In this perspective, the growing interest in device compact models, valid from room to deep cryogenic temperatures, is justified by the increasing complexity of the analog circuits required in quantum computers. Indeed, compared to numerical simulations, analytical models provide easier calculations useful for circuit design and modeling.

This chapter focuses on the compact modeling of FD-SOI at cryogenic temperature. First, in section 3.2, the Lambert function is described, and its effectiveness is demonstrated from room down to deep cryogenic temperatures. In section 3.3, the concept of 2D inversion layer is introduced, together with the charge conservation equation for an FD-SOI. Thanks to these concepts, we propose an explanation of the origin of the zero temperature coefficient (ZTC) point in capacitance curves, developing later on a transport analysis in order to understand which conditions mobility must satisfy to preserve the ZTC also in current. Finally, the density of states band tail is discussed, with particular attention on its impact on the device electrostatics. In section 3.4 is shown how to model 1D quantum confinement in nanowires at cryogenic temperature, illustrating its impact on both drain current and trans-conductance. Section 3.5 is entirely devoted to the subthreshold regime of FD-SOI and to the modeling of physical effects that occur in sub-micrometer devices. The concepts of “resistive networks” and “percolation transport” are introduced and discussed.

3.2 LAMBERT FUNCTION

The Lambert W function was shown to be very efficient in describing $C_{gc}(V_G)$ curves in FDSOI devices [71] [72]. In the following we recalculate the equations shown in [71] and [73]. The gate charge conservation equation in an FD-SOI reads:

$$V_G = V_{fb} + \psi_S + \frac{Q_{inv}}{C_{ox}} + \frac{C_b.(\psi_S - V_b)}{C_{ox}} \qquad (3.2.1)$$

where V_{fb} is the flat-band voltage, ψ_S is the surface potential, Q_{inv} is the channel inversion charge, $C_b = C_{Si}.C_{BOX}/(C_{Si} + C_{BOX})$ is the coupling capacitance, C_{Si} and C_{BOX} are the silicon film and the BOX capacitances, respectively, and V_b is the back-bias potential. In order to simplify the calculations, let us consider the inverse of gate to channel capacitance that, according to eq.(3.2.1), can be written as:

$$\frac{1}{C_{gc}(V_G)} = \frac{\partial V_G}{\partial Q_{inv}} = \frac{\partial V_G}{\partial \psi_S}\frac{\partial \psi_S}{\partial Q_{inv}} = \left(1 + \frac{C_b}{C_{ox}}\right).\frac{1}{\beta Q_{inv}} + \frac{1}{C_{ox}} \qquad (3.2.2)$$

where $\beta = q/k_B T$. We consider here that, according to the Maxwell-Boltzmann statistics, $Q_{inv} \propto \exp(\beta\psi_S)$, and then $\frac{\partial \psi_S}{\partial Q_{inv}} = \frac{1}{\beta . Q_{inv}}$. Furthermore, defining the ideality factor $n = \left(1 + \frac{C_b}{C_{ox}}\right)$, eq.(3.2.2) becomes [71]:

$$C_{gc}(V_G) = \frac{C_{ox}.\frac{q.Q_{inv}}{n.k_B T}}{C_{ox} + \frac{q.Q_{inv}}{n.k_B T}} \qquad (3.2.3)$$

Following [71] and [74], the inversion charge in eq.(3.2.3) can be expressed in terms of ideality factor n, threshold voltage V_{th} and gate oxide capacitance per unit area C_{ox} using the Lambert W function:

$$Q_{inv}(V_G) = C_{ox}.n.\frac{k_B T}{q}.LW\left(e^{q.\frac{V_G - V_{th}}{n.k_B T}}\right) \qquad (3.2.4)$$

that can be well approximated with [73]

$$Q_{inv}(V_G) = C_{ox}n.\frac{k_B T}{q}\ln\left(1 + e^{q.\frac{V_G - V_{th}}{n.k_B T}}\right)\left(1 - \frac{\ln\left(1 + ln\left(1 + e^{q.\frac{V_G - V_{th}}{n.k_B T}}\right)\right)}{2 + \ln\left(1 + e^{q.\frac{V_G - V_{th}}{n.k_B T}}\right)}\right) \qquad (3.2.5)$$

Eqs.(3.2.3) and (3.2.5) can be used to fit the experimental curves, from subthreshold to strong inversion regime, using two fitting parameters, i.e. the ideality factor n and the threshold voltage V_{th}, since C_{ox} can be easily extracted with an alternative method, as described in [71] and as we will clarify in the next chapter.

Lambert W function-based modeling was validated down to deep cryogenic temperatures [75], as further confirmed in Fig.(3.2.1), where it was used to fit $Q_i(V_G)$ (Fig.(3.2.1).(a),(b)) and $C_{gc}(V_G)$ (Fig.(3.2.1).(c)) curves of a large n-type FDSOI device $(W = 20\,\mu m, L = 3\,\mu m,\ t_{ox} = 6\,nm, t_{Si} = 9.8\,nm, t_{BOX} = 145\,nm)$ from $T = 300\,K$ down to $T = 4.2\,K$. Concerning the inversion charge, it increases exponentially below threshold voltage, and its slope is steeper at cryogenic temperatures (Fig.(3.2.1).(b)), whereas above threshold is almost independent on T, and it increases linearly with V_G, according to $Q_{inv} \approx C_{ox}(V_G - V_{th})$ [56]. The C_{gc} slope in weak and moderate inversion becomes steeper as the temperature is lowered down. Furthermore, it is worth noticing that the ideality factor n explodes at deep cryogenic temperatures (Fig.(3.2.1).(d)). Since $n = (C_{ox} + C_b + C_{it})/C_{ox}$, where

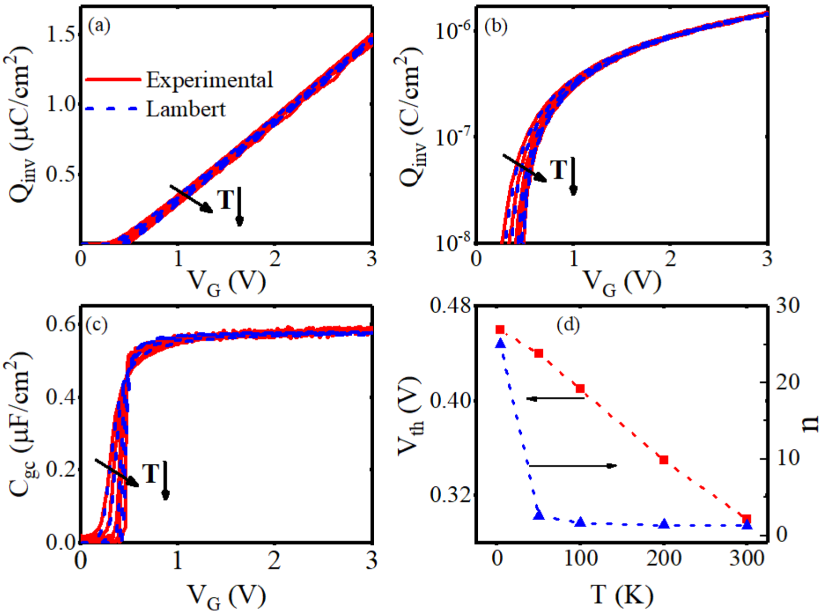

Figure 3.2.1 Experimental (red straight line) and modeled (blue dotted line) inversion charge $Q_i(V_G)$ in linear (a) and logarithmic (b) scale for various temperatures $T(K) = 300, 200, 100, 50, 4.2$. Experimental (red straight line) and modeled (blue dotted line) $C_{gc}(V_G)$ (c). V_{th} and n as function of temperature (d).

$C_{it} = q.N_{it}$ is the interface trap capacitance, in order to justify a value as high as $n = 25$ at $T = 4.2\,K$, $N_{it} \approx 9.10^{13}\,cm^{-2}$, that is close to the number of atomic sites in silicon [76] [77]. This is due, as we will explain in the following, to both the inadequacy of Maxwell-Boltzmann statistics at cryogenic temperatures and the localized states band tails in the density of states. Because of this, the ideality factor at cryogenic temperatures is not physically meaningful anymore. Finally, the threshold voltage V_{th} increases quasi linearly with temperature, as reported in literature, both for FD-SOI [63] [75] [78] [79] and bulk technologies [80] [81] [82].

In linear regime, the channel of a MOSFET behaves like a resistor, whose conductance is given by

$$G_{ch}(V_G) = \frac{W}{L}.Q_{inv}(V_G).\mu_{eff} \tag{3.2.6}$$

In this case, instead of using the conventional formulation with gate voltage overdrive [83], it is preferable expressing the effective mobility μ_{eff} in terms of Q_{inv}:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1.\frac{Q_{inv}}{C_{ox}} + \theta_2 \frac{Q_{inv}}{C_{ox}}^2} \tag{3.2.7}$$

since the LW function based inversion charge expression of eq.(3.2.4) is applicable from weak to strong inversion. $\theta_1 = \theta_{10} + R_{SD}\beta$ and θ_2 are the first and second order mobility attenuation coefficients, θ_{10} being the intrinsic first order mobility attenuation factor, R_{SD} being the source/drain access resistance and $\beta = \frac{W}{L}.C_{ox}\mu_0$ the current gain factor. The drain current is simply given by $I_D(V_G) = G_{ch}(V_G).V_D$.

Therefore, using five parameters, i.e. $V_{th}, n, \mu_0, \theta_1, \theta_2$, the Lambert W function enables to fit both $I_D(V_G)$ (Fig.3.2.2.(a)) and $g_m(V_G)$ (Fig.3.2.2.(b)), from subthreshold to strong inversion regime, and from $T = 300\ K$ to $T = 4.2\ K$. The curves plotted in Fig.(3.2.2) come from the characterization of the same device as the one described before.

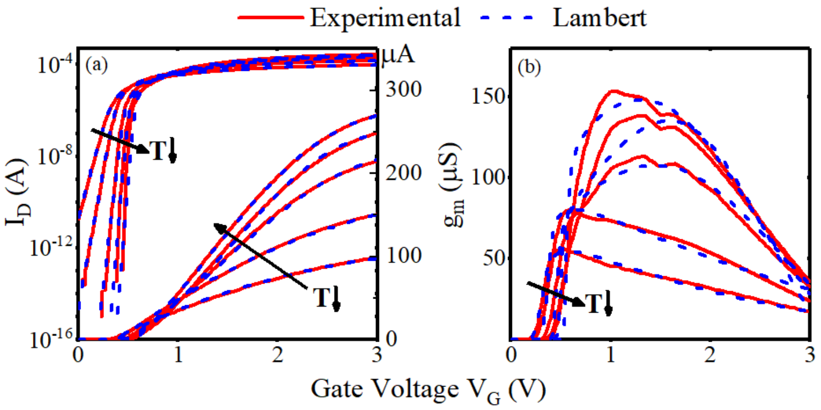

Figure 3.2.2 (a) Experimental (red straight line) and modeled (blue dotted line) drain current $I_D(V_G)$ in linear and logarithmic scale for various temperatures $T(K) = 300, 200, 100, 50, 4.2$. (b) Experimental (red straight line) and modeled (blue dotted line) $g_m(V_G)$

Details about the values of the extracted parameters will be provided in the next chapter, dedicated to the devices' characterization. However, it is worth to stress that the Lambert function is based on the Boltzmann statistics, which is valid until the inversion layer does not degenerate. At cryogenic temperatures, the Fermi-Dirac statistics must be taken into account in calculations. Whereas LW function is a reliable extraction method in strong inversion regime, since the Fermi level goes over the conduction (valence) band edge and $Q_{inv} \approx C_{ox}(V_G - V_{th})$, the parameter extracted below threshold, i.e. the ideality factor, does not have any physical meaning at cryogenic temperature, and it is used just as a fitting parameter. This is due not only to the difference between Maxwell-Boltzmann and Fermi-Dirac statistics, but also to the presence of exponential band tails in the density of states [64].

3.3 FDSOI MODELLING

In Chapter 2, the limits of the Maxwell-Boltzmann statistics as the temperature is lowered down have been illustrated. Moreover, as quickly mentioned at the end of the previous section, device physics at cryogenic temperature comprehends other effects and features, like the subthreshold slope saturation and zero temperature coefficient. In this section, we will introduce some compact models which include some of the main aspects of cryogenic FDSOI physics.

3.3.1 2D Systems and the Fermi-Dirac distribution

In order to describe properly the charge density in the inversion layer at cryogenic temperatures, Fermi-Dirac statistics must be considered, that we recall for the sake of clarity:

$$n(E_F,T) = \int_{-\infty}^{\infty} f(E,E_F,T).\,N(E)\,dE \qquad (3.3.1)$$

Moreover, due to quantum confinement at $Si - SiO_2$ interface, that is more effective at cryogenic temperature [84], the inversion layer can be depicted by a single 2D sub-band [58] [85] and the bottom of the conduction band is set to $E_C = 0$. Eq.(3.3.1) becomes [58] [86]:

$$n(E_F,T) = k_B T.\,A_{2D}.\ln\left(1 + e^{\frac{E_F}{k_B T}}\right) \qquad (3.3.2)$$

where $A_{2D} = \frac{g.m_d^*}{\pi\hbar}$ is the 2D density of states, g is the sub-band degeneracy factor, m_d^* is the DOS electron mass and $\hbar$ is the reduced Planck constant.

By solving the gate charge conservation equation (eq.(3.2.1)), it is possible to obtain the surface potential $\psi_S(V_G, V_D, V_b, T)$ for given front and back biases and temperature. From ψ_S, one can calculate the Fermi level (in eV) as (Appendix A):

$$E_F(V_G,V_b,T) = q.\,(\psi_S(V_G,V_b,T) - V_0) \qquad (3.3.3)$$

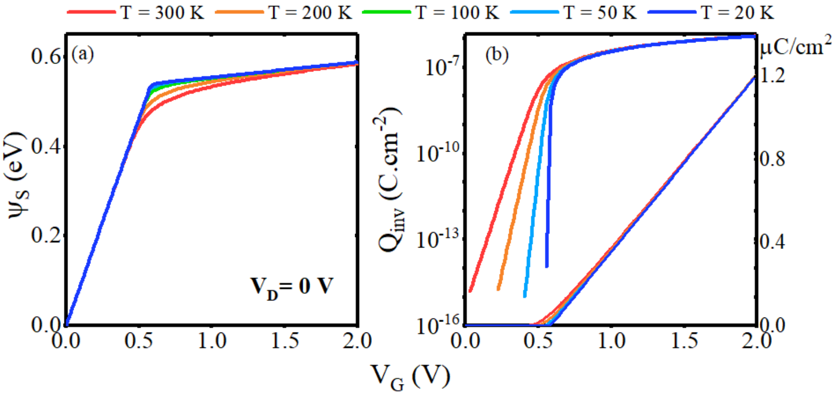

Figure 3.3.1 Surface potential ψ_S (a) and inversion charge Q_{inv} (b) versus V_G for different temperatures.

where V_0 is a reference potential depending on the channel doping level. $V_0 = E_g/2$ for undoped film, E_g being the silicon gap. Once the Fermi level is known, one can find the inversion charge density using eq.(3.3.2). In Fig.(3.3.1).(a) is reported the surface potential ψ_s calculated by solving eq.(3.2.1). It increases linearly with V_G, no matter the temperature, before saturating to a fairly constant value once the channel is inverted [56] [87]. Lowering down T, the transition from subthreshold to strong inversion becomes steeper and ψ_S slightly increases in strong inversion. It is worth to point out that this is the same behaviour followed by the Fermi level (eq.(3.3.3)), meaning that it increases at low temperatures as well. Concerning the inversion charge, curves shown in Fig.(3.3.1) are in agreement with those reported in Fig.(3.2.1).

3.3.2 The Zero Temperature Coefficient

From Fig.(3.2.1).(c) it is possible to see that C_{gc} curves crosses in a single point. This point, called "zero temperature coefficient (ZTC)" point, has been widely observed in literature for different technologies, both for n- and p-type devices, and in both capacitance and drain current characteristics [61] [63] [75] [88] [89] [90] [91]. Previous studies and modelling of the ZTC focused on the drain current characteristics, and its existence was attributed to a compensation effect between carrier mobility and threshold voltage temperature variation [92]. However, its origin cannot be only justified by transport considerations, but it should stem from the channel gate charge control. Indeed, from eq.(3.2.1):

$$C_{gc}(V_G) = \frac{dQ_{inv}}{dV_G} = \frac{C_{ox}.C_{inv}}{C_{ox} + C_b + C_{inv}} \tag{3.3.4}$$

with C_{inv} being the inversion capacitance deduced from eq.(3.3.2) as,

$$C_{inv} = \frac{dQ_{inv}}{d\psi_S} = \frac{dQ_{inv}}{dE_F} = C_q.f(E_F, T) \tag{3.3.5}$$

where $C_q = q.A_{2D}$ is the quantum capacitance.

Inspection of eq.(3.3.4) implies that a capacitance value constant in temperature requires C_{inv} and, ultimately, $f(E_F, T)$ to be temperature independent. This is verified if $\frac{E_F}{k_B.T} = \lambda$, where λ is a constant. Therefore, the existence of the ZTC point could be interpreted by the compensation between the Fermi level increase and the temperature decrease. In this case, eq.(3.3.3) reads

$$q.\psi_S(V_G, V_b, T) = q.V_0 + \lambda.k_BT \tag{3.3.6}$$

Thus, one can express the gate voltage value at which the ZTC occurs using eq.(3.1.1) as:

$$V_{G,ZTC}(C,T) = V_{FB} + \lambda.k_BT + V_0 + \frac{Q_{inv}(\lambda.k_BT/q,T)}{C_{ox}} + \frac{C_b.(\lambda.k_BT/q + V_0 - V_b)}{C_{ox}} \quad (3.3.7)$$

The existence of the ZTC point implies $\partial V_{G,ZTC}/\partial T = 0$, yielding from eq.(3.3.7),

$$\lambda.(C_b + C_{ox}) + C_q.\ln\left(1 + e^{\lambda}\right) = 0 \quad (3.3.8)$$

Once the value of the constant λ is known by numerical resolution of eq.(3.3.8), it is easy to calculate $V_{G,ZTC}$ using eq.(3.3.7).

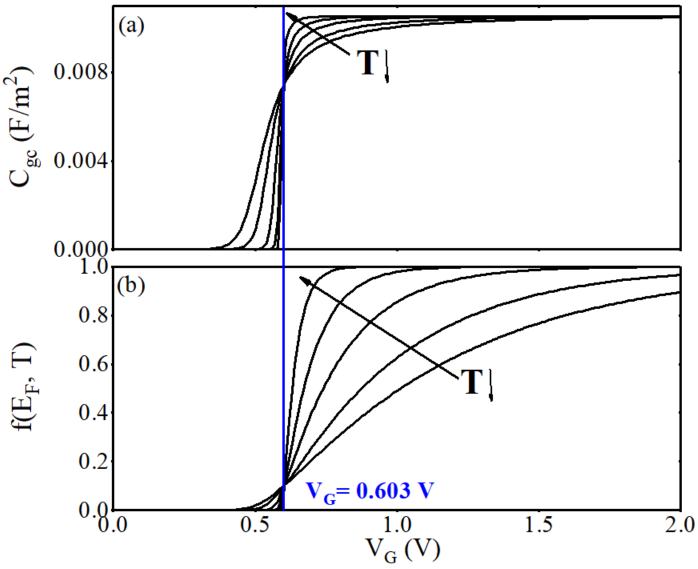

Figure 3.3.2 (a) Modeled gate to channel capacitance and (b) Fermi-Dirac function from $T = 300\ K$ to $T = 20\ K$. In this example: $t_{Si} = 7\ nm, t_{ox} = 3.2\ nm, t_{BOX} = 25\ nm$ and $V_{fb} = 0$

In Fig.(3.3.2) are shown Fermi-Dirac function $f(E_F,T)$ and gate-to-channel capacitance $C_{gc}(V_G,T)$ versus V_G curves calculated using eqs.(3.3.2)-(3.3.5). As can be seen, both C_{gc} and $f(E_F,T)$ cross at the same V_G value for different temperatures, validating the above analysis and providing an insight on the origin of the ZTC point in the C_{gc} characteristics. Indeed, it clearly appears that the ZTC point corresponds to a constant sub-band occupation probability $f(E_F,T)$. Solving eq.(3.3.8), it is possible to find this critical value for the occupation probability, which is here $f(\lambda.k_BT,T) = 0.101$. Finally, it is worth to point out that the reason why no ZTC point is observed in the Q_{inv} curves lies in the temperature linear factor in the inversion charge (see eq.(3.3.2)), which is removed by taking its derivative with respect to E_F.

Effects of Transport

Exploring the ZTC in $I_D(V_G)$ characteristics requires taking into account the temperature dependence of carriers' mobility. We will limit the analysis to the linear regime. Moreover, for simplicity, no mobility attenuation laws with respect to vertical electric are considered. We recall here for convenience eq.(2.3.2) describing the mobility temperature dependence [65]:

$$\mu_0 = \left(\frac{T}{300.\mu_{ph}} + \frac{300}{T.\mu_C} + \frac{1}{\mu_{nd}}\right)^{-1} \tag{3.3.9}$$

In long channel devices with thick gate oxide, the mobility is phonon scattering driven, meaning that $\mu_0 \approx 300.\frac{\mu_{ph}}{T}$. Reducing the gate oxide thickness, the $1/T$ trend drifts away, due to Coulomb scattering [65].

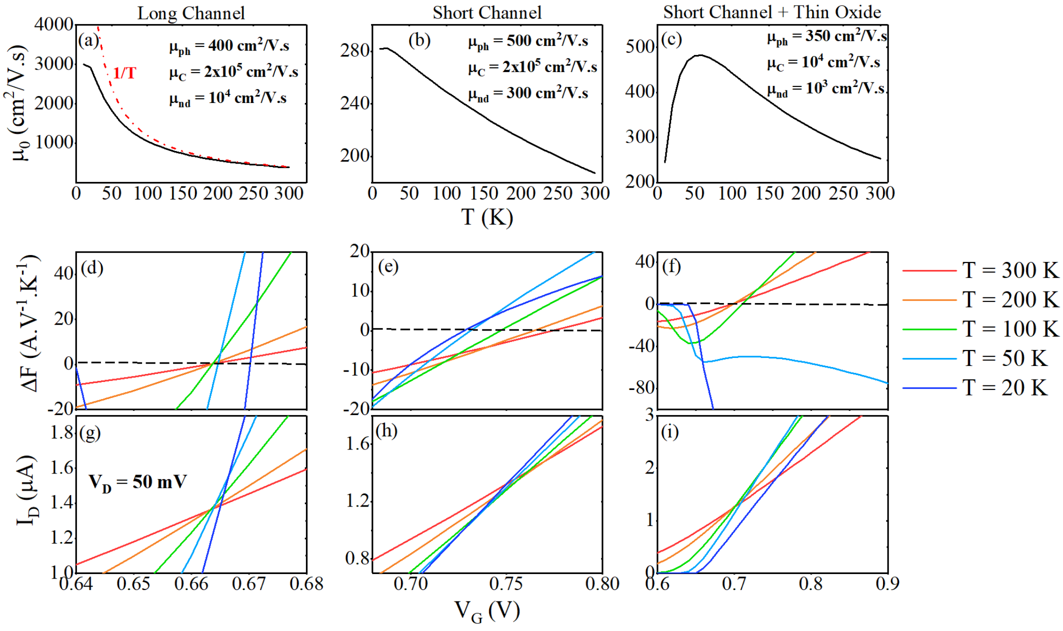

Figure 3.3.3 . $\mu_0, \Delta F, I_D(V_G)$ for long (a)-(d)-(g), short (b)-(e)-(h) and short and thin gate oxide (c)-(f)-(i) devices. In this example: $t_{Si} = 7\,nm, t_{ox} = 3.2\,nm, t_{BOX} = 25\,nm,\ \mu_{300} = 1000\,\frac{cm^2}{V.s}, W = 1\,\mu m, L = 1\mu m.$

Shortening the channel length, instead, brings an increase of the neutral defects scattering. Using Eq.(3.3.9), it is possible to express the device ohmic conductance as:

$$G_d = \frac{W}{L}\mu_0 Q_i =$$

$$= \frac{W}{L}.C_q.\left(\frac{T}{300.\mu_{ph}} + \frac{300}{T.\mu_C} + \frac{1}{\mu_{nd}}\right)^{-1} k_B T.\ln\left(1 + e^{\frac{E_F}{k_B T}}\right) \quad (3.3.10)$$

where W and L are the channel width and length, respectively. In order to preserve the ZTC, eq.(3.3.10) must satisfy the condition,

$$\frac{\partial G_d}{\partial T} = 0 \tag{3.3.11}$$

which implies,

$$\Delta F = -\frac{\mu_0(T).T}{1+e^{-\frac{E_F}{k_B T}}}.\left(\left(\frac{\partial E_F}{\partial T}.k_B T - E_F.k_B\right).\frac{1}{(k_B T)^2}\right)..$$

$$..-\left(\frac{d\mu_0(T)}{dT}.T+\mu_0(T)\right).\ln\left(1+e^{\frac{E_F}{k_B T}}\right) = 0 \tag{3.3.12}$$

where $\Delta F \triangleq \partial G_d/\partial T$. Eq.(3.3.12) was solved for different mobility trends, representative of the channel and gate oxide dimensions. The values of μ_{ph}, μ_C *and* μ_{nd} used here are taken from [65], and are relevant to 14nm FD-SOI technology of STMicroelectronics. In Fig.(3.3.3).(a) is shown the long channel case, where the main scattering process is governed by phonons, and the mobility goes as $\mu_0 \sim 1/T$ until $T = 100\ K$; in Fig.(3.3.3).(b),(c) are reported two examples of mobility in short channel devices, with thick and thin oxide, respectively. The small transport improvement at cryogenic temperatures is due to the presence of neutral defects in the channel (Fig.(3.3.3).(b)), whereas the steep mobility decrease at $T < 50\ K$ must be attributed to Coulomb scattering (Fig.(3.3.3).(c)). As can be seen in Fig.(3.3.3).(d)-(f), eq. (3.3.12) is never verified, and no ZTC point can be found in the current characteristics (Fig.(3.3.3).(g)-(i)), calculated as

$$I_D(V_G) = G_d.\frac{V_D}{1+R_{SD}.G_d} \tag{3.3.13}$$

where R_{SD} are the source/drain access resistances, here fixed at $R_{SD} = 1\ k\Omega$. With further examination of eq. (3.3.12) and Fig.(3.3.3), it can be observed that, if phonon and neutral defects scattering prevail, it is still possible identifying a region where $I_D(V_G)$ slightly changes with temperature. If μ_0 decreases with T, instead, the current drifts away at temperatures where Coulomb scattering is effective. Furthermore, from Fig.(3.3.3).(a),(d), eq. (3.3.12) seems to be verified until the mobility follows the ideal long channel behaviour, i.e. $\mu_0 \sim 1/T$. In order to investigate better which conditions eq. (3.3.12) is satisfied for, eq. (3.3.9) is simplified to

$$\mu_0 = \mu_{300}\left(\frac{300}{T}\right)^{\gamma} \tag{3.3.14}$$

where μ_{300} is the mobility at room temperature and γ is a coefficient to take into account the influence of other scattering mechanisms besides phonons. It should be noted that Eq. (3.3.14) is not equivalent to Eq. (3.3.9), and does not provide any information about the scattering processes involved in the transport. On the other side, it allows to analyze easily which conditions transport must fulfill in order to have a ZTC point. It is worth to stress that, from the previous analysis, Coulomb and neutral defects scattering do not preserve the ZTC point found in capacitance curves. For this reason, the attention is focused on phonon scattering-limited processes, and their deviations from the ideal case, i.e. $\gamma = 1$.

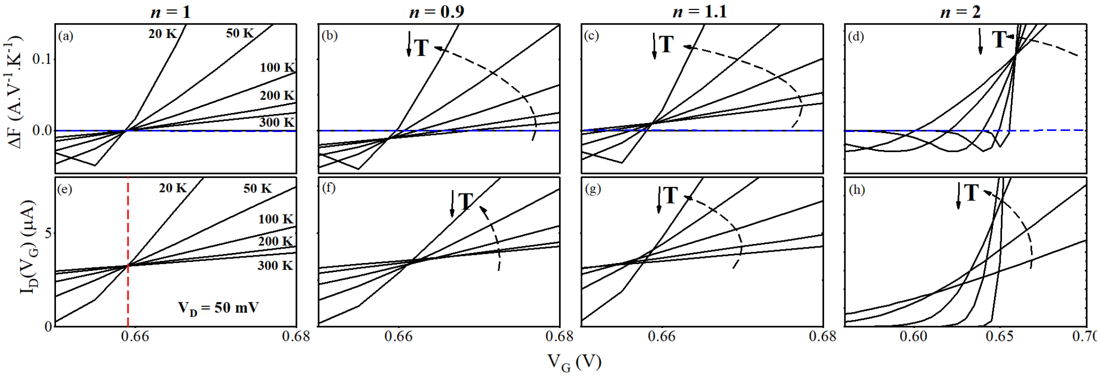

Figure 3.3.4 ΔF and $I_D(V_G)$ for $n = 1$ (a)-(e), $n = 0.9$ (b)-(f), $n = 1.1$ (c)-(g) and $n = 2$ (d)-(h). In this example: $t_{Si} = 7\,nm, t_{ox} = 3.2\,nm, t_{BOX} = 25\,nm,\ \mu_{300} = 1000\,\frac{cm^2}{V.s}, W = 1\,\mu m, L = 1\mu m.$

Replacing eq.(3.3.9) with eq.(3.3.14), eqs.(3.3.10) and (3.3.12) read, respectively

$$G_d = \frac{W}{L}.C_q.\mu_{300}\left(\frac{300}{T}\right)^{\gamma} k_B T.ln\left(1 + e^{\frac{E_F}{k_B T}}\right) \tag{3.3.16}$$

$$\Delta F = -\frac{T}{1 + e^{-\frac{E_F}{k_B T}}}.\left(\left(\frac{\partial E_F}{\partial T}.k_B T - E_F.k_B\right).\frac{1}{(k_B T)^2}\right)..$$
$$..-(1-\gamma).\ln\left(1 + e^{\frac{E_F}{k_B T}}\right) = 0 \tag{3.3.17}$$

As shown in Fig.(3.3.4).(a), eq. (3.3.17) is only verified if $\gamma = 1$. Indeed, in this case, G_d of eq.(3.3.16) depends on temperature only through the exponential term, since the temperature linear factor in the inversion charge is balanced by the mobility temperature trend. In this situation, the ZTC point in the $I_D(V_G)$ curves has the same origin and interpretation as for the capacitance characteristics. As soon as μ_0 departs from $1/T$ law, eq.(3.3.17) is not verified anymore (Fig.(3.3.4).(b),(d)).

In Fig.(3.3.4).(f)-(h) are plotted the corresponding $I_D(V_G)$ characteristics from $T = 300\ K$ to $T = 20\ K$ for $\gamma \neq 1$, confirming that the ZTC is wiped out. However, for γ close to one, $I_D(V_G)$ characteristics have small dispersion in temperature (Fig.(3.3.4).(f)-(g)), whereas they visibly spread as γ departs from one (Fig.(3.3.4).(h)). It is worth pointing out that $V_{G,ZTC}$, when $\gamma = 1$, is higher in current than in capacitance because C_{gc} is normally measured at $V_D = 0$ (see Fig.(3.3.2).(a) and Fig.(3.3.4).(e)).

Finally, it is useful to study the behaviour of the trans-conductance $g_m = \frac{dI_D}{dV_G}$. For a constant mobility in V_G, we have:

$$g_m = \frac{W}{L}\mu_0\frac{dQ_i}{dV_G}V_D = \frac{W}{L}\mu_0.C_{gc}.V_D \qquad (3.3.18)$$

Therefore, when μ_0 varies as $1/T$ due to phonon scattering, it is easy to see that $g_m \propto 1/T$, and no ZTC point can exist. Instead, when the mobility μ_0 is constant in temperature due to e.g. neutral scattering domination, g_m should exhibit a ZTC point as in the C_{gc} case. In experiments, this condition is never verified, since μ_0 slightly increases at cryogenic temperatures, even in short devices. In Fig.(3.3.5) are reported both $I_D(V_G)$ and $g_m(V_G)$ for a more realistic case ($n = 1/5$) which accounts for the impact of neutral defects scattering. Even if there is not a ZTC point, it is possible to identify a region where current and trans-conductance characteristics slightly change in temperature.

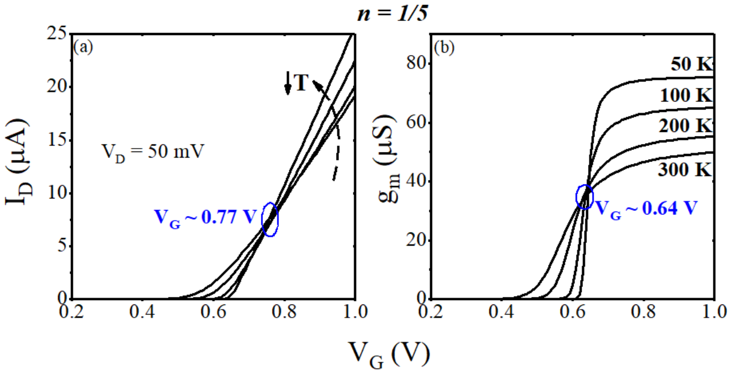

Figure 3.3.5 . $I_D(V_G)$ (a) and $g_m(V_G)$ (b) characteristics from $T = 300\ K$ to $T = 50\ K$.

The corresponding gate voltages are different, and the g_m one is lower, as experimentally observed [75]. Furthermore, according to Eq. (3.3.18), if μ_0 would be constant in temperature, the ZTC points in $g_m(V_G)$ and in C_{gc} should be the same, within V_D.

3.3.3 The Band Tails

The density of states in the surface inversion layer at $Si - SiO_2$ interface manifests tails of localized states in the proximity of the conduction (valence) band edge [93]. These are likely due to the presence of potential-fluctuations-induced disorder [93] [94]. Indeed, “fixed” charges are randomly distributed at the $Si - SiO_2$ interface, causing potential variations. At cryogenic temperatures, carriers do not have enough thermal energy to leave potential valleys created by these random charges, and the macroscopic effect of the fluctuations is to smear the sharp band edges into tails of localized states [93].

Recently, band tails have been proposed as explanation of the subthreshold slope saturation in MOSFETs [64] [76] [95]. Indeed, according to the Boltzmann statistics, $SS = n.\frac{k_B T}{q}$. Experimentally, the subthreshold slope follows the Boltzmann limit down to a critical temperature, below which it saturates to a constant value. It is now clear why the ideality factor explodes at deep cryogenic temperature: in order to keep SS constant, it must compensate the temperature decrease. A detailed discussion of the band tail impact on the subthreshold slope and an easy way to extract the critical temperature can be found in [64]. Here, we would like to focus on its effect on the device electrostatics, especially on the gate-to-channel capacitance.

The density of states of the inversion layer with exponential band tails can be written as [64]:

$$N(E, \Delta E) = \frac{A_{2D}}{1 + \exp\left(-\frac{E}{\Delta E}\right)} \tag{3.3.19}$$

where $\Delta E = k_B T_S$ is the band tail extension and T_S is the critical temperature. The carrier density is given by eq.(3.3.1). Once calculated the surface potential ψ_S and the Fermi level E_F with eq.(3.2.1) and eq.(3.3.3), respectively, it is possible to obtain the gate-to-channel capacitance as $C_{gc}(V_G) = \frac{dQ_{inv}}{dV_G}$. In Fig.(3.3.6) are reported the fits of experimental Q_{inv} and C_{gc} both neglecting (Fig.(3.3.6).(a),(b)) and including (Fig.(3.3.6).(c),(d)) band tails. The experimental data are the same shown in Fig.(3.2.1) for a large and long FD-SOI device.

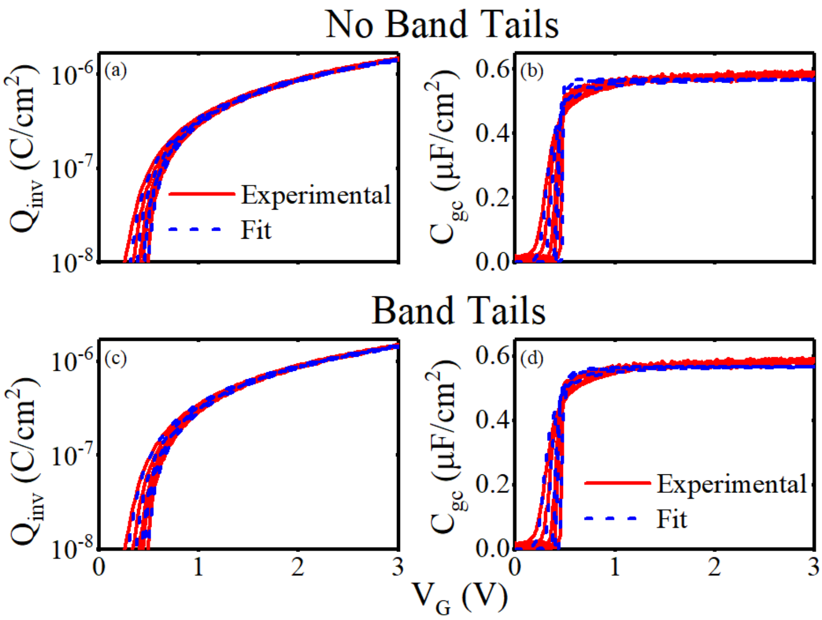

Figure 3.3.6 Experimental (red straight line) and modeled (blue dotted line) inversion charge $Q_i(V_G)$ without (a) and with (c) band tails for various temperatures $T(K) = 300, 200, 100, 50, 4.2$. Experimental (red straight line) and modeled (blue dotted line) $C_{gc}(V_G)$ without (b) and with band tails (d).

It is worth to underline that the fit relies on two parameters, in case band tails are taken into account: flat band voltage V_{fb} (Fig.(3.3.7).(a)) and critical temperature T_S. In the present case, $T_S = 50\ K$, meaning that the tails extension is $\Delta E \approx 4\ meV$. This value is consistent with 28 nm FD-SOI technology [64] [95]. In case band tails are not considered, there is only one fitting parameter, i.e. V_{fb}. Furthermore, no interface traps N_{it} were added in the models in order to fit the experimental values.

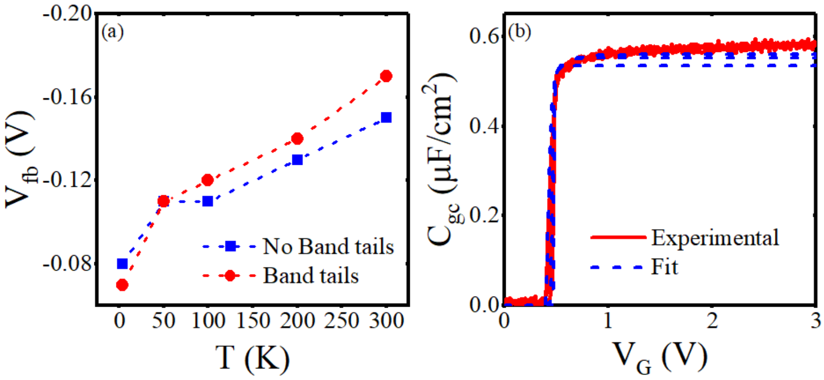

Figure 3.3.7 (a) Values of flat-band voltage with and without band tails. (b) Experimental (red straight line) and fit (blue dotted line) of C_{gc} curves without band tails for various temperatures $T(K) = 50, 20K, 4.2$. Interface traps values used: $N_{it}(50\ K) = 2.10^{12}$, $N_{it}(20\ K) = 4.10^{12}$, $N_{it}(4.2\ K) = 1.10^{13}$

The main difference in the models is in the transition between weak to strong inversion: the inclusion of the band tails smooths the sharp step-like edge of C_{gc} at deep cryogenic temperatures. Indeed, in Fig.(3.3.6).(b), C_{gc} is overestimated while approaching the strong inversion region, where $C_{gc} \approx C_{ox}$. Including interface traps, that is, adding a capacitance in series to C_{ox}, allows to recover the experimental behavior, as shown in Fig.(3.3.7).(b). Here, only curves at $T \leq 50\ K$ are considered, since band tails are relevant only at temperatures $T \leq T_S = 50\ K$. Indeed, at these temperatures, the Fermi level sweeps both interface and localized states belonging to the band tails [96]. Therefore, the need of considering additional traps at cryogenic temperatures to fit properly the experimental curves comes from the missing integration of band tails in the model. Analogous considerations are valid also for others interface traps extraction techniques [64] [96].

3.4 ONE DIMENSIONAL CONFINEMENT IN FDSOI NANOWIRES

Several theoretical studies [97] [98], supported by experimental evidences [99] [100], reveal the presence, at cryogenic temperatures, of quantum 1D confinement related features in both the electrostatic and the transport characteristics of 3D FD-SOI transistors [101], such as silicon nanowires (Si NW) and Triple-gate devices.

We electrically characterized multi-gate MOS based qubit devices (Chapter 1 and Fig.(3.4.1)) down to cryogenic temperatures, where they exhibit oscillatory behavior in both the current and trans-conductance. Afterwards, considering a 1D density of states in the calculation of channel inversion charge, we introduce a compact model able to reproduce the experimental behavior, in both linear and saturation regime.

Device details

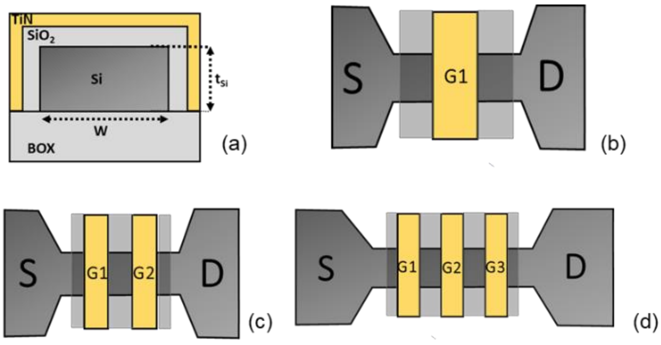

Figure 3.4.1 Cross section (a) and top view of 1G11 (b), 2G11 (c) and 3G11 (d) devices.

The p-type multi-gate devices (1G11, 2G11 and 3G11) are sketched in Fig.(3.4.1). The non-intentionally doped silicon film thickness is $t_{Si} = 17.9\, nm$, defining the NW height, and covered by a 6 nm thick SiO_2 oxide and by a 5 nm TiN metal gate (Fig.(3.4.1).(a)). Si_3N_4 spacers, whose length is nominally equal to the gate one, i.e. $L_G = 50\, nm$, separate the gates. The top channel width is $W_G = 75\, nm$. The devices have been tested from room temperature down to $T = 10\, K$. Static measurements of the drain current both in linear ($|V_{DS}| = 50\, mV$) and saturation ($|V_{DS}| = 0.5\, V$) regime were performed sweeping the voltage on one gate (*active gate*), while keeping the other gates (*external gates*) at a fixed potential, namely $V_{G,ext} = -2V$. In such a way, the current was controlled by the active gate. In the case of the single gate device shown in Fig.(3.4.1).(b), it was characterized as a classical transistor, using the same V_{DS} values.

Experimental results

In Fig.(3.4.2).(a) are reported the drain current characteristics $I_D(V_G)$ of the 3G device from $T = 300\, K$ to $T = 10\, K$, in linear regime.

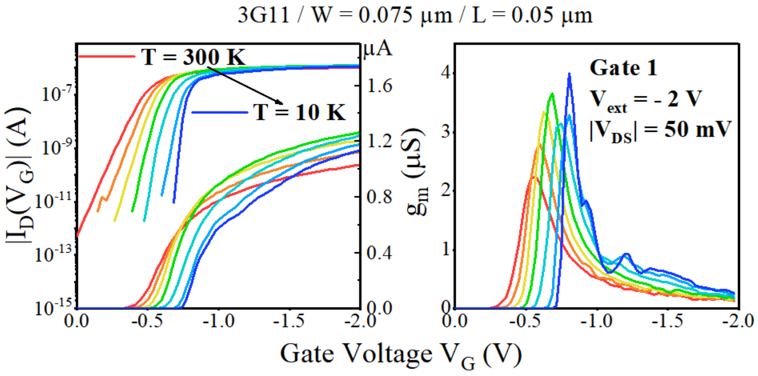

Figure 3.4.2 . $I_D(V_G)$ (a) and $g_m(V_G)$ in linear regime from $T =$ $300\ K$ to $T = 10\ K$.

Both the subthreshold slope SS and the threshold voltage V_{th} increases by lowering the temperature but the current in strong inversion does not augment significantly, due to the neutral defect-limited mobility, as we will explain in Chapter 4. Furthermore, at $T \leq 50\ K$, the current exhibits some humps above V_{th}, likely due to 1D carrier confinement [102]. These oscillations are more evident if we consider the trans-conductance $g_m = dI_D/dV_G$, as shown in Fig.(3.4.2).(b). Increasing the drain voltage, the oscillations disappeared (Fig.3.4.3), since qV_{DS} is much larger than the energy separation between sub-bands [98] [102].

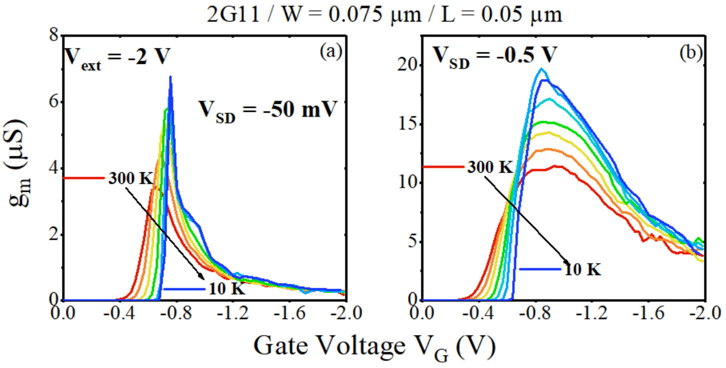

Figure 3.4.3 . $g(V_G)$ in linear (a) and saturation (b) regime from $T = 300\ K$ to $T = 10\ K$.

3.4.1 Electrostatic and linear regime

The approach used to model the experimental curves is the same as the one described before, with the exception that instead of using a 2D density of states in eq.(3.3.1), we used 1D DOS considering several sub-bands contribution (Fig.(3.4.4).(a)):

$$N(E) = \sum_i A_{1D} \cdot \sqrt{\frac{1}{E - E_{C_i}}} \tag{3.4.1}$$

where $A_{1D} = \frac{1}{\pi} \cdot \sqrt{\frac{2 \cdot m_d^*}{\hbar^2}}$, m_d^* is the DOS effective mass and E_{C_i} is the ith sub-band edge. Using the gate charge conservation equation (eq.(3.2.1)) and eq.(3.3.3), one can calculate the inversion charge, plotted in Fig.(3.4.4).(b),(c) versus the Fermi level E_F and gate voltage V_G, respectively. At cryogenic temperature, small humps in the inversion charge can be observed, especially in $Q_i(E_F)$. When the temperature is increased, these oscillations are smeared out, since the electrons' thermal energy is much higher than the energy difference between sub-bands [99]. Knowing the inversion charge $Q_i(V_G)$, it is easy to calculate the gate-to-channel capacitance. In Fig.(3.4.5), modeled $C_{gc}(V_G)$ at both room and cryogenic temperature are plotted. As for the inversion charge, the oscillations that are evident at $T = 50\ K$, are completely smoothed out at $T = 300\ K$. These results are in agreement both with Poisson-Schrodinger simulations [103] and experiments [100].

The drain current $I_D(V_G)$ in linear regime, including the contribution of source and drain series resistances R_{SD} is calculated as:

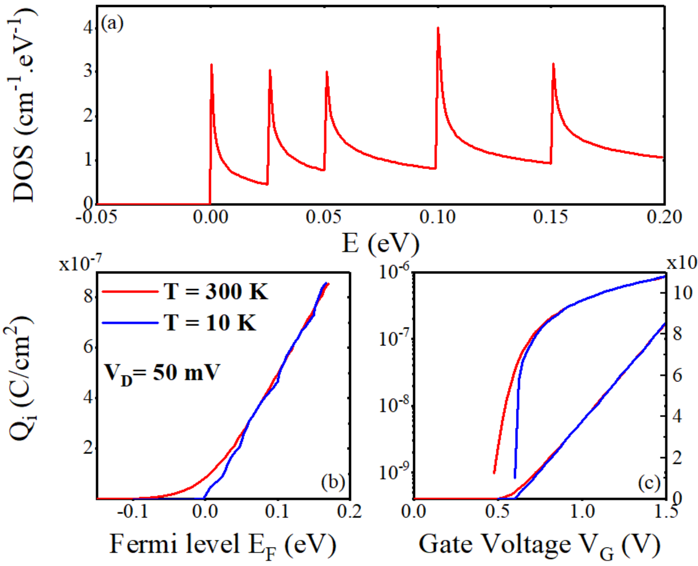

Figure 3.4.4 . (a) DOS profile used in the model. Inversion charge as function of Fermi level (b) and gate voltage (c) both at $T = 300\ K$ and $T = 10\ K$.

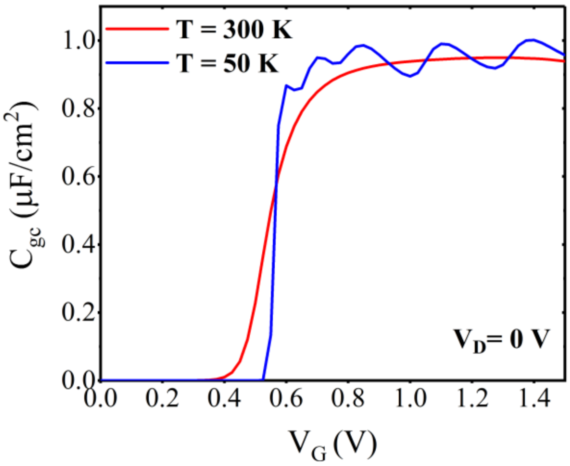

Figure 3.4.5 Modeled $C_{gc}(V_G)$ curves at $T = 300\ K$ and $T = 50\ K$

$$I_D(V_G,V_D,V_b,T,R_{SD}) = \frac{W}{L}.\frac{\mu_{eff}.Q_{inv}(V_G,V_D,V_b,T).V_D}{1+R_{SD}\left(\frac{W}{L}\left(\mu_{eff}.Q_{inv}(V_G,V_D,V_b,T)\right)\right)} \tag{3.4.2}$$

The calculated drain current and trans-conductance at cryogenic temperature are shown in Fig.(3.4.6). The model well reproduces the oscillations in $g_m(V_G)$ that disappear at higher temperatures (Fig.(3.4.7)), in agreement with the experimental curves. These oscillations are a direct signature of the 1D sub-bands filling. In $I_D(V_G)$, instead, humps are less obvious than in experiments. This is likely due to the fact that a constant mobility value was considered in eq.(3.4.2) without taking into account the different scattering mechanisms. In particular, inter-sub-band scattering is believed to be non-negligible, leading to additional mobility degradation at each new sub-bands filling [98].

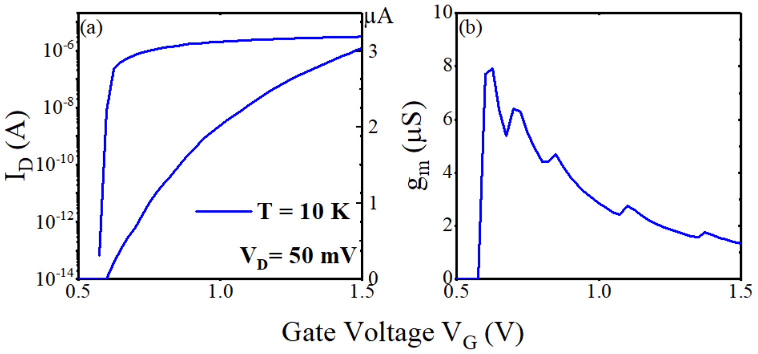

Figure 3.4.6 Modeled $I_D(V_G)$ (a) and $g_m(V_G)$ (b) in linear regime. (Model parameters: $C_{ox} = 1.18\ \mu F/cm^2$, $C_{Box} = 0.078\ \mu F/cm^2$, $V_0 = 0.54\ V$, $C_{Si} = 0.7\ \mu F/cm^2$, $C_b = 0.07\ \mu F/cm^2$)

It is finally worth to point out that the access resistance value used in the model is $R_{SD} = 10\ k\Omega$, which is coherent with those extracted for this technology, as it will be shown in next chapter.

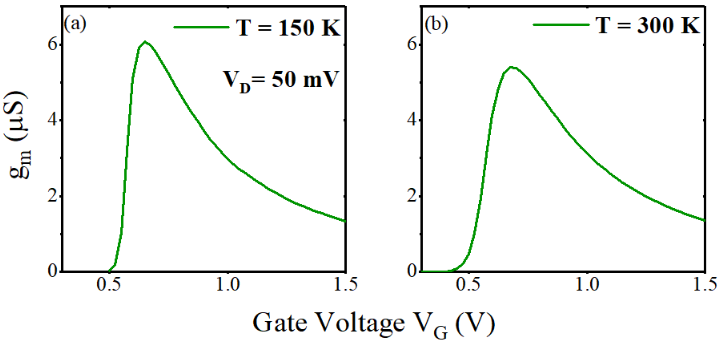

Figure 3.4.7 Modeled $g_m(V_G)$ at $T = 150\ K$ (a) $T = 300\ K$ (b) in linear regime.

3.4.2 High Bias Regime

At high drain bias, the drain current reads [56]:

$$I_{D0}(V_G, V_D, V_b, T) = \int_0^{V_D} \mu_{eff} . Q_{inv}(V_G, U_C, V_b, T)\, dU_C \qquad (3.4.3)$$

where U_C is the quasi-Fermi level shift between source and drain. Eq.(3.4.3) does not include the access resistances contribution. In order to incorporate their effect, we assume that the drain voltage drop across source and drain resistances is small. In this way, it is possible to show that the drain current can be written in first order as

$$Id(V_G, V_D, V_b, T, R_S, R_D) = \frac{I_{D0}(V_G, V_D, V_b, T)}{1 + g_{m0}(V_G, V_D, V_b, T) \cdot R_S + g_{d0}(V_G, V_D, V_b, T) \cdot (R_S + R_D)} \qquad (3.4.4)$$

where R_S and R_D are the source and drain resistance, respectively, $g_{m0} = \frac{dI_{D0}}{dV_G}$ and $g_{d0} = \frac{dI_{D0}}{dV_D}$.

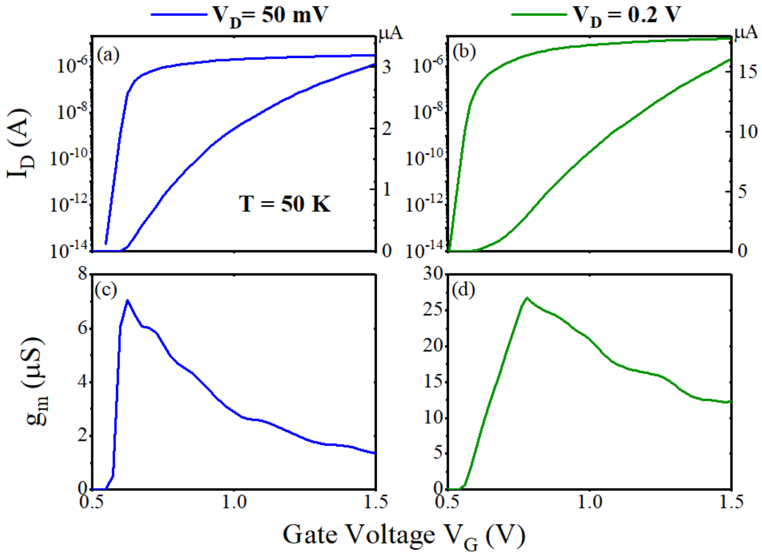

Figure 3.4.8 Modeled $I_D(V_G)$ and $g_m(V_G)$ at $V_D = 50\ mV$ (a), (c) and at $V_D = 0.2\ V$ (b), (d)

The effect of V_D at cryogenic temperature on both $I_D(V_G)$ and $g_m(V_G)$ is shown in Fig.(3.4.8). The oscillations are damped at $V_D = 0.2\ V$, in agreement with what is observed experimentally (Fig.(3.4.3)). Finally, $I_D(V_D)$ characteristics were also plotted and compared with the experimental ones (Fig.(3.4.9)). At room temperature $I_D(V_D)$ is linear at low V_D values, but at cryogenic temperature it shows a non-ohmic behavior. The reason could be linked to the presence of charges at the interface between the Si channel and the spacers. Indeed carriers, in order to populate the channel, must overcome a potential barrier caused by the thick spacers, that is enhanced by the presence of fixed charges [104] (Fig.3.4.10.(a)). At low temperature, because of the reduced thermal energy, carriers can hardly populate the regions underneath the spacers, as shown in Fig.(3.4.10).(b). Using a reasonable value for the fixed charge density, that is $Q_{it} = 1.2.10^{12} q/cm^2$, it was possible to qualitatively reproduce the non-linear behavior of the $I_D(V_D)$, using the simulations tools described in Chapter 2 (see Fig.(3.4.11)).

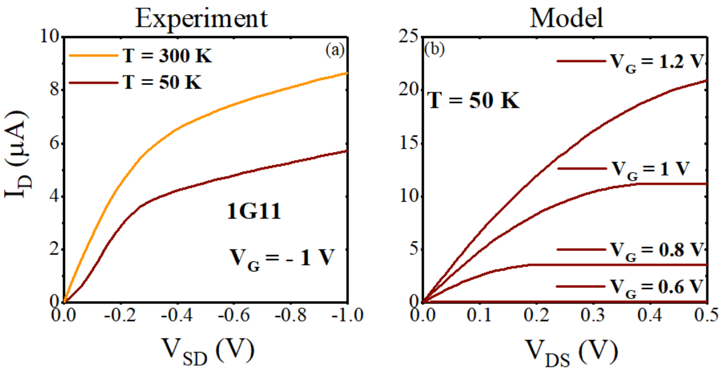

Figure 3.4.9 Experimental (a) and modeled (b) $I_D(V_G)$.

Therefore, the non-ohmic behavior is not related to the 1D confinement, as confirmed by the results obtained by the model, shown in Fig.(3.4.9).(b), where neither non-linear behaviors nor oscillations are evidenced. Finally, it is worth to notice that the current in Fig.(3.4.9).(a) still increases above saturation: this is due to short channel effects, particularly DIBL (drain induced barrier lowering) [69].

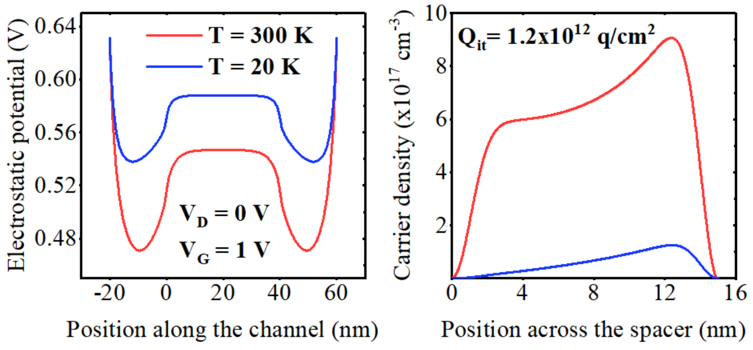

Figure 3.4.10 Experimental (a) and simulated (b) $I_D(V_G)$ for various T with a fixed amount of interface charges

amount of interface charges.

3.5 SUBTHRESHOLD REGION: BEYOND THE BAND TAIL APPROACH

Oscillations observed in the subthreshold current are a known signature of small area MOSFETs operating at cryogenic temperature [52] [89] [90] [105] (Fig.3.5.1). We first study these features using an engineering-like compact model based on the concept of “resistive networks”. Afterwards we provide a physical background showing how it can be interpreted in terms of percolation transport. Indeed, the origin of subthreshold current oscillations is intimately connected to that of the band tails, and it must be traced back to the potential fluctuations caused by interface traps. Band tails are the macroscopic effect of the electrostatic potential randomization, whereas percolation emphasizes the microscopic nature of disorder at $Si - SiO_2$ interface.

3.5.1 Resistive Networks

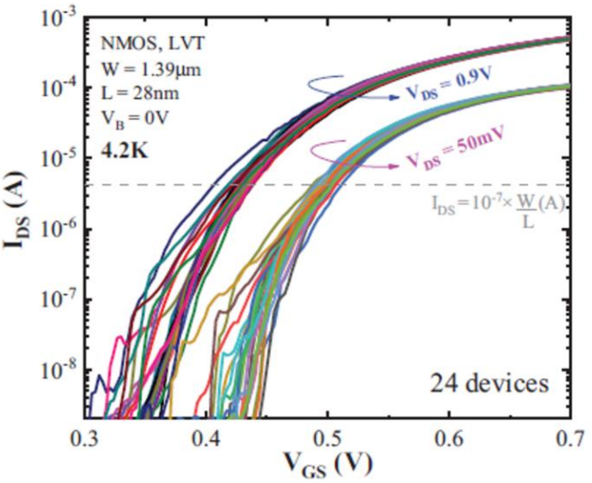

Figure 3.5.1 $I_D(V_G)$ curves for 24 short channel (L = 28 nm) N-type MOSFETs at 4.2 K, at $V_D = 50\ mV$ and $0.9\ V$. Figure taken from [59]].

Potential fluctuations at $Si - SiO_2$ interface randomize the allowed conductive paths in the inversion layer. Indeed, in subthreshold regime, where the carrier density is low, some carriers will participate to transport and some others will be localized [106]. To take into account the conduction paths randomization we model the inversion layer as a network of parallel transistors with different aspect ratios $K = \frac{W}{L}$ and threshold voltages V_{th}. Series transistors do not participate to transport since series paths are extinguished by the most limiting resistance. An example of drain current in the case of three transistors network is plotted in Fig.(3.5.1): each transistor is activated at a different V_{th}, and gives a contribution to the total conductance proportional to its aspect ratio. In this case, the total current is given by:

$$I_{D,Sum}(V_G, V_{th}) = I_D(V_G, V_{th1}, K_1) + I_D(V_G, V_{th2}, K_2) + I_D(V_G, V_{th3}, K_3) \qquad (3.5.1)$$

where $I_D(V_G, V_{th}, K) = K.\mu_0.Q_{inv}(V_G, V_{th}).V_D$, being $Q_{inv}(V_G, V_{th})$ the inversion charge given by the Lambert – W function for the sake of simplicity (eq.(3.2.5)).

In order to emulate the experimental behaviour, the model must be generalized

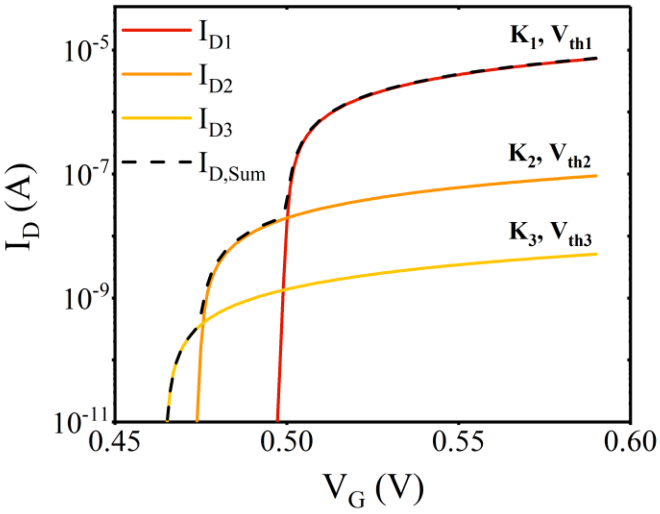

Figure 3.5.2 $I_D(V_G)$ of a three transistors network. Here $K_1 = 1$, $K_2 = 0.01$, $K_3 = 0.0005$, $V_{th1} = 0.5\ V$, $V_{th2} = 0.475\ V$ and $V_{th3} = 0.465\ V$.

to a generic number N_p of transistors whose V_{th} and K are randomly distributed. In the discrete case, the total current can be expressed as

$$I_D = \frac{30}{N_p + 1}.\sum_{i=1}^{N_p} \left(V_D.\mu_0.exp(-30.RE_i).Q_i(V_G, V_{th0} - 30.k_B T_S.RE_i)\right) \qquad (3.5.2)$$

where RE is a vector of random numbers between 0 and 1, V_{th0} is the reference value of the threshold voltage and Q_i is the inversion charge calculated with LW function. Increasing T_S, the subthreshold slope increases as well (Fig.(3.5.3).(a)): the critical temperature defines the energy range of the transistors that participate to conduction, that is, $30. k_B T_S$. Reformulating, in the context of this model, the band tails can be thought as a network of parallel transistors (resistors since we are considering just the linear regime) which are activated at different threshold voltages. Higher critical temperature, that is, a wider band tail, is equivalent to a network whose transistors threshold voltages' are more spread in energy and, therefore, start to conduct at lower gate voltages.

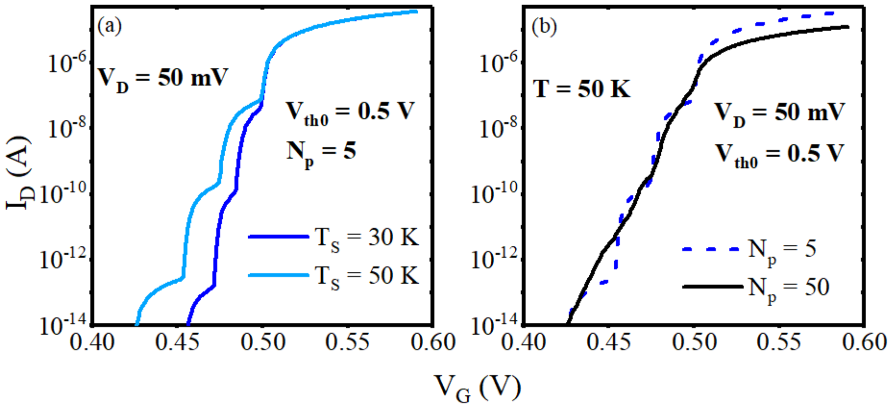

Figure 3.5.3 (a). Impact of T_S in a network with few transistors ($N_p = 5$). (b) Impact of transistors number at a fixed T_S.

A further proof of the validity of this model is plotted in Fig.(3.5.3).(b). Indeed, increasing the number of transistors N_p, the subthreshold current oscillations are smoothed out, and a straight slope can be recovered. At a given T_S, a larger N_p implies a broader conduction area. Large area devices do not show subthreshold oscillations because, even if the number of interface traps is higher, the potential landscape is less sensitive to random fluctuations, and conduction paths are vaster. Eq.(3.5.2) can be written for the continuous case as

$$I_{D,con} = \int_0^1 V_D . \mu_0 . \exp(-30. u). Q_i(V_G, V_{th0} - u. 30. k_B T_S) du \qquad (3.5.3)$$

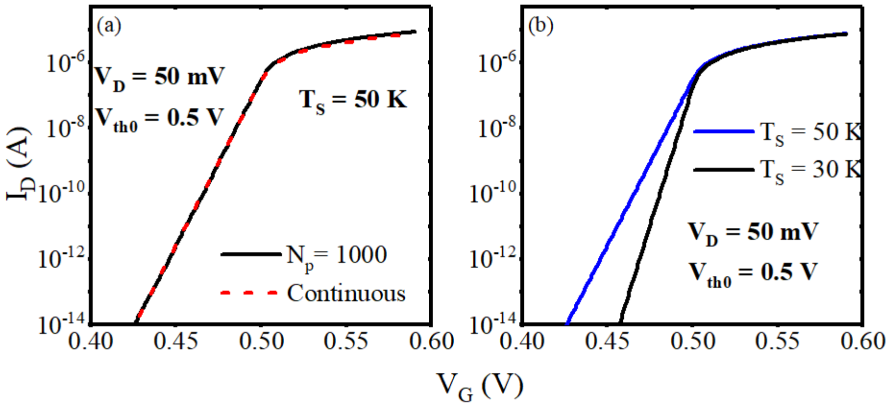

Figure 3.5.4 (a) Comparison between continuous and discrete case. (b) Continuous case $I_D(V_G)$ for $T = 30, 50\ K$.

As can be seen in Fig.(3.5.4).(a), eq.(3.5.2) and eq.(3.5.3) are equivalent if N_p is large enough. Furthermore, also for the continuous case the critical temperature defines the subthreshold slope minimum value (Fig.(3.5.4).(b)).

3.5.2 Percolation transport

In the following, we will provide a physical background to the resistive network model previously introduced.

Let us consider a randomly distributed potential. As already mentioned, potential fluctuations are caused by $Si - SiO_2$ interface traps. Since the trap density is very high ($N_{it} \sim 10^{11}$), according to the central-limit theorem [107], the potential follows a Gaussian distribution [93]:

$$P(V) = (2\pi\sigma^2)^{-\frac{1}{2}}.\exp\left(-\frac{V^2}{2.\sigma^2}\right) \tag{3.5.4}$$

where V is the electrostatic potential and σ is the standard deviation. A derivation of σ can be found in [93] [106], here we will just point out that it can be used as an adjustable tail-width parameter, as shown after. An example of Gaussian potential simulated with FlexPDE is shown in Fig.(3.3.5). If we consider carriers in the inversion layer as classical particles, it is clear from Fig.(3.3.5) that they are excluded from those regions of space where $V > E$, being E the particle energy. On the other side, there are regions where carriers are allowed to propagate, if $V < E$. Using a similitude from [106], the inversion layer can be though as a sea of classical particles, and the prohibited regions as landmass. As the particle energy increases, the level of the sea increases as well, and the amount of lands reduces. Above a critical threshold,

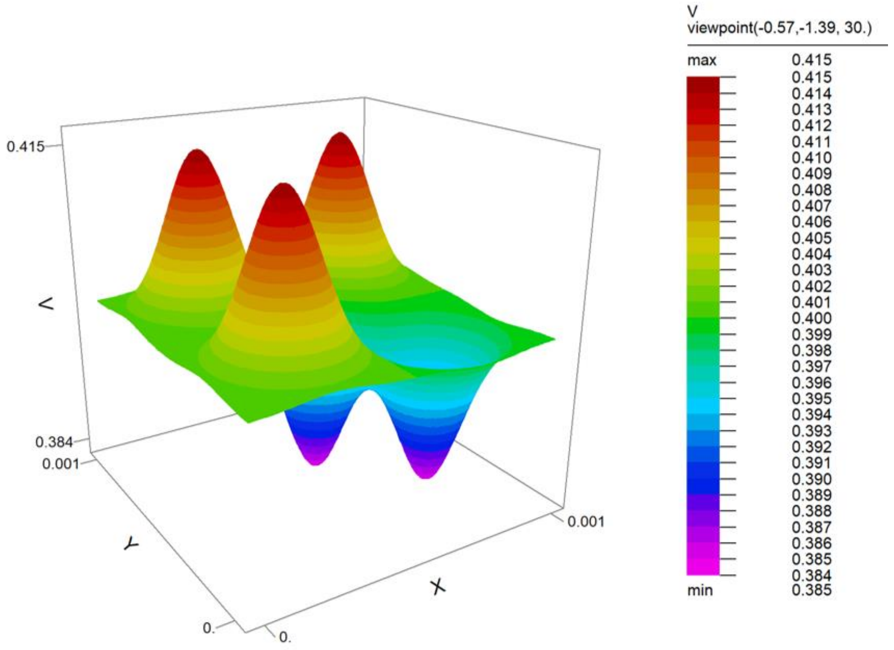

Figure 3.5.5 Example of Gaussian 2D potential simulated with FlexPDE

called "percolation threshold", nearly all space is allowed and carriers can move freely. Below this threshold, allowed regions are separated from continents of prohibited space. At $T = 0$, particles placed in one such region are localized. In such potential landscape, the density of states can be written as [93]

$$N(E) = N_0 . p(E) = \int_{-\infty}^{E} N_0 P(V) dV = N_0 \frac{1}{2} erfc\left(-\frac{E}{\sqrt{2}.\sigma}\right) \qquad (3.5.6)$$

where $erfc$ is the complementary error function, $N_0 = A_{2D} = \frac{g.m_d^*}{\pi\hbar}$ is the 2D density of states and $p(E)$ is the fraction of allowed space. In [107] was demonstrated that, for a Gaussian potential, delocalized states occur for $p(E) > \frac{1}{2}$, whereas isolated allowed regions are found for $p(E) < \frac{1}{2}$. The percolation threshold, i.e. the energy that corresponds to $p(E_C) = \frac{1}{2}$, in this approach, is found at $E_C = 0$ [93]. In Fig.(3.5.6).(a) is plotted $p\left(\frac{E}{\sqrt{2}.\sigma}\right)$. Below $E = 0$, states are localized and transport is thermally activated. Indeed, for $T \to 0$, the conductivity drops to zero. Above $E = 0$, conductive paths are formed and the transport is predominantly free-carrier-like [93] [94][106]. It is worth to point out that the density of states derived directly from the potential distribution (eq.(3.5.6)) is equivalent to the analytical expression introduced previously (eq.(3.3.19)), as can be observed in Fig.(3.5.6).(b). Here, we used the standard deviation in the Gaussian distribution as a fitting parameter, and its value is

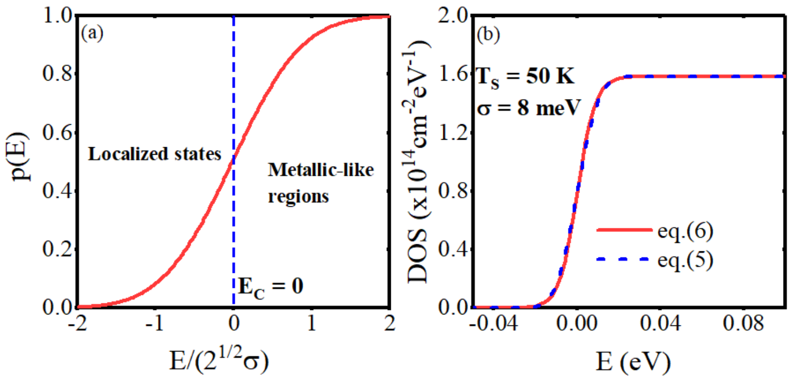

Figure 3.5.6 (a) Fraction of allowed space $p(E)$, reproducing model in [42]. (b) Comparison between ea.(3.3.19) and eq.(3.5.6).

consistent with the literature [106]. In such a way, the microscopic origin of the density of states band tail is lightened.

In Fig.(3.5.7) is sketched the current in the two dimensional potential plotted in Fig.(3.5.5) at different gate voltages V_G. When $V_G = 0.38\ V$, prohibited regions are clearly visible in purple, and only few carriers can flow in a small channel. At a higher voltage, carriers are free to flow, even if there are still more resistive regions. In percolation, metallic-like and thermally activated transport coexist around the percolation threshold. Increasing or decreasing the particle energy will favor one of the two transport mechanisms, until the other one is completely suppressed. We can now link the restive networks model with percolation transport. The randomly distributed charges at $Si - SiO_2$ interface induce potential fluctuations that, in turns, produce areas where carriers can propagate freely and prohibited “islands”, where particles are localized. Therefore, the inversion layer can be thought as an arrangement of conductive and non-conductive regions. Resistors networks’ can be used to model paths where transport is allowed [108]: the higher the number of resistors, the wider the metallic-like conduction area. On the other hand, few resistors mean that the prohibited regions are vast. From a subthreshold current point of view, large areas of free carrier transport translate in a straight subthreshold slope, where no features related to the microscopic potential fluctuations are visible.

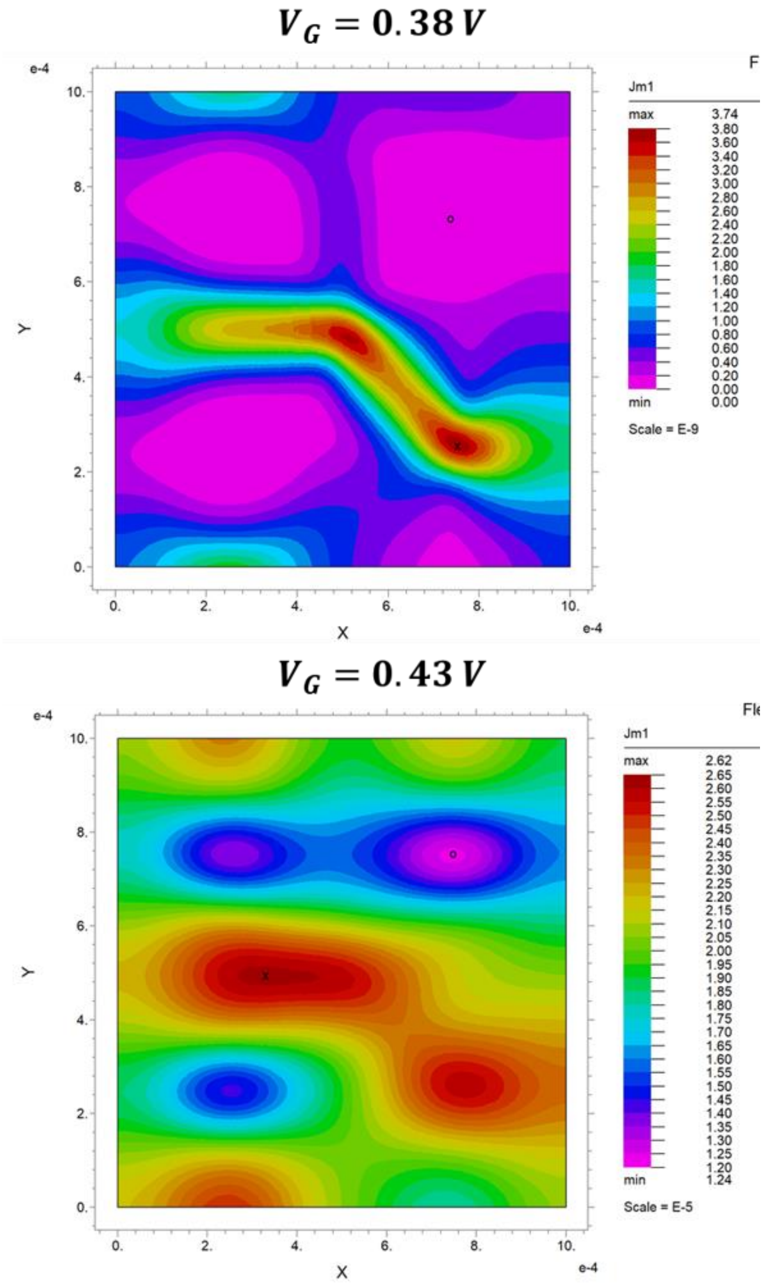

Figure 3.5.7 Simulated 2D current in the Gaussian potential plotted in Fig.3.5.5

The macroscopic effect is the subthreshold slope saturation caused by the band tails, whose width is defined by the standard deviation of the Gaussian distribution of the electrostatic potential. This is the typical behavior observed in large area devices. Reducing device dimensions, the microscopic details of percolation are visible in the subthreshold current.

3.5.3 **Percolation in 1D Systems**

The model previously described does not explain all the features experimentally observed. Indeed, by looking at the subthreshold current in Fig.(3.5.1), one can notice that it sometimes decreases. A possible way to justify it, it is through 1D quantum confinement. Indeed, in the percolation picture previously introduced, it is reasonable assuming that some carriers can move just along 1D channels and not in 2-dimensional valleys. Therefore, the first hypothesis of the following model is that carriers that participate to conduction can be treated as 1D systems. For simplicity, we assume that they occupy just the lowest energy sub-band, and the density of states reads

$$N(E) = A_{1D}.\frac{1}{\sqrt{E}} \tag{3.5.7}$$

The carrier density is calculated using eq.(3.3.1). In order to compute the conductivity of a single transistor, we introduce the Kubo-Greenwood (K-G) integral [58] [109]:

$$\sigma(E_F,T) = \int_0^\infty \sigma_E(E).\left(-\frac{\partial f}{\partial E}\right)dE \tag{3.5.8}$$

where $\sigma_E(E)$ is the microscopic conductivity function and $f(E_F,T)$ is the Fermi-Dirac function. K-G formula allows to calculate the macroscopic conductivity as function of temperature. Moreover, no particular hypothesis concerning the disorder of the system are required, making it suitable also for non-crystalline structures. A classical derivation of eq.(3.5.8) can be found in [110].

The second hypothesis of this model concerns the expression of $\sigma_E(E)$. Indeed, we assume a constant diffusivity function $D(E)$. In such a way, the microscopic conductivity can be written [110]:

$$\sigma_E(E) = q.D(E).N(E) = q.D.N(E) \tag{3.5.9}$$

According to eq.(3.5.9), the conductivity, through the 1D density of states, is inversely proportional to energy, and consequently to gate voltage.

By solving the gate charge conservation equation (eq.(3.2.1)), it is possible to calculate the surface potential $\psi_S(V_G,V_D,V_b,T)$ and the Fermi level $E_F(V_G,V_D,V_b,T)$. The current for a single transistor is given by

$$I_D = \frac{W}{L}\frac{\sigma(E_F,T)}{W_{eff}}.V_D \tag{3.5.10}$$

where W_{eff} is the effective channel width. Eq.(3.5.2) can be rewritten as:

$$I_{D,dis} = \frac{30}{N_p + 1} . \sum_{i=1}^{N_p} \left(exp(-30. RE_i). I_D(V_G + 30. k_B T_S. RE_i, V_D, V_b, T) \right) \quad (3.5.11)$$

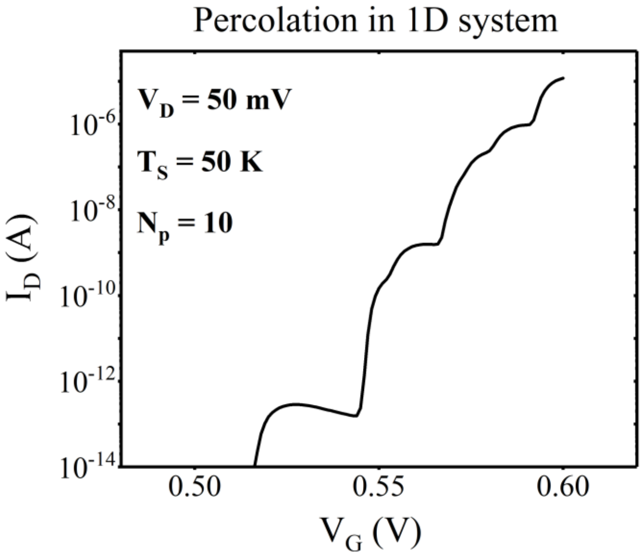

Figure 3.5.8 Percolation in 1D system.

In Fig.(3.5.8) is plotted an example of $I_{D,dis}(V_G)$ obtained using eqs.(3.5.7)-(3.5.11), with $N_p = 10$. The current shows oscillations with negative slope, as observed in experimental data.

3.6 CONCLUSION

In this chapter, we introduced several compact models for FD-SOI devices at cryogenic temperatures. First, we described the Lambert-W function, and its applicability in calculating the channel inversion charge. Afterwards, we introduced a more advanced model based on the Fermi-Dirac statistics and the gate charge conservation equation. Exploiting these equations, we propose an original explanation of the zero temperature coefficient in FD-SOI, going through the transport impact. The band tails has been introduced and its influence on device electrostatics has been outlined. After that, 1D confinement in Si nanowires at cryogenic temperature has been modeled, showing its impact on both drain current and trans-conductance. Finally, a model based on the physical concept of percolation transport was introduced in order to account for subthreshold current oscillations.

Chapter 4: Device Characterization

4.1 INTRODUCTION

Quantum bits mass production is a necessary step to achieve for the realization of quantum computers able to accomplish high demanding tasks. Indeed, hundreds or even millions of quits will be required in the future quantum computers. In such a scenario, fast screening and selection of functional devices is mandatory and electrical parameters extraction methods effective in a wide range of temperature must be developed accordingly. Indeed, industrial approach to qubit manufacturing requires not only the technology to be mature and reliable, but also easy-to-use device compact models for device rapid characterization.

This chapter is dedicated to the characterization of both FD-SOI and qubit devices from room down to deep cryogenic temperature. First, we rapidly describe the set-up used in experiments. Afterwards, we focus on the capacitance and current characterization of large FD-SOI devices, fabricated using the LETI qubit technology process, in order to extract the main physical quantities, such as inversion charge and effective mobility. Finally, short channel qubit devices with several gates in series are characterized. In this context, we introduce a compact model based on the Lambert-W function able to fit the experimental curves from subthreshold to strong inversion regime and from room down to deep cryogenic temperatures. Particular attention is devoted to the extraction of low field mobility and access resistances. Indeed, the first turned out to provide important insights on the devices physics that can be used to fathom which gates can offer better performances as quantum dots. To conclude, we mention about the mobility temperature trend in saturation regime.

4.2 EXPERIMENTAL SETUP

In this section, we will describe the setup used to collect cryogenic temperature measurements.

4.2.1 Cryo bench

The cryo bench used in the experiments is shown in Fig.(4.2.1). It is a CPX Lake Shore cryoprober, with a temperature control from $T = 300\ K$ to $T = 4.2\ K$. The sample is placed in a chamber (Fig.4.2.2) that is put under vacuum ($p_{Chamber} \cong 1.3.10^{-4}\ mbar$). The cryostat is equipped with six probe arms, which allow contacting the devices under test with six individuals DC or RF probes.

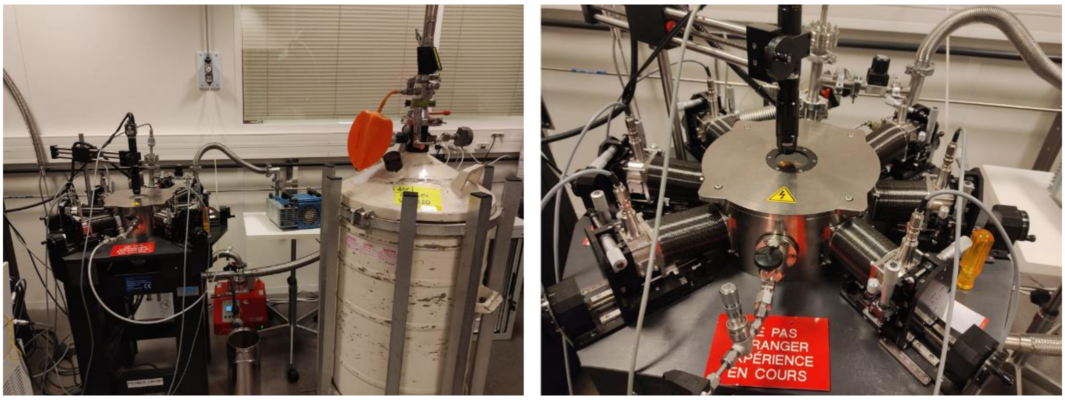

Figure 4.2.1 Photographs of the experimental setup

Once the vacuum is reached, liquid helium is made to flow inside the cryostat through a stick that has been previously inserted inside the He bottle.

It is possible to tune the temperature of the sample holder thanks to a heating resistance controlled by a PID system.

In our experiments, a Keysight LCR – meter E4980A was used to measure capacitance, whereas a semiconductor device analyser Keysight B1500 was used to perform drain current measurements.

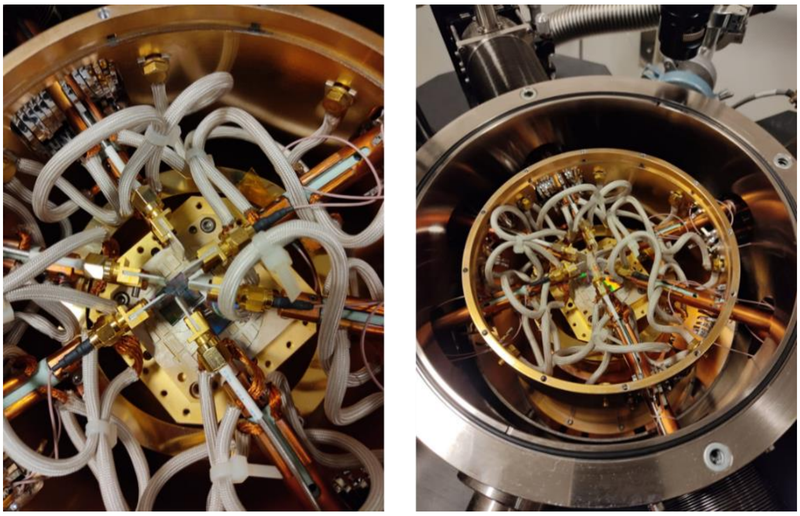

Figure 4.2.2 Inner chamber of the cryostation.

4.3 FDSOI CHARACTERIZATION

In the following, we present the characterization from room down to $T = 4.2\ K$ of a large and wide FD-SOI device fabricated using the LETI qubit process flow [48] [37]. The gate length and width are, respectively, $L_G = 3\ \mu m$ and $W_G = 20\ \mu m$. It is worth pointing out that the device is composed of two fins placed in parallel, each of which has a width of $W_{G,fin} = 10\ \mu m$. Since the total conductance of two identical parallel transistors is twice the single conductance, and the measured capacitance corresponds to the total device capacitance, in the following we assume to have a single device with a total width of $W_G = 20\ \mu m$. The unintentionally doped silicon body thickness is $t_{Si} = 9.8\ nm$, whereas the gate oxide consists of $6\ nm$ of SiO_2. Finally, the BOX is made of 145 nm of SiO_2 .

4.3.1 Split C-V Methodology

Capacitance characteristics permit the extraction of several intrinsic channel properties, such as the inversion charge Q_{inv}, flat band voltage V_{fb} and gate oxide capacitance C_{ox}. Moreover, exploiting together capacitance and current curves, it is possible to also extract the effective mobility as function of Q_{inv}. One of the most popular techniques to measure the gate-to-channel capacitance $C_{gc}(V_G)$ is the so-called "Split C-V method" [111]. In Fig.(4.3.1) is shown the schematic of the experimental set-up [73].

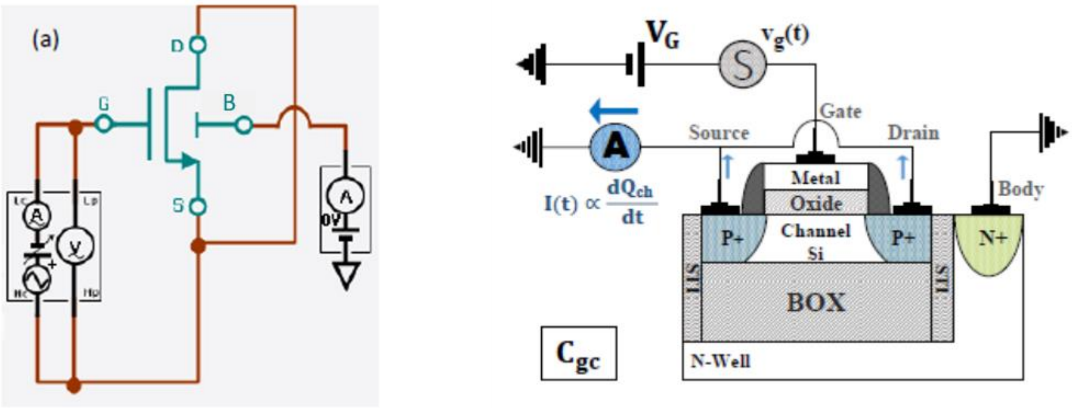

Figure 4.3.1 Set-up configuration for split C-V technique. Taken from [27]

The "low" terminal of a LCR-meter is connected to the Source (S), Drain (D), whereas the "high" terminal is connected to the Gate (G). The substrate under the BOX is used as a back – gate access.

Influence of AC signal frequency and oscillator level

There are two critical experimental parameters to tune properly during capacitance measurements: AC signal frequency f and oscillator level ΔV_G. In general, increasing f allows reducing the measurement noise. We decided to set $f = 100\ kHz$, since going at higher frequencies did not provide any benefit, as shown in Fig.(4.3.2).

The AC signal oscillator level was set at $\Delta V_G = 5\ mV$, except at $T = 300\ K$, where it was set at $\Delta V_G = 40\ mV$. The time-dependent signal is superimposed to a specific bias point, and the LCR-meter measures the charge variation with respect the potential variation around this point. Since at deep cryogenic temperatures the transition from weak to strong inversion is really steep (see Fig.(4.3.2)), a signal with large amplitude spans points that are in both regions, and the resulting capacitance will be flattened with respect to the real one. For this reason we choose a signal oscillator level of $\Delta V_G = 5\ mV$ [79]. The drawback is that, decreasing the signal amplitude, the measurement is more susceptible to noise.

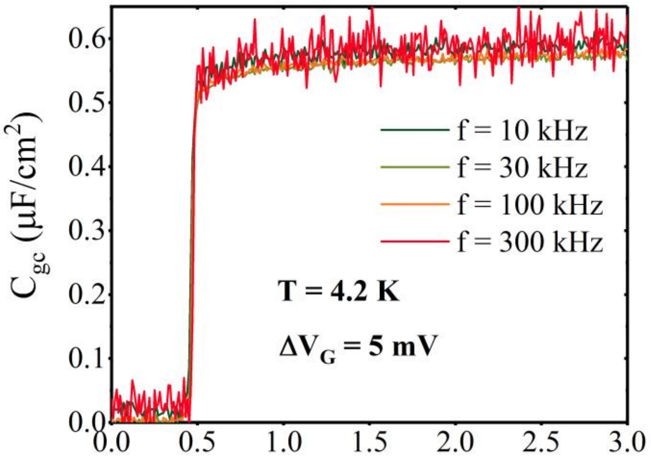

Figure 4.3.2 $C_{gc}(V_G)$ curves at $T = 4.2\ K$ taken at different frequencies.

4.3.2 Inversion charge and gate oxide capacitance extraction

Given the gate-to-channel capacitance (Fig.(4.3.3).(a)), it is possible to calculate the channel inversion charge $Q_{inv}(V_G)$ as [111] [112]:

$$Q_{inv}(V_G) = \int_{V_{acc}}^{V_G} \frac{C_{gc}(V)}{W_G . L_G} dV \tag{4.3.1}$$

where V_{acc} is the lower integration limit in accumulation regime, where the capacitance C_{gc} drops to zero, and V_G is the value at which the inversion carrier density is computed. The extracted inversion charge from $T = 300\ K$ down to $T = 4.2\ K$ is plotted in Fig.(4.3.3).(b).

Recalling eq.(3.2.2), one can writes [71]:

$$\frac{1}{C_{gc}} \approx \frac{1}{C_{ox}} + \frac{1}{\beta Q_{inv}} \tag{4.3.2}$$

that can be reformulated as

$$\frac{Q_{inv}}{C_{gc}} \approx \frac{Q_{inv}}{C_{ox}} + \frac{1}{\beta} \tag{4.3.3}$$

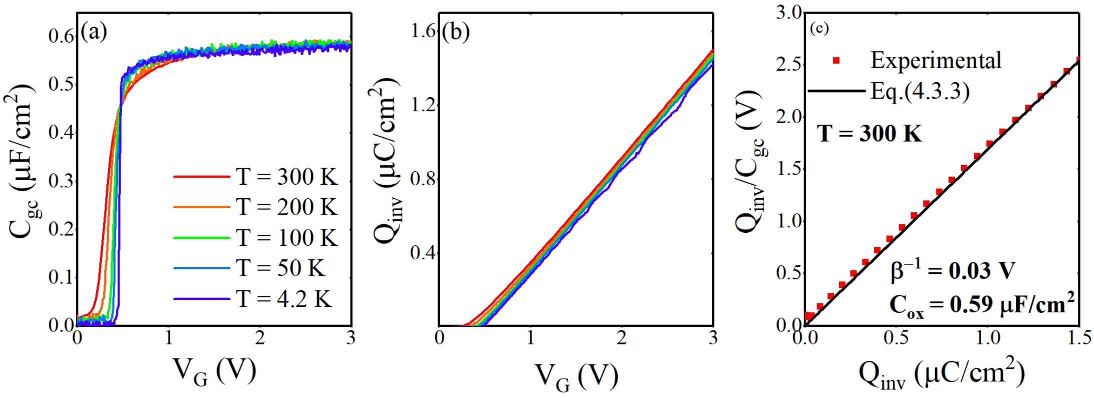

Figure 4.3.3 Experimental $C_{gc}(V_G)$ (a) and extracted $Q_{inv}(V_G)$ (b). (c) $Q_{inv}/C_{gc}(Q_{inv})$

The previous equation, considering that $\frac{1}{\beta} = \frac{k_B.T}{q} \approx 0.03\ V$ at $T = 300\ K$, is a linear function of Q_{inv}, as shown in Fig.(4.3.3).(c), and from its slope one can extract C_{ox}. In this case, we obtained $C_{ox} = 0.59\ \mu F/cm^2$, that is equivalent to $t_{ox} = \frac{\epsilon_{SiO_2}}{C_{ox}} = 6\ nm$, that is, the nominal value. Eq.(4.3.3) thus provides an easy way to extract the oxide capacitance and the equivalent oxide thickness.

4.3.3 Mobility curves

As we already mentioned, in order to extract the effective mobility as function of gate potential or inversion charge, we have to couple capacitance and current measurements. The drain current in linear regime reads

$$I_D(V_G) = \frac{W_G}{L_G}.\mu_{eff}(V_G).Q_{inv}(V_G).V_D \tag{4.3.4}$$

and the effective mobility $\mu_{eff}(V_G)$ can be expressed as

$$\mu_{eff}(V_G) = \frac{L_G}{W_G} \cdot \frac{I_D(V_G)}{Q_{inv}(V_G).V_D} \tag{4.3.5}$$

where $Q_{inv}(V_G)$ is given by eq.(4.3.1). In the experiments, in order to avoid the effect of the gate leakage current I_G, we adopted the approach described in [113]: both the drain and the source currents were collected by reversing the drain bias, and the mobility was given by the average between the source and drain contribution:

$$\mu_{eff}(V_G) = \frac{L_G}{W_G} \cdot \frac{I_D(V_G) + I_S(V_G)}{2.\,Q_{inv}(V_G).V_D} \tag{4.3.6}$$

Both drain current characteristics and associated mobility curves from $T = 300\ K$ down to $T = 4.2\ K$ are plotted in Fig.(4.3.4).

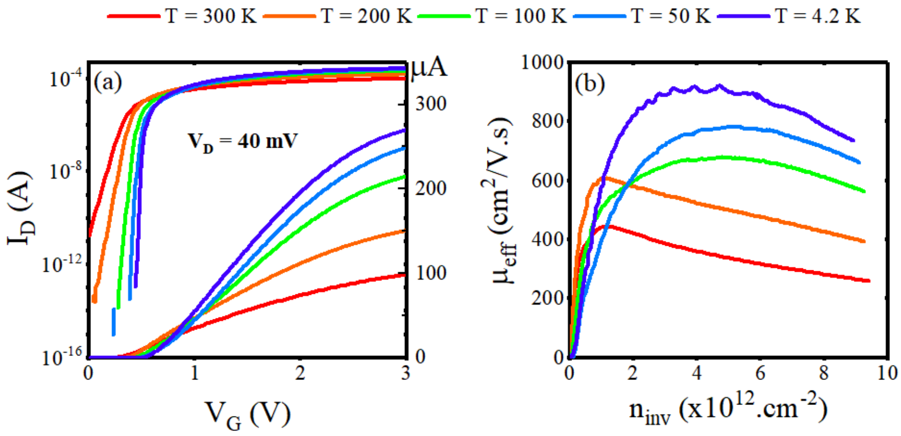

Figure 4.3.4 $I_D(V_G)$ from $T = 300\ K$ down to $T = 4.2\ K$ (a). Associated mobility curves (b).

No clear ZTC point is present in $I_D(V_G)$ curves, contrary to what one can observe in $C_{gc}(V_G)$ (Fig.(4.3.3).(a)). This disappearance is due to the low field mobility temperature behavior, as it will be explained afterwards. Concerning the effective mobility $\mu_{eff}(n_{inv})$, it follows the typical bell shape at cryogenic temperature, as a consequence of the phonon scattering reduction [114] [115] [116]. At high inversion carrier densities, that is, at high electric fields, the mobility is mainly limited by surface roughness, whereas at low inversion carrier densities, μ_{eff} is limited by Coulomb scattering. It is worth pointing out that the drop to zero of the mobility at low densities is not physical, and must be attributed to a limit of the C-V split method [75].

4.3.4 Y-function parameter extraction method

$Y - function$ was introduced for the first time in [117]. Neglecting the second order mobility attenuation coefficient θ_2, the drain current in linear regime can be written as

$$I_D(V_G) = \frac{W_G}{L_G} C_{ox}. \frac{\mu_0}{1 + \theta_1.(V_G - V_{th})}.(V_G - V_{th}).V_D \qquad (4.3.7)$$

The trans-conductance can be obtained by derivation of eq.(4.3.7) with respect to V_G:

$$g_m(V_G) = \frac{dI_D}{dV_G} = \frac{W_G}{L_G}.C_{ox} \frac{\mu_0}{\left(1 + \theta_1.(V_G - V_{th})\right)^2}.V_D \qquad (4.3.8)$$

The idea behind the $Y - function$ is to provide a linear function of V_G that enables the extraction of the main device intrinsic parameters, i.e. V_{th} and μ_0. In other words, it is necessary to get rid of the access resistances contribution to the drain current, through the first order attenuation factor i.e. $\theta_1 = \theta_{10} + R_{sd}.\frac{W_G}{L_G} C_{ox}.\mu_0$. The $Y - function$ is defined as:

$$Y(V_G) = \frac{I_D(V_G)}{\sqrt{g_m(V_G)}} = \sqrt{\frac{W_G}{L_G} C_{ox}.\mu_0.V_D}.(V_G - V_{th}) \qquad (4.3.9)$$

From the slope of the function defined in eq.(4.3.9), shown in Fig.(4.3.5), it is easy to deduce the low field mobility μ_0, whereas from its intercept with the x-axis, one can

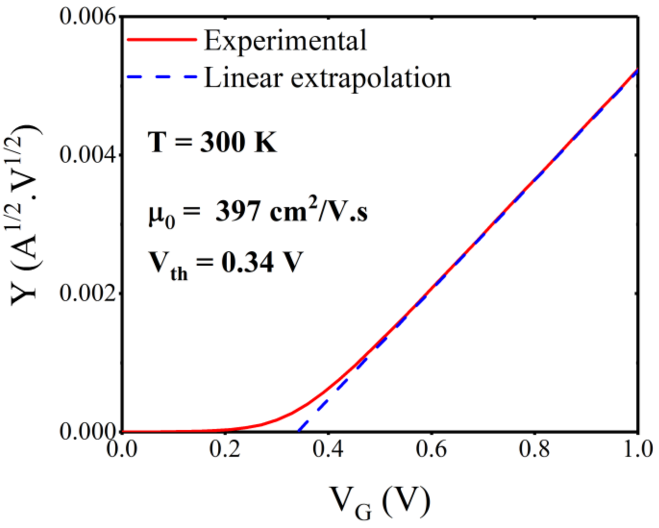

Figure 4.3.5 $Y(V_G)$ obtained at $T = 300\ K$.

extract the threshold voltage V_{th}. $Y(V_G)$ reported in Fig.(4.3.5) was calculated from the $I_D(V_G)$ characteristics at room temperature shown in Fig.(4.3.4).

Considering that LETI quantum bits devices are based on trigate nanowires, and that we already shown how quantum confinement can affect the inversion charge and, ultimately, the drain current, it is worth to clarify the meaning of eq.(4.3.9). Indeed, it is based on the assumption that the inversion charge Q_{inv} depends linearly on V_G in strong inversion. This is experimentally verified in planar devices with thick oxide even at deep cryogenic temperatures (Fig.(4.3.3).(b)), and corroborated by the compact models based both on Maxwell-Boltzmann and Fermi-Dirac statistics introduced in the previous chapter. When 1D quantum confinement comes into play, however, Q_{inv} shows some signatures of the 1D DOS and it is no more perfectly linear with V_G (see Fig.(3.4.4).(b),(c)). Anyway, in such case, it is still possible to consider an “average” $Y - function$, and extracting average intrinsic parameters, neglecting the oscillations and the features linked to quantum confinement.

4.3.5 Results and comments

As explained in Chapter 3, the Lambert-W function can be used to model the channel inversion charge Q_{inv} and, from eqs.(3.2.6)-(3.2.7), it is possible to fit the experimental current curves using five fitting parameters: V_{th}, $\mu_0, \theta_1, \theta_2$ and n. The experimental curves fitted by the LW model are plotted in Fig.(4.3.6). In

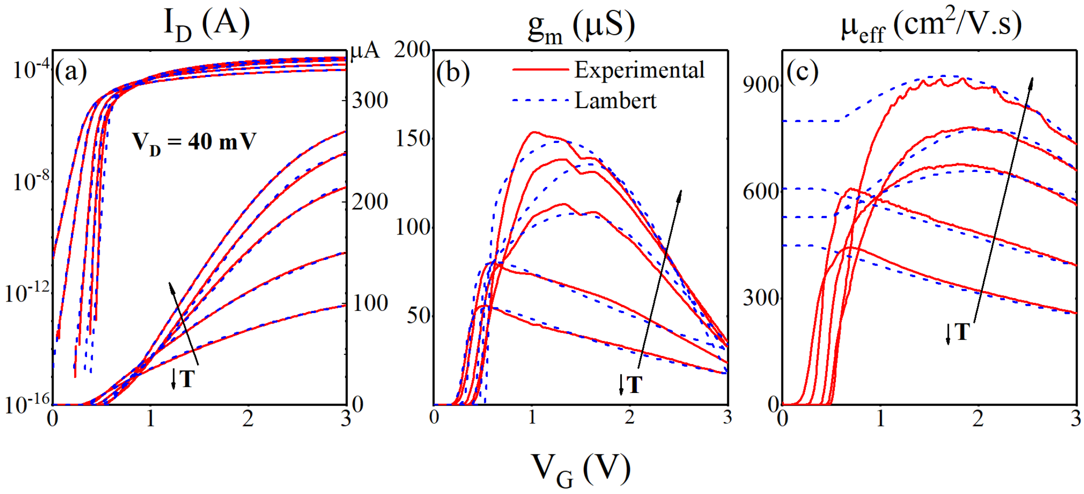

Figure 4.3.6 Experimental (red straight lines) and Lambert modeled (dashed blue lines) $I_D(V_G)$ (a), $g_m(V_G)$ (b) and $\mu_{eff}(V_G)$ (c) at various temperature.

Fig.(4.3.6).(c), is shown μ_{eff} extracted with the C-V split method and the one obtained using eq.(3.2.7). The two methodologies are in good agreement in strong inversion, whereas around and below threshold they strongly differ. This can be explained by the finite value of μ_{eff} reached below threshold according to eq.(3.2.7), that is $\mu_{eff} = \mu_0$, and by the erroneous value of μ_{eff} estimated by the C-V method at low inversion carrier densities.

In Fig.(4.3.7) are plotted the $Y(V_G)$ at several temperatures. $Y - function$ was used to extract mobility and threshold voltage. It is worth noticing that, especially at $T \leq 100\ K$, it is arduous to locate the linear region of $Y(V_G)$ to extrapolate the threshold

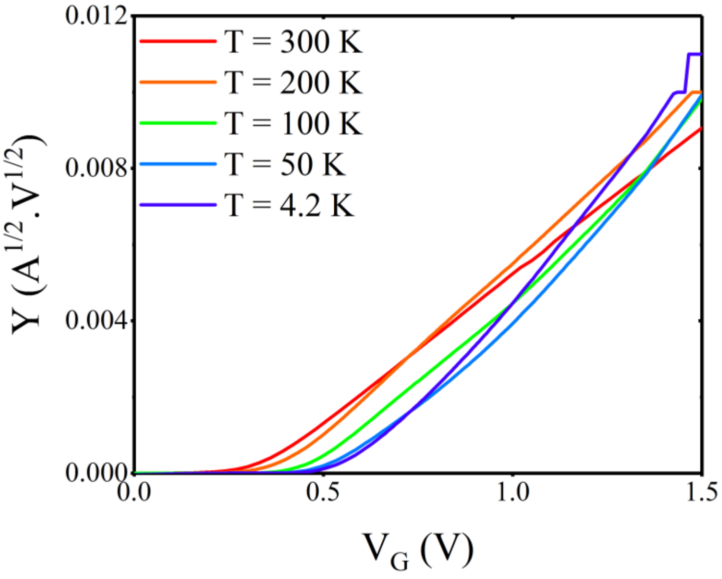

Figure 4.3.7 $Y(V_G)$ at various T.

voltage and the mobility. This is the main reason why, at deep cryogenic temperatures, LW function provides an easier parameters extraction.

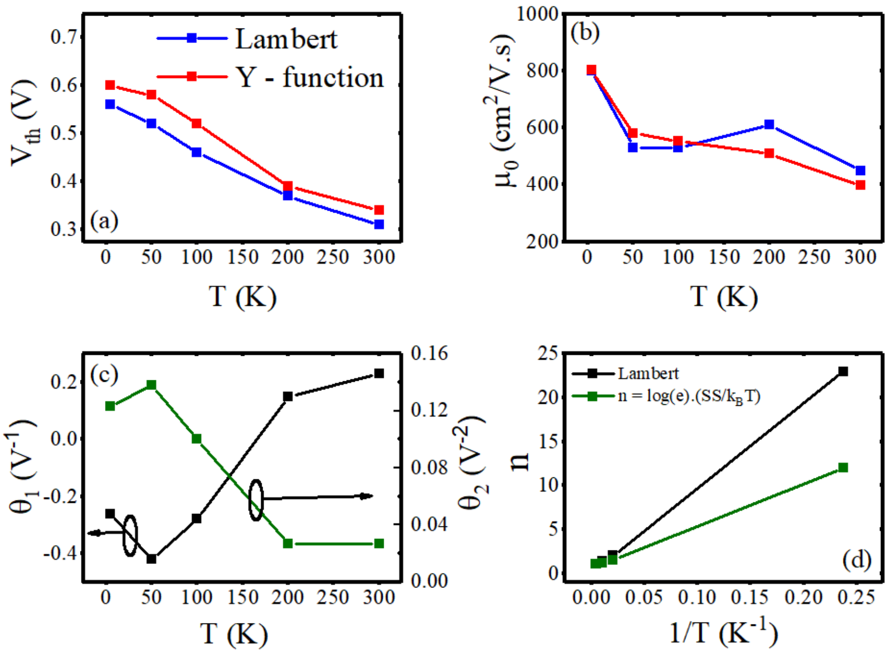

Figure 4.3.8 V_{th} (a) and μ_0 (b) values extracted with $Y - function$ (red symbols) and LW function (blue symbols). (c) θ_1 and θ_2 obtained with LW function. (d) comparison between ideality factors extracted with different methods.

A comparison between the intrinsic parameters extracted using LW function and $Y - function$ is shown in Fig.(4.3.8).(a),(b). There is good agreement between the two methods: V_{th} increases quasi-linearly with temperature whereas μ_0 does not show a clear trend. Indeed, it slightly augments from $T = 300K$ to $T = 50\ K$, and then it increases of almost 50% at $T = 4.2\ K$. Using the Mathiessen equation (eq.(2.3.2)) to fit the experimental data extracted with $Y(V_G)$, it was possible to derive the values of the mobility scattering parameters (Fig.(4.3.9).(a)). The main contributions come from neutral defects and phonons. Coulomb scattering does not really play a role, and this can be easily seen by looking at the mobility temperature trend. Indeed, below 50 K, μ_0 rapidly increases, whereas Coulomb scattering, if present, should reduce the mobility at these temperatures (see Fig.(3.3.3)). The fact that neutral defects scattering is so relevant in this device explains why no ZTC point is observed neither in $I_D(V_G)$ nor in $g_m(V_G)$ (Fig.(4.3.6).(a),(b)), whereas it is clearly visible in $C_{gc}(V_G)$ (Fig.(4.3.3).(a)). In Fig.(4.3.8).(c) are plotted the first and second order mobility attenuation factors. θ_1 is found to be negative at $T < 200\ K$. These values allow to mimic the increase of μ_{eff} at cryogenic temperature (Fig.(4.3.6).(c)). Indeed, negative values of θ_1 permit to extend the validity of the classical mobility law expressed in eq.(3.2.7) even at cryogenic temperatures, where $\mu_{eff}(V_G)$ is represented by a bell shape function [118]. The increase of θ_2 at low temperatures, on the other side, must be attributed to higher influence of surface roughness scattering, since the carriers get closer to the $Si - SiO_2$ interface ([119] and Fig.(2.3.2)). Finally, in Fig.(4.3.9).(d), are reported the ideality factor values extracted both with LW function and from the subthreshold slope, through the classical expression $n = \log(e) . \frac{SS}{k_B.T}$. n goes almost as $1/T$, even if the LW function method overestimates its value at deep cryogenic temperature. As already remarked, the high values of the ideality factor at low temperature do not have any physical meaning, but they are consequence of the saturation of the subthreshold slope, as can be seen in Fig.(4.3.9).(b). Here, the values of n were extracted by considering the subthreshold slope at a constant current value, i.e. $I_D = 10^{-9}$.

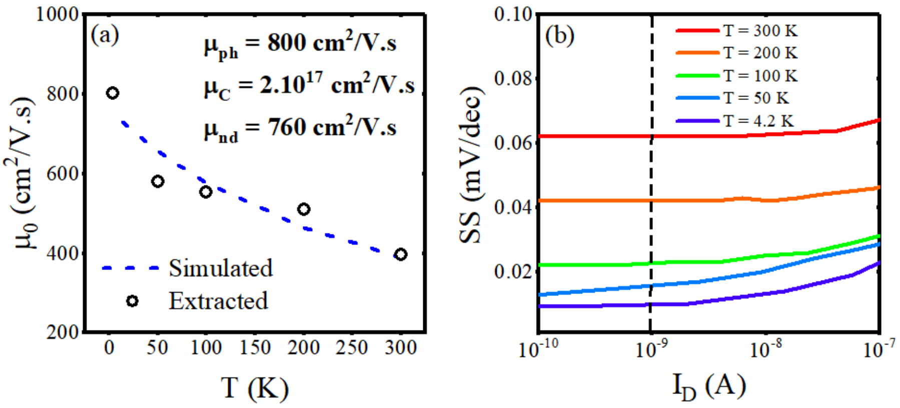

Figure 4.3.9 (a) Experimental (symbols) and simulated (dashed line) low field mobility as function of temperature. (b) Subthreshold slope as function of drain current for different temperatures.

Subthreshold regime

Several methods have been proposed in order to model the subthreshold slope saturation at cryogenic temperatures [64] [76] [95]. Here we follow the model described in [64].

The subthreshold slope temperature trend can be fitted by the following function:

$$SS(T_S, \alpha, C_{it}) = 2.3.\, k_B T_S . \frac{C_{ox} + C_b + C_{it}}{C_{ox}} . \left(1 + \alpha . \ln\left(1 + e^{\frac{T - T_S}{\alpha . T_S}}\right)\right) \qquad (4.3.10)$$

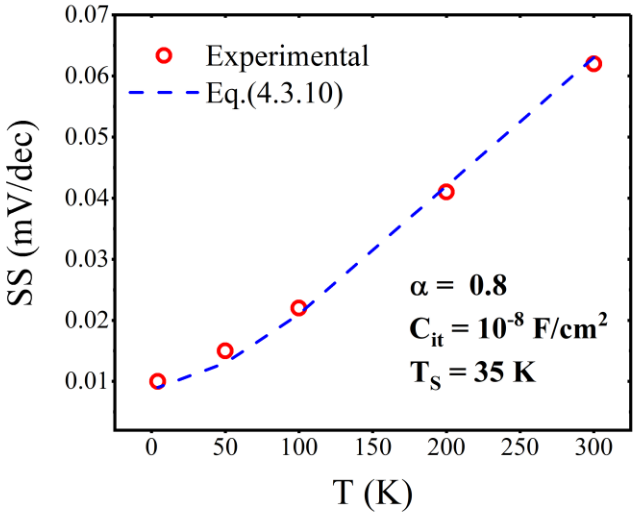

Figure 4.3.10 Experimental (symbols) and modeled (dashed line) SS.

where α is a smoothing parameter. As shown in Fig.(4.3.10), eq.(4.3.10) and experimental data are in good agreement, and the temperature behaviour of SS is well reproduced. The critical temperature ($T_s = 35\,K$) is slightly lower than the one extracted from the capacitance in Chapter 3, but it is still coherent with the values reported in literature [64] [76]. The C_{it} extracted corresponds to $N_{it} = \frac{C_{it}}{q} = 6.25 \cdot 10^{10} \frac{1}{cm^2.eV}$. It is worth pointing out that this value corresponds to the room temperature one. Indeed, as already remarked, at deep cryogenic temperature the Fermi level sweeps both interface charge and localized states, and the extracted trap density is not reliable.

4.4 MULTI-GATE DEVICES CHARACTERIZATION AND MODELING

In this section, we characterize a typical p-type FD-SOI qubit MOS device from $T = 300\,K$ down to $T = 20\,K$. We develop a compact model based on Lambert W function in order to extract the main device intrinsic parameters. We chose to characterize a qubit device with five gates (5G device) and it is shown in Fig.(4.4.1).

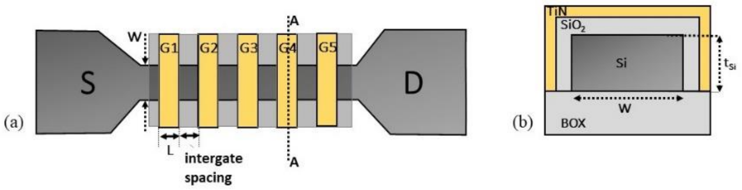

Figure 4.4.1 5G device schematic top view (a) and AA cross section (b).

The 5G device has the same dimensions as those presented in Chapter 3, i.e. $W_G = 75\ nm$, $L_G = 40\ nm$, $t_{Si} = 17.9\ nm$. The silicon gate oxide and the buried oxide are $t_{ox} = 6\ nm$ and $t_{BOX} = 145\ nm$, respectively. Gates are separated by Si_3N_4 spacers, whose length is nominally equal to the gate one. The device has been tested in a dilution fridge from room temperature down to $T = 20\ K$. Static measurements of the drain current in linear regime ($|V_{DS}| = 50\ mV$) were performed sweeping the voltage on one gate (*active gate*), while keeping the other gates (*external gates*) at a fixed potential, namely $V_{G,ext} = -2\ V$. In such a way, the current was controlled by the active gate.

4.4.1 Electrical Characterization

Drain current $I_D(V_G)$ transfer characteristics for the five gates at room temperature are shown in Fig.(4.4.2).(a). From $I_D(V_G)$ curves, it is clear that each gate exhibits a different threshold voltage V_{th} and a different low field mobility μ_0. Furthermore, access resistance strongly affects the behavior of the device at high gate voltages. It is worth pointing out that here the access resistance comprehends the source/drain series resistances, the external gate channels and the regions underneath the spacers. In Fig.(4.4.2).(b), we plot the corresponding $Y - function$.

Both $I_D(V_G)$ and $Y(V_G)$ for different temperatures from $T = 300\ K$ to $T = 20\ K$ are presented in Fig.(4.4.3). Note the strong increase in the subthreshold slope as the temperature decreases (see also Fig.(4.4.4)), as well as the increase of both the threshold voltage and the drain current in strong inversion (typically for $|V_G|$ above 1 V). The latter is due to the increase of the mobility μ_0, consequence of the phonon number reduction at cryogenic temperatures, as confirmed by the $Y - function$ slope, steeper at lower temperatures. As it will be shown further, the increase of μ_0 and of

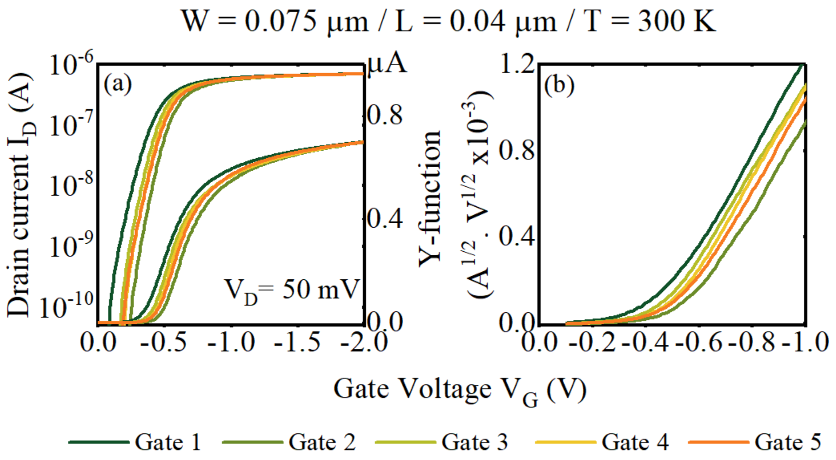

Figure 4.4.2 $I_D(V_G)$ (a) and $Y(V_G)$ (b) for every gate at $T = 300\ K$

the drain current accordingly, strongly depends on the proximity of source and drain. Indeed, different trends have been observed for different gates.

Concerning the subthreshold regime, the subthreshold swing SS, extracted at a fixed current value (vertical line in Fig.(4.4.4).(a)), follows the Boltzmann limit, before saturating to a value close to $SS = 20\ mV/dec$ (Fig.(4.4.4).(b)). The trend is the same independently of the gate, and it is caused by the potential fluctuations at the $Si - SiO_2$ interface as already explained.

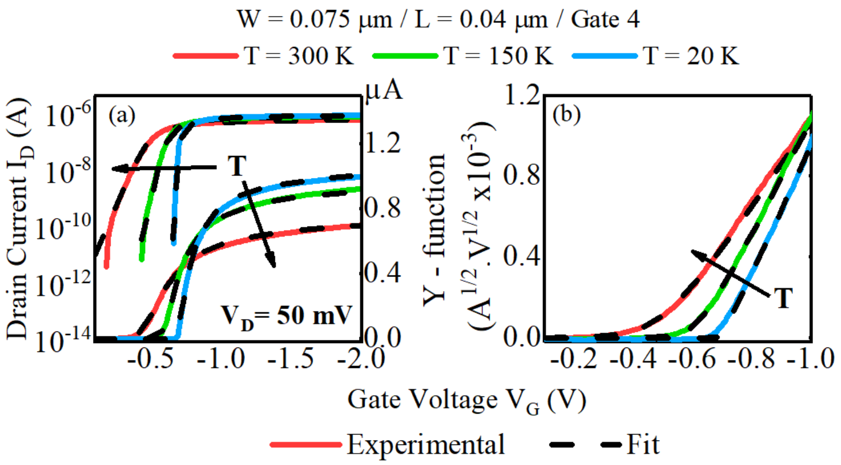

Figure 4.4.3 Experimental (straight lines) and fitted (dashed lines) $I_D(V_G)$ (a) and $Y(V_G)$ (b) curves at different temperatures.

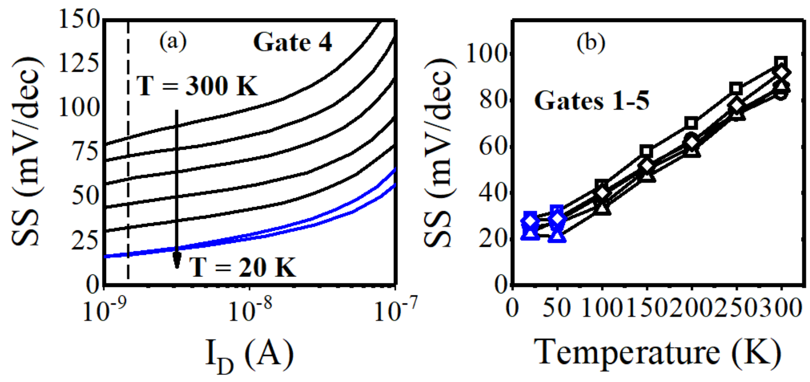

Figure 4.4.4 (a) $SS(I_D)$ for different temperatures extracted at a fixed current value (dashed line). Below $T = 100\ K$ it starts to saturate. (b) $SS(T)$ for all the five gates.

Exploiting eq.(4.3.10) one can extract both T_S and N_{it} for every gate (Fig.(4.4.5)). The critical temperature oscillates between $T_S = 60 - 80\ K$, which corresponds to a band tail width of $\Delta E \approx 5 - 7\ meV$. These values are slightly higher both than those of the larger FD-SOI device presented previously and also of those found for the 28nm FD-SOI technology [95]. It is worth to highlight that, knowing C_{ox} and C_b, the trap density can be extracted from the ideality factor, since $n = (C_{ox} + C_b + C_{it})/C_{ox}$. Comparing the values such extracted with those obtained using eq.(4.3.10), one can find good agreement (Fig.(4.4.5).(c). The trap density, in this case, is much higher than for the case of a large planar device, even if the technology is the same. This is likely linked to the more aggressive dimensions of the 5G device.

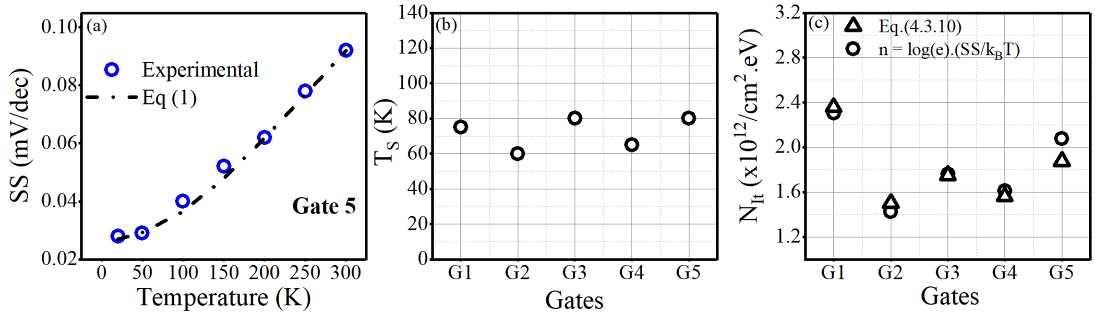

Figure 4.4.5 (a) Experimental (symbols) and fitted (dot-dashed line) subthreshold swing as function of temperature. (b) Critical temperatures as function of different gates. (c) Comparison of the interface trap density extracted with different methods.

4.4.2 Lambert W function – based modelling

We modeled the 5G device in linear operation with five independent gate-controlled resistances placed in series, whose values depend on V_G (active channel) and $V_{G,ext}$ (access channels). Each resistance is characterized by different intrinsic parameters, i.e. V_{th}, n and μ_0. The active channel resistance, corresponding to gate i, is given by**:**

$$R_{ch,i}\left(V_G, \mu_{0,i}, V_{th,i}, n_i\right) = \frac{L_G}{W_G \,.\, Q_{inv} . \, \mu_0} \qquad (4.4.1)$$

where $Q_{inv} = Q_{inv}(V_G, V_{th,i}, n_i)$ is the channel inversion charge given by the LW function. The access resistance is computed as:

$$\begin{aligned} R_{Acc}\left(V_{G,ext}\right) &= R_{ch,j}\left(V_G, \mu_{0,j}, V_{th,j}, n_j\right) + R_{ch,k}\left(V_G, \mu_{0,k}, V_{th,k}, n_k\right) \\ &+ R_{ch,l}\left(V_G, \mu_{0,l}, V_{th,l}, n_l\right) + R_{ch,m}\left(V_G, \mu_{0,m}, V_{th,m}, n_m\right) + R_{Series} \qquad (4.4.2) \end{aligned}$$

where $R_{ch,j}$, $R_{ch,k}$, $R_{ch,l}$, $R_{ch,m}$ are the channel resistances of gates i, j, k and l, and R_{Series} is an additional fitting parameter to take into account the contribution of source and drain access. Since the number of fitting parameters is quite high, each gate has been considered individually, allowing the extraction of the intrinsic parameters from $Y(V_G)$ and the subthreshold current. After, the access resistance has been automatically computed according to eq.(4.4.2), using R_{Series} as input parameter to fit $I_D(V_G)$ in strong inversion. It is worth noticing that no degradation mobility laws as function of V_G have been introduced to account for current saturation at high voltages, actually dominated by access resistance effect. It is worth to notice that this model can be generalized to devices with any number of gates, even if it must be considered that, increasing the number of gates, the number of fitting parameters increases accordingly. The fittings for both $I_D(V_G)$ and $Y(V_G)$ characteristics and for temperature varying from $T = 300\ K$ to $T = 20\ K$ are shown in Fig.(4.4.3).

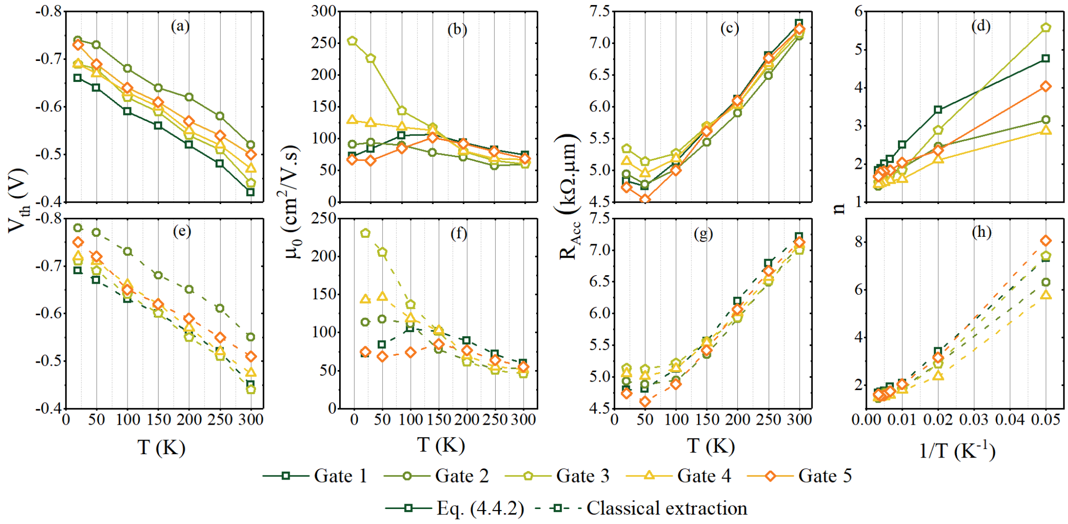

Figure 4.4.6 Parameters extracted for the every gate from room T down to $T = 20\ K$ using eq. (4.4.2) (a)–(d) and classical extraction methods (e)–(h).

The model successfully fits the drain current from subthreshold to strong inversion regime, allowing the extraction of the main device parameters (Fig.(4.4.6).(a)–(d)), whose values and trends are in good agreement with those extracted using classical methods. Indeed, both $V_{th}$and μ_0 have been extracted using the $Y - function$, while R_{Acc} has been derived from the expression of the first order attenuation factor $\theta_1 = \theta_{10} + R_{Acc} G_m$ [117], where θ_{10} is the intrinsic mobility reduction factor and $G_m = WLC_{ox}\mu_0$. θ_{10} has been neglected, since in such short channels the access resistance effect prevails. Finally, n has been extracted from the subthreshold swing according to eq.(4.4.2). The threshold voltage decreases quasi linearly with temperature (Fig.(4.4.6).(a),(e)), independently on the gate, whereas the ideality factor n varies nearly as $1/T$ below $T = 70 - 80\ K$ since SS is plateauing (Fig.(4.4.6).(d),(h)). The low field mobility (Fig.(4.4.6).(b),(f)), instead, shows different trends for different gates, revealing that the central device (gate 3) has a better mobility at low temperature. Exploiting the Mathiessen rule (eq.(2.3.2)) it is possible to have a the quantitative analysis of mobility behaviour (Fig.(4.4.7).(a)). It is clear from Fig.(4.4.7).(b) that, approaching the center of the channel, the scattering is driven by phonons, whereas closer to source and drain there is a similar impact of both phonons and neutral defects. These results are consistent with recent studies of mobility and transport in FD-SOI nano-devices, where it is shown that the scattering processes in highly scaled devices are led by source and drain neutral defects [65] [66].

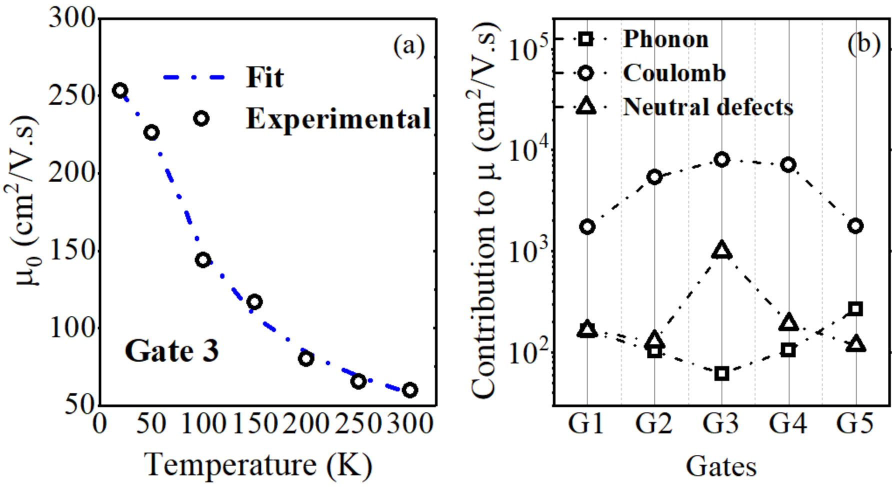

Figure 4.4.7 (a) Experimental (symbols) and simulated (dashed line) low field mobility as function of temperature. (b) Contribution of different scattering mechanisms to the total mobility.

Finally R_{Acc}, computed using eq.(4.4.2), also shows a linear decrease with temperature down to $T = 100\ K$, before saturating for temperature $T \leq 100\ K$. In Fig.(4.4.8) are plotted both R_{Series} and $R_\beta = R_{Acc} - R_{Series}$. The latter decreases down to $T = 100\ K$, then it increments again for almost all the gates. This is coherent with the definition given in eq.(4.4.1), since R_{ch} is inversely proportional to the low field mobility that has been shown to be not very sensitive to temperature. The behavior of R_{Acc} is therefore driven by R_{Series}, that shows a metallic-like trend versus temperature. It should be pointed out that, except for R_{Acc}, the values of the parameters extracted at room temperature are in line with standard FD-SOI MOSFET technology [72]. The highest value of both R_{Acc} and R_β below $T = 100\ K$ is found for gate 3, consistently with the mobility trend. Indeed, the resistance viewed from the other four gates is smaller because it includes the contribution of the central gate, which shows the highest mobility. For the same reason, the access resistance of gate 3 is the highest. It is worth highlighting that, with the exception of the central gate, the drain current increase at deep cryogenic temperature cannot be justified neither with an increased mobility nor a decreased R_β. Actually, it is mainly related to a reduction of R_{Series}.

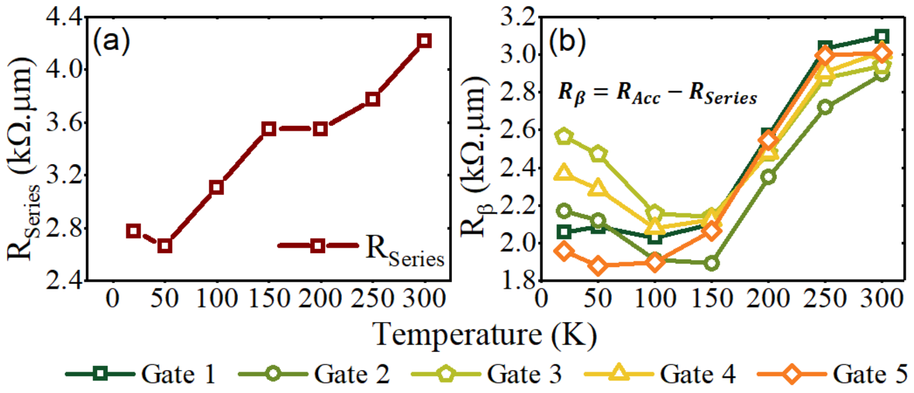

Figure 4.4.8 Series resistance R_{Series} (a) and R_β (b) down to $T = 20\ K$.

Numerical Simulations

Electrostatic and transport simulations of the 5G device have already been discussed in Chapter 2. Here, we would like to show how it is possible to take into account qualitatively the mobility gate dependence exhibited experimentally. The parabolic mobility profile displayed in Fig.(4.4.9).(a) was used in the simulations. The temperature was set to $T = 20K$, and three gates, namely Gate 1, Gate 3 and Gate 5, were compared in order to investigate the impact of the different mobility on the transport. For gates 1 and 5, both $I_D(V_G)$ and $Y(V_G)$ are identical (Fig.(4.4.9).(b),(c)), coherently with the shape of the mobility profile. The higher mobility of Gate 3 translates in an improved current above threshold and in a steeper $Y(V_G)$ slope. At high

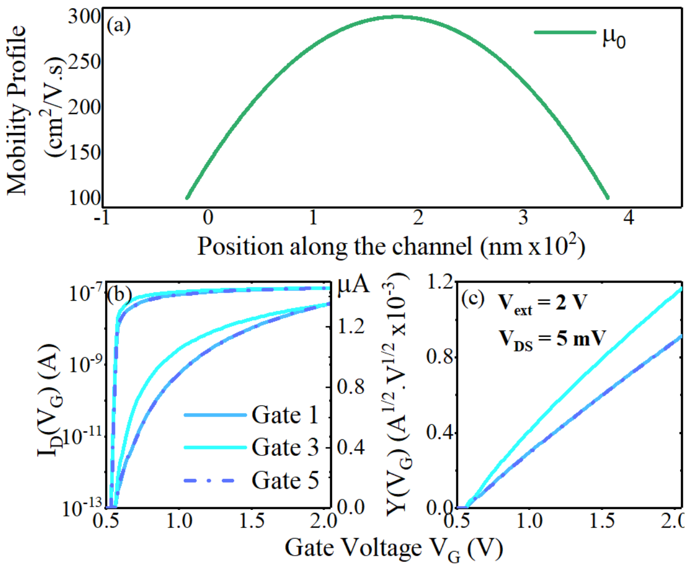

Figure 4.4.9 (a) Mobility profile used in the simulations shown in Fig. 11. $I_D(V_G)$ (b) and $Y(V_G)$ (c) simulated at $T = 20\ K$ with the parabolic mobility profile.

voltages, where the access resistances dominate the current, $I_D(V_G)$ get closer and finally joins the drain currents of gates 1 and 5.

4.5 MOBILITY FROM LINEAR TO SATURATION

We then compare the drain current characteristics in linear and saturation regime of a p-type single gate device (see section 3.4), from $T = 300\,K$ to $T = 10\,K$ (Fig.4.5.1). The channel length is $L_G = 50\,nm$, and the channel width is $W_G = 75\,nm$. At $V_{SD} = 50\,mV$, the current clearly decreases at low temperatures, as well as the mobility (Fig.(4.5.2).(a)). In saturation regime, on the other hand, the current shows an opposite behavior, since $I_D(V_G)$ curves tend to join at high voltages.

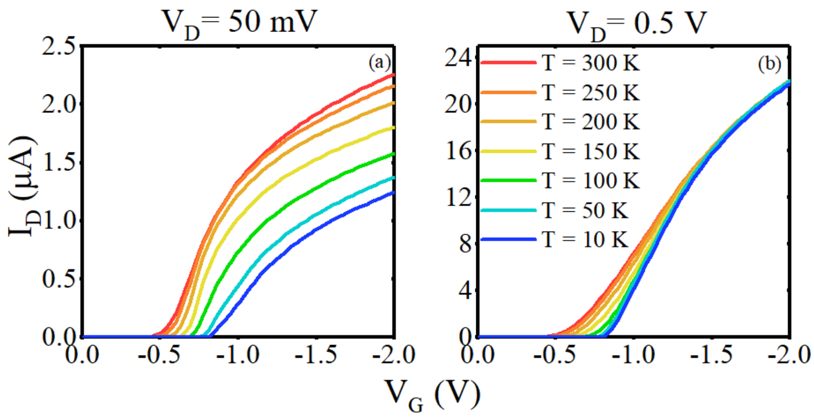

Figure 4.5.1 $I_D(V_G)$ from $T = 300\,K$ to $T = 10\,K$ in linear (a) and saturation (b) regime.

By extracting μ_0 with the $Y - function$ and using the Mathiessen rule (eq.(2.3.2)), it is easy to prove that this behaviour is due to Coulomb scattering (Fig.(4.5.2).(a)). Indeed, as already mentioned in section 3.3.2, Coulomb scattering reduces the low field mobility at cryogenic temperature.

$Y - function$ was also used to extract the mobility in saturation regime $\mu_{0sat} = \frac{\mu_0}{1+\frac{\mu_0 . V_D}{v_{sat} . L}}$, where v_{sat} is the saturation velocity [120] (Fig.(4.5.2).(b)). From μ_{0sat}, it is possible to calculate the saturation velocity as

$$v_{sat} = \frac{V_D . \mu_0}{L . \left(\frac{\mu_0}{\mu_{0sat}} - 1\right)} \qquad (4.5.1)$$

μ_{0sat} should be lower than μ_0, meaning that the saturation velocity should be positive. Indeed, at high longitudinal electric fields, carrier velocity saturation due to inter-valley and optical phonon scattering leads to a decrease of the mobility [121]. The saturation velocity at room temperature is $v_{sat} = 7.4.10^6\ cm/s$. Moreover, v_{sat} is expected to increase as the temperature is lowered down [122], but this is not the case for the example showed here (this behavior has been observed quite consistently within this technology). Indeed, by looking at Fig.(4.5.2), it is clear that $\mu_{0,sat} > \mu_0$ at cryogenic temperatures and, therefore, eq.(4.5.1) is not valid anymore (v_{sat} turned out to be negative, and this is physically meaningless).

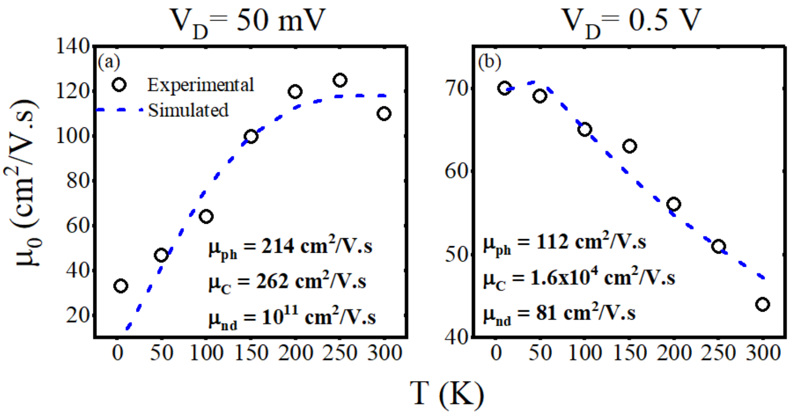

Figure 4.5.2 Experimental (symbols) and simulated (dashed line) low field mobility as function of temperature in linear (a) and saturation (b) regime.

The reason of this inconsistency is likely due to the unexpected low values of the mobility at cryogenic temperature. Indeed, to detriment μ_0 and, in turn, the current, contributes not only the Coulomb scattering, but also the non – ohmic behavior at low biases showed in Chapter 3 (Fig.(3.4.9)-(3.4.11)). Increasing the longitudinal electric field, i.e. V_D, carriers have more energy to overcome the potential barrier underneath the spacers, and the mobility increases accordingly.

4.6 CONCLUSION

In this chapter, we described the main MOSFET DC – characterization methods. Both the electrostatics and the transport of a large area FD – SOI device was characterized from $T = 300\ K$ down to $T = 10\ K$. Exploiting capacitance curves, the main physical quantities were extracted, such as inversion charge and gate oxide capacitance. With the inclusion of drain current characteristics, it was possible to plot mobility curves as function of inversion charge density, for different temperatures. The experimental curves have been finally modeled with the Lambert – W function, that allowed to extract the main devices parameters. Low field mobility and threshold voltage values such extracted were compared to those obtained through the $Y -$

$function$. Lambert – W function was also applied to unconventional five-gate device down to deep cryogenic temperatures. Here, an ad – hoc model was developed in order to fit and extract the main device's parameters. Indeed, the 5G device was modeled as a series of five independent resistances, each one characterized by a different set of intrinsic parameters. Moreover, particular emphasis was devoted to mobility and transport analysis. Indeed, it was demonstrated that the limiting scattering process in this technology was related to neutral defects, independently on the device length. Finally, the impact of high drain bias was discussed. The saturation velocity was extracted at room temperature, where the mobility in saturation regime is higher than in linear regime, whereas at cryogenic temperature no velocity saturation could have been computed with the classical formulation since it turned out to be negative and, therefore, physically meaningless. This behavior was attributed to the non-linearity characteristics of the qubit devices already discussed in the previous Chapter.

Chapter 5: Static and Dynamic Variability

5.1 INTRODUCTION

A massive production of qubits will be necessary for the future quantum processors. However, these qubits, to be functional, usually must be cooled down to a few tens of mK. Recently, spin based qubits operating above $1\ K$ have been demonstrated, raising this upper limit to a temperature range compatible with cryogenic systems offering cooling power order of magnitude higher [28] [29]. Measuring the physical properties of qubits at these very low temperatures is currently done on individual devices, and requires a lot of time, typically a few days per qubits [41] [47]. The preselection of qubit devices potentially functional from the physical and technological parameters measured at $T = 300\ K$ and down to $T = 4.2\ K$, using faster measurements and compatible with a quasi-industrial approach, remains a challenge [41] [47].

This chapter is devoted to static and dynamic variability of four-gate qubit MOS devices (4G). First, we focus on a statistical analysis at $T = 300\ K$, where 48 dies have been tested, applying two different values of external gates bias in order to explore its impact on the active channel. In this context, a matching analysis between the gates of the 4G devices is carried out. The average drain current and $Y - function$ characteristics have been reproduced using a Lambert – W function – based model. Indeed, it was assumed that the four-gate device could be modeled as a series of four identical transistors. The model was demonstrated to be able to fit also the matching curves. Afterwards, a dynamic variability study is performed on two 4G devices. Low frequency noise was measured both at $T = 300\ K$ and $T = 10\ K$. At room temperature, the noise clearly shows a $1/f$ behavior, whereas at cryogenic temperature some signatures of Lorenzian spectra are observed. In order to confirm the link between the observed spectra and the random telegraph noise (RTN), the drain current as function of time is presented. Moreover, it is demonstrated that the main noise sources are carrier number and mobility fluctuations. After, the average noise of all the eight gates tested is studied. It is shown that the drain current power spectrum decreases at cryogenic temperature. Finally, the model introduced in the static variability analysis is extended to time variability. Its effectiveness is demonstrated at both room and cryogenic temperature.

5.2 STATIC VARIABILITY AT ROOM TEMPERATURE

The importance of room temperature characterization of qubit devices relies on technological benchmarking. To alleviate the onerous process of cryogenic measurements, a previous screening of devices can be performed at room temperature. Therefore, technology optimization is compelling to make such approach feasible. In fact, characterization and modelling of MOS devices at deep cryogenic temperatures are mostly performed on mature technologies [52] [80] [123] [124].

5.2.1 Theoretical Background

Drain current local variability is one of the critical problems in nanoscale devices. Local variability analysis, or matching analysis, consists in comparing the current of two nominally identical devices. The main variability sources for FD – SOI devices were identified in threshold voltage V_{th}, current gain factor $\beta = \frac{W_G}{L_G}.\mu_0$ and access resistance R_{Acc} [125]. In order to develop a model able to take into account all the main variability sources, let us consider the first order Taylor approximation of the drain current [125] [126]:

$$\frac{\Delta I_D}{I_D} = \left(\frac{1}{I_D}.\frac{\partial I_D}{\partial V_{th}}\right).\Delta V_{th} + \left(\frac{1}{I_D}.\frac{\partial I_D}{\partial \beta}\right).\Delta\beta + \left(\frac{1}{I_D}.\frac{\partial I_D}{\partial R_{Acc}}\right).\Delta R_{Acc} \tag{5.2.1}$$

where $\frac{\Delta I_D}{I_D}$ is the relative difference between the drain currents of two identical devices, ΔV_{th}, $\Delta\beta$ and ΔR_{Acc} are the threshold voltage, current gain factor and access resistance mismatches, respectively. It is worth noticing that eq.(5.2.1) corresponds to the error propagation formula for the drain current. The derivatives in eq.(5.2.1) can be calculated by expressing the drain current as $I_D(V_G) = G_d.V_D$, where G_d is the device conductance [125]:

$$G_d = \frac{G_{d0}}{1 + G_{d0}.R_{Acc}} = \frac{\beta.Q_{inv}}{1 + \beta.Q_{inv}.R_{Acc}} \tag{5.2.2}$$

where G_{d0} is the intrinsic channel conductance and Q_{inv} is given by the Lambert – W function. Mobility attenuation factors have been neglected in eq.(5.2.2) for the sake of simplicity, but their inclusion would not affect the final result. From eq.(5.2.2)

$$\frac{1}{I_D}.\frac{\partial I_D}{\partial V_{th}} = -\frac{g_m}{I_D} \tag{5.2.3}$$

$$\frac{1}{I_D}.\frac{\partial I_D}{\partial \beta} = \frac{1}{(1+\beta.Q_{inv}.R_{Acc}).\beta} = \frac{1-G_d.R_{Acc}}{\beta} \tag{5.2.4}$$

$$\frac{1}{I_D}.\frac{\partial I_D}{\partial R_{Acc}} = \frac{\beta.Q_{inv}}{(1+R_{Acc}.Q_{inv}.\beta)} = G_d \tag{5.2.5}$$

Eq.(5.2.3) is obtained assuming that the drain current is function of the gate overdrive voltage $V_{OV} = V_G - V_{th}$ and not of V_G and V_{th} separately [126]. From eq.(5.2.1) and eqs.(5.2.3)-(5.2.5), it is possible to express the drain current variance as [125]

$$\sigma\left(\frac{\Delta I_D}{I_D}\right)^2 = \left(\frac{g_m}{I_D}\right)^2 \sigma(\Delta V_{th})^2 + (1-G_d.R_{Acc})^2.\sigma\left(\frac{\Delta\beta}{\beta}\right)^2 + G_d.\sigma(\Delta R_{Acc})^2 \tag{5.2.6}$$

where $\sigma\left(\frac{\Delta I_D}{I_D}\right)$, $\sigma(\Delta V_{th})$, $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ and $\sigma(\Delta R_{Acc})$ are the drain current, threshold voltage, current gain factor and access resistance standard deviations, respectively.

Eq.(5.2.6) does not include the subthreshold slope variability. It is possible to extend eq.(5.2.1) to include all the main sources of variability [127]:

$$\begin{aligned}\sigma\left(\frac{\Delta I_D}{I_D}\right)^2 &= \left(\frac{g_m}{I_D}\right)^2 \sigma(\Delta V_{th})^2 + (1-G_d.R_{Acc})^2.\sigma\left(\frac{\Delta\beta}{\beta}\right)^2 + G_d.\sigma(\Delta R_{Acc})^2 \\ &+ \left[\ln\left(\frac{I_D}{I_{Dth}}\right)\right]^2.\left[\exp\left(-\frac{I_{Dth}}{I_D}\right)-1\right]^2.\frac{\sigma(\Delta n)^2}{n^2}\end{aligned} \tag{5.2.7}$$

where I_{Dth} is a constant current factor near threshold. SS variability is accounted for the ideality factor n.

Eq.(5.2.7) contains four variability sources. Since $Y-function$ is immune to the effect of the access resistance, we can consider also its variability, which will embody just three matching parameters, and repeat the same calculations we did for $\sigma\left(\frac{\Delta I_D}{I_D}\right)$. In such a way, the $Y-function$ variance reads [125] :

$$\begin{aligned}\sigma\left(\frac{\Delta Y}{Y}\right)^2 &= \beta.\frac{\sigma(\Delta V_{th})^2}{4.\beta.n^2.\left(\frac{k_B.T}{q}\right)^2 + Y^2} + \frac{1}{4}.\sigma\left(\frac{\Delta\beta}{\beta}\right)^2 \\ &+ \left[\ln\left(\frac{I_D}{I_{Dth}}\right)\right]^2\left[\exp\left(-\frac{I_{Dth}}{I_D}\right)1\right]^2.\frac{\sigma(\Delta n)^2}{n^2}\end{aligned} \tag{5.2.8}$$

5.2.2 Devices and Experimental Details

Here, we present a complete room temperature electrical and statistical characterization of n-type four-gate MOS qubit devices (Fig.(5.2.1)). Devices' channel length varies from $L_G = 40\ nm$ to $L_G = 60\ nm$, whereas the channel top view width is $W_G = 70\ nm$. The silicon body and BOX thickness are $t_{Si} = 9.8\ nm$ and $t_{BOX} = 145\ nm$, respecively. The SiO_2 gate oxide is 6 nm thick.

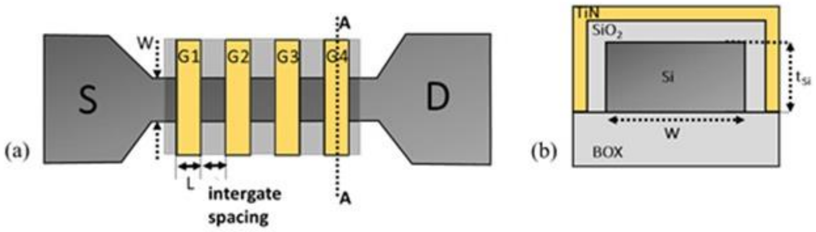

Figure 5.2.1 (a) 4G device top-view schematic. (b) AA cross-section view.

Static measurement of drain current I_D were performed on 48 dies all around the wafer sweeping the voltage on one gate (*active gate*), while keeping the other gates (*external gates*) at a fixed value. In order to investigate the impact of gate crosstalk on the active channel, two external voltages were set: $V_{G,ext} = 1\ V$ and $2\ V$. The measurements were performed in linear region ($V_D = 50\ mV$).

5.2.3 Electrical Characterization – Mean Characteristics

$I_D(V_G)$ characteristics of 48 dies are plotted in Fig.(5.2.2) for different $V_{G,ext}$. Average $I_D(V_G)$ calculated over 48 curves for the four active gates are compared in Fig.(5.2.3).(a). It is worth noting that all curves show similar behaviours, whatever the

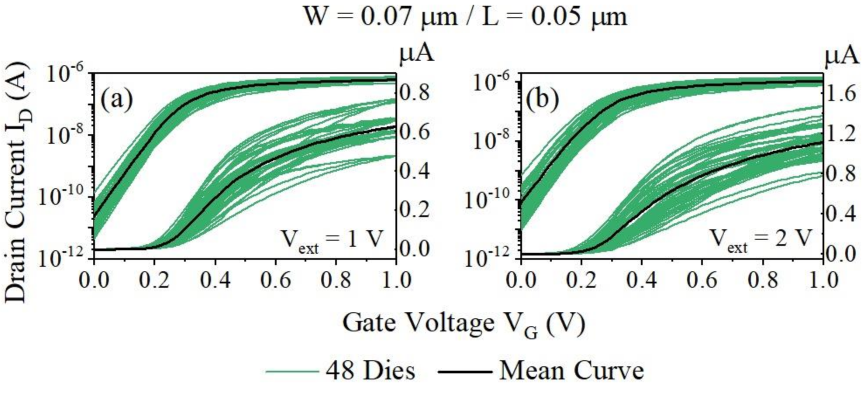

Figure 5.2.2 $I_D(V_G)$ characteristics of 48 dies (green) and mean values (black), both for $V_{G,ext} = 1\ V$ (a) and $V_{G,ext} = 2\ V$ (b).

active gate, with small differences between them only for high V_G. This trend was confirmed by simulating an ideal 4G structure (see next paragraph). Similarly, $Y(V_G)$ characteristics of each active gate (Fig.(5.2.3).(b)) also show very close behaviour. This clearly indicates that the 4G transistors are almost identical on average and that, in first instance, they can be modeled as the series combination of 4 identical transistors.

The $I_D(V_G)$ and $Y(V_G)$ curve dependence with external voltage was also explored in Fig.(5.2.3). The drain current is enhanced for higher $V_{G,ext}$, which could be expected as a higher $V_{G,ext}$ decreases the resistance of the channel underneath and so the overall access resistance.

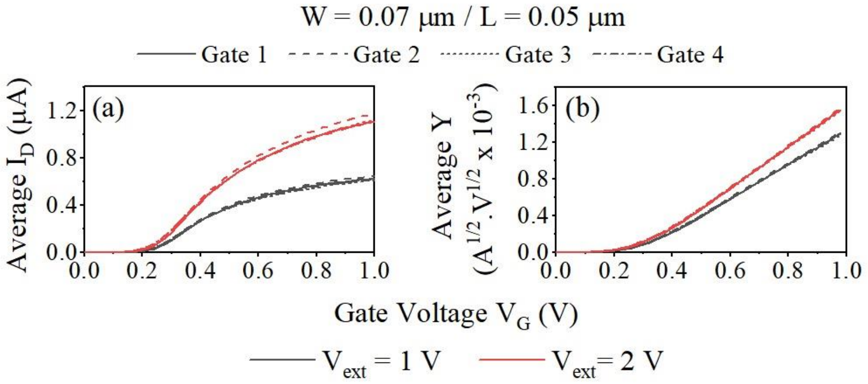

Figure 5.2.3 (a) Comparison among mean $I_D(V_G)$ characteristics computed over 48 curves collected by sweeping different gates. (b) Corresponding mean $Y - functions$ from different active gates

Interestingly, the slope of the linear part of $Y(V_G)$ above threshold voltage, which is given by

$$\frac{dY_i}{dV_{G,i}} = \sqrt{\frac{W}{L_{eff,i}} C_{ox,i}.\mu_{0,i}.V_D} = \beta^{\frac{1}{2}} \qquad (5.2.9)$$

is also enhanced for higher $V_{G,ext}$. In eq.(5.2.1), i stands for the $i-th$ gate, β is the current gain factor in strong inversion and $L_{eff} = L_G(V_{G,ext} = 1\,V)$ is the effective channel length. This slope increase could be related to *(i)* an increase of the electron mobility in the active channel or *(ii)* more likely to a decrease of the effective channel length $L_{eff,i}$, due to the electrostatic effect induced by the external gates. Considering the first assumption, an increase of $V_{G,ext}$would lead to a higher electric field inside the channel that should result in a decrease of mobility, in contrast with what was observed experimentally. Numerical simulations have been performed with FlexPDE to point out the effect of $V_{G,ext}$. A constant mobility value $\mu_0 = 100\,\frac{cm^2}{V.s}$ was used, in order to verify the hypothesis *(ii)*. In Fig. (5.2.4).(a),(b) are reported the simulated $I_D(V_G)$ and $Y(V_G)$, respectively, for different gates at different $V_{G,ext}$.

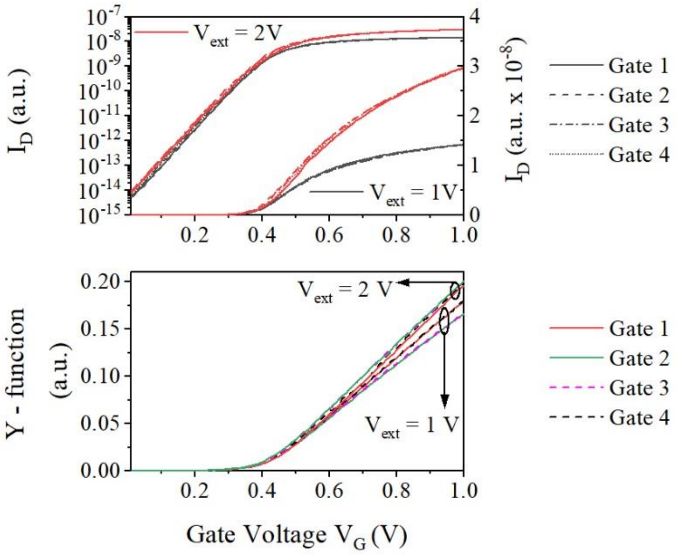

Figure 5.2.4 Simulated $I_D(V_G)$ in linear and log scale (a) and $Y-function$ (b) as a function of V_G for different active gates and different $V_{G,ext}$ values.

As in experimental curves, $I_D(V_G)$ does not depend on the active gate i considered, and increases above threshold with $V_{G,ext}$. Simulated $Y(V_G)$ overall exhibit a global dependence with $V_{G,ext}$, in agreement with what is observed in experiments (Fig.(5.2.3)). Nevertheless, simulated $Y(V_G)$ curves reveal an additional trend not present in the experimental ones i.e., at $V_{G,ext} = 1\,V$, the slope of $Y(V_G)$ shows a slight gate dependence. It is higher for G1 and G4 (see Fig.(5.2.1)), meaning that L_{eff} for these active gates is smaller, since μ_0 has a fixed constant value. A possible explanation is that, when $V_{G,ext} = 1\,V$, the influence of the built-in potential V_{bi} on the outer gates is more significant, due also to the greater proximity of S/D with respect to the nearest neighbour gates, whereas at higher $V_{G,ext}$ it is likely overcame by the surrounding gate potential. Thus, in the ideal case, G1-G4 and G2-G3 should be identical.

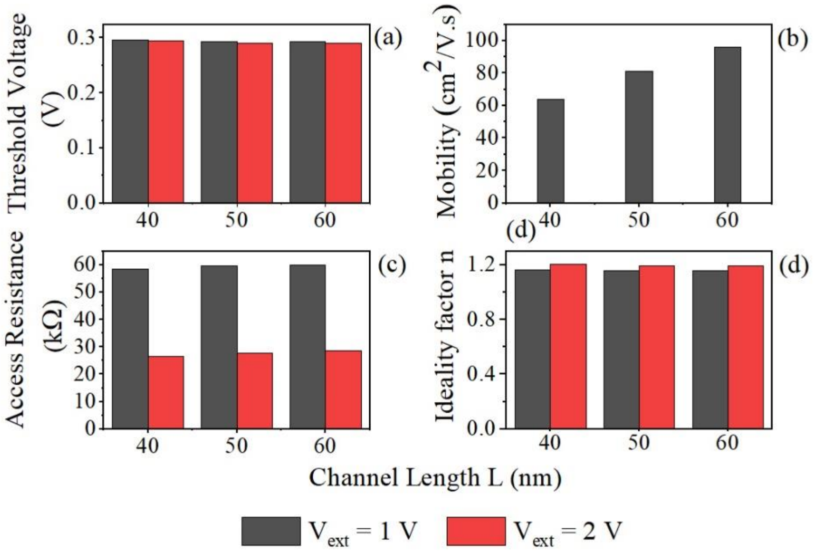

Figure 5.2.5 Mean values of the parameters extracted through $Y - function$ method for different gate lengths and different $V_{G,ext}$.

Four figures of merit were extracted, averaged over all the 48 devices and over all the active gates i, and plotted as a function of the gate length and of $V_{G,ext}$ (Fig.(5.2.5)): V_{th}, μ_0, R_{Acc} and n. We first observe that V_{th} slightly changes with $V_{G,ext}$ and L_G. The decrease of μ_0 with channel length reduction is a phenomenon commonly observed in standard FD – SOI MOSFETs [67], [68], likely due to neutral defects scattering [65], [66]. As discussed previously, R_{Acc} is greatly reduced at higher $V_{G,ext}$. It is worth pointing out that the access resistance has been extracted directly from the first order mobility attenuation factor $\theta_1 = \theta_{10} + R_{Acc}.G_m$. Also in this case, as already mentioned, θ_{10} has been neglected since the channel resistance is much smaller than the access one. Finally, the ideality factor undergoes only a slight increase with $V_{G,ext}$. It should be emphasized that all the extracted parameters values, except for those of R_{Acc}, are in line with the standard FD – SOI MOSFET technology [72].

5.2.4 Electrical Characterization – Matching Analysis

In the previous paragraph it was shown that, starting from mean $I_D(V_G)$ curves, it is possible to infer that the active channels of the 4G device are approximately identical at the same gate voltage. To better capture this behaviour, drain current matching analysis was performed. In standard MOSFETs, this is carried out by comparing two identical devices, spaced by the minimum allowed distance and place in identical environment. Here, drain current and $Y - function$ variability between gates of the same device was explored.

Drain current mismatch (Fig.(5.2.6).(a)) is defined using the logarithmic difference as [128], [127], [129],

$$\frac{\Delta I_D}{I_D} = \ln\left(\frac{I_{D,i}}{I_{D,j}}\right) \tag{5.2.10}$$

where $I_{D,i}$ and $I_{D,j}$ are the currents controlled by gate i and j, respectively. Eq.(5.2.10) was also used to calculate $Y(V_G)$ mismatch (Fig.(5.2.6).(b)).

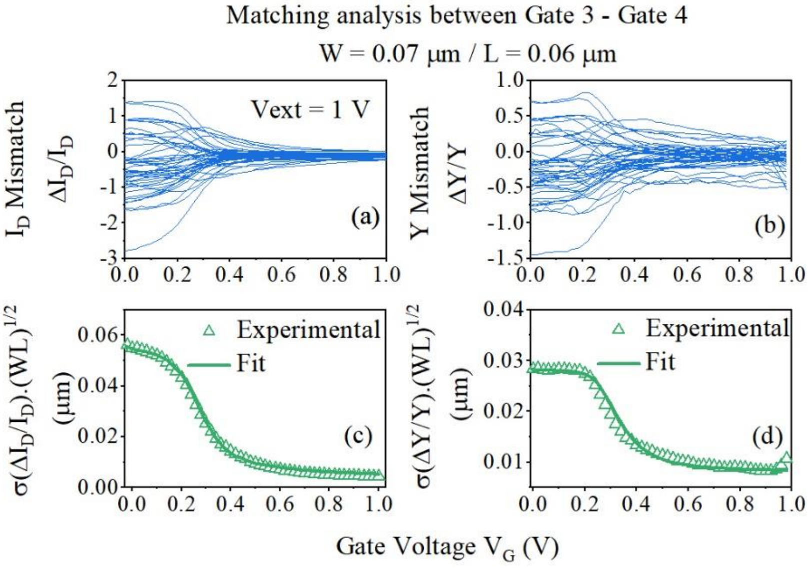

Figure 5.2.6 (a) $\frac{\Delta I_D}{I_D}$ and (b) $\frac{\Delta Y}{Y}$ for 48 devices. Experimental (symbols) and fitted (lines) (c) $\sigma\left(\frac{\Delta I_D}{I_D}\right)$ and (d) $\sigma\left(\frac{\Delta Y}{Y}\right)$.

In order to quantify drain current and Y variations, standard deviations of their mismatches $\sigma\left(\frac{\Delta I_D}{I_D}\right)$ and $\sigma\left(\frac{\Delta Y}{Y}\right)$ were computed, normalized by $(W_G.L_G)^{\frac{1}{2}}$ (Fig.(5.2.6).(c),(d), symbols). These quantities were fitted (Fig.(5.2.6).(c),(d), lines) using eq.(5.2.7) and eq.(5.2.8). It is worth pointing out that the channel length variability is taken into account by $\sigma\left(\frac{\Delta\beta}{\beta}\right)$, which will be shown to have a big impact in strong inversion, confirming the previous comments about $V_{G,ext}$ dependence of the effective channel length. Since $Y(V_G)$ is immune to the access resistance, $\sigma\left(\frac{\Delta Y}{Y}\right)$ was fitted first, extracting $\sigma(\Delta V_{th})$, $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ and $\sigma(\Delta n)$. The values found were then used to fit $\sigma\left(\frac{\Delta \mathrm{I_D}}{I_D}\right)$ with the additional fitting parameter $\sigma(\Delta R_{Acc})$.

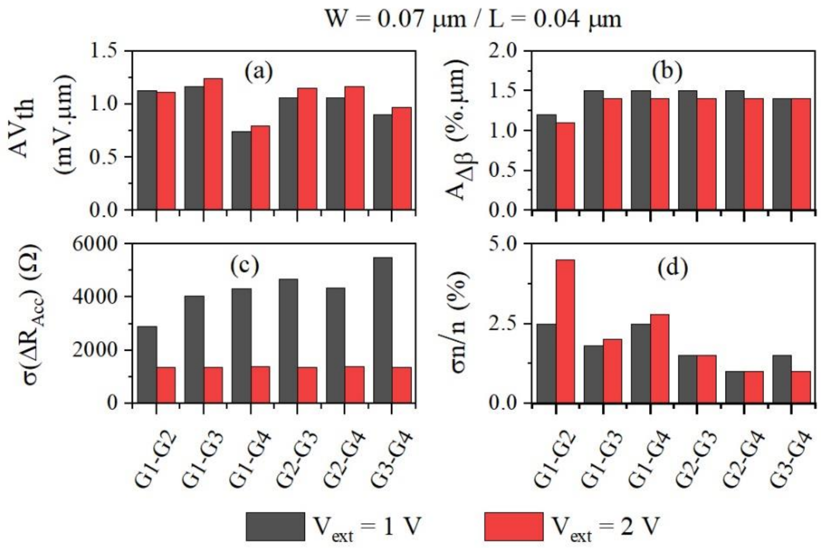

Figure 5.2.7 Matching parameters obtained using eqs.(5.2.3)-(5.2.4).

In Fig.(5.2.7) are reported the values of the matching parameters as function of active gates 2-by-2 comparison ($AV_{th} = \sigma(\Delta V_{th}).\sqrt{W.L_G}$, $A_{\Delta\beta} = \sigma(\Delta\beta/\beta).\sqrt{W.L_G}$ [130]). AV_{th} exhibits values around 1 $mV.\mu m$, which is close to the state-of-the-art for undoped film CMOS technologies [128], [131], [132]. $A_{\Delta\beta}$ is almost 50% larger than typical state-of-the-art values [128]. Both AV_{th} and $A_{\Delta\beta}$ confirm the quality of these 4G devices, that is close to the state-of-the-art 28nm FD – SOI technology. It should also be noted that $\sigma(\Delta\beta/\beta)$ includes the contribution of L_{eff} variability, which is, as already mentioned, very sensitive to external gate voltage and potential fluctuations in the spacers. This could explain the increase of $\sigma(\Delta\beta/\beta)$ as compared to the state-of-the-art 28nm FD – SOI results. Finally, $\frac{\sigma(\Delta n)}{n}$ has values in line with those of standard FD – SOI MOSFET 14nm technology [129].

Based on eq.(5.2.7), the percentage contribution of main variability sources of the total current mismatch has been computed and is shown in Fig.(5.2.8). It can be observed that $\sigma(\Delta V_{th})$ has the largest impact in subthreshold region, as expected. Instead, $\sigma(\Delta\beta/\beta)$ is predominant in strong inversion; its contribution is even larger for higher $V_{G,ext}$, where the R_{Acc} contribution is reduced since the access transistors are less resistive.

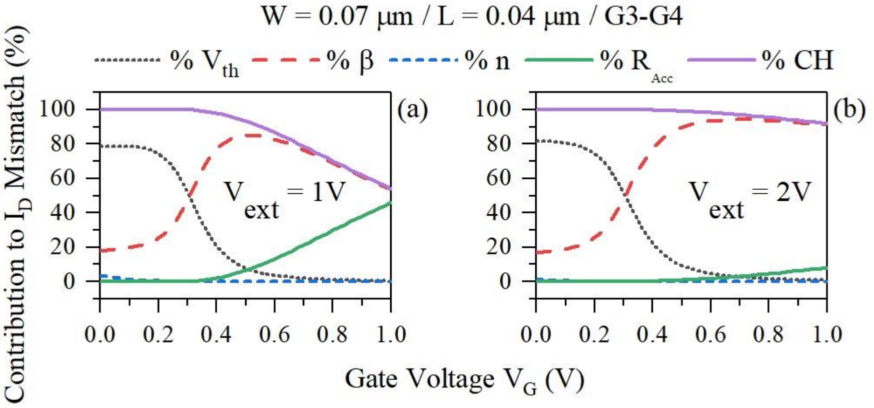

Figure 5.2.8 Percentage contribution of the main variability sources to current mismatch for $V_{G,ext} = 1\ V$(a) and $V_{G,ext} = 2\ V$ (b).

Another interesting parameter in mismatch analysis is the so-called input referred normalized matching parameter, given by

$$iA\Delta V_G = \left(\frac{\sigma\left(\frac{\Delta I_D}{I_D}\right)}{\frac{g_m}{I_D}} \right) \sqrt{W_G . L_G} \tag{5.2.11}$$

It is a concept borrowed from noise analysis, and specifically from equivalent input gate voltage spectral density, as we will show later. $iA\Delta V_G$ corresponds to the equivalent gate voltage variability of the external variability sources that one has to put on the gate in order to induce the same drain current variability. It is plotted in Fig.(5.2.9). At low V_G, $iA\Delta V_G$ shows a plateau, whose value is approximately given by $\sigma(\Delta V_{th})$. Increasing the gate voltage, the contribution of other variability sources starts to be significant. The raising difference among gates at high V_G might be due to variability in technological processes. In particular, the smallest impact is observed

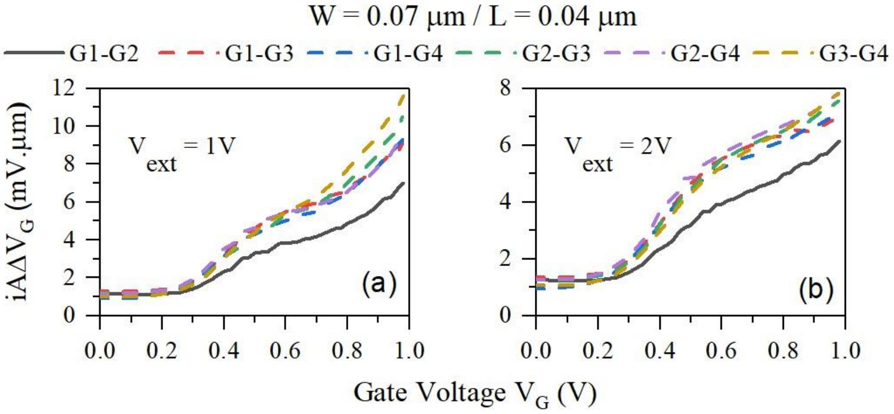

Figure 5.2.9 Input referred normalized matching parameter between all the gates of a 4G device and for different external voltages.

between G1 and G2. At $V_{G,ext} = 2\,V$, $iA\Delta V_G$ shows a reduction in strong inversion, which is a consequence of the decrease of $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ and, in particular, of $\sigma(\Delta R_{Acc})$ (Fig.(5.2.7).(b),(c)). Thus, the increase of the external voltage results in an improvement of the mismatch between gates, because the access transistors are more conductive.

5.2.5 Lambert Function – based modeling

Based on the characterization results previously discussed, our modeling assumes that the 4G transistor can be modeled in linear operation with four identical and independent gate controlled resistances placed in series, whose values depend on V_G (active channel) and $V_{G,ext}$ (series channels), as,

$$R_{Acc}\left(V_{G,ext}\right) = 3.R_{ch}\left(V_{G,ext}\right) + R_{Series} \tag{5.2.12}$$

$$R_{tot}\left(V_G, V_{G,ext}\right) = R_{ch}(V_G) + 3.R_{ch}\left(V_{G,ext}\right) + R_{Series} \tag{5.2.13}$$

where $R_{tot}\left(V_G, V_{G,ext}\right)$ is the total 4G resistance. R_{Series} is an additional fitting parameter that allows to consider external resistance contribution, i.e. a fixed contribution from source and drain access. As will be shown, this contribution becomes important at high $V_{G,ext}$. The single channel resistance R_{ch} is given by:

$$R_{ch}(V_G) = \frac{L_G}{W_G.Q_{inv}(V_G).\mu_0} = \frac{V_D.C_{ox}}{\beta.Q_{inv}(V_G)} \tag{5.2.14}$$

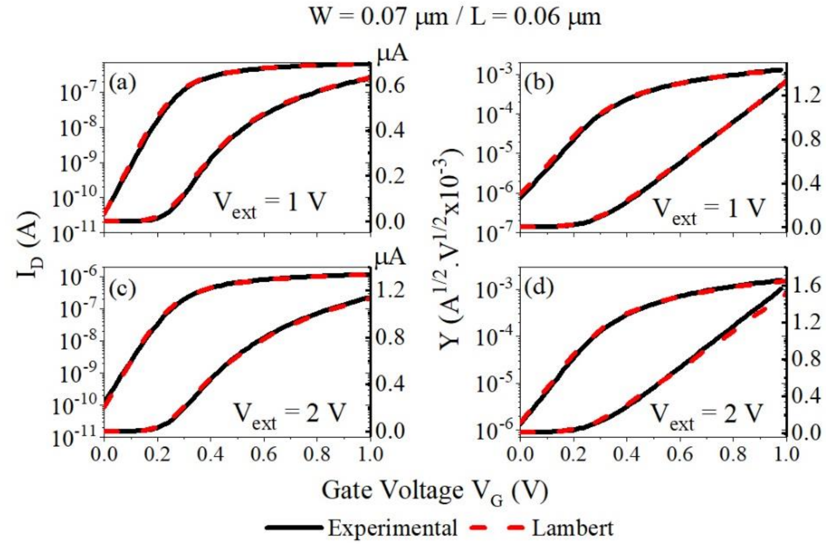

Figure 5.2.10 (a)-(c) Experimental (straight black line) and fitted (dashed red line) $I_D(V_G)$. (b)-(d) Experimental (straight black line) and fitted (dashed red line) $Y(V_G)$.

where Q_{inv} is given by eq.(3.2.5). As can be seen from Fig.(5.2.10), very good $I_D(V_G)$ and $Y(V_G)$ fits can be achieved with the Lambert function based model over the entire V_G range and for different $V_{G,ext}$.

At $V_{G,ext} = 1\ V$ the value of R_{Series} is found to be negligible (≈0), for all the channel lengths and for all the gates considered. This trend is confirmed in Fig.(5.2.11).(c), where R_{Acc} extracted from $Y - function$ and Lambert modelling are compared for a device with $L_G = 40\ nm$: their values are almost identical, meaning that the main contribution to R_{Acc} actually comes from the series transistor channels. Concerning the other extracted parameters, the values fall in good agreement within 15% of change, inherent to the difference in extraction methodology.

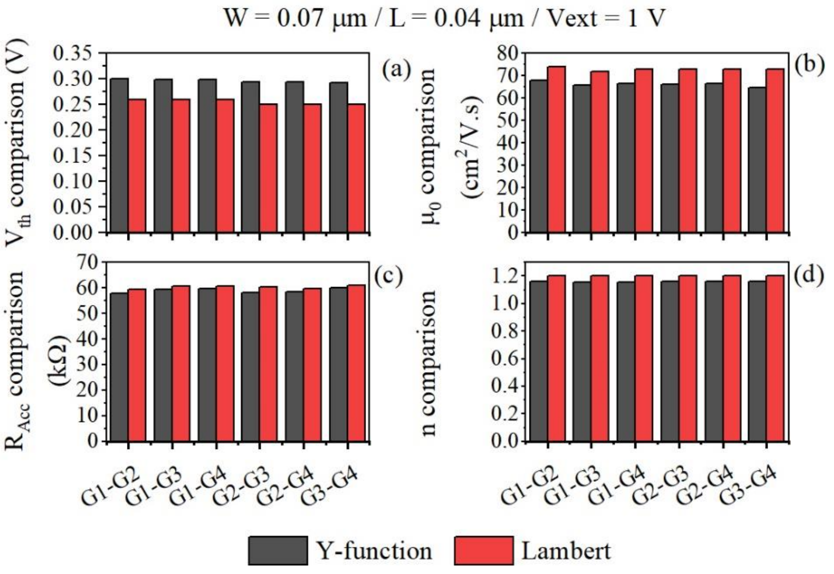

Figure 5.2.11 Comparison between parameters extracted through $Y - function$ and Lambert methods.

When the external voltage is increased to $V_{G,ext} = 2\ V$, the access transistors are less resistive and the external resistance contributes significantly to the total access resistance. In Fig.(5.2.12).(a) it is shown the comparison between R_{Acc} extracted with the Lambert function with a fixed $R_{Series} = 8\ k\Omega$ and that extracted with $Y - function$ method. The values are in good agreement, and the contribution of the external resistance to the total R_{Acc} is around 30%. It is worth underlining that, whereas for $V_{G,ext} = 1\ V$, μ_0 was used to fit both $I_D(V_G)$ and $Y(V_G)$ considering the nominal values for all the other parameters appearing in the second term of eq.(5.2.14), in the case of $V_{G,ext} = 2\ V$, β was directly used as fitting parameter. From the latter, assuming μ_0 to be constant in $V_{G,ext}$, it is possible to extract the effective channel length $L_{eff}(V_{G,ext} = 2\ V)$:

$$L_{eff} = \frac{W_G . C_{ox} . \mu_0 . V_D}{\beta\left(V_{G,ext} = 2\ V\right)} \tag{5.2.15}$$

where μ_0 has been extracted from $\beta(V_{G,ext} = 1\ V)$.

In Fig.(5.2.12).(b) are reported the L_{eff} variations from the nominal length L_G for every gate i and $L_G = 40, 50$ and $60\ nm$. At fixed dimension, no significant difference is found between each active gate. The effective gate length decrease is almost independent from device dimension and it is around 30%.

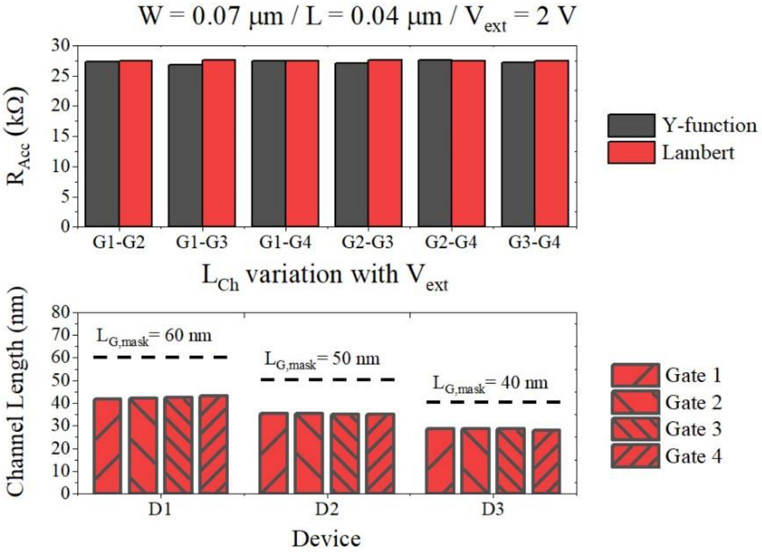

Figure 5.2.12 (a) Comparison between R_{Acc} values extracted through $Y - function$ and Lambert model at $V_{G,ext} = 2\ V$. (b) Channel length variation from nominal value at $V_{G,ext} = 2\ V$ for different gates and dimensions.

Matching modelling

The matching analysis of the 4G transistor can also be carried out using the Lambert function – based model, with eqs.(5.2.12) - (5.2.14). Since the variance of uncorrelated resistances in series is the sum of their variances, we have:

$$var\left(R_{Acc}\left(V_{G,ext}\right)\right) = 3.\, var\left(R_{ch}\left(V_{G,ext}\right)\right) + var\left(R_{Series}\right) \tag{5.2.16}$$

$$\begin{aligned} var\left(R_{tot}\left(V_G, V_{G,ext}\right)\right) &= var\left(R_{ch}\left(V_G\right)\right) \\ &+3.\, var\left(R_{ch}\left(V_{G,ext}\right)\right) + var\left(R_{Series}\right) \end{aligned} \tag{5.2.17}$$

Within the Lambert function approach, the variance of a single transistor can be calculated using the first order Taylor approximation:

$$var\left(\frac{\Delta R_{ch}}{R_{ch}}\right)(V_G) = \left(\frac{1}{R_{ch}}\frac{dR_{ch}}{dV_G}\right)^2 .\sigma(\Delta V_{th})^2 + \sigma\left(\frac{\Delta\beta}{\beta}\right)^2 + \left(\frac{1}{R_{ch}}\frac{\delta R_{ch}}{\delta n}\right)^2 .\sigma(\Delta n)^2 \qquad (5.2.18)$$

Therefore, the mismatch of the whole resistance and, by turn, of the drain current $\sigma\left(\frac{\Delta I_D}{I_D}\right) = \sigma\left(\frac{\Delta R_{tot}}{R_{tot}}\right)$ is thus obtained from eqs.(5.2.16)-(5.2.18) as:

$$\sigma\left(\frac{\Delta I_D}{I_D}\right)^2 (V_G, V_{G,ext}) = var\left(\frac{\Delta R_{ch}}{R_{ch}}\right)(V_G).\frac{R_{ch}(V_G)^2}{R_{tot}\left(V_G, V_{G,ext}\right)^2} + \frac{3.var\left(\frac{\Delta R_{ch}}{R_{ch}}\right)\left(V_{G,ext}\right)R_{ch}\left(V_{G,ext}\right)^2}{R_{tot}\left(V_G, V_{G,ext}\right)^2} + \frac{var\left(\frac{\Delta R_{Series}}{R_{Series}}\right)R_{Series}^2}{R_{tot}\left(V_G, V_{G,ext}\right)^2} \qquad (5.2.19)$$

This Lambert function based matching model has been used to fit the 4G device drain current mismatch data as illustrated in Fig.(5.2.13). Note that a good agreement with global matching model of eq.(5.2.7) and experiment can be achieved. At $V_{G,ext} = 1\,V$ (Fig.(5.2.13).(a)), $R_{Series} \approx 0$, meaning that only 3 matching parameters are needed,

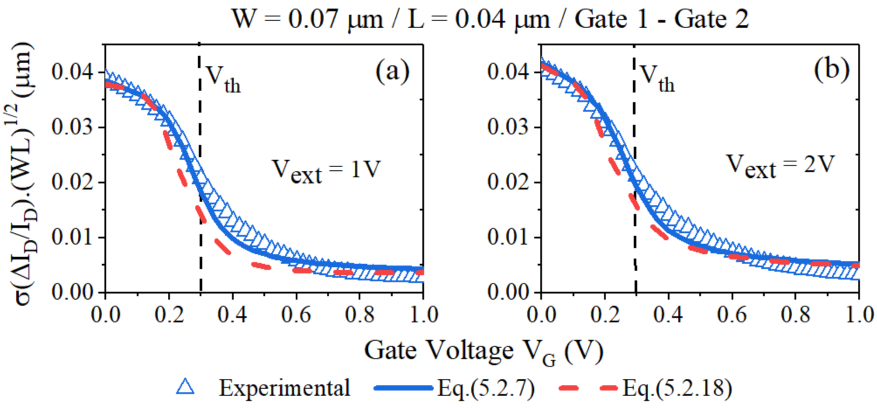

Figure 5.2.13 $\left(\frac{\Delta I_D}{I_D}\right)$ variation with gate voltage. Comparison between global matching model of eq.(5.2.7) and Lambert-based matching model of eq.(5.2.18) at (a) $V_{G,ext} = 1\,V$ and (b) $V_{G,ext} = 2\,V$.

i.e. $\sigma(\Delta V_{th})$, $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ and $\sigma(\Delta n)$. Indeed, here in the Lambert approach, there is no need to use access resistance R_{Acc} and standard deviation $\sigma(\Delta R_{Acc})$ additional parameters as they are included in the access transistors.

At $V_{G,ext} = 2\ V$ (Fig.(5.2.13).(b)), instead, the standard deviation of the series resistance must be taken into account. In this case, the Lambert model relies again on four matching parameters, but it provides a more insightful characterization, since it allows to separately quantifying the contribution of the series and the transistor related resistances. It is worth to underling that, in order to verify the consistency of the two models, the value of $\sigma(\Delta R_{Acc})$ used in the fits of Fig.(5.2.13) was the same and it was derived directly from eq.(5.2.16) (Fig.(5.2.14)).

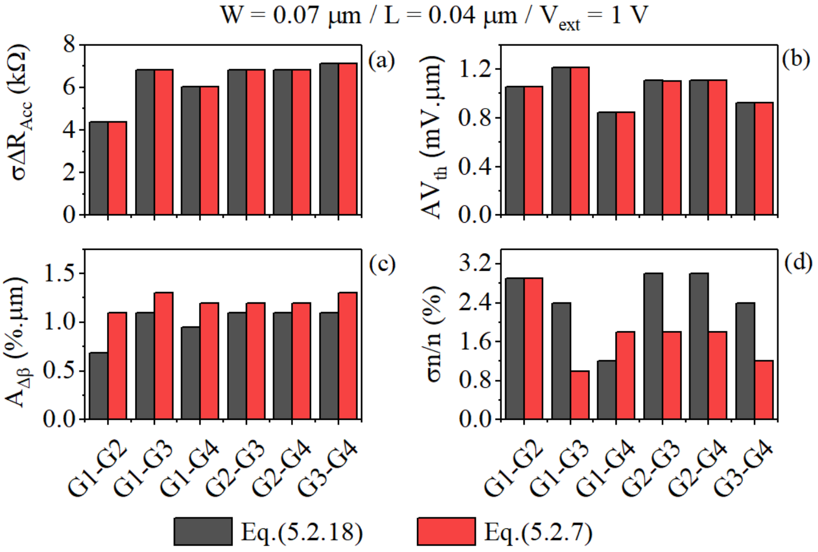

Figure 5.2.14 Comparison between matching parameters extracted using the global matching model of eq.(5.2.3) and the Lambert-based matching model of eq.(5.2.12).

At $V_{G,ext} = 1\ V$ (Fig.(5.2.13).(a), the two models perfectly match in subthreshold regime. From threshold to strong inversion, they appreciably differ. This discrepancy is mainly due to $\sigma\left(\frac{\Delta\beta}{\beta}\right)$: the Lambert model tends to underestimate it, as shown in Fig.(5.2.14).(c). Indeed, from eq.(5.2.18) it is clear that $\sigma(\Delta R_{Acc})$ depends on $\sigma\left(\frac{\Delta\beta}{\beta}\right)$, and a variation of this latter entails a variation of the former. Also $\sigma(\Delta n)$, whose values are reported in Fig.(5.2.14).(d), was not found to be the same, but its impact on the global mismatch is very small, since in subthreshold regime the main variability source is $\sigma(\Delta V_{th})$, which is identical for both eq.(5.2.7) and eq.(5.2.18) (Fig.(5.2.14).(b))

At $V_{G,ext} = 2\ V$ (Fig.(5.2.13).(b)), instead, both models fit almost perfectly the experimental curve. This is likely due to the minor impact of $\sigma(\Delta R_{Acc})$ at higher external voltages (Fig.(5.2.8)). Indeed $\sigma\left(\frac{\Delta\beta}{\beta}\right)$, that is the largest variability source in strong inversion, is the same for both eq.(5.2.7) and eq.(5.2.18) (Fig.(5.2.15)).

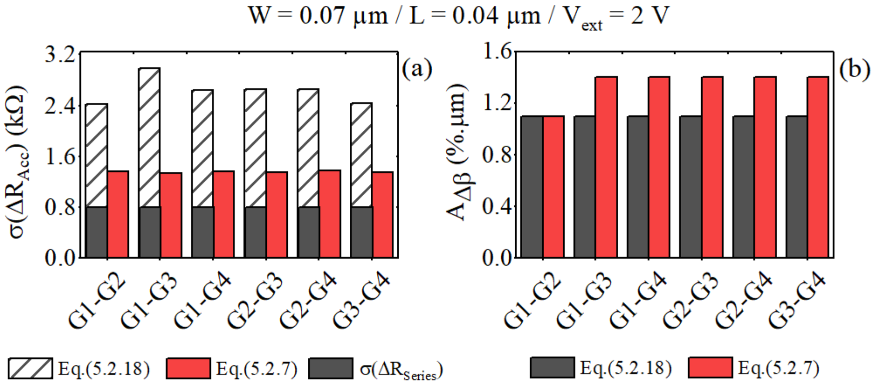

Figure 5.2.15 Comparison between $\sigma(\Delta R_{Acc})$ and $A_{\Delta\beta}$ extracted using eq.(5.2.3) and eq.(5.2.12)

Finally, the values of $\sigma(\Delta R_{Acc})$ and $A_{\Delta\beta}$ extracted with eq.(5.2.18) are compared to that obtained using eq.(5.2.7) and already shown in Fig.(5.2.7). Concerning $\sigma(\Delta R_{Acc})$, the Lambert model overestimates it of almost 50% with respect the classical fit of eq.(5.2.7). Moreover, $\sigma(\Delta R_{Series})$ is around 30% of the total $\sigma(\Delta R_{Acc})$. $A_{\Delta\beta}$, instead, is found to be underestimated by the Lambert model. This was expected, since $\sigma(\Delta R_{Acc})$ and $\sigma\left(\frac{\Delta\beta}{\beta}\right)$ are the main matching sources in strong inversion, and a variation of one of them results in a variation of the other. It is worth noticing that a large mismatch between $\sigma(\Delta R_{Acc})$ slightly affects $\sigma\left(\frac{\Delta I_D}{I_D}\right)$ since, at $V_{G,ext} = 2\ V$, the main variability contribution in strong inversion is given by $\sigma\left(\frac{\Delta\beta}{\beta}\right)$.

5.3 DYNAMIC VARIABILITY

Noise is an unwanted phenomenon that occurs in all the electrical circuits. It can come from external sources, such as AC power lines or adjacent circuits, or it can be a direct consequence of random fluctuations of physical processes governing the electrical transport in a medium. In this second case, which is the one we are interested in, the noise cannot be eliminated, since it is a process intrinsic to the device.

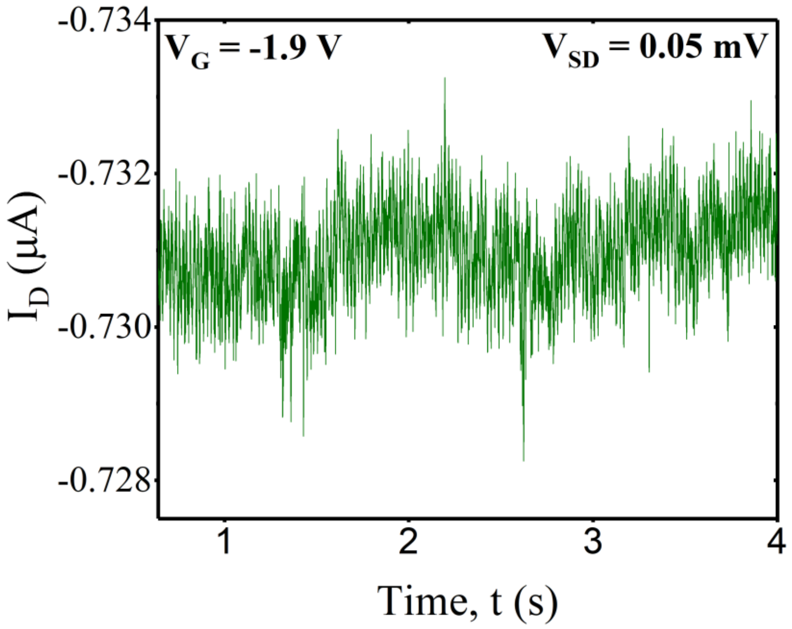

Figure 5.3.1 $I_D(t)$ of p-type 4G device at $T = 300\ K$.

Drain current noise is the result of a spontaneous random time fluctuation of the current around a mean value (Fig.5.3.1) [133]. Noise characterization are time – domain measurements, even if the frequency domain is often exploited using the FFT (*Fast Fourier Transform*) [134] to plot the current power spectral density (PSD) $S_{Id} = \Delta I_D^2\ (A^2 Hz^{-1})$. It is worth pointing out that the noise is nothing but a current variation over time and, therefore, the formalism used to describe the main noise quantities will be similar to the one used in static variability. Indeed, the total variance of a stationary signal satisfies,

$$\sigma_{Id}^2 = \int_0^{+\infty} S_{Id}(f)df \tag{5.3.1}$$

From eq.(5.3.1) it is evident that noise can be interpreted as the signal variance at a specific frequency.

5.3.1 Fundamental noise mechanisms

As devices' dimensions reduce, the study of low frequency noise becomes more and more important, since $1/f$ noise increases as the reciprocal of the device area [135] [136] [137].

In this section, we will describe the main noise mechanisms: thermal noise, shot noise, Generation – Recombination (G – R) noise, Random telegraph (RTS) noise and flicker noise.

Thermal noise

Thermal or “white” noise was observed for the first time by John B. Johnson in 1926 and explained by Harry Nyquist. It can be regarded as the background of any low frequency fluctuation. It is due to the random carrier motion inside a conductor that results in a frequency independent power spectral density. Every resistor produces thermal noise, whose PSD is given by:

$$S_V = 4k_B TR \iff S_I = 4k_B TG \tag{5.3.2}$$

where R and G are the resistance and the conductance, respectively [138] [139].

Shot noise

Shot noise, introduced by Walter Schottky in 1918 [140], is related to the discrete nature of electrons flowing through a potential barrier, like in p-n junctions, during a period of time. The associated PSD is,

$$S_I = 2qI \tag{5.3.3}$$

where I is the current across the barrier.

Generation – Recombination noise

G – R noise is associated to carriers’ trapping – detrapping processes taking place in a semiconductor device. More specifically, G – R noise occurs when one of the following situations happens:

- ✓ Recombination of a free electron and a free hole;
- ✓ Generation of a free electron and a free hole;
- ✓ Trapping of a free electron in an empty trap;
- ✓ Trapping of a free hole in a filled trap.

These results in a “Lorenzian – like” spectrum, described by [133]:

$$S_{Id} = \frac{A}{\left(1 + \frac{f}{f_c}\right)^2} \tag{5.3.4}$$

where A is the plateau at low frequencies and f_c the corner frequency above which the PSD goes as $S_{Id} \sim 1/f^2$.

Random Telegraph Signal Noise

Random telegraph signal (RTS) noise was observed in small area devices [141], and consists of individual carrier trapping at the $Si - SiO_2$ interface. RTS noise can be observed directly in the time domain signal (Fig.(5.3.2).(a)). Since only few traps are involved in the process, the current can switch between two or more states due to the random trapping – detrapping of carriers.

The PSD is described by a Lorenzian spectrum (Fig.(5.3.2).(b)) [142]:

$$S_{Id} = 4A.\Delta I_D^2 \frac{\tau}{(1 + (2\pi f)^2 \tau^2)} \tag{5.3.5}$$

where ΔI_D is the average drain current RTS amplitude, τ is the time constant of the transitions and is given by

$$\tau = \left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right)^{-1} \tag{5.3.6}$$

τ_c and τ_e being the capture and emission time of the trap. A is the space mark ratio:

$$A = \frac{\tau}{\tau_c + \tau_e} \tag{5.3.7}$$

τ_c and τ_e are generally determined by Shockley – Read – Hall statistics [142]:

$$\tau_c = \frac{1}{\sigma.n_S.v_{th}} \tag{5.3.8}$$

$$\tau_e = \frac{1}{\sigma.n_l.v_{th}} \tag{5.3.9}$$

where v_{th} is the thermal velocity, n_S the surface carrier concentration and n_l the surface carrier concentration when the Fermi level equals the trap energy.

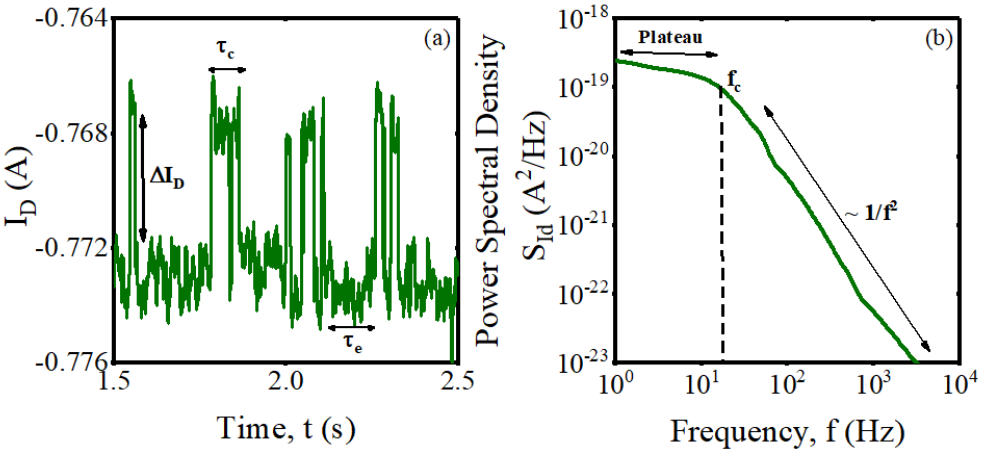

Figure 5.3.2 (a) $I_D(t)$ with RTS example and (b) associated PSD

Moreover for a tunnelling trapping process,

$$\sigma = \sigma_0 . e^{-\left(\frac{x_t}{\lambda}\right)} \tag{5.3.10}$$

being σ_0 the intrinsic cross-section, x_t the in-depth location of the trap into the oxide and λ the tunnelling attenuation length. Finally, the trap occupancy factor f_t is:

$$f_t = \frac{1}{1 + e^{(E_t - E_f)/kT}} \tag{5.3.11}$$

where E_t and E_f are the trap and Fermi energy levels.

Flicker Noise

Flicker noise, or "$1/f$ noise", is given by the contribution of several Lorenzian-like spectra [143], as shown in Fig.(5.3.3). In general, it is the dominant noise in MOSFETs, and it is the result of the action of several traps located at very small distances from the interface. The associated PSD reads:

$$S_{Id} = K . \frac{I_D^{\beta}}{f^{\gamma}} \tag{5.3.12}$$

where K is a constant, β the drain current exponent and γ the frequency exponent. If $\gamma = 1$, the oxide traps are uniformly distributed in oxide depth and energy. If $\gamma < 1$, the trap density is higher closer to the $Si - SiO_2$ interface, whereas if $\gamma > 1$, it increases deeper in the oxide.

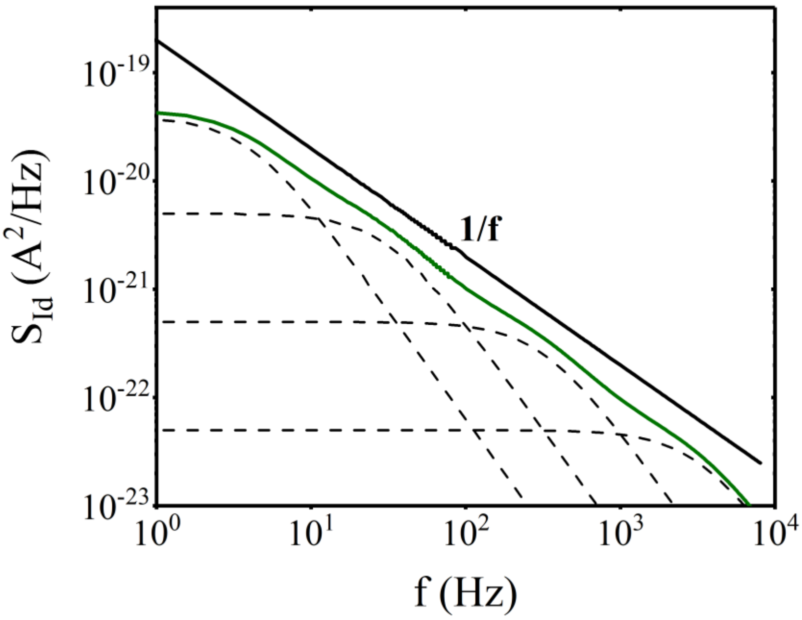

Figure 5.3.3 Flicker noise PSD spectrum.

5.3.2 Flicker noise – Theoretical Background

As previously mentioned, flicker noise constitutes the main noise source in MOSFET devices. This is the case also for the 4G devices shown here. Before presenting and discussing the experimental results, a theoretical background about the $1/f$ noise is provided.

Flicker noise is generally attributed to carrier number fluctuations (CNF) due to the carriers' trapping – detrapping process at the $Si - SiO_2$ interface [144]. The interface charge fluctuation δQ_{ox} can be regarded as a flat band voltage fluctuation [145]:

$$\delta V_{fb} = -\frac{\delta Q_{ox}}{W_G L_G . C_{ox}} \tag{5.3.13}$$

The drain current fluctuation can be written as [145]

$$\delta I_D = -g_m \delta V_{fb} = g_m \frac{\delta Q_{ox}}{C_{ox}} \tag{5.3.14}$$

and the associated drain current spectral density is

$$S_{Id} = g_m^2 S_{Vfb} = g_m^2 \frac{S_{Q_{ox}}}{W_G L_G C_{ox}^2} \tag{5.3.15}$$

being S_{Vfb} and $S_{Q_{ox}}$ the flat band spectral density and the oxide trapped charge spectral areal density, respectively.

A more detailed approach takes into account the fluctuations induced in the scattering rate, and thus in the mobility, by the variations of the oxide charge [146] (carrier number fluctuation with correlated mobility fluctuations (CNF/CMF)). Including mobility fluctuations, the drain current fluctuations can be expressed as:

$$\delta I_D = -g_m \delta V_{fb} \mp \alpha I_D \mu_{eff} \delta Q_{ox} \tag{5.3.16}$$

where α is the Coulomb scattering coefficient. The sign of the mobility term is chosen either negative for "acceptor – like" traps or positive for "donor – like" traps. The associated spectral density is given by,

$$S_{Id} = \left(1 \pm \alpha \mu_{eff} C_{ox} \frac{I_D}{g_m}\right)^2 g_m^2 S_{Vfb} = \left(1 + \Omega . \frac{I_D}{g_m}\right)^2 g_m^2 S_{Vfb} \tag{5.3.17}$$

where $\Omega = \alpha \mu_{eff} C_{ox}$.

If the trapping – detrapping process occurs though a tunneling process, the flat band voltage spectral density can be written as,

$$S_{Vfb} = \frac{q^2 \lambda k_B T N_t}{f^{\gamma} W_G L_G C_{ox}^2} \tag{5.3.18}$$

where $\lambda = 0.1\, nm$ [136] is the tunnelling attenuation length and N_t is the oxide trap volume density.

It is finally worth defining the so-called "equivalent input gate voltage spectral density" [146]:

$$S_{Vg} = \frac{S_{Id}}{g_m^2} = \left(1 \pm \alpha \mu_{eff} C_{ox} \frac{I_D}{g_m}\right)^2 S_{Vfb} \tag{5.3.19}$$

It is important to highlight that, if the impact of interface charges on mobility is negligible, $S_{Vg} \approx S_{Vfb}$. S_{Vg}, however, does not have any physical meaning, but it is a pure electrical parameter. Indeed, it corresponds to the equivalent gate voltage spectral density of the external noise source that one has to put on the gate in order to induce the same drain current noise [145]. Emulating this idea, we have defined a similar quantity also for the static variability, that is, the input referred normalized matching parameter of eq.(5.2.11).

5.3.3 Hooge mobility fluctuation model

A completely different approach was proposed by Hooge [137]. In this model, the drain current fluctuations are caused by mobility fluctuations, which are induced only by phonon scattering [147], while each conducting carrier contributes independently to the mobility fluctuations. According to these hypotheses, the current spectral density reads:

$$S_{Id} = I_D^2 \frac{q.\alpha_H}{W_G L_G f.Q_{inv}} \tag{5.3.20}$$

where α_H is the Hooge parameter.

This approach was shown to be valid only in bulk semiconductors and in metals [148], whereas it can be rarely encountered in MOSFETs.

5.3.4 Device and experimental details

Two p – type 4G devices, with $W_G = 75\ nm$, $L_G = 50\ nm$ and $t_{Si} = 17.9\ nm$ (Fig.(5.2.1)) were tested at both $T = 300\ K$ and $T = 10\ K$ using the six – probes cryo bank described in Chapter 4. A Keysight B1500 with dedicated B1530 module was used to measure the time signal. Since the probing time had to be small in order to be able to probe high frequencies, pulsed I-V (PIV) measurements instead of classical SMU were performed. Indeed, both the active gate and the source (since we tested p – type devices) were connected to PIVs, whereas the external gates were connected to the SMUs. The external gate voltage was fixed at $V_{G,ext} = -2\ V$, while the source was biased at $V_{SD} = 50\ mV$. The increase in speed provided by the PIVs entailed a decrease in measurement sensitivity: the minimum detectable current was 2 nA, limiting the subthreshold current range to a couple of decades. Moreover, no LNA have been used. Finally, all the spectra shown in the following have been corrected by subtracting the background noise.

5.3.5 Experimental results

In Fig.(5.3.4).(a),(b) are sketched the $I_D(V_G)$ of a 4G device both at $T = 300\ K$ and $T = 10\ K$. The characteristics of the four gates at room temperature are very close, whereas they differ more at deep cryogenic temperature. In general, variability gets worst at low temperature [52].

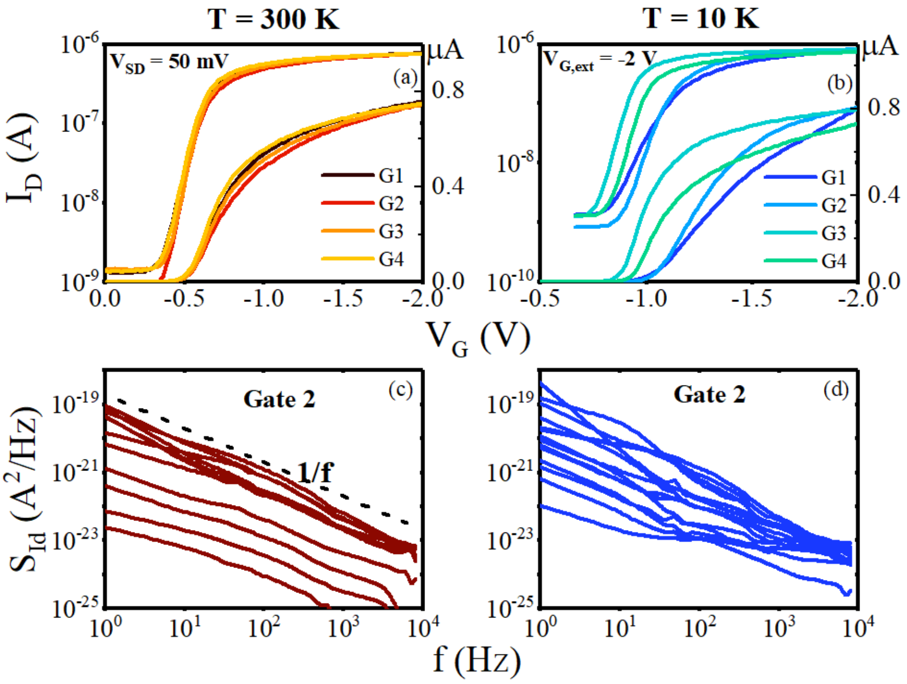

Figure 5.3.4 $I_D(V_G)$ and S_{Id} at $T = 300\ K$ (a)-(c) and $T = 10\ K$ (b)-(d).

In Fig. (5.3.4).(c),(d) are reported the current spectral densities for gate 2 (see Fig.(5.2.1)) at both $T = 300\ K$ and $T = 10\ K$, for different gate voltages. At room temperature, $S_{Id} \sim 1/f$, whereas at cryogenic temperature there are some Lorenzian – like spectra. In order to verify their origin, we plotted in Fig.(5.3.5) $I_D(t)$, that clearly shows the presence or RTS even at $T = 10\ K$.

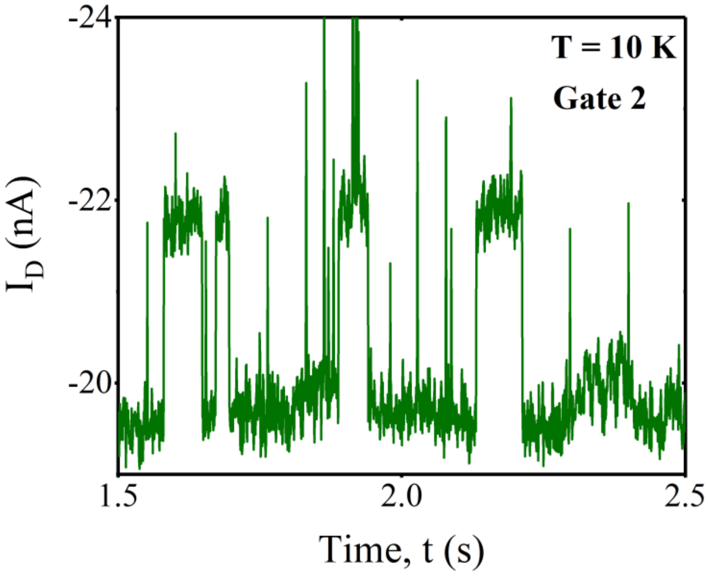

Figure 5.3.5 $I_D(t)$ of gate 2 shown in Fig.(5.3.4). (d) at $T = 300\ K$.

In Fig.(5.3.6) are reported the extracted normalized power spectral densities S_{Id}/I_D^2 at room and cryogenic temperatures for one active gate of the 4G device at $f = 7.8\ Hz$. The experimental data are fitted using both the CNF model expressed in eq.(5.3.15) (Fig.(5.3.6).(a),(b)) and the CNF/CMF model, where eq.(5.3.17) was corrected in order to include the impact of the access resistance noise [149]:

$$\frac{S_{Id}}{I_D^2} = S_{Vfb}.\frac{g_m^2}{I_D^2}\left(1+\Omega.\frac{I_D}{g_m}\right)^2 + S_{RAcc}\left(\frac{I_D}{V_D}\right)^2 \tag{5.3.21}$$

Indeed, in these devices, R_{Acc} was shown to have a big impact in current characteristics in strong inversion, and it is worth verifying if it has a similar influence also on noise curves. It is important to point out that eq.(5.3.21) relies on three fitting parameters, i.e. S_{Vfb}, Ω and S_{RAcc}.

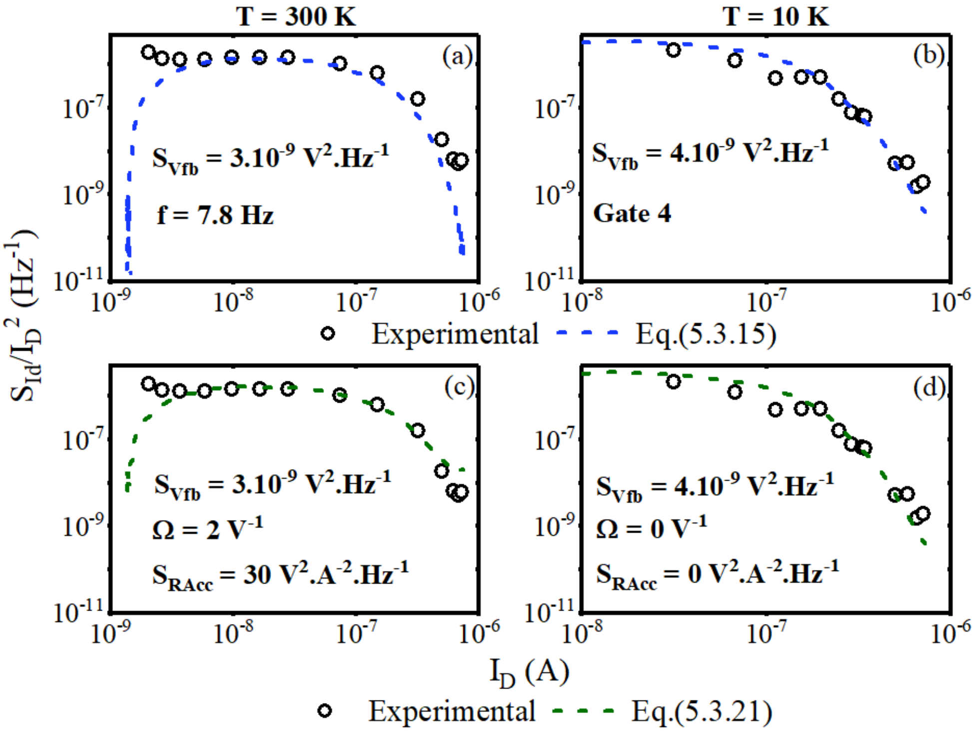

Figure 5.3.6 Experimental (symbols) and modeled (dashed lines) S_{Id}/I_D^2 at $T = 300\ K$ (a),(c) and at $T = 10\ K$ (b),(d).

CNF model fits quite well the curves both at $T = 300\ K$ and $T = 10\ K$, even if in strong inversion and at room temperature, eq.(5.3.15) appreciably differs from the experimental behaviour. Indeed, exploiting eq.(5.3.21), it turns out that mobility fluctuations impact the noise at high gate voltages ($\Omega = 2\ V^{-1}$). Moreover, the slight increase of the current spectral density in strong inversion is due to the influence of the access resistance, and the associated spectral density is $S_{RAcc} = 0.3.\Omega^2.Hz^{-1}$.

At $T = 10\ K$, on the other hand, the CNF perfectly fits the experimental curve, and the mobility fluctuations, as well as the access resistance, does not affect the drain spectral density in strong inversion. In conclusion, at $T = 300\ K$, CNF constitutes the main source of noise from subthreshold to moderate inversion, whereas CMF and access resistance noise have a bigger impact in strong inversion. At $T = 10\ K$ and CNF represents the only noise source, from subthreshold to strong inversion.

The number of tested devices, i.e. two, is not enough to perform a systematic study about the impact of gate position and, in turn, of the source/drain proximity, on the noise. Therefore, we will not present any parameter extraction as function of gate position, as we did for the static variability. We preferred to consider each gate as an independent device and investigate the noise temperature evolution by taking into account the average behaviour of the eight gates (transistors) tested. In such a way, we can get a fairly reliable estimation of the noise for this gate stack technology.

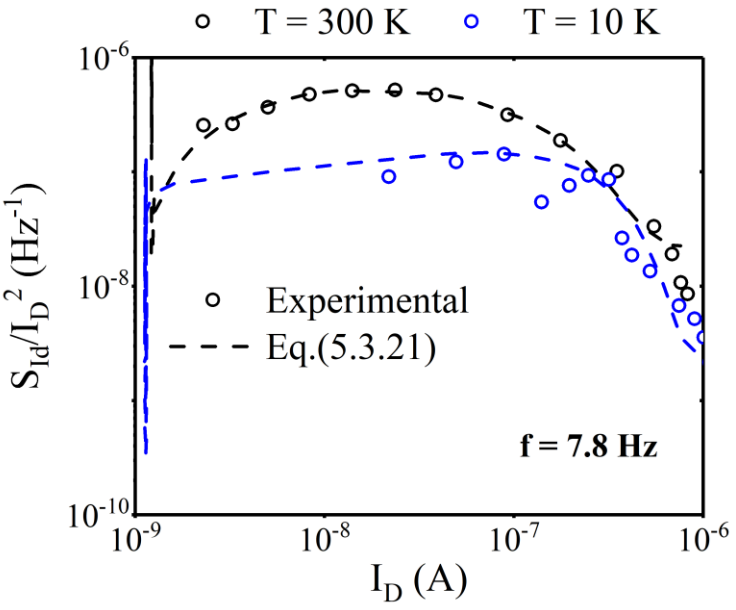

Figure 5.3.7 Average S_{Id}/I_D^2 for $T = 300\ K$ (black) and $T = 10\ K$ (blue).

In Fig.(5.3.7) are compared the averaged normalized current spectral densities at room and low temperature. S_{Id}/I_D^2 slightly decreases lowering down T. This is likely due to the slight decrease of the ratio g_m/I_D at cryogenic temperatures, already observed in DC measurements (see Chapter 4).

The parameters extracted from eq.(5.3.21) are reported in Table (5.3.1). With the exception of the volume trap density N_t, all the other parameters decrease at cryogenic temperature. The flat band voltage spectral density at $T = 10\ K$ is a bit smaller than at $T = 300\ K$. Both in bulk and FD – SOI MOSFETs it was shown to be more or less constant with temperature [63] [150]. Ω decreases as well, contrary to what found for 22nm FD – SOI technology [63], suggesting that mobility fluctuations have a smaller impact on current noise at cryogenic temperatures.

Extracted Parameters	**T = 300 K**	**T = 10 K**
$S_{Vfb}\ [V^2/Hz]$	8.10^{-10}	2.10^{-10}
$\Omega\ [\mathrm{V}^{-1}]$	4	1
$S_{RAcc}\ \left[\frac{\Omega^2}{Hz}\right]$	30	5
$N_t\ [eV^{-1}.cm^{-3}]$	$2.24 \cdot 10^{16}$	$1.682 \cdot 10^{17}$

Table 5.3.1

The reduction of S_{RAcc} at $T = 10\ K$ is likely caused by the diminution of the access resistance of the multi-gates devices at cryogenic temperature (see Fig.(4.4.8) and Fig.(5.3.9)). Finally, the trap density N_t was computed using eq.(5.3.18). The value at room temperature is in line with thermally grown $Si - SiO_2$ gate stack technology and the oxide thickness ($t_{Si} = 6\ nm$). At $T = 10\ K$, instead, the increase of trap density at cryogenic temperature is likely due the presence of the band tail in the density of states since the Fermi level get closer to the band edge [63] [96] [150].

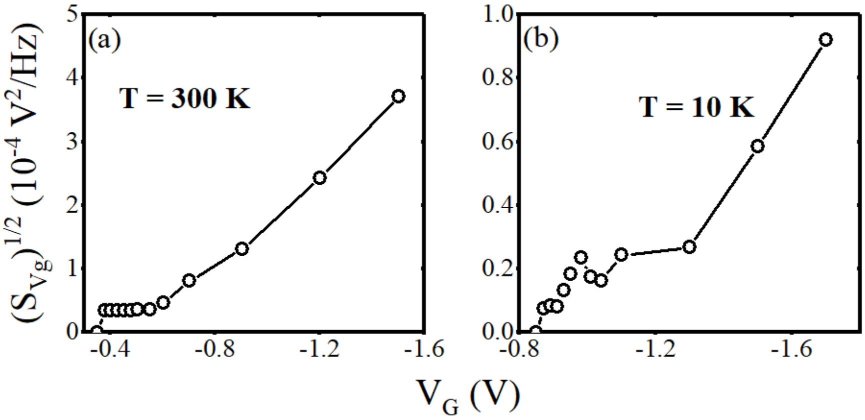

Figure 5.3.8 $\sqrt{S_{Vg}}$ at $T = 300\ K$ (a) and $T = 10\ K$ (b).

In Fig.(5.3.8) are reported $\sqrt{S_{Vg}}$ at room and cryogenic temperature, in order to investigate the impact of mobility fluctuations in strong inversion. Indeed, if CMF is the predominant noise source at high gate voltages, $\sqrt{S_{Vg}}$ should be a linear function of V_G, since $I_D \approx C_{ox}(V_G - V_{th})$ in eq.(5.3.19) [146]. At both $T = 300\ K$ and $T = 10\ K$, $\sqrt{S_{Vg}}$ shows a linear behaviour at high V_G, corroborating the analysis carried out previously. Moreover, CMF influences more the noise at room than at cryogenic temperature, as found in Table (5.3.1), since $\sqrt{S_{Vg}}$ is 4 times higher at $T = 300\ K$. It is worth pointing out, finally, that, in weak inversion, $\sqrt{S_{Vg}}$ saturates to a value close to $\sqrt{S_{Vfb}}$ [146].

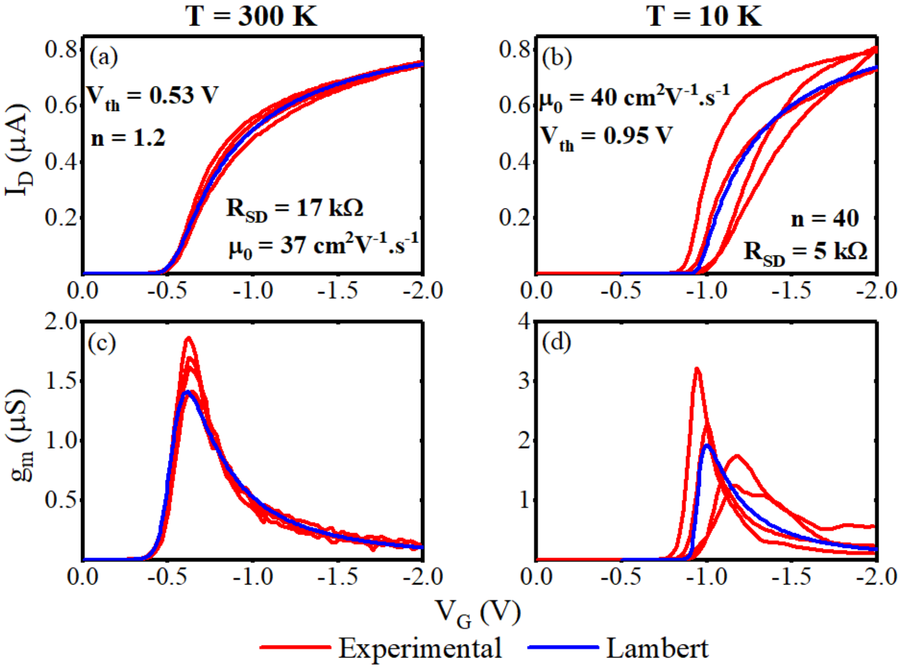

Figure 5.3.9 Modeled (blue line) and experimental (red line) $I_D(V_G)$ and $g_m(V_G)$ at $T = 300\ K$ (a),(c) and at $T = 10\ K$ (b),(d).

5.3.6 Lambert – based Modeling

To go further, we adapted the Lambert – based model previously developed for the static variability to the dynamic variability.

The current characteristics of the 4G devices were modelled using eq.(5.2.12) and eq.(5.2.13) both at $T = 300\ K$ and $T = 10\ K$. In Fig.(5.3.9) are compared the experimental and modeled $I_D(V_G)$ and $g_m(V_G)$ for a given device. The gate variability is small, especially at room temperature, and the assumption that the 4G can be modeled as a series of four identical resistances is still reasonable.

Considering eq.(5.3.1), the power spectral density of a given signal coincides with the signal variance at a given frequency. This allows to re-write eq.(5.2.16) as

$$S^*_{RAcc} = 3.S_{Rch}(V_G = V_{G,ext}) \tag{5.3.22}$$

where S^*_{RAcc} is the access resistance contribution to current spectral density due to the access gates (S_{Rch} for $V_{G,ext}$). Eq.(5.3.22) expresses the access resistance spectral density in terms of noise contributions coming from each access gate. In such a way, the total spectral density can be written as:

$$S_{Rtot} = S_{Rch} + S_{RAcc} = S_{Rch}(V_G) + 3.S_{Rch}(V_G = V_{G,ext}) \tag{5.3.23}$$

Considering that the normalized current spectral density for the active channel reads [149]

$$\frac{S_{Rch}}{R^2_{ch}} = \left(\frac{g_m}{I_{D,ch}}\right)^2 .S_{Vfb,ch}.\left(1 + \Omega_{\mathrm{ch}}.\frac{I_{D,ch}}{g_{m,ch}}\right)^2 \tag{5.3.24}$$

where $R_{ch}$is given by eq.(5.2.14), the total normalized current spectral density can be written as

$$\frac{S_{Id}}{I^2_D} = \frac{S_{Rch}}{R^2_{ch}}.\frac{R^2_{ch}(V_G)}{R^2_{tot}(V_G, V_{G,ext})} + .\frac{3.S_{Rch}(V_{G,ext})}{R^2_{tot}(V_G, V_{G,ext})} \tag{5.3.25}$$

where $R_{tot}(V_G, V_{G,ext})$ is given by eq.(5.2.13).

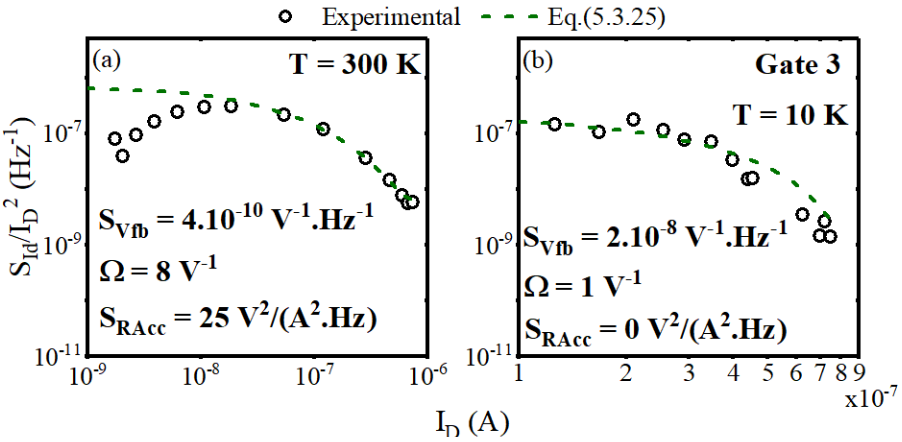

Figure 5.3.10 Experimental (symbols) and modeled (dashed lines) S_{Id}/I^2_D at $T = 300\ K$ (a) and at $T = 10\ K$ (b).

In Fig.(5.3.10) are reported an example of curves fitted with eq.(5.3.25). The Lambert model works well in strong inversion, whereas there is a little disagreement in subthreshold regime for the room temperature case. In this example, the flat band voltage spectral density increases of two orders of magnitude at cryogenic temperature, whereas the mobility fluctuations and the access resistance contributions decrease. It is hard to deduce a global trend for this technology with the data available. Indeed, we insist that, in order to provide a reliable extraction of the noise parameters as function of gate position, a statistical noise characterization must be performed. In particular, the Lambert – model discussed should be applied to average curves, as we did for the static variability.

5.3.7 A glimpse on the low frequency noise in quantum dots

A detailed understanding of the noise is essential also in quantum dot regime. Indeed, the LFN source remains the same, independently on the kind of transport involved. This, in principle, could pave the way to the possibility of linking transistor and quantum dot figures of merit. In [151] is highlighted that the main noise source comes from surface potential ψ_S fluctuations. Afterwards, an expression for the so-called "charge noise spectral density" S_ϵ is proposed. However, this quantity cannot be directly compared to S_{Id} or S_{Vg}, and the relation with the gate oxide capacitance C_{ox} is not evident.

In the following, an expression for the surface potential spectral density S_{ψ_S} is obtained starting from the classical MOSFET noise theory. It will be shown that surface potential fluctuations arise from gate oxide charges fluctuations.

Surface potential fluctuations $\delta\psi_S$ can be expressed as

$$\delta\psi_S = \frac{d\psi_S}{dV_G}.\delta V_G \tag{5.3.26}$$

where δV_G is the equivalent input gate voltage fluctuations. From eq.(3.2.1), in subthreshold regime:

$$\frac{d\psi_S}{dV_G} = \frac{C_{ox}}{C_{ox} + C_{it} + C_d} \tag{5.3.27}$$

Moreover, CMF can be neglected in this case, and $\delta V_G \approx \delta V_{fb}$. Furthermore, by combining eq.(5.3.26)-eq.(5.3.27) and eq.(5.3.13):

$$\delta\psi_S = \frac{C_{ox}}{C_{ox} + C_{it} + C_d}.\delta V_G = \frac{C_{ox}}{C_{ox} + C_{it} + C_d}.\delta V_{fb} \tag{5.3.28}$$

Finally, the surface potential spectral density S_{ψ_S} is

$$S_{\psi_S} = S_{Vfb}.\left(\frac{C_{ox}}{C_{ox} + C_{it} + C_d}\right)^2 = \frac{S_{Qss}}{WL.(C_{ox} + C_{it} + C_d)^2} \qquad (5.3.29)$$

Eq.(5.3.29) can be used to calculate the surface potential spectral density of a quantum dot, where S_{Qss} is known at the charge noise. The extracted S_{Vfb} can be compared to that extracted in transistor – like regime, both at cryogenic and room temperature.

5.4 CONCLUSION

This chapter was dedicated to the study of static and dynamic variability of four-gates qubit devices. In the first part, we introduced the theoretical background of static variability, followed by a complete electrical and statistical characterization at room temperature of 48 dies containing devices with three different channel lengths. Afterwards, we developed a compact model based on the Lambert – W function, under the assumption, well grounded on the experimental results, that the four gates devices could be modeled as a series of four identical resistances. We showed this model to be effective in fitting drain current and $Y - function$ curves. Moreover, this model has been extended to fit matching curves, exhibiting good agreement with both experimental results and the classical model previously used.

In the second part of the chapter, dynamic variability, i.e. low frequency noise, was explored at both room and cryogenic temperature. Devices showed "$1/f$" behaviour, even if at cryogenic temperature some signatures of Lorenzian – like spectra were exhibited. This turned out to be consequence of RTS noise. Furthermore, CNF and CMF were shown to constitute the main noise sources, at both $T = 300\ K$ and $T = 10\ K$. In order to benchmark the gate stack technology, we considered the noise averaged on the eight gates composing the two 4G devices tested. The average current spectral density decreases at cryogenic temperature, whereas the trap density increases. This trend was likely due to the presence of the density of states band tail. Afterwards, we adapted the Lambert – based model developed for the static variability to model the current spectral density. The model showed good agreement with the experimental data. Finally, a possible approach to investigate the LFN in quantum dot regime was briefly discussed, by showing how the charge noise can be eventually replaced by the surface potential spectral density. Indeed, this quantity can be easily extracted also at room temperature in case of transistor – like transport. Concluding, the surface potential spectral density could not only represent a parameter valid from room down to deep cryogenic temperature, but it could also constitute a suitable figure of merit to link the transistor and the quantum dot behaviour.

Chapter 6: General Conclusion and Perspectives

The purpose of this dissertation was double: *(i)* characterize MOS based qubit devices from room down to deep cryogenic temperature to support the realization of a qubit industrial process flow, and *(ii)* develop simulation tools and compact models able to provide insights about the technology and the device physics.

We first developed a TCAD model able to simulate an FD-SOI device down to deep cryogenic temperatures, using an analytical approximation of the Fermi integral, and even to zero kelvin, using the metallic statistics. Carrier densities computed with Maxwell – Boltzmann and Fermi – Dirac statistics were compared, proving that at cryogenic temperature the quantum nature of electrons and holes cannot be neglected. Furthermore, it was demonstrated that no significant change in the device electrostatics occurs at temperatures lower than 20 K. This TCAD model turned out to be essential to explain some experimental features of the devices we characterized.

Compact modeling chapter went through two kinds of approaches. The first one relied on the Maxwell – Boltzmann statistics and it was based on the Lambert – W function, and it turned out to be an important tool for experimental fitting and device parameter extraction. The second one considered the inversion layer as a 2D system and exploited Fermi – Dirac statistics for the calculation of the carrier density. It enabled the modeling and a deeper understanding of some cryogenic device behaviours and features, such as the origin of the zero temperature coefficient, the impact of the band tail on capacitance and the cause of oscillations in the trans-conductance. Finally, a model based on the percolation transport theory was proposed to explain the subthreshold current oscillation often observed in small area MOSFETs.

For what concern devices' characterization, we started by measuring both the capacitance and the drain current as function of gate voltage of a large area FD – SOI. The main parameters were extracted and the experimental curves were fitted with the Lambert – W function method, showing its effectiveness in the whole gate voltage range and from room down to deep cryogenic temperature. Afterwards, a five – gate p-type device was tested in linear regime. An ad – hoc model, based on the Lambert –

W function was developed to easily extract the main device figures of merit. Finally, the impact of high bias voltages was investigated.

Lastly, static and dynamic variability of four – gate devices were studied. Concerning the matching analysis, it was carried out at room temperature and in linear regime, and it was found that, in terms of local variability, the LETI qubit technology was comparable to the 28nm FD – SOI one. A Lambert – based model was used to reproduce both the electrical and statistical curves. The dynamic variability, on the other side, was performed on only two devices, both at room and deep cryogenic temperatures. Flicker and random telegraph signal noise were found to be the main noise sources. Concerning the $1/f$ noise, it was mainly caused by carrier number and correlated mobility fluctuations. In this context, the same Lambert – W function based model introduced for the static variability was applied, providing good agreement with the experimental results.

In conclusion, the models introduced and developed in this thesis allowed to interpret most of the experimental data observed. Transport analysis in temperature revealed the impact of defective scattering, likely related to dopant or defect diffusion into the channel. This turned out to be responsible of mobility degradation in both long and short multi – gate devices. Moreover, some "unconventional" behaviours, like the non-linear current in the output characteristic at low drain biases and at cryogenic temperatures, were attributed to the presence of traps underneath the nitride spacers. The impact of high drain voltages on mobility was ascribed to the thick nitride spacers as well. Summarizing, two possible critical aspects can be identified in qubit FD-SOI devices: doping or defect diffusion that degrades the transport in the entire temperature range investigated, and that will jeopardize the correct functioning of the device in quantum dot regime; traps underneath the thick nitride spacers, that limits the transport as well, as clearly visible from $I_D(V_D)$ curves at cryogenic temperature, and that are likely responsible of a larger device noise.

Concerning the possibility to link the room temperature transistor behaviour to the cryogenic quantum dot one, the most promising way is probably constituted by the low frequency noise characterization. Indeed, transistor's DC figures of merit can hardly be applied to the quantum dot regime, since the carrier transport is completely different: parameters such as the low field mobility could provide useful insights about the channel defectivity but there is not a clear quantum counterpart that could enable a quantitative comparison between the two regimes. Low frequency noise, on the other hand, focuses on the study of current fluctuations, without involving any microscopic description of transport. In Chapter 5, an expression for the surface potential spectral density was derived starting from the gate charge conservation equation, therefore a pure electrostatic description of the device, and from the expression that links flat band voltage and oxide charges fluctuations. It is evident that the obtained surface potential spectral density can be used as a figure of merit both for the transistor and the quantum dot – like behaviour. In such a way, a parameter common to the classical and quantum regime is provided.

6.1 FUTURE PERSPECTIVES

The work carried out in this thesis can be extended in different ways:

- Static variability at deep cryogenic temperature. This would include the development of a statistical model to take into account subthreshold current oscillations.
- Statistical noise analysis, in order to be able to study the impact of source and drain proximity and device area scaling.
- Differential noise analysis characterizing devices with different dimensions, in order to discriminate between the noise coming from the spacers and that coming from the channel.
- Investigation of back bias impact on DC and noise measurements. Indeed, the buried oxide interface has a better quality than the top gate one, and the quantum dot, if formed at the interface between BOX and Si body, should be less susceptible to the interface traps.

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Appendix A: Band diagram and Fermi level

In Fig.(A.1) is sketched the band diagram of an FDSOI device when a positive gate voltage V_G is applied. For sake of simplicity, the flat band voltage is considered to be $V_{fb} = 0$.

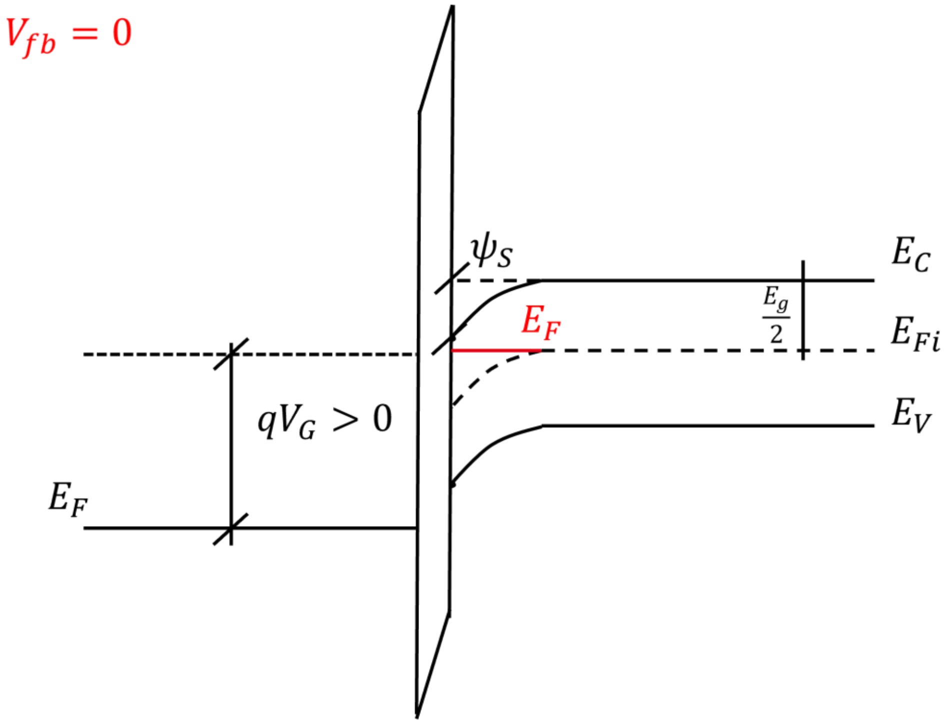

Figure 6.1A.1 FDSOI Band diagram

From Fig.(A.1) it is easy to demonstrate the validity of eq.(3.3.3):

$$q\psi_S = [E_C(+\infty) - E_{Fi}(+\infty)] - [E_C(0) - E_F] = \frac{E_g}{2} + E_F - E_C(0) \qquad (A.1)$$

$$E_F - E_C(0) = q\psi_S - \frac{E_g}{2} = q\psi_S - qV_0 \qquad (A.2)$$

If the bottom of the conduction band at the interface is set to $E_C(0) = 0$,

$$E_F = q.(\psi_S - V_0) \qquad (A.3)$$

Résumé en français

L'objectif de cette thèse était double : *(i)* caractériser les dispositifs qubit basés sur le TMOS de la température ambiante jusqu'aux températures cryogéniques pour soutenir la réalisation de qubit par un procédé industriel, et *(ii)* développer des outils de simulation et des modèles compacts capables de fournir des informations sur la technologie et la physique du dispositif.

Nous avons d'abord développé un modèle TCAD capable de simuler un dispositif FD-SOI jusqu'à des températures cryogéniques intenses, en utilisant une approximation analytique de l'intégrale de Fermi, et même jusqu'à zéro kelvin, en utilisant la statistique métallique. Les densités de porteurs calculées avec les statistiques de Maxwell – Boltzmann et de Fermi – Dirac ont été comparées, prouvant qu'à température cryogénique, la nature quantique des électrons et des trous ne peut être négligée. De plus, il a été démontré qu'aucun changement significatif dans l'électrostatique du dispositif ne se produit à des températures inférieures à $20\,K$. Ce modèle TCAD s'est avéré essentiel pour expliquer certaines caractéristiques expérimentales des dispositifs que nous avons caractérisés.

Le chapitre sur la modélisation compacte est basé sur deux approches. La premiere s'appuie sur les statistiques de Maxwell - Boltzmann et repose sur la fonction W de Lambert qui s'est avérée être un outil important pour l'ajustement expérimental et l'extraction des paramètres du dispositif. La seconde considère la couche d'inversion comme un système 2D et exploite les statistiques de Fermi – Dirac pour le calcul de la densité de porteurs. Cela a permis la modélisation et une compréhension plus approfondie de certains comportements et caractéristiques des dispositifs cryogéniques, tels que l'origine du coefficient de température zéro, l'impact de la queue de bande sur la capacité et la cause des oscillations dans la transconductance. Enfin, un modèle basé sur la théorie du transport par percolation a été proposé pour expliquer la saturation de la pente sous le seuil et l'oscillation de courant sous le seuil souvent observée dans les MOSFET de dimension nanométrique.

Pour ce qui concerne la caractérisation des dispositifs, nous avons commencé par mesurer à la fois la capacité et le courant de drain en fonction de la tension de grille d'un FD - SOI de grande surface. Les principaux paramètres ont été extraits et les courbes expérimentales ont été ajustées avec la méthode de la fonction W de Lambert, montrant son efficacité dans toute la plage de tension de grille et de la température ambiante jusqu'aux températures cryogéniques. Ensuite, un dispositif de type p à cinq grilles a été testé en régime linéaire. Un modèle ad-hoc, basé sur la fonction Lambert-W a été développé pour extraire facilement les principales figures de mérite du composant. Enfin, l'impact des tensions de polarisation élevées a été étudié.

D’autre part, la variabilité statique et dynamique des dispositifs à quatre grilles a été étudiée. Concernant l'analyse d'appariement, elle a été réalisée à température ambiante et en régime linéaire, où il a été constaté qu'en termes de variabilité locale, la technologie qubit du LETI était comparable à celle 28nm FD – SOI industriel. Un modèle basé sur la fonction de Lambert a été utilisé pour reproduire à la fois les courbes électriques et statistiques. La variabilité dynamique (bruit), quant à elle, n'a été réalisée que sur deux dispositifs, à la fois à température ambiante et à température cryogénique. Dans les TMOS, les principales sources de bruit à basse fréquence sont constituées par le bruit « flicker » (1/f) et le bruit en créneaux (RTS). Concernant le bruit 1/f, il est principalement causé par les fluctuations du nombre de porteurs et la mobilité corrélées. Dans ce contexte, le même modèle basé sur la fonction W de Lambert introduit pour la variabilité statique a été appliqué pour modéliser le bruit 1/f, offrant un bon accord avec les résultats expérimentaux.

En conclusion, les modèles introduits et développés dans cette thèse ont permis d'interpréter la plupart des données expérimentales observées. L'analyse du transport en température a révélé l'impact de la diffusion sur les défauts du canal sur la mobilité, probablement liée à des dopants ayant diffusé dans le canal. Ce phénomène est responsable de la dégradation de la mobilité dans les dispositifs multi-grilles longs et courts. De plus, certains comportements anormaux comme le courant non linéaire dans la caractéristique de sortie à faible polarisation de drain et à des températures cryogéniques ont été expliqués par la présence de pièges chargés sous les espaceurs en nitrure. L'impact des tensions de drain élevées sur la mobilité à fort champ a également été attribué aux espaceurs épais en nitrure. En résumé, deux aspects critiques possibles peuvent être identifiés dans les dispositifs qubit FD-SOI : le dopage ou la diffusion de défauts dans le canal qui dégrade le transport dans toute la plage de température étudiée, et qui pourrait mettre en péril le bon fonctionnement du dispositif en régime de points quantiques ; des pièges sous les espaceurs épais en nitrure qui limitent également le transport, comme le montrent clairement les courbes $I_D\,(V_D)$ à température cryogénique, et qui sont aussi probablement responsables d'un bruit de dispositif plus important.

Concernant la possibilité de lier le comportement du transistor à température ambiante à celui de la boîte quantique cryogénique, la voie la plus prometteuse est probablement constituée par la caractérisation du bruit à basse fréquence. En effet, les figures de mérite DC du transistor peuvent difficilement être appliquées au régime de points quantiques, puisque le transport des porteurs est complètement différent : des paramètres tels que la mobilité à faible champ pourraient fournir des informations utiles sur la défectuosité du canal, mais il n'y a pas de contrepartie quantique claire qui pourrait permettre une comparaison quantitative entre les deux régimes. Le bruit à basse fréquence, quant à lui, se concentre sur l'étude des fluctuations de courant, sans impliquer aucune description microscopique du transport. Dans le chapitre 5, une expression de la densité spectrale de potentiel de surface a été dérivée à partir de l'équation de conservation de charge de grille, donc une description électrostatique pure du dispositif, et de l'expression qui relie la tension de bande plate et les fluctuations de charges d'oxyde. Il est évident que la densité spectrale de potentiel de surface obtenue peut être utilisée comme facteur de mérite à la fois pour le transistor et le comportement de type boîte quantique. De cette manière, un paramètre commun au régime classique et quantique est fourni.

List of Publication

Journals

[1] E. Catapano *et al*., "Statistical and Electrical Modeling of FDSOI Four-Gate Qubit MOS Devices at Room Temperature", IEEE J. Electron Devices Soc., 582-590, 2021

[2] E. Catapano *et al*., "Modeling and simulations of FDSOI five-gate qubit MOS Devices down to deep cryogenic temperatures", Solid – State Electronics, 2022

[3] E. Catapano *et al*., "Modeling of 1D confinement in FD-SOI Trigate Nanowires at deep cryogenic temperatures", Solid – State Electronics, 2022

[4] E. Catapano *et al*., "On the Zero Temperature Coefficient in Cryogenic FD-SOI MOSFETs", in publication at IEEE Trans. Electron Devices, 2022

Conferences

[1] E. Catapano *et al*., "Characterization and Lambert – W Function based modeling of FDSOI five-gate qubit MOS devices down to cryogenic temperatures", *2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon* (EuroSOI-ULIS), 2021

[2] E. Catapano *et al*., "TCAD simulations of FDSOI devices down to deep cryogenic temperature", *2022 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon* (EuroSOI-ULIS), 2022