



Behavioral Analysis and Design of K-Band Low-Phase-Noise Digitally Controlled Oscillators in 22 nm FD-SOI for 76 - 81 GHz Automotive Radars

Zhigang Li

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THESE

Pour l'obtention du Grade de

DOCTEUR DE L'UNIVERSITE DE POITIERS

(Faculté des Sciences Fondamentales et Appliquées)
(Diplôme National - Arrêté du 25 mai 2016)

Ecole Doctorale : Mathématiques, Informatique, Matériaux, Mécanique, Energétique
(MIMME)

Secteur de Recherche : Electronique, Microélectronique et Nanoélectronique

Présentée par :

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Behavioral Analysis and Design of K-Band Low-Phase-Noise Digitally Controlled Oscillators in 22 nm FD-SOI for 76 - 81 GHz Automotive Radars

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Soutenue le **05 Mai 2023** Devant la Commission d'Examen

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Acknowledgements

This research work was carried out within the framework of a collaboration between the research institute of XLIM (UMR 7252, IUT of Angoulême, University of Poitiers) and the company IDDO-IC. Firstly, I would like to thank Mr. Denis MASLIAH, the founder of IDDO-IC, for welcoming me into his team and for his trust and support.

In particular, I would like to express my sincere thanks to my thesis director, Mr. David Cordeau, Maître de Conference HDR at the University of Poitiers, and co-director, Mr. Jean-Marie Paillot, Professor at the University of Poitiers. Their guidance and support have been the key to all my achievements. Their expertise, patience and encouragement have given me a deeper understanding and higher motivation during my research. Moreover, they always encouraged me to keep exploring and trying. I still remember one time when David told me not to worry that my operations would kill Cadence software. All these were like sparks that helped me to cross one obstacle after another. In addition, I would like to thank them for their precious and valuable feedback and comments that I have greatly benefited from during the process of writing my articles and dissertation.

I would also like to acknowledge Mr. Yann Deval, Professor at the University of Bordeaux; Mr. Philippe Ferrari, Professor at the University of Grenoble Alpes; Mr. Philippe Descamps, Professor at the Ecole Nationale Supérieure d'Ingénieurs de Caen (ENSICAEN); Mr. Bruno Barelaud, Professor at the University of Limoges; Mr. Florin Hutu, Maître de Conférences at the Institut National des Sciences Appliquées de Lyon (INSA Lyon); Mr. Francis Huin, Engineer at the IDDO-IC; whom I am very honored to have as the committee members for my oral defense. I am equally grateful to them for their examinations of my dissertation and for all their valuable comments and suggestions.

Special thanks are given to my dear colleagues from the IDDO-IC, Mr. Sébastien Charpentier, Mr. Matthieu Lecuyer, Mr. Sébastien Vauclair, Mr. Lewis Macdonald and others. Starting from the initial installation and configuration of the PDK to the various details of the circuit design and layout, their constant guidance meant a lot to me. In addition, their selfless care and assistance in my work and life made me feel at home. Of course, I also enjoyed the jokes they occasionally shared, even though some of them were not so funny. My sincere thanks also go to Ms. Emmanuelle Baldinger for helping me with many administrative tasks and keeping me worry-free. Time flies, but the memories

of my time at IDDO-IC will stay with me forever.

I would like to sincerely thank the members of the ReSYST research group, including Mr. Claude Duvanaud, Mr. Smail Bachir, former and current Ph.D. students (Tayeb, Younès, Nuraddeen, Abdulrazaq, Manuel, Bhanu, etc.). I would also like to thank other colleagues and friends, Maxime, Mohamed, Sergueï, Dounia, Baptiste, Georgian, etc. I have to say that they have consistently provided me with invaluable assistance and have supported, encouraged, and accompanied me throughout my academic journey.

Lastly, I would like to thank all my sisters and brothers (Yan Li, Yu Li, Wei Li, Liang Li, Kongliang Liu, Sanqiang Cen, Meng Liu) for their enduring love and encouragement. Especially, I would like to express my deepest appreciation to my lovely parents Zhanguo Li and Xinju Zhang. I will forever be grateful for their unconditional love, their endless sacrifices, and their unwavering faith in me.

Zhigang Li

March 2023

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List of Abbreviations

ACC	Adaptive Cruise Control
ADAS	Advanced Driver Assistance Systems
ADC	Analog-to-Digital Converter
ADPLL	All-Digital Phase-Locked Loop
AM	Amplitude Modulation
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
CMOS	Complementary Metal-Oxide-Semiconductor
CPPLL	Charge-Pump Phase-Locked-Loop
DAC	Digital-to-Analog Converter
DCO	Digitally Controlled Oscillator
DSP	Digital Signal Processor
EDA	Electronic Design Automation
FD-SOI	Fully Depleted Silicon-On-Insulator
FinFET	Fin Field-Effect Transistor
FMCW	Frequency-Modulated Continuous-Wave
FoM	Figure-of-Merit
FoMT	Figure-of-Merit including FTR
FSCW	Frequency-Stepped Continuous-Wave
FSK	Frequency Shift-Keying
FTR	Frequency-Tuning Range
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HCI	Hot-Carrier Injection
HF	High Frequency
IC	Integrated Circuit
InP	Indium Phosphide
LDO	Low-dropout Regular
LFM	Linear Frequency Modulation
LNA	Low-Noise Amplifier
LPF	Low-Pass Filter

LRR	Long-Range Radar
MMIC	Monolithic Microwave Integrated Circuit
MRR	Medium-Range Radar
OTH	Over-The-Horizon Radar
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PM	Phase Modulation
PN	Phase Noise
PVT	Process, Voltage, and Temperature
Q-factor	Quality factor
RF	Radio Frequency
RO	Ring Oscillator
RX	Receiver
SDM	Sigma-Delta Modulator
SiC	Silicon-Carbide
SiGe	Silicon-Germanium
SoC	System-on-Chip
SRR	Short-Range Radar
TDC	Time-to-Digital Converter
TX	Transmitter
UHF	Ultra-High Frequency
VCO	Voltage Controlled Oscillator
VHF	Very-High Frequency

General Introduction

As one of the core sensors for advanced driver assistance systems (ADAS), the automotive radar is becoming mainstream for applications such as obstacle detection and automatic cruise control. Meanwhile, the millimeter-wave (mm-W) band, 76 – 81 GHz, is promised to be a long-term solution for automotive radar development as it allows for a smaller antenna size, uncrowded spectrum, larger bandwidth, etc. In particular, the frequency-modulated continuous-wave (FMCW) automotive radar greatly benefits from the high carrier frequency and the large bandwidth to improve its angular and radial resolution, which is also inseparable from the linear triangular or sawtooth chirp generated by the phase-locked loop (PLL).

However, some bottlenecks of the analog PLL are revealed at deep nanoscale CMOS nodes. For instance, the chip area of PLL does not decrease significantly with process scaling, and it is difficult to migrate it from one process to another, leading to long design cycles and high costs. Based on these facts, implementing PLLs like digital circuits has recently been a hot research topic, i.e., all-digital phase-locked loop (ADPLL). Compared to the analog PLL, the ADPLL shows excellent prospects in terms of low cost, small area, low power consumption, easy integration, and high compatibility with other digital baseband circuits. As one of the essential building blocks of ADPLLs, Digitally Controlled Oscillators (DCO) are employed to generate a periodic waveform with a frequency that can be digitally controlled, making them a versatile and flexible alternative to traditional analog Voltage-Controlled Oscillators (VCO). While numerous DCOs operating at frequencies below 10 GHz have been published so far, reports of those operating above 10 GHz are scarce. There is even less material on the design challenges of K-band DCOs and the solutions to address them.

In such a context, the objective of this thesis is not only to investigate the feasibility of designing a K-band DCO in an advanced 22 nm FD-SOI process, but also the proposed DCOs need to meet stringent specifications to be suitable for 76 – 81 GHz FMCW automotive radars, such as achieving low phase noise, wide tuning range, and high frequency resolution simultaneously, which is quite challenging.

Chapter I aims to comprehensively review the research background related to automotive radars, frequency synthesis techniques, and oscillators. We will begin by

presenting an overview of the principles, structures, categories, operating bands, and processes relevant to automotive radars, followed by a brief review of the research conducted on 76 – 81 GHz automotive radars. This will highlight the significant commercial value of this research topic. Next, we will review some common frequency synthesis techniques and emphasize the basic theory and main modules of PLLs and ADPLLs, while also comparing them to show the potential of ADPLLs for future applications. Finally, we will introduce the theory and types of oscillators and conduct a brief analysis of their phase noise performances. These are crucial factors in DCO design and serve as the theoretical foundation for the discussion in later chapters.

In Chapter II, we will begin by briefly introducing GlobalFoundries' 22 nm FD-SOI process, including the flipped well structure, the back-gate biasing technique, and the available components in the library. We will then compare different DCO topologies, focusing on LC-based DCOs, as well as classical frequency tuning techniques. We will also briefly introduce the fundamental theory of FMCW radars and DCO gain calibration for chirp linearity. Our main focus will be on the design and implementation of a K-band low-phase-noise triple-bank DCO (T-DCO) for 76 – 81 GHz automotive radars. We will not only discuss the design difficulties and important considerations, but also provide a theoretical analysis and a detailed presentation of the switched-capacitor structure used, along with a novel back-gate-based fine-tuning structure. Finally, we will compare the post-layout simulation results of the T-DCO with the specifications and other state-of-the-art DCOs to demonstrate the feasibility of designing a K-band DCO in a 22 nm FD-SOI process. This will further solidify the potential of using this process for high-frequency applications such as automotive radars.

In Chapter III, we will first briefly elucidate the frequency overlap problem that arises in a multi-bank DCO, as well as the complex frequency calibration and linearization problems. In order to address these issues at the design level rather than only at the algorithmic level, we will present a new dual-bank DCO (D-DCO) prototype that has seldom been disclosed before. We will describe the circuit implementation in detail, along with the key considerations and design challenges. Finally, we will compare the post-layout simulation results of the D-DCO with the specifications to verify its compliance with the 76 – 81 GHz automotive radar requirements.

CHAPTER I

Introduction to Research Work

This research work aims to design a high-performance digitally controlled oscillator (DCO). It is a core module of an all-digital phase-locked loop (ADPLL) that will be used in 76 – 81 GHz automotive radars. Therefore, this chapter focuses on presenting and reviewing the background in the existing literature related to the research purpose. In Section I.1, we will briefly introduce the development footprint, main architectures and principles of automotive radars. In Section I.2, the fundamentals of frequency synthesizers will be elaborated, followed by an introduction and comparison of PLLs and ADPLLs. In Section I.3, we will mainly present the theory and types of oscillators, and finally their phase noise is analyzed.

I.1. Automotive Radar

I.1.1. Radar Fundamentals

Radar is an acronym standing for Radio Detection and Ranging. As the name implies, it uses radio/electromagnetic (EM) waves to detect the targets. The first practical radar was invented by the British physicist Robert Watson-Watt and his team in 1935, and a flying bomber was clearly detected in their experiment. During the World War II, radar was developed explosively in the military field. Today, radar plays an important role in our daily life owing to its wide variety of applications in many fields:

- Military: airborne early warning radar, airborne ground surveillance radar, anti-aircraft artillery radar, missile guidance radar, fire control radar;
- Air traffic control and navigation: airport surveillance radar, precision approach;

- Meteorology and geography: weather (rain, fog, snow, hail, etc.) surveillance radar, wind profiling radar, millimeter cloud radar, imaging radar, 3D radar;
- Traffic and road safety: radar speed gun, anti-collision radar, blind-spot detection radar, car parking/reversing radar, automatic cruise control system.

Such diverse applications are inseparable from the inherent properties of the EM waves used in radar. For example, EM waves propagate at the speed of light ($c = 3 \times 10^8$ m/s) and are highly immune to the environment and weather conditions, making radar capable of rapidly determining the location, speed, orientation, etc., of aircraft, ships or other invisible objects at long distances. In addition, radar often works together with different types of sensors to provide better and more comprehensive performances, among which ultrasonic and optical sensors are commonly used, especially in the automotive industry, which is the theoretical basis for autonomous driving technology.

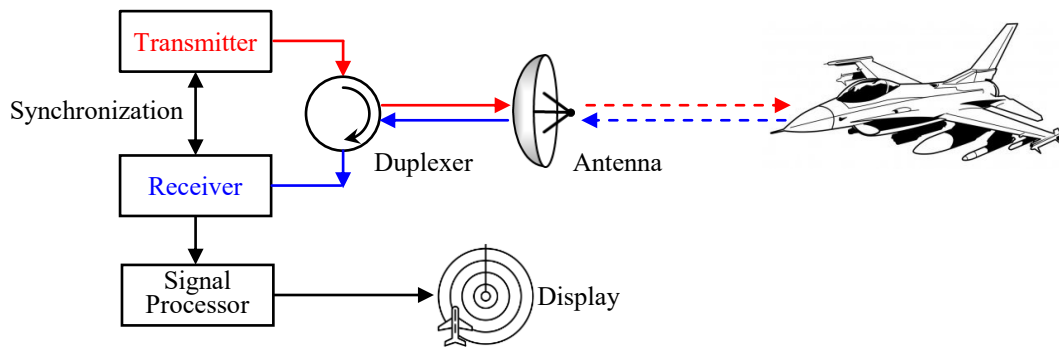


Figure I.1.1 Simplified block diagram of a radar system.

A simplified block diagram of a radar system is shown in [Figure I.1.1](#). Although the details of radar systems are not identical, their sub-modules basically contain a transmitter, an antenna, a receiver, a signal processor and a display. The radio frequency (RF) signal of interest is generated by the transmitter and amplified to a sufficient power level to reach the desired maximum range detection, and then emitted outward to a target through an antenna. Owing to the atmospheric attenuation of signal propagation, a small portion of the signals reflected by the target (also called an echo) can return to the antenna, where they are amplified and demodulated by the receiver. The target characteristics can then be extracted and displayed by processing these received signals. Moreover, it is possible to use a single antenna for both transmission and reception, and the antenna can be switched alternatively between the transmitter and receiver through a duplexer (or circulator). This switching is necessary because it prevents powerful transmit signals from entering the sensitive receiver. Otherwise, the receiver may be damaged or destroyed.

I.1.1.1. Radar-Frequency Bands

Table I.1.1 Standard radar-frequency letter band nomenclature.

Band designation	Nominal frequency range	Specific frequency ranges for radar based on ITU assignments		
		Region 1	Region 2	Region 3
HF	3 – 30 MHz			
VHF	30 – 300 MHz	None	138 – 144 MHz	223 – 230 MHz
			216 – 225 MHz	
UHF	300 – 1000 MHz	420 – 450 MHz		
		890 – 942 MHz		
L	1 – 2 GHz	1215 – 1400 MHz		
S	2 – 4 GHz	2300 – 2500 MHz		
		2700 – 3600 MHz	2700 – 3700 MHz	
C	4 – 8 GHz	4200 – 4400 MHz		
		5250 – 5850 MHz	5250 – 5925 MHz	
X	8 – 12 GHz	8.5 . 10.68 GHz		
Ku	12 – 18 GHz	13.4 – 14 GHz		
		15.4 – 17.7 GHz		
K	18 – 27 GHz	24.05 – 24.25 GHz	24.05 – 24.25 GHz	24.05 – 24.25 GHz
			24.65 – 24.75 GHz	
Ka	27 – 40 GHz	33.4 – 36 GHz		
V	40 – 75 GHz	59 – 64 GHz		
W	75 – 110 GHz	76 – 81 GHz		
		92 – 100 GHz		
mm	110 – 300 GHz	136 – 148.5 GHz		
		151.5 – 155.5 GHz		
		231.5 – 235 GHz		
		238 – 248 GHz		
THz	300 – 1000 GHz	300 – 3000 GHz		

The characteristics and applications of radars are mainly determined by their operating frequencies, and most radar systems have a frequency range from approximately 3 MHz to 300 GHz, which means that the wavelengths of the emitted electromagnetic waves are between 1 mm and 100 m ($\lambda = c/f$, where λ is the wavelength, c is the speed of light, and f is the carrier frequency). In order to distinguish such wide radar-frequency bands, radar systems engineers have used band letter designations as a short notation for describing the operating frequencies. The IEEE standard radar-frequency letter band nomenclature is given in [Table I.1.1](#) [I-1]. The band designations mainly include HF, VHF, UHF, L, S, C, X, Ku, K, Ka, V, W, mm, and THz. Moreover, some specific bands are assigned for radar by the International Telecommunication Union (IUT) depending on the regions.

Figure I.1.2 illustrates the atmospheric absorption versus frequency at sea level and 4 km altitude for water density of 7.5 g/m³ and 1 g/m³, respectively [I-2], [I-3]. It should be noted that the major atmospheric constituents absorbing radar energy are oxygen (O₂), water (H₂O) and other gaseous molecules, the absorption is usually neglected at frequencies of 300 MHz and lower, but becomes increasingly important at mm-Wave frequencies.

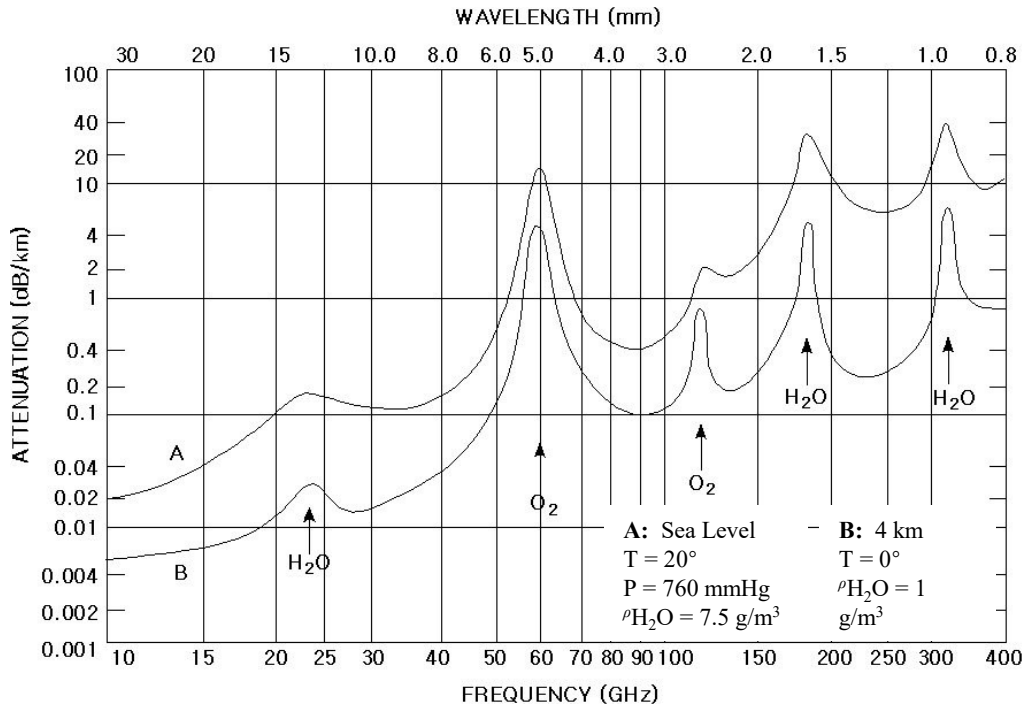


Figure I.1.2 Atmospheric absorption at altitudes of sea level and 4 km.

The main factors affecting the choice of the frequency band for radars can be summarized as: usage scenario, antenna size, detection distance, resolution, atmospheric attenuation, available bandwidth, process and cost, and so on [I-4]. Generally, the radars in HF, VHF and UHF bands are commonly used for ultra-long-range detection, such as tracking and searching for satellites and ballistic missiles, because of the low atmospheric attenuation. In addition, radars below 300 MHz can detect targets beyond the horizon using the refractive effect of the ionosphere on electromagnetic waves, known as over-the-horizon radar (OTH). However, the spectrum below 1 GHz is crowded because civil radio communications occupy the channels. The notation L refers to the large antenna or long range. The L-band radars have a relatively wide bandwidth and high emitted power, making them suitable for modern long-range air surveillance up to a range of about 400 km. The notation S means the small antenna or short range. Most land-based and shipborne radars are in this band, where the atmospheric attenuation is higher than in the

L-band, so the radars require a much higher emitted power to achieve long-range detection. Moreover, some special airport surveillance radars also use this band to detect aircraft within 120 km. Most mobile military battlefield and weather radars are based on C-band, allowing for quick installation, good angular accuracy and reasonable resolution.

The radar in Ku and K bands are commonly used as airborne radars, maritime navigation radars and imaging radars (spaceborne or airborne), which have appropriately small antennas and adequate angular accuracy. The high-frequency K and Ka bands are heavily influenced by weather and atmospheric attenuation. Therefore, radars in these bands are suitable for some short-range scenarios such as traffic radars, terrain avoidance and terrain tracking radars. The mm-Wave radars in V, W and mm bands offer a series of advantages in terms of the large spectrum space, low latency time, compact antenna size and high resolution. However, they also suffer from severe atmospheric attenuation, and three attenuation peaks occur at about 60 GHz, 120 GHz and 180 GHz, coinciding with the resonant frequencies of the oxygen and water molecules (Figure I.1.2). Correspondingly, there are some frequency windows between these peaks where the atmospheric attenuation is relatively lower, and most mm-Wave applications are within these windows, such as 76 – 81 GHz automotive radars.

I.1.1.2. Mono-static and Multi-static Radars

The physical configurations of the antennas can classify the radars into monostatic and multi-static (including bistatic) as shown in Figure I.1.3. A traditional radar in which the transmitting and receiving antennas are located in the same place is referred to as a monostatic radar, regardless of whether single or two antennas are used. A multi-static radar system contains two or more transmitting or receiving antennas, which are all far apart compared to the size of the antennas [I-5].

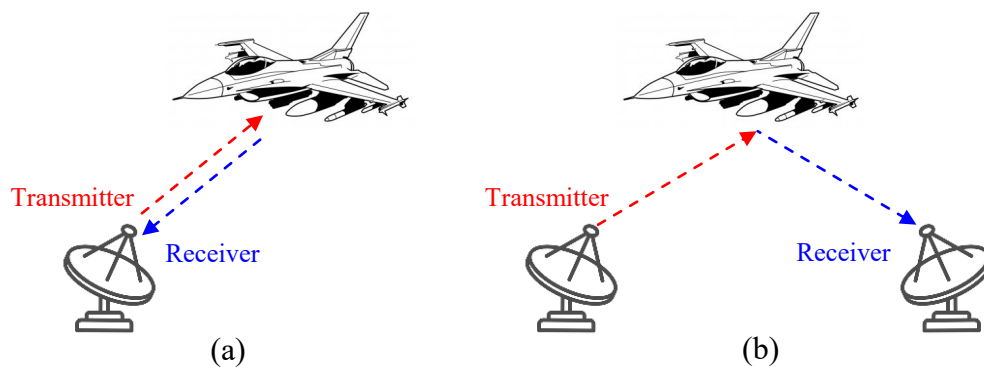


Figure I.1.3 Radar configurations. (a) Monostatic. (b) Bistatic.

In a monostatic radar system, the time and phase synchronization between transmission and reception can be performed by the same frequency source and clock, resulting in a relatively simple structure. Moreover, for most short-range civil scenarios, the radar size can be petite because of the low emitted power required, such as automotive radars. In military applications, the monostatic radar can also be equipped inside the rocket head to track and attack aircrafts, tanks, etc.

Multi-static radar offers some advantages over monostatic radar in cases where the reflected energy from the target is deficient, such as long-range and weather radars. Furthermore, it allows more comprehensive observations of targets from different transmit-receive pairs, thereby adding potentially valuable information. Hence, it is more likely to detect stealthy objects and less susceptible to interference. However, in such a separated system, a precise standard time reference and complex algorithms are required for synchronization and data processing.

I.1.1.3. Radar Equation

The radar equation quantitatively describes the relationship between the radar parameters, the detection distance, and target characteristics [I-6]. Assuming that a target is located at a range of R from the radar, P_t is the radar transmitted power, and G_t is the transmit antenna gain, the directional power density S_1 at this target is given by

$$S_1 = \frac{P_t G_t}{4\pi R^2} \quad (\text{I. 1. 1})$$

The reflected power P_1 by the target is

$$P_1 = S_1 \cdot \sigma = \frac{P_t G_t \sigma}{4\pi R^2} \quad (\text{I. 1. 2})$$

where σ is the radar cross section (RCS). A target with a larger RCS means that it is more easily detected. The returned power density S_2 at the radar is given by

$$S_2 = \frac{P_1}{4\pi R^2} = \frac{P_t G_t \sigma}{(4\pi R^2)^2} \quad (\text{I. 1. 3})$$

Thus, the total received power P_r by the radar is

$$P_r = S_2 \cdot A_e \quad (\text{I. 1. 4})$$

where A_e is the effective antenna aperture. The relationship between the receive antenna gain G_r , the wavelength λ , and A_e can be expressed as

$$G_r = \frac{4\pi A_e}{\lambda^2} \quad (\text{I. 1.5})$$

Substituting (I.1.5) into (I.1.4), the total received power P_r is therefore written as

$$P_r = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 R^4} \quad (\text{I. 1.6})$$

If the minimum received power that can be detected by the radar is $P_{r,min}$, then the maximum achievable range R_{max} can be derived as

$$R_{max} = \sqrt[4]{\frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 P_{r,min}}} \quad (\text{I. 1.7})$$

I.1.1.4. Pulsed and Continuous-Wave Radars

According to the waveform of the radar signal, radar can be classified into pulsed radars and continuous-wave (CW) radars [I-7]-[I-10]. Pulsed radars transmit short and powerful pulses and receive echo signals from the target, which means that the transmission and reception are separated, so pulsed radars can utilize only one antenna. CW radars transmit continuous waves and receive echo signals while transmitting, i.e., transmission and reception are simultaneous, so it requires two independent antennas.

I.1.1.4.1. Pulsed Radar

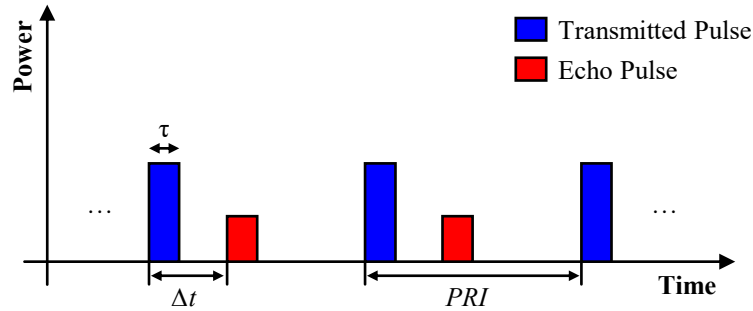


Figure I.1.4 Range measurement principle of the pulsed radar.

The range measurement principle of the pulsed radar is shown in [Figure I.1.4](#). Typically, the transmitter emits a train of rectangular pulses, each pulse has a width τ of about 0.1 to 1 microsecond (μs). During this pulse emission, the receiver is isolated from the antenna to protect its sensitive components from the high-power transmit pulse. Once the pulse emission is completed, the receiver is connected to the antenna, enabling it to pick up the reflected echo signals from the target. The distance R between the radar and the target can then be measured by simply calculating the round-trip time Δt from the

pulse emission to the reception of its return, which is given by

$$R = \frac{c \cdot \Delta t}{2} \quad (\text{I. 1. 8})$$

Note that the pulse is emitted periodically with a pulse repetition interval PRI , so the pulse repetition frequency PRF can be written as

$$PRF = \frac{1}{PRI} \quad (\text{I. 1. 9})$$

The transmitted duty cycle D represents the ratio between τ and PRI and is given by

$$D = \frac{\tau}{PRI} = \tau \cdot PRF \quad (\text{I. 1. 10})$$

If the transmitted pulse is a square wave, its average power P_{av} is equal to its peak power P_t multiplied by its duty cycle D , which can be expressed as:

$$P_{av} = P_t \cdot D = P_t \cdot \tau \cdot PRF \quad (\text{I. 1. 11})$$

P_{av} is crucial because it determines the potential detectable range of the pulsed radar. To maximize the detection range, P_{av} can be increased by three means: improving the PRF , enlarging τ , and increasing P_t .

In addition, to avoid the range ambiguity, the echo pulse must be received before the next pulse is emitted, which means that the round-trip time Δt of the radar pulse must be less than its PRI , and this relation can be defined as

$$\Delta t = \frac{2R}{c} \leq PRI \quad (\text{I. 1. 12})$$

Therefore, the maximum unambiguous range R_{max} is

$$R_{max} = \frac{c \cdot PRI}{2} = \frac{c}{2PRF} \quad (\text{I. 1. 13})$$

The minimum detectable range R_{min} (or blind distance) depends on the radar pulse width τ . When the front of the echo pulse reaches the antenna while the radar is still in transmission mode, the round-trip time Δt cannot be determined. Considering the recovery time t_r of the duplexer, R_{min} is approximately given by

$$R_{min} \approx \frac{c \cdot (\tau + t_r)}{2} \quad (\text{I. 1. 14})$$

In the above range measurements, only the amplitude of the echo pulse is employed. In

order to further acquire the velocity of the target v_t , the frequency of the echo pulse has to be extracted and compared with that of the transmitted pulse, and the resulting frequency difference f_d is known as a Doppler shift. This coherent radar is also referred to as pulsed Doppler radar, and the relationship between the Doppler frequency shift and the velocity of the target can be expressed as

$$f_d = \frac{2v_t}{\lambda} \quad (\text{I. 1. 15})$$

where λ is the wavelength of the transmitted pulse.

Another important parameter is the resolution, which represents the capability of the radar to distinguish between two or more adjacent targets, whether in range, angle, or frequency. Let's take the range resolution as an example, if two targets are close enough, their reflected echo pulses will be merged or overlapped, and they will be considered as the same target in the receiver. The minimum resolvable range is defined as the range resolution ΔR , which is proportional to the pulse width τ . The relationship is

$$\Delta R = \frac{c \cdot \tau}{2} \quad (\text{I. 1. 16})$$

Therefore, the fine range resolution can be achieved by shortening the pulse. Recall that in this case, the average power (or pulse energy) will be correspondingly decreased, which makes the detection more difficult. To solve this contradiction, pulse compression techniques are used to maintain the pulse energy while providing better range resolution by modulating the amplitude, phase, or frequency of the pulse signal.

Pulsed radars have shown excellent performances in some long-range scenarios such as weather radars, over-the-horizon (OTH) radars, and satellite-based remote sensing radars. However, they are rarely used in short-range scenarios due to their minimum detectable range which is limited by the pulse width and the switching time of the duplexer. Meanwhile, the accurate target localization also requires additional information about the antenna directionality, which further increases the complexity of the system.

I.1.1.4.2. Continuous-Wave Radar

Unlike pulsed radar, CW radar continuously transmits EM wave, and its waveform may be considered as a sine wave with constant frequency. The velocity of the target can be measured by Doppler shift, but not the range. Therefore, the EM wave must be modulated so as to obtain the round-trip time for the range determination. There are

several ways to modulate a frequency in time, such as linear frequency modulation (LFM), frequency shift-keying (FSK), and frequency-stepped continuous-wave (FSCW) modulation [I-11]. Among them, the LFM method consists in varying the signal frequency linearly with time, and it is the most commonly used method in automotive radars.

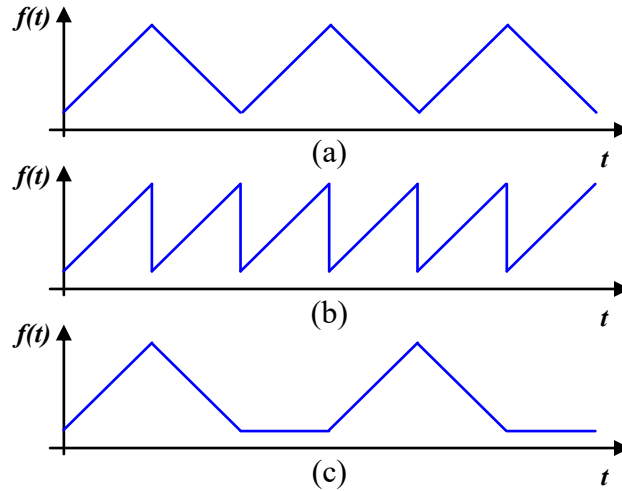


Figure I.1.5 LFM methods. (a) Linear triangular frequency modulation. (b) Linear sawtooth frequency modulation. (c) Segmented linear frequency modulation.

Typically, the LFM waveform of a CW radar changes periodically as shown in [Figure I.1.5](#). The frequency $f(t)$ is the instantaneous frequency. Moreover, three LFM methods are widely employed, namely linear triangular frequency modulation, linear sawtooth frequency modulation, and segmented linear frequency modulation. The LFM waveform is often referred to as a chirp because in early radar systems this waveform would produce a chirping sound similar to that made by birds. The term chirp is also used interchangeably with sweep signal. Moreover, CW radars using the frequency modulation method are also known as frequency-modulated continuous-wave (FMCW) radars.

I.1.1.5. Transceiver Architectures

As the core of wireless communications and radar systems, the transceiver acts as the link between the digital signal processor (DSP) and the RF antenna usually consisting of two or more independent transmitter and receiver chains. The transmitter is used to up-convert a modulated signal to a higher RF signal, which is then amplified to a specific power level to drive the antenna. The receiver is used to filter, amplify and down-convert the received weak signals while suppressing external interferences (e.g., noise, jamming,

and clutter). The choice of transceiver architectures is mainly determined by complexity, performance, cost, and power consumption. In the following, we will take a representative PLL-based transmitter and a superheterodyne receiver as examples to briefly elaborate their principles. Another commonly used homodyne architecture will not be presented here, but some details can be found in [I-12], [I-13].

I.1.1.5.1. PLL-Based Transmitter

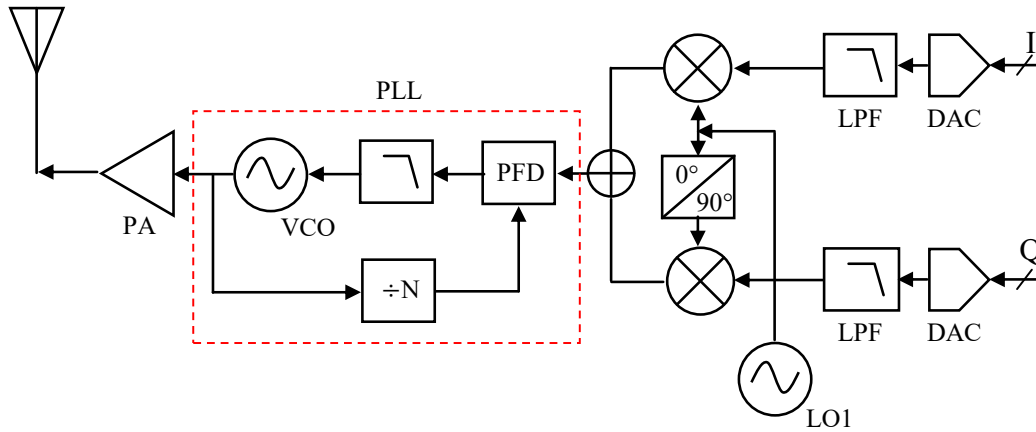


Figure I.1.6 Block diagram of a PLL-based transmitter.

The block diagram of a typical PLL-based transmitter is shown in [Figure I.1.6](#), which is usually employed in FMCW radars. The PLL is followed and modulated by a reference signal from the output of the quadrature I/Q modulator (or a high-precision clock). The out-of-band noise generated by the I/Q modulator can be suppressed if the loop bandwidth of the PLL is appropriately selected, so the output RF filter can be omitted and the output noise of the transmitter at large frequency offsets is mainly determined by the VCO employed [I-14]. Therefore, this architecture permits some advantages such as low phase noise, low power consumption, and high linearity. However, a major challenge is to reduce the lock-in time of the PLL to further lower the power consumption.

Another critical issue is that this architecture is limited to the systems using constant amplitude modulation (AM) because the modulated PLL does not reproduce AM information. The polar modulation architecture can be used to address this issue. For example, the output signal of the modulator is divided into the amplitude and phase components. Phase modulation (PM) is still performed by the PLL, and an additional mixer prior to the PA is added to apply the AM. More details can be found in [I-15].

I.1.1.5.2. Superheterodyne Receiver

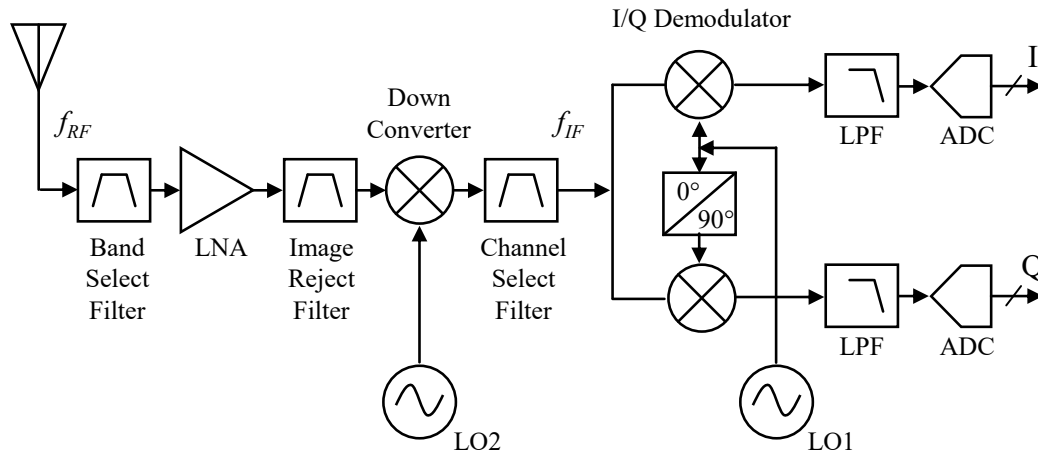


Figure I.1.7 Block diagram of a typical superheterodyne receiver.

The block diagram of a commonly used superheterodyne receiver is shown in [Figure I.1.7](#). Generally, the superheterodyne receiver employs two (or more) stages of down-conversion. The RF signal received by the antenna is first filtered by the band-select filter, which allows to select the whole receiver band and to remove unwanted out-of-band interferences. It is then amplified by a low-noise amplifier (LNA) and down-converted to the intermediate frequency (IF) signal by a frequency mixer connected with the RF local oscillator (LO2). The LNA is critical to reach good reception sensitivity. Before and behind the frequency mixer, the image-reject filter and channel-select filter are required to suppress the image frequency and to select the frequency band of the desired channel, respectively. The second down-conversion is performed by the I/Q demodulator and IF local oscillator (LO1), which converts this resulting IF signal to baseband quadrature I and Q signals (i.e., two 90° phase shifted signals). The 90° phase shift is carried out with a polyphase filter or a frequency divider to produce two IF signals with a 90° phase difference. The low-pass filters (LPF) in the I and Q channels are used to filter out the mixing high-frequency components and further attenuate interferences. The analog-to-digital converter (ADC) converts the baseband analog signals to digital signals for further processing in the digital signal processor (DSP).

Note that the choice of the IF is critical for the superheterodyne architecture. As depicted in [Figure I.1.8](#), the useful RF signal at frequency f_{RF} and its undesired image signal at frequency f_{IM} are symmetrically located above and below the LO2 frequency f_{LO2} , and they can both be converted to the IF signal at frequency f_{IF} through the mixing operation. To eliminate this image frequency f_{IM} , an image-reject filter is necessary to be

placed before the mixer, which has a large attenuation around f_{IM} and a relatively small loss around f_{RF} . Since the frequency difference between f_{IM} and f_{RF} is $2f_{IF}$, a higher IF leads to a better rejection of the image frequency. However, the IF cannot be too high, otherwise the interference nearby the IF is hard to be filtered out by the channel-select filter because of the limitation of its quality factor (Q -factor). Therefore, the trade-off between image rejection and channel selection should be well considered when determining the IF. In addition, the image rejection can also be performed by the Hartley and Weaver architectures, the corresponding principles are detailed in [I-16], [I-17].

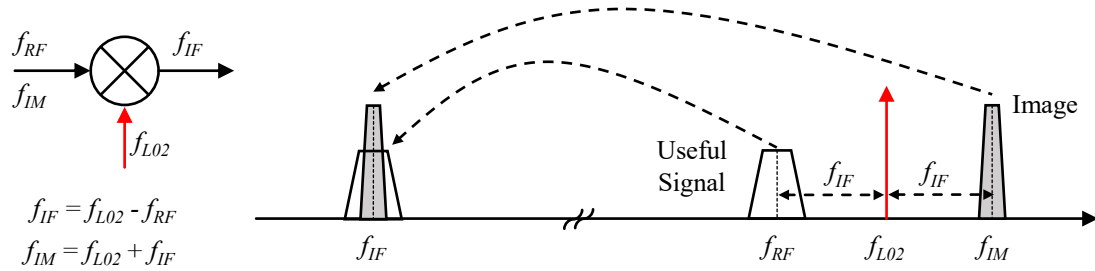


Figure I.1.8 Impact of the image frequency on the spectrum of the useful signal.

Nevertheless, in superheterodyne receivers, high-performance image-reject filters are still required. Passive filters, such as surface acoustic wave (SAW) or high-order LC filters, are frequently employed. They typically have a large physical size and are difficult to integrate, leading to an increase in design complexity, power consumption, and cost. However, the use of IF and multiple filters in the superheterodyne architecture enables a wide dynamic range of reception and excellent suppression of interference, thus improving its selectivity and sensitivity.







I.1.2. Automotive Radar for Autonomous Driving

Autonomous driving usually refers to self-driving vehicles that relies on cutting-edge technologies such as powerful processors, multi-purpose sensors and artificial intelligence to travel without any driver manipulation. Such intelligent vehicles can not only improve the travel efficiency by planning routes and times in advance, but also accurately perceive the road conditions and timely react. In addition, they are capable of avoiding road traffic accidents caused by risky behaviors such as drunk, fatigue or distracted driving. According to the World Health Organization (WHO), about 90% of road traffic accidents are caused by human errors, and more than 1.3 million people die and up to 50 million get injured worldwide each year, making them the leading cause of

death among people aged 15 – 29 years [I-18], [I-19]. These numbers are expected to decrease significantly in the near future with the widespread deployment of autonomous driving technology, which will also bring tremendous social and economic benefits.

I.1.2.1. SAE Levels of Autonomy

In 2014, the Society of Automotive Engineers (SAE) J3016TM standard laid out six levels of autonomy for on-road motor vehicles as shown in [Figure I.1.9](#) [I-20]. These levels span from no automation, partial automation to fully automation. As the level of autonomy increases, the vehicle will take over more of the operations of the driver.

0. DRIVER	1. FEET OFF	2. HANDS OFF	3. EYES OFF	4. MIND OFF	5. PASSENGER
					
No Assistance	Assisted	Partially Automated	Highly Automated	Fully Automated	Autonomous
Human	Transfer of responsibility				Machine

Source: Evercore ISI, SAE International

Figure I.1.9 Five levels of autonomy.

Most vehicles on the road today are still stuck at level 0, which means they are always under control of the driver. Part of them may be equipped with some electronic or mechanical systems for driving safety, such as automatic emergency braking (AEB) systems and the electronic stability control (ESC) systems, but since these systems do not directly drive the vehicle, they cannot be counted as driving automation.

Some new cars of the latest years can be qualified as level 1, which means that the vehicle can assist the driver to perform simple driving tasks, such as steering, acceleration or braking, but not simultaneously. A driver must control the vehicle and respond to unexpected situations. An example is the collision mitigation braking system (CMBS), which only permits the vehicle to automatically brake when a collision is imminent.

Currently, the majority of automakers have reached the level 2, such as Tesla Autopilot, Volvo Pilot Assist, and Cadillac Super Cruise System. The often-mentioned adaptive cruise control (ACC) allows the vehicle to follow its predecessor at a safe distance, and to maintain cruising speed and lanes on the highway. However, the driver needs to constantly monitor the changes in the surrounding environment and be prepared

to take over the vehicle in case of danger.

At the level 3, the driver no longer needs to take over the vehicle and can close the eyes in ideal road conditions, but still requires vigilance. The vehicle can handle almost all driving tasks independently, and it is highly capable of detecting and processing more details in its surrounding environment. Certain automakers have introduced their commercially available level 3 vehicles, such as the Audi A8L with Traffic Jam Pilot and the Mercedes S-Class with Drive Pilot.

The level 4 and level 5 both reach the fully autonomous driving, and the vehicle can perform all driving tasks without driver intervention. The difference is that the level 4 is applicable to some scenarios, usually in cities or on highways. The level 5 has none of these restrictions, the vehicle does not even need a steering wheel, and the driver becomes a passenger. However, these two levels of vehicles are still in the development and testing phase, and significant investments by some automakers and technology companies are expected to accelerate this process.

I.1.2.2. Advanced Driver-Assistance System

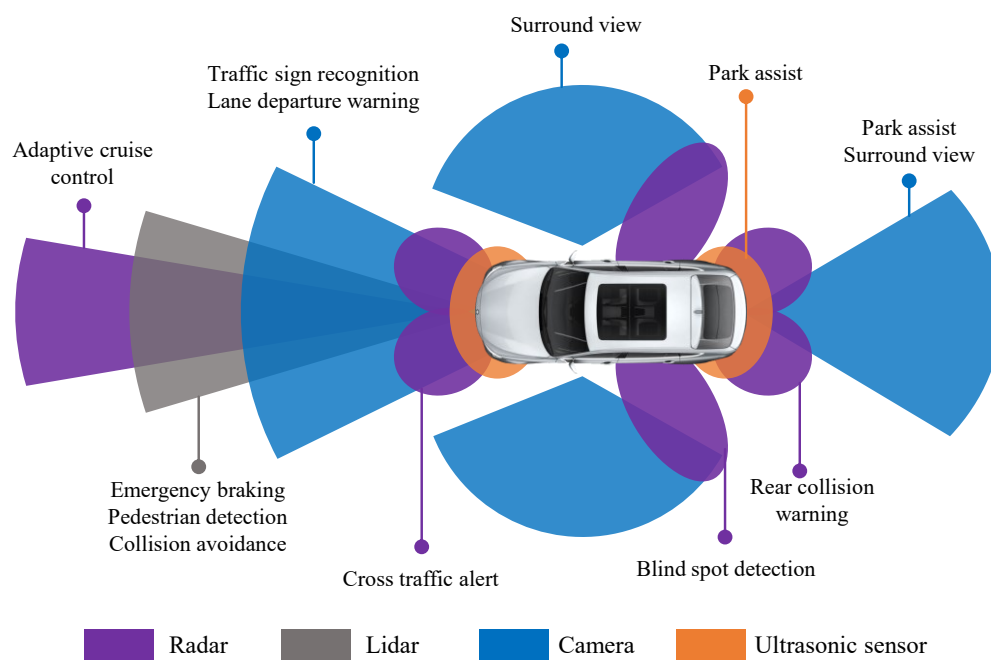


Figure I.1.10 Typical types of sensors used in ADAS.

Note that previously described systems such as AEB, ESC, and ACC all belong to the advanced driver-assistance systems (ADAS). In addition, ADAS also includes the pedestrian protection system (PPS), automatic parking system (APS), night vision system

(NVS), lane keep assistance (LKA), traffic sign recognition (TSR), blind spot detection (BSD), adaptive light control (ALC), etc. The realization of these functions is highly dependent on the sensors employed. [Figure I.1.10](#) illustrates an ADAS platform with multiple sensors and functions integrated [I-9].

The most common sensors in state-of-the-art ADAS are radars, ultrasonic sensors, cameras, and lidars. The primary role is to sense the surrounding environment in real time and provide the vehicle's central processor with accurate and complete data about the road condition, such as obstacles, traffic signals, and road markings.

As the previous sections explain, radar detects a target by emitting EM waves and receiving echoes. Depending on the frequency and bandwidth, radar is widely applied in ADAS scenarios such as ACC and BSD. In addition, it is less affected by weather conditions such as fog, rain, and snow and can operate at night.

Similar to the principle of the radar, ultrasonic sensors use the round-trip time of ultrasound to detect obstacles. Due to the low propagation speed and weak environmental robustness of ultrasound, both the response time and the detection accuracy of ultrasonic sensors are poor. However, because of their low price, they are often adopted in parking systems, and the effective detection range is generally no more than 10 m.

Lidar refers to light detection and ranging, which scans the environment with laser beams. Because the wavelength of the laser signal can reach the nanometer level, lidar offers higher detection accuracy than radar, and it also allows to detect smaller obstacles and construct their high-resolution three-dimensional (3D) images. However, the attenuation of the laser signal in the air is more aggressive (see [Figure I.1.2](#)), especially in harsh weather conditions, so its detection range and stability are lower than those of radar.

Camera sensors are passive sensors that perceive the surrounding environment mainly by capturing real-time image information. Camera sensors permit the acquisition of rich color, contour and brightness information that is impossible with radar and lidar, such as lane monitoring and traffic light recognition. In addition, they also feature mature technology and low price, making them indispensable in autonomous vehicles. The main disadvantages are their sensitivity to light changes and the complexity of image processing algorithms.

[Table I.1.2](#) shows a comparison of the sensors as mentioned earlier in ADAS. It can

be noted that each kind of sensor has its unique advantages and limitations. Therefore, autonomous vehicles usually use several types of sensors in combination to achieve more stable and comprehensive performances. At the same time, as autonomous driving transitions to higher levels, the demand for high-performance sensors becomes more pressing. In particular, automotive radar is growing rapidly and is replacing other sensors as the dominant sensor in autonomous vehicles thanks to its advantages, such as all-weather and all-day capability, easy integration, and cost-effectiveness. A typical example is the 4D imaging mm-Wave radar [I-21]. In contrast to the conventional 3D mm-Wave radar, it can detect not only an object's distance, velocity, and azimuth, but also the vertical height, thus outlining the object.

Table I.1.2 Comparison of sensors in ADAS.

Parameters	Ultrasonic	Lidar	Camera	Radar
Detection range	10 m	150 m	100 m	250 m
Response time	Long	Short	Medium	Short
Velocity measurement	Fair	Poor	Poor	Excellent
Object identification	Poor	Medium	Good	Poor
Weather robustness	Poor	Fair	Fair	Good
Algorithm complexity	Low	High	High	Medium
Cost	Low	High	Medium	Medium

I.1.2.3. Automotive Radar Frequency Bands

Automotive radar was first proposed around the 1960s [I-22]-[I-27]. Some early automotive radar systems are shown in Figure I.1.11, their implementations are mainly based on existing two-terminal diode devices, such as GUNN and Schottky diodes, which suffered from low operating frequencies and large volumes.



Figure I.1.11 Early automotive radar systems. (a) 10 GHz radar in the early 1970s. (b) 16 GHz radar in 1975. (c) 35 GHz radar in 1974.

Later, 24 GHz, 60 GHz, and 77 GHz frequency bands were introduced into

automotive radar almost simultaneously. Among them, the 60 GHz frequency band was mainly settled in Japan as a result of political considerations. The 77 GHz frequency band was officially assigned as a global standard for automotive radar by the World Administrative Radio Conference (WARC) in 1989. It was not until 1992 that the 24 GHz automotive radar system developed by EATON-VORAD became commercially available in the USA. By 1998, Mercedes-Benz's DISTRONIC system using 77 GHz automotive radar was also commercially released in its premium S-Class sedans. Eight years later, two 24 GHz short-range radars (SRR) and one 77 GHz long-range radar (LRR) are integrated into its next-generation DISTRONIC PLUS system. The safety, stability, and comfort of vehicles were significantly improved.

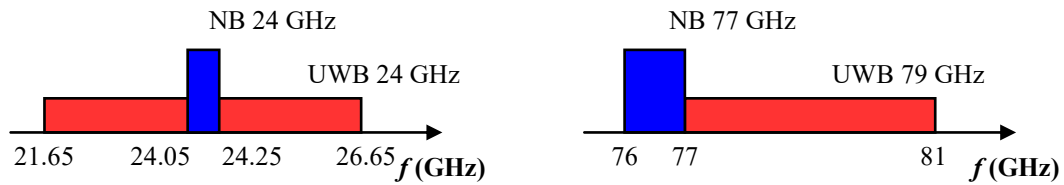


Figure I.1.12 Frequency bands for automotive radars.

In 2002, the Federal Communications Commission (FCC) allocated an ultra-wideband of 22 – 29 GHz for SRR automotive radars in North America. In the same year, Europe also started the standardization process. Finally, two UWBs were allocated for SRR automotive radars at approximately 24 GHz and 79 GHz as shown in [Figure I.1.12](#). The first band, 21.65 – 26.65 GHz, was authorized on 17 January 2005. The other band, 77 – 81 GHz, was authorized in March 2004. In addition, two narrow bands (NB) of 24.05 – 24.25 GHz and 76 – 77 GHz were already available, mainly for LRR automotive radars. Subsequently, these bands dominated the global automotive radar market.

In fact, 24 GHz UWB was only a temporary option. In 2013, the European Telecommunications Standards Institute (ETSI) and the FCC decided to phase out this 24 GHz UWB. One reason is that the spectrum is crowded as it covers the industrial, scientific, and medical (ISM) band of 24 – 24.25 GHz. Moreover, 77 GHz automotive radars outperform 24 GHz automotive radars in many aspects, such as antenna size, resolution, and accuracy. Thus, 24 GHz UWB is no longer applied to new autonomous vehicles from 1 January 2022, which is also known as the “sunset date”.

I.1.2.4. Automotive Radar Classification

It is worth mentioning that there are various classifications of automotive radar, which

can generally be separated in three categories according to the effective detection distance: long-range radar (LRR), medium-range radar (MRR) and short-range radar (SRR). Current autonomous vehicles are equipped with about seven automotive radars (e.g., one LRR, two MRRs and four SRRs). [Table I.1.3](#) summarizes the technical characteristics of these three automotive radar systems operating in the frequency band of 76 – 81 GHz.

Table I.1.3 *Automotive radar characteristics in 76 – 81 GHz frequency band.*

Type	LRR	MRR	SRR
Frequency band	76 – 77 GHz	77 – 81 GHz	77 – 81 GHz
Maximum transmit power (EIRP)	55 dBm	33 dBm	33 dBm
Bandwidth	600 MHz	600 MHz	4 GHz
Distance range	10 – 250 m	1 – 100 m	0.15 - 30 m
Distance resolution	0.5 m	0.5 m	0.1 m
Distance accuracy	0.1 m	0.1 m	0.02 m
Velocity resolution	0.6 m/s	0.6 m/s	0.6 m/s
Velocity accuracy	0.1 m/s	0.1 m/s	0.1 m/s
Angular accuracy	0.1°	0.5°	1°
3 dB beamwidth azimuth	±15°	±40°	±80°
3 dB beamwidth elevation	±5°	±5°	±10°

The LRR operating at 76 – 77 GHz features a maximum equivalent isotropically radiated power (EIRP) of 55 dBm and a large detection range of up to 250 m, which is primarily deployed at the front of automotive vehicles for ACC. A narrow bandwidth of 600 MHz is sufficient to obtain a moderate distance resolution of 0.5 m and a velocity resolution of 0.6 m/s. Moreover, a precise angular accuracy of 0.1° and a 3 dB beamwidth azimuth of ±15° are necessary to achieve a narrow field of view (FOV).

The MRR operating at 77 – 81 GHz provides a maximum detection range of 100 m with an allowable EIRP of 33 dBm. Compared to the LRR, the MRR has comparable bandwidth, distance resolution, and velocity resolution, but requires a 3 dB beamwidth azimuth of ±40° to cover a wider area. The main applications include, but are not limited to, lane-change assistance, cross-traffic alerts and rear collision warnings.

The SRR also operating at 77 – 81 GHz offers a maximum detection range of 30 m with an allowable EIRP of 33 dBm, which often adopt the FMCW method to achieve a fine distance resolution of 0.1 m thanks to the UWB of 4 GHz. Moreover, the 3 dB beamwidth azimuth of ±80° provides a large coverage area surrounding the vehicle, allowing for features such as pedestrian and cyclist detection, parking assistance.

I.1.3. Technologies Trends in Automotive Radar

This section provides an overview of semiconductor technologies applicable to mm-Wave automotive radars operating in the frequency band of 76 – 81 GHz [I-28]-[I-30]. Historically, semiconductors have evolved for three generations. The first generation of semiconductors was mainly based on silicon and germanium, such as the conventional CMOS process. Their early development followed Moore's law, and the technology was relatively mature and widely used in large-scale integrated circuits. However, at deep nanometer nodes, silicon processes are becoming increasingly crucial in RF and mm-Wave circuits. Second- and third-generation semiconductors are mainly based on III-V compounds. Compared to first-generation semiconductors, they feature superior high-temperature and high-frequency performances. Second-generation semiconductors, such as gallium arsenide (GaAs) and indium phosphide (InP), are widely used in optoelectronic and wireless communication devices. The prominent representatives of the third-generation semiconductors are gallium nitride (GaN) and silicon-carbide (SiC), which offer tremendous advantages in high-frequency and high-power scenarios such as 5G and electric vehicles. However, they are still in their infancy.

A comparison of the approximate unit gain cut-off frequencies (f_T) achieved by these semiconductor technologies is given in Table I.1.4. In general, the maximum frequency of oscillation (f_{max}) is much higher than f_T . Considering that the maximum operating frequency in RF circuit design should be one-half to one-third of f_T , it can be concluded that all these advanced processes can support 76 – 81 GHz automotive radars due to the high f_T of over 250 GHz.

Table I.1.4 Cutoff frequencies for various semiconductor technologies.

Process	GaAs mHEMT	GaN HEMT	InP HBT	SiGe HBT	RF CMOS 45 nm
f_T	1000 GHz	300 GHz	500 GHz	250 GHz	400 GHz

However, like other mm-Wave integrated circuits (ICs), the mm-Wave radars were previously dominated by III-V compound semiconductors (primarily GaAs). For example, Mercedes-Benz's first commercially available 77 GHz automotive radar utilized GaAs Gunn diodes embedded in a waveguide cavity as the mm-Wave signal source. Compared to silicon semiconductors, III-V compound semiconductors have shown some superior electrical characteristics, such as high electron mobility and low resistive parasitic, thus

making them suitable for high-performance mm-Wave applications such as PAs and LNAs, as well as enabling oscillators with excellent phase noise properties. However, the GaAs process has some inherent disadvantages, such as the high difficulty of wafer fabrication and few available metal layers, resulting in high cost and low integration for early mm-Wave radars. Since the chip is the product of a trade-off between performance, cost and benefit, this determines that GaAs will not replace silicon as the dominant semiconductor material.

The emergence of silicon-germanium (SiGe) process can be dated back to 1980, IBM doped germanium into silicon material in order to increase the flow rate of electrons and reduce power consumption. Starting in 1998, IBM officially announced that the SiGe process was in mass production. A significant advantage of the SiGe process is that it is highly compatible with the mature silicon process. It not only has the integration and cost advantages of the silicon process, but also has the advantages of the GaAs process in terms of speed. Since about 2007, mm-Wave radars have officially entered the SiGe era, and its cost has dropped about 50% compared to that of the GaAs process. In addition, the SiGe BiCMOS process, which combines the high-speed and high-gain characteristics of bipolar transistors, can integrate RF, analog and digital circuits on a single chip, significantly reducing the number of external components while optimizing power consumption. Currently, 0.13 μm SiGe transistors with f_T and f_{max} in excess of 250 GHz occupy a pivotal position in the automotive radar market.

Figure 1.1.13 compares the f_T and f_{max} of SiGe BiCMOS [I-31]-[I-37] and CMOS processes [I-38]-[I-46] at different nodes. It can be seen that under 0.18 μm process, the f_T of SiGe BiCMOS process is about 250 GHz, the f_T of CMOS process is about 60 GHz. Empirically, the operating frequency in the RF circuit design should be about one-third of f_T . Thus, SiGe BiCMOS process can allow an operating frequency of about 80 GHz, while the CMOS process can only reach about 20 GHz. In order to achieve similar operating frequencies as the SiGe BiCMOS process, CMOS-based circuits must use smaller process nodes.

More recently, those CMOS processes with f_T and f_{max} greater than 200 GHz have started to gradually penetrate the 76 – 81 GHz automotive radar field, such as the advanced 65 nm, 45 nm, 28 nm and 22 nm process nodes. Obviously, some of their key characteristics have been disclosed and need to be carefully considered when designing.

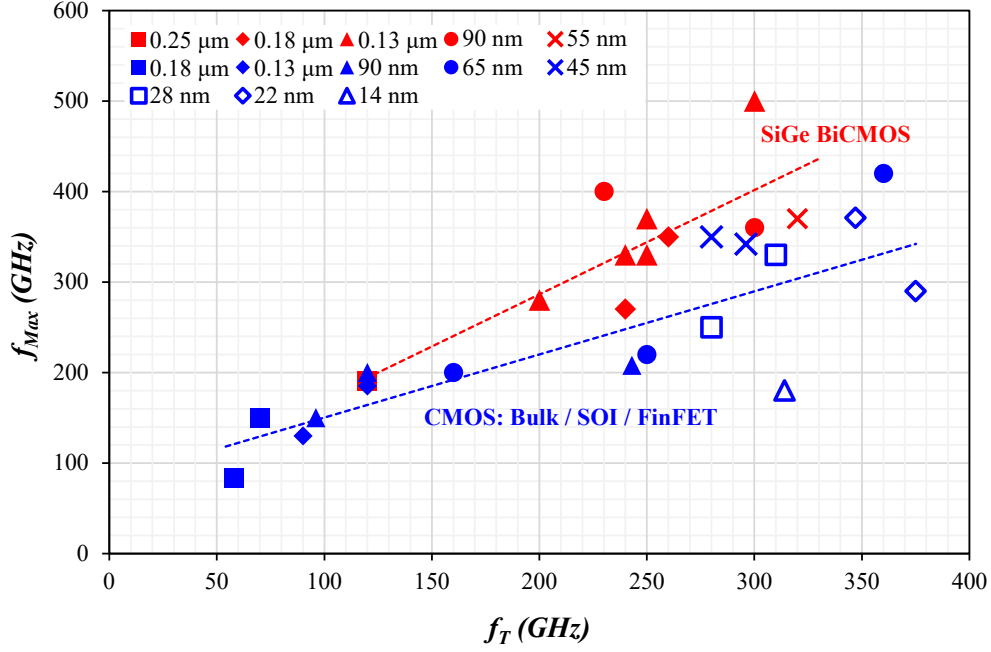


Figure I.1.13 Comparison of f_T / f_{max} collected from published papers. (a) SiGe BiCMOS. (b) CMOS-Bulk/SOI/FinFET.

- Because of the smaller nodes, mature processes, and more available metal layers, these nanoscale CMOS processes can achieve extremely high levels of integration at a very low cost. For example, GlobalFoundries' 22 nm fully depleted silicon-on-insulator (FD-SOI) technology provides up to 10 layers of metal.
- Nanoscale planar CMOS processes permit the supply voltage as low as about 1 V, thus making them very suitable for low-power designs. However, their relatively high threshold voltage of about 0.5 V results in very low headroom voltages, which greatly increases the difficulty of the design.
- Note that the noise performances of nanoscale CMOS processes is still not as good as that of SiGe and GaAs processes.
- FD-SOI technology fits very well into the nanoscale CMOS process. For example, with f_T and f_{max} of about 350 GHz, the 22 nm FD-SOI technology provides the best mm-Wave performances in the most advanced submicron nodes (above 14 nm). This process isolates the entire channel from the substrate via a buried oxide layer, featuring low parasitic capacitance and high speed. Meanwhile, the back-gate bias technique permits more design flexibility and is well suited for low-voltage, low-power applications. More details will be presented in Chapter II.
- The fin field-effect transistor (FinFET) technology is much more complicated than

planar FD-SOI technology. Its 3D gate resembles a fish fin surrounding the channel and thus provides better control. This structure can significantly reduce the leakage current and also significantly shorten the gate length of the transistor, such as the 14/16 nm nodes commonly used today. However, the f_T and f_{max} of FinFET is lower than those of FD-SOI, so the FinFET process currently lacks sufficient attractiveness in mm-Wave radars.

I.1.4. Examples of 76 – 81 GHz FMCW Automotive Radars

In the bibliography, there are a number of researches on automotive radar systems. In this section, several representative papers from academic and commercial fields are cited to introduce the current progress in this field.

I.1.4.1. Academic Works

I.1.4.1.1. J. Lee et al., 2010 [I-47]

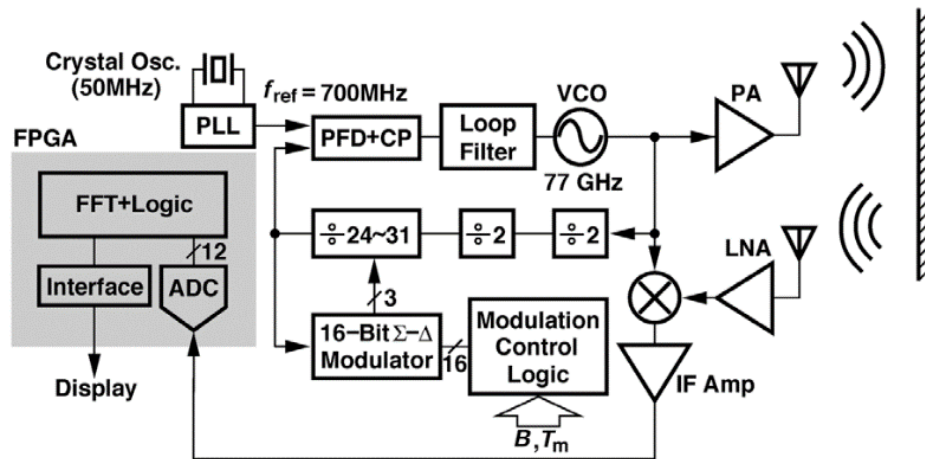


Figure I.1.14 Schematic of the fully integrated 77 GHz FMCW radar transceiver in 65 nm CMOS technology.

This research work from National Taiwan University was published in 2010. A 77 GHz fully integrated FMCW automotive radar system is proposed, and it is also one of the first monolithic microwave integrated circuit (MMIC) to integrate the entire radar transceiver. As illustrated in Figure I.1.14, the transmitter utilizes an analog fractional-N frequency synthesizer to generate the triangularly FMCW signal, while the reference of this frequency synthesizer is set to 700 MHz, which is provided by an external 50 MHz crystal oscillator-based PLL. The received signal is processed by an external FPGA-based signal processor and the corresponding speed and distance information can then be

extracted. Moreover, the 77 GHz VCO utilizes a standard LC resonant structure with a thick-oxide (5.6 nm) varactor to suppress the leakage, and the frequency tuning range is about 1 GHz. The mm-Wave PA and LNA are integrated on the chip to improve the emitting power and the receiving sensitivity. The implementation of this radar transceiver is based on TSMC's 65 nm CMOS process with a chip area of $0.95 \times 1.1 \text{ mm}^2$, and it consumes 243 mW from a 1.2 V supply voltage.

I.1.4.1.2. H. Jia et al., 2016 [I-48]

This research work from Tsinghua University was published in 2016. The simplified schematic of this 77 GHz fully integrated frequency doubling two-path phased-array FMCW transceiver is given in Figure I.1.15. Compared with the previous one, the output frequency (triangular wave) of this analog fractional-N frequency synthesizer is reduced to about 38.5 GHz, and 77 GHz is achieved by a frequency doubling circuit, which not only reduces the design complexity of the frequency synthesizer (primarily VCO) but also enlarges the maximum chirp bandwidth to 1.93 GHz. In addition, the frequency doubler adopts an injection-locked structure, which is placed between the frequency synthesizer and the PA, providing a favorable isolation. Consequently, the frequency synthesizer no longer needs to drive the PA, which relaxes the requirement for its output power. Two LNAs and a PA are integrated on the chip to provide sufficient bandwidth and gain, and the LNAs can be digitally controlled to further improve frequency calibration capabilities. This automotive radar transceiver is fabricated in a 65 nm CMOS process with a total area of 4.64 mm^2 including pads, and it consumes 343 mW from a 1.2 V supply voltage.

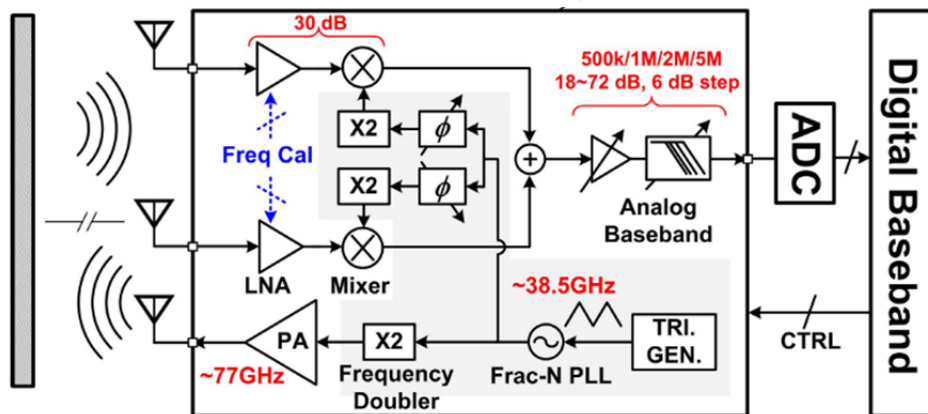


Figure I.1.15 Schematic of the 77 GHz frequency doubling two-path phased-array FMCW transceiver for automotive radar.

I.1.4.1.3. T. Ma et al., 2019 [I-49]

This research work also from Tsinghua University was published in 2019. The simplified schematic of this fully integrated 76 – 81 GHz FMCW transceiver is depicted in Figure I.1.16. First, unlike the previous two, this radar transceiver has a large bandwidth tuning capability from 250 MHz to 4 GHz, so it can meet the requirements of Table I.1.3 for SRR, MRR and LRR. That means it is suitable for both short-range and long-range scenarios, which is one of the main trends of current automotive radar. Then, it integrates two transmitters (TXs) and three receivers (RXs) for multiple-input multiple-output (MIMO) processing. The two TXs can be quickly switched on and off by a bottom-switching PA for bi-phase modulation. In addition, a mixed-mode PLL is proposed, which mainly contains a delay-locked loop (DLL)-based cursor time-to-digital converter (TDC), a digital loop filter, and a current DAC-based VCO oscillating at about 38.5 GHz. It can regulate the loop bandwidth and rapidly generate reconfigurable sawtooth chirps for achieving high-precision distance and angular resolution. This radar transceiver prototype is based on a 65 nm CMOS process with a chip area of 7.29 mm² and a total power consumption of 921 mW.

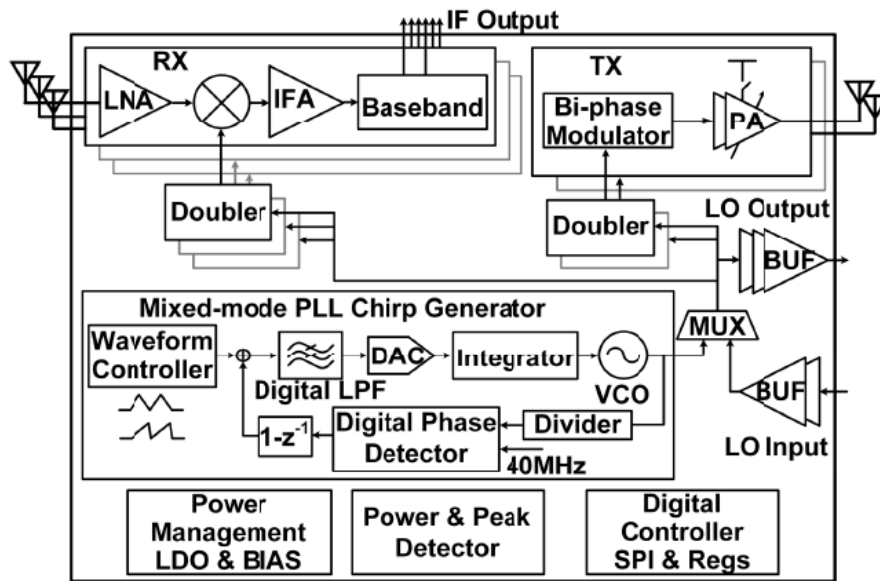


Figure I.1.16 Schematic of the CMOS 76 – 81 GHz 2-TX 3-RX FMCW radar transceiver based on mixed-mode PLL chirp generator.

I.1.4.2. Commercial Works

I.1.4.2.1. H. P. Forstner et al., 2008 [I-50]

This research work from Bosch was published in 2008. As illustrated in Figure I.1.17,

a commercially available 77 GHz fully integrated 4-channel automotive radar transceiver was implemented. It is also the first radar chip using the SiGe process at 77 GHz and is fabricated based on Infineon's automotive-compliant B7HF200 SiGe bipolar technology for Bosch's LRR3 system. This SiGe-MMIC integrates all necessary components such as VCO, buffer amplifier, active mixer, IF amplifier, coupler and external ceramic resonator. The FMCW signal at 76 – 77 GHz is generated by the differential Colpitts-based VCO. The buffer amplifier is dedicated to guarantee high output power and temperature stability. The 19 GHz dielectric resonant oscillator (DRO) is used as a reference oscillator, mixed with the divided-by-4 RF frequency (77 GHz) to generate an IF signal, which serves as an input to the PLL of the Radar-ASIC. The modulation control and the signal pre-processing (pre-amplification, A/D conversion, filtering) are integrated in the Radar-ASIC. The SiGe-MMIC is mounted on a multi-layer PCB and bonded to the RF substrate on the top of the PCB, and the patch antenna is also placed on the RF substrate. In addition, the radar has four receiver channels, two of which are used as transmit/receive channels simultaneously. The total power consumption of this radar transceiver is about 4 W from a 5.5 V supply voltage and allows operating temperature from -40 °C to +125 °C.

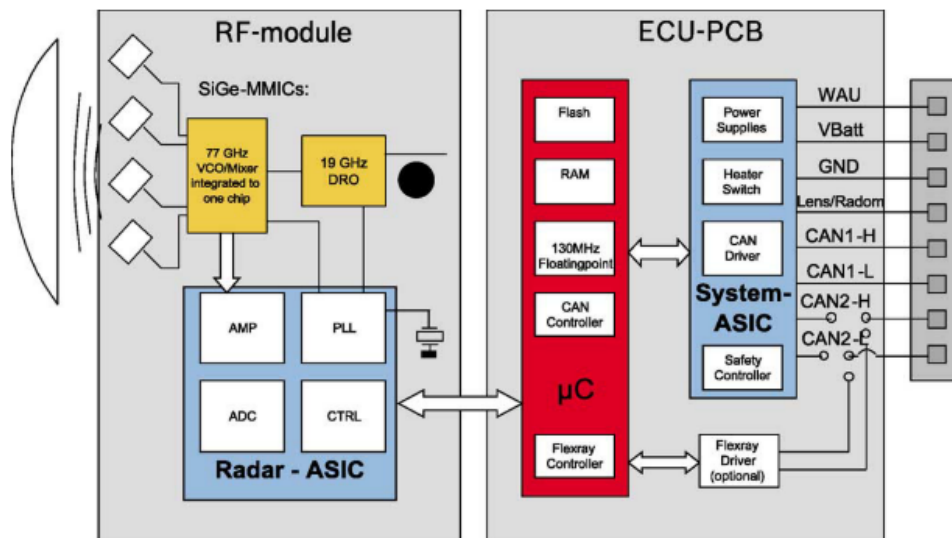


Figure I.1.17 Schematic of the Bosch's LRR3 system.

I.1.4.2.2. T. Usugi et al. 2020 [I-51]

This recent research work from Denso was published in 2020. [Figure I.1.18](#) illustrates the simplified block diagram of this fully integrated 77 GHz automotive radar transceiver, which consists of a 3-channel TX, an 8-channel RX, a PLL, power and temperature compensation modules, and the corresponding digital control module. Since the advanced

CMOS process is strongly affected by process, voltage, and temperature (PVT) variations, a highlight of this transceiver is the compensation mechanism used to mitigate the impact of PVT variations on the radar transceiver. The building blocks of the transmitter are PA, frequency multiplier, phase shifter (PS) and power compensation loop. The power compensation loop is composed of a power detector and a digital module to control the transmit power, which guarantees a constant transmit power over the bandwidth. The receiver has a very low NF for receiving weak reflected signals from remote obstacles. The conventional fractional-N PLL employs a 50 MHz crystal oscillator as the reference clock. The LC-based VCO oscillates at 38.5 GHz with a bandwidth of 1 GHz. The generation of the FMCW signal is controlled by a 3rd order multi-stage noise shaping (MASH) cell and a ramp-up counter, and its linearity is enhanced by the pulse width modulation (PWM) technique. Furthermore, the modules sensitive to supply voltage are powered uniformly by low-dropout regulators (LDOs) to reject common-mode noise from the external power supply and to suppress supply voltage variation with temperature. This automotive radar prototype is implemented in a 40 nm CMOS process with a chip area of $2.7 \times 6 \text{ mm}^2$ and a maximum detection distance of about 250 m.

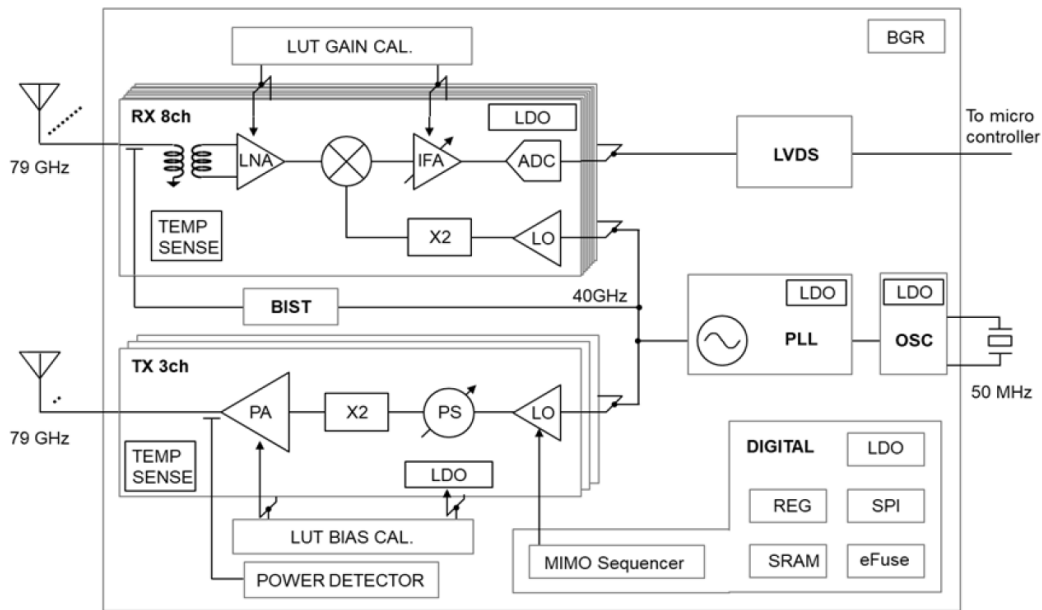


Figure I.1.18 Schematic of the Denso's LRR system.

I.1.4.2.3. P. Ritter et al. 2021 [I-52]

This recent research work from Bosch was published in 2021. [Figure I.1.19](#) illustrates a simplified schematic of this fully integrated 76 – 81 GHz automotive radar evaluation chip, which integrates a 2-channel TX and a 2-channel RX, a DCO, an analog baseband

with ADC and a digital signal processing unit with on-chip memory. Apparently, radar systems are becoming more and more integrated. Moreover, the DCO adopts a cross-coupled structure and achieves a 25 – 27 GHz frequency output by digitally controlling its capacitor banks. A subsequent frequency triplexer upconverts this frequency band (intercepting its 3rd order harmonic) to the 76-81 GHz automotive radar band. The received signal is amplified by a high linearity LNA and down-converted to the IF signal by a passive mixer, then further processed by a high-pass filter and an anti-alias filter. A successive-approximation-register (SAR) ADC converts this IF signal into a digital signal for fast Fourier transform (FFT) processing by an on-chip digital signal processing unit. This radar system-on-chip (SoC) utilizes an industry-leading 22 nm FD-SOI process, with a 14 mm² chip area and a total power consumption of about 0.7 W, and is expected to be the next generation of low-cost and small-size automotive radar.

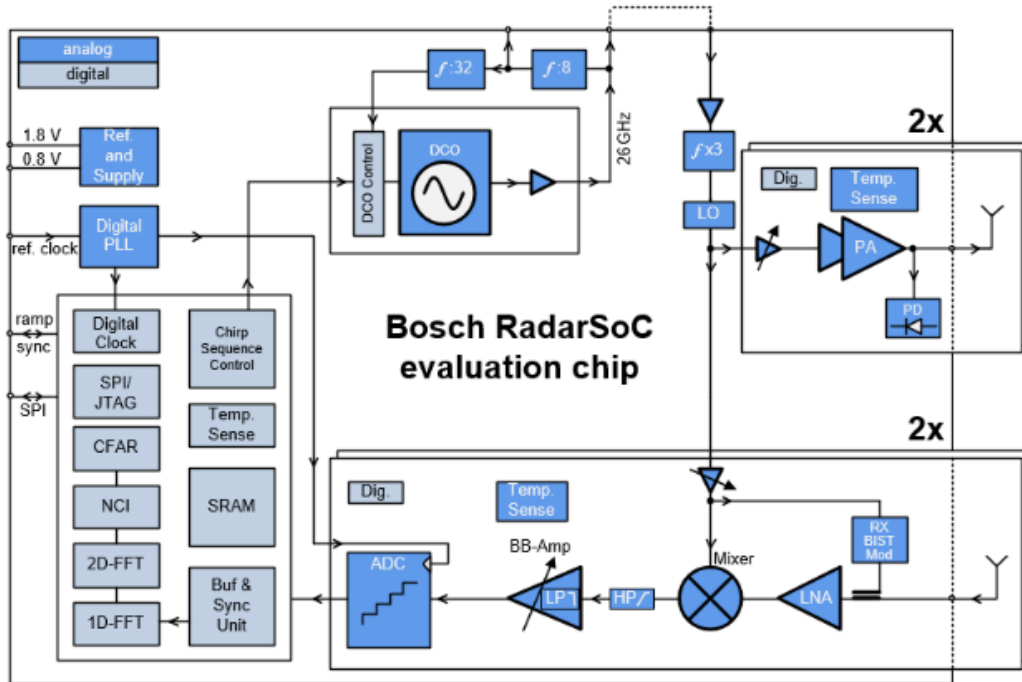


Figure I.1.19 Schematic of the Bosch's 76 – 81 GHz automotive radar.

I.1.4.3. Performance Summary and Comparison

Table I.1.5 summarizes the recently reported 76 – 81 GHz automotive radar transceivers. Note that more and more automotive radars are implemented based on advanced CMOS processes, such as 45 nm and 22 nm. In addition, the combination of multimode functions, i.e., LRR, MRR and SRR, in a single radar SoC using 76-81 GHz FMCW signals, is another important trend. Overall, automotive radars are reducing design complexity and cost through higher integration.

Table I.1.5 Performance summary of 76 – 81 GHz automotive radars

Reference	Technology	FMCW Generator	Frequency (GHz)	TX		RX		Area (mm ²)	Power Consumption (W)
				P _{OUT} (dBm)	PN (@1MHz (dBc/Hz))	Gain (dB)	NF (dB)		
[I-47] JSSC 2010	65 nm CMOS	Fractional-N PLL	77	5.1	-85.53	38.7	7.4 @1MHz	1.04	0.243
[I-53] JSSC 2010	90 nm CMOS	Fractional-N PLL	77	-2.8	-85	23.1	15.6	6.83	0.416
[I-54] TCAS-I 2013	65 nm CMOS	Fractional-N PLL	77	6.4	-85	23	14.8 @1MHz	0.97	0.275
[I-55] TMTT 2015	65 nm CMOS	External PLL	77	8.9	-97.6	13	7.95 @1MHz	2.56	0.468
[I-56] TMTT 2015	65 nm CMOS	Fractional-N PLL	76 – 81	3	-83.43	–	–	2.74	0.32
[I-48] JSSC 2016	65 nm CMOS	Fractional-N PLL	77	13	-81	47.8 – 100.7	5.04 @3.3MHz	4.64	0.343
[I-57] JSSC 2017	0.13 μ m SiGe	External PLL	76 – 81	17	-99	15	10 @1MHz	12.7	1.8
[I-58] ASSCC 2017	28 nm CMOS	Integer-N PLL	79	8.5	-85	45	12 @100MHz	7.9	1
[I-59] ISSCC 2018	45 nm CMOS	Fractional-N PLL	76 – 81	10.8	-94	–	18 @1MHz	22	3.4
[I-49] JSSC 2020	65 nm CMOS	Mixed-mode PLL	76 – 81	13.4	-87.4	26.2 – 78.8	15.3 @600kHz	7.29	0.921
[I-51] RFIC 2020	40 nm CMOS	Fractional-N PLL	76 – 77	11 – 14.1	-91	–	8.7 – 14 @10MHz	46.2	–
[I-60] TCAS-I 2021	65 nm CMOS	Fractional-N PLL	76 – 81	0	–	18 – 66	11 – 26	14.5	0.52
[I-61] EuRAD 2021	22 nm FD-SOI	ADPLL	78	7 – 11	–	16	14.5	14	0.7

I.2. Frequency Synthesizer

As mentioned earlier in Section I.1.1.5, the local oscillator (LO) is one of the key modules of the radar transceiver. It can be employed in the transmitter to synthesize frequency modulated chirp signals for transmitting, and in the receiver to demodulate the received RF signal to extract useful informations. The frequency synthesizer is usually used to provide a stable LO with high spectral purity, which largely determines the overall performances of the transceiver system. Therefore, its design is always a challenge and

needs to take into account many constraints and process influences.

I.2.1. Frequency Synthesis Techniques

The choice of the frequency synthesis technique depends on many factors, such as operating frequency, frequency range, phase noise, frequency resolution, design complexity and cost. There are three main types of frequency synthesis techniques: direct analog, direct digital, and indirect or PLL.

The direct analog frequency synthesizer generally produces the desired frequency directly by multiplying, dividing or mixing a reference frequency source. Its main advantages are short time of frequency synthesis and low phase noise. However, due to the requirement of a great number of frequency dividers, mixers and filters, direct analog frequency synthesizers have the disadvantages of large size, complex structure, high spurious and high-power consumption. This method is mainly used in the instrumentation, and is generally not applicable to communication systems.

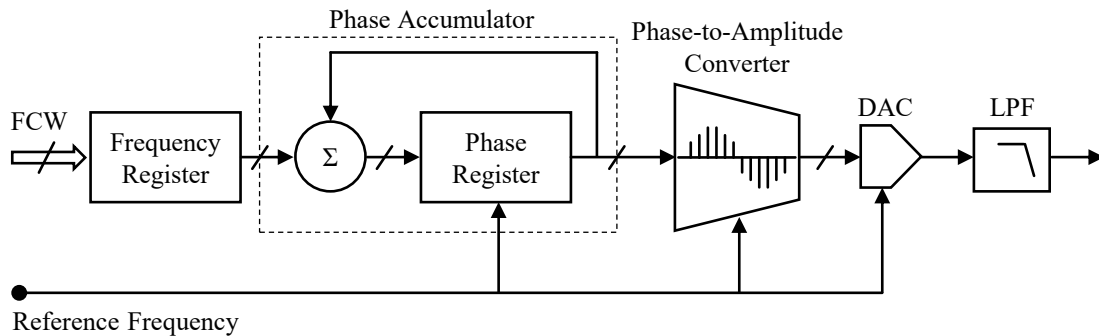


Figure I.2.1 Simplified block diagram of a DDS.

The direct digital frequency synthesizer (DDFS) generates the desired frequency directly by manipulating the phase. The simplified block diagram is shown in [Figure I.2.1](#). The frequency control word (FCW) regulates the phase step of the phase accumulator and then finds the corresponding amplitude using a known phase-to-amplitude conversion table. These digital amplitude signals are sent to the DAC module and converted into analog stepped signals, which are finally processed by the LPF to obtain the desired analog output signals.

In addition to the DAC and filter, the DDS is implemented mainly through digital technology, thus offering a high level of integration and low cost. Meanwhile, the short frequency switching time and low phase noise make it suitable for advanced digital

modulation techniques such as frequency shift keying (FSK) and frequency hopping. Moreover, by modifying the phase-to-amplitude conversion table, flexible output waveforms such as sine, triangle or sawtooth can be obtained. Unfortunately, the DAC process inevitably introduces digital quantization errors, which in turn lead to phase and amplitude distortions. In addition, there are other problems such as large spurs, truncation errors in the phase accumulator, limited word length of the conversion table and leakage of the clock signal. All these factors also limit the achievable frequencies to a few gigahertz.

For operating frequencies up to tens of gigahertz, an indirect frequency synthesizer is generally required. Currently, the implementation of indirect frequency synthesizers is mainly based on PLL, which combines phase feedback and phase-locking techniques to synthesize frequencies. This synthesis technique has the advantages of high output frequency, low phase noise, strong spurious suppression, low cost, and easy integration. It will be highlighted in the following subsections.

I.2.2. Phase-Locked Loop Fundamentals

In general, PLLs are used to lock the phase and frequency of an oscillator to provide a stable output signal. This output signal frequency is usually a multiple of a high-precision reference frequency, such as that of a crystal oscillator, which also makes it possible to use the same PLL to generate different output frequencies. In addition, since the change in phase with respect to time can be used to calculate the corresponding frequency, the frequency can also be locked as long as the phase of the oscillator is locked.

I.2.2.1. PLL Building Blocks

The PLL is a closed-loop feedback control system. In case of a phase difference between the output frequency of the PLL and the input reference frequency, the error is fed back to the VCO input for frequency correction so that the phase difference is gradually reduced to zero, i.e., the PLL reaches a locked state. As a result, the PLL is able to generate one or more output signals synchronized to the input reference signal [I-62].

The current mainstream RF synthesizers are still based on the analog charge-pump PLL (CPPLL) structure. As depicted in [Figure I.2.2](#), a typical CPPLL consists of the following modules: phase-frequency detector (PFD), charge pump, loop filter, voltage-controlled oscillator (VCO) and frequency divider.

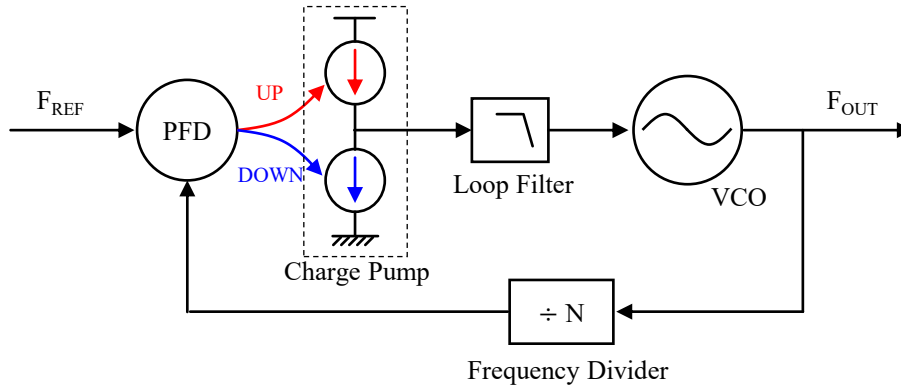


Figure I.2.2 Simplified block diagram of a typical CPPLL.

The PFD is primarily used to compare the phase difference between the reference frequency and the PLL output frequency, and output two pulse signals UP and DOWN. The charge pump controls the two current sources to charge and discharge the post-stage capacitor depending on the UP and DOWN signals, respectively, and converts the current signal into a voltage signal to drive the VCO. The loop filter (usually an analog LPF) is employed to suppress the spurs caused by the PFD during phase comparison and by the charge pump during charging and discharging, so as to produce a smooth control voltage and reduce the jitter in the VCO output frequency. The VCO is the heart of the PLL and is responsible for generating the desired oscillation frequency. The phase noise of the VCO directly determines the overall noise performances of the PLL. The frequency divider divides the high output frequency of the VCO, and the divided frequency is sent to the PFD for comparison with the reference frequency.

I.2.2.2. PLL Transfer Functions

We all know that the PLL, as a feedback system, is essentially a nonlinear circuit. However, when the PLL is in the locked state, its loop behavior is well suited to be characterized by a linear model, which is essential for analyzing the loop stability as well as the noise contribution, etc.

Since the parameter of interest in a PLL is the phase rather than the frequency, the phase relationship between the input and output of each module in the PLL needs to be considered and used to construct the transfer function of the PLL. [Figure I.2.3](#) gives a linear s -domain (Laplace transform) model of a typical analog PLL. The PFD can be represented by $(\phi_i - \phi_d) \cdot K_{PFD}$, where $(\phi_i - \phi_d)$ is the input-output phase difference, and K_{PFD} is the gain of the PFD and the charge pump. $F(s)$ is the transfer function of the loop filter. The VCO can be characterized by an integrator with a gain of K_{VCO} (since frequency

is the derivative of phase with respect to time) and its transfer function can be expressed as K_{VCO}/s . The input-output phase relationship of the frequency divider is $\phi_d = \phi_o / N$. Therefore, the open-loop transfer function $G(s)$ of the PLL can be written as

$$G(s) = \frac{\phi_o(s)/N}{\phi_e(s)} = \frac{K_{PFD}F(s)K_{VCO}}{Ns} \quad (\text{I. 2. 1})$$

Open-loop gain typically decreases monotonically with the frequency, with at least one pole at zero frequency. Moreover, the order of the PLL is defined by the number of the poles of the open-loop transfer function and equals the order of the loop filter plus one. The type of the PLL is defined by the number of the integrators (poles at the origin or at zero frequency) within the loop. Many critical characteristics of the loop are determined by the type of the PLL, such as the commonly used type-II PLL.

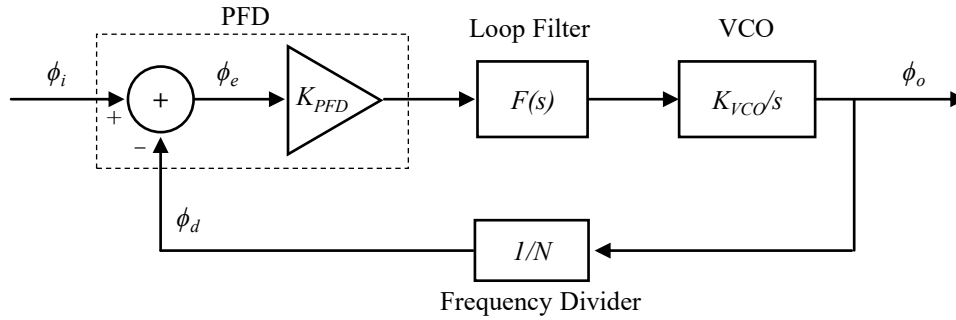


Figure I.2.3 Linear s -domain model of a typical analog PLL.

The closed-loop transfer function $H(s)$ of the PLL is given by

$$H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{G(s)N}{1 + G(s)} = \frac{K_{PFD}F(s)K_{VCO}N}{Ns + K_{PFD}F(s)K_{VCO}} \quad (\text{I. 2. 2})$$

It can be seen that the closed-loop transfer function is a low-pass function with a DC gain equal to N . Its cutoff frequency is the bandwidth of the PLL. In addition, in order to simplify the analysis, we assume that a simple first-order RC low-pass filter is used as the passive loop filter whose transfer function $F(s)$ can be written as

$$F(s) = \frac{1}{1 + RCs} = \frac{1}{1 + \frac{s}{\omega_{LPF}}} \quad (\text{I. 2. 3})$$

where ω_{LPF} represents the cutoff frequency or -3 dB bandwidth of the LPF. The closed-loop transfer function $H(s)$ of this second-order PLL can then be rewritten as

$$H(s) = \frac{K_{PFD}K_{VCO}N\omega_{LPF}}{Ns^2 + N\omega_{LPF}s + K_{PFD}K_{VCO}\omega_{LPF}} \quad (I.2.4)$$

According to the classical feedback control theory, $H(s)$ can be reformulated into the standard form as

$$H(s) = \frac{N\omega_n^2}{s^2 + 2\xi\omega_ns + \omega_n^2} \quad (I.2.5)$$

The natural frequency ω_n and the damping factor ξ are given by

$$\omega_n = \sqrt{\frac{\omega_{LPF}K_{PFD}K_{VCO}}{N}} \quad (I.2.6)$$

$$\xi = \frac{1}{2} \sqrt{\frac{\omega_{LPF}N}{K_{PFD}K_{VCO}}} \quad (I.2.7)$$

The two poles of the closed-loop transfer function can be expressed as

$$s_{1,2} = -\xi\omega_n \pm \sqrt{(\xi^2 - 1)\omega_n^2} = (-\xi \pm \sqrt{\xi^2 - 1})\omega_n \quad (I.2.8)$$

When $\xi = 1$, the closed-loop transfer function has two coincident real poles and the system is in a critically damped state. When $\xi > 1$, there are two symmetric real poles and the system is overdamped. When $\xi < 1$, these two poles become complex and the system is underdamped, and the step response to the input frequency $\omega_{in} = \Delta\omega \cdot u(t)$ can be obtained by the inverse Laplace transform as

$$\omega_{out} = \left[1 - \frac{e^{-\xi\omega_nt}}{\sqrt{1-\xi^2}} \sin(\omega_n\sqrt{1-\xi^2}t + \theta) \right] \Delta\omega \cdot u(t) \quad (I.2.9)$$

where $\theta = \sin^{-1}\sqrt{1-\xi^2}$. Note that this step response includes a sinusoidal component decaying with a time constant $(\xi\omega_n)^{-1}$. As shown in [Figure I.2.4](#), the exponential decay term determines the settling speed of the PLL, and the damping factor should generally be set to about 0.7. Meanwhile, considering the relationship $\xi\omega_n = \omega_{LPF}/2$, there is a critical trade-off between the settling speed and the VCO input interference. The lower the ω_{LPF} , the better the suppression of the high-frequency disturbance generated by the PFD, but the smaller damping factor and the slower the settling speed.

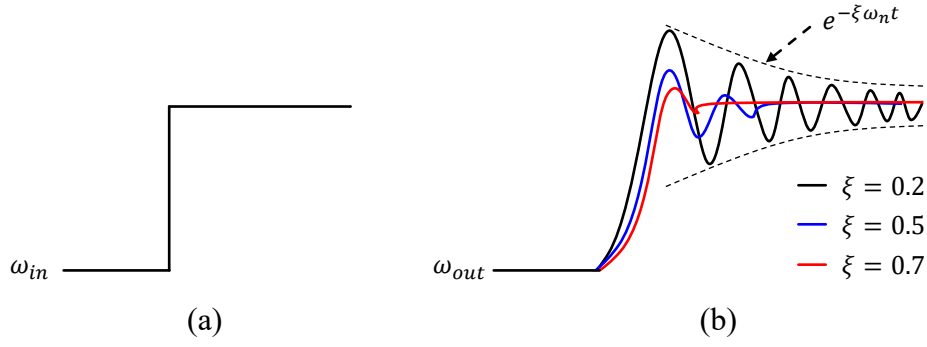


Figure I.2.4 Step response of the underdamped system. (a) Input step signal. (b) Step response with different damping factors.

Some detailed descriptions of type-II PLLs using high-order loop filters, such as their linear models, design considerations and overall noise analysis, can be found in [I-63].

I.2.2.3. Integer-N PLL and Fractional-N PLL

Depending on the type of the frequency divider employed, PLLs can be further classified into the integer-N PLL and the fractional-N PLL, and block diagrams of these two types of PLLs are illustrated in Figure I.2.5.

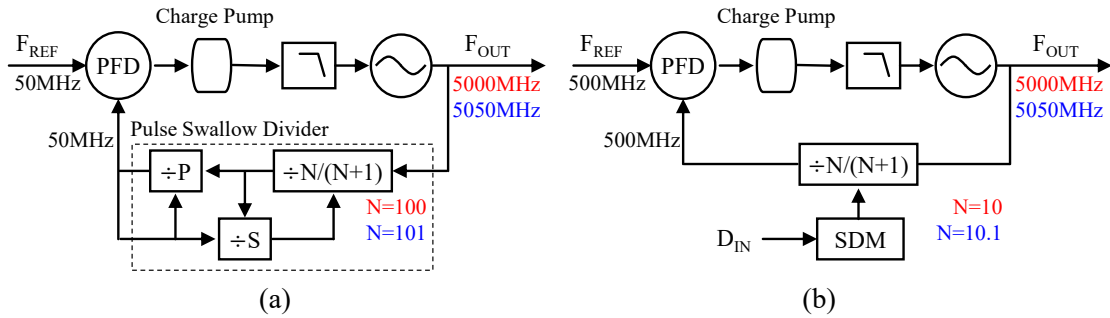


Figure I.2.5 Block diagrams of (a) integer-N PLL with a pulse swallow frequency divider and (b) fractional-N PLL with an SDM.

The output frequency resolution of the integer-N PLL is equal to the reference frequency F_{REF} and is usually chosen to be the same as the channel spacing of the RF transceiver. The PLL in-band (loop filter bandwidth) phase noise is directly affected by the N value, and the phase noise accumulates to the output in a ratio of $20\log(N)$. Therefore, the integer-N PLL is not suitable for narrow loop bandwidth applications with very high N values because of its severe phase noise degradation, long settling times, and sensitivity to power supply and substrate noise. In addition, the frequency divider often adopts a pulse swallow structure as shown in Figure I.2.5(a), which provides a very large

value and continuously programmable frequency division ratio in a simpler structure with low power consumption and is therefore well suited for the RF integer-N PLL.

As shown in [Figure 1.2.5\(b\)](#), the fractional-N PLL permits an output frequency resolution ΔF_{OUT} equal to a fraction of the reference frequency, allowing a higher reference frequency far greater than the desired channel spacing. Therefore, a very low N value and fine frequency resolution can be effectively achieved, resulting in a significant reduction in both in-band phase noise and settling time, and an important improvement in loop dynamics. For example, a fractional-N division ratio of 10.1 can be obtained by dividing the output frequency F_{OUT} by 10 in 9 cycles and by 11 in 1 cycle. Moreover, this fractional division is typically accomplished by performing frequency dithering via a sigma-delta modulator (SDM). Unfortunately, due to the large perturbations generated by this continuous frequency division operation, the PFD and charge pump will constantly attempt to correct for transient phase errors, which in turn produces a large number of spurs at the output, while the modulator is also burdened with heavy computational tasks. In addition, the PLL bandwidth is usually set to less than 10% of the reference frequency to avoid any significant feed-through of the reference source and to maintain loop stability.

1.2.2.4. Limitations of the Analog CPPLL

Remarkably, the analog fractional-N CPPLL is still the dominant architecture for frequency synthesizers in today's RF communications. However, the large area of its analog modules (such as the charge pump, loop filter, and VCO) makes the CPPLL occupy most of the chip area in a frequency synthesizer. In recent years, the performances of the analog CPPLL have been further improved as CMOS processes have entered the deep nanometer node. However, limited by the non-ideal and mismatch properties of analog circuit modules, the chip area of the CPPLL has not been consistently reduced, leading to relatively high chip costs. Furthermore, such an analog-intensive PLL also lacks portability from one process to another, and thus still requires a long design cycle. Meanwhile, the ongoing reduction of CMOS supply voltage further complicates the design of analog modules of the CPPLL, especially voltage-controlled oscillators. For example, the 22 nm FD-SOI process can have supply voltages as low as 0.8 V, but the threshold voltage is about 0.35 V and the tunable voltage range is extremely narrow.

1.2.3. An Overview of All-Digital Phase-Locked Loop

In order to alleviate these bottlenecks encountered by the conventional analog CPPLL,

TI developed the first generation of all-digital phase-locked loop (ADPLL) that could replace the CPPLL in 2003 [I-64], [I-65]. However, restricted by the CMOS process at that time, the main application scenario was around 2.4 GHz wireless communication system. In recent years, mm-Wave ADPLLs have come into the limelight with the popularity of more advanced 45 nm, 28 nm and 22 nm process nodes. A typical example is the previously mentioned 76 – 81 GHz automotive radar. One can be seen that analog PLLs will inevitably be replaced by ADPLLs in certain scenarios in order to maximize the integration benefits of advanced processes.

I.2.3.1. ADPLL Basic Principles

The block diagram of a conventional divider-based ADPLL is depicted in Figure I.2.6. Its loop mainly consists of a time-to-digital converter (TDC), a digital loop filter, a digitally controlled oscillator (DCO) and a digital frequency divider. Compared with the CPPLL in Figure I.2.2, it can be seen that this ADPLL has a very similar topology. However, the analog CPPLL uses mainly analog control signals like current and voltage between the modules, while the ADPLL uses mainly digital signals.

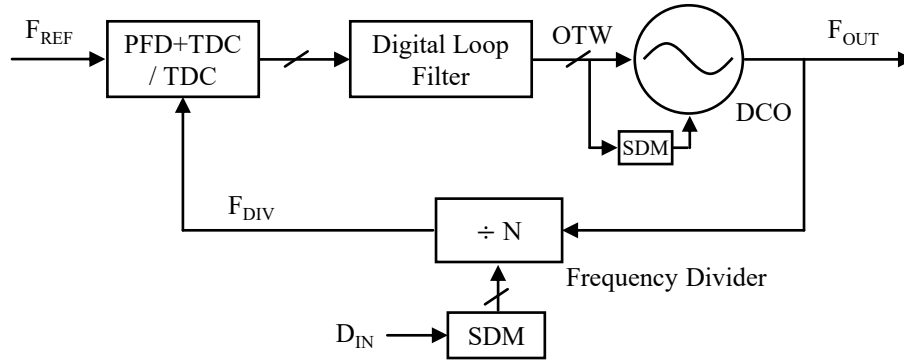


Figure I.2.6 Simplified block diagram of an ADPLL based on frequency divider.

The TDC takes the place of the charge pump and converts the time error (or phase error) between the reference frequency F_{REF} and the divider output frequency F_{DIV} into a digital control signal, which is then fed into the digital loop filter to eliminate high frequency noise. Subsequently, the DCO output frequency F_{OUT} can be changed by this pure digital control signal or the oscillator tuning word (OTW). Furthermore, the SDM dynamically modulates a programmable divider to perform a fractional frequency division. Another SDM is introduced into the DCO to obtain ultra-fine frequency resolution by dithering the least significant bit (LSB) of the DCO control signal. Note that not only the TDC structure is deployed to detect phase errors between F_{REF} and F_{DIV} , but

also the PFD+TDC structure or the Bang-Bang PFD structure. The latter two allow the detection of the phase along with the frequency in order to avoid the system locking on the second harmonic of the output signal.

As illustrated in Figure I.2.7, another common structure of the ADPLL is based on the loop counter [I-66]. The frequency control word (FCW) is actually the dividing ratio of the ADPLL, and the reference phase can be obtained by accumulating FCW. The variable phase is partitioned into an integer part and a fractional part. The integer part is captured by counting the rising edge of the DCO output frequency F_{OUT} . The fractional part is estimated by TDC measuring the time difference between the adjacent rising edges of F_{REF} and F_{OUT} . The difference between the reference phase and the variable phase represents the actual quantization error $\varepsilon(k)$ between F_{REF} and F_{OUT} . This error is then filtered by the digital LPF and converted into the digital control signal that varies the DCO frequency. When the ADPLL is locked, the output frequency F_{OUT} is identical to the reference frequency F_{REF} times FCW.

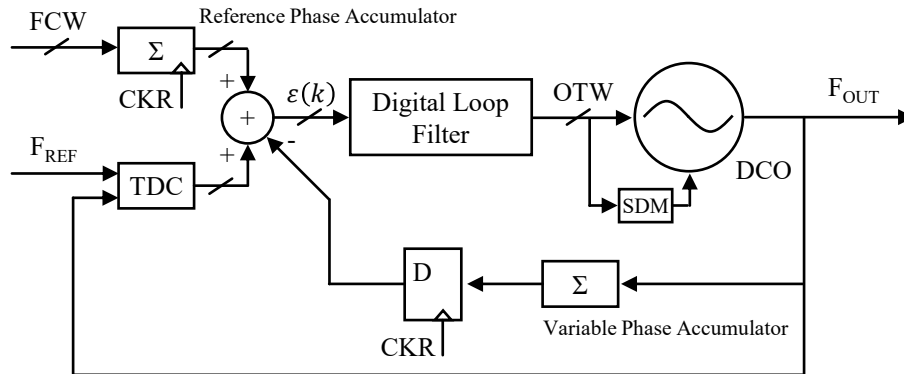


Figure I.2.7 Simplified block diagram of an ADPLL based on loop counter.

Compared to the previous one, this counter-based ADPLL avoids the use of the divider and the wide-range of TDC. Instead, two high-speed counters are used and the resolution can be improved by increasing the number of counter bits. Theoretically, these two architectures are quite similar, except that some modules have different specification requirements. Hereafter we will briefly introduce several core blocks of ADPLL.

I.2.3.2. ADPLL Key Building Blocks

I.2.3.2.1. System Clock Retiming

The clock is very important in digital circuit systems. As shown in Figure I.2.8, the reference frequency F_{REF} and the output frequency F_{OUT} in ADPLL are unsynchronized

clocks, and if these two clocks are compared directly to extract the phase difference, it will inevitably cause sub-stability problems. Therefore, a D flip-flop can be introduced to retime the clocks. The principle is to use the F_{REF} as the input to the D flip-flop, the F_{OUT} as the control clock, and then the output clock CKR can serve as the system clock.

I.2.3.2.2. Time-to-Digital Converter

The CKR frequency generated by the D flip-flop is the same as the F_{REF} frequency, but there is an initial time deviation Δt_d between the rising edge of the F_{OUT} and F_{REF} , and this deviation is part of the phase error. Since we expect the ADPLL to be locked on a stable reference frequency F_{REF} , this deviation must be corrected to meet the requirements of some high-precision systems. The TDC is the one used to measure this deviation. Figure I.2.8 shows that this deviation is less than the clock period of F_{OUT} , so the deviation measured by TDC is also called the fractional phase error, i.e., the fractional part of the variable phase.

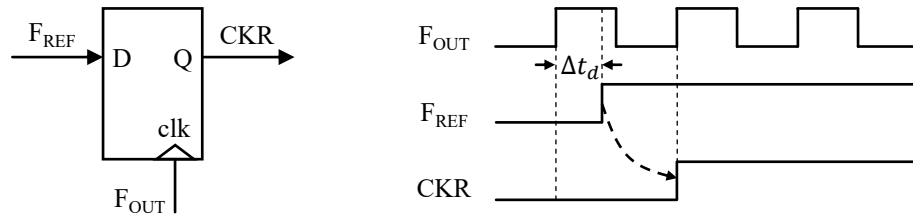


Figure I.2.8 D flip-flop used for system clock retiming.

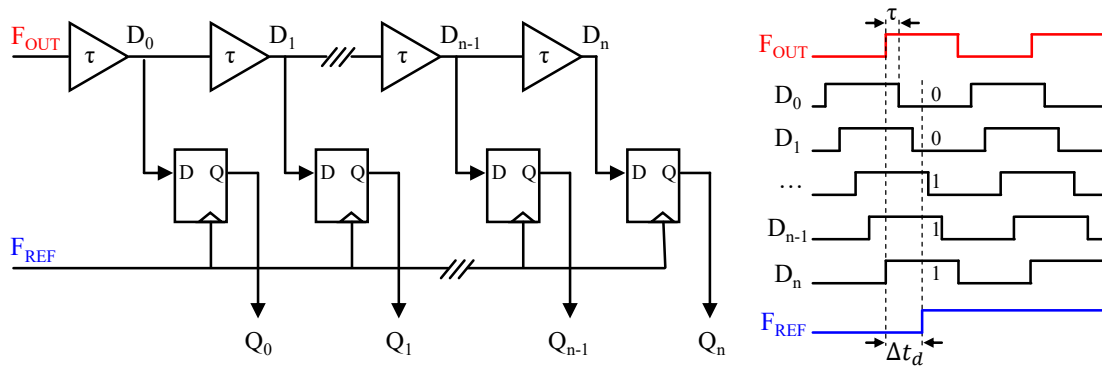


Figure I.2.9 Classical diagram of the TDC based on an inverter chain.

Figure I.2.9 illustrates a classical diagram of the TDC. This TDC is implemented by an inverter chain consisting of basic delay units with a time delay τ , and the D flip-flops sample the output state of each delay unit at the rising edge of the F_{REF} clock to determine the mentioned time deviation Δt_d . The accuracy of such a TDC is the time delay τ of a single delay unit, and a larger dynamic range can be obtained by increasing the number

of delay units. In addition, it is also possible to make the delay chain end-to-end in a loop, so as to obtain a large dynamic range with fewer delay units. Note that the implementation of a high-precision TDC is one of the major difficulties in ADPLL design because the TDC is sensitive to power supply noise [I-67].

I.2.3.2.3. Digital Loop Filter

The primary function of a digital loop filter is to suppress digital high-frequency noise and spurs generated by other blocks in the loop such as TDC, DCO, and SDM, thereby preserving the low-frequency digital control signal. As illustrated [Figure I.2.10](#), a typical digital loop filter generally adopts a proportional-integral (PI) structure, which consists in a proportional circuit with a gain of K_P and an integral circuit with a gain of K_I . The choice of K_P and K_I is crucial for the phase margin and stability of the ADPLL loop [I-68]. Its z-domain transfer function is given by

$$H(z) = K_P + K_I \frac{1}{1 - z^{-1}} \quad (\text{I. 2. 10})$$

Compared with analog RC filters with large capacitors and resistors, digital loop filters can dramatically reduce chip area and power consumption. Moreover, digital loop filters allow dynamic configuration of their type, loop bandwidth (adaptive filtering), etc., which facilitates fast locking and improved loop dynamic performances.

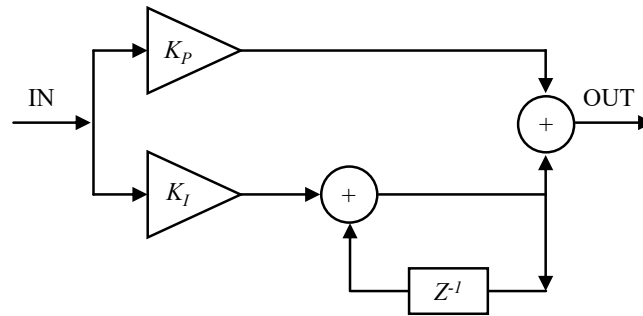


Figure I.2.10 Discrete z-domain transfer function of the PI loop filter.

I.2.3.2.4. Digitally Controlled Oscillator

Unlike VCO, the oscillation frequency of a DCO is controlled by the input binary OTW [I-69]. Since the input signal is digital, it is more immune to interferences. However, the discrete property of the OTW leads to discontinuity in the DCO output frequency, i.e., the frequency resolution of the DCO. Normally, the higher the frequency resolution of the DCO, the lower the quantization noise and the more accurate the ADPLL lock.

The common structures of the DCO are direct digital synthesis (Section I.2.1), ring

oscillator-based DCO, DAC-based DCO and LC-based DCO. Generally, the LC-based DCO has a much higher oscillation frequency and better phase noise performances and is therefore commonly used in mm-Wave ADPLLs. Nevertheless, the LC-based DCO is still essentially an analog circuit due to the presence of inductors and capacitors. However, in terms of overall behavior, the DCO input is a binary OTW and its output frequency is discrete, so the ADPLL using an LC-based DCO is still considered all digital. In addition, it should be noted that achieving a high-performances DCO is another major challenge for ADPLL design as the performances of the ADPLL is highly dependent on the characteristics of the DCO such as phase noise, linearity and resolution. More details on the DCO will be presented in Chapter II.

I.2.3.3. Several Representative Examples of ADPLL

I.2.3.3.1. R. Staszewski et al., 2004 [I-70]

This research work by Dr. Staszewski from TI was published in 2004. The ADPLL with digital direct frequency modulation capability based on a 130 nm CMOS process is proposed for easy integration with a digital baseband and processor.

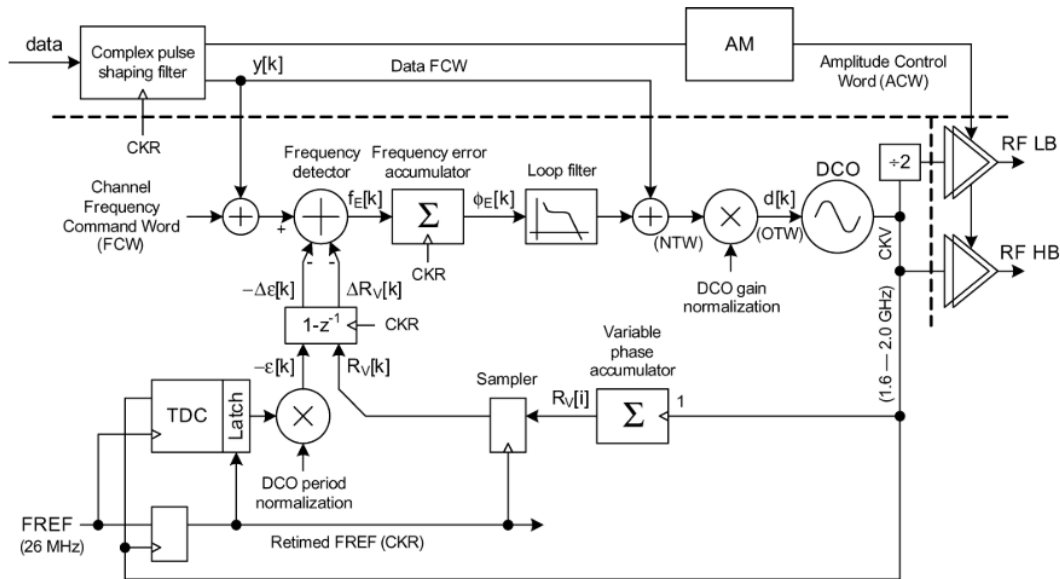


Figure I.2.11 Schematic of the TI's ADPLL-based transmitter system.

As shown in Figure I.2.11, the ADPLL is based on a loop counter structure with wideband frequency modulation capability and built-in automatic compensation to ensure modulation accuracy. The DCO incorporates three capacitor banks with an output frequency of 2.4 GHz and frequency resolutions of 2.3 MHz, 160 kHz and 23 kHz respectively. In addition, the 5-bit fractional tuning word achieves a fine frequency

resolution of 718 Hz ($23 \text{ KHz}/2^5 \approx 718 \text{ Hz}$) through an extra high-speed SDM dithering bank and thus meets the requirements of Bluetooth applications. The DCO achieves a phase noise at 500 kHz frequency offset of -110 dBc/Hz at 2.4 GHz carrier frequency. The TDC adopts the inverter chain structure shown in [Figure I.2.9](#) to obtain a time conversion resolution better than 40 ps at a reference frequency of 13 MHz, and it introduces an in-band noise of -86.3 dBc/Hz at 2.4 GHz carrier frequency.

The ADPLL is revolutionary in its use of an all-digital LC-based DCO. However, there are many areas of improvement, such as long lock time (about 50 μs), unsatisfactory noise performances, low frequency resolution, and capacitor bank mismatch problem in the DCO.

I.2.3.3.2. W. Wu et al., 2014 [I-71]

This research work from Delft University of Technology was published in 2014. As the first reported mm-Wave fractional ADPLL based on 65 nm CMOS process, it provides wideband frequency modulation capability required for FMCW radars.

As shown in [Figure I.2.12](#), the structure of this ADPLL is similar to the previous one. The DCO has three different capacitor banks and employs distributed switched-metal capacitors for frequency tuning to avoid the use of MOS varactors, which suffers from poor Q -factor at 60 GHz. The DCO achieves a wide frequency tuning range of about 10% and a fine frequency resolution of about 1 MHz. The SDM dithering bank operating at 1 GHz can further increase the frequency resolution up to 400 Hz. In addition, the proposed DCO gain linearization scheme is performed to calibrate multiple sets of DCO tuning curves and generate triangular chirps with high linearity. For a 62 GHz carrier frequency with a 1.22 GHz bandwidth, the frequency error (i.e., nonlinearity) measured in the FMCW ramp is as low as 117 kHz rms. The 60 GHz ADPLL achieves in-band phase noise of -75 dBc/Hz, rms jitter of 590.2 fs, and a settling time of 3 μs . The whole ADPLL consumes 48 mW from a 1.2 V supply voltage.

There is no doubt that this ADPLL offers excellent mm-Wave performances. However, from the author's point of view, there are still some minor drawbacks. Firstly, the design and optimization of customized distributed switched-metal capacitors are complicated and susceptible to the process, which goes against the high portability of ADPLLs. Secondly, the algorithm complexity of the gain linearization scheme to calibrate three capacitor banks with different gains is relatively high, particularly at 60

GHz. Finally, considering the PVT variations, for FMCW radars, especially SRRs, the DCO frequency tuning range needs to be around 15 %. This can be simply interpreted as 8 % for the PVT compensation and 7 % for the chirp generation.

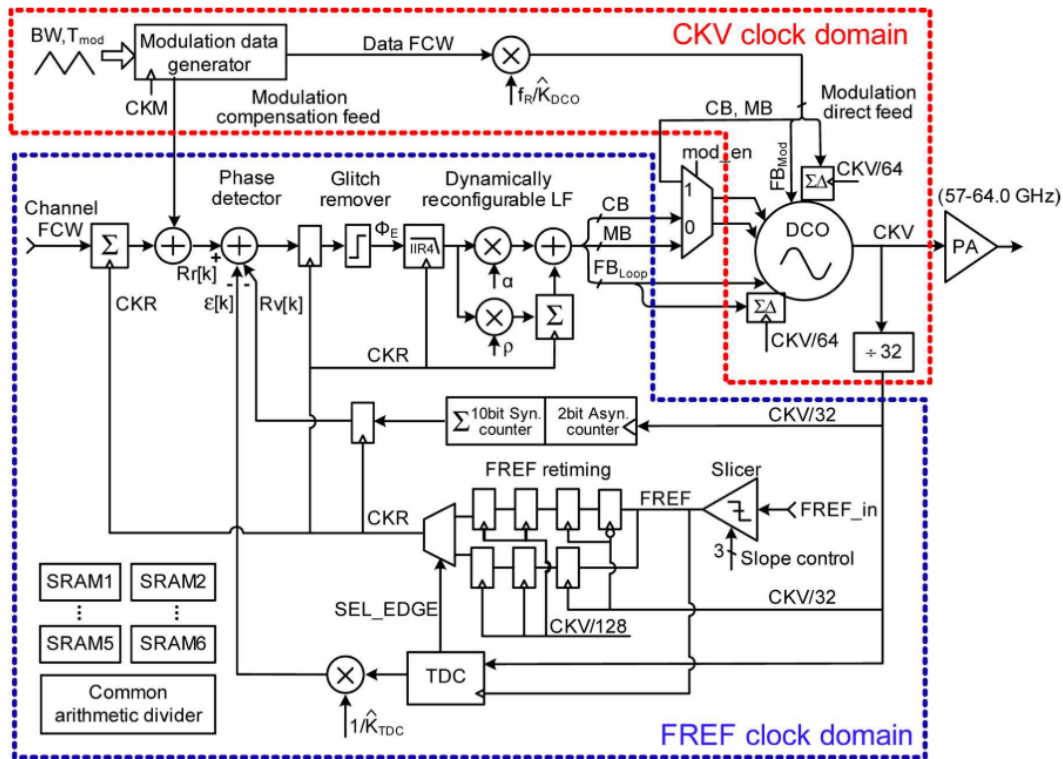


Figure I.2.12 Schematic of the 60 GHz ADPLL-based FMCW transmitter system.

I.2.3.3.3. A. Fridi et al., 2019 [I-72]

This research work from GlobalFoundries was published in 2019. [Figure I.2.13](#) illustrates the proposed divider-based ADPLL, which is primarily used for FMCW automotive radars at 76 - 81 GHz.

The quantization noise cancellation module is introduced before the digital loop filter to suppress the quantization noise generated by the SDM fractional division operation. The TDC is built on a ring oscillator structure and achieves a time conversion resolution of 6 ps. The DCO output frequency is around 20 GHz, and the 76 – 81 GHz band is generated by a frequency multiplier by 4. Since the system loop works around 20 GHz instead of directly at 76 – 81 GHz, the design difficulty and the loop control difficulty are relatively reduced. In addition, the DCO can adopt the conventional switched-capacitor structure and does not require complex electromagnetic simulations.

Note that the DCO has only two capacitor banks for frequency tuning. One coarse-tuning bank is used to compensate for PVT variations and the other fine-tuning bank is

used to cover the 4 GHz FMCW chirp for SRRs. This structure avoids the sophisticated frequency calibration algorithm in a multi-bank DCO. However, considering the trade-off between frequency resolution and frequency tuning range, the fine-tuning bank requiring numerous fine-tuning units leads to a large area and undesirable linearity.

This ADPLL is implemented in an advanced 22 nm FD-SOI process with a power dissipation of 85 mW. It achieves a phase noise of -95 dBc/Hz at 1 MHz frequency offset for chirp rates of less than 50 MHz/ μ s, and -92 dBc/Hz for chirp rates of 100 MHz/ μ s.

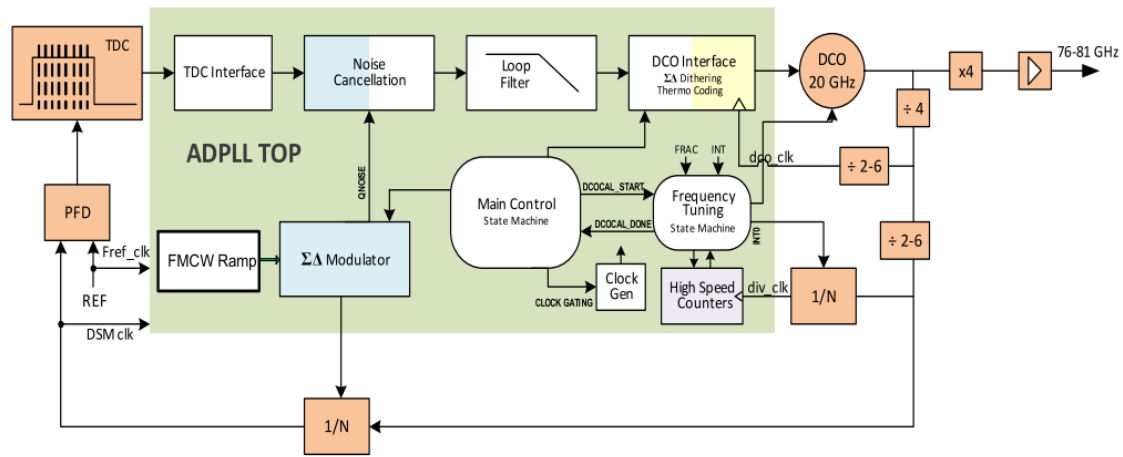


Figure I.2.13 Schematic of the divider-based ADPLL.

I.2.3.4. Advantages of the ADPLL

With more than a decade of development, the ADPLL is competitive or superior to the conventional analog CPPLL in many aspects, such as integration, portability, configurability, stability, and system noise.

- **Integration:** many of the analog modules in the CPPLL are implemented based on passive devices, such as capacitors and resistors in the analog loop filter, resulting in a large area. In the ADPLL, except for the inductors and capacitors of the DCO, which occupy a similar area to the VCO, the other modules have a smaller area, especially the digital loop filter. Thus, the ADPLL allows a very high level of integration.
- **Portability:** most of the modules in the ADPLL are digital circuits, except for customized high-speed circuits such as DCO, TDC and high-speed counters. Therefore, it is easier to migrate the ADPLL from one process to another, and the design cycle is relatively short.
- **Configurability:** the signals in the ADPLL are mainly digital, so it is easy to evaluate them to obtain the loop performance and status, and thus to dynamically configure

some loop parameters. A typical example is the loop filter. Once the analog loop filter based on capacitors and resistors in the CPPLL is determined, it is difficult to change its order and loop bandwidth. However, the digital loop filter in the ADPLL has the flexibility to configure its gain K_P and K_I to further optimize the overall dynamic performance of the loop. In addition, dynamic configuration of the closed-loop response of the CPPLL is extremely challenging, requiring not only monitoring of the VCO transfer function, but also a high-precision DAC to generate the compensation signal, which is why the CPPLL is suitable for narrowband applications. Thanks to the digital signal in the ADPLL, it is much easier to compensate its closed-loop response, such as the commonly used two-point modulation, which not only enables a wideband modulated signal, e.g., more than the loop bandwidth, but also keeps the carrier frequency unshifted.

- Stability: the digital signal in the ADPLL is insensitive to coupling noise from other modules in the transceiver, so the system is more stable.
- System noise: the ADPLL usually includes five noise sources. They are phase noise of the reference signal, quantization noise of the TDC, phase noise and quantization noise of the DCO and quantization noise of the SDM. The CPPLL generally includes six noise sources. They are the phase noise of the reference signal, the thermal noise and flicker noise of the charge pump, the phase noise of the VCO, the quantization noise of the SDM, the thermal noise of the loop filter and the phase noise of the loop divider. The quantization noise of TDC is similar to that of charge pump and is mainly distributed within the loop bandwidth. The phase noise performances of DCO and VCO is basically the same, and the quantization noise of DCO can be reduced to negligible by SDM dithering. The quantization noise of SDM is mainly located at high frequencies outside the loop bandwidth. Moreover, the noise level of the loop filter and divider in the CPPLL is relatively low. Therefore, it can be considered that the noise performances of ADPLL and CPPLL is pretty similar.

Nevertheless, ADPLL will not completely replace CPPLL in the foreseeable future, mainly because of the large fractional spurs in ADPLL, which are caused by the limited accuracy of TDC, making it difficult to meet the requirements of some high-precision systems. In fact, fractional spurs also exist in CPPLL, mainly due to the mismatch, coupling and other mechanisms in the system, but their level is rather low and may be further suppressed by some calibration methods.

I.3. Oscillators

As one of the core modules in a PLL, the performance of the oscillator is critical. This section will briefly review the oscillator fundamentals, especially the LC oscillator. We first analyze the theoretical basis of oscillation through linear feedback systems and negative resistance compensation systems. Then we analyze and compare three different types of oscillators, including ring oscillators, Colpitts oscillators, and differential cross-coupled oscillators. Finally, we present some theories and models of phase noise. All these will contribute to the analysis of DCO performances in the next chapter.

I.3.1. Principles of an Oscillator

The core of an oscillator is a loop with positive feedback at the oscillation frequency and a certain gain to compensate for the energy loss in the feedback path in order to maintain stable oscillations. There are two methods usually used to analyze the oscillator behavior, one is based on a two-terminal linear feedback system, and the other is based on a negative resistance compensation system [I-73]. In the following, we will introduce these two methods.

I.3.1.1. Linear Feedback System

To explain the physical mechanism of oscillations, we can consider the oscillator as a simple linear positive feedback system. As shown in [Figure I.3.1](#), the input and output of this system are $X(j\omega)$ and $Y(j\omega)$, respectively, and the open-loop transfer function is $G(j\omega)F(j\omega)$, then its closed-loop transfer function $H(j\omega)$ can be expressed as

$$H(j\omega) = \frac{Y(j\omega)}{X(j\omega)} = \frac{G(j\omega)}{1 - G(j\omega)F(j\omega)} \quad (\text{I. 3. 1})$$

When $G(j\omega_0)F(j\omega_0) = 1$, the closed-loop gain at angular frequency ω_0 is infinite, which means that any weak noise at ω_0 in the system will be continuously amplified and eventually reach stability and make the system oscillate. Thus, the well-known Barkhausen stability criterion for oscillations is given by

$$|G(j\omega_0)F(j\omega_0)| = 1 \quad (\text{I. 3. 2})$$

$$\angle[G(j\omega_0)F(j\omega_0)] = 2\pi n, n \in \{0, 1, 2, \dots\} \quad (\text{I. 3. 3})$$

That is, in the steady state, the open-loop gain is unity and the total phase shift of the open-loop must be 0° (or a multiple of 360°). In practice, considering the PVT variation

as well as the nonlinearity, the open-loop gain has to be greater than one in the beginning to start up the oscillation.

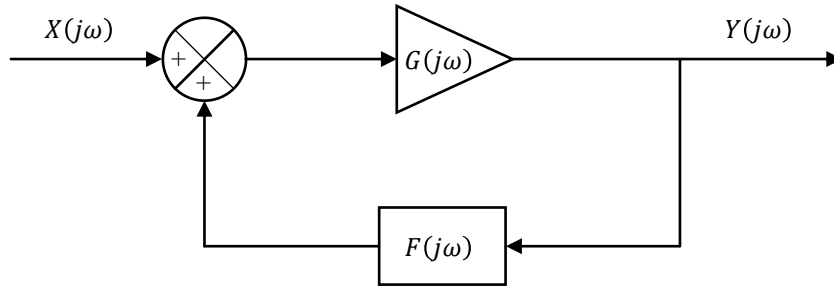


Figure I.3.1 Linear positive feedback system for oscillators.

I.3.1.2. Negative Resistance Compensation System

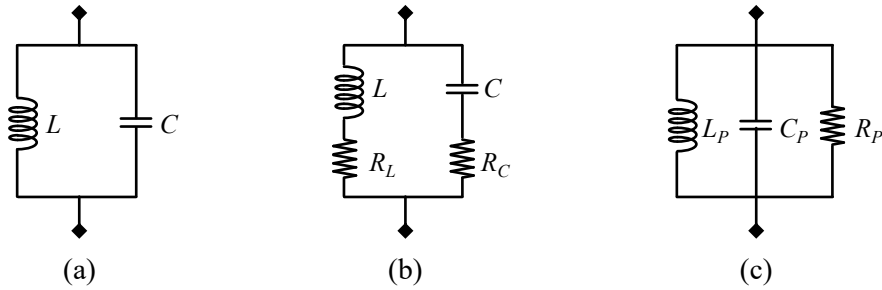


Figure I.3.2 LC resonant circuit. (a) Ideal parallel LC circuit. (b) Practical parallel LC circuit. (c) Equivalent parallel RLC circuit.

As shown in [Figure I.3.2 \(a\)](#), for an ideal LC resonant circuit, at resonant frequency ω_r , the inductive reactance $\omega_r L$ of the inductor and the capacitive reactance $1/(\omega_r C)$ of the capacitor are equal in magnitude and opposite in sign. The LC resonant circuit produces stable oscillation with infinite Q -factor and no energy loss. In practice, both the inductor and capacitor have series resistance as shown in [Figure I.3.2 \(b\)](#), R_L and R_C are the series resistances of the inductor and the capacitor, respectively. Thus, the Q -factor of the inductor is $Q_L = \omega L/R_L$, the Q -factor of the capacitor is $Q_C = 1/(\omega C R_C)$. The Q -factor of this parallel LC circuit can then be written as

$$\frac{1}{Q_{LC}} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (\text{I. 3. 4})$$

In addition, [Figure I.3.2 \(b\)](#) can be equated by the parallel RLC resonant circuit in [Figure I.3.2 \(c\)](#). L_P , C_P and R_P are the parallel equivalent inductance, capacitance and resistance, which can be expressed as

$$L_P = L \left(1 + \frac{1}{Q_L^2} \right) \quad (\text{I. 3. 5})$$

$$C_P = C / \left(1 + \frac{1}{Q_C^2} \right) \quad (\text{I. 3. 6})$$

$$R_P = R_L(1 + Q_L^2) || R_C(1 + Q_C^2) = \frac{1 + Q_L^2 + Q_C^2 + Q_L^2 Q_C^2}{2 + Q_L^2 + Q_C^2} \quad (\text{I. 3. 7})$$

Moreover, at the resonant frequency ω_r , the Q -factor of this parallel RLC resonant circuit can be written as

$$Q_{RLC} = \frac{R_P}{\omega_r L_P} = \omega_r C_P R_P \quad (\text{I. 3. 8})$$

Due to the presence of the lossy R_P , the energy in the resonant circuit drops as it oscillates, and the amplitude decreases until the oscillation stops. In order to maintain stable oscillation, it is necessary to compensate for these losses in the circuit.

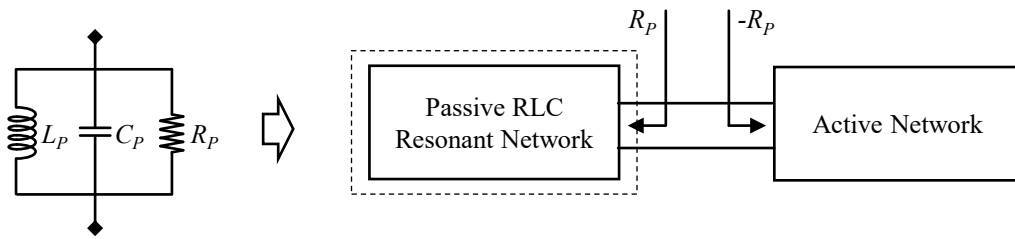


Figure I.3.3 Negative resistance compensation system for oscillators.

As shown in [Figure I.3.3](#), the negative resistance compensation system can be considered as the interconnection of a passive RLC resonant network with an active network. The active network presents a negative resistance $-R_P$, which is used to offset the R_P and keep the parallel resistance of the RLC circuit at zero, thus maintaining stable oscillations. In practical circuits, a negative resistance is usually generated by the active devices, which means that the energy dissipated by R_P is continuously compensated by the active circuit.

I.3.2. Different Types of Oscillators

I.3.2.1. Ring Oscillators

The basic architecture of a ring oscillator is depicted in [Figure I.3.4](#). To satisfy the Barkhausen criterion, it consists of an odd number of inverters connected in series, where

the output of the last inverter is fed back to the input of the first inverter, so that the total phase shift of the loop is an integer multiple of 2π radians. The oscillation frequency of this single ended ring oscillator can thus be expressed as

$$f_{ro} = \frac{1}{NT_d} \quad (I.3.9)$$

where N represents the number of inverters in the inverter chain, T_d represents the time delay for a single inverter. Therefore, the oscillation frequency of the ring oscillator is highly dependent on the number of inverters and the process.

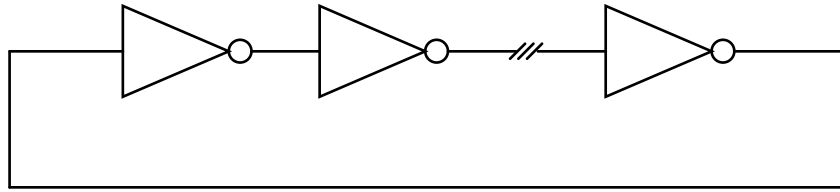


Figure I.3.4 Ring oscillator based on an inverter chain.

The ring oscillator can be implemented entirely based on transistors, avoiding the use of large inductors and leading to a very compact structure and small size. It can also provide multi-phase outputs and a wide tuning range. However, its shortcomings are fatal. When the inverter is charged and discharged, for example, noise from the power supply or the transistor itself is injected into the signal path. Thus, the phase noise performances of ring oscillators are much worse than those of oscillators using LC resonators, which greatly limits their use in low-noise applications. Therefore, we do not describe it in detail here.

I.3.2.2. Colpitts Oscillator

The LC oscillator can be implemented with an LC resonant tank and a single MOS transistor. The LC resonant tank features a purely resistive characteristic at the resonant frequency, i.e., the phase difference is 0. The signals at the source and drain of the MOS transistor also have the same phase. According to the Barkhausen criterion, if the drain signal is fed directly back to the source, then the positive feedback required by the oscillator is obtained.

As shown in [Figure I.3.5 \(a\)](#), the MOS transistor M1 as an active device is used to amplify the output signal of the feedback, and the LC resonant tank (L_P and C_I) performs frequency selection. Another role of the employed capacitor (C_I) is to avoid coupling that affects the bias point of M1. Remarkably, this circuit introduces the source impedance

$1/g_m$ of M1 into the resonant circuit, resulting in its inability to oscillate due to insufficient loop gain. An effective solution is to transform the source impedance to a very high level. The commonly used approaches are to insert an inductive divider or capacitive divider in the feedback path, the so-called Hartley oscillator and Colpitts oscillator.

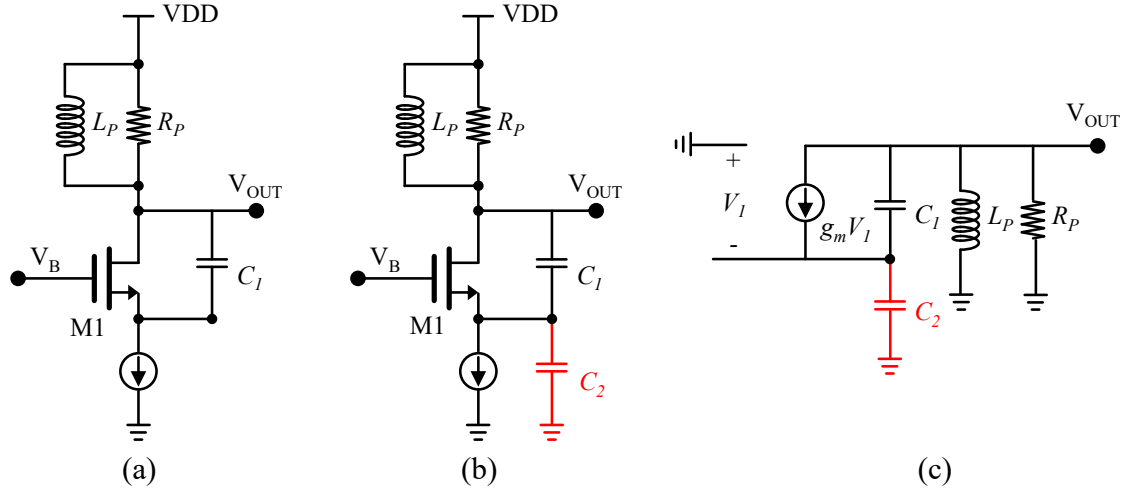


Figure I.3.5 (a) Single MOS transistor with feedback applied from drain to source. (b) Colpitts oscillator. (c) Equivalent small-signal model of the Colpitts oscillator.

The most representative LC oscillator based on a single MOS transistor is the Colpitts oscillator, which can achieve a very high oscillation frequency and good phase noise. Its structure is illustrated in Figure I.3.5 (b), where the two capacitors (C_1 and C_2) together form the capacitive feedback. The oscillation frequency can be expressed as

$$f_{co} = \frac{1}{2\pi \sqrt{L_P \frac{C_1 C_2}{C_1 + C_2}}} \quad (\text{I. 3. 10})$$

The oscillator voltage gain $g_m R_P$ to maintain stable oscillation can be derived as

$$g_m R_P = \frac{C_2}{C_1} \left(1 + \frac{C_1}{C_2} \right)^2 \geq 4 \quad (\text{I. 3. 11})$$

where g_m is the transconductance of M1 and R_P is the equivalent parallel resistance of the resonator. It can be derived that when $C_1 = C_2$, the voltage gain is minimized to 4.

Therefore, a critical drawback of the Colpitts oscillator is that it requires a voltage gain of at least 4. Considering the difficulty of implementing a high Q -factor inductor in CMOS processes, the R_P is generally small, so the Colpitts oscillator requires a high transconductance, leading to an increase in power consumption.

resistance. Neglecting substrate effects and channel modulation effects, the small-signal model of the cross-coupled pair can be simplified as shown in [Figure I.3.6 \(b\)](#). Therefore, the input voltage V_{IN} can be expressed as

$$V_{IN} = V_{GS1} - V_{GS2} \quad (\text{I. 3. 12})$$

The input current I_{IN} is given by

$$I_{IN} = g_m V_{GS2} = -g_m V_{GS1} \quad (\text{I. 3. 13})$$

The negative resistance can be derived by

$$\frac{V_{IN}}{I_{IN}} = \frac{V_{GS1}}{I_{IN}} - \frac{V_{GS2}}{I_{IN}} = -\frac{1}{g_m} - \frac{1}{g_m} = -\frac{2}{g_m} \quad (\text{I. 3. 14})$$

In addition, the equivalent parallel impedance of the combined LC resonant circuit is $2R_P$, the absolute value of the negative resistance generated by the cross-coupled pair needs to be no greater than $2R_P$, which can be expressed as

$$\frac{2}{g_m} \leq 2R_P \quad (\text{I. 3. 15})$$

Thus, we have

$$g_m R_P \geq 1 \quad (\text{I. 3. 16})$$

That is, when $g_m \geq 1/R_P$, the energy dissipated by R_P can be continuously compensated by the active cross-coupled pair and the oscillator starts to oscillate.

The cross-coupled oscillator offers a number of advantages. Firstly, compared to the Colpitts oscillator it can be seen that the cross-coupled oscillator no longer requires a very high MOS transistor transconductance. Secondly, this simple differential structure facilitates the elimination of common-mode noise. Moreover, the cross-coupled oscillator is capable of operating at low supply voltages, such as 0.8 V, which makes it very suitable for some low-power scenarios. Finally, the cross-coupled oscillator allows for large voltage swings, resulting in excellent phase noise.

Reviewing the literature, one can learn that there are many different topologies of the cross-coupled oscillator, and new structures are emerging all the time. To simplify the analysis, three commonly used structures will be highlighted and discussed, which are NMOS-only structure, PMOS-only structure, and complementary structure.

I.3.2.3.1. NMOS-Only Structure with Tail Current Source

As illustrated in Figure I.3.7 (a), the NMOS-only structure with a tail current source is the most classic and commonly adopted LC oscillator structure. Since the electron mobility is much higher than that of holes, under the same size, the transconductance that the NMOS transistor can provide is about twice larger than that of the PMOS transistor, but the price is that the flicker noise of the NMOS transistor is higher.

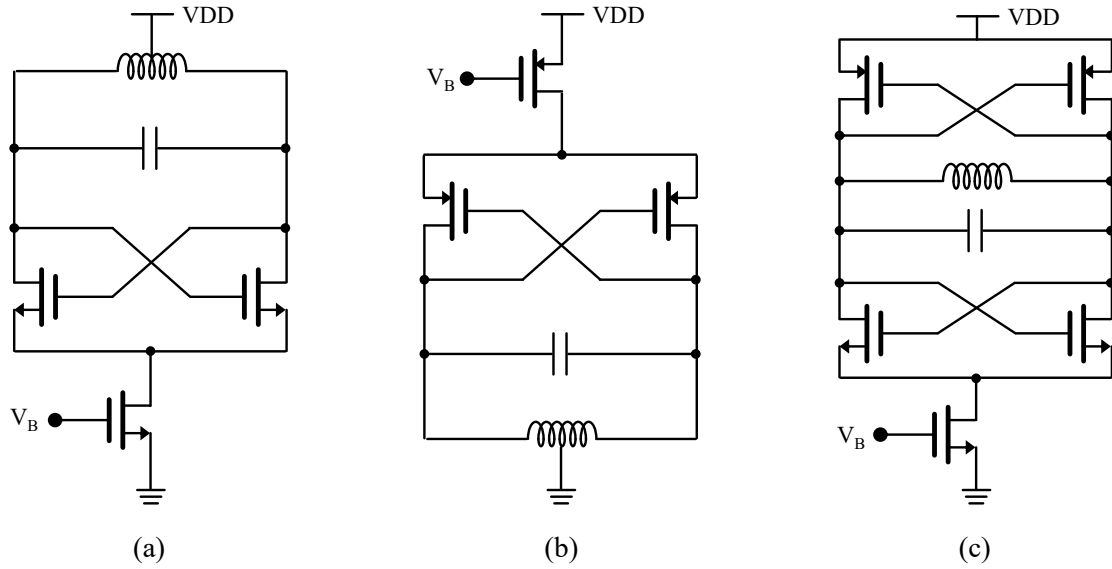


Figure I.3.7 Cross-coupled oscillators with a tail/top current source. (a) NMOS-only structure. (b) PMOS-only structure. (c) Complementary structure.

Therefore, compared to the PMOS-only structure, for the same transconductance and the same bias current, the NMOS-only cross-coupled pair has a smaller size, i.e., less parasitic capacitance. Alternatively, for the same transconductance and the same cross-coupled pair size, the NMOS-only cross-coupled oscillator features a lower power consumption.

Note that the tail current source plays a very critical role in controlling power dissipation and phase noise. By providing a stable bias current for the cross-coupled pair, the tail current source can speed up the switching of the differential pair, as well as reduce the oscillator's sensitivity to changes in supply voltage and optimize phase noise by manipulating the output voltage swing. This is why many cross-coupled oscillators incorporate a tail current source, even though the tail current itself can introduce noise.

The NMOS-only cross-coupled oscillator can also provide an output voltage swing in excess of the supply voltage, making it suitable for low supply voltage scenarios.

However, considering the hot-carrier injection (HCI) effect, excessive voltage swing can reduce the lifetime of the cross-coupled pair, which needs to be taken into account in the design.

Moreover, the cross-coupled oscillator can also be biased by a top current source. The high output impedance of the top current source suppresses the effect of supply voltage variations on the resonant LC tank. However, the top current source itself will continuously inject noise, which in turn leads to a poor phase noise performance.

I.3.2.3.2. PMOS-Only Structure with Top Current Source

Compared to the former, the PMOS-only cross-coupled oscillator leads to higher power consumption and larger parasitic capacitances. However, it has better phase noise performances due to the lower flicker noise and thermal noise (larger size) of the PMOS transistors than that of the NMOS ones. In addition, the high output impedance of the top current source isolates the supply voltage from the resonant LC tank, further enhancing the phase noise performances.

I.3.2.3.3. Complementary Structure with Tail Current Source

This complementary structure combines NMOS transistors and PMOS transistors to provide the negative resistance required for the resonant LC tank. One of its distinct advantages is low power consumption. For the same bias current, it has twice the output voltage swing of the NMOS-only or PMOS-only structure. Furthermore, the rising and falling times of its output waveform are more symmetrical, which contributes to the reduction of flicker noise and thus improves phase noise performances. Therefore, the complementary structure is well suited for low-power, low-phase noise applications.

However, it also suffers from some significant drawbacks. Firstly, the introduction of an extra transistor between power and ground makes the implementation of this structure difficult considering the low supply voltage of 0.8 V and the threshold voltage of about 0.35 V for advanced processes. Although this issue can be addressed by removing the tail current source, this would require a high-performance low-dropout regulator (LDO) to stabilize the supply voltage and would also lead to an increase in power consumption. Secondly, the maximum voltage swing allowed by the complementary cross-coupled oscillator is small, which is not favorable for further phase noise improvement. Therefore, without considering the power consumption, the optimal phase noise achievable by this complementary structure is significantly worse than the previous two structures. Finally,

this structure introduces a large parasitic capacitance, which ultimately leads to a reduction in the output frequency and frequency tuning range of the oscillator.

I.3.3. Phase Noise Analysis of the Oscillators

Phase noise is one of the most important indicators of how good an oscillator is and how it affects the sensitivity of an RF transceiver. The noise sources of the LC oscillator can be classified into two main categories: internal noise and external interference noise. The former includes thermal noise, flicker noise, etc. The latter includes supply voltage noise as well as substrate coupling noise, etc. This section will therefore focus on the main sources of phase noise, its definition and the classical phase noise model.

I.3.3.1. Noise Sources

I.3.3.1.1. Thermal Noise

Due to thermal excitation, random displacement of the charge carriers forms a varying current, thereby causing a random voltage across the resistive element, which is the origin of thermal noise. Thus, thermal noise exists in the vast majority of electronic devices at temperatures above absolute zero, for example, non-ideal capacitors and inductors can also generate thermal noise due to the presence of series resistance. The thermal noise of a resistor can be modeled by a series noise voltage source $\overline{V_n^2}$. Its one-sided spectral density is given by

$$S_v(f) = \frac{\overline{V_n^2}}{\Delta f} = 4kTR \quad (\text{I. 3. 17})$$

where k is the Boltzmann constant ($k = 1.38 \times 10^{-23}$ J/K), T is the absolute temperature, R is the resistance, Δf is the bandwidth around the frequency f . In addition, the channel resistance of MOS transistors also produces thermal noise, which can be modeled by a noise current source I_n^2 connected between the drain and source terminals whose spectral density can be expressed as

$$S_i(f) = \frac{\overline{I_n^2}}{\Delta f} = \frac{2}{3} \cdot 4kTg_m \quad (\text{I. 3. 18})$$

where g_m is the transconductance of the MOS transistor and the factor $2/3$ is only applicable to long-channel devices. For short-channel devices, the thermal noise becomes much greater as the strong electric field makes the charge heated.

I.3.3.1.2. Shot Noise

The shot noise is mainly found in active non-linear devices with DC currents. The carriers need to have sufficient energy and speed to cross the potential barrier, and each carrier crossing the barrier can be seen as a random event, i.e., an independent small current pulse. The fluctuations in the current caused by these current pulses can be described in terms of shot noise. The spectral density is given by

$$S_i(f) = \frac{\overline{I_n^2}}{\Delta f} = 2qI \quad (\text{I. 3. 19})$$

where q is the amount of charge, I is the DC current. Since the carriers cross the potential barrier at random times, the shot noise is frequency independent and is also a white noise.

I.3.3.1.3. Flicker Noise

The flicker noise is mainly caused by lattice defects at the interface between single-crystal silicon and its oxide during the fabrication of MOS transistors. Flicker noise is also known as $1/f$ noise, and its spectral density can be expressed as

$$S_i(f) = \frac{\overline{I_n^2}}{\Delta f} = \frac{\gamma h}{f^\alpha N} I^2 \quad (\text{I. 3. 20})$$

where γh is the global Hooge coefficient, α is an empirical coefficient, N is the number of carriers, and I is the DC current.

I.3.3.2. Definition of the Phase Noise

In the ideal case, i.e., without noise, the output of the oscillator is a single frequency sine wave, which can be expressed as

$$V_{OUT}(t) = A \cos(\omega_0 t + \phi) \quad (\text{I. 3. 21})$$

where A is the amplitude, ω_0 is the angular frequency, and ϕ is the phase. It can be seen that the amplitude and phase of the oscillator are fixed. As shown in [Figure I.3.8 \(a\)](#), its power spectral density is a pulse (blue arrow) at the angular frequency ω_0 .

However, the active and passive devices that make up the oscillator inevitably introduce some noise, such as the previously mentioned thermal noise, shot noise and flicker noise. In practice, these noises constantly disturb the phase and amplitude of the oscillator output signal, causing its power spectral density to extend from ω_0 to both sides, and thus two sidebands appear as shown in the gray area in [Figure I.3.8 \(b\)](#). The actual output waveform can thus be represented as

$$V_{OUT}(t) = A(t) \cos(\omega_0 t + \phi(t)) \quad (I.3.22)$$

where both amplitude $A(t)$ and phase $\phi(t)$ are functions of time t . Therefore, the noise of the oscillator is mainly manifested as amplitude noise and phase noise. Normally, the amplitude noise is attenuated by the amplitude limiting circuit or nonlinear circuit and does not have a significant impact on the circuit performances. However, the phase noise cannot be eliminated and needs to be carefully considered in the oscillator design.

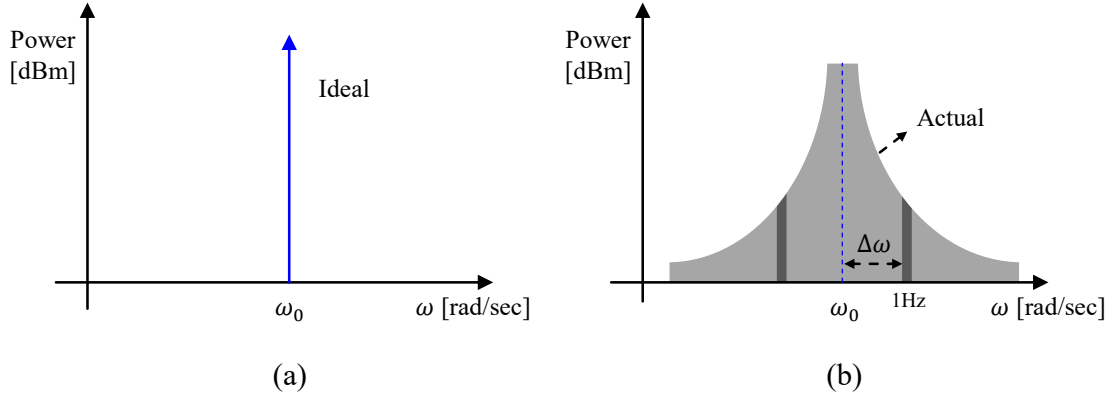


Figure I.3.8 (a) Ideal power spectral density of oscillators. (b) Actual power spectral density of oscillators.

The phase noise of the oscillator is usually expressed as the ratio of the single sideband noise power per unit bandwidth (1Hz) at a certain offset angular frequency $\Delta\omega$ deviating from the carrier ω_0 to the carrier power, which can be denoted as

$$L\{\Delta\omega\} = 10 \log \left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1\text{Hz})}{P_{carrier}} \right] \quad (I.3.23)$$

where $\Delta\omega$ is the offset angular frequency, $P_{sideband}(\omega_0 + \Delta\omega, 1\text{Hz})$ is the single sideband power per unit bandwidth at the offset angular frequency $\Delta\omega$, and $P_{carrier}$ is the total carrier power. The unit of phase noise is dBc/Hz, where dBc refers to the ratio of the two powers (dB).

I.3.3.3. Phase Noise Models

For decades, a lot of research works have been carried out to understand the physical mechanisms of phase noise and to develop mathematical models to predict the phase noise performances of oscillators [I-74]-[I-79]. Here, we will focus on the following two typical phase noise models: linear time-invariant model and linear time-variant model.

I.3.3.3.1. Linear Time-Invariant Model

Leeson proposed a well-known phase noise model based on the linear time-invariant assumption for oscillators in 1966, which was the first model widely used for phase noise analysis, partly due to its simplicity. The corresponding empirical formula derived from Leeson's model is given by [I-75]

$$L\{\Delta\omega\} = 10 \log \left\{ \frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega} \right)^2 \right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right\} \quad (\text{I.3.24})$$

where F is the noise factor, k is the Boltzmann constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the resonator, ω_0 is the carrier angular frequency, Q_L is the loaded quality factor of the resonator, $\Delta\omega$ is the offset angular frequency from the carrier, and $\Delta\omega_{1/f^3}$ is the corner frequency between the $1/f^3$ region and the $1/f^2$ region.

It can be concluded that a low phase noise can be achieved by increasing the power dissipated in the resistive part of the resonator or by improving the quality factor of the LC resonator. Furthermore, the phase noise of the oscillator can be partitioned into three different regions, as shown in Figure I.3.9.

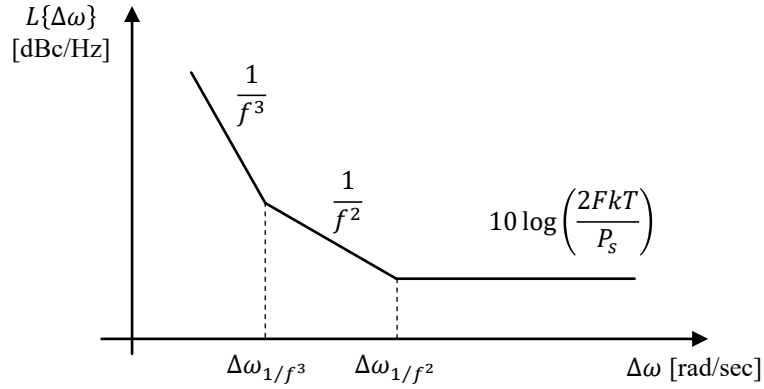


Figure I.3.9 Typical characteristic curve of oscillators' phase noise

- When the frequency offset is less than $\Delta\omega_{1/f^3}$, the phase noise rolls off at a rate of $1/f^3$, i.e., the slope of the phase noise curve is 30 dB/decade, so this region is called the $1/f^3$ region. In this region, the flicker noise plays a dominant role.
- When the frequency offset is between $\Delta\omega_{1/f^3}$ and $\Delta\omega_{1/f^2}$, the slope of the phase noise curve becomes 20 dB/decade, which corresponds to the $1/f^2$ region. In this region, the thermal noise plays a dominant role.

- When the frequency offset is greater than $\Delta\omega_1/f^2$, the phase noise is approximated as $10 \log \left(\frac{2FkT}{P_s} \right)$, which is independent of frequency. Moreover, the frequency offset $\Delta\omega_1/f^2$ is close to $\omega_0/2 Q_L$.

However, because the oscillator itself is a nonlinear circuit, there are some shortcomings in the analysis with a linear time-invariant model. For example, experimental data are required to obtain the noise factor F , and corner frequency $\Delta\omega_1/f^3$ cannot be directly determined, thereby leading to inaccurate prediction of the phase noise performances of the oscillators. In addition, $\Delta\omega_1/f^3$ is considered to be the same as the corner frequency of the MOS transistor' flicker noise, which does not match well with the actual measurement results.

In response to these shortcomings of the Leeson's model, several more refined models have been proposed, among which the Rael's model takes into account the contributions of the LC resonant tank, cross-coupled pair and bias current source to the phase noise, which is more instructive for our design. The formula is given by

$$L\{\Delta\omega\} = 10 \log \left[\frac{2F(\Delta f)kT}{P_s} \left(\frac{\omega_0}{2Q_L\Delta\omega} \right)^2 \right] \quad (I.3.25)$$

It can be observed that this phase noise model is identical to the Leeson's model in the $1/f^2$ region, but the factor $F(\Delta f)$ is determined by [I-80]

$$F(\Delta f) = 1 + \frac{2\gamma I_{bias} R_P}{\pi A} + \frac{4}{9} \gamma g_{m,bias} R_P \quad (I.3.26)$$

where γ is the MOS transistor channel current noise factor, A is the amplitude of the output signal, I_{bias} is the bias current, $g_{m,bias}$ is the transconductance of the tail MOS transistor. The first term represents the thermal noise contribution of the LC resonator tank, the second term represents the noise contribution of the differential cross-coupled pair, and the third term represents the noise from the tail current source.

As we know, in the case of small voltage swing, the output amplitude A can be expressed as $A = (2I_{bias} R_P)/\pi$, where the second term is approximately equal to a constant γ . As the bias current I_{bias} increase, both the power consumption P_s and the output voltage swing increase, so that the on-time of the cross-coupled pair decreases, i.e., the time of noise injection also decreases, which eventually manifests as a phase noise improvement. This region where the phase noise is boosted as the bias current increases

is known as the current-limited region. Beyond the current-limited region, the voltage swing does not change as the bias current continues to increase, and the phase noise enters a relatively stable state, although the power consumption continues to increase, and this region is known as the voltage-limited region. It can be concluded that the best phase noise performances can be obtained in the transition region from the current-limited region to the voltage-limited region.

To better understand the noise contribution of the tail current source, we can consider the differential cross-coupled pair as a mixer, and then the noise signal of the tail current source is mixed with the carrier signal into the resonant tank. Since the mixer exhibits the maximum conversion gain at the fundamental frequency ω_0 , the low-frequency flicker noise from the tail current source can be up-converted around ω_0 . Similarly, the high-frequency thermal noise near $2\omega_0$ can be down-converted near ω_0 . The latter can be attenuated by adding an LC resonator with a frequency around $2\omega_0$.

I.3.3.3.2. Linear Time-Variant Model

The time-invariant model assumes that the noise has the same effect on the result of the oscillator output at any moment, which is apparently not rigorous enough. Based on this fact, a linear time-variant model has been proposed by Hajimiri et al., [I-77].

For each noise source, the system can be considered as a single-input, single-output system, so the time-domain impulse response of the amplitude $A(t)$ and phase $\phi(t)$ of the oscillator can be characterized as shown in [Figure I.3.10](#). Thus, the effect on the oscillation waveform when the current impulse $i(t)$ is injected into the LC resonant tank can be represented in [Figure I.3.11](#), and the instantaneous voltage change ΔV is given by $\Delta V = \Delta q / C_{tot}$, where Δq is the total injected charge by the current impulse and C_{tot} is the total capacitance at the node considered. Obviously, the current impulse will change only the instantaneous voltage across the capacitor and will not affect the instantaneous current through the inductor.

As shown in [Figure I.3.11 \(a\)](#), when the current impulse is injected at the peak of the capacitor voltage, it will only change the amplitude of the oscillator. Because of the nonlinear limiting mechanism in the oscillator, the oscillation amplitude is able to return to a steady state after a period of time. [Figure I.3.11 \(b\)](#) shows that when the current impulse is injected at the zero-crossing point, the current impulse will only change the phase of the oscillator. When the current impulse is added at any other time, it will change

both the amplitude and the phase of the oscillator. Since the phase change cannot be eliminated, the effect of noise source on phase shift is usually of interest.

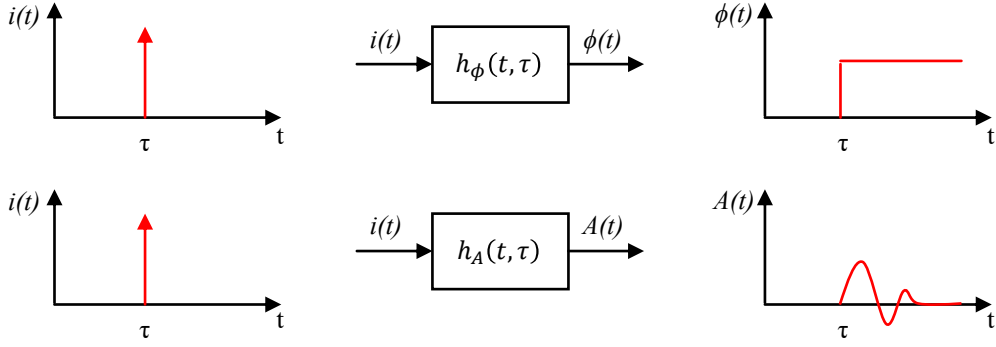


Figure I.3.10 Phase and amplitude impulse response model

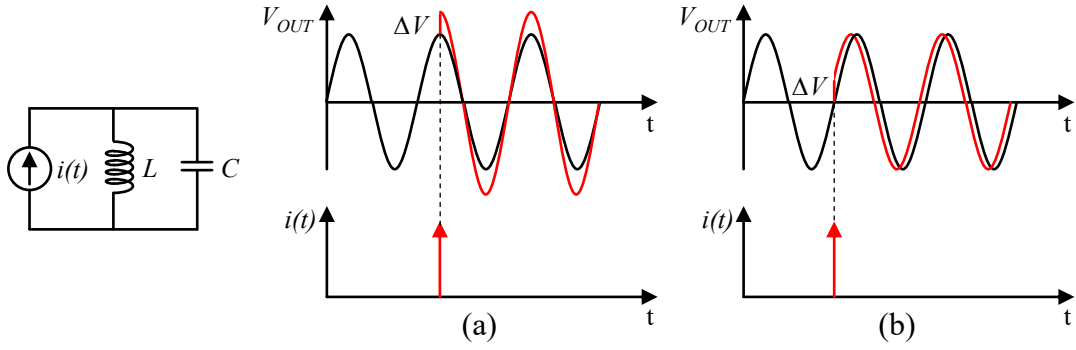


Figure I.3.11 (a) Noise impulse injected at the peak. (b) Noise impulse injected at the zero-crossing point.

Based on the above phenomenon, an impulse sensitivity function (ISF) is introduced in the Hajimiri model, which is a periodic function independent of frequency and amplitude, and it contains the amount of phase shift resulting from applying a unit impulse. For the oscillator, it is known from the above analysis that the ISF reaches its maximum value at the zero-crossing point of the oscillation signal, while the ISF is 0 at the peak of the oscillation signal. The mathematical model of the phase noise given by Hajimiri is

$$L\{\Delta\omega\} = 10 \log \left(\frac{\frac{\overline{i_n^2}}{\Delta f} \sum_{n=0}^{\infty} c_n^2}{4q_{max}^2 \Delta\omega^2} \right) \quad (I.3.27)$$

where $\overline{i_n^2}/\Delta f$ represents the power spectral density of the white noise considered, c_n is the Fourier coefficient of the ISF function, q_{max} is the maximum charge swing across the capacitor on the node, and $\Delta\omega$ is the offset angular frequency. This formula indicates that

the noise located near an integer multiple of the oscillator frequency is shifted to the vicinity of the carrier frequency through the up-conversion or down-conversion process. As shown in Figure I.3.12, the noise in the $1/f^3$ region is mainly the low-frequency flicker noise of the MOS transistor weighted by the coefficient c_0 . The noise in the $1/f^2$ region is the sum of the white noise on higher harmonics weighted by coefficients c_n , and the white noise region is the white noise of the oscillator itself.

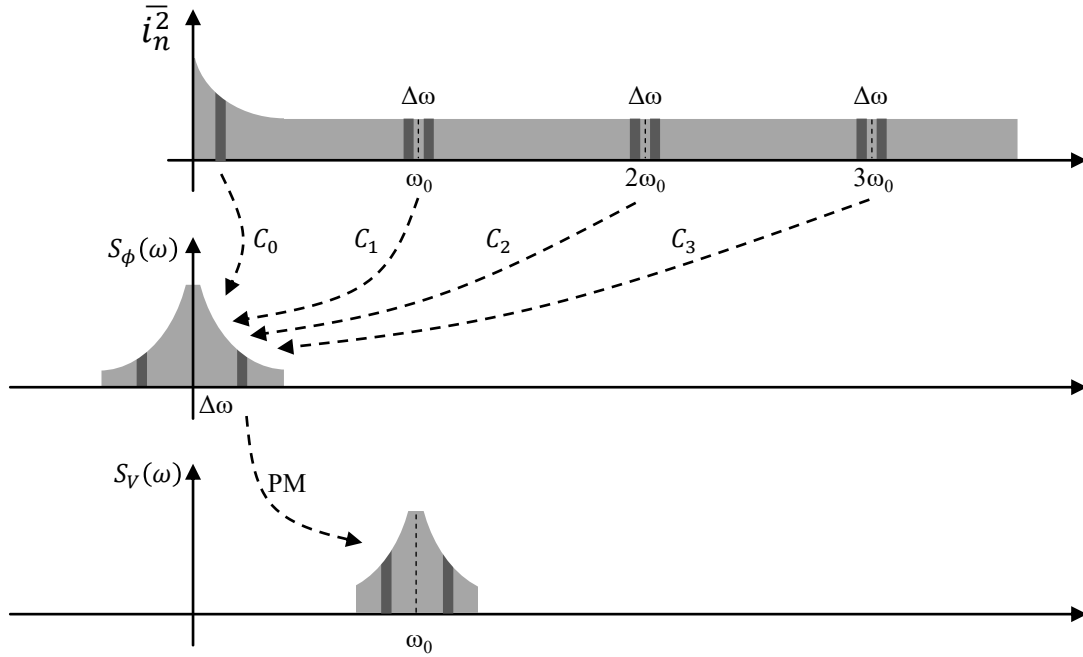


Figure I.3.12 Conversion of noise to phase fluctuations and phase noise sidebands.

It can be concluded that Hajimiri's time-variant model not only elaborates the contribution of each noise sources in the oscillator to the overall phase noise, but also provides a relatively accurate method for calculating the phase noise, although solving the ISF function for each noise source is complex. In general, benefiting from this model, we can reduce the effect of some specific noise sources at the beginning of the design.

I.4. Conclusion

The purpose of our research project is to design a high-performance K-band DCO, which is one of the core modules of an ADPLL used in a 76 – 81 GHz FMCW automotive radar. Therefore, in this chapter, we introduced the research background in three main aspects: the automotive radars, the frequency synthesizer and the oscillator.

In Section I.1, we began with the introduction of radar fundamentals, i.e., radar-frequency bands, radar types, radar equations, and commonly used transceiver architectures. Then, we reviewed the autonomous driving technology, including the level of autonomy, the ADAS system, the development and classification of automotive radars. Moreover, typical processes applied to automotive radars and related academic and commercial works were also discussed.

In Section I.2, we first reviewed several common frequency synthesis techniques. Next, we introduced two basic structures of the analog PLL (integer-N type and fractional-N type), and then analyzed some key loop characteristics through its transfer functions. Finally, we presented some core modules and two widely used structures of the ADPLL (loop divider-based structure and loop counter-based structure) and summarized its advantages and disadvantages. It can be concluded that the ADPLL features great advantages in terms of integration, power consumption, and low supply voltage, which certainly cannot be achieved without a high-performance DCO.

In Section I.3, we first reviewed the basic principles of oscillators, including the linear feedback system and the negative resistance compensation system applied to the determination of start-up conditions. Secondly, we compared three popular structures of oscillators, which are ring oscillators, Colpitts oscillators and differential LC cross-coupled oscillators. The latter is also the structure that will be used in our high-performance DCOs. Finally, we presented some critical noise sources in electronic devices and exposed the phase noise performances of oscillators by the classical Leeson's model and Hajimiri's model, and these theories are also applicable to the phase noise analysis of DCOs.

I.5. Résumé du Chapitre I

Le Chapitre I présente le contexte des travaux de recherche et traite des radars automobiles, des techniques de synthèse de fréquence et des oscillateurs, qui constituent la base théorique des Oscillateurs à Commande Numérique (OCN) dont l'analyse et la conception sont proposés dans ce mémoire.

Dans la Section I.1, nous avons d'abord étudié les principes de base du radar, lequel permet la détection d'une cible (distance, vitesse, caractéristiques, etc.) en émettant des

ondes électromagnétiques vers celle-ci et en recevant le signal de l'écho. Par conséquent, les caractéristiques des ondes électromagnétiques utilisées, principalement la bande de fréquence, déterminent les performances et les applications du radar. La relation entre les principaux paramètres du radar (puissance d'émission, gain d'antenne, etc.), la portée détectée et les caractéristiques de la cible peuvent être décrites quantitativement par l'équation du radar. En outre, il existe différents types de radars, mais, quelle que soit la catégorie de radar étudié, celui-ci est inévitablement constitué d'un système émetteur-récepteur, servant de lien entre le processeur de traitement de signal numérique et l'antenne. Les émetteurs basés sur la boucle à verrouillage de phase (PLL en anglais) sont souvent utilisés dans les radars à ondes continues modulées en fréquence (FMCW en anglais) pour obtenir un chirp linéaire. Les structures hétérodynes et superhétérodynes classiques sont également couramment utilisées dans les systèmes émetteurs-récepteurs et il est utile de préciser que l'Oscillateur Contrôlé en Tension (OCT) joue un rôle primordial dans ces dispositifs. Par ailleurs, le développement de technologies de conduite autonome dépend fortement des capteurs, en particulier dans les véhicules autonomes de niveau trois et supérieur, dont le plus représentatif est le radar automobile. Les bandes de fréquences actuellement les plus utilisées pour les radars automobiles sont la bande étroite de 76 à 77 GHz et la bande ultra-large de 77 à 81 GHz, lesquelles conviennent respectivement aux radars à longue portée avec une distance de détection d'environ 250 mètres et aux radars à courte portée avec une distance de détection inférieure à 30 mètres. Le développement de technologies de radars pour des applications automobiles à ondes millimétriques a traversé trois phases principales. Initialement, il était dominé par les semi-conducteurs composés III-V, surtout l'arséniure de gallium (GaAs), mais avec une faible intégration et un coût élevé. Les alliages silicium-germanium (SiGe) sont ensuite devenus populaires car ils sont hautement compatibles avec les process silicium matures et présentent non seulement les avantages des process silicium en termes d'intégration et de coût, mais aussi les avantages du GaAs en termes de réponse en fréquence. Ces dernières années, grâce à la maturation progressive des process CMOS à l'échelle nanométrique, en particulier le process FD-SOI (Fully Depleted Silicon-On-Insulator en anglais), il est ainsi devenu possible de mettre en œuvre un radar automobile à ondes millimétriques entièrement intégré en technologie CMOS, ce qui a suscité une grande attention de la part du milieu universitaire et de l'industrie.

Dans la Section I.2, nous avons présenté trois techniques de synthèse de fréquence

couramment utilisées, notamment la synthèse de fréquence analogique directe, la synthèse de fréquence numérique directe et la boucle à verrouillage de phase. Elles peuvent toutes être utilisées afin de délivrer un signal stable avec une pureté spectrale élevée. Cependant, pour les applications supérieures à 10 GHz, la PLL est préférée en raison de fréquence élevée du signal de sortie et de son faible bruit de phase, etc. Actuellement, les PLLs analogiques sont encore les plus courantes dans les applications industrielles, bien que les boucles à verrouillage de phase entièrement numérique (ADPLL en anglais) les remplacent progressivement dans certains domaines en raison de leurs avantages en matière d'intégration, de reconfigurabilité et de stabilité. Les modules de base d'une ADPLL sont presque tous implémentés en utilisant des circuits numériques, tels que le TDC (Time-to-Digital Converter en anglais), le filtre numérique de boucle, le diviseur de fréquence. L'OCN est, quant à lui, un circuit à signaux mixtes. Néanmoins, comme son entrée et sa sortie peuvent être représentées sous forme de signaux numériques, il peut aussi être considéré comme "entièrement numérique".

Finalement, dans la Section I.3, nous avons présenté les principes de base des oscillateurs. Nous avons notamment exposé trois topologies d'oscillateurs typiques. Par rapport aux oscillateurs en anneau et aux oscillateurs Colpitts, les oscillateurs à résonateur LC et à simple paire croisée différentiels sont la structure la plus utilisée dans les circuits radiofréquences en raison de leur simplicité et de leurs performances en termes de bruit de phase. Nous avons également présenté les principales sources de bruit dans les oscillateurs, notamment le bruit thermique, le bruit de scintillement et le bruit de grenaille. Enfin, nous avons présenté le modèle linéaire invariant dans le temps de Leeson et le modèle linéaire variant dans le temps de Hajimiri pour analyser et comprendre les performances en bruit de phase des oscillateurs.

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CHAPTER II

K-Band Triple-Bank DCO (T-DCO) Design

As the core frequency generation module, the DCO mainly determines the overall performances of the ADPLL. Like the conventional VCO, the DCO design suffers from three trade-offs: frequency tuning range, frequency resolution, and phase noise. Moreover, when a DCO is used to generate frequency-modulated chirp, the linearity of frequency tuning also becomes very important. This chapter will focus on some key issues in the design of high-performances K-band DCOs. In Section II.1, we will briefly introduce the GlobalFoundries' 22 nm FD-SOI process (also known as 22 FDX technology) and its main highlights. In Section II.2, the principles and types of DCOs will be summarized. In Section II.3, we will review the development and current research status of DCOs and highlight some typical frequency tuning techniques found in the literature. In Section II.4, we will present the principle of FMCW radars and DCO gain calibration, which is the theoretical basis for the DCO proposal. In Section II.5, we will detail the circuit implementation and simulation results of the proposed K-band low-phase-noise triple-bank DCO (T-DCO) for 76 – 81 GHz FMCW automotive radars, involving a novel back-gate-based fine-tuning structure.

II.1. Overview of 22FDX Technology

II.1.1. Supported EDA Tools

Before introducing the DCO, we first give the EDA (Electronics Design Automation) tools we are currently using and their corresponding versions in [Table II.1.1](#). Virtuoso integrates powerful mixed-signal chip design capabilities that support full-flow design from front-end to back-end. ICADV is Virtuoso's version for advanced node processes.

Spectre is a multi-mode (Spectre, Spectre APS, Spectre X, Spectre XPS MS, etc.) simulation tool for custom chip simulations. Actually, the Spectre APS is used in our simulations. Moreover, with the exponential growth in design rule check (DRC) complexity in advanced nodes, first- and second-generation DRC solutions can no longer support the turnaround requirements needed to ensure that design schedules are met. As shown in [Figure II.1.1](#), the third-generation Pegasus Verification System is a massively parallel, cloud-ready, physical verification signoff solution that improves the performance of DRC runs by up to 10 times, enabling engineers to deliver advanced node integrated circuits to market faster [II-1].

Table II.1.1 Supported EDA Tool Versions.

Tool	Version
Cadence Virtuoso	ICADVM18.1-64b.500.13
Spectre	19.1
Pegasus Verification System	21.31-e114-64b

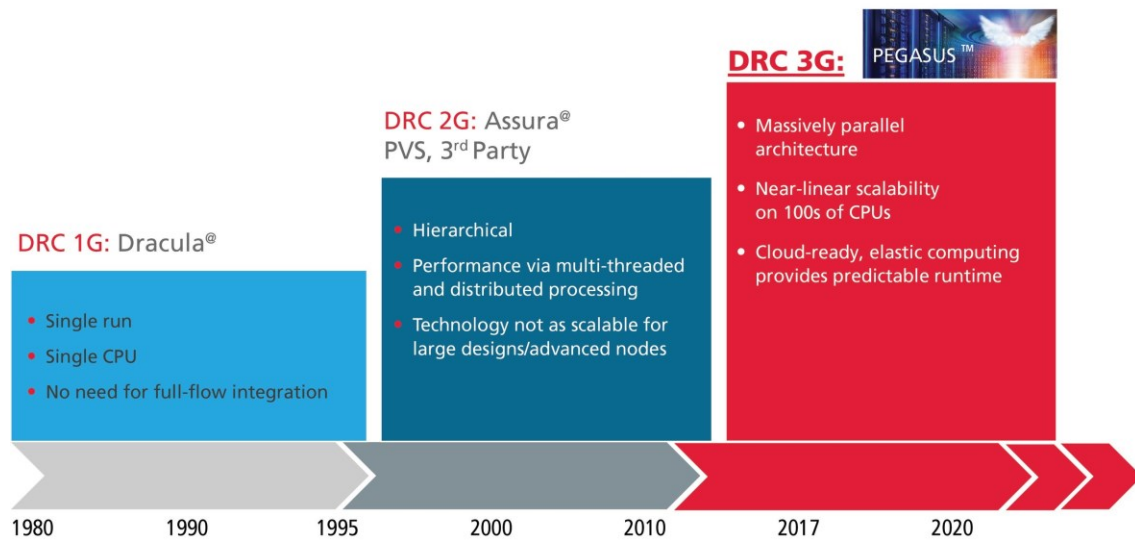


Figure II.1.1 Third-generation Pegasus Verification System.

II.1.2. Preferred Choice for Automotive Radar: FD-SOI

It is well known that the performances of early MOS transistors continued to improve as their size shrank. However, as its gate length approaches 20 nm, its ability to control the current drops dramatically, and the leakage current rises significantly, which makes the conventional planar bulk CMOS technology no longer applicable. Based on this fact,

around 2000, the research group led by Professor Chenming Hu proposed two solutions: the three-dimensional FinFET technology and the FD-SOI technology, which allows Moore's Law to continue today. Moreover, it is worth mentioning that only FinFET technology is feasible in smaller nodes (< 20 nm), however, its cost is too high and it is only suitable for applications with large volumes (mainly for digital circuits) and ultra-high performances. Therefore, planar FD-SOI technologies (28 nm, 22 nm) remain the mainstream for commercial applications due to its cost-effectiveness and FinFET-like performance with energy-efficiency.



Figure II.1.2 (a) Bulk CMOS versus (b) FD-SOI. (Source: STMicroelectronics).

Furthermore, several other advantages of FD-SOI technology make it the preferred choice for current millimeter-wave automotive radars. These advantages are inextricably linked to its particular structure. Figure II.1.2 shows the simplified structures of bulk CMOS and FD-SOI. Unlike bulk CMOS, FD-SOI uses a thin and fully depleted layer of silicon as the active layer. The silicon is placed on top of an insulating buried oxide layer, which is made of silicon dioxide and is separated from the underlying substrate. The following are typical highlights of FD-SOI technology:

- The thin silicon layer in FD-SOI improves the ability of the gate to fully turn off and on the transistor, thus enabling higher circuit speeds and allowing it to operate in the millimeter-wave band.
- The buried oxide layer reduces the parasitic junction (source, drain) capacitance as well as various types of noise, and also effectively suppresses electron flow from source to drain, thus significantly reducing the leakage current that causes performances degradations and improving the threshold voltage stability.
- FD-SOI provides a robust back-gate bias function. By controlling the back-gate bias voltage, the threshold voltage can be flexibly changed to optimize the power consumption and performances of the circuit.

- FD-SOI devices are more reliable under high-temperature conditions due to less power leakage, which makes them ideal for automotive radar applications.

II.1.3. Device Options in 22FDX Library

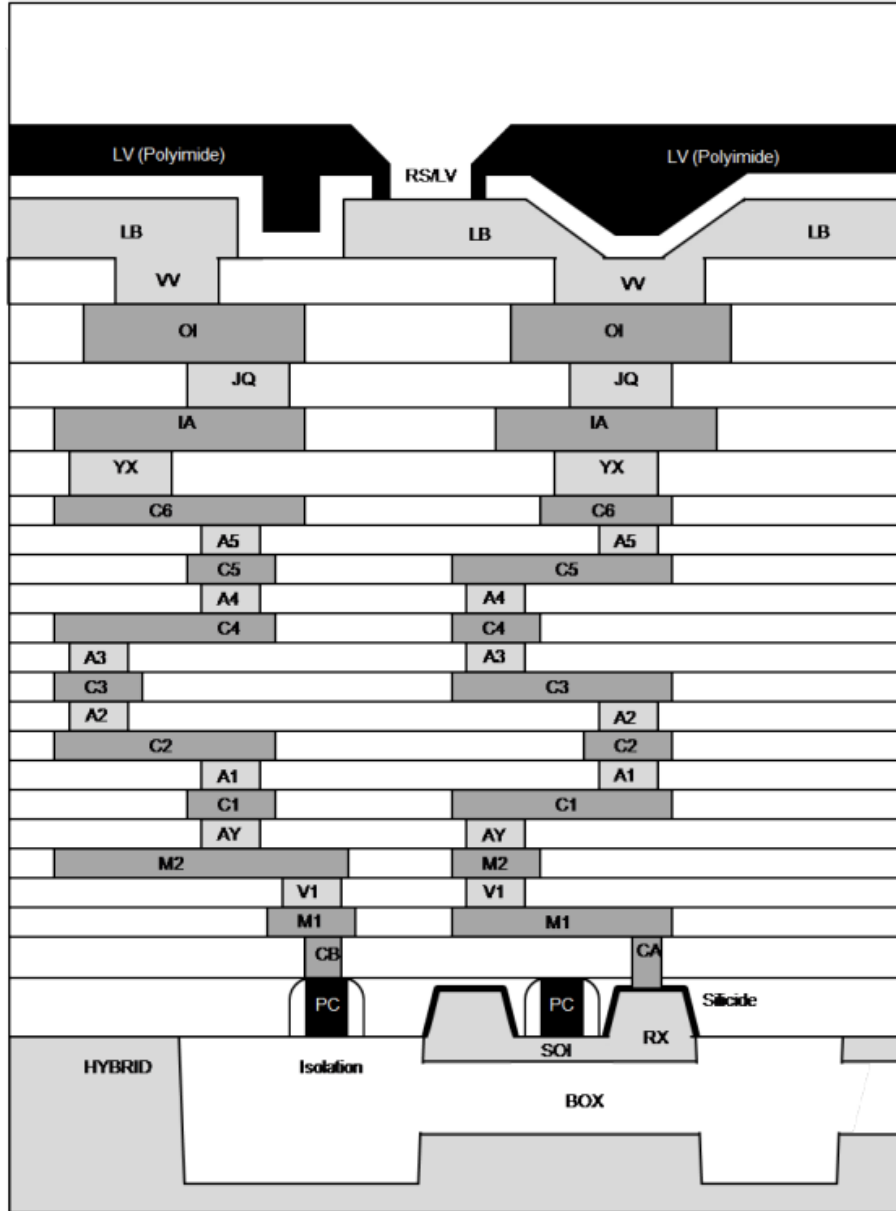


Figure II.1.3 22FDX cross section example.

Prior to introducing the device options, we first give an example of a typical 22FDX cross-section in [Figure II.1.3](#) [II-2]. Each metal layer is responsible for carrying different signals and is separated from other metal layers by insulating materials. It should be noted that the available metal stack in our design is 10M_2Mx_5Cx_1Jx_2Qx_LB (option 19). 10M means that the total number of metal layers in this option is 10. The M1 and M2

metal layers (2Mx) are mainly used for short and narrow wirings inside transistors. The C1 to C5 metal layers (5Cx) are dedicated to wirings between transistors. The J1, Q1, and Q2 metal layers (1Jx, 2Qx) are dedicated to form complex circuits such as differential pairs and high current routings. The top LB metal layer (aluminum) is not included in the above 10 metal layers and is mainly used to form reliable metal-to-metal bonds with the substrate. In summary, the routing of circuits should introduce the lowest possible resistance and capacitance, which helps to ensure that signals are transmitted with the least possible loss and delay.

Note that the 22FDX technology provides a wide range of available device options for the design and manufacture of integrated circuits. These devices can be divided into two categories according to the gate length: standard gate (SG) devices and extended gate (EG) devices. SG devices have a thin oxide layer with a minimum gate length of 20 nm and a nominal voltage of 0.8 V. EG devices have a medium oxide layer and can be further divided into three categories: EGU, EGV, and EG devices, corresponding to minimum gate lengths of 70 nm, 100 nm, and 150 nm, and nominal voltages of 1.2V, 1.5V, and 1.8V, respectively.

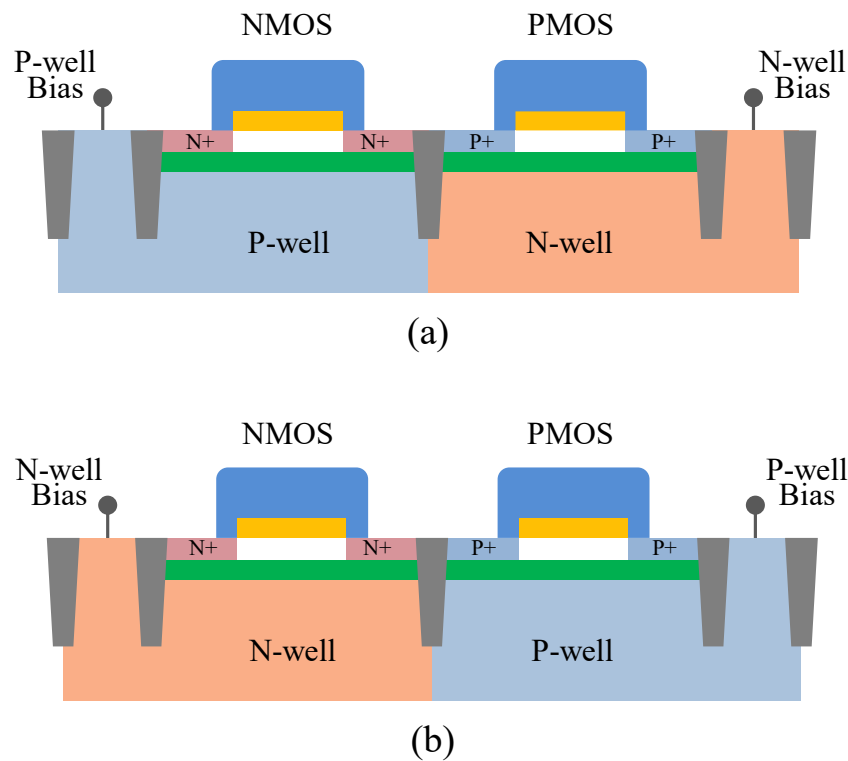


Figure II.1.4 Cross-section view of (a) conventional well and (b) flipped well.

Additionally, SG devices offer four different types of threshold voltages (V_T), namely

high- V_T (HVT), regular- V_T (RVT), low- V_T (LVT), and super-low- V_T (SLVT) [II-3]. As shown in Figure II.1.4, HVT-SG and RVT-SG devices employ conventional well, meaning NMOS is in P-well and PMOS is in N-well. LVT-SG and SLVT-SG devices employ flipped well, meaning NMOS is in N-well and PMOS is in P-well. EG devices offer two types of threshold voltages, namely LVT and SLVT. LVT-EG devices employ conventional well, and SLVT-EG devices employ flipped well. Table II.1.2 summarizes the devices mentioned above and their designations in the Process Design Kit (PDK).

Table II.1.2 Summary of different devices in the PDK.

Device Options	SG Devices				EG Devices	
	HVT	RVT	LVT	SLVT	LVT	SLVT
Conventional Well	√	√			√	
Flip Well			√	√		√
Device Names	hvtnfet hvtpfet	nfet pfet	lvtnfet lvtpfet	slvtnfet slvtpfet	eglvtnfet eglvtpfet	egslvtnfet egslvtpfet

The simulation results for the four smallest size NMOS ($W = 100$ nm, $L = 20$ nm) are given in Figure II.1.5. They are all SG devices, and it can be seen that the threshold voltage difference between the hvtnfet and the slvtnfet is up to about 120 mV. Figure II.1.6 shows the simulation results of the lvtnfet under different back-gate bias voltages, and the variation rate of threshold voltage with back-gate voltage is approximately 70 mV/V, which is much higher than the variation rate in the bulk CMOS process (25 mV/V).

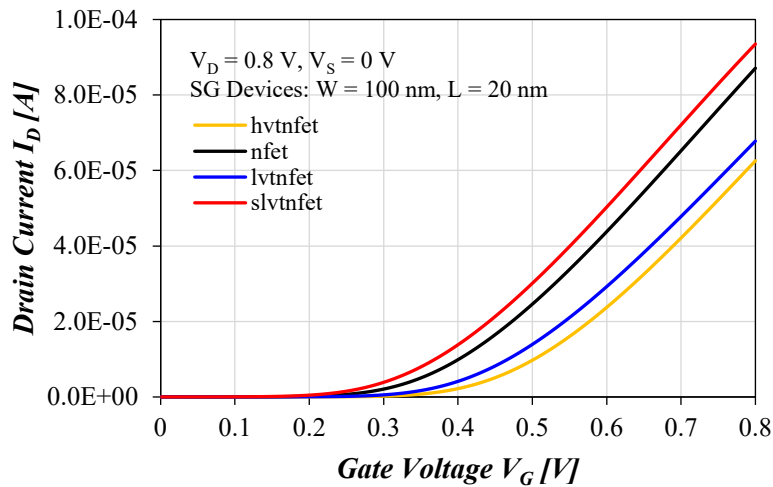


Figure II.1.5 Threshold voltage for different SG devices.

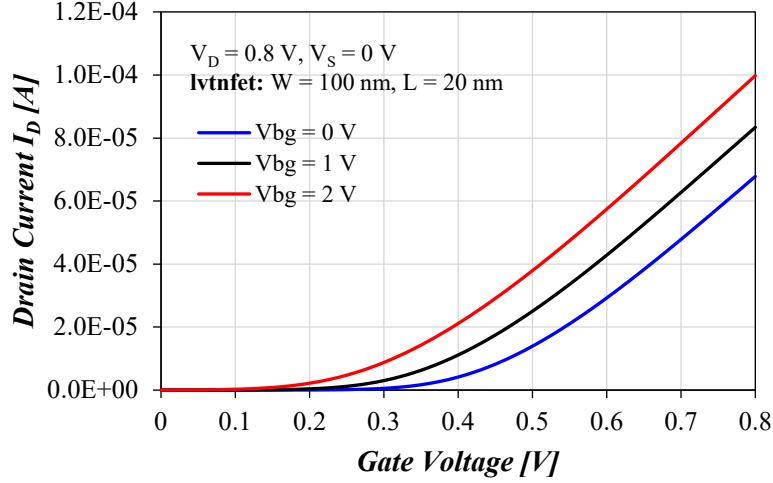


Figure II.1.6 Threshold voltage for different back-gate voltages.

Moreover, it should be noted that the 22FDX technology offers several different libraries, with three being primarily used for our design: the core library (cmos22fdsoi), the RF library (cmos22fdsoi_rf), and the mm-W library (cmos22fdsoi_mmw). As the names implies, the RF and mm-W libraries are mainly suitable for RF and mm-W circuit designs. Of course, in actual design, it is necessary to flexibly select the device type, back-gate voltage, and process library for optimal performances.

II.2. Introduction to DCO

II.2.1. From VCO to DCO

Most oscillators, such as VCOs, require tunable oscillation frequencies within a certain range in order to achieve channel selection, frequency modulation, or frequency compensation. Figure II.2.1 illustrates a simplified structure of a typical cross-coupled LC-based VCO using a MOS varactor and its frequency-voltage (F - V) characteristic curve. When the control voltage V_{ctrl} applied to the analog MOS varactor is gradually increased from V_1 to V_2 , the oscillation frequency gradually changes from f_1 to f_2 . The slope of the curve K_{VCO} represents the gain of the VCO, and the output frequency f_{VCO} can then be expressed as

$$f_{VCO} = f_0 + K_{VCO}V_{ctrl} \quad (\text{II. 2. 1})$$

where f_0 represents the frequency at the intersection point of the F - V extension line and

the y-axis. Moreover, in practice, the value of K_{VCO} is not constant, which leads to nonlinearity in the frequency tuning of the VCO.

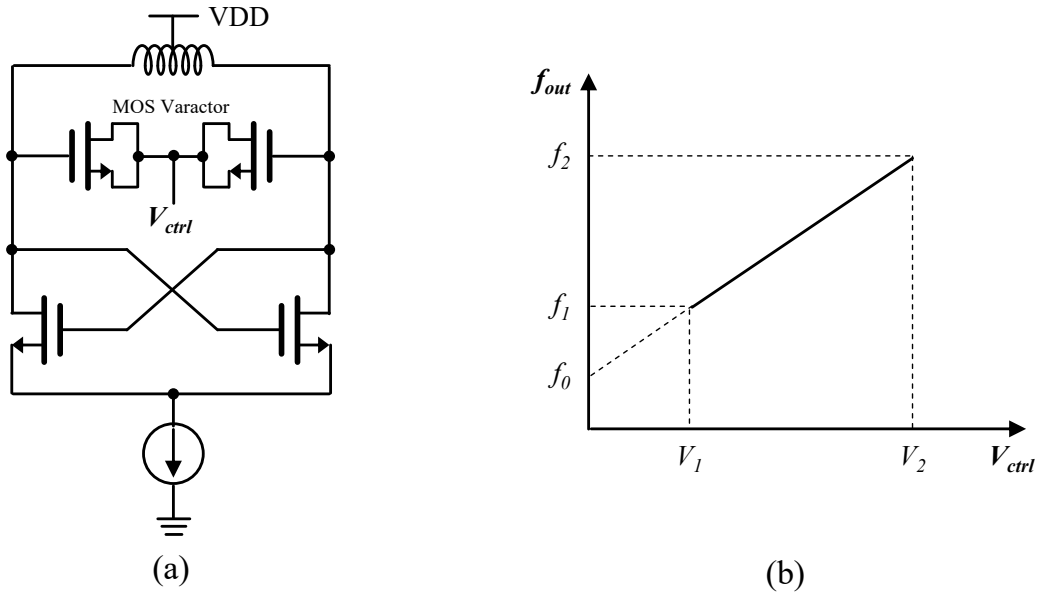


Figure II.2.1 (a) Simplified structure of a typical LC-based VCO using the MOS varactor. (b) Frequency-voltage characteristic curve.

However, several specific limitations of the LC-based VCO in advanced deep sub-micrometer (or nanoscale) CMOS processes are revealed:

- The supply voltage gradually decreases as the CMOS process scales, and the nominal voltage for the advanced 22 nm FD-SOI process can be as low as 0.8 V. Such a low voltage makes it difficult for VCOs in advanced nodes to achieve wide frequency tuning range, high resolution and low phase noise simultaneously.
- The nanoscale transistor features a relatively high threshold voltage, such as 0.35 V, further reducing the available voltage margin.
- The nonlinearity of the capacitance-voltage ($C-V$) curve becomes more and more severe at low supply voltages. As shown in Figure II.2.2(a), the linear tuning range is strongly compressed and the gain K_{VCO} is undesirably high in deep sub-micrometer CMOS processes, so the oscillator is very sensitive to noise and interference, leading to severe degradation of its overall performances [II-4].

To verify these findings, a differential MOS varactor is designed and simulated. The cross-section diagram of a MOS varactor (NFET in N-well) in the GF 22 nm FD-SOI process is illustrated in Figure II.2.2(b). It is a 3-terminal device, where pin 1 (Gate)

represents the polysilicon finger, pin 2 (N-well) represents N^+ over N-well, and pin 3 (PSUB) is the substrate contact and should always be connected to the ground [II-5]. The differential MOS varactor using the device egncap_rf (extended gate NFET over N-well capacitor from the RF library) is configured as in Figure II.2.2(c). The control voltage V_{ctrl} is applied to the common pin 2, the DC voltage of the two differential gates (pin 1) is 1.2 V. The employed egncap_rf has a single polysilicon finger with a length and width of 250 nm and 1 μm , respectively.

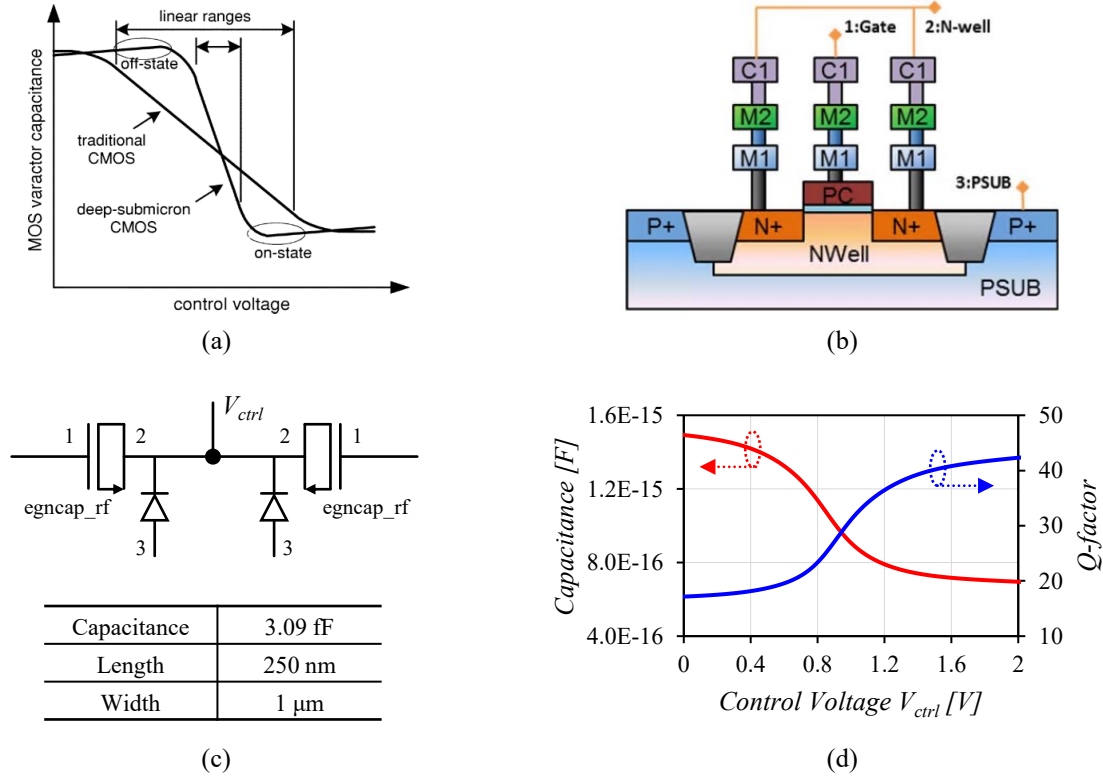


Figure II.2.2 (a) Idealized C - V curves of a MOS varactor for both a traditional and deep sub-micrometer CMOS process. (b) Cross-section view of the MOS varactor model. (c) Differential MOS varactor using the device egncap_rf and its main parameters. (d) Simulated capacitance and Q -factor versus voltage curves of (c).

Furthermore, this differential MOS varactor is characterized by 2-port S -parameter simulations. The total capacitance and Q -factor are defined by using Y_{11} :

$$C = \text{Im}(Y_{11})/\omega \quad (\text{II. 2. 2})$$

$$Q = \text{Im}(Y_{11})/\text{Re}(Y_{11}) \quad (\text{II. 2. 3})$$

As shown in Figure II.2.2(d), the C - V curve of this varactor has a relatively narrow and imperfect linear range, while its Q -factor is poor. Therefore, designing a high-

performance wideband VCO using this varactor is challenging.

Based on these facts, DCOs that use digital signals rather than analog voltages to control the oscillation frequency have become a current research hotspot and are receiving more and more attention. There are three main types of DCOs in the literature: the ring oscillator-based (RO-based) DCO, the DAC-based DCO, and the LC-based DCO.

II.2.2. Different Types of DCO

II.2.2.1. RO-Based DCO

In Chapter I, the basic principle of a single-ended ring oscillator based on a chain of inverters has been described, whose oscillation frequency can be regulated by changing the number or the delay time of the inverters. Therefore, an RO-based DCO can be implemented by digitally controlling these two parameters.

II.2.2.1.1. Changing the number of inverters

A typical structure of this type of RO-based DCO is shown in [Figure II.2.3](#) [II-6], which is composed of a coarse-tuning block to extend the frequency range and a fine-tuning block to improve the resolution. The number of inverters in the loop can be changed by controlling the multiplexer through digital coarse-tuning words. Fine frequency resolution is achieved by changing the driver strength on the fixed loading or adjusting the load capacitance.

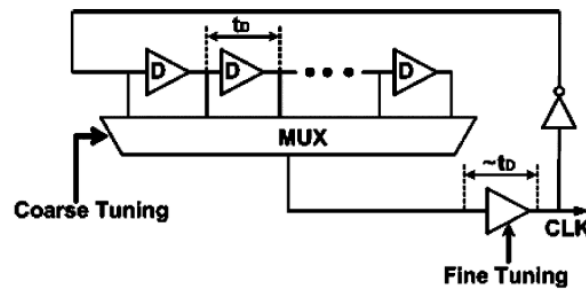


Figure II.2.3 A conventional RO-based DCO.

II.2.2.1.2. Changing the delay time of inverters

[Figure II.2.4](#) illustrates a seven-stage RO-based DCO in which one inverter is replaced by a NAND gate to disable the oscillator during idle mode [II-7]. A set of 21 tri-state inverters are connected in parallel with each inverter. When the tri-state inverters driven by 126-bit digital control words are enabled, additional current is added to each inverter stage, thereby changing its delay time. However, this structure suffers from some

drawbacks, such as relatively high power consumption and low maximum oscillation frequency due to the high capacitive load. By the way, these are the main drawbacks of RO-based VCO as well.

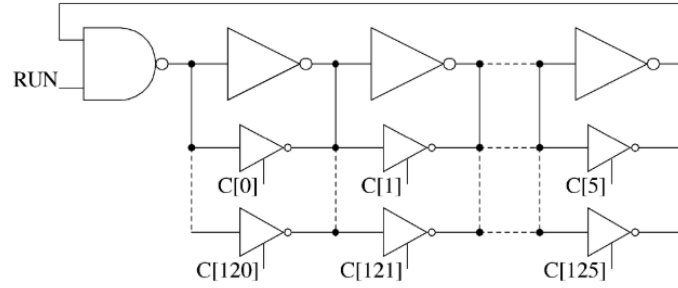


Figure II.2.4 RO-based DCO using parallel tri-state inverters.

II.2.2.2. DAC-Based DCO

As shown in [Figure II.2.5\(a\)](#), the DAC-based DCO is implemented by using a DAC to convert digital control words into an analog voltage signal that directly controls the VCO [II-8], [II-9], or into an analog current signal that controls the ring oscillator [II-10]. The advantage is that this structure allows the use of an existing VCO in a digital PLL. However, the performances of the DAC-based DCO are strongly dependent on the DAC itself. Since DAC introduces additional power consumption and noise, and the matching design between DAC and VCO is quite complex, thus, this approach is not widely used.

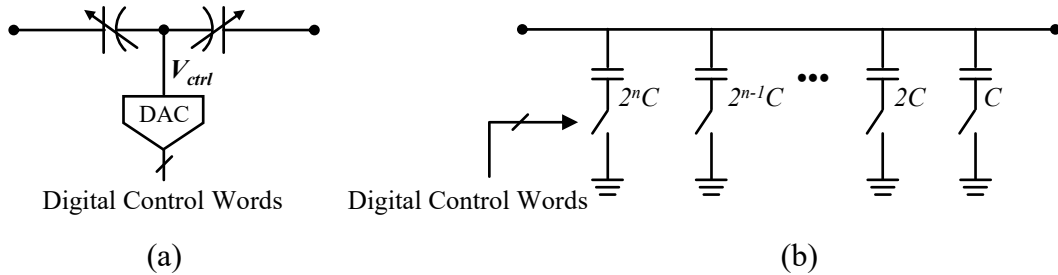


Figure II.2.5 (a) MOS varactor controlled by the DAC. (b) Binary-weighted switched-capacitor bank controlled by the digital signal.

II.2.2.3. LC-Based DCO

The achievable frequency tuning range of early VCOs relying on MOS varactors is often narrow. Therefore, a straightforward approach to enlarge the frequency tuning range is to use switched capacitors in parallel with the MOS varactor. As shown in [Figure II.2.5\(b\)](#), the switched capacitors can be arranged in a binary weighted bank, which can be controlled by digital control words. Essentially, this type of wideband VCO is no

longer a purely analog circuit, but a mixed-signal circuit. If the voltage-controlled varactor is also removed and replaced by digitally controlled capacitor banks with different frequency resolutions, a classical multi-bank LC-based DCO can be formed. Consequently, the LC-based DCO inherits the advantages of the LC-based VCO, such as high operating frequency and excellent phase noise performances, making it the most popular DCO. Moreover, the LC-based DCO can also be implemented by changing the inductance value using digital control signals. However, this approach is rarely employed due to its complexity.

II.3. Development and Research Status

II.3.1. First Multi-Gigahertz DCO for RF Applications

In 2003, the first multi-gigahertz LC-based DCO for RF applications was proposed in [II-4], contributing significantly to the in-depth development of DCOs.

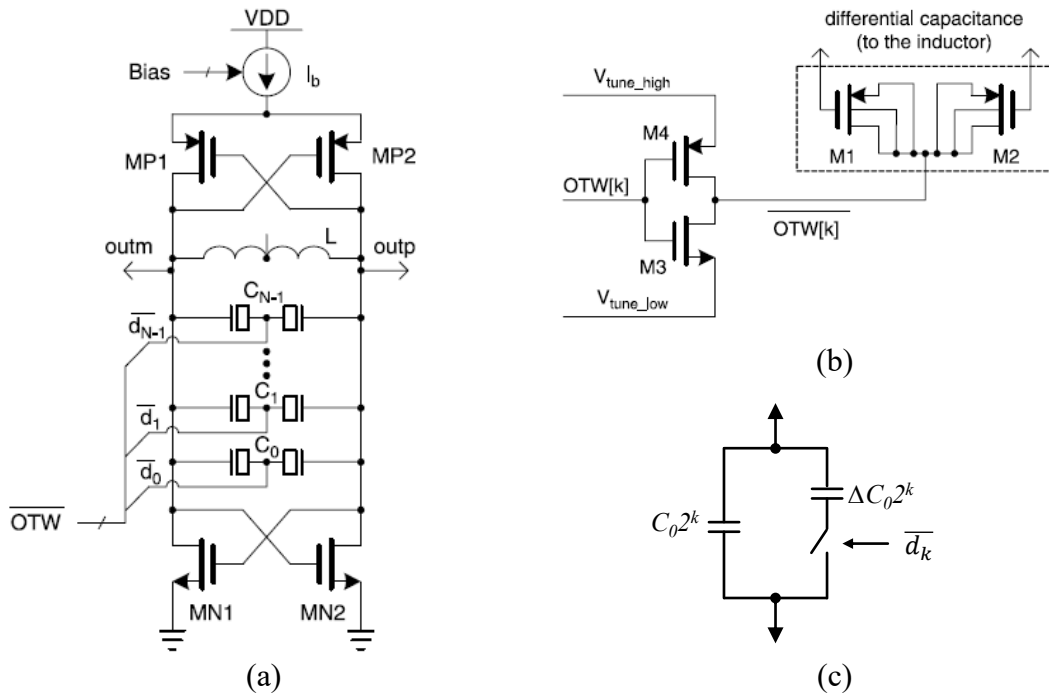


Figure II.3.1 (a) DCO with discrete tuning controls. (b) Differential PMOS varactor driven by an inverter. (c) Modeling a binary-weighted switched capacitor.

As shown in Figure II.3.1(a), the DCO employs a complementary cross-coupled structure with a top current source. The resonant frequency of the parallel LC tank is

given by

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (\text{II. 3. 1})$$

where L and C are the total inductance and capacitance, respectively. Moreover, the total capacitance is quantized into an N number of smaller digitally controlled MOS varactors. As shown in Figure II.3.1(b), they are configured differentially and each of them consists of two PMOS transistors M1 and M2, whose drain, source, and back gate are shorted together and tied to the inverter output. Depending on the oscillator tuning word (OTW), the inverter output has only two discrete voltage values ($V_{\text{tune_high}}$ and $V_{\text{tune_low}}$), which in turn make the PMOS varactor operate either in the off-state or in the on-state. The capacitance difference between these two states of the k_{th} PMOS varactor is

$$\Delta C_k = C_{1,k} - C_{0,k} \quad (\text{II. 3. 2})$$

where $C_{1,k}$ and $C_{0,k}$ represent the high and low capacitance, respectively. Considering the digital control bit $\overline{d_k}$, the capacitance of k_{th} PMOS varactor can be expressed as

$$C_k = C_{0,k} + \overline{d_k} \cdot \Delta C_k \quad (\text{II. 3. 3})$$

Hence, the Equation (II. 3.1) can be rewritten as

$$f = \frac{1}{2\pi\sqrt{L \sum_{k=0}^{N-1} (C_{0,k} + \overline{d_k} \cdot \Delta C_k)}} \quad (\text{II. 3. 4})$$

Figure II.3.1(c) shows a model of a binary-weighted switched capacitor with the digital control bit $\overline{d_k}$, the k_{th} such switched capacitor has a weight of 2^k , which is composed of 2^k basic PMOS varactors in parallel for better matching. The low capacitance and capacitance difference of one basic PMOS varactor are C_0 and ΔC_0 , respectively. Thus, the capacitance of k_{th} switched capacitor is

$$C_k = C_0 \cdot 2^k + \overline{d_k} \cdot \Delta C_0 \cdot 2^k \quad (\text{II. 3. 5})$$

Therefore, as shown in Figure II.3.2, the total capacitance of the binary-weighted switched-capacitor bank of size N can be expressed as

$$C_B = \sum_{k=0}^{N-1} (C_0 \cdot 2^k + \overline{d_k} \cdot \Delta C_0 \cdot 2^k)$$

$$\begin{aligned}
&= \sum_{k=0}^{N-1} C_0 \cdot 2^k + \sum_{k=0}^{N-1} \overline{d}_k \cdot \Delta C_0 \cdot 2^k \\
&= C_{0,SUM} + \sum_{k=0}^{N-1} \overline{d}_k \cdot \Delta C_0 \cdot 2^k
\end{aligned} \tag{II. 3. 6}$$

where the first term $C_{0,SUM}$ represents all non-adjustable capacitance, and the second term represents the effective capacitance for frequency regulation of the DCO.

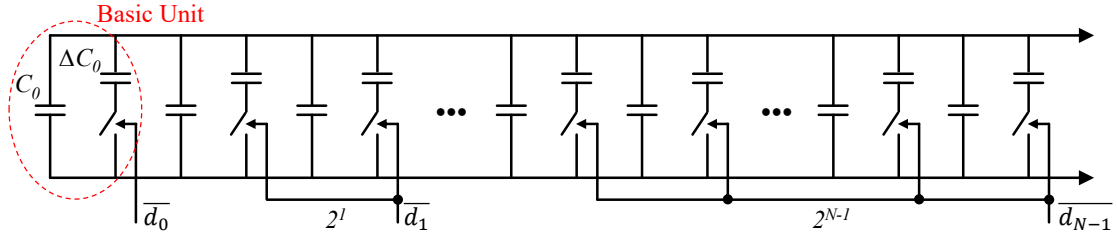


Figure II.3.2 Binary-weighted switched-capacitor bank of size N .

In addition, to obtain a Bluetooth band of 80 MHz and a frequency resolution of 1 kHz in the RF band of 2.4 GHz, as shown in Figure II.3.3, three-stage switched-capacitor banks with different frequency steps are deployed in each of the three operating modes: PVT, acquisition, and tracking. The tracking mode is further divided into integer tracking mode and fraction tracking mode, and the latter is used to achieve a fractional resolution.

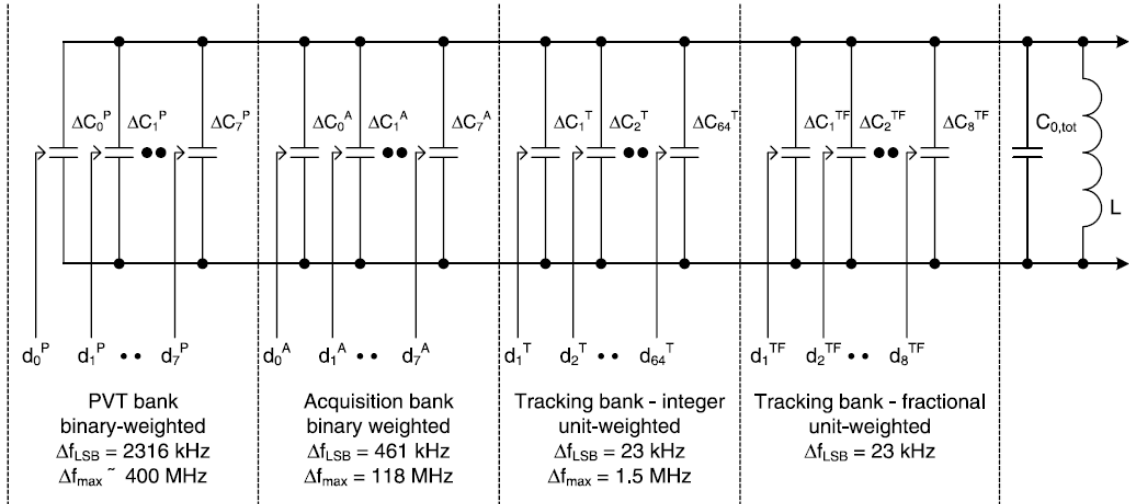


Figure II.3.3 LC tank with three-stage switched-capacitor banks.

Once the ADPLL is powered on, the PVT and acquisition banks coarsely set the desired frequency in sequence for channel selection. Since these two banks need to achieve a wide frequency range at the cost of a relatively poor frequency resolution, the

binary-weighted structure is employed to arrange a large number of PMOS varactors. Therefore, based on the Equation (II. 3.6) the total capacitance of these two banks can be given by

$$C^P = C_0^P + \sum_{k=0}^{N^P-1} \overline{d}_k^P \cdot \Delta C^P \cdot 2^k \quad (\text{II. 3. 7})$$

$$C^A = C_0^A + \sum_{k=0}^{N^A-1} \overline{d}_k^A \cdot \Delta C^A \cdot 2^k \quad (\text{II. 3. 8})$$

where C_0^P and C_0^A represent the total non-adjustable capacitance of the PVT bank and the acquisition bank, N^P and N^A are the number of binary-weighted switched capacitors, \overline{d}_k^P and \overline{d}_k^A are the inverted PVT and acquisition bits, and ΔC^P and ΔC^A represent the capacitance difference of the basic unit.

Furthermore, during the actual transmission and reception, the tracking bank is used to precisely regulate the oscillation frequency with a fairly high frequency resolution, thereby employing the unit-weighted structure controlled by thermometer codes, which means all switched capacitors in this bank are identical. Thus, the total capacitance is

$$C^T = C_0^T + \sum_{k=0}^{N^T-1} \overline{d}_k^T \cdot \Delta C^T \quad (\text{II. 3. 9})$$

where C_0^T represents the total non-adjustable capacitance, N^T is the number of unit-weighted switched capacitors, \overline{d}_k^T is the inverted tracking bits, and ΔC^T represents the capacitance difference of one switched capacitor in the tracking bank. Considering the fixed capacitance $C_{0,tot}$ in [Figure II.3.3](#), the total capacitance of the LC tank is given by

$$C = C_{0,tot} + C^P + C^A + C^T \quad (\text{II. 3. 10})$$

In addition, it should be noted that at any given time, only switched capacitors belonging to the same capacitor bank are allowed to switch, while the digital control words of the other two banks are in the locked state. Moreover, the high-speed dithering technique is used for the fractional operation, the capacitance of the smallest switched capacitor (tracking bank) alternates between the low capacitance and high capacitance several times during the one reference cycle, thus leading to a fractional multiple of its capacitance difference ΔC^T . Meanwhile, the issue of spurs generated by the periodic

dithering is addressed by the $\Sigma\Delta$ modulation. The implementation of this 2.4 GHz DCO is based on a 0.13 μm CMOS process, and it achieves a large frequency tuning range of 500 MHz and consumes 2.3 mW from a 1.5 V supply voltage. The phase noise is -112 dBc/Hz at 500 kHz frequency offset.

II.3.2. Overview of Frequency Tuning Techniques

In recent years, one of the research hotspots of DCOs is their frequency tuning techniques. In addition, according to different application scenarios, some DCOs also aim to achieve low power consumption or low phase noise, which is mainly related to the choice of the DCO structure, but also cannot be separated from the frequency tuning techniques. Therefore, in this subsection, we will highlight several typical frequency tuning techniques found in the literature.

II.3.2.1. Mismatched MOS Varactors

In order to achieve a finer frequency resolution than the traditional single MOS varactor in Figure II.3.1(b), a common approach is to use two parallel mismatched MOS varactors.

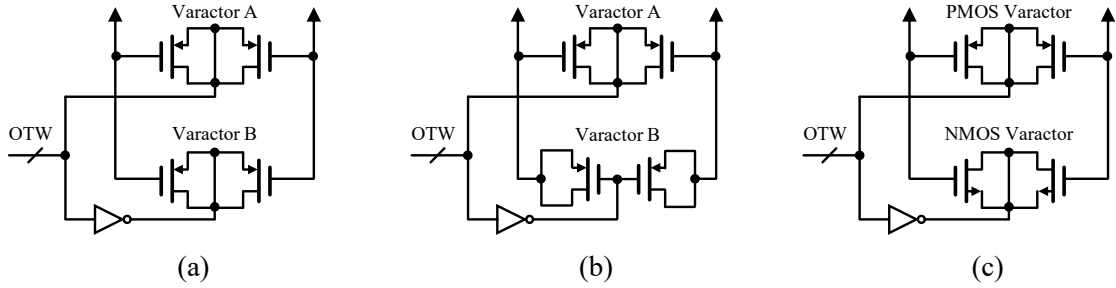


Figure II.3.4 (a) Mismatch between two PMOS varactors with different sizes. (b) Mismatch between two PMOS varactors with different connections. (c) Mismatch between a PMOS varactor and a NMOS varactor.

As illustrated in Figure II.3.4(a), this structure proposed in [II-11] consists of two differential PMOS varactors (denoted as A and B). The PMOS size of varactor A is slightly larger than that of varactor B (smallest). In addition, the OTW is directly applied to the varactor A, and its inverted complementary signal ($\overline{\text{OTW}}$) is used to control the varactor B. It is known that at any given OTW, only one varactor operates in the inversion region and the other in the depletion region. Since they are very close in size, this leads to a tiny capacitance difference. When the width/length ratios of the PMOS in varactor A

and varactor B are $0.24\ \mu\text{m}/0.18\ \mu\text{m}$ and $0.22\ \mu\text{m}/0.18\ \mu\text{m}$, respectively, the simulation results show that a capacitance difference of 21 aF can be obtained in a $0.18\ \mu\text{m}$ CMOS process. Meanwhile, using this structure, the proposed 3.8 GHz DCO achieves a fine frequency resolution of 20 kHz.

In addition, two PMOS varactors of the same size but different connections form a similar mismatched structure shown in [Figure II.3.4\(b\)](#), the proposed DCO covers the frequency band from 5.7 GHz to 6.3 GHz, and it achieves a capacitance difference of 28 aF in a $0.18\ \mu\text{m}$ CMOS process, the corresponding fine frequency resolution is about 110 kHz [II-12]. Moreover, another mismatched structure is shown in [Figure II.3.4\(c\)](#), which consists of a PMOS varactor and an NMOS varactor, and both varactors are of the same size. The proposed DCO is implemented in a 65 nm CMOS process and oscillates from 4.5 GHz to 5.5 GHz, it achieves a fine frequency resolution of 1.4 kHz through the obtained capacitance difference of 0.8 aF [II-13].

Apparently, this type of mismatched structure allows for a tiny capacitance difference; however, the stability of this structure is highly dependent on the process.

II.3.2.2. Switched Capacitors

Switched-capacitor structures were first widely used to extend the frequency tuning range of VCOs, and a commonly used single-ended structure is shown in [Figure II.3.5\(a\)](#). The NMOS transistor switches one plate of a fixed capacitor to the ground (ON state) or leaves it floating (OFF state), while the other plate is connected to the resonant tank of the oscillator [II-14], [II-15].

Furthermore, as shown in [Figure II.3.5\(b\)](#), its differential structure has also been widely employed [II-16], [II-17]. Compared with the single-ended structure, the two NMOS switches will contribute two series drain-to-source parasitic resistors in the ON state ($EN = 1$) and a smaller parasitic capacitance in the OFF state ($EN = 0$). It is worth noting that the voltage at the two floating points A and B is slightly higher than the supply voltage V_{DD} in the OFF state, which does not significantly reduce the lifetime of the NMOS switches M_0 and M_1 since their channel do not conduct any current in the OFF state [II-18].

Moreover, as shown in [Figure II.3.5\(c\)](#), an optimized differential structure using only one NMOS switch was proposed in [II-19] and adopted in [II-20] where the inverter does not consume any static power and the main role of the large resistors is to bias the voltage

at the drain/source of M_0 to VDD in the OFF state, thereby reducing and getting a better control of the capacitance due to the reverse biased drain-to-bulk junction. In addition, there is only one ON parasitic resistor in this structure, so its Q -factor is about twice that of the previous structure for the same size MOS switch; however, its parasitic capacitance in the OFF state is higher.

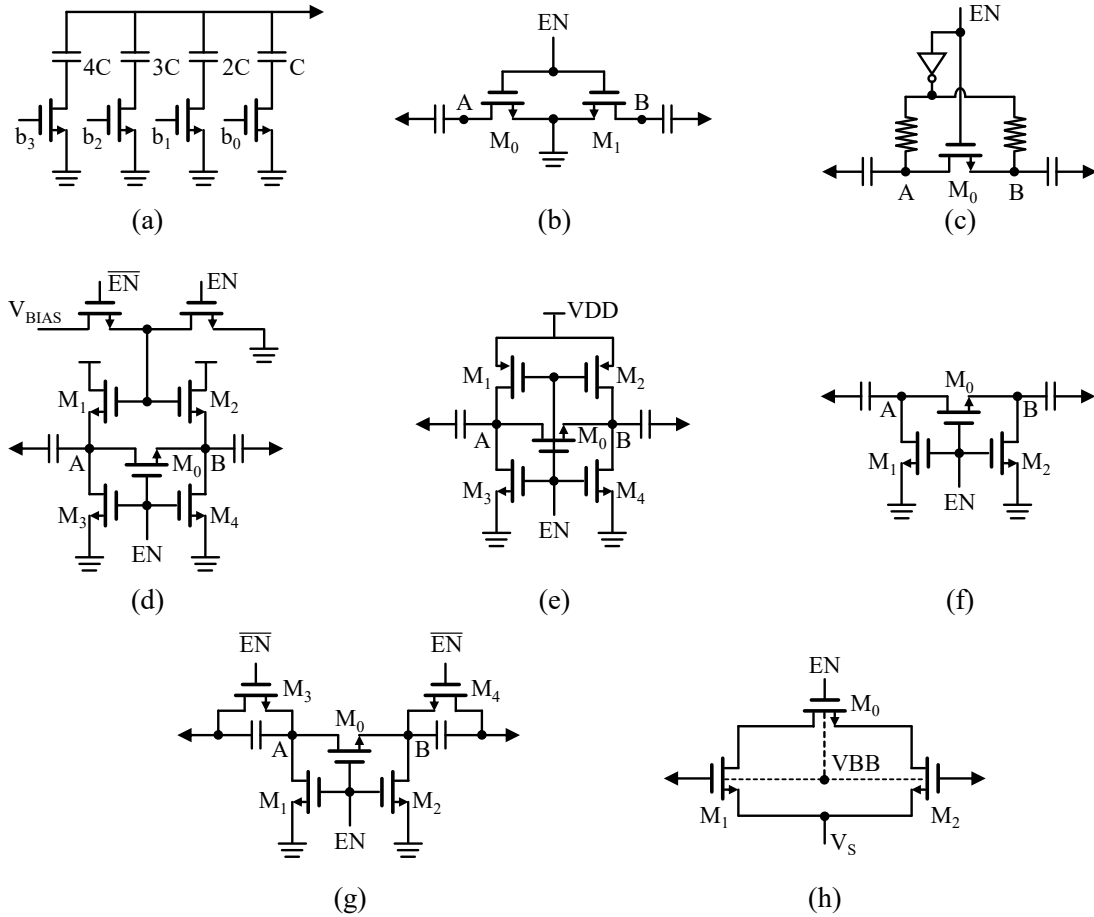


Figure II.3.5 Common structures of switched capacitors.

An alternative equivalent structure was proposed in [II-18]. As shown in [Figure II.3.5\(d\)](#), this switched capacitor adopts two cascaded NMOS switches instead of a large resistor. In the OFF state, the two pull-up NMOS transistors M_1 and M_2 are turned on and the two pull-down NMOS transistors M_3 and M_4 are turned off, so that the drain and source of M_0 are charged to VDD. Correspondingly, in the ON state, they are discharged via M_3 and M_4 to ground. The disadvantage is that such a single switched capacitor employs up to nine transistors (including inverters), thus inevitably leading to a large area and a higher noise level.

In addition, [Figure II.3.5\(e\)](#) illustrates a simplified structure utilized in [II-21]-[II-23].

The gates of two pull-up PMOS transistors are directly connected to the enable signal EN, avoiding the use of the bias circuit and the inverter. Therefore, the same functionality as the previous structure can be achieved by using only five transistors. However, it is still a more complex structure compared to Figure II.3.5(b) and Figure II.3.5(c).

Figure II.3.5(f) illustrates a more straightforward structure that contains only three transistors, the series switch M_0 with two pull-down transistors, M_1 and M_2 , are used to effectively turn the cell between its high and low capacitance states [II-24]-[II-26]. In the ON state, the source and drain of the M_0 are biased to the ground. In addition, a comparable size of these three transistors results in a smaller ON resistance, hence a better Q -factor, although M_1 and M_2 contribute part of the parasitic capacitance in the OFF state.

Another structure suitable for large fixed capacitors was employed in [II-17] and [II-27]. As shown in Figure II.3.5(g), two fixed large capacitors are connected in parallel with two switches. In the OFF state, these two parallel switches are turned on, thus shorting the large capacitors and leading to a better OFF Q -factor (Q_{OFF}). Moreover, in the ON state, the forward back-gate bias reduces the ON resistance, improving the ON Q -factor (Q_{ON}).

Figure II.3.5(h) shows a new switched-capacitor structure [II-27]. The sizes of M_{0-2} are the same, and V_S is biased to a voltage slightly higher than the gate voltage of M_1 and M_2 , making them (M_1 and M_2) completely switched off. As a result, only the gate-to-source and gate-to-drain overlap capacitances are employed in this structure, thereby allowing an excellent capacitance resolution. In addition, this structure is very compact, although suffering from a trade-off between stability and parasitic.

Switched-capacitor structures have been used for more than 20 years and have a wide range of applications in both VCOs and DCOs. This structure is insensitive to the control voltage and has excellent robustness due to the use of MOS switches whose ON/OFF is determined by the threshold voltage. Moreover, this structure allows very flexible configurations and offers a more attractive Q -factor, making it more favorable for our DCO designs.

II.3.2.3. Digital Controlled Artificial Dielectric (DiCAD)

An open-circuited DiCAD stub used as the tuning element was innovatively proposed in [II-28]. As shown in Figure II.3.6, the top two metal layers M9 and M8 constitute a 2.25 μm thick RF differential transmission line (DTL: $L = 152 \mu\text{m}$, $W = 20 \mu\text{m}$, $G = 10$

μm), and the following metal layers M7 and M6 form the underlying periodic artificial dielectric floating strips ($D = 3 \mu\text{m}$, $S = 0.5 \mu\text{m}$), which are digitally controlled by uniformly inserted NMOS π -switches. By turning on or off these switches, the effective dielectric constant of the DiCAD DTL can be manipulated linearly, thereby changing the oscillation frequency of the DCO.

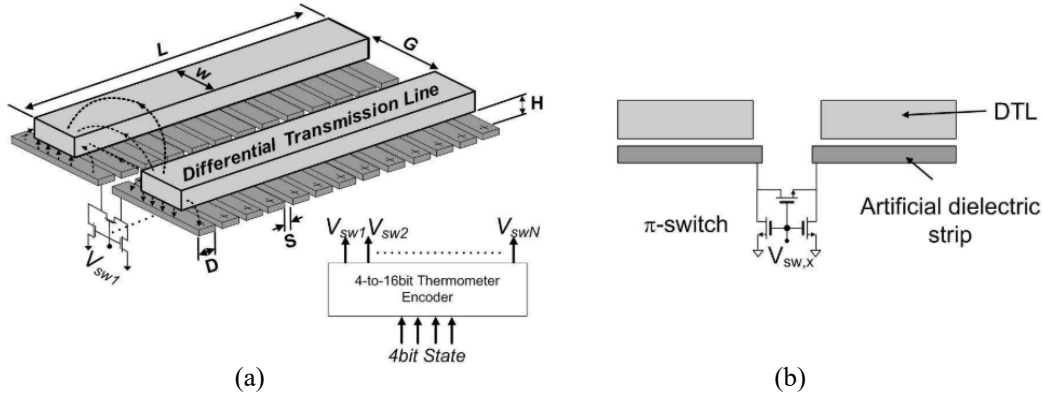


Figure II.3.6 General DiCAD differential transmission line configuration. (b) Cross-sectional view of DiCAD differential transmission line strip.

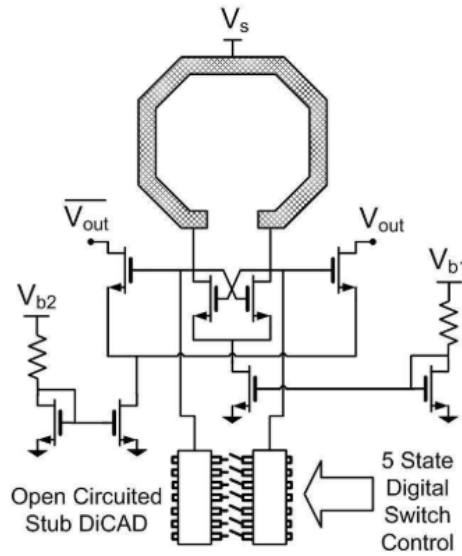


Figure II.3.7 Schematic of the DiCAD DCO

The corresponding DiCAD DCO is illustrated in [Figure II.3.7](#), which adopts a standard cross-coupled NMOS pair loaded by a single-turn center-tapped inductor and an open-circuited DiCAD DTL, standard current mirrors are employed to drive the DCO core and buffers. This DiCAD DCO is implemented in UMC's 90 nm CMOS process and achieves a frequency tuning range of approximately 9.27 % (5.56 GHz) around the center

frequency of 61 GHz, leading to a frequency resolution of about 1.39 GHz. Moreover, its phase noise is lower than -90 dBc/Hz at 1 MHz frequency offset, and it consumes 8.52 mW from a 1.2 V supply voltage.

Based on the same DiCAD technique, two other 60 GHz DCOs were proposed in [II-29], [II-30]. Simplified schematics of the inductor-based DCO and the transformer-based DCO are shown in Figure II.3.8(a) and Figure II.3.9(a), respectively. Their coarse- and medium-tuning banks using digitally controlled DTL are identical, as illustrated in Figure II.3.8(c). Shorting metal strips (i.e., on M7 and M6) beneath the DTL via NMOS switches increases the capacitance per unit length, which further increases the phase shift along the DTL and reduces the resonant frequency of the LC tank. Moreover, to ensure monotonicity, the coarse- and medium-tuning banks employ 19-bit and 8-bit thermometer codes, respectively. Each bit in the coarse-tuning bank achieves a capacitance difference of ~ 1 fF, corresponding to a coarse frequency resolution of ~ 315 MHz at 60 GHz, whereas each bit in the medium-tuning bank introduces a capacitance difference of ~ 0.13 fF, the medium frequency resolution is ~ 39 MHz.

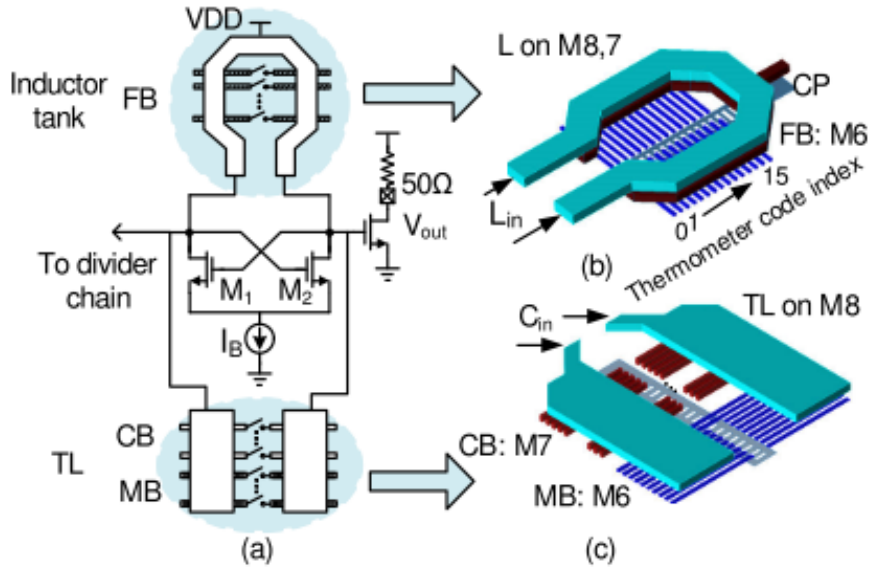


Figure II.3.8 (a) Schematic of the 60 GHz inductor-based DCO. (b) Inductor-based fine-tuning bank. (c) Reconfigurable TL for coarse-tuning and medium-tuning.

The inductor-based fine-tuning bank is illustrated in Figure II.3.8(b). Equal-width metal shield strips on M6 (1 μ m width and 1 μ m spacing) are placed beneath the inductor, which acts as the capacitive load to the inductor. When an NMOS switch controlled by a thermometer code shorts a metal strip pair, the capacitive loading on the input inductance

L_{in} increases. Moreover, the simulated inductance change per bit ($\Delta L/\text{bit}$) is reduced progressively from 54.4 fH to 0.21 fH, corresponding to fine frequency steps of 23 MHz and 140 kHz at 60 GHz, respectively.

The transformer-based fine-tuning bank is illustrated in Figure II.3.9(b). The primary and secondary coils feature a weak coupling factor (k) of 0.25. Compared to directly loading the primary coil inputs, the capacitive loading effect on the input inductance L_{in} is reduced by a factor proportional to k^2 . Moreover, the secondary coil is configured by a digitally controlled DTL. Shorting each strip pair introduces a capacitance difference of 50 aF, and the equivalent inductance difference seen from the primary coil is 6 fH/bit, corresponding to a frequency step of ~ 2.5 MHz at 60 GHz.

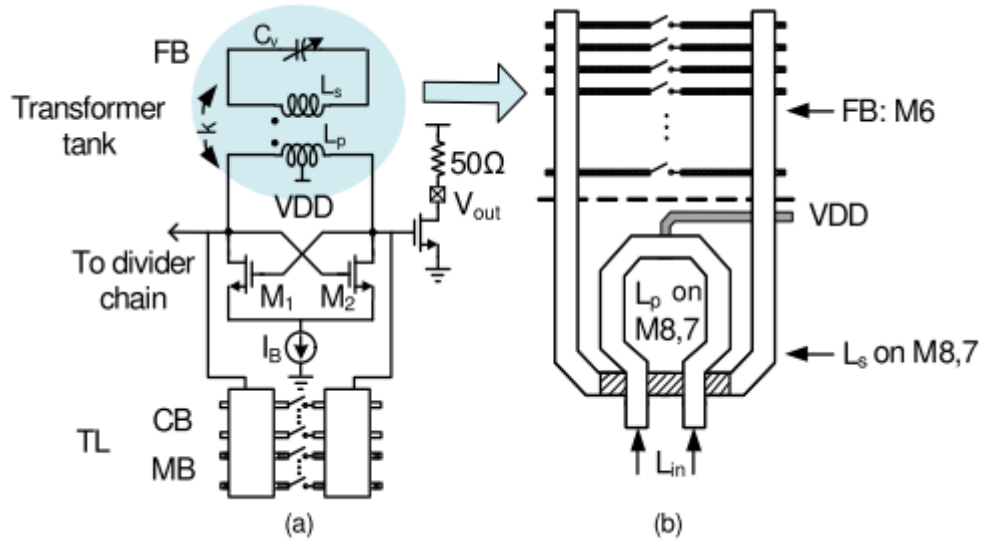


Figure II.3.9 (a) Schematic of the 60 GHz transformer-based DCO. (b) Transformer-based fine-tuning bank.

Furthermore, the frequency range of these two DCOs is ~ 6 GHz, with PN lower than -90.5 dBc/Hz at 1 MHz frequency offset across the 56 – 62 GHz range. Meanwhile, the inductor-based DCO and transformer-based DCO are implemented in a 90 nm CMOS process and consume 10 mW and 12 mW, respectively, from a supply voltage of 1.2 V.

II.3.3. Performances Summary of LC-Based DCOs

Table II.3.1 gives the performances of some typical LC-based DCOs. It can be seen that the DCOs are mainly evolving towards low power consumption, high frequency, and low phase noise. Meanwhile, depending on the application scenarios, they differ in

frequency-tuning range (FTR) and frequency resolution.

A low-power DCO typically employs a complementary cross-coupled structure driven by a low supply voltage, as in [II-16], [II-31], and [II-26]. Moreover, most DCOs operate at frequencies below 10 GHz and typically use a multi-stage switched-capacitor structure to achieve both wide FTR and high resolution, as in [II-11], [II-12], [II-32], and [II-33].

Table II.3.1 Performances summary of LC-based DCOs.

Reference	Technology	Frequency (GHz)	FTR	ΔC_{fine}	ΔF_{fine}	Phase Noise (dBc/Hz)	P_{DC} (mW)	Voltage (V)
[II-4] TMTT 2003	0.13 μm	2.4	23%	38 aF	23 kHz	-112 @500kHz	3.45	1.5
[II-34] JSSC 2005	90 nm	3.6	25%	50 aF	12 kHz	-165 @20MHz	25.2	1.4
[II-35] ISSCC 2006	65 nm	10	10%	55 aF	1.03 MHz	-102 @1MHz	3.3	1.1
[II-11] ISCAS 2007	0.18 μm	3.8	26%	21 aF	20 kHz	-123 @1.2MHz	5.04	1.8
[II-36] ASSCC 2007	90 nm	3.3	18%	10 aF	5 kHz	-118 @1MHz	2.4	1.2
[II-13] EL 2008	65 nm	5	20%	0.8 aF	1.4 kHz	-102 @1MHz	2.16	1.2
[II-12] RFIT 2009	0.18 μm	5.9	10%	28 aF	14 kHz	-117 @1MHz	9.2	1.8
[II-28] MWSYM 2009	90 nm	58 – 64	9.27%	–	1.39 GHz	-90.1 @1MHz	10.6	1.2
[II-30] JSSC 2013	90 nm	60	9.75%	50 aF	2.5 MHz	-94 @1MHz	14	1.2
[II-32] ESSCIRC 2014	65 nm	3 – 4.3	36%	60 aF	3 kHz	-149.5 @10MHz	6.5	0.5
[II-27] RWS 2017	22 nm	4	35%	20 aF	12 kHz	-122 @1MHz	2.5	1
[II-37] TCSI 2017	65 nm	54.8 – 63.2	14.2%	–	4 Hz	-94.1 @1MHz	15	1.2
[II-16] EuMIC 2018	28 nm	3.9 – 4.7	17%	–	400 kHz	-109.5 @1MHz	0.35	0.8
[II-23] CICC 2019	28 nm	2.02 – 2.87	35%	12 aF	–	-118 @1MHz	0.75	0.3
[II-38] TVLSI 2019	65 nm	24	29%	–	1.1 MHz	-106 @1MHz	12.8	1.2
[II-31] TMTT 2019	65 nm	23.7	24.4%	–	187 MHz	-106.6 @1MHz	4.8	0.45
[II-33] TSP 2020	28 nm	2.4	–	4.23 aF	8 kHz	-113 @1MHz	1.5	1
[II-39] ISCAS 2021	14 nm	14	18%	–	7 kHz	-110 @1MHz	6.3	0.8
[II-26] LMWC 2021	28 nm	24.4	27.3%	4 aF	150 kHz	-97 @1MHz	1.2	0.65

Not many K-band and mm-W DCOs have been disclosed. The multi-stage (more than 3) switched-capacitor structure can still be used in K-band DCOs, as in [II-26], [II-38]. However, it is necessary to carefully set the inductance and capacitance values of the LC tank. The aforementioned DiCAD technique is usually employed in mm-W DCOs, e.g., a multi-stage frequency-tuning structure using the DiCAD technique is applied in [II-30].

To the author's knowledge, the K-band DCO in [II-31] achieves the best PN of -106.6 dBc/Hz. However, it is a dual-band design with a minimum frequency resolution of ~187 MHz. Moreover, the mm-W DCO in [II-28] has only one frequency-tuning bank and its frequency resolution is up to ~1.39 GHz. It can be seen that none of them can meet the requirements of FMCW automotive radar.

Note that the DCO in [II-37] using a multi-stage C-2C exponentially scaling switched-capacitor ladder achieves very fine frequency resolution (several Hz), similar to the DCO in [II-39]. However, the implementation of this type of DCO is more complicated and is susceptible to various constraints, such as the scaling factor and the matching problem, thereby limiting its application.

II.4. DCOs for FMCW Radars

Most of the DCOs mentioned in the previous section are not applicable to FMCW radars, which have more stringent requirements for DCOs, requiring not only excellent phase noise performances, but also a large frequency tuning range to generate chirp signals. Therefore, before presenting the proposed DCO, we will first analyze the principle of FMCW radars for detecting stationary and moving targets, and then briefly introduce the DCO gain calibration and linearization in chirp signal generation. These details are essential to the design of the DCO and to understand its specifications.

II.4.1. Principle of FMCW Radars

As we know, unmodulated continuous-wave (CW) radar emits a constant frequency signal, which can only detect the relative velocity of a target through a Doppler shift. In order to determine the distance to the target simultaneously, frequency-modulated continuous-wave (FMCW) radar is commonly employed. In the following, we will briefly introduce the principle of FMCW radars for stationary target and moving target detections,

respectively.

II.4.1.1. Stationary Target Detection

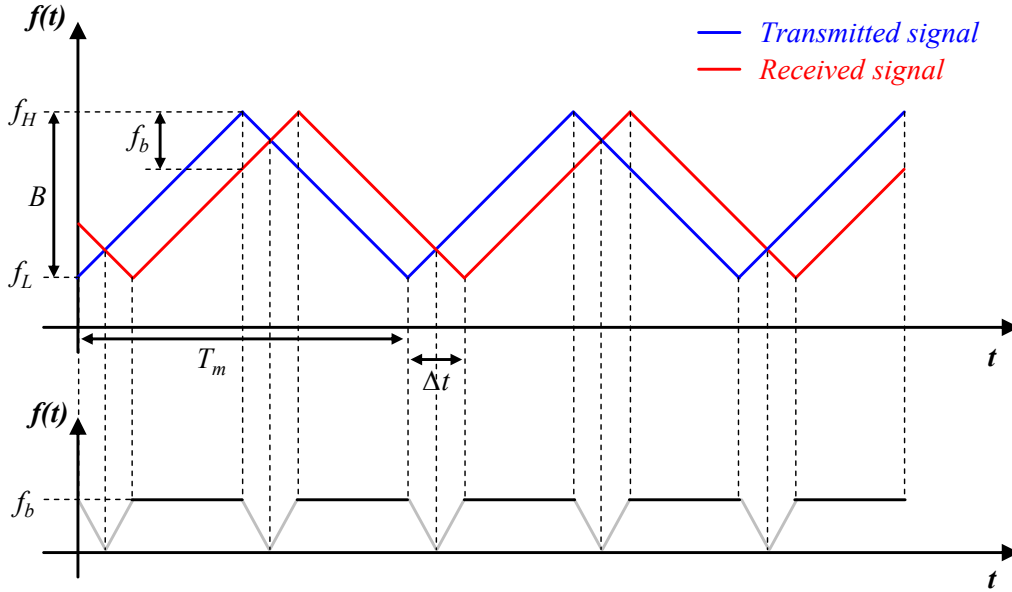


Figure II.4.1 The principle of FMCW radars with triangular modulation for detecting a stationary target and the resulting beat signal.

The principle of a FMCW radar with triangular modulation for the detection of a stationary target is depicted in Figure II.4.1. The transmitted signal $f_T(t)$ (blue line) is characterized by the lowest frequency f_L , the highest frequency f_H , the time period T_m , and the sweep bandwidth B . Thus, the correspondingly instantaneous frequency is given by

$$f_T(t) = \begin{cases} f_L + \frac{2B}{T_m}(t - nT_m) & nT_m \leq t \leq \frac{(n+1)T_m}{2} \\ f_L + \frac{2B}{T_m}(t - 2nT_m) & \frac{(n+1)T_m}{2} \leq t \leq 2nT_m \end{cases} \quad (\text{II. 4. 1})$$

where n is a positive integer. The ratio $2B/T_m$ represents the slope of the chirp and is known as the ramp rate or the sweep rate. Assuming that the received signal from a target at a distance R has a round-trip time Δt so that $\Delta t = 2R/c$, the instantaneous frequency of this received signal $f_R(t)$ (red line) can be expressed as

$$f_R(t) = \begin{cases} f_L + \frac{2B}{T_m}(t - nT_m - \Delta t) & nT_m + \Delta t \leq t \leq \frac{(n+1)T_m}{2} + \Delta t \\ f_L + \frac{2B}{T_m}(t - 2nT_m - \Delta t) & \frac{(n+1)T_m}{2} + \Delta t \leq t \leq 2nT_m + \Delta t \end{cases} \quad (\text{II. 4. 2})$$

Taking into account $\Delta t \ll T_m$, the baseband beat frequency f_b generated by the down-

conversion represents the frequency difference between the transmitted signal and the received signal and is given by

$$f_b = |f_T(t) - f_R(t)| = \frac{2B}{T_m} \cdot \Delta t = \frac{4B}{c \cdot T_m} \cdot R \quad (\text{II. 4. 3})$$

This beat frequency is proportional to the distance and is usually at the megahertz level for automotive radars. To further determine the range resolution, the limiting case of a beat signal with a duration of $T_m/2$ (chirp duration) is considered as shown in [Figure II.4.2\(a\)](#). Since the frequency of this beat signal is fixed, this signal can be further represented as a solitary rectangular pulse $x(t)$ with a pulse width $T_m/2$ and amplitude A , as shown in [Figure II.4.2\(b\)](#), which can be expressed as

$$x(t) = \begin{cases} A & -\frac{T_m}{4} \leq t \leq \frac{T_m}{4} \\ 0 & \text{otherwise} \end{cases} \quad (\text{II. 4. 4})$$

The Fourier transform or spectrum of this rectangular pulse is given by

$$|X(f)| = A\tau \cdot \text{sinc}\left(\pi \frac{T_m}{2} f\right) \quad (\text{II. 4. 5})$$

The spectrum is plotted in [Figure II.4.2\(c\)](#). Note that the first zero point occurs at the frequency of $2/T_m$ (and $-2/T_m$), which is the inverse of the pulse width $T_m/2$. Typically, the value $2/T_m$ can also be used as a rough estimation of the frequency resolution.

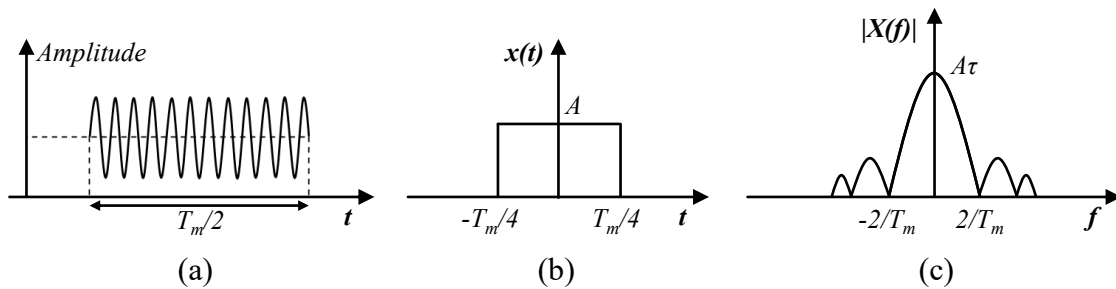


Figure II.4.2 (a) A solitary rectangular pulse and (b) its spectrum.

Therefore, for a single beat frequency pulse with a pulse width of about $T_m/2$ (up/down chirp duration), the approximate beat frequency resolution Δf_b is

$$\Delta f_b \approx \frac{2}{T_m} \quad (\text{II. 4. 6})$$

Substituting (II.4.6) into (II.4.3), the relationship between the range resolution ΔR and the chirp bandwidth B can be expressed as

$$\Delta R \approx \Delta f_b \cdot \frac{c \cdot T_m}{4B} \approx \frac{c}{2B} \quad (\text{II. 4. 7})$$

It can be seen that the chirp bandwidth limits the range resolution, and a large bandwidth provides a higher range resolution. For example, for a typical mm-W SRR with a 4 GHz bandwidth (77 – 81 GHz), a range resolution of ~ 3.75 cm can be achieved. However, in practice, the range resolution is further deteriorated due to the use of digital Fourier transform (DFT) for spectrum estimation, even though windowing techniques are applied to enhance the spectrum estimation results. For example, the range resolution is worsened by a factor of 1.8 when using the Blackman-Harris window [II-40].

II.4.1.2. Moving Target Detection

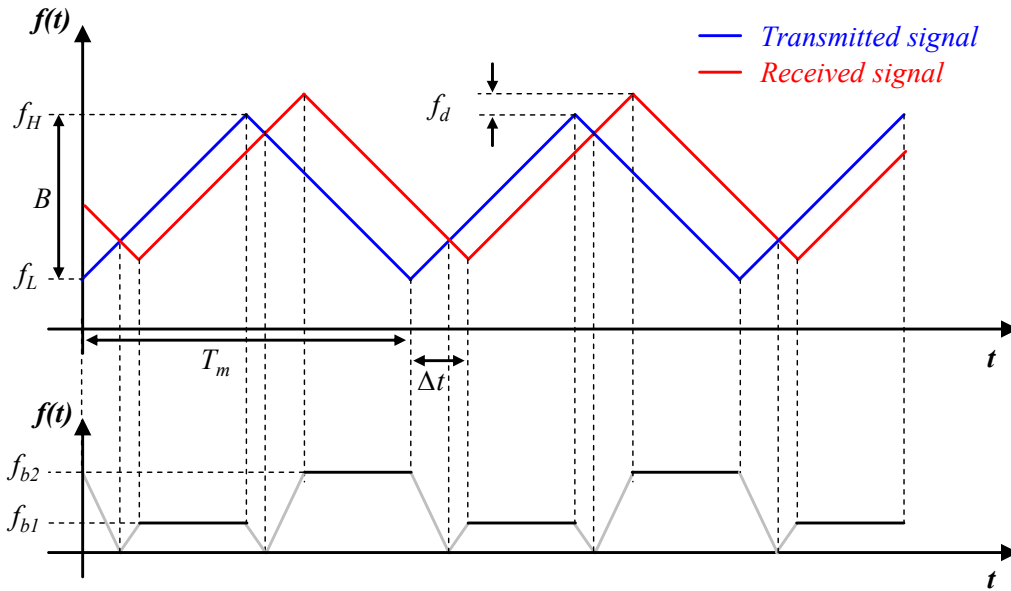


Figure II.4.3 The principle of FMCW radar with triangular modulation for detecting a moving target and the resulting beat signal.

For detecting a moving target at the identical distance R , the principle of FMCW radar with triangular modulation is shown in Figure II.4.3. The Doppler shift f_d leads to inconsistent beat frequencies of the up-chirp and down-chirp, i.e., f_{b1} and f_{b2} . Their relationship with the beat frequency f_b produced by a stationary target at a distance R is

$$f_{b1} = f_b - f_d \quad (\text{II. 4. 8})$$

$$f_{b2} = f_b + f_d \quad (\text{II. 4. 9})$$

Once beat frequencies f_{b1} and f_{b2} are determined in the baseband, the velocity v_t and the distance R can be approximated by

$$v_t \approx \frac{\lambda \cdot (f_{b2} - f_{b1})}{4} \quad (\text{II. 4. 10})$$

$$R = \frac{c \cdot T_m \cdot (f_{b1} + f_{b2})}{8B} \quad (\text{II. 4. 11})$$

where λ is the wavelength of the transmitted signal. Note that any variation in the chirp waveform will affect the accuracy and resolution of the range and velocity measurements. Consequently, a purely linear chirp is required to obtain high-performance beat frequencies in both stationary and moving target measurements.

II.4.2. DCO Gain Calibration for Chirp Linearity

For an ADPLL-based FMCW generator, the DCO tuning words (OTW) are stepped up/down on each rising edge of the modulation clock, following the triangular chirp trajectory. The accuracy of such FMCW radar depends not only on the ADPLL's phase noise and robustness to PVT variations, but also on the chirp's linearity that determines the beat frequency's quality. As we know, most DCOs are based on multi-bank structures to achieve both high frequency resolution and wide tuning range. Therefore, the wideband triangular modulation requires traversing multiple capacitor banks with different gain K_{DCO} . Consequently, in multi-bank DCOs, gain calibration and linearization techniques are critical for generating a linear chirp.

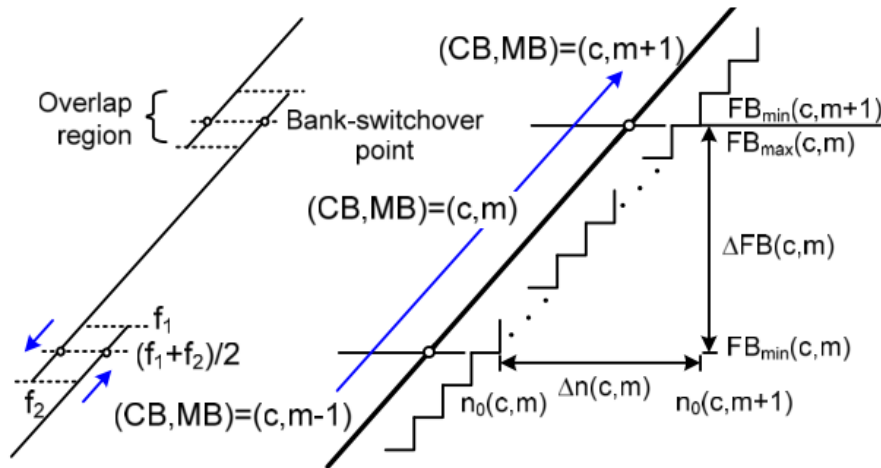


Figure II.4.4 Gain calibration and linearization technique of multi-bank DCOs.

The open-loop calibration algorithm employed in [II-41] corrects the K_{DCO} via a look-up table for individual bits in each bank. However, this algorithm leads to a long calibration time (up to hours) and an unacceptably large look-up table for a wideband chirp. Therefore, an alternative closed-loop DCO gain linearization technique was

proposed in [II-42]. Let us take it as an example to describe how a multi-bank DCO achieves a linear chirp briefly. As shown in [Figure II.4.4](#), accurate DCO tuning words (OTW) are determined only in the vicinity of the bank-switchover points instead of finding and storing accurate OTWs for each frequency point along the chirp trajectory. Therefore, the size of the look-up table is determined by the number of bank-switchover points, and the mid-point of the overlap region is chosen for a robust switchover. Meanwhile, to ensure the monotonic tuning against PVT, the whole fine-tuning range is set to 1.5 times the frequency step size of the medium-tuning bank. It is worth noting that the gains of the fine- and medium-tuning banks vary with different coarse-tuning codes due to the wide coarse-tuning range, which also leads to non-linearity. Therefore, the gains of DCOs need to be continuously calibrated in the background to make the estimation error less than 1% [II-43]. Moreover, depending on the design requirements, other digital calibration techniques for mitigating DCO non-linearity can be found in [II-44]-[II-48]. Overall, the DCO gain calibration is another complex task that we do not describe in detail here.

II.5. Design and Implementation of a K-Band Low-Phase-Noise T-DCO for 76 – 81 GHz FMCW Automotive Radars

II.5.1. Introduction

As the core frequency generation module, the DCO mainly determines the overall performances of the ADPLL. To integrate multi-range detection in a single radar, a DCO with an FTR of $\sim 10\%$ is required to cover the entire band of 76 – 81 GHz. Moreover, considering process, voltage, and temperature (PVT) variations (e.g., harsh operating temperatures from -25° to 125°), the FTR should be extended to $\sim 20\%$. In addition, a DCO with low PN and high frequency resolution is necessary to produce a high-purity linear chirp. However, in practice, the Q -factor of the mm-W passive devices is relatively low, which restricts the PN of the DCO, and the large parasitic capacitances associated with the LC tank and active devices limit the FTR. Therefore, achieving low PN and wide FTR simultaneously at mm-W frequencies has always been a great challenge.

A straightforward approach to make the DCO operate at mm-W frequencies is to

design a mm-W LC tank (e.g., at 80 GHz) as mentioned in Section II.3.2.3. Metal strips placed beneath the resonator (i.e., transmission line, inductor, or transformer) are configured by MOS switches to load the tank with more (or less) capacitance, thereby varying the DCO frequency [II-30]. However, it is hard to achieve a wide FTR of more than 10 % in this case due to the large parasitic capacitance. Another approach is to design a sub-mm-W LC tank (e.g., at 20 GHz), where mm-W frequencies can be obtained by using multipliers or higher-order harmonics [II-26], [II-49]. Thus, classical switched-capacitor structures can still be utilized to reach a wide FTR of ~20 %. However, to our knowledge, the best PN achieved using this approach at 23.7 GHz is -106.6 dBc/Hz at 1 MHz frequency offset, as presented in [II-31].

Therefore, our main objective is to explore the feasibility of implementing a K-band high-performance DCO for 76 – 81 GHz automotive radars in the advanced 22 nm FD-SOI process. Meanwhile, this DCO needs to achieve both best-in-class phase noise performances, excellent FTR, and high frequency resolution to ensure accuracy and robustness of the automotive radar.

II.5.2. K-Band DCO Design Considerations

II.5.2.1. DCO Specifications

Since the proposed DCO is intended for the FMCW automotive radar, its design needs to meet some specifications as outlined in [Table II.5.1](#). Prior to the design process, it is imperative to highlight several essential constraints that are listed as follows:

- The K-band DCO output frequency needs to completely cover the frequency band of 19 – 20.25 GHz, which is a quarter of the 76 – 81 GHz, and is mainly used to generate linear frequency-modulated (chirp) signals;
- The coarse-tuning step is about 200 MHz, and the coarse-tuning bank is dedicated to compensate for PVT variations;
- The fine-tuning step is approximately 2.5 MHz, which allows the output frequency of a FMCW radar to be swept linearly over time at this step while ensuring a low level of quantization noise;
- The chirp range is about 2.5 GHz. Compared to the actual useful chirp range of 1.25 GHz (19 – 20.25 GHz), we left a sufficient margin;
- The phase noise at 1 MHz frequency offset is about -115 dBc/Hz, which is far lower

than the phase noise of other K-band DCOs.

It is noteworthy that, to more easily cover the wide chirp range of about 2.5 GHz, we have incorporated a medium-tuning step into this design, with a value between the coarse-tuning step and the fine-tuning step. The medium-tuning bank will be used in conjunction with the fine-tuning bank to generate the chirp signal. Along with the coarse-tuning bank, they form the prototype of the triple-bank DCO (T-DCO). The most significant advantage of this prototype is that a wide FTR and ultra-fine frequency resolution can be achieved simultaneously by using fewer capacitor tuning units.

Table II.5.1 DCO Specifications.

Parameters	Minimum	Typical	Maximum	Units	Description
temperature	-25°		125°		
dvdd		0.8		V	digital DC supply for control
avdd_reg	0.85	0.9	0.95	V	analog DC output ($\pm 5\%$ depending on the performance)
ibias_prog		4		bits	step programming from the bias current mirror
icc_on			60	mA	consumption of DCO and its buffer (no load)
icc_off			1	mA	leakage (power off mode)
frequency	19		20.25	GHz	
supply voltage		1		V	depending on the life-time of the MOS components
coarse step		200		MHz	indicative coarse step
fine step		2.5		MHz	
chirp range		2.5		GHz	
phase noise		-115		dBc/Hz	frequency offset – 1 MHz
		-135		dBc/Hz	frequency offset – 10 MHz
		-155		dBc/Hz	frequency offset – 100 MHz
Ton		50		ns	settling time (to 95 % of the final vdd_dco)

II.5.2.2. Selection of DCO Structures

Among the different structures of DCOs reported in recent years, LC resonator-based cross-coupled DCOs are preferable due to their low PN, low power consumption, simplicity, and robustness. As mentioned in Section I.3.2.3, since the electron mobility is much higher than that of holes, the NMOS-only structure can provide a higher transconductance compared to the PMOS-only structure, which implies a smaller size cross-coupled pair and less parasitic capacitance. The complementary structure offers low PN and low power consumption. However, introducing an extra transistor between the

supply voltage and ground makes it unsuitable for low supply voltage applications in advanced process nodes. Therefore, only NMOS-only structures will be considered in this design. Three of these representative structures are shown in [Figure II.5.1](#).

[Figure II.5.1\(a\)](#) shows the structure of a class-B cross-coupled oscillator, which is one of the most famous and widely used topologies. When the oscillation amplitude is small, the oscillator operates in the current-limited region, where the oscillation amplitude is proportional to the tail current. As the tail current keeps increasing, the oscillation amplitude continues to increase gradually until it remains constant, i.e., entering the voltage-limited region [II-50]. Since the single-side transistor of the cross-coupled pair conducts in about half a cycle, which means that its conduction angle is 180° , this type of oscillator is called the class-B oscillator.

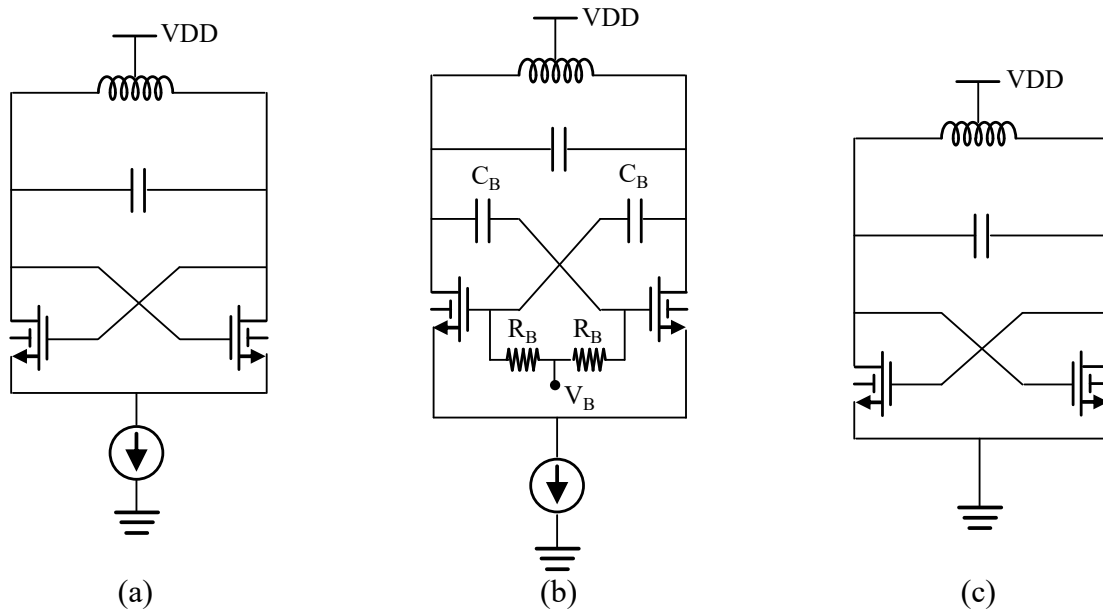


Figure II.5.1 Commonly used NMOS-only structures of cross-coupled LC DCO. (a) Class-B structure. (b) Class-C structure. (c) Class-D structure.

[Figure II.5.1\(b\)](#) shows the structure of a class-C cross-coupled oscillator. Compared with the class-B oscillator, the gates of its cross-coupled pair are no longer biased to VDD, but at a lower bias voltage V_B , and the output signal is coupled through capacitor C_B . Therefore, the class-C structure prevents the cross-coupled pair from entering the deep triode region by controlling the V_B (reducing the overdrive voltage), thus improving the PN performances. Since the conduction time of a single-side transistor is less than half a cycle, i.e., the conduction angle is less than 180° , this type of oscillation is referred to as

the class-C oscillator. However, it suffers from the trade-off between maximum oscillation amplitude and start-up robustness [II-51].

Figure II.5.1(c) shows the structure of a class-D cross-coupled oscillator, which eliminates the tail current source, thus avoiding its noise from entering the resonant tank through the cross-coupled pair. Moreover, this structure allows a much higher oscillation amplitude ($\sim 2 \cdot V_{DD}$) than the previous two structures, resulting in better phase noise performances. In addition, the differential transistors are used as switches, since the product of the drain voltage and the channel current of the switches is very close to zero during the whole oscillation period, all the power dissipation occurs in the LC tank, leading to excellent power efficiency. Based on these characteristics, this type of oscillator is known as the class-D oscillator. However, the current consumption of a class-D oscillator depends on the VDD and the losses of the LC tank, thus this approach generally features higher power consumption. Furthermore, it is highly sensitive to the supply voltage and therefore requires a high-performance regulator [II-52].

Consequently, we chose the class-B cross-coupled oscillator architecture shown in Figure II.5.1(a) as the K-band DCO architecture.

II.5.2.3. K-Band LC Tank Design Considerations

As we know that the resonant frequency of the parallel LC tank is approximately $f = 1/(2\pi\sqrt{LC})$, where L and C are the total inductance and total capacitance, respectively. Therefore, the relationship between the frequency-tuning step Δf and the capacitance-tuning step ΔC can be estimated as

$$\Delta f = -2\pi^2 f^3 L \Delta C \quad (\text{II. 5. 1})$$

Therefore, for an oscillation frequency of 20 GHz and a typical inductance of 140 pH, a ΔC of only ~ 100 aF is required to achieve a fine frequency resolution of ~ 2.5 MHz, which is the first challenge of the K-band LC tank design, i.e., achieving a tiny capacitance-tuning step. In addition, the FTR of a DCO can be expressed as

$$FTR = 2(f_{max} - f_{min})/(f_{max} + f_{min}) = 2 \frac{\sqrt{C_{max} + C_p} - \sqrt{C_{min} + C_p}}{\sqrt{C_{max} + C_p} + \sqrt{C_{min} + C_p}} \quad (\text{II. 5. 2})$$

where f_{max} and f_{min} are the maximum and minimum oscillation frequencies of the DCO, C_{max} and C_{min} are the maximum and minimum capacitances of LC tank, C_p represents the whole parasitic capacitance. For instance, to achieve an FTR of ~ 20 %, assuming an

oscillation frequency of 18 – 22 GHz (4 GHz bandwidth) and with a constant inductance of 140 pH, C_{max} and C_{min} can be estimated to be 560 fF and 375 fF, respectively, which means a capacitance ratio C_{max}/C_{min} of ~ 1.5 . Considering the contribution of C_p to the total capacitance, this ratio needs to be larger, which is the second challenge in the K-band LC tank design.

Note that inductance values for wide-FTR DCO designs generally do not exceed 200 pH since sufficient margin needs to be reserved for the total capacitance (>300 fF). Meanwhile, according to the Equation (II. 5.1), if the inductance L increases, ΔC must be further reduced for the same Δf . Figure II.5.2 shows some simulation results for several typical inductance values of center-tap inductors and their Q -factors at 20 GHz in GlobalFoundries' (GF) 22 nm FD-SOI process. Inductors between 100 – 150 pH exhibit a good Q -factor of ~ 22 . In general, the MOS varactor structure shown in Figure II.5.3(a), which is often used in sub-10 GHz DCO designs, offers a much higher Q -factor (>100) than the inductor. Therefore, according to the Equation (I.3.4), the Q -factor of the final LC tank depends mainly on that of the inductor.

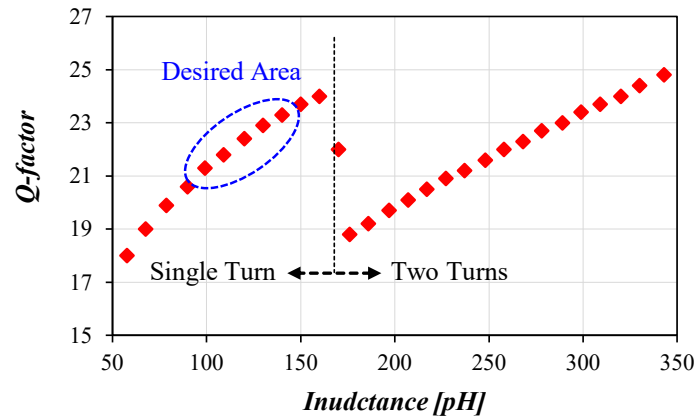


Figure II.5.2 Typical inductance and Q -factor of a center-tapped inductor at 20 GHz implemented in the GF' 22 nm FD-SOI process.

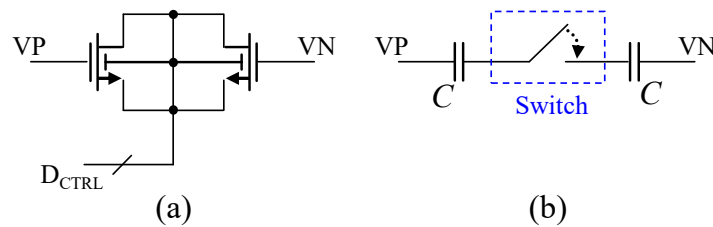


Figure II.5.3 (a) MOS varactor structure commonly used for sub-10 GHz DCOs. (b) Simplified switched-capacitor structure adapted to K-band DCOs.

However, for K-band DCO designs, this is no longer applicable because the Q -factor of the MOS varactor tends to be close to or slightly higher than that of the inductor. Furthermore, the Q -factor of the MOS varactor is even lower in the FD-SOI process due to the presence of the buried oxide layer. For example, the simulated minimum capacitance step of the smallest size NMOS varactor is ~ 1.4 fF with a worst Q -factor (inversion mode) of ~ 20 at 20 GHz in the 22 nm FD-SOI process. Although the switched-capacitor structure with a better Q -factor in [Figure II.5.3\(b\)](#) is proposed, it endures the trade-off between Q -factor and parasitic capacitances, which is the third challenge in the K-band LC tank design.

II.5.2.4. Low Phase Noise Considerations

Let us remind the well-known Leeson's formula in the Equation (I.3.24), which can also be applied to the PN analysis of LC-DCOs and is given in [II-53]. One can conclude that the PN of DCOs can be boosted by increasing the dissipated power and improving the Q -factor of the LC tank.

More dissipated power implies a higher tail current, since, in the current-limited region, the output voltage swing is proportional to the tail current. Consequently, the conduction time of the transistors of the cross-coupled pair can be reduced accordingly, resulting in a minimization of cyclostationnary noise sources contribution to the overall PN. Furthermore, as the tail current still increases, the oscillator eventually enters the voltage-limited region, i.e., the amplitude no longer increases [II-50]. Therefore, the best PN performances of the DCO can be obtained at the edge of the current-limited and voltage-limited regions.

As mentioned above, the inductor of the K-band DCO has a relatively constant Q -factor at 20 GHz, so the Q -factor of the LC tank is highly dependent on that of the capacitors. Since the Q -factor of the LC tank directly affects the PN and power consumption of the DCO, the switched-capacitor structure needs to be optimized in order to achieve the best Q -factor with acceptable parasitic capacitances. Meanwhile, the back-gate bias provided by the 22nm FD-SOI process will be used in the design of the MOS switch to further improve its Q -factor, and this point will be discussed in detail in the following Section.

In addition, unlike the conventional VCOs, the DCOs exhibit a quantization noise introduced by its finite frequency resolution Δf_{res} , whose contribution to phase noise is

given by

$$L\{\Delta f\} = \frac{1}{12f_R} \cdot \left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \cdot \text{sinc}\left(\frac{\Delta f}{f_R}\right)^2 \quad (\text{II. 5. 3})$$

where f_R and Δf are the reference frequency and the offset frequency, respectively. Therefore, in order to reach an ultra-fine frequency resolution (several kHz) or a fractional input, two additional fine-tuning units are connected to a digital high-speed $\Sigma\Delta$ modulator to perform the dithering [II-54].

II.5.3. Circuit Implementation of the Proposed T-DCO

II.5.3.1. Block Diagram of the K-Band T-DCO

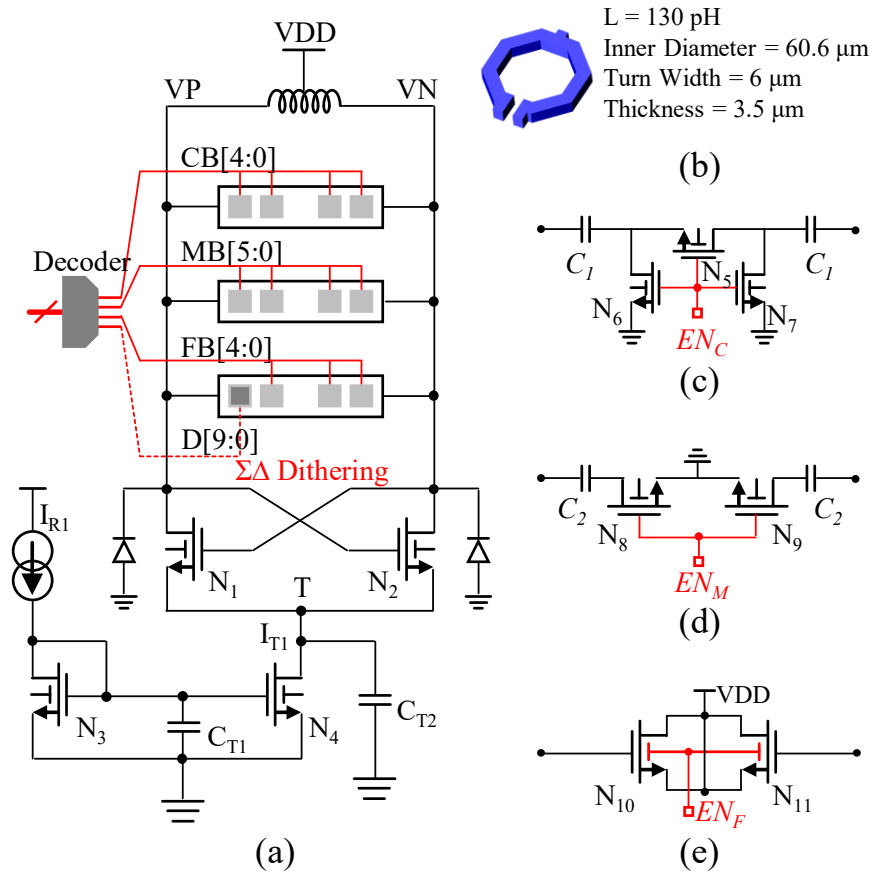


Figure II.5.4 (a) Block diagram of the proposed T-DCO. (b) Center-tapped inductor and its main parameters. (c) Schematic of the coarse-tuning unit. (d) Schematic of the medium-tuning unit. (e) Schematic of the fine-tuning unit.

The simplified block diagram and main parameters of the proposed T-DCO are illustrated in Figure II.5.4 and Table II.5.2, respectively. The single-turn center-tapped

inductor of 130 pH is implemented using the tenth layer of thick metal with a width of 6 μm , as shown in Figure II.5.4(b). It achieves a Q-factor of about 22 at 20 GHz. The oscillation frequency adjustment is carried out by three parallel capacitor banks: the coarse-tuning bank, the medium-tuning bank, and the fine-tuning bank.

Table II.5.2 Main parameters of the proposed T-DCO.

VDD	I _{R1}	N _{1,2}	N ₃	N ₄	N ₅₋₇
1.2 V	2 mA	40 $\mu\text{m}/100\text{ nm}$	400 $\mu\text{m}/1\text{ }\mu\text{m}$	4000 $\mu\text{m}/1\text{ }\mu\text{m}$	12 $\mu\text{m}/20\text{ nm}$
N _{8,9}	N _{10,11}	C ₁	C ₂	C _{T1}	C _{T2}
16 $\mu\text{m}/20\text{ nm}$	2.4 $\mu\text{m}/70\text{ nm}$	15.97 fF	6.53 fF	16.8 pF	12.2 pF

Two NMOS transistors (N_{1,2}) form a differential cross-coupled pair with a negative transconductance $-g_m/2$ to compensate for the losses caused by the parallel resistance R_P of the LC tank. As shown in Figure II.5.5, a minimum $R_P \approx 240\text{ }\Omega$ arises at the lowest resonant frequency of 20.1 GHz. In addition, N₁ and N₂ are thick oxide devices with a channel length of 100 nm, targeting to compensate for the lifetime degradation caused mainly by the hot carrier injection (HCI) effect, particularly for large voltage swing cases. Furthermore, two diodes placed underneath the gates of N₁ and N₂ are employed to protect their thin gate dielectrics from the antenna effect during chip manufacturing and to avoid mismatch problems.

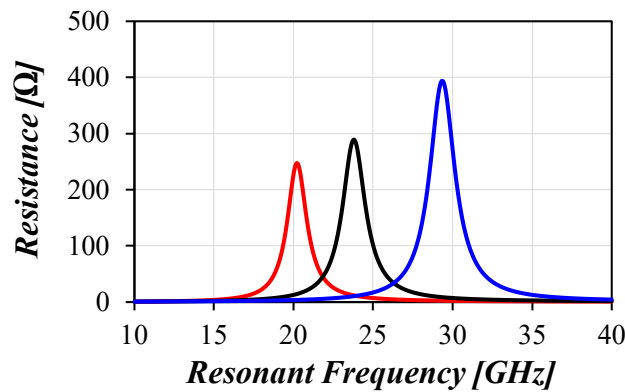


Figure II.5.5 Real part of the impedance versus the resonant frequency of the LC tank.

The current mirror (N_{3,4}) is well biased in the saturation region to provide a stable tail current and drive the output voltage swing. Moreover, two additional large tail capacitors (C_{T1} and C_{T2}) connected in parallel with the tail current source act as a filter, providing a path for the high-order harmonics at the common source node T and filtering out the thermal noise from the tail current mirror.

II.5.3.2. Parasitic Analysis of MOS Switches

In RF circuits, the parasitic capacitances of MOS transistors play an important role in circuit performances. Before analyzing the switched-capacitor structure, we first need to introduce the parasitic capacitance distribution of MOS transistors.

Figure II.5.6(a) shows the pre-simulation parasitic model of the MOS transistor in 22FDX technology [II-55]. Because of the overlap between the gate and drain/source regions, when the gate voltage V_{gs} is applied, the charge accumulates in this overlap region, forming the gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs} , which are the main parasitic capacitances of FD-SOI devices. In addition, parasitic capacitances are formed between the gate/drain/source and the substrate of the transistor, which are C_{gb} , C_{db} , and C_{sb} , respectively, and these values are significantly reduced due to the presence of the buried oxide layer in FD-SOI devices. Hence, C_{db} and C_{sb} can be combined through the substrate to form the so-called drain-source capacitance C_{ds} . Detailed definitions of these parasitic capacitances and resistances are given in Figure II.5.6(b), where the definition of the vias and metal layers in the metal stack can be found in Figure II.1.3.

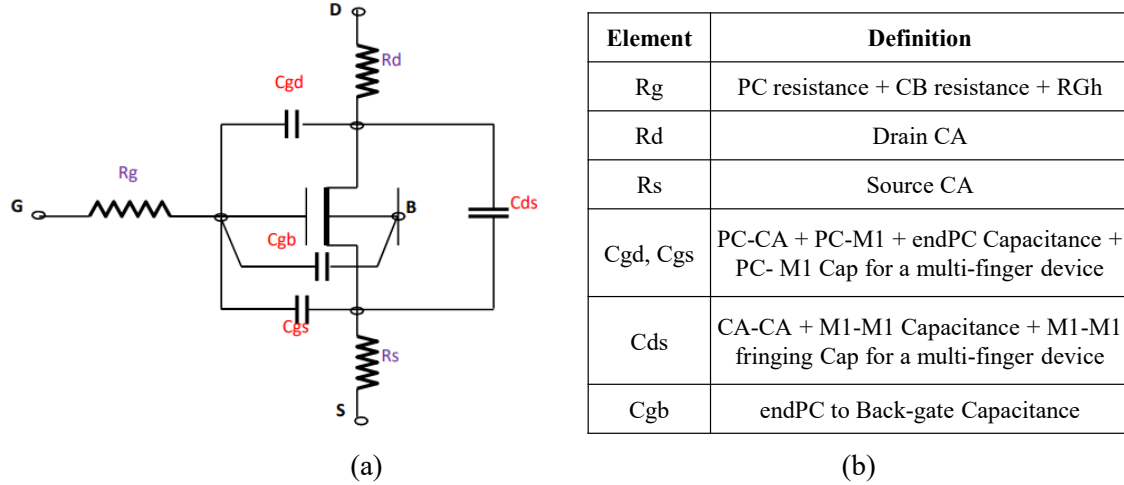


Figure II.5.6 (a) Pre-layout parasitic model and (b) instance settings for transistors in 22FDX technology.

Figure II.5.7(a) shows more visually the parasitic distribution in a flipped well NMOS with M1 metal layer. Its equivalent circuit model is shown in Figure II.5.7(b), and the corresponding labels of the circuit components are given in Figure II.5.7(c). For a MOS switch, we are interested in the three wiring capacitances, C_{wiregs} , C_{wiregd} , and C_{wireds} , which include the previously mentioned C_{gs} , C_{gd} , and C_{ds} . More specifically, the C_{wiregd}

and C_{wiregs} include PC-CA, M1-PC, M1-CA, and CA-CA capacitances between the gate and the source/drain regions. M1-M1 parasitic capacitances will be extracted by PEX (Parasitic Extraction). C_{wireds} include CA-CA, M1-M1 capacitances, and fringing capacitances between M1-M1 in multi-finger devices [II-56].

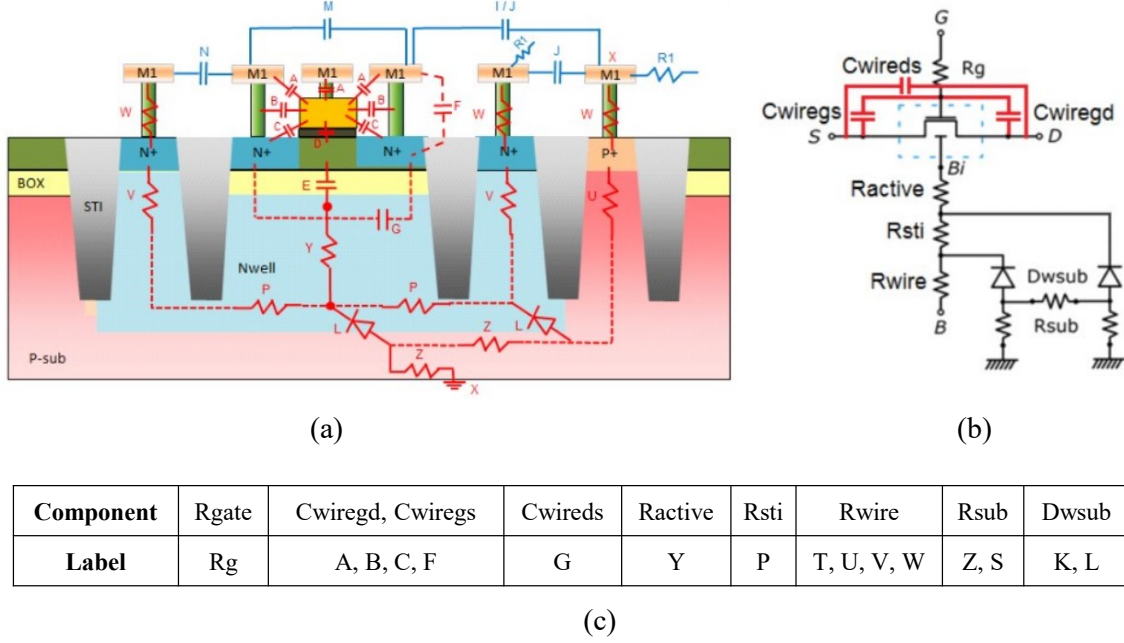


Figure II.5.7 NMOS in N-well (flipped well) with M1 reference plane: (a) cross-section view, (b) RF sub-circuit, (c) corresponding labels of the components.

Moreover, the analysis of MOS switches needs to consider the operation region of MOS transistors, whose parasitic capacitances are different under different operation regions. The 22FDX technical paper does not disclose some relevant theoretical basis. However, considering that the parasitic capacitance distribution in a planar FD-SOI process is similar to that of a conventional bulk CMOS process, we will use the latter for our analysis. Taking Figure II.5.6(a) as an example, we will mainly analyze the relationship between C_{gs} , C_{gd} , and C_{gb} . C_{ds} is regarded as a process-related independent capacitance, which is less affected by the gate voltage and will not be discussed.

The parasitic capacitances of MOS transistors for different operation regions are given in Table II.5.3. When the MOS transistor is in the cutoff region, i.e., $V_{gs} < V_{th}$, C_{gs} is the same as C_{gd} and is about $C_{ox}L_DW$, where C_{ox} is the oxide's dielectric constant, L_D is the gate-drain/source overlap length, W is the width of the channel. In addition, C_{gb} is approximately $C_{ox}LW$, which can be seen as proportional to the effective length L and width of the channel. When the MOS transistor is in the linear triode region ($V_{gs} > V_{th}$,

$V_{ds} < V_{gs} - V_{th}$), the capacitance value C_{gb} is assigned symmetrically to the source and drain. When the MOS transistor is in the saturation region ($V_{gs} > V_{th}$, $V_{ds} \geq V_{gs} - V_{th}$), most of C_{gb} is added to C_{gs} , and C_{gd} becomes $C_{ox}L_DW$ again [II-57].

Table II.5.3 Parasitic capacitances of MOS transistors.

Operation Region	C_{gs}	C_{gd}	C_{gb}
Cutoff	$C_{ox}L_DW$	$C_{ox}L_DW$	$C_{ox}LW$
Triode	$C_{ox}L_DW + C_{ox}LW/2$	$C_{ox}L_DW + C_{ox}LW/2$	0
Saturation	$C_{ox}L_DW + 2C_{ox}LW/3$	$C_{ox}L_DW$	0

II.5.3.3. 5-Bit Coarse-Tuning Bank

The 5-bit (CB[4:0]) coarse-tuning bank employs a 5-31 binary-to-thermometer decoder to control 31 coarse-tuning units to compensate for PVT variations. As shown in Figure II.5.8, we take a more concise 3-7 binary-to-thermometer decoder as an example to explain its decoding and control mechanism. This decoder consists of 3 inputs (B0 - B2) and 7 outputs (T0 - T6), where the input value and the corresponding output value are identical in decimal representation, so that a large number of outputs can be represented with a small number of inputs. In addition, the thermometer code provides a more efficient representation of numbers, as can be seen from the truth table, where the number of '1' is incremented, meaning that it allows to monotonically turn the coarse-tuning units on or off.

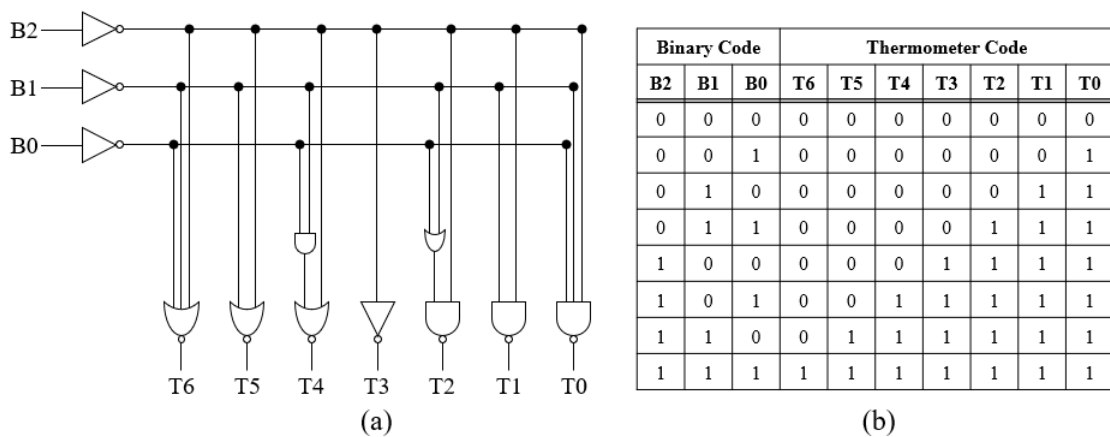


Figure II.5.8 (a) Typical schematic and (b) truth table of a 3-input 7-output binary-to-thermometer decoder.

As shown in Figure II.5.4(c), each coarse-tuning unit contains two identical APMOM

(alternative-polarization metal-oxide-metal) capacitors ($C_I = 15.97$ fF) and three thin-oxide NMOS switches (N_{5-7}) connected via the gates. When the control voltage EN_C is 0 V, the switches are in the OFF-state ($V_{gs} < V_{th}$). The equivalent schematic is depicted in [Figure II.5.9\(a\)](#). C_{ds} , C_{gd} , and C_{gs} represent the drain-source, gate-drain, and gate-source parasitic capacitances, respectively.

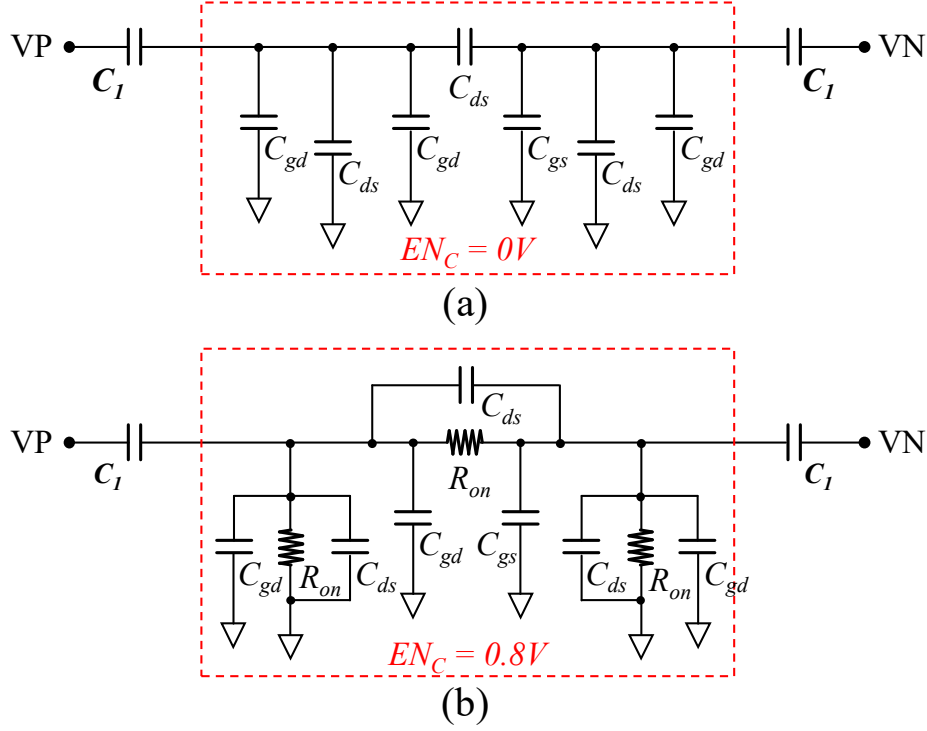


Figure II.5.9 Equivalent schematic of the coarse-tuning unit: (a) in the OFF-state, (b) in the ON-state.

Since the switches operate in the cutoff region, hence, $C_{gd} = C_{gs}$. Therefore, the total differential parasitic capacitance of these switches, C_{par} , highlighted by the red dashed box, can be expressed as:

$$C_{par} = \frac{3}{2} \cdot C_{ds} + C_{gd} \quad (\text{II. 5. 4})$$

The total differential capacitance in the OFF-state, C_{OFF_CB} , which consists of two capacitances C_I in series with C_{par} , can be estimated as follows:

$$C_{OFF_CB} \approx \frac{C_I \times C_{par}}{C_I + 2C_{par}} = \frac{1}{2} \cdot \frac{C_I \times (3C_{ds} + 2C_{gd})}{C_I + (3C_{ds} + 2C_{gd})} \quad (\text{II. 5. 5})$$

Moreover, the equivalent schematic in the ON-state is shown in [Figure II.5.9\(b\)](#). Since the switches operate in the triode region, they can be equated as resistors. More

specifically, R_{ON} can be used to represent the ON-state resistance between the drain and source of each switch. Considering that $R_{ON} \approx 0 \Omega$, then the parasitic capacitances are shorted, and the expression for the ON-state capacitance, C_{ON_CB} , can be formulated as follow:

$$C_{ON_CB} \approx \frac{1}{2} \cdot C_1 \quad (\text{II. 5. 6})$$

Therefore, the coarse capacitance step ΔC_{CB} representing the difference between the ON-state capacitance C_{ON_CB} and the OFF-state capacitance C_{OFF_CB} is given by:

$$\Delta C_{CB} = \frac{C_1}{2} - \frac{C_1 \times C_{par}}{C_1 + 2C_{par}} = \frac{C_1^2}{2(C_1 + 2C_{par})} = \frac{1}{2} \cdot \frac{C_1^2}{C_1 + 3C_{ds} + 2C_{gd}} \quad (\text{II. 5. 7})$$

Since $C_1 \gg C_{par}$, a large capacitance step ΔC_{CB} can be obtained. In addition, the ON-state parasitic resistance (R_{ON}) significantly degrades the Q -factor of the coarse-tuning unit ($Q = 1/2\pi f R_S C_S$, C_S is the equivalent series capacitance, R_S is the equivalent series resistance, and $R_S \propto R_{ON}$). Thus, to reduce R_{ON} , a higher W/L ratio of MOS switches is required at the cost of larger OFF-state capacitance.

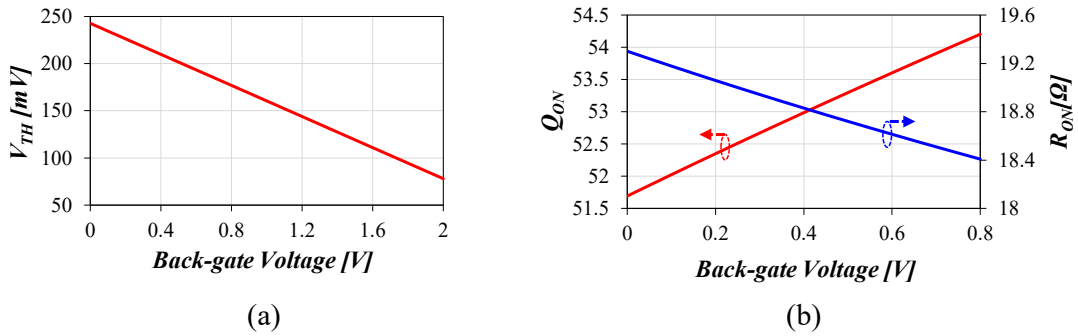


Figure II.5.10 (a) Threshold voltage V_{TH} of N_{5-7} versus back-gate voltage. (b) Q_{ON} and R_{ON} of the coarse-tuning unit versus back-gate voltage.

Furthermore, as shown in Figure II.5.10, the back-gate bias voltage of MOS switches can reduce the depletion region to lower their threshold voltage V_{TH} , leading to an improvement in the conductivity or a drop in the on-resistance R_{ON} . Consequently, the Q -factor of the capacitor bank can be further increased for a better PN. Note that the back-gate voltage allowed by this process can reach 2 V. However, since MOS switches have already employed super-low threshold voltage devices with better performances, a too high back-gate bias voltage would cause the MOS switches to fail to turn off completely when the gate voltage is 0 V, resulting in a deterioration of Q_{OFF} . Therefore, a nominal

voltage of 0.8 V is finally chosen as the forward back-gate voltage. In addition, the pre-layout simulation results show that the coarse-tuning unit achieves a capacitance ratio C_{ON_CB}/C_{OFF_CB} of 7.97 fF/2.97 fF and a Q -factor ratio Q_{ON_CB}/Q_{OFF_CB} of 54.2/84.7. Thus, the 5-bit coarse-tuning bank allows to cover a frequency range of 18.45 – 21.12 GHz (post-layout simulations), leading to an average coarse frequency resolution of 86 MHz.

II.5.3.4. 6-Bit Medium-Tuning Bank

To ensure the monotonicity of the frequency chirp, the whole frequency range of 19 – 20.25 GHz, equaling a quarter of 76 – 81 GHz, should mainly rely on the medium-tuning bank as the fine-tuning bank has a very narrow FTR. Considering the trade-off between the frequency range and the frequency resolution, a 6-bit (MB[5:0]) medium-tuning bank is thermometer decoded to sweep the 63 medium-tuning units. Moreover, to avoid the large interconnect parasitic capacitances caused by the large area of the medium-tuning bank, a more compact structure with only two NMOS switches ($N_{8,9}$) is employed, as shown in Figure II.5.4(d).

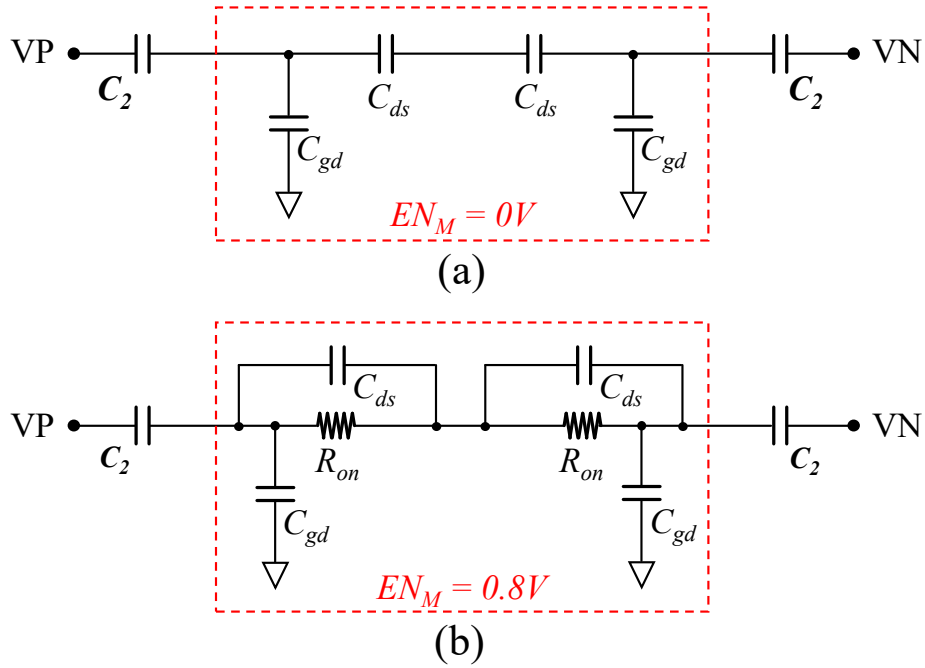


Figure II.5.11 Equivalent schematic of the medium-tuning unit: (a) in the OFF-state, (b) in the ON-state

The equivalent schematic of the medium-tuning unit is depicted Figure II.5.11, and the corresponding ON-state and OFF-state capacitances can be expressed as follows:

$$C_{OFF_MB} = \frac{1}{2} \cdot \frac{C_2 \times (C_{ds} + C_{gd})}{C_2 + (C_{ds} + C_{gd})} \quad (\text{II. 5. 8})$$

$$C_{ON_MB} \approx \frac{1}{2} \cdot C_2 \quad (\text{II. 5. 9})$$

Thus, the medium capacitance step ΔC_{MB} can be given by

$$\Delta C_{MB} = \frac{1}{2} \cdot \frac{C_2^2}{C_2 + C_{ds} + C_{gd}} \quad (\text{II. 5. 10})$$

Owing to the employed small MOM capacitors ($C_2 = 6.53$ fF) and the back-gate bias voltage of 0.8 V, the pre-layout simulation results show that the medium-tuning unit achieves a capacitance ratio of 3.21 fF/1.53 fF and a Q -factor ratio of 55.8/73.6. Furthermore, the post-layout simulation results show that this 6-bit coarse-tuning bank allows to cover a frequency range of 18.77 – 20.61 GHz, resulting in an average medium frequency resolution of 29.2 MHz.

II.5.3.5. 5-Bit Novel Back-Gate-Based Fine-Tuning Bank

As described in Section II.5.2.3, a high capacitance resolution of tens of attofarads is required to achieve a fine frequency resolution of ~ 2 MHz for the purpose of low quantization noise. Therefore, we propose a novel back-gate-based fine-tuning bank, as shown in [Figure II.5.4\(e\)](#). The drain and source nodes of the two MOS switches ($N_{10,11}$) are connected to the supply voltage (VDD) to make them operate in the depletion region, providing lower capacitance and better Q -factor. The control signal EN_F is applied to their back-gates. Note that the back-gate technique is often used to flexibly control the threshold voltage and thus improve the performances and energy efficiency of the circuit. Here, it is used for the first time in a frequency-tuning unit of a DCO. Meanwhile, we note that the back-gate structure was also applied to the frequency regulation of a VCO, and its role is equivalent to that of a varactor [II-58]. To be precise, the functions of the back-gate structure are similar in both the VCO and the DCO.

The cross-section view is illustrated in [Figure II.5.12](#). The substrate ring of $N_{10,11}$ isolates the back-gate deep-N well to make this structure more stable. Another advantage is that the back gate allows a higher breakdown voltage (i.e., up to 2 V in a 22 nm FD-SOI process) compared to the front gate. As shown in [Figure II.5.13](#), varying the EN_F from 0 V to 1.2 V allows a small capacitance step of about 63 aF. Meanwhile, since the total capacitance of the fine-tuning bank is much smaller than that of the coarse- and

medium-tuning banks, thus the poor Q -factor (~ 26) of the fine-tuning bank has a negligible influence on the total Q -factor of the LC tank.

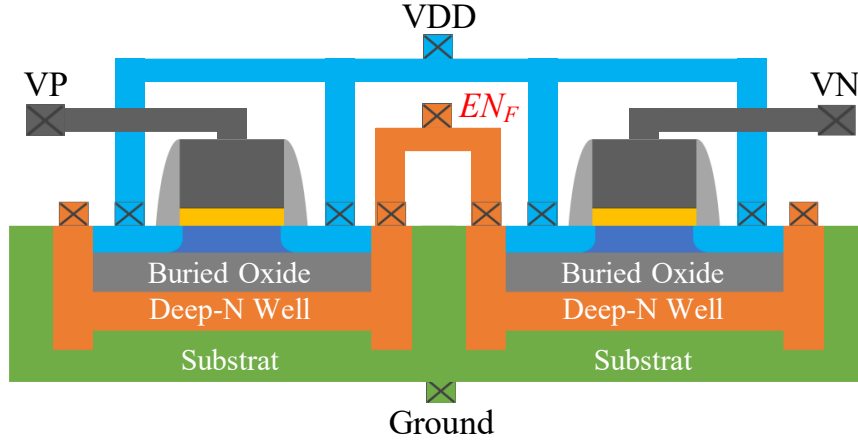


Figure II.5.12 Cross-section view of the novel fine-tuning unit.

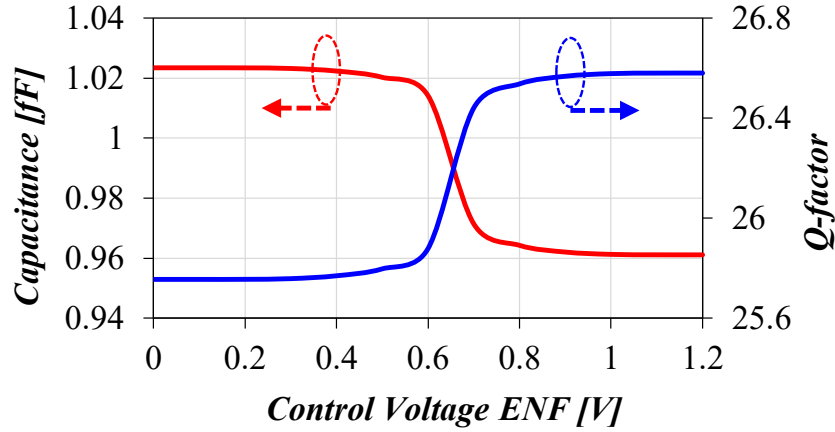


Figure II.5.13 Capacitance and Q -factor of the proposed fine-tuning unit versus control voltage EN_F .

II.5.4. Pre-Layout Simulation Results

II.5.4.1. PN Optimization

Figure II.5.14 shows the output waveforms of the proposed T-DCO for tail currents (I_{T1}) of 5 mA and 20 mA, respectively. The initial condition is set to zero, i.e., the DCO only utilizes its noise to start, and the simulation step is 1 ps. It can be seen that the T-DCO can oscillate and reach stability in a very short time (< 2 ns) thanks to the large gain provided by the cross-coupled structure. Meanwhile, the output voltage swing can be increased from ~ 0.9 V to ~ 2 V by changing the tail current from 5 mA to 20 mA, i.e., into

the voltage-limited region mentioned in Section II.5.2.4. Note that 20 mA is not the maximum current value that this current mirror structure can offer, and a current margin of ~ 5 mA is reserved for flexible compensation of PVT variations.

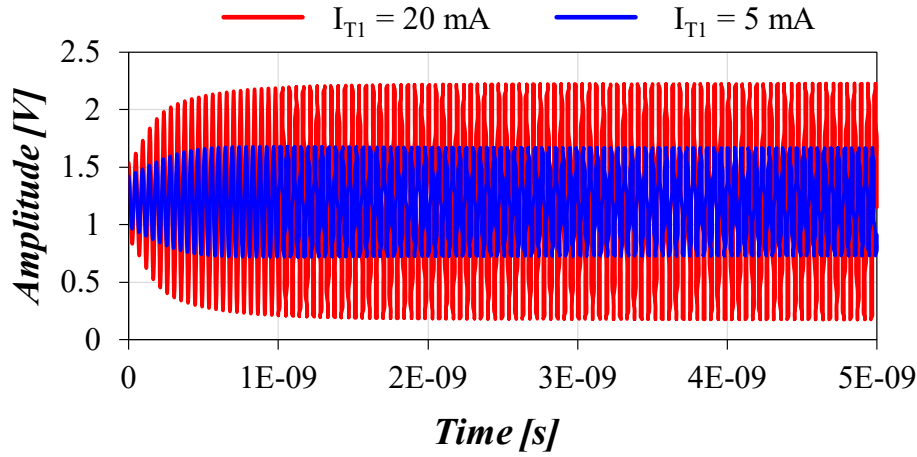


Figure II.5.14 Output waveforms for tail currents (I_{T1}) of 5 mA and 20 mA, respectively.

Figure II.5.15 illustrates the drain-source current waveforms on one side of the cross-coupled pair after the T-DCO reaches the steady state. It can be seen that there is a large spike in the waveform when the tail current is 20 mA, which means that the transistor on the other side is completely off, and almost no noise is introduced. In contrast, when the tail current is 5 mA, the cross-coupled pair is conducting most of the time, thus continuously injecting noise into the resonant tank.

Figure II.5.16 illustrates the PN performances of this T-DCO. At a carrier frequency of about 21.5 GHz, the PN at 1 MHz frequency offset can be boosted from -107.4 dBc/Hz to -111.4 dBc/Hz (i.e., an improvement of 4 dB) when the tail current is increased from 5 mA to 20 mA. Meanwhile, simulation results also show that the PN performances (at 1 MHz frequency offset) at the maximum frequency of 26.4 GHz and the minimum frequency of 19 GHz are also improved by 2.5 dB and 4.6 dB, respectively.

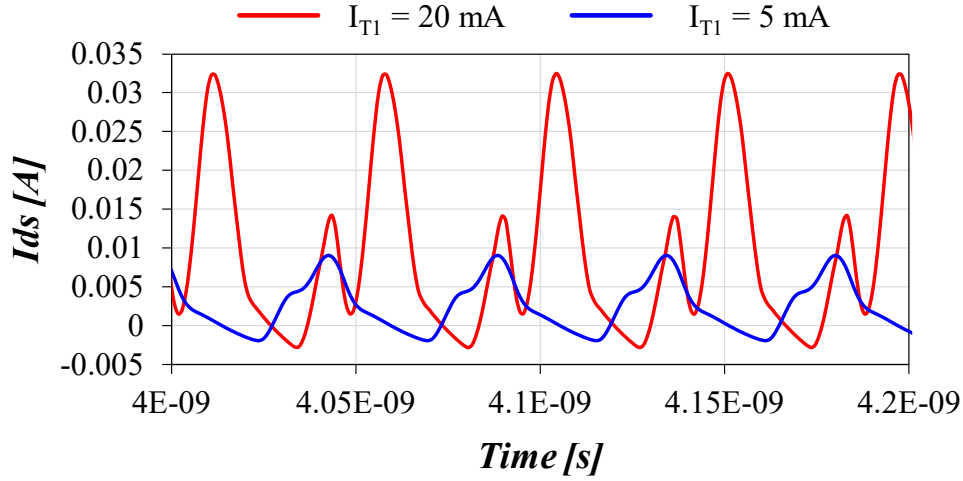


Figure II.5.15 Drain-source current (I_{ds}) waveforms of $N_{1,2}$ for tail currents (I_{T1}) of 5 mA and 20 mA, respectively.

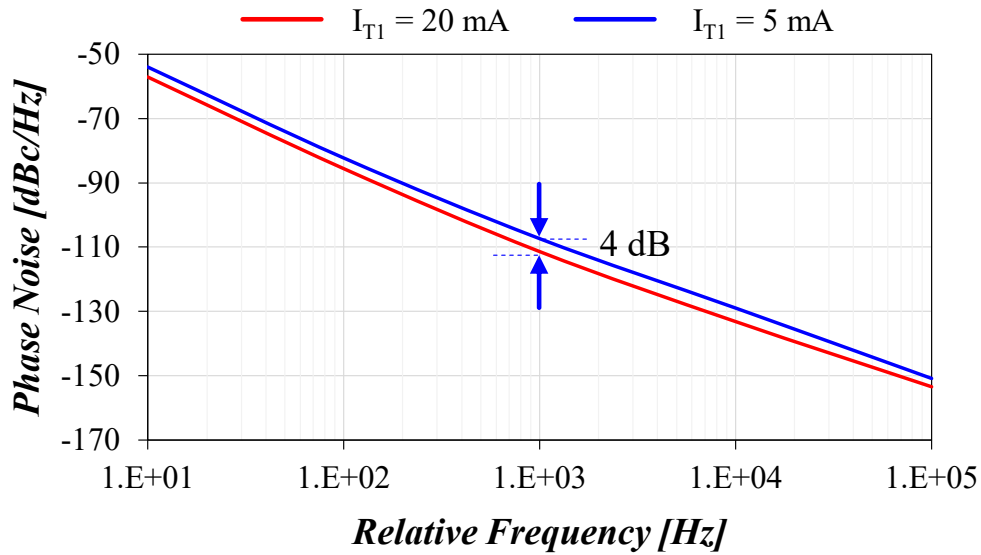


Figure II.5.16 PN performances of the T-DCO for tail currents (I_{T1}) of 5 mA and 20 mA, respectively.

II.5.4.2. FMCW Chirp with Frequency Overlap

It is worth noting that the T-DCO combines both the medium-tuning bank and the fine-tuning bank to produce a wide FTR and high-resolution FMCW chirp, which requires the medium frequency resolution (Δf_{MB}) to be smaller than the fine-tuning range (BW_{FB}) to avoid frequency modulation gaps.

Figure II.5.17 shows the partial frequency-code characteristic curves of the medium-tuning bank and the fine-tuning bank when the coarse-tuning code is 16 ($CB = 16$). When

the medium-tuning code (MB) increases by 1, the oscillation frequency drops by about 45 MHz, which is approximately the medium frequency resolution. Moreover, when the fine-tuning code (FB) is varying from 1 to 31, a fine frequency resolution of ~ 1.8 MHz and a fine-tuning range of ~ 55 MHz can be obtained, resulting in a frequency overlap of more than 15 %. This frequency overlap allows the entire FMCW chirp to be generated with a minimum frequency step, i.e., fine frequency resolution (Δf_{FB}). However, the fine-tuning code jumps back and forth in the frequency overlap area, thus affecting the continuity of the frequency modulation, and this issue requires complex DCO gain calibration and linearization algorithms to address as mentioned in Section II.4.2.

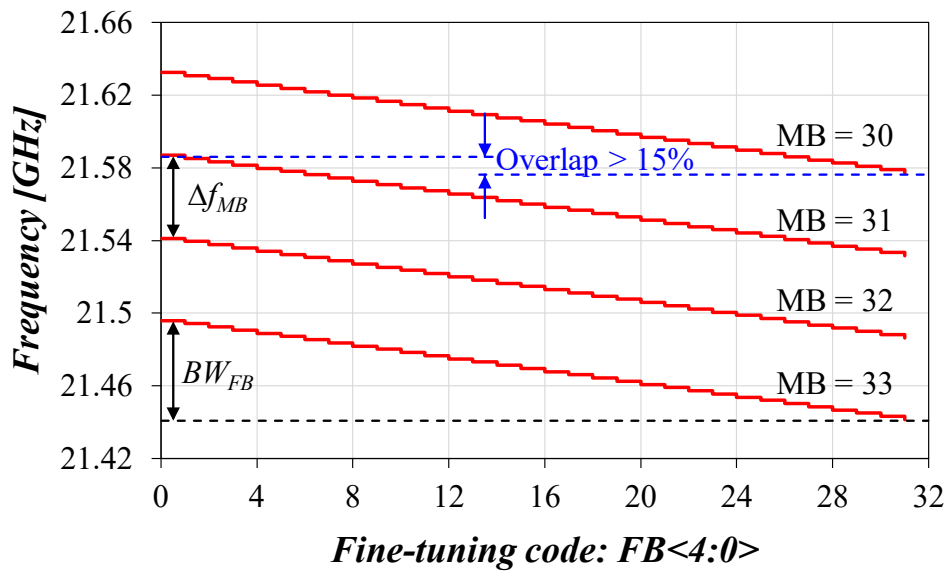


Figure II.5.17 Frequency-code characteristics of the medium-tuning bank and the fine-tuning bank when $CB = 16$.

II.5.5. Post-Layout Simulation Results

The top layout view of the proposed T-DCO is shown in [Figure II.5.18](#). The cross-coupled pair, coarse-tuning bank, medium-tuning bank, fine-tuning bank, and current mirror are sequentially placed below the center-tapped inductor. The large tail capacitors (C_{T1} and C_{T2}) are symmetrically distributed on both sides and bottom of the T-DCO to filter out the high-order harmonics on the long common-source line of the cross-coupled pair and the thermal noise from the tail current mirror. The total area of the T-DCO is $201 \times 302 \mu\text{m}^2$.

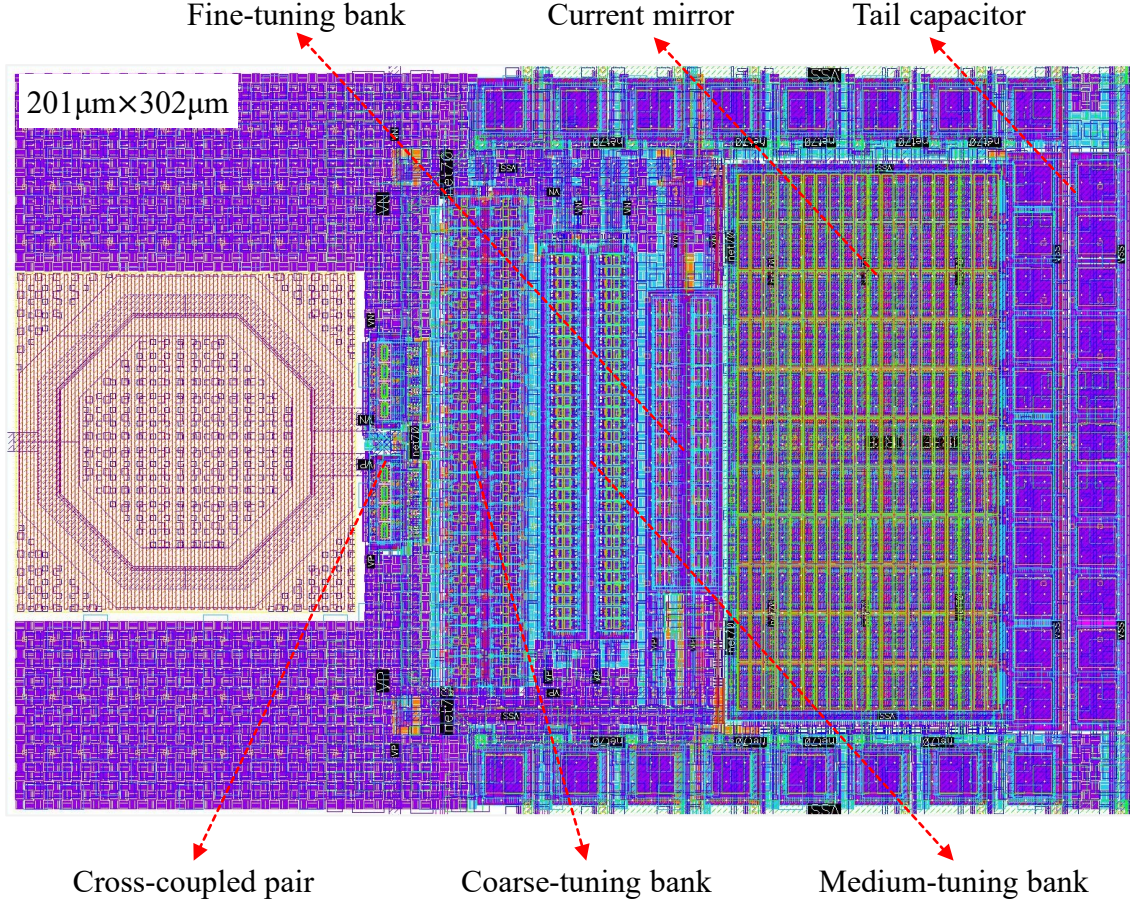
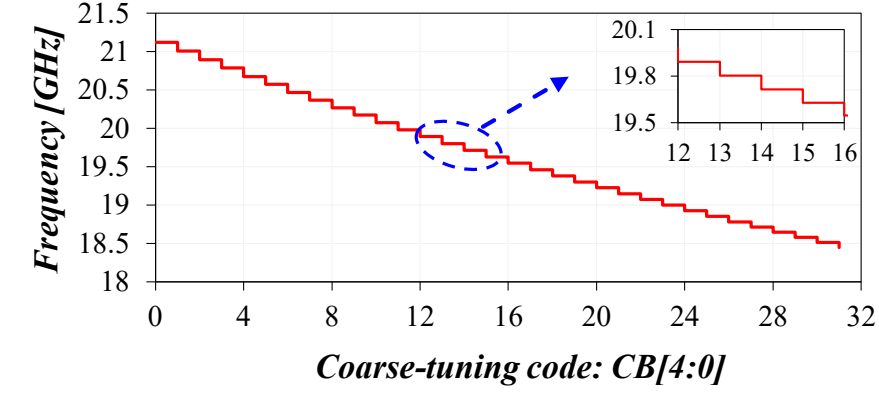
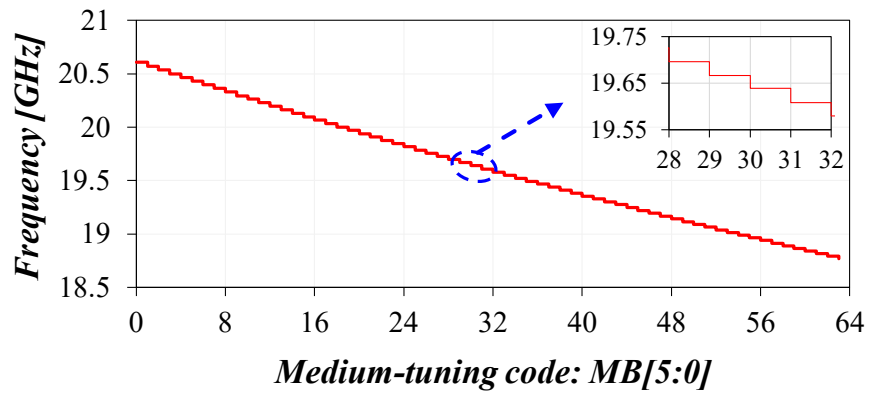


Figure II.5.18 Top layout view of the proposed T-DCO

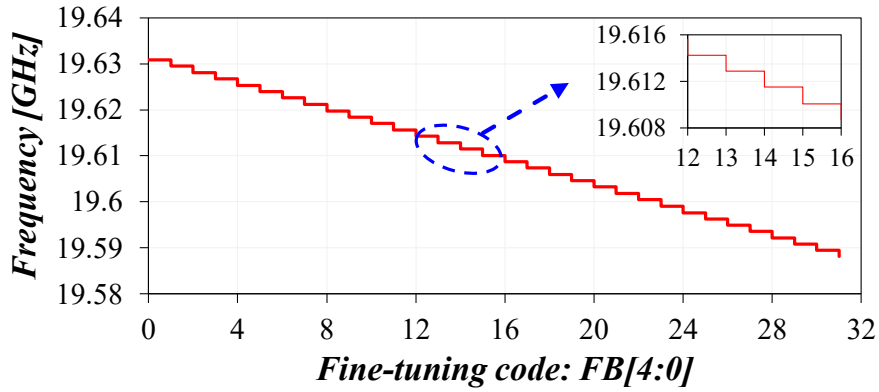
The frequency-code characteristics of the post-layout simulation with RC extraction are plotted in Figure II.5.19. It can be noted that the T-DCO oscillates from 18.45 GHz to 21.12 GHz for the coarse-tuning bank (MB = 32, FB = 16), which results in a frequency range of 2.67 GHz and an average coarse frequency resolution of about 86 MHz as shown in Figure II.5.19(a). Furthermore, by changing the medium-tuning code from 0 to 63 (CB = 16, FB = 16), a frequency range of roughly 1.84 GHz is obtained (18.77 – 20.61 GHz), which leaves a sufficient margin to cover the desired chirp bandwidth of 1.25 GHz. Finally, the fine-tuning bank allows changing the T-DCO frequency from 19.5881 GHz to 19.6309 GHz (CB = 16, MB = 32), corresponding to a fine frequency resolution of about 1.38 MHz. The combination of these three banks allows to cover a frequency band from 17.7 GHz (CB = 31, MB = 63, FB = 31) to 22.4 GHz (CB = 0, MB = 0, FB = 0), leading to a wide FTR of 23.4 %.



(a)



(b)



(c)

Figure II.5.19 Frequency-code characteristics of (a) the coarse-tuning bank, (b) the medium-tuning bank and (c) fine-tuning bank.

The PN performances of this T-DCO for the minimum, medium, and maximum oscillation frequency are shown in [Figure II.5.20](#). For a medium frequency of 19.61 GHz (CB = 16, MB = 32, FB = 16), the post-layout simulated PN is about -112.6 dBc/Hz at 1 MHz frequency offset. Moreover, the PN at 1 MHz frequency offset is lower than -110

dBc/Hz over the entire frequency range (i.e., for all codes).

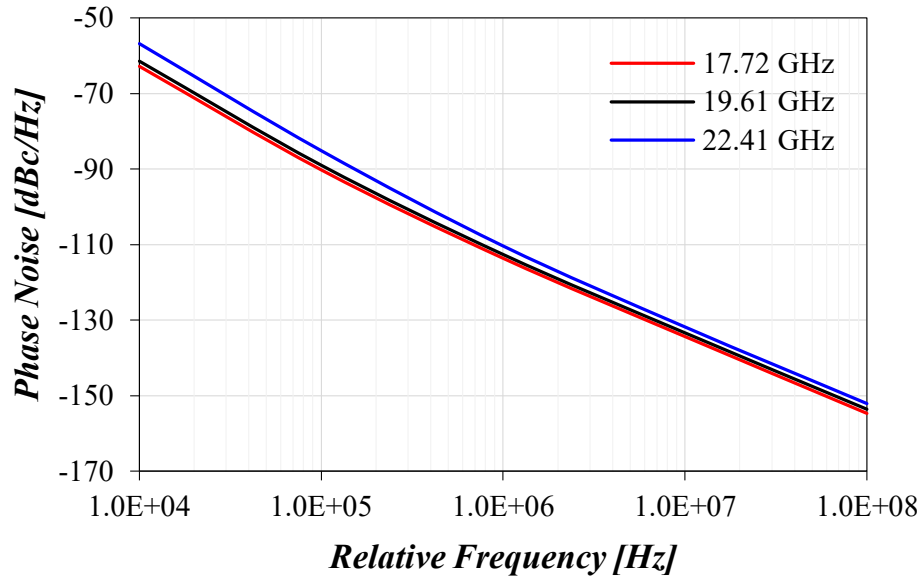


Figure II.5.20 Simulated phase noise plot at the minimum frequency of 17.72 GHz, the medium frequency of 19.61 GHz, and the maximum frequency of 22.41 GHz.

Table II.5.4 Post-layout simulated T-DCO performances for the three most representative PVT configurations

T-DCO	Worst case	Typical case	Best case
Configuration	125°, ss, 1.14 V	27°, tt, 1.2 V	-25°, ff, 1.26 V
Minimum Frequency (CB = 31, MB = 63, FB = 31)	16.03 GHz	17.72 GHz	19.77 GHz
Medium Frequency (CB = 16, MB = 32, FB = 16)	17.97 GHz	19.61 GHz	21.49 GHz
Maximum Frequency (CB = 0, MB = 0, FB = 0)	21.06 GHz	22.41 GHz	23.86 GHz
FTR	27.1 %	23.4 %	18.7 %
PN@1MHz (CB = 16, MB = 32, FB = 16)	-104.4 dBc/Hz	-112.6 dBc/Hz	-112 dBc/Hz

Table II.5.4 summarizes the post-layout simulated T-DCO performances for the three most representative PVT configurations: the worst case (125°, ss corner, 1.14 V), the typical case (27°, tt corner, 1.2 V), and the best case (-25°, ff corner, 1.26 V). Compared with the typical case, the medium frequency deviations are 1.64 GHz and 1.88 GHz for the worst and best cases, respectively. Fortunately, the coarse-tuning bank with a frequency tuning range of 2.67 GHz can fully compensate for these deviations. Moreover, the FTR is reduced to 18.7 % for the best case, but it is still sufficient to cover the FMCW chirp. In the worst case, the T-DCO suffers from severe voltage swing compression, leading to substantial degradation of the PN. At the medium frequency of 17.97 GHz, the

PN has dropped to -104.4 dBc/Hz at 1 MHz frequency offset. However, this PN degradation can be further compensated by increasing the tail current.

II.5.6. Comparative Study

Table II.5.5 T-DCO performances vs DCO specifications.

Parameters	DCO Specifications			T-DCO Performances			Units
	Minimum	Typical	Maximum	Minimum	Typical	Maximum	
temperature	-25°		125°	-25°		125°	
dvdd		0.8			0.8/1.2		V
avdd_reg	0.85	0.9	0.95	1.14	1.2	1.26	V
ibias_prog		4					bits
icc_on			60		20		mA
icc_off			1				mA
frequency	19		20.25	17.72	19.61	22.41	GHz
supply voltage		1			1.2		V
coarse step		200			86		MHz
fine step		2.5			1.38		MHz
chirp range		2.5			1.84		GHz
phase noise		-115		-113.6	-112.6	-110.3	dBc/Hz
		-135		-134.3	-133.4	-131.8	dBc/Hz
		-155		-154.6	-153.6	-152	dBc/Hz
Ton		50					ns

Table II.5.5 compares the performances of the T-DCO with the specifications. It can be seen that the current consumption of the T-DCO is much less than the 60 mA in the specifications, while T-DCO also has a very wide frequency-tuning range. The chirp range, which relies on the medium and fine-tuning banks, does not reach 2.5 GHz, but is still well above the theoretical 1.25 GHz, and the coarse- and fine-tuning steps are both better than the specifications. Unfortunately, we have taken various measures to improve the phase noise performances, but there is still about 2 dB difference from the requirement of -115 dBc/Hz at 1 MHz frequency offset. In general, the proposed T-DCO basically meets the required specifications.

Moreover, to quantify the overall performances of oscillators, the widely used figure-

of-merit (FoM) and FoM including FTR (FoM_T) are given by

$$FoM = PN + 10 \log \left(\frac{P_{DC}}{1mW} \right) - 20 \log \left(\frac{f}{\Delta f} \right) \quad (\text{II. 5. 11})$$

$$FoM_T = FoM - 20 \log \left(\frac{FTR}{10} \right) \quad (\text{II. 5. 12})$$

where P_{DC} is the dissipated power, f is the carrier frequency and Δf is the offset frequency. Moreover, the performances of the proposed T-DCO compared with the state-of-the-art are presented in Table II.5.6. It can be noted that the proposed T-DCO achieve the best-in-class PN with a competitive power consumption while also featuring a comparable FTR, FoM, and FoM_T.

Table II.5.6 Comparison with state-of-the-art K-band DCOs

Reference	Technology	Frequency [GHz]	FTR [%]	P _{DC} [mW]	PN ^c [dBc/Hz]	FoM ^c [dBc/Hz]	FoM _T ^c [dBc/Hz]
[II-26] ^a LMWC 2021	28 nm	24.4	27.2	1.2	-97	-184	-193
[II-49] ^a JSSC 2018	28 nm	27.3	14	12	-106	-184	-187
[II-31] ^a TMTT 2019	65 nm	23.7	24.4	4.8	-106.6	-187.2	-194.9
[II-38] ^b TVLSI 2019	65 nm	24	29	16.9	-104	-179	-188
[II-59] ^a JSSC 2018	65 nm	24.6	17	10	-102	-180	-184
This Work ^b	22 nm	19.61	23.4	24	-112.6	-184.65	-192.03

^a: measured results; ^b: post-layout simulation results; ^c: @ Δf = 1MHz

II.5.7. Summary

The proposed T-DCO achieves a wide FTR of 23.4 % and a low PN of -112.6 dBc/Hz at the medium frequency of 19.61 GHz. The novel back-gate-based fine-tuning bank allows a fine frequency resolution of ~1.38 MHz. Moreover, a frequency overlap of more than 15 % between the medium-tuning and fine-tuning banks allows for constructing a linear FMCW chirp with a frequency range of approximately 1.84 GHz. In the typical case, the T-DCO achieves a best-in-class PN lower than -110 dBc/Hz over the entire frequency range at 1 MHz frequency offset, allowing a wide FTR of more than 20 %

simultaneously. Furthermore, the T-DCO consumes about 24 mW from a 1.2 V supply voltage, leading to a FoM of -184.65 dBc/Hz and a FoM_T of -192.03 dBc/Hz. It is implemented in a 22 nm FD-SOI technology, and the occupied area is 201×302 μm².

II.6. Conclusion

In Section II.1, we focused on introducing the 22FDX technology, including its advantages and the supported libraries and components.

In Section II.2, we first introduced the challenges faced by conventional VCO designs in nanoscale CMOS processes, which is also the reason for the emergence of DCOs. We then reviewed three common types of DCOs. The RO-based DCO features poor phase noise performances and low oscillation frequency. The DAC-based DCO is highly dependent on a high-performance DAC and it is still essentially a VCO. The LC-based DCO not only exhibits excellent phase noise, but also can achieve both wide FTR and fine frequency resolution through a multi-stage capacitor bank structure, which is undoubtedly the most favored DCO structure at present.

In Section II.3, we started with a brief introduction of the first LC-based DCO for RF applications and its principle of digital-to-frequency conversion, where digitally controlled MOS varactors are used as frequency tuning units. We then reviewed and compared some of the commonly used frequency tuning techniques in DCOs, including mismatched MOS varactor structures, various switched-capacitor structures, and mm-W DiCAD structures. Finally, we summarized the performances of some typical LC-based DCOs in the literature at different frequencies.

In Section II.4, we mainly analyzed the principle of FMCW radar for detecting stationary and moving targets, and also briefly introduced the DCO gain calibration and linearization in chirp signal generation.

In Section II.5, we first outlined the background of DCO design for 76 – 81 GHz FMCW automotive radars. Next, we discussed some critical considerations for K-band DCO designs. Then, we detailed the proposed K-band T-DCO using the 22 nm FD-SOI process. We further analyzed the employed three different switched-capacitor structures, which allow to a wide FTR of more than 20 % and a frequency resolution of about 1.38 MHz. Moreover, the post-layout simulation results show that the T-DCO achieves best-

in-class phase noise in a compact area.

II.7. Résumé du Chapitre II

Le Chapitre II est consacré à la conception et la réalisation d'OCN à triple banques de capacités commutées (T-OCN) en bande K.

Dans la Section II.1, nous avons brièvement présenté les outils d'automatisation de la conception électronique (EDA en anglais) et la technologie 22 nm FD-SOI de GlobalFoundries utilisée dans le cadre de ces travaux de thèse. Par rapport aux process CMOS traditionnels, les dispositifs FD-SOI permettent de mieux contrôler le canal et de concevoir des circuits aux fréquences millimétriques. Grâce à la couche d'oxyde enterrée, les capacités parasites des jonctions (source, drain), le courant de fuite et les différentes sources de bruits sont considérablement réduits. En outre, la technologie de polarisation de la grille arrière et la structure à puit inversé (flipped well en anglais) sont les deux autres avantages du process FD-SOI, qui offre davantage de choix pour la conception des circuits qu'un process CMOS conventionnel.

Dans la Section II.2, nous avons d'abord indiqué les limites des Oscillateurs Contrôlés en Tension (OCT) traditionnels à résonateur LC utilisant un varactor MOS et implémentés en utilisant des process CMOS avancés, telles que la faible tension d'alimentation, la tension de seuil relativement élevée et la non-linéarité de la courbe capacité-tension. Nous avons ensuite comparé trois types courants d'OCN. Les OCNs à oscillateur en anneau qui ont un faible bruit de phase et une fréquence d'oscillation relativement basse. Les OCNs basés sur un Convertisseur Numérique-Analogique (CNA) qui dépendent fortement des performances du CNA et restent essentiellement des OCTs. Les OCNs à résonateur LC qui présentent non seulement un excellent bruit de phase, mais qui permettent également d'obtenir une large plage de réglage de la fréquence et une très bonne résolution en fréquence grâce aux multiples banques de capacités commutées qui peuvent être utilisées.

Dans la Section II.3, nous avons d'abord présenté le premier OCN à résonateur LC réalisé et fonctionnant à 2.4 GHz, dans lequel un varactor MOS contrôlé numériquement est utilisé comme unité de réglage de la fréquence. En outre, nous avons comparé certaines techniques de réglage de la fréquence couramment utilisées dans les OCNs,

telles que les varactors MOS non appariés, différentes structures de capacités commutées et les structures diélectriques artificielles contrôlées numériquement (DiCAD en anglais). Parmi ces techniques, la structure à capacité commutée est le premier choix pour la conception d'un OCN en bande K en raison de sa flexibilité, de sa stabilité et de sa simplicité. Nous avons également résumé les performances des OCNs typiques à résonateur LC oscillant à différentes fréquences et présents dans la littérature. Nous avons pu constater que peu d'OCN en bande K ou à ondes millimétriques ont été publiés, et que la plupart d'entre eux ne peuvent répondre aux contraintes imposées par les radars automobiles FMCW en raison de la limitation de la plage de réglage de la fréquence et de la résolution en fréquence.

Afin de mieux comprendre les particularités des OCNs appliqués aux radars FMCW, nous avons analysé en détail, dans la Section II.4, le principe du radar FMCW pour la détection de cibles stationnaires et mobiles, dont la précision dépend non seulement du bruit de phase et de la robustesse du système aux variations de process, de la température et de la tension d'alimentation (PVT en anglais), mais aussi de la linéarité des signaux modulés en fréquence. À notre connaissance, la plupart des OCNs sont basés sur des structures à multiples banques de capacités commutées permettant d'obtenir simultanément une haute résolution en fréquence et une large bande, ce qui signifie que la génération du signal modulé à large bande requiert l'utilisation de plusieurs banques de capacités commutées avec différents gains. Par conséquent, nous avons ensuite discuté brièvement des techniques d'étalonnage et de linéarisation du gain dans les OCNs à multiples banques de capacités commutées, lesquelles sont essentielles à la génération du chirp.

À la suite de ces discussions, dans la section II.5, nous avons d'abord décrit le contexte et les défis à relever afin de concevoir un OCN pour les radars automobiles FMCW fonctionnant entre 76 et 81 GHz. Nous avons ensuite présenté quelques considérations importantes pour la conception d'un OCN en bande K, notamment les spécifications de l'OCN souhaité, sa topologie, la conception du résonateur LC en bande K et le faible bruit de phase. Afin d'atteindre une largeur de bande de fréquence d'environ 2.5 GHz et une résolution d'environ 2.5 MHz, nous avons d'abord proposé d'utiliser trois banques de capacités commutées. Parmi ces banques, la banque de réglage grossier est principalement utilisée pour compenser les variations de PVT, tandis que les banques de réglage moyen et fin permettent de couvrir la largeur de bande du chirp. Afin de satisfaire

aux exigences de faible bruit de phase et de stabilité, la structure classique d'oscillateur à simple paire croisé fonctionnant en classe B a été adoptée. Par ailleurs, nous avons étudié en détail les capacités parasites des commutateurs MOS pour différentes régions de fonctionnement, ce qui est utile pour l'analyse qualitative de la structure à capacité commutée. Dans ces conditions, les résultats de simulations post-layout montrent que le T-OCN proposé oscille à une fréquence moyenne de 19.61 GHz et permet d'obtenir une large plage de réglage de la fréquence de 23.4 % et un faible bruit de phase de -112.6 dBc/Hz à 1 MHz de la porteuse. Une nouvelle structure de réglage fin basée sur la grille arrière permet d'obtenir une résolution de fréquence fine d'environ 1.38 MHz. En outre, le chevauchement de fréquence de plus de 15 % entre les banques de réglage moyen et fin permet la génération d'un chirp linéaire avec une plage de fréquence d'environ 1.84 GHz. Le T-OCN consomme environ 24 mW sous une tension d'alimentation de 1.2 V, ce qui conduit à une FoM de -184.65 dBc/Hz et une FoM_T de -192.03 dBc/Hz. Il est implémenté en technologie 22 nm FD-SOI et occupe une surface de 201×302 μm².

En conclusion, bien que le bruit de phase obtenu par le T-OCN proposé n'atteint pas les spécifications de -115 dBc/Hz à 1 MHz de la porteuse, les résultats de simulation post-layout montrent qu'il permet d'obtenir un bruit de phase à l'état de l'art. En outre, le T-OCN proposé est relativement robuste aux variations de PVT. Dans un cas typique (27°, tt corner, 1.2V), le T-OCN atteint un bruit de phase inférieur à -110 dBc/Hz à 1 MHz de la porteuse sur l'ensemble de la plage de fréquences, tout en permettant une large plage de réglage de la fréquence d'environ 20 %. Enfin, ce travail de recherche confirme la faisabilité de la conception d'un OCN à faible bruit de phase en bande K pour un radar automobile FMCW fonctionnant entre 76 et 81 GHz en technologie 22 nm FD-SOI. En outre, la nouvelle structure de capacité commutée basée sur la grille arrière proposée dans le T-OCN s'avère essentielle à l'obtention d'une résolution de fréquence fine.

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CHAPTER III

K-Band Dual-Bank DCO (D-DCO) Design

In the previous chapter, we described the principle of DCOs and introduced the circuit implementation of a K-band T-DCO for 76 – 81 GHz FMCW automotive radars. To the best of our knowledge, almost all published DCOs employ a multi-bank (more than three) structure similar to that of the T-DCO, which inevitably leads to a frequency overlap problem and therefore requires complex frequency calibration algorithms to achieve linear FMCW chirps. Therefore, in Section III.1, we will first briefly introduce the proposed K-band dual-bank DCO (D-DCO) to address this issue and meet the required specifications. The implementation of a linear FMCW chirp relies entirely on a single fine-tuning bank in the D-DCO, which means that the problem of frequency overlap no longer exists, leading to a significant reduction in the complexity of the algorithms. In Section III.2 and Section III.3, we will describe in detail the implementation process, the difficulties, and the post-layout simulation results of the proposed D-DCO.

III.1. Introduction to D-DCO

According to the principle of FMCW radar and DCO gain calibration introduced in Section II.4, one can be sure that covering the entire chirp range with a single capacitor bank is the most desirable case since the K_{DCO} of a single bank is approximately constant, which is the mentioned dual-bank DCO (D-DCO) prototype that we will discuss in the following sections, whose circuit implementation is the main objective of this chapter. Intuitively, this approach avoids frequent switching between multiple switched capacitor banks, leading to a short chirp setup time. Moreover, this approach allows us to address the issue of frequency linearization and calibration in multi-bank DCOs (similar to T-

DCO) from the design level rather than only from the algorithm level, thereby making it more suitable for FMCW automotive radars.

Note that the coarse-tuning bank of a D-DCO is not involved in frequency modulation and is only used to compensate for PVT variations. The implementation of the linear chirp depends entirely on the fine-tuning bank, i.e., the fine-tuning bank needs to achieve a large bandwidth of about 2.5 GHz according to the DCO specifications presented in Chapter II (Table II.5.1). Meanwhile, the D-DCO needs to achieve a relatively satisfactory frequency resolution of about 2.5 MHz to reduce quantization noise, meaning that the fine-tuning bank must integrate a large number of fine-tuning units ($2.5 \text{ GHz} \div 2.5 \text{ MHz} = 1000$) to meet the requirements of both large bandwidth and fine frequency resolution, which is the first challenge faced by this design. Meanwhile, the large number of fine-tuning units inevitably introduces enormous parasitic capacitances, making it difficult for the DCO to reach the K-band frequency. As a consequence, a proper design must be done in order to minimize these parasitic capacitances, which is the second challenge faced by this circuit.

Moreover, to the best of our knowledge, only several K-band DCOs have been published so far, and almost no prototype similar to the proposed D-DCO has been disclosed in the literature. Therefore, the research on K-band D-DCO in this chapter is of great significance for the future development of 76 – 81 GHz FMCW automotive radars. For this purpose, two versions of the D-DCO design are demonstrated in detail. Although the parasitic extraction results show that the first version of the D-DCO cannot reach the desired frequency and it fails from the design point of view, it is still meaningful for the relevant readers. The second version of the D-DCO solves the critical problems such as large parasitic capacitances and proves that the idea of D-DCO design is feasible.

III.2. First Version of D-DCO (D-DCO.1)

In this section, we present a D-DCO prototype based on standard components in the process library, called the first version of the D-DCO, named D-DCO.1.

Table III.2.1 Main parameters of the proposed D-DCO.1

VDD	I _{R1}	N _{1,2}	N ₃	N ₄	N ₅₋₇
1.2 V	1 mA	28.8 $\mu\text{m}/70\text{ nm}$	200 $\mu\text{m}/1\text{ }\mu\text{m}$	2400 $\mu\text{m}/1\text{ }\mu\text{m}$	36 $\mu\text{m}/70\text{ nm}$
N _{8,9}	C ₁	C ₂	C _{T1}	C _{T2}	L
5 $\mu\text{m}/70\text{ nm}$	36 fF	1.33 fF	12 pF	9 pF	78.6 pH

III.2.1.2. 4-Bit Coarse-Tuning Bank

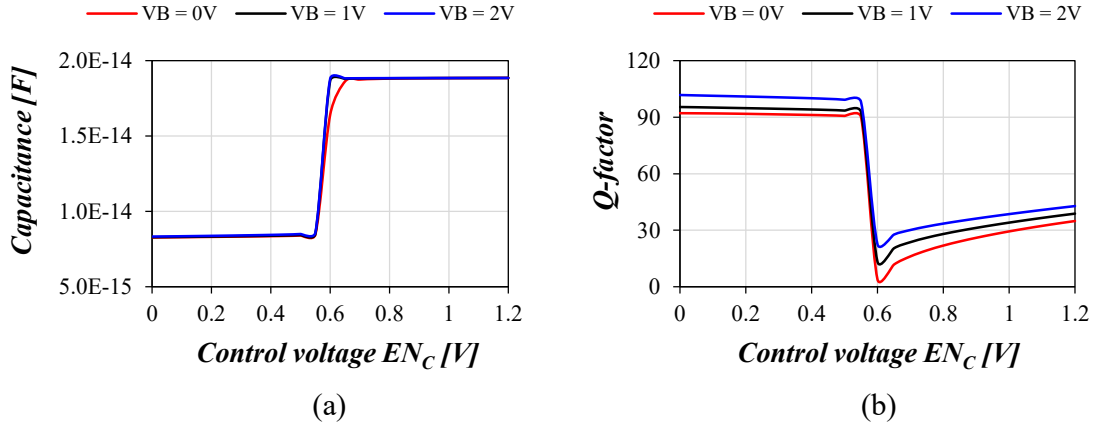


Figure III.2.2 Pre-layout simulation results of the coarse-tuning unit. (a) Capacitance values and (b) Q -factor versus control voltage EN_C when the back-gate voltage (VB) is 0 V, 1V, 2V, respectively.

The 4-bit (CB[3:0]) coarse-tuning bank consists of 15 identical coarse-tuning units to compensate for PVT variations. As shown in Figure III.2.1(c), the structure of this coarse-tuning unit is similar to that of the coarse-tuning unit of the T-DCO, except that the common source terminal of N_6 and N_7 is connected to the control terminal EN_C through an inverter (Note that this structure was the initial one we proposed, which was later completely abandoned due to the increase in layout area and parasitic capacitance caused by the introduced inverter). Therefore, when the control voltage is 0 V, the common source terminal is biased to a high voltage VDD for better switching off. Moreover, two large tri-metallic APMOM capacitors (3.5 $\mu\text{m}/3.5\text{ }\mu\text{m}$, $C_l = 36\text{ fF}$) are connected in series to achieve a large frequency step. Accordingly, to achieve a favorable Q -factor, three large-size MOS switches (N_{5-7} , 36 $\mu\text{m} / 70\text{ nm}$) are employed to reduce the ON-state parasitic resistance R_{ON} . As shown in Figure III.2.2, such a coarse-tuning unit achieves a capacitance ratio C_{ON_CB}/C_{OFF_CB} of 18.856 fF/8.274 fF when the back-gate voltage is 2 V, and the back-gate voltage (VB) has a negligible effect on the capacitance value.

However, when the back-gate voltage is increased from 0 V to 2 V, the Q -factor ratio can be boosted significantly from 34.7/92.2 to 42.6/101.8 due to the reduction of the equivalent series resistance.

III.2.1.3. 10-Bit Fine-Tuning Bank

As shown in Figure III.2.1(d), the structure of the fine-tuning unit is similar to that of the medium-tuning unit of the T-DCO; however, there are two differences between them. The first difference is that the common source terminal of N_8 and N_9 is connected to the control terminal EN_F through an inverter, and the other is that the capacitance value C_2 of 1.33 fF is achieved by connecting in series the two smallest tri-metallic APMOM capacitors (1 $\mu\text{m}/1 \mu\text{m}$, 2.66 fF) provided by the design kit. These are three main reasons for choosing such a small capacitance value: (1) it allows a higher frequency resolution; (2) there are 961 such fine-tuning units in the fine-tuning bank, and too large a capacitance value would cause the DCO to fail to oscillate around 20 GHz; (c) the fine-tuning unit with a small capacitance value allows the use of small-size MOS switches ($N_{8,9}$, 5 $\mu\text{m}/70 \text{ nm}$) while not degrading its Q -factor significantly. Moreover, the pre-layout simulation results of the fine-tuning unit are illustrated in Figure III.2.3. It can be seen that the Q -factor can also be further improved by increasing the back-gate voltage. When the back-gate voltage is 2 V, the proposed fine-tuning unit achieves a capacitance ratio of 747 aF/513 aF and an excellent Q -factor ratio of 80.4/278.9.

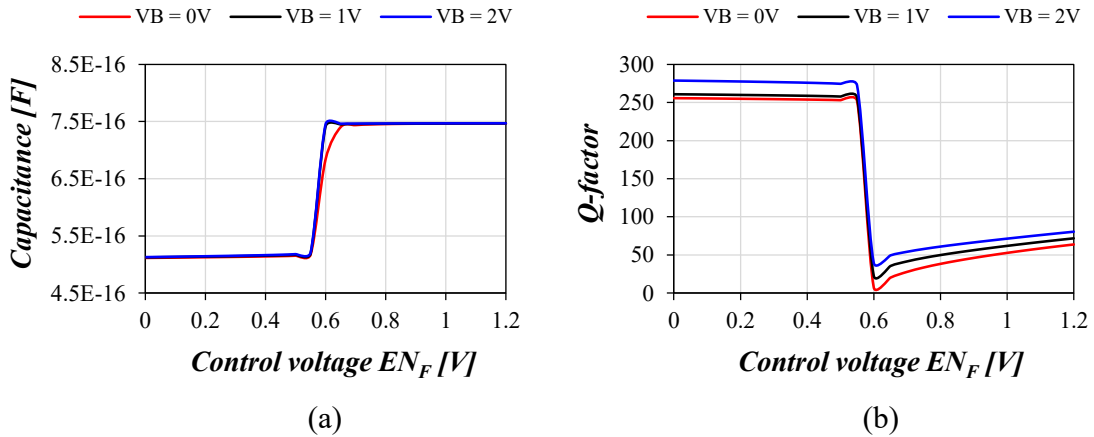


Figure III.2.3 Pre-layout simulation results of the fine-tuning unit. (a) Capacitance values and (b) Q -factor versus control voltage EN_F when the back-gate voltage is 0 V, 1V, 2V, respectively.

Figure III.2.4 shows the schematic of the 10-bit fine-tuning bank, which is array-

controlled and consists of 31 rows and 31 columns of fine-tuning units. To better understand the principle of this array control, a simplified architecture is given in Figure III.2.5(a). The 10-bit binary codes include 5-bit row codes and 5-bit column codes, which are converted into 31-bit thermometer codes through the binary-thermometer decoder (Section II.5.3.3), respectively. These thermometer codes are then fed into digital control blocks consisting of basic NAND and NOT logic circuits in Figure III.2.5(b) to precisely turn on or off the 961 fine-tuning units.

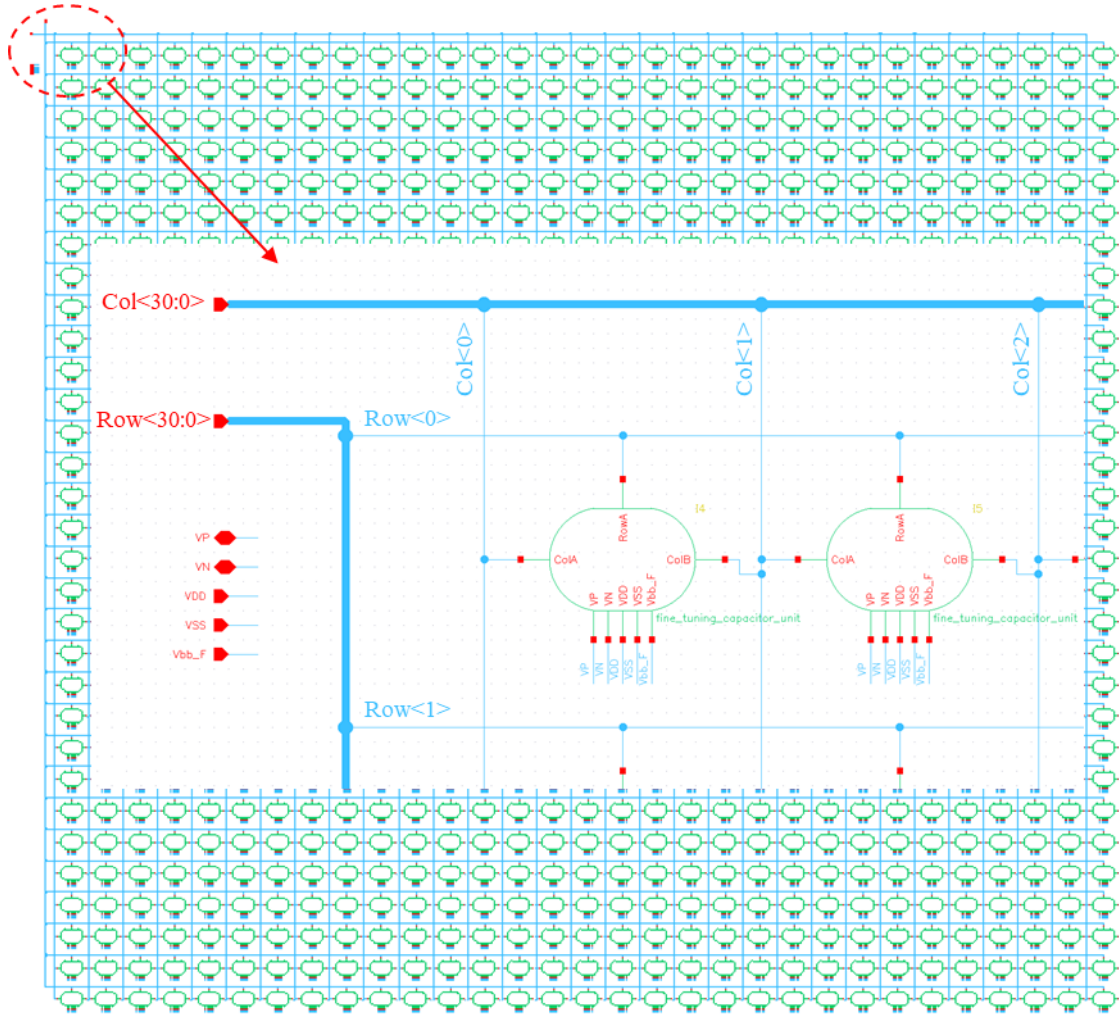


Figure III.2.4 Schematic of the 10-bit fine-tuning bank.

Figure III.2.5(c) depicts an example of logical values in the array control architecture. It can be seen that there are three possibilities: (1) one column is completely on; (2) one column is completely off; (3) one column is partially on. More specifically, if $C(i) = 1$ and its next bit $C(i+1) = 1$, the output logical value $Y = 1$, meaning that the corresponding i_{th} and $(i+1)_{th}$ columns are fully on. If $C(i) = 1$, $C(i+1) = 0$, the i_{th} column is still fully on, but the $(i+1)_{th}$ column is partially on, and $R(j)$ is used to control the number of turned-on

units in $(i+1)_{th}$ column.

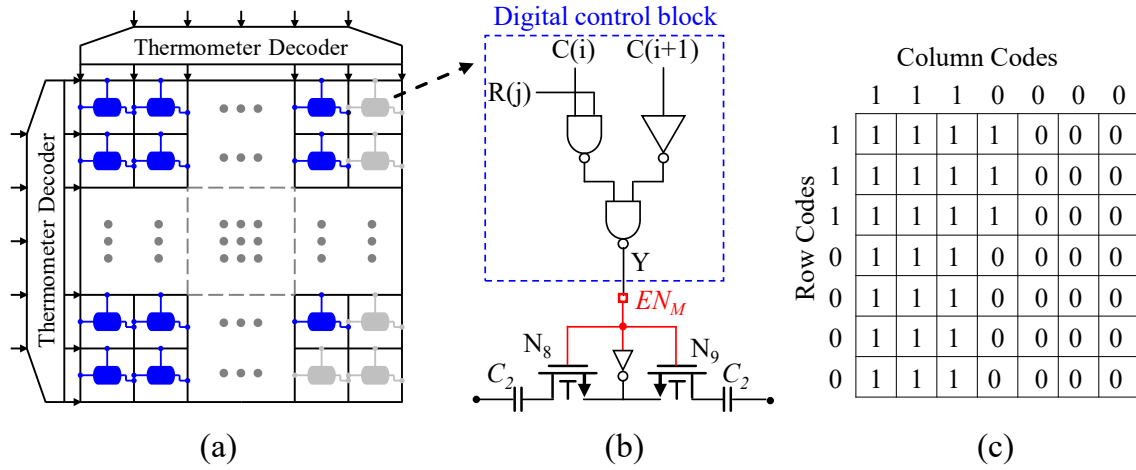


Figure III.2.5 (a) Simplified array control architecture of the fine-tuning bank, (b) digital control block implementation, and (c) example of output logical values.

The truth table of this digital control block is given in Table III.2.2; its output Y can be expressed mathematically as

$$Y = \overline{\overline{R(j)} \cdot \overline{C(i)} \cdot \overline{C(i+1)}} \quad (\text{III. 2. 1})$$

Thus, one can conclude that the column code $C(i+1)$ is assigned to turn 31 fine-tuning units (one column) on or off simultaneously, i.e., if $C(i+1) = 1$, $Y = 1$. The column code $C(i)$, together with the row code $R(j)$, is assigned to control an individual fine-tuning unit, which means that if $C(i) = 0$ and $R(j) = 1$, then $Y = 1$, otherwise $Y = 0$.

Table III.2.2 Truth table of the digital control block.

R(j)	0	0	0	0	1	1	1	1
C(i)	0	0	1	1	0	0	1	1
C(i+1)	0	1	0	1	0	1	0	1
Y	0	1	0	1	0	1	1	1

III.2.1.4. LC Resonant Tank

The minimum, medium, and maximum resonant frequencies of the LC tank and the corresponding equivalent parallel resistance R_P are plotted in Figure III.2.6. It can be seen that the R_P increases with the resonant frequency. Thus, the minimum R_P occurs at the lowest resonant frequency of 17.9 GHz (CB = 15, FB = 961, meaning that all 15 coarse-tuning units and 961 fine-tuning units are on), which is about 133.5 Ω . According to the

start-up condition, i.e., $g_m R_p \geq 2$, the cross-coupled pair's transconductance value g_m needs to be higher than 15 mS.

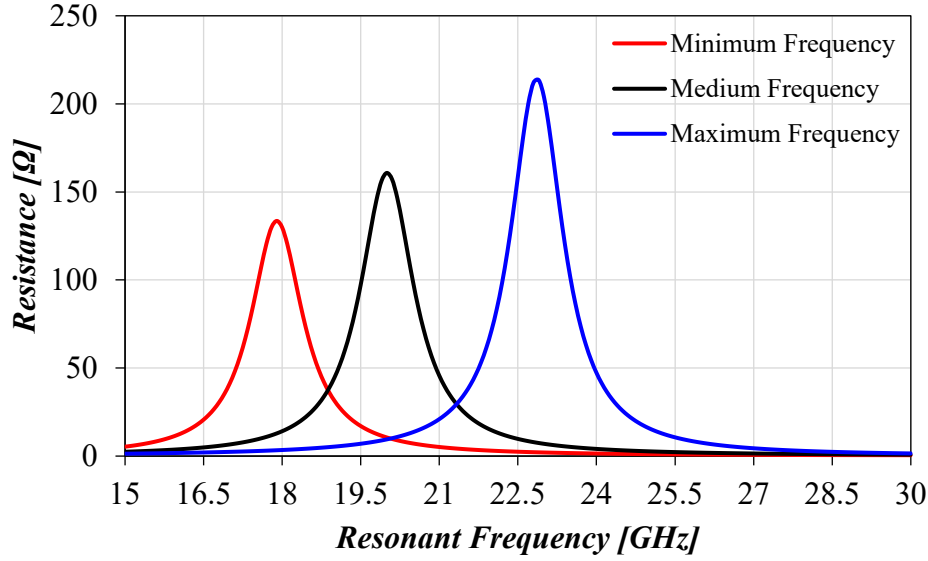


Figure III.2.6 Real part of the impedance versus the resonant frequency of the LC tank.

III.2.2. Pre-Layout Simulation Results

III.2.2.1. Frequency-Code Characteristic Curves

Table III.2.3 DC operating points of the transistors N_{1-4} .

Parameters	id	vth	vds	vgs	gm
N_{1-2}	5.964 mA	485.3 mV	909.3 mV	913.4 mV	23.35 mS
N_3	1 mA	518.2 mV	694.1 mV	694.1 mV	10.26 mS
N_4	11.93 mA	518.6 mV	283 mV	694.1 mV	122.4 mS

Before determining the frequency-code characteristic curves of the D-DCO.1, the DC analysis is required to determine the cross-coupled pair's transconductance value and the operating state of transistor N_4 in the current mirror. The transistor N_4 has to be biased in the flat saturation region to provide a stable tail current. When $CB = 8$ and $FB = 481$, the main parameters of the DC operating points of transistors N_{1-4} are shown in [Table III.2.3](#). It can be seen that the single-side transistors of the cross-coupled pair provides a transconductance of 23.35 mS and its threshold voltage is 485.3 mV. In addition, since the drain-source voltage of transistor N_4 is larger than its overdrive voltage, it is well biased in the saturation region, and its drain current is 11.93 mA, which is very close to

the ideal value of 12 mA.

The differential output oscillation waveforms (VP and VN, transient simulation) of the D-DCO.1 at medium frequency f_0 (CB = 8, FB = 481) are shown in Figure III.2.7. The output voltage ranges from 0.68 V to 1.72 V. In addition, VT is the waveform of the signal at the common mode point T, and the frequency of this signal is $2f_0$. Furthermore, this signal can be mixed to the oscillator output frequency by the cross-coupled pair, thereby degrading its phase noise. Therefore, in order to filter out this second-order harmonic, a large capacitor C_{T2} is inserted at node T, resulting in a small voltage swing (almost a constant voltage) of VT.

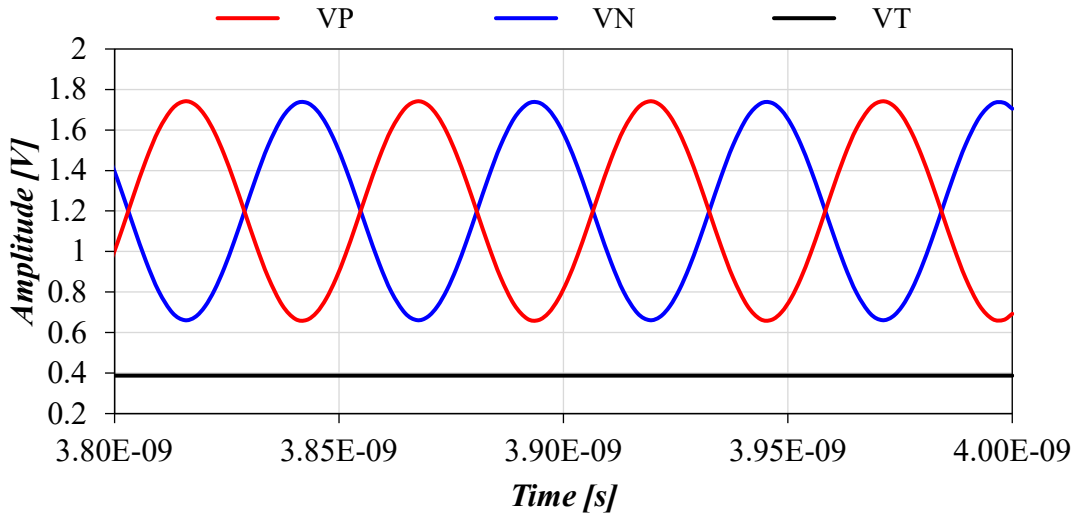


Figure III.2.7 Output oscillation waveforms of the D-DCO.1.

When the fine-tuning code is 481, the pre-layout simulated frequency-code characteristic curve of the coarse-tuning bank is shown in Figure III.2.8. The frequency of the D-DCO.1 decreases from 20.76 GHz to 18.87 GHz as the coarse-tuning code varies from 0 to 15, leading to a coarse-tuning range of 1.89 GHz. Moreover, a gradual reduction of the step size from 150 MHz for the lowest code value CB = 0 to 110 MHz for the highest code value CB = 15 is observed due to the change in total capacitance value, and the average coarse-tuning step is about 126 MHz. When the coarse-tuning code is 8, the pre-layout simulated frequency-code characteristic curve of the fine-tuning bank is shown in Figure III.2.9. The D-DCO.1 oscillates from 21.05 GHz to 18.44 GHz when the fine-tuning code changes from 0 to 961. The fine-tuning range is 2.61 GHz, which is slightly larger than the chirp bandwidth of 2.5 GHz required in the specifications. The average fine-tuning step is about 2.72 MHz.

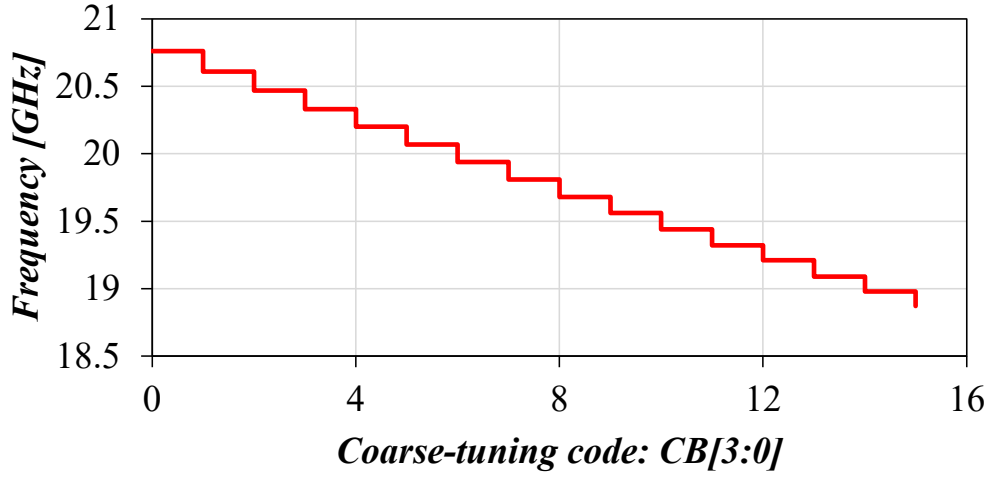


Figure III.2.8 Frequency-code characteristic of the coarse-tuning bank when the fine-tuning code is 481.

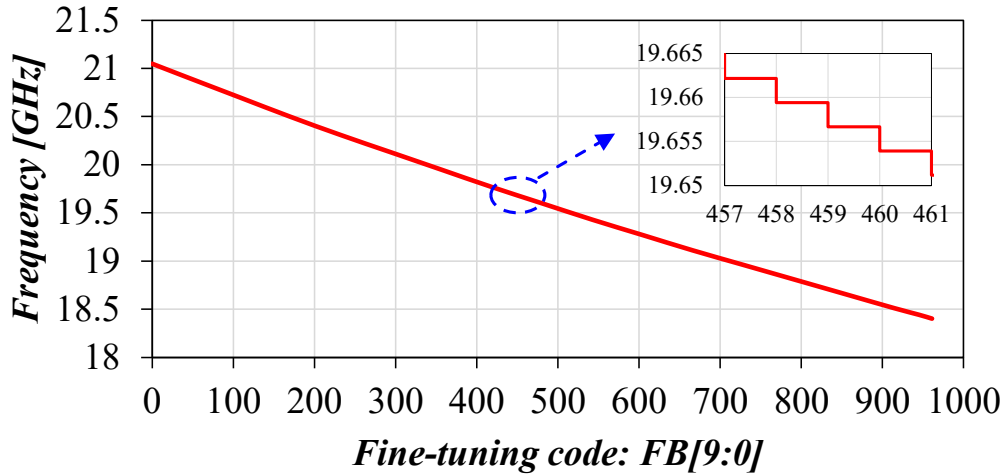


Figure III.2.9 Frequency-code characteristic of the fine-tuning bank when the coarse-tuning code is 8.

III.2.2.2. PN Performances

Considering the trade-off between the power consumption and the phase noise, the tail current is set to 12 mA, so the D-DCO.1 consumes 14.4 mW from a 1.2 V supply voltage. Its pre-layout simulated PN performances at minimum, medium, and maximum frequencies are shown in [Figure III.2.10](#). At the medium frequency (CB = 8, FB = 481) of 19.68 GHz, the PN is -70.3 dBc/Hz and -116.1 dBc/Hz at 10 kHz and 1 MHz frequency offsets, respectively. Compared to the PN at medium frequency, the PN has no significant improvement at the minimum frequency (CB = 15, FB = 961) of 17.73 GHz due to the

reduction of the Q -factor as the tuning units are turned on. Meanwhile, we notice a significant PN degradation close to the carrier frequency (at 10 kHz frequency offset). Fortunately, this kind of noise close to the carrier will be filtered by the ADPLL loop. Moreover, the worst PN occurs at the maximum frequency (CB = 0, FB = 0) of 22.37 GHz, where the PN decreases by 8.6 dB and 1.6 dB at 10 kHz and 1 MHz frequency offsets, respectively, compared to the PN at medium frequency. The main reason is the significant increase in carrier frequency.

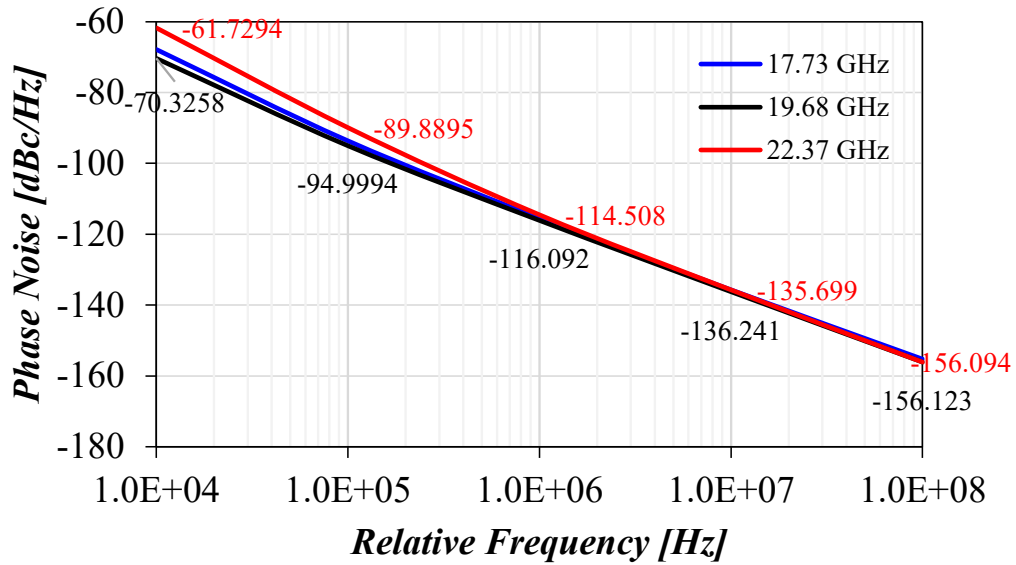


Figure III.2.10 Pre-layout simulated PN at the minimum frequency of 17.73 GHz, the medium frequency of 19.68 GHz, and the maximum frequency of 22.37 GHz.

Moreover, when the fine-tuning code is set to 481, the PN variations versus the coarse-tuning codes are shown in Figure III.2.11. It can be seen that the PN variations at 10 kHz frequency offset are lower than 1.5 dB, while the PN is almost unchanged (less than 0.3 dB variations) at 100 kHz, 1 MHz, and 10 MHz frequency offsets. When the coarse-tuning code is set to 8, the PN variations versus the fine-tuning codes are shown in Figure III.2.12. It can be noted that the PN variations for all the fine-tuning codes are less than 1 dB, which is very useful for achieving wide modulation bands.

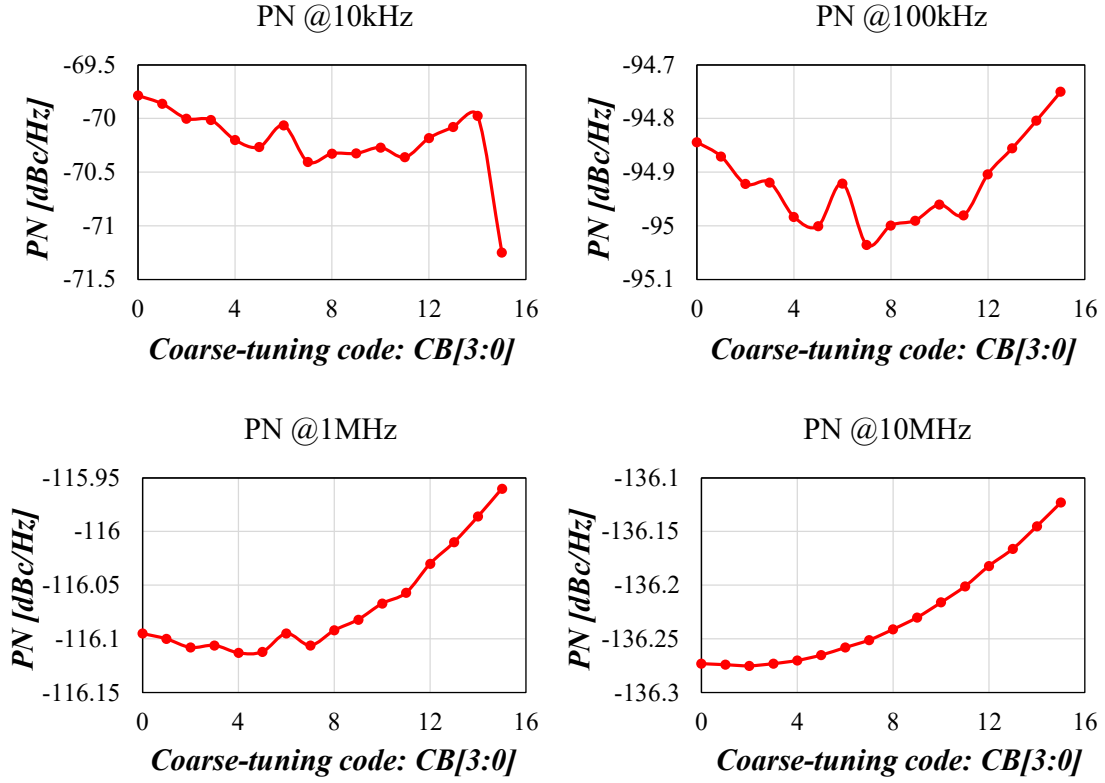


Figure III.2.11 PN variations versus the coarse-tuning codes.

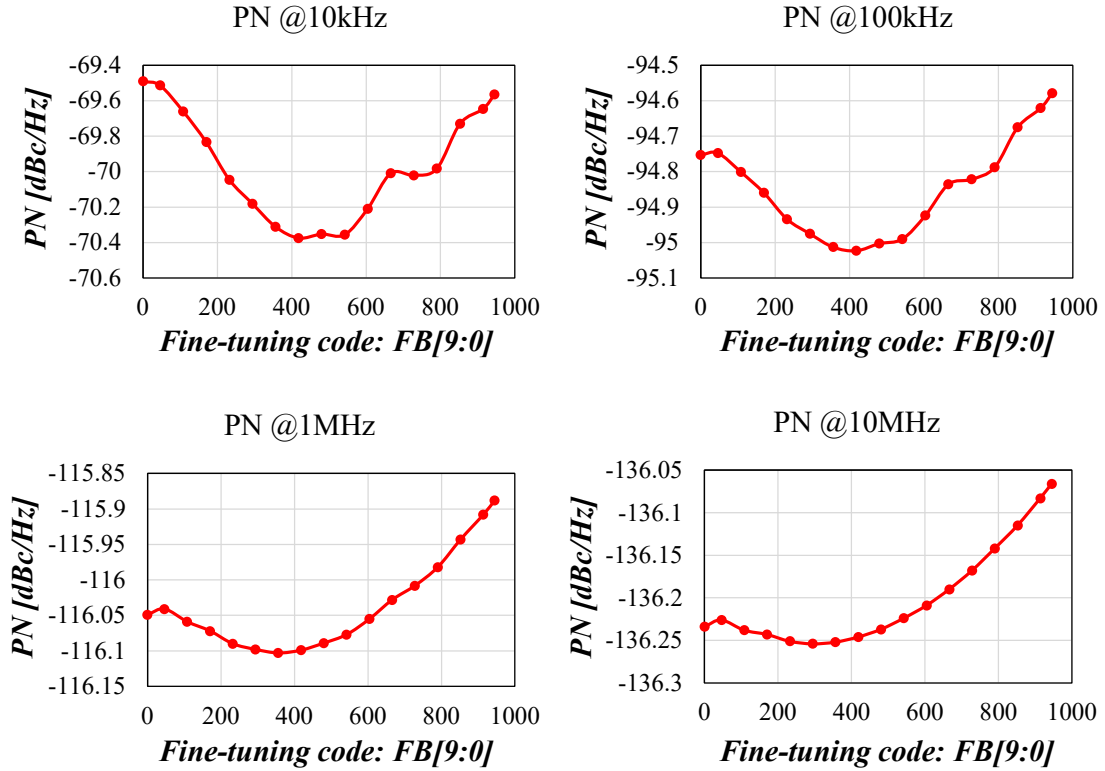


Figure III.2.12 PN variations versus the fine-tuning codes.

III.2.2.3. PVT Variations

When $CB = 8$, $FB = 481$, the supply voltage is 1.2 V and the temperature is 27° , the effects of different process corners on the oscillation frequency and the phase noise are given in Figure III.2.13. The selected process corners are fast-fast (ff), typical-typical (tt), and slow-slow (ss). Compared to the tt corner, the ff and ss corners result in a frequency deviation of about 2 GHz. Fortunately, the different process corners have no significant effect on the phase noise except for the low frequency offset.

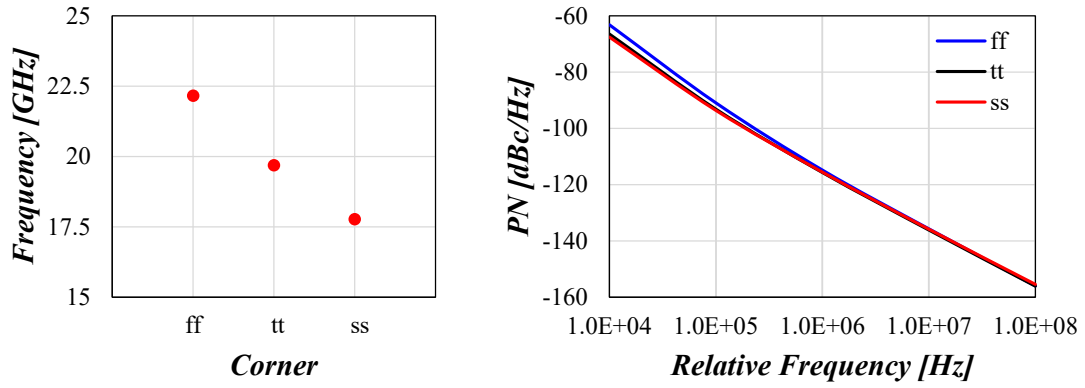


Figure III.2.13 Frequency and PN variations versus different processes.

When $CB = 8$, $FB = 481$, the corner is tt, and the temperature is 27° , the simulation results with different supply voltages are shown in Figure III.2.14. The supply voltages are chosen to be 1.14 V, 1.2 V, and 1.26 V, i.e., 5 % supply voltage fluctuations. It can be seen that it has an almost negligible effect on the oscillation frequency and the phase noise.

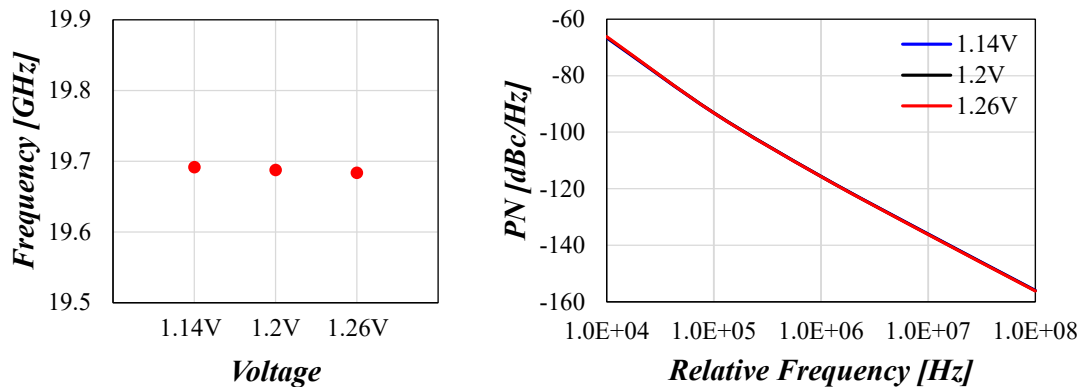


Figure III.2.14 Frequency and PN variations versus different supply voltages.

Moreover, When $CB = 8$, $FB = 481$, the corner is tt, and the supply voltage is 1.2 V,

the simulation results at different temperatures are shown in Figure III.2.15. The temperatures are set to -40° , 27° , and 140° . Compared to the room temperature of 27° , the frequency deviation caused by -40° and 140° temperatures is about 150 MHz. Meanwhile, the phase noise performances degrade severely at high temperatures, which needs to be compensated from the system design level and is not the focus of our studies.

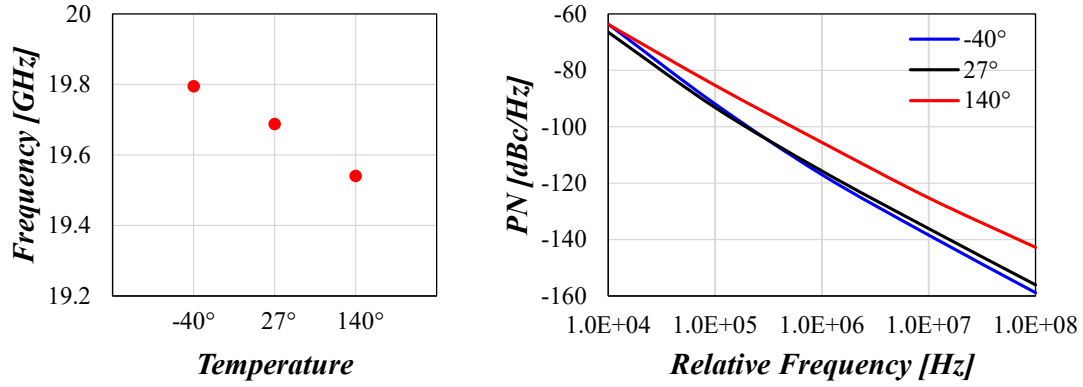


Figure III.2.15 Frequency and PN variations versus different temperatures.

III.2.2.4. Overall Performances of the D-DCO.1

Table III.2.4 compares the pre-layout simulated performances of the D-DCO.1 with the specifications of the DCO. One can see that the current consumption of the D-DCO.1 is only 12 mA (without buffer), which is much lower than the 60 mA in the specifications. Moreover, the 10-bit fine-tuning bank allows to cover a frequency range of 2.61 GHz, which is also larger than the 2.5 GHz expected in the specifications, so the chirp range of 19 – 20.25 GHz for 76 – 81 GHz automotive radars can be wholly generated by such a fine-tuning bank with a large margin. Moreover, the combination of the coarse-tuning bank and the fine-tuning bank allows to cover a frequency range of 17.73 – 22.73 GHz, i.e., a wide FTR of 23.6 %. The achieved coarse-tuning step is 126 MHz, which is better than what the specifications require. The achieved fine-tuning step is 2.72 MHz, which is comparable to the desired 2.5 MHz in the specifications. Meanwhile, at the medium frequency of 19.68 GHz, the D-DCO.1 achieves an excellent PN of -116.1 dBc/Hz at 1 MHz frequency offset thanks to the large output voltage swing and the designed high Q -factor LC tank, which also exceeds the specifications. Furthermore, the D-DCO.1 consumes 14.4 mW from a supply voltage of 1.2 V. In summary, the pre-layout simulation results show that the performances of the D-DCO.1 satisfies the design specifications very well.

Table III.2.4 D-DCO.1 performances vs DCO specifications

Parameters	DCO Specifications			D-DCO.1 Performances			Units
	Minimum	Typical	Maximum	Minimum	Typical	Maximum	
temperature	-25°		125°	-40°		140°	
dvdd		0.8			1.2		V
avdd_reg	0.85	0.9	0.95	1.14	1.2	1.26	V
ibias_prog		4					bits
icc_on			60		12		mA
icc_off			1				mA
frequency	19		20.25	17.73	19.68	22.37	GHz
supply voltage		1			1.2		V
coarse step		200			126		MHz
fine step		2.5			2.72		MHz
chirp range		2.5			2.61		GHz
phase noise		-115			-116.1		dBc/Hz
		-135			-136.2		dBc/Hz
		-155			-156.1		dBc/Hz
Ton		50					ns

III.2.3. Problems in Post-Layout Simulations

The pre-layout simulation results of the D-DCO.1 are encouraging; however, it can be inferred that the 10-bit fine-tuning bank inevitably occupies a large area and introduces large interconnect parasitic capacitances. The question remains, how large are the parasitic capacitances and do the post-layout simulation results of the D-DCO.1 still meet the design requirements ? These are the key points that will be discussed in this subsection.

Figure III.2.16 gives the layout view of a single fine-tuning unit. It can be seen that the digital control block occupies twice the area of the fine-tuning unit since it contains more transistors. Note that all the used transistors and capacitors are from the standard library of the 22 nm FD-SOI process. Then, taking into account the DRC rules, such as the minimum distance between two adjacent transistors, a non-compact layout is obtained. The total size of such a fine-tuning unit is $29.148 \mu\text{m} \times 23.01 \mu\text{m}$.

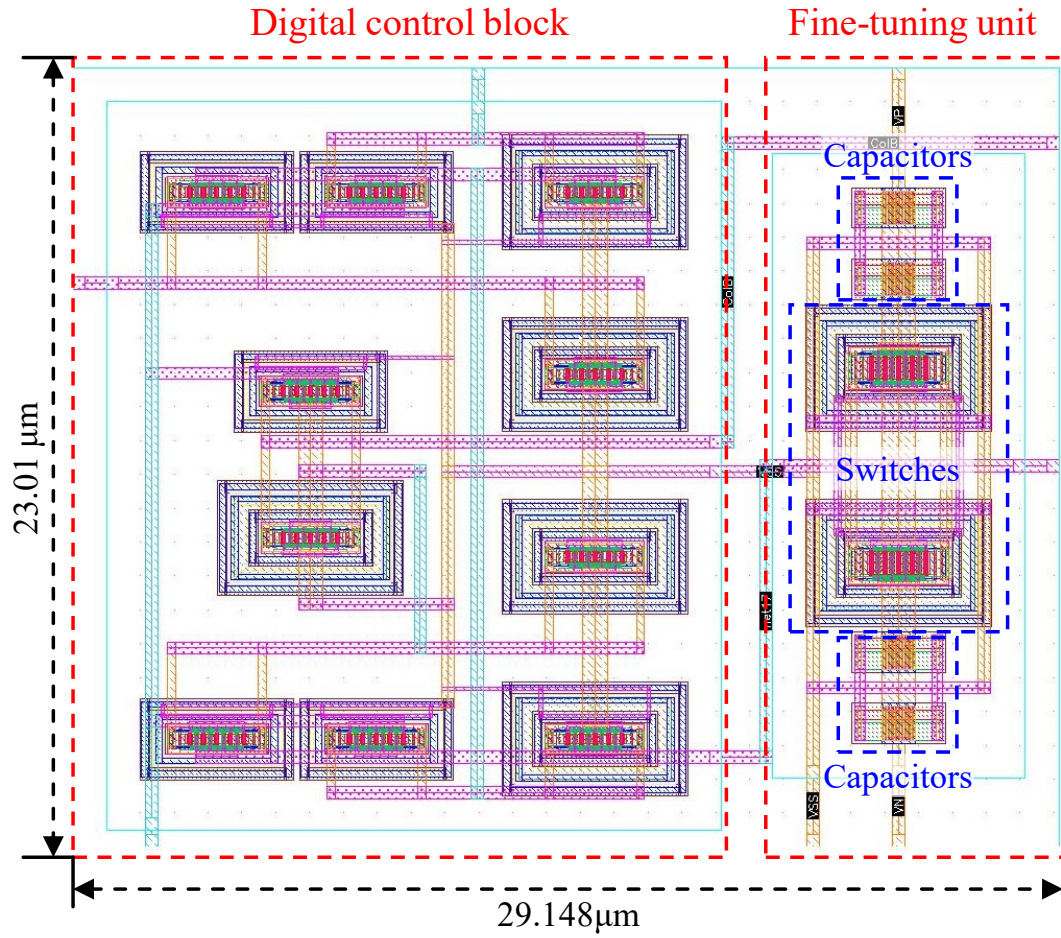


Figure III.2.16 Layout of a single fine-tuning unit with a digital control block.

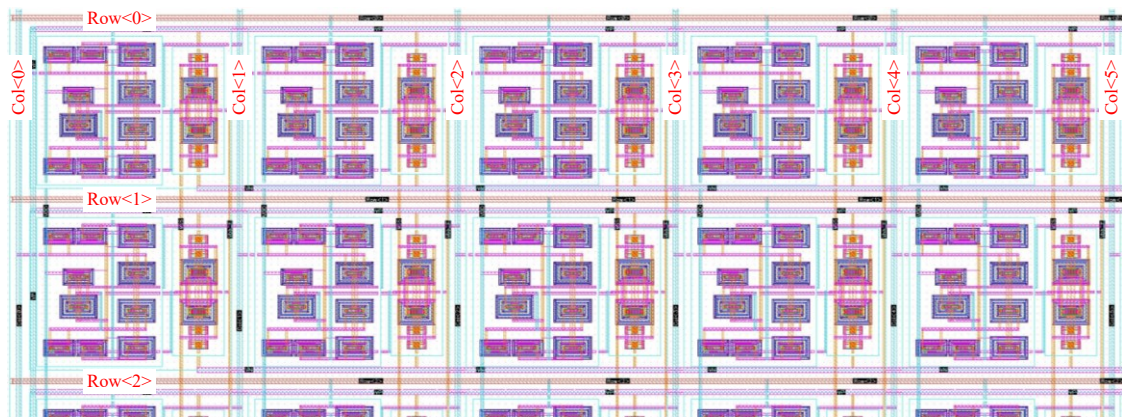


Figure III.2.17 Internal connection of partial fine-tuning bank.

Figure III.2.17 shows the internal connection of the upper left part of the 10-bit fine-tuning bank. As explained in Figure III.2.5, this fine-tuning bank adopts an array control architecture, where all 961 fine-tuning units can be precisely controlled by row codes (Row<0>, Row<1>, ...) and column codes (Col<0>, Col<1>, ...).

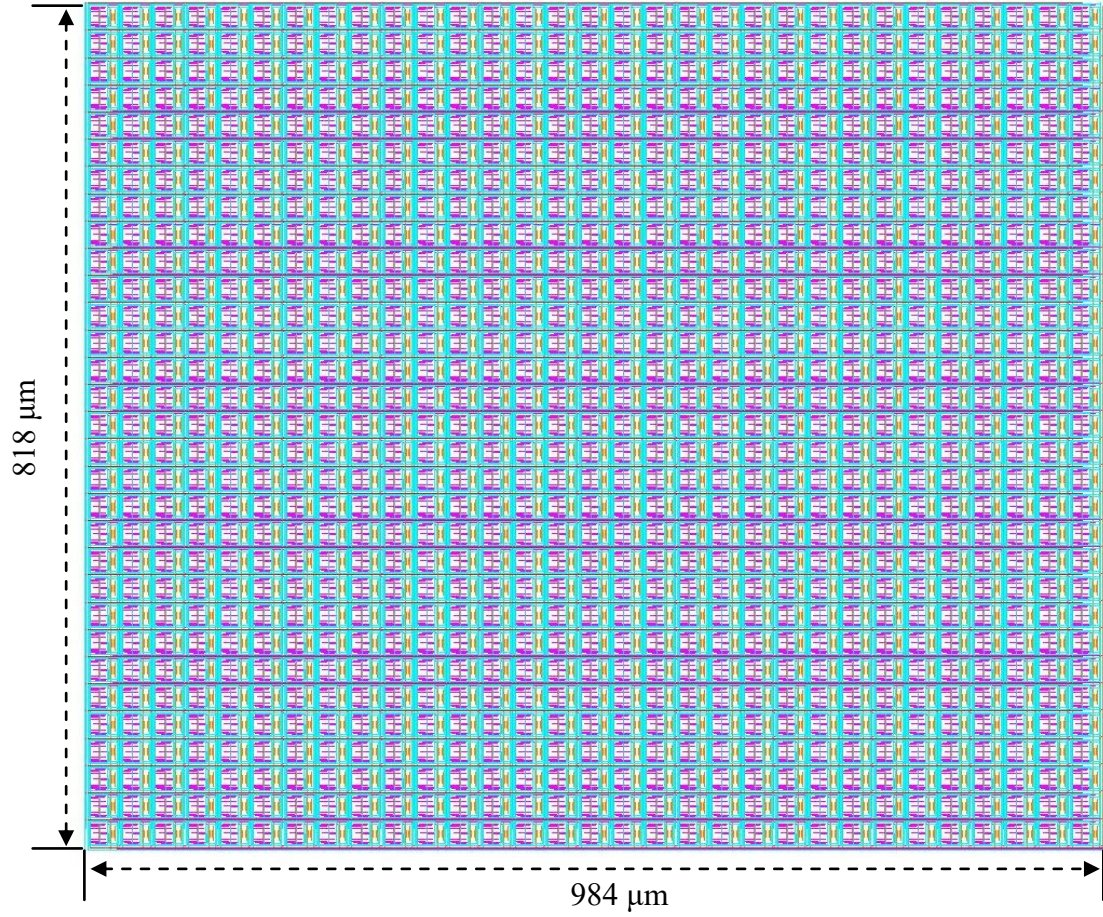


Figure III.2.18 Layout view of the 10-bit fine-tuning bank.

The layout of the 10-bit fine-tuning bank is shown in Figure III.2.18. Since the fine-tuning bank contains 961 digital control blocks, its layout area is enormous, about $984 \mu\text{m} \times 818 \mu\text{m}$. Considering that the inner diameter and width of the center-tapped inductor used in D-DCO.1 are $44.5 \mu\text{m}$ and $6 \mu\text{m}$, respectively, that is to say, the layout area of this inductor is about one-300th of that of the fine-tuning bank. There is no doubt that this layout is unacceptable.

Therefore, the first thing that should be done is to reduce the layout area. Since the digital control blocks occupy a large portion of the total area, there are two intuitive ways to reduce the total area. One is to fuse the transistors in the digital control block, i.e., to remove the substrate ring of the transistors or even to change the finger structure, but this way of using non-standard components requires various technical support. In contrast, the other way is more attractive, which is to move all digital control blocks out of the oscillator so that they can be implemented through digital circuits.

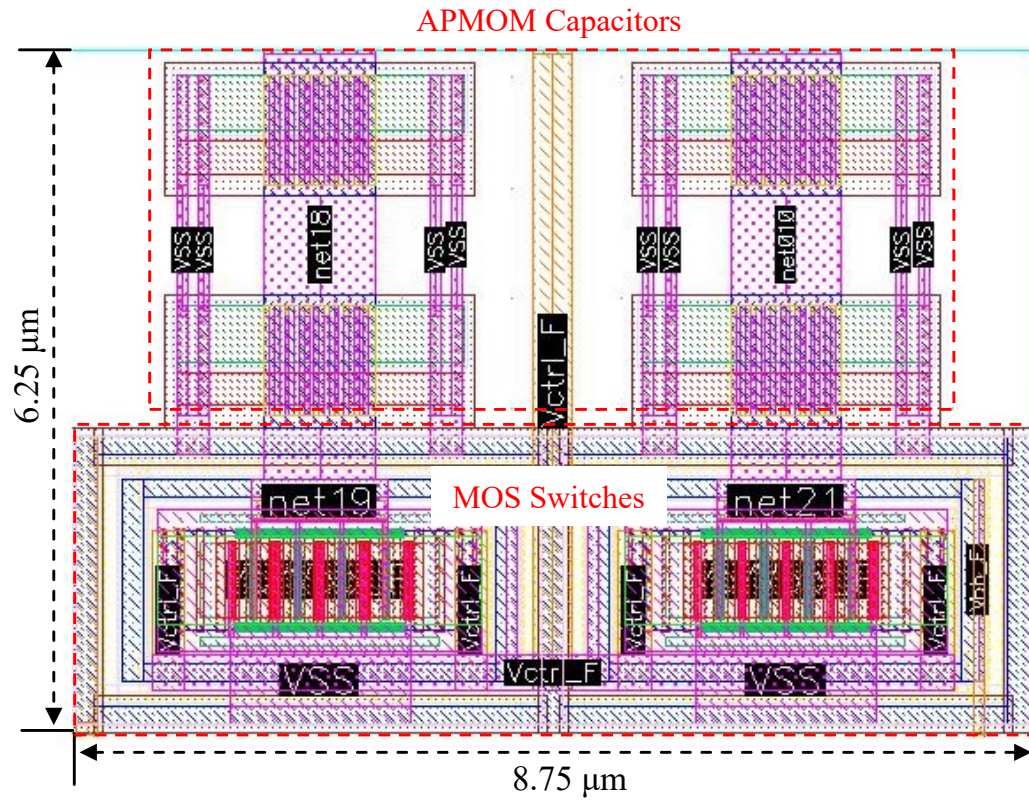


Figure III.2.19 New fine-tuning unit without the digital control block.

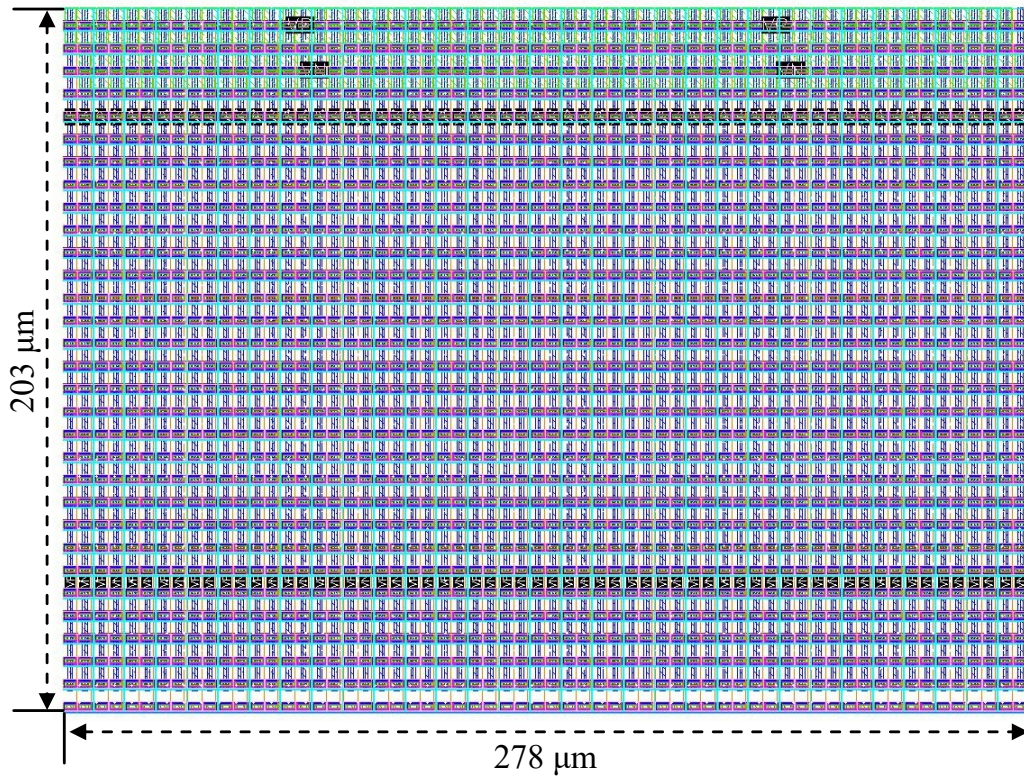


Figure III.2.20 New 10-bit fine-tuning bank without the digital control block.

Once we move out of the digital control block, it can be seen from Figure III.2.16 that the only remaining layout of the fine-tuning unit on the right side is not an approximately square, and using this layout directly to construct a 10-bit fine-tuning bank would lead to an imbalance in its length-to-width ratio, which is imperfect. Thus, a new proposed layout of the fine-tuning unit without the digital control block is shown in Figure III.2.19, which is close to a square structure. Consequently, a new layout of the 10-bit fine-tuning bank using 31×31 such fine-tuning units is shown in Figure III.2.20. Compared to the previous fine-tuning bank with digital control blocks, the total area is considerably reduced to $278 \mu\text{m} \times 203 \mu\text{m}$.

In order to evaluate the parasitic capacitances, the post-layout simulation results of the fine-tuning unit and the fine-tuning bank are given in Table III.2.5. One can see that such a fine-tuning unit achieves a capacitance ratio of 762 aF/602 aF and a Q -factor ratio of 72/88. The 10-bit fine-tuning bank achieves a capacitance ratio of 1.37 pF/1.2 pF, and its Q -factor ratio deteriorates to 14.5/17.8 due to the large interconnect parasitic resistances. Apparently, the total capacitance value of the fine-tuning bank still remains too high, making it difficult for the D.DCO.1 to oscillate near 20 GHz. Furthermore, it is impossible to achieve low phase noise performances by such poor Q -factors of the fine-tuning bank.

Table III.2.5 Post-layout simulation results with RC extraction of the new fine-tuning unit and the new 10-bit fine-tuning bank with 31×31 fine-tuning units.

Parameters	C_{ON}	C_{OFF}	ΔC	Q_{ON}	Q_{OFF}
Fine-tuning unit	762 aF	602 aF	160 aF	72	88
Fine-tuning bank (31×31)	1.37 pF	1.2 pF	170 fF	14.5	17.8

In addition, based on these data, the interconnect parasitic capacitance C_{wire} in the fine-tuning bank can be calculated. Since the capacitance of a single fine-tuning unit in the ON-state is 762 aF, if C_{wire} is ignored, the total capacitance of 961 such fine-tuning units would be 732.3 fF ($762 \text{ aF} \times 961$). Nevertheless, the simulated total capacitance of the fine-tuning bank with 961 fine-tuning units in the ON-state is 1.37 pF, meaning that C_{wire} is $1.37 \text{ pF} - 732.3 \text{ fF} = 637.7 \text{ fF}$. Indeed, an approximate C_{wire} value can be obtained by using the capacitance in the OFF-state. Therefore, it can be concluded that the C_{wire} value in this fine-tuning bank is about half of the total capacitance value.

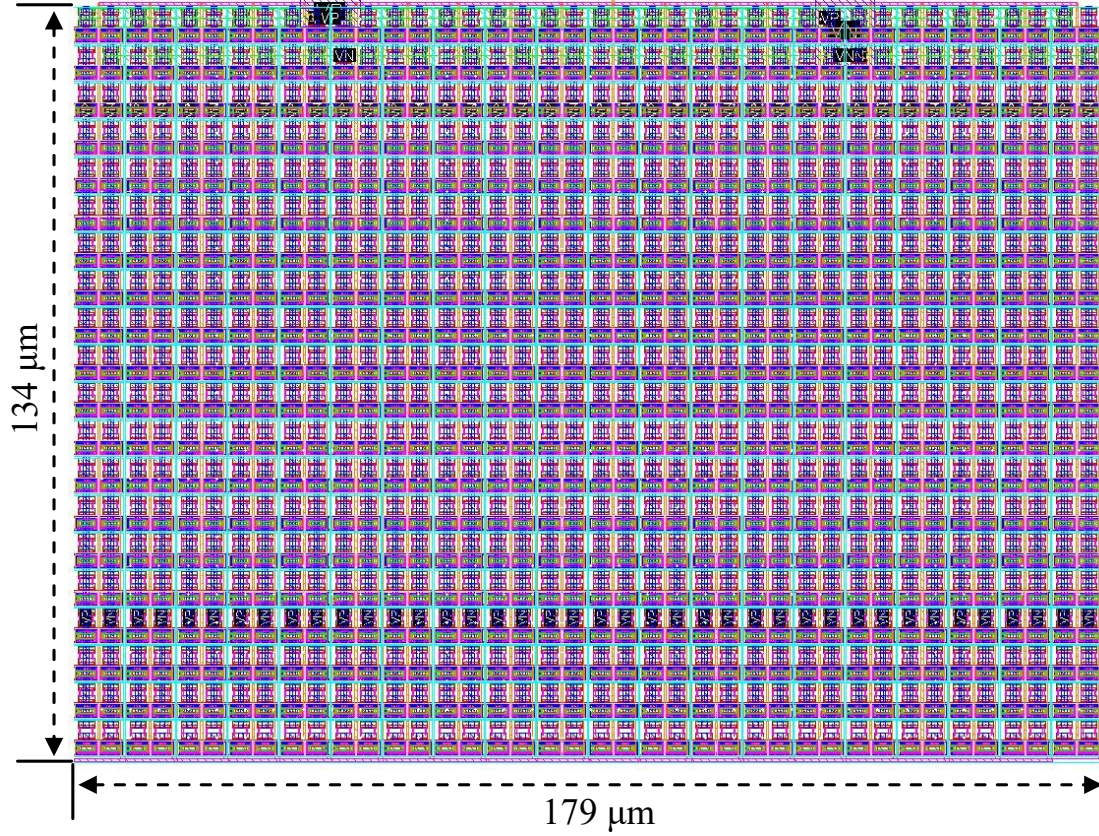


Figure III.2.21 New resized fine-tuning bank with 20×20 fine-tuning units.

Moreover, one can be vaguely aware that the interconnect parasitic capacitance C_{wire} is proportional to the layout area, which is also in line with common sense since a larger layout area often implies more complex internal connections. To verify this point, another resized fine-tuning bank containing 20×20 fine-tuning units is simulated and analyzed, as shown in Figure III.2.21, its total area is $179 \mu\text{m} \times 134 \mu\text{m}$. The post-layout simulation results are given in Table III.2.6. The C_{wire} of this resized fine-tuning bank is calculated to be approximately 196.2 fF, which indicates that the interconnect parasitic capacitance C_{wire} can be reduced by minimizing the layout area. Therefore, a more compact fine-tuning bank is required for a K-band D-DCO design, which means that the layout area of the fine-tuning unit in Figure III.2.19 needs to be further reduced. This will be one of the critical points in the next Section.

Table III.2.6 Post-layout simulation results of the new resized fine-tuning bank.

Parameters	C_{ON}	C_{OFF}	ΔC	Q_{ON}	Q_{OFF}
Fine-tuning bank (20×20)	501 fF	432 fF	69 fF	50	63

III.2.4. Summary

In this Section, we described in detail the circuit implementation and the problems faced by designing the D-DCO.1. The pre-layout simulation results of D-DCO.1 are fully compliant with the design specifications; however, the post-layout simulation results are not satisfactory, mainly due to the large layout area of the fine-tuning bank, which leads to large interconnect parasitic capacitances. Although some measures were taken to optimize the layout, they were still insufficient. Therefore, some other unique methods are still required to further reduce the layout area of the 10-bit fine-tuning bank. In addition, other modules in D-DCO.1, such as the coarse-tuning bank and the cross-coupled pair, also need to be further optimized in order to reduce their own parasitic capacitances and to compensate for the performance degradations that may be caused by these parasitic capacitances. Based on these points, we propose a second version of D-DCO, named D-DCO.2, in the following Section.

III.3. Second Version of D-DCO (D-DCO.2)

In this section, we will highlight some of the crucial parameters and performances of D-DCO.2, as well as some essential modifications relative to the D-DCO.1. The transition from D-DCO.1 to D-DCO.2 shows in detail the whole design process and difficulties of D-DCO.

III.3.1. Circuit Implementation of the Proposed D-DCO.2

III.3.1.1. Block Diagram of the K-Band D-DCO.2

As shown in [Figure III.3.1](#), the structure of D-DCO.2 is basically the same as that of D-DCO.1. However, as the final version of D-DCO, intuitively, two high-speed $\Sigma\Delta$ dithering units are inserted in D-DCO.2, while two diodes are placed under the gates of the cross-coupled pair (N_{10} and N_{11}) to protect their thin gate dielectric from the antenna effect. The main parameters of D-DCO.2 are given in [Table III.3.1](#). Several other notable differences can be noted:

- The tail current (I_{T2}) and width-to-length ratio (W/L) of the cross-coupled pair are significantly increased. In D-DCO.1, we separately simulate different process corners, different voltages, and different temperatures without considering the worst case (ss

corner, low voltage, high temperature), and the gain of D-DCO.1 has reached its limit value. Therefore, for D-DCO.2, it is necessary to further increase its gain to compensate for the PVT variations in the worst case.

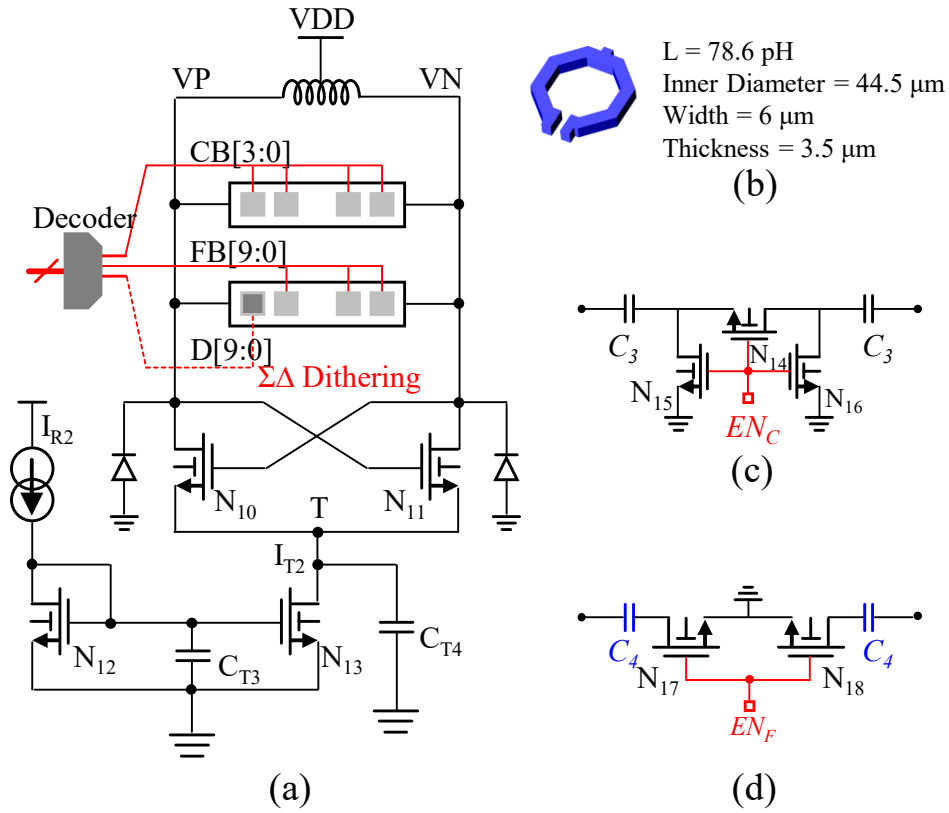


Figure III.3.1 (a) Block diagram of the proposed D-DCO.2. (b) Center-tapped inductor and its main parameters. (c) Schematic of the coarse-tuning unit. (d) Schematic of the fine-tuning unit.

Table III.3.1 Main parameters of the proposed D-DCO.2

VDD	I_{R2}	$N_{10,11}$	N_{12}	N_{13}	N_{14-16}
1.2 V	2 mA	60 $\mu\text{m}/100$ nm	400 $\mu\text{m}/1$ μm	4000 $\mu\text{m}/1$ μm	20 $\mu\text{m}/20$ nm
$N_{17,18}$	C_3	C_4	C_{T3}	C_{T4}	L
2.4 $\mu\text{m}/20$ nm	34.2 fF	973 aF	21.4 pF	38.2 pF	78.6 pH

- The channel length of the cross-coupled pair is increased from 70 nm to 100 nm. The nominal voltage (V_{ds} and V_{gs}) for the transistors with a minimum channel length of 70 nm is 1.2 V, while the nominal voltage for the transistors with a minimum channel length of 100 nm is 1.5 V. Considering the supply voltage of 1.2 V and the requirement to achieve better phase noise performances, the maximum value of the

output voltage swing of the DCO is typically required to be 1.8 V or higher. Thus, the transistors with a channel length of 100 nm can better compensate for the lifetime degradation caused by the HCI (hot-carrier injection) effect.

- The width-to-length ratio (W/L) of the current mirror (N_{12} and N_{13}) is doubled. Although this leads to a larger layout area, the flatness of the drain-source current in its saturation region is further improved as the channel length modulation effect is suppressed, thereby providing a more stable tail current.
- The channel length of the MOS switches (N_{14-16} , $N_{17,18}$) in the coarse- and fine-tuning units is reduced from 70 nm to 20 nm. This initiative can further reduce the layout area, especially for the fine-tuning bank. Moreover, the performances of the switches can be improved because the parasitic resistance of the switches is inversely proportional to their channel lengths. However, this requires a digital control voltage of 0.8 V as the thin-oxide devices have a nominal voltage of 0.8 V.

Moreover, the coarse-tuning unit is shown in [Figure III.3.1\(c\)](#), which achieves a capacitance ratio of 17.25 fF/7.04 fF and a Q -factor ratio of 82/25 using a large series MOM capacitor of 34.2 fF. The 4-bit coarse-tuning bank (CB[3:0]) incorporates 15 such coarse-tuning units to cover the frequency range of 19.18 – 21.17 GHz for PVT compensation, resulting in an average coarse frequency resolution of 133 MHz.

As shown in [Figure III.3.1\(d\)](#), the 10-bit fine-tuning bank (FB[9:0]) incorporates 961 fine-tuning units. Ideally, they allow to cover the entire 19 – 20.25 GHz FMCW chirp with a constant fine frequency resolution, thus avoiding the complex gain calibration required in the T-DCO. In addition, a small single-turn center-tapped inductor of 78.6 pH is selected to leave enough margin for the large fine-tuning bank. This inductor features a Q -factor of about 20 at 20 GHz.

III.3.1.2. Fine-Tuning Bank Using a Novel Customized MOM Capacitor

Implementing a fairly large fine-tuning bank faces several significant trade-offs: Q -factor, frequency resolution, FTR, and parasitic capacitances. The same structure of two NMOS switches as the fine-tuning unit of the D-DCO.1 is used to attain a high Q -factor, thereby ensuring excellent PN performances. The frequency resolution can be flexibly configured by changing the size of the NMOS switches (parasitic capacitance in the OFF-state). The resonant frequency of about 20 GHz requires that the total capacitance of the fine-tuning unit must not exceed 1 fF. However, the capacitance value of the smallest capacitor that the standard library can provide is 2.63 fF. Therefore, in the fine-tuning

layer metal (fifth layer) is deployed to reduce the substrate coupling capacitance. A shield is placed at its bottom and serves to maintain a stable capacitance value. Furthermore, this customized capacitor is characterized by the 2-port S-parameters, and its simplified equivalent π model is illustrated in Figure III.3.2(b). The parasitic parameters extracted by Momentum show a main capacitance C_s of 819.7 aF, a series resistance R_s of 33 m Ω , and coupling capacitances C_{p1} and C_{p2} are 152.7 aF and 107.7 aF, respectively. The total capacitance is ~ 973 aF.

The layout of the fine-tuning unit with the customized capacitors is shown in Figure III.3.3(a), the layout area is $2.8 \mu\text{m} \times 5.56 \mu\text{m}$, which is only 29 % of the layout area of the fine-tuning unit used in D-DCO.1 (Figure III.2.19). In addition, the layout of the 10-bit fine-tuning bank is shown in Figure III.3.3(b), the layout area is $98 \mu\text{m} \times 234 \mu\text{m}$, which is about 40 % of the layout area of the fine-tuning bank in D-DCO.1 (Figure III.2.20). Meanwhile, simulation results show that this new fine-tuning unit achieves a capacitance ratio of 380 aF/536 aF (i.e., a capacitance difference of 156 aF) and a Q -factor ratio of 140/88. In addition, the electrostatic discharge (ESD) effect caused by long digital control lines, especially high-frequency $\Sigma\Delta$ dithering control lines, is avoided by placing diodes under the common gate of NMOS switches.

III.3.2. Pre-Layout Simulation Results

Table III.3.2 gives the DC operating points of the cross-coupled pair ($N_{10,11}$) and the current mirror ($N_{12,13}$) in the D-DCO.2. The transconductance provided by the single-side transistors of the cross-coupled pair has increased to 38.34 mS. Moreover, the tail current is around 19.93 mA, which is quite close to the ideal current of 20 mA, meaning that the current mirror operates well in the saturation region.

Table III.3.2 DC operating points of the transistors N_{10-13} .

Parameters	id	vth	vds	vgs	gm
$N_{10,11}$	9.964 mA	409.2 mV	831 mV	834.6 mV	38.34 mS
N_{12}	2 mA	375.7 mV	553 mV	553.1 mV	20.34 mS
N_{13}	19.93 mA	375.8 mV	361.6 mV	553.1 mV	202.6 mS

When the fine-tuning code is 481, the frequency-code characteristic of the coarse-tuning bank is plotted in Figure III.3.4. The D-DCO.2 oscillates from 24.27 GHz to 21.04 GHz when the coarse-tuning code changes from 0 to 15, resulting in a coarse-tuning range

of 3.23 GHz and an average coarse-tuning step of about 215 MHz. Meanwhile, the frequency-tuning step decreases as the oscillation frequency drops, and the maximum frequency step for the lowest code value $CB = 0$ is about 268 MHz, the minimum frequency step for the highest code value $CB = 15$ is about 151 MHz.

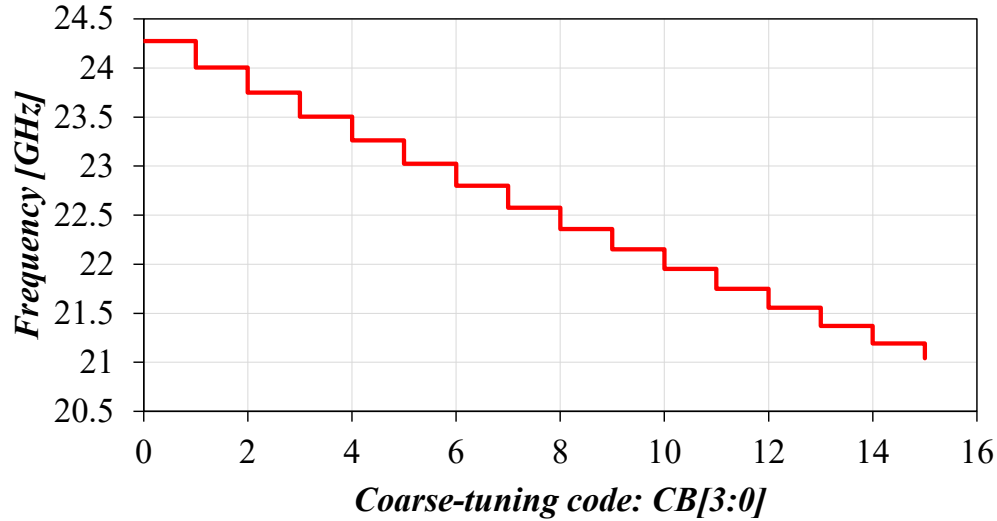


Figure III.3.4 Frequency-code curve of the coarse-tuning bank when $FB = 481$.

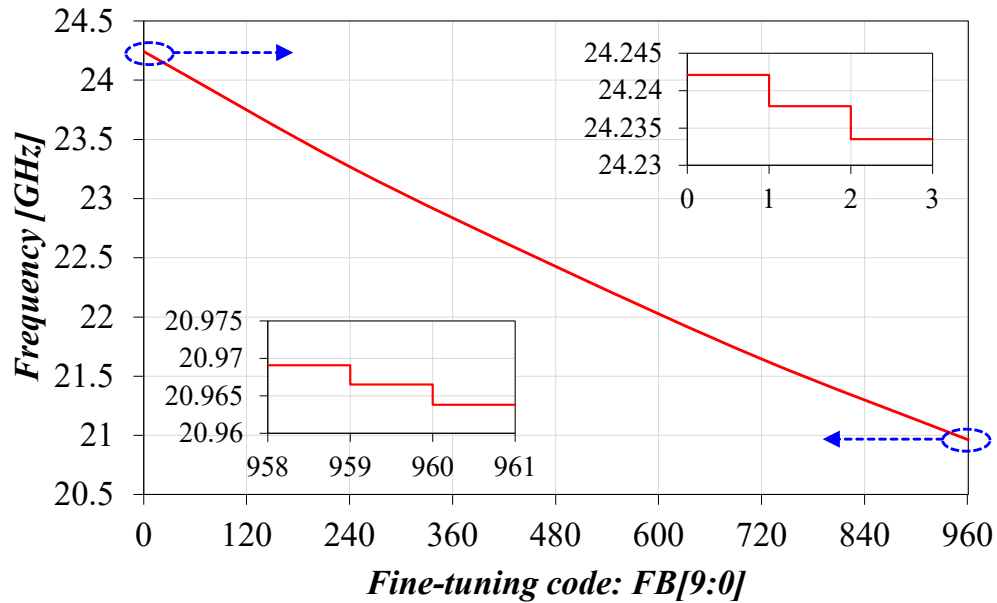


Figure III.3.5 Frequency-code curve of the fine-tuning bank when $CB = 8$.

The frequency-code characteristic of the fine-tuning bank when $CB = 8$ is plotted in Figure III.3.5. A continuous frequency tuning range of about 3.28 GHz (20.96 – 24.24 GHz) can be achieved by relying only on the fine-tuning bank. Note that the fine-tuning

resolution is also not constant in practice, it decreases gradually as the total capacitance increases, and its average value is ~ 3.4 MHz. Nevertheless, due to the absence of frequency overlap in the frequency-modulated band, D-DCO.2 can generate a high-linear FMCW chirp with a simpler and more accurate gain calibration algorithm.

III.3.3. Post-Layout Simulation Results

The top layout view of the proposed D-DCO.2 is shown in Figure III.3.6. It can be noticed that the 10-bit fine-tuning bank occupies a large area, resulting in a 50 % increase in the area of the D-DCO.2 compared to the T-DCO presented in Chapter II. The total area of the D-DCO.2 is $196 \times 469 \mu\text{m}^2$. Moreover, the center-tapped inductor, coarse-tuning bank, fine-tuning bank, and current mirror are arranged in sequence to form the core of the D-DCO.2. The large tail capacitors are symmetrically distributed on both sides and bottom of the D-DCO.2 core for noise filtering.

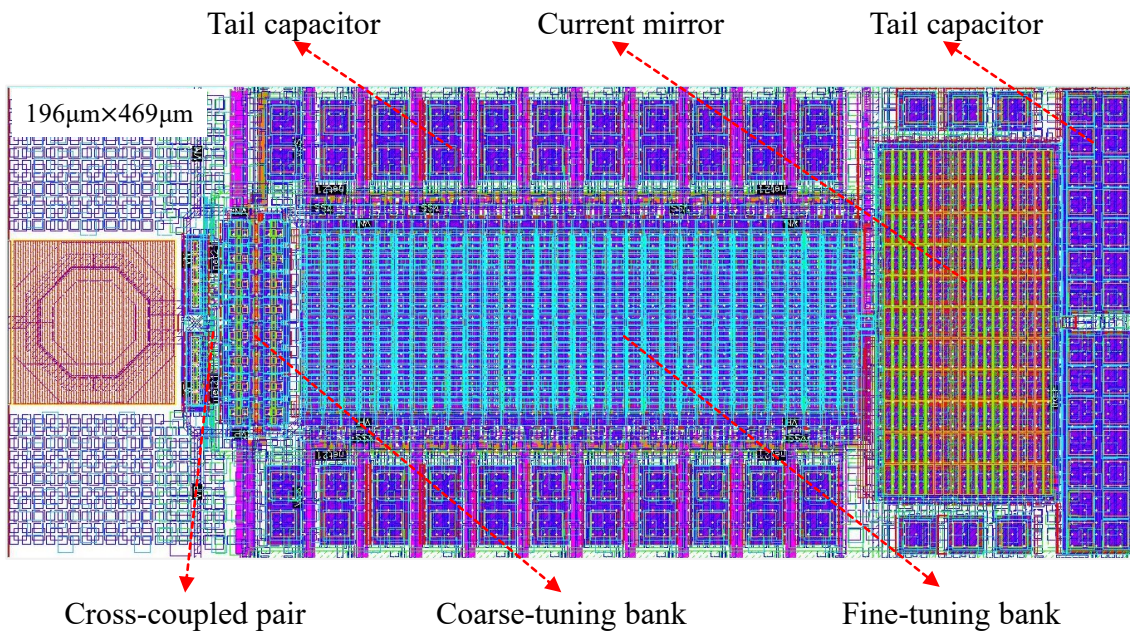


Figure III.3.6 Top layout view of the proposed D-DCO.2.

The post-layout simulated frequency-code characteristic of the coarse-tuning bank is plotted in Figure III.3.7. As with the pre-layout simulation, the frequency-tuning step is gradually narrowed with the increase of the coarse-tuning code. The coarse-tuning bank covers a frequency range of 1.99 GHz (19.18 – 21.17 GHz), and the average coarse frequency resolution is ~ 133 MHz.

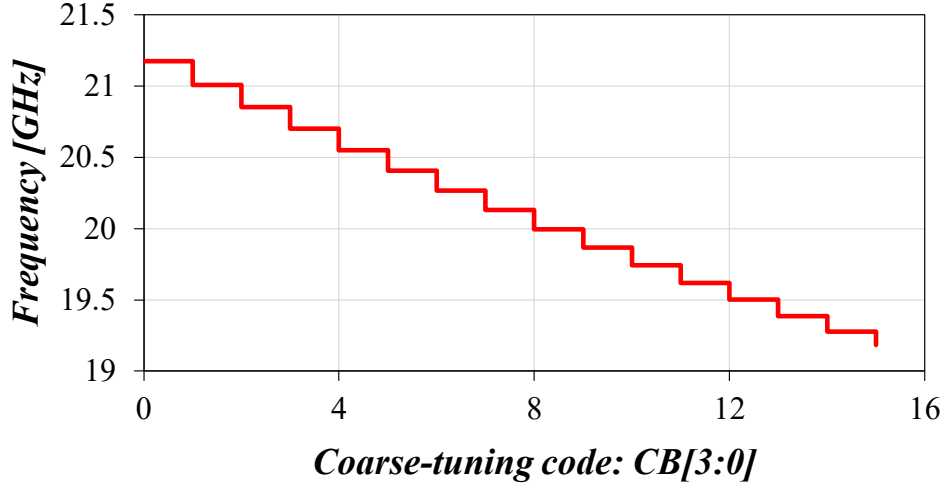


Figure III.3.7 Frequency-code curve of the coarse-tuning bank when $FB = 481$.

In addition, compared with the fine-tuning range of 3.28 GHz in the pre-layout simulations, [Figure III.3.8](#) indicates that for a fine-tuning code varying from 0 to 960, the range is dramatically reduced to 2 GHz (19.12 – 21.12 GHz) and the average frequency resolution becomes ~ 2.1 MHz due to the large parasitic capacitances introduced by the fine-tuning bank, the cross-coupled pair and the interconnects, etc. Nevertheless, the combination of these two banks still enables D-DCO.2 to cover a frequency band from 18.37 GHz to 22.44 GHz, leading to a comparable FTR of 20 % with the T-DCO.

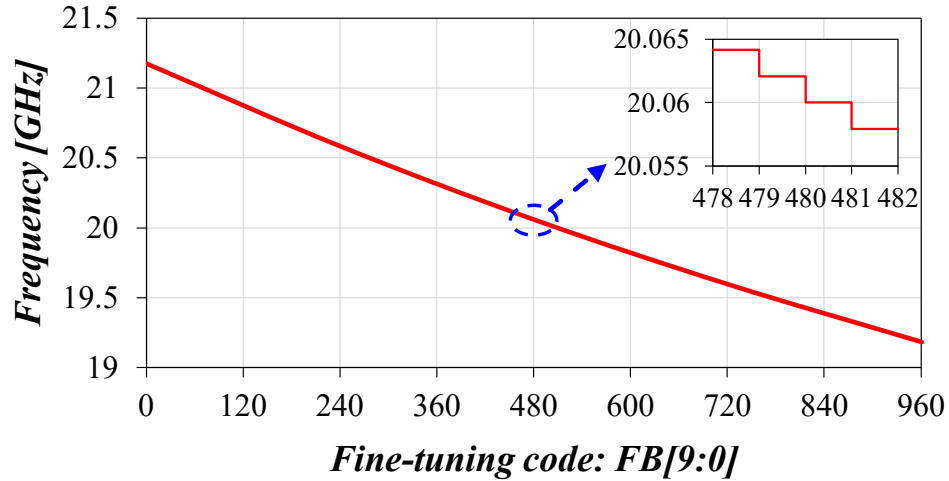


Figure III.3.8 Frequency-code curve of the fine-tuning bank when $CB = 8$.

The PN performances of the D-DCO.2 for the minimum, medium, and maximum oscillation frequencies are shown in [Figure III.3.9](#). At the medium frequency of 20.06 GHz ($CB = 8$, $FB = 481$), the PN at 1 MHz frequency offset is -113.04 dBc/Hz. The worst

PN occurs at the maximum frequency of 22.44 GHz (CB = 0, FB = 0), which is -111.483 dBc/Hz at 1 MHz frequency offset.

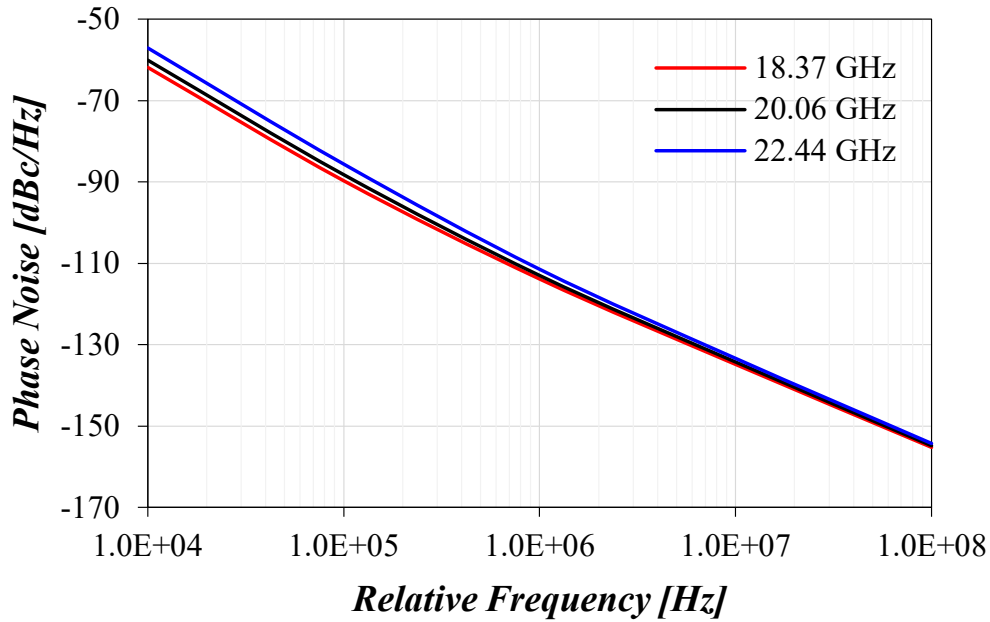


Figure III.3.9 Simulated phase noise plot at the minimum frequency of 18.37 GHz, the medium frequency of 20.06 GHz, and the maximum frequency of 22.44 GHz.

Table III.3.3 indicates that in the worst case and the best case, the medium frequency variation of the D-DCO.2 does not exceed 1.1 GHz due to its large total capacitance, which is significantly smaller than that of the T-DCO. The coarse-tuning range of 1.99 GHz available from the D-DCO.2 can fully accommodate PVT variations. In addition, the FTR also remains similarly around 20%. In the worst case, the PN varies by no more than 4 dB and still reaches -109.13 dBc/Hz at 1 MHz frequency offset.

Table III.3.3 Post-layout simulated D-DCO.2 performances for the three most representative PVT configurations.

D-DCO.2	Worst case	Typical case	Best case
Configuration	125°, ss, 1.14 V	27°, tt, 1.2 V	-25°, ff, 1.26 V
Minimum Frequency (CB = 15, FB = 961)	17.29 GHz	18.37 GHz	19.51 GHz
Medium Frequency (CB = 8, FB = 481)	19.13 GHz	20.04 GHz	21.12 GHz
Maximum Frequency (CB = 0, FB = 0)	21.5 GHz	22.44 GHz	23.34 GHz
FTR	21.7 %	20 %	18.3 %
PN@1MHz (CB = 8, FB = 481)	-109.13 dBc/Hz	-113.04 dBc/Hz	-112.92 dBc/Hz

III.3.4. Comparative Study

Table III.3.4 compares the post-layout simulated performances of the D-DCO.2 with the specifications. In general, the proposed D-DCO.2 almost meets the design specifications.

Table III.3.4 D-DCO.2 performances vs DCO specifications.

Parameters	DCO Specifications			D-DCO.2 Performances			Units
	Minimum	Typical	Maximum	Minimum	Typical	Maximum	
temperature	-25°		125°	-25°		125°	
dvdd		0.8			0.8		V
avdd_reg	0.85	0.9	0.95	1.14	1.2	1.26	V
ibias_prog		4					bits
icc_on			60		20		mA
icc_off			1				mA
frequency	19		20.25	18.37	20.04	22.44	GHz
supply voltage		1			1.2		V
coarse step		200			133		MHz
fine step		2.5			2.1		MHz
chirp range		2.5			2		GHz
phase noise		-115		-113.9	-113	-111.5	dBc/Hz
		-135		-134.8	-134.3	-133.4	dBc/Hz
		-155		-155.2	-154.9	-154.3	dBc/Hz
Ton		50					ns

The performances of the proposed D-DCO.2 compared with the state-of-the-art and the T-DCO are presented in Table III.3.5. To the best of our knowledge, only few K-band DCOs have been published so far. The DCO presented in [III-1] is a dual-band design with a minimum frequency resolution of ~187 MHz, which does not meet the specifications of FMCW automotive radar. No less than three switched-capacitor banks are employed in [III-2]-[III-4], which is similar to the proposed T-DCO and requires complex frequency calibration algorithms to generate FMCW chirps. Moreover, it should be noted that the more switched-capacitor banks in the DCO, the higher the complexity of the algorithm. Therefore, unlike the above published DCOs, the proposed D-DCO.2 solely relies on the fine-tuning bank to completely cover the frequency range of the

FMCW chirp. The trade-off between frequency resolution and FTR, as well as the issue of interconnect parasitic capacitances caused by the large size of the fine-tuning bank, are also well addressed. Subsequently, the D-DCO.2 no longer needs to constantly switch between different switched-capacitor banks to generate linear FMCW chirps.

Table III.3.5 Comparison with the state-of-the-art K-band DCOs.

Reference	Technology	Frequency [GHz]	FTR [%]	P _{DC} [mW]	PN ^c [dBc/Hz]	FoM ^c [dBc/Hz]	FoM _T ^c [dBc/Hz]
[III-2] ^a LMWC 2021	28 nm	24.4	27.2	1.2	-97	-184	-193
[III-5] ^a JSSC 2018	28 nm	27.3	14	12	-106	-184	-187
[III-1] ^a TMTT 2019	65 nm	23.7	24.4	4.8	-106.6	-187.2	-194.9
[III-3] ^b TVLSI 2019	65 nm	24	29	16.9	-104	-179	-188
[III-4] ^a JSSC 2018	65 nm	24.6	17	10	-102	-180	-184
T-DCO ^b	22 nm	19.61	23.4	24	-112.6	-184.65	-192.03
D-DCO.2^b	22 nm	20.06	20	24	-113.04	-185.64	-191.67

^a: measured results; ^b: post-layout simulation results; ^c: @ $\Delta f=1\text{MHz}$

III.3.5. Summary

The proposed D-DCO.2 features a wide FTR of 20 % and a low PN of -113.04 dBc/Hz at the medium frequency of 20.06 GHz. Post-layout simulation results indicate that it is capable of operating in the harshest environment, i.e., the worst case (125°, ss corner, 1.14 V). The construction of the FMCW chirp solely relies on the fine-tuning bank, and the frequency overlap problem in conventional muti-bank DCOs is no longer present. Meanwhile, the 961 fine-tuning units employ the novel customized interdigitated MOM capacitor of about 973 aF, thereby enabling a fine frequency resolution of ~2.1 MHz and a fine-tuning range of ~2 GHz. Moreover, the D-DCO.2 consumes about 24 mW from a 1.2 V supply voltage, leading to a FoM of -185.64 dBc/Hz and a FoM_T of -191.67 dBc/Hz. It is implemented in a 22 nm FD-SOI technology, and the occupied area is $196 \times 469 \mu\text{m}^2$.

III.4. Conclusion

In Section III.1, we briefly described the main objectives of designing a K-band D-DCO to address the frequency overlap and calibration issues in multi-bank DCOs, and also introduced the main challenges of D-DCO design. In Section III.2, we presented the initial version of the D-DCO using standard components from the process library. Unfortunately, this design suffered from large interconnect parasitic capacitances introduced by the large size of the fine-tuning bank. Despite a series of layout optimization efforts, its performances were still far from meeting the specification requirements. Therefore, in Section III.3, we proposed an alternative version of the D-DCO. The issues such as large parasitic capacitances were well addressed by using customized tiny MOM capacitors. Post-layout simulation results show that this version of the D-DCO almost meets the design specifications.

III.5. Résumé du Chapitre III

Dans le Chapitre III, nous avons étudié une architecture alternative d'OCN dédié aux radars automobiles FMCW. En effet, l'intégration d'un OCN conventionnel basé sur une structure à multiples banques de capacités commutées (plus de trois banques, similaire au T-OCN) dans une ADPLL s'avère complexe à mettre en œuvre car la génération d'un chirp linéaire avec une bande supérieure à 1 GHz nécessite un processus complexe et long d'étalonnage et de linéarisation du gain de l'OCN. Dans le cas d'un étalonnage, les résultats doivent être stockés en mémoire et l'étalonnage doit être répété périodiquement pour compenser les variations du PVT. Par conséquent, nous avons proposé un prototype d'OCN à seulement deux banques de capacités commutées (D-OCN) qui peut résoudre les problèmes susmentionnés au niveau « hard » plutôt qu'au niveau « soft », et, à notre connaissance, pratiquement aucun OCN de ce type n'a été publié jusqu'à présent.

Ainsi, dans la Section III.1, nous avons d'abord décrit brièvement le D-OCN en bande K proposé pour répondre aux spécifications requises. Alors que la banque de réglage grossier n'est encore utilisée que pour compenser les variations de PVT, la génération d'un chirp linéaire repose entièrement sur une seule banque de réglage fin du D-OCN, ce qui signifie que le problème de chevauchement de fréquence n'existe plus, réduisant ainsi significativement la complexité de l'algorithme d'étalonnage.

Dans la Section III.2, nous avons détaillé les problèmes rencontrés lors de la conception du circuit de la première version du D-OCN, à savoir le D-OCN.1. Il convient de noter que la conception du D-OCN.1 est entièrement basée sur des composants de la bibliothèque de process 22 nm FD-SOI utilisé. En outre, le chirp est généré par une banque de réglage fin de 10 bits seulement et qui se compose de 961 unités de réglage fin. Étant donné que la plus petite capacité disponible dans le PDK a une valeur de 2.66 fF, l'utilisation de seulement deux de ces capacités dans une unité de réglage fin entraînerait une grande valeur de capacité totale de la banque de réglage fin et empêcherait le D-OCN.1 d'osciller dans la bande K. Pour cette raison, nous avons utilisé quatre capacités de ce type en série dans l'unité de réglage fin afin d'obtenir une faible valeur de capacité. Dans ces conditions, les résultats de la simulation pré-layout du D-OCN.1 était entièrement conformes aux spécifications. Cependant, les résultats de simulation post-layout prouvent que cette conception n'est pas réalisable, la raison principale étant que la grande surface de la banque de réglage fin entraîne une grande capacité parasite d'interconnexion, ce qui rend le D-OCN.1 incapable d'osciller dans la bande K.

Dans la Section III.3, nous avons ensuite présenté la deuxième version du D-OCN, à savoir le D-OCN.2. La banque de réglage fin de 10 bits contient également 961 unités de réglage fin. Afin de réduire la surface occupée par la banque de réglage fin, nous avons conçu une nouvelle capacité MOM interdigitée d'environ seulement 973 aF, ce qui permet de n'utiliser que deux capacités dans chaque unité de réglage fin. En outre, nous avons encore réduit la surface du layout, par exemple en partageant le substrat des commutateurs MOS. Ces opérations diminuent considérablement les capacités parasites des interconnexions, rendant ainsi possible la conception d'un D-OCN en bande K. Enfin, les résultats de simulation post-layout du D-OCN.2 montrent que sa banque de réglage fin permet d'obtenir une largeur de bande d'environ 2 GHz et une résolution de fréquence fine d'environ 2.1 MHz. Parallèlement, à une fréquence moyenne de 20.06 GHz, le D-OCN.2 permet d'obtenir une large plage de réglage de la fréquence d'environ 20 % et un faible bruit de phase de -113.04 dBc/Hz à 1 MHz de la porteuse. De plus, le D-OCN.2 consomme environ 24 mW sous une tension d'alimentation de 1.2 V, ce qui conduit à une FoM de -185.64 dBc/Hz et une FoM_T de -191.67 dBc/Hz. Il est implémenté en technologie 22 nm FD-SOI et occupe une surface de 196×469 μm².

En conclusion, le D-OCN.2 proposé répond presque aux exigences des spécifications. Comme le T-OCN, le D-OCN.2 est également robuste aux variations de PVT. En outre,

dans un cas typique (27°, tt corner, 1.2V), le D-OCN.2 atteint des performances en bruit de phase à l'état de l'art et inférieures à -110 dBc/Hz à 1 MHz de la porteuse sur l'ensemble de la plage de fréquence, tout en permettant une large plage de réglage de fréquence d'environ 20 %. Enfin, le prototype D-OCN est plus adapté aux radars automobiles FMCW que les prototypes OCN à multiple banques conventionnels, ce qui est très important pour la recherche et le développement futurs dans ce domaine.

III.6. References

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General Conclusion

The 76 – 81 GHz FMCW automotive radar has gained significant attention due to its importance in the development of ADAS and autonomous driving technologies. The 76 – 81 GHz frequency band provides a good balance between range, resolution, and sensitivity, making it highly desirable for automotive applications. Meanwhile, FMCW technology enables accurate and reliable real-time object detection and distance measurement. Furthermore, the automotive industry's demand for advanced safety features, as well as the increasing popularity of electric and hybrid vehicles, further promote the widespread adoption of automotive radars.

As a critical component of FMCW radar systems, the PLL is used to generate a stable oscillation frequency, which is then used to generate the modulation frequency of the radar. Compared with traditional analog PLLs, ADPLLs offer several advantages, including the ability to be integrated with digital systems, lower power consumption, and ease scalability to advanced CMOS technologies. In addition, ADPLLs can be easily programmed and reconfigured to adapt to variations in operating conditions. This makes ADPLLs more robust and reliable, particularly in harsh environments, which is critical for safety-critical applications such as automobiles. Therefore, ADPLLs have become an increasingly popular choice in modern frequency synthesis systems.

The implementation of a DCO is a necessary step in the design of ADPLLs. Some critical issues in DCO design have been largely solved in the field of wireless communications below 10 GHz. However, the possibility of obtaining a K-band DCO with a high spectral purity applicable to FMCW automotive radar remains to be proven. Therefore, the main goal of this thesis was to implement a wideband low-phase-noise K-band DCO in an advanced 22 nm FD-SOI process. To achieve this goal, we first studied some classical oscillator theories to understand the strengths and weaknesses of each design. Meanwhile, compromises must be made in DCO design, such as phase noise, power consumption, and frequency tuning range. According to the specifications, the phase noise of the DCO should be extremely low, reaching about -115 dBc/Hz at 1MHz frequency offset from a carrier frequency of about 20 GHz, the frequency-tuning range should be about 20 % with a frequency resolution as low as 2.5 MHz, and the requirement to operate under high-temperature conditions should also be met, which are the most

challenging aspects of the DCO design.

In Chapter I, we introduced the research background from three topics. We first briefly reviewed automotive radars, including the radar fundamentals, autonomous driving technologies, and the selection of frequency bands and processes of automotive radars. Several representative examples of 76 – 81 GHz FMCW automotive radars and their performance summaries were also presented. Secondly, we reviewed several different frequency synthesis technologies, focusing on explaining the principles, structures, and advantages and disadvantages of PLL and ADPLL. Finally, we described the operating principles and structure of different types of oscillators, different electronic noise sources, and the effects of these noise sources on oscillators' phase noise performances. These literature reviews are necessary because they not only help us to understand the current status and trends in the field of automotive radar and the necessity of ADPLL research, but also the introduction of oscillator theory greatly contributes to the analysis of DCOs.

In Chapter II, we focused on the circuit design and implementation of the K-band T-DCO. We first provided a brief introduction of the GlobalFoundries' 22 nm FD-SOI process and common types of DCOs. To achieve low phase noise, we ultimately selected an LC-based DCO architecture. We also compared various types of frequency tuning techniques to determine which structures were more suitable for our designs. In addition, considering the DCO specifications, we adopted a conventional multi-stage switched-capacitor structure, which allows to achieve both a wide frequency-tuning range and a fine frequency resolution with a small number of switched-capacitor units. We also introduced the principle of FMCW radars and existing DCO gain calibration techniques for generating linear chirp signals. Moreover, in the proposed T-DCO prototype, the coarse-tuning tank is mainly used to compensate for PVT variations, while the medium- and fine-tuning banks work together to cover the chirp range. We also proposed a novel back-gate-based fine-tuning structure that allows for a small capacitance step of approximately 63 aF and a fine frequency resolution of about 1.38 MHz around 20 GHz. Furthermore, the proposed T-DCO achieves a frequency-tuning range of about 23.4 % and a low phase noise of -112.6 dBc/Hz at 1 MHz frequency offset for a medium frequency of 19.61 GHz. Although the phase noise achieved by this T-DCO has not yet reached the set target, the post-layout simulation results demonstrate that it is still the best among its counterparts.

In Chapter III, we investigated another DCO prototype dedicated to FMCW automotive radars. Indeed, when the modulation bandwidth is wide, it is challenging to integrate a conventional DCO based on a multi-stage (more than three banks, similar to the T-DCO) switched-capacitor structure into an ADPLL, and complex and lengthy DCO gain calibration and linearization are required to obtain a linear frequency-modulated band beyond 1 GHz. In the case of offline calibration, the results must be stored in memory and the calibration must be repeated periodically to compensate for the variations. Based on these facts, we proposed a D-DCO prototype that allows to address the above issues at the design level rather than only at the algorithm level, and to our knowledge, this prototype has barely been disclosed before. In the proposed D-DCO, the coarse-tuning bank is still used only to compensate for PVT variations, while the wide chirp signal relies entirely on the 10-bit fine-tuning bank to be generated. The fine-tuning bank contains 961 fine-tuning units and a novel customized interdigitated MOM capacitor of about 973 aF is used to reduce interconnect parasitic capacitances. Finally, the fine-tuning bank allows to achieve a linear chirp band of about 2 GHz with a fine frequency resolution of about 2.1 MHz. Meanwhile, the proposed D-DCO achieves a wide frequency-tuning range of about 20 % and a best-in-class phase noise of -113.04 dBc/Hz at 1 MHz frequency offset for a medium frequency of 20.06 GHz.

Overall, the proposed T-DCO and D-DCO almost meet the specification requirements. Our research work has confirmed the feasibility of designing K-band low-phase-noise DCOs in 22 nm FD-SOI for 76 – 81 GHz FMCW automotive radars. Moreover, the novel back-gate-based switched-capacitor structure proposed in the T-DCO has significant implications for achieving fine frequency resolution in a DCO design. Furthermore, we addressed some key issues in the D-DCO design, such as large parasitic capacitances. Since the D-DCO prototype is more suitable for FMCW automotive radar applications than traditional multi-bank DCO prototypes, it is of great importance for future research and development in this field.

List of Publications

- Z. Li, D. Cordeau, J.-M. Paillot, S. Charpentier, M. Lécuyer, and F. Huin, "Analysis and design of K-band low-phase-noise differential DCOs implemented in 22 nm FD-SOI for 76–81 GHz automotive radars," *Microelectronics J.*, p. 105780, 2023, doi: <https://doi.org/10.1016/j.mejo.2023.105780>.
- Z. Li, D. Cordeau, J. -M. Paillot, S. Charpentier, M. Lécuyer and F. Huin, "A K-band Wide-Tuning-Range Low-Phase-Noise Digitally Controlled Oscillator in 22 nm FD-SOI for Automotive Radars," *2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Glasgow, United Kingdom, 2022, pp. 1-4, doi: 10.1109/ICECS202256217.2022.9971055.
- Z. Li, D. Cordeau, J. -M. Paillot, S. Charpentier, M. Lécuyer and F. Huin, "Conception d'un oscillateur à commande numérique en bande K à faible bruit de phase et à large bande en technologie 22nm FD-SOI pour les radars automobiles," *22èmes Journées Nationales Microondes*, Limoges, France, 07-10 Juin 2022.

Abstract

The millimeter-wave radar is indispensable for realizing vehicle safety and autonomous driving functions, making it one of the current research hotspots. The main objective of this thesis is to implement a K-band low-phase-noise digitally controlled oscillator (DCO) with a frequency tuning range of more than 20 % for an all-digital phase-locked loop (ADPLL), which will be further applied to 76 – 81 GHz frequency-modulated continuous-wave (FMCW) automotive radars. Two different solutions are proposed. The first is a triple-bank DCO (T-DCO). Its coarse-tuning bank is mainly used to compensate for the PVT variations, while the medium- and fine-tuning banks work together to cover the frequency modulation bandwidth, thus requiring a frequency overlap of more than 15 % like conventional DCOs. Thanks to the proposed novel back-gate-based fine-tuning structure, the T-DCO achieves a fine frequency resolution of 1.38 MHz at a carrier frequency of approximately 20 GHz. The second is a dual-bank DCO (D-DCO), which solely relies on a large 10-bit fine-tuning bank to generate frequency-modulated signals. This original approach allows us to address the issue of frequency overlap and calibration in multi-bank DCOs (more than three frequency-tuning banks, similar to the T-DCO) from the design level rather than only from the algorithm level, thereby making it more suitable for FMCW automotive radars. Meanwhile, the D-DCO achieves a fine frequency resolution of 2.1 MHz and a fine-tuning range of 2 GHz by employing a novel customized MOM capacitor of 973 aF. Furthermore, both T-DCO and D-DCO are implemented in an advanced 22 nm FD-SOI process, achieving the best-in-class phase noise lower than -110 dBc/Hz over the entire frequency range at 1 MHz frequency offset.

Keywords: Digitally controlled oscillator, DCO, K-band, low phase noise, 22 nm FD-SOI, ADPLL, FMCW, automotive radar.

Résumé

Les radars à ondes millimétriques sont indispensables dans la réalisation de fonctions de sécurité des véhicules et pour la conduite autonome, ce qui en fait l'un des domaines de recherche les plus en vogue actuellement. L'objectif principal de cette thèse est de mettre en œuvre un oscillateur à commande numérique (OCN) en bande K à faible bruit de phase avec une large bande d'accord en fréquence de plus de 20 % pour une boucle à verrouillage de phase entièrement numérique (ADPLL en anglais), qui sera ensuite appliquée aux radars automobiles à ondes continues modulées en fréquence (FMCW en anglais) de 76 à 81 GHz. Deux solutions différentes sont proposées. La première est un OCN à triple banques de capacités commutées (T-OCN), dont la banque de réglage grossier est principalement utilisée pour compenser les variations de PVT, tandis que les banques de réglage moyen et fin permettent de couvrir la largeur de bande de fréquence désirée, nécessitant ainsi un chevauchement des fréquences de plus de 15 % comme dans les OCN conventionnels. En outre, grâce à la nouvelle architecture de réglage fin proposée et basée sur la polarisation de la grille arrière, le T-OCN permet d'obtenir une résolution de fréquence fine de 1.38 MHz à une fréquence porteuse d'environ 20 GHz. Le second est un OCN à double banque (D-OCN), qui s'appuie uniquement sur une banque de réglage fin à grand nombre d'éléments contrôlée sur 10-bit afin de générer des signaux modulés en fréquence. Cette approche originale nous permet de nous affranchir du problème de chevauchement et de calibration de la fréquence indispensable dans le cas des OCNs à plusieurs banques (plus de trois banques de réglage de fréquence, similaire au T-OCN), le rendant ainsi plus adapté à une utilisation dans le domaine des radars automobiles FMCW. Parallèlement, le D-OCN permet d'obtenir une résolution de fréquence fine de 2.1 MHz et une plage de réglage fin de 2 GHz en utilisant une nouvelle capacité MOM personnalisée de 973 aF. De plus, le T-OCN et le D-OCN sont tous les deux implémentés en technologie 22 nm FD-SOI, ce qui permet d'atteindre des performances en bruit de phase à l'état de l'art et inférieures à -110 dBc/Hz à 1 MHz de la porteuse sur l'ensemble de la plage de fréquences.

Mots clés : Oscillateurs à commande numérique, OCN, bande K, faible bruit de phase, 22 nm FD-SOI, ADPLL, FMCW, radars automobiles.