Hole Quantum Dots in Strained Ge/SiGe Quantum-Well Heterostructures

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Hole Quantum Dots in Strained Ge/SiGe Quantum-Well Heterostructures

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"Ante los fenómenos que desfilan por los órganos sensoriales, la actividad del intelecto sólo puede ser verdaderament útil y fecunda reduciendose modestamente a observarlos, describirlos, compararlos y clasificarlos, según sus analogías y diferencias, para llegar después, por inducción, al conocimiento de sus condiciones determinantes y empíricas."
-Santiago Ramón y Cajal

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Résumé

Les points quantiques des semi-conducteurs ont été un domaine de recherche fructueux au cours des 30 dernières années. Les atomes artificiels ouvrent un grand nombre de possibilités. De l'effet quantique orbital à la polarisation de spin, des groupes du monde entier ont mené des études. La publication de DiVicenzo en 1998 soulignait la possibilité de coder des informations quantiques dans les états de spin des charges à l'intérieur de points quantiques semi-conducteurs définis par une grille. Depuis lors, plusieurs démonstrations ont montré que cette possibilité est une réalité, même s'il reste encore pas mal de pierres sur le chemin. Parmi les semi-conducteurs utilisés pour fabriquer des points quantiques, le germanium est un nouveau candidat qui présente un fort potentiel.

Parmi ses propriétés intrinsèques, on trouve une faible interaction hyperfine, due au caractère de type p de sa bande de valence, et un fort couplage spin-orbite. Grâce à ces deux caractéristiques, les états de spin dans les points quantiques ont une longue durée de vie en cohérence et peuvent être pilotés par un champ électrique externe. Dans les hétérostructures de puits quantiques en germanium/silicium-germanium (Ge/SiGe), on obtient des gaz de trous à haute mobilité avec de faibles masses effectives. L'hétérostructure consiste en une couche de germanium (Ge) de 16 nm comprimée entre deux couches de silicium germanium (SiGe). L'alignement de la bande de valence entre les semi-conducteurs crée un puits quantique pour les trous dans la couche de Ge, formant un gaz de trous bidimensionnel (2DHG). L'objectif de cette thèse est de développer une recette de fabrication robuste pour former des points quantiques dans les hétérostructures Ge/SiGe. Plusieurs étapes de gravure au plasma, de dépôt de diélectrique, de lithographies de grille et d'évaporation de métal ont été sondées et optimisées. Une fois la recette obtenue, nous avons fabriqué avec succès des transistors à effet de champ de trous (H-FET), des contacts ponctuels quantiques (QPC), des points quantiques simples (SQD) et des points quantiques doubles (DQD). Nous avons effectué des mesures de transport de ces dispositifs quantiques à basse température. Dans les derniers chapitres, nous avons démontrons la viabilité de la recette pour obtenir des points quantiques simples (SQD) et doubles (DQD), et avons atteint l'état de l'art pour la fabrication de dispositifs quantiques à hétérostructures de Ge. Cette thèse est la base d'une recherche future basée sur des points quantiques à trous en germanium de haute qualité pour explorer la physique de l'interaction spin-orbite, pour réaliser le traitement de l'information quantique avec des qubits à trous et plus...

Abstract

Semiconductor's quantum dots has been a fruitful research field for the last 30 years. Artificial-made atoms open a large amount of possibilities. From orbital quantum effect down to spin-polarization, studies have been carried on from groups all around the world. DiVicenzo's publication in 1998 pointed out the possibility of encoding quantum information in the spin states of charges inside gate defined semiconductor quantum dots. Since then, several demonstrations have shown that this possibility is a reality, even though there are still quite a few stones along the path. Out of the semiconductors used to fabricate quantum dots, Germanium is a new candidate that shows strong potential.

Among its intrinsic proprieties, we find low hyperfine interaction, due to its p-type character of the valence band, and a strong spin-orbit coupling. With these two characteristics, the spin states in the quantum dots have long coherence lifetime and can be driven with an external electric field. In germanium/silicon germanium (Ge/SiGe) quantum well heterostructures, high mobility holes gases with low effective masses are achieved. The heterostructure consists in a germanium (Ge) layer of 16 nm compress between two silicon germanium (SiGe) layer. The valence band alignment between the semiconductor creates a quantum well for holes at the Ge layer, forming a two-dimensional hole gas (2DHG). The purpose of this thesis is developing a resilient fabrication recipe to form quantum dots in Ge/SiGe heterostructures. Several steps of plasma etching, dielectric deposition, gate lithographies and metal evaporation have been probed and optimized. After the recipe was obtained, we successfully fabricated Hole-Field Effect Transistors (H-FET), Quantum Point Contacts (QPC), Single Quantum Dots (SQD) and Double Quantum Dots (DQD). We performed transport measurements of these quantum devices at low temperature. In the last chapters, we probed the viability of the recipe to host SQD and DQD, and reached the state-of-the-art for the Ge heterostructures quantum device fabrication. This thesis is the foundation for a future research based on high quality germanium hole quantum dots to explore the physics of the spin-orbit interaction or to realize quantum information processing with hole spin qubits and more...

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Introduction

It remains unclear who was the first person to construct an atomic theory for Nature. Historically, it was attributed to Democritus, an ancient Greek presocratic philosopher from the fifth century BC. In his book *The Great World-System, Cosmography,On the Planets, On Nature, On the Nature of Man or On Flesh* [1], he claims that everything was made of small, indestructible particles that he called "atoms". Controversy comes when we account for his master and predecessor, Leucippus, who could also have developed an atomic theory. Since none of their books have survived to our days, we only know about them from third-party historians. Around one millennium needed to pass until new theories were born.

In the 17th century, people recovered the atomic theory and continue the research: François Bernier, Walter Charleton, Robert Boyle, John Dalton, Amedeo Avogardo... They started to view solid matter as a conglomerate of atoms, and begin to explain their macroscopic properties from the small scale. It was in the early 1940 when, in the American Physical Society, the term "Solid State Physics" was finally proposed. It merged the new Quantum Theory with the atomic-like definition of matter, creating a new field of research.

On another side of History, we have the technological development of materials. Since the old days, people were studying the properties of solids; electrical conductance, strain, optical properties, etc... From the old pre-historic Iron Age and Bronze Age, to the modern steel and plastic era, material research has always been a motor to technological development in Human Society.

Now days, new technological challenges appear and new solution are proposed. In this thesis, the objective is the development of gate defined quantum dots based on a germanium quantum well. There are several applications for these devices, from qubits for Quantum Computation to current generators in solar cells. Here we will learn how they work, how they are produced and how to characterize them.

Quantum dots as artificial atoms

As it is said in L.P. Kouwenhoven et al. [2], "quantum dots are small man-made structures in a solid, typically with sizes ranging from nanometers to a few microns. They consist of $10^3 - 10^9$ atoms with an equivalent number of electrons. In semiconductors all electrons are tightly bound to the nuclei except for a small fraction of free electrons. This small number can be anything from a single, free electron to a puddle of several thousands in quantum dots defined in a semiconductor". The characteristic of few isolated electrons in a confinement potential has given to quantum dots the name of "artificial atoms" [2, 3]. They also resemble in the formation of discrete energy spectrum. Same as in real atoms, the symmetries in the QD electric confinement lead to an orbital degeneracy known as shells (1s, 2s2p, 3s3p3d...). Electron's wave functions must be well-defined according to these orbital levels. Same way that a single QD forms an artificial atom, two QDs coupled together form an artificial molecule [4]. If the nature of the coupling is more capatitance coupling than tunnel coupling, the artificial molecule would replicate an ionic bonding. If the tunnel coupling strength excess the capacitance coupling, it would simulate a covalent bonding. Instead of using light interaction to study the atom-like properties of the QDs, they are observed with transport measurement [5, 6]. QDs research field is being very active and fruitful since the first experiments in the late eighties [7]. The range of phenomena starts with artificial atoms and coupled quantum systems, pass by quantum Chaos and quantum Hall effect, and finishes with Quantum Computation and quantum sensors.

Since the first QDs were fabricated, a large variety of architectures have been tested. The classification of these architectures can be done by its dimension. In the 0-dimensional materials, we can find self-assembled quantum dots with GaAs or InAs [8], or with Si and Ge [9]. In the 1-dimensional architectures there are nanopillars made of PbS, Si and CdS/CdTe, strongly used in solar cell research [10, 11]. Same way, III-IV semiconductors [12], Si and Si/Ge nanowires [13, 14] and CMOS nanowires [15] have been developed. We can also find 1-dimensional QDs in carbon nanotubes [16, 17]. As 2-dimensional QDs, we can find quantum well structures in type III-IV semiconductors [18–20], in bilayer graphene [21], in SiMOS structures [22, 23] and finally, in Si/Ge heterostructures [24, 25].

Ge, the chosen semiconductor

This thesis' research is about the QD's fabrication and characterization in Ge/SiGe quantum well heterostructures. The heterostructures consists in a Ge layer of 16 nm compress between two layers of SiGe. A 2DHG is formed in the Ge. Figure 1 shows a schematic of the Ge/SiGe heterostructure.

Ge is not chosen randomly. Because of its appealing electrical properties, the first transistor ever made was Ge-based [27]. It is well known that Si overcame Ge in the early microprocessor development because of its exceptional oxide quality,

Figure 1: Schematic of the Ge/SiGe heterostructure. Figure taken from [26].

but due to the Second Quantum Revolution, Ge is living a "Renaissance" [28–30]. The heterogeneous integration with Si in a convention CMOS process allows an accessible framework for Ge-based circuit development. The same industrial process for Si can be used for Ge. Even more, the compatibility of Ge with high-κ dielectric has been demonstrated, a keystone in the microelectronic circuit integration. This big interest in Ge-based devices lunched the research of quantum nature phenomena and hole's properties in such heterostructures. Some of them are the ultra-high mobility [31, 32], which provides the formation of high-quality quantum dots. The low strain-tunable effective mass [26, 33], that enhance the QDs energy level spacing, allowing to relax the gate lithography requirements. The anisotropy in the g-factor and the large out-of-plane component [34, 35], which complements with the intrinsic hole's Spin-Orbit Interaction (SOI) [36, 37]. Lastly, the p-type orbital wavefunction for holes in the valence band decrease the hyperfine interaction, which enhance the coherence time of the spin states.

Quantum Computation with QDs

Out of the several quantum properties of matter, one of them is the superposition of states. This is a consequence of a purely quantum phenomenon, the wave function. It is still not settled why Nature behaves like this, but we can trust all the experiments carried on in the last century to believe that it does. In 1982, the physicist Richard Feynman formulated the idea of using the superposition propriety of Nature to create the primitive idea of quantum computers [38]. Opposite to the classical computer numeration for bits (0 or 1), its quantum counterpart could be a superposition of states ($\alpha|0\rangle + \beta|1\rangle$). Feynman's proposition was focused on simulation of quantum systems, but Peter Shor went a bit further. In 1994, he published a paper developing the idea of quantum mechanics to solve a computational problem [39]. This date is accepted as the birth of Quantum Computation. Four years later, Daniel Loss and David P. DiVincenzo published a paper where they merge the new field of Quantum Computation with QDs [40]. They proposed using the spin-states of electrons in QDs as a coding element for quantum computing.

Specifically talking about the topic in this thesis. Ge-based devices has shown in the Quantum Computation field an impressive development in the last years. QDs have been measured in nanowires, hut-wires and quantum wells [14, 25, 41–48]. Electrical manipulation of spin and the qubit formation has also been achieved [49–52]. Ge has also been used for the implementation semiconductor/superconductor hybrid devices, either for spin-photon coupling [45, 46, 53] or gatemons [54, 55].

This thesis...

This thesis is a travel diary from the birth of the Ge-based semiconductor substrate to the final electrical tune of QDs. In the chapter 1, the basis of band theory applied to strained Ge quantum well is discussed, as well as the QDs transport theory for Single Quantum Dots (SQD) and Double Quantum Dots (DQD). Second chapter 2 speaks about the fabrication development. Here we will see the different decisions we took during the recipe creation, and we will learn that the path to success is not a straight line. In chapter 3 we will discuss the heterostructures mobility measurements, as well as some surface trap tunneling effect and pinch-off voltage drift. For this purpose, we fabricated Hole-Field Effect Transistors (H-FET) and Quantum Point Contacts (QPC). Next chapter 4 is about the SQD. We show the tuning protocol to reach the Coulomb blockade regime, and we measure some figures of merit, like lever arm, charging energy, g-factor, etc... The final chapter 5 is focus on a DQD device characterization. Here, we demonstrate the tuning of the two dots coupling strength, and we measure stability diagrams to extract the relevant capacitances of the system. Eventually, suing a proximal charge-sensor, we were able to count charge occupation in the DQD down to the last occupation. The last section is dedicated to the final discussion and perspectives of the project.

Chapter 1

Theoretical background

In this first chapter, the theoretical background related to the electronic transport measurements performed in the experimental section is discussed. It is divided into two parts. The first part focus on solid state physics, mainly on band theory and on the Luttinger-Kohn Hamiltonian. The second part is about quantum confinement and quantum transport, with special attention to the devices built in this thesis: H-FET, QPC and single and double QD.

Piece of germanium. Alfred Pasieka. Image taken from *Science Photo Library, Getty Images.*

1.1 Band structure in Ge

Germanium is a semiconductor and its Bravais lattice is diamond cubic. The atomic number is 32 and has an atomic mass of 72.64u. Knowing that its density is 5.3g/cm^2, this gives 4.41×10^{21} atoms per square centimeter. Each of those atoms contributes with 32 electrons to the system and with their corresponding electrostatic field, it would be nearly impossible to solve the many-body Hamiltonian. Thankfully, we can apply some simplifications to the problem [56].

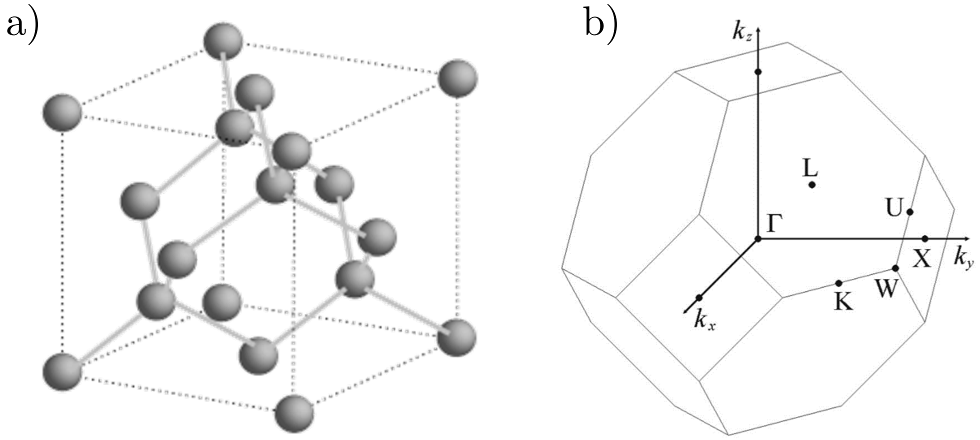


Figure 1.1: a) schematic of a diamond lattice. Each sphere represents an atomic site. This lattice is observed in type-IV semiconductors. Image taken from the NSO website. b) the first Brillouin zone for the diamond lattice.

The first approximation we will consider is that only the most external electrons (those in the last atomic orbitals) contribute to transport. We assume the inner electrons are strongly bonded to the atom nuclei. The next approximation is the Born-Oppenheimer, or adiabatic, approximation. Electrons dynamic is faster than the ion's vibration frequency. From the electron point of view, ions inside the lattice are essentially stationary. This approximation allow us to split the Hamiltonian in two parts: one for electrons and another one for nuclei. Finally, the last approximation is the mean-field approximation. The sum of all the electric field contribution from the atoms in the crystal is recovered as an average potential $V(\mathbf{r})$. The Schrödinger equation for an electron in such potential is:

$$\mathscr{H}_n \Phi_n(\mathbf{r}) = \left(\frac{p^2}{2m} + V(\mathbf{r})\right) \Phi_n(\mathbf{r}) = E_n \Phi_n(\mathbf{r}). \tag{1.1}$$

Φ_n is the electron wavefunction of a single electron in the electrostatic potential $V(\mathbf{r})$. We can go further and consider a translational symmetry due to the atom's periodicity inside the crystal. This implies that the potential can be expressed as $V(\mathbf{r}) = V(\mathbf{r}+\mathbf{R}))$, where $\mathbf{R}$ is the lattice's periodic length. A schematic of the Ge atomic unit cell is represented in figure 1.1 a). In a periodic potential, the electron wave function can be expressed as a complete set of eigenfunctions $\Psi(\mathbf{r})$ that has the form of flat waves. This conclusion is derived from the Bloch theorem, and the basis is known as Bloch functions. They are

$$\Psi(\mathbf{r}) = e^{i\mathbf{kr}}u(\mathbf{r}), \tag{1.2}$$

where $\mathbf{r}$ is the length dimension and k is known as the wave vector. The crystal symmetry is also reflected in the wave vector: k and $k + 2n\pi/R$ are solutions of the Bloch function. This symmetry allows us to define, in the reciprocal space, the first Brillouin zone, represented in figure 1.1 b) This three-dimensional surface are the bounds in a three-dimensional lattice of the periodic wave vector. Each crystal lattice has its own Brillouin zone associated.

1.1.1 k-p theory for spin-degenerate bands

This section is mainly based in the book of Peter Y. Yu and Manuel Cardona *Fundamentals of semiconductor* [56] and the book of Roland Winkler *Spin-Orbit Coupling Effects in Two-Dimensional Electron and Hole Systems* [36]. I also got inspiration from the thesis of Raisei Mizokuchi [57].

There are several methods to analytically resolve the electronic wavefunction in a periodic potential. The eigenvalues for equation 1.1 are known as energy bands in the solid. The bands are the allowed energy states for electrons in the lattice. The method known as tight-binding allows to resolve the band structure of a solid for any value of $\mathbf{k}$. It considers the superposition of the orbital wavefunction of isolated atoms located in each atomic site. In figure 1.2 a) we see the Ge band diagram solved with tight binding.

In this thesis we will follow the **k-p** approach for spin-degenerate electrons. If we replace the Bloch function into the Schrödinger equation 1.1, we obtain

$$\left[\frac{p^2}{2m} + \frac{\hbar\mathbf{k}\cdot\mathbf{p}}{m} + \frac{\hbar^2k^2}{2m} + V_0\right]u_{n\mathbf{k}} = E_{n\mathbf{k}}u_{n\mathbf{k}}. \tag{1.3}$$

Around the high-symmetric point $k_0 = (0, 0, 0)$, previous equation is reduced to

$$\left[\frac{p^2}{2m} + V_0\right]u_{n0} = E_{n0}u_{n0}. \tag{1.4}$$

This equation is much easier to solve than equation 1.1. Here, the Bloch functions are periodic, and they form a complete and orthogonal set of basis.

The other terms from the Hamiltonian $\frac{\hbar\mathbf{k}\cdot\mathbf{p}}{m}$ and $\frac{\hbar^2k^2}{2m}$ can be treated as perturbations in the degenerate or non-degenerate perturbation theory. Around a chosen $\mathbf{k_0}$, only a few experimental parameters are necessary to compute the full $\mathbf{k}$-values of the Brillouin zone. We expand the basis u_{n0} around the k_0 point

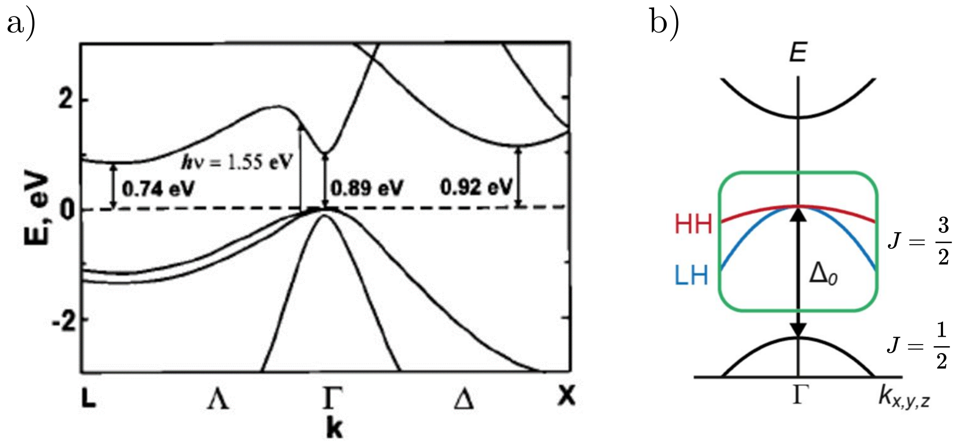


Figure 1.2: a) Ge band diagram solved using tight-binding. Over the Fermi level (dashed line), we see the conduction bands for electrons. Below the Fermi level, we observe the valence bands for holes. The difference between the bottom-most point in the conduction band and the top-most point in the valence band is the gap energy. Figure taken from [58] b) quadratic band dispersion of the Ge bands around the point $k = 0$. We observe the splitting of valence band with the hole spin value. The lowest energetic band correspond to the holes with $J = \frac{1}{2}$ and the top-most valence band is for $J = \frac{3}{2}$. Figure taken from [30].

$$u_{n\mathbf{k}} = u_{n0} + \frac{\hbar}{m} \sum_{n' \neq n} \frac{|\langle u_{n0}|\mathbf{k}\cdot\mathbf{p}|u_{n'0}\rangle|^2}{E_{n0} - E_{n'0}}. \tag{1.5}$$

The associated energy taking into account the perturbation theory is

$$E_{n\mathbf{k}} = E_{n0} + \frac{\hbar^2 k^2}{2m} + \frac{\hbar^2}{m^2} \sum_{n' \neq n} \frac{|\langle u_{n0}|\mathbf{k}\cdot\mathbf{p}|u_{n'0}\rangle|^2}{E_{n0} - E_{n'0}}. \tag{1.6}$$

Here, the linear terms in k are no longer considered because the calculations are taken in an extremum of E_{nk}. For small k values, we can write

$$E_{n\mathbf{k}} = E_{n0} + \frac{\hbar^2 k^2}{2m^*}. \tag{1.7}$$

Where m^* is defined as effective mass. This is a very relevant concept in semiconductor band theory. The expression for the effective mass comparing the two previous equation is

$$m^* = m \left[1 + \frac{2}{mk^2} \sum_{n' \neq n} \frac{|\langle u_{n0}|\mathbf{k}\cdot\mathbf{p}|u_{n'0}\rangle|^2}{E_{n0} - E_{n'0}} \right]^{-1}. \tag{1.8}$$

We observe that the effective mass of the electron is different from the one in vacuum. Actually, the inverse of the effective mass corresponds to the curvature of the energy band.

1.1.2 Luttinger Hamiltonian

Up to now, we have seen the band theory applied to a generic case. In this section we will focus in the particular case of type-IV semiconductors, which have a diamond kind of lattice. In particular, we will consider Ge.

The previous Hamiltonian have only taken into account the interaction between the electrostatic potential from the lattice and the electrons. Due to lattice symmetries, we can add an extra term known as "spin-orbit interaction" (SOI). This phenomenon is well known in atomic physics and can be derived from the Dirac equation. It is a relativistic correction whose nature arise from the interaction of lattice-generated magnetic fields and the electron spins in the solid bands. We consider the SOI as

$$E_{SOI} = \delta_{SOI} \mathbf{l} \cdot \mathbf{s}, \tag{1.9}$$

where the factor δ_{SOI} is a material dependent magnitude, $\mathbf{l}$ is the orbital number and $\mathbf{s}$ is the electron spin. We will consider that $(\mathbf{l}+\mathbf{s})^2 = \mathbf{l}\cdot\mathbf{l}+\mathbf{s}\cdot\mathbf{s}+2(\mathbf{l}\cdot\mathbf{s})$ and $\mathbf{l}\cdot\mathbf{s} = 1/2\left[(\mathbf{l}+\mathbf{s})^2 - \mathbf{l}\cdot\mathbf{l} - \mathbf{s}\cdot\mathbf{s}\right]$. From the sum of angular momentum, we can use that for a given ν we can say $\nu \cdot \nu = \nu(\nu+1)$. We can then mix all previous terms into the spin-orbit equation and obtain that

$$\delta_{SO} \mathbf{l} \cdot \mathbf{s} = \frac{\delta_{SO}}{2}\left[j(j+1) - l(l+1) - s(s+1)\right]. \tag{1.10}$$

The Ge has 32 electrons, its electron configuration is $[Ar]3d^{10}4s^2 4p^2$. The last orbital has angular momentum of $p \rightarrow l = 1$. We know that the electron spin is $s = 1/2$. The sum of both angular momentum is $\mathbf{j} = \mathbf{l} + \mathbf{s} = 3/2, 1/2$. When we replace the angular momentum values for the last Ge electrons, we obtain:

If $j = \frac{3}{2}$, then $\mathbf{l}\cdot\mathbf{s} = \frac{1}{2}$, and the spin-orbit becomes $E_{SOI,j=3/2} = \frac{1}{2}\delta_{SOI}$.
If $j = \frac{1}{2}$, then $\mathbf{l}\cdot\mathbf{s} = -1$, and the spin-orbit becomes $E_{SOI,j=1/2} = -\delta_{SOI}$.

From previous equation, we observe an energy difference between the two bands for electron with angular momentum $j = 3/2$ and $j = 1/2$. For Ge, the energy difference is $E_{SO,j=3/2} - E_{SO,j=1/2} \approx 300\text{meV}$. In band theory, we say that the valence bands are populated by holes, and the spin $j = 3/2$ correspond to the hole spin.

The previous spin-orbit calculation can be generalized with the interaction Hamiltonian

$$H_{SOI} = \frac{\hbar}{4c^2m^2}(\nabla V \times \mathbf{p})\sigma, \tag{1.11}$$

where c is the speed of light and σ are the Pauli matrix for spin $s = 1/2$. When we add the interaction term in the **k-p** theory (equation 1.4), we arrive to the Luttinger-Kohn Hamiltonian

$$H_{LK} = -\frac{\hbar^2}{2m}\left[\left(\gamma_1 + \frac{5}{2}\gamma_s\right)k^2 - 2\gamma_s(\mathbf{k}\cdot\mathbf{J})^2\right]. \tag{1.12}$$

The derivation of this equation is not easy, for a deeper calculation we refer to [36]. The parameters γ_1 and γ_s are material-dependents and known as Luttinger parameters.

The purpose of this thesis is to discuss the quantum dots viability with holes. This implies that we can perform a simplification on the Luttinger-Kohn Hamiltonian and focus only in the $j = 3/2$ hole subband. Inside this band, the possible projection for J along the z-directions are $J_Z = 3/2, -3/2$, know as heavy-holes, and $J_Z = 1/2, -1/2$, known as light holes. The k-p theory Hamiltonian with the spin orbit interaction for holes of $J = 3/2$, in the basis $\left\{|+\frac{3}{2}\rangle, |+\frac{1}{2}\rangle, |-\frac{1}{2}\rangle, |-\frac{3}{2}\rangle\right\}$, has the form

$$H_{4kp} = \frac{\hbar^2}{2m}\begin{pmatrix} P+Q & -S & R & 0 \\ -S^* & P-Q & 0 & R \\ R^* & 0 & P-Q & S \\ 0 & R^* & S^* & P+Q \end{pmatrix}, \tag{1.13}$$

where:

$$P = \gamma_1(k_x^2 + k_y^2 + k_z^2) \tag{1.14}$$

$$Q = \gamma_2(k_x^2 + k_y^2 - 2k_z^2) \tag{1.15}$$

$$R = \sqrt{3}[-\gamma_3(k_x^2 - k_y^2) + 2i\gamma_2 k_x k_y] \tag{1.16}$$

$$S = 2\sqrt{3}\gamma_3(k_x - ik_y)k_z, \tag{1.17}$$

k_z, k_y and k_x are the wave vector components in the different crystallographic directions. For Ge, $\gamma_1 = 13.38$, $\gamma_2 = 4.24$ and $\gamma_3 = 5.69$. We can observe the off-diagonal terms in equation 1.13 which account for the coupling between light and heavy holes.

1.1.3 Planar structures

We will consider the particular case of two-dimensional structures. These structures form a sandwich of SiGe/Ge/SiGe. Because of the valence band alignment, the Ge acts as a quantum-well for holes. A 2DHG is formed in the SiGe/Ge top interface. Let's call the vertical confinement direction z and x, y the in-plane directions. The hole wavefunction has border constriction in the z direction, it vanishes at both interfaces. We can use the Hamiltonian 1.13 for the case where $k^2 = k_x^2 + k_y^2$. We take the two diagonal terms for heavy holes ($H_{HH}, J_Z = \pm 3/2$) and light holes ($H_{LH}, J_Z = \pm 1/2$) and obtain

$$\begin{aligned} H_{HH} &= \frac{\hbar^2}{2m}(P+Q) = \frac{\hbar^2}{2m}\left[(\gamma_1+\gamma_2)k^2 + (\gamma_1 - 2\gamma_2)k_z^2)\right] \\ H_{LH} &= \frac{\hbar^2}{2m}(P-Q) = \frac{\hbar^2}{2m}\left[(\gamma_1-\gamma_2)k^2 + (\gamma_1 + 2\gamma_2)k_z^2)\right]. \end{aligned} \tag{1.18}$$

From these two equation we can define the effective mass for heavy holes and light holes for in-plane axis and out-of-plane. In-plane light-hole effective mass is $m^l_{\parallel} = m/(\gamma_1 - \gamma_2)$, in-plane heavy hole effective mass is $m^h_{\parallel} = m/(\gamma_1 + \gamma_2)$. The out-of-plane components read as $m^l_{\perp} = m/(\gamma_1 + 2\gamma_2)$ and $m^h_{\perp} = m/(\gamma_1 - 2\gamma_2)$. It is noticeable how the in-plane heavy hole effective mass is lighter than the light holes effective mass.

Lattice strain also plays a role in the two-dimensional quantum-well structures. In the SiGe/Ge/SiGe heterostructures, the Ge is under a compressive strain due to the lattice parameter mismatch with the SiGe. The strain will affect the band dispersion and the effective masses of heavy and light hole. In addition, it will break the degeneracy in the $k = 0$ maximum of the valence band. Schematics in figure 1.3 shows the top-maximum of the valence band for different strain cases. We observe that for our case, the compressive strain creates a gap between the heavy and light holes. In practice, this will produce that the first holes accumulated at the quantum-well will be heavy holes. Eventually, if the gate potential keeps increasing, light holes will also be accumulated. When both kind of holes cohabit in the quantum well, the effective mass becomes a combination of heavy and light holes, and same with the Landé g-factor.

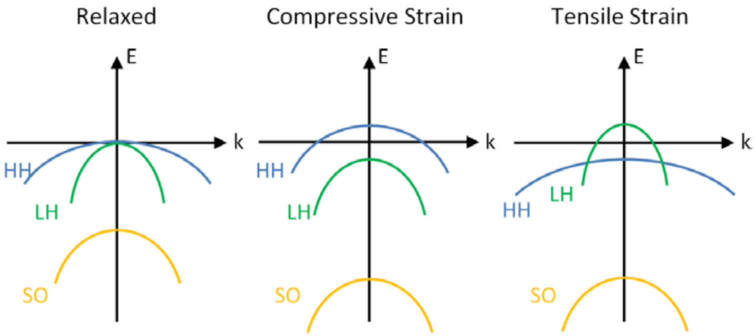


Figure 1.3: Band diagram splitting due to the effect of strain in the lattice. We observe how with compressive strain, the heavy hole and light hole bands separate each other in energy. For tensile strain the effect is the opposite. The subband below correspond to the holes with $j = 1/2$, it also called split-off band. Figure taken from [59].

In Ge, the spin splitting is caused by the Rashba Spin-Orbit Interaction. This phenomenon arises in two-dimensional systems where there is an inversion-asymmetry [36, 37, 60]. The derivation of this term is out of the scope of this work.

1.2 Quantum devices

Along this chapter section I will introduce the mesoscopic transport theory for three quantum devices in particular: Field Effect Transistor (FET), Quantum Point Contact (QPC) and quantum dots (QD). From all the bibliography, I wrote in this thesis a brief summary of the relevant aspect for the experiments. If the reader wants a deeper discussion, I recommend going to the cited references.

The FET section is mainly based in two books and two reviews. The band structure approach, where the Schottky barrier are discussed is taken from the development of *Physics of semiconductor* by S.M. Sze [61], the paper review from Y. Wang et al. [62] and finally the study from R.T. Tung [63]. The field effect as a parallel plate capacitor is based from the book *Semiconductor Nanostructures* by Thomas Ihn [64].

The QPC section is inspired by the two books of *Semiconductor Nanostructures* by Thomas Ihn [64] and *Mesoscopic Electron Transport* [7]. Some development is also inspired from the Boris Brun-Barriere's thesis [65].

For the final section of quantum dots, I based this thesis in the books of *Semiconductor Nanostructures* by Thomas Ihn [64] and *Mesoscopic Electron Transport* [7] again. But also from the reviews of R. Hanson et all. [66], the J.M. Elzerman review [67], the W.G. van der Wiel [4] and the review from F.A. Zwanenburg [24].

1.2.1 Field effect in a quantum well

When two solids enter in contact, they minimize the overall energy by a charge displacement until the Fermi level of both materials align. In semiconductors, the Fermi level is not defined the same way as it is for metals. It does not exist an overlapping in the electrons k-surfaces between two consecutive Brillouin zones. We define it by the energy value corresponding to the electron density average between the densities in the conduction and the valence bands. The Fermi energy would be in the middle of the gap. When a metal and a semiconductor enter in contact, the Fermi level of the metal align with the virtual position of the semiconductor's Fermi level. At the interface, the valence and conduction bands pinch to the metal, bending its potential energy. This is known as Schottky effect. Far from the interface, the semiconductor bands recover their bulk value.

In the case studied here, the metal and the semiconductor have a high-k dielectric in between. The top-most value of the valence band in the heterostructure is represented in figure 1.4. We can appreciate the Schottky barrier at the interface. The amplitude of the bending depends up on the metal work function (Φ_m) and the virtual semiconductor position for the Fermi level (Φ_S).

When a gate voltage is applied (figure 1.4 c) the bands bend according to the gate displacement of E_F. Once the top-band overcome the Fermi level defined by the ohmic contacts, holes start to accumulate and a 2DHG is formed.

This effect can be model as a parallel plate capacitor. One side of the capacitor is the metallic gate, and the other side is the 2DHG. This model has one

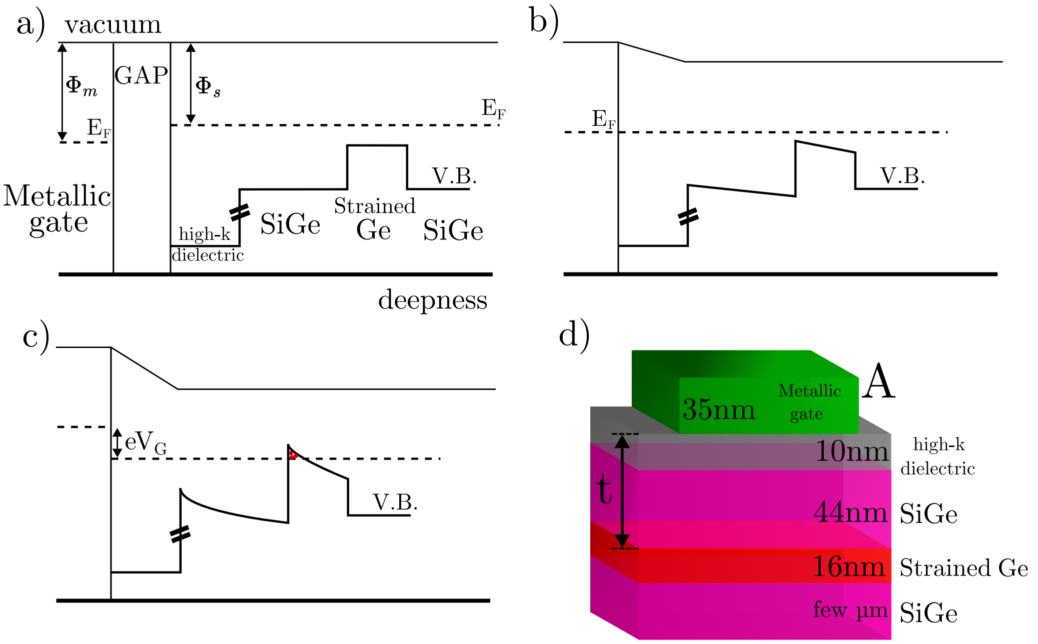


Figure 1.4: a) to c) are schematics showing the top-most point in the heterostructure valence band and the metallic gate. In a), the two materials are not in contact and their electronic potential is defined with respect to the vacuum. In b), they are contacted and the Fermi level align. For this case, the Schottky barriers raised in the interfaces between different materials. c) is the system with a voltage V_G applied to the gate. In d) we can see a schematic of the heterostructure with the different materials between the metallic gate and the quantum well.

disadvantage. It does not consider the activation potential to accumulate carriers in the quantum well. But on the other hand, it gives an easy insight on the physics and can be quite accurate in the low-density regime. We consider the capacitance equation for a plate capacitor

$$C = \frac{\epsilon_{eff}\epsilon_0 A}{t}, \tag{1.19}$$

where ϵ_{eff} is the effective dielectric constant between the gate and the quantum well, ϵ_0 is the vacuum dielectric constant, A is the gate surface and t is the distance between gate and quantum well. In the figure 1.4 d) we can see a system's schematic. When a potential V_g is applied to the gate, the charges accumulate as $Q = V_g C$. The total charge is equal to the number of carriers times the individual charge of a carrier $Q = |e|N$. Because of the energy conservation principle, the same quantity of charges are accumulated at the quantum well. We can say that $V_g = |e|Nt/\epsilon_{\text{eff}}\epsilon_0 A$. Writing the density as $n = N/A$ we obtain

$$n(V_g) = \frac{t\epsilon_{\text{eff}}\epsilon_0}{|e|}V_g. \tag{1.20}$$

This model does not take into account the surface tunneling effect [68] or disorder potential, which are pure quantum effects. This is a classical approach which connects a capacitively model with the band theory. In the following section, we will take the advantage of the capacitively models to explain the physics in the QPC and the quantum dots.

1.2.2 Quantum Point Contact

In a quantum-well heterostructure, a QPC device consists in two metallic gates facing each other with a gap between them. When the metallic gates are biased, the potential created confines the carrier gas in a one-dimensional channel. Conductance through such constriction will be quantized according to a multiple of the quantum of conductance $G_0 = 2e^2/h$.

In figure 1.5 a) we can see a representation of the parabolic approximation for the electrostatic potential at the QPC. Conductance is only allowed through the states in the potential. In figure 1.5 b) we observe the conductance curve of a QPC and the typical plateaus, multiples of G_0.

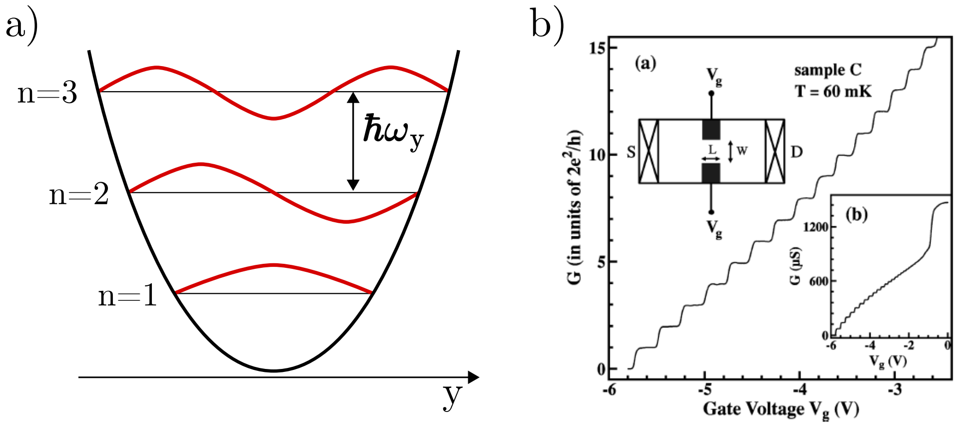


Figure 1.5: a) schematic of the parabolic potential energy states along the y-direction (the direction perpendicular to carrier transport). The wavefunction of the carries that pass through the QPC should match the eigenfunction of the electrostatic potential. b) typical QPC conductance plot (taken from [69]). We observe how each plateau appears at an integer value of G_0. The small inset image (a) shows a schematic of the sample from top view. The inset (b) is the conduction measured before correcting the line resistance.

The parabolic potential, the saddle-point model

In order to have a theoretical approach, we can follow the development in [70], we can model the electrostatic potential in the middle of the QPC as a saddle-point. Being the x-axis the conduction direction and the y-axis the transversal direction, the saddle-point potential increase towards the y-axis and decrease in the x-axis. The two electronic reservoirs are considered to be in electrochemical equilibrium.

In the parabolic approximation, the electrostatic potential created by the two gates at the quantum well level can be seen as a quadratic potential. We write

$$V(x,y) = V_0 - \frac{1}{2}m^*\omega_x^2 x^2 + \frac{1}{2}m^*\omega_y^2 x^2, \tag{1.21}$$

where ω_x and ω_y are the angular frequencies associated with the parabolic potential, and m^* is the carrier effective mass. We can assume the potential is separable. Along the perpendicular direction to transport, the parabolic potential forms quantized states. They are represented in figure 1.5 a). The energy for those states is $E_n = (n + 1/2)\hbar\omega_y$.

Conduction through the QPC for charges in the 2DHG can be seen as a scattering mechanism. Particles are transmitted with $T(E) = 1$ if their energies match the QPC energy levels, and they are fully reflected if they do not. Considering that the Fermi level is the last occupied energy state, all the QPC levels below the Fermi level are contributing to the conductance.

Transport through a QPC

Transport in the small bias regime δV_{bias} can be calculated from the current through a one-dimensional channel. We integrate the density of states $D(E)$ with the group velocity $v(E)$ around the Fermi level and multiply by the transmission probabilities $\tau(E)$. The formula read as

$$I = e\int_{E_F}^{E_F+|e|\delta V_{bias}} D(E)v(E)\tau(E)dE. \tag{1.22}$$

The carrier density in one dimension is $D(E) = \frac{2}{2\pi\hbar}\sqrt{2m^*/E}$. The group velocity is $v(E) = \partial E/\partial v_x$ which equals to $v(E) = \sqrt{E/2m^*}$. When we solve the current equation, we can see than the terms related to the effective mass and the energy vanish, and it is only kept the pre-factor. The current is $I = \frac{2e}{h}|e|\delta V_{\text{bias}}\tau(E_F)$. To express the conduction, we divide $G = I/\delta V_{\text{bias}} = \frac{2e^2}{h}\tau(E_F)$.

The previous equation only took into account one transmission channel through the QPC. We have seen in the previous section that each time an eigenstate of the parabolic potential falls below the Fermi level, it opens another channel of transmission. In figure 1.6 we see a schematic of the QPC potential and the Fermi level. The sum of all the conduction channel contribution to the total conductance is known as the Landauer formula, and it looks like

$$G = \frac{2e^2}{h}\sum_n^N \tau_n. \tag{1.23}$$

In figure 1.5 b) we can see the typical curve of conductance through a QPC. We can appreciate the quantization in the conductance plateaus as multiples of $2e^2/h$.

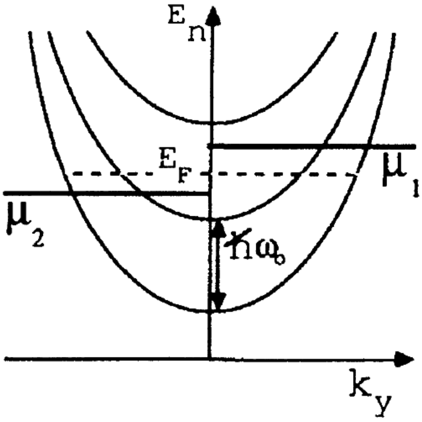


Figure 1.6: Schematic of the QPC parabolic potential next to the source and drain electrochemical potential and the Fermi level. All the QPC states below the Fermi level contribute to conductance through the constriction with a quantum of conductance G_0.

1.2.3 Quantum Dots

In order to quantitatively describe a QD, we will use the constant interaction model. In this model, we assign a capacitance between the different electrodes in the system. We work in a constant electric field interaction among all the elements. To form a QD, we need two terminals for the current to flow, and a region in space where the carriers can be confined. The confinement is produced by an electrostatic potential. The carrier island is what we know as QD. In order to have a better control over the electrostatic potential shape, it is convenient to have a third terminal that is capacitively couple to the QD. A schematic is represented in figure 1.7. If there is no coupling between the island and the source-drain electrodes, the carrier number in the QD is fixed an equal to N. The total charge of the island is then eN. In the case that carriers can go in and out of the QD, the system will always tend to minimize its energy by exchanging particles with the reservoirs. The change of dot's electrostatic energy because of a charge going in or out of the island is $E_C = e^2/C$, where $C = C_D + C_G + C_S$. This magnitude called charging energy.

Quantum dot energy scales

Now, we need to discretize the charge energy levels, but some conditions needs to be fulfilled. First, the charging energy has to be larger than thermal energy k_BT. Second, the coupling between the QD and the reservoirs has to be large

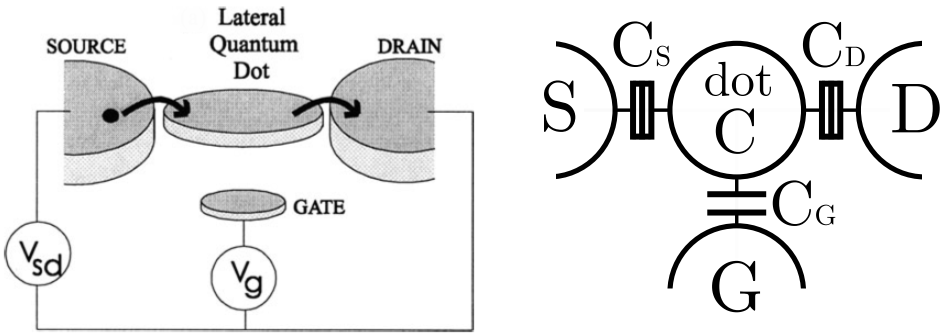


Figure 1.7: Schematic of a single quantum dot with three terminals: source, drain and gate. Figure taken from [71]. The dot is tunnel coupled to source and drain (C_S, C_D) and capacitively to the gate (C_G).

enough to allow particle exchange, but small to allow particle accumulation in the confinement potential. To estimate this values, we say that the discharging time for a carrier is $\Delta t = R_t C$, where R_t is the tunnel resistance between the QD and the source-drain reservoirs. By the Heisenberg uncertainty relation, we obtain $\Delta E \Delta t = (e^2/C) C R_t > h$. This implies that $R_t > h/e^2$, which is the quantum of resistance $R_0 = 25.813\text{k}\Omega$. In conclusion, the two conditions are:

$$R_t >> \frac{h}{e^2} \quad , \quad \frac{e^2}{C} >> k_B T. \tag{1.24}$$

The gate purpose is to continuously change the total dot potential. With this constant interaction, the system will minimize its energy by adding or subtracting one carrier from the QD when $|e| = C_G V_G$, being V_G the gate voltage. With the gate electrode, we can directly control the particle number in the quantum dot.

Level spacing in a QD

We can roughly estimate the quantum dot energy level spacing with its size. This estimation is good to have an idea of the length scales. Also, it will be use eventually to calculate the dot size.

We can assume that the electric potential which defines the QD is a sharp quantum well potential being $V(x) = \infty$ if $x < 0$ or $x > L$ and $V(x) = 0$ if $0 < x < L$. This is a text book exercise where the boundary condition force us to some quantized solution for the Schrödinger equation. We will not consider any spin.

$$\hat{E}|\Psi(k)\rangle = E_n|\Psi_n(k)\rangle, \qquad E_n = \frac{\hbar^2 k_n^2}{2m^*}, \tag{1.25}$$

where m^* corresponds to the carrier effective mass and $\hbar$ is the Plank constant. The wavefunction of the charges inside the quantum well must vanish at the edges

$x = 0$ and $x = L$. So we guess $|\Psi(k)\rangle_n = \Psi_0 \sin(k)$. The possible solution for k are $k = n\pi/L$ being n an integer and positive number. When we add the wavevector to the eigenenergy, for a 1D quantum well we obtain

$$E_n = \frac{(\hbar\pi)^2 n^2}{2m^* L}. \tag{1.26}$$

We can then generalize the solution of the equation to higher dimensions; 2D and 3D. A schematic representation of the wavefunction and the QD states is pictured in figure 1.8.

Another approach to this problem is considered the electric potential as a parabolic function in the in-plane direction. This scenario is closer to reality in the sense that a real electric field decays along the dielectric, and the potential experimented by holes at the quantum well is parabolic in the in-plane direction. The potential energy would read as

$$V(x,y,z) = \frac{1}{2}m^*\omega_0^2(x^2+y^2) + \frac{1}{2}m^*\omega_z^2 z^2, \tag{1.27}$$

where x, y and z are the space directions and ω_0 and ω_z are the angular parabolic potential frequencies. The solution of this Hamiltonian are the Fock-Darwin states.

$$E_{N,M,N_Z} = \hbar\omega_0(2N + |M| + 1) + \hbar\omega_z(N_z + 1/2), \tag{1.28}$$

where N is the radial quantum number, M is the angular momentum number and N_z is the out-of-plane quantum number. In such systems, the characteristic unit of length of the extended ground state is

$$l_0 = \sqrt{\frac{\hbar}{m^*\omega_0}} \tag{1.29}$$

To compare energy scales, we calculate the excited state energy difference between two consecutive levels $\Delta E = E_n - E_{n-1}$ for the infinite potential and between $\Delta E = E_{N+1,M,N_z} - E_{N,M,N_z}$:

$$\text{For 1D:} \qquad \Delta E = (N/4)\hbar^2\pi^2/mL^2 \tag{1.30}$$

$$\text{For 2D:} \qquad \Delta E = (1/\pi)\hbar^2\pi^2/mL^2 \tag{1.31}$$

$$\text{For 3D:} \qquad \Delta E = (1/3\pi^2 N)^{1/3}\hbar^2\pi^2/mL^2. \tag{1.32}$$

$$\text{For parabolic potential:} \qquad \Delta E = 2\hbar\omega_0. \tag{1.33}$$

We observe that for a 2D potential, the energy spacing is independent of the number of particles in the dot. With a first estimation, for a QD size of 100 nm and an effective mass $m^* = 0.08m_e$, we obtain an energy spacing of 0.5meV. In temperature, it corresponds to $\sim$ 8K. We observe that lower effective mass contributes to enlarge the level spacing.

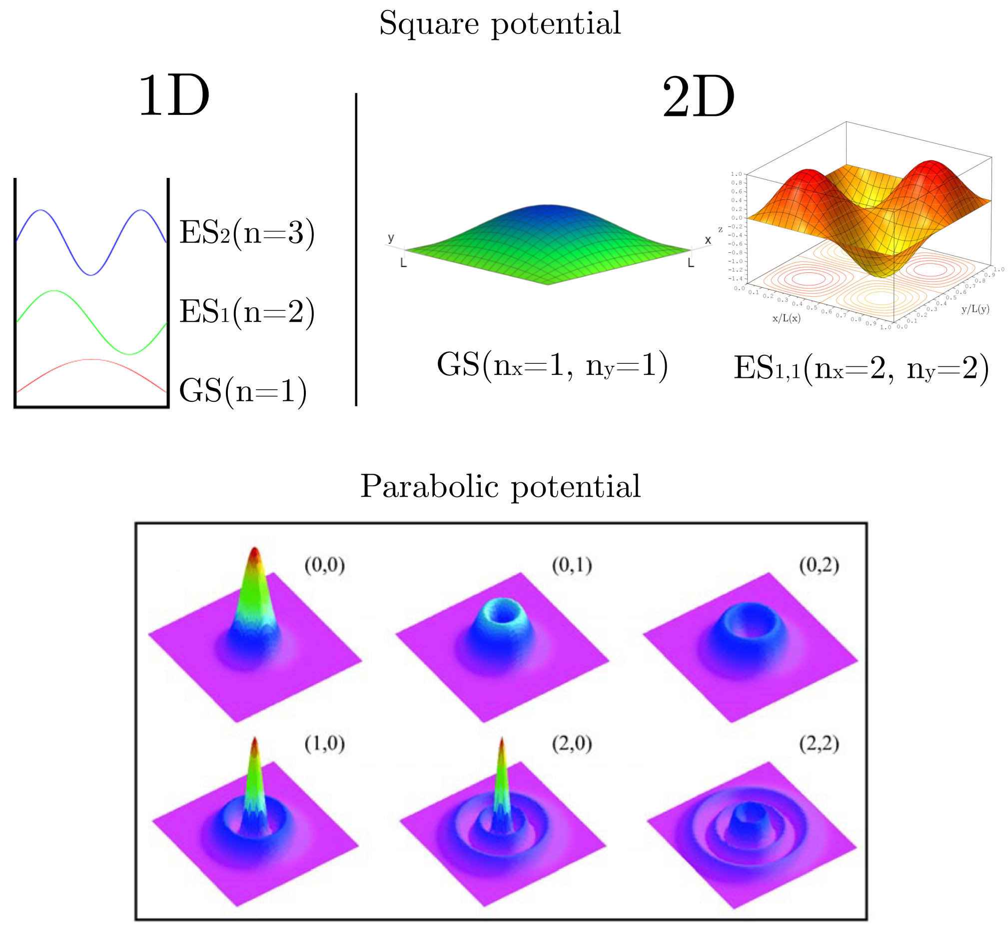


Figure 1.8: Schematic for a particle wavefunction inside square potential potential with 1D and 2D. GS stands for ground state and ES for excited state. In the bottom, we see the rep[resentation of the excited states in a parabolic potential. Figure taken from [18].

An important remark here is to not confuse the charging energy E_C with the level spacing ΔE. In the first case, we count the particle-particle interaction. It comes from a pure electrostatic treatment of the QD. The quantum confinement energy level spacing, also known as orbital level spacing, is a quantum treatment of particles in a potential. In each charge energy configuration there is space for several orbital levels.

Interaction model

Now let us define the charge energy levels in a quantum dot with several particles. We start by making a couple of assumptions. First, we say that the quantum levels can be calculated independently of the particles number in the dot N. Second, we assume that the particle number N does not affect the overall dot capacitance C, represented in schematic from figure 1.7. This is a strong assumption which is true for many particles, but becomes false when the quantum dot is almost empty. In this regime, the dot shape, and by extension its capacitance, is very sensitive to disorder potential, which influence in the energy levels.

We start by approximating the QD to a perfect capacitor of capacitance C. The electrostatic energy is

$$U(N) = \frac{Q^2}{2C}. \tag{1.34}$$

The charge of our model is the number of particles inside the dot N. It is also affected by the potential at the three electrodes, which are capacitively coupled to the dot. We can also count the charges in the QD (N_0) which compensate the dislocation potential of the quantum-well. The energy contribution from the orbital levels is E_n. The new expression for the energy becomes

$$U(N) = \frac{[-|e|(N - N_0) + C_S V_S + C_D V_D + C_G V_G]^2}{2C} + \sum_n E_n, \tag{1.35}$$

Previous equation is useful for understanding the energies in the system, but not to experimentally observe the quantum dot. We measure the dot in transport, what we really see is the current produced by carrier exchange in the quantum dot. That is why we define a new energy scale called dot electrochemical potential, it is defined as $\mu(N) \equiv U(N) - U(N-1)$. In terms of the dot capacitance it is

$$\mu(N) = \left(N - N_0 - \frac{1}{2}\right) E_C - \frac{E_C}{|e|}\left(C_G V_G + C_S V_S + C_D V_D\right) + E_n. \tag{1.36}$$

We observe that the electrochemical potential linearly depends upon the gate voltage. This makes a very convenient representation of the dot tunneling. We see $\mu(N)$ as a "ladder" that goes upwards or downwards with the gate voltage. When the chemical potential is aligned with the source-drain reservoirs, we observe current through the system. Figure 1.9 shows a schematic of the chemical potential.

The energy difference between two consecutive charge transition states is defined as the addition energy $E_{\text{add}}(N)$:

$$E_{\text{add}}(N) = \mu(N+1) - \mu(N) = E_C + \Delta E. \tag{1.37}$$

This magnitude is very convenient because we directly observe it in transport measurement.

Transport in a SQD

The current through a SQD can be described with the Landauer-Buttiker theory [4, 64]. This formula is applied for two terminals system in the limit of a low source-drain bias:

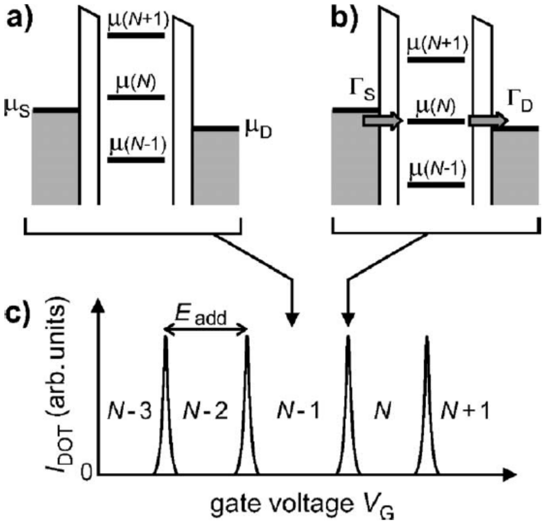


Figure 1.9: Schematic of the quantum dot chemical potential ladder and the source and drain chemical potential. When $\mu_S > \mu(N) > \mu_D$ there is current through the dot. $\Gamma_{S,D}$ are the source and drain tunnel rates. In c) there is a schematic of the system current in function of the gate voltage. Figures taken from [66].

$$I = \frac{e}{h}\int \tau(E)\,[f_L(E) - f_R(E)]\,dE. \tag{1.38}$$

In the case of a SQD, the left $f_L(E)$ and the right $f_R(E)$ reservoir act as source and drain. Between them, there is a small bias difference $e\delta V$. The Fermi distribution is also affected by temperature. The term $\tau(E)$ is the transmission probability of a particle to go L to R (or vice-versa).

In a SQD, we have two tunnel barrier gates in series. We can start by approximating those barrier gates to a Fabry-Perot interferometer. Instead of photons and an electromagnetic wave we have the charge carriers and the particle wavefuntion. This approximation is accurate in the lengths of the carrier's mean free path, where particles behave ballisticaly. Figure 1.10 a) shows a schematic of the Fabry-Perot interferometer with the reflecting and transmission probabilities for the two barriers. We can approximate the resonance to a Lorentzian by the Lorentz approximation, but we have to fulfill some conditions. The transmission coefficient for both barriers should have small transmission $|t_L|, |t_R| \ll 1$, and by extension $|r_L|, |r_R| \sim 1$. And the Lorentz model is only valid close to a resonance point. This means that the electrochemical potential of the dot is aligned with the source-drain chemical potential. With a general channel p contributing to conductance, the total transmission τ for carrier through the system is

$$\tau = \frac{|t_0|^2}{1 + (E - E_p)^2/(\Gamma_p/2)^2}, \tag{1.39}$$

where E_p is the chemical potential energy for transmission channel p and Γ_P is the Lorentzian line width of the curve, represented in figure 1.10 b). The third term $|t_0|$ is

$$|t_0| = \frac{4\tau_R\tau_L}{(\tau_L + \tau_L)^2}, \tag{1.40}$$

where $\tau_R = |t_R|^2$ and $\tau_L = |t_L|^2$ are related to each barrier in the Fabry-Perot interferometer. The equation 1.40 has a maximum value when $\tau_R = \tau_L$. This implies than when two barriers are in series, the amplitude is maximum when both barriers have the same transmission.

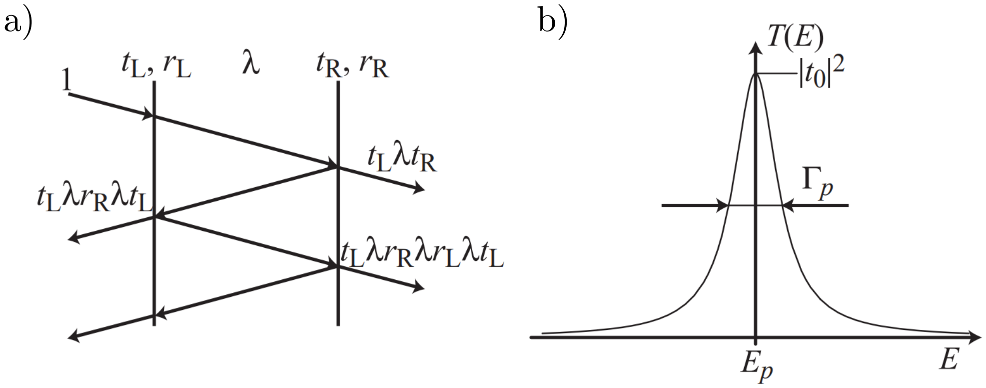


Figure 1.10: a) schematic of the Fabry-Perot interferometer for model the two tunnel barriers. We observe the transmission and reflection probabilities en each of the barrier. b) is the Lorentzian line-shaped curve for the transmission in a double barrier quantum dot. The resonance is around the energy value E_p for the transmission channel p. The Lorentzian width is given by the tunnel rate $\Gamma_p = \Gamma_p^{(R)} + \Gamma_p^{(L)}$. Figures taken from [64].

With all the previous equation and using that the tunnel rate for right and left barriers, around the resonance is proportional to the transmission $\Gamma_p^{R/L} \propto \tau_p^{R/L}$, we can write

$$\tau = \sum_p \frac{\Gamma_p^{(L)}\Gamma_p^{(R)}}{\Gamma_p^{(L)} + \Gamma_p^{(R)}} \frac{\Gamma_p}{(\Gamma_p/2)^2 + (E - E_p)^2}. \tag{1.41}$$

Coming back to the Lorentzian width Γ_p, we observe that the peak is broadened by the contribution of the source and drain tunnel rates. For now, we have not considered any other phenomenon, so the total peak width can be expressed as $\Gamma_p = \Gamma_p^{(R)} + \Gamma_p^{(L)}$. It is convenient to express the Lorentzian-shape function as

$$\mathscr{L}_p[E - E_p] = \frac{\Gamma_p}{(\Gamma_p/2)^2 + (E - E_p)^2}. \tag{1.42}$$

If we solve the equation 1.38 with the calculated transmission, we obtain the final conductance $G = I/\delta V$ equal to

$$G = \frac{e^2}{h} \sum_p \frac{\Gamma_p^{(L)}\Gamma_p^{(R)}}{\Gamma_p^{(L)} + \Gamma_p^{(R)}} \int dE \mathscr{L}_p[E - E_p] \left(\frac{\partial f}{\partial E}\right). \tag{1.43}$$

At this point, we can consider different thermal regimes for transport. They are:

- $e^2/C \ll k_B T, eV_{\text{bias}}$, transport happen through several QD levels. There is not any Coulomb blockade.
- $h\Gamma_p, \Delta E \ll k_B T \ll e^2/C$, metallic quantum Coulomb blockade regime. Transmission happens through several states in the QD.
- $h\Gamma_p, k_B T \ll \Delta E < e^2/C$, quantum Coulomb blockade regime. Transmission happens through a single QD level.

In the first limit, the thermal energy is larger that the QD charging energy. In this regime, there is no Coulomb blockade. The system conductance is given by the ohmic sum of the two tunnel barrier conductance $1/G = 1/G_R + 1/G_L$. The conductance is fully characterized by the barrier and is independent of the QD size.

The second and third regime are very similar. The difference in the transmission curve is the width of the signal. This width is broadened by temperature $k_B T$ and by each transmission channel through the dot. The excited states contribute with their own tunnel rate. We can solve equation 1.43 and obtain

$$G = \frac{e^2}{h} \frac{1}{4k_B T} \sum_p \frac{\Gamma_p^{(L)}\Gamma_p^{(R)}}{\Gamma_p^{(L)} + \Gamma_p^{(R)}} \cosh^{-2}\left[(E_p - E_F)/2K_B T\right]. \tag{1.44}$$

In this equation, if the case is a metallic quantum dot, we add the tunnel rate for each excited estate. If the dot is in the quantum regime, only one state contributes to conductance.

We can also calculate the limit for conductance when $k_B T \ll h\Gamma_p$. We obtain the Breit-Wigner formula

$$G_{BW} = \frac{e^2}{h} \frac{\Gamma^{(R)}\Gamma^{(L)}}{(\Gamma^{(R)} + \Gamma^{(L)})^2}. \tag{1.45}$$

In order to illustrate the previous calculation, in figure 1.11 we see two measurements of Coulomb peaks in different regimes. The idea of both experiments is to fit the peak shape to the transport equation shown previously. In the case that $h\Gamma_p \approx k_B T$ the approximation taken before are not good enough and the equation 1.38 must be computed numerically.

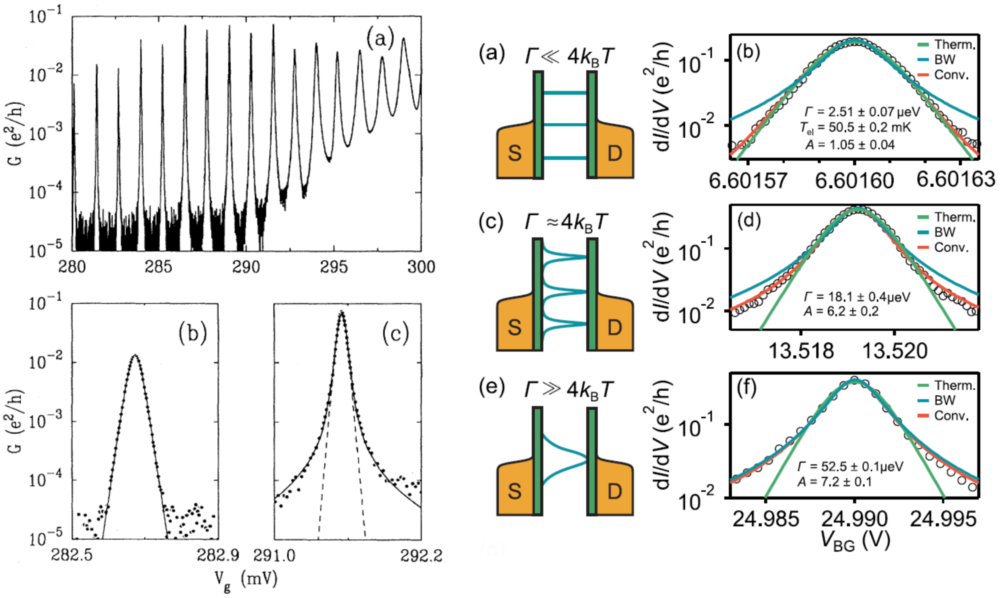


Figure 1.11: Images from [5] (left) and [72] (right). In the left panels, we can see two regimes for conductance. When $k_B T \approx h\Gamma_p$ in the broad peaks and $h\Gamma_p \ll k_B T$ for the narrow ones. In the right panels there are schematics for three cases and their corresponding measurements. We can observe how the used different fiting method for each case.

Cotunneling

So far, we have considered the cases where transport is a first order process. Nevertheless, it is possible that two transport event happen at the same time. This second order process is known as cotunneling. We will study two regimes: elastic and inelastic cotunneling. In figure 1.12 we observe two measurements where they observed cotunneling. In a) it is measured the elastic cotunneling, its signature is the broadening of the peaks as the gate voltage increases. This measurement was done in GaAs/AlGaAs in the many-body regimes. The case we observe in b) is measured in the low-electron regime in double quantum-well structures of AlGaAs/InGaAs/AlGaAs. They observed inelastic cotunneling for the even ocupation number inside the dot.

For the elastic cotunneling, represented in figure 1.13, the total process' energy is conserved. This effect can happen through another QD charge state or through an excited QD state. It is typically observed in cases where the tunnel rates to source and drain are large enough, so equation 1.41 does not apply. In the limit of zero temperature and for QD orbital level spacing being smaller than the charging energy $\Delta E \ll E_C$, Averin and Nazarov [75] calculated the conductance with the elastic cotunneling:

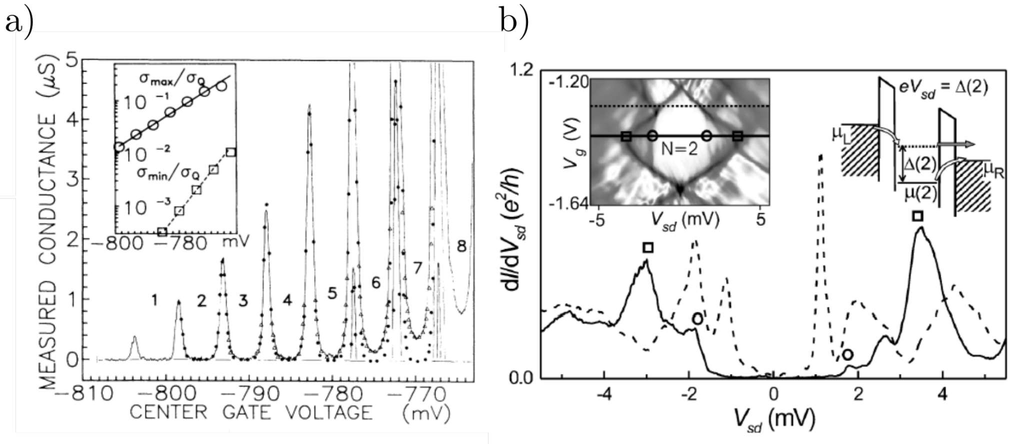


Figure 1.12: Two measurements of SQD cotunneling transport. In a) [73] they measured the change in regime from an isolated Coulomb island, where cotunneling does not occur, to the regime where cotunneling transport is visible. The SQD is in the many-body regime. In b) [74] they measured in the low-electron number regime. They were able to observe inelastic cotunneling when increasing the bias voltage.

$$G_{el} = \frac{\hbar G_S G_D \Delta E}{4\pi e^2} \left(E_e^{-1} + E_h^{-1} \right). \tag{1.46}$$

In this equation, G_S and G_D are the conductance of the barrier connecting source and drain. $E_e = \mu_{N+1} - E_F$ and $E_h = E_F - \mu_N$, where E_F is the Fermi energy of source and drain. These magnitudes represent the energy difference of the next QD charge level and the previous one with respect to the source and drain chemical potential. We observe that a larger coupling with source and drain produce a large cotunneling conductance.

The inelastic cotunneling may look like it does not conserve energy. We can observe in figure 1.13 how the final state of the QD is different from the initial, but actually the energy difference comes from the bias voltage. The inelastic cotunneling can only happen when a finite bias is applied to the system, and even more, when $eV_{bias} > \Delta E$. Using again the Fermi golden rule, we can calculate the transmission

$$G_{inel} = \frac{\hbar G_S G_D \pi}{3e^2} (k_B T)^2 \left(E_e^{-1} + E_h^{-1} \right)^2. \tag{1.47}$$

In this case, we consider also the thermal broadening of the peak. Eventually, the excited state inside the QD may decay to the ground state. This effect contributes to the broadening of the conductance peak.

1.2.4 Double Quantum Dots

The energy scale requisites in a DQD are the same as in the SQD. Tunnel barrier resistance has to be larger than the quantum of resistance $R_0 \ll R_t$ and

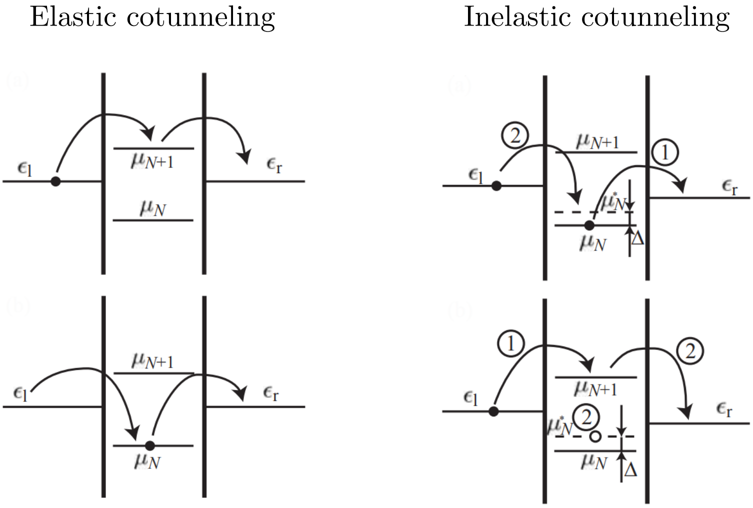


Figure 1.13: Schematic of an elastic and an inelastic cotunneling process. Figure taken from [64].

the dot charging energy should exceed thermal energy $k_BT \ll e^2/C$. With these considerations, we will directly jump to the electrostatic calculation of the system energies in the constant interaction model.

Constant interaction model in a DQD

For the DQD, we will also start with the constant interaction model seen in the SQD section. This time, the system will be expanded to cover a second quantum dot next to the previous one. The quantum dots are in series with the reservoirs. In figure 1.14 is drawn a schematic of the DQD system. N_1 and N_2 are the charge number for dots 1 and 2. The numeration is kept for the gate electrodes with $\mathrm{V_{G1}}$ and $\mathrm{V_{G2}}$. Both dots are considered to be tunnel-coupled with the capacitance $\mathrm{C_m}$.

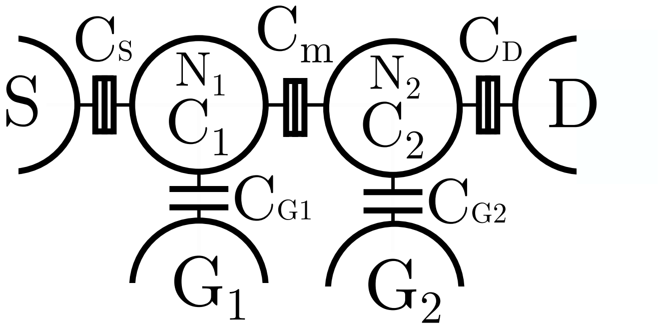


Figure 1.14: Schematic of a DQD system.

We can do the same calculation as in previous chapter and define an electrostatic energy in the system. We count the charges in each quantum dot as well as the potential influence of the gates around, without forgetting the coupling between dots:

$$\begin{aligned} Q_1 &= -|e|(N_1 - N_{0,1}) + C_S V_S + C_{G1} V_{G1} + \frac{C_m}{C_2} Q_2 \\ Q_2 &= -|e|(N_2 - N_{0,2}) + C_D V_D + C_{G2} V_{G2} + \frac{C_m}{C_1} Q_1. \end{aligned} \tag{1.48}$$

The charge $N_{0,1}$ and $N_{0,2}$ represent the screening charges that compensate the disorder potential in dots 1 and 2, respectively. From the previous charge definition, we obtain that the electrostatic potential $U(N_1, N_2)$ is

$$U(N_1, N_2) = \frac{1}{2} N_1^2 E_{C1} + \frac{1}{2} N_2^2 E_{C2} + N_1 N_2 C_m + f(V_{G1}, V_{G2}) \tag{1.49}$$

where the $f(V_{G1}, V_{G2})$ read as

$$\begin{aligned} f(V_{G1}, V_{G2}) = \frac{1}{-|e|} &[C_{G1} V_{G1} (N_1 E_{C1} + N_2 E_{Cm}) \\ &+ C_{G2} V_{G2} (N_1 E_{Cm} + N_2 E_{C2})] \\ &+ \frac{1}{e^2} \left[\frac{1}{2} C_{G2}^2 V_{G1}^2 E_{C1} + \frac{1}{2} C_{G2}^2 V_{G2}^2 E_{C2} \right] \\ &+ \frac{1}{e^2} C_{G1} V_{G1} C_{G2} V_{G2} E_{Cm}. \end{aligned} \tag{1.50}$$

In equation 1.49 we have defined a charging energies for each dot, E_{C1} and E_{C2}. The other term E_{Cm} is the coupling energy of one dot when a charge is added into the other dot. Their expressions are

$$E_{C1(C2)} = \frac{|e|^2}{C_{1(2)}} \left(\frac{1}{1 - \frac{C_m^2}{C_1 C_2}} \right), \quad E_{Cm} = \frac{|e|^2}{C_m} \left(\frac{1}{\frac{C_1 C_2}{C_m^2} - 1} \right). \tag{1.51}$$

In order to understand a bit more the coupling between the two dots, we can picture the extremes where the coupling is zero ($C_m \approx 0$) and where the coupling is large ($C_m \approx C_{1(2)}$).

In the first case, $C_m \approx 0$, both quantum dots are independent of each other. The equation 1.49 becomes

$$U(N_1, N_2) = \frac{(-|e|(N_1 - N_{01}) + C_{G1} V_{G1})^2}{2C_1} + \frac{(-|e|(N_2 - N_{02}) + C_{G2} V_{G2})^2}{2C_2}. \tag{1.52}$$

We can see how there is not any interaction between the dots. Previous equation could be divided into $U(N_1, N_2) = U(N_1) + U(N_2)$ where $U(N_{1(2)})$ are the SQD electrostatic energy. The charge stability diagram of such system is in figure 1.15 a).

In second case, $C_m \approx C_{1(2)}$, we are in the high coupled dot regime. When solving equation 1.49 we get

$$U(N_1, N_2) = \frac{(-|e|(N_1 + N_2 - N_{01} - N_{02}) + C_{G1}V_{G1})^2 + C_{G2}V_{G2})^2}{2(C_1^* + C_2^*)}, \tag{1.53}$$

where both C_1^* and C_2^* are $C_{1(2)}^* \approx C_{1(2)} - C_m$. We observe that when coupling is too large, the charge in each dot can be renamed as $N = N_1 + N_2$, and we recover the SQD electrostatic energy. In practice, when dot coupling C_m is too large, the DQD behaves as a big single quantum dot whose chemical potential is tuned with the two plunger gates $\mathrm{V_{G1}}$ and $\mathrm{V_{G2}}$. The charge stability diagram can be seen in figure 1.15 c).

In figure 1.15 b) we see an intermediate case of both discussed above. The electrostatic energy of each dot is mainly controlled by its gate voltage, but it exists a cross-talk between gates and a tunnel coupling between dots. The pattern formed is known as "honeycombs".

Due to the coupled quantum dot, the way we define the chemical potential must take into account the charges in the other dot. Each chemical potential is not independent of each other. Same as in the previous section, the chemical potential is equal to the energy difference between two consecutive charge states: $\mu_1(N_1, N_2) = U(N_1, N_2) - U(N_1 - 1, N_2)$ and $\mu_2(N_1, N_2) = U(N_1, N_2) - U(N_1, N_2 - 1)$. The expression in terms of capacitance and charging energies are

$$\mu_1(N_1, N_2) = \left(N_1 - N_{01} - \frac{1}{2}\right) E_{C1} + N_2 E_{Cm} - \frac{C_{G1}V_{G1}E_{C1} + C_{G2}V_{G2}E_{C2}}{|e|} \tag{1.54}$$

$$\mu_2(N_1, N_2) = \left(N_2 - N_{02} - \frac{1}{2}\right) E_{C2} + N_1 E_{Cm} - \frac{C_{G1}V_{G1}E_{C1} + C_{G2}V_{G2}E_{C2}}{|e|}. \tag{1.55}$$

From the honeycomb sizes we can extract some experimental values of the capacitive system. Figure 1.15 d) shows a zoom into a honeycomb. In the horizontal axis, the energy difference between the charge regions can be related with the chemical potential of N_1 and $N_1 + 1$ and the gate voltage difference. We can say that $\mu_1(N_1, N_2, V_{G1}, V_{G2}) = \mu_1(N_1 + 1, N_2, V_{G1} + \Delta V_{G1}, V_{G2})$. With some algebra in equation 1.54 we arrive to

$$\Delta V_{G1} = \frac{|e|}{C_{G1}}, \quad \text{and} \quad \Delta V_{G2} = \frac{|e|}{C_{G2}}. \tag{1.56}$$

Comparably, we can extract the voltage influence of one dot by adding a charge in the other dot. We write that $\mu_1(N_1, N_2, V_{G1}, V_{G2}) = \mu_1(N_1, N_2 + 1, \Delta V_{G1}^m + V_{G1}, V_{G2})$, which results in

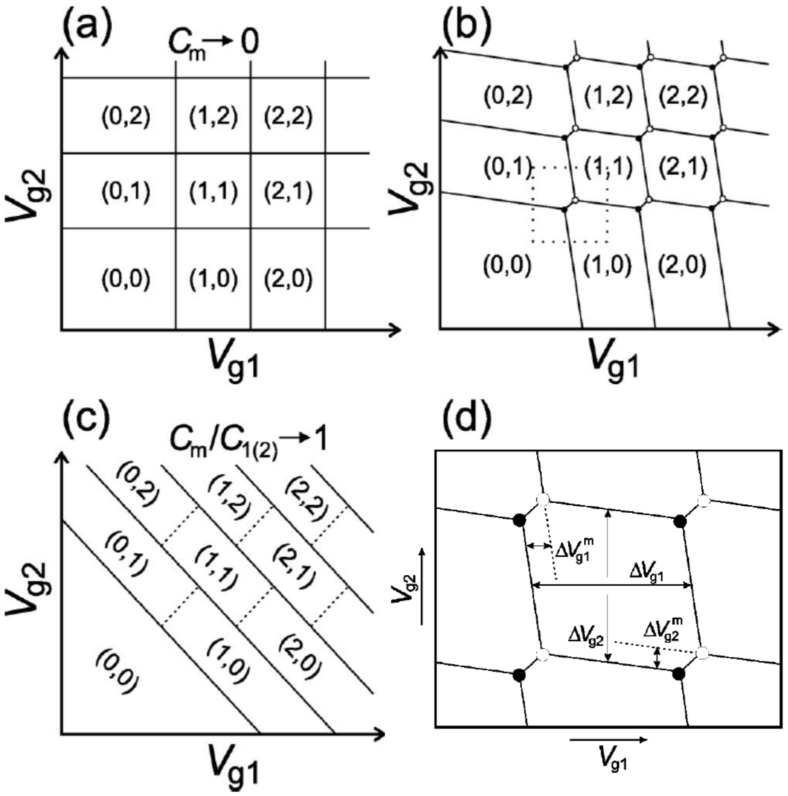


Figure 1.15: This plot shows some schematics of the charge stability diagram of a DQD. We see in both axis the plunger gate voltages for gate 1 versus gate 2. The numbers inside each section indicates the charges in both quantum dots (N_1, N_2). The difference among each plot is the coupling between the quantum dots C_m. In a), we see the case for two uncoupled quantum dots where each chemical potential is control by its own gate. In b) there is a finite coupling which affect the charge configuration, and we observe the honeycombs features. We can also appreciate the slope in the charge transition which comes from the cross-talk between a dot and the other dot's plunger gate. In c) we see the case where the coupling between dots is too large. In this regime, the system behaves as a big single quantum dot whose chemical potential is controlled by the two plunger gates. c) represents a zoom into a honeycomb from which we can extract some electrostatic capacitance, like C_{G1} and C_{G2}. Figures taken from [4].

$$\Delta V_{G1}^m = \frac{|e|C_m}{C_{G1}C_2} = \Delta V_{G1}\frac{C_m}{C_{G2}}. \tag{1.57}$$

For the other dot is

$$\Delta V_{G2}^m = \frac{|e|C_m}{C_{G2}C_1} = \Delta V_{G2}\frac{C_m}{C_{G1}}. \tag{1.58}$$

Triple points and charge lines

In order to understand a bit more the charge stability diagram, we will focus on the region between the states (0,0) and (1,1). We can see in figure 1.16 a schematic of these charge states. In the plot we find the called "triple points". They are called like that because the two dot chemical potentials μ_1, μ_2 are aligned with the source-drain chemical potentials μ_S, μ_D, and there is conductance at zero bias. The two triple points in the schematics are $\mu_S = \mu_1(0,0) = \mu_2(0,0) = \mu_D$ and $\mu_S = \mu_1(1,1) = \mu_2(1,1) = \mu_D$. In the diagonal line which join both points, the chemical potential of both dots are aligned. This line is called "interdot" line.

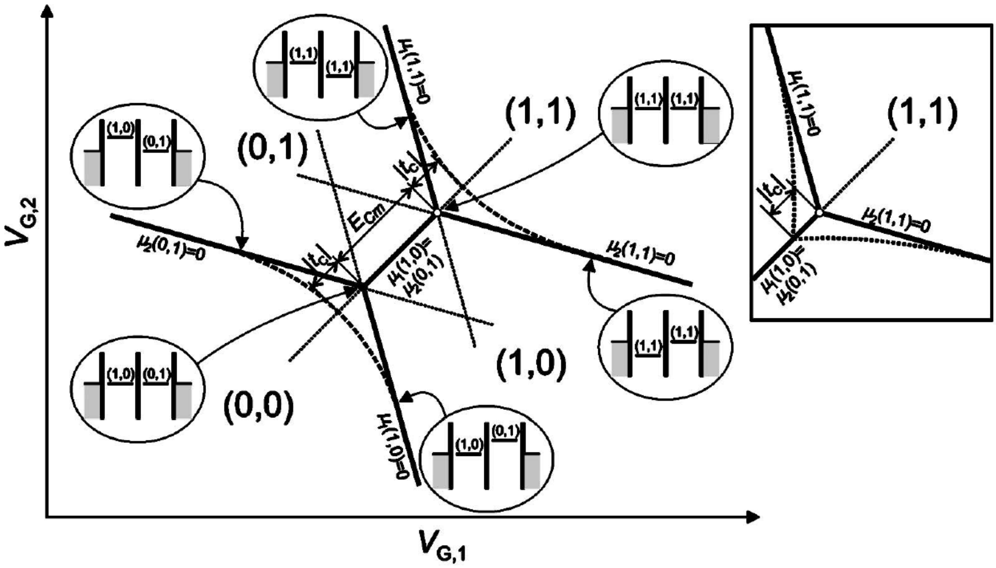


Figure 1.16: Schematic of the triple points in a DQD. We see the change between the regions (0,0) and (1,1). In this schematic, the source and drain electrochemical potential are grounded $\mu_S = \mu_D = 0$. Figure taken from [66].

From the schematic we can also appreciate the difference between the dot coupling C_m and the tunnel ratio between the dots t_c. The effect of C_m is reflected in the cross-talk between the plunger gate on the other dot. It bends the charge stability lines and create the apparition of the interdot lines. The tunneling rate is a pure quantum effect. Charges have a possibility of tunnel through the barrier between dots. The effect on the charge stability diagram is the rounding of the corners in the triple points.

In the schematic we can also see the charge lines. Those lines represent the edges of the charge regions. For a charge to be loaded in one of the two dots, it is necessary to align the electrochemical potential of that dot with the reservoir. This event does not produce current through the device. In order to observe them we need other techniques like charge sensing [76], [77], [67].

Bias triangles

The DQD signature of current measurement are the bias triangles. When a finite bias voltage is applied between the source and drain reservoirs $\mu_S - \mu_D = |e|V_{\text{bias}}$, the triple point seen in the previous section becomes a bias triangle. Now, we have opened a window through which transport can occur. The size of the bias triangles is directly related with the bias voltage V_{bias}. We can see the experimental data of two bias triangles in figure 1.17 a) and b). We can observe how a larger bias increase the size of the bias triangles. Transport through the excited states is also visible. In figure 1.17 c) we can see a schematic of the triple points with a finite bias applied. In figure 1.17 d) there is a zoom into on of the triangles, with special attention to the QD excited states.

The same way as in the SQD, each of the DQD has quantum excited states. In the regime where $h\Gamma \ll \Delta E$ we can observe transport through the excited states, as it is represented in figure 1.17 c).

1.2.5 Charge sensor

As it was mention before, the charge sensing is a measurement technique to observe the charge transition in the quantum dots. It was first performed in 1993 by M. Field et al. [76]. The idea is to use the capacitively coupling between the QD and a quantum transport device nearby. Schematic in figure 1.18 a) shows the system's capacitively model. In the beginning, a QPC was used [67] (as it shown in figure 1.18 b)), but eventually, the charge sensing was also performed with QD [52].

The physics behind this device is that a small change in the dot charge $\Delta Q = |e|$ will produce an effect on the QPC electrostatic environment of a magnitude $\Delta V_{QPC} = |e|/C_{QPC}$. This change in the QPC voltage can be observed in the QPC conductance as an abrupt step. In figure 1.18 c) we can see a plot of a QPC coupled to a DQD device. The top curve is the current of the last QPC plateau and the bottom plot is the QPC conductance while sweeping the interdot gate in the DQD device. We observe each time a charge is charged (or discharged) into the left QD as a displacement in the conductance through the QPC.

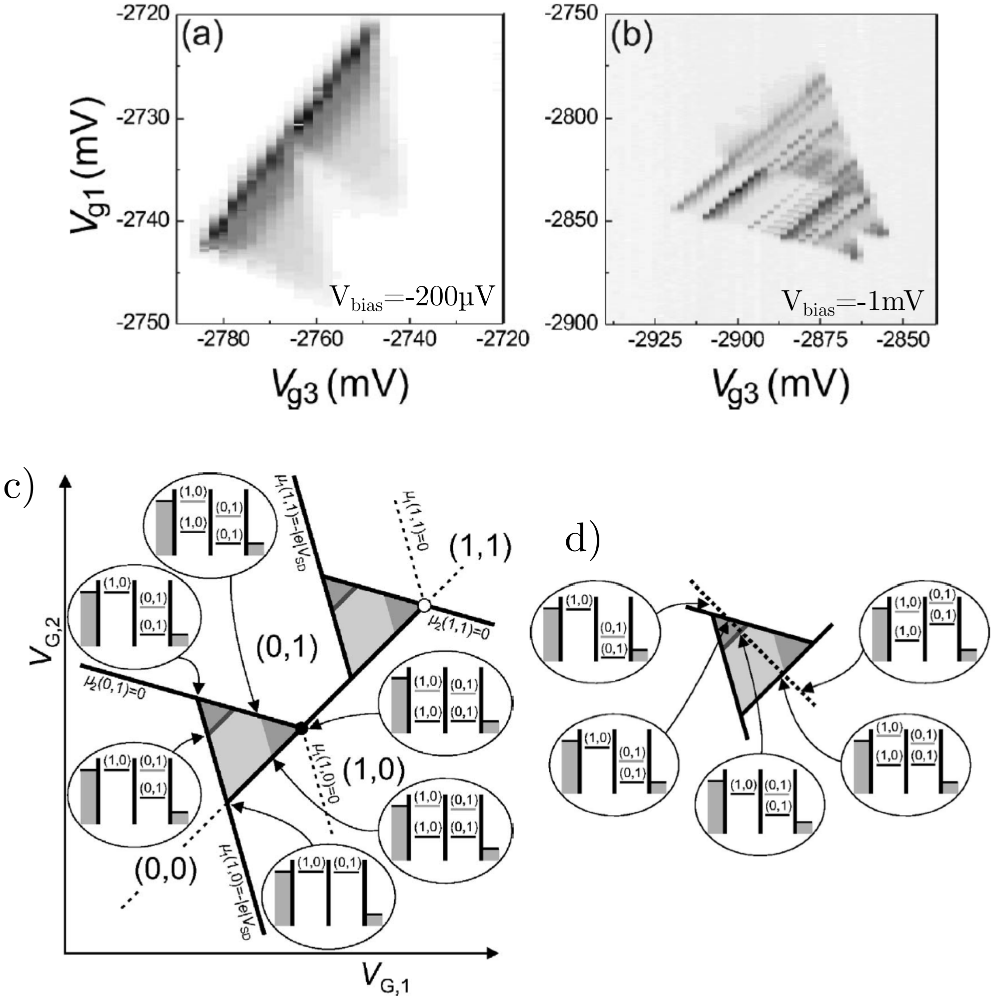


Figure 1.17: a) and b) show two measurement of two bias triangles taken from [4]. The difference between plots is the bias voltage. At the bottom there are two schematics of the triple points under a source-drain bias $\mu_S - \mu_D = |e|V_{bias}$. In b) we see the two bias triangles created between the charge regions (0,0) and (1,1). We can also see the charge edge regions lines. c) shows a close look into a single bias triangle. We observe better the transport through the excited states of the quantum dot. The triangle base is the conduction through the ground state in each dot. The other lines raising in the middle of the triangle is transport through at least one excited state. Bottom figures taken from [66]

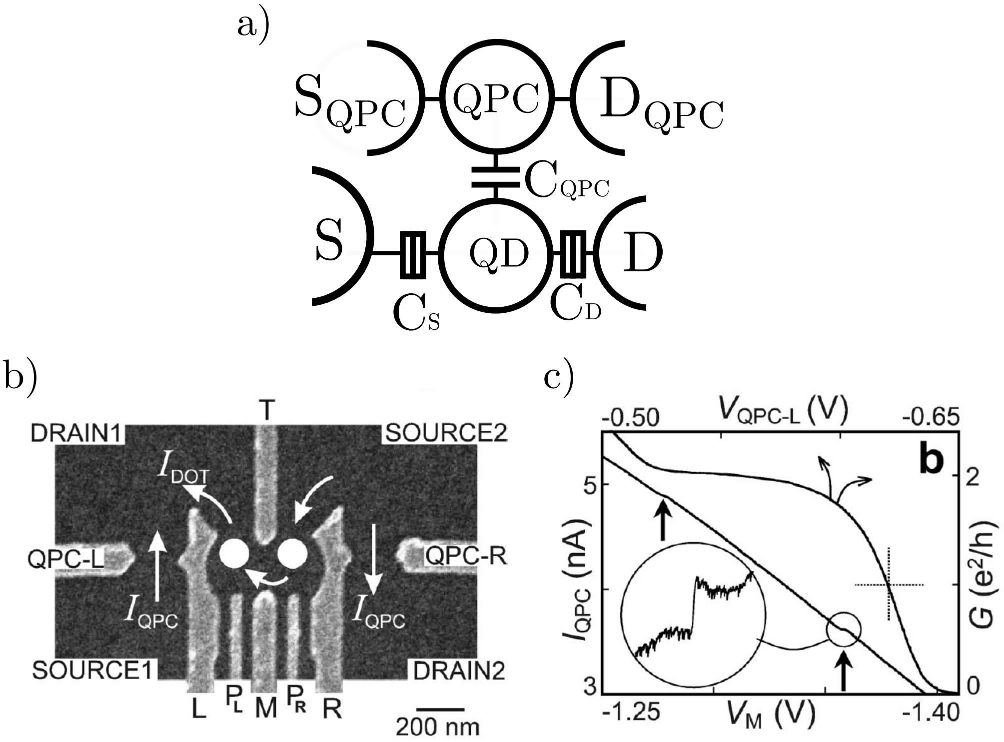
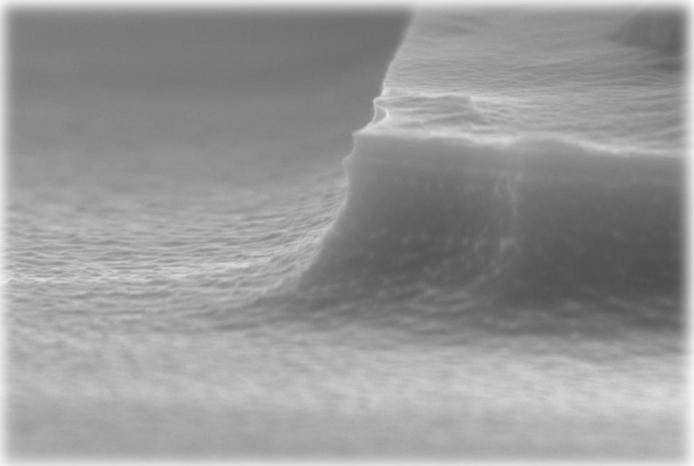


Figure 1.18: a) charge sensing schematic in a SQD. In this case, it is a QPC capacitively coupled to the dot with C_{QPC}. b) SEM picture of a DQD with two QPC in the extremes to measure charge sensing, image is taken from [67]. c) typical plot from a QPC charge sensor. The top curve is the QPC conductance versus the QPC gate. We observe the last conductance plateaus and the cross indicates the QPC voltage chosen to perform the charge sensing. Bottom curve is the QPC conductance while sweeping the interdot gate. We can observe the flat regions in the conductance, indicating a change in the QPC gate voltage of $\Delta V_{QPC} = |e|/C_{QPC}$. This is produce by a charge moving in the DQD device.

Chapter 2

Fabrication



Fabrication of devices is, without any doubt, a fundamental brick in the quantum physics research. Complex and technological challenges must be overcome to build nanometric size structures. In fabrication, development dynamic consists in a good amount of process characterization and optimization feedback. In this chapter, we will explore the fabrication for our quantum devices, specially focus on quantum dots development. The chapter will start with an overlook to the features needed to create and measure quantum devices and the bibliography support. Second part is a brief description of the Ge/SiGe heterostructure growth. After that, all the different fabrication steps are discussed in detail. Last section is the recipe that we found to be optimal.

SEM picture of a mesa edge.

2.1 Introduction and overlook to the process

The fabrication process consists in several steps. We start with the optical markers, follow by the ohmic contacts. Then, mesa structures and dielectric are built. We finish the devices with the metallic gates. Image in figure 2.1 a) shows a top schematic view of the sample. This image is a small portion of the total sample surface. The processed samples were 2 × 2cm. The pattern we see in figure 2.1 a) is repeated sixteen times.

First step is for markers, they are used all along the fabrication chain. We align for each UV lithography with these markers, and also for the first exposition inside the e-beam masker.

Next step is the ohmic contact fabrication. A schematic can be seen in figure 2.1 b). An ohmic contact consists in a metallic lead electrically connected to the 2DHG. It is used to feed carriers into the quantum well and to drive current through the devices. The quantum well is Ge, a semiconductor. When a metal and a semiconductor enter in contact they form Schottky barriers at the interface. In order to avoid this phenomenon, we anneal after the ohmic contact deposition. An increment in temperature produces the Ge diffusion into metals, and vice-versa [78]. This new mix of metal and Ge does not behave a Schottky barrier anymore, but shows an ohmic behavior, even at low temperature. The electrical current flowing through such contacts experiences a resistance known as "ohmic contact resistance" [78]. Ge has the feature of hybridize with almost any metal [79, 80], and it forms good alloys. The easy-to-contact proprieties of Ge quantum well become evident when we see that Al [25], Pt [35] and Pd [51] have been used as ohmic contacts.

Another step in fabrication is the construction of a mesa. We can see a schematic in figure 2.1 c). Its purpose is to isolate the 2DHG in a small region of the sample, where the quantum devices will be located. The rest of the sample surface has the quantum well etched away. It is in this absence-of-quantum-well region where the gate's bonding pads are built. The absence of quantum well below the bonding pads avoids the possibility of shorting the 2DHG and the gates while bonding. This method is used in [35, 51, 55]. Other groups, like [49] and [81], rely on the oxide thickness below the gate's pads to avoid shorts. In our group, we already had some experience with mesa etching, so we decided to go for this method. Two possible ways of etching were considered; wet etching (with chemical compounds) and dry etching (with plasma leading to chemical-mechanical reactions). We tested both method looking for the optimal process for us.

Next step is the dielectric deposition, shown in figure 2.1 d). Its quality is directly related to the device performance. A big effort is invested in improving and studying new dielectric materials and new deposition techniques. Dielectric properties research is a scientific field in its own. There are different deposition techniques like Chemical Vapor Deposition (CVD) or Atomic Layer Deposition (ALD). We decided to go with ALD technique because of its conformal growth,

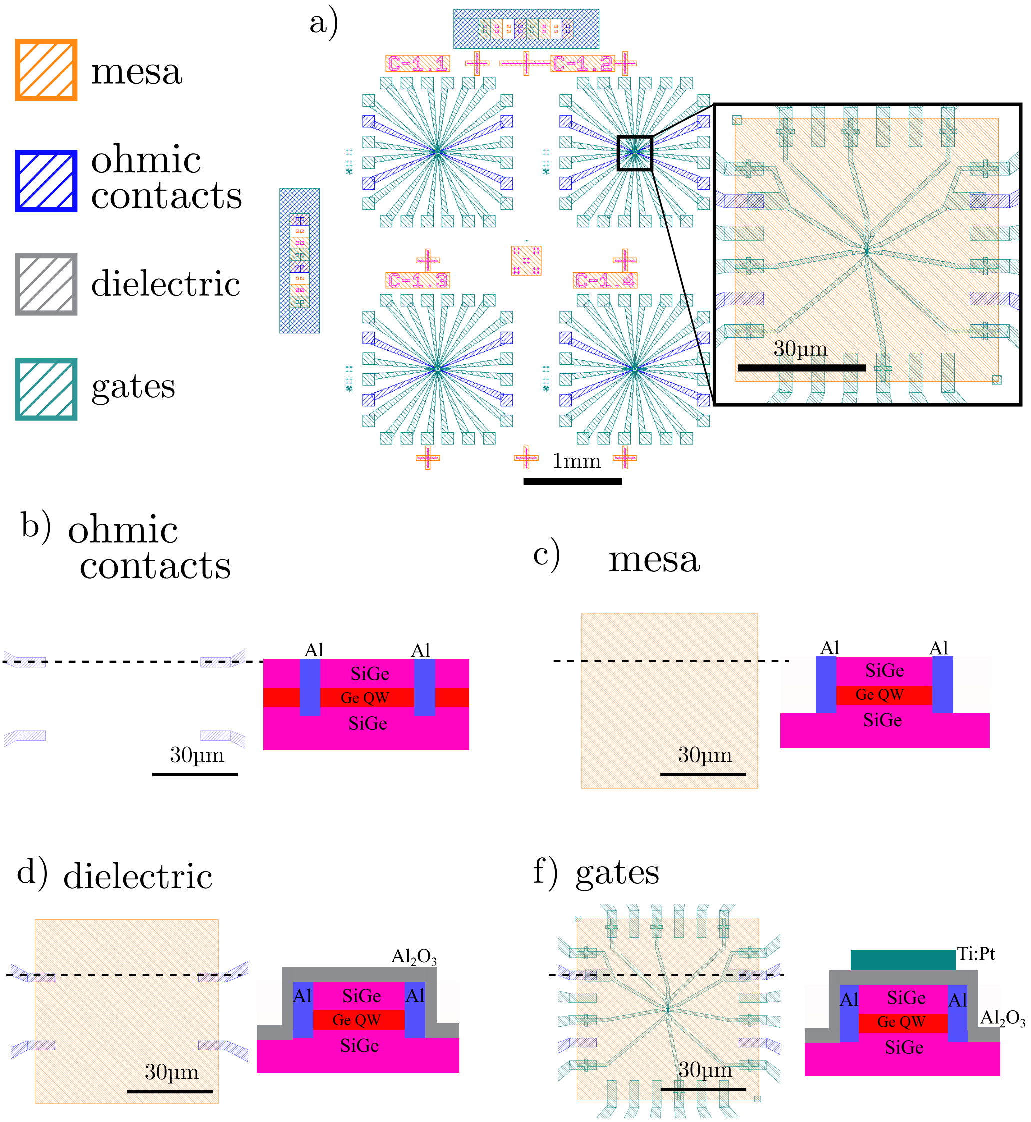


Figure 2.1: a) top schematic view of the sample. We observe four patterned structures, the optical and the e-beam markers, and the device names (C-1.1, C-1.2...). Each color correspond to a different fabrication layer. The inset image is a zoom into the mesa, where we can appreciate the metallic gates of a quantum device (in this case a DQD). From b) to f) there is a schematic for each step in the fabrication chain. It shows the mesa from the top view and a cut along the dashed line. The pictures are taken from the software *Klayout*, used for design the lithography patterns.

even in rough surfaces. Same as in [49] and [51], we decided to use Al_2O_3 as dielectric insulator. ALD works by sequentially mixing an active molecule with Al (trimethyl aluminium) and a precursor. Precursor role is to chemical activate the oxidation of the Al on the sample's surface. Historically, water was used as

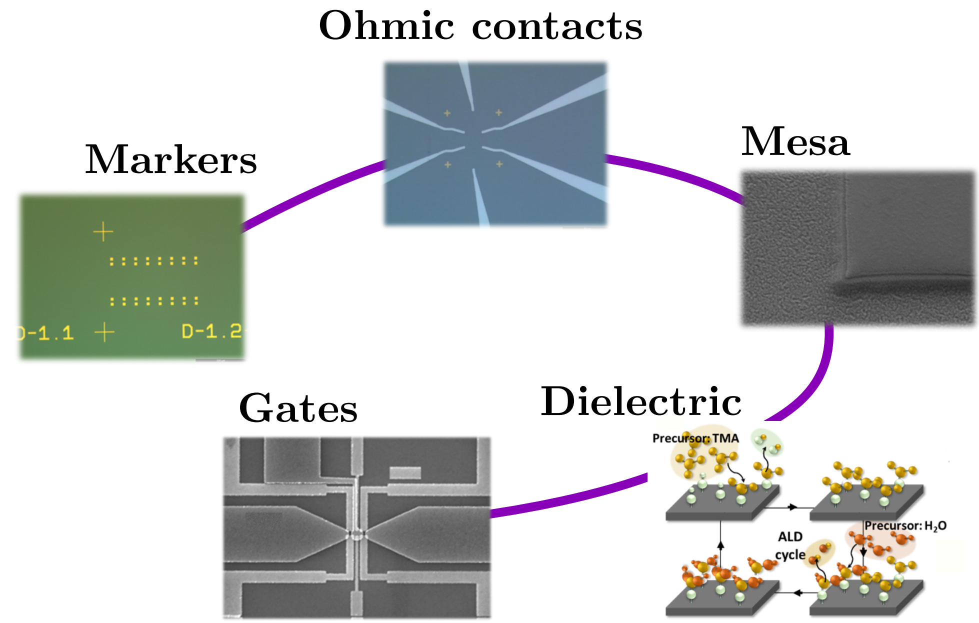


Figure 2.2: Representation of the fabrication steps with different images for each stage. All images are taken from our sample except the dielectric schematic, taken from [82].

precursor molecule in the ALD process, but in the last times, O_2 plasma has growth as a promising alternative [83, 84].

The last step in fabrication are the metallic gates. The technological advancements in lithography, like electron-beam lithography [85] and immersion lithography [86], allow the creation of nanometer size structures. In this thesis, we used an electron-beam masker for developing our QPC and QD devices. The QPC designs where pretty straight-forward, two metallic gates facing each other, same as in [87] or [88]. For QD, we can find lift-off designs where only a single gate layer is required. This is seen in GaAs devices [89–91], in Ge/SiGe heterostructures [25, 51] and in Ge-core nanowires [41, 92]. For some other cases, the QD were fabricated in a double gate layer. This process is used in undoped heterostructures where carrier accumulation is necessary like Si/SiGe [93–95] and Ge/SiGe [49]. In some other processes, instead of lift-off, gates are fabricated by etching. This is done in Ge/SiGe heterostructures [81] and also in CMOS nanowires [96].

In figure 2.2 there is a representation of all steps and the order we followed to fabricate them. Along the fabrication process, we used several machines in the PTA-CEA clean-room.

2.2 Ge/SiGe heterostructure fabrication

The heterostructure growth is done on a 200 mm Si(001) wafer by CVD at high temperature ($T = 850^\circ$C) and low pressure. Figure 2.3 a) shows a schematic of the heterostructure transversal view.

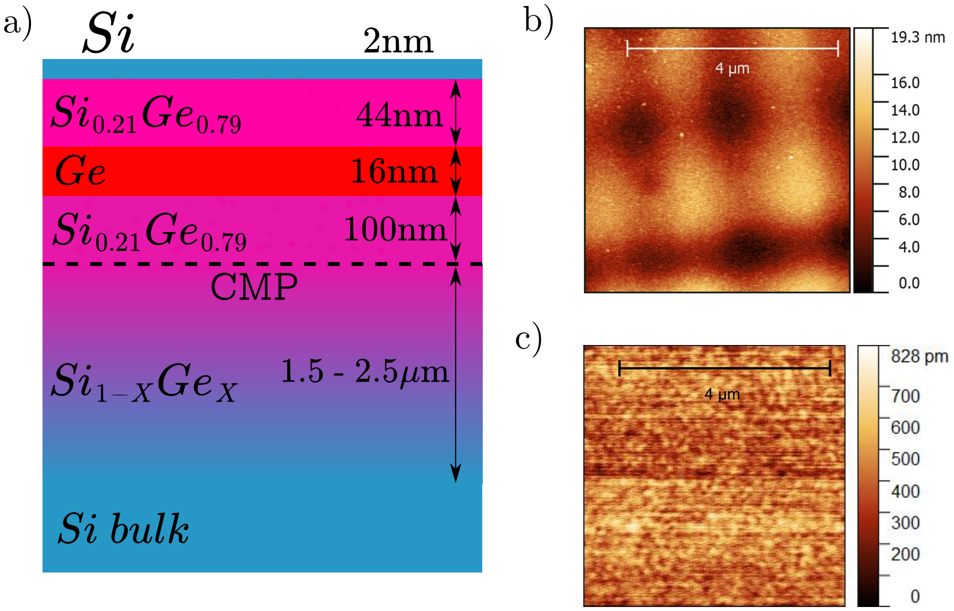


Figure 2.3: a) is a schematic of the heterostructure layer stack. b) and c) show two AFM images of the sample surface. b) is without the CMP step in the process and c) with the step.

The first step in the process is a SiGe deposition with an increment gradient in the Ge concentration. Being $Si_{1-X}Ge_X$ the heterostructure composition, with X ranging from 0 to 1, the process starts with X = 0 and increase until X = 0.79. The deposition is done over a thickness of several microns. We use an increment gradient because the dislocations and defects in the SiGe are reduced. On the other hand, the slow change in the lattice parameter produces strain in the semiconductor. We can observe the strain's effect on the sample surface. Figure 2.3 b) shows an image of a usual Ge/SiGe heterostructure surface. We observe a square pattern of several nanometers high. This effect is produced by the lattice strain. In order to get rid of that roughness, growers implemented a Chemical-Mechanical Planarization (CMP) step in the fabrication. With this technique the surface is flatted. Results can be observed in figure 2.3 c). Once the CMP is finished, we continue the deposition in the CVD for another 100 nm. At this point the 16 nm Ge quantum-well is grown. Its growth on the $Si_{0.21}Ge_{0.79}$ lattice creates a mismatch between the lattice parameter of the substrate (5.61Å) and the Ge (5.66Å). This mismatch forces a compressibility strain in the Ge lattice. The quantum well thickness is smaller than the Ge relaxation length, so all the quantum well is under strain. The strained Ge quantum well is then packed with a cap layer of $Si_{0.21}Ge_{0.79}$ of 44 nm thickness. Finally, all the process is capped with 2 nm of pure Si for surface protection.

2.3 Optical and e-beam lithography markers

Even though markers for lithography seems like a trivial step, it is not. Good markers are essential when several sequential lithography steps are performed, and even more if the process includes e-beam lithography. In our fabrication, we evaporate two set of markers at different stages in the process chain. The first ones are done with UV lithography and the second ones with e-beam lithography.

The first set is exposed just after the heterostructure growth. We use a mask aligner MJB4 with a UV lamp working at 365 nm wavelength and 6 mW/cm^2. The resist is AZ-1512-HS, which has a thickness of 1.2 μm. After some calibration, we found that 35 s of exposition time performs the best results. We also studied the different exposure methods availables in the machine: vacuum mode, hard contact mode, soft contact... Vacuum mode shows the largest precision. With the help of a plastic o-ring, the machine generates vacuum around the sample, between the mask and the sample holder. This reduction in pressure push the sample surface against the mask, making a full homogeneous contact and increasing resolution.

In figure 2.4 a) and b) there are two optical images of the UV lithography-made markers. Markers in a) are used for optical alignment and in b) for e-beam alignment. In figure 2.4 c) we see the second set of markers, done with the e-beam masker.

The e-beam masker uses a secondary electron detector to find the markers and align on them. We observed that the electron signal scattered from the quantum well interferes with the signal from the markers. For the same metal thickness, the marker's contrast when they were located above the quantum well was drastically reduced. To solve this problem, instead of gold as metal we used platinum, and at the same time we increased the marker's metal thickess up to 100nm. We evaporate 5:100 nm of Ti:Pt. This was not an issue for the second set of markers, the e-beam lithography-made. They are located at the bottom of the mesa, where there is not a quantum well. For those markers, the deposition is 3:32 nm of Ti:Pt.

2.4 Ohmic contacts

The ohmic contact lithography, similar to the mesa and markers one, was performed in a MJB4 with UV lithography. We use Al as leads, same as in the Delft group [25].

Al's diffusion rate in SiGe increase with temperature, but for the heterostructure, there is an upper limit of 400°C. If the temperature increase beyond that limit, the Ge in the quantum well starts to relax. The first time we tried to fabricate ohmic contacts, we directly evaporate Al in the top of the sample and rely on the Al diffusion through the dielectric, this process didn't work. We did not realise that Al does not diffuse across SiO_2, and the heterostructure was capped with Si, which naturally oxidized to SiO_2. For the next samples, we decided to etch the SiO_2 and the SiGe until we reached the quantum well, and then deposit

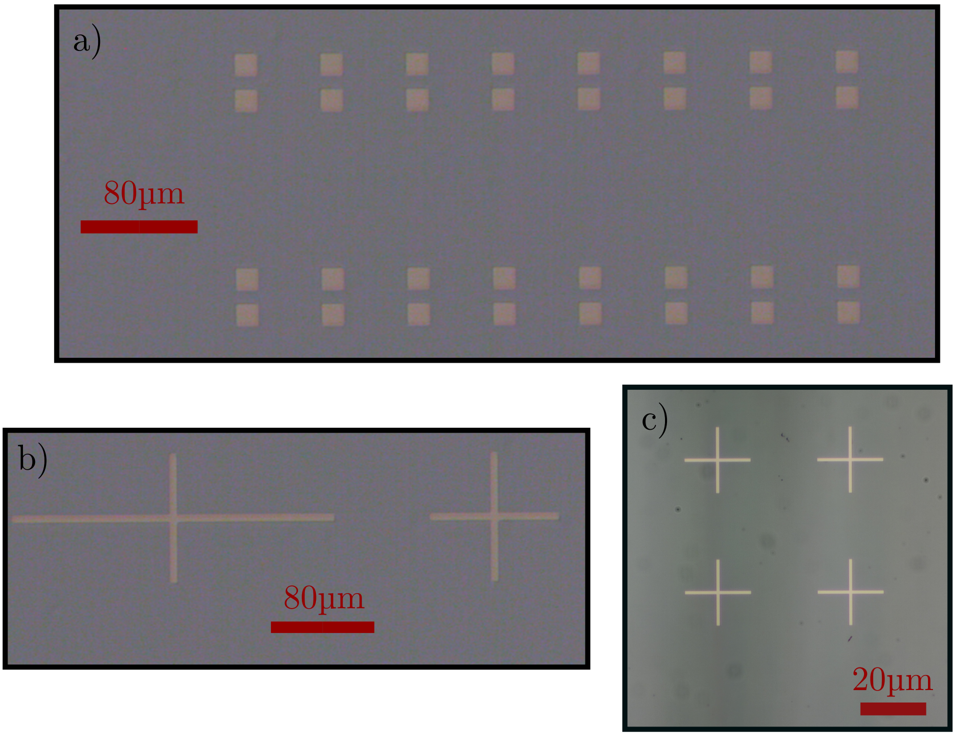


Figure 2.4: Three optical images for the different markers in the sample. Markers in a) and b) are done with UV lithography. a) squares are used to align the different UV-lithography layers. b) crosses are used in the e-beam masker. c) show the markers done with the e-beam lithography.

the Al. This process was successful, and we manage to have ohmic contact. Results for both process with some schematic can be seen in figure 2.5. In order to study a bit further the metal/Ge interface, we compare an annealed sample and a not-annealed sample, also shown in figure 2.5.

The no-etched curve in figure 2.5 plot, clearly shows an open circuit, the Al ohmic contacts never reached the quantum well, so there is no conduction through the sample. In the other cases we observe a current flow. At small bias, the resistance for non-annealed sample is three order of magnitude larger than for annealed (2.5MΩ versus 3.3kΩ). Also, the curve shape is different. For the annealed sample, the system is purely ohmic, while for non-annealed, there is a zero-current region at low bias. This behavior is the typical response of a Schottky barrier [97, 98]. At finite voltage, carrier tunneling through the Schottky barrier is induced because of the bias difference. If source-drain bias keeps increasing, the Schottky barrier replicates an ohmic contact with a tunnel-barrier resistance.

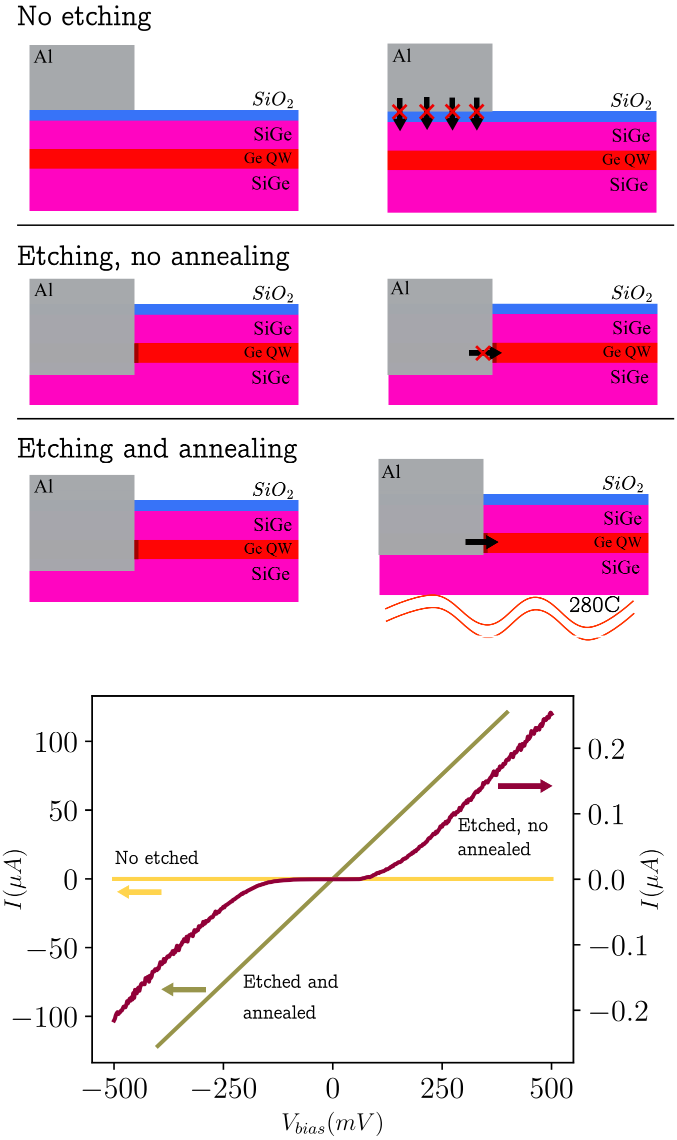


Figure 2.5: Schematic and resistance measurement at 4K for the three ohmic contact fabrication processes. When the Al is directly deposited over the sample surface, there is not an ohmic contact between metal and Ge. In the etched process but not-annealed, we found a Schottky barrier behavior. For the etched and annealed sample, the results were purely ohmic with a hole gas resistance plus the ohmic contact resistance of 3.3 kΩ.

2.5 Mesa structure

For the mesa etching, we explored two different possibilities; wet etching and dry etching with ICP. In this step the lithography is also done with the UV lithography mask aligner, following the same process that for the markers and ohmic contacts.

2.5.1 Wet etching

The chemical solution used for wet etching, which is taken from a recipe to etch Si and SiO_2, was HF : HN_3 : H_2O with proportion of 10 : 26 : 20. After several trials, we never manage to have a reproducible process. In figure 2.6 c) and 2.6 d) we present two profilometer measurements of two samples. In principle, the processes used for both samples are equal, but the mesa thickness are different by 50 nm, around a 50% of the total thickness. We were having this kind of results for every test we did.

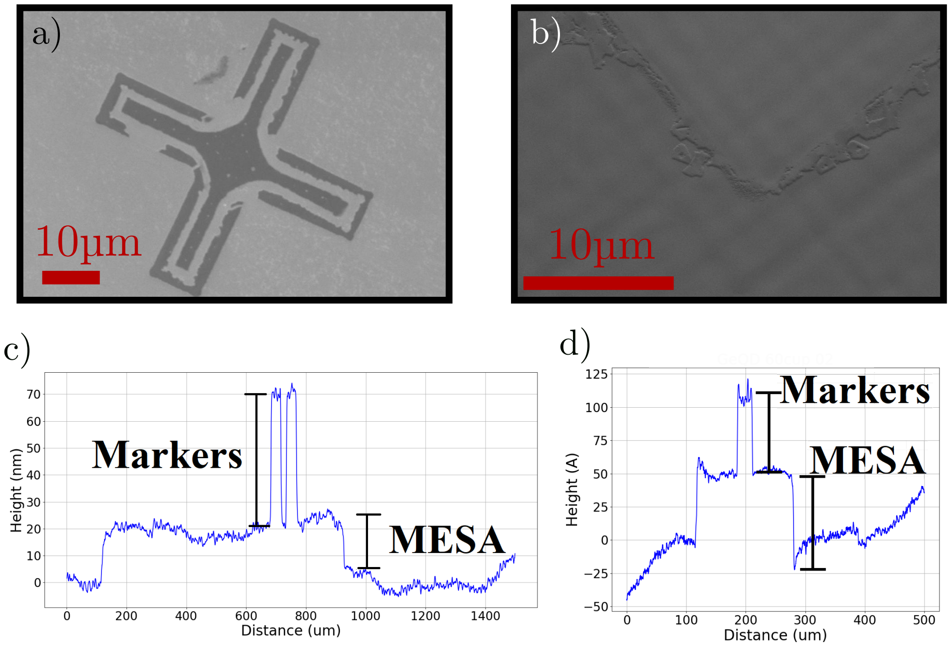


Figure 2.6: a) and b) show two SEM images of two mesas etched with wet etching. We can observe that the mesa edges are not clean and straight. It looks like the wet compounds diffused below the resist and etched the mesa from the sides. c) and d) are two profilometer measurement of two mesas in different samples. Both etching time were 3 min, but c) mesa thickness is 20 nm and d) is 75 nm.

Each time we perform a wet etching process, there are a few parameters that need to be exactly the same, and are human dependent: the amount of each compound, the etching times, the temperature, the aging of the solution... A small variation in any of those parameters would create a different process's etching rate. May be for long etching (several microns), where a bigger absolute error can be tolerated, it is not a problem to have this variability in the etching ratios. For us, this was not the case. We were looking for a nanometer-scale precision. We found another drawback of using wet etching, it is the final etching profile. In figure 2.6 a) and 2.6 b) we can observe some SEM images of the mesa after the etching. The profile is not clean and eventually, this would be a problem for growing quantum devices gates.

After the previous results, we decided to continue the development with dry etching. Results will be shown in the next section.

2.5.2 Dry etching

We already had a SiGe etching recipe previously developed in the group. It consists in a mixture of CF_4 : Ar with 10:40 sccm. This recipe produces a vertical etching. It has good reproducibility and a known etching rate. There is one issue with this method, we were not looking for a vertical etching but for smooth slope edges. The reason for this is that for a thin metal layer (≈ 10nm) it would be easier to make a contact between the top and the bottom of the mesa. Two schematic images are represented in figure 2.7.

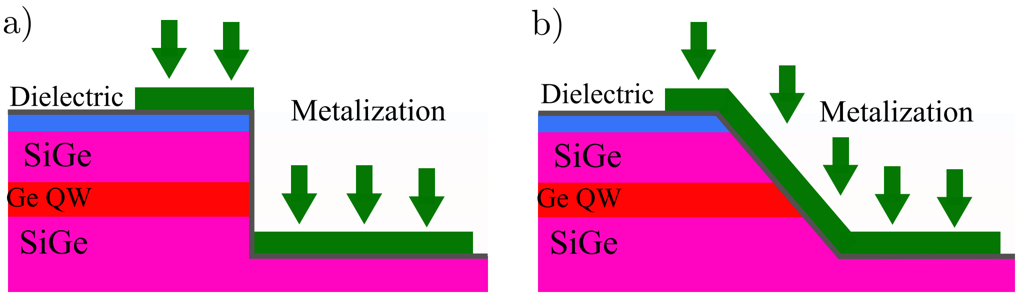


Figure 2.7: Schematic of a transversal view with a vertical etching process in a), and a sloppy edges in b). We want to illustrate how, for a gate deposition, the profile in b) allows a non-interrupted metal contact between the top and the bottom of the mesa. This is true for any gate thickness smaller than the mesa.

We started testing other recipes with $SF_6 : O_2 : CH_2O_2$ [51]. We tried different pressures, plasma power and ratios. Our objective was to find a reproducible etching process leading to a smooth mesa edges. Some examples of these experiments can be seen in figure 2.8. In terms of reproducibility, dry etching was more stable than wet etching, but taking some precautions. Because of the heavy usage of the ICP machine in the clean-room, the main chamber atmosphere was constantly changing. We always took the precaution of cleaning the chamber before using it We also performed a special conditioning for our process. The cleaning consisted in a 1000W power plasma of O_2 for 10 minutes. The conditioning was done by running the etching recipe for 5 minutes, but without a sample inside the machine. This way the inside atmosphere was already saturated with the same gases as for the etching recipe.

The smooth angled mesa edges were a complicated issue to achieve, we thought that an isotropic etching would help to create the desired profile. The problem is that there are too many parameters interfering in the process: chamber pressure, gases flows, ICP power, RF power, etc... The work flow for recipe optimization consisted in applying changes in one parameter at a time and observe the results in the SEM. From the microscopy images we decided which parameter gave the

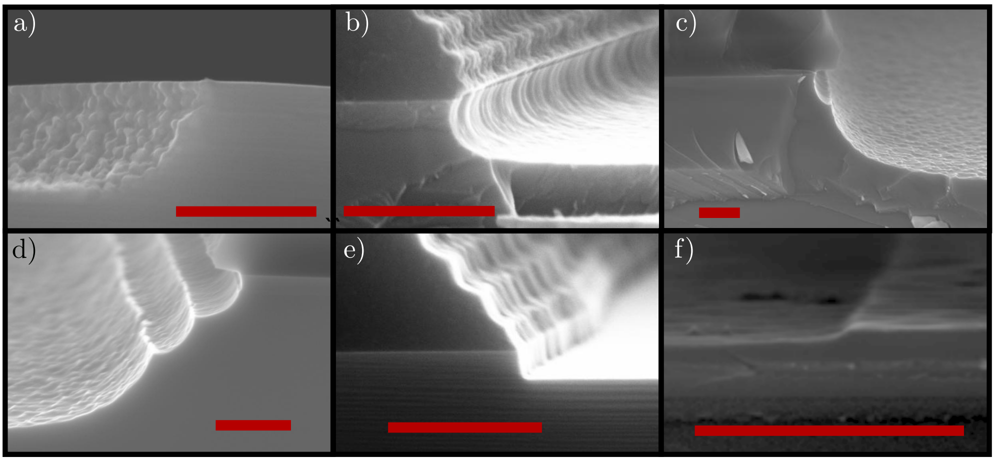


Figure 2.8: SEM images of the different test sample for the mesa etching step. Scale bar is 100 nm for every image. We can observe the huge variety in the mesa profiles. From a very roughness surface in a) to a step-edge mesa in c) and d). Somehow we did some wave-like border in b) and a totally vertical etch in e). When we found f), we considered it a success and save that recipe for all the samples.

best result, keep that parameter and proceed to change another one. A wide variety of recipes were fabricated. A selection of mesas can be seen in figure 2.8, each of them with a different recipe. After a quite large amount of tests, we found the desired conditions in 2.8 f). The approach we followed in this last recipe was to decrease as maximum the plasma power (15W) while the chamber pressure is relatively high (4Pa). We observed that this condition decreases the etching ratio and produces a more isotropic etching.

2.6 Dielectric growth

The dielectric used in our fabrication process is Al_2O_3 grown by ALD . The groth temperature is 280°C, the machine limit. High temperature helps to grow a better quality dielectric and, at the same time, diffuse the Al deposited in section 2.4 to form ohmic contacts. We studied five different processes to deposit Al_2O_3, table 2.1 presents a summary.

Oxide thickness (nm)	Precursor	Surface pre-treatment	Temperature
7	water	-	280 $(°C)$
7	water	NH_3	280 $(°C)$
7	O_2 plasma	NH_3	280 $(°C)$
7	O_2 plasma	10 min O_2 plasma	280 $(°C)$
10	O_2 plasma	10 min O_2 plasma	280 $(°C)$

Table 2.1: Summary of ALD parameters.

In order to compare the quality among the different processes, we fabricated samples with two metallic layers separated by the ALD dielectric. For each layer, we imprint a pattern of long metallic leads. The second layer is rotated 90° from the first one, so the leads cross each other and create an array of capacitors. Figure 2.9 a) shows a sample's schematic. The experiment's objective was to measure the voltage value for which the current breakthrough the dielectric. To do it, we apply a voltage difference between two leads until we observe current, as it is shown in 2.9 b). This curve is the system response for one of the overlaps in the sample. We recover the data for many of the sample overlaps. In this particular plot, we observe a step in current at $V = 7.9V$, where the current saturates to the DMM limit ($0.5\mu A$). The inset image shows a zoom into the beginning of the step. We can observe how the current increases exponentially. In our experiment, we consider the dielectric broken at this voltage value.

For the two first samples in table 2.1, with water precursor, the number of broken contacts (short contacts before applying any voltage) was extremely high. More than 3/4 of the capacitors were broken. We found no difference between the NH_3 pre-treatment sample and the other. Because of that reason, we directly rejected these fabrication processes. For the O_2 plasma precursor results were more promising. We can see in figure 2.10 a histogram of the breakthrough voltage for each sample. Between the sample without pre-treatment and the sample with NH_3 there is not too much difference. It seems like the second one has a bigger dispersion, but the statistic is small to get a clear conclusion. Where there is an obvious difference is in the 10 nm oxide thickness. More thickness increase the field limit for which the dielectric breaks. The average voltage is increased with respect to the other two samples. The median in voltage for each sample is: 7.4V for the 7 nm Al_2O_3, 7.8V for the 7 nm Al_2O_3 and NH_3 pre-treatment and 8.4V for 10nm Al_2O_3 and O_2 plasma pre-treatment.

There is another comparison possible. We can count the number of broken contacts and compare it with the total number of contacts measured. These short may come from a badly deposited dielectric. The yield is defined as

$$Y = \frac{\text{broken contacts}}{\text{total contacts}}. \tag{2.1}$$

We found $Y = 0.66$ for the 7 nm oxide sample, $Y = 0.43$ for the 7 nm oxide and NH_3 pre-treatment and $Y = 0.32$ for the 10 nm and O_2 pre-treatment. In this analysis we observe that the 10 nm thickness with O_2 plasma pre-treatment has the lower yield. Thicker dielectrics have a higher resistance to shorts, so it could be that the slight improvement in yield is not because of the precursor, but because of the increment in thickness. Finally, for our fabrication process we decided to continue with the 10 nm O_2 precursor dielectric and the 10 min of O_2 pre-treatment.

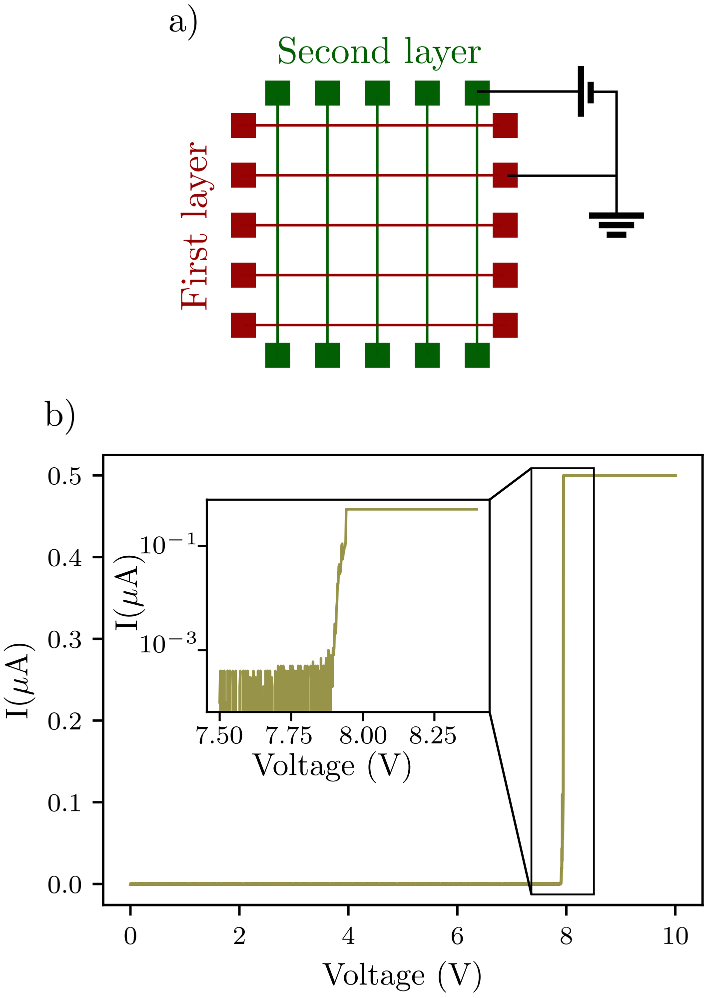


Figure 2.9: a) shows a schematic representation of the sample. Two layers with a dielectric between them. The experiment consists in applying voltage to two gates at different layers and observe the breakthrough voltages. b) typical plot of current versus voltage showing the breakthrough voltage. In the plot it occurs at $V = 7.9V7.9\,V$. The inset figure is a semi-log plot around the break through voltage. We can observe tunneling current before the dielectric breaks.

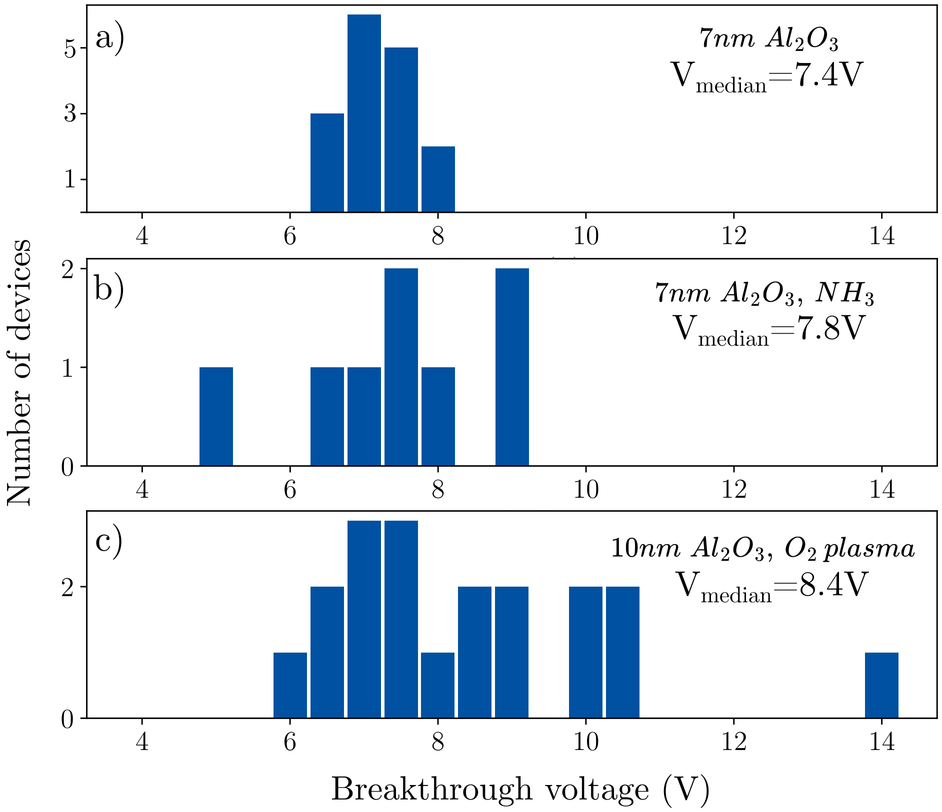


Figure 2.10: Histograms representing breakthrough voltages of three different dielectric growth process. It exists a tendency towards higher voltages values with the use of precursor. A correlation between oxide thickness and higher voltages can also be observed.

2.7 Metallic gates

The final step in the fabrication process is the metallic gate construction. Up to now, fabrication is the same for any kind of sample; QD, QPC, FET... It is in the last step where, depending on the experiment we want to perform, we design the device gate layout. For the big structures (FET, Hall-Bars, and those whose features are $>2\,\mu$m) we use UV lithography. For small structures (QD, QPC, and those whose feature are $<2\,\mu$m) we use the e-beam lithography masker.

The conditions for the UV lithography gates are equal to those previously discussed. We use the MJB4 mask aligner with the AZ-1512-HS resist. In figure 2.11 we see an example of a FET device done with UV lithography. It consists in a NbN metallic layer which overlaps, at least, two ohmic contacts. This sample was fabricated before the bevelled mesa edge recipe was fully developed.

In the next sections we will comment on the results we obtained with the e-beam lithography masker.

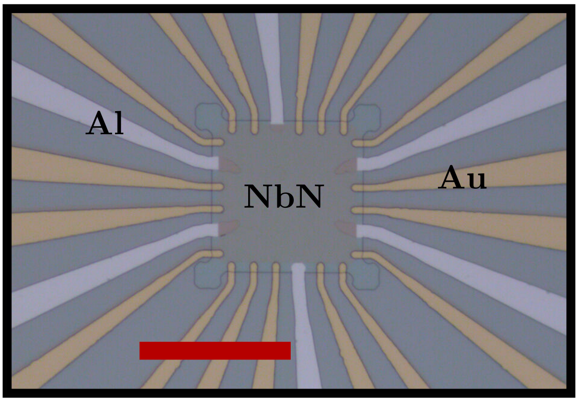


Figure 2.11: Optical image of a FET. Scale bar is 50 μm. We can see the top of the mesa covered with a NbN metallic gate which overlaps six Al ohmic contacts. The Au gates are used to connect the NbN with the bonding pads, located at the end of the gates (out of the picture).

2.7.1 One layer, NbN etching

Our first approach was to develop a recipe to work with a 10 nm thickness layer of NbN. The metal was deposited by sputtering, and it covered all the sample's surface. The idea was to etch the metal from all the surface except from the mesas. We did a UV lithography exposition to protect the mesas and then, dry etched non-covered NbN with the ICP machine. Once there was only NbN on the mesas, we patterned the gates with the e-beam lithography masker. After the gate lithography was done, we etched again with the same recipe. This technique has some advantage: only one gate layer was needed. Even more, future implementation of a high impedance superconducting resonator would be easier, since it can be fabricated with the same metal [99]. At some point, we abandoned the idea because of the difficulties found in resolving the QD gates.

In the clean-room, the e-beam masker machine is shared among several research groups. The strong usage of the machine forces that two masker parameters were fixed, and we could not changed them. The e-beam current was fixed at 1 nA, and the potential at 1000 kV.

Figure 2.12 show four SEM images of different devices patterned in NbN. The etching process was the same for all four samples, it is summarized in table 2.2. Resist used for the lithography is also the same: ZEP. We can observe that the SiO_2 substrate has better resolved gates than the Al_2O_3. It turns out that the etching described in table 2.2 also etch SiO_2, and even at a higher ratio that NbN. We relate the well-defined gates in 2.12 a) to the fact that the gases kept etching the substrate once the NbN is fully etched. This generates more surface chemical reactions and avoids metal redeposition. As opposite, on Al_2O_3 the etching is abruptly stopped, so the gases start to react with the metal below the resist by

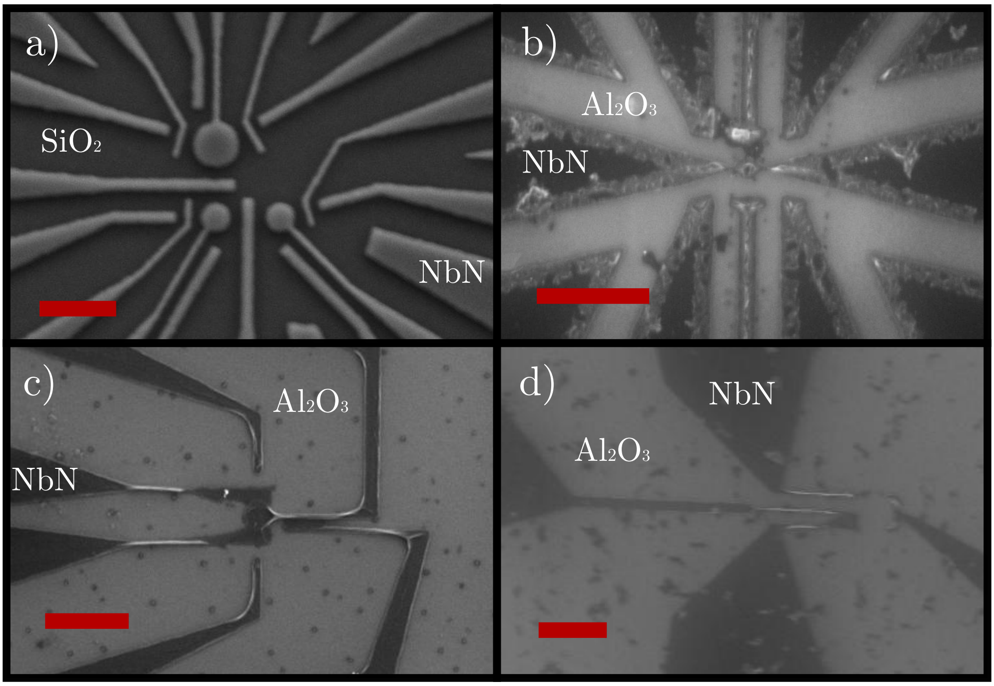


Figure 2.12: SEM pictures of NbN gates, scale bar is 500 nm for the four images. In a), substrate is SiO_2 and dose is 360 $\mu C/cm^2$. For b), c) and d), substrate is Al_2O_3 and doses are 350 $\mu C/cm^2$, 280 $\mu C/cm^2$ and 245 $\mu C/cm^2$. The etching used for the NbN also etch SiO_2, but not Al_2O_3. That is the reason why lithography in a) seems cleaner and well-defined while in the other pictures is the opposite.

side contact and etch it horizontally. In the SEM images b), c) and d) we can see some border features around the gates, typical from redeposited metals. We can also see the dielectric surface with some cross-linked resist leftover.

This problem could have been solved by changing the dielectric to SiO_2, but this was not an option. The low thickness of 10 nm didn't allow us to try SiO_2 because of technical issues. In our clean-room, SiO_2 is grown with CVD, which does not assure good dielectric quality for thin layers. It also requires high temperatures, which compromise the Ge quantum well strain. We tried to overcome this problem with dose optimization and proximity effect correction, but never manage to have clean gates. We already observe in 2.12 that a dose change of 50% does not resolve the problem of gate definition. After all the difficulties we decided to try some other method.

Gases and flow (sccm)	ICP power	RF power	Pressure	Time
$SF_6(5) + O_2(10)$	0	50W	5mTor	40s

Table 2.2: Etching recipe to etch NbN and SiO_2.

2.7.2 One layer, Ti:Pt lift-off

The first new process we tried was single metal layer with lift-off. We changed the resist to PMMA 2%, the metal to Ti:Pt with 3 : 32nm thickness, and repeat the dose tests. In figure 2.13 we see four SEM pictures of a structure done with four different doses. We did more tests but figure 2.13 can summarize the results. As expected, the lower dose has the lower proximity effect. When dose increase, the effect becomes larger. For the dose 2000 μC/cm^2, all structures are already merged. One could think that the lower dose is the better, but this is not always true. For small structures (40 nm width gates), 1000μC/cm^2 was not enough to properly resolve the lithography. Then, we had to choose a compromise between not overdosing the structures and still be able to resolve every gate. We finally chose 1200μC/cm^2.

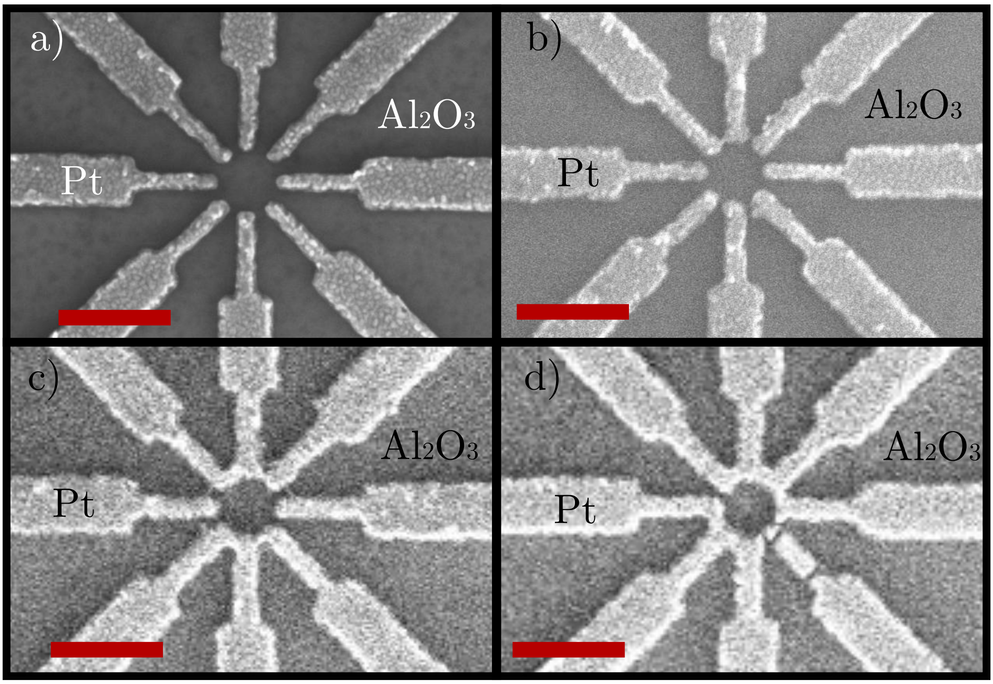


Figure 2.13: SEM pictures for lift-off test structures done at different doses: a) 1000μC/cm^2, b) 1200μC/cm^2, c) 1600μC/cm^2 and d) 2000μC/cm^2. Scale bar is 500 nm for each picture.

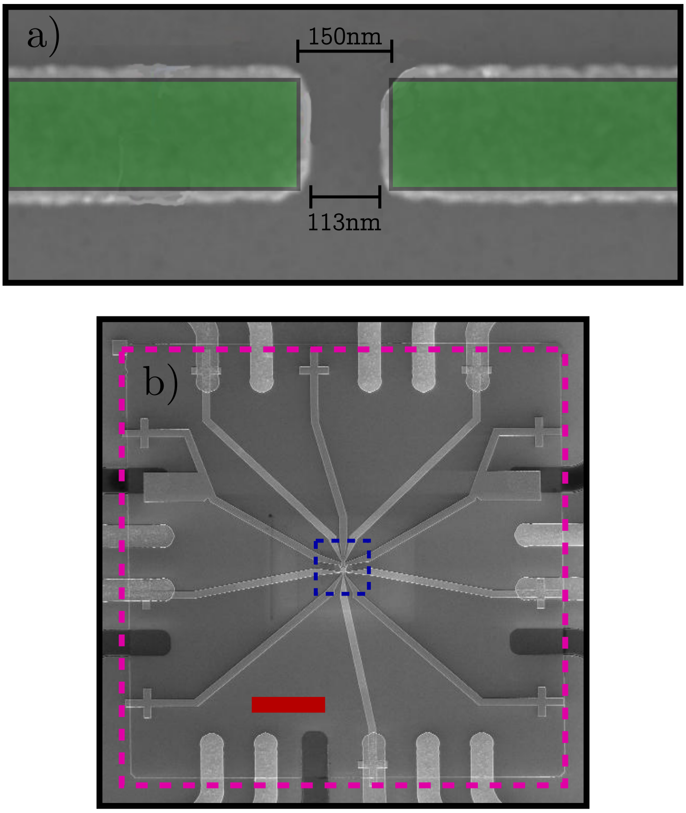


Figure 2.14: a) SEM picture of two lift-off gates with a colored region representing the original gate design. Because of proximity effect, resist is overdose and the final gate size increases: 20 nm in length and 10 nm for each side. b) SEM picture where we can observe the gates on the top of the mesa. The two colored squares represent the regions where the dose is $1200\mu\text{C/cm}^2$ (blue) and $1400\mu\text{C/cm}^2$ (purple). Scale bar is $10\,\mu$m.

After setting the dose, we had to face the proximity effect corrections in the gate shapes. Gates in the design are not exactly equal to the gate lithography in the sample. Proximity effect distorts the sizes. Even though there are software which correct this effect with physical calculation, we did it by hand. After all the dose tests, we could extract the increment in size for each gate. In figure 2.14 a) we see a SEM image of two gates with a gap in the middle and a colored region in green. The colored region is the original design of the gate. As we can see, they do not exactly match. From this and other similar test, we found a thumb rule to follow: increment in length is 20 nm and an increment in width is 10 nm, for each side. These two magnitudes were constant without any correlation to the gate width, at least in for small sizes ($<$ 500nm). This increment in size is really important because of the small dimensions for QD gates. We had to be really careful to don't pattern two gates too close to each other. Anyhow, always before depositing the metal for QD gates, we tested the dose with dummy devices to check that all the gates pop out correctly. We lose some time doing so, but definitely, less time than having to repeat the full fabrication process because some gates were merged.

There is another issue worth to discuss, it is related to the exposition field in the e-beam masker. The masker has a working field where it is able to electrostatically shift the electron beam to lithography the design. This field can have different sizes, but we always used the 62.5 μm one. The sample design is cut in square portions of 62.5 μm, each corresponding to an exposition field. When the structures inside a field are completely exposed, the machine mechanically moves to another field and continue with the process. It may happen that some structures are in two different fields. Then, a stitching problem in the masker would produce that some parts of the designs to not be exposed. These cuts are typically in the nanometer scale, around 50 nm. To avoid this from happening, we increased the dose close to the field edge. This exposes the possible gap. If it is done far from the quantum gate structures, there is not any risk of overdosing the small gates, and we avoid the field effect cuts. In figure 2.14 b) we see the e-beam lithography gates and the two regions for doses: the small structures $1200\text{cm}^2/\mu\text{C}$ region (where the QD are located, in blue) and the overdose $1400\mu\text{C}/\text{cm}^2$ region (in purple).

2.7.3 Two layers, Ti:Pt lift-off

We realised after the first measurements (discussed in the next chapter) that we needed another extra gate layer to have functional devices. Dose problems were already solved, but now we faced another issue: alignment. The original crosses done with optical lithography did not have enough resolution to align QD gate layers. The trend was having misalignment in the order of 200 nm, very far from the nominally 10 nm assure by the masker manufacturer. In figure 2.15 a) we observe a SEM image of the first layer for a DQD device. Figure 2.15 b) shows the same structure as in a) but with the second layer on top. To solve this problem, we started to imprint some markers at the same time as the first gate layer lithography was exposed. Image in 2.15 c) shows the same structure as in b), but align on the e-beam lithography markers. We observed an improvement in alignment precision. In 2.15 b), the bumps in the surface come from a not well cleaned exposition, issue that was solved for the next sample c). Finally, in figure 2.15 d) we see a well aligned SQD structure.

From this point on, we were able to fabricate different nanometric structures with good alignment and good resolution. Figure 2.16 shows two DQD examples.

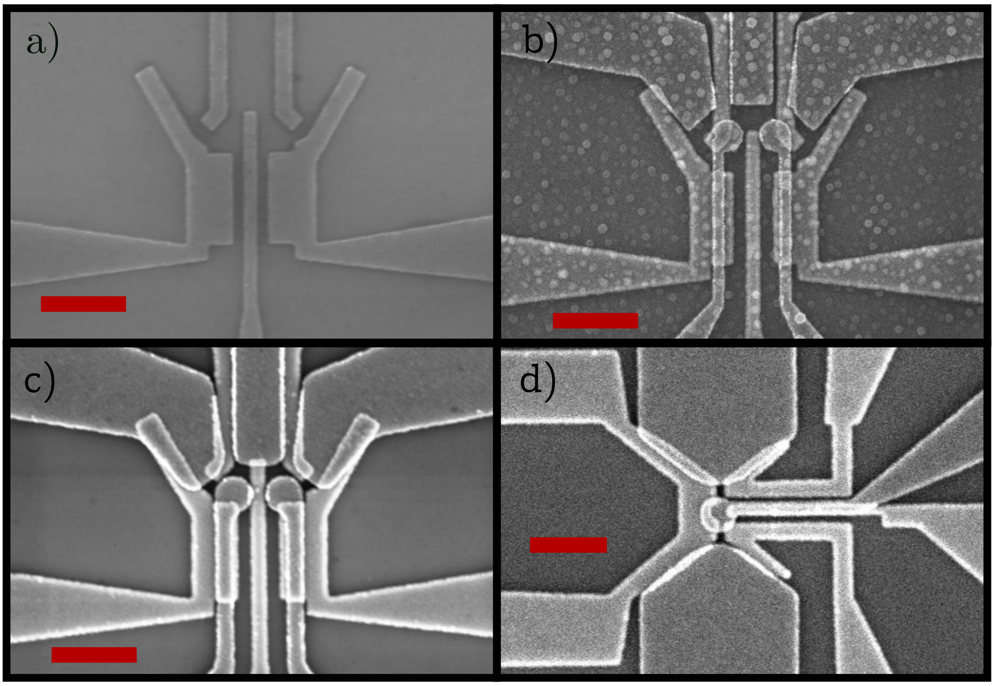


Figure 2.15: SEM pictures of QD gates. Scale bars are 500 nm. a) is the first gate layer of a DQD. b) is the second layer of a DQD whose lithography was aligned using the global markers, the one exposed with the UV-lithography. c) is the same second gate structure as in b), but align to the e-beam lithography markers. d) is an example of well-align SQD device.

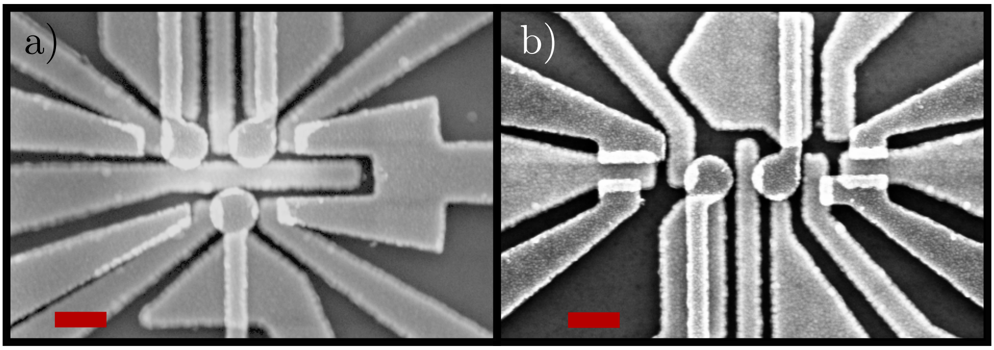


Figure 2.16: SEM images of full processed devices. Scale bars are 200 nm. Both are DQD, but a) has a charge sensor at the bottom and b) has two QPC at both sides of the DQD.

2.8 Conclusions

Here I will summarize all the fabrication processes and discuss what we believe was the best final option to choose. At the end, we came up with a recipe which was reproducible and achieve the objective of creating QD.

For every UV lithography exposition, we found the best resolution and reproducibility was given with vacuum mode exposure and 35 s exposition time. Resist is always AZ 1512 HS. Also, it is worth to mention that the development time is 35 s instead of the 30 s recommended by the manufacturer. In UV lithography markers, we observed the best results with respect to the e-beam masker alignment when the metals are $5:100$nm of Ti:Pt.

For ohmic contacts, the best results were given when we etched the heterostructure and contact directly the metal with the Ge quantum well. We also observed the importance of annealing to obtain clean contacts. Recipe for etching uses $CF_4 + Ar$ at 1.2Pa with 50W of RF power and 200W of ICP power. Opposite to the mesa etching recipe, this is a fully vertical etch. After reaching the quantum well with etching, 50 nm of Al was deposited in an EBM.

The mesa structure fabrication was a difficult step. The characteristics we were looking for are not easy to get: small etched distances (100 nm) and bevelled slopes. After quite some effort, we discarded wet etching because of lack in reproducibility. We chose dry etching with ICP. At the end of an optimal recipe research, we found one with $SF_6 + O_2 + CH_2F_2$ at 4Pa and 15W of RF power.

Dielectric growth was performed in an ALD machine. We used Al_2O_3 with 10 nm thickness. After testing water and O_2 plasma as precursor, we found plasma as the best option. The surface pre-treatment was also studied with NH_3 and O_2 plasma. Here, results were inconclusive from the lack in statistics. The dielectric deposition is done at 280°C. The high temperature diffuse the ohmic contacts into the quantum well.

Finally, for the quantum device gates, we discarded the single layer NbN etching because of the impossibility to obtain clean gates. We changed to lift-off using PMMA 2% as resist. Optimal dose for our structures was studied and we develop a thumb rule to correct the proximity effect, with very good accurate results. For first layer exposition, optimal doses turned to be 1200 and 1400μC/cm^2, the metal deposition was 3:32nm of Ti:Pt. Finally, for reason discussed in next chapter, we were forced to do a second gate layer. We faced some alignment issues that were solved by using the first gate layer as reference. Exposition dose was 1200μC/cm^2 with same metal gates thickness, 3:32 of Ti:Pt.

It is worth to say that developing this fabrication process was long and sometimes exhausting. The final recipe with which we were happy is shown in next section. We remind the final objective of this recipe is to form quantum dots in Ge/SiGe heterostructures. In the next chapters we will test our fabrication process in addition to the heterostructures characteristics. With the results from those measurements, we will conclude in the quantum dot fabrication viability.

2.8.1 Final fabrication recipe

UV lithography

MJB4

Resist	Exposition (time)	Developper (time)
AZ 1512 HS	Vacuum mode (35s)	AZ developper:DIE [1:1] (35s) + DIE (5min)

Markers

EBM

Metal	Thickness (nm)	Rates (nm/s)
Ti:Pt	5:100	0.5:0.5

Ohmic contacts

ICP

Gases (sccm)	ICP power	RF power	Pressure	Etch time
$CF_4(10) + Ar(40)$	200 W	50 W	1.5 Pas	25s

EBM

Metal	Thickness (nm)	Rates (nm/s)
Al	50	0.5

Mesa structure

ICP

Gases (sccm)	ICP power	RF power	Pressure	Etch time
$SF_6(15) + O_2(20) + CH_2F_2(5)$	0	15 W	4 Pas	35s

Dielectric

ALD

Oxyde	Precursor	Temperature	Thickness	Pre-treatment
Al_2O_3	O_2 plasma	280C	10nm	10min, O_2 plasma

Gates

Electron-beam masker, first layer

Resist	Dose	Developper
PMMA 2%	1200, 1400 $\mu C/cm^2$	MIBK:IPA[1:3] (45s) + IPA (45s)

EBM

Metal	Thickness (nm)	Rates (nm/s)
Ti:Pt	3:32	0.5:0.5

Electron-beam masker, second layer

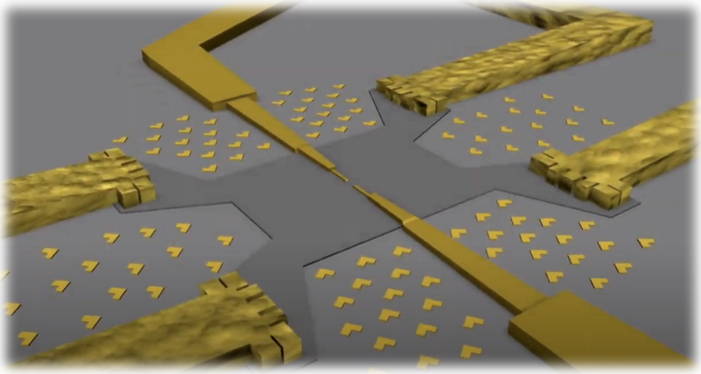
Resist	Dose	Developper
PMMA 2%	1200 $\mu C/cm^2$	MIBK:IPA[1:3] (45s) + IPA (45s)

EBM

Metal	Thickness (nm)	Rates (nm/s)
Ti:Pt	3:32	0.5:0.5

Chapter 3

QPC and H-FET mesoscopic transport characterization



We will explore in this chapter the viability of the Ge/SiGe heterostructure, as well as the fabrication recipe from chapter 2, to form quantum dots. We will start by measuring Hole Field Effect Transistor (H-FET). From this experiment we can extract the conduction pinch-off voltage and calculate the 2DHG sheet resistance. After that, we will discuss on some fabrication improvement and hysteresis effect due to surface charge tunneling. The first section will finish with the extraction of the 2DHG mobility. The second part of the chapter will focus on Quantum Point Contact (QPC) and their transport characterization. Single and double gate layer devices have been tested. The chapter will finish with the nonlinear transport measurement of a QPC under bias voltage.

Image taken from the *YouTube* video "QPC quantization". Boris Brun-Barriere.

3.1 Set-up

All the measurements in this chapter where performed in a home-made 4K stick. It consists in a PCB holder at the end on a metallic stick shield with a vacuum cane. There are 24 direct current lines (DC) down to the PCB. Everything is introduced in a liquified He^4 bottle. With this set-up, we were able to measure at 4.2 K. The advantage of this measurement system is the low time required to have a sample at base temperature. In less than two hours we were able to measure a new device.

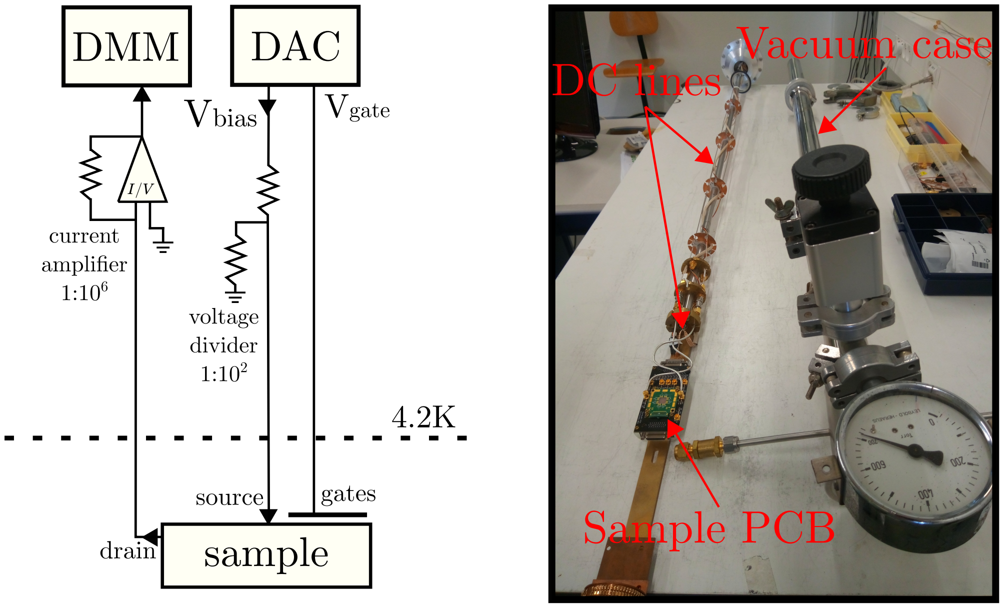


Figure 3.1: Schematic and picture of the 4K stick set-up. There is a voltage divider for the input voltage bias and a I/V converted in the output line. The vacuum case is sealed around the 4K-Stick. With a rotatory and a turbo pump, we achieve a vacuum of $< 10^{-4}$mBar. Then, we introduce a small quantity of He in the cane to provide heat exchange between the PCB and the liquid He from the bottle.

During this chapter, we used three different technique to measure the H-FET and the QPC. We measured in direct current from source to drain, in two-point contact circuit and in four-point contact circuit. For gating the device, we used a DAC (Digital Analog Converter) featuring 24 low noise DC sources with 16 bits on ±2V or 8 V. Along the source-drain DC line there is a voltage divider of 10^{-2}V/V for the DC bias and 10^{-4}V/V for the low-frequency lock-in bias. In the detector chain there is an I/V-converter. We had a Digital Multimeter (DMM)

Delft IVVI-Rack

Agilent 34401A

to measure the current amplitude. We also counted with a Lock-In to measure low-frequency differential conductance (77.66Hz) with an amplitude of 50μV. In figure 3.1 we can see a schematic of the circuit line and a picture of the 4kStick in the laboratory.

3.2 Field effect

The first quantum device we measured was a H-FET. The transport results demonstrate our ability to control the 2DHG density with an electrostatic field. This requisite is fundamental to form quantum dots in semiconductors.

The H-FET devices consist in a mesa, a top metallic gate and a total of six ohmic contacts to the quantum well. In figure 3.2 a) there is an optical image of the sample, and in figure 3.2 b), there is a transversal cut along the dashed line. The depleting (or accumulating) voltage is applied at the top gate. For a direct contact or a two-point measurement, we will only use two out of the six ohmic contacts. In the four-point measurement, four contacts will be used. The picture shown in figure 3.2 a) has a NbN top gate, but along the chapter we used Ti:Pt gates. The devices are essentially the same, a single top gate covering four or six ohmic contacts.

3.2.1 Pinch-off voltage

We understand as pinch-off, or threshold voltage, the voltage value that turns on the H-FET. This phenomenon was described in the theory section 1.2.1. We observe current through the sample when a conduction channel is formed in the 2DHG between two ohmic contacts.

We fabricated several H-FET devices, all with the same fabrication process. Results for three samples can be seen in figure 3.3. We observe a hysteresis in the sample's pinch-off voltage which depends on the top gate voltage sweep direction. We assume this hysteresis of few tens of mV comes from the charging traps in the different dielectric interfaces [100, 101]. Charge traps in the dielectric interfaces are filled by charge tunneling from the quantum well. A positive voltage in the gate induces the filling of the negative charges. The negative charges at the dielectric interfaces induce an effective field on the quantum well which displaces the effective gate voltage. That is why hysteresis is always in the same direction.

It is also clear that for each device, the threshold voltage varies. Each sample is located in a different place on the wafer surface. Local variations in defect densities can produce a non-homogeneous disorder potential influencing the pinch-off voltage. Small changes in the gate work function would also affect the threshold voltage. What all samples have in common is the positive pinch-off voltage, from $V_g = 1.2$V up to $V_g = 1.35$V. Theoretically, the undoped Ge/SiGe strained quantum well should not have carriers at zero field [102, 103]. From the Ti:Pt work-

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HF2L, Zurich instruments

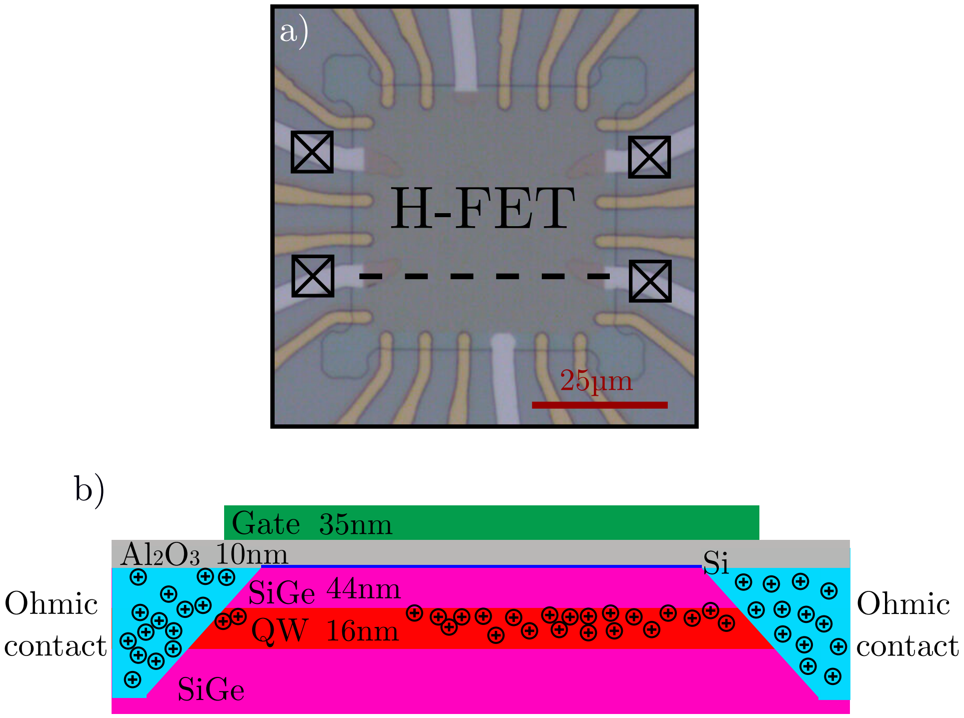


Figure 3.2: a) optical image of the sample used to measure field effect and hole mobility. b) is a transversal schematic view along the dashed line. We observe the different layer stack and a representation of the holes in the heterostructure (the circle with a plus symbol).

function ($\Phi_{\mathrm{Ti}} \sim 4.3$eV) and the Ge electron affinity ($\chi_{\mathrm{Ge}} \sim 4$eV), we can estimate the gate voltage necessary to push the semiconductor valence band over the Fermi level. Ge gap is ~ 0.7eV, so the Ti Fermi level falls more-less in the middle of the gap. There are around ~ 0.35eV energy difference. With the top gate, we would need to this energy difference to accumulate holes, around $V_g \sim -0.35$V. We can see how far the samples measured are from this estimation. We conclude that there should be a charged layer somewhere in the heterostructure that effectively populate the quantum well. In figure 3.4 there are two schematic representation of the band alignment with a top metallic gate. In case a), the top gate bends the valence band but not enough to overpass the Fermi level; there are not any hole in the quantum well. For case b), there is an extra charged region between top gate and quantum well. The electric potential caused by this charged layer bends the band structure, and at the quantum well they overcome the Fermi level. This induces hole's accumulation.

We believe from the experiments that the system is in the case b) of figure 3.4. Is therefore necessary to apply a gate depletion potential (positive voltage, because carriers are holes) to close conductance from source to drain. The quantum well was feed with carriers at zero gate voltage. It is not the first time this phenomenon

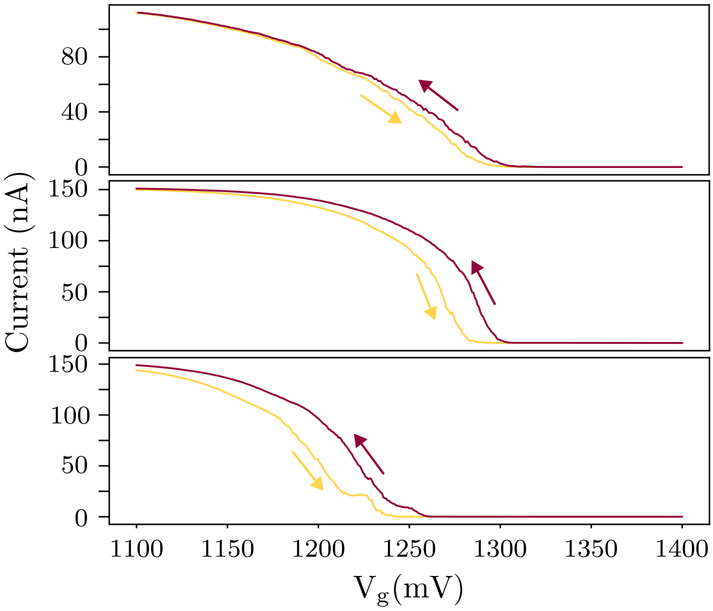


Figure 3.3: Three source-drain current versus gate voltage for three different H-FET devices. Bias voltage is $V_{bias} = 1mV$. Yellow plot is ramping up the voltage and maroon plot is ramping down. We observe some differences in the pinch-off voltage of ±150mV, and also hysteresis in the field effect of ±15mV.

is observed, oxide interfaces are well known to from dislocations that bond carriers into charge traps [101, 104, 105]. If the trap density is high enough, its electrostatic potential could act as a virtual gate which accumulate holes in the quantum well. Another possibility is that charges are being trapped at the CMP surface in the heterostructure growth. But this scenario was discarded after testing other heterostructures with different cap buffer thickness. We observed a correlation between the SiGe thickness above the quantum well and the pinch-off voltage, but the CMP layer is at the same distance for all samples. The hypothetical influence of the CMP layer should not change from sample to sample. Even more, we observed than the pinch-off voltage for the thinner cap buffer layers needed to be stronger. These results made us believe that the charged layer should be above the quantum well.

3.2.2 Dielectric charged interface

To test which interface was acting as a gate, we made samples that where measured after each step in the fabrication process. We tested a sample with a top gate, another one just after the ALD and a third one after the mesa etching.

In figure 3.5 a) we see a H-FET curve. The threshold voltage is around

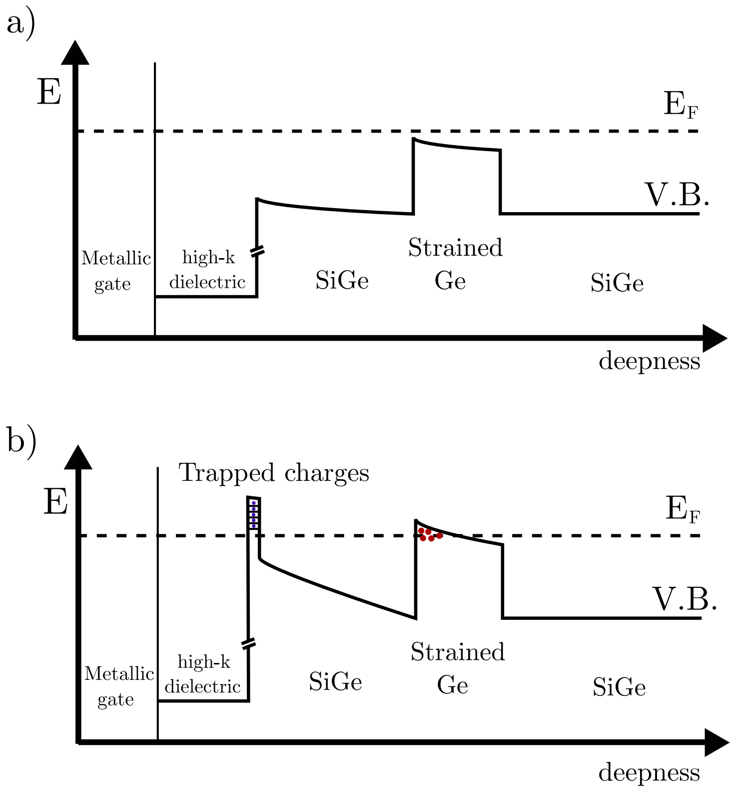


Figure 3.4: Two schematics of the band structure of the SiGe heterostructure. In case a), there is a small bending produced by the metallic top gate, but the bending is not large enough to accumulate holes in the quantum well. In case b), there is an extra layer of charged traps that act as a virtual gate. The bending produced by the trapped charges is large enough to accumulate holes at the quantum well. Holes are represented as red circles.

$V_g = 1.3$V. At the right of the plot there are two schematics representing the 2DHG density for both gate states. In the top image, the gate voltage is not large enough to deplete the hole gas and there are still carriers in the quantum well. In the bottom schematic, the gate voltage is large enough to electrostatically empty the quantum well. The samples stopped during the fabrication process are in figure 3.5 b) (ALD) and figure 3.5 c) (MESA). Sample named ALD is measured after the ALD step and sample named MESA is measured after the mesa etch. In figure 3.5 d) we see the transport results for those two samples. We observe that the resistance for both cases is purely ohmic. This means that there are holes in the quantum well for both cases, even without an accumulating gate.

From this experiment, we can estimate the sheet resistance of the 2DHG using that $\rho_{2D} = L/wR$ where L is the distance between ohmic contacts and w is the width of the contacts. For ALD and MESA sample, resistance is extracted directly from the slope of the plot, it is $3\,\mathrm{k\Omega}$, after removing the line resistance ($1\,\mathrm{k\Omega}$) and the PCB lumped resistances ($4\,\mathrm{k\Omega}$). A broad estimation of the resistivity

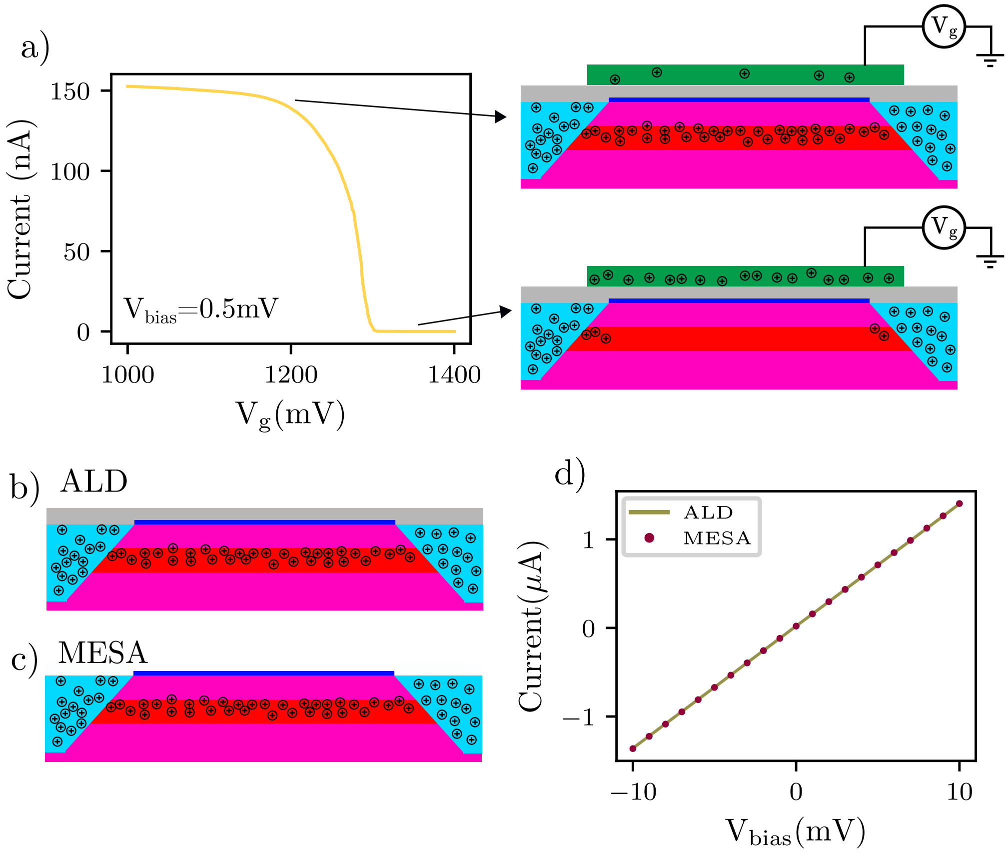


Figure 3.5: Results for the accumulation threshold voltage for three sample at three different stage in the fabrication process. Plot a) represent the source-drain curve vs top gate voltage of a sample with a H-FET. Next to it there are two schematic showing the hole gas density for the two top gate voltage values. In b) and c) there two schematic of two sample done until the MESA step and the ALD. d) is a plot of current vs bias voltage for the two samples in the schematic of b) and c). We can see the ohmic response of the current, which indicates the presence of carriers in the quantum well.

give a value of $\rho_{2D} = 150\Omega_\square$. In the sample with the top gate, the differential conductance was obtained with four-point circuit, which directly gives then 2DHG resistance. In saturation, $R = 3.3\text{k}\Omega$. The estimated sheet resistance is $\rho_{2D} = 165\Omega_\square$. There is around 9% difference with respect to the other samples. The difference may be related to the 2DHG density or to a difference in the ohmic contacts' resistance.

With data from figure 3.5, we conclude that the interface that is acting as a gate is not related to our fabrication development. The only interface left to test was the SiGe/Si cap layer, but we also think there may be a second interface. As the Si cap layer naturally oxidize to SiO_2, there is a possibility that it didn't fully oxidize, and Si/SiO_2 interface is formed. We will study this scenario in the next section.

3.2.3 Si oxidation with oxygen plasma

Following the assumption of the Si/SiO_2 interface, we found two possible ways to solve it. One possibility would be removing the Si and the SiO_2 layers with wet-etching of HF [47]. But this process raised two problems for us. The first is that we had to use HF, and in our research center we don't have easy access to it. Second, the complete removal of the Si cap layer would expose the SiGe beneath, and this layer will oxidize itself again. Then, we would have to deal again with some semiconductor-oxide interface. The other solution we thought was to fully oxidize the Si and create a $SiGe/SiO_2$ interface. We found in bibliography that it was possible to use oxygen plasma to oxidize several nm of Si [106–108]. We tried to replicate this process in the ICP with a strong O_2 plasma. The recipe used was 1000 W of ICP at 1Pa with an oxygen flux of 50 sccm. This was done over 1 min. This step was performed just after the mesa etching and before the ALD. A schematic of the sample surface before and after the plasma is pictured in figure 3.6.

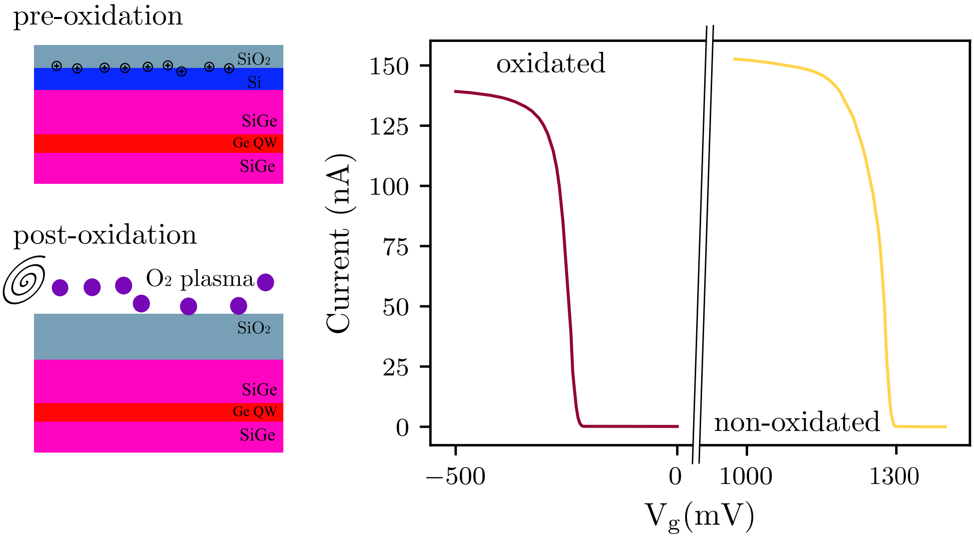


Figure 3.6: At the left, two schematics of the surface oxidation process with the ICP plasma. At the right, current versus gate voltage for two H-FET devices. Bias voltage in both experiment was $V_{bias} = 0.5mV$. The red curve is data from an oxidized device and yellow correspond to a non-oxidized one. For non-oxidize H-FET, the threshold is $V_g = 1.3V$ while for the oxidize sample is $V_g = -0.3V$

To test the results of the experiment, we measured again the threshold voltage of the oxidized sample. Results can be seen in figure 3.6. There is a clear difference in pinch-off voltage for oxidized and non-oxidized samples, it drifted towards negative values more than 1V. We assume this displacement is due to the elimination of charge traps in the Si or in the Si/SiO$_2$ interface. Now, all the Si layer is fully oxidize. In principle, it may look like this result is not relevant, it just moved the threshold voltage, but we found it to be of a great importance. Applying less gate voltage means less risk for leaks in the dielectric. Also, it improves the sample hysteresis, this will be discussed in the next section. In conclusion, after these results, we decided to apply this fabrication step to all future samples.

3.2.4 Field effect drift

Our scenario is that the sample hysteresis comes from the surface trap charging, as it was commented before. A schematic representation of the tunneling effect is in figure 3.7 a). There is another consequence for the surface trap tunneling. The more electric potential is applied to the gate, the more charges tunnel to the surface states [68, 100]. The trap states have a slow dynamics, which means that once a trap is charged, it will take long time to decay. This is translated in a constant compensation from the top gate to overcome the effect of the virtual gate. This effect is known as voltage drift or field effect drift.

Results for the voltage drift experiment are in figure 3.7 b). We see current versus gate voltage in four different plots. The current was measured chronologically from top to bottom. In the first plot, voltage start from zero and is swept until $\mathrm{V_g} = -500\mathrm{mV}$. The pinch-off voltage is $\mathrm{V_g} = -200\mathrm{mV}$. We wait 3 min at $\mathrm{V_g} = -500\mathrm{mV}$, then the gate is swept again to zero. We observe how both traces (ramping up the gate voltage and ramping down) are almost equal. In this case, hysteresis is negligible. In the second plot, gate voltage is swept from 0 to $\mathrm{V_g} = -1000\mathrm{mV}$, stopped during 3 min, and swept again to 0. Now we can observe a strong hysteresis. When decreasing the voltage, the H-FET opens at the same point as the previous plot, $\mathrm{V_g} = -200\mathrm{mV}$, but coming back to zero, it closes at $\mathrm{V_g} = -600\mathrm{mV}$. This difference comes from the accumulation of charges at the surface states. The gate has to compensate the effect of those charges. The same pattern is replicated for the other two plots. In figure 3.7 c) all the returning to zero curves are plotted together. The increment in gate voltage for each plot was $\Delta\mathrm{V} = 500\mathrm{mV}$, and the voltage drift for each plot is equally spaced by 400 mV.

The field effect drift could be a problem for the quantum devices' stability. The more voltage is applied to the gate, the more charges tunnel. There are two ways to "reset" the sample. Warming up until the SiGe becomes conductive or applying positive potential to the gate for long time. Warming up works great for this purpose, samples were always coming back to its original threshold values. The technique of positive potential was not as effective. We observed some drift towards less negative pinch-off values, but after waiting several hours.

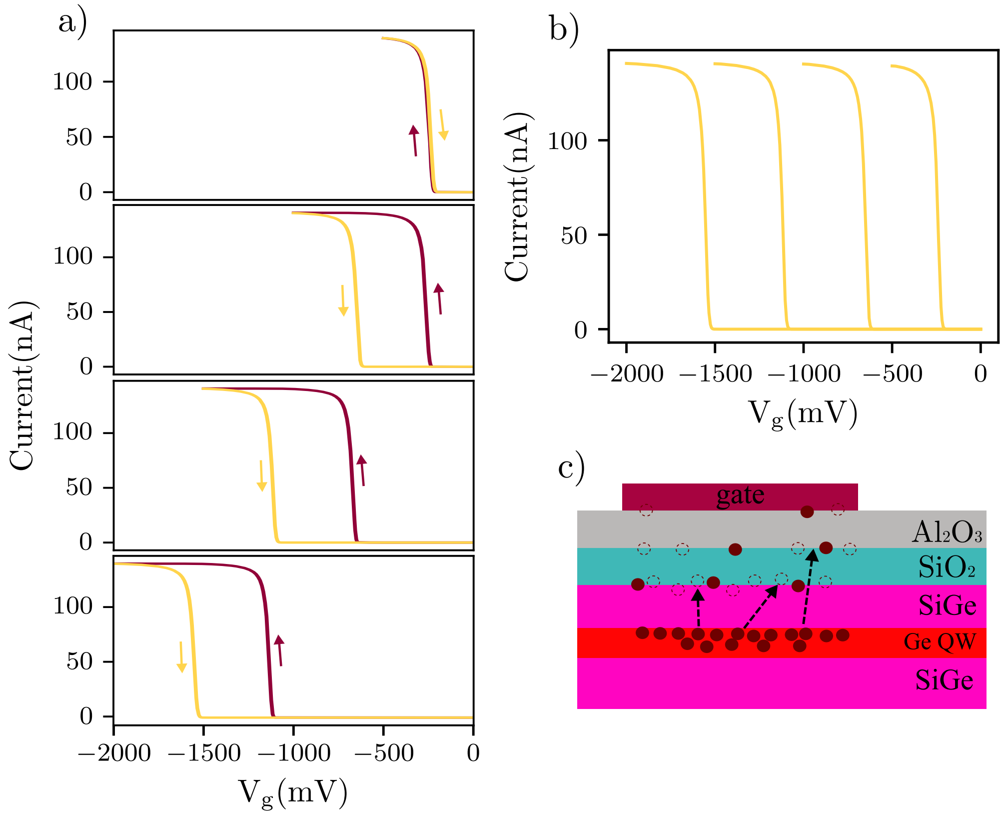


Figure 3.7: a) H-FET plots showing current vs gate voltage. Bias voltage was $V_{\text{bias}} = 0.5\text{mV}$ for all plots. They are chronologically arranged from top to bottom. We can observe in the threshold voltage drift that surface states are being filled by carriers from the quantum well [100]. b) shows the current plot for gate sweep towards zero voltage. c) is a schematic of the carrier tunneling to the surface states. These charges act as a virtual gate and screen the effect of the metallic top gate. The slow dynamic for the traps discharge makes the voltage drift a one-way effect.

3.2.5 Mobility measurements

Usually, mobility is extracted measuring the Quantum Hall effect [102, 109]. But to observe this phenomenon a magnetic field is needed. The set-up we used was not equipped with a magnet, so we had to apply some approximations to estimate the mobility. We have the chance to be able to compare our estimation with Hall-bar measurement data. Those experiments were carrying on by another PhD in the laboratory, Elyjah Kiyooka.

The approximation we will use is consider the H-FET and the 2DHG as a parallel capacitor. This scenario works well when the system is far from saturation (close to the pinch-off voltage) [100]. From a perfect plate capacitor, we take the equation from the theory section 1.20. The system permittivity is given by the dielectric constant of the materials between the metallic gate and the quantum well. To calculate it we have to take into account the three materials: SiO_2, Al_2O_3 and SiGe. Considering three capacitors in series, the effective dielectric constant, with data from [110, 111], is $\epsilon_{\text{eff}} \approx 11.9$. Another way to extract the effective dielectric constant is by fitting Hall-bar measurement to a linear function. In figure 3.8 we can see the density measured with Hall-bar and the fit to equation 1.20. We can observe how both values match.

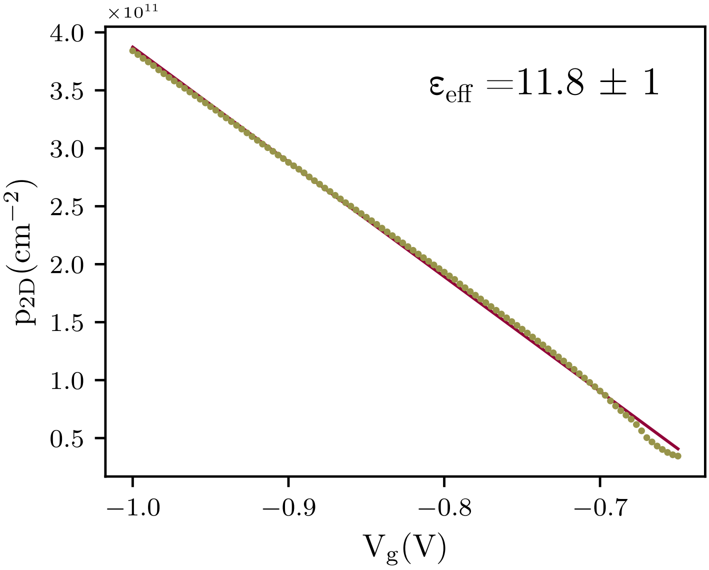


Figure 3.8: Density versus top gate voltage in a Hall-bar device. The solid line is a fit to a linear function from which we can extract the ϵ_{eff}.

From the Drude model, we know that the mobility of a two-dimensional carrier gas is expressed as

$$\mu = \frac{\sigma}{p_{2\text{D}}|e|}, \tag{3.1}$$

where σ is 2DHG conductance, $p_{2\text{D}}$ is the hole density in two-dimensions and $|e|$ is the electron charge. The current flowing through the sample is directly related to the conductance $I = \sigma V_{\text{bias}}$. We observe from the experiment, that conductance and current vary with respect to the gate voltage. This is due to field effect and the carrier density modulation. If we differentiate the current with respect to the gate voltage we get that

$$\frac{dI}{dV_g} = \frac{d\sigma}{dV_g} V_{\text{bias}}. \tag{3.2}$$

We can take the differential equations for the mobility and the hole density in a parallel plate capacitor

$$dp_{2\mathrm{D}} = \frac{\epsilon_0 \epsilon_{\mathrm{eff}}}{d|e|} dV_g,\ \mu = \frac{1}{|e|} \frac{d\sigma}{dp_{2D}}. \tag{3.3}$$

After some algebra, we arrive to the differential equation

$$\mu = \frac{tV_{\mathrm{bias}}}{\epsilon_0 \epsilon_{\mathrm{eff}}} \frac{dI}{dV_g}. \tag{3.4}$$

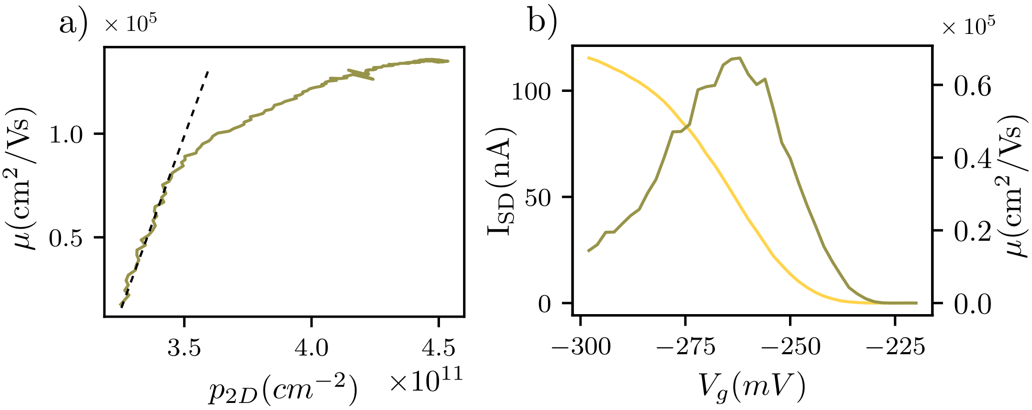


Figure 3.9: a) mobility versus hole density measured with Hall bars and quantum Hall effect. This experiment gives the exact density for every gate voltage. b) current plot and mobility estimation versus gate voltage. The mobility here was extracting by a parallel plate capacitor model. We can only trust the right half of the peak, where the system behaves as a capacitor. After the peak, the mobility decrease, which is an artifact of the model. The maximum mobility from this method is $65\,000\,\mathrm{cm}^2/\mathrm{V}$

We can differentiate the curve for the H-FET and find the mobility for each gate voltage. This is done in figure 3.9 b), green line. The yellow plot is the current versus gate voltage. For the mobility, we can see that there is a peak at $V_g = -260$mV, and then it decreases. The reduction in mobility is an artifact from the capacitor model we have used. In reality, the mobility doesn't decrease. We can trust the results in the first half of the peak and in its maximum, which corresponds to the maximum slope in the H-FET plot. The maximum mobility we find is $\mu = 65000\mathrm{cm}^2/\mathrm{Vs}$. In figure 3.9 a) we have the plot of mobility versus hole density measured with Hall bars. With this technique, we can extract the 2DHG density at every top gate voltage. This measurement is much more accurate. We see that the beginning of the mobility plot is a linear function, and eventually it flattens. The beginning of the curve correspond to the system behaving as a parallel capacitor (dashed line); there is a linear response of the carrier density with the gate voltage. In the plot b), this corresponds to the right side of the mobility peak. We can observe that this region ends with a maximum mobility of

80 000 cm^2/V. There is a 20% difference with respect to the parallel plate model. Once the system overcome the first region, it begins to flatten because of the surface trap tunneling [68, 100]. The maximum mobility measured in our devices was 135 000 cm^2/V. For quantum dots, the region we are most interested in is the beginning of the curve, when the system just start to accumulate carriers.

If we take a look into the bibliography, the best hole mobility in Ge/SiGe heterostructure is for A. Dobbie et al. [31] for a value over 1 000 000 cm^2/Vs. Their heterostructure was doped with B ions and the quantum well had a deepness of 70 nm. In undoped heterostructure, measurement in A. Sammak et al. [102] found values between 40000 and 500 000 cm^2/Vs. We don't reach values as high as the state-of-the-art, but our maximum mobility is at the same order of magnitude. We can claim that our heterostructure is good enough to host quantum dots, and eventually, hole spin qubits.

3.3 QPC

The construction of QPC is the next step we did to test the mesoscopic proprieties of our heterostructures. With a QPC we locally control the carrier density of states and measure quantum transport.

QPC devices consist in depositing two metallic gates face to face. We tested different gate width and gap length between gates. Since our objective is a proof of concept gate shapes are rectangular. In previous chapter 2 we can see a SEM image of a QPC in figure 2.14 a). We have to mention that these measurements were done before the discovery of the O_2 plasma treatment to oxidize the SiO_2. That is the reason why all voltage gates are strongly positive and there is a 2DHG without a top gate.

In total, we measured three different gap length (40, 60, 80 nm) with six gate lengths each (70, 110, 150, 180, 210, 230 nm). We did this for the two fabrication development; single gate layer and double gate layer. For simplicity, we will only show the more interesting results. All samples shown have a gap length of 40 nm.

3.3.1 Single gate layer QPC

The first generation of QPC we did were with Ti:Pt gates and in a single layer lithography. In figure 3.10 a) we have a sample SEM image. For each QPC there are two gates face to face. The differential conductance was measured in two-point contact configuration. Figure 3.10 b), c) and d) are the transport results for different length QPC. The inset figure is a SEM picture of the device. What we expect to see are quantum transport plateaus according to Landauer equation 1.23.

We can observe conductance plateaus in figure 3.10 b) (233 nm width) and in figure 3.10 d) (78 nm width). These plateaus are broad by temperature (the measurements were taken at 4.2K) and by the system's geometry [70]. For the QPC c), the conductance is more similar to a H-FET. If we look to the SEM image

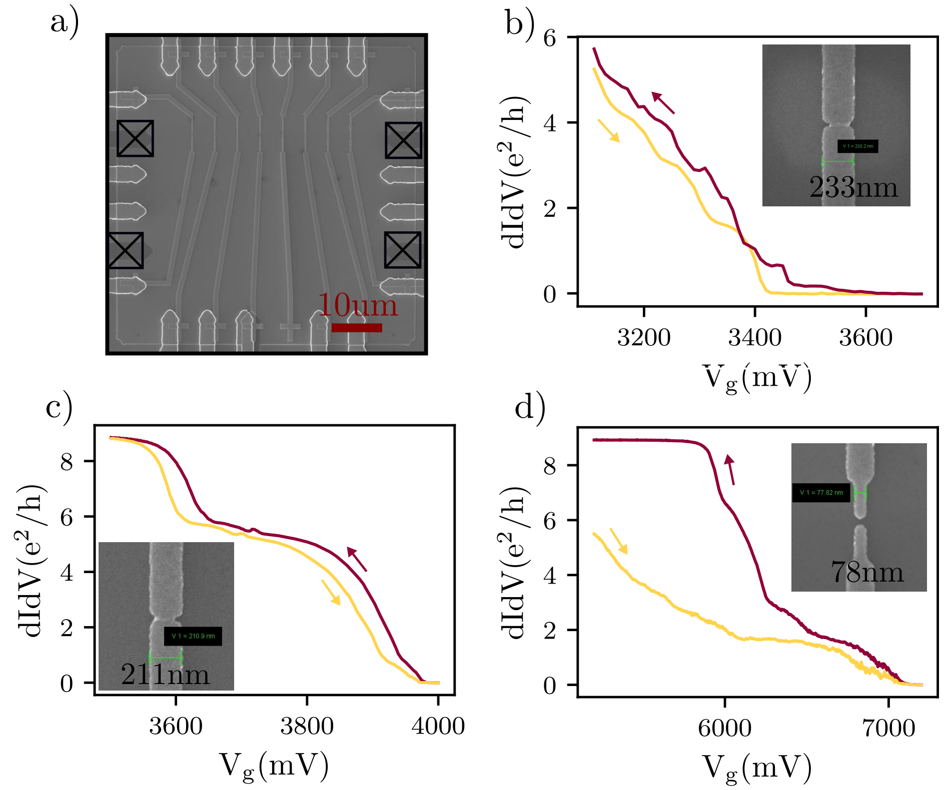


Figure 3.10: Results for the sample of single layer QPC. The heterostructure had carriers at zero bias, so there was not needed an accumulation gate. a) shows a SEM image of the device. Each QPC has two metallic gates. In total there are four ohmic contact, but only two were used, the measurement was taken with two-point contact. b), c) and d) are the conductance versus gate voltage with the corrected conductance value. The line resistance were removed from the data. The QPC gates had lengths of 233, 213 and 77 nm. The inset image is a SEM picture of each QPC. We can distinguish plateaus in the plot b) and another plateau in plot d). For c), the sample behaves as a H-FET.

of b), it looks like the gap is totally metalized, but the fact that we observe very clear plateaus means that there is a quantum transport channel. We believe that there is some resist left-over in the gap, and the metal has been deposited above it. The gate forms a bridge which allows conductance beneath it. Opposite, the curve in c) indicates a gate like a H-FET device. Finally, for d) we can distinguish one big plateau with some noise. The voltage needed to apply to this QPC is $V_g = 7V$, 3V larger than for the other devices. Our scenario is that, with a constant trapped charge density at the dielectric, there is a screening effect proportional to the surface inside the QPC. The wider the gates are, the less potential we need to apply to overcome the trap density. To support this idea we have the data of the QPC with larger gaps (60, 80 nm). In those devices, the pinch-off QPC voltage was never reached, it fell above $V_g > 8$V. In those cases, the constant trapped charge density increases the trapped charged because the gap is bigger. This forces the QPC gates to apply a larger voltage to pinch-off. Eventually, at higher enough voltage the QPC would be closed.

The better conductance plateaus were observed in the QPC which formed a bridge. Essentially, this is an extra gate layer over the QPC transport channel. From this result we decided to build devices with a second gate layer. The top gate will be used to reduce the 2DHG density around the QPC, and, at the same time, the voltage applied to the QPC gates would decrease. This reduces the risk of leaking.

3.3.2 Double gate layer QPC

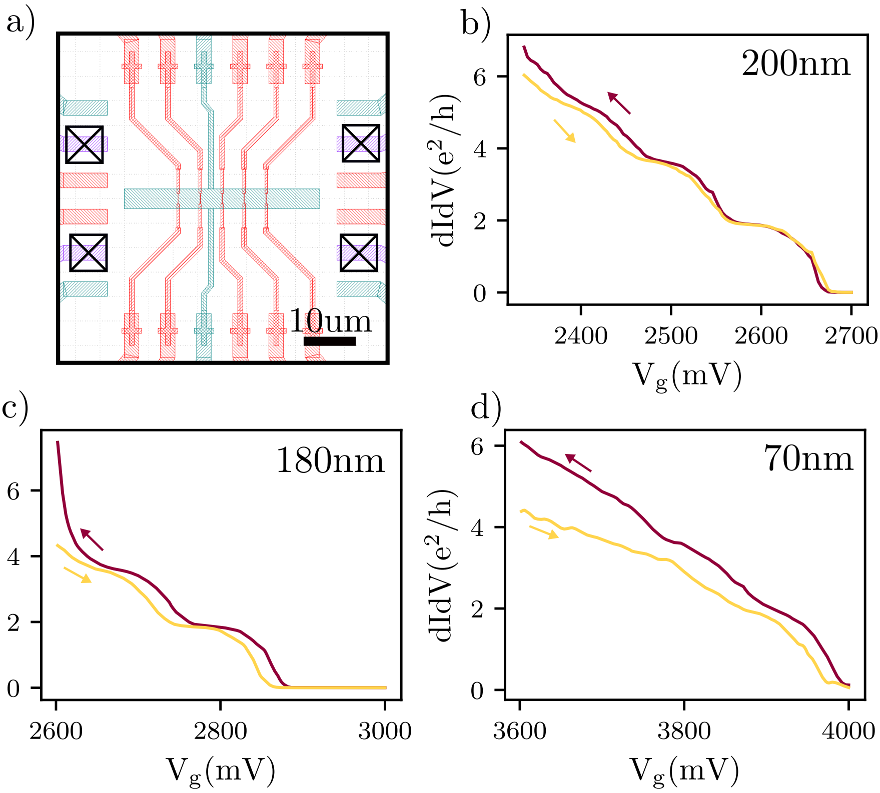


Figure 3.11: Results for the double gate layer QPC sample. a) schematic of the sample. Red are first gate layer and green second gate layer. This sample was measured in four-point contact. Lengths are 200, 180 and 70 nm for plots b), c) and d). Top gate layer was at 3 V. We can now distinguish more plateaus for all the samples.

In the double layer QPC devices, we used a four-point circuit to extract the differential conductance. In figure 3.11 we have the results. Picture a) shows an image from a digital software of the sample. Green structures are a second gate layer that overlaps the QPC's, done in the first gate layer. In plots b), c) and d) we observe the conductance vs gate voltages for QPC of lengths 200, 180 and 70 nm respectively. The top gate was at $V_{TOP} = 3V$ for all the measurements. We can already observe that there are plateaus for all the devices. Even in d), with 70 nm, we can distinguish the two first plateaus at $2\,e^2/h$ and $4\,e^2/h$. If we compare with the previous sample of single layer, we conclude that lowering the overall hole density helps to define the quantum transport channel.

3.3.3 Comparison between double and single gate layer

The other big difference between double and single gate layer devices is the pinch-off voltage. In figure 3.12 we see the six conductance measurement in one graph. Yellow plot are single gate layer devices and maroon plot are double gate layer. The trend for threshold voltage from single to double layer is towards smaller values. For the 70 nm length, the sweep is 3.2 V.

In conclusion, we have improved in two ways the device response by adding a second gate layer. First, the threshold voltage is shifted to lower voltages, which helps to avoid leaks through the dielectric. Second, the devices shows better conductance plateaus, certainly due to less charge disorder above the QPC channel.

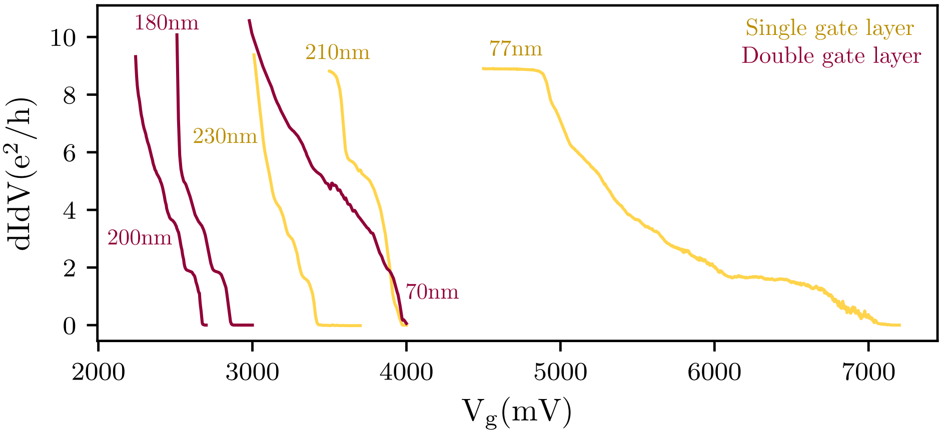


Figure 3.12: All the conductance plots for double (maroon) and single (yellow) gate layer in the same graph. Here we can appreciate the threshold voltage drift for the double gate layer.

3.3.4 Nonlinear quantum conductance in a QPC

The last experiment we performed with the QPC was exploring the nonlinear conductance. This effect raises when a voltage bias is applied to the conductance channel. In figure 3.13 we can see some bibliography examples of this phenomenon. When a bias voltage is applied to a QPC, we find regions where conductance is not a multiple of the quantum of conductance. In the early 90's people started to develop a theory framework around this effect. Here we will present a taste of the theoretical derivation.

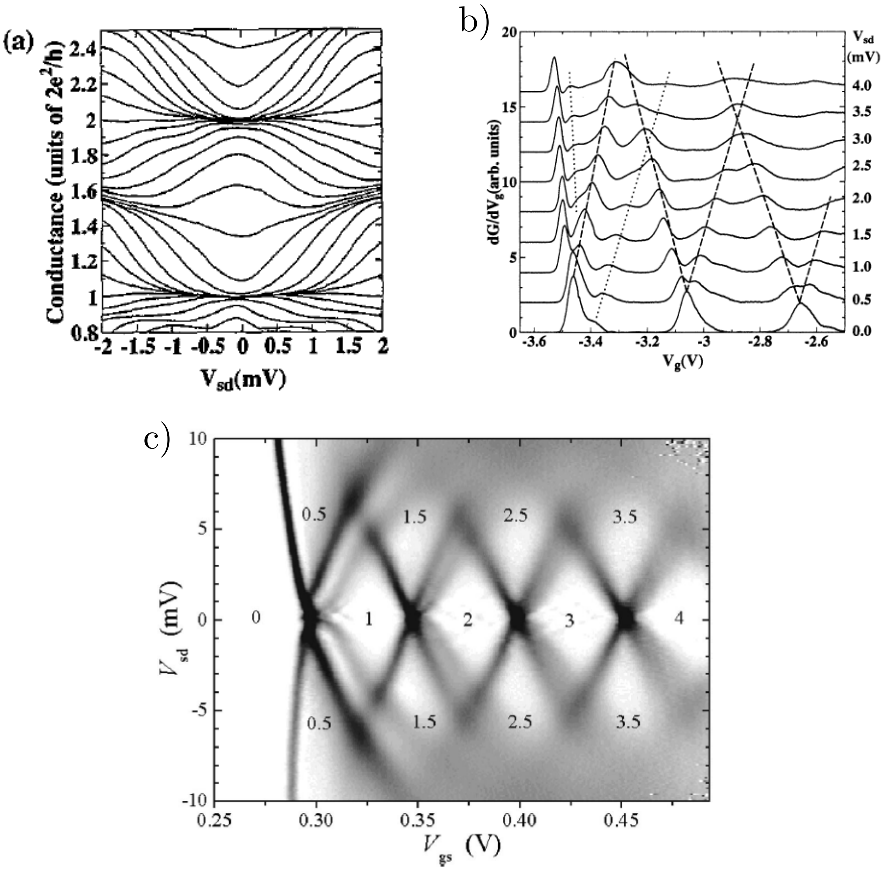


Figure 3.13: Literature examples of non-linear transport in a QPC. a) is taken from [112], b) from [113] and c) from [114]. The three devices presented consisted in GaAsAl/GaAs two-dimensional quantum well. In all the plots we can observe the half integer conductance plateaus that rise from the non-linear transport. The color plot in c) shows the transconductance, defined as dG/dV_g.

If we situated ourselves in the QPC reference frame, the system source (μ_s) and drain (μ_d) chemical potential when there is a voltage bias applied are

$$\mu_s = E_F + \beta e V_{\text{bias}} \quad \text{and} \quad \mu_d = E_F + (1-\beta) e V_{\text{sd}}, \tag{3.5}$$

where E_F is the Fermi energy, e the electron charge and β is a coefficient between 0 and 1 that define how much of the bias potential drops in the 2DHG before the constriction. The transport subbands spacing is given by the QPC lateral gates. If a voltage bias is applied, it is possible to force the chemical potential of source or drain to overcome an upper QPC subband. In this scenario, the forward and backward direction don't align with the same number of QPC subbands. According to GK theory [115] and to [112], conductance through the QPC in this case can be written as

$$G = \frac{2e^2}{h}[\beta N_+ + (1-\beta)N_-], \tag{3.6}$$

where N_+ are the subbands below the Fermi level in the forward direction and N_- in the backwards one. Equation 3.6 is pertinent in the ballistic transport and when the QPC potential is adiabatic. We can define the subband difference as $N = N_+ - N_-$ and rewrite the conductance in the nonlinear regime as

$$G = (N-\beta)\frac{2e^2}{h}. \tag{3.7}$$

In our devices, to observe this effect we used the device 200 nm double gate layer. It was measured in a four-point contact circuit while a bias voltage was applied to source. Results are in figure 3.14. In plot a), we see the direct conductance measurement of gate voltage vs bias voltage. In b) the gate transconductance is plotted.

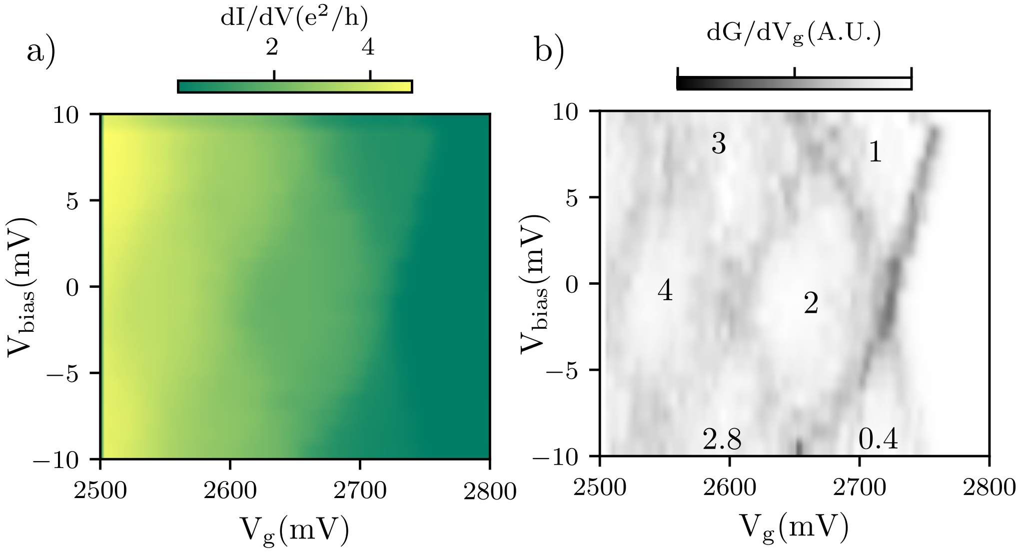


Figure 3.14: Color plot showing the QPC behavior under voltage bias. a) shows the system conductance varying V_g vs V_{bias}. We observe a diamond-shape structures due to the self-gate effect and the half integer conductance of the QPC. b) shows the transconductance from color-plot a). We observe again the diamond-shape structures and the number represent the unities of e^2/h for each diamond.

In both plots we observe diamond shaped structures. Each of the diamond correspond to a different conductance values. At zero bias, conductance plateaus appears at the known values; $2e^2/h$, $4e^2/h$, etc... But when the system enters the nonlinear regime, we observe how the conductance starts to have odd number of the quantum conductance, e^2/h and $3e^2/h$ for positive bias and $0.4e^2/h$ and $2.8e^2/h$ for negative bias. The difference is produced because the factor β is different for each polarity. When reversing the bias, the current is affected by the sheet resistance of the 2DHG, which depends on the distance from the device to the source. Since the QPC is not in the center of the sample (see figure 3.11 a)), the resistance is different.

From figure 3.14 b) we can extract the subband level spacing. It is given by the half height of the diamond and correspond to 9 meV. If we compare the subband energy with the temperature $T = 4.2\text{K} \rightarrow 300\mu\text{eV}$, we see we are in the order where temperature is 30 times smaller. This means that the broadening in the QPC plateaus comes mainly from the curvature of the parabolic potential. We can estimate the QPC channel width using the subband level spacing. With equation 1.29, distance of $l_0 \sim 20\text{nm}$ is obtained for an effective hole mass of 0.08m_e, and $l_0 \sim 10\text{nm}$ for an effective hole mass of 0.02m_e. These two magnitudes are in the order of what we could expect. The channel width at the device surface is $\sim 40\text{nm}$, so a reduction of up to 75% at the quantum well is not surprising.

3.4 Conclusions

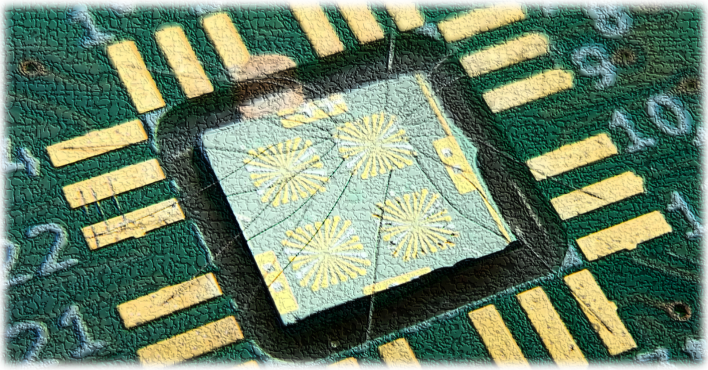
Along this chapter, we have studied some electrical proprieties of the SiGe heterostructures. Our objective was to estimate the viability of the samples to host quantum dots. All the experiments were measured in a 4K-Stick at 4.2 K.

We have done some field effect experiment and found that the pinch-off voltage was too positive for what we would expect. We conclude that the cause was a virtual gate of charges trapped in the Si/SiO_2 interface. After that, we improved the fabrication recipe by adding an extra O_2 plasma step. Then, the surface trap tunneling was studied. The first part is finished by the estimation of the field effect mobility, 65 000 cm^2/V, only 9% off from the values obtained with Hall bars: 80 000 cm^2/V. In the second part of the chapter, we focused on quantum transport and QPC devices characterization. We tested single and double gate layer devices and found that double gate layer structure gave a better quantum transport results. Several conductance plateaus were measured for different devices. We found that a second gate layer helps to reduce the overall electric potential that we need to apply to the gates for depleting the hole gas. The last experiment performed was the nonlinear response of the system under a voltage bias. We studied the half integer conductance of the QPC. We could also extract the subband level spacing of the QPC levels, which is 9 meV. The estimated channel width according to the parabolic potential is $\sim 20\text{nm}$ and $\sim 10\text{nm}$ for effective masses of 0.08m_e and 0.02m_e. The two values are smaller than the device width at the surface, 40nm, but inside what we could expect.

In conclusion, all the characterization and experiments performed in the heterostructure open the way to develop quantum dots. We are able to control the 2DHG density and achieve quantum transport. The next step, and the next chapter, is the quantum dot characterization.

Chapter 4

Single Quantum dot



In this chapter, we present the preparation of a single quantum dot (SQD) into the Coulomb blockade regime and the measurements to characterize its quantum transport features. The purpose of this experiment is to qualitatively estimate the fabrication method viability to host a hole spin qubit in the gate design produced in 2. The chapter starts with the sample and set-up description, followed by the technique used to tune the device in the Coulomb blockade regime. The second part focuses on the coupling optimization of the tunnel barriers to enhance Coulomb peak visibility. This regime is achieved when both barriers have similar tunnel rates $\Gamma_R \approx \Gamma_L$. In the next section, we present the extraction method of the charging energy ($\mathrm{E_C}$) and the lever arm (α) from Coulomb diamonds. At the end of this chapter, we focus on measurements used to extract the hole Landé g-factor as well as charge noise characterization.

PCB after bonding a SQD sample.

4.1 Device description

The presented SQD is thought to be measured in transport. Figure 4.1 a) shows a SEM picture of the device. The plunger gate ($\mathrm{V_P}$) finish with a disk of 200 nm diameter. $\mathrm{V_{DP}}$ is used for depleting the 2DHG beneath the plunger gate arm. Barrier gates between the SQD and the reservoirs have a width of 120 nm and their names are $\mathrm{V_{BT}}$ for the top barrier, $\mathrm{V_{BB}}$ for the bottom barrier and $\mathrm{V_{BR}}$ for the right barrier. Finally, to accumulate carriers from the ohmic contacts to the quantum dot, we use $\mathrm{V_{OT}}$ and $\mathrm{V_{OB}}$ as ohmic top and ohmic bottom gates. As it was seen in the previous chapter, the heterostructure field effect oscillates up to a few percent of mV. Sometimes the pinch-off voltages being positive and sometimes negative. Due to this variability, we specially thought this design to be functional for both scenarios. The high density of gates around the SQD allows a complete tuning of the confinement potential. On the other hand, the dot's chemical potential is sensitive to any of the gates, not only to the plunger. This effect is referred as cross-talk.

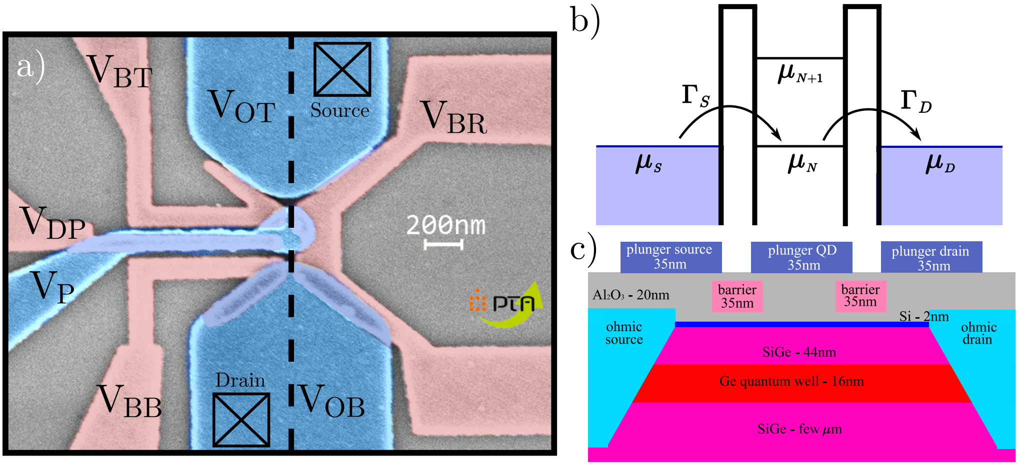


Figure 4.1: a) colored SEM picture of the SQD device. Red colored gates indicate the first gate layer while blue are for the second gate layer. Source and drain are connected to the top and bottom ohmic accumulation gates, respectively. b) represents a schematic view of the system chemical potentials. c), schematic that shows a transversal view of the layer stack along the dashed line in a).

Figure 4.1 b) shows a schematic of the system chemical potentials. As it was discussed in the theory section, when the dot's chemical potential μ_{N} is located between the source and drain chemical potentials, carrier transport is possible. Γ_{S} and Γ_{D} are the tunnel rates to source and drain respectively, and they are mainly controlled by gates $\mathrm{V_{BB}}, \mathrm{V_{BR}}$ and $\mathrm{V_{BT}}$. I emphasize "mainly" because of the cross-talk, the other gates around also play a role in the tunnel coupling. The dot's chemical potential μ_{N} is mainly controlled by $\mathrm{V_P}$. The chemical potentials μ_{S} and μ_{D} are given by the source-drain voltage bias.

In figure 4.1 c) we picture the layer stack along the black dashed line in figure 4.1 a). The barrier gates are fabricated in the first gate layer (at 56 nm from the quantum well) and the accumulation gates in the second gate layer (at 66 nm from the quantum well).

4.2 Measurement technique and set-up

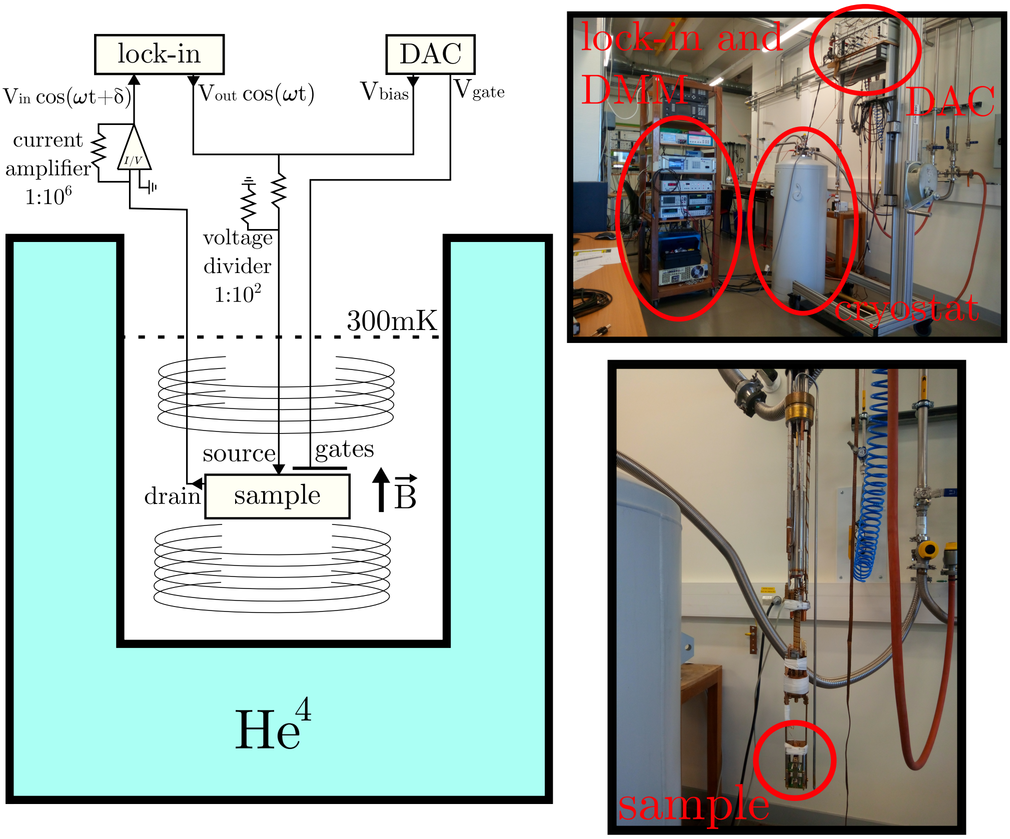


Figure 4.2: Cryostate and wiring schematic of the set-up. The cooling power is driven by an He^3 condensation circuit. It can last up to 11 h at 300 mK. The pictures are taken in the lab showing the fridge chamber and the electric measurement systems. We can also see the probe with the sample holder and the cooling system.

The set-up used to measure the SQD was a commercial **HelioxVT** from **Oxford Instruments**. It is a He^3 condensation cryostate with a base temperature of 300 mK. The schematic of the fridge and the measurement set-up is represented in figure 4.2. For sample characterization, we measured the differential conductance with a standard low-frequency (77.66 Hz) lock-in technic . The chosen AC-amplitude was 30 μV. In the charge-noise section, the device was measured in direct current using a DMM (Digital Multimeter). The set-up also includes a coil magnet with a **Cryomagnet** power supply which provides a bipolar magnetic field. It is oriented perpendicular to the sample. For gating the device, we used a DAC (Digital Analog Converter) featuring 24 low noise DC sources with 16 bits on ±2V or 8 V. Along the source-drain DC line there is a voltage divider of 10^{-2}V/V for the DC bias and 10^{-4}V/V for the low-frequency lock-in bias. In the detector chain there is an I/V-converted.

4.3 Tuning a SQD into Coulomb blockade regime

As it was discussed in the theory section, there are two requisites to enter the Coulomb blockade regime. First, the quantum dot charging energy must excess thermal energy $k_B T \ll e^2/C$. Second, the tunnel resistance from the reservoirs to the SQD should be larger than the quantum of resistance $R_t > R_0$. In order to find the gate voltages that electrostatically define a Coulomb blockade regime, we always follow the same procedure. First, we accumulate carriers below the accumulation gates ($\mathrm{V_P}$, $\mathrm{V_{OT}}$ and $\mathrm{V_{OB}}$,) until we observe current from source to drain. Second, we test the quantum transport regime by forming a QPC with each barrier gate ($\mathrm{V_{BT}}$, $\mathrm{V_{BB}}$ and $\mathrm{V_{BR}}$,). Finally, we try to observe Coulomb oscillations with the plunger gate. This method has been successfully used during all the experiments.

4.3.1 Carriers accumulation

In the case that there are not carriers at zero gate voltage, we start by applying negative potential to the accumulation gates, $\mathrm{V_P}, \mathrm{V_{OT}}$ and $\mathrm{V_{OB}}$, until current is observed between source and drain. This state is represented in figure 4.3 a). The fuchsia cloud is a schematic representation of the 2DHG. We want to characterize the conduction threshold voltages for each accumulation gate. To do so, conductance is measured by sweeping independently $\mathrm{V_P}, \mathrm{V_{OT}}$ and $\mathrm{V_{OB}}$, and by sweeping the three gates at the same time. Figure 4.3 b) shows the results of such sweeps. When only one gate is swept, the other two are kept at −700 mV and all the rest ($\mathrm{V_{BB}}, \mathrm{V_{BR}}, V_{DP}$, $\mathrm{V_{BT}}$) are at 0 V. The maximum conductance is $\mathrm{dI/dV} = 0.29\mathrm{e}^2/\mathrm{h}$ when the three gates are at $\mathrm{V_{gate}} = -700\mathrm{mV}$. At that voltage, the circuit resistance is $\mathrm{R} \approx 89\mathrm{k}\Omega$. In the circuit we have in series the resistance of the measurement elements (I/V converter, voltage divider, wires, etc...) and the resistance related to the sample (tunnel barriers, 2DHG resistivity, ohmic contacts, etc...). The sum among the measurements elements is not larger than 10 kΩ. The other $\approx 79\mathrm{k}\Omega$ resistance comes from the sample. We don't know what

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is the 2DHG density, so we cannot estimate its resistivity. But we know that the hole gas reach saturation in less than 150 mV of the top gate. Then we can say that in the SQD device, the hole gas is highly accumulated, so its contribution to resistance is of $\sim 150\Omega\square$. We presume that the main contributions for resistance come from the ohmic contact resistance and the tunnel barriers. The tunnel resistance should be at least $R_t > R_0 = 25.8\text{k}\Omega$, and this resistance is twice because of the two tunnel barriers. The rest of the total resistance should come from the ohmic contact resistance. In the etching step before the Al deposition for the ohmic contact, the etched deepness came out larger of what we aim for. This means that the metal is side-contacted with the quantum well in a smaller surface than in other samples. This effect could increase the ohmic contact resistance.

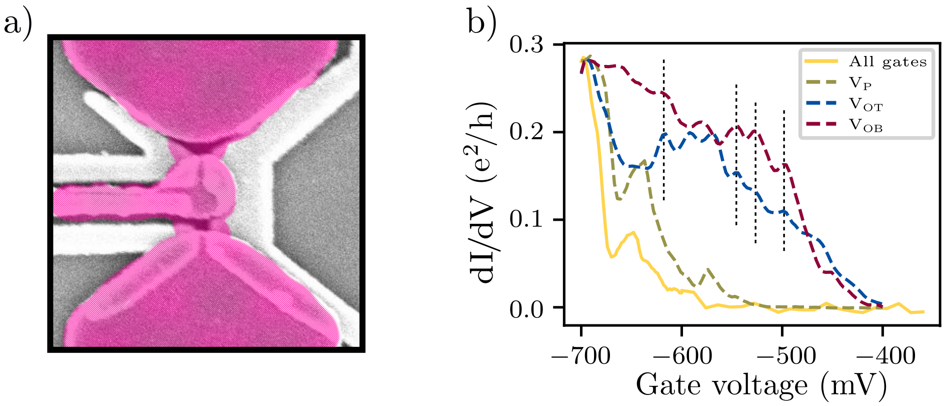


Figure 4.3: a) schematic representation of the 2DHG density over a device SEM picture. b) differential conductance versus the accumulation gate voltage for the three accumulation gates. Dashed lines show the coinciding peaks for $\mathrm{V_{OT}}$ and $\mathrm{V_{OB}}$.

The pinch-off voltage for the ohmic gates is around $\mathrm{V_{OB,OT}} = -400\text{mV}$, and for the plunger gate $\mathrm{V_P} = -500\text{mV}$. The threshold voltage of the three gates is limited by the lower one among them, in this case $\mathrm{V_P}$. We observe that for both ohmic accumulation gates, the voltage is higher than for the plunger gate $\mathrm{V_{OB,OT}} > \mathrm{V_P}$. This is understood from an electrostatic potentials point of view. The distance to the quantum well is the same for all gates: $\mathrm{t} = 66\text{nm}$, but the width of each gate is different. The QD plunger gate width is $\mathrm{w_{QD}} = 200\text{nm}$ and the ohmic contact accumulation are $\mathrm{w_{ohmic}} = 1\mu\text{m}$, figure 4.4 shows a schematic of both gates and their distance to the quantum well.

From the schematic in figure 4.4, we can picture the capacitor model for each gate. The limit where less gate potential is needed to accumulate charges in the quantum well is the infinite plate capacitor. A comparison of the gate width with the capacitor thickness raises that $w_{QD}/t \approx 3$ and $w_{ohmic}/t \approx 15$. The ohmic accumulation gates are closer to an infinite parallel plate capacitor than the QD plunger.

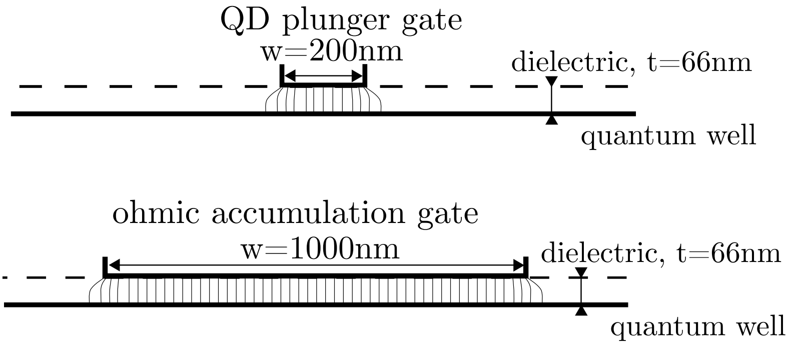


Figure 4.4: Schematic of the QD plunger and the ohmic accumulation gates. Both designs are made to scale.

Another feature in the plot are the oscillations between $\mathrm{V_{OT,OB}} = -500\mathrm{mV}$ and $\mathrm{V_{OT,OB}} = -700\mathrm{mV}$, marked with dashed lines in figure 4.3 b). We observe that the peaks are at the same gate voltage for $\mathrm{V_{OT}}$ and $\mathrm{V_{OB}}$. Those oscillations may correspond to the SQD Coulomb peaks in the regime where barrier gates are very transparent $e^2/C < h\Gamma_{barrier}$. This highly coupled dot is formed by the gate constriction in the sample geometry. When sweeping the ohmic gate voltage, we are controlling the dot chemical potential by cross-talk. Both ohmic gates are more-less symmetric with respect to the QD plunger gate, and that is the reason why the oscillations coincide in gate voltage. We can also observe two oscillations with $\mathrm{V_P}$ at $\mathrm{V_P} = -575\mathrm{mV}$ and $\mathrm{V_P} = -650\mathrm{mV}$.

From these measurements, we conclude that is possible to form a source-drain conduction channel using the accumulation gates.

4.3.2 QPC with barrier gates

Once we know that the accumulation gates have control over the 2DHG density, we probe the barrier gates. While the accumulation gates are set at $\mathrm{V} = -700\mathrm{mV}$, QPC contacts are formed using $\mathrm{V_{BB}}, \mathrm{V_{BR}}$ and $\mathrm{V_{BT}}$. Figure 4.5 a) presents, in red and in blue, a schematic of the two possible sample's QPC. From the data in figure 4.5 b) we observe that the differential conductance as a function of $\mathrm{V_{BR}}$ and $\mathrm{V_{BT}}$ follow almost the same line. If we sweep $\mathrm{V_{BB}}$, the threshold voltage increases. We don't know what is the cause of the pinch-off difference, it may come from lithography or disorder potential, or even material issues. What we care about is that we are able to close the conductance channel with the barrier gates.

4.3.3 Coulomb peaks with plunger gate

Last step to probe the quantum dot viability is, of course, to form a quantum dot. We set the accumulation gates at $\mathrm{V} = -600\mathrm{mV}$ and the barrier gates close to the QPC pinch-off of figure 4.5 b). Once in this configuration, we apply a

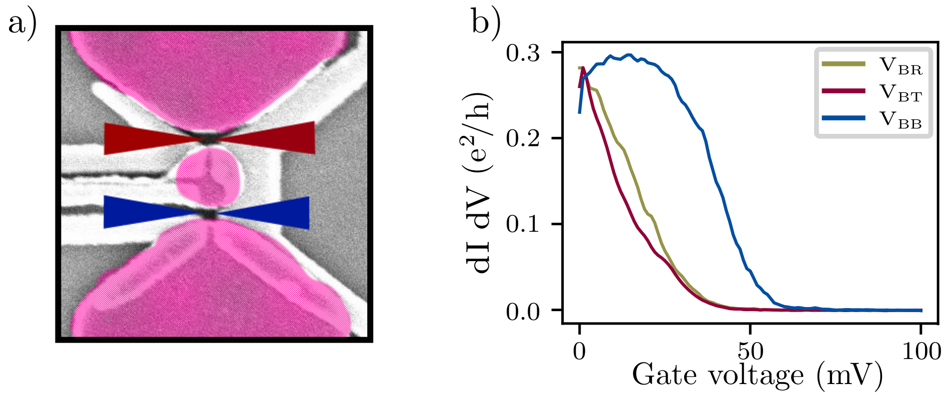


Figure 4.5: a) shows a schematic of a QPC formed with the barrier gates. b) source-drain differential conductance vs barrier gate voltage. While sweeping one gate, the other barrier gates remain at 0 V. Accumulation gates are still at −700 mV and each plot in b) is taken while the other barrier gates remain at 0 V

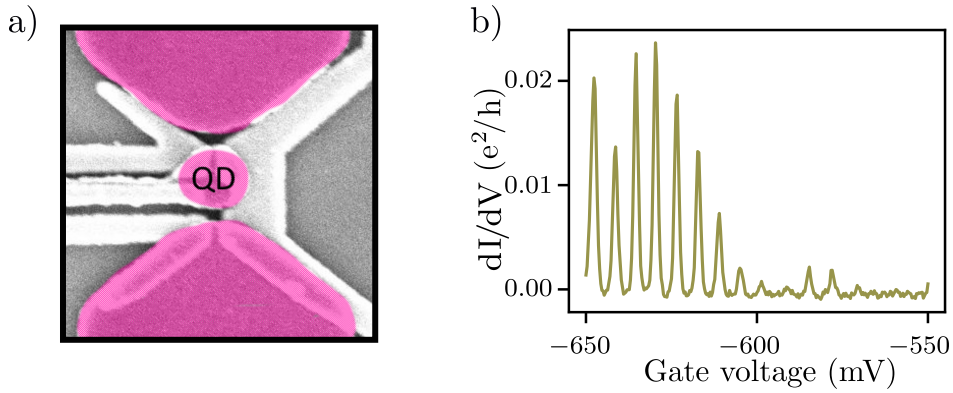


Figure 4.6: a) is a schematic of the hole density in a quantum dot. b) shows differential conductance versus plunger gate V_P. The oscillations observed are Coulomb peaks.

voltage to V_{DP} to deplete the 2DHG beneath the plunger gate. This voltage will be constant all along the next experiments, $V_{DP} = 500$mV. Then after, we sweep V_P. If oscillations are found, we know we are in the good regime. If not, we slightly change the tunnel barriers and repeat the plunger sweep.

A qualitative representation of the hole gas density is given in figure 4.6 a). In figure 4.6 b) we see a typical plot of Coulomb peaks. When $V_P > -600$mV, the peaks are separated by Coulomb blockade. This is noticeable because the conductance drops to zero between oscillations. The SQD regime is $k_B T \ll h\Gamma, e^2/C$. Below this voltage, $V_P < -600$mV, the peak tails overlap with each other, so we don't find Coulomb blockade anymore. This is caused by too large tunnel rates, which induce conductance through cotunneling events.

4.4 Symmetric tunnel rate for barrier gates

Symmetric tunnel rates were discussed in the theory section 1.2.3. In Coulomb blockade regime, with barrier tunnel rates $k_B T \ll h\Gamma \ll e^2/C$, the highest conductance amplitude is achieved when both tunnel rates are equal $\Gamma_{BB} = \Gamma_{BT}$ [116, 117]. In this section, we will see how to find the regime $h\Gamma \ll e^2/C$ and how to symmetrize the barrier as much as possible.

4.4.1 Barrier gate space

First approach is shown in figure 4.7 a). We set some barrier voltage value and sweep the plunger gate voltage. We see some Coulomb peaks in a regime where barrier gates are widely open. Once we set $\mathrm{V_P}$ in the top of a Coulomb peak (black arrow), we start to explore the barrier vs barrier gate space. Results are in figure 4.7 b). Here, $\mathrm{V_{BB}}$ and $\mathrm{V_{BT}}$ limits are 0 and $-40\,\mathrm{mV}$. We observe that $\mathrm{V_{BT}}$ totally suppress the current if $\mathrm{V_{BT}} > -15\mathrm{mV}$ while $\mathrm{V_{BB}}$ does not fully close the conductance channel. From this plot we learn that barrier gate influence in the 2DHG density is not symmetric in voltage. With this we mean that the same voltage in both gates, does not produce the same effect in the tunnel rates. We had an insight of this asymmetry in figure 4.5, where the QPC formed by $\mathrm{V_{BB}}$ and $\mathrm{V_{BT}}$ are not equal. To form a QD, we need to go to the low tunnel rate regime. For this is very useful to know the barrier gate pinch-off values. In order to do so, we need to continue the color-map towards positive values in $\mathrm{V_{BB}}$. In our system, source tunnel rate is controlled by $\mathrm{V_{BT}}$ and drain tunnel rate by $\mathrm{V_{BB}}$. We say $\Gamma_{BT} \equiv \Gamma_S$ and $\Gamma_{BB} \equiv \Gamma_D$.

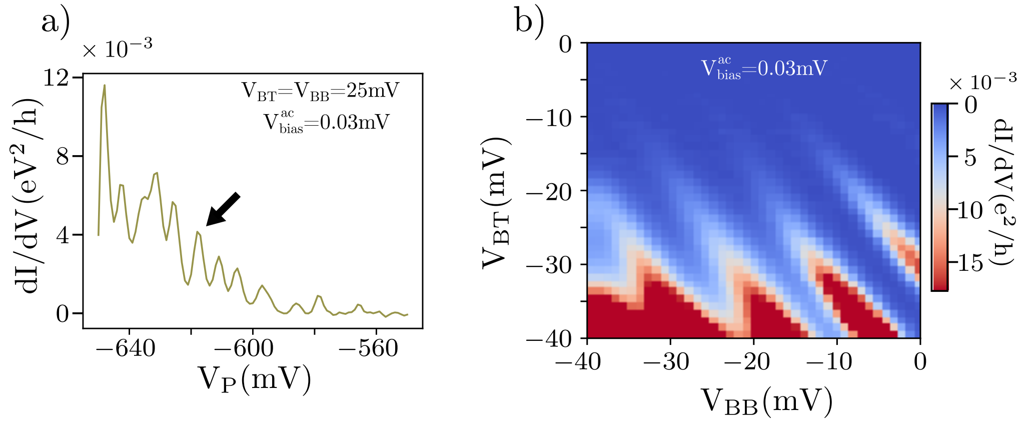


Figure 4.7: a) differential conductance versus plunger gate. It shows some Coulomb peaks in the first approach to barrier optimization. The overlapping of the peak tails indicates that the QD dot is in the high conductance barrier regime. b) color-map exploring the $\mathrm{V_{BB}}$ vs $\mathrm{V_{BT}}$ space. The plunger voltage is set to the black arrow value in figure a).

Figure 4.8 a) is an extended region from 4.7 b) to a more positive $\mathrm{V_{BB}}$ voltages.

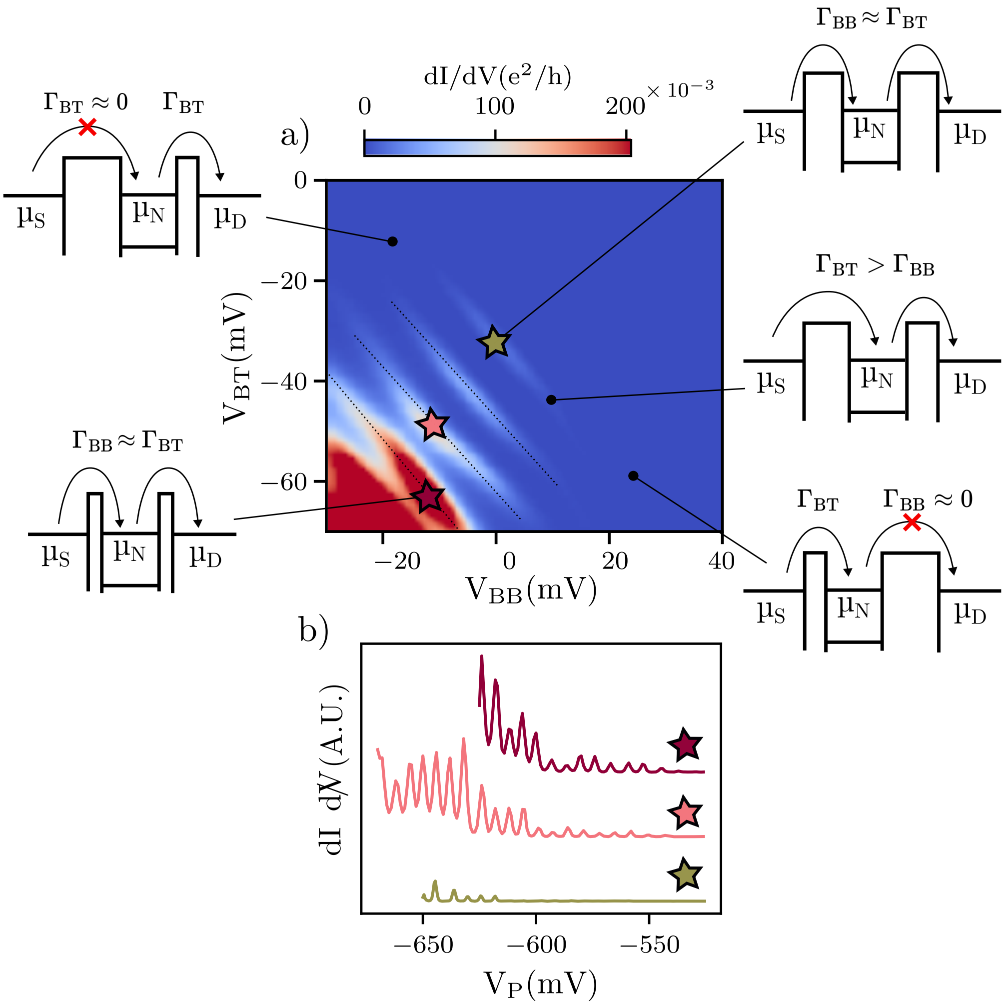


Figure 4.8: a) color-plot of the differential conductance versus barrier gates V_{BB} and V_{BT}. We reach the pinch-off value for the gate voltage where current is fully suppressed. There are different regimes for the barrier gates represented with schematics around the color plot. When $\Gamma_{BT} \approx 0$ or $\Gamma_{BB} \approx 0$, conductance is totally suppressed. Inside the conductance diagonal features (withe diagonal marks), we sweep in the regime where tunnel rates are quasi symmetric $\Gamma_{BT} \approx \Gamma_{BB}$, to the extremes where $\Gamma_{BT} > \Gamma_{BB}$ or vice-versa. The dashed lines indicate the conductance regions used to define the voltage for the symmetric tunnel rates. b) differential conductance versus plunger gate V_P in three different configuration for barrier gates. Each color star correspond to the color star in figure a).

We can observe how both barrier gates close the conductance channel. This happens for gate values $V_{BB} > 15$mV and $V_{BT} > -15$mV. The diagonal features in the middle of the plot correspond to Coulomb peaks tuned by the barrier gates, we will use them to symmetrize the tunnel rates. We can observe how conductance modulates along the longitudinal axis of these regions (dashed lines), being larger around the middle and vanishing as it approach the edges. Inside these features, the point with the largest conductance shoueld have the most similar tunnel rates. This symmetry in barriers is specific to a value of $\mathrm{V_P}$. Due to the cross-talk, a change in plunger value would move the symmetric point somewhere else.

In figure 4.8 d) we observe three conductance plots sweeping $\mathrm{V_P}$ in three different symmetric configuration for the barrier gates, represented with colored stars in figure 4.8 a). The bottom plot (green) is the one done with the lowest tunnel rates, the middle plot (pink) is in an intermediate stage and the top one (maroon) has the largest tunnel rates. We can observe that the plunger voltage $\mathrm{V_P}$ for the first Coulomb peak is different for each cut. This effect is again due to the cross-talk between the barrier gates and the SQD. When barrier gate voltage decrease, to compensate the effect on the SQD, the plunger gate must apply higher voltage. And the opposite for an increasing barrier gate voltage.

With this method we found a technique to easily tune the barrier gates in a close-to-symmetric regime. But we can go a bit further.

4.4.2 Sweeping barrier gates along the symmetric tunnel rates

So far, we have found the quasi-symmetric tunnel rates for a single pair of barrier gate voltages $\mathrm{V_{BB}}$ and $\mathrm{V_{BT}}$. We can define a linear combination of those gates that will keep the symmetry at different voltages. We call this linear combination a virtual barrier gate V_{com}. The new gate is extracted by joining the highest conductance point in each diagonal feature from plot 4.8 a). The green dashed line in figure 4.9 b) is a schematic representation of the line along which V_{com} exists.

The mathematical expression for the virtual gate is

$$\mathrm{V_{com}} = \mathrm{V_{BB}} + 1.38\mathrm{V_{BT}}. \tag{4.1}$$

We observe how much one barrier changes with respect to the other to keep the tunneling symmetric. In figure 4.9 a) we see a color plot of conductance with $\mathrm{V_{com}}$ and $\mathrm{V_P}$ as axis. At higher values of $\mathrm{V_{com}}$, both barrier gates remain closed. When $\mathrm{V_{com}}$ becomes more negative (tunnel rate increase), more Coulomb oscillations appear in the plot, but also the peak broadness increase. If $\mathrm{V_{com}}$ is too negative, the high conductance barriers prevent the formation of Coulomb blockade. This is observable in the bottom left corner, where conduction is strongly affected by disorder.

We can see the cross-talk between the barrier gates and the QD in the Coulomb peaks diagonal displacement. As mention before, this cross-talk is responsible for the QD chemical potential tuning with the barrier gates. From the diagonal displacement slope of plot 4.9 a) we can extract $V_P/V_{com} = -0.596$. Each mV swept in V_{com} is a virtual tuning of V_P of $-0.596\,\mathrm{mV}$. It could be possible, following this argument, to create a second virtual gate $V_P^{(v)}$ with the plunger gate which account all the chemical potential influence of the barriers. This new virtual gate would modify the QD chemical potential without affect the tunnel rates, its equation is $V_P^{(v)} = V_P - 0.596 V_{com}$. Unfortunately, we did not have enough time to do experiments with this new virtual gate. We can find the use of virtual gates in some publications [49, 52].

In figure 4.9 c) we see two horizontal cuts of the color plot at different $\mathrm{V_{com}}$. The green one is done with low tunnel rates $h\Gamma_{BT,BB} \ll e^2/C$. We observe Coulomb blockade between peaks and a lower conductance maximum compare with the other cut. The pink cut is done with barrier gates more open. In that regime, Coulomb peaks overlap with each other and the conductance increase.

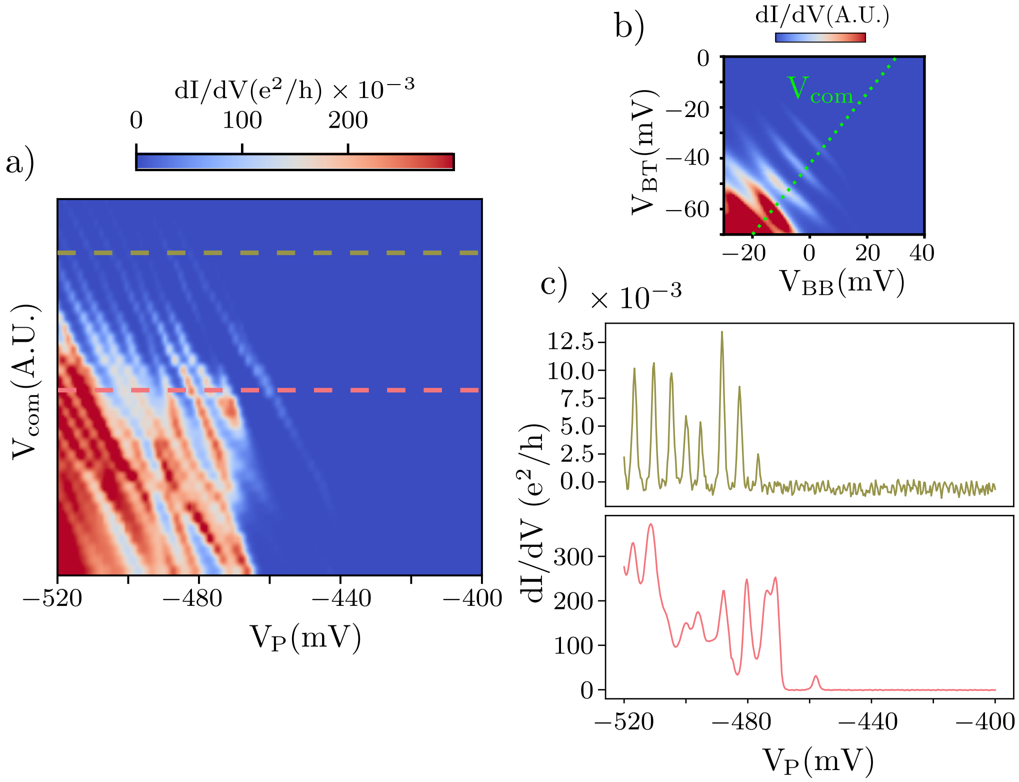


Figure 4.9: a) color plot of conductance with $\mathrm{V_P}$ in the horizontal axis and the linear combination of barrier gates $\mathrm{V_{com}}$ in the vertical axis. b), in green the barrier gate combination that defines $\mathrm{V_{com}}$c) two cuts in the color plot to observe the conductance versus $\mathrm{V_P}$ for different barrier gates values. In both regimes, the barrier gates are supposed to be symmetric.

This study is interesting to find the barrier gate values where we can preserve the Coulomb blockade regime and, at the same time, try to maximize the conductance signal. For the next experiments in the chapter, we just choose a slide of V_{com} from figure 4.9 a).

4.5 Coulomb diamonds

Once the tunnel barriers are tune with symmetric tunneling rates, we performed non-linear transport measurements to observe Coulomb diamonds and extract some figures of merit, like charging energy (E_C), lever arm (α) and QD excited states (ΔE). Figure 4.10 shows a compilation of some Coulomb diamonds observed in different architectures. The experiment consists in measuring differential conductance sweeping the QD plunger gate versus V_{bias}. The diamond structure formed in the plot are the so-called Coulomb diamonds. The inner part of the diamond (zero conductance) is in Coulomb blockade and the charge number in the dot is fixed. When the bias voltage overcomes the limits of the diamond, an electrochemical potential state falls in the bias window, and current flows through the SQD.

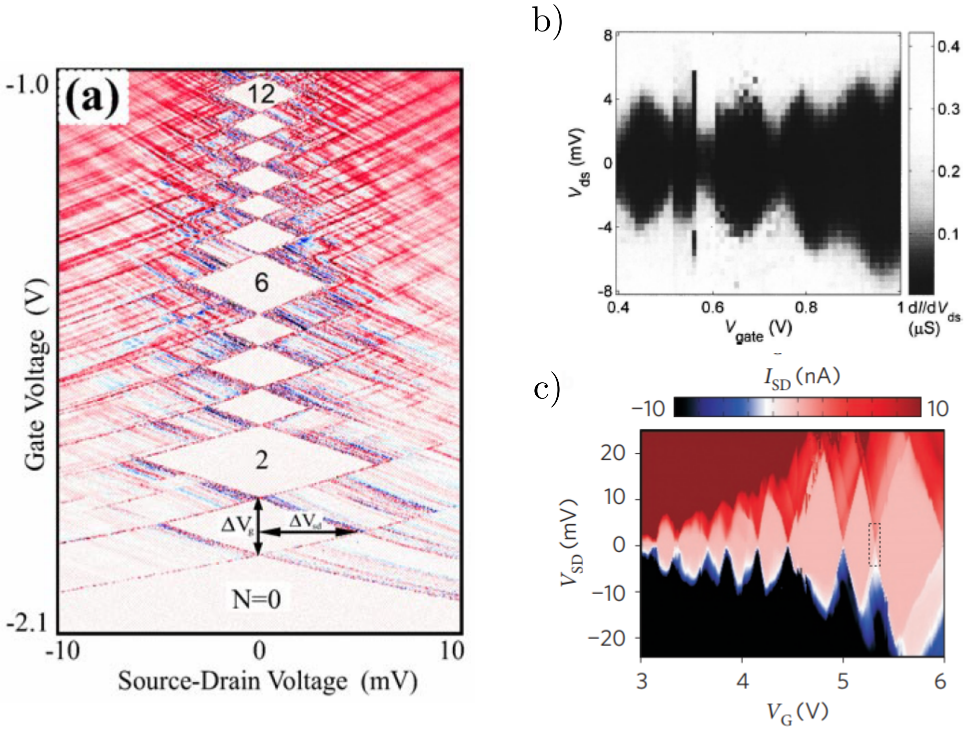


Figure 4.10: Coulomb diamonds in different devices. a) is taken from [2] in the few-electrons regime. b) are the first Coulomb diamonds measured in Si/SiGe heterostructures [118]. c) are data taken in SiGe nanocrystal [9]. It is noticeable for a) and c) how the diamond size increase as we approach an empty dot. This is due to an increasing addition energy.

We performed the same experiment in our SQD and results can be seen in figure 4.11. It exists some asymmetry in the diamonds. This indicates a difference between the plunger gate coupling to the dot C_G and the source and drain coupling C_S, C_D, more precisely, the coupling to the plunger gate is larger than the others

$C_G > C_S, C_D$.

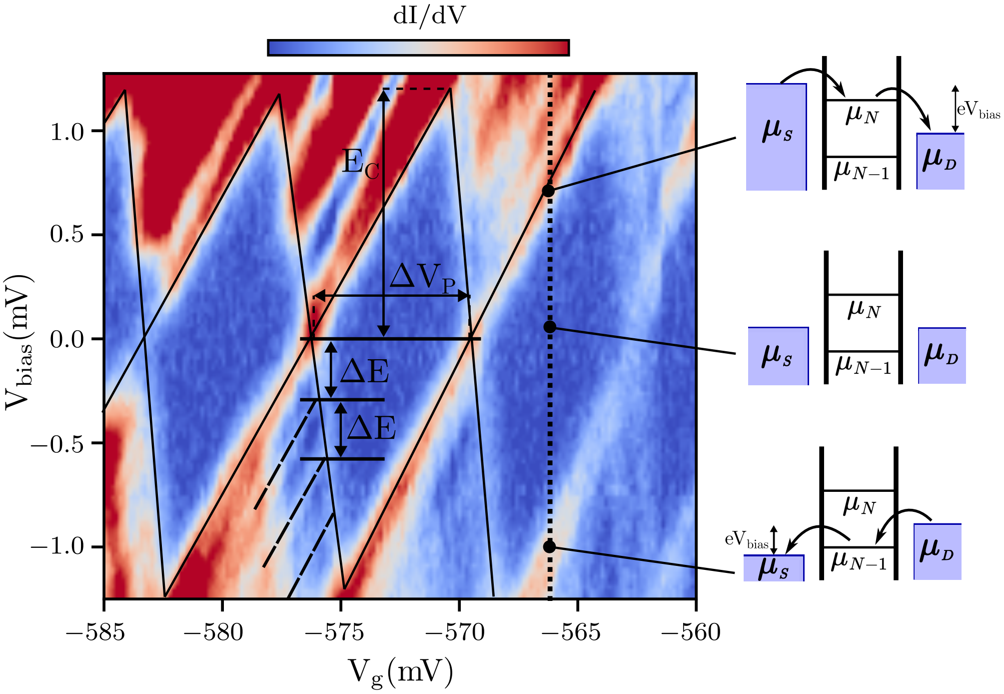


Figure 4.11: Coulomb diamonds in the SQD. The plot is a color-plot for the differential conductance sweeping V_P vs V_{bias}. The barrier gate voltages are $V_{BT} = -47$mV and $V_{BB} = -14$mV. The charging energy is $E_C = 1.2 \pm 1$meV. The plunger voltage difference between Coulomb peaks is $\Delta V_P = 6.7$mV. In the bottom of the plot we can see three excited states with $\Delta E = 275\mu$eV. At the right there are three schematics showing the system chemical potential at the diamond edge and in the Coulomb blockade.

First thing we will extract from the plot is the lever arm (α factor). The lever arm is the capacitance coupling ratio between the plunger gate V_P and the SQD total capacitance. It shows the effective control of the plunger voltage on the dot chemical potential. In the constant interaction model, this is expressed as the ratio between the gate capacitance (C_G) and the total dot capacitance (C); $\alpha = C_G/C$. The distance between two Coulomb peaks at zero bias is $e/C_G = \Delta V_P$. The height of the diamonds is the addition energy E_{add}. This energy depends on the particle number inside the dot and the orbital filling. It is $E_{\text{add}} = E_C$ when two holes are charged in the same orbital and $E_{\text{add}} = E_C + \Delta E$ when the holes are charged in different orbital. With the equations we have, we can then divide both values and write

$$\alpha = \frac{E_C}{e\Delta V_P}. \tag{4.2}$$

From figure 4.11 we obtain $\alpha = 0.18$eV/V.

The charging energy can be used to estimate the QD size. We consider the SQD as a 2D charge disk which is capacitively coupled to the top gate. The simplest assumption is considering parallel plate capacitor

$$C_G = \frac{\epsilon_{\text{eff}}\epsilon_0 A}{d}, \tag{4.3}$$

where ϵ_0 is the vacuum dielectric constant, ϵ_{eff} is the effective dielectric constant. A and d are the disk surface and the distance between gate and the quantum well, respectively. For this value, we will take $\epsilon_{\text{eff}} = 11.8 \pm 1$, calculated in the previous chapter. Using that $\Delta V_P = e/C_G$ and knowing that the distance between gate and quantum well is 66 nm, we obtain a disk surface of $A = 15000 \pm 2000\text{nm}^2$ with a diameter $D = 140 \pm 20\text{nm}$. This value is in accordance with the 200 nm diameter disk in SEM picture 4.1 a). The calculated SQD size is smaller, something understood taking into account the distance between the plunger gate and the quantum well.

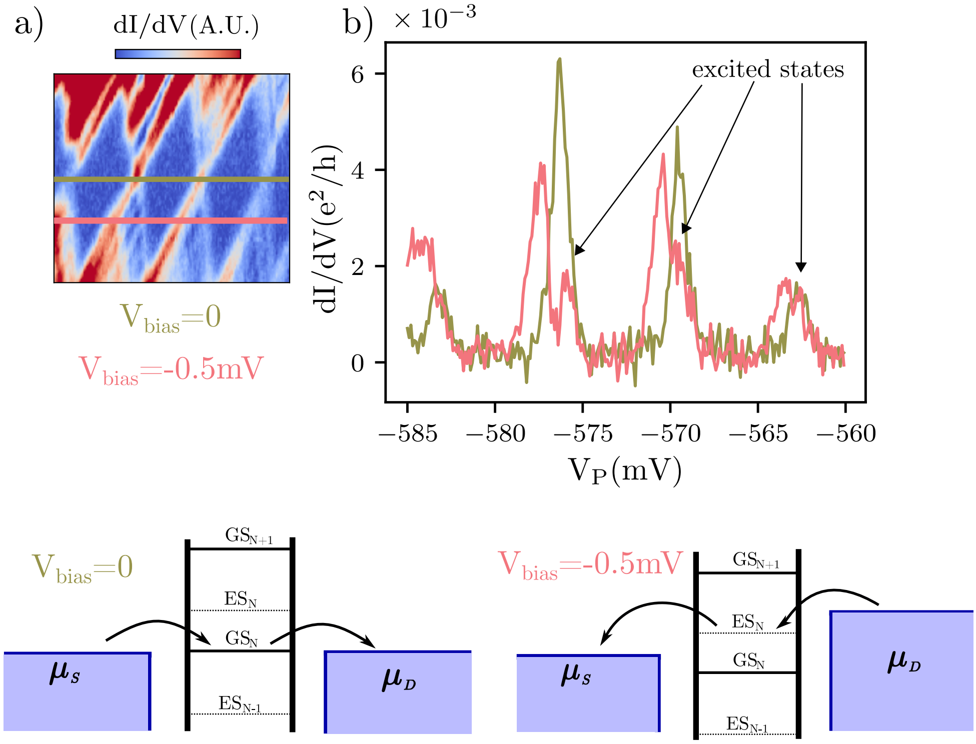


Figure 4.12: a) color-plot from figure 4.11 with two cuts at different bias. In b) we can see the differential conductance versus V_P for those two cuts. The appearance of a second oscillation each Coulomb peak is due to the conductance through an excited state. In the bottom we can see a schematic for each case. GS stands for "Ground State" and ES is "Excited State".

Another feature visible in figure 4.11 are the conductance through the SQD excited states. Figure 4.12 b) shows two cuts at two different bias from the

Coulomb diamonds plot, shown in figure 4.12 a). At zero bias, we see a single peak for each conductance level in the dot. When bias is applied, we observe that the peak unfolds in two peaks. One of them correspond to conductance through the ground state and the other through the excited state. The exited state in the first peak ($\mathrm{V_P} = -576\mathrm{mV}$) is very well resolved, it indicates that the tunneling rate is smaller than the excited energy difference inside the QD $h\Gamma < \Delta E$. That is not the case for the third peak ($V_P = -562\mathrm{mV}$). The peak tail of the excited state and the ground state are merged, the regime is $h\Gamma \approx \Delta E$. In both cases, the barrier gate voltages are the same, but not the plunger gate voltage. The cross-talk between V_P and the tunnel barriers is enough to sweep the tunnel rates from one regime into the other.

The last interesting thing we can calculate is the QD size from the excited state's energy difference. We can approximate the dot's potential to a square quantum well, the level energy difference is given by equation 1.31. To know the size, we write

$$L = \sqrt{\frac{1}{\Delta E}\frac{\hbar^2 \pi}{m_h^*}}. \tag{4.4}$$

The same argument can be used but with the parabolic potential of equations 1.33 and 1.29. If we replace the terms with obtain the ground state characteristic length of

$$l_0 = \sqrt{\frac{2\hbar^2}{m^* \Delta E}}. \tag{4.5}$$

In our SQD, the excited energy is $\Delta E = 275\mu\mathrm{eV}$. We don't know the effective hole mass at the measurement density, but we know it should be in a range from $m_h^* = 0.02 m_e$ to $m_h^* = 0.09 m_e$ [102], where m_e is the vacuum electron mass. The estimated length for a two-dimensional box vary from $L \approx 200\mathrm{nm}$ to $L \approx 100\mathrm{nm}$, and for a parabolic potential $l_0 \approx 170\mathrm{nm}$ to $l_0 \approx 80\mathrm{nm}$.

The three methods to calculate the QD size give similar values. In the last two method, we considered a square potential and a parabolic potential, whereas in reality, the shape of the dot is unknown. The assumption to a disk is also not true. The disorder potential in the quantum well affects the dot shape. We can say that at least, the estimated size is in the order of magnitude of the expected value.

4.6 Charge-noise

Charge noise is one of the limiting factor for quantum devices [119]. In the last years, research advances has been done in InGaAs quantum dots [120], GaAs heterostructures [121] and Si/SiGe heterostructures quantum dots [122]. The dominant cause of the noise is believed to be the sum of two-level fluctuators with different decay rates. Each of the fluctuators contributes to noise with a

Lorentzian spectrum function that has a cutoff at the decay rate. The sum of many fluctuators with equally distributed decay rates raises a 1/f noise spectral density. This power law is known as telegraphic noise.

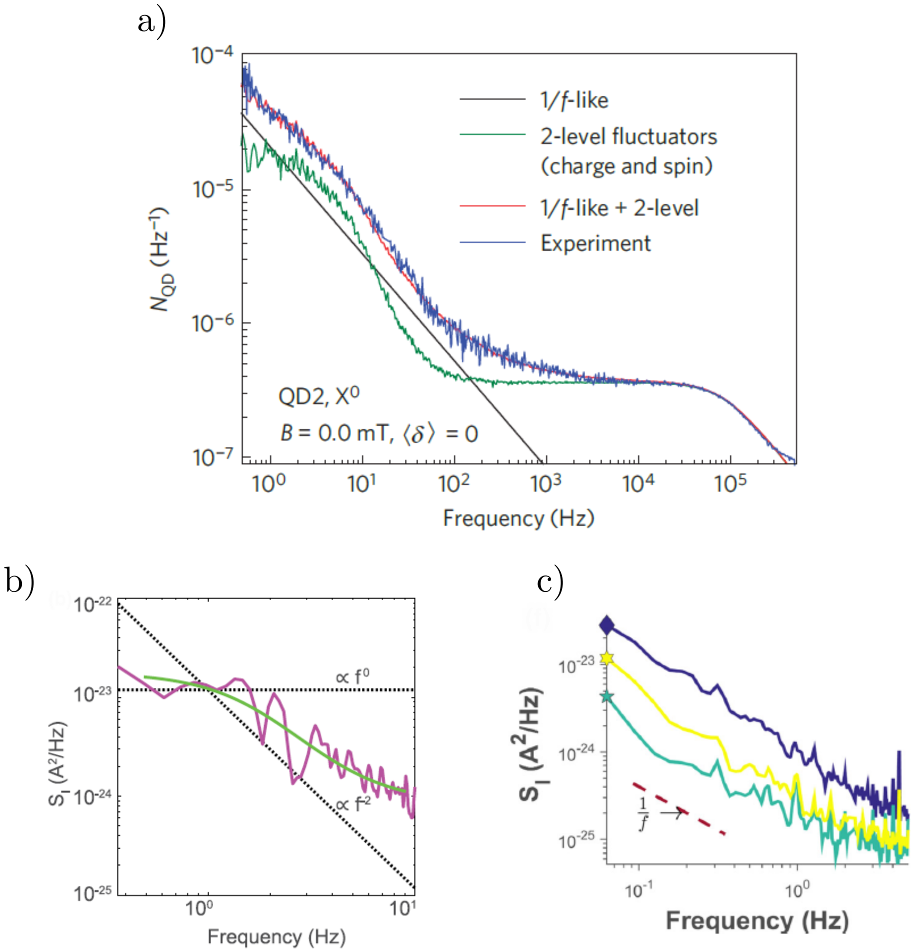


Figure 4.13: Charge-noise measurements taken from the literature, a) [123] measured in InGaAs quantum dots, b) [124] in Si/SiGe quantum-well electron quantum dots and c) [125] in Si/SiO$_2$ devices. The case in a), data are fit to the sum of two functions, a 1/f telegraphic noise and the two-level contribution with a given decay rate. In b), the fit is done to a power law 1/f and a Lorentzian-like function of $1/(f^2+1)$, which account again with the single two-level fluctuator contribution. For c), the fit is directly done to a 1/f.

In some cases, like the ones shown in figure 4.13 a) and 4.13 b), the best fit for the charge-noise spectrum is a sum of a 1/f power law and a single fluctuator contribution. In figure 4.13 a) they calculated the noise for two decays rates, one for charge and one for spin. For the case exposed in 4.13 c), a simple 1/f function can fit the data. With these three examples we want to illustrate that charge-noise spectrum for QD devices can have different behaviour depending on the device. The general trend is to have a 1/f spectrum of noise. However, in presence of few fluctuators well coupled to the QD, it is possible that the noise spectrum is affected by 1/f^2 spectral component as a signature of single fluctuators. It can be related to defects in the lattice or surface states [123]. In the following, we will show the analysis that we performed in our devices.

The first approach to charge-noise we did is the color plot shown in figure 4.14 a). Here we studied the ultra-low frequency noise ($\sim$ 1.7mHz). We swept over several Coulomb peaks and wait 10 min before doing another sweep. The Coulomb peak displacement in plunger gate voltage is due to the SQD chemical potential perturbations. There are two remarkable Coulomb peak displacement where the peak moves over 2 mV (the double of the peak width) in plunger gate, after 170 min and after 290 min. This experiment evidences the slow dynamics in the sample and gives us a lower boundary in frequency for the next measurement.

In figure 4.14 b) there is the Coulomb peak measurement where the charge-noise was calculated. A deeper analysis of the peak width is in annex B. In order to extract information about charge-noise over several frequencies, we set $\mathrm{V_P}$ in two regimes: at Coulomb blockade (pink star $\mathrm{V_P} = -541$mV in figure 4.14 b)) and at the peak slope (blue star $\mathrm{V_P} = -553.5$mV in figure 4.14 b)). At the slope, the sensitivity to the chemical potential fluctuations is maximal [124]. We observe the charge-noise produce by the sample environment and the contribution from the electronic. In Coulomb blockade, current through the sample is zero, so any noise must come from the electronics in the set-up, like the I/V converter and the DMM.

For each regime, we measure current over two minutes, as it shown in figure 4.14 c). The upper time limitation was set to avoid the strong peak displacement observed in figure 4.14 a). The lower limitation was given by the cycling time of the DMM, each point in 4.14 c) was taken with a sampling rate of 10Hz. It is already clear that the dispersion in the peak slope is much larger than in Coulomb blockade. From the current plot, we can calculate the SQD chemical potential oscillations. It goes as followed.

We can make use of the known lever arm α to extract that

$$\delta_I = \frac{dI}{dV}\frac{\delta_\mu}{\alpha}, \tag{4.6}$$

where dI/dV is the peak slope, δ_μ are the chemical potential energy fluctuations and δ_I are the current fluctuations. The energy dispersion is plotted in 4.14 d). We can use the relation between chemical potential and the current fluctuations to extract the current noise spectrum S_I and the charge noise spectrum S_μ:

$$S_\mu = \frac{1}{|dI/dV|^2}\alpha^2 S_I. \tag{4.7}$$

Current noise spectrum is the correlation function of the current amplitude. For the power spectra calculation, we will use the Barlett analysis method [126]. Its purpose is reducing statistical error. If a time measurement has non-correlated

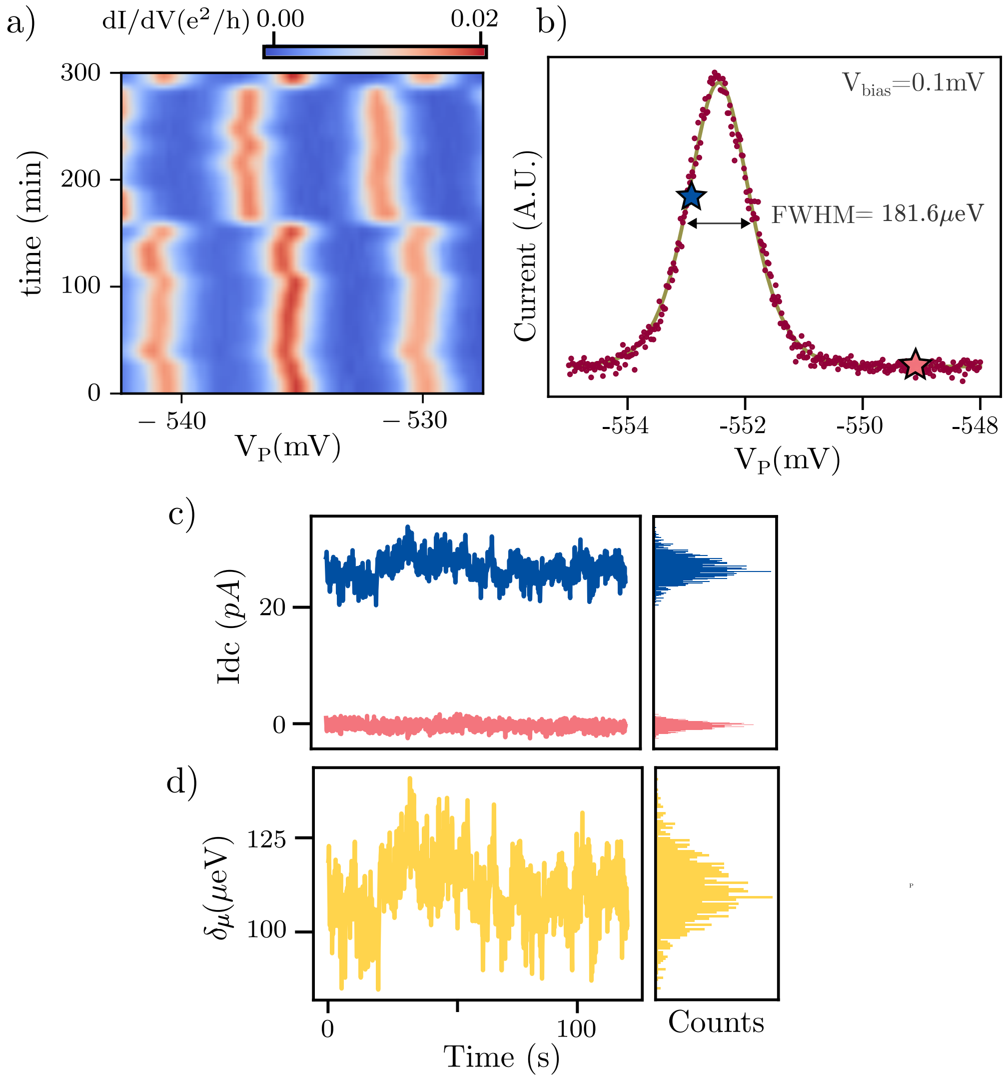


Figure 4.14: a) differential conductance color plot as a function of V_P and time. We can see that the resonance peaks are wiggling in the ultra-slow frequency regime. It is also remarkable the two big swept that displace the peak more than two times the peak width. b) Current versus plunger voltage showing the Coulomb peak where the charge-noise was measured. c) current versus time to extract the charge-noise fluctuations at higher frequency than a). Each point of this plot was taken with a cycle time of 0.1 s. Pink plot is at Coulomb blockade regime (pink star in b) and blue plot is at the Coulomb peak slope (blue star in b). At the right there is a histogram of the current values distribution d) chemical potential energy fluctuations versus time. This plot was derived from the slope current measurement in b). At the right we see the energy distribution.

noise, it is possible to take equal-spaced sections in time domain and apply the Fourier transform independently, then, average all the Fourier transform. We applied this method to the sample in sections of 12s. We were able to map noise between 0.16 Hz and 5 Hz.

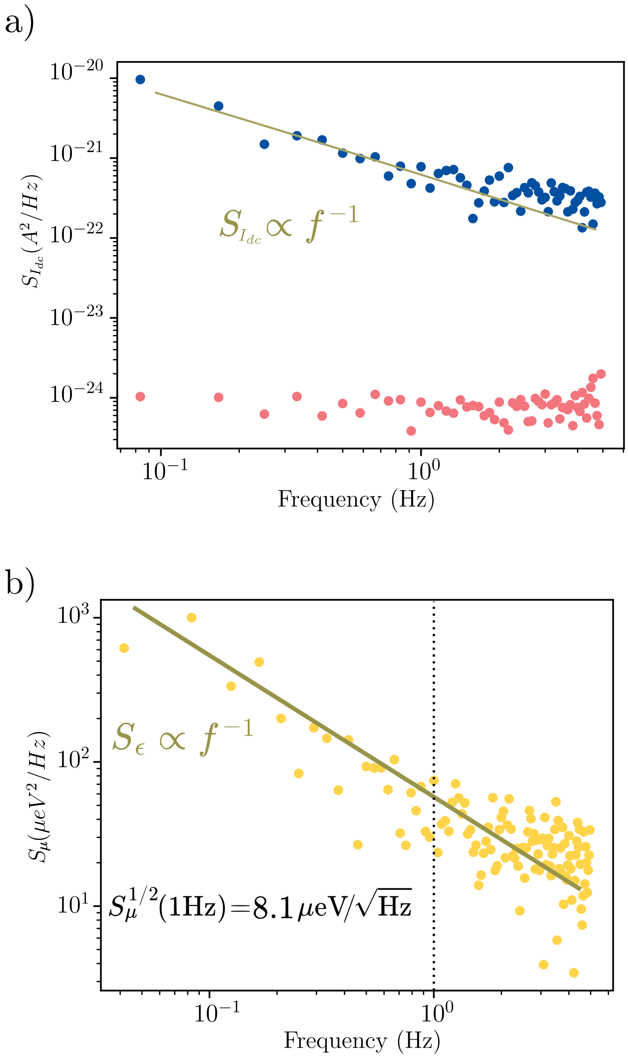


Figure 4.15: a) power spectrum of the current amplitude in figure 4.14 a). Blue points are in the Coulomb peak slope and pink in Coulomb blockade (represented in figure 4.14 b)). The solid line is a fit to a 1/f function. b) chemical energy power spectrum using the transformation of equation 4.7. The 1 Hz amplitude (marked with dashed line) is $S_\mu^{1/2}(1Hz) = 8.1 \pm 2\mu\text{eV}/\sqrt{\text{Hz}}$.

In figure 4.15 a) we can see the current noise spectrum in Coulomb blockade (pink) and in the peak slope (blue). The noise amplitude in Coulomb blockade is smaller than at the peak. More precisely, three order of magnitude smaller. This is understood since for Coulomb blockade perturbations, there is only the noise contribution from the electronics. Even though there are only two order of magnitudes, we plotted a 1/f function over the experimental data that fits the results very accurately. From this fit we will extract the 1 Hz noise amplitude.

The figure of merit used to measure the charge-noise.

Figure 4.15 b) represents the chemical energy spectrum. We have applied to the current amplitude the transformation in equation 4.7. The noise amplitude at 1 HZ is $S_{\mu}^{1/2}(1Hz) = 8.1 \pm 2\mu\text{eV}/\sqrt{\text{Hz}}$. The error is estimated by the window where the 1/f fits the experimental results. Two other devices measured with same conditions gave values of $7.9 \pm 2\mu\text{eV}/\sqrt{\text{Hz}}$ and $8.7 \pm 2\mu\text{eV}/\sqrt{\text{Hz}}$. The average is $8.3 \pm 2\mu\text{eV}/\sqrt{\text{Hz}}$. In the paper from Blake M. Freeman et al. [125] (data in figure 4.13 c)), they consider that the Coulomb peak current fluctuations are not just produced by the charge-noise, but also by fluctuations in tunnel rates. In order to get rid of the tunnel rates contribution to noise, they recorded current in both slopes of the Coulomb peak and in the top. At the peak maximum, the chemical potential fluctuations due to charge-noise does not affect the current through the device since $dI/dV_P = 0$. In other words, a change in the dot chemical potential would not be observed if the drift in gate voltage is small. With this assumption, any current fluctuation at the peak top comes from a change in the tunnel rates. In the experiment, they removed the noise spectrum obtained at the peak top from the measurement at the peak slopes. In our case, it is very likely that our tunnel rate is being modified by charge-noise, and we see the consequences in the peak conductivity. Unfortunately, we did not measure the Coulomb peaks in all the region necessary for this analysis.

If we compare our device charge-noise amplitude with that of the state-of-the-art, we see that for other Ge quantum well, the value is $0.6\,\mu\text{eV}/\sqrt{\text{Hz}}$ [127]. For SiMOS devices it is $0.5\,\mu\text{eV}/\sqrt{\text{Hz}}$ [122]. In Si/SiGe heterostructures we find $0.8\,\mu\text{eV}/\sqrt{\text{Hz}}$ [125]. We find $0.5\,\mu\text{eV}/\sqrt{\text{Hz}}$ for GaAs [128]. All state-of-the-art values are below $1\,\mu\text{eV}/\sqrt{\text{Hz}}$, while ours is eight time larger.

The conclusion to this measurement is that the charge-noise in our devices is around eight times larger, but still in the same order of magnitude as the state-of-the-art literature. It should not be an impediment to continue towards spin qubit fabrication. We also conclude that there is still room to improve our measurements.

4.7 Magnetic field spectroscopy

Last characterization we performed in the SQD is the Landé g-factor extraction and the study of the hole spin states under large magnetic fields. In figure 4.16 we observe two method to extract the hole g-factor. The plot in a), taken from the paper [34], show the Subnikov-de Hass (SdH) oscillations. These oscillations are produced when the hole Landau levels exceed the Fermi level due to the Zeeman splitting $E_Z = 1/2g\mu_B|\vec{B}|$, where $|\vec{B}|$ is the magnetic field amplitude, μ_B is the Bohr magneton and g Landé g-factor. From the oscillation periodicity it is possible to extract the hole g-factor. This method is also been used to explore the g-factor asymmetry in strained Ge quantum-well [129]. Another technique for extracting the g-factor is shown in 4.16 b), from the paper of Matthias Brauns et al. [130]. Here we observe the splitting in the SQD excited states with an increasing magnetic field. The difference in energy is directly produced by the Zeeman splitting. In the same paper they also discussed the g-factor asymmetry for holes, but in nanowires instead of quantum-well.

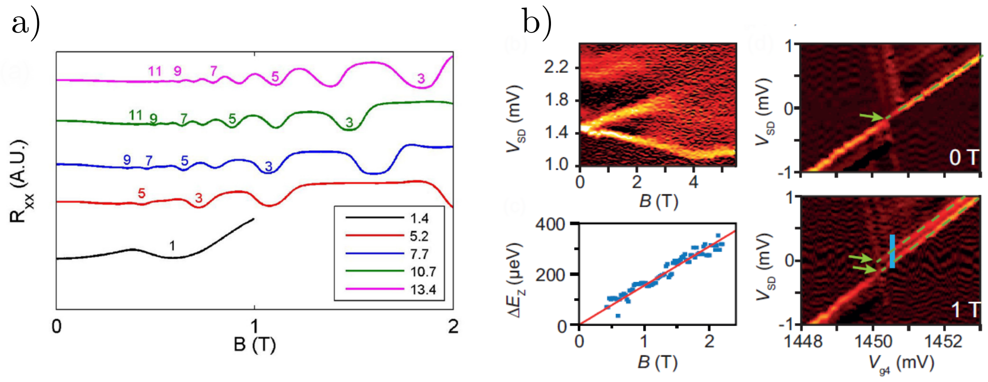


Figure 4.16: Examples of literature experiment where the g-factor for holes was extracted. a) is taken from [34] and b) from [130].

In our experiment, we tried to perform the QD excited states spectroscopy, but we did not achieve enough resolution to clearly differentiate between states. So we had to improvise another method to calculate the g-factor. At the same time, another colleague in the lab was measuring the SdH oscillations, which we will use to compare with the results presented in this thesis.

Our experiment consists in measuring conduction while V_P and a perpendicular magnetic field are swept. Figure 4.17 a) show a color plot with the results. We can appreciate that the Coulomb peaks displace with magnetic field. Image 4.17 b) is a zoom into the first peak. The peaks chemical potential energy displacement is due to the Zeeman energy. The charge state is spin polarize because of the quantum dot orbital level filling. The Zeeman energy is given by the interaction between the hole pseudo-spin $S_Z = 1/2$ and the magnetic field. From the plot, we can extract a g-factor of $g = 9.8 \pm 3$ by fitting the peak drift to the Zeeman splitting. In similar structures as ours (undoped Ge/SiGe heterostructures), there has been reported values from $g = 13$ to $g = 28$ in [34] and $g = 10$ to $g = 12$ in [35]. These values are in accordance with our experiment. Moreover, measurements of the SdH oscillations performed on Hall bar devices revealed values of $g = 9 \pm 2$. The other interesting effect we observe in plot 4.17 a) is the vanishing of the conductance with increment in the magnetic field. That will be discussed in the next figure.

After obtaining the g-factor, we can study the SQD in high magnetic field. Figure 4.18 a) shows a color plot of the conductance changing V_P vs B. We observe that the Coulomb peaks have a diagonal displacement, again produced by the spin-magnetic field interaction. There is also an oscillatory effect. Conductance appears and disappears as magnetic field is increased. We explain this effect

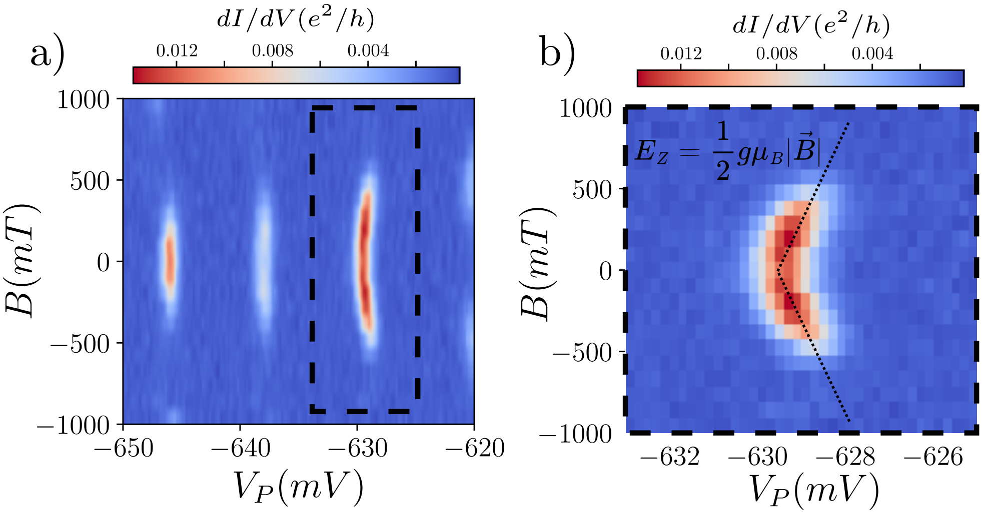


Figure 4.17: Color plots showing Coulomb peaks under perpendicular magnetic field. a) shows three Coulomb peaks in a field from 1 to -1 T. b) is a zoom in the dashed square region from a). There are two dashed lines indicating the peak displacement in magnetic field. The displacement is due to the Zeeman energy of the hole sate in the QD. By fitting $E_Z = 1/2g\mu_B|\vec{B}|$ we extract a g-factor of 9.8 ± 3.

with two main reasons: the spin polarization in the reservoirs and the spin-state displacement caused by the Zeeman interaction.

The framework of our hypothesis is that the 2DHG in the reservoirs is spin-polarized under the external magnetic field. It is known that the tunnel rates can depend upon the carrier spin orientation [131, 132]. If the spin tunnel rate for a given spin orientation is too low, we would not be able to measure it. This is what we think is happening. The tunnel rate for the antiparallel spin orientation with the magnetic field is too low, enough to suppress the conduction through the device.

The dashed lines of figure 4.18 a) indicate the spin state position. The Zeeman splitting produce crossing of antiparallel spin states. In figure 4.18 b) we can see a schematic showing the effect of the magnetic field in the SQD states. Each of the E_N, E_{N+1} level represent a charge state in the SQD. At zero B, these states are spin-degenerate. The degeneration is broken when the dot is under a magnetic field. The state with the spin parallel to the magnetic field decrease its energy with B and the antiparallel-spin state, increase it. At some point, the spin-state cross each other. When this happens, the spin of the fundamental state in the SQD (the last occupied state) changes. We can follow the last state in the dot with the green line in 4.18 b). The quantum dot conductance is through this last state.

Taking both effect into account, we expect to see a change in the conductance of the Coulomb peak caused by the spin-dependent tunnel rate, and we also expect to see a spin-sweep of the last occupied state in the SQD. This is what we observe in figure 4.18 a). In the case of our SQD, the change in tunnel current with the spin is large enough to suppress the current. The crossings we observe in figure 4.18 a) are produced by excited states of the SQD.

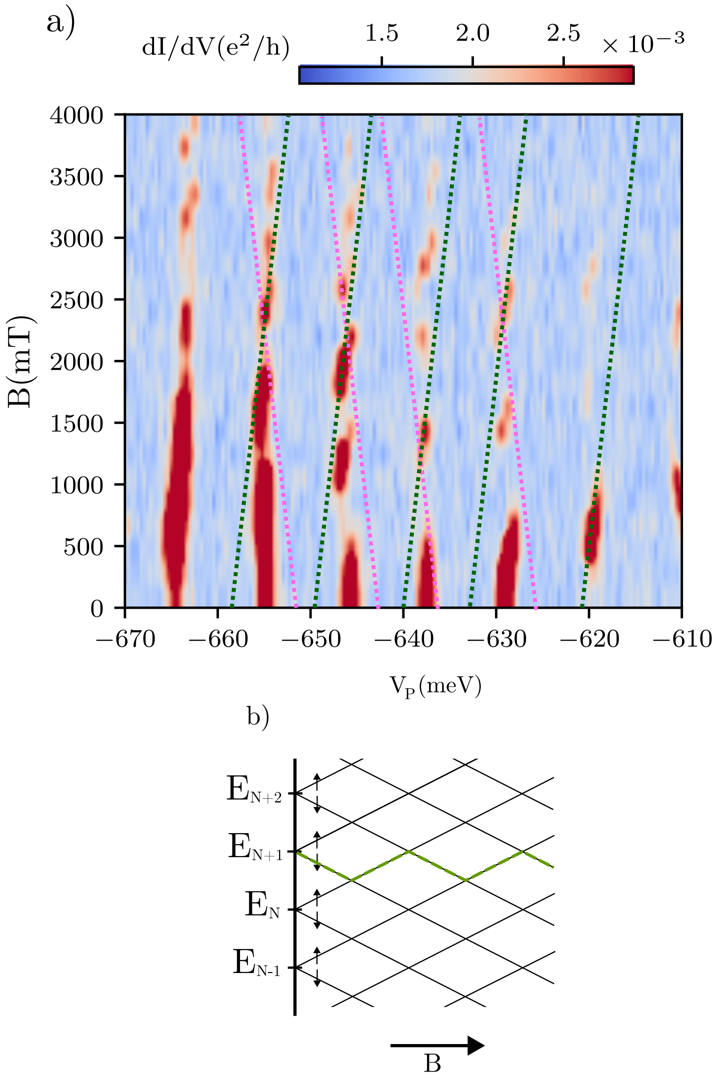


Figure 4.18: a) color plot of the QD conductance with respect to V_P and the perpendicular magnetic field. The two color dashed lines represent the spin state evolution with parallel orientation to the external magnetic field (green) and antiparallel orientation (pink). Both are plotted with the g-factor of 9.8 ± 3. b) schematic of the QD states under magnetic field. The spin state crosses each time that $E_Z = \frac{1}{2}(E_N - E_{N-1})$.

4.8 Conclusions

In this chapter we have studied the viability of our Ge/SiGe heterostructures to form a SQD. All the experiments were done measuring electronic transport in a 300 mK condensation cryostate, **HelioxVT** from **Oxford**.

At the beginning of the chapter, we discussed a reliable method to find Coulomb blockade and Coulomb oscillations. We also studied the barrier gate space and describe a technique to symmetrize the tunnel rates $\Gamma_{BB} \approx \Gamma_{BT}$. The symmetric points enhance the SQD conductance. A virtual gate was defined with the two barrier gates. We discussed the methodology to create a second virtual gate with the plunger gate and the two barrier gates.

Once the tunnel barrier are symmetric and the SQD is in the Coulomb blockade regime, we studied the Coulomb diamonds and extracted some figures of merit. The values we found are $\mathrm{E_C} = 1\ 2\mathrm{meV}$ and $\alpha = 0.176 eV/V$. Some QD excited states were resolved in the Coulomb diamonds with an excited energy around $\Delta \mathrm{E} = 275\mu\mathrm{eV}$. These results indicate a SQD of around $140 \pm 20\mathrm{nm}$ diameter, in accordance with a parallel plate capacitor model, with a strong lever arm (typical values for dots are between 0.05-0.1 eV/V).

The next experiment discussed was the charge-noise measurement. We recorded the current noise over time in a Coulomb peak and transform it into a power spectrum. At 1 Hz, we found a power amplitude average of $\mathrm{S}_\mu^{1/2}(1\mathrm{Hz}) = 8.3 \pm 2\mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$. It is one order of magnitude larger that those in the state-of-the-art.

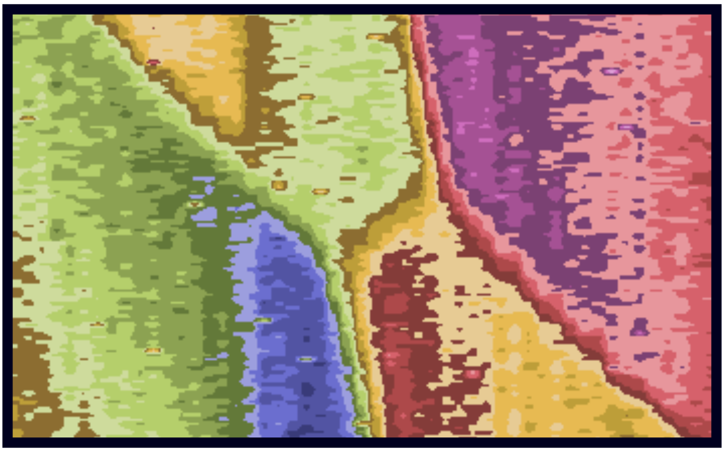
Last chapter section is focus on the spin spectroscopy under magnetic field. We extract the out-of-plane g-factor $\mathrm{g} = 9.8 \pm 3$. It is in accordance with SdH oscillations in the same heterostructure Hall bar devices. We also observed some spin-state crossing at large magnetic field and deduce that the reservoir are spin-polarized. The combination of spin polarized reservoirs and the Zeeman splitting of the spin states produced the conductance oscillations we measured.

In conclusion, we are able to form a SQD and measure some figures of merits. This was the objective propose in this chapter. We can claim that our fabrication method from chapter 2 is proper to the hole SQD formation. The probe of spin polarization is another good news towards the hole spin qubit fabrication.

Even more, having QD opens a good amount of choices for other experiments. We could start improving the SQD design. Shorter barrier gates would imply more control on the tunnel rate and make it possible to enter the regime $h\Gamma \ll k_B T$. We could also implement a charge sensor in the vicinity of the SQD and measure in charge sensing. This technique allows the possibility of reaching the few-holes regime for the QD. This regime is very interesting for studying the orbital filling of the dot [18]. We could also consider measuring Kondo effect in QD. It is being found in GaAs [20] but not in strained Ge quantum-well. Using the spin to charge conversion [133] we have access to spin state of the dot and observe singlet-triplet states [66, 134]. Another path to follow would be the addition of a second QD close enough to have tunnel coupling, as J. M. Elzerman et al. did for first time in planar structures [135]. This is what we decided to do.

Chapter 5

Double Quantum dot



In this final chapter we present the characterization of a double quantum dot device. Measurements were taken in a dilution fridge at a base temperature of 7 mK. The first section is focus on the set-up description. Just after, we will present the sample design and the measurement techniques. In the first half of the chapter the DC current measurements are presented. We will discuss on the process followed to achieve Coulomb blockade in a DQD as well as the barrier gate's tunnel rates symmetrization. Next section is about the interdot gate between dots. We show that the voltage applied to the interdot gate is able to change the device from a big single QD to a double quantum dot with a weak interdot tunnel rate. The last features observed in DC are the bias triangles and the transport through QD excited states. The second half of the chapter shows a discussion on how to tune a proximal charge-sensor for read-out. In the final section, we will present a stability diagram showing our system in the last hole regime.

Creative representation of an interdot coupling.

5.1 Set-up

The DQD measurements were done in a commercial **BlueFors** fridge. It is a dilution fridge that reach 7 mK at base temperature, a schematic can be found in figure 5.1. The fridge is equipped with 24 DC lines. For sample characterization, we measured the DC current with two I/V converter with $1:10^8$ amplification. We used two DMM to record the voltage produced by tho tow I/V converters. Sample design will be explained in the next section. For gating the device, we used a low-noise DAC with a precision of 21 bits with a voltage range of ±1.2V.

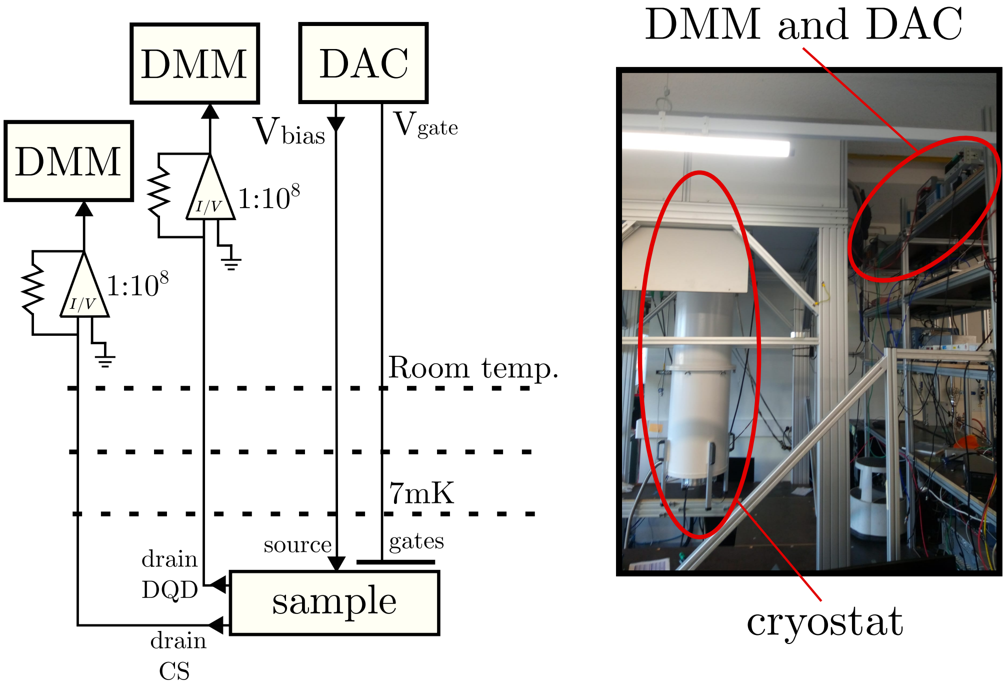


Figure 5.1: In the left, it is represented a schematic of the set-up circuit. In the right, a cryostate's picture taken in the laboratory.

5.2 Device description

The DQD device, same as the SQD design seen in previous chapter, is though to be functional in accumulation and depletion regimes. It is built with a double gate layer stack. The main device's features are the two quantum dots, tunnel-coupled with each other, and a third charge-sensor quantum dot capacitively coupled to the other two. The plunger gates associated to each chemical potential are G1 and G2 for dots 1 and 2, and CP for the charge-sensor. To control the

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coupling with the different leads, there are several tunnel barriers and depletion gates. An SEM image can be seen in figure 5.2. In red color we have the first gate layer and in blue, the second gate layer. The two gates with a circular ending in the top are the accumulation gates for dots 1 (G1) and 2 (G2). Around them, we see the barrier gates (B2 and B1) and the depletion gates (D2 and D1). Between the dots there is the interdot barrier gate (BT). The charge-sensor circuit is located at the bottom. It consists in another quantum dot with a plunger gate (CP), its own depletion gates (DC) and the two barriers connected to the ohmic accumulation gates (CBL and CBR).

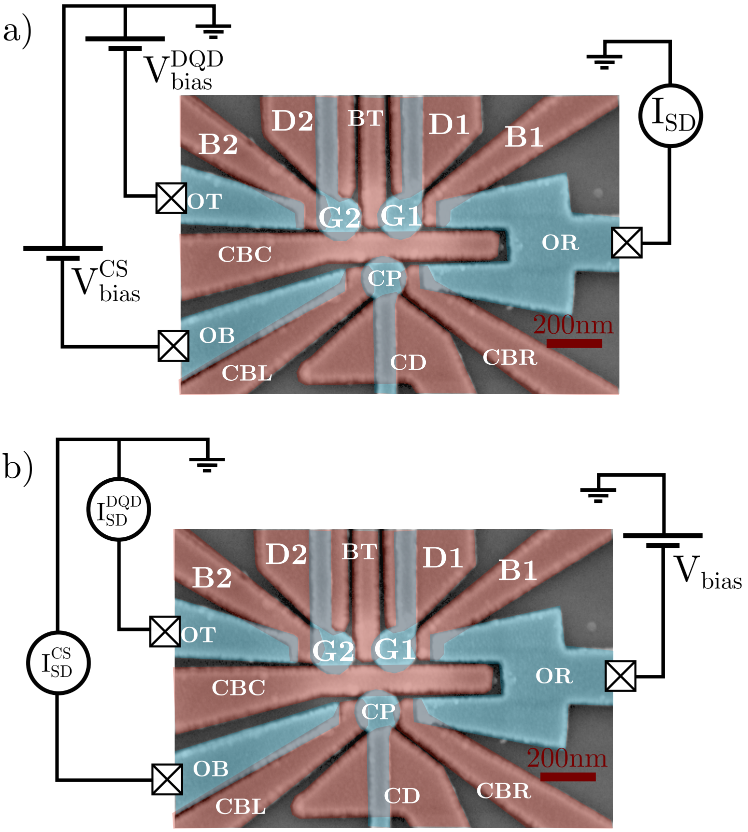

Figure 5.2: SEM picture of the DQD device. Red color gates are the first gate layer and blue color gates are the second. a) shows the configuration for the charge sensing read-out. b) shows the configuration for the DC current measurements.

There are three ohmic contact in the device. The idea is to be able to independently measure current through the DQD and the charge-sensor. The position of source and drain will vary along the chapter.

In the first half of the chapter, the circuit design is the one presented in 5.2 b) We had one bias voltage applied to the right ohmic (V_{bias}) and two DMM recording current through the charge-sensor ($I_{\text{SD}}^{\text{CS}}$) and the DQD ($I_{\text{SD}}^{\text{DQD}}$). For the second half, we measure current only through the charge-sensor. In that case, the sample circuit is in figure 5.2 a). The current is measured through the righ ohmic contact ($\mathrm{I_{SD}}$). The device can be biased at the charge-sensor lead ($\mathrm{V_{bias}^{CS}}$), and at the DQD lead ($\mathrm{V_{bias}^{DQD}}$).

5.3 Tuning the DQD into Coulomb blockade regime

For the DQD device tuning, we followed the same process as for the SQD, discussed in section 4.3. First, we test all the gates to see that there is not gate leakage in the sample. Once this is checked, we accumulate carriers with the plunger gates until we observe current. After this, we proceed to form QPC with all the gates. Once this is achieved, we look for Coulomb oscillations in both dots. We can look back to the theory section 1.2.4 and observe the system's capacitances: C_m between dots and $C_{1,2}$ between each plunger gate and its dot. At this point, the system could be in a high-coupled regime ($C_m \approx C_{1,2}$) or a low-coupled one ($C_m \ll C_{1,2}$). For barrier optimization, we found it better to let the system in a high-coupled regime, where the double dots behave as a single big dot.

The device shown in this chapter turns out to work in a depletion regime. There were carriers in the quantum well at zero gate voltage, so we skipped the first step of carrier accumulation and jumped directly to the QPC formation. The system's circuit is shown in figure 5.2 b).

5.3.1 QPC with barrier and depletion gates

The QPC test, same as in previous chapter, consist in forming a QPC with each barrier and depletion gate. It is done independently for every gate. Here we focus on the double dot gates and let the charge-sensor aside.

Results for the QPC test are in figure 5.3 a) (barrier gates) and figure 5.3 (depletion gates). In figure 5.3 c) there is a colored SEM picture of the device with the sample's QPC. In plot a), we observe that the saturation current for the three QPC is at similar amplitude, $\mathrm{I_{SD}^{DQD}} \sim 500\mathrm{nA}$. We see a difference in the pinch-off voltage. For $\mathrm{V_{BT}}$ and $\mathrm{V_{B1}}$ is $\mathrm{V_{B1,BT}} \sim 225\mathrm{mV}$, but for $\mathrm{V_{B2}}$ it is $\mathrm{V_{B2}} \sim 150\mathrm{mV}$. This difference can be attributed to some lithography difference in the gate shape. Also, we can think that the influence of CBC is bigger at B2 than at the other gates. We can also observe that there is an oscillation below B1 just before pinch-off. It can be caused by disorder below the gate that form a high-coupled quantum dot.

In figure 5.3 b) we see the response of the system when we sweep the two depletion gates. Current pinch-off is not reached, but we clearly see a linear response of the current as the voltage is increased. This is enough to probe their influence on the 2DHG density. For these gates, the conduction channel is wider than for the plunger gates. Nevertheless, the trend is that at higher voltage it would close.

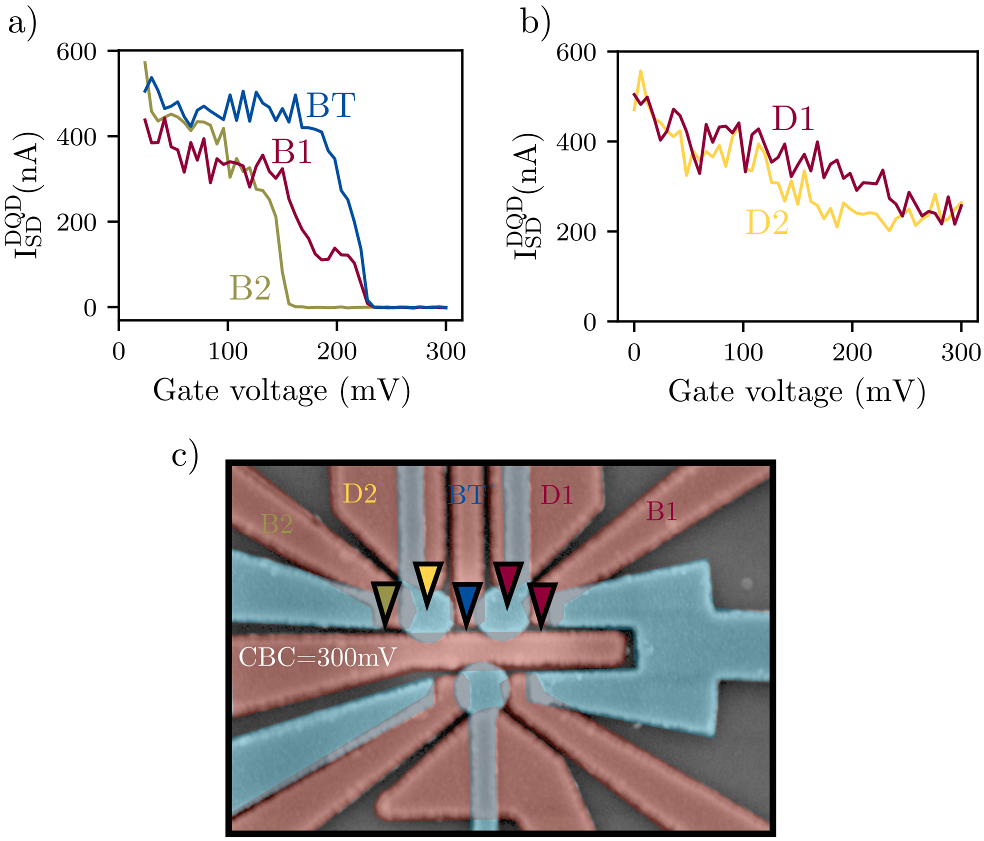

Figure 5.3: QPC test for the barrier and depletion gates. The objective is to see the 2DHG response for each of the gate swept independently. Bias voltage is $V_{bias} = 1mV$. a) shows the source-drain current vs gate voltage for the barrier gates. All of them are able to close the conductance channel. b) shows the results for the two depletion gates. In c) we can see a colored SEM image of the device with some marks indicating each of the QPC formed from the plots above. The gates for the charge-sensor circuit (in the bottom of the device) are all at 200 mV except CBC, which is at 300 mV. With this configuration, we were sure that the current was flowing to the DQD ohmic lead.

Once we are sure that the sample can reach the quantum transport regime, and we have an idea of the pinch-off voltages, we can proceed to the next step. Studying the barrier gate space and search for Coulomb oscillations.

5.3.2 Barrier and plunger gates

In this section we will discuss the barrier optimization. The way to proceed is the same as in the previous chapter, section 4.4. We look for symmetric tunnel rates to enhance the transport signal. Instead of explaining all the steps again, we will directly jump to the barrier vs barrier plot. Figure 5.4 a) shows the current through the DQD versus barrier gates. For this configuration, the depletion gates are high enough to deplete the 2DHG below the plunger gate's arm. We observe in the voltage window that B2 is fully close above $\mathrm{V}_{\mathrm{B2}} > 140\mathrm{mV}$ and B1 above $\mathrm{V}_{\mathrm{B1}} > 220\mathrm{mV}$. For the next plot, we stay in the figure a) star value for the barrier gates.

In the plots in figure 5.4 b) and figure 5.4 c), we start to explore the plunger vs plunger gate space. Figure 5.4 b) shows a broad map and c) a zoom into few mV. The transversal oscillations are the DQD Coulomb oscillations in a high interdot coupling regime. The system behaves as a big single quantum dot whose chemical potential is tuned by the two plunger gates. It is understood since the interdot barrier gate is at 0V. In plot b), there is a region in the bottom left that shows a higher conductance. We assume this is caused by disorder in the sample heterostructure, or by a change in the tunnel barrier to the leads, caused by the gate cross-talk. It totally banishes as we approach the upper right part of the graph, the region we are interested in.

The final plot in figure 5.4 d) shows the Coulomb oscillation of the big single dot but only sweeping V_{G1}. This plot is very similar to those of a SQD. At voltage below $\mathrm{V}_{\mathrm{G1}} < -130\mathrm{mV}$, the Coulomb peaks start to merge with each other. In the middle region $-130\mathrm{mV} < \mathrm{V}_{\mathrm{G1}} < -75\mathrm{mV}$, it seems that Coulomb blockade is achieve between oscillations. We see the total absence of current above $\mathrm{V}_{\mathrm{G1}} > -75\mathrm{mV}$.

After this section, we already know the configuration for the gates to enter the Coulomb blockade regime. The next step is testing the interdot barrier gate and see if we can drive the system from a big single quantum dot into two separated double dots.

5.4 Tunneling barrier

In this section we will study the interdot barrier gate (V_{BT}). This gate tunes two coupling mechanisms: the capacitively coupling between dots and the tunnel coupling between holes in each dot. A high electric potential between dots would push the hole's wavefunction apart, increasing their distance. On the other hand, a low potential would bring them together. The dots' distance is directly related with the two coupling phenomena. Tunnel coupling is a pure quantum effect, it

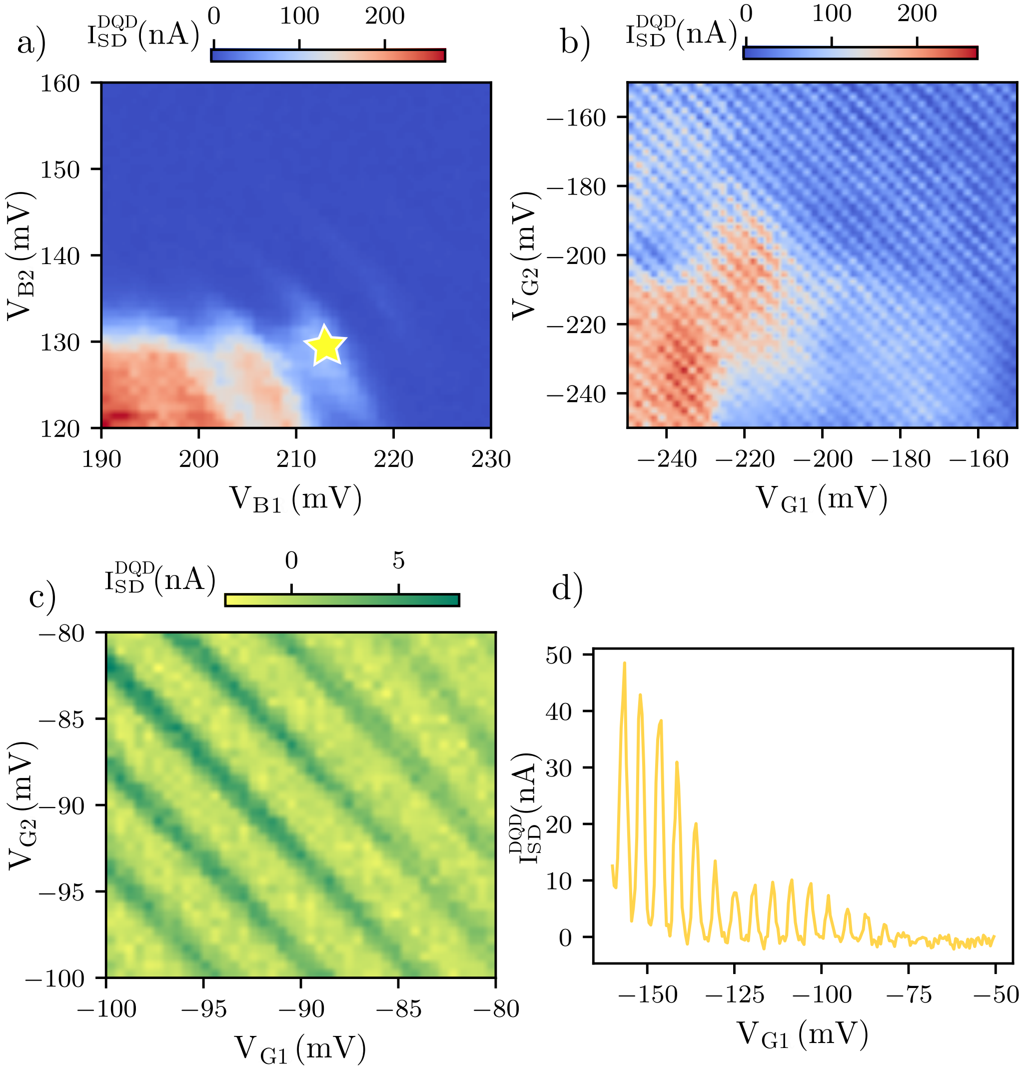

Figure 5.4: Color plots of the process to achieve the Coulomb blockade regime. Bias voltage is $V_{bias} = 0.2$mV. a) shows barrier vs barrier. We observe the typical traces, similar to the SQD. Plunger voltages in this plot are $V_{G2,G1} = -200$mV and depletion voltages $V_{D2,D1} = 440$mV. In the next plots, the system is at the star barrier voltage values $V_{B1} = 213$mV and $V_{B2} = 128$mV. b) and c) are plots exploring the plunger vs plunger gate space. b) has a broader range and c) is a zoom into a smaller region. The transversal oscillation observed are the Coulomb peaks of a big single quantum dot below both plunger gates. d) is a plot of the Coulomb oscillation by sweeping only one of the plunger, V_{G1}.

exponentially depends on the distance. The capacitively coupling is a classical effect, its relation with the distance is linear.

In this experiment we will observe the transition from a single dot to a double

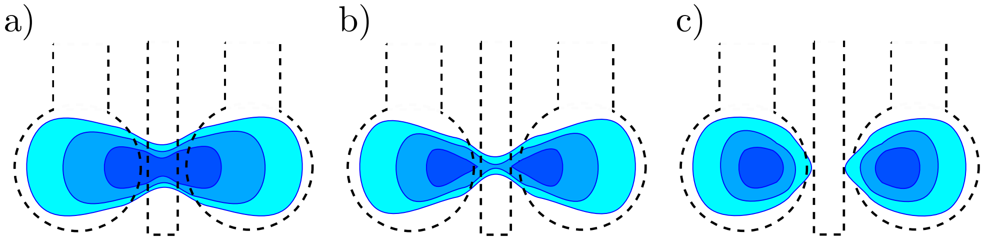

Figure 5.5: Schematic of the DQD device for different tunnel barrier gate voltages. We can see the transition from a big single quantum dot (a) to a two separated quantum dots (c). The middle regime is represented in (b).

dot. A schematic of the system's evolution is represented in figure 5.5. In a), the hole wavefunction is extended below both plunger gates. It forms a unique quantum dot. In b) we start to localize the holes below both plunger gates. In c), the two dots are totally separated.

We will measure current through the DQD in the Coulomb blockade regime while we sweep both plunger gates. In figure 5.6 there are four color plots with four different voltage in the interdot barrier gate. The four plots are measured in the same range for the plunger gates. We can observe the system's evolution from a single dot to two dots, same than in schematic from figure 5.5. Plot a) shows the behavior of a single dot whose chemical potential is controlled by the two plunger gates, sames as in figure 5.4 c). In b), we start to see that the diagonal lines bend. The dot wavefuntion start to localize below each plunger gate. In c), a honey comb pattern raises. Now we can clearly distinguish each charge state. The cotunneling through the interdot barrier make the charge addition lines visible for both dots. In d) we see the typical plot for a DQD measure in current. There is conductance through the device when the dot's electrochemical potentials are aligned, and they are also align with the reservoirs.

With these results we can conclude that the interdot barrier gate controls the capacitance coupling between dots. We can shape the system from a single dot to a double dot, with all the intermediate regimes. The tunneling control on a DQD is a key element in order to do two qubit gate based on exchange interaction, or to do a single-triplet spin qubit.

5.5 Bias triangles and transport measurements

In this section we will discuss the measurements of bias triangles. We can see in figure 5.7 two examples from bibliography. In the left panels we see a differential conductance measurement with honey combs patterned on top. The device consisted in a carbon nanotube controlled with two plunger gate electrodes and a back gate. In this paper they demonstrated interdot tunneling tuning, and

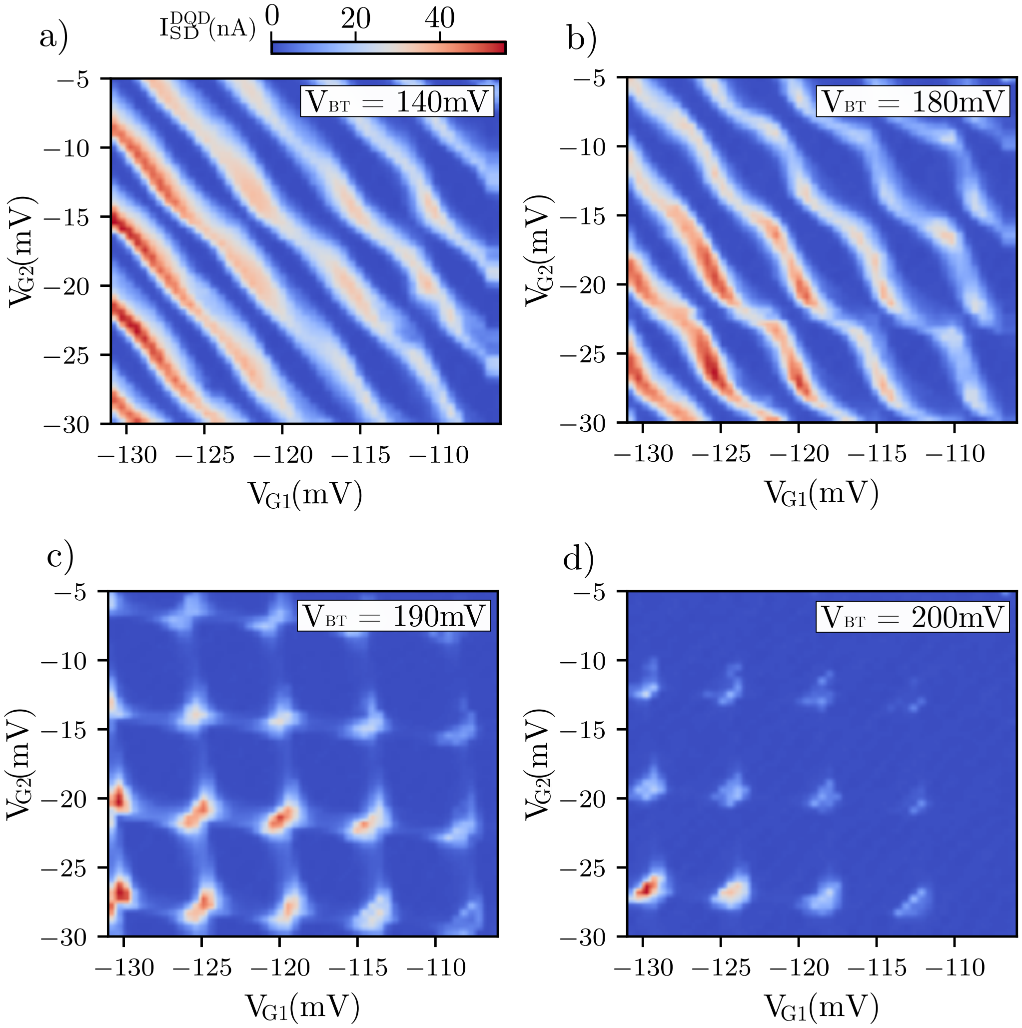

Figure 5.6: Color-plots showing the transition from a single dot to a double dot measured in current. We observe source-drain current sweeping V_{G2} versus V_{G1}. Bias voltage for the four plots is $V_{bias} = 0.4$mV. Barrier and depletion voltages are the same as in figure 5.4.

they show control over the ohmic lead transparency. From the honey combs in transport, it is impossible to distinguish between capacitively coupling and tunnel coupling, but we can define the ratio between them. It is known as fractional splitting ratio $f = 2\Delta V_S/V_P$ [136] (in the bottom left panel of figure 5.7 there are the voltage definitions). They observed from $f \sim 0.3$ up to $f \sim 0.7$. In the right panel we see some bias triangles measured in SiMOS gate defined DQD. This was the first experiment of Si DQD at 50mK. The splitting ratio in this case is $f \sim 0.2$. They even observed some excited states across the bias triangles.

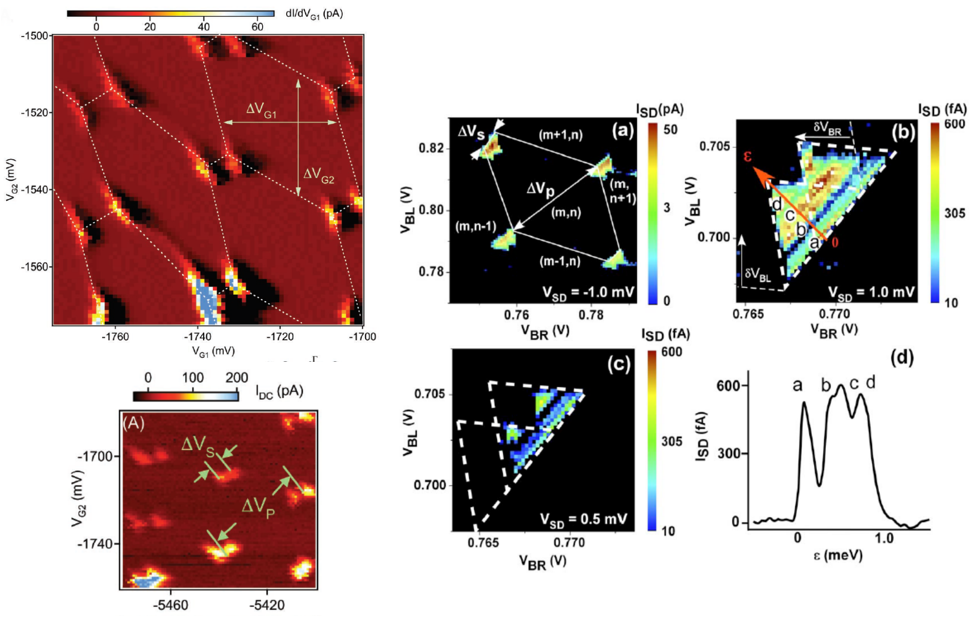

Figure 5.7: Left panel is taken from [137]. They measured DQD in carbon nanowire. From this experiment we can extract the system capacitance. This method was discussed in the theory section 1.2.4. Right panels are taken from [22]. They measured in SiMOS DQD. In this case, they also extracted the system capacitance and were even able to observe excited states through the bias triangles.

In our case, we will start by analyzing the system capacitance from the honey comb patterns. Figure 5.8 shows the honey comb lattice drawn over the bias triangles previously presented in figure 5.6 d).

We can use equations 1.56 and obtain each gate capacitance. They are equal to $C_{G1} \sim 27$aF and $C_{G2} \sim 22$aF. We can also calculate the splitting ratio between tunnel rate and coupling capacitance, it is $f \sim 0.3$. This value means that the capacitance coupling dominates. In order to extract the dot coupling $\mathrm{C_m}$ and the charging energies, we have to measure the bias triangles.

In figure 5.9, a) shows a zoom into a triangle pair from figure 5.8. We see current versus both plunger gates and a guide to the eye to reconstruct the triangles. Two triangles are observed which overlap each other. From this plot we can extract the lever arm for each plunger gate α_1, α_2. With the level arm we have access to the charging energies and to the interdot coupling.

To extract the level arm, we use that the applied bias voltage gives the boundaries for conduction through the DQD. The horizontal projection of the triangle gives a voltage difference of $\Delta \mathrm{V_{G1}} \sim 2.1$meV and the vertical projection $\Delta \mathrm{V_{G2}} \sim 1.7$meV. From these two values and the bias voltage $\mathrm{V_{bias}} = 0.4$meV, we calculate that both lever arms are $\alpha_1 = 0.19$eV/V and $\alpha_2 = 0.24$eV/V. The lever arm is the ratio between the gate capacitance and the total dot capacitance, we can say that $\alpha_1 = C_{G1}/C_1$ and the equivalent for dot 2. With this relation, we

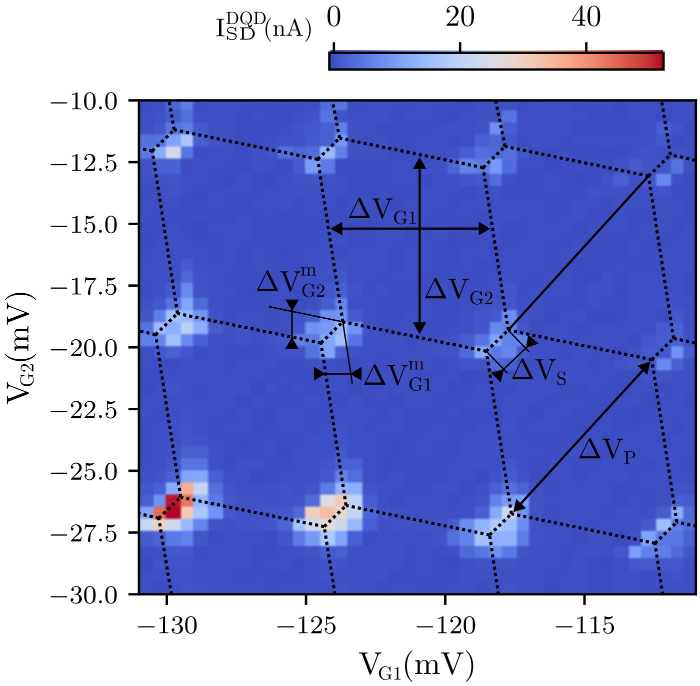

Figure 5.8: Color plot of the source-drain current by sweeping the two plunger gates V_{G1} and V_{G2}. Bias voltage is $V_{bias} = 0.4$mV and the interdot barrier gate is at $V_{BT} = 205$mV. We observe the patterned honey combs joining the different bias triangles. From the plot, the voltage values are $\Delta V_{G1} = 5.9$mV, $\Delta V_{G2} = 7.3$mV, $\Delta V_{G1}^{m} = 0.88$mV and $\Delta V_{G2}^{m} = 0.98$mV. We also measure $\Delta V_P = 8.1$mV and $\Delta V_S = 1.3$mV.

use equations 1.57 and 1.58 to write that

$$C_m = \frac{\Delta V_{G1}^{m}|e|}{\Delta V_{G1}\Delta V_{G2}\alpha_2} = \frac{\Delta V_{G2}^{m}|e|}{\Delta V_{G1}\Delta V_{G2}\alpha_1}. \tag{5.1}$$

We obtain that $C_m \sim 13$aF. The respective charging energies are $E_{C1} \sim 1.1$meV and $E_{C2} \sim 1.8$meV. The last factor we will extract is the interaction energy, equal to $E_{Cm} \sim 162\mu$eV.

In figure 5.9 b) we see two peaks corresponding to the ground and excited state of the QD. The clear distinction of the peaks indicate that the thermal and the tunnel rate broadening are smaller than the excited state energy $h\Gamma, k_BT < \Delta E$. The energy difference of the first excited state transition is $\Delta E \approx 190\mu$eV. This value is in the same order as the one obtained in the previous chapter for a SQD $\Delta E_{SQD} = 275\mu$eV. Without further analysis we cannot tell through which excited states conductance is happening. Between the peaks, the current does not drop to zero. The tail overlapping is a signature that the tunneling rate of some the DQD are similar to temperature, and we observe elastic cotunneling.

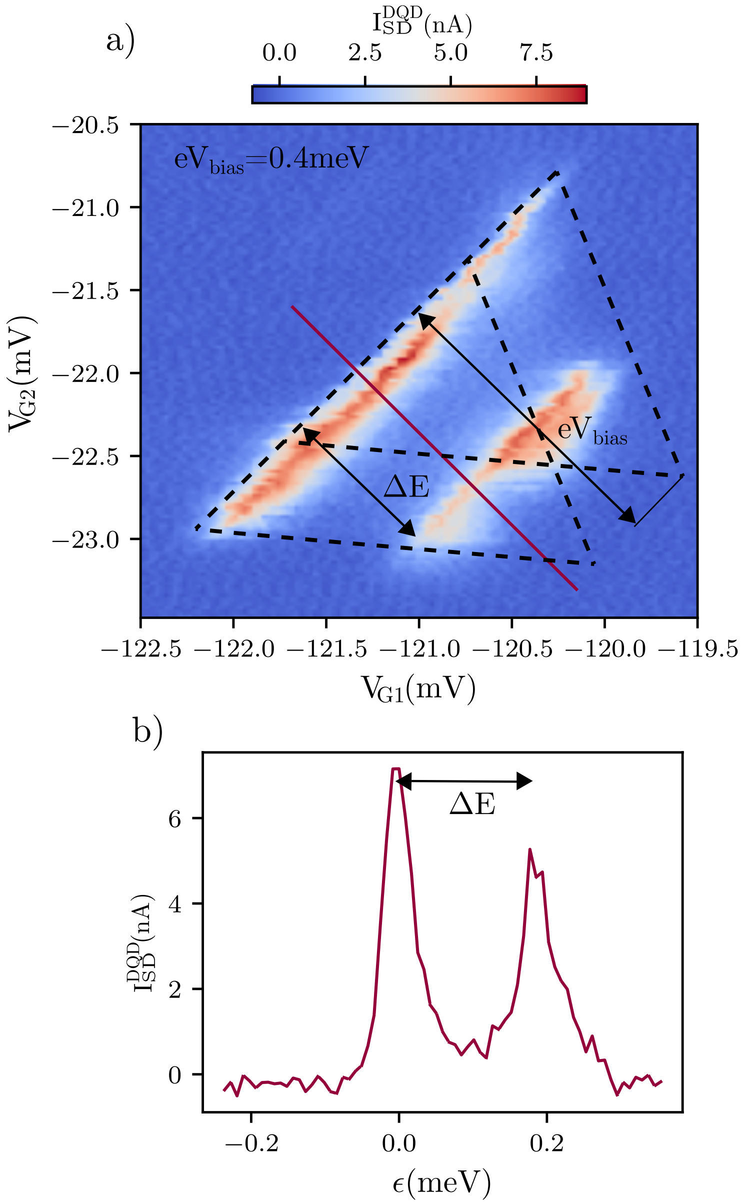

Figure 5.9: a) Color plot of two bias triangles in the DQD. We see the two plunger gates being swept in both axis. The dashed lines indicate the lines for the two bias triangles presented in the measurement. The triangle base feature is the conductance signal through the two ground states in the DQD, while the shorter feature is the conductance through some excited state. From the plot, we can recover the bias voltage $eV_{bias} = 0.4$meV weighed by the lever arm. Lever arms are $\alpha_1 = 0.19$eV/V and $\alpha_2 = 0.24$eV/V. b) shows a plot of current versus detuning along the maroon line in plot a).

5.6 DQD in charge sensor

The original idea was to use the bottom QD (CP) as the charge-sensor, but eventually we moved to the QPC formed with CBR.

5.6.1 QD as charge-sensor

The first step is tuning the charge-sensor QD in the Coulomb blockade regime. For this purpose, we let the DQD gates in the same configuration than for the bias triangles. Then, we looked for the Coulomb peaks in the charge-sensor QD same way as in chapter 4. Figure 5.10 shows the Coulomb peaks of the charge-sensor QD.

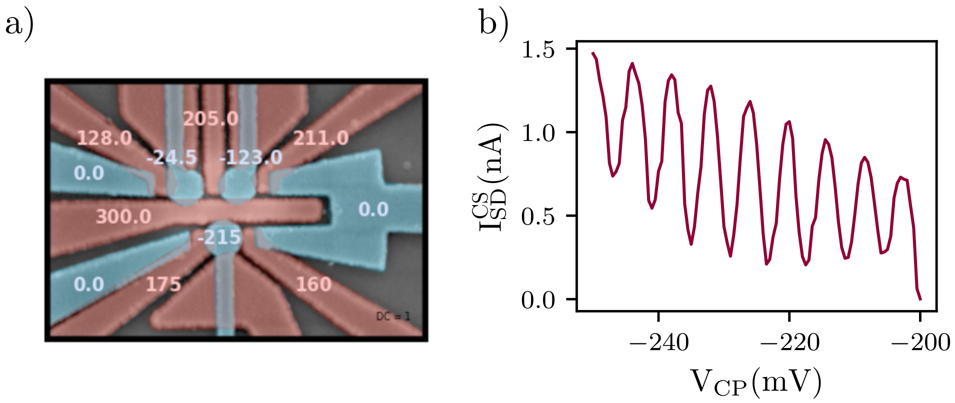

Figure 5.10: Coulomb peaks in the charge-sensor QD. a) shows a colored SEM image of the DQD device with the gate voltages. b) shows current versus charge-sensor QD's plunger gate (V_{CP}). We observe Coulomb oscillations in the open barrier regime. For the purpose of the charge-sensor, this regime is fine. The bias voltage applied was $V_{bias} = 1$mV.

Once the Coulomb oscillations are found, we start sweeping the DQD plunger gates while measuring the current through the charge-sensor. What we expect to see are some step's displacement in the current amplitude, as it was discussed in the theory section 1.2.5.

The system circuit for this measurement is with two DMM, represented in figure 5.2 b). This way we can measure the current through the DQD and the charge-sensor at the same time. Results of the experiment are in figure 5.11. We swept both DQD plunger gates V_{G1} and V_{G2} towards more positive values. At some point, the DC current through the dots banishes. However, with the charge-sensor we are still able to recover the charge transition signal, meaning that holes are tunneling into the DQD.

At this point, we decided to change our QD charge-sensor to the QPC formed with the gate CBR, mainly because the QPC has not the same distance to both quantum dots in the DQD. It is closer to dot 1, so in principle it would be easier

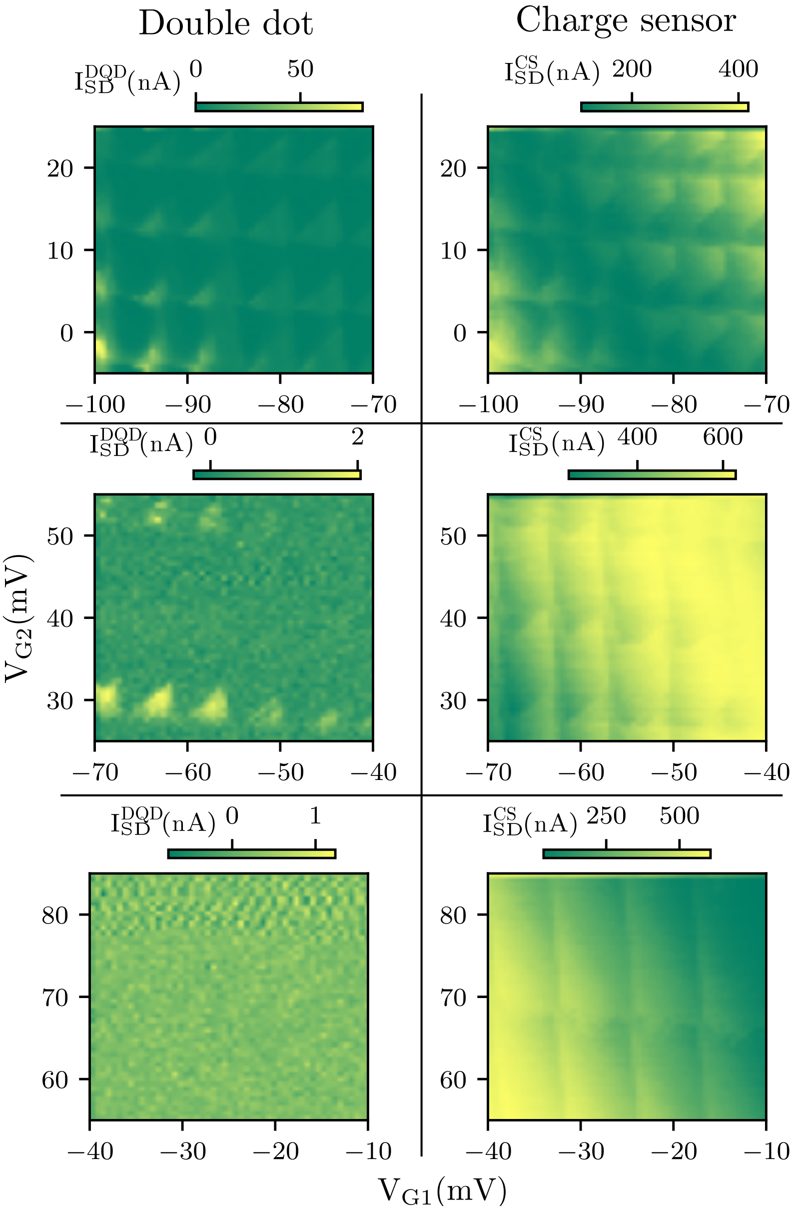

Figure 5.11: Color plot showing DC current through the DQD (left) and the charge-sensor current (right). We swept the DQD plunger gates while measuring both currents at the same time. We can directly have a comparison between both techniques. As the DQD plunger gate voltages increase (the dot is being emptied), the DC signal start to vanish and the bias triangles are no longer visible. On the other hand, the charge sensor technique still shows some charge transition lines with the typical honey comb pattern. Voltage bias was $V_{bias} = 1$mV

to discriminate when a charge is loaded in each dot. The next section will talk about the QPC charge sensor optimization.

5.6.2 QPC as charge sensor

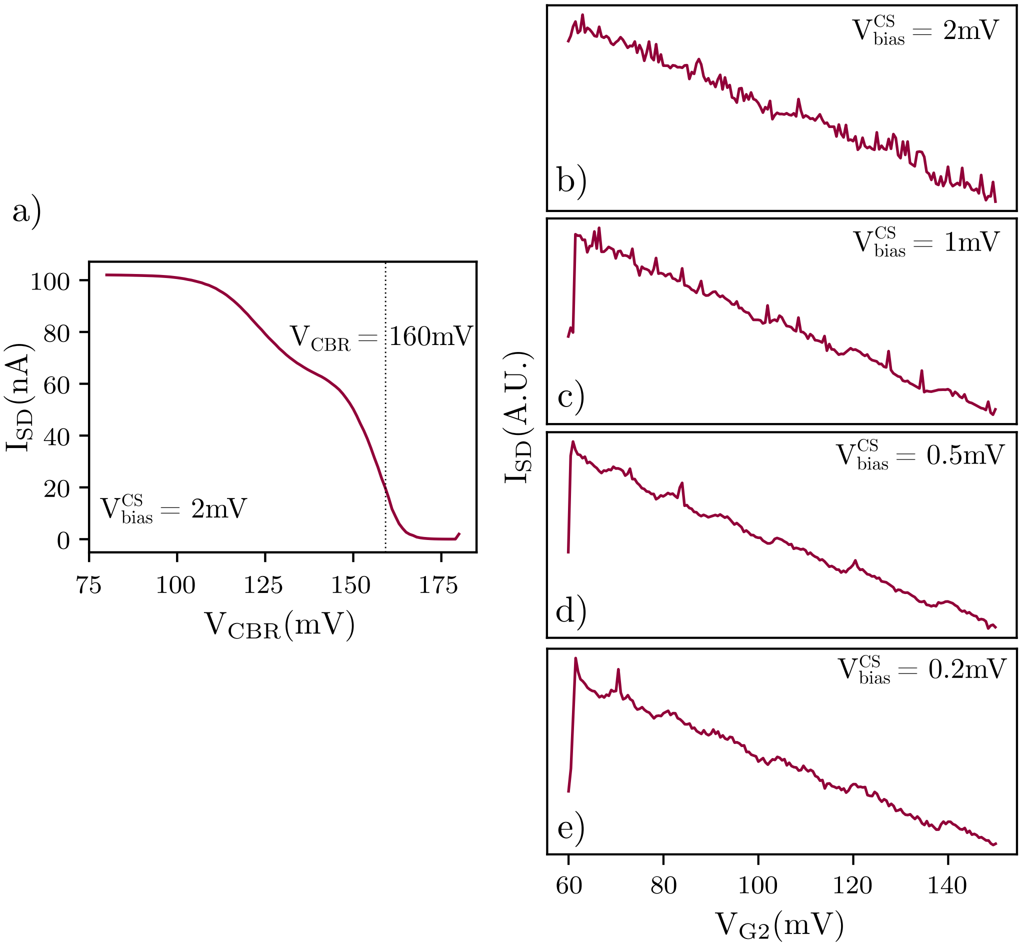

Figure 5.12: QPC as charge sensor. In a) we see the QPC current I_{SD} produced by sweeping V_{CBR}. The chosen amplitude to record the charge loading in the DQD was $V_{CBR} = 160$mV. In b), c), d) and e) we see four plots of the QPC current while sweeping the dot 2 plunger gate V_{G2} at different bias voltage V^{CS}_{bias}. We can observe the noise evolution with bias. The step resolution also changes with the bias voltage.

From now on, the system is biased at the QPC ohmic contact. The DQD ohmic is connected to ground. The system's circuit is shown in figure 5.2 a). The first thing we did was observe the QPC formed by CBR. Same as before, we let the DQD charged with some holes and swept V_{CBR}. Results can be seen in figure 5.12 a). We set $V_{CBR} = 160$mV and sweep the plunger gates. At the right, we observe the QPC curve while sweeping one of the plunger. We can clearly observe the steps in current each time a hole is loaded or unloaded from the quantum dot.

In order to optimize the QPC resolution, we studied the system's response at different bias. Results of this experiment is in figure 5.12 b), c), d) and e).

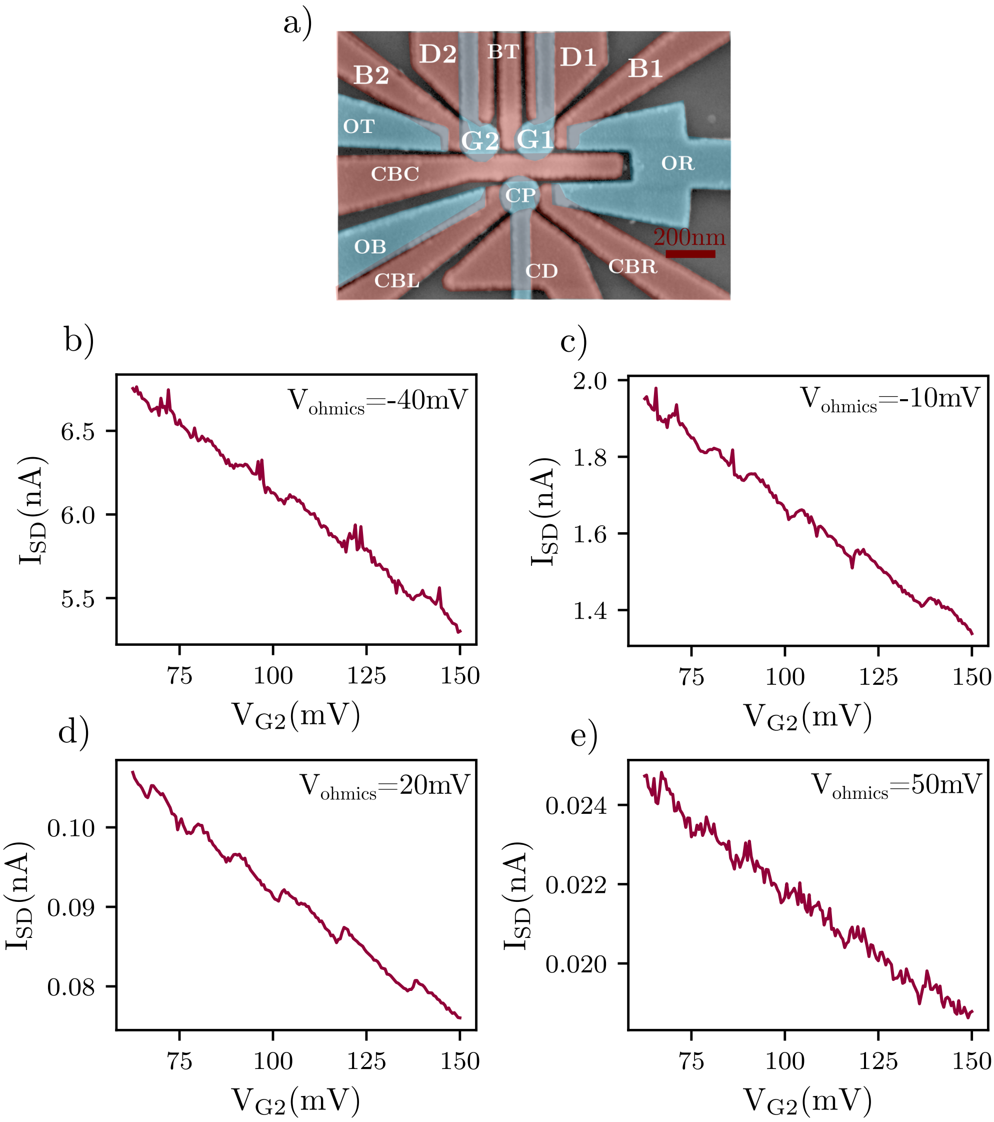

Figure 5.13: Charge sensor measurements at different ohmic accumulation values. In a) there is a colored SEM image. In the bottom figures, what is called V_{ohmics} are the gates $V_{\text{OR}}, V_{\text{OT}}$ and V_{OB}.

The slope presented in all plots is due to the cross-talk between the QPC and the plunger gate V_{G2}. At $V_{\text{bias}}^{\text{CS}} = 2$mV, the charge steps are quite smooth and almost indistinguishable from noise. When we reduce the bias to $V_{\text{bias}}^{\text{CS}} = 1$mV, the steps start to be better resolved and the noise peaks decrease. The curve looks even better when $V_{\text{bias}}^{\text{CS}} = 0.5$mV. Each charge state is clear. We tried to push a bit more and measure at $V_{\text{bias}}^{\text{CS}} = 0.2$mV. In this stage, the resolution does not get better, and neither the noise. We can clearly see a trend in noise level with the bias voltage. Increase the bias window increases the noise. This may be produced by unwanted charge states close to the Fermi level. Finally, we decided that the best bias to measure was $V_{\text{bias}}^{\text{CS}} = 0.5\text{mV}$.

The last optimization we performed on the QPC sensitivity was modifying the ohmic gate accumulation. We performed the QPC current measurement sweeping V_{G1} at different accumulation values in V_{OR}, V_{OT} and V_{OB}. We ranged from $-50\,\text{mV}$ up to $50\,\text{mV}$ in steps of $10\,\text{mV}$. In figure 5.13 we present a selection of four plots. Among the plots, b) and c) are quite similar. In both of them we can distinguish the charge loading step with some noise peaks. The plot d) has the lowest noise and the biggest contrast to locate the charge loading. Finally, e) steps are the worse resolved and noise level is the highest. The total current amplitude also changes with the ohmic accumulation. We observe the largest current amplitude in the most accumulated regime, and it decreases as the 2DHG is depleted. We believe this effect is caused by two phenomena. The first is that the hole density in the reservoirs is reduced, so the sheet resistivity increase. The second one, may be less relevant, is that the cross-talk between gates modify the tunnel rate between the charge-sensor QD and the reservoirs. We decided that the $20\,\text{mV}$ at the ohmic accumulation gates gave the best results for charge sensing.

5.7 Charge stability diagram

The last experiment we performed is the charge stability diagram. We manage to empty both dots.

In figure 5.14 there are some charge diagram examples. In all the cases, the (0,0) charge region is reached. Once the system is in this region, just by counting the charge lines we know the total number of carriers in each QD. For all the experiment, they used charge sensing to measure the DQD, but with small differences in the methodology. In figure 5.14 a), the current through the charge-sensor is kept constant. Every time that there is a charge addition in the dots, the change in the electrostatic environment affects the current in the charge-sensor. The magnitude plotted is the compensation current ΔI applied to recover the original current. In figure 5.14 b) and figure 5.14 c), the charge-sensor is a QPC. They plotted the derivate of the QPC conductance. Finally, last plot in figure 5.14 d), the stability diagram is measured with a SQD as charge-sensor. They used reflectometry in the SQD's ohmic lead. This technique allows measuring faster than in DC current. In this last example, the DQD had holes as carriers, and that is why the charge regions are inverted. The (0,0) is at top-right corner.

The results for our DQD device are in figure 5.15. In a) it is plotted the big charge stability map. We used this plot to be sure that the last holes in each quantum dot was reached. The top right region of the plot is the (0,0) charge region. We can distinguish lines in two direction. The almost vertical ones, related to the charge loading into dot 1. And the lines of $\sim 45°$ inclination, which correspond to a charge loading into dot 2. From the line's angle we can calculate the coupling between plunger gates. The almost vertical charge lines

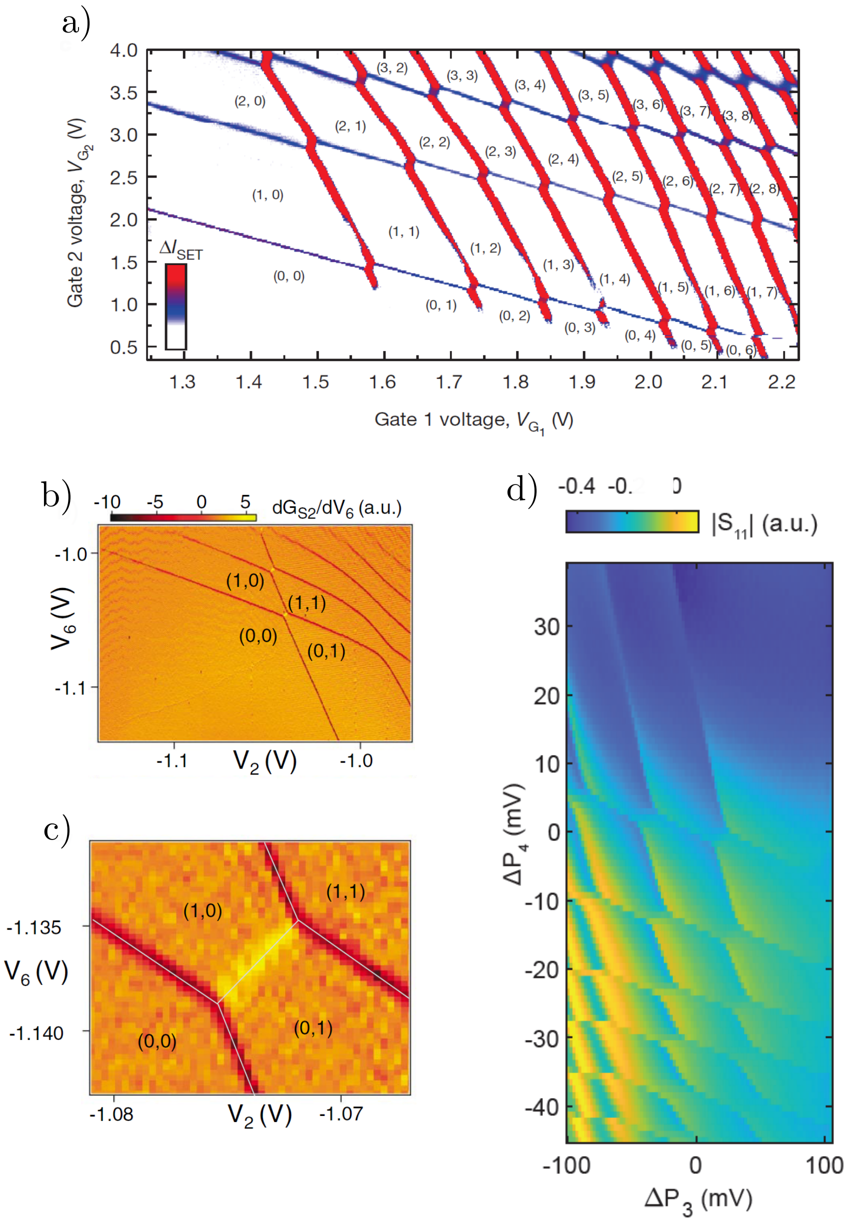

Figure 5.14: Figure with the charge stability diagrams from different groups. a) is measured in a SiMOS double quantum dot [23]. In the plot we see the ΔI for the charge sensor. b) and c) are taken from [19]. The device was a DQD in GaAs/AlGaAs. b) shows the charge stability diagram in a large scale while c) focus in the $(0,0) \rightarrow (1,1)$ charge transition. d) is taken from [138]. Here we see the charge stability diagram, but for holes in Ge/SiGe quantum well. This data was recorded with a reflectometry circuit in the charge sensor.

for dot 1 indicates a strong coupling between plunger G1 and dot 1, and a weak coupling between plunger G2 and dot 1. On the other hand, the tilted lines for charge loading into dot 2 show that G1 coupling with dot 2 is similar to the coupling between G2 and dot 2. We explain this effect by assuming that the dot 2 wavefunction position is in the midway between gate G1 and gate G2. Another interesting phenomenon in plot a) is the decrease in the addition energy as the dots are filled with holes. The first honey combs are bigger than the ones at the bottom left. We can see how the hole occupation modifying the dot size.

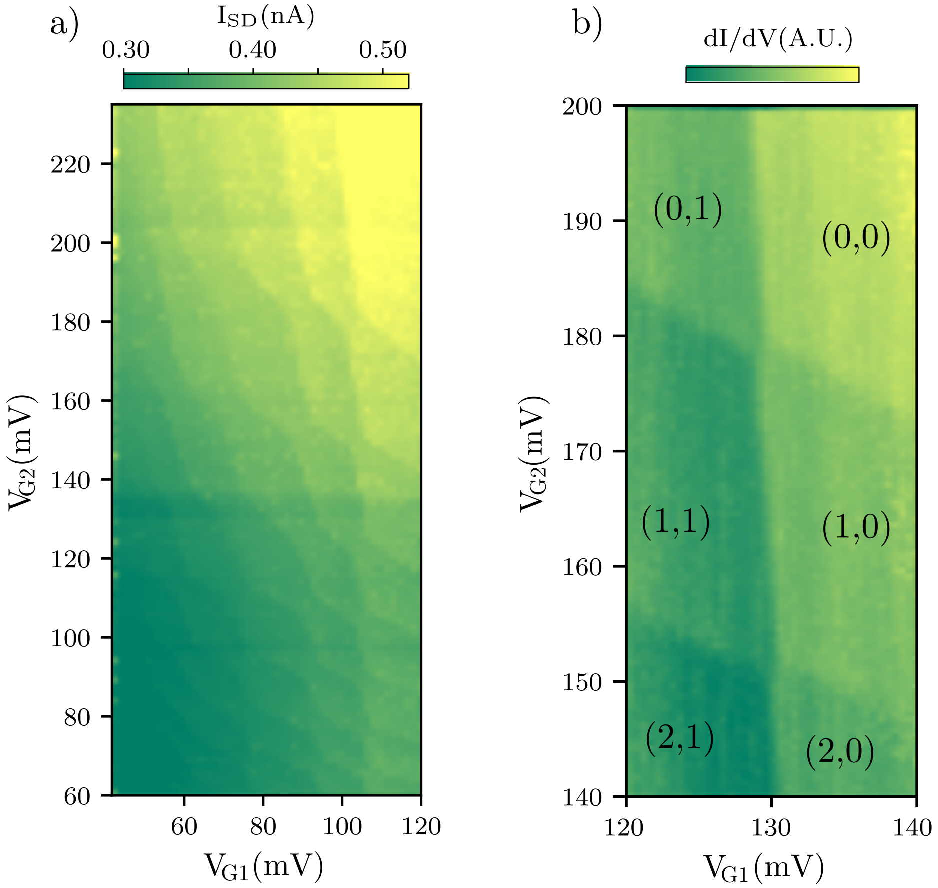

Figure 5.15: Two stability diagrams of our DQD. a) shows the big map of several charge states. We see charge sensor current versus both plunger gates. The top right corner shows the (0,0) charge region. We can distinguish the charge loading lines corresponding to dots 1 and 2. b) shows a zoom into the top right corner of map a). Here we see the differential conductance versus both plunger gate voltages. The interdot coupling is lower than in plot a). This probes that we can access the few-charges regime for our DQD.

In plot from figure 5.15 b) we observe a zoom into the top right corner of figure 5.15 a). The labels indicate the number of charges in each dot. They are counted from the (0,0) charge region. The few-charges regime is very interesting to perform experiments. Knowing the number of charges in each dot gives more control in the formation of singlet and triplet states, and allows to perform Coulomb spin-blockade for read-out.

5.8 Conclusions

Along this chapter we have shown the results of the DQD device produced with our fabrication method. The device consisted in a double gate layer with a charge-sensor near-by. It was measured in a dilution fridge at 7 mK.

The first section of the chapter was focus on DC measurement through the DQD. We discussed the Coulomb blockade regime tuning and the barrier gate optimization. The interdot barrier gate was used to tune the dot capacitance coupling $\mathrm{C_m}$, being able to form a big SQD with both plunger gates and two independent QD.

We measured bias triangles in the many-hole regime from which we extracted some characteristic parameters of the system: charging energies $\mathrm{E_{C1}}$ and $\mathrm{E_{C2}}$, the dot capacitance $\mathrm{C_1}$ and $\mathrm{C_2}$, the dots lever arm α_1 and α_2, and the interdot coupling $\mathrm{C_m}$. This measurement can be used to fully characterize the system's electrostatic capacitance. In the bias triangles, we also see some traces of transport through excited states.

The second part of the chapter is focused on the charge sensing technic. We searched for the most sensitive points to measure. The best conditions were with a charge sensor bias of $\mathrm{V^{CS}_{bias}} = 0.5\mathrm{mV}$. We also observe that decreasing the hole density at the ohmic reservoirs helped to increase the contrast of signal versus noise. The best results were when the ohmic accumulation gates were tune at $\mathrm{V_{ohmics}} = 20\mathrm{mV}$.

The last part of the chapter are measurements of the charge stability diagram. We were able to reach the (0,0) charge region, where both dots are empty. We also measure the last charge regions with high precision and nice contrast.

The results in this chapter are very promising, here we are touching the top of the iceberg. We demonstrated the viability of our Ge/SiGe quantum well heterostructures to host DQD. And even more, we reached the empty dot region measuring with a charge sensor. In terms of technology, we have reached the state-of-the-art framework for quantum dots in Ge heterostructures. From here on, there are a lot of possible ways to continue the research. In the system's configuration for figure 5.15 b), the hole's tunnel rate dependence with the interdot barrier gate could be studied. This experiment could have been easily achieved, but we lacked of time to perform it. In a more long-term experiment, with a DQD it is already possible to form a charge qubit. It's been done in GaAs [139, 140] and in Si based devices [141]. With applied magnetic field, we would have access to the hole's spin states. This can also be used to form qubits, as it is being demonstrated in Si nanowires [142], SiMOS [143], Si/SiGe heterostructures [144], CMOS nanowires [96] and Ge/SiGe heterostructures [145]. With two quantum dots, a two-qubit logic gate can be created like in [23, 146, 147]. Another step we could take is the implementation of a reflectometry line for read-out or to a superconductive resonator [45, 46]. The strong photon-spin interaction has still not been reached in strained Ge quantum well structures, but it has been in other architectures [148–150]. Another path to follow could be the scalability with more quantum dots to perform more complicated quantum operation [52].

Chapter 6

Conclusions

6.1 Summary

Along this PhD thesis, I have presented the development of a fabrication recipe for quantum devices in a Ge/SiGe heterostructure, with the posterior characterization and analysis of mesoscopic transport measurement. Ge/SiGe heterostructure is growing as a promising material for quantum spintronic, quantum computing hardware and superconductor-semiconductor hybrid devices. The key proprieties of Ge/SiGe heterostructures are the small in-plane hole effective mass, a large out-of-plane g-factor, the intrinsic spin-orbit coupling and the reduced hyperfine interaction due to the p-wave symmetry in the hole's wavefunction.

An important part of my work was focus on the recipe development and its optimization. The process consists in several steps, each of them with its own particularities. I used optical lithography for the large scale features of the sample (ohmic contacts, mesa, gate pads) and e-beam lithography for the quantum device gates. For both lithography process, a study in the exposition conditions was necessary. Specially for the e-beam lithography, where doses tests and proximity effect corrections were performed for almost every design. Two different etching steps had to be optimized, one for the ohmic contact and another one for the mesa etching. I paid special attention to the mesa etching step, several recipes were developed and pictured with SEM. Finally, for the two dielectric steps in the recipe, an ALD process was tested and improved. Oxygen plasma precursor and high temperature conditions are growing a high quality Al_2O_3 dielectric, characterize by a high breakdown voltage. The final recipe was obtained after several years of work in the clean-room.

The heterostructure and the fabrication process were tested with several mesoscopic transport measurement. We observed field effect, tunneling into surface traps and pinch-off voltage drift. I implemented an extra step in the fabrication recipe focus on oxidizing the samples' surface with a strong oxygen plasma. This way surface traps were reduced and hysteresis improved. The first quantum devices measured were QPC and H-FET. With H-FET I observed a control over the 2DHG density, and quantum transport was obtained with the QPC devices. Both of these results are important for the QDs construction. They demonstrate the viability of the fabrication recipe and the Ge/SiGe heterostructures to host QDs.

Another probe for the fabrication process is the SQD measurements. Several text-book characterizations were performed, like extracting the charging energy, the lever arm, the dot size, etc... A study on the barrier gates is performed, looking for the symmetric tunnel rate regime. At the end of the corresponding chapter, we also measured charge-noise with results not very far from the state-of-the-art. Last measurement was transport under magnetic field, showing a polarization of the reservoir's spin. With this data, the out-of-plane Landé g-factor was extracted.

The last chapter is focus on DQD devices, measured in DC current and with charge sensing. Here we arrived to the final step in the viability study for the Ge/SiGe heterostructures. The DQD construction is the final keystone to start building a functional qubit, either spin qubit or charge qubit. I demonstrate interdot coupling control, being able to switch from a single quantum dot to a double quantum dot. Characterization of the system's capacitances was also performed. Eventually, a charge sensor in the vicinity of the DQD has been tuned and used for the charge state readout of the DQD. Even the (0,0) charge region was obtained.

Eventually, the PhD work reported in this manuscript demonstrate that the Ge/SiGe heterostructure complemented with electrostatic gates can host particularly good semiconductor quantum devices. The recipe developed is also been probed to be resilient and useful for different layouts. In conclusion, quantum dots have been successfully created and measured.

6.2 Perspectives

I would like to conclude this thesis with the perspective and possible future plans. The results obtained in the SQD and DQD devices, plus the demonstration that we can spin-polarize the holes in the sample, open the road to a quite large amount of future experiments.

In a SQD, an improvement in the design could easily be done. Smaller barrier gate length would allow a better control over the tunnel rates. Because of a tight schedule, we didn't have enough time to properly measure the SQD under magnetic field, but we could have done a study on the g-factor anisotropy [44]. We could also consider measuring Kondo effect in QD. It is being found in GaAs [20] but not in strained Ge quantum-well. Using the spin to charge conversion [133] we have access to spin state of the dot and observe singlet-triplet states [66, 134], and measure the recently proposed Rabi anisotropy [151].

In a DQD, with our device it is already possible to form a charge qubit. It's been done in GaAs [139, 140] and in Si based devices [141]. With applied magnetic field, we would have access to the hole's spin states. This can also be used to form spin qubits, as it is being demonstrated in Si nanowires [142], SiMOS [143], Si/SiGe heterostructures [144], CMOS nanowires [96] and Ge/SiGe heterostructures [145]. With two quantum dots, a two-qubit logic gate can be created like in [23, 146, 147]. Another step we could take is the implementation of an RF line for read-out, as they do in [45, 151, 152], or a superconducting circuit, like in [153]. Strong photon-spin interaction has still not been reached in strained Ge quantum well structures, but it has been in other architectures, like CMOS spin qubits [148] and Si/SiGe quantum well heterostructures [149, 150]. Another path to follow could be the scalability with more quantum dots to perform more complicated quantum operation [52]. Nevertheless, scalability implies an increment in the number of quantum dot gates, and this leads to a more complex process to tune the Coulomb blockade regime. In order to relax this effort, a solution could be machine learning algorithms [154, 155].

Another way to go would be exploring more exotic quantum phenomena. The fabrication process developed in this thesis has been probed strong enough to try other device designs. We could study spin pumps in strained Ge/SiGe heterostructures, like in [156]. Another brave option could be the electron temperature cooling with hole's exchange, what is known as Maxwell's daemon [157]. Other interesting termodynamic experiments can be carried on [158, 159] We could also go into the semiconductor-superconductor hybrid devices [53–55, 160].

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Appendix A

Clean-room techniques

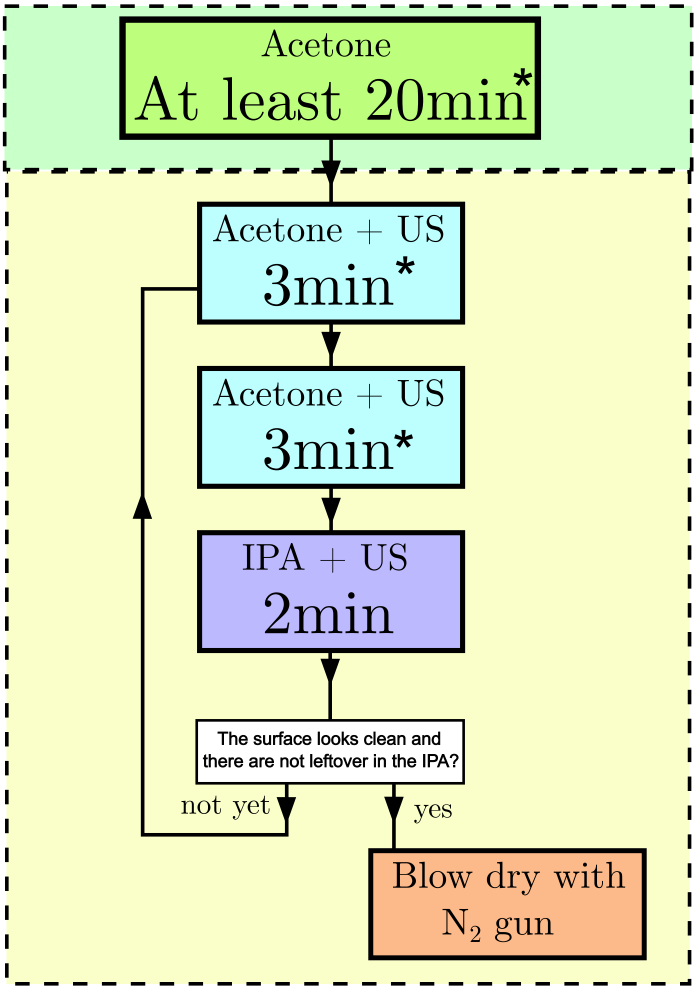
In this annex I want to explain the different techniques I used in the clean-room. Most of them related to lithography processes like lift-off or resist spinning.

A.1 Clean surfaces are important

No one knows what is going on with interfaces. People have tried to explain it, and some have success up to some point, but it still remains as a dark side of science. An interface can charge your device, discharge it, can make it leaky or can protect it. Semiconductor devices are very sensitive to anything around them. In a normal fabrication process, several steps add layer of material to the sample. A dirty surface will make a dirty interface, and we don't want that. If I had to just give one advice out of the hours I spend in the clean-room, it would be "clean surface are important".

In general, I found three different situations where I had to clean a sample: the very beginning of the fabrication process, after a lift-off and for removing the resist (either because of a wrong lithography exposition or because the fabrication step was just etching). For each of those three situation, the cleaning process slightly changes. In figure A.1 I represented a chart-graph with the process. When doing a lift-off, it works much better if the sample is deposited in the acetone for some time before doing the real lift-off. If it can be a full night, it would be fantastic. Another trick for the lift-off is pipetting the sample surface with a plastic pipette (the same used for the resist). The pipetting is done inside the same acetone directly on the sample surface. I do this until I don't see any more metal attach to the surface. At than point, I start with the yellow-background process of the figure.

If the process is followed propertly, I assure clean and brilliant surfaces or your sample. Another important thing is to clean the cleaves from time to time. Just acetone and a clean-room napkin make the job.



*** It is better if there is a small plate inside the baker and the sample is facing down inside the plate.**

Figure A.1: Protocol for cleaning a sample. Green background indicates the steps to follow when doing alift-off. Yellow background indicates the step to follow in any case.

A.2 Resist spinning

Only two advices. Before putting the sample into the spinner, I like to heat it at $100°C$ for one minute so all the water attached to the surface evaporate. In the clean-room there should not be water, but you never know. After the minute in the hot plate, I put it in the spinning machine and start the vacuum. Next step is taking the resist from the bottle. Never ever, no matter what happen, let a resist drop falling again in the bottle. The pipette for taking the resist should be introduced only once. If something fails in the process, take another pipette. The advice is to blow with nitrogen the pipette before introducing them into the resist bottle.

If those steps are well followed, the resist spinning should go well. Resist quantity should be just enough to cover the surface, but in case of doubt, it is better to put more resist than less. Just after the spinning, there should not be any small particles in the surface. In case that there are, cleaning the resist and trying again is the way to go, otherwise there will be problems in the mask aligner. If the resist is for e-beam, then the particles in the surface are not a big issue. Still it would be better if they are not there.

Appendix B

Coulomb peak analysis

B.1 Coulomb peak analysis

In this annex we will analyise the Coulomb peak with a conduction equation fit. A schematic of the system is in figure B.1 a) and next to it the results for the experiment, in figure B.1 b). The current through the peak follows the equation [reference to theory section], just that now, the bias voltage applied is not negligible. We write

$$I = \frac{e}{h}\int \frac{\Gamma_S \Gamma_D}{(\Delta E)^2 + (\Gamma_P/2)^2}[f_S(E) - f_D(E)]dE, \tag{B.1}$$

where $\Gamma_P = \Gamma_S + \Gamma_D$, $\Delta E = E - E_P$ being E_P the resonant peak energy, and $f_{S,D}(E)$ are the Fermi source and drain distribution due to temperature, they are defined as

$$f_{S,D}(E) = \frac{1}{(1 + \exp\left(\frac{E + eV_{bias}^{S,D}}{k_B T}\right)}. \tag{B.2}$$

We already see that the solution for equation B.1 is not trivial and it needs to be solved numerically. In our case, the bias voltage is $V_{bias} = 100\mu$V, and temperature 300mK. The tunnel rates remain unknown for us. We could have extracted the tunnel rate values if we had measured the Coulomb peak at different temperatures. For now, we will do a peak broadening analysis in terms of energy. The FWHM for peak in figure B.1 b) is $FWHM = 181.6\mu eV$, (we extracted it from a fit to a Lorentzian function). Thermal energy is $E_{temp} = 4k_B T = 102\mu$eV. The bias voltage adds $eV_{bias} = 100\mu$V. The tunnel rates are not known. But already bias voltage and temperature will broad the peak by $\sqrt{E_{temp}^2 + (eV_{bias})^2} = 140\mu$eV. The rest of the peak broadness is assumed to come from the tunnel rates $\Gamma \approx 114\mu$eV.

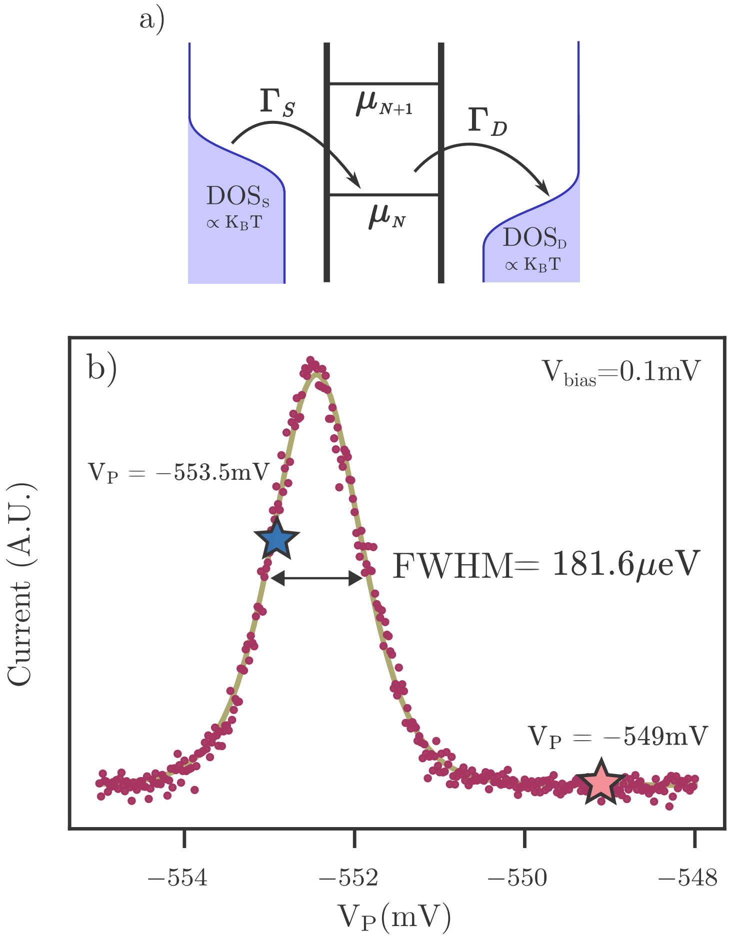


Figure B.1: a) schematic of the QD state during the charge-noise measurements. We can observe a Fermi level broadening at the reservoirs because of thermal excitation. b) Coulomb peak where the charge noise measurements have been performed. It shows current through the SQD versus plunger gate voltage. The blue star correspond to the slope measurements and the pink start to the Coulomb blockade measurements. Solid line is a fit to the Buttenkir conductance.