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# Fast short-circuit protection for SiC MOSFETs in extreme short-circuit conditions by integrated functions in CMOS-ASIC technology

Yazan Barazi

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Université  
de Toulouse

# THÈSE

En vue de l'obtention du

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Institut National Polytechnique de Toulouse (Toulouse INP)

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**Titre :**

Fast short-circuit protection for SiC MOSFETs in extreme short-circuit conditions by integrated functions in CMOS-ASIC technology

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*To my Mom*

## Table of Contents

THÈSE .....	0
Acknowledgement.....	2
Table of Contents .....	5
List of Acronyms.....	8
Résumé.....	9
Abstract .....	11
Chapter I: Challenges associated with driving SiC MOSFETs.....	14
1. Introduction .....	14
2. Specificities of SiC MOSFETs.....	15
2.1. Wide-band gap power devices evolution.....	15
2.2. Electrical and switching characterization of SiC MOSFET .....	18
2.3. Switching mechanism analysis.....	21
3. Gate Drivers for SiC FETs .....	25
3.1. Gate Drivers fundamentals for power FETs.....	26
3.1.1. Gate driver functions .....	26
3.1.2. Gate driver fundamental parameters.....	28
3.1.3. Isolation .....	29
3.1.4. Buffer Architecture.....	32
3.2. SiC MOSFET power device and the challenges faced by the gate driver.....	34
3.2.1. Switching and transmission monitoring .....	36
3.2.2. Health monitoring.....	39
3.2.3. Safety monitoring .....	40
3.3. Technology review .....	43
4. Behavior of SiC MOSFET Under Short-Circuit .....	48
4.1. Characteristics impacts of SiC MOSFET and Si IGBT under short-circuit.....	48
4.2. Turn-on analysis of SiC MOSFET .....	50
4.2.1. Normal Turn-on.....	50
4.2.2. Hard Switch Fault.....	52
4.2.3. Fault under load.....	53
4.3. Unique SiC MOSFET behavior under Short-circuit .....	53
4.4. Possible Failure mode .....	54
5. Short-Circuit Detection techniques .....	56
5.1. Shunt resistor monitoring method .....	57

5.2.	Sense-Fet monitoring method.....	58
5.3.	Current transformer monitoring method .....	58
5.4.	Desaturation monitoring method.....	58
5.5.	Gate current leakage monitoring method .....	60
5.6.	Gate Charge monitoring method .....	61
5.7.	Fault detection methods Summary / Benchmark.....	64
6.	Conclusion.....	65
Chapter II: Design of integrated gate drivers in 0.18 $\mu$ m SOI CMOS technology for MOSFET SiC power device .....		67
1.	Introduction .....	67
2.	Design of the power test benches .....	67
2.1.	Power Test bench V1 .....	68
2.2.	Power Test bench V2 .....	69
3.	CMOS technology and Buffer specification .....	70
3.1.	SOI CMOS 0.18 $\mu$ m Technology.....	71
3.1.1.	Bulk CMOS vs SOI CMOS.....	71
3.1.2.	0.18 Micron Modular BCsD-on-SOI Technology.....	72
3.2.	Buffer Specifications and adaptation.....	73
3.3.	Buffer Architecture & Technology options.....	76
4.	Design and sizing of an integrated active gate driver.....	78
4.1.	Active gate driver Architecture .....	79
4.1.1.	Level shifter.....	79
4.1.2.	Output Buffer .....	81
4.1.3.	Active Miller Clamp (AMC).....	89
4.1.4.	High impedance and Soft shut down.....	93
4.2.	Summary of the Gate driver .....	95
4.3.	Gate driver layout design & packaging .....	95
4.4.	Characterization and experimental validation of the gate driver.....	101
4.4.1.	V0.A under a load capacitor with no power.....	101
4.4.2.	V2.A implementation in the power test bench V2 .....	107
5.	Modular Multilevel Gate driver MMAGD.....	108
5.1.	MMAGD topology .....	109
5.2.	MMAGD design and layout .....	113
6.	Conclusion.....	116
Chapter III: Proposed High-speed Short-Circuit monitoring and Protection for SiC MOSFETs .....		118

1. Introduction .....	118
2. Gate charge monitoring .....	119
2.1. Analytical study of the Gate charge .....	119
2.1.1. Normal Turn-on condition.....	119
2.1.2. Hard switch Fault condition .....	122
2.1.3. Fault under load condition.....	125
2.1.4. Open Circuit condition .....	126
2.2. Gate charge robustness study .....	128
2.3. Proposed schematic, RC rating and trade-off.....	132
2.4. Experimental results .....	137
2.4.1. V1.A Discrete components prototype .....	137
2.4.2. V1.b SMD prototype .....	143
3. Gate Derivation Monitoring .....	146
3.1. Proposed schematic & review of the method .....	147
3.1.1. Slope approach .....	149
3.1.2. Dip approach .....	150
3.2. Detection circuit based on derivation monitoring and simulation behavior.....	151
3.3. Design and layout of the derivation method.....	155
3.4. Experimental results .....	163
3.4.1. Experimental results under an equivalent capacitor and no power, V0.1.....	163
3.4.2. Experimental results using a DUT and power test bench, V2.2.....	164
4. Feedback from power FET to CMOS: Third monitoring method.....	167
5. Comparison between the proposed detection techniques .....	168
6. Conclusion.....	170
Conclusion & Outlook.....	172
Appendix A .....	175
Appendix B .....	178
Appendix C .....	180
List of Figures .....	205
List of Tables.....	210
References .....	212
Author's references .....	224

## List of Acronyms

Si	Silicon
WBG	Wide Band Gap
SiC	Silicon Carbide
GaN	Gallium Nitride
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SiO <sub>2</sub>	Silicon dioxide
SJ-MOSFET	Super-Junction MOSFET
JFET	Junction-Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
HEMT	High-Electron-Mobility Transistor
GTO	Gate Turn-Off Transistor
DUT	Device Under Test
BJT	Bipolar Junction Transistor
HV	High voltage
LV	Low voltage
HS	High side
LS	Low side
EMI	Electro-Magnetic Interference
EMC	Electro-Magnetic Compatibility
CMTI	Common Mode Transient Immunity
HT	High temperature
EV	Electric vehicle
PWM	Pulse Width Modulation
AGD	Active Gate Driver
MMAGD	Multi-level Modular Active Gate Driver
CMOS	Complementary metal–oxide–semiconductor
PMOS	P-type metal–oxide–semiconductor
NMOS	N-type metal–oxide–semiconductor
SC	Short-Circuit
HSF	Hard Switch Fault
FUL	Fault Under Load
OC	Open Circuit
DESAT	Desaturation
ASIC	Application-Specific Integrated Circuit
SMD	Surface Mounted Diode
PCB	Printed Circuit Board
DRC	Design Rule Checking
LVS	Layout Versus Schematic
FPGA	Field programmable gate arrays
SOI	Silicon On Insulator structure
AMC	Active Miller Clamp
SSD	Soft Shut Down
Drv	Drive

## Résumé

*Le manuscrit est rédigé en anglais, vous pouvez trouver un résumé de l'ensemble de la thèse à l'Annexe C.*

Les transistors de puissance grands gaps tels que les MOSFETs SiC et HEMT GaN repoussent les compromis classiques en électronique de puissance. Brièvement, des gains significatifs ont été démontrés par les transistors SiC et GaN: meilleurs rendements, couplés à une augmentation des densités de puissance offertes par la montée en fréquence de découpage. Les MOSFET SiC à haute tension présentent des spécificités telles qu'une faible tenue en court-circuit (SC) par rapport aux IGBT Si et un oxyde de grille aminci, et une tension de commande rapprochée grille-source élevée. La polarisation négative sur la grille à l'état bloqué crée un stress supplémentaire qui réduit la fiabilité du MOSFET SiC. La forte polarisation positive de la grille provoque un courant de saturation de drain important en cas de SC. Ainsi, cette technologie fait émerger des besoins spécifiques de surveillance et de protection ultra-rapides. Pour cela, le travail de cette thèse se focalise sur **deux études** pour surmonter ces contraintes tout en gardant un bon compromis de performances entre « niveau d'intégration technologique 'CMS/ASIC-CMOS'–rapidité–robustesse ». La première, regroupe un ensemble de solutions nouvelles permettant une **détection du court-circuit** sur le cycle de commutation, sur la base d'une architecture conventionnelle de commande rapprochée dite à 2 niveaux de tension. La deuxième étude est plus exploratoire et basée sur une **nouvelle architecture de gate–driver**, dite **multi-niveaux**, à faible niveau de stress pour le MOSFET SiC tout en maintenant les performances dynamiques.

Les travaux portent tout d'abord sur l'environnement du SiC MOSFET, (caractérisation et propriétés de comportement en SC par simulations orientées "circuit" de type PLECS™ et LTSpice™), puis présentent une étude bibliographique sur les commandes rapprochées dites Gate Driver, une étude approfondie a été réalisée sur les court-circuits type I & II (Hard switch fault) (Fault under Load) ; regroupés dans un premier chapitre du manuscrit.

Un banc de test réalisé antérieurement au sein du laboratoire, a permis de compléter et de valider l'étude d'analyse-simulation et de préparer des stimuli test pour l'étape de conception des nouvelles solutions.

Inspirée par la méthode de Gate charge apparue pour les IGBTs en silicium et évoquée pour les MOSFETs SiC, cette première approche fait l'objet d'un travail de conception, de dimensionnement et de prototypage. Cette méthode de référence permet une détection de type HSF en moins de 200ns sous 0-600V avec des composants 1,2kV allant de 80 mOhm à 120mOhm.

S'agissant des nouvelles méthodes de détection rapides et intégrées, les travaux de cette thèse se focalisent particulièrement sur la conception d'un circuit ASIC CMOS. Pour cela, la conception d'un gate driver adapté est essentiel. Un ASIC est conçu en technologie X-Fab XT-

0,18 $\mu\text{m}$  SOI-CMOS sous Cadence™, et puis mis en boîtier et assemblé sur PCB conçu pour les besoins de tests et adaptable au banc principal. La conception du gate driver a considéré de nombreuses fonctions (détection du SC, SSD Soft shut down, buffer segmenté, AMC Active Miller Clamp", ...). Du point de vue de la détection du SC, les fonctions nouvelles de surveillance intégrées concernent la méthode de dérivation temporelle de  $V_{GS}$  qui est basée sur une détection par un circuit dérivateur analogique RC sur la séquence de plateau avec deux variantes. Une deuxième méthode nouvelle partiellement intégrée dans l'ASIC a été conçue, non développée dans ce mémoire dans le but d'une valorisation.

En marge de cette étude principale, une étude exploratoire a porté sur une nouvelle architecture modulaire de commande rapprochée à plusieurs niveaux de tension de polarisation tirant profit de l'isolation SOI et des transistors CMOS à basse tension pour piloter les MOSFETs SiC et améliorer leur fiabilité grâce à une sélection active et dynamique à plusieurs niveaux sur les séquences de commutation et les états marche/arrêt.



## **Abstract**

Wide band gap power transistors such as Silicon Carbide (SiC) MOSFETs and High Electron Mobility Transistors (HEMTs) Gallium Nitride (GaN) push furthermore the classical compromises in power electronics. Briefly, significant gains have been demonstrated by SiC and GaN transistors: better figure of merit, coupled with an increase in power densities offered by the increase in switching frequency. High-voltage SiC MOSFETs have specific features such as a low short-circuit withstand time capability compared to Si IGBTs, a thinner gate oxide, and a higher gate-to-source switching control voltage. The negative bias on the gate at the off-state creates additional stress which reduces the reliability of the SiC MOSFET. The high positive bias on the gate causes a large drain saturation current in the event of a short-circuit. Thus, this technology gives rise to specific needs for ultra-fast monitoring and protection. For this reason, the work of this thesis focuses on two studies to overcome these constraints. The first one, gathers a set of new solutions allowing a detection of the short-circuit on the switching cycle, based on a conventional switch control architecture with two voltage levels. The second study is more exploratory and is based on a new gate-driver architecture, called multi-level, with low stress level for the SiC MOSFET while maintaining dynamic performances. These studies were conducted with the objective of reaching a good performance compromise between “SMD/ASIC-CMOS technological integration level - speed – robustness”.

The first chapter of the manuscript covers firstly the SiC MOSFET environment, (characterization and properties of short-circuit behavior by simulation using PLECS and LTSpice software) and covers secondly a bibliographical study on the Gate drivers. At last, an in-depth study was carried out on type I (Hard Switch Fault, HSF) and type II (Fault Under Load, FUL) short-circuits, as well as detection circuits proposed in the literature. Most of these detection circuits are insufficient as they do not achieve and allow the above performance compromise.

A test bench, previously carried out in the laboratory, was used to complete and validate the analysis-simulation study and to prepare test stimuli for the design stage of new solutions. In order to remain in the low-voltage environment of the gate driver, the problems were treated directly and solely exploiting the gate voltage and current of the SiC MOSFET. Inspired by the Gate charge method that appeared for Si IGBTs and evoked for SiC MOSFETs, our effort was initially directed towards this method as a reference. This method has therefore been the subject of design, dimensioning and prototyping work. This reference allows an HSF type detection in less than 200ns under 400V with 1.2kV components ranging from 80mΩ to 120mΩ.

Regarding new rapid and integrated detection methods, the work of this thesis focuses particularly on the design of a CMOS ASIC circuit. For this, the design of an adapted gate driver is essential. An ASIC is designed in X-Fab XT-0.18 SOI-CMOS technology under Cadence, and then packaged and assembled on a PCB. The PCB is designed for test needs and adaptable to the main bench. The design of the gate driver considered many functions (short-circuit detection, soft-shut-down, segmented buffer, an "Active Miller clamp", ...). From the

short-circuit detection point of view, the new integrated monitoring functions concern the  $V_{GS}$  time derivative method which is based on a detection by an RC analog shunt circuit on the plateau sequence ( $V_{GS}$  above  $V_{GS\_M}$ ) with two approaches: the first approach is based on a dip detection, i.e. the presence or not of the Miller plateau. The second approach is based on slope detection, i.e. the variability of the input capacitance of the power transistor under short-circuit HSF compared to normal operation. These methods are compared in the third chapter of the thesis, and demonstrate fault detection times between 40ns and 80ns, and preliminary robustness studies and critical cases are presented. A second new method is partially integrated in the ASIC, was designed. This method is not developed in the manuscript because it is confidential.

In addition to the main study, an exploratory study has focused on a modular architecture for close control at several bias voltage levels taking advantage of SOI isolation and low voltage CMOS transistors to drive SiC MOSFETs and to improve their reliability through active and dynamic multi-level selection of switching sequences and on/off states. This work is presented in the second chapter of the manuscript.

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# Chapter I: Challenges associated with driving SiC MOSFETs

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## Chapter I: Challenges associated with driving SiC MOSFETs

*In this first chapter, we describe a brief overview of the state of the art of power transistors. As well, an overview of the power device, gate drivers; and the challenges faced by the gate driver for SiC power devices is presented. Thus, the functions of monitoring and control around power transistors are discussed. Thus, an insightful study of the state of the art of short-circuit behavior and detection methods is developed.*

### 1. Introduction

The activities of power electronics consist of providing the capability to transfer energy to one or more electrical loads from one or more primary energy sources. In order to be able to control, modulate and transfer energy, power converters need to use at least one controlled power switch. For this purpose, there is a wide range of switches in silicon technology (GTO-Thyristor, IGBT, MOSFET), as well as, wide band gap semiconductor components (SiC, GaN) available from various manufacturers and research institutes. Insulated gate transistors such as the MOSFETs or IGBTs must be driven by a control circuit, called gate driver. The purpose of the gate driver circuit is to provide, control and manage the charge and/or discharge of the gate electrode of the power transistor, and to allow changes of state (from On to Off or vice versa).

Wide bandgap semiconductor materials, such as Silicon Carbide (SiC), have undergone a tremendous evolution in recent years. Power semiconductor devices, such as Insulated Gate Bipolar Transistors (IGBTs) and Super-Junction (SJ-MOSFET) silicon devices, are limited in terms of maximum switching speeds and more generally, with figures of merit close to the theoretical limits of Silicon [1]. Consequently, silicon power devices have high switching losses and large and expensive thermal management systems, leading to limits in terms of maximum converter efficiency and switching frequency. In contrast, SiC MOSFETs are promising power semiconductor devices for high density converters, with low conduction and switching losses and high temperature stability [2]. As the SiC MOSFETs gain maturity and their cost goes down with time, SiC MOSFETs are expected to be adapted and used in more and more applications.

However, the higher power densities enabled brings the issue of how long a short-circuit fault can be sustained by a SiC power device. Regardless of the short-circuit robustness, the short-circuit fault must be turned OFF as soon as detected to preserve the device from degradation and possible repeated short-circuit occurrences. The short-circuit (SC) delay time capability for SiC MOSFETs is lower than for silicon devices [3]. Power converters designed with these components are therefore less robust.

Power semiconductor devices are used in various industrial applications, including motor drives, battery chargers, switch mode power supplies and converters. These devices are exposed to several types of short-circuit (SC). The hard switch fault (HSF, SC type I) and fault under load (FUL, SC type II) are the two main fault behaviors. Safety is necessary for these typical applications.

In order to fully design a gate driver with different functions oriented protection and safety, dedicated for SiC MOSFETs, the electrical characterization of SiC MOSFET is mandatory. Gate driver fundamentals and their key requirement are presented. Different architectures of the gate driver are proposed, for the purpose to get fully familiar with the environment of the SC detection functions.

A clear and detailed comparison between SiC MOSFET and Si IGBT behavior under short-circuit is presented in this chapter. As well as, the two main fault types HSF and FUL are developed. Different monitoring and protection methods for SiC MOSFETs are investigated and developed. The aim is to establish how fast a short-circuit fault can be detected and how fast it can be turned OFF. Therefore, detailed analyses and comparisons between the SC detection methods are presented.

## 2. Specificities of SiC MOSFETs

In this section, the evolution of the power devices is introduced. This evolution shows how the market is oriented towards new wide band-gap (WBG) devices. Wide band-gap transistors have significant advantages and offer new market opportunities. In order to benefit from the opportunities offered by the new WBG components, their implementation must be carefully studied within the power circuit and in association with their gate drivers.

In this section as well, detailed analysis of the switching mechanisms will be introduced of a power inverter cell consisting of SiC MOSFETs. This analysis will allow us to highlight the main physical parameters and freedom degrees to consider in order to optimize the switching sequences by the gate driver.

### 2.1. Wide-band gap power devices evolution

Power semiconductor devices are used to control the energy transfer of electronic systems. Over the last two decades the technology of power semiconductors has made impressive progress. Power transistors are mainly classified into two types [4] [5] :

- Unipolar components Field Effect Transistors (FET): such as the JFET (Junction-Field Effect Transistor) or MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) or the schottky-diode; where only one type of carrier circulates in the component (majority carriers). The FET transistors have control on the size and shape of a channel between source and drain which is created by applied voltage [6].
- Bipolar components: such as PIN diode, IGBT (Insulated-Gate Bipolar Transistor); where for IGBTs have both types of carriers circulate in the component. The name itself indicates that it has two junctions between p-type and n-type semiconductors.

Fig.I. 1 shows the large families of Silicon power components. They are distributed regarding their power and frequency operation range. Each type has its advantages and disadvantages, which respond to different application areas, [7].

The new generations of power converters are based on higher power densities, higher efficiencies and greater robustness. In addition to this, they are based on even faster operation,

low conduction and switching losses and higher temperatures operation. While the converter topology may vary depending on the application, the typical specifications are to process power in an efficient manner, safely, and at low cost. Commonly, the semiconductor devices have been made with silicon (Si) (narrow band semiconductors). However, this leads the semiconductors to adapt and to gain maturity in order to meet those criteria. For a while, silicon devices face its limits, unless new breakthroughs are identified. Therefore, wide band-gap (WBG) semiconductors take place by their different advantages, cited above [8]. The large energy separation between the conduction and the valance bands allows these devices to operate theoretically at elevated temperatures and at critical electrical field, Fig.I. 2.

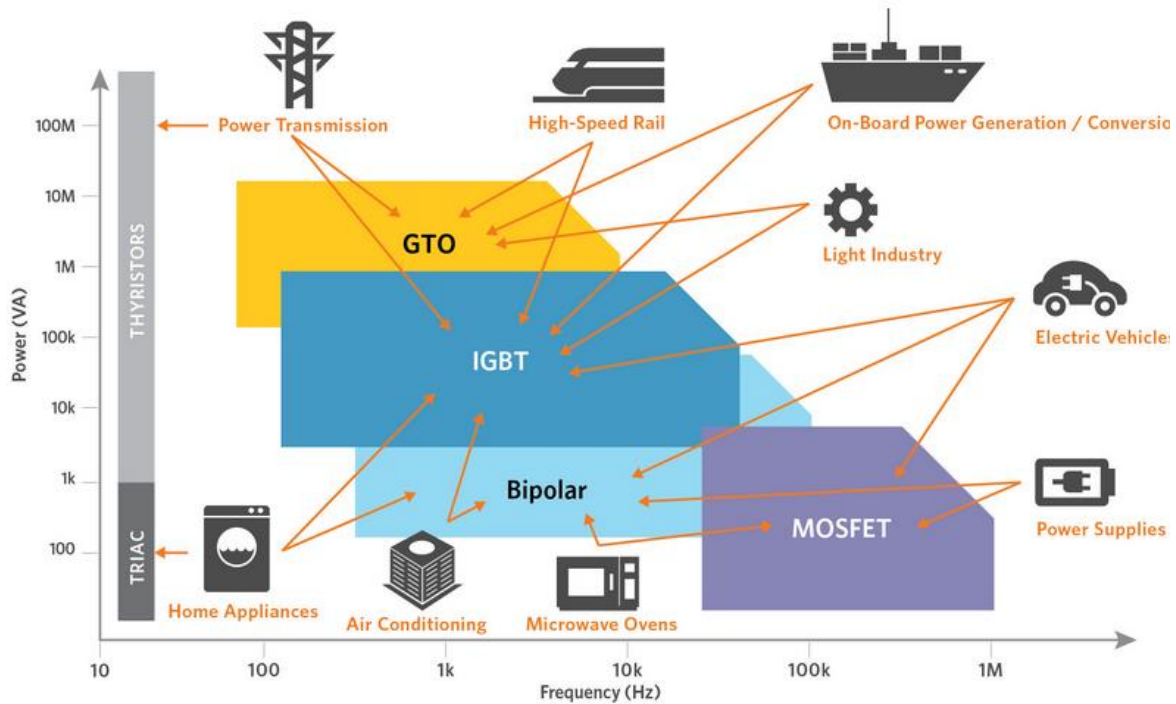


Fig.I. 1. Application areas of classical discrete power semiconductors [9].

The first silicon carbide (SiC) power device to become commercially available in 2001 is the SiC--Schottky-diode mostly used in power supply application [10]. The WBG devices are out of the laboratories and into the real world. In particular, SiC, and Gallium Nitride (GaN) have led to tremendous advances in power switching and/or power amplifier applications [11]. Nowadays, SiC MOSFETs are commonly found in several areas (Rail, motor drive, PV, etc ), and GaN power transistors have found applications in 600V market segments such as data center server power supplies [8] [12] .

SiC attracts attention as material for power devices because of its high thermal capability, high carrier mobility and high critical electric field before avalanche breakdown. Also, SiC is the only compound semiconductor whose native oxide is silicon dioxide (SiO<sub>2</sub>), the same insulator as Si. The SiO<sub>2</sub> has good performance as passivation film in Si power devices, so that this makes it possible to fabricate the entire MOS-based devices in SiC. The main advantage of SiC semiconductor device is the very low resistance of the drift region even if it is designed to

support higher voltage [13]. This favors the development of high voltage unipolar devices which have much superior switching speed than bipolar devices. Also, much lower resistance of the drift region in SiC could enable the development of SiC high power devices [14]. However, the channel region of SiC power transistors still remains an issue due to interface traps and the consequent degradation on the channel-mobility, threshold-voltage drift, whereas the channel resistance is not negligible even for high voltage SiC MOSFETs.

$$R_{Specific} [\Omega \cdot cm^2] = 4 * \frac{V_{BR}^2}{\mu_N \epsilon_0 \epsilon_r E_C^3} \quad (I. 1)$$

$$E_{switching} [J] = \frac{1}{2} * V * I * \frac{Q_G}{i_{G\_Drive}}$$

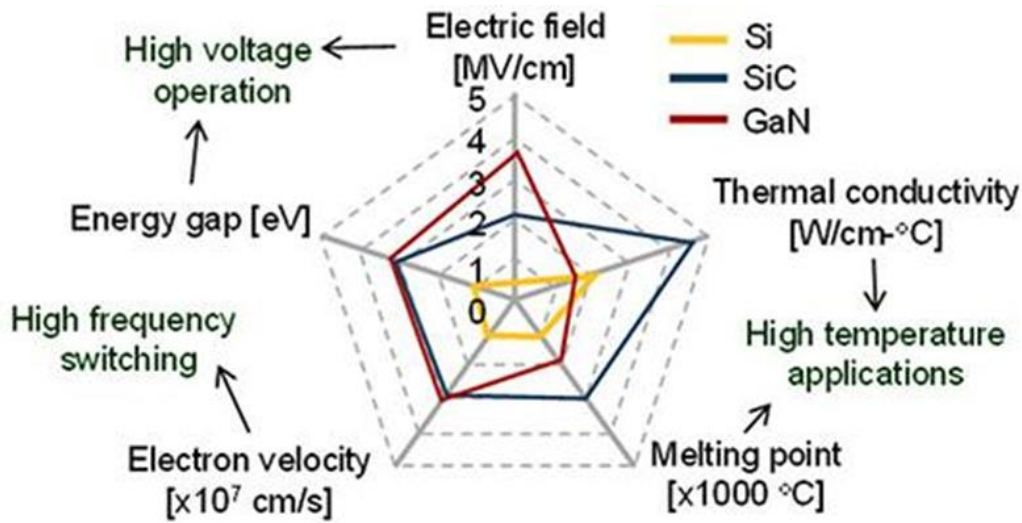


Fig.I. 2. Material properties of Silicon, Silicon Carbide and GaN

Reducing the channel resistance has a direct impact on increasing the area of the semiconductors. The reduction in parasitic capacitances also results in a lower driving energy and a higher switching speed of the component in nominal operation by agreeing to manage the EMC issue. In the event of a short-circuit, however, the high channel polarization will impose a very high short-circuit current-density which, due to the small chip area, will rapidly heat up the component to an extreme value especially for medium and high voltage device. This effect can be exacerbated on the decreasing threshold voltage in a very low negative bias just before the short-circuit event. This property is further enhanced by the presence of a short-channel in many MOSFET SiC structures, which further reduces the on-state resistance but increases the high-voltage drain-source dependency unlike Si device. The behavior study of SiC MOSFETs under short-circuit is detailed in the chap.I.4.

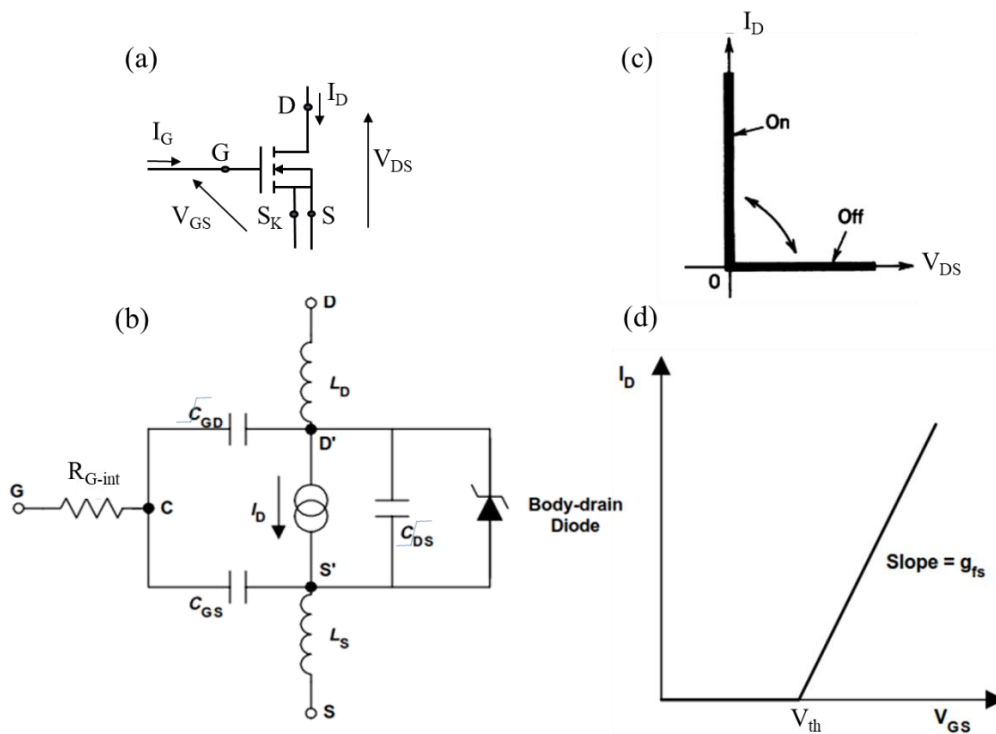
$$\Delta T_j(t) = \frac{2 \cdot V_{ds} \cdot J_{sat}}{\sqrt{\pi \rho \lambda C_p}} \sqrt{t_{sc}} \quad (I. 2)$$



Eq.(I. 2) represents a simplified adiabatic 2D junction temperature transient from idealized constant SC [15]. Note that SiC chip exhibits higher “SC  $J_{Sat}$  (A/mm<sup>2</sup>)” than Si chip + thinner epi N-layer than Si  $\rightarrow T_{SC-SiC} \ll T_{SC-Si}$ .

## 2.2. Electrical and switching characterization of SiC MOSFET

A MOSFET (type of FET) is a voltage-controlled device easy to control. It uses an electric field to control the shape and hence the electron conductivity through the channel in a semiconductor material. The circuit symbol of an n-channel inversion MOSFET is shown in Fig.I. 3.(a). The equivalent circuit model used for the analysis of MOSFET switching performance is presented in Fig.I. 3.(b). When the MOSFET is used as a switch, its basic function is to control the drain to source current or impedance by the gate voltage. MOSFET transistors require the continuous application of a gate-source voltage of appropriate magnitude in order to be in the on state. There is no gate current flow except during the switching of the transistor from on to off or vice versa. Nowadays, the switching times are very short, being in the range of few nanoseconds or few tens of nanoseconds, depending on the size of the chip and the gate device capability. The idealized characteristics of the device operating as a switch is shown in Fig.I. 3.(c) [16].



**Fig.I. 3.** N-channel MOSFET, (a). Symbol (b). Equivalent circuit (c). Idealized  $I_D$ - $V_{DS}$  characteristics (d). Transfer  $I_D$ - $V_{GS}$  characteristic.

The equivalent circuit shows parasitic components that have the greatest effect on the switching characteristics. The switching performance of a device is determined by the time required to establish voltage changes across the input capacitance  $C_{iss} = C_{GS} + C_{GD}$ .  $R_{G\_int}$  is the internal gate resistance, approximate inversely proportional to active area.  $L_S$  and  $L_D$  are



source and drain lead inductances; they are equivalent to few nH. They are involved in the power loop of the circuit. In the other hand  $L_G$ , not taken into consideration in the figure, gets involved in the switching behavior. Those values can increase dramatically depending on the used package and interconnection techniques.

The SiC MOSFET – PIN body diode has low recovery charges, resulting in ultralow switching losses but has higher forward voltage. This is due to the fact that the bandgap of SiC is 3 times larger than that of Si. So it will generally only be used for dead-time sequence. Designs based on Schottky body-diode, are also proposed but not yet commercialized on many references. The diode forward voltage is the guaranteed maximum forward drop of the body-drain diode at a specified value of source current.

The on-state resistance  $R_{DS\_ON}$  is not presented in the equivalent circuit between the drain and the source. This resistance is a representation of the ohmic losses, which arises from the drain drift region. Also, ohmic losses in the channel are included in the  $R_{DS\_ON}$  value.

Briefly, the gate-source controlled drain-source current source shown in the equivalent circuit is equal to 0 before  $V_{GS}$  reaches  $V_{th}$  and then proportional, for high  $V_{GS}$  polarization, to  $g_{fs}(V_{GS}-V_{th})$ . On Fig.I. 3. (d). the transfer curve is presented. As shown the MOSFET is in cutoff when the gate-source  $V_{GS}$  is below the threshold voltage  $V_{th}$ . The value of the threshold voltage is around a few volts for most power MOSFETs but, due oxide traps, a drift of several hundred mV can be seen in operation depending on the levels of gate polarization, duty cycle and switching frequency. The device is under open-circuit operation and must hold off the power supply voltage applied to the circuit. This means that the drain-source breakdown voltage  $BV_{DSS}$  must be larger than the applied  $V_{DS}$  to avoid breakdown and the attendant high power dissipation. When breakdown occurs, it is due to the avalanche breakdown of the drain-body (source) junction; after the cutoff region when the device is driven by greater  $V_{GS}>V_{th}$ . Afterwards the transistor reaches its saturation region, the drain current is independent of  $V_{DS}$  and depends only in  $V_{GS}$  (in the case where Early effect and self-heating is not taken into consideration). The approximated equation is given by eq.(I. 3) for a small voltage difference  $V_{GS}-V_{th}$ , where  $K$  is a constant that depends on the device geometry,  $C_{ox}$  is the oxide capacitance. Taking the velocity saturation into consideration, eq.(I. 4) is proposed, with  $K'$  its respective constant [17], this equation can be used as well for  $V_{DS}\gg V_{GS}$ . The saturation region goes by the name of active region as well.

$$i_D = \frac{K}{2} * \frac{\mu_0}{C_{ox}} * (V_{GS} - V_{th})^2 \quad (I. 3)$$

$$g_{fs} = \frac{di_D}{dV_{GS}}$$

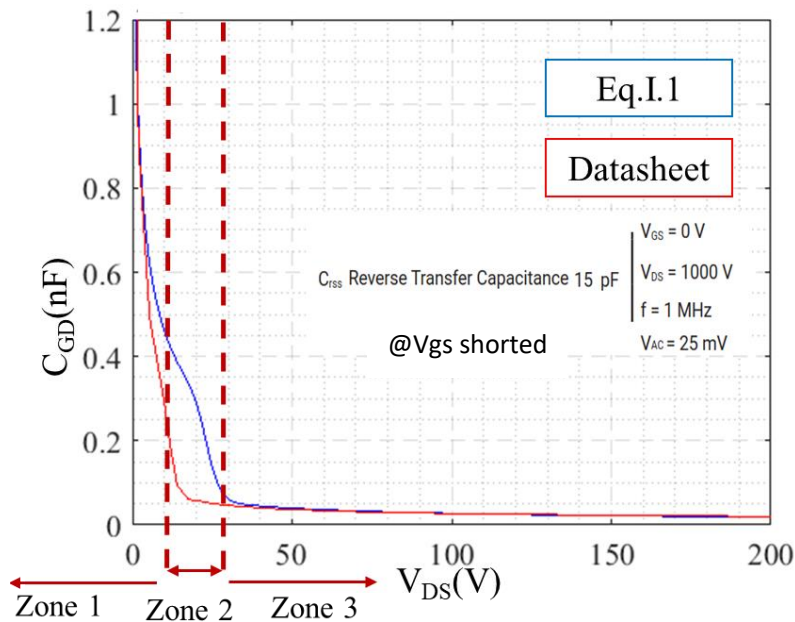
$$i_D = K' * (V_{GS} - V_{th}) \quad \text{with } K' = W * V_{Sat} * C_{ox} \quad (I. 4)$$

Each power component has its own data sheet, providing the typical value of the input capacitance  $C_{iss}$ , the output capacitance  $C_{oss} = C_{DG} + C_{DS}$  and the reverse transfer capacitance  $C_{rss} = C_{GD} = C_{Miller} = C_M$ . Both  $C_{GD}$  and  $C_{DS}$  capacitances are nonlinear capacitances as function of gate-drain voltage. The datasheet provides the nonlinear curves of those capacitance vs Drain-Source voltage.  $C_{GS}$  can also be affected by trapped volume and interface charges, through the elementary P-MOS and N-MOS junction capacitances between the oxide and the substrate in the channel region.

$C_{GD}$  is the most important parameter because it provides a feedback loop between the output and the input terminals of the transistor.  $C_{GD}$  is also called the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances. In order to facilitate the analytical study and analysis simulation of the power transistor on Matlab or PLECS; the non-linearity of the reverse transfer capacitance can be typically modelled by eq.(I. 5), [18].

$$C_{GD} = a_f * K_1 * \frac{1}{\left[ (1 + V_{GD}) * \left( 1 + \frac{K_a * [1 + \tanh(K_b * |V_{GD}| - K_c)]}{2} \right) \right]^{K_2}} \quad (I. 5)$$

Where  $a_f$ ,  $k_1$ ,  $K_2$ ,  $K_a$ ,  $K_b$ ,  $K_c$  are parameters to adjust the equation regarding to each power transistor. These parameters can be easily manipulated to get the image curve of the  $C_{GD}$  non linearity compared to datasheet, as illustrated in Fig.I. 4. The used datasheet curve is from the Wolfspeed second generation transistor C2M0025120D, where  $C_{GD\_Min} = 15\text{pF}$ .



**Fig.I. 4.** Comparison curve of the "small signal" nonlinear capacitance  $C_{GD}$ , between datasheet and eq.(I.2).

This expression is mainly based on the mathematical function, hyperbolic tangent  $\tanh(x)$ , which allows three operation regions: The first region is marked by the sharp decrease of the capacitor value, from  $C_{GD\_Max}$  to an approximate  $C_{GD\_Min}$ . At this region,  $V_{GS}$  is at its maximum

value and  $V_{DS} = 0V$ . The hyperbolic tangent tends towards -1, which leads to eq. (I. 6).  $K_2$  is approximately equal to  $\frac{1}{2}$ . With  $V_{GD} < V_{GS\_Miller}$ .

$$\tanh(K_b * |V_{GD}| - K_c) \approx -1 \quad ; C_{GD} = \frac{a_f * K_1}{[(1 + |V_{GD}|)]^{K_2}} \quad (I. 6)$$

The second region, is where there is a soft decline of the capacitor value, to reach  $C_{GD\_Min}$ . The main parameters responsible of the acute slow curve are  $K_c$  and  $K_b$ .

The third region is marked this time by  $C_{GD\_Min}$ , where the capacitor is almost constant. This time the hyperbolic tangent tends towards +1,  $V_{GS}$  is at its minimum value, and  $V_{DS}$  is high enough not to interfere with the value of the capacitor, eq. (I. 7). With  $V_{GD} > V_{GS\_Miller}$ .

$$\tanh(K_b * |V_{GD}| - K_c) \approx +1 \quad ; C_{GD} = \frac{a_f * K_1}{[(1 + |V_{GD}|) * (1 + K_a)]^{K_2}} \quad (I. 7)$$

### 2.3.Switching mechanism analysis

The switching characteristic was briefly introduced. In this section the switching mechanism will be developed at the turn-on and the turn-off. A commonly encountered circuit in power electronics is examined under PLECS, while simulating a power inverter leg, Fig.I. 5. Modeled SiC MOSFET are positioned on the high side HS and low side LS of the half bridge. The free-wheeling diode reverse-recovery effect is slightly taken into consideration. Parasitic inductances of the power loop and the switching loop are added as well. The load current is introduced by an ideal current source. Both MOSFETs are driven by a modeled representative gate driver which provides a command between -5/20V with a gate resistance  $R_G = 12.5\Omega$  with  $(R_{G\_Ext} + R_{G\_int})$

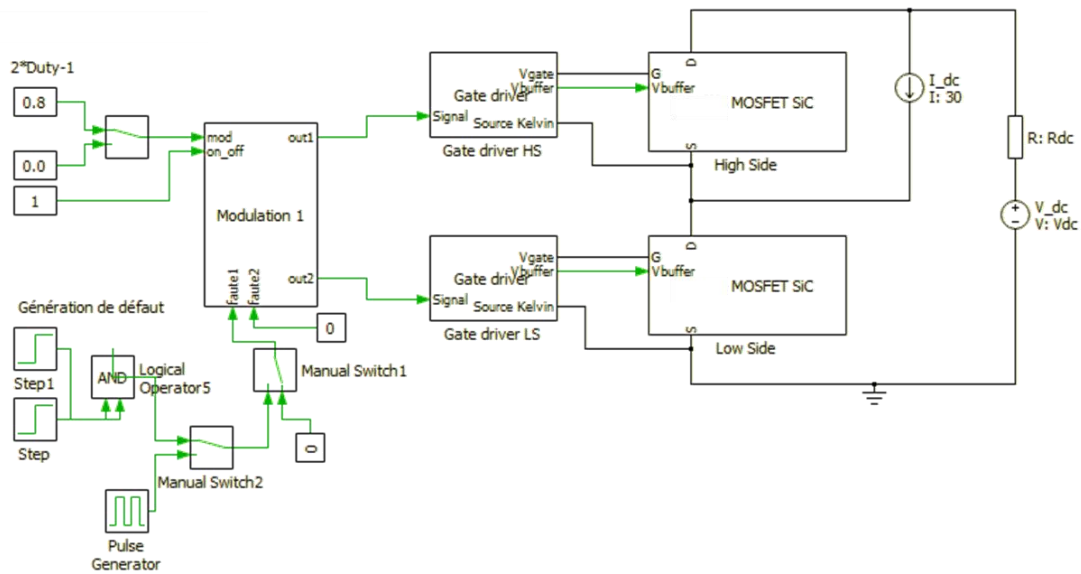
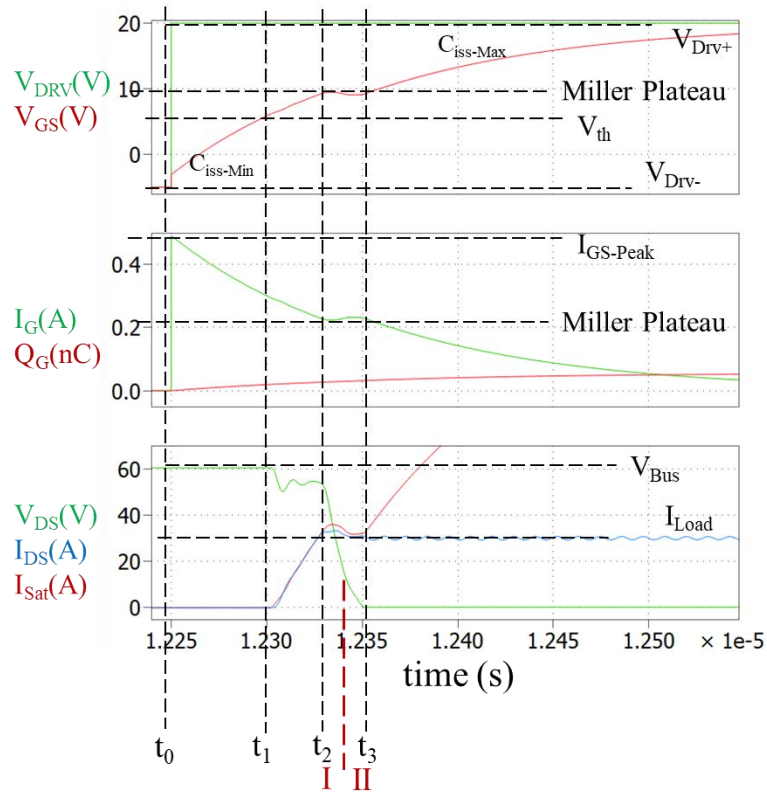


Fig.I. 5. Inverter leg under PLECS



**Fig.I. 6.** Turn-on voltage and current waveforms of the LS MOSFET

Both transistors, HS and LS, are at the dead-time sequence where  $V_{GS-HS} = V_{GS-LS} = V_{DRV-}$  the drain current  $I_{D-LS}$  is zero and the drain-source voltage is high  $V_{DS-LS} = V_{Bus} + V_{Body\_HS}$ ; with  $V_{DRV}$  is the drive voltage. The turn-on waveforms of the low side are shown in Fig.I. 6, where  $V_{GS-LS}$  rises from  $V_{DRV-}$  (-5) to  $V_{DRV+}$  (+20) in four steps. At first, the gate driver provides the voltage command  $V_{DRV}=V_{DRV+}$ , then  $V_{GS-LS}$  rises from  $V_{DRV-}$  to  $V_{th}$ , a gate current flows through  $C_{GS}$  and  $C_{GD-Min}$ , the sum of this capacitors is equal to  $C_{iss\_Min}$ . The  $V_{GS}$  at  $[t_0; t_1]$  has a time-constant  $\tau = R_G * C_{iss\_Min}$ . At this interval  $V_{DS-LS}$  remains equal to  $V_{Bus} + V_{Body\_HS}$  and the drain current at its lowest value, zero. The gate current on the other hand reaches its peak current  $I_{G-Peak}$  considering  $V_{GS}=V_{DRV-}$  and then starts to decrease, eq. (I. 8). Afterwards in the second step  $[t_1; t_2]$ ,  $V_{GS}$  follows the same rise with the same  $\tau$  constant, and the drain current begins to increase according to the linearized transfer curve with a  $\frac{dI_D}{dt}$  slope. At this sequence,  $V_{DS}$  those slightly drop due to the free-wheeling diode and other phenomena by  $2 * L_p * \frac{di_{D\_sat}}{dt}$ . The drain current  $I_D$  follows the  $I_{D\_Sat}$  equation which is given in eq. (I.11).

$$I_{G\_Peak} = \frac{V_{DRV+} - V_{DRV-}}{R_{G-EXT} + R_{G-in}} ; I_{GS1}(t) = C_{iss-Min} \frac{dV_{GS}}{dt} \quad (I. 8)$$

Once the MOSFET is carrying the full load current  $I_{Load}$  added to the recovery current of the freewheel diode if this one is a PIN diode,  $I_D=I_{Load}$ , the  $V_{GS}$  becomes temporarily clamped at a plateau called the Miller plateau if Early effect is neglected, where  $V_{GS}=V_{GS\_M}$ . At this sequence  $[t_2; t_3]$  the gate current is maintained in a plateau as well, due to the reverse capacitor  $C_{rSS}$ , eq.

(I. 9) in the equation below the Miller plateau is considered constant. This causes the drain-source to drop with  $\frac{dV_{DS}}{dt}$  rate. Note that  $I_{Sat}$  is higher than  $I_D=I_{Load}$ .

$$I_{GS-M} = \frac{V_{DRV+} - V_{GS-M}}{R_{G-EXT} + R_{G-in}} \quad (I. 9)$$

$$V_{GS-Miller} = \frac{(2 * C_{oss} * V_{DRV+}) + [C_{GD} * (I_D + g_{fs} * V_{th})]}{2 * C_{oss} + R_G * C_{GD} * g_{fs}} \quad (I. 10)$$

Eq.(I. 10) is given by finding  $I_{G-M}$  expression and merging it with  $I_{D-M}$ , equations below,  $I_{HS}$  is not taken into consideration, in those equations, but added in the main one by taking into account the high side capacitance,  $C_T$  is the capacitor of the depletion zone :

$$I_{D-M} = I_{D-sat} - C_{GD} * \frac{dV_{GD}}{dt} + C_{DS} * \frac{dV_{DS}}{dt} + I_{HS} \quad (I. 11)$$

$$I_{HS} = C_T * \frac{d|V_{GD}|}{dt}$$

With  $\frac{dV_{GD}}{dt} + \frac{dV_{DS}}{dt} = \frac{dV_{GS}}{dt}$  ;  $V_{GS} = Cte \rightarrow \frac{dV_{GD}}{dt} = -\frac{dV_{DS}}{dt}$  (I. 12)

Therefore  $I_{D-M} = I_{D-sat} - C_{oss} * \frac{dV_{GD}}{dt} + C_T * \frac{d|V_{GD}|}{dt}$  (I. 13)

Eq. (I. 14). is giving by replacing  $I_{D-sat}$  by its basic equation

$$I_{D-M} = g_{fs} * (V_{GS-M} - V_{th}) - C_{oss} * \frac{dV_{GD}}{dt} + C_T * \frac{d|V_{GD}|}{dt} \quad (I. 14)$$

Finally,  $I_{GS-M} = \frac{C_{GD} * [g_{fs} * (V_{GS-M} - V_{th}) - I_{D-M}]}{C_{oss} + C_T}$  (I. 15)

Above the Miller plateau was considered constant, for a non-constant Miller plateau  $\frac{dV_{GS}}{dt} \neq 0$ , the Early effect should be considered. The equation  $I_D$  should be changed as well, taking into consideration the Early effect, eq.(I. 16). In the  $I_D$ - $V_{DS}$  characteristic merit curve at the saturation region, the curve shows a positive slope due to Early effect, where  $U_X$  is negative and equal to few volts.

$$i_D = K' * (V_{GS} - V_{th}) * (1 - \frac{V_{DS} - V_{GS} + V_{th}}{U_X}) \quad (I. 16)$$

In addition to these equations, one may replace  $V_{GS-M}$  in the equation (I. 17) to express  $dV_{DS}/dt$ . The decrease of  $V_{DS}$  occurs in two steps. The first step corresponds to the current flow through the active region where  $C_{GD}$  is minimal, then the second step is where the transient is in the ohmic region, and the  $C_{GD}$  is maximal.

$$\frac{dV_{DS}}{dt} = \frac{1}{C_{GD}} * \frac{V_{GS-M} - V_{DRV+}}{R_G} \quad (I. 17)$$

$$\frac{dV_{DS}}{dt} = - \frac{g_{fs} * (V_{DRV+} - V_{th}) - I_D}{(C_{oss} + C_T) + R_G * C_{GD} * g_{fs}} \quad (I. 18)$$

In the last sequence [t<sub>3</sub>; ...] the MOSFET need to maintain the entire load current. V<sub>DS</sub> completely drops to the on-state value of I<sub>D</sub>\*R<sub>DS\_ON</sub>. The gate-voltage resume its growth, but this time with a different time constant  $\tau = R_G * C_{iss-Max}$ . Finally the gate-current decreases towards zero, eq.(I. 19).

$$I_{GS3}(t) = C_{iss-Max} \frac{dV_{GS}}{dt} \quad (I. 19)$$

The free-wheeling diode affects the switching waveforms. The reverse recovery current is slightly introduced in the waveforms (body diode). Its cause the small decrease of V<sub>DS</sub> in the second sequence. Therefore, in the third sequence, the drain current rises above I<sub>Load</sub>; causing V<sub>GS</sub> to increase beyond the Miller plateau. Those increase can be high, but they are present for a short period off time and decrease rapidly when the diode current snaps off and recovers to zero.

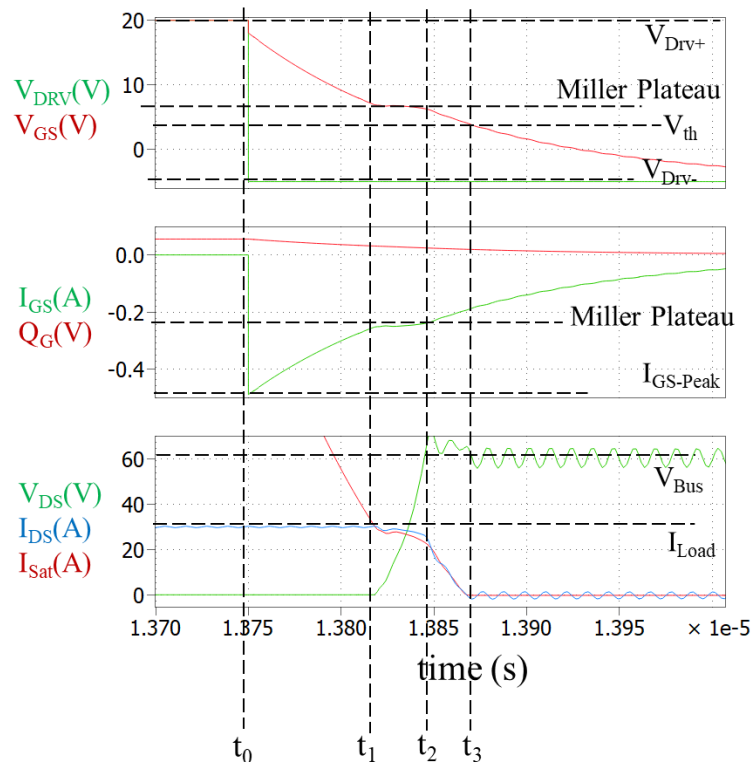


Fig.I. 7. Turn-off voltage and current waveforms of the LS MOSFET

The turn-off of the MOSFET is mostly the inverse sequence of events that occurs during the turn-on, Fig.I. 7. The same basic analytical approach used in the turn-on can be used under the

turn-off waveforms. The value of  $R_G$  used during turn-off may be different from that used during the turn-on.

The turn-off sequence can be cut into four sequences, basically tracking the turn-on steps. The sequences are assured by, the gate-source voltage  $V_{GS}$  drops from  $V_{DRV+}$  to  $V_{DRV-}$  inversely following the turn-on sequence.  $V_{DS}$  goes back to its high value  $V_{BUS}$ , causing the transistor to open. Some of the capacitors are gradually discharged and others charged [18] [19] [20].

The electrical switching results in power losses, which can be divided into two categories. The gate driver losses of the device and the transistors switching losses. As presented in Fig.I. 6 and Fig.I. 7, the total gate charge  $Q_G$  describes the transfer charge amount while the voltage across the input capacitance changes. Therefore, the  $V_{GS}$ - $Q_G$  typical curve characteristic generates the total gate charge. Thus the gate charge losses is given eq.(I. 20), where  $f_{Drv}$  is the switching frequency:

$$P_{Gate} = V_{Drv} * Q_{G|V_{DS_{Max}}} * f_{Drv} \quad (I. 20)$$

On the other hand, the switching losses occurs due to high current and high voltage being present in the device simultaneously for a short period. In order to ensure the least amount of switching losses, the duration of this time interval must be minimized. The only interval time where it is possible; it is the interval time that corresponds to the linear (ohmic) operation of the device. It is when the gate voltage is between  $V_{th}$  and  $V_{GS\_M}$ , causing changes in the current of the device and to the Miller plateau region when the drain voltage goes through its switching transition. Even though the switching transitions are well understood, calculating the exact switching losses is almost impossible. The reason is the impact of the parasitic inductances and capacitances.

The behavior and length of both turn-on and turn-off sequences are a function of the parasitic capacitances values, the parasitic inductance values, the required voltage change across these capacitors, the gate internal/external resistance and the available gate driver current. All this brings into play the importance of the proper component as presented above, and the efficient gate drive design. All of this behavioral study helped us to well identify normal turn-on behavior, which is a key to distinguish between short-circuit behavior and normal turn-on. The short-circuit can be detectable by two means, rather by detecting the short-circuit behavior or by detecting the absence of Normal Turn On NTO. Moreover, the detection circuit should not at any point detect normal behavior.

### 3. Gate Drivers for SiC FETs

This section proposes to demonstrate a systematic approach to design high performance gate drive circuits for high speed switching applications. In order to keep up with the WBG growth, the performances of the gate driver should involve and should face the common design challenges. The main gate driver features are high efficiency, advanced protection and compact solution. With WBG power FETs such as SiC MOSFETs, the gate drivers should also adapt to



their specificities (e.g. gate charge, capacitance values, threshold voltages, voltage range and maximum ratings, high switching speeds, ...)

### 3.1. Gate Drivers fundamentals for power FETs

The primary function of a gate driver circuit is to switch a power semiconductor device from the off state to the on state and vice versa. MOSFET transistors are mainly driven by the high and low voltage between the  $V_{GS}$  [21]. There are mainly two types of control, voltage control and current control. Current control is a technique based on a full H-bridge and an inductive element that reduces control losses by recovering part of the energy used to control the gate of a power transistor. This type of control is very complex for small gains in the order of a watt when using converters with a power of few kilowatt range, and very useful at high switching frequencies [22] [23].

#### 3.1.1. Gate driver functions

The basic topology of the gate driver circuit consists of three fundamental block functions. First, the amplification circuit (buffer and pre-amplification), which provides the gate current and voltages to charge and discharge the input capacitor of the power transistor. The second functionality is the dc gate driver power supply. And last is the isolation. The signal processing and external control circuit that generate the logic level controls signals (FPGA,  $\mu$ processor, etc), which probably needs electrical isolation as well, Fig.I. 8. On the other hand, primary logic circuit is included within the gate driver. Additional functionalities are added with time, to complete the basic gate driver, in different many levels:

- Switching and I/O transmission monitoring
- Health monitoring
- Safety monitoring (device and auxiliary voltage supply)

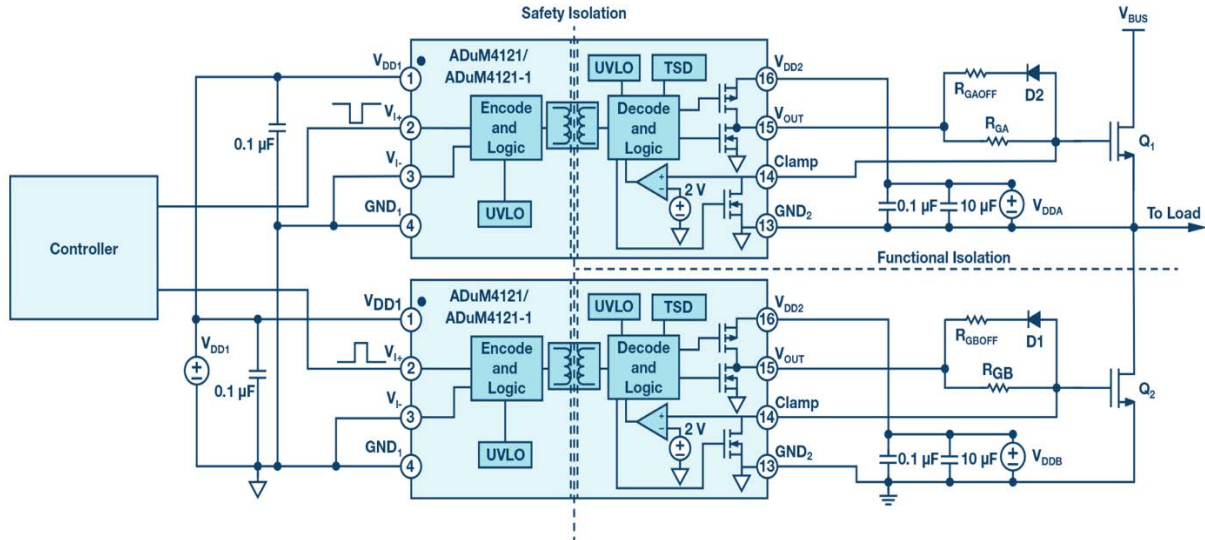
Those functionalities push a large part of the control circuit to merge with the drive circuit. Nowadays, the basic gate driver consists of a variety of function responding to the challenges the WBG devices bring along with their growth. All of this while keeping the low cost and minimization of the gate drivers circuit in mind.

In order to drive the power semiconductors properly, there are few considerations that need to take place. The first consideration is to drive the switch with low switching losses and acceptable EMI/EMC specifications. Which leads us to the first function on the gate driver, the amplification circuit or the output buffer which provides the source/sink current towards the power transistor's gate and source electrodes. The second function on the gate driver, the gate driver power supply, its main function is to provide the gate voltages relatively to the source or Kelvin source electrode. As maintaining the switch in ON state and to make sure that the voltage drop is minimum which corresponds to reducing the conduction losses. As well as maintaining safely the switch in OFF state, in order to minimize the drain-source leakage current and prevent accidental turn-on. Last and not least, one of the important considerations is the noise immunity, in order to tolerate large static and dynamic ground-potential differences and disruptive ground



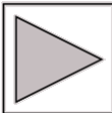
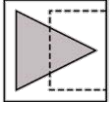
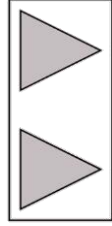
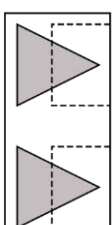
loops in circuit that have high energy. Which brings the importance of the last function, the isolation, separate the power ground and the signal ground.

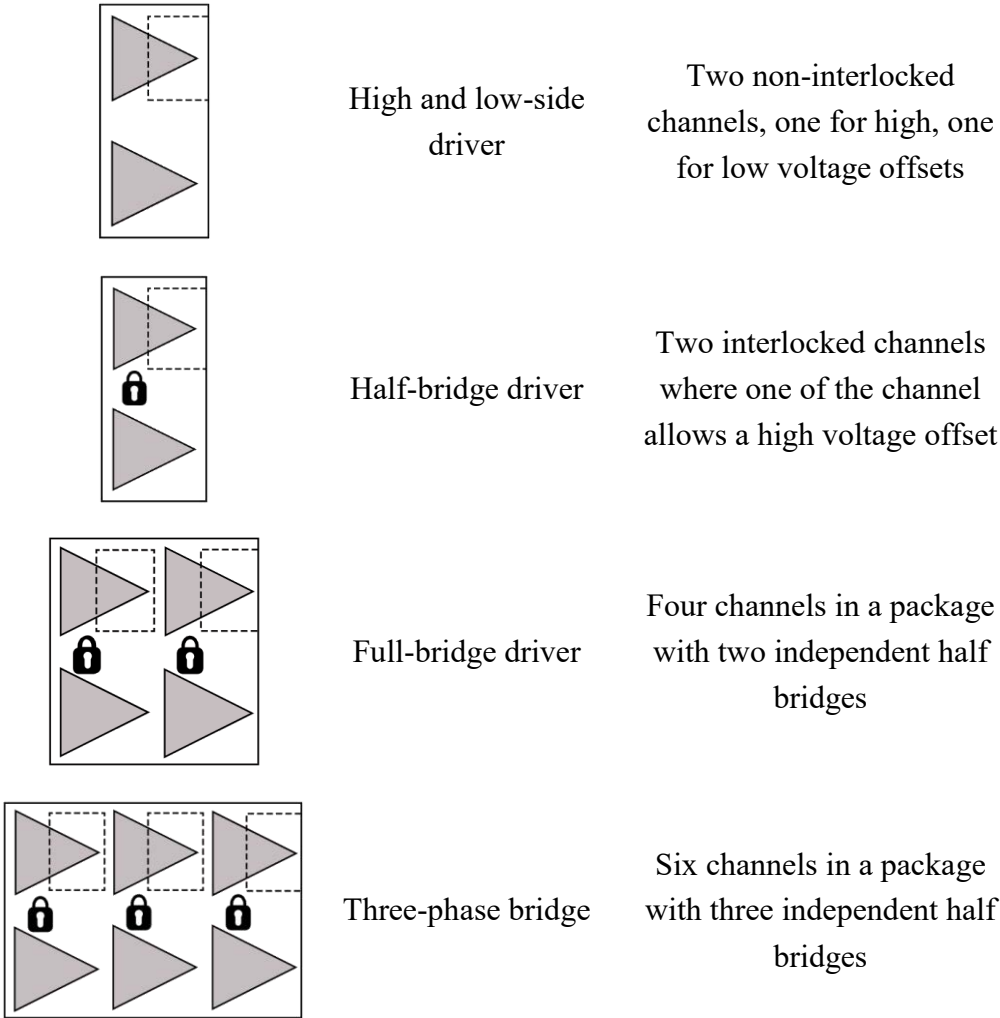
Different gate driver architectures are proposed in the literature adapted to SiC applications, each focused in a different function and with different configurations, in order to have better figure of merits [24] [25] [26] .



**Fig.I. 8.** Block diagram of a synchronous buck converter presenting the essential gate driver functions for the control of both HS and LS (**ADuM4121 isolated gate drivers**)

**Tab.I. 1.** Driver Configuration overview, Infineon [27]

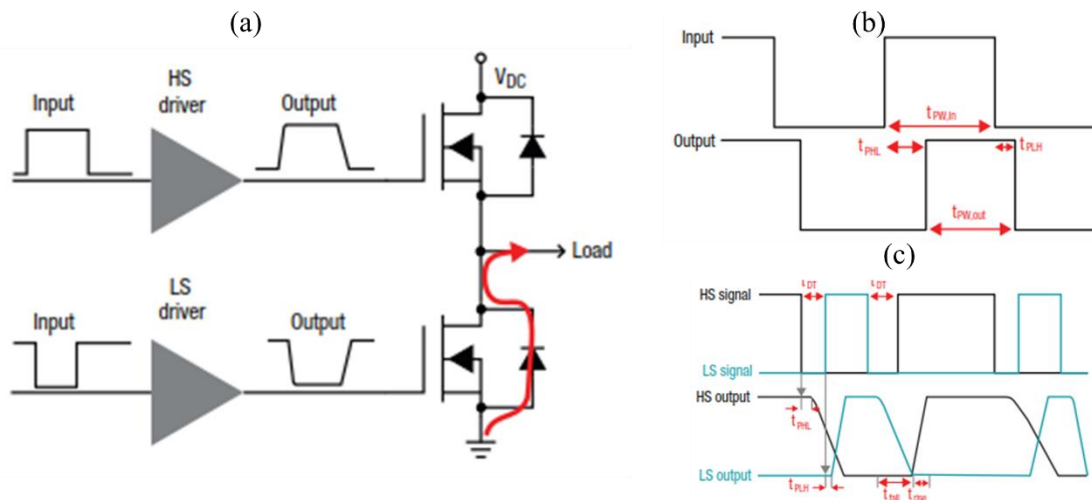
	Types	Definition
	Single-channel low-side driver	Allows low offset of the voltage between input and output
	Single-channel high-side driver	Allows high voltage offset between input and output
	Dual-channel low-side driver	Both channels allow individual low voltage offsets, no interlock
	Dual-channel high-side driver	Both channels allow individual high voltage offsets, no interlock



**3.1.2. Gate driver fundamental parameters**

There are five main important gate driver parameters, which have a big impact on the system. The first one is the negative voltage handling. The negative voltage handling is the ability of the gate driver to withstand negative voltages at the input and output. This negative voltage spikes can result from parasitic inductances from switching transition, leakage or even the poor layout design. The second one is the gate drive source/sink currents, which allows to charge and discharge the gate capacitance power switch. The higher the drive current capability, the faster the capacitance can be charged or discharged. Therefore, being able to turn-on/off a MOSFET quickly, can help to minimize the power switching losses, albeit with higher impacts on EMI (Electro-Magnetic Interference) and EMC (Electro-Magnetic Compatibility) issues. Which leads to the gate driver to source/sink large amount of current. The third one is the delay matching and dead-time management. Dead-time is the period during which neither devices is switched to avoid any potential overlap when they are in half-bridge configuration. As the switching is faster, the dead times are smaller. The management of the dead time between HS and LS is critical, and therefore the classical dispersions on the propagation times between HS and LS can be problematic. Delay matching is where the internal propagation delays between

the channels are matched. The smaller the delays specification, the better performing the gate driver. During the dead time, current flows back through the IGBT or MOSFET body diode, as shown in Fig.I. 9. The body diode has a much larger voltage drop than the device itself, and thus there are more conduction losses. The longer the dead time, the higher the losses, which reduce efficiency and generate heat. Thus, it is best to minimize the dead time by using a gate driver with low pulse-width distortion, low propagation delay, and small rise and fall times. The delay matching and dead-time management provide several benefits. As the paralleled MOSFETs are driven in simultaneous fashion with minimum turn-on delay difference. Other benefit is, it eases paralleling of gate driver output to effectively double current capability and to ease driving parallel power switches. Additionally, rise and fall time may also affect the overlap of these signals, Fig.I. 9. The fourth parameter is  $V_{DrV+}$  the positive supply voltage, and  $V_{DrV-}$  the negative one, which define the operational range of drive outputs. The fifth one is the operating temperature range, which robustness should be satisfied under extreme temperatures.[28]



**Fig.I. 9. (a) Synchronously switched half bridge (b). Pulse width distortion (c). Effect of propagation time [29]**

### 3.1.3. Isolation

The isolation in the gate driver is the electrical separation between various functional circuits such that there is no direct conduction path available between them, Fig.I. 10. This allows individual functions to possess different reference potentials. Signal and/or power can still pass through isolated functions using inductive, capacitive, or optical paths. The isolation can be located in different spots:

- Between the primary logic control (microprocessor / FPGA) and the secondary control (Connected directly to the gate driver).
- Between the power supply of each side, high side and low side.
- Between the low side gate driver and the high side gate driver.
- Between the feedback monitoring flags (detection, protection, control, verification, ...)

Gate drivers can be classified in two main categories with respect to isolation. Non-isolated gate driver, and isolated gate drivers.

Non-isolated technology refers to gate driver ICs utilizing low voltage circuitry, most of them are low-side gate drivers. In other words, the input signal levels of conventional low-side gate driver ICs are referenced to the ground potential of the gate driver IC. For high-side non isolated gate drivers, the direct drive can be generated by a level shifted drive and bootstrap technique. The level shifter is a circuit used to shift the voltage domain. There are 600V level-shifters which transfer the signals to the fully insulated high sides, where the differential transmission signals are filtered and reconstructed. The bootstrap power supply is one of the most common techniques for supplying power to the high-side driver circuitry due to its simplicity and low cost. The bootstrap power supply mainly consists of a bootstrap diode or an active synchronous-diode and capacitor.

The presence of high voltage functions can introduce significant potential differences, which may cause damaging DC currents or unwanted AC currents to flow to other parts of the system of the gate driver. This may cause errors or create hazardous conditions of operation. In these circumstances galvanic isolation is needed. The galvanic isolation is not only used to separate the high voltage side from the low voltage side but they are used for human safety and are mandatory by standards; prevent ground potential differences, or ground loops and improve noise immunity as well. There are multiple topology options available to isolate the gate driver functions,[30] .

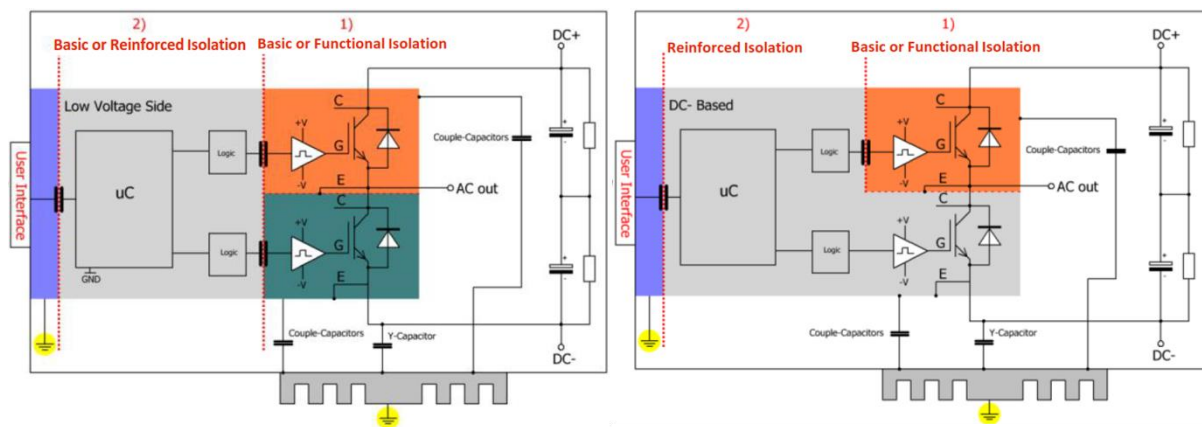


Fig.I. 10. Two Different level topology of isolation, according to IEC 60664-1 and IEC 61800-5-1

There are three primary technologies used for analog and digital isolation of signals today-- optical, inductive, and capacitive, Fig.I. 11. Each technology uses a different insulator material with different dielectric strength. Dielectric strength is a measurement used to describe the maximum applied electric field that a material can withstand without undergoing electrical breakdown and becoming electrically conductive. As for Air the dielectric strength is 1Vrms/ $\mu\text{m}$ , for Polyimide it is 300Vrms/ $\mu\text{m}$  and for SiO<sub>2</sub> it is 500Vrms/ $\mu\text{m}$ , which depends on the conditions of distance, pressure and humidity in particular, etc.

- An optical isolator or opto-coupler consists of an input LED, a receiving photodetector, and an output driver. The driver circuit and LED circuits are typically built using

Complementary Metal Oxide Semiconductor technology, or CMOS technology. Both the input and output of the opto-coupler require a separate voltage supply connected through an anode and collector pins and separate grounds, typically connected through a cathode or emitter pin, in order to maintain signal isolation between input and output. The opto-coupler isolation has high power consumption. An electrostatic shield layer can be also embedded to reduce the common-mode capacitive coupling between inputs (signal and ref.) and outputs (signal and ref.).

- Inductive isolators are based on a magnetic transformer technology or core-less magnetic transmission on silicone /  $Al_2O_3$  substrate. The logic inputs are used to generate an electromagnetic field and to transfer proportional energy signals across the inductive transformer barrier.
- Differential capacitive isolation is based on energy transfer across the silicon dioxide, or CMOS barrier, through a high frequency carrier. A digital input signal is applied and modulated, then communicated across the isolation barrier. A proportional output is then produced to the level of the measured signal at the input. Because capacitive isolators are designed with the highest dielectric strength material for insulation, they offer high data rates, low thermal profiles, and long lifetime operation. The method does not need a power supply and has less power consumption compared to the opto-coupler.

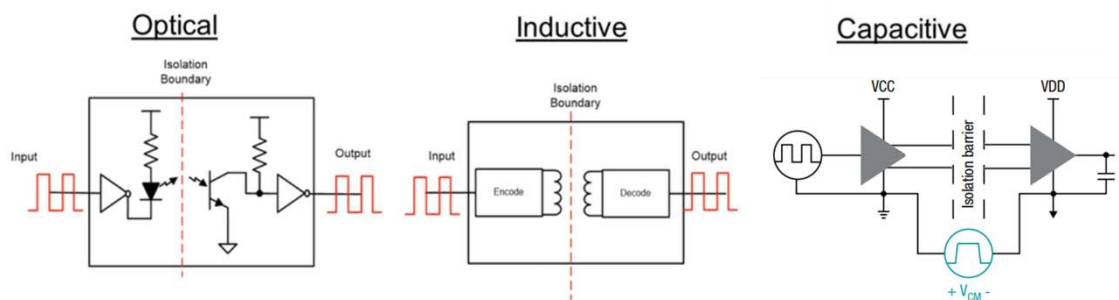


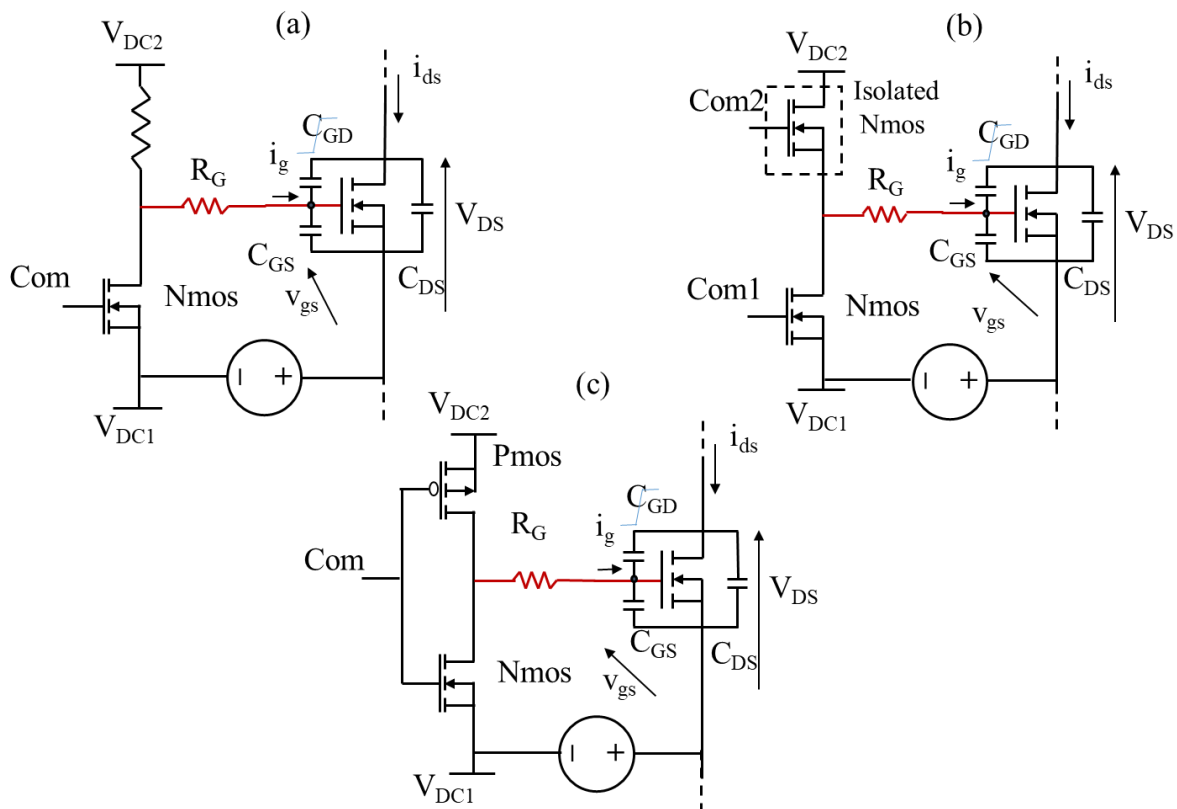
Fig.I. 11. Different isolation technologies [29]

Isolated gate drivers can have different galvanic isolation integrated in different places, depending on its functionality [27]:

- Basic isolation: Certified isolation applied to live parts to provide basic protection against electric shock.
- Functional isolation: Isolation between conductive parts only for the purpose of correct equipment operation.
- Supplementary isolation: Additional isolation to basic isolation as a fallback solution in case basic isolation fails.
- Double galvanic isolation: Certified isolation consisting of both basic isolation and supplementary isolation.
- Reinforced Isolation: single certified isolation applied to live to protect against electric shock.

### 3.1.4. Buffer Architecture

There are different topologies for the output buffer. It depends on different parameters such as the sink/source current, the gate resistor, the type of the used transistors, the voltage levels, ... The most common architectures are presented in this section. Fig.I. 12. presents different inverter structures. The Totem-pole and the push-pull variants structures are the elementary architectures of the output buffer. The inverter of totem pole consists of two identical switches of the same type in serial. The switches can be two NMOSs or two NPNs, which requires two complementary command signals (Com1 and Com2) delayed with a small dead time, Fig.I. 12 (b). On the other hand, the push-pull inverter consists of two opposite switches in series (NMOS + PMOS or NPN+PNP), Fig.I. 12 (c). [18]



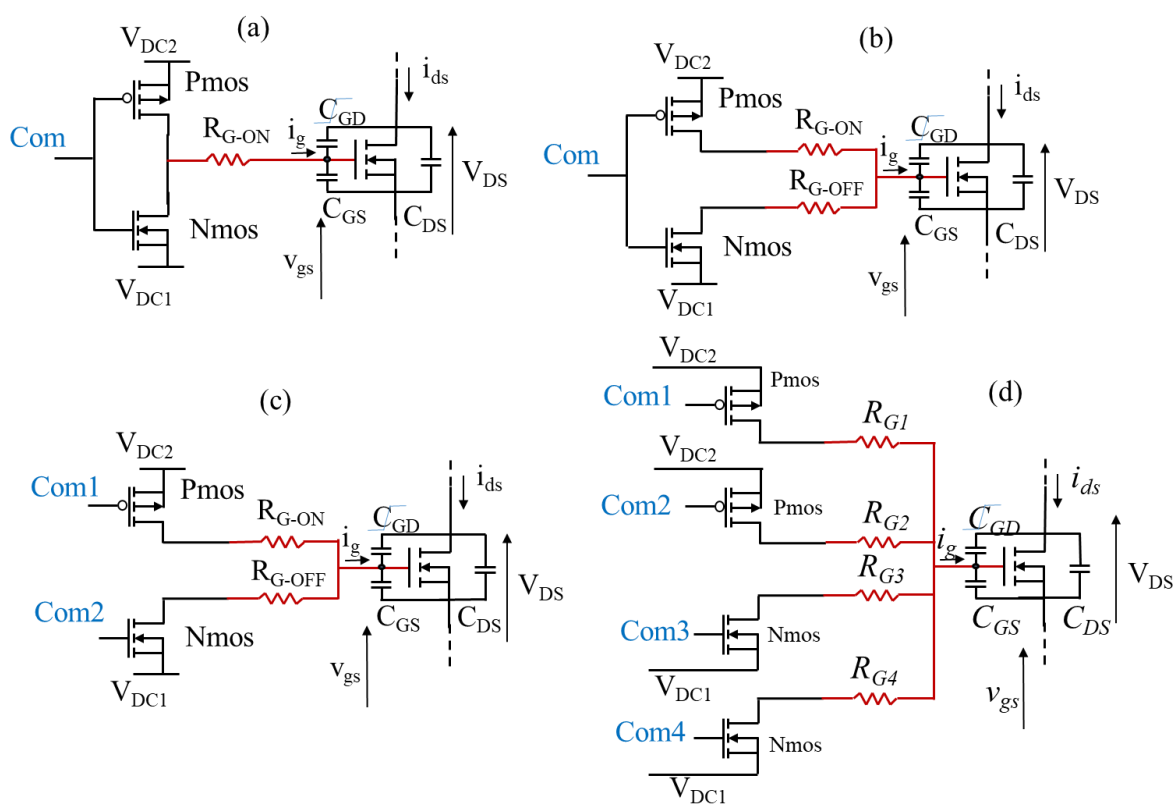
**Fig.I. 12.** Three elementary output buffer structures with a single gate resistance.

These structures are named non-differential 2-level buffers and require two power supplies or with the possibility of having the lower one two the ground, which makes it only one gate power supply. The command signal requires a generation of an internal dead time for the buffer, driving one power transistor. Moreover, the structures are presented with one resistance. Nevertheless, it is interesting to dissociate the gate resistance into two elements, where each resistance is in series with a switch (HS and LS), Fig.I. 13.(b). In addition to dissociation the turn-on resistance  $R_{G\_ON}$  from the turn-off resistance  $R_{G\_OFF}$ , the absence of internal dead time in the driver is allowed. The short-circuit current is limited by the presence of the two resistors. In a Push-Pull configuration, are complementary, this allows the use of only one control signal,



Fig.I. 13.(b), also known as split output buffer. The separation of this commands signals allows more flexibility on the dead time behavior, Fig.I. 13.(c), and easy settings of different gate resistors for turn-on and turn-off.

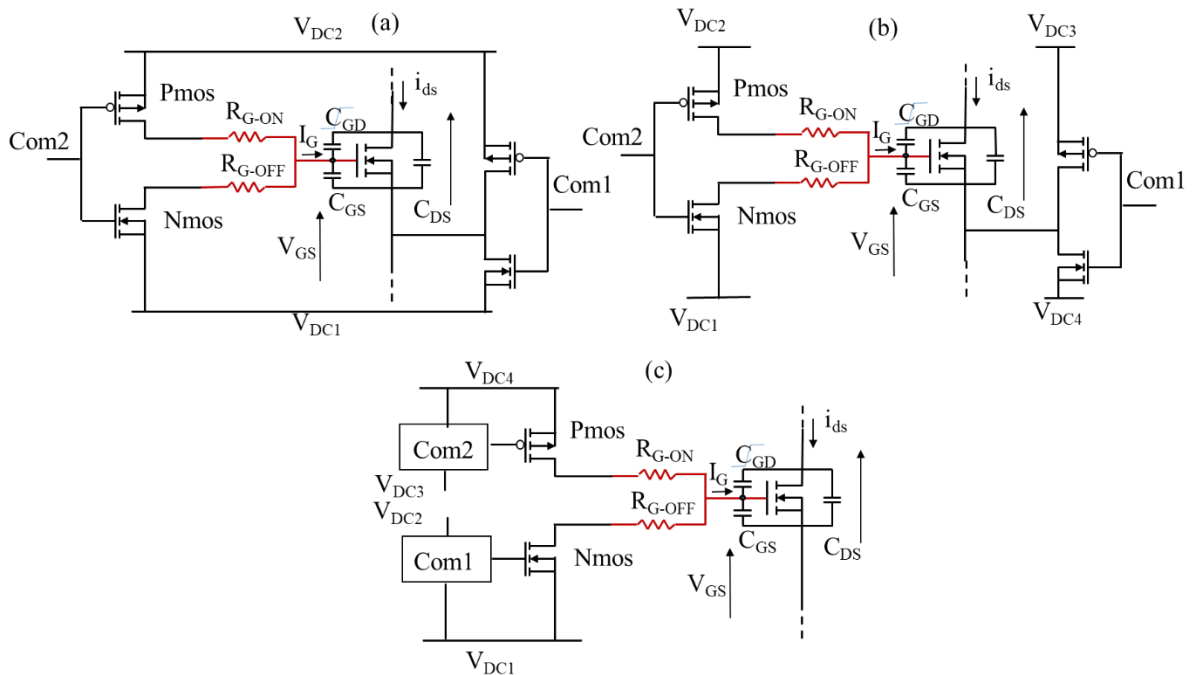
Fig.I. 13.(d) presents a different structure with separate gate resistances for the PMOS and NMOS, which allows more flexibility to control the gate current [31], also known as segmented buffer. Several slew rate control methods have been designed to adapt the charging/discharging speed of  $C_{iss}$ . The capacitor charging/discharging speed is affected by four aspects, which are: gate driver voltage, gate resistance, gate current, and  $C_{iss}$ . Consequently, the AGD (active gate driver) methods can be divided into four different methods: variable gate resistance method, variable input capacitance method, variable gate voltage method, and variable gate current method. These methods will be further developed in the section below.



**Fig.I. 13.** Four elementary output buffer structures with a several gate resistances.

The illustrated structures offer only two output voltage levels,  $V_{DC1}$  and  $V_{DC2}$ , in other words  $V_{DrV+}$  and  $V_{DrV-}$ . Fig.I. 14 presents different named differential 3-level architectures, with the flexibility to change the output voltage levels and therefore the gate to source voltage levels of the power transistor. Fig.I. 14 (a) and (b) presents the H-bridge structure, the benefit from this structure is the possibility to have three or even four output voltage levels,  $V_{DrV+}$ , 0,  $V_{DrV-}$ , and another intermediate level. With these structures the split gate resistance or the split command is mandatory. These structure applies a different voltage level at the gate and the source of the power transistor with only a reduced number of power supply. Fig.I. 14 (c) presents a last structure with two output voltage levels  $V_{DrV+}$  and  $V_{DrV-}$ , but in this structure the commands of

each side is supplied with different power supplies. In other words, structures in Fig.I. 14 (a) and (b) are limited at the power supply voltage, if the gate oxide of the PMOS and NMOS does not support the same power supply voltage. As an example if  $V_{DC2}$  in (a) and (b) is equal to 20V the  $V_{GS-PMOS}$  of the PMOS should support the 20V. Therefore, Fig.I. 14 (c) is an alternative to use the split power supply ( $V_{DC1}$ ,  $V_{DC2}$ ,  $V_{DC3}$ ,  $V_{DC4}$ ) which allows the use of transistors with less gate breakdown voltage.



**Fig.I. 14.** Three elementary output buffers structures with split gate resistance, and split power supply.

### 3.2. SiC MOSFET power device and the challenges faced by the gate driver

The emerging of SiC MOSFET is an attractive replacement of Si IGBT for high voltage and high power density applications. Due to the similar MOS gate structure, the gate drivers for SiC MOSFETs can directly inherit from the Si IGBTs various functions. However, the high switching speed with increasing  $dv/dt$  and  $di/dt$  ratios makes the gate driver design for SiC MOSFET new challenges. The high  $dv/dt$  and  $di/dt$  may lead to parasitic effects including phase-leg crosstalk and Electro-Magnetic Interference (EMI) issues due to the ringing. Therefore, the gate driver design for SiC MOSFETs should follow such features:

- Negative gate driver power supply to avoid crosstalk in half-bridge configuration;
- A low impedance path for faster turn-off and suppression of crosstalk;
- A small gate loop inductance to reduce the gate-source voltage ringing, especially the common source inductance should be minimized to reduce the interference between the two loops;



- A small power loop inductance to reduce the ringing of drain-source voltage and drain current with the low-ESL (equivalent stray inductance) decoupling capacitance placed as close as possible.
- High gate source/sink current for fast switching

Moreover, the short-circuit SC withstanding time for SiC MOSFETs is shorter than Si IGBTs. Short-circuit faults are the most critical failure mechanism in power converters, which may result from the controller fault, device failure breakdown, or load short-circuit. Due to the excessive power dissipation during the short-circuit transient, the device junction temperature may easily exceed the limit and lead to thermal runaway and fail-to-short permanent failure, sometimes explosion. The device manufacturers normally specify a short-circuit withstand capability, which is the amount of time from the start of short-circuit fault until the device exhibits a sign of irreversible damage.

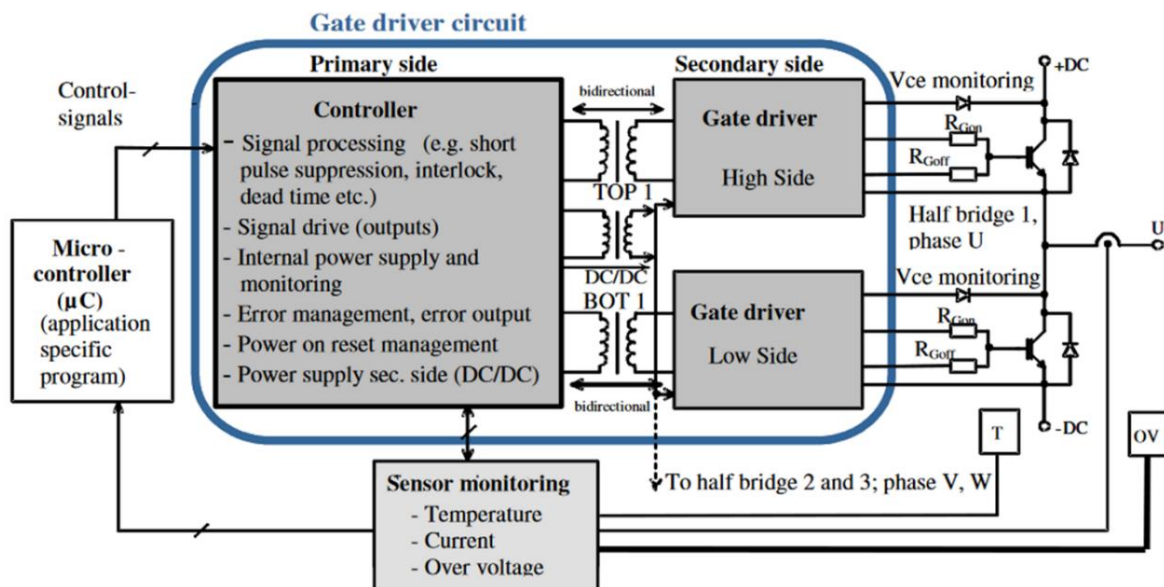


Fig.I. 15. Principle topology of monitoring [32]

In order to maximize switching performance with lower switching losses, the drivability should be enhanced. The work of this thesis is focused on monitoring oriented safety and oriented switching and transmission. Several buffer structures can be proposed to further enhance and overcome the challenges faced by the SiC MOSFETs [33], or GaN power devices [34]. Moreover, different functions can be added in the gate driver. These functions and structures can be classified in three categories, switching and transmission monitoring, safety monitoring and healthy monitoring. These monitoring includes:

- Dead-time management and switching time monitoring [7],
- Voltage control and measurement ( $dV_{DS}/dt$ ,  $V_{DS}$ ) [36], overvoltage protection,
- Current control and measurement ( $dI_D/dt$ ,  $I_D$ ) [37], overcurrent protection [3], peak gate current measurement,
- $dV_{DS}/dt$  and  $dI_D/dt$  monitoring [38],

- Gate charge monitoring,
- Thermal monitoring and junction-temperature measurement [39] [40],
- Driver power supply monitoring levels [41],
- Short-Circuit monitoring, and protection,
- State information diagnosis,
- Other monitoring and diagnostic...

These monitoring/diagnostic and protection functions, can be bi-directional with the power transistor and the driver or bi-directional inter-driver, Fig.I. 15, [32] .

Programmable digital gate drivers are actively studied in recent years. In these programmable gate drivers, the switching characteristics of a power device can be actively controlled based on implementation and operation conditions [42], [43].

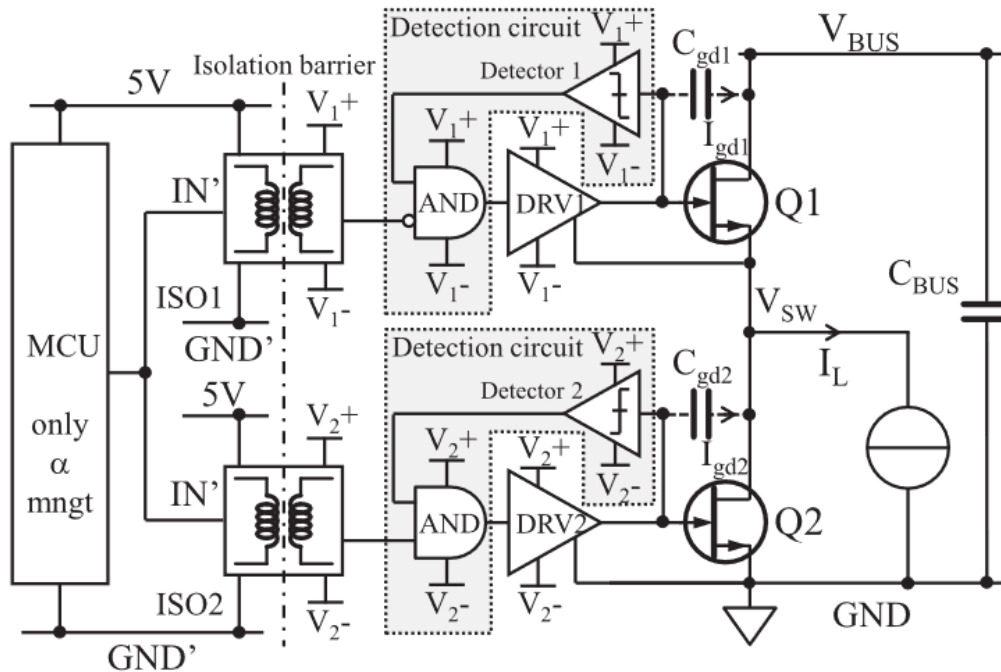
### 3.2.1. Switching and transmission monitoring

In order to insure the right drivability of a SiC MOSFET, few key requirements should be considered. The first requirement is to have a high output drive voltage between 20-35V. Silicon carbide MOSFETs, like silicon IGBTs, have thick gate oxide to enable high voltage operation. SiC MOSFETs have been designed to be driven between +15V to +20V, the extra voltage drive capability ensures that the driver provides high noise immunity High voltage driving capability, implies lower ohmic resistance of the power switch, which on the other hand reduces the conduction losses and increase the power efficiency. Silicon carbide MOSFETs typically have a low turn-on threshold voltage, typically between 2 volts to 5 volts. SiC MOSFETs are driven with a negative gate to source voltage as well. With the gate voltage below the source voltage in the turn-off condition, false turn-on event can be avoided because much more additional charge needs to be transferred into the gate in order to bring the gate potential as high as the turn-on voltage of the MOSFET.

In order to further improve the system efficiency, smaller propagation delay is required for SiC MOSFET drivers. During the dead time, the current can be conducted through the body diode of the MOSFET. Silicon carbide MOSFET body diode has a relatively large voltage drop, which causes significant energy loss in each switching cycle [44]. The minimum dead time depends on the pulse width distortion of the input signal, where the pulse width distortion is determined by the propagation delay mismatch of the rising edge and the falling edge. With smaller propagation delay (low propagation delay mismatch), the smaller can be the dead time, which reduces power loss through the body diode of the power transistor. Smaller propagation time enhance the response time of the feedback from a diagnostic or a monitoring, allowing to intervening as quickly as possible.

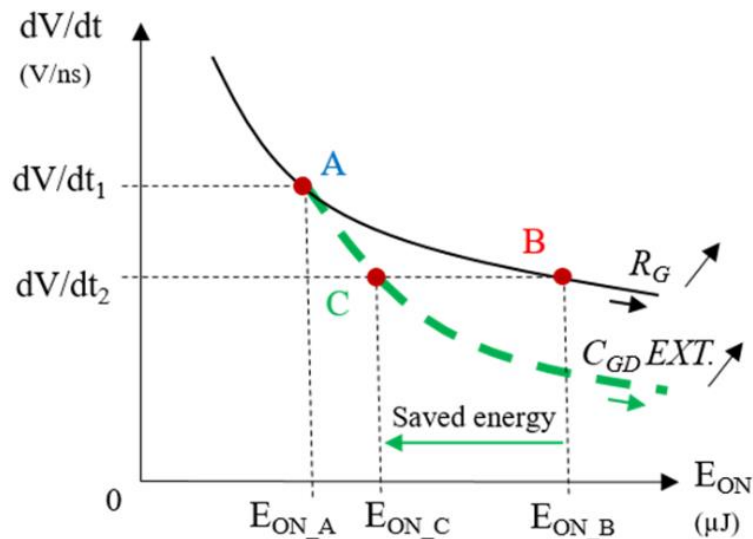
The dead time monitoring starts to be essential for SiC MOSFETs. Dead time are required to avoid simultaneous conduction of high-side and low-side power transistors, and simultaneous activation/deactivations of the gate driver output switches. In the literature [45] adapted and controlled dead time are proposed. The proposed dead time generator is based to detect the

reverse conduction mode directly on the gate side of power transistors by taking advantage of the gate-to-drain parasitic capacitance. In this way, dead-times are generated and managed closer to power transistors by each isolated gate driver instead of the MCU. Moreover, with this particular dead time management, the only limiting factor in dc to raise the maximum operating voltage is the breakdown voltage of power transistors and characteristics of isolation barriers.



**Fig.I. 16.** Circuit schematic of the synchronous buck converter implementing a self-switching technique at turn-on to safely generate reduced dead time [45].

The detection-generation circuit of the dead time management is proposed in Fig.I. 16 [45]. Several sensing methods to detect both derivatives  $dV/dt$  and  $dI/dt$  are also proposed in the literature [46] [47] [48]. Since WBG power transistors turn-on faster, a larger amount of electromagnetic emission (EMI) is generated and can interfere with the systems close by. Therefore, several techniques to reduce  $dV/dt$  (and so undesired EMI effects) are being investigated in the literature [46] [47]. The classical trade-off between the output voltage switching speed of a power device  $dV/dt$  and switching losses  $E_{ON}$  is presented in Fig.I. 17 [36]. Classically, the gate resistor  $R_G$  is adjusted to obtain a good balance between EMI performance (related to switching speed) and switching losses. A low  $R_G$  value reduces switching losses but increases the  $dV/dt$  value (point A. in the figure compared to point B). As a consequence, the Common Mode Transient Immunity (CMTI) of signal and power isolators are pushed further, and EMI issues can dramatically degrade the operation of power converters. Higher  $R_G$  values are then used to reduce the  $dV/dt$ , leading consequently to higher losses (point B in Fig.I. 17). Thus, innovative techniques are required to reduce at the same time the switching losses and the  $dV/dt$ . Using the proposed approach, presented hereinafter, point C of Fig.I. 17 can be reached, where  $dV/dt$  is reduced with a limited increased of  $E_{ON}$  [36].

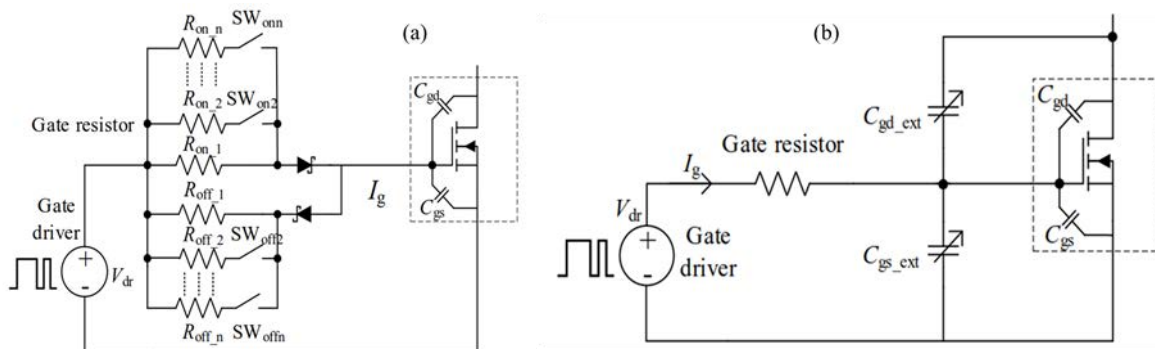


**Fig.I. 17.** Trade-off  $E_{ON}$  vs  $dV/dt$  function of  $R_G$  (solid line) or  $C_{GD}$  (dashed line) values for constant  $V_{HV-DC}$ ,  $I_L$  and temperature [36].

Still in the slew rate control monitoring, but this time the monitoring is located at the gate of the power transistor. Several slew rate control methods have been designed to regulate the charging/discharging speed of  $C_{iss}$  [31]. The switching speed can be summarized by four aspects, gate current gate resistance, gate driver voltage and  $C_{iss}$ , as mentioned above in chap.I.3.3.4, where few structures have been presented. In order to furthermore have a large controllability over the WBG power transistors more structure are proposed in Fig.I. 18.

Fig.I. 18.(a) presents the typical circuit of a variable gate resistance method. The variable gate resistance method is implemented by connected many gate resistors in parallel to regulate  $dv/dt$  and  $di/dt$ . In other words, the gate resistance of the driver is changed for different stages during the switching process for slew rate control. Fig.I. 18.(b) presents a pre-idea of a variable input capacitance circuit [49]. This method is based on adding an extra capacitor in parallel with either gate-source, or Miller capacitance which results in regulating the charging speed. Different techniques are presented in [50], [51].

Another method based on having a variable gate current is illustrated above in Fig.I. 13.(d). This method is based on putting in parallel the switching commands with different gate resistance and a controlled logic to choose how much switches to use, in order to source/sink more or less current. Other structures are illustrated in [52], [53].



**Fig.I. 18.** Equivalent control slew rate circuit (a). Variable resistance (b). Variable capacitance [49]

### 3.2.2. Health monitoring

Discrete power switches and power modules are designed to operate within a certain temperature range – typically  $-50^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  – due to packaging material limitations and avalanche issues. However, power losses caused by switching and conduction losses will cause the die to heat up, resulting in its damage over time or complete destruction. The environment where the device operates may include extreme heat, which can also contribute to excessive die temperatures. Gate drivers for SiC MOSFETs can have a switch temperature sensing feature to provide thermal shutdown for the power MOSFET. The threshold temperature can be pre-set to shut down the device at a certain temperature in applications requiring advanced switch protection. It is also critical to prevent a silicon carbide MOSFET from overheating in high temperature applications [39] [40] [54]. Temperature is typically monitored using a thermistor or thermal diode. Negative temperature coefficient (NTC) thermistors often monitor temperatures in IGBT power modules, and are integrated to be physically close to the devices in order to provide the most accurate readings [29],[55] (AlGaIn/GaN HEMT).

Other than temperature warning and shut-down, the Gate driver can be oriented in different test and diagnosis and checks in order to insure a healthy operation. As what NXP propose with it MC33GG3100 gate driver,[56]. As the one can find in the literature as well [57].

- Built-in self-check and built-in self-test (BISC and BIST) of all analog and digital circuits
- Continuous watchdog of die-to-die communications
- Built-in self-diagnosis (BISD) of  $V_{\text{DS}}$ ,  $V_{\text{GS}}$  and  $I_{\text{GSS}}$
- $V_{\text{GS}}$  real time cycle-by-cycle monitoring (at the on-state and off-state)

Aging of the power component can be as well monitored [49] [58]. Paper [48] presents a comprehensive study on degradation monitoring of SiC MOSFETs and proposes an early warning method to detect aging.

Other indirect-monitoring techniques can be introduced to the power component in order to extend its lifetime. One of the best way to extend the lifetime of the SiC MOSFET is by improving the short-circuit robustness of the SiC MOSFET. The objective is to optimize the design structure to reach a  $t_{\text{sc}}$  (short-circuit withstand time) higher than  $10\mu\text{s}$ , in order to be able to re-use the same IGBT protection circuit proposed in the literature. [61] presents the possibility of optimizing the doping levels in the channel region to find the best  $t_{\text{sc}}$  vs  $R_{\text{DS\_ON}}$  trade-off. Four parameters were studied separately:

- reduction of the source doping (N+ depletion) from 100% to 3.3%;
- reduction of the channel width (section reduction per  $W_{\text{ch}}$ ) from 100% to 29%;
- increase of the doping of the double diffused channel box (over-doping of the P region and desensitization of the channel inversion zone) from 100% to 200%
- depolarization of the grid from 20V to 12V.

The results are presented in Fig.I. 19 . A classical design for a 1.7kV leads to a  $t_{\text{sc}}$  of  $3.6\mu\text{s}$  and  $I_{\text{sat}} 10 \cdot I_{\text{N}}$ . By depleting the N+ doping by a factor of 1/30th the  $t_{\text{sc}}$  increases to  $11\mu\text{s}$ .



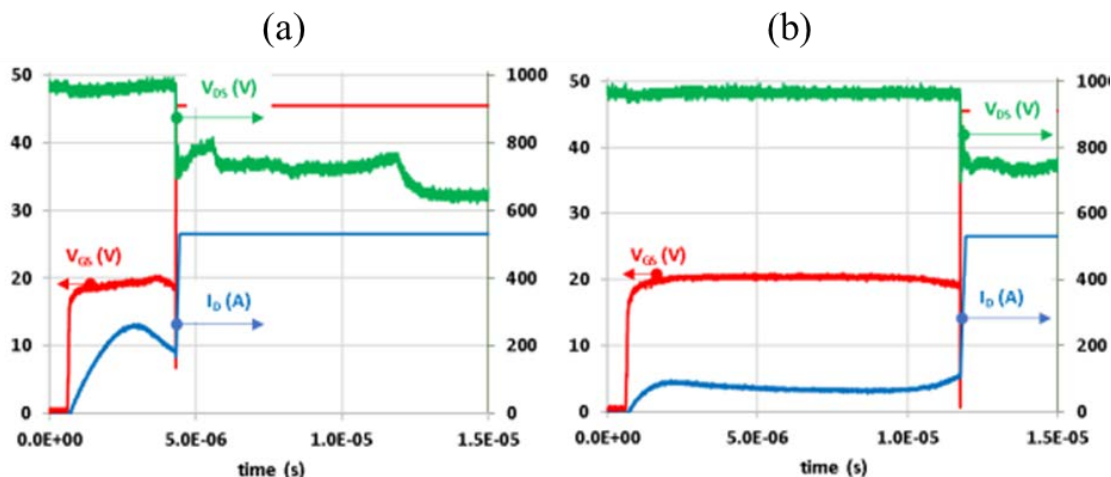


Fig.I. 19. (a). Classic test. (b). Modified test [61]

This objective to increase  $t_{sc}$  is being actively pursued by other manufacturers such as ABB, and Semiconductor Components Industries, LLC. This last manufacturer proposes a natural limitation of the saturation current. The idea is to co-integrate in the same chip a VDMOS and LDJFET normally-on in the gate region (between the channel and the source). The LDJFET depolarizes the VDMOS grid in overcurrent mode like a cascode limiter but keeps control over the main grid electrode of the VDMOS, Fig.I. 20. Patent number US 10,504,995 B1 (10/12/2019). In this article [62], this technique is applied and shows promising results.

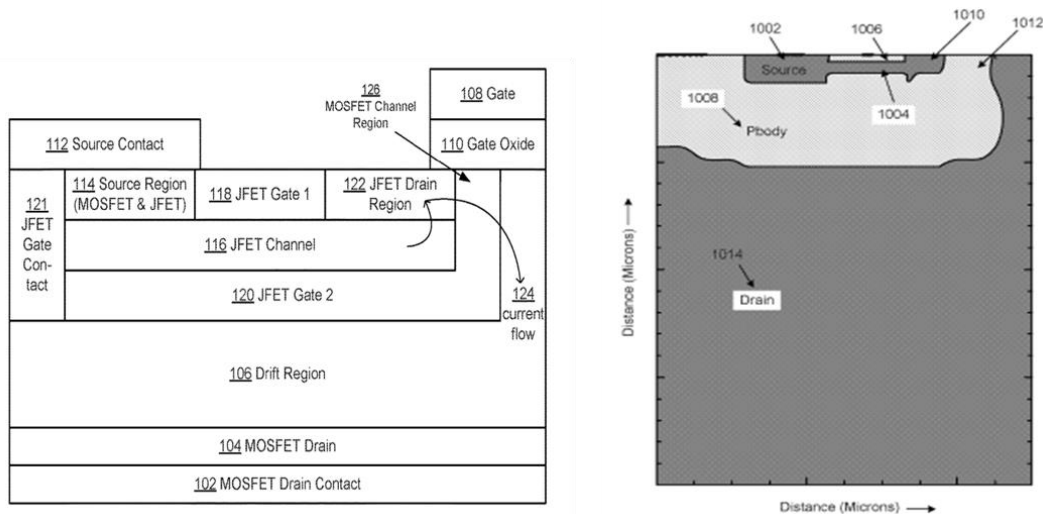


Fig.I. 20. Co-integration VDMOS and LDJFET “Patent number US 10,504,995 B1”

### 3.2.3. Safety monitoring

One of the common problems faced by WBG power devices is parasitic turn-on due to the Miller capacitor  $C_{rss}$  and to the  $V_{GS}$  coupling. A high  $dV/dt$  transient created during turn-off can induce parasitic turn-on, spikes at the gate voltage and possible ageing of the oxide, Fig.I. 21. In order to avoid these spikes, the current flow through  $C_{rss}$  at this high  $dV/dt$  at the turn-off should be sunk with the lowest impedance [63] or using a negative gate-bias but this technique well known in Si can cause an accelerated  $V_{GS-th}$  drift and additional electric field stress through the SiC MOSFET oxide. An additional  $C_{GS}$  will shunt the  $R_{G\_off}$  path, but on the other hand

will affect the switching speed and losses. The measure taken in this case to prevent this unwanted spikes is by shorting the gate-source path. This can be achieved by an additional transistor between the gate and source of the power transistor. This technique is called Active Miller Clamp AMC [64]. Note that the  $R_{DS\_ON}$  of the AMC should be lower than the gate resistance. Therefore, the occurring currents across the Miller capacitance are shunted by the transistor instead of flowing through the output driver. The AMC will be further discussed in chap.II.

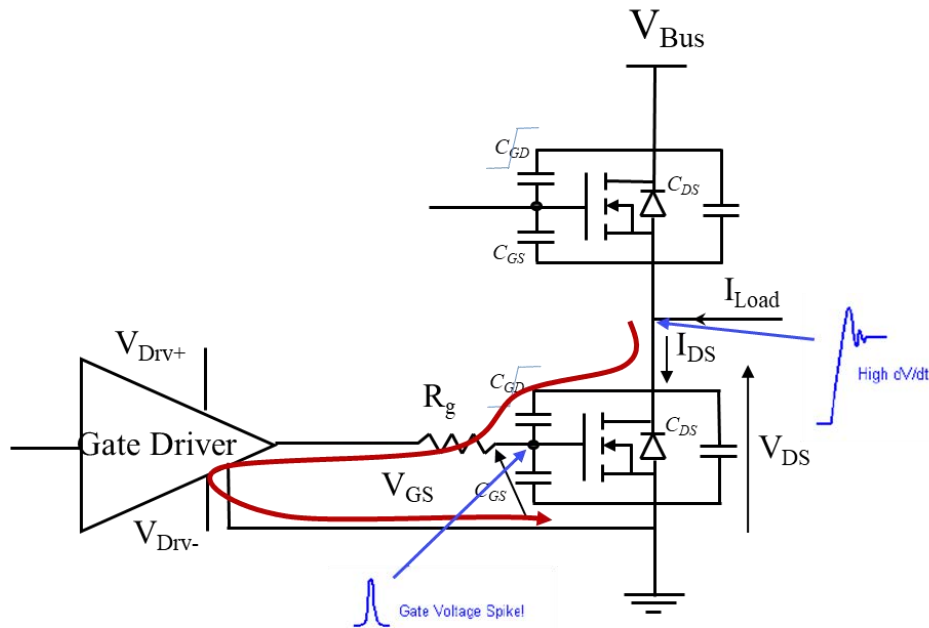


Fig.I. 21. Low-side parasitic turn-on, and current flow due to the Miller capacitor.

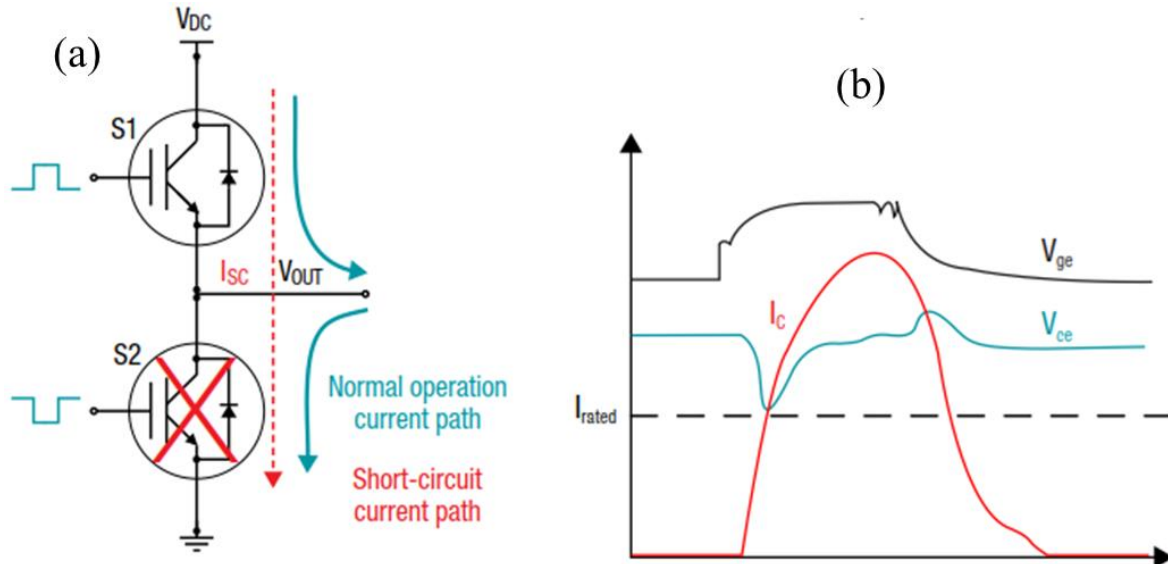
Other than the WBG transistor getting affected by high  $dV/dt$ , WBG transistors suffers from severe short-circuit SC. Due to the popularity of Si IGBT in the modern power converters, its short-circuit protection has been extensively investigated. The device manufacturers normally specify a short-circuit withstand capability, which is the amount of time from the start of short-circuit fault until the device appears damaged. The SC withstand time  $t_{SC}$  can be determined by the critical energy, which means the minimal dissipated energy leading to device failure fore one SC pulse. The energy dissipation during a SC is given in eq.(I. 21), [65].

$$E_C = \int V_{DS} * I_D * dt \quad (I. 21)$$

The short-circuit current is limited by  $V_{DC}/R_{DS\_ON}$  and device saturation current, whichever is smaller. The stray inductance  $L_S$  has a direct impact on the overshoot voltage at turn-off, where  $V_{DS}$  increases at a higher voltage compared to  $V_{Bus}$  for a short period. Fig.I. 22 presents waveforms under hard switch fault.

Regardless of the short-circuit robustness, the device must be turned OFF as soon as a SC is detected to preserve the device from degradation. The short-circuit (SC) withstand time for SiC MOSFETs ( $2\mu s$ ) is lower than for silicon devices ( $10\mu s$ ) [65], [66] [67].

Therefore, the SiC MOSFETs gate driver compared to the Si IGBT ones have lesser time to detect the SC and to protect the power device and to avoid ageing of the chip. A clear and detailed comparison between SiC MOSFET and Si IGBT behavior under short-circuit is presented in the section below. Different monitoring and protection methods for SiC MOSFETs are investigated and developed.



**Fig.I. 22. (a).** Hard switch faults half bridge with non-overlapping inputs, **(b).** Waveforms of S2 during a short-circuit event [29]

A fast detection system is needed to turn-off the power transistor, in order to avoid self-heating of the power chip and to prevent drain overcurrent which could potentially result in the destruction of the device. Several circuits have been proposed to protect safely the power device. The well-known circuit goes by the name of soft shut down SSD. The SSD circuit consist of a transistor commanded by the flag of SC detection and consists of a large resistance  $R_{SSD}$  to smoothly discharge the gate of the power device, after the detection of SC occurs, Fig.I. 23.(a). Fig.I. 23.(b) presents a two stage turn-off circuit [19]. This protection circuit complement the SSD circuit with an additional resistor  $R_{Clamp}$  which is much smaller than  $R_{SSD}$ , and a zener diode  $Z_{Clamp}$ . With both resistors the two stage soft turn-off is achieved. The use of such a clamp diode allows to discharge the gate current faster from  $V_{Drvt}$  to a threshold level determined by the designer. The discharge will be first by  $R_{Clamp}$  and then when  $V_{GS}$  reaches the threshold set, the RSSD will be activated to further more discharge softly  $V_{GS}$ ; in order to completely turn-off the device. Another turn-off strategy is proposed in [68].

Different monitoring methods have been investigated to keep up with WBG growth, to maximize SiC benefits, to assure a safe switching operations and to protect the device. Other functions included in the gate driver towards a smart driver are investigated here, [69], [70],[71] [72]. A recent overview of SiC MOSFET gate drivers is presented in [73].



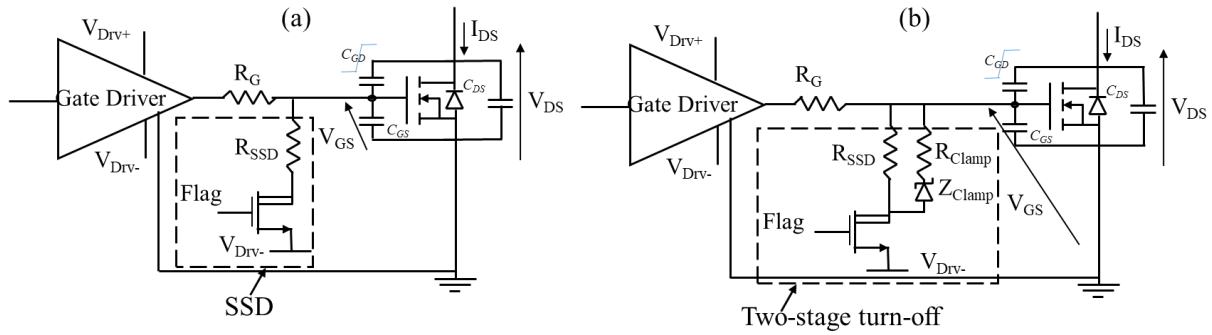


Fig.I. 23. Different protection circuits

### 3.3. Technology review

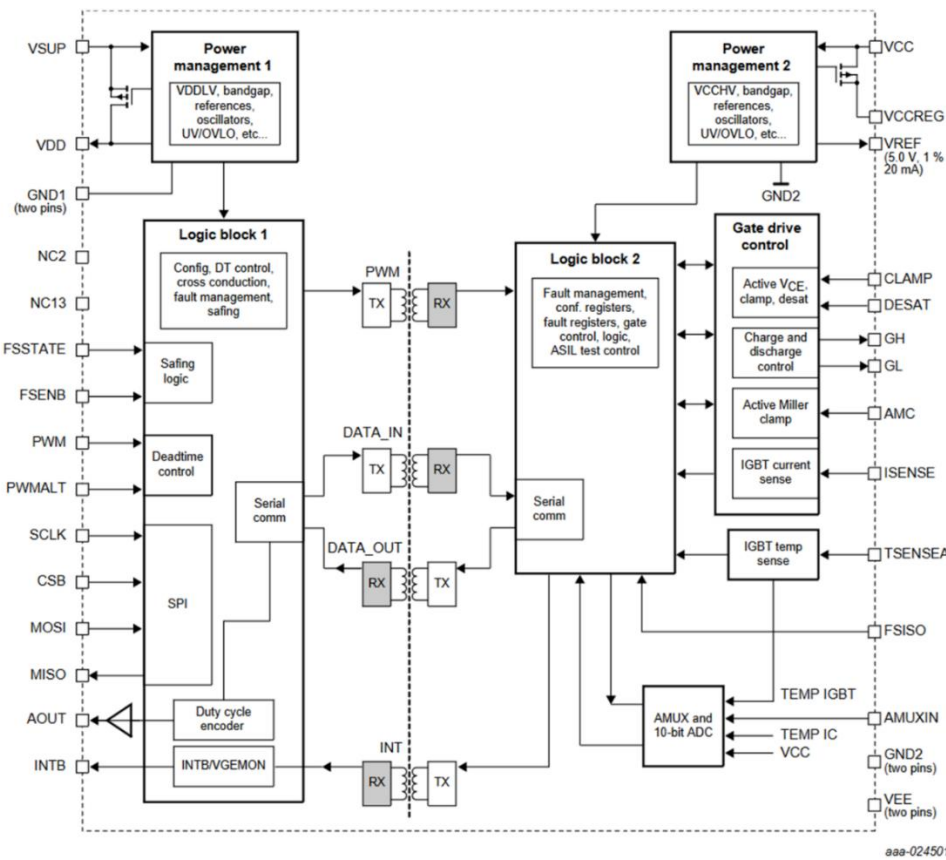


Fig.I. 24. Internal block diagram of a single channel gate driver, MC33GD3100 NXP, [56]

Different monitoring topologies have been discussed above. Semiconductor companies oriented gate driver make sure to implement more sensors and monitoring functions, in order to handle critical operation modes, and to keep the device within the specified safe operating area. One of the recent advanced SiC gate driver is presented in Fig.I. 24, [56]. NXP one of many other companies ensure the growth trend of SiC MOSFETs. The **MC33GD3100** has an integrated galvanic isolation, as many other manufacturers such as Silicon labs, analog device or Infineon, etc. Isolated gate driver functions can be isolated with a circuitry (as presented above) or within the layout. The layout fabrication techniques are proposed by Infineon (developed below), and many other different industrials. But before developing layout isolated

techniques, some brief gate driver topologies is presented in Tab.I. 2. Tab.I. 2. summarizes the different techniques for insulation, signal and energy transmission in dependence on the application range, [74].

**Tab.I. 2.** Gate driver topologies, insulation and transmission principles depending in application range [75]

Driver type [74]	Insulation	Signal transmission	Energy transmission	Application
<b>IC drivers (single, Half bridge, etc)</b>	No galvanic insulation	Integrated level shifter, Coreless transformer or HV capacities	Bootstrap-circuit	Low power (<5 kW)
<b>Hybrid driver (Single, half bridge, etc)</b>	Galvanic insulation	Optic pulse transformer Optic fiber	DC/DC converter	Medium power (5..10 kW) High power (>100 kW)

Medium- and high-power applications have been implemented using hybrid integration. Hybrid integration covers a large range of power electronics. IPM (intelligent power modules) or ASIPM (application specific intelligent power modules) are used for voltage ratings up to 600V for a current rating from a few Amps up to 100A, and the standard power modules for current ranges greater than 100A and voltages over 1200V. High-power requirements (currents from 100A to 2000A and voltages up to 3000V) can be implemented with standard power modules using conventional system designs. In general integration of standard power modules is restricted to parallel construction of IGBT (or power MOSFET) dies in order to increase the current rating including free-wheeling diodes. There is no control or protection circuitry inside the modules. These modules use classical assembly technologies like solder mount on the backside of the die and ultrasonic bonding of aluminum wires for the top side contacts. They are limited in terms of reliability, thermal performance, and voltage performance (blocking voltage and insulation voltage of the overall module).

Monolithic integration of output power semiconductors with digital and analog circuitry includes power devices, signal processing and sensing (and protection) circuits on the same chip [76] [76], [77]. Monolithic solutions for power conversion and amplification are highly desirable not only for the reduction of interfaces, and thus volume, weight and electromagnetic interferences, but also for increasing efficiency, performance and reliability of the overall system. A wide range of applications is predictable for these monolithic solutions, since the power delivered by a power IC (PIC) into a load can be tens and even thousands of watts. In recent years, power integrated circuit (PIC) are oriented into two paths high voltage integrated circuit HVIC and smart power integrated circuit SPIC.

“Usage of single channel and half bridge gate driver ICs will increase over the next few years due to the need for isolation integration”, “Half bridge gate driver ICs are estimated to have accounted for over 40% of gate driver revenues in 2016. Single side gate driver ICs were the second most popular topology with about 30% of revenue. While full bridge and three phase

gate drivers are mostly found in motor control and inverter applications for low-mid power.” explains Jonathan Liao, Senior Analyst & Business Development Manager at Yole. [78]. This growth and demand brings to light, and emphasizes the shift from discrete solution to integrated solutions [79]. This shift is towards two paths integrating the driver and MOSFETs/IGBT in the same package IPM (or system-on-package) for high power applications or in the same chip (SoC: system on chip) towards deep miniaturization (monolithic solutions) for low and medium power applications, Fig.I. 25.

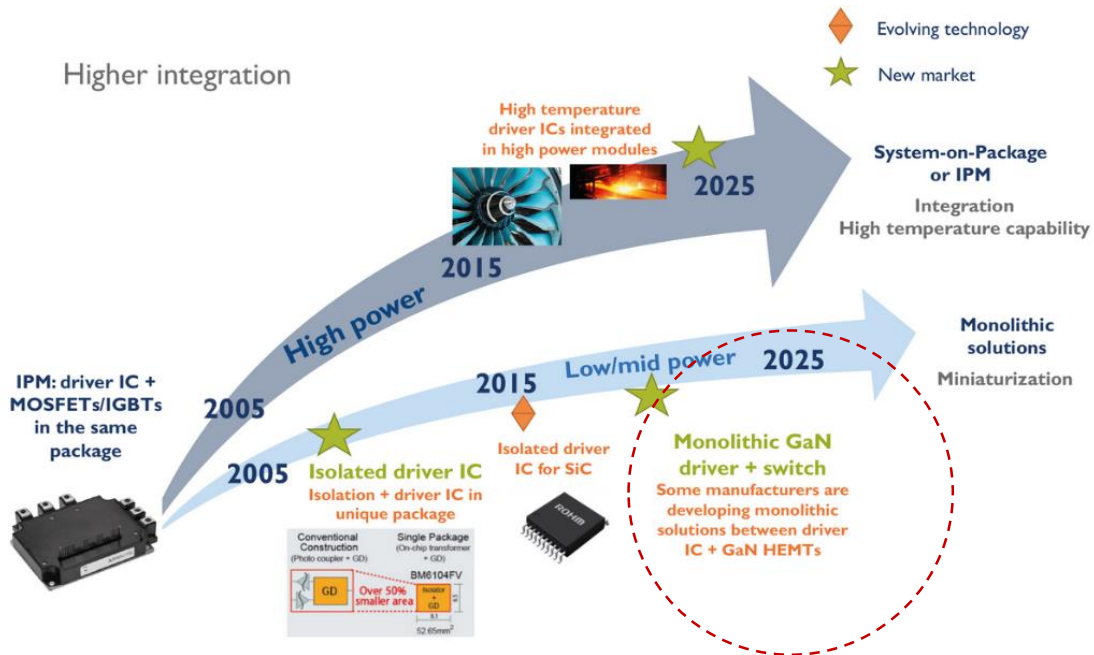


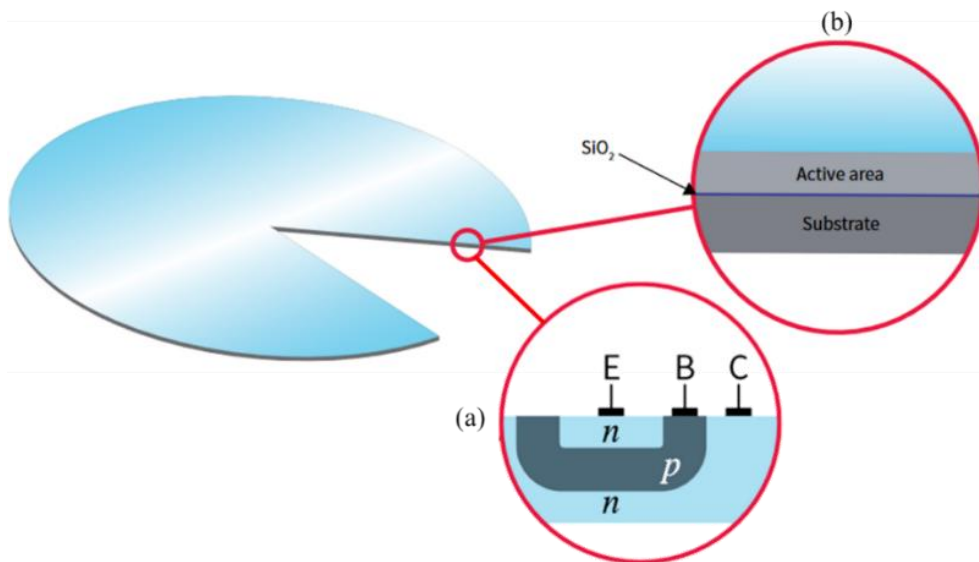
Fig.I. 25. Gate driver technology roadmap for high power and low/mid power application. [78]

The supply chain of the gate driver is evolving, pushed by higher integration needs, as well as an increasing need for more complete product solutions. Therefore, new technical requirements related to isolation or the use of GaN and SiC power transistor demand advanced drive IC technologies to be developed.

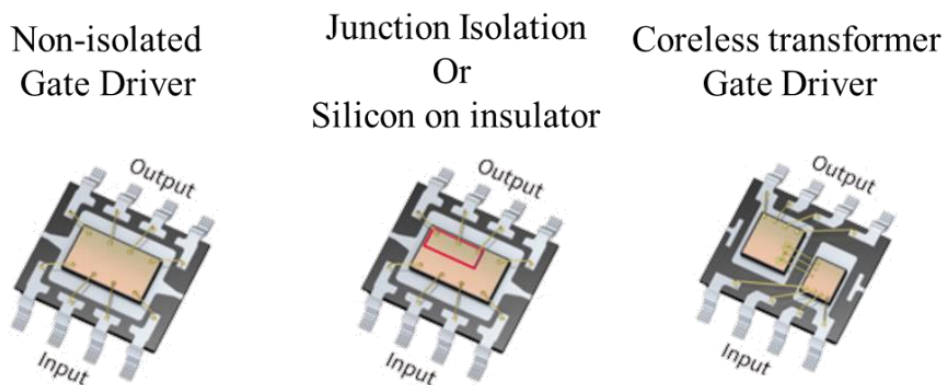
One of the main features of smart power technologies relates to the isolation techniques used between the power part and the low-voltage IC part. The isolation between the power part and the low-voltage part is achieved by JI technologies or dielectric isolation. The traditional approach of the industry is to use the JI for cost reduction. The conventional dielectric isolation with polysilicon deposited as a substrate layer is very expensive. Over the last years a cheaper solution based on SOI wafers has been developed. However, a development of this kind of isolation is linked to cost reduction. Thus, isolation by means of a junction remains the preferred solution for standard applications, whereas the dielectric isolation is being used for specific applications requiring a high level of isolation.

Infineon propose the junction isolation JI and the silicon-on-insulator SOI [27]. Fig.I. 26. (a) presents the p-n junction-isolation technology layer. This technology brings to light the high-voltage integrated circuit HV-IC and latch immune CMOS technologies which enable rugged monolithic construction. These HVIC gate drivers with floating switches are well-suited for

topologies requiring high-side, half-bridge, and three-phase configurations. Fig.I. 26 . (b) presents the silicon-on-insulator SOI technology layer. This technology is a high voltage level-shift technology. Each transistor is isolated by buried silicon dioxide, which eliminates the parasitic bipolar transistors that causing latch-up. This technology can also lower the level-shift power losses to minimize device-switching power dissipation. The advanced process allows monolithic high-voltage and low-voltage circuitry construction with technology-enhanced benefits.



**Fig.I. 26.** Wafer view of (a). Junction-Isolation (b). Silicon-on-insulator [80]

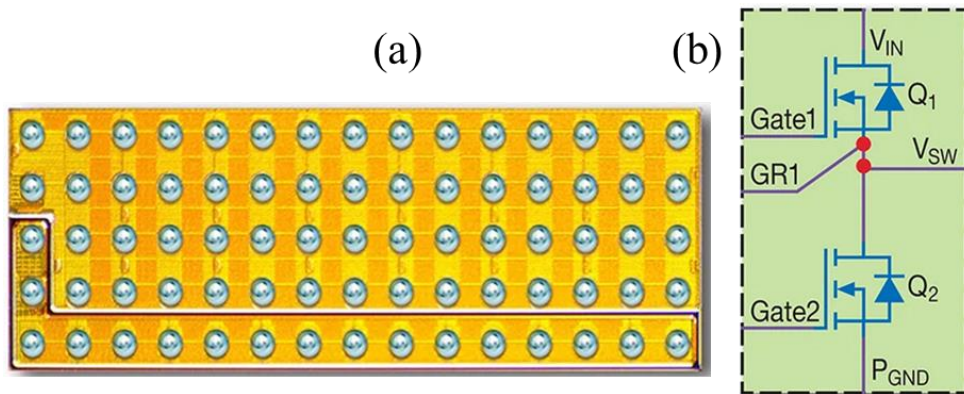


**Fig.I. 27.** Infineon gate driver IC technologies [80]

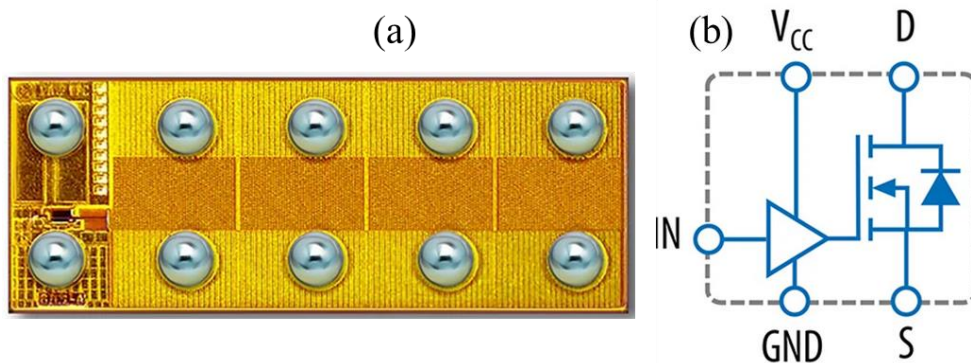
In addition to gate driver IC manufacturers, other players emerged along the supply chain to offer alternative solutions for various power management needs. Two of the more notable solutions are Intelligent Power Modules (IPMs) and Plug-and-Play (PnP) gate driver boards. An IPM integrates control, protection, gate driver, and power switching devices in a single package to address the need for compact, efficient, and application-specific power management needs. Some notable players such as Mitsubishi, ON Semiconductor, Semikron, and Infineon compete fiercely in the IPM market.



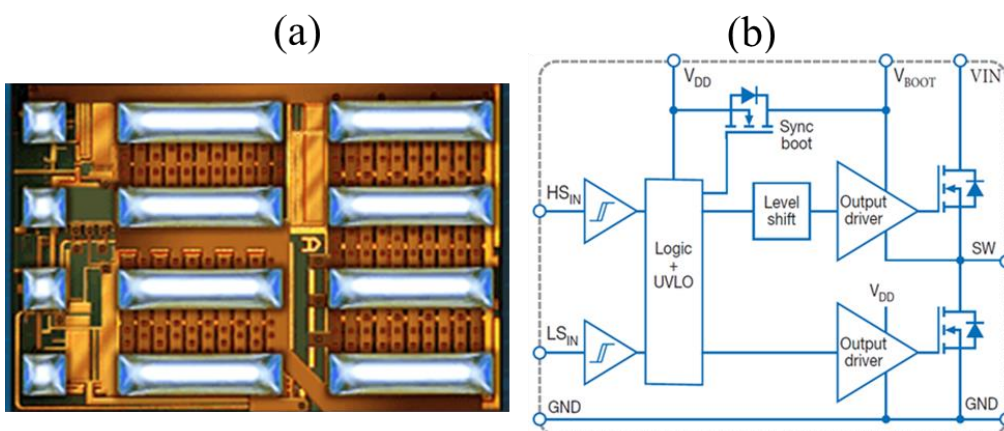
GaN technology, as opposed to standard silicon IC technology, allows designers to implement monolithic power systems on a single chip in a more straightforward and cost-effective way. Integrated circuits made using GaN-on-Si substrates have been in production for over five years. Since that time, GaN-based ICs have gone through various “phases” of integration from pure discrete devices to monolithic half-bridge devices, to power FETs that included their own monolithically integrated driver, and more recently, to fully monolithic power stages containing power FETs, drivers, level shifting circuits, logic, and protection. Fig.I. 28, Fig.I. 29 and Fig.I. 30 present these three phases of integration [81].



**Fig.I. 28.** Integration Phase One: Monolithic half bridge (a). Image of an EPC2100 monolithic half bridge measuring 6mm x 2mm (b). equivalent circuit diagram [81]



**Fig.I. 29.** Integration Phase Two: Half bridge + Driver (a). Image of an EPC2112 monolithic GaN-on-Si FET with integrated driver measuring 1.1mm x 2.9mm. (b). equivalent circuit diagram [81].



**Fig.I. 30.** Integration Phase Three: ePower™ stage (a). Image of an EPC2152 monolithic ePower stage measuring 3.9mm x 2.6mm (b). equivalent circuit diagram [81]

## 4. Behavior of SiC MOSFET Under Short-Circuit

The key to ensure a robust system and a safe operation of the SiC MOSFET device, is to fully understand the device characteristics and behavior under short-circuit (SC). SiC MOSFETs compared to Silicon IGBTs have better figures of merit, where SiC MOSFETs can have similar conduction losses with much improved switching losses. As the SiC MOSFETs gain maturity and their cost goes down with time, SiC MOSFETs are expected to be adapted and used in more and more applications.

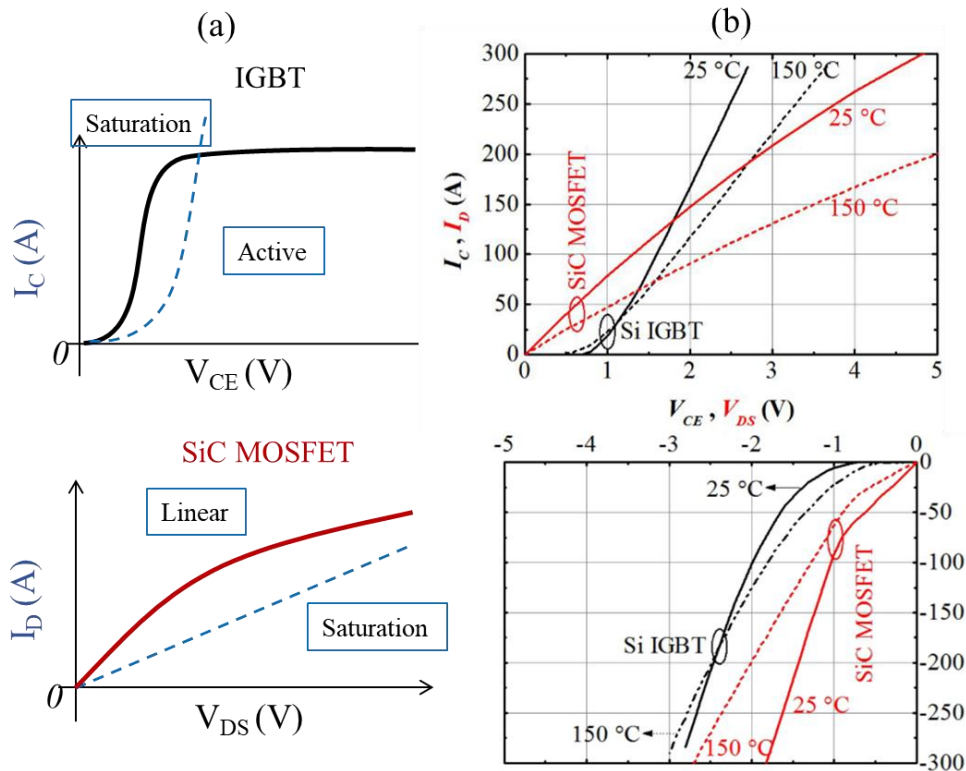
### 4.1. Characteristics impacts of SiC MOSFET and Si IGBT under short-circuit

Silicon power devices with higher breakdown voltages are considerably high on-resistance per unit area, which increases approximately by the 2nd to 2.5th power of the breakdown voltage. As a result, Si IGBTs have been mainly used in devices with breakdown voltages of 600V or higher. IGBTs achieve lower on-resistance than MOSFETs by injecting minority and majority carriers into the drift region, a phenomenon called conductivity modulation. But these minority and majority carriers generate a tail current when transistors are turned off, resulting in a significant switching loss. SiC devices do not need conductivity modulation to achieve low on-resistance since they have much lower drift-layer resistance than Si devices. MOSFETs generate no tail current in principle. As a result, SiC MOSFETs have much lower switching loss than IGBTs, which enables higher switching frequency [82]. The switching depends mainly on the power device capacitors, the gate driver parameters and power loop, ...

On other words, for the same ON resistance, SiC MOSFET has much smaller chip size [82] but with a stronger and tighter electric field than in silicon, especially close to the gate oxide. This results in lower parasitic capacitances and faster switching speed, which significantly reduces switching losses as a counterpart to a more intense electric field stress in the oxide. Lower switching losses will improve power converters efficiency, allowing the power converters to operate at a much higher frequency. However, due to the smaller chip MOSFET has lower static and transient thermal dissipation capability [83] [84] [85].

As in silicon technology, all wide band gap transistors should be protected from short-circuits. However, the higher power densities enabled bring the issue of how long a SC fault can be sustained by a SiC power device. Additionally, a higher frequency operation implies the SC should be detected faster.

Si IGBT typically works in the saturation regime during the normal on-state, contrary, to SiC MOSFET who works in the linear regime [86], as illustrated in Fig.I. 31.



**Fig.I. 31.** Si IGBT vs SiC MOSFET Output Characteristics ( $I_D$ - $V_{DS}$ ) (a). Representative (b). [87]

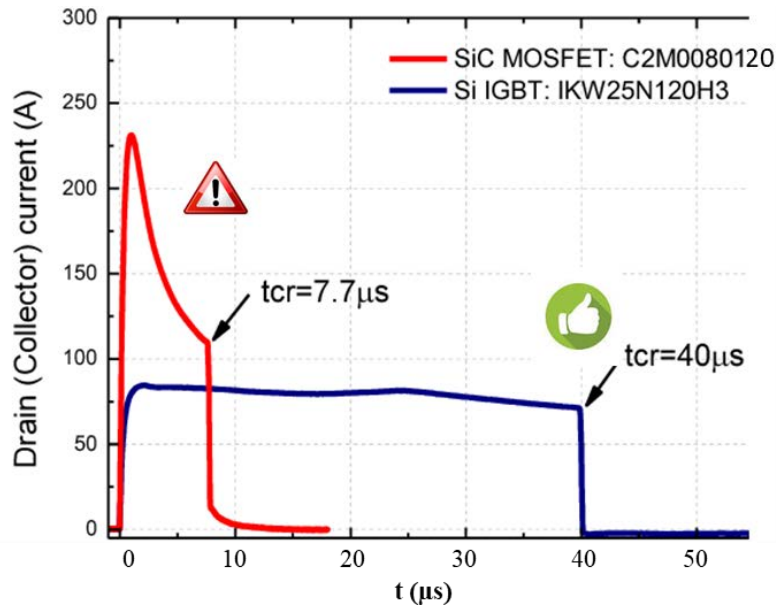
For Si IGBTs, when a short-circuit happens, the collector current  $I_C$  increases and goes through a sharp transition from the saturation injected-mode region to the desaturation active region. While in the active region, the collector current  $I_C$  cannot get any higher and gets self-limited and becomes independent of collector emitter voltage  $V_{CE}$  variation excepted by the Early effect. Consequently, the power dissipation gets self-limited as well [88]. Due to this behavior, Si IGBTs have long SC withstanding capability, typically within 10 $\mu$ s.

SiC MOSFETs on the other hand; which work in the linear ohmic-mode regime; have a larger linear region compared to Si IGBTs. Therefore, under short-circuit, the transition from the linear ohmic-mode region to the limited-current saturation region occurs under a higher drain-source voltage  $V_{DS}$ . Contrary to Si IGBT, the drain current  $I_D$  keeps increasing along with the drain-source voltage  $V_{DS}$ . This rise causes damage to the device before reaching the transition point (transition between the linear and saturation mode) [89]. As a result, SiC MOSFETs have significantly reduced SC withstanding capability compared to IGBTs, and therefore need to be protected quickly, typically within 2-3 microseconds, as presented in Fig.I. 32. [90].

In Fig.I. 32, in addition to the higher current density involved in the chip, there is a very high peak current on the first microsecond of the short-circuit. This is a source of additional stress in power device. It originates from two phenomena specifically to the SiC MOSFET:

- A mobility part of the electrons in the channel called Coulomb scattering which is characterized by a positive temperature coefficient in the range  $T_{amb}$  to 300°C on the one hand,

- A threshold voltage  $V_{GS\_th}$  drift sometimes evolving at the same time as the voltage  $V_{GS}$  increase, i.e. initially of low value ( $V_{GS} < 0$ ) then of higher value ( $V_{GS} \gg V_{GS\_th}$ ), this variable threshold voltage has a dynamic of the order of one microsecond, it is conditioned by the de-trapping of the holes (positive mobile charges) from the oxide towards the channel region, which increases the density of carriers in the channel (hence the current peak) before relaxing by recombination (hence the current decrease) in addition the self-heating effect.



**Fig.I. 32.** Experimental current waveforms during critical short-circuit test for SiC MOSFET and Si IGBT (SiC MOSFET:  $V_{DS}= 600V$ ,  $V_{GS}= 20V$ ; Si IGBT:  $V_{CE}= 600V$ ,  $V_{GE}= 15V$ ) [90]

## 4.2. Turn-on analysis of SiC MOSFET

Regardless of the short-circuit robustness, the short-circuit fault must be turned OFF as soon as detected to preserve the device from degradation. Hence, a study is conducted in the beginning of the turn-on, to distinguish between Normal Turn-on NTO operation and SC operation.

The power device is exposed to several types of SC. There are three regular types of SC faults. The Hard Switch Fault (HSF, SC type I); and Fault Under Load (FUL, SC type II) are the two main SC fault behaviors. The third SC type (SC type III) occurs when the upper diode is freewheeling [91]. Other than short-circuit fault, an open circuit fault can occur as well. Other special short-circuit configurations exist for multi-level topologies, they are beyond the scope of this work and will not be considered.

### 4.2.1. Normal Turn-on

Section I.2 fully covered the analytical behavior of the SiC MOSFET at the turn-on and turn-off. In this section, only parameters that are relevant to the study of short-circuit are discussed. In SiC MOSFETs, the dynamic drain current  $I_{DS}$  is controlled by the gate-source voltage  $V_{GS}$ , as previously mentioned. The reverse transfer capacitance; the gate-drain capacitance; “ $C_{rss} =$



$C_{GD}$  of a SiC MOSFET, also known as the Miller capacitance, is one of the most important parameters in switching performances for unipolar devices. This capacitance is nonlinear function of voltages  $V_{GS}$  and  $V_{DS}$  and it provides a feedback between the output voltage  $V_{DS}$  and the input  $V_{GS}$  of the device. Another useful parameter from the circuit design point of view is the gate charge  $Q_G$ , which will be elaborated upon in the section further below.

Fig.I. 33. (a) presents the turn-on transitions. The turn-on transitions are divided into 3 main regions. The first region A, where the gate-source voltage  $V_{GS}$  rises to Miller plateau voltage. The gate current is used to charge the input capacitors  $C_{GS}$  and  $C_{GD-Min}$ . Thus, the gate-drain voltage  $V_{GD}$  drops from  $[V_{Bus}]$  to  $[V_{Bus}-V_{GS\_M}]$ ,  $V_{GS\_M}$  is the Miller voltage. Afterwards in the second region B,  $V_{GS}$  remains at  $V_{GS\_M}$ . The gate current is used to charge the reverse transfer capacitance  $C_{rss}$ . Thus,  $V_{GD}$  drops from  $[V_{Bus}-V_{GS\_M}]$  to  $[I_D * R_{DS\_ON}]$ . The  $R_{DS\_ON}$  value is at near the minimum value, equivalent to the  $R_{DS\_ON}$  between ohmic and saturation transition point, when  $V_{GS}=V_{GS\_M}$ . In the presence of a SiC transistor, a short channel is generally used to reduce the losses in the on-state. This property causes a greater dependence of  $V_{GS\_M}$  to variations in drain voltage than it can be in vertical silicon device (ex. SJ-VDMOS and IGBT), with a slight slope appearing instead of the Miller plateau [9]. In the last region C,  $V_{GS}$  rises back again to reach  $V_{Drv+}$ . The SiC MOSFET enters into the ohmic regime, Fig.I. 34. This time the gate current is used to fully charge the input capacitors  $C_{GS}$  and  $C_{GD-Max}$ , and reach the lowest on-state voltage drop [93]. Note that the corresponding diode of the transistors is assumed to be a unipolar Schottky diode.

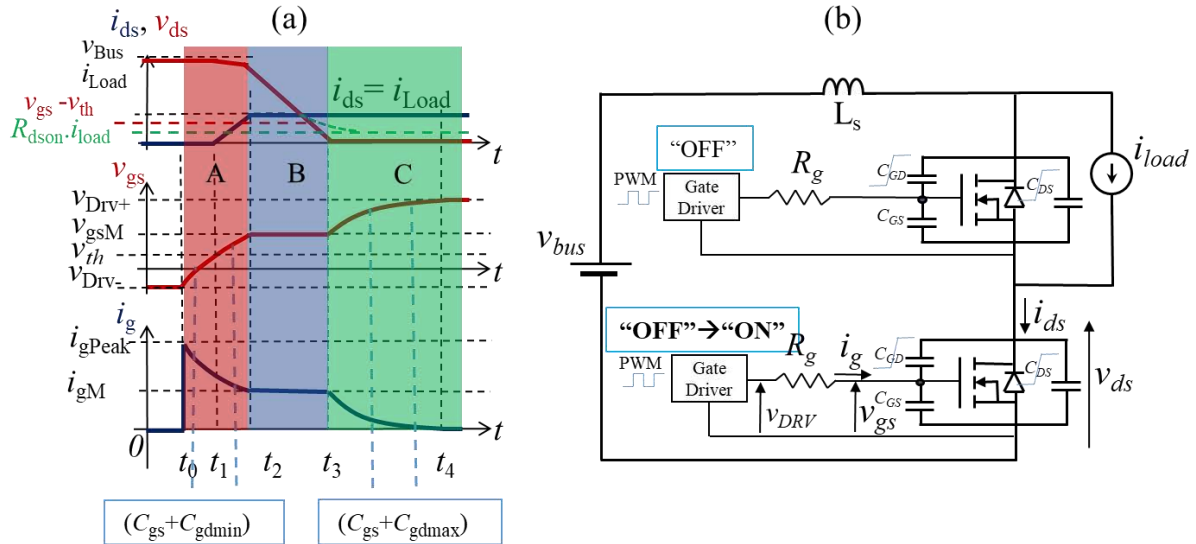


Fig.I. 33. (a). Turn-on switching characteristics of SiC MOSFET under NTO conditions. (b). Equivalent circuit of the half bridge.

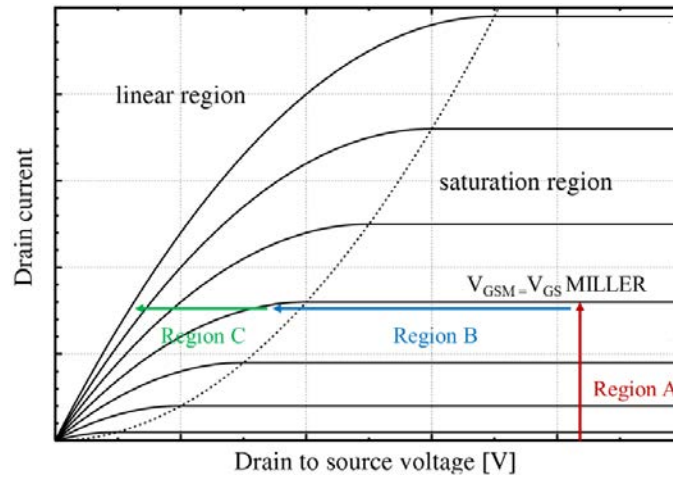


Fig.I. 34. Turn-on regions presented on  $I_D$ - $V_{DS}$  curve.

### 4.2.2. Hard Switch Fault

HSF occurs when the switch turns on with a permanent full bus voltage across itself typically caused by faulted control signals, as presented in Fig.I. 35. (b) [94]. The stray inductance  $L_S$  induces a slight voltage  $V_{DS}$  drop from  $V_{Bus}$ , as given by the equation eq.(I. 22).

$$\Delta V_{DS} = L_S \cdot \frac{dI_D}{dt} \tag{I. 22}$$

Distinctively from NTO, when  $V_{GS} = V_{GS\_M}$  at  $t_2$  under HSF operation,  $V_{GS}$  and  $I_{DS}$  continue to increase until  $V_{GS}$  reaches  $V_{Drv+}$  and  $I_{DS}$  overcurrent,  $t_3$ ,  $I_{DS} = I_{Sat-Channel}$ .  $V_{DS}$  stays at the  $V_{Bus}$  value, which causes the transistor to operate in its saturation regime, as shown in Fig.I. 35. Such a regime can be sustainable only for a couple of  $\mu s$ , as presented in [95]. In this SC operation, there is no discharge of the Miller capacitance. As a consequence, a significant difference appears in the  $Q_G$  characteristic between NTO and HSF.

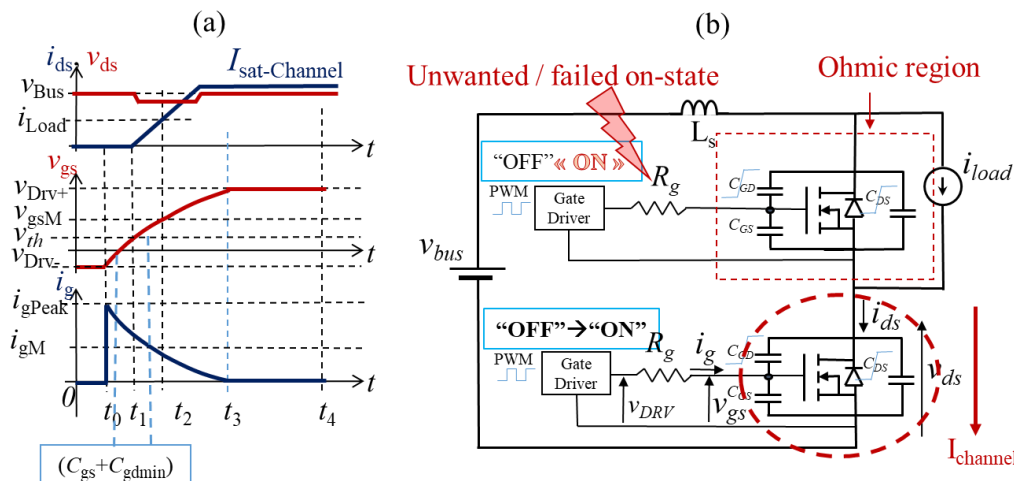


Fig.I. 35. (a). Turn-on switching characteristics of SiC MOSFET under HSF conditions. (b). Equivalent circuit of the half bridge.

### 4.2.3. Fault under load

In contrast, fault condition type II appears after the three normal time intervals are accomplished, namely, after  $t_4$ , where the MOSFET is in on-state ohmic mode  $V_{GS} = V_{Drv+}$  and  $I_{DS} = I_{Load}$ . In this fault condition,  $I_{DS}$  increases to  $I_{DS-Saturation}$  (which can be calculated by the trans-conductance curve  $I_{DS} = f(V_{GS})$  at  $V_{Bus}$ ), which in turn raises  $V_{DS}$  to the bus voltage  $V_{Bus}$ , due to the MOSFET entering the saturation regime. Therefore, a positive value  $dV_{DS}/dt$  appears and a reverse current flows into the gate  $I_G < 0$  through  $C_{GD}$ , due to the Miller coupling and the capacitance  $C_{GD}$  decreases. All these phenomena lead to a voltage bump on  $V_{GS}$  towards a larger value  $V_{GS-ov}$  gate-source over-voltage, as shown in Fig.I. 36. (a) [96].

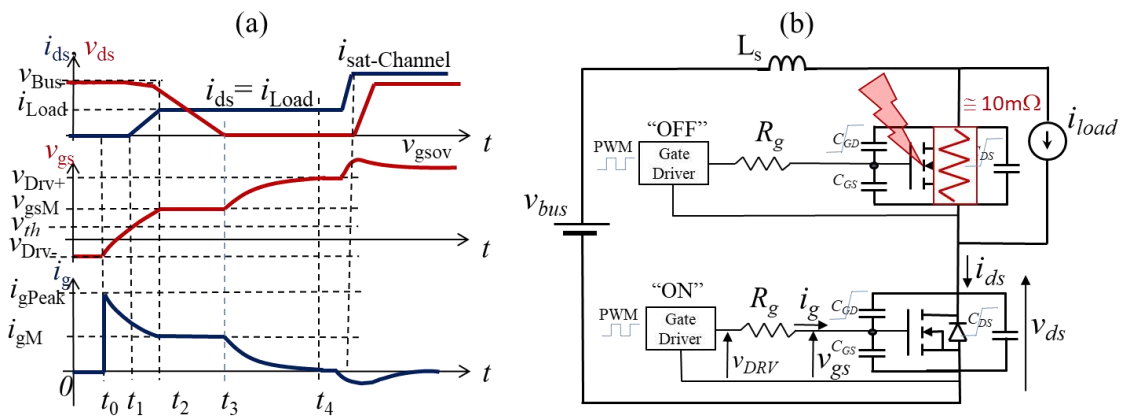


Fig.I. 36. (a). Turn-on switching characteristics of SiC MOSFET under FUL conditions. (b). Equivalent circuit of the half bridge.

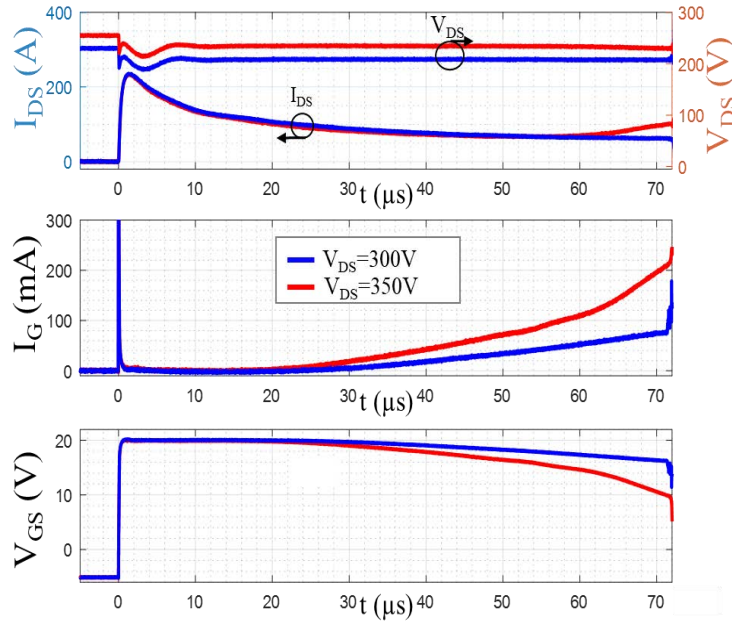
### 4.3. Unique SiC MOSFET behavior under Short-circuit

As mentioned in the section [Chap.I.4.2.2], when the temperature rapidly increases in the beginning of the HSF, the threshold level of the component decreases causing the drain current to reach its saturation current  $I_{D\_Sat}$ . In the second place, the main mobility part by acoustic phonons of the free carriers in the channel under the gate decreases with the temperature [97], leading to a decrease in the saturation current.  $V_{DS}$  experiences a slight drop as well, due to the internal resistance of the component as well as the Bus capacitance.

Another interesting parameter to take into consideration while detecting a short-circuit, is the gate current  $I_G$ . Fig.I. 37 shows a strong dependence of the saturation current on the gate polarization due to the electric field in the gate oxide. [98]. From the start of the short-circuit, the temperature of the chip rises rapidly, because the power dissipated in the chip ( $P = I_{DS} * V_{DS}$ ) is very high: about 50 kW. This increase in temperature initially causes the threshold voltage of the component to decrease, resulting in an increase in the saturation current. In a second step, the mobility of the free carriers in the channel under the gate decreases with the temperature, [99], which leads to a decrease of the saturation current. The increase of the temperature and the weakness of the oxide lead to gate leaks lead to hot-electrons injection, described by Schottky thermos-emission [99]. Therefore, the gate leakage current flowing through the

external gate resistance; at the output of the buffer; under a SC, causes a slight drop on the gate-source voltage  $V_{GS}$ .

Experimental results are presented in [100], showing that the leakage current behavior is unique to SiC MOSFETs, where this behavior is not observed for Si MOSFETs : in silicon technology the thermal runaway and after fail-to-short mode of the chip appears at a temperature level lower than that which would be necessary to trigger of the Schottky emission or Fowler-Nordheim gate leakage current as we can see in SiC MOSFET. The article presents the behavior for different variable parameters. This study had been lead in the thesis of F.Boige [99].



**Fig.I. 37.** SC under HSF experimental waveforms for  $V_{GS}= 20V$  and  $V_{DS}= 300V; 350V$

#### 4.4.Possible Failure mode

There are different test failure mode operations:

- The current limitation mode also known as Failures under long duration short-circuit: the DUT is maintained in an on-state during a very long short-circuit duration  $T_{SC\_Max}$ , Fig.I. 38. (a). [95] [101]. The estimated critical maximum energy of destruction is given in eq.(I. 23).

$$E_{C\_Max} = \int_{t=0}^{t=T_{SC\_Max}} I_{DS} \cdot V_{DS} \cdot dt \quad (I. 23)$$

- Short-pulse mode is another operation to induce the DUT into a failure. Therefore, a gradual augmentation of the pulse width is performed until the destruction of the DUT, Fig.I. 38. (b). Thus,  $T_{SC\_Min}$  is referred to the previous pulse before destruction, and Thus,  $E_{C\_MIN}$  is its critical energy.

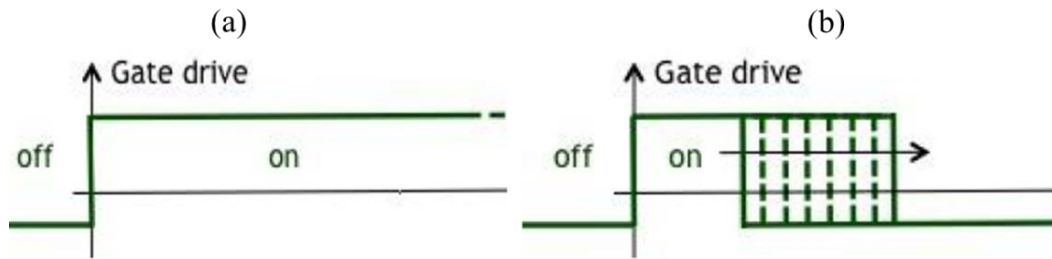


Fig.I. 38. SC failure mode test (a). Current limitation (b). Short-pulse

Both SC types have their own failure behavior, in addition to Fig.I. 35 and Fig.I. 36, fault behavior. In respects to Kirchoff law, the equations eq.(I. 24) are given, with HS: High Side transistor, LS: Low Side transistor.

$$V_{Bus} = V_{DS-HS} + V_{DS-LS} \quad ; \quad I_{Load} = I_{D-HS} - I_{D-LS} \quad (I. 24)$$

Failure analysis type I (HSF) in a 2-level voltage source inverter: Two cases are presented, depending on the current direction.

-  $I_{Load} < 0$ , as presented in Fig.I. 35.(b). Implies that the drain current of the high side is lower than the low side, eq. (I. 25). The low side transistor saturates first  $I_{D\_Sat}$  causing a thermal overheating then possible latch-up and destruction of the low side transistor, when the high side is in the ohmic region. Then, the high side undergoes the same consequence.

$$I_{D-HS} > I_{D-LS} \quad (I. 25)$$

-  $I_{Load} > 0$ , Implies that the drain current of the high side is higher than the low side, eq. (I. 26). This time, the high side saturates first  $I_{D\_Sat}$  causing the total opposite sequence when  $I_{Load}$  is positive, Fig.I. 39.

$$I_{D-HS} < I_{D-LS} \quad (I. 26)$$

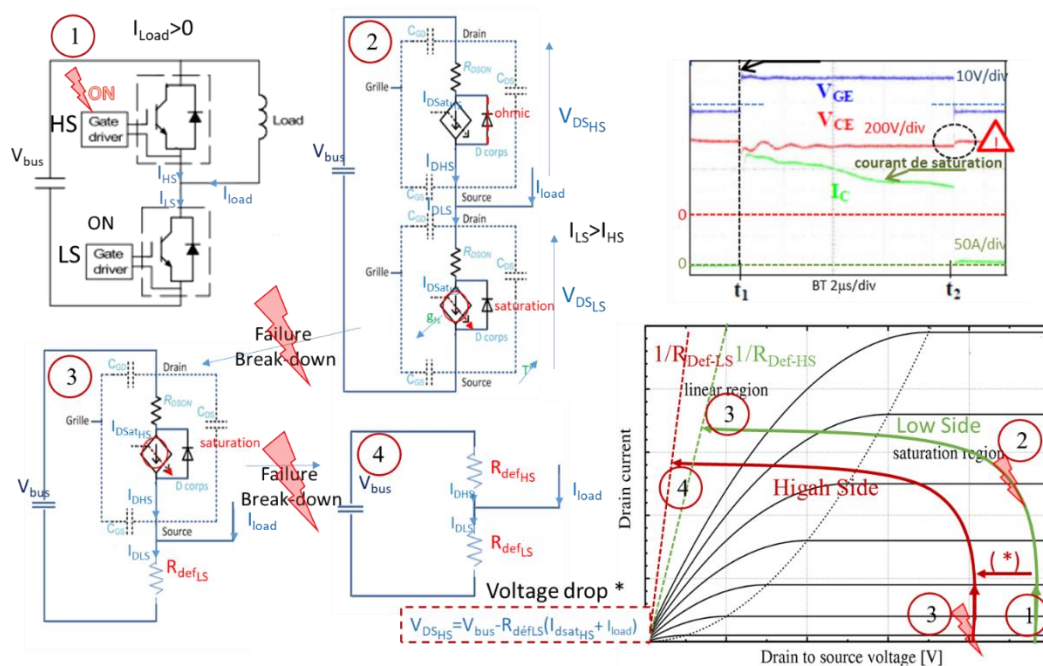
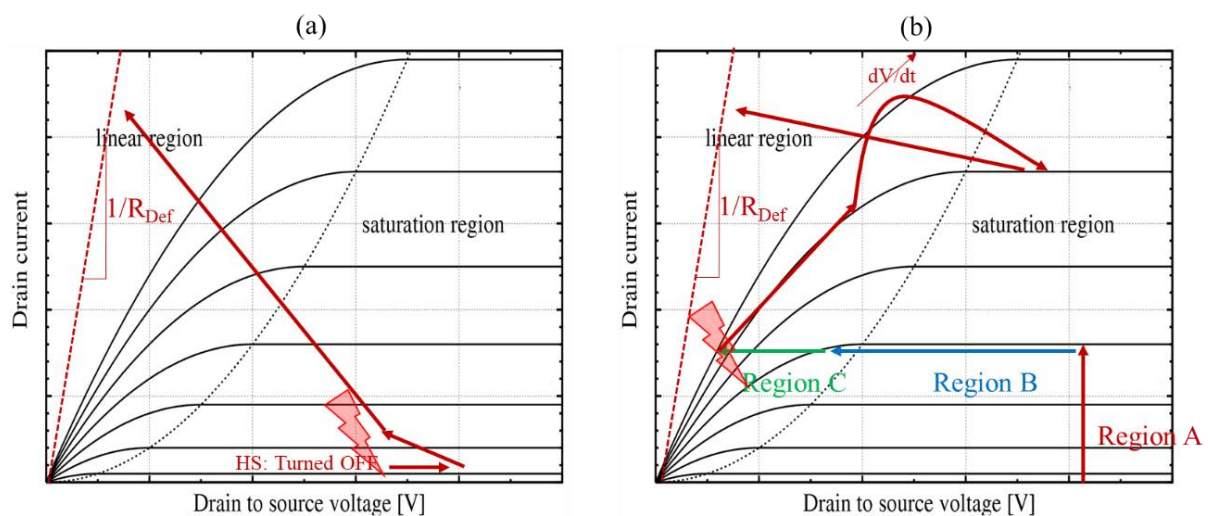


Fig.I. 39. Failure breakdown schematic steps and  $I_D$ - $V_{DS}$  curve failure analyses fault, type I. Typ.  $T^\circ$



### Failure analysis type II (FUL):

For a negative  $I_{Load} < 0$ ; as presented in the circuit of Fig.I. 36. (a); the high side transistor is the first to be destroyed, as shown in Fig.I. 39. (a). The low side SiC MOSFET is in on-state, so the MOSFET is in the linear region before the faults happens. In the linear region, the  $V_{DS}$  of the power transistor is determined by the  $R_{DS\_ON}(V_{GS})$  and the drain current. Then, the low side transits from the linear regime to the saturation regime, where the low side is unable to limit the current leading to a significant self-heating of the device. The device is shut down by the gate driver. The drain current is cut off, and a significant high  $di/dt$  is generated, which causes a large voltage spike on the device. This is caused by the stray inductance and the power switching loop. The voltage spike can be as high as the DC bus voltage, which can cause the device destruction, Fig.I. 40. (b).



**Fig.I. 40.** Illustration of the failure analysis fault points, type II (a). High side and (b). low side  $I_D$ - $V_{DS}$  curve. Typ.  $T^\circ$

Other failure types do exist such as cascaded propagation, where one of the transistors undergoes destruction of the type I and the other one undergoes destruction of the type II. Those cases are not discussed here.

Those classical destruction mechanisms failures of an inverter arm composed of two power switches can be limited by reducing the drain source voltage overshoot, to do so:

- Minimizing the stray inductance of the power loop. Hence reduces the short-circuit withstand time.
- Increasing the gate resistance to slow down the  $dI_{DS}/dt$ . But this method will increase the switching losses during every switching cycle. Also, larger gate resistance leads to larger voltage spike on the gate source voltage involved under load events.

## 5. Short-Circuit Detection techniques

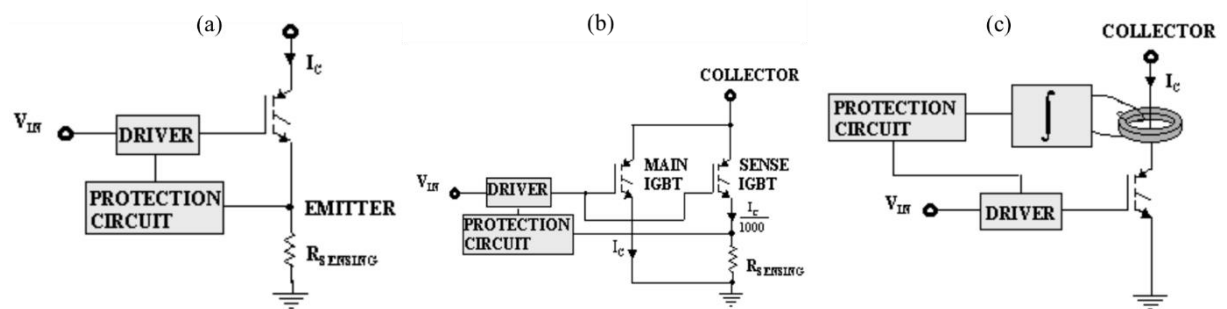
The two fault behavior presented, HSF and FUL are the main faults discussed in this section. Si IGBTs have been around way before the SiC MOSFETs. This has made the Si IGBTs more mature and led to the development of different short-circuit protection and detection circuits.

The literature is rich in protection and converter reconfiguration in case of critical fault [102] [103]. Monitoring techniques must fulfill various requirements, such as:

- High sensitivity
- High accuracy and linearity
- Low temperature drift
- Interference rejection
- Low voltage monitoring
- IC packaging
- Low power consumption
- Low price

For better understanding and developing new detection methods, several ancient and modern monitoring methods are discussed below. Those methods are based on the abnormalities created under SC discussed above, as the drain current  $I_D$ ,  $dV_{DS}/dt$ ,  $dV_{DS}/dt$ ,  $Q_G$  or the presence of the Miller plateau...

### 5.1. Shunt resistor monitoring method



**Fig.I. 41.** Three current monitoring methods schematic (a). Shunt resistor method (b). SenseFet method. (c). Transformer method [102]

The common and simple approach to current sensing is the use of a shunt resistor in series with the power loop. The voltage drop across the shunt is proportional to its current flow  $I_D$ . This approach is straight forward. To guarantee the accuracy of the detection, a high precision resistor and a fast analog-to-digital converter ADC is required, Fig.I. 41.(a) [102].

In high power systems, the high current passing by the sensing resistor creates large power loss. On the other hand, in low power systems, the current is low, so a larger resistor is needed. By doing so, power loss is generated. This method suffers from several inconveniences, as not being galvanically isolated, low noise tolerance, and most importantly the additional parasitic inductance added to the power loop. This parasitic inductance considerably damages the switching performance of the fast switching SiC or GaN components. All these obstacles push this study not to be developed any further. A study on shunt resistor-based current measurements for fast Switching GaN Devices is proposed in [104].

## 5.2. Sense-Fet monitoring method

Another current-based sensor is the Sense-Fet detection method. This method requires a non-standard integrated power chip, where a scaled-down transistor is in parallel with the main device. The scaled-down transistor copies and divides the drain current passing by the main one subject to keeping the measurement potential is kept low, approximately the diffusion voltage 0.6V. The scaled-down current is then measured with different techniques, the shunt resistor can be applied this time without worrying about the size of the resistor, Fig.I. 41.(b) [102].

As a non-standard chip is required and the system cost increases. The main advantage of this method is low noise will be generated by integrating the sensor, there is no parasitic inductance added here again subjected to be able to integrate the electronic sensing on-chip on in-package. This method will not be further detailed here; it is essentially relevant for automotive applications, subject to numerous safety standards, which may require current monitoring to anticipate any risk of excessive thermal overload and risk of overheating or even fire.

## 5.3. Current transformer monitoring method

A more traditional current sensing is the current transformer method, currently used in power IGBT module, specifically in lab. testing. This method requires a Rogowski Coil (toroidal ferrite core) around the drain wire of the power transistor. Rogowski coil is based on the principle of Faraday's law of induction and the output voltage  $V_{out}$  of the Rogowski coil is determined by integrating the drain current  $I_D$  to be measured. The output voltage is proportional to the time derivative of the linkage flux. Then, integrated to get an image of the current, Fig.I. 41. (c) [102].

The need of a wide bandwidth extending from low switching frequencies, due to the rapid time rise of the fault current, is a clear disadvantage of this method. As well the integration complication, and the cost and size used by the transformer. A PCB current sensor is developed in [105], otherwise this method is not further developed here.

## 5.4. Desaturation monitoring method

Besides the Sense-Fet monitoring method which is used in automotive application, there are several other detection methods [106]. Another detection method with greater maturity in the field of IGBT is presented in this section. Unlike the other methods above, this method is an indirect voltage detection based. This method goes by the name of desaturation method DESAT coming from the BJT – IGBT vocabulary .... The most popular detection method for Si IGBT and SiC MOSFET. [107] [108]

As presented earlier,  $V_{DS}$  slopes changes is one of the critical parameters that changes under NTO, HSF and FUL faults. DESAT method detects the voltage at the terminals of the power transistor  $V_{DS}$  or  $V_{CE}$ .

When a SiC MOSFET is switched on, the component is in the ohmic zone: its resistance is very low, as is the voltage difference at its terminals. On the other hand, if the device in the switching cell is unable to withstand the voltage or if the load itself is short-circuited, the



component will have to withstand the entire supply voltage  $V_{Bus}$ . Under these extreme stress conditions, the device goes into saturation zone and the current density in the channel is 5 to 10 times higher than the nominal value [10]. DESAT technique will detect the abnormal presence of the voltage when the component is switched-on. Fig.I. 42. presents the schematic of this method. The circuit consists of a rapid high voltage diode connected in series with a decoupling resistor of a high value and a blanking capacitor, [109]. When the power MOSFET turns on, a current source charges the blanking capacitor and the diode is forward biased when the capacitor voltage is higher than  $V_{CE}$  or  $V_{DS}$ . During normal operation, the capacitor voltage is clamped at the forward voltage of the device. When short-circuit happens, the capacitor voltage is quickly charged to the threshold voltage above the pre-set reference voltage, which triggers the device shut down.

For DESAT protection circuit, a blanking time is needed to prevent false trigger during switching turn-on transients. A small current is generated by the gate driver or external circuit to charge the blanking capacitor. The blanking time is calculated as eq.(I. 27).

$$t_{Blk} = \frac{C_{Blk} * V_{DSAT}}{I_{Ch\_G}} \quad (I. 27)$$

DESAT threshold voltage varies between different devices due to the output characteristics, especially IGBT and SiC MOSFET. As SiC MOSFET has less short-circuit withstand time than IGBT, DESAT threshold voltage should be set lower for silicon carbide MOSFET than IGBT to shorten blanking time. To adjust the detection voltage, the resistance value, or the number of diodes, can be adjusted, in order to use LV diodes and decrease the capacitance. Except for changing the resistance value and the number of diodes, a resistor divider can be used to modify the saturation circuit for low threshold voltage. However, the threshold voltage should not be too low to prevent false trigger [109].

The DESAT is simple and easy to realize and the DESAT circuit has negligible power loss. Even with its many advantages, the DESAT encounters several challenges, especially for SiC MOSFETs.

- The high voltage diode should be fast reverse recovery, which increases the cost;
- Multiple series high voltage diodes are needed to share blocking voltage for applications above 1200V and to reduce the apparent equivalent series capacitance in off-state, finally which increases the cost;
- Blanking time makes the protection time too long for SiC MOSFETs. Also parallel diode is needed to prevent the negative voltage after the high voltage diode, to prevent the destruction of the gate driver; ...
- In principle, this method is not suitable for majority carrier's conduction device. Indeed, in overload current and at high temperature, the increase of the  $R_{DS\_ON}$  can cause a voltage drop above the threshold and trip the protection without a fault. Compensating techniques exist.

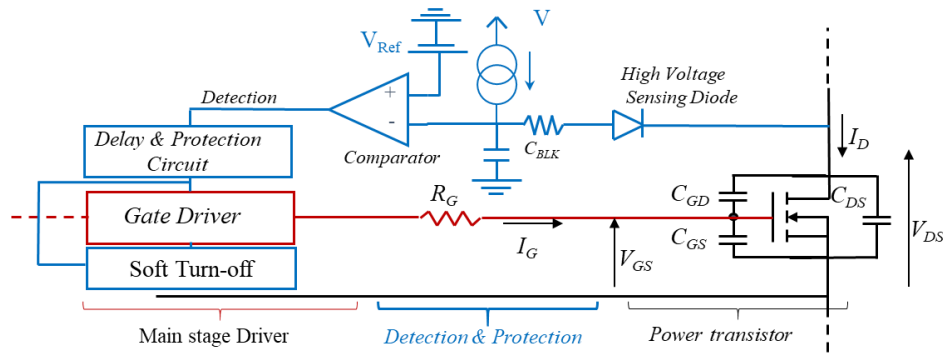


Fig.I. 42. Desaturation detection schematic

### 5.5. Gate current leakage monitoring method

Detection methods based on the voltage or current of the power loop have been presented above. This time, the detection method presented below is more towards the gate. As shown in [Chap.I.4.3], the static and dynamic gate currents are, respectively, a marker of component ageing and a short-circuit indicator. SiC MOSFETs have this dynamic gate leakage during a short-circuit stress, this stress being caused by different phenomena. One of them is the conduction phenomenon through the gate oxide called Schottky emission, which is triggered by the extreme temperature of the component. Thus, detecting this current is a SC marker and with the appropriate electronics, can lead to a fast shutdown to avoid failure.

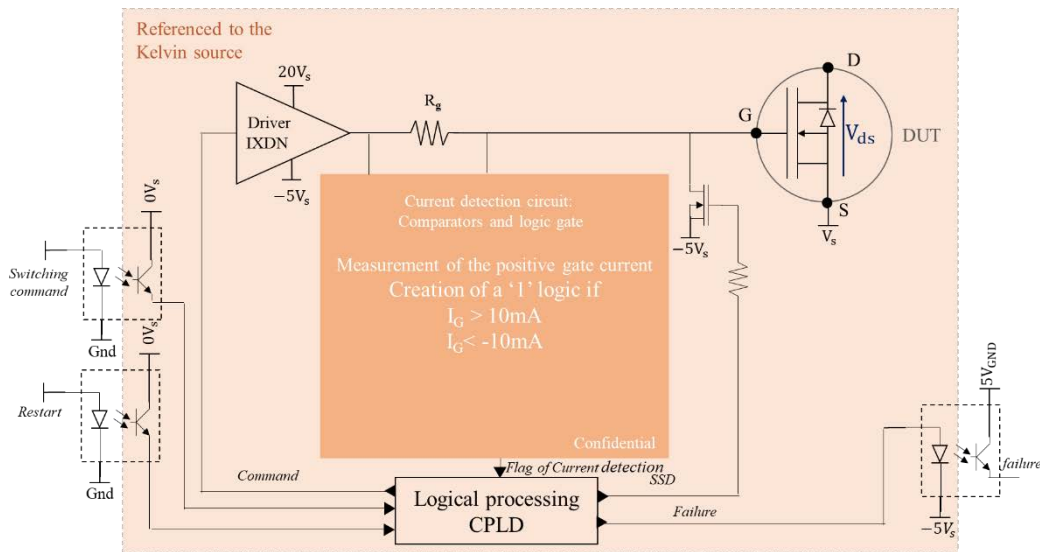
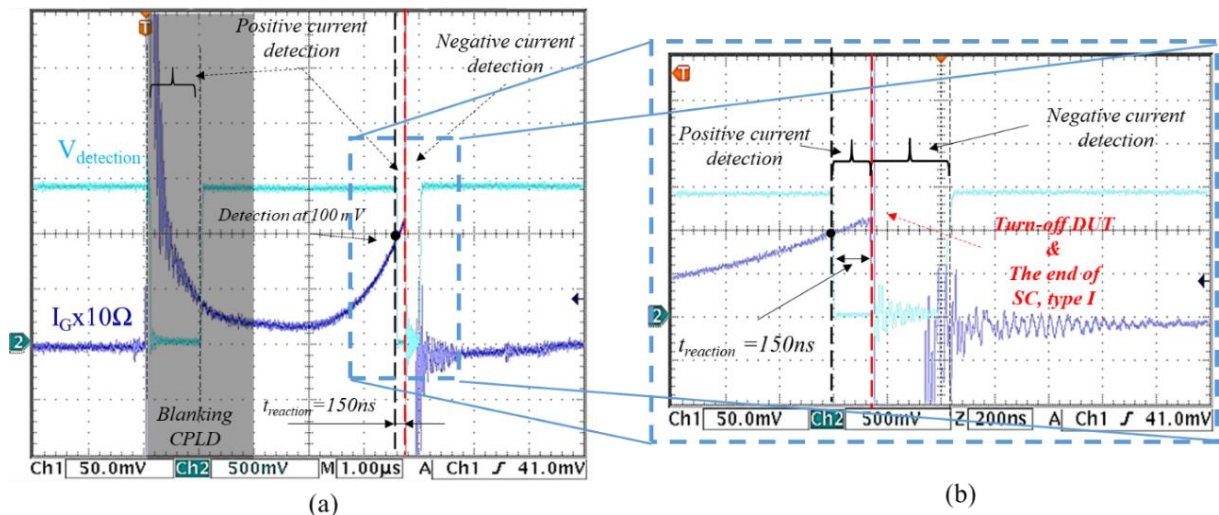


Fig.I. 43. Partial Gate leakage detection schematic.

The study of this method was led by F.Boige in his thesis [99]. This method is a novel, rapid fault detection using only the singular evolution of the SiC MOSFET gate current. The dynamic gate leakage current can be observed at about half the devices short-circuit withstanding time ( $t_{sc}/2$ ). However, detecting a current on the gate can be the normal switching order of device or a current injection through the parasitic Miller capacitance caused by the switching of another device as cross-talk phenomena in inverter leg. A blanking window must be introduced as the VDSAT method. The proposed detection method relies on a low current detection and a

dedicated logical circuit to sort out the normal operating condition from the short-circuit behavior.

The partial detection circuit principle is presented in Fig.I. 43. The current is measured using the external gate resistor as a shunt with an excellent SNR (Signal Noise Ratio) enabling a high robust detection method. The logic circuit uses the PWM switching signal as a reference starting a blanking time of  $2\mu\text{s}$  to avoid true false positive that is equivalent to  $t_{sc}/4$  for the device considered. The experimental results show the dynamic gate current detection at  $10\text{mA}$  ( $100\text{mV}$  across  $10\Omega$ ) and the device shut down in less than  $150\text{ns}$ .



**Fig.I. 44. (a)** Experimental waveforms of the gate current and the detection voltage. **(b).** A closer look at the leakage current at the detection.

Fig.I. 44 presents experimental waveforms of the gate current and the detection behavior, [110]. The figure displays the leakage current more vividly and distinctly. As the one can see, the detection voltage is dropped when a positive current is detected. Hence, a blanking window interval is necessary at the beginning of the turn-on.

Since this method is based on the gate current monitoring, it can be also used to detect the reverse gate current caused by  $dV_{DS}/dt$  under FUL in a much shorter time than the one imposed in HSF, typically less than 1 microsecond. On the other hand, this current is much faster and of greater amplitude than what is detectable under HSF.

As a result, this method is a physical unique phenomenon, specific to SiC MOSFETs. It has high SNR tolerance, to easily realize and integrate. However, the protection intervenes after a few microseconds, which makes it slow compared to the other types of protection usually used. As well, the necessity of the blanking time, can be challenging for different SiC MOSFETs.

## 5.6. Gate Charge monitoring method

Another useful parameter from the circuit design point of view and the gate, is the gate charge  $Q_G$  [111]. Since the input capacitance of power MOSFETs is non-linear, the gate charge is an easier parameter for estimating switching behavior. In this method, the gate charge  $Q_{GD}$  is

related to  $C_{GD}$  which is predominant to distinguish between NTO, HSF and FUL. This method shows promising results for Si IGBT and SiC MOSFETs. It is based on the gate current, as the preceding method. In contrast to the other method, this one detects small changes at the beginning of the switching event, as well as the gate charge quantity, Fig.I. 45. Therefore, the circuit behind this method must have a high accuracy. The integration of current is given by eq.(I. 28).  $Q_G$  characteristic and the equation of each operation of the gate charge will be further more detailed in Chap.III.

$$Q_G = \int I_G * dt \quad (I. 28)$$

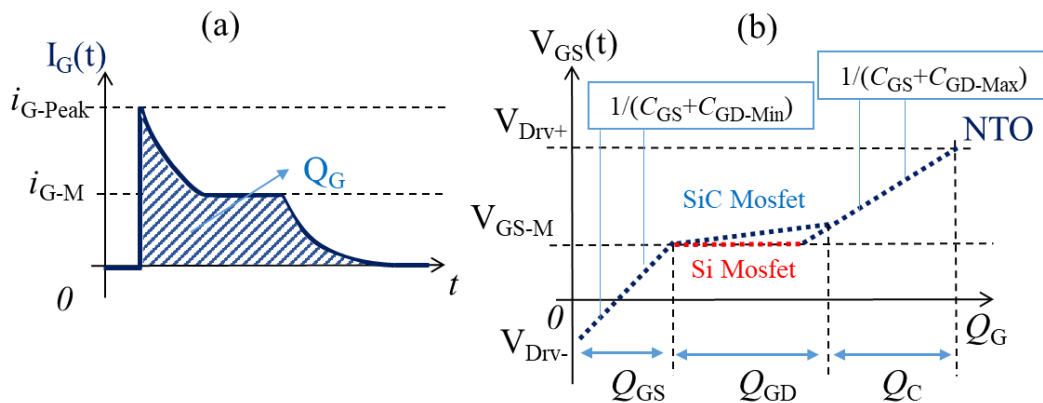


Fig.I. 45. (a).  $I_G$  curve under NTO (b). Gate Charge Characteristics under NTO.

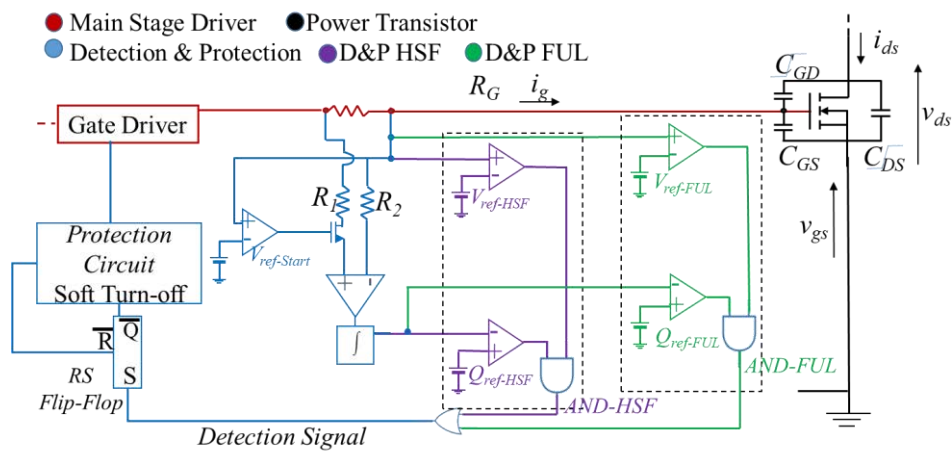
This method has no-time dependency, basically based on two references levels, a reference level on the gate-source voltage  $V_{GS}$ , and another on the gate charge integral. Therefore, this method can be included in the 2D diagnosis family.

In the case of a HSF short-circuit, for the same  $V_{GS}$ , the value of the charge is lower than in the case of a NTO, because there is no Miller plateau. The  $V_{Ref}$  should be set between  $V_{GS-M}$  and  $V_{Drv+}$ . The  $Q_{Ref\_HSF}$  should be set depending on the datasheet and the design of the integrator.

In the other case of FUL short-circuit, the value of the gate charge is slightly lower than NTO, but at higher  $V_{GS}$  called the gate overvoltage caused by the reverse gate current. The  $V_{Ref}$  should be set above  $V_{Drv+}$ . The  $Q_{Ref\_FUL}$  setting is easier than under NTO, because it should be set slightly lower than  $Q_{G\_Tot}$ . More detailed analysis of this method is presented in Chap.III.

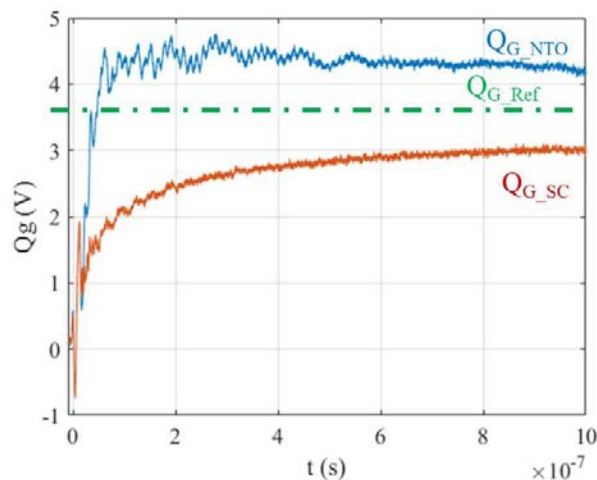
The main advantage of this method is that the detection is realized in low voltage monitoring, as close as possible to the gate driver, which allows it to be cheap and fast. On the other hand, the distinction between values of gate charges can be complex. Indeed, considering the oscillations created by the  $dI_D/dt$ , the parasitic inductances, the amplification chain and the noise, the  $Q_G$  calculation requires a high degree of accuracy. Moreover, for SiC MOSFET components and even more for GaN components, since the Miller  $C_{GD}$  capacitance is very low or even zero, it can be difficult to differentiate between a short-circuit and normal switching.

Fig.I. 46. shows standard gate charge detection schematic. The schematic is either for HSF or FUL faults, depending on the set of the references levels  $V_{Ref}$  &  $Q_{Ref}$  as mentioned above. The monitoring of the gate current across the gate resistance is made by a differential amplifier. The differential amplifier across  $R_G$  provides an image of the gate current  $I_G$  which is later integrated to calculate the  $Q_G$  [111]. Each of  $V_{GS}$  and the output of the integrator are sent to two comparators, respectively each one is compared to its reference level. The outcome of both comparators are added with an AND gate, then sent to protect the power transistor. Other detection methods based on sensing the gate charge is proposed as in [112]. The [112] method circuit is based on a current mirror connected to gate driver transistors. The current mirror generates an image of the gate current, this current is integrated and then compared with a set of threshold level. The outcome of this comparator is the detection flag.



**Fig.I. 46.** Gate Charge monitoring method schematic for either HSF or FUL

Fig.I. 47. presents experimental results realized in this thesis. More in-depth details are presented in the Chap.III on this work. The figure presents the output of the integrator under NTO and HSF conditions, where we can see the major difference between the different operations.



**Fig.I. 47.** Experimental waveforms of the Integrator output signals under NTO and HSF conditions. @  $R_G= 10\Omega$ ,  $V_{GS}= -5/20V$   $V_{DS}= 400V$ , C2M0080120

### 5.7. Fault detection methods Summary / Benchmark

Different detection methods are presented above. Each method has its pros and cons. A short-circuit detection for Wide Band Gap power devices should be evaluated by the following aspects: fast response time, high accuracy, low power, high noise immunity and low cost [3]. Two comparative tables are presented, one about the approach and integration of the detection methods, Tab.I. 3. And the other table presents the comparison of the performance between the detection circuits, Tab.I. 4 [113] [114] [115].

**Tab.I. 3.** Approaches and Integration of basic approaches related to fault detection

<u>Methods</u>	<u>Terminal Pin</u>	<u>Approaches</u>	<u>Integration Capability in Gate Driver</u>
Shunt Resistor	Source	Straight forward	Difficult, external Sensing resistor
SenseFET	Additional Pin	Most Straight forward	Adapted chip
Transformer	Drain	Very Indirect	Very difficult, depending on the transformer
Desaturation	Drain	Very Indirect	External HV Diode
Gate current leakage	Gate	Indirect	Easy
Gate Charge	Gate	Indirect	Easy

**Tab.I. 4.** Performances comparison of basic approaches related to fault detection

<u>Methods</u>	<u>Responses time</u>	<u>Accuracy</u>	<u>Losses</u>	<u>Cost</u>	<u>Reliability</u>
Shunt Resistor	Short+	High, Depends on shunt quality	High (Rs)	High precision Sensing resistor	Low
ShuntFET	Very Short+ +	Medium, depends on scaling	Low	Non-Standard Chip	High
Transformer	Very Short	Medium, depends on the transformer	High	Rogowski coil	Low
Desaturation	Long (Blanking time)	Low for SiC MOSFET	Negligible	High Voltage sensing Diode	Low for SiC MOSFET
Gate current leakage	Very long (Blanking time)	High, depends on $V_{Ref}$	-	Low-Voltage Circuits	Very high
Gate Charge	Very short	Medium, depends on Diff.Amp	-	Low-Voltage Circuits	High

SiC MOSFETs are promising power semiconductor switches to improve efficiency and to reduce system size. Some SiC MOSFETs seem much less robust to short-circuits and higher switching frequencies. The 10 $\mu$ s per 1000 short-circuit cycles, well known for industrial-class IGBTs, are not at all guaranteed for SiC MOSFETs today. Therefore, the sensing device will have to be much faster and more immune to high dv/dt parasitic noises.

The detection and protection turn-off time should be less than a fourth of the critical time  $t_{sc-Max}$ , the short-circuit withstand time. Thereby, it does not only give a warning about an abnormal behavior between the drain and source, in the power loop, but it also prevents the gate oxide damaging, which could increase the gate current leakage.



Short-Circuit detection methods should comply with the new paradigm of SiC devices, by increasing their accuracy, and noise immunity; and by reducing their power loss, response time and cost. Improvements should be made from the gate drivers and PCB as well. Therefore, further work to integrate SC detection and protection circuit on a gate driver will be described.

**Tab.I. 5.** Benchmark of the two main detection methods in the literature

<b>Methods</b>	<b>Reference</b>	<b>Year</b>	<b>Operating condition</b>	<b>Response Time</b>	
				<b>HSF</b>	<b>FUL</b>
<b>DESAT</b>	[94]	1995	IGBT $V_{Bus} = 420V$ $R_G = 50\Omega$ $V_{GE} = -10/15V$	$3\mu s$ ( $t_{BLK} > 500ns$ )	
	[108]	2018	SiC MOSFET $V_{Bus} = 600V$ $V_{GS} = -5/20V$ $R_G = 12\Omega$	$2.2\mu s$	-
	[105]	2018	SiC MOSFET $V_{Bus} = 600V$ $V_{GS} = -5/20V$	$500ns$ (including $t_{BLK}$ $250ns$ )	$670ns$ (including $t_{BLK}$ $420ns$ )
<b>Gate Charge</b>	[111]	2014	Si IGBT $V_{Bus} = 300V$ $R_G = 25\Omega$ $V_{GE} = -10/15V$	$1\mu s$	$3\mu s$
	[112]	2010	Si IGBT $V_{Bus} = 300V$ $R_G = 25\Omega$ $V_{GE} = -10/15V$	$<1\mu s$	-
	[116]	2019	SiC MOSFET $V_{Bus} = 650V$ $R_G = 25\Omega$ $V_{GE} = -10/15V$	$1.2\mu s$	-

## 6. Conclusion

This chapter presents the background motivation of this thesis. After presenting the development of power modules in the recent years, the focus was on the SiC MOSFETs component which is the main element, presenting promising efficiency (speed, quality and costs). This chapter highlights the main parameters of SiC MOSFETs to take into consideration when the design of a function related to SiC MOSFETs is under consideration. The chapter can be separated into two main section respectively to two functions, the control/command of SiC MOSFETs and the detection/protection of SiC MOSFETs under short-circuit. Each part has its own key players in order to design an adapted gate driver with short-circuit monitoring function, with very high speed and accuracy. SiC MOSFET characteristic study is mandatory in order to differentiate between normal operation mode and short-circuit operation mode. Several functions are not developed in the course of this thesis, as the isolation and the gate driver power supplies; as well as; all the charming monitoring methods such as  $dV/dt$  monitoring or dead-time optimization. Therefore, the next chapters present the novel developed functions, the buffer including mandatory functions and the detection/protection methods.

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## Chapter II: Design of integrated gate drivers in 0.18 $\mu$ M SOI CMOS technology for MOSFET SiC

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## **Chapter II: Design of integrated gate drivers in 0.18 $\mu$ m SOI CMOS technology for MOSFET SiC power device**

*After having studied the gate driver mandatory functions, and integration levels, in the first chapter, this study focuses on the output buffer to control the power transistor. Two buffers architectures are proposed. The first one is a straightforward solution, adapted to the needs of fulfillment of this thesis. In other words, few complementary functions were added to the buffer, and a novel short circuit detection functions is designed and integrated, in order to have a gate driver worthy of its name. The short-circuit function is presented in the third chapter. The second buffer, is an exploratory study which is focused on a modular architecture for close control at several bias voltage levels taking advantage of SOI isolation and low voltage CMOS transistors to drive SiC MOSFETs and improve their robustness and reliability through active and dynamic multi-level selection of switching sequences and on/off states. The structure contains several buffers in series in order to have a modular multilevel active gate driver MMAGD.*

### **1. Introduction**

SiC MOSFETs present better figure of merit, and are better candidates to take over the market, as developed in Chap.I. Their gate drivers are following the trend in order to keep up with this high efficiency provided by SiC MOSFETs. However, the lack of a gate driver compatible with the capabilities of the power components can limit the performance of wide-bandgap-based power converters. There is a clear trade-off between the SiC MOSFET power transistor and the gate driver. Moreover, different configurability (shortened design cycle, design flexibility, etc...) and different monitoring and control function (better diagnostics, enhanced reliability) are needed in order to ensure the safety and the well behavior of both environments, (Gate driver, and power converters). One of the main functions integrated in the gate drivers is the reliability of detection and protection against short circuit (SC) events. This detection and protection should be fast since SiC MOSFET short-circuit withstand capability is shorter compared to Si IGBTs. In addition, the SiC MOSFET has a much lower endurance for repeated short-circuit events than a silicon device. Therefore, the SiC MOSFETs gate driver compared to the Si IGBT ones have lesser time to detect the SC and protect the power device and to avoid ageing of the chip. Besides the detection methods developed in Chap.III, this chapter will be focused on adapted gate drivers for SC behavior and SiC performances. First gate driver is a host to the detection functions, with other features. And the second one, is a multi-level gate driver that will allow to improve the reliability of SiC MOSFET and reduce their stress under SC operation, therefore increase the lifetime of the device.

### **2. Design of the power test benches**

In order to characterize and to observe electrical behavior of the SiC MOSFETs under normal operations and short-circuit operation, and to observe and study the behavior of the CMOS gate driver, a power test bench is required. The power test bench must be a host for both the power

device DUT (device under test) and the CMOS gate driver. As well as, the test bench should allow high voltage capability higher than 600V, and low voltage capability to supply the gate driver.

Two power test benches were designed within the lab. The first one V1 is developed within F.Boige's Ph.D. work [99]. The second one V2 is more an extended version of the V1, accumulating the experience from the V1 in order to enhance the performance towards a better version.

## **2.1. Power Test bench V1**

The power test bench presented in Fig.II. 1, has for purpose to be able to offer switching characterization, to test both short-circuit type faults (type I, type II) and to carry out double pulse configuration. The test bench is designed taken into consideration different aspects:

- Operates up to 600V with current pulses up to 500A in the main loop without significant variation of the bus voltage.
- Small power loop inductance, in order to avoid high voltage surges at the turn-off, and SC.
- Fast safety circuits are included (active and passive devices, as fuses, ...), in order to protect from destruction of the bench or even explosion of the components during critical failure of the semiconductors under test.
- Highly accurate measures of the power loop current.
- Adjustable and flexible positive/negative bias voltage of the gate driver.
- Easily replaceable gate driver.
- Flexibility in changing the device under test DUT. (limited to TO-247-3 packages)

An adjustable voltage (0-600V) current-limited DC power supply is used, with 4 film capacitors of 220 $\mu$ F placed in parallel with the power voltage source. Then as close as possible to the power loop, 1 film capacitor of 10 $\mu$ F was inserted to reduce as much as possible the inductive voltage at the time of switching and the ohmic voltage drop of the bus film capacitors, the stray inductance is less than 15nH. Only one capacitance has been placed in this second capacitance bank because the energy has to be reduced at this level of the circuit. Indeed, being placed after the fuses (circuit breaker), the energy will be dissipated in the power component that could cause its explosion, in case of a faulted DUT. The PCB is designed with 4 metal layers and was carefully designed in order to consider short paths, less inductance, minimization of the EMI perturbations, ...

In general, the DUT is the component placed in the low side LS position. Voltage measurement can therefore be made with classical voltage probes (non-differential probes, referenced closer to the converter ground). The potential reference of the measurements has been taken on the kelvin source of the DUT, which is at the ground potential. Low voltage signals (as  $V_{GS}$  and  $V_{Drv}$ ) are mostly measured with self-compensated voltage probes (300 V and 1 GHz bandwidth (BP) Tektronix TPP1000). High voltages (as  $V_{DS}$ ) is typically measured with a probe (1000 V

and 800 MHz BP Tektronix TPP0850). The current is measured through a shunt resistor by a conventional coaxial cable of minimum length. On the other side, if a component is placed on the high side HS, a 1000V differential voltage probe is required. A 1GHz bandwidth oscilloscope (Tektronix DPO414B) is used to measure the different signals. The propagation time of the probes has been compensated in order to align the waveforms. Moreover, a generic plug-and-play gate driver is used, typically using IXDD614. For gate drivers with different potential as their ground, another isolated oscilloscope is required. The isolation can be done through a transformer or an oscilloscope with an internal battery.

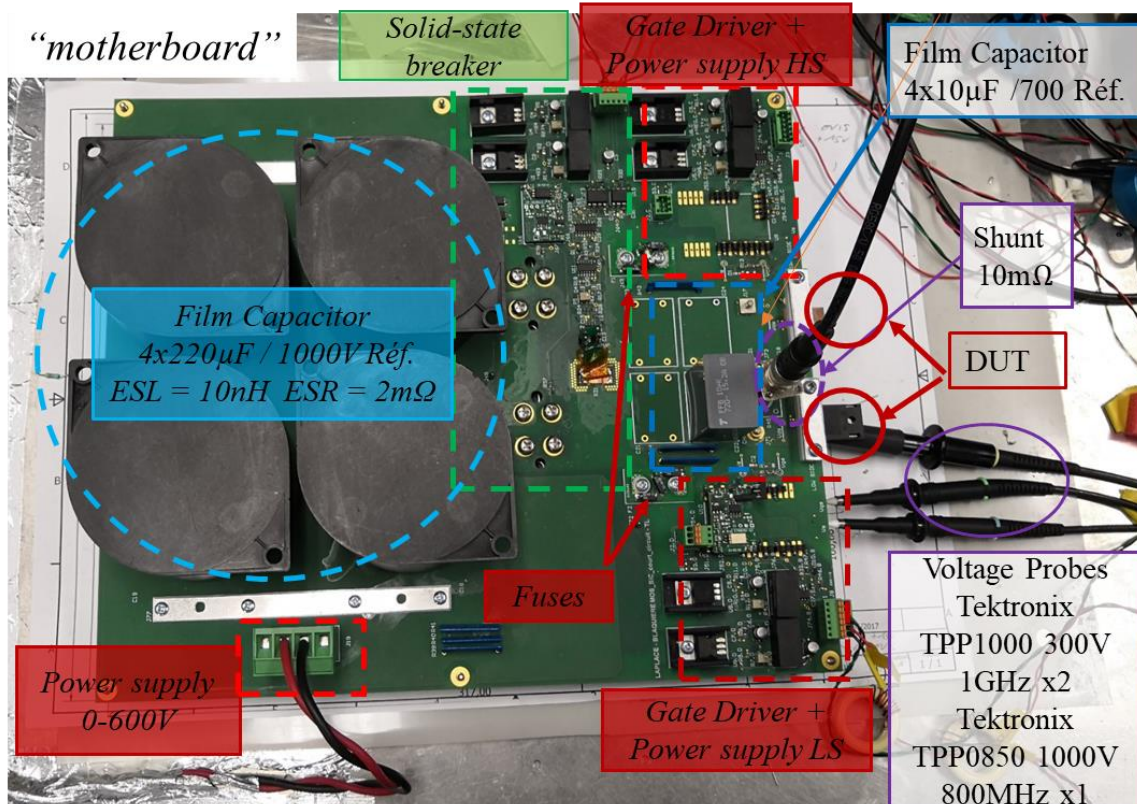


Fig.II. 1. Test bench V1 for Extreme short-circuit and double pulse operations

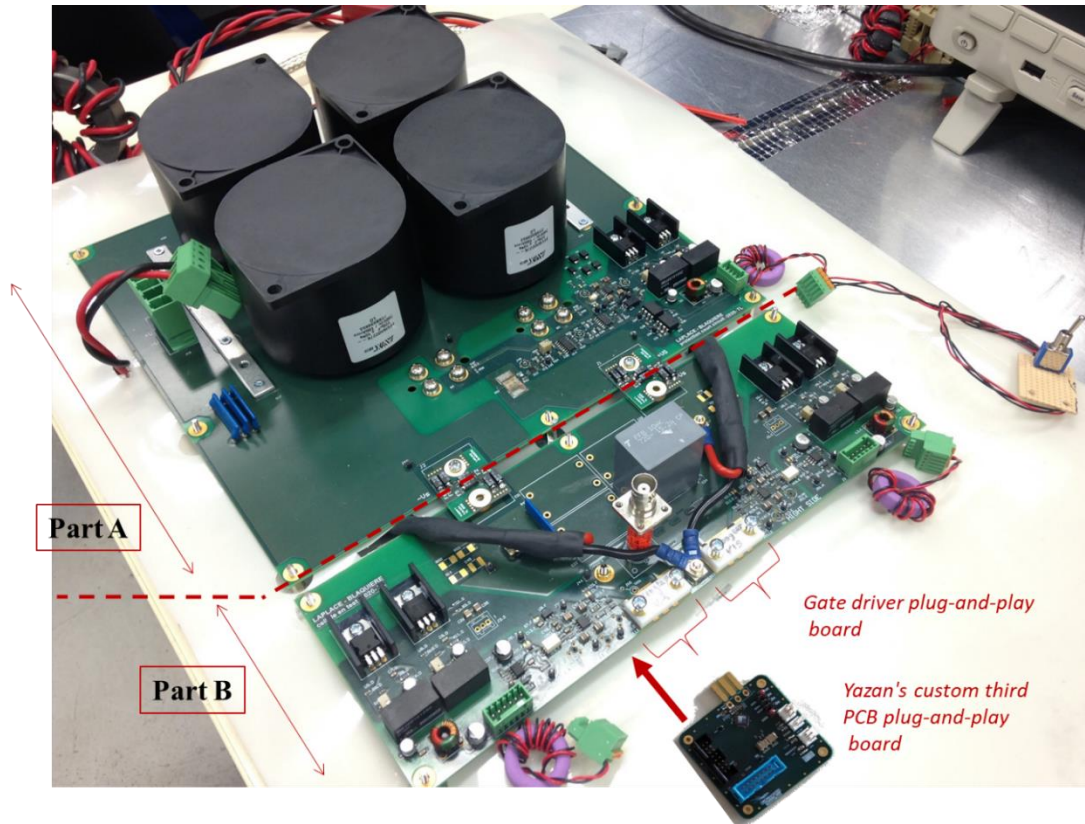
## 2.2.Power Test bench V2

The second power test bench is divided in two separated parts, part A and part B. This separation offers the flexibility in case the second part is required to be modified for different reasons.

- Part A: Standalone principal board. This part consists of pulse power capacitors bank, and two safety stages. The first stage consists of an electronic fast breaker (900A max -  $t_{delay} < 500ns$ ); and the second one which is an ultimate safety stage, consists of SMD bar dual-fuses. This SMD bar connects both parts.
- Part B: Custom secondary board. This part is a host for an inverter phase-leg or synchronous buck switching cell, using a DUT with TO220/247. This part consists of an optional generic dual isolated gate-drive embedded with  $V_{GS\_on}/V_{GS\_off}$  adjustment (SiC MOSFET SiC and GaN compatibility) 2GHz coaxial 10m $\Omega$  high-pulse current shunt (2J). This generic gate-driver can be electrically disconnected by straps on the



PCB, and to use instead an external gate-driver PCB circuitry with an embedded DUT. Moreover, Decoupling capacitors are added as close as possible to the DUT, for both cases.



**Fig.II. 2.** Test bench V2 600V -160J, for extreme short-circuit and double pulse operations

### 3. CMOS technology and Buffer specification

In order to realize the desired integrated functions; it is necessary to choose a technology adapted to our requirements. There is a wide choice of foundries such as AMS, X-fab, On-semiconductors, ST-microelectronics, TSM, UMC and others. Each of those foundries proves their utilities and main strength in different applications. These technologies services are accessible via Europractice [117] a shared manufacturing service, (multi project wafer MPW) or CMP (circuit multi project) [118]. Tab.II. 1 presents a brief overview comparison between the CMOS technologies. The table presents elements which will be our first pre-dimensioning specifications. The elements are miniaturization, cost, operating voltage and temperature. In order to have high operation performances and offers high voltage transistors and thick metallization for better routing for high current level functions.

Most of the developed functions in the integrated circuit IC require the existence of an electrical isolation between the circuits, whose potentials are referenced at two different local ground levels. As a solution, the use of high voltage lateral technology on insulated substrate (SOI silicon on insulator) is required. It provides complete electrical isolation of each component by the possibility of using buried oxide and lateral oxide layers. Moreover, HV transistors using SOI technology are better in terms of latch-up immunity, integration density, and performance.

**Tab.II. 1.** Technologies comparison [119]

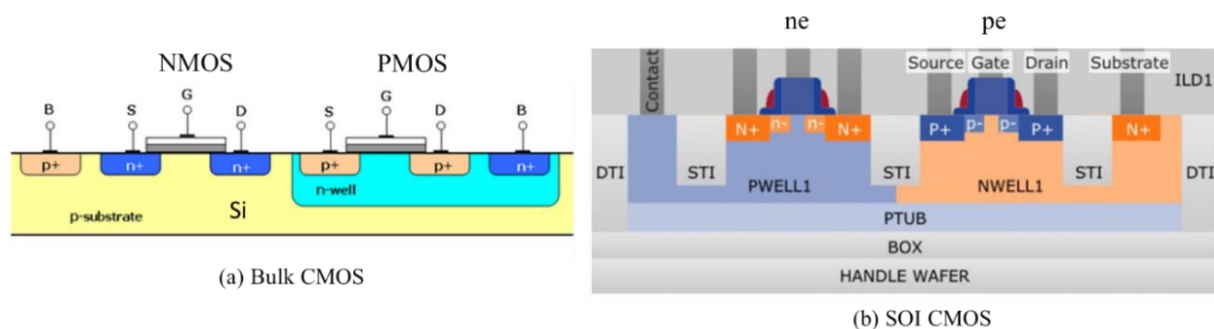
CMOS Technologies	AMS LV C35B4C3	AMS HV H35B4D3	X-Fab SOI	ST-Microelectronics SOI
Channel length	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	180nm	160nm
Operational Voltages range	3.3V/5V	3.3V/5V/20V/50V/120V	1.8V/5/10V/40V/60V/100V/200V	1.2V/3.3V/6V/20V/40V/70V/200V
T° <sub>Max</sub>	125°C	125°C	175°C	175°C
Cost via Europractice/CMP	640 €/mm <sup>2</sup>	800 €/mm <sup>2</sup>	1635 €/mm <sup>2</sup>	2500 €/mm <sup>2</sup>

### 3.1.SOI CMOS 0.18 $\mu\text{m}$ Technology

Silicon on Insulator SOI technology is used in several applications such as radiation-hardened and low-power high performance applications, and more importantly high voltage integrated circuits. One of several other microelectronics manufacturing processes is still working on extending Moore’s law. SOI technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon in semiconductor manufacturing. Dielectric isolation feature allows to reduce significantly the junction capacitance, thereby improves the performance of the circuit (increase the speed and reduce the power).

#### 3.1.1. Bulk CMOS vs SOI CMOS

Fig.II. 3 presents the difference between the Bulk and the SOI structures, where SOI has no wells into the substrate (complete isolation of the n- and p- well) and therefore no latch up problems (higher density) or leakage path. Lower parasitic capacitance due to isolation from the bulk silicon ( $C_{DS}$  significantly reduced by eliminating the depletion regions extending into the substrate), which improves power consumption and speed at matched performance. Reduced temperature dependency due to no doping and reduced antenna issues. Improves the short channel effect and soft error immunity.[120]



**Fig.II. 3.** LV transistors (a) Bulk CMOS layer structure (b) SOI CMOS layer structure

3.1.2. 0.18 Micron Modular BCsD-on-SOI Technology

The XT018 series is X-FAB’s 0.18 µm modular high-voltage BCD-on-SOI technology. It combines the benefit of SOI wafers with Deep Trench Isolation (DTI) and those of a state-of-the-art six metal layers 0.18 µm process, Fig.II. 4. High voltage devices support up to 200V combined with a full range of Non-Volatile-Memory options. The XT018 platform is specifically designed for the next generation automotive, industrial and medical applications operating in the temperature range of -40 to 175 °C.

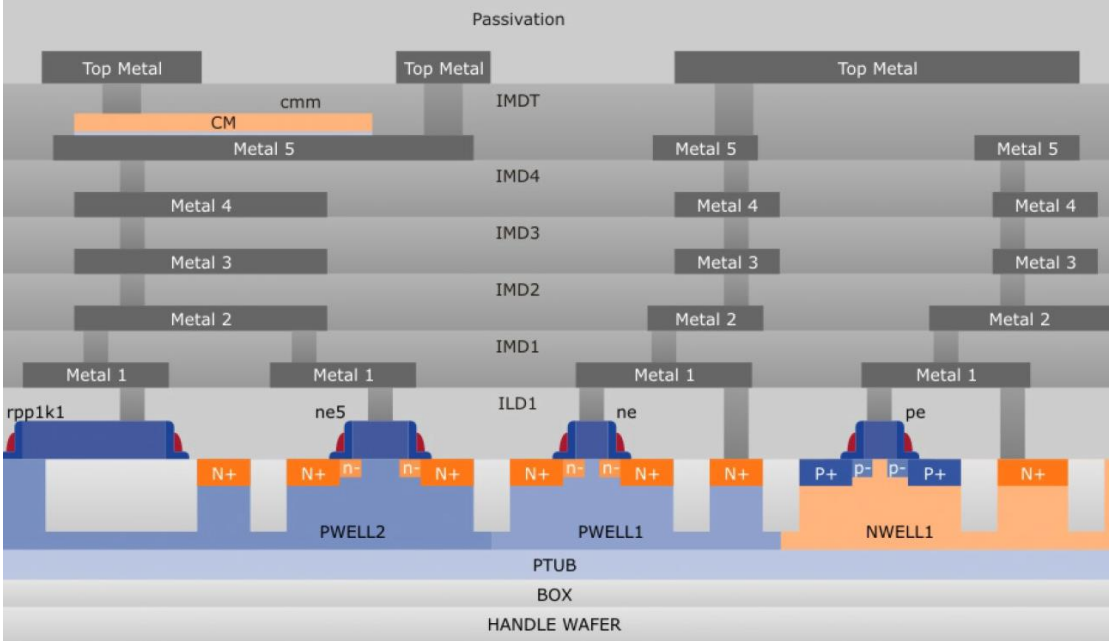


Fig.II. 4. View of different layers of the X-Fab CMOS SOI 0.18µm technology [121]

Complementary modules are available with the X-Fab design kit, as logic functions under 1.8v and 5v, high/medium resistance polysilicon modules, single / double / triple MIM capacitor modules, high capacitance single / double / triple MIM capacitor modules, various diodes modules, and many other functions and modules, with their associated schematics, models and layout.

The software used to design and draw the layout is Cadence Virtuoso. Cadence Virtuoso allows different levels of design. Circuit design and transistor sizing is done under “Schematic Editor”. Simulation validation and PVT (process-voltage-temperature) corners is done under “ADL or ADXL” (analog design environment). Layout design is done under “LayoutXL”, there is an automatic generator of path and wires, but not adapted to current calls, therefore the layouts are handmade. Thanks to Assura or PVS (DRC and LVS) (Design rule checking) (layout versus schematic) , the layouts are validated and verified for any design rules errors, or any differences between schematic and layout. In this thesis, two runs have been sent using europractice, first one included the active gate driver AGD with detection circuit (buffer\_V1) + multi-level modular active gate driver MMAGD + HV capacitors (08/2019) and the second run included other detection circuits (03/2020).

### 3.2. Buffer Specifications and adaptation

SiC MOSFET transistors show a better index of merit ( $R_{DS\_ON} \times Q_G$ ) compared to Si IGBT transistors. They allow high-frequency operation with an excellent level of performance, making power converters smaller, faster and more efficient. Therefore, Tab.II. 2 presents the targeted power device to be controlled. The devices are from the WolfSpeed Cree manufacturers, have a wide range of choices in current and voltages. The choice of these devices is based on their merit index ( $R_{DS\_ON} \times Q_G$ ), their input capacitance (useful for the detection of Short-Circuit, see Chap.III) and studies are already have be led in different aspects of these transistors within the lab. One of the main focuses of this thesis is SC monitoring for SiC MOSFETs. Therefore, the gate driver should be adapted for this function, and should be able to show promising operational results for a wide range of SiC MOSFETs devices available in the market. The scope of this study will not include isolation functions and power supplies for the gate driver.

**Tab.II. 2.** Different SiC MOSFETs power transistors for both 2<sup>nd</sup> and 3<sup>rd</sup> generation

Typical Parameter	C3M 0120090J	C3M 0075120K	C3M 0032120K	C3M 0016120K	C2M 0025120D	C2M 0040120D
$V_{DS}$ (V)	900	1200	1200	1200	1200	1200
$I_D$ (A)	22	30	63	115	90	63
$R_{DS\_ON}$	120m $\Omega$	75m $\Omega$	32m $\Omega$	16m $\Omega$	25m $\Omega$	40m $\Omega$
$V_{GS\_op}$ (V)	-4/15	-4/15	-4V/15	-4V/15	-5/20	-5/20
$V_{th}$ (V)	2.1	2.5	2.5	2.5	2.6	2.6
$R_{G\_INT}$	16 $\Omega$	10.5 $\Omega$	1.7 $\Omega$	2.6 $\Omega$	1.1 $\Omega$	1.8 $\Omega$
$R_{G\_EXT\_op}$	2.5 to 20 $\Omega$	0 to 20 $\Omega$	2.5 to 20 $\Omega$	0 to 20 $\Omega$	2.5 to 20 $\Omega$	2.5 to 20 $\Omega$
$Q_G$ (nC)	17.3	51	118	211	161	115
$C_{ISS}$ (pF)	350	1350	3357	6085	2788	1893
$C_{RSS}$ (pF)	3	3	8	13	15	10
$t_r/t_f$	9/5ns	11/11ns	18/9ns	33/13ns	32/28ns	52/34ns
$t_{d\_on}/t_{d\_off}$	12/15ns	22/33ns	25/32ns	34/65ns	14/29ns	15/26ns
$\tau_{iss}@R_G=10\Omega$	3.5ns	13.5ns	33.5ns	60.8ns	27.9ns	18.9ns
$i_{G\_Peak}$ (A)	3.2	1.15	3.57	5.77	5.5	4.5

Note: op\* stand for recommended operational values. For more details, check their respective datasheet.

Typically, SiC MOSFETs are driven between -4/15V and -5/20, as shown in the Tab.II. 2, with an average internal/external gate resistance equal to 10 $\Omega$ . The choice of the gate voltage should be at least higher than the threshold voltage in order to turn-on the device and lower to turn it off. Increasing the gate voltage reduces  $R_{DS\_ON}$  of the power device therefore increasing conduction losses. Moreover, increasing the gate voltage for a given  $R_{G\_Ext}$  increases the gate charge  $Q_G$  therefore the gate current and switching losses. The impact of the gate resistor is



very important to establishing the specifications of the gate driver, especially its output buffer. High gate resistor values limit the peak value of the gate current, slow the switching speed of the SiC MOSFETs, therefore more power losses and potential heat issues are presented, affecting the performance of the transistor. On the other hand, low gate resistance increases the switching speed and become more sensitive to voltage surge and oscillations, while increasing the chance for device failure and damage.

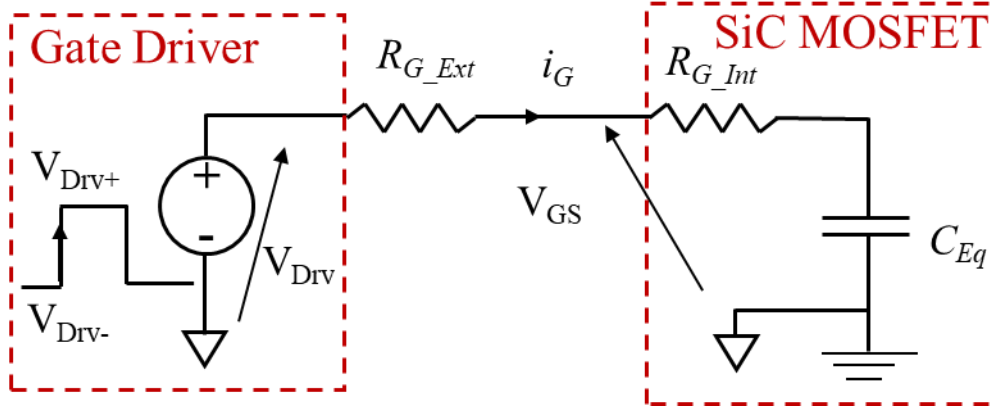


Fig.II. 5. Simplified circuit between the gate driver and the SiC MOSFET

A simplified circuit between the gate driver and the SiC MOSFET power transistor, is illustrated in Fig.II. 5. Both resistances in the figure (internal and external) are equivalent to the gate resistance  $R_G$ . The equivalent capacitor  $C_{Eq}$  and the internal gate resistance  $R_{G\_INT}$  represents the SiC MOSFET. This equivalent capacitor is the input capacitance of the SiC MOSFET  $C_{iss}$ . This equivalent schematic gives place to different equations, in order to support the choice and the sizing of the gate driver. At first,  $V_{Drv}$  is considered with an infinite slew rate.

$$i_{G_{t=0}} = i_{G\_Peak} = \frac{(V_{DRV+} - V_{DRV-})}{R_G} = \frac{V_{Drv}}{R_G} \quad \text{with} \quad \tau = R_G * C_{iss} \quad (\text{II. 1})$$

$$i_{G\_Peak} = \frac{V_{Drv} * C_{iss}}{\tau_{iss}} = \frac{Q_{iss}}{\tau_{iss}}$$

Therefore, temporal equation can be presented as:

$$V_{GS}(t) = V_{Drv} * (1 - e^{-\frac{t}{\tau_{iss}}}) \quad (\text{II. 2})$$

$$i_G(t) = C_{iss} * \frac{dV_{GS}}{dt} = \frac{V_{Drv}}{R_G} * e^{-\frac{t}{\tau_{iss}}}$$

The energy  $E$  supplied from the gate driver source is given in eq. (II. 3), and the gate charge losses can be calculated using

$$E = \int V_{Drv} * i_G * dt = \int V_{Drv} * \frac{dQ_G}{dt} * dt = \int V_{Drv} * dQ_G \quad (\text{II. 3})$$

$$P_G = V_{Drv} * Q_G * f_{Drv} \quad (II. 4)$$

The power lost to drive the gate of the MOSFET transistor is dissipated in the gate driver circuitry, given in (II. 5). the dissipating components can be identified as the combination of the series ohmic impedances in the gate drive path. In every switching cycle the required gate charge has to pass through the driver output impedances, the external gate resistor, and the internal gate mesh resistance. As it turns out, the power dissipation is independent of how quickly the charge is delivered through the resistors. For a CMOS gate driver with a PMOS and NMOS, their equivalent resistors are respectively  $R_H$  and  $R_L$ . The driver power dissipation can be expressed as eq.(II. 5). [122].

$$P_{Drv\_ON} = \frac{1}{2} * \frac{R_H * V_{Drv} * Q_G * f_{Drv}}{R_H + R_G} \quad (II. 5)$$

$$P_{Drv\_off} = \frac{1}{2} * \frac{R_L * V_{Drv} * Q_G * f_{Drv}}{R_L + R_G}$$

The choice of the power transistor ranges and the presented equation, led to a set of driven voltage range, with an average resistor choice. Moreover, a gate driver with large source and sink currents will result in large silicon areas. Therefore, the targeted output peak current is around 3A. In order to support our choices a benchmark table for different gate drivers is presented in Tab.II. 3. These gate drivers are single channel isolated drivers commercially available. These gate drivers are compared regarding their peak current, driving voltage, propagation delay and rise & fall time for a given load capacitance.

**Tab.II. 3.** Comparison of the commercial gate drivers

<b>Driver</b>	<b>Silicon Labs</b> <b>SI8261BAC-C-IS</b>	<b>Infineon</b> <b>IED020I12</b>	<b>TI</b> <b>UCC27525</b>	<b>IXYS</b> <b>IXD614</b>
<b>I<sub>Peak</sub></b>	±4A	±2.4A	±5A	±14A
<b>V<sub>Drv</sub></b>	0/30V	-12/20V	-4.5/18V	-4.5/35V
<b>t<sub>p</sub></b>	40ns	160ns	17ns	50ns
	C <sub>L</sub> = 200pF	C <sub>L</sub> = 100pF	C <sub>L</sub> = 1.8nF	C <sub>L</sub> = 15nF
<b>t<sub>r</sub>/t<sub>f</sub></b>	5.5/8.5ns	30/50ns	7/6ns	25/18ns
<b>T°</b>	125°C	150°C	125°C	125°C
<b>Year</b>	2011	2017	2015	2017

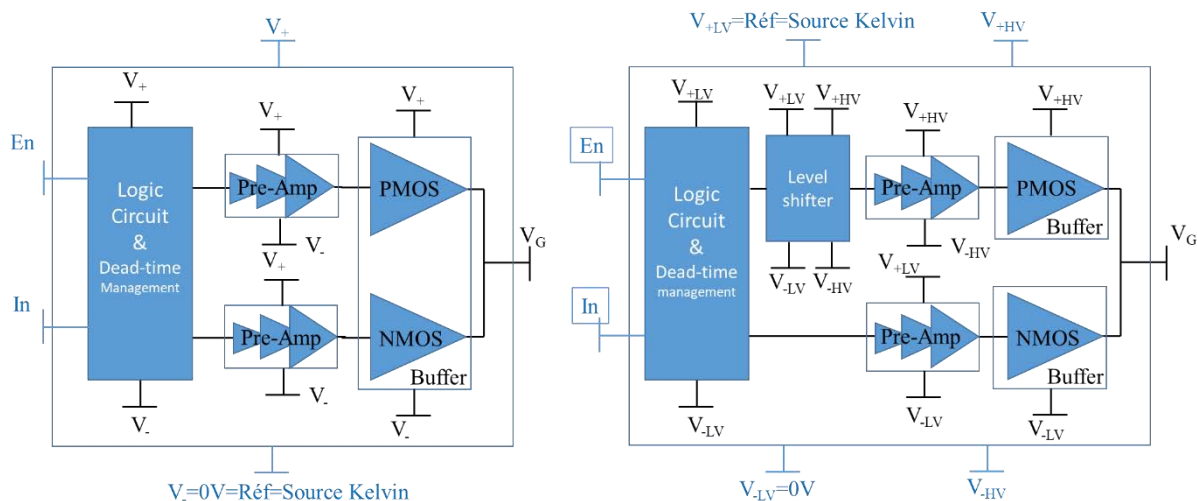
The propagation delay of the gate driver is high which adds more delay in order to protect the circuit or sending internal/external feedback signals. With regard to the analysis above, main parameters in order to design the buffer of the gate driver were highlighted. Indeed, new gate drivers must be able to transfer switching signals with low propagation delays (less than 30ns) and low levels of mismatch between channels (less than 5ns). This induces that the entire order transfer chain must be controlled, including the transfer of orders from the reference potential

of the remote control to the transistor gate. In fact, they must withstand the consequences induced by high switching edges  $dV/dt$  above  $50\text{kV}/\mu\text{s}$  and up to  $200\text{kV}/\mu\text{s}$ , with suppression of common mode coupling between the control loop and the external switching command, static immunity is required between  $600\text{V}$  and several hundred  $\text{kV}$ .

In order to be able to simulate the behavior of the AGD under power transistors effects, the power transistor model should be integrated in cadence. In order to do so; Wolfspeed provides files in format “.lib” that illustrate the sub-models and the behavior of the SiC MOSFET. This library files are commonly used under LTSpice™. Thanks to a team work [Bau Plinio & Barazi Yazan], the library files .lib is converted to spectre language “.scs”. For more details about the translation and the steps in order to do so, check Appendix. A.

### 3.3. Buffer Architecture & Technology options

Different CMOS buffer structures are proposed in the literature. Fig.II. 6 presents two different architectures, commonly used and straightforward. These architectures are based on an output buffer (large width PMOS, NMOS), which generates the gate current and the output voltage. A pre-Amp, amplifies gradually the current through the output buffer. And a logic circuit, in order to control the dead-time between the two channels and as well as managing all the logic signals in the circuit, for complex functions. Moreover, the output PMOS and NMOS must have  $BV_{DS\_Max}$  beyond  $V_{Drv+}$ - $V_{Drv-}$ . On the other hand, they are commanded with  $V_{GS} < V_{GS\_Max}$ . in addition, the PMOS has the particularity of having its source connected to  $V_{Drv+}$ , so  $V_G$  must be at least  $V_{Drv+} - V_{GS\_Max}$ . One last thing, classically, the "HV CMOS" components with  $BV_{DS} > 5\text{V}$  or  $10\text{V}$ , have a  $V_{GS\_Max}$  lower than  $V_{DS\_Max}$ . Therefore, a voltage regulator might be necessary in the case where the gate voltage of the PMOS is lower than the output voltage. In this case the double power supply architecture, is no longer useful, Fig.II. 6.(a), and the quadruple power supply architecture takes place Fig.II. 6.(b).



**Fig.II. 6.** Block diagram of the Output buffer with (a). double power supply (b). quadruple power supply

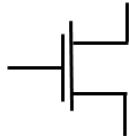
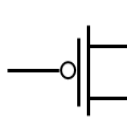
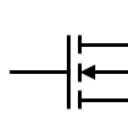
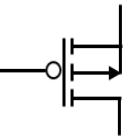
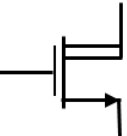
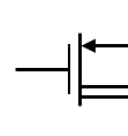
In order to decide which architecture is suitable for our application, a technology component study is necessary. Therefore, Tab.II. 4 is presented; illustrating the electrical parameters of the available transistors. Different transistors are available within the SOI X-Fab technology. However, several of them are not adapted to this work, (10V, 200V) (no need for higher voltages operation, or voltages operation with no safety margin). From this table different choices are available to size the output buffer structure and the pre-amplification buffers.

As SiC MOSFETs need to be typically driven around -5/+20V, the suitable structure is the quadruple structure, where the output buffer power supply is separated from the logic circuit power supply. Nhvta and Phvta transistors are the best fit to provide (15 – 25 V) with enough BV safety margin. And these transistors are driven with 5V, therefore (ne5, pe5) transistors are used to pre-amplify and command the output PMOS and NMOS (40V). It is the same circuit for the NMOS and PMOS preamp, (using 5V transistors). Expect that the PMOS preamp is isolated using DTI and referenced to V<sub>-HV</sub>.

The logic circuit can be powered by 1.8V transistor for better density and performance, but requires another voltage regulator and more power supplies. Moreover, on power environment it is not favorable to use such low voltage, which can be more sensitive to noise. Therefore, the logic circuit is being powered by the 5V.

On the other case, if 5V (ne5, pe5) transistors are used for the output buffer power supply, the output will be limited at 5V, which is good for transistors that are driven with 5V, as GaN. Or other solutions should be explored to reach -5/20V, (Chap.II.5). The one should note that the other structure with two power supplies can be used. In this case, the logic circuit can be powered by 1.8V transistors (ne, pe) and the output buffer with 5V transistors.

**Tab.II. 4.** Electrical parameters for the used CMOS transistors in the technology X-Fab 0.18 SOI

Parameters						
Type	ne 1.8V NMOS	pe 1.8V PMOS	ne5 5V NMOS	pe5 5V PMOS	nhvta low Ron 40V NMOS	phvta low Ron 40V PMOS
L <sub>min</sub>	0.18 $\mu$ m	0.18 $\mu$ m	0.5 $\mu$ m	0.5 $\mu$ m	0.4 $\mu$ m	0.5 $\mu$ m
V <sub>GS-Max</sub>	1.98V	1.98V	5.5V	5.5V	5.5V	5.5V
V <sub>DS-Max</sub>	1.98V	1.98V	5.5V	5.5V	40V	40V
V <sub>th</sub>	0.58V	0.65V	0.78V	0.82V	1.08V	1.07V
R <sub>DS_ON</sub> (K $\Omega$ $\mu$ m)	-	-	-	-	10.3 @W= 100 $\mu$ m	27.5 @W= 100 $\mu$ m
I <sub>DS</sub> ( $\mu$ A/ $\mu$ m)	515 @W= 10 $\mu$ m	195 @W= 10 $\mu$ m	520 @W= 100 $\mu$ m	280 @W= 100 $\mu$ m	200 @W= 100 $\mu$ m	131 @W= 100 $\mu$ m



## 4.1. Active gate driver Architecture

In this section, all the integrated functions will be presented, except the short circuit detection/protection (covered in chap.III).

### 4.1.1. Level shifter

Due to the use of transistors with 5.5V breakdown gate voltage, and in order to command HV PMOS transistors (40V), the use of a level shifter (or a similar topology) is mandatory. Level shifters are used in applications where there is a need to interface between different voltage domains. Two types of level shifters can be distinguished by whether the voltage domains share a common ground potential or not. Full-swing level shifters translates signals between voltage domains sharing a ground potential. These level shifters are commonly used in gate drivers for high voltage drain-extended MOS (DMOS) transistors, with medium or thin gate oxides where  $V_{GS\_Max}$  is significantly lower than  $V_{DS\_Max}$ . The second one, is the floating level shifters, where they are characterized by two voltage domains not sharing a common ground potential. The floating level shifters often translate signals up to high voltage levels of tens to hundreds of Volts. Sourcing charges from a high-voltage supply to ground will result in a high power consumption, rendering reduction of the current drawn from the high voltage supply paramount to the design of efficient floating level shifters [123]–[125].

In our case, the level shifter is used to shift the command of the PMOS from [ $V_{-LV}$  to  $V_{+LV}$ ] (0 to 5V) to [ $V_{-HV}$  to  $V_{+HV}$ ] ('5V to 10V' or '10V to 15V' or ... or '20V to 25V'); in order to stay proportional to 5V ( $V_{+HV} - V_{-HV} = 5V \pm 0.5V$ ). The design of the level shifter is realized for a typical gate driver power supply  $V_{Drv} = V_{+HV} + V_{+LV} = 25V$ , therefore the floating ground should be at  $V_{-HV}$  typically 20V. Moreover, the pre-amp of the PMOS is also at a floating ground. In order to summarize, the equations presented below explains in detail the analytical approach.

$$V_{GS\_P} = V_{G\_P} - V_{S\_P} \text{ with } V_{S\_P} = V_{+HV} \text{ and } 0 < |V_{GS\_P}| < |V_{GS\_Max}|$$

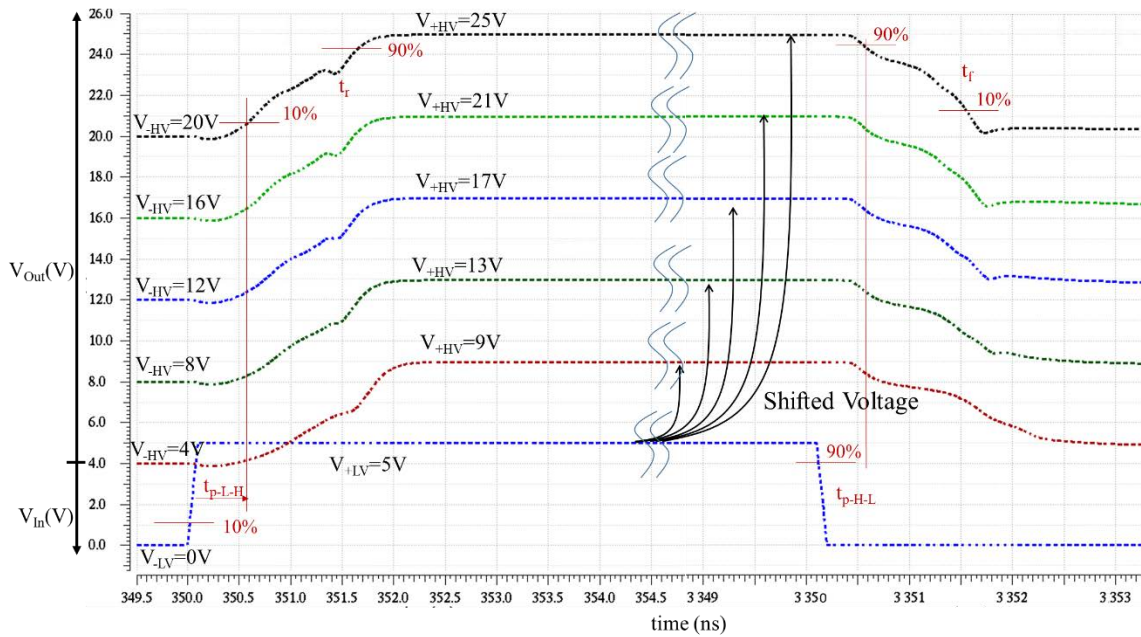
$$\text{Therefore, } V_{+HV} - |V_{GS\_Max}| < |V_{G\_P}| < V_{+HV} \quad (\text{II. 6})$$

$$\text{Moreover, } V_{-LV} < V_{logic} < V_{+LV} \text{ with } V_{+LV} - V_{-LV} < V_{GS\_Max} \text{ and } V_{DS\_Max} (5.5V)$$

After a review of different level-shifter topologies Fig.II. 8 is proposed. This structure uses both 5V transistors (ne5, pe5) and 40V transistors (phvta, nhvta). The high voltage potentials are  $V_{+HV}$  and  $V_{-HV}$ . And the low voltage domain is  $V_{+LV}$  and  $V_{-LV}$ . Nhvta and Phvta transistors includes DTI, deep trench isolation, which is a positive point when the isolation is needed between those two voltage domains (HV & LV). Each transistor in this structure should not exceed 5V difference at their drain-gate, drain-source and gate-source; specially M7 and M8. Ne5 and pe5 transistors are used intentionally for M7 and M8, in order to optimize the layout surface, therefore a DTI ring is necessary for both transistors, as well as for the PMOS pre-amp. In order to size the transistors, the DC operation of the circuit is investigated. Upon a low-to-high (0 to 5V) transition of  $V_{In}$ , M1 is activated pulling down the source of M3 to ground resulting in M3 pulling its drain to the ground as well (because the gate is permanently at 5V







**Fig.II. 9.** Simulated input and output of the level shifter under cadence

In order to avoid latch-up and mismatch problems, transistors are sized symmetrically, therefore M2/M4/M6/M8 are respectively seized as M1/M3/M5/M7, Tab.II. 6. Moreover, modification and changes are added to the size of the transistor regarding the simulation respond. R<sub>1</sub> and R<sub>2</sub> are both added to ensure a well-defined initial condition.

The Output of the level shifter is inverted compared to the PWM, therefore an inverter is added. this inverter represents the first inverter in the pre-amp of the PMOS chain. Tab.II. 7 illustrates simulated performance of the level shifter for different temperature, and as a load capacitor the 1<sup>st</sup> stage of the PMOS pre-Amp is used.

**Tab.II. 7.** Simulated performance of the level shifter for different temperature,

Performance	Min @ -40°C	Typ @ 27°C	Max @ 175°C
t <sub>r</sub> (ps)	744	982	1321
t <sub>f</sub> (ps)	880	1077	1415
t <sub>L-H</sub> (ps)	509	535	688
t <sub>H-L</sub> (ps)	414	435	471
<I> (μA)	31	41	56

#### 4.1.2. Output Buffer

The output buffer includes different blocks, the output buffer stage, their respective pre-amplification, their logic circuit, and level-shifter (developed in the section above).

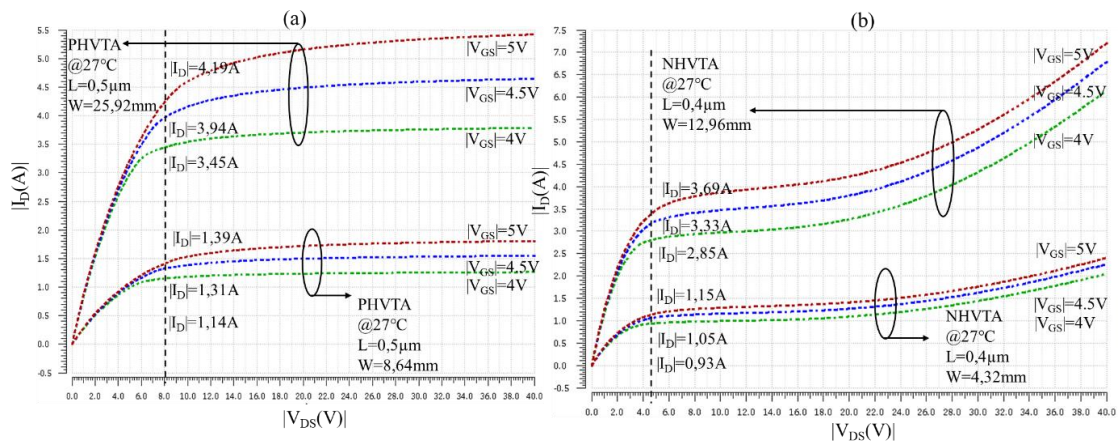
The output buffer stage consists of phvta and nhvta transistors as explained before, the used architecture is a push-pull. The purpose of the buffer stage is to provide the required SiC gate current; up to +/-3A. Therefore, the transistors are seized using eq.(II. 9), with a minimum transistor length L<sub>P\_Min</sub>= 0.5 $\mu\text{m}$ , L<sub>N\_Min</sub>= 0.4 $\mu\text{m}$ . Moreover, to have similar current capabilities

for both source and sink, the width of the PMOS must be greater than the NMOS. One should note that the mobility of the PMOS is approximately 2 time the mobility of the NMOS,  $\mu_p \approx 2 * \mu_n$ . Therefore, in the design  $W_{PMOS} \approx 2 * W_{NMOS}$  is considered.

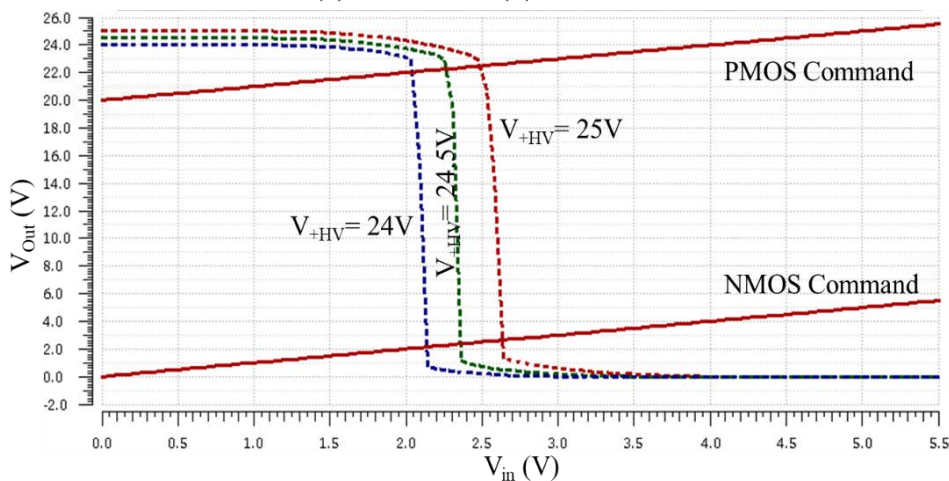
$$|I_{DSat}| \approx \frac{\mu_{n/p} * C_{ox}}{2} * \left(\frac{W}{L}\right)_{n/p} * |V_{GS} - V_{th}|^2 \quad (II. 9)$$

Before introducing the behavior of the buffer, the characteristics of the PMOS and NMOS are mandatory. Fig.II. 10 presents  $|I_D - V_{DS}|$  characteristics of both nhvta and phvta for different  $V_{GS}$ .

In order to reach 1 or 3 amperes capability at  $V_{GS}=4.5V$ , the PMOS transistor width should be respectively 8.64mm ( $R_{DS\_ON}= 4.75\Omega$ ) or 25.92mm ( $R_{DS\_ON}= 1.5\Omega$ ); and the NMOS transistor width should be respectively 4.32mm ( $R_{DS\_ON}= 2.75\Omega$ ) and 12.96mm ( $R_{DS\_ON}= 1.0\Omega$ ). Seizing transistors with a large width must follow certain rules, these rules are developed in Chap.II.4.2. The layout of the transistors contains a transistor multiplier (\*m), and for each transistor a number of fingers. The multipliers of the transistors represent how many transistors in parallel (more parallel transistors allows more current). Fig.II. 11 presents the simulation behavior of the (Output, input) voltage of the output buffer.



**Fig.II. 10.**  $|I_D - V_{DS}|$  characteristic under different  $V_{GS}$  and two different widths (1A,3A) for both 40V (a). PMOS and (b). NMOS

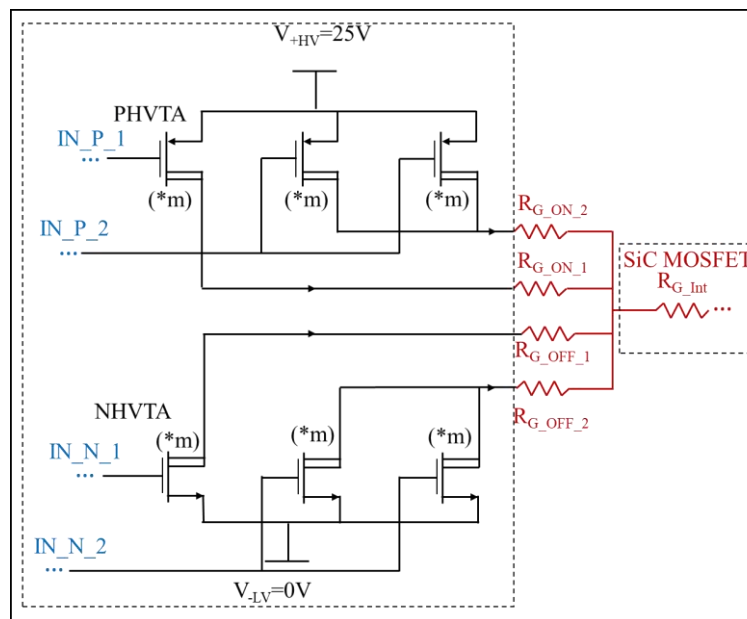


**Fig.II. 11.** DC characteristic of the inverter

The purpose of the output buffer is to have a “home-made” circuit, to demonstrate and validate the detection and protection circuit of Chap.III. It is important to be able to study the robustness and the protection technique under different gate charge dynamics. Therefore, it is important to easily modulate the gate current for a given DUT “SiC MOSFET” without having to solder/unsolder the external gate resistance. There are three possible solutions:

- Having a segmented PMOS and NMOS transistors, without operating with an external gate resistor. Thus, the buffer works more like a current source (but the important conduction losses are dissipated in the CMOS chip during gate charge and discharge). Another advantage of this solution is have only a single pad.
- Having a segmented PMOS and NMOS transistors, associated with a selectivity external gate resistance on each transistor output. Thus, the buffer works in voltage source mode. The current is defined by the external gate resistor which is being fixed by soldering/unsoldering different values and by different configuration of the output buffer.
- Both solutions can be mixed, so one of the segmented transistors can operates as a current source, and the other one + an external gate resistor as a voltage source.

In all cases, the buffer is sized according to the worst case, with separated segmented outputs (PMOS and NMOS), + discrete external gate resistance, Fig.II. 12. By doing so, two choices are presented, either connect them externally, or keep the split output in order to have more flexibility (different values for turn-on and turn-off gate resistors). More details on output buffer topologies are presented in [126]. It is recommended that the split external gate resistors should be equally to reduce the parasitic inductance which induce unbalance between the channels [127]. This separated rail-to-rail outputs simplify gate resistor selectivity, save an external high current bypass diode and enhance dV/dt control [31], [128].



**Fig.II. 12.** Segmented architecture with multiple outputs for different source/sink currents and different external gate resistors.

The segmented output buffer is separated into 1 ampere and 2 amperes sink/source currents, Fig.II. 12. The used split outputs require for each output segment its own pre-amplification. The selectivity of this current is managed by the logic circuit. This segmented output buffer allows three source/sink direct current configurations (e.g +/- 1.5A, +/- 3A, +/-4.5A) @ 27°C, enable bits are labelled EnP1, EnP2, EnN1, EnN2. Before going furthermore in details about the logic circuit, the pre-amplification circuit is necessary and needed to be developed.

The pre-amplification circuit does not only have the role of amplification but also dead-time management and propagation delay optimization. In our case, we choose to keep the management time at the logic circuit level.

For illustration purposes, the output buffer is reduced to one transistor, and one should note each configuration (1A/2A) has its own pre-amp circuit, Fig.II. 13. The pre-amp circuit consist of several CMOS inverters, that amplifies the current gradually (the width of the transistor increases as well). In order to have a high performance and less propagation delay, the number of inverters is decided to be 3 stages [39], [129]. For the PMOS and NMOS pre-amplification, 5V transistors (ne5, pe5) are used, albeit with DTI isolation for the PMOS preamp, due to the use of 5V transistors to command 40V transistors  $V_{GS\_Max}= 5V$ . The NMOS inverters are supplied with 5V between ( $V_{+LV}=5V$  and  $V_{-LV}=0V$ ). On the other hand, PMOS inverters are supplied with 5V (differential) where it is referenced between ( $V_{+HV}$  and  $V_{-HV}$ ), typically between 25V and 20V or 20V and 15V; depending on the chosen  $V_{+HV}$  voltage.

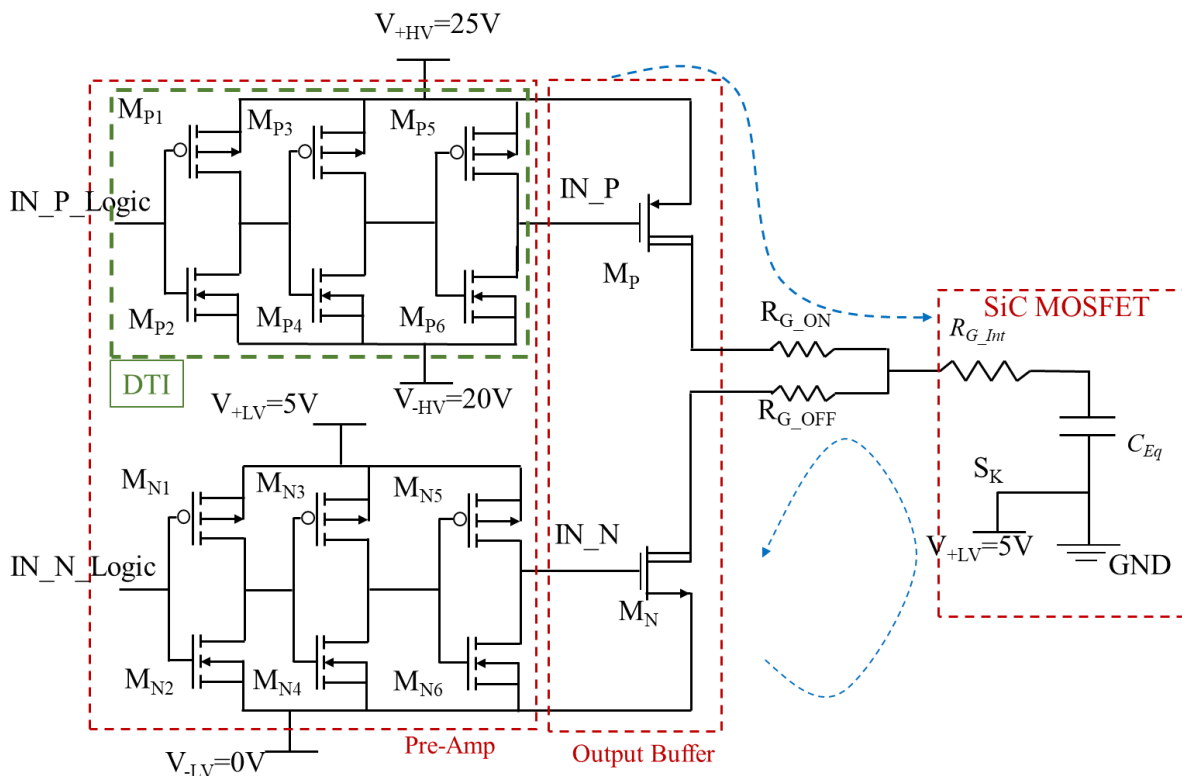


Fig.II. 13. Simplified structure of the PMOS and NMOS pre-amp

The pre-amp stages were sized reversely, starting with the last stage (the one directly connected to the 40V PMOS is stage 3). The 3<sup>rd</sup> stage is sized regarding the dynamic current required at the gate of the 40V PMOS of NMOS, then the 2<sup>nd</sup> stage is sized regarding the 3<sup>rd</sup> stage required current, and go on until the 1<sup>st</sup> stage is sized (few modifications have been done after simulation overview). Tab.II. 8 presents the provided current by each stage and the width of each transistor. In order to be able to control the pre-Amp of the PMOS which is referenced to 20V, a level shifter is required, presented in the section above.

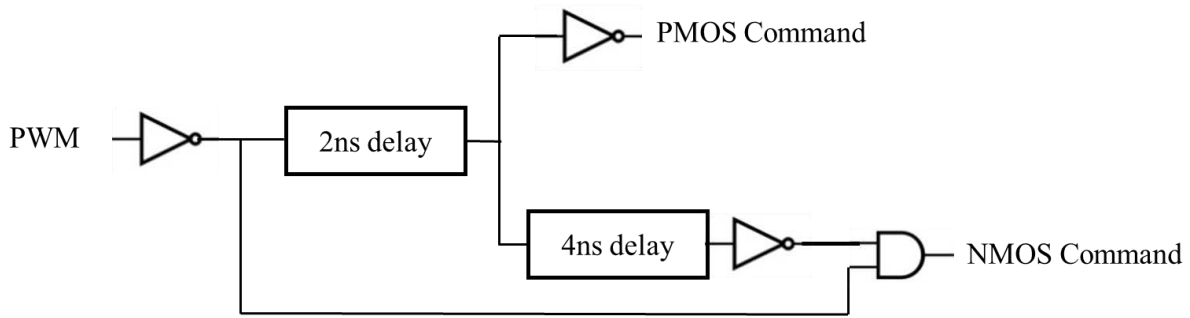
**Tab.II. 8.** Pre-amp stages source/sink current including width of each transistor

Pre-Amp	PMOS		NMOS	
	I <sub>Source</sub>	I <sub>sink</sub>	I <sub>Source</sub>	I <sub>sink</sub>
3 <sup>rd</sup> stage	225mA	100mA	22mA	22mA
	W <sub>Mp5</sub> = 600 $\mu$ m	W <sub>Mp6</sub> = 240 $\mu$ m	W <sub>Mn5</sub> = 120 $\mu$ m	W <sub>Mn6</sub> = 60 $\mu$ m
2 <sup>nd</sup> stage	22mA	22mA	2.75mA	1.3mA
	W <sub>Mp3</sub> = 120 $\mu$ m	W <sub>Mp4</sub> = 60 $\mu$ m	W <sub>Mn3</sub> = 15 $\mu$ m	W <sub>Mn4</sub> = 3 $\mu$ m
1 <sup>st</sup> stage	2.75mA	1.3mA	350 $\mu$ A	350 $\mu$ A
	W <sub>Mp1</sub> = 15 $\mu$ m	W <sub>Mp2</sub> = 3 $\mu$ m	W <sub>Mn1</sub> = 2 $\mu$ m	W <sub>Mn2</sub> = 1 $\mu$ m
0 Stage	350 $\mu$ A	350 $\mu$ A	-	-
(level-shifter)	W <sub>Mp0</sub> = 2 $\mu$ m	W <sub>Mp0</sub> = 1 $\mu$ m	-	-

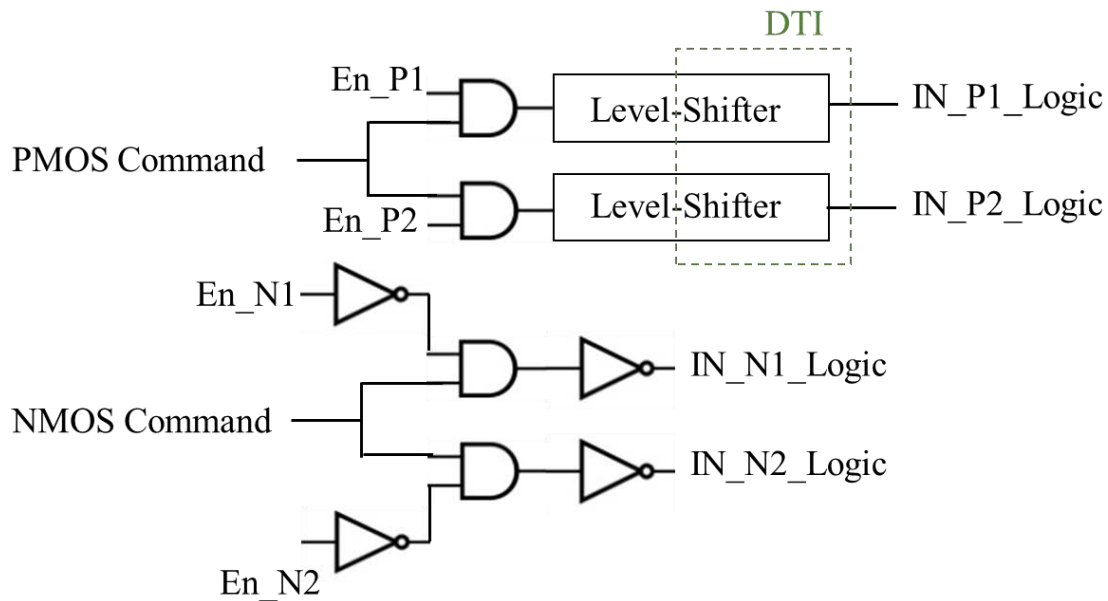
With this width values, the propagation time from IN\_N\_Logic to IN\_N is equal to  $t_{p\_L\_H}$ = 1.3ns, and from IN\_P\_Logic to IN\_P is equal to  $t_{p\_H\_L}$ = 1.7ns (with the level shifter 3ns) under 4.5V power supply, and the output buffer as a load capacitor at 27°C. And the rise/fall time of IN\_P is 520/500ps and of IN\_N is 1.45/1.4ns.

The propagation times are not final. Due to dead time management, and logic circuit the propagation time is higher. In fact, with split outputs and external gate resistance, dead-time management is not critical. But, in order to reduce short-circuit current flow existing in CMOS invertors, which is a high risk and a problematic for the output buffer with high current capacity, a delay is required between the control signals of the NMOS and PMOS. The dead-time should be calculated for the worst case, where the output buffer still sources current at  $R_{G\_Ext}$ = 0 $\Omega$ . In this case, the risk of short-circuit of the output buffer is critical. Since the buffer stage has a low  $R_{DS\_ON}$  for both PMOS and NMOS, there is a high risk of having a high short-circuit current when switching the DUT. Therefore, the PWM input is internally managed to create a dead-time and separate PMOS and NMOS control signals, as presented in Fig.II. 14. Therefore, an internal delay around 6ns is added between the PMOS and NMOS commands. After the generation of both PMOS and NMOS commands **Fig.II. 15** is presented to show the set of enables for each stage of the output pre-amp + buffer.





**Fig.II. 14.** Logic circuit including dead-time management and enable configuration.



**Fig.II. 15.** Enable configuration for each NMOS and PMOS pre-amp

Fig.II. 16 presents the chronogram between the PWM input and internal PMOS/NMOS control signals. And **Tab.II. 9** presents an overview of the enables configuration behavior. Note that for PMOS configuration the enables were set for a high voltage 5V, and NMOS enables were set for lower voltage 0V. The enable configuration for PMOS and NMOS can be further subdivided in order to have better control at the switching phase. By doing so, both surge voltage and switching loss are improved [42], [130], [131]. This separation and control of the commands converge towards segmented gate drivers [132] [133]. The dead-time between the PMOS command and NMOS command should be different, in order to compensate the level-shifter propagation time. Moreover, the critical short-circuit situation is when the PMOS is still activated and the NMOS is turning-on. As the one can see later, the mismatch between the propagations time are around 1,5ns.

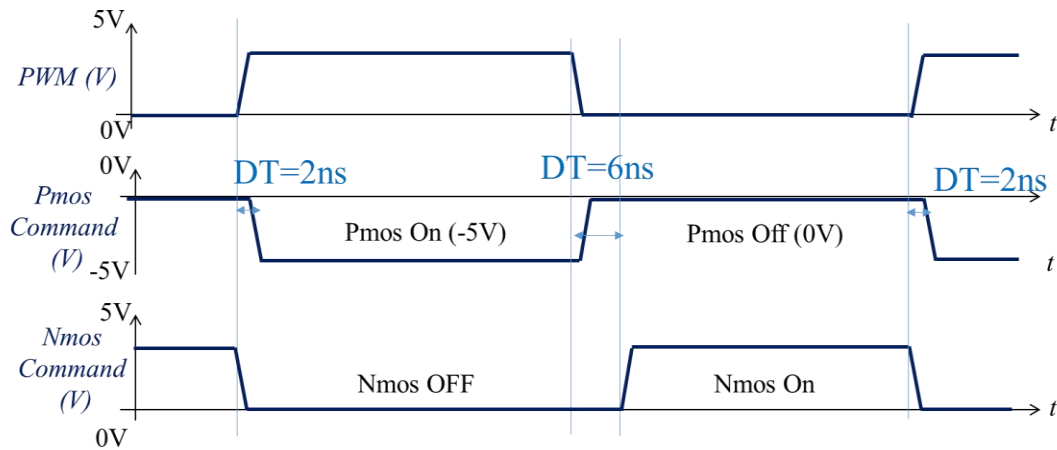


Fig.II. 16. Chronogram presenting dead-time management.

Tab.II. 9. Truth tables for both En\_P1 and En\_N

En_P1	PWM	V <sub>G</sub> PMOS1	En_N1	PWM	V <sub>G</sub> NMOS1
0	0	Off (25V)	0	0	On (5V)
0	1	Off (25V)	0	1	Off (0V)
1	0	Off (25V)	1	0	Off (0V)
1	1	On (20V)	1	1	Off (0V)

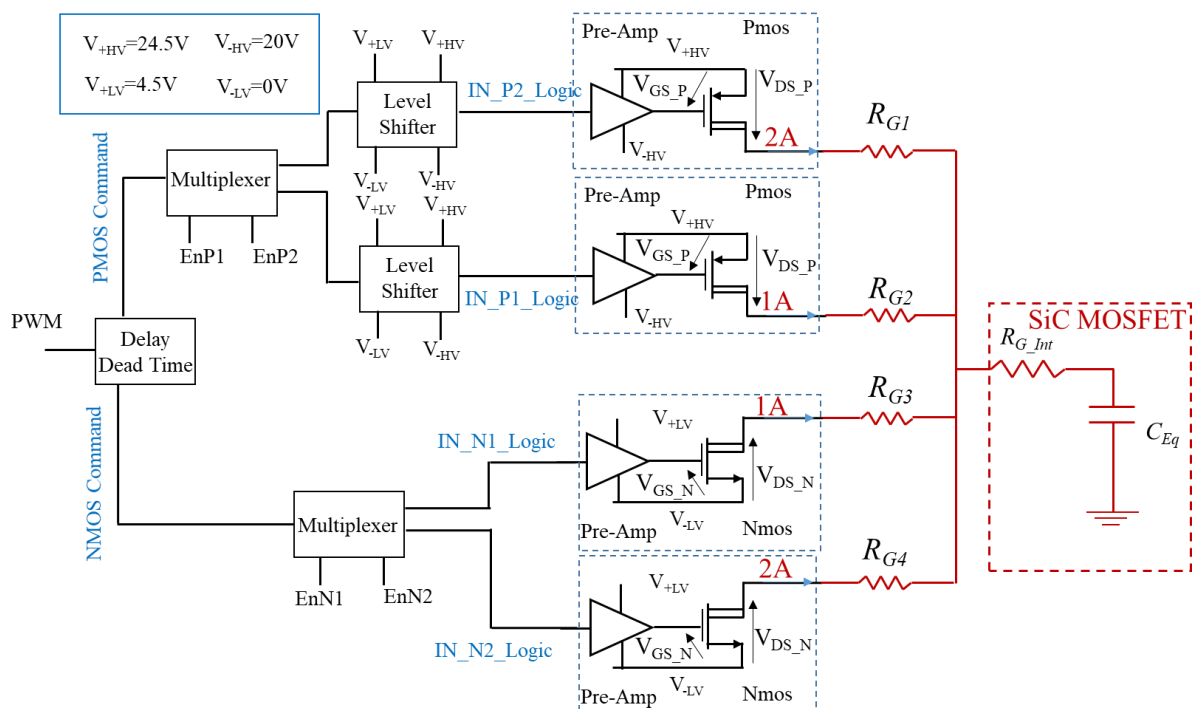
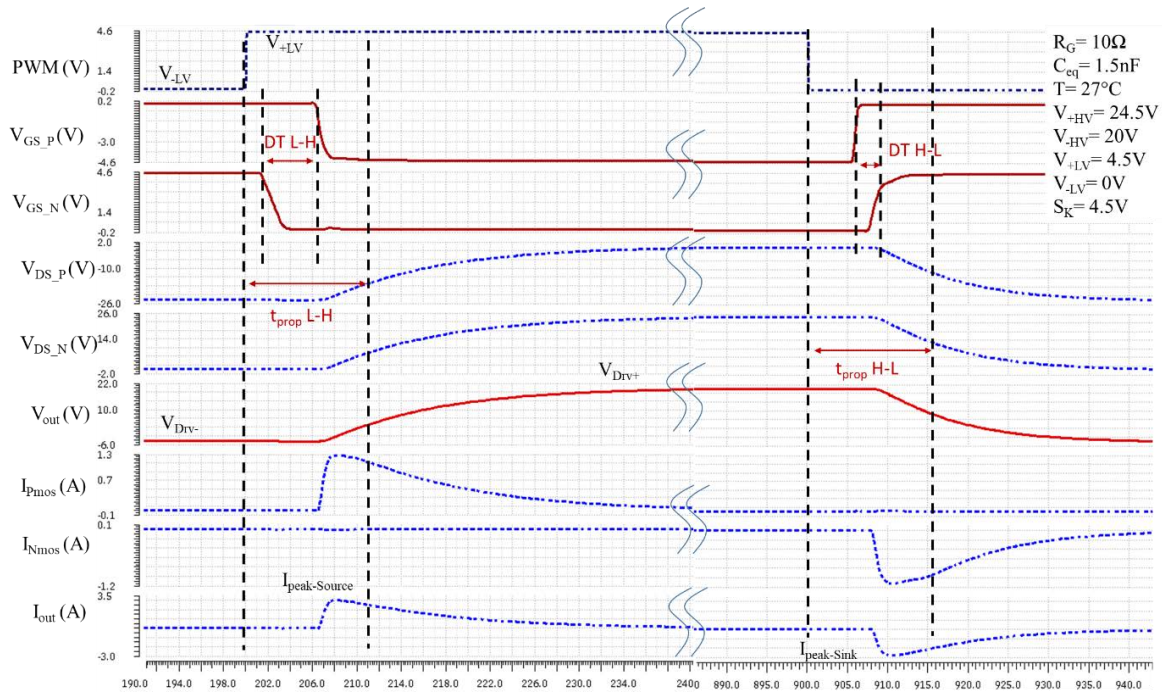


Fig.II. 17. Partial architecture of the gate driver (non-complete)

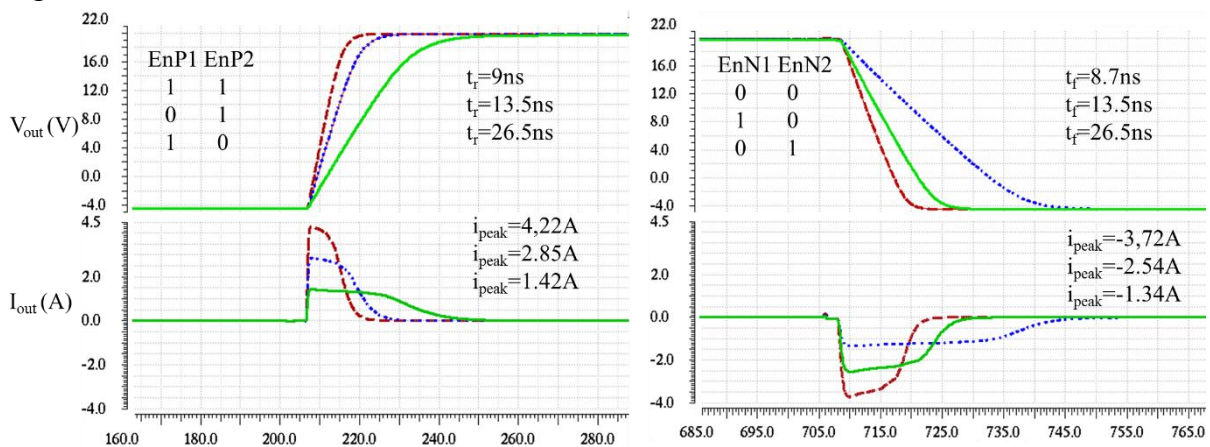




**Fig.II. 18.** Simulation waveforms of the buffer under  $R_{G\_On}=R_{G\_Off}= 10\Omega$ ,  $C_{eq}= 1.5nF$ ,  $V_{+HV}= 24.5V$ , referenced to kelvin source +5V.

In order to summarize the output buffer and its pre-amplification, Fig.II. 17, Fig.II. 18 and Tab.II. 10 are presented. The figure presents the dead-time (DT) management and  $V_{GS}$ ,  $V_{DS}$  of the PMOS and the NMOS. Tab.II. 10 presents different simulation parameters (dead-time DT, propagation time  $t_p$ , rise/fall time  $t_r/t_f$ , and mismatch ‘mis’). These parameters have been studied under different  $R_G$ ,  $C_{eq}$ , at first no charge, then  $R_G= 0\Omega$  and  $C_{eq}= 1.5nF$ , and finally  $R_{G\_ON}=R_{G\_OFF}= 10\Omega$ ,  $C_{eq}= 1.5nF$ . Note that the level-shifter is taken into consideration in this results.

Fig.II. 19 presents the output buffer under different enable configurations. The figure illustrates the peak current for each configuration, and the rise/fall time. In this case the buffer works as current source, which is the worst case to size the internal dead-time between PMOS and NMOS stages.



**Fig.II. 19.**  $V_{out}$  and  $I_{out}$  for different enable configurations,  $C_{Eq}= 1.5nF$ ,  $R_{G\_Ext}= 0\Omega$ ,  $V_{+HV}= 24.5V$

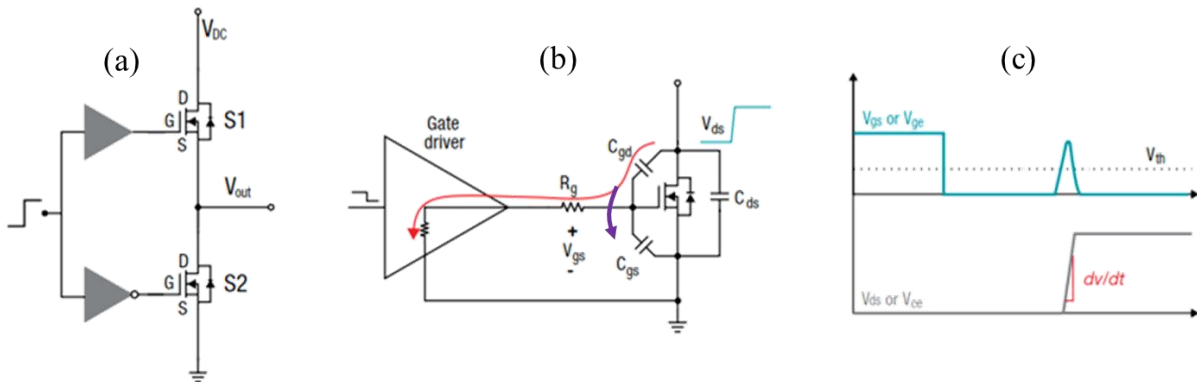
**Tab.II. 10.** Different parameters of the gate driver

$R_{G\_on}/R_{G\_off}$		$I_{peak}$ (A)	SlewRate $V_{DS}$ V/ns	$t_r, t_f$ (ns) Vds	$t_p$ (ns) Vds	Mis (ns)	$t_r/t_f$ (ns) $V_{GS}$	DT (ns)
$C_{eq}$								
Pmos	Rise	0.047	36.75	0.53	6.73	1,65	0.53	H-L
0 $\Omega$	Fall		-31.5	0.62	<i>H-LPWM</i>		1.83	1.93
Nmos	Rise	0.035	36.75	0.53	8.38	1,62	2.89	L-H
0 $\Omega$	Fall		-31.5	0.62	<i>L-HPWm</i>		1.66	3.36
Pmos	Rise	4.44	2.38	8.22	7.78	1,62	0,56	H-L
1.5nF	Fall		-2.22	8.82	<i>H-LPWM</i>		0.693	1.76
Nmos	Rise	3.74	2.38	8.22	9.40	1,62	1.41	L-H
1.5nF	Fall		-2.22	8.82	<i>L-HPWM</i>		1.69	3.38
Pmos	Rise	2.04	6.18	3.17	6.72	1.34	0.53	H-L
1.5nF	Fall		-0.60	32.5	<i>H-LPWM</i>		1.78	1.78
Nmos	Rise	1.96	0.43	45.2	8.06	1.34	2.9	L-H
1.5nF	Fall		-11.8	1.66	<i>L-HPWM</i>		1.6	3.4

#### 4.1.3. Active Miller Clamp (AMC)

On power domain, in a half bridge configuration, the collector or drain transient voltage of the power transistor can get coupled to the gate of the IGBT or SiC MOSFET through the parasitic Miller capacitance, leading to false turn-on of the transistor if no negative voltage is applied to the gate, Fig.II. 20. A Miller clamp allows sinking the Miller current across a low impedance path in this high dV/dt situation. Therefore, in many applications, the use of a negative supply voltage can be avoided. During turn-off, the gate voltage is clamped by activating different enables set of delays. In other cases, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below a typical voltage value. A Miller clamp in the gate driver allows the use of a unipolar gate drive supply instead of a bipolar gate drive supply, thus simplifying the power supply design, causing a lower size solution at a reduced cost and smaller board size. Different resistances are used at the turn-on and turn-off, as our gate driver allows it with a split output. With different resistances at the turn-on/turn-off, it ensures that the AMC resistance, when the Miller current is flowing through, is smaller. This limits any voltage glitch

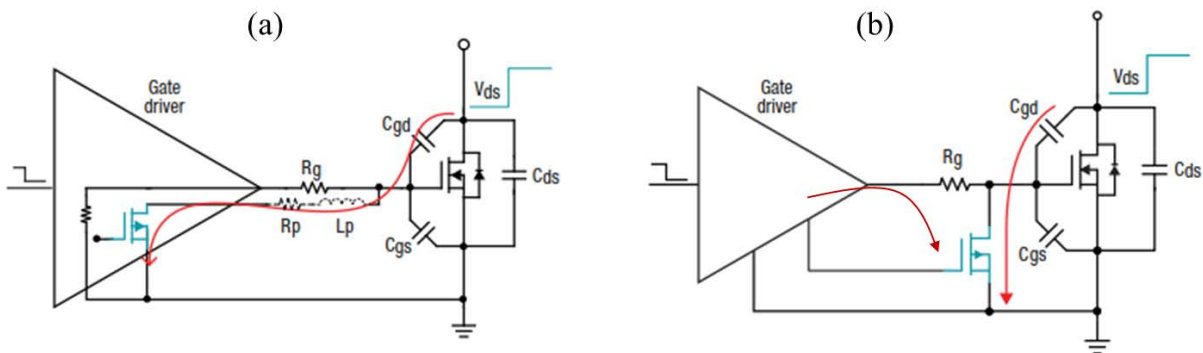
at the gate. However, the turn-off resistance should not be too small. If it is too small, it causes the transistor to turn off too quickly, resulting in too high a  $di/dt$  and EMI disturbance [64][134].



**Fig.II. 20.** (a). Half bridge configuration (b). Miller current path (c). Effect of Miller current on the gate voltage. [29]

The best way to sink the Miller current is by adding a low impedance transistor in parallel to the gate of the power transistor. For the Miller clamp to be effective, the induced current must be less than the Miller clamps current sinking capability. Eq.(II. 10) represents the induced current, with  $C_{rss}$  the reverse capacitance of the power transistor. With higher switching speed, the higher  $dv/dt$  gets, therefore the Miller current causes  $V_{GS}$  to rise above the threshold voltage, and activating the transistor.

$$i_r = C_{rss} * \frac{dV_{DS}}{dt} \quad (II. 10)$$



**Fig.II. 21.** Gate driver with (a). internal Miller Clamp (b). External Miller Clamp [29]

In our case the AMC is located inside the driver IC. With this configuration the surface required is reduced, but it is possible that parasitic resistance and inductance,  $R_P$  and  $L_P$  are added to the path of the Miller current, depending on how far the circuit is from the power switch. On the other hand, external AMC is controlled by the driver but located externally as close as possible to the gate of power device. In this way, any impedance in the current path is reduced. This implementation is best for devices with high  $dv/dt$ .

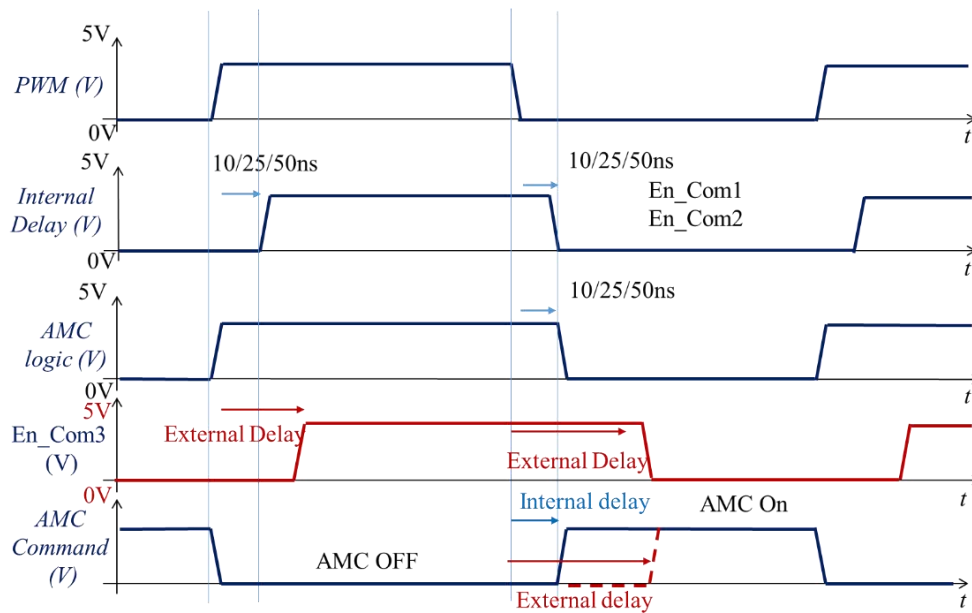
For a given transistor from Wolfspeed products, C2M0080120D, its typical threshold voltage is equal to 2.9V and its the minimum reverse capacitance is equal to 92pF. Using this value and

multiplying it by the average  $dV_{DS}/dt$  of 25V/ns, the Miller current is equal to 2.3A. Moreover, the AMC transistor should sink 2.3A and respect this inequality  $(V_{th}/R_{G\_int}+R_{AMC}) > i_r$ . Therefore, low impedance is required, so we have decided to take the same size of the NMOS output buffer transistor ( $R_{DS\_ON}= 1.5\Omega$ ) with the same pre-amplification blocks.

As mentioned, the AMC is activated by a set of delays instead of monitoring  $V_{GS}$ . Two delay settings have been configured, internal and external. The internal delay is configured by a multiplexer that allows four states, off, 10ns delay, 25ns delay and 50ns delay, configured by two enables  $En\_Com1$  and  $En\_Com2$ . The external delay setting, is a more flexible solution to set a different desired delay. In order to do so, the delay signal is a delay added to the PWM signal, that can be easily controlled by an external source, (FPGA, or an RC circuit) by the third pad,  $En\_Com3$ , Tab.II. 11. (\*) Note: that X is the external delay time. Then, internally the signal is adapted in order to have the delays only effective at the turn-off and does not affect the turn-on for both external and internal delays set, Fig.II. 22. Note: In order to activate the external delay, one of the internal enables ( $En\_Com1$  or  $En\_Com2$ ) should be activated, as an enable. The better choice is to activate the smaller delay to have more flexibility above 10ns, as presented in the tab.II.10.

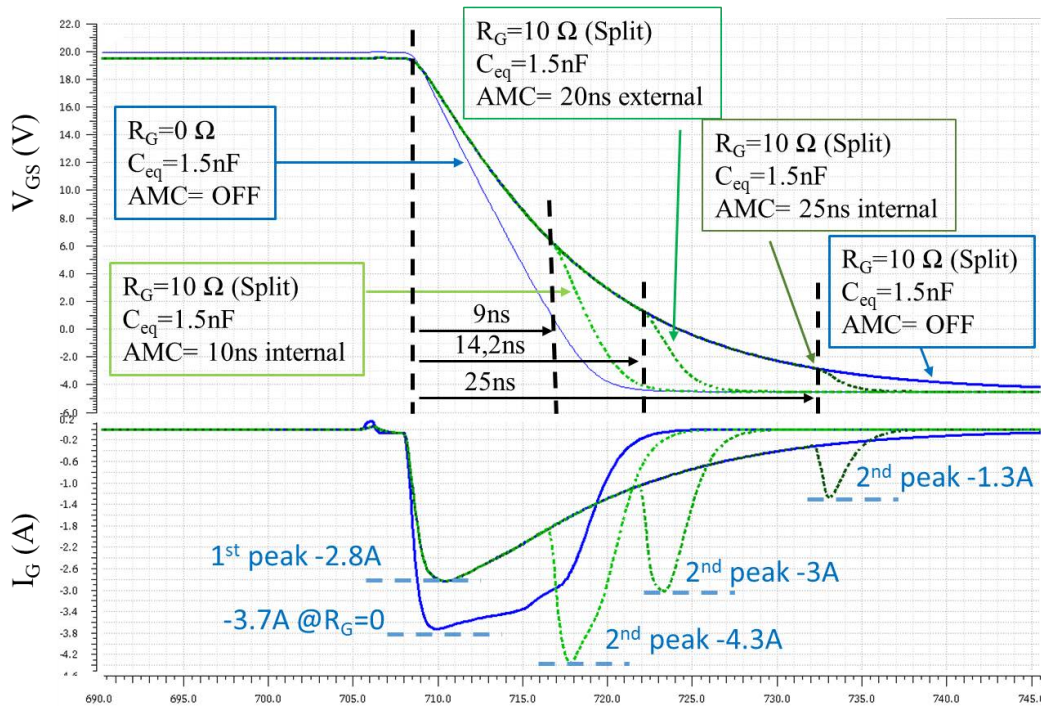
**Tab.II. 11.** Delay configuration of the AMC, Note: X\* is the external delay

En_Com3	En_Com2	En_Com1	Output_Delay
0	0	0	No delay
0	0	1	10 ns
0	1	0	25 ns
0	1	1	50 ns
1 (X* ns)	0	1	X* ns



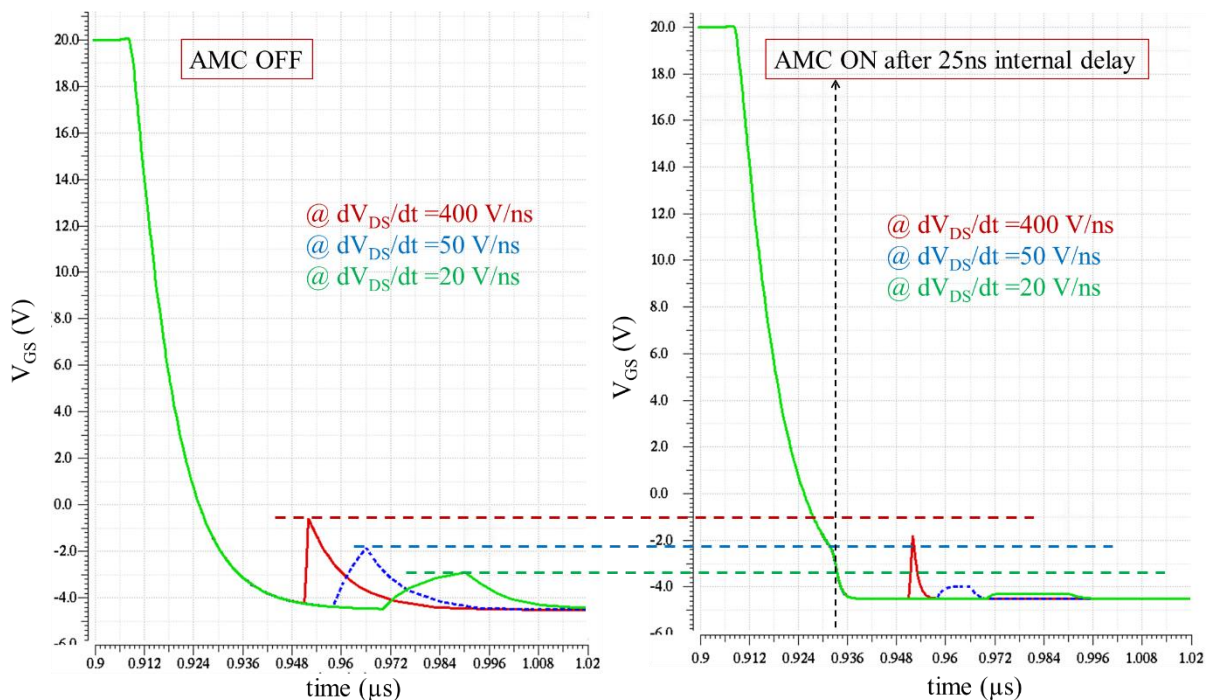
**Fig.II. 22.** Qualitative chronogram of the AMC internal and external delay settings





**Fig.II. 23.** Simulation results of the gate voltage and current under different AMC activation delays

Fig.II. 23 illustrates the simulation behavior of the gate-source voltage and current under different configuration delay, (internally 10ns and 25ns, externally 20ns). As a reference, the signals are simulated without delay under  $R_G=0\Omega$ ,  $C_{eq}=1.5\text{ns}$  and  $R_G=10\Omega$  (split output),  $C_{eq}=1.5\text{ns}$ . The response time illustrated in Fig.II. 23 presents the configurable delay. The internal delays are nearly respected and on the other hand, the external delay is compensated by skipping the propagation time of the multiplexer and logic circuit.



**Fig.II. 24.** dV/dt immunity: AMC effect under Miller effect for different dV/dt

4.1.4. High impedance and Soft shut down

Different solutions are proposed in the literature to protect and turn-off safely the power device, once a short circuit has been detected [135] [70] [71] [28]. The technology implemented for Si IGBT components cannot be directly applied to the SiC MOSFET gate drivers [136]. The protection function, on its own is mandatory, where it can be used for several monitoring functions (temperature monitoring, short-circuit monitoring, ...). In our case the protection function is used with the short-circuit detection function. The short-circuit detection functions are developed in depth in chap.III. In this section, the behavior and the design of this function in the gate driver is developed, adapted for short-circuit operation. Because under short-circuit the SiC drain current increases rapidly, in the range of several kilo-amperes per microsecond. For example, when a short-circuit is detected at an inverter leg, it is imperative to turn-off quickly and with a controlled di / dt. Moreover, because of the various parasitic inductances distributed within the switching cell, turning-off the power component with a high di/dt causes a high over-voltage ( $V = L di/dt$ ). In such a condition, the normal blocking of the power component, through its  $R_{G\_off}$  gate resistor, should be avoided. Moreover, SiC MOSFET withstand time is very short under short-circuit, therefore turning-off the power device must be executed as soon as possible. The most adequate and adapted solution goes by the name of SSD, soft shut down. In order to softly turn off the power SiC MOSFET in the case of short circuit event, a driving transistor with a high impedance or a high resistor in series with the resistance is required. Thanks to the  $R_{SSD}$  resistor in the gate charge method [Chap.3] or the small resistor (high-impedance) which is implemented in the ASIC, any overvoltage phenomenon that could destroy the power device is prevented.

The  $R_{DS\_ON}$  of the integrated SSD is around 100 ohms, assuring a soft shut down (small size transistor within the IC  $W/L= 320\mu m/0.4\mu m$ ). The SSD circuit is not internally connected to the segmented buffer, for the purpose to validate it separately and to connect it at our convenience. Therefore, two inputs are required for this circuit, the  $En\_SSD$  in order to enable and disable the circuit once connected externally, and  $SSD\_In$  which is the input to receive the output detection flag (the external connection).  $SSD\_In$  is an external pad for two main reasons. First in order to command the SSD using the FPGA to validate the function, Fig.II. 25. And second, in order to be able to use this function and the gate driver for different external detection circuits. The HZ and SSD function have been chosen to be activated when a logic ‘0’ (0V) is sent.

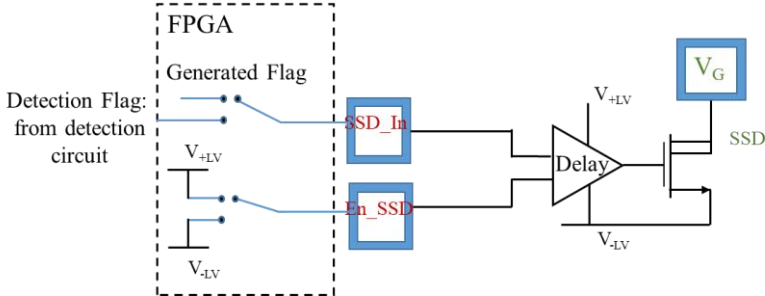
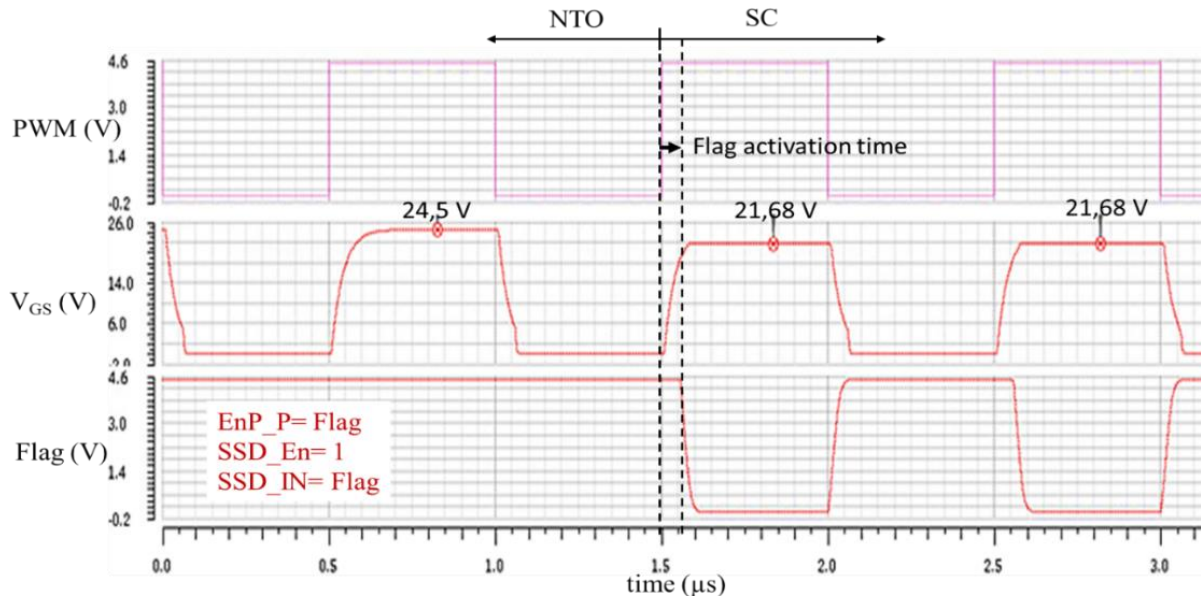


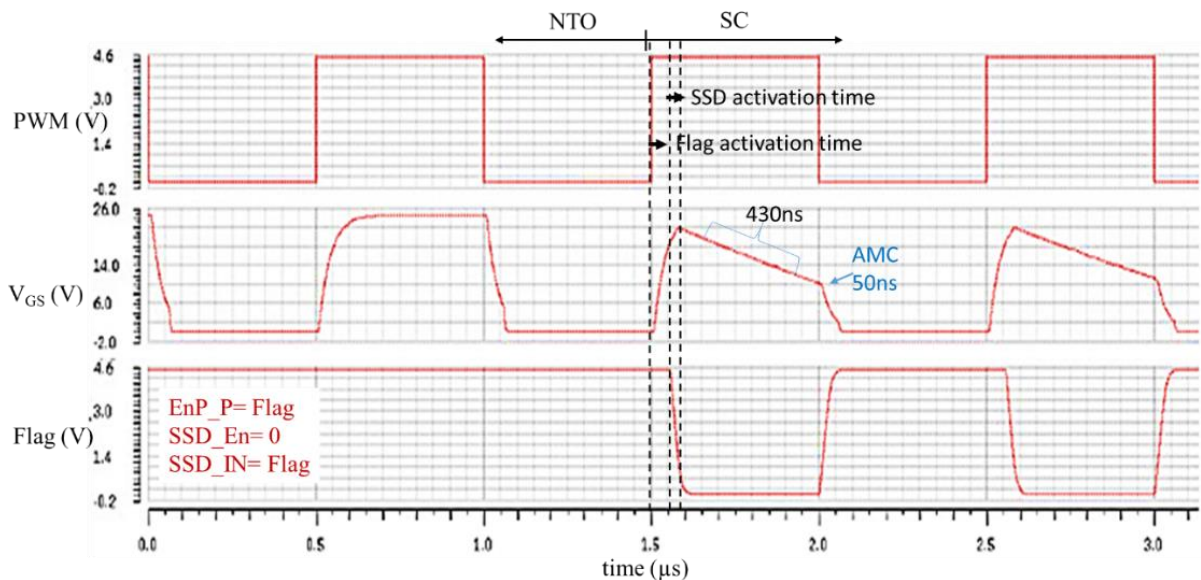
Fig.II. 25. Soft shut down circuit with both inputs connected to an FPGA

**Tab.II. 12.** Configuration of HZ and SSD

En_HZ	En_P1/P2	PWM	V <sub>G</sub>	SSD_IN	En_SSD	V <sub>G</sub>
1	X	X	X	Flag	1	SSD 'Off'
0	X	X	0	Flag	0	SSD 'On'
Flag	X	X	HZ 'ON'			



**Fig.II. 26.** Simulation waveforms of the AGD under HZ, SSD is OFF



**Fig.II. 27.** Simulation waveforms of the AGD under HZ and SSD is ON

The SSD is not directly activated after the SC is detected. Once the SC has been detected, the segmented buffer goes to a high impedance state HZ first, where the gate of the power device becomes floating (PMOS and NMOS in output buffer are in OFF state). This additional state is typically not available in standard output buffers and gate drivers. However, it is required to





Adaptation can still be added to the design kit depending on the requirements. Each layer has its own parasitic resistance and capacitance value. A trade-off between the total surface of the metal used and the parasitic added need to be found. Therefore, the layout was carefully designed.

Afterwards, first and foremost, the layout should satisfy other requirements, set by the performance of the schematic. Those requirements are straightforward to the electrical circuit, and non-checked by the manufacturer or Cadence tools.

In our design, large width transistors have been used. Therefore, the transistors are divided in multiple transistors (\*m) and each transistor has a significant number of fingers. Several fingers (several stripes: SS) provide more flexibility in layout planning, which allows making the layout more square-shaped. SS-layout allows better matching of transistors, and a better distribution of the gate and drain currents. Using SS reduces gate resistance and reduces the current density. Moreover, for large transistors the gate-channel capacitance forms a low-pass with the gate resistance and switching speed is reduced. In addition, the drain area is reduced because two or several fingers share a common drain and therefore parasitic are reduces as well. In order to have a better distribution of the gate current, and not affect the switching speed, gates are often contacted at both ends to reduce the effective resistance.

The gate terminal is made of polysilicon, which is relatively very resistive. For large transistors the apparent resistance between the gate contacts (at the center) is high, which would cancel the gate bias at the center, if not a wide range in the center. To overcome the problem, each large transistor is divided in several fingers, which reduces the voltage drop in the middle by  $n^2$ , Fig.II. 29, eq.(II. 11) for single finger and eq.(II. 12) for several fingers. Moreover, recommended ratios by XFAB datasheet were used in order to design the output buffer, Tab.II. 13.

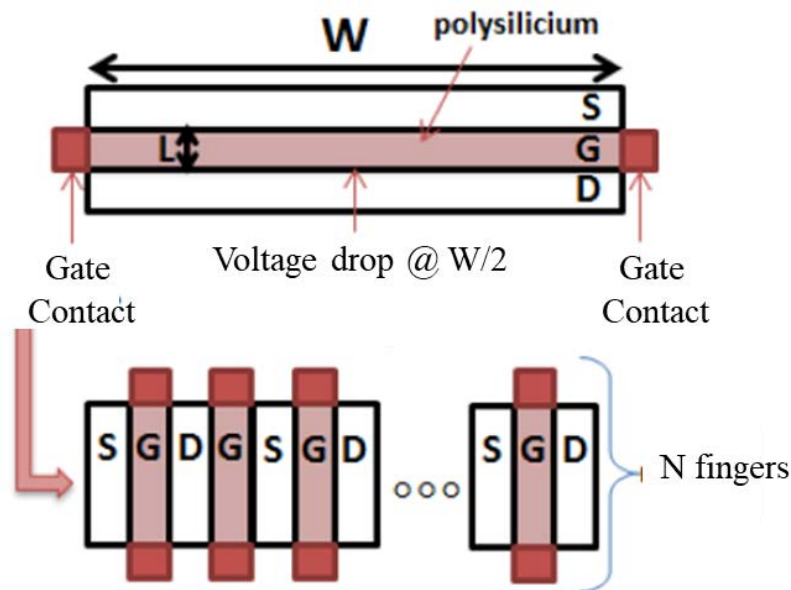


Fig.II. 29. Different set of the layout for a single finger and multiple fingers

$$\Delta V_{W/2} \approx \frac{15 * W(\mu m)}{4} * i_G \quad (II. 11)$$

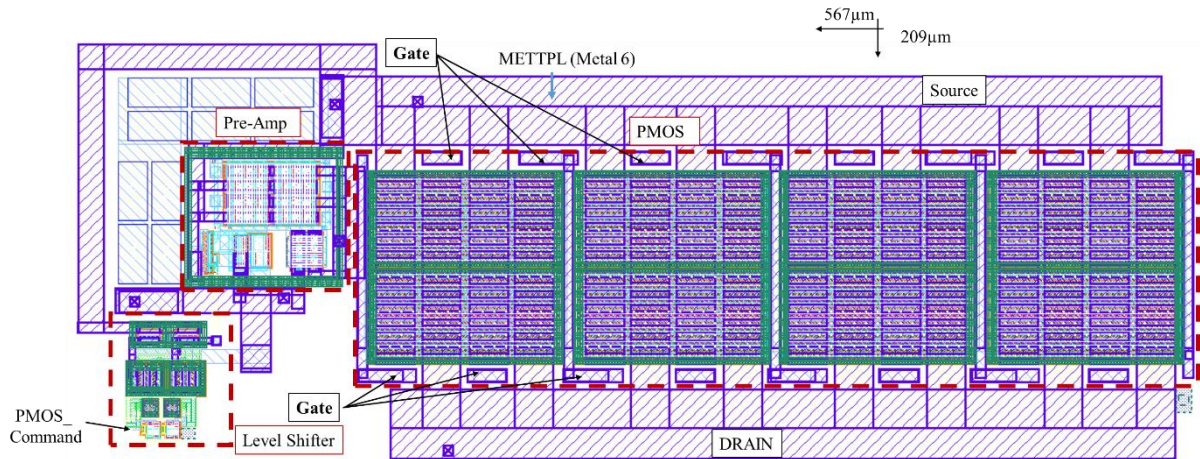
$$\Delta V_{W/2} \approx \frac{15 * W(\mu m)}{4 * n^2} * i_G \quad (II. 12)$$

**Tab.II. 13.** Finger and multiplier numbers for each function. (Note the blocks name refers to Fig.II. 28)

Functions	Blocks	# Fingers	W <sub>finger</sub>	W <sub>tot</sub>	# Multipliers	W <sub>Final</sub>
<b>Phvta</b>	PMOS1	12	90μm	1.08mm	8	8.64mm
	PMOS2	12	90μm	1.08mm	16	17.28mm
<b>Nhvta</b>	NMOS1	12	90μm	1.08mm	4	4.32mm
	NMOS2	12	90μm	1.08mm	8	8.64mm
<b>Nhvta</b>	AMC	12	90μm	1.08μm	12	12.96mm

In order to connect these fingers (drain together, gate together and source together), the metal with the lowest sheet resistance  $R_{\square}$  is favorable. Moreover, a trade-off should be set between the surface used and the parasitic resistance and capacitance added, [137]. Therefore, conductive metal 6 (METTPL, metal top thick layer) and metal 5 (METTP, metal top) are mostly used. The drop voltage across a metal wire can be expressed by eq.(II. 13) [138], where L and W are respectively the length and the width of the wire. Fig.II. 30 presents the layout of one PMOS chain (PMOS output transistors, Pre-amp and level shifter).

$$V_{Drop} = R_{\square} * \frac{L}{W} * i \quad (II. 13)$$



**Fig.II. 30.** Layout of one PMOS chain (level shifter + pre-amp + output buffer)

The layout of the whole circuit is carefully done, decoupling capacitors were added between  $V_{-HV\_V-LV}$  and  $V_{+HV\_V-HV}$ , as Fig.II. 28 illustrates. Moreover, ESD pads (Electro-Static Discharge); type HVP2J2PM; are used for each input pads used for configuration (5V inputs), and normal pads for most outputs. The HVP2J2PM are latch-up robust HV supply/IO ESD protection circuit for 13V maximum operating voltage and 2kV HBM ESD robustness. The 5V ESD pads are proposed by the technology library, which is composed with a multi-layer

pad and a diode-connected MOS transistor (5V, pe5), Fig.II. 31. The diode connected transistor has a W equal to 20 $\mu\text{m}$  multiplied by 40, which is equivalent to a large parasitic capacitor (confidential X-Fab data), so it is important to ensure that sufficient current is supplied for a fast configuration. Therefore, buffers should be added at the inputs of the ASIC. Moreover, protection diodes called dpp6 in the design kit, which are 6V Zener diodes, will clamp undesired ESD and overcome antenna problems. The layout size of each main block is given in Tab.II. 14. The view of the whole layout under Cadence is presented in Fig.II. 32 (a).

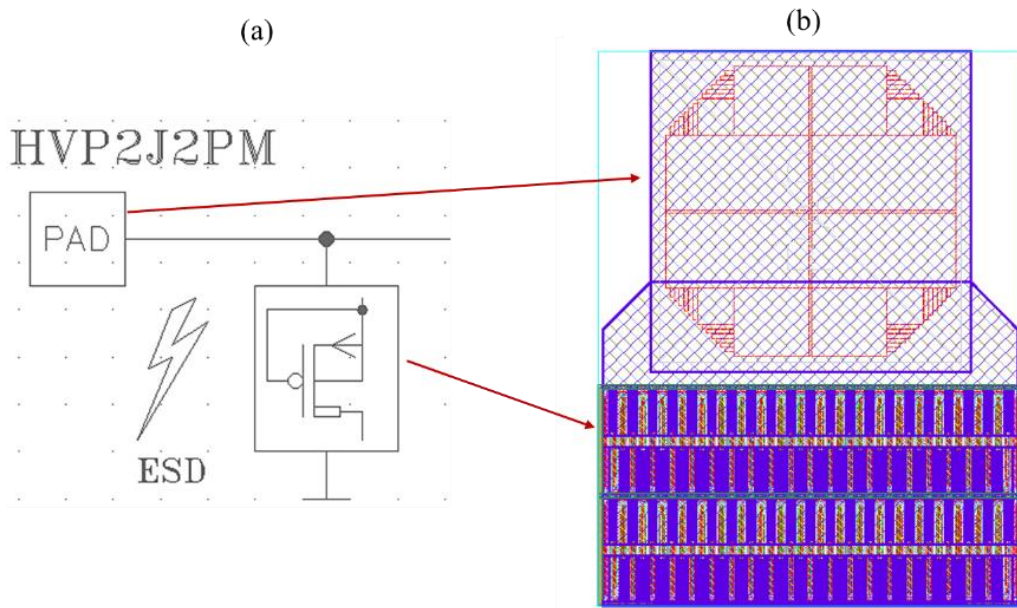


Fig.II. 31. (a). ESD pad equivalent schematic (b). layout view.

Tab.II. 14. Layout size for the ADG

Function	Layout Size	Multipliers
<b>Logic circuit</b>	41 $\mu\text{m}$ *59 $\mu\text{m}$	-
<b>PMOS chain</b> (HS output)	568 $\mu\text{m}$ *209 $\mu\text{m}$	*3 (2Parallel +1Parallel)
<b>NMOS chain</b> (LS output)	216 $\mu\text{m}$ *260 $\mu\text{m}$	*3 (2Parallel +1Parallel)
<b>AMC chain</b>	216 $\mu\text{m}$ *260 $\mu\text{m}$	*3 (3Parallel)
<b>5V capacitor</b>	503 $\mu\text{m}$ *490 $\mu\text{m}$	-
<b>40V capacitor</b>	377 $\mu\text{m}$ *565 $\mu\text{m}$	-
<b>Detection circuits</b>	620 $\mu\text{m}$ *150 $\mu\text{m}$	*2 (approaches including 3 variants)
<b>Protection (SSD)</b>	80 $\mu\text{m}$ *30 $\mu\text{m}$	-
<b>ESD-PADS</b>	121 $\mu\text{m}$ *92 $\mu\text{m}$	*15 (active area 66 $\mu\text{m}$ *66 $\mu\text{m}$ )
<b>PADS</b>	76 $\mu\text{m}$ *76 $\mu\text{m}$	*19 (active area 66 $\mu\text{m}$ *66 $\mu\text{m}$ )
<b>Total</b>	2414 $\mu\text{m}$ *1559 $\mu\text{m}$	-



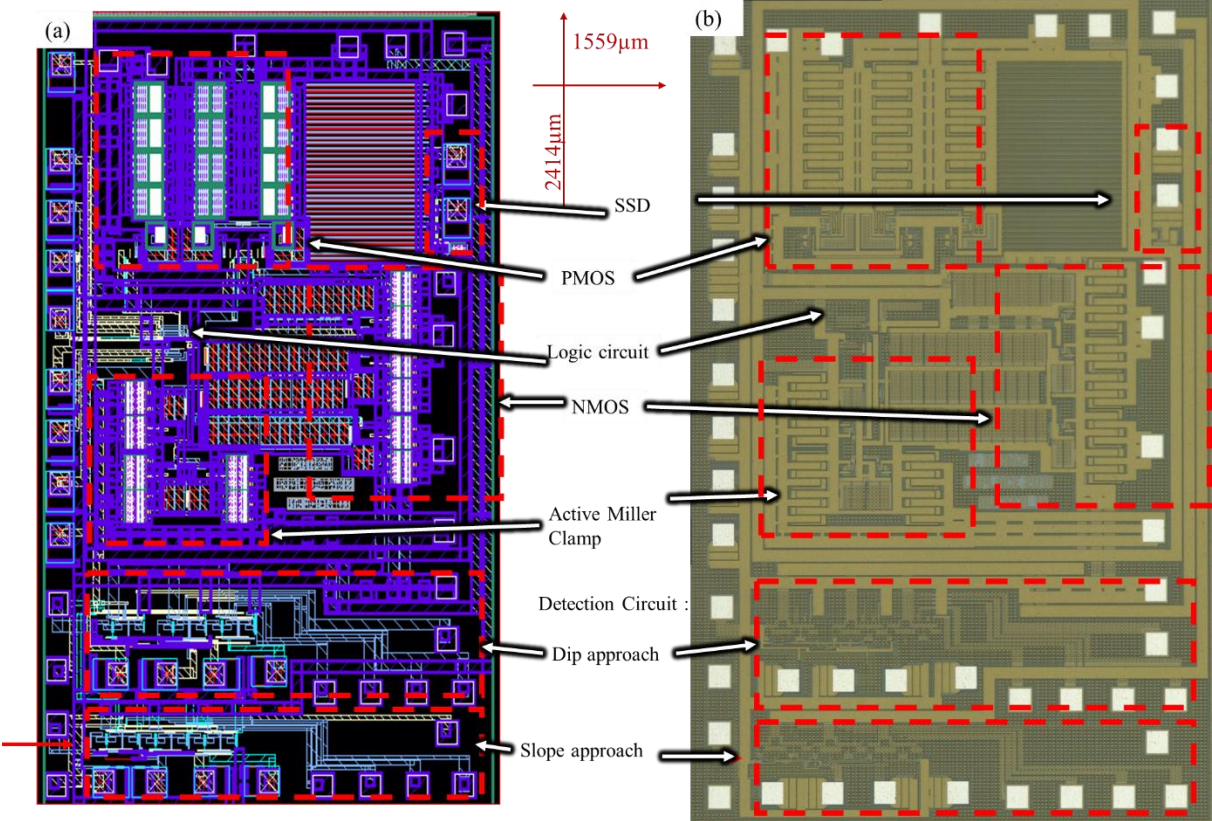


Fig.II. 32.(a). Layout view under cadence, (b). microscopic view of the fabricated chip

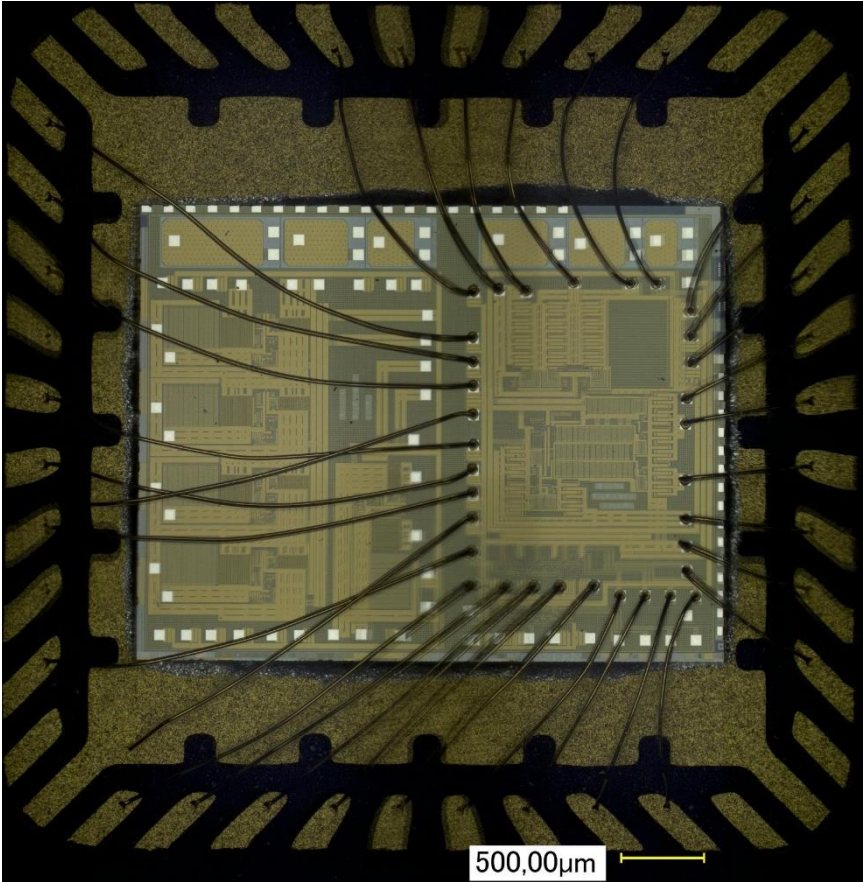
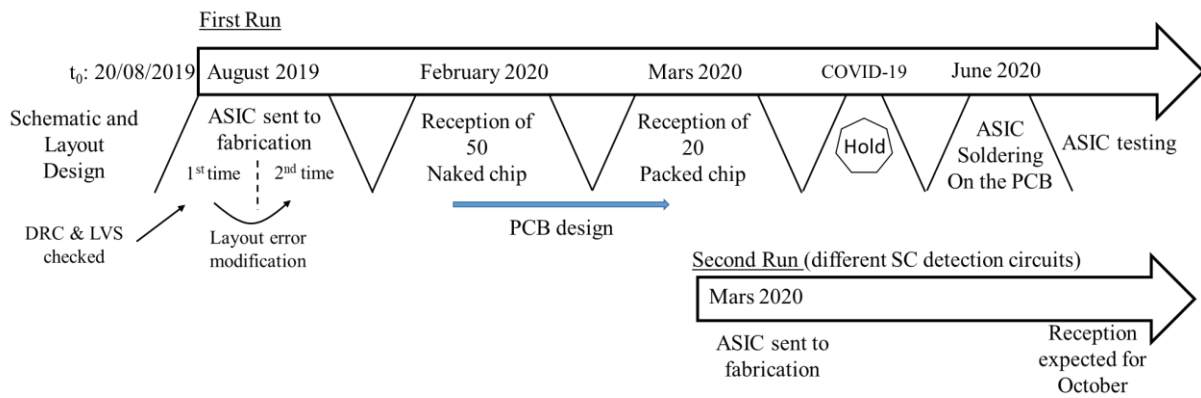


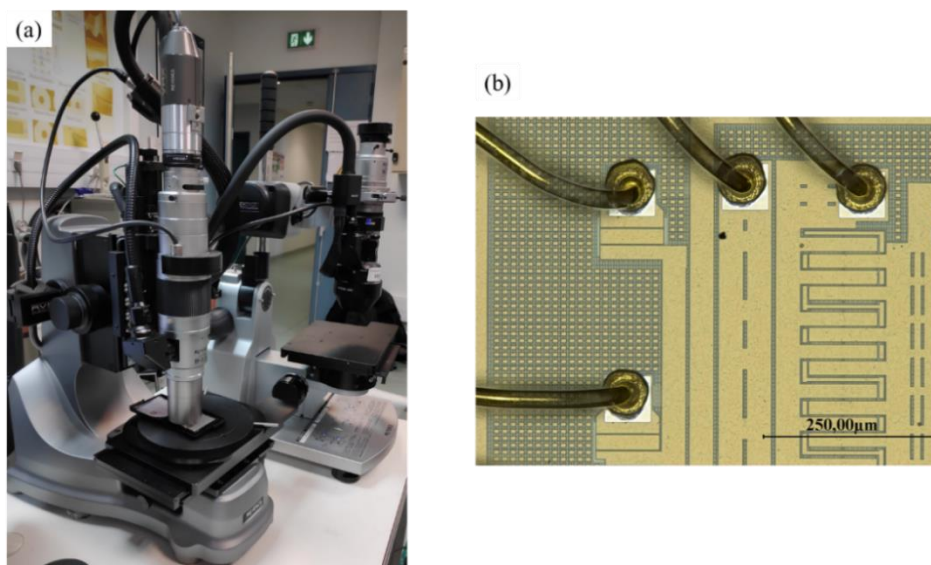
Fig.II. 33. Packaged ASIC on the QFN 40 6mm\*6mm, with the AGD connected, (failed prototype)



**Fig.II. 34.** Time chart of the ASIC

After DRC and LVS check, the layout was sent to fabrication through Europractice-IC. After few months of patience, the bun is out of the oven, and the ASIC is ready for packaging, Fig.II. 34 . Fig.II. 32. (b) Fig.II. 33 presents the microscopic view of the AGD. The chip is afterwards packed in a QFN40 6mmX6mm, as illustrated in Fig.II. 33. The package is chosen regarding the number of mandatory pads (34), as well as to reduce chips with different bonding. The packaging was subcontracted to IMEC [139] via Europractice-IC service, where the CMOS IC were glued in the cavity, and gold bonding wires were used. Ten CMOS dies have been initially packaged and received in the beginning of Mars 2020, Fig.II. 34. The figure is illustrated using Keyence Vhx-1000 digital microscope, Fig.II. 35.(a), high resolution can be reached with this microscope, a zoom on the pads is illustrated in Fig.II. 35.(b). Note the fabrication run included three main works:

- The AGD (active gate driver), on the right side of the chip
- the MMAGD (multilevel modular active gate driver) presented in section 5, on the left side of the chip
- HV breakdown capacitors.



**Fig.II. 35.(a).** Keyence Vhx-1000 digital microscope **(b).** zoom on the pads with the gold bonding wire



#### 4.4. Characterization and experimental validation of the gate driver

The CMOS ASIC is experimentally validated in two steps, first using a fixed load capacitor, V.0.A, and second using SiC MOSFET power transistor using the second version of the power bench, V.2.A. V0 stands for initial prototype, and V2 for the second power bench. And, the A stand for the first PCB prototype.

##### 4.4.1. V0.A under a load capacitor with no power

A dedicated PCB is realized in order to host the ASIC and to allow further dynamic characterization. The PCB is realized with 4 layers, and has an area of 6cm by 6cm, Fig.II. 36. All the enables and delay control are driven by an external FPGA. The PCB is divided in two main parts:

- External functions: The FPGA connectors and the power supplies inputs.
- On board functions: which includes the gate resistors, test points, straps and jumpers, and potentiometers for the detection function.

Test points are limited in the PCB. In order to reduce parasitic paths and to get the gate driver as much as possible closer to the power transistor, only the gate-source voltage and the PWM input are accessible, apart from the detection functions, Fig.II. 37. Fig.II. 38 presents as well the physical placement of the chip, which is done within the lab. A specific process for the soldering the ASIC is done specifically for our chip by 3DPhi.

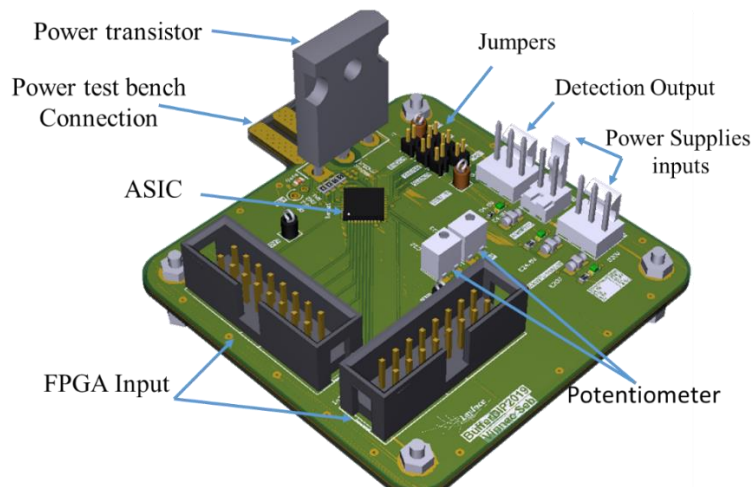


Fig.II. 36. 3D view of the PCB

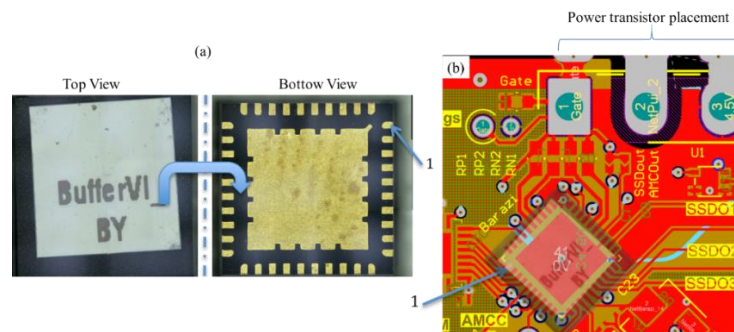


Fig.II. 37. (a). AGD in package (b). placement of the AGD on the PCB

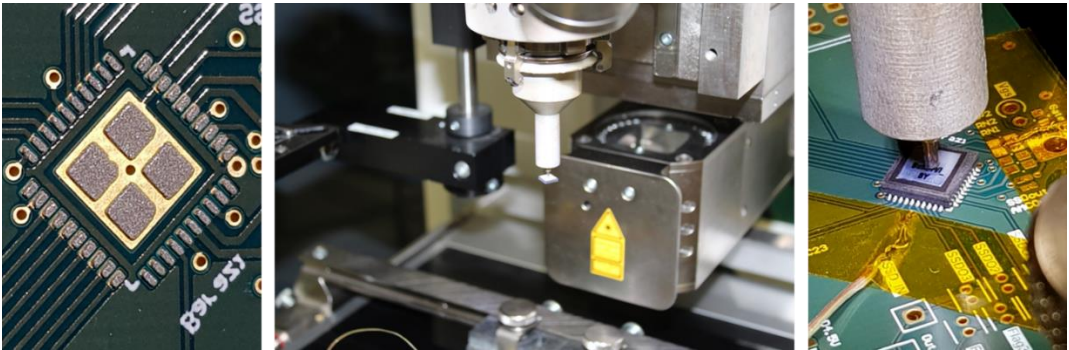


Fig.II. 38. Physical placement of the ASIC on the PCB (by 3DPhi)

Fig.II. 39 shows the platform of the test. A Gate resistor equal to 10Ω is soldered at each output of the output buffer (PMOS1, PMOS2, NMOS1 and NMOS2), and an equivalent capacitor of 1.5nF is soldered instead of the power transistor for a first ASIC characterization. Two Keithley 2612 are used to supply the PCB, each Keithley has two isolated power supplies, the order of the connectivity with PCB is presented in Fig.II. 40. A look at the touch screen in Fig.II. 41 is presented along with the PCB, the touch screen allows easy configuration of the desired enables set, as well as to send the PWM signal. The enable set can be high or low logic commands or even generated signal by the FPGA. The PWM signal can be configured into an infinite pulses or into double pulse or into a single pulse. The single pulse and double pulse are mainly used in order to confirm the correct functionality of the ASIC and reducing the stress upon it, especially under SC. The touch screen is directly connected to the FPGA ‘dev de0 nano’ (operational under 5V) which is in turn connected to the board to send the required data.

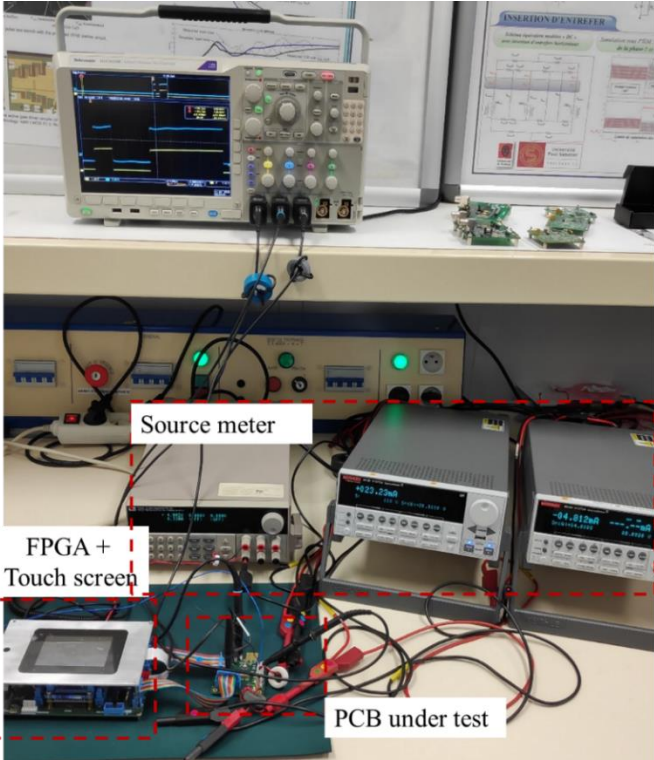
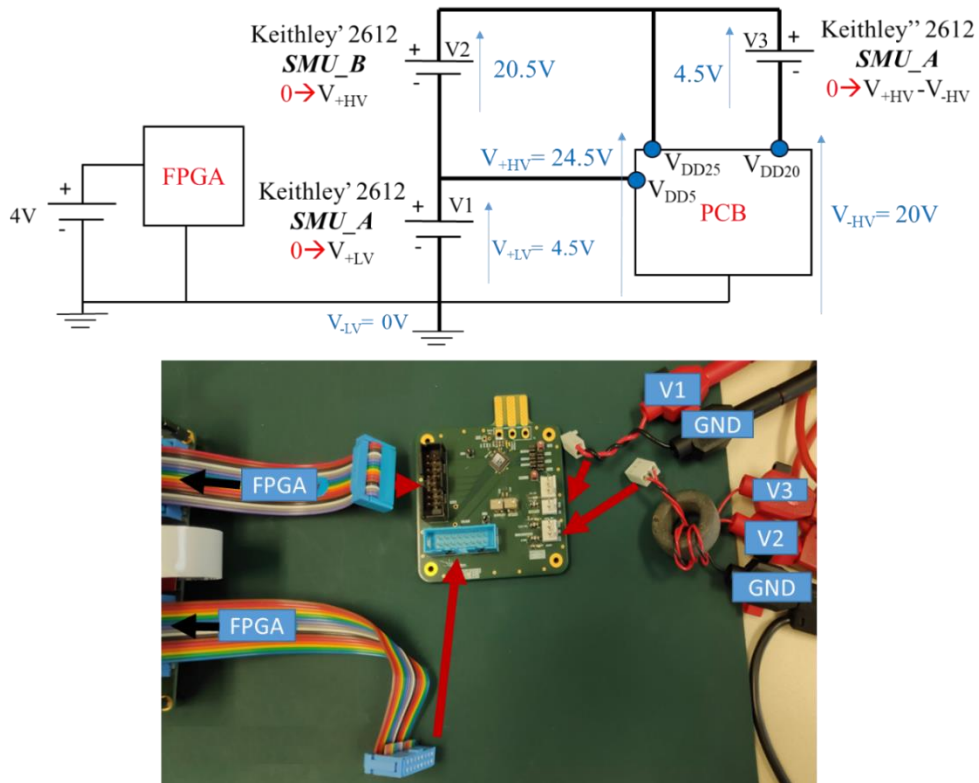


Fig.II. 39. Test bench V0.A



**Fig.II. 40.** PCB Power sources connectivity

The FPGA facilitates the interaction between the desired commands and the ASIC. Moreover, the ASIC has numerous I/O, therefore the FPGA use can be mandatory. The interface and the program were developed by technical support at the lab level (By Sebastien Vinnac). A preliminary characterization of the FPGA has been done, to validate the different I/O configurations (PWM, enable and configuration pins, min/max voltages ...). Following this preliminary setup, the PCB with the CMOS ASIC has been connected to the FPGA board. All the tests are done using probes with adapted specifications (3.9pF, 10M $\Omega$ , 1GHz, 300V), and a Tektronix oscilloscope 1GHz. First the main function; the buffer; has been tested under typical configuration, Tab.II. 15. Step-by-step the voltage ( $V_{DD25} = V_{+HV}$ ) is increased in order to reach the typical operational point, as Fig.II. 42 shows. Moreover, Tab.II. 16 presents all main parameters of the waveforms, (current consumption by the source meter, propagation time and rise/fall time). Note that only one PCB is validated in this process. Therefore, values may change for different PCBs.

**Tab.II. 15.** Typical configuration of the ASIC commands

Commands	Configurations	Function
PMOS1 / PMOS2	1 / 1	Full current source
NMOS1 / NMOS2	0 / 0	Full current sink
En_HZ	1	HZ OFF
En_Com1 / En_Com2 / En_Com3	0 / 0 / 0ns	AMC OFF
En_SSD / SSD_In	1 / 1	SSD OFF



Fig.II. 41. Touch screen with different parameters configuration and the PCB

Tab.II. 16. Summary of measured propagation delays and rise/fall time between PWM and  $V_{GS}$

$V_1 / V_2 / V_3$ (V)	Current consumption (mA)	$t_{pL-H} / t_{pH-L}$	$t_{pL-H} / t_{pH-L}$	$t_r / t_f (V_{GS})$
		@10% / 90% (ns)	@50% (ns)	@10%=>90% (ns)
4 / 4 / 4	15.37 / 2.04 / -0.39	19 / 17	27 / 29,5	39,8 / 47
4 / 8 / 4	17.4 / 4.04 / -1.49	19 / 17,8	28,4 / 31	37 / 45
4 / 12 / 4	19.4 / 6.07 / -2,59	19.5 / 18	29,2 / 33	31,4 / 45
4 / 16 / 4	21.4 / 8,11 / -3.70	19 / 20	30 / 35,5	32 / 43
4 / 20 / 4	23.5 / 10.1 / -4.81	19 / 20,3	30,7 / 38,3	32 / 43

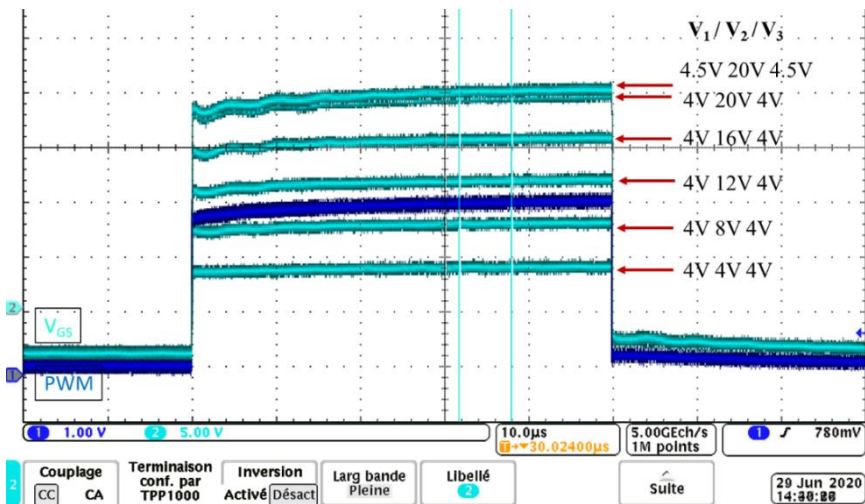
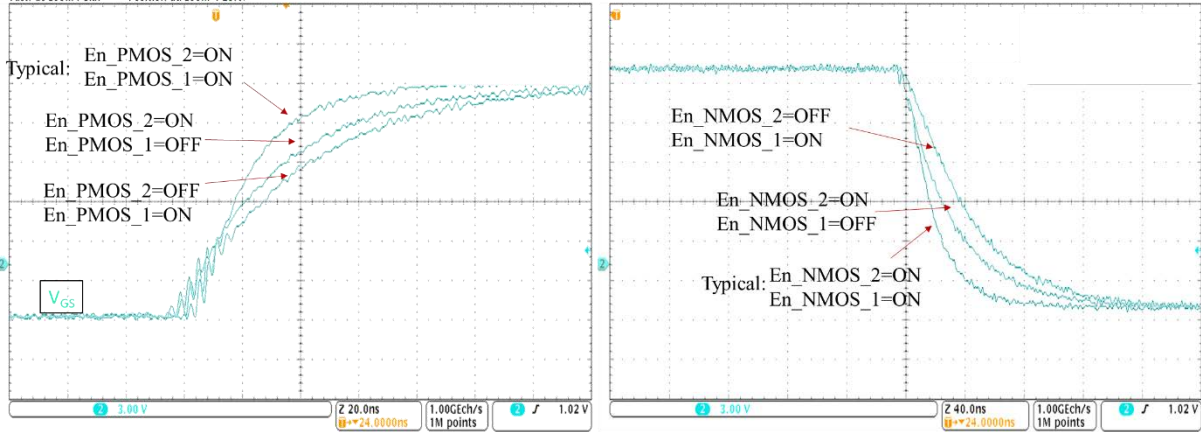


Fig.II. 42.  $V_{GS}$  for different power supplies

After validating and ensuring the correct behavior of the main functions under typical configuration, a validation of the other functions has been carried out, starting by the segmented configuration. A typical configuration is when the PMOS enables are both ON ('1') and the NMOS enables are both ON ('0'). As Fig.II. 43 shows  $V_{GS}$  under different enables configuration, which ensure a well-functionality of the segmented function. Tab.II. 17 and



Tab.II. 18 presents  $V_{GS}$  parameters for different power supplies ( $V_{DRV} = V_{+HV} + V_{+LV} = 20V$  and  $= 24V$ ) and respectively for different PMOS and NMOS enable configurations.



**Fig.II. 43.**  $V_{GS}$  under different NMOS and PMOS configurations @  $V_{HV+} = 16V$  and each  $R_{G\_Ext} = 10\Omega$ ,  $C_{Eq} = 1.5nF$

**Tab.II. 17.** Measured propagation delays and rise/fall time between PWM and  $V_{GS}$  for different power supplies and different PMOS enable configurations

En_Configuration PMOS1 / PMOS2	$V_1 / V_2 / V_3$ (V)	$t_{pL-H}$	$t_{pL-H}$	$t_r$
		@10% (ns)	@50% (ns)	@10%=>90% (ns)
'1' '1'	4 / 16 / 4	19	30	32
'0' '1'	4 / 16 / 4	23	40	76
'1' '0'	4 / 16 / 4	23	46	90
'1' '1'	4 / 20 / 4	19	30	32
'0' '1'	4 / 20 / 4	20	40	68
'1' '0'	4 / 20 / 4	22	62	90

**Tab.II. 18.** Measured propagation delays and rise/fall time between PWM and  $V_{GS}$  for different power supplies and different NMOS enable configurations

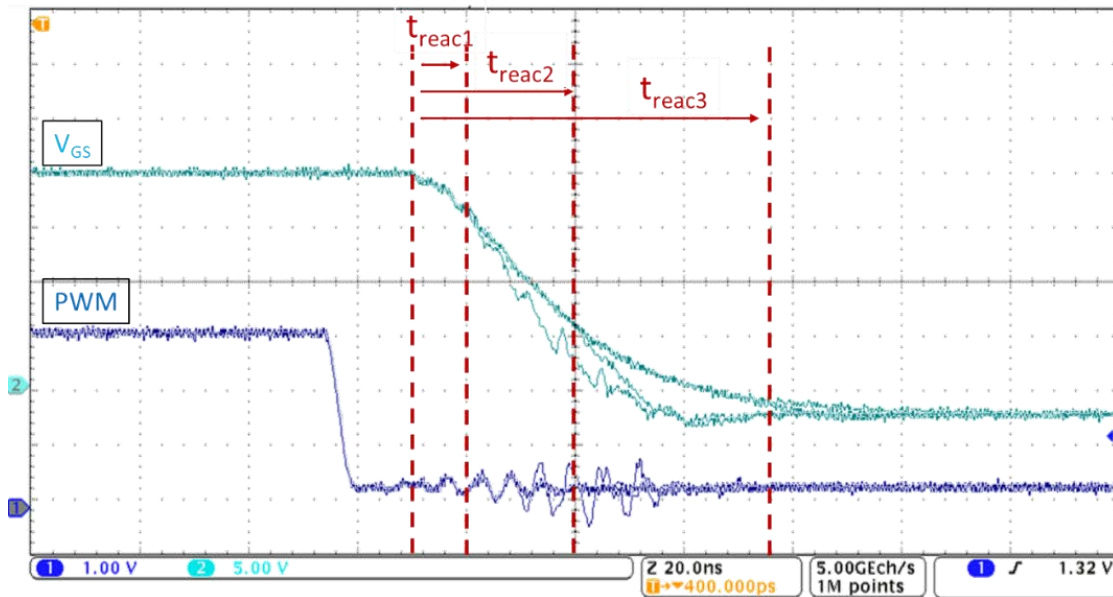
En_Configuration NMOS1 / NMOS2	$V_1 / V_2 / V_3$ (V)	$t_{pH-L}$	$t_{pH-L}$	$t_r$
		@10% (ns)	@50% (ns)	@90%=>10% (ns)
'1' '1'	4 / 16 / 4	20	35	43
'0' '1'	4 / 16 / 4	21	40	74
'1' '0'	4 / 16 / 4	25	55	92
'1' '1'	4 / 20 / 4	20	38	43
'0' '1'	4 / 20 / 4	22	48	87
'1' '0'	4 / 20 / 4	22	67	112

Secondly the active Miller clamp is being validated. Fig.II. 44 presents  $V_{GS}$  under different AMC configurations. The reaction time corresponds to the internal or external delay set.

The PWM propagation time is not considered in the reaction time, Fig.II. 44 . One can see for different AMC delays the fall time is decreased , Tab.II. 19. External delay set is configured by the FPGA.

**Tab.II. 19.**  $V_{GS}$  parameters for different AMC configuration @20V

En_Configuration COM1 / COM2	Delay set	$t_{reac}$	$t_r$
		@10% (ns)	@90%=>10% (ns)
'0' '0'	0ns internal	0	43
'1' '0'	10ns internal	10ns	33
'0' '1'	25ns internal	27ns	35
'1' '1'	50ns internal	50ns	43
'1' '0'	20ns external	20ns	35



**Fig.II. 44.**  $V_{GS}$  under different AMC configurations @  $V_{HV+}= 25V$  and each  $R_{G\_Ext}= 10\Omega$ ,  $C_{Eq}= 1.5nF$

Afterwards thanks to the FPGA configuration, besides the detection function, the high impedance state and the soft shut down can be validated by generating a detection flag with programmable delay generated by the FPGA. In this case the flag is generated after 150ns as one can see in the Fig.II. 45. The HZ state is activated first, then both HZ and SSD are activated. Under only HZ the gate voltage drops with a slow slope, probably due to SSD transistor leakage or another phenomenon that is not visible (capacitor discharge with a medium impedance, parasitic capacitor bridge). And under HZ+SSD there is faster drop which equal to 1 $\mu$ s. Nonetheless, both functions (HZ and SSD) are validated.



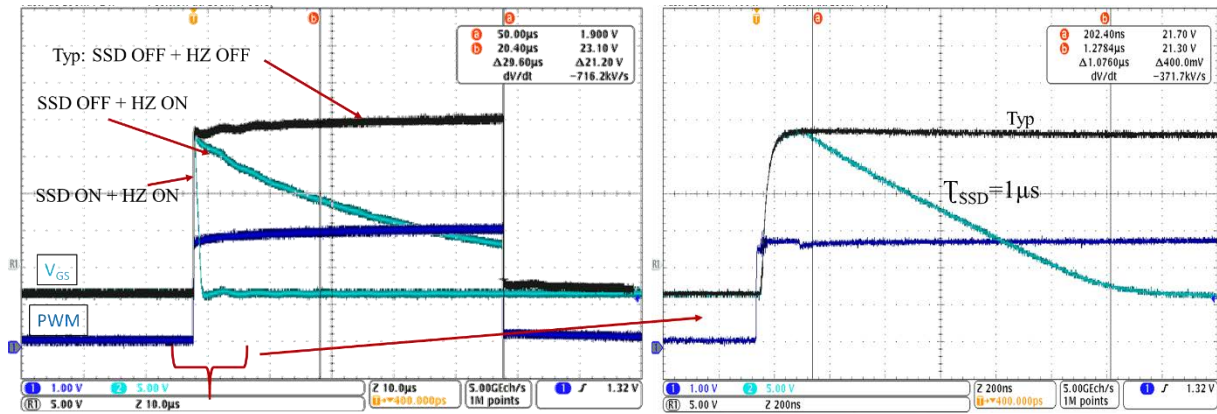


Fig.II. 45.  $V_{GS}$  under HZ and then under HZ + SSD @25V

#### 4.4.2. V2.A implementation in the power test bench V2

The ASIC was fully validated with a capacitor as load, equivalent to the input capacitance of the power device. In this section, the equivalent capacitor is removed and replaced with a power transistor C2M0080120 (DUT). The DUT was soldered vertically on the PCB. And the PCB was placed horizontally into the power test bench, Fig.II. 46 (b). On the high side, a 600V SiC diode is used, in parallel with a load inductor of 270 $\mu\text{H}$ . Fig.II. 46. (a) presents the test bench V2 with the different source meters. The circuit was validated under different bus voltages from 25V to 200V, under normal operation and short circuit operation, developed in details in Chap.III. Fig.II. 47. illustrates oscilloscope waveforms of the AGD under double pulse with  $V_{D_{rv+}} = 16\text{V}$  and  $V_{D_{rv-}} = 4\text{V}$  and with a split output where each output has a gate external resistor of 10 $\Omega$ ; and the DUT is supplied with 200V. Fig.II. 48 presents the zoom view at turn-on and turn-off with the same conditions. Note that the validation of the other functions has already been validated under an equivalent capacitor, as well as under SiC MOSFET.

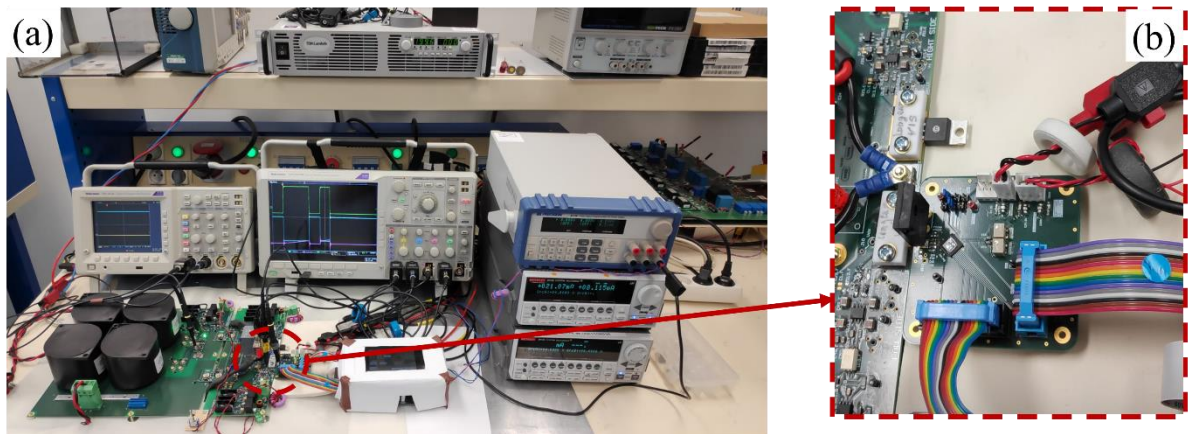
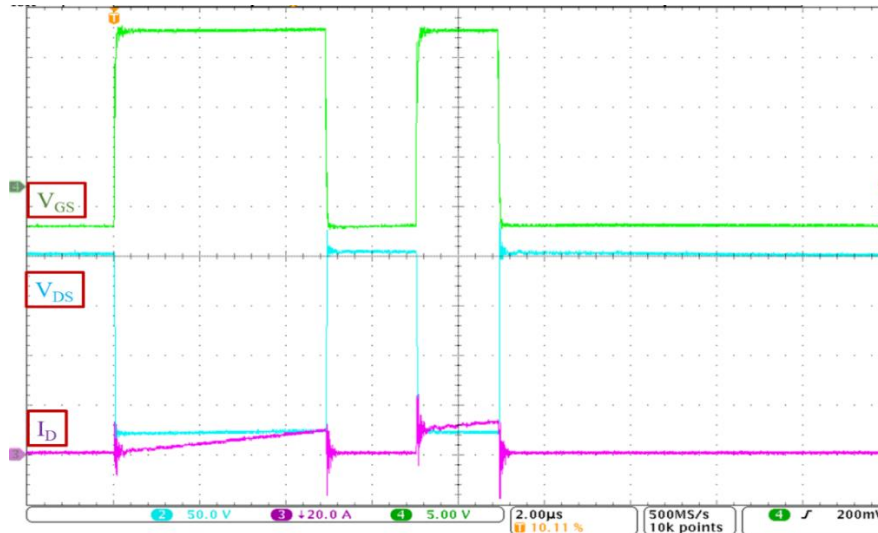
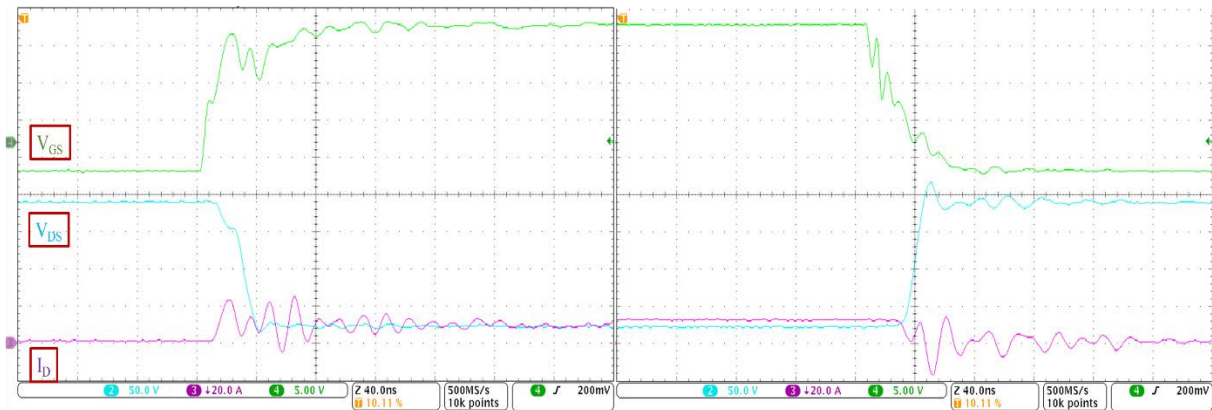


Fig.II. 46 . (a). test bench V2 with the PCB plugged-in (b). a zoom view on the plugged PCB



**Fig.II. 47.** Oscilloscope waveforms of the AGD under double pulse and DUT under 200V @  $V_{\text{Drv}+}=16\text{V}$  and  $V_{\text{Drv}-}=4\text{V}$



**Fig.II. 48.** Oscilloscope waveforms view at the turn-on and the turn-off of the DUT under 200V @  $V_{\text{Drv}+}=16\text{V}$  and  $V_{\text{Drv}-}=4\text{V}$

## 5. Modular Multilevel Gate driver MMAGD

Several features offered by SiC MOSFETs present specific driving challenges such as: a reduced short circuit capability (compared to Si IGBTs) and a weak field oxide layer, a large gate to source driving voltage (compared to GaN FETs), a high electric field under negative gate bias in off-state and a high switching speed. The negative bias in off-state creates a high stress which reduces the reliability of the SiC MOSFET. The high positive gate bias can generate large drain saturation current in case of short circuit events, [140] [67] [141]. In order to improve the overall performances and reliability of SiC MOSFETs and to offer new gate driving degrees of freedom, we propose a multilevel gate driver architecture (building-block approach) on a single CMOS IC, [142]. The principle is to use the highly efficient 5V transistors and capacitors for the gate driver, and to connect several stages in series, each stage being isolated via Deep Trench Isolation (DTI) and integrated on the same chip. As a consequence, the applied gate-to-source voltage of the SiC power MOSFET can be easily shaped, with new functionalities.

## 5.1. MMAGD topology

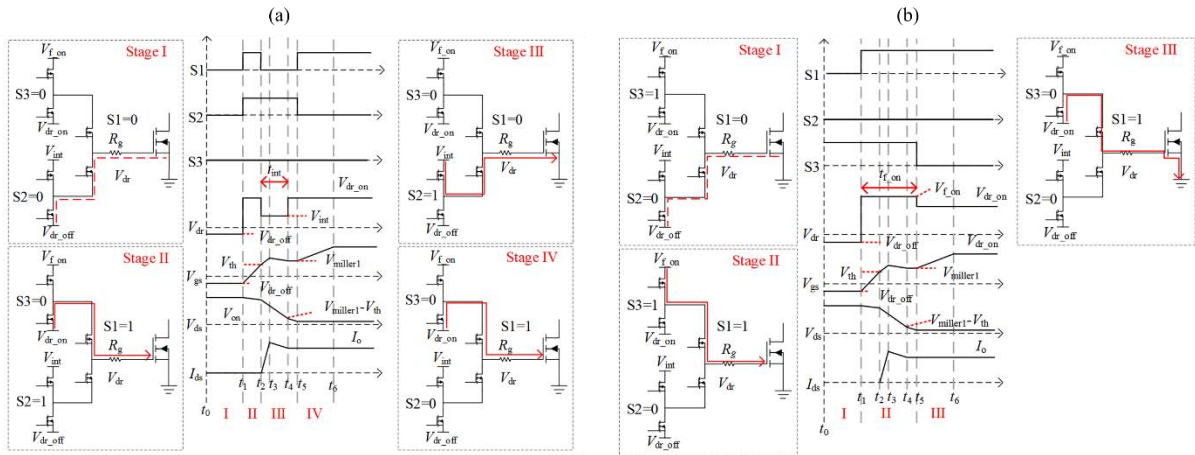
Classical gate driver topologies as the one developed above suffers from important limitations:

- The SiC gate driving voltages are linked with the IC technology and gate driver supply levels, hence neither their values nor the switching speed can be dynamically and quickly tuned. High voltage CMOS MOSFETs are required to be compatible with SiC driving voltages (e.g. >40V HV PMOS and NMOS for the output buffer).
- Under hard switching fault (HSF) type I short-circuit, the SiC MOSFET's drain current is only limited by the high saturation current (between 7 and 10 times the rated current), which is related to the large applied gate-to-source voltage during turn-on.
- In order to increase the safety margin of parasitic Miller coupling during  $dV_{DS}/dt$ , the negative  $V_{GS}$  during off-state creates a high stress on the SiC gate stack and also reduces the performances in III<sup>rd</sup> quadrant operation, [143] [144].
- The stored SiC gate charge is dissipated through the  $R_{G\_off}$  gate resistor during turn-off, whereas recycling such a gate charge would offer the possibility to downsize the isolated gate driver power supply.
- The high speed of the gate drivers has come at the expense of a low 5V maximum output voltage, due to the need to use fast low-voltage transistors in the design.

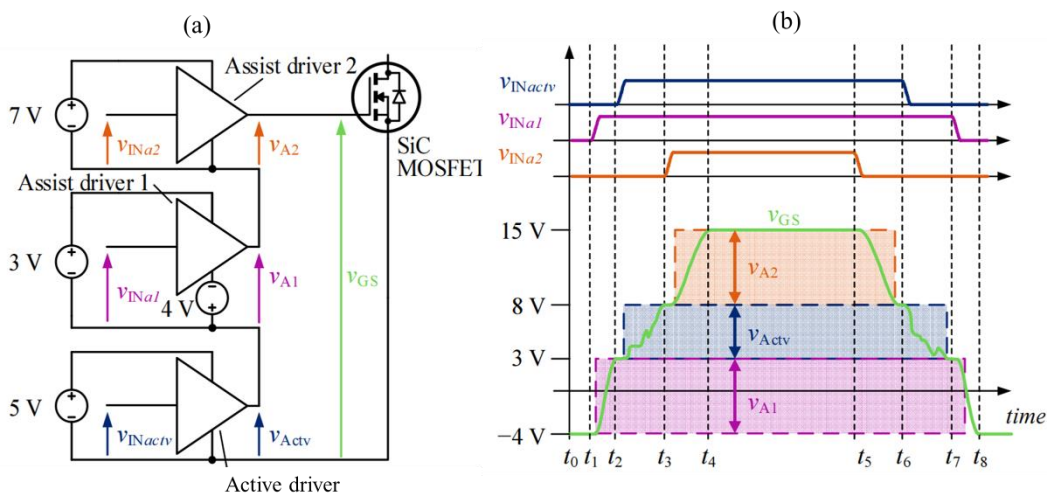
As a consequence of these limitations, one would like to actively tune the gate to source driving voltage of the SiC MOSFETs, to combine a high switching speed capability, low SiC on-state resistance, high immunity to  $dV_{DS}/dt$ , improved short circuit capability, and to modify the gate driver architecture.

Typical active gate driver would be connected directly to the source and gate terminals of the power device. However, drivers that operate with a 5V maximum supply cannot fully enhance a SiC MOSFET that requires 15V (or 20V) gate-source for minimum  $R_{DS\_On}$ , such as the 900-V, 65-m $\Omega$  C3M0065090J. Therefore, the idea is based on having a series of submodules, with a voltage supply range around 3V to 5V.

In the literature, one can find several ways to overcome one of this limitation. As far as the control of the slew rate of the semiconductor device is concerned, it is possible by different topologies as presented in chap.I variable gate resistance method, which can be programmable [145] [146]. These strategies balance the switching energy losses, EMI noise, and switching process duration, Fig.II. 49. Or other concepts such as [147] have been introduced in order to suppress crosstalk phenomena. Other attempts for multilevel gate drivers have been presented in the literature, mainly with discrete solutions [148] [149] [150] [34] [152] [153].



**Fig.II. 49.** The current flow for the (a). slow turn-on process (b). fast turn-on process.[31]

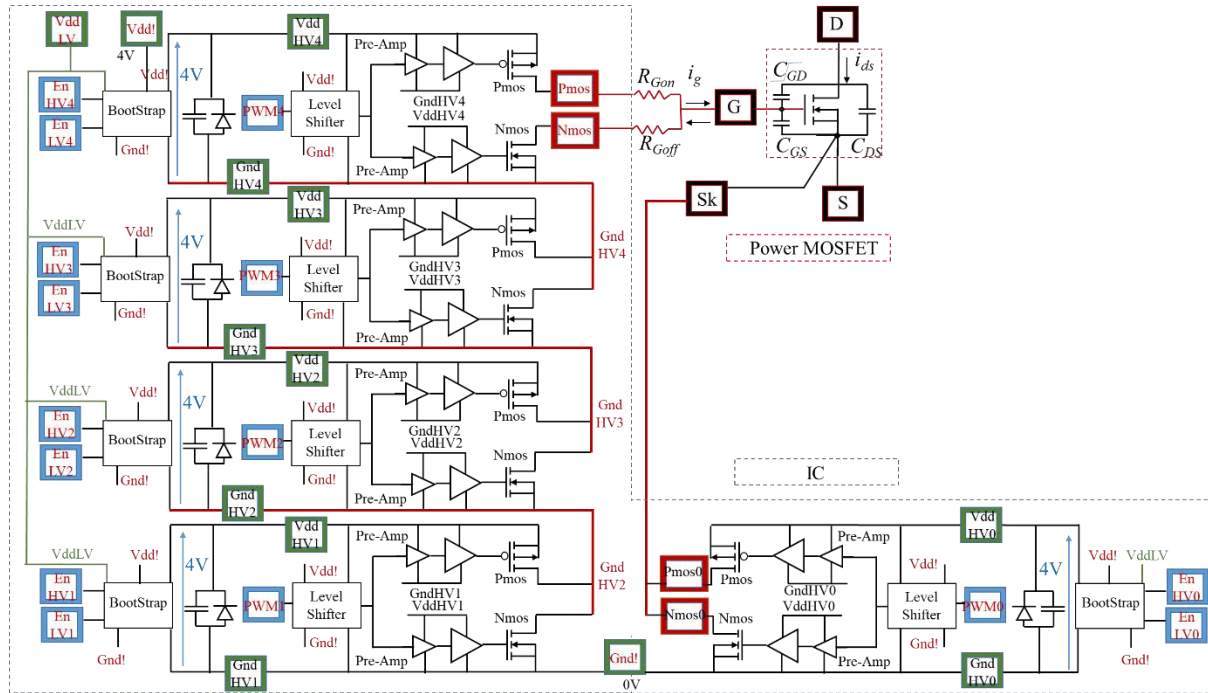


**Fig.II. 50.** (a). Multi-level Gate driver topology based on a discrete assembly (b). idealized waveforms demonstrating the multi-level series operation.[131]

Other than Fig.II. 49. which presents a different multi-level topology, reference [154] presents a three level gate driver with a different control strategy in order to turn the transistor into the saturation state. Our topology on the other hand is quite similar to the one in [131], where Fig.II. 50 presents the circuit topology and the relative activation timing, which is a discrete solutions. Referring to [131], in time period  $t_0$  to  $t_1$ , the input demands to all drivers ( $V_{INa1}$ ,  $V_{INa2}$ , and  $V_{INactv}$ ) are logic-low and their outputs ( $V_{A1}$ ,  $V_{A2}$ ,  $V_{Actv}$ ) held low. The output of the active gate driver is therefore connected to the gate of the SiC MOSFET via the low resistance of the assist drivers' pull-down transistors operating in the ohmic region, in series with the 4 V bias supply in the negative rail of assist driver 1. The MOSFET gate is therefore driven to 4 V below its source and it is off. From  $t_1$  to  $t_2$ ,  $V_{INa1}$  transitions to logic high and the first assist driver raises the gate potential to around the threshold region of the SiC MOSFET. From  $t_2$  to  $t_3$ ,  $V_{INactv}$  transitions to logic high, lifting the floating grounds of assist drivers 1 and 2 so the gate potential of the SiC MOSFET is increased by a further 5 V, with the active driver able to shape its output voltage during this switching transition. From  $t_3$  to  $t_4$ ,  $V_{INa2}$  goes high and the second assist gate



driver's output transitions to pull up, resulting in an overall gate-source voltage of 15V. The turn-off transient follows a similar pattern in reverse order, from  $t_5$  to  $t_8$ . The main purpose of [131] (Fig.II. 50) was actually to reuse a 5V CMOS active gate driver to drive SiC MOSFET. Hence, other discrete drivers were externally associated, and the CMOS active gate driver, initially developed for GaN power transistors, was able to actively control the SiC switching transient around its Miller and threshold voltages.



**Fig.II. 51.** Proposed multi-level modular SOI-CMOS gate driver (MMAGD), based on five submodules. All functions are integrated on one IC.

In our topology, the core idea here is to cascade 5V CMOS push-pull circuits in series, each being supplied by the energy stored in 5V floating capacitors, Fig.II. 51. This technique can also be applied with 1.8V or other voltages, which takes benefits of low voltage transistors and integrated capacitors with better figures of merit than high voltage CMOS transistors (e.g. >40V) for 2-level gate drivers. However, it is required to isolate each low voltage transistor, due to the non-zero common mode voltage (e.g. higher than 20V) and floating potentials as a function of the state of the other series-connected transistors. The X-FAB XT-018 SOI CMOS technology meet these criteria, thanks to its isolation capability with DTI. Each floating push-pull, pre-amplification circuits and level shifters are identical and can be described as an elementary 5V submodule, which must be compatible with the specified common mode voltages, Fig.II. 52. As presented in Fig.II. 51, we propose to integrate monolithically five identical submodules (four towards the gate, one to the Kelvin source) to allow a 6-level driving possibility, and both positive and negative  $V_{GS}$ . There is no modification on the SiC MOSFET and its interconnection with the gate driver. The main issue with this monolithic topology is that floating grounds and floating P-epitaxy regions of each submodule is typically not allowed by the foundry, albeit being isolated by Deep Trench Isolations and SOI substrate. When one

submodule changes its state, parasitic common-mode capacitive currents will flow through the isolated local substrates of each submodule. This issue must be carefully analyzed. However, a preliminary design has been done, while minimizing the common-mode parasitic capacitors.

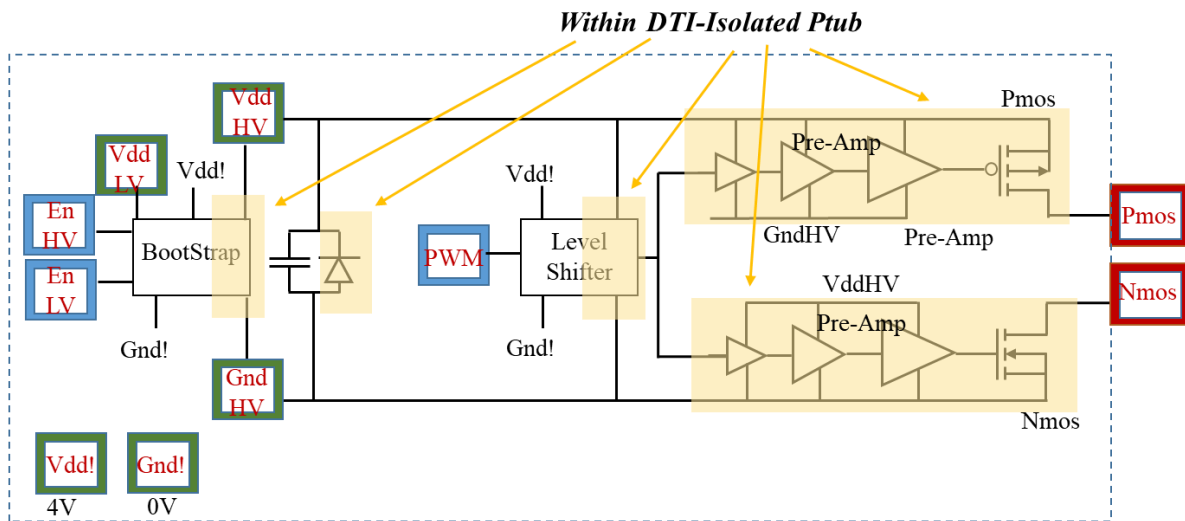


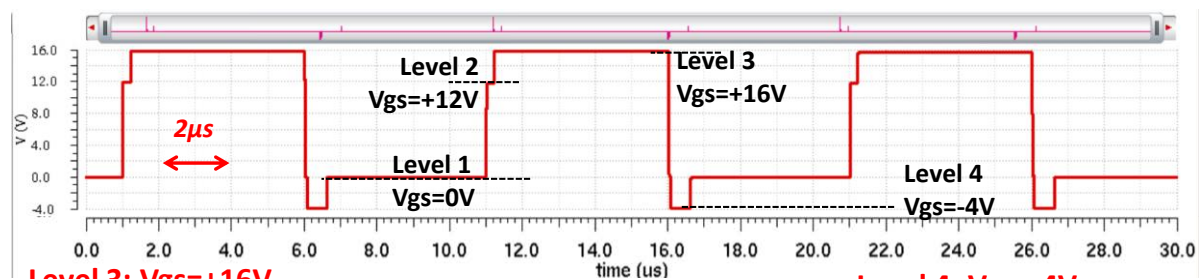
Fig.II. 52. Single stage of the multi-level highlighting DTI isolation

**Level 1:  $V_{GS}=0V$**

static turn-off at low field stress for DUT'SiO<sub>2</sub> and improved 3rq quadrant operation (static and dynamic)

**Level 2:  $V_{GS}=+12V$**

dynamic turn-on with low drain – source saturation current enabling a safe operation and a non critical protection delay in short-circuit event



**Level 3:  $V_{GS}=+16V$**

static on-state at high gate – source bias with low drop voltage and low on-state losses

**Level 4:  $V_{GS}=-4V$**

dynamic turn-off with high cross-talk immunity

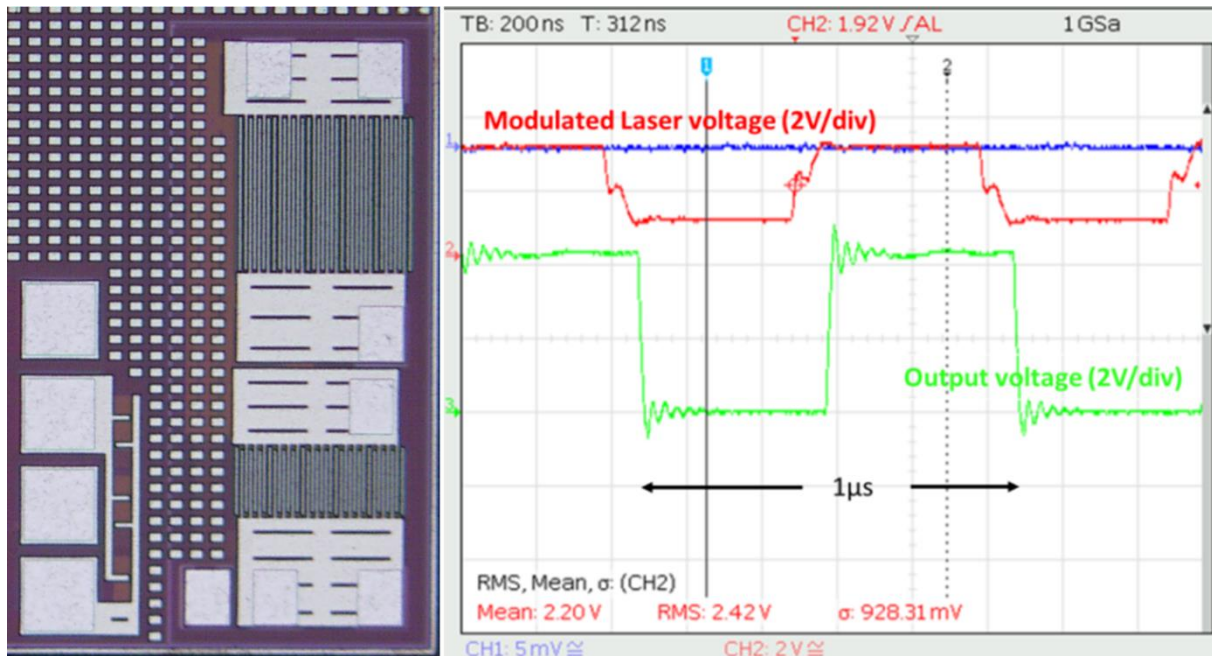
Fig.II. 53.  $V_{GS}$  simulated waveform with the multilevel architecture, highlighting the benefits of the multilevel driving scheme on the SiC MOSFET.

Fig.II. 53. shows the simulation of the MMAGD, where each floating capacitor is previously charged at 4V and an improved SiC driving is proposed. The PWM0...4 signals are generated based on the input PWM signal and the desired SiC  $V_{GS}$  voltage sequence. Several voltage levels can also be obtained by a different combination of PWM0...4 signals (e.g.  $V_{GS}=0V, +4V...+12V$ ). Benefits of the MMAGD are highlighted in Fig.II. 53: a reduced HSF short circuit current thanks to a reduced  $V_{GS}$  only during turn-on (albeit higher than the worst case Miller plateau voltage), a high  $V_{GS}$  for low SiC conduction losses, a dynamic negative  $V_{GS}$  to improve immunity to  $dV_{DS}/dt$  (high/low side crosstalk), and a zero  $V_{GS}$  in off-state to reduce the SiC field oxide stress. Even if the  $V_{GS}$  voltage is reduced to +12V during turn-on, the peak gate



current is maintained high to guarantee high switching speeds and low SiC switching losses thanks to a lower gate resistance than the one in classical 2-level operation. One has to note that the source internal resistance distributed on each submodule naturally contributes to this apparent gate resistance. The floating capacitors can be recharged by two ways: each submodule has a bootstrap-like circuit which can recharge its floating capacitor as long as the floating ground GND\_HV0...4 is connected to the IC GND, and/or by harvesting a part of the SiC gate charge during switching transitions.

The 5V output buffer used in each submodule was initially designed in a different PhD work [25] [155] [156]. Fig.II. 54 presents the characterization such a 5V buffer, which was designed and previously validated. The output 5V PMOS and NMOS of one submodule have a  $R_{DS\_ON}$  of  $0.26\Omega$  ( $25^\circ\text{C}$ ),  $\pm 5\text{A}$  source/sink capability and a maximum slew rate of  $5\text{V/ns}$ . Other specifications can be found in Davy Colin's and Thanh Long Le's work respectively [155] [157].

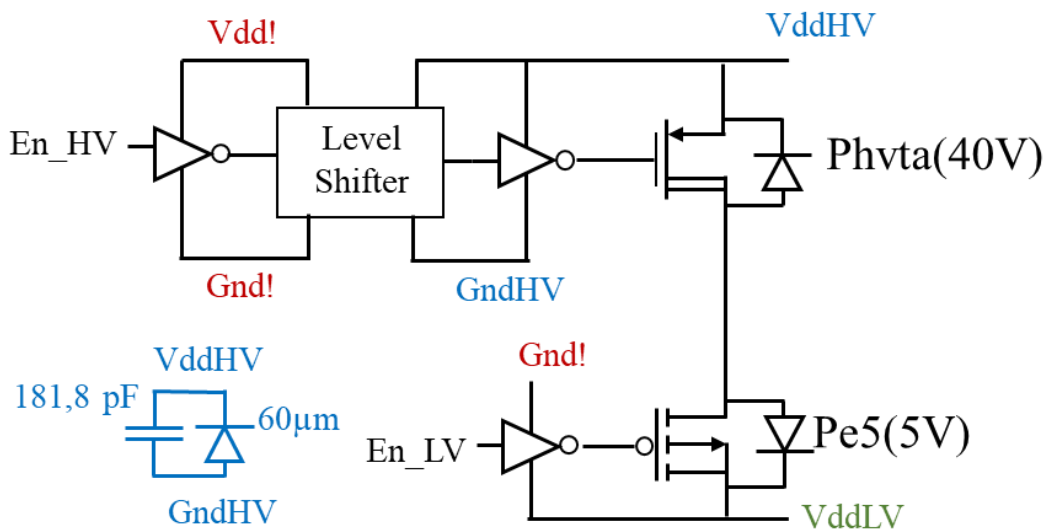


**Fig.II. 54.** Left, Optical microscope view of a 5V split output buffer [157]. Right, Experimental waveforms of one submodule on a 1nF constant capacitor, @ 1MHz,  $V_{GS} = 0\text{V}\dots+4\text{V}$ .

## 5.2. MMAGD design and layout

Each submodule is based on the previously proposed 5V- $0.26\Omega$  split output buffer. Hence the complete MMAGD exhibits a maximal total gate driver resistance of  $1.3\Omega$  for 5 submodules connected in series. In each submodule, the 5V split output buffer and its 5V pre-amplification have been within DTI-isolated P-type substrates. To be able to send the PWM0...4 activation signals from an input signal referenced to the IC global GND (labeled Gnd! On Fig.II. 51), differential level shifters are also integrated in each submodule. The same level shifter presented in the sections above is used. To store enough energy and to generate 4V floating supplies for each submodule, 180pF double density 5V-class MIM capacitors are integrated on chip. It is

however possible to extend the stored energy through external capacitors. However it is then required to add extra bonding wires to further connect to external capacitors for Gnd\_HV2..4 and Vdd\_HV2..4. This tradeoff between floating capacitor integration and constraints on packaging will be further optimized. In order to recharge the 4V floating capacitors for each submodule, a low voltage drop bootstrap circuit is integrated, **Fig.II. 55**. This bootstrap consists of a current source associated with a high voltage transistor rated for a maximum current of 0.1A and blocking capability of more than 40V. This current capability has been chosen as a good compromise between charging speed and Silicon area, considering that the prototype is aiming for a first proof of concept. First, an enable signal, En\_LV0...4, referenced to the chip ground Gnd!, activates the charge transfer from the global 4V Vdd\_LV to the floating submodule, should its floating ground Gnd\_HV0...4 be connected to the IC ground Gnd!. As soon as the floating Vdd\_HV0...4 has a high enough value, the low drop bootstrap can be activated through En\_HV0...4, reducing to less than 1mV the total bootstrap voltage drops to guarantees that Vdd\_HV0...4 reaches Vdd\_LV (e.g. 4V). These floating capacitors can also be recharged by recycling the stored SiC gate charge, if the PWM0...4 states offer a path for the gate current to flow through the floating capacitors. A protection Zener diode is also integrated to prevent over voltages.



**Fig.II. 55.** Bootstrap circuit

All these discussed blocks and circuit, are designed under cadence, the layout respects the same rules, developed in the previous section. ESD pads were used for the enables and the inputs and pads with metal 6 at the outputs, with an opening of 66 $\mu$ m\*66 $\mu$ m. The layout checks DRC and LVS rules, and added next to the AGD designed previously, at the left side of the chip. Fig.II. 56 presents a microscopic view of a single sub-module from the fabricated ASIC, with an area of 1050 $\mu$ m\*500 $\mu$ m. The whole view of the MMAGD is presented in Fig.II. 57 with an area of 2400 $\mu$ m\*1865 $\mu$ m. This layout has been done while focusing on time constraints: the 5V submodule has been duplicated, and most of the total area is used by the floating 5V capacitors and metal interconnection with the top power metal. Due to the Covid19 pandemic,

the characterization of the MMAGD has been postponed, whereas the top priority has been to characterize the core functions of this thesis (i.e. detection and protection of short circuit events). However, ten bare dies of MMAGD have been packaged, and the following works need to be done:

1. To design a specific PCB layout, which is required to comply with the packaging of the MMAGD
2. To characterize one 5V submodule: the bottom right submodule of Fig.II. 51 can also be used as a standalone 5V gate driver, to confirm the correct behavior and performance levels.
3. To characterize the MMAGD: fixed isolated power supplies can be used for the first measurements, whereas a FPGA must be programmed to generate the PWM signals.
4. To compare the monolithic MMAGD (i.e. all 5 submodules are integrated in one chip) with a discrete assembly of different 5V gate drivers (e.g. discrete assembly of several packaged 5V gate drivers). The purpose of this work would be to investigate the effects of parasitic capacitive currents in the monolithic version of the MMAGD.

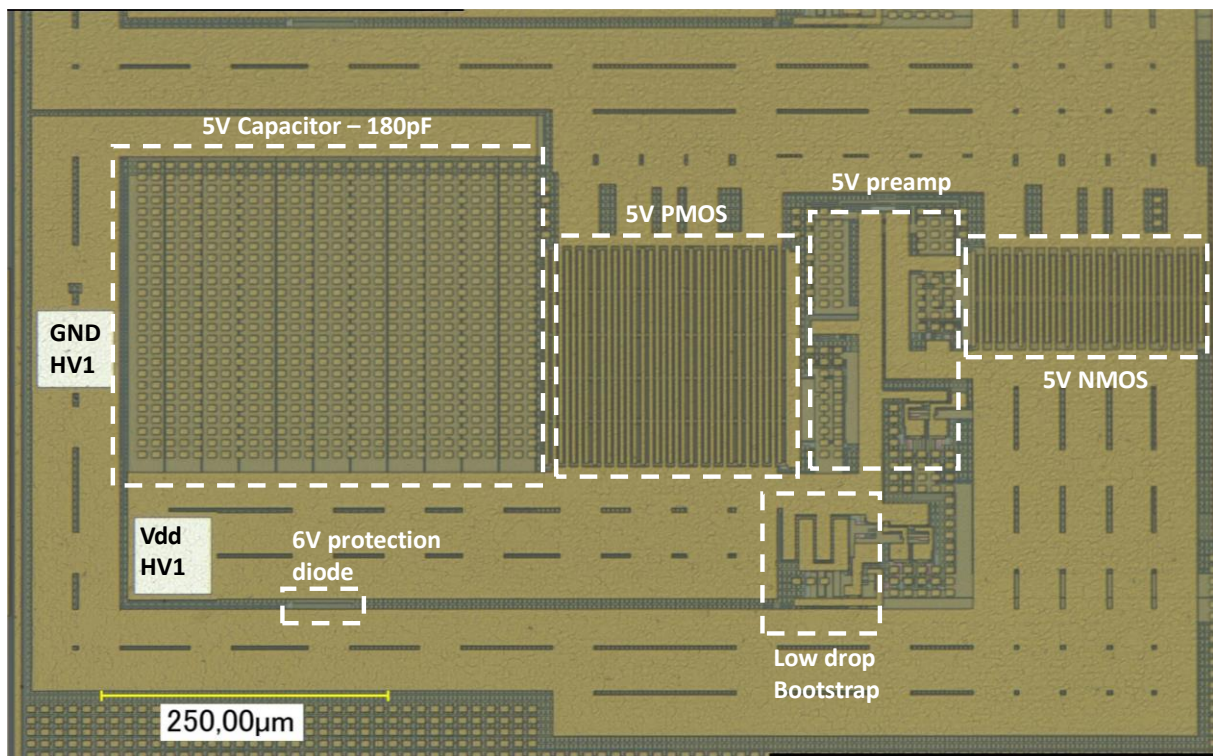


Fig.II. 56. Microscopic view of a single sub-module. Area is 1050 $\mu\text{m}$  x 500 $\mu\text{m}$ .



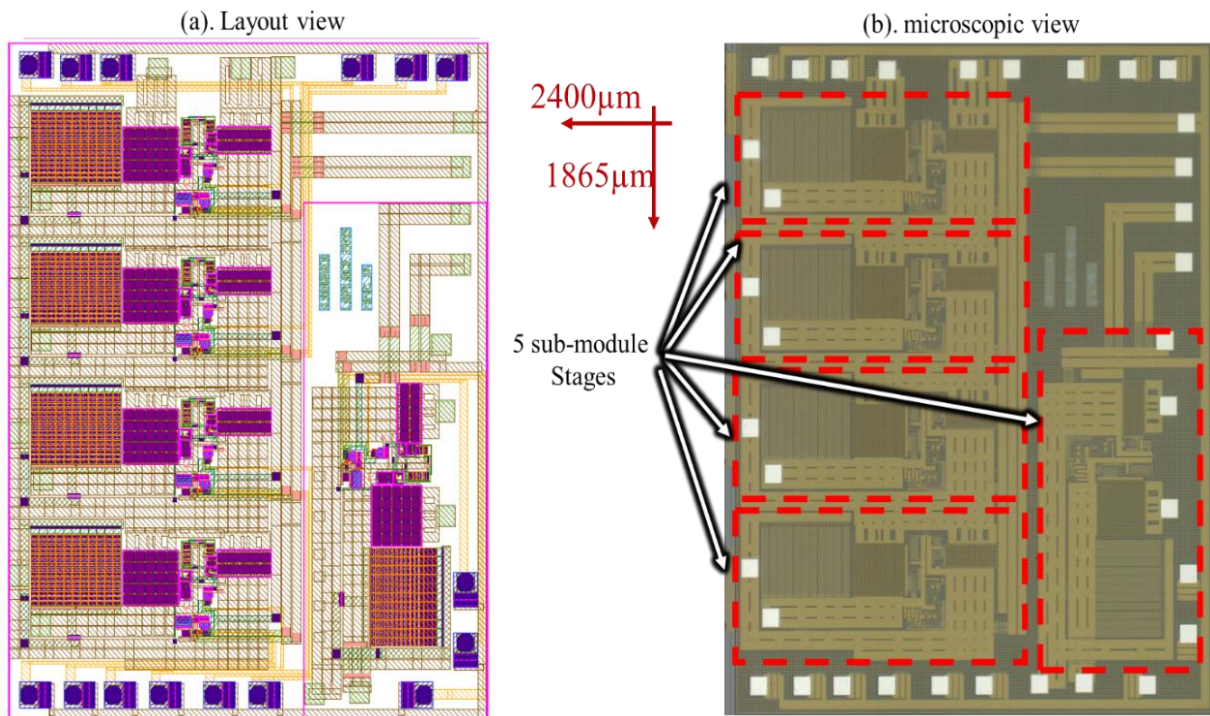


Fig.II. 57. (a). Layout view of MMAGD (b). Microscopic view of MMAGD

## 6. Conclusion

Two active gate drivers are integrated in a single chip using X-Fab SOI 0.18 $\mu\text{m}$ . The first active gate driver is a high voltage (40V) CMOS buffer with high current capability and integrated control functions, which is designed in order to host short-circuit detection techniques. This CMOS buffer also offers tunable gate current thanks to split output architecture and segmented design. On the other hand, an innovative architecture for an active gate driver for SiC MOSFET has been proposed. This modular multilevel active gate driver (MMAGD) offers new perspectives to tune the voltage levels of power MOSFETs during their switching transients. The key benefits of the MMAGD are to use elementary low differential voltage submodules, to reduce the stress for SiC short-circuit detection and protection, to reduce the electric field on the SiC gate stack during on-state while keeping a high immunity to Miller coupling, to offer the recharge of the integrated floating capacitors on each submodule and to reduce the isolated gate driver supply to 5V rather than 16-20V. In our first prototype, large values of floating capacitors are integrated on-chip to be able to assess the possibility to remove any external floating capacitor to supply the floating submodules. Experimental characterization of the monolithic MMAGD on SOI-CMOS is ongoing, with a focus on the optimized control technique to actively drive SiC MOSFETs and to recharge the floating capacitors with the highest efficiency. The ongoing experimental validations are aiming to compare the fabricated monolithic CMOS MMAGD with a PCB-integration of five submodules, and to demonstrate the driving and reliability improvements on SiC MOSFETs. The benefits of the modified gate driving scheme are also under investigation.

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## Chapter III: Proposed High-speed Short-Circuit monitoring and Protection for SiC MOSFETs

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## Chapter III: Proposed High-speed Short-Circuit monitoring and Protection for SiC MOSFETs

*Three short-circuit detection circuits are presented in this chapter in order to pile on exciting detection methods and to fill the present gap. As well as to answer to several problematics faced nowadays by SiC MOSFETs. The first method is based on the gate of the power transistor, integrating the sensed gate current to obtain the gate charge. This method goes by the name of the gate charge method. The second method is also based on the gate of the power transistor. But this time, the method is based on the derivative of the gate-source voltage, which shows promising differences. The third one is confidential. These methods have different levels of integration, each with its own benefits, most of the methods are experimentally validated and developed in this chapter.*

### 1. Introduction

As the SiC MOSFETs gain maturity and their cost goes down with time [2], SiC MOSFETs are expected to be adapted and used in more and more applications, as mentioned in Chap.I. In order to ensure high operations that is provided by the SiC MOSFETs devices, the gate driver should adapt to the specificities of SiC MOSFETs. Essentially, the driving peak current, small propagation delay, high frequency operation, and small power consumption, as discussed in the previous chapters. Another performance feature to be taken into account by the gate driver is the reliability of detection and protection against short-circuit (SC) events. Moreover, this detection and protection should be fast since SiC MOSFET short-circuit withstand capability is within  $t_{SC} = 2\mu\text{s}$  [3] [158], [159] instead of  $t_{SC} = 10\mu\text{s}$  for Si IGBTs. ( $t_{SC}$ : Short-Circuit Time capability). In addition, the SiC MOSFET has a much lower endurance for repeated short-circuit events than a silicon device. This endurance capability becomes lower, the longer the short-circuit application time, typically for  $t_{\text{Faulted-pulse}} > \frac{t_{SC}}{2}$  [65]. This is therefore clearly an additional reason to detect and turn-off softly the device with the shortest delay while providing robust detection to switching noise (typically  $t_{\text{Detection-delay}} \ll \frac{t_{SC}}{2}$ ). Therefore, the SiC MOSFET gate drivers compared to the Si IGBT ones have lesser time to detect the SC and protect the power device and to avoid ageing of the chip.

The methodology followed in Chap.I, is a clear study of the behavior of SiC MOSFETs under SC. The observed behavior permitted to identify the variables and parameters which can be leaned on in the circuit in order to detect a short-circuit as fast as required. Then, an in-depth study about the detection methods proposed by the literature is performed. The study shows that the short-circuit event can be detected by means of the de-saturation technique. However, the method requires a long blanking time, a high voltage diode root of disturbance by capacitive cross talk between power circuit and gate driver, and therefore impossible to integrate within a low voltage CMOS technology and without an adapted, expensive and non-standard case or package. Moreover, this monitoring strategy is not well suited, with MOSFET device, under high current overload operations because its ohmic on-state greatly depends on the junction temperature. Another detection method that showed promising results is the gate charge

method, which is developed and adapted for SiC MOSFETs in this chapter as a benchmark using discrete components. Due to the unique short-circuit damage and failure mechanisms the SiC MOSFETs have compared to those known for Si MOSFETs. Protection and reconfiguration devices are therefore no longer necessarily suitable for the use of SiC MOSFETs and new ones must be developed in accordance with these properties. The parameters and variables changes under SC and Normal Turn-On NTO helped to propose novel fast methods integrated in the gate driver designed and presented in this chapter. The active gate driver (AGD) is designed on purpose to detect the SC and to protect SiC MOSFETs [160].

The objective of this study is to contribute to filling this gap. This study presents and compares three original high-speed protection circuit methods. In order to do so, two original detection approaches are integrated: the occurrence (or not) of the Miller plateau, and the slope differences at the gate voltage, between normal operation and SC events, which offer different solutions and better performances than the prior art. These SC detection techniques are based on low voltage signals available in the gate driver.

Besides methods that are based on the gate side of the power transistor, a method based on the derivation of the power transistor drain-source voltage is proposed as well. The method is integrated in CMOS technology within low voltage transistors and a designed high voltage capacitor. None of the proposed or studied methods require a blanking time since they rely on the existence of particular geometric properties of the correlated waveforms. All of them have no time dependency, and can be easily integrated within the gate driver.

## 2. Gate charge monitoring

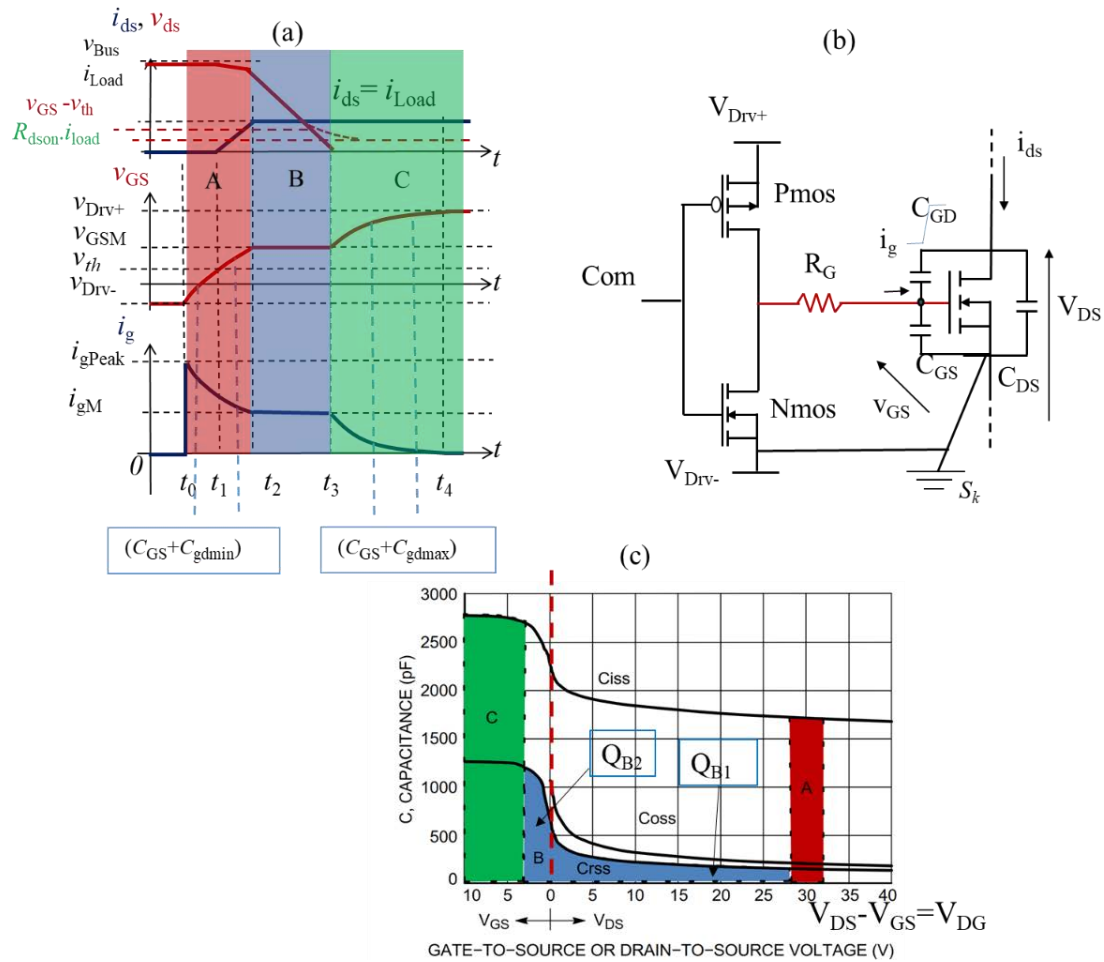
In order to experimentally validate the gate charge method, the method should be fully studied under NTO, HSF and FUL. Analytical and robustness studies are proposed in this section. As well the proposed detection circuit with its experimental results. This method is integrated using surface mounted devices SMD for a pre-validation, then a printed circuit board PCB dedicated to fully validate the gate charge method.

### 2.1. Analytical study of the Gate charge

#### 2.1.1. Normal Turn-on condition

( $V_{GS}$ ,  $V_{DS}$ ) characteristics are re-illustrated in Fig.III. 1.(a). In order to simplify the analytical study, all the non-linearity of the  $C_{OSS}$  capacitor is not considered, and the  $C_{RSS}$  capacitor is associated with only two state values without the non-linear transition being considered. The "short channel" effect is also not taken into account at this level and will be taken into account in the rest of this chapter. Moreover, we consider a constant threshold voltage  $V_{GS-th}$  over the switching cycle, this approximation is not always possible in MOSFET SiC technology because of the phenomenon of trapping/de-trapping of parasitic charges in the volume of the oxide in the increasing phase of  $V_{GS}$  [161].

Afterwards, the characteristic at turn-on and turn-off under NTO, HSF and FUL are fully presented in Chap.I. Fig.III. 1.(c) is presented, showing the variation of the capacitors of the power transistor [162] [90]. As shown, the basic three regions A, B, and C of the turn-on period, are highly reliant on the reverse capacitor  $C_{rss}$  of the power transistor [83] .



**Fig.III. 1. (a).** Simplified turn-on switching characteristics of SiC MOSFET under NTO conditions **(b).** Equivalent circuit of the command and the SiC transistor **(c).**Capacitance variation [162].

Note: in all graphical representations, the voltage  $V_{GS}$  is considered across of the field oxide. The internal equivalent polysilicon resistor is considered to be included in the external gate resistance. We will discuss this approximation in the implementation of detection methods.

### Region A:

Fig.III. 2. presents the qualitative typical switching waveforms and the different contributions to the total gate charge during normal turn-on (NTO). The first gate charge amount  $Q_A$  “ $Q_{GS}$ ” is defined by region A in the first time interval  $[t_0 - t_2]$  of Fig.III. 1.(a), where  $1/C_{iss\_Min}$  is its slope, eq.(III. 1).  $C_{iss}$  in region A is minimal and depends only  $V_{DS}$ , which is maximal.

$Q_1$  is a direct simplified representation amount of the gate charge between  $[V_{Drv-}; V_{GS\_M}]$  from the 2D diagram.

$$Q_A(V_{DG}) = \int_{V_{Bus}-V_{GS\_M}}^{V_{Bus}} C_{iss}(V_{DS-Max}, V_{GS}) * dV_{DG} \quad (III. 1)$$

With  $C_{iss}(V_{DS-Max}, V_{GS}) = C_{iss}(V_{DS-Max}) = C_{iss\_Min}$

$$Q_1(V_{GS}) = C_{iss\_Min} * (V_{GS} - V_{Drv-}); \quad V_{GS} \in [V_{Drv-}; V_{GS\_M}]$$

**Region B:**

$Q_{GD}$  is the second gate charge amount, between  $[t_2 - t_3]$  during the Miller plateau, where  $V_{DS}$  drops from  $(V_{Bus} + V_{Body})$  to approximately  $(V_{GS}-V_{th})$ , slightly higher than  $R_{DS\_ON} * I_{Load}$  while  $V_{GS}$  stays constant at  $V_{GS\_M}$  and  $C_{GD}$  or  $C_{Miller}$  starts to charge, allowing the fast voltage to change across the drain-source terminals, region B in Fig.III. 1.(c). In the presence of a SiC transistor, a short channel is generally used to reduce the losses in the on-state. This property causes a greater dependence of  $V_{GS\_M}$  to variations in drain voltage ( $I_{DS}-V_{DS}$  curve) than it can be in vertical silicon device (ex. SJ-VDMOS and IGBT), with a slight slope appearing instead of the plateau [9]. The gate charge is given in eq.(III. 2).  $Q_2$  cannot be simplified in a representative equation due to the constant  $V_{GS}$  at this period.

$$Q_B(V_{DG}) = \int_{-V_{GS\_M}}^{V_{Bus}-V_{GS\_M}} C_{rss}(V_{DG}) * dV_{DG}$$

With  $V_{DG} = V_{DS} - V_{GS}$  &  $C_{rss}(V_{GD}) = C_{rss\_B1} + C_{rss\_B2}$

With  $C_{rss\_B1} = C_{rss\_Min}$  &  $C_{rss\_B2} = C_{rss\_Max}$  (III. 2)

$$Q_B = Q_{B1} + Q_{B2}$$

$$Q_B(V_{DS}, V_{GS}) = \int_{V_{GS\_M}}^{V_{Bus}} C_{rss}(V_{DS}) * dV_{DS} + \int_0^{V_{GS\_M}} C_{rss}(V_{GS}) * dV_{GS}$$

**Region C:**

The third time interval begins at  $t_3$  with  $V_{GS}$  increasing back, until it reaches  $V_{Drv+}$ , and gate charge amount  $Q_G$  reaches  $Q_{G\_Tot}$  eq.(III. 4), with  $1/C_{iss\_Max}$  as a slope of the third amount of gate charge  $Q_C$  eq.(III. 3), region C in Fig.III. 1.(a). At the end of this time interval, the capacitance  $C_{GD}$  and  $C_{GS}$  are fully charged.

$Q_3$  is a direct representation amount of the gate charge between  $[V_{GS\_M}; V_{Drv+}]$  from the 2D diagram..

$$Q_C(V_{DG}) = \int_{V_{GS\_M}}^{V_{Drv+}} C_{iss}(V_{DS\_Min}, V_{GS}) * dV_{DG} |_{V_{Ds}=0} \quad (III. 3)$$

$$Q_3(V_{GS}) = C_{iss\_Max} * (V_{GS} - V_{GS\_M}); \quad V_{GS} \in [V_{GS\_M}; V_{Drv+}]$$

$Q_{G\_Tot}$  total is given by:

$$Q_{G\_Tot} = \Delta Q_1 + \Delta Q_{GD} + \Delta Q_3$$

$$Q_{G\_Tot} = C_{iss\_Min} * (V_{GS\_M} - V_{DRV-}) + [C_{rss\_Max} * V_{GS\_M} + C_{rss\_Max}] + C_{iss\_Max} * (V_{Drv+} - V_{GS\_M}) \quad (III. 4)$$

Note\*: Equations below are complementary to the gate charge equations, eq.(III. 5). In these equations we consider  $C_{GS}$  to be constant. In reality this capacitor is governed by the behavior of the internal PMOS and NMOS capacitors between the gate, the P-Well and the local N+ implementation in the MOSFET SiC channel region. These two equivalent capacitors themselves depend on the accumulation, depletion and inversion modes as a function mainly of the voltage  $V_{GS}$ . This fine modeling is not necessary in our study because it is more a "large signal" representation of the main phenomena.

$$C_{iss\_Max} = C_{iss}(V_{GS}) = C_{GD\_Max} + C_{GS} \quad (III. 5)$$

$$C_{iss\_Min} = C_{iss}(V_{DS}) = C_{GD\_Min} + C_{GS}$$

$$C_{rss} = C_{GD}$$

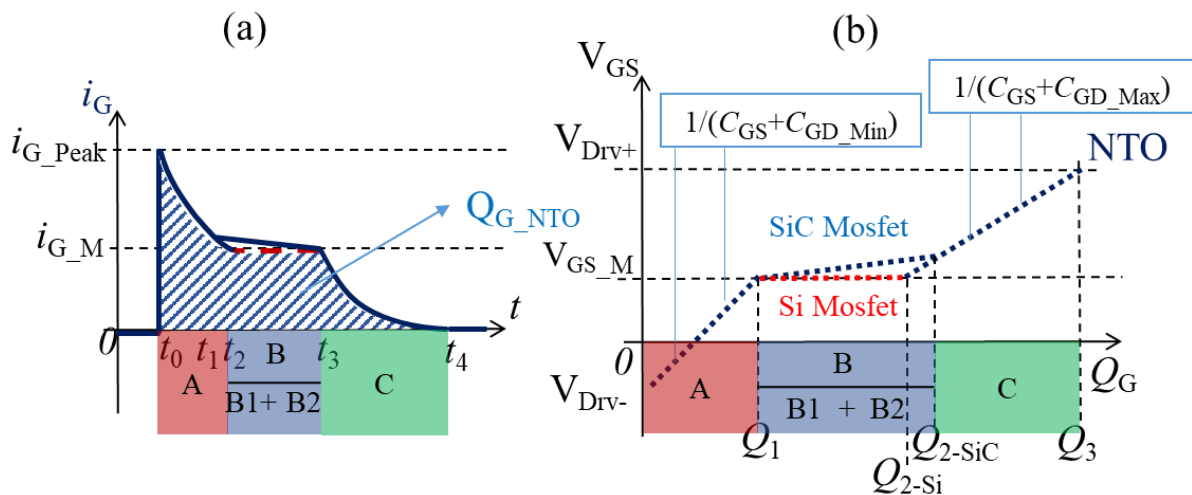


Fig.III. 2. (a).  $I_G$  curve under NTO (b). Gate Charge Characteristics under NTO.

### 2.1.2. Hard switch Fault condition

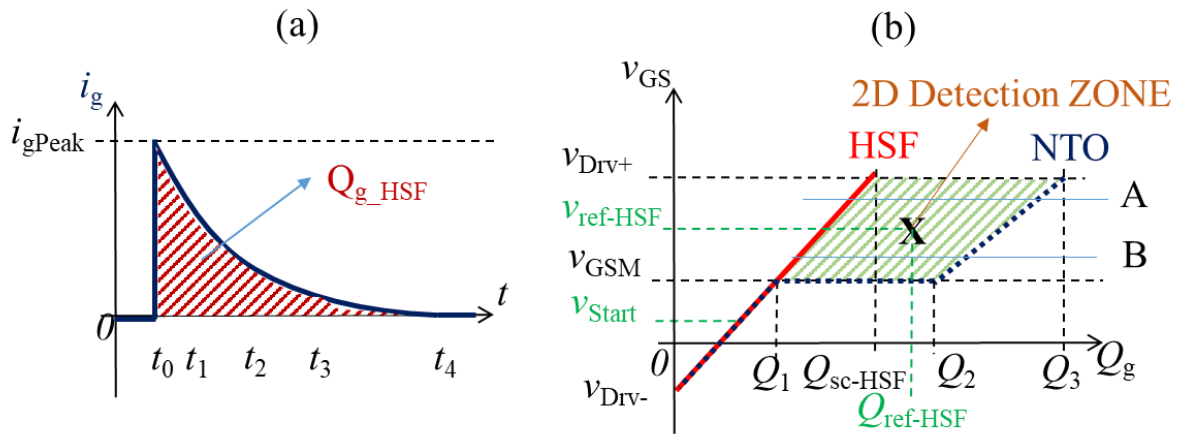
The amount of gate charge under HSF  $Q_{SC\_HSF}$  is given with a  $1/C_{iss\_Min}$  slope, exhibiting no change in the charging rate of the input capacitance [111]. In this SC operation, there is no



discharge of the Miller capacitance as long as the voltage  $V_{DS}$  does not show a significant variation so as not to induce charge transfer by  $C_{GD}$ . As a consequence, a significant difference appears in the  $Q_G$  characteristic between NTO and HSF, as shown in Fig.III. 3.

An HSF can be detected by monitoring  $V_{GS}$  and the amount of  $Q_G$ , whereas the assessment of the time variable is not directly required. As mentioned previously, a significant difference appears in the  $Q_G$  amount, as shown in  $Q_G$  characteristics, Fig.III. 3. A detection selectivity criterion can be introduced by the ratio  $(1/S)$  with  $S = (Q_{SC\_HSF})/(Q_{G\_Tot})$ . The ratio  $S$  is therefore a ratio between the quantity of gate charge under HSF and NTO. The smaller the ratio, the better the margin for the reference level  $Q_{Ref}$  set. A ratio close to unity but slightly lower, as on GaN device imply a difficulty in setting the  $Q_{Ref}$  level, especially when adding the oscillation and circuit parasitic elements.

In the Fig.III. 3, the one can observe two lines, A & B. These lines present the slowest but robust solution, line A; and the fastest but less robust solution, line B. The one should find the best comprise between both lines, in order to match the X point.



**Fig.III. 3. (a).**  $I_G$  curve under SC- HSF **(b).** Gate Charge Characteristics under HSF.

For a better detection, the threshold level of  $V_{Ref}$  and  $Q_{Ref}$  need to be in the hatched trapezoid  $\{(Q_1, V_{GS\_M}); (Q_2, V_{GS\_M}); (Q_{SC}, V_{Drv+}); (Q_3, V_{Drv+})\}$  of Fig.III. 3. Hence, this detection method represents a two-dimensional diagnosis. Most of the time, this  $Q_G$  characteristic figure is given in the datasheet under NTO. The choice of the threshold detection levels  $V_{Ref}$  and  $Q_{Ref}$  can then be assessed from the datasheet, respecting eq.(III. 6). Both  $V_{Ref\_HSF}$  and  $Q_{Ref\_HSF}$  are sets of a reference voltage respecting to  $k$  and  $k'$  in order to give the appropriate multiplier. On the other,  $V_{Start}$  is a fraction of the driven voltage ( $V_{Drv+} - V_{Drv-}$ ) of the gate driver with  $p$  as it ponderation multiplier, which is should be higher than  $V_{GS\_th}$ . For a selective detection the start reference can be set as a fraction of  $V_{Drv+}$ . Better selectivity reference is detailed later on the chapter. The method is naturally robust against variation in switching delay time due to variation in threshold voltage or current operating point of the load. With a constant threshold level, the detection will simply be a matter of integrated block design to obtain the gate charge  $Q_G$ .

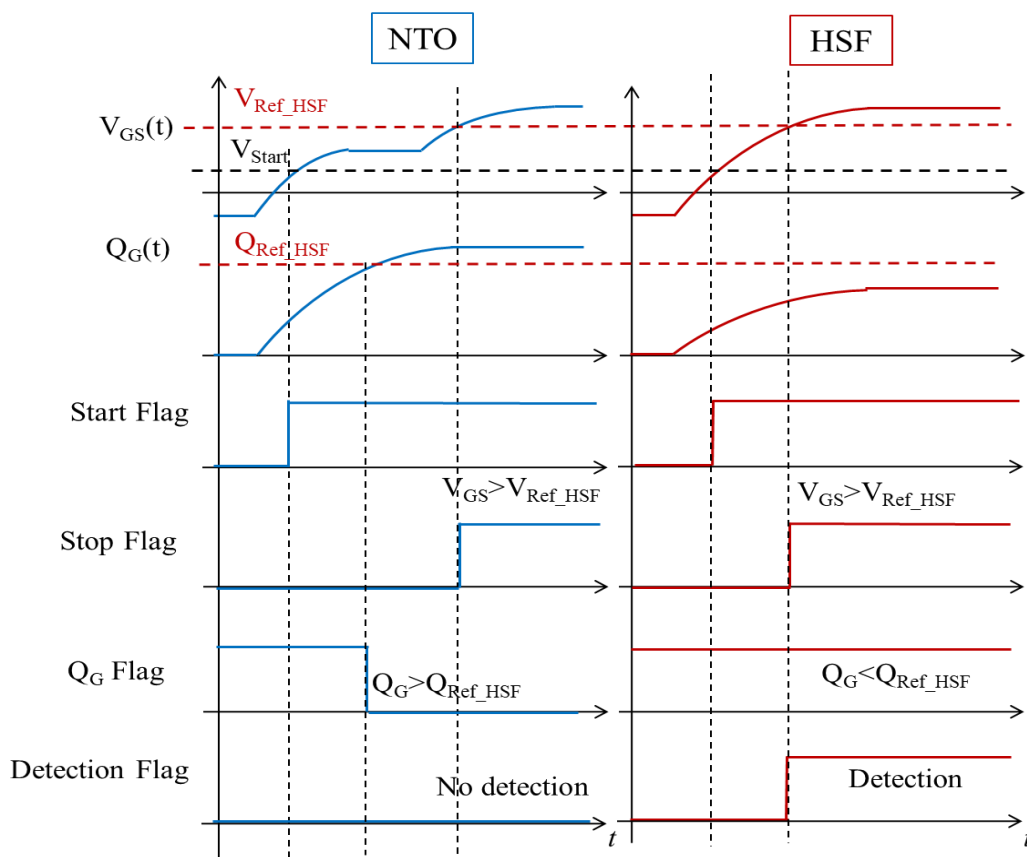
Note: the closer the coordinate point ( $V_{Ref}$ ,  $Q_{Ref}$ ) will be to the upper edge of the trapezoid, the more robust the detection will be at the cost of a longer delay than if the coordinates of the point are located on the lower edge. In theory, a choice between robustness and speed could be made. In practice, the best compromise will have to be found. However, like any ultra-fast detection method based on the switching cycle, the robustness criterion will be more important.

$$\begin{aligned}
 V_{Ref\_Start} &= p * V_{Drv+} \\
 V_{Ref\_HSF} &= k * V_{Drv+} \\
 Q_{Ref\_HSF} &= k' * Q_{G\_Tot}
 \end{aligned}
 \tag{III. 6}$$

With  $p$ ,  $k$ ,  $k'$  ponderation multipliers needed for the appropriate position of the reference levels.

**Tab.III. 1.** 2D diagnosis algorithm for HSF.

Comparator	Output diagnosis
If $Q_G > Q_{Ref\_HSF}$ AND $V_{GS} > V_{Ref\_HSF}$ then	NTO
If $Q_G < Q_{Ref\_HSF}$ AND $V_{GS} > V_{Ref\_HSF}$ then	HSF



**Fig.III. 4.** Timing chart under NTO and HSF conditions

For HSF in Tab.III. 1, when the output of the  $V_{Ref\_HSF}$  comparator reaches a logic state '1' (non-priority value of the AND gate), this signal goes through the first input of the AND-HSF gate. The second input decides the state of the detection circuit: if the calculated  $Q_G$  is below the

$Q_{Ref\_HSF}$ , then the second input (the output of the  $Q_{Ref\_HSF}$ ) of the AND-HSF gate goes to the high '1' logic state. The output of the AND-HSF gate goes high as well, which generates a flag for further SC protection. In contrast, if one of those two inputs; the two outputs of the  $V_{Ref\_HSF}$  and  $Q_{Ref\_HSF}$  comparators; is in a '0' logic state, there is no flag and no detected SC, Fig.III. 4.

### 2.1.3. Fault under load condition

In contrast, fault condition type II appears after the three normal regions are accomplished, namely, after  $t_4$ , fig.III. 1.(a), where the MOSFET is in on-state ohmic mode  $V_{GS} = V_{Drv+}$ . In this fault condition,  $I_{DS}$  increases to  $I_{DS\_Saturation}$  causing a positive value  $dV_{DS}/dt$ . A reverse current flows into the gate  $I_G < 0$  through  $C_{GD}$ . All these phenomena lead to the increase of  $V_{GS}$  towards a larger value  $V_{GS\_OV}$ . The amount of gate charge is  $Q_{SC\_FUL}$ , which also corresponds to a higher gate voltage  $V_{GS\_OV}$ , [163]. A FUL can be detected by monitoring  $V_{GS}$  and the amount of  $Q_G$  as well, like HSF, but for different threshold levels of  $V_{Ref}$  and  $Q_{Ref}$ , eq.(III. 7), whose values need to be in the hatched triangle of Fig.III. 5.

$$\begin{aligned} V_{Ref\_Start} &= p * V_{Drv+} \\ V_{Ref\_FUL} &= (1 + r) * V_{Drv+} \end{aligned} \quad (III. 7)$$

$$Q_{Ref\_FUL} = r' * Q_{G\_Tot}$$

With  $p, r, r'$  ponderation multipliers needed for the appropriate position of the reference levels.

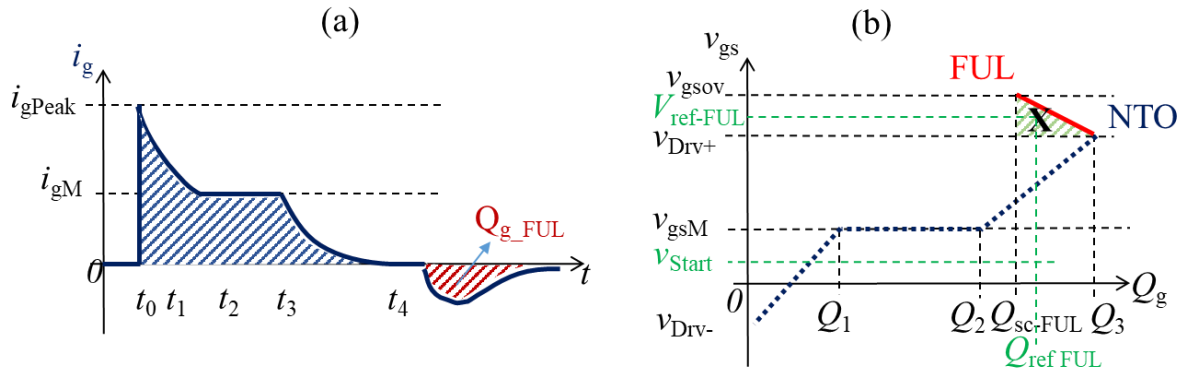


Fig.III. 5. (a).  $I_G$  curve under SC- FUL (b). Gate Charge Characteristics under FUL.

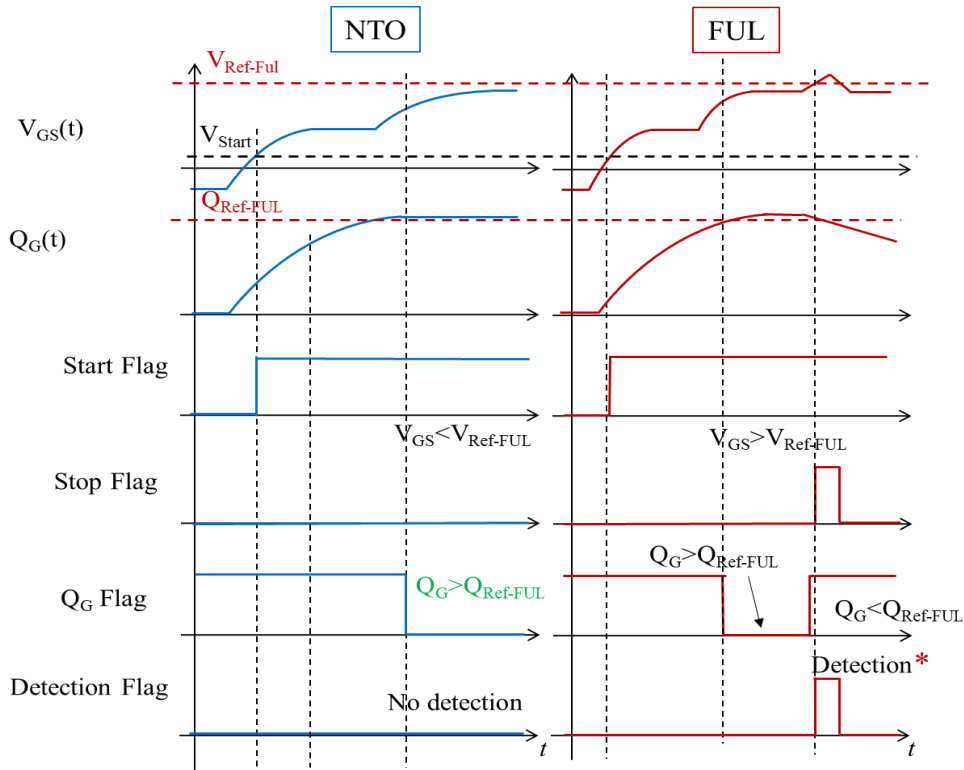


Fig.III. 6. Timing chart under NTO and FUL conditions.

Tab.III. 2. Diagnosis algorithm for FUL

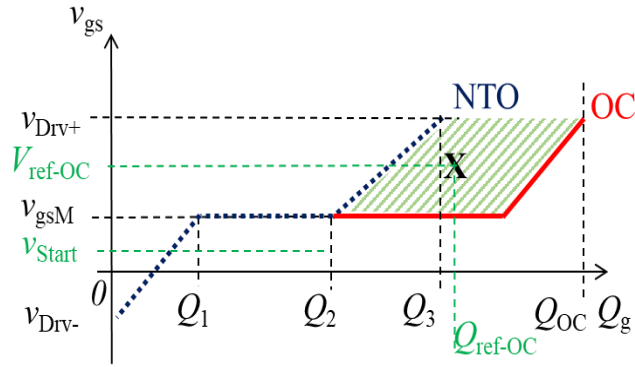
Comparator	Output diagnosis
If $Q_G > Q_{Ref\_FUL}$ AND $V_{GS} < V_{Ref\_FUL}$ then	NTO
If $Q_G < Q_{Ref\_FUL}$ AND $V_{GS} > V_{Ref\_FUL}$ then	FUL

For FUL, the same method is applied as HSF, where both  $V_{Ref\_FUL}$  and  $Q_{Ref\_FUL}$  comparator outputs need to have a ‘1’ logic state. The output of the AND-FUL gate goes high as well, which generates a detection flag, to be used to protect the circuit, Fig.III. 6. The detection (\*) is for a brief period, which add the necessity of an RS flip-flop to maintain the flag detection.

#### 2.1.4. Open Circuit condition

Moreover, the open-circuit fault can also be detected by gate charge characteristics. Open circuit occurs at zero bus voltage, or other phenomena. The open circuit can be due to several aspects as the package is broken, or and an open fuse in the power circuit, or a physical internal opening (disconnection of the internal paths), etc ...

When the open-circuit fault occurs, the value of drain-source voltage  $V_{DS}$  stays at its minimal value, which is approximately zero [164] [106] [165]. Hence, the capacitance  $C_{GD}$  under open-circuit fault is larger than that of short-circuit faults. The turn-on gate voltage comparison between the open-circuit fault and the normal condition is plotted in Fig.III. 7. The time duration of the Miller plateau voltage during normal condition is shorter than during the open-circuit condition, and  $Q_{G\_Tot}$  under NTO is also less than the charge  $Q_{OC}$  under open-circuit fault, eq.(III. 8).



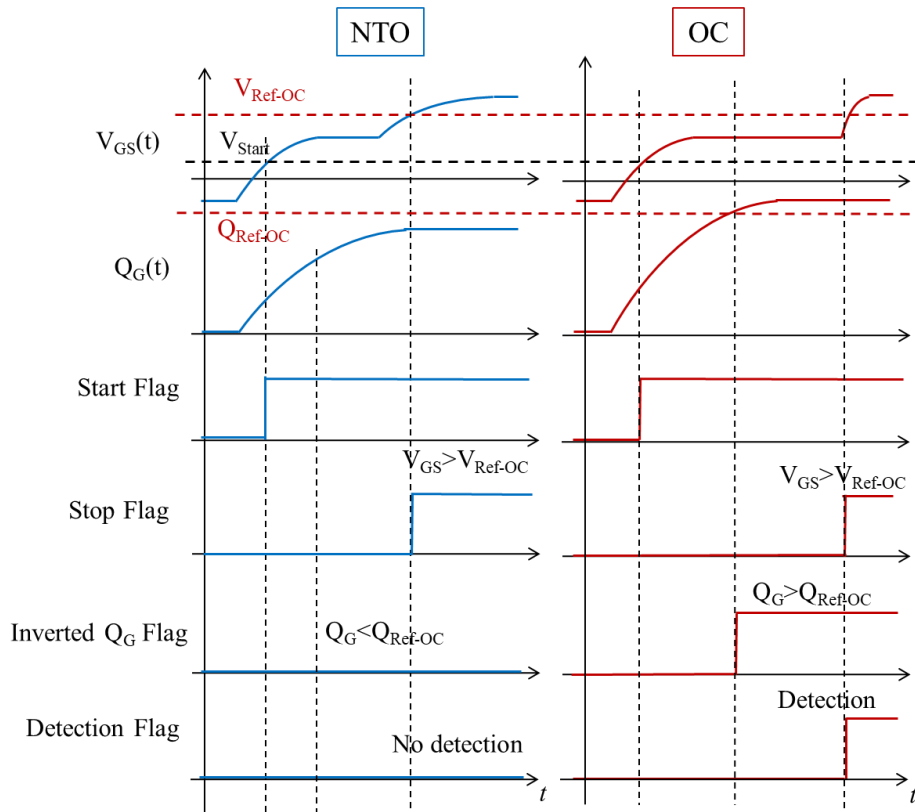
**Fig.III. 7.** Gate Charge Characteristics under open circuit condition.

$$\begin{aligned}
 V_{Ref\_Start} &= p * V_{Drv+} \\
 V_{Ref\_OC} &= j * V_{Drv+} \\
 Q_{Ref\_OC} &= (1 + j') * Q_{G\_Tot}
 \end{aligned}
 \tag{III. 8}$$

With  $p, j, j'$  ponderation multipliers needed for the appropriate position of the reference levels.

**Tab.III. 3.** Diagnosis algorithm for OC

Comparator	Output diagnosis
If $Q_G < Q_{Ref\_OC}$ AND $V_{GS} > V_{Ref\_OC}$ then	NTO
If $Q_G > Q_{Ref\_OC}$ AND $V_{GS} > V_{Ref\_OC}$ then	OC



**Fig.III. 8.** Timing chart under NTO and OC conditions.



Fig.III. 3, Fig.III. 5 and Fig.III. 7 are mandatory to design the integrator of the detection design by providing the value of the gate charge and its position regarding  $V_{GS}$ .

Tab.III. 1, Tab.III. 2 and Tab.III. 3 simplify the aforementioned figures regarding the gate charge  $Q_G(V_{GS})$  and  $V_{GS}(t)$  characteristics under NTO, HSF, FUL or OC. The table as well provides a direct guidance for the design of the comparators and the logic gates of the circuit.

## 2.2. Gate charge robustness study

The gate charge method is naturally robust against variation in switching delay time due to variation in threshold voltage or current operating point of the load, but it starts to be challenging when it comes for very smaller input capacitance, and high  $dV_{DS}/dt$  switching parasitic [111]. With a constant threshold level, the detection will simply be a matter of integrated block design to obtain the gate charge  $Q_G$ . A detection selectivity criterion can be introduced by the ratio  $S$ . The ratio  $S$  is therefore a ratio between the quantity of gate charge under HSF and NTO. The ratio is given by, eq.(III. 9):

$$\begin{aligned} S(V_{GS1}) &= \frac{Q_{SC\_HSF}(V_{GS1})}{Q_{G\_Tot}(V_{GS1})} & V_{GS} \in [0, V_{Drv+}] \\ S(V_{GS2}) &= \frac{Q_{SC\_HSF}(V_{GS2})}{Q_{G\_Tot}(V_{GS2})} & V_{GS} \in [V_{Drv-}, V_{Drv+}] \\ S(V_{GS3}) &= \frac{Q_{SC\_HSF}(V_{GS3})}{Q_{G\_Tot}(V_{GS3})} & V_{GS} \in [V_{th\_80\%}, V_{Drv+}] \end{aligned} \quad (III. 9)$$

This principle will be more sensitive and robust for lower  $Q_{SC\_HSF}/Q_{G\_Tot}$  ratios. This constraint is far from assured for WBG devices, where the  $C_{GD}/C_{GS}$  ratio is voluntarily minimized by designers to reduce the cross-talk phenomenon in inverter leg operation. As shown in Tab.III. 4, some commercially available SiC devices will be more suitable than others. Commercially available high-voltage GaN power transistors seem poorly adapted to this technique, while other protection techniques are adapted for GaN [166]. Higher  $V_{Ref\_HSF}$  values lead to a more robust diagnosis, albeit with longer delay times. Nevertheless, it remains a general principle, also named "2D adaptive detection", only combining two low-voltage waveforms or signals without resorting directly to time measurements. Moreover, the  $Q_G$  method is an integral technique that will introduce less signal-to-noise ratio (SNR).

The ratio  $S$  in the table is calculated for different  $V_{GS}$  which allows to reduce the stress on the integration, as well as to have more controllability on when to start the integration and when to stop it, regarding the fault type.

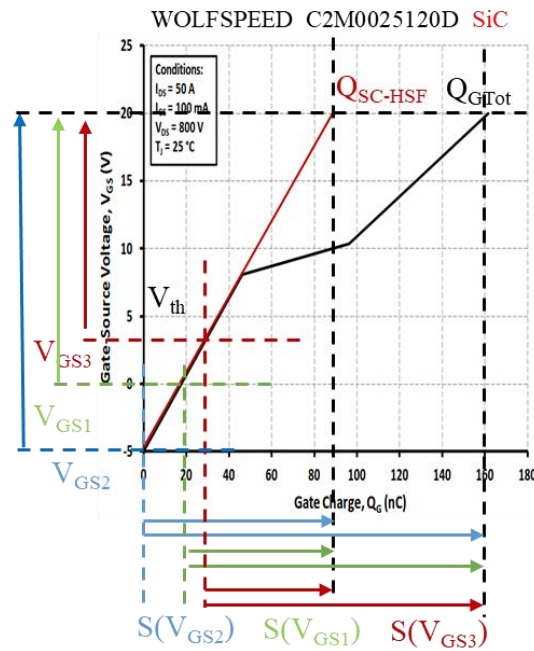
The different ratios  $S$  presented in Tab.III. 4 are extracted from their gate charge plot proposed in their data sheet, as shown in Fig.III. 9. The table offers a different perspective on the amount of the gate charge and flexibility between NTO and HSF. As one can see the smaller the ratio the better the safe margin to set the reference level. GaN semiconductors have a smaller

input capacitor which makes it harder to distinguish between NTO and HSF. Contrary to silicon semiconductors which have the lowest ratio and the best flexibility.

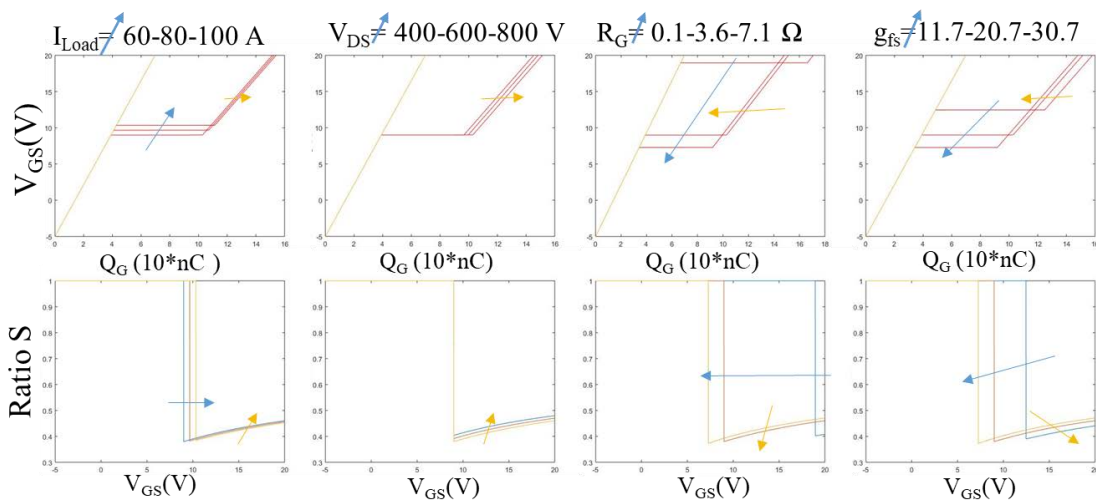
**Tab.III. 4.** Ratio S for different  $V_{GS}$  and different power semiconductors (GaN, SiC IGBT, Silicon)

Techno	Model	Type	$Q_{sc\_HSF}$ (nC)		$S(V_{GS1})$	$Q_{sc\_HSF}$ (nC)		$S(V_{GS2})$	$Q_{sc\_HSF}$ (nC)		$S(V_{GS3})$	Condition															
			$Q_{G\_Tot}$ (nC)	$Q_{G\_Tot}$ (nC)		$Q_{G\_Tot}$ (nC)	$Q_{G\_Tot}$ (nC)		$Q_{G\_Tot}$ (nC)	$Q_{G\_Tot}$ (nC)		$V_{GS1}$	$V_{GS2}$	$V_{GS3}$	$V_{DD} : I_D$	$R_{G\_Int} \Omega$	$C_{iss} \text{ pF}$ Min/Max										
GAN	GANSYSTEM S	GS61008TDS	8,5	11,2	0,71	11,2	0,78	6,8	0,66	0/6V	-3/6V	$V_{GS80\%/6V}$	50V : 90A	0,64	600/700												
			12	14,2		10,2																					
		GS66506TDS	3,1	4,5	0,70	5,8	0,77	2,6	0,66	0/6V	-3/6V	$V_{GS80\%/6V}$	400V : 22,5A	1,1	220/185												
			4,4	5,8		3,9																					
GS66508TDS	3,7	5	0,64	6,9	0,72	2,9	0,59	0/6V	-3/6V	$V_{GS80\%/6V}$	400V(100V): 30A	1,1	290/240														
	5,8	6,9		4,9																							
GS66516TDS	8,5	12,4	0,70	16	0,77	6,9	0,64	0/6V	-3/6V	$V_{GS80\%/6V}$	400V(100V): 60A	0,34	610/520														
	12,1	16		10,7																							
SiC	Littelfuse	LSIC1M0120E080	-	43,6	-	95	0,46	30,6	0,37	-	-5/20V	$V_{GS80\%/20V}$	80V : 20A	1	3000/1820												
			-	95	82																						
	MICROSEMI	APT40SM120BC	44,3	57	0,34	143	0,4	37,8	0,30	0/20V	-5/20V	$V_{GS80\%/20V}$	800V : 20A	0,7	3900/2080												
			130	143		123,5																					
	ROHM	SCT2080KE	50	65	0,47	121	0,53	44,3	0,44	0/18V	-5/18V	$V_{GS80\%/18V}$	400V : 10A	6,3	3800/2080												
			106	121		100,3																					
			26	33		22,4	0,32	0/18V		-5/18V	$V_{GS80\%/18V}$					400V : 7A	13,7	2050/1200									
			62	69		68,4																					
			75	95		59		0,36		0/18V									-5/18V	$V_{GS80\%/18V}$	300V : 47A	4	4700/2880				
			176	196		160																					
	26,5	33,4	20,4	0,48	0/18V	-5/18V			$V_{GS80\%/18V}$	300V : 10A		13	1000/570														
	48	54,9	41,8																								
	20,4	26,4	15,8		0,47	0/18V	-5/18V				$V_{GS80\%/18V}$			300V : 6,7A	18	700/460											
	38	44	33,4																								
	ST	SCT30n120	40,5			48,5	0,38	113									0,42	33,9	0,34	0/20V	-4/20V	$V_{GS80\%/20V}$	800V : 20A	5	2500/1700		
			105			113		98,4																			
WOLFSPEED	C2M0025120D	-	90	-		161	0,56	65	0,47	-		-5/20V	$V_{GS80\%/20V}$				800V : 50A	1,1	4100/2780								
		-	28,8			20,4	0,38	-		-5/20V		$V_{GS80\%/20V}$								800V : 20A	4,6	1900/1100					
		-	62		53,6																						
		-	16		11,5	0,39		-		-5/20V	$V_{GS80\%/20V}$			800V : 10A	6,5	800/600											
		-	34		29,5																						
		-	38,4		27,4			0,36		-													-4/15V	$V_{GS80\%/15V}$	600V : 35A	3	2100/1740
		-	87		76																						
-	15,5	11	0,42	-	-4/15V				$V_{GS80\%/15V}$	400V : 20A			4,7				1060/760										
-	30,4	25,9																									
-	8,4	5,8		0,39	-		-4/15V					$V_{GS80\%/15V}$						400V : 15A	16	420/350							
-	17,3	14,7																									
-	19	10																									
SILICON	INFINEON	IKW15N120H3			15	19	0,20	79			0,24			10	0,13	0/15V					-4/15V	$V_{GS80\%/15V}$	960V : 40A	-	1200/870		
					75	79		75																			
		IKW25N120H3	22,5		29,5	0,19	122	0,24	15,4	0,14	0/15V		-4/15V	$V_{GS80\%/15V}$	960V : 25A	-	2000/1430										
			115		122		107,9																				
IKW40N120H3	33,2	43,7	0,18	195,5	0,22	23,8	0,13	0/15V	-4/15V	$V_{GS80\%/15V}$	960V : 15A	-	3400/2230														
	185	195,5		175,6																							

The SiC MOSFETs have an average ratio, which makes the gate charge detection method still a good candidate. And by reducing the gate-source voltage detection period it gives a smaller ratio, and a wide area of accuracy to detect the short-circuit, between  $Q_{G\_NTO}(t)$   $Q_{G\_HSF}(t)$ , as presented in HSF timing chart. On other words, limiting  $V_{GS}$  integration window; by starting the integration later from  $V_{GS2}$  or  $V_{GS1}$  or even  $V_{GS3}$  reduces the similar gate charge amount, therefore after integrating only the wanted gate charge the integrator will have a wider difference between the faults, Fig.III. 9, thus the difference between the ratios S in Tab.III. 4. The same can be applied for OC fault monitoring and for FUL monitoring the set of the start level should be around 80% of  $V_{Drv+}$ .



**Fig.III. 9.** Illustration of different ratios on the Gate charge characteristic for a WolfSpeed 2<sup>nd</sup> generation power transistor



**Fig.III.10.** Analytical Gate charge characteristics under different parameters variations, Standard parameters used are  $I_{Load} = 80A$ ,  $V_{DS} = 800V$ ,  $R_G = 3.6\Omega$ ,  $g_{fs} = 20.7S$ , DUT: C2M0025120

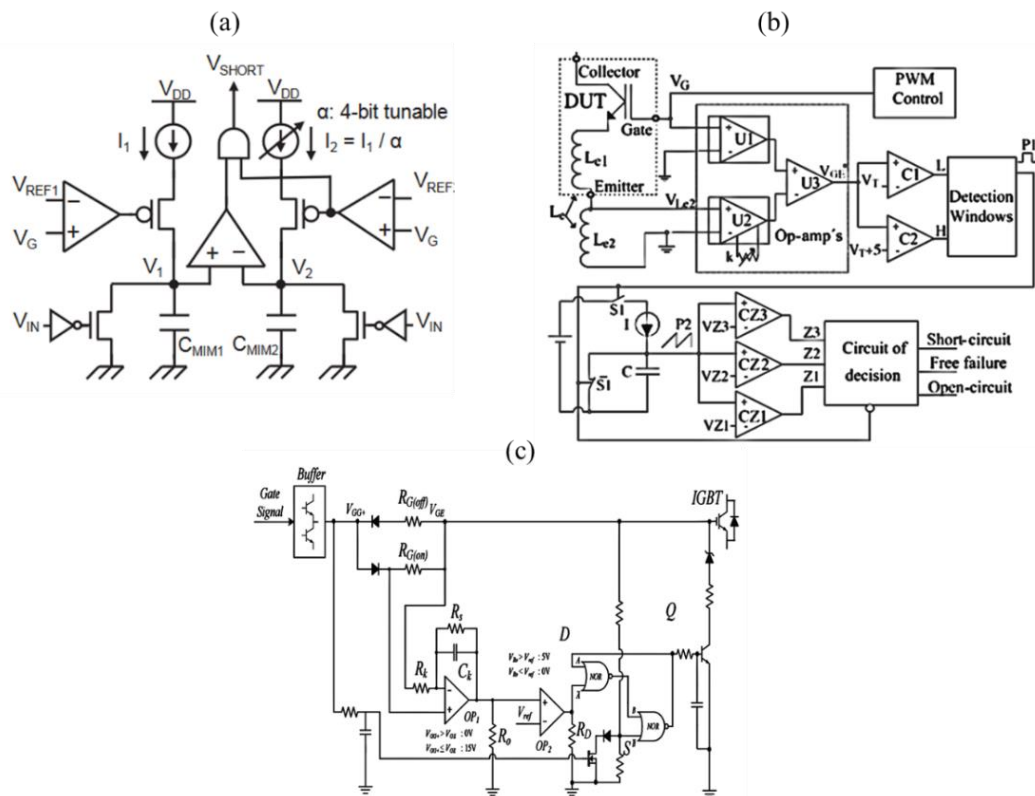
After all, to give more perspective on the robustness of the gate charge, Fig.III.10 is presented. The figure illustrates the variation effect of the main parameters of the gate charge as  $I_{LOAD}$ ,  $V_{DS}$  for the operating point of load  $R_G$  (external resistance) as user parameter, and the trans-conductance  $g_{fs}$ .

$V_{GS\_th}$  can also be subject to a strong drift for the SiC MOSFET [161] and impact the robustness of the detector. Its effect can be deduced from the study of the  $V_{Start}$  effect. The lower its value, the lower the value of the S coefficient and the higher the robustness.

Other parameters influence the gate charge as the input capacitance  $C_{iss}$  and the internal gate resistor  $R_{G\_Int}$ . As Fig.III.10 shows, with different circuit conditions, how datasheet gate charge parameters changes. Only simple mathematics is needed in getting the accurate estimations in designing a robust circuit. Therefore, the representative equations discussed above, in relation III.4 for  $Q_G$  and  $S$  in relation III.9 are introduced to Matlab. The power transistor C2M0025120D is considered in this scope of study. The standard parameters used are  $I_{Load}=80A$ ,  $V_{DS}=800V$ ,  $R_G=3.6\Omega$ ,  $g_{fs}=20.7S$ , then each parameter is varied in order to have a perspective of the parameter variation on the ratio  $S$ . The ratio  $S$  as presented in Fig.III.10 is for a  $V_{GS2}$ , where it equal to  $-5/20V$ . The variation of  $S(V_{GS})$  is slightly small, but for a defined  $V_{GS}$  (as  $V_{GS1}$  or  $V_{GS3}$ ) the range of study will be wider. Therefore, the variation of  $S(V_{GS})$  will be clearer and more defined.

The references levels ( $V_{Ref}$ ) set have a huge impact in the design as well. As explained above, under HSF, FUL or OC condition the references levels are different. And they can easily lead to a false detection with these circuit and device parameters variations.

In the literature [167], a high reference variation-tolerance schematic is proposed, Fig.III.11.(a). The idea is to introduce an adaptive threshold-time determination. The adaptation is realized by using an analog delay multiplier circuit. The method is well adapted for Si IGBTs, where the detection period is wider than SiC MOSFETs, allowing enough time for the analog circuit to adapt the determined time.



**Fig.III. 11.** Gate charge fault-detection scheme for Silicon IGBTs (a). based on adaptive threshold level [167] (b). based on the measurement and evaluation in the turn-on transient period [165] (c). Common schematic [16].

A different set of the threshold levels is presented in [165], where the fault can be evaluated from  $V_{th}$  (threshold voltage) to upper gate voltage, which can assure full evaluation of the depletion region ( $V_{DS} < V_{GS}$ ) for IGBTs, Fig.III. 11.(b). Moreover, the plateau zone of the gate voltage is almost constant when the gate voltage is 5V. Then, the threshold levels can be defined from  $V_{th}$  to  $V_{th}+5V$  in order to assure the existence of a depletion region. By doing so, it creates a detection window around the Miller plateau, therefore the detection can be assured.

The most used schematic [16] is proposed in Fig.III. 11.(c), to illustrate the difference between the other methods.

### 2.3. Proposed schematic, RC rating and trade-off

The proposed SC detecting schematic is achieved to protect SiC MOSFETs. This method is based on the measurement of the gate voltage, as presented above in Fig.III. 11.(c). The proposed study is a fruit of several analytical studies. The method is based on differential amplifier at the  $R_G$  terminals or  $R_S$  terminals (sensing resistance integrated on the gate driver,  $R_S \ll R_G + R_{G\_int}$ ). This differential amplifier will amplify the image of the gate current  $V_{in}$  that is created from the voltage across the sense resistor  $R_S$ . Thus, in order to get the gate charge, the image of the current should be integrated. With those two main blocks (Diff. Amp. followed by Integrator), one obtains the gate charge  $Q_G$ , which is then further compared with the threshold  $Q_{Ref\_HSF}$  and  $Q_{Ref\_FUL}$  levels. Before that, to ensure that the detection is at the right moment, two additional comparators with  $V_{Ref\_HSF}$  and  $V_{Ref\_FUL}$  are used to activate the monitoring. A reset option can be added in parallel to the integrator, in order to set the different  $V_{GS1}$ ,  $V_{GS2}$  or  $V_{GS3}$  start command of the integration. Each block has been studied for a better robustness and high speed detection.

The miniaturization of electronic components is an important issue in the industry. Among other things, this trend makes it possible to reduce the power consumption of systems, to offer more functionalities and to reduce the price. The gate charge method has been chosen to be integrated in a PCB level. This method was studied for Silicon IGBTs, and more recently presented under SiC MOSFETs. However, it is not yet available in commercially advanced gate-drivers. In order to pile more robustness studies about the gate charge method for SiC MOSFETs, and overcome the unclarified problematics that this method faces, this method was integrated using discrete components. By doing so, our study has an open flexibility. The main reasons why this study was integrated in a PCB level and not a CMOS level is to benchmark this exciting method, and to furthermore develop it, while having in the same time more flexibility to change the components and the parameter value at our convenience. The CMOS integration level requires more time and study, and moreover no flexibility due to the impossibility to change the layout after design and packaging.

This straightforward solution is based on a fast differential amplifier and to be referenced to the kelvin source of the power component. The main disadvantage of this method is to find fast components (Differential amplifier, integrator) that must support the large common and differential mode. It quickly becomes apparent that fast amplifiers are limited in common and



differential mode. It is then necessary to use more capacitive and therefore slower detection. This approach was only validated by simulation. In order to avoid the amplification common mode, another solution is proposed. This solution is not described in this thesis due to an ongoing industrial valorization, in order to scale-up in the TRL scale and a possible commercial use. The various components that compose the final circuits are completely integrated in SMD technology. The study of each block is described below, step by step. The typical schematic is presented in fig.III.12. Note that the analytical study depends on the adapted circuit (final circuit).

**Tab.III. 5.** Different differential amplifiers parameters.

<b>Param.</b>	<b>LT1395</b>	<b>ADA4807</b>	<b>AD8034</b>	<b>AD8512</b>
<b>BW</b>	400MHz	180MHz	80MHz	10MHz
<b>AV</b>	65db	130db	92db	107db
<b>I<sub>os</sub></b>	10 $\mu$ A	8nA	1.5pA	5pA
<b>CMRR</b>	52db	100db	100db	100db
<b>SR</b>	800V/ $\mu$ s	225V/ $\mu$ s	80V/ $\mu$ s	20V/ $\mu$ s
<b>V<sub>os</sub></b>	1mV	20 $\mu$ V	1mV	0.08mV
<b>V<sub>Supply</sub></b>	-5/5V	-5/5V	-5/5V	-5/5V
<b>R<sub>in</sub></b>	1M $\Omega$	45M $\Omega$	100M $\Omega$	-
<b>C<sub>in</sub></b>	2pF	1pF	1.7pF	11.5pF

- Differential amplifier:

The goal of the differential amplifier is to amplify the difference between two input voltages ( $V_{DrV}$ ,  $V_G$ ) but reject the common mode voltage. By doing so, the image of the gate current is created. Several differential amplifiers showed promising results, but not a high accuracy of the current image  $V_{In}$ , despite their high band-width (BW), or their high Slew Rate (SR). There is no differential amplifier which complies with the specifications (high BW, high SR, small input capacitance  $C_{in}$ , lower input offset voltage  $V_{os}$  or input bias current  $I_{os}$ ), Tab.III. 5, and can support the large common and differential voltages (CMRR Common-Mode Rejection Ratio). Small input capacitance  $C_{in}$  is required in order to be operational with low current sourced towards the circuit.

- Integrator:

The use of the integrator is to integrate the image of the gate current  $V_{In}$ . It accumulates the input quantity over a defined time to produce a representative gate charge at the output, eq.(III. 10). The time window is respectively the reference levels  $V_{Ref\_Start}$  and PWM.



The ratio  $V_{Out\_SC}/V_{Out\_NTO}$  is equal to the ratio  $S$ . The  $V_{Out}$  depends as well on the input capacitor of the power transistor and the external/internal gate resistor, by means the gate current  $i_G(t)$ , eq.(III. 14) before the Miller plateau.

$$i_G(t) = \frac{-V_{DRV}}{R_G} * e^{-\frac{t}{R_G C_{Eq}}} \quad (III. 14)$$

Eq.(III. 11) becomes Eq.(III. 16) by the merge of the equations eq.(III. 12), eq.(III. 14) and eq.(III. 15), where the gate charge appears on the equation.

$$Q_G = \int I_G * dt \quad (III. 15)$$

$$V_{Out} = \frac{R_G}{R_1 C_1} * Q_G \quad (III. 16)$$

with  $R_1 \gg R_G$

Relation (III. 16) shows that at a given  $Q_G$  and  $R_G$ , product  $R_1.C_1$  must be minimized. However,  $R_1/R_G$ ,  $C_1/C_{in\_amplifier}$  and  $C_1/C_{oss\_reset\_Tr}$  must remain high. An additional constraint corresponds to the range of the output voltage for maximum sensitivity :  $V_{Out\_NTO} \cong 5V$  (i.e.  $V_{DD}$ ) ;  $V_{Out\_SC} \cong 2.5V$  (i.e.  $V_{DD}/2$ ).

Fig.III. 13 presents a 3D plot of  $V_{Out}$  under different variation of the parameters  $C_{Eq}$ ,  $C_1$  and  $R_1$ . The plot is realized under Matlab<sup>TM</sup> by representing the equation above. The  $C_{Eq}$  is based on the input capacitance of the SiC MOSFETs transistors, which varies between 350pF to 6nF under NTO. Respecting the proportionality of the ratio of the gate charge  $S$  (example= 50%), under SC HSF the  $C_{Eq}$  should be approximately half. The output voltage range of the op-amps is 5V, which allows a choice of  $C_1$  and  $R_1$  respectively around 80pF and 1k $\Omega$ .

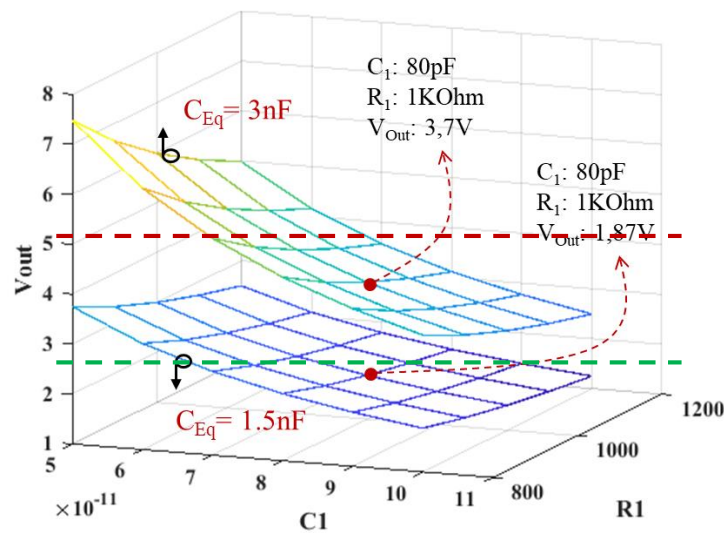
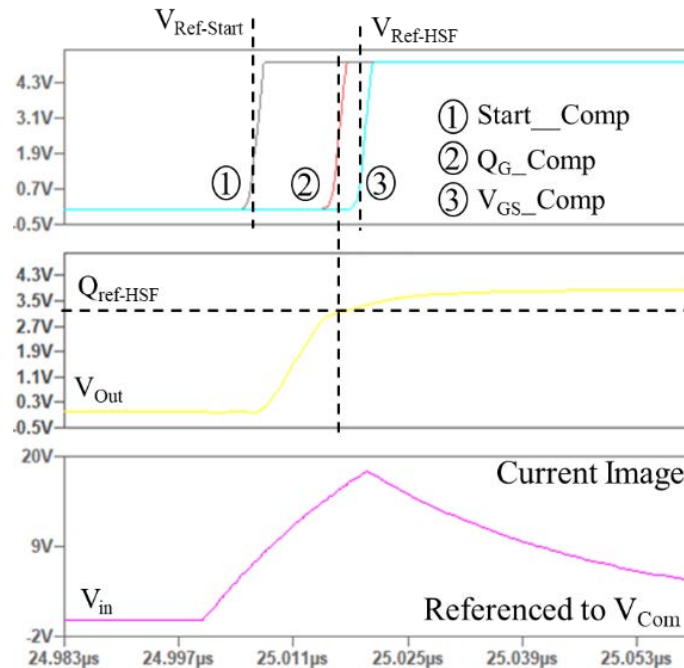


Fig.III. 13. 3D plot of  $V_{Out}$  under different variation

With these values:  $C_1/C_{in}= 40$ ;  $C_1/C_{oss}= 8$ ;  $R_1/R_G= 100$  and thus we consider that all functional and technological design constraints are respected.

With all the accumulated data, the final circuit is proposed, Fig.III. 15. Fig.III. 14 presents a simulation of the equivalent circuit using an equivalent capacitor  $C_{Eq}= 3nF$  to represent the power MOSFET. In the simulation all blocks were replaced by their references.

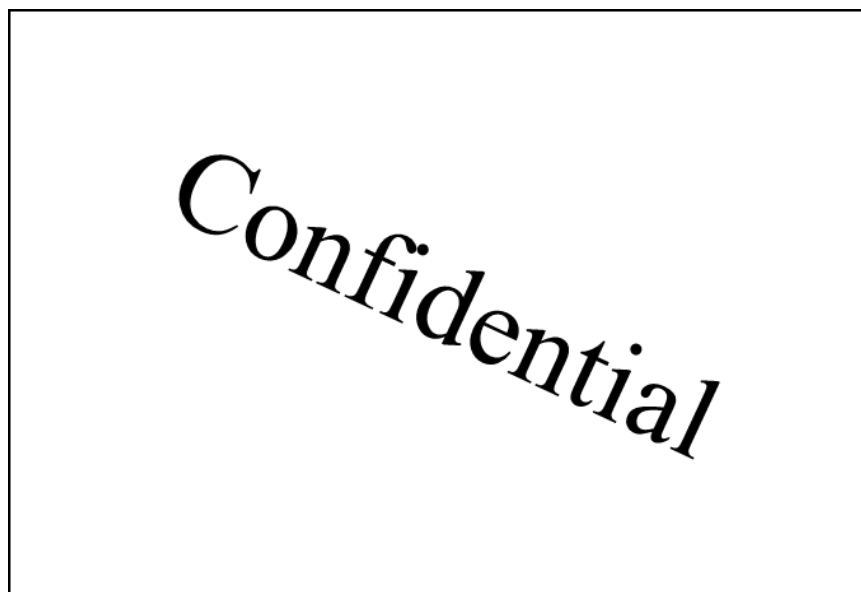


**Fig.III. 14.** Simulation waveforms under LTspice of the partial circuit, Detection logic circuit and protection is not included.

$V_{GS}$  is compared to  $V_{Ref\_HSF}$  and the Output of the integrator is compared to  $Q_{Ref\_HSF}$  as well. Both signals are compared to their respective thresholds levels, Fig.III. 14. The gate Driver has a high impedance “HZ” input, where the gate of the power device becomes floating, allowing the Soft shut down SSD to pull down the gate voltage and to sink the current. The SSD is activated after a small delay equivalent to the gate driver propagation time. This protection system allows to bypass the incoming PWM signal and to prevent a SC flowing through the output of the buffer and the NMOS transistor of the SSD. Afterwards the detection flag is sent to the centralized control to take further actions.

Classically, the centralized control can decide to restart operation for confirmation of the fault or to avoid detection error on a false fault. This restart can typically be done three times, with a time spacing of several hundred milliseconds or seconds. If the fault is confirmed, the centralized control orders the turn-off of all the transistors of the converter if no redundancy is provided. In the case of a converter with redundancy, a procedure to confirm the isolation of the fault is necessary, then the activation of the redundant circuit, the reset of the regulators and finally the restart of all the transistor control signals.

In our lab. set-up, the SC detection/protection is done at each PWM pulse. In other words, the HZ is reset once the next PWM pulse is sent.



**Fig.III. 15.** The proposed gate charge schematic. Confidential

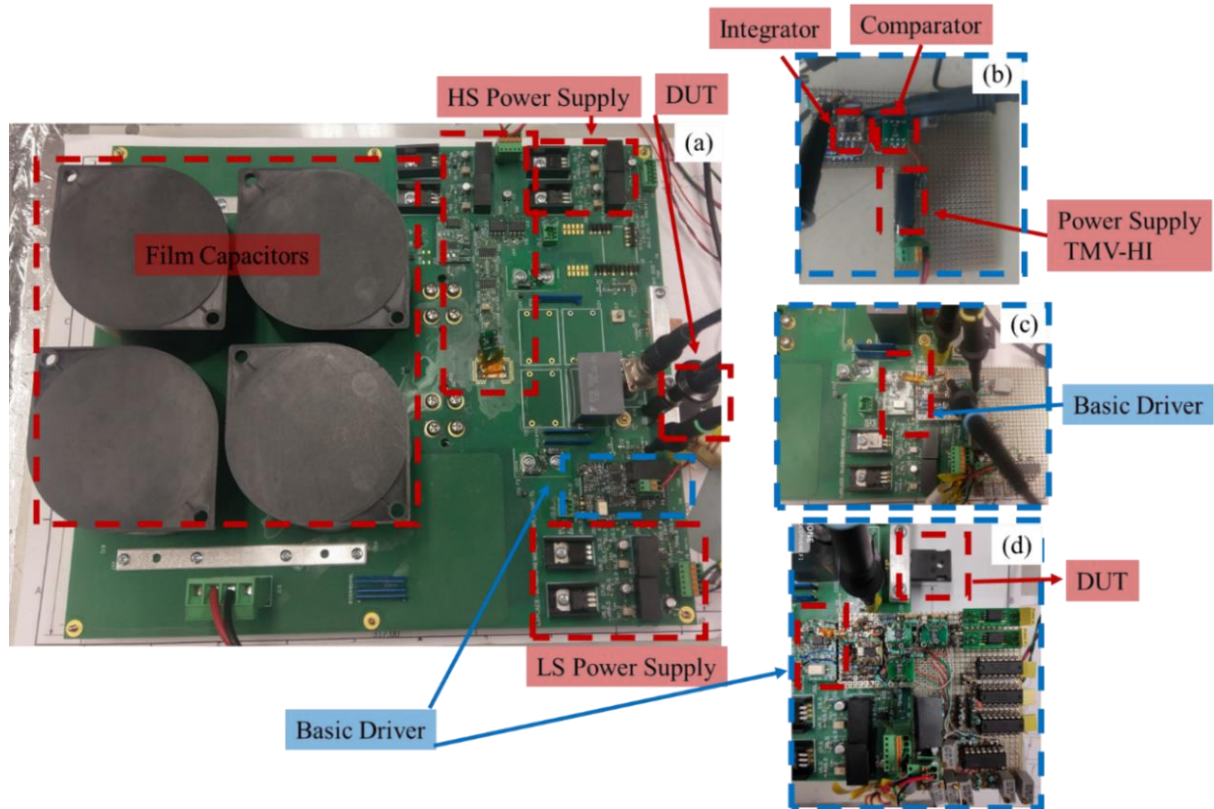
The detailed schematics is still confidential and subject to potential IP protection (figure III.15). Nonetheless, the overall approach has been publicly presented hereinbefore. The proposed study is focused on Hard Switch Fault, to monitor the gate charge and to detect as fast as possible regarding different parameters. The method is experimentally validated below. For the other faults; Fault Under Load or Open Circuit; as mentioned above their gate charge have unique behavior, that can be detected as well with different threshold level set.

## **2.4.Experimental results**

### **2.4.1. V1.A Discrete components prototype**

The first prototype derived from the study above, will be titled V1.A. The V1 stands for the first version of the motherboard presented in chap.II. “A”, in the other hand, stands for the 1<sup>st</sup> prototype of the gate charge monitoring method. The first prototype is validated fragment by fragment, only using discrete components. Fig.III. 16 presents the different evolution of the circuit from (b) to (d) as well as the motherboard used to validate the circuit under real components, (a).





**Fig.III. 16.** (a). Motherboard V1 presented in Chap.II. (b). Demo prototype of (V1.A) of gate charge detection method under  $R_G$  and  $C_{Eq}$ . (c). Evolution of the demo prototype under HV and DUT. (d). Complete V1.A prototype using discrete components.

At first, only the integrator and comparator were under test, as shown in Fig.III. 16. The power transistor was replaced by an equivalent capacitor  $C_{Eq}$  and the gate resistor was kept the same  $R_G$ . Fig.III. 17 shows the output of the integrator and the equivalent current  $I_G$ . The output of the integrator is around 1.4V for a  $C_{Eq} = 3\text{nF}$ ,  $R_G = 10\Omega$  and  $C_1 = 82\text{pF}$ .

At second, the circuit was plugged in the motherboard, to be tested under NTO and HSF. The test conditions under NTO are on the low side a 1.2kV-80m $\Omega$ , C2M0080120D SiC MOSFET transistor, and on the high side a SiC 600V SDB (schottky barrier diode) with a load coreless inductor of 270 $\mu\text{H}$ . A copper short-strap across the high side is used for the SC-HSF mode. For both operations the parameters are  $C_{iss} = 1.13\text{nF}$  (C2M0080120D input capacitance),  $R_G = 10\Omega$ , and  $C_1 = 80\text{pF} +$  the parallel  $C_{oss}$  of the reset transistor of 10pF. The circuit was validated under different  $V_{Bus}$  values between (0-400V). In Fig.III. 18 the experiment was under  $V_{Bus} = 400\text{V}$ . Under NTO the amount of the gate charge is higher than under SC, which activates the  $Q_G$  comparator. The output of the integrator  $V_{Out}$  or  $Q_{G\_NTO}$ ,  $Q_{G\_HSF}$  as mentioned in the Fig.III. 18 respects the analytical study shown above, as well as the ratio  $S$ , with  $Q_{G\_NTO} = 4.3\text{V}$  and  $Q_{G\_SC} = 2.2\text{V}$ . This quantity ratio is approximately 50% for  $V_{GS} = -5/20\text{V}$ . For a selective detection between NTO vs SC and a better ratio  $S$ , the integration can be controlled by adding another threshold level to start the integration. Unfortunately, this reduces the integrator output level, gives less robust range for other power components and a trade-off must be reached.

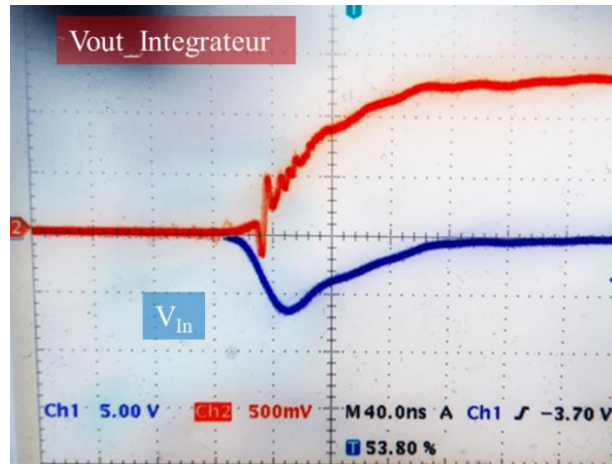


Fig.III. 17. Experimental waveforms under equivalent capacitor

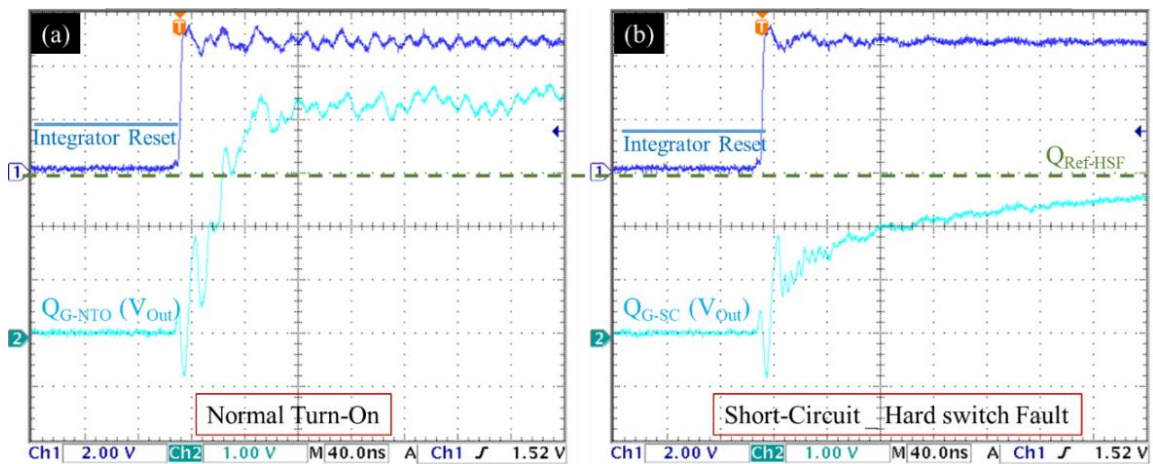


Fig.III. 18. Experimental waveforms of the beginning of the integration, under NTO and HSF:  
 1.2kV-80m $\Omega$ , C2M0080120D SiC MOSFET @ $V_{DS} = 400V$ ,  $V_{GS} = -5/20V$ ,  
 $R_G = 10\Omega$ , and  $C_1 = 80pF$ ,  $R_1 = 1K\Omega$

At third, the rest of the detection circuit is added, comparators for each signal ( $Q_G$ ,  $V_{GS}$ ) and digital blocks to process the flag. As well the protection circuit. The circuit was validated under the same operational parameters listed above. Fig.III. 19 presents a zoom on the complete prototype V1.A.

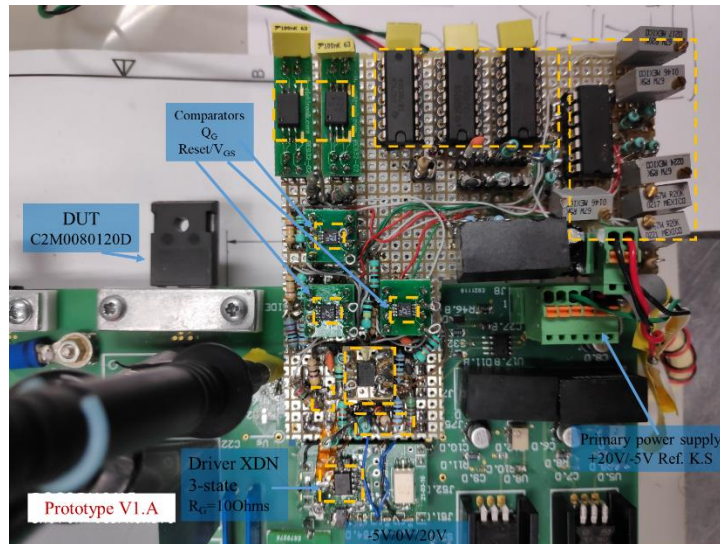


Fig.III. 19. Zoom on the complete prototype V1.A

Fig.III. 20 presents oscilloscope waveforms under NTO, gate and drain NTO waveforms are presented in Fig.III. 20. (a); and digital outputs are presented in Fig.III. 20.(b) including PWM and the detection flag. Under NTO the amount of the gate charge is higher than under SC, which activate  $Q_G$  comparator, as shown in Fig.III. 20. (b), this activation will be scanned at the arrival of the  $V_{GS}$  comparator, therefore, the flag remains low. (propagation time of the comparator is 4.5ns)

On the other hand, under SC-HSF; Fig.III. 21. (a) shows the short-circuit effect (no drain-source  $dv/dt$  or Miller plateau) on the drain and gate waveforms. The circuit is under SC, hence the amount of the gate charge is lower than NTO condition, the  $Q_G$  comparator remains low, which at the arrival of the  $V_{GS}$  comparator activate the short-circuit detection flag, Fig.III. 21. (b).

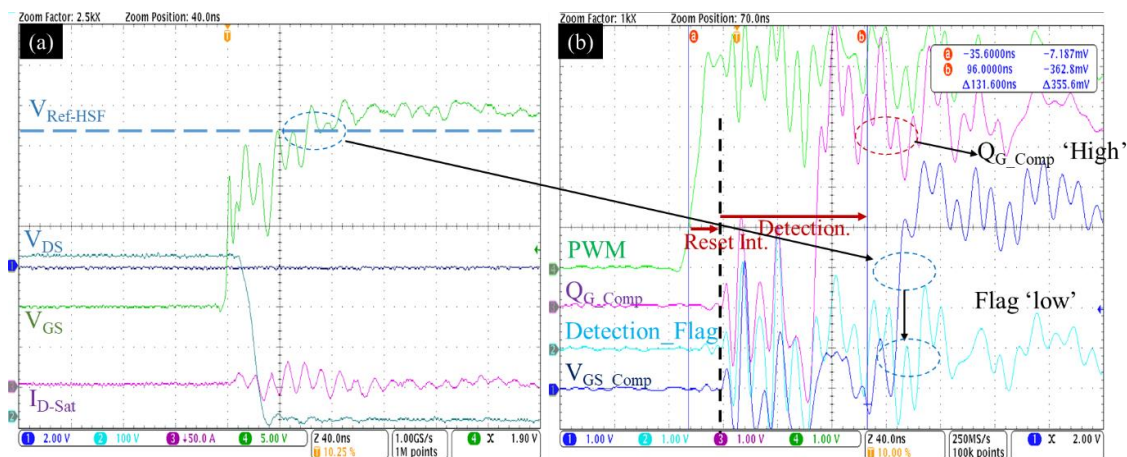
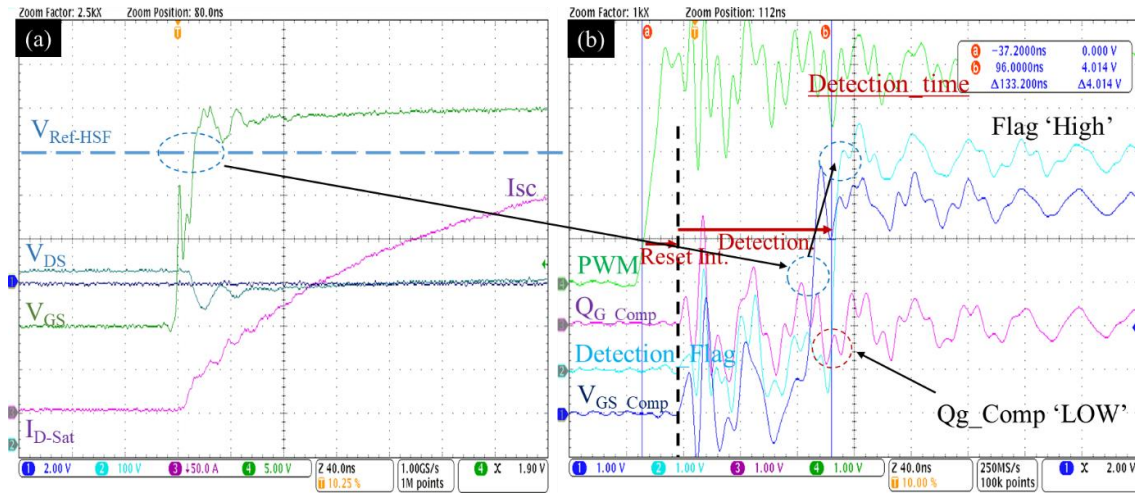


Fig.III. 20. Oscilloscope waveforms under NTO (Prototype V1.A)





**Fig.III. 21.** Oscilloscope waveforms under SC-HSF (Prototype V1.A) 1.2kV-80mΩ, C2M0080120D SiC MOSFET @ $V_{DS}= 400V$ ,  $V_{GS}= -5/20V$ ,  $R_G= 10\Omega$ , and  $C_1= 80pF$ ,  $R_1= 1K\Omega$ ,

The detection flag has been activated after 133ns including the buffer propagation time (10 ns). The detection time does not depend only on how fast the system is, the detection time depends on the value of  $R_G$ , the input capacitance of the power device, slew rate  $dV_{GS}/dt$  and how low the reference level is defined ( $>V_{GS\_M}$ ) and other parameters influence. Then, for a relative evaluation of the performance of this detector, it would therefore be useful to normalize this delay value with the apparent time constant in SC mode, in order to have a performance criterion intrinsic to the detection method.

In our lab. set-up, the slew rate between NTO vs SC changes as presented in Fig.III. 20 and Fig.III. 21, the  $V_{GS}$  comparator under NTO arrives after SC, which is a positive thing to detect faster. Same as the reference levels, the threshold gate level was defined at a robust level 18V, with a lower level the detection will be earlier but with a trade-off on the SNR.

Note that in this prototype, the waveforms are measured with probes, which bring back oscillations of which only a part is really present on the circuit. These oscillations may appear to be important even though their amplitude is much lower than the switching thresholds and the values of supply range.

- **Protection of the device:**

After the detection of the fault, the SiC MOSFET must be turned off safely, to stop  $I_{DS}$  from increasing and to avoid a dangerous over-voltage. Therefore, to protect the circuit safely, a soft shut down SSD system is included in the designed PCB, 1<sup>st</sup> prototype. If the protection is not well designed it can lead to breakdown voltage due to high negative  $dI_{DS}/dt$  through the total stray inductance, the protection should be mandatory soft to prevent this phenomenon.

After activation of the D flip-flop (Detection flag), the driver IXDN614 output is turned under high impedance (HZ), to avoid being short circuited by the SSD circuit. Then, after a delay equivalent to the driver propagation time (50ns), the SSD is activated, including a serial resistance  $R_{SSD}= 75\Omega$ , to turn-off softly the power MOSFET through discharging its gate input capacitance. The shut-down is around 500ns giving only an overvoltage of 50V, which can be

reduced or increased regarding the  $R_{SSD}$ , depending on the acceptance level of the overvoltage at the drain-source MOSFET terminals: The SiC technology gives much higher avalanche levels than the Si technology, at the same voltage rating and a shorter SSD effect could be used. In this case, it has been chosen that the power MOSFET had to be blocked with a lower dynamic range than in nominal switching in order to avoid any risk of avalanche at the DUT due to the high saturation current present.

Fig.III. 22 presents the waveforms of the device under short-circuit, including protection. After the detection flag and the buffer is placed under HZ and the SSD is activated, the  $V_{GS}$  starts to softly decrease, limiting  $I_{DS}$  to go higher. The  $V_{GS}$  comparator goes back to low but the flag remains high until the PWM of the buffer goes low, allowing the system to detect at the next PWM pulse.

It is important to note that with such a fast protection, the fault current is limited to 175A against nearly 290A without any protection, Fig.III. 23. In such a short time and at such a low current value, even less than the saturation current of the device, the dynamic temperature of the chip remains lower than the melting temperature of the aluminum to metal of the die, which would allow a large number of repeated short-circuits without ageing effect [60]. Finally, it is to be noted that such a fast detection is quite competitive with a detection that would be obtained by a special chip with an integrated sense-current.

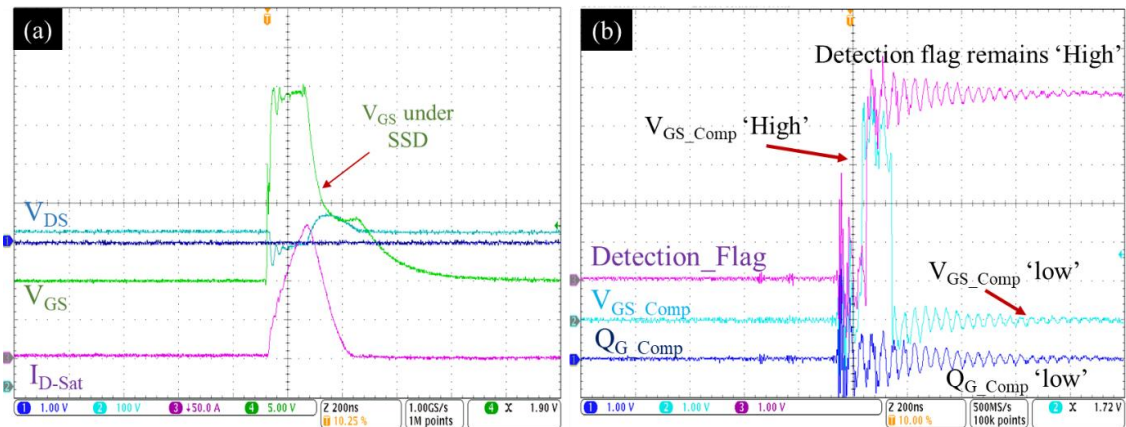


Fig.III. 22. Oscilloscope waveforms, Circuit under SSD protection (Prototype V1.A) under 400V

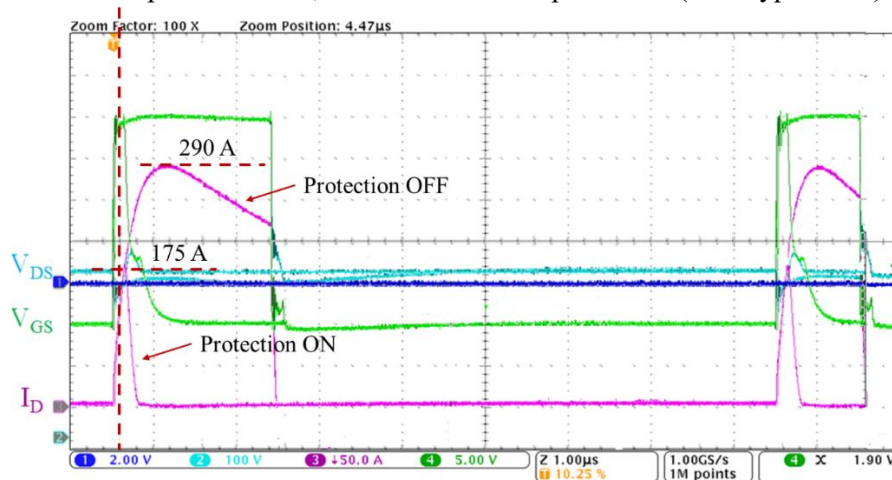


Fig.III. 23. Oscilloscope waveforms, Circuit under SSD protection and without protection

### 2.4.2. V1.b SMD prototype

The initial prototype V1.a showed promising results and accurate measures. Therefore, a better version is designed and finalized, Fig.III. 24. The internal signals and the expected behavior is well developed in the section above. In this section, the study will be focused more on the robustness of the method. Therefore, two DUT are used with different parameters, C2M0080120 & C3M0065090, covering a wide range of components, Tab.III. 6. As demonstrated in the section above:

- Due to the power supply of the driver of each generation  $V_{Ref}$  should adapt for each generation G2 and G3, respectively 3.3V and 2.7V.
- Moreover, due to different input capacitance  $C_{iss}$  of each power component  $Q_{Ref}$  should adapt for each component.

Tab.III. 6. Different main parameters for both DUT

Power component	C2M0080120	C3M0065090
$V_{Drv\_Supply}$	-5/20V	-4/15V
$R_{G\_Ext}/R_{G\_Int}$	10/3.9 $\Omega$	10/3.5 $\Omega$
$C_{iss}$	1.13nF Min @1kV	0.76nF Min @600V
$C_{rss}$	7.5pF min @1kV	5pF Min @600V
$V_{Ref}$	3.3V ( $V_{GS\_th}$ 2.4-2.9V)	2.7V ( $V_{GS\_th}$ 1.6-2.1V)
$Q_{Ref}$	3V (71nC max @ 800V-20A)	1.7V (35nC max @ 400V-20A)

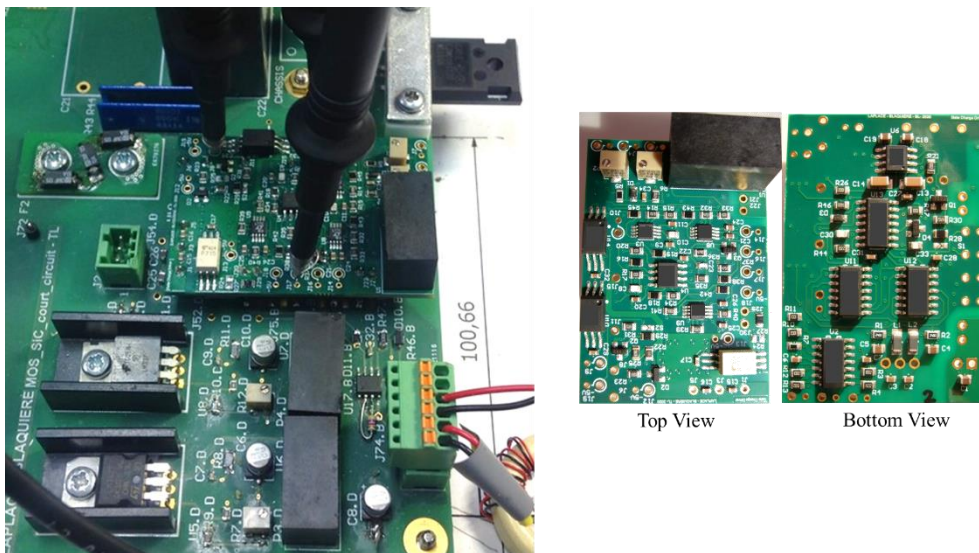


Fig.III. 24. View of V1.b prototype

Both  $V_{GS}$  are represented in Fig.III. 25.  $V_{GS}$  is compared with a reference level  $V_{Ref}$  higher than the Miller plateau. Thanks to the circuitry behind it, clear waveforms are presented between both generations illustrating the reference levels set, Fig.III. 26. As the one can see the presence of Miller Plateau under NTO is visible, where under SC-HSF is not. The set of the reference



levels is defined high for better robustness and safety margin, both references can be set lower as close as to the Miller Plateau.

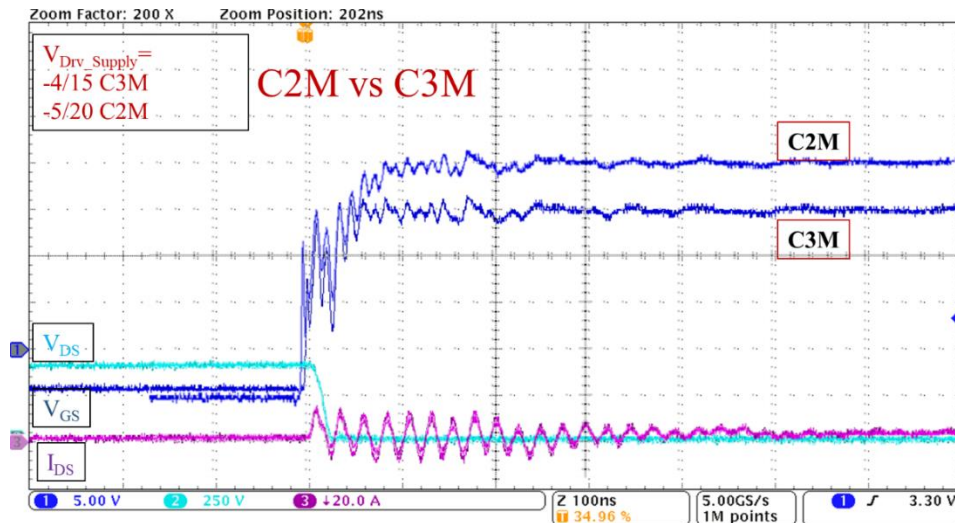


Fig.III. 25. Experimental waveforms for each DUT @400v and  $R_{g\_Ext} = 10\Omega$ .

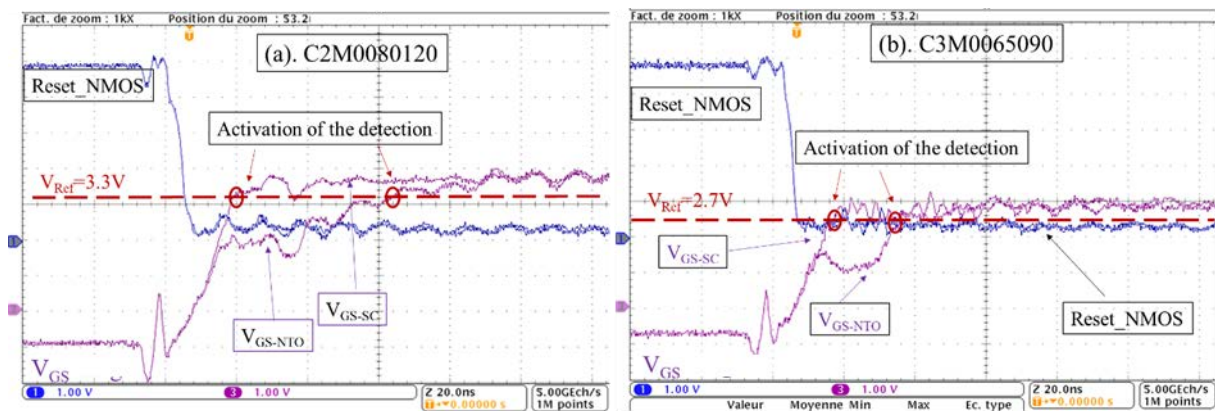
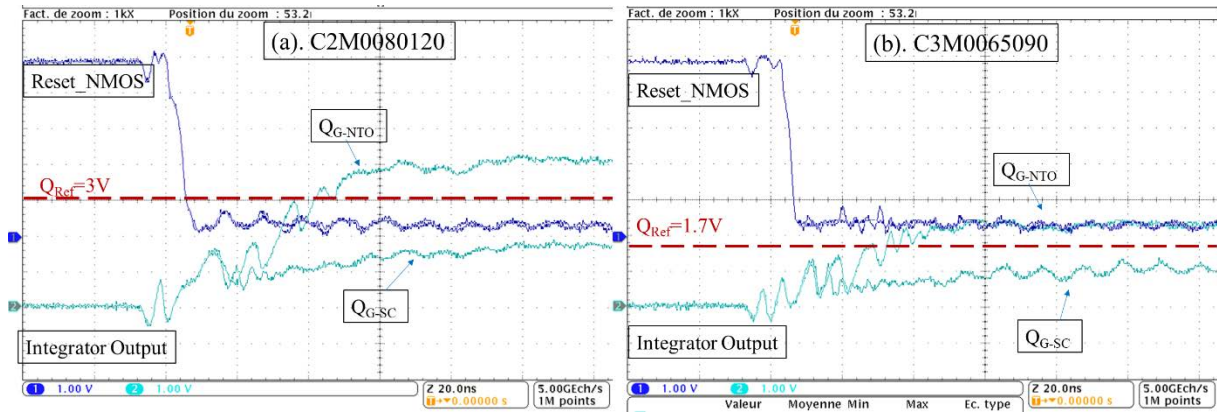


Fig.III. 26. Oscilloscope waveforms presenting  $V_{GS}$  for both DUT. (a).C2M0080120D (b).C3M0065090D @400V &  $R_{g\_Ext} = 10\Omega$

On the other hand, Fig.III. 27 presents the gate charge waveforms under both DUT. The gate charge waveform is the essential one, where the difference between NTO and SC-HSF is detectable. ( $V_{GS}$  affect the speed of the detection and trigger the detection.). As the one can see, the gate charge is proportional to the input of the power device, the smaller the capacitor, the lower the gate charge is. The reset of the integrator causes a selectivity in the integration, therefore there is a visible period in the waveforms in the begging, where the integration is off. From Fig.III. 27, the immunity band  $IB$  is equal  $|Q_{Ref}-Q_G|/Q_{Ref}$ , presented in detail in Tab.III. 7. The ratio  $S$  is presented as well, and compared with the gate charge ( $C$ ) from the datasheet. The difference between the ratio from the datasheet and the measured ratio in voltage (the output of the integrator), is due to the reset added to the integrator to reduce the stress in the beginning of the integration. All the data seems to converge to the pre-study of the method.

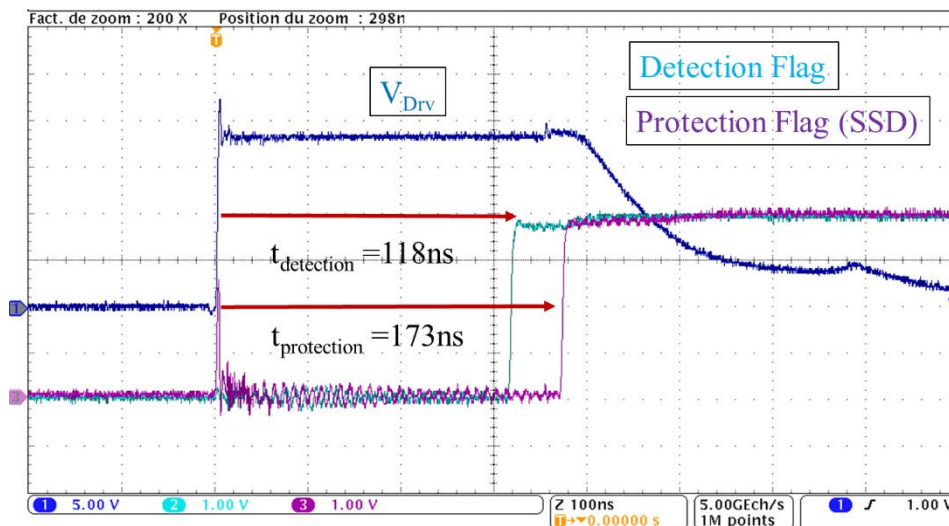


**Fig.III. 27.** Oscilloscope waveforms presenting  $Q_G$  (the integrator output in Voltage) for both DUT. (a).C2M0080120D (b).C3M0065090D @400V &  $R_{g\_Ext}= 10\Omega$

**Tab.III. 7.** Gate charge Immunity Band and Ratio S

Component	C2M0080120D	C3M0065090D
$Q_{G\_NTO}$	4.2V	2.3V
$Q_{G\_SC\_HSF}$	1.8V	1V
$Q_{Ref}$	3V	1.7V
$IB =  Q_{Ref}-Q_G /Q_{Ref}$	NTO	0.4
	SC	0.4
$S\% = Q_{G\_SC\_HSF}/Q_{G\_NTO}$ (V/V)	43%	42%
$S_{DS}\%$ (nC/nC)	34/71 => 48%	17.5/35 => 50%

Last and not least is the detection and protection time, few nanoseconds were gained from the previous prototype in the detection time, 118ns vs 133ns. And the protection time remains the same 50ns, which makes it in total 173ns, as Fig.III. 28 illustrate.



**Fig.III. 28.** Detection and protection flags with their respective time.

The high speed detection allows safety turned off at a current level well below the saturation current of the channel. Indeed, the turn-off is done here at 175A while the saturation current is

290A. The SSD could therefore be accelerated in order to further reduce the energy stress at turn-off detection for the SiC MOSFET and to preserve its capability of endurance to the short-circuit cycles that the device could have to undergo throughout its life in accidental conditions of use. In order to fully cover the robustness of this detection method, the circuit is validated under different bus voltages (50, 150, 250, 400V) which is lower than the typical 1.2kV (or 0.9kV) operational voltage, which makes the detection between NTO vs SC critical, Fig.III. 29. The one can see that with the final prototype the drain SC current is lower and stopped earlier than the previous prototype. The current is limited around 130A. Fig.III. 30 presents both DUT under protection at 600V, protection is assured.

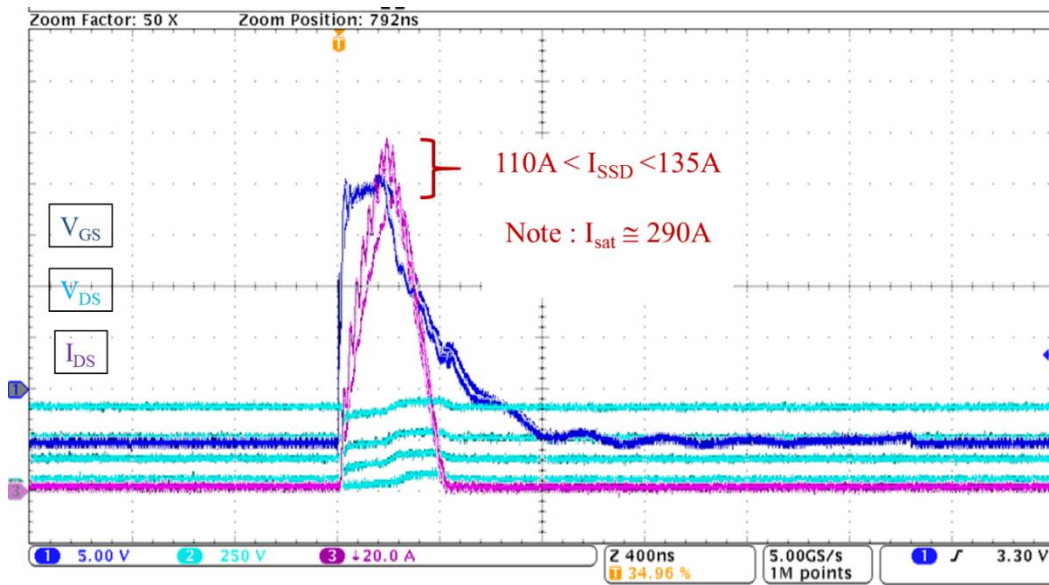


Fig.III. 29. DUT under protection for different  $V_{Bus} \in [50,150,250,400V]$ , C2M0080120 DUT, @ $R_{g\_ext}=10\Omega$ .

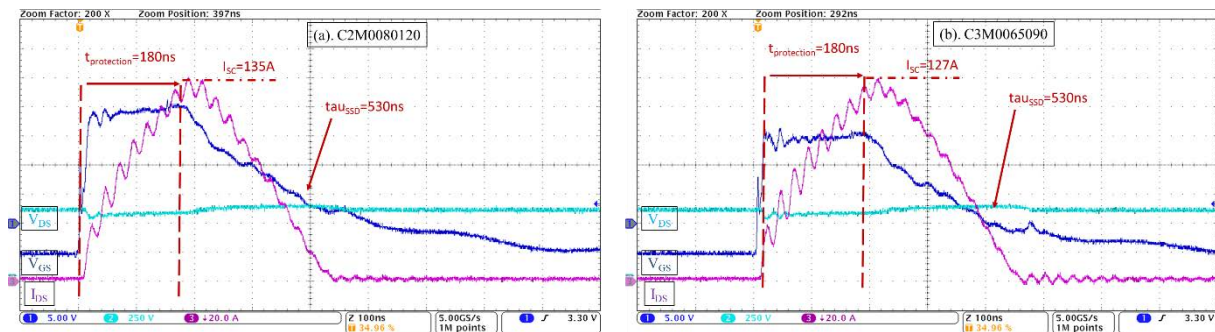


Fig.III. 30. Both DUT under protection @600V and  $R_{G\_Ext}=10\Omega$

### 3. Gate Derivation Monitoring

An in-depth discussion and validation of the gate charge method was presented above. In this section a second method is proposed to stack an additional method and to fill the void that exists among detection methods. The parameters and variables changes under SC and normal turn-on NTO helped to propose novel fast methods integrated in the gate driver. The active gate driver (AGD) is designed on purpose to detect the SC and to protect SiC MOSFETs. The

second method consists of the reconstruction of the  $dV_{GS}/dt$  by means of a capacitive current sensing to provide the  $V_{GS}$  derivation combined with the  $V_{GS}$  monitoring. In order to do so, two original detection approaches are integrated: the occurrence (or not) of the Miller plateau, and the slope differences at the gate voltage, between normal operation and SC events, which offer different solutions and better performances than the prior art. These SC detection techniques are based on low voltage signals available in the designed gate driver. As the gate charge does serve as benchmark, this method (gate derivation) is chosen to be integrated in a CMOS level. Since this method is based on a sensing capacitor, noises will be high under discrete integration. On the other hand, using CMOS integration, will help us to further reduce the detection time.

### 3.1. Proposed schematic & review of the method

The previous method based on the gate-current integration over the gate-voltage range requires a sufficiently low S-factor and accurate threshold set of the gate charge signal. The previous method has been integrated and validated on a PCB scale, where this other proposed method is now integrated in a CMOS level. The following methods provide more direct quasi-instantaneous detection without the need for the gate charge method. The impact of the capacitance  $C_{GD}$  on the switching behavior is also demonstrated for a new detection method based on monitoring the quasi-derivation of  $V_{GS}$ . There are three important time intervals on the behavior of  $V_{GS}$ , as explained above. The first one has a slope of  $1/C_{iss\_Min}$ , followed by the Miller plateau, where  $C_{GD}$  is involved, and the last one has a slope of  $1/C_{iss\_Max}$ . Using this alteration of slopes, a significant impact appears on their time derivatives.

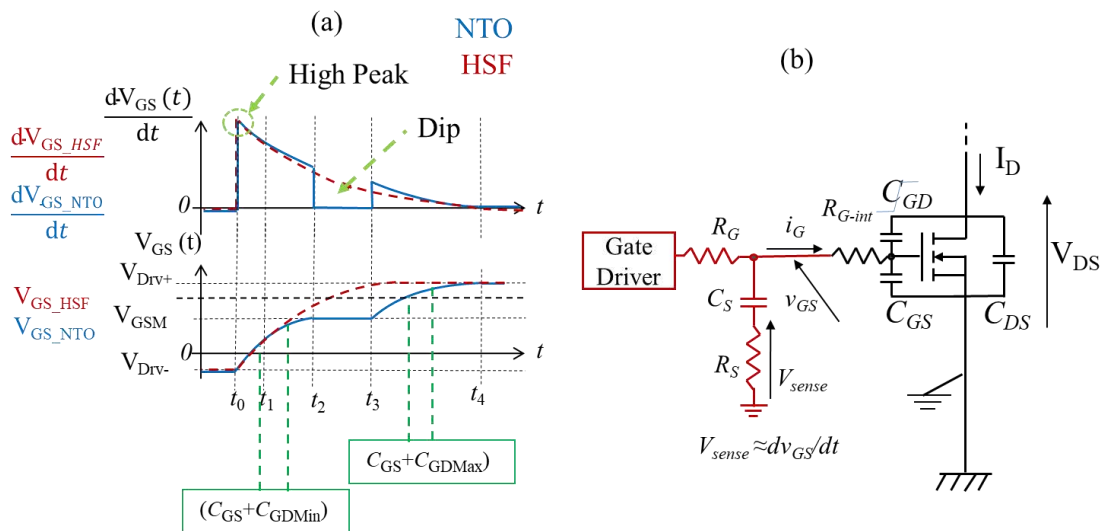


Fig.III. 31. (a).  $dV_{GS}/dt$  characteristics under “NTO” and “HSF” (b). Derivative circuit

Fig.III. 31 shows the  $dV_{GS}/dt$  signal behavior under NTO and SC-HSF conditions, where two distinctive changes of slope can be observed. During the time interval  $[t_0, t_2]$ ,  $dV_{GS}/dt$  signal presents a high peak “ $1/C_{iss\_Min} > 1/C_{iss\_Max}$ ”, followed by a decrease until reaching a dip presenting the plateau period  $[t_2, t_3]$ . A smaller peak occurs at  $t_3$  to present  $1/C_{iss\_Max}$ . The  $dV_{GS}/dt$  signal under SC-HSF is reasonably straight forward, where there is only  $1/C_{iss\_Min}$  as a slope for  $V_{GS}$  signal, from  $t_0$  to  $t_4$   $dV_{GS}/dt$  is the derivation of the slope  $1/C_{iss\_Min}$ , the dip or the



smaller peak is not present. There are two different ways to analyze the derivation signal. The first approach is the slope approach, based on the differences between the slope before and after the Miller plateau under NTO; or the unchanged slope under SC. The second one is the dip approach, where the presence or non-presence of the Miller plateau is detected. The proposed method is based on the derivation method. As known, the current that runs through a capacitor is given by the voltage-current relationship eq.(III. 17), where  $C_s$  is the sensing capacitor in parallel with the gate of the power device. Using this voltage-current relationship gives the time derivative of  $V_{GS}$ .

$$V_{GS} = V_{Cs} + R_s * i_{Cs}$$

$$V_{GS} = V_{Cs} + R_s * C_s * \frac{dV_{Cs}}{dt}$$

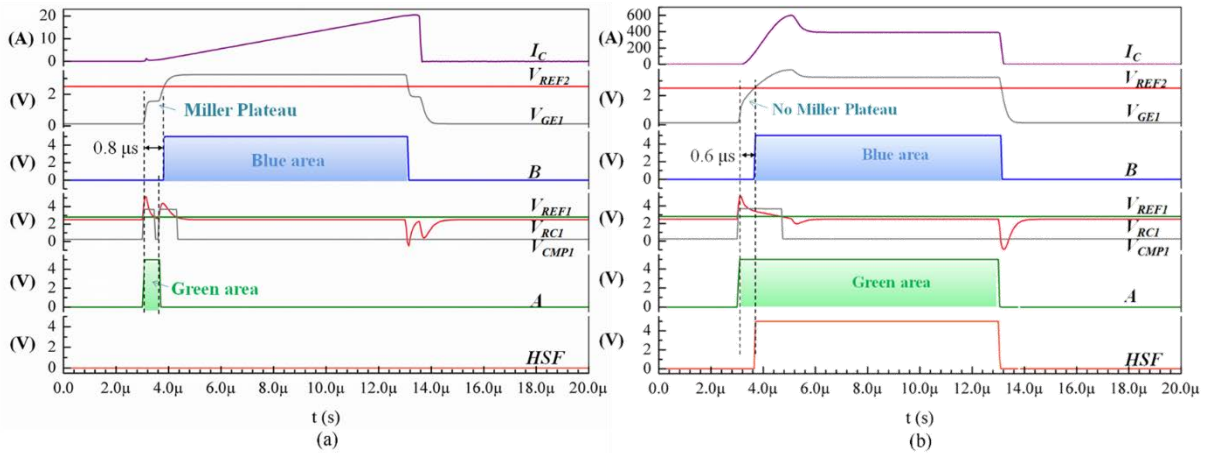
With 
$$V_{Sense} = R_s * i_{Cs}$$

$$V_{Sense} = R_s * C_s * \frac{dV_{Cs}}{dt}$$

If  $R_s * i_{Cs} \ll V_{Cs}$  is verified then  $V_{Cs} \cong V_{GS}$

Then 
$$V_{Sense} \cong R_s * C_s * \frac{dV_{GS}}{dt}$$

$$\frac{dV_{GS}(t)}{dt} = \frac{i_{Cs}(t)}{C_s} \tag{III. 17}$$



**Fig.III. 32.** Simulated waveforms of the gate voltage pattern analyzer for the HSF [169]. **(a).** IGBT normally turn-on condition. **(b).** IGBT HSF turn-on condition ( $V_{DC}= 250V$ ,  $V_{G-Supply}= 13V$ ,  $R_G= 50\Omega$ ,  $L_{SC}= 0.5\mu H$ )

Other approaches are studied on the detection of the plateau as presented in [169] but on IGBT technology only and using a SMD-PCB integration set-up . As shown in [169], the detection is based on the detection of the Miller plateau, Fig.III. 32. An RC filter is introduced after the  $V_{Sense}$  voltage to generate the  $V_{RC1}$  signal, which is similar to the topology studied in

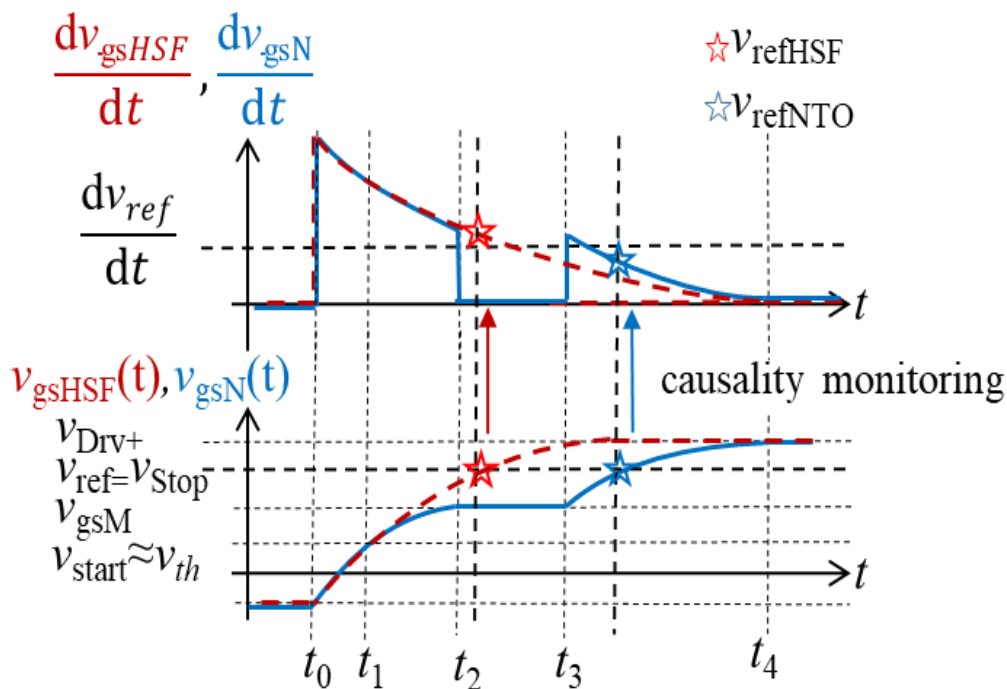


this thesis. The signal after threshold set undergoes a dip in the presence of the Miller plateau, Fig.III. 32.(a).

### 3.1.1. Slope approach

From this characteristic, two detection approaches can be concluded. The first one is the slope approach based on the changes of the  $dV_{GS}/dt$  waveforms, where a threshold level  $dV_{Ref}/dt$  is needed to be fixed for the  $dV/dt$  signal to distinguish between  $1/C_{iss\_Max}$  for NTO and  $1/C_{iss\_Min}$  for HSF at the threshold level  $V_{GS} = V_{Ref}$ . This threshold level  $V_{Ref}$  is used to activate the readout of the comparison, as well as the SC detection, seen in Tab.III. 8. Fig.III. 33 shows the importance of the  $V_{Ref}$  level (represented by stars), while removing any direct dependency with time if a constant function of threshold set is used. On the other hand, there is a direct dependency with  $R_G$ ,  $C_{iss}$ ,  $T^\circ$ ,  $V_{Drv+}$ ,  $SR$ , ... Indeed, the  $V_{Ref}$  detection is indirectly reflected in different times for NTO and HSF. Therefore, the difference between the slopes define the NTO or HSF detections.

Special function of thresholding, in theory, would allow to gain in robustness by obtaining a first comparison point with a higher slope (red color star in Fig.III. 25) and a second comparison point with a lower slope (blue color star in Fig.III. 25.). Such a function would be monotonically increasing in order to give the greatest possible amplitude difference in the slope values. But this one remains complex to generate and then to adjust in practice. In a first integrated validation approach, only a constant threshold function is considered in the rest of the study.



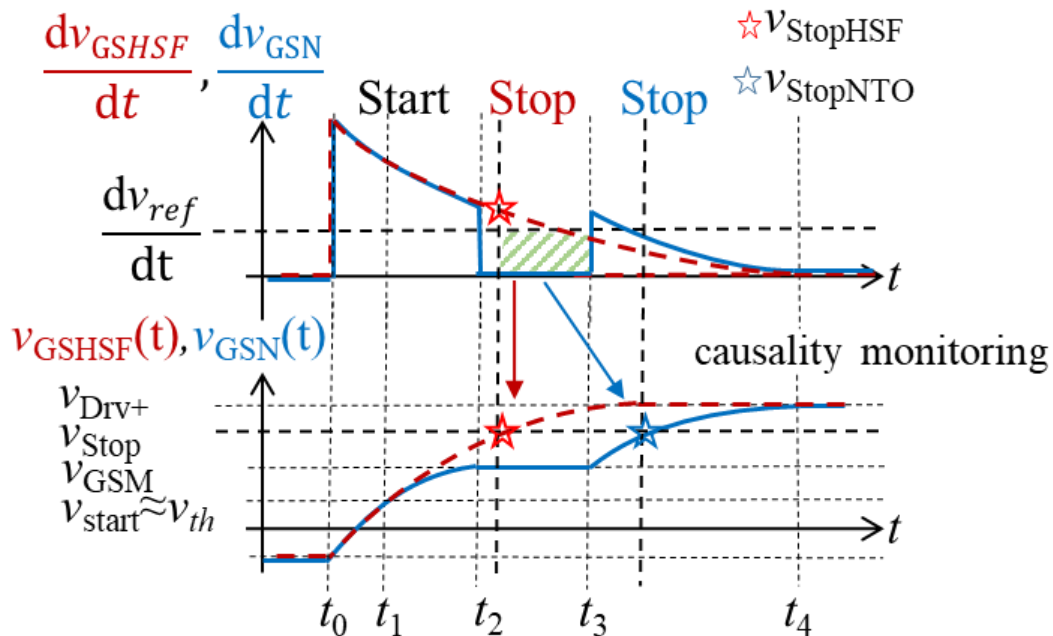
**Fig.III. 33.**  $dV_{GS}/dt$  characteristics under “NTO” and “HSF”, Slope detection approach. Stars represent the levels obtained for the same gate voltage,  $V_{GS} = V_{Ref} = V_{Stop}$ , with  $V_{Ref} > V_{GS\_M}$  for the slope approach

**Tab.III. 8.** 2D diagnosis for HSF with  $V_{GS}$  slope approach.

Comparator	Output diagnosis
If $V_{GS} = V_{Ref}$ AND $dV_{GS}/dt < dV_{Ref}/dt$ then	NTO
If $V_{GS} = V_{Ref}$ AND $dV_{GS}/dt > dV_{Ref}/dt$ then	HSF

### 3.1.2. Dip approach

The second detection approach, the dip approach is based on the detection of the dip in the derivation signal, the presence of the Miller plateau. A threshold level  $dV_{Ref}/dt$  is also needed. Under SC conditions, the two approaches do not have any difference detecting at  $V_{Ref}$  the presence of  $1/C_{iss\_Min}$  or a non-presence of a dip. The approach is to detect the signal above  $dV_{Ref}/dt$  before reaching  $V_{Ref}$ , as illustrated in Tab.III. 8 and Tab.III. 9. In contrast, under NTO conditions, the two approaches are almost similar, both of them being based on the detection of the signal below  $dV_{Ref}/dt$ . The only difference between the detection is to detect the dip before  $V_{GS} > V_{Ref}$  or to detect  $1/C_{iss\_Max}$  slope at  $V_{GS} = V_{Ref}$ , Fig.III. 34.



**Fig.III. 34.**  $dV_{GS}/dt$  characteristics under “NTO” and “HSF”, Dip approach. Stars represent the levels obtained for the same gate voltage,  $V_{GS} = V_{Stop}$ , for the dip approach  $V_{GS} = V_{Stop}$  is not a reference level for comparison.

**Tab.III. 9.** 2D diagnosis for HSF with dip approach.

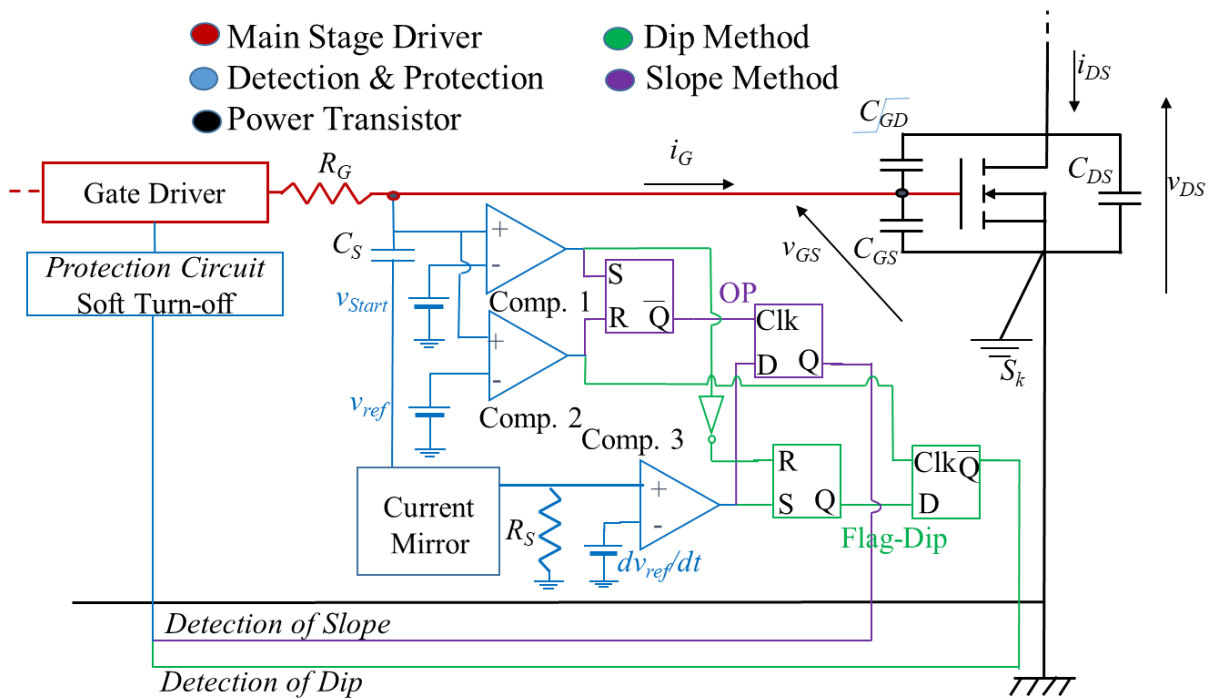
Comparator	Output diagnosis
If $dV_{GS}/dt < dV_{Ref}/dt$ AND $V_{GS} < V_{Ref}$ then	NTO
If $dV_{GS}/dt > dV_{Ref}/dt$ AND $V_{GS} > V_{Ref}$ then	HSF

Both approaches can be accurate and robust because they are based on 2D detection  $dV_{GS}/dt$  combined with  $V_{GS}$ . The second approach may be faster in NTO operation, where dip detection is before reaching  $V_{Ref}$ . More importantly, the second approach (dip approach) should present a higher SNR than the slope method thanks to the high signal amplitude detection.

This one, dip approach, may help the robustness of the detection by allowing a lower  $dV_{Ref}/dt$ ; consequently, a wider discrimination range for a SC detection is offered, avoiding the small critical zone whenever  $V_{GS\_NTO}$  and  $V_{GS\_HSF}$  have similar values. The different threshold voltages must be defined from key parameters extracted from the datasheet, operating conditions and experimental results. Threshold voltages must take into consideration the variation of  $R_G$ ,  $C_{iss}$ ,  $T^\circ$  and  $V_{Drvt+}$ , ... these variations can affect the level of the miller plateau, the slew rate, and the range of detection. Therefore, these reference levels must be well defined.

### 3.2. Detection circuit based on derivation monitoring and simulation behavior

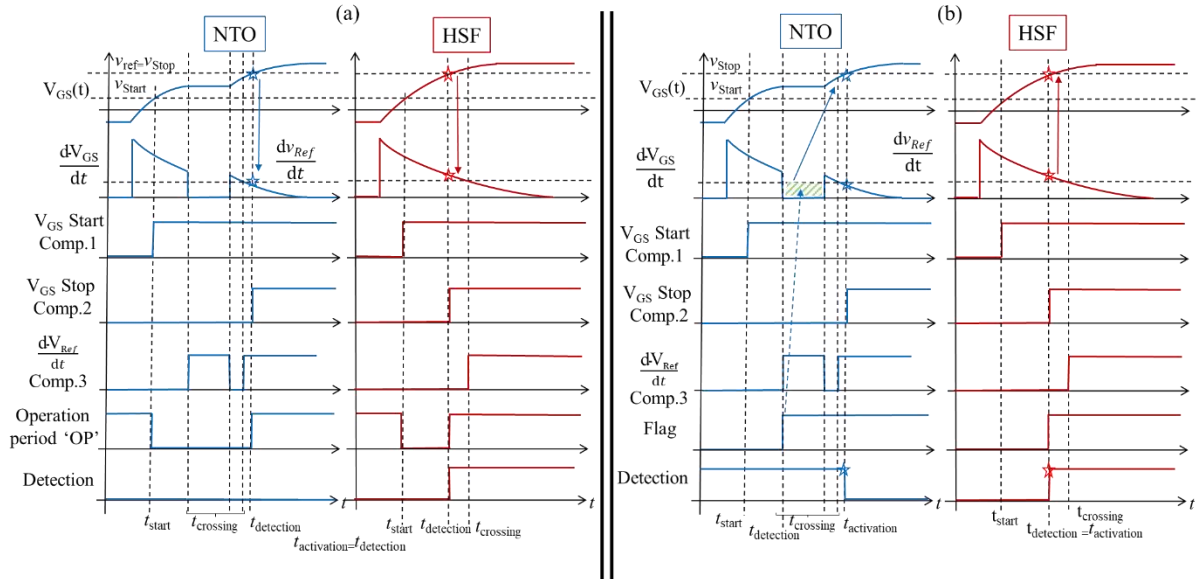
Fig.III. 35 presents the detection circuit for a fixed  $R_G$ . The capacitor  $C_s$  connected in parallel with the gate is a sense capacitor, sensing the derivation of the voltage  $V_{GS}$ . This sense capacitor must be much smaller than the minimum input capacitor of the power transistor ( $C_s \ll C_{iss\_Min}$ ).  $R_s$  and  $C_s$  are seized using the equation developed above, and adapted with simulations. The  $I_{Cs}$  current passing through  $C_s$  is further amplified and converted in voltage, which is then compared with  $dV_{Ref}/dt$ . Two other comparators with  $V_{GS}$  signal are used to create a monitoring window for the readout and detection. Flip-flops are added for both approaches, with the purple parts being the dip detection circuit and the green ones being the slope detection circuits.



**Fig.III. 35.** Detection and protection circuit based on slope and dip approaches. Note:  $C_s = 100\text{pF}$ ,  $R_s = 100\Omega$  and other blocks are considered ideals.

The difference in the circuit between the approaches is visible in the digital blocks. Therefore, Fig.III. 36 (a) and (b) show a timing chart for both approaches (dip and slope) under NTO and HSF. One can see that  $V_{GS}$  is still rising to its saturation value. As shown in Fig.III. 36 (a), the detection starts at  $t_{Start}$  where  $V_{GS} \approx V_{th}$  and stops at  $t_{Detection}$  where  $V_{GS} = V_{Ref} = V_{Stop}$ ,

at this time the detection signal depends on the output of the third comparator, as shown in Fig.III. 36 The output of the third comparator signal is neglected before and after  $V_{Ref}$ . Fig.III. 36. (b) shows the same detection start signal, the stop signal is where  $V_{GS} = V_{Ref}$  but it differs at reading the flag. The flag is activated at  $t_{Detection}$  the first crossing  $dV_{GS}/dt$  and the reference signal, where it is saved until  $t_{Activation}$ .



**Fig.III. 36.** Timing chart for derivation detection method under NTO and HSF (a) Slope approach (b) Dip approach.

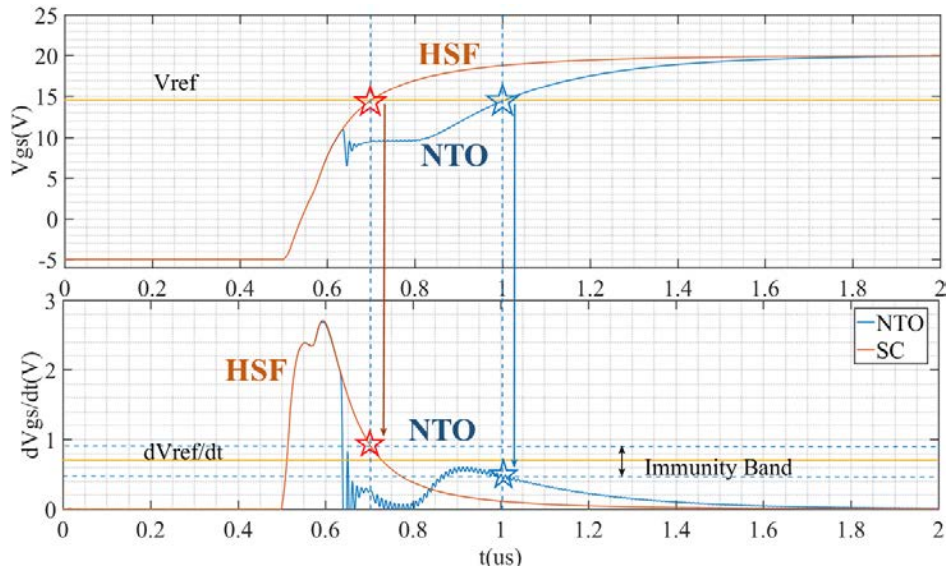
The discussed approaches have no time dependency; however, they depend on when the gate voltage rises above the reference level  $V_{Ref}$ , so the lower the reference, the earlier the detection, with the only condition of the  $V_{GS} > V_{GS\_M}$ . So which of these approaches is the fastest? In order to verify the validity of the proposed detection circuits, to achieve more accurate and robust study of the methods, and to answer the question above, simulation results using LTspice<sup>TM</sup> are performed.

The parameters used in the simulations are:

- On the low side a power device,  $V_{Bus} = 600V$ ,  $I_{Load} = 50A$ ,  $V_{Drv} = -5/+20V$  and  $R_G = 50\Omega$  (the high  $R_G$  value is deliberately chosen high for representation purposes).
- On the high side a Schottky diode C4D20120A, 20A, 1200V.

The power device C2M0025120D library model is proposed by WolfSpeed easily imported in LTspice<sup>TM</sup>. The LTspice<sup>TM</sup> model does not take into consideration the thermal self-heating during accidental short-circuit operations, which is fast and at high temperature levels. Modifications need to be added on the power transistor structure. [20] presents a transient electro thermal circuit model, which allows for analysis of the SC operation. The C2M0025120D specifications are  $V_{DS} = 1200V$ ,  $I_D = 90A$ ,  $R_{DS\_ON} = 25m\Omega$  with  $C_{iss} = 2788pF$ ,  $C_{oss} = 220pF$  and  $R_{G\_Int} = 1.1\Omega$ . In addition to have more accurate results, gate loop and power loop parasitic inductances were included to better reproduce experimental waveforms,  $L_D =$

25nH  $L_{SK}= 25\text{nH}$ ,  $L_G= 5\text{nH}$  (values are deliberately chosen high for representation purposes and to bring the approach to its limit).



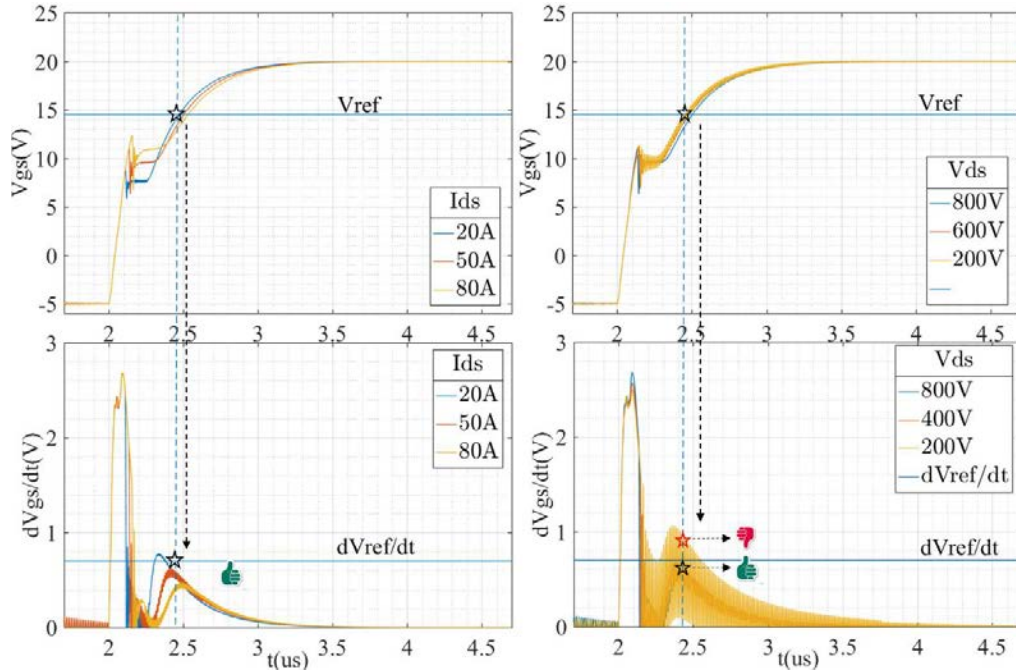
**Fig.III. 37.** Simulation waveforms of the derivation method, using the slope detection, under NTO and SC-HSF

Fig.III. 37 presents the simulation voltage signal  $V_{GS}$  and its derivative under NTO and HSF conditions. Fig.III. 38 takes the NTO condition further into different  $I_{DS}$  and  $V_{DS}$  values. The simulations show the slope differences and the dip presence in the gate voltage derivative. Parasitic inductors ( $L_{D\ side}= 25\text{nH}$ ,  $L_{S\ side}= 25\text{nH}$  and  $L_{G\ side}= 5\text{nH}$ ) were added to bring the approaches to their limits. The values of  $L_{S\ side}$  and  $L_{G\ side}$  have been increased by a factor of 5 to 10 to test the robustness of the detector. The slope approach shows its limits in Fig.III. 38, in particular at low current, giving a reduced Miller plateau and a higher slope of the voltage  $V_{GS}$  in the second phase, after the plateau sequence. The dip approach assures a better robust functionality, as shown in Fig.III. 39. The dip approach overcomes the overvoltage caused in the beginning of the Miller plateau, where this overvoltage makes the presence of the dip more remarkable and apparent in the derivative signal. Fig.III. 39 supports the dip approach as well, where the dip is detected before the stop signal appearance and the flag remains 0, even when oscillations are present.

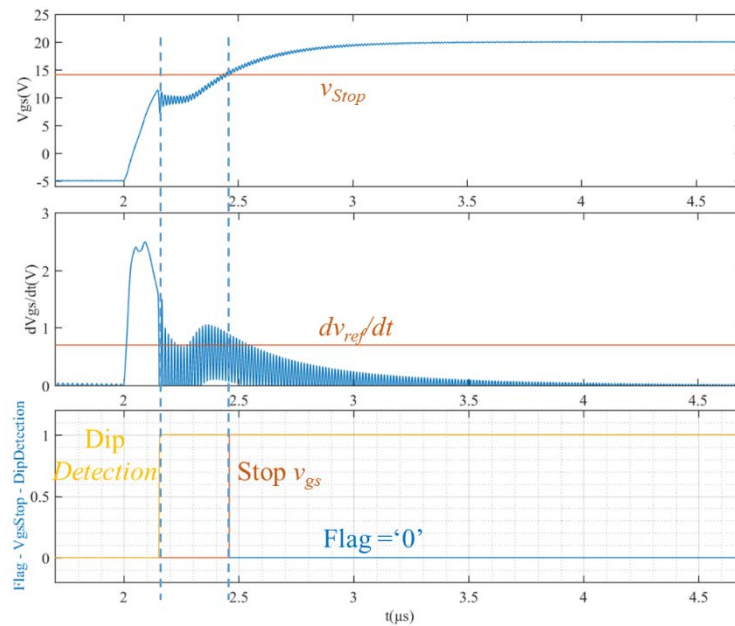
The detection flag is assured under both approaches (dip and slopes). The detection time for both methods is below 200 ns due to the same reference gate voltage of  $V_{Ref}$  15.5V. Note that the impact of this reference level has a direct effect on the detection time. However, the slope approach shows its limits in Fig.III. 39 under NTO where it can trigger false detection flags due to the high oscillations. Fig.III. 39 proves that both methods are independent of time. Fig.III.40 illustrates how important  $V_{Ref}$  should be early for the detection of SC. With an early  $V_{Ref}$ , an early detection will take place and probably  $V_{Ref}$  interfering with the second peak in NTO mode, causing a false detection. To overcome this interference, the dip method will not take into consideration the second peak, even if there are interferences. Fig.III. 38 represents a variation



of  $I_{Load}$  and  $V_{Bus}$  in the circuit under HSF, where we can see the oscillation reaches  $dV_{Ref}/dt$ , for low  $i_{ds}$  and  $V_{DS}$ . Under SC,  $dV_{GS}/dt$  does not show any oscillation.



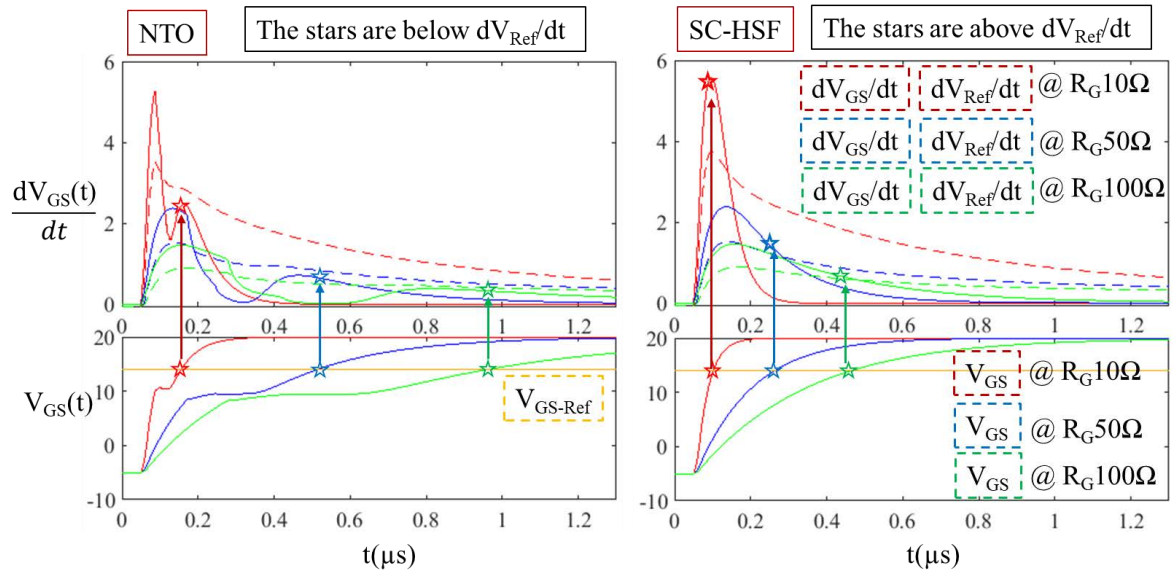
**Fig.III. 38.** Simulation waveforms of derivation method using the slope approach under NTO conditions for different  $I_{DS}$  and  $V_{DS}$ . Typical condition:  $V_{Bus}= 800V$ ,  $I_{Load}= 50A$ ,  $R_G= 50\Omega$ , DUT: C2M0025120,  $L_G= 5nH$   $L_S=L_D= 25nH$



**Fig.III. 39.** Simulation waveforms of derivation method using the dip approach under NTO condition at  $V_{Bus}= 200V$  and  $I_{Load}= 50A$ . Parasitic inductances are added.

The study of this method has been focused on a constant reference voltage. Fig.III. 40 presents another simulation study. This study has been led for variable references. The circuit of the variable reference that binds the reference level to the variation of  $R_G$  and  $C_{iss}$  is not presented. The circuit is based on the detection of the high peak of  $dV_{GS}/dt$  and then adapt the

reference to allow a safe detection. The variations of the reference are adapted to each power transistor input capacitance and different gate resistors  $R_G$ . Fig.III. 40 presents simulation results of the automatic variation of the reference level  $dV_{Ref}/dt$  and its behavior. The simulation is done for three different  $R_G$  values under NTO and SC-HSF. As one can see, the representation of the stars in the curves under NTO is below  $dV_{Ref}/dt$ ; and under SC-HSF are above it, which leads to a clean and robust detection. The studied power transistor is C2M0025120D under  $V_{Bus}= 800V$ ,  $I_{Load}= 50A$ ,  $V_{Drv}= -5/+20V$ .



**Fig.III. 40.**  $dV_{GS}/dt$  (solid line) under different  $R_G$  with variable reference level (dashed line).

One should note the importance of the gate resistor effect on the detection time. The lower the gate resistance, the higher the relative immunity band. This behavior is well compatible with the tendency to take advantage of the turn-on fast switching speed of the SiC MOSFET. But note that this result is established by not taking into account measurement oscillations and external disturbances. As shown in Fig.III. 40 the stars present the detection moment, when  $V_{GS}$  reaches  $V_{GS\_Ref}$ , plus the propagation time of the digital and protection circuit around (20 ns maximum with the right technology). These stars are distributed differently in time depending on  $R_G$ . This method will not be further developed here.

### 3.3.Design and layout of the derivation method

All the blocks used in the derivation method, Fig.III. 35, are carefully designed using X-Fab SOI 0.18 $\mu m$  CMOS technology (XT018) under Cadence<sup>TM</sup>. In general, the circuit consists of a sensing capacitor, a sensing resistor, three comparators and few digital blocks. Both approaches (dip approach and slope approach) were integrated in the adapted active gate driver CMOS AGD presented in chap.II, including SSD and the ability of the segmented buffer to go to a high impedance state HZ. The SSD is activated after the segmented buffer undergoes the HZ state, which is equivalent to the propagation time of the segmented buffer.

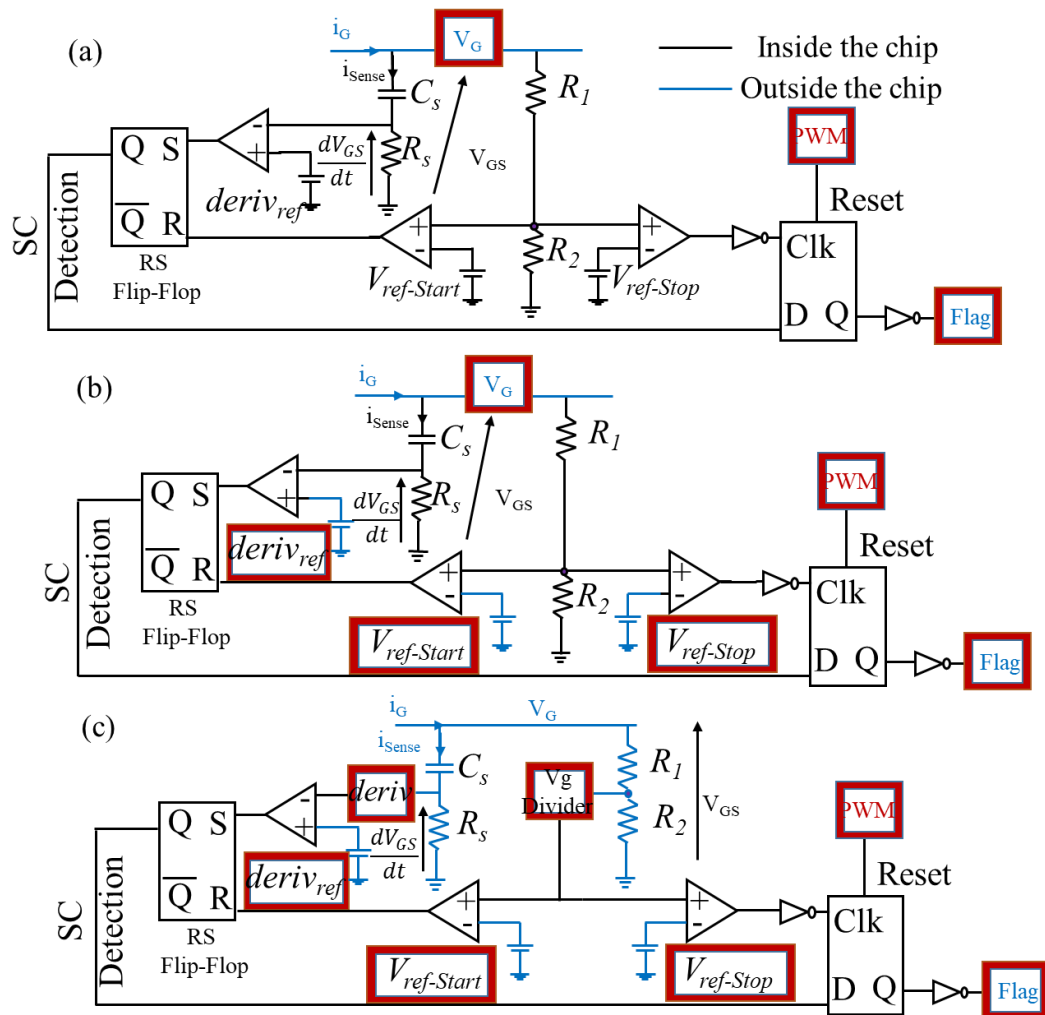


Fig.III. 41. Detection schematic based on the dip approach (with  $R_s \times I_{sense} \ll V_{GS}$ ) with different level of integration.

In order to validate this detection method, few steps are considered. The detection circuit is simplified in different level to ensure the detection of the SC and the study of this method (Constant threshold levels, different level of integration, ...). As Fig.III. 40 presents the possibility to adjust and adapt the reference levels, however, in this study the reference levels are taken constant. Otherwise parameter variation ( $R_G$ ,  $C_{iss}$ , ...) have a huge impact on the derivative of the gate-source signal  $dV_{GS}/dt$ , which required an adapted RC filter. Therefore, the dip detection schematic is illustrated in Fig.III. 41, the figure shows the input-output pads as well. For each approach, there are three degrees of integration choices. The first degree is all the blocks are integrated, Fig.III. 41 (a). The second degree has the set of the references levels outside the microchip, and they are not fixed and integrated inside as the first degree, Fig.III. 41 (b). The third degree is a back-up plane with the sensing capacitor and the sensing resistor non-integrated, which will add more noise to the detection, Fig.III. 41 (c). All the digital blocks used are offered by the XT018 logic library. The used blocks operate under 5V supply voltage, with  $0.5\mu\text{m}$  channel length, standard speed and power, where the gate-source voltage of the power transistor is driven by a range from 15 to 25V. Therefore, a voltage divider is introduced

in the circuit. The circuit is referenced to the kelvin source of the power transistor, unlike the gate charge method.

The sizing of  $C_S$  and  $R_S$  depends on the approach, respectively to the equations, eq.(III. 18), where the sensing capacitor and resistor behave as a first-order high pass filter, realized by an RC circuit. For a given amplitude of  $V_{Out}$  (chosen around 4.5V) and for  $i_G \gg i_{sense}$  the sizing of  $R_S$  and  $C_S$  is just a matter of equations. For the dip approach, they are equal to  $C_S= 4pF$   $R_S= 2k\Omega$ , and for the slope approach  $C_S= 5pF$   $R_S= 1k\Omega$ , (the values are proportional to LTspice Values 100pF and 100 $\Omega$ ). The difference between the slope and dip approach values are due to what is important to amplify and shape. For the slope approach the second peak should have a high peak and a slew rate. For the dip approach, the dip should be well shaped and present.

$$f_c = \frac{1}{2 * \pi * R_S * C_S}$$

$$V_{Out}(t) = i_{sense}(t) * R_S$$

$$i_{sense}(t) = C_S * \left( \frac{dV_{GS}(t)}{dt} - \frac{dV_{Out}(t)}{dt} \right) \quad (III. 18)$$

$$V_{Out}(t) = R_S * C_S * \left( \frac{dV_{GS}(t)}{dt} - \frac{dV_{Out}(t)}{dt} \right)$$

The used resistors are a N+ poly ohmic resistor, their sheet resistance is equal to 330 $\Omega/\square$  (MRpoly); and N+ poly high ohmic resistor, its sheet resistance is equal to 6700 $\Omega/\square$  (HRpoly). Power  $V_{GS}$  varies in an average range of 25V, even if the output of the filter  $V_{Out}$  is sized for 4.5V, unexpected parameter variation can lead to high  $dV_{GS}/dt$  peaks. The library of XT-0.18 offers different capacitors, in our range of study, there are few interesting capacitors. The used capacitor is a fringe capacitor with a breakdown voltage  $>70V$ , and its capacitance per cell is 37.7fF for a  $W= 5.76\mu m$  /  $L= 11.1\mu m$ . the occupied space for each capacitor in the layout is 200 $\mu m * 34\mu m$  and 255 $\mu m * 34\mu m$ .

One of the main blocks is the comparator. The used comparator must have high DC gain and high bandwidth in order to operate correctly up to frequencies of MHz. Moreover, the structure of the comparator must allow operation with a power supply range between 4 to 5V. As well as low energy consumption. Thanks to le-long [171] for his previous work, the comparator structure is proposed in Fig.III. 42.

This comparator is designed based on a differential preamplifier which allows having a wide common mode input voltage range. the transistors of the pairs (M1, M2), (M3, M4) have the same geometrical parameters (W, L). The second stage of the "common source" amplifier is then used to amplify the output signal from the first floor. Finally, a buffer in push-pull configuration is added to minimize the reaction time of the output commands. In order to size this comparator, all the transistors are considered to be at saturation point, the parameters of the

comparators are given in Tab.III. 10. The total layout of the comparator is  $56\mu\text{m} \times 53\mu\text{m}$ . The DC gain of the comparator is expressed by, eq.(III. 19). [171]

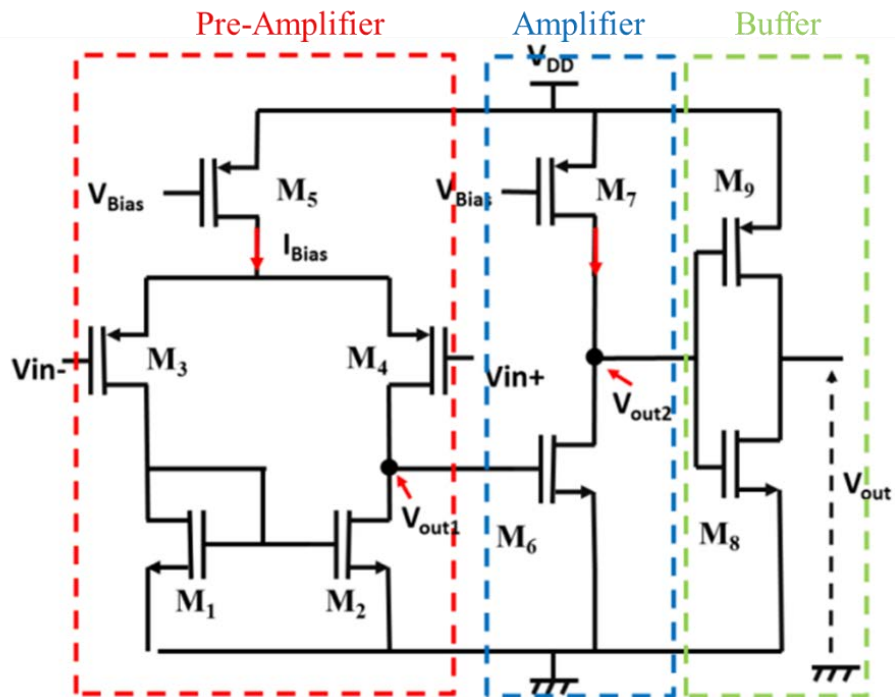


Fig.III. 42. Comparator structure , [171]

$$A_0 = g_{m3} \cdot g_{m6} \cdot R_1 \cdot R_2 \quad (\text{III. 19})$$

Tab.III. 10. Design and simulation parameters under Cadence

Design parameters		Simulation parameters	
(W/L) <sub>1,2</sub>	50 $\mu\text{m}$ /0.5 $\mu\text{m}$	V <sub>Supply</sub>	5V
(W/L) <sub>3,4</sub>	3 $\mu\text{m}$ /0.5 $\mu\text{m}$	A <sub>0</sub>	54db
(W/L) <sub>5</sub>	150 $\mu\text{m}$ /0.5 $\mu\text{m}$	f <sub>-3db</sub>	25.87MHz
(W/L) <sub>6</sub>	12 $\mu\text{m}$ /0.5 $\mu\text{m}$	SR <sub>(Vout2)</sub> (C <sub>c</sub> = 0.5pF)	1250V/ $\mu\text{s}$
(W/L) <sub>7</sub>	150 $\mu\text{m}$ /0.5 $\mu\text{m}$	Consumption	834 $\mu\text{A}$

The  $V_{\text{bias}}$  of the comparator can be generated by different ways. The basic one is the one pull-up diode-connected PMOS transistor, Fig.III. 43 (a). The common used one is the current mirror, it depends on how much current the circuit needs. The generation of the reference level in the proposed detection circuit can be provided by different ways. Fig.III. 43 proposes three basic voltage references schematics. The used one is (a). the pull-up diode-connected PMOS transistor, where the transistor operates in the saturation region  $V_{\text{DS}}=V_{\text{GS}}$ . For a given  $I_{\text{DS\_NMOS}}=I_{\text{DS\_NMOS}}$  and a low  $V_{\text{eff\_NMOS}}$ , eq.(III. 20) is provided to size the transistors. The PMOS and NMOS resistances are equivalent respectively to  $1/g_{\text{mP}}$  and  $1/g_{\text{mN}}$



$$\frac{W}{L} = \frac{2 \cdot I_{Dsat}}{\mu_N C_{ox}} \cdot \frac{1}{V_{eff}^2} \quad (III. 20)$$

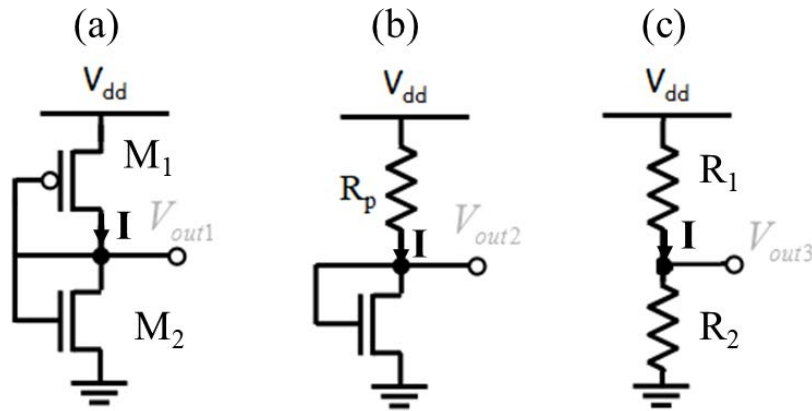


Fig.III. 43. Three basic voltage references schematics

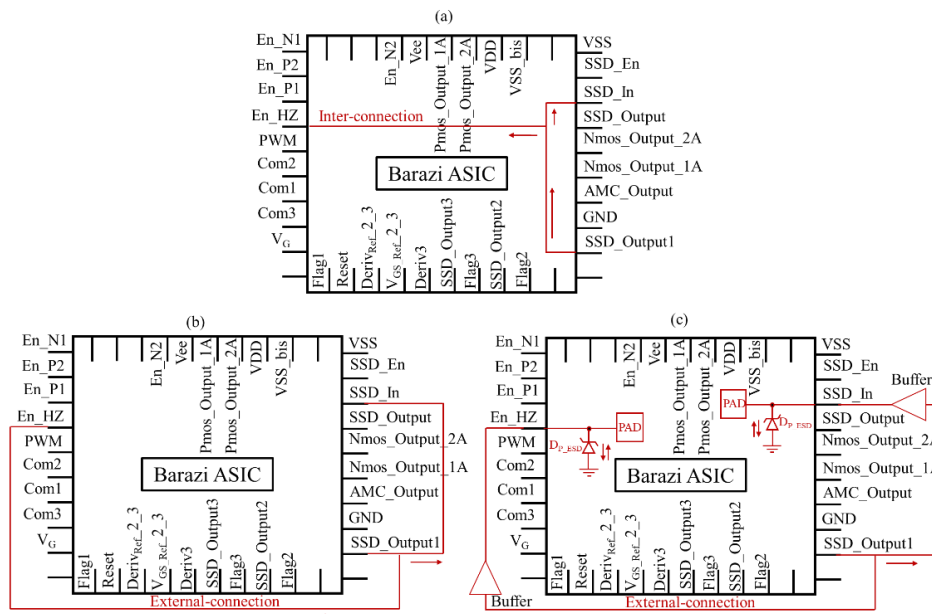
A brief study was led for both circuit in Fig.III. 43 (a) and (c). This study was focused on generating an output reference level equal to 3V from a voltage supply of 4.5V. Tab.III. 11 presents the different parameters for each circuit. One should note, the XT-0.18 library propose two resistors in the scope of our study, rnp1 (>1.6KΩ) and rnp1h (>30KΩ). Temperature variation from -40°C to 120°C shows slight changes in the output voltage. The table highlights a trade-off between power consumption and area. The Rnp1/Rnp1 structure is the one with the best performance on all criteria in Tab. III. 9.

Tab.III. 11. Different voltage reference circuits parameters

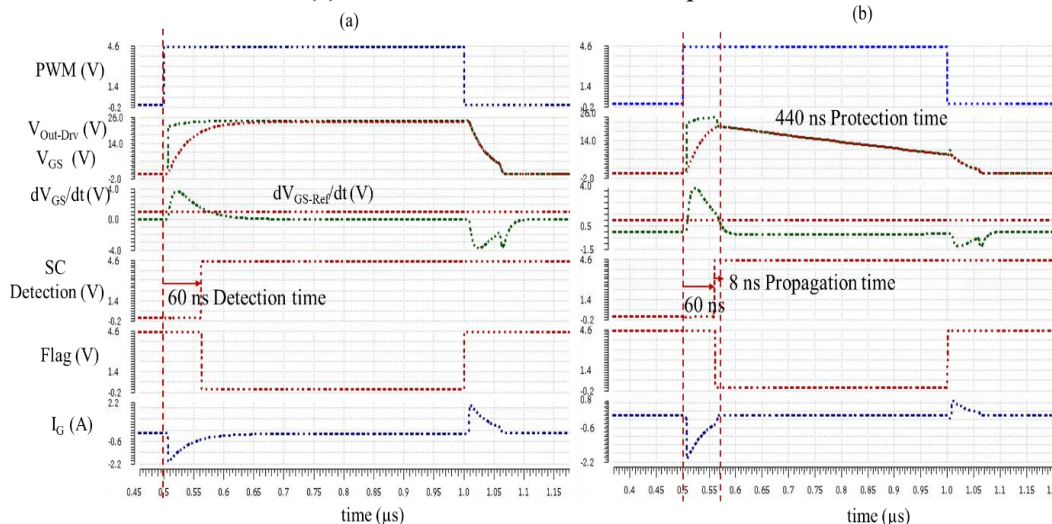
	Fig.III. 43 (a)	Fig.III. 43 (c)	Fig.III. 43 (c)	Fig.III. 43 (c)
	Pe5/ne5	Rnp1/ Rnp1	Rnp1h/ Rnp1h	Rnp1/ Rnp1h
(W/L) <sub>1</sub>	20μ/0.5μ	R <sub>1</sub>	5kΩ	R <sub>1</sub>
(W/L) <sub>2</sub>	1μ/0.5μ	R <sub>2</sub>	10kΩ	R <sub>2</sub>
<b>V<sub>out</sub>@ 25°C</b>	3.095V	2.971V	2.993V	3.025V
<b>I</b>	258μA	49.5μA	297μA	297μA
<b>V<sub>dd</sub></b>	4.5V	4.5V	4.5V	4.5V
<b>Surface</b>	3.6μm*24.3μm	2.5μm*33μm	5.5μm*63μm	2.5μm*106μm
<b>ΔV<sub>out</sub>@ T° (- 40°,120°)</b>	± 0.05V	± 0.001V	± 0.001V	± 0.20V

The pre-study of the behavior of the gate driver including the detection and protection circuit is presented in Fig.III. 45. The figure presents simulation waveforms using Cadence under 25°C with R<sub>G</sub>= 10Ω and V<sub>Drv</sub>= -5/20V and an equivalent capacitor of 3nF representing the power transistor. The different commands of the gate driver are presented in Tab.III. 12. The gate

driver commands are explained in detail in Chap.II. Fig.III. 45.(a) presents the behavior of the AGD without the feedback loop of the detection Flag. The detection time of the SC is equal to 60ns. In the second configuration, En\_HZ and SSD\_IN receives the output flag. This configuration will activate the HZ state first and then softly shut down the transistor, in this case the equivalent capacitor, which leads to a propagation time equal to 8ns. In the first place, the logic output (SSD\_Output1) was designed in order to have the feedback loop inside the chip, Fig.III. 44 (a). Unfortunately for more flexibility, in practice this feedback loop is done externally from AGD, which will add more delay, Fig.III. 44 (b). And due to the used pad of protection (which requires few hundred  $\mu\text{A}$ ) an external buffer at each Pad is required, adding more delay on the detection, Fig.III. 44 (c). The difference is visible in the experiment section. The set of the reference levels are for the derived  $V_{GS}$  3V and for the  $dV_{GS}/dt$  0.9V.



**Fig.III. 44.** Representation of the SSD feedback loop. (a). Internal connection. (b). External connection (c). Bufferized PADS due to the protection diode.

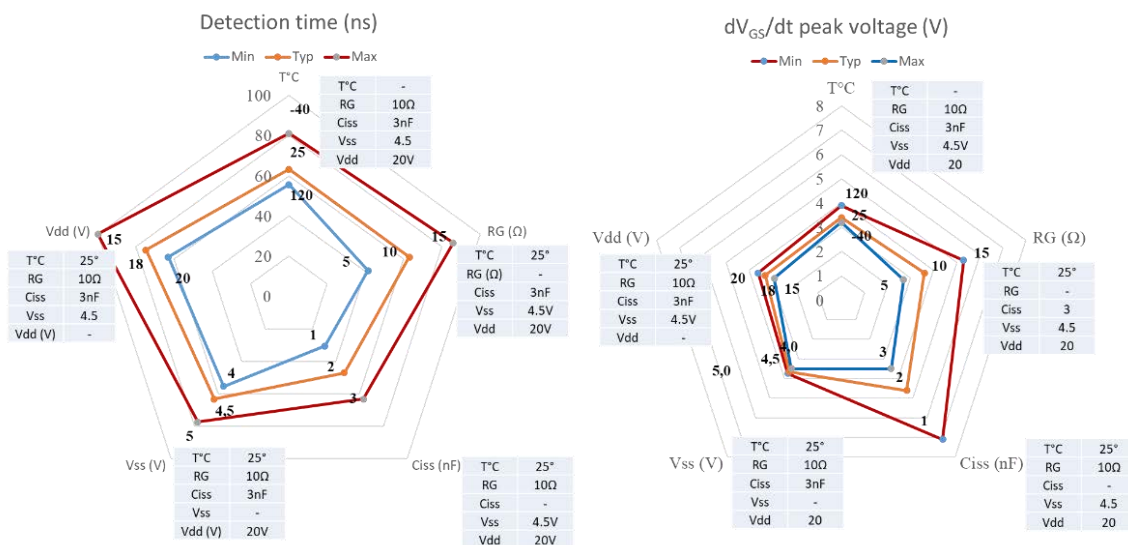


**Fig.III. 45.** Simulation waveforms under Cadence of the Gate driver including the detection circuit (dip method) under SC-HSF. (a). without protection (b). with protection.

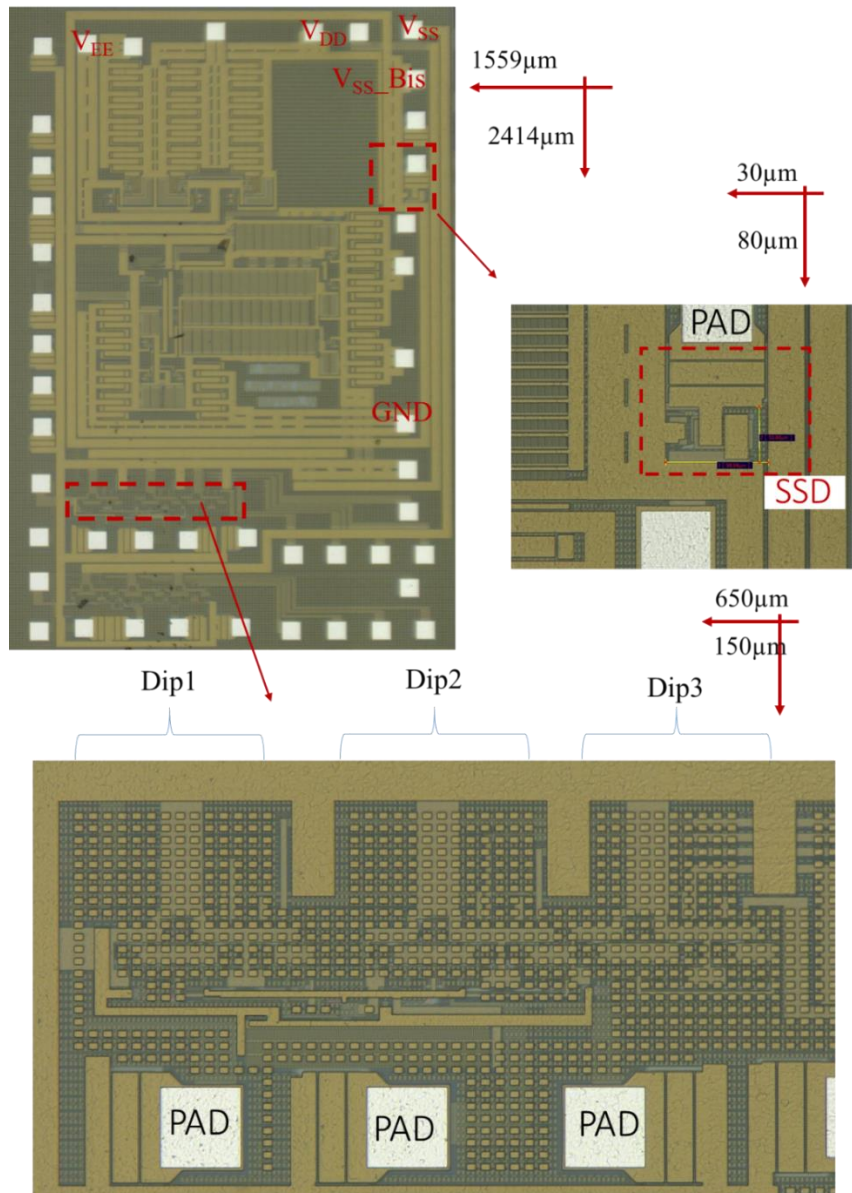
**Tab.III. 12.** Different configurations of the commands used to simulate the behavior of Fig.III. 45

Configuration	(a)	(b)
AMC	'1', (150ns)	'1', (150ns)
En_P1/En_P2	'1', '1', (3A)	'1', '1', (3A)
En_N1/En_N2	'0', '0', (3A)	'0', '0', (3A)
Reset	'0'	'0'
En_HZ	'1'	'SSD_Output1'
SSD_In	'0'	'SSD_Output1'
SSD_En	'0'	'0'

Fig.III. 46. displays a variation of different parameters which affects directly or indirectly the detection time and the  $dV_{GS}/dt$  peak. The parameters are the temperature (-40, 25, 120°C), the supply voltage  $V_s$  (4, 4.5, 5V), the supply voltage  $V_{DD}$  (15, 18, 20V), the gate resistor (5, 10, 15Ω) and the equivalent capacitor representing the power transistor (1, 2, 3nF). The set of threshold levels is fixed 3V for  $V_{GS}$  and 0.9V for  $dV_{GS}/dt$ . As the detection time on the radar chart illustrates, the detection is assured in all the cases with different detection times. At extreme values the detection will not be possible anymore, as in the case where  $C_{iss}= 1nF$ ,  $dV_{GS}/dt$  peak voltage exceeds 5V (operation voltage). In order to understand this clearly the peak of  $dV_{GS}/dt$  is presented in a radar chart as well. The two limiting parameters are the gate resistor and the equivalent capacitor, where the  $dV_{GS}/dt$  peak increases for high gate resistor and low capacitor values. In the case when the capacitor is equal to 1nF the peak reaches 7.1V, which will cause breakdown of the used transistors. But most power transistor with a  $C_{iss}= 1nF$ , are transistors driven by 15V. As  $V_{Drv+}$  is equal to 15V leads to attenuate this peak. Therefore, a trade-off between these parameters is strongly recommended. Otherwise, the AGD designed offers the possibility to set a different  $R_s$  &  $C_s$  values, if the integrated ones do not fit the configuration.



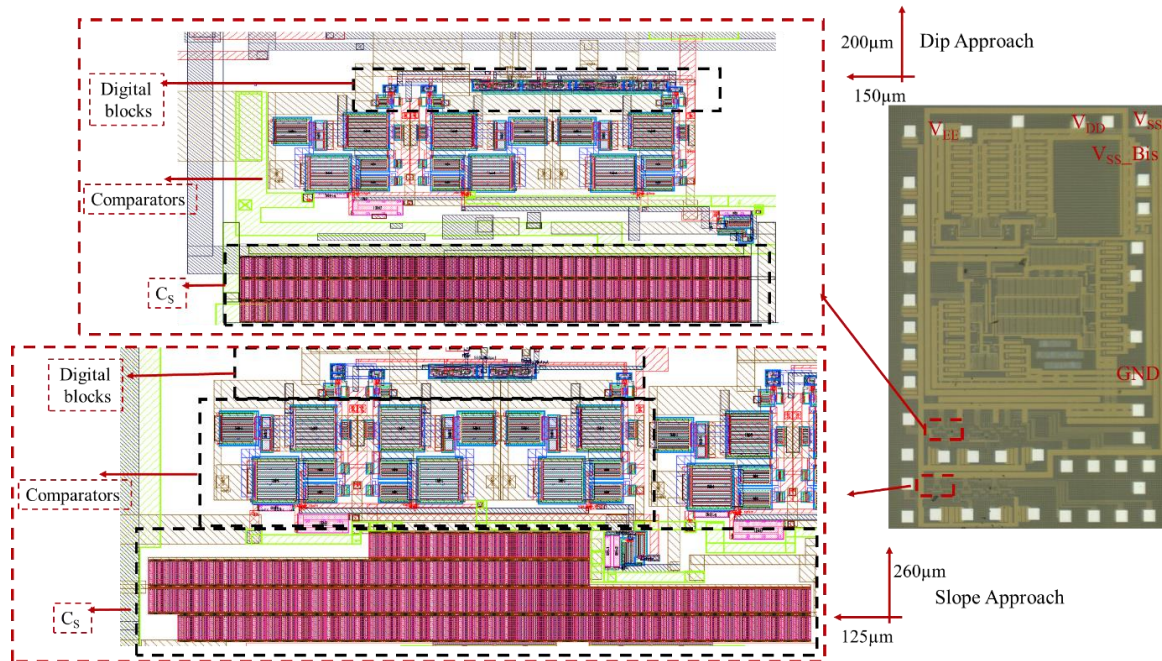
**Fig.III. 46.** Two radar charts displaying multivariate data of the detection time and  $dV_{GS}/dt$  peak



**Fig.III. 47.** Microscopic zoom at the Dip approach (detection) and SSD (protection)

As a reminder, the layout of the whole ASIC is divided in two main parts. The Active Gate Driver is  $2414\mu\text{m} \times 1559\mu\text{m}$ , as presented in Chap.II. And, the detection block for both detection techniques has a surface of  $200\mu\text{m} \times 150\mu\text{m}$ , and the SSD has a surface of  $80\mu\text{m} \times 30\mu\text{m}$ . The detection circuit has a typical DC consumption of 1.52 mW (or 0.34 mA at 4.5V, 25°C). Fig.III. 48 presents a zoom view of the detection circuit layout. The IC is packaged in a QFN40 6mmx6mm, presented in Chap.II.





**Fig.III. 48.** Layout view of the detection circuit under Cadence™ (dip and slope approach) and the microscopic view of the AGD

### 3.4.Experimental results

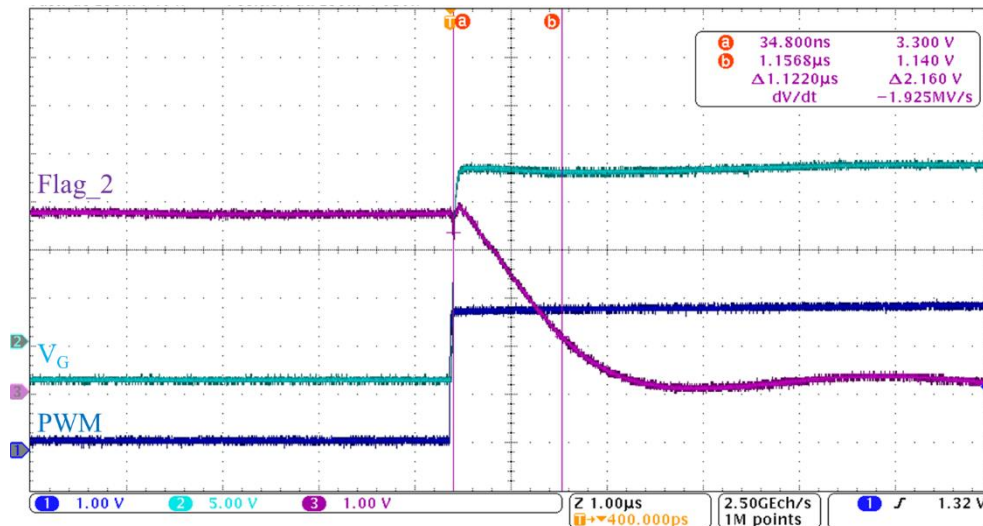
After validating the main buffer under an equivalent capacitor and under a DUT, the gate derivation circuit has been investigated. The detection circuit is investigated into two part, first under the same equivalent capacitor 1.5nF, and second the capacitor is replaced by a power transistor C2M0080120. Self-compensated voltage probes (300 V and 1 GHz bandwidth (BP) Tektronix TPP1000) with a 3.9pF input capacitance is used with A 1GHz bandwidth oscilloscope. For the test bench view, and the PCB view, check Chap.II.

#### 3.4.1. Experimental results under an equivalent capacitor and no power, V0.1

In order two have more flexibility in the detection, the second circuit has been used. The second circuit is the one with only the reference level set non-integrated. Therefore, the levels are set to  $V_{Ref} = 3V$  and  $dV_{Ref}/dt = 0.7V$ . The driver positive and negative voltages are respectively  $V_{Drv+} = 24V$  and  $V_{Drv-} = 4V$ .

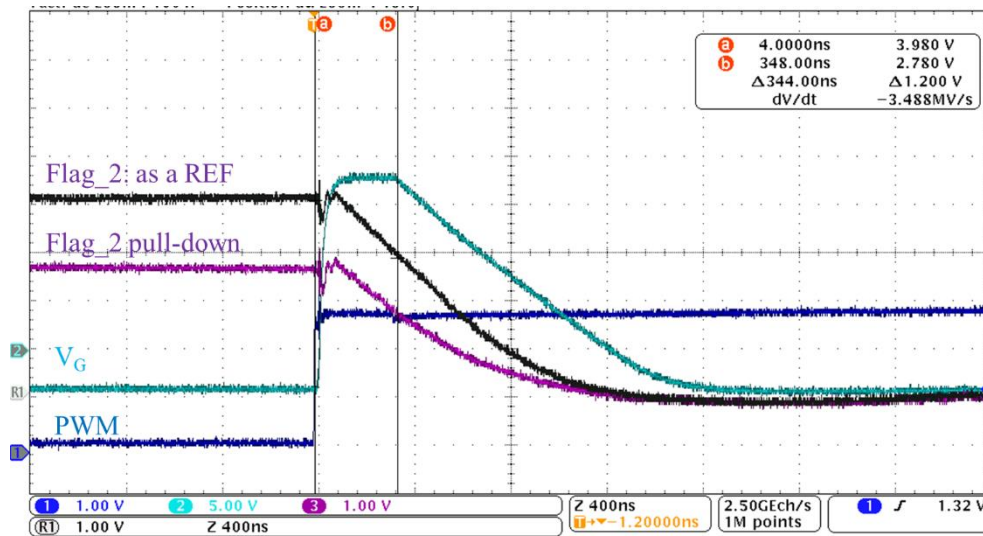
As the one can see, in Fig.III. 49 the flag of the second circuit (flag\_2) is generated. The flag passes from high voltage (4V, no detection) to low voltage (0V, SC detection). The one should note, the fall time is so slow, around  $2\mu s$ , due to an design error at the output of the detection circuit. A logic 5V inverter was used, which is very small, and source less than  $5\mu A$ , which is insufficient for even a probe with an input capacitance of 3.9pF. Therefore, this problem should be compensated with an extended buffer with a low input capacitance  $<500fF$ .





**Fig.III. 49.** Oscilloscope waveforms of the ASIC including the detection flag, (the protection is not considered)

Afterwards, the flag\_2 is sent to the FPGA, in order to be able to re-send the command to the high impedance and the SSD input pins. Due to the slow fall time, the propagation time of the protection flag is delayed. The protection of the ASIC is done after 500ns. A pull down resistor of 20kΩ is added in order to gain in speed, therefore the protection time is generated after 340ns, which is slow compared to what was anticipated in the design, Fig.III. 50.



**Fig.III. 50.**  $V_{GS}$  under protection, using a pull-down resistor on the Flag\_2

### 3.4.2. Experimental results using a DUT and power test bench, V2.2

After validation of the behavior of the buffer and C2M0080120, the detection circuit is tested. The PCB of the AGD is connected in the low side of the power test bench V2, including vertically the DUT (C2M008120 transistor). In order to validate the detection circuit, two configurations are required:

NTO: in the High side a 600V SiC diode in parallel with a load inductance 270µH is used.

SC-HSF: in the high side a piece of copper is used in order to short the drain and the source.

In both configuration, the output of the buffer is split with an external gate resistor of  $10\Omega$  at each output. In order to be able to use the first detection circuit using C2M0080120 ( $C_{iss}=1.13\text{nF}$ ,  $C_{rss}=7.5\text{pF}$ ) (circuit 1, where everything is integrated in the CMOS ASIC, with constant references set), the gate driver voltages are reduced to  $V_{DrV+}=16\text{V}$  and  $V_{DrV-}=-4\text{V}$  (instead of  $24.5\text{V}$  and  $4.5\text{V}$ ). Note that the integrated reference level set are designed for C2M0025120.

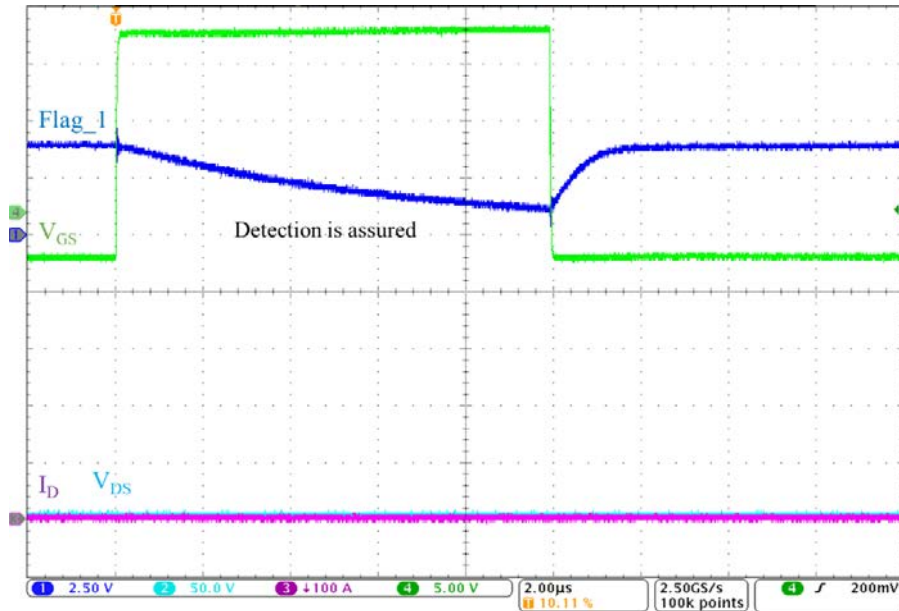


Fig.III. 51. Oscilloscope waveforms under  $V_{Bus}=0\text{V}$  showing the detection flag

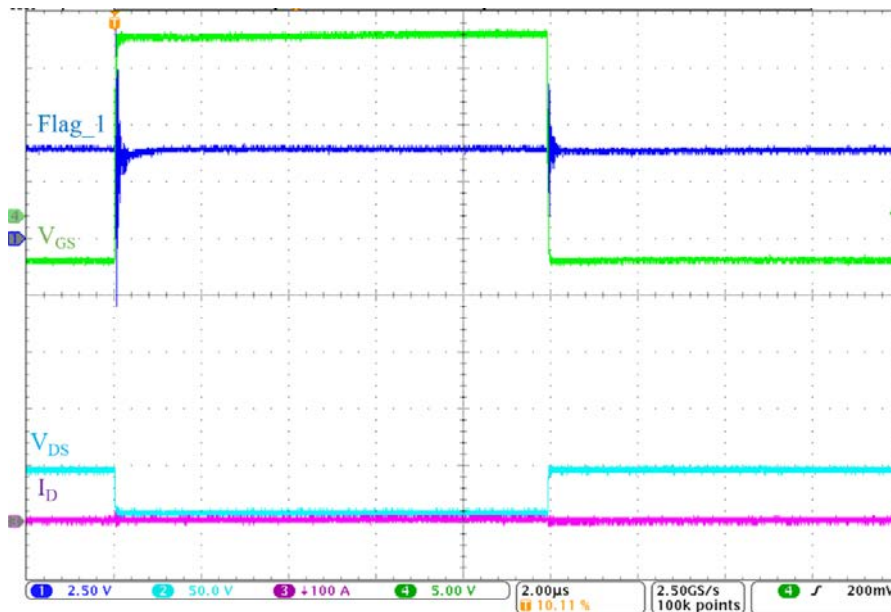


Fig.III. 52. Oscilloscope waveforms under NTO and  $V_{Bus}=50\text{V}$

Fig.III. 51 presents that at  $V_{Bus}=0\text{V}$  the detection is assured, with a long fall time, due to the error in the design ( $5\text{V}$  logic inverter used in the output of the circuit). This error caused us more problems under high bus voltages, as generating oscillation or delay the detection flag. The detection of the short-circuit is assured for a  $V_{Bus}$  range of  $25\text{V}$  to  $200\text{V}$ . And moreover the

non-detection of normal operation is assured as well for the same range. Fig.III. 52 and Fig.III. 53 presents the non-detection (flag remains at 5V) under normal operation. The voltage drop at the Flag\_1 signal in Fig.III. 53 is due to noise effect on the 5V logic inverter used. Fig.III. 54, presents the detection of the SC-HSF under 50V, the detection is assured for higher voltages. The one should note that detecting at low voltage is more challenging for devices the operates typically under 1.2kV. Robustness of the method is under investigation.

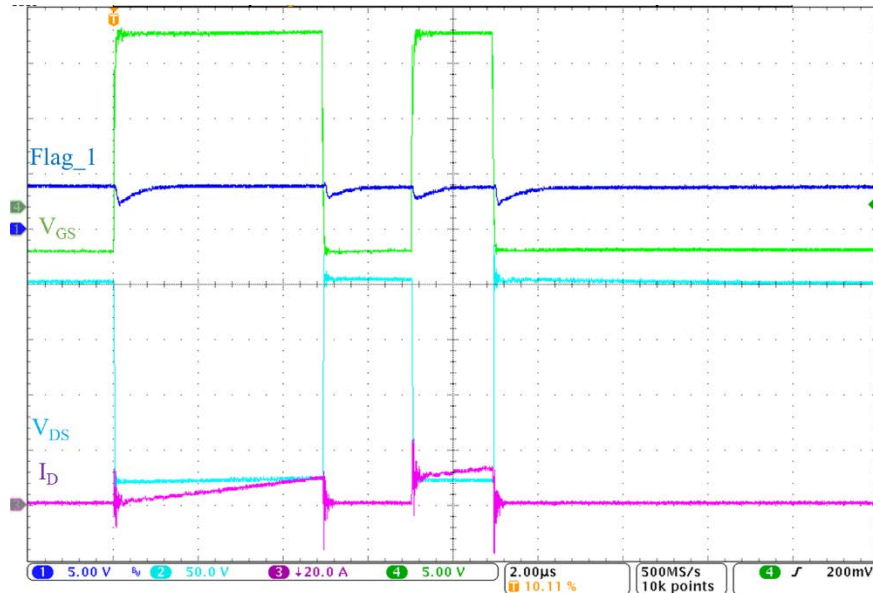


Fig.III. 53. Oscilloscope waveforms under NTO, double pulse and  $V_{Bus}= 200V$

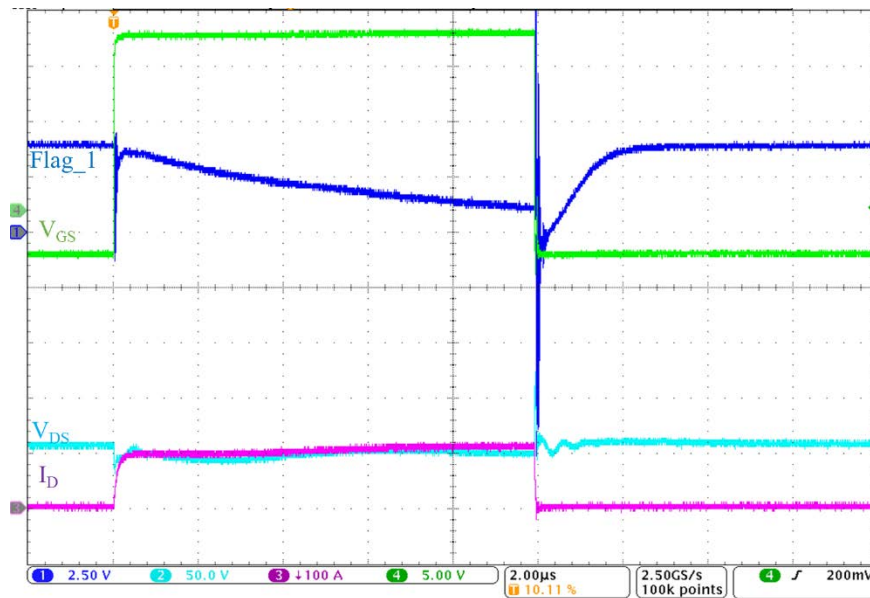


Fig.III. 54. Oscilloscope waveforms under SC-HSF @  $V_{Bus}= 200V$

#### **4. Feedback from power FET to CMOS: Third monitoring method**

An innovative technique was designed and sent for fabrication. This technique is being considered for IP protection, and was a complementary technique as a side project of this work. Hence, this won't be presented in this manuscript.





- Simplified circuit is used (RC filter). Therefore, the circuit is not robust for different parameters variation. Further study is required.
- Detection can be assured for different reference sets for a small range of variations.
- Dip approach
  - Novel approach
  - Medium SNR tolerance. Noise can be in favor for this approach
  - Gate pin based
  - HSF fault
  - Two references set ( $dV_{GS\_Ref}/dt$ ,  $V_{GS\_Ref}$ )
  - $V_{Bus}$  &  $I_{load}$  robust
  - Simplified circuit is used (RC filter). Therefore, the circuit is not robust for different parameters variation. Further study is required.
  - Detection can be assured for different reference set for a small range of variation.

All the methods can be easily integrated and adapted to its respective application. All the blocks are low voltage circuitry. All the designed blocks were targeted for 5V functions, basic circuitry is used (compactors, integrators, mirror current, etc).

Simulation and experimental results show that the ASIC integrated functions are faster than the PCB integration. Before reaching to this conclusion a proper comparison should be done for each method under the same condition. Unfortunately, simulation finds difficulties to converge sometime, and the availability of components wasn't a great fit. Hence, components with main parameters were compared, and the diversity of the components give a different perspective towards a better detection system.

The gate charge shows a detection time of 120ns at 600V with a  $R_{G\_Ext} = 10\Omega$ , C2M0080120 ( $C_{iss} = 1130pF$ ,  $C_{oss} = 92pF$ ); experimentally validated. On the other hand, by simulation the third method shows a detection time of 60ns at 600V a  $R_{G\_Ext} = 10\Omega$ , C3M0075120 ( $C_{iss} = 1390pF$ ,  $C_{oss} = 58pF$ ). And last the gate derivation method which is validated by simulation as well at 600V,  $R_{G\_Ext} = 10\Omega$  with C2M0025120 ( $C_{iss} = 2788pF$ ,  $C_{oss} = 220pF$ ), detecting at 60ns.

The speed of the detection as mentioned depends on several things:

- The propagation time of the circuitry,
- The gate resistor and capacitor,
- $V_{Bus}$ ,  $I_{Load}$ , SR,  $g_{fs}$ , ...
- And, Mainly the set of the reference levels,

The three methods depend on when the gate voltage rises above the reference level  $V_{Ref}$ , so the lower this reference, the earliest the detection, with the only condition of the  $V_{GS} > V_{GS\_M}$ . So which of these approaches is the fastest?

The gate method shows that reducing  $V_{Ref}$  is difficult due to the limitation of the  $Q_G$  curve (oscillation in the beginning of the integration can be high). On the other hand, the gate derivation method shows that the dip approach is more robust than the slope approach. Using



2D diagnosis once again proves it is the perfect candidate for short-circuit detection and protection. These circuits can be combined with cleverness in a single chip, in order to cover all the tracks, and don't miss the SC.

There is still a wide range of changes and optimization that can be added to the circuit. Moreover, the protection delays can be strongly reduced. At the end, the goal is to integrate all the functions in the dedicated gate driver IC in CMOS technology, for fast detection. It is important to note that with such a fast protection, the fault current is limited to 135A (or lower) against nearly 290A (or higher) with no protection. In such short time and at such low current value, the dynamic temperature of the chip remains lower than the melting temperature of the aluminum to metal of the die, which would allow a large number of repeated short-circuits without ageing effect, and reducing the chances to damage the component sooner.

## Conclusion & Outlook

In a context of increasing electrification of our economy (transport, production of renewable energy, digitalization of services, automation, automotive, and railway), static converters based on power electronics will be required to transit and condition a large part of the energy produced and consumed on earth. The losses of these converters will lead to an oversizing of the resources of energy production, in particular renewable ones. The efficiency, power density and reliability of static converters are the main challenges. To improve the efficiency, wide-band gap semiconductor power transistors (GaN and SiC) have been introduced to the market. By increasing switching speeds, these components (mainly MOSFET SiC and HEMT GaN) have less losses and greater compactness, which offer higher switching frequencies. On the other hand, the maintenance costs of power electronics are largely related to the reliability of the power transistors. In particular, during operation events generally external to the converter (EMI disturbances, human error, environment), which can disturb the system and cause extreme regimes (avalanche, short-circuit) on the power transistors which can lead to their failure. These extreme regimes are critical because they cannot be avoided by preventive maintenance of equipment and can cause cascades of failures that can lead to a failure compromise the integrity of the system and its users. The robustness is therefore an important characteristic of the reliability of the power converters. In particular, short-circuit robustness is most critical compared to avalanche both in terms of occurrence in systems and levels of electro-thermal stresses on the transistor.

The SiC MOSFET is of great interest for increasing the efficiency of PV and wind turbine applications where maintenance and cost requirements are critical. Its short-circuit robustness is therefore of major interest for the development of these industries. Moreover, the short-circuit withstand capability of SiC MOSFETs is short compared to Si IGBTs. Therefore, the detection techniques used for Si IGBT are no longer of great use. Adaptation and new circuits are required.

Therefore, this thesis is a contribution to the protection methods of SiC MOSFETs under short-circuit, with the goal to increase detection speed, robustness and safety. The objective is to ensure safe and healthy static converters to the market, encouraging the use of SiC MOSFET power transistors.

In order to protect and reduce the stress under short-circuit events of a given SiC MOSFET, several ways are offered.

- The straightforward solution in order to reduce the stress of the power transistor is to protect the device as early as possible, which requires a detection circuit (the main work of this thesis). In order to do so, an overview and modeling of the SiC MOSFET were led, under normal behavior and short-circuit behavior. Several switching parameters showed promising opportunities, which led to different topologies in order to protect the SiC MOSFET. These topologies were discussed, designed; validated by simulation

and then experimentation. Not all the circuits had the chance to be experimentally validate due to time constraints. Each circuit shows pros and cons.

- The non-straightforward solution, is to make a physical change to the structure of the SiC MOSFET. Physical changes require non-standard chip, which can be difficult to market it; as presented in the chap.I changes can be made the structure of the SiC MOSFET as reducing the oxide doping level.
- On the other hand, electrical changes can be made as well, in order to reduce the stress under SC, by changing the typical gate driver structure; as the multi-modular gate driver, or using other techniques.

In future works, the merge of this solution can open new opportunities by reducing the stress on the SiC MOSFET, reducing the drain current surge, and protecting as fast as possible; in order to have larger SC withstand capability time, and offer longer lifetime durability.

The thesis followed a sequence of work. The sequence started with a full understanding of the environment of the SiC MOSFET, and its behavior under normal operation versus short circuit operation. As well as, the market positioning of SiC MOSFET gate driver. This study including the state of the art was covered in chap.I. This study led us to different criteria in order to seize our active gate driver, adapted for short-circuit detection and protection circuit. The active gate driver was experimentally validated. The AGD showed in experiment great results under different circumstances. The AGD still can be enhanced and optimized, specially the numerous enable pads, and the layout design. The one should note the complexity behind the layout can lead easily to high parasitic resistance and capacitance. The AGD was developed and presented in chapt.II, along with the exploratory multi-modular active gate driver. The MMGD should be experimentally validated and compared with a discrete solution. Both drivers were integrated in the same layout run, respectively  $2414\mu\text{m} \times 1559\mu\text{m}$  //  $2400\mu\text{m} \times 1865\mu\text{m}$ , with different packages, QFN40 6mm\*6mm. The size of the PCB host of the chip is 6cm\*6cm. In chap.III, the detection methods are presented and experimentally validated. First, the gate charge method is developed as a benchmark, in order to be able to compare with the other detection methods. Under HSF, this detection showed great performance with a 130ns detection time. In order to enhance this method, the reference level set can be adaptable for different parameter variation. Moreover, the detection circuit under FUL is in progress. On the other hand, the second method developed the gate derivation method. This method which is integrated in CMOS technology is also experimentally validated. Due to the impossibility to make changes in the CMOS chip after fabrication, the gate derivation circuit is simplified using a capacitor and sense resistor to generate the derivative gate-source signal. Therefore, a focused study should be led in order to cover this method, and offer better and optimized circuit with less SNR. Moreover, few mistakes in the design should be rectified, as the output circuitry of the detection flag. And in order to gain in the speed of the detection and have high robustness, the reference levels set can be adapted as well. This detection time in this method cannot be defined due to the error at the output of the detection circuit, using a small 5V logic inverter. Third the last detection method,



which shows high robustness compared to the other methods, for a wide parameter variation, which requires only low-fixed reference levels. This method is under fabrication.

In summary, few things are required in order to fully grasp the developed detection methods.

- To adapt the circuit to different parameters variation, mainly by designing adapted reference level set, especially for the gate charge and gate derivation method.
- To optimize and to enhance the circuits, especially the gate derivation method.
- To fully validate the circuit by leading experiments under extreme operations, especially for the third method, which showed better robustness.
- To develop detection circuit using the gate charge and gate derivation methods under Fault under load SC type.
- To adapt the detection circuit for power modules, and multilevel structures.
- To further optimize the configuration of the techniques (e.g. threshold levels, filter parameters, ...) and more generally, to reduce the number of PADs used for configuration, towards a compact single Chip
- To adapt these methods for GaN power transistors.

The active gate driver could be further enhanced, and could merge several detection circuits. The AGD still have a long journey in front of it, by integrating more functions as power supply, isolation, high side gate driver, etc... Moreover, the AGD can be furthermore integrated towards in-package or on-chip solution. The one should keep in mind, more and more functions can be and should be integrated in gate driver, in order to present safe, healthy and smaller AGD. Different diagnostic function can be added as well, as permanent diagnosis on the threshold level, gate current leakage, internal propagation time, voltage level-set or the temperature of the device, on-state and off-state. Moreover, GaN's dynamics and figure of merits may lead to take over the market, which push the research into investing more time and developing in safe AGD with high diagnosis and monitoring functions.

## Appendix A

In order to be able to simulate the behavior of the AGD under power transistors effects, the power transistor model should be integrated in cadence. In order to do so; Wolfspeed provides files in format “.lib” that illustrate the sub-models and the behavior of the SiC MOSFET. This library files are commonly used under LTSpice™. The sub-model code is translated in blocks in Fig.A. 1, in order to clarify nodes connectives and to have an organized schematic netlist. Therefore, two possibilities are presented, either the microelectronic models must be imported in LTSpice™ or the power device model “.lib” file must be translated to other format adapted to Cadence such as “.scs”. Thanks to a team work [Bau Plinio & Barazi Yazan], in order to convert library files .lib to specter language “.scs”, few steps are required:

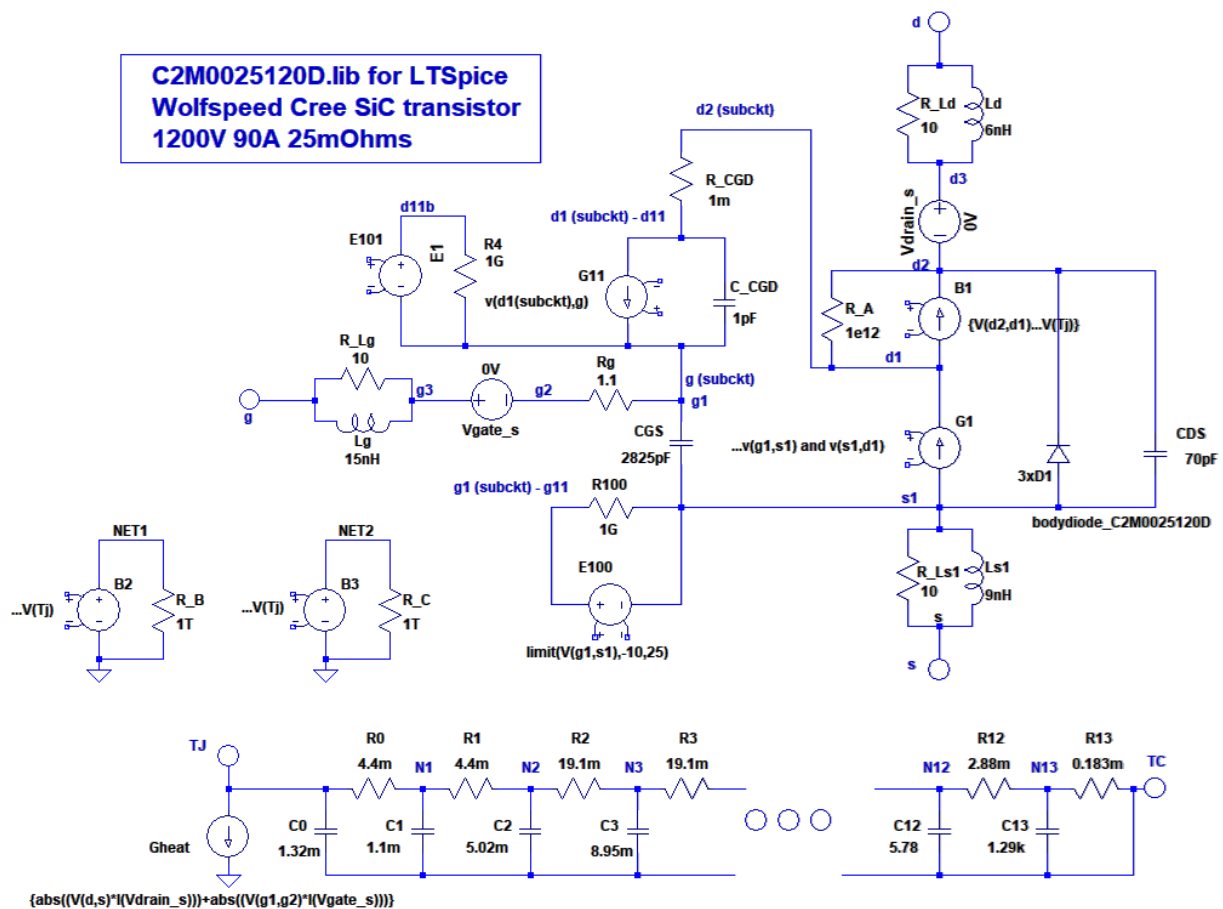


Fig.A. 1. Illustration of the netlist file .lib in circuit elements for the SiC MOSFET C2M0025120D.

- 1) Get familiar with .lib language,
- 2) Identification of the primary and secondary nodes. As well as differentiate between the sub-circuit nodes and primary-circuit nodes. Name change might be necessary.
- 3) Illustrate the netlist in a schematic.
- 4) Translate the “.lib” to specter language “.scs”
- 5) In cadence: Create a schematic. Then, Create an instance (under library analogLib find a cell with a name “scasubckt” or similar depending on the version), Name of the model should

much the “.scs” file name, and point to the path of the file. Change the number of pins to the number of main nodes on your “.scs” file.

After following those steps, specter language requires few changes:

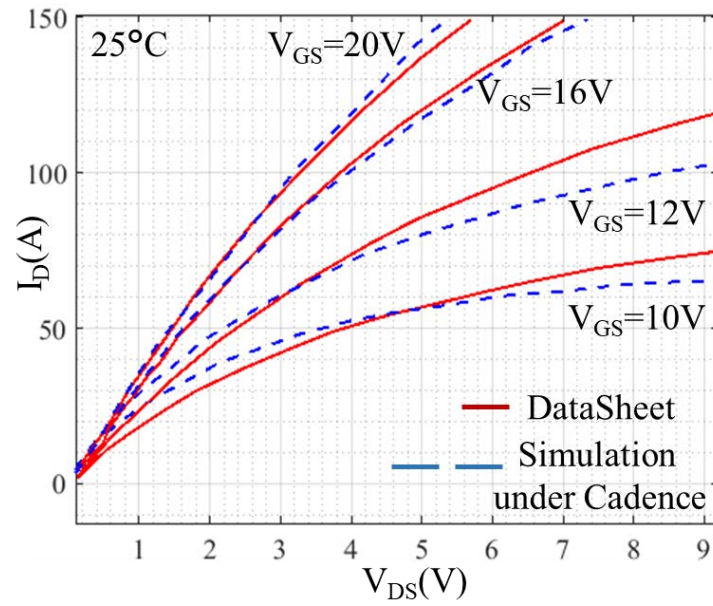
- Add “simulator lang=spectre” as first line
- Change sub-circuit to subckt. Main circuit is considered as a sub-circuit, therefore others sub-circuit are not allowed. All the sub-circuit in .lib should be developed in the main circuit. (Be aware of nodes names).
- The sub-circuit name must match the file name.
- Syntax changes, Model changes, Tab.A. 1.

For other syntax changes or mathematical syntax changes use [175].

**Tab.A. 1.** Syntax Translation

LTSpice™ file (.lib)	Cadence Spectrum™ file (.scs)
{}	()
.param	parameters
.ends	ends (subcircuit name)
TANH(...)	tanh(...)
If	?
*	//
, (=ELSE inside the if loop)	: (=ELSE inside the if loop)
Rth_1 T11 TJ {0.011}	Rth_1 (T11 TJ) resistor r=(0.011)
Cth_1 0 TJ {4.25e-5}	Cth_1 (T11 TJ) capacitor c=(4.25e-5)
G1 d2 d1 Value {V(d1,s)}	G1 (d2 d1) bsource i=(v(d1,s))
Limit function	If function or max value as a parameter of a current source.
.model bodydiode_C3M0016120K d(is=158.89n cjo=1119p)	bodydiode_C3M0016120K (s d2) d01 model d01 diode is=158.89e-9 cjo=1119e- 12

After these steps and adaptations, the power model behavior is validated with comparisons between simulation results and data-sheet. Fig.A. 2 presents ( $I_D$ - $V_{DS}$ ) characteristic plot under Cadence and data-sheet for the C2M0025120D component. Other models have been translated with success and other with convergence problems. Some differences have been observed in the simulations, when the device did not completely match with the datasheet. This unmatched sequences are observed by the manufacturer models provided, which has the same behavior under LTSpice.



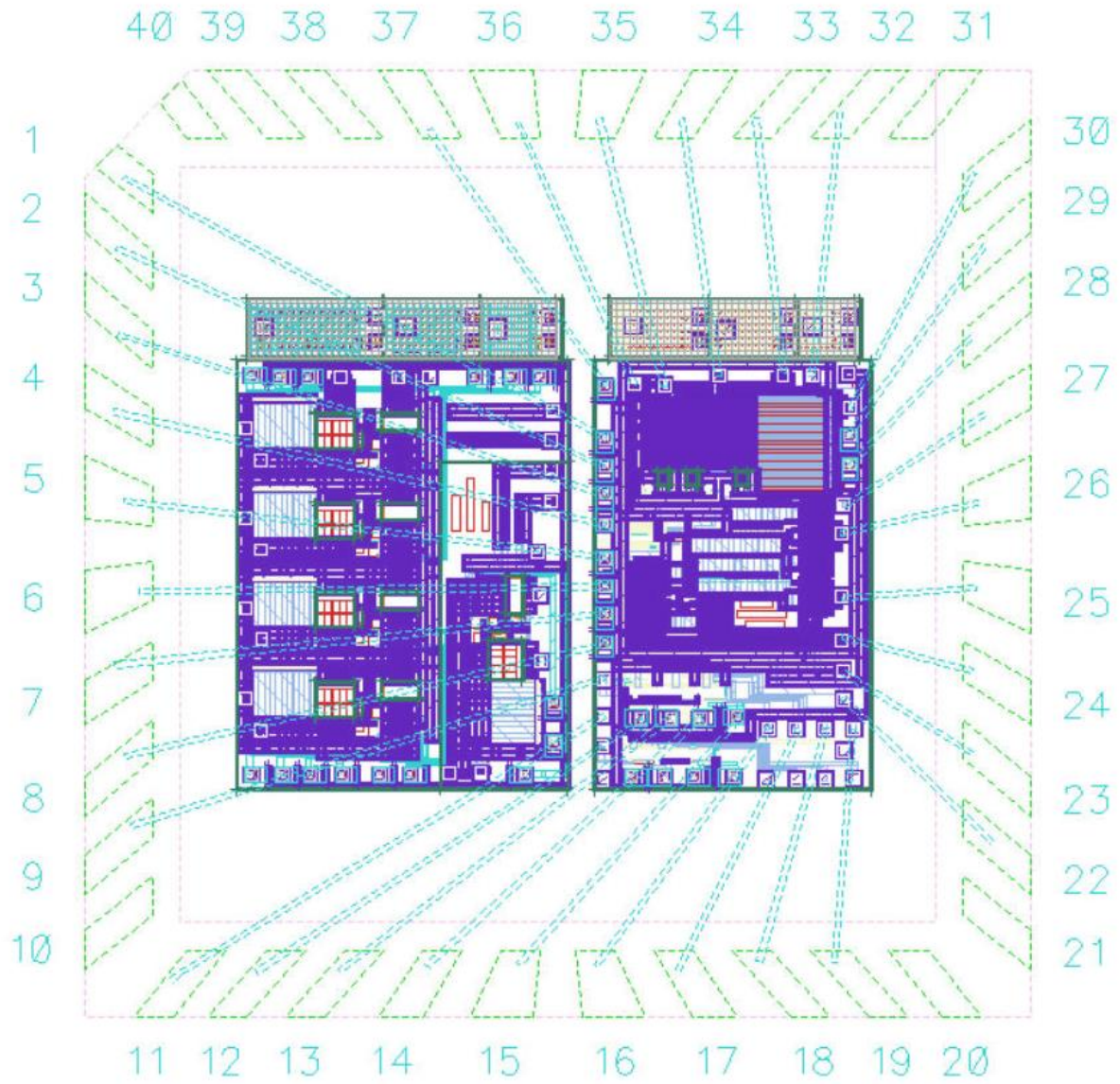
**Fig.A. 2.** Comparison of the device C2M0025120D ( $I_D$ - $V_{DS}$ ) characteristics under Cadence simulation and datasheet

## Appendix B

Core Module	Additional Modules	
Wafer Start	Handle wafer contact	HWC
	N-buried Implant	NBUR
Epitaxy		
Active area	Deep trench Isolations	DTI
SUB	HV Pwell	HVP
	SJNP Implant	1XN
	HV Nwell	HVN
	SJPN Implant	1XP
	NBUF Implant	NBUF
	N-drain extension implant	NHVA
	P-drain extension implant	PHVA
	NPN bipolar implant	BJTC
	PNP bipolar implant	BJTA
5.0V Nwell		
5.0V Pwell	PZENER Implant	DIODEB
	NZENER Implant	DIODEC
	nDMOS Pwell	NHVA, DIODEA
1.8V Nwell		LP5MOS, DNC, DPC (MOSS)
1.8V Pwell	Depletion Implant	DEPL
	1.8V low Vt well	LVT (LP5MOS only)
1.8V gate oxide		LP5MOS only
5.0V gate oxide		
Poly silicon gate		
1.8V NMOS LDD		LP5MOS, HRPOLY
1.8V PMOS LDD		LP5MOS only
5.0V NMOS LDD		
5.0V PMOS LDD		
Source/Drain Implants	MR poly implant	MRPOLY
Salicidation		
Contact		
Metal 1	High Cap /Double MIM Implant	DMIM, DMIMH
Via 1	High Cap /Triple MIM Implant	TMIM, TMIMH
Metal 2	Via 2	MET3
	Metal 3	
	High Cap /Double MIM Implant	DMIM, DMIMH
	High Cap /Triple MIM Implant	TMIM, TMIMH
	Via 3	
	Metal 4	MET4
	High Cap /Triple MIM Implant	TMIM, TMIMH
	Via 4	
	Metal 5	MET5
	High Cap /MIM Implant	MIM, MIMH
	Top Via	METMID
	Top metal	
	Thick Via	METTHK
	Thick Metal	
	Planarized Passivation	FLATPV
PAD	Polyimide	PIMIDE
	Bottom dielectric	BOTDIE
	Thick copper metal	THKCOP

Fig.B. 1. XT018 different layers divided in core and additional modules





**Fig.B. 2.** Bonding diagram of the active gate driver using a QFN40, 6mm\*6mm

## Appendix C

### Chapitre I : Les défis associés à la commande des MOSFETs SiC

*Résumé : Dans ce premier chapitre, nous décrivons un bref aperçu de l'état de l'art des transistors de puissance. Nous présentons également une vue d'ensemble de la commande, gate driver et des défis rencontrés par le gate driver pour les dispositifs de puissance SiC. Ainsi, les fonctions de surveillance et de contrôle autour des transistors de puissance sont abordés. Ainsi, une étude approfondie de l'état de l'art du comportement des courts-circuits et des méthodes de détection est développée.*

Les activités de l'électronique de puissance consistent à fournir la capacité de transférer de l'énergie à une ou plusieurs charges électriques à partir d'une ou plusieurs sources d'énergie primaire. Afin de pouvoir contrôler, moduler et transférer l'énergie, les convertisseurs de puissance doivent utiliser au moins un interrupteur de puissance contrôlé. À cette fin, il existe une large gamme de commutateurs en technologie silicium (thyristor GTO, IGBT, MOSFET), ainsi que des composants semi-conducteurs à large bande interdite (SiC, GaN) disponibles auprès de divers fabricants et instituts de recherche, Figure 1. Les transistors à grille isolée tels que les MOSFET ou les IGBT doivent être pilotés par un circuit de commande, appelé "gate driver". Le but du circuit pilote de grille est de fournir, de contrôler et de gérer la charge et/ou la décharge de l'électrode de grille du transistor de puissance, et de permettre les changements d'état (de On à Off ou vice versa).

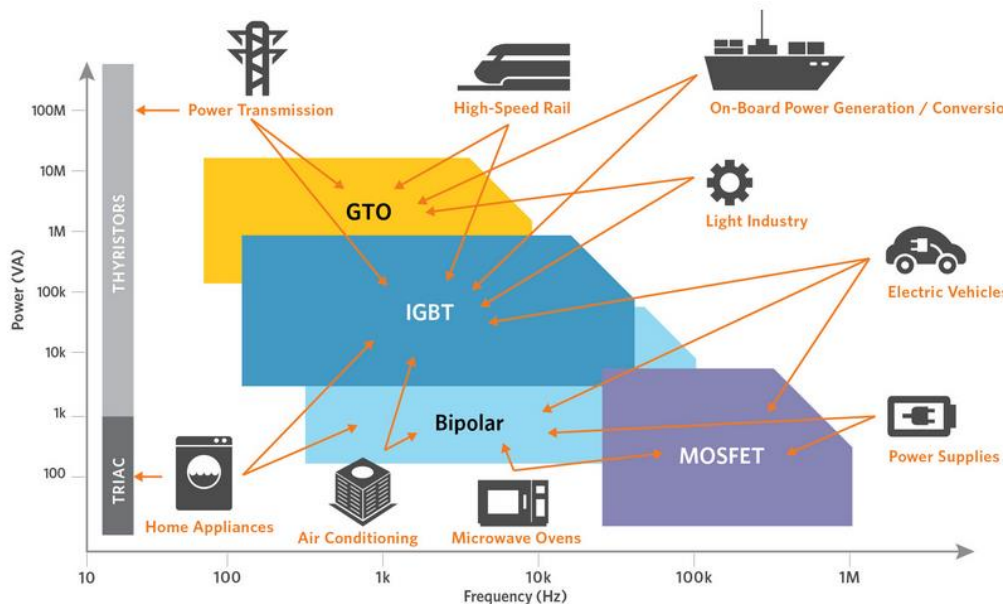


Figure 1. Évolution et Domaines d'applications ; des semi-conducteurs discrets de puissance [1].

Les matériaux semi-conducteurs à large bande interdite, tels que le carbure de silicium (SiC), ont connu une évolution considérable ces dernières années. Les dispositifs à semi-conducteurs de puissance, tels que les transistors bipolaires à grille isolée (IGBT) et les dispositifs en silicium à super-jonction (SJ-MOSFET), sont limités en termes de vitesse de commutation

maximale et, plus généralement, avec des facteurs de mérite proches des limites théoriques du silicium [1], Figure 2. Par conséquent, les dispositifs de puissance en silicium présentent des pertes de commutation élevées et des systèmes de gestion thermique importants et coûteux, ce qui entraîne des limites en termes d'efficacité maximale du convertisseur et de fréquence de commutation. En revanche, les MOSFETs en SiC sont des dispositifs semi-conducteurs de puissance prometteurs pour les convertisseurs à haute densité, avec de faibles pertes de conduction et de commutation et une grande stabilité à la température [2]. À mesure que les MOSFETs SiC gagnent en maturité et que leur coût diminue avec le temps, les MOSFETs SiC devraient être adaptés et utilisés dans de plus en plus d'applications.

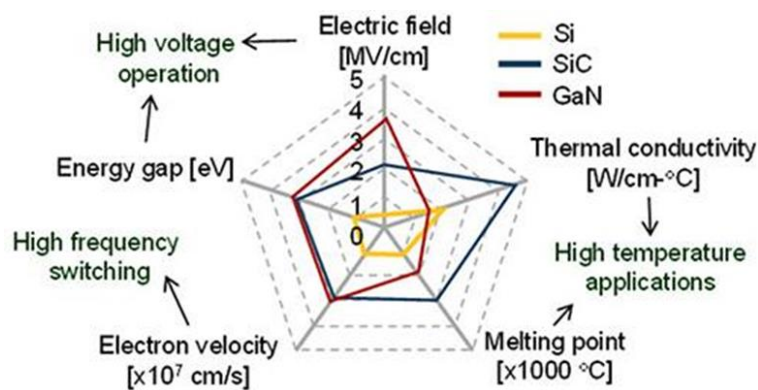


Figure 2. Propriétés matérielles du silicium, du carbure de silicium et du GaN

Cependant, les densités de puissance plus élevées qui sont appliquées à la puce posent la question de la durée pendant laquelle un dispositif de puissance en SiC peut supporter un défaut de court-circuit. Quelle que soit la robustesse du court-circuit, le défaut de court-circuit doit être désactivé dès qu'il est détecté afin de préserver le dispositif de la dégradation et d'éventuelles occurrences répétées de court-circuit. La tenue de court-circuit (SC) des MOSFETs en SiC est inférieure à celle des dispositifs en silicium [3], Figure 3. Les convertisseurs de puissance conçus avec ces composants sont donc moins robustes. Cette faiblesse doit être compensée par une protection dont le retard ne doit pas dépasser  $T_{SC}/2$ , comme c'est le cas aujourd'hui pour les IGBTs silicium, ou encore moins si la robustesse aux SC répétés est requise.

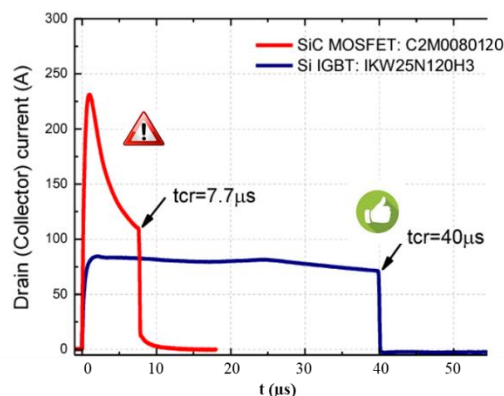


Figure 3. Formes d'ondes expérimentales de courant sous court-circuit critique pour les MOSFET en SiC et les IGBT en Si (SiC MOSFET:  $V_{DS}=600V$ ,  $V_{GS}=20V$ ; Si IGBT:  $V_{CE}=600V$ ,  $V_{GE}=15V$ ) [4]

Les dispositifs à semi-conducteurs de puissance sont utilisés dans diverses applications industrielles, notamment les entraînements de moteurs, les chargeurs de batterie, les alimentations à découpage et les convertisseurs, avec un comportement typique (NTO), Figure 4. Ces dispositifs sont exposés à plusieurs types de court-circuit (SC). Le défaut d'interrupteur dur (HSF, SC type I) et le défaut sous charge (FUL, SC type II) sont les deux principaux comportements de défaut, Figure 5 Figure 6. La sécurité est nécessaire pour ces applications typiques. Le HSF se produit lorsque l'interrupteur se met en marche avec une tension de bus permanente à ses bornes, généralement causée par des signaux de commande défectueux. En revanche, la condition de défaut de type II apparaît après le cycle de commutation des trois intervalles de temps normaux, notamment après  $t_4$ , où le MOSFET est en mode ohmique à l'état passant  $V_{GS} = V_{Drv+}$  et  $I_{DS} = \text{charge}$ .

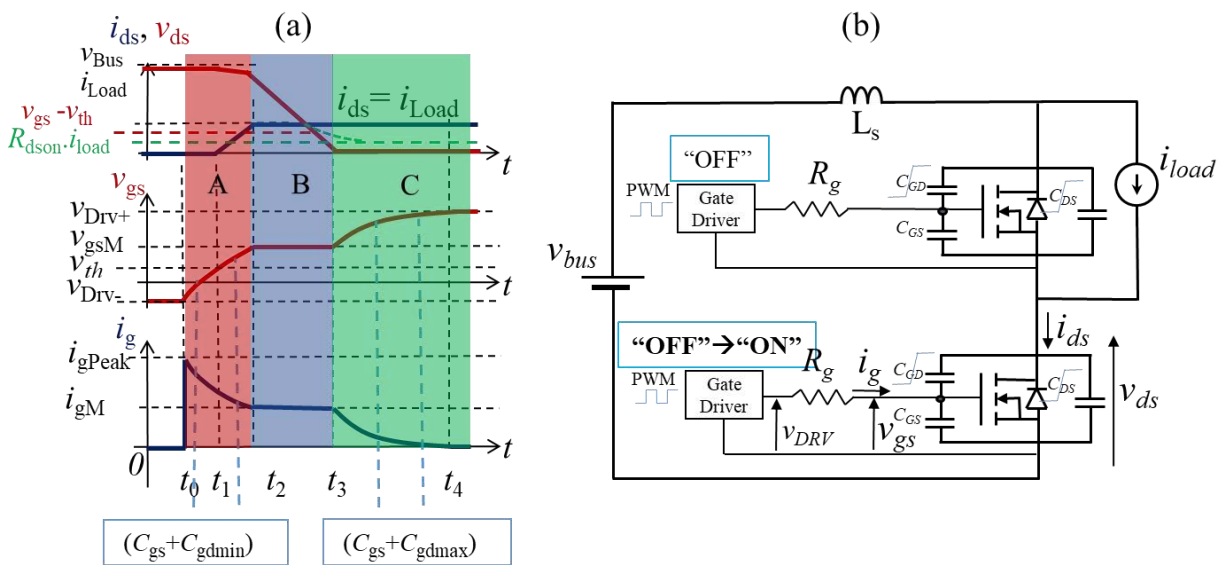


Figure 4. (a). Caractéristiques de commutation du MOSFET SiC dans les conditions NTO. (b). Circuit équivalent du demi-pont.

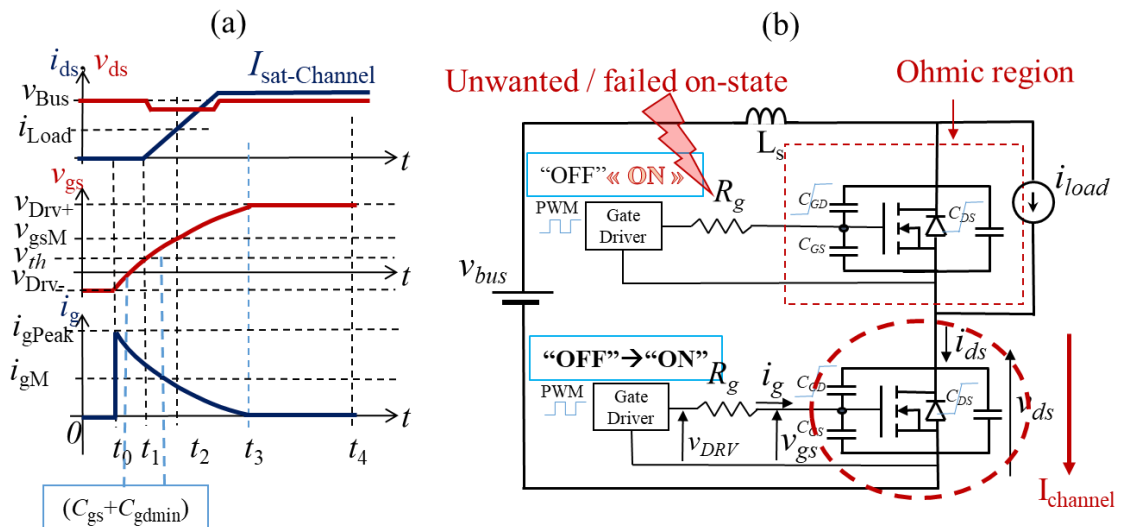


Figure 5. Caractéristiques de commutation du MOSFET SiC sous des conditions de HSF. (b). Circuit équivalent du demi-pont.



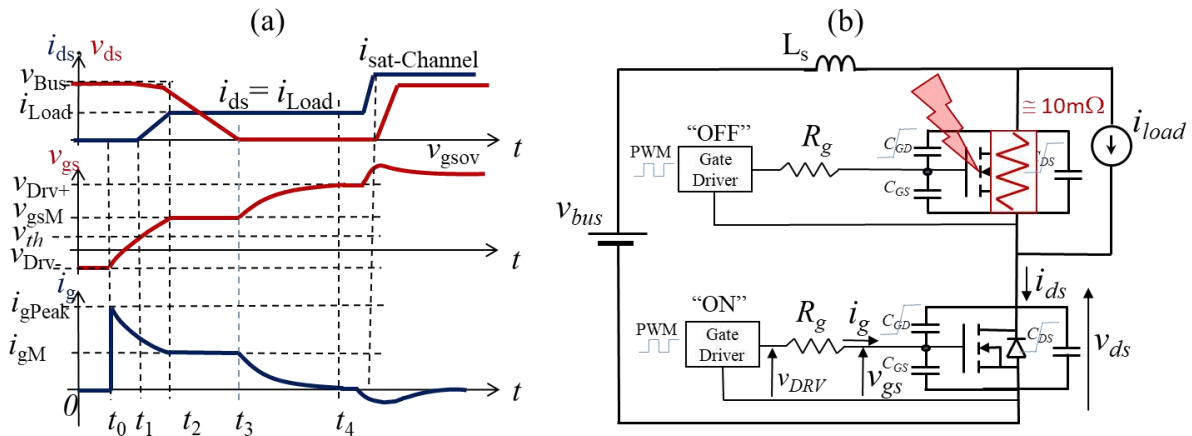


Figure 6. . Caractéristiques de commutation du MOSFET SiC sous des conditions de FUL. (b). Circuit équivalent du demi-pont.

On peut remarquer brièvement, l'absence du plateau Miller, le changement sur les pentes au niveau de la tension grille-source, le changement au niveau du  $dV_{DS}/dt$  et les surintensités au niveau du drain qui sont observées sous SC-HSF et SC-FUL. Comme il sera présenté ci-après, ce comportement distinctif est utilisé pour détecter et protéger le MOSFET SiC en cas de HSF. Différentes méthodes de surveillance et de protection des MOSFETs SiC sont étudiées et développées. L'objectif est de déterminer à quelle vitesse un défaut de court-circuit peut être détecté et à quelle vitesse il peut être désactivé. C'est pourquoi des analyses et des comparaisons détaillées entre les méthodes de détection des SC sont présentées.

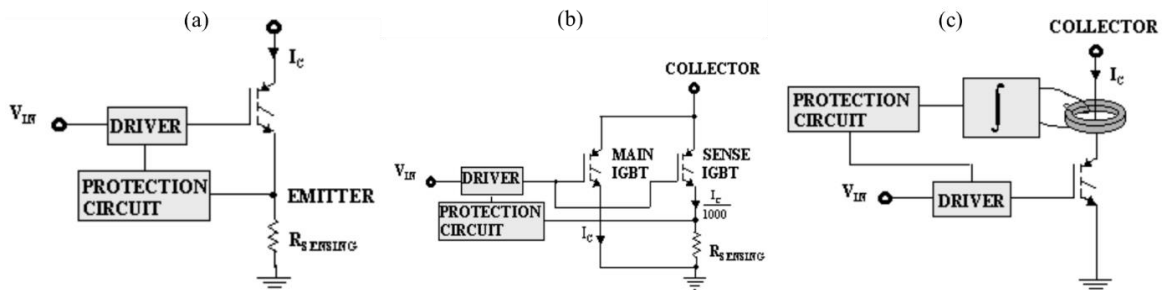


Figure 7. Trois schémas de méthodes de surveillance (a). Méthode de la résistance shunt (b). Méthode SenseFet. (c). Méthode du transformateur [5].

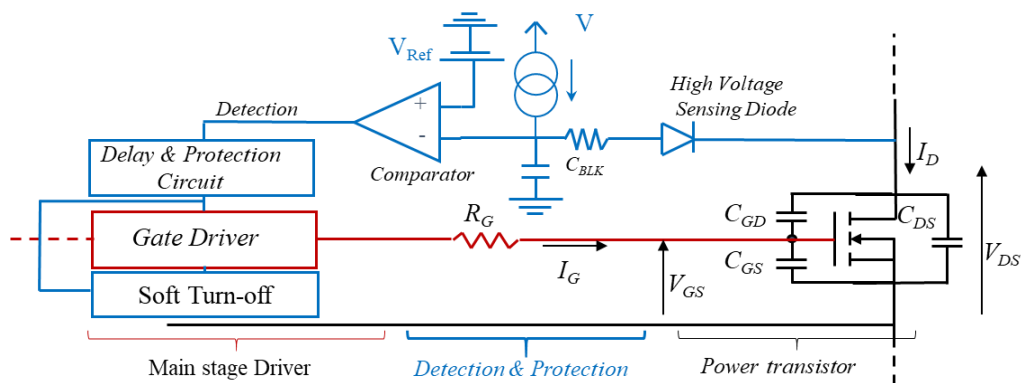


Figure 8. Schémas de la méthode de désaturation



Plusieurs types de méthodes de détection SC ont été proposés pour IGBTs silicium et MOSFETs SiC [6]. La plupart des techniques reposent sur la détection d'un niveau de tension ou de courant drain-source de valeur anormale par rapport à un seuil [7]. La détection en tension est bien adaptée aux composants bipolaires tels que l'IGBT mais nécessite l'utilisation d'une diode rapide haute tension tandis que la détection en courant utilisée pour le MOSFET et parfois pour l'IGBT requiert une puce spécialement conçue avec miroir de courant [8], une électrode de mesure supplémentaire et aussi une fenêtre de masquage relativement longue est nécessaire dans le cas de la méthode de détection de la tension drain-source afin d'atteindre un régime ohmique stable après le cycle de commutation [9], Figure 7 et Figure 8.

Différemment des méthodes précédentes, la méthode étudiée dépend de l'intégration rapide du courant de grille dans la séquence de charge de la grille à l'amorçage. La méthode connue sous le nom « gate charge » a déjà fait l'objet d'articles pour les IGBTs Silicium [10] et quelques résultats partiels pour les MOSFETs SiC en termes de performances et de mise en œuvre pratique [11], Figure 9.

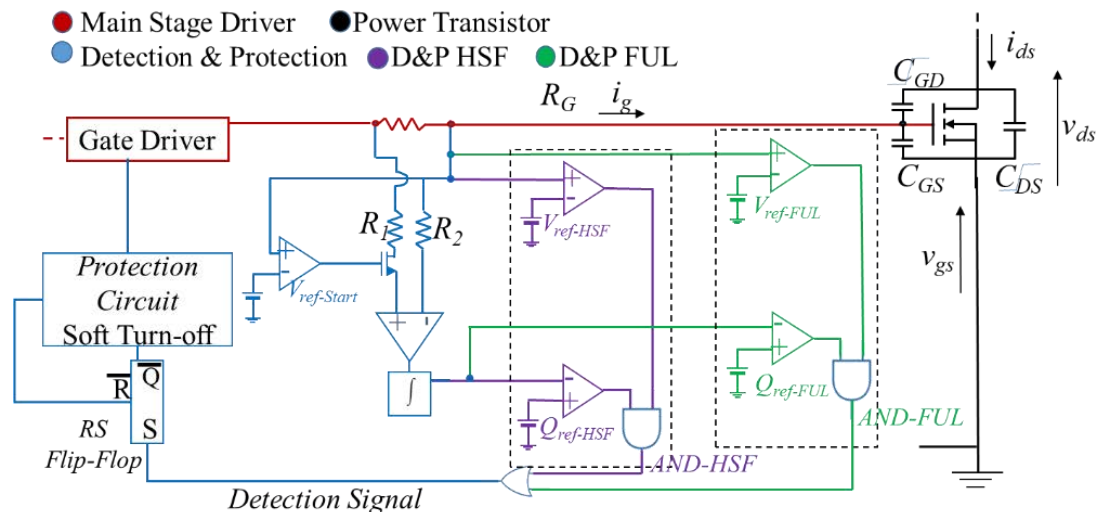


Figure 9. Schémas de la méthode gate charge

Afin de concevoir entièrement un driver de grille avec différentes fonctions orientées protection et sécurité, dédié aux MOSFETs SiC, la caractérisation électrique des MOSFETs SiC est obligatoire. Les principes de base des pilotes de grille et leurs principales exigences sont étudiés. Différentes architectures de commande de grille sont examinées, afin de se familiariser avec l'environnement des fonctions de détection des SC.

## Chapter II: Conception de commande de grille intégrées en technologie CMOS SOI 0,18 $\mu$ m pour un dispositif de puissance SiC MOSFET

*Après avoir étudié les fonctions essentielles du gate driver, et les niveaux d'intégration, chapitre I, cette étude se concentre sur le buffer de sortie pour contrôler le transistor de puissance. Deux architectures de buffer sont proposées. La première est une solution simple, adaptée aux besoins de la réalisation de cette thèse. En d'autres termes, peu de fonctions*

complémentaires ont été ajoutées au buffer, et une nouvelle fonction de détection de court-circuit est conçue et intégrée, afin d'avoir un gate driver digne de ce nom. La fonction de détection de court-circuit est présentée dans le troisième chapitre. Le deuxième buffer, est une étude exploratoire qui se concentre sur une architecture modulaire pour un contrôle rapproché à plusieurs niveaux de tension de polarisation en tirant parti de l'isolation SOI et des transistors CMOS basse tension pour piloter les MOSFETs SiC et améliorer leur robustesse et leur fiabilité grâce à une sélection active et dynamique à plusieurs niveaux des séquences de commutation et des états de marche/arrêt. La structure contient plusieurs buffers en série afin de disposer d'un active gate driver modulaire multiniveau MMAGD.

### **Active Gate Driver :**

Les transistors MOSFET SiC présentent un meilleur facteur de mérite ( $R_{DS\_ON} \times Q_G$ ) que les transistors IGBT Si. Ils permettent un fonctionnement à haute fréquence avec un excellent niveau de performance, ce qui rend les convertisseurs de puissance plus petits, plus rapides et plus efficaces. Par conséquent, le Tableau 1 **Erreur ! Source du renvoi introuvable.** présente le dispositif de puissance ciblé à contrôler. Les dispositifs sont issus du fabricant WolfSpeed™, qui dispose d'un large éventail de choix de calibres en matière de courant et de tension. Le choix de ces dispositifs est basé sur leur facteur de mérite ( $R_{DS\_ON} \times Q_G$ ), leur capacité d'entrée (utile pour la détection de court-circuit, voir le chapitre III) et des études ont déjà été menées sur différents aspects de ces transistors au sein du laboratoire. L'un des principaux axes de cette thèse est la surveillance des MOSFETs en SiC. Par conséquent, le pilote de grille devrait être adapté à cette fonction, et devrait pouvoir montrer des résultats opérationnels prometteurs pour une large gamme de dispositifs MOSFETs SiC disponibles sur le marché. La portée de cette étude n'inclura pas les fonctions d'isolation et les alimentations électriques pour le gate driver.

**Tableau 1. Différents transistors de puissance SiC MOSFETs pour la 2ème et 3ème génération**

Paramètre	C3M	C3M	C3M	C3M	C2M	C2M
typique	0120090J	0075120K	0032120K	0016120K	0025120D	0040120D
$V_{DS}$ (V)	900	1200	1200	1200	1200	1200
$I_D$ (A)	22	30	63	115	90	63
$R_{DS\_ON}$	120m $\Omega$	75m $\Omega$	32m $\Omega$	16m $\Omega$	25m $\Omega$	40m $\Omega$
$V_{GS\_op}$ (V)	-4/15	-4/15	-4V/15	-4V/15	-5/20	-5/20
$V_{th}$ (V)	2.1	2.5	2.5	2.5	2.6	2.6
$R_{G\_INT}$	16 $\Omega$	10.5 $\Omega$	1.7 $\Omega$	2.6 $\Omega$	1.1 $\Omega$	1.8 $\Omega$
$R_{G\_EXT\_op}$	2.5 to 20 $\Omega$	0 to 20 $\Omega$	2.5 to 20 $\Omega$	0 to 20 $\Omega$	2.5 to 20 $\Omega$	2.5 to 20 $\Omega$
$Q_G$ (nC)	17.3	51	118	211	161	115
$C_{ISS}$ (pF)	350	1350	3357	6085	2788	1893
$C_{RSS}$ (pF)	3	3	8	13	15	10
$t_r/t_f$	9/5ns	11/11ns	18/9ns	33/13ns	32/28ns	52/34ns

$t_{d\_on}/t_{d\_off}$	12/15ns	22/33ns	25/32ns	34/65ns	14/29ns	15/26ns
$\tau_{iss}@R_G=10\Omega$	3.5ns	13.5ns	33.5ns	60.8ns	27.9ns	18.9ns
$i_{G\_Peak}$ (A)	3.2	1.15	3.57	5.77	5.5	4.5

Le choix des gammes de transistors de puissance et l'étude analytique réalisée, ont conduit à un ensemble de gammes de tension de commande, avec un choix de résistance externe-interne. De plus, un command de grille avec des courants de source et de sink importants donnera de grandes surfaces de silicium. Par conséquent, le courant de crête de sortie visé est d'environ 3A. Afin d'étayer nos choix, un tableau de référence pour les différents drivers de grille est présenté dans le Tableau 2. Ces pilotes de grille sont des pilotes isolés à canal unique disponibles dans le commerce. Ils sont comparés en ce qui concerne leur courant crête, leur tension d'attaque, leur délai de propagation et leur temps de montée et de descente pour une capacité de charge donnée.

Tableau 2. Comparaison des gate driver commerciaux avec notre cahier de charge fixer

Driver	Silicon Labs SI8261BAC-C-IS	Infineon IED020I12	TI UCC27525	IXYS IXD614	<a href="#">Barazi</a>
$I_{Peak}$	±4A	±2.4A	±5A	±14A	±3A
$V_{Drv}$	0/30V	-12/20V	-4.5/18V	-4.5/35V	-5/35V
$t_p$	40ns	160ns	17ns	50ns	<30ns
	$C_L=200pF$	$C_L=100pF$	$C_L=1.8nF$	$C_L=15nF$	$C_L=1.5nF$
$t_r/t_f$	5.5/8.5ns	30/50ns	7/6ns	25/18ns	<10ns
$T^\circ$	125°C	150°C	125°C	125°C	-40<T°<175
Year	2011	2017	2015	2017	2020

Les tendances récentes pour les gate drivers intégrés sont d'intégrer une variété de fonctions complexes pour améliorer encore les performances de la gestion de la commutation de puissance. La méthode de désaturation  $V_{DS}$  est classiquement utilisée pour les IGBTs Si et aujourd'hui, pour les MOSFETs SiC à défaut d'alternative performante et économique. Rappelons que cette méthode nécessite une diode rapide haute tension, chemin sensible en présence d'un  $dv/dt$  entre le circuit de puissance et le circuit de commande de grille, ce qui rend cette méthode délicate et difficile à intégrer dans une technologie CMOS basse tension. Pour surmonter ces problèmes, un circuit de commande rapproché actif et rapide (« active gate driver ») est conçu en technologie CMOS pour détecter le SC et protéger les MOSFETs SiC, en utilisant uniquement des fonctions analogiques basse tension (transistors 5V et 40V).

Le prototype du circuit intégré est basé sur la technologie SOI CMOS 0,18  $\mu m$  XT018 de XFAB. Cette technologie qui combine les avantages des plaquettes SOI avec une isolation profonde par DTI (Deep Trench Isolation) et six couches métalliques de 0,18  $\mu m$ , ainsi que des transistors haute tension jusqu'à 200V et un fonctionnement à haute température (175 à 225°C). Ces propriétés facilitent la conception de ce circuit intégré, afin de fournir un courant élevé et

de piloter le transistor de puissance avec la tension de grille exigée [10]. Ce gate driver comprend plusieurs fonctions, Figure 10:

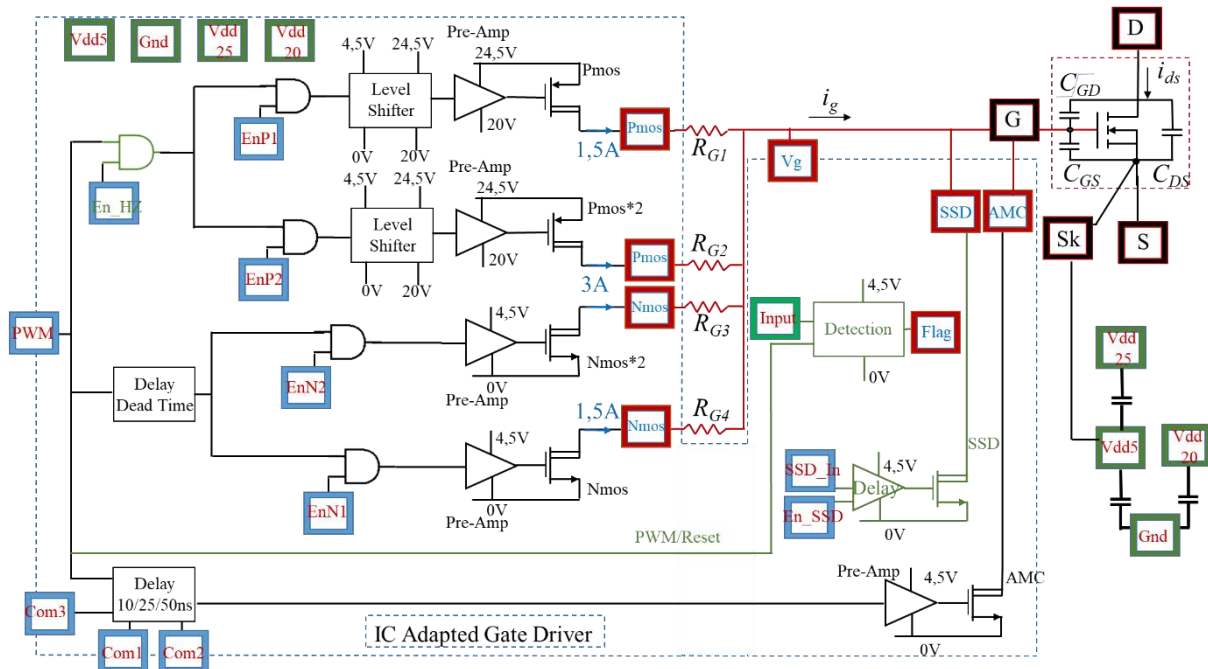


Figure 10. Schéma simplifié de l'active gate driver

Un buffer de sortie segmenté (40 V, +/- 4,5 A), utilisant des transistors 40 V proposés par la technologie. Les temps de propagation et de leur dispersion sont respectivement de 10 ns et 2 ns. La sortie segmentée du buffer permet trois configurations de courant (par exemple +/- 1,5 A ; +/-3 A ; +/-4,5 A, 25 °C), cela est réalisable de manière dynamique en fonctionnement avec des transistors PMOS et NMOS divisées et à chaque sortie une résistance de grille est connectée. Cette sélectivité est configurable par des bits logiques (libellés, EnP1, EnP2). Cette segmentation permet un ajustement dynamique selon le point de fonctionnement du meilleur compromis vitesse de commutation, pertes en commutation par rapport aux perturbations électromagnétiques générées par des commutations rapides.

- Un level shifter : Dans notre cas, le décalage (shifteur) de niveau est utilisé pour déplacer la commande du PMOS de  $[V_{-LV} \text{ à } V_{+LV}]$  (0 à 5V) à  $[V_{-HV} \text{ à } V_{+HV}]$  ('5V à 10V' ou '10V à 15V' ou ... ou '20V à 25V') ; afin de rester proportionnel à 5V ( $V_{+HV} - V_{-HV} = 5V \pm 0,5V$ ). La conception du shifteur de niveau est réalisée pour une alimentation électrique typique du gate driver  $V_{Drv} = V_{+HV} + V_{+LV} = 25V$ , donc la masse flottante devrait être à  $V_{-HV}$  typiquement 20V. De plus, le préamplificateur du PMOS est également à masse flottante.
- Un "active Miller clamp" dit AMC actif ( $R_{DS\_ON} < 1 \Omega$ ), protégeant efficacement le transistor de puissance contre les fronts de  $dv/dt$  élevés et verrouillant en toute sécurité le transistor de puissance en l'absence d'alimentation négative.

- Deux approches de détection SC différentes basées sur la méthode de dérivation [11]. Le circuit de détection a une surface de  $150\ \mu\text{m} \times 200\ \mu\text{m}$ , avec une consommation typique de  $1,52\ \text{mW}$  (ou  $0,34\ \text{mA}$  à  $4,5\text{V}$ ,  $25^\circ\text{C}$ ). Ces fonctions seront détaillées plus bas.
- Un blocage de sécurité (soft shut down SSD) pour un arrêt progressif ( $< 100\ \Omega$ ), dans un cas de court-circuit.

Le layout de l'ensemble des fonctions intégrées dans l'ASIC CMOS est divisé en deux parties principales. Le gate driver est de  $2414\ \mu\text{m} \times 1559\ \mu\text{m}$ , y compris les condensateurs de découplage des alimentations du circuit qui sont partiellement intégrés. Le bloc de détection pour les deux techniques de détection a une surface de  $150\ \mu\text{m} \times 200\ \mu\text{m}$ , et le SSD a une surface de  $80\ \mu\text{m} \times 30\ \mu\text{m}$ . La Figure 11 présente une vue microscopique de la puce. La puce est mise dans un boîtier QFN40  $6\ \text{mm} \times 6\ \text{mm}$ .

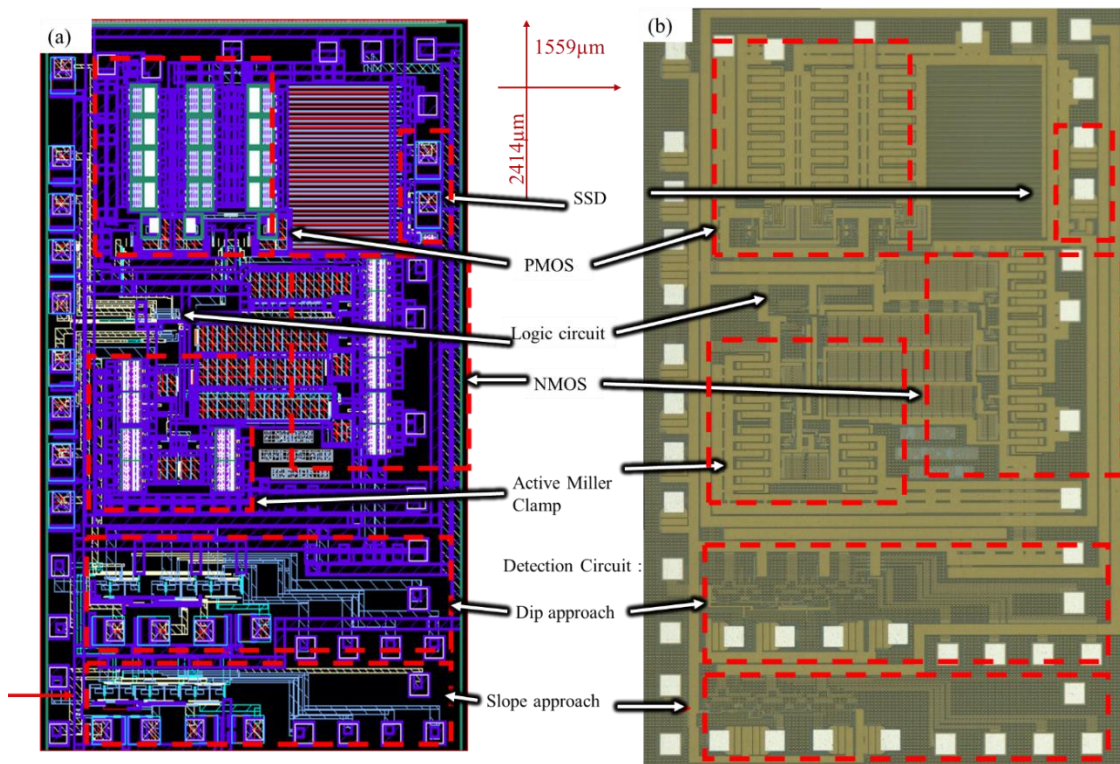


Figure 11. (a). Vue du layout sous Cadence. (b). Vue microscopique de la puce fabriquée

Un circuit imprimé dédié est réalisé afin d'héberger l'ASIC et permet une caractérisation dynamique plus poussée. Le PCB est réalisé avec 4 couches et a une surface de  $6\ \text{cm}$  par  $6\ \text{cm}$ , Figure 12. Toutes les commandes et le contrôle des délais sont pilotés par un FPGA externe.

Afin d'assurer le bon fonctionnement de l'ASIC, deux tests ont été réalisés. Le premier test, est sous capacité équivalente de  $C_{Eq} = 1.5\ \text{nF}$ . Et le deuxième test est sous puissance en utilisant des composants de puissance et le banc de puissance développé au sein du laboratoire. Une résistance de grille égale à  $10\ \Omega$  est soudée à chaque sortie du buffer de sortie (PMOS1, PMOS2, NMOS1 et NMOS2). Deux SMU Keithley 2612 sont utilisés pour alimenter le circuit imprimé,



chaque SMU possède deux alimentations indépendantes et isolées. De multiples tests ont été menés afin d'assurer le bon fonctionnement de l'ASIC. La Figure 13 présente les formes d'ondes expérimentales de la tension du grille sous différentes configurations. On peut trouver la configuration typique de l'ASIC dans le Tableau 3.

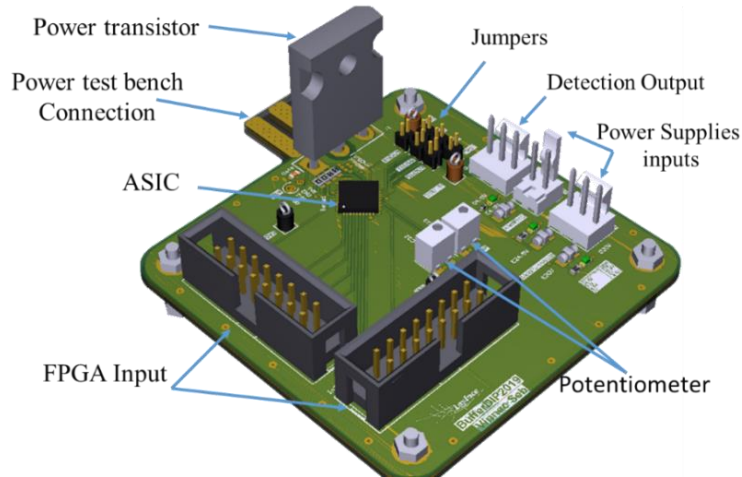


Figure 12. Vue 3D du PCB, incluant le DUT (transistor de puissance) et l'ASIC

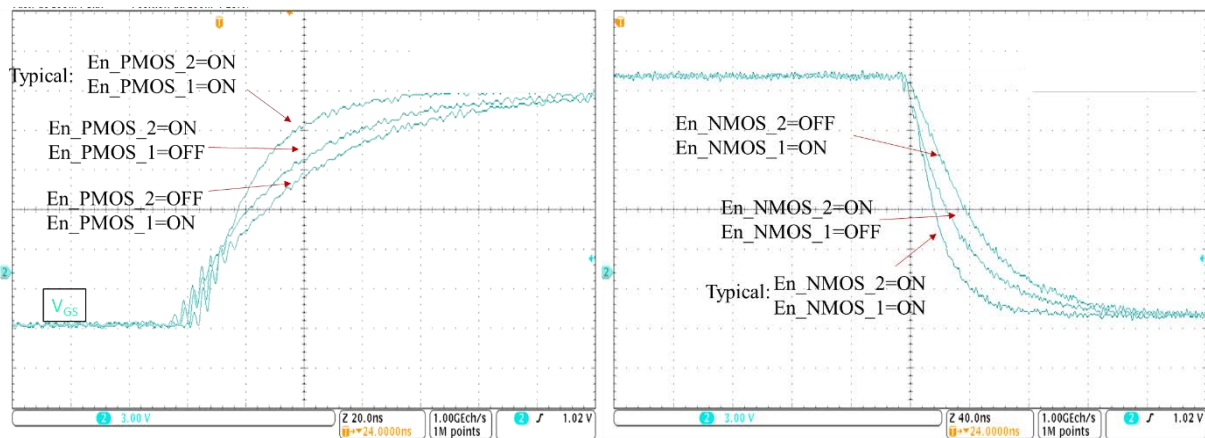


Figure 13.  $V_{GS}$  sous différentes configurations NMOS et PMOS @  $V_{HV+} = 16V$   $V_{LV+} = 4V$  et chaque  $R_{G\_Ext} = 10\Omega$ ,  $C_{Eq} = 1.5nF$

Tableau 3. Configurations typiques des commandes ASIC

Commands	Configurations	Function
En_PMOS1 / PMOS2	1 / 1	Full current source
En_NMOS1 / NMOS2	0 / 0	Full current sink
En_HZ	1	HZ OFF
En_Com1 / En_Com2 / En_Com3	0 / 0 / 0ns	AMC OFF
En_SSD / SSD_In	1 / 1	SSD OFF

L'ASIC a été entièrement validé sous un condensateur équivalent à la capacité  $C_{iss}$  du DUT. Dans cette partie, le condensateur équivalent est retiré et remplacé par un transistor de puissance

C2M0080120 (DUT). Le DUT a été soudé verticalement sur la carte de circuit imprimé. Et le PCB horizontalement dans le banc d'essai de puissance, Figure 14 (b). Sur le High Side, une diode SiC de 600V est utilisée, en parallèle avec une inductance de charge de  $270\mu\text{H}$ . Figure 14 (a) présente le banc d'essai V2 avec les différentes SMU. Le circuit a été validé sous une tension de bus de 25V à 200V, en fonctionnement normal et en court-circuit, développée au Chap.III. Figure 15 illustre les formes d'ondes de l'AGD sous NTO et SC-HSF avec  $V_{\text{Drv}+} = 16\text{V}$  et  $V_{\text{Drv}-} = 4\text{V}$  et avec une sortie divisée ; chaque sortie a une résistance externe de grille de  $10\Omega$ ; et le DUT sous 200V.

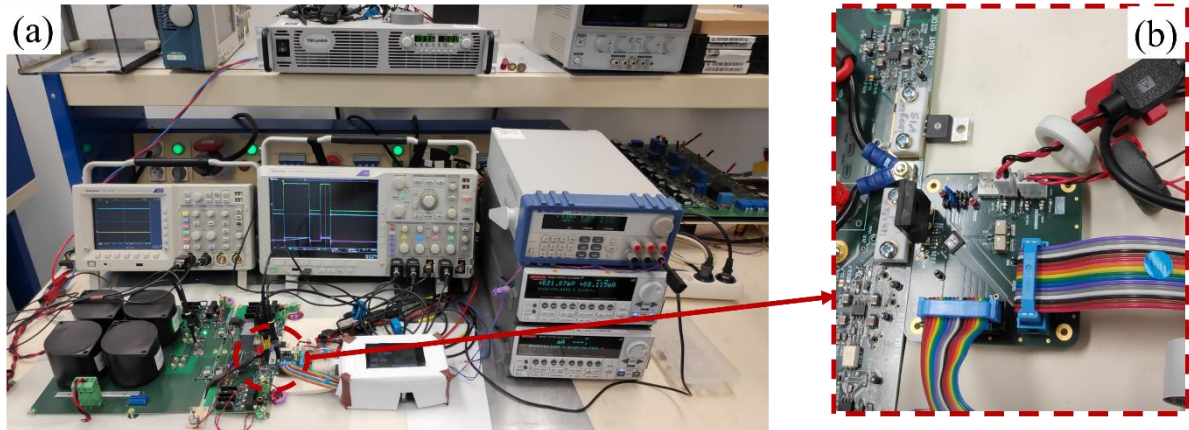


Figure 14. . (a). Banc de test V2 avec le PCB connecté (b). Une vue zoomée sur le PCB

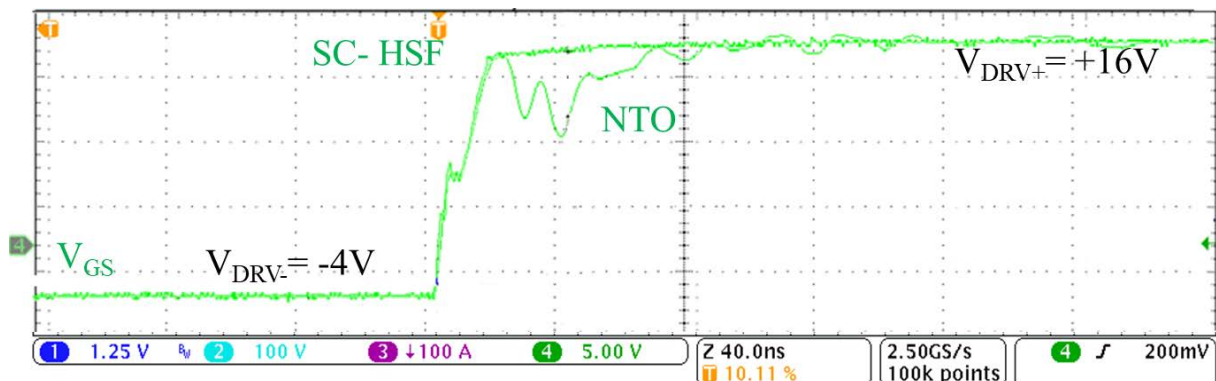


Figure 15.  $V_{\text{GS}}$  sous NTO et SC-HSF en utilisant l'ASIC et DUT : C2M0080120

### Modular Multilevel Gate driver MMAGD :

Plusieurs propriétés des MOSFETs SiC nécessitent de relever des défis nouveaux : une capacité de court-circuit réduite (par rapport aux IGBTs Si) et une faible couche d'oxyde de champ, une grande tension de pilotage grille-source (par rapport aux FETs GaN), un champ électrique élevé sous polarisation de grille négative en état de repos et une vitesse de commutation élevée. La polarisation négative en état de repos crée une forte contrainte qui réduit la fiabilité du MOSFET en SiC. La forte polarisation positive de la grille peut générer un courant de saturation du drain important en cas de court-circuit [12] [13]. Afin d'améliorer les performances et la fiabilité globales des MOSFETs SiC et d'offrir de nouveaux degrés de liberté pour la commande de grille, nous proposons une architecture de commande de grille à plusieurs niveaux (approche

par blocs de construction) sur un seul circuit intégré CMOS, [14]. Le principe est d'utiliser les transistors et les condensateurs 5V très efficaces pour le gate driver, et de connecter plusieurs étages en série, chaque étage étant isolé via la technologie Deep Trench Isolation (DTI) et intégré sur la même puce. En conséquence, la tension grille-source appliquée du MOSFET de puissance en SiC peut être facilement mise en forme, avec de nouvelles fonctionnalités.

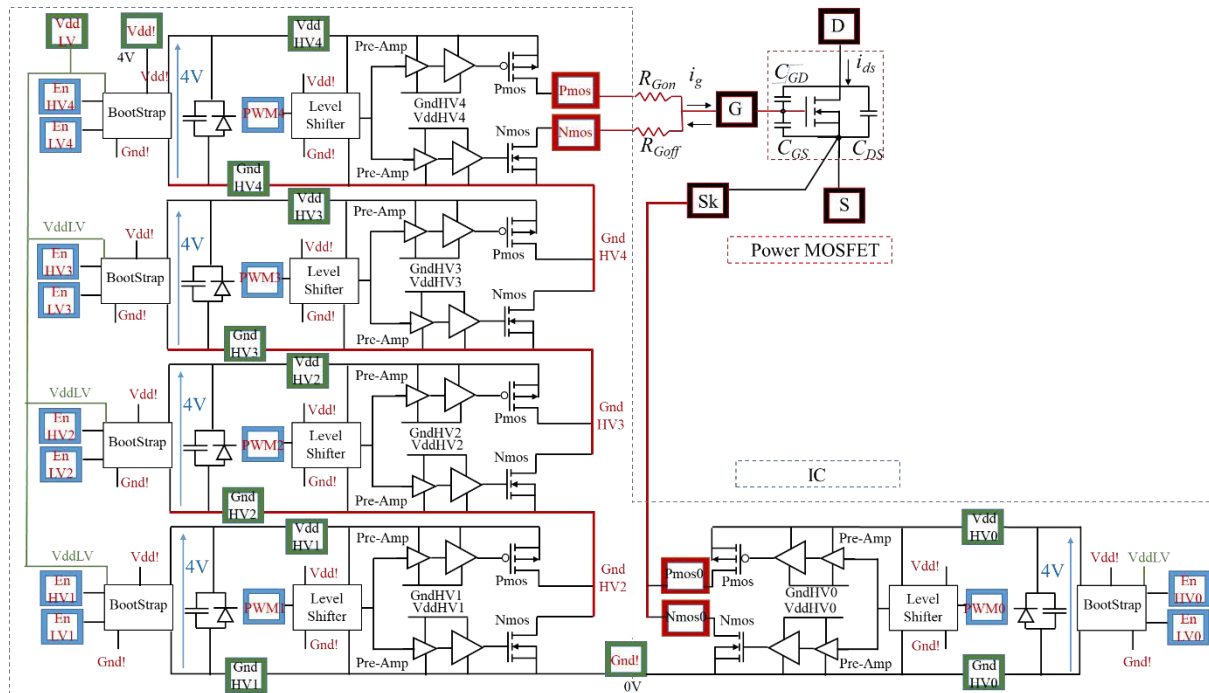


Figure 16. Schémas simplifié du MMAGD, basée sur 5 sous-modules

Dans notre topologie, l'idée centrale est de mettre en cascade des circuits push-pull CMOS 5V en série, chacun étant alimenté par l'énergie stockée dans des condensateurs flottants 5V, Figure 16. Cette technique peut également être appliquée à 1,8 V ou à d'autres tensions, ce qui permet de tirer parti des avantages des transistors basse tension et des condensateurs intégrés dont les facteurs de mérite sont meilleurs que ceux des transistors CMOS haute tension (par exemple  $>40$  V) pour les commandes de grille à deux niveaux. Cependant, il est nécessaire d'isoler chaque transistor basse tension, en raison de la tension de mode commun non nulle (par exemple supérieure à 20V) et des potentiels flottants en fonction de l'état des autres transistors connectés en série. La technologie CMOS SOI X-FAB XT-018 répond à ces critères, grâce à sa capacité d'isolation avec le DTI. Chaque circuit push-pull flottant, chaque circuit de pré-amplification et chaque shifteur de niveau sont identiques et peuvent être décrits comme un sous-module élémentaire de 5V, qui doit être compatible avec les tensions de mode commun spécifiées. Comme présenté dans la Figure 16, nous proposons d'intégrer de manière monolithique cinq sous-modules identiques (quatre vers la gate du DUT, un vers la source Kelvin) pour permettre une possibilité de pilotage à 6 niveaux, et un  $V_{GS}$  positif et négatif. Il n'y a pas de modification sur le MOSFET SiC et son interconnexion avec le driver de grille. Le principal problème de cette topologie monolithique est que les ground flottants et les régions d'épitaxie P flottantes de



chaque sous-module ne sont généralement pas autorisés par la fonderie, bien qu'ils soient isolés par des isolations en tranchées profondes et un substrat SOI. Lorsqu'un sous-module change d'état, des courants capacitifs parasites en mode commun circulent à travers les substrats locaux isolés de chaque sous-module. Cette question doit être analysée avec soin. Cependant, une conception préliminaire a été faite, tout en minimisant les condensateurs parasites en mode commun.

Le layout vérifie les règles DRC et LVS, et a été ajoutée à côté de l'AGD conçu précédemment, sur le côté gauche de la puce. Le sous-module unique de l'ASIC fabriqué a une surface de  $1050\mu\text{m} \times 500\mu\text{m}$ . L'ensemble de la vue du MMAGD est présenté dans la Figure 17, avec une surface de  $2400\mu\text{m} \times 1865\mu\text{m}$ . Ce layout a été réalisé en tenant compte des contraintes de temps : le sous-module 5V a été dupliqué, et la plus grande partie de la surface totale est utilisée par les condensateurs flottants de 5V et l'interconnexion métallique avec le métal supérieur.

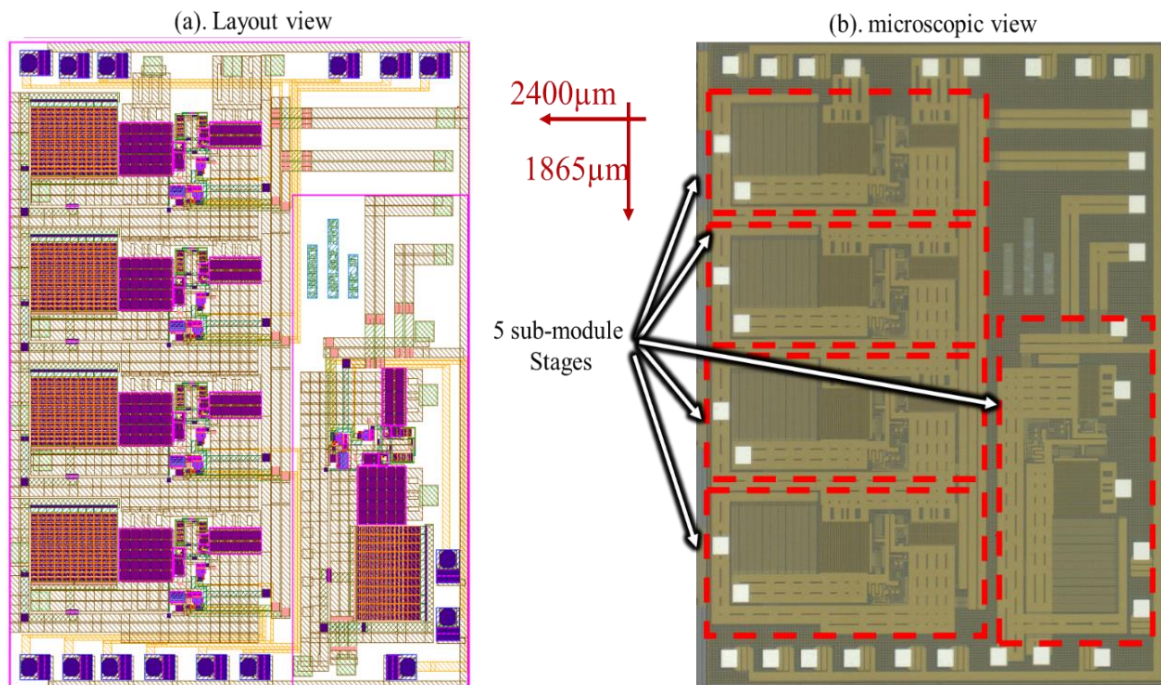


Figure 17. (a). Vue du layout sous Cadence. (b). Vue microscopique du MMAGD

Figure 18 montre la simulation du MMAGD, où chaque condensateur flottant est préalablement chargé à 4V et où un pilotage SiC amélioré est proposé. Les signaux PWM0...4 sont générés sur la base du signal PWM d'entrée et de la séquence de tension  $V_{GS}$  souhaitée. Plusieurs niveaux de tension peuvent également être obtenus par une combinaison différente des signaux PWM0...4 (par exemple  $V_{GS}=0V, +4V...+12V$ ). Les avantages du MMAGD sont mis en évidence dans la Figure 18: un courant de court-circuit HSF réduit grâce à un  $V_{GS}$  réduit uniquement lors de la mise sous tension (bien que plus élevé que la tension de plateau de Miller dans le pire des cas), un  $V_{GS}$  élevé pour de faibles pertes par conduction du SiC, un  $V_{GS}$  dynamique négatif pour améliorer l'immunité au  $dV_{DS}/dt$  (diaphonie haut/bas), et un  $V_{GS}$  nul à l'état hors tension pour réduire la contrainte d'oxyde de champ du SiC. Même si la tension  $V_{GS}$

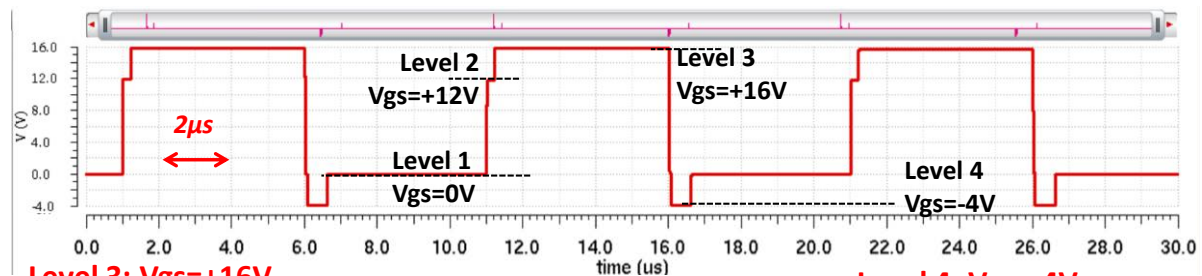
est réduite à +12V lors de la mise en marche, le courant de grille de pointe est maintenu élevé pour garantir des vitesses de commutation élevées et de faibles pertes de commutation du SiC grâce à une résistance de grille plus faible que celle d'un fonctionnement classique à 2 niveaux. Il faut noter que la résistance interne de la source distribuée sur chaque sous-module contribue naturellement à cette résistance de grille apparente. Les condensateurs flottants peuvent être rechargés de deux manières : chaque sous-module possède un circuit de type bootstrap qui peut recharger son condensateur flottant tant que la masse flottante GND\_HV0...4 est connectée à la masse du circuit intégré, et/ou en récoltant une partie de la charge de la grille SiC pendant les transitions de commutation.

#### Level 1: $V_{gs}=0V$

static turn-off at low field stress for DUT'SiO<sub>2</sub> and improved 3rq quadrant operation (static and dynamic)

#### Level 2: $V_{gs}=+12V$

dynamic turn-on with low drain – source saturation current enabling a safe operation and a non critical protection delay in short-circuit event



#### Level 3: $V_{gs}=+16V$

static on-state at high gate – source bias with low drop voltage and low on-state losses

#### Level 4: $V_{gs}=-4V$

dynamic turn-off with high cross-talk immunity

**Figure 18. Formes d'ondes du  $V_{GS}$  simulé avec l'architecture multi-niveaux, mettant en évidence les avantages du schéma de pilotage multi-niveaux sur le MOSFET SiC.**

La caractérisation expérimentale du MMAGD monolithique sur SOI-CMOS est en cours, avec un focus sur la technique de contrôle optimisée pour piloter activement les MOSFETs SiC et pour recharger les condensateurs flottants avec la plus grande efficacité. Les validations expérimentales en cours visent à comparer le MMAGD CMOS monolithique fabriqué avec une intégration PCB de cinq sous-modules, et à démontrer les améliorations de commande et de fiabilité des MOSFETs SiC. Les avantages du système de commande de grille modifié sont également à l'étude.

### **Chapter III: Nouveaux circuits de surveillance et protection contre les courts-circuits à grande vitesse pour les MOSFETs en SiC**

Trois circuits de détection de court-circuit sont présentés dans ce chapitre afin de relayer les challenges propres au Mosfet SiC en termes de rapidité de détection et d'intégration. La première méthode est basée sur la grille du transistor de puissance, intégrant le courant de grille détecté pour obtenir la charge de grille. Cette méthode porte le nom de méthode de charge de grille. La deuxième méthode est également basée sur la grille du transistor de



*puissance. Mais cette fois, la méthode est basée sur la dérivée de la tension grille-source, ce qui montre des différences prometteuses. La troisième méthode est confidentielle. Ces méthodes ont différents niveaux d'intégration, chacune ayant ses propres avantages. Les méthodes sont validées et développées expérimentalement dans ce chapitre.*

### **Surveillance en utilisant la Gate Charge :**

Cette méthode repose sur l'intégration rapide du courant de grille dans la séquence de charge de la grille à l'amorçage. La méthode connue sous le nom « gate charge » a déjà fait l'objet d'articles pour les IGBTs Silicium [15] et quelques résultats partiels pour les MOSFETs SiC en termes de performances et de mise en œuvre pratique [16]. Notre étude est menée puis validée expérimentalement pour la méthode de gate charge et la gestion des défauts pour les MOSFETs SiC en utilisant uniquement des composants CMS (composants montés en surface) sous pleine tension.

Cette méthode de charge de grille ne nécessite pas de diode haute tension pour la détection ou le réglage d'une période de masquage de détection. Cette méthode est aussi potentiellement robuste en termes de SNR sans pour autant rivaliser avec la méthode précédente. Dans le principe, Cette méthode nécessite un intégrateur ré-initialisable sur le front de commande ou un seuil de  $V_{GS}$  pour estimer la quantité de charge de grille  $Q_G$ ; et deux comparateurs. Le premier comparateur sert à distinguer la différence entre la quantité de charge en cas de SC  $Q_{G-SC-HSF}$  et dans le cas de l'amorçage  $Q_{G-NTO}$  ; le second comparateur vient créer un drapeau de lecture en utilisant uniquement un franchissement de seuil du signal  $V_{GS}$  compris entre la tension de plateau et le niveau de polarisation maximal, Figure 19 [17], permettant une indépendance au temps et aux dispersions temporelles. Ensuite, les deux sorties des comparateurs sont envoyées dans un circuit logique (porte AND, bascule D) pour traiter cette double condition. Une fois que le SC a été détecté et traité par le circuit logique, le DUT est mis sous protection. Le circuit de protection est similaire à celui de la littérature (Soft Shut Down - SSD), où une résistance plus importante est utilisée pour décharger en douceur la grille du transistor de puissance. Le  $R_{DS\_ON}$  du transistor auxiliaire SSD intégré est d'environ 7,5 ohms plus une résistance de 75 ohms en série, assurant un blocage progressif. Avant l'activation du SSD, le gate driver passe à un état de haute impédance HZ (signal HZ dans la Figure 19), où la grille du dispositif de puissance devient flottante afin de permettre au SSD d'agir pleinement. Afin de concevoir le circuit, la charge de grille en fonction de  $V_{GS}$  sous NTO et SC a été étudiée. Le circuit est directement proportionnel au diagramme 2D Figure 20. Ce diagramme en 2D est bien connu pour l'étude de la méthode de la gate charge, il offre deux clés de détection importantes : la zone de détection, et le rapport  $S = Q_{G-SC-HSF}/Q_{G-NTO}$ .

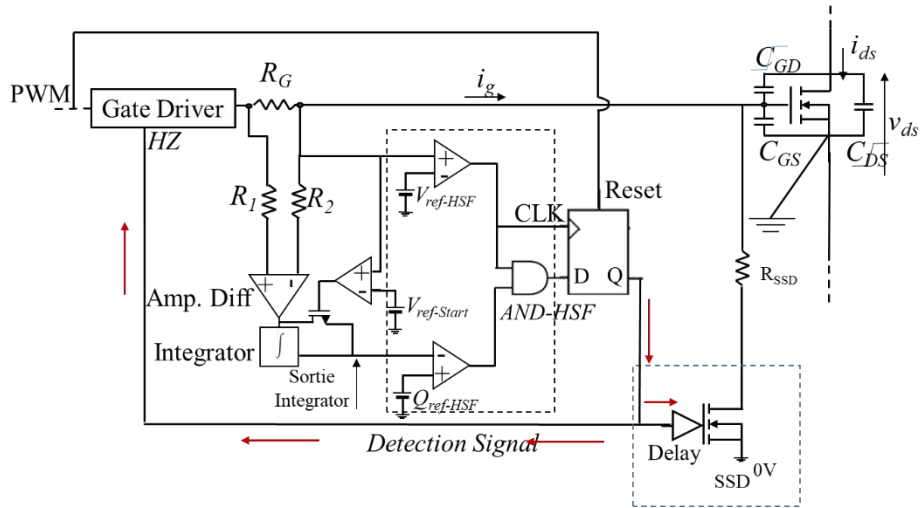


Figure 19. Schémas simplifier de la méthode de gate charge

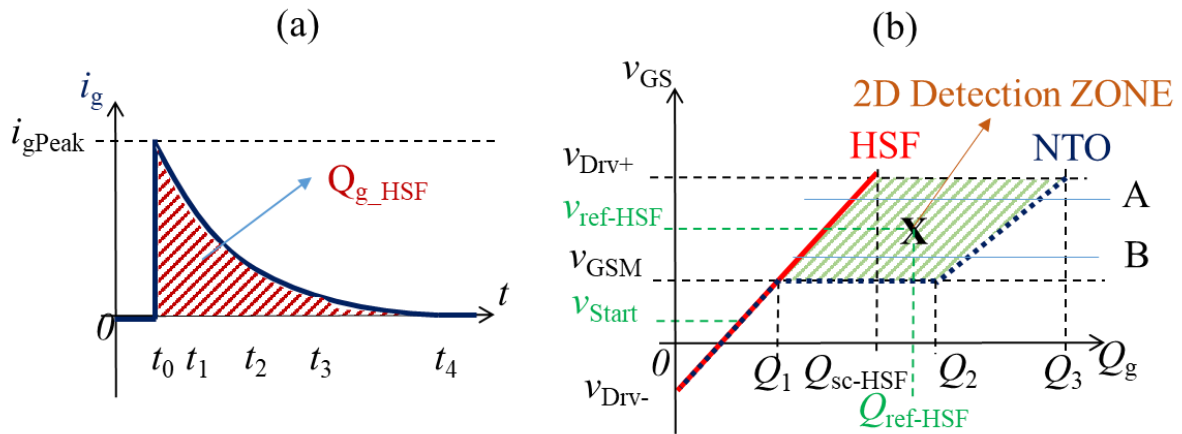


Figure 20. (a). Courant de grille sous SC-HSF. (b). Gate charge sous NTO et SC-HSF

Pour valider la méthode de charge de grille, une expérience a été menée pour la méthode de surveillance de la gate charge. La Figure 21 a été proposée en utilisant un transistor MOSFET SiC de 1,2 kV-80 mΩ, C2M0080120D et une diode Schottky SiC avec une inductance de charge à air de 270 μH pour le fonctionnement normal en double pulse. Une barrette de court-circuit en cuivre est utilisée pour le mode HSF. Le buffer de commande de grille utilisée est un IXDN614 à 3 états, permettant une configuration à haute impédance. Figure 22 illustre le prototype final de détection de SC.

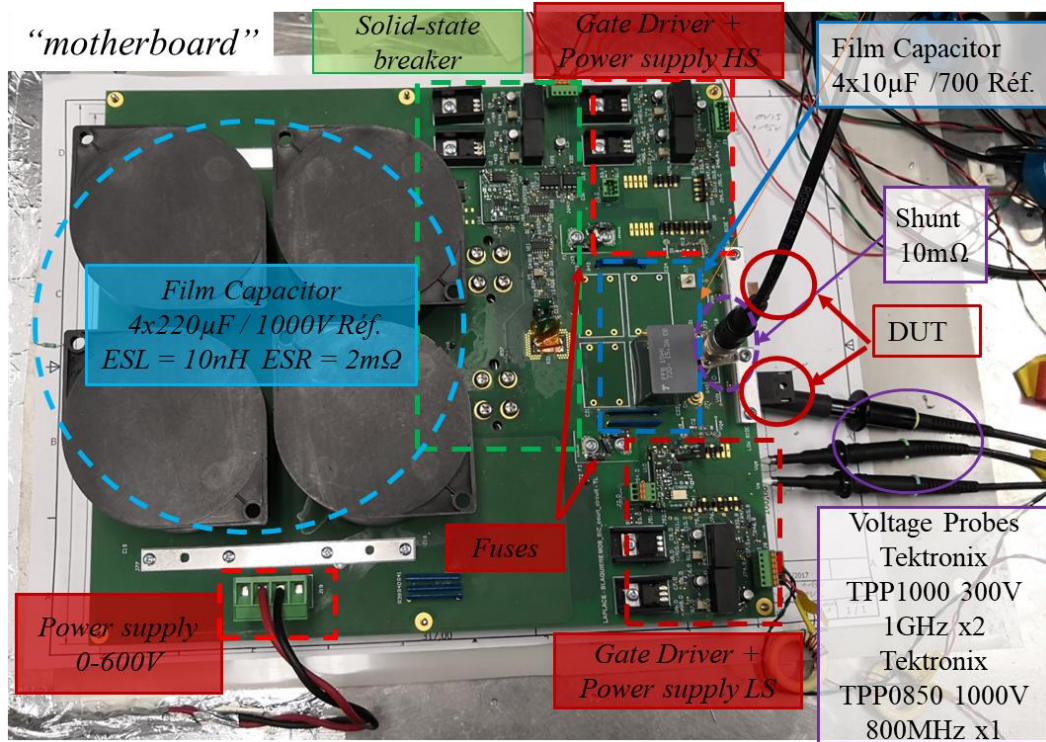


Figure 21. Banc de test de puissance V1

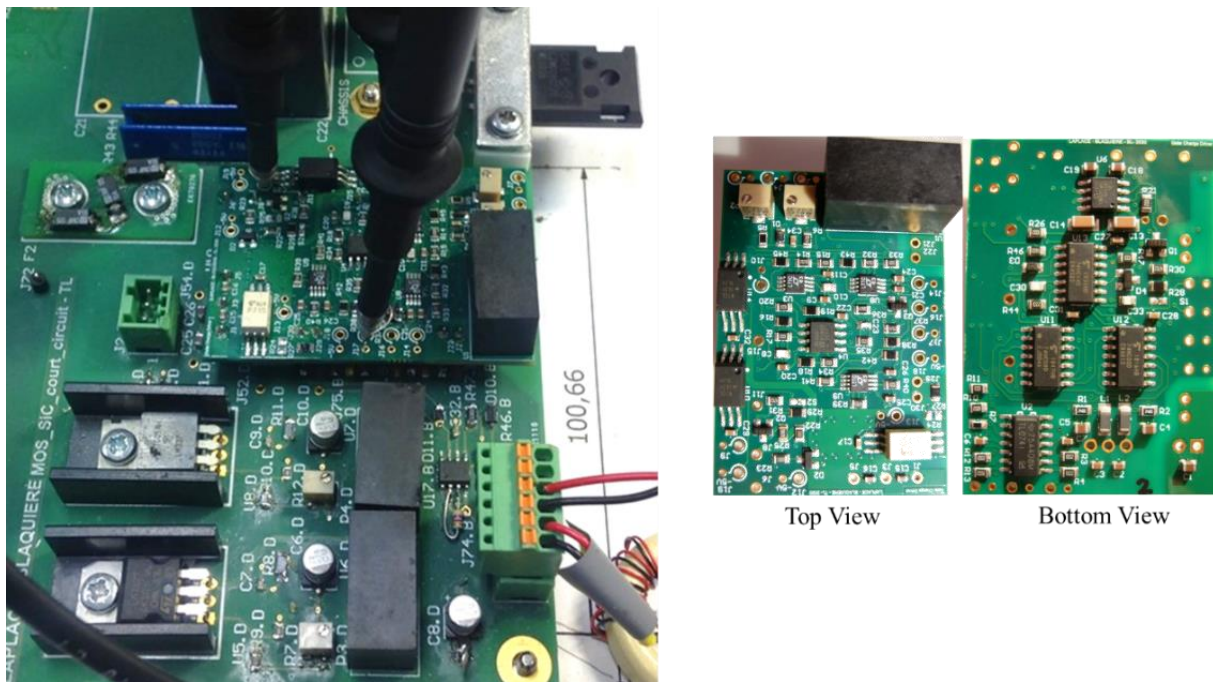


Figure 22. Prototype final connecter au banc de test V1

Figure 23 présente les formes d'ondes de la charge de grille sous les deux DUT, C2M0080120 et C3M0065090. La forme d'onde de la charge de grille est la forme essentielle, où la différence entre NTO et SC-HSF est détectable. ( $V_{GS}$  affecte la vitesse de détection et déclenche la détection). Comme on peut le voir, la charge de grille est proportionnelle à l'entrée du dispositif de puissance, plus le condensateur est petit, plus la charge de grille est faible. La réinitialisation



de l'intégrateur provoque une sélectivité dans l'intégration, il y a donc une période au début visible dans les formes d'ondes où l'intégration est désactivée.

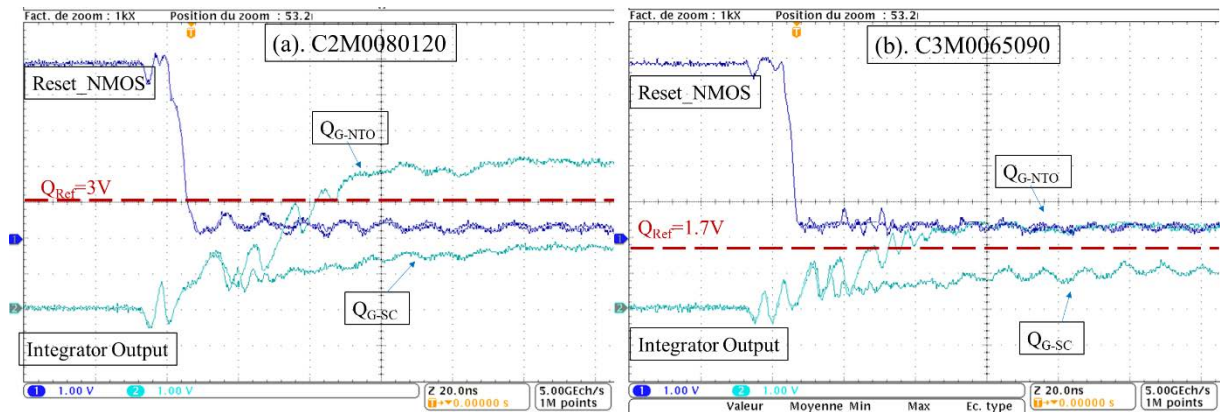


Figure 23. Formes d'ondes d'oscilloscope de la sortie de l'intégrateur pour les deux DUT. (a).C2M0080120D (b).C3M0065090D @400V &  $R_{G\_Ext}=10\Omega$

La détection du court-circuit se fait à 118ns et la protection à 173ns ; correspondant au délai nécessaire au passage en HZ, Figure 24 (a). Avec cette détection à grande vitesse permet de couper la sécurité à un niveau de courant bien inférieur au courant de saturation du canal. En effet, la coupure se fait ici à 130A alors que le courant de saturation est de 290A. Le SSD pourrait donc être accéléré afin de réduire davantage le stress énergétique à la détection de l'extinction pour le MOSFET SiC et de préserver sa capacité d'endurance aux cycles de court-circuit que le dispositif pourrait avoir à subir tout au long de sa vie dans des conditions d'utilisation accidentelle. Afin de couvrir pleinement la robustesse de cette méthode de détection, le circuit est validé sous différentes tensions de bus (50, 150, 250, 400, 600V) , , Figure 24 (b). Le courant est limité à environ 130A.

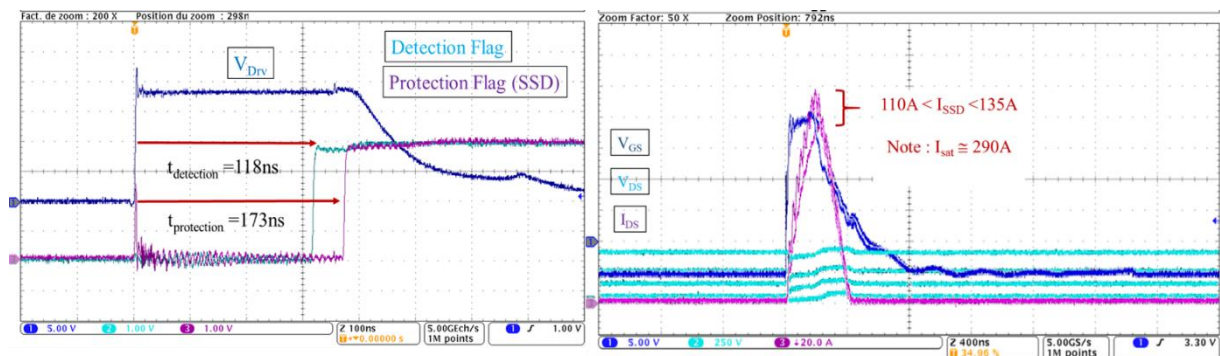


Figure 24. (a) Temps de protection et de détection, (b).  $V_{GS}$  sous protection pour différent  $V_{Bus}$

### Surveillance en utilisant la dérivée de la tension de grille :

Dans cette section, une deuxième méthode est proposée pour empiler une méthode supplémentaire et pour combler le vide qui existe parmi les méthodes de détection. Les changements de paramètres et de variables sous SC et NTO ont permis de proposer de nouvelles méthodes rapides intégrées dans le gate driver. Le AGD conçu dans ce chapitre 2, pour but de détecter la SC et protéger les MOSFETs SiC.

Cette deuxième méthode consiste à reconstruire le  $dV_{GS}/dt$  en utilisant une détection de courant capacitive pour fournir la dérivée de  $V_{GS}$  combinée à la surveillance  $V_{GS}$ . En d'autres termes, la méthode intégrée de surveillance est la méthode de la dérivation de  $V_{GS}$  qui est basée sur une détection par un circuit dérivateur analogique RC dans la séquence de plateau ( $V_{GS}$  proche de  $V_{GSM}$ ), Figure 25. Pour ce faire, deux approches de détection originales sont intégrées : l'occurrence (ou non) du plateau de Miller, et les différences de pente à la tension de grille, entre le fonctionnement normal et le fonctionnement sous court-circuit SC. Les deux méthodes offrent des solutions différentes et de meilleures performances que l'état de l'art. Ces techniques de détection SC sont basées sur des signaux à basse tension disponibles dans le AGD conçu. Comme la charge de la grille sert de référence, cette méthode (dérivation de la grille) est choisie pour être intégrée dans un niveau CMOS. Comme cette méthode est basée sur un condensateur de détection, les bruits seront élevés en cas d'intégration discrète. D'autre part, l'utilisation de l'intégration CMOS nous aidera à réduire encore le temps de détection. Il y a trois intervalles de temps importants sur le comportement du  $V_{GS}$ . Le premier a une pente de  $1/C_{iss\_Min}$ , suivi par le plateau de Miller, où la non-linéarité de  $C_{GD}$  est impliquée, et le dernier a une pente de  $1/C_{iss\_Max}$ . En utilisant cette différence des pentes, un impact significatif apparaît sur leurs dérivées temporelles. Ce changement sur utilisé afin de détecter le court-circuit sous HSF, Figure 26 et Figure 27.

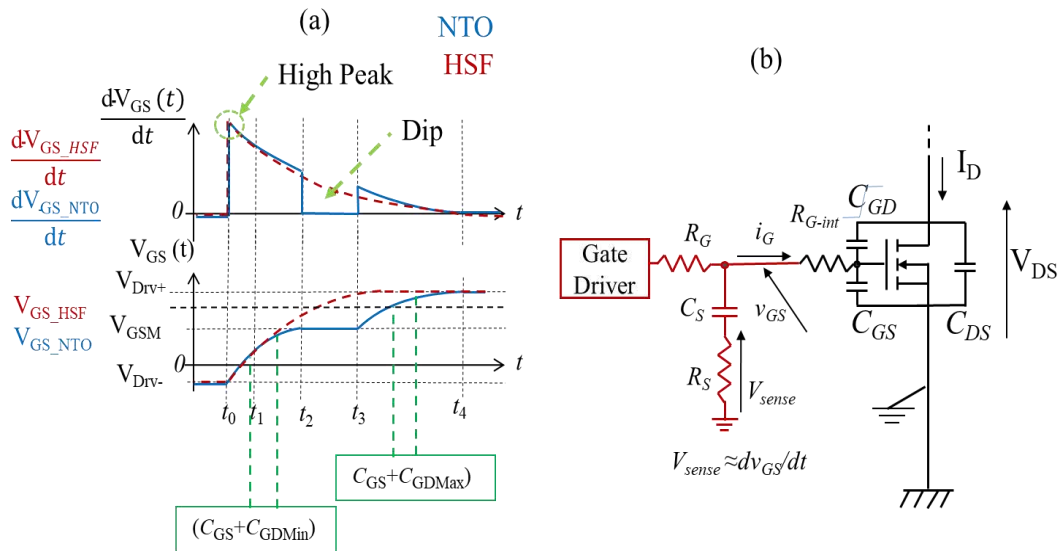
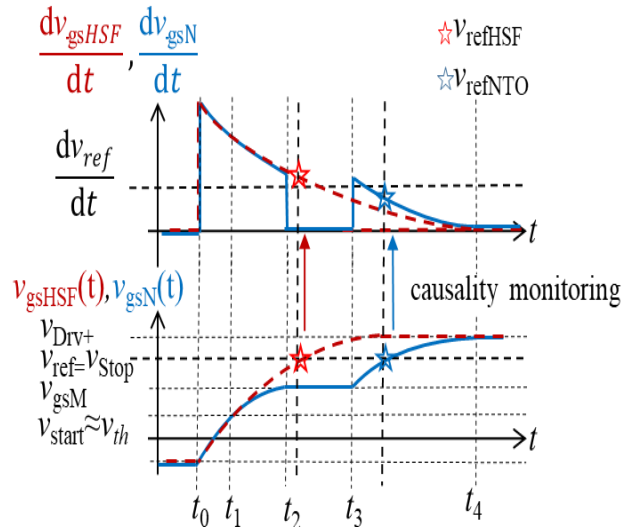
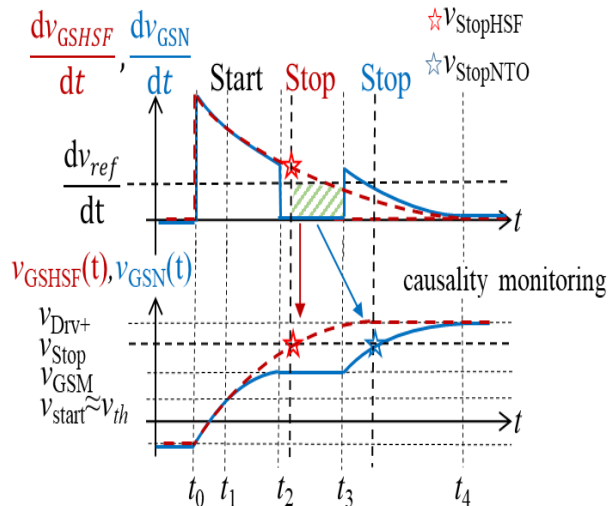


Figure 25. (a). Le signal  $dV_{GS}/dt$  sous NTO et SC-HSF. (b). Le circuit de dérivation.





**Figure 26. Caractérisation  $dV_{GS}/dt$  sous “NTO” et “HSF”, approches des pentes. Les étoiles représentent les niveaux obtenus pour la même tension de grille,  $V_{GS} = V_{Ref} = V_{Stop}$ , avec  $V_{Ref} > V_{GS\_M}$  pour l’approche des pentes.**



**Figure 27. Caractérisation  $dV_{GS}/dt$  sous “NTO” et “HSF”, approches du creux. Les étoiles représentent les niveaux obtenus pour la même tension de grille.  $V_{GS} = V_{stop}$  pour l’approche du creux, ce niveau n’est pas un niveau de comparaison**

Les approches discutées n'ont pas de dépendance temporelle directe. Cependant, elles dépendent du moment où la tension de grille s'élève au-dessus du niveau de référence  $V_{Ref}$ , donc plus la référence est basse, plus la détection est rapide, avec la seule condition du  $V_{GS} > V_{GS\_M}$ . Afin de valider le circuit de détection, Figure 28 ; une étude analytique a été menée. Puis des simulations ont aidé à cerner plus la compréhension du circuit, Figure 29. Les paramètres utilisés dans les simulations sont les suivants :

Au niveau du DUT : composant de puissance C2M0080120,  $V_{Bus} = 600V$ ,  $I_{Load} = 50A$ ,  $V_{Drv} = -5/+20V$  et  $R_G = 50\Omega$ , la valeur de la résistance est choisie élevée afin d’avoir une meilleure visualisation du phénomène de la dérivée.

Au niveau du High Side : Schottky diode C4D20120A, 20A, 1200V.

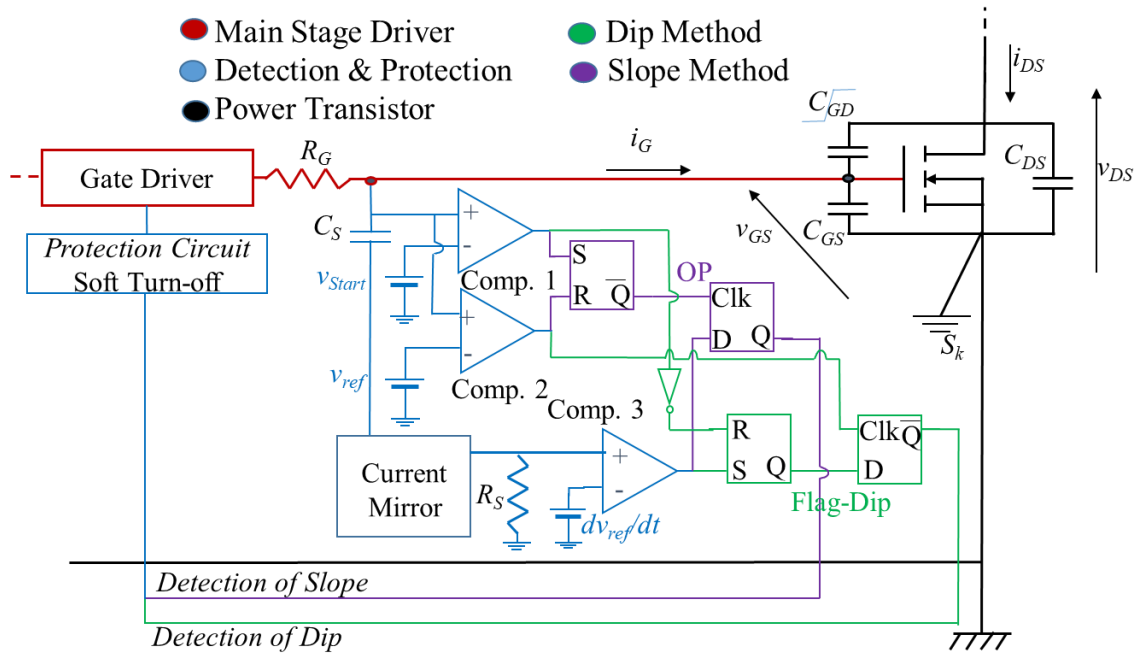


Figure 28. le schémas du circuit de détection par dérivée de la grille, pour les deux approches

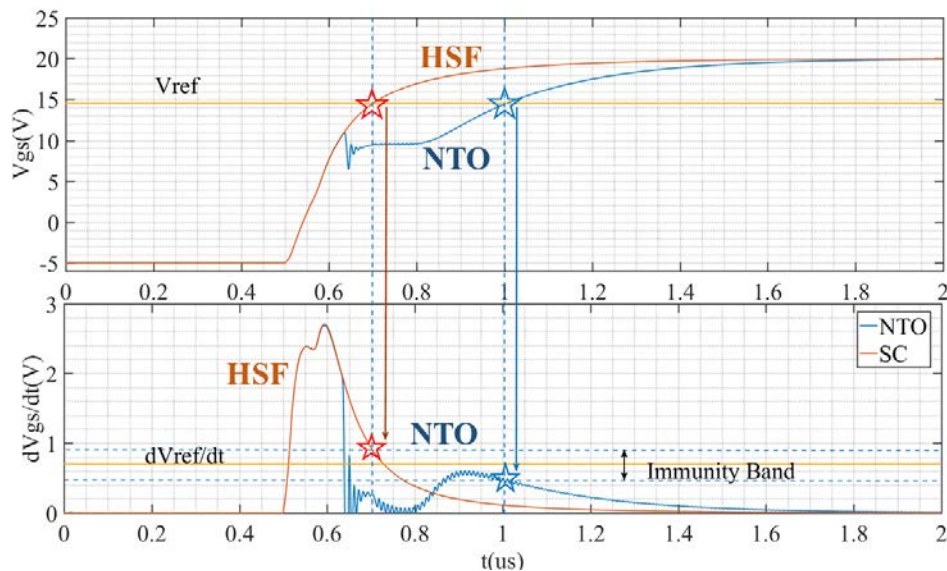


Figure 29. Forme d'ondes simulées de la tension de grille et sa dérivée, sous NTO et SC-HSF, avec  $L_D=25\text{nH}$   $L_{SK}=25\text{nH}$ ,  $L_G=5\text{nH}$

Les deux approches ont été intégrées dans l'ASIC, avec les fonctions de protection. Après validation du comportement du buffer et du C2M0080120, le circuit de détection est testé. Le circuit imprimé du AGD est connecté dans la partie basse du banc d'essai de puissance V2, y compris verticalement le DUT (transistor C2M008120). Afin de valider le circuit de détection, deux configurations sont nécessaires :

- NTO : Dans la partie haute, une diode SiC de 600V en parallèle avec une inductance de charge de  $270\mu\text{H}$  est utilisée.
- SC-HSF : Dans la partie haute, une pièce de cuivre est utilisée pour court-circuiter le drain et la source.

Dans les deux configurations, la sortie du buffer est divisée avec une résistance de grille externe de  $10\Omega$  à chaque sortie. Afin de pouvoir utiliser le premier circuit de détection utilisant C2M0080120 ( $C_{iss}=1,13\text{nF}$ ,  $C_{rss}=7,5\text{pF}$ ) (circuit 1, où tout est intégré dans l'ASIC CMOS, avec des références constantes), les tensions de commande de la grille sont réduites à  $V_{DrV+}=16\text{V}$  et  $V_{DrV-}=4\text{V}$  (au lieu de  $24,5\text{V}$  et  $4,5\text{V}$ ). Notez que les jeux de niveaux de référence intégrée sont réglés pour C2M0025120.

La détection est assurée, avec un long temps de descente sur le Flag, en raison de l'erreur de conception (petit inverseur logique 5V utilisé en sortie du circuit). Cette erreur nous a causé plus de problèmes sous des tensions de bus élevées, comme la génération d'oscillations ou le retard du drapeau de détection. La détection du court-circuit est assurée pour une gamme de  $V_{Bus}$  de  $0\text{V}$  à  $400\text{V}$ . De plus, la non-détection du fonctionnement normal est également assurée pour la même plage, Figure 30 et Figure 31.

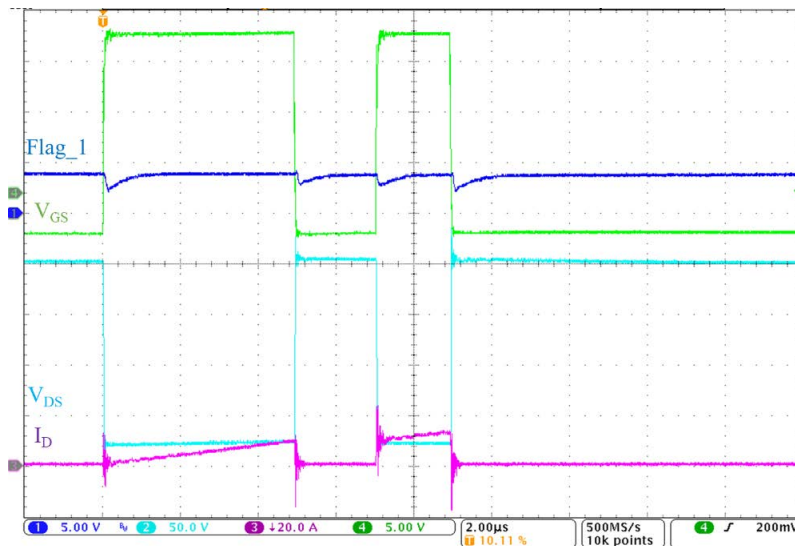


Figure 30. Formes d'ondes expérimentales sous NTO à  $200\text{V}$ , double pulse. La non-Détection est assurée

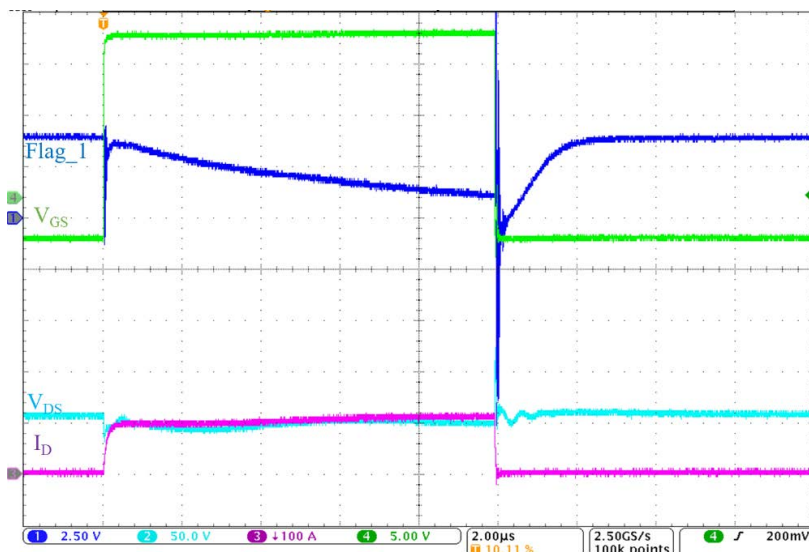


Figure 31. Formes d'ondes expérimental sous SC à  $200\text{V}$ , mono-pulse. la Détection est assuré

### **Troisième méthode :**

Confidentielle

## **Conclusion Général**

Dans un contexte d'électrification croissante de notre économie (transports, production d'énergie renouvelable, numérisation des services, automatisation, automobile et ferroviaire), des convertisseurs statiques basés sur l'électronique de puissance seront nécessaires pour faire transiter et conditionner une grande partie de l'énergie produite et consommée sur terre. Les pertes de ces convertisseurs conduiront à un surdimensionnement des ressources de production d'énergie, notamment renouvelables. L'efficacité, la densité de puissance et la fiabilité des convertisseurs statiques sont les principaux défis à relever. Pour améliorer leur efficacité, des transistors de puissance à semi-conducteurs à large bande interdite (GaN et SiC) ont été introduits sur le marché. En augmentant la vitesse de commutation, ces composants (principalement le SiC MOSFET et le GaN HEMT) présentent moins de pertes et sont plus compacts, ce qui permet d'obtenir des fréquences de commutation plus élevées. D'autre part, les coûts de maintenance de l'électronique de puissance sont largement liés à la fiabilité des transistors de puissance. En particulier, lors du fonctionnement, des événements généralement externes au convertisseur (perturbations EMI, erreur humaine, environnement), qui peuvent perturber le système et provoquer des régimes extrêmes (avalanche, court-circuit) sur les transistors de puissance qui peuvent conduire à leur défaillance. Ces régimes extrêmes sont critiques car ils ne peuvent être évités par une maintenance préventive des équipements et peuvent provoquer des cascades de défaillances qui peuvent conduire à une panne compromettant l'intégrité du système et de ses utilisateurs. La robustesse est donc une caractéristique importante de la fiabilité des convertisseurs de puissance. En particulier, la robustesse aux court-circuits est la plus critique en termes d'occurrence dans les systèmes.

Le MOSFET SiC est d'un grand intérêt pour augmenter l'efficacité des applications PV et éoliennes où les exigences de maintenance et de coût sont critiques. Sa robustesse aux court-circuits est donc d'un intérêt majeur pour le développement de ces industries. De plus, la capacité de résistance aux court-circuits des MOSFETs SiC est réduite par rapport aux IGBTs Si. Par conséquent, les techniques de détection utilisées pour les IGBT en Si ne sont plus d'une grande utilité. Une adaptation et de nouveaux circuits sont nécessaires.

Par conséquent, cette thèse est une contribution aux méthodes de protection des MOSFETs SiC en court-circuit, avec pour objectif d'augmenter la vitesse de détection, la robustesse et la sécurité. L'objectif est de mettre sur le marché des convertisseurs statiques sûrs et sains, en encourageant l'utilisation de transistors de puissance à base de MOSFETs SiC.

Afin de protéger et de réduire le stress en cas de court-circuit d'un MOSFET SiC donné, plusieurs moyens sont proposés.

- La solution la plus simple pour réduire le stress du transistor de puissance est de protéger le dispositif le plus tôt possible, ce qui nécessite un circuit de détection (le principal

travail de cette thèse). Pour ce faire, une vue d'ensemble et une modélisation du MOSFET SiC ont été menées, sous comportement normal et comportement en court-circuit. Plusieurs paramètres de commutation ont montré des opportunités prometteuses, ce qui a conduit à différentes topologies afin de protéger le MOSFET SiC. Ces topologies ont été discutées, conçues et validées par simulation puis expérimentation. Tous les circuits n'ont pas eu la chance d'être validés expérimentalement en raison de contraintes de temps. Chaque circuit présente des avantages et des inconvénients.

- La solution la plus complexe consiste à modifier physiquement la structure du MOSFET en SiC. Les changements physiques nécessitent une puce non standard, ce qui peut être difficile à commercialiser ; comme présenté dans le chapitre I, des changements peuvent être apportés à la structure du MOSFET en SiC.
- D'autre part, des modifications électriques peuvent également être apportées, afin de réduire la contrainte sous SC, en changeant la structure typique du driver de grille ; comme le driver de grille multi-modulaire, ou en utilisant d'autres techniques.

Dans les travaux futurs, la fusion de cette solution peut ouvrir de nouvelles opportunités en réduisant la contrainte sur le MOSFET SiC, en réduisant la surtension du courant de drain, et en protégeant le plus rapidement possible ; afin d'avoir une plus grande durée de vie de la SC, et d'offrir une plus grande durabilité.

La thèse a suivi une séquence de travail. La séquence a commencé par une compréhension complète de l'environnement du MOSFET SiC, et de son comportement en fonctionnement normal par rapport au fonctionnement en court-circuit. De même, le positionnement sur le marché du gate driver pour MOSFET SiC. Cette étude incluant l'état de l'art a été couverte dans le chapitre I. Cette étude nous a conduit à différents critères afin de concevoir notre active gate driver, adapté pour la détection de court-circuit et le circuit de protection. Le AGD a été validé expérimentalement. Il a donné d'excellents résultats dans différentes circonstances. L'AGD peut encore être amélioré et optimisé, en particulier les nombreux plots de validation et la conception de l'agencement. Il faut noter que la complexité de la configuration peut facilement conduire à une résistance et une capacité parasites élevées. L'AGD a été développé et présenté dans le chapitre II, en même temps que le multi-modulaire gate driver a été exploré. Le MMGD devrait être validé expérimentalement et comparé à une solution discrète. Les deux drivers ont été intégrés dans la même puce, respectivement  $2414\mu\text{m} \times 1559\mu\text{m}$  //  $2400\mu\text{m} \times 1865\mu\text{m}$ , avec des boîtiers différents, QFN40 6mm\*6mm. La taille de l'hôte PCB de la puce est de 6cm\*6cm. Au chapitre III, les méthodes de détection sont présentées et validées expérimentalement. Tout d'abord, la méthode de la charge de grille est développée comme référence, afin de pouvoir la comparer aux autres méthodes de détection. Sous HSF, cette détection a montré de grandes performances avec un temps de détection de 130ns. Afin d'améliorer cette méthode, l'ensemble des niveaux de référence peut être adapté à la variation de différents paramètres. De plus, le circuit de détection sous FUL est en cours. D'autre part, la deuxième méthode développée c'est la méthode de dérivation de la grille. Cette méthode, qui a été intégrée dans la technologie



CMOS, a également été validée expérimentalement. En raison de l'impossibilité d'apporter des modifications à la puce CMOS, le circuit de dérivation de la grille est simplifié en utilisant un condensateur et une résistance de détection pour générer le signal dérivé grille-source. Par conséquent, une étude ciblée devrait être menée afin de couvrir cette méthode et d'offrir un circuit meilleur et optimisé avec un rapport signal/bruit plus faible. En outre, il convient de rectifier quelques erreurs de conception, comme le circuit de sortie du drapeau de détection. Afin de gagner en rapidité de détection et d'avoir une grande robustesse, les niveaux de référence fixés peuvent également être adaptés. Dans cette méthode, le temps de détection ne peut être défini en raison d'une trop forte résistance interne (ou "sortance" réduite) à la sortie du circuit de détection, en utilisant un petit inverseur logique de 5V. Troisièmement, la dernière méthode de détection a été développée. Cette méthode montre une grande robustesse par rapport aux autres méthodes, pour une grande variation de paramètres, qui ne nécessite que des niveaux de référence fixes bas. Cette méthode est en cours de fabrication, elle devrait donc être validée expérimentalement. Afin de compléter les circuits développés quelques propositions sont énoncées.

- Adapter le circuit à la variation de différents paramètres, principalement en concevant un ensemble de niveaux de référence adaptés, en particulier pour la charge de grille et la méthode de dérivation de la grille.
- Optimiser et améliorer les circuits, en particulier la méthode de dérivation de la grille.
- Valider entièrement le circuit en menant des expériences dans des conditions extrêmes.
- Développer le circuit de détection en utilisant les méthodes de charge et de dérivation de la grille sous le type SC-FUL.
- Adapter le circuit de détection pour les modules de puissance et les structures à plusieurs niveaux.
- Optimiser davantage la configuration des techniques (par exemple, les niveaux de seuil, les paramètres de filtrage, ...) et, plus généralement, réduire le nombre de PAD utilisés pour la configuration, afin d'obtenir une puce unique compacte
- Adapter ces méthodes pour les transistors de puissance en GaN.

Le AGD pourrait être encore amélioré et pourrait fusionner plusieurs circuits de détection. L'AGD a encore un long chemin à parcourir, en intégrant plus de fonctions comme l'alimentation, l'isolation, le driver de high side, etc... De plus, l'AGD peut être intégré dans un boîtier vers des solutions monolithiques. Il faut garder à l'esprit que de plus en plus de fonctions peuvent et doivent être intégrées, afin de présenter un AGD sûr et plus petit. Différentes fonctions de diagnostic peuvent également être ajoutées, comme le diagnostic permanent au niveau du seuil, la fuite de courant de grille, le temps de propagation interne, le réglage du niveau de tension ou la température de l'appareil, à l'état actif et à l'état inactif. En outre, la dynamique de GaN, qui s'attaque au marché de la conversion d'énergie, pousse la recherche à investir plus de temps et à développer un AGD sûr avec des fonctions de diagnostic et de surveillance dédiées.

<b>List of Figures</b>	
Fig.I. 1. Application areas of classical discrete power semiconductors [9].	16
Fig.I. 2. Material properties of Silicon, Silicon Carbide and GaN.	17
Fig.I. 3. N-channel MOSFET, (a). Symbol (b). Equivalent circuit (c). Idealized $I_D$ - $V_{DS}$ characteristics (d). Transfer $I_D$ - $V_{GS}$ characteristic.	18
Fig.I. 4. Comparison curve of the "small signal" nonlinear capacitance $C_{GD}$ , between datasheet and eq.(I.2).	20
Fig.I. 5. Inverter leg under PLECS.	21
Fig.I. 6. Turn-on voltage and current waveforms of the LS MOSFET.	22
Fig.I. 7. Turn-off voltage and current waveforms of the LS MOSFET.	24
Fig.I. 8. Block diagram of a synchronous buck converter presenting the essential gate driver functions for the control of both HS and LS (ADuM4121 isolated gate drivers).	27
Fig.I. 9. (a) Synchronously switched half bridge (b). Pulse width distortion (c). Effect of propagation time [29].	29
Fig.I. 10. Two Different level topology of isolation, according to IEC 60664-1 and IEC 61800-5-1.	30
Fig.I. 11. Different isolation technologies [29].	31
Fig.I. 12. Three elementary output buffer structures with a single gate resistance.	32
Fig.I. 13. Four elementary output buffer structures with a several gate resistances.	33
Fig.I. 14. Three elementary output buffers structures with split gate resistance, and split power supply.	34
Fig.I. 15. Principle topology of monitoring [32].	35
Fig.I. 16. Circuit schematic of the synchronous buck converter implementing a self-switching technique at turn-on to safely generate reduced dead time [45].	37
<b>Fig.I. 17.</b> Trade-off $E_{ON}$ vs $dV/dt$ function of $R_G$ (solid line) or $C_{GD}$ (dashed line) values for constant $V_{HV-DC}$ , $I_L$ and temperature [36].	38
<b>Fig.I. 18.</b> Equivalent control slew rate circuit (a). Variable resistance (b). Variable capacitance [49].	38
Fig.I. 19. (a). Classic test. (b). Modified test [61].	40
Fig.I. 20. Co-integration VDMOS and LDJFET "Patent number US 10,504,995 B1".	40
Fig.I. 21. Low-side parasitic turn-on, and current flow due to the Miller capacitor.	41
Fig.I. 22. (a). Hard switch faults half bridge with non-overlapping inputs, (b). Waveforms of $S_2$ during a short-circuit event [29].	42
Fig.I. 23. Different protection circuits.	43
Fig.I. 24. Internal block diagram of a single channel gate driver, MC33GD3100 NXP, [56].	43
Fig.I. 25. Gate driver technology roadmap for high power and low/mid power application. [78].	45
Fig.I. 26. Wafer view of (a). Junction-Isolation (b). Silicon-on-insulator [80].	46
Fig.I. 27. Infineon gate driver IC technologies [80].	46
Fig.I. 28. Integration Phase One: Monolithic half bridge (a). Image of an EPC2100 monolithic half bridge measuring 6mm x 2mm (b). equivalent circuit diagram [81].	47
Fig.I. 29. Integration Phase Two: Half bridge + Driver (a). Image of an EPC2112 monolithic GaN-on-Si FET with integrated driver measuring 1.1mm x 2.9mm. (b). equivalent circuit diagram [81].	47

Fig.I. 30. . Integration Phase Three: ePower™ stage (a). Image of an EPC2152 monolithic ePower stage measuring 3.9mm x 2.6mm (b). equivalent circuit diagram [81] .....	47
Fig.I. 31. Si IGBT vs SiC MOSFET Output Characteristics ( $I_D$ - $V_{DS}$ ) (a). Representative (b). [87] .....	49
Fig.I. 32. Experimental current waveforms during critical short-circuit test for SiC MOSFET and Si IGBT (SiC MOSFET: $V_{DS}$ = 600V, $V_{GS}$ = 20V; Si IGBT: $V_{CE}$ = 600V, $V_{GE}$ = 15V) [90] .....	50
Fig.I. 33. (a). Turn-on switching characteristics of SiC MOSFET under NTO conditions. (b). Equivalent circuit of the half bridge.....	51
Fig.I. 34. Turn-on regions presented on $I_D$ - $V_{DS}$ curve.....	52
Fig.I. 35. (a). Turn-on switching characteristics of SiC MOSFET under HSF conditions. (b). Equivalent circuit of the half bridge.....	52
Fig.I. 36. (a). Turn-on switching characteristics of SiC MOSFET under FUL conditions. (b). Equivalent circuit of the half bridge.....	53
Fig.I. 37. SC under HSF experimental waveforms for $V_{GS}$ = 20V and $V_{DS}$ = 300V; 350V .....	54
Fig.I. 38. SC failure mode test (a). Current limitation (b). Short-pulse .....	55
Fig.I. 39. Failure breakdown schematic steps and $I_D$ - $V_{DS}$ curve failure analyses fault, type I. Typ. $T^\circ$ .....	55
Fig.I. 40. Illustration of the failure analysis fault points, type II (a). High side and (b). low side $I_D$ - $V_{DS}$ curve. Typ. $T^\circ$ .....	56
Fig.I. 41. Three current monitoring methods schematic (a). Shunt resistor method (b). SenseFet method. (c). Transformer method [102] .....	57
Fig.I. 42. Desaturation detection schematic .....	60
Fig.I. 43. Partial Gate leakage detection schematic. ....	60
Fig.I. 44. (a) Experimental waveforms of the gate current and the detection voltage. (b). A closer look at the leakage current at the detection.....	61
Fig.I. 45. (a). $I_G$ curve under NTO (b). Gate Charge Characteristics under NTO. ....	62
Fig.I. 46. Gate Charge monitoring method schematic for either HSF or FUL .....	63
Fig.I. 47. Experimental waveforms of the Integrator output signals under NTO and HSF conditions. @ $R_G$ = 10 $\Omega$ , $V_{GS}$ = -5/20V $V_{DS}$ = 400V, C2M0080120 .....	63
<b>Fig.II. 1.</b> Test bench V1 for Extreme short-circuit and double pulse operations .....	69
<b>Fig.II. 2.</b> Test bench V2 600V -160J, for extreme short-circuit and double pulse operations	70
<b>Fig.II. 3.</b> LV transistors (a) Bulk CMOS layer structure (b) SOI CMOS layer structure .....	71
<b>Fig.II. 4.</b> View of different layers of the X-Fab CMOS SOI 0.18 $\mu$ m technology [121].....	72
<b>Fig.II. 5.</b> Simplified circuit between the gate driver and the SiC MOSFET .....	74
<b>Fig.II. 6.</b> Block diagram of the Output buffer with (a). double power supply (b). quadruple power supply .....	76
<b>Fig.II. 7.</b> Schematic block of the active gate driver – quadruple power supply .....	78
<b>Fig.II. 8.</b> Schematic of the used level-shifter.....	80
<b>Fig.II. 9.</b> Simulated input and output of the level shifter under cadence.....	81
<b>Fig.II. 10.</b> $ I_D$ - $V_{DS} $ characteristic under different $V_{GS}$ and two different widths (1A,3A) for both 40V (a). PMOS and (b). NMOS .....	82
<b>Fig.II. 11.</b> DC characteristic of the inverter.....	82

<b>Fig.II. 12.</b> Segmented architecture with multiple outputs for different source/sink currents and different external gate resistors. ....	83
<b>Fig.II. 13.</b> Simplified structure of the PMOS and NMOS pre-amp.....	84
<b>Fig.II. 14.</b> Logic circuit including dead-time management and enable configuration. ....	86
<b>Fig.II. 15.</b> Enable configuration for each NMOS and PMOS pre-amp .....	86
<b>Fig.II. 16.</b> Chronogram presenting dead-time management. ....	87
<b>Fig.II. 17.</b> Partial architecture of the gate driver (non-complete).....	87
<b>Fig.II. 18.</b> Simulation waveforms of the buffer under $R_{G\_On}=R_{G\_OFF}= 10\Omega$ , $C_{eq}= 1.5nF$ , $V_{+HV}= 24.5V$ , referenced to kelvin source +5V. ....	88
<b>Fig.II. 19.</b> $V_{out}$ and $I_{out}$ for different enable configurations, $C_{Eq}= 1.5nF$ , $R_{G\_Ext}= 0\Omega$ , $V_{+HV}= 24.5V$ .....	88
<b>Fig.II. 20. (a).</b> Half bridge configuration <b>(b).</b> Miller current path <b>(c).</b> Effect of Miller current on the gate voltage. [29] .....	90
<b>Fig.II. 21.</b> Gate driver with <b>(a).</b> internal Miller Clamp <b>(b).</b> External Miller Clamp [29].....	90
<b>Fig.II. 22.</b> Qualitative chronogram of the AMC internal and external delay settings .....	91
<b>Fig.II. 23.</b> Simulation results of the gate voltage and current under different AMC activation delays.....	92
<b>Fig.II. 24.</b> dV/dt immunity: AMC effect under Miller effect for different dV/dt .....	92
<b>Fig.II. 25.</b> Soft shut down circuit with both inputs connected to an FPGA .....	93
<b>Fig.II. 26.</b> Simulation waveforms of the AGD under HZ, SSD is OFF .....	94
<b>Fig.II. 27.</b> Simulation waveforms of the AGD under HZ and SSD is ON .....	94
<b>Fig.II. 28.</b> Simplified schematic of the AGD .....	95
<b>Fig.II. 29.</b> Different set of the layout for a single finger and multiple fingers .....	96
<b>Fig.II. 30.</b> Layout of one PMOS chain (level shifter + pre-amp + output buffer).....	97
<b>Fig.II. 31. (a).</b> ESD pad equivalent schematic <b>(b).</b> layout view. ....	98
<b>Fig.II. 32.(a).</b> Layout view under cadence, <b>(b).</b> microscopic view of the fabricated chip .....	99
<b>Fig.II. 33.</b> Packaged ASIC on the QFN 40 6mm*6mm, with the AGD connected, (failed prototype) .....	99
<b>Fig.II. 34.</b> Time chart of the ASIC .....	100
<b>Fig.II. 35.(a).</b> Keyence Vhx-1000 digital microscope <b>(b).</b> zoom on the pads with the gold bonding wire.....	100
<b>Fig.II. 36.</b> 3D view of the PCB.....	101
<b>Fig.II. 37. (a).</b> AGD in package <b>(b).</b> placement of the AGD on the PCB.....	101
<b>Fig.II. 38.</b> Physical placement of the ASIC on the PCB (by 3DPhi).....	102
<b>Fig.II. 39.</b> Test bench V0.A .....	102
<b>Fig.II. 40.</b> PCB Power sources connectivity.....	103
<b>Fig.II. 41.</b> Touch screen with different parameters configuration and the PCB.....	104
<b>Fig.II. 42.</b> $V_{GS}$ for different power supplies .....	104
<b>Fig.II. 43.</b> $V_{GS}$ under different NMOS and PMOS configurations @ $V_{HV+}= 16V$ and each $R_{G\_Ext}= 10\Omega$ , $C_{Eq}= 1.5nF$ .....	105
<b>Fig.II. 44.</b> $V_{GS}$ under different AMC configurations @ $V_{HV+}= 25V$ and each $R_{G\_Ext}= 10\Omega$ , $C_{Eq}= 1.5nF$ .....	106
<b>Fig.II. 45.</b> $V_{GS}$ under HZ and then under HZ + SSD @25V.....	107
<b>Fig.II. 46 . (a).</b> test bench V2 with the PCB plugged-in <b>(b).</b> a zoom view on the plugged PCB .....	107

<b>Fig.II. 47.</b> Oscilloscope waveforms of the AGD under double pulse and DUT under 200V @ $V_{Drv+}= 16V$ and $V_{Drv-}= 4V$ .....	108
<b>Fig.II. 48.</b> Oscilloscope waveforms view at the turn-on and the turn-off of the DUT under 200V @ $V_{Drv+}= 16V$ and $V_{Drv-}= 4V$ .....	108
<b>Fig.II. 49.</b> The current flow for the (a). slow turn-on process (b). fast turn-on process.[31] 110	
<b>Fig.II. 50.</b> (a). Multi-level Gate driver topology based on a discrete assembly (b). idealized waveforms demonstrating the multi-level series operation.[131] .....	110
<b>Fig.II. 51.</b> Proposed multi-level modular SOI-CMOS gate driver (MMAGD), based on five submodules. All functions are integrated on one IC. ....	111
<b>Fig.II. 52.</b> Single stage of the multi-level highlighting DTI isolation .....	112
<b>Fig.II. 53.</b> $V_{GS}$ simulated waveform with the multilevel architecture, highlighting the benefits of the multilevel driving scheme on the SiC MOSFET. ....	112
<b>Fig.II. 54.</b> Left, Optical microscope view of a 5V split output buffer [157]. Right, Experimental waveforms of one submodule on a 1nF constant capacitor, @ 1MHz, $V_{GS} = 0V...+4V$ .....	113
<b>Fig.II. 55.</b> Bootstrap circuit .....	114
<b>Fig.II. 56.</b> Microscopic view of a single sub-module. Area is $1050\mu m \times 500\mu m$ .....	115
<b>Fig.II. 57.</b> (a). Layout view of MMAGD (b). Microscopic view of MMAGD.....	116
Fig.III. 1. (a). Simplified turn-on switching characteristics of SiC MOSFET under NTO conditions (b). Equivalent circuit of the command and the SiC transistor (c).Capacitance variation [162]. .....	120
Fig.III. 2. (a). $I_G$ curve under NTO (b). Gate Charge Characteristics under NTO. ....	122
Fig.III. 3. (a). $I_G$ curve under SC- HSF (b). Gate Charge Characteristics under HSF.....	123
Fig.III. 4. Timing chart under NTO and HSF conditions.....	124
Fig.III. 5. (a). $I_G$ curve under SC- FUL (b). Gate Charge Characteristics under FUL. ....	125
Fig.III. 6. Timing chart under NTO and FUL conditions. ....	126
Fig.III. 7. Gate Charge Characteristics under open circuit condition. ....	127
Fig.III. 8. Timing chart under NTO and OC conditions. ....	127
Fig.III. 9. Illustration of different ratios on the Gate charge characteristic for a WolfSpeed 2 <sup>nd</sup> generation power transistor .....	130
Fig.III.10. Analytical Gate charge characteristics under different parameters variations, Standard parameters used are $I_{Load}= 80A$ , $V_{DS}= 800V$ , $R_G= 3.6\Omega$ , $g_{fs}= 20.7S$ , DUT: C2M0025120.....	130
Fig.III. 11. Gate charge fault-detection scheme for Silicon IGBTs (a). based on adaptive threshold level [167] (b). based on the measurement and evaluation in the turn-on transient period [165] (c). Common schematic [16]. .....	131
Fig.III. 12. Typical schematic based on the gate charge method. ....	134
Fig.III. 13. 3D plot of $V_{Out}$ under different variation .....	135
Fig.III. 14. Simulation waveforms under LTspice of the partial circuit, Detection logic circuit and protection is not included. ....	136
Fig.III. 15. The proposed gate charge schematic. Confidential .....	137
Fig.III. 16. (a). Motherboard V1 presented in Chap.II. (b). Demo prototype of (V1.A) of gate charge detection method under $R_G$ and $C_{Eq}$ . (c). Evolution of the demo prototype under HV and DUT. (d). Complete V1.A prototype using discrete components. ....	138



Fig.III. 17. Experimental waveforms under equivalent capacitor .....	139
Fig.III. 18. Experimental waveforms of the beginning of the integration, under NTO and HSF: .....	139
Fig.III. 19. Zoom on the complete prototype V1.A .....	140
Fig.III. 20. Oscilloscope waveforms under NTO (Prototype V1.A).....	140
Fig.III. 21. Oscilloscope waveforms under SC-HSF (Prototype V1.A) 1.2kV-80m $\Omega$ , C2M0080120D SiC MOSFET @ $V_{DS}= 400V$ , $V_{GS}= -5/20V$ , $R_G= 10\Omega$ , and $C_1= 80pF$ , $R_1=$ 1K $\Omega$ , .....	141
Fig.III. 22. Oscilloscope waveforms, Circuit under SSD protection (Prototype V1.A) under 400V .....	142
Fig.III. 23. Oscilloscope waveforms, Circuit under SSD protection and without protection	142
Fig.III. 24. View of V1.b prototype .....	143
Fig.III. 25. Experimental waveforms for each DUT @400v and $R_{g\_Ext}= 10\Omega$ . .....	144
Fig.III. 26. Oscilloscope waveforms presenting $V_{GS}$ for both DUT. (a).C2M0080120D (b).C3M0065090D @400V & $R_{g\_Ext}= 10\Omega$ .....	144
Fig.III. 27. Oscilloscope waveforms presenting $Q_G$ (the integrator output in Voltage) for both DUT. (a).C2M0080120D (b).C3M0065090D @400V & $R_{g\_Ext}= 10\Omega$ .....	145
Fig.III. 28. Detection and protection flags with their respective time.....	145
Fig.III. 29. DUT under protection for different $V_{Bus} \in [50,150,250,400V]$ , C2M0080120 DUT, @ $R_{g\_ext}= 10\Omega$ . .....	146
Fig.III. 30. Both DUT under protection @600V and $R_G\_Ext= 10\Omega$ .....	146
Fig.III. 31. (a). $dV_{GS}/dt$ characteristics under “NTO” and “HSF” (b). Derivative circuit .....	147
Fig.III. 32. Simulated waveforms of the gate voltage pattern analyzer for the HSF [169]. (a). IGBT normally turn-on condition. (b). IGBT HSF turn-on condition ( $V_{DC}= 250V$ , $V_{G-Supply}=$ 13V, $R_G= 50\Omega$ , $L_{SC}= 0.5\mu H$ ).....	148
Fig.III. 33. $dV_{GS}/dt$ characteristics under “NTO” and “HSF”, Slope detection approach. Stars represent the levels obtained for the same gate voltage, $V_{GS} = V_{Ref} = V_{Stop}$ , with $V_{Ref} > V_{GS\_M}$ for the slope approach .....	149
Fig.III. 34. $dV_{GS}/dt$ characteristics under “NTO” and “HSF”, Dip approach. Stars represent the levels obtained for the same gate voltage, $V_{GS} = V_{Stop}$ , for the dip approach $V_{GS}=V_{Stop}$ is not a reference level for comparison. ....	150
Fig.III. 35. Detection and protection circuit based on slope and dip approaches. Note: $C_s=$ 100pF, $R_s= 100\Omega$ and other blocks are considered ideals.....	151
Fig.III. 36. Timing chart for derivation detection method under NTO and HSF (a) Slope approach (b) Dip approach. ....	152
Fig.III. 37. Simulation waveforms of the derivation method, using the slope detection, under NTO and SC-HSF .....	153
Fig.III. 38. Simulation waveforms of derivation method using the slope approach under NTO conditions for different $I_{DS}$ and $V_{DS}$ . Typical condition: $V_{Bus}= 800V$ , $I_{Load}= 50A$ , $R_G= 50\Omega$ , DUT: C2M0025120, $L_G= 5nH$ $L_S=L_D= 25nH$ .....	154
Fig.III. 39. Simulation waveforms of derivation method using the dip approach under NTO condition at $V_{Bus}= 200V$ and $I_{Load}= 50A$ . Parasitic inductances are added.....	154
Fig.III. 40. $dV_{GS}/dt$ (solid line) under different $R_G$ with variable reference level (dashed line). .....	155

Fig.III. 41. Detection schematic based on the dip approach (with $R_S \times I_{Sense} \ll V_{GS}$ ) with different level of integration.....	156
Fig.III. 42. Comparator structure , [171].....	158
Fig.III. 43. Three basic voltage references schematics .....	159
Fig.III. 44. Representation of the SSD feedback loop. (a). Internal connection. (b). External connection (c). Bufferized PADs due to the protection diode. ....	160
Fig.III. 45. Simulation waveforms under Cadence of the Gate driver including the detection circuit (dip method) under SC-HSF. (a). without protection (b). with protection. ....	160
Fig.III. 46. Two radar charts displaying multivariate data of the detection time and $dV_{GS}/dt$ peak .....	161
Fig.III. 47. Microscopic zoom at the Dip approach (detection) and SSD (protection).....	162
Fig.III. 48. Layout view of the detection circuit under Cadence™ (dip and slope approach) and the microscopic view of the AGD .....	163
Fig.III. 49. Oscilloscope waveforms of the ASIC including the detection flag, (the protection is not considered) .....	164
Fig.III. 50. $V_{GS}$ under protection, using a pull-down resistor on the Flag_2 .....	164
Fig.III. 51. Oscilloscope waveforms under $V_{Bus}=0V$ showing the detection flag.....	165
Fig.III. 52. Oscilloscope waveforms under NTO and $V_{Bus}= 50V$ .....	165
Fig.III. 53. Oscilloscope waveforms under NTO, double pulse and $V_{Bus}= 200V$ .....	166
Fig.III. 54. Oscilloscope waveforms under SC-HSF @ $V_{Bus}= 200V$ .....	166
Fig.III. 55. Summarized schematic of the different detection methods and their integration level. ....	168
Fig.III. 56. (a). Protection circuit embedded in the gate driver of proposed method. (b). The relationship between $V_{QG}$ and a referential voltage $V_{Ref}$ for normal and SC condition [112]	170

## List of Tables

Tab.I. 1. Driver Configuration overview, Infineon [27] .....	27
Tab.I. 2. Gate driver topologies, insulation and transmission principles depending in application range [75].....	44
Tab.I. 3. Approaches and Integration of basic approaches related to fault detection .....	64
Tab.I. 4. Performances comparison of basic approaches related to fault detection .....	64
Tab.I. 5. Benchmark of the two main detection methods in the literature .....	65
<b>Tab.II. 1.</b> Technologies comparison [119].....	71
<b>Tab.II. 2.</b> Different SiC MOSFETs power transistors for both 2 <sup>nd</sup> and 3 <sup>rd</sup> generation .....	73
<b>Tab.II. 3.</b> Comparison of the commercial gate drivers .....	75
<b>Tab.II. 4.</b> Electrical parameters for the used CMOS transistors in the technology X-Fab 0.18 SOI .....	77
<b>Tab.II. 5.</b> Summary of the specification of the active gate driver.....	78
<b>Tab.II. 6.</b> Level shifter parameters .....	80
<b>Tab.II. 7.</b> Simulated performance of the level shifter for different temperature,.....	81
<b>Tab.II. 8.</b> Pre-amp stages source/sink current including width of each transistor .....	85
<b>Tab.II. 9.</b> Truth tables for both En_P1 and En_N .....	87
<b>Tab.II. 10.</b> Different parameters of the gate driver .....	89
<b>Tab.II. 11.</b> Delay configuration of the AMC, Note: X* is the external delay.....	91

<b>Tab.II. 12.</b> Configuration of HZ and SSD.....	94
<b>Tab.II. 13.</b> Finger and multiplier numbers for each function. (Note the blocks name refers to Fig.II. 28).....	97
<b>Tab.II. 14.</b> Layout size for the ADG .....	98
<b>Tab.II. 15.</b> Typical configuration of the ASIC commands .....	103
<b>Tab.II. 16.</b> Summary of measured propagation delays and rise/fall time between PWM and $V_{GS}$ .....	104
<b>Tab.II. 17.</b> Measured propagation delays and rise/fall time between PWM and $V_{GS}$ for different power supplies and different PMOS enable configurations .....	105
<b>Tab.II. 18.</b> Measured propagation delays and rise/fall time between PWM and $V_{GS}$ for different power supplies and different NMOS enable configurations .....	105
<b>Tab.II. 19.</b> $V_{GS}$ parameters for different AMC configuration @20V .....	106
Tab.III. 1. 2D diagnosis algorithm for HSF. ....	124
Tab.III. 2. Diagnosis algorithm for FUL .....	126
Tab.III. 3. Diagnosis algorithm for OC .....	127
Tab.III. 4. Ratio S for different $V_{GS}$ and different power semiconductors (GaN, SiC IGBT, Silicon) .....	129
Tab.III. 5. Different differential amplifiers parameters.....	133
Tab.III. 6. Different main parameters for both DUT .....	143
Tab.III. 7. Gate charge Immunity Band and Ratio S.....	145
Tab.III. 8. 2D diagnosis for HSF with $V_{GS}$ slope approach. ....	150
Tab.III. 9. 2D diagnosis for HSF with dip approach.....	150
Tab.III. 10. Design and simulation parameters under Cadence .....	158
Tab.III. 11. Different voltage reference circuits parameters .....	159
Tab.III. 12. Different configurations of the commands used to simulate the behavior of Fig.III. 45 .....	161

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**Journal Paper:** .....

- ❖ **Yazan Barazi**, Nicolas Rouger, Frédéric Richardeau, Comparison between ig Integration and vgs Derivation methods dedicated to fast Short-Circuit 2D-Diagnosis for Wide Band Gap Power Devices. Matcom 2020. Accepted: 05/2020.  
<https://doi.org/10.1016/j.matcom.2020.05.011>

**International Conference Paper:**.....

- ❖ **Y. Barazi**, N. Rouger and F. Richardeau, "CMOS Gate Driver with fast short circuit protection for SiC MOSFETs," *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Vienna, Austria, 2020, pp. 94-97, doi: 10.1109/ISPSD46842.2020.9170164.  
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- ❖ **Y. Barazi**, F. Boige, N. Rouger, J. -M. Blaquiere and F. Richardeau, "'ig,vgs' Monitoring for Fast and Robust SiC MOSFET Short-Circuit Protection with High integration Capability," *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France, 2020, pp. P.1-P.10, doi: 10.23919/EPE20ECCEurope43536.2020.9215619.  
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- ❖ **Yazan Barazi**, Nicolas Rouger, Frédéric Richardeau. *Oral presentation*. Comparison between ig Integration and vgs Derivation methods dedicated to fast Short-Circuit 2D-Diagnosis for Wide Band Gap Power Devices. Electrimacs 2019. Salerno, Italy, 05/2019  
<https://hal.archives-ouvertes.fr/hal-02180892v1>

**National Conference Paper:** .....

- ❖ **Yazan Barazi**, François BOIGE, Nicolas ROUGER, Jean-Marc BLAQUIERE, Sébastien Vinnac, Frédéric RICHARDEAU, *Article accepté pour présentation orale*. Protection rapide et robuste contre les courts-circuits internes de convertisseurs à base de MOSFETs SiC. SGE 2020. Nantes, France 06/2020.

**Titre :** *Protection rapide en régime extrême de court-circuit des transistors MOSFET SiC par fonctions intégrées en technologie ASIC CMOS*

**Mots clés :** Conception CMOS - Electronique analogique et numérique - électronique de puissance - Commande de transistors grands gaps - MOSFET SiC - Court-Circuit & protection

**Résumé :** Les transistors de puissance grands gaps tels que les MOSFETs SiC repoussent les compromis classiques en électronique de puissance. Brièvement, des gains significatifs ont été démontrés, meilleurs rendements, couplés à une augmentation des densités de puissance offerte par la montée en fréquence de découpage. Les MOSFET SiC à haute tension présentent des spécificités telles qu'une faible tenue en court-circuit par rapport aux IGBT Si, un oxyde de grille aminci, et une tension de commande rapprochée grille-source élevée. La polarisation négative sur la grille à l'état bloqué crée un stress supplémentaire qui réduit la fiabilité des SiC. Ainsi, cette technologie fait émerger des besoins spécifiques de surveillance-protection ultra-rapides et d'adaptation de la commande rapprochée. Pour cela, le travail de cette thèse se focalise sur deux études de gate driver pour surmonter ces contraintes, toute en gardant un compromis entre niveau d'intégration-CMS/ASIC-CMOS-rapidité-robustesse.

**Title:** *Fast protection for SiC MOSFETs in extreme short-circuit conditions by integrated functions in CMOS-ASIC technology*

**Keywords:** CMOS design - Analog and Digital Electronics - Power Electronics - Control of Wide Band Gap transistors - Gate Driver - MOSFET SiC - Short-Circuit & Protection

**Abstract:** Wide bandgap power transistors such as SiC MOSFETs push furthermore the classical compromises in power electronics. Briefly, significant gains have been demonstrated by SiC transistors: better efficiency, coupled with an increase in power densities offered by the increase in switching frequency. HV SiC MOSFETs have specific features such as a low short-circuit withstand time capability compared to Si IGBTs and thinner gate oxide, and a high gate-to-source switching control voltage. The negative bias on the gate at the off-state creates additional stress which reduces the reliability of the SiC MOSFET. The high positive bias on the gate causes a large drain saturation current in the event of a short circuit. Thus, this technology gives rise to specific needs for ultra-fast monitoring and protection. For this reason, the work of this thesis focuses on two gate drivers studies to overcome these constraints, with a compromise between CMS/ASIC-CMOS integration level-speed-robustness.