RF design methodology based on MOS transistors for circuit / technology optimization

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Abstract

Thanks to advances in recent technological nodes, the weak and moderate inversion regimes of the MOS transistor become interesting for low power RF circuit design. This work proposes a design-oriented model and an RF design methodology based on the inversion charge of the transistor.

Our proposal considers the most impacting short-channel effects of advanced nanometric CMOS technologies to accurately model the dependence on the drain voltage and to describe correctly not only the I-V curves but also the small signal model of the MOS transistor.

In this regard, firstly a the 7-parameter model has been developed and implemented in Matlab for STMicroelectronics 28nm FD-SOI technology. The feasibility and accuracy of the model have been verified by direct comparison to DC measurements, demonstrating a good agreement for the drain current behavior and its derivatives as a function of the transistor node voltages. Obtained results open the door to estimating the non-linear behavior of the transistor.

Additionally, a parameter extraction methodology is present to estimate the model parameters based on simple simulations (or DC measurement campaigns) proving its accuracy for different channel lengths of the studied technology.

Finally, a simple RF design methodology based on the proposed design-oriented model has been proposed for the case study of a resistive feedback LNA. The developed design methodology allows to explore the design space for the selected resistive feedback LNA case study. This exploration allows to determine the best operating point depending on the targeted specifications. The results obtained from the model are compared with simulation results in Cadence and actual probe-station measurements from a fabricated LNA, for a given sizing and biasing of the circuit. Obtained results prove a really good accuracy among the three of them. Furthermore, a really simple study of the LNA performances under the variation of the proposed model parameters is carried out to provide a first glance on the way to circuit/technology co-optimization.

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General Introduction

The interest in producing low power consumption circuits for radiofrequencies (RF) applications such as Internet of Things (IoT) has led the current CMOS technologies to evolve accordingly to meet the requirements for these standards. This has allowed the transistors in today's technology nodes to have a higher transit frequency (f_T) and therefore to operate at weak and moderate inversion regimes.

This has led to the development of design methodologies based on inversion coefficient to be implemented for RF circuit design. However, the simplified models used on these methodologies fail to correctly represent the drain current dependence on V_D and the short channel effects (SCE) on the most advanced CMOS technologies. As a result, previous design methodologies rely on cumbersome lookup tables to capture the V_D dependencies and are not able to address the non-linearity behavior of the targeted circuits, mainly dominated by SCEs.

In this thesis work, the aim is then to address the improvement of the RF circuit design methodologies based on the inversion coefficient of the MOS through two main axes connected to each other.

The first one is to work directly on transistor modeling based on its inversion charge to considering the SCE and the dependence on V_D to accurately reproduce the transistor characteristic I-V curves, but also the partial derivatives of the current.

The second axis is based on implementing this model to improve RF low power circuit design methodologies based on the transistor inversion coefficient in order to consider the modeling of transistor non-linearities within the transistor performance considerations. For this purpose, a specific LNA topology will be used to implement the proposed design methodology.

This document begins by describing the context and the state of the art of both design methodologies for RF circuit applications and design-oriented models in Chapter 1:. In Chapter 2:, the proposed design-oriented model based on the inversion charges of the MOS transistor is described and Chapter 3: presents a methodology to extract the corresponding parameters of the model along with an evaluation of the model robustness for different channel lengths. Chapter 4: presents the design methodology applied to a resistive feedback LNA along with the comparison with respect to the simulation and on-chip measurements of the circuit. Finally, Chapter 5: summarizes the contributions of this work as well as the perspectives for future work on the subject.

Chapter 1: Context and State of the Art

1.1 Internet of Things: Towards ultra-low power RF devices

It is a well-known fact that the number of connected devices has increased exponentially and that this number will continue to increase in the coming years. At the moment of writing this manuscript, it has been estimated that there are more than 10 billion IoT (Internet of Things) devices in the world. Reducing the energy consumption of this huge number of devices goes beyond extend the battery life of the device. Actually, it can have a significant impact in the global power consumption with a non-negligible effect in our society's carbon footprint. For this reason, we must continue to explore how to reduce the energy consumption of electronic devices, reduce their cost and increase their lifetime.

Circuit design for low power RF applications has evolved over the years thanks to advances in technology and also thanks to circuit design methodologies improvement. Advanced technologies and technology node reductions have pushed RF design from the strong inversion regime toward moderate and weak inversion regimes of operation of the MOS transistor, especially because of the f_T increase but also due also to the decrease of the supply voltages that comes with the shrink of the transistor channel length.

Advances in CAD simulation tools have allowed designers to develop state-of-the-art devices in nanometric technologies based on accurate and complex compact models. However, the complexity of the CAD models make designers lose a bit of their design intuition and the understanding of the physical effects of the transistor on the circuit performances is lost. On the other hand, analytical methodologies based on traditional piecewise models are not valid anymore due to the physical effects that are now present in the latest technologies.

Design methodologies have then evolved to follow these major technology changes. Most of these new methodologies are based on inversion coefficient approach since it is an accurate and convenient way to describe the MOS behavior in weak and moderate inversion regimes. From basic recommendations on the inversion level up to complex methods based on Look-up Tables (LUTs) and analytical design approaches, many different design strategies have been proposed and will be detailed here. A promising method, that will be privileged in this PhD manuscript, relies on the use of simplified design-oriented charge-based models based on EKV and ACM models. These design-oriented models use a small set of parameters to describe the

MOS behavior and allow to define analytical design methodologies based on physical design equations.

However, current models used for the analytical design methodologies fail to accurately capture non-linearities and V_D dependency which highly limits their use. This is the reason why there is a need for accurate but simple design-oriented models that helps designers to develop non-linearity-aware design methodologies. This is indeed one of the key objectives of this thesis.

This chapter will expand on the concepts described here and the motivation for this thesis work. Inversion coefficient-based design methodologies will be first studied in the state of the art. Then, design-oriented models will be analyzed in order to set the basis of this work.

1.2 Circuit design methodologies

1.2.1 Circuit design in strong inversion: maximum f_T

In the 90's with the advance on wireless communications through standards as global system for mobile, GSM, (from 900 to1800 MHz) and the further development of the global positioning system, GPS, (~1100 to 1600 MHz), the demand for RF integrated circuits (RFIC) highly increased. At that time, designers started to use CMOS technologies for radiofrequency (RF) devices. To obtain the best possible frequency response and the best performances that comply with the standards requirements, RF circuits were designed in strong inversion to reach the highest transit frequency, f_T.

A clear example of this, is the work presented by Shaeffer *et al.* in 1997 [1] with the implementation of an LNA (Low Noise Amplifier) for a GPS receiver operating at 1.5 GHz in 0.6 μm technology. Their results demonstrate the interest in using MOS transistors for RF applications and point to future improvements that arrived with the transistor size reduction of the more recent CMOS technologies.

Thanks to the advance of technological nodes, stronger f_T and lower supply voltage are now possible. With a low voltage supply, the transistor cannot operate in saturation or strong inversion especially for circuits such as a cascode configuration where the supply voltage is divided among several transistors. Hence, transistors have to operate with a V_{DS} closer to the threshold voltage, pushing the design toward the weak and moderate inversion regimes and in the low saturation region. Fortunately, the increase in f_T makes possible to operate the transistors at RF frequencies even in weak and moderate inversion regimes.

1.2.2 Circuit design in weak inversion: the interest of the g_m/I_D characteristic

In 1977, Vittoz and Fellrath in [2], highlighted the interest of weak inversion regime for low-power applications, demonstrating the concept with two different circuits, an amplitude detector and a low-frequency bandpass amplifier.

Furthermore, the weak inversion regime keeps high interest for the design of low-power RF circuits, since the maximum of g_m/I_D is reached in this zone, as illustrated in Figure 1-1. Thus, the trade-off between the intrinsic gain of the transistor, proportional to g_m, and the power consumption, I_D, can be optimized.

However, working at high g_m/I_D to improve the energy efficiency of the MOS transistor implies large W to compensate for low I_D while keeping constant g_m. Large W leads to large parasitic capacitances which finally reduces the bandwidth of the circuit. This phenomenon is well described in Figure 1-2, where the f_T of a MOS is plotted as function of the inversion coefficient. This shows that where g_m/I_D is at its maximum, f_T is at its minimum, simply justifying why g_m/I_D design methodologies were only dedicated to low frequency designs up to the early 2010.

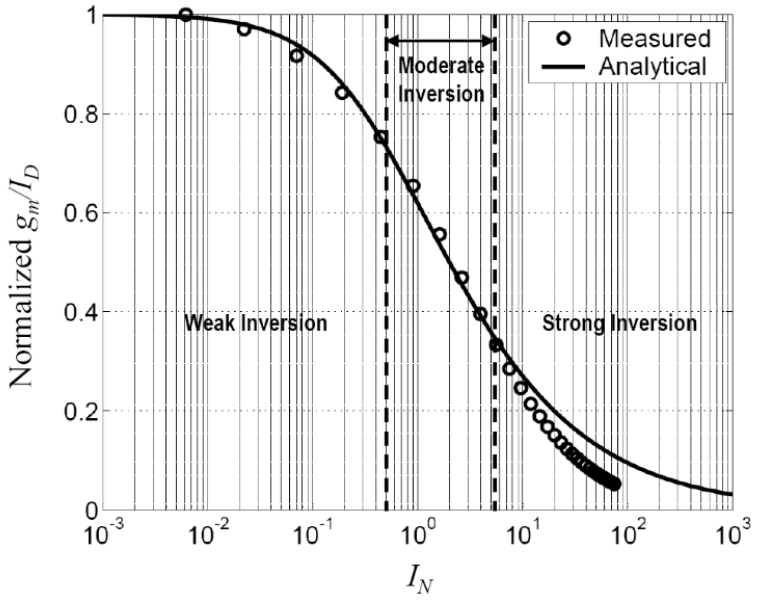


Figure 1-1. Normalized g_m/I_D characteristic respect to the inversion coefficient [3].

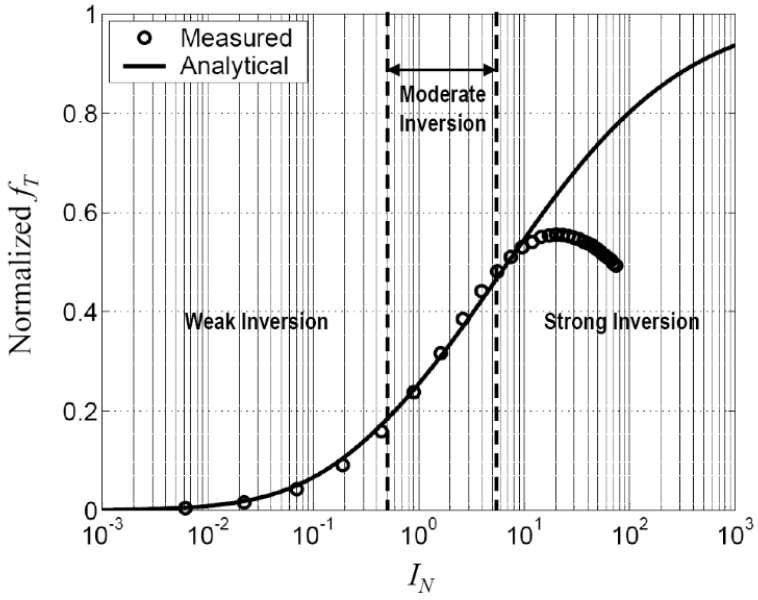


Figure 1-2. Normalized f_T characteristic respect to the inversion coefficient [3].

1.2.3 Circuit design in moderate inversion: recent technologies

$g_m.f_T/I_D$ characteristic

The importance of the transit frequency, f_T, and the energy efficiency, g_m/I_D, characteristics for low-power RF circuits has been highlighted in sections 1.2.1 and 1.2.2 . In advanced technology nodes with the increase of f_T, the circuit operation frequency is no more a limitation in the RF domain and lower inversion regime can be considered to save power. Then, a new figure of merit (FoM) becomes interesting for low-power RF domain: $g_m.f_T/I_D$, it combines the desired operating frequency or frequency band, and a good trade-off between the gain and the power consumption.

In [3], Shameli and Heydari present an study for a 0.18 µm CMOS technology that leads them to conclude that the moderate inversion is the best operation regime, as the maximum of $g_m.f_T/I_D$ is reached at this regime as illustrated in Figure 1-3. Then, for a given technology, the designer shall investigate which regime give the best $g_m.f_T/I_D$ and then, shall use it for its entire design. As a proof, [4] shown that the typical FoM of a LNA is maximized in the same region as $g_m.f_T/I_D$ as depicted in Figure 1-4.

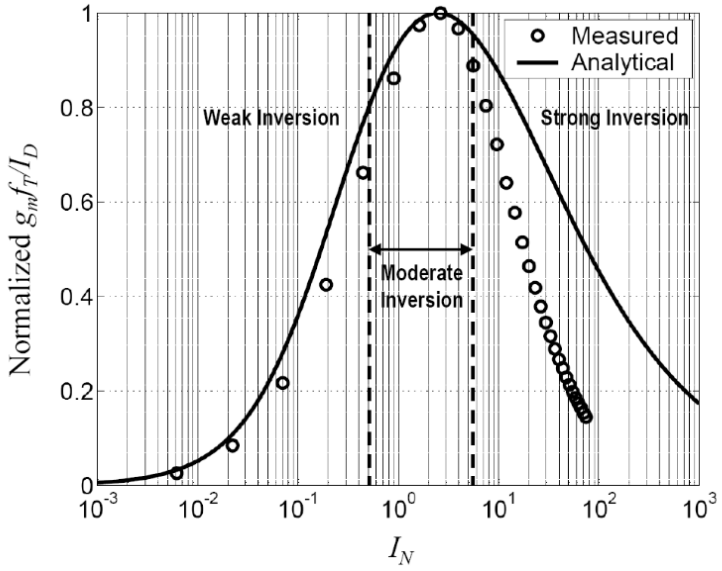


Figure 1-3. Normalized $g_m.f_T$ /I_D characteristic respect to the inversion coefficient [3].

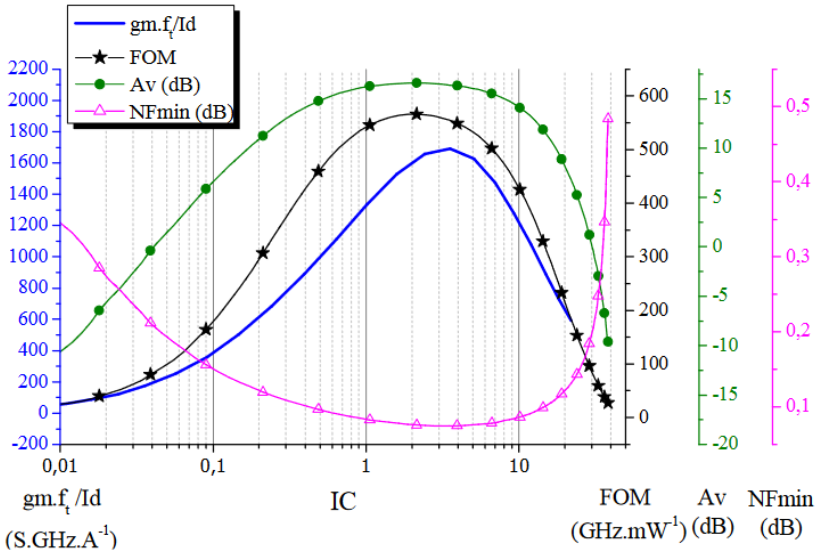


Figure 1-4. $g_m.f_T$ /I_D characteristic used as design metric for an RF LNA in [4] based on the inversion coefficient (IC).

1.2.4 Circuit design using Figures of Merit

To choose an inversion regime better suited to a topology, authors proposed to explore FoMs that are more properly linked to one specific type of block in the RF reception chain. This allows to determine an inversion level not only based on the technological point of view, but also by considering the designed function (LNA, VCO, etc.). To illustrate this, Song *et al.* [5] propose that g_m^2/I_D can be used as a FoM to optimize the performance of the LNAs, as this characteristic allow to estimate the better

biasing taking into account the noise figure, F, gain, G, and power consumption, P. The article shows that this characteristic follows the same trend that the figure of merit for LNA in (1-1), which is quite traditional because it considers the most critical performances in the design of an LNA.

$$FoM_{LNA} = \frac{G}{(F-1)P} \tag{1-1}$$

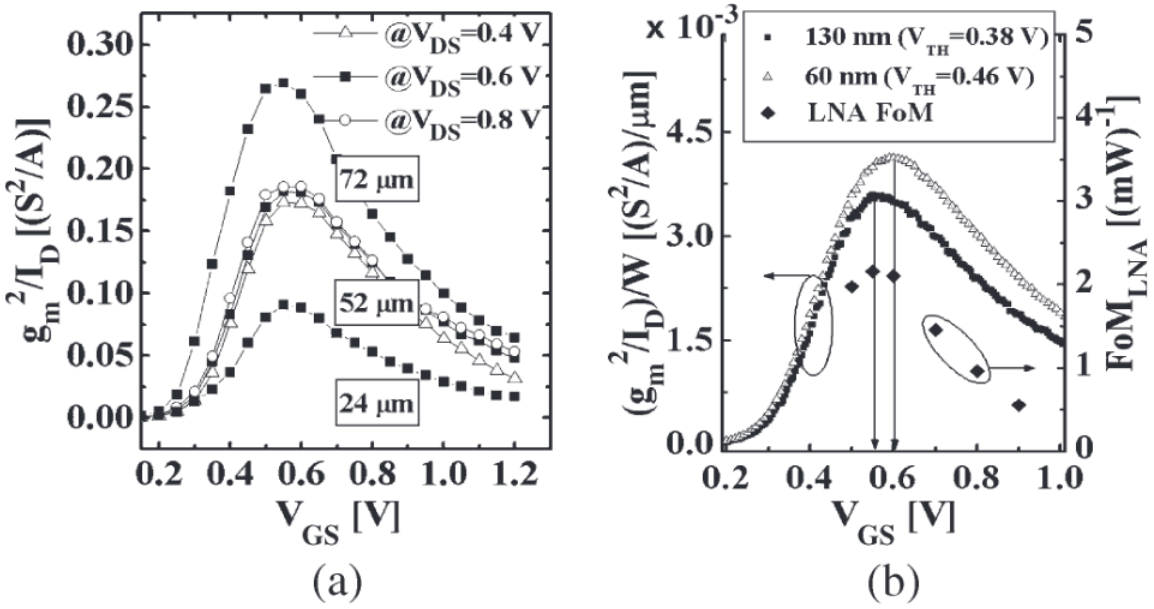


Figure 1-5. g_m^2/I_D and FoM for LNA. a)L=130nm, different widths (24,52,72um) and several VDS, presenting an optimum around V_{GS}=0.55V. b)Similar trends for both characteristics: FoM for LNA and g_m^2/I_D, good estimation of corresponding V_{GS} for the maximum of FoM for the LNA [5].

Following the same kind of proposal, in [6], Chicco *et al.* present a FoM to compare different topologies of LC Oscillators based on LUTs with respect to the inversion coefficient, IC, to determine in which inversion regime, a certain oscillator class is more performant. In this case the FoM is given by (1-2), considering power consumption, P_{DC}, and phase noise $\mathcal{L}(\Delta f)$ depending on IC.

$$FoM_{LC\_osc} = \frac{kT}{\mathcal{L}(\Delta f, IC)P_{DC}(IC)}\left(\frac{f_0}{\Delta f}\right)^2 \tag{1-2}$$

The three topologies studied are presented in Figure 1-6, and Figure 1-7 illustrates that the classes B and C reach the maximum FoM in moderate inversion regime, while the class D has its optimum in weak inversion regime.

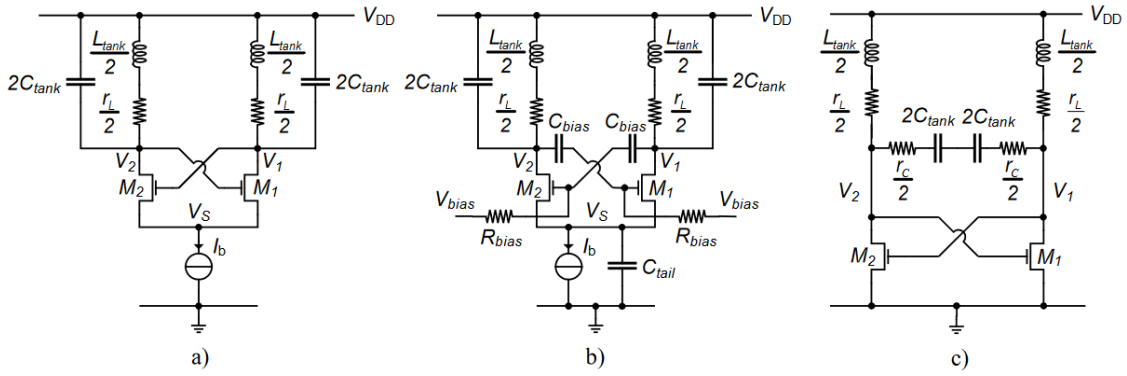


Figure 1-6. Three topologies of LC oscillators studied in [6]: a) Class-B, b)Class-C, c)Class-D.

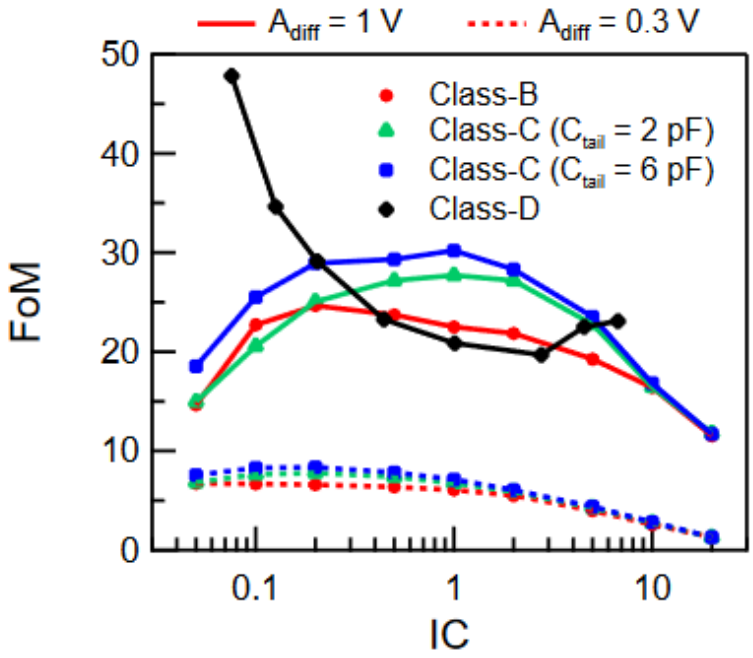


Figure 1-7. FoM for LC Oscillators respect to IC [6].

1.2.5 Design methodologies based on design space exploration

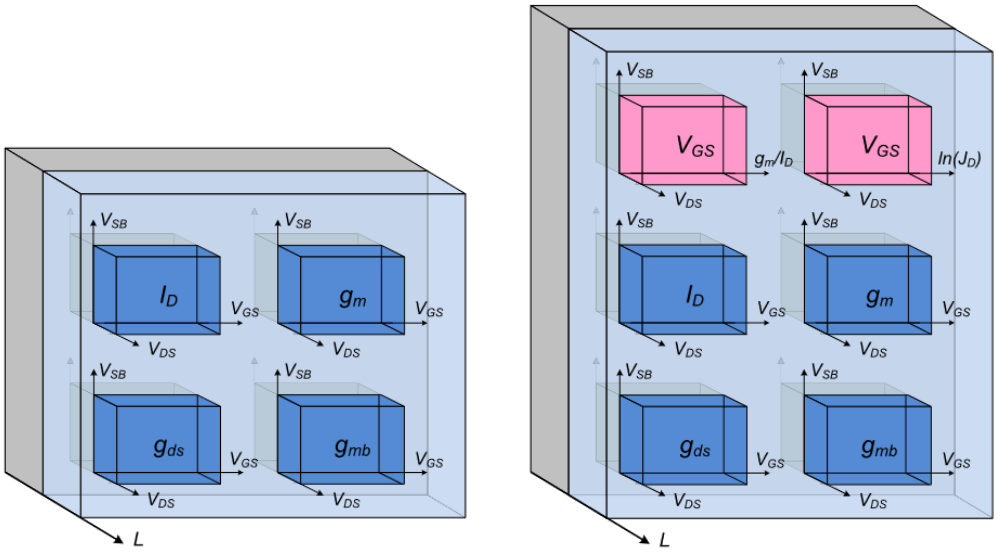
FoMs based on the MOS transistor characteristics can be very interesting to make a comparison between different technologies and can give an overview of the inversion regime in which a transistor should operate depending on some characteristics. However, it has been shown that these FoMs are not ideal since they focus on general characteristics and lead to an optimal trade-off. However, they fail to help the designer when particular requirements are targeted. Depending on the specific circuit and its application, the optimum inversion regime will differ from a circuit to another.

For this reason, other design methodologies were developed to explore the design space and to find the optimum operating points regarding a specific topology and requirements from particular applications.

In this regard, there are two trends in RF low-power circuit design methodologies. On the one hand, methodologies based on LUTs and on the other hand, methodologies based on design-oriented models leading to a quasi-analytical/ analytical-based design. As will be detailed later, generally the design-oriented model methodology is complemented with the LUTs or with simulation information to provide better results for design.

1.2.5.1 Circuit design based on Look Up Tables

The LUTs are charts where a set of characteristics of the transistor are plotted under the variation of other parameters in the circuit, or design variables such as the size of the transistor or the components that make up the circuit. The LUTs can also contain the circuit performance estimation depending on whether other performance or transistor characteristics are varied. It is essential to remember that the main interest of the LUTs is that it allows a global observation of the design space of the circuit under the variation of different variables.



(a) (b)

Figure 1-8. Set of 4D LUTs based on MOS transistor parameters to limit the design space for a given circuit to reach specifications: (a) First proposition (b) Improvement for fastest estimation of the design space [7].

The general concept of the LUTs is illustrated on Figure 1-8(a) where Youssef *et al.* present 4 of the main parameters of the MOS transistor to evaluate several scenarios to design two circuits, a bandgap reference and a folded cascode. However, they added two other parameters (Figure 1-8(b)) to the design space in order to reach

a given set of specifications [7]. This demonstrates that a series of criteria must be taken into account to select the LUTs to be used, without neglecting essential elements for the circuit design to target all specifications, what may not be an obvious task.

The design based on LUTs has proven to be of great interest for the design of all types of circuits as it is found in a whole series of different publications. Here, we will mention only a few that are relevant as they integrate the energy efficiency feature, g_m/I_D. In [8], Jespers and Murmann present a guide for circuit design based on LUTs for different kind of circuits employing CMOS transistors that allow to obtain results very close to the simulation while dealing with the different trade-offs that occur when designing RF circuits, highlighting furthermore the interest of the g_m/I_D characteristic.

In [9], a design methodology for common source Low Noise Amplifiers (LNAs) is proposed based on the gain, G, and noise figure, NF, in function of g_m/I_D to determine the design space for the circuit as illustrated in Figure 1-9. In [10], a similar proposal to determine the sizing and the biasing of a capacitive feedback LNA is presented based on the same performances of gain and noise figure. Behind of the both methods presented in publications [9] and [10], the design methodology applies an algorithm with several loops to optimize and determine of the operating point of the circuit depending on the targeted specifications as depicted in Figure 1-10.

Apart from LNAs, LUT-based design methodologies have been also developed for other circuit families. Thus, an LC VCO is conceived in [11] through an optimization loop based on the characteristics of g_m/I_D and g_{ds}/I_D allowing to minimize the phase noise taking into account the constraints of current consumption, output voltage and output amplitude. In [12], the LUTs are used to develop a design methodology for an envelope detector. Here, the second order non-linearities of the transistor are employed for the operation of the circuit demonstrating the interest of LUT approaches for non-linear devices or non-linearity studies. The second derivative divided by the current is used as FoM and a guide to reach the final conditions for the circuit.

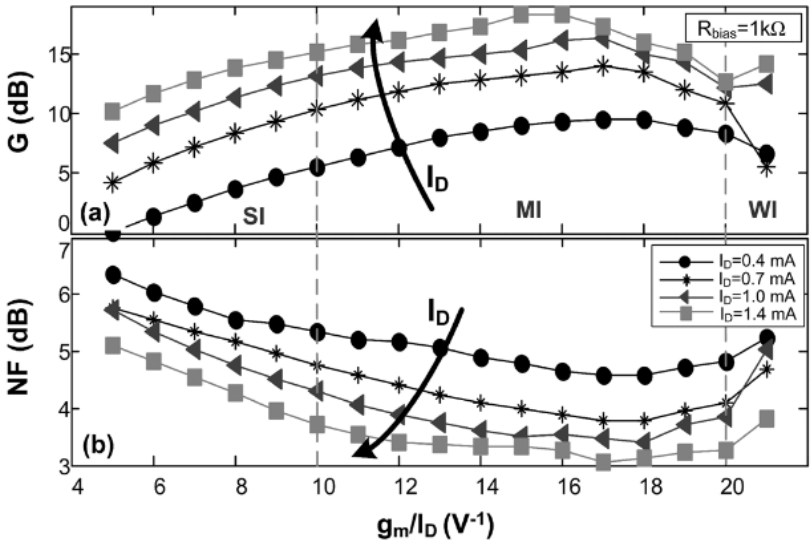
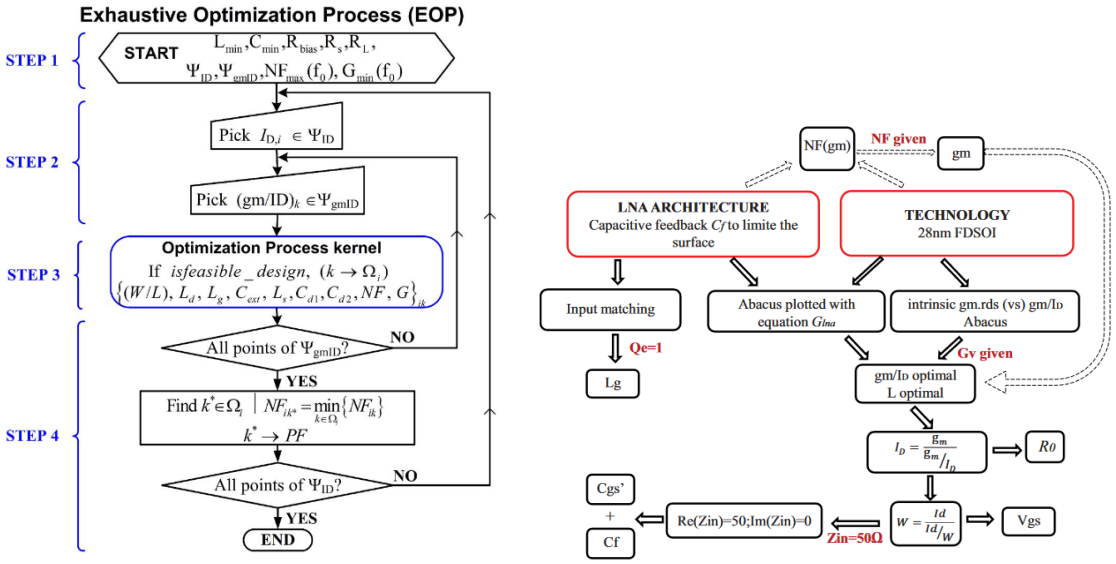


Figure 1-9. (a) Gain and (b) Noise Figure based on g_m/I_D for different drain currents to estimate the design space for common source LNAs at 2.4 GHz [9].



(a) (b)

Figure 1-10. Algorithm for sizing and optimization of (a) common source LNA [9] and (b) Capacitive feedback LNA [10].

1.2.5.2 Circuit design based on design-oriented models

The design-oriented models that are considered in the methodologies explained in this section are based on the inversion level of the transistor as it is of major interest for RF low-power circuit design. A trend in the main algorithm of these design methodologies is noticeable and can be illustrated as shown in Figure 1-11. Firstly, a model based on the inversion coefficient describing the transistor at a technological level is proposed, secondly, an analytical study of the circuit is carried out taking into

account the most critical performances and finally, a determination of the transistor size and biasing is done by linking both, the transistor model and the circuit analysis through certain variables such as the width and length of the transistor and the inversion coefficient level, W, L and IC respectively, in this example taken from [13].

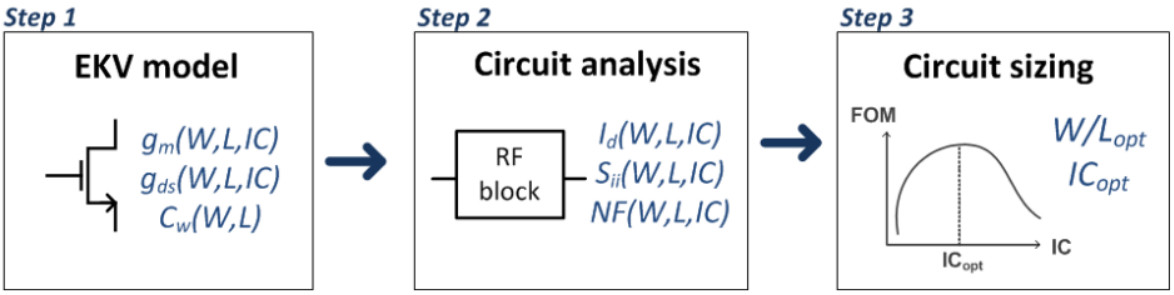


Figure 1-11. Design methodologies based on the inversion coefficient-based models [13].

In the case of the LNA presented in [13], an optimum point is found depending on the target application using a single FoM (1-3) that is optimized through the design algorithm. This determines the design space presented in Figure 1-12, where the FoM is plotted as a function of two of the three parameters initially set, W and IC. In [14], a similar procedure is followed using also EKV model to represent the MOS behavior, what slightly differs from the previous work is simply the FoM (1-4), which, being also for an LNA, takes into account the same criteria, although using the power instead of the current directly.

$$FoM_{LNA[13]} = \frac{BW_{-3dB} G_v}{I_{total}|F-1|} \tag{1-3}$$

$$FoM_{LNA[14]} = \frac{BW_{-3dB} G_v}{P_{DC}|F-1|} \tag{1-4}$$

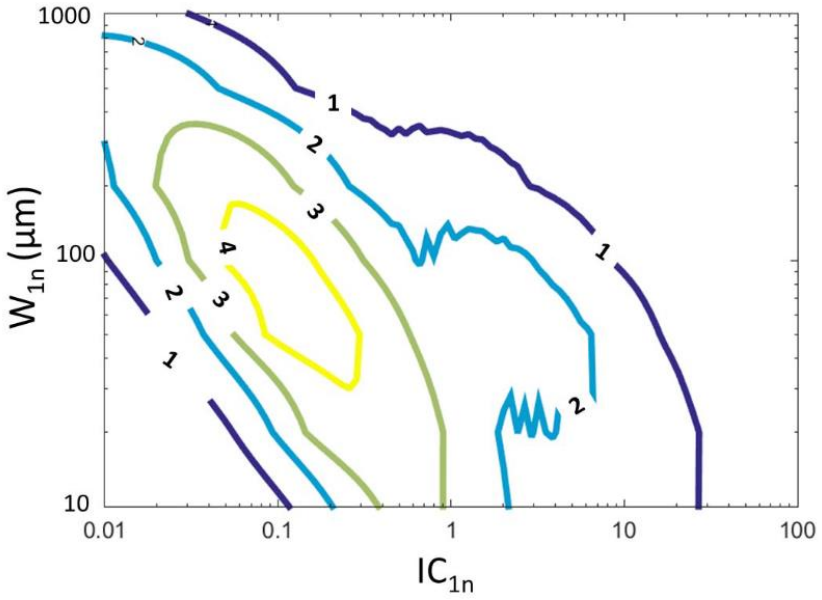


Figure 1-12. Design space for LNA based on FoM with respect to W and IC [13].

The authors in [15] presents a design methodology for a resistive feedback LNA also employing an inversion coefficient-based model (ACM). This design methodology is more focused on achieving the desired performances without necessarily going through a FoM. The proposal consists of expressing the performances as a function of certain metrics of the transistor, for example the gain, G_v, in function of the g_m/I_D characteristic or the inversion coefficient, i_f, as illustrated in Figure 1-13 or the noise figure, NF, in function of g_m. This methodology allows to reach in a direct way the polarization and sizing of the transistor.

If we take a closer look at what the different publications presented in this section have in common, where various design methods for inductorless LNAs are illustrated, none of them take into account one of the most important metrics of this block for an RF reception chain, the IIP3. The 3rd order input intercept point, IIP3, is a fundamental metric to show how linear (or not linear) is the behavior of a circuit. In the case of the LNA, high linearity prevents the generation of undesired signals in the operating frequency band and improve the resilience to interferers and blockers.

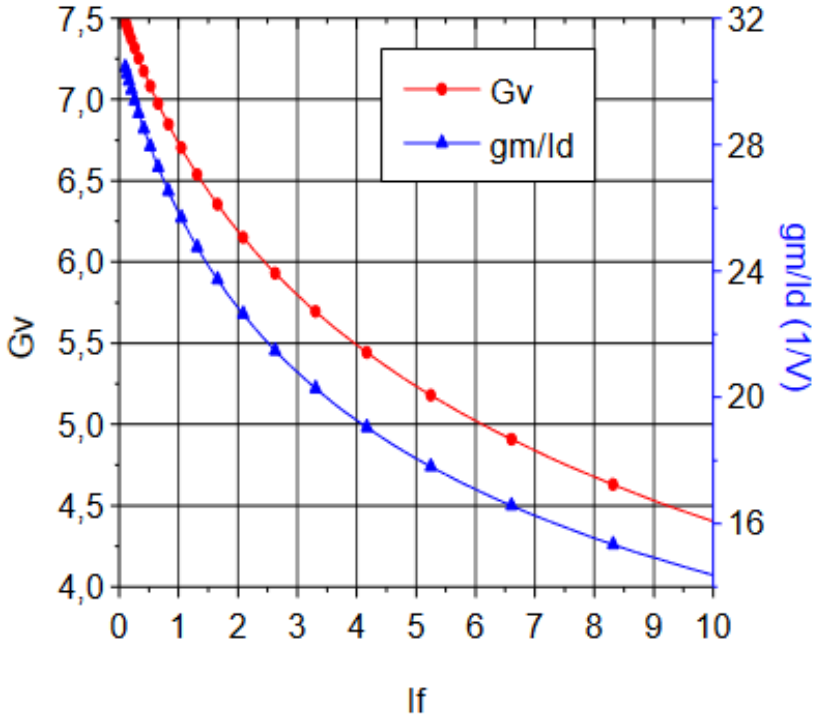


Figure 1-13. Gain, G_v, and energy efficiency factor, g_m/I_D, in function of the inversion coefficient, i_f [15].

1.2.6 Limitations of the design-oriented models for circuit design methodologies

The design methodologies built from models based on the inversion coefficient are very interesting because they help the designer understand the circuit behavior based on analytical equations. In addition, they provide a powerful tool to easy explore the design space that leads to required specifications taking into account the trade-offs. However, as highlighted, these methodologies are not suited to non-linear studies. This comes from some limitations in the models used that do not consider non-linearities that come with short-channel effects (SCEs).

In order to improve the proposals in these design methodologies, it is required to improve the design-oriented models, particularly with the aim of correctly estimating the transistor nonlinearities, to integrate metrics such as the IIP3 in the design of LNAs.

Subsequently, an overview of the models currently used for circuit design for advanced MOS technology nodes and their progress over the last few years is presented.

1.3 Design-oriented models

1.3.1 Analytical models for circuit design

Models describing MOS transistor behavior for the most advanced technological nodes can be classified into two families of models: compact models implemented in simulation tools and design-oriented analytical models that are simple enough to be used in hand calculations or can easily be implemented in algorithms to predict the performances of a given circuit. Each of them is presented below and their advantages and drawbacks for RF low power circuit design are briefly summarized.

1.3.1.1 Compact models in CAD tools

Compact models implemented in CAD (Computer-Aided Design) simulation tools are based on the complex semiconductor physics of the MOS transistors, but it also includes certain fitting parameters that allow to bring these models closer to the measurements obtained directly from the implementation of the technology. Making a focus on the chosen technology to carry out this thesis work, the 28nm FD-SOI (Fully depleted silicon on insulator) [16] of STMicroelectronics, it is a very advanced and complex technology that requires models with hundreds of parameters to accurately describe the transistor behavior in simulation tools.

FD-SOI technologies in SPICE simulators and industrial design kits are modeled by BSIM-IMG model [17], [18] but also, by UTSOI2 model [19], [20], which additionally takes into consideration the effects related to the ultrathin body and buried oxide (UTBB). Of course, these models are very accurate in predicting the behavior of a given circuit, but they are difficult to understand at the technological parameter level. Using directly these models in design requires a design approach relying only in simulations that leads to extensive simulation campaigns to properly size and bias transistors in order to comply with a set of given design specifications.

For this reason, it is necessary to use simpler analytical design-oriented models that preserve the physics of the transistor and describe in a more general way its behavior with sufficient accuracy to perform preliminary design studies. Preliminary sizing, either with hand calculations or with rather simple algorithms implemented in a computer, allows the designer to start CAD based optimization with compact models from an operating point that is closer to the optimum, saving a huge simulation time.

1.3.1.2 Analytical models based on the inversion coefficient

In the last few years, design-oriented models based on the transistor inversion level are gaining strength over the conventional piecewise model, as they allow a better approximation to the transistor behavior in advanced technologies, especially in moderate and weak inversion regimes by using a small set of parameters.

ACM (Advanced Compact MOSFET) [21]–[24] and EKV (named after its developers' initials: C. C. Enz, F. Krummenacher and E. A. Vittoz) [25]–[29] models are based on inversion charge linearization describing continuously the MOS drain current characteristic as a function of the terminal voltages. The main differences between both models lie in different definitions for the normalization charge and the pinch-off voltage. However, from a designer's point of view, the equations are similar and can be transposed from ACM to EKV or vice versa.

The main advantage of the simplest versions of these models is that by using a small number of parameters, the model is easy to understand and to be used in design methodologies through hand calculations or simple algorithms.

1.3.2 Evolution of the inversion coefficient-based models

Both, the ACM and the EKV models have followed a very similar trajectory in terms of their development. The interested reader is referred to the corresponding books, [23], [24] for ACM and [27] for EKV, for a further explanation of their basis, extensions and even some application cases. However, as far as we are concerned, it is more interesting to start by presenting the basic versions of both models and the evolution that has taken place for their use in more advanced nodes.

The simplest version of the models based on the inversion coefficient have three main parameters as presented by Schneider *et al.* in [30] based on the ACM model or by Jespers *et al.* in [31] based on the basic EKV model, introducing also the first equations describing the harmonic distortion in the transistor, giving a first step towards the estimation of transistor nonlinearities. Up to this point, the modeling of the drain current is independent on the drain voltage, this limitation is considered by Jespers in [31], through calibration curves for two of the three main parameters, which leads to an equivalent LUT to deal with this issue making this solution unpractical for hand calculations with arbitrary transistor biasing.

To go beyond the three-parameter model presented above, several authors consider that one of the main effects to be modeled next is the carrier velocity saturation effect. In [32], Mangla proposes three different ways to model this effect depending on the effective carrier mobility, in the end, most authors who take up this effect in the model tend to take the same approach among the proposed ones.

This fourth parameter integrated in the model is directly related to the carrier mobility saturation effect, but in general, it is also fitted to capture other SCEs presented in saturation and in strong inversion for the MOS transistor operation [28], [33]–[35]. The non-linearity behavior of the transistor is also deduced under the resulting 4-parameter model that may be very useful in many analog and RF design scenarios, as it represents a good trade-off between complexity and accuracy.

However, the simplicity of the model comes at the cost of not describing the linear region and being limited to a fixed value of drain voltage.

Adornes *et al.* proposed very recently (in 2021) [36] a different approach for a 4-parameter inversion coefficient-based model focused on ultra-low voltage applications adding to the basic 3-parameter model a parameter related to the drain induced barrier lowering effect which becomes significant for short-channel devices. This parameter is essential to accurately describe SCEs in weak and moderate inversion regimes of the MOS transistor.

The simple inversion coefficient-based analytical models already proposed until these days are very useful as they are employed for the transistor operation regions for which they have been conceived. Nevertheless, there is still an interest on developing a simple analytical model that describe accurately all the inversion regimes and the operation from linear to saturation regions of the MOS transistor.

1.4 Motivation

Advanced nanometric technologies imposed the need for more accurate but simple analytical models that allow to describe the operation of the MOS transistor in all operation regions (from linear to saturation regions) and all inversion regimes (from weak to strong inversion regimes) that additionally can be implemented in adapted design methodologies for RF low power circuit design.

Two main joint objectives are addressed in this thesis: on the one hand, the development of a design-oriented model for non-linear aware design methodologies and in the second hand, the development of a sizing methodology for a LNA to validate the efficiency of the proposed model in the context of RF design. Concerning the model, the ACM formulation will be chosen as a basis of the work. The basic 3-parameter ACM model will be refined to describe several of the most important SCEs, especially through parameters that have a physical meaning and that are not only based on the optimization or fitting of the device measurements. In addition, it is sought that this model provides modeling features that can be integrated in a design methodology for RF low power circuits, especially integrating metrics such as IIP3, which implies a correct modeling of the transistor non-linear behavior.

Chapter 2: Design-oriented 7-Parameter Model

The previous chapter has confirmed the need for an improvement in the proposal of design-oriented models, especially for more advance nanometric technologies. Simple models are required that can describe well the MOS transistor behavior from simple but representative parameters that can be used in the early stages of the design, to size the circuit using analytical or algorithm-based methodologies. Of course, the use of comprehensive SPICE models like UTSOI2 [19], [20] is still a fundamental step for design validation.

Therefore, taking up the current state of the design-oriented models, basic 3-parameter EKV and ACM inversion coefficient-based models [21], [27], although accurate enough for describing a long-channel transistor behavior, are not appropriate for advanced technologies, where short-channel effects (SCEs) dominate the behavior of the transistor. This chapter proposes an all-region, all-regime 7-parameter inversion coefficient-based model that considers the most impacting SCEs present in nanometric technologies, i.e., drain-induced barrier lowering (DIBL), carrier velocity saturation, carrier mobility reduction, and channel length modulation (CLM).

This chapter follows a didactical approach to present the model. As a starting point in our derivation, we first introduce the basic 3-parameter ACM model. This model employs the threshold voltage (V_{T0}), the specific current (I_{S0}), and the subthreshold slope factor (n) to describe an all-region DC model of a long-channel MOS transistor. Then, SCEs are introduced one by one and incrementally added to the model equations illustrating their effects on the I-V characteristics of the MOS. Comparisons to silicon measurements show the cumulative improvement of the model fitting when introducing each new parameter.

After presenting the DC modeling of the transistor, the small signal modeling is introduced, using first order derivatives of the drain current. Then, high order derivatives are considered to address the description of the transistor nonlinearities. Finally, the perspectives of a complete model considering the high frequency behavior are discussed. Conclusions on the proposed model are drawn at the end of the chapter.

2.1 3-Parameter model: n, I_{S0}, and V_{T0}

2.1.1 Description of the 3-parameter model

ACM and EKV models are inversion charge linearization-based models that describe, continuously, the MOS transistor drain current characteristic as a function of its source, drain, gate, and body voltages. The main differences between ACM and

EKV lie in different definitions for the normalization charge and the pinch-off voltage, V_P, [24], [28]. However, from a designer's point of view, the equation sets are similar, and the following work can be transposed from ACM to EKV formalism. In the coming discussion, voltages are referred to the body terminal, whose voltage, V_{BB}, is set to zero. However, the discussion remains valid for any V_{BB} value knowing that a unique set of parameters must be extracted for every specific value of V_{BB}.

The cornerstone of ACM and EKV model is that drain current is a function of the forward and reverse currents, I_F and I_R. In an ideal MOS, these currents are independent of each other and are a function of the gate (V_G), drain (V_D), and source voltages (V_S) as: $I_F = I(V_G, V_S)$ and $I_R = I(V_G, V_D)$. So, I_D can be expressed as [24]

$$I_D = I_F - I_R = I_{S0}\left(i_f - i_r\right), \tag{2-1}$$

where, $i_f = I_F/I_{S0}$, $i_r = I_R/I_{S0}$, and I_{S0} is the specific current, defined for the n-channel transistor as

$$I_{S0} = \mu_n C'_{ox} n \frac{U_T^2}{2} \frac{W}{L_{eff}}, \tag{2-2}$$

where, μ_n is the electron mobility, W and L_{eff} are the width and the effective length of the transistor, respectively, $U_T = kT/q$, is the thermal voltage, $C'_{ox} = \varepsilon_{ox}/t_{ox}$, is the oxide capacitance per unit area, and ε_{ox} and t_{ox} are the permittivity and equivalent thickness of the oxide, respectively.

i_f and i_r are the inversion coefficients that are directly related to the density of the normalized inversion charges at the source and the drain terminals of the transistor, q_S and q_D, respectively. These charges are derived from the source and drain charge densities, Q'_{IS} and Q'_{ID}, respectively, as

$$q_S = \frac{Q'_{IS}}{Q'_{IP}}, \tag{2-3}$$

$$q_D = \frac{Q'_{ID}}{Q'_{IP}}, \tag{2-4}$$

with, $Q'_{IP} = -nC'_{ox}U_T$ for the n-channel transistor.

Finally, q_S and q_D are related to the inversion coefficients as

$$q_S = \sqrt{1 + i_f} - 1\,, \tag{2-5}$$

$$q_D = \sqrt{1 + i_r} - 1\,. \tag{2-6}$$

Therefore, the normalized drain current can be also expressed as [22]

$$i_d = \frac{I_D}{I_{S0}} = (q_S - q_D)(q_S + q_D + 2)\,. \tag{2-7}$$

As described in the literature [22], [28], [30], [35], inversion regimes are usually defined as a function of i_d (or IC[1]). Indeed, weak inversion corresponds to $i_d < 0.1$, moderate inversion to $0.1 < i_d < 10$, and strong inversion to $i_d > 10$.

In long-channel devices, the use of inversion coefficients (i_f and i_r) is quite convenient since the latter can be easily related to the g_m transconductance, which is related to most of the circuit performances (gain, noise figure, input impedance, etc.). In a more general context, the use of normalized drain and source charges (q_D and q_S) is preferred since it allows a straightforward introduction of SCEs and simplifies the associated derivations (section 2.6).

The computation of the normalized charges is done as follows. The pinch-off voltage, V_P, is introduced as the channel to substrate voltage for which the channel charge density is equal to Q'_{IP}, or, $Q'_{IS} = Q'_{ID} = Q'_{IP}$. Then, the threshold voltage, V_T, is defined as the gate voltage for which $V_P = 0$ and is linearly approximated by [25]

$$V_P \approx \frac{V_G - V_T}{n}\,. \tag{2-8}$$

The pinch-off voltage is then related to the source and drain voltages, V_S and V_D, through their corresponding normalized charges as [22]

$$V_P - V_S = U_T(q_S - 1 + ln(q_S))\,, \tag{2-9}$$

$$V_P - V_D = U_T(q_D - 1 + ln(q_D))\,. \tag{2-10}$$

[1] Here, we made a distinction between i_d and IC (Inversion Coefficient) as IC is often referred to an approximation of i_d in the saturation region of operation [28], [35].

Therefore, the drain to source voltage, V_{DS}, normalized by U_T is given by

$$\frac{V_{DS}}{U_T} = q_S - q_D + ln\left(\frac{q_S}{q_D}\right). \tag{2-11}$$

2.1.2 Comparison of the 3-parameter model and DC measurements

To illustrate the accuracy of the model and the improvements given by the integration of the different parameters modeling SCEs, a comparison is done against the measurements for a 30 nm length and 1 µm width n-channel transistor of the 28 nm FD-SOI technology. All model parameters shown in the comparison were extracted following the procedure explained in section 3.1

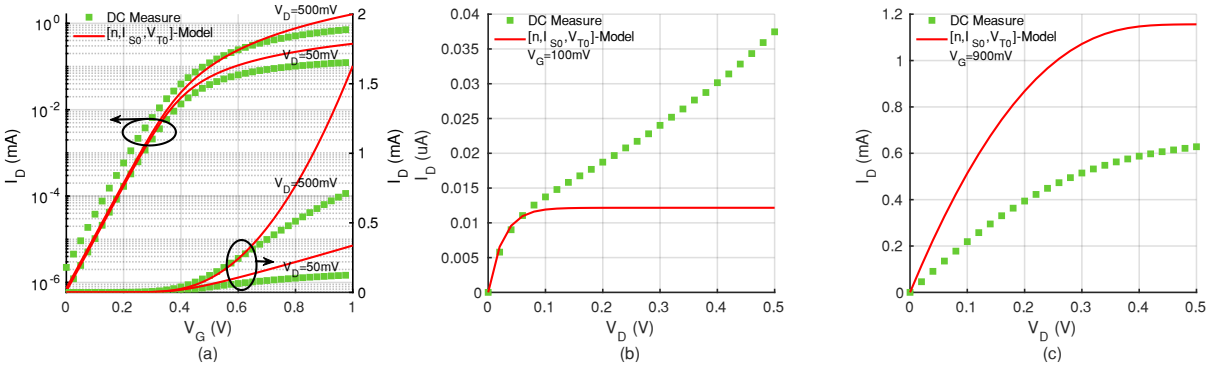


Figure 2-1. L=30 nm and W=1 µm N-MOS transistor characteristic curves: $I_D(V_G)$ for V_D=50 mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for V_G=100 mV (b) and for V_G=900 mV (c): Comparison between measures (green squares) and model based on 3 parameters (solid red line): n=1.377, I_{S0}=5.9 µA and V_T=380.3 mV.

Figure 2-1 shows a comparison between the 3-parameter model and some DC measurements. The two main characteristic curves $I_D(V_G)$ and $I_D(V_D)$ are presented.

As it can be noticed in the $I_D(V_G)$ characteristic (Figure 2-1(a)), the model has good accuracy in the weak and moderate inversion regimes of the transistor ($V_G < 600$ mV), but presents an overestimation of the drain current in the strong inversion regime also visible in Figure 2-1(c). This can be explained by two short-channel phenomena in strong inversion regime: the apparent reduction of the carrier mobility due to series resistances and the carrier velocity saturation. The first one mainly impacts the triode region ($V_D = 50\,mV$) and the second one, the saturated region of operation ($V_D = 500\,mV$).

Besides, the semilogarithmic scale of $I_D(V_G)$ (Figure 2-1(a)) brings to light two discrepancies with respect to the measured current in saturated region ($V_D = 500\,mV$) from weak to moderate regime ($V_G < 500\,mV$). The first one is a difference of the slope, n, and the second one is an underestimation of the drain current. The first discrepancy

can be minimized by slightly adjusting the slope factor, n, to optimize the fit with the measurements [35], noticing that the variation of n with respect to V_D is small enough to be neglected.

On the contrary, the current increase with V_D has to be modeled by taking into account two major short-channel effects: the DIBL and the CLM. In the absence of these two effects, the 3-parameter model cannot correctly reproduce the $I_D(V_D)$ behavior. As shown in Figure 2-1, the current is underestimated in weak inversion while in saturated region it remains constant with V_D.

In the following subsections, we address the introduction of each of the four above-mentioned physical effects into the transistor model. The discussion starts with the carrier mobility reduction, which has a major impact in linear region in strong inversion regime and continues with the V_D dependence in saturated region operation.

2.2 Modeling the carrier mobility reduction and series resistances effects: θ

2.2.1 Carrier mobility reduction effect

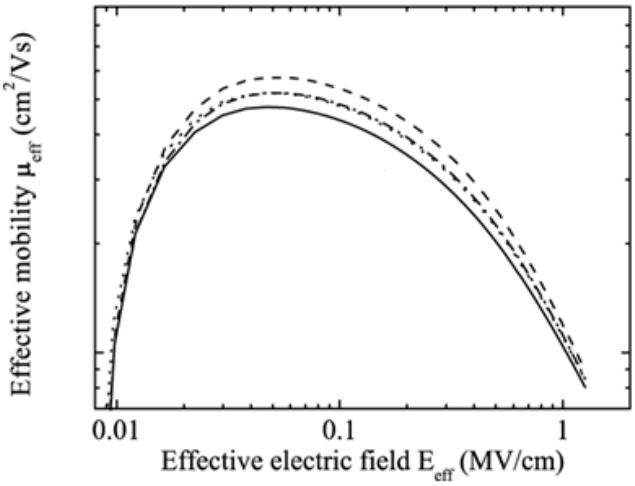


Figure 2-2. Impact of the effective electric field on the effective mobility.

The effective mobility of the carriers in the inversion layer of the MOS transistor depends on several scattering mechanisms causing a complex dependence of the mobility on the transversal and the longitudinal components of the electric field [23], [37]. The first one, related to carrier mobility reduction, is modeled here by θ, and the second one by ζ, related to the carrier velocity saturation, is described in section 2.4 .

As illustrated in Figure 2-2, when a high vertical (or transversal) electric field is applied in the transistor channel, the mobility in the inversion layer near the semiconductor-oxide interface is reduced. This reduction, that leads to an effective

carrier mobility, is mainly due to three mechanisms: Coulomb scattering, photon scattering, and surface roughness scattering [23]. The carrier mobility reduction will cause a decrease of the drain current, especially in strong inversion regime and in linear region.

2.2.2 Series resistances effect

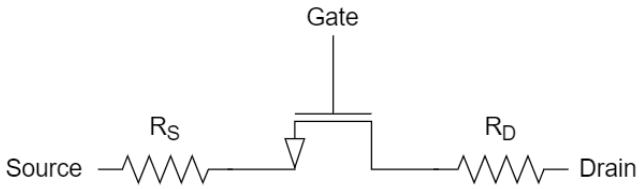


Figure 2-3. Drain and source series resistances.

The source and drain series resistances cannot be overlooked in short-channel devices. For short-channel transistors, the voltage drop in the source and drain regions becomes important in strong inversion and especially in linear region, where the channel resistance is minimal. In practice, provided that the voltage drops in source and drain regions are small compared to the applied voltages, the series resistances effect can be modeled by just adding an extra contribution to the θ parameter. As result, the presence of source and drain series resistances can be described as a further reduction of the apparent carrier mobility [23].

2.2.3 Model of carrier mobility reduction and series resistances effects

As explained above, both effects, the carrier mobility reduction and the drain and source series resistances, can be introduced in the drain current expression through a parameter related to the carrier mobility reduction, θ, and the average inversion charge, $(q_S + q_D)/2$, which represents the vertical field dependence. Hence (2-7) is modified as

$$I_D = I_{S0}\frac{(q_S - q_D)(q_S + q_D + 2)}{1 + \theta\left(\frac{q_S + q_D}{2}\right)}. \qquad (2\text{-}12)$$

2.2.4 Comparison of the 4-parameter model and DC measurements

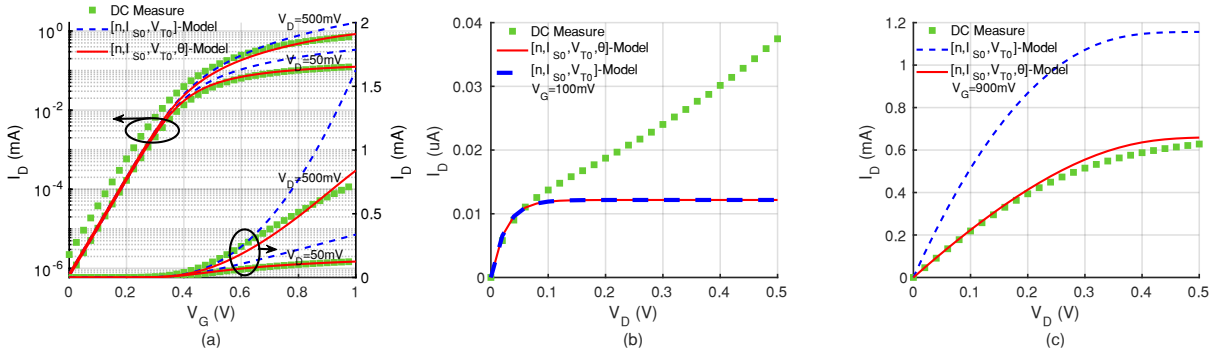


Figure 2-4. L=30 nm and W=1 µm N-MOS transistor characteristic curves: $I_D(V_G)$ for V_D=50 mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for V_G=100 mV (b) and for V_G=900 mV (c): Comparison between measures (green squares) model based on 3 parameters (dashed blue line) and on 4 parameters (red solid line): n=1.377, I_{S0}=5.9 µA, V_T=380.3 mV and θ=0.115. Note that for (b) there is no change between models based on 3 and 4 parameters, as the effect of mobility reduction (θ) appears only in strong inversion.

In Figure 2-4(a), the impact of carrier mobility reduction is visible. Compared with the 3-parameter (n, I_{S0} and V_{T0}) model presented previously, the fitting with the measurements is better in strong inversion without degrading the behavior at weak and moderate inversion levels in triode region ($V_D = 50\,mV$), proving that a 4-parameter (n, I_{S0}, V_{T0} and θ) model could be enough to describe the $I_D(V_G)$ behavior for a single V_D. For $V_D = 500\,mV$, the model also improves the estimation of the current in strong inversion, even if the latter is still overestimated.

On the other hand, the underestimation of the drain current in weak inversion as the drain voltage increases (Figure 2-4(a) for $V_G < 500\,mV$ and Figure 2-4(b)) remains, due to the DIBL effect, as explained in the next section.

Figure 2-4(b) clearly shows that the carrier mobility reduction (θ) does not have any effect on the current in weak inversion regime. Contrary to this, Figure 2-4(c) depicts the importance of including this effect in the modeling of the strong inversion regime. Unlike other design-oriented analytical models previously proposed [30], [31], the inclusion of θ parameter allows to fully model all inversion regimes of operation of the MOS transistor for a given V_D. As it will be shown later, the V_D dependence will be further improved thanks to the introduction of additional parameters.

2.3 Modeling the drain-induced barrier lowering effect: σ

2.3.1 Drain-induced barrier lowering effect

The formation of the conduction channel in long-channel transistors depends mainly on the gate voltage which controls the electric field between the gate and the

substrate terminals. However, as the channel length decreases, a drop of the potential barrier at the source side occurs when the drain voltage increases (Figure 2-5). This phenomenon, known as the Drain-Induced Barrier Lowering (DIBL), allows the creation of a conduction channel at a lower gate voltage, which can be interpreted as a reduction of the threshold voltage, V_T [37].

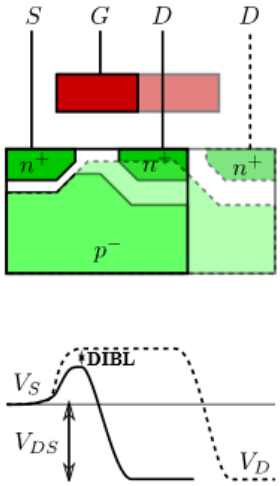


Figure 2-5. Reduction of the potential barrier for short-channel transistors when applying a V_{DS} voltage [38].

Introducing the DIBL parameter, σ, this effect is modeled by adding a $\sigma(V_D + V_S)$ term in the V_T expression as [24]

$$V_T = V_{T0} - \sigma(V_D + V_S)\,. \tag{2-13}$$

As a consequence, the pinch-off voltage increases and can be expressed from (2-8) as

$$V_P \approx \frac{V_G - V_{T0} + \sigma(V_D + V_S)}{n}\,. \tag{2-14}$$

2.3.2 Comparison of the 5-parameter model and DC measurements

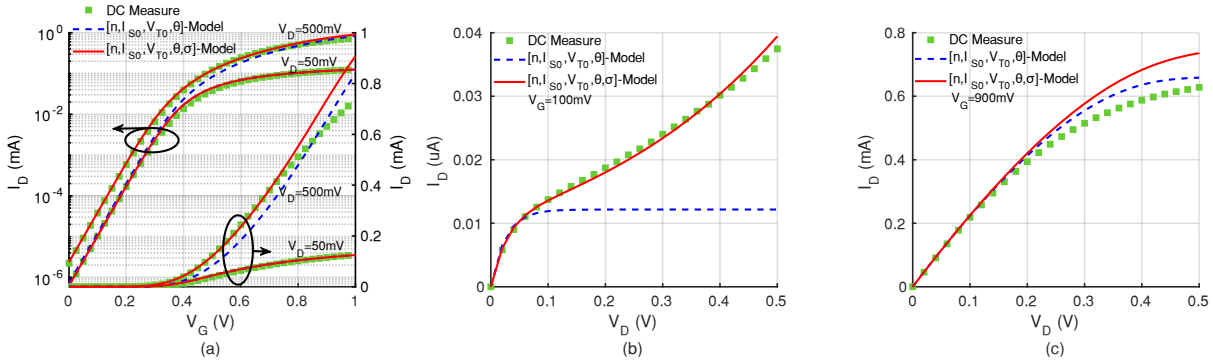


Figure 2-6. L=30 nm and W=1 µm N-MOS transistor characteristic curves: $I_D(V_G)$ for V_D=50 mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for V_G=100 mV (b) and for V_G=900 mV (c): Comparison between measures (green squares) model based on 4 parameters (dashed blue line) and on 5 parameters (red solid line): n=1.377, I_{S0}=5.9 µA, V_{T0}=384.9 mV, θ=0.115 and σ=0.093

Figure 2-6(a), and (b) show is the importance of DIBL effect to correctly model the drain current in weak and moderate inversion regimes, introducing a dependence on V_D which was not accounted for in previous analytical models. The remaining drain current overestimation by the model, mainly in strong inversion regime as shown in Figure 2-6(c), is related to carrier velocity saturation effect which will be treated in the next section.

2.4 Modeling the carrier velocity saturation effect: ζ

2.4.1 Carrier velocity saturation effect

When the longitudinal electric field (V_{DS}/L) is low enough, as in long-channel transistors for instance, the carrier velocity is proportional to it. Nevertheless, for short-channel devices, the longitudinal electric field is higher and when it increases, the carrier velocity may reach a limit and saturate, leading to a reduced saturation current compared to that of a long-channel device (Figure 2-7). This effect is known as carrier velocity saturation [37].

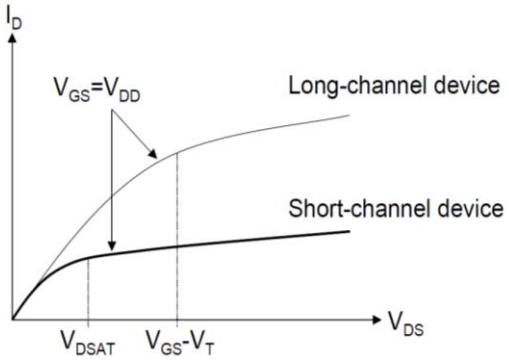


Figure 2-7 Comparison of the drain current saturation for short and long-channel devices [39].

The carrier velocity saturation effect has already been widely considered in the literature [28], [33]–[35]. In those published models, the carrier velocity saturation parameter is represented by ζ, which is defined as

$$\zeta = \frac{\mu_n U_T}{L v_{sat}}, \tag{2-15}$$

where, v_{sat} is the saturation velocity of the carriers. To be more accurate, μ_n in (2-15) should be replaced by the effective mobility that includes the effects of the vertical electric field and series resistances presented in section 2.2.2 . Keeping here μ_n for simplicity purpose will lead to an effective value of ζ.

When the carrier velocity saturation is reached, the drain current is given by [23]

$$I_{Dsat} = -W v_{sat} Q'_{IDsat} . \tag{2-16}$$

Or, using the normalized quantities,

$$i_{dsat} = \frac{I_{Dsat}}{I_{S0}} = \frac{2}{\zeta} q_{Dsat} . \tag{2-17}$$

Then, the approximation introduced in [40], considering that the saturation of carrier velocity only occurs at the drain side is made. This assumption simplifies the model equations at the cost of a lower accuracy in the transition from linear to saturated region. With these considerations, the general expression of the drain current (2-12) can still be used to extract q_{Dsat} value, replacing q_D by q_{Dsat},

$$i_{dsat} = \frac{2}{\zeta} q_{Dsat} = \frac{(q_S + q_{Dsat} + 2)(q_S - q_{Dsat})}{1 + \theta\left(\frac{q_S + q_{Dsat}}{2}\right)}. \tag{2-18}$$

Doing so, we obtain the following relation between q_S and q_{Dsat}:

$$q_S = \frac{\theta}{2\zeta} q_{Dsat} - 1 + \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)}. \tag{2-19}$$

Defining V_{DSsat} as the drain-to-source voltage for which $q_D = q_{Dsat}$, and using (2-11), one obtains [23]

$$\frac{V_{DSsat}}{U_T} = q_S - q_{Dsat} + ln\left(\frac{q_S}{q_{Dsat}}\right). \tag{2-20}$$

In order to preserve the continuity of the model from linear to saturated region, we can define an effective drain-to-source voltage accounting for the carrier velocity saturation effect,

$$V'_{DS} = \frac{V_{DS}}{\sqrt[4]{1 + \left(\frac{V_{DS}}{V_{DSsat}}\right)^4}}. \tag{2-21}$$

This formulation, inspired from industry-standard compact models, ensures a smooth behavior of the model around $V_{DS} = V_{DSsat}$.

Similarly, one can define an effective drain voltage,

$$V'_D = V'_{DS} + V_S\,, \tag{2-22}$$

and its associated drain charge q'_D, using (2-10),

$$V_P - V'_D = U_T(q'_D - 1 + ln(q'_D))\,. \tag{2-23}$$

Finally, the drain current expression of (2-12), becomes

$$I_D = I_{S0}\frac{(q_S + q'_D + 2)(q_S - q'_D)}{1 + \theta\left(\frac{q_S + q'_D}{2}\right)}. \tag{2-24}$$

2.4.2 Comparison of the 6-parameter model and DC measurements

Figure 2-8 illustrates the benefits of introducing the carrier velocity saturation effect in the model through the sixth parameter, ζ, especially in strong inversion regime for a transistor in saturated region (Figure 2-8(a) for $V_D = 500\,mV$ and Figure 2-8(c)). As expected, ζ parameter has no impact in linear regime (Figure 2-8(a) for $V_D = 50\,mV$).

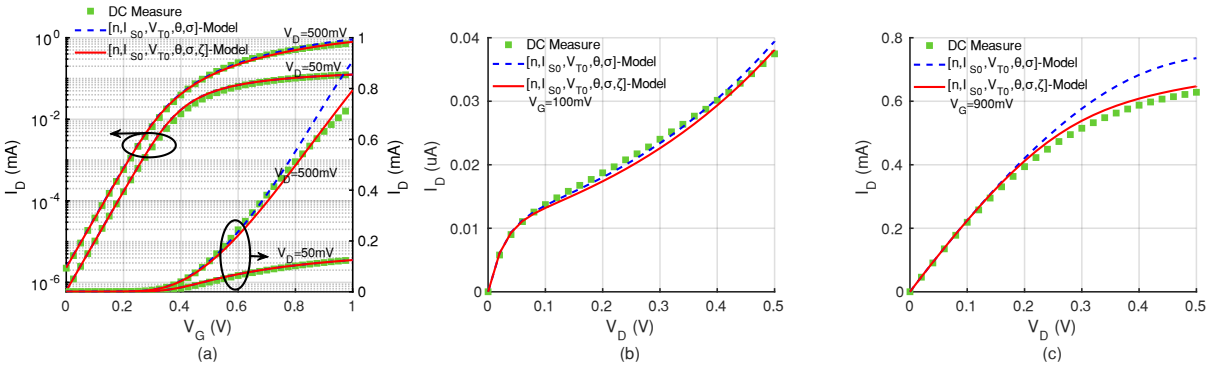


Figure 2-8. L=30 nm and W=1 µm N-MOS transistor characteristic curves: $I_D(V_G)$ for V_D=50 mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for V_G=100 mV (b) and for V_G=900 mV (c): Comparison between measures (green squares) model based on 5 parameters (dashed blue line) and on 6 parameters (red solid line): n=1.377, I_{S0}=5.9 µA, V_{T0}=384.9 mV, θ=0.115, σ=0.093 and ζ=0.035.

2.5 Modeling the channel length modulation: V_E

2.5.1 Channel Length Modulation effect

The CLM effect occurs when the drain voltage increases after the pinch-off occurrence, creating a depletion region at the drain side which extends towards the source, and thus a reduction of the effective length of the channel by a quantity ΔL, which, in turns, increases the current as V_D increases [37]. Considering this phenomenon in the presented analytical model will add a third effect directly linked to the dependency of the drain current on V_D.

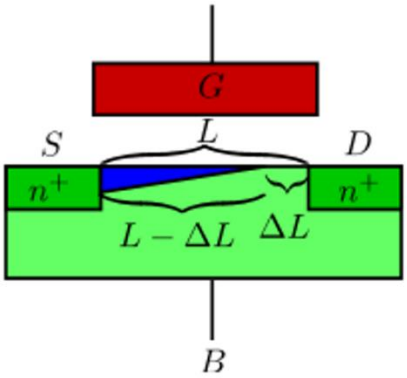


Figure 2-9. Channel length modulation effect [38].

Taking advantage of the expression of ΔL as a function of V_D, CLM can be accounted for by simply introducing a seventh parameter, V_E, leading to the following drain current expression:

$$I_D = \left(1 + \frac{V_{DS} - V'_{DS}}{V_E}\right) \frac{I_{S0}(q_S + q'_D + 2)(q_S - q'_D)}{1 + \frac{\theta}{2}(q_S + q'_D)}. \qquad (2\text{-}25)$$

2.5.2 Comparison of the 7-parameter model and DC measurements

Figure 2-10 illustrates the effect of adding CLM modeling on a 30nm length transistor. As observed in the figure, the difference compared to the 6-parameter model is weak since for this channel length, the DIBL effect is strong and overshadows the CLM one. Hence, it is worth noticing here, that for short-channel devices, the 6-parameter model may be enough to capture the main characteristics of the electrical behavior of such devices.

For this reason, a further comparison for an N-MOS transistor with $L = 150\ nm$ and $W = 1\ \mu m$ is presented in Figure 2-11, where the V_E effect is clearly visible on the output characteristic of this longer transistor, especially in the saturation region (Figure 2-11(b), and (c)).

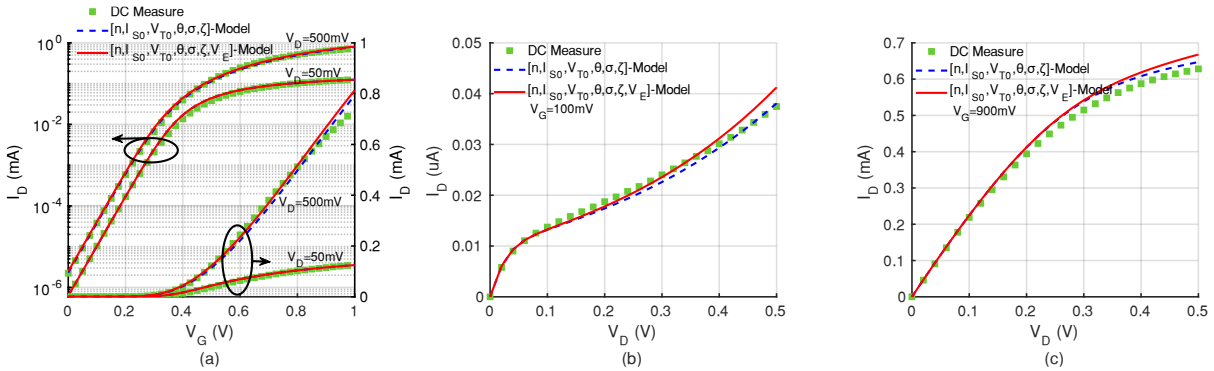


Figure 2-10. L=30 nm and W=1 µm N-MOS transistor characteristic curves: $I_D(V_G)$ for V_D=50 mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for V_G=100 mV (b) and for V_G=900 mV (c): Comparison between measures (green squares) model based on 6 parameters (dashed blue line) and on 7 parameters (red solid line): n=1.377, I_{S0}=5.9 µA, V_{T0}=384.9 mV, θ=0.115, σ=0.093, ζ=0.035 and V_E=5 V.

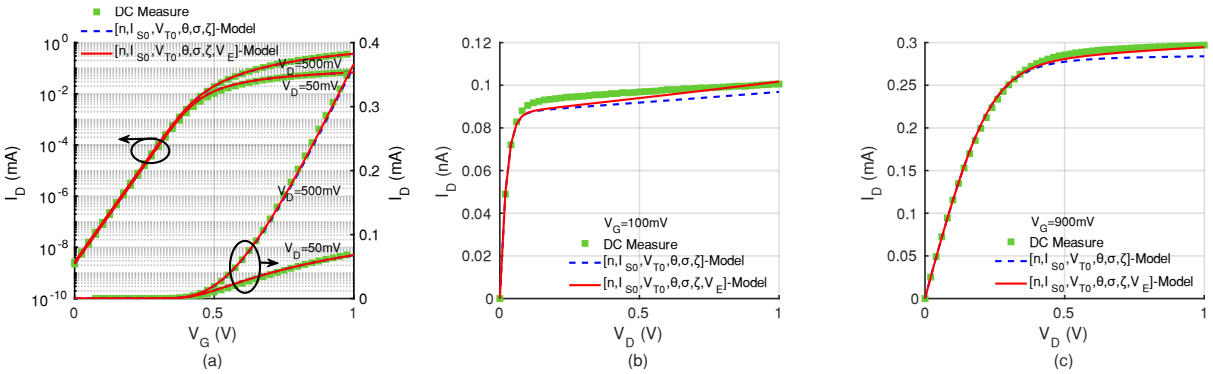


Figure 2-11. L=150 nm and W=1 µm N-MOS transistor characteristic curves: $I_D(V_G)$ for V_D=50 mV and 500 mV in linear (right axis) and in semilogarithmic scale (left axis) (a), $I_D(V_D)$ for V_G=100 mV (b) and for V_G=900 mV (c): Comparison between measures (green squares) model based on 6 parameters (dashed blue line) and on 7 parameters (red solid line): n=1.092, I_{S0}=1.83 µA, V_{T0}=427 mV, θ=0.047, σ=0.003, ζ=0.06 and V_E=18.5 V.

Thanks to the four parameters added to the original model, the 7-parameter model is now able to simulate the drain current of transistors of any length, from weak to strong inversion regime in both linear and saturated regions. Also, this wide coverage in terms of V_G and V_D values makes the model suitable for describing any derivative of the drain current, as it will be shown in next section.

2.6 Small-signal modeling of drain current

On top of an accurate description of the MOS DC behavior (I-V characteristics), a design-oriented model should provide analytical formulas for the transconductance, the output conductance and the drain current high order derivatives in general. This is the first step to enable analog/RF designers to develop analytical design methodologies for transistors sizing. Furthermore, since the model allows to derive the analytical expressions of successive order current derivatives, especially versus V_D, it also allows to study nonlinear effects that impact the performance of many analog/RF designs exhibiting large V_D swings.

In this section, we will compare the modeled transconductances with actual measurements for a FD-SOI transistor of $L = 30\,nm$ to demonstrate the wide validity domain of the proposed model. Furthermore, analytical expressions of the transconductance and its derivatives will be proposed. Since the region of operation of the MOS transistors is often defined at the beginning of the design process, this information can be used to provide simplified analytical expressions of the current derivatives by considering the linear and saturated regions separately. These expressions are developed in the following subsections.

2.6.1 Analytical expressions of the current derivatives in absence of carrier velocity saturation

In advanced technologies, where transistors frequency limitations are relaxed thanks to large f_T, weak and moderate inversion are often selected for RF design, in order to increase the energy efficiency. In this particular biasing conditions, carrier velocity saturation can be neglected (see chapter 2.5.2), allowing the use of (2-12) to obtain analytical expressions of the current derivatives, valid for any transistor geometry as,

$$\frac{\partial i_d}{\partial v_x} = \frac{1}{B}\left[\left(2 + 2q_S - \frac{\theta}{2} i_d\right)\frac{\partial q_S}{\partial v_x} - \left(2 + 2q_D + \frac{\theta}{2} i_d\right)\frac{\partial q_D}{\partial v_x}\right], \tag{2-26}$$

with v_x standing for the considered normalized voltage, $v_g = V_G/U_T$, $v_d = V_D/U_T$, or $v_s = V_S/U_T$ and

$$B = 1 + \frac{\theta}{2}(q_S + q_D), \tag{2-27}$$

and from equations (2-9), (2-10)and (2-14),

$$\frac{\partial q_{S(D)}}{\partial v_g} = \frac{1}{n}\frac{q_{S(D)}}{q_{S(D)} + 1}, \tag{2-28}$$

$$\frac{\partial q_D}{\partial v_d} = \left(1 - \frac{\sigma}{n}\right)\frac{q_D}{q_D + 1}, \tag{2-29}$$

$$\frac{\partial q_S}{\partial v_d} = \frac{\sigma}{n}\frac{q_S}{q_S + 1}, \tag{2-30}$$

$$\frac{\partial q_D}{\partial v_s} = \frac{\sigma}{n}\frac{q_D}{q_D + 1}, \tag{2-31}$$

$$\frac{\partial q_S}{\partial v_s} = \left(1 - \frac{\sigma}{n}\right)\frac{q_S}{q_S + 1}. \tag{2-32}$$

Equations (2-26), (2-27), and (2-28) give an explicit analytical expression of the gate transconductance,

$$g_m = \frac{\partial i_d}{\partial v_g} = \frac{2}{nB}\left[q_S - q_D - i_d\frac{\theta}{4}\left(\frac{q_S}{1 + q_S} + \frac{q_D}{1 + q_D}\right)\right]. \tag{2-33}$$

Going further, the second and third order current derivatives (g_{m2}, g_{m3}) can be expressed under the same assumption used for estimating the transconductance, as follows,

$$g_{m2} = \frac{\partial^2 i_d}{\partial v_g^2} = \frac{2}{n^2 B}\left[\frac{q_S}{1+q_S} - \frac{q_D}{1+q_D} - \frac{\theta}{4}\left[2n g_m\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + i_d\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right)\right]\right], \tag{2-34}$$

$$g_{m3} = \frac{\partial^3 i_d}{\partial v_g^3} = \frac{2}{n^3 B}\left[\frac{q_S}{(1+q_S)^3} - \frac{q_D}{(1+q_D)^3} - \frac{\theta}{4}\left[3n^2 g_{m2}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + 3n g_m\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right) + i_d\left(\frac{q_S(1-2q_S)}{(1+q_S)^5} + \frac{q_D(1-2q_D)}{(1+q_D)^5}\right)\right]\right]. \tag{2-35}$$

Moreover, thanks to the integration of a direct dependence of the current on the drain voltage in the model, it is now possible to estimate the drain conductance, g_d, resulting in the following equation,

$$g_d = \frac{\partial i_d}{\partial v_d} = \frac{2}{B}\left[\frac{\sigma}{n} q_S - \left(\frac{\sigma}{n} - 1\right) q_D - i_d \frac{\theta}{4}\left(\frac{\sigma}{n}\frac{q_S}{1+q_S} + \left(\frac{\sigma}{n} - 1\right)\frac{q_D}{1+q_D}\right)\right]. \tag{2-36}$$

2.6.2 Analytical expressions of the current derivatives in saturated region

Similarly, simple generic analytical expressions can be drawn for the derivatives of the current in the saturated region, using the saturation expression of the drain current I_{Dsat} in (2-18). These expressions include the effects of carrier velocity saturation, mobility reduction and DIBL. Using (2-18), the transconductances and conductance can be expressed as,

$$\frac{\partial i_{dsat}}{\partial v_x} = \frac{\partial i_{dsat}}{\partial q_S}\frac{\partial q_S}{\partial v_x} = 2\frac{E}{D + \frac{\theta}{2}E}\frac{\partial q_S}{\partial v_x}. \tag{2-37}$$

Using the same naming convention for the transistor terminals as before and with

$$D = 1 + \zeta - \frac{\theta}{2} + q_{Dsat}\left(\zeta + \theta + \frac{\theta^2}{2\zeta}\right), \tag{2-38}$$

$$E = \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)}, \tag{2-39}$$

$\partial q_S/\partial v_x$ is given by (2-28), (2-30), or (2-32) depending on the considered terminal.

Specifically, the approximated expression in saturation of the transconductance, g_m, is given by

$$g_{m\_sat} = \frac{\partial i_{dsat}}{\partial v_g} = \frac{2}{n}\frac{Eq_S}{\left(D + \frac{\theta}{2}E\right)(q_S + 1)}, \tag{2-40}$$

and, for conductance, g_d, by

$$g_{d\_sat} = \frac{\partial i_{dsat}}{\partial v_d} = \frac{2\sigma}{n}\frac{Eq_S}{\left(D + \frac{\theta}{2}E\right)(q_S + 1)}. \tag{2-41}$$

2.6.3 Numerical approach of the current derivatives

Gate transconductance, g_m, and transconductance efficiency, g_m/I_D, are key parameters for the small-signal approach of the design [10], [13], [41]. At the same time, the second and third derivatives of I_D, namely g_{m2} and g_{m3}, determine circuit linearity performances, such as harmonic distortion, intermodulation products and compression point and thus must be accurately modeled.

A numerical approach of the derivatives can be done with the design-oriented 7-parameter model. Numerical derivatives will be compared against both analytical approximations and the correspondent DC measurement in the following subsection.

2.6.4 Comparison of the derivatives from different approaches and DC measurements

The main objective of this section is to compare the different approaches proposed previously for the current derivatives and the g_m/I_D characteristic against

the DC measurements (green squares in the comparative figures) for a n-MOS transistor of $W = 1\ \mu m$ and $L = 30\ nm$.

Figure 2-12 presents the comparison of the transconductance g_m with respect to the normalized current, i_d, for several values of V_D, $50\ mV$ (a), $250\ mV$ (b) and $500\ mV$ (c). It can be observed that, the numerical derivation of the model (red solid curve) estimates very well the behavior of the transconductance with a good accuracy in all operation regions, especially for values of i_d below 40.

On the other hand, (2-33) representing the derivative without the carrier velocity saturation (dashed blue lines), allows to predict the existence of a maximum of g_m for a given value of i_d, contrary to what occurs with the approximation for saturation region (dot-dashed violet curves in Figure 2-12(b) and (c)), given by (2-37). The first expression is very accurate for all inversion regimes in linear region (Figure 2-12(a)), but is limited in saturation region as shown in Figure 2-12(b) and (c), even if it still provides a good estimation in weak and moderate inversion regimes.

The approximation in (2-40) is in good agreement with the measurements and the numerical derivative in the saturated region ($V_D = 500\ mV$) up to a large inversion level ($i_d = 50$). However, since the computation is only valid when the transistor is in deep saturated region, the results are less accurate for all the other biasing conditions.

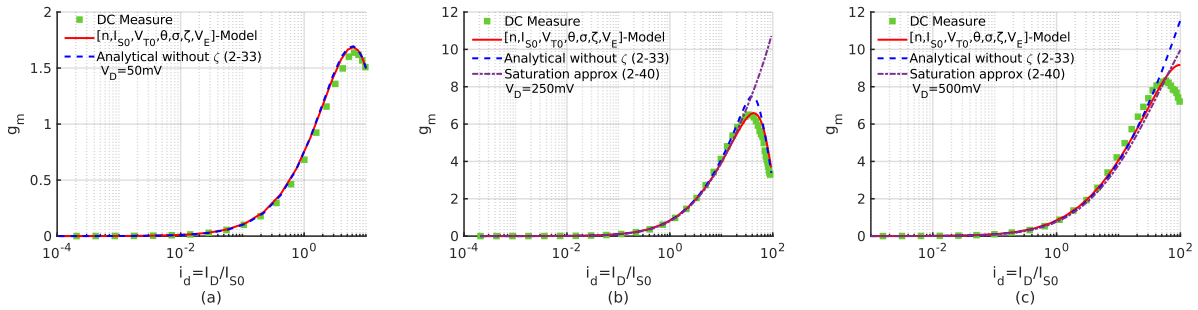


Figure 2-12. L=30 nm and W=1 µm N-MOS transistor g_m (i_d) curve for V_D=50mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares), numerical derivative based on 7 parameters model (red solid line), analytical expression without carrier velocity saturation (dashed blue line) and analytical expression based on saturation approximation (dot-dashed violet line).

Figure 2-13 and Figure 2-14 represent the analytical expressions of g_{m2} and g_{m3} in (2-34) and (2-35), respectively, as a function of i_d. There is a good agreement with both measurements and numerical derivations of the complete model. As g_{m2} and g_{m3} are used to estimate non-linearities of analog/RF circuits, the proposed model provides accurate results (using numerical derivatives) in all regions and inversion regimes. Also, the rather simple g_{m2} and g_{m3} analytical expressions can be used in analytical design methodologies to get an estimate of the circuit behavior.

It is worth noticing that these curves allow an accurate estimation of the sweet spot of device linearity (the value of i_d that makes $g_{m3} = 0$). This estimation is not possible with simpler models [30], [31] that do not count for short-channel effects and related bias dependences. The maximum and minimum of these derivatives are also in good agreement with the measurements.

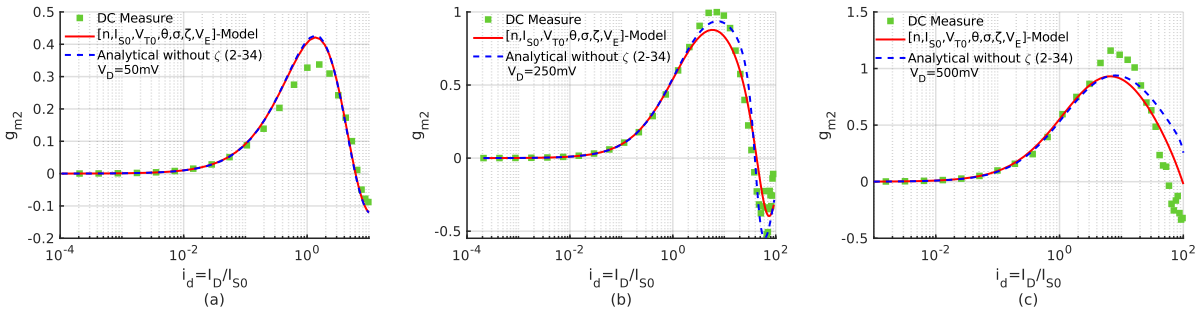


Figure 2-13. L=30nm and W=1 µm N-MOS transistor g_{m2} (i_d) curve for V_D=50 mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares), numerical derivative based on 7 parameters model (red solid line) and analytical expression without carrier velocity saturation (dashed blue line).

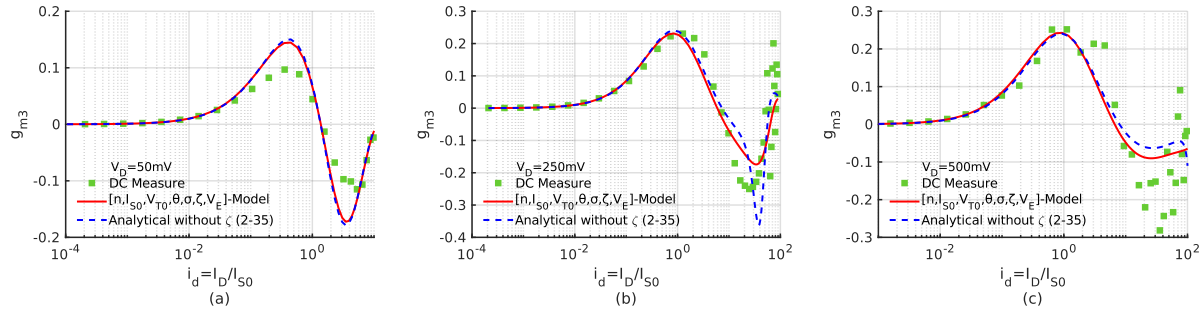


Figure 2-14. L=30nm and W=1 µm N-MOS transistor g_{m3} (i_d) curve for V_D=50 mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares) and numerical derivative based on 7 parameters model (red solid line) and analytical expression without carrier velocity saturation (dashed blue line).

Figure 2-15 illustrates the transconductance efficiency g_m/I_D, for DC measurements (green squares) and the numerical derivation of the characteristic (red solid line). A good consistency between the curves is observed, with only a slight overestimation (lower than 10%) in moderate inversion regime in linear region ($V_D = 50\ mV$).

Finally, Figure 2-16 shows the conductance, g_d, versus the drain voltage, V_D, for several values of V_G. As observed, the analytical approximation without carrier velocity saturation effect (dashed blue line) results to be more accurate for linear region and for not so high values of gate voltage. Moreover, it can be noticed how the saturation approximation (dot-dashed violet line) results in a line that coincides in saturation with the previous analytical approximation.

The proposed model proves to be sufficiently useful to estimate the drain current derivatives through the different approximations demonstrated here depending on the transistor operating region, this is very useful for further implementation within an analytical design methodology. The modeling of the transistor for high frequency response will be discussed next, as this is also fundamental to develop a complete circuit design methodology for RF applications.

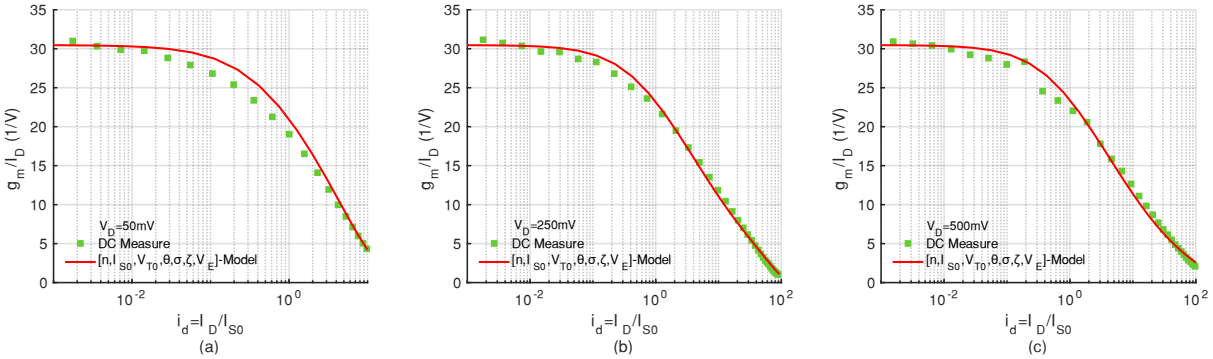


Figure 2-15. L=30nm and W=1 µm N-MOS transistor g_m/I_D (i_d) curve for V_D=50 mV (a), 250 mV (b) and 500 mV (c): Comparison between measures (green squares) and numerical derivative based on 7 parameters model (red solid line).

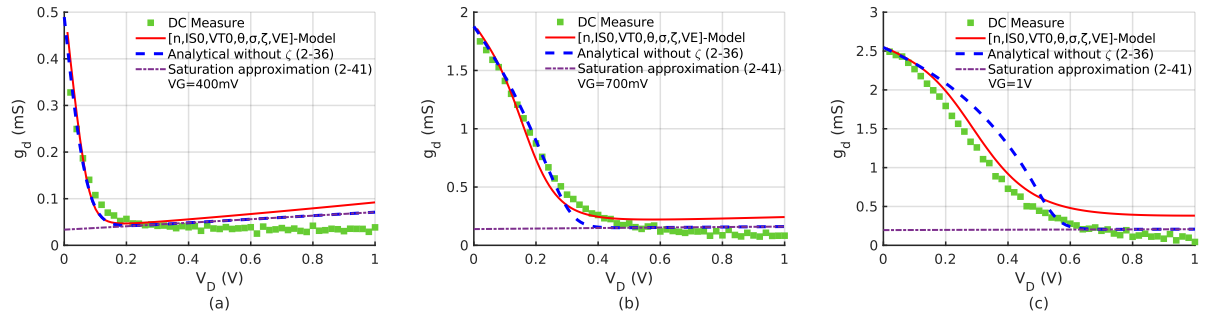


Figure 2-16. L=30 nm and W=1 µm N-MOS transistor g_d (V_D) curve for V_G=400mV (a), 700 mV (b) and 1 V (c): Comparison between measures (green squares), numerical derivative based on 7 parameters model (red solid line), analytical expression without carrier velocity saturation (dashed blue line) and analytical expression based on saturation approximation (dot-dashed violet line).

2.7 Discussion on RF modeling

To enable analog and RF circuit design, a complete model must consider not only the DC current flowing in the device and its derivatives, but also the other elements that participate to the frequency response of the transistor when integrated into a circuit. These elements consist in the intrinsic capacitances of the device, linked to its intrinsic charges, as well as extrinsic capacitances that exist between the device terminals due to the presence of polysilicon gate, contacts and metal lines. Then, parasitic resistances must be considered to capture the right dynamic response of the transistor, especially at high frequencies. The resistance on the gate terminal is one of

the most important, especially when the transistor is used as an amplifier. All these considerations are well known and extensively described in the literature.

Concerning the intrinsic capacitances, which are some of the most difficult elements to describe, a first proposition of modeling relying on the 3-parameter approach described in section 2.1 is presented in [23] for ACM and in [27] for EKV, where the main 5 capacitances on the transistor are considered, as illustrated in Figure 2-17.

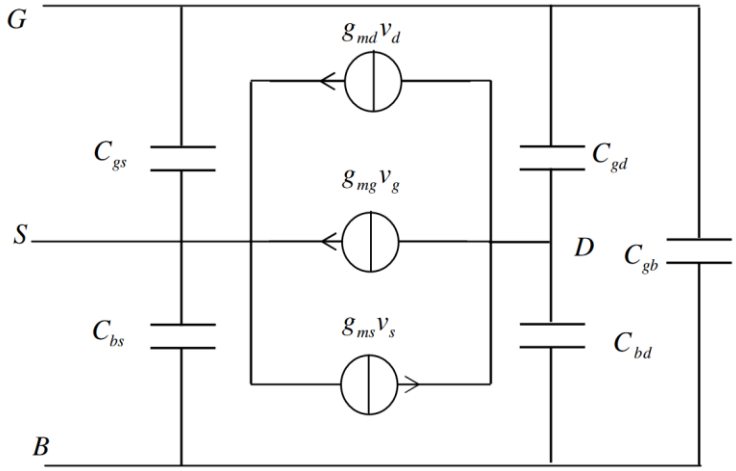


Figure 2-17. Simple 5-capacitance small signal equivalent circuit for MOS modeling in ACM [23].

Some refinements of the intrinsic capacitance model are also proposed, which include the integration of the carrier velocity saturation effect [23], and the DIBL effect [42].

Finally, a complete RF model will need the integration of noise sources, considering both the intrinsic noise due to the channel and the noise due to parasitic resistances. Doing so, such a model can be efficiently used for RF design [13], [14], [43].

2.8 Conclusion

In this chapter a design oriented 7-parameter model has been proposed, that includes all the main effects needed to capture the DC behavior of the MOS transistor in advanced technologies. Its accuracy has been proven by comparing the simulated characteristics to DC measurements for a 30 nm transistor in STMicroelectronics 28nm FD-SOI technology.

One of the most interesting aspects of the model is that each of its parameters is directly related to a physical effect on the transistor. This allows a simplification of the model depending on the operating regime of the transistor by neglecting some of the effects that do not have a major impact on the given regime. Moreover, the physical

nature of the model parameters opens the way to link the technology features and the device performance.

Since the proposed model is analytical, explicit expressions of the derivatives of the drain current have been determined, including the transconductances, conductance, and also the higher order derivatives, which enables nonlinear behavior studies. Finally, some simplified expressions have been proposed, depending on the considered operation regime.

While the proposed model offers a really good accuracy in all operation regions and inversion regimes of the MOS transistor DC behavior, extensions towards a complete analytical RF model have been discussed, starting with a description of the MOS intrinsic capacitances. Once completed, such a model can be integrated in a circuit design methodology for low-power analog and RF applications, without neglecting the fact that it is necessary to study also the MOS behavior under the variation of the temperature or the possibility of use the body biasing feature of this technology, that are not addressed in this work.

Chapter 3: Parameter Extraction and Consistency of the Proposed Model

Providing a simple and accurate parameter extraction methodology is essential to implement the proposed MOS transistor model in any compatible technology, and thus facilitate its adoption by the design community. There are different existing proposals in the literature [44]–[49] for parameter extraction, especially for the 3 parameters-based model. In this thesis, we will focus on a methodology based on a common source configuration, that is presented in this chapter.

The theoretical basis behind the extraction of each model parameter is firstly presented and then, to illustrate the process, each parameter is extracted and optimized, using the I-V characteristics obtained from the PDK simulations of a 28nm FD-SOI technology, for a 30 nm length transistor. To show the consistency and accuracy of the model, a comparison is made among different channel transistor lengths, 30 nm, 60 nm and 150 nm, allowing to carry out a validation of the model for both short and long-channel transistors and to study the short-channel effects on the technology node. The relative error on the simulations using the extracted model is also evaluated in this chapter for different transistor lengths, and a comparative discussion about other design-oriented models concludes the chapter.

3.1 Parameter extraction

A brief description of the extraction of each model parameter is given below. The procedure can be applied using simulation or measurements results. Here, it will be illustrated with electrical simulations of an n-channel low threshold voltage (“lvt”) transistor of $L = 30\,nm$ and $W = 1\,\mu m$ using the models from STMicroelectronics 28 nm FD-SOI technology PDK.

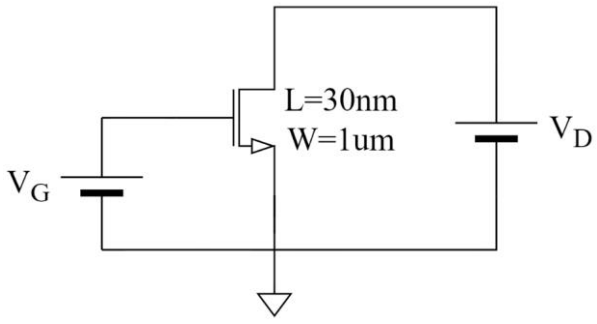


Figure 3-1. Common source configuration circuit for parameter extraction.

Most of the parameters can be directly extracted from a common source configuration as illustrated in Figure 3-1, sweeping V_G with a fixed V_D value.

In the following subsections, we will first describe the g_m/I_D extraction procedure, originally presented in [48], that is applied to extract the 3 main physical parameters, n, I_{S0} and V_{T0}.

3.1.1 Subthreshold slope factor

The subthreshold slope factor, n, is determined by calculating the slope of the semilogarithmic $I_D(V_G)$ curve, for small values of V_G, in linear region as

$$n = \frac{1}{U_T}\frac{\Delta V_G}{\Delta \ln\,(I_D)}. \tag{3-1}$$

In practice, n can be easily calculated from the $I_D(V_G)$ curve. In linear region (small V_D), two points of the $I_D(V_G)$ curve are taken in weak inversion regime (small V_G values), denoted as (V_{G1}, I_{D1}) and (V_{G2}, I_{D2}). Then, the difference between the two V_G values is taken, $\Delta V_G = V_{G2} - V_{G1}$, as well as the difference between the natural logarithm of the two drain current values, $\Delta \ln(I_D) = \ln(I_{D2}) - \ln(I_{D1})$. The ratio between these two differences normalized respect to the thermal voltage, U_T, gives an approximation of the slope factor, n.

To illustrate the procedure, the $I_D(V_G)$ curve simulated for the 30 nm transistor at $V_D = 50\,mV$ is plotted in Figure 3-2. Two points in weak inversion are taken, $(V_{G1}, I_{D1}) = (0.2\,V, 264.3\,nA)$ and $(V_{G2}, I_{D2}) = (0\,V, 1.099\,nA)$. Using (3-1), the value of the subthreshold slope factor corresponds to $n = 1.41$.

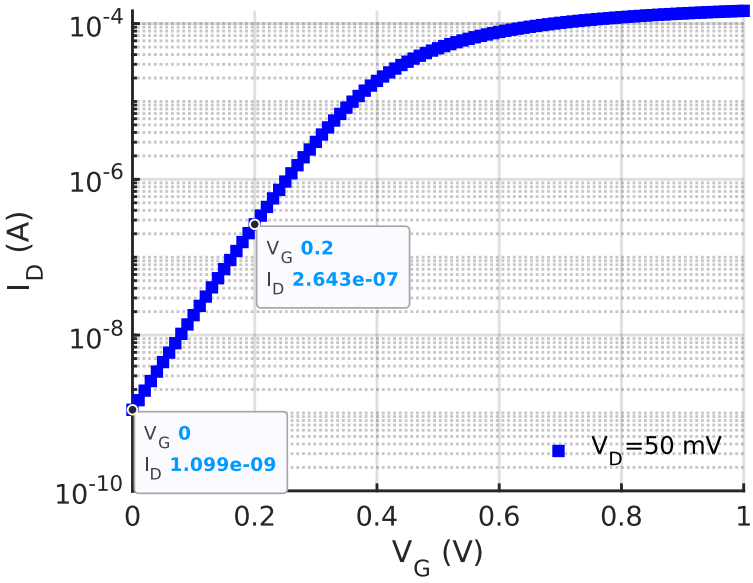


Figure 3-2. Extraction of the subthreshold slope factor, n=1.41, for a L=30 nm and W=1 um lvt n-channel transistor based on $I_D(V_G)$ characteristic at V_D=50 mV.

3.1.2 Threshold voltage and specific current

Based on the procedure g_m/I_D described in [48], V_{T0} and I_{S0} are extracted from the $I_D(V_G)$ and $g_m/I_D(V_G)$ characteristics in a common source configuration (Figure 3-1) with V_{DS} fixed to $U_T/2$ as depicted in Figure 3-3.

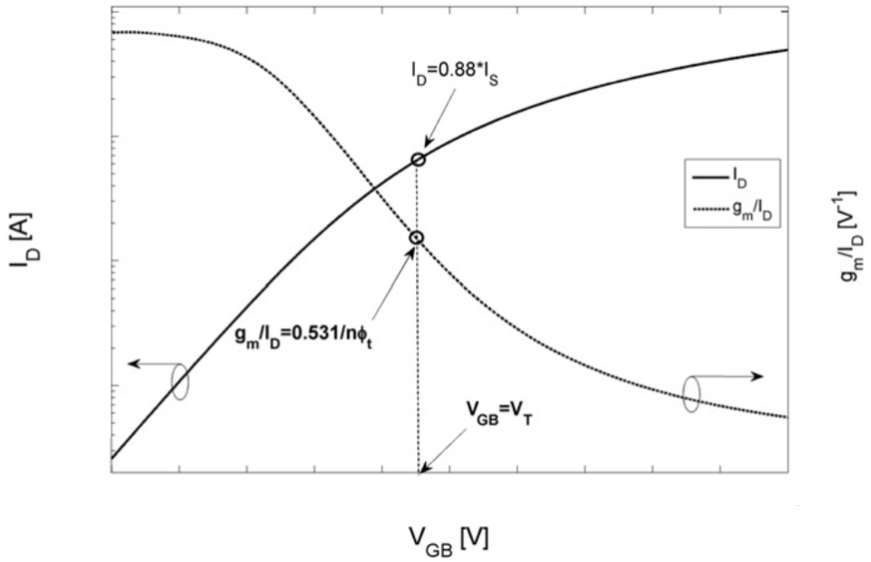


Figure 3-3. $I_D(V_G)$ and $g_m/I_D(V_G)$ characteristics and biasing condition allowing to extract the threshold voltage and the specific current at $V_{DS} = U_T/2$ [48].

The threshold voltage, V_{T0}, equals V_G when $V_P = 0\,V$, as suggested by the 3-parameter model equation (2-8) recalled below,

$$V_P = \frac{V_G - V_{T0}}{n} \tag{3-2}$$

Considering also that $V_S = 0\,V$, (*2-9*) gives

$$q_S - 1 + ln(q_S) = 0 \tag{3-3}$$

As a result, the threshold voltage equals the gate voltage when $q_S = 1$. Since V_{DS} is fixed to $V_{DS} = U_T/2 \ = 12.92\,mV$ for $T = 300\,K$, (2-11) leads to $q_D = 0.77$.

g_m/I_D is given by (3-4) for the 3-parameter model, so, $g_m/I_D = 0.531/nU_T$ for $q_S = 1$ and $q_D = 0.77$. Therefore, the threshold voltage is equal to the gate voltage for which $g_m/I_D = \ 0.531/nU_T$, as illustrated in Figure 3-3.

$$\frac{g_m}{I_D} = \frac{2}{nU_T(q_S + q_D + 2)}. \tag{3-4}$$

Additionally, I_{S0} can be computed from (2-7) as

$$I_{S0} = \frac{I_D}{(q_S - q_D)(q_S + q_D + 2)} \tag{3-5}$$

Consequently, from the same operating point, $I_{S0} = I_D(V_G = V_{T0})/0.88$. Figure 3-4 illustrates this procedure for the transistor of $L = 30\,nm$.Using (3-4) with $n = 1.41$, the g_m/I_D of interest is equal to $14.57\,V^{-1}$, and, at this point, $V_{T0} = V_G = 365.5\,mV$ and $I_{S0} = 3.82\mu A/0.88 = 4.34\,\mu A$.

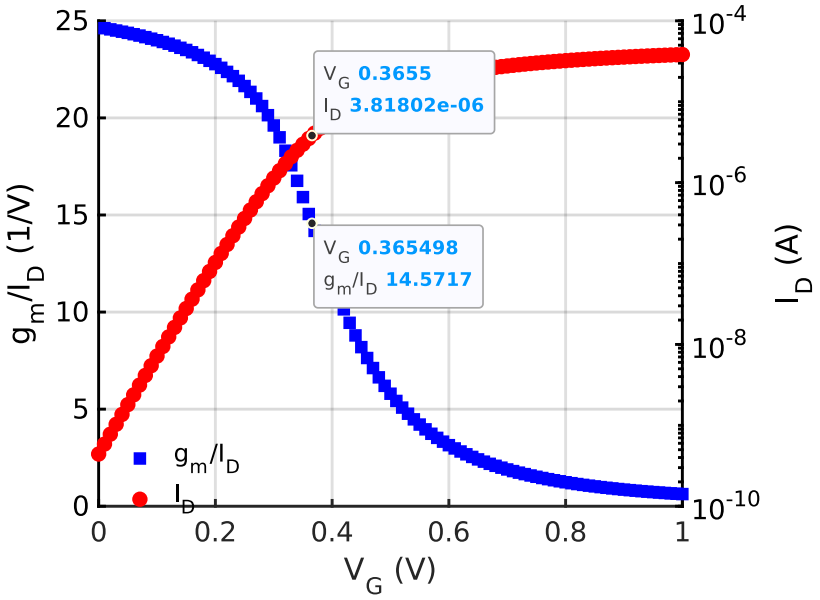


Figure 3-4. g_m/I_D and I_D characteristics versus V_G used for extraction of threshold voltage, V_{T0}=365.5 mV, and specific current, I_{S0}=4.34 μA.

3.1.3 Drain-induced Barrier Lowering (DIBL)

The DIBL parameter, σ, can be extracted from the semilogarithmic $I_D(V_G)$ characteristic taken for two values of V_D, V_{D1} and V_{D2}, preferably with a large difference between them. Then, we extract the crossing point of the two $I_D(V_G)$ curves with a constant current curve set at a low value, for example, $I_{D0} = W/L * 1\,nA$. Let us denote the V_G corresponding to the two crossing points as, $V_{G1}(I_{D0})$ and $V_{G2}(I_{D0})$, respectively. The DIBL parameter is given by the ratio between the difference of the gate voltages and difference of the drain voltages, as stated below:

$$\sigma = -\frac{\Delta V_G(I_{D0})}{\Delta V_D} = \frac{V_{G1}(I_{D0}) - V_{G2}(I_{D0})}{V_{D2} - V_{D1}}. \tag{3-6}$$

Applying this method to the studied transistor, two curves of $I_D(V_G)$ are taken, for $V_{D1} = 50\,mV$ and $V_{D2} = 1\,V$ as illustrated in Figure 3-5. As, $W = 1\,\mu m$ and $L = 30\,nm$, $I_{D0} = 33.3\,nA$, and the corresponding values of V_G are extracted, $V_{G1} = 122\,mV$ and $V_{G2} = 38\,mV$, resulting in $\sigma = 0.088$.

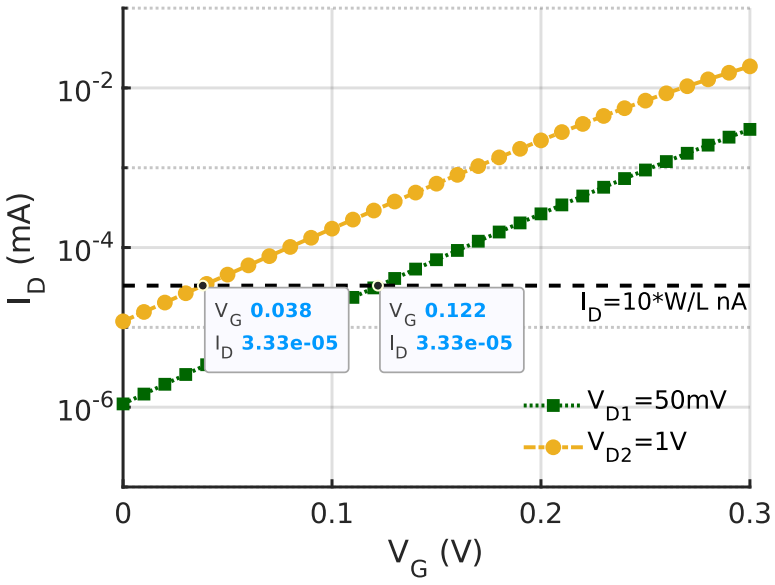


Figure 3-5. Extraction of DIBL parameter, σ=0.088, based on $I_D(V_G)$ characteristic for V_{D1}=50 mV and V_{D2}=1 V.

3.1.4 Mobility reduction factor, carrier velocity saturation and Channel Length Modulation (CLM)

Parameters related to carrier mobility reduction factor, carrier velocity saturation and CLM, are extracted by fitting $I_D(V_G)$ or $I_D(V_D)$ curves for specific biasing conditions where these parameters play a dominant role.

The first parameter to be determined is the carrier mobility reduction factor, θ. Given that in linear region (small values of V_D), carrier velocity saturation is not yet reached and CLM is negligible, the effect of θ parameter can be isolated. This means that, under the above conditions, a model based on simply five parameters (n, I_{S0}, V_{T0}, σ and θ) is enough to accurately describe the MOS transistor behavior. In practice, a $I_D(V_G)$ curve for a V_D in the linear region is taken and a fitting is done in the strong inversion regime ($V_G > 0.6\,V$) part of the characteristic, as is illustrated in Figure 3-6. The addition of the carrier mobility reduction in the model changes the drain current equation (2-7) to (2-12), and thus impacts the extraction of the specific current parameter, I_{S0}. Consequently, the fitting is done by optimizing both parameters, θ and I_{S0}, simultaneously.

For the 30nm transistor at $V_D = 100\,mV$, a least-square based optimization (using the function *'lsqcurvefit'* in MATLAB) gives $I_{S0} = 5.79\,\mu A$ and $\theta = 0.09$. It can be observed that the final value of I_{S0} is larger than initially, which is consistent with the expected effect of θ on the drain current.

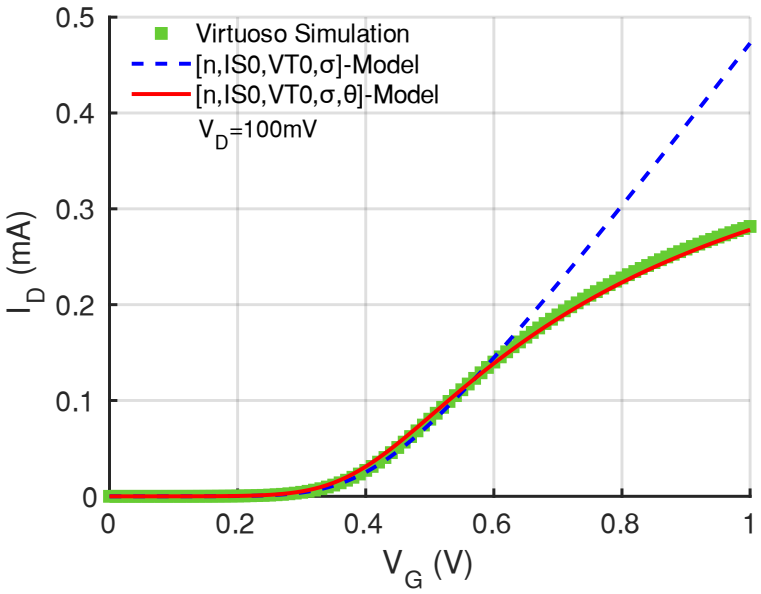


Figure 3-6. Fitting of $I_D(V_G)$ characteristic for V_D=100 mV, to determine specific current, I_{S0}=5.79 μA, and carrier mobility reduction parameter, $\theta = 0.09$.

Carrier velocity saturation effect becomes dominant in strong inversion regime for large values of V_D (in saturation region). So, as illustrated in Figure 3-7, its associated parameter, ζ, is determined by fitting the $I_D(V_G)$ characteristic, for a $V_D = 1\,V$, leading to $\zeta = 0.04$. For comparison, a simulation using a 5-parameter model (n, I_{S0}, V_{T0}, σ and θ) and using the optimized 6-parameter model (n, I_{S0}, V_{T0}, σ, θ and ζ) with $\zeta = 0.04$ is also shown.

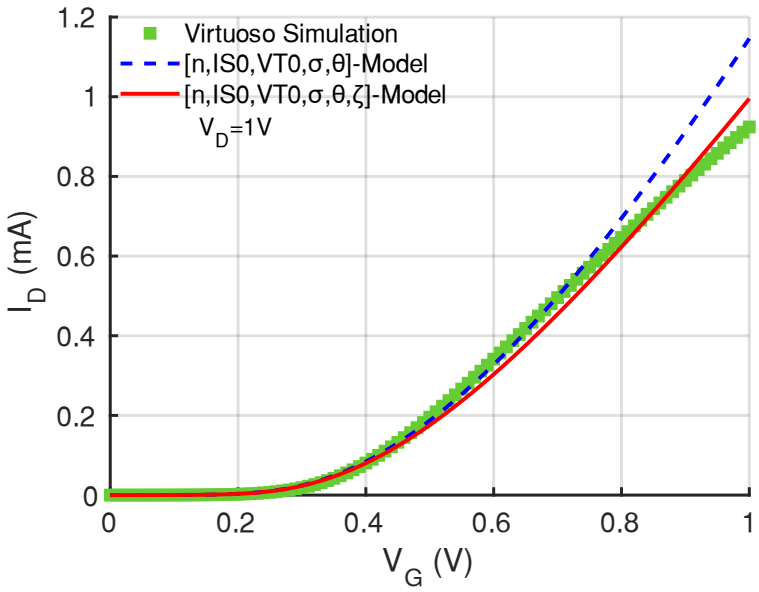


Figure 3-7. Fitting of $I_D(V_G)$ characteristic for V_D=1 V, to determine carrier saturation velocity parameter, $\zeta = 0.04$.

Finally, the CLM parameter, V_E, is a challenging parameter to determine, as it varies with V_G and the length of the transistor, L. Additionally, in short-channel devices, its effect can be hidden by the DIBL one, whereas for longer channel devices it becomes more visible. In our work, the estimation of the V_E is also done by fitting, comparing the model built with the 6 previous parameters and the simulation of the output characteristic, $I_D(V_D)$, of the MOS transistor. For the evaluated device, an optimization is done using least-square curve-fitting on $I_D(V_D)$ curves for values of V_G from $0.1\,V$ to $1V$ with a step of $0.1\,V$, obtaining $V_E = 5\,V$. The obtained model is illustrated in Figure 3-8 for $V_G = 400\,mV$.

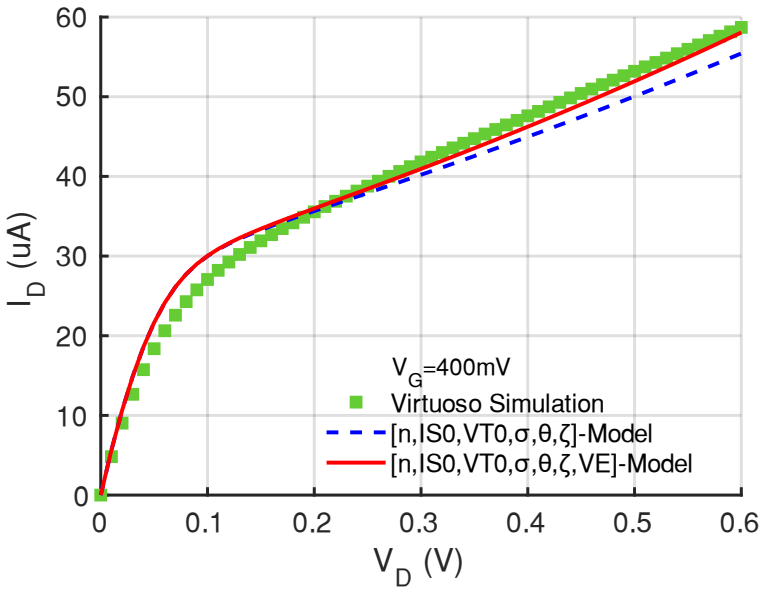


Figure 3-8. Fitting of $I_D(V_D)$ characteristic for several valued of V_G, illustrated here for V_G=400 mV, to determine CLM parameter, $V_E = 5\,V$.

3.2 Consistency of the proposed model

3.2.1 Validity for different channel lengths

The proposed 7-parameter model, based on physical effects as presented in chapter 2, is able to accurately describe the DC characteristics of the MOS transistors, for both long and short-channel lengths. Indeed, as it has been already published in the literature, the main parameters of the model can be made scalable with L [28], [35], [50]. However, in a practical design application, designers often prefer to extract the model parameters for a fixed L in order to keep the model as simple as possible and, therefore, reduce the set of parameters to be extracted. In that case, however, L cannot be used as a design variable. This drawback is mitigated by the fact that L is often determined at the beginning of the design sizing stage, as a function of the application requirements [13], [28].

In order to analyze the variation of the parameters with transistor channel length, a set of parameters has been extracted from DC measurements for three n-channel electrical lengths in 28 nm FD-SOI technology: $30\,nm$, $60\,nm$ and $150\,nm$, with a constant width of $1\,\mu m$. These parameters are presented in Table 3-1. The evolution of parameter values for different transistor lengths illustrates the physical mechanisms behind the parameters.

Table 3-1. Model Parameters for Three N-MOS Transistor Lengths (30 nm, 60 nm and 150 nm) in 28 nm FD-SOI Technology

Length/ Parameter	30 nm	60 nm	150 nm
Su*bthreshold* slope factor: n	1.377	1.138	1.092
Specific current: I_{S0} (uA)	5.9	3.25	1.83
Threshold voltage: V_{T0} (mV)	384.9	390.5	427
Mobility reduction: θ	0.115	0.079	0.047
DIBL: σ	0.093	0.018	0.003
Velocity saturation: ζ	0.035	0.056	0.06
CLM: V_E (V)	5	15	18.5

The subthreshold slope factor, n, and the DIBL factor, σ, increase for shorter channel devices, which is consistent with the larger impact of source-drain region on transistor electrostatics when the channel length reduces.

Also, when the channel length gets smaller, a consistent evolution in the value of the specific current, I_{S0}, is perceived, following (2-2), and the mobility reduction factor, θ, increases due to the series resistances contribution embedded in this factor.

According to (2-15), the carrier velocity saturation parameter, ζ, should monotonously increase when L reduces, which is not observed in the reported values of Table 3-1. As explained in section 2.4.1 , this is due to the impact of mobility reduction factor which lowers the carrier velocity saturation parameter value for small gate lengths.

Finally, the V_E value increases with the channel length, which is expected since CLM effect is proportional to $1/V_E$ and more pronounced on short-channel transistors.

3.2.2 Short-Channel Effects (SCEs)

To further appreciate the integration of SCEs in the proposed model, a comparison of the drain current normalized with respect to the size ratio, W/L, is done between a short ($L = 30\,nm$) and a long ($L = 150\,nm$) channel NMOS transistors in Figure 3-9. Several SCEs are visible when comparing both curves. First of all, the slope in subthreshold region, which reflects the subthreshold slope factor n, increases for the shorter transistor. The reduction of the threshold voltage when the channel length is reduced is also visible in this figure. Finally, the current reduction in strong inversion can be observed for the short-channel transistor showing the effect of the carrier velocity saturation and the series resistances.

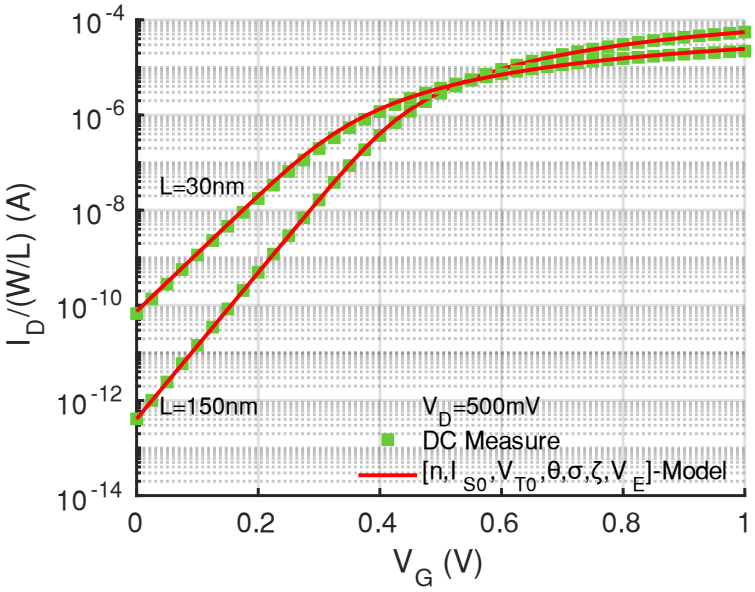


Figure 3-9. $I_D/(W/L)$ (V_G) curve: Comparison of a long (L=150 nm) and a short (L=30 nm) channel NMOS transistors, for DC measures (green squares) and 7-parameters model simulations(red solid line). The impact of SCEs on the subthreshold slope, threshold voltage, carrier velocity saturation and series resistance, is clearly visible.

3.2.3 Threshold Voltage Roll-off

The threshold voltage roll-off, $V_{T\,Roll-off}$, when transistor channel length reduces is an accurate measure of the SCEs, as reported in [51]. Figure 3-10 presents the $V_{T\,Roll-off}$ for three different values of V_D, built with the three channel lengths studied in this chapter. The simulations with the proposed model are in good agreement with the DC measurements, with a maximum error of around $20\,mV$ in the worst-case scenario.

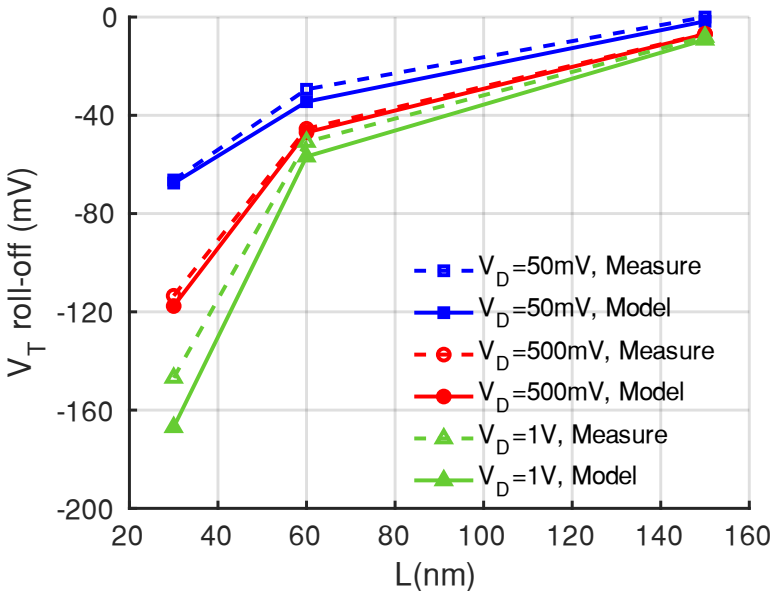


Figure 3-10. V_T roll-off for three values of drain voltage, V_D=50 mV (square blue line), V_D=500 mV (circle red line) and V_D= 1 V (triangle green line) from DC measures (dashed curves) and 7-parameter model simulations (solid curves).

3.2.4 Relative Error

To further evaluate the accuracy of the 7-parameter model, we estimated, for each channel length, the Relative Error (RE) between the simulated and measured $I_D(V_G)$ and $I_D(V_D)$ characteristics as follows:

$$\mathrm{RE}\ (\%) = \frac{Model - Measure}{Measure} * 100\% \,. \tag{3-7}$$

As presented in Figure 3-11, the relative error is well contained in weak and strong inversion regimes for the $I_D(V_G)$ and $I_D(V_D)$ curves, while the maximum relative error reaches 30% close to the threshold voltage (around $0.4\ V$) for small values of V_D ($V_D = 50\ mV$) in triode region. Regarding the $I_D(V_D)$ curves, for V_D values above $150\ mV$, the relative error does not exceed 10%.

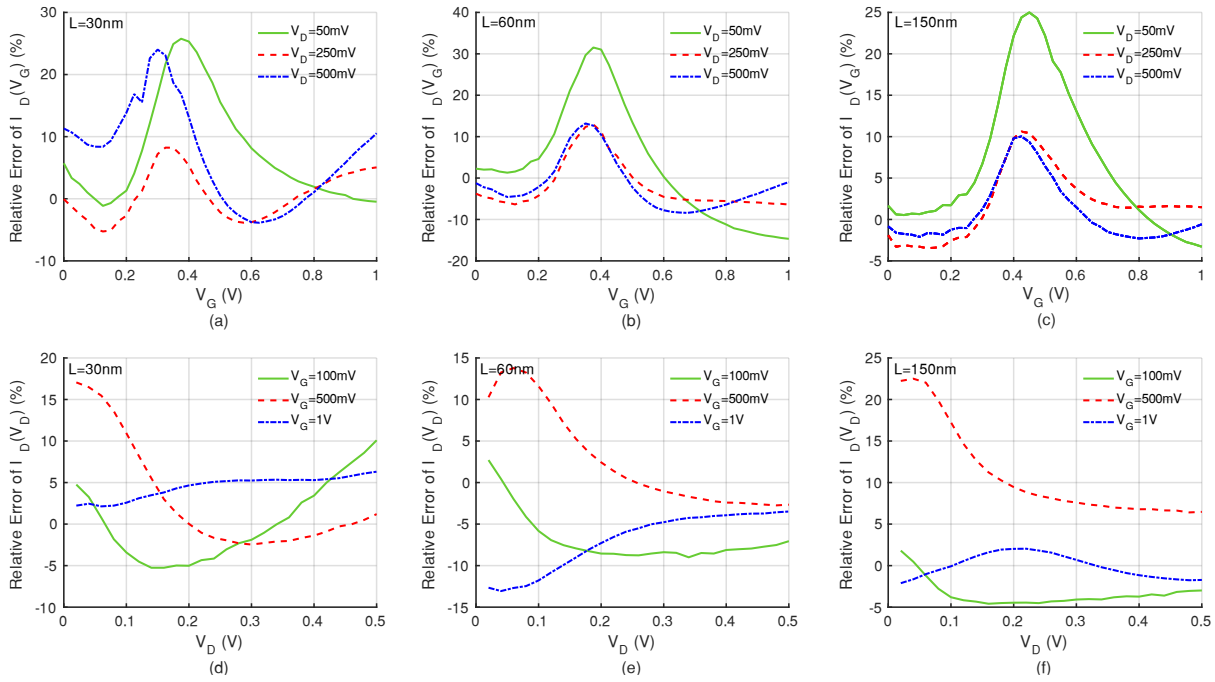


Figure 3-11. Top: Relative error for three $I_D(V_G)$ curves for L=30 nm (a), L=60 nm (b) and L=150 nm (c) N-MOS transistors for different values of V_D: 50 mV (solid green line), 250 mV (dashed red line) and 500 mV (dot-dashed blue line).Bottom: Relative error for three $I_D(V_D)$ curves for L=30 nm (d), L=60 nm (e) and L=150 nm (f) N-MOS transistors for different values of V_G: 100 mV (solid green line), 500 mV (dashed red line) and 900 mV (dot-dashed blue line).

3.2.5 Discussion on design-oriented models

To summarize the advantages and disadvantages of the proposed design-oriented model, Table 3-2 presents a comparison of its main features to the ones of complete compact models, 4-parameter EKV/ACM simplified models, and LUT-based models. The comparison is illustrated using “+” and “-” signs for designating advantages and disadvantages respectively. Besides, the degree of improvement of a model according to a feature is highlighted by the number of these signs, where “+++” refers to the best-in-class.

Table 3-2. Comparison of the different models in terms of main design methodology features

Features	Compact models	4-param. EKV/ACM models	LUT models	This work
Simulation accuracy	+++	+	++	++
Model simplicity	--	++	++	+
V_D dependency	+++	-	+	++
Ease of use	++	++	+	++
Explicit link with technology	++	+	-	++

+++ Very good, ++ Good, + Fair, - Poor

Compact models present in CAD simulator tools, such as BSIM-IMG [18] and UTSOI2 [19], [20] for FD-SOI technologies, have hundreds of parameters some of them being based on the transistor physics, but others being only fitting parameters to provide a larger flexibility of the model. This makes the model not easy to understand by circuit designers, many of these parameters being difficult to interpret. On the other hand, those models are rather complete and provide a good accuracy for matured, well-characterized technologies. Design methodologies based on such compact models rely on extensive simulation campaigns, and, of course, the designer experience, but also heavily on trial-and-error optimization loops to discover the influence of the different variables or components on the circuit performance.

Much simpler 4-parameters EKV/ACM models presented in [33], [34], [36] have been applied to the design of different kind of RF circuits [35], [36], [52]. Even if these models are easy to use in design methodologies due to their simplicity, they are generally limited to the operation point of the given circuit or application, and, therefore, used in a certain operation region (linear or saturated) or inversion regime, as for applications in ultra-low-power domain, for example.

LUT-based models [10], [12] have a good accuracy and represent very well the trends followed by certain parameters needed for design. However, the link to the MOS transistor physics or to the technology is lost, since the LUTs are obtained in large and automated simulation campaigns.

Some design methodologies make use of 3-parameter models and LUT [15], [50] or 4-parameter models and LUT [4], [13], [14].In these approaches, the active part of the circuit, linked to the transistor, is modeled based on the inversion coefficient and the parameters related to the transistor size and the technology, while the LUT are used to determine the RF behavior, proposing curves or tables with the extracted values of the intrinsic capacitances of the transistor, for example. This allows to

compensate some of the limitations of the LUT in the active part (physical transistor behavior). However, this is still not enough to have a complete analytical design methodology based on the model.

The proposed 7-parameter model, although more complex due to the integration of the above-mentioned SCEs, remains a reduced set of equations and provides a really good accuracy for all inversion regimes and all operation regions, presenting also a good agreement with the dependence on the drain voltage. An example the application in an RF circuit design methodology using this model will be presented in chapter 4.

3.3 Conclusions

The results presented so far demonstrate that the proposed analytical design-oriented model is robust and able to describe the behavior of the transistor drain current in all inversion regimes and all operation regions. The validity of the model has been proved for both short and long-channel transistors of STMicroelectronics 28nm FD-SOI technology, and a straightforward methodology to extract the model parameters has been also presented.

The comparison of the extracted models for different channel lengths highlights the short-channel effects in this technology node, and a clear variation of the parameters with respect to channel length is observed. In addition, the trend of the parameter values can be predicted according to the physics of the transistor since the model parameters have a physical meaning.

The increased complexity of the model has to be compared to previously presented approaches based on look-up tables or empirical V_D-dependent parameters, and also to compact models implemented in CAD simulators. In practice, the 7-parameter model can be used in circuit design as it is simple to implement and offers a good accuracy on the estimation of the MOS transistor behavior, without leaving aside the dependence on V_D. Moreover, the fact that the model keeps a direct link with the technology through its parameters may open the door to future applications for circuit/technology co-optimization.

Chapter 4: Resistive Feedback LNA Design based on the 7-Parameter Model

It has been demonstrated that the proposed analytical 7-parameter model presents a good trade-off between the number of parameters used and its accuracy when describing the MOS transistor operation in advanced technology such as the 28nm FD-SOI of STMicroelectronics.

The aim of this chapter is to validate the model through its implementation in a RF circuit design methodology considering for the first time the non-linear performances ($IIP3$) thanks to the modeling of the transistor non-linear behavior (g_m and g_d) in a simple charge-based model. The proposed design methodology allows to explore the design space for a Resistive feedback (R-feedback) LNA and to select the right sizing (transistor W and bias, passive components values) to comply with the target specifications of noise figure, NF, voltage gain, G_V, power consumption, I_{DC}, third order input interception point, $IIP3$, for an operation frequency, f_0.

The R-feedback topology is chosen for several reasons. First, it is a common topology for low-cost and low-power applications such as IoT which correspond to one of the main research tracks of the TIMA laboratory and STMicroelectronics. Secondly, this topology presents a good trade-off between cascode structure which requires high power voltage and common gate structure which exhibits relatively high noise factor. In addition, previous works in the field of design methodology using charge-based models exist in the laboratory and the presented study aims to improve the existing method especially concerning non-linearities [15]. The targeted requirements are given in Table 4-1 and are typical for ultra-low power applications:

Table 4-1. Specifications for Resistive Feedback LNA performance

f_0 (GHz)	G_T (dB)	NF (dB)	$IIP3$ (dBm)	I_{DC} (mA)
1	> 22	< 3	> -20	< 0.6

Hereinafter, the architecture for the R-feedback LNA is presented together with the main performance equations related to this topology. In this first step, the transistor is abstracted to its small signal equivalent circuit (g_m, g_{ds}, etc.). Then, the 7-parameter model will be used to express a direct relationship between the LNA performances in saturation region and the design variables (components, biasing and size) that will be used for the transistor sizing and biasing conditions. Later, a comparison is made

between the results obtained through the proposed design methodology with respect to the simulations in cadence and, with respect to the circuit measurements for an LNA which had been previously conceived by Serge Subias (a former research engineer at TIMA laboratory). Finally, the last section shows how this model can be used to evaluate the variation of the R-feedback LNA performances in function of the variation of the parameters of the transistor model (I_{S0}, ζ, θ). This analysis will directly lead to a real analysis to choose the best technology to achieve targeted performances, paving the way to a real circuit/technology co-optimization. The chapter ends with the conclusions on the proposed design methodology and the perspectives on the way towards improved analytical RF circuit design methodologies.

4.1 Resistive Feedback LNA

The main design equations related to the topology are provided here. A particular attention to the input Q factor (Q_{IN}) is given in the analysis. In addition, the maximum operating frequency defined by the cutting frequency is also kept as an explicit parameter to better understand the limit of the design space. The R-feedback LNA topology is presented in Figure 4-1 and its small signal equivalent circuit in Figure 4-2. For following equation development, a dashed square box identifies the LNA core.

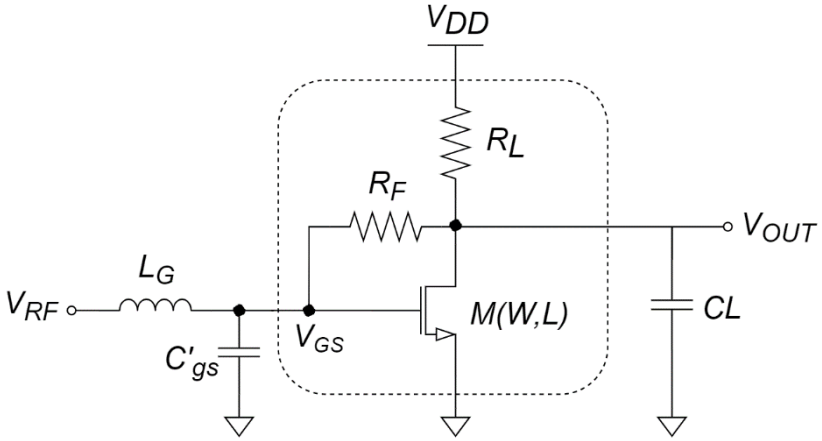


Figure 4-1. Resistive Feedback LNA circuit.

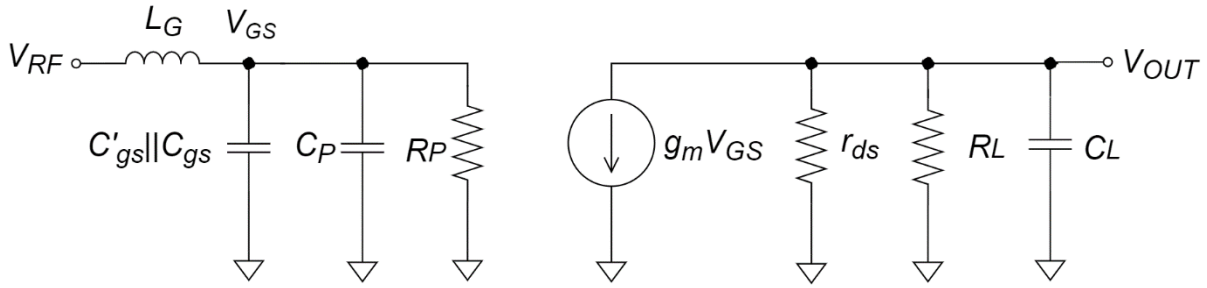


Figure 4-2. Small signal equivalent circuit for Resistive Feedback LNA.

One of the main interests of this architecture is that the feedback resistance, R_F, allows to synthesize the real part of the input impedance of the circuit, Z_{in}. However, an LC matching network composed of L_g and C'_{gs} is also implemented to null the imaginary part of the input impedance. The input impedance of the circuit is given by:

$$Z_{in} = L_g s + \left(\frac{1}{(C_{gs} + C'_{gs})s} || Z_P \right), \tag{4-1}$$

where, Z_P is the input impedance of the LNA core, seen at the gate (Figure 4-2), expressed as

$$Z_P = \frac{1}{\frac{1}{R_P} + C_P s}, \tag{4-2}$$

where R_P and C_P are respectively the equivalent parallel resistance and capacitance seen at the gate. R_P and C_P can be defined relatively to the operating frequency f_0 and output cutoff frequency,

$$f_c = \frac{R_{out} + R_F}{2\pi R_{out} R_F C_L}. \tag{4-3}$$

where R_{out} is the output resistance given by the drain-source resistance, r_{ds}, and the load resistance, R_L, in parallel,

$$R_{out} = r_{ds} || R_L . \tag{4-4}$$

The expressions of R_P and C_P are:

$$R_P = \frac{1 + \left(\frac{f_0}{f_c}\right)^2}{\frac{1 + G_m R_{out}}{R_{out} + R_F} + \frac{1}{R_F}\left(\frac{f_0}{f_c}\right)^2}, \tag{4-5}$$

$$\frac{1}{C_P} = \left(1 + \frac{R_F}{R_P}\right)^2 \frac{1 + \left(\frac{f_0}{f_c}\right)^2}{C_L(1 - G_m R_F)}, \tag{4-6}$$

Under the assumption where the operating frequency is well below the cutoff frequency, R_P and C_P can be simplified as bellow:

$$R_P = \frac{R_{out} + R_F}{1 + G_m\ R_{out}}, \tag{4-7}$$

$$C_P = \frac{R_{out}^2 C_L (G_m R_F - 1)}{(R_{out} + R_F)^2}. \tag{4-8}$$

The conditions to be matched to source generator impedance (R_S) the, which corresponds to the antenna impedance for an LNA. are:

$$\Re(Z_{in}) \triangleq R_{in} = \frac{R_P}{1 + Q_P^2} = R_S\,, \tag{4-9}$$

and,

$$\Im(Z_{in}) = L_g s + \frac{Q_P^2}{C_T s(1 + Q_P)^2} = 0\,, \tag{4-10}$$

where,

$$C_T = C_{gs} + C'_{gs} + C_P\,, \tag{4-11}$$

is the total capacitance at the input node, and Q_P defined as follow:

$$Q_P = R_P C_T \omega_0\,. \tag{4-12}$$

The total voltage gain of the resistive feedback LNA is given by:

$$G_T = \left|\frac{V_{OUT}}{V_{RF}}\right| = |G_V| \frac{Q_{IN}}{\sqrt{1 + \left(\frac{f_0}{f_c}\right)^2}} \cong\ Q_{IN}|G_V| \text{ if } f_0 \ll f_c\,, \tag{4-13}$$

where, G_V is the circuit voltage gain of the LNA core, with respect to the gate terminal and without considering the matching network given by

$$G_V = \frac{V_{OUT}}{V_{GS}} = -\frac{(G_m R_F - 1)\, R_{out}}{R_{out} + R_F}. \tag{4-14}$$

The input quality factor (Q_{IN}) is related to Q_P as:

$$Q_{IN} = \sqrt{1 + Q_P^2}. \tag{4-15}$$

The noise factor is given by:

$$F = 1 + A\left[\gamma + \frac{1}{G_m R_L} + \frac{\left(1 + \frac{G_m R_S R_F}{R_F/Q_{IN}^2 + R_S}\right)^2}{G_m R_F}\right], \tag{4-16}$$

with

$$A = \frac{\left(\frac{R_{in} + R_S}{R_{in}}\right)^2 (R_F/Q_{IN}^2 + R_S)^2}{Q_{IN}^2 G_m R_S \left(R_F/Q_{IN}^2 + R_S + G_m R_S (R_F || R_{out})\right)^2}. \tag{4-17}$$

Therefore, the noise figure is given by

$$NF = 10 \log_{10}(F)\,. \tag{4-18}$$

When the input impedance is matched to the source, $R_{in} = R_S$,

$$\frac{R_{in} + R_S}{R_{in}} = 2\,. \tag{4-19}$$

The 3rd order interception point is expressed as

$$IIP3 = \sqrt{\frac{4G_T}{3A_{V3}}} = \sqrt{\frac{8}{Q_{IN}^2}\frac{G_m R_F - 1}{G_{m3} R_F}}, \tag{4-20}$$

where A_{V3} is the third order coefficient in the Taylor series for the gain considering the non/linearities. Given in dBm is

$$IIP3_{\ dB} = 20\log_{10}(IIP3)\,. \tag{4-21}$$

4.2 Exploration of the design space

Proposed design methodology consists in using the circuit equations developed in previous section to compute all possible performances values combination (design space) and then, depending on the specifications, to choose the right set of values (namely, L_g, C_P, …) fulfilling the requirements.

To explore the design space of this circuit, it is proposed to integrate the equations given in the previous section, establishing the performances of the R-feedback LNA, with those that constitute the 7-parameter model. For that purpose, a set of parameters must be defined to represent the transistor.

In former design methodologies based on 3 parameters, the g_m/I_D characteristic was used conveniently as it was possible to have a directly relationship with respect to the inversion level (i_f or IC) and to its size, W, allowing to have simple analytical design methodologies, but which included some iterations to calculate the size and polarization of the circuit.

In the proposed method, we use the equations of (g_m, g_{m3} and g_{ds}) derived in absence of carrier velocity saturation (but taking into account DIBL and carrier mobility reduction) given by (*2-33*), (*2-35*) and (*2-36*) recalled here for sake of clarity:

$$g_m = \frac{2}{nB}\left[q_S - q_D - i_d\frac{\theta}{4}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right)\right],$$

$$\begin{aligned} g_{m3} = \frac{2}{n^3 B}\Bigg[&\frac{q_S}{(1+q_S)^3} - \frac{q_D}{(1+q_D)^3} \\ &- \frac{\theta}{4}\Bigg[3n^2 g_{m2}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + 3n g_m\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right) \\ &+ i_d\left(\frac{q_S(1-2q_S)}{(1+q_S)^5} + \frac{q_D(1-2q_D)}{(1+q_D)^5}\right)\Bigg]\Bigg], \end{aligned}$$

$$g_{ds} = \frac{2}{B}\left[\frac{\sigma}{n}q_S - \left(\frac{\sigma}{n} - 1\right)q_D - i_d\frac{\theta}{4}\left(\frac{\sigma}{n}\frac{q_S}{1+q_S} + \left(\frac{\sigma}{n} - 1\right)\frac{q_D}{1+q_D}\right)\right],$$

with

$$B = 1 + \frac{\theta}{2}(q_S + q_D)\,.$$

Because the MOS operates in saturation region in the R-Feedback LNA, q_D is replaced by q_{Dsat} which can be evaluated for each q_S by (*2-19*), recalled here for sake of clarity:

$$q_S = \frac{\theta}{2\zeta} q_{Dsat} - 1 + \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)}.$$

Hence, (g_m, g_{m3} and g_{ds}) only depends on q_S and the 7 parameters. Denormalizing the small signal parameters allows to introduce W as follows:

$$G_{yx}(W, q_S) = \mu C'_{ox} \frac{(U_T)^x}{2} \frac{W}{L} g_{yx}(q_S) \tag{4-22}$$

where yx is chosen in $[m; ds]$ depending on the transconductance nature and x is the order of the considered conductance. Then, it appears that the small signal parameters (g_m, g_{m3} and g_{ds}) only depend on W and q_S which will be considered as design parameters and the 7 model parameters which will be considered as constant. Based on the small signal circuit analysis, the performances (G_V, NF, $IIP3$, I_D) will be expressed as a function of the transistor size and its inversion level, through W and q_S to explore de design space.

As mentioned before, the 7-parameter model is not scalable with respect to the transistor length and thus, L is not considered among the design variables. However, it is possible to build different design spaces for different L to choose the best suited length. On the other hand, L value is mainly determined by the operating frequency, and thus transistor f_T requirements, so, L can be determined a-priori.

For sake of simplicity, many design approaches do not consider the input Q-factor (Q_{IN}) and perform the optimization on the LNA core (inside the dotted line of Figure 4-1), knowing that Q_{IN} finally improves both, gain and noise figure. However, this can lead to an overdesign that impacts the energy efficiency and leads to several iterations or optimization. In this work, we propose to perform the optimization on the complete LNA considering Q_{IN} at the first steps for a direct estimation of the performances and an accurate sizing.

4.2.1 Maximum gain

For a Resistive feedback LNA, as pointed by the authors in [15], maximizing the load resistor, R_L, does not always maximize the gain especially when the supply voltage, V_{DD}, is larger than V_A, as it is often the case in advanced technologies.

The intrinsic voltage gain (i.e., without input matching network) of the resistive feedback LNA, G_V, can be expressed as (4-14). As $R_{out} = r_{ds}||R_L$, both resistances can be expressed as

$$R_L = \frac{V_{DD} - V_{DS}}{I_0}, \tag{4-23}$$

$$r_{ds} = \frac{V_A + V_{DS}}{I_0}. \tag{4-24}$$

Therefore, the intrinsic voltage gain can be approximated by

$$|G_V| = \frac{g_m R_F - 1}{1 + \frac{I_0 R_F (V_A + V_{DD})}{(V_{DD} - V_{DS})(V_A + V_{DS})}}, \tag{4-25}$$

and, the maximum gain is achieved under the condition of

$$r_{ds} = R_L = \frac{V_A + V_{DD}}{2I_0}. \tag{4-26}$$

In consequence,

$$R_{out} = \frac{r_{ds}}{2} = \frac{1}{2G_{DS}}, \tag{4-27}$$

for an optimal V_{DS}:

$$V_{DS,opt} = \frac{V_{DD} - V_A}{2}. \tag{4-28}$$

4.2.2 Operating frequency

As already mentioned, the operating frequency shall be chosen well below f_c to satisfy (*4-7*) and (*4-8*) and guaranty a good accuracy of the method. In the following sections we consider $f_c = 4f_0$ which guaranty 10% variation on R_P and C_P. From (4-3) and (*4-27*), it is possible to express R_F as follows:

$$R_F = \frac{1}{f_c 2\pi C_L - 2G_{DS}} = \frac{1}{8\pi f_0 C_L - 2G_{DS}} \tag{4-29}$$

Setting f_c allows to reduce R_F dependency to only C_L (and q_S and W) which will be the third design parameter used in this method.

4.2.3 Design space graphic representation

The design space will be explored for the transistor given in Table 4-2. To observe the effect of L, the designer shall run the method for different values. This may be considered as the most limiting issue of the presented method. However, the sizing using mathematical tools such Matlab is quite fast to run and an iterative study is possible.

Table 4-2. Model parameters for an NMOS lvt of L=40 nm and W=1 µm

$L\ (nm)$	n	$I_{S0}\ (\mu A)$	$V_{T0}\ (mV)$	θ	σ	ζ	$V_E\ (V)$
40	1.8	5.4	386	0.096	0.047	0.04	10

4.2.3.1 q_S versus W

Getting an understandable and meaningful graphic representation of the design space is not obvious since the number of parameters is quite large. To reduce the number of parameters we chose to introduce a relationship between q_S and W through the gain since it is one of the most important performance in the amplifier design. The design space will be explored for a fixed voltage gain, G_T and for different values of C_L. To do so, the G_T expression is first rearranged. From the input matching condition (4-9) we have,

$$Q_{IN} = \sqrt{1+Q_P^2} = \sqrt{\frac{R_{out}+R_F}{R_S(1+G_m R_{out})}} = \sqrt{\frac{\frac{1}{2G_{ds}}+\frac{1}{8\pi f_0 C_L - 2G_{ds}}}{R_S\left(1+\frac{G_m}{2G_{ds}}\right)}} \qquad (4\text{-}30)$$

leading (from (4-13)) to an expression of the gain that only depends on C_L, q_S and W:

$$G_T = \frac{\frac{G_m}{8\pi f_0 C_L - 2G_{ds}} - 1}{1+\frac{1}{4\pi f_0 C_L/G_{ds} - 1}} \sqrt{\frac{\frac{1}{2G_{ds}}+\frac{1}{8\pi f_0 C_L - 2G_{ds}}}{R_S\left(1+\frac{G_m}{2G_{ds}}\right)}}. \qquad (4\text{-}31)$$

In Figure 4-3, the relationship between q_S and W investigated for different C_L and it is computed for $G_T = 12{,}98\ (22{,}3dB)$ which is the value that gives the DC current that has been measured (obtained after few iterations). Since the circuit has been designed before the study, we choose to run the method based on this particular gain value to better observe the precision of the method and compare the different performances obtained with simulation, measurement and the method at constant I_{D}. As expected, when W increases, the inversion level can be reduced for a given gain allowing to increase the energy efficiency by increasing the transistor size. On the other hand, increasing C_L leads to a higher q_S to maintain the same maximum frequency showing a trade-off. In other word, charging the LNA will require more inversion (i.e. more energy) to maintain the same gain.

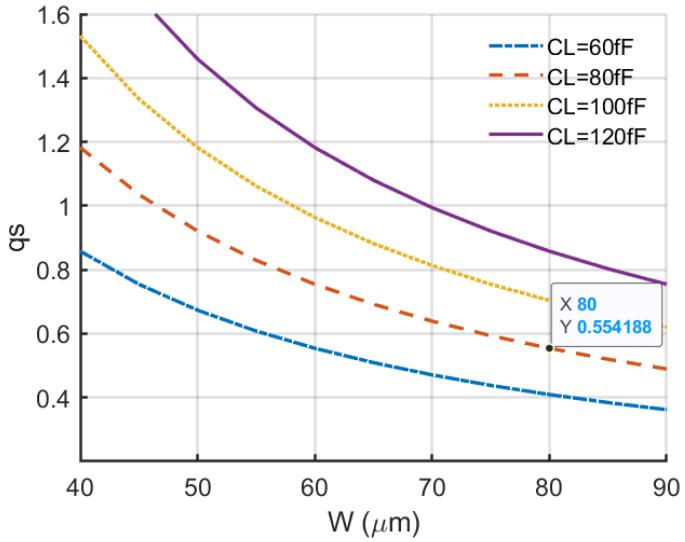


Figure 4-3. (W, q_S) relationship for fixed value of total gain $G_T = 12{,}98$.

Thanks to the relationship between q_S and W obtained for a given G_T, it is possible to explore the design space. Prior to explore the performances, it is interesting to plot few important design features such as g_m or Q_{IN} which will give interesting insight to better analyze the R-feedback LNA behavior.

4.2.3.2 Transconductance (G_m) output conductance (G_{ds}) and input Q-factor (Q_{IN})

The transconductance (G_m) is plotted with (2-33) and (4-22) on Figure 4-4. It appears to be constant over W which is due to the fact that, as shown in Figure 4-3, W varies accordingly with q_S to maintain a constant gain G_T leading to a constant G_m and G_{DS} since G_T only depend on these two parameters (when C_L is fixed) as shown by (4-31). Over C_L the G_m increases showing the fact that the circuit need more current to charge the load while maintaining the same gain.

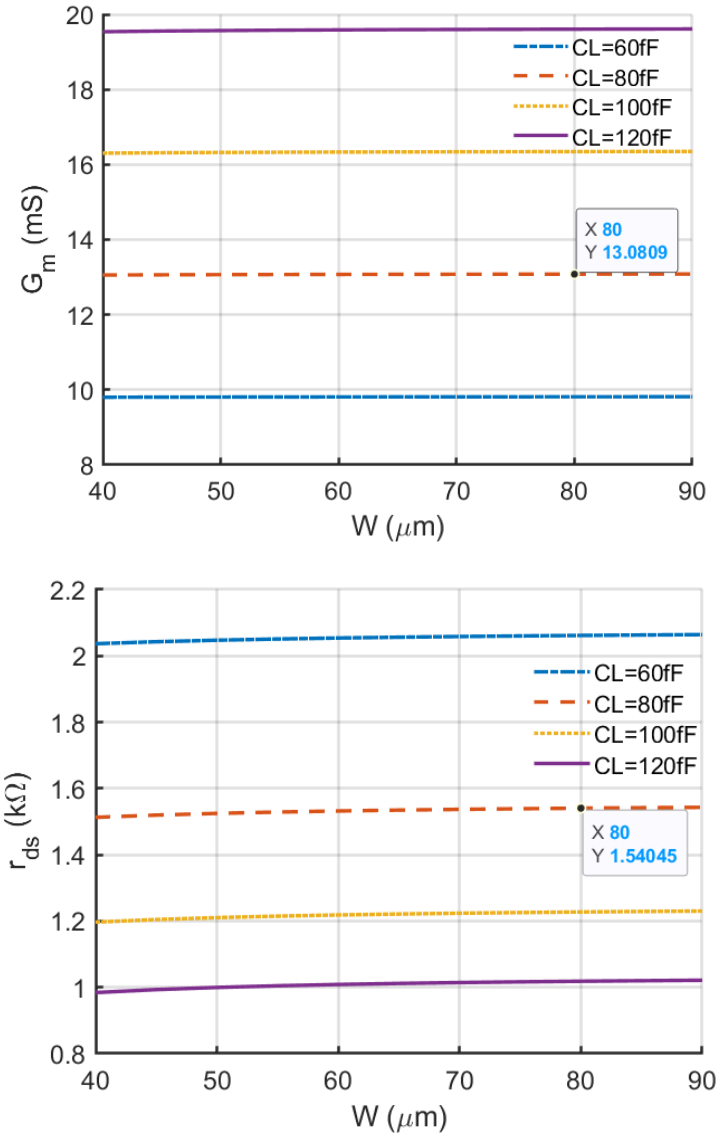


Figure 4-4. G_m and $r_{DS} = 1/G_{DS}$ for a total gain $G_T = 12{,}98$.

In the same manner, as shown in Figure 4-5, the Q-factor remain quite constant with W.

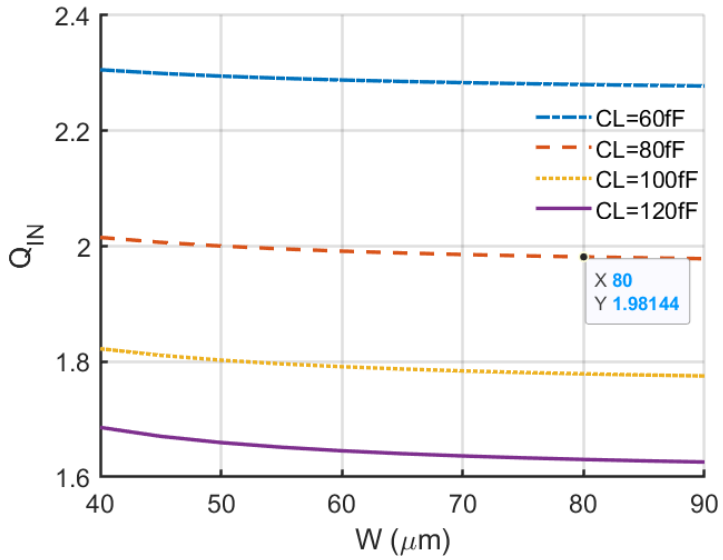


Figure 4-5. Input quality factor (Q_{IN}) for different values of W and C_L.

4.2.3.3 Noise factor

From (*4-16*) and (*4-17*), an expression of the noise factor that only depends on C_L, q_S and W is derived as follows:

$$F = 1 + A\left[\gamma + \frac{G_{ds}}{G_m} + \frac{\left(1 + \frac{G_m}{\frac{2g_{ds}+G_m}{1+\frac{G_{ds}}{4\pi f_0 C_L - G_{ds}}} + 8\pi f_0 C_L - 2G_{ds}}\right)^2}{\frac{G_m}{8\pi f_0 C_L - 2G_{ds}}}\right], \tag{4-32}$$

$$A = \frac{4\left(\frac{R_S(1+G_m G_{ds})}{4\pi f_0 C_L/G_{ds}} + R_S\right)^2}{g_m \frac{1+\frac{2G_{ds}}{8\pi f_0 C_L - 2G_{ds}}}{2G_{ds}+G_m}\left(1+\frac{G_m + 2G_{ds} + 2G_m G_{ds}^2}{8\pi f_0 C_L}\right)^2}, \tag{4-33}$$

It is observed in Figure 4-6 that the NF is quite constant and depends weakly on W and C_L. This comes from that the design space is explored from a constant

gain G_T. It is well known that the noise factor is inversely proportional to the square of the gain.

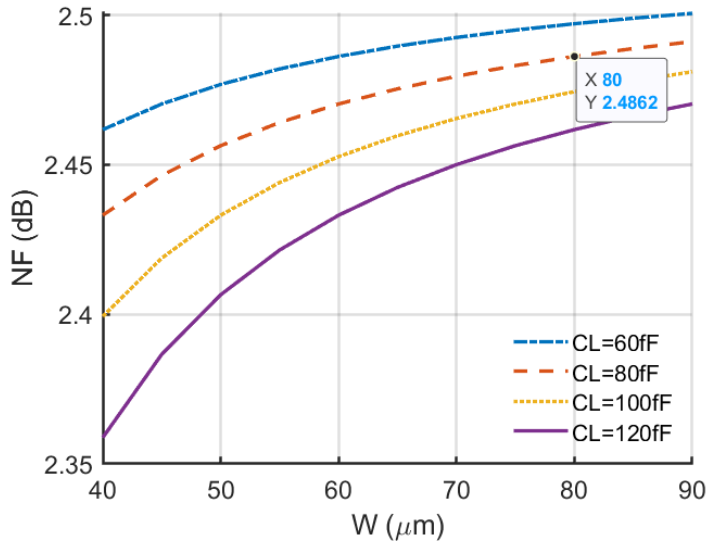


Figure 4-6. Noise figure for different values of W and C_L.

4.2.3.4 Non-linearities

Non-linearities are maybe the most interesting characteristic to be explored since it has never been proposed in former published method and consist in one of the main objectives of this PhD thesis. From (*4-20*), the following expression of the $IIP3$ which only depends on C_L, q_S and W is derived leading to the graph presented in Figure 4-7.

$$IIP3 = \sqrt{\frac{8R_S\left(1+\frac{G_m}{2G_{ds}}\right)(G_m - 8\pi f_0 C_L + 2G_{ds})}{G_{m3}\left(\frac{1}{2G_{ds}} + \frac{1}{8\pi f_0 C_L - 2G_{ds}}\right)}}. \quad (4\text{-}34)$$

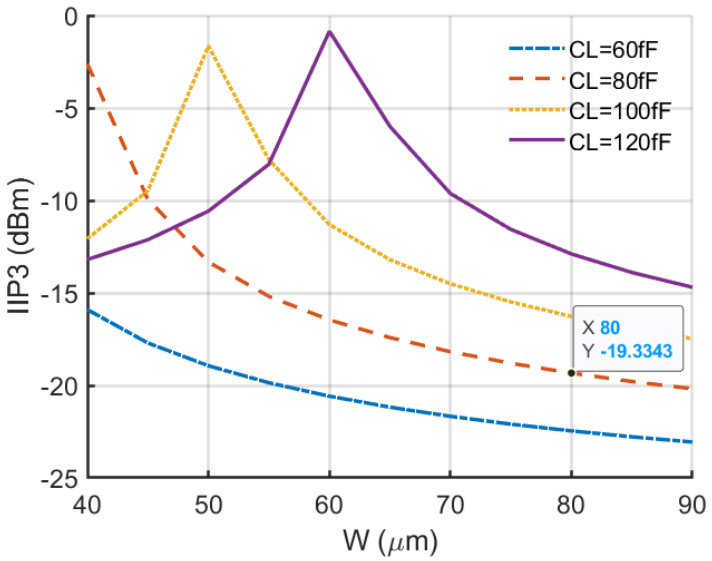


Figure 4-7. 3rd order input interception point, $IIP3$ for different values of W and C_L.

The effect of the sweet spot (see Figure 2-14) is observed in Figure 4-7. The maximum of $IIP3$ is due to the fact that the $IIP3$ tends to a theoretical infinite value when the g_{m3} is null. For $C_L = 80\ fF$ this infinite value occurs for values of W between 35 and 45 μm. Even if this sweet spot is never reached, it corresponds to an optimum when highly linear applications are targeted.

The effect of the load is also interesting to observe. Charging the output (i.e. increasing C_L), moves the sweet spot toward the large W. For a given W, $IIP3$ rises with C_L because the current increases to maintain the constant gain which is achieved by increasing the G_m that compensates for the r_{ds} lowering.

4.2.3.5 DC current

The DC current is the last main characteristic to be explored. I_D is directly plotted in Figure 4-8, from (*2-25*) which is recalled here:

$$I_D = I_{S0}\left(1 + \frac{V_{DS} - V_{Dsat}}{V_E}\right)\frac{(q_S + q_{Dsat} + 2)(q_S - q_{Dsat})}{1 + \frac{\theta}{2}(q_S + q_{Dsat})}.$$

Since V_{Dsat} only depends on q_S and q_{Dsat} as shown by (*2-20*) recalled here for sake of clarity, I_D can be plotted as a function of W and C_L as shown in Figure 4-8.

$$\frac{V_{DSsat}}{U_T} = q_S - q_{Dsat} + ln\left(\frac{q_S}{q_{Dsat}}\right).$$

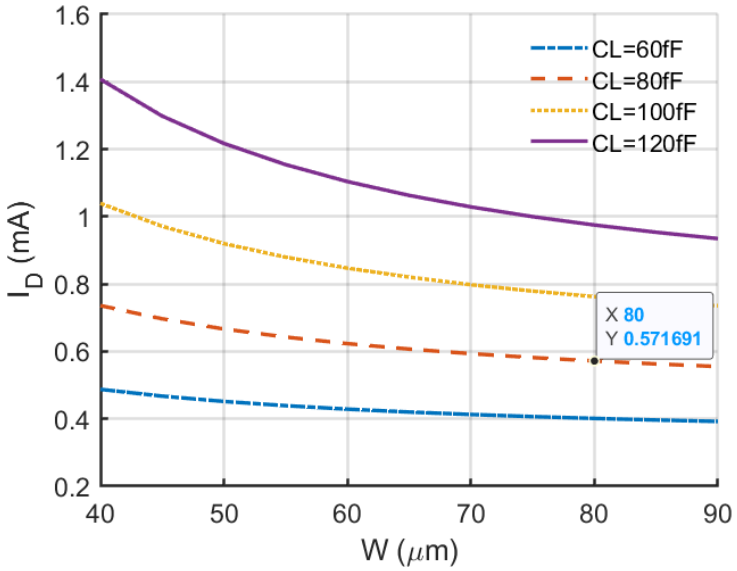
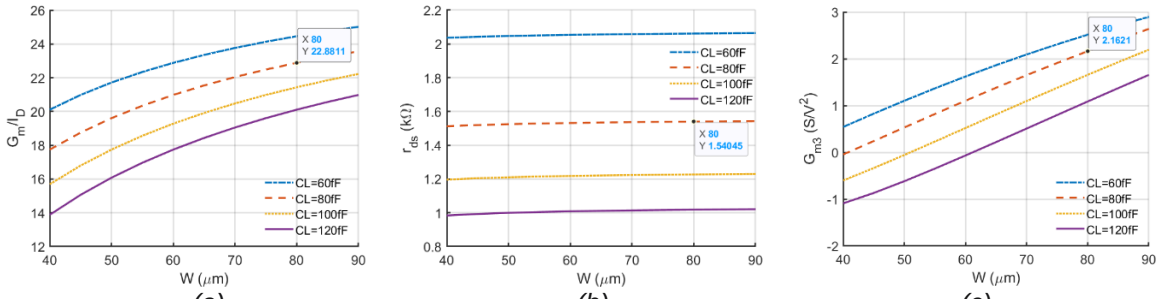


Figure 4-8. DC Current consumption, I_{DC} for different values of W and C_L.

As expected, increasing W allows to reduce the current consumption. This is the most significative variation among all the performances for high C_L. Here appears the most significant trade-off for the considered topology of R-Feedback: for a given gain and NF, improving the $IIP3$ by the mean of W or C_L will always leads to more consumption needed to keep a constant gain. In addition, Figure 4-8 shows how high is the impact of the output capacitance on the current consumption.

4.2.3.6 Additional features (g_{m3}, g_m/I_D)

To have a better insight, other features such as g_{m3} , r_{ds}, and g_m/I_D ratio can be drawn to observe their variation functions with respect to the circuit performances, and also to consider the energy efficiency in the circuit as is illustrated in Figure 4-9.



(a) (b) (c)

Figure 4-9. Main characteristics of the transistor to evaluate the design space in terms of W: (a) G_m/I_D, (b) r_{ds} and (c) G_{m3}.

As expected and discuss earlier, the drain efficiency (G_m/I_D) characteristic increases with W and decreases with C_L. The output resistance is constant over W and

increases with C_L since the inversion level increases to drive more current which increases the output conductance. Finally, in Figure 4-9(c), the sweet-spot can be observed which is consistent with the $IIP3$ curves shown in Figure 4-7.

To summarize this section, it is demonstrated that by combining R-feedback LNA electrical equations with the 7-parameter model it is possible to have a graphic representation of the design space, meaning all combination of performances that the circuit can reach with a given technology. This graphical representation enables to have an accurate portrayal of the different mechanisms driven LNA performances as well as possible trade-offs. In next section, this representation will be used to select the proper LNA sizing fulfilling the specifications.

4.3 From design space to practical case

Exploring the design space allows different trade-offs analysis. For example, for a high linear device, the designer shall enforce the output load. For a given output load of $80\ fF$ as it is the case for this design where a buffer is used for measurement purposes, a $W = 40\ \mu m$ shall be selected leading to a DC current of $I_D = 770\ \mu A$.

The circuit used to develop this method has been designed for IoT applications with the aim of lowering as much as possible the current consumption while maintaining the specification on NF and $IIP3$ given in Table 4-1 ($NF < 3\ dB$ and $IIP3 > -20\ dBm$). The chosen width is $W = 80\ \mu m$ leading to $I_D = 571\ \mu A$. All the LNA characteristics obtained during the design space exploration are marked on the different plots presented in the previous section and are summarized in Table 4-3.

Table 4-3. MOS operating point and circuits performances

q_S	$W\ (\mu m)$	$G_m\ (mS)$	$G_{DS}\ (mS)$	$C_L\ (fF)$	$G_T\ (dB)$	$I_{DC}\ (\mu A)$	$NF\ (dB)$	$IIP3\ (dBm)$
0.55	80	13.08	0.65	80	22.3	571.7	2.49	-19.33

Once W is chosen G_m, G_{DS} are determined and all the intermediate variables can be computed: R_F with (4-29), Q_{IN} with (4-30), Q_P with (4-15), R_P and C_P with (*4-7*) and (4-8). To end the design, the matching circuit must be sized. Knowing Q_P, the capacitance C'_{gs} added in parallel to C_{gs}, to reach the expected R_S, is computed with (4-11). Prior to that, knowing W, C_{gs} has to be evaluated. Finally, the imaginary part is null with L_g which is calculated with (4-10). The complete sizing of the circuit is presented in Table 4-4.

Table 4-4. Components for the Resistive feedback LNA for the chosen study case

$R_F\ (k\Omega)$	$R_L\ (k\Omega)$	$C'_{gs}\ (pF)$	$L_G\ (nH)$
1.6	1.4	1.31	14.9

The proposed design method is summarized in the following algorithm.

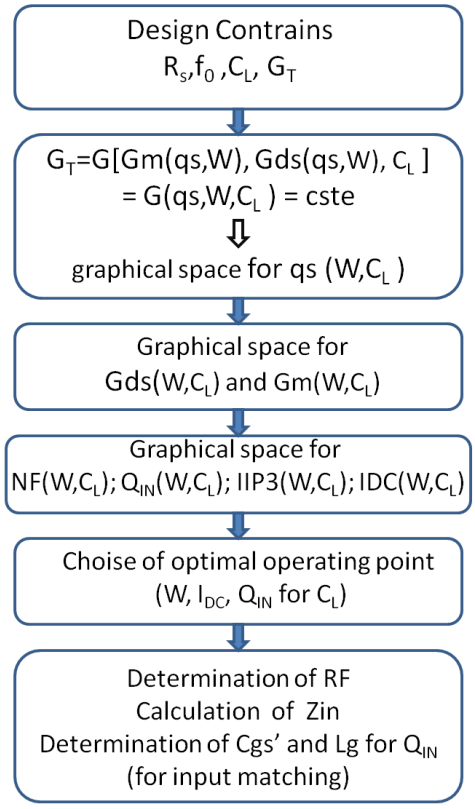


Figure 4-10. Algorithm for the exploration of the design space and calculation of the circuit components and biasing.

4.4 Simulation and measurement results

The R-feedback LNA was realized by Serge Subias (former research engineer at TIMA laboratory). The circuit, shown in Figure 4-11, embeds an output buffer composed of a 2 stages, common source and source follower amplifier. As mentioned, the buffer achieves a $80\ fF$ input capacitance mainly due to the parasitic capacitance of the $0.7\ pF$ input DC blocking capacitor and the C_{gs} of the common source. This capacitance value is introduced as C_L to run the design method.

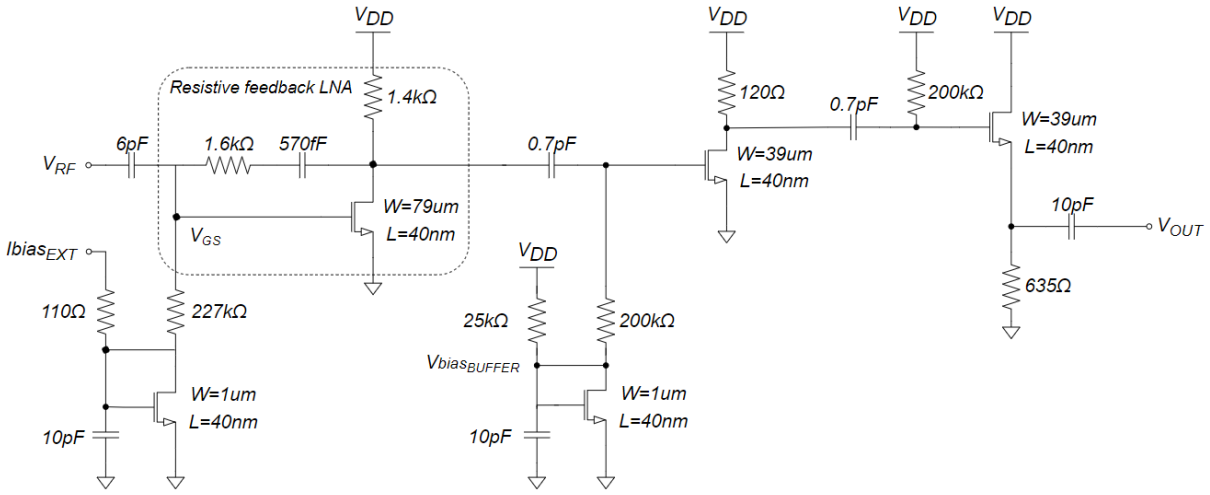


Figure 4-11. Schematic of the implemented circuit on silicon (TOP_LNA_2020 made by Serge Subias)

Simulation and measurement of the circuit are provided in Figure 4-12 and are summarized in Table 4-5. For measurement, the circuit has been biased at the nominal value of $I_D = 571.8\,\mu A$, closed to the simulated one.

In the same manner, the method has been tuned to provide the same current as in simulation which finally allows to do a comparison at constant DC current. As shown in Table 4-5, the measured and simulated total gain (LNA + Buffer) show a drop of about $1.16\,dB$ which remains in good agreement.

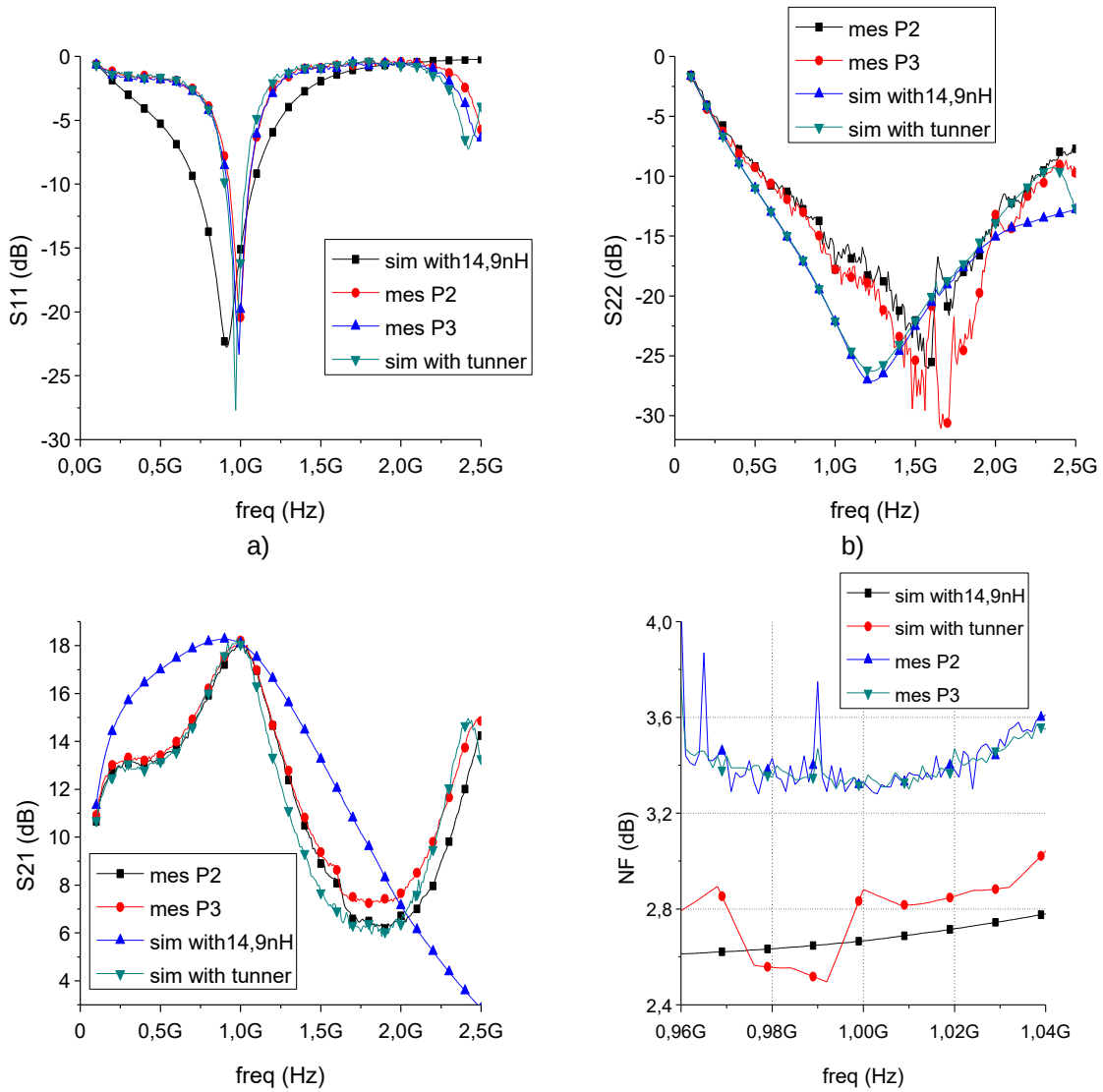
Knowing the buffer gain ($G_{BUFF} = -4\,dB$), G_T is estimated in measurement by subtracting the buffer gain to the LNA + Buffer gain. As shown in Table 4-5, G_T is in good agreement between, the method, the simulations and the measurement.

The noise factor is slightly higher in simulation ($2.6\,dB$ instead of $2.48\,dB$) and drop in measurement ($3.3\,dB$) certainly due to measurement imprecision. The $IIP3$ estimated by the method is also in good agreement with simulation. In measurement, the $IIP3$ of the LNA without buffer is not measured, but the $IIP3$ of LNA + Buffer are in good agreement between measure and simulation which confirm that the estimation of $IIP3$ is quite accurate with our model. Finally, the modified behavior on the frequency response in Figure 4-12, is due to the use of an impedance tuner (to measure the circuit at different operating frequencies) instead of two localized components L_g and C'_{gs}.

Table 4-5. Performance comparison for Matlab model and Virtuoso simulation for resistive feedback LNA at $f_0 = 1.8\ GHz$

Performance @ $f_0 = 1\ GHz$	$G_T\ (dB)$	$G_T + G_{buff}\ (dB)$	$NF\ (dB)$	$I_D\ (\mu A)$	$IIP3\ (dBm)$	$IIP3_{LNA+buff}\ (dBm)$
Model (Matlab)	22.3	NC	2.49	571.7	-19.07	NC
Virtuoso Simulation	22.96	19.46	2.6	572	-19.18	-25
Measurements	21.8#	18.3	3.3	570	NC	-24.86

#obtained by subtracting the -3.5 dB gain of the buffer.



c) d)

Figure 4-12. Simulation and measurement (2 samples: P2 & P3) of the R-Feedback LNA indifferent configuration (w/o impedance tuner). a) S11, b) S22, c) S21 and d) NF.

This exercise demonstrates that LNA performances predicted by our analytical method are very closed to the simulated ones using classical CAD tools. It demonstrates the accuracy of the proposed 7-parameter if it is used in the good inversion regime (weak or moderate inversion). Proceeding this way has two major advantages, no time-consuming design loops are needed and, having a good illustration of the trade-offs between all performances, guarantees to be on an optimal operating point.

4.5 Evaluation of the LNA performances under variation of the proposed model parameters of the MOS transistor

All along the development of the model and the design methodology, care has been taken to preserve the link with the physics. The purpose was to enable a process-design co-simulation flow. During this PhD, I was not able to go that far, but this chapter will show how the proposed model parameters impact the different performances of the LNA. This can be extracted from the flow, as it is available, and is enough to give indications to people developing technologies.

At least, two major fields of application can be enabled by this feature:

- Variability: If I want to keep gain, for example, in a given range, how many variations can I tolerate on MOS parameters?
- Optimization: If I want to have a better linearity, which parameter of the MOS transistors should I modify? In which direction? And what will be the collateral damages (if any)?

A variability study has been achieved using our analytical model. In this approach, performance variation is studied at constant current. In this scenario, a nominal $I_D = 578\ \mu A$ is. In the same manner as a relationship has been used between q_S and W for a constant G_T, a relationship between q_S and parameters of the model is used. To do so, the expression on the current from (*2-25*) which is recalled here for sake of clarity is used:

$$I_D = I_{S0}\left(1 + \frac{V_{DS} - V_{Dsat}}{V_E}\right)\frac{(q_S + q_{Dsat} + 2)(q_S - q_{Dsat})}{1 + \frac{\theta}{2}(q_S + q_{Dsat})}$$

with,

$$\frac{V_{DSsat}}{U_T} = q_S - q_{Dsat} + ln\left(\frac{q_S}{q_{Dsat}}\right)$$

and,

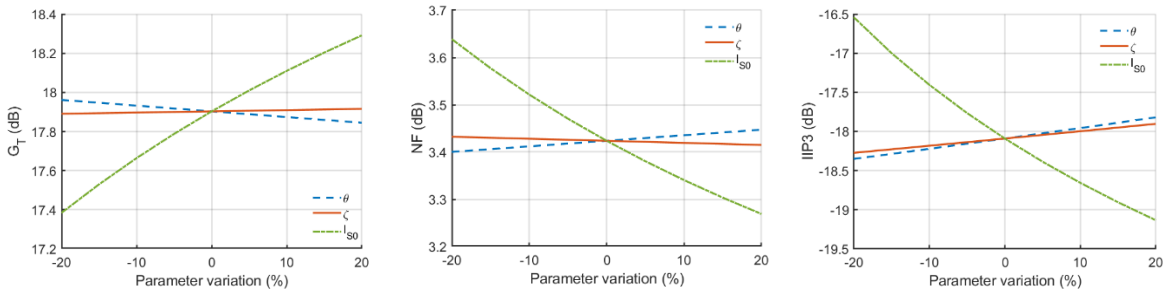
$$q_S = \frac{\theta}{2\zeta}q_{Dsat} - 1 + \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)}.$$

It clearly appears that I_D is directly dependent on θ, ζ and I_{S0} and the variability study is straightforward. Concerning the other parameters (n, V_{T0} and σ), they modify the current through the pinch-off voltage which is dependent on V_G. Such a dependency increases the complexity of the analysis and is not discussed here.

In this variability study, we choose to variate from +/-20% the value of the selected parameter of the model to visualize what are its impact on three of the main performances of the LNA: total voltage gain, G_T, noise figure, NF, and third order input interception point, $IIP3$. The results of this simulation are summarized in Figure 4-13.

Let's first point a limitation of this exercise. The choice of varying all parameters within +/-20% has been dictated by time constrains and can be misleading. When +/-20% of variability can be small (compared to actual variations in a given technology) it can be large for other parameters, making the comparison unfair. The analysis should be redone adjusting the exploration range for each parameter. Nevertheless, the analysis is interesting by itself, without focusing too much on the conclusions.

At first glance, as shown in Figure 4-13, the parameter that have a major impact on the set of the LNA performances is the specific current, I_{S0}, whereas the variation of the carrier velocity saturation and the carrier mobility reduction parameters, ζ and θ, have much less impact on the LNA performances.



(a) (b) (c)

Figure 4-13. Impact of the variation of some parameters (θ, ζ and I_{S0}) of the 7-parameter model on the Resistive feedback LNA performances: (a)G_T, (b)NF and (c)$IIP3$.

As illustrated in Figure 4-13 , 40% variation of I_{S0} leads to 2 dB variation on the G_T, 3 dB variation on $IIP3$ and 0.4 dB variation on NF. Increasing I_{S0} increases the G_m leading to an augmentation of the gain and an $IIP3$ and a NF reduction, showing how the main characteristics of the LNA are sensitive to this parameter. Increasing ζ leads a gain that remains quite constant while the $IIP3$ and the NF are little improved. Concerning θ, the study shows a little degradation of the performances when increasing its value.

In conclusion for this exercise, it has been demonstrated that, on top of finding the right part values of a R-feedback LNA to fulfill a given set of specifications, the methodology based on the 7-parameter model enables to provide LNA performances sensitivity with respect to MOS parameters opening the capability of design-process co-optimization.

4.6 Conclusion and perspectives on the design methodology proposition

This chapter demonstrates that the 7-parameter model, presented in Chapter 2:, is suited to be used in a design methodology enabling technology-circuit co-optimization.

Several tools, based on Matlab implementation of the 7-parameter model, were presented and illustrated with a R-feedback LNA. Initially, the characteristics of this topology were presented as well as its main equations to estimate the most relevant performances expressed in terms of the MOS equivalent model. In a next step, we presented a way to relate these equations to the parameters of the 7-parameter model and thus, a proposal was made on how to set up a design space graphic representation. Finally, a design (set of component values and biasing condition) has been determined using the design space representation to find the optimal operating point corresponding to the specifications. Then the measurements on R-feedback LNA previously implemented in silicon were compared with the results obtained both

through the proposed Matlab model and those obtained thanks to a simulation using the PDK of the 28nm FD-SOI technology in Cadence framework.

As the results obtained with our methodology are very close to the Cadence simulated ones and the measurements; it validates that our methodology is an excellent methodology to design an LNA, while having a visual representation of the different trade-offs. This analytical methodology, that will require to manipulate equations by making models, much simpler, but with a smaller coverage of the operating region and regime, or by breaking the link between technology and model to be able to reduce the number of parameters. It should be noted that without the help of the new model proposed in the previous chapters, it would not have been possible to consider the non-linear characteristics of the transistor within the circuit performances, which allowed to estimate an $IIP3$ quite close to what was obtained both in simulation and in measurements and which constitute a major contribution regarding actual state of the art.

Finally, a very brief section was also presented in which we try to represent how the variation of a parameter of the model can be fundamental to reach a certain required performance, however this carries with it a corresponding variation of the characteristics with which we can have a trade-off, and this only allows us to give some clues on how to implement the model and the design methodologies to find the most optimal technologies depending on the performance to be achieved in a given circuit. This study must be completed, with a study of the n, V_{T0} and σ and a more realistic variation range for each parameter, so that the sensibility results become more representative of the actual context.

Of course, the work done here has to be pushed in different directions. The methodology developed here for the R-feedback LNA can be generalized to other type of LNAs, in a first place and to other type of blocks. When moving from R-feedback LNA to other types of LNA will be straightforward, going to other blocks may reveals novel challenges.

Blocks exhibiting strong non-linearities (such as PA, VCO or Mixers) will require more complex analytical tools to put all performances in equation.

Regarding the model, as pointed in Chapter 3, the model of capacitances, valid in all operation regime and regions has not been developed. In the R-feedback LNA we see this limitation in the discrepancy of f_{max}, but with a very limited impact. For strongly non-linear functions, and especially the VCO where capacitance is fundamental to calculate the frequency, this will become a severe limitation.

Chapter 5: Conclusions and perspectives

5.1 General conclusions

With the reduction of supply voltage that comes along with the recent advances in the technology nodes roadmap, MOS transistor operation in weak and moderate inversion regimes appears to be really interesting for low power RF circuit design. This trend has led to the development of design methodologies focusing on the inversion coefficient (IC) or the g_m/I_D characteristic of MOS transistor to find the best operating point for a given application.

These methodologies rely on a rather simple description of the MOS transistor electrical behavior, generally limited to a fixed V_D value and a very simplified bias dependence on V_G. As a result, the models used prevent from studying non-linearities or account for V_D dependence of Short Channel Effects (SCE), which are dominating the transistor performances in advance CMOS technology nodes.

Therefore, the first goal of this PhD work was to derive an improved inversion charge-based model, combining all the features mentioned above, and thus able to accurately reproduce the I-V characteristics and their derivatives with respect to both, V_G and V_D. Such a model will not only allow DC and small-signal analysis, but also will open the way to circuit non-linearities optimization, and subsequently improve the RF circuit design methodology accordingly.

Finally, care was taken to keep the model parameter meaningful, in terms of physical effects. The purpose here was to allow, through this model, a communication between circuit designers and process developers, that can be further pushed up to a circuit-technology co-design.

To do so, the main physical effects involved in the SCE of the MOS transistor and their V_D dependence were determined and modeled. This drastically improved the estimation of the partial current derivatives, especially g_m, g_{m2}, g_{m3} and g_{ds}, as demonstrated by the comparison of the simulations with the measurements performed on a 28nm FD-SOI technology. This technology was used because it represents the modern technologies used in low power context and all transistors' measured characteristics were available.

The proposed model has its basis on the 3-parameter model based on the inversion level of the MOS transistor whose parameters are: the specific current, $\mathrm{I_{S0}}$, the subthreshold slope factor, n, and the subthreshold voltage, V_{T0}. This model is appropriate to describe all DC operation regions of a long channel transistor but

requires some additional parameters to consider the dependence on V_{D} and the SCE. So, the effects of the Drain-Induced Barrier Lowering (DIBL) and the Channel Length Modulation (CLM) are essential to model the V_{D} dependence. The former specially to model the drain current in weak and moderate inversion regimes and the latter to improve the accuracy of the $\mathrm{I}_{\mathrm{D}}(V_{\mathrm{D}})$ characteristic curve.

Additionally, to improve the modeling in saturation and strong inversion regime, the effect of the carrier velocity saturation has to be considered as demonstrated previously in the literature.

With only six parameters, the proposed model can capture all the main effects involving a V_D dependence. However, in order to also improve the V_G dependence, especially in linear region, a seventh parameter has been introduced to implement the carrier mobility reduction effect.

It should be noted here that the task of studying the physical effects of the transistor and modeling them in a simple and analytical way took more time than initially foreseen, leaving less time to the development and assessment of the associated design methodology. However, very satisfactory results have been obtained on the simulation of the MOS transistor I-V curves and its derivatives, providing a solid basis to the proposed approach.

It was also shown that the model is valid for different transistor lengths, which allows the model to be used for the device sizing and biasing in a circuit design methodology. In this regard, we developed a design methodology for a simple case study, consisting in a resistive feedback LNA, taking advantage of previous work on this circuit in our research team.

In a first step of the design methodology a circuit study leads to establish a relationship between the LNA performances and the small signal parameters of the active and passive components. In a second step, using MOS model equations, a relationship between the small signal parameters of the MOS and its sizing and biasing is performed. This leads a graphical exploration of the design space linking LNA performances to transistor sizing and biasing and passive component values. Doing so, this methodology demonstrates the possibility of determining an optimum design point depending on the targeted specifications.

To go further and compare simulations with the proposed model to measurements, a specific design space point corresponding to a real circuit implementation in silicon has been reproduced.

As a result, it was not only possible to compare the proposed model to a transistor-level electrical simulation, but also to carry out a comparison with actual measurements, proving that the model results were very similar to those obtained with both simulation and measurements.

Summarizing, the main contributions of this work are: a) the proposal of a 7-parameter model, with a limited set of equations and parameters to be used in analytical design methodology; and b) developing such design methodology, demonstrating this way that this model was accurate enough to optimize and predict the performances of a resistive feedback LNA. Moreover, our work demonstrates that keeping the link between the model parameters and physical mechanisms open the way to circuit technology co-design.

Finally, the sensitivity analysis performed in chapter 4.5 can bring a lot of useful information for technology optimization. Looking at the result, it becomes obvious what parameters are important to preserve the performances of the LNA and thus, how the technology must be defined to fulfill a set of specifications.

An obvious usage is to be able to control LNA performance variability by controlling device parameters variability, either by putting constraints in the manufacturing chain or by control on manufactured wafers.

5.2 Perspectives

Looking back and with the knowledge I have acquired over time about the model proposal that was made, I would consider the model differently in several aspects:

- Considering the short-channel effects, a model simplification may be considered for very short-channel transistors where there is no real need for the parameter related to the Channel Length Modulation (CLM), V_E. Indeed, as demonstrated previously in section 2.5.2 , the CLM effect is overshadowed by the DIBL effect for this type of devices. However, if relaxed gate lengths are considered, CLM may help to capture output conductance in saturation region.
- I would perform a different modeling of the current considering the different models of carrier velocity saturation proposed by Mangla in [32], where instead of using equation (2-25), I would use a more precise estimation by using (5-1). This would lead to a better estimation of the current derivatives in linear or saturation regions of operation considering both effects, carrier saturation velocity and carrier mobility reduction, play an important role in the direct definition of the drain current.

$$I_D = \left(1 + \frac{V_{DS} - V'_{DS}}{V_E}\right) \frac{I_{S0}(q_S + q'_D + 2)(q_S - q'_D)}{1 + \frac{\theta}{2}(q_S + q'_D)}. \qquad (2\text{-}25)$$

$$I_D = \left(1 + \frac{V_{DS} - V'_{DS}}{V_E}\right) \frac{I_{S0}(q_S + q'_D + 2)(q_S - q'_D)}{1 + \frac{\theta}{2}(q_S + q'_D) + \zeta(q_S - q'_D)}. \quad (5\text{-}1)$$

- Finally, I would say that to further improve the model for this technology and to go beyond of the presented application, aspects such as the intrinsic capacitance modeling, the back-bias voltage and the temperature modeling should be considered. Scalability over gate length is also an aspect that I did not address but can be useful in other contexts.
- Obviously, the question of the number of parameters to describe the model is still open. In other words, what is the optimum balance between accuracy and capacity of the model to be used in an analytical design methodology. On the accuracy aspect, the simplified model cannot compete with a compact model, implemented in the simulation tools, which thanks to it hundreds of parameters provides a good accuracy in any situation. Nevertheless, compact model is not a solution for analytical circuit calculations and optimization. On the other hand, the proposed 7-parameter model opens the way to hand calculations without sacrificing too much accuracy neither limiting operation region. Anyways, because 7-parameter model is still complex, hand calculations will not be that easy to perform and probably the way forward will be to create simpler models. By limiting the domain of application (operation regions and domains, technology, etc.) it is possible to simplify the 7-parameter model equations (or even the number of parameters) to come to a much simpler model easy to manipulate suited for a certain application.

Now, focusing on the aspect of the design methodology proposal:

- Considering the study case of the resistive feedback LNA, almost all the performances of the circuit can be calculated after fixing a targeted performance, in the presented case, the total gain of the LNA. The designer must decide over the trade-offs and the performance that have to be prioritized. In further design methodologies would be convenient to provide some tools to consider process variations, for example, to give some hints to the designers about the possible achievement on the targeted specifications in their circuit design.
- To consolidate this model-based design methodology, other LNA topologies or even other types of circuits should be explored to have

clarity on the aspects that should be optimized and improved at general level.

The work carried out in this PhD project will be continued thanks to at least two PhD thesis that has already begun in our research group:

- The work of Khalil Bouchoucha, where a simplification of the model is made according to its application for a multimode LNA and where a parameter modeling the body-bias voltage (V_{BB}) has been added to the model.
- The work of Julien Poupon, aiming to develop a design methodology for VCO using a charge-based model including the transistor intrinsic capacitances modeling.

Work spreading

Throughout the three years of my PhD thesis, I had the opportunity to present my work through some presentations or publications listed below and giving to the scientific community for knowledge.

Journal publications:

- **D. A. Pino-Monroy**, P. Scheer, M. K. Bouchoucha, C. Galup-Montoro, M. J. Barragan, P. Cathelin, J.-M. Fournier, A. Cathelin, and S. Bourdel,"Design-Oriented All-Regime All-Region 7-Parameter Short-Channel MOSFET Model Based on Inversion Charge," *IEEE Access*, vol. 10, p. 16, 2022.
- **D. A. Pino-Monroy**, M. K. Bouchoucha, P. Cathelin, M. J. Barragan, P. Scheer, J.-M. Fournier, A. Cathelin, and S. Bourdel, "Design Methodology for RF LNA using Charge-Based Model Accounting for Non-Linearity," *in writing* status.

International conferences:

- A. Al Shakoush, S. Ibrahim, S. Subias, F. Podevin, M. J. Barragan, **D. A. Pino-Monroy**, I. Bendjeddou, E. Lauga-Larroze, L. Fesquet, T. Taris, and S. Bourdel, "N-Path Mixer with Wide Rejection Including the 7th Harmonic for Low Power Multi-standard Receivers," pp. 256-260, 2022 20th IEEE Interregional NEWCAS Conference (NEWCAS), Quebec City, QC, Canada, 2022.
- **D. A. Pino-Monroy**, P. Scheer, M. K. Bouchoucha, C. Galup-Montoro, M. J. Barragan, P. Cathelin, J.-M. Fournier, A. Cathelin, and S. Bourdel, "Design-Oriented model for short-channel MOS transistors based on inversion charge," p. 4, accepted for 2023 IEEE PhD Research in Microelectronics and Electronics Conference in Latin America (PRIME-LA) and to be presented end February 2023 in Quito, Ecuador.
- M. K. Bouchoucha, **D. A. Pino Monroy**, P. Scheer, P. Cathelin, J. M. Fournier, M. J. Barragan, A. Cathelin, and S. Bourdel, "Resistive Feedback LNA Design Using a 7-Parameter Design-Oriented Model for Advanced Technologies," p. 5, accepted for 2023 IEEE International

Symposium on Circuits & Systems (ISCAS) and to be presented end May 2023 in Monterey, California, USA.

Workshops:

- 7-parameter model in Joint IEEE & SoC² Day on Inversion Coefficient & RF Low Power, 12 October 2021, Grenoble.

PhD days presentations:

- 7-parameter model in ST iDNA Innovation PhD's days, 15 October 2021, Crolles.
- 7-parameter model in TIMA PhD's days (180 seconds), 18 November 2021, Grenoble.
- 7-parameter model and the proposed design methodology in ST iDNA Innovation PhD's days, 18 October 2022, Crolles.
- 7-parameter model and the proposed design methodology in TIMA PhD's days (180 seconds), 25 November 2022, Grenoble.

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Appendices

A.1 Deduction of equations and calculation of current derivatives

A.1.1 Relation between q_S and q_{Dsat}

For (2-19)

$$q_S = \frac{\theta}{2\zeta} q_{Dsat} - 1 + \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)} \quad \text{(A.1.1-1)}$$

From (2-18) we have,

$$\frac{2}{\zeta} q_{Dsat} = \frac{(q_S + q_{Dsat} + 2)(q_S - q_{Dsat})}{1 + \theta\left(\frac{q_S + q_{Dsat}}{2}\right)} \quad \text{(A.1.1-2)}$$

By rearranging the terms, we have,

$$q_S^2 + q_S\left(2 - \frac{\theta}{\zeta} q_{Dsat}\right) - q_{Dsat}\left(2 + \frac{2}{\zeta}\right) - q_{Dsat}^2\left(1 + \frac{\theta}{\zeta}\right) = 0 \quad \text{(A.1.1-3)}$$

And solving for q_S, we get,

$$q_S = \frac{\theta}{2\zeta} q_{Dsat} - 1 + \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)} \quad \text{(A.1.1-4)}$$

A.1.2 Calculation of the drain current derivatives

A.1.2.1 Current derivative with respect to any voltage

For (2-26)

$$\frac{\partial i_d}{\partial v_x} = \frac{1}{B}\left[\left(2 + 2q_S - \frac{\theta}{2} i_d\right)\frac{\partial q_S}{\partial v_X} - \left(2 + 2q_D + \frac{\theta}{2} i_d\right)\frac{\partial q_D}{\partial v_X}\right] \quad \text{(A.1.2-1)}$$

From (2-12)

$$i_d = \frac{I_D}{I_{S0}} = \frac{(q_S - q_D)(q_S + q_D + 2)}{1 + \theta\left(\frac{q_s + q_D}{2}\right)} \tag{A.1.2-2}$$

If

$$D = (q_S - q_D)(q_S + q_D + 2) = q_S^2 + 2q_s - q_D^2 - 2q_D \tag{A.1.2-3}$$

And

$$E = 1 + \theta\left(\frac{q_S + q_D}{2}\right), \tag{A.1.2-4}$$

Therefore,

$$i_d = \frac{D}{\mathrm{E}}. \tag{A.1.2-5}$$

So,

$$\frac{\partial i_d}{\partial v_x} = \frac{\partial D}{\partial v_x}\frac{1}{E} - \frac{D}{E^2}\frac{\partial E}{\partial v_x} = \frac{1}{E}\left(\frac{\partial D}{\partial v_x} - \frac{D}{E}\frac{\partial E}{\partial v_x}\right) = \frac{1}{E}\left(\frac{\partial D}{\partial v_x} - i_d\frac{\partial E}{\partial v_x}\right) \tag{A.1.2-6}$$

And,

$$\frac{\partial D}{\partial v_x} = 2(1 + q_S)\frac{\partial q_S}{\partial v_x} - 2(1 + q_D)\frac{\partial q_D}{\partial v_x} \tag{A.1.2-7}$$

$$\frac{\partial E}{\partial v_x} = \frac{\theta}{2}\left(\frac{\partial q_S}{\partial v_x} + \frac{\partial q_D}{\partial v_x}\right) \tag{A.1.2-8}$$

Therefore,

$$\frac{\partial i_d}{\partial v_x} = \frac{1}{E}\left(2(1 + q_S)\frac{\partial q_S}{\partial v_x} - 2(1 + q_D)\frac{\partial q_D}{\partial v_x} - i_d\frac{\theta}{2}\left(\frac{\partial q_S}{\partial v_x} + \frac{\partial q_D}{\partial v_x}\right)\right) \tag{A.1.2-9}$$

Arranging the terms, we get (2-26)

$$\frac{\partial i_d}{\partial v_x} = \frac{1}{B}\left[\left(2 + 2q_S - \frac{\theta}{2} i_d\right)\frac{\partial q_S}{\partial v_x} - \left(2 + 2q_D + \frac{\theta}{2} i_d\right)\frac{\partial q_D}{\partial v_x}\right]. \quad \text{(A.1.2-10)}$$

A.1.2.2 Drain and source charges derivatives with respect to any voltage

For (2-28)

$$\frac{\partial q_{S(D)}}{\partial v_g} = \frac{1}{n}\frac{q_{S(D)}}{q_{S(D)} + 1} \quad \text{(A.1.2-11)}$$

We use (2-9) or (2-10), depending on the desired derivative (q_S or q_D) and (2-14):

$$V_P - V_S = U_T(q_S - 1 + ln(q_S)), \quad \text{(A.1.2-12)}$$

$$V_P - V_D = U_T(q_D - 1 + ln(q_D)). \quad \text{(A.1.2-13)}$$

$$V_P \approx \frac{V_G - V_{T0} + \sigma(V_D + V_S)}{n}. \quad \text{(A.1.2-14)}$$

So,

$$V_G = nV_P + V_{T0} - \sigma(V_D + V_S), \quad \text{(A.1.2-15)}$$

In terms of q_S,

$$V_G = nU_T(q_S - 1 + ln(q_S)) + nV_S + V_{T0} - \sigma(V_D + V_S) \quad \text{(A.1.2-16)}$$

Normalizing respect to U_T,

$$v_g = n(q_S - 1 + ln(q_S)) + nv_s + V_{T0}/U_T - \sigma(v_d + v_s) \quad \text{(A.1.2-17)}$$

The derivative of v_g respect to q_S , for a given V_D and V_S is:

$$\frac{\partial v_g}{\partial q_S} = n\left(1 + \frac{1}{q_S}\right) = n\frac{q_S + 1}{q_S}. \quad \text{(A.1.2-18)}$$

As equations (A.1.2-12) and (A.1.2-13), are equivalent depending on the terminal, the derivative of v_g respect to q_D can be derived following the procedure shown for q_S, giving:

$$\frac{\partial v_g}{\partial q_D} = n\left(1 + \frac{1}{q_D}\right) = n\frac{q_D + 1}{q_D} \ . \tag{A.1.2-19}$$

A.1.2.3 Deduction of the complete current derivatives

For (2-29), (2-30), (2-31) and (2-32):

$$\frac{\partial q_D}{\partial v_d} = \left(1 - \frac{\sigma}{n}\right)\frac{q_D}{q_D + 1}, \tag{A.1.2-20}$$

$$\frac{\partial q_S}{\partial v_d} = \frac{\sigma}{n}\frac{q_S}{q_S + 1}, \tag{A.1.2-21}$$

$$\frac{\partial q_D}{\partial v_s} = \frac{\sigma}{n}\frac{q_D}{q_D + 1}, \tag{A.1.2-22}$$

$$\frac{\partial q_S}{\partial v_s} = \left(1 - \frac{\sigma}{n}\right)\frac{q_S}{q_S + 1}. \tag{A.1.2-23}$$

We use again equations (A.1.2-12), (A.1.2-13) and (A.1.2-14)

$$v_g - \frac{V_{T0}}{U_T} + \sigma v_d + \sigma v_s - v_s = n(q_S - 1 + ln(q_S)) \tag{A.1.2-24}$$

$$v_g - \frac{V_{T0}}{U_T} + \sigma v_d + \sigma v_s - v_d = n(q_D - 1 + ln(q_D)) \tag{A.1.2-25}$$

Therefore,

$$\frac{\partial v_d}{\partial q_S} = \frac{n}{\sigma}\left(1 + \frac{1}{q_S}\right) = \frac{n}{\sigma}\frac{q_S + 1}{q_S} \tag{A.1.2-26}$$

$$\frac{\partial v_d}{\partial q_D} = \left(\frac{n}{n - \sigma}\right)\frac{q_D + 1}{q_D} \tag{A.1.2-27}$$

$$\frac{\partial v_s}{\partial q_S} = \left(\frac{n}{n - \sigma}\right)\frac{q_S + 1}{q_S} \tag{A.1.2-28}$$

$$\frac{\partial v_s}{\partial q_D} = \frac{n}{\sigma}\frac{q_D + 1}{q_D} \tag{A.1.2-29}$$

For (2-33)

$$g_m = \frac{\partial i_d}{\partial v_g} = \frac{2}{nB}\left[q_S - q_D - i_d\frac{\theta}{4}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right)\right]. \quad \text{(A.1.2-30)}$$

We replace (A.1.2-11) on (A.1.2-10)

$$\frac{\partial q_{S(D)}}{\partial v_g} = \frac{1}{n}\frac{q_{S(D)}}{q_{S(D)}+1}, \quad \text{(A.1.2-31)}$$

$$\frac{\partial i_d}{\partial v_x} = \frac{1}{B}\left[\left(2 + 2q_S - \frac{\theta}{2}i_d\right)\frac{\partial q_S}{\partial v_x} - \left(2 + 2q_D + \frac{\theta}{2}i_d\right)\frac{\partial q_D}{\partial v_x}\right], \quad \text{(A.1.2-32)}$$

For (2-34), (2-35), (2-36) and (2-37) the same procedure of the derivative on (A.1.2-10)

$$g_{m2} = \frac{2}{n^2 B}\left[\frac{q_S}{1+q_S} - \frac{q_D}{1+q_D} - \frac{\theta}{4}\left[2ng_m\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + i_d\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right)\right]\right]. \quad \text{(A.1.2-33)}$$

$$g_{m3} = \frac{2}{n^3 B}\left[\frac{q_S}{(1+q_S)^3} - \frac{q_D}{(1+q_D)^3} - \frac{\theta}{4}\left[3n^2 g_{m2}\left(\frac{q_S}{1+q_S} + \frac{q_D}{1+q_D}\right) + 3ng_m\left(\frac{q_S}{(1+q_S)^3} + \frac{q_D}{(1+q_D)^3}\right) + i_d\left(\frac{q_S(1-2q_S)}{(1+q_S)^5} + \frac{q_D(1-2q_D)}{(1+q_D)^5}\right)\right]\right]. \quad \text{(A.1.2-34)}$$

$$g_d = \frac{\partial i_d}{\partial v_d} = \frac{2}{B}\left[\frac{\sigma}{n}q_S - \left(\frac{\sigma}{n} - 1\right)q_D - i_d\frac{\theta}{4}\left(\frac{\sigma}{n}\frac{q_S}{1+q_S} + \left(\frac{\sigma}{n} - 1\right)\frac{q_D}{1+q_D}\right)\right]. \quad \text{(A.1.2-35)}$$

$$\frac{\partial i_{dsat}}{\partial v_x} = \frac{\partial i_{dsat}}{\partial q_S}\frac{\partial q_S}{\partial v_x} = 2\frac{E}{D + \frac{\theta}{2}E}\frac{\partial q_S}{\partial V_x}. \quad \text{(A.1.2-36)}$$

$$D = 1 + \zeta - \frac{\theta}{2} + q_{Dsat}\left(\zeta + \theta + \frac{\theta^2}{2\zeta}\right), \quad \text{(A.1.2-37)}$$

$$E = \sqrt{1 + q_{Dsat}\left(2 + \frac{2}{\zeta} - \frac{\theta}{\zeta}\right) + q_{Dsat}^2\left(1 + \frac{\theta}{\zeta} + \frac{\theta^2}{4\zeta^2}\right)}. \qquad \text{(A.1.2-38)}$$

A.2 MATLAB codes

A.2.1 Drain current and its derivatives as function of the gate voltage

The function implemented in Matlab to calculate the current and their partial derivatives in terms of the variation of V_G is the following:

```
function [ID, gm, gm2, gm3]=model_7param(T,n,Is0,vt0,sigma,zeta,ve,theta,VG,vd,vs)

    k=1.38e-23;
    q=1.602e-19;
    ut=k*T/q;

  for g=1:length(VG)
   for d=1:length(vd)
    vp=(VG(g)-vt0+sigma*vd(d))/n;
    vds=vd(d)-vs;

    syms qs_sym
    eq1=(vp-vs)/ut==qs_sym-1+log(qs_sym);

    syms idsat_sy
    eq2=qs_sym==-1+theta*idsat_sym/4+sqrt(1+idsat_sym*(zeta+1-
theta/2)+zeta^2*idsat_sym^2/4*(1+theta/zeta+theta^2/(4*zeta^2)));

    [qs_eq,idsat_eq]=solve([eq1,eq2],[qs_sym,idsat_sym],'PrincipalValue',true);
    qs(g)=double(qs_eq);
    idsat=double(idsat_eq);
    qdsat(g)=zeta*idsat/2;
    vdssat=ut*(qs(g)-qdsat(g)+log(qs(g)/qdsat(g)));


    vds_p=vds/((1+(vds/vdssat)^4))^(1/4);
    vd_p=vds_p+vs;

    Is=Is0*(1+(vds-vds_p)/ve);

    syms qd_sym
    eq3=(vp-vd(d))/ut==qd_sym-1+log(qd_sym);
    qd_eq=solve(eq3,qd_sym);
    qd(g)=double(qd_eq);

    syms qd_p_sym
```

```
    eq4=(vp-vd_p)/ut==qd_p_sym-1+log(qd_p_sym);
    qd_p_eq=solve(eq4,qd_p_sym);
    qd_p(g)=double(qd_p_eq);

    ID(g,d)=Is*(qs(g)-qd_p(g))*(qs(g)+qd_p(g)+2)/(1+theta*(qs(g)+qd_p(g))/2);

    id(g,d)=ID(g,d)./Is0;
    B=1+theta*(qs(g)+qd(g))/2;
    A=qs(g)/(1+qs(g))^3-qd(g)/(1+qd(g))^3;
    C=qs(g)/(1+qs(g))+qd(g)/(1+qd(g));
    D=qs(g)/(1+qs(g))^3+qd(g)/(1+qd(g))^3;
    E=qs(g)*(1-2*qs(g))/(1+qs(g))^5+qd(g)*(1-2*qd(g))/(1+qd(g))^5;


    % Expressions of gm in linear normalized
    gm(g,d)=2*(qs(g)-qd(g)-id(g,d)*theta*(qs(g)/(1+qs(g))+(qd(g)/(1+qd(g))))/4)/B;
    gm2(g,d)=2*(qs(g)/(1+qs(g))-(qd(g)/(1+qd(g)))-
theta*(2*gm(g,d)*(qs(g)/(1+qs(g))+(qd(g)/(1+qd(g))))+id(g,d)*(qs(g)/(1+qs(g))^3+(qd(g)/(1+
qd(g))^3)))/4)/B;
    gm3(g,d)=2*(A-theta*(3*gm2(g,d)*C+3*gm(g,d)*D+id(g,d)*E)/4)/B;

  end
 end
end
```

A.2.2 Drain current and its derivatives as function of the drain voltage

The function implemented in Matlab to calculate the drain current and the partial derivative with respect to the variation of V_D is the following:

```
function [ID, gd]=model_7param_vd(T,n,Is0,vt0,sigma,zeta,ve,theta,VG,vd,vs)

    k=1.38e-23;
    q=1.602e-19;
    ut=k*T/q;

  for g=1:length(VG)
   for d=1:length(vd)
    vp=(VG(g)-vt0+sigma*vd(d))/n;
    vds=vd(d)-vs;

    syms qs_sym
    eq1=(vp-vs)/ut==qs_sym-1+log(qs_sym);

    syms idsat_sym
    eq2=qs_sym==-1+theta*idsat_sym/4+sqrt(1+idsat_sym*(zeta+1-
theta/2)+zeta^2*idsat_sym^2/4*(1+theta/zeta+theta^2/(4*zeta^2)));

    [qs_eq,idsat_eq]=solve([eq1,eq2],[qs_sym,idsat_sym],'PrincipalValue',true);
```

```
        qs(g)=double(qs_eq);
        idsat=double(idsat_eq);
        qdsat(g)=zeta*idsat/2;
        vdssat=ut*(qs(g)-qdsat(g)+log(qs(g)/qdsat(g)));

        vds_p=vds/((1+(vds/vdssat)^4))^(1/4);
        vd_p=vds_p+vs;

        Is=Is0*(1+(vds-vds_p)/ve);

        syms qd_sym
        eq3=(vp-vd(d))/ut==qd_sym-1+log(qd_sym);
        qd_eq=solve(eq3,qd_sym);
        qd(g)=double(qd_eq);

        syms qd_p_sym
        eq4=(vp-vd_p)/ut==qd_p_sym-1+log(qd_p_sym);
        qd_p_eq=solve(eq4,qd_p_sym);
        qd_p(g)=double(qd_p_eq);

        ID(g,d)=Is*(qs(g)-qd_p(g))*(qs(g)+qd_p(g)+2)/(1+theta*(qs(g)+qd_p(g))/2);
        IDsat(g,d)=Is*idsat;

        id(g,d)=ID(g,d)./Is;
        B=1+theta*(qs(g)+qd(g))/2;

        % Expression of gd in linear normalized
        gd(g,d)=2*(sigma*qs(g)/n-(sigma/n-1)*qd(g)-
id(g,d)*theta*((sigma/n)*qs(g)/(1+qs(g))+(sigma/n-1)*(qd(g)/(1+qd(g))))/4)/B;

      end
    end
  end
```

A.3 Resistive feedback noise factor calculation

A.3.1 Elements for noise calculation: Gain and Input matching

A.3.1.1 Intrinsic voltage Gain

We recall the voltage gain of the R-feedback LNA core without the input matching:

$$G_V = \frac{V_{OUT}}{V_{GS}} = -\frac{(G_m R_F - 1) R_{out}}{R_{out} + R_F} \qquad \text{(A.3.1-1)}$$

with

$$R_{out} = r_{ds}||R_L\ . \tag{A.3.1-2}$$

A.3.1.2 Miller impedance

The input impedance in parallel with C_{gs} corresponds to:

$$R_P = \frac{R_F}{1 + |G_V|} = \frac{R_{out} + R_F}{1 + G_m\ R_{out}} \tag{A.3.1-3}$$

A.3.1.3 Transformation parallel/series at the input

The series input impedance can be transformed to its equivalent in parallel (Figure A.3.1-1) as:

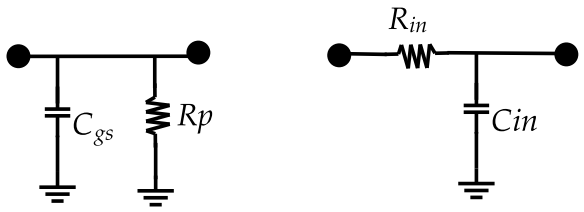
$$\Re(Z_{in}) \triangleq R_{in} = \frac{R_P}{1 + Q_P^2} \tag{A.3.1-4}$$

and

$$C_{in} = C_{gs}\frac{1 + Q_P^2}{Q_P^2}, \tag{A.3.1-5}$$

with

$$Q_P = R_P C_{gs}\omega_0 = \frac{1}{R_{in}C_{in}\omega_0}. \tag{A.3.1-6}$$



(a) *(b)*

Figure A.3.1-1. Input impedance a) in parallel and b) in series

A.3.1.4 Input matching at operation frequency

Considering the input series network, requires an inductance, L_g, to null the imaginary part of the input impedance:

$$L_g C_{in} \omega_0^2 = 1\,. \tag{A.3.1-7}$$

Or, in parallel:

$$L_g C_{gs} \frac{1 + Q_P^2}{Q_P^2} \omega_0^2 = 1\,. \tag{A.3.1-8}$$

Therefore,

$$L_g C_{gs} \omega_0^2 = \frac{Q_P^2}{1 + Q_P^2}\,. \tag{A.3.1-9}$$

A.3.1.5 Passive amplifying coefficient from input matching network

The passive network matching provides an overvoltage coefficient that will amplify the signal as follows:

$$\frac{V_{GS}}{V_{RF}} = \frac{\dfrac{1}{j\omega_0 C_{gs} + 1/R_P}}{j\omega_0 L_g + \dfrac{1}{j\omega_0 C_{gs} + 1/R_P}} \tag{A.3.1-10}$$

with

$$\frac{1}{R_P} = \frac{C_{gs}\omega_0}{Q_P} \tag{A.3.1-11}$$

Using the relations established in A.3.1.4, we name Q_{IN} as

$$Q_{IN} = \frac{V_{GS}}{V_{RF}} = \sqrt{1 + Q_P^2}\,. \tag{A.3.1-12}$$

Therefore, the total gain of the LNA considering the input network matching is given by

$$G_T = \frac{V_{OUT}}{V_{RF}} = \frac{V_{OUT}}{V_{GS}} \frac{V_{GS}}{V_{RF}} = G_V \sqrt{1 + Q_P^2} = G_V Q_{IN}\,. \tag{A.3.1-13}$$

A.3.2 Elements for noise calculation: LNA sources of noise

In the derivation of the noise factor of the R-feedback LNA, three main sources were considered: transistor channel, feedback resistance and load resistance. The calculation of these contributions is detailed below using

$$F = \frac{v_{n0}^2}{\beta^2 G_T^2 4kTR_S}, \tag{A.3.2-1}$$

with

$$\beta = \frac{1}{2} \tag{A.3.2-2}$$

if the circuit is matched at the input.

A.3.2.1 Transistor channel output noise

The output noise given by the noise in the transistor channel is given by:

$$|v_{n0}| = R_{out}\left(i_{nd} + g_m v_{gs} + i_{RF}\right), \tag{A.3.2-3}$$

with

$$i_{RF} = \frac{v_{n0} - v_{gs}}{R_F}. \tag{A.3.2-4}$$

v_{gs} can be expressed in terms of i_{RF}

$$v_{gs} = i_{RF}\left(\frac{\left(j\omega_0 L_g + R_S\right)\frac{1}{j\omega_0 C_{gs}}}{j\omega_0 L_g + R_S + \frac{1}{j\omega_0 C_{gs}}}\right). \tag{A.3.2-5}$$

So,

$$v_{gs} = R_P i_{RF} = R_S(1 + Q_P^2) i_{RF} \tag{A.3.2-6}$$

From (A.3.2-3) and (A.3.2-6)

$$|v_{n0}| = R_{out} i_{nd} \frac{\frac{R_F}{1+Q_P^2} + R_S}{\left(\frac{R_F}{1+Q_P^2} + R_S\right) + g_m R_S R_{out}}. \quad \text{(A.3.2-7)}$$

A.3.2.2 Output noise of the charge resistance

The estimation of the thermal noise contributed by the charge resistance, R_L, follows the same development than the transistor channel noise, replacing i_{nd} by $i_{n,RL} = 4kT/R_L$,

$$|v_{n0}| = R_{out} i_{n,RL} \frac{\frac{R_F}{1+Q_P^2} + R_S}{\left(\frac{R_F}{1+Q_P^2} + R_S\right) + g_m R_S R_{out}}. \quad \text{(A.3.2-8)}$$

A.3.2.3 Output noise of the feedback resistance

The output noise given by the feedback resistance, R_F, is given by

$$|v_{n0}| = R_{out} i_{n,RF} \frac{\frac{R_F}{1+Q_P^2} + R_S + g_m R_S R_F}{\frac{R_F}{1+Q_P^2} + R_S + g_m R_S R_{out}}. \quad \text{(A.3.2-9)}$$

with $i_{n,RF} = 4kT/R_F$.

A.3.3 Noise factor calculation

The contributions of the three main sources considered are given by (A.3.3-1) from the transistor channel noise, (A.3.3-2) from the load resistance, and (A.3.3-3) from the feedback resistance following (A.3.1-1).

$$F_{i_{nd}} - 1 = \frac{4\gamma \left(\frac{R_F}{Q_{IN}^2} + R_S\right)^2}{Q_{IN}^2 g_m R_S \left(\frac{R_F}{Q_{IN}^2} + R_S + g_m R_S R_{out}\right)^2} \quad \text{(A.3.3-1)}$$

$$F_{i_{n,RL}} - 1 = \frac{4 \left(\frac{R_F}{Q_{IN}^2} + R_S\right)^2}{Q_{IN}^2 g_m^2 R_S R_{out} \left(\frac{R_F}{Q_{IN}^2} + R_S + g_m R_S R_{out}\right)^2} \quad \text{(A.3.3-2)}$$

$$F_{i_{n,RF}} - 1 = \frac{4\left(\frac{R_F}{Q_{IN}^2} + R_S + g_m R_S R_F\right)^2}{Q_{IN}^2 g_m^2 R_S R_F \left(\frac{R_F}{Q_{IN}^2} + R_S + g_m R_S R_{out}\right)^2} \quad \text{(A.3.3-3)}$$

Therefore, the total noise factor is given by

$$F_{total} = 1 + A\left[\gamma + \frac{1}{g_m R_L} + \frac{\left(1 + \frac{g_m R_S R_F}{R_F/Q_{IN}^2 + R_S}\right)^2}{g_m R_F}\right], \quad \text{(A.3.3-4)}$$

with

$$A = \frac{\left(\frac{R_{in} + R_S}{R_{in}}\right)^2 (R_F/Q_{IN}^2 + R_S)^2}{Q_{IN}^2 g_m R_S \left(R_F/Q_{IN}^2 + R_S + g_m R_S (R_F || R_{out})\right)^2}. \quad \text{(A.3.3-5)}$$