Light amplification and laser emission in electrically driven hybrid III-V semiconductor on SOI nanostructures

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Tired of lying in the sunshine, staying home to watch the rain
You are young and life is long, and there is time to kill today
And then one day you find ten years have got behind you
No one told you when to run, you missed the starting gun

Time – Pink Floyd

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Résumé en français

L'exploitation de la lumière comme véhicule de l'information au lieu des électrons est considérée comme l'une des meilleures solutions pour dépasser les limites des interconnexions électriques. Alors que des solutions photoniques ont déjà remplacé les lignes électriques pour les applications à longue distance, une alternative optique aux interconnexions métalliques à l'intérieur des circuits intégrés n'existe pas encore : en particulier, même si les guides d'ondes en silicium représentent une excellente opportunité pour transférer le signal optique dans l'ensemble de la puce, des composants nanophotoniques actifs consommant peu d energie et présentant des dimensions réduites, une vitesse ultra-élevée et une compatibilité avec la technologie CMOS, n'ont pas encore été commercialisés.

Cette thèse vise à développer deux dispositifs fondamentaux que l'on peut trouver à l'intérieur d'un circuit photonique intégré : un nanoamplificateur optique et une source nanolaser. Leur concept repose sur un cristal photonique bidimensionnel (2D-PhC) injecté électriquement constituant une structure hybride InP sur SOI. Tout d'abord, nous avons modélisé les deux dispositifs, démontrant l'efficacité de leur schéma d'injection électrique ainsi que leur interfaçage optique avec un guide d'onde de silicium. Ensuite, nous avons développé un procédé de technologie complet, permettant de fabriquer ces structures tout en respectant les limitations imposées par l'industrie de la microélectronique. Cette tâche méticuleuse nous a permis de valider le schéma d'injection électrique et de démontrer un nanolaser à injection électrique, fonctionnant à température ambiante et présentant une puissance de seuil laser ultra-faible (environ 75 µA à 1 V) sous une polarisation électrique AC. Finalement, l'étape technologique limitante a été identifiée et discutée. Sa résolution conduira à la démonstration de ces nanolasers en regime continu.

Mots clés : Nanotechnologie, Nanophotonique, Optoélectronique, Photonique-sur-Silicium, Cristaux-Photoniques, Nanolaser-en-Semiconducteur, Nanoamplificateur-Optique

Abstract

Exploiting light as a vehicle of the information instead of electrons is thought to be one of the best solutions to go beyond the electrical interconnects limitations. While photonic solutions have already replaced electrical lines for long-distance applications, an optical alternative to the lossy metallic interconnects inside integrated circuits is still missing: particularly, even though silicon waveguides represent a great opportunity to transfer the optical signal throughout the whole chip, active nanophotonic components for low-power applications presenting small footprint, ultra-high driving speed and compatibility with the CMOS-technology, suitable for the on-chip cointegration of photonic and electronic integrated circuits, have not been commercialized yet.

This PhD aimed at developing two fundamental devices we can find inside an integrated photonic circuit: an optical nanoamplifier and a nanolaser source, both relying on an electrically injected hybrid InP on SOI bidimensional Photonic Crystal (2D-PhC). Firstly, we modeled the two devices, demonstrating their efficient electrical injection scheme as well as optical interfacing with a silicon-based passive circuitry, rendering them good candidates for low-power applications. Then, we developed a full technological process flow, fabricating these structures while respecting the limitations imposed by the microelectronic industry. This meticulous task allowed us to validate the designed electrical injection scheme and to demonstrate electrically driven nanolaser, working at room temperature and presenting ultra-low laser threshold power (around 75 μA at 1 V) under an AC electrical bias. Eventually, the limiting technological step was identified and discussed. Its resolution will lead to the demonstration of these nanolasers under a DC electrical signal.

Keywords: Nanotechnology, Nanophotonics, Optoelectronics, Silicon-Photonics, Photonic-Crystals, Semiconductor-Nanolaser, Optical-Nanoamplifier

Synthèse en français

Au cours de ce doctorat, nous avons travaillé sur le développement d'une solution nanophotonique basée sur un cristal photonique bidimensionnel (2D-PhC) optoélectronique intégré sur une plateforme silicium pour la conception d'une source laser et d'un amplificateur optique. Ces derniers se révèlent être des composants clés dans les circuits intégrés optiques pour les applications de télécommunications et d'informatique. Le manuscrit est organisé comme suit :

1) Introduction
2) Conception et modélisation du nanoamplificateur en 2D-PhC
3) Conception et modélisation du nanolaser en 2D-PhC
4) Fabrication des dispositifs
5) Caractérisation expérimentale
6) Conclusion et travaux futurs

1) Introduction

La société moderne fait face à une profonde digitalisation, représentant aujourd'hui l'un des principaux défis d'un point de vue technologique. La croissance exponentielle des échanges de données liées à l'internet exige une vitesse de transfert toujours plus grande tout en minimisant la consommation d'énergie. Jusqu'à présent, la technologie des circuits intégrés pour les systèmes informatiques et de communication a été basée sur la microélectronique, même si elle approche un point bloquant : bien que le nœud technologique du transistor a atteint aujourd'hui 3 nm, la principale préoccupation vient des interconnexions, qui limitent les performances en termes de vitesse et de consommation d'énergie. Des nouvelles solutions sont à l'étude afin de remplacer ces problématiques interconnections métalliques. La photonique représente depuis les années 80 une bonne alternative à l'électronique pour les systèmes de télécommunication longue distance. Aujourd'hui, 99% du trafic de données transocéaniques est transporté par des fibres optiques. De plus, depuis l'apparition des centres de données, des modules émetteurs-récepteurs optiques sont entrés en scène, devenant l'entité en charge de la gestion du transfert de données entre serveurs. Cependant, la principale source de consommation d'énergie à l'intérieur de ces immenses infrastructures réside dans les serveurs de calculs. Dans ce contexte, aucune alternative viable aux interconnexions des circuits intégrés n'est encore disponible. L'une des meilleures prospectives pour répondre à ce problème est la nanophotonique, qui consiste à

utiliser des dispositifs ultracompacts (dimensions inférieures à 100 µm^2) permettant de piéger et de gérer la lumière dans des volumes proches de la limite de diffraction $\left(\lambda/n\right)^3$. Parmi eux, les cristaux photoniques (PhC) alimentés électriquement semblent être la technologie la plus mature et le meilleur compromis en termes d'empreinte, de consommation d'énergie et de coût [59].

2) <u>Conception et modélisation du nanoamplificateur en 2D-PhC</u>

Une membrane 2D-PhC est une structure confinant la lumière dans deux dimensions grâce à la variation périodique de l'indice de réfraction (généralement obtenue en perçant des trous dans le matériau adopté), tandis que dans la direction normale au plan de périodicité, la lumière est piégé grâce à la réflexion interne totale (RIT). Dans le diagramme de bande photonique, selon les paramètres géométriques de la structure, il y a une gamme de fréquences pour laquelle la propagation de la lumière est interdite : cette région est appelée bandgap photonique. En introduisant un défaut linéaire à la membrane 2D-PhC (c'est-à-dire en enlevant une rangée entière de trous), on peut observer l'apparition de nouvelles bandes photoniques, où la lumière est emprisonnée dans la région du défaut linéaire : une bande est localisée à l'intérieur du bandgap photonique (bande gap-guided), tandis que l'autre bande possède un vecteur d'onde plus grand que les modes du PhC sans défaut (bande index-guided). Notre nanoamplificateur 2D-PhC présente une géométrie asymétrique, exploitant d'un côté la configuration périodique des trous du PhC comme métamatériau (c'est-à-dire la bande index-guided du PhC) pour confiner la lumière, tandis que de l'autre côté le signal est piégé par RIT grâce au flanc gravé. La conception asymétrique provoque l'apparition d'une composante verticale de champ électrique. Celle-ci est une composante indésirable, car notre région active composée de puits quantiques contraints ne fait qu'amplifier la lumière polarisée TE. Un soin particulier doit être apporté au choix des paramètres géométriques, afin de minimiser l'indice effectif de la composante TM par rapport à celle TE. L'interfaçage entre le circuit de silicium passif et le guide d'ondes 2D-PhC est réalisé par couplage évanescent au moyen de convertisseurs de mode, où l'idée est de jouer avec la différence d'indice effective entre les deux guides d'ondes (en faisant varier la largeur du guide d'ondes PhC) pour obtenir un transfert de lumière progressive d'une plateforme à l'autre. La distance verticale entre le guide d'ondes en silicium et PhC est réglée à 230 nm. Nous présentons deux convertisseurs de mode : le premier consiste à faire varier linéairement l'indice effectif du guide d'ondes PhC (convertisseur linéaire), et permet d'atteindre une efficacité de couplage d'environ 90% dans une gamme de longueurs d'onde de 150 nm pour une longueur du convertisseur de 100 µm; l'autre est basée sur le critère d'adiabaticité présenté en [74], réduisant la longueur du convertisseur par rapport à la version linéaire tout en maintenant un couplage efficace entre les plates-formes passive et active (avec une efficacité de couplage et une gamme de longueurs d'onde identiques à la version linéaire). D'un point de vue électrique, la membrane

III-V est conçue comme une diode formée par une jonction P-i-N. Le but principal de la conception asymétrique est de mettre en œuvre un schéma d'injection latéral des porteurs : le contact P est placé sur le côté de la paroi du PhC, où la membrane III-V est partiellement gravée en ne laissant que la couche dopée P (base du PhC), tandis que le contact N est placé sur le côté des trous du PhC. L'objectif est de concentrer la majorité des recombinaisons radiatives à l'intérieur du guide d'ondes PhC, afin d'obtenir une interaction efficace avec le mode optique pour l'amplification de la lumière. Le guide d'ondes en PhC est placé à proximité de la base dopée P, profitant de la grande différence de mobilité entre les électrons et les trous. Une telle conception s'avère adaptée à une application à faible puissance, comme l'exigent les circuits intégrés photoniques, avec une longueur et une puissance de polarisation du dispositif réduites d'un ordre de grandeur par rapport aux solutions de l'état de l'art pour atteindre le même niveau d'amplification (300 µm de long et ∼10 mW de puissance de polarisation pour une amplification de 10 dB). Il est possible de réduire ultérieurement la longueur du dispositif en profitant du régime de lumière lente, consistant en une perturbation locale de la géométrie du guide d'ondes PhC provoquant une réduction de la vitesse de groupe du mode s'y propageant (c'est-à-dire un indice de groupe accru), améliorant l'interaction lumière-matière : nous montrons ici une conception capable d'augmenter l'indice de groupe entre 20 et 30 pour une gamme de longueurs d'onde de 23 nm.

3) *Conception et modélisation du nanolaser en 2D-PhC*

Notre structure 2D-PhC est adaptée et modélisée pour réaliser une source laser. Pour cela, contrairement au nanoamplificateur, nous n'exploitons pas la bande index-guided du 2D-PhC mais plutôt la bande gap-guided, afin de construire une cavité apodisée. Il a été démontré, en effet, que la meilleure façon de minimiser les pertes hors plan dans une cavité résonnante est de la concevoir de manière à ce que le mode fondamental possède une forme gaussienne, en profitant du *gentle confinement* du champ [91-92]. L'apodization est effectuée en perturbant la largeur de la cavité PhC du centre de la cavité à ses bords. Pour ce faire, nous modifions uniquement la structure du côté de sa paroi gravée tout en gardant la position des trous du PhC intacte, pour choisir librement la fréquence spatiale de la perturbation à l'intérieur de l'algorithme d'apodisation et de se débarrasser de la limitation posée par la période du PhC. La largeur à mi-hauteur (LMH) du mode gaussien et la largeur minimale (W_{min}) de la cavité sont sélectionnés pour rendre nos cavités monomodes. La géométrie asymétrique limite le facteur Q réalisable, puisque, comme pour le nanoamplificateur, nous observons l'apparition d'une composante verticale non négligeable du champ électrique du mode de résonant qui n'est pas confinée par les trous du PhC. Cette composante indésirable disparaît complètement en l'absence de la base du PhC. Cependant, étant donné que la base dopée P est fondamentale pour l'injection des porteurs électriques, nous minimisons l'impact de la composante verticale du

champ électrique en y perçant des trous supplémentaires. De cette façon, nous obtenons un facteur Q intrinsèque de l'ordre de 10^5 pour une longueur de structure de 20 µm, qui est réduit à $2.8 \cdot 10^4$ en incluant les dopages P et N dans la simulation. L'extraction du signal est effectuée en exploitant le couplage évanescent entre la cavité et le guide d'ondes en silicium : la très courte distance verticale avec laquelle nous travaillons (230 nm) nous oblige à appliquer un décalage transversal entre la cavité et le guide d'ondes en silicium afin de les découpler, considérant que nous avons affaire à un système surcouplé. La meilleure configuration pour le système hybride est atteinte avec une largeur de guide d'ondes en silicium de 600 nm et un déplacement transversal de 300 nm, montrant un facteur Q total d'environ $4 \cdot 10^4$ et une efficacité de couplage proche de 90%. En tenant compte des couches dopées dans la simulation, le facteur Q tombe à $1.6 \cdot 10^4$. Le schéma d'injection électrique repose sur la même idée que pour les nanoamplificateur, même si pour le nanolaser nous réduisons la longueur de la base afin de recouvrir efficacement le profil longitudinal de recombinaisons radiatives avec le champ électromagnétique gaussien pour minimiser la puissance électrique. En interfaçant les résultats des simulations optiques et électriques, nous observons que la cavité conçue dans le système hybride complet, avec un facteur Q total de 10^4, possède un courant de seuil laser inférieur à 100 µA, avec une efficacité de conversion électro-optique (wall-plug efficiency) de 23% pour un courant injecté de 250 µA et une efficacité différentielle (slope efficiency) de 32%, la rendant très compétitive pour les applications de circuits intégrés.

4) Fabrication des dispositifs

L'étalonnage complet d'un processus technologique compatible avec l'industrie CMOS est analysé. L'interfaçage des plateformes passive et active (substrat SOI et membrane InP) est réalisé par collage adhésif exploitant le benzocyclobutène (BCB) comme polymère de collage pour ses propriétés de thermodurcissement et de planarisation [100]. Le matériau III-V est ensuite structuré en deux étapes pour fabriquer la structure asymétrique 2D-PhC : la première définit le périmètre des dispositifs et le motif des trous, tandis que la seconde définit la base du PhC et le flanc du guide. Les deux étapes reposent sur l'utilisation de la HSQ comme masque dur et de la gravure ICP pour retirer le matériau InP. Ensuite, les contacts P et N sont métallisés et activés par recuit thermique rapide (RTR). Le Pd et le Zn sont utilisés pour le contact P afin d'obtenir un contact ohmique : alors que le but du Zn est de diffuser à travers l'interface métal/semi-conducteur (pendant l'étape RTR suivant la métallisation) pour la sur-doper, le Pd est exploité pour créer une morphologie uniforme à l'interface métal/semi-conducteur, sans protubérances indésirables qui affecteraient la qualité de contact. Après cela, une multi-couche en Ti/Pt/Ti/Au est déposé pour les contacts P et N, où le Pt est exploité comme une couche de blocage : dans le côté P, il force le Zn à diffuser seulement vers le bas, c'est-à-dire vers l'interface

métal/semi-conducteur, tandis que dans le côté N il empêche la diffusion de l'or jusqu'au semi-conducteur III-V pendant RTR. Ensuite, le flanc du guide et les parois des trous sont passivées pour annihiler les liaisons pendantes de surface causées par le processus de gravure sèche ICP, afin de minimiser les recombinaisons non radiative. L'échantillon est immergé dans une solution $(NH_4)_2S$, favorisant l'adhésion des atomes de soufre sur les surfaces ouvertes de l'InP. Pour protéger la couche volatile de passivation de soufre et évacuer la chaleur accumulée autour des nanostructures lors de leur polarisation, une couche d'encapsulation de silice de 1 µm d'épaisseur est déposée par PECVD. Ce type de dépôt conforme permet de protéger les parois passivés des trous. Finalement, afin de polariser électriquement les structures pendant la caractérisation, des vias sont ouvertes à travers la couche d'encapsulation juste au-dessus des contacts P et N et des pads métalliques sont déposés sur la couche de silice de 1 µm d'épaisseur pour le contact avec les sondes électriques.

La première idée a été d'intégrer le MgF_2 comme inter-couche entre le SOI et le III-V pour protéger les circuits passifs des attaques chimiques, car ce matériau présente une inertie chimique parfaite aux acides à base de HF. De plus, il possède un indice de réfraction faible, une conduction thermique élevée et est transparent aux longueurs d'onde des télécommunications. Ceci en fait un diélectrique inter-couche idéale pour notre objectif. Cependant, le MgF_2 est aussi un matériau contraint, ce qui peut conduire à l'apparition de fissures sur toute la surface de l'échantillon pendant les étapes technologiques : ceci représente une limitation puisque le substrat SOI n'est plus protégé parfaitement contre les attaques chimiques. Ainsi, le MgF_2 est remplacé par le SiO_2 et le processus technologique initial a été légèrement varié, inversant les étapes de fabrication (structuration du III-V) et exploitant le BOE pour retirer le masque dur de HSQ seulement après la première gravure ICP (création du flanc du guide et de la base dopée P), tout en le laissant après la gravure des trous (pour éviter d'attaquer l'inter-couche de silice, ce qui provoquerait l'effondrement et la rupture subséquente de la base du PhC). Dans le processus réadapté, le dépôt des métaux P et N est effectué immédiatement après la première étape de structuration du semiconducteur III-V, ce qui permet ensuite de garder le masque de HSQ après la deuxième gravure ICP.

5) *Caractérisation expérimentale*

Les travaux expérimentaux réalisés au cours de ce projet sont commentés. Tout d'abord, nous avons étudié des structures TLM pour optimiser notre étape RTR lors de la fabrication : notre objectif est de trouver les meilleurs temps et température de recuit pour obtenir un contact ohmique pour les métaux P et N tout en minimisant leur résistance. Des résistivités de contact de $5.6 \cdot 10^{-5}\ \Omega\,\mathrm{cm}^2$ et $3.7 \cdot 10^{-4}\ \Omega\,\mathrm{cm}^2$ pour respectivement métal P et N sont obtenues avec un processus RTR de 30 s à 400°C. Ensuite, nous discutons de la caractérisation de type EBIC (

courant induit par faisceau d'électrons), effectuée pour analyser si, avec le schéma d'injection électrique conçu, les paires électron-trou sont efficacement injectées pour interagir avec le mode optique. Le résultat valide la conception de notre schéma d'injection électrique latérale, montrant l'apparition d'un courant induit uniquement à l'intérieur du guide d'ondes du PhC. L'analyse de l'électroluminescence de la diode P-i-N renforce nos conclusions sur le schéma d'injection conçu, car sous une polarisation directe de la jonction, les photons émis sont localisés à proximité du flanc de la structure. Malheureusement, aucun résultat remarquable n'a été extrait des caractérisations sur les nanoamplificateurs, même si elles nous ont beaucoup aidés à améliorer le processus technologique. Nous discutons ensuite des mesures sur nos nanolasers. Nous observons un bon accord avec la modélisation optique en les pompant avec un laser CW, car ils s'avèrent fonctionner comme des sources nanolaser monomodes. Après cela, nous montrons leur caractérisation sous injection électrique. Tout d'abord, nous soulignons que la HSQ est une source de fuite de courant, nous poussant à l'isoler complètement du semi-conducteur ainsi que des métaux par des couches de silice déposées par PECVD. Ensuite, avec l'amélioration du processus technologique, les nanocavités sont polarisée avec un signal AC. Deux échantillons sont caractérisés, différant l'un de l'autre par le processus d'enlèvement de la couche de passivation de silice créée pendant la gravure ICP : nous les appelons « Sample dry » (couche de passivation ICP enlevée par attaque au plasma SF_6 non accélérée) et « Sample wet ». (couche de passivation ICP enlevée par gravure humide en BOE). Les courants (et les puissances) de seuil mesurés sont très faibles et en bon accord avec le modèle théorique, en particulier pour les cavités de « Sample wet » ($I_{th} \sim 75\ \mu A$, $P_{th} \sim 75\ \mu W$). Finalement, les cavités sont caractérisées à l'aide d'une polarisation électrique DC : même si à partir des spectres extraits nous pouvons voir l'apparition de pics de résonance, le régime laser n'est pas atteint. Ce résultat indique que la principale limitation est représentée par l'élimination sous-optimale de la couche de passivation ICP en silice, qui empêche la passivation des parois latérales par le dépôt de soufre. Pour le vérifier, nous comparons les caractéristiques I-V des cavités dans des conditions de polarisation directe et inverse : les nanocavités de « Sample dry », comparées à celles de « Sample wet » avec des paramètres géométriques identiques, présentent une résistance plus élevée en raison de la présence de trous dans la base et d'un courant inverse plus élevé. Cela souligne que la gravure par voie humide BOE est bien meilleure que la gravure au plasma SF_6 non accélérée pour éliminer la silice déposée lors de la gravure ICP. Ensuite, nous montrons le résultat d'une caractérisation de la photoluminescence résolue en temps, ce qui nous permet d'extraire la durée de vie des porteurs d'une cavité de « Sample wet » et d'un morceau non gravé du même semiconducteur III-V : notre objectif est de récupérer les temps de vie des recombinaisons radiatives et de surface de la cavité pour les comparer. Grâce au résultat extrait, nous sommes en mesure de conclure que dans nos structures, en raison de l'élimination sous-optimale de la couche de passivation ICP, les processus non radiatifs de surface sont prédominants par rapport aux processus radiatifs,

ce qui explique pourquoi nos cavités ne fonctionnent pas dans des conditions de polarisation en continue.

6) *Conclusion et travaux futurs*

Le modèle théorique établi suggère qu'avec ce type de structures, il est possible de confiner la lumière dans des petits volumes proches de la limite de diffraction et de concevoir des dispositifs ciblant des applications à très faible puissance. En outre, le processus technologique calibré respecte la limite de température posée par la technologie CMOS (back-end-of-line), rendant nos structures compatibles pour la co-intégration sur puce de circuits photoniques et microélectroniques. Les résultats des caractérisations sont en bon accord avec la modélisation mise en œuvre : en particulier, les nanolasers montrent des courants (et des puissances) de seuil ultra-bas sous une polarisation électrique AC. Cependant, pour les faire fonctionner en régime continue, la passivation de surface doit être optimisée pour annihiler les liaisons pendantes de surface : une méthode efficace pour ouvrir complètement les parois latérales des trous du PhC après la gravure ICP doit être mise en œuvre. Une autre optimisation très importante qui doit être considérée est l'enlèvement du masque de HSQ après la deuxième étape de fabrication III-V : en fait, elle limite l'évacuation de la chaleur et elle est source de fuite de courant si elle n'est pas correctement isolée des métaux et du semi-conducteur. L'exploitation d'une solution de gravure humide BOE après la gravure des trous apporterait un double avantage : si nous pouvions tremper l'échantillon dans l'acide aussi longtemps que souhaiter, en une seule étape nous pourrions nous débarrasser du masque dur de HSQ et de la couche de passivation ICP en silice. Pour ce faire, nous devons développer un processus de protection de la silice sous les structures : une des tâches les plus importantes à accomplir sera d'étudier en profondeur les propriétés du MgF_2 et d'améliorer son processus de dépôt pour minimiser sa contrainte et prévenir sa fissuration. Une fois le problème de passivation résolu, l'un des principaux travaux à venir sera d'évaluer les performances des nanoamplificateurs, afin de démontrer leur adéquation aux applications de faible puissance. Une optimisation supplémentaire peut également être effectuée sur la modélisation des structures : une idée serait de minimiser le nombre de trous du PhC, en minimisant le rapport surface/volume. Même si le problème de la passivation n'était pas résolu, la réduction du nombre de trous réduirait sûrement l'impact des mécanismes de recombinaison de surface non radiatifs. Une autre optimisation intéressante qui mérite d'être étudiée concerne l'hydrogénation de la couche dopée P dans la région des trous du PhC, afin de maximiser l'injection de paires électron-trou à l'intérieur du guide d'ondes (ou de la cavité) du PhC et d'éviter les fuites de courant dans la région des trous. Une fois l'opération sous tension de polarisation DC démontrée, il sera très important d'analyser la bande passante de ces nanostructures. Compte tenu de leurs petites dimensions et du faible volume couvert par la zone

de déplétion de la jonction P-i-N (ultérieurement réduit par l'hydrogénation de la couche P), nous nous attendons que leur capacité soit ultra-faible : nous croyons fermement que ces dispositifs peuvent être adaptés pour des opérations à grande vitesse.

La grande polyvalence de la structure 2D-PhC optoélectronique permet de concevoir tous les dispositifs que nous pouvons trouver dans un circuit photonique, en réajustant simplement les paramètres géométriques. Outre un nanoamplificateur et un nanolaser, il est possible de concevoir la géométrie 2D-PhC comme un photodétecteur. La capacité ultra-faible de ce dispositif permettrait de supprimer le module d'amplificateur transimpedance (ATI) que nous trouvons dans les systèmes de photodétection standard et de le remplacer par une simple résistance [127], beaucoup moins chère et moins énergivore qu'un ATI. Le développement de notre structure en tant que photodétecteur fait l'objet d'un programme de prématuration du CNRS que nous avons remporté au cours de la dernière année de ce projet de doctorat. La polyvalence démontrée par la structure asymétrique 2D-PhC ouvre également de grandes perspectives pour l'intégration des dispositifs conçus dans un circuit intégré photonique. Leur empreinte réduite et leur faible consommation énergétique donnent la possibilité d'envisager leur intégration dense dans un seul circuit. De plus, grâce au processus technologique développé respectant les limitations imposées par la technologie CMOS back-end-of-line, ces structures peuvent ouvrir la voie à la cointégration sur puce de circuits intégrés photoniques et microélectroniques. Cela permettrait d'aller au-delà des limites du goulot d'étranglement des interconnexions électroniques. En particulier, ces solutions nanophotoniques possèdent les performances requises pour la conception de modules émetteurs-récepteurs intégrés (par exemple, pour la communication à haute vitesse entre les entités électroniques à l'intérieur d'un microprocesseur), capable de transférer les données à des vitesses supérieures à 1 Tbit/s. En outre, leurs dimensions réduites ainsi que leur faible consommation énergétique et leur vitesse opérationnelle ultra-élevée peuvent également être bénéfiques pour la conception de solutions hardwares tout-optiques pour les applications d'intelligence artificielle (IA) et d'apprentissage profond (AP).

Contents

Chapter 1: Introduction

We currently live in the digital era and one word has become of utmost importance in all our lives: internet. Many domains during the last decade have changed and have been readapted to fit in the increasing world's digitalization: economy (for example, with the growth of cryptocurrencies), social interaction (with social media and dating websites), news media (newspaper digitalization), health (databanks for statistical analysis of drugs' effectiveness) are just few examples of the rising importance the internet is occupying in our everyday life. Figure 1 represents the evolution of the number of internet users in the last 20 years.

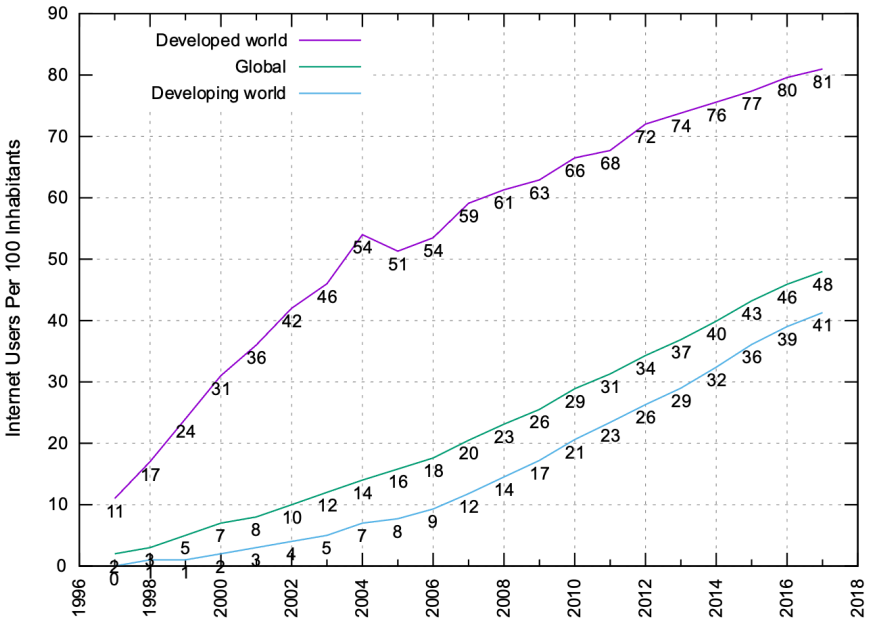


Figure 1: Internet users per 100 inhabitants from 1997 to 2017 [1]

As we can see, the number is increasing year by year, and today we can say that, considering all the cities in the world, half the population, on average, uses internet.

Apart from single users, internet nowadays is widely used to connect objects to let them communicate and exchange information: we can talk, in this case, about Internet of Things (IoT). The idea behind IoT is the automation: facilitating work and everyday life for each person is the ultimate goal and one way to achieve it is getting the best result with the least amount of effort. So how about having machines connected all together on the same network and controlled by a

single device (a smartphone, or a computer), which are able to perform multiple tasks with extremely high resolution and efficiency, without the need for the human to intervene? Behind this idea, multiple technologies like “smart homes” or Machine Learning have come to light. The only action the user is demanded to perform is to enable/disable the connected machines with the control device.

This massive digitalization trend has a single consequence: there is an increasing amount of digital data streaming on network systems. According to [2], the internet traffic is growing exponentially and in 2017 we reached the record level of 1.1 zettabytes (10^{21} bytes) to and from the data centers, the organizational unities coordinating and managing the storage and the traffic of information in companies as well as in the public administration. These huge structures emerged about a decade ago, when giants like Google, Facebook or Amazon needed several hundreds of thousands (even a million) of servers for their business: since then, the data center market went through a rapid growth. It is now usual for companies to store their servers in these dedicated centers. But if the world’s digitalization process is improving the human race’s lifestyle on one hand, on the other hand it requires a faster and faster technological evolution, for two main reasons:

- To keep up with the increasing demand of data’s computation and transfer speed, so to continue achieving the non-blocking network condition (internet is a fundamental mean of connection between people all around the world, and the same is valid for industries and companies: the internet’s saturation would basically mean the collapse of global economy).
- To preserve environmentally our Planet, due to the dramatic increase in the amount of energy burnt in data centers.

In the next section we will analyze the electronic Integrated Circuit Technology (ICT) and we will try to understand why its performances are no more sufficient to face and give a solution to the two major requirements we just listed.

1.1 Electronic Integrated Circuit Technology

Since the transistor entered the scene in the 50s, the ICT has been dominated by electronics. Despite the very first prototypes made in Germanium, the Silicon-based transistor became quickly dominant for its better thermal properties and its low cost. During the years, evolution in research has given the possibility to improve more and more the so-called technology node, which means that the size of a single transistor has continuously been reduced, increasing at the same time the integration of multiple transistors per unit surface. Such a growth in integrability is well described by the Moore’s law, postulated by the Intel co-founder Gordon Moore in 1965 (Figure 2).

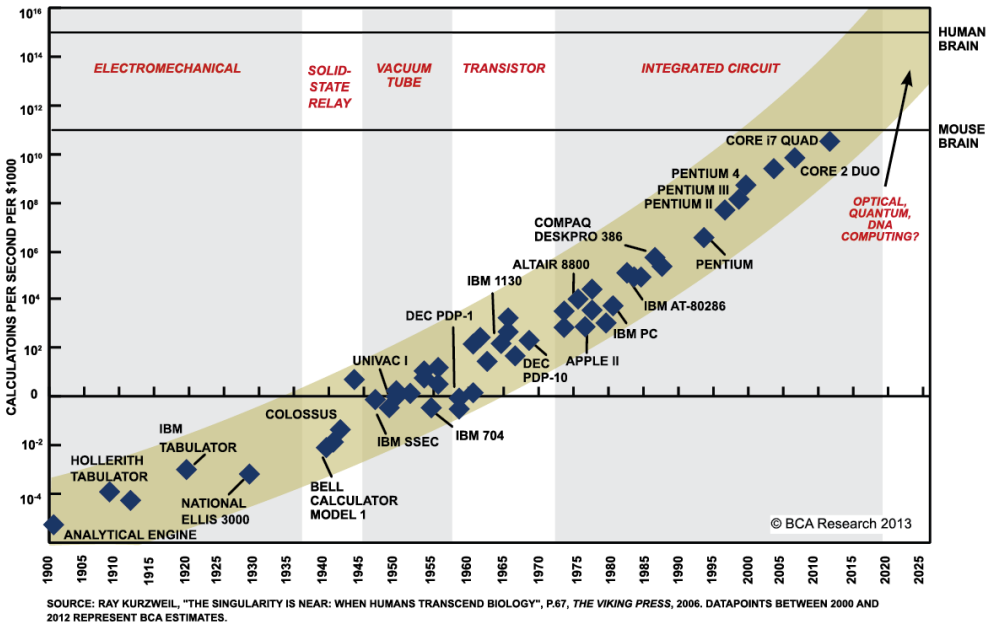


Figure 2: Moore's law

According to Moore, the number of transistors per unit volume in a silicon integrated chip doubles every two years: this basically means that we are able to concentrate more computing power in the same space at a lower cost. This trend has been respected for decades; however, in the recent years the integration rate is slightly slowing down as we approach closer and closer a technological limit in terms of footprint and performances. Many experts, including Moore himself, expect that Moore's law is coming to its end [3].

The greatest limitation regarding electronic circuits is linked with the interconnections: in fact, even though by reducing the size of a transistor we are able to improve its performance in terms of speed, the same does not apply for the electrical lines. This is due to the fact that, depending on the adopted geometry, metallic wires present an electrical resistance and capacitance, limiting the operating speed of the whole circuit. Additionally, the resistive loss physics dominating electrical lines is the source of thermal losses by Joule effect: this is a major concern in densely integrated circuits, often requiring cooling down systems to counteract this effect and, consequently, increasing the overall amount of burnt energy [4]. Therefore, no matter how small we can conceive a transistor, in densely-integrated electronic circuits the interconnects are always the main source of signal losses, at the same time imposing an upper limit for the driving frequency.

New solutions are under investigation to go beyond Moore's law bottleneck: one of the most popular is certainly the exploitation of Photonics Integrated Circuits and Optical Interconnects to

replace the lossy electrical lines, paving the way for the co-integration of electronics and photonics chip.

1.2 Photonics

A Photonic Integrated Circuit (PIC) is a system exploiting light as a vehicle to transfer the information. In the previous section, we have stated that the main limitation of modern integrated electronic circuits is linked to the metallic interconnects. This is not the case in PICs: in fact, the adopted transmission lines for the light, waveguides, present very low loss and are able to carry the electromagnetic signal from input to output substantially unvaried, since they avoid the resistive loss physics dominating the propagation loss and the distortion of electrical lines [4]. Therefore, while in electronic circuits the interconnects are designed to work at a defined frequency limit, in photonic ones the high speed operation is limitless in waveguides, the frequency being limited only by the photonic devices present in the circuit.

Since the 80s photonics has started to attract attention from researchers, becoming more and more important over the years. The first application in which photonics replaced electronics is telecommunication: in 1988 the first optical fiber cable (TAT-8) substituted the coaxial cable used for transatlantic communication between United States, United Kingdom and France. Nowadays, undersea optical fibers carry the 99% of data traffic crossing the ocean.

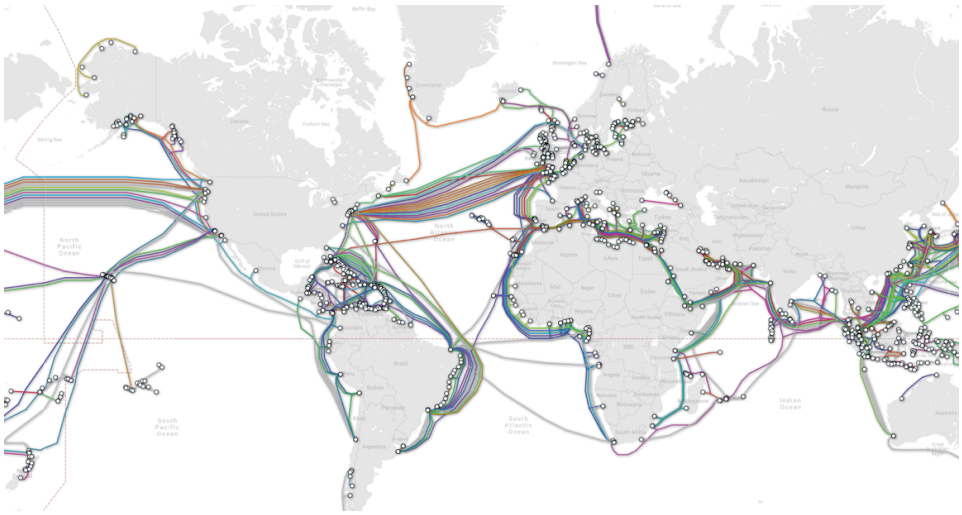


Figure 3: The world's submarine cable map [5]

During the years optical fibers replaced coaxial cables even for short-distance communication: today many Local Area Networks (LANs) are based on optical fibers (who does not want the internet connection based on the optical fiber at home?).

With the evolution of the Internet, the development of new photonic technologies has been necessary to keep up with the exponential growth of digital data traffic. Particularly, the conception of Optical Transceiver (Transmitter-Receiver) entered the scene. This circuit represents the bridge between the electronic and the photonic world: it is able to convert an electrical input signal into light and transmit it (transmitter) and to convert back an optical signal into an electrical one (receiver), achieving unprecedented transfer speeds. There are few fundamental blocks that constitute a full Optical Transceiver:

- A laser source, modulated by an electronic driver, to create the light signal.
- An optical channel, the waveguide, to move the information throughout the whole circuit.
- A photodetector, to collect the light output signal, convert it to an electronic one and send it to a receiver electronic circuit.

Additionally, we could find two optional components:

- A modulator, to encode the optical signal (whether the modulation is not directly applied to the laser source).
- An optical amplifier, in order to increase and preserve the signal power throughout the circuit.

To understand the importance of optical transceivers, it is sufficient to think that, in every data center, the hundreds of thousands of servers are interconnected with each other thanks to pluggable optical transceivers and kilometers of optical fibers (Figure 4), with data rates going beyond 400 Gbits/s.

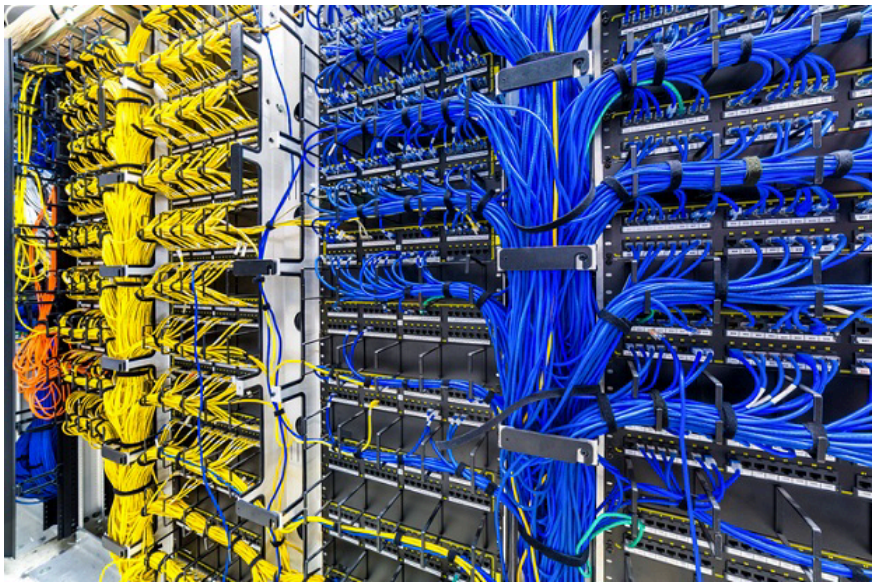


Figure 4: Example of optical fibers interconnecting several servers

In this manuscript, we will focus our attention on laser sources and amplifiers constituting a PIC. In the next section, we will start analyzing the solution already available on the market.

1.3 Laser sources and amplifiers: standard solution

1.3.1 Introduction

In a PIC we need to provide active and passive functionalities, while maintaining low cost production. That is why Silicon has been considered as a particularly important material for photonic circuits. However, it is already well known that while Silicon is a great material for passive photonics applications [6][7] in the O band (1.3 μm) and C band (1.55 μm) of the telecom window, the same does not apply for active ones: in fact, its indirect band gap does not allow efficient radiative recombination of carriers and, consequently, efficient emission of light. There has been some interesting work in the past years like [8][9], trying to fabricate silicon-based laser sources: however, these solutions are considered too inefficient for real applications.

The best materials for active functionalities are undoubtedly III-V semiconductor compounds: most of them present a direct band gap, which is ideal for light generation. Moreover, just by changing their composition, it is possible to control at will the emission wavelength.

We can then talk about hybrid platforms, where III-V compounds play the role of light-emitters, while Si-based waveguides play that of the bus circuitry. During the years many solutions have been used to combine both platforms together, like flip-chip bonding, direct growth of III-V on silicon and heterogeneous integration; more details can be found in [10][11][12].

1.3.2 Laser sources

1.3.2.1 VCSEL

VCSELs (Vertical Cavity Surface Emitting Laser) are laser sources emitting perpendicularly to the top surface, as the name suggests. It is used in many applications, like computer mouse, face recognition, laser printers and data communication. It consists of a classic Fabry-Pérot feedback system, with a gain material (typically Multiple Quantum Wells) placed in between the two Distributed Bragg Reflectors (DBRs). A typical schematics is shown in Figure 5. One of the key advantages of VCSELs in communication systems is that they have been capable to replace highly consuming electronic systems reducing drastically the power consumption (from several pJ/bit to around 300 fJ/bit in the latest advancements [14]), while operating at high speed (> 20 Gbits/s). Their dimensions are also quite small, presenting diameters of around 10 μm and lengths of few μm. For example, they can be made of GaAs-based materials, with the gain medium made of alternated InGaAs/GaAs compounds [15].

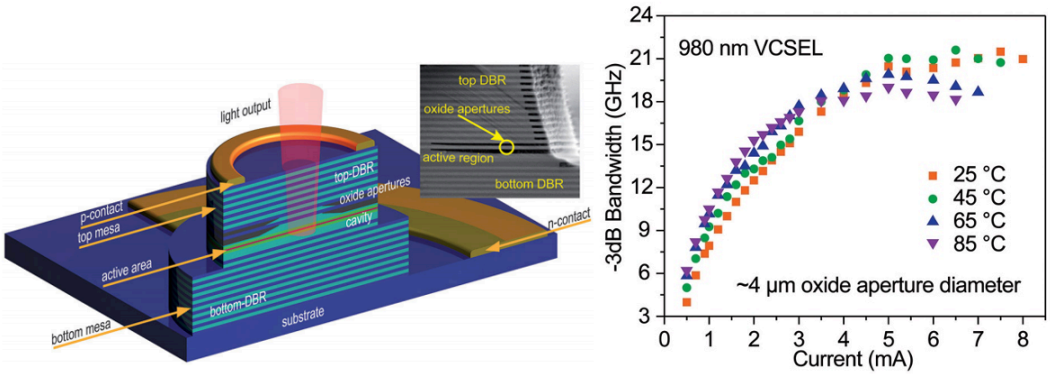


Figure 5: On the left, classic schematics of a VCSEL ; on the right, bandwidth vs bias current [13]

The main limitations of VCSELs is related to the limited bandwidth of emitted wavelengths and above all their difficult integration in a silicon PIC, rendering until now very difficult their exploitation for on-chip applications.

1.3.2.2 DFB laser

Distributed Feedback (DFB) lasers are the most diffused edge-emitting lasers. Contrarily to standard Fabry-Pérot feedback lasers, it presents a periodic diffraction grating along its whole length, taking advantage of Bragg scattering to provide optical feedback (Figure 6).

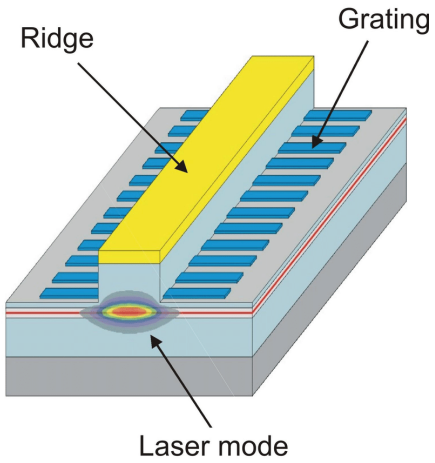


Figure 6: Typical schematics of a DFB laser [16]

This kind of laser is widely used for high-speed fiber optic telecommunications, where a single mode operation is needed: they are still commonly used for long haul optical links in the C band, the telecom window with the lowest loss, thanks to their high emitting power.

While for long distance applications DFB lasers are still dominating the market, they seem to be hardly exploitable for silicon PIC. In fact, even though interesting solutions have been studied [17], they present dimension (from several hundreds of μm to mm) and power consumption (few pJ/bit) way too high for efficient on-chip integration.

1.3.3 Amplifiers

While there has been and there is still an intense research on laser sources for PICs, the Semiconductor Optical Amplifier (SOA) world seems to stimulate a bit less interest of the community. In fact, up to now, photonic solutions have mainly been exploited for long-and-medium distance applications, with high output power sources and Erbium Doped Fiber Amplifier (EDFA) repeaters to avoid the degradation of the power level. Anyway, with the continue scaling-down of silicon photonics systems, even if power levels has been drastically reduced, power regeneration is required to preserve a readable signal input/output.

1.3.3.1 Hybrid III-V on silicon evanescent amplifier

The state of the art of hybrid SOAs is based on the structure shown in Figure 7.

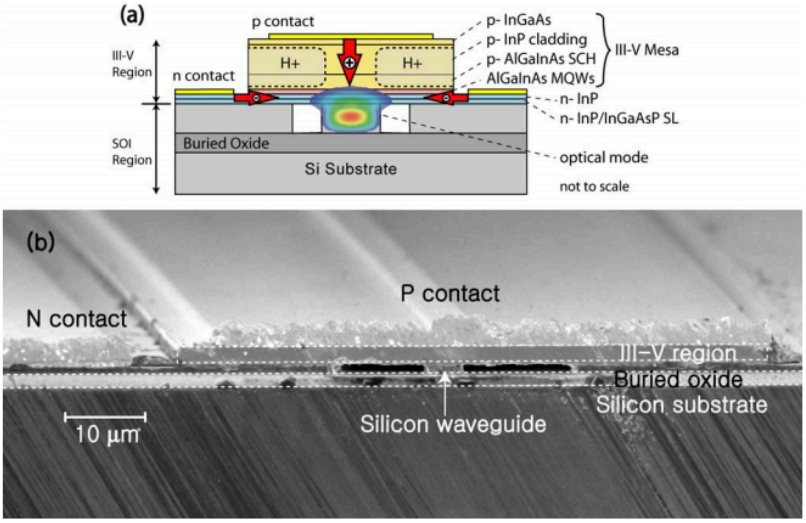


Figure 7: (a) SOA's cross section; (b) SEM picture of the fabricated device [18]

The idea is to bond the III-V layer as close as possible to the Si waveguide and take advantage of taper structures to evanescently couple the optical mode confined in the passive circuitry to the amplifier: in that way, the light signal becomes a hybrid mode, propagating in both materials simultaneously and, consequently, getting amplified during its propagation. Amplification is possible thanks to the electrical injection of carriers in the Multiple Quantum Wells (MQWs) gain

region: the hybrid mode, then, propagating through the gain material, gives rise to stimulated emission [21]. At the output of the amplifier, other taper structures couple the signal back to the Si waveguide.

Thanks to this geometry, chip gains beyond 10 dB and saturation powers beyond 15 dBm have been demonstrated [18][19][20]. However, exactly like the previously discussed laser sources solutions, the main limitations come from the footprint and the power consumed to bias the SOA. Particularly, the reported devices were always approximately 1 mm long, burning several hundreds of mW to get the desired level of amplification: a denser and efficient integration in PICs appears to be complicated.

1.4 Critical need for on-chip photonic solutions: nanophotonics

As we mentioned before, the digital data exponential growth grabbed researchers' attention on the need to find new technologies capable to provide the demanded information's pace with low power consumption. So far, we have described the generic components (in terms of signal generation and amplification) constituting the core of the main photonic solution available in the communication market: the optical transceiver.

However, this is not enough. Environmentally, data centers still represent a major concern: in fact, it has been estimated that nowadays they contribute to the 5% of world's electrical power dissipation (corresponding to 40% more than UK's total energy dissipation!) and according to some forecasts they will reach 20% by 2030. In order to evaluate data centers' power consumption, a figure of merit called Power Usage Efficiency (PUE) was introduced, defined by the ratio between the total power needed in the center and the power consumed for computations. PUE values are ranging from 2 for conventional data centers to 1.1 for hyperscale ones, which means that 50% to 90% of the energy burnt in a data center is due to computations [2], still relying on densely integrated electronic circuits. There is an imperative need, then, to replace the highly consuming electronic computing systems, mainly limited by their metallic interconnections.

Unfortunately, for the already mentioned limits, the previously cited photonic devices are not good candidates to pave the way for the on-chip cointegration of photonic and electronic integrated circuits. According to [4], in order to achieve such a milestone, an optical interconnect must:

- be Si-based and compatible with the CMOS back-end-of-line technology;
- possess low energy consumption, on the order of few tens of fJ/bit;
- have high integration capacity, with devices' footprints not exceeding 100 μm^2;
- be driven at high data rates (bandwidth > 10 Gbits/s).

State of the art devices present a much larger footprint (with sections > 10 µm²), resulting in a reduced light-matter interaction and, consequently, with limited energetic efficiency. Reducing the footprint of these components is an imperative need, in order to realize the convergence of microelectronics and photonics. We can introduce at this point the concept of Nanophotonics: we need to conceive optoelectronic devices where the light is confined in very small volumes (comparable to the semiconductor's operating wavelength) to accomplish the previously listed requirements.

In the next section, we will describe the nanophotonics state of the art focusing on laser sources. From now on, we will refer to them as Nanolasers. To the best of our knowledge, we are not aware of existing Nanoamplifier solutions.

1.4.1 Nanolaser state of the art

In order to attain the listed characteristics, different possibilities are under study. Among them, we can find microdisk or microring lasers on Si, even though the most promising solutions seem to be the Metallic Cavity and the Photonic Crystal nanolasers.

1.4.1.1 Microring lasers

The hybrid microring laser on silicon represents a good improvement for on-chip applications with respect to the marketable laser sources previously discussed. It presents smaller footprint with respect to DFB lasers and, contrarily to VCSELs, can be rather simply integrated with a Si circuitry. Figure 8 shows a typical microring laser architecture.

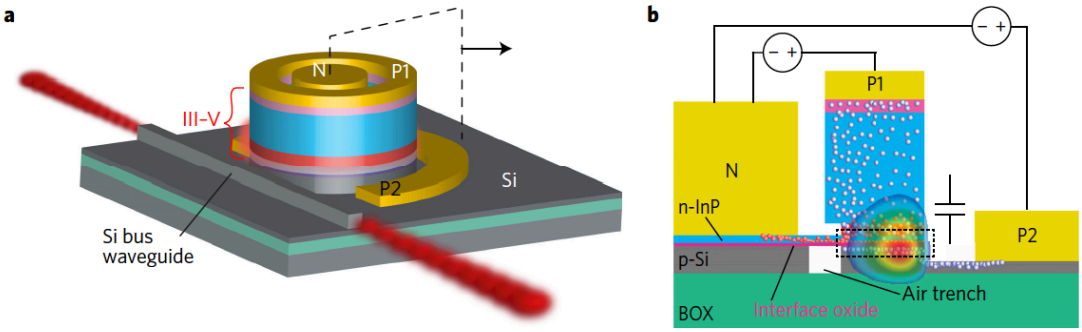


Figure 8: microring laser on silicon schematics : (a) 3D view, (b) cross section [22]

In this particular work, there is an additional terminal (P2) in order to form a MOS capacitor localized between the n-InP and p-Si (there is a thin layer of Al_2O_3 in between). In that way, by biasing the capacitor, it is possible to vary the Si and InP free carriers concentration, causing a

variation of both materials' refractive index and free-carrier absorption, modulating laser diode's resonance wavelength and output power.

Another interesting work is represented in [23], where the authors show the benefit of undercutting the MQWs gain region: in that way it is possible to concentrate the carriers' injection into the outer edge of the microring, increasing the gain/optical mode overlap and consequently reducing the laser threshold while increasing the output power.

In [24] the laser's performances are evaluated investigating different metallic contact displacement as well as different evanescent coupling configurations between laser diode and passive circuitry.

Even though hybrid microring lasers represent an improvement with respect to DFB lasers and VCSELs, they still present relatively large footprint (radius > 20 μm) and energy consumption (bias power on the order of mW).

1.4.1.2 Microdisk lasers

Similarly to microring-based cavities, a microdisk takes advantage of successive Total Internal Reflection (TIR) events as a feedback, giving rise to a whispering gallery mode. A microdisk schematic representation is shown in Figure 9.

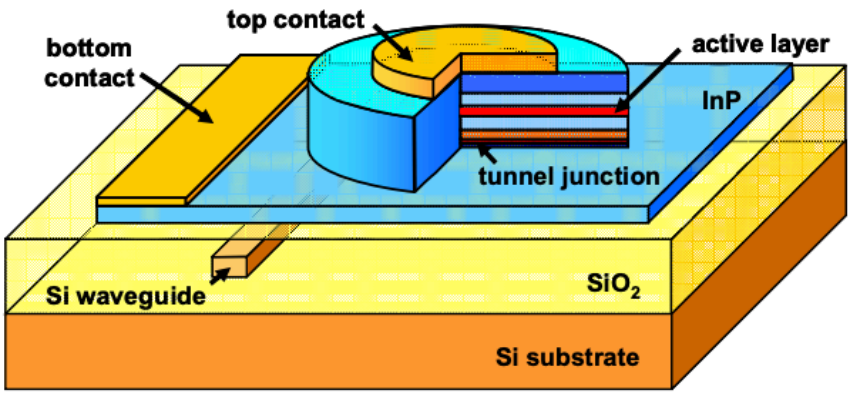


Figure 9: schematic representation of a hybrid microdisk laser [27]

Many microdisk-based works have been published consisting of III-V laser cavities evanescently coupled to Si waveguides, with CW electrical pumping and reduced dimensions [25][26][27][28]. Particularly, in [27], they show a very interesting solution with a microdisk radius of 7.5 μm and laser threshold current of 0.5 mA (at 1.65 V) emitting at 1600 nm. While the footprint falls into

the requirements for on-chip and intra-chip optical interconnect, the biasing electrical power still is in the mW range and the resulting output optical power is quite low (few μW), rendering the device inefficient from the energetic point of view.

Microrings and microdisks represent a good step forward for the development of micro/nanolaser sources. They enable an easy interfacing between active material and passive circuitry, CW electrical injection and room temperature operation. Additionally, their dimension is highly reduced with respect to DFB lasers, increasing their integration capacity. On the other hand, they still present sections on the μm^2 order, increasing the needed amount of power to light them up.

The next laser families we are going to talk about represent another step ahead to the conception of nanolaser devices: in fact, their footprint goes down to the sub-μm scale, with reduced parasitic capacitances (leading to high driving speeds) and reduced bias power, thanks to a higher light-matter interaction.

The first family is the metallic laser cavities one.

1.4.1.3 Metallic laser cavities

A metallic laser cavity presents a particular design with respect to conventional light sources. In fact, while in standard semiconductor lasers the metal contacts are located far from the emission regions to prevent parasitic absorption, metallic nanolasers pave the way to the quest for miniaturization, presenting nm-scale active materials with metal contacts placed very close to the cavity. Thanks to these nanolasers it is possible to confine light in ultra-small volumes, approaching or even surpassing the diffraction limit (plasmonic nanolasers). Metallic cavities do not present high quality factor Q (ratio between the energy stored in the cavity and the energy lost), due to the very close metals, but they allow to increase considerably the confinement factor (overlap between cavity mode and gain material). The goal of this section is to analyze and discuss the main improvements done so far for these devices.

Hill et al [29] firstly demonstrated a metallic nanolaser cavity (Figure 10). It consists of a III-V nanopillar with diameter of 210 nm, heavily doped in order to constitute a P-i-N junction and encapsulated with a thin dielectric layer (10 nm of Si_3N_4) and gold (serving as N-contact). The P-contact is taken laterally with respect to the nanopillar. They could demonstrate laser emission at 1400 nm with CW electrical pumping and bias power smaller than 1 mW but at cryogenic temperature (77 K). As mentioned in this section's introduction, such a structure presents low quality factor (Q = 180 at room temperature) but a high confinement factor (Γ = 0.43), permitting to achieve laser emission cooling down the structure.

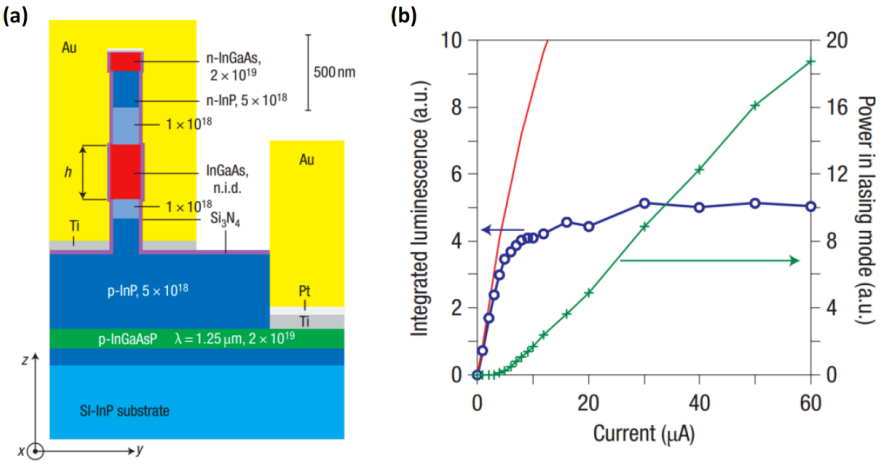


Figure 10: (a) encapsulated nanopillar schematics and (b) corresponding laser characteristics at 77 K [29]

An improved version of their work [30] shows laser emission at 1591 nm with a CW electrical bias but this time at room temperature. Such an improvement has been obtained by fabricating the nanopillar with a rectangular shape instead of a cylindrical one and by substituting gold with silver to reduce absorption. On the other hand, the bias power to obtain laser emission this time is above 1 mW, since the operating temperature is no more cryogenic.

In [31], a metallic-coated disk with volume of 3 μm^3 has shown laser operation at 1515 nm with very similar CW electrical injection power and cryogenic temperature as [29].

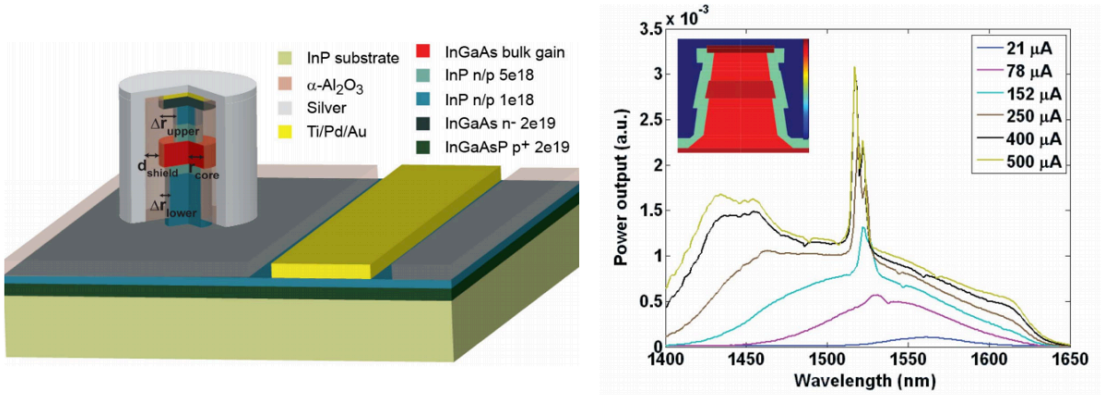


Figure 11: on the left, schematics of the metallic-coated disk; on the right, output laser characteristics [31]

Starting from 400 μA of injected current, we can clearly see the appearance of an additional cavity mode.

So far we have discussed about metallic nanolaser reducing the modal volume to the diffraction limit $(\lambda_0/2n)^3$, where λ_0 is the resonant wavelength and n is the cavity's material refractive index. There is a class of nanolasers that is able to reduce even further the cavity dimension, surpassing the diffraction limit: the plasmonic metallic cavities (or Spasers).

The spasers have been demonstrated for the first time in 2009 [32][33][34].

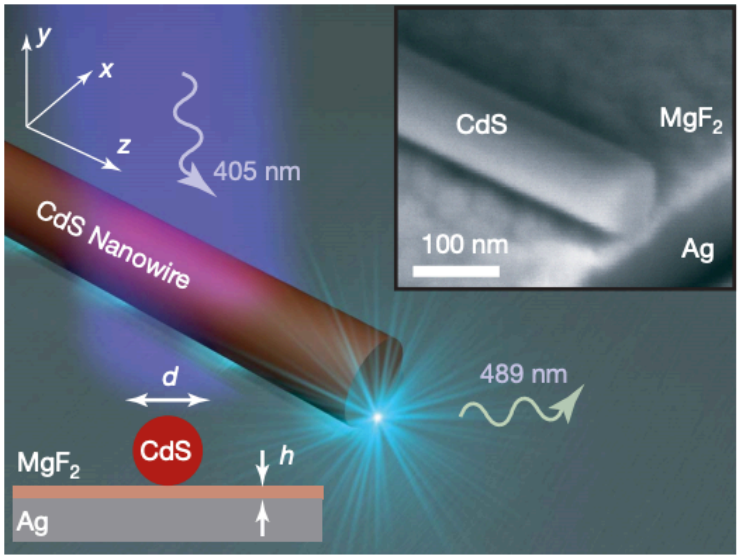


Figure 12: Plasmonic nanowire 3D schematics from [32]

While [32] shows laser emission in the visible range (490 nm) at 10 K and with pulsed optical pumping, in [33] they demonstrate laser emission at room temperature, under the same pumping regime. However, in [34] laser emission is obtained with CW electrical pumping, even if another time at 10 K.

However, surface plasmons are a very recent research subject, where many different architectures are proposed (see [35-44]).

We have seen that metallic cavities can concretely reduce the nanolaser footprint down to the diffraction limit, or even surpass it. We have also presented some interesting works where the lasing regime has been obtained with an electrical injection scheme: particularly, in [30] they achieve it at room temperature. The main advantage of such structures is the extremely small footprint, giving rise to unprecedented confinement factors (between 25% and 45%); on the other hand, the metals are deposited in close proximity to the active region, causing huge absorption and a dramatic Q reduction. That is why at room temperature all these nanolasers

register relatively high pumping power, exceeding 1 mW. Additionally, the small Q poses serious doubts about a possible integration of such nanolasers onto a silicon-based platform: in fact, such a hybrid structure would result in highly inefficient coupling between the cavity and the Si bus waveguide.

After the discussion about metallic cavities, it is time to introduce and comment the second family fitting into the definition of nanolaser: the Photonic Crystal (PhC) lasers.

1.4.1.4 Photonic crystal lasers

Photonic Crystals have been firstly theorized by Yablonovitch and John [45][46]. They showed that in 2D or 3D superlattices it was possible, by properly choosing the geometrical parameters, to open a frequency window in the structure's band diagram where the light propagation was forbidden: it is the so-called photonic band gap. Such an achievement opened the road for the realization of brand new laser cavities, where the light was trapped in ultra-small volumes, approaching the diffraction limit $(\lambda_0/2n)^3$. A more detailed theoretical analysis of PhCs will be presented in the next chapter.

During years, many technological advancements allowed to improve PhC performances: in fact, it has been possible to reduce the laser size and threshold, as well as to obtain CW optical pumping at room temperature. Particularly, to achieve these milestones, a key role has been covered by improving surface treatment techniques: surfaces, in fact, are trap states sources for carriers, causing a dramatic reduction of radiative emission effiency. Smoother surfaces, obtained by more controlled etching processes as well as chemical treatment to clean and passivate them, allowed to improve more and more PhC lasers performances [47-54].

However, in order to exploit nanolaser cavities for real on-chip applications, one of the major requirement is the presence of an electrical injection scheme. In the next section, we will analyze and compare the work published so far showing electrically driven PhC nanolasers.

1.4.1.5 Electrically driven PhC lasers

The very first demonstration of an electrically pumped PhC laser has been made in 2004 [55]. It consists of a "mushroom-like" membrane made in a vertical P-i-N junction for the carriers' electrical injection (Figure 13). The cavity is placed right in the center of the membrane, taking advantage of a point defect in the 2D-PhC holes' array. The holes' (charges) injection is achieved through the mushroom stem, while the N-metal is placed on the membrane circumference. Laser emission has been obtained at room temperature, at 1520 nm, under AC electrical biasing. Despite the very fancy design and the incredible achievement of a working electrical injection scheme, such a device cannot be exploited for communication systems, for the complex interfacing with passive silicon circuitry, the impossibility to drive it with DC bias and the small output power (few nW).

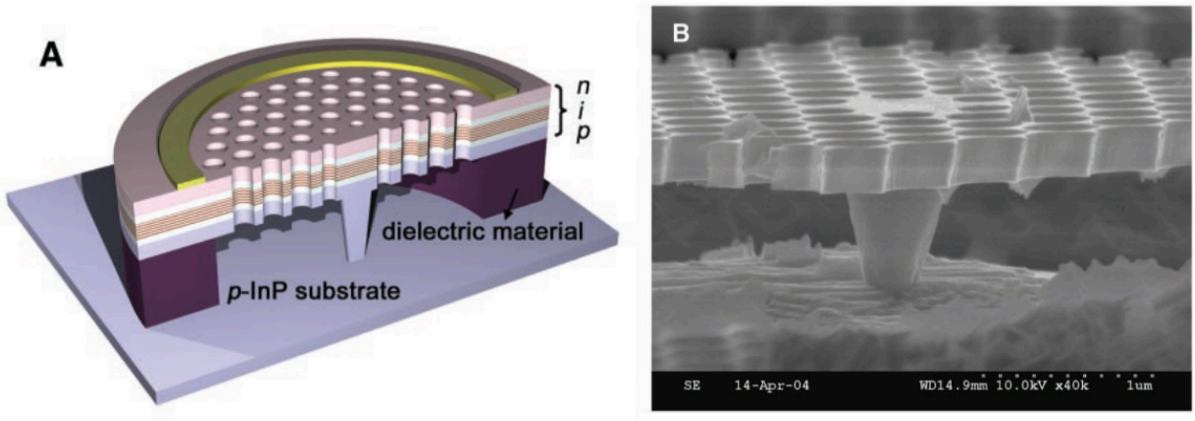


Figure 13: (A) schematics of the mushroom-like membrane; (B) SEM picture of the fabricated device [55]

In 2011, Jelena Vuckovic's group in Stanford, in collaboration with Berkeley University published a quantum dot-based PhC nanolaser in GaAs pumped by a lateral P-i-N junction formed by ion implantation [56].

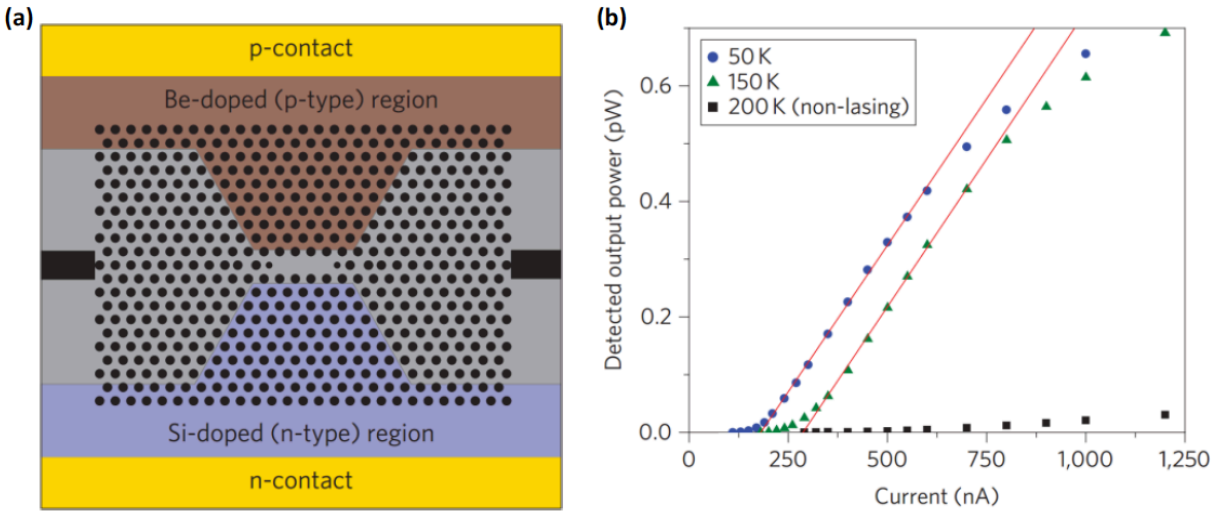


Figure 14: (a) schematics top-view of the PhC laser proposed by [56]; (b) output signal characteristics for different environmental temperatures

The laser emission was attained with a very low threshold current and with CW electrical pumping, but at cryogenic temperatures (Figure 14-(b)).

In 2013, the same group as of [55] proposed another electrically driven nanolaser [57]: this time the geometry consisted of a suspended nanobeam (1D) PhC cavity, contacted from the bottom with the same idea as for the mushroom stem (Figure 15).

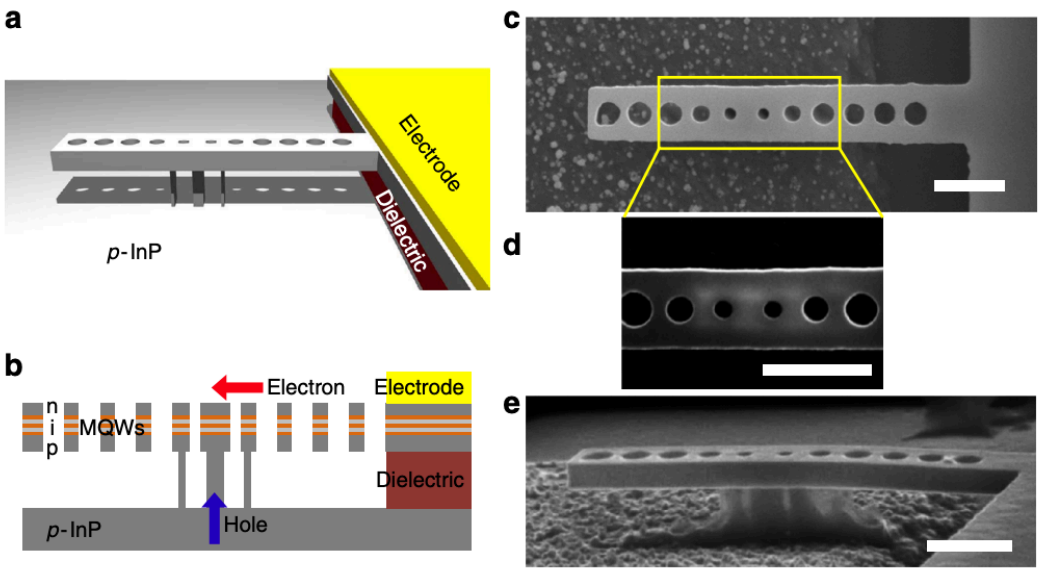


Figure 15: 3D-schematics of the suspended nanobeam; (b) cross-section schetamics of the nanolaser cavity; (c)(d)(e) SEM pictures of the fabricated structure [57]

Another time, their nanolaser showed laser emission at room temperature for pulsed electrical injection, but this time the laser threshold was more than one order of magnitude lower (around 4 μA).

A very interesting solution for integrated on-chip communication applications has been demonstrated by NTT Photonics Laboratories in 2013 [58]. Similarly to [56], the nanolaser relies on a lateral injection scheme, with doped region obtained by ion implantation. This particular structure relies on a complex technological know-how on epitaxy regrowth: in fact, they are able to localize the active region only in the central part of the structure (depicted in red on Figure 16). With such a design, they obtained laser emission for a CW electrical injection at room temperature, with a laser threshold of 5 μA and output laser power of few μW. Additionally, their device could be driven at 10 Gbits/s, with a power consumption estimated to be 4.4 fJ/bit. All these results are in good agreement with the required performances for a nanolaser to be considered for on-chip and intra-chip applications.

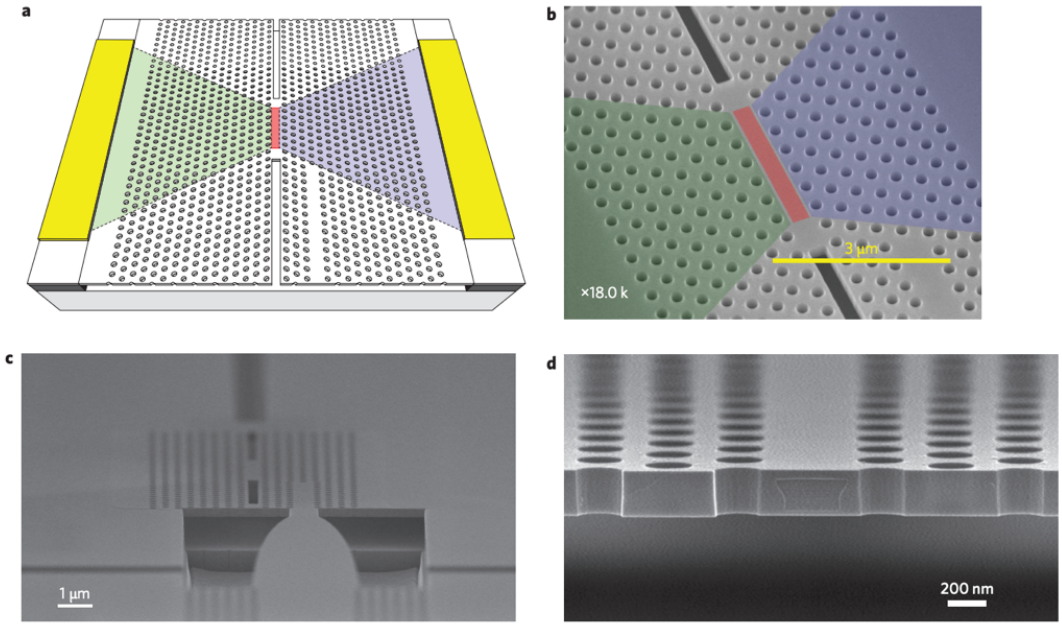


Figure 16: PhC nanolaser proposed by [58]. (a) 3D-schematics ; (b)(c)(d) SEM pictures of the fabricated structures (in green and violet are depicted the doped regions)

However, such a technological process flow poses some perplexities when talking about the nanolaser integration on a silicon-based platform: particularly, the PhC fabrication cannot be directly performed on a microelectronic circuit for the elevated temperature required for dopants activation, which is much higher than the maximum limit imposed by the CMOS technology (400°C).

The last work we propose in this state of the art section is the one published by my research group in 2017 [59], consisting of an electrically pumped PhC nanobeam cavity.

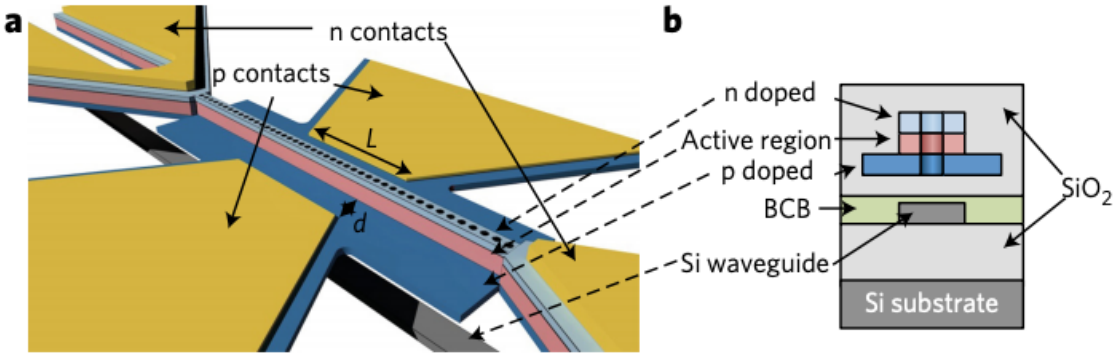


Figure 17: 3D-schematics (a) and cross section (b) of the nanobeam laser [59]

It consists of a 1D PhC cavity achieved thanks to Gaussian apodization (that will be treated more in details during next chapter). The electrical injection scheme consists of four pads (2 P-metals and 2 N-metals) properly designed in order to maximize the overlap between the optical mode and the injected electrical carriers (giving rise to optical recombination events). Moreover, the nanobeam presents an efficient evanescent coupling scheme with the silicon waveguide, allowing to extract the emitted laser from the cavity and transmit it through to the output of the circuit. As we can see from Figure 18, the nanolaser emits at 1560 nm at room temperature and with a DC electrical bias, showing a threshold current of 100 μA.

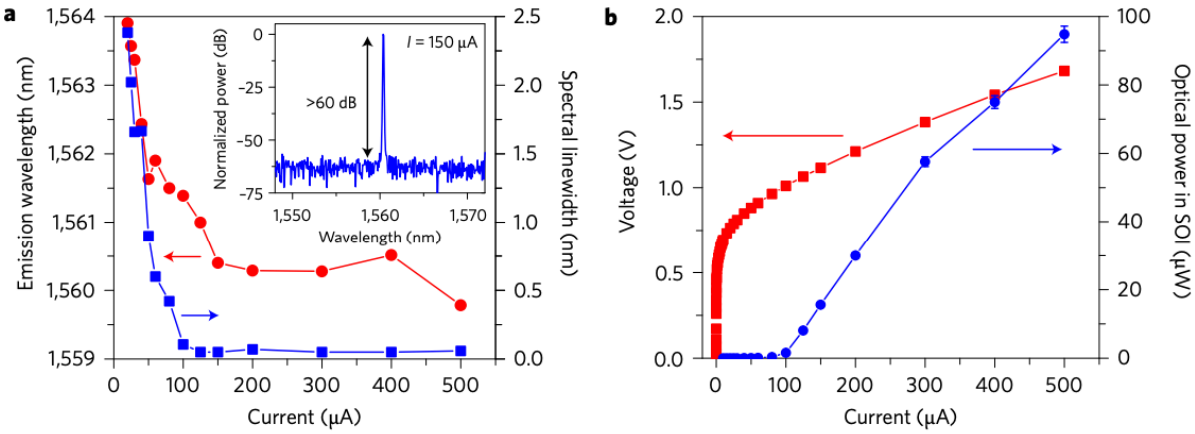


Figure 18: (a) emission wavelength and spectral linewidth values varying the injected current; (b) IV and laser characteristics [59]

The nanolaser is fabricated directly onto the Si circuitry after the adhesive bonding step, meaning that the process flow is CMOS compatible. According to our knowledge, this is the very first work showing a nanolaser structure validating all the requirements for a dense on-chip co-integration of electronic and photonic circuits.

Since their theorization, PhCs structures have been through immense improvements, both from theoretical and from technological point of view. Today, with the latest advances in the field, they seem to be the most mature technology for the convergence of microelectronics and nanophotonics, giving the possibility to achieve unprecedented performances in the field of Information Technology, both in terms of speed and power consumption.

1.5 Thesis context and goal

This PhD work was part of 2 European projects, ICT-STREAMS and HYPNOTIC ERC project. The goal of ICT STREAMS was to develop the necessary Silicon Photonics Transceiver and Routing

technologies towards a new, power efficient, WDM-based, Tb/s, optical on-board interconnection paradigm that enables multiple high bandwidth, point-to-point direct links on the board level, as a step forward to the realization of exa-scale computing systems. Particularly, the goal of this PhD project was to realize a PhC optical pre-amplifier stage at the front-end of the Photonic Transceiver's photodetectors. Our team was involved in this European project thanks to the very important results achieved in the past 15 years in the field of PhCs, where a technological know-how has been fully established for the conception and realization of hybrid III-V on SOI PhC nanocavities, both with optical and electrical pumping schemes.

This PhD also deals with the development of a novel type of nanolaser diodes exploiting 2D PhC (ERC HYPNOTIC) in order to take advantage of the simple electrical injection scheme and minimize the electrical resistance, which would lead to extremely-high driving speed and lower power consumption.

In summary, the goals of this PhD were:

- to design, both optically and electrically, a bidimensional Photonic Crystal (2D-PhC) device integrated on a silicon passive circuit and adapt it to achieve laser emission and light amplification;
- to fabricate the designed structures, optimizing each step of the process flow to obtain a final chip as close to the ideal simulated one as possible;
- to characterize the fabricated samples from the electrical and the optical point of view.

1.5.1 Thesis structuration

This manuscript is composed by 5 chapters. The first one, which is about to end, is the introduction, where we put in context the domain and commented the research state of the art on devices.

The second chapter will deal, firstly, with a theoretical introduction of PhC structures, discussing the main properties and specificities. Then, the design and modeling of the 2D-PhC nanoamplifier will be extensively explained from an optical and electrical point of view, showing the theoretical performances it can achieve. Eventually, we will comment a possible nanoamplifier optimization, talking about slow-light regime and its implementation in such a device.

Chapter 3, will be focused on the design and modeling of the same 2D-PhC structure but for the conception of a laser source, introducing the *gentle confinement* principle, allowing us to achieve a nanolaser cavity with high quality factor and small modal volume (close to the diffraction limit). The theoretical performances will be then listed and discussed.

In chapter 4, we will describe the fabrication of the 2D-PhC nanoamplifier and nanolaser structures integrated on the SOI platform. We will show the great advances we made on the

conception of a CMOS-compatible technological process flow, reducing further the vertical distance between active III-V devices and passive silicon circuitry with respect to previous work of our team [71].

The fifth chapter will be devoted to the characterization of the fabricated structures, commenting the achieved results. Finally we will conclude this PhD thesis by discussing the future work.

Chapter 2: The PhC nanoamplifier

In this chapter, we will focus our attention on the first device studied during the PhD: the PhC nanoamplifier. Firstly, we will give a general introduction to PhCs, describing their most important characteristics, followed by the electro-optical design and the theoretical study of our PhC based amplifier. Eventually, the chapter will conclude with some the future work, talking about slow-light regime, which would allow a further reduction of the device's footprint.

2.1 Photonic crystal: general introduction

A Photonic Crystal is a structure in which there is a periodic variation of the refractive index (RI) at the wavelength scale in one, two or three dimensions of space. It is the photonic analogue to atomic lattices in solid state physics, where the dielectric constant corresponds to the atomic potential. The main properties of a PhC are determined by its band diagram: it represents the optical mode frequencies as a function of the wavevector [60]. By managing the structure's opto-geometrical parameters (lattice configuration and RI), it is possible to obtain a photonic band-gap, which is a range of frequencies in which the propagation of light is forbidden in all directions. This is due to constructive and destructive interferences phenomena inside the periodic structure. In Figure 19 it is possible to observe an example of a photonic band structure.

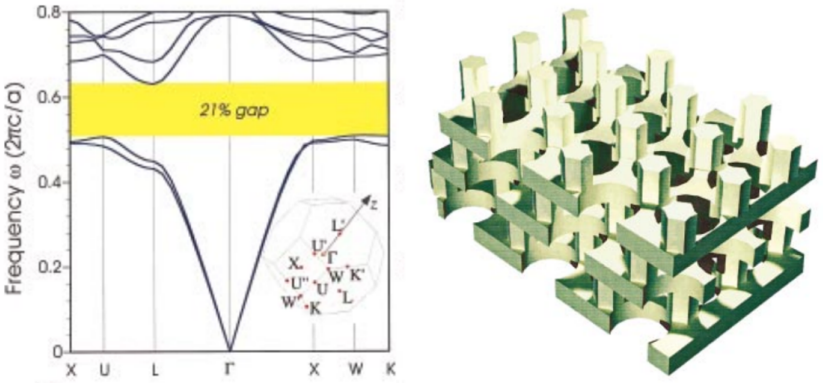


Figure 19: On the left, band structure of a 3D Photonic Crystal; in yellow, we can appreciate a Photonic Band Gap. On the right, schematic representation of the PhC from [60]

In order to obtain the photonic band diagram it is sufficient to solve Maxwell's equations and apply the Bloch's theorem [61]. Taking advantage of the structure's periodicity, the band structure is typically traced only in the first Brillouin zone ($0 < |k| < \pi/a$). The frequencies corresponding to a purely real wavevector constitute the PhC propagative modes. On the other hand, there are optical modes associated to frequencies with imaginary wavevector showing an exponentially decreasing electromagnetic (EM) field amplitude during propagation: this range of frequencies constitutes the photonic band-gap.

PhCs are a very versatile structures, offering different advantages: one of the most remarkable properties is their ability to confine the light in very small volumes of material, close to the diffraction limit ($V \sim (\lambda_0/2n)^3$). This is typically achieved combining the control of light propagation induced by the PhC structuration and Total Internal Reflection (TIR). This allows 3D confinement even using unidimensional (1D) and bidimensional (2D) PhCs drilled in semiconductor membranes. For a better description of the work developed during this PhD, in the next section, we will focus our attention on bidimensional PhCs, giving a general introduction and describing their main properties.

2.1.1 2D-PhC: introduction

As mentioned in the previous lines, a 2D-PhC membrane is a structure confining light in two dimensions taking advantage of the photonic band diagram properties, while in the direction normal to the plane of periodicity light is trapped thanks to TIR. Figure 20 shows a general schematic of a 2D-PhC.

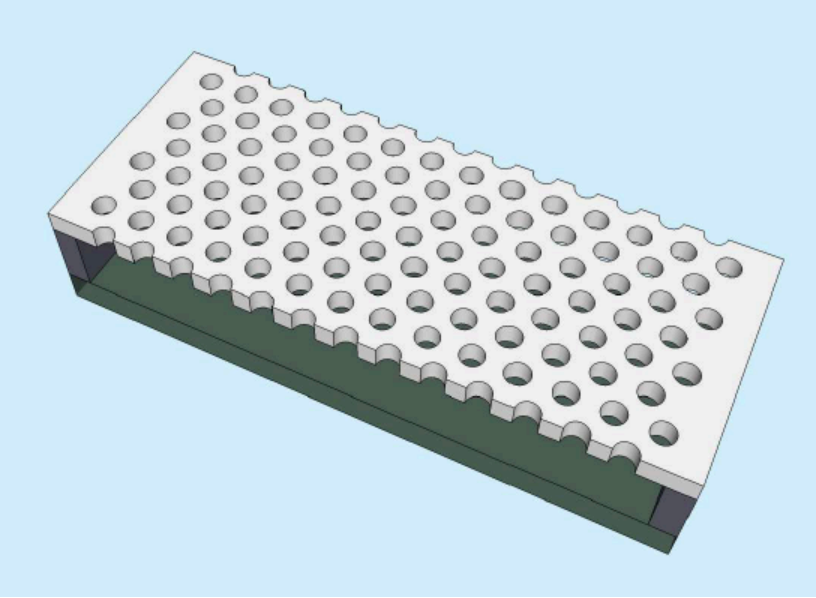


Figure 20: Typical schematics of a 2D-PhC membrane

The plane of periodicity is defined by drilling holes periodically in the membrane, alternating in that way a high RI material (typically a semiconductor) with a low RI one (air or silica). To fully describe the band structure of a 2D-PhC membrane (represented in Figure 21) we have to take into account also the so-called light-cone. This cone materializes in the band structure the leaky modes which are not fully confined in the PhC membrane. In this region, the TIR condition is not fulfilled and light is radiated in the surroundings of the structure.

The PhC modes which are confined by TIR obey to the following relation:

$$\omega < \frac{c\,|k_{//}|}{n_2} \tag{2.1}$$

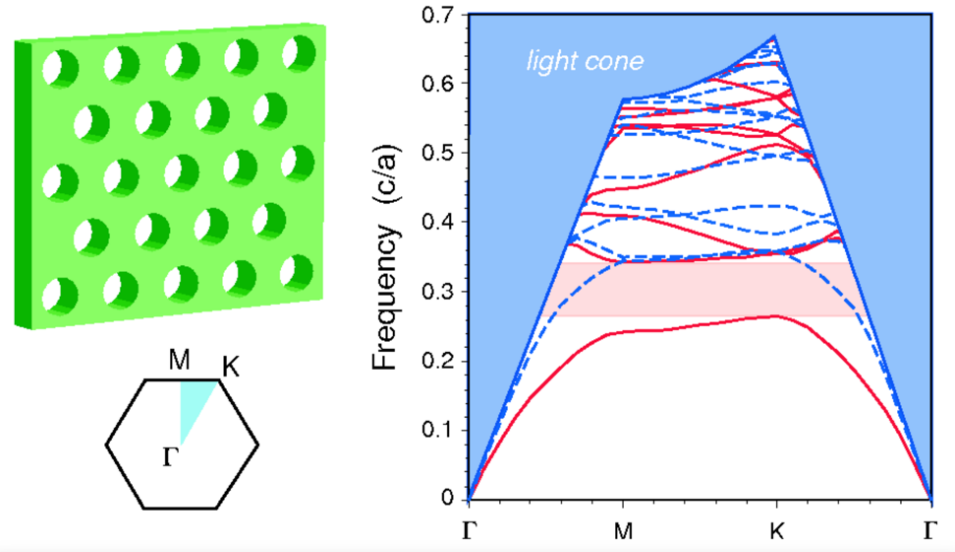


Figure 21: Photonic band diagram of an infinite 2D-PhC membrane composed by a triangular lattice of air holes etched in a dielectric slab. The blue area is the light cone, the modes which are not confined in the PhC membrane and which get radiated in air. The red solid lines and blue dashed ones represent the modes that remain confined in the slab: the formers with TE-like and the latters with TM-like polarization. As we can observe, it exists a band gap only for TE-like modes (shaded red region) [62]

Where $k_{//}$ is the wavevector component parallel to the plane of periodicity and n_2 the RI of the material surrounding the PhC membrane. A very interesting property of 2D-PhC membranes is that we observe the appearance of a photonic band gap only for TE-like polarized modes (Electric field (E_{field}) parallel to the plane of periodicity - shaded red area), while not for the TM-like ones (E_{field} orthogonal to the plane of periodicity). Such a property will be discussed more in details later in this manuscript, as it has fundamental importance for the design of the nanoamplifier and the nanolaser cavity.

The main interest of PhCs is that, by creating a local defect in the periodic pattern it is possible to create "trap states" inside the photonic band gap: in that way, resonant cavities [63] as well as waveguides [64][65] are created by a point (e.g. one hole removed) or a linear (an entire row of holes removed) defect in the PhC pattern (Figure 22).

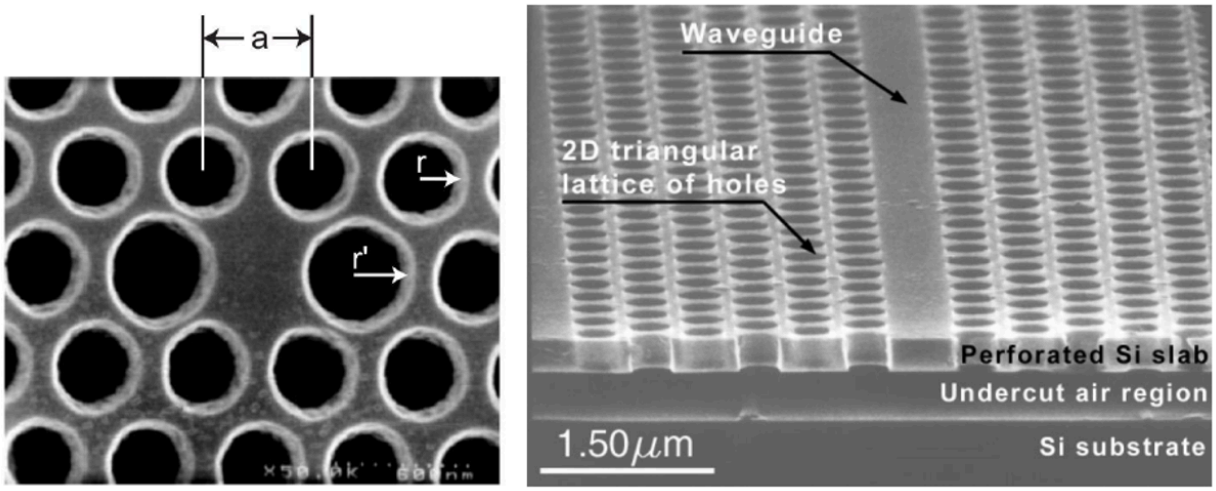


Figure 22: Examples of single defect (on the left) [66] and linear defect (on the right) [65] in a 2D-PhC membrane

During the PhD, the work has been focused on the study of devices with a linear defect in the PhC periodic pattern. In the next section we will comment the general properties of a 2D-PhC membrane with a missing row of holes.

2.1.2 2D-PhC with linear defect

We have seen in Figure 21 that if we deal with an infinitely large 2D-PhC membrane there is a range of frequencies where the light propagation is forbidden in the plane of periodicity (photonic band gap below the light cone). If we move further and we remove a single row of holes from the periodic pattern, we will observe, along the missing row direction, the appearance of new photonic bands: we can analyze an example of such a band structure in Figure 23. In this graph, we are referring to TE-like modes (E_{field} in the plane of periodicity and orthogonal to the waveguide direction). Λ represents the period of the triangular lattice of holes defining the PhC (schematics shown in the inset). The large grey surfaces are the 2D-PhC slab modes: if we select frequencies and wavevectors falling in these areas, we refer to optical modes whose propagation is allowed inside the periodic pattern. In between the two grey surfaces, we can observe the 2D-PhC band gap: along the linear defect direction (depicted as z in this example), the light propagation is forbidden inside the holes pattern.

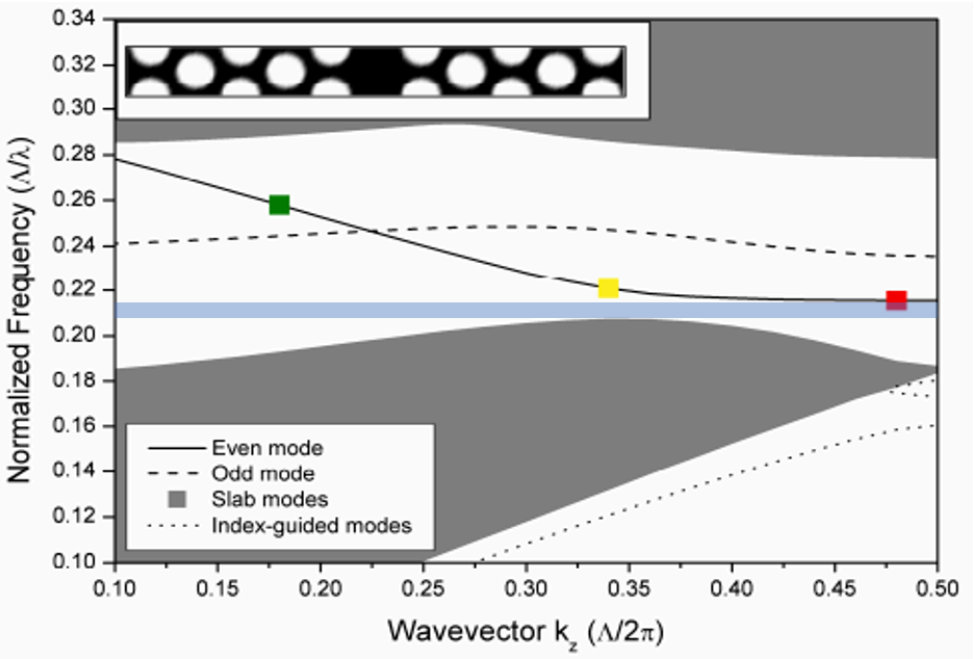


Figure 23: Typical example of band diagram for a 2D-PhC with a linear defect [67]

Moreover, with the introduction of a linear defect we can observe the creation of new bands: the index-guided bands (underneath the bottom slab modes), traced with dotted lines, and the gap-guided bands, placed inside the photonic band gap and drawn with a solid line and a dashed one. To describe their meaning, let us start with the band diagram analysis for the light propagation in a homogeneous unidimensional medium.

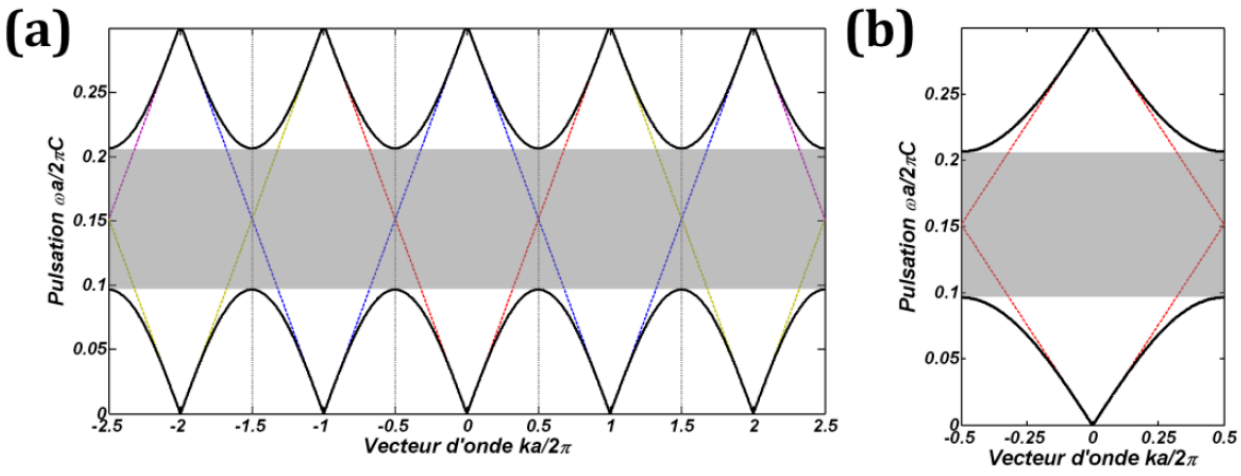


Figure 24: (a) band diagram for a uniform 1D material (dotted lines) and for a 1D material where the RI is perturbed with a period "a" (black-solid lines); (b) representation of the same band diagram restricted to the 1st Brillouin zone

The dispersion relation states that the pulsation of an optical mode is:

$$\omega(k) = \frac{c|k|}{n} \tag{2.2}$$

where c is the speed of light, k the wavevector and n the RI of the considered material. In Figure 24 this relation is represented by the dotted lines. If we introduce a perturbation with a defined periodicity "a" to the RI (in the case of our PhC, drilling holes in the homogeneous medium), we can notice a folding of the bands at every wavevector corresponding to $k = {}^{m\pi}/_{a}$ (m being an integer constant), with the opening of a band gap. Additionally, thanks to the Bloch theorem, we can state that the solutions for each wavevector k are repeated with a periodicity of 2π:

$$\omega(k) = \omega\left(k + \frac{2m\pi}{a}\right) \tag{2.3}$$

which gives us the freedom to analyze just the 1st Brillouin zone to fully describe the solutions of our system (Figure 24-b).

If we focus our attention to the positive k solutions in the 1st Brillouin zone, introducing a periodic perturbation to the RI we break the degeneracy of the homogeneous medium solution, giving rise to interference phenomena between propagative (bottom band) and counter-propagative (top band) optical waves [68]: this results into a folding and a separation of the bands, creating a band gap.

We can observe similar phenomena occurring in a PhC line-defect waveguide as it can be seen, in first approximation, as a step index waveguide surrounded by a periodic structure inducing distributed feedback. Looking at Figure 23, the index guided and the even gap guided modes originate from the folding of the fundamental mode of the waveguide at the edge of the 1st Brillouin zone. The former mode does not fall inside the 2D PhC band gap but possesses a wavevector larger than that of the slab modes. At these frequencies, the 2D PhC lattice acts as a metamaterial (effective medium) of low RI enabling TIR at the interfaces with the line defect. The gap guided mode falls within the band gap meaning that the PhC structures act as mirrors confining light in the line defect. This mode exhibits a unique property close its cut off frequency: a low group velocity regime of propagation, or slow light. This behavior stems from the anticrossing of the waveguide fundamental mode with the slab modes. In addition, an odd mode also appears in the PhC band gap.

Finally, we can observe on Figure 23 that there is still a range of frequencies (highlighted in blue) where the light propagation is prohibited along the linear defect direction: we will show that such a band gap will be fundamental for the conception of our nanolaser cavity. To conclude, by applying a linear defect to a 2D-PhC membrane we enable the creation of new bands, giving us the possibility to trap light inside the defect and guide it either exploiting TIR (index-guided band)

or the 2D-PhC band gap (gap-guided band). In both ways, light is confine in very small volumes, approaching the diffraction limit and responding to the specifications a nanophotonic device requires (small footprint, small energy consumption and high-speed).

We are now ready to start the discussion about the design of the first device conceived during this PhD: the PhC nanoamplifier.

2.2 Nanoamplifier: general description

In modern PIC an amplification stage is required. In fact, the quest for power consumption and footprint reduction in photonic components has increased the need for signal power magnification and preservation along the whole circuit. There are three major situations where optical amplification might be needed, as it is shown in Figure 25.

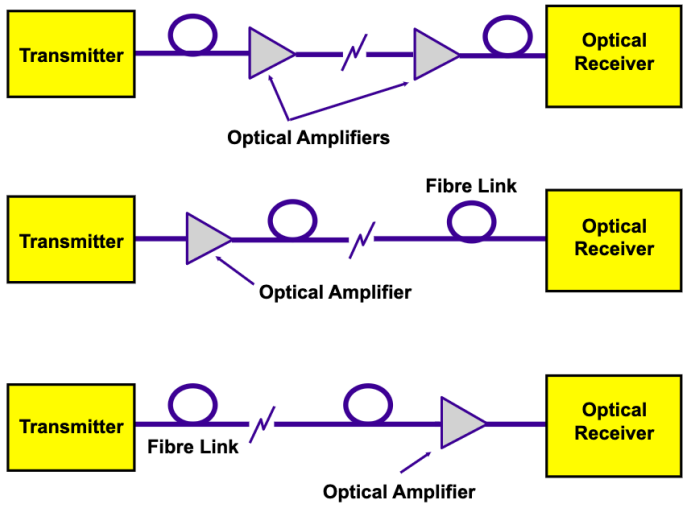


Figure 25: General scheme of an optical link. From top to bottom, we can see that an amplification stage is introduced as, respectively, an in-line amplifier, a booster amplifier and a pre-amplifier

The case represented on the top-scheme takes typically place on long-distance application rather than on-chip ones. In this context, optical links transferring data over hundreds of kilometers require in-line amplification stages to recover the power level previously attenuated during signal transmission; a widely used solution for such application is the Erbium Doped Fiber Amplifier (EDFA). However, in this manuscript we want to focus our attention to PICs, which means that we are referring to the center- and bottom-scheme of Figure 25. The former acts as a booster amplifier: according to the circuit's specifications, the signal generated by the laser source may present an inadequate power level and may require a boost for a correct deployment throughout

the whole circuit. The latter, instead, is used as a pre-amplification stage before the receiver part, with the goal to increase the photodetector's Signal to Noise ratio (S/N) and, consequently, its sensitivity.

2.2.1 State of the art SOA: general schematics

As we have discussed in the introduction, state of the art SOAs present lengths on the mm order of magnitude and consume several hundreds of mW to attain amplification levels of at least 10 dB. One of the main limitations comes from their large footprint: as depicted in Figure 26, the general approach is to electrically bias the device with a vertical injection scheme. On top of the III-V P-i-N junction waveguide there is the P metal, while the N-doped layer is contacted laterally. However, metallic contacts present high optical absorption, which could lead, if they are placed in too close proximity to the optical mode, to signal attenuation. Consequently, the P-doped layer is grown thick enough to prevent this kind of losses.

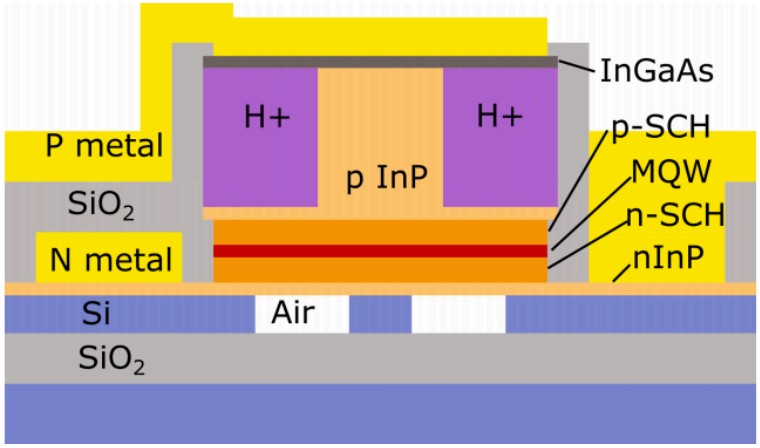


Figure 26: Typical schematic cross section of a heterogeneous SOA waveguide [69]: starting from the bottom we have the passive circuitry made on SOI with the III-V membrane bonded on top. We can distinguish the different doped layers composing a P-i-N junction, with the MQW active material falling inside the intrinsic part

At the same time, such a thick III-V membrane (several µm) represents a limitation for the device's miniaturization. This is easily understandable by analyzing the optical gain expression.

2.2.1.1 Gain per unit length derivation

Let us consider an optical wave propagating through the waveguide of the example above. The equation expressing the power variation during transmission is the following:

$$\frac{dP}{dx} = (\Gamma g(N) - \alpha)P(x) \tag{2.4}$$

Where x is the direction of propagation, $g(N)$ the material gain depending on the amount of injected carriers N (varying with the pumping level), α the coefficient linked to photon losses (free-carrier absorption in the doped regions and loss due surface roughness for example) and Γ is the confinement factor, expressing the overlap between the guided mode and the active region. This parameter plays a key role in the conception of optical amplifiers: in fact, even if the material used for the active region nominally provides high gain, it is fundamental that the propagating optical mode's shape fits as good as possible with the active region (Quantum Wells or Quantum Dots), providing gain. The smaller this parameter is, the longer the waveguide will be in order to attain a certain level of amplification. Since the optical mode's and the active region's shape remain unvaried along the whole amplification region, we can calculate the confinement factor considering just the EM field and the waveguide composition in the transverse plane. Supposing that the active region is formed by n layers of active material contributing to the gain, of surface S_i (with i ranging from 1 to n) in the cross section, we can mathematically define the confinement factor as:

$$\Gamma_{yz} = \frac{\sum_{i=1}^{n} \iint_{S_i} |E(y,z)|^2 dzdy}{\iint_{yz} |E(y,z)|^2 dzdy} \tag{2.5}$$

From now on we will omit the subscript "yz" from the confinement factor in the equations, knowing that we will always refer to the cross-section overlap between the EM field and the active material. Moving back to the transmission equation, we can set the material gain g, for simplicity, as linearly dependent from the carriers' density [70]:

$$g = \sigma(N - N_{tr}) \tag{2.6}$$

where σ is the material's differential gain, defined as $\sigma = {}^{dg}/_{dN}$ (expressing the gain variation as a function of the carrier density injected in the active region, N) and N_{tr} is the carrier density at transparency, representing the amount of carriers to inject in the active region in order to obtain an unvaried output optical power with respect to the input one, separating the absorption ($g < 0$) and gain ($g > 0$) regimes. Substituting it into the differential equation we have as a solution that the power in the propagating optical mode varies with an exponential law:

$$P(x) = P_0 e^{(\Gamma\sigma(N-N_{tr})-\alpha)x} \tag{2.7}$$

We obtain for the gain per unit length expressed in ${}^{dB}/_{cm}$:

$$\left.\frac{G}{cm}\right|_{dB} = \frac{10}{\ln(10)}(\Gamma\sigma(N - N_{tr}) - \alpha) \tag{2.8}$$

2.2.2 State of the art SOA: limited confinement factor

Let us consider the state of the art SOA example described in the introduction, by casting its geometry in the formula we just calculated. While this configuration surely reduces α, avoiding unwanted signal absorption from the top-metal, it limits Γ to rather small values (Figure 27).

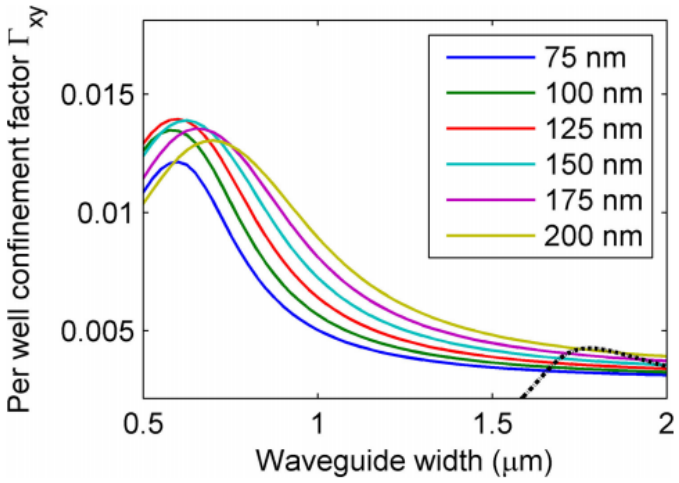


Figure 27: Per-well confinement factor versus waveguide width from [69]: the different colors represent different p-SCH and n-SCH thicknesses (see Figure 26), while the black-dotted line shows the confinement factor for the first higher-order mode in the 125 nm SCH case

As we can see, the per-well confinement factor roughly reaches 1.5% in the best case condition. This is due to the fact that the optical mode propagating in such a thick semiconductor structures is not tightly confined, which in turns dramatically reduces its overlap with the active medium. One way to overcome such a problem would be to integrate many Quantum Wells (ten or even more): however, even if the gain would be surely increased, so would be the power consumption, since a larger active volume requires more electrical power to inject the same carrier density. This is why such amplifiers are quit long.

The only solution to increase the confinement factor (and consequently the gain per unit length) without paying in terms of power budget is to scale-down the device's footprint in order to compress the optical mode's shape: it is in this context that the 2D-PhC structure comes into play.

2.3 2D-PhC: our structure

Our idea to improve the SOA performances in terms of length and energy consumption is the device's miniaturization. Consequently, we turned our attention to a nanophotonic solution: A

2D-PhC membrane exploited as an optical waveguide. The 3D-schematics of our device is represented in Figure 28. It consists of a hybrid structure interfacing a Silicon-based passive platform (with the silicon waveguide acting as a bus circuitry, driving the signal to the input of the amplifier and extracting it at its output) with an active III-V membrane bonded on top, designed to work as a 2D-PhC waveguide amplifier. The exploited active material is made of Multiple Quantum Wells (MQWs). During this PhD we worked with signals in the C band telecom window (~1.55 µm): thus, we used InP-based III-V heterostructures.

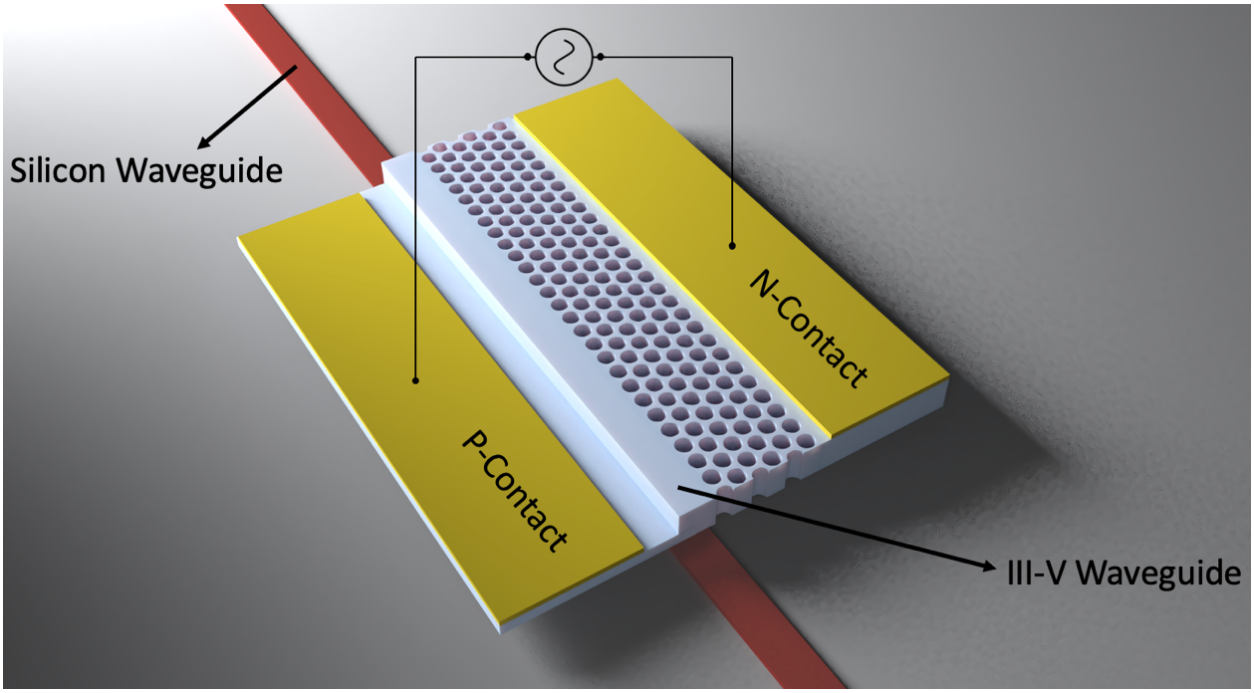


Figure 28: general 3D-schematics of our 2D PhC nanoamplifier

As we can see, the optical waveguide is constituted thanks to a linear defect in the bidimensional pattern of holes: in that way, while the optical signal propagates through the waveguide, it gets amplified as well, thanks to the presence of the active material. The specificity of our structure is that we do not use a regular linear defect within the holes' pattern, but we implement it on the edge of the periodic pattern creating an asymmetric waveguide. Consequently, the signal is trapped inside the waveguide due to TIR in the vertical direction and on the P-contact side and thanks to the 2D-PhC on the other side. The reason for such an asymmetric geometry has to do with the injection of electron-hole pairs: we will see later that, with this configuration, the electrical carriers are properly injected inside the waveguide region, interacting efficiently with the optical propagating mode. The cross-section of the structure is represented in Figure 29.

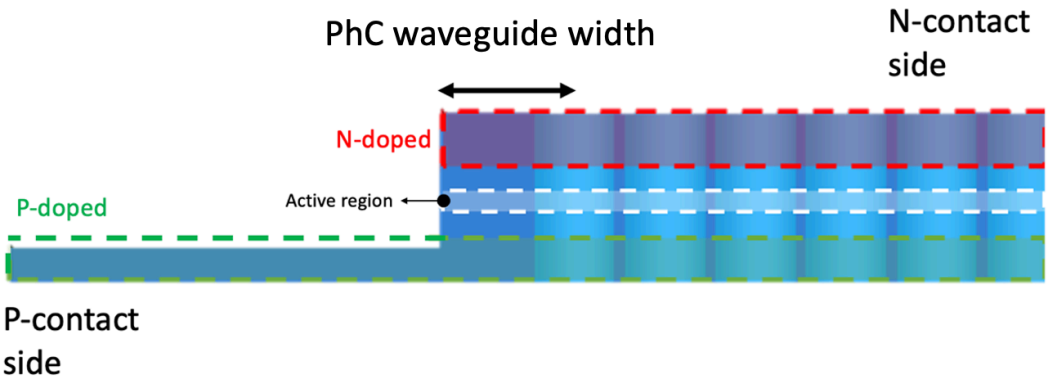


Figure 29: Cross-section schematics of the PhC nanoamplifier

Our III-V membrane forms a P-i-N junction: on the left of the PhC waveguide we etch the heterostructure down to the P-doped layer in order to contact it with metal (P-contact), while on the right the holes are etched through the whole membrane. At the right extremity, another metal is deposited to create the N-contact. Before recombining in the intrinsic region, electrons and holes undergo a horizontal diffusion inside their respective layers of origin: that is why we refer to this configuration as a lateral electrical injection scheme. Consequently, metals are not placed on the top or on the bottom of the amplifier waveguide avoiding absorption: we are free, then, to minimize the III-V membrane thickness.

2.3.1 Hybrid structure: general parameters

At the beginning of this project, the choice of the active membrane's parameters followed the great results obtained during Guillaume Crosnier's PhD work [71]. The membrane thickness was fixed at 450 nm. In Table 1, we indicate the grown materials' electro-optical parameters.

Material	Thickness (nm)	Doping concentration (cm^{-3})	Optical refractive index
i-InP	10	n.i.d.	3.1872
P-InGaAsP	100	P (Zn) $-$ $2 \cdot 10^{18}$	3.3
i-InGaAsP	47.75	n.i.d.	3.3
$\times 5$ { i-InGaAsP_QB	15.5	n.i.d.	3.3
i-InGaAsP_QW	6.3	n.i.d.	3.4
i-InGaAsP	63.25	n.i.d.	3.3
N-InP	120	N (Si) $-$ $2 \cdot 10^{18}$	3.1872
TOTAL	450		

Table 1: III-V membrane's electro-optical parameters

Concerning the passive circuitry, we based our study referring to Silicon On Insulator (SOI) substrates we firstly bought from the Institut de Microélectronique Et Composants (IMEC) and then from the University of Southampton's Cornestone foundry. We always exploited substrates with single mode silicon waveguides, measuring 220 nm in thickness and with widths ranging from 400 nm to 600 nm in steps of 50 nm. The choices of the higher and the lower limits were dictated by two reasons: the maximum width was not exceeding 600 nm so to keep the waveguides single mode, while the lower limit was set to 400 nm in order to keep propagation loss sufficiently low.

In order to confine an optical signal with a wavelength of 1550 nm inside the PhC waveguide, we design the periodic pattern so that this wavelength falls inside either the index-guided or the gap-guided band of the photonic band diagram. We firstly started exploiting the index-guided band, as shown in Figure 30. The chosen PhC parameters to obtain such a band structure were:

- periodicity $\mathrm{a} = 260\ \mathrm{nm}$;
- holes' radius $\mathrm{r} = 100\ \mathrm{nm}$;
- PhC waveguide width $\mathrm{wgw} = \mathrm{a}\sqrt{3} = 450.3\ \mathrm{nm}$.

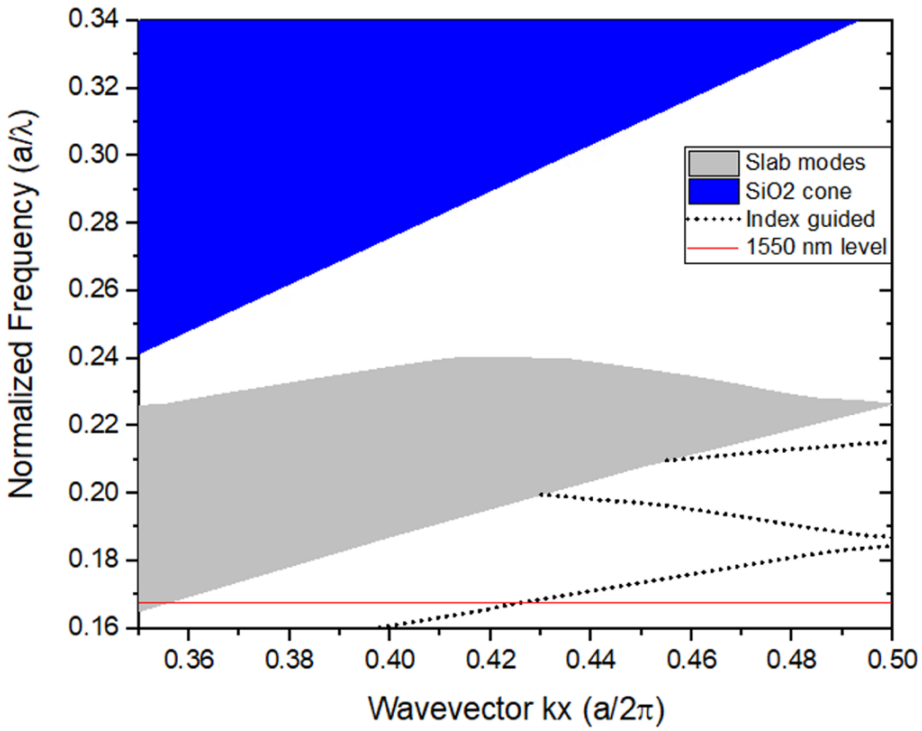


Figure 30: Band diagram of our PhC nanoamplifier. The grey surface represents the PhC slab modes, the blue one the SiO_2 light cone, the red horizontal line 1550 nm and the dotted lines the index-guided bands of the PhC waveguide

From this band diagram we can understand that light propagating inside the PhC waveguide with a wavelength of 1550 nm sees an effective index n_{eff} higher than the slab modes.

Up to now we have described the general properties of the active part of the device; now, it is fundamental to conceive an optimal optical interfacing between the passive circuitry and the nanoamplifier, in order to efficiently inject light coming from the bus silicon waveguide inside the III-V waveguide. In the next section, we will analyze the designed coupling schemes.

2.4 Mode converters

From Figure 28, we can see that our hybrid device is composed by a silicon waveguide with the III-V nanoamplifier bonded on top. What we want to achieve is a full transfer of light from the silicon waveguide to the PhC one at the nanoamplifier's input, while at its output we want to perform the exact opposite transition with the amplified signal. We need, then, to conceive efficient mode converters.

2.4.1 Evanescent wave coupling

The coupling between the two levels is realized taking advantage of evanescent wave coupling. As indicated by its name, this coupling mechanism exploits the evanescent tail of propagating modes to transfer light from one waveguide to the other.

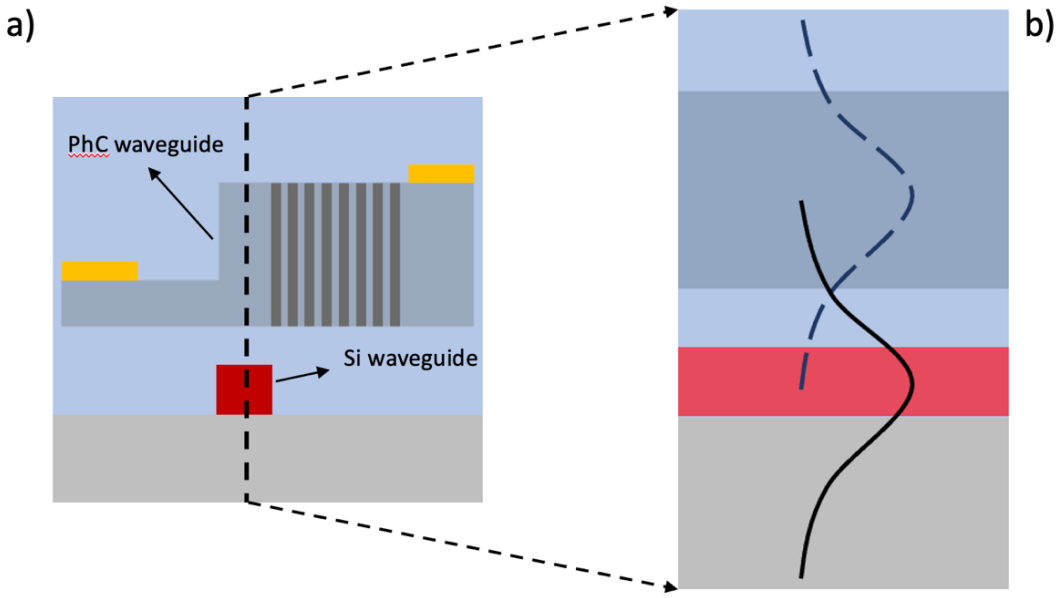
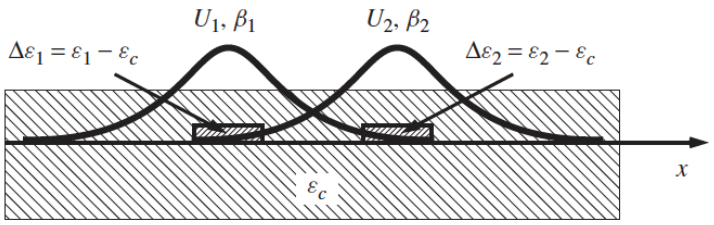


Figure 31: a) cross-section schematics of the hybrid III-V on Silicon device; b) longitudinal cut of the two waveguides, extracted from the dashed line of a). We can see the overlap between the PhC waveguide mode (dashed-blue curve) and the Si waveguide one (black curve)

As seen previously, when an optical mode is confined by TIR inside a waveguide, it presents a real wavevector's parallel component $k_{//}$ also called waveguide's propagation constant, defined as $\beta = n_{eff}\frac{2\pi}{\lambda}$: n_{eff} is the effective refractive index and λ the wavelength. Moreover, the perpendicular wavevector component $k_{\perp}$ is fully imaginary: it translates the EM field's exponential decreasing behavior inside the low-index surrounding material. If now we consider two waveguides close enough to each other as shown in Figure 31, the evanescent tail of each mode penetrates into the core of the other waveguide: in that way, we can state that the two waveguides are coupled to each other. The coupling strength is determined by the coupling coefficient κ: this parameter is proportional to the overlap between the two modes. Particularly, it is possible to demonstrate that, in a system with two waveguides coupled to each other, we have [21]:



$$\kappa_{12} = \frac{\kappa_0^2}{2\beta_1}\frac{\int_{G1}(\varepsilon_1 - \varepsilon_c)U_1^* \cdot U_2 dA}{\int |U_1|^2 dA} \tag{2.9}$$

$$\kappa_{21} = \frac{\kappa_0^2}{2\beta_2}\frac{\int_{G2}(\varepsilon_2 - \varepsilon_c)U_2^* \cdot U_1 dA}{\int |U_2|^2 dA} \tag{2.10}$$

Where $\kappa_{12,21}$ are the coupling coefficients expressing respectively the coupling strength to transfer a mode propagating inside waveguide-2 to waveguide-1 and vice versa, κ_0 is the propagation constant of the electromagnetic field in the vacuum, $\beta_{1,2}$ and $U_{1,2}$ represent respectively the propagation constants and the eigenmodes of two waves propagating inside waveguides 1 and 2 in an unperturbed scenario (uncoupled waveguides), $\varepsilon_{1,2,c}$ are the permittivity associated to the two waveguides and the cladding material and eventually $G_{1,2}$ represent the waveguides cross-sectional area. Additionally, an average coefficient for asymmetric waveguides (as in our system) can be defined:

$$\kappa = \sqrt{\kappa_{12}\kappa_{21}} \tag{2.11}$$

It has been demonstrated [72] that the spatial evolution of two optical waves a_i propagating inside two waveguides with propagation constant β_i and close enough to be coupled can be expressed as:

$$a_1(x) = \left(a_1(0)\left(\cos(\beta_0 x) + j\frac{\beta_1 - \beta_2}{2\beta_0}\sin(\beta_0 x)\right) + \frac{\kappa}{\beta_0}a_2(0)\sin(\beta_0 x)\right)e^{-j\frac{(\beta_1+\beta_2)x}{2}} \quad (2.12)$$

$$a_2(x) = \left(a_2(0)\left(\cos(\beta_0 x) + j\frac{\beta_2 - \beta_1}{2\beta_0}\sin(\beta_0 x)\right) + \frac{\kappa}{\beta_0}a_1(0)\sin(\beta_0 x)\right)e^{-j\frac{(\beta_1+\beta_2)x}{2}} \quad (2.13)$$

Where:

$$\beta_0 = \sqrt{\left(\frac{\beta_1 - \beta_2}{2}\right)^2 + |\kappa|^2} \quad (2.14)$$

Let us now consider these two equations for our case: at $x = 0$ we have the optical mode only in the silicon waveguide (i.e., $a_2(0) = 0$) and we want to fully transfer it into the active level. The waves' expressions become:

$$a_1(x) = a_1(0)\left(\cos(\beta_0 x) + j\frac{\beta_1 - \beta_2}{2\beta_0}\sin(\beta_0 x)\right)e^{-j\frac{(\beta_1+\beta_2)x}{2}} \quad (2.15)$$

$$a_2(x) = \frac{\kappa}{\beta_0}a_1(0)\sin(\beta_0 x)\,e^{-j\frac{(\beta_1+\beta_2)x}{2}} \quad (2.16)$$

And if we analyze the electromagnetic fields' intensity inside each waveguide we get:

$$|a_1(x)|^2 = a_1(0)^2\left(\cos^2(\beta_0 x) + \left(\frac{\beta_1 - \beta_2}{2\beta_0}\right)^2\sin^2(\beta_0 x)\right) \quad (2.17)$$

$$|a_2(x)|^2 = \frac{\kappa^2}{{\beta_0}^2}a_1(0)^2\sin^2(\beta_0 x) \quad (2.18)$$

We can notice that it is possible to play with the propagation constants in order to transfer light from one waveguide to the other: particularly, the smaller the propagation constant difference the better the signal is transferred. The full transfer can be achieved for $\beta_1 = \beta_2$, the so-called phase-matching condition: in such a situation, in fact, we have:

$$|a_1(x)|^2 = a_1(0)^2\cos^2(\kappa x) \quad (2.19)$$

$$|a_2(x)|^2 = a_1(0)^2\sin^2(\kappa x) \quad (2.20)$$

This means that, depending on the phase fixed by κx, we have a full mode transfer from one waveguide to the other and vice versa. It is interesting to highlight that the higher the coupling coefficient is, the shorter the distance to achieve a full transfer becomes.

2.4.2 Smooth light transfer: effective index difference

Going back to our system, since our ultimate goal is the device's miniaturization, it is clear that we want to transfer light from the bus waveguide to the PhC one in the shortest distance. Additionally, we do not want the optical power to oscillate back and forth from one waveguide to the other as it is the case when the system is invariant in the longitudinal direction. Our goal is to design a coupler converting the mode confined in the SOI waveguide into the mode propagating inside the PhC. To do so, as we will see, we engineered two different types of mode converters or tapers (linear and adiabatic). The general idea is to vary the difference of the waveguides propagation constant ($\Delta\beta = \beta_2 - \beta_1$) as a function of the propagation distance in order to smoothly transfer light from one waveguide to the other. More precisely, we can vary one of the PhC waveguide's geometrical parameters in order to increase its propagation constant (β_2) while maintaining fixed the silicon waveguide's one (β_1). Starting from $\beta_2 < \beta_1$ at the beginning of the taper, phase matching condition is gradually achieved by modifying the PhC waveguide. The taper is finished in a configuration where $\beta_2 > \beta_1$, preventing light to couple back to the SOI waveguide. One of the simplest ways to design an efficient taper for our nanoamplifier is to increase the waveguide width along the taper's length. Figure 32 shows the effective index variation of the TE mode propagating inside the PhC waveguide, for different waveguide widths. The working wavelength is set to 1550 nm.

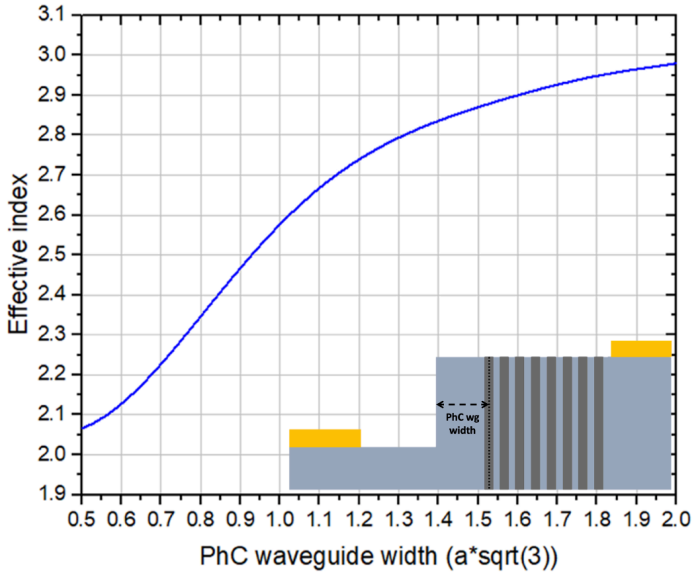


Figure 32: PhC waveguide n_{eff} as a function of the waveguide width, with $a = 260$ nm

In the same way, we plot, on Figure 33, the TE mode effective index as a function of the silicon waveguide width. Since the effective index range for the silicon waveguides is restricted between 2.21 and 2.56, it is understandable that a good compromise to smoothly transfer the signal from the silicon waveguide to the III-V one is to vary the taper n_{eff} from 2 to 3. This also will allow to achieve efficient coupling for silicon waveguides of different widths as shown later. This corresponds to vary the PhC waveguide width from $0.5 \cdot a\sqrt{3}$ to $2 \cdot a\sqrt{3}$ (i.e., from 225.2 nm to 900.7 nm).

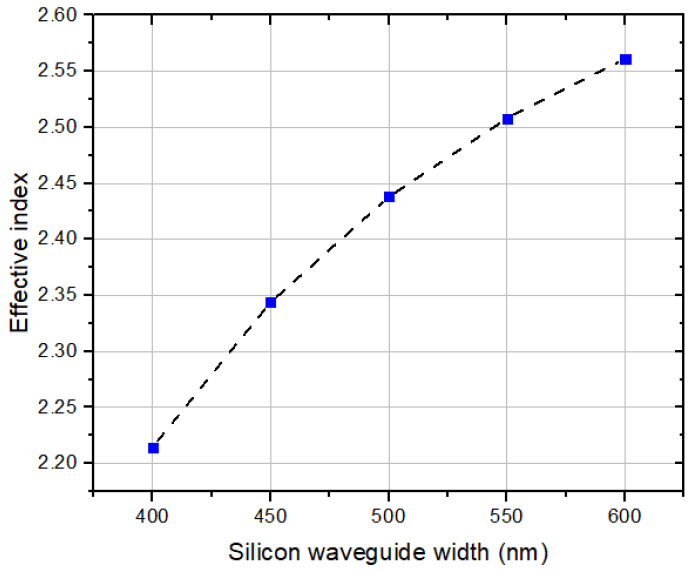


Figure 33: Silicon waveguides n_{eff} variation as a function of the waveguide width

Before describing the details of the tapers' design, the next section deals with an unexpected issue linked to the asymmetric nature of our PhC waveguide: the possible coupling between the SOI TE mode and the TM mode of the PhC.

2.4.2.1 TM-mode effective index limitation

One of the striking features of our PhC waveguide is its asymmetry. While in symmetric waveguides TE- and TM-like modes are orthogonal, it is not the case in asymmetric structures like ours, meaning that E_z is non zero for TE-like modes (E_y non zero for TM like modes). As the scalar product between electric fields inside equations (2.9) and (2.10) for TE-TM modes is non-zero, evanescent wave coupling can occur between modes of different polarizations. This must be avoided in order to maximize the coupling efficiency from the SOI waveguide TE mode to the PhC quasi TE mode. This is important as our active region composed of compressively strained

MQWs only amplifies light in TE-like modes. This can be done by ensuring along the taper structure that:

- at a fixed PhC waveguide width, the effective index of the TM like mode ($n_{eff,TM}$) in the PhC structure is always smaller than that of the TE-like modes ($n_{eff,TE}$) meaning $\beta_{2,TE} > \beta_{2,TM}$;
- phase matching condition is not achieved for the TM like mode in the PhC waveguide.

This means that we should always have $\beta_1 > \beta_{2,TM}$. Figure 34 shows n_{eff} of the TE an TM like modes of the PhC waveguide as a function its width (membrane thickness 450 nm).

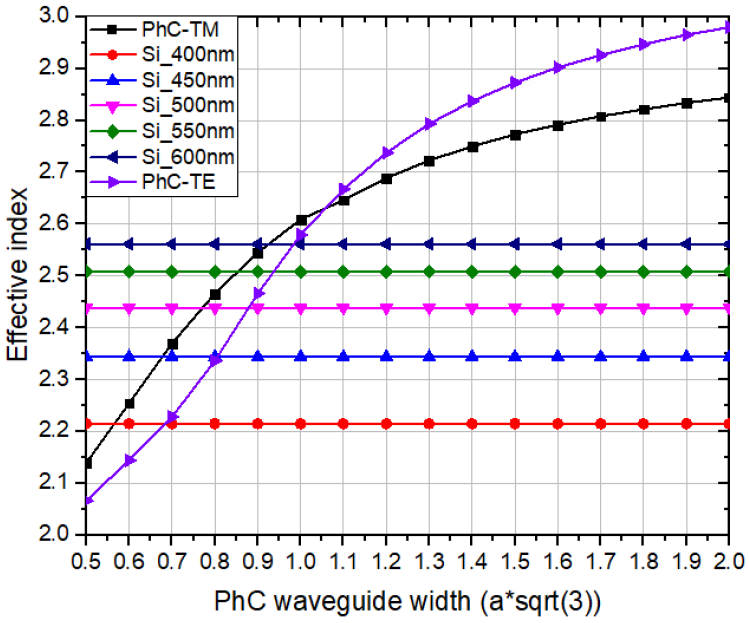


Figure 34: n_{eff} variation for TE and TM components vs PhC waveguide width; the constant values represent each silicon waveguide effective index

We can see that for widths under $a\sqrt{3}$, $n_{eff,TM}$ is always higher than $n_{eff,TE}$. Moreover, as the maximum achievable effective index for our SOI waveguides is 2.56 (width of 600 nm, thickness of 220 nm), phase matching condition will always occur for the TM mode at shorter widths than for the TE mode. This configuration is not at all favorable to achieve perfect coupling from a SOI waveguide to the PhC one.

2.4.2.2 Readapted III-V membrane

Following the previous reasoning, we modified the III-V material's parameters in order to obtain the desired situation. Particularly, we moved to a thinner membrane, whose parameters are listed in the next table.

Material	Thickness (nm)	Doping concentration (cm^{-3})	Optical refractive index
i-InP	10	n.i.d.	3.1872
P-InGaAsP	90	P (Zn) $-$ $2 \cdot 10^{18}$	3.3
i-InGaAsP	47.75	n.i.d.	3.3
i-InGaAsP_QB	15.5	n.i.d.	3.3
i-InGaAsP_QW	6.3	n.i.d.	3.4
i-InGaAsP	63.25	n.i.d.	3.3
N-InP	51.8	N (Si) $-$ $2 \cdot 10^{18}$	3.1872
TOTAL	350		

$\times 4$ { (i-InGaAsP_QB, i-InGaAsP_QW)

Table 2: Updated III-V membrane's electro-optical parameters

Concerning the PhC parameters, in order to keep working with the TE index-guided band, we fixed:

- periodicity $a = 240$ nm;
- holes' radius $r = 80$ nm;
- PhC waveguide width $wgw = a\sqrt{3} = 415.7$ nm.

Figure 35 shows the updated n_{eff} variation for the PhC waveguide's TE and TM modes.

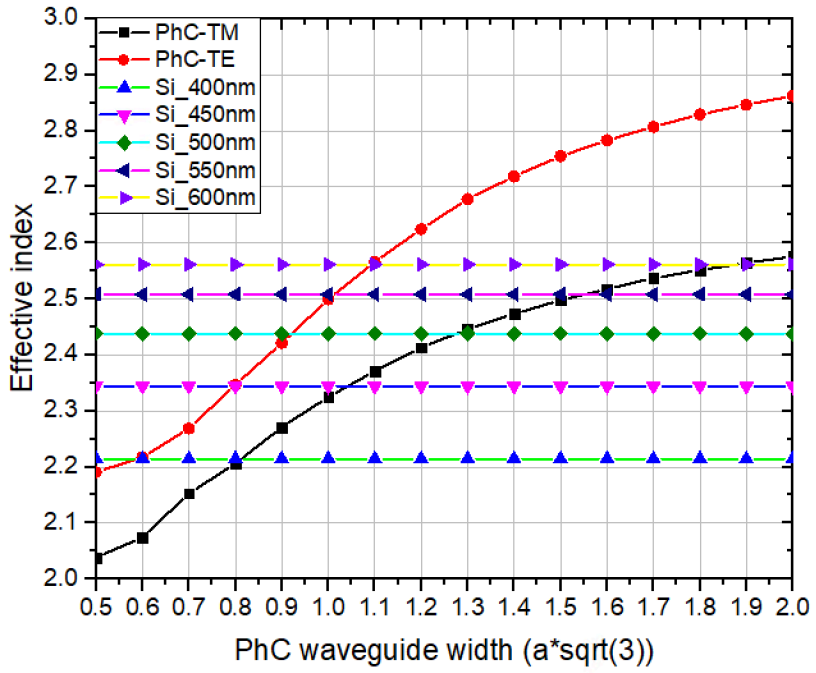


Figure 35: n_{eff} variation for TE and TM components vs PhC waveguide width with the updated membrane parameters; the constant values represent each silicon waveguide effective index

We can immediately see that this new PhC configuration is much better compared to the previous one: in fact, for every PhC waveguide width, $n_{eff,TE}$ is larger than $n_{eff,TM}$. Furthermore, for each silicon waveguide, it is possible to select a range of PhC waveguide widths where $n_{eff,TE}$ is varied from a smaller to a higher value with respect to the SOI waveguide mode $n_{eff,SOI}$, while keeping $n_{eff,TM}$ always smaller than $n_{eff,SOI}$.

Let us describe, as an example, the silicon waveguide width case of 600 nm: for the TE-like mode, phase-matching is achieved for a PhC waveguide width of around $1.1 \cdot a\sqrt{3}$, while the same condition for the TM-like component is satisfied increasing the PhC waveguide width up to around $1.9 \cdot a\sqrt{3}$. This means that, designing our mode converter, we are able to increase the PhC waveguide width above $1.1 \cdot a\sqrt{3}$ keeping it below $1.9 \cdot a\sqrt{3}$ in order to couple the light signal from the passive circuitry to a quasi-TE mode inside the nanoamplifier while minimizing the TM component.

In the next two sections, we will present the designed mode converters.

2.4.3 Linear taper

2.4.3.1 Design

The first coupler we designed was the linear taper. The starting point of this conception was to take into account the physical parameters of the hybrid heterostructure such as the thickness of the layers. Concerning the distance between the two waveguides, we faced a trade-off: while, on one hand, our wish was to maximize the coupling coefficient (minimizing consequently the vertical distance), on the other hand we were limited by fabrication constraints that we will discuss later in the dedicated chapter. Consequently, we set the vertical gap to 230 nm (top of SOI to bottom of III-V). As we will see more in details during the fabrication chapter, the materials used in between the III-V membrane and the silicon circuitry were a polymer called Benzoyclobutene (BCB), whose role was to stick together the active and passive levels of the hybrid device, and SiO_2, used for many reasons among which heat dissipation and improved adhesion provided for the adhesive bonding. Additionally, silica was also used as an encapsulation layer for the III-V structures. Of course, these materials are transparent in the telecom window around 1.55 µm.

In order to evaluate the linear taper efficiency, we performed optical simulations with the software *Lumerical FDTD Solutions* [73]. Such a software allows to solve the time-dependent Maxwell's equations discretizing them with a Finite-Difference-Time-Domain (FDTD) method.

As we have previously seen from the equations, in order to achieve a full light signal transition we need to attain the phase-matching condition ($\beta_1 = \beta_2$) between the coupled waveguides. Additionally, considering that once fully transferred the signal to the nanoamplifier we do not

want it to couple-back to the bus circuitry, we designed the taper so that its n_{eff} could reach values greater than the phase matching condition. As its name suggests, the idea behind the linear taper is to linearly increase the PhC waveguide n_{eff} by increasing its width, while the passive circuitry's n_{eff} is fixed. As discussed at the end of the previous sub-section, special attention has to be taken to avoid increasing too much the taper width, in order to limit the fraction of signal coupled into the TM mode. The silicon waveguides are terminated at the end of the coupling region with 10 μm long section where the width was linearly reduced to 250 nm, minimizing the silicon's n_{eff} preventing back reflections.

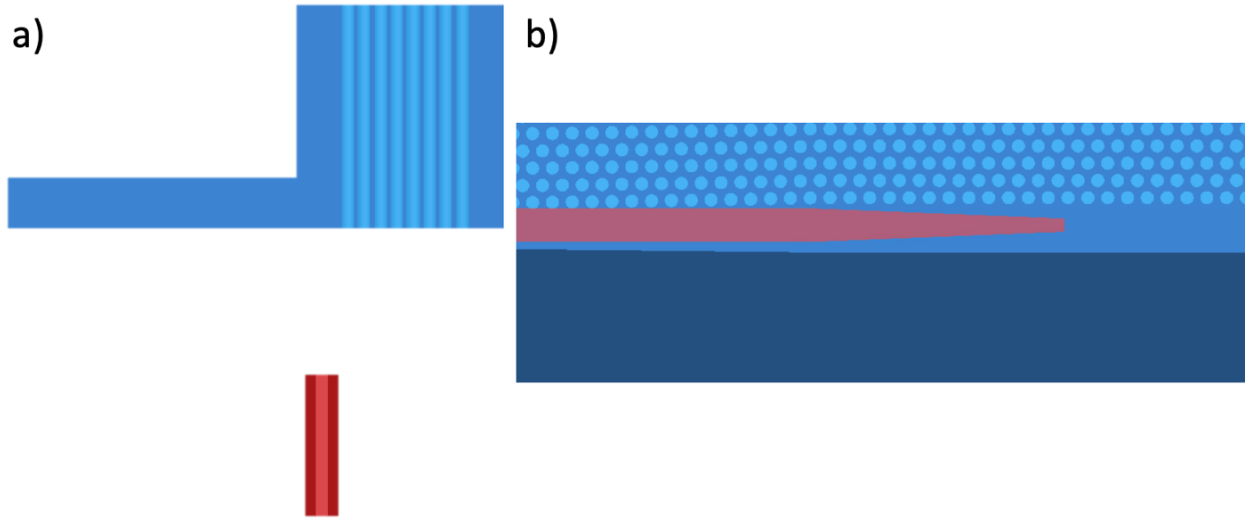


Figure 36: a) cross-section schematics of the hybrid system, with the nanoamplifier in blue and the silicon waveguide in red. b) top-view of the coupling region, with the taper in blue and the silicon waveguide in red (see-through view). We can appreciate the silicon waveguide termination with characteristic width reduction. Both schematics have been extracted from the FDTD simulation

We decided to vary smoothly the III-V taper effective index from $n_{eff}(Si) - 0.115$ to $n_{eff}(Si) + 0.115$ along the propagation distance. The last parameter to choose is the taper length, that we arbitrarily fixed at 100 μm to allow for an effective index variation as gentle as possible. The variation of the effective index as a function of the longitudinal distance is indicated on Figure 37 for different Si waveguides. The phase-matching condition is attained at half of the taper length (50 μm), apart from the case of the 400 nm wide silicon waveguide: there, the matching condition is achieved after a distance of 16 μm since the minimum amplifier waveguide width has been set to $0.5 \cdot a\sqrt{3}$, corresponding to an neff of 2.19. In fact, according to the rule we have fixed for the minimum PhC waveguide neff, we should have set it to 2.09, but no waveguide width has such a small index.

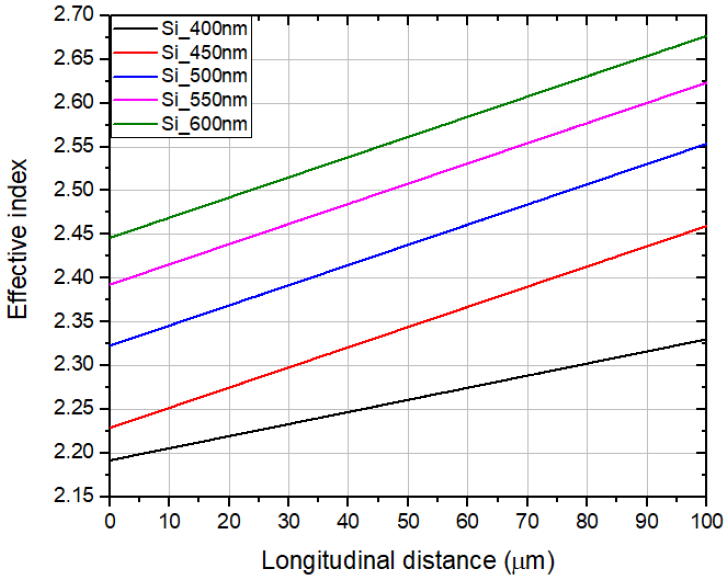


Figure 37: Amplifier taper's effective index variation for each silicon waveguide width case

Consequently, knowing the PhC waveguide's neff as a function of its width (Figure 35), we could design the linear taper adapting it to the available silicon waveguides.

2.4.3.2 Simulation results

Once all the geometrical parameters set, we performed FDTD optical simulations (Figure 38) in order to evaluate the performance of the designed linear mode transformer. A light source (fundamental mode) was inserted in the Si waveguide at a position where the PhC waveguide is absent.

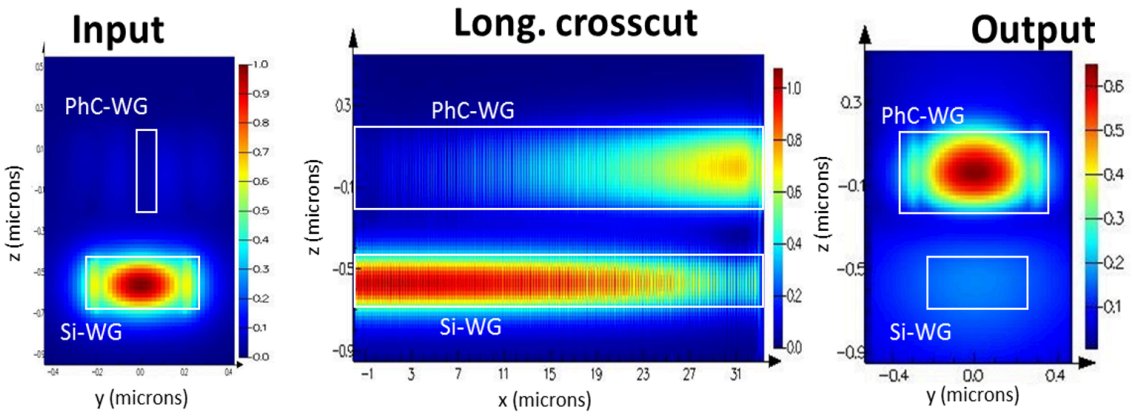


Figure 38: Extracted mode evolution for the designed coupling scheme: at the beginning, the signal is totally inside the silicon waveguide, while along the taper length it starts to be transferred inside the PhC waveguide due to the increasing effective index difference. Eventually, the mode is fully confined inside the PhC waveguide

As we can see, the mode is smoothly transferred from the silicon waveguide to the PhC one from the input (left picture) to the output (right picture). Let us now analyze the extracted coupling efficiencies for each silicon waveguide width case (Figure 39).

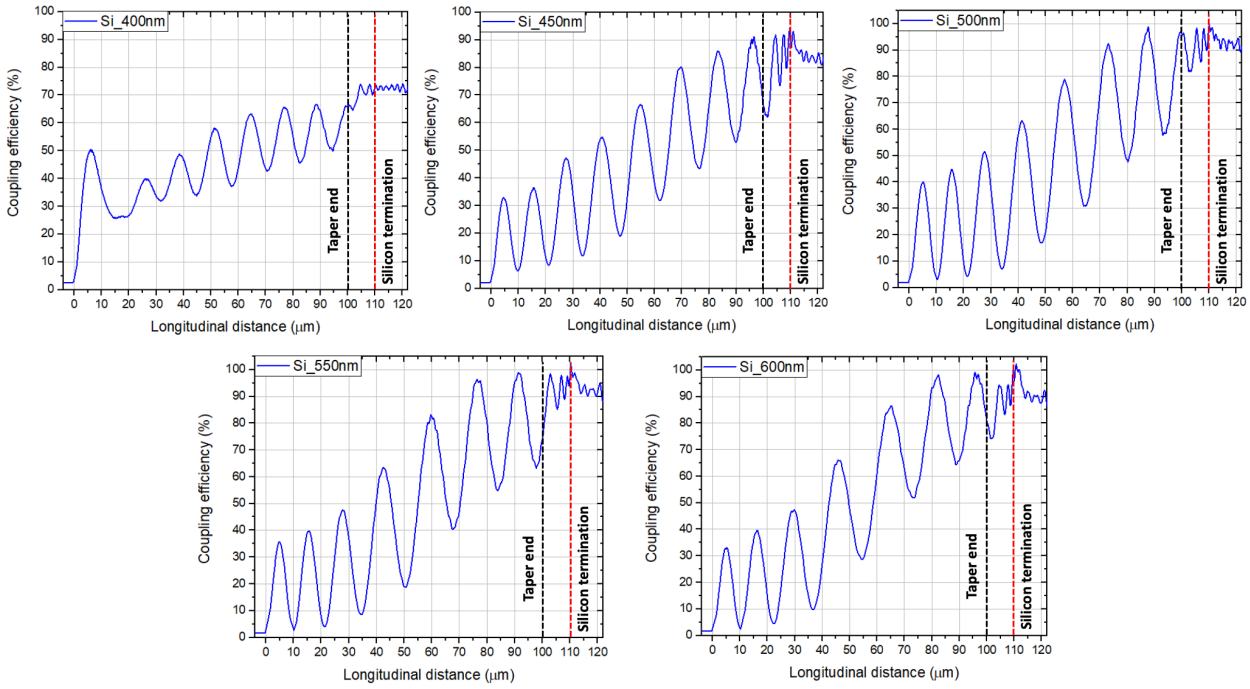


Figure 39: Coupling efficiencies for all the hybrid structures' linear tapers

For all the plots, the linear taper begins at $L = 0$ and finishes at $L = 100\ \mu m$. For $L > 100\ \mu m$, the width is fixed to that of $L = 100\ \mu m$. For the 400 nm case, we can notice that starting the taper with a width corresponding to an effective index close to the silicon waveguide, as explained before, has a negative impact compared to the other configurations. In fact, at $L = 0$ where the taper starts, the system abruptly changes form a Si waveguide to a coupled waveguides system where the eigenmodes share almost evenly optical power in the 2 waveguides. This results in signal diffraction due to mode mismatch and, consequently, losses. Additionally, the final taper's n_{eff} for the TE mode is 2.33, corresponding to a III-V waveguide width of $0.78 \cdot a\sqrt{3}$: as we can see from Figure 35, the TM mode's n_{eff} for such a width is smaller but very close to the silicon one (2.2 vs 2.21), preventing us from increasing even further the taper width. The resulting coupling efficiency is limited to 74% for this configuration. The 450 nm case improves the coupling efficiency: we get at the end of the taper a signal fraction of 85% coupled to the PhC waveguide. Another time the TM mode limits us in the taper maximum width choice, since its n_{eff} is quite close to that of the passive circuitry (2.29 vs 2.34). Moreover, we can

observe a signal reduction around $L = 110\ \mu m$: it corresponds to the silicon waveguide's termination area, causing a 6% drop of signal. We can actually remark that the latter happens for all the successive cases as well. This means that the way we terminate our Si waveguide should be rethought in order to obtain better results. Eventually, we can state that the best case conditions are the 500 nm and 550 nm cases, where we efficiently couple 95% of the input signal to the PhC waveguide. In the 600 nm configuration, again the abrupt ending of the Si waveguide induces a 10% loss signal, giving a coupling scheme transferring 90% of the input signal to the output. Moreover, the linear mode transformer's behavior has been studied for a range of wavelength between 1450 nm and 1650 nm, so to define the designed coupler optical bandwidth. As we can observe in Figure 40, where we show calculations for a 600 nm wide silicon waveguide, the coupling efficiency stays above 90% for wavelengths below 1625 nm. After 1625 nm, the efficiency drops due to the fact that the optical mode's propagation constant inside the PhC waveguide is reduced, turning into a less efficient signal coupling. Figure 40 tells us that the designed linear taper can be exploited to transfer light with an efficiency of 90% or more for an optical bandwidth of about 150 nm, which is a promising result for the conception of a nanoamplifier for integrated circuits applications.

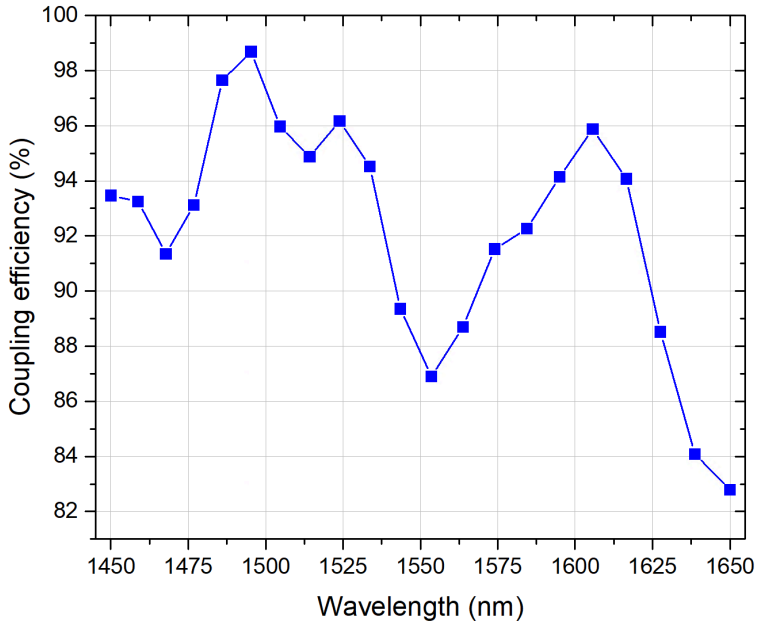


Figure 40: Linear mode transformer's optical bandwidth

The linear taper proved to be an efficient way to inject light inside the nanoamplifier. We will show, however, that we can transfer light in an even shorter distance while always maintaining high coupling efficiency by exploiting an adiabatic taper.

2.4.4 Adiabatic taper

2.4.4.1 Adiabaticity criterion

The design of the adiabatic taper has been inspired by [74]. The idea is to improve our linear taper design, minimizing its total length. In a system containing two coupled waveguides like ours, we firstly define a parameter ε, expressing the maximum fraction of power allowed to couple back and forth between the two waveguides. The adiabaticity criterion then states that:

$$\frac{1}{2\kappa(1+\gamma^2)^{3/2}}\frac{d\gamma}{dx} \leq \sqrt{\varepsilon} \tag{2.21}$$

Where κ is the waveguides coupling coefficient and $\gamma = {}^{\delta}/_{\kappa}$, with $\delta = {}^{(\beta_2 - \beta_1)}/_{2}$ expressing the propagation constants mismatch between the two waveguides. It follows that if we want to minimize the taper length we have to maximize the γ variation along x: this is possible only when the equality of (2.21) is verified. The solution for that equation then becomes:

$$\gamma = \frac{2\kappa\sqrt{\varepsilon}(x - x_0)}{\sqrt{1 - \left(2\kappa\sqrt{\varepsilon}(x - x_0)\right)^2}} \tag{2.22}$$

Which can be also written as:

$$n_{eff_{III-V}} = \frac{\lambda}{\pi}\frac{2\kappa^2\sqrt{\varepsilon}(x - x_0)}{\sqrt{1 - \left(2\kappa\sqrt{\varepsilon}(x - x_0)\right)^2}} + n_{eff_{Si}} \tag{2.23}$$

Where $n_{eff_{III-V}}$ is the PhC waveguide effective index, $n_{eff_{Si}}$ is the Si waveguide one, λ is the operating wavelength and x_0 is the phase-matching point position along the taper direction, where $n_{eff_{III-V}} = n_{eff_{Si}}$. For this expression to be valid, the term inside the square root has to be positive, meaning that:

$$-\frac{1}{2\kappa\sqrt{\varepsilon}} < (x - x_0) < \frac{1}{2\kappa\sqrt{\varepsilon}} \tag{2.24}$$

We can notice that when $x - x_0$ varies in this range, the effective index difference spans from $-\infty$ to $+\infty$: as a consequence, if we design a taper of length $L = {}^{1}/_{\kappa\sqrt{\varepsilon}}$ by increasing the PhC waveguide width as illustrated in the adiabaticity criterion solution, we are able to completely transfer an optical mode from the first waveguide to the other one, keeping the fraction of power coupling back below ε.

2.4.4.2 Design

Applying the adiabaticity criterion to our taper design is straightforward: we just need to arbitrarily set ε and calculate κ with FDTD simulations, according to our system's geometrical parameters. In that way, we obtain the taper length and the required $n_{eff_{III-V}}$ variation along the considered direction, translating it in the PhC waveguide width modification we have to apply to build the taper.

We performed FDTD simulations to extract the field profiles from all the previously analyzed silicon and PhC waveguides, calculating the coupling coefficients. In order to simplify our task, we determined the coupling coefficients at phase-matching (see Figure 41). The result highlights the fact that the more we increase the silicon waveguide width, the weaker the coupling strength becomes.

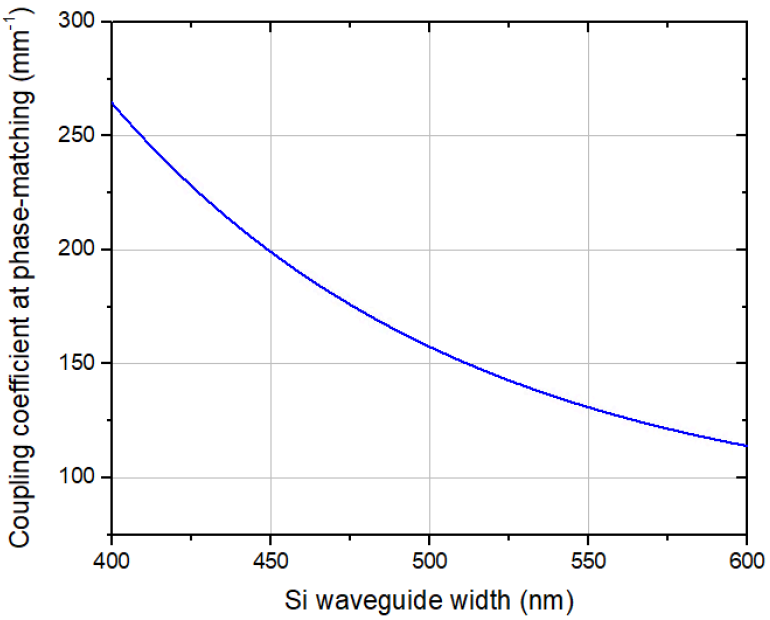


Figure 41: Coupling coefficients between PhC and silicon waveguides considered at phase-matching for each case

As we can clearly understand from this plot and recalling that the adiabatic taper length is fixed as $L = {}^{1}/_{\kappa\sqrt{\varepsilon}}$, the wider the silicon waveguide is, the longer the taper will be. The last parameter to set is ε: we decided to fix it to 0.02, meaning that we accepted maximum ripples of 2% of power coupling back and forth between the two waveguides at the taper's end. In our case due to the silicon waveguides termination, we did not observe such ripples.

Following the same reasoning as for the linear taper, we fixed the lower and the upper limits for the PhC waveguide effective index variation respectively to $n_{eff}(Si) - 0.115$ and $n_{eff}(Si) + 0.115$: Figure 42 shows such a variation obtained using the adiabaticity criterion.

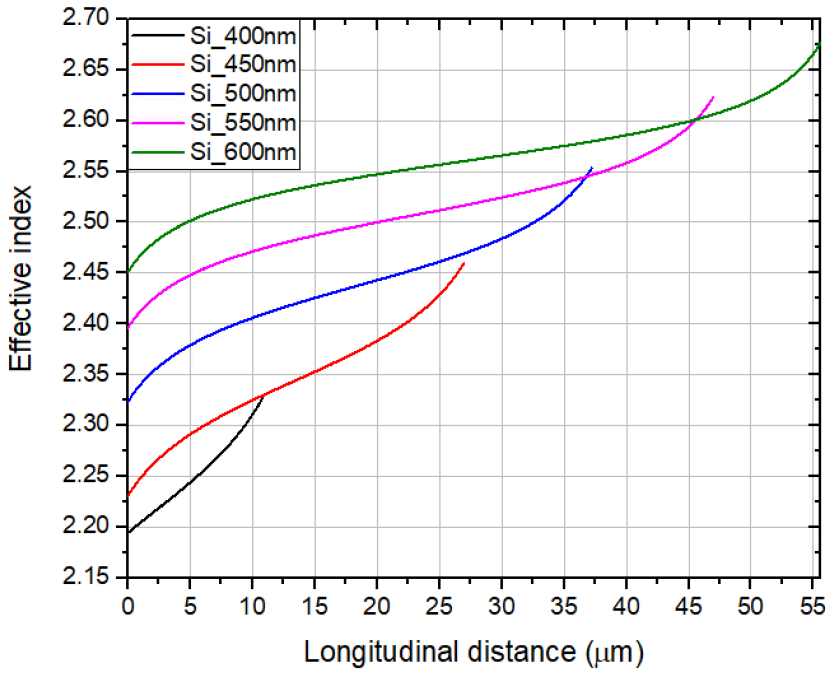


Figure 42: Adiabatic taper effective indexes variation for all silicon waveguide cases

Firstly, it is remarkable that, as previously anticipated, the wider the silicon waveguide the longer the adiabatic taper. Secondly, we can notice that the taper length is highly reduced with respect to the linear taper case, with the longest configuration being around 56 µm long.

2.4.4.3 Simulation results

Figure 43 shows the obtained results with the designed tapers. In terms of coupling efficiency, the results are very similar to the linear taper case: however, the adiabatic taper allows us to achieve a power transfer for much shorter lengths (respectively, 11 µm, 27 µm, 37 µm, 47 µm and 56 µm for the 400 nm, 450 nm, 500 nm, 550 nm and 600 nm silicon waveguide width cases). We can also see signal loss at the silicon waveguides termination, just like in the linear taper configuration. Eventually, the best coupling efficiencies are achieved for the 500 nm, 550 nm and 600 nm cases, with values around 90% or even above. This result gives us the opportunity to optimize even further the already efficient linear taper, by reducing its length.

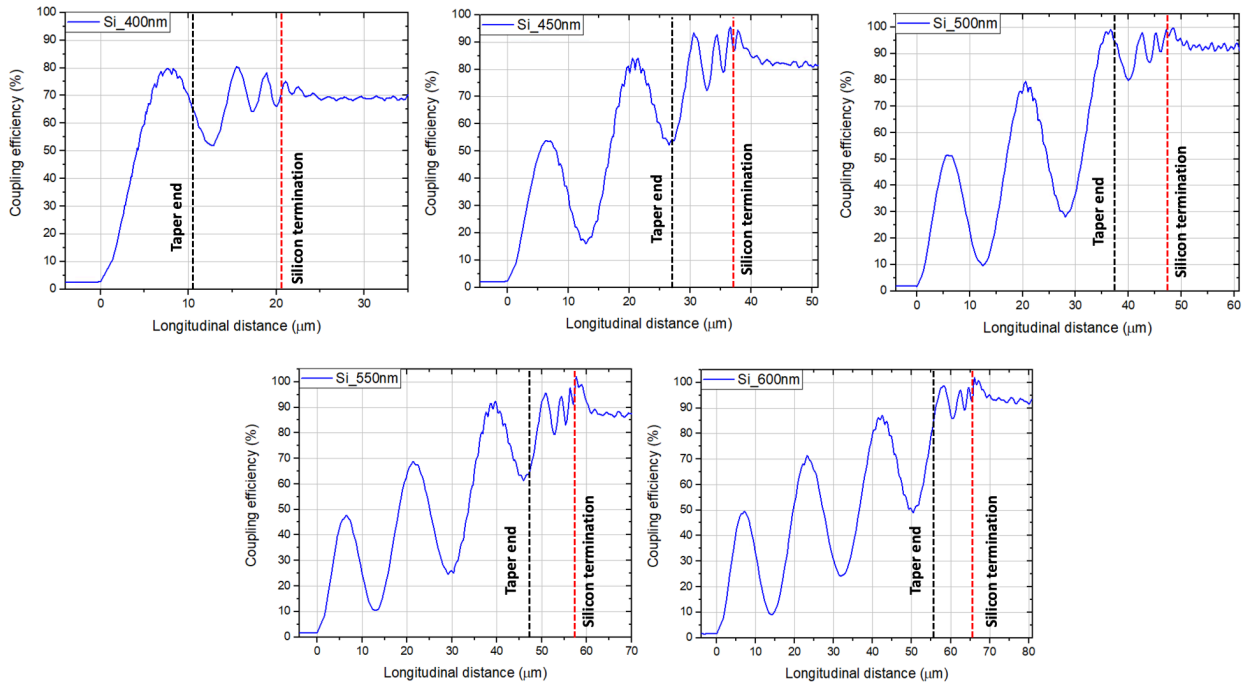


Figure 43: Coupling efficiencies for all the hybrid structures' adiabatic tapers

Moreover, the optical bandwidth study shows very similar behavior compared to the previously discussed mode transformer, the adiabatic taper showing coupling efficiencies around 90% or above for a range of wavelengths of about 150 nm.

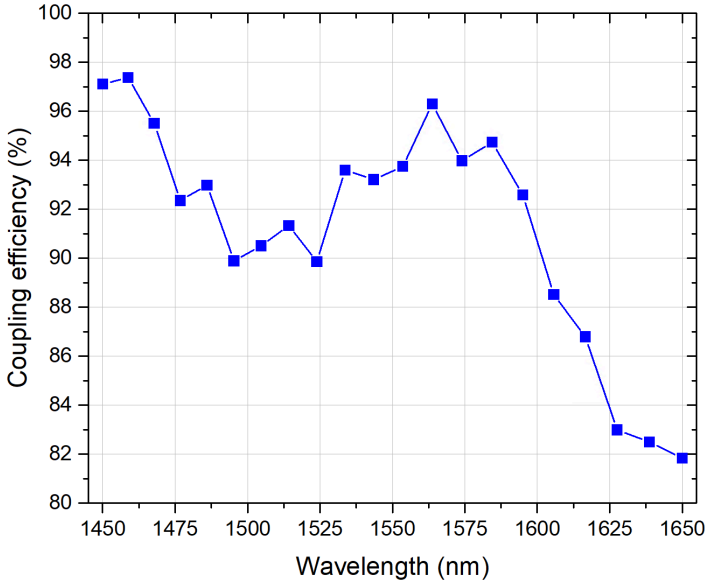


Figure 44: Adiabatic mode transformer's optical bandwidth

2.5 Amplification region

2.5.1 Amplification mechanism

Once the signal transferred from the silicon bus circuitry to the PhC waveguide, it is time to perform the amplification. The idea is straightforward: the optical mode propagates through the III-V waveguide while being amplified thanks to the presence of an active material, that is a MQWs structure. Such a heterostructure is based on the alternation of III-V materials with different band gap: by growing very thin layers (on the order of 10 nm) alternatively with higher and lower band gap, we create bidimensional materials that do not present anymore valence and conduction bands with a continuum of energy states, leading to the appearance of discrete energy levels for the carriers confined inside the wells. Additionally, since the wells exhibit lower energy states for electrons in the conduction band (or higher energy states for holes in the valence band) with respect to the surrounding barriers, the carriers tend to be trapped inside the wells at discrete energy levels. Therefore, we have a high density of carriers available for radiative recombination: when an external photon with a frequency corresponding to the energy level of the QWs impinges, electrons relax to a lower energy state, recombining with a hole in the valence band and emitting a photon with same frequency, phase and direction of the impinging one. At the output, then, we have two coherent photons, meaning that we have amplified our input signal. Such a mechanism is called stimulated emission and it represents the base to achieve optical amplification. Figure 45 highlights a simple schematics explaining the stimulated emission process.

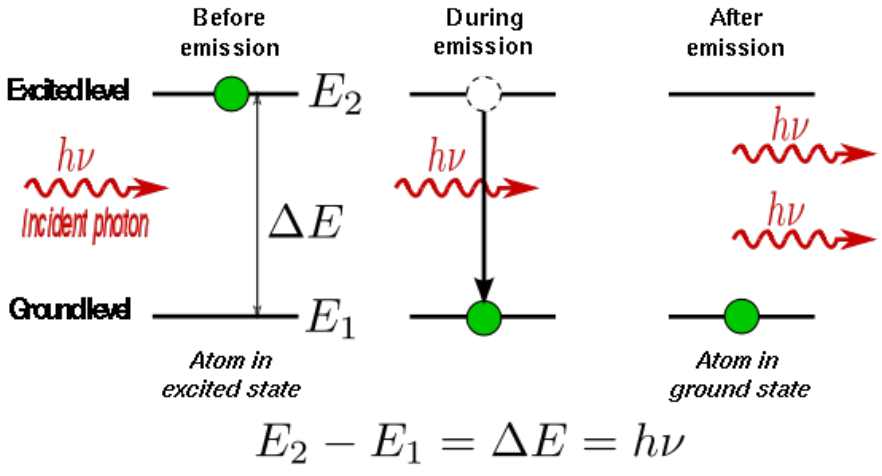


Figure 45: Basic schematics showing the stimulated emission mechanism. An incident photon with energy ΔE collides on an excited electron at an energy state E2, causing it to relax to a lower energy state E1 and emitting an additional photon, coherent with the first one

In order to achieve efficient amplification our device needs to provide multiple stimulated emissions: this is only possible by attaining population inversion, which means that in our system we always need to have more carriers in the excited state than in the fundamental state, so to continuously provide carriers for radiative recombination. The population inversion depends on the device's carriers injection scheme: we will treat it later during the electrical design section.

2.5.2 2D-PhC: improved confinement factor

Contextualizing the previous discussion to our device, from an optical point of view, our goal is to maximize the confinement factor, that we introduced at the beginning of this chapter. It is defined as the overlap between the optical propagating mode, that we want to amplify, and the MQWs heterostructure, providing the gain. Here relies one of the main advantages exploiting a photonic crystal: it gives the possibility to minimize the modal volume close to the diffraction limit, increasing in turns the confinement factor. Figure 46 shows, as an example, the squared modulus of the index-guided mode's electric field propagating inside the PhC waveguide with width $1.1 \cdot a\sqrt{3}$, extracted from FDTD simulation.

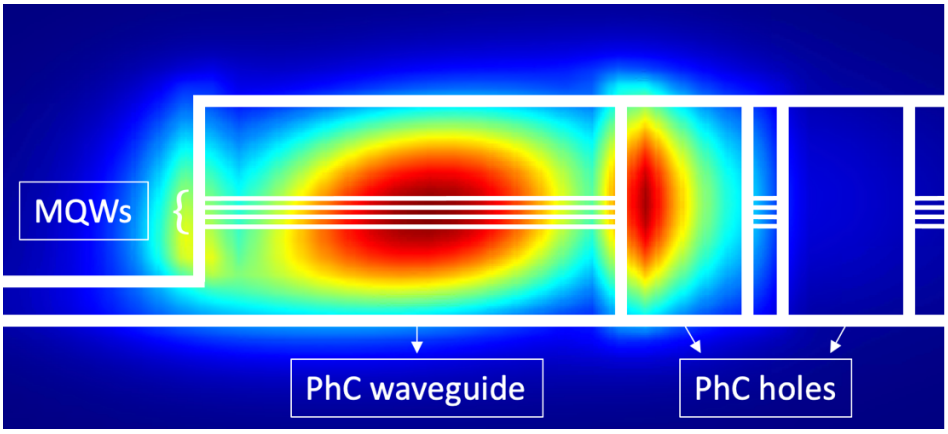


Figure 46: Cross-section's close-up view of the propagating optical mode's $|\mathbf{E}|^2$, extracted from FDTD simulation; in white we represent the nanoamplifier's perimeter, to highlight the mode confinement, as well as the MQWs heterostructure

The whole heterostructure was made of InGaAsP as a material, varying the percentage of composites to modulate the energy gap for the constitution of barriers and wells. In order to have the discrete energy levels at suitable values for our purpose (radiative recombination with stimulated emission processes of photons around 1550 nm), the MQWs heterostructure has been designed with wells of 6 nm and barriers of 15 nm. Clearly, the confinement factor is highly dependent on the number of integrated quantum wells: the more they are, the higher the confinement factor gets.

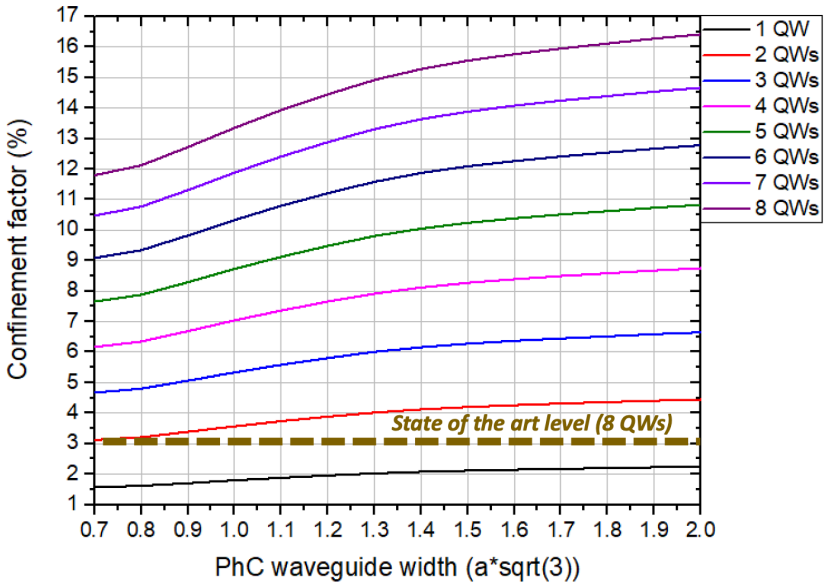


Figure 47: Confinement factor as a function of the PhC waveguide width, for different number of integrated QWs. The state of the art confinement factor level has been extracted from [18]

On the other hand, increasing the well's number would lead to a higher active volume, meaning that a higher power would be required to inject the same electrical carriers density inside the wells. For technological purposes and facing the trade-off between gain maximization and power consumption minimization, we decided to fix the number of QWs in our structure to 4. Figure 47 shows that, for the same amount of integrated QWs, the confinement factor is at least four times higher for our PhC structure compared to state of the art SOAs based on standard technology [18]. This is not astonishing, considering that the propagating optical mode is more confined in a PhC waveguide than in a regular SOA. Additionally, we can see that the confinement factor increases with the PhC waveguide width: in fact, the index-guided mode tends to widen horizontally while simultaneously shrinking its vertical profile when the waveguide width increases, improving the overlap with the active material.

2.5.3 Loss mechanism

During its propagation, the optical mode is not only subject to amplification, but also to losses. The main source of loss in our PhC waveguide is surely linked to free-carrier absorption, caused by the presence of P- and N-doped layers. In fact, carriers inside such doped layers can absorb propagating photons, increasing their energy and performing intra-band or even inter-band transitions. The total absorption loss actually depends on the doping level and mainly on the overlap between the light signal and the doped layers: the higher the mode's portion overlapping with P- and N-side, the higher the losses. We have calculated with FDTD simulations the amount of free carrier absorption loss for our nanoamplifier at 1550 nm as a function of the waveguide

width, reporting it in Figure 48. As we will see more in details during the electrical simulations section, we fixed for our nanoamplifier a N-doped layer of 50 nm and a P-doped one of 100 nm, both with a doping level of $2 \cdot 10^{18}$ cm^{-3}.

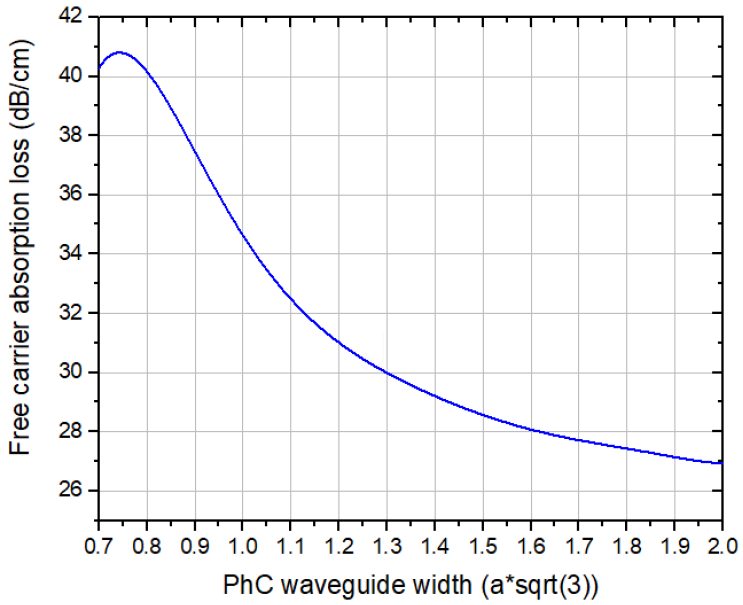


Figure 48: Free carrier absorption losses vs PhC waveguide width

Similarly to the previous discussion regarding the confinement factor, the mode shape tends to shrink vertically and widen its longitudinal profile increasing the PhC waveguide width: as a consequence, while the QWs get more covered by the optical mode, the overlap with the doped layers reduces more and more. Such a high loss is mainly due to the P-doped layer: in fact, P-carriers cause a much higher free carrier absorption loss compared to N-carriers (typical bulk losses for N-type and P-type doped InP-based materials at $1 \cdot 10^{18}$ cm^{-3} and at a wavelength of 1500 nm are respectively 4 dB/cm and 56 dB/cm) [21].

We have finished the discussion about our nanoamplifier from an optical point of view: we have seen how to efficiently transfer the signal from the bus circuitry to the active level and we have treated the amplification region, commenting the confinement factor and the free carrier absorption loss in this device. What we still need to treat in order to have a full description of our PhC nanoamplifier is the electrical injection scheme, commenting on how the population inversion is achieved and which power is actually needed to attain a certain level of amplification. In the next section, we will discuss the electrical simulations performed. These results will serve as inputs for the calculation of the PhC amplifier performances (gain per unit length as well as power consumption).

2.6 Electrical behavior

So far we have treated the nanoamplifier from an optical point of view. Our goal is now to design an efficient electrical injection scheme. It is in this context that we can appreciate the beauty of the asymmetric design we have chosen for the nanoamplifier, as we will see during the simulation results discussion.

The electrical behavior of our structure has been studied with the software *Lumerical CHARGE solutions* [75]. It is a simulation tool based on the Finite-Element-Method (FEM), meaning that the full system is discretized (meshed) into smaller domains (finite elements). Each domain is modeled by a set of equations describing the electrostatic potential (Poisson's equations) and density of free carriers (drift-diffusion equations). All the domains are merged together to obtain the total simulation result.

As we mentioned in the introduction of this chapter and represented in Figure 29, our structure behaves electrically as a P-i-N junction diode. The intrinsic region represents the diode's depletion zone, where the majority carriers under forward bias condition tend to diffuse, being then trapped in a discretized energy level of the MQWs. In that way we create electron-hole pairs, that can either recombine by radiative processes like stimulated emission (signal amplification) and spontaneous emission (emitting photons which are not coherent with the propagating signal and consequently contributing to noise rather than signal amplification), or by non-radiative processes like Shockley-Read-Hall (SRH) recombination (trap-assisted recombination, where electrons relax into trap states formed inside the band gap for the presence of lattice defects), surface recombination (dangling bonds at the semiconductor surface creating trap states for the carriers) and Auger recombination (three-particles transition where an electron-hole pair recombines transferring the excess energy to another electron or hole, exciting it to a higher energy state within the same band). It is clear that, to increase the injection efficiency, non-radiative events have to be minimized: in other words, non-radiative lifetime (average time before an electron in the conduction band recombines with a hole through non-radiative mechanism) has to be much longer than the radiative one. During the fabrication chapter we will discuss about the adopted solution to minimize surface recombination. By the way, from a design point of view, our main objective is to conceive an electrical injection scheme maximizing the radiative recombination events: in the next subsections we will fully describe the nanoamplifier's electrical design and the related performances.

2.6.1 The structure

Figure 49 represents the cross-section schematics of our structure, from an electrical point of view.

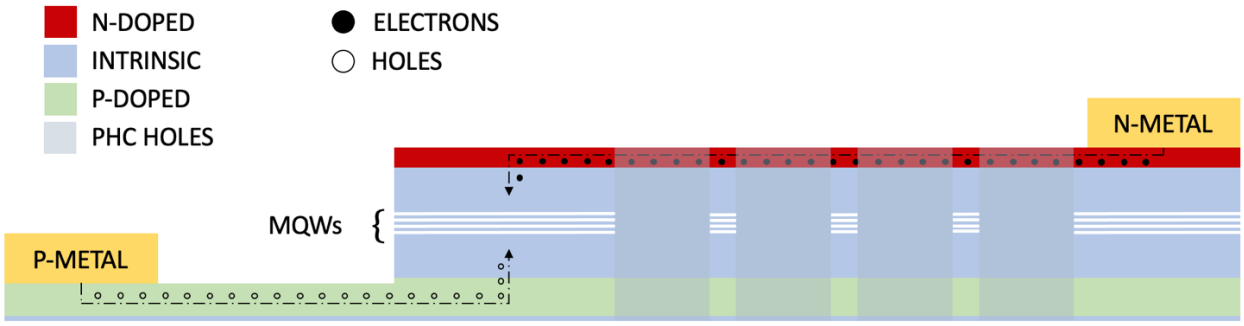


Figure 49: Electrical cross-section schematics of the PhC nanoamplifier

The N-doped layer is made of InP (doped with silicon), while the P-doped one is made of InGaAsP (doped with zinc) as well as the intrinsic layer in between the doped layers. Eventually, the thin intrinsic layer at the very bottom of the structure is made of InP: as we will discuss more in details during the fabrication chapter, this choice has been made in order to avoid trap-states from the dangling bonds at the bottom surface of the device. In fact, InP presents a higher band gap with respect to InGaAsP (1.35 eV vs 1 eV), introducing a barrier that prevents the holes from diffusing to the bottom surface. Both P- and N-doping level have been set to $2 \cdot 10^{18}\ \mathrm{cm}^{-3}$, with total layer thicknesses of 90 nm for the P-doped and 51.8 nm for the N-doped layer. All the other thicknesses have been set as listed in Table 2.

The idea behind this structure is the following: while we contact the N-doped layer on the side of the PhC pattern, we etch the III-V down to the P-doped layer on the area where we want to contact it with metal, referring to this region as the base of our structure. The total base thickness is 80 nm, composed of 70 nm of P-doped layer and 10 nm of intrinsic InP. Even though our P-layer is 90 nm thick nominally, we cannot be completely sure during fabrication whether the doping profile abruptly decreases from $2 \cdot 10^{18}$ cm^{-3} to an intrinsic carriers concentration exactly at the nominal thickness. This is why, to be sure of depositing metal on the P layer at its nominal doping level, we slightly etch it underneath the P-i interface. The forming of the base is also used to define our waveguide edge, creating an asymmetric PhC waveguide.

This configuration enables lateral injection of electron-hole pairs within the waveguide region, from the N contact on top of the heterostructure and the P contact on the base. It allows us to exploit the large difference in mobility between electrons and holes. While electrons in the N-layer with the chosen level of doping have a mobility of 1493 cm^2/(V·s), that of the holes in the P-layer with the same amount of dopant is just 30 cm^2/(V·s (i. e., 50 times smaller). When we bias the diode, electrons start to diffuse through the N-doped layer to the P contact, as well as holes through the P-doped layer to the N contact. However, because of the important difference in mobility, electrons diffuses through a much longer distance compared to the holes, meaning that

electron may be transported all the way down to the PhC waveguide edge inside the N-doped layer, before diffusing inside the intrinsic layer. This will not happen for the holes as they will diffuse through a much shorter path inside the P-layer, diffusing inside the intrinsic layer as soon as it is possible (see Figure 49). This scheme is different than that of regular SOAs where the transport of charges occurs mainly in the vertical direction.

We will introduce now the performed electrical simulation, beginning with the simulation setup.

2.6.2 Simulation setup

Firstly, we had to deal with the material definition. While in the software library InP was already defined, the quaternary alloys $In_{1-x}Ga_xAs_yP_{1-y}$ used for QWs, barriers and P-layer (the latter being the same as the barriers one) were missing. We introduced, then, proper material parameters in order to build-up a simulation's reliable model, with a correct representation of the device's electronic as well as recombination properties. The two quaternary alloys present different composition: for the QWs we used $In_{0.84}Ga_{0.16}As_{0.16}P_{0.84}$, while for the barriers and P-doped layer we used $In_{0.84}Ga_{0.16}As_{0.48}P_{0.52}$. It is not possible with this software to calculate the physical properties of quantum confined materials such as quantum wells using the parameters of their constituting bulk material. Since we were interested in the study of radiative recombination inside our structure, we fixed the energy gap E_g to an energy corresponding to the transition from the excited discretized state in the QWs conduction band to the ground state in the QWs valence band. In that sense, since we want stimulated emission processes emitting photons with a wavelength of 1550 nm, E_g for the QWs was set to $E_g = 0.8\ eV$. For the barriers (and the P-layer), the transition wavelength was 1240 nm: consequently, corresponding to $E_g = 1\ eV$. Concerning the electrical conduction, the mobility was calculated from the widely used Caughey-Thomas model [76]. Particularly, that model derives the mobility from the following equation:

$$\mu_{n,p} = {\mu_{n,p}}^{min} + \frac{{\mu_{n,p}}^{max} - {\mu_{n,p}}^{min}}{1 + \left(\frac{{N_D}^{+} + {N_A}^{-}}{N_{ref}}\right)^{\alpha}} \tag{2.25}$$

Where n,p refer to the doping type. This equations tells us that when the doping level (${N_D}^{+}$ or ${N_A}^{-}$) is very low, the mobility saturates at its maximum value ${\mu_{n,p}}^{max}$, which is the lattice-scattering mobility (the fundamental process of thermal scattering impeding the free motion of carriers in the lattice). On the other hand, when the doping concentration is very high, the resulting mobility saturates at its lower value ${\mu_{n,p}}^{min}$. N_{ref} is the doping concentration at which mobility reduces to almost half of its maximum value at low doping. Eventually, α is an exponent weighting the influence of doping concentration to the carriers mobility for the considered material. Since we always conducted our analysis at room temperature, in that model we do not take into account the temperature dependence of each parameter. The extraction of

each coefficient reported in the model has been carried out following [77]. The last coefficients we had to assign are the ones defining the different types of recombination we could have in the material. Particularly, the considered types of recombination in the simulation are listed below, followed by the equations describing the related recombination rates.

- SRH recombination: a non-radiative process where trap-states resulting from impurities appear within the band gap, giving the possibility to electron-hole pairs to relax into them releasing a phonon instead of a photon.
- Auger recombination: another non-radiative process where the recombination of an electron-hole pair releases energy that is transferred to a third carrier (electron or hole); the latter moves then to a higher energy level within the same band.
- Radiative recombination: this is the type of recombination we want to take advantage of in order to achieve signal amplification. An excited electron recombines with a hole in the ground state emitting a photon with energy equal to the energetic transition.

$$R_{SRH} = \frac{np - n_{i,eff}^2}{\tau_{SRH}(n + p + 2n_{i,eff})} \tag{2.26}$$

$$R_{Au} = C(n + p)(np - n_{i,eff}^2) \tag{2.27}$$

$$R_{Rad} = B(np - n_{i,eff}^2) \tag{2.28}$$

Where n and p are respectively the electrons and holes concentration, $n_{i,eff}$ the effective carriers concentration for the undoped semiconductor (intrinsic case), τ_{SRH} the SRH non-radiative lifetime, C the Auger carrier capture coefficient and B the spontaneous radiative recombination coefficient. Table 3 resumes the assigned parameters, extracted from Crosnier's PhD thesis.

Recombination type	Coefficient
SRH	$\tau_{SRH} = 20\ ns$
Auger	$C = 5 \cdot 10^{-29}\ cm^6/s$
Radiative	$B = 3 \cdot 10^{-10}\ cm^3/s$

Table 3: Assigned coefficients for radiative and non-radiative recombination mechanisms considered in the simulation (from [71])

Once all the materials declared, we made some useful approximations in order to reduce the required computational power and, consequently, the simulation time. First of all, we did not consider 4 quantum wells of 6.3 nm each but we merged them together into a single active region of 25.2 nm: considering the original MQWs heterostructure, in fact, would have required an extremely fine mesh, leading to very long simulation times. Such an assumption makes sense

since we are interested in the total radiative recombination rate and its distribution along the device's transverse direction, in order to validate our electrical injection scheme. Secondly, another time with the desire of saving some simulation time, we did not include inside the simulation region the full dimension of the nanoamplifier but we considered just a length of two PhC periods, while including the full device's width and thickness (Figure 50).

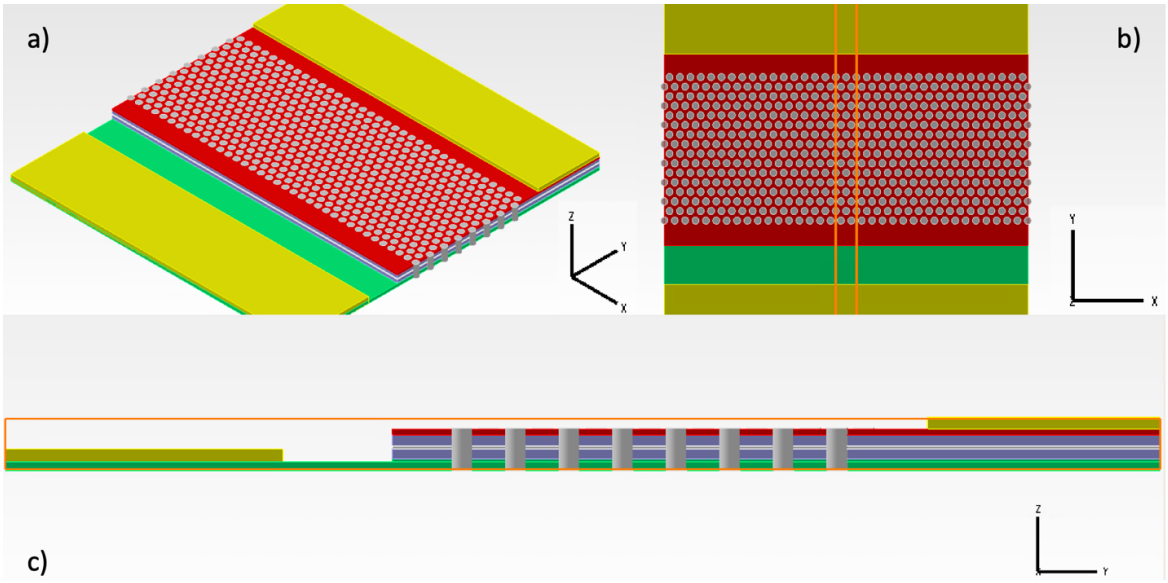


Figure 50: Nanoamplifier schematics extracted from Lumerical CHARGE. The three pictures represent the scaled-down full structure's a) 3D-view, b) top-view with simulation region (orange) only covering two PhC periods (X-direction), c) cross-section with simulation region covering the full device's width (Y-direction) and thickness (Z-direction). The choice of each layer's color has been made to match the ones of Figure 49

Starting from the results of the reduced simulation, we are able to calculate the behavior for the full structure: in fact, the device can be electrically modeled as represented in Figure 51. Segmenting the full structure into K smaller segments, it is analogue to consider K equal parallel arms, each of them composed by a P-i-N PhC junction diode being just two PhC periods long (along X-direction referring to Figure 50). The standard simulation settings consider perfect electrical contacts, with a contact resistivity equal to zero. However, for a more reliable model, we can introduce contact resistances as we did in Figure 51 and divide them into K parallel arms each of them with a resistance $R^{i}_{P,N} = K \cdot R^{C}_{P,N}$. Additionally, since we develop our model with a DC-voltage, we do not consider the diodes capacitances, which means that the current of the full structure is just given by the sum of each arm's current; however, since each arm is composed by the same elements and has the same voltage drop upon them, the total current is nothing but $I_{tot} = K \cdot I_i$.

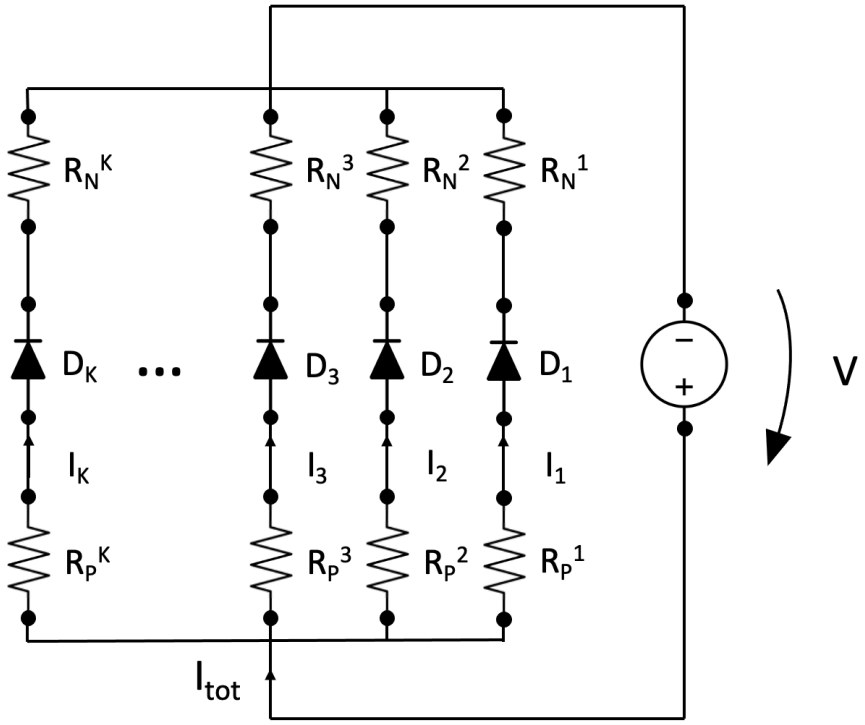


Figure 51: Electrical model of the simulated structure

The last parameter to set before showing the simulation results is the P-metal distance from the PhC waveguide's sidewall. For this, we have to face a trade-off: on one hand, we want to maximize carriers injection inside the waveguide, which would lead to the P-metal distance minimization, while on the other hand we want to avoid optical absorption from the metal, prohibiting us to reduce such distance at will. As we will show during the nanolaser's optical simulation section, we have found that optical absorption is harmless starting from a distance of around 800 nm. We decided to fix the P-metal distance from the PhC waveguide's sidewall to 850 nm, adding a little bit of safety margin to the minimum distance.

2.6.3 Simulation results

Figure 52 shows the extracted IV curves. We have calculated them setting the PhC waveguide width to the five values at the taper's output associated to the different silicon waveguides of the previous section. In order to evaluate the amount of amplification the optical mode undergoes, we need to investigate carriers injection inside the PhC waveguide. We recall that the simulation considers a reduced nanoamplifier's region (only two PhC periods along X) and that it neglects the contact resistances. However, we will later include them in our electrical model to analyze how the simulation results vary.

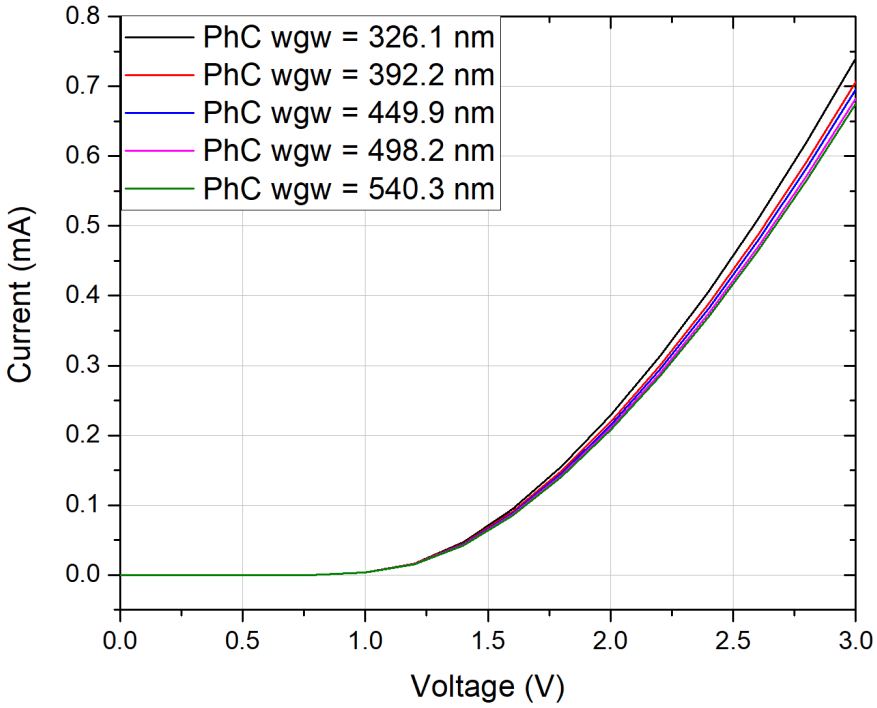


Figure 52: I-V curves for the five different PhC waveguide widths (listed in the inset). They are associated, from narrower to wider, respectively to 400 nm, 450 nm, 500 nm, 550 nm and 600 nm silicon waveguide width case. The structure is 2 periods long

The characteristics have the typical diode trend: under a forward bias, the current through the junction stays very small up to the threshold voltage, where it starts to exponentially increase. Such a voltage corresponds to the point where majority carriers gets enough energy to overcome the built-in potential established by the junction's inner electric field: in that way, carriers diffuse inside the depletion region, getting trapped by the MQWs. As we can observe, the curves are very close to each other. However, it is possible to remark that the wider the PhC waveguide is the slightly bigger the series resistance associated to the diode (R_s) gets. This is understandable since a wider waveguide width adds up an additional portion of material to travel through for the carriers, increasing the device's resistance. If we look back to our electrical model, we can derive the full structure's characteristic: since the simulation considers two PhC periods, it is sufficient to multiply the current of Figure 52 by a factor $K = {L_{tot}}/{2a}$, where L_{tot} is the total nanoamplifier length and a is the PhC period. As an example, we can consider a nanoamplifier with a 100 µm long amplification region; if we use the adiabatic coupling scheme, for the total length we need to add up twice the taper length (considering one taper to couple the signal in, the other one to transfer the signal back to the passive circuitry). The total device's length is then 122 µm, 154 µm, 174 µm, 194 µm and 212 µm respectively for the interfacing with the 400 nm, 450 nm, 500 nm, 550 nm and 600 nm silicon waveguide width cases.

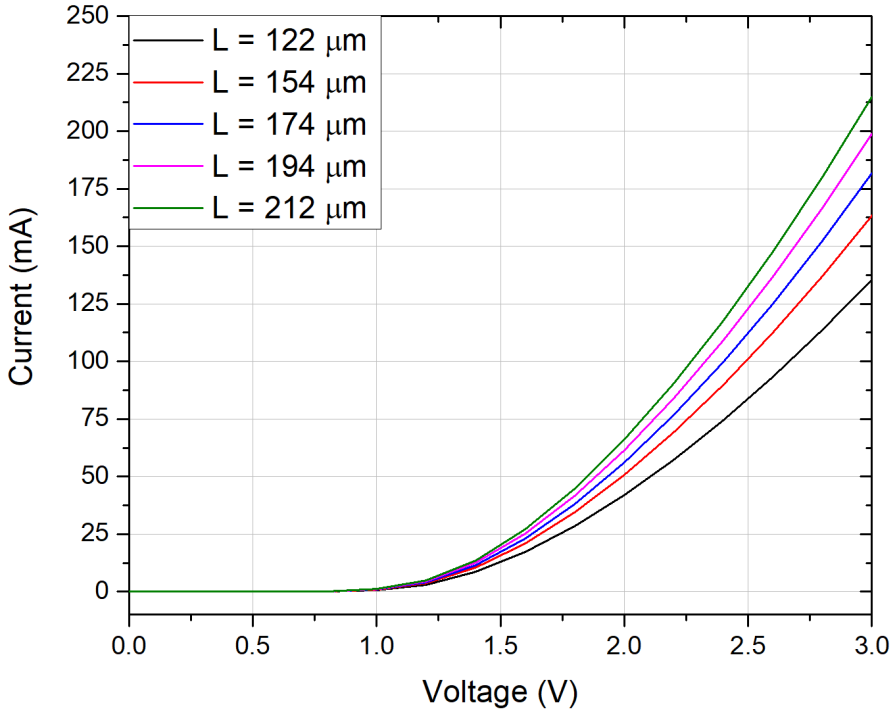


Figure 53: I-V curves for the total nanoamplifier length cases

The first thing we can observe is that the longer the amplifier is, the higher the current. In fact, it is equivalent to compare electrical circuits with different number of parallel arms, each of them contributing with a very similar amount of current as we have seen from Figure 52. The higher the number of parallel arms, the more current contributions we have and consequently the higher the total current is. In order to fully describe the system we need to also add contact resistances: from Transmission Line Measurement (TLM) we performed (detailed further during the characterization chapter), we obtained contact resistivities of $5.6 \cdot 10^{-5}\ \Omega \cdot \mathrm{cm}^2$ for the P-contact and $3.7 \cdot 10^{-4}\ \Omega \cdot \mathrm{cm}^2$ for the N-contact, with transfer lengths of respectively 0.55 µm and 11 µm. Considering contacts with same lengths as Figure 53 and effective widths of 11 µm for the N-contact and 0.55 µm for the P-contact, the corresponding resistances are listed in the table below.

Amplifier length	R_P	R_N
122 µm	83.5 Ω	27.6 Ω
154 µm	66.1 Ω	21.8 Ω
174 µm	58.5 Ω	19.3 Ω
194 µm	52.5 Ω	17.3 Ω
212 µm	48 Ω	16 Ω

Table 4: Contact resistances for each nanoamplifier length

Referring to the analogue circuit as the one depicted in Figure 51, the total voltage drop now is given by the one across the ideal simulated junction (with zero-contact resistivity) plus the voltage drops across the contact resistances, simply given by the Ohm's law $V = I \cdot R$. The resulting I-V curves for the complete nanoamplifier's model are plotted on Figure 54.

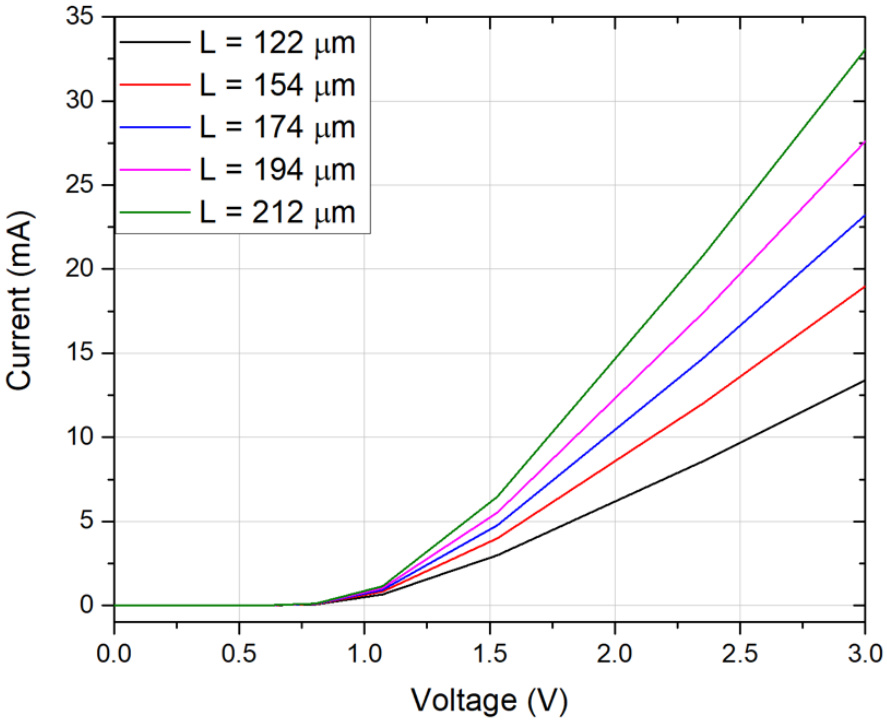


Figure 54: Nanoamplifier's complete model I-V curves, considering the full device's length as well as its contact resistances

Let us focus our attention now on the radiative recombination rate across the structure. To simplify the representation, we will show only the case of the PhC waveguide width of 449.9 nm. We can immediately remark that the highest amount of recombination takes place inside the PhC waveguide, suggesting that our electrical design is quite efficient. The PhC waveguide's sidewall is at 0 µm along the transverse direction. The more we increase the transverse direction distance, the more we go inside the PhC pattern, approaching the N-contact on the other side of it. The regions where the radiative recombination rates fall to zero correspond to PhC holes. For a clearer plot, only three cases of applied voltage have been represented, starting around the diode's threshold voltage.

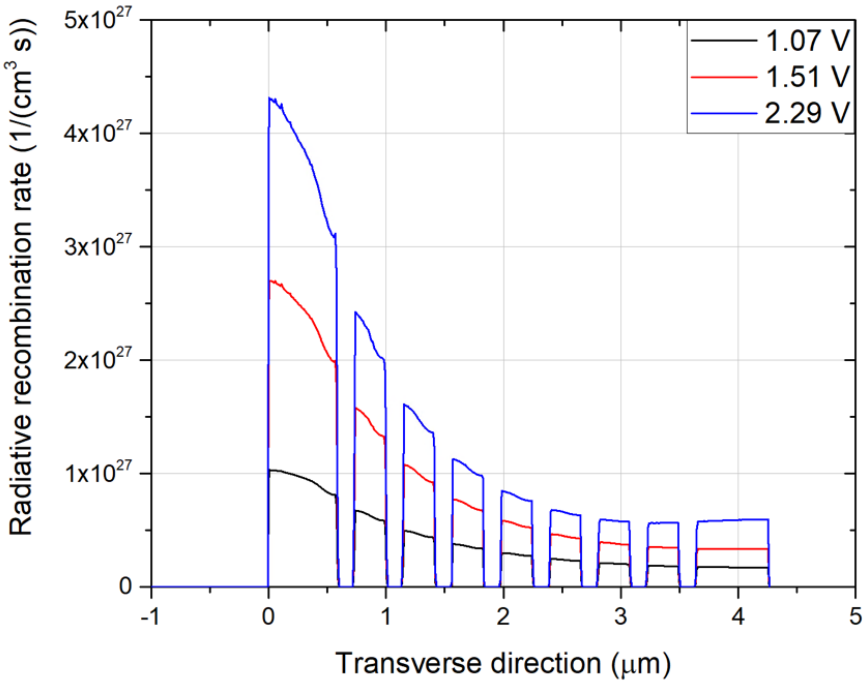


Figure 55: Radiative recombination rate along the amplifier's transverse direction as a function of the applied voltage

Clearly, the higher the voltage drop the more radiative recombination events take place. It is interesting to notice that the stronger recombination rate growth takes place inside the PhC waveguide indicating that the smallest potential barrier to overcome for diffusing majority carriers is localized inside the waveguide, while the required energy for the carriers to diffuse inside the intrinsic region increases more and more moving away from it. This is reasonable since, in forward bias, the positive voltage signal is applied to the P-metal, while the N-one represents the signal ground: since in our case we deal with an asymmetric design, we can assume that the closer we are to the P-contact, the stronger the voltage across the junction is felt by electrical carriers, while moving away from the P-contact such a signal becomes a little bit weaker. This is confirmed by the electronic band diagrams shown in Figure 56. As we can see, at a fixed voltage of 1.51 V, the difference between the conduction band energy E_c and the electrons quasi-Fermi level Ef_n is different in the two band diagrams; recalling that, at non-equilibrium, the electron population in the conduction band is described by a Boltzmann distribution of the form $N_c \cdot e^{-(E-Ef_n)/kT}$, where N_c is the density of states, we immediately understand that electrons have a higher probability of diffusing through the intrinsic layer to the quantum wells in the PhC waveguide compared to the region in close proximity to the N-contact, since in the former case Ef_n is higher than the intrinsic layer's conduction band. The diffusion through the N-doped layer up to the PhC waveguide represents a more favorable path for electrons in terms of energy.

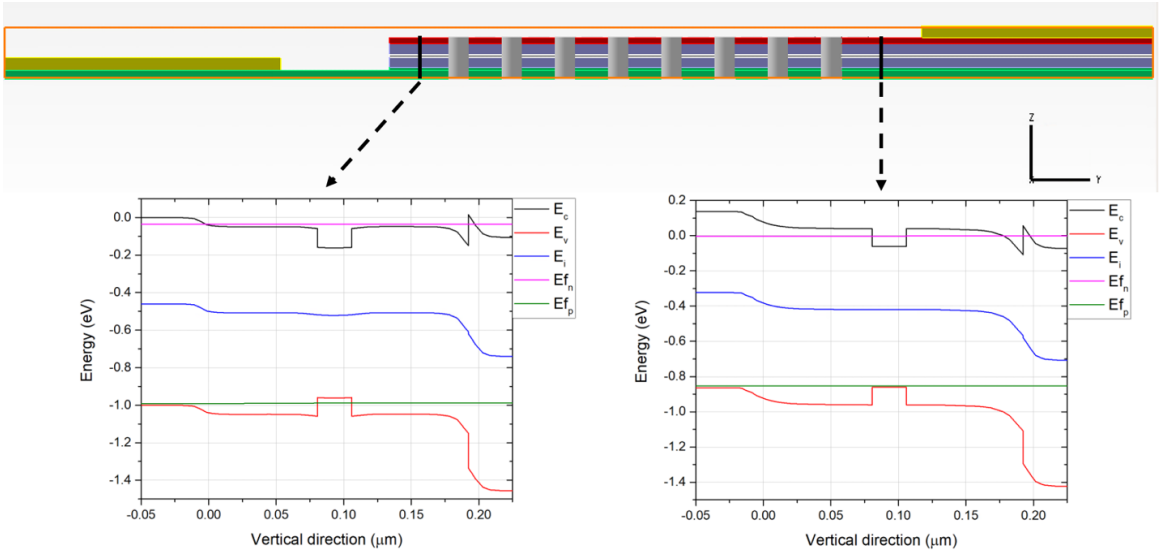


Figure 56: Band diagrams for an applied voltage of 1.51 V extracted from the center of the PhC waveguide and in close proximity to the N-contact. For each band diagram we have, from left to right referring to the X-axis, P-, intrinsic and N-layer

Now that we have determined the optical recombination rate, we possess all the ingredients to calculate the nanoamplifier gain. In the next section we will interface optical and electrical behavior of the structure, in order to analyze the device's performances.

2.7 Gain calculation

At the beginning of this chapter, we have seen that the gain per unit length is expressed as:

$$\left.\frac{G}{cm}\right|_{dB} = \frac{10}{\ln(10)}(\Gamma\sigma(N - N_{tr}) - \alpha) \tag{2.29}$$

We have now all the needed data to calculate such an expression, as a function of the applied voltage (i.e., the bias power). The only parameter we miss is the differential gain, which is a material's property. Considering our MQWs active material and following the results of [78], we fixed it to $\sigma = 8 \cdot 10^{-16}\ cm^2$. The free-carrier absorption, α, has already been calculated (Figure 48). Anyway, the key Figure Of Merit (FOM) for the gain expression is $\Gamma(N - N_{tr})$: basically, recalling also the confinement factor definition from equation (2.5), this FOM evaluates the overlap between the squared modulus of the propagating electric field and the carriers concentration profiles. In other words, it tells us that the more carriers we are able to inject inside the gain region and the better these carriers interact with the propagating optical mode, the higher the gain will be. The asymmetric PhC waveguide design as well as the lateral carriers injection scheme were specifically designed to maximize such a FOM: as shown in Figure 57, the higher injected carriers concentration is localized to the PhC waveguide, efficiently interacting with the propagating signal.

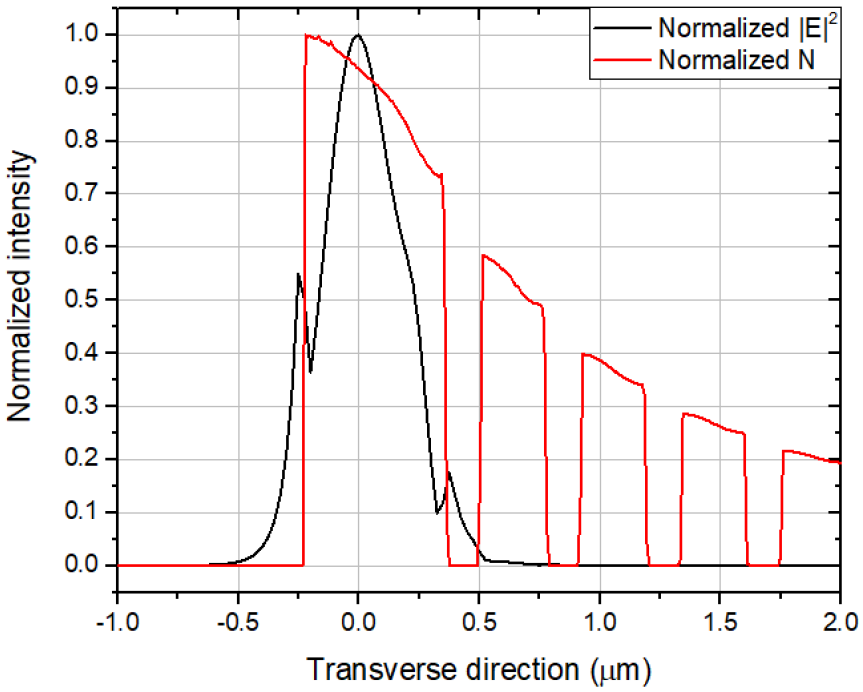


Figure 57: Normalized $|\mathrm{E}|^2$ and N profiles along the transverse direction

The injected carriers concentration is extracted from the electrical results we previously showed, knowing that the radiative recombination rate is:

$$\mathrm{R_{Rad}} = \mathrm{B}\left(\mathrm{np} - \mathrm{n_{i,eff}^2}\right) \cong \mathrm{BN}^2 \tag{2.30}$$

Where N is the injected electron-hole pairs concentration (this approximation is valid in the case of a doped structure). Taking into account the injected carriers distribution along the structure and $\mathrm{N_{tr}} = 10^{18}\ \mathrm{cm}^{-3}$, we are finally able to calculate the gain per unit length from equation (2.29) as a function of the applied voltage (Figure 58). We can notice that, at a fixed voltage, the structure providing the highest gain is the one with a wider PhC waveguide width. This result derives from the considerations we made about the confinement factor: the better overlap takes place when the PhC waveguide width is wider, since the propagating mode widens and at the same time gets thinner in the vertical direction, better covering the QWs cross-section. It is interesting that the transition from absorption ($\mathrm{G} < 0$) to gain ($\mathrm{G} > 0$) happens for a voltage around the diode's threshold ($V_{bias} \sim 0.95$ V): this tells us that, as soon as we start to exponentially increase the amount of injected carriers, the nanoamplifier begins to provide signal gain, suggesting another time that the designed electrical injection scheme is efficient.

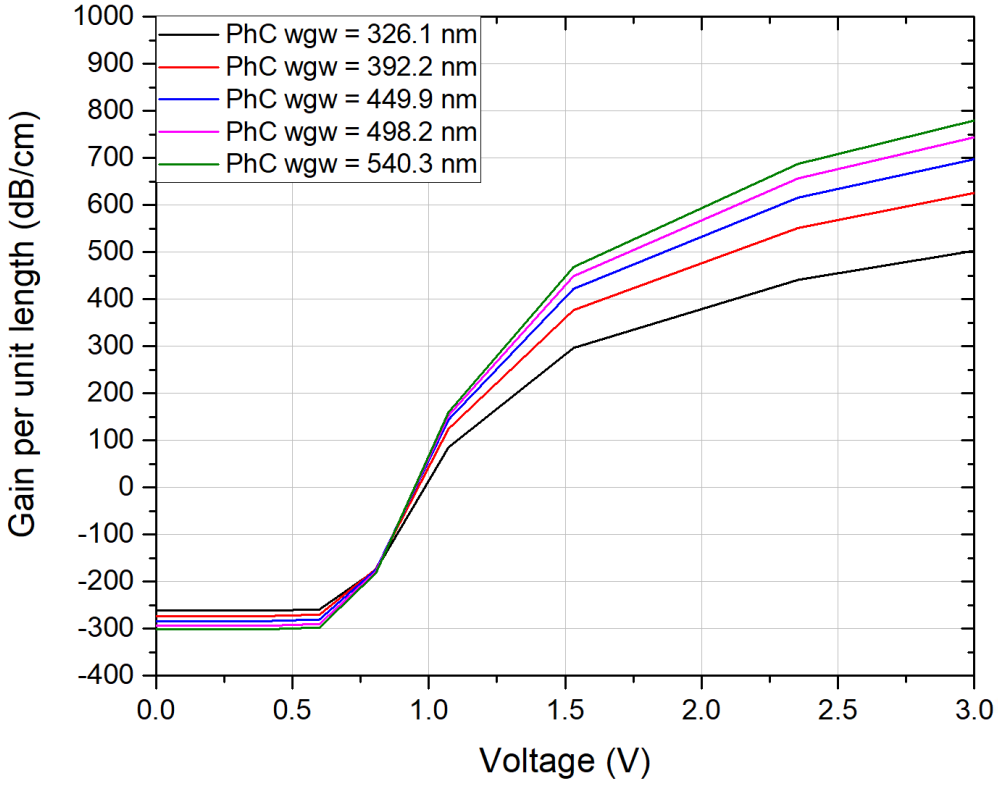


Figure 58: Gain per unit length as a function of the bias voltage across the junction. We have reported the results for the five different PhC waveguide width cases

Eventually, we want to highlight that the gain increase with voltage starts to stall for $V > 1.5\ V$. This is due to the fact that increasing the voltage across the junction, majority carriers get more and more energy, up to the point where a certain fraction of them is not only able to diffuse inside the intrinsic region, but also to travel through it inside the P-doped layer, recombining with holes. In other words, starting from a certain voltage, we do not continue to increase the amount of injected carriers in the same way due to the appearance of a leakage current. One way to overcome this leakage would be to engineer an electron-blocking layer between the P-doped layer and the MQWs heterostructure. Such a layer, which would be a composite presenting an energy gap higher with respect to the adopted quaternary alloy for the MQWs, would be able to oppose a high-energy barrier to electrons, blocking them from further diffusing to the P-layer. As a consequence, electrons would be forced to stay inside the intrinsic layer, getting trapped inside the MQWs. However, such a solution has not been adopted during this PhD.

The gain characteristics we just showed represent the unsaturated gain; nevertheless, in the real case we cannot ignore the existence of a gain saturation power, that we will discuss in the next section.

2.7.1 Gain saturation

The more general model of our nanoamplifier has to take into account also the gain saturation. In fact, from the carrier density rate equation, we have:

$$\frac{dN(x,t)}{dt} = \frac{\eta_i I}{qV} - \left(R_{nr}\left(N(x,t)\right) + R_{sp}\left(N(x,t)\right) + R_{st}\left(N(x,t)\right)\right) \tag{2.31}$$

Where $N(x,t)$ is the electrical carriers concentration, which is a function of space (the propagation direction x) and time, I is the injected current, η_i is the injection efficiency, q is the electric charge, V is the active region volume occupied by electrons and R_{nr}, R_{sp} and R_{st} represent respectively non-radiative, spontaneous and stimulated recombination rates. Particularly, R_{st} is the key term in this expression, since stimulated recombination processes are the ones providing signal gain. Considering a certain photon concentration N_p, we can state that the photon density's growth rate with distance due to stimulated recombination events is:

$$N_p(x) = N_p(0)e^{gx} \tag{2.32}$$

Where g is the material gain per unit length. Considering the covered distance $x = v_g t$, where v_g is the propagating mode's group velocity, the stimulated recombination rate is given by:

$$R_{st} = \frac{dN_p}{dt} = v_g g N_p \tag{2.33}$$

The carrier density rate equation then becomes:

$$\frac{dN(x,t)}{dt} = \frac{\eta_i I}{qV} - \left(R_{nr}\left(N(x,t)\right) + R_{sp}\left(N(x,t)\right)\right) - v_g g\left(N(x,t)\right)N_p(x,t) \tag{2.34}$$

As we can see, the electrical carrier concentration depends also on the photon density: the larger the photon density is, the higher the rate of carriers recombination by stimulated emission gets. However, since we do not dispose of an infinite reservoir of electrical carriers, when the photon density becomes too high along the amplifier length, the amount of available injected carriers is reduced: therefore, the amplifier gain is reduced as well. Let us relate the carrier density rate equation to the optical power: we have seen that, considering the PhC waveguide's cross-section, the confinement factor is given by the ratio between the square-modulus of the electric field confined in the QWs and the square-modulus of the electric field inside the full waveguide. This expression can also be expressed in terms of energy density, defined by the ratio of the mode's energy density stored inside the MQWs to the mode's energy density stored in the entire waveguide:

$$\Gamma = \frac{N_p \hbar\omega A_{yz}}{W} \tag{2.35}$$

Where $\hbar\omega$ is the photon energy, A_{yz} is the MQWs cross-sectional area and W is the energy per unit length in the entire waveguide's cross-section. Knowing that $P = Wv_g$, we can express the photon density as a function of the optical power:

$$N_p = \frac{\Gamma P}{\hbar\omega\, v_g\, A_{yz}} \tag{2.36}$$

Putting this term back in equation (2.34) and considering the linear approximation that we made for the gain in equation (2.6) we get:

$$\frac{dN(x,t)}{dt} = \frac{\eta_i I}{qV} - \Big(R_{nr}\big(N(x,t)\big) + R_{sp}\big(N(x,t)\big)\Big) - \sigma(N(x,t) - N_{tr})\frac{\Gamma}{A_{yz}}\frac{P(x,t)}{\hbar\omega} \tag{2.37}$$

Where σ is the material's differential gain. Additionally, to simplify the equation, we can assume that the non-radiative and the spontaneous emission rates are linearly dependent from the carriers concentration:

$$\frac{dN(x,t)}{dt} = \frac{\eta_i I}{qV} - \frac{N(x,t)}{\tau_R} - \sigma(N(x,t) - N_{tr})\frac{\Gamma}{A_{yz}}\frac{P(x,t)}{\hbar\omega} \tag{2.38}$$

With τ_R the global carriers lifetime. Since we work with a DC-bias, we can study the steady-state solution of such an equation:

$$\frac{\eta_i I}{qV} = \frac{N(x)}{\tau_R} + \sigma(N(x) - N_{tr})\frac{\Gamma}{A_{yz}}\frac{P(x)}{\hbar\omega} \tag{2.39}$$

And this gives us:

$$N(x) - N_{tr} = \frac{\frac{\eta_i I \tau_R}{qV} - N_{tr}}{1 + \sigma\frac{\Gamma}{A_{yz}}\tau_R\frac{P(x)}{\hbar\omega}} = \frac{\frac{\eta_i I \tau_R}{qV} - N_{tr}}{1 + \frac{P(x)}{P_{SAT}}} \tag{2.40}$$

$$P_{SAT} = \frac{A_{yz}}{\Gamma}\frac{h\,c}{\sigma\,\tau_R\,\lambda} \tag{2.41}$$

P_{SAT} is the material gain saturation power, defined as the optical power value at which gain saturation cannot be ignored. At the beginning of this chapter we have seen that:

$$\frac{dP}{dx} = (\Gamma\sigma(N(x) - N_{tr}) - \alpha)P(x) \tag{2.42}$$

If we insert (2.40) in (2.42) we obtain:

$$\frac{dP}{dx} = \left(\frac{\Gamma g_{uns}}{1 + \frac{P(x)}{P_{SAT}}} - \alpha \right) P(x) \tag{2.43}$$

This equation is clear: when the optical power $P(x) \ll P_{SAT}$, the material gain as well as the amplifier total gain are equal to the respective unsaturated values. However, when the optical power at a certain position x along the amplifier's propagation direction becomes equal to the saturation power, then the material gain is halved.

The appearance of a saturation power gives us some concern regarding the signal's input power level. In fact, the higher the input power is, the higher the risk of reaching saturation will be. A typical FOM for an optical amplifier is the so-called Input Saturation Power, defined as the input power level at which the gain has been reduced to half of its unsaturated value. It is possible to demonstrate that [19]:

$$G = G_0 \frac{1 + {P_{IN}}/{P_{SAT}}}{1 + G_0 {P_{IN}}/{P_{SAT}}} \tag{2.44}$$

Where G is the amplifier gain including gain saturation, G_0 the unsaturated gain and P_{IN} the signal's input power. As a consequence of that formula, we have that the Input Saturation Power is:

$$P_{IN,sat} = \frac{P_{SAT}}{G_0 - 2} \tag{2.45}$$

Let us analyze and discuss these parameters for the designed nanoamplifier. For a clearer representation, we fix the bias voltage to 1.51 V and the full amplifier length to 300 µm. The currents flowing for the 5 PhC waveguide width studied cases are around 7 mA, corresponding to a bias power of around 10 mW. In Figure 59 we represent the performances for each nanoamplifier's waveguide width. What we can immediately retain from these graphs is that, as expected, such an optoelectronic device finds its usefulness for low-power on-chip applications. In fact, the overall gain stays quite stable at its unsaturated value for low injected power values, on the order of hundreds of nW up to few µW. Then saturation starts to take over, as we can also understand from the Input Saturation Power values. When the input power becomes too high (hundreds of µW to 1 mW) the overall gain tends to 0 dB, meaning that the input signal propagates through the PhC waveguide over the whole amplifier's length and reaches the output with unvaried power level.

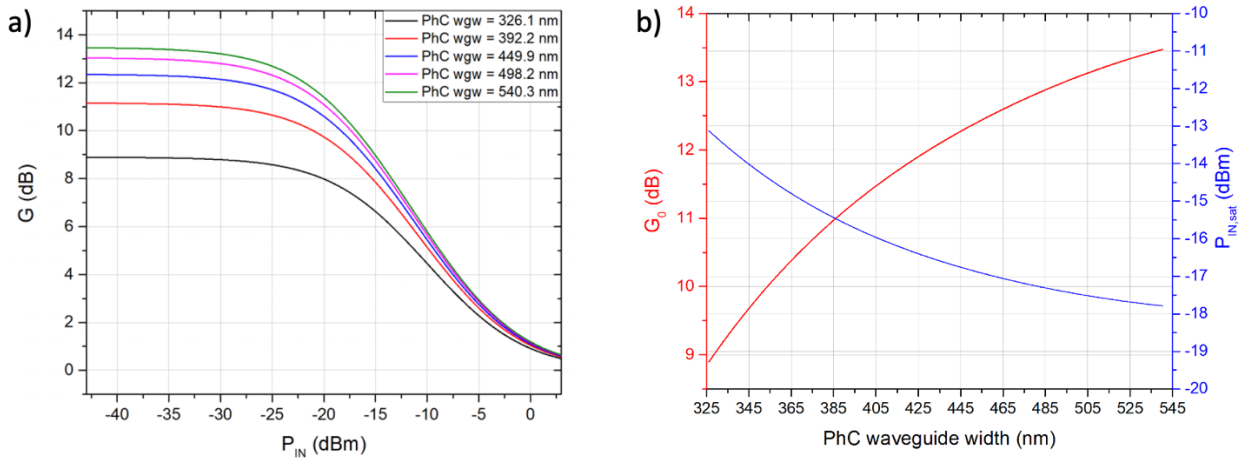


Figure 59: a) Total gain (including saturation) versus input optical power for each PhC waveguide width case; b) unsaturated gain (red) and Input Saturation Power (blue) versus PhC waveguide width. All these results refer to a bias power of 10 mW and an amplifier length of 300 µm

Comparing the performances of each amplifier with different PhC waveguide width, we can state that we are in front of a trade-off: in fact, while a narrower PhC waveguide has higher Input Saturation Power but smaller unsaturated gain, a wider one presents a larger G_0 but for a smaller range of input power. Depending on the required specifications, we can choose the adequate geometry observing the obtained results.

2.8 Conclusion

During this chapter, we have introduced the 2D-PhC structure and designed a nanoamplifier. While on one hand the asymmetric W1 waveguide design allows to efficiently interface the propagating light signal and the injected electrical carriers, on the other hand it permits the propagation of quasi-TE polarized modes, with non-zero vertical electric field component. As a consequence, good care has been taken choosing the PhC geometrical parameters, so to minimize the coupling to unwanted TM-like component.

Two types of mode transformers have been studied to interface the silicon waveguide with the PhC one: the first solution relied on the linear PhC waveguide's n_{eff} variation around the silicon waveguide's one, while the second model was based on the adiabaticity criterion theorized in [74]. Both designs showed coupling efficiencies around 90% or above, with optical bandwidths close to 150 nm; moreover, the adiabatic taper allowed to reduce the mode transformer's length much below 100 µm.

The adopted geometry gave the possibility to increase the confinement factor by at least a factor of four compared to state of the art solutions [18]. This, combined to the reduced device's length

to few hundreds of µm, renders the modeled nanoamplifier suitable for low power applications: as we have seen in the previous subsection, in fact, when the input signal power is limited to few tens of µW the designed nanoamplifier's gain stays fixed at its unsaturated value of around 10 dB for a full amplifier length of 300 µm (considering all the silicon waveguide width cases). The power budget to achieve such performances is around 10 mW. On standard state of the art SOAs [18], we can observe that the same amplification value is obtained for a device's length exceeding 1 mm and for a bias power of the order of several hundreds of mW. The main advantage of our nanophotonic solution is clearly the drastic reduction in terms of power consumption and footprint, making it an extremely interesting candidate for integrated circuit applications. On the other hand, state of the art SOAs show $P_{IN,sat}$ values of the order of hundreds of µW or even few mW, while in our case this parameter is limited to few tens of µW: such a result makes them much more suitable for off-chip high-power applications compared to the device we modeled so far.

We have concluded the discussion about the nanoamplifier's design. Before moving to the next studied device (the nanolaser cavity), we want to comment a possible improvement for this geometry, which surely deserves to be treated in depth for future device's optimizations. In fact, it exists a physical phenomenon for which a light mode can be forced to propagate with a smaller group velocity, called slow-light regime. Such a group velocity reduction, in turns, induces increased light-matter interaction. This effect suggests us that we can achieve the same amount of amplification as a standard PhC nanoamplifier but for a smaller amplifier length, reducing even further the power consumption while increasing the device's on-chip integrability. In the last section of this chapter, we will focus our attention on this fascinating property of light, adapting it to our PhC nanoamplifier.

2.8.1 Future prospect: slow-light nanoamplifier

The group velocity of an optical mode is the velocity an electromagnetic wave propagates through a certain medium, and it is expressed as:

$$v_g = \frac{d\omega}{dk} \tag{2.46}$$

Representing the slope of a PhC band in the dispersion relation. We can relate the group velocity to the speed of light in vacuum c_0 as:

$$v_g = \frac{d\omega}{dk} = \frac{c_0}{n_g} \tag{2.47}$$

Where n_g is the group index. If we focus our attention to the gap-guided band, we can observe that the more we approach the Brillouin Zone's cutoff, the smaller the group velocity (i.e., the stronger the group index) becomes.

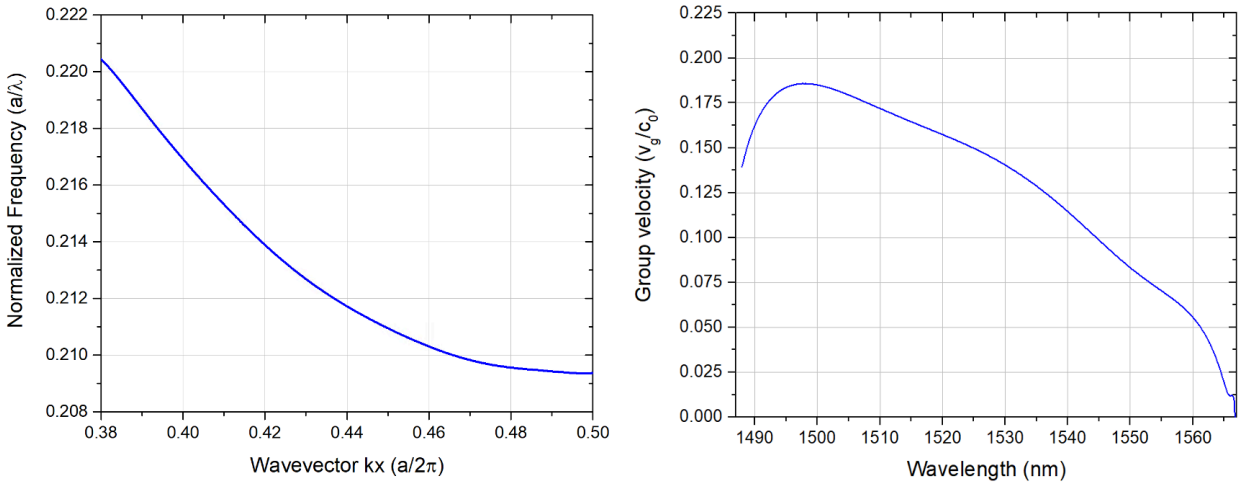


Figure 60: On the left, dispersion relation for the PhC waveguide's gap-guided band; on the right, group velocity evolution as a function of the wavelength

Such a reduction in group velocity is called slow-light regime: when the optical mode is slowed-down, light-matter interactions are enhanced compared to a "standard" group velocity case. If we take advantage of this phenomenon for our nanoamplifier, we can straightforwardly deduce that we could achieve the same amount of gain while reducing the device's footprint. It has been demonstrated, in fact, that the modal gain coefficient can be approximated as [79-80]:

$$g_{mod} = \Gamma \frac{n_g}{n} g_0 \qquad (2.48)$$

Where Γ represents the field overlap with the active material, n_g the group index, n the active material refractive index and g_0 the bulk-material gain. It follows that a stronger n_g gives us a higher modal gain.

However, the main goal would be to maximize not only the group index, but also the bandwidth, in order to exploit the slow-light regime for a certain range of wavelengths. It is possible to tailor the dispersion properties of our PhC waveguide just by applying a local perturbation to the structure's geometry [81-82], as depicted in Figure 61. We applied a local shift on second and third rows of holes, moving them along the structure's transverse direction ($S_2 = -0.2a$, $S_3 = -0.35a$, where $a = 333$ nm is the PhC period) and we obtained a linearization of the PhC gap-guided band, where the group index is increased compared to the unperturbed case and maintained nearly constant for a certain range of wavelengths (in the highlighted case, the group index has a value between 20 and 30 for a wavelength range of 23 nm). Depending on the applied perturbation, we face a trade-off: either we highly increase the group index in a small wavelength range, or we slightly increase the group index for a bigger range of wavelengths. Additionally, while exploiting slow-light, we cannot neglect the effect of disorder. In fact, local perturbation in

the PhC lattice leads to light backscattering and localization [83-85]. Considering that we do not want to build up a PhC cavity, but a PhC waveguide to amplify the propagating optical mode, we cannot increase the group index too much: it is preferable to keep it around few tens.

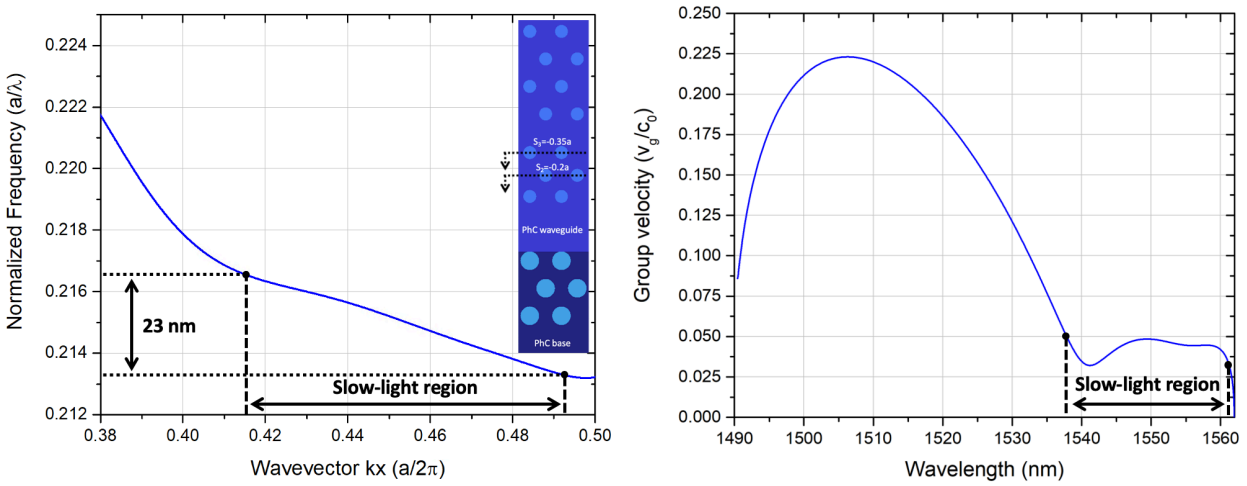


Figure 61: On the left, dispersion relation for the PhC waveguide's gap-guided band (in the inset, schematics top-view of the PhC geometry, indicating the applied local perturbation); on the right, group velocity evolution as a function of the wavelength. The applied local perturbation consists in a transversal shift of second and third rows of holes ($S_2 = -0.2a$, $S_3 = -0.35a$, where $a = 333$ nm is the PhC period)

From the inset on the left-side of Figure 61, we can notice that we drilled additional holes inside the PhC base: another time, the purpose of this was to minimize the electric field's vertical component of the quasi-TE polarized signal, this time for a mode belonging to the gap-guided band. We will analyze the effect of drilling a set of holes in the base more into details during next chapter, when we will study the 2D-PhC structure modeled as a nanolaser device.

If we want to exploit the slow-light regime, we have to engineer also a proper coupling scheme, to efficiently transfer light from the passive silicon circuitry to the slow-light perturbed region of the nanoamplifier. Our study regarding the slow-light nanoamplifier did not go further, due to the lack of time; however, from the literature, we found many interesting solutions to achieve a smooth signal coupling into the slow-light mode [86-90]. The conception of a full PhC slow-light nanoamplifier definitely deserves to be investigated as a future work, in order to further reduce the amplifier's footprint and, as a consequence, improve its performance in terms of power consumption.

Chapter 3: The PhC nanolaser

During this chapter, we will describe the design and modeling of the 2D-PhC structure as a nanolaser source (schematized in Figure 62). Firstly, we will give the theoretical background for the conception of a high quality factor (Q-factor) cavity, introducing the concept of *gentle confinement*. Then we will describe the optical design, extensively commenting on the adopted solution to counteract the geometrical asymmetry (that if not treated would lead to limitation in Q), as well as the electrical one, which is based on the same idea as the nanoamplifier's. After that, we will show the designed coupling scheme with a silicon waveguide, keeping the vertical distance identical to the one chosen for the nanoamplifier. Eventually, we will comment the theoretical performances of the designed device.

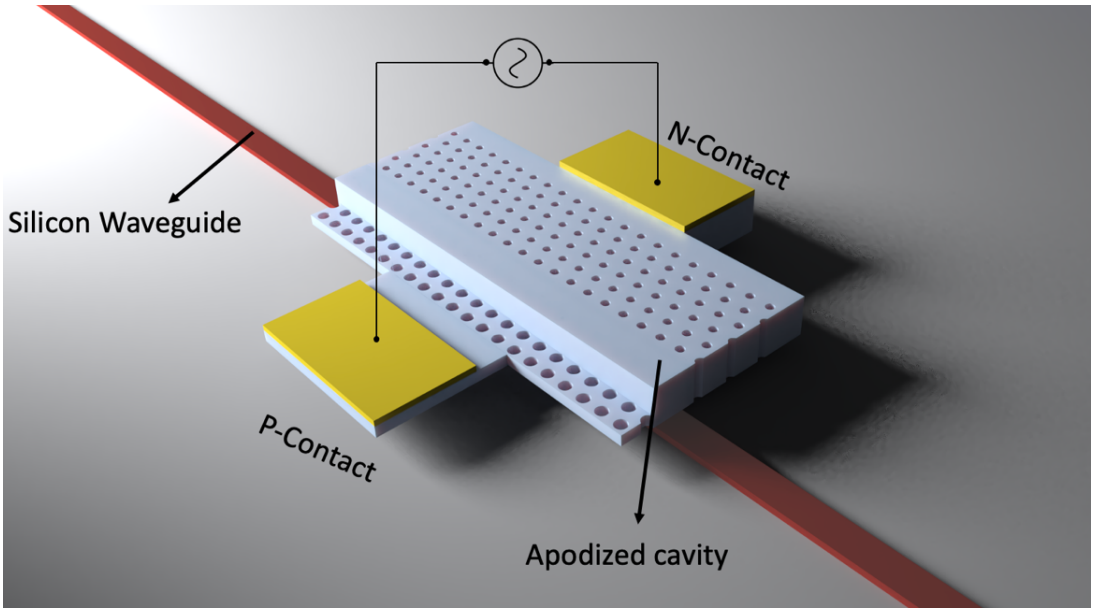


Figure 62: general 3D-schematics of our 2D-PhC apodized cavity

3.1 Design of high-Q PhC cavity: the apodization principle

One of the most efficient methods to design PhC cavities with high Q-factor and small modal volume is the one theorized by Akahane et al. [91] and further implemented by Tanaka et al. [92], consisting in the so-called *gentle confinement* using an "apodized" cavity.

Considering the model of a cavity as depicted in Figure 63(a), we can state that light confinement is achieved in the in-plane direction (x-direction) thanks to the two mirrors placed on both sides of the cavity, while in the out-of-plane direction (z-direction) it is achieved thanks to TIR.

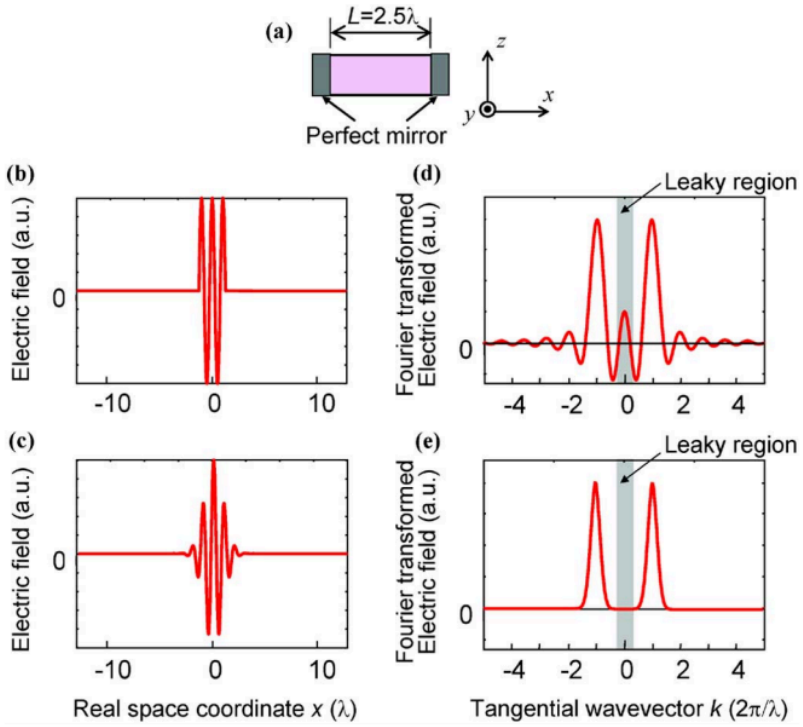


Figure 63: Simplified cavity model (a) analyzing (b) a rectangular and (c) a gaussian envelope function for the cavity's electric field profile. (d) and (e) represent the Fourier Transform spectra respectively for (b) and (c) [92]

Such a model tells us that while the in-plane confinement can be optimized by increasing the mirrors reflectivity, the out-of-plane confinement limits the cavity Q-factor. We can consider the two cases of Figure 63 to better explain this principle, analyzing the EM field distribution in the reciprocal space (Spatial Fourier Transform (FT) of the field plotted as a function of $k_{//}$ is a powerful method to design high-Q cavities). As shown in Figure 63, when light is abruptly reflected at the mirrors interface, the electric field profile has rectangular envelope, giving a "sinc" distribution in the wavevector space (Figure 63(d)). In the figure, the grey zone highlights the leaky region, where $|k_{//}| < k_0$, k_0 being the wavevector of light freely propagating in the cladding material: it is basically the region where light component are not confined by TIR in the vertical direction. As we can observe, the fraction of radiated mode into the cladding is non-zero. On the other hand, if we consider a cavity mode presenting a gaussian electric field profile envelop function like in Figure 63(c), we can notice that the resulting FT presents an almost-zero

component inside the leaky region. We can conclude that the Gaussian EM field apodization is an extremely efficient way to confine a light mode in a cavity, since it allows to minimize the losses in the out-of-plane direction leading to cavities with very-high Q-factor. In the next section we will see how to adapt such a method to our structure to create a 2D-PhC nanolaser apodized cavity.

3.1.1 2D-PhC nanolaser apodized cavity

In order to design the nanolaser cavity with a Gaussian shaped mode, we follow the footsteps of the previous works of our team for the design of high-Q nanobeam PhC cavities [71][93][94], this time applying it to the 2D-PhC geometry. Particularly, we exploit the gap-guided band of the 2D-PhC structure, as represented in Figure 64.

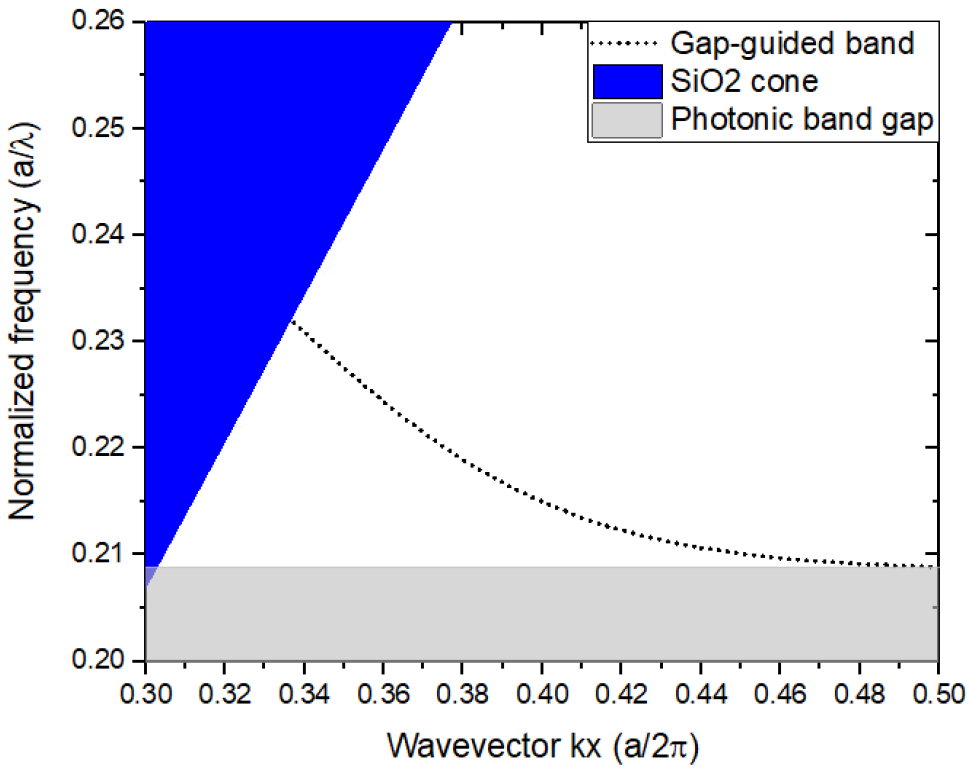


Figure 64: Photonic band diagram for the 2D-PhC configuration, highlighting the gap-guided band

While, for frequencies corresponding to the gap-guided band, the EM field presents a purely real wavevector, it is not the case for frequencies falling in the photonic band gap below this band. The EM field possesses a non-zero imaginary wavevector component q (which varies according to the selected frequency) characterizing the exponential decay of its amplitude ($\sim e^{-qx}$) in space.

Our goal here is to shape the EM field of our cavity mode into a Gaussian, formally described by an envelope function proportional to e^{-Bx^2}, x being the distance from the cavity center (where the gaussian function is at its maximum) and B a constant. Once chosen the resonant wavelength, we set the 2D-PhC geometrical parameters so that:

1) in the cavity center, the electric field of the corresponding light mode has a $q = 0$ (i.e., the selected wavelength is in the gap-guided band);
2) moving away from the central position along the x-direction, we want the resonant EM field to decay ($q \neq 0$) with a Gaussian envelop function. It follows that, to satisfy the *gentle confinement* principle, the decay factor q has to be linearly proportional to x:

$$q = Bx \tag{3.1}$$

In order to meet these requirements, the resonance wavelength must coincide with the gap-guided band's cutoff frequency, satisfying 1); at the same time, in order to fulfill 2), we must perturb one of the structure's geometrical parameters moving away from the cavity center, pushing the operating wavelength more and more inside the photonic band gap while forcing the condition from equation (3.1).

The following steps, then, have to be followed in order to build a 2D-PhC apodized cavity:

- we firstly need to choose which cavity's parameter to play with to satisfy the proportionality between q and x;
- secondly, we set the resonance wavelength (i.e., all the geometrical parameters in order to have the gap-guided band's cutoff at the chosen resonance wavelength) and we calculate the decay factor q as a function of the frequency for different values of the perturbed geometrical parameter;
- then, we need to fix the Full Width at Half Maximum (FWHM) of the Gaussian envelope, that will be a key feature defining the cavity length as well as the Q-factor;
- eventually, knowing the relationship between q and x, knowing the constant B of the Gaussian function thanks to the defined FWHM and knowing the relationship between q and the perturbed geometrical parameter, we are able to define an algorithm telling us how the chosen parameter has to vary along the longitudinal direction starting from the cavity center.

Considering our geometry, consisting in an asymmetric 2D-PhC with a linear defect forming a waveguide, we decided to perturb the waveguide width in order to achieve the gaussian apodization. In fact, while varying the period would limit us in the control and the accuracy of the apodization (the perturbation occurring at each hole, limiting the algorithm's spatial frequency to the PhC period), the waveguide width variation gives us the freedom to design the PhC pattern

and leave it unvaried, just changing the sidewall's position. In this way, we can arbitrarily choose the perturbation's resolution (i.e., the apodization algorithm's spatial frequency).

Before to begin with the apodization algorithm calculation we had to define the general structure parameters in order to work at the gap-guided band's cutoff.

3.1.2 General structure parameters

As we mentioned at the beginning of chapter 2, the adopted III-V membrane has been chosen following the results of [71] (Table 1). We recall here for simplicity the grown materials' electro-optical parameters.

Material	Thickness (nm)	Doping concentration (cm^{-3})	Optical refractive index
i-InP	10	n.i.d.	3.1872
P-InGaAsP	100	P (Zn) $-\ 2 \cdot 10^{18}$	3.3
i-InGaAsP	47.75	n.i.d.	3.3
$\times 5$ { i-InGaAsP_QB	15.5	n.i.d.	3.3
i-InGaAsP_QW	6.3	n.i.d.	3.4
i-InGaAsP	63.25	n.i.d.	3.3
N-InP	120	N (Si) $-\ 2 \cdot 10^{18}$	3.1872
TOTAL	450		

Table 5: (same as Table 1) Electro-optical parameters of the adopted epitaxy for the conception of a nanolaser cavity

In order to exploit the gap-guided band's cutoff, we set the following geometrical parameters for our 2D-PhC structure:

- periodicity $a = 333$ nm;
- holes' radius $r = 72$ nm;
- PhC waveguide width $wgw = 0.9 \cdot a\sqrt{3} = 519.1$ nm.

The resulting band diagram is shown in Figure 64.

Note that the cutoff wavelength has not been chosen to be 1550 nm but rather around 1590 nm: As we will see during the characterization chapter, the fabricated nanolaser emitted at wavelength of about 45 nm smaller than the designed one. So, in order to fabricate a laser with emission wavelength around 1550 nm. we readapted the design increasing the modeled cavity resonance up to 1590 nm.

Up to now, we have fixed the general 2D-PhC structure parameters (consequently setting the laser working wavelength) and have chosen to apply a perturbation on the sidewall's position (varying the PhC waveguide width) in order to build the apodization algorithm. It is now time to calculate the electric field's decay factor q as a function of the propagating mode's wavelength for different PhC waveguide widths.

3.1.3 Decay factor evaluation

The analysis of the field attenuation inside the photonic band gap was conducted using the software *Lumerical FDTD Solutions*. The simulation setup is quite straightforward: we want to inject an optical mode (thanks to a mode source) inside our 2D-PhC waveguide and study the transmission, to see whether it propagates unvaried towards the output or if it is attenuated. In that way, thanks to a linear monitor deliberately placed in the waveguide center, we are able to record the field intensity along the propagation direction for a wide range of wavelengths, so to fully analyze the photonic band gap as well as the waveguide bands. Just like for the nanoamplifier, the material surrounding the III-V geometry was set to be silica, since, as we will see during the fabrication chapter, this material was used as an encapsulation layer and as a bonding inter-layer directly in contact with the III-V material. Figure 65 shows the schematic top-view and the result of the described simulation.

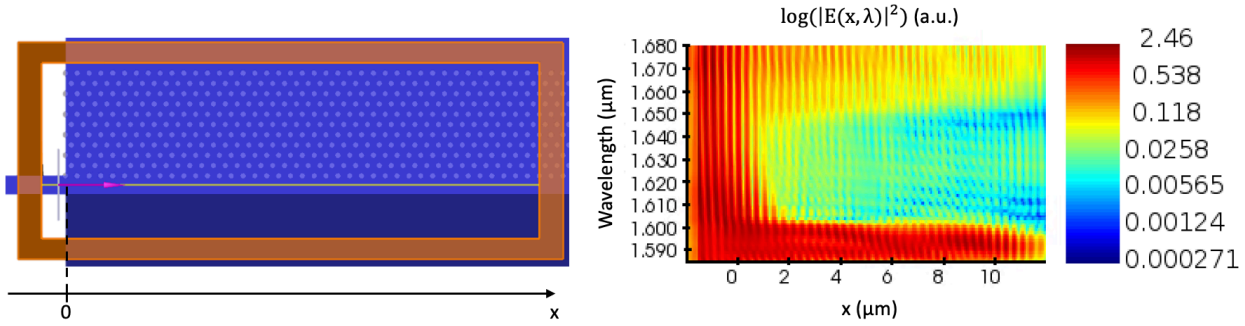


Figure 65: On the left, schematic top-view of the FDTD simulation. An optical mode is injected inside the PhC waveguide and its transmission is then evaluated with a linear field monitor. The resulting field intensity as a function of the longitudinal direction and the mode's wavelength is then plotted (on the right), showing the opening of a photonic band gap around 1600 nm

As we can observe from the schematics on the left-side, the optical mode is injected by means of a mode source placed inside a ridge waveguide before the PhC pattern. The ridge waveguide is designed so that its effective index matches the one of the PhC waveguide, in order to efficiently inject the signal and avoid back-reflections. The darker-blue region below the PhC pattern represents the base of the device. There, the P-contact to inject positive-charge carriers inside

the waveguide's active region was not considered. The orange rectangle surrounding the full structure defines the simulation region, while the yellow line placed at the PhC waveguide's center is the linear field monitor, saving the field evolution during propagation for a certain range of wavelengths. The simulation result is depicted on the right-side of Figure 65: we can observe that for the shortest wavelengths the mode propagates until to the end without any attenuation, suggesting that we are inside the gap-guided band. For wavelength large than 1600 nm, the EM filed intensity spatially decays in the structure indicating the opening of a photonic band gap. For each wavelength falling inside the band gap, it is possible to demonstrate that the field decay can be fitted by a function given by the product of a cosine and an exponential decay:

$$E \propto e^{i\frac{\pi}{a}x} e^{-qx} \tag{3.2}$$

In that way, we are able to extract the q values as a function of the mode's wavelength, as depicted in Figure 66.

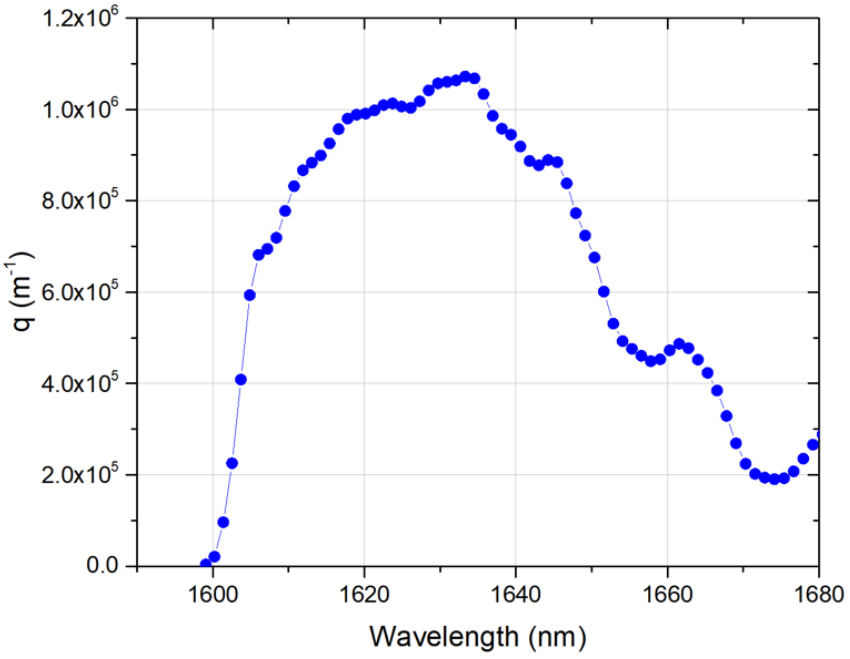


Figure 66: decay factor q as a function of the propagating mode's wavelength; the waveguide width has been fixed to $0.9 \cdot a\sqrt{3} = 519.1$ nm

The gap-guided cutoff wavelength is obtained at 1599 nm. Increasing the wavelength, the attenuation becomes more and more important, as the mode falls deeper in the photonic band gap. The maximum attenuation is reached around 1630 nm, before decreasing with some local maxima and minima.

Thanks to this simulation we are finally able to fix the cavity's resonance wavelength to the cutoff frequency of the studied band, corresponding to a value of 1599 nm. The following step is to repeat the same simulation for different waveguide widths, so to shift the gap-guided band and push the chosen working wavelength inside the photonic band gap. In this way we are able to establish a relationship between the waveguide width and the attenuation factor q. Figure 67 reports the evolution of q as a function of the PhC waveguide width when the wavelength is fixed at 1599 nm.

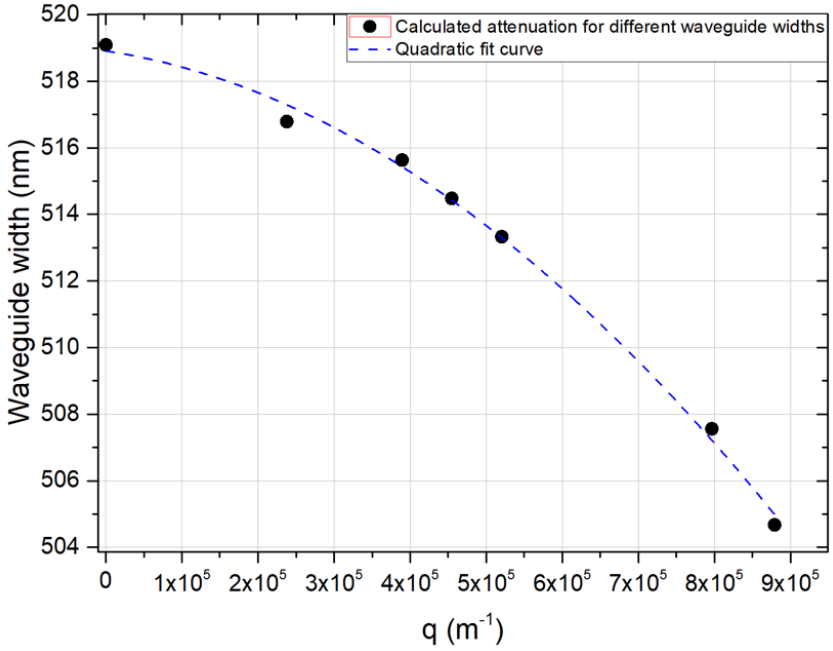


Figure 67: Relationship between attenuation factor q and PhC waveguide width and related fit. The working wavelength is set to 1599 nm

The q variation as a function of the PhC waveguide width can be efficiently fitted by a quadratic function. From now on, considering that we are designing a resonant cavity, we will refer to the PhC cavity width rather than the PhC waveguide width.

Now that the signal attenuation inside the photonic band gap as a function of the chosen structure's geometry is determined, it is time to build the Gaussian apodization algorithm.

3.1.4 Gaussian apodization algorithm

As previously introduced, our cavity mode must have a Gaussian shape of the form e^{-Bx^2} along the longitudinal direction, in order to minimize the out-of-plane losses. This leads to the linear relation between the field's decay factor and longitudinal position $q = Bx$. We need then to

calculate the constant B in order to find the q evolution as a function of the position along the cavity. The FWHM is defined as:

$$\mathrm{FWHM} = 2\sqrt{\frac{\ln(2)}{\mathrm{B}}} \tag{3.3}$$

This equation tells us that once arbitrarily fixed the FWHM for our gaussian mode, we can calculate the constant B and, consequently, q as a function of x.

At this point, we had to face a tradeoff choosing the FWHM and the minimum cavity width $\mathrm{W_{min}}$ (i.e., the maximum field's decay factor $\mathrm{q_{max}}$ inside the cavity). Our goal was to design a cavity with the highest possible Q-factor but by ensuring single mode operation. These 2 parameters control almost entirely these properties.

On the one hand, for a fixed $\mathrm{W_{min}}$, a large FWHM allows to reduce the fraction of Gaussian field's FT component inside the leaky region, thus increasing the fundamental mode's Q-factor; at the same time, however, by increasing its size, the cavity may become multimodal as the Free Spectral Range (FSR) would be reduced and higher order cavity modes may fit inside the photonic band gap's spectral bandwidth. On the other hand, for a fixed FWHM, ideally the cavity should exploit the full range of W (i.e. exploiting that of q) in order to shape as good as possible the EM field into a Gaussian. However, $\mathrm{W_{min}}$ is also a key parameter to render our cavities single mode: the chosen $\mathrm{W_{min}}$ fixes the lower limit in wavelength of the cavity mirrors spectral bandwidth due to the dependence of the photonic band diagram on W. This way, by not reducing $\mathrm{W_{min}}$ to the value where q reaches its maximum value, allows to filter out higher order modes from the photonic band gap's spectral bandwidth. We decided, then, to fix FWHM to 3 µm and $\mathrm{W_{min}}$ to 506.1 nm (leading to a q of around $0.83 \cdot 10^6\ \mathrm{m^{-1}}$).

We have now all the ingredients to build the cavity's geometry following the apodization algorithm, since:

1) we know the relationship of q with the position along the cavity through the constant B of the Gaussian function (determined by the selected FWHM);
2) we previously extracted the q variation as a function of the waveguide width (Figure 67), which combined with 1) allows us to determine how the cavity width has to vary along the device's length;
3) we have set $\mathrm{W_{min}}$.

We can appreciate the perturbation to apply to the cavity width as a function of the distance from the cavity center in the next graph.

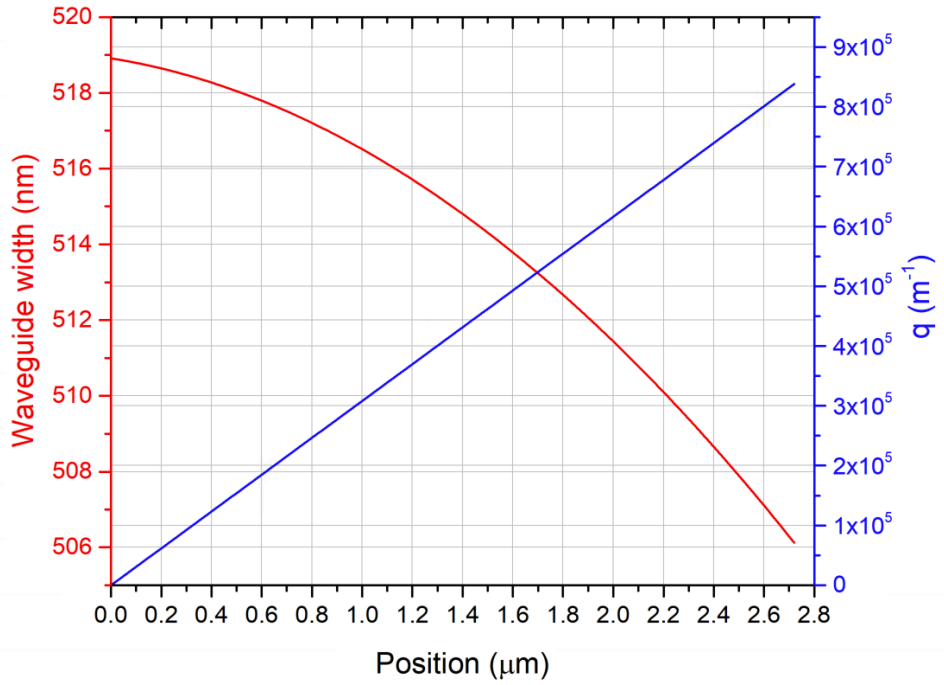


Figure 68: Final gaussian apodization algorithm; the cavity extends on both sides of its center for a length of 2.72 µm and the cavity width varies from 519.1 nm to 506.1 nm

From this figure, we can observe that the cavity extends on both sides of its center for a length of 2.72 µm, leading to a total apodization region length of 5.44 µm. Particularly, we want to highlight the fact that the cavity width variation to achieve is less than 20 nm, confirming that the device we are designing belongs to the nanostructures family.

In the next section we will present the full cavity simulation and we will comment the results, showing that we still miss one piece of the puzzle for the design of an efficient single mode nanolaser cavity.

3.2 Intrinsic 2D-cavity simulation

Figure 69 shows the top-view schematics of the simulation setup. The goal of such a simulation is to evaluate the resonant wavelength as well as the Q-factor of the nanolaser cavity. We will refer to that structure as the intrinsic 2D-cavity, since the simulation is set so to study the device on its own, without any other entity coupled to the system. In the top-view schematics, the 2D-PhC base is shown in dark-blue. The simulation region is delimited on each side by an orange layer, representing the Perfectly Matched Layers (PMLs) of the boundary conditions. On the left-side of the simulation region there is a blue shading highlighting that a symmetry has been applied to the system in order to reduce the simulation time: the system's geometry, in fact, is symmetric with respect to the cavity center (highlighted with the vertical orange line).

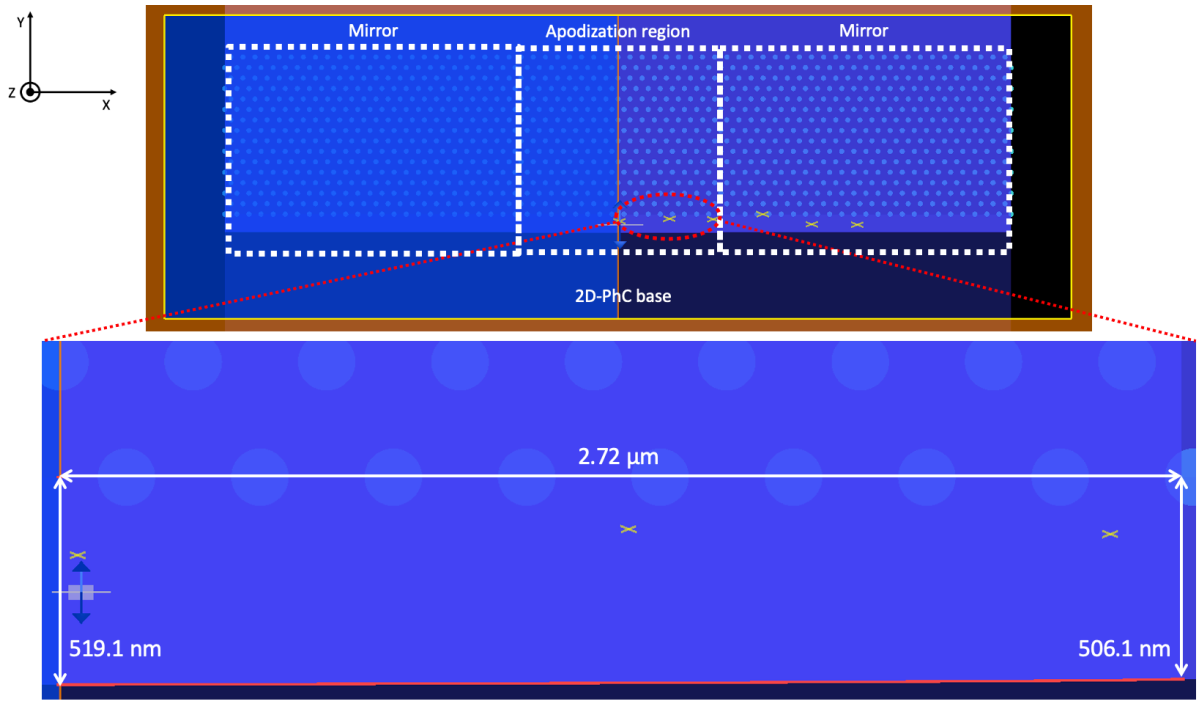


Figure 69: Top-schematics view of the intrinsic 2D-cavity simulation; the close-up view shows the apodization region, where the wall position varies according to the obtained algorithm to vary the PhC cavity width. On the left of the close-up view we can appreciate the electric dipole source, properly oriented to excite TE cavity modes

To build the cavity, we have applied the apodization algorithm just perturbing the PhC waveguide's sidewall: in fact, as previously explained, controlling the sidewall's position gives us the possibility to choose the resolution for the apodization (i.e., the spatial frequency to apply for the local sidewall's perturbation along the longitudinal direction x), leaving the holes position unvaried. We decided to work with a spatial resolution of 10 nm. As we can observe from the close-up view, the wall position variation is highlighted in red. Beyond the apodization region, the structure is extended by fixing the PhC cavity width to 506.1 nm, to provide further longitudinal confinement of the electromagnetic field ("mirror" regions in Figure 69). The longer this extension is, the weaker the losses are. We chose to fix its length to 38 PhC periods, corresponding to a length of 12.5 µm.

The idea behind the simulation is straightforward: we place an electric dipole source close to the cavity center properly oriented so to only excite TE modes in a wide range of wavelengths. In that way, only the resonant mode selected by the apodization algorithm is trapped inside the cavity. Once the simulation time has been set, the goal is to analyze, thanks to time monitors appropriately placed along the PhC cavity (yellow crosses in Figure 69), the trapped EM field evolution in time, to estimate the cavity's resonant wavelength and Q-factor. While for the former it is sufficient to apply the FT of the field over time to analyze the frequency spectrum,

for the latter we can take advantage of the fact that the field evolution in time inside the cavity can be expressed by an exponential decay of the form $e^{-t/\tau}$, where τ is the field's decay time. The Q-factor, expressing the ratio between the stored and the dissipated energy in a resonant system, can be expressed as:

$$Q = \frac{\omega_0 \tau}{2} \tag{3.4}$$

Where ω_0 is the resonant mode's pulsation. For all the simulations, the simulation time has been set to 17 ps.

However, the simulation result was not satisfying: although the cavity proved to be a single-mode and the obtained resonance wavelength (1597 nm) was in good agreement with the one set at the beginning of the design (1599 nm), the calculated Q-factor was 7764, which was quite low compared to previous works on 1D nanocavities made by our group (with Q-factors exceeding 10^5).

3.2.1 Quasi-TE resonant mode

It is possible to retrieve the origin of such a low Q-factor by observing the resonant field components. In fact, even though our design was supposed to accept only TE resonant modes, it turned out that the cavity mode presented a non-negligible vertical component E_z as well, as we can see in Figure 70.

As explained in [95], in conventional triangular lattice 2D-PhC structures with circular holes, there is no photonic band gap for TM polarization: it means that in our structure the fraction of resonant mode presenting TM component is not trapped inside the apodized cavity but gets lost inside the PhC pattern through the mirror regions, dropping the Q-factor. Similarly to the nanoamplifier case, the presence of a non-negligible TM component seems to be related to the asymmetry of the cavity. In fact, we are not dealing with a classical 2D-PhC waveguide, where the mode is confined on both sides thanks to the holes lattice symmetrically placed with respect to the waveguide center. In our case the mode confinement is achieved on one side thanks to the PhC lattice and on the other side thanks to a rib-like geometry (composed by structure's base and sidewall).

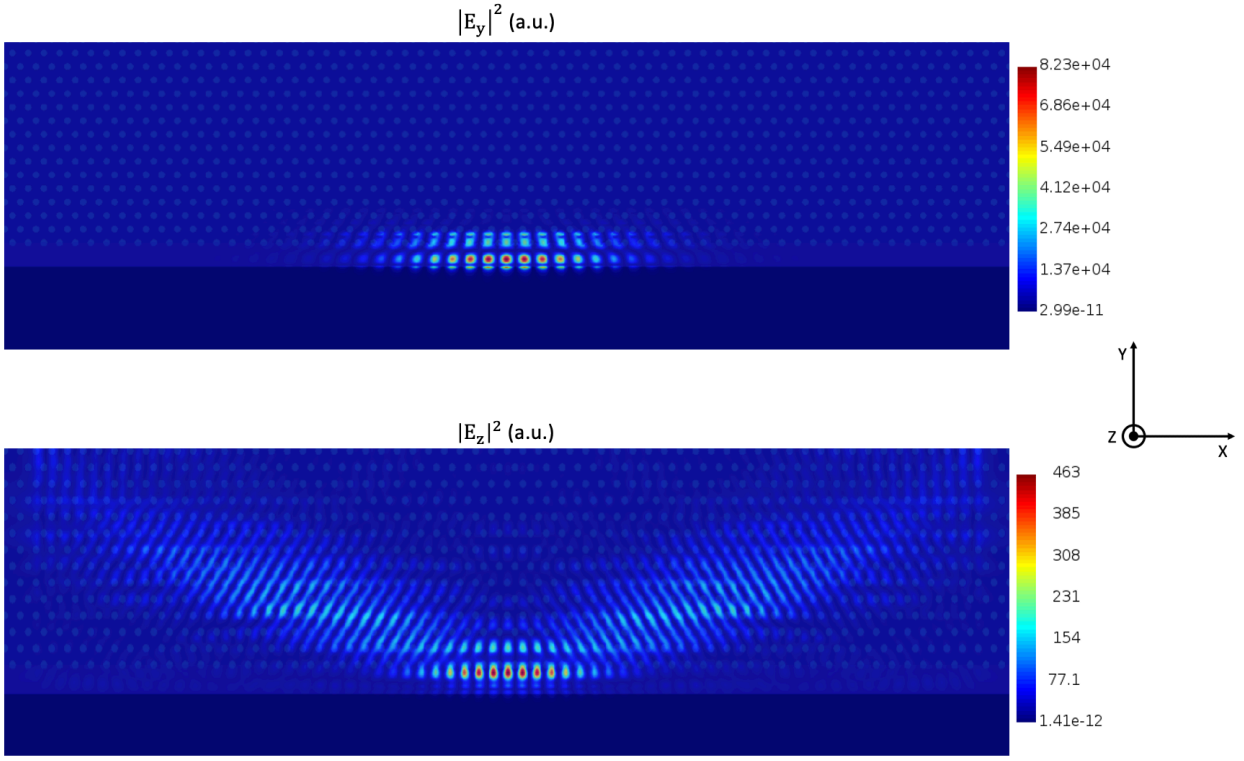


Figure 70: E_y (top) and E_z (bottom) resonant mode components from a top view. It is remarkable the appearance of a TM component drastically reducing the Q-factor

In order to validate such an observation, we performed another simulation where we redesigned the 2D-PhC apodized cavity, this time removing the P-doped base. In that way we increased the structure's symmetry, since in addition to the previous plane of symmetry (along the YZ surface and placed at an X corresponding to the cavity center, referring to Figure 70) there is a second one along the XY surface, placed at a Z coordinate another time cutting the cavity in half. Such a cavity gave nice results, since it showed single-mode behavior with a Q-factor increased up to $2.5\ 10^6$. It is also remarkable that, just by removing the base, the TM-like component is not only reduced but it is completely eliminated, with the appearance of a purely TE polarized resonant mode.

This result confirmed our suspicions regarding the structure's asymmetry. Particularly, it turned out that the main limitation was due to the presence of the base: however, while from an optical point of view it may represent a limitation, from an electrical perspective it is a fundamental block for the overall device, since it enables the structure's electrical pumping. We needed then to find an alternative design, in order to keep the base while minimizing the resonant mode's electric field vertical component.

3.2.2 TM component minimization: additional holes in the base

The adopted solution to counteract the asymmetry introduced by the base was to drill an additional holes pattern inside the base. The idea behind is to render the structure more symmetric by reducing the n_{eff} of the base by partially removing material. We readapted then the apodization algorithm, without varying the 2D-PhC holes radius (72 nm), the period (333 nm), the starting PhC cavity width ($0.9 \cdot a\sqrt{3} = 519.1\ \mathrm{nm}$) and the base thickness (80 nm) and introducing additional rows of holes in the base, with the same triangular lattice configuration and same period as the 2D-PhC pattern. The mirror regions were still 38 PhC periods long. Figure 71 shows the new schematics. The holes pattern in the base is displaced so that its first row is tangent to the PhC sidewall.

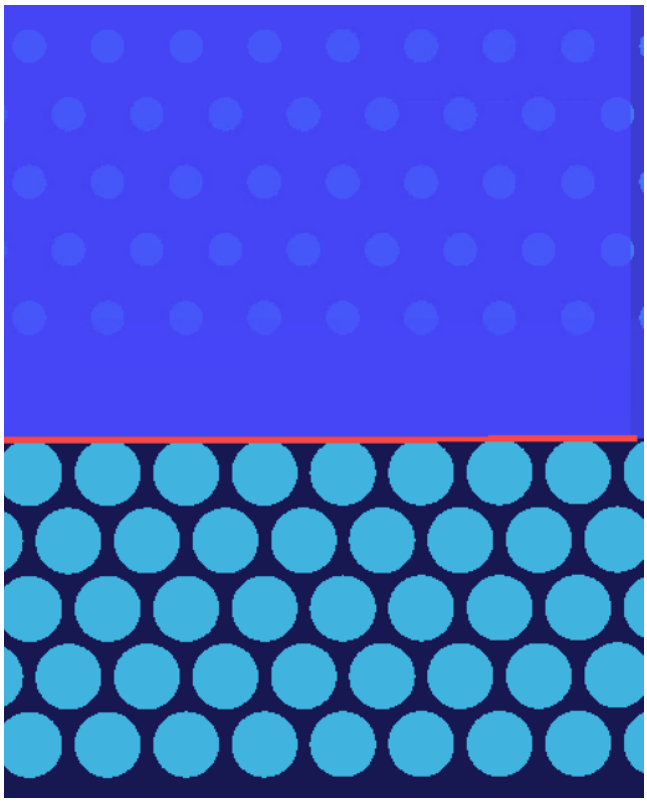


Figure 71: Close-up top-view of the apodization region (highlighted in red) with the new holes pattern in the base (dark violet)

This first simulation with 5 rows of holes in the base each one with a radius of 140 nm showed very good cavity performances, with a resonance wavelength of 1588 nm and a Q of $4.35 \cdot 10^5$. Unfortunately, such a structure is difficult to fabricate as the hole-to-hole distance in the base is only 53 nm, rendering it very fragile. Additionally, such a small fraction of available P-doped

material would dramatically increase the structure resistance, making the electrical carriers injection much trickier and less efficient. We studied, then, the Q-factor behavior for different radius of the holes in the base (R_{base}), as reported in Figure 72. This study was made reducing the number of rows from 5 to 3, since the Q-factor remained essentially unvaried for the reference case with $R_{base} = 140\ nm$.

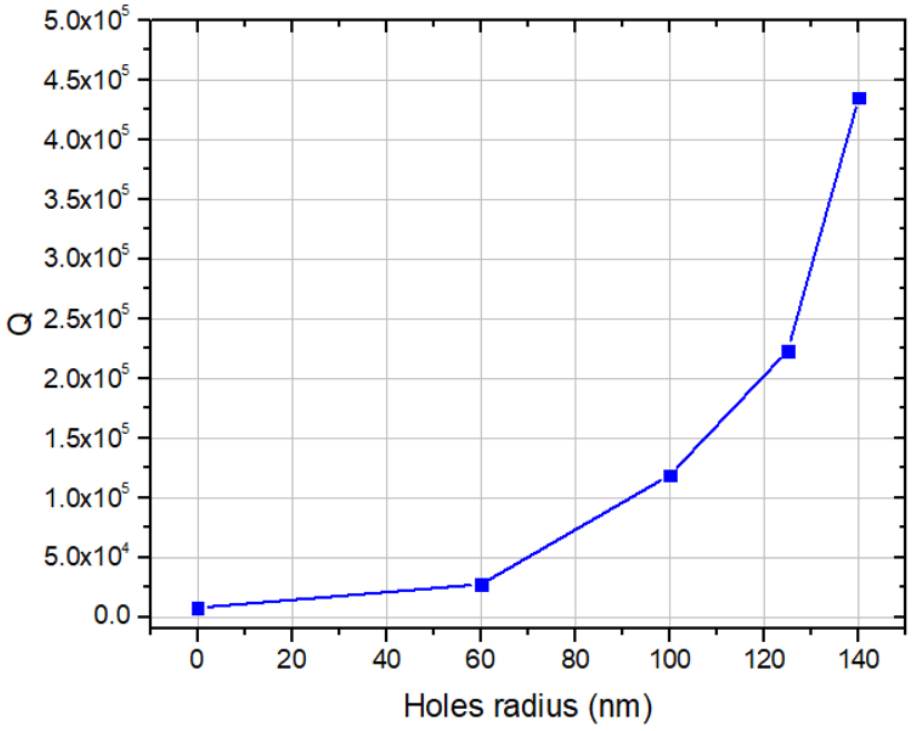


Figure 72: Q-factor evolution as a function of R_{base}

We can notice that the Q-factor stays below $5 \cdot 10^4$ for radii smaller than 70 nm, and quickly raised for greater ones. For the kind of structure we want to build, we considered that a Q-factor of 10^5 was enough, which corresponds to a radius of 100 nm (giving a Q-factor of $1.19 \cdot 10^5$). For the rest of the nanolaser design chapter, we will keep R_{base} fixed to 100 nm.

Additionally, we observed that we could improve the device's footprint by reducing the mirror region's length: in fact, designing each mirror with 25 PhC periods instead of 38 slightly reduced the Q-factor from $1.19 \cdot 10^5$ to $1.06 \cdot 10^5$, which we still considered as an acceptable value. We also studied the performances by varying the number of rows of holes in the base (Figure 73). Our goal was to minimize them for a more favorable electrical injection while providing an acceptable Q-factor.

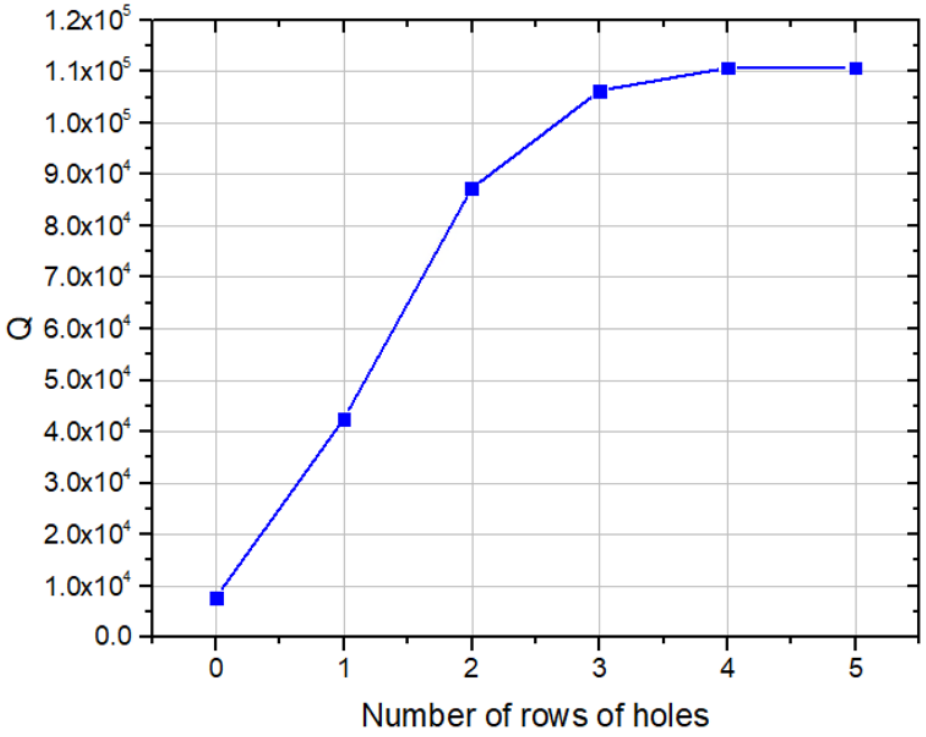


Figure 73: Q-factor evolution as a function of the number of rows of holes in the base

Starting from 3 rows of holes in the base, the average index felt by the electromagnetic field confined in the PhC cavity remains practically unvaried, explaining why the cavity's Q-factor saturates at values slightly above 10^5. We can notice also that the resulting Q-factor placing just 2 rows of holes is very close to our target value of 10^5 ($8.7 \cdot 10^4$), while 1 row or no-rows of holes reduce too much the Q-factor.

Another important parameter to consider for the final nanolaser configuration is the P-metal distance from the PhC sidewall. In fact, as already mentioned in the previous chapter, while on one hand we wanted to put it as close as possible to the PhC cavity to improve the holes injection efficiency, on the other hand putting the P-metal too close would introduce large optical absorption, limiting the cavity's Q-factor. For this analysis, we used a cavity with 3 rows of holes in the base with a radius of 100 nm. From Figure 74 we notice that for distances close to 800 nm or higher the Q-factor remains almost constant, suggesting that the P-metal is far enough to avoid significant signal absorption. As a consequence, we decided for the structure modeling to fix the P-metal distance to 850 nm; that result pushed us to set the same P-metal distance for the nanoamplifier, as we have already seen during the previous chapter.

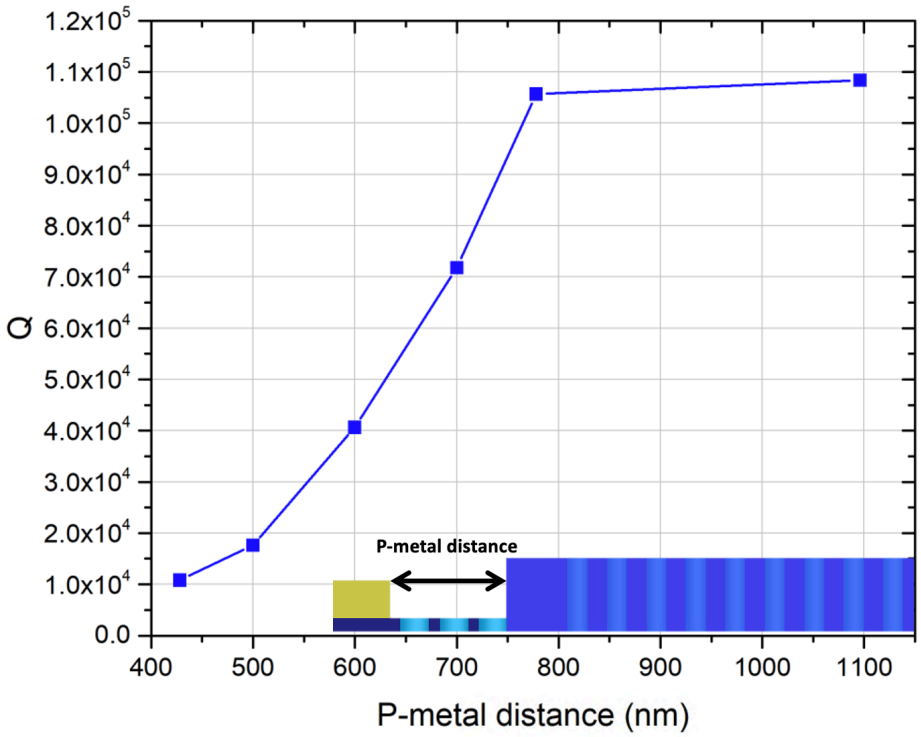


Figure 74: Q-factor variation as a function of the P-metal distance from the PhC sidewall (in the inset, cross-section schematics highlighting the P-metal distance)

3.2.2.1 Final design

The last modification we brought to the system was on the PhC base: more precisely, we did not want to inject electrical carriers on the full structure's length, but only inside the area covered by the Gaussian cavity mode, whose longitudinal profile can be observed in Figure 75. The FWHM is a little bit higher than expected (around 3.6 µm compared to the target value of 3 µm) and the gaussian tails drop below 5% of the top signal level at a distance of 4 µm from the cavity center. Thus, we chose to reduce the base length (and consequently, the P- and N-metal pads length) to 25 PhC periods, corresponding to a total length of 8.325 µm. As we will see during the electrical simulation section, such a decision on the base width proved to be quite efficient, since the injected electrical carriers' longitudinal profile properly overlapped with the Gaussian optical mode. We left however a small part of the base at the foot of the PhC sidewall so to drill 2 rows of holes along the full nanolaser length: our intention was to prevent signal diffractions at the interface between the central part of the cavity, where the base remained unvaried, and the mirror sides, where we wanted to remove the base.

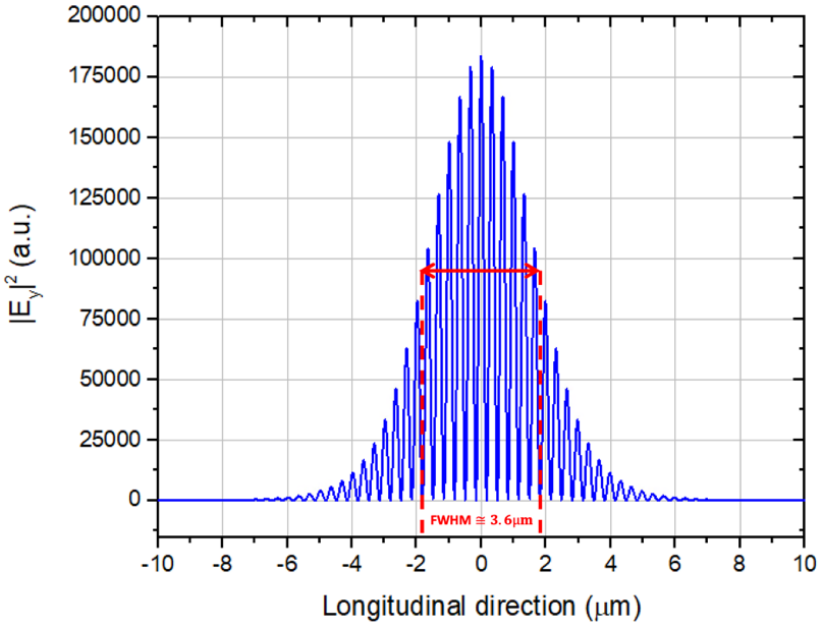


Figure 75: Gaussian cavity mode profile

We show, in Figure 76, the final 3D-model of our single-mode nanolaser cavity, emitting at a wavelength of 1591 nm with a Q-factor on the order of 10^5.

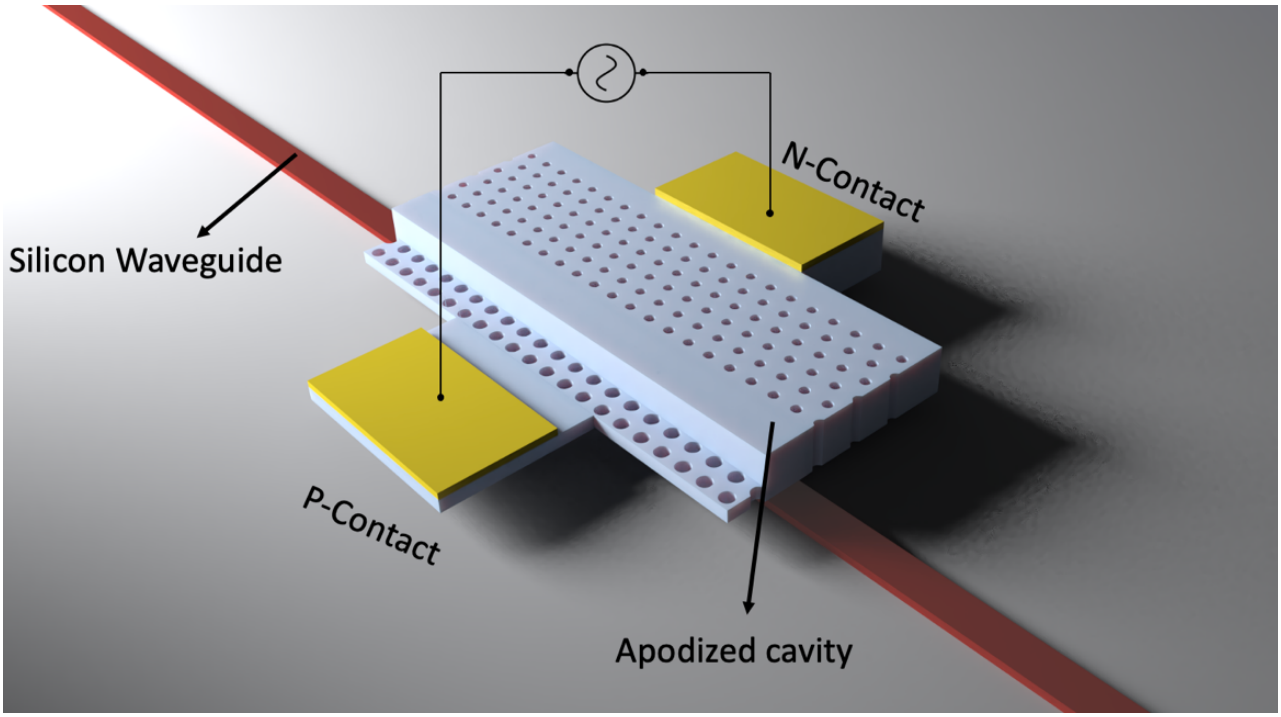


Figure 76: general 3D-schematics of our 2D-PhC apodized cavity (same as Figure 62)

The last study we performed before moving to the coupling between nanolaser and passive circuitry was on the introduction of the doped layers inside the geometry. In fact, in the optical simulation we have showed up to now, the InP material composing the geometry was considered without any absorption. However, when we dope a material, we also introduce an imaginary part to the refractive index, which describes the optical loss by free carrier absorption: as we have seen during the nanoamplifier chapter, typical bulk losses for N-type and P-type doped InP-based materials with a doping level of $1 \cdot 10^{18}$ cm^{-3} and at a wavelength of 1500 nm are respectively 4 dB/cm and 56 dB/cm [21]. For the chosen P and N doping levels of around $2 \cdot 10^{18}$ cm^{-3} we calculated that the nanolaser Q-factor dropped to $2.8 \cdot 10^4$. However, as we will see in the next section, a cavity with such an intrinsic Q-factor can be properly interfaced with a silicon waveguide and still present a total Q-factor high enough to observe laser emission.

3.3 Evanescent wave coupling

So far, we have designed a single-mode nanolaser cavity with high Q-factor and small modal volume. However, in order to exploit this structure for real applications, we also need to engineer an efficient coupling scheme to extract the laser signal. In this section, we will show the design of the hybrid nanolaser on SOI platform, exploiting the same waveguides dimension as well as the same evanescent coupling mechanism we showed during the nanoamplifier chapter.

Referring to the evanescent coupling between two waveguides, in chapter 2 we have seen that the EM field intensity inside each waveguide is:

$$|a_1(x)|^2 = a_1(0)^2 \left(\cos^2(\beta_0 x) + \left(\frac{\beta_1 - \beta_2}{2\beta_0} \right)^2 \sin^2(\beta_0 x) \right) \tag{3.5}$$

$$|a_2(x)|^2 = \frac{\kappa^2}{{\beta_0}^2} a_1(0)^2 \sin^2(\beta_0 x) \tag{3.6}$$

Where β_1 and β_2 are the propagation constants of a mode propagating respectively in waveguide 1 and 2, κ is the coupling coefficient determining the overlap between the coupled modes and $\beta_0 = \sqrt{\left(\frac{\beta_1 - \beta_2}{2} \right)^2 + |\kappa|^2}$. Particularly, at phase-matching ($\beta_1 = \beta_2$) we have:

$$|a_1(x)|^2 = a_1(0)^2 \cos^2(\kappa x) \tag{3.7}$$

$$|a_2(x)|^2 = a_1(0)^2 \sin^2(\kappa x) \tag{3.8}$$

These expressions tell us that the key parameters to achieve efficient coupling are the propagation constant β and the coupling coefficient κ. The closer the two propagation constants are, the higher the percentage of mode in waveguide-1 transferred into waveguide-2 will be.

Parallelly, the larger the coupling coefficient is, the shorter the distance to transfer the signal becomes.

Coupling a cavity to a waveguide works almost the same. Our cavities are constructed in such way to obtain a Gaussian profile of EM field not only in the direct space but also in the reciprocal one. We can show that the EM field distribution of the cavity's resonant mode is composed of 2 gaussians centered around $k = \pm\frac{\pi}{a}$. It follows that the closer the SOI waveguide's propagation constant is to this wavevector, the more efficient the signal transfer will be. In order to find the best configuration, we tuned the silicon waveguide's propagation constant by varying its width, considering the available waveguide widths in the ordered SOI chips. We also chose to fix the vertical distance to 230 nm, as for the nanoamplifier. In order to tune the coupling coefficient, we played on the lateral misalignment between the silicon waveguide and the PhC apodized cavity.

3.3.1 Coupling efficiency

The cavity we have studied in the previous sections was intentionally not coupled to the external world, meaning that the Q-factor we were referring to described the cavity's intrinsic behavior. However, when we couple the 2D-PhC cavity to a silicon waveguide, we have to consider a new channel of "loss", as schematized in Figure 77.

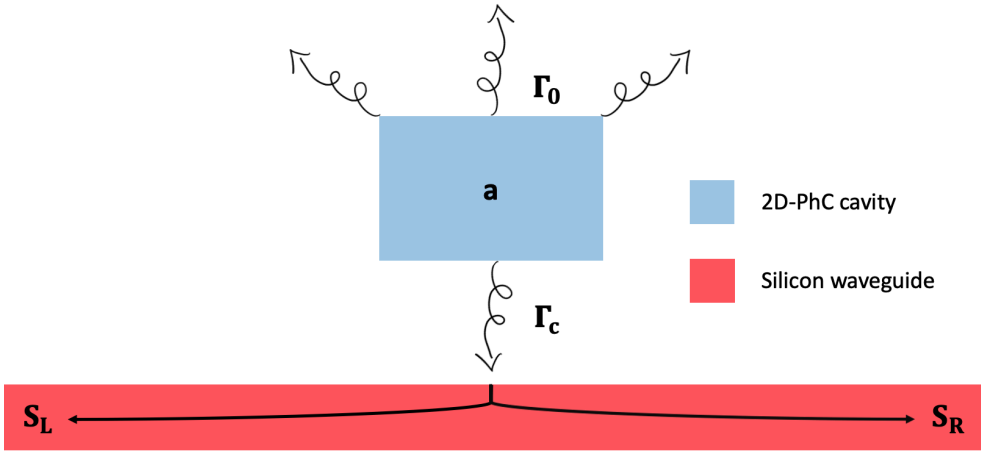


Figure 77: Schematics of the coupled system composed by the 2D-PhC cavity and the silicon waveguide

This schematics represents a resonant cavity with a cavity mode electric field a, coupled to a silicon waveguide whose coupling is described by the quantity $\Gamma_c = {}^{1}/_{\tau_c}$, expressing the cavity's evanescent coupling losses (τ_c being the coupling lifetime). The cavity internal losses are

described by the quantity $\Gamma_0 = \Gamma_{tr} - \Gamma_g = {}^{1}/_{\tau_0}$, where Γ_{tr} represents the cavity losses in absence of active medium and Γ_g the gain/losses of the active medium (if positive it represents gain, if negative losses). $S_{L,R}$ represent the propagating waves inside the silicon waveguide, originated from the cavity. It is possible to describe the full system with the total factor $\Gamma_{tot} = \Gamma_0 + \Gamma_c = {}^{1}/_{\tau_0} + {}^{1}/_{\tau_c} = {}^{1}/_{\tau_{tot}}$. As we have seen previously during this chapter, the Q-factor can be expressed as $Q = {}^{\omega_0 \tau}/_{2}$, meaning that we can introduce new Q-factor expressions to describe the coupled system which are related between each other by the relation:

$$\frac{1}{Q_{tot}} = \frac{1}{Q_0} + \frac{1}{Q_c} \tag{3.9}$$

For the intrinsic cavity, we had $Q_{tot} = Q_0$, since no external entity was coupled. Now, with the introduction of a silicon waveguide, we are adding up the Q-factor related to coupling Q_c, which reduces the total cavity Q-factor. To complete the system description, we can also introduce the coupling efficiency, described by the ratio between the rate of optical losses from the PhC cavity to silicon waveguide and the rate of total optical losses:

$$\eta = \frac{{}^{1}/_{\tau_c}}{{}^{1}/_{\tau_{tot}}} = \frac{{}^{1}/_{\tau_c}}{{}^{1}/_{\tau_c} + {}^{1}/_{\tau_0}} = \frac{Q_0}{Q_0 + Q_c} = \frac{1}{1 + {}^{Q_c}/_{Q_0}} \tag{3.10}$$

Equation (3.10) tells us that the signal transfer from nanolaser cavity to silicon waveguide is determined by the ratio ${}^{Q_c}/_{Q_0}$. When Q_c is much smaller than Q_0, the system is efficiently coupled, with η approaching 100%. However, when Q_c becomes too small, Q_{tot} diminishes accordingly, deteriorating the nanolaser performances in terms of power budget to attain the lasing regime. On the other hand, when ${}^{Q_c}/_{Q_0}$ is too large, the coupling efficiency tends to zero and Q_{tot} approaches Q_0, the system becoming more and more similar to the intrinsic case.

3.3.2 Coupled system simulation

3.3.2.1 Simulation setup

In order to find the optimal configuration maximizing both Q_{tot} and η, we ran some FDTD simulations studying the coupled system, where we varied alternatively the silicon waveguide width and the shift between the silicon waveguide and the 2D-PhC cavity. We took always the same cavity as reference, with 3 rows of holes in the base with radius 100 nm which exhibits a $Q_0 = Q_{tot} = 10^5$ in the intrinsic case. As already mentioned, the vertical distance between the cavity and silicon waveguide has been fixed to 230 nm. The simulation was organized as follows: similarly to the intrinsic cavity simulation, the EM field was excited by means of a dipole source and the resulting Q_{tot} was extrapolated from a set of time monitors measuring the field's time

evolution. Then, 2D power monitors were placed at each simulation region's edge and around one extremity of the silicon waveguide, so to extract respectively the total optical power dissipated from the cavity (Γ_{tot}) and the one coupled to the passive waveguide ($\Gamma_c/2$ in Figure 77). From the definition of Γ_{tot} and Γ_c we have that:

$$\frac{P_c}{P_{tot}} = \frac{\tau_{tot}}{2\tau_c} = \frac{Q_{tot}}{2Q_c} \tag{3.11}$$

Where P_c is the fraction of power measured in the silicon waveguide's monitor and P_{tot} is the overall optical power inside the simulation. Knowing Q_{tot} from the time monitors, from (3.11) we are able to calculate Q_c and from (3.9) we can extract Q_0. Eventually, we can retrieve the coupling efficiency from (3.10).

3.3.2.2 Simulation results

Let us start to analyze the performances of the hybrid structure by varying the transversal shift between the silicon waveguide and the cavity. The silicon waveguide width has been fixed at 600 nm.

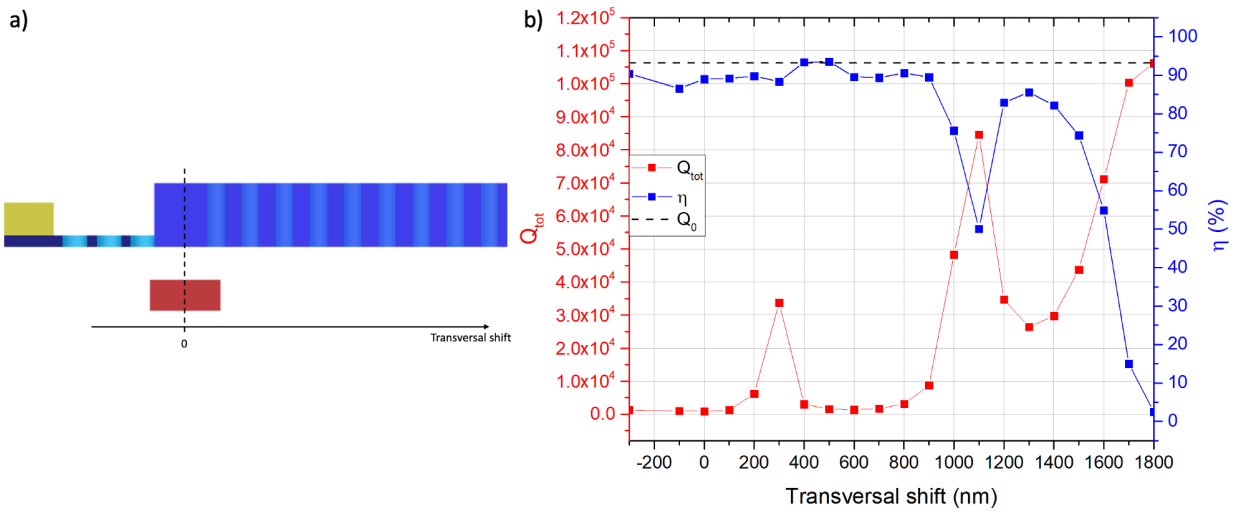


Figure 78: a) cross-section schematics of the simulated hybrid system. b) Q_{tot} (left axis) and coupling efficiency (right axis) variation as a function of the transversal misalignment between silicon waveguide and PhC cavity center; the vertical distance has been fixed to 230 nm and the cavity parameters to $a = 333$ nm, $r = 72$ nm, central wgw $= 0.9 \cdot a\sqrt{3} = 519.1$ nm, $R_{base} = 100$ nm with 3 rows of holes in the base

As we can observe, for shift values less than 300 nm, the total Q-factor is highly reduced compared to the intrinsic simulation, with values around 10^3. Conversely, the coupling efficiency is very high, ranging between 85% and 90%. This behavior suggests us that the system is over-

coupled: when the signal is created in the cavity, it starts to resonate but since it is strongly coupled to the silicon waveguide, a high fraction of it is lost by coupling. In that way, the amount of bias power to attain a sufficient gain inside the cavity to get a laser signal increases (i.e., the laser threshold becomes higher). However, for a shift of 300 nm we can see that Q_{tot} increases to a value close to $4 \cdot 10^4$: the system is less coupled with respect to the previous cases but the coupling efficiency is close to 90%. Increasing the shift, Q_{tot} drops back to few thousands and the system gets over-coupled again. This effect is related to the cavity mode's transversal shape: in fact, working at the gap-guided band's cutoff, the mode's group index is increased with respect to modes on the same band presenting a lower wavevector. Such an increased group index makes that the EM field distribution spreads within the first rows of holes (see Figure 70), as we have already discussed during the slow-light section. Consequently, a shift of 300 nm places the silicon waveguide in between the first two maxima of the EM field along the y-direction, reducing the modes' overlap (i.e., decoupling the system) and consequently increasing the total Q-factor. We can observe a similar effect increasing the shift to 1100 nm, where the system is highly decoupled and Q_{tot} rises to $8.5 \cdot 10^4$, but this time the coupling efficiency drops to 50% (system too decoupled). If we keep increasing the shift, we can notice the appearance of a plateau where Q_{tot} stabilizes to around $3 \cdot 10^4$ with a coupling efficiency around 85%, proving to be a good range respecting the tradeoff of maximizing both Q_{tot} and η. After this plateau, the system is more and more decoupled approaching the intrinsic cavity situation, as we can observe from the reduced coupling efficiency and from the Q-factor tending to the intrinsic value Q_0.

Up to now, the coupling efficiency was calculated for a fixed silicon waveguide's propagation constant. Let us now analyze what happens when we set the transversal shift at an arbitrary value while sweeping the silicon waveguide width. Figure 79 shows the coupling efficiency, Q_{tot}, Q_c and Q_0 dependence as a function of the silicon waveguide width for three reported transversal shifts. We can immediately notice that for a silicon waveguide width of 400 nm the energy transfer is less efficient: in fact, we have seen from equation (3.10) that η depends on the ratio Q_c/Q_0 and from Figure 79-c) we can highlight that Q_c is higher for the 400 nm wide silicon waveguide case, reducing the coupling efficiency. This shows that the propagation constant for such a silicon waveguide width is too small to achieve an efficient coupling. For wider waveguides, then, the coupling efficiency stabilizes at values around 90%, even though Q_c continuously varies for each silicon waveguide case: the simulations show in fact that Q_0, contrarily to what we expect from the coupled mode theory, does not remain constant for all the analyzed cases, but it is modified by the presence of a waveguide coupled to the system (which perturbs the cavity's EM field) [124], leaving the ratio Q_c/Q_0 practically unvaried.

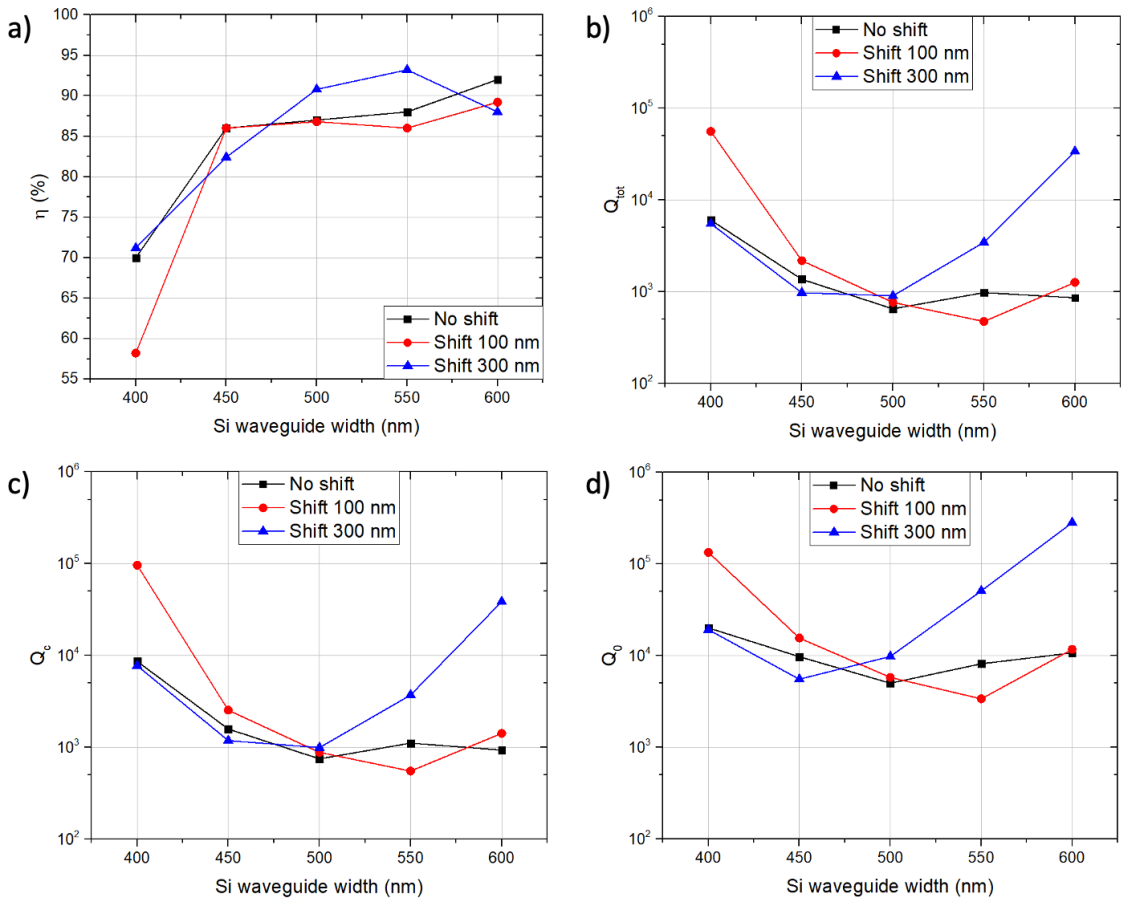


Figure 79: a) coupling efficiency, b) total Q-factor, c) coupling Q-factor and d) intrinsic Q-factor as a function of the silicon waveguide width for different transversal shifts

To conclude, we can state that, due to the small vertical distance between the passive circuitry and the cavity, we deal in general with an over-coupled system. For all the selected silicon waveguide widths, the system's total Q-factor remains low unless we do not apply the proper transversal shift, in order to reduce the overlap between the silicon waveguide and the cavity mode. In that way, we have seen that it is possible to achieve high coupling efficiencies (around 90%) as well as high enough Q-factors (higher than 10^4). Moreover, we have also simulated the cavity coupled to a silicon waveguide presenting a width of 600 nm with a transversal shift of 300 nm between the two by introducing the doped layers as well, and we observed that Q_{tot} got reduced from around $3 \cdot 10^4$ to $1.6 \cdot 10^4$. We considered ourselves satisfied with such a result, since, how we will see later, it allows us to obtain a low laser threshold and high wall-plug efficiency.

We have completely treated the nanolaser cavity design from an optical point of view; it is time now to move to the electrical injection design, to understand how efficiently we can inject electrical carriers inside the apodized cavity in order to complete the device's modeling.

3.4 Electrical behavior

The electrical injection scheme designed for the nanolaser cavity follows exactly the same idea as the nanoamplifier's. It relies on the lateral injection scheme already explained during chapter 2, where the P-contact is placed on the PhC sidewall side and the N-contact on the holes pattern side. Such a design provides a shorter path for holes to diffuse through the P-doped layer and reach the PhC cavity's area with respect to electrons, due to the huge difference in mobility between the two electrical carriers. However, there are some differences:

- the III-V nanolaser membrane is 450 nm thick (the nanoamplifier's one being 350 nm);
- the laser cavity is much shorter, being only around 20 µm long (few hundreds of µm for the amplifier);
- the nanocavity is more resistive than the nanoamplifier, having a reduced carrier injection area and an additional holes pattern drilled in the base.

In order to evaluate the electrical behavior of the nanocavity, we start with a structure with the following PhC geometrical parameters:

- period $\mathrm{a} = 333\ \mathrm{nm}$;
- radius $\mathrm{r} = 72\ \mathrm{nm}$;
- waveguide width $= 0.9 \cdot \mathrm{a}\sqrt{3} = 519.1\ \mathrm{nm}$;
- 3 rows of holes in the base with radius $\mathrm{R_{base}} = 100\ \mathrm{nm}$;
- P-contact distance from the PhC sidewall of 850 nm;
- reduced P- and N-contact length (25 periods, being 8.325 µm) with respect to the whole structure length (being around 20 µm).

Our goal was to completely model such a structure by studying its electrical behavior and extract the relevant properties to calculate the laser threshold and the optical output power. The simulation setup followed the same criteria as the nanoamplifier's one. The MQWs were considered as a single layer to reduce the constraints regarding the simulation spatial resolution. The simulation region was limited to two PhC periods saving simulation time and memory; the full structure's electrical behavior, then, was reconstructed exploiting the same circuital model shown in Figure 51. In the next section, we will analyze the electrical simulation results.

3.4.1 Electrical simulation results

Figure 80 shows the nanolaser's IV curve. The contact resistances were calculated using the same resistivities from the previous chapter ($5.6 \cdot 10^{-5}\ \Omega \cdot \mathrm{cm}^2$ for the P-contact and $3.7 \cdot 10^{-4}\ \Omega \cdot \mathrm{cm}^2$ for the N-contact) and added to the circuital model for a more accurate evaluation ($\mathrm{R_P} = 1.4\ \mathrm{k\Omega}$, $\mathrm{R_N} = 1.3\ \mathrm{k\Omega}$). The resulting diode characteristics shows a turn-on voltage $\mathrm{V_{to}} = 1.1\ \mathrm{V}$ and a series resistance $\mathrm{R_s} = 3.2\ \mathrm{k\Omega}$.

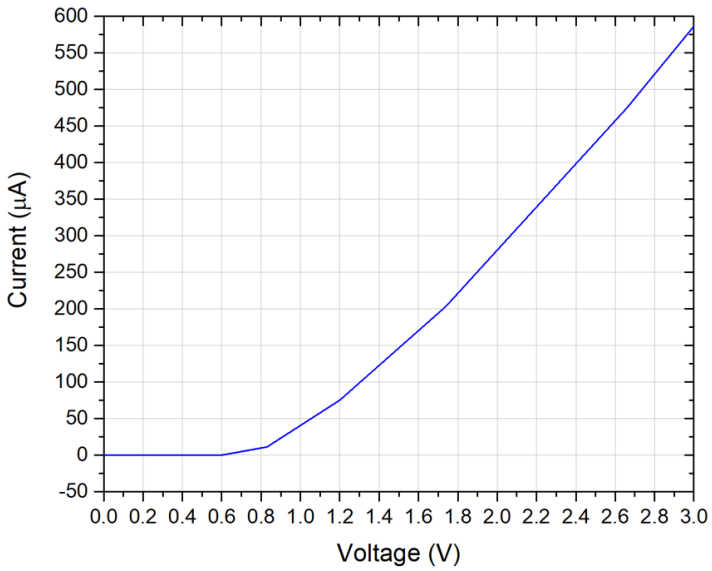


Figure 80: IV curve for the studied nanolaser structure

Thanks to this result, we are able to confirm that, compared to the nanoamplifier, the nanolaser shows a more resistive behavior, which is mainly due to the reduced dimensions of both the diode itself and the electrical contacts. What we are really interested in is how the injected current contributes to radiative recombination: Figure 81 shows the transversal radiative recombination profile for different amounts of injected current.

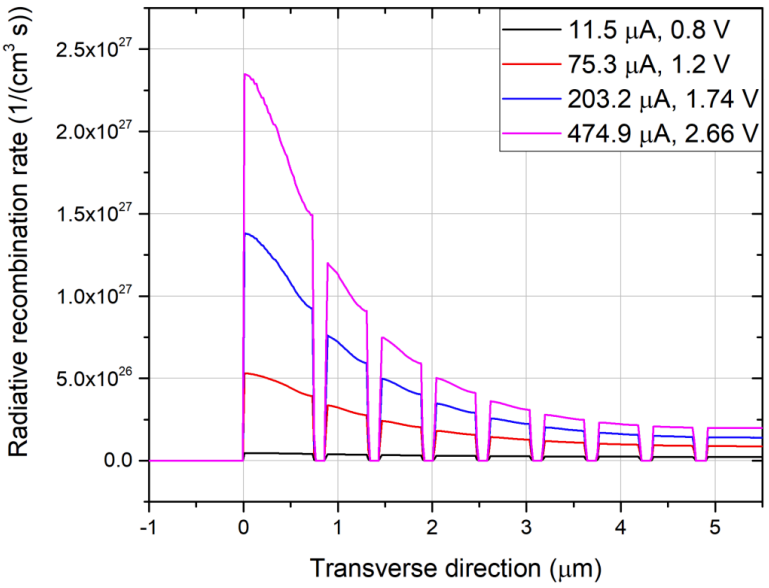


Figure 81: Transversal recombination profile taken at the cavity center for different injected currents (in the legend we report also the corresponding voltages applied across the junction)

The highest part of radiative recombination events occurs inside the PhC cavity (delimited between 0 and 519.1 nm along the transverse direction), with a profile that decreases more and more approaching the N-contact side along the transverse direction. This time, contrarily to the nanoamplifier case, we are also interested in providing enough carriers for radiative recombination not only inside the PhC cavity but also in between the holes of the very first row, due to the characteristic shape of the resonant mode. Figure 82 shows that we properly cover the full field profile with radiative recombination events.

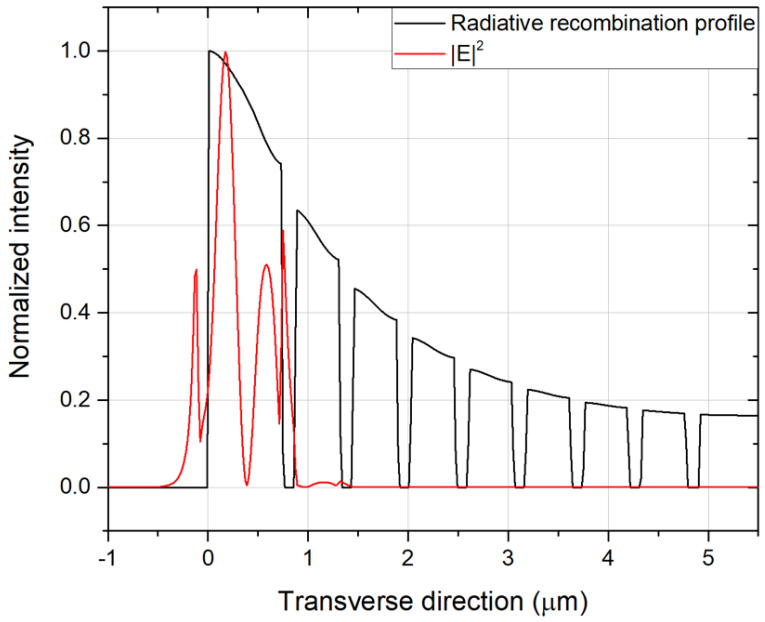


Figure 82: Overlap between radiative recombination profile and squared modulus of the field profile; we can notice the appearance of a second lobe for the field profile, representing the dispersive shape characteristic of a slow-light mode

The simulation result is satisfying also concerning the longitudinal optical recombination profile: in fact, we want to maximize its overlap with the gaussian mode, efficiently providing carriers inside the apodized cavity. We can see that, with this base configuration, the longitudinal overlap is very efficient, as it is confirmed by Figure 83, where the longitudinal radiative recombination profile and the squared modulus of the field profile at the PhC cavity center are plotted.

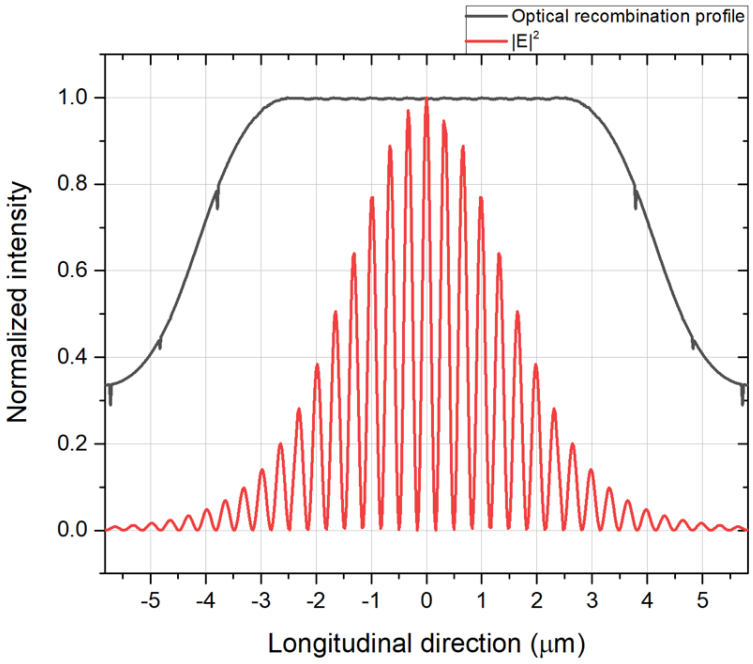


Figure 83: Overlap between longitudinal optical recombination profile and squared modulus of the field profile

We have now all the required ingredients to complete the modeling of our 2D-PhC apodized cavity: in the next section, we will interface the optical simulation results with the electrical ones and we will calculate the laser threshold for such a geometry as well as the achievable signal output power as a function of the injected current.

3.5 Nanolaser cavity model

3.5.1 General rate equations model

Our analysis is based on the exploitation of the rate equations model, whose general expressions can be written as [21]:

$$\frac{dN}{dt} = R_{inj} - R_{NR} - R_{sp} - R_{st} \tag{3.12}$$

$$\frac{ds}{dt} = -\frac{s}{\tau_{tot}} + V_a \beta R_{sp} + V_a R_{st} \tag{3.13}$$

The first one expresses the time evolution of the electrical carrier density N inside the cavity's active region (MQWs): the net amount of electron-hole pairs increases thanks to the injection mechanisms, described by the injection rate inside the cavity R_{inj}, and it decreases due to radiative recombination (spontaneous and stimulated recombination, respectively R_{sp} and R_{st}) and non-radiative recombination events (R_{NR}). The second equation describes, instead, the

photons number (s) time evolution inside the active region for the single cavity mode: they are generated by spontaneous ($V_a\beta R_{sp}$) and stimulated ($V_a R_{st}$) recombination events, resonating inside the cavity for a certain amount of time τ_{tot} (describing the photon lifetime inside the cavity) before being lost ($-\frac{s}{\tau_{tot}}$). β is the spontaneous emission factor, taking into account only the fraction of spontaneous emissions coupled to the resonant mode. V_a is the volume of active material spatially overlapped with the cavity mode and it can be expressed as:

$$V_a = \frac{\sum_{i=1}^{n} \iiint_{V_i} |E(x,y,z)|^2 dzdydx}{\max\left(|E(x,y,z)|^2\right)} \tag{3.14}$$

Where V_i is the volume of every single quantum well and n is the total number of quantum wells.

The injection rate is given by:

$$R_{inj} = \frac{\eta_i I}{qV_a} \tag{3.15}$$

Where I is the injected current, q is the elementary charge and η_i is the injection efficiency, defined as the percentage of injected current contributing to the creation of electron-hole pairs inside the MQWs.

Similarly to what we saw in chapter 2, the spontaneous emission rate is:

$$R_{sp} = F_p B\left(np - n_{i,eff}^2\right) \cong F_p B N^2 \tag{3.16}$$

Where B is the bi-molecular recombination coefficient and F_p is the Purcell factor, taking into account the acceleration of the spontaneous emission rate for the MQWs. Concerning the non-radiative recombination rate, we can approximate it by:

$$R_{NR} = \frac{N}{\tau_{NR}} \tag{3.17}$$

Where τ_{NR} is the non-radiative carriers lifetime. Eventually, the stimulated recombination rate writes as follows:

$$R_{st} = G(N)s \tag{3.18}$$

With $G(N)$ an expression of the net material gain depending on the electron-hole pairs concentration inside the active region. Since we are dealing with a MQWs heterostructure, the material gain expression can be approximated as [21]:

$$G(N) = G_0 \ln\left(\frac{N+N_s}{N_{tr}+N_s}\right),\ G_0 = \frac{\beta F_p B}{A'} \tag{3.19}$$

Where N_s represents a shift to force the natural logarithm to be finite also at N=0 and N_{tr} is the transparency carrier density. A' is a material related parameter, independent from the optical mode inside the cavity.

We are now able to rewrite the rate equations as follows:

$$\frac{dN}{dt} = \frac{\eta_i I}{qV_a} - \frac{N}{\tau_{NR}} - F_p B N^2 - \frac{\beta F_p B}{A'} \ln\left(\frac{N + N_s}{N_{tr} + N_s}\right) s \tag{3.20}$$

$$\frac{ds}{dt} = -\frac{s}{\tau_{tot}} + V_a \beta F_p B \left(N^2 + \frac{1}{A'} \ln\left(\frac{N + N_s}{N_{tr} + N_s}\right) s\right) \tag{3.21}$$

These equations refer to a model where the carrier density is constant in every part of the active volume; however, as previously observed, it is not the case in our nanolaser. In order to write these equations for our system, we have to redefine the terms related to spontaneous and stimulated recombination and define an "effective cavity" system where the carriers concentration is a constant value depending only on the applied bias.

3.5.2 Effective cavity rate equations model

Let us first consider the spontaneous recombination term: we know that this emission mechanism depends on the electrical carriers injection scheme. We can evaluate the carrier density profiles along the whole cavity and extract an average spontaneous emission term related to the MQWs volume, as follows:

$$\langle R_{sp} \rangle = \frac{\sum_{i=1}^{n} \iiint_{V_i} R_{sp} dz dy dx}{\sum_{i=1}^{n} \iiint_{V_i} dz dy dx} = F_p B \frac{\sum_{i=1}^{n} \iiint_{V_i} N^2 dz dy dx}{\sum_{i=1}^{n} \iiint_{V_i} dz dy dx} \tag{3.22}$$

The same reasoning is applied to the non-radiative recombination factor, where we extrapolate an average value for N. For what concerns the stimulated recombination term, it is dependent on the spatial overlap between the carriers density and the EM field intensity profiles. Consequently, if we want to reduce the problem to an "effective cavity", considering an effective modal gain, we need to weight the stimulated emission term analyzing the overlap between the material gain and the optical field profile all over the cavity:

$$\langle R_{st} \rangle = \langle G(N) \rangle s = \frac{\sum_{i=1}^{n} \iiint_{V_i} E^*(x,y,z) G(N) E(x,y,z) dz dy dx}{\sum_{i=1}^{n} \iiint_{V_i} |E(x,y,z)|^2 dz dy dx} s \tag{3.23}$$

The final form of the rate equations, then, takes into account these updated terms for $\langle R_{st} \rangle$, $\langle R_{sp} \rangle$ and $\langle R_{NR} \rangle$:

$$\frac{dN}{dt} = \frac{\eta_i I}{qV_a} - \frac{\langle N \rangle}{\tau_{NR}} - F_p B \langle N^2 \rangle - \langle G(N) \rangle s \tag{3.24}$$

$$\frac{ds}{dt} = -\frac{s}{\tau_{tot}} + V_a \left(\beta F_p B \langle N^2 \rangle + \langle G(N) \rangle s \right) \tag{3.25}$$

These equations describe the nanolaser behavior for whatever injected current and can be solved in a parametric form. However, for an easier analysis, we split the cavity behavior describing it below- and above-threshold, in order to calculate the laser characteristics showing the available output power as a function of the injected current.

Below-threshold we can neglect the stimulated emission term, as it is very small. If we observe then the steady-state solution for s, we have:

$$\frac{s}{\tau_{tot}} = V_a \beta F_p B \langle N^2 \rangle \tag{3.26}$$

$$s = \tau_{tot} V_a \beta F_p B \langle N^2 \rangle \tag{3.27}$$

Where $\langle N^2 \rangle$ is calculated from the simulation results, as a function of the injected current.

On the other hand, above-threshold we can neglect the spontaneous emission term, rewriting the rate equations as:

$$\frac{dN}{dt} = \frac{\eta_i (I - I_{th})}{qV_a} - \frac{\langle N \rangle}{\tau_{NR}} - \langle G(N) \rangle s \tag{3.28}$$

$$\frac{ds}{dt} = -\frac{s}{\tau_{tot}} + V_a \langle G(N) \rangle s \tag{3.29}$$

If we want to solve the steady-state solution of such equations we must take into account that, above threshold, the carriers density and the modal gain clamp at their threshold value:

$$N(I > I_{th}) = N_{th} \tag{3.30}$$

$$G(I > I_{th}) = G_{th} \tag{3.31}$$

Focusing on (3.29), we can observe that the above-threshold steady-state solution gives us the possibility to extract the threshold value for the gain:

$$s \left(\frac{1}{\tau_{tot}} - V_a G_{th} \right) = 0 \tag{3.32}$$

$$G_{th} = \frac{1}{\tau_{tot} V_a} \tag{3.33}$$

From the simulation results, then, we are able to calculate the effective modal gain as a function of the injected current: in that way, knowing G_{th}, we are able to deduce I_{th}, building an above-threshold steady-state equation for the photons number inside the cavity:

$$s = \frac{\eta_i (I - I_{th})}{G_{th} q V_a} - \frac{N_{th}}{G_{th} \tau_{NR}} \tag{3.34}$$

3.5.3 Nanolaser performances

The following table resumes the associated coefficients to the constant parameters. η_i was approximated to 1 for simplicity, considering our system as an ideal one. B and N_{tr} were set as for the nanoamplifier case, while β, F_p and A' were chosen from [94]. N_s, instead, was extracted from [96] while the active volume was calculated from the field shape resulting from FDTD simulations. Eventually, the total Q-factor was set to 10^4 following the discussion made at the end of the optical simulation section, in order to model the full system as realistically as possible.

Constant	Coefficient
$\boldsymbol{\eta_i}$	1
B	$3 \cdot 10^{-10}\ cm^3/s$
$\boldsymbol{\beta}$	0.1
$\boldsymbol{F_p}$	2.3
$\boldsymbol{A'}$	$5 \cdot 10^{-36}\ cm^6$
$\boldsymbol{N_{tr}}$	$1 \cdot 10^{18}\ cm^{-3}$
$\boldsymbol{N_s}$	$0.92 \cdot \boldsymbol{N_{tr}}$
$\boldsymbol{V_a}$	$4.06 \cdot 10^{-14}\ cm^3$
$\boldsymbol{Q_{tot}}$	10000

Once all these parameters set and recalling that $\tau_{tot} = {}^{2Q_{tot}}/_{\omega_0}$, we are able to calculate the threshold value for the modal gain:

$$G_{th} = \frac{1}{\tau_{tot} V_a} = 1.46 \cdot 10^{24}\ \mathrm{cm^{-3}/s} \tag{3.35}$$

From the obtained simulation results, we are able to plot the effective modal gain evolution as a function of the injected current (Figure 84). We can clearly see the transition from negative values (loss regime) to positive ones (gain regime), considering that when $\langle G(N) \rangle = 0$ we are in the transparency region ($N = N_{tr}$).

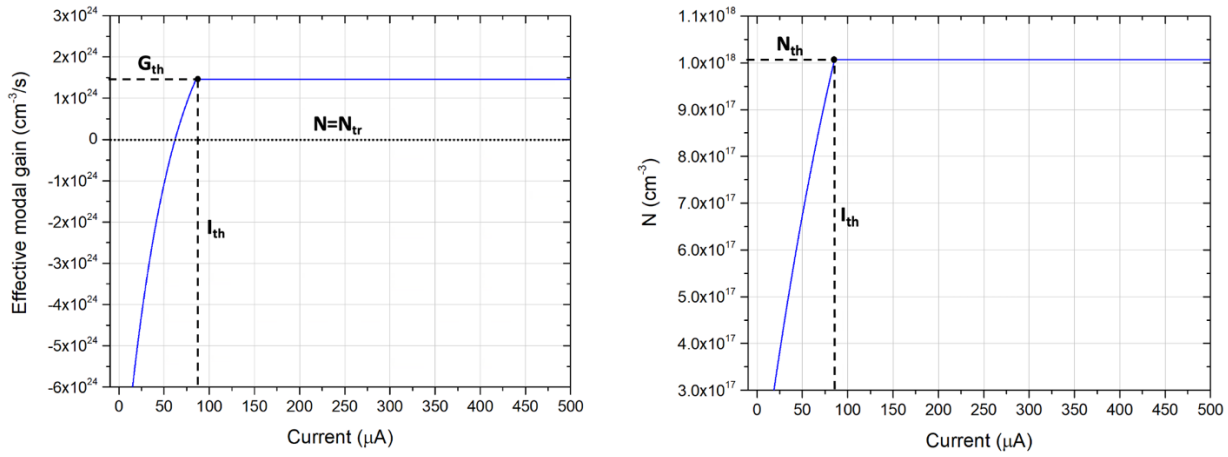


Figure 84: Effective modal gain (left) and carriers density (right) as a function of the injected current; we can observe that when they reach the threshold value they pin to it, remaining constant even for higher injected currents

From these graphs we can extract the threshold current $I_{th} = 85.5\ \mu A$. In that way, we have all the parameters we need to build-up a full nanolaser model, calculating the emitted photons with the sub- and above-threshold approximations.

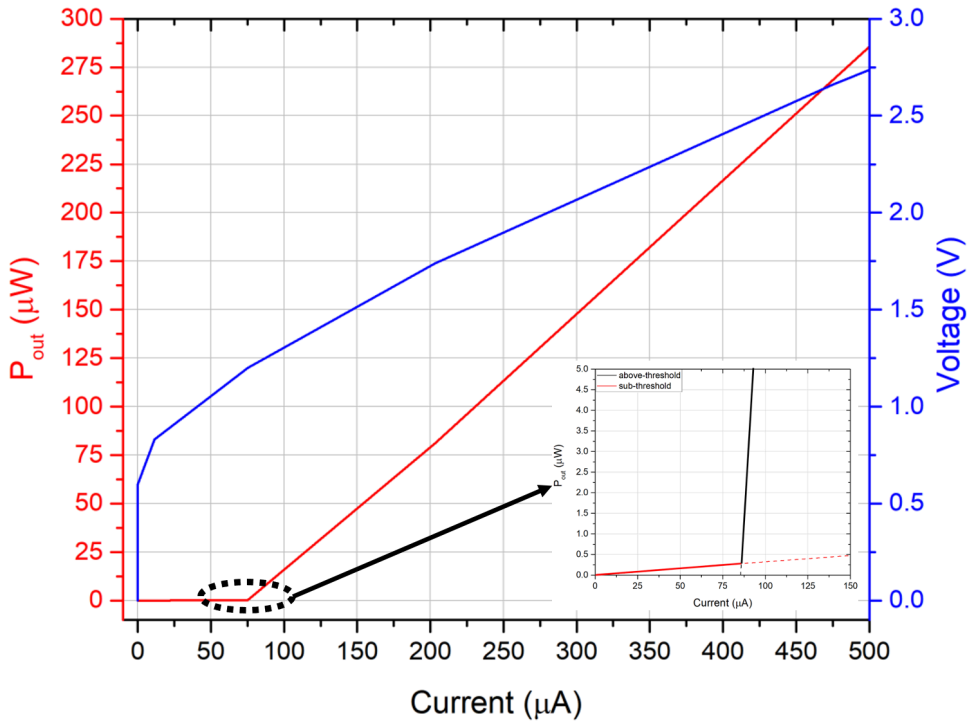


Figure 85: P-I characteristics for the modeled nanolaser; in the inset, a close-up view around the laser threshold, where the two regimes describing the structure's behavior intercept

Figure 85 shows the obtained laser characteristics, taking also into account the coupling efficiency between the nanolaser cavity and the 600 nm wide silicon waveguide shifted by 300 nm with respect to the cavity center ($\eta = 88\%$). The corresponding I-V characteristics is reported as well. The emission curve in sub-threshold shows values of the order of tens or hundreds of nW. It is remarkable that, with just few hundreds of μW of bias power we are able to excite and extract a laser signal carrying a power on the order of a hundred of μW: this is possible thanks to the ultra-small active volume achievable with PhCs and the efficient lateral injection scheme we engineered during this PhD. Such a result is confirmed by the nanolaser's wall-plug efficiency (Figure 86), defined as:

$$\eta_{wp} = \frac{P_{out}}{P_{in}} \tag{3.36}$$

And expressing the device's energy conversion efficiency from bias electrical power (P_{in}) to output optical one (P_{out}).

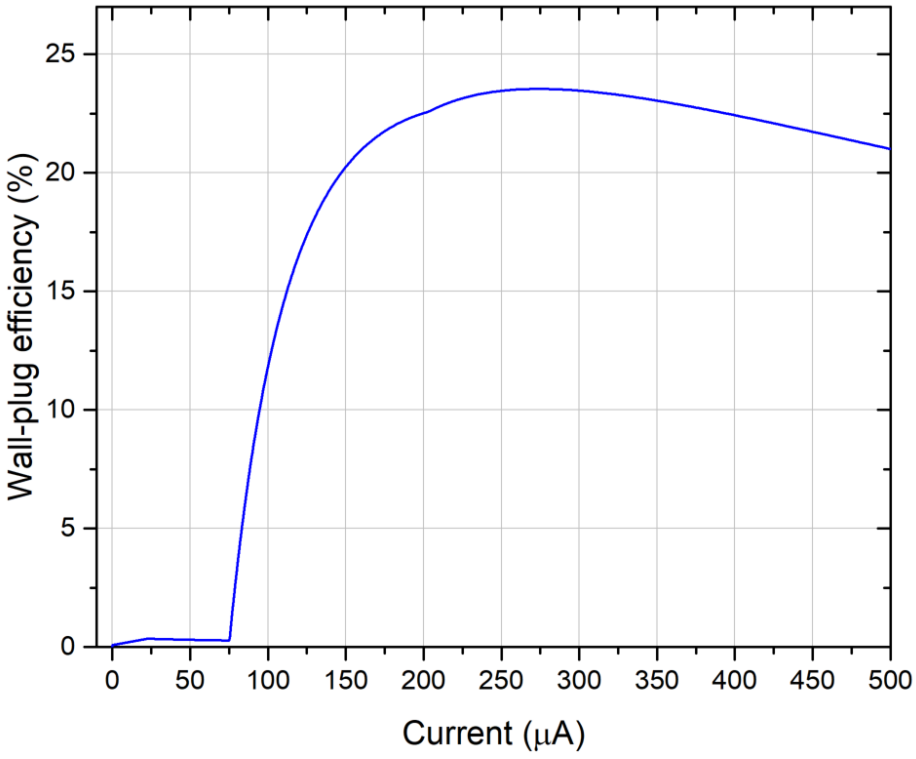


Figure 86: Wall-plug efficiency of the designed nanolaser

As we can observe, the peak η_{wp} is around 23% for an injected current of 250 μA. This result is really promising since it can potentially improve the record wall-plug efficiency showed in [59].

Another important parameter used to define the device's energy efficiency above the laser threshold is the slope efficiency (or differential power efficiency), defined as the above-threshold slope of the laser characteristics:

$$\eta_d = \left.\frac{dP_{out}}{dP_{in}}\right|_{P_{in}>P_{th}} \tag{3.37}$$

The calculated η_d is of 32%, which is in good agreement with the one from [59].

Figure 87 represents another important characteristics we calculated to fully model the designed nanolaser: it shows the laser threshold current variation as a function of the total Q-factor.

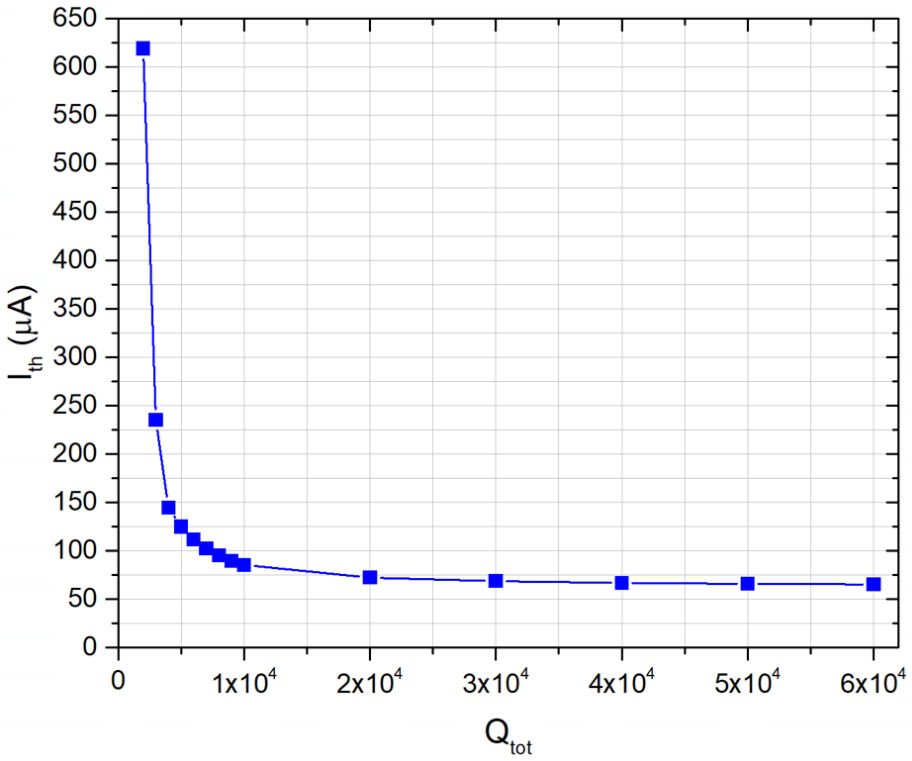


Figure 87: Laser threshold current variation as a function of the cavity's Q-factor

It is interesting to notice that, while for Q-factors of few thousands I_{th} presents a steep variation, when Q_{tot} increases above $5 \cdot 10^3$ the laser threshold current is less and less reduced until it almost stalls for $Q_{tot} > 10^4$: the current difference between $Q_{tot} = 6 \cdot 10^4$ and $Q_{tot} = 10^4$ is just 20 μA (85.5 μA versus 65.5 μA). This is a very interesting result, since it tells us that it is sufficient to have a Q_{tot} of the order of 10^4 in order to achieve ultra-low laser threshold current: considering, in fact, that to increase the Q-factor we have to increase R_{base}, that would turn,

from an electrical point of view, to a reduction of the available material for positive-charge carriers to diffuse through to the PhC cavity's active region, increasing the base's resistance and, consequently, the needed bias power to attain the lasing behavior. However, thanks to the result depicted in Figure 87, we know that a R_{base} corresponding to a Q_{tot} on the order of few 10^4 is enough to have a laser threshold current below $100\,\mu A$. As we will see during the characterization chapter, we could demonstrate that a radius of 70 nm for the holes drilled in the base is enough to achieve these performances.

3.6 Conclusion

During this chapter, we focused our attention on the design of our 2D-PhC structure as a single mode nanolaser cavity. The mode's confinement is achieved through the *gentle confinement* principle, minimizing the out-of-plane losses: in order to do that, we built the structure by means of a Gaussian apodization algorithm, playing on the PhC cavity width. Similarly to the nanoamplifier, the geometrical asymmetry caused the appearance of a non-zero electric field's vertical component, which was limiting the attainable Q-factor. In order to minimize this effect, we inserted an additional pattern of holes inside the PhC base: in that way, we could achieve a Q-factor of the order of 10^5 for a cavity presenting dimension of 20 µm in length.

We have studied, then, the evanescent wave coupling of the designed nanocavity with a silicon waveguide placed at a fixed vertical distance: in order to achieve an efficient signal transfer while maintaining a total Q-factor of at least 10^4 a tradeoff has to be faced choosing the silicon waveguide width and the lateral shift between cavity and passive waveguide.

While on one hand the structure's asymmetry was causing the resonant modes to be quasi-TE (instead of fully-TE), on the other hand it allowed to efficiently inject electrical carriers inside the cavity's active region. In the last section we have also built a cavity model to evaluate the interaction between the injected electrical carriers and the electromagnetic field: we have seen that, when the designed nanocavity presents a total Q-factor around 10^4, it is possible to achieve a laser threshold current below 100 µA. Moreover, we reported also the nanolaser's wall-plug efficiency and slope efficiency, being respectively of 23% at 250 µA of injected current and 32%, proving that our structure is a valid candidate for ultra-small and ultra-low power integrated system applications.

In the next chapter, we will focus our attention on the technological process flow to fabricate both the structures we treated so far.

Chapter 4: Fabrication

In the previous chapters, we have seen how to design the asymmetric 2D-PhC structure respectively as a nanoamplifier and a nanolaser source. We will now go through the required technological steps to fabricate these structures, showing all the challenges we had to face to achieve a full hybrid device. Even though the two devices needed slightly different membrane thickness, the general fabrication process flow was identical: during this chapter, every fabrication step will generally refer to both implemented devices.

The calibration of a full process flow to conceive the studied 2D-PhC optoelectronics structures represented the most difficult and most time consuming task of the PhD. We will show the amount of required fabrication steps to get through and how they are correlated to each other: a slight modification of a single technological process required the recalibration of many subsequent steps. Additionally, during this PhD project, we had to face the moving of C2N, which forced us to recalibrate every single step starting from scratch, adapting them to the new clean room environment. Even though all this nanofabrication work represented a huge challenge, it will remain, from a personal point of view, the most exciting and stimulating part I have been involved, since it gave me the possibility to gain a lot of experience in the technical environment that is a clean room. Additionally, our technological work represents a major success of this PhD project, since the calibrated process flow allowed us to fabricate high quality nanostructures with a great reproducibility. During the rest of this chapter, we will describe the developed technology, relating it to the modeled structures and commenting on each step, showing, among other things, that the adopted temperatures are compatible with the CMOS back-end-of-line. Particularly, we will describe:

a) the adopted passive and active platforms and their interfacing through adhesive bonding, also commenting on the exploited dielectric inter-layers;
b) the III-V material processing to fabricate the asymmetric 2D-PhC structure, which was divided in two steps (the first step defining the devices perimeter and the holes pattern, while the second one defining the PhC base and the PhC sidewall);
c) the P- and N-contact metallization and their activation through Rapid Thermal Annealing;
d) the PhC and holes' sidewalls passivation to remove surface dangling bonds and the subsequent structures encapsulation, to protect the devices as well as the passivated surfaces while guaranteeing an efficient heat evacuation;
e) the vias opening and the final top-pads metallization, to provide an electrical contact for the electrical probes during characterization.

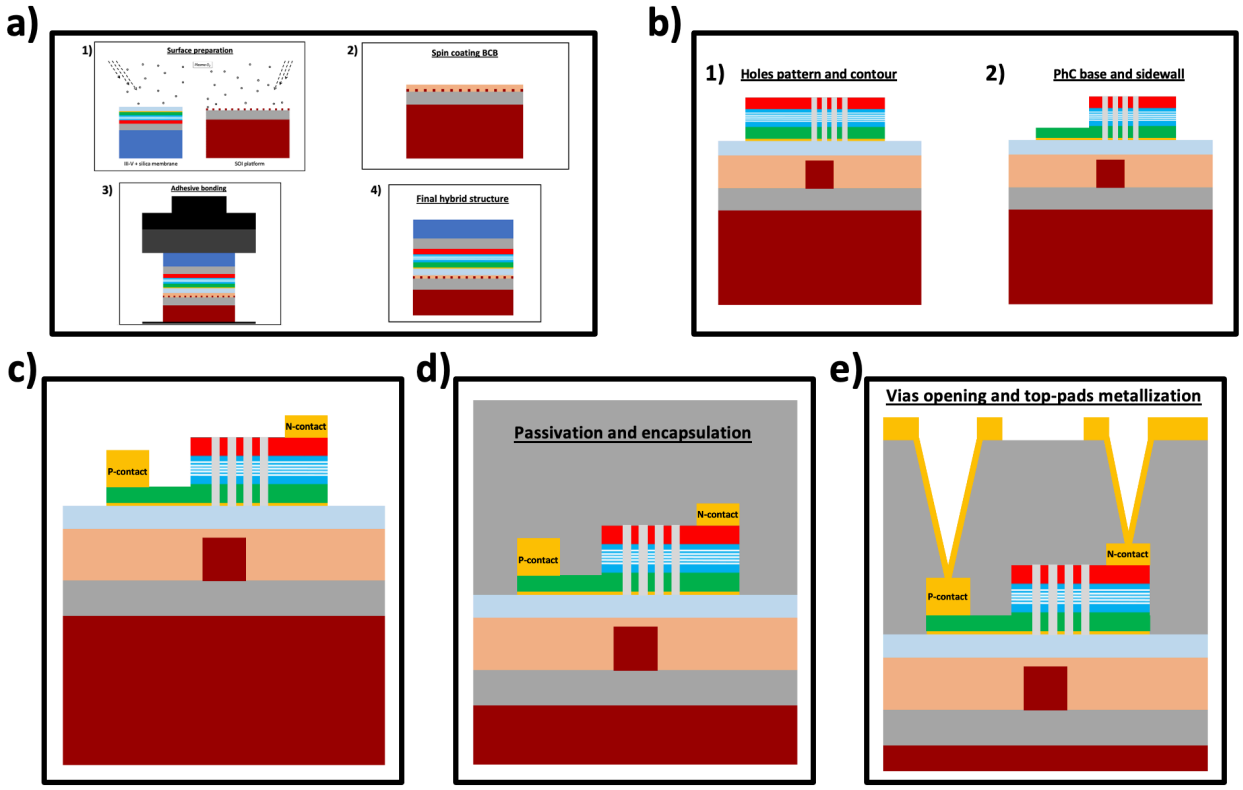


Figure 88: Schematics of the fabrication process flow

4.1 Full structure description: active and passive levels

As already mentioned during the modeling chapters, our full hybrid devices are composed of two main components: a passive level, in charge of interfacing from an optical point of view the chip with the outer world (injecting/extracting the input/output signal) and an active one, creating and/or amplifying the optical signal. These two levels are, respectively, a Silicon On Insulator (SOI) chip, containing silicon waveguides for the bus circuitry, and an Indium Phosphide (InP) based membrane, containing the gain media for light processing. In the next two sections, we will briefly describe the two adopted platforms.

4.1.1 SOI

For the passive circuitry we employed a SOI substrate, taking advantage of the reduced losses such a platform presents with respect to a standard Silicon substrate. The SOI wafer is composed by a silicon substrate with a silica layer (2 µm thick) called Buried Oxide (BOX) and a thin silicon layer (220 nm thick) on top of it. The silicon layer is then etched to create the ridge silicon waveguides pattern, while the thick silica layer prevents the coupling between the waveguides and the silicon substrate. The high refractive index difference between silicon ($n_{Si} = 3.46$) and

silica ($n_{SiO_2} = 1.45$) allows to confine the propagating optical mode in extremely compact ridge waveguides: that is why for our SOI we chose to put silicon waveguides with widths ranging from 400 nm to 600 nm. As we can see from Figure 89, we have two types of waveguides: a group of straight silicon waveguides, where the idea is to exploit them to extract the signal from the nanolasers, and a group of silicon waveguides with trenches of different length, in order to integrate the nanoamplifiers.

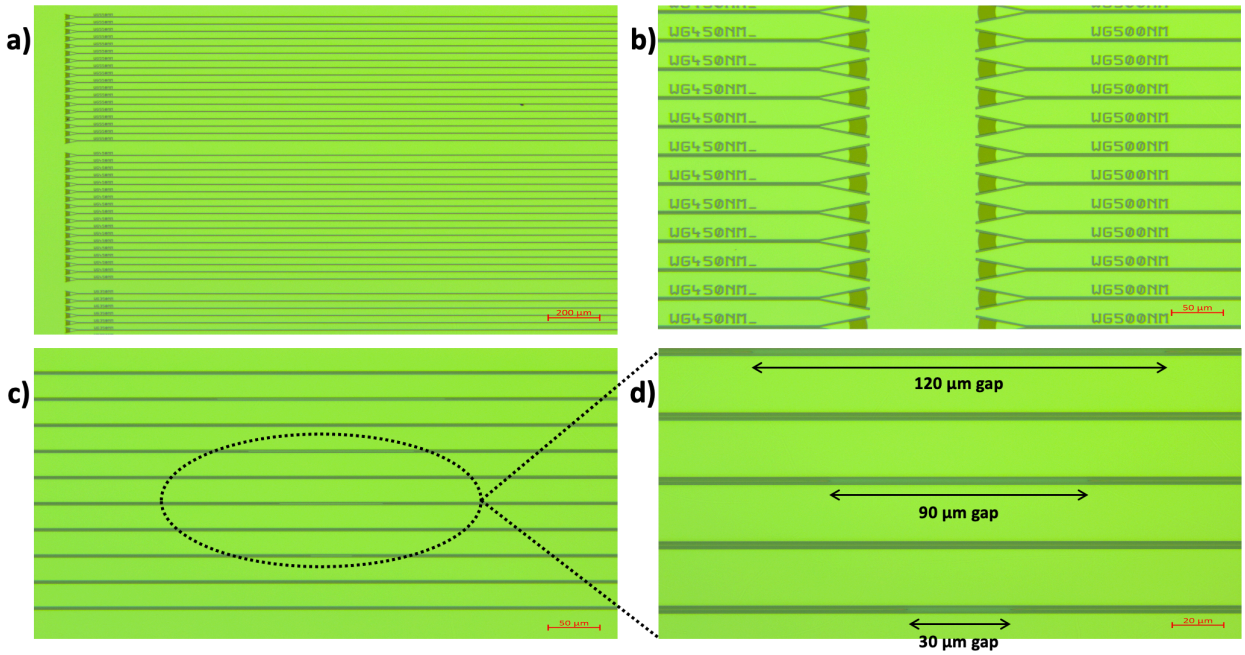


Figure 89: a) straight waveguides used for the nanolasers, b) grating couplers exploited to inject/extract a light signal in/from the chip, c) waveguides with trenches of different lengths where to fabricate the nanoamplifiers and d) close-up view of c)

On the top and bottom of the SOI chip two sets of etched global markers with dimension of 10 µm x 10 µm were integrated: their utility comes into play when we want to perform some lithographic step in order to precisely align our structures with the passive circuitry. In order to inject/extract a signal in/from the chip, at the extremities of each silicon waveguide we can find grating couplers [97]: thanks to these structures we were able, with our setup, to inject and extract a signal into/from the SOI chip with cleaved single mode optical fibers with insertion losses of about 4 to 6 dB.

Such a passive platform was not produced in our clean room facility but was ordered from the Cornestone foundry, based at the University of Southampton, UK. It was fabricated on a 8" wafer, where the same pattern was reproduced multiple times. The wafer was appropriately diced to exploit each reproduction for our technological purposes, each die having dimensions of 1.5 cm

x 1.2 cm. Cornestone was buying the SOI material from the Soitec company to successively process them. The fabrication of such a platform relies on the Smart Cut technology, developed during the 90s at the CEA-LETI laboratory [98-99]. The idea is to firstly oxidize a silicon wafer, creating the thermal BOX layer, and then to implant hydrogen ions, travelling through the thick BOX and reaching the beginning of the silicon wafer, weakening the lattice bonds between silicon atoms. Such a wafer is then bonded to another silicon wafer (on the BOX side). Then the Smart Cut technique takes place, where a high temperature process ($1000℃$) splits the silicon wafer along the weaker atomic bonds zone. Eventually, a Chemical Mechanical Polishing (CMP) technique is performed to thin-down the silicon layer to 220 nm with a smooth surface. Once the platform is created, the silicon waveguides pattering is performed through deep-UV lithography followed by plasma etching.

4.1.2 III-V

The composition of the adopted III-V membranes has always been the same during this PhD: we worked with InP-based heterostructures, exploiting the direct band-gap of such materials to create devices working at telecom wavelengths. The main parameters of the membrane we worked with are the ones listed in the nanolaser chapter: it is a 450 nm thick membrane, embedding a MQWs heterostructure as a gain material made of 5 $In_{0.84}Ga_{0.16}As_{0.16}P_{0.84}$ QWs alternated with $In_{0.84}Ga_{0.16}As_{0.48}P_{0.5}$ barriers, while P-doped and N-doped layers are respectively made of $In_{0.84}Ga_{0.16}As_{0.48}P_{0.52}$ and InP. The adopted dopants are Zinc for the P-doped layer and Silicon for the N-doped one, both carrying a doping concentration of $2 \cdot 10^{18}\ \mathrm{cm}^{-3}$. InGaAsP has been chosen for the P-layer instead of InP for its lower electronic band gap (1 eV for InGaAsP while 1.35 eV for InP), for the easier constitution of an ohmic contact between P-metal and P-doped layer. As already explained during the nanoamplifier's electrical design, we asked for 10 nm of InP underneath the P-layer in order to prevent non-radiative surface recombination events at the bottom-surface of the membrane, exploiting the higher InP electronic band gap as a barrier for the electrical carriers. On top of the N-doped layer we have 300 nm of InGaAs exploited as an etch-stop layer followed by the InP substrate (around 300 μm thick). The etch stop layer is fundamental to protect our 450 nm membrane when we perform the substrate removal by wet etching, as we will see later. Figure 90 shows a schematics of the described membrane. The adopted III-V membranes were grown at C2N (Palaiseau, France) using Metal-Organic Chemical Vapor Deposition (MOCVD). Two types of heterostructures were produced: 450 nm and 350 nm thick diodes, exploited to fabricate respectively the nanolasers and the nanoamplifiers.

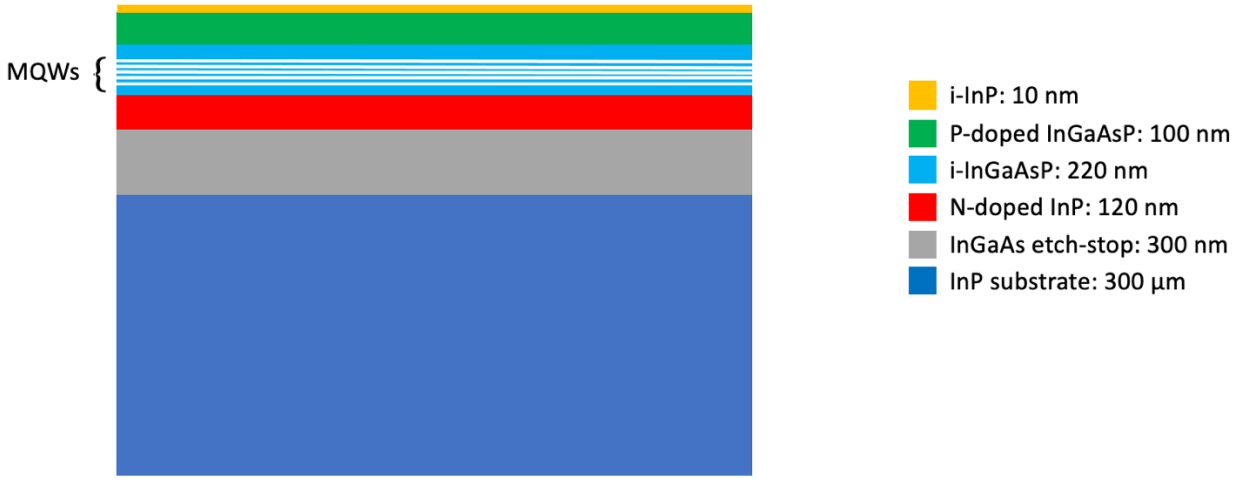


Figure 90: Schematics of the adopted InP-based membrane

4.1.3 Inter-layers dielectrics

For the correct interfacing of the passive and active levels while respecting the vertical distance determined during design (230 nm), good care had to be taken selecting the inter-layer materials, which need to possess the following properties:

1) low refractive index, for the optimal mode's confinement inside the 2D-PhC in the out-of-plane direction by TIR;
2) be transparent at telecom wavelengths to avoid signal absorption;
3) high thermal conductivity, for an efficient heat sinking.

Additionally, we also had to select the proper material to bond the two platforms together. For this, we took advantage of a polymer called Benzocyclobutene (BCB): in fact, not only it possesses excellent thermosetting and planarization properties [100], proving to be a great bonding polymer, but it also satisfies 1) ($n_{BCB} = 1.54$) and 2). On the other hand, BCB is a bad thermal conductor with a poor adhesion on InP, resulting in failing bonding processes. In order to fulfill 3) and to guarantee a successful bonding, then, 2 types of inter-layer dielectrics configurations can be adopted:

- BCB/SiO_2, since silica has a low refractive index ($n_{SiO_2} = 1.45$), transparency at telecom wavelengths and higher thermal conductivity than BCB, with improved adhesion compared to InP;
- BCB/SiO_2/MgF_2, since Magnesium Fluoride respects 1) ($n_{MgF_2} = 1.38$), 2) and 3), with a thermal conductivity 10 times larger than that of silica. Additionally, MgF_2 shows perfect

chemical inertia to Hydrofluoric acid (HF), rendering it a very useful material for the following technological steps.

During the next sections, we will analyze both configurations, commenting on their advantages and drawbacks. Let us now focus our attention on the first fabrication step, which is the bonding of the SOI substrate with the III-V membrane.

4.2 Adhesive bonding

In order to create the hybrid device, we needed to engineer a process capable of sticking together the passive and active platforms. For that, we took advantage of the so-called adhesive bonding, which is a thermo-compressive process that, through the exploitation of an appropriate polymer, glues together the desired platforms. In the next section we will describe and comment this step.

4.2.1 Technological procedure

The adhesive bonding is a technique consisting in bonding two wafers (or, like in our case, two dies) together by means of an adhesion polymer and the application of a compressive force at high temperature: the idea is to heat up the system going beyond the polymer's glass transition temperature, so that it can pass from viscous state to a more rigid one, while adhering to the surfaces placed above and below. In order to perform an efficient bonding, many degrees of liberty have to be taken into account:

- the kind of adopted polymer and its dilution;
- the surfaces on which the polymer has to adhere;
- the environmental temperature and humidity, dramatic for the surfaces preparation;
- the pressure and the temperature to exploit for the process.

As already anticipated in the previous subsection, for the choice of the polymer we relied on BCB, commercialized from Dow Chemicals under the name Cyclotene 3022-35. However, we could not work just with out-of-the-bottle BCB: in fact, spin coating the polymer alone would result in a thick layer (around 1 µm) compared to the targeted vertical distance (230 nm). The BCB was then diluted with its solvent, mesitylene, in order to achieve a smaller BCB thickness after spin coating. Moreover, as discussed in the previous subsection, the introduction of inter-layer dielectrics is necessary to counteract the poor BCB adhesion on InP and to improve the thermal dissipation. Firstly, an MgF_2 layer is deposited on the III-V surface through thermal evaporation by Ion Beam Assisted Deposition (IBAD); then, an intermediate silica layer deposited by sputtering or Atomic Layer Deposition (ALD) must be added in order to make BCB adhere on the III-V side. On the SOI side, instead, the BCB adhesion is achieved thanks to the exposition of the substrate under an accelerated oxygen plasma, cleaning the surface from any remained leftover and also creating a

thin layer of silica on the SOI surface, rendering it hydrophilic and consequently improving the polymer's adhesion.

Another very important variable is the clean room environmental condition: unfortunately, humidity represented a major problem while using our clean room facility. This caused many times the treated surfaces transition from hydrophilic to hydrophobic, making the BCB adhesion impossible neither on the SOI nor on the silica on the III-V side. That is why we needed to add-up an additional step to the bonding process, leaving both SOI and III-V inside an oven at 300°C to completely evacuate the traces of water from the silica layers, proceeding then to the oxygen plasma process to treat the surfaces for the successive BCB adhesion.

Once completed the surfaces treatment, we could perform the BCB spin coating on the SOI, where we calibrated a dilution and a rotation speed allowing us to maintain a thin and planar BCB layer. After spin coating, the SOI undergoes a soft baking step to evacuate the excess solvent. Eventually the adhesive bonding process can be performed, which we did exploiting the bonding machine SB6e from SUSS MicroTec: the two platforms are placed on top of the other (III-V on SOI) and are inserted inside the machine's main chamber under a moderate vacuum.

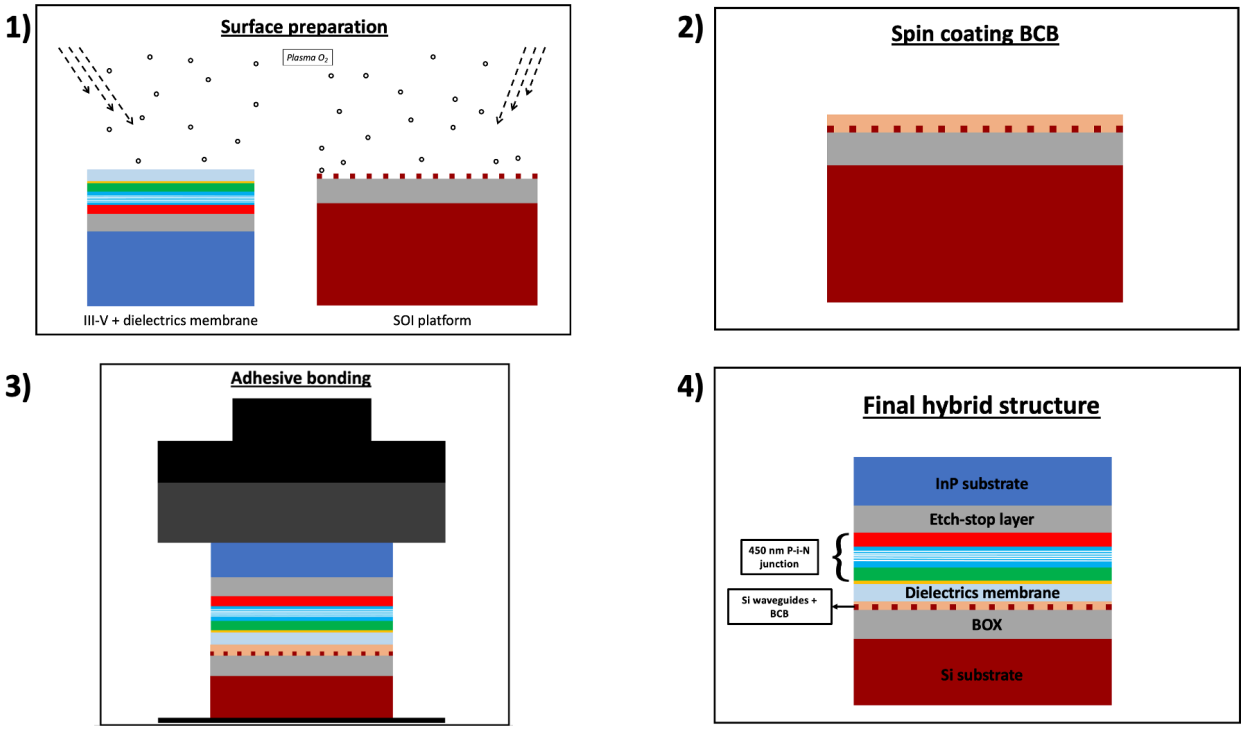


Figure 91: Schematics resuming the whole steps for the adhesive bonding process. 1) surface preparation with a plasma O_2 cleaning the two wafers surfaces, rendering them hydrophilic, 2) spin coating of the diluted BCB on the SOI wafer, 3) thermo-compressive bonding performed under vacuum and 4) final bonded structure

The calibrated recipe consists in slowly increasing the temperature to 170°C, in order to liquefy the polymer, then take down a piston to apply a pressure on top of the created sandwich (completely planarizing the BCB and evacuating any possible air bubble formed inside it thanks to the under-vacuum atmosphere) and keep increasing the temperature to 320°C, where the uniform BCB strengthens and sticks to both surfaces, gluing them together. Figure 91 shows a schematics resuming all the steps involved in the calibrated adhesive bonding process.

4.2.1.1 BCB thickness

As explained in the previous sections, BCB is a great polymer for adhesive bonding, being also transparent at telecom wavelengths, but it presents very tricky adhesion properties depending on the exploited surfaces and a poor thermal conduction, limiting heat dissipation around the 2D-PhC. Thus, we chose to minimize the BCB thickness, ensuring bonding while controlling the coupling distance by arbitrarily choosing the inter-layer dielectrics thickness. In our developed process, after bonding, an ultra-thin layer of BCB (30 to 50 nm) remains between the top of the SOI waveguide and the dielectrics deposited on top of the III-V (Figure 92).

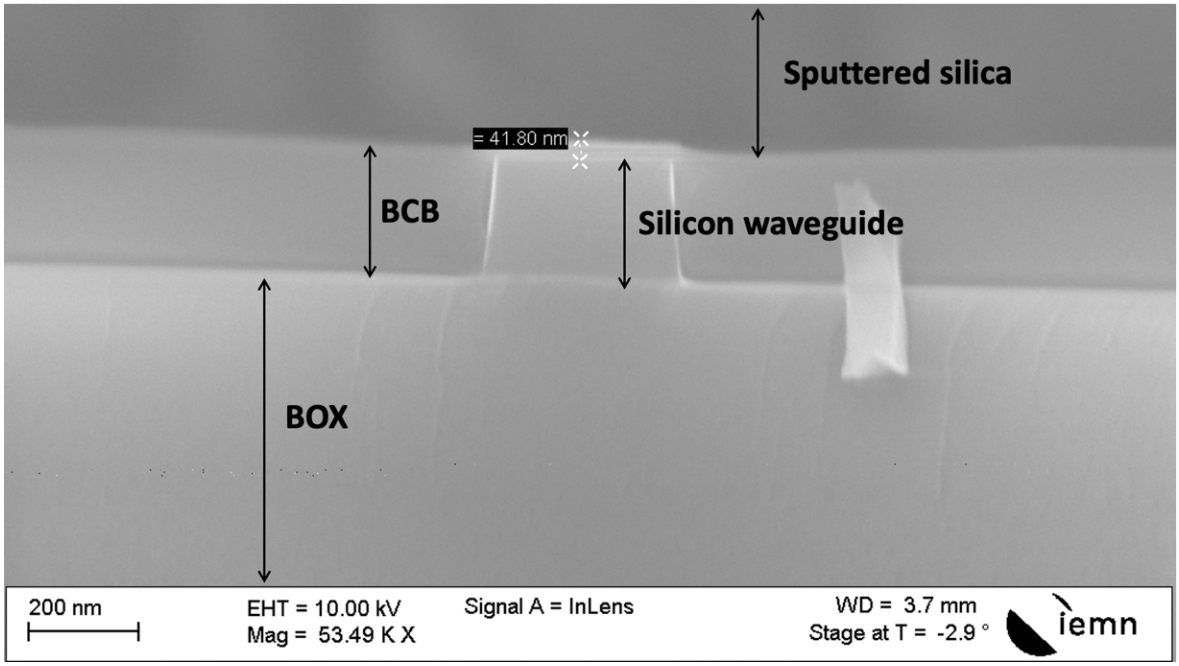


Figure 92: Cross-cut of a test sample to evaluate the BCB thickness. As we can observe, on top of the silicon waveguide we have a very thin BCB layer with thickness of around 40 nm

Considering the BCB thickness to be 50 nm, 180 nm of dielectric material have to be deposited on the III-V surface prior to bonding in order to have the desired 230 nm between the passive and active structures.

4.2.2 Substrate removal

Once the two material dies are bonded together, it is time to remove the InP substrate to access the epitaxial layers for the device's patterning. For that, we exploited two different solutions:

- Firstly, we used a $HCl:H_3PO_4$ solution with ratio 3:1 to etch away the InP substrate [101]. The InGaAs etch-stop protects the epitaxial layers, since it is not attacked by the adopted solution: in that way we could completely remove the substrate, as we can observe from Figure 93.
- In order to access the 450 nm epitaxial layer for the devices patterning, the etch-stop material has still to be removed. For that, we took advantage of the $H_2SO_4:H_2O_2:H_2O$ solution, quickly dissolving the 300 nm of InGaAs etch-stop and stopping the etching at the N-doped InP layer right underneath.

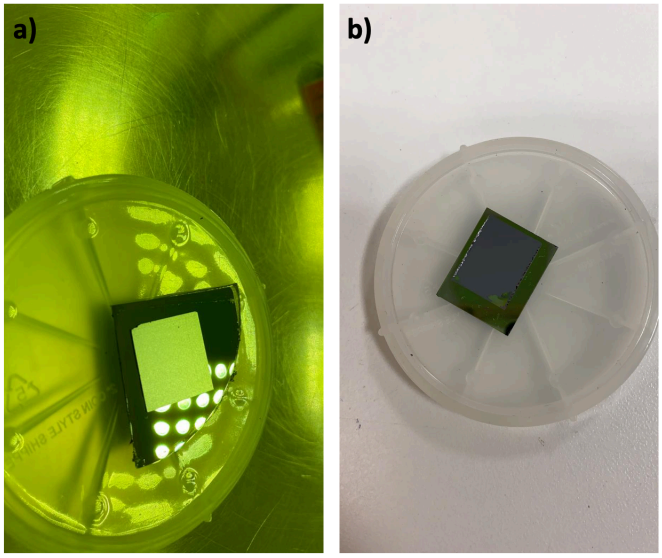


Figure 93: Pictures of substrate removal sequence: a) sample right after the adhesive bonding with the InP substrate still present and b) right after removal in a buffered HCl solution

4.3 Asymmetric 2D-PhC patterning and etching

Once the substrate and the etch-stop layer removed, we are ready to begin with the nanoamplifer and nanolaser patterning. The III-V material processing is achieved in two steps: firstly, we perform electron beam (e-beam) lithography to define zones to be fully removed followed by ICP etching, constituting the devices perimeter and the holes pattern. Secondly, with another e-beam lithography, we protect the holes pattern so to partially etch the unprotected III-V material, defining the 80 nm thick base and the 2D-PhC sidewall (Figure 94).

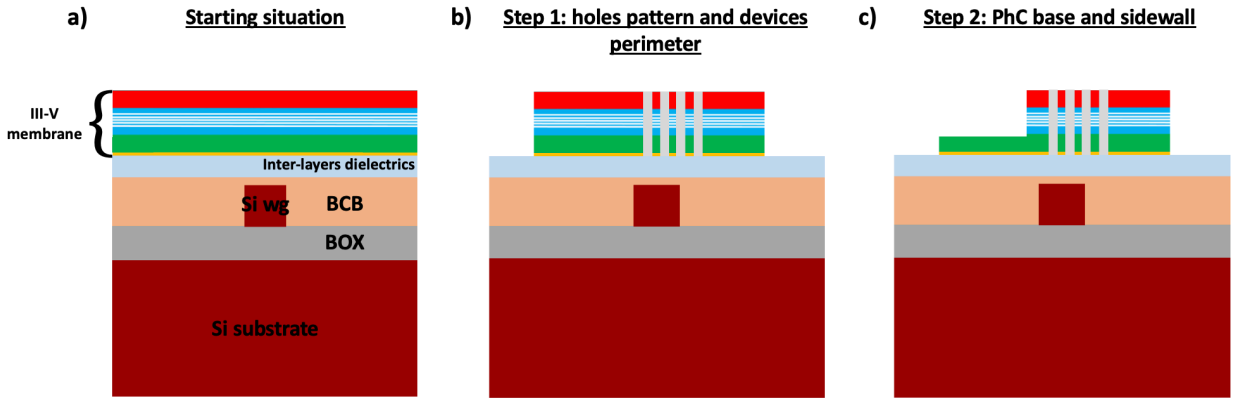


Figure 94: Schematics of the III-V material processing. a) shows the starting situation, after InP substrate and InGaAs etch-stop layer removal; b) represents step 1, where the PhC holes are drilled and the devices perimeter is defined, while c) represents the partial III-V etch, defining the PhC base and sidewall

In the next sections we will analyze and comment these two levels.

4.3.1 1st step

The layout is designed using the IPKISS library (python language), allowing us to create a GDS file. The latter is transformed into a GPF one using the software Layout BEAMER from GenISys [104]. This software defines actually the electron-beam path, giving us the opportunity to choose the lithographic resolution as well as the relative dose during exposure. Particularly important for this level is the definition of a proper fracturing [105] to precisely expose the holes contour, minimizing roughness.

The adopted resist was Hydrogen Silsesquioxane (HSQ), a flowable oxide highly used for high resolution masks. It is a negative resist, meaning that the pattern exposed to the electron beam strengthens and is not removed during development, becoming the mask for the successive etching step. Particularly, HSQ is described by the chemical formula $[HSiO_{3/2}]_n$ [106]: the exposure under an electron-beam breaks the hydrogen bonds, converting it to a hard mask of SiO_2.

The sample preparation for the e-beam lithography follows these steps: first of all, the HSQ Flowable Oxide (Fox) 15 (from Dow Corning Corporation) is spin-coated, in order to obtain an HSQ thickness of 300 nm. Then, a soft baking process takes place, in order to evacuate the excess solvent improving the resist planarization as well. After that, the sample is ready to go through e-beam lithography ebpg 5200 from Raith Company, capable of writing patterns with resolution below 1 nm and at frequencies up to 120 MHz. In order to precisely align the patterns to be written, we exploited the set of global markers mentioned during the SOI section. The idea is straightforward: the sample is aligned with the e-beam axis by identifying three reference markers, assigning them spatial coordinates. In that way the machine is able to write the defined

patterns at the desired position, with an uncertainty of the order of few tens of nm. After exposure, the sample undergoes a development process, in order to remove all the unexposed resist. This was done using a buffered-KOH solution (AZ400K) diluted in deionized (DI) water. Figure 95 shows the remained hard mask after development.

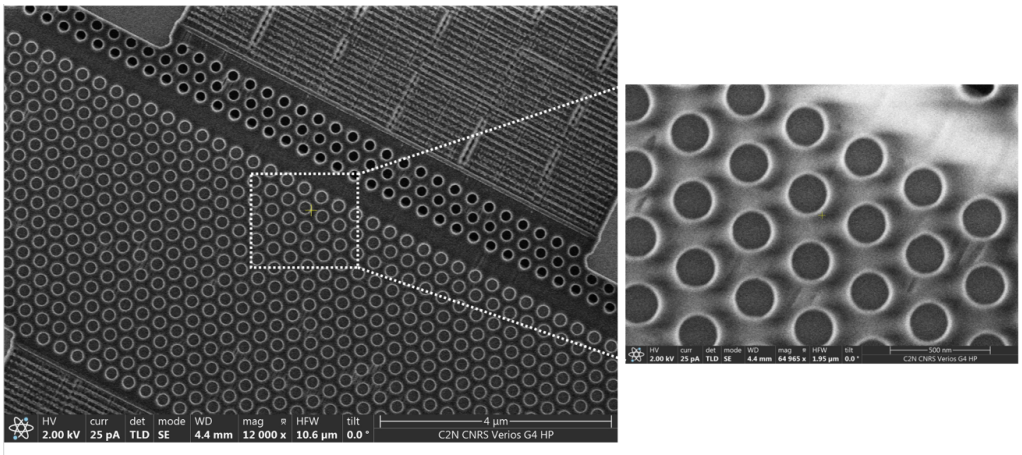


Figure 95: HSQ mask after development

The sample is then ready to be etched, drilling the 2D-PhC holes and defining the devices perimeter as well as the areas where the metallic contacts have to be deposited. Additionally, on the sides of each structure, we wrote also a set of local markers, in order to improve the alignment precision with respect to the global markers for the successive lithographic steps, reducing the alignment uncertainty to less than 10 nm.

4.3.1.1 ICP etching

After preparing the hard mask, it is time to perform the III-V etching. For that, we exploited an Inductively Coupled Plasma (ICP) RIE system (from Sentech). The particularity of such an etching system with respect to a standard RIE is that the plasma is turned on thanks to a RF antenna creating a magnetic field, which in turns induces an RF electric field exciting the electrons of the ionized species inside the chamber. The stronger the induced electric field is, the more ionized species available to chemically react with the material to be etched are created. In parallel to the RF ICP power, there is another RF bias power applied on the cathode, setting up the DC self-bias that controls the ions acceleration onto the sample: this process defines the sputtering rate. This etching technique combines chemical and physical etching, respectively controlled by the plasma density (induced by the RF magnetic field) and the bias power. The adopted gases are $HBr/O_2/He$: the calibrated recipe follows the work developed by Sophie Bouchoule et al. [107], where they could demonstrate that a passivation layer made of SiO_2 is formed on the sample's surfaces

during the etching process by using a silicon cathode. HBr is both accelerated onto the cathode, sputtering some silicon, and onto the InP material, chemically removing it: at the same time, the sputtered silicon reacts with O_2 in the chamber's atmosphere creating SiO_2, successively passivating the PhC holes surfaces. Our goal was to drill PhC holes presenting highly vertical sidewalls, in order to fabricate PhC devices as close to the ideal theoretical design as possible, minimizing the losses coming from fabrication imperfections. From Figure 96 we can appreciate the high quality etching we have calibrated during this PhD.

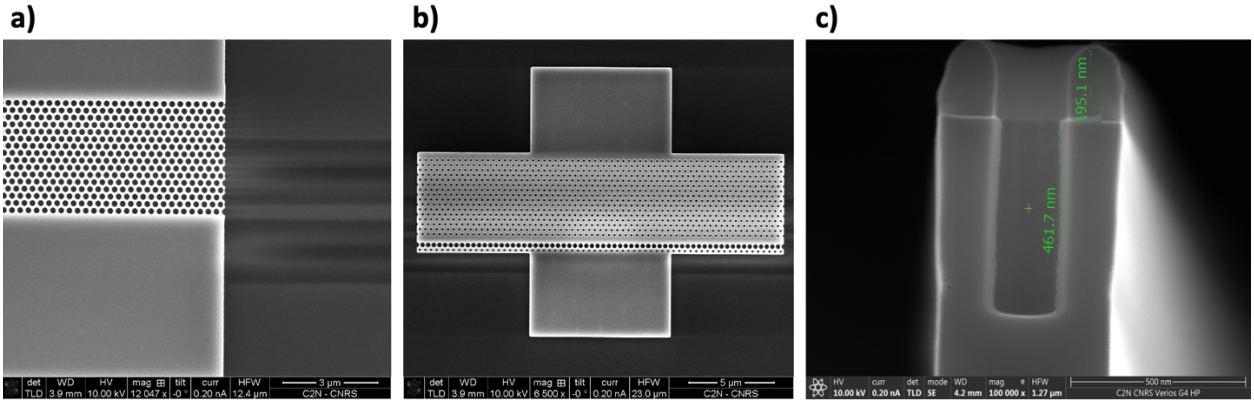


Figure 96: SEM pictures of ICP holes etching result for a) the nanoamplifier and b) the nanolaser. c) shows the cleaved facet of a test sample, where we can appreciate the high aspect ratio achieved with the calibrated ICP recipe

From Figure 96-a) we can observe the nanoamplifier's alignment with the silicon waveguide, placed right below the active structure (right side of the picture). Figure 96-b), instead, shows the full nanolaser structure, where apart from the holes pattern we can notice the two rectangles placed above and below it, representing respectively the areas where the N- and P-metal are going to be deposited. Eventually, on Figure 96-c), we can see the perfect sidewalls verticality achieved with the calibrated ICP etching; additionally, the whiter layers on the hole's sidewalls correspond to the SiO_2 passivation layer created during the process, while on top of the III-V material we can distinguish the HSQ hard mask.

4.3.1.2 HSQ removal

At the end of the ICP etching, the HSQ mask must be removed in order to process the patterned devices during the successive fabrication steps. To do that, reminding that the HSQ hard mask has a similar stoichiometry to SiO_2, we put the sample inside a BOE solution for a time of around 1 minute. It is during this process that we can finally appreciate the MgF_2 utility. We recall in fact that this material is not attacked by any hydrofluoric acid mixture. In that way, since we deposited

it onto the III-V surface prior to adhesive bonding, we can protect the underlying SOI platform from the BOE chemical attack. Figure 97 shows SEM pictures after the HSQ removal.

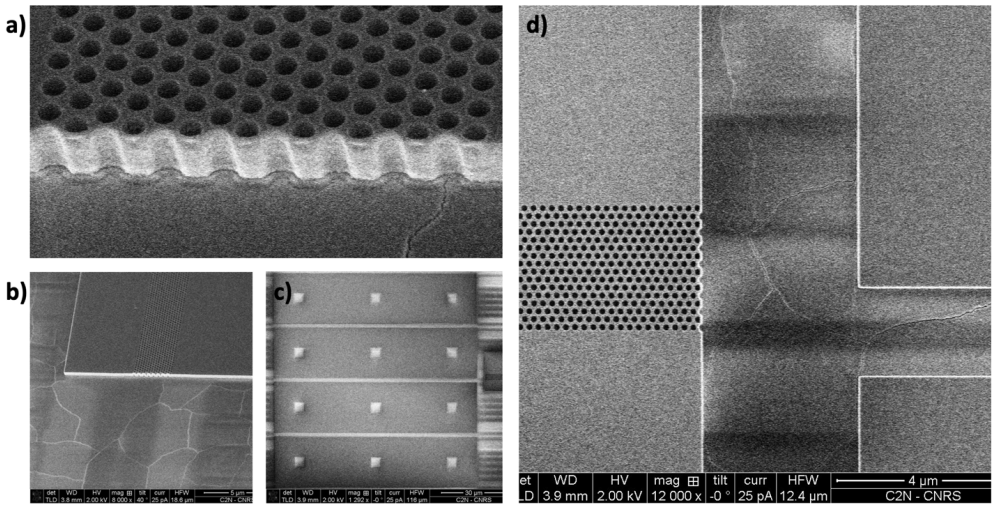


Figure 97: End of the first III-V fabrication stage after HSQ removal. a) close-up and b) zoomed-out tilted view of the nanoamplifier; c) etched local markers to minimize the alignment uncertainty for the successive levels; d) top-view of the nanoamplifier's right side, where we can appreciate the alignment with the underlying silicon waveguide and the local markers' extremities

From these pictures, we can immediately notice that the underlying MgF_2 has started to crack: this effect takes place once we put the sample inside the BOE solution for about a minute. Additionally, at the end of the second III-V material processing step we are going to remove another time HSQ by BOE wet etching, deteriorating even more the MgF_2 layer. We will comment on this later on this chapter.

We have finished with the first III-V fabrication stage; let us move now to the second one, consisting in etching down the III-V material on the base side, in order to access the P-doped layer for the P-contact metallization and to define the 2D-PhC sidewall.

4.3.2 2nd step

The general idea behind the second III-V fabrication stage is very similar to the first one: we protect the PhC holes pattern with a hard mask of HSQ Fox-15 and we etch the III-V membrane down to the P-doped layer, leaving a P-layer thickness of 80 nm. This time during the GPF file creation with Layout BEAMER, we had to be very careful to force the electron beam to scan the structures tangent to the PhC sidewall, applying the fracturing algorithm to smoothly define the wall's edge. If not, large sidewalls roughness would be obtained after ICP etching as shown in Figure 98.

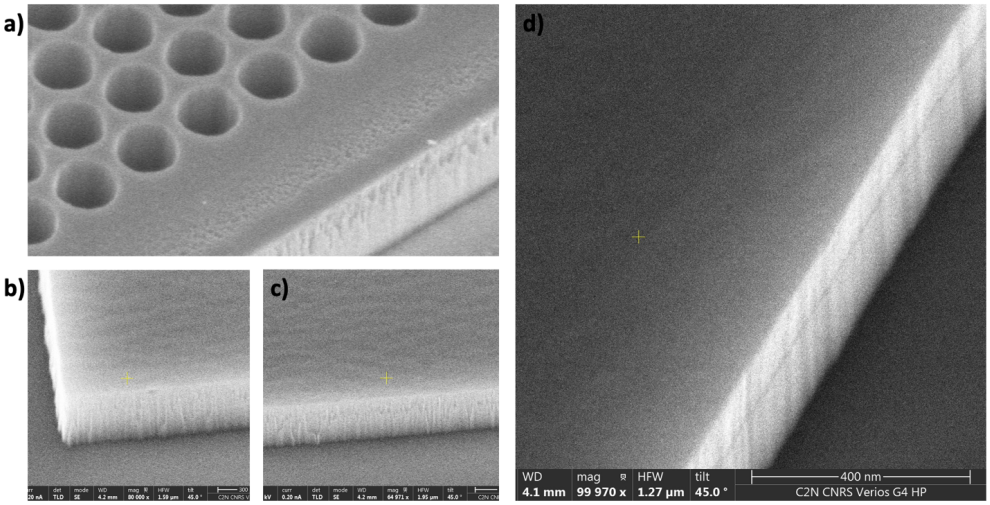


Figure 98: Second III-V fabrication stage etching examples. a), b) and c) show the sidewall's etching profile when the electron beam scan was not forced to be parallel to the wall; we can see that the profile presents a huge rugosity transferred from the HSQ mask. d) instead shows the etching result when the fracturing algorithm was applied to the layout mask

Figure 98-d) highlights the smooth etching profile achieved by properly controlling the electron beam writing direction. After the half-rib structure etching, the HSQ mask has to be removed: again, we used a BOE solution to do that. In that way, the fabrication of the asymmetric 2D-PhC structure is complete and we can proceed with the metallization of P- and N-contact. Figure 99 shows the patterned PhC structure at this stage.

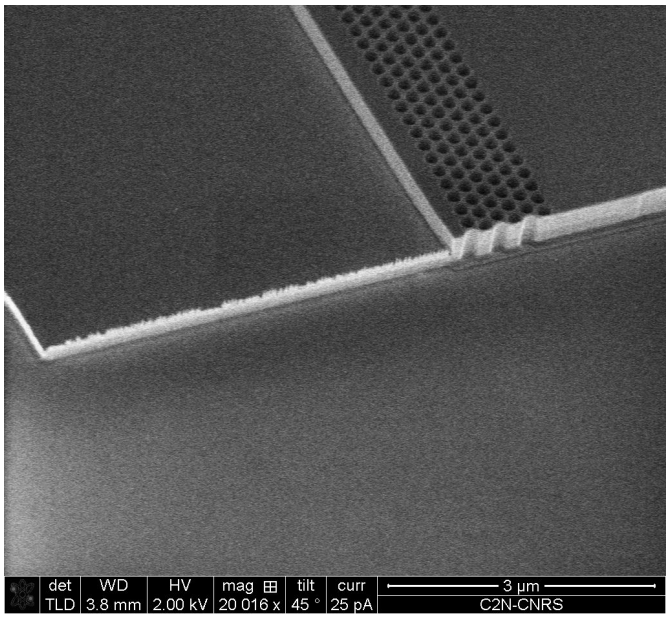


Figure 99: Final half-rib structure after base etching and HSQ removal (the example of that picture refers to the nanoamplifier)

4.4 Metallization

Once finished the patterning of the PhC structure, it is time to deposit metallic contacts, in order to inject electrical carriers inside the PhC waveguide (or cavity). The contacts pattern is designed by e-beam lithography, exploiting precise local alignment through markers like the one of Figure 97-c). This time, the adopted resist is a positive one called PMMA: the goal of this lithographic step is in fact to expose the contacts area, opening up the III-V surface where to evaporate the metals, eventually performing a lift-off to remove the unwanted metal deposited on top of the resist, using trichloroethylene as a stripper. We divided the metallization in two steps: firstly, the P-contact and then the N-contact metallization.

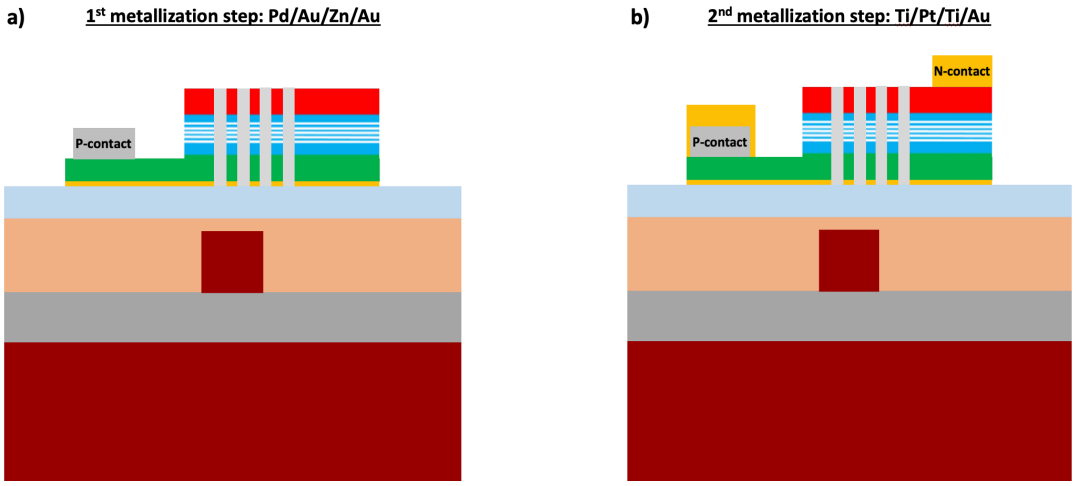


Figure 100: Schematics of the performed metallization steps

4.4.1 P-contact

After the e-beam lithography and subsequent development in a MIBK:IPA solution (with ratio 1:3), we performed a deoxidation step on the opened III-V surface: we immerged the sample in a HCl:H_2O solution, slightly etching the P-doped InGaAsP surface (few nm) in order to clean up the P-layer's surface as well as removing the native oxide, for an improved metal adhesion and P-contact electrical conduction. Then, we moved to the metallization step: for the P-contact, we adopted a multilayered metal of the type Pd/Au/Zn/Au/Ti/Pt/Ti/Au, with thicknesses 10/10/30/20/30/50/20/100 nm. This choice comes from the study developed in [108] and used in [71]: the goal is to create an ohmic contact performing, after P- and N-metal deposition, a Rapid Thermal Annealing (RTA) process to diffuse Zn down to the P-layer. The original multilayered sandwich from [108] is composed only by Pd/Zn/Pt/Au, but considering our clean room facilities not allowing to evaporate all these metals inside the same machine we were

forced to add a gold layer after Pd and Zn to avoid their oxidation once the sample was taken out from the vacuum chamber of their respective evaporator. Additionally, we decided to add a Ti layer before Pt and before the last Au layer to improve these metals' adhesion. The first Pd layer is used to create a uniform interface between the metallic contact and the P-doped layer, reacting and mixing with it at moderately low temperature (around 250°C). Zn is exploited to over-dope the metal-semiconductor interface through diffusion coming from the successive annealing process: with that over-doped interface, the electronic band energy difference between metal and semiconductor is reduced almost to zero, basically reducing the contact resistivity. Pt is used as a barrier to block the Zn diffusion through to the overlying Au layer during annealing and during the sample's electrical polarization [109].

After metallization we performed a lift-off process by immersing the sample inside a trichloroethylene solution, heated-up at 90°C, for a time between 30 minutes to one hour. During the characterization chapter we will show the achieved contact resistivity with such a multilayered P-contact.

4.4.2 N-contact

The N-contact fabrication relies on the same technological steps as the P-contact. After an e-beam lithography to pattern the contact, the N-doped InP surface is prepared for the successive metal evaporation through the same deoxidation step described for the P-contact. The adopted metals to constitute the full N-contact are Ti/Pt/Ti/Au with thicknesses 30/50/20/100 nm. The Ti guarantees good adhesion of the full metallic stack onto the InP surface. The Pt is useful to block the gold diffusion through the semiconductor. Again, a final lift-off procedure is performed to remove the unwanted metal from the whole sample's surface. Figure 101 shows a picture of the nanoamplifier after P- and N-contact constitution.

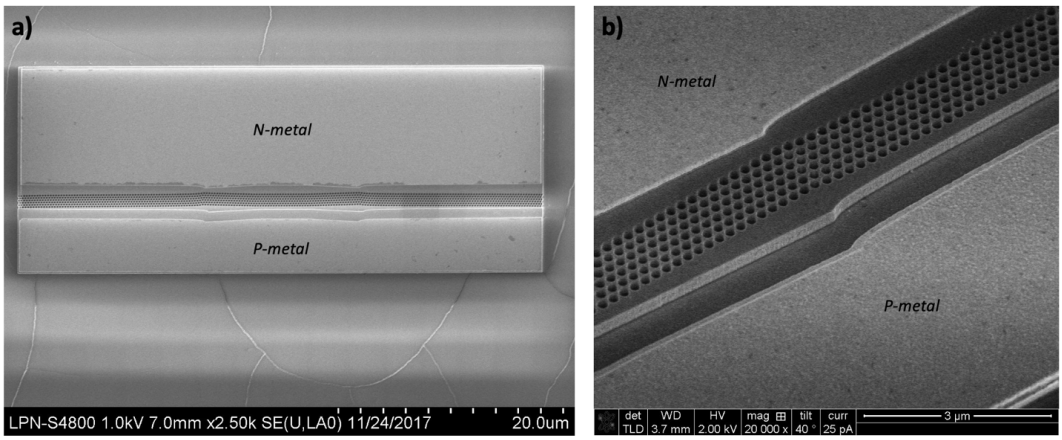


Figure 101: Nanoamplifier pictures after metallization. a) SEM top-view of the full device and b) tilted close-up view, where we can highlight P- and N-contact as well as the 2D-PhC waveguide's adiabatic taper

4.5 Annealing

As mentioned before, once P and N metallic contacts are deposited, we performed a RTA to diffuse Zn through to the metal/P-doped layer interface ensuring an ohmic contact and in parallel to activate the N-contact. This process was performed at 400°C for 30 seconds: as we will see during the last chapter, this temperature and this annealing time proved to be the best choices to minimize the contact resistivities. We can remark that such a temperature perfectly respects the limits imposed by CMOS technology, rendering the process flow suitable for a future co-integration of photonic and electronic platform on the same chip.

Up to this point, we have created the optoelectronic structures, by firstly patterning the III-V material (PhC holes and half-rib wall) and successively depositing the metallic contacts, activating them by a relatively low temperature process. What we still need to do in order to complete the 2D-PhC fabrication is surface passivation, structures encapsulation, via opening and final pads metallization. Before to proceed with these last steps, however, we want to dedicate the next section to the main technological problem we encountered during this PhD project, that forced us to slightly vary the order of the fabrication steps we have discussed so far.

4.6 MgF_2 problem: adhesion and strain

MgF_2 is a very attractive material to be integrated inside our hybrid structures for many reasons. As already discussed at the end of section 4.3.1.2, the HSQ hard mask removal with an HF-based solution after ICP etching is allowed thanks to its presence underneath the III-V membrane, protecting the underlying SOI circuitry by chemical attacks. Additionally, from a thermo-optical point of view, it presents small refractive index (improving the signal confinement by TIR inside the PhC structure), transparency at telecom wavelengths (avoiding signal absorption) and relatively high thermal conductivity (for an efficient heat sinking). On the other hand, MgF_2 is well known from the community for its elevated internal stress and for its poor adhesion: for a long time, in fact, many techniques have been under investigation to improve these characteristics [110]. Focusing on our structures, its internal stress begins to leave a mark once the HSQ hard mask is completely removed at the end of the first III-V fabrication stage by dipping the sample inside a BOE solution: MgF_2 starts to present some cracks (Figure 97). This effect is dramatic for the passive circuitry, since the cracks opens up a path for BOE to attack the SOI substrate. This was happening during the second HSQ removal step (after the PhC base etching): many areas of the samples were systematically destroyed by BOE chemical attacks. Some examples of the damages occurred after this step are shown in Figure 102. We can clearly notice the BOE diffusion through the MgF_2 cracks from Figure 102-e): around the cracks, there are black shadows where the SiO_2 is attacked by BOE. The consequence of the MgF_2 breaking is the damaging of the grating couplers (Figure 102-f)) and silicon waveguides (Figure 102-c)), rendering impossible the injection and/or extraction of an optical signal.

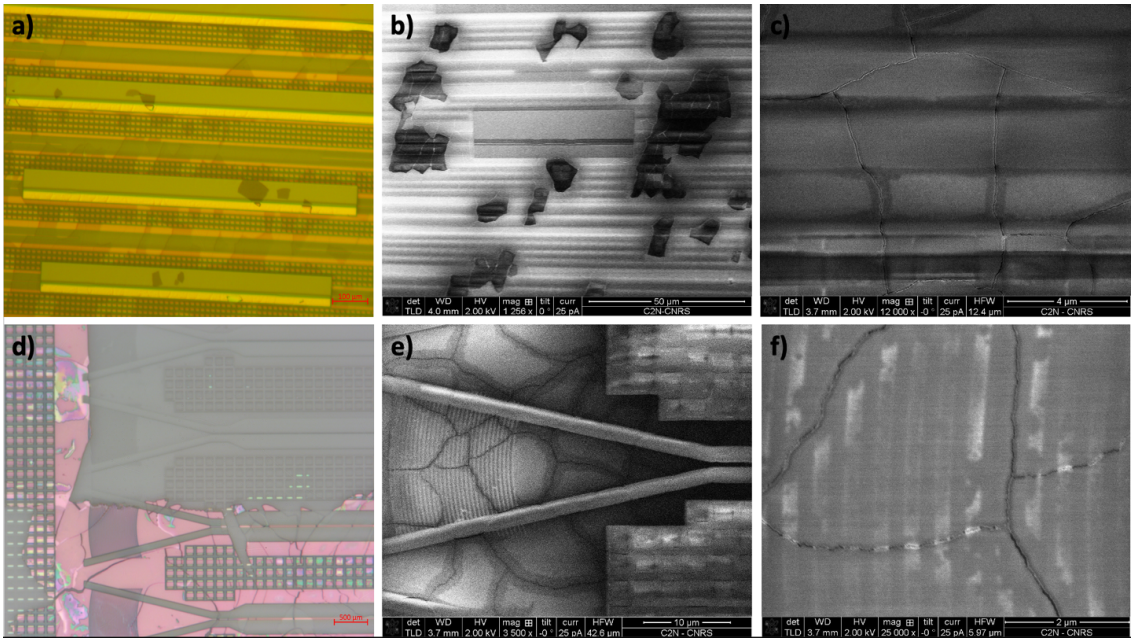


Figure 102: Pictures of damaged samples by MgF_2 cracks. a) optical microscope picture where we can see MgF_2 pieces lifted up after BOE bath, while b) shows a SEM picture showing the same problem. c) highlights a silicon waveguide clearly damaged around the cracks, where the BOE could diffuse through to the SOI. From d) we can observe a sample left for a longer time inside BOE, where some areas of the SOI are not only attacked but completely dissolved. e) and f) show respectively the MgF_2 cracks on top of a grating coupler and the close-up view highlighting the broken gratings

The understanding of this effect grabbed our attention for a long time during this PhD, looking for the reason of the cracks creation. First of all, MgF_2 is a hygroscopic material, meaning that when too much exposed to a humid environment or immersed in water, it is capable of absorbing water molecules at room temperature. This might lead to the material swelling, which in turns, once overcome the tolerated limit, starts to release the inner material stress, creating cracks all over the place. Another possibility is that the material breaking derives from its porosity: once the sample is immersed inside BOE, some small fraction of acid passes through the MgF_2 pores, attacking the underlying SiO_2 and ruining the MgF_2/SiO_2 interface as well as the MgF_2 adhesion on silica, which induces surface stress that cracks MgF_2. The material porosity can actually be increased when the sample is placed inside room temperature water or in a highly humid environment, according to [111]. The study of this material and its properties to optimize its deposition process would require further investigation beyond the scope of this PhD. Thus, we decided to remove it from our samples and to find an alternative way to achieve the fabrication of our devices.

The main difficulty surely resides in the small distance between active and passive circuitry: just putting silica underneath the III-V membrane would lead anyway to the SOI attack by HF-based acid, since silica etch rate in BOE is too high to protect the SOI level. An alternative solution has to be found in order to prevent as much as possible silica to be attacked by BOE.

4.7 Inversion of processing steps

After a huge effort trying to resolve the wet etching removal of HSQ, we found a good compromise by inverting the order of the III-V fabrication stages, as schematized in Figure 103.

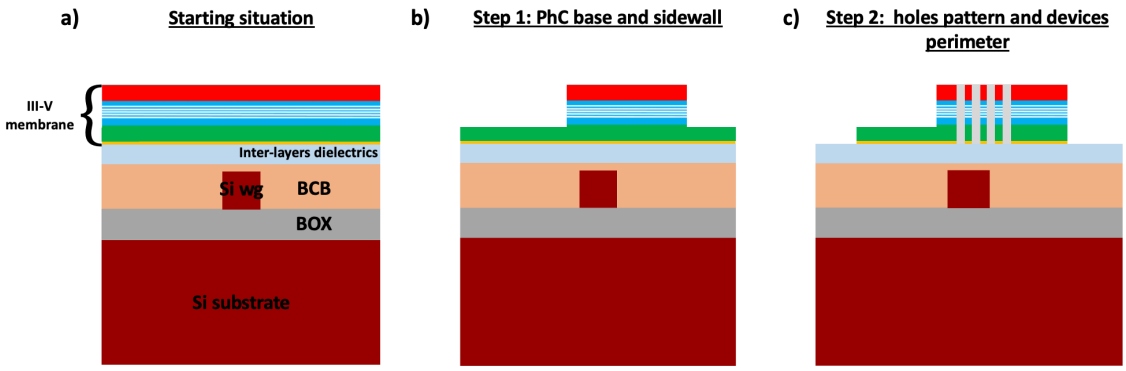


Figure 103: Schematics of the inverted III-V material processing. a) shows the starting situation, after InP substrate and InGaAs etch-stop layer removal. b) represents the partial III-V etch, defining the PhC base and waveguide's sidewall; the III-V material remaining on top of the SOI protects the passive circuitry from BOE chemical attacks. c) represents the PhC holes drilling and the devices perimeter definition

By patterning firstly the PhC base level, we guarantee the SOI protection by leaving III-V material on top, fully covering the passive circuitry from BOE chemical attacks while removing HSQ.

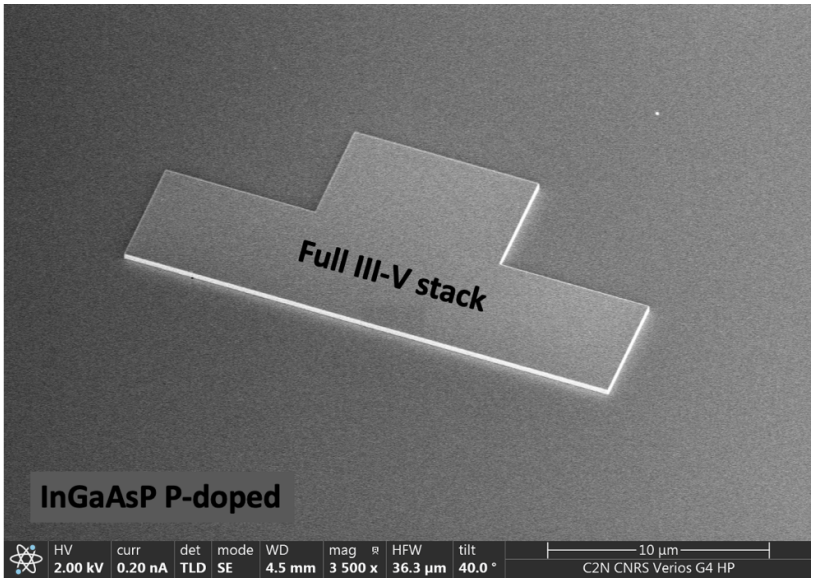


Figure 104: PhC base and sidewall creation performed as a first III-V fabrication stage; the SOI was covered everywhere by III-V semiconductor

In the course of our technological development, we firstly tried to pattern the PhC holes after this step. This was a poor choice: HSQ chemical removal is still a problem as BOE undercuts SiO_2 below the PhC structure which results in the collapse and the breaking of the structure's base. This effect is emphasized on the nanolaser cavities due to the presence of holes in the base, adding another channel to travel through for the acid solution, as we can clearly see from the next figure.

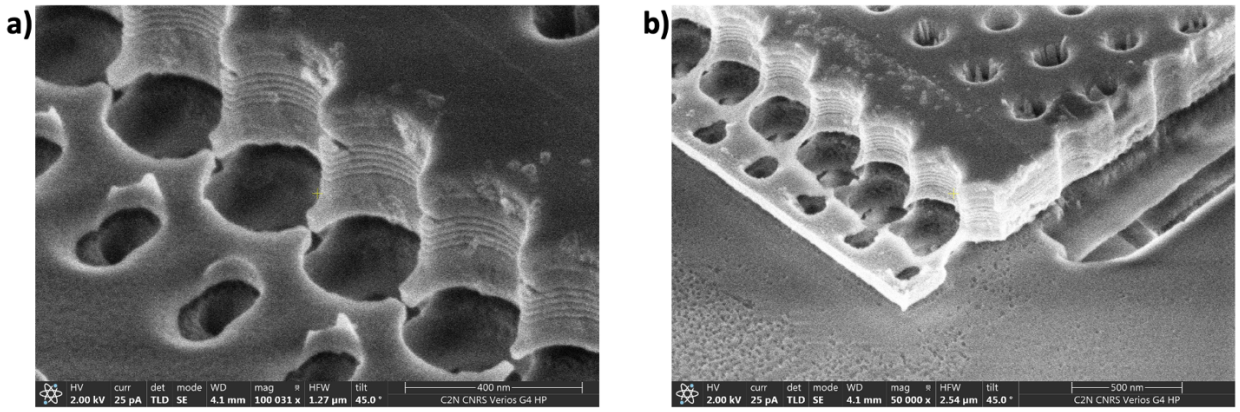


Figure 105: Close-up view of the PhC holes in the base for the nanolaser cavity after HSQ removal by BOE. We can notice that many connections between base and wall got destroyed due to the base collapse

A lot of silica below the III-V structure is attacked and we can see that at the sidewall's feet the base gets suspended, causing its successive collapse and, consequently, the cracking of many useful connections to inject electrical carriers inside the PhC active region.

Thus, we applied an additional variation to our fabrication steps leading us to the last calibrated technological process flow of the PhD work. We decided to firstly pattern the PhC base (always removing the HSQ through BOE at the end of the ICP), but instead of drilling the holes right after the partial etching we anticipated the metallization steps, leading to the configuration highlighted in Figure 106.

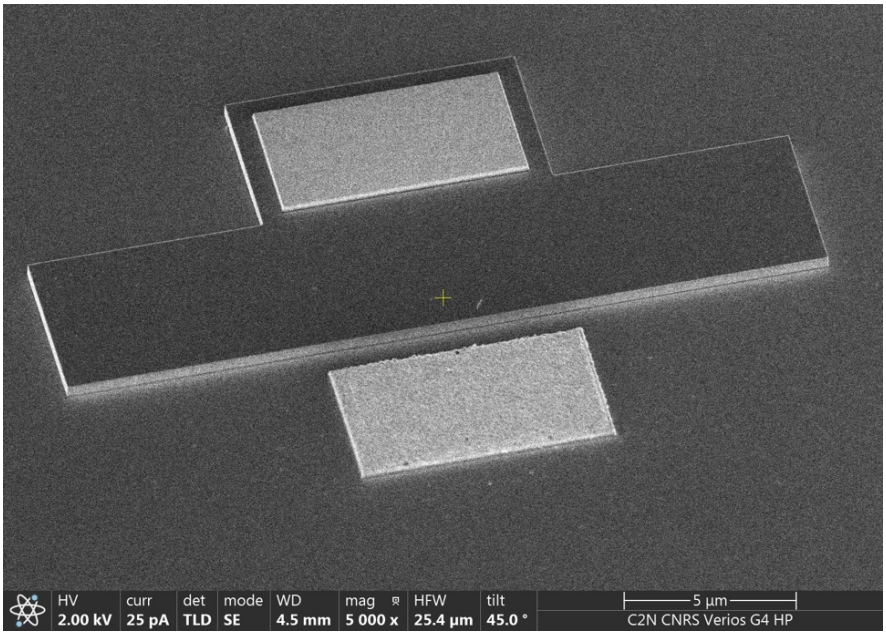


Figure 106: Nanolaser cavity example after PhC base etching and P- and N-contact metallization steps

At this point, we performed the PhC holes etching using HSQ as a mask. As the metallic contacts are already deposited, it is possible to leave the remaining HSQ and use it as a first encapsulation layer. In that way the second wet etching bath can be skipped, preserving the silica layer and, consequently, avoiding the collapse of the PhC base. Figure 107 shows the final device's configuration after this fabrication step.

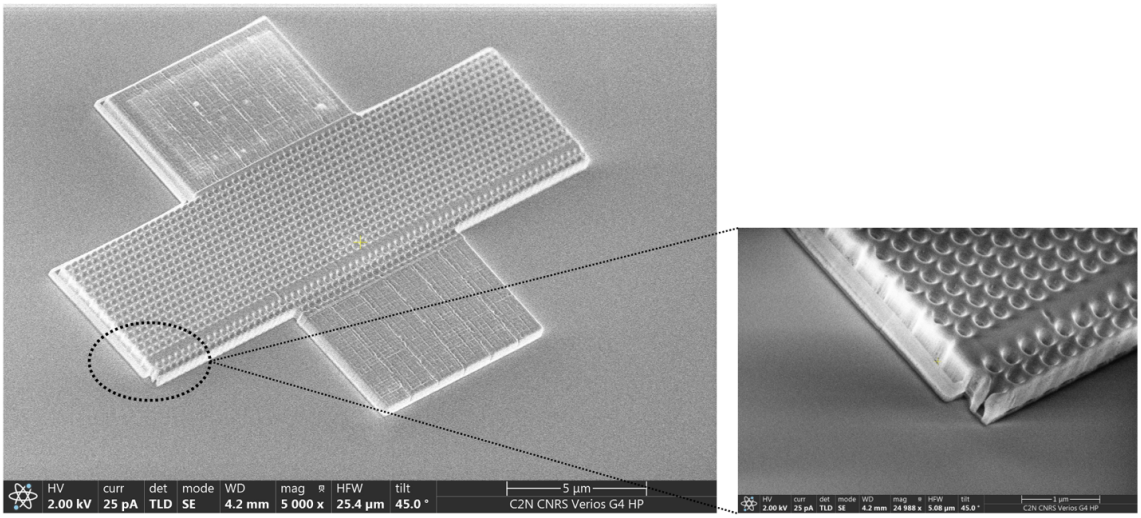


Figure 107: Final structure with the recalibrated process flow after both III-V fabrication stages and metallization, where the HSQ hard mask after the holes drilling is not removed. In the inset we observe a close-up view of the structure's corner, to highlight that the underlying SiO_2 is totally undamaged

The great advantage of such a configuration is that it gave us the possibility to fabricate PhC devices with great quality and with preserved SOI substrate in a highly reproducible way. On the other hand, leaving the HSQ mask onto the nanostructures surely degrades heat sinking, since HSQ is a bad thermal conductor. Up until now, this is the best tradeoff we achieved to fabricate this kind of devices. However, great efforts are currently done to improve MgF_2 adhesion and stress in order to exploit it as a protective layer, giving us the possibility to remove also the adopted HSQ mask to etch-down the PhC holes.

After this section where we discussed the re-calibrated process flow, we will analyze and comment the last technological steps we need to perform in order to complete the devices' fabrication.

4.8 Passivation

Our goal with these structures, as fully discussed during the chapters dedicated to their modeling, is to inject electrical carriers inside the active region and maximize the fraction of radiative recombination processes (consequently minimizing non-radiative recombination). However, a PhC device presents an elevated surface-to-volume ratio due to the large number of drilled holes, leading to a great amount of dangling bonds and crystalline defects at the opened surfaces and creating many trap states for the electrical carriers. As a consequence, non-radiative mechanisms significantly increase. It is fundamental, then, to counteract the non-radiative recombination events by passivating the surfaces.

To do that, we took advantage of two chemical solutions: firstly, the sample is dipped in a H_2SO_4:H_2O_2:H_2O solution with ratios 1:8:5000 for few seconds. The goal of this step is to slightly etch the III-V, cleaning the surfaces by removing interface crystalline defects. Then, the sample is immersed inside an ammonium sulfide solution ($(NH_4)_2S$), which both slightly etches the surface and deposits sulfur atoms onto the freshly opened surface, removing surface's dangling bonds. Thanks to this passivation step, we are able to increase the non-radiative carriers lifetime by at least an order of magnitude, as it has been demonstrated in [71].

4.9 Encapsulation

After the passivation, we can proceed with the encapsulation of our structures inside a silica layer. Such a fabrication step is necessary for three main reasons:

- Firstly, sulfur passivation has been demonstrated to be extremely volatile [112]. A dielectric deposition as a cap layer is fundamental to ensure the passivation's long-term stability.
- Secondly, when the structures are biased, we get some heat generation by Joule effect (electrical conduction through metals and through doped layers) and by non-radiative

recombination events; the heat accumulated around the devices must be evacuated to guarantee their correct operation. Instead of leaving the structures surrounded by air, we encapsulate them inside silica, which is a better thermal conductor.

- Thirdly, we want to protect the devices from the external environment.

The targeted silica layer thickness is 1 µm thick, to grant a safety margin for the heat evacuation as well as for the successive top-pads metallization. Our clean room disposed of different deposition techniques, each of them presenting some pros and cons.

4.9.1 Atomic Layer Deposition (ALD)

ALD is a thin-film deposition technique taking advantage of reactants inserted inside the chamber by mean of sequential pulses. During each pulse, reactants interact with the surface of the sample and the targeted material is chemically grown on top of it. Such a mechanism allows to control the growth at the atomic scale, providing extremely uniform, dense and conformal layers. Referring to our case, SiO_2 deposited by ALD would represent a great passivation cap layer thanks to its conformality, but due to the very slow deposition rate and the thickness limits imposed by our clean room engineers (few tens of nm) it cannot be exploited to fully encapsulate the structures inside a thick silica layer.

4.9.2 Plasma Enhanced Chemical Vapor Deposition (PECVD)

As the name suggests, this technique allows to grow the targeted material thanks to the exploitation of a plasma constituted by the reacting gases. An RF electric field creates the plasma and the ionized species are accelerated onto the sample's surface through the RF discharge between the two electrodes: the desired dielectric is then deposited by means of chemical reactions occurring at the exposed surface. PECVD offers the advantage of controlling the deposition rate, giving the possibility to grow thin as well as thick dielectric layers (at the expense of the material density, decreasing for faster deposition rates). Similarly to ALD, this technique gives conformal dielectrics, rendering it suitable for the passivation cap layer. On the other hand, PhC holes cannot be completely filled by SiO_2 if we choose to deposit the full encapsulation layer by PECVD: in fact, due to the important holes' aspect ratio (~ 3), the dielectric is conformally deposited on the holes' sidewalls but is grown more rapidly on the top surface of the III-V and especially on the holes' top circumference. As a consequence, the holes are plugged on their top surface before to be completely filled by SiO_2, leaving air bubbles inside them.

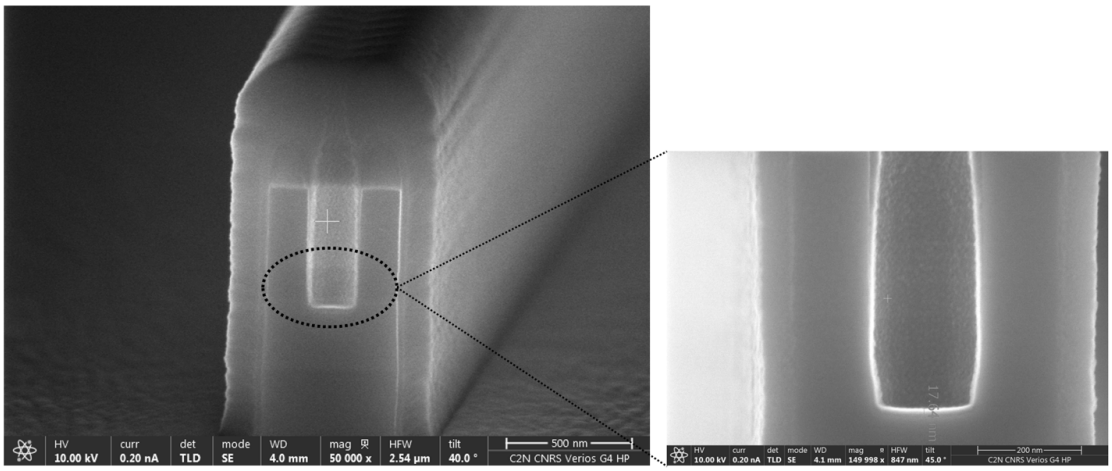


Figure 108: PECVD silica cap layer deposition on a test sample; as we can see the hole remains unfilled apart for a thin layer deposited on its sidewalls and on its bottom-side, due to the top surface closure during deposition

4.9.3 Sputtering

The sputtering deposition, contrarily to the techniques shown so far, is a Physical Vapor Deposition (PVD) process. An inert gas (such as Argon) is used to sputter a target material (in our case, silica) placed in front of the sample; the sputtered ions possess high energy due to Argon bombardment and they are accelerated through to the sample's surface thanks to the potential difference between anode (target material) and cathode (onto which the sample is clamped). Eventually, silica impacts energetically the sample's surface, completing the deposition process.

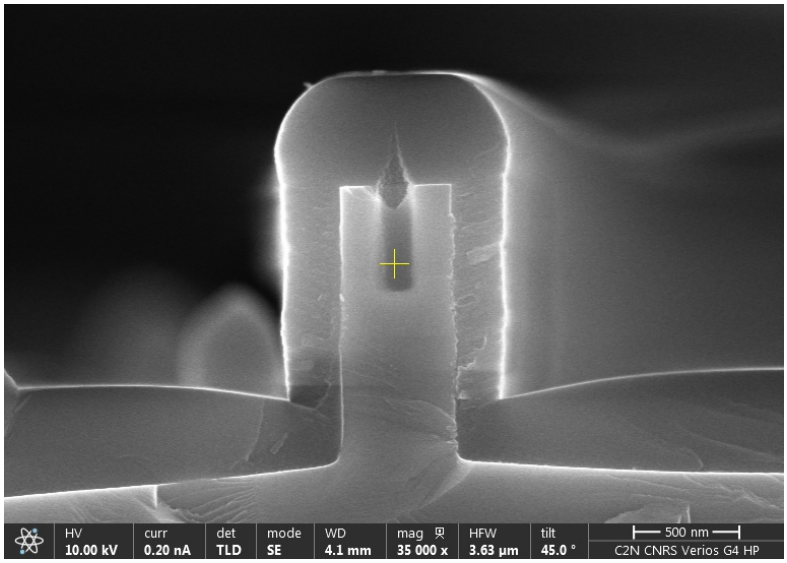


Figure 109: Sputtered silica deposited on a test sample; the PhC hole is entirely filled except for a small volume on top of it, due to the isotropic deposition plugging the aperture

Sputtering is an isotropic growth technique, which allows us to completely fill the PhC holes with SiO_2 except for an extremely reduced volume right above them (Figure 109); on the other hand, being a physical process, the main drawback is that the III-V surface is damaged if we directly deposit sputtered silica on top of it. In order to exploit it, we must firstly deposit a SiO_2 layer with proper thickness through one of the previously discussed techniques, capping the passivation layer and protecting the III-V material from the sputtered silica.

4.9.4 HSQ spin coating

The last encapsulation technique we tested during this PhD project relies on the utilization of HSQ. This resist, as previously discussed, can be converted into SiO_2 by breaking the hydrogen bonds composing its chemical structure. Such a transition can be achieved by focusing an electron beam on the desired pattern (in case of its exploitation as a hard mask) but also performing a high temperature curing. The idea is then to spin coat HSQ on the sample and then put it under vacuum increasing the substrate temperature to around 300°C: in that way, HSQ flows inside the PhC holes, perfectly filling them, and it evacuates the H-atoms becoming a SiO_2-like material.

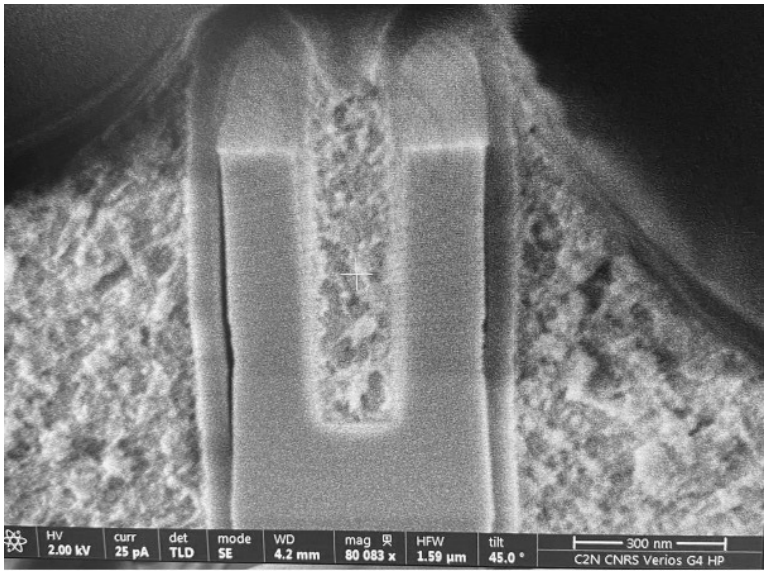


Figure 110: Test sample showing HSQ filling the PhC hole; we can immediately notice its higher porosity compared to CVD silica cap layer (conformally deposited on the hole's sidewalls)

The main advantages are the improved holes filling with respect to the previous techniques together with the encapsulation layer planarization, as well as the almost-zero optical losses that HSQ guarantees; on the other hand, this material offers a poor thermal conduction, deteriorating

heat evacuation. Additionally, it was observed during measurements that when structures encapsulated in HSQ were electrically biased, current leakage was occurring and radiative recombination mechanisms were highly reduced: by observing the biased devices through an IR camera, light scattering through the top surface was totally absent for any voltage drop, while the same structures encapsulated in SiO_2 deposited by CVD or PVD techniques were always showing surface electroluminescence starting from a certain amount of injected current. The exploitation of HSQ to encapsulate our devices proved to be a poor choice.

4.9.5 Final considerations

After all these calibrations, we decided to work with devices fully encapsulated in SiO_2 deposited by PECVD: this guarantees an efficient cap layer to protect the passivated sidewalls, even though holes are not completely filled. Figure 111 shows a TEM cross-section of the fabricated 2D-PhC structure after SiO_2 encapsulation by PECVD: as we can observe, the PhC holes get plugged on their top surface before being completely filled with silica. According to us, the best solution to fulfill the objectives listed at the beginning of this section would be to firstly deposit a PECVD cap layer, protecting the holes' sidewalls, and then finish with sputtered silica, in order to fill the PhC holes as much as possible; however, to do that, a minimum PECVD thickness must be deposited to protect the III-V from the highly energetic sputtered ions. Unfortunately, during our technological calibration work, we could not explore more into details these two techniques, but it absolutely represents an interesting prospect to further optimize the fabrication of our optoelectronic devices.

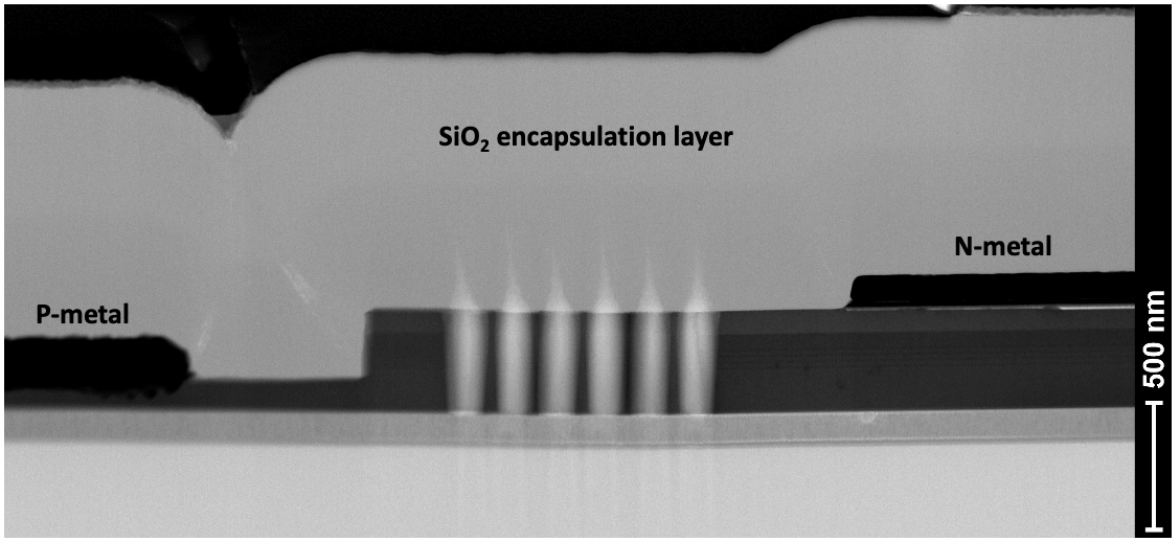


Figure 111: TEM-cross section of our 2D-PhC structure after encapsulation with silica deposited by PECVD. As we can observe, the holes get plugged on their top-surface during SiO_2 deposition, preventing their correct filling

4.10 Vias opening

After the structures encapsulation we must open vias through the thick silica layer in order to recontact P- and N-metal for the devices biasing. We calibrated a complex process in order to obtain vias with sidewalls possessing an appropriate slope: our goal was to metallize the vias sidewalls to provide metal continuity between top pads and bottom P- and N-contacts.

The calibrated process is composed of four different masks: on top of the silica encapsulation layer we have, in the order, a thick Silicon Nitride (Si_3N_4) layer deposited by PECVD, a thin Nickel (Ni) layer deposited by evaporation, another Si_3N_4 layer by PECVD (a bit thicker than the previous Ni layer) and eventually a spin coated PMMA mask. Figure 112 schematizes all the deposited layers.

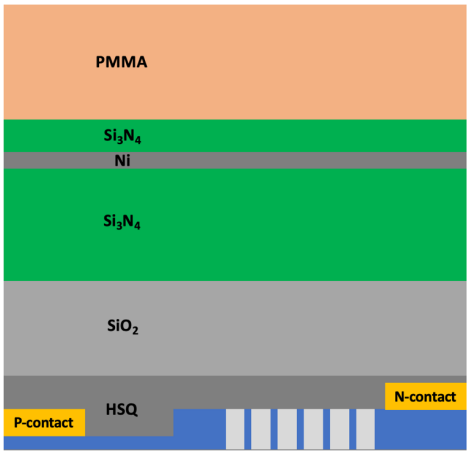


Figure 112: Cross-section schematics indicating all the different deposited layers

Once all layers deposited, we perform an e-beam lithography to write the vias on top of the structures' metallic contacts. After development, the Si_3N_4 is etched by RIE with a CHF_3/SF_6 plasma using PMMA as a mask. The remaining PMMA is then removed by plasma oxygen. After that, Ni is etched using Si_3N_4 as a mask: we do this by Ion Beam Etching (IBE), which is a physical process where an inert gas like Ar is accelerated onto the sample in order to sputter away the materials to be etched. Considering that Ni and Si_3N_4 have an almost equal etching rate with the calibrated IBE recipe, the deposited Si_3N_4 layer must have a sufficient thickness to be used as a mask in order to remove the exposed Ni areas: that is why we chose to deposit a Si_3N_4 layer slightly thicker than the Ni one. The successive step consists in etching down the thick Si_3N_4 layer with Ni as a mask: this is done using RIE with an SF_6 plasma. This process, in fact, etches very selectively Si_3N_4 with respect to Ni. Before moving to the final SiO_2 vias etching, the Ni mask is

chemically removed by dipping the sample in a HNO_3:H_2O solution with ratio 1:1. For the final vias etching, the thick Si_3N_4 layer is exploited as a mask. All these steps are summed up in the schematics of Figure 113.

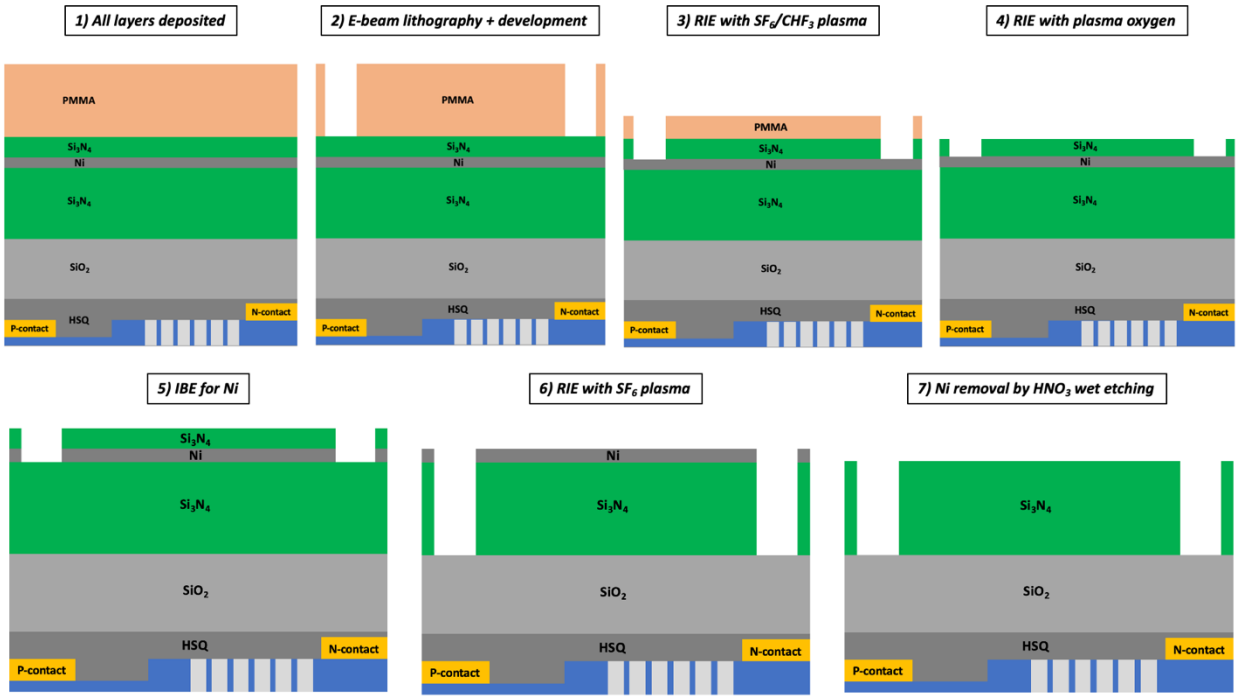


Figure 113: Schematics of the listed steps to prepare the final etching for the vias opening

The silica etching is then performed in two steps: firstly, an IBE process is used to facet the Si_3N_4 mask and the underlying SiO_2 layer. Then, a RIE process is exploited to complete the via opening, transferring the mask's slope on the protected part of the silica layer and avoiding to aggressively attack the N-metal while finishing the P-side opening (due to the height difference between P- and N-metal).

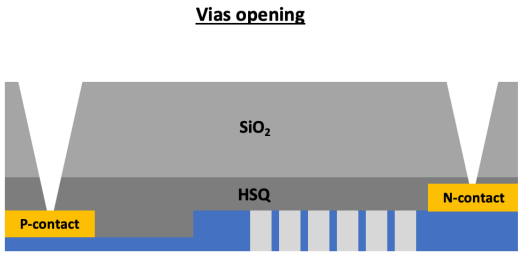


Figure 114: Schematics of the vias opening process

The calibrated IBE recipe was performed with normal ion incidence onto the sample's surface to cause a substantial faceting of the Si_3N_4 mask sidewalls due to the angular dependence of the etch rate [113]. While the Si_3N_4 mask edges are faceted, the silica layer is vertically etched due to the Si_3N_4 protection on the SiO_2 sidewalls: once that Si_3N_4 is consumed, anyway, the SiO_2 edges get faceted as well, properly shaping the vias for their successive metallization. Figure 115 shows the evolution of this etching process.

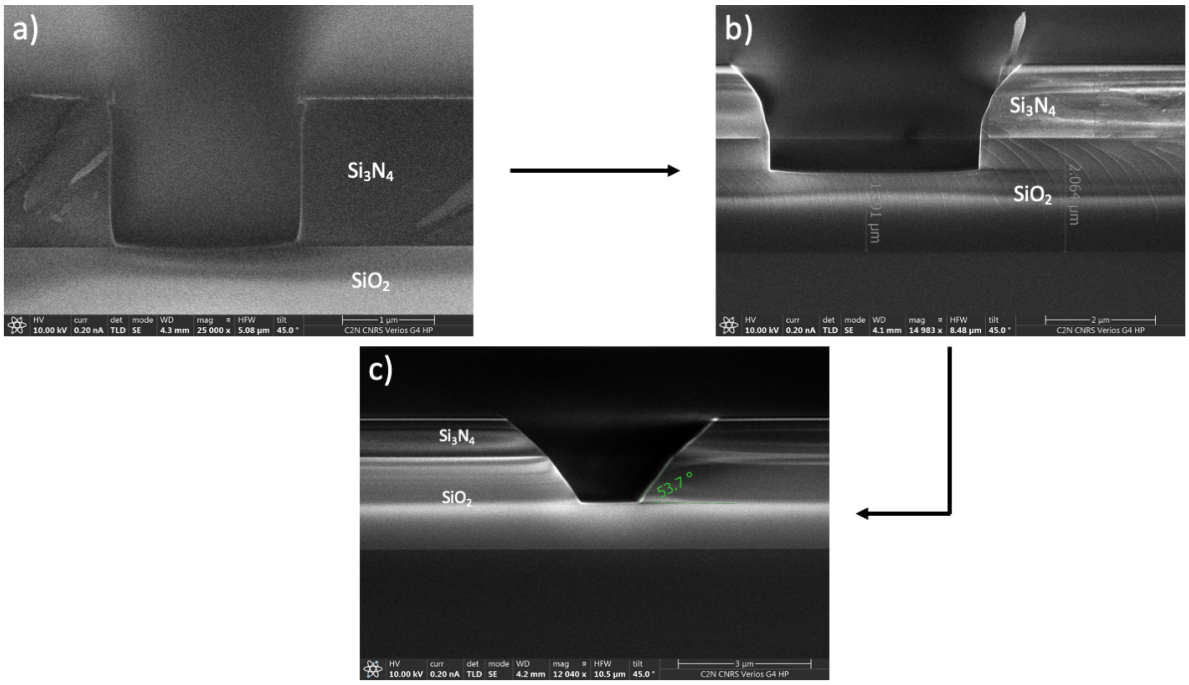


Figure 115: Si_3N_4 and SiO_2 evolution during IBE; a) Si_3N_4 mask right after its deep etching by RIE, b) IBE situation after an intermediate etching time showing the beginning of the Si_3N_4 mask faceting and c) final situation after full IBE, where both mask and silica present faceted sidewalls

In the next figure we can appreciate the final configuration after the RIE of the remaining SiO_2 in the vias.

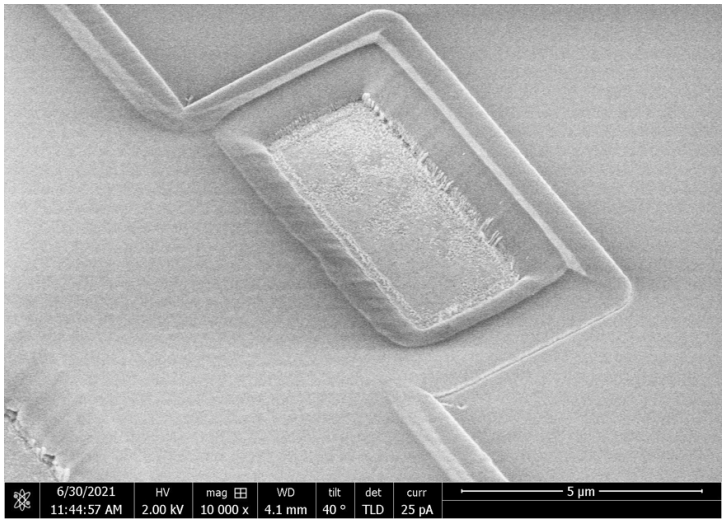


Figure 116: Opened via for a nanolaser structure, showing the nice slope we achieved thanks to the calibrated process

4.11 Final metallization

The last step of the process flow consists in creating the top metallic pads for the electrical probes, in order to be able to electrically bias the structures for their characterization.

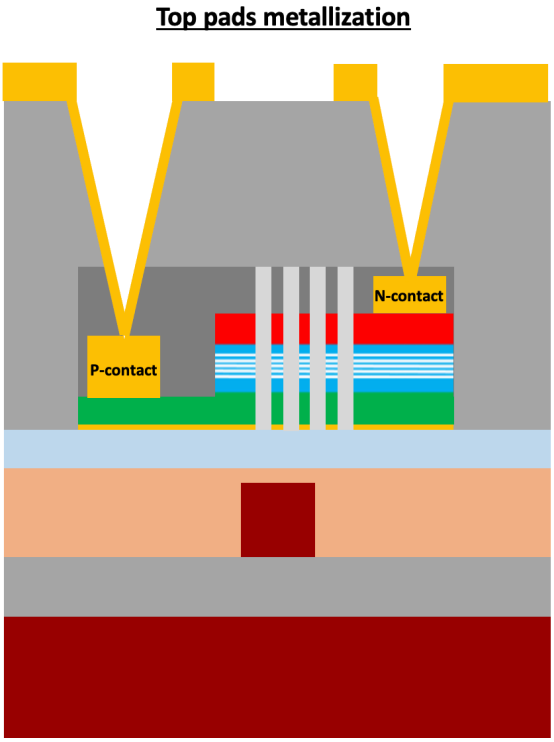


Figure 117: Schematics of the top-pads metallization

We performed an e-beam lithography using PMMA as a resist followed by a simple Ti/Au evaporation, where Ti is useful to guarantee a good gold adhesion on SiO_2. Eventually, the metal connections are created through liftoff. The tilted vias ensured metal continuity from the top of the encapsulation layer down to the structures' electrical contacts.

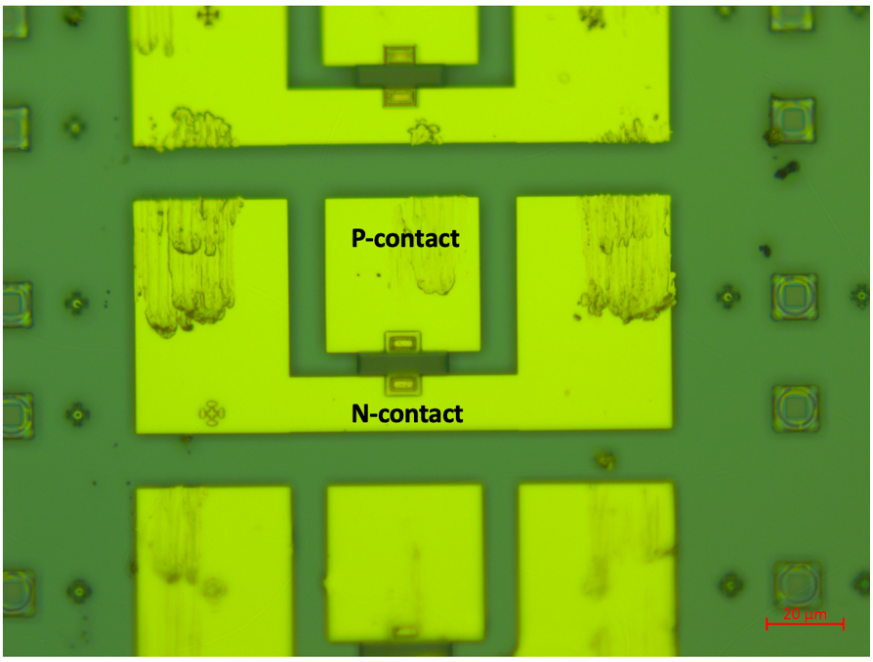


Figure 118: Final metallization realized on nanolaser structures, where we can distinguish the top pads (fabricated to perform electrical measurements with GSG probes) and the encapsulated nanolaser structure in the center

4.12 Conclusion

Such a long process flow gives us the possibility to fabricate the designed optoelectronic structures on a SOI substrate. The calibration of all the necessary steps took a long time, since we had to deal with a large number of technological steps interdependent with each other. Eventually we succeeded to develop a highly reproducible process flow, respecting the limitations posed by the CMOS back-end-of-line technology, fundamental for the conception of nanophotonic platforms co-integrated with microelectronic systems. The high quality achieved for each fabrication step was also confirmed by the obtained results during the devices characterization, that we will analyze in next chapter. Figure 119 shows a summary of the whole calibrated process flow.

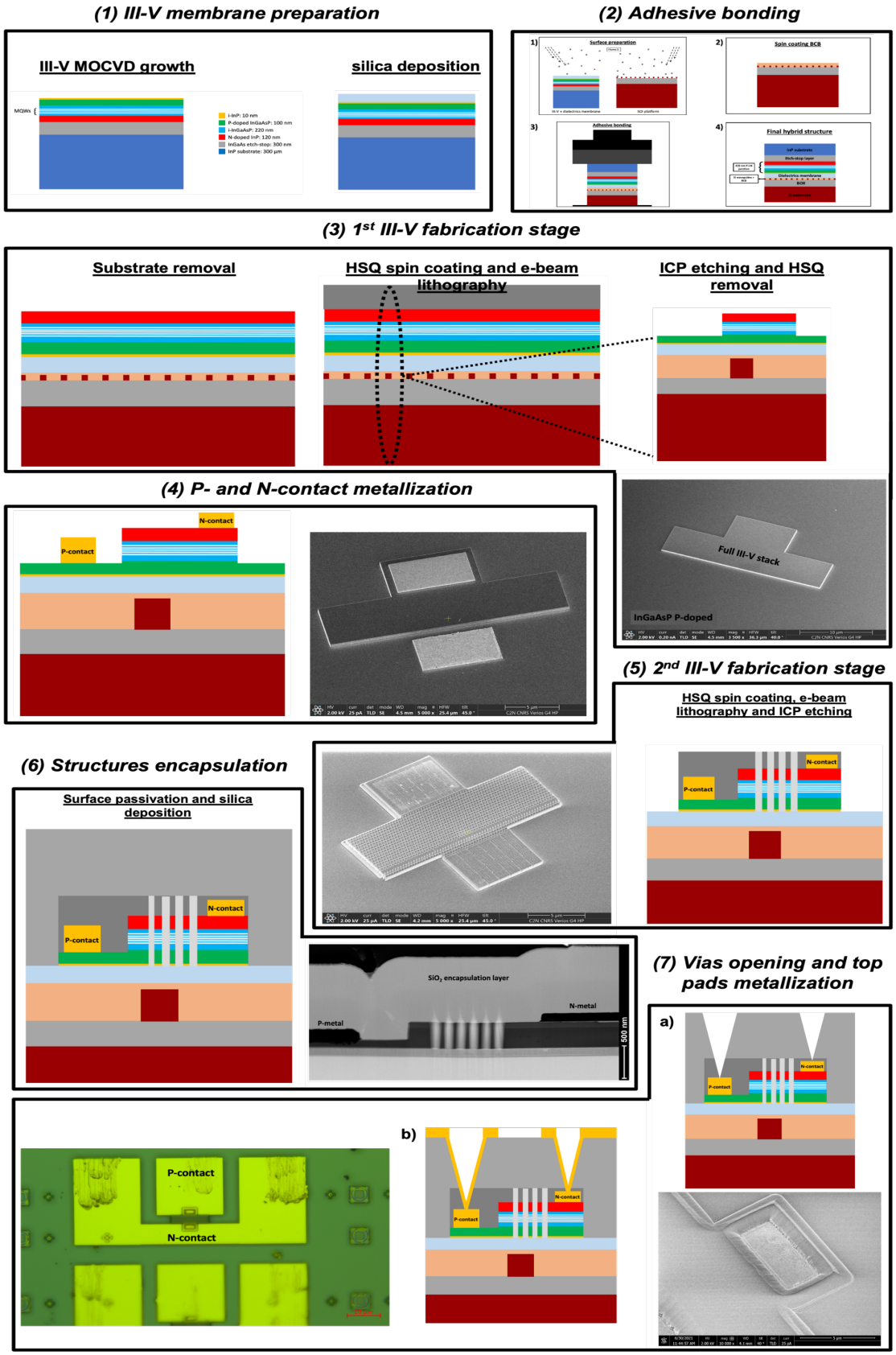


Figure 119: Process flow schematics for the fabrication of our 2D-PhC optoelectronics structures

Chapter 5: Experimental characterization

So far, we have seen how to design from an optical and electrical point of view a nanoamplifier and a nanolaser device based on a hybrid 2D-PhC structure (chapter 2 and 3). Later on, in chapter 4, we have analyzed the required technological steps to fabricate the full structures, showing the encountered difficulties and the acquired capabilities for the control of such a long and complex process flow. During this chapter, we will analyze and comment the measurements performed on the fabricated structures.

Firstly, we will show the electrical characterization of the 2D-PhC asymmetric structure: our goal is to analyze the contact resistivity, seeking for the bias power minimization and then to check whether our electrical injection scheme is comparable to the designed one. Then, we will treat the devices' characterization: in this manuscript, we will only show the results obtained for the nanolaser devices. The nanoamplifiers are the first structures we tried to fabricate and characterize during this PhD, but the measurements carried out for them are not conclusive, due to the fabrication problems we discussed during chapter 4. Thus, we decided to move to the nanolasers, fabricating them on plane silicon substrates: this allowed us to perform an easier characterization (signal extraction from the devices' top-surface) while working on the improvement of the technological process flow without wasting too many SOI dies. Firstly, we will investigate the cavities behavior under Continuous Wave (CW) optical pumping, moving then to their study under electrical Alternating Current (AC) and Direct Current (DC) bias. Eventually, we will analyze the cavities dark current and the carrier lifetime demonstrating that we still need to optimize the surface passivation process in order to achieve an efficient electrically DC biased nanolaser.

5.1 Electrical characterization

As already anticipated, from an electrical point of view, our goal was to understand how to minimize the contact resistivity and how efficient the designed lateral injection scheme was. For that, Transmission Line Measurement (TLM) and an Electron Beam Induced Current (EBIC) measurement were performed to study the highlighted points. In the next two sections, we will explain the idea of both measurements and discuss the obtained results.

5.1.1 TLM

Transmission Line Measurement is a characterization technique allowing to extract the contact resistivity between a metal and a semiconductor but also the resistivity of the semiconductor itself [125]. The idea behind that measurement is to place a series of identical metal pads on top of the semiconductor, varying the separation distance between them. We then perform an electrical measurement by polarizing each pair of adjacent contacts, measuring the resulting resistances and plotting them as a function of the metal-to-metal distance, as depicted in Figure 120.

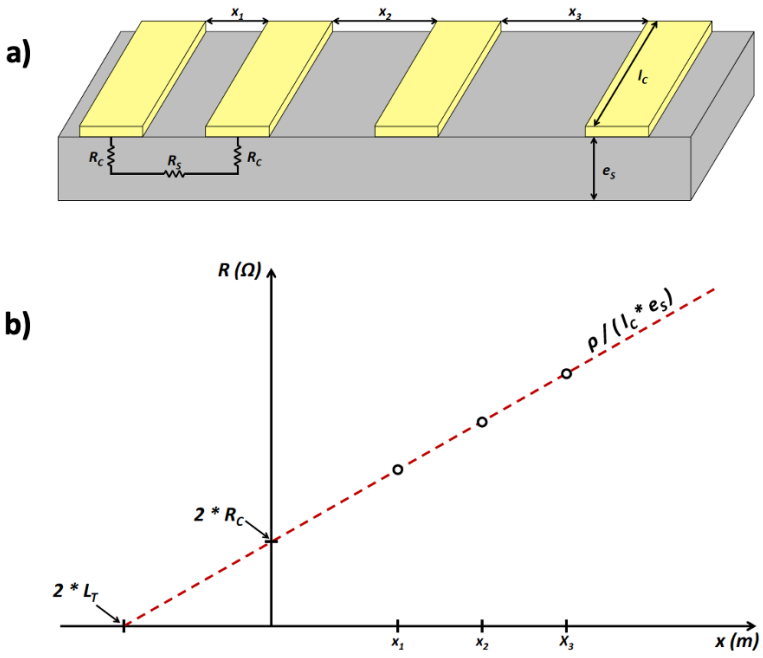


Figure 120: a) 3D schematics of the TLM configuration, with metals separated by different distances on top of the semiconductor (in grey); b) plotted measured resistances as a function of the corresponding inter-metal distance

As we can observe from Figure 120-a), each measured resistance results from the contact resistances R_c of the two metals and the resistance of the semiconductor portion between the two contacts R_s. By fitting the measured resistances, we can extract the contact resistance from the intercept of the fitting curve with the y-axis as well as the transfer length L_T from the intercept with the x-axis. The latter is a key parameter: it tells us which is the effective longitudinal length to take into account for the deposited contacts. The current, in fact, does not flow uniformly beneath the metallic contact, but it is mainly distributed at the inner edge of it: this effect is known as current crowding. We define the transfer length as the average distance an electron

travels in the semiconductor beneath the metallic contact before flowing up into the contact (see Figure 121).

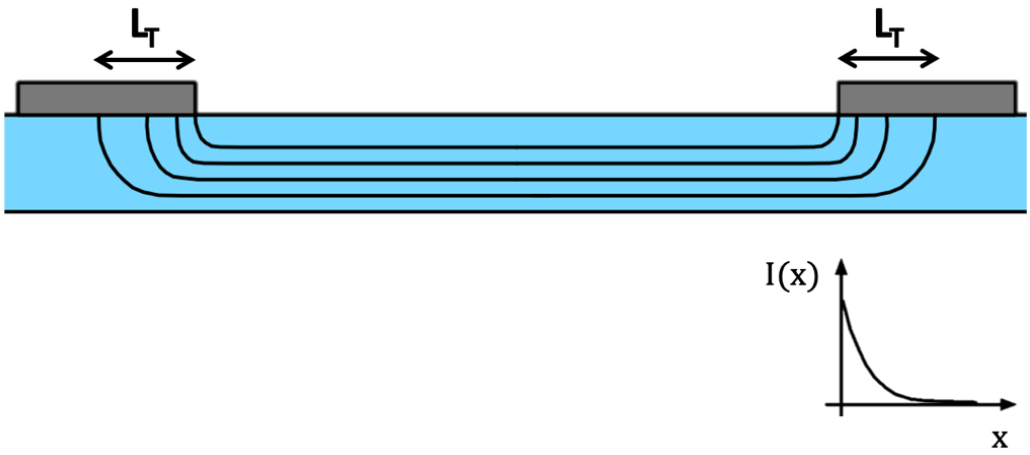


Figure 121: Cross-section schematics representing the current crowding effect: the current flux inside the semiconductor (light-blue block) is constant between the two metals (grey blocks), while beneath the contacts it is not uniform, being valuable for an effective length called transfer length (L_T). As we can observe from the plot placed below the contact on the right side of the picture, the current tends to decrease exponentially as far as we move away from the contact's inner edge, where the characteristic length of the exponential decay is exactly L_T

Once these two parameters extracted, it is possible to calculate the contact resistivity ρ_c as the product between the contact resistance and the contact effective area. Referring to Figure 120-a) we have:

$$\rho_c = R_c \, L_T \, l_c \tag{5.1}$$

Where l_c is the contact width. We can notice that we are also able to extract the semiconductor resistivity from the slope of the linear fit:

$$\frac{\partial R}{\partial x} = \frac{\rho}{l_c \, e_s} \tag{5.2}$$

Where ρ is the semiconductor resistivity and e_s the semiconductor thickness.

5.1.1.1 Performed characterization

Considering our structures, we recall that in the stack of metals composing the P-contact we also have Zn, which is diffused by RTA to the metal/semiconductor interface in order to over-dope it, rendering the contact ohmic: without this process, the contact would present a Schottky barrier, dramatically increasing the contact resistance. Additionally, the final contact resistance is directly dependent on the annealing time and temperature: our goal with this characterization was to

find the best tradeoff in order to obtain an ohmic P-contact with a resistivity as low as possible. On the other hand, the N-contact did not worry us from that point of view, since it relied on a stack of Ti/Pt/Ti/Au, which is very well known to provide an ohmic contact even without an annealing, when deposited on N-doped semiconductors [114], just like in our case.

In order to choose the RTA temperature, we started by imposing an upper limit: the BCB used for the adhesive bonding, began to be degraded at a temperature of 450°C due to the emergence of bubbles. As a consequence, we started to test our TLMs at a temperature of 350°C, with an annealing time of 30 s. However, as we can see from the graph of Figure 122, after the RTA with the chosen parameters the P-contact still presented a Schottky characteristics.

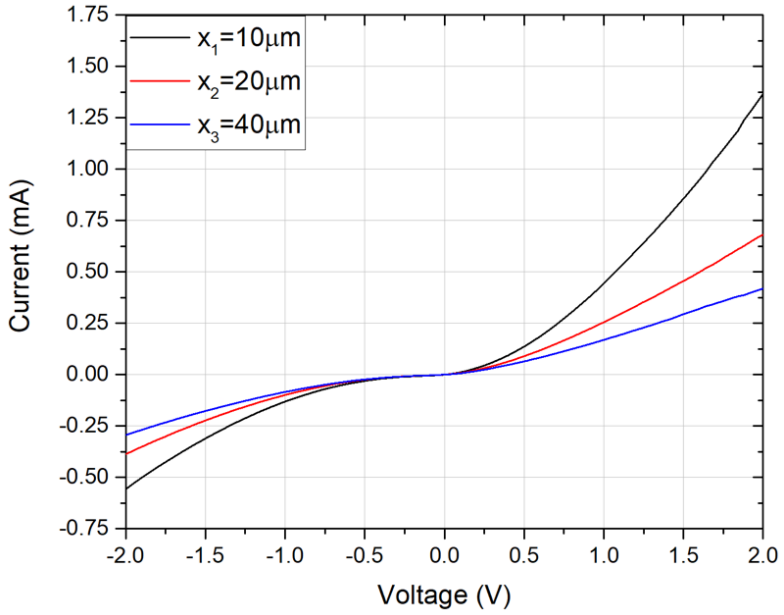


Figure 122: IV curves for three different distances after RTA at 350°C for 30 s

We have two possibilities to achieve an ohmic contact: either we increase the annealing time or the annealing temperature (or both). We decided to increase the temperature to 400°C: this time, ohmic contact condition was successfully achieved starting from an annealing time of 30 s, as we can observe in Figure 123.

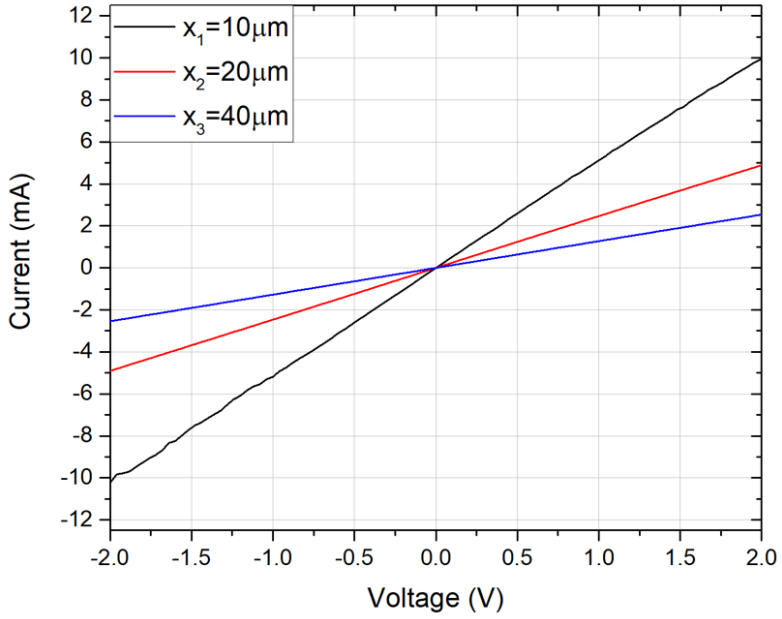


Figure 123: IV curves for the same distances as Figure 116, this time after an RTA at 400℃ for 30s

Once extracted the resistances associated to each separation distance between metal pads, we could plot the TLM graph as in Figure 120-b. We also performed tests by increasing the annealing time (see Figure 124).

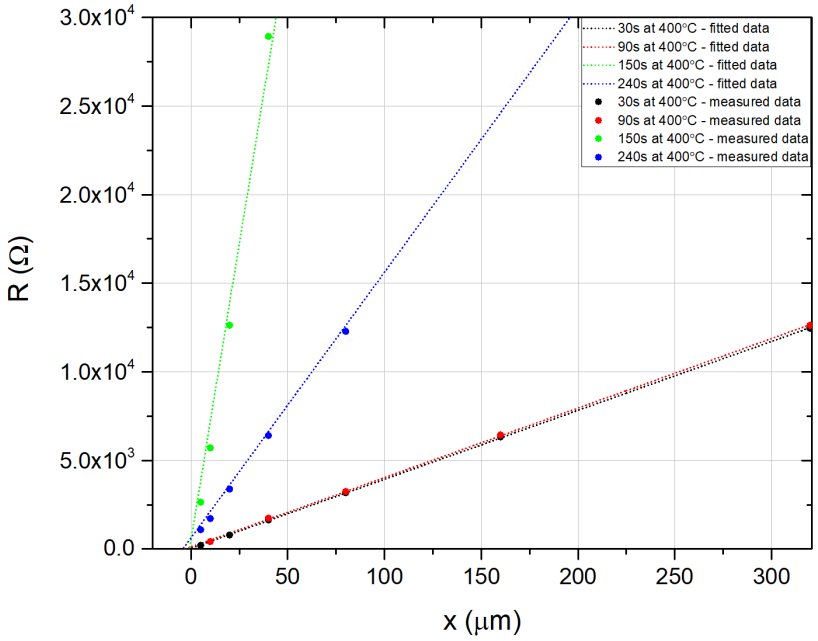


Figure 124: Measured resistances as a function of the metal-to-metal distance

The linear fits allow us to extract the necessary parameters to calculate the resistivities: all the extracted data are listed in the following table.

Annealing time	Rc	L_T	ρ_c
30 s	$21.4\ \Omega$	$0.55\ \mu m$	$5.6 \cdot 10^{-5}\ \Omega\ cm^2$
90 s	$55.1\ \Omega$	$1.4\ \mu m$	$4 \cdot 10^{-4}\ \Omega\ cm^2$
150 s	$259.1\ \Omega$	$0.4\ \mu m$	$5 \cdot 10^{-4}\ \Omega\ cm^2$
240 s	$313.3\ \Omega$	$2.1\ \mu m$	$3.3 \cdot 10^{-3}\ \Omega\ cm^2$

Table 6: Extracted parameters from the TLM measurement at 400°C

At 400°C, the optimum of resistivity is achieved after a rather short annealing time (30 s), while if we increase it, the resistivity grows rapidly, becoming two orders of magnitude larger for an annealing process of just 4 minutes. Thanks to this characterization, we found the best RTA parameters allowing us to minimize the P-contact resistivity. Additionally, performing the TLM measurement with the same RTA parameters for the N-contact, we could extract a contact resistivity of $3.7 \cdot 10^{-4}\ \Omega \cdot \mathrm{cm}^2$, with L_T of 11 µm.

5.1.2 EBIC

The second electrical characterization we want to show and comment during this chapter is Electron Beam Induced Current (EBIC) measurement. This technique is typically used in semiconductor physics: it allows to identify and highlight material properties of the Device Under Test (DUT), such as crystalline defects [115], diffusion length of minority carriers [116], doping profiles [117] and surface recombination rate [118]. Particularly, when dealing with a P-N or P-i-N junction, EBIC gives the opportunity to locate the DUT's depletion region and map the diode's electronic activity. This is of great importance to us: we want to be sure that the modeled electrical carrier injection scheme is actually accurate and reproducible for the fabricated samples.

5.1.2.1 EBIC working principle

An EBIC measurement is typically run in a Scanning Electron Microscope (SEM): the idea is to focus an electron beam on the DUT surface with an arbitrary acceleration voltage, in order to inject energetic electrons inside the semiconductor and excite electron-hole pairs. If the generated pairs are able to diffuse through to the junction's depletion region, the carriers are separated by drift due to the built-in electric field. By placing electrical probes on P- and N-contact and connecting them to an Ampere meter, it is possible to measure a drift current of minority carriers, induced by the SEM electron beam focused on the DUT. In order to completely map the DUT electronic activity, the electron beam is scanned across the full device's surface.

Thanks to the SEM, then, it is possible to image the current flowing inside the sample: the higher the induced current is, the brighter the image at the SEM screen will be. On the other hand, a darker image highlights regions where the generated electron-hole pairs spontaneously recombine without contributing to the induced current. In that way, thanks to the image contrast in the EBIC map, we are able to highlight the flow of minority carriers inside the junction diode, mapping the device's electronic activity. Depending on the DUT characteristics, it is fundamental to properly choose the characterization parameters: particularly, the SEM acceleration voltage and the DUT bias voltage have to be carefully selected. The former defines the electron-hole pairs generation volume, as depicted in Figure 125.

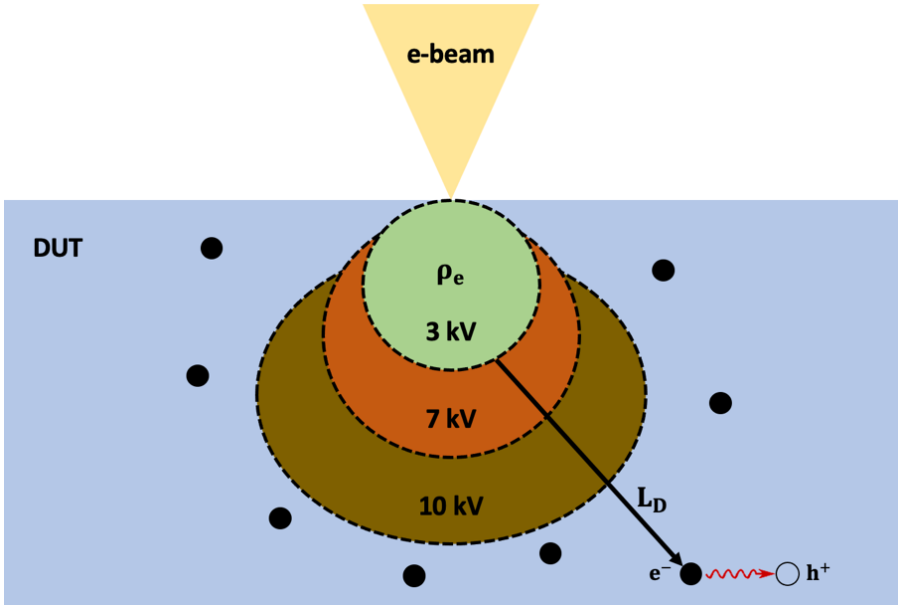


Figure 125: Cross-section schematics of the electron bombardment from the SEM cannon. The electron beam (in yellow) is focused on the DUT's surface and minority carriers are generated inside the semiconductor (with density ρ_e); the higher the acceleration voltage is, the bigger the volume of generated electron-hole pairs becomes. L_D represents the minority carriers' diffusion length: once covered that distance, the generated pairs spontaneously recombine

The represented schematics stresses out the importance of the electron beam acceleration voltage: the higher it is, the bigger the volume of generated electron-hole pairs becomes and the deeper the carriers are generated inside the semiconductor. The black dots represent the generated electrons propagating inside the DUT: once they cover a distance corresponding to the diffusion length L_D, they spontaneously recombine with the corresponding hole composing the excited electron-hole pair. It is fundamental that the acceleration voltage is high enough to generate carriers in close proximity to the junction's depletion region, letting them diffuse into it, but not too high to avoid generating pairs deeper than the depletion region position.

The second parameter we can play with during this characterization is the bias voltage of the DUT. It is well known that in a P-N or P-i-N junction, the depletion region width can be modulated by the applied voltage across the junction: in forward bias, the higher the voltage is the thinner the depletion region becomes, since a higher fraction of majority carriers is able to diffuse through the depletion region neutralizing opposite charges. Under reverse bias, instead, the smaller the applied voltage is, the wider the depletion region becomes, since majority carriers are pushed away from the junction, depleting more and more the P-N (or P-i-N) interface. In that way, the built-in field becomes stronger, increasing the amount of drift current flowing through the depletion region. This property might come handy in an EBIC measurement when we are facing some difficulties in getting the generated pairs captured by the built-in electric field: reducing the bias voltage leads to the widening of the depletion region, which in turns increases the capture rate of the generated pairs and, consequently, the induced drift current.

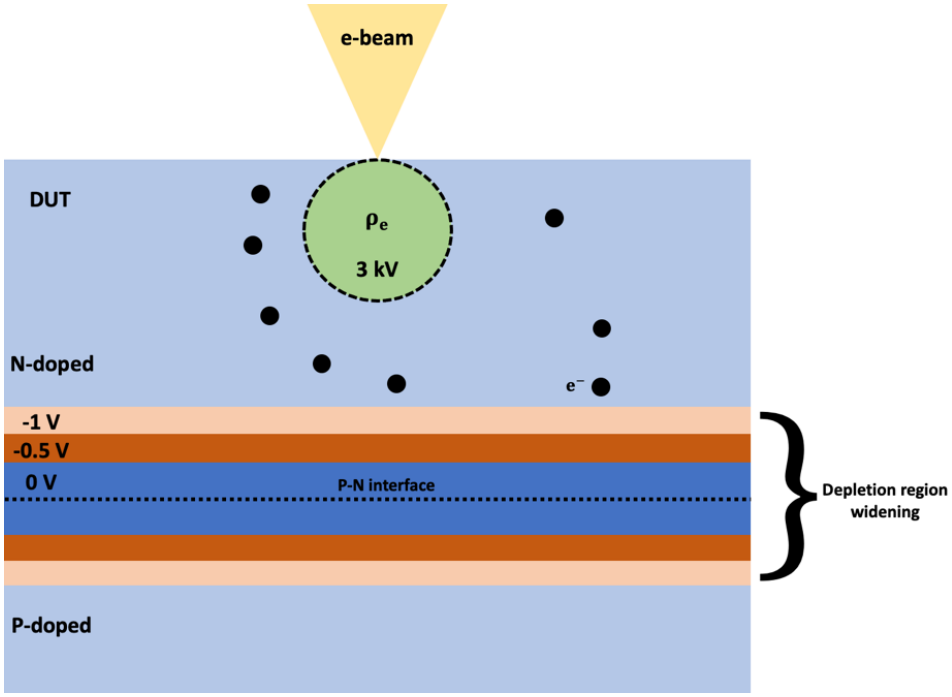


Figure 126: Cross-section schematics showing the widening of the depletion region under increasing reverse-bias voltage condition. It is possible to appreciate the reducing vertical distance from the generated minority carriers and the depleted region, increasing the generated pairs capture probability from the built-in electric field

We have discussed the general properties of an EBIC measurement, commenting also on the critical parameters to be taken into account: in the next section, we will show the results obtained from the performed characterization.

5.1.2.2 Characterization setup

As we mentioned earlier, our goal with this measurement was to qualitatively map our structure's electronic activity, in order to validate the adopted asymmetric design. In fact, we wanted to be sure that the 2D-PhC waveguide was the area with the higher amount of current flow.

We performed this measurement exploiting a nanoamplifier structure. Firstly, we took an already fabricated sample and removed by RIE the silica encapsulation layer above the 2D-PhC structure, exploiting a selective recipe with respect to gold. In that way, the top metallic pads are accessible for the EBIC probes contacting and the PhC can be properly exposed to the SEM electron beam.

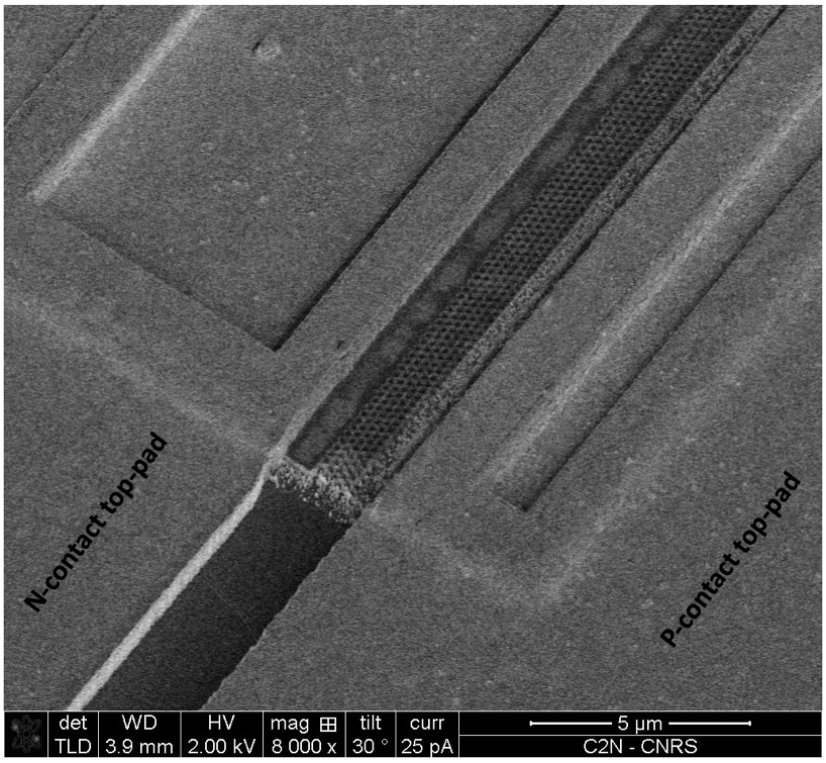


Figure 127: SEM image of the nanoamplifier prepared for the EBIC measurement. The encapsulation layer on top of the PhC pattern was deliberately opened by RIE

We proceeded then with the measurement by placing the DUT inside the SEM chamber and contacting P- and N-contact with the electrical probes. Figure 128 sums up the characterization setup.

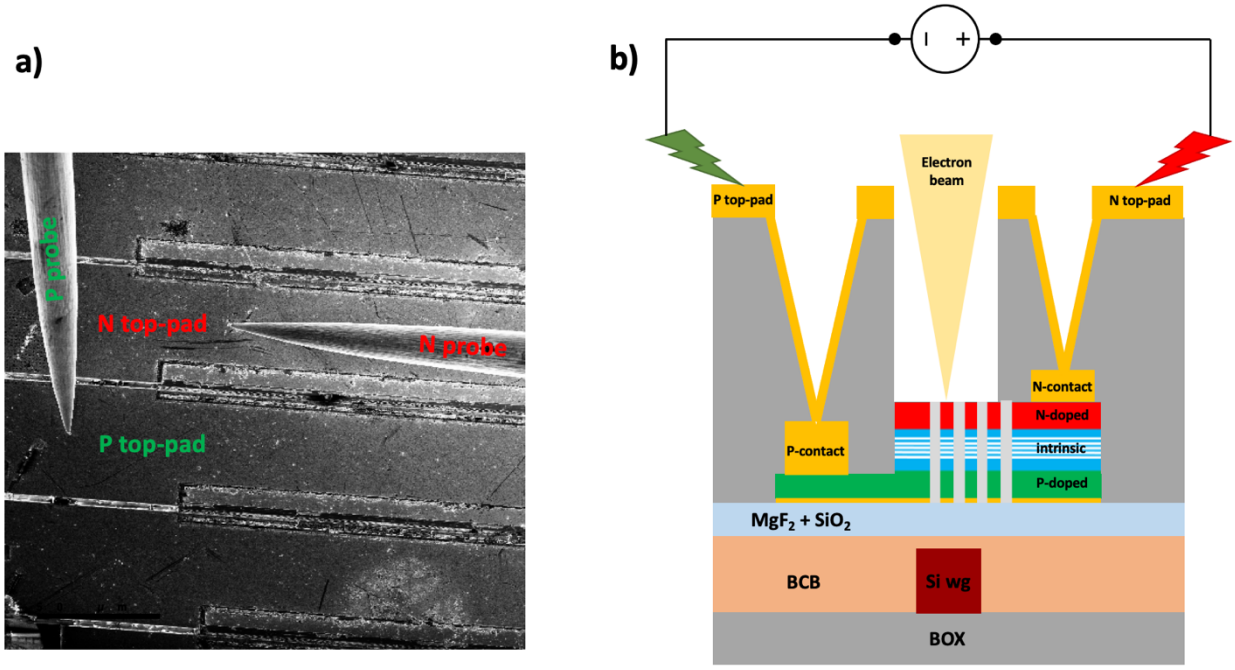


Figure 128: a) SEM top-view of the DUT. We can see the electrical probes contacting the top-pads and a column of nanoamplifiers with different length. b) cross-section schematics of the DUT, highlighting the silica opening for the electron beam bombardment

Considering the thin III-V membrane we worked with, we decided to fix the bias voltage to 0 V, being quite confident that it was sufficient to play with the electron beam acceleration voltage to induce a drift current in our device without the need of enlarging the junction's depletion region. Figure 129 shows the obtained result, for an acceleration voltage of 7 kV and a beam current of 10 µA. The result is extracted in the nanoamplifier's taper region. The EBIC map reveals that the higher amount of induced current is confined inside the PhC waveguide and that the brighter contrast exponentially decreases moving inside the holes pattern. This is a direct consequence of the lateral injection scheme: when electron-hole pairs are excited inside the PhC waveguide, there are more holes contributing to the drift current since they have to cover a shorter path to reach the P-contact. However, when we excite electron-hole pairs inside the PhC pattern, the limited holes mobility as well as the higher resistance characterizing this region make that positive-charge carriers, once separated from the electron constituting the pair by drift, are lost by Joule effect, strongly reducing the amount of induced current. Placing the PhC waveguide in close-proximity to the P-contact is, then, a winning decision: this result suggests, in fact, that when a positive voltage is applied across the diode, positive charge carriers diffuse to the junction's depletion region through the shortest available path to create electron-hole pairs, meaning that, in our devices, the injected current will be mainly concentrated inside the PhC waveguide (or PhC cavity).

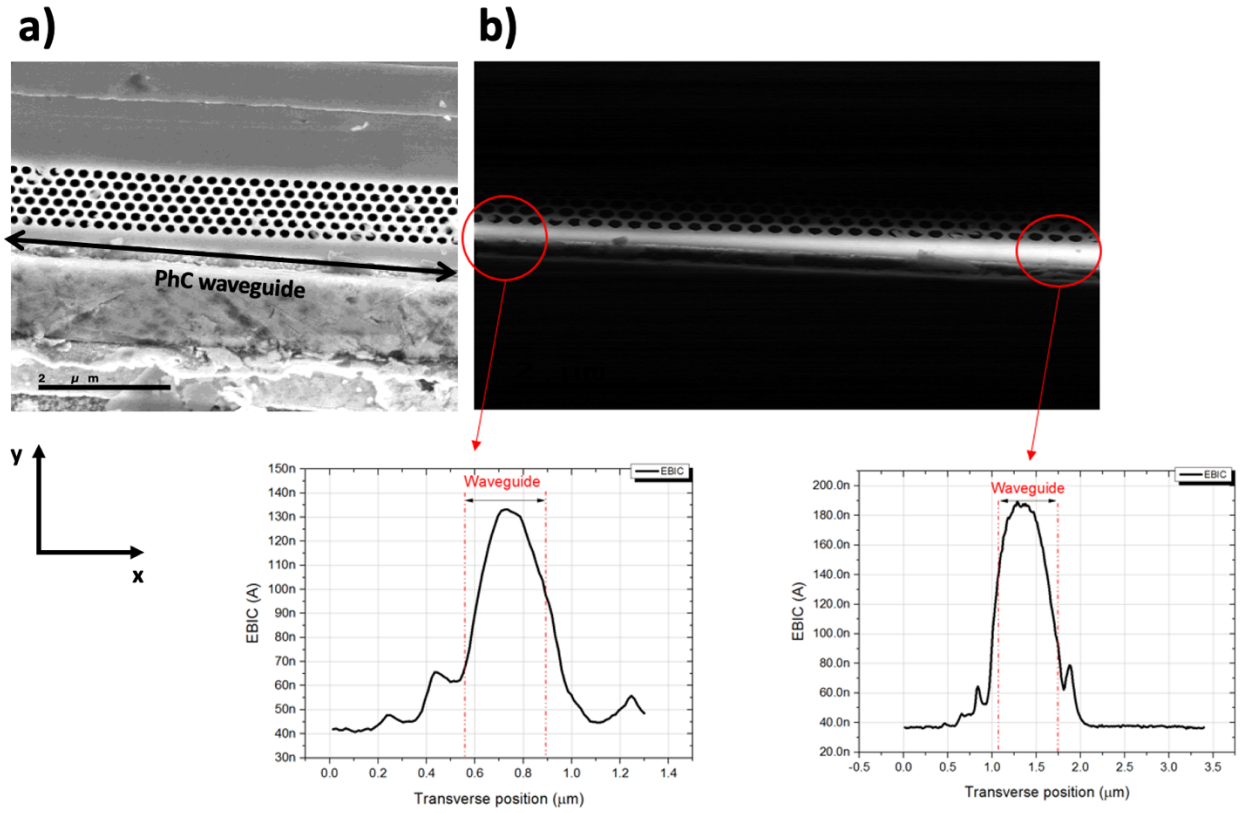


Figure 129: Result of the EBIC characterization for the nanoamplifier structure. a) shows the SEM top-view of the 2D-PhC pattern, while b) the EBIC map. As we can observe, the brighter contrast covers the PhC waveguide, meaning that the higher amount of electronic activity is restricted to the area of interest

To double check this behavior, we made another similar measurement: the tested device this time did not present any PhC pattern, but from an electrical point of view it was designed as the usual P-i-N junction diode we studied during this PhD, with the lateral carriers injection scheme (Figure 130).

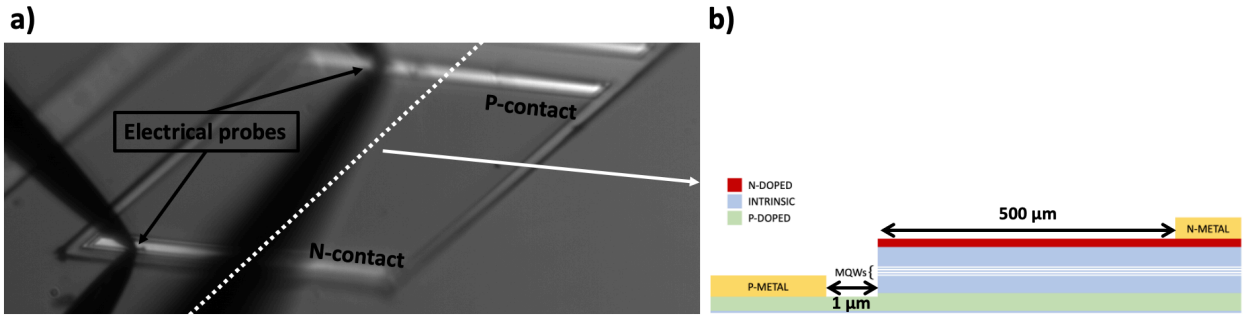


Figure 130: a) 3D-view of the tested P-i-N junction diode; b) cross-section schematics of the DUT

Our goal was to analyze the diode's Electroluminescence (EL) under forward bias condition, to see whether the emitted photons' intensity profile was mainly localized in close proximity to the structure's sidewall. The EL was extracted by mean of an infrared (IR) camera, placed on top of the DUT. Figure 131 shows the experiment's result.

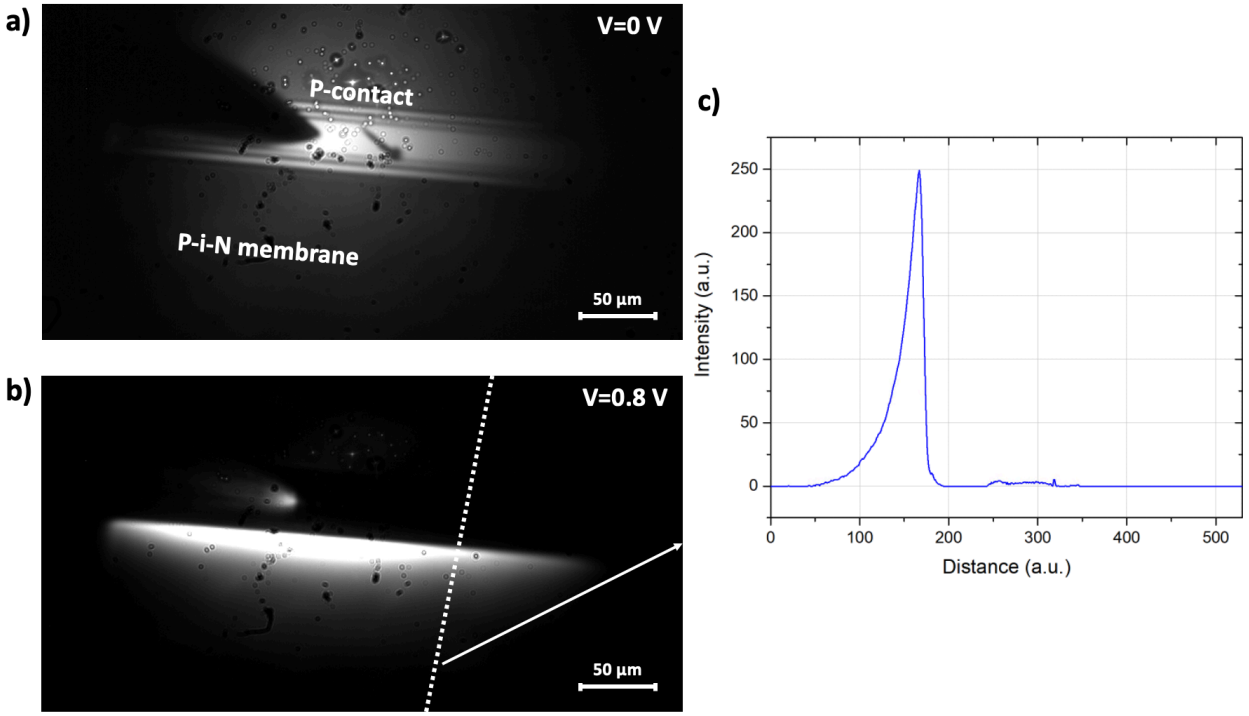


Figure 131: Top-view of the P-i-N diode with a) no bias and b) 0.8 V across the junction, where we can appreciate the EL quite localized in close proximity to the diode's sidewall. In c) we observe the extracted transverse profile, confirming that the emitted photons' intensity do not extend far from the sidewall

The IR camera image was zoomed on the P-contact and the diode's sidewall to better analyze the emitted photons profile. As we can observe, under forward bias condition with 0.8 V applied across the junction, the EL is mainly localized in close proximity to the structure's sidewall. Even though the DUT does not contain the PhC holes pattern, we can see that positive charge carriers only reach the diode's depletion region from the shortest available path, contributing to radiative recombination processes along a transverse length of about 10 µm. This confirms that, adapting this injection scheme to the designed nanodevices, the current flow will be mainly concentrated inside the PhC waveguide (or cavity), as we saw with the EBIC map. The obtained results represent a great milestone, validating our lateral electrical injection scheme appropriately designed for the optimal interaction between the optical signal and the injected electron-hole pairs.

During this section we showed the performed characterization to study the electrical behavior of our structures: we were able to achieve ohmic contacts minimizing their resistivity and we validated the electrical injection scheme for the asymmetric 2D-PhC geometry, fundamental requirements to achieve satisfying performances from the designed optoelectronic devices. In the next sections we will move to the nanolaser characterization, showing firstly its operation under CW optical pumping and then confirming the quality of our electrical injection scheme by analyzing the results when the cavity is electrically driven.

5.2 Nanolaser characterization

After an extensive work improving the technological process flow of the hybrid devices, we performed measurements on the nanolaser structure, which gave us the opportunity to validate their optical as well as electrical design and demonstrate the fabrication quality achieved. The characterized nanolasers were designed as we saw during chapter 3. Moreover, to study the impact of the geometry on their performances, we fabricated nanocavities varying the holes radii (R_{PhC} and R_{base}). The fabrication relied on the final process flow calibration, with inverted levels fabrication and silica encapsulation layer entirely deposited by PECVD. The structures were adhesively bonded onto a silicon substrate using a thick BCB layer (more than 1 µm): in that way, no passive element was coupled to the cavities and we could study their intrinsic behavior by extracting the output signal from the devices top surface.

The following sections are organized as follows: firstly, we will show and comment the structures behavior under CW optical pumping, demonstrating a nice correlation with the theoretical model. Then, we will move to the study of their electro-optic performance under AC and DC biasing, commenting the promising results. We will end-up this chapter by analyzing the dark current behavior as well as the carriers lifetime of the fabricated samples, showing that we still have room for improvements concerning surface passivation.

5.2.1 Nanolaser optical characterization

The adopted characterization setup is schematized in Figure 132. A 1180 nm CW laser diode is used to pump the cavities in order to achieve population inversion by exciting electron-hole pairs inside the MQWs heterostructure. The pump signal is firstly transmitted through a variable attenuator wheel in order to sweep the pump power from low to high values by remotely controlling it. A beam splitter is then adopted to send the pump signal to the sample on one side and to measure its power through an optical power meter on the other side. A dichroic mirror is placed after the beam splitter to reflect the pump laser and inject it in a microscope objective, which in turn plays a double role: focus the pump on the sample surface and collect the structures' surface emission. The latter is eventually sent to a spectrometer equipped with linear array of InGaAs detectors (passing through the dichroic mirror without being filtered out), in

order to analyze the cavities' emission spectrum. The characterization was performed at room temperature.

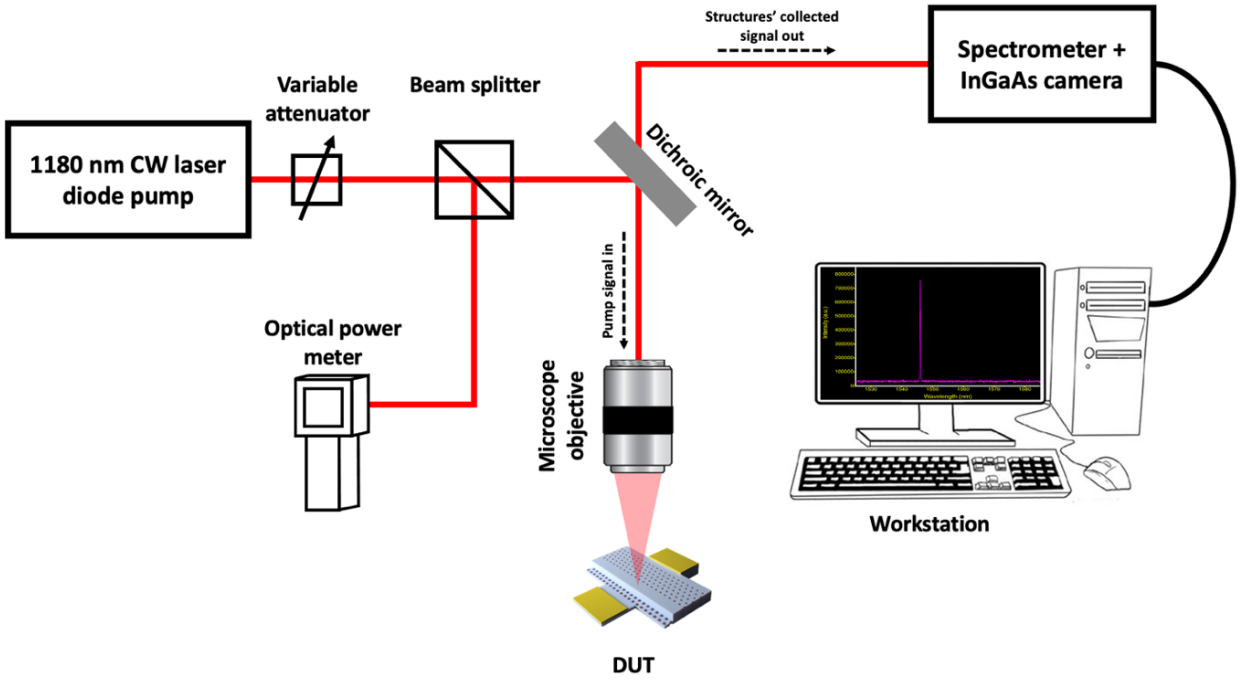


Figure 132: Schematic model of the adopted setup for the nanolasers optical characterization

Thanks to this setup, we could sweep the pump power (measured step by step from the optical power meter) and extract the resulting emission spectra, to evaluate the nanocavities behavior.

The extracted results are in good agreement with the nanolaser modeling: Figure 133 shows an example of the emission spectrum evolution under different bias powers for a structure presenting the same parameters as the reference cavity of chapter 3 ($a = 333\ nm$, $R_{PhC} = 72\ nm$, PhC cavity width $= 0.9 \cdot a\sqrt{3} = 519.1\ nm$, with 3 rows of holes in the base with radius $R_{base} = 100\ nm$). What we can immediately notice is that, as expected from the design, the laser shows a single-mode behavior: this validates our theoretical model for the Gaussian apodization and the choice we made fixing the FWHM to 3 µm and the minimum cavity width W_{min} to 506.1 nm, providing a high-Q cavity avoiding higher order modes excitation. Additionally, from 133-a), we can observe the typical sub-threshold resonance wavelength blue-shift of a laser cavity: this is due to the fact that, as we saw during chapter 3, the more bias power we inject inside the cavity the higher the carrier concentration becomes, reaching the maximum value at the laser threshold and remaining constant in the lasing regime. The higher amount of carriers inside the

cavity slightly changes the cavity's effective index, causing a blue-shift of the resonance wavelength.

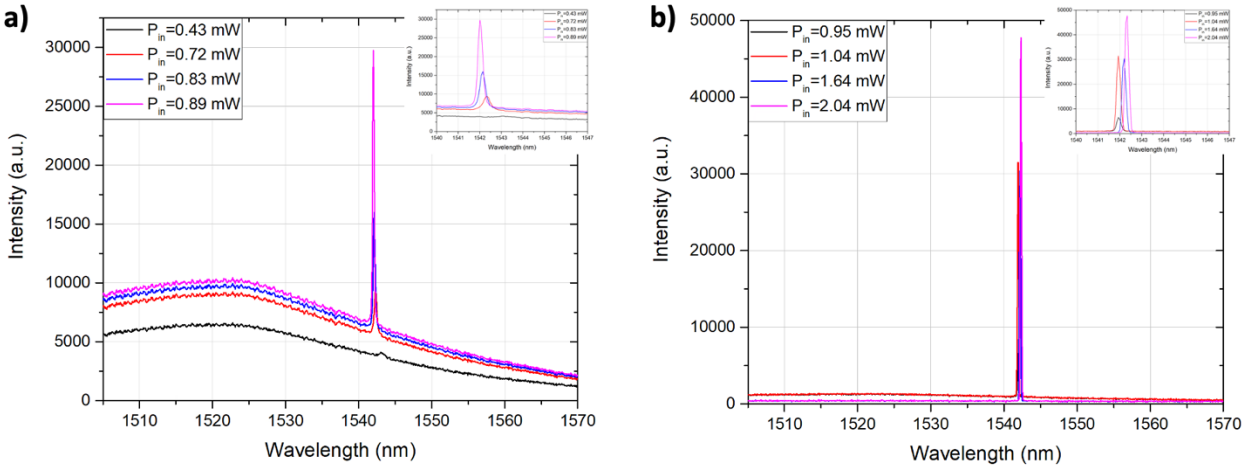


Figure 133: Spectrum evolution for the selected cavity under different pump powers a) below laser threshold and b) above laser threshold. The power P_{in} depicted in the legends refers to the power focused on the sample surface

However, if we keep increasing the pump power, the resonance goes through a red-shift (133-b)): this is the consequence of the heat accumulated around the structure due to a higher pump power, meaning that our system does not completely evacuate the accumulated heat. Such an effect might be due to a couple of reasons:

- Firstly, we remind that after the holes etching the adopted HSQ mask was not removed; considering that HSQ is a bad thermal conductor, the heat is less efficiently dissipated.
- Secondly, the cavities were encapsulated exploiting silica deposited by PECVD as an encapsulation layer: as seen during chapter 4, this deposition method does not allow to completely fill the PhC holes with SiO_2, leaving air bubbles inside them. Another time, the presence of air instead of silica reduces heat dissipation.

We can observe these effects more clearly on Figure 134. Together with the resonant wavelength, Figure 134-b) shows the resonance peak linewidth variation: it decreases below laser threshold and then it stabilizes once the laser threshold is overcome. This measurement is here limited the spectrometer resolution. In Figure 134-a) we can appreciate the typical S-curve obtained from a lasing structure: the output signal rapidly increases around the laser threshold (located at the curve's inflection point) and once in lasing regime it keeps growing linearly.

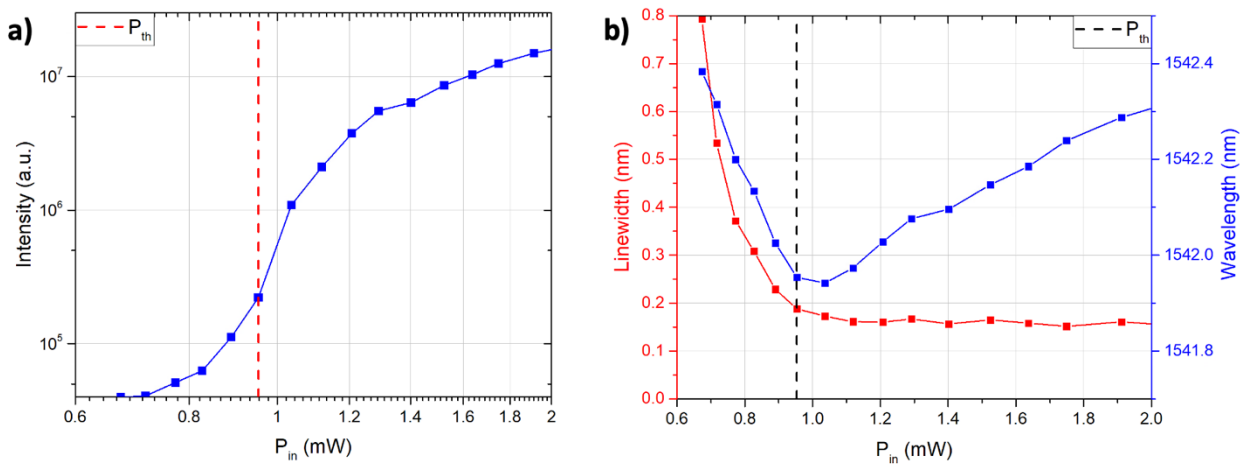


Figure 134: a) laser output power, b) linewidth (red curve) and resonance wavelength (blue curve) variation as a function of the pump power

We have also performed the same measurements on cavities with different R_{PhC} and R_{base}, to observe the laser threshold and the resonance wavelength variation: the results are reported in Figure 135. From Figure 135-a), we can observe the threshold powers as a function of the characterized cavities geometrical parameters. It is quite difficult to deduce something from this graph, since the threshold power varies differently for each R_{base}: in fact, when the R_{base} is 80 nm we can notice that the threshold diminishes by increasing R_{PhC}, while for R_{base} of 100 nm and 105 nm it goes on the opposite way. The extracted results are highly dependent on the pump alignment on top of each structure: considering that the cavity have dimensions of 5.44 µm longitudinally and 519.1 nm transversally, while the spot size of the pump laser on the DUT is of the order of 5 µm, it is hard to be completely sure that each nanolaser was characterized precisely under the same alignment conditions. Additionally, we must consider that a different pump focalization on top of the cavities changes the photons absorption efficiency from the active layer, consequently varying the real pump power exciting carriers inside the MQWs heterostructure. Anyway, our goal with this characterization was not to analyze the threshold power variation, but rather to check whether the designed devices were actually working as single-mode nanocavities and at which wavelength they were emitting. As already mentioned at the beginning of chapter 3, during our work we noticed a resonance wavelength difference of about 45 nm between the nanolaser model and the fabricated structure. Considering that we were targeting nanolasers emitting around 1550 nm, we chose to design the apodized cavity fixing its resonance wavelength at around 1590 nm. Our choice is justified if we look at Figure 134-b), where the structure with same geometrical parameters as the modeled reference cavity presents a resonance wavelength of 1542 nm.

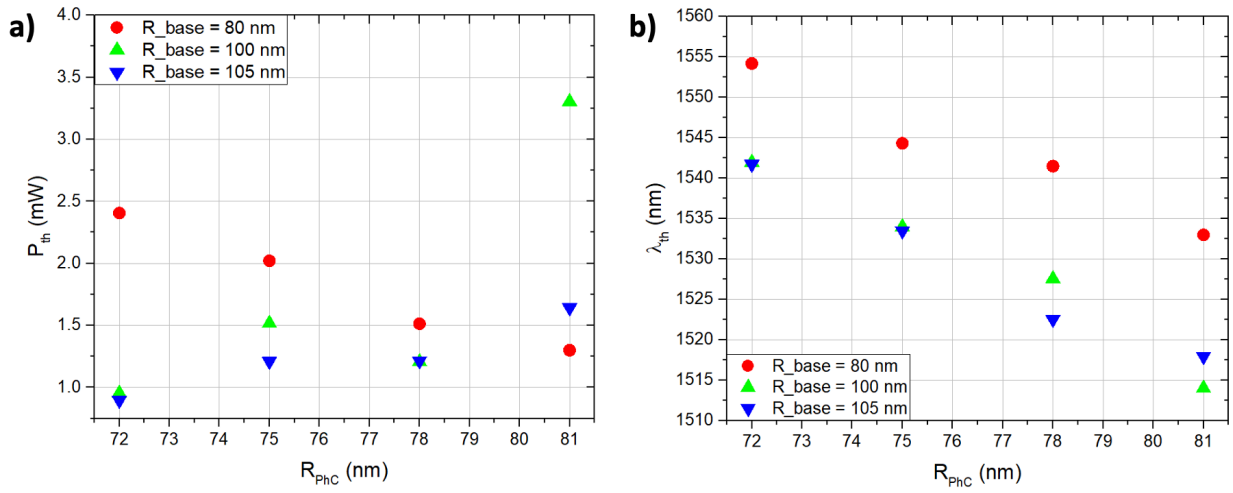


Figure 135: a) laser threshold and b) resonance wavelength variation for different R_{PhC} and R_{base}

If we now observe Figure 135-b), we can appreciate how the laser's emitting wavelength varies as a function of R_{PhC}. Fixing R_{PhC} at 78 nm, for example, we can see that by increasing R_{base} the resonance wavelength undergoes a blue-shift. The same happens by fixing R_{base} and increasing R_{PhC}.

The characterization of our structures in CW optical pumping gave us satisfying results: it validated our optical design as well as the technological quality achieved with our process flow, demonstrating the cavities' single-mode behavior while obtaining information on the resonance wavelength variation as a function of the holes dimension. This characterization also allowed us to highlight the limited heat dissipation efficiency: the presence of HSQ on top of the nanolasers surely contributes to that effect, due to its low thermal conduction. Additionally, we have observed that HSQ deteriorates the cavities behavior not only from a thermal point of view, but also from an electrical one. Before moving to the structures' electro-optical characterization, in the following sub-section we will analyze and comment the HSQ impact on the device's electrical behavior.

5.2.2 HSQ impact

As seen during chapter 4, HSQ might be thought as a good solution to encapsulate our devices since it allows to entirely fill the PhC holes, guaranteeing at the same time useful encapsulation layer planarization and presenting almost-zero optical losses. On the other hand, the previous section highlighted how its presence on top of our 2D-PhC nanolasers impacts heat sinking: we recall, in fact, that the HSQ hard mask exploited for the holes drilling is not removed to avoid attacking the silica underneath the devices, which would cause the structures' base to collapse.

In this sub-section, we will show the characterization performed on devices fully encapsulated in HSQ, replacing the silica layer deposited by PECVD by HSQ spin-coated on the sample and successively baked at moderate temperature to strengthen its crystalline structure. By optically pumping these cavities, we could observe, like in the previous subsection, a nice single-mode behavior, the only remarkable variation being the ~ 40 nm red-shift resonant wavelengths went through. However, under electrical biasing (both AC and DC) the story is different: even though we could measure a current flow by applying a bias voltage across the nanolasers, no light scattering was observable from their top-surface with the IR camera, meaning that no radiative recombination mechanisms (or a very small amount of them) were taking place inside the MQWs. We assumed the presence of a current leakage, detrimental for the correct functioning of the devices. The HSQ turned out to be the source of such a leakage: in order to understand it, we compared the P-i-N junction diode electrical behavior for the reference cavity of chapter 3 under different fabrication conditions, aiming at the progressive insulation of the HSQ from the metallic contacts:

1) cavity fully encapsulated inside HSQ;
2) cavity encapsulated inside SiO2 by PECVD, with the HSQ hard mask on the top-surface;
3) cavity same as 2) but with the presence of a trench inside the encapsulation layer close to the N-contact, abruptly interrupting the HSQ connection between P- and N-metals;
4) cavity same as 2) but with an additional PECVD silica deposition right after the vias opening, completely preventing the HSQ from contacting the metals or the semiconductor.

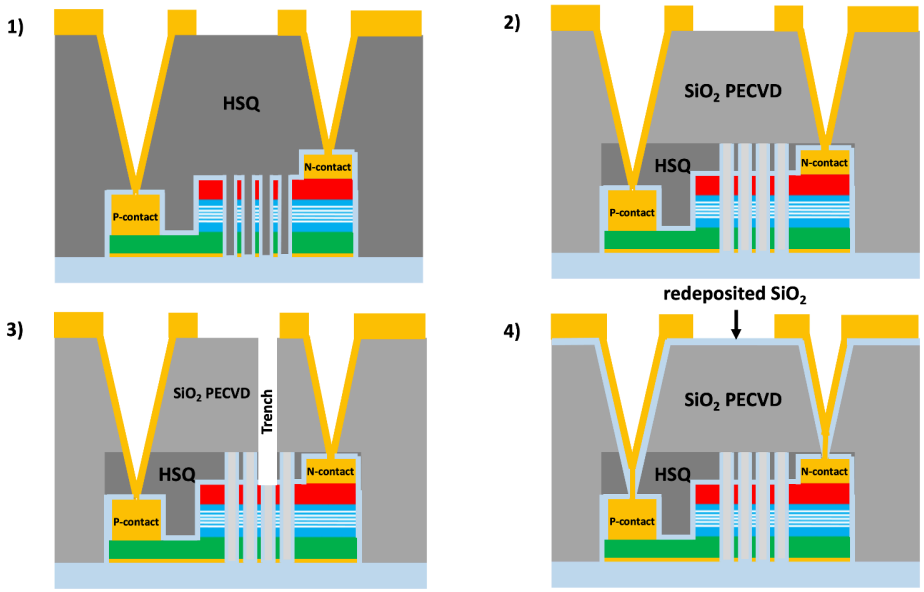


Figure 136: Cross-section schematics of the four tested configurations, showing a progressive HSQ isolation from case 1) (HSQ contacting both metals) to case 4) (HSQ fully isolated from semiconductor and metals)

Figure 136 schematizes the four studied cases. In 1), the semiconductor is insulated from the HSQ thanks to a thin silica layer deposited by PECVD in two steps: the first one prior to the spin coating of HSQ used as a hard mask (deposited on the top-surface of the half-rib structure), while the second one before the spin coating of HSQ used to encapsulate the structures (deposited on the PhC holes' sidewalls). In all other cases, only the first PECVD silica deposition is necessary to insulate the III-V from the HSQ, since the encapsulation layer is entirely composed by PECVD silica without any HSQ addition. However, in cases 1) to 3), the HSQ is always in contact with the metals: in configuration 1) the encapsulation layer is fully made of HSQ, in contact with both P- and N-metal in the vias and under the top pads; in case 2) and 3) the HSQ hard mask only touches the metal deposited in the vias. Additionally, in case 3) we opened a trench in the encapsulation layer, etching it down to the semiconductor in order to break the eventual connection between P- and N-metal through HSQ. Case 4) does not allow any contact between metals and HSQ, since after the via opening another step of silica deposition by PECVD is performed to fully insulate the HSQ hard mask. Figure 137 shows the measured I-V curves for the four studied cases.

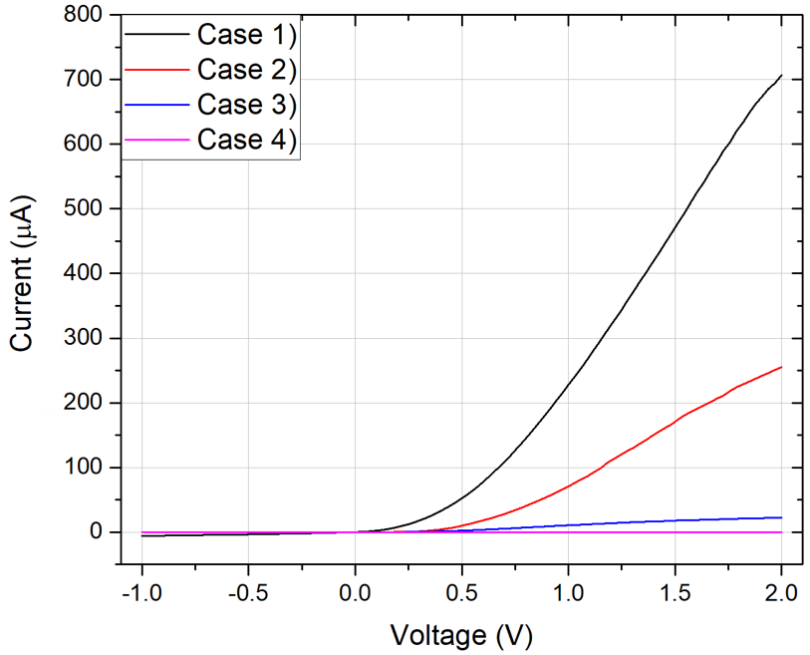


Figure 137: I-V curves for the studied cases. It is remarkable that the more we reduce the HSQ area in contact with the metals the smaller the current gets, meaning that HSQ is actually a source of current leakage

The plot clearly highlights the HSQ's progressive insulation effect: from case 1) to case 4) the measured current drops from hundreds of µA to almost-zero, meaning that almost all the current measured in 1) is leaked from the metals inside the HSQ. The leaking of this current can also be understood by observing the diode threshold voltage of the black curve, corresponding to ~ 0.5 V: such a threshold is very low considering the structure and the materials we work with, which should instead present a diode threshold voltage around 1 V, as we observed from the cavity's

simulated electrical behavior during chapter 3 and as we will see later during the I-V curves characterization. Another important information we gain from this characterization is that R_{base} of 100 nm is too big to allow carrier injection inside the PhC cavity's active area: in case 4), where the HSQ is fully isolated from the metals and the semiconductor, the current inside the semiconductor is very low, on the order of the nA. There might be two explanations for that effect:

- Firstly, the portion of available III-V material in the base might be too small to allow carrier diffusion through the holes pattern. Moreover, this effect could be emphasized due to Fermi level pinning in the middle of the gap at the holes sidewalls, caused by surface defects created by the ICP dry etching process: this turns into the appearance of an electrically insulating region (i.e., a depleted region) around the drilled holes, increasing their effective electrical size more than their physical size [119-120] and thus limiting the amount of positive-charge carriers reaching the junction's depletion region inside the PhC cavity. This might tell us that the surface passivation step we perform during fabrication to counteract surface effects is not efficient enough, as we will discuss during the last section of this chapter.
- Alternatively, the small hole-to-hole distance might render the base very fragile, getting damaged during one of the technological steps after the holes drilling and disconnecting the higher part of it from the 2D-PhC sidewall.

Thanks to this characterization we understood that the HSQ is a bad choice as an encapsulating material, since, if placed in contact with the metals, it causes current leakage; additionally, it is a bad thermal conductor. As a consequence of all these considerations, for the cavities electro-optical characterization the DUT were fabricated as in case 4), where the structures are encapsulated using PECVD silica and the HSQ hard mask is insulated from the metals through another silica deposition right after the vias opening. In the next section, we will analyze the performed measurements.

5.2.3 Electro-optical characterization

After the nanolasers' characterization under optical pumping and after the final fabrication optimization following the study of the HSQ impact, we moved to the electro-optical characterization of the designed devices. During this section, we will focus our attention on two samples differing from each other just for one fabrication step: the ICP passivation layer removal. As we said during the ICP etching subsection of chapter 4, a silicon-rich silica passivation layer is formed during the III-V etching process, protecting the drilled holes surface. Consequently, before proceeding with the III-V surface passivation with ammonium sulfide, we have to remove this silica layer that prevents the proper deposition of sulfur atoms to annihilate surface dangling

bonds. We performed the ICP passivation layer removal in two different ways, so to analyze the efficiency of each process:

- by dry etching, using unaccelerated SF_6 plasma etching (presenting high etch-rate for silicon);
- by wet etching, dipping the sample in a BOE solution for few seconds to avoid the silica layer underneath the III-V devices undercut, preventing the base to collapse and break (Figure 105 during chapter 4).

We will refer to these samples, respectively, as to “Sample dry” and “Sample wet”.

The signal collection is performed in the same way as for the optical pumping measurements, but this time the structures are electrically biased. In the following sub-sections, we will have a look at the nanolasers’ behavior firstly under AC bias and then under a DC bias.

5.2.3.1 AC electrical injection

Figure 138 schematizes the adopted setup.

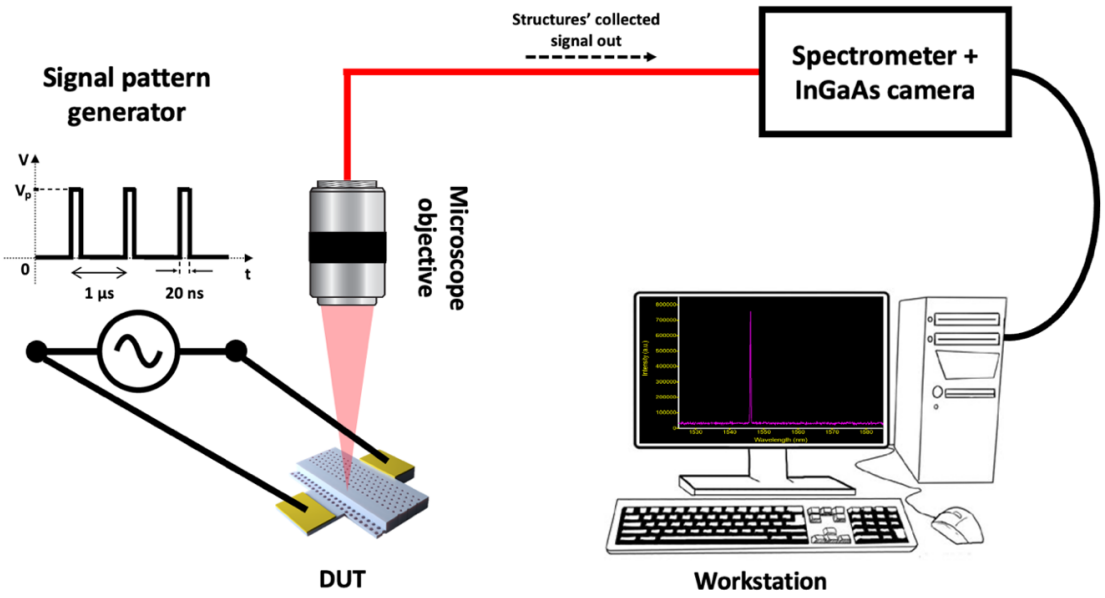


Figure 138: Schematic model of the adopted setup for the cavities’ AC electro-optical characterization

The potential difference across the structures is applied thanks to a signal pattern generator, where we define the voltage pulses length, intensity and frequency to bias the cavities. The adopted signal is a square wave, with 20 ns long pulses at a frequency of 1 MHz; their peak-to-peak amplitude is fixed between 0 V and the peak voltage V_p. This way of biasing is optimal to

pump the nanolaser without heating, as thermal diffusion time is of the order of 1 µs [126]. The emitted light signal is then collected from the sample's surface through the same microscope objective exploited during the optical characterization and sent to the spectrometer, in order to analyze the resulting spectrum from the DUT. Another time, the measurements are performed at room temperature.

Single mode laser emission is observed from the characterized structures, but this time only from cavities presenting holes in the base with radius of 70 nm, apart from two exceptions of "Sample wet" with radius of 80 nm. Figure 139 shows an example of the spectrum evolution for a cavity of "Sample wet" presenting the following parameters: $a = 333\ \mathrm{nm}$, $R_{PhC} = 81\ \mathrm{nm}$, PhC cavity width $= 0.9 \cdot a\sqrt{3} = 519.1\ \mathrm{nm}$, with 3 rows of holes in the base with radius $R_{base} = 70\ \mathrm{nm}$.

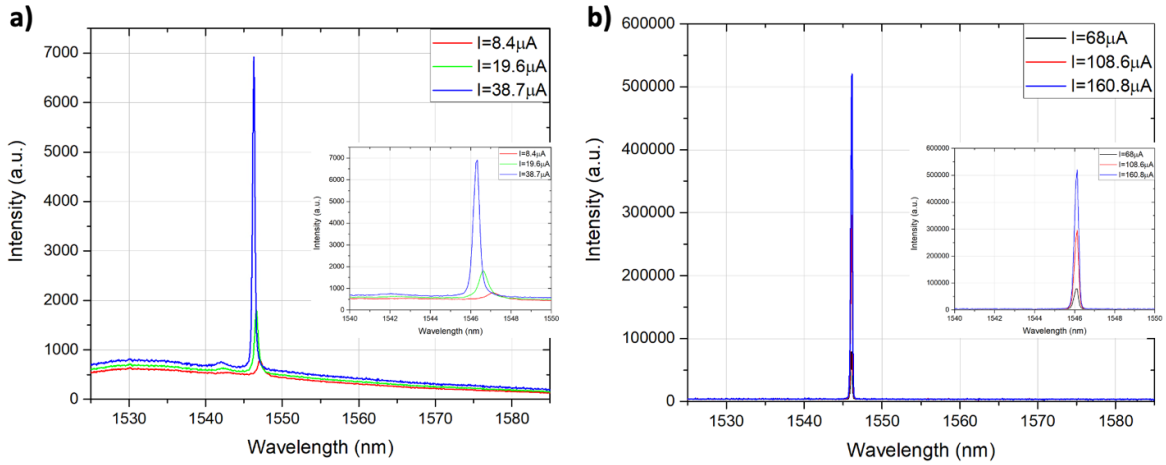


Figure 139: Spectrum evolution for the selected cavity under different amounts of injected current a) below laser threshold and b) above laser threshold. The insets show a close-up view around the resonance peaks

Below threshold, we can clearly observe the typical resonance blue-shift due to electrical carrier injection inside the active region. This time, however, in the lasing regime, the resonance peak does not red-shift contrarily to what was seen under CW optical pumping, where we could clearly observe a wavelength red-shift. This is directly due to the adopted biasing mechanism: in fact, the voltage pulses frequency is 1 MHz, which is of the same order of magnitude of the thermal relaxation time constant for the adopted materials. In that way, between one pulse and the other, the system is able to evacuate the heat produced by non-radiative recombination events more efficiently than in the CW optical pumping configuration, stabilizing the resonance wavelength once the laser threshold reached. Figure 140 shows the selected structure's S-curve and the wavelength as well as the linewidth variation as a function of the injected current.

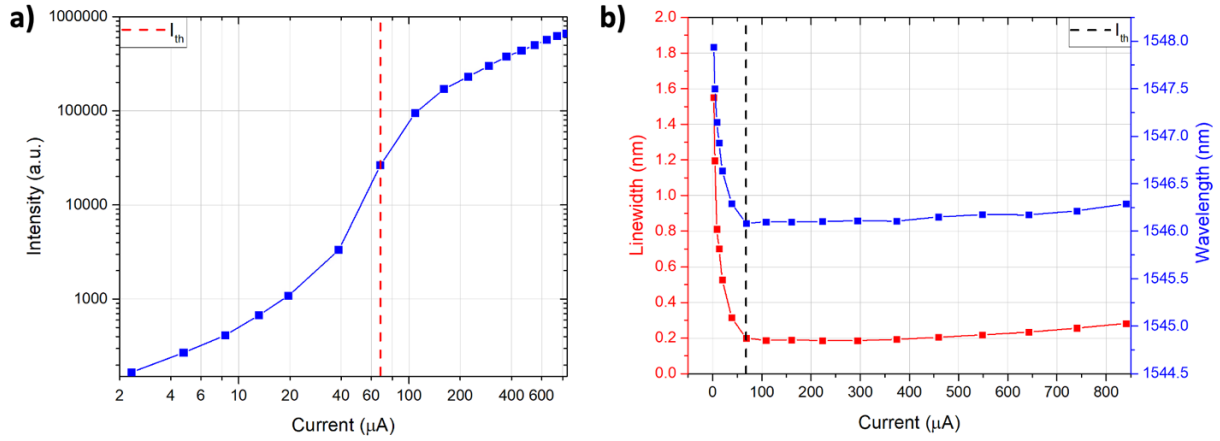


Figure 140: a) Selected cavity's S-curve characteristic, b) linewidth (red curve) and resonance wavelength (blue curve) variation as a function of the injected current

The laser threshold is achieved for an injected current of around 68 µA at 1V applied across the P-i-N junction, corresponding to a threshold power of 68 µW. Such a low power value confirms that the designed cavities are suitable for integrated circuits low power applications.

The same measurements were performed on cavities presenting different R_{PhC}, both for "Sample wet" and "Sample dry". We can analyze the laser threshold variation from Figure 141. We can immediately notice that, for R_{base} of 70 nm, "Sample wet" presents lower threshold than "Sample dry". Additionally, for "Sample wet", the threshold current is almost constant as a function of R_{base} and R_{PhC}, around 75 µA. On the other hand, for "Sample dry", I_{th} steeply increases with R_{PhC}. For R_{base} of 80 nm, laser emission was only observed for "Sample wet" (R_{PhC} of 75 nm and 81 nm) with current thresholds comparable to the case where R_{base} = 70 nm. From all these results, we can deduce that the sidewalls passivation is more efficient for "Sample wet" than for "Sample dry". Let us firstly focus our attention on "Sample dry": the fact that the threshold diminishes by reducing R_{PhC} means that the holes sidewalls are sources of non-radiative recombination centers. The more we increase their dimension, the higher the carriers capture rate from trap states is and, consequently, more current is needed to provide electrical carriers for radiative recombination, in order to achieve the required modal gain. The situation is highly improved on "Sample wet": varying R_{PhC}, the laser threshold remains stable at values around 75 µA, which is moreover smaller than all the plotted threshold current values of "Sample dry". This indicates that the ICP silica passivation layer removal is more efficient with the BOE wet etching than with dry etching.

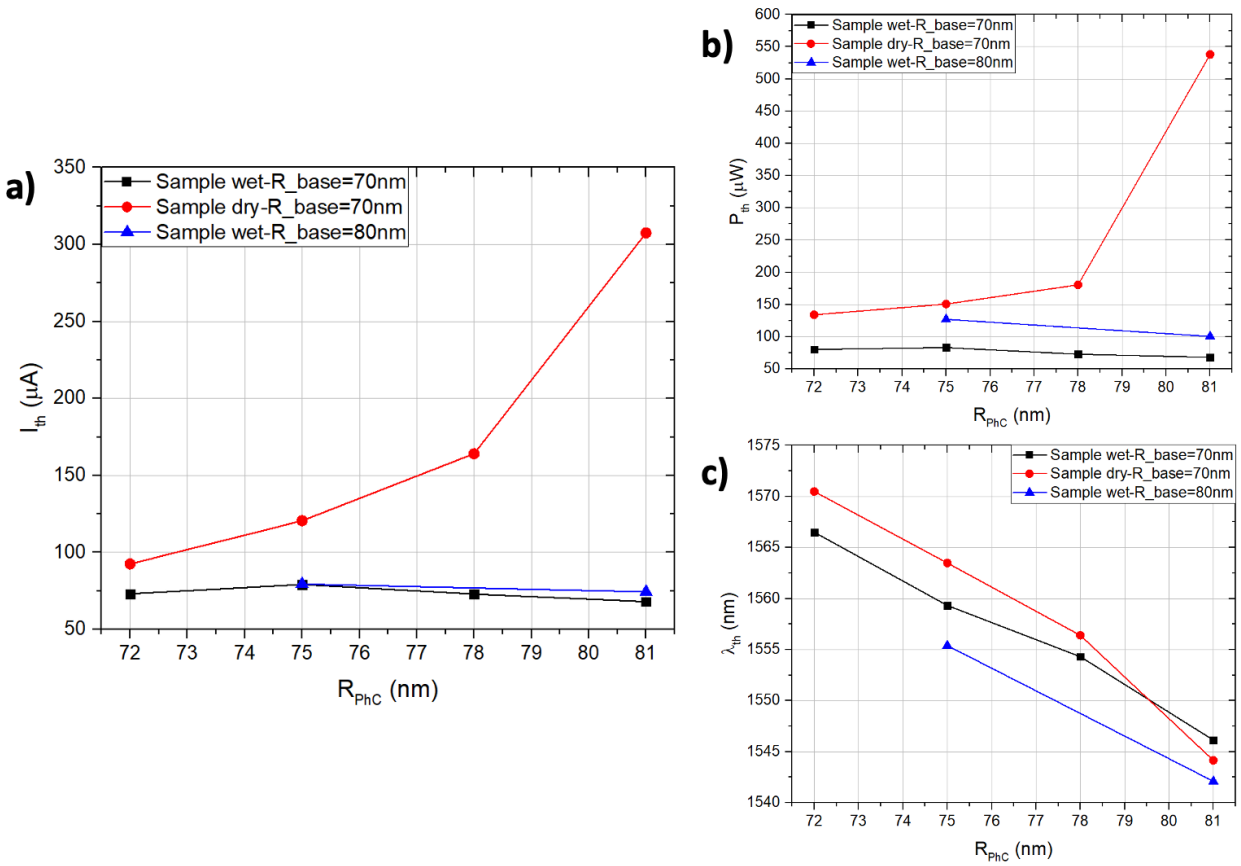


Figure 141: Threshold a) current, b) power and c) wavelength as a function of R_{PhC} and R_{base} for the two characterized samples

This is also demonstrated by the fact that we are able to observe laser emission for structures with R_{base} of 80 nm fabricated on "Sample wet", and not on "Sample dry": we attribute this to the fact that the large amount of surface recombination in "Sample dry" induces a depleted region around the holes of the base (as we have already discussed during the HSQ impact section) rendering the whole structure more resistive. As a consequence, the bias voltage to apply to inject sufficient current inside the active region to reach the laser threshold is so high that it causes damage to the III-V structure. On the other hand, the same PhC base on "Sample wet" is less resistive and allows to achieve laser emission. Moreover, looking at the threshold power (Figure 141-b)), we can see that the amount of power to provide to the cavities is higher for R_{base} of 80 nm case compared to the 70 nm one, even though the threshold currents are very close. Another time, the bigger holes introduce a higher resistance, requiring a higher voltage to obtain the same current flow inside the device. For the same reason, cavities presenting bigger R_{base} (90 nm and 100 nm) do not show any lasing behavior under an electrical bias.

We consider these results as an important achievement, since we demonstrated electrically driven nanocavities presenting ultra-low threshold current independently from R_{base}. The reason why no significant threshold difference was observed in devices with R_{base} of 70 nm and 80 nm can be explained by considering that our structures contain quite highly-doped layers, introducing optical loss by free-carriers absorption. As we saw from the optical simulations during chapter 3, such a loss mechanism limits the total Q-factor, modifying the Q_{tot} relation as follows:

$$\frac{1}{Q_{tot}} = \frac{1}{Q_0} + \frac{1}{Q_{fc}} \tag{5.3}$$

Q_0 being the intrinsic Q-factor and Q_{fc} the additional term accounting for free-carriers absorption. As a matter of fact, doping introduces a predominant loss effect on these nanostructures, rendering the total Q-factor for cavities with different R_{base} (and consequently different Q_0) comparable.

After characterizing the nanocavities under AC biasing, we moved to the analysis of their response under a DC pumping. In the next section, we will discuss the obtained results.

5.2.3.2 DC electrical injection

The setup is identical to the AC characterization, the only difference relying on the utilization of a source meter providing a DC bias to the DUT (Figure 142).

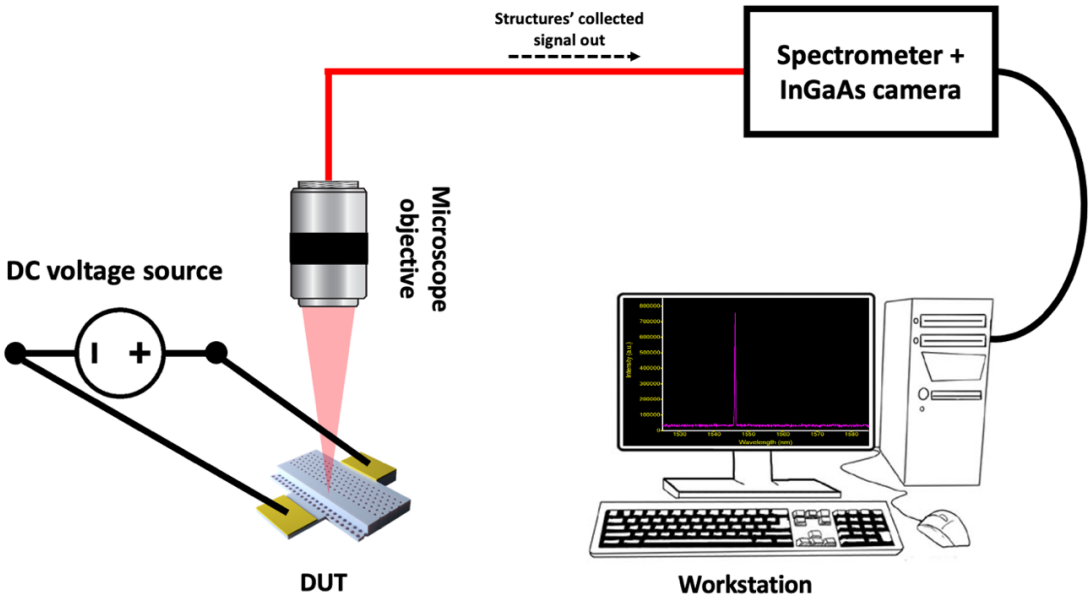


Figure 142: Schematic model of the adopted setup for the cavities' DC electro-optical characterization

This time, however, the lasing regime was not observed with any of the characterized cavities, neither from "Sample dry" nor from "Sample wet". This behavior was again attributed to non-radiative surface recombination where carriers are lost releasing phonons, which in turn contribute to accumulate heat around the nanocavity. When the temperature in close proximity to the device grows, non-radiative events tend to increase, since the accumulated heat makes additional electron-hole pairs recombine another time releasing energy in the form of phonons, continuing to heat up the structure. Consequently, the fraction of carriers involved in radiative recombination mechanisms is less and less important, reducing the material gain. While no "interesting" spectrum was extracted from cavities of "Sample dry", from few structures of "Sample wet" we could observe the appearance of the resonance peak, even though its intensity was just slightly higher than the Amplified Spontaneous Emission (ASE) of the MQWs. Figure 143 shows the spectrum evolution for different amounts of injected current under a DC bias voltage for a cavity fabricated on "Sample wet" with the following parameters: $a = 333\ \mathrm{nm}$, $R_{PhC} = 78\ \mathrm{nm}$, PhC cavity width $= 0.9 \cdot a\sqrt{3} = 519.1\ \mathrm{nm}$, with 3 rows of holes in the base with radius $R_{base} = 70\ \mathrm{nm}$.

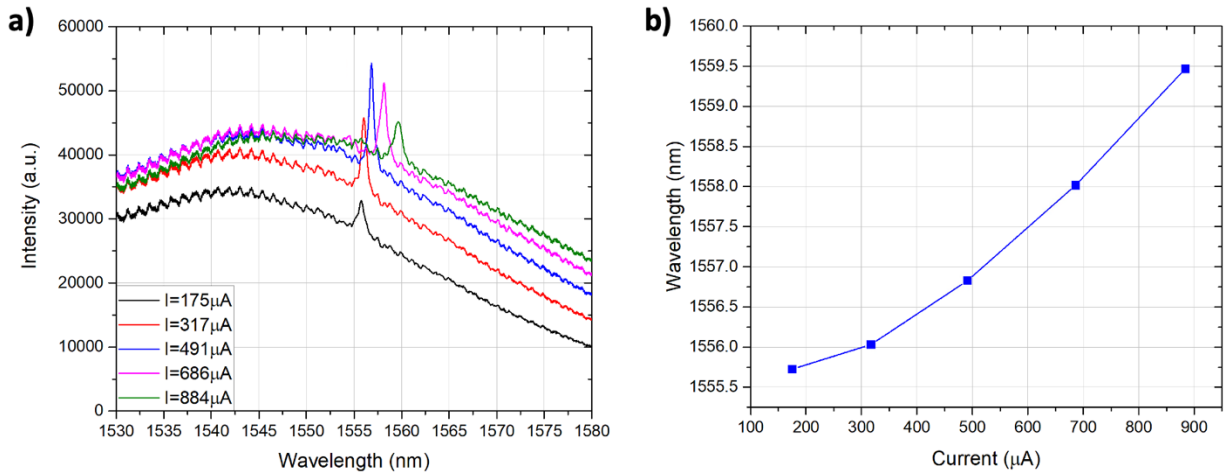


Figure 143: a) spectrum evolution for different amounts of injected currents under a DC bias voltage for the selected nanocavity and b) resonance peak wavelength variation

It is clear that the lasing regime is not achieved, since the signal-to-noise (S/N) ratio is very close to 1 for all the represented cases. Additionally, we cannot observe any resonance blue-shift but a continuous red-shift while increasing the injected current (Figure 143-b)). Also, increasing the current, the S/N ratio approaches more and more 1, meaning that the material gain reduces as a consequence of the increasing non-radiative recombination processes.

This result suggests that, even though the passivation on "Sample wet" is more efficient than on "Sample dry, it still has to be improved. In order to reinforce our conviction about the fact that our performances were limited by the holes sidewalls passivation, we performed two additional characterizations:

- Firstly, we measured and compared the I-V diode characteristics of different nanostructures from "Sample dry" and "Sample wet", confirming that the ICP silica layer removal was much more efficient by dipping the sample inside a BOE solution.
- Secondly, we measured the electrical carrier lifetime from a cavity of "Sample wet" and compared it to the one extracted from an unprocessed piece of the same III-V material, showing that there is still room for the passivation improvement.

5.2.4 IV characteristics comparison

The goal of this characterization was to compare the current flowing inside our nanostructures with the same geometrical parameters fabricated on "Sample dry" and "Sample wet" both in forward and reverse bias condition. While the forward current comparison was mainly highlighting the resistive behavior introduced by the holes drilled in the PhC base, the reverse one was extremely useful to underline the presence of surface trap states inside the PhC pattern. We can say, in fact, that the total reverse current contribution can be divided into the following components [121]:

$$I_{rev} = I_{drift} + I_{B2B} + I_{GR} + I_{TAT} \tag{5.4}$$

Where I_{drift} is the minority carriers current, induced by the inner electric field established inside the junction's depletion region, I_{B2B} is the band-to-band tunneling current, induced by electrons tunneling from the valence band to the conduction band when their energy is close enough (typically under strong reverse bias conditions), I_{GR} is the generation-recombination current, caused by generation-recombination mechanisms inside the depletion region and I_{TAT} is the Trap-Assisted Tunneling current, caused by carriers tunneling mechanisms from the valence band to the conduction band with the assistance of a trap state situated between initial and final energy state. Additionally, I_{TAT} is composed by the contribution of I_{SRH} (Shockley-Read-Hall current), where the trap states are created from defects in the semiconductor's crystal lattice, and I_{SURF} (surface states current), where the trap energy states are originated from surface defects and dangling bonds. Considering that "Sample dry" and "Sample wet" are fabricated in the exact same way, exploiting the same III-V membrane and differing from each other only for the ICP silica passivation layer removal, we can assume that all the reverse current components are equal in both samples except for I_{SURF}, since the passivation mechanism was performed in a slightly different way. Comparing the reverse current of structures with same geometrical parameters fabricated on the two samples, we can understand which silica removal process is more efficient: the higher the reverse current is, the more surface trap states are present and

consequently the less efficient the silica layer removal is (causing a poor sulfur atoms adhesion on the holes sidewalls to annihilate defects and dangling bonds).

We proceeded firstly with the forward current comparison. The setup just consists in a source meter used to electrically bias the 2D-PhC nanolasers, where the applied voltage is swept from -1 V to 2 V and the resulting current is measured and saved. Figure 144 shows the comparison for three R_{base} cases (70 nm, 80 nm and 90 nm) fixing R_{PhC} to 81 nm, a to 333 nm and the PhC cavity width to 519.1 nm.

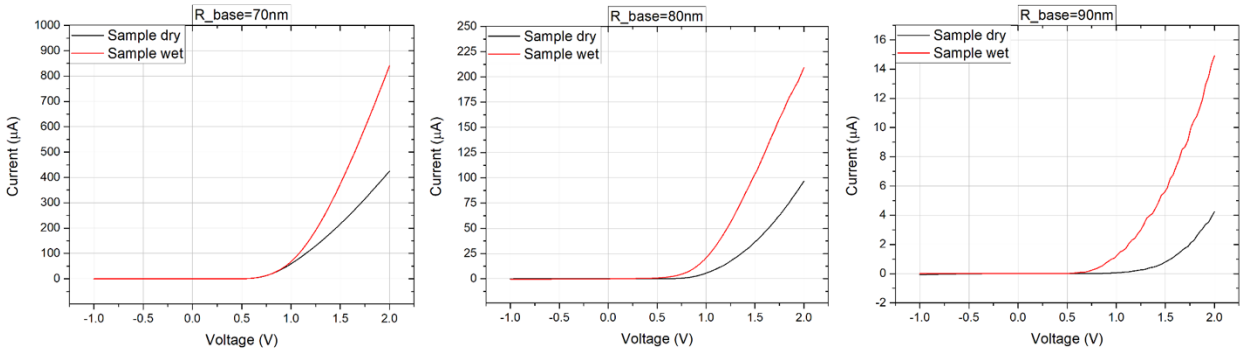


Figure 144: I-V diode characteristics variation as a function of the selected sample and R_{base}

The structures fabricated on “Sample wet” show a less resistive behavior compared to the analogue devices on “Sample dry”. This behavior mainly comes from the holes in the base’s passivation: in fact, we already discussed that the holes tend to create an insulating charge region around them, increasing their effective electrical size compared to their physical one. The only way to counteract this effect is the holes sidewalls’ passivation: the more their passivation is efficient, the closer their effective electrical size will be compared to their real dimension and the less resistive the structure will be. That depletion region around the holes is created not only around the holes in the base, but also the PhC ones: however, considering the much higher electron mobility compared to electrical holes and considering that the PhC holes pattern is mainly crossed by electrons (diffusing from the N-contact through to the PhC cavity) while the diffusion through the holes in the base is only done by low-mobility positive-charge carriers, we can state that the most important resistive contribution comes from the holes drilled in the PhC base. This statement is confirmed by the diode threshold evolution in Figure 144, where it increases with R_{base} while keeping R_{PhC} constant. We can conclude that the better passivation performed on “Sample wet” has a great impact on the holes drilled in the base, since it allows to minimize their resistive behavior by minimizing their effective electrical size.

Let us now focus our attention on the two samples' reverse current characterization: as we have introduced, this comparison gives us useful information on the Trap-Assisted Tunneling current, specifically on I_{SURF}. The reverse current investigation only deals with the PhC holes sidewalls, where the junction is spatially situated. For this characterization, we exploited PhC nanocavities without holes in the base, to avoid additional resistive components only concentrating on the PhC holes sidewalls response. The DUT presented R_{PhC} of 78 nm, with the same PhC period and cavity width compared to the structures of Figure 144.

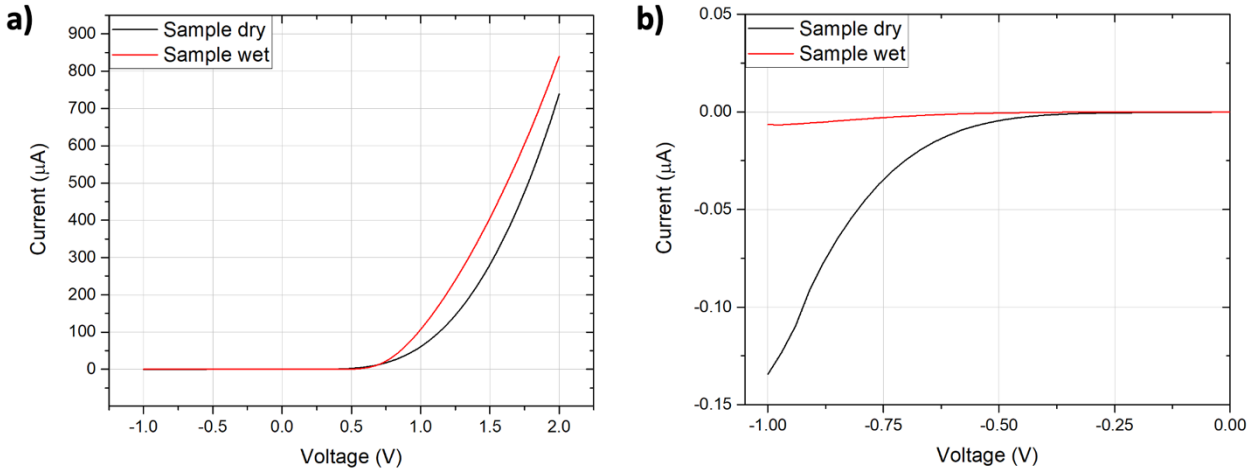


Figure 145: a) full I-V characteristics and b) reverse current comparison between cavities without holes in the base

From Figure 145-a), we can observe the current evolution under forward bias voltage: the resistance difference between the cavities of "Sample dry" and "Sample wet" is not very high, confirming another time our previous reasoning regarding the holes-in-the-base's resistive component. Focusing on 145-b), then, we notice that the reverse current is stronger for the cavity fabricated on "Sample dry" than for the "Sample wet" one: considering that the geometrical parameters are identical for the two structures, this means that I_{SURF} is more important on "Sample dry" and, consequently, confirms that the holes sidewalls on "Sample dry" present more trap states originated by surface defects and dangling bonds.

Thanks to this characterization we reinforce the hypothesis made after the comparison between the electro-optical measurement results. However, even though "Sample wet" showed a better AC electro-optical behavior than "Sample dry", moving to a DC biasing none of the fabricated samples were showing lasing behavior, meaning that even the ICP silica passivation layer removal by wet etching can be improved. We recall, in fact, that "Sample wet" was dipped inside the BOE solution only for few seconds, to avoid over-etching the silica layer underneath the nanocavities that would have caused very likely the PhC base to break and collapse. We decided, thus, to

perform carrier lifetime measurements on a cavity of "Sample wet" and on the same III-V semiconductor but unprocessed, in order to compare them.

5.2.5 Carriers lifetime measurement

As already anticipated, the goal of this characterization is to analyze the effect of holes' surface trap states on the repartition of radiative and non-radiative recombination mechanisms, to understand how efficient the passivation performed on "Sample wet" is. To do so, we extracted the carrier lifetime from a fabricated PhC nanolaser and from an unprocessed bulk semiconductor: the final goal was to derive radiative and surface lifetimes for the nanocavity and compare them, in order to understand which recombination mechanism was dominating. For this characterization we used Time-Resolved Photoluminescence measurements (setup schematized in Figure 146).

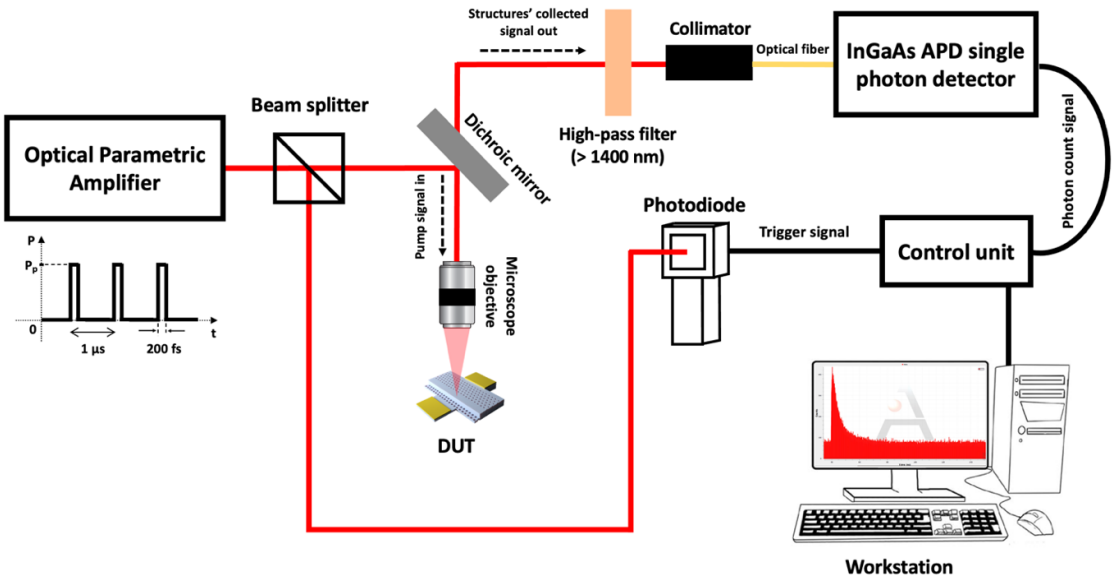


Figure 146: Schematic model of the adopted Time-Resolved Photoluminescence setup

The idea is to optically pump the DUT with an Optical Parametric Amplifier (OPA), emitting laser pulses at 1180 nm of 200 fs duration with a repetition rate of 1 MHz, in order to excite carriers inside the tested structure. The pulsed laser pump signal is divided by a beam splitter, sending a part to a photodiode and the rest to the DUT. The output signal, just like in the previous setups, is collected from the surface by means of a microscope objective and sent to a fiber collimator. The collected signal passes through a high-pass filter in order to filter out the pump. The collimator couples the light signal into an optical fiber, connected on the other terminal to an

InGaAs Avalanche Photodiode (APD) single photon detector: such a detection system allows to count the number of photons emitted from the DUT. The detector is connected to a Time tagging unit allowing the measurement of the arrival time of the photons on the detector with respect to a trigger signal (here provided by the photodetector on the pump path): in that way, a histogram can be built, representing the photon counts as a function of the time delay.

The resulting histogram gave us information about the electrical carriers' decay time once excited by the OPA: we could consequently fit the collected data by an exponential decay and extract the resulting time constant, representing nothing but the total carriers lifetime (Figure 147 represents as an example the histogram extracted from the bulk semiconductor fixing the bias voltage to 1.2 V).

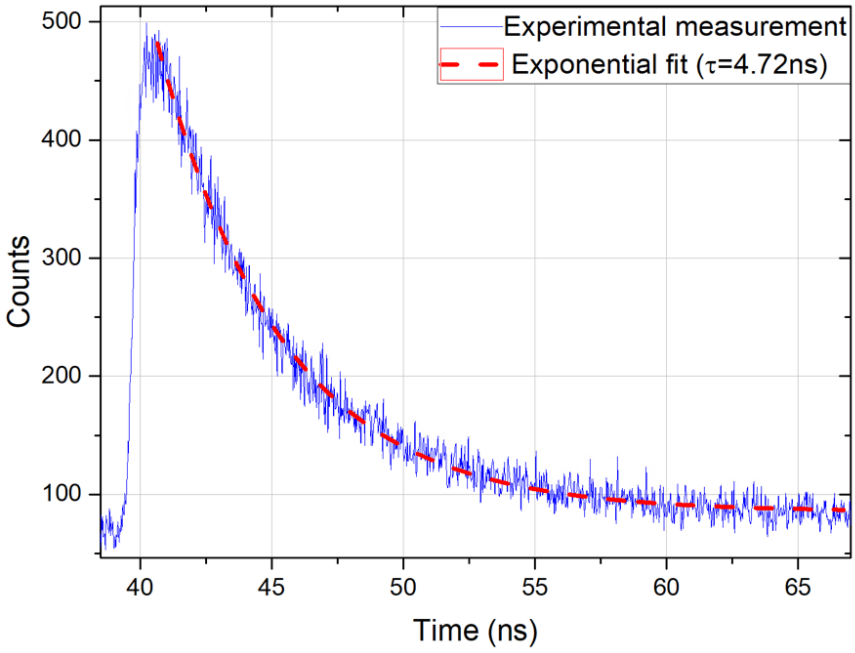


Figure 147: Measured photon counts decay (in blue) and relative exponential fit (dashed-red) for the unprocessed III-V semiconductor under a bias voltage of 1.2 V

During the measurement, the DUT was electrically biased with a constant voltage and several histograms were collected sweeping the voltage difference across the junction. We can appreciate the carrier lifetime evolution as a function of the electrical bias on Figure 148. The selected cavity for this measurement is from "Sample wet" and presents the following parameters: $a = 333\ \text{nm}$, $R_{PhC} = 81\ \text{nm}$, PhC cavity width $= 0.9 \cdot a\sqrt{3} = 519.1\ \text{nm}$, with 3 rows of holes in the base with radius $R_{base} = 70\ \text{nm}$.

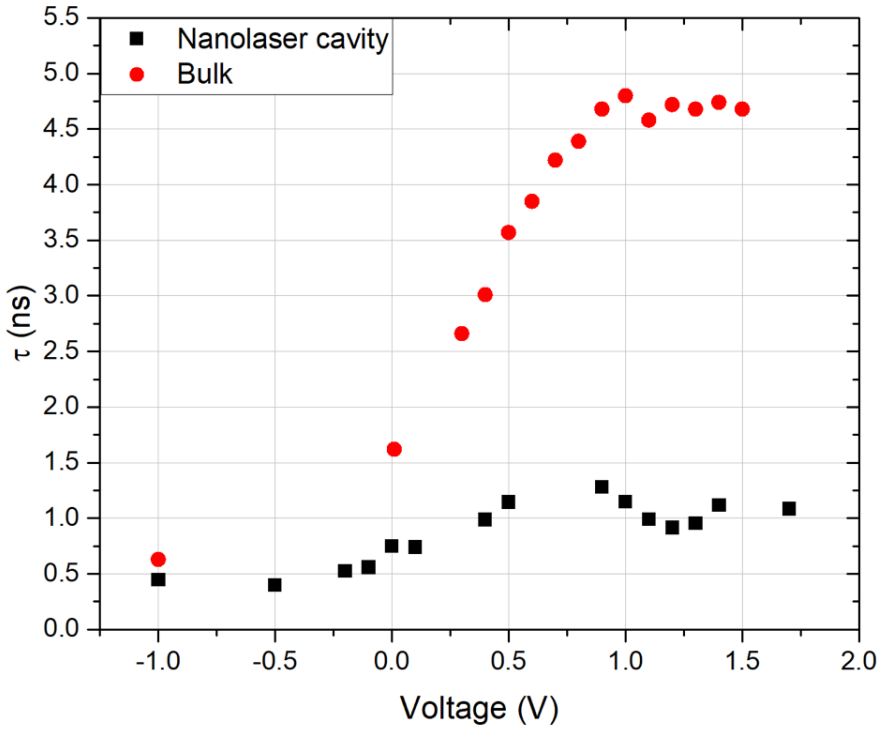


Figure 148: Carriers lifetime evolution as a function of the applied voltage for the selected nanolaser cavity and an unprocessed bulk semiconductor

As we can see, for both bulk semiconductor and nanolaser cavity, the carrier lifetime grows up to a voltage of around 0.9 V and then stabilizes. This effect is due to the P-i-N diode's band structure configuration (Figure 149). Due to the built-in potential inside the heterostructure, in fact, the energy difference between the conduction and valence band of the P- and N-doped layers can be small. This might allow inter-band tunneling transitions, reducing the overall carrier lifetime. However, when the external voltage grows, the energy difference between the two conduction bands (and the two valence bands) is reduced and an increasing amount of carriers diffuses through the junction's depletion region rather than performing interband tunneling transitions. The carrier lifetime grows up to the point where it saturates (for an applied voltage of 0.9 V), meaning that carriers leakage by tunneling effect has become negligible. Figure 148 tells us that the overall carriers lifetime for the nanolaser cavity and the bulk III-V is different, the former saturating at a value of around 1 ns while the latter at 4.7 ns.

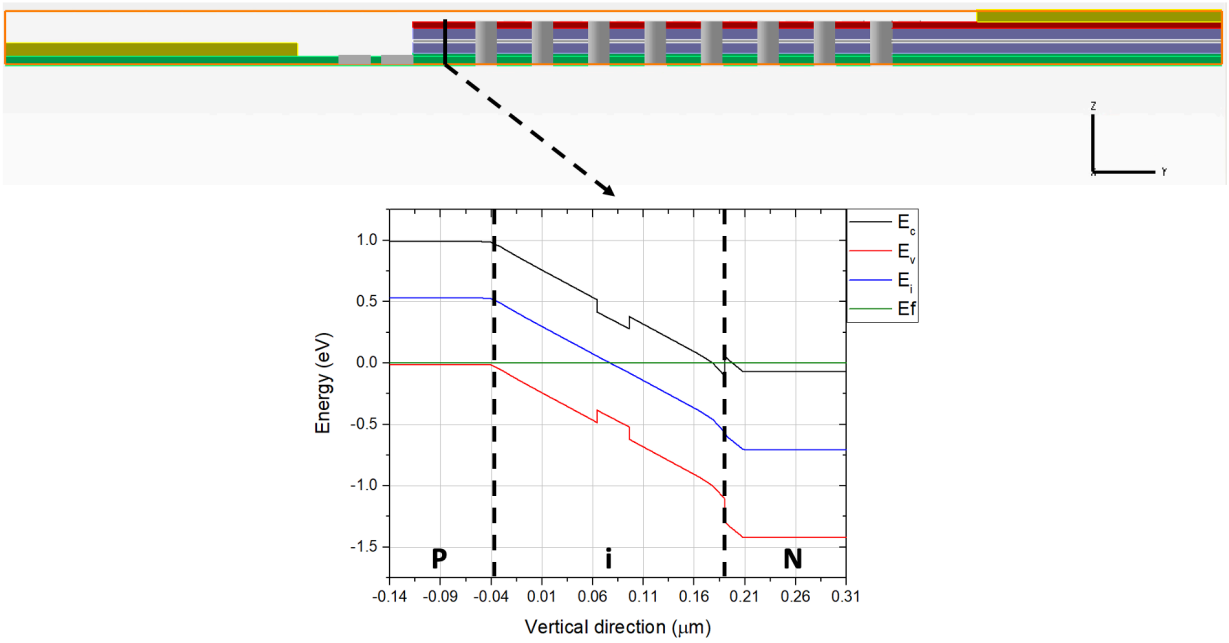


Figure 149: Nanolaser cavity's electronic band diagram at 0 V across the junction

As anticipated at the beginning of this section, with this characterization we mainly wanted to compare the lifetime for carriers recombining by radiative and surface mechanisms inside the nanocavity, in order to understand which predominated. To do so, we have to consider all the recombination processes we can observe in our structures, which are related by the following expression:

$$\frac{1}{\tau_{cav}} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{NR}} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Au}} + \frac{1}{\tau_{surf}} \tag{5.5}$$

Where τ_{cav} is the nanocavity's total carriers lifetime, composed by the lifetimes associated to radiative (τ_{Rad}) and non-radiative (τ_{NR}) recombination processes. From the literature we found that, for structures presenting InGaAsP MQWs heterostructures, τ_{SRH} and τ_{Au} can be fixed, respectively, at 20 ns [122] and 100 ns [123]. As we already saw in the previous sections of this chapter, surface recombination is the most critical among the non-radiative processes for a PhC, since the surface/volume ratio is very high for the presence of many drilled holes. On the other hand, the unetched III-V semiconductor does not present any opened surface, meaning that we can neglect the surface carriers lifetime from the equation:

$$\frac{1}{\tau_{Bulk}} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{NR}} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Au}} \tag{5.6}$$

Which leads to the following relation:

$$\frac{1}{\tau_{surf}} = \frac{1}{\tau_{cav}} - \frac{1}{\tau_{Bulk}} \tag{5.7}$$

Considering the bulk and nanocavity's carriers lifetimes extracted from Figure 146 ($\tau_{cav} = 1$ ns and $\tau_{Bulk} = 4.7$ ns), it follows that $\tau_{surf} = 1.27$ ns. Consequently, we can calculate the radiative carriers lifetime as:

$$\frac{1}{\tau_{Rad}} = \frac{1}{\tau_{cav}} - \frac{1}{\tau_{SRH}} - \frac{1}{\tau_{Au}} - \frac{1}{\tau_{surf}} \tag{5.8}$$

Which gives $\tau_{Rad} = 6.5$ ns. We can notice that the surface recombination lifetime is much shorter than the radiative one, meaning that non-radiative surface mechanisms dominate the recombination processes inside our nanolaser. This result explains why we could not achieve the lasing regime with a DC bias voltage: considering that surface recombination events are much more frequent than radiative ones, we lose the higher part of the injected current into non-radiative mechanisms, which locally heat up the device reducing the achievable gain.

5.3 Conclusion

During this chapter, we discussed the experimental results obtained during this PhD. We firstly showed the performed measurements on TLM structures, where we studied the P- and N-contact resistivities as a function of the RTA time and temperature. Our goal was to find the best parameters providing ohmic contacts with minimum contact resistance. This is achieved for a 30 s long RTA at 400°C, allowing to obtain $\rho_P = 5.6 \cdot 10^{-5}\ \Omega\,\mathrm{cm}^2$ and $\rho_N = 3.7 \cdot 10^{-4}\ \Omega \cdot \mathrm{cm}^2$. Then, we commented the EBIC characterization, which gave us the opportunity to map the 2D-PhC electronic activity and validate the designed electrical injection scheme: the appearance of an induced current, in fact, was only remarkable inside the PhC waveguide, where positive-charge carriers, once divided from the paired electron by the depletion region's electric field, could reach the P-contact from the shortest available path. This was confirmed by the EL analysis we did on a P-i-N diode designed with the same injection scheme, where the emitted photons were localized in close-proximity to the structure's sidewall.

After the electrical characterization, we showed the work developed on the fabricated nanolaser devices. The measurements under a CW optical pumping are in good agreement with the optical design, since all the investigated cavities showed single-mode behavior. Before moving to the analysis of their behavior under an electrical bias, we reported that the presence of HSQ was actually detrimental for carriers injection, being the source of current leakage: this forced us to fully insulate it from the semiconductor and the metals through exploitation of PECVD silica layers. For the electro-optical characterization, we considered two samples differing from the

adopted process to remove the silica passivation layer deposited during ICP etching: SF_6 dry etching ("Sample dry") and BOE wet etching ("Sample wet"). In both samples, under an AC electrical bias, we observed single-mode laser emission from the cavities with $R_{base} = 70\ nm$. "Sample wet" is the one showing the best performances, with laser threshold currents very close to the theoretical model derived at the end of chapter 3 ($I_{th} \sim 75\ \mu A$). The main limitation for "Sample dry" originates from the inefficient ICP passivation layer removal, preventing the successive holes' sidewalls sulfur passivation: in that way, a higher amount of carriers is lost in non-radiative surface recombination. Unfortunately, none of the characterized samples showed lasing behavior under a DC electrical bias, even though laser peaks are observable in nanocavities' emission spectra from "Sample wet".

The last two characterizations we showed during this chapter are focused on the study of the holes' sidewalls passivation: firstly, we compared the I-V characteristics of nanolaser diodes from the two samples, confirming that the BOE wet etching is a much better solution to remove the silica passivation layer created during ICP etching. In fact, the holes drilled in the base of cavities from "Sample dry" showed a more resistive behavior and a stronger reverse current than the same structures of "Sample wet". Eventually, we analyzed the carrier lifetime for a cavity of "Sample wet" and compared it to the one of an unprocessed bulk semiconductor. This last characterization gave us the confirmation that the passivation method used on "Sample wet" must be improved in order to make our structures work under a DC polarization voltage, since the lifetime associated to non-radiative surface recombination is shorter than the one associated to radiative processes (1.27 ns vs 6.5 ns).

Chapter 6: Conclusion and future work

6.1 Conclusion

Modern society is going through deep digitalization, representing nowadays one of the main challenges from a technological point of view. The huge amount of digital data streaming in network systems is still following an exponential growth, demanding for an increasing transfer speed while minimizing energy consumption. Up to now, integrated circuit technology for computational as well as communication systems has been based on microelectronics though it is approaching a technological bottleneck: even if the transistor's technology node has reached nowadays 3 nm feature size, the main concern comes from interconnections, limiting the performances in terms of speed and power consumption. New solutions are under investigation in order to replace the lossy metallic wires. Photonics represented since the 80s a good alternative to electronics for long distance telecommunication systems: today, 99% of transoceanic data traffic is carried by optical fibers. Moreover, ever since the appearance of data centers, optical transceivers entered the scene, becoming the major entity in charge of managing the server-to-server data transfer. However, the main source of energy consumption inside these huge infrastructures sits in server computations: in this context, no valid alternative to integrated circuits' interconnections is available yet. One of the best prospectives to answer this problem is nanophotonics, consisting in low power and ultra-high speed devices with dimensions below 100 μm^2, allowing to trap and manage light within volumes close to the diffraction limit $\left(\lambda/n\right)^3$. Among them, electrically driven Photonic Crystals (PhC) seem to be the most mature technology and the best tradeoff in terms of footprint, power consumption and costs [59], as we saw during chapter 1.

During this PhD, we worked on the development of a nanophotonic solution based on an optoelectronic bidimensional photonic crystal (2D-PhC) integrated on a silicon platform for the conception of a laser source and an optical amplifier, key components of optical integrated circuits for telecom and computercom applications.

Chapter 2 was dedicated to the theoretical modeling of the 2D-PhC nanoamplifier. After introducing the general optical properties of a 2D-PhC membrane, we presented our asymmetric

geometry exploiting the PhC pattern as a metamaterial (i.e., the index-guided PhC band) to confine light. This asymmetrical design causes the appearance of a non-zero electric field's vertical component: particular care had to be taken choosing the geometrical parameters, in order to minimize the TM component's effective index with respect to the TE one. The interfacing between passive silicon circuitry and 2D-PhC waveguide was performed through evanescent coupling by means of taper structures, where the idea is to play with the effective index difference between the two waveguides (varying the PhC waveguide width) to achieve smooth light transfer from one platform to the other. We presented two mode converters: the first one consisted in linearly varying the PhC waveguide's effective index (linear taper); the other one was based on the adiabaticity criterion presented in [74], reducing the taper length with respect to the linear version while maintaining smooth coupling between passive and active platforms. The main purpose of the asymmetric design, anyway, is to implement, from an electrical point of view, a lateral carrier injection scheme: the goal is to concentrate the majority of radiative recombination events inside the PhC waveguide, so to achieve efficient interaction with the propagating optical mode for light amplification. We did that by placing the PhC waveguide in close proximity to the PhC P-doped base, taking advantage of the large difference in mobility between electrons and holes. Such a design proved to be suitable for low power application as required by photonic integrated circuits, with device's length and bias power reduced by an order of magnitude compared to state of the art solutions to attain the same amplification level. It is possible to further reduce the device's length by taking advantage of the slow-light regime, consisting in a local perturbation of the PhC waveguide geometry causing a reduction of the propagating mode's group velocity, enhancing light-matter interaction.

In chapter 3, we focused our attention on the design of our 2D-PhC structure as a laser source. Differently from the nanoamplifier, we did not exploit the index-guided band of the 2D-PhC but rather the gap-guided one, in order to build an apodized cavity. It has been demonstrated, in fact, that the best way to minimize the out-of-plane losses in a resonant cavity is to design it so that the fundamental mode possesses a Gaussian shape, taking advantage of the field's *gentle confinement* [91-92]. The apodization was performed by perturbing the PhC cavity width from the cavity center to its edges. To do so, we played only on the PhC wall side while keeping the PhC holes position unvaried, to freely choose the spatial step inside the apodization algorithm getting rid of the limitation posed by the PhC period. The asymmetrical geometry limited the achievable Q-factor, since similarly to the nanoamplifier we observed the appearance of a non-negligible vertical component of resonance mode's electric field. Such an unwanted component completely disappears in absence of the PhC base. However, considering that the P-doped base is fundamental for the electrical carrier injection, we managed to minimize its impact by drilling additional holes in the base, getting as close as possible to the ideal no-base case from an optical point of view. The signal extraction is done exploiting the evanescent coupling between the cavity and the silicon waveguide: the very short vertical distance we worked with forced us to apply a

transversal shift between the cavity and the silicon waveguide in order to decouple them, considering that we were dealing with an over-coupled system. The electrical injection scheme design is similar to the nanoamplifier's, even though for the nanolaser we decided to reduce the base length to efficiently overlap the longitudinal radiative recombination profile with the Gaussian electromagnetic field, so to minimize the bias power. Interfacing optical and electrical simulation results, we observe that the designed cavity possesses a laser threshold current below 100 µA, with a wall-plug efficiency of 23% for an injected current of 250 µA and a slope efficiency of 32% rendering it highly competitive for integrated circuits applications.

Chapter 4 was dedicated to the fabrication of the previously designed devices, demonstrating the calibration of a CMOS-compatible technological process flow. The first idea was to integrate MgF_2 as an interlayer between SOI and III-V to protect the passive circuitry from chemical attacks, presenting perfect chemical inertia to HF-based acids. Additionally, it possesses low refractive index, transparency at telecom wavelengths and high thermal conduction, making it a great inter-dielectric layer for our purpose. However, the elevated material strain represents a limitation: we constantly observed cracks appearing all over the MgF_2 surface during the sample processing, no more protecting the SOI substrate. Thus, we decided to modify the initial process flow, inverting the III-V fabrication stages and exploiting BOE to remove the HSQ hard mask only after the first ICP etching (PhC waveguide's sidewall and P-doped base creation), while leaving it after the holes drilling (to avoid the collapse and subsequent breaking of the PhC base). Concerning the metallization, Pd and Zn were used for the P-metal so to achieve an ohmic contact: while Zn purpose is to diffuse through to the metal/semiconductor interface (during the Rapid Thermal Annealing step following metallization) to over-dope it, Pd is exploited to create a uniform morphology at the metal/semiconductor interface, without unwanted protrusions that would affect the contact quality. For both P- and N-contact, then, a multi-layer made of Ti/Pt/Ti/Au was deposited, where Pt is exploited as a blocking layer: while on the P-side it forces the Zn to only diffuse downwards, towards the metal/semiconductor interface, on the N-side it prevents the Au diffusion down to the III-V semiconductor during RTA. Sidewalls passivation was a very critical step to perform, to annihilate surface dangling bonds caused by ICP dry etching process and minimize non-radiative surface recombination. To protect the volatile sulfur passivation layer and evacuate the heat accumulated around the nanostructures, a 1 µm thick silica encapsulation layer was deposited by PECVD. Its conformal deposition allows to protect the passivated holes sidewalls. Eventually, in order to bias the fabricated structures during characterization, vias were opened through the encapsulation layer right above P- and N-contacts and metallic pads were deposited on top of the 1 µm thick silica layer for the electrical probes contacting.

Chapter 5 was devoted to the experimental work developed during this project. Firstly, we studied TLM structures to optimize our RTA step during fabrication: our goal was to find the best annealing temperature and time to achieve an ohmic contact for the metallic contacts with the

smallest resistance. Then, we performed an EBIC characterization which validated the design of our electrical injection scheme, showing the appearance of an induced current only inside the PhC waveguide. The analysis of the P-i-N diode's electroluminescence reinforced our conclusions on the designed injection scheme, since under a forward bias across the junction the emitted photons were localized in close-proximity to the structure's sidewall. Unfortunately, no remarkable results have been extracted from the nanoamplifier characterizations, even though they helped us a lot to improve the technological process flow. We moved to measurements on our nanolasers: we observed good agreement with the optical design by pumping them with a CW laser, as they proved to work as single-mode nanolaser sources. After that, we characterized them under electrical bias. Firstly, we improved our fabrication process flow by observing that HSQ is a source of current leakage, pushing us to completely insulate it from the semiconductor as well as the metals by means of silica layers deposited by PECVD. Then, with the improved process flow, we investigated the nanocavities operation biasing them with an AC signal, obtaining a good agreement with the theoretical model concerning the measured low threshold currents, especially from "Sample wet" (ICP passivation layer removed by BOE wet etching). Eventually, the cavities were characterized using a DC electrical bias: even though from the extracted spectra we could see resonance peaks, the lasing regime was not achieved. These results indicate that the main limitation was the suboptimal ICP silica passivation layer removal, which was preventing sulfur deposition to passivate the sidewalls. To verify it, we firstly compared the cavities' I-V characteristics both under forward and reverse bias conditions: the nanocavities of "Sample dry" showed higher resistance due to the presence of the holes-in-the-base and higher reverse current with respect to the ones of "Sample wet" with identical geometrical parameters. This highlights that BOE wet etching is much better than unaccelerated SF_6 plasma etching to remove silica deposited during ICP etching. Secondly, we performed a Time-Resolved Photoluminescence characterization, in order to extract the carrier lifetime from a cavity of "Sample wet" and from an unetched piece of the same III-V semiconductor: our goal was to retrieve the cavity's surface and radiative recombination lifetimes and compare them. Thanks to the extracted result we concluded that the non-radiative surface processes were dominating compared to the radiative ones, understanding why our cavities were not working under DC-bias condition.

6.2 Future work

6.2.1 Short-term prospects

During this PhD, an extensive work was performed on the design and fabrication of 2D-PhC devices for light amplification and laser emission. The established theoretical model suggests that with this kind of structures it is possible to confine light in small volumes close to the diffraction limit and conceive devices targeting ultra-low power applications. Additionally, the calibrated technological process flow respects the temperature limitation posed by the CMOS back-end-of-

line, rendering our structures compatible for the on-chip co-integration of photonic and microelectronic circuits. This could open up a new road for the conception of ultra-fast communication and computing systems, such as integrated optical transceivers or all-optical microprocessors. However, to get to that point, we still need to improve and optimize some technological as well as design steps.

As fully discussed, surface recombination is a critical process for the performances of 2D-PhC optoelectronic structures: a proper passivation must be engineered to annihilate surface dangling bonds. The deposition of sulfur atoms was calibrated by the team before the beginning of my PhD project and it proved to be a very efficient method to increase non-radiative surface lifetime [71]. However, before proceeding with sulfur passivation, it is of crucial importance to properly remove the ICP silica passivation layer created at the holes sidewalls during their etching. In this work, we implemented two removal methods: the first one by taking advantage of an unaccelerated SF_6 plasma etching process, while the second one was based on the silica wet etching by BOE. The obtained results underline the fact that, even though the ICP silica passivation layer removal by wet etching proves to be more efficient than dry etching, just dipping the sample inside the BOE solution for few seconds as we did is not sufficient to fully remove it from the holes' sidewalls. The main limitation of the calibrated process flow is that we cannot perform the silica wet etching process for as much time as we want, for two main reasons:

- Firstly, we would risk to chemically attack the SOI passive circuitry. We must consider, in fact, that we work with a small vertical distance between silicon waveguides and III-V devices (around 200 nm) and that we have silica as an interlayer dielectric, which is rapidly etched by BOE.
- Additionally, an extended BOE wet etching would attack the silica underneath the 2D-PhC structures causing the collapse of 2D-PhC base (as we saw in Figure 105 during chapter 4), breaking it and rendering the electrical carriers injection impossible.

The very first goal to improve the nanostructures performances following the results and ideas of this PhD work is to implement an efficient method to fully open the PhC holes sidewalls after ICP etching. Another very important optimization that must be considered is the HSQ mask removal after the second III-V fabrication stage: as we saw, in fact, it limits the heat evacuation and it is source of current leakage if not properly isolated from metals and semiconductor. Thus, the exploitation of a BOE wet etching solution after the holes drilling has a double advantage: if we could dip the sample inside the acid for as long as we want, in one step we could get rid of the HSQ hard mask and the ICP silica passivation layer. To do so, we must develop a process protecting the silica underneath the structures: the exploitation of a material presenting chemical inertia to HF-based solutions, like MgF_2, seems to be a good way. However, during chapter 4, we discussed how tricky the exploitation of this material is. From a technological point of view, one of the most important tasks to tackle will be to study in depth this material's

properties and optimize the process by minimizing its strain and its exposure to humid environments.

Some additional optimization can be done as well on the structures' design: one idea, in fact, would be to minimize the number of PhC holes, minimizing the surface/volume ratio. Even though the passivation problem was not solved, reducing the number of holes would surely reduce the impact of non-radiative surface recombination mechanisms. Consequently, another important work to develop will be to find the minimum amount of PhC rows of holes we actually need to confine the electromagnetic field inside the PhC waveguide (or cavity) without affecting the performance.

Another interesting optimization that deserves to be studied concerns the injection efficiency: in fact, we recall from the design chapters that the radiative recombination rate profile along the transversal direction is peaked inside the PhC waveguide (or cavity), decaying once entering the PhC pattern. However, inside this region, the recombination rate does not really fall to zero: this surely introduces current leakage reducing the carriers concentration inside the PhC waveguide (or cavity). This can be improved by using hydrogenation of the P-doped layer inside the PhC holes' pattern by ion implantation. In this way, P-doping would be annihilated in the region exposed to hydrogen and the only available junction would remain the one inside the PhC waveguide, concentrating all the radiative recombination mechanisms there.

Eventually, once the operation under a DC bias voltage demonstrated, it will be very important to analyze the bandwidth of these nanostructures. Considering their small dimensions and the small volume covered by the P-i-N junction's depletion region (which will be further reduced through the P-layer hydrogenation), we expect the capacitance to be ultra-low: we strongly believe that these devices can be suitable for ultra-high speed operation.

6.2.2 Long-term prospects

The designed 2D-PhC optoelectronic structure presents a high versatility: just readapting the geometrical parameters, it is possible to conceive all the devices we can find in a photonic circuit. During this thesis, we saw that it can be modeled as an amplification stage and a laser source. Unfortunately, the encountered fabrication problems did not allow us to extract reliable results from the characterized nanoamplifiers. This structure, in fact, was the first one we tried to fabricate during this PhD, using MgF_2 as an interlayer dielectric. The main limitation was posed by the high material strain, which was cracking and opening up paths through which the BOE could pass, attacking the SOI substrate and damaging the silicon waveguides: during characterization, the signal injection and/or extraction was not reliable. Once the passivation issue solved, one of the main future work will be to evaluate the nanoamplifier performances, to demonstrate its suitability for low-power applications.

Another possibility is to adapt the 2D-PhC geometry for the conception of a photodetector. When an incoming optical signal is coupled to the III-V device, it can excite electron-hole pairs inside the active heterostructure which are then divided by the built-in electric field. Polarizing the P-i-N junction diode with a reverse bias, we actually generate a current of minority carriers. We can adapt the structures designed during this PhD to create two types of photodetectors:

- A PhC waveguide photodetector, based on the nanoamplifier design, presenting large optical bandwidth.
- A resonant photodetector, based on the nanolaser design, working at a single resonance wavelength but presenting smaller footprint and power consumption compared to the wide bandwidth alternative.

Standard photodetection solutions need transimpedance amplifiers (TIAs) at their output: the role of this electronic block is to read the output voltage from the photodetector while minimizing its thermal noise (maximizing the S/N ratio of the output signal) and its output impedance (minimizing the RC time constant to increase the driving speed). TIAs are generally expensive and highly energy-consuming. The great interest to design a photodetector with the asymmetric 2D-PhC geometry relies on the fact that the junction's capacitance is ultra-small. It is then possible to simply provide a high output impedance so to maximize the S/N ratio, while the RC time constant remains low "regardless" of R thanks to the ultra-small C. Consequently, the TIA can be replaced by a simple resistor with sufficiently high resistance value, as it has been demonstrated in [127]. The development of our structure as photodetector is the object of a CNRS prematuration program we won during the last year of this PhD project.

The versatility showed by the asymmetric 2D-PhC structure opens up great prospects also for the integration of the conceived devices in a photonic integrated circuit. Their reduced footprint and power consumption give the possibility to envisage their dense integration in a single circuit. Moreover, thanks to the developed technological process flow respecting the limitation imposed by the CMOS back-end-of-line, these structures can pave the way for the on-chip cointegration of photonic and microelectronic integrated circuits. This would allow to go beyond the limitations of the electronic interconnection bottleneck. Particularly, these nanophotonic solutions possess the required performances for the conception of integrated optical transceivers (for example, for the high speed communication between electronic entities inside a microprocessor), capable of transferring data at speeds above 1 Tbit/s. Furthermore, their reduced dimensions together with their low power consumption and ultra-high driving speed can also be beneficial for the conception of all-optical hardware solutions for Artificial Intelligence (AI) and Deep Learning (DL) applications.

Table of Figures

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