Prediction and Optimization of Electromagnetic Behavior of Multi-cell Converters

Glauber de Freitas Lima

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ GRENOBLE ALPES

École doctorale : EEATS - Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS) Spécialité : GENIE ELECTRIQUE
Unité de recherche : Laboratoire de Génie Electrique

Prediction and Optimization of Electromagnetic Behavior of Multi-cell Converters.

Présentée par :

Glauber DE FREITAS LIMA

Direction de thèse :

Jean-Christophe CREBIER Directeur de recherche, CNRS	Directeur de thèse
Yves LEMBEYE Professeur des universités, UGA	Co-directeur de thèse
Fabien NDAGIJIMANA Professeur des universités, UGA	Co-directeur de thèse

Rapporteurs :

Eric LABOURE
Professeur des universités, Université Paris-Saclay
Cristhian VOLLAIRE
Professeur des universités, EC-Lyon

Thèse soutenue publiquement le, devant le jury composé de :

Jean-Luc SCHANEN Professeur des universités, Grenoble INP UGA	Président
Daniel MONTESINOS-MIRACLE Professeur des universités, UPC	Examinateur
Eric LABOURE Professeur des universités, Université Paris-Saclay	Rapporteur
Christian VOLLAIRE Professeur des universités, EC-Lyon	Rapporteur

Invités :

Fabien NDAGIJIMANA
Professeur des universités, UGA
Jean-Christophe CREBIER
Directeur de recherche, CNRS
Yves LEMBEYE
Professeur des universités, UGA

"The only way to make sense out of change is to plunge into it, move with it, and join the dance." - Alan Watts

Résumé

Alors que les convertisseurs conventionnels requièrent une étude et une qualification EMI post-conception, l'approche suivie au G2Elab repose sur une analyse pré-manufacturation du comportement du convertisseur à partir d'un ensemble de prototypes représentatifs grâce à l'utilisation de réseau de convertisseur. Pour les applications de faible et moyenne puissance, ils sont innovants pour les ingénieurs et concepteurs en électronique de puissance. Ils s'appuient sur un nouveau paradigme et une expertise, en complément des connaissances traditionnelles requises, et peuvent offrir des opportunités de conception automatisée, y compris en ce qui concerne les aspects CEM, qui constituent le sujet de cette thèse. Sur la base de résultats analytiques théoriques et expérimentaux allant d'un seul convertisseur cellulaire à un ensemble de convertisseurs cellulaires et de leurs configurations de connexion possibles, il est possible de construire une base de données et une expertise afin de prédire et d'améliorer la signature EMI d'un convertisseur multicellulaire. En résumé, ce travail est une compilation de sujets: (i) dimensionnement d'un DAB dans le contexte d'un convertisseur modulaire axé sur les performances EMI conduites, la prévisibilité et l'amélioration, (ii) fondamentaux des ensembles de convertisseurs modulaires/multicellulaires/de puissance, et enfin (iii) prédiction/amélioration de la signature EMI dans un aspect CEM général.

Abstract

While conventional converters require a post design EMI study and qualification, the approach followed at G2Elab relies on a pre-manufacturing analysis of the converter behavior from a set of representative prototypes through the use of Multicell converters. For low and medium power applications, they are innovating for power electronics engineers and designers. They rely on new paradigm and expertise, in complement to the traditional knowledge needed, and can be an opportunity for automated design, including in EMC aspects, which is the topic of this thesis. Based on analytic theoretical and experimental results from one single-cell converter up to a set of cell converters and their possible connection configurations, it is feasible to build database and expertise in order to predict and improve the EMI signature of a multicell converter. In summary, this work is a gathering of subjects: (i) dimensioning of a Dual Active Bridge in the context of modular converter focusing on Conducted EMC performance, predictability and improvement, (ii) fundamentals of Modular/Multicell/Power Converters Arrays and, finally (iii) EMI signature prediction / improving in a general EMC aspect.

Acknowledgements

I would like to express my deep gratitude to the individuals who supported me throughout my approximately three-year journey in pursuit of my PhD. This journey started with Andre Andreta, a Brazilian PhD candidate at the time, who not only informed me about the PhD opportunity at Université Grenoble Alpes but also evolved into a close friend. Other fellow Brazilians also played an important role in my initial experiences of adapting to life in the old country, but new at the time to me, France — along with its culture and language.

Likewise, all the people of the EPICUB project who actively helped whether it was diving into theories or getting hands-on with practical stuff: once again Andre Andreta, Théo Lamorelle, Boubakr Rahmani, Hugot Pichon, and new ones who arrived 1.5 years later, Tugce Turkbay and Li Fang. To you all, thank you for this awesome work environment! To the inter in which I was supervising, Adrien Bourmann, thank you specially for your hard work and I hope you may see some of the results you have contributed to this thesis. To all others of " équipe EP", you are many and thank you all similarly!

I must emphasize even more my comrade Bakr's contributions. We teamed up and published a journal article together. He's not just a colleague but also a true friend who has been there through the good times and the challenging ones right from the start.

Additionally, I would like to express my sincere appreciation to the members of the jury for my PhD defense: Prof. Eric Labouré from Université Paris-Saclay, Prof. Christian Vollaire from École Centrale de Lyon, Prof. Jean-Luc Shanen (who also participated in my "CSI") from Université Grenoble Alpes, and Prof. Daniel Montesinos i Miracle (who I had the privilege of collaborating for three months at Universitat Politècnica de Catalunya (UPC) through an exchange program).

Last but not least, I want to give a huge thanks to my supervisors: Jean-Christophe Crébier, Fabien Ndagijimana and Yves Lembeye. We made a seriously creative team, and I appreciate for sharing your insights, thoughts and guidance. Thanks for trusting me and letting me roam free with my PhD exploration.

I wish I had more time and talent to really craft more words, but when it comes to the folks who cross our paths, what matters most is the snapshot we hold when we close our eyes. To everyone I have mentioned, I think and picture you all with beautiful smiles. Thanks again for being a major part of my journey and helping me grow and succeed.

Content

General introduction

Electromagnetic compatibility (EMC) standards, driven by Electromagnetic Nuclear Impulses and High EM fields from lightning, address the impact of electromagnetic interference (EMI) on aircraft. Catastrophic incidents prompted the formation of commissions that established EMC compliance standards for electronic devices. Unfortunately, power electronics courses often overlook EMI issues and their solutions, focusing solely on efficiency, power density, and cost of prototypes (mostly at the lower technology readiness level (TRL)). This approach falls short of ensuring EMC compliance and overlooks vital aspects such as input/output filters, electromagnetic shielding, and final case design. Consequently, at the final TRL stage, it can lead to increased prices, complexity, time, volume, and losses.

In the conventional power electronics (PE) industry, compliance with EMC standards is typically entrusted to Electromagnetic engineers who are skilled in setting up and operating EMC measuring equipment. However, they may lack knowledge about the origins and pathways of EMI issues specifically in power electronics. As a result, only palliative solutions are commonly implemented, not seldom leading, once again, to the use of bulky passive filters and denser case shields, without achieving optimal product design.

Indeed, the increasing trends in switching frequency, dv/dt, and compactness in power electronics have the potential to intensify EMI issues if not addressed during the initial design phase. Recent findings highlight the importance of considering EMI at the outset, particularly after accurately calculating and extracting coupling parasitic paths. Switched models, implemented using software such as LTspice, PSIM or ADS Keysight, can provide a representative EMI Conducted Emission (CE) signature. Achieving accuracy in these models relies on extracting parasitic elements, which is typically done in the pre-phase using analytical equations or finite element methods (FEM) with low step time requirements, making it a time-consuming process. High-frequency models of input and output filters can then be employed to proactively verify CE compliance.

However, knowledge solely based on simulation and extraction accuracy does not necessarily lead to effective decision-making or interactive optimization. This approach tends to be time-consuming and presents challenges in terms of conclusiveness, comprehensiveness, generality, and unification. In contrast, by constructing equivalent and/or analytical equations, the EMI signature can be more easily understood in a generalized manner, requiring less time

and enabling mitigation at the source. In many cases, first-order solutions, coupled with an appropriate margin, may suffice in an environment where relative errors between theoretical and practical results can easily reach 100 % (6 dB).

As a matter of fact, first-order analysis and testing can be a useful tool for analysis if it is representative, conservative, and comparative. It provides a simplified and initial understanding of the system or problem at hand. However, there are situations where first-order and simplifying models may not capture all the complex issues, such as the self-resonance of a capacitor in the context of electromagnetic compatibility (EMC) compliance.

If a designer solely relies on first-order analysis and simplifications and fails to achieve satisfactory theoretical EMC compliance, it indicates the need to explore other solutions. In such cases, increasing the complexity of the model may not necessarily help address the underlying issues. Instead, the designer should consider alternative mitigating solutions.

This highlights the importance of using appropriate analysis techniques that align with the specific requirements and constraints of the problem. It's crucial to strike a balance between simplicity and accuracy, considering both the limitations of the analysis approach and the complexity of the real-world system being analysed.

The ability to simplify complex physical problems like EMI, even when occasionally overlooked, stems from insightful reflections based on extensive experimentation, simulation, and thorough mathematical analysis. Consequently, a significant portion of this manuscript is dedicated to qualitatively and reflectively exploring this topic, prioritizing a comprehensive understanding rather than a focus on quantitative analysis.

Once the initial first-order solutions have been implemented and observed, the designer can proceed to improve and complexify the model, as in the case of digital twins. Digital twins are virtual replicas of physical systems that can simulate and analyse their behaviour in a more detailed and accurate manner.

By incorporating more complex models and simulations, designers can gain a deeper understanding of the system's behaviour and potentially identify additional factors that may affect electromagnetic interference (EMI) issues. This can help in refining the design and mitigating EMI problems.

However, it's important to note that even with more sophisticated models and simulations, there is no guarantee that all EMI issues will be completely resolved. EMI is a complex phenomenon influenced by various factors, including electromagnetic compatibility (EMC) standards, component characteristics, system layout, grounding techniques, and more.

Therefore, it is required a comprehensive approach that combines both theoretical analysis and practical testing to ensure EMC understanding and compliance.

In addition to theoretical understanding, practical measurement, and data analysis of EMI signature and optimization, the focus of this thesis is on achieving fast and automated design, in line with the concept of Power Electronics Design 4.0 [1] [2]. Recent progress has been made in automated design, supported by models and simulations, but interactive features are still limited. By mapping the performance space and utilizing virtual prototypes and parameter extraction, power electronics can be conceptualized. The next steps involve assisted design, leveraging past designs and experience, followed by augmented design, which aims for the independent generation of full designs. However, achieving this objective still requires significant advancements.

EMI issues have been identified as a major concern that hinders the optimization of the design process. Specifically in the context of EMC, before reaching the ideal point envisioned by Power Electronics Design 4.0, a substantial amount of standardized experimental, simulation, and analytical data is necessary. While extremely AI-optimized methodologies and heterogeneous solutions have shown promise, they risk further widening the gap between academia and industry. Perhaps, the solution lies not in relying solely on Artificial Intelligence, complex simulations, and time-consuming parameter extractions, but rather in employing simple natural intelligence. This middle ground solution would strike a balance between industry's reliance on "rule of thumb" methods to ensure safety and durability, and the highly sophisticated approaches found in academic references.

In the absence of the arguable utopian AI-based virtual simulation solution, there exists a methodology developed by G2Elab called Power Converters Arrays (PCAs) [3], [4], [5], [6], [7] which offers an alternative or at least a facilitator for power electronic design automation. This methodology revolves around the concept of multi-cell or modular converters. The advantages of multi-cell converters for high-power and/or high-voltage applications have been extensively documented in the literature [8]. By dividing voltage and/or current ratings in various configurations such as input-series output-parallel (ISOP), input-series output-series (ISOS), input-parallel output-series (IPOS), or input-parallel output-parallel (IPOP), it has been demonstrated that the overall converter can be optimized in terms of efficiency, power density, Differential Mode (DM) current signature through interleaving modulation solutions, and even cost. This optimization is achieved by employing lower-rated components and reducing cooling requirements, which are highly desirable in industrial applications [9], [10].

Besides the aforementioned advantages, plug-and-play multi-cell topologies can also offer similar benefits in low/medium power/voltage applications. By implementing multiple Conversion Standard Cells (CSCs) based on the Dual Active Bridge (DAB) architecture, it becomes possible to predict the characteristic behaviour, including EMI signature of any power converter within the framework of the multi-cell/modular converter approach. It is worth noting that the Power Converters Arrays (PCA) approach discussed here represents a specific application/concept within the broader domain of multi-cell/modular converters. However, throughout this manuscript, the terms "multi-cell converter", "power converter array (PCA)" and "modular converter" will be used interchangeably.

The selection of a suitable Conversion Standard Cell (CSC) topology for a specific application should consider multiple criteria, including efficiency, charging profile characteristics, power density, galvanic isolation, power directionality, costs, dynamic behaviour, controllability, expertise, and complexity. Each criterion plays a crucial role in determining the appropriateness of a topology for a given application.

This thesis acknowledges that its objective is not to enforce the adoption of the most optimal topology choice or seek a modulation technique that enhances efficiency and power density performances. Instead, it is an opportunity mainly focus on providing a comprehensive EMI signature description of a popular topology, namely the Dual Active Bridge (DAB) converter operating with a simple modulation strategy, which is the single phase-shift modulation (SPS), as a representative use case. This focus on EMC performance will contribute to a more holistic understanding of the converter's behaviour and enable the development of effective EMI mitigation strategies.

On the other hand, different features allows to consider it among other DC/DC converter topologies, since it has become a popular DC-DC converter over the last ten years that allows galvanic isolation, bidirectionality in power, symmetricity, controllable output, high power density, and efficiency. Due to such exceptional performance and features, it is mostly used in renewable energy systems [11], [12], energy storage systems [13], DC distribution systems [14], and solid-state transformer (SST) [15].

The subsequent sections of this Chapter 1 are divided into two parts. Firstly, an overview of the main EMC topics and concepts that form the basis for the subsequent chapters. This section lays the foundation for the discussion and analysis that follows in this manuscript regarding EMC. In the second part it is provided the context of assessing EMC compliance through multi-cell converter approach is presented. This framework sets the stage for the thesis and establishes the context within which the research is conducted

Chapter 2 of the thesis focuses on the analysis of the Dual Active Bridge (DAB) using single phase-shift modulation, which is the DC/DC converter component of the Power Converters Arrays (PCA). The chapter examines the differential mode (DM) noise, Zero Voltage Switching (ZVS) performance, and drain-to-source voltage of the DAB. The impact of AC resistance is also discussed and compared to a lossless model. Additionally, the chapter explores the characterization and prediction of DM noise through open circuit (OC) testing, a facilitating method to predict EMI signature either Conducted Emission (CE) or Radiated Emission (RE), proved through experimental results across appendixes and following chapters.

In *Chapter 3*, the emphasis shifts to the analysis of the common mode (CM) noise model of the DAB. A novel approach is proposed that considers the asymmetry of the parasitic capacitances of the full-bridge configuration. Simulation and experimental results highlight the importance of maintaining a symmetrical design to reduce resonances and achieve up to a 20 dB reduction in CM noise.

Chapter 4 delves into the impact of mismatch on voltage, current, and power sharing in multi-cell converters due to device tolerances / component dispersions. A new theory based on two-port network theory is presented, offering a unified perspective. The lossless cases of buck, boost, flyback, and DAB-based converters are discussed, along with connection realization rules and an explanation of why a lossless DAB cannot be connected in an ISOP or IPOS configuration in theory. Experimental results regarding DAB in the context of multi-cell converters validate the proposed theory and its advantages.

In *Chapter 5*, the challenges of filter design in multi-cell converters are addressed through a parameter derived from the conventional insertion loss (IL) parameter, detached from the power converter topology. The objective is to comprehend and compare the attenuation of DM noise for input parallel (IP) and input series (IS) connection configurations. It is demonstrated that IS connections degrades DM attenuation performance, and an energy equivalent methodology is insufficient for achieving desired attenuation performance. Approximating the insertion loss equations allows for deriving equivalent performance for IP and IS configurations. Regarding CM noise, the chapter highlights the difficulties faced by the IP configuration in reducing CM noise through conventional filtering design. An innovative solution involving a 180° interleaving technique is provided, effectively suppressing CM noise and transforming inter-cell interference into an EMC solution.

Lastly, *Chapter 6* is dedicated to the radiated field of an entire PCA. It begins by presenting a simple analytic algorithm based on Biot-Savart's law for studying the near radiated field o the interconnections of multi-cell converters as passive elements independent

of the power converter in operation. Then, the chapter then explores the correlation between experimental near-field measurements using near-field probes and a transverse electromagnetic cell (TEM) and electrical parameters/performance, such as ZVS realization. It demonstrates the potential for EMC improvement through early-stage pre-compliance platforms capable of identifying EMI challenges.

To summarize, this thesis encompasses several key topics: (i) the dimensioning of a Dual Active Bridge within the context of a modular converter, with a specific focus on enhancing EMC performance, predictability, and improvement; (ii) a comprehensive exploration of the fundamentals surrounding Modular/Multi-cell/Power Converters Arrays; and (iii) the prediction and improvement of EMI signature, including near field analysis, along with an examination of various aspects related to EMC.

1. Multi-cell converters: an opportunity for automated design regarding EMC

In order to familiarize the power electronic engineer reader, basic concepts of EMC and EMI signature of a power converter are presented. The concepts are useful for better comprehending the following chapters.

The first subsection of this Chapter is a general literature review and introduction on EMC related to power converters. The reader will be able to be in contact with up to dated definitions of EMI noise, model/predictability and mitigation for EMC compliance. New and common methods and technology for empirically observe the EMI signature and improvement are also presented.

In the second part of this Chapter, the motivation of this thesis, through the use of the multi-cell approach for acquiring EMI signature is presented, and subsequently, an opportunity for design manufacture automated design.

1.1 Brief review of EMC for Power Electronics

Power electronics is a field that deals with the switching of *dv/dt, di/dt* through switching devices, which is often trendily increasing with the advance of Wideband gaps (WBG) semiconductors devices. The connection with the mains (AC – 50, 60Hz) or even with other equipment in a DC grid raise awareness over the power quality and safety that should not interfere up to the point of damaging or interfering with the surrounding (equipment or living creatures). Therefore, the concept of Electromagnetic Compatibility [16] is essential and mostly mandatory for any commercial electric/electronic equipment, and can be, ordinarily, divided into Emission or Susceptibility as presented in *Figure 1.1*. The topics highlighted in black are the ones concerned to this thesis.

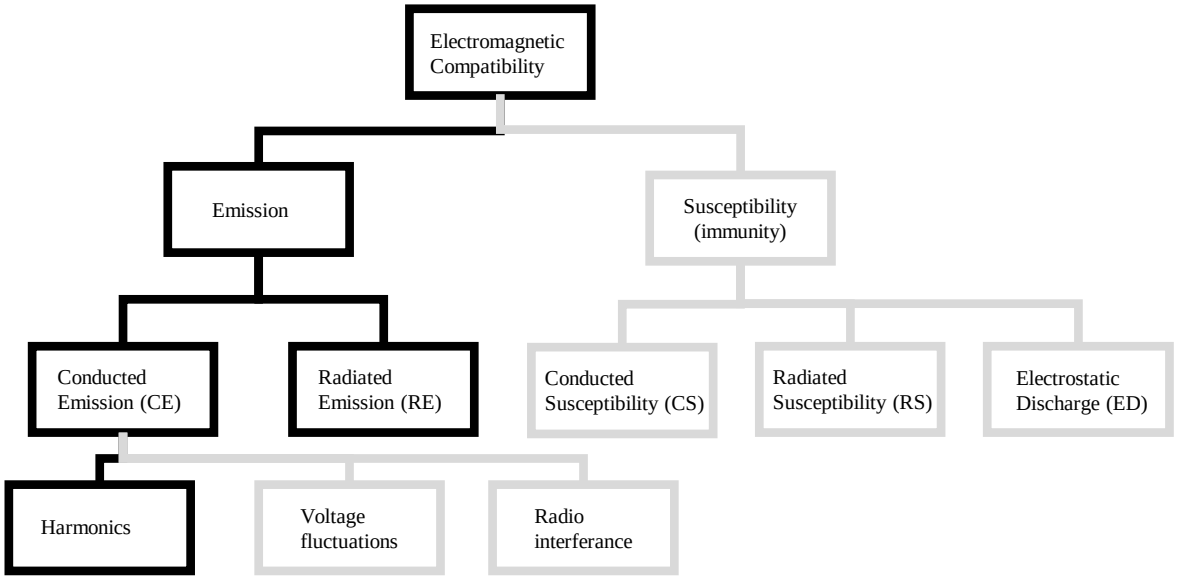


Figure 1.1 Classical subdivision of EMC categories. Content inspired by [16].

For the purpose of this work, the conducted emission (CE) is the most important point of discussion and study. Usually, they are often the first worrying EM compatibilities, as treating them in early stage is cheaper, easier and are directly related to the other EMC categories. The need of knowledge and EMI education at early stage is also justified by cost and time spending for certifying equipment, as presented in *Figure 1.2*. As it can be seen, not treating EMI issues at initial stages may result in time and cost consuming projects.

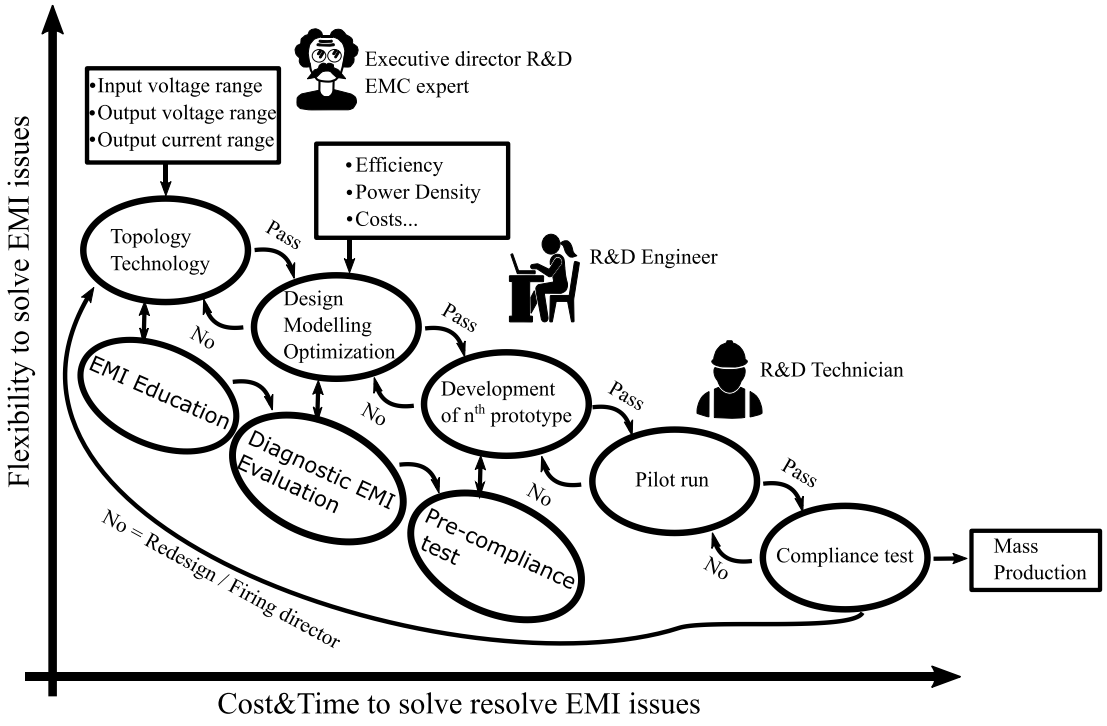


Figure 1.2 Conventional and advisable EMI tasks in parallel with DC/DC power converter design for EMC certification. Content inspired by [17].

Previous work at G2Elab, the development of the DC/DC power converter prototype (Topology technology - Design and optimization – Development of the n^{th} prototype) had been made without the two initial phases (i) EMI education; and (ii) Diagnostics and EMI evaluation.

The goal of this work is, therefore, to provide enough knowledge for performing the following group of tasks:

i. Topology Technology;
ii. Design, Modelling and Optimization;
iii. Development of the nth prototype.

While performing the second group of task:

i. EMI education;
ii. Diagnostic EMI evaluation;
iii. EMC Pre-compliance testing.

Meanwhile, the goal of sub-section 1.1 is to provide, briefly, the fundamentals of EMC regardless of the DC/DC converter topology. In depth analysis specifically for the DAB are presented in the following Chapters.

1.1.1 Regulation and compliance on Emission

To conserve and ensure the integrity, safety and quality of energy, signals and information, different mandatory regulating standards and certifications [18], [19] are imposed depending on the application (Aircraft, Spaceship, military and defence, household and industrial appliances) and the location (European, USA, among others). For the context of this thesis, the applications of the DC/DC prototype, made of DABs, are open / undefined. However, a common limit regulation found on most literatures is the EMI standards for IT and Multimedia ruled by the well-known CISPR/EN 55022/32, which is measured in 50 uH/ 50 Ohms system, ranging from 150 kHz up to 30 MHz for Conducted Emission (CE) and from 30 MHz up to 40 GHz for Radiated Emission (RE). It is an updated version from the CISPR 22. In *Figure 1.3*, it is presented the CE (red) and RE (blue) limits for CISPR/EN 55022/32 Class B (Quasi-peak detector) intendent for residential purposes. Such CISPR/EN 55022/32 Class B standard is used as guiding limits throughout the work presented in this thesis.

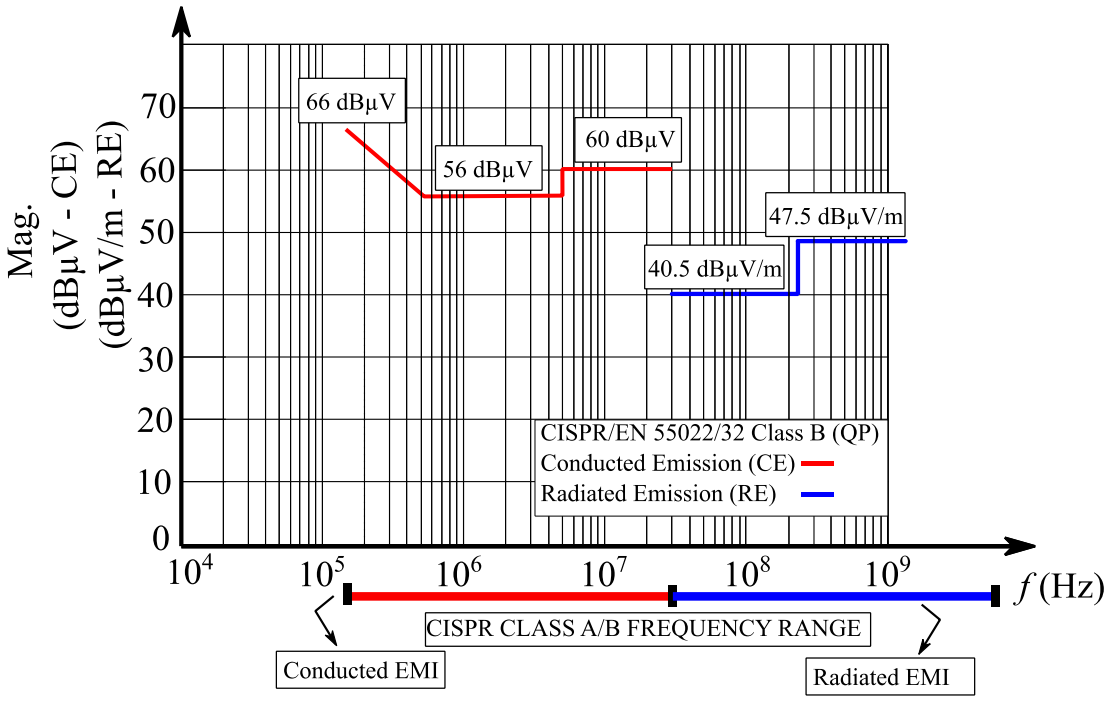


Figure 1.3. Limits of CISPR/EN 55022/32 *Class B: (red) Conducted Emission; (blue) Radiated Emission.*

Finally, one should be aware that the tendency is to increasingly impose more limits and restriction due to the advancing technology and concepts allied with Internet of Things (IoT) and data safety allied with power electronic devices penetration.

1.1.2 Equipment and setup testing

It is important to differentiate an EMC compliance testing from the EMC pre-compliance testing. Compliance testing must be accurate, precise, follow strict rules as well as certified; and are implemented as a final EMC testing. The EMC compliance test tries to reduce as much as possible uncertainties, which is itself subjected to standards (e.g IEEE/ANSI C63.4-2014) and must be quantified. An official electromagnetic emission compliance report in [20], presents an uncertainty of ± 1.92 dB for CE and up to ± 5.32 dB for RE. This means that a relative error of around 100% might occur. It is important to notice that an EMC certificating test does not intend to describe exactly the EMI signature, but rather an image in which directives should be followed to assure standard, repetitiveness and faster results. A difference as large as 10 dB for example might be found between the real FFT of a signal and the results after passing through the Spectrum Analyser and its different detector methods (Quasi-peak, Peak, RMS, Average, Max Peak, Min Peak). If the objective remains

only accuracy matching between theoretical and practical results, the studies may be cumbersome and time consuming, since uncertainty measurement is absolutely required, or even vicious with a large amount of variables and very specific curve fitting. Indeed, when considering the uncertainty of measurement, component tolerance and worst case, a margin of up to 16 dB was considered for the EMI filter design (representing 8% of the total volume) of a Telecom power supply application (98% efficiency and 2.2kW/dm3) presented in [21], while others consider a margin of 10 dB.

Even though pre-compliance testing should be as rigid as possible to ensure precision and avoid unintended coupling, they are less strict, cost less and should be used during the earlier stages, privileging precision rather than accuracy. New and inexpensive techniques may be used for the sake of qualitative and comparative results. In this regard, as much of the work is dedicated for reducing EMI signature among different configurations and possibilities, pre-compliance testing are used throughout this work. The EMC compliance testing, many methods and set of equipment are used, as presented in *Figure 1.4.*

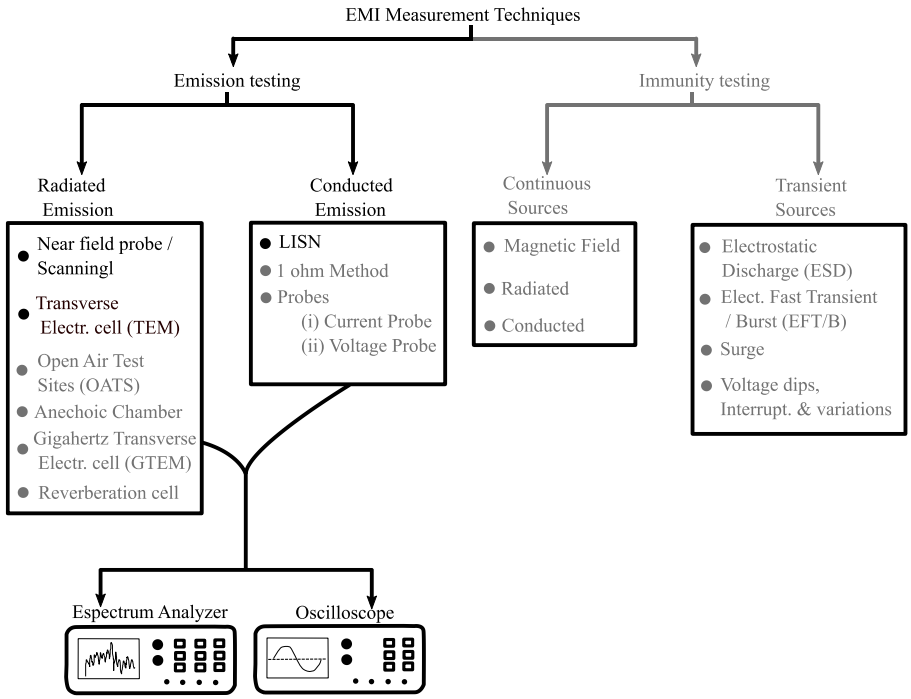


Figure 1.4 EMI measurement techniques. Content inspired by [17].

In general, the two most important equipment are the LISN (together with its CM and DM rejection [22].) and the Spectrum Analyzer / EMI Receiver. The experimental results presented in this thesis are performed with an LISN [23], spectrum analyzer [24], [25], [26], [27], TEM cell [28] [29], and near field probe. It is important to notice that all EMC equipment should pass through calibration and verification [30], which is not often the case

for the testing equipment in this thesis, increasing the uncertainty even further. For better details and understanding of each of the used equipment, please refer to Appendix 1.A

1.1.3 Differential mode (DM), common mode (CM) and mixed mode (MM) conducted emission definition

Besides the circulating current in which Power Electronic engineers are used to deal with to guarantee acceptable input/output voltage and current ripple at, respectively, voltage and current source devices, known as Differential Mode (DM) current, another type, coupled by parasitic capacitance with respect to ground and defined as Common Mode (CM), is extremely important when passing the CE standards.

More complexity in the case where the system is not balanced, either downstream or upstream of a port-network system, may also cause what is called Mixed Mode (MM). Such impedance asymmetries can be handled and known in the lower frequency, but can be complicated to handle it in the very high frequency range.

In this thesis, the definition presented in [31] of DM, CM and MM is used. It is a generalized Differential-Common-Mode (*dcm*) decomposition for modelling conducted emission in asymmetric converter structures, such as half-bridge multi-chip power module [32]; wide bandgap-based converters [33]; and derive equivalent circuits to model CM current in an entire micro-grid [34], lumping them together, including CM equivalent for a generic machine, DC bus/transmission lines, three-phase active rectifier and three-phase inverter. The impact of asymmetry becomes even more evident in groundless structures as presented in [35], which is demanded by certain safety regulations. More about impact on symmetric path such EMI filter [36], [37]. As such proposed theory allows not only definition of CM, DM and MM noise, but also a powerful method for deriving and building simplifying equivalent circuits, it will be presented a brief review based on [31]. While the approach allows drawing simplified equivalent circuits to get insights, other definition based on 4-port network theory [38] is better suited for studying EMI filter through Vector network analysers (VNAs).

As presented in Figure 1.5, it is presented a diagram for generic DM and CM and decomposition for introducing definition. As it can be seen CM and DM are defined with respect to an arbitrary floating reference, distinct from ground, facilitating systematic piecemeal transformation of MM system components. Therefore, the generic system presented in Figure 1.5 can represent a filter line, transmission line, electric machine of N phase, a half-bridge structure, DC grid and etc [34]...

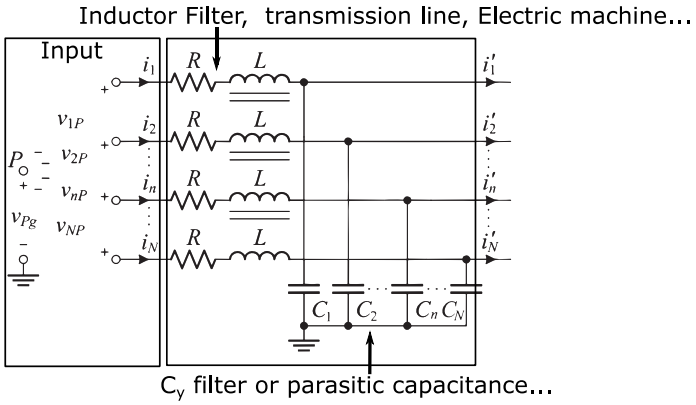


Figure 1.5 Diagram for DM and CM definitions and decomposition demonstration of a N line system. Adapted from *[31]*.

The definition of CM current and voltages are presented, respectively, in (1.1) and (1.2)

$$i_{cm} \triangleq \sum_{n=1}^{N} i_n \tag{1.1}$$

$$V_{cm} \triangleq \frac{1}{N} \sum_{n=1}^{N} v_{nP}. \tag{1.2}$$

The definition of DM currents and voltages are presented, respectively in (1.3) and (1.4)

$$i_{mn} \triangleq \frac{1}{2}(i_m - i_n) \tag{1.3}$$

$$v_{mn} \triangleq v_{mP} - v_{nP.} \tag{1.4}$$

Therefore, it is possible to put together the $(N-1)$ DM definitions and one CM definition, lumping together into a $N \times N$ linear transformation, called decomposed differential-common-mode (*dcm*), of voltages (1.5) and currents (1.6)

$$\mathbf{v}_{1\ldots N}^{\boldsymbol{dcm}} \triangleq \mathbf{T}_N^{\boldsymbol{v}} \mathbf{v}_{nP} \tag{1.5}$$

$$\mathbf{i}_{1\ldots N}^{\boldsymbol{dcm}} \triangleq \mathbf{T}_N^{\boldsymbol{i}} \mathbf{i}_n. \tag{1.6}$$

Where $\mathbf{v}_{1\ldots N}^{\boldsymbol{dcm}}$ and $\mathbf{i}_{1\ldots N}^{\boldsymbol{dcm}}$ are the vectors of DM and CM voltages and currents, respectively. For a two-line system and three-line system, the transformations matrixes $\mathbf{T}_N^{\boldsymbol{v}}$ (1.7) and $\mathbf{T}_N^{\boldsymbol{i}}$ (1.8) are defined by 2×2 and 3×3 dimension matrixes, respectively (refer to [31] for generalized $N \times N$ version)

$$\mathbf{T}_2^v = \begin{pmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{pmatrix};\ \mathbf{T}_3^v = \begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{pmatrix} \tag{1.7}$$

$$\mathbf{T}_2^i = \begin{pmatrix} \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 \end{pmatrix};\ \mathbf{T}_3^i = \begin{pmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & 1 \end{pmatrix}. \tag{1.8}$$

Such definition is in agreement with a 2-phase system presented in [39], which results in the simplifying known definitions of and CM and DM voltages and current (1.9)-(1.12). Please, note that depending on other definitions by different school of thoughts and measuring systems, the definition of CM and DM may linearly vary by a difference of 6 dB for example

$$i_{cm} = i_1 + i_2 \tag{1.9}$$

$$v_{cm} = \frac{v_1 + v_2}{2} \tag{1.10}$$

$$i_{dm} = \frac{i_1 - i_2}{2} \tag{1.11}$$

$$v_{dm} = v_1 - v_2. \tag{1.12}$$

Considering a more complex system with impedance path, such as filter, electric machine, half-bridge structure, etc., a matricidal decomposition of MM can be found firstly through Kirchhoff's voltage and current laws with respect to the arbitrary reference point *P* (1.13). For example, let $\mathbf{Z}_{\boldsymbol{i}_n}$ be the impedance given by the resistance and an uncoupled inductance; and $\mathbf{Z}_{\boldsymbol{o}_n}$ be the impedance of the capacitance-to-ground as presented in Figure 1.5

$$\mathbf{v}_{nP} + v_{Pg}(1 \quad \dots \quad 1)^T = \mathbf{Z}_{\boldsymbol{i}_n}\mathbf{i}_n + \mathbf{Z}_{\boldsymbol{o}_n}(\mathbf{i}_n - \mathbf{i}'_n). \tag{1.13}$$

Using the definitions in (1.5) and (1.6), the matricidal decomposition of MM is finally expressed in (1.14)

$$\mathbf{v}_{1\dots N}^{dcm} + v_{Pg}(0 \quad \dots \quad 1)^T = \mathbf{T}_N^v\mathbf{Z}_{\boldsymbol{i}_n}\left(\mathbf{T}_N^i\right)^{-1}\mathbf{i}_{dcm} + \mathbf{T}_N^v\mathbf{Z}_{\boldsymbol{o}_n}\left(\mathbf{T}_N^i\right)^{-1}(\mathbf{i}_{dcm} - \mathbf{i}'_{dcm}). \tag{1.14}$$

When using a 3×3 and considering only $\mathbf{Z}_{\boldsymbol{o}_n}$, it can represent the capacitive coupling of half-bridge, and its asymmetry can be studied [32]. Therefore, by simply analysing the matrix composing $\mathbf{T}_N^v\mathbf{Z}_{\boldsymbol{i}_n}\left(\mathbf{T}_N^i\right)^{-1}$, presented in (1.15), as well as $\mathbf{T}_N^v\mathbf{Z}_{\boldsymbol{o}_n}\left(\mathbf{T}_N^i\right)^{-1}$**,** presented in (1.16), it is possible identify whether or not MM coupling is occurring, as shown in (1.17)

$$\mathbf{T}_2^v\mathbf{Z}_{\boldsymbol{i}_n}\left(\mathbf{T}_2^i\right)^{-1} = \begin{pmatrix} \mathrm{Z}_{i1} + \mathrm{Z}_{i2} & \dfrac{\mathrm{Z}_{i1} - \mathrm{Z}_{i2}}{2} \\ \dfrac{\mathrm{Z}_{i1} - \mathrm{Z}_{i2}}{2} & \dfrac{\mathrm{Z}_{i1} + \mathrm{Z}_{i2}}{4} \end{pmatrix} \tag{1.15}$$

$$\mathbf{T}_2^v\mathbf{Z}_{\boldsymbol{o}_n}\left(\mathbf{T}_2^i\right)^{-1} = \begin{pmatrix} \mathrm{Z}_{o1} + \mathrm{Z}_{o2} & \dfrac{\mathrm{Z}_{o1} - \mathrm{Z}_{o2}}{2} \\ \dfrac{\mathrm{Z}_{o1} - \mathrm{Z}_{o2}}{2} & \dfrac{\mathrm{Z}_{o1} + \mathrm{Z}_{o2}}{4} \end{pmatrix} \tag{1.16}$$

$$\begin{aligned} &\mathbf{v}_{dcm} + v_{Pg}[0 \quad 1]^T + = \begin{pmatrix} v_{12} = v_{DM} \\ v_{CM} + v_{Pg} \end{pmatrix} \\ &= \left(\mathbf{T}_2^v\mathbf{Z}_{\boldsymbol{i}_n}\left(\mathbf{T}_2^i\right)^{-1} + \mathbf{T}_2^v\mathbf{Z}_{\boldsymbol{o}_n}\left(\mathbf{T}_2^i\right)^{-1}\right)\begin{pmatrix} i_{12} = i_{DM} \\ i_{CM} \end{pmatrix} \\ &- \left(\mathbf{T}_2^v\mathbf{Z}_{\boldsymbol{o}_n}\left(\mathbf{T}_2^i\right)^{-1}\right)\begin{pmatrix} i'_{12} = i'_{DM} \\ i'_{CM} \end{pmatrix}. \end{aligned} \tag{1.17}$$

The focus on this thesis is the *dcm*, which found by solving second line of (1.17). Notice that if the coupling path is fully symmetrical $\mathrm{Z}_{i1} = \mathrm{Z}_{i2}$ and $\mathrm{Z}_{o1} = \mathrm{Z}_{o2}$ in the entire frequency range, the resulting matrix is diagonal, and therefore, the DM and CM are decoupled. In practice, the tolerance of components, routing design, filter placing (e.g. at one phase), grounding (which short circuit capacitance-to-ground at one phase) may result in slight or large difference impedances: $\mathrm{Z}_{i1} \neq \mathrm{Z}_{i2}$ and $\mathrm{Z}_{o1} \neq \mathrm{Z}_{o2}$. Besides, even at the slightest parameter variation, the MM coupling is well visible in the resonances with high

oscillations and high quality factor equivalent circuits, as the difference in impedances are radically changing due to difference in resonance frequency and phase.

Thus far, a general overview has been provided on how the coupling path can impact the differential-mode (DM) and common-mode (CM) noise in a 2-phase system. Understanding the formation of DM and CM noise sources in a converter is crucial to proactively address the issue at its root. Although EMC standards do not distinguish between them, having knowledge of these sources is important for determining appropriate actions such as filter design, adjusting the gate driver to slow down the slope, employing parallel capacitances, impedance matching, symmetrization, PWM (Pulse Width Modulation), synchronization, PCB routing improvements, and other relevant measures.

To identify the noise sources and capture the EMI signature, it should be initially assumed that there is complete symmetry between the input and output of power converters in theoretical terms. It is crucial to minimize the number of cascaded connecting systems, such as loads, filters, and lines, to prevent coupling and avoid a multitude of parameters that are difficult to control. In [35], a methodology for EMI characterization is presented, involving the placement of two LISNs (Line Impedance Stabilization Networks) at the input and output ports, as illustrated in *Figure 1.6* of the schematic of an H-bridge structure. This setup should be conducted either empirically or theoretically to draw conclusions about both input and output noise. By assuming that the mixed-mode (MM) coupling caused by external propagating paths is negligible or neglected due to an ideal LISN, the primary noise sources can be identified, in which meaningful insights can be gained.

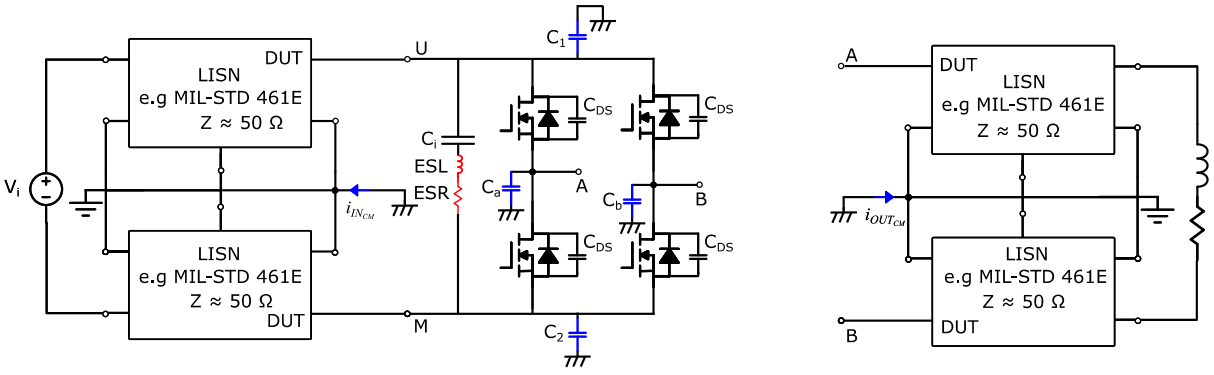


Figure 1.6 Schematic of an H-bridge converter as used for EMI characterization. Content inspired by [35].

Once well isolated from other unknown cascaded noise sources, it is possible to describe and define the noise produced exclusively by the power converter. In this thesis, the input noise is the main focus and needs to adhere to EMC standards. The explanation of main

DM and CM noise sources and coupling paths presented here are based on [39]. In *Figure 1.7* depicts the equivalent representation of these noise sources and propagation paths: inside the red dashed box, the DM noise, $i_{s,DM}$, intrinsically mitigated by the impedance Z_b, that can the equivalent impedance (all in parallel) of the DC-link capacitor C_i, snubber and further DC-bus parasitic capacitances; whereas inside the blue dashed box, the CM noise, $v_{s,CM}$, which can be considered as an equivalent Thevenin voltage, coupled by the impedance's phase $Z_{s,U}$ and $Z_{s,M}$ which is capacitive thorough the entire CE frequency range, as further better explained.

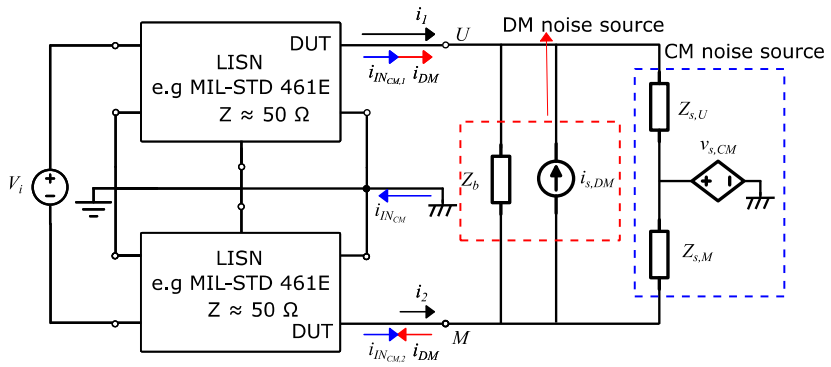


Figure 1.7 HF equivalent of the CE measurement circuit. Content inspired by [39].

1.1.3.1 Comprehension and modelling of Differential Mode EMI noise source and propagation path

The DM current, as mentioned earlier, is the typical current that power electronic engineers deal with. Therefore, it can be confidently stated that DM noise manifests as current sources. The literature discusses whether the natural behaviour of DM noise can be accurately represented by a pure current source, which remains an "open question" as stated in [39]. *Figure 1.8* presents a simplified circuit for decoupling the DM noise source, which has been previously utilized with satisfactory results in [40] at G2Elab. In this circuit, the LISN can be approximated as a simple resistance, either 100 ohms or 50 ohms, depending on its type, for the sake of simplification. The equivalent circuit representation aligns well with the idea that certain power converters, such as DAB in this thesis, require a DC-link capacitor placed as close as possible to the power source, which exhibits a current-like source nature. It is important to note that depending on the specific topology, the DM noise should be considered as voltage sources connected through an inductor. This is particularly applicable in the case of AC/DC converters where the AC side is treated as the input connected through inductors, e.g L_i to an H-bridge (inverters).

(a) (b)

Figure 1.8 Simplified DM noise measured in simplified high-frequency equivalent system: (a) a noise source represented by a current flowing through a DC-link capacitor; (b) a noise source represented by voltage fluctuations coupled through an inductor, commonly observed in AC/DC converters. Content inspired by [39] and [41].

Indeed, the DM noise can be described as being the current caused by the *dv/dt* across a known inductance. Describing and addressing DM noise is, therefore, generally not challenging, especially for lower frequencies. The required attenuation is typically based on the first harmonic appearing in the conducted emissions (CE) frequency range. A preliminary estimation solution involves calculating or measuring the root mean square (RMS) current circulating in the power converter and assuming that it contains the necessary information and energy for DM filter design. In [42], this approach was applied to an AC/DC converter (boost power factor correction) with an acceptable positive error of around 3-6 dB, indicating a slight over-dimensioning in the filter design. The same procedure can be applied to any DC/DC converter. The AC circulating RMS current noise value $\left(I_{s,DM\ rms}\right)$ can be calculated according to equation (1.18), being a function of the total RMS current $\left(I_{in,rms}\right)$ and the input average current $\left(I_{in}\right)$

$$I_{s,DM\ rms} = \sqrt{I^2_{in,rms} - I^2_{in}}\ . \tag{1.18}$$

Once the noise amplitude has been extracted, the next step involves determining the frequency at which it needs to be filtered according to the specified standards (e.g., > 150 kHz). Two crucial considerations need to be addressed with regards to the power converter topology. In cases where the converter topology is based on single switching cells like buck, boost, etc., the noise appearing at the input is a multiple of the switching frequency, with the fundamental frequency located at $1f_s$. However, if the topology is based on H-bridge structures such as Full-bridge, DAB, etc., the noise appearing is a multiple of the apparent or equivalent switching frequency, which is twice the switching frequency, with the fundamental

frequency located at $2f_s$. If the fundamental frequency falls within the range of 150 kHz to 30 MHz, the filter can be designed based on the amplitude mentioned in equation (1.18). In the case of the DAB presented in this thesis, with a switching frequency (≥ 100 kHz), its fundamental frequency (≥ 200 kHz) is certainly located within the CE frequency range.

On the other hand, if the fundamental frequency of the noise falls below 150 kHz (applicable to power converters with lower switching frequencies), an additional estimation step is required. This estimation is based on the envelope of known waveforms, such as rectangular and triangular waveforms shown in *Figure 1.9*. The choice of waveform depends once again on the power converter topology and operating points. Considering the envelope due to a square-waveform is a conservative and useful approach, but it may lead to an over dimensioned filter. Conversely, if a triangular waveform, which is more commonly encountered in power converters, is assumed, the filter could be underestimated. In such cases, it is important to accurately determine the shape and its envelope for improved accuracy. An approximation specifically for the DAB under SPS modulation is presented in *Chapter 2* to address this issue.

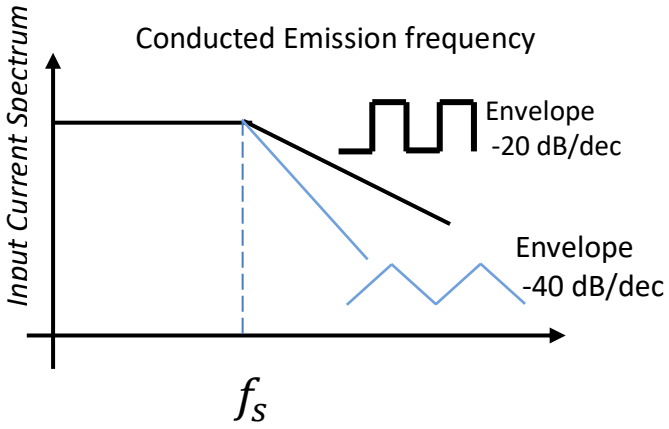


Figure 1.9 Typical shape of an input current spectrum: (a) its envelope based on square or triangle; (b) a typical shape as presented in [42].

As mentioned earlier, the DC-link capacitance plays a crucial role in the operation of a power converter. It is typically sized not only to ensure compliance with EMC regulations but also to control voltage ripple within acceptable limits. Consequently, a significant portion of the conducted differential-mode (DM) current is effectively attenuated by the DC-link capacitor. However, there is still a remaining portion that requires additional attenuation to meet EMC requirements.

1.1.3.2 Comprehension and modelling of Common Mode EMI noise source and propagation path

Based on *Figure 1.7*, supposing an equivalent capacitive propagation path, a simplifying equivalent circuit that represents the CM noise is presented in *Figure 1.10*. It is represented by an equivalent Thevenin voltage noise source $v_{s,CM}$, and an equivalent thevenin impedance coupling, which is general capacitive (with a magnitude vary from pF to nF depending on the device and application) for the CE frequency range. Therefore, an important assumption, useful for *Chapter 5* is made: the CM noise of any power converter can be modelled by a given Thevenin equivalent noise sources and impedance paths.

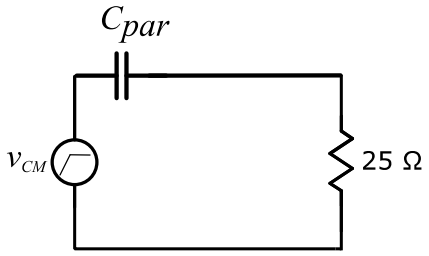


Figure 1.10 Simplified CM noise as a voltage source and measured in simplified high-frequency equivalent system.

The CM current flows through unintended parasitic capacitance to the ground ($i = C\frac{dv_c}{dt}$) along an electric circuit. It is therefore necessary to identify the electric points in which there is a sudden change in voltage and large surface area with respect to ground. In general, with the increasing in switching frequency, switching transitions and compactness, the CM noise can be said to be the most challenging to describe, predict and mitigate. The capacitive coupling ($C\frac{dv_c}{dt}$) has a lower impedance with the increasing frequency, occupying a large band on the CE frequency range.

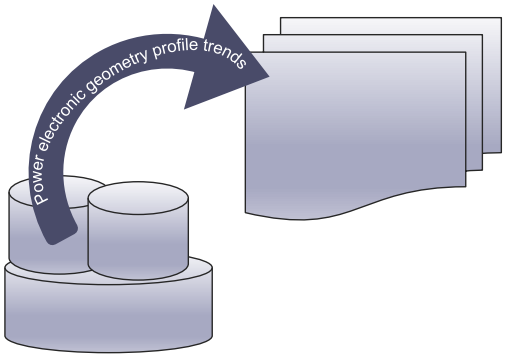


Figure 1.11 Trending geometry profile of power electronic devices.

This means that the 20 dB/dec decay of the noise source is not enough to attenuate the CM current and it seems "constant" until 40 dB/dec, as possible to observe in Figx. This usually demands effective attenuation losses with cascaded or bulky filters. For that reason, different from DM noise, only the first harmonic located at the CE frequency range is not enough. Besides, due to same direction displacement current orientation, they contribute positively to the increase of radiated field, as it will be further better explained.

It is also possible to calculate the RMS value of CM noise to draw important conclusions on the required CM noise attenuation [8] (boost interleaving), but it is not advisable, as the authors concluded. As previously mentioned, the harmonics are contained in a large range of the CE. This means that, it is indispensable to understand the behaviour of a typical voltage noise source in the frequency domain in a power converter. As it can be observed from Figure 1.10, the CM noise are caused mostly by voltage sources. In general, the noise sources can modeled by trapezoidal waveforms superposed with ringing and "recovery energy". For simplifying purposes, a symmetric trapezoidal (equal rise and fall times) waveform, duty cycle of 50% can be used to model the voltage noise source.

A brief review is presented on the Fourier series theory in order to situate the reader with respect to the spectrum magnitude of a symmetric trapezoidal waveform. The normalized spectrum of a generic trapezoidal waveform $\bar{x}(t)$ is presented in (1.20) and its reconstruction in the time domain is presented in (1.19). It is noticed that for the particular symmetric trapezoidal wave, the even harmonics are ideally zero, consisting only on odd harmonics in the spectrum domain (f_s, $3f_s$, $5f_s$…). Therefore, different from the DM noise, the CM noise is mostly and often contained in odd harmonics. As an equivalent noise is composed of linear combination of other trapezoidal waveforms, it can be assumed that the equivalent CM noise will most likely to present same odd harmonics. Equation (1.20) can be heavy for computation and hard to get insights, and therefore, the envelope curve (1.21) is presented by replacing nf_s with a smooth frequency variable f. Further observations and simplification of sinusoidal properties result in the spectrum magnitude as presented in (1.22), which will be preferred for analysis in *Chapter 3* due to its simplicity

$$\bar{x}(t) = \frac{1}{2} + \sum_{n=0}^{\infty} C_n \cos(2\pi n f_s t + \theta_n) \tag{1.19}$$

$$C_n \angle \theta_n = \frac{\sin(n\pi/2)}{n\pi/2} \frac{\sin\left(n\pi f_s t_{rise,fall}\right)}{n\pi f_s t_{rise,fall}} \angle \left(-n\pi \left(\frac{1}{2} + f_s t_{rise,fall}\right)\right) \tag{1.20}$$

$$C_{nEnv1} = \frac{1}{\sqrt{2}} \left| \frac{\sin(\pi f / 2f_s)}{\pi f / 2f_s} \right| \left| \frac{\sin(\pi f t_{rise,fall})}{\pi f t_{rise,fall}} \right|, f = f_s, 2f_s, 3f_s \ldots \quad (1.21)$$

$$C_{nEnv2} = \begin{cases} \frac{1}{2\sqrt{2}} \text{ if } f \leq \frac{2f_s}{\pi} \\ \frac{\sqrt{2}f_s}{\pi f} \text{ if } \frac{2f_s}{\pi} \leq f \leq \frac{1}{\pi t_{rise,fall}} \\ \frac{\sqrt{2}f_s}{\pi^2 f^2} \frac{1}{t_{rise,fall}} \text{ if } f \geq \frac{1}{\pi t_{rise,fall}} \end{cases}. \quad (1.22)$$

Such equation presents important information on the magnitude spectra and its dependence on switching frequency and rise/fall time. As it can be seen, the decrease (in dB) is at a rate of -20 dB/decade starting at the first breaking point f_s due to a *1/f* decrease of magnitude; and at a rate of -40 dB/decade as of a second breakpoint due to a *1/f* ^{2} decrease of magnitude.

In *Figure 1.12*, it is presented as an example the impact of switching different switching frequencies (10 kHz, 100 kHz and 500 kHz) and *dv/dt* (10 ns and 100 ns) on the spectrum magnitude content. As it can been seen, the *dv/dt* and f_s are variables that are trendily increasing, while EMI compliance becomes an important factor to be account from the initial phases of designing a power converter. The switching frequency impact both on lower (conducted) and higher (radiated) frequency range of CISPR Class A/B, while the rise/fall time impacts on the higher frequency range (end of conducted emission range up to radiated emissions).

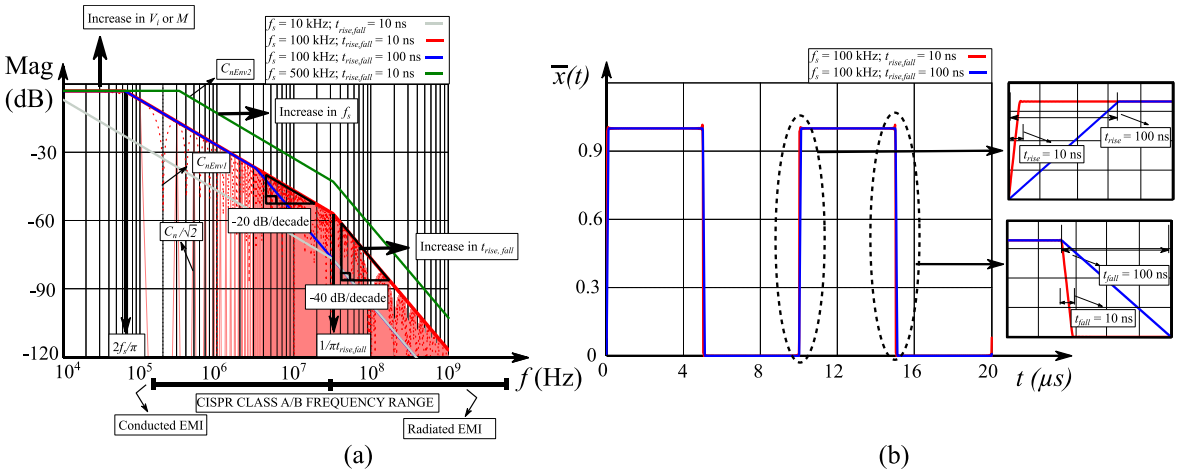


Figure 1.12 EMI measurement techniques. Content inspired by [17].

Identifying previously the CM noise before prototyping is, therefore, desirable. This passes, necessarily through parasitic capacitance extraction, which can be carried out using

analytical, empirical, or physical models based on FEM or PEEC. Within a switching cell, one of the significant parasitic elements is the parasitic capacitance to ground, along with the parasitic inductances that make up the switch cell. Initially, the focus should be on the parasitic capacitance to a perfect ground (assuming no inductance) for a first-order solution. Typically, during the design phase, efforts are concentrated on reducing parasitic inductances to improve DM behaviour and efficiency, achieved by compacting structures and ground planes. However, this often leads to an increase in parasitic capacitances. Thus, a trade-off exists between these two elements, requiring the designer to be aware of them simultaneously. Instead of solely reducing one or the other, designers should prioritize addressing resonances, strategically placing the resonance frequency and known amplitude to comply with EMC standards. Nevertheless, this thesis primarily focuses on the parasitic capacitance to ground. The simplification of parallel plates between any electrical point and a ground mass (such as a ground plane, heatsink, chassis, etc.) should not be disregarded due to its simplicity. Although it involves further simplifications, it can provide a worst-case scenario estimation of the maximum capacitance to ground [41], as depicted in *Figure 1.13*. The concept involves representing a power converter by its surface board area separated by air at a distance dictated by the application. In other words, the assumption collapses all electrical points into one, creating a path for the CM equivalent noise source. While this is an oversimplification, it remains a conservative first-order solution for worst-case scenarios caused by CM currents. Notably, trends in power converters, such as low profile designs and larger surface areas, contribute to increased challenges related to CM noise.

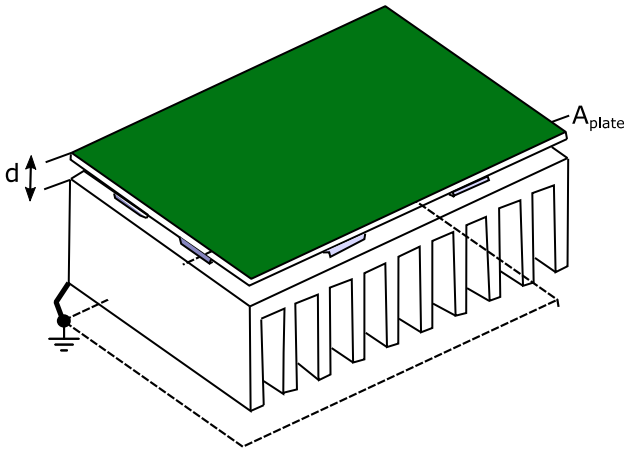


Figure 1.13 Approximation for estimating a maximum common mode capacitance of a board and a grounded mass. Adapted from [41].

Regarding the simplified model depicted in *Figure 1.13*, it may be suitable for the lower frequency range worst-case scenarios and possibly designing an over-dimensioned EMI

filter. However, it does not facilitate optimization of the power converter or the reduction of its noise sources.

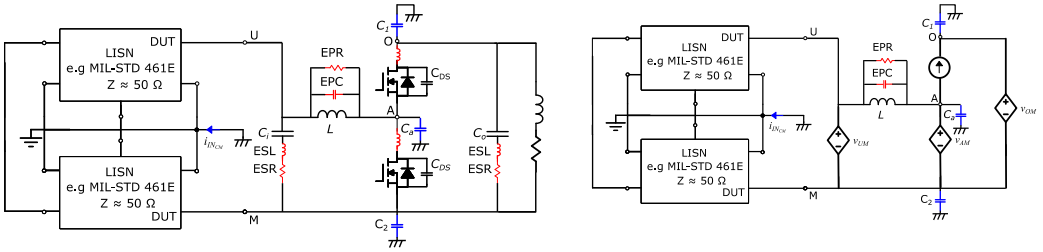
Another simplifying empirical method involves offline measurements (when the converter is not operating) of the electrical points using RLC meters or impedance analyzers. This approach has been utilized in [43], revealing a capacitive behaviour across the entire CE frequency range (up to 30 MHz) with magnitudes on the order of pF.

After parasitic extraction from the most important parameters, the designer may use switched models, such as performing numerical simulation using software's, e.g MATLAB/Simulink, PSIM, SABER, LTspice, [44], [45], presenting a fairly good results (difference up to 11 dB presented in [44]) when comparing to practical results. On the other hand, they are time-consuming since low step times are necessary for detailing the switching transitions and also because transitory regime may occupy a lot of memory and information, not useful for EMC analysis, until steady-state is reached. The required inclusion of LISN turns this task even heavier. After signal acquired through time analysis, it must still passes through FFT, DFT, or any EMI receiver emulation. They are less intuitive to perform improvement at the noise source level, and usually are used for complying with EMC standards after a first prototype is made, by including external elements, such as conventional EMI filter (three cascaded stages) [9], [45]; resonance peak reduction (which requires knowledge on equivalent circuits for different frequency ranges; or any trial and error, iterative techniques. Indeed, even though such techniques are extensively used in academic and industry for CM attenuation, it is still very specific and should not be considered as the most optimum result, but rather as the last method after design phase.

To solve the issue of time in simulation, or to be able to acquire the CE EMI signature in practice with online measurement [46], it proposed the "black box" in [47], also known as behavioural model [48]. On the other hand, important information about the noise source may be intrinsically lost, from which the designer may not be able to act on the design phase.

If at one hand, as presented in *Figure 1.13*, there is an oversimplified system and at the other hand over complexified system of time-domain analysis, or another powerful and simple, but supressing information as in "black box", there is a reasonable good way of modelling a power converter through substitution theorem, by substituting conveniently any branch, mainly switch devices, by known voltage and current sources [49], [50], [51], [52] described in the spectrum domain. In *Figure 1.14*, it is presented a boost converter with its main parasitic elements as well as it simplification. Such simplification allows further use of superposition theorem in order to obtain EMI signature, highlighting naturally the main parameters and path affecting CM noise. It also allows the designer to effectively tackle and

reduce CM noise through different techniques, such as symmetrisation, impedance balancing, Wheatstone bridge, shielding, and even the preferred winding transformer termination in the case of isolated DC/DC converters.



(a) *(b)*

Figure 1.14 (a) Boost converter including parasitics; (b) Substitution of MOSFET, input capacitor and output load with voltage sources, and the diode with a current source. Content inspired by [50].

Concerning H-bridge structures with no inner phase-shift, which is the case of the DAB operating with SPS modulation, it is interesting to notice that it is itself, in theory, intrinsically symmetric, as the potential variation of one of each leg is complementary to the other. In this case, each disturbance source should "see" the same impedance and creates identical currents but of opposite directions. We are faced with specific behaviour where the common mode disturbances created by one of the disturbance sources are compensated by the other [49]. In reality, the presence of CM noise is observed through experimental results in this thesis and other literatures. It is, therefore, necessary the CM noise mechanism, considering a complete asymmetric structure.

As it will be interesting for *Chapter 3* to generate a CM model of the DAB, and it is still a generic procedure for CM noise model in any power converter based on Half-bridge [31], [32], the noise generated by an H-bridge is then described. In *Figure 1.15*, the CM noise is separated into an input, due to DC-bus parasitic capacitance (circled in green - left) and output, due to the midpoint voltages, or switching nodes, of the H-bridge (circled in light blue - right). Only the input side CM noise model is demonstrated, whereas the output side CM noise can be systematically performed.

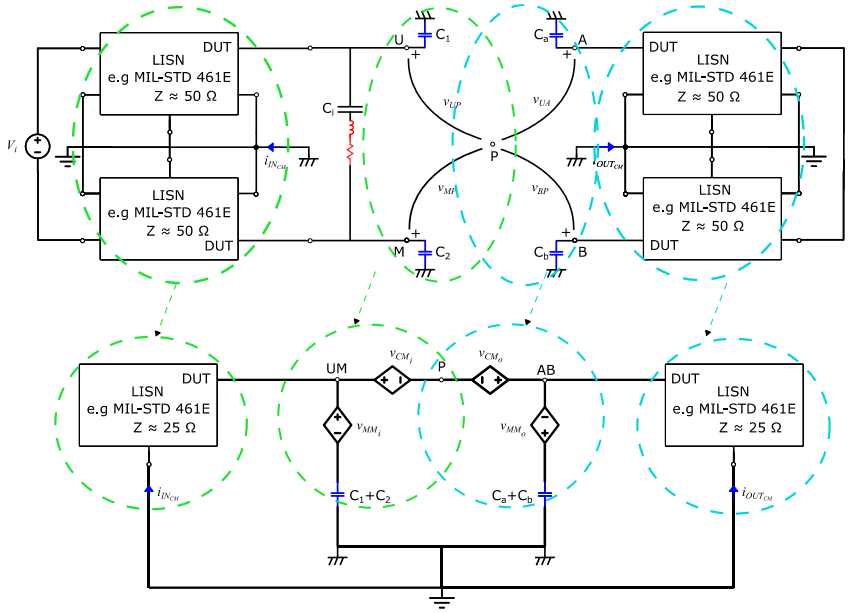


Figure 1.15 H-bridge EMI characterization and modelling with unbalanced parasitic capacitors.

The input CM noise v_{CM_i} is simply derived through the definition in (1.2), as presented in (1.22)

$$v_{CM_i} \triangleq \frac{1}{2}(v_{\mathrm{UP}} + v_{\mathrm{MP}}). \tag{1.23}$$

By considering $(\mathrm{Z}_{i1} = \mathrm{Z}_{i2} = 50\ \Omega)$ in (1.15)**,** it is easy to see that that two identical LISNs (50 Ω) connected as an input of a 2-phase system results in no MM as well as an input impedance equal to 25 Ω, as presented in *Figure 1.15* (see LISN input and output sides).

For the input analysis, let v_{CM_i} substitutes v_{CM} in (1.17) .Since the impedance matrix is capacitive, following (1.16)**,** let $\frac{\mathbf{S}'}{\mathrm{p}}$ be defined by $\mathbf{T}_N^v \frac{\mathbf{S}'}{\mathrm{p}} \left(\mathbf{T}_N^i\right)^{-1}$, as presented in (1.24), which is then substituted in (1.17) and solving second line, resulting in (1.25)

$$\frac{\mathbf{S}'}{\mathrm{p}} = \frac{1}{\mathrm{p}}\begin{pmatrix} \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 \end{pmatrix}\begin{pmatrix} \frac{1}{\mathrm{C}_1} & 0 \\ 0 & \frac{1}{\mathrm{C}_2} \end{pmatrix}\begin{pmatrix} 1 & -1 \\ \frac{1}{2} & \frac{1}{2} \end{pmatrix}^{-1} = \frac{1}{\mathrm{p}}\begin{pmatrix} \frac{1}{\mathrm{C}_1}+\frac{1}{\mathrm{C}_2} & \frac{1}{2}\left(\frac{1}{\mathrm{C}_1}-\frac{1}{\mathrm{C}_2}\right) \\ \frac{1}{2}\left(\frac{1}{\mathrm{C}_1}-\frac{1}{\mathrm{C}_2}\right) & \frac{1}{4}\left(\frac{1}{\mathrm{C}_1}+\frac{1}{\mathrm{C}_2}\right) \end{pmatrix} \tag{1.24}$$

$$v_{CM_i} + v_{Pg} = \frac{1}{2\mathrm{p}}\left(\frac{1}{\mathrm{C}_1}-\frac{1}{\mathrm{C}_2}\right) i_{12} + \frac{1}{4\mathrm{p}}\left(\frac{1}{\mathrm{C}_1}+\frac{1}{\mathrm{C}_2}\right) i_{CM}. \tag{1.25}$$

As explained in [31], the representation in terms of current and its integral are exact, but does not allow greater insight into noise mechanism. A parasitic capacitor DM voltage, $v_{C,12}$, can be defined as presented in (1.26), therefore resulting in the symbolic equation as shown in (1.27). Finally, by left multiplying $\mathrm{p}\boldsymbol{S'}^{-1}$, as presented in (1.28), and solving its second line for the CM noise, as in (1.29) and rearranging it, it results in the analytic equation (1.35) that is used to draw the equivalent CM noise circuit, presented in *Figure 1.15*

$$\mathbf{v}_{dcm} + v_{Pg}[0 \quad 1]^T = \begin{pmatrix} v_{12} = v_{DM} \\ v_{CM_i} + v_{Pg} \end{pmatrix} = \begin{pmatrix} v_{C,12} = v_{DM} \\ v_{C,CM_i} + v_{Pg} \end{pmatrix} \tag{1.26}$$

$$v_{C,DCM} \triangleq \begin{bmatrix} v_{C,12} & v_{C,CM_i} \end{bmatrix}^T = \frac{\boldsymbol{S'}}{\mathrm{p}} \begin{bmatrix} i_{12} & i_{CM_i} \end{bmatrix}^T \tag{1.27}$$

$$\begin{aligned} \mathrm{p}\boldsymbol{S'}^{-1}\begin{bmatrix} v_{C,12}\, v_{C,CM_i} \end{bmatrix}^T = \begin{bmatrix} i_{12} & i_{CM_i} \end{bmatrix}^T &= \begin{pmatrix} \frac{1}{4}(\mathrm{C}_1 + \mathrm{C}_2) & \frac{1}{4}(\mathrm{C}_1 + \mathrm{C}_2) \\ \frac{1}{2}(\mathrm{C}_1 - \mathrm{C}_2) & \mathrm{C}_1 + \mathrm{C}_2 \end{pmatrix} \begin{pmatrix} v_{C,12} \\ v_{C,CM_i} \end{pmatrix} \\ &= \begin{pmatrix} i_{12} \\ i_{CM_i} \end{pmatrix} \end{aligned} \tag{1.28}$$

$$\frac{\mathrm{p}}{2}(\mathrm{C}_1 - \mathrm{C}_2)v_{C,12} + \mathrm{p}(\mathrm{C}_1 + \mathrm{C}_2)v_{C,CM_i} = i_{CM_i} \tag{1.29}$$

$$\begin{gathered} v_{C,CM_i} + v_{Pg} = -\frac{(\mathrm{C}_1 - \mathrm{C}_2)}{(\mathrm{C}_1 + \mathrm{C}_2)} v_{C,12} + \frac{i_{CM_i}}{\mathrm{p}(\mathrm{C}_1 + \mathrm{C}_2)} \\ \text{Where } v_{C,CM_i} \leftrightarrow v_{CM_i} \\ v_{C,12} \leftrightarrow v_{UM} \leftrightarrow v_{MM_i}. \end{gathered} \tag{1.30}$$

Lastly, the virtual point P must be addressed conveniently as a known voltage node. Therefore, the point P is substituted by M, the negative input DC electrical point. Therefore, the voltage sources v_{CM_i} and v_{MM_i} presented in *Figure 1.15* can finally be expressed analytically as presented in (1.31)

$$\begin{cases} v_{CM_i} = \frac{1}{2} v_{\mathrm{UM}} \\ v_{MM_i} = \frac{(\mathrm{C}_1 - \mathrm{C}_2)}{(\mathrm{C}_1 + \mathrm{C}_2)} v_{\mathrm{UM}} \end{cases}. \tag{1.31}$$

Following the same procedure for the output CM noise (from the midpoint of the H-bridge), it is possible to define an equivalent circuit the can be connected through the point M, in which the output CM and MM voltage sources are, therefore, expressed as in (1.37)

$$\begin{cases} v_{CM_o} = \dfrac{1}{2}(v_{\mathrm{AM}} + v_{\mathrm{BM}}) \\ v_{MM_o} = \dfrac{(\mathrm{C_a} - \mathrm{C_b})}{(\mathrm{C_a} + \mathrm{C_b})} v_{\mathrm{AB}} \end{cases}. \tag{1.32}$$

Substituting the expressions in (1.31) and (1.37) in *Figure 1.15*, the equivalent circuit is presented in *Figure 1.16.*

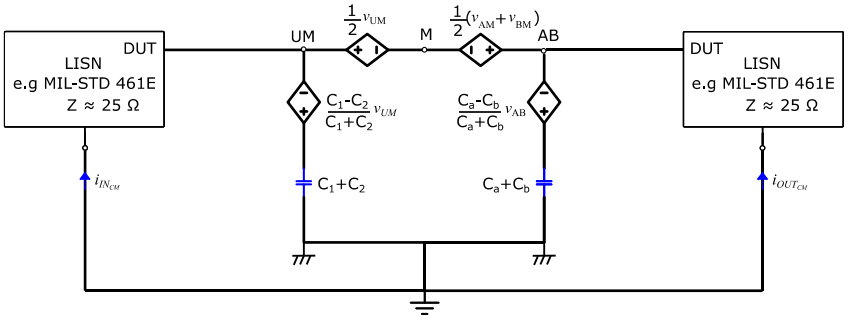


Figure 1.16 H-bridge EMI characterization and modelling with unbalanced parasitic capacitors.

It is possible now to quickly conclude over EMI signature of an H-bridge:

- Notice that, more important than the absolute value of parasitic capacitances, its unbalance may be more important for the CM noise generation;
- For the input side, the use of a good DC-link capacitor contributes to provide a clean DC voltage without spikes. This in turn helps to mitigate the CM voltage noise due DC-bus bar parasitic capacitance. They may even contribute to filter partially the output CM noise (switching nodes A and B), working as Y-cap filter;
- For the output side, the SPS modulation does not create CM voltage level, ideally, so that $v_{\mathrm{AM}} + v_{\mathrm{BM}} = 0$;
- On the other hand, depending on the modulation, e.g inner phase-shift modulation or three-level modulation in AC/DC application, or depending on undesired delays, it will create CM voltage noise level;
- The squared wave from midpoints AB may increase CM noise level if C_a and C_b are not the same;

- Finally, there is a large amount of possible combinations between unbalanced impedance path and voltage noise sources due to modulation, delays and synchronizations. By acting on them continently, it is possible to considerably mitigate the CM noise from the design phase. More about attenuation techniques are further discussed.

In *Chapter 3*, an equivalent circuit for the DAB based on such definitions is derived by simply "mirroring" a second H-bridge connected through a symmetric AC-link. It is then presented an extensive comparison between different proposed equivalent circuits concerning validation with respect to simulation results and symmetrisation and its impact on EMI through simulation and experimental results.

1.1.3.3 Main parasitic capacitances and equivalent high frequency models

An important task for acquiring the EMI conducted emission is the estimation of parasitic capacitances, which can be extracted through measurements, simple analytical equations such as parallel plates, or complex simulation through Finite Element Methods (FEM).

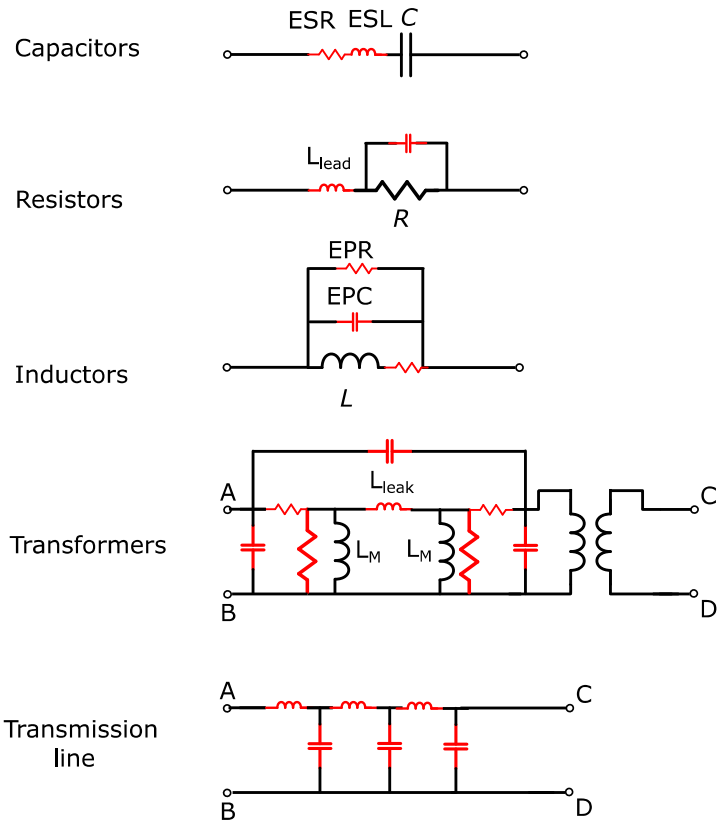


Figure 1.17 Parasitic elements of passive components. Adapted from [53].

The high-frequency model of the reactive elements are important for precise and accurate EMI signature, as the intrinsic parasitic are responsible for deteriorating attenuation and causing resonances. To synthesize, it is presented in *Figure 1.17* the main models of the passive components used in the literature for describing the EMI signature of power converters.

For EMI signature, the transformer and the switch devices are then explained and described as they represent the main sources and paths of EMI problems. Notice, however, the goal is to be more descriptive and qualitative than quantitative, as theoretical simulation and equations are not used to compare with practical results, but rather to build comprehensive analysis.

- AC-link transformer

The transformer is a key reactive device in isolated power converters, including the DAB. It can be divided into magnetic and electrostatic subsystems. The magnetic one plays an important role for the power transfer and its efficiency, while the electrostatic subsystem is responsible for HF circulation through parasitic (mostly intra- and inter-windings). The parasitic capacitances are accentuated by interleaving and compact structures, usually in high efficient and density systems. The analysis of the electrostatic subsystem becomes extremely important for the increasingly high frequency systems together with the large stray capacitance, even more evident on the context of planar transformers [54] [55] [56].

They can deteriorate the performance of the converter at high frequency operation mainly for two reasons: i) by providing coupling and low impedance path; and ii) stablishing resonance throughout the circuit. The high frequency oscillations (HFO) [57] due to stablished resonances are responsible to increase in the transformer temperature, reduced efficiency [58], power quality degradation as in a PV application case [59]; and poor voltage regulation, mainly under light-load condition as in an LLC converter [60] case. The low path is responsible for CM circulating currents that can reduce the effectiveness of protective system as in a PV cases [61] [62] and insert voltage ring on gate-driver, which may cause *crosstalking*. Therefore, the electrostatic model of the transformer is essential for understanding the propagation path of HF currents, CMC and DMC.

From the EMC conducted tests point of view, two important points should be pointed out:

- Considering DM observation, the HFO is harmful for the aforementioned reasons, but also because the DM currents created by the resonance circuits are visible as DM

noise. Intra-winding capacitances are mostly responsible for increasing such issue. Eventually, the voltage ring oscillation may couple into CM noise. Therefore, intra-winding capacitances are highly linked to DM analysis.

- Considering CM observation, low impedance coupling path provided by the inter-winding capacitances are responsible for creating a path from secondary to primary and vice-versa, which will increase CM noise. If stray capacitances to ground are non-negligible, it can be considered a noise path/deviation. The inter-winding capacitance is, therefore responsible for coupling path between primary and secondary stages of a power converter. They are presented in the CM models and analysis [63], decoupled from intra-winding capacitances, considering that intra-capacitances does not change the waveform voltages on the input and output voltages of the transformer.

Such facts proves that the EMC education includes the knowledge of the parasitic capacitances in a transformer, their effects and how to reduce them. Considering a two-winding transformer, different capacitance-models exist to take into account inter and in-tra-winding capacitances. They can be separated into two diverse models. One that consider the internal physical structure of the transformer, composed of all parasitic capacitances, e.g turn-to-turn, layer-to-layer inter-winding, turn-to-ground, which can be solved numerically e.g FEM or analytically. Notice that the physical system is composed of many stored capacitances along the windings, while voltage is not constant, but rather distributed on turns and layers, usually supposed linearly. Even if all complex physical parameters are well known, there need equivalent circuits and models for analyzing properly the effects of all stray capacitances. This is possible through electric network theory, which attempts to describe the electromagnetic behavior that exists entirely or partially in the physical world by setting up a mathematical models with fewer reactive elements. The advantage of such methods is that, the designer may apply tests without knowing the structure of the transformer and obtain high precision in the frequency domain, very useful for EMC analysis.

The latter one, besides useful for interpreting physical structures and reducing complexity into simpler equivalent circuits, are important for treating the device as black box respecting network theory principles. This means that the capacitive interactions can be found through experimental results without the need of knowing what is inside the device.

A mathematical model based on 3-port network [64] [65] is exhaustively used through the literature [58] [60] [63] [66]. The principle is based on the conservation of electrostatic energy stored in a 3-port network, which results in equations that once solved results on the value of the capacitances. Three fundamental capacitances are measured through acquiring

the resonance points observed in the impedance analyser, which are shifted depending on the connections. Those capacitances are associated with the three-port network system capacitances, which is then associated though the 6-capacitance model. In general, such model is valid in the medium frequency range (up to 5 MHz), or up to one or two decades beyond the maximum usable frequency of the transformer. Under the assumption that the placement of the stray capacitances are free as long as energy is conserved, the parasitic capacitors are analysed considering the leakage inductance, and more accuracy is provided (around 10 MHz). The 6-capacitance model can be reduced into a three-capacitance model, under the condition that one voltage port is dependent, which can be referenced to the primary. The three-capacitance model is also used in the literature [55] [57] [67] [68] [69] . The frequency range of this model is around 5 MHz.

Further simplification neglecting the leakage inductance can result in a one-capacitance model [54] [57] [60]. Notice that further simplifications reduce the frequency range validation up to the second resonance frequency, but the equivalent capacitance value is still dependent on the 6 capacitances. Indeed, such reduced equation when combined with analytical or FEA [60], becomes an important tool for optimizing the transformer along with the converter, as the first resonance is more apparent and harmful, and basically defines the working frequency of the transformer. Observing through the DM current circulation, the intra- and inter-winding capacitance can be lumped into one parallel capacitance that will resonate with magnetic elements within or outside the transformer, causing very oscillatory current in which may affect efficiency by increasing AC losses and reducing EM performance.

Another important parasitic capacitance, but rarely discussed in the literature, are the capacitances with respect to ground. Indeed, besides an equivalent capacitance to ground, the electrical terminals of the transformer (pads, connectors, etc) will always introduce parasitic capacitance that should be lumped together. An initial step as estimation is to calculate the capacitance of the pads with respect to the ground plane, in the order of pF. Such value is used for qualitative results when studying the CM noise in *Chapter 3*, mainly concerning the of the AC-link found in a DAB.

More about such complex model, with 10 – capacitance model is presented in [71]. Such model was used in the context of high frequency, high-power and high-voltage transformer (H3T) with metal soft magnetic material, such as nanocrystaline material, which has much larger conductivity than ferrite. Therefore, for safety reasons the core has to be grounded, and the parasitic capacitance with respect to a ground plane becomes more important. The model may be reduced into 6-capacitance or 3-capacitance models if primary

or secondary are grounded. In such work, the capacitance parameters were extracted through 2-D FEM based algorithms and the stored electrostatic energy conservation. For the transformer, the frequency range was experimentally validated up to 300 kHz due to the electric and magnetic parameters. It can be observed that the frequency range is valid showing a dynamic of one pole and one zero in open circuit.

Not often discussed in the literature, it is important to emphasize the impact of parasitic capacitances to ground of reactive devices. Indeed, for the transformer the focus are often comprehending only intra- and inter-winding capacitances through 6-capacitance model. On the other hand, the inclusion of parasitic capacitance to ground , shielding [72] [73] or core [74], forming a 10-capacitance model [71] are important to not only understand the CM noise mechanism, but also used to attenuate [75]. For example, by combining a symmetric design of the transformer and passive out-of-phase compensation in [76] for a full-bridge converter, the filter size was reduced by 76.5%.

For a Flyback case, the studies in [77] explain that the noise is in function of the winding arrangement, transformer terminal connections and voltage distribution of winding layers; and a reduction of around 40 dB is observed. In [78], it is shown how through simply placing the diode in the return path of a Flyback can beneficial for CM noise reduction; and, despite of implementing a transformer with 70 times larger parasitic capacitance, the noise was reduced by 8 dB, eliminating the trade-offs between leakage inductance and parasitic capacitances in Flyback and Forward converters. Finally, in [79] winding and external capacitor compensations are used, resulting in very low CM noise in the CE middle range frequency (around 30 dBuV).

In [80], the lumped parasitic capacitance ground in a full-bridge converter are addressed as being the main cause of mismatch capacitance, harmful for successfully recycling CM current. Splitting of the resonant network is then proposed, and another method one based on added external capacitance compensation across mid-point to ground of one H-bridge leg. The necessary capacitance is estimated by observing difference in slope of lower switches measured experimentally. In [81] [82], the intra and inter-windings capacitances are converted into CM stray capacitance by including a layer of chassis ground, providing low impedance path for the CM noise, which according to the author, can be used as Y-capacitors. A trade-off between DM noise and CM noise is observed, but focus are given for CM noise since, according to the authors, 80% of the CE EMI in SMPS can be attributed to CM type. Indeed, the proposed planar transformer has accentuated a peak at 400 kHz, observed as DM noise, while considerably improving further frequency range, observed as CM noise. Since treating DM noise and one frequency peak is easier than a flat spectrum content, the proposed

solution is superior in terms of EMC. Such facts make us concluded that there is still the need of lines of research that take into account the subtle trade-offs that required careful attention in terms of EMI.

So far the 6-coupling capacitance has been presented as a mean of observing the DM structure of the converter, by giving importance to intra-winding capacitances, and, more specifically to the equivalent primary capacitance. However, when analysing the CM noises, the inter-winding are important because, as already mentioned, they are coupling path from secondary to primary and vice-versa. A reduction of the 6-coupling capacitance into a two-capacitance, respecting the energy conservation rule, is presented in [63]. In a two-winding transformer 6 possibilities can arbitrarily be chosen, from which certain models simplifies the CM noise analysis. The model is derived for many DC/DC converters, including Full-bridge LLC resonant converter, which assimilates more to DAB converter. As in the case of simplifying and reduced capacitance models, the validation of the model works by neglecting transformer's leakage inductance. Therefore, the frequency range is valid for up to the resonance frequency between total capacitance between primary and winding and leakage inductance. Another condition is that at least one winding of the transformer are connected to equivalent independent voltage sources. It also provides the procedure for deriving the CM noise model and then for extracting the lumped capacitances from simple measurements. In [83], more about the two-winding capacitance is discussed, and an equivalent Thevenin is provided. In order to simplify our CM noise analysis, the 6-capacitance model can be represented by a two-capacitance model under certain conditions: i) the transformer's leakage inductance is neglected, therefore valid for lower leakage inductance which is not often the case for DAB applications; ii) one terminal winding should be connected to an equivalent voltage source. The estimated extracted value of the inter-winding capacitance is 25 pF, which will be used in this work.

The frequency range of all models is validated in practice with impedance meter testing open and short circuit. The models with more reactive elements are able to describe more resonances, and therefore, are to present more accuracy in the higher frequency range. As it has been observed in the literature, regarding DM aspects, 3 capacitances are enough for defining 3 resonance frequencies, whereas one capacitance model is able to provide only one resonance. Therefore, defining a specific frequency range for each model is not easy, since it depends on the value of the reactive elements defining the main zeros and poles of the transfer functions.

Another reason for limiting the frequency range is respecting the λ/4 condition, in which beyond it, antenna or transmission line theory are needed. Another reason is the neglecting of the Mixed-mode, which may be the reason for a range frequency in the order of around 10 MHz. To consider these aspects, a model based on an impedance two-port network is capable of describing the behaviour up to 100 MHz is presented in [84].

- Power loop high frequency model

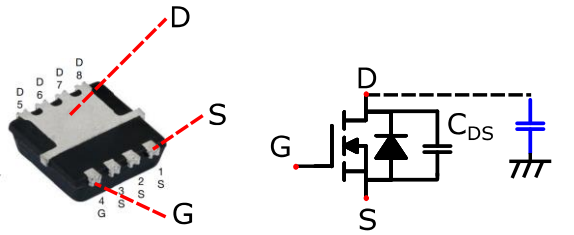
Methods for calculating the parasitic elements before the prototype include simulation on PEEC, Finite elements, datasheet information and analytically. Once prototyped, methods for measuring the parasitics include observing the resonances (poles and zeros) found on wave-forms, impedance analyser, VNAs. The power loop high frequency model, which is highly impacted by the equivalent parasitic due to layout and device placements [85] [86] [87] [88] [89] [90] of half-bridge based structures . As it is presented in [91], a numerical approach of two different layouts, rectangular and square, shows a difference of up to 7 dbuV in favour of square geometry shape. In [92], theoretical simulated results portray 6 cases, in which the most optimized one was verified for the case of ground power directly under the substrate. In [93], it is presented a study of bus bar optimization based on symmetric loops for a SiC-based H-bridge PEBB. Particularly for the DAB, in [94], for the layout of a DAB (2022), the switch devices are placed in such a way that flux cancelation is realized, reducing parasitic inductance and resistances. Another layout for the DAB is discussed in [95] for a GaN DAB at 400 W. In [96], the power loop is discussed and improved in a 200 kW DAB (99.6% efficiency) based on 1700 V SiC power MOSFET module. In [97] [98], a PCB bus-bar design for loop inductance minimization is discussed for an ANPC phase leg for DAB based DC system. Finally, the power loop, drain-to-source waveform and ringing are discussed in [99] for Si MOSFETs and GaN HEMTs.

1.1.3.4 Main parasitic capacitances of switching devices

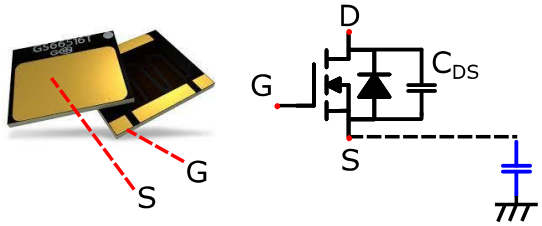
In *Figure 1.18*, it is presented the main parasitic capacitances in Si and GaN MOSFET switch technologies. They represent one of the main WBG devices nowadays in power electronics. As it was presented in Chapter 1, the value of C_{oss}, which can be approximated as being the drain-to-source capacitance C_{DS}, is an important parameter for calculating switching losses, dead-time and ZVS conditions. Moreover, its value defines the drain-to-source V_{DS} waveform, e.g rise and fall times, which is useful for the describing the EMI behaviour mainly for the higher frequency. In practice, a voltage bias should be

considered. An energy / charge equivalent capacitance [100] should be calculated for the operating voltage for more accurate analysis. It is interesting to notice that, as applied voltage increases, the energy equivalent drain-to-source capacitance decreases significantly.

Parasitic capacitance to ground are the most important for CM noise model in the CE frequency range. For the H-bridge composed of SiC and Si devices, the drain is the surface in which heat is dissipated through the aluminium layer, whereas the H-bridge composed of GaN devices, the source is the part in which heat should be dissipated. Therefore, as presented in *Figure 1.18*, the main parasitic capacitance to ground are located in the drain for SiC and Si and source for GaN, since they are larger. The most important parasitic capacitance to ground were extracted using the simple ideal parallel plate capacitance. Notice that other parasitic capacitances with respect to ground, also affect the switch speed and efficiency. Indeed, the appeal for compactness provided by GaN and SiC through thermal interfaces have a negative impact on switching speed and CM currents!



(a)



(b)

Figure 1.18 Equivalent parasitic capacitor of different MOSFET technologies: (a) Si PowerPAK-1212-8W – Ref SQS660CENW; (b) GaN GS66516. Adapted from [101].

.

1.1.3.5 Attenuation techniques

This paragraph is dedicated to present a brief review on the CE attenuation techniques in power electronics. According to [102], the current attenuation techniques can be listed as portrayed in *Figure 1.19*.

It can be said that EMI filter, or any input/output easily cascaded system for attenuation purposes should be classified as a post-designed power converter, while the others

methods are used during the design phase. A combination of many methods may result in high attenuation of CE in power converters. During this thesis, the use and discussion on passive EMI filter, Soft switching, interleaving, active compensation, symmetric topology, Wheatstone bridge, PCB layout & optimization, grounding and shielding are approached and / or briefly discussed.

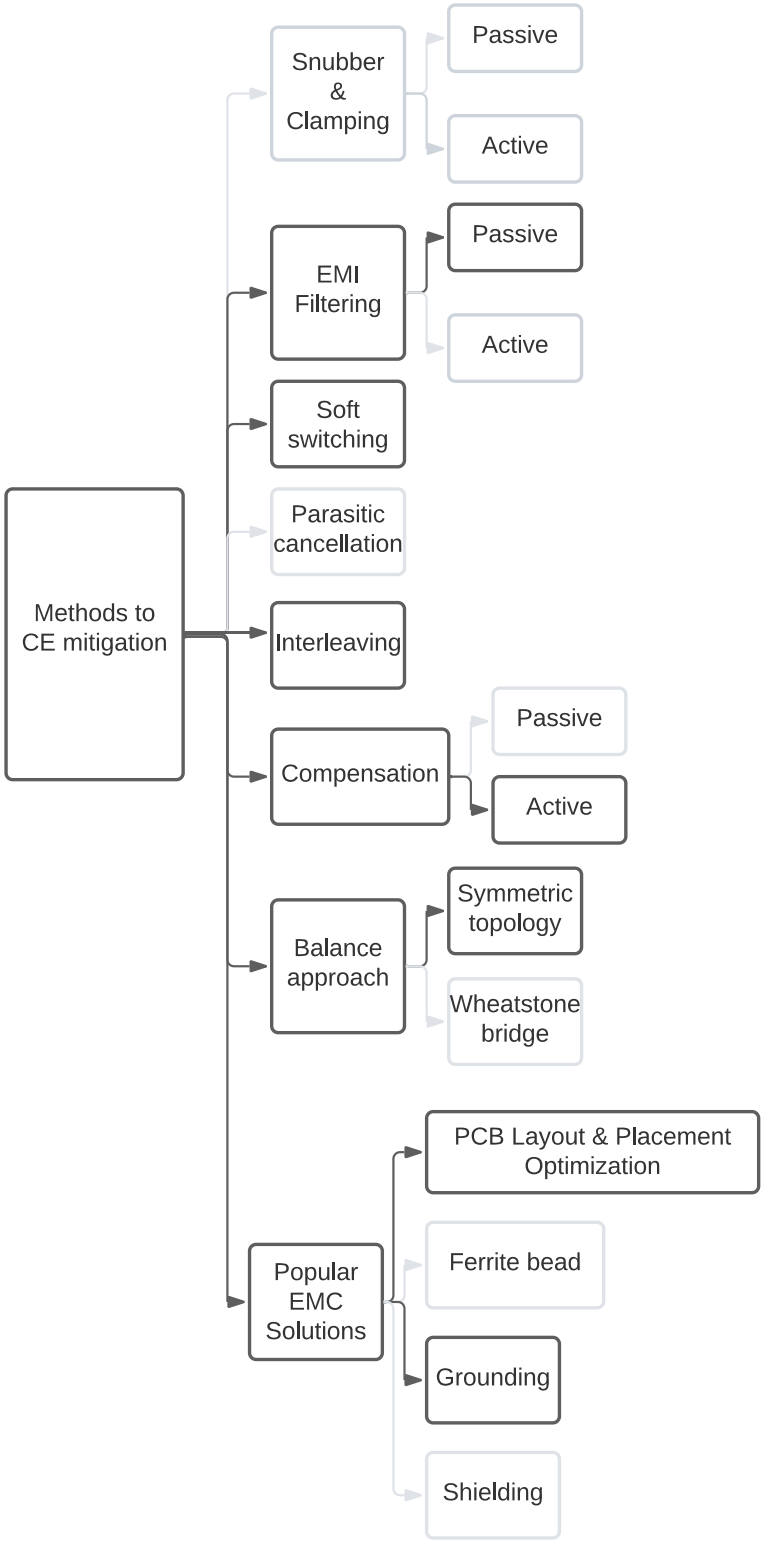


Figure 1.19 EMI mitigations methods applied in power converters (bold squared topics are applied or discussed in this thesis). Adapted from [102].

- Passive EMI filter attenuation

There are infinite topologies for filter design (C, LC, CLC, etc..). They are designed according to the required attenuation. A typical EMI filter, presented in *Figure 1.20* , is based on a two-stage and are meant for both CM and DM noise reduction.

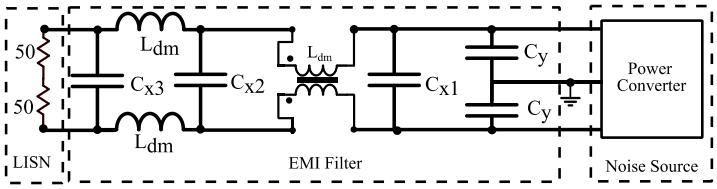


Figure 1.20 Typical two-stage passive filter. Adapted from [39].

When decoupled based on pure symmetrical EMI filter, the equivalent DM and CM circuits are presented *Figure 1.21*.

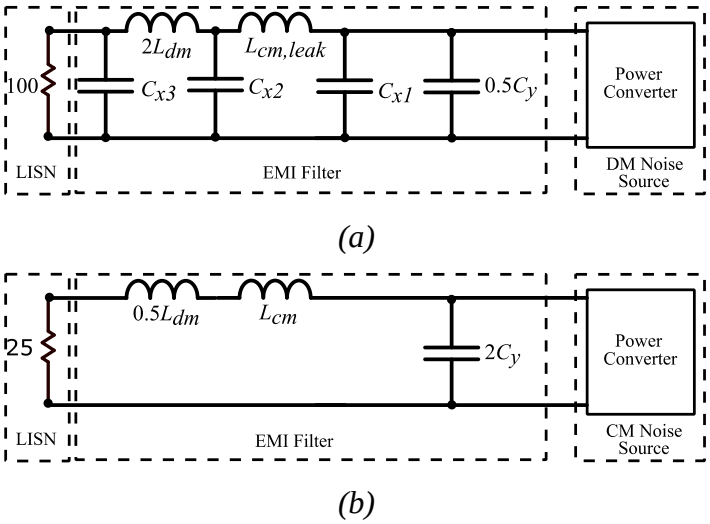
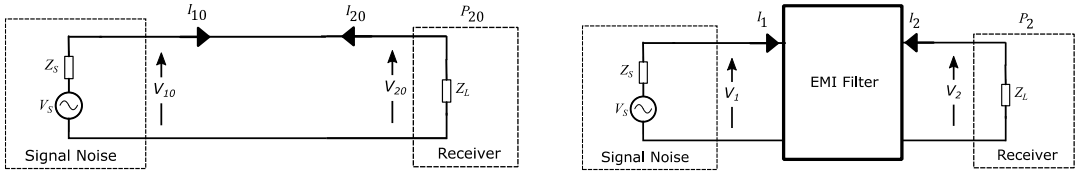


Figure 1.21 Decoupled HF equivalent circuit: (a) DM; (b) CM. Adapted from [39].

For measuring the attenuation, the definition of insertion loss, widely used for filter design and datasheet is recalled from [39] is presented in *Figure 1.22* and (1.33). Some of the concerns that can be observed right away is that, even though higher order filters attenuate more effectively, they create undesirable resonances that can be located in the lower frequency, impacting on efficiency, and even the intermediate (CE frequency range) or higher

frequency, impacting on EMC. Techniques for damping the resonance frequency should be used. The expression in terms of two-port network theory (*T*- or *ABCD*- parameters), used for easily calculating of voltage/current attenuation or insertion loss, is presented in (1.34).



(a) *(b)*

Figure 1.22 Insertion loss IL extraction required measuring voltage, current and power: (a) before EMI filter; (b) after EMI filter. Adapted from [39].

$$IL = 10log\left(\frac{P_{20}}{P_2}\right) = 20log\left(\frac{I_{20}}{I_2}\right) = 20log\left(\frac{V_{20}}{V_2}\right) \tag{1.33}$$

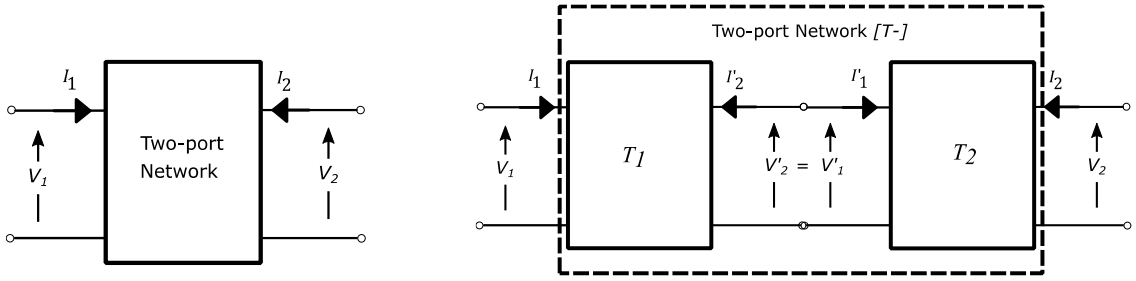
$$IL = 20log\left(\left|\frac{AZ_L + DZ_s + B + CZ_LZ_s}{Z_s + Z_L}\right|\right) \tag{1.34}$$

As previously mentioned, for DM noise, it is considered that its nature has a pure current source behaviour. If that is the case, then an infinite impedance at the source noise should be considered, and the definition of IL for DM is redefined in (1.35), which is in agreement with the same definitions used in previous and satisfactory work at G2Elab [40], [5]. Indeed, it becomes the simple transfer function of output to input current, as sometimes used in the literature

$$IL = 20log(|CZ_L + D|). \tag{1.35}$$

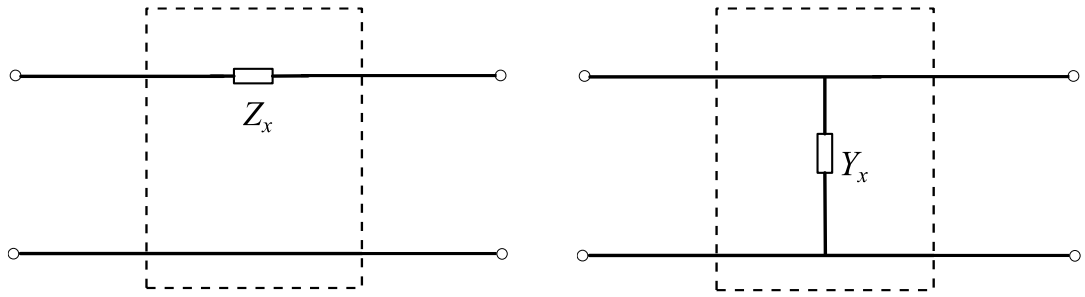
It is possible to build up the filter design in a two-port network representation [39] with the goal easing the analysis of the impact of the filter design topology on insertion loss, by simply cascading subsystems, as presented in *Figure 1.23*.

Firstly, it is recalled through *Figure 1.24*, the representation of the *T*- parameter representations for series impedance (1.36) and parallel admittance (1.37). Therefore, the designer is capable of building any filter topology from cascaded parallel admittances and series impedance. As matrix multiplication in non-commutative, it is important to build the equivalent chain matrix in the exact order, that is, as seen from the converter's side (the first reactive elements seen from the converter stays at the left-hand side orderly).



(a) *(b)*

Figure 1.23 (a) Generic two-port network; (b) cascaded two-port network through Chain parameters. Adapted from [102].



(a) *(b)*

Figure 1.24 (a) Series impedance connected component; (b) parallel admittance connected component. Adapted from [102].

$$T(Z_x) = \begin{pmatrix} 1 & Z_x \\ 0 & 1 \end{pmatrix} \tag{1.36}$$

$$T(Y_x) = \begin{pmatrix} 1 & 0 \\ Y_x & 1 \end{pmatrix} \tag{1.37}$$

An example of an equivalent *T*-matrix is provided (1.38) for a π-topology. When building in the inverse order, the designer can obtain the impedance for stability analysis, e.g meeting Middlebrook Stability Criteria, far from being covered in this work. As it can been seen, the versatility brought by the use of two-port network simplify the analysis, of any complexity. Moreover, the implementation through *T*- matrix of two-port network can also be easily transformed into *S*- parameters and be analysed through more sophisticated equipment such as VNAs. Later in *Chapter 4*, inspired by the use of two-port network, it proposed a theory for deriving analytically through two-port network theory the impact on voltage, current and power distribution in a multi-cell converter due to component dispersion. In Chapter 5, based on two-port network as well as insertion loss definition, an adaption for

multi-cell converter for both CM and DM are proposed and analysed, theoretically, with respect to the connection configuration of a multi-cell converter and number of cells.

$$T(\pi) = \begin{pmatrix} 1 & 0 \\ Y_1 & 1 \end{pmatrix} \begin{pmatrix} 1 & Z_2 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} 1 & 0 \\ Y_3 & 1 \end{pmatrix} = \begin{pmatrix} 1 + Z_2 Y_3 & Z_2 \\ Y_1 + Z_2 Y_3 & 1 \end{pmatrix} \tag{1.38}$$

Notice that, once the EMI signature is identified, through theoretical or experimental results, the designer will be concerned only on the attenuation at the given frequency, through the insertion loss equations. Such assumption allows to “look for” a suitable filter design without the need of always simulating or calculating the noise source. Indeed, through the simplifying circuits of DM (current source) and CM (voltage noise source coupled with a given parasitic capacitance, e.g. 20 pF) it is possible to draw important conclusions. For example, with typical or maximum allowed values, such as Y-capacitor that are limited by safety standards of the maximum total leakage current to earth (e.g. 3.5 mA RMS, leading to a maximum value of 36 nF [9]), it is possible to conclude that providing the necessary attenuation, mainly at lower frequency can be quite complicated. In some occasions, the use of Y-capacitor is not possible as the power converter does not contain access to Protective Earth (PE), making the task even more complicated, if not impossible through only EMI filter design. Once again, before we learned that the CM noise occupied a large range of the spectrum, now there is the fact that they are very hard to attenuate. Besides, they can easily provide near field coupling to the surrounding, which may impact on resonances and far field. Either way, the use of filter design as the main method for surpassing CM noise is not the most optimum, or, being more pragmatic it can be considered an obsolete technique.

It is interesting to notice that, not only the first harmonic, which are produced and the largest, are important. The other harmonics can also be accentuated due to parasitic resonances.

The harmonic of concern can be eliminated, conventionally by filter, through the conventional post-prototyped method: filter designed by selecting a suitable topology, e.g T or PI, based on the input and output impedance of the switch mode power supply, followed by the cut-off frequency once the attenuation is known, necessary damping and other parasitic eliminations. In a more sophisticated method is proposed in [103], in which the design method of filter is based on EMI suppression at the resonance frequency, which may occupy 1/5 of size compared to conventional method.

- Active compensation

The principle is based as follows: if two nodes have complementary voltage transition, while keeping same parasitic capacitances, there is more chance for CM noise reduction. When closer investigating the topology of a power converter, it is possible to compensate, actively (with additional switches) or passively (through additional windings). Proposition of different topologies [104], [105], and/or new modulation [106] for the sake of reducing noise, could also be considered active compensation, as long as one or more active switching devices are involved, which may result in more devices and lower efficiency. On the other hand, one can benefit from connecting structures that will have a function, such as splitting of voltage and current stresses, while actively compensation the CM noise current [105] [107], [108]. The concept is very clear in [108], which parallelized two DAB structures (NPC and regular DAB – 10 kW at 50 kHz), as presented in Figure 1.25, with a type of arrangement that is justified in a high power Medium Voltage DC (MVDC) for power sharing and improving reliability through redundancy.

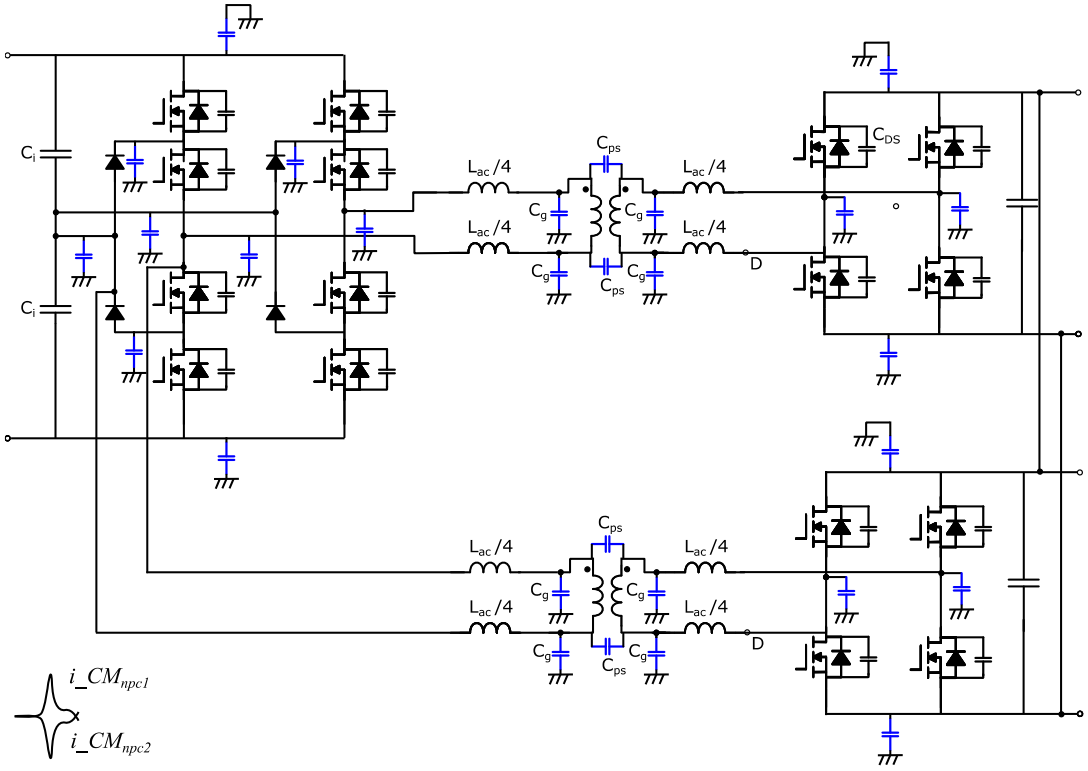


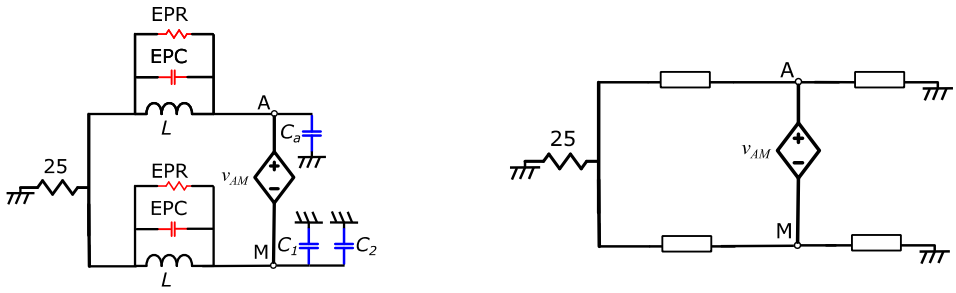
Figure 1.25 DAB architecture with parallel NPC and full-bridge units for conducted EMI reduction. Two opposite CM currents. Adapted from [108].

It is easy to see that such technique is convenient for CM noise attenuation in Multi-cell /Modular converters. It is better explained in *Chapter 5*, in which experimental results

provided reduction of up to 40 dB, by actively compensation from one cell to another in amount of pair.

- Balance approach

The balance approach [50], [109], [110], [111], [112] is based on Wheatstone bridge. It first consists on deriving equivalent CM circuits through previous mentioned methods, and verifying and inserting impedance paths that will satisfy null voltage across a Wheatstone bridge. When combining with the substitution theorem, previously presented, it becomes a powerful method for CM noise attenuation. As an example, the boost converter modelled as presented before in *Figure 1.14*, can have its inductors splitted [50], so that it is possible to design impedances that will form a Wheatstone bridge, as presented in *Figure 1.26*.



(a) *(b)*

Figure 1.26 (a) Splitting the boost inductor; (b) a Wheatstone bridge observed across the noise source. Adapted from [50].

- Symmetrisation

As it has been previously explained, the symmetrisation of impedance paths, (e.g. EMI filter design) has superior advantages, as noise due to MM (CM to DM or DM to CM [36], [37]) are reduced. When a topology is not symmetrical, one can derive symmetrical variations at the cost of adding switch devices and / or reactive elements [105] [107], [113], [114]. This is exemplified trough the two-channel interleaved PFC converter presented in *Figure 1.27*. There can be very subtle or no difference in classification between symmetrisation and active/passive compensation, as some structures will be symmetric; or even balance approached if it is possible to keep same impedance through an equivalent Wheatstone bridge. Indeed, providing the three features at once is probably possible and could mean very low CM noise.

Some topologies, as in H-bridge structures (Ful-bridge converter, DAB) has intrinsic symmetry with respect to topology. One should take advantages of such feature privileging symmetrisation on any impedance path (Busbar, AC-link, EMI filter). Symmetric topologies

should definitely benefit from a fully symmetrized impedance system to reduce CM, MM and even ringing. More about H-bridge structures and its AC-link is explained in detail in *Chapter 3*, consisting in a large attenuation on CM noise proved theoretically and experimentally.

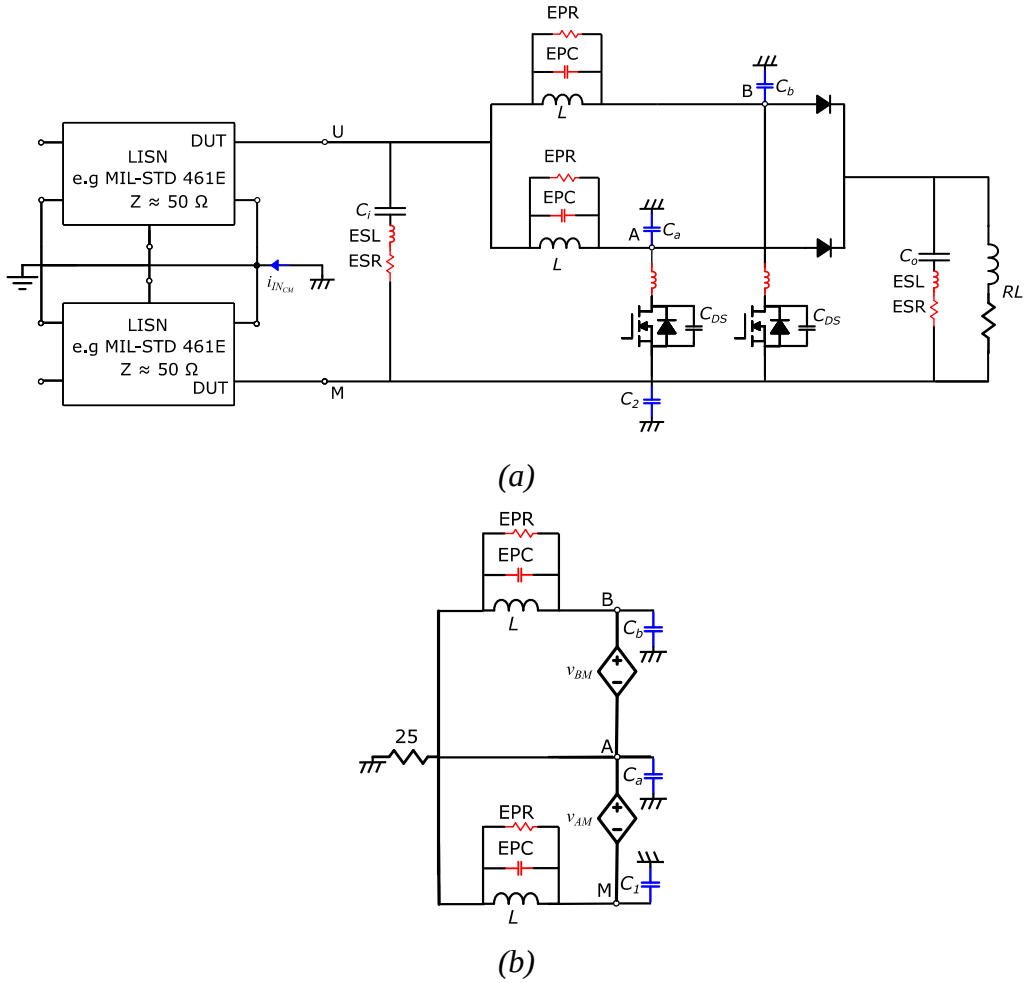
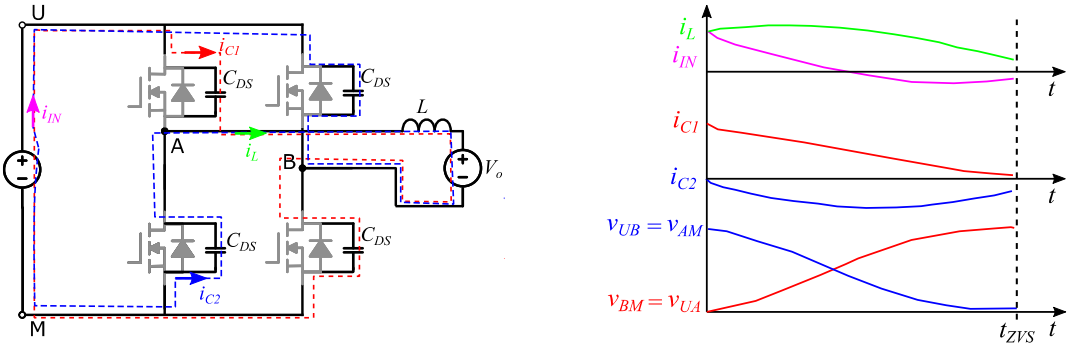


Figure 1.27 (a) Two-channel interleaved PFC converter; (b) CM noise model for the two-channel PFC converter. Adapted from [110].

- Soft Switching

Soft switching techniques enable the switch devices to have a slower dv/dt, with no drastic change in voltage and currents. Its impact is more visible in the higher spectrum, as ringing and rise and fall time are located in such frequency range. A common technique of soft switching is through zero voltage switching (ZVS), which is when the gate signal triggers only when voltage across a switch is reduced to zero. Knowledge on the reactive elements, including C_{oss}, series inductance and current value at the switching transitions are necessary to well investigate the ZVS. A simple condition is to consider the energy associated with the

series inductance ($^1/_2 LI^2$) is larger or equal to the energy associated with the C_{oss} of the MOSFET ($^1/_2 CV^2$).



(a) *(b)*

Figure 1.28 ZVS process in H-bridge based converters: (a) Equivalent circuit at transition; (b) observed typical waveforms. Adapted from [115].

It is important to notice that, depending on the modulation, e.g inner phase-shift in H-bridge, it may create a CM voltage level that will be visible on the lower frequency spectrum (as of the switching frequency). This has been verified and discussed in [116], [117] for full-bridge, and for a DAB [118], other modulation that provide ZVS through inner phase.

1.1.3.6 Grounding aspects

It is important to understand that, there exists different safe standards with respect to grounding [119], which play an important role on the CM noise mitigation. For single-phase utility power lines, some applications have 2-wires, others 3-wires. The attenuation in 2-wire systems is more challenging than in a 3-wire, as the Protection Earth (PE) wire is not available for the Y-capacitor connection.

Sometimes, for safety reasons, the output is grounded in [77] and the CM noise generated by the inter-windings circulates more easily through the LISN, and therefore, becomes critical for CM aspects. On the other hand, the noise source of secondary stage is shunted on the secondary side (e.g in a Flyback, the noise due to diode parasitic capacitance will tend to be circulating on the secondary stage and not go to the LISN, and in the same way for the DAB, the noise generated by the switching cells will circulate locally at the secondary side). If, on the other hand, one of the power lines is connected to the ground, often the case of DC power lines, one of the Y-capacitor and the 50 Ohms resistance from the LISN are shunted, and therefore, the insertion loss, filtering capability, symmetry and measured noise

voltage are modified. Therefore, it is important to identify the ground connections according to the safety standards and applications before designing the power converter and the noise attenuation decision takings. Another important factor is that such Y-capacitors must meet safety standards that limits the leakage-current according to different specifications. Therefore, the preferences for no Y-capacitor solutions in certain cases.

Another point of discussion is whether a ground plane could be beneficial in terms of EMI mitigation. In one hand, by not grounding, there is the equivalent decrease of the parasitic capacitance to the ground, but the decrease is less significant with the increase of distance due to the fringing effect in the capacitor. For larger distance between parallel plates, the classical equation is no longer valid [120]. For large separation, the decrease of the parasitic capacitance is actually decreasing much slower than the classical equation provides. Due to others edge or angle of the electric plates with respect to a ground plane (the one found in certifying test for example), a larger asymmetry of capacitance may be more harmful than the decrease of equivalent capacitance.

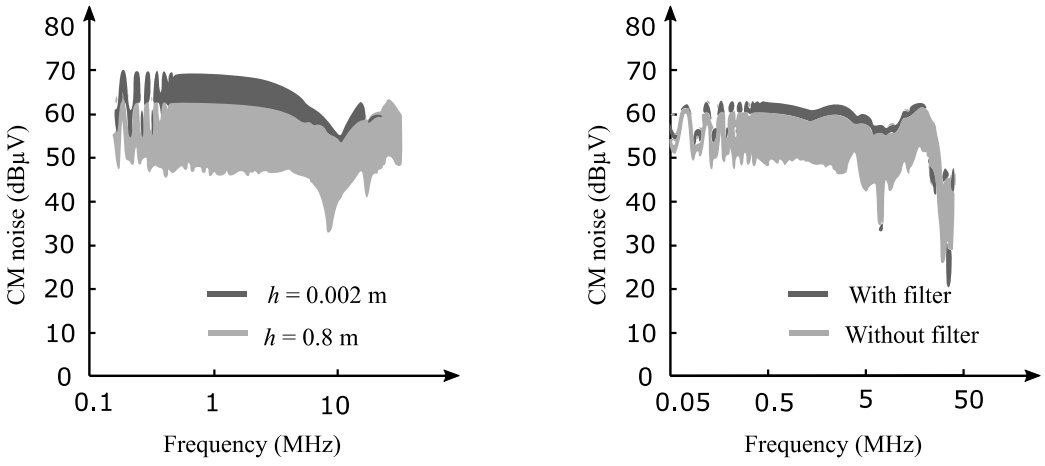


Figure 1.29 CM noise generated mode the absence of grounding: (a) by varying height; (b) by including or not filter stage. Adapted from [121].

Above all, the ground plane is important reduce parasitic inductance in PCB while acting as shielding for radiated emission. Therefore, it may be important to have a referential ground plane to be able to control such parameters. Indeed, power converters that does not have a third PE wire still generates CM [121] (e.g shipboard applications [122]) finds difficulty on passing the EMC standards, even though the parasitic capacitance to ground are lower than usual. This is well visible in *Figure 1.29 (a)*, which shows that, even though the separation has increased 400 times, the reduction of CM noise is only around 8 dB, that is 2.5

in absolute value. In *Figure 1.29 (a)*, it is possible to notice that the inclusion of filter does not affect effectively on the CM noise.

1.1.4 Partial conclusion

A general literature review and information on EMC dedicated for power converter has been addressed. The reader is now capable of understanding the main issues, how to simplify analysis through equivalent circuits and the best methods for attenuating CE noise. All the observation of EMC also requires a careful understanding on the EMC testing equipment, which is provided in Appendix 1.A.

A simplified approach has been presented to address the EMI issue in the lower frequency range (MHz). This approach assumes that the propagating path primarily consists of ideal switching and reactive devices. However, in reality, the presence of parasitic inductances and capacitances, particularly across the power loop, can significantly contribute to resonances and oscillations. These phenomena typically occurs at frequencies higher than 30 MHz and can result in reduced efficiency and increased conducted emissions (CE) noise. It is worth noting that this thesis does not take into account such high-frequency and saturation models.

1.2 Power Converter Array for EMC compliance

The concept of Power converter array (PCA) is well addressed in [5] [6]. The idea is, through standardization, provide automated design to manufacture in power electronics [123], while benefiting from modular/multicell converter properties and advantages. Indeed, it is the merging of concepts Power Electronics Building Block (PEBB) and successful highly efficient and dense power converter through multicell approach.

1.2.1 Multi-cell / Modular converter approach

According to [6], in the 90s, the term "multi-cell" was used to describe a flying capacitor converter focused on high voltage power conversion, which is now used in both high and low voltage applications with high efficiency and power density. In the early 2000s, "multi-cell converter" referred to any topology with multiple conversion cells. Improvements in MOSFET performance and integrated gate driver stages made it possible to design more

efficient converters using the multi-cell approach, which offers benefits such as reduced losses, improved harmonic spectrum, and spread of voltage and current ratings. Multi-cell converters can achieve higher efficiency and better power densities than single-cell converters in various applications

- ISOS, to build in input and output voltages;
- ISOP, to build in input voltage and output current, allowing higher input voltage to be integrated with lower output voltage;
- IPOS, to build in input current and output voltage, allowing lower output voltage to be integrated with higher input voltage;
- IPOP, to build in input and output currents.

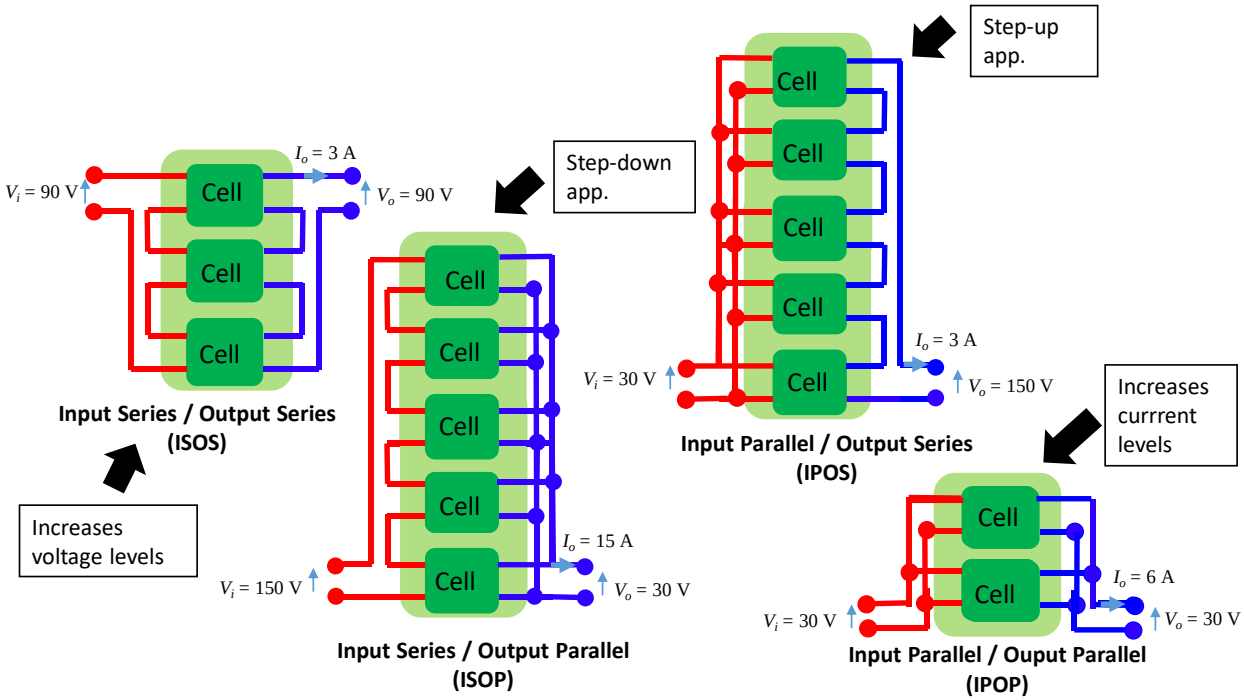


Figure 1.30 Example of possible connection configurations among multi-cell converters.

In the literature, the most common connections presented are the ISOP/IPO, due to its high voltage/current gains, for isolated AC/DC applications by integrating full-bridge AC-DC rectifier. As it has been presented in [21], there is an optimal amount of cells for a given application. Meaning that for very diverse applications, when considering efficiency and power density, there should be a different converter standard cell (CSC). When a given CSC has been designed, the efficiency tends be kept the same if component dispersion is minimum. The literature has not considered and / or demonstrated theoretically and analytically the

impact of component dispersion on efficiency, and seldom on the voltage, current and power sharing.

In *Chapter 2*, a standardized and dimensionless method is introduced for designing the DAB CSC based on three variables, namely output current, input voltage, and voltage gain. This approach ensures that the CSCs remain predictable and maintain consistent performance characteristics on a dimensionless plane, encompassing aspects like EMI signature and linear solvability in absolute values. Although specific cells may be required for varying output currents, input voltages, or voltage gains, the presented methodology enables the design to remain versatile and applicable to different scenarios. . The situation can be analogously compared to the cells of human beings, in which different ones are composing different organs.

The CM noise attenuation of the multi-cell (AC/DC) converters presented in [124] is based on centralized filter of three stages, focusing more on the DM noise attenuation through interleaving. In [45], for a single DAB, the EMC managing is neither detailed, and a switch model through simulation is used to verify a filter of three stages as well. It is unclear, however, if the filter design is included in the optimizing process and whether or not the solution presented is, indeed optimized in terms of costs, volume and efficiency. In [40], [5], previous work at G2Elab, regarding EMC, only DM noise is treated. A discussion on centralized versus distributed filter is given, and important conclusion on a topology that does not depend on the number of cells, but only on its configuration (Input series or Input parallel).

1.2.2 Standard Cell Methodology

The main block inside a PCA is it modular power converter unity, also known as converter standard cell (CSC). Once one CSC is well characterized in terms of important parameters, such as efficiency, temperature, sensibility and EMI aspects for a given mission profile, the total impact of the n^{th} CSC and their superposition may be well predicted. This is especially true when considering ideal and not mismatched CSCs for any electromagnetic parameter by applying superposition theorem. The prediction and tendencies can be performed theoretically and/or experimentally. A modular approach, power electronic building block (PEBB), existing in Vicor products as presented in *Figure 1.31* , allowing high power density and quick prototyping, has inspired the concept of power converter arrays (PCAs).

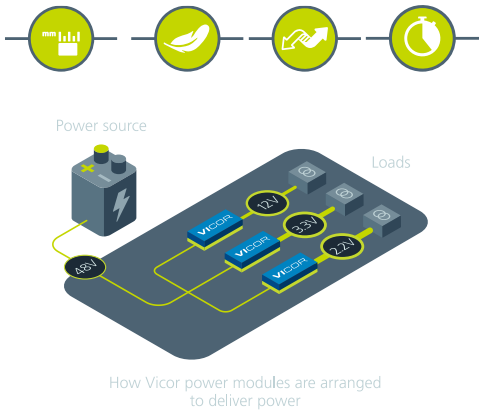


Figure 1.31 An example of power deliver network that is power-dense and scalable. Adapted from [Vicor].

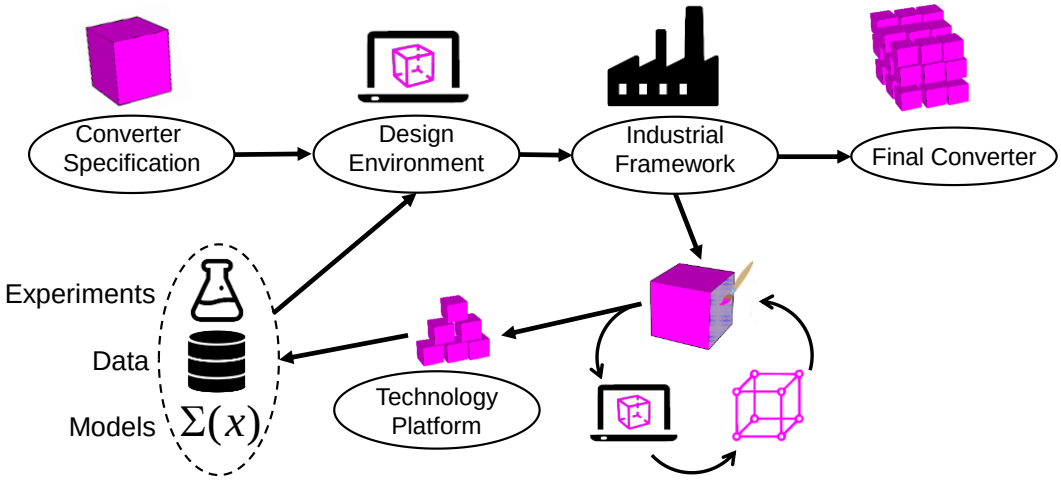


Figure 1.32 The diagram depicts the industrialization process of power converters, centered around the implementation of power converter arrays (PCAs). Adapted from [6].

Due to standardized and well stablished and divided function blocks, such as interconnections, filter and cooling, each standard block can be characterized, designed and optimized separately. To solve the issue of prototyping, it has been presented a methodology based on bricks/ or cells pre-characterized in which it can be assembled just like a “Lego” build an entire power converter. The methodology describing the PCA approach is well explained through the diagram presented in *Figure 1.32.*

In sum, the PCA can be constructed, optimized and predicted through first order and simplifying solutions in a computer aided design (CAD). It turns highly complex tasks, such as managing temperature and EMC into an almost intuitive puzzle problem of well comprehended and predictable structures. In this work, a different philosophy from ordinary fashion way of research is employed. Standardization, predictability and EMC improvement for automated design are, therefore, the master keys driving this thesis. As a result, the

decisions are deliberately taken not only considering efficiency and power density. Some advantages of standardization, include:

- Easy prototyping;
- Known supply chain;
- Carbon footprint, Life Cycle analysis, Circular economy and design for reuse [125];
- Open-source, since the technology stablishes standardizing principles that allows easier and sharing ideas;
- Easier to repair;
- Redundancy.

It is presented in *Table 1-I* and *Table 1-II*, the main electrical rated specification and component devices, respectively, treated in this work. The first Dab (Cell 1) was already available from previous work [5] [6]. Cells 2 and 3 have then been designed considering EMI constraints. Two versions of Cell 3 containing and not containing a ground plane has also been prototyped. The "motherboard", structure in which the cells are inserted has also been designed and prototyped. In *Figure 1.33*, it is presented the many prototypes used to characterize the EMI signature as well as experimental results validation in this work.

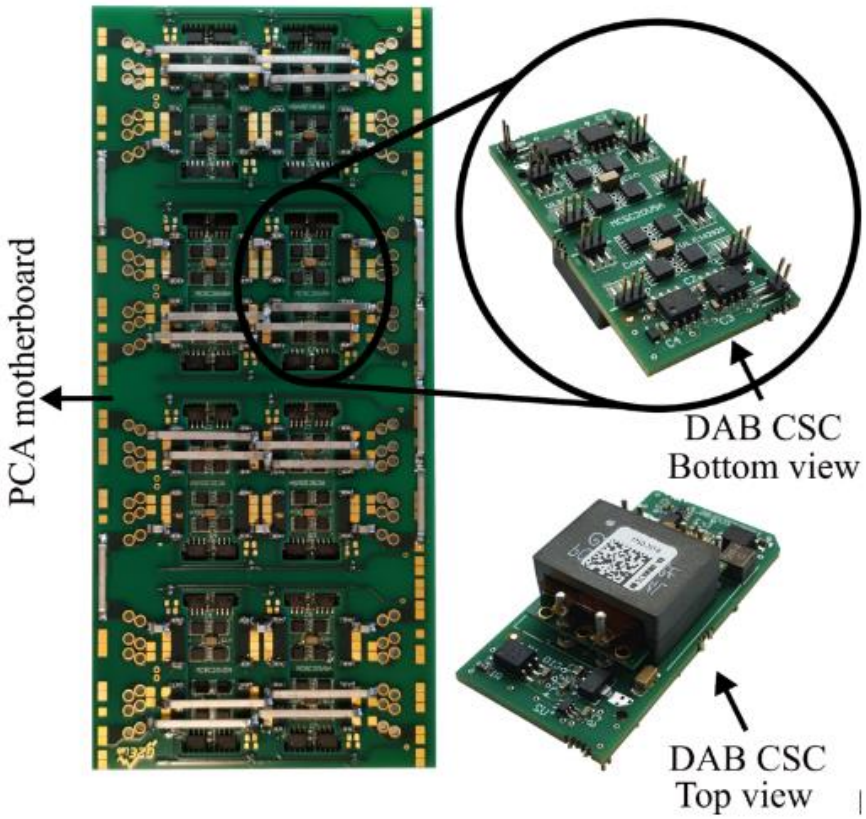
Table 1-I Prototype main electrical rated specifications.

Parameter	**Symbol**	**Value (Cell 1)**	**Value (Cell 2)**	**Value (Cell 3)**
Input voltage	V_i	20 (V)	20 (V)	20 (V)
Output voltage	V_o	20 (V)	20 (V)	20 (V)
Output power	P_o	100 W	100 W	100 W
Switching frequency	f_s	250 kHz	120 kHz	100 kHz

Table 1-II Prototype main component devices.

Component	**Symbol**	**(Cell 1) Value**	**(Cell 2) Value**	**(Cell 3) Value**
AC-link inductance	L_{ac}	1 x 350 (nH) XEL3530-301ME	2 x 540 (nH) XEL4030-471ME_	4 x 540 (nH)
Transformer		300 nH	300 nH	300 nH

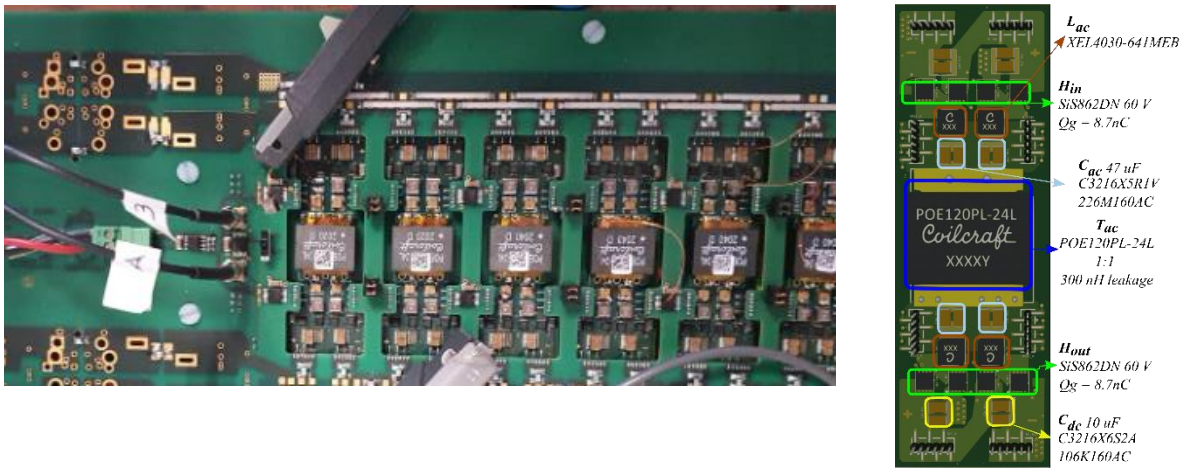
r = 1:1		Lk. induc. *Ref: POE120PL-24*	Lk. induc. *Ref: POE120PL-24*	Lk. induc. *Ref: POE120PL-24*
DC-link capacitance	C_i	20 uF	20 uF	5 x 20 uF
DC-link capacitance	C_o	20 uF	20 uF	5 x 20 uF
AC-link capacitance	C_{ac}	20 uF	20 uF	5 x 470 nF
Switch devices (Input)		N-Channel Si 5 mΩ 30 V C_{oss}: 730 pF @15V Ref: SiSA10DN	N-Channel Si 5 mΩ 30 V C_{oss}: 730 pF @15V Ref: SiSA10DN	N-Channel Si 16 mΩ 60 V C_{oss} 565 pF @25 V *Ref: SQS660CENW*
Switch devices (Output)		N-Channel Si 5 mΩ 30 V C_{oss}: 730 pF @15V Ref: SiSA10DN	N-Channel Si 5 mΩ 30 V C_{oss}: 730 pF @15V Ref: SiSA10DN	N-Channel Si 16 mΩ 60 V C_{oss} 565 pF @25 V *Ref: SQS660CENW*


PCA motherboard
DAB CSC
Bottom view
DAB CSC
Top view

(a)


POE120PL-24L
Coilcraft
XXXXY
L_{ac} 470 nH
XEL4030-471ME_
H_{in}
SISA10DN 30 V
Qg = 15.4nC
C_{ac} 22 uF
C3216X5R1V
226M160AC_
T_{ac}
POE120PL-24L
1:1
300 nH leakage
H_{out}
SISA10DN 30 V
Qg = 15.4nC
C_{dc} 10 uF
C3216X7R1H
106K160AC

(b)



(c)

Figure 1.33 Different version of CSCs and motherboard prototyped and/or tested through this thesis (a) Version CSC 1; (b) Version CSC 2; (c) Version CSC 3.

1.2.3 Goal and methodology

The objective of this thesis is to develop a methodology capable of analysing worst-case scenarios and trends efficiently, leveraging fast theoretical analytical results, as well as quick experimental results through simpler experimental setups and result interpretation. For example, the interconnections, path and source of radiated emission, can be studied detached from other blocks.

The analysis and observation of previous work consist in improving the design from acquired data as well as theoretical results as presented in *Figure 1.34*. Once analysed, the design of the CSCs is provided, privileging ZVS and lower impact on CM and DM noise for a given voltage and current profile.

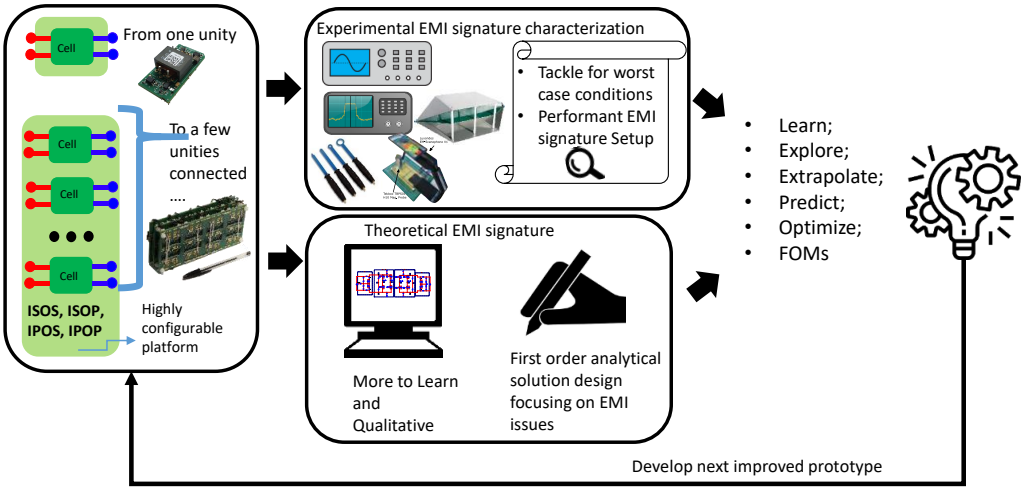


Figure 1.34 This diagram depicts the methodology based on EMI signature and learn from both theoretical and practical results.

Thereafter, methods for reducing CM noise in one single cell and the entire PCA are discussed and implemented, with significant reduction proved through theoretical and practical results. Different solutions for complying with EMC standards exist, as it has been extensively presented previously. The PCA design is focused either on the design phase of the cell, privileging not only efficiency, but also standardization and predictability. A diagram describing such statement is presented in *Figure 1.35*, exemplified with the filter design. Notice that, even though complete different solutions for different PCAS will exist, only one will be "looked for" for the many varieties of PCAs (number of cells, configuration etc), with the goal of standardization towards automated design for manufacturing process.

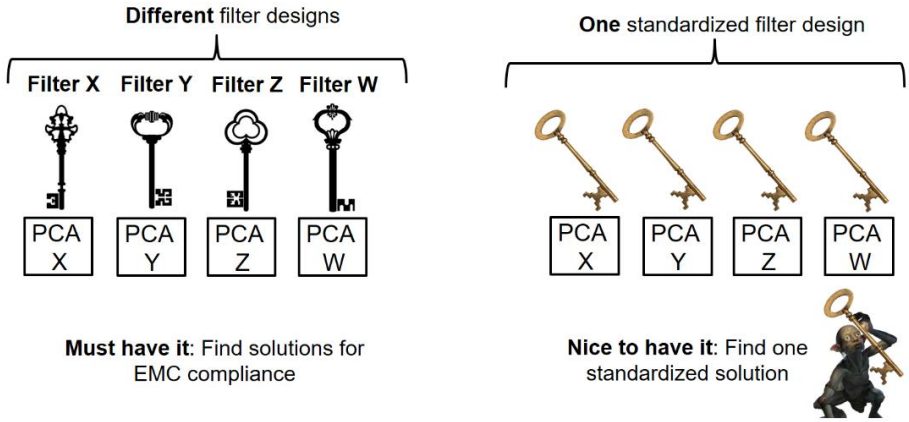


Figure 1.35 Different filter designs for different PCAs may be used, only one standardized will be chosen.

Hence, combining the data basing from experimental and theoretical results as presented in *Figure 1.34* as well as the standardized EMI attenuation solution, as in *Figure 1.35*, it is possible to affirm that this may significantly increase the speed of power electronics

converter design and industrialization, leading to a revolutionary power electronic design automation, as presented in *Figure 1.36*, compared to conventional methodology, as presented in *Figure 1.2*. The ultimate goal is to provide aided tool and guidance that are easy to follow, assuming it is possible to extrapolate in advance the EMI signature

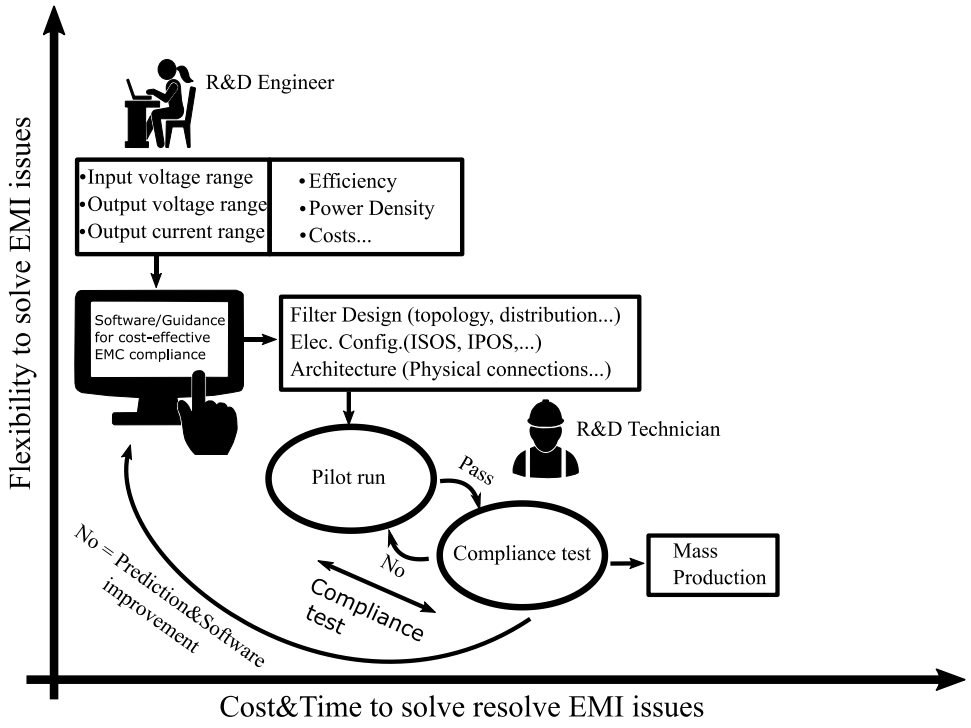


Figure 1.36 Design manufacture of automated design focusing on EMC in which this thesis aims to open an opportunity.

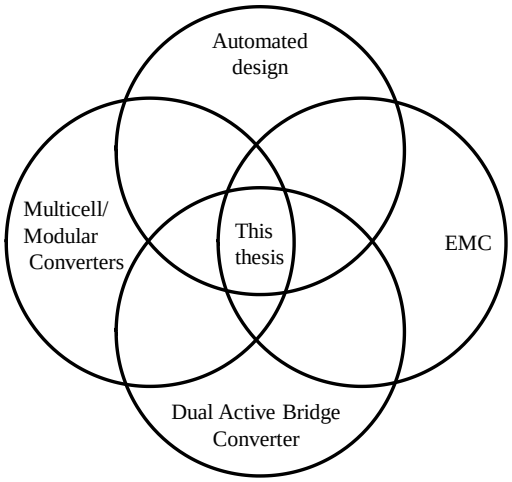


Figure 1.37 Lines of research investigated in this thesis.

To sum up, the line of research in this thesis is an intersection of different subjects such as multi-cell converters, automated design focus, EMC and Dual Active Bridge as presented in *Figure 1.37*. Finally, the methodology is presented for a DAB and low power

application (<MW), but it is not limited, being able of being implementing different “cells” for very different purposes such higher power or voltage applications.

Reference Chapter 1

[1] A. J. Marques Cardoso, "Power Electronics Design Methods and Automation in the Digital Era: Evolution of Design Automation Tools," *IEEE Power Electron. Mag.*, vol. 7, no. 2, pp. 36–40, Jun. 2020, doi: 10.1109/MPEL.2020.2988077.
[2] K. Hermanns, Y. Peng, and A. Mantooth, "The Increasing Role of Design Automation in Power Electronics: Gathering What Is Needed," *IEEE Power Electron. Mag.*, vol. 7, no. 1, pp. 46–50, Mar. 2020, doi: 10.1109/MPEL.2019.2959706.
[3] L. Kerachev, "Technologies de mise en oeuvre et stratégies de configuration de réseaux de micro-convertisseurs - Application au photovoltaïque," p. 210.
[4] O. Deleage, "Conception, réalisation et mise en oeuvre d'un micro-convertisseur intégré pour la conversion DC/DC," p. 202.
[5] T. Lamorelle, "Contribution à la conception et la production automatique en électronique de puissance via les réseaux de convertisseurs," p. 158.
[6] A. Andreta, "Automatic Design for Manufacturing in Power Electronics Based on Power Converter Arrays," p. 139.
[7] T. Lamorelle, A. Andreta, Y. Lembeye, J.-C. Crebier, and J.-C. Podvin, "Design level power electronics building block: Industrial framework for DC-DC conversion," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Lyon: IEEE, Feb. 2018, pp. 670–675. doi: 10.1109/ICIT.2018.8352258.
[8] M. Kasper, D. Bortis, and J. W. Kolar, "Scaling and balancing of multi-cell converters," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Hiroshima, Japan: IEEE, May 2014, pp. 2079–2086. doi: 10.1109/IPEC.2014.6869875.
[9] M. Kasper, C.-W. Chen, D. Bortis, J. W. Kolar, and G. Deboy, "Hardware verification of a hyper-efficient (98%) and super-compact (2.2kW/dm^3) isolated AC/DC telecom power supply module based on multi-cell converter approach," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, USA: IEEE, Mar. 2015, pp. 65–71. doi: 10.1109/APEC.2015.7104333.
[10] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002, doi: 10.1109/TIE.2002.803174.
[11] D. A. Herrera-Jaramillo, E. E. Henao-Bravo, D. González Montoya, C. A. Ramos-Paja, and A. J. Saavedra-Montes, "Control-Oriented Model of Photovoltaic Systems Based on a Dual Active Bridge Converter," *Sustainability*, vol. 13, no. 14, p. 7689, Jul. 2021, doi: 10.3390/su13147689.
[12] E. E. Henao-Bravo, C. A. Ramos-Paja, A. J. Saavedra-Montes, D. González-Montoya, and J. Sierra-Pérez, "Design Method of Dual Active Bridge Converters for Photovoltaic Systems with High Voltage Gain," *Energies*, vol. 13, no. 7, p. 1711, Apr. 2020, doi: 10.3390/en13071711.
[13] E. L. Carvalho, L. H. Meneghetti, E. G. Carati, J. P. da Costa, C. M. de O. Stein, and R. Cardoso, "Asymmetrical Pulse-Width Modulation Strategy for Current-Fed Dual Active Bridge Bidirectional Isolated Converter Applied to Energy Storage Systems," *Energies*, vol. 13, no. 13, p. 3475, Jul. 2020, doi: 10.3390/en13133475.
[14] H. Choi, W. Lee, and J. Jung, "Practical Controller Design of Three-Phase Dual Active Bridge Converter for Low Voltage DC Distribution System," *Electronics*, vol. 9, no. 12, p. 2101, Dec. 2020, doi: 10.3390/electronics9122101.
[15] M. A. Shamshuddin, F. Rojas, R. Cardenas, J. Pereda, M. Diaz, and R. Kennel, "Solid State Transformers: Concepts, Classification, and Control," *Energies*, vol. 13, no. 9, p. 2319, May 2020, doi: 10.3390/en13092319.

[16] R. Redl, “Power electronics and electromagnetic compatibility,” in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, Baveno, Italy: IEEE, 1996, pp. 15–21. doi: 10.1109/PESC.1996.548553.
[17] P. Mathur and S. Raman, “Electromagnetic Interference (EMI): Measurement and Reduction Techniques,” *Journal of Elec Materi*, vol. 49, no. 5, pp. 2975–2998, May 2020, doi: 10.1007/s11664-020-07979-1.
[18] T. Hegarty, “An overview of conducted EMI specifications for power supplies,” p. 7, 2018.
[19] T. Hegarty, “An overview of radiated EMI specifications for power supplies,” p. 12, 2018.
[20] Y. S. Ban, “Electromagnetic Emission FCC MEASUREMENT REPORT.” BWS Tesging Laboratory, Oct. 07, 2020. Accessed: Oct. 19, 2022. [Online]. Available: https://fcc.report/FCC-ID/2AXQD-ASP-2000/4946949.pdf
[21] M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, “Design of a Highly Efficient (97.7%) and Very Compact (2.2 kW/dm ^{3}) Isolated AC–DC Telecom Power Supply Module Based on the Multicell ISOP Converter Approach,” *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7750–7769, Oct. 2017, doi: 10.1109/TPEL.2016.2633334.
[22] K. S. Kostov, S. Schroth, F. Krismer, M. Priecinsky, H.-P. Nee, and J. W. Kolar, “The Input Impedance of Common-Mode and Differential-Mode Noise Separators,” *IEEE Trans. on Ind. Applicat.*, vol. 51, no. 3, pp. 2352–2360, May 2015, doi: 10.1109/TIA.2014.2370094.
[23] M. Chaluvadi, G. Vincentraj, and K. G. Thomas, “A Comparison Study on Conducted Emission Test in International EMC Standards,” in *2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI)*, Chennai: IEEE, Sep. 2017, pp. 1352–1355. doi: 10.1109/ICPCSI.2017.8391931.
[24] Anritsu Corporation, “Technical note ‘The Basis of Spectrum Analyzers.’” Accessed: Oct. 18, 2022. [Online]. Available: https://www.naic.edu/~phil/hardware/Misc/anritsu/SpectrumAnalyzer_basis_of.pdf
[25] C. Rauscher, V. Janssen, R. Minihold, and C. Rauscher, *Fundamentals of spectrum analysis*, 9. ed. München: Rohde & Schwarz, 2016.
[26] CISPR 22, “Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement.” Oct. 04, 2006.
[27] A. Bendicks, “MATLAB/Octave function to evaluate time-domain signals according to the measurement bandwidth and average/peak detector of EMI test receivers”.
[28] A. A. Takach, “Design and Investigation of the Use of TEM Cells in the Characterization ofUnderground Targets”.
[29] A. A. Takach, F. Ndagijimana, J. Jomaah, and M. Al-Husseini, “Position optimization for Probe Calibration Enhancement Inside the TEM Cell,” in *2018 IEEE International Multidisciplinary Conference on Engineering Technology (IMCET)*, Beirut: IEEE, Nov. 2018, pp. 1–5. doi: 10.1109/IMCET.2018.8603026.
[30] R. A. Menke, “A FULL SYSTEM CHARACTERIZATION OF THE MEASUREMENT UNCERTAINTY OF A CONDUCTED EMISSIONS MEASUREMENT SYSTEM”.
[31] A. D. Brovont, “Generalized Differential-Common-Mode Decomposition for Modeling Conducted Emissions in Asymmetric Power Electronic Systems,” *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6461–6466, Aug. 2018, doi: 10.1109/TPEL.2018.2789348.
[32] A. D. Brovont and A. N. Lemmon, “Common-mode/differential-mode interactions in asymmetric converter structures,” in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, Arlington, VA, USA: IEEE, Aug. 2017, pp. 84–90. doi: 10.1109/ESTS.2017.8069264.
[33] A. N. Lemmon, A. D. Brovont, C. D. New, B. W. Nelson, and B. T. DeBoi, “Modeling and Validation of Common-Mode Emissions in Wide Bandgap-Based Converter

Structures," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8034–8049, Aug. 2020, doi: 10.1109/TPEL.2019.2963883.
[34] A. D. Brovont and S. D. Pekarek, "Derivation and Application of Equivalent Circuits to Model Common-Mode Current in Microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 297–308, Mar. 2017, doi: 10.1109/JESTPE.2016.2642835.
[35] A. N. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. D. Brovont, and M. S. Mazzola, "Methodology for Characterization of Common-Mode Conducted Electromagnetic Emissions in Wide-Bandgap Converters for Ungrounded Shipboard Applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 300–314, Mar. 2018, doi: 10.1109/JESTPE.2017.2721429.
[36] S. Negri, X. Wu, X. Liu, F. Grassi, G. Spadacini, and S. A. Pignari, "Mode Conversion in DC-DC Converters with Unbalanced Busbars," in *2019 Joint International Symposium on Electromagnetic Compatibility, Sapporo and Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Sapporo/APEMC)*, Sapporo, Japan: IEEE, Jun. 2019, pp. 112–115. doi: 10.23919/EMCTokyo.2019.8893915.
[37] S. Wang and F. C. Lee, "Investigation of the Transformation Between Differential-Mode and Common-Mode Noises in an EMI Filter Due to Unbalance," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 3, pp. 578–587, Aug. 2010, doi: 10.1109/TEMC.2009.2038899.
[38] J. J. Kyyrä and K. S. Kostov, "Insertion loss in terms of four-port network parameters," *IET Science, Measurement & Technology*, vol. 3, no. 3, pp. 208–216, May 2009, doi: 10.1049/iet-smt:20080107.
[39] K. Kostov, "DESIGN AND CHARACTERIZATION OF SINGLE-PHASE POWER FILTERS," 2009.
[40] T. Lamorelle, Y. Lembeye, and J.-C. Crebier, "Handling Differential Mode Conducted EMC in Modular Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5812–5819, Jun. 2020, doi: 10.1109/TPEL.2019.2947735.
[41] B. Bertoldi, "Systematic Procedures for the Design of Passive Components Applied to a High Performance Three-Phase Rectifier," 2021.
[42] K. Raggl, T. Nussbaumer, and J. W. Kolar, "Guideline for a Simplified Differential-Mode EMI Filter Design," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 1031–1040, Mar. 2010, doi: 10.1109/TIE.2009.2028293.
[43] F. Salomez, "Modélisation des effets capacitifs des bobines simple couche et choix du matériau magnétique du noyau pour le dimensionnement des filtres CEM," PhD Thesis, 2022. [Online]. Available: http://www.theses.fr/2022ULILN029/document
[44] L. Zhai, G. Hu, M. Lv, T. Zhang, and R. Hou, "Comparison of Two Design Methods of EMI Filter for High Voltage Power Supply in DC-DC Converter of Electric Vehicle," *IEEE Access*, vol. 8, pp. 66564–66577, 2020, doi: 10.1109/ACCESS.2020.2985528.
[45] J. Everts, "Design and Optimization of an Efficient (96.1%) and Compact (2 kW/dm3) Bidirectional Isolated Single-Phase Dual Active Bridge AC-DC Converter," *Energies*, vol. 9, no. 10, p. 799, Oct. 2016, doi: 10.3390/en9100799.
[46] A. Ales, Jl. Schanen, J. Roudet, and D. Moussaoui, "A new analytical EMC model of power electronics converters based on quadripole system: Application to demonstrate the mode decoupling condition," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, USA: IEEE, Mar. 2015, pp. 2684–2690. doi: 10.1109/APEC.2015.7104730.
[47] M. Foissac, J.-L. Schanen, and C. Vollaire, "“Black box” EMC model for power electronics converter," in *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA: IEEE, Sep. 2009, pp. 3609–3615. doi: 10.1109/ECCE.2009.5316113.

[48] F. A. Kharanaq, A. Emadi, and B. Bilgin, “Modeling of Conducted Emissions for EMI Analysis of Power Converters: State-of-the-Art Review,” *IEEE Access*, vol. 8, pp. 189313–189325, 2020, doi: 10.1109/ACCESS.2020.3031693.
[49] J.-C. Crébier, “CONTRIBUTION A L’ETUDE DES PERTURBATIONS CONDUITES DANS LES REDRESSEURS COMMANDES,” 1992.
[50] S. Wang, P. Kong, and Fred. C. Lee, “Common Mode Noise Reduction for Boost Converters Using General Balance Technique,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007, doi: 10.1109/TPEL.2007.900503.
[51] Y. Zhang, S. Wang, and Y. Chu, “Comparison of Radiated Electromagnetic Interference (EMI) Generated by Power Converters with Silicon MOSFETs and GaN HEMTs,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA: IEEE, Mar. 2019, pp. 1375–1382. doi: 10.1109/APEC.2019.8722225.
[52] H. Zhang, S. Wang, Y. Li, Q. Wang, and D. Fu, “Two-Capacitor Transformer Winding Capacitance Models for Common-Mode EMI Noise Analysis in Isolated DC–DC Converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8458–8469, Nov. 2017, doi: 10.1109/TPEL.2017.2650952.
[53] V. Tarateeraseth, “EMI Filter Design Part I: Conducted EMI Generation Mechanism”.
[54] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, “Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC–DC Converters,” *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2800–2810, Jul. 2012, doi: 10.1109/TIE.2010.2046005.
[55] R. Barlik, “Determination of the basic parameters of the high-frequency planar transformer,” *ELECTROTECHNICAL REVIEW*, vol. 1, no. 6, pp. 73–80, Jun. 2016, doi: 10.15199/48.2016.06.13.
[56] Z. Ouyang and M. A. E. Andersen, “Overview of Planar Magnetic Technology—Fundamental Properties,” *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4888–4900, Sep. 2014, doi: 10.1109/TPEL.2013.2283263.
[57] B. Cui, P. Xue, and X. Jiang, “Elimination of High Frequency Oscillation in Dual Active Bridge Converters by dv/dt Optimization,” *IEEE Access*, vol. 7, pp. 55554–55564, 2019, doi: 10.1109/ACCESS.2019.2910597.
[58] Naizeng Wang, Haiyang Jia, Mofan Tian, ZhenWei Li, GuangZhao Xu, and Xu Yang, “Impact of transformer stray capacitance on the conduction loss in a GaN-based LLC resonant converter,” in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, Taiwan: IEEE, Jun. 2017, pp. 1334–1338. doi: 10.1109/IFEEC.2017.7992237.
[59] Himanshu *et al.*, “High Frequency Transformer’s Parasitic Capacitance Minimization for Photovoltaic (PV) High-Frequency Link-Based Medium Voltage (MV) Inverter,” *Electronics*, vol. 7, no. 8, p. 142, Aug. 2018, doi: 10.3390/electronics7080142.
[60] M. A. Saket, N. Shafiei, and M. Ordonez, “LLC Converters With Planar Transformers: Issues and Mitigation,” *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4524–4542, Jun. 2017, doi: 10.1109/TPEL.2016.2602360.
[61] D. Barater, E. Lorenzani, C. Concari, G. Franceschini, and G. Buticchi, “Recent advances in single-phase transformerless photovoltaic inverters,” *IET Renewable Power Generation*, vol. 10, no. 2, pp. 260–273, Feb. 2016, doi: 10.1049/iet-rpg.2015.0101.
[62] K. Zeb *et al.*, “A Review on Recent Advances and Future Trends of Transformerless Inverter Structures for Single-Phase Grid-Connected Photovoltaic Systems,” *Energies*, vol. 11, no. 8, p. 1968, Jul. 2018, doi: 10.3390/en11081968.
[63] H. Zhang, S. Wang, Y. Li, Q. Wang, and D. Fu, “Two-Capacitor Transformer Winding Capacitance Models for Common-Mode EMI Noise Analysis in Isolated DC–DC Converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8458–8469, Nov. 2017, doi: 10.1109/TPEL.2017.2650952.
[64] F. Blache, J.-P. Keradec, and B. Cogitore, “Stray capacitances of two winding transformers: equivalent circuit, measurements, calculation and lowering,” in *Proceedings of*

1994 IEEE Industry Applications Society Annual Meeting, Denver, CO, USA: IEEE, 1994, pp. 1211–1217. doi: 10.1109/IAS.1994.377552.
[65] A. Schellmanns, J.-P. Keradec, J.-L. Schanen, and K. Berrouche, "Representing electrical behaviour of transformers by lumped element circuits: a global physical approach," in *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No.99CH36370)*, Phoenix, AZ, USA: IEEE, 1999, pp. 2100–2107. doi: 10.1109/IAS.1999.806025.
[66] M. I. Hassan, N. Keshmiri, A. D. Callegaro, M. F. Cruz, M. Narimani, and A. Emadi, "Design Optimization Methodology for Planar Transformers for More Electric Aircraft," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 568–583, 2021, doi: 10.1109/OJIES.2021.3124732.
[67] A. Baccigalupi, P. Daponte, and D. Grimaldi, "On a circuit theory approach to evaluate the stray capacitances of two coupled inductors," *IEEE Trans. Instrum. Meas.*, vol. 43, no. 5, pp. 774–776, Oct. 1994, doi: 10.1109/19.328886.
[68] I. Grobler and M. Gitau, "Modelling and measurement of high switching frequency conducted EMI," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, Austria: IEEE, Nov. 2013, pp. 1031–1036. doi: 10.1109/IECON.2013.6699275.
[69] C. Liu, L. Qi, X. Cui, and X. Wei, "Experimental Extraction of Parasitic Capacitances for High-Frequency Transformers," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4157–4167, Jun. 2017, doi: 10.1109/TPEL.2016.2597498.
[70] "Cui et al. - 2019 - Elimination of High Frequency Oscillation in Dual .pdf."
[71] C. Liu, L. Qi, X. Cui, Z. Shen, and X. Wei, "Wideband Mechanism Model and Parameter Extracting for High-Power High-Voltage High-Frequency Transformers," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3444–3455, May 2016, doi: 10.1109/TPEL.2015.2464722.
[72] L. Xie, X. Ruan, and Z. Ye, "Equivalent Noise Source: An Effective Method for Analyzing Common-Mode Noise in Isolated Power Converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2913–2924, May 2016, doi: 10.1109/TIE.2016.2517064.
[73] Y. Yang, D. Huang, F. C. Lee, and Q. Li, "Transformer shielding technique for common mode noise reduction in isolated converters," in *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, USA: IEEE, Sep. 2013, pp. 4149–4153. doi: 10.1109/ECCE.2013.6647252.
[74] Y. Chu, A. Kumar, and Y. Ramadass, "Common-Mode EMI Cancellation in Full-Bridge Based Isolated DC-DC Converters," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA: IEEE, Jun. 2021, pp. 284–291. doi: 10.1109/APEC42165.2021.9487124.
[75] Y. Chu and S. Wang, "A Generalized Common-Mode Current Cancelation Approach for Power Converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4130–4140, Jul. 2015, doi: 10.1109/TIE.2014.2387335.
[76] L. Xie, X. Ruan, and Z. Ye, "Reducing Common Mode Noise in Phase-Shifted Full-Bridge Converter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7866–7877, Oct. 2018, doi: 10.1109/TIE.2018.2803761.
[77] P. Kong and F. C. Lee, "Transformer structure and its effects on common mode EMI noise in isolated power converters," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, USA: IEEE, Feb. 2010, pp. 1424–1429. doi: 10.1109/APEC.2010.5433416.
[78] M. A. Saket, M. Ordonez, and N. Shafiei, "Planar Transformers With Near-Zero Common-Mode Noise for Flyback and Forward Converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1554–1571, Feb. 2018, doi: 10.1109/TPEL.2017.2679717.

[79] K. Fu and W. Chen, “Evaluation Method of Flyback Converter Behaviors on Common-Mode Noise,” *IEEE Access*, vol. 7, pp. 28019–28030, 2019, doi: 10.1109/ACCESS.2019.2902462.
[80] M. Borage, S. Tiwari, and S. Kotaiah, “Common-mode noise source and its passive cancellation in full-bridge resonant converter,” in *8th International Conference on Electromagnetic Interference and Compatibility*, Chennai, India: IEEE, 2003, pp. 9–14. doi: 10.1109/ICEMIC.2003.237835.
[81] M. Pahlevaninezhad, D. Hamza, and P. K. Jain, “An Improved Layout Strategy for Common-Mode EMI Suppression Applicable to High-Frequency Planar Transformers in High-Power DC/DC Converters Used for Electric Vehicles,” *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1211–1228, Mar. 2014, doi: 10.1109/TPEL.2013.2260176.
[82] M. Pahlevani, D. Hamza, and P. Jain, “High frequency analysis of an integrated planar transformer with common mode EMI suppression capability,” in *2013 IEEE Energy Conversion Congress and Exposition*, Denver, CO, USA: IEEE, Sep. 2013, pp. 3700–3705. doi: 10.1109/ECCE.2013.6647189.
[83] Y. Li, H. Zhang, S. Wang, H. Sheng, C. P. Chng, and S. Lakshmikanthan, “Investigating Switching Transformers for Common Mode EMI Reduction to Remove Common Mode EMI Filters and Y-Capacitors in Flyback Converters,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2287–2301, Dec. 2018, doi: 10.1109/JESTPE.2018.2827041.
[84] H. Zhao, J. Yao, and S. Wang, “A Universal DM/CM Physical Model for Power Transformer EMI Analysis within both Conducted and Radiated Frequency Ranges,” in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA: IEEE, Sep. 2018, pp. 6592–6599. doi: 10.1109/ECCE.2018.8558313.
[85] J. Wang *et al.*, “Accurate Modeling of the Effective Parasitic Parameters for the Laminated Busbar Connected With Paralleled SiC MOSFETs,” *IEEE Trans. Circuits Syst. I*, vol. 68, no. 5, pp. 2107–2120, May 2021, doi: 10.1109/TCSI.2021.3064010.
[86] K. Ishikawa, S. Ogasawara, M. Takemoto, and K. Orikawa, “Development of an SiC High-Frequency PWM Inverter Using a Thick Multilayer PCB to Minimize Stray Inductance,” in *2018 International Power Electronics Conference (IPEC-Niigata 2018 - ECCE Asia)*, Niigata: IEEE, May 2018, pp. 2725–2731. doi: 10.23919/IPEC.2018.8507376.
[87] M. Pulvirenti, L. Salvo, A. G. Sciacca, G. Scelba, and M. Cacciato, “Modeling of SiC-MOSFET Converter Leg Including Parasitics of Printed Circuit Board Layout and Device Packaging,” in *2020 22nd European Conference on Power Electronics and Applications (EPE’20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, p. P.1-P.10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215618.
[88] M. Ali, J.-K. Muller, J. Friebe, and A. Mertens, “Analysis of Switching Performance and EMI Emission of SiC Inverters under the Influence of Parasitic Elements and Mutual Couplings of the Power Modules,” in *2020 22nd European Conference on Power Electronics and Applications (EPE’20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, p. P.1-P.10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215600.
[89] M. Ali, J. Friebe, and A. Mertens, “Simplified Calculation of Parasitic Elements and Mutual Couplings of Wide-bandgap Power Semiconductor Modules,” in *2020 22nd European Conference on Power Electronics and Applications (EPE’20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, p. P.1-P.10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215953.
[90] C. Kueck, “Application Note 139 October 2012”.
[91] W. Belloumi, A. Breard, J. Ben Hadj Slama, and C. Vollaire, “Numerical approach to study layout influence on electromagnetic emissions signature,” in *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, Suntec City, Singapore: IEEE, May 2018, pp. 1093–1098. doi: 10.1109/ISEMC.2018.8393956.

[92] W. Belloumi, A. Breard, J. Ben Hadj Slama, and C. Vollaire, "Impact of Layout on the Conducted Emissions of a DC-DC Converter Using Numerical Approach," in *2018 15th International Multi-Conference on Systems, Signals & Devices (SSD)*, Hammamet: IEEE, Mar. 2018, pp. 287–291. doi: 10.1109/SSD.2018.8570701.
[93] N. R. Mehrabadi, I. Cvetkovic, J. Wang, R. Burgos, and D. Boroyevich, "Busbar design for SiC-based H-bridge PEBB using 1.7 kV, 400 a SiC MOSFETs operating at 100 kHz," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA: IEEE, Sep. 2016, pp. 1–7. doi: 10.1109/ECCE.2016.7854903.
[94] H. Wang, L. Jiang, X. Wu, M. Shao, B. Wang, and X. Wu, "Design of Onboard 270V/28V DAB Converter for Optimized Parasitic Paramters," in *2022 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, Haining, China: IEEE, Oct. 2022, pp. 1–6. doi: 10.1109/ITECAsia-Pacific56316.2022.9942115.
[95] M. Zhu, C. Shao, S. Wang, L. Hang, Y. He, and S. Fan, "System Design of Dual Active Bridge (DAB) Converter Based on GaN HEMT Device," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, Harbin, China: IEEE, Aug. 2019, pp. 1–6. doi: 10.1109/ICEMS.2019.8921597.
[96] W. Xu, R. yang Yu, Z. Guo, and A. Q. Huang, "Design of 1500V/200kW 99.6% Efficiency Dual Active Bridge Converters Based on 1700V SiC Power MOSFET Module," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA: IEEE, Oct. 2020, pp. 6000–6007. doi: 10.1109/ECCE44975.2020.9235903.
[97] S. Kumar and G. Gohil, "Conducted EMI Performance of Active Neutral Point Clamped Phase Leg for Dual Active Bridge Converter based DC system," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA: IEEE, Mar. 2020, pp. 1697–1704. doi: 10.1109/APEC39645.2020.9124272.
[98] S. Kumar, B. Akin, and G. Gohil, "EMI Performance of Active Neutral Point Clamped Phase Leg for Dual Active Bridge DC–DC Converter," *IEEE Trans. on Ind. Applicat.*, vol. 57, no. 6, pp. 6093–6104, Nov. 2021, doi: 10.1109/TIA.2021.3102000.
[99] Y. Zhang, S. Wang, and Y. Chu, "Analysis and Comparison of the Radiated Electromagnetic Interference Generated by Power Converters With Si MOSFETs and GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8050–8062, Aug. 2020, doi: 10.1109/TPEL.2020.2972342.
[100] D. J. Costinett, "Analysis and Design of High Efficiency, High Conversion Ratio, DC-DC Power Converters," p. 308.
[101] Y. Yan, Y. Huang, R. Chen, and H. Bai, "Building Common-Mode Analytical Model for Dual Active Bridge Incorporating With Different Modulation Strategies," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12608–12619, Nov. 2021, doi: 10.1109/TPEL.2021.3071440.
[102] M. R. Yazdani, H. Farzanehfard, and J. Faiz, "Classification and Comparison of EMI Mitigation Techniques in Switching Power Converters - A Review," *Journal of Power Electronics*, vol. 11, no. 5, pp. 767–777, Sep. 2011, doi: 10.6113/JPE.2011.11.5.767.
[103] L. Zhai, G. Hu, M. Lv, T. Zhang, and R. Hou, "Comparison of Two Design Methods of EMI Filter for High Voltage Power Supply in DC-DC Converter of Electric Vehicle," *IEEE Access*, vol. 8, pp. 66564–66577, 2020, doi: 10.1109/ACCESS.2020.2985528.
[104] G. Buticchi, D. Barater, L. F. Costa, and M. Liserre, "A PV-Inspired Low-Common-Mode Dual-Active-Bridge Converter for Aerospace Applications," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10467–10477, Dec. 2018, doi: 10.1109/TPEL.2018.2801845.
[105] D. Han, C. T. Morris, and B. Sarlioglu, "Common-Mode Voltage Cancellation in PWM Motor Drives With Balanced Inverter Topology," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2683–2688, Apr. 2017, doi: 10.1109/TIE.2016.2633234.
[106] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "Active Suppression of Selected DC Bus Harmonics for Dual Active Bridge DC–DC Converters," *IEEE Trans.*

Power Electron., vol. 32, no. 11, pp. 8857–8867, Nov. 2017, doi: 10.1109/TPEL.2016.2647078.
[107] B. Li, Q. Li, F. C. Lee, and Y. Yang, "A symmetrical resonant converter and PCB transformer structure for common mode noise reduction," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH: IEEE, Oct. 2017, pp. 5362–5368. doi: 10.1109/ECCE.2017.8096898.
[108] S. Kumar, S. K. Voruganti, and G. Gohil, "Common-mode Current Analysis and Cancellation Technique for Dual Active Bridge Converter based DC System".
[109] L. Yang, H. Zhao, S. Wang, and Y. Zhi, "Common-Mode EMI Noise Analysis and Reduction for AC–DC–AC Systems With Paralleled Power Modules," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6989–7000, Jul. 2020, doi: 10.1109/TPEL.2019.2957358.
[110] P. Kong, S. Wang, F. C. Lee, and C. Wang, "Common-Mode EMI Study and Reduction Technique for the Interleaved Multichannel PFC Converter," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2576–2584, Sep. 2008, doi: 10.1109/TPEL.2008.2002090.
[111] M. S. S. Nia, P. Shamsi, and M. Ferdowsi, "EMC Modeling and Conducted EMI Analysis for a Pulsed Power Generator System Including an AC–DC–DC Power Supply," *IEEE Trans. Plasma Sci.*, vol. 48, no. 12, pp. 4250–4261, Dec. 2020, doi: 10.1109/TPS.2020.3035640.
[112] M. Maeda, T. Matsushima, T. Hisakado, and O. Wada, "Impedance balance control for reduction of common mode noise in full bridge converter," in *2015 International Conference on Electronic Packaging and iMAPS All Asia Conference (ICEP-IAAC)*, Kyoto, Japan: IEEE, Apr. 2015, pp. 695–699. doi: 10.1109/ICEP-IAAC.2015.7111100.
[113] M. Shoyama, Ge Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1095–1099, Dec. 2003, doi: 10.1109/TIE.2003.819677.
[114] B. Dwiza and J. Kalaiselvi, "Analytical Approach for Common Mode EMI Noise Analysis in Dual Active Bridge Converter," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, Singapore: IEEE, Oct. 2020, pp. 1279–1284. doi: 10.1109/IECON43393.2020.9254895.
[115] Y. Yan, H. Gui, and H. Bai, "Complete ZVS Analysis in Dual Active Bridge," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1247–1252, Feb. 2021, doi: 10.1109/TPEL.2020.3011470.
[116] Jin Zhi Li, T. Q. Zheng, and Ming Zhi He, "Common mode noise modeling and analysis of full-bridge DC-DC converter," in *Intelec 2012*, Scottsdale, AZ, USA: IEEE, Sep. 2012, pp. 1–7. doi: 10.1109/INTLEC.2012.6374490.
[117] I. A. Makda and M. Nymand, "Comparison of Common-Mode EMI Noise in a Phase-Shifted and Hard-Switched Full-Bridge Forward Converters," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium: IEEE, Sep. 2021, pp. 1–9. doi: 10.23919/EPE21ECCEEurope50061.2021.9570698.
[118] Y. Yan, Y. Huang, R. Chen, and H. Bai, "Building Common-Mode Analytical Model for Dual Active Bridge Incorporating With Different Modulation Strategies," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12608–12619, Nov. 2021, doi: 10.1109/TPEL.2021.3071440.
[119] J. Goff, "Electrical Design Handbook".
[120] Y. Feng, B. Shao, X. Tang, Y. Han, T. Wu, and Y. Suzuki, "Improved Capacitance Model Involving Fringing Effects for Electret-Based Rotational Energy Harvesting Devices," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1597–1603, Apr. 2018, doi: 10.1109/TED.2018.2803145.
[121] S. Mastuhisa, E. Ikuta, and T. Shimizu, "Common-mode EMI reduction method and filter configuration for equipment without grounding," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing: IEEE, Oct. 2017, pp. 7006–7011. doi: 10.1109/IECON.2017.8217225.

[122] A. N. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. D. Brovont, and M. S. Mazzola, "Methodology for Characterization of Common-Mode Conducted Electromagnetic Emissions in Wide-Bandgap Converters for Ungrounded Shipboard Applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 300–314, Mar. 2018, doi: 10.1109/JESTPE.2017.2721429.
[123] A. Andreta, L. F. Lavado Villa, Y. Lembeye, and J. C. Crebier, "A Novel Automated Design Methodology for Power Electronics Converters," *Electronics*, vol. 10, no. 3, p. 271, Jan. 2021, doi: 10.3390/electronics10030271.
[124] M. Kasper, "Analysis and Multi-Objective Optimization of Multi-Cell DC/DC and AC/DC Converter Systems," ETH Zurich, 2016. doi: 10.3929/ETHZ-A-010836609.
[125] B. Rahmani, M. Rio, Y. Lembeye, and J.-C. Crebier, "Design for Reuse: residual value monitoring of power electronics' components," *Procedia CIRP*, vol. 109, pp. 140–145, 2022, doi: 10.1016/j.procir.2022.05.227.
[126] M. L. Heldwein, "EMC Filtering of Three-Phase PWM Converters," ETH Zurich, 2008. doi: 10.3929/ETHZ-A-005635188.

2. Modelling and Design of the DAB under Single Phase-Shift (SPS) Modulation focusing on DM

Before entering into the topic of multi-cell converter approach, it is necessary to understand and optimize the EMI signature of a single DAB cell. In this *Chapter*, the analysis are focused on a single Dual Active Bridge converter (DAB) under Single Phase-Shift. In the context of Power Converter Arrays (at G2Elab), the input and output parameters as well as the load profile are not fixed. A generalized analysis of DM and CM has, therefore to be done, in order to ensure that the design and operation are compatible to any desired electrical characteristic. Such general analysis is useful as well for demonstrating mathematically the characteristics of the DAB, its limitation and figure of merits (FOM). Moreover, thanks to the proposed modelling technique, the design and its possible optimization are simplified, as the amount of variables and their domain are reduced. This chapter has, therefore, the goal of providing a comprehensive mathematical modelling technique and analysis focusing on the EMI behaviour of the DAB under Single Phase-Shift Modulation. It is important to highlight that the design and analysis focus not only on efficiency and volume optimization, but also the EMC aspects that are important for lowering EMI emissions and in turns necessary EMI shield and filters. The goal is to provide simplified equivalent circuits, advises that it will be able useful in the context of power converter arrays. In this work, analytical solutions are preferred, since they are capable of generalize and speed up the process of design.

2.1 Lossless DAB for DM analysis

The lossless model is first analyzed and it has been vastly addressed in the literature. The main advantage comparing to previous literature is that a normalized analysis in the output characteristic (Static gain vs parametrized output current) focusing not only on power density and efficiency, but also EMI aspects such as DM harmonics is performed. Then, considering the C_{oss} capacitance of MOSFETs, the ZVS realization in terms of another added dimensionless parameter. It is shown how the optimization can be performed in such plan by analyzing three parameters.

The following simplifying assumptions allow to draw important conclusions and are adopted for the modelling in this *Chapter*, and generally in this Thesis, except otherwise mentioned:

- The DAB is operated under classical SPS modulation [1];
- The input and output voltages are assumed to be a constant voltage sources;
- Only steady state operation is considered, and therefore, control and dynamics are out of scope of this thesis;
- The following non-ideal as propagation delays, dead-times [2], magnetic and switching losses [3] [4]. The series parasitic resistances [5] is modelled and discussed in Section 2.3, but for Section 2.1 and 2.2, it is neglected;
- The AC link capacitance is considered to be infinite and its effect [6] is neglected;
- The magnetizing inductance is considered to be infinite and its effect [7] is neglected;
- Profile charge (light load and heavy load) has equal importance for all operating points;
- Even though bidirectional, only unidirectional power flow analysis are depicted;

The input current of the DAB SPS is governed by a first order solution of two square-waves phase-shifted applied to an ideal AC-link inductor, as presented in *Figure 2.1* for a converter with a unity transformation ratio.

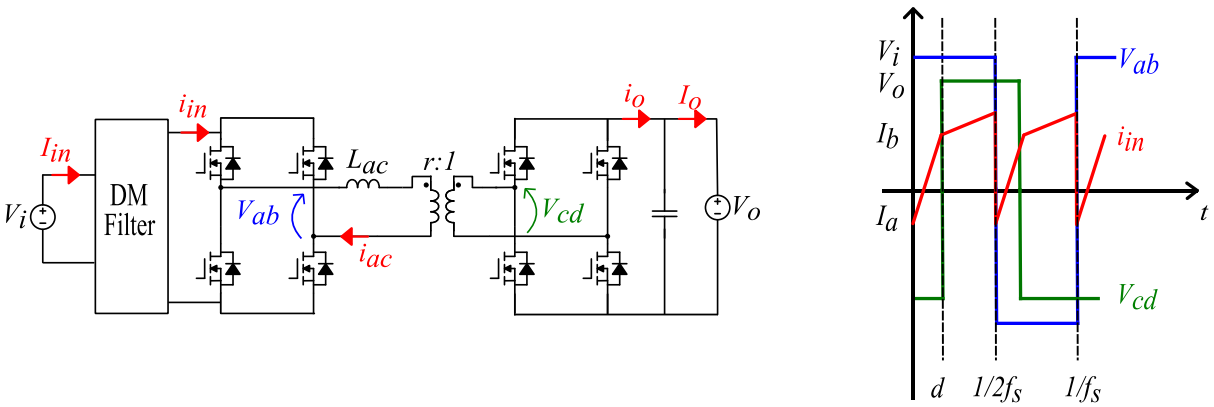


Figure 2.1 *Ideal electrical equivalent circuit of a DAB (left); Main waveforms (right).*

Where:

- V_i is the input voltage (V);
- V_o is the output voltage (V);
- I_o is the average output current (A);

- I_a and I_b are the currents during a switching event of the input and output H-bridges, respectively (A);
- f_s is the switching frequency (Hz);
- L_{ac} is the AC link equivalent total inductor (H);
- $d = \alpha/180$, in which α is the phase-shift in degrees from 0° to 90° (only positive power flow is analyzed throughout this thesis);

2.1.1 External Characteristic plane

Some of the future and trends of power electronic systems consists of multi-objective optimization designs such as power density, overall or peak efficiency, technology and economic viability [8]. Looking for best performance over large output voltage and/or current ranges while keeping high efficiency and power density requires a comprehensive mathematical modeling. For a power electronic converter, as presented in [9], assuring optimum power density while keeping high efficiency for the entire range of power is a challenging work as there is always a compromise between power density and efficiency. Therefore, analyzing the converter over a frame of operating points: static gain, input and output voltages and currents are fundamental for design optimization.

Particularly, it is known that the design of a DAB under phase-shift modulation requires a careful choice of the phase-shift, switching frequency and AC-link inductance regarding reactive power [10], ZVS operation [11], [12] for high-efficiency. Commonly, in the literature, these issues are usually treated with respect to output power [11], [12], making the analysis more specific to a single design. Besides output power information does not differentiate low voltage and high current from high voltage and low current applications.

As it is demonstrated through this *Chapter*, for a DAB converter, even at same output power operating points, getting the input and output voltage and current information is essential to analyze its performance characteristics. Similar to [7], the plane of the static gain, M (2.1), versus an output parametrized current γ (2.2), as presented in *Figure 2.2*, will be used for the sake of a generic, dimensionless and still meaningful analysis. Indeed, the analysis of the DAB (or any power converter) is designed with respect to a well-defined power and profile charge specifications. On the other hand, following the technology presented in G2Elab, the DAB should be capable of presenting rated output current of 2.5 A, overloading (with forced-air cooling (5 A)), wide input and output voltages (10 V, 40 V). It is true that such profile charge specification could be inputted in optimizing tools to generate designs and conclusions. On the other hand, it is possible to demonstrate, mathematically, that

a family of results can be analyzed through an output plan, limiting the design space domain and facilitating iteration in optimizing tools as well as portraying efficient and generic understanding of a power converter.

Throughout this work, the design is focused on $0.8 \leq M \leq 1.2$ with such capability of overloading when air-forced cooling, forming a rectangular region to be analyzed. The goal is, therefore, be able to choose a γ that optimizes a given important function. To exemplify, in *Figure 2.2*, it is presented two different designs with same profile charge (allowing double of the current and static gain from 0.8 to 1.2). Notice that the profile charge in this work is considering a rectangular shape, but any profile charge such as, the profile charge of battery could be analyzed.

Notice that, a simple lossless theoretical analysis is presented, and therefore, it does not allow finding separately the optimum f_s and L_{ac}, but rather its product $f_s L_{ac}$.

$$M = \frac{V_o}{V_i} \tag{2.1}$$

$$\gamma = \frac{2 f_s L_{ac} I_o}{V_i} \rightarrow \gamma = d(1-d)\,, if\ lossless \tag{2.2}$$

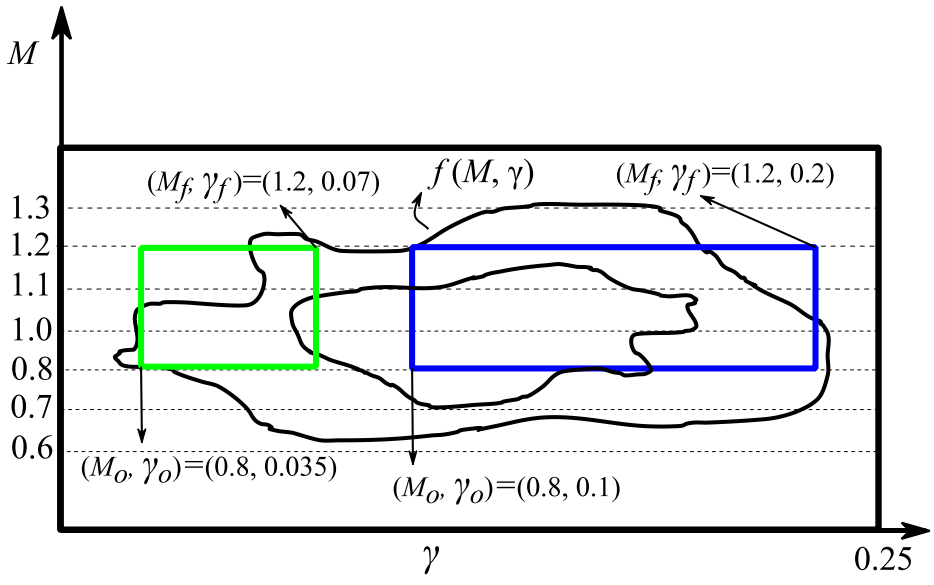


Figure 2.2 Use of the external characteristic plane ($M\ vs\ \gamma$) for two different designs in (green and blue) and equivalent profile charge in order to analyze a given function $f(M, \gamma)$.

Where:

- M_o is the minimum static gain equal to 0.8;

- M_f is the maximum static gain equal to 1.2;
- γ_o is parametrized output current with no overload nor forced-air cooling;
- γ_f is parametrized output current with no overload and no forced-air cooling. Notice that γ_f can also mean a decreasing in half of the input voltage (e.g. from 30 V, to 15 V);
- $f(M,\gamma)$ is a normalized function (ZVS boundary, RMS circulating current, Harmonic Distortion);

2.1.2 Normalized piecewise functions

When main waveforms are generated though differential equations by piecewise functions, the converter can entirely be analyzed analytically. The waveform of input current is the variable that will impact on RMS, harmonic distortion and ZVS realization, extremely necessary for EMI signature. The normalized piecewise function of the input current in the time domain, t, is described in (2.3), which is in function of the normalized currents switching instant at input and output H-bridges, presented, respectively in (2.4) and (2.5).

$$\frac{i_{in}(M,\gamma,f_s,t)}{I_o} = \begin{cases} \dfrac{2f_s(1+M)}{\gamma}t + \bar{I}_a(M,\gamma), & for\ 0 \le t \le \dfrac{1-\sqrt{1-4\gamma}}{4f_s} \\ \dfrac{2f_s(1-M)}{\gamma}\left(t - \dfrac{1-\sqrt{1-4\gamma}}{4f_s}\right) + & \\ \bar{I}_b(M,\gamma), & for\ \dfrac{1-\sqrt{1-4\gamma}}{4f_s} \le t \le \dfrac{1}{2f_s} \end{cases} \tag{2.3}$$

$$\bar{I}_a(M,\gamma) = \frac{I_a}{I_o} = \frac{M\sqrt{1-4\gamma}-1}{2\gamma} \tag{2.4}$$

$$\bar{I}_b(M,\gamma) = \frac{I_b}{I_o} = \frac{M-\sqrt{1-4\gamma}}{2\gamma} \tag{2.5}$$

A necessary condition for ZVS realization at input and output H-bridges are given by $\bar{I}_a < 0$ and $\bar{I}_b > 0$, respectively, yielding

$$ZVS\ condition \rightarrow \begin{cases} M < \dfrac{1}{\sqrt{1-4\gamma}}, & for\ input\ H-bridge \\ M > \sqrt{1-4\gamma}, & for\ output\ H-bridge \end{cases} \tag{2.6}$$

It is possible, therefore, to define the RMS current following the integration development (analytically or numerically) of (2.3) . The harmonic analysis can be approximated as presented in *Chapter 1*. For accurate information, the frequency domain is derived without loss of generality in the following section.

2.1.2.1 Normalized frequency domain analysis

The frequency domain modelling is known for its importance towards the prediction of EMI signature, specifically treating here the DM emissions. Such results can be found through numerical simulation. Its advantaged rely on analysis of very complex and detailed modeled, but the time consuming for drawing simple first order approximate results is unneglectable.

In [13], the DAB is modeled by imposing two square-waves (V_{ab} and V_{cd}) across an AC-link, modeled as a two-port admittance, Y, while observing the harmonic content. As in simulation approach, it is used to derive accurate results of complex systems, e.g dead-time effect, parasitic capacitances, joule and magnetic losses and etc. The harmonic spectrum results are run much faster than a simulation and accuracy is given by the n^{th} harmonic order composing the square-waves. On the other hand, as input and output voltages are imposed, the closed-solution requires numerical solution, and, therefore, the analysis are presented in the conventional *(M* vs d) plane, not desired in this section. Indeed, the approach can be seen as a very fast numeric simulation of a DAB in which the input and output voltage are modelled by voltage sources without output current control. For the simplifying aforementioned assumptions, the need of such tool is not required, and should be used only when analytical results become extremely complicated to be derived.

Finally, the frequency domain can be found from Fourier transformation analysis of the periodic normalized piecewise function (2.3), resulting (2.7) [1].

$$\frac{i_{in}(M,n,\gamma,t)}{I_o} = M + \sum_{n=1}^{\infty}\left(\bar{a}_n(M,\gamma,n)\cos(4\pi f_s n t) + \bar{b}_n(M,\gamma,n)\sin(4\pi f_s n t)\right) \tag{2.7}$$

$$\bar{a}_n(M,\gamma,n) = \frac{a_n(M,\gamma,n)}{I_o} = \frac{-2\sin\left(\pi\frac{1-\sqrt{1-4\gamma}}{2}n\right)M}{\pi^2 n^2 \gamma} \tag{2.8}$$

$$\bar{b}_n(M,\gamma,n) = \frac{b_n(M,\gamma,n)}{I_o} = \frac{\sin\left(2\pi\frac{1-\sqrt{1-4\gamma}}{2}n\right)M + \pi n\left(M - 2M\frac{1-\sqrt{1-4\gamma}}{2} - 1\right)}{\pi^2 n^2 \gamma} \tag{2.9}$$

For qualitative verification purposes, a comparison between piecewise time and Fourier series for the ten first harmonics is presented in *Figure 2.3*. Notice that the frequency of the input current DM corresponds in theory to the double of the switching frequency as illustrated in Fig. 2.1, meaning that even harmonics will be largely affected by the DM noise.

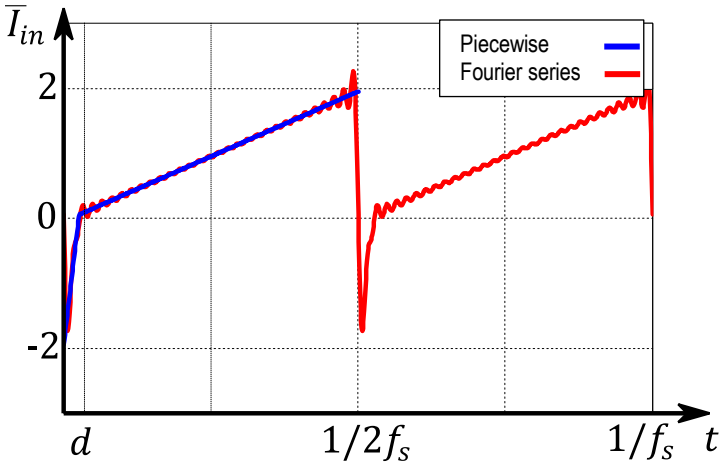


Figure 2.3 Normalized Input current of a piecewise time (in blue) and Fourier series containing the 10 first harmonics (in red) for a given operating $M = 0.9$ and $\gamma = 0.05$.

Once (2.7) has been validated theoretically, the harmonics, which are even multiples of the switching frequency can be expressed by (2.10). A computational simulation through PSIM for a given operating point is compared to the analytical results, as presented in *Figure 2.4*. The error is kept below 1% for all harmonic amplitudes, which confirms the correctness of equations.

$$\overline{H}_{DM} = \overline{H}_{DM}(M,\gamma,n) = \sqrt{\frac{\left(\bar{a}_n(M,\gamma,n)\right)^2 + \left(\bar{b}_n(M,\gamma,n)\right)^2}{2}} \tag{2.10}$$

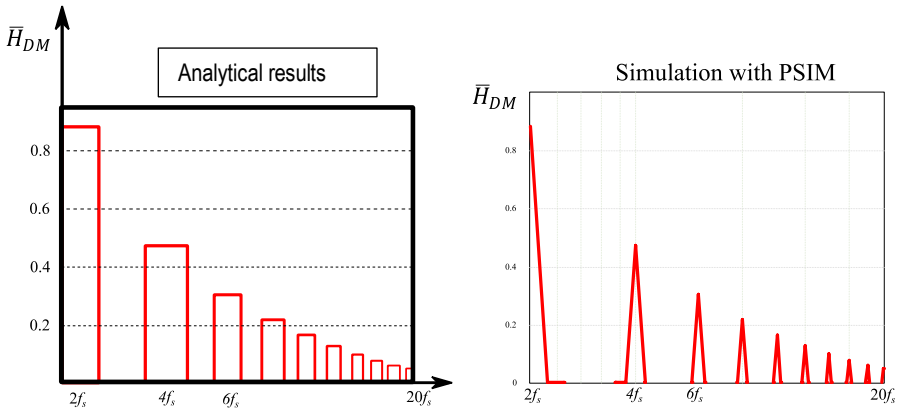


Figure 2.4 Spectrum of the normalized input current: (a) proposed analytical results (b) simulation results using PSIM.

Notice that, as expected and discussed in Chapter 1, the first harmonic is the highest one and it decays with an envelope of approximately -20 dB/dec, due to a more or less triangular shape. The focus on the DM filter should be on the first harmonic if it is allocated on the EMC standards, e.g EN5505. Nevertheless, in the case presented here, the switching frequency is higher than 100 kHz, and therefore, the first DM harmonic will be allocated higher than 200 kHz which is inside the CE frequency range. Therefore, by taking first harmonic in (2.10), it is possible map the first harmonic in the external characteristic plane, as presented in (2.11), in which plotting results are presented in *Figure 2.5*. Notice that the choice of γ is related to the limit desired for M in a given application and that there is an almost symmetrical behavior over the unitary gain behaviour.

$$\bar{H}_{1_{in}} = \bar{H}_{DM}(M, \gamma, 1) \tag{2.11}$$

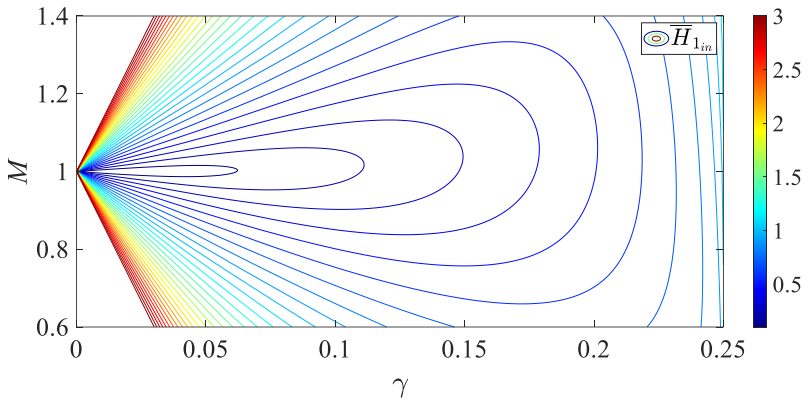


Figure 2.5 3D *mapping of normalized first harmonic magnitude in the external characteristic plane* (M *vs* γ).

The RMS current, as discussed in *Chapter 1*, is an image of the reactive power, and therefore, losses, useful for designing the DAB. It is possible to develop the normalized RMS value, as presented in (2.12) by applying the normalized the harmonic amplitudes presented in (2.10) .

$$\bar{I}_{in_{RMS}}(M,\gamma) = \frac{I_{RMS}(M,\gamma)}{I_o} = \sqrt{M^2 + \sum_{n=1}^{\infty}\left(\bar{H}_{DM}(M,\gamma,n)\right)^2} \tag{2.12}$$

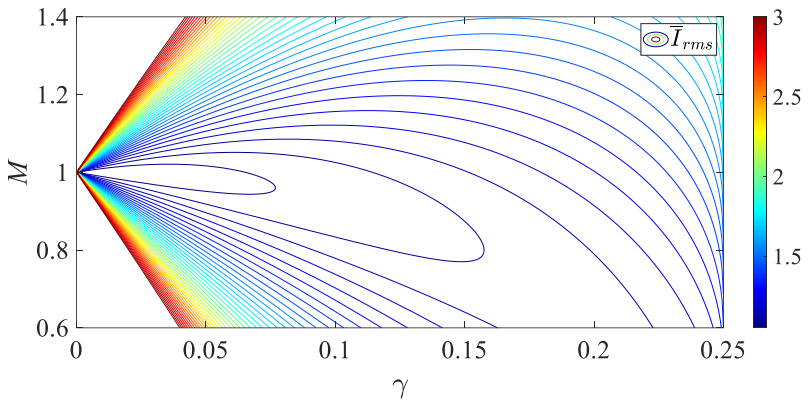


Figure 2.6 3D *mapping of normalized input RMS current in the external characteristic plane* (M *vs* γ).

As discussed in *Chapter 1*, if the RMS value is found through conventional integration of a piecewise equation, a parameter $\bar{I}_{ac_{RMS}}$ that contains all harmonics can be used for filter design. Such parameter is for now unnecessary since (2.11) is the exact solution. On the other hand, for the further analysis considering joule losses in *Section 2.2.3*, the Fourier series is not developed, and the analysis are performed considering the AC circulating current $\bar{I}_{ac_{RMS}}$, which is given in (2.13).

The division between $\bar{H}_{1_{in}}$ and $\bar{I}_{ac_{RMS}}$ is also an interesting parameter, named here e_f (2.14) interesting to investigate the error of the simplifying approach, and possibly use it for fitting simplifying cases.

$$\bar{I}_{AC_{RMS}}(M,\gamma) = \frac{\bar{I}_{AC_{RMS}}(M,\gamma)}{I_o} = \sqrt{\bar{I}_{in_{RMS}}{}^2 - \left(\frac{M}{\eta}\right)^2} \rightarrow \sqrt{\sum_{n=1}^{\infty}(\bar{H}_{DM})^2} \tag{2.13}$$

$$e_r = \frac{\bar{H}_{1_{in}}}{\bar{I}_{ac_{RMS}}} \tag{2.14}$$

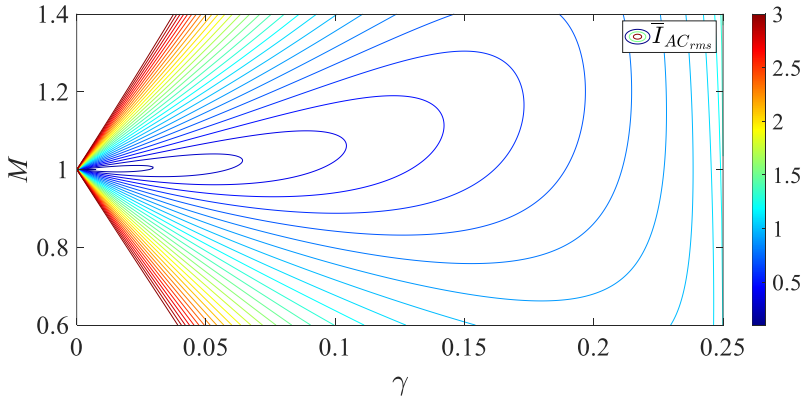


Figure 2.7 3D *mapping of normalized AC RMS circulating current in the external characteristic plane* ($M\ vs\ \gamma$).

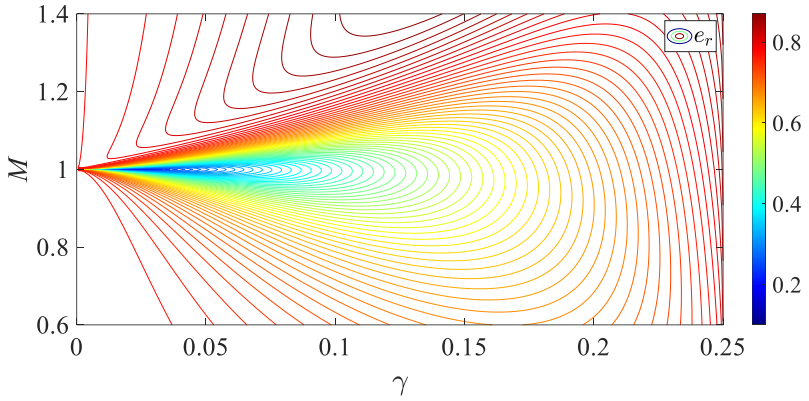


Figure 2.8 3D *mapping of the parameter* e_f *in the external characteristic plane* ($M\ vs\ \gamma$).

As it can be concluded, the error is minimized for step-up mode. The rated power of the (step-up mode and rated current) is the point in which the power converter should be specified, and simplifying assumption can be used! If, on the other hand the desired static gain specification is unitary, the designer should consider the exact solution or fitting to avoid important errors.

2.1.2.2 Minimized normalized DM first harmonic amplitude methodology

As previously mentioned, different purpose methodologies to design the DAB have been presented in the literature based on ZVS performance, reactive minimization and efficiency. In this section, it is proposed a design, that is choice of γ, based on the minimum value of $\bar{H}_{1_{in}}$, expressed mathematically in (2.15). To better visualize or find numerically

such condition, it is suggested the plotting in 2D for different static gains, as presented in *Figure 2.9*.

$$\gamma_o = root\left(\frac{d\left(\bar{H}_{DM}(M_{o,f},\gamma,1)\right)}{d\gamma} = 0\right) \tag{2.15}$$

The DM noise should account for its worst case, which can be either step-up or step-down modes. As it can be seen, the step-down mode is therefore considered the worst case in a lossless system. For a design specification $M_o = 0.8$, the value of γ_o is equal to approximately 0.12, which is translated to a phase-shift in degree equal to 25°.

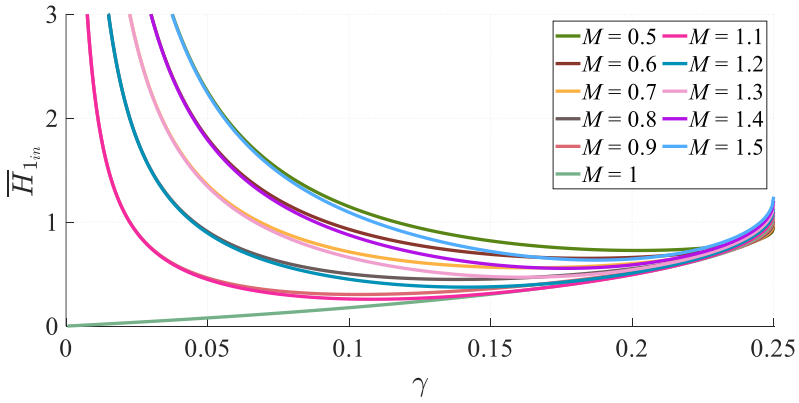


Figure 2.9 Normalized *first harmonic magnitudes with respect to γ for different static gains M.*

It is important to analyze maximum and minimum output currents, mainly considering the desired overload specification. Once a design is chosen and fixed, the variable γ can be expressed as a function of the percentage of output current $I_{o\%}$, as presented (2.16). Then, a parameter is defined as in (2.17) to analyze output current level impact on the first harmonic.

$$\gamma = \frac{2f_s L_{ac} I_o}{V_i}\, I_{o\%} \tag{2.16}$$

$$\bar{\bar{H}}_{1_{in}} = \bar{H}_{DM}(M, \gamma \times I_{o\%}, 1)\, I_{o\%} \tag{2.17}$$

Considering $M = 0.8$, and different values of γ, it is presented in *Figure 2.10* the plotting ($\bar{\bar{H}}_{1_{in}}$ vs $I_{o\%}$) varying $I_{o\%}$ from 0 to 2. It is interesting to notice that, indeed, the value $\gamma = 0.12$ is the minimum for $I_{o\%}$ varying from 0 to approximately 1. On the other hand, the

overload specification increases approximately 3 times higher for the double of the desired current. When considering $\gamma = 0.1$ there is a slight increase of the magnitude for the lower output current, on the other hand, the first harmonic level is increased by the double at $I_{o\%} = 2$. By further reducing the value $\gamma = 0.08$, the there is an increase of the harmonic level for the lower output current, and a reduction when increasing the output current value. Notice that the values $\gamma \leq 0.06$ does not bring any improvement in terms of harmonic distortion. It is, therefore, possible to conclude that the domain of the design space for the minimization of first harmonic distortion is $0.06 \leq \gamma \leq 0.12$ for $M = 0.8$.

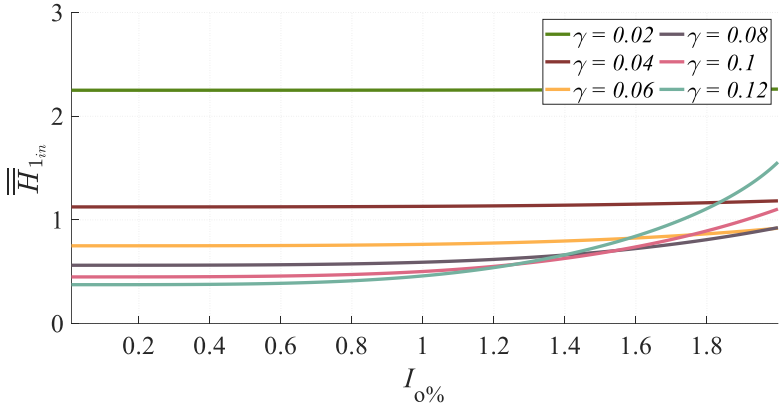


Figure 2.10 *Plotting results* $\left(\overline{\overline{H}}_{1_{in}} \; vs \; I_{o\%}\right)$ *for different values of* γ *considering* $M = 0.8$.

2.1.2.3 Discussion

As it can be concluded, through comprehensive mathematic analysis, it is possible to find, objectively, the design, or at least, the domain of the design space represented by output parametrized current γ as a function of the desired M. For the example presented in this Section, the minimization of the first harmonic distortion is objectively tackled, considering even overload condition. A simple strategy to keep same performance, that is, keeping the design choice γ unaltered for the overload condition, is to decrease the switching frequency at the same rate of the output current. Another interesting fact to notice is that, the saturated model behavior of the AC-link inductor is beneficial for the overload condition, as it tends to reduce AC-link inductance, while RMS current is increased.

It is also interesting to propose simple strategies for the change in input voltage, also desired. The goal is to keep the design choice of γ unaltered to keep equivalent performance:

- If the input voltage is increased, the value of γ is naturally decreasing. This can be done by varying the switching frequency, accordingly, e.g. as input voltage increases, the switching frequency should increase at the same rate;

- Another simple strategy is to vary the output current accordingly, e.g. as input voltage increases, the rated output current should increase at the same rate;

Notice that the conclusions and decision taking can easily be drawn out of the external characteristic plane (M vs γ), which is not the case for the conventional (M vs d) plane.

2.1.3 Drain-to-Source voltage waveform and ZVS realization

As discussed in *Chapter 1*, the ZVS realization is not only important for improving efficiency, but it is a key issue regarding EMI aspects. A necessary condition, but not sufficient, is that at switching time, the current value of the switch should be negative in order to benefit from natural parallel free-wheel diode in MOSFETs to conduct before the switch is trigged by Gate-to-Source channel. When the body diode conducts, the voltage V_{DS} across MOSFET is zeroed. Therefore, the MOSFET will be switched at zero voltage condition. Such ZVS boundary condition has been presented in (2.6).

On the other hand, the ZVS realization depends also on the energy between the resonant tank formed by the AC-link inductance, the input and output voltages and the capacitances C_{DS}, as it has been demonstrated efficiently through the state-space plane in [14]. Therefore, such capacitance is added on the equivalent circuit modeled in this section, improving the precision provided in *Figure 2.1*. Notice that the lossless model is still partially assumed as long as ZVS realization is performed.

2.1.3.1 Energy boundary condition

The principle can be easily explained and solved in terms of energy. Basically the energy stored at C_{DS} must be zeroed by the energy stored at the AC-link inductance. Therefore, the well known condition $LI_c{}^2 \geq C_{DS}V_{DS}{}^2$, in which I_c is the current at the switching instant, should also be satisfied for achieving ZVS realization across the H-bridges. The challenge lies in the non-linearity of C_{oss}, which can be improved by an energy-equivalent or charge-equivalent capacitances [14] [15], as presented in (2.18). Considering the aforementioned equivalent capacitance and the current at the switching instant for the H-bridges in the DAB, it is derived (2.19).

$$C_{eq} = \frac{2}{V_{i,o}{}^2} \int_0^{V_{i,o}} C_{oss}(V_{DS}) \times V_{DS} dV_{DS} \tag{2.18}$$

$$ZVS\ \ condition \rightarrow \begin{cases} \frac{1}{2}LI_a{}^2 \geq \frac{1}{2}C_{eq}V_{DS}{}^2 \text{ and } I_a < 0 \ \ for\ input\ H-bridge \\ \frac{1}{2}LI_b{}^2 \geq \frac{1}{2}C_{eq}V_{DS}{}^2 \text{ and } I_b < 0 \ \ for\ output\ H-bridge \end{cases} \quad (2.19)$$

Searching for comprehensive insights and dimensionless results in the same external characteristic plane *(*M vs γ*)*. , the boundary condition of energy is expressed without loss of generality in (2.20), as a function of a new parameter, σ in (2.21), in order to take into account C_{DS}. The plotting results of (2.20) are presented *Figure 2.11* for different values of σ. The region between the ideal and more realistic boundaries can be interpret as incomplete ZVS realization.

$$ZVS\ condition \rightarrow \begin{cases} M \leq \dfrac{1-4\sqrt{\gamma/\sigma}}{\sqrt{1-4\gamma}}, & for\ input\ H-bridge \\ M \geq \dfrac{\sqrt{1-4\gamma}}{1-4\sqrt{\gamma/\sigma}}, & for\ output\ H-bridge \end{cases} \quad (2.20)$$

$$\sigma = \frac{I_o}{2f_s C_{eq} V_i} \quad (2.21)$$

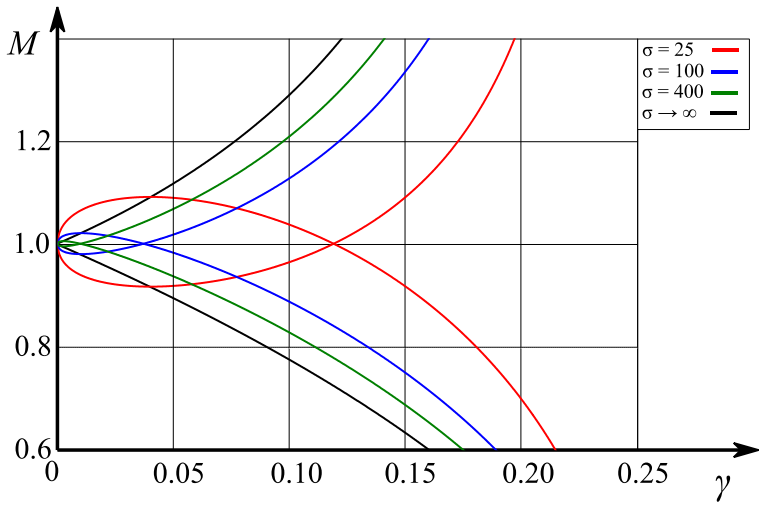


Figure 2.11 *ZVS performance for different values of* σ *in the in the external characteristic plane* (M *vs* γ).

Therefore, the variable σ can be seen as a FOM when choosing the switching frequency of the converter. The result of the plotting presents that σ should be as large as possible, meaning lowering frequency is advantageous for ZVS realization.

Considering that the ZVS realization performance observed for $\sigma \geq 100$ and that step-up mode, e.g. $M_f = 1.2$ is desired to perform ZVS at rated current, it is possible to conclude that $\gamma \geq 0.1$. It is therefore, possible to define the switching frequency domain in the design space as given in this example by (2.21):

$$\frac{V_i}{20 L_{ac} I_o} \leq f_s \leq \frac{I_o}{200 C_{eq} V_i} \tag{2.22}$$

Notice that, for the aforementioned example, the ZVS is accomplished for input H-bridge at its worst case (step-up $M_f = 1.2$), whereas for Output H-bridge it is not accomplished at its worst case (step-up $M_o = 0.8$). Due to tolerance, it is recommended to operate far from the boundary conditions.

2.1.3.2 Normalized Drain-to-Source voltage waveform

Analysis based on energy equation are always valid. However, one loses information about the switching event during the dead time itself e.g., how much should the dead time be or how much is the $d(V_{DS})/dt$, which is important for CM modelling since they are the main exciting source of noises. The expressions of the normalized waveform across V_{DS} during the fall time switching instant, assuming sufficient dead-time is presented in (2.23), in which a qualitative example *at* $\sigma = 400$ and $f_s = 250\ kHz$ is plotted against the time and presented in *Figure 2.12*.

$$\bar{V}_{DS} = \frac{V_{DS}}{V_i} = \begin{cases} \frac{1}{2}\left(1 - \begin{pmatrix} -\bar{I}_a\sqrt{\gamma\sigma}\sin\left(2f_s\sqrt{\sigma/\gamma}\,t\right) + \\ (M-1)\cos\left(2f_s\sqrt{\sigma/\gamma}\,t\right) - M \end{pmatrix}\right), & for\ input\ H-bridge \\ \frac{1}{2}\left(M - \begin{pmatrix} -\bar{I}_b\sqrt{\gamma\sigma}\sin\left(2f_s\sqrt{\sigma/\gamma}\,t\right) + \\ (1-M)\cos\left(2f_s\sqrt{\sigma/\gamma}\,t\right) - 1 \end{pmatrix}\right), & for\ output\ H-bridge \end{cases} \tag{2.23}$$

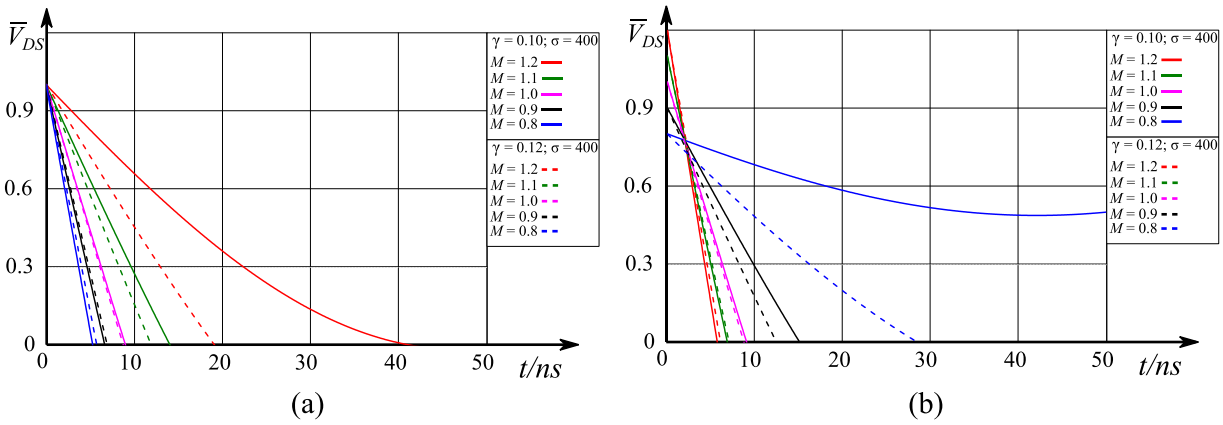


Figure 2.12 Qualitative example of a normalized waveform $\bar{V}_{DS}$ during the fall time switching instant at $\sigma = 400$ *and* $f_s = 250\ kHz$, *for* $\gamma = 0.1$ *(continuous lines) and* $\gamma = 0.12$ *(dashed lines) at different static gains: (a) across input H-bridge; (b) across output H-bridge.*

A dual behavior with respect to the static gain is observed. Notice that, a small increase of γ, up to 0.12 besides allowing ZVS fully accomplished on both H-bridges, tends to present a fall-time more similar to each other and less dependent on the static gain. Such fact can be beneficial since the idle time between the dead times and fall-time is minimized.

The root solution of the derivative of (2.23) defines the maximum dead-time t_{dt} (19) that will guarantee that $\bar{V}_{DS}$ will not regenerate due to resonance (as observed in *Figure 2.12* (b), being independent applied voltages or current at the switching instant. The $\bar{V}_{DS}$ fall-time of input and output MOSFETs can be calculated according (2.25), in which the example with $\sigma = 400$ and $f_s = 250\ kHz$ is plotted against γ for both input and output H-bridges in *Figure 2.13*.

$$t_{dt} \leq \frac{\pi}{4f_s}\sqrt{\frac{\gamma}{\sigma}} \tag{2.24}$$

$$t_{H\,in,out} = \begin{cases} \dfrac{\arcsin\left(\dfrac{1+M}{-\bar{I}_a\sqrt{\gamma\sigma}}\right)}{2f_s\sqrt{\dfrac{\sigma}{\gamma}}}, & for\ input\ H-bridge \\ \dfrac{\arcsin\left(\dfrac{1+M}{-\bar{I}_b\sqrt{\gamma\sigma}}\right)}{2f_s\sqrt{\dfrac{\sigma}{\gamma}}}, & for\ output\ H-bridge \end{cases} \tag{2.25}$$

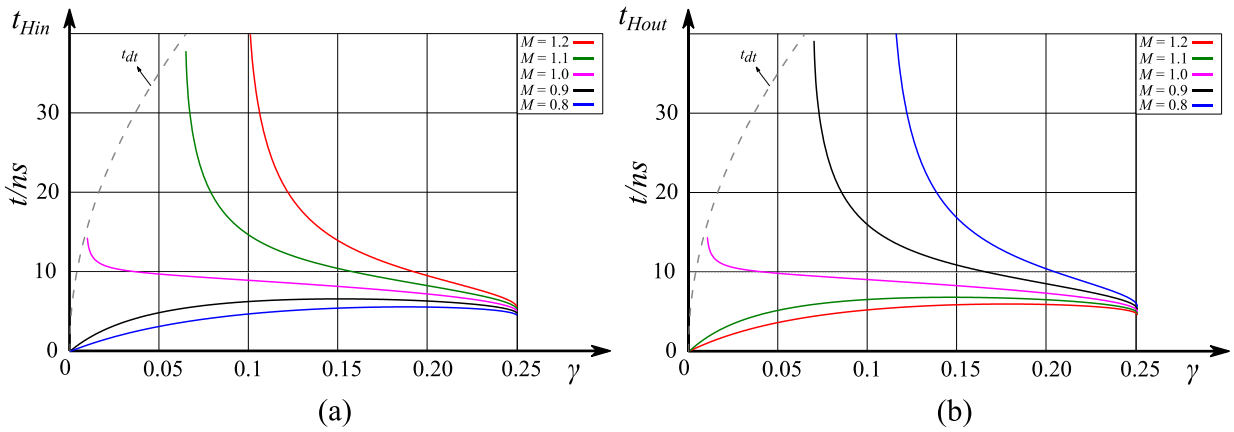


Figure 2.13 The fall-time for σ = 400 and fs = 250 kHz for different static gains: (a) input H-bridge and (b) output H-bridge.

2.2 Resistive model of the DAB

The inclusion of a resistance in the model allows the analysis of conduction joule losses, and, therefore, optimization in terms of minimizing losses and better accuracy of phase-shift for a given operating point, including the current at the switching instants, important for ZVS operation. Besides, it avoids absurd operating points such as infinity gain, and singular point such as zero division. Indeed its inclusion is a necessary condition for ISOP and IPOS connections of DAB converters, as it will be presented in *Chapter 4*. The assumptions before mentioned in Section 2.1 will be kept, except, of course, the inclusion of a resistance.

The impact of the resistance on ZVS performance has been addressed analytically in through an AC coupling admittance Y in [16]. For the same reasons aforementioned in a lossless model, it is desired to have an analytical closed-form solution relating the output current to the static gain. Since it is simple to derive piecewise solution from a first order RL system, it still worth it preferring a piecewise solution. In [5], analytical solutions are derived from piecewise equations, but such equations are not easy to visualize and only simulation results are provided while losses are neither discussed. Usually, in the literature, to the best author's knowledge, the conduction – and other – losses are treated numerically or analytically but not in a closed-form, which can certainly bring errors while important inaccuracies regarding phase-shift vs operating point can happen, as it will be further discussed theoretically and experimentally.

In this work, a closed-form solution is provided as a function three dimensionless parameters M , γ as already explained previously and quality factor, Q, a parameter presented

in (2.26) in the equations of the DAB. The analysis remains without dimension, and, therefore, more insightful and comprehensive. As it can be seen, calculating the value of Q with accuracy can be a difficult task and it depends on the technology employed. For our case, the value of the AC link Inductance (Coil Craft Inductor(s) + Transformer) depends less on the frequency. However, depending on its value and reference, a saturated model should be considered for accuracy. Noting that all devices and instrumentation have their own drift in precision, it is not searched for accuracy here, but rather reasonable values that can be obtained quickly in order to get analytical, fast and comprehensive results.

Measuring the equivalent inductance and resistance using an impedance analyzer of the AC-link of the CSC 2.0, it is possible to plot the parameter Q as presented in *Figure 2.14* as a function of the switching frequency. In general, it can be concluded that for the specific technology the value of Q can vary from 4 to 6.

$$Q\left(f_s, L_{ac}(I_{rms}, f_s), R_{ac}(f_s)\right) = \frac{2\pi f_s L_{ac}(I_{rms}, f_s)}{R_{ac}(f_s)} \cong \frac{2\pi f_s L_{ac}}{R_{ac}(f_s)} \tag{2.26}$$

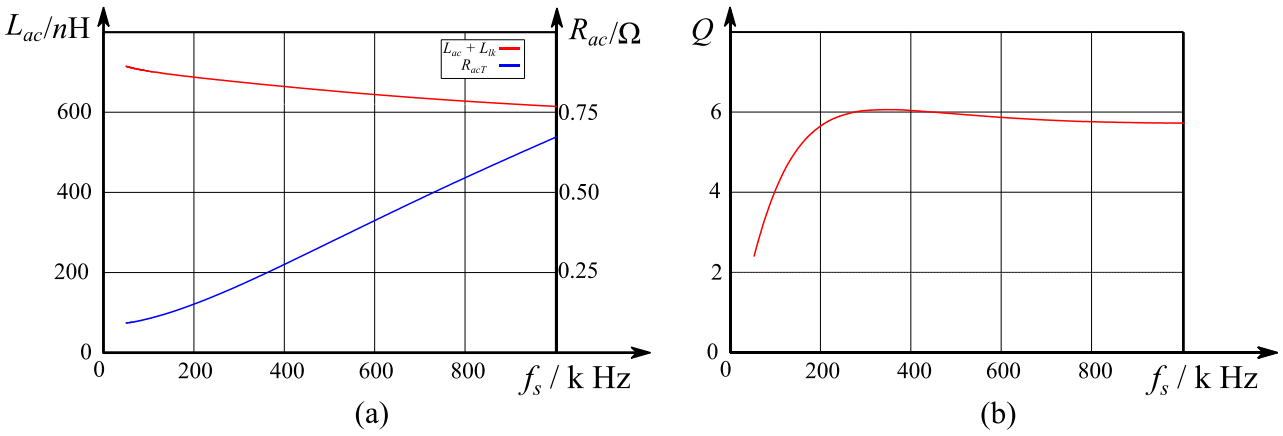


Figure 2.14 *Plotting results of the AC-link of CSC 2.0: (a) inductance and resistance measured through impedance analyser; (b) Quality factor (Q) according to (2.26).*

The impact on the input wave of the resistive model through Q, is qualitatively exemplified in *Figure 2.15*. It is presented the waveform reproduction of the parametrized the Input current for lossless (in blue) and resistive models $Q = 4$ (in red) for the same operating point $M = 1$ and $\gamma = 0.1$, meaning same output power.

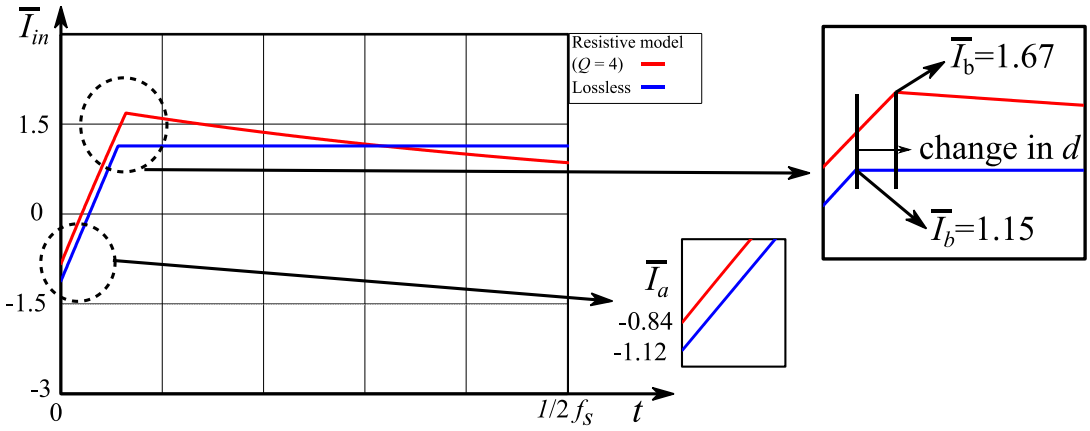


Figure 2.15 *A qualitative example portraying the waveforms of a normalized input current for* $M = 1$ *and* $\gamma = 0.1$ *in a lossless (blue curve) and a resistive model represented by* $Q = 4$.

Notice that in the example given, the resistive model requires a larger phase-shift, as expected to compensate the losses. It is possible to notice that current at the switching instants, important for ZVS operation is also altered. The resistive model is, therefore, presented and compared to the lossless model, and its main importance is highlighted through this section.

2.2.1 Static gain characteristic

The closed-loop solution of the static gain, as presented in (2.27), allowed the analysis to be kept in the same output plane, by including the parameter quality factor Q. The relationship γ vs d for lossless model is quadratic, as presented in (2.2), and does not depend on M. To investigate such a relationship in the resistive model, (2.27) is rearranged to be plotted *Figure 2.16* against d for different static gains (0.8, 1 and 1.2) and $Q = 5$.

$$M = \frac{1 - 2d + \frac{2Q}{\pi}\left(1 - \operatorname{sech}\left(\frac{\pi}{2Q}\right)e^{\frac{\pi}{2Q}(1-2d)}\right) - \frac{\pi}{Q}\gamma}{1 - \frac{2Q}{\pi}\tanh\left(\frac{\pi}{2Q}\right)} \tag{2.27}$$

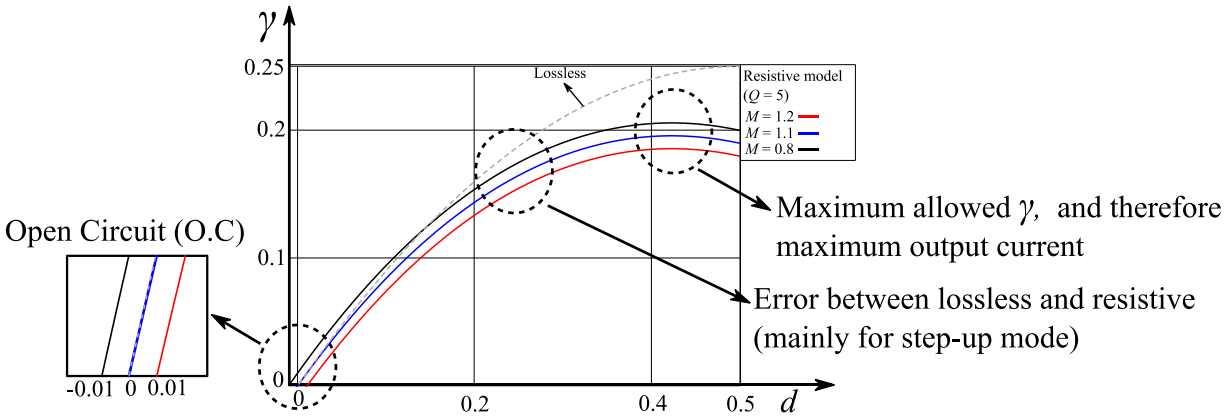


Figure 2.16 Curve γ *vs* d *for different static gains at* $Q = 5$.

Four conclusions to be highlighted: i) the behaviour is still kept quadratic; ii) the limit of maximum γ and d are equal or less than 0.25 and 0.5, respectively, meaning that overload current becomes also limited (this can be found interactively as portrayed, or, analytically); iii) the difference between lossless and resistive models are quite significant mainly for larger phase-shift and step-up; and, finally iv) the existence of no load (Open Circuit) operating points are theoretically proved even for step-up and step-down modes, which can be interesting for characterizing and predicting the EMI signature of the converter more easily.

2.2.2 Conductive joule losses and normalized RMS current value

Another main advantage of the resistive model is to be able to calculate the efficiency (η) of system. As there are other losses in the converter, it is preferable to present the conductive joule losses ($1 - \eta$) as in (2.28). Notice that it does not depend on the output current, but only on static gain, phase-shift and the quality factor. As previously, it is preferable to use the external characteristic plane *(*M vs γ), which can be done by imposing, numerically, (2.27) in (2.28), from which plotting results for $Q = 5$ is presented in *Figure 2.17*. The normalized RMS current is derived from η in (2.28), and it is presented in (2.29), with plotting results presented in *Figure 2.18*. Similarly, the normalized AC circulating current is derived for the resistive model in (2.30), and plotting results are presented in *Figure 2.19*.

$$1-\eta = 1 - M\,\frac{1-2d+\frac{2Q}{\pi}\left(1-\operatorname{sech}\left(\frac{\pi}{2Q}\right)e^{\frac{\pi}{2Q}(1-2d)}\right)+M\left(\frac{2Q}{\pi}\tanh\left(\frac{\pi}{2Q}\right)-1\right)}{1+M\left(2d+\frac{2Q}{\pi}\left(1-\operatorname{sech}\left(\frac{\pi}{2Q}\right)e^{-\frac{\pi}{2Q}(1-2d)}\right)-\frac{2Q}{\pi}\tanh\left(\frac{\pi}{2Q}\right)\right)} \qquad (2.28)$$

$$\bar{I}_{RMS} = \frac{I_{RMS}}{I_o} = \sqrt{\frac{M\left(\frac{1-\eta}{\eta}\right)\frac{Q}{\pi}}{\gamma}} \tag{2.29}$$

$$\bar{I}_{ac_{RMS}}(M,\gamma) = \frac{\bar{I}_{ac_{RMS}}(M,\gamma)}{I_o} = \sqrt{\frac{M\left(\frac{1-\eta}{\eta}\right)\frac{Q}{\pi}}{\gamma} - \left(\frac{M}{\eta}\right)^2} \tag{2.30}$$

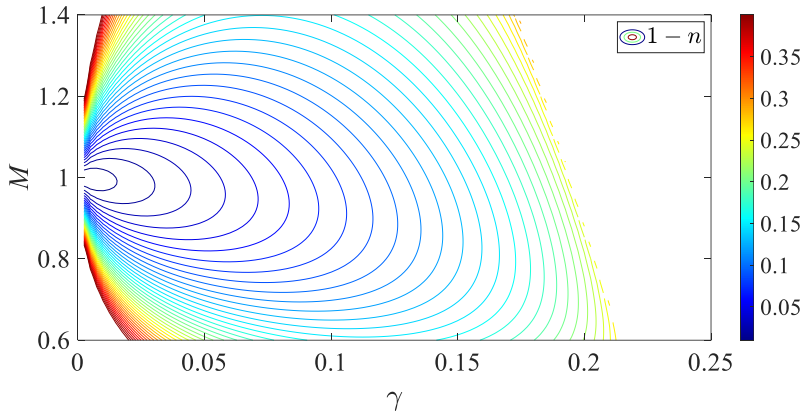


Figure 2.17 3D *mapping of conductive joule losses in the external characteristic plane* $(M\ vs\ \gamma)$ *for* $Q = 5$.

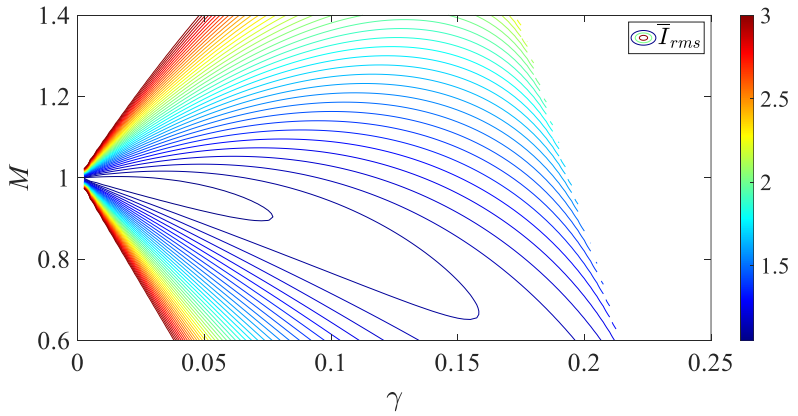


Figure 2.18 3D *mapping of normalized RMS current for* $Q = 5$ *in the external characteristic plane* $(M\ vs\ \gamma)$.

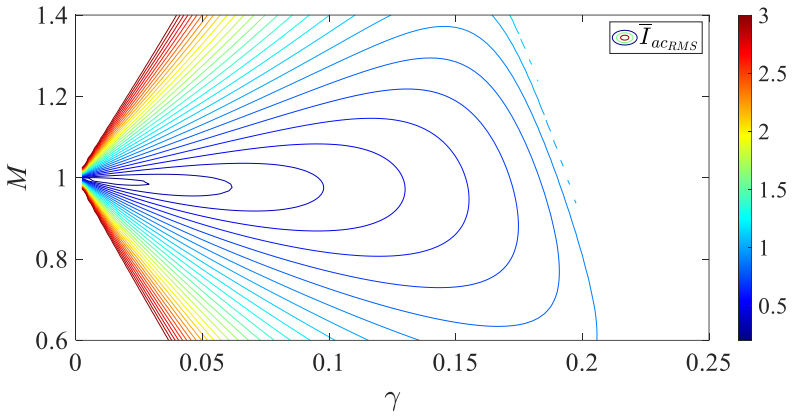


Figure 2.19 3D *mapping of normalized AC RMS circulating current for* $Q = 5$ *in the external characteristic plane* (M *vs* γ).

As previously presented in the lossless model, the designer can choose which function it is desired to optimise. The first harmonic magnitude was not derived for the resistive model, but it can be approximated by analysing the behaviour of the RMS and the first harmonic magnitude lossless model and assume same behaviour for the resistive model.

2.2.3 Drain-to-Source voltage waveform and ZVS realization

As observed in *Figure 2.15* , the inclusion of the resistance changes the behaviour of the operating point. It is interesting, therefore, to study its effect on ZVS performance. The equivalent circuit is still considered a resonant tank as previously, with the modification of $\bar{I}_a$ and $\bar{I}_b$, taking into account the resistance in the model. Such approximation is valid as long as the circuit is highly oscillatory. For a qualitative example, continuing with the conclusion of σ = 400 and numerically imposing the phase-shift from (2.27) , it is possible to observe the effect on the ZVS condition (2.31) for different Q and the lossless case, as presented in *Figure 2.20*.

ZVS condition

$$\rightarrow \begin{cases} M \leq \dfrac{\dfrac{2}{1+e^{-\frac{\pi}{Q}}} - \left(1 + 2\dfrac{\pi}{Q}\sqrt{\gamma/\sigma}\right)}{1 - \dfrac{2e^{-\frac{\pi}{Q}(1-d)}}{1+e^{-\frac{\pi}{Q}}}}, & for\ input\ H-bridge \\ M \geq \dfrac{1 - \dfrac{2e^{-\frac{\pi d}{Q}}}{1+e^{-\frac{\pi}{Q}}}}{\left(1 + 2\dfrac{\pi}{Q}\sqrt{\gamma/\sigma}\right) - \dfrac{2}{1+e^{-\frac{\pi}{Q}}}}, & for\ output\ H-bridge \end{cases} \quad (2.31)$$

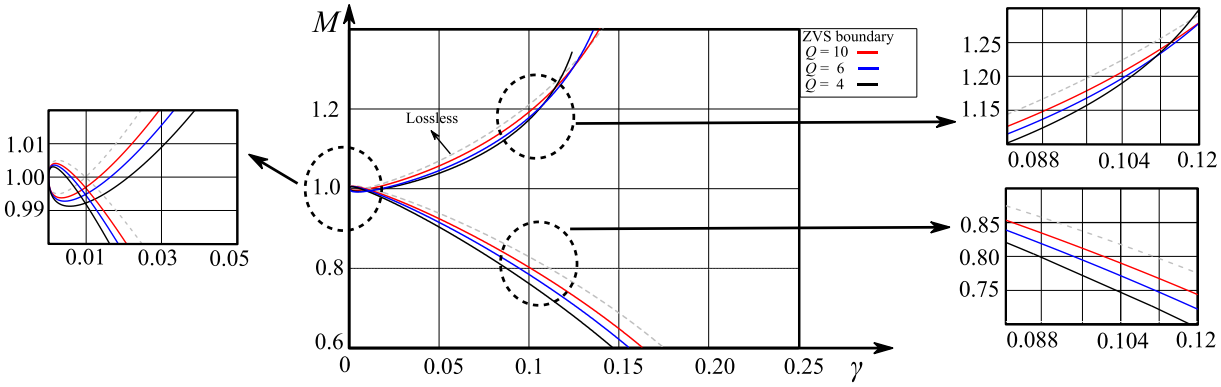


Figure 2.20 Effect of resistive model in the ZVS performance for Q = 10 (red); Q = 6 (blue); Q = 4 (black) and $Q \rightarrow \infty$ *(dashed line).*

As it can be concluded, the increasing of Q worsens ZVS region for input H-bridge, in such a way that step-up mode has a tendency to lose its ZVS. On the other hand, ZVS for output H-bridge and step-down mode are improved.

Finally, the effect of Q = 6 in the drain-to-source during fall-time instant is presented in *Figure 2.21*. Notice that the results show the input H-bridge won't perform ZVS for M = 1.2 and will perform ZVS for output H-bridge for M = 0.8. Again, to assure ZVS on both H-bridges, increasing γ slightly (e.g γ = 0.12) is a solution, while keeping σ = 400. Indeed, it is interesting to notice that Q affects more drastically the zones in the boundary conditions. Outside of the boundary, the lossless model can be used due to its simplicity. As a guidance, it is suggested to design a bit further away from such boundary.

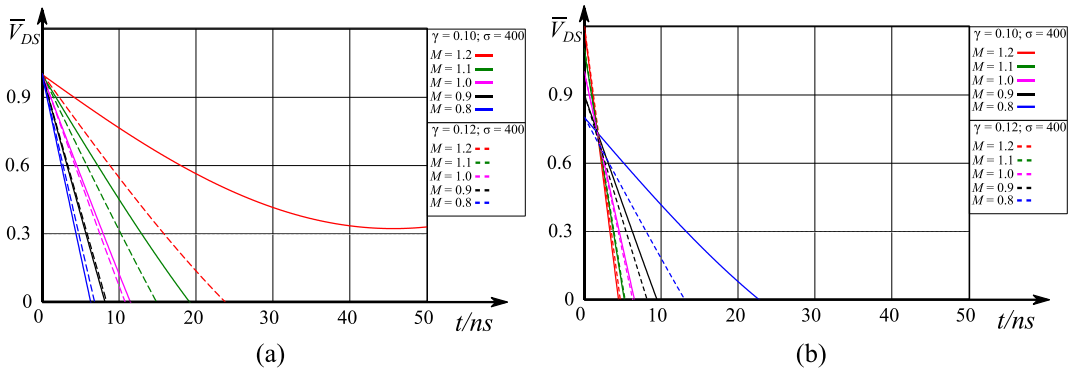


Figure 2.21 Qualitative example of *a normalized waveform* $\bar{V}_{DS}$ *considering* $Q = 6$ *during the fall time switching instant at* $\sigma = 400$ *and* $f_s = 250\ kHz$, *for* $\gamma = 0.1$ *(continuous lines) and* $\gamma = 0.12$ *(dashed lines) at different static gains: (a) across input H-bridge; (b) across output H-bridge.*

2.3 Prediction of important DM noise and drain-to-source parameters in the plane $M\ vs\ I_{o\%}$

As it can be concluded from previous sections, the analysis of EMI in terms of power is not suitable to describe the EMI signature accurately, as important parameters are not depending linearly with power, such as harmonics and ZVS realization. Once the parameters σ, γ and Q are fixed, it is interesting to observe in another plane (M vs $I_{o\%}$) (see *Figure* 2.22), as previously demonstrated in (2.17) the effect of partial load, including open circuit (OC) and overload.

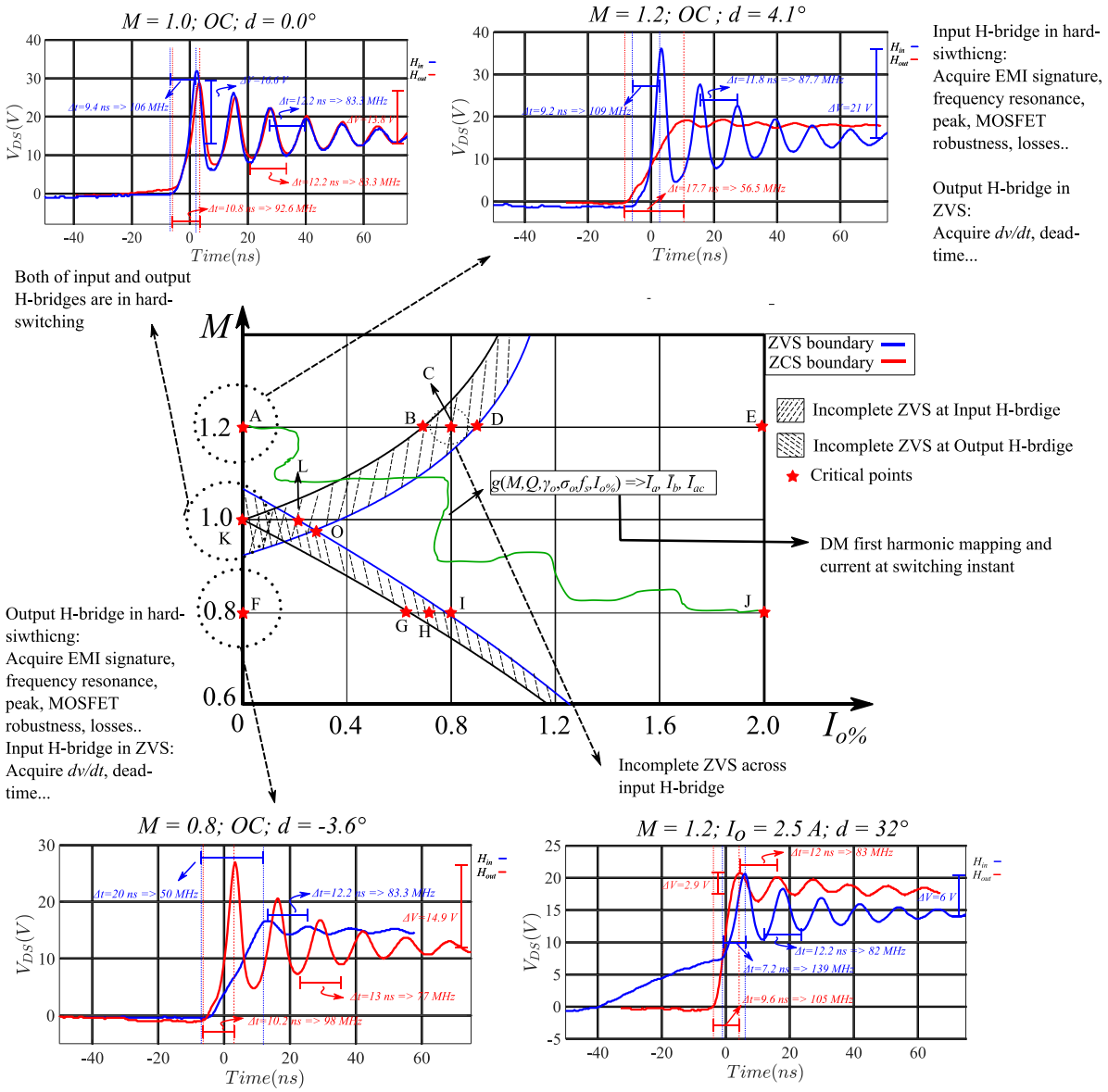


Figure 2.22 Analysis of important parameters impacting EMI signature, such as ZVS and ZCS boundary, AC circulating current and current at switching instant tackling critical and important points in the plane (M *vs* $I_{o\%}$) for Q = 5, σ = 400 and γ = 0.12. *Experimental drain-to-source voltage measurement for different OC conditions also provided.*

Some critical points, regarding ZVS realization is then first observed. Let TR be defined as the operating point trajectory, or segment of the operating point in the following discussion:

- Step-up mode: for A ≤ TR ≤ B, the DAB loses entirely its ZVS at Input H-Bridge. Notice that at point B, a ZCS condition is observed, which can be beneficial in terms of EMI noise; ZVS is performed at Output H-bridge;
- Step-up mode: for B ≤ TR ≤ D, incomplete ZVS realization. At point D, ZVS is entirely achieved with a *dv/dt* very softly; ZVS is performed at Output H-bridge;

- Step-up mode: for D ≤ TR ≤ E, the DAB realize ZVS for both Input and Output H-bridges. Notice however that due to higher current at switching instant, the *dv/dt* will also increase;
- Unitary mode: for K≤ TR ≤O the DAB does not realize ZVS 100% at both Input and Output H-bridges;
- Unitary mode: for O ≥ TR complete ZVS realization at both input and output H-bridge, with the tendency of increasing rise and fall times due to increasing in output current;
- Step-down mode: For F ≤ TR ≤ I a dual behavior with respect to the step-up mode is observed.

Even though only drain-to-source waveform performing ZVS is analyzed in this thesis, the DAB under SPS modulation is at some point subjected to hard switching or incomplete ZVS. It is, therefore, useful to calculate the current at the switching instants $\bar{\bar{I}}_a$ and $\bar{\bar{I}}_b$, defined in (2.32) and (2.33), respectively, since they are an image of both switching losses and high frequency oscillations. Besides, when in ZVS region, their values are used to calculate the fall time of the MOSFET when performing ZVS. In *Figure 2.23*, the plotting results of (2.32) and (2.33) are presented.

$$\bar{\bar{I}}_a(M, \gamma \times I_{o\%}) = \bar{I}_a(M, \gamma \times I_{o\%})\, I_{o\%} \tag{2.32}$$

$$\bar{\bar{I}}_b(M, \gamma \times I_{o\%}) = \bar{I}_b(M, \gamma \times I_{o\%})\, I_{o\%} \tag{2.33}$$

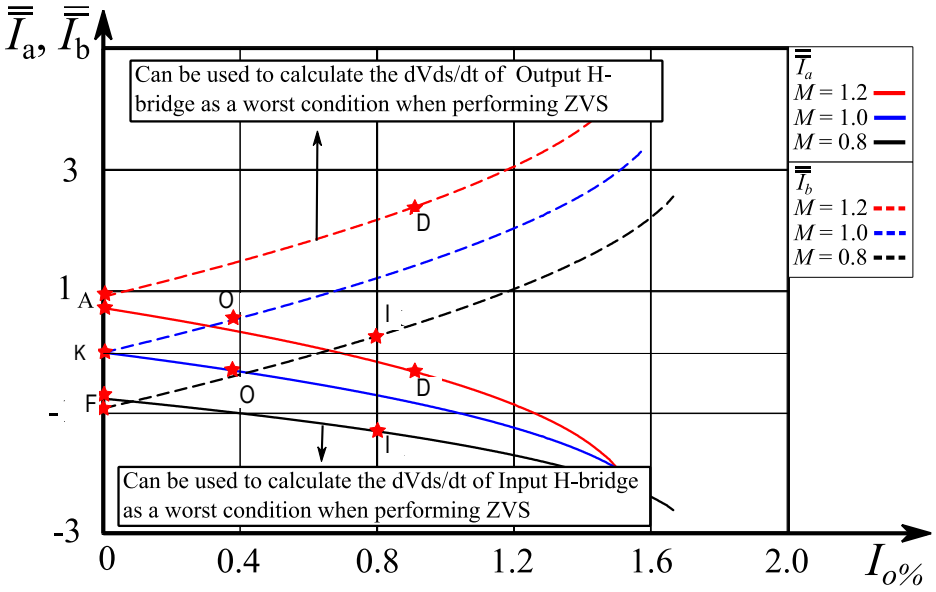


Figure 2.23 Normalized current at the switching instant of input H-bridge (continuous line) and output H-bridge (dashed line) for different static gains. Red stars point marks placed to define operating points of ZVS limit and OC according to Figure 2.22.

Similarly, the normalized input RMS and AC circulating RMS currents are presented in *Figure 2.24* and *Figure 2.25*, respectively.

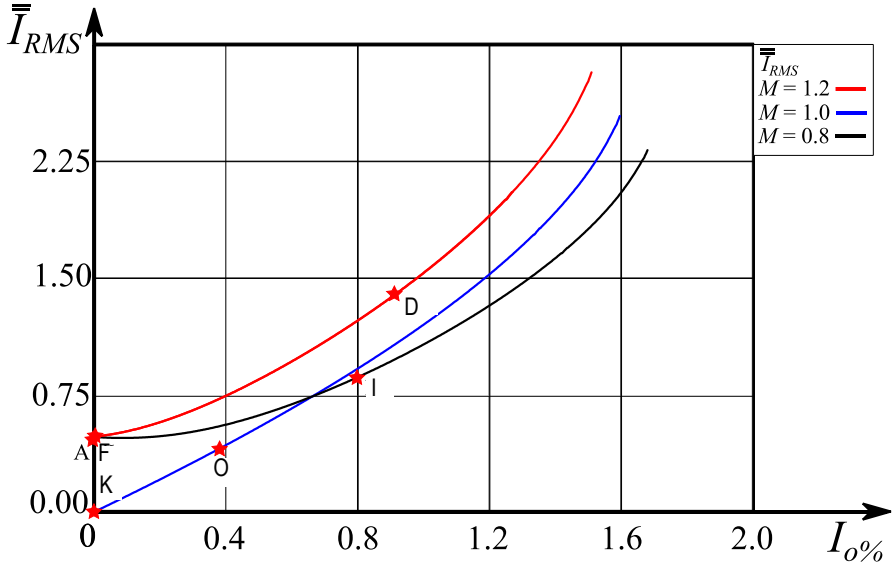


Figure 2.24 Normalized input RMS current for different static gains. Red stars point marks placed to define operating points of ZVS limit and OC according to Figure 2.22.

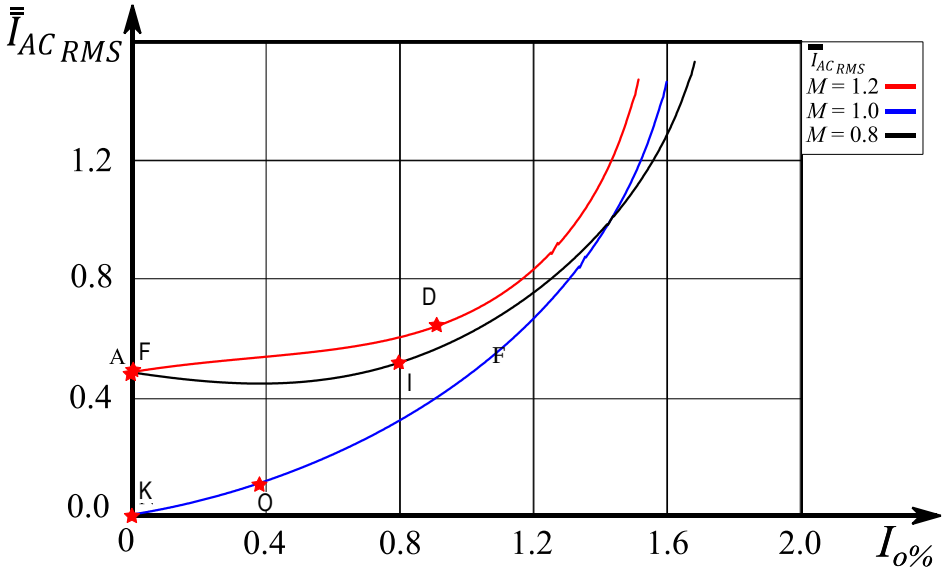


Figure 2.25 Normalized input AC circulating current for different static gains. Red stars point marks placed to define operating points of ZVS limit and OC according to Figure 2.22. Red stars point marks placed to define operating points of ZVS limit and OC according to Figure 2.22.

2.3.1 Discussion of Open Circuit (OC) for straightforward EMI characterization and prediction

As it can be seen in *Figure 2.22*, there are many points to be analyzed that will impact on the EMI signature, in which the worst case should be evaluated, or predicted. The goal of this section is to provide a methodology and proof of concept by testing in OC to easily predict the EMI signature.

A common way of simplifying setups focusing on reducing the need of current of power supply is connection the output to the input of the power converter. In such a way, the unitary mode can be tested at full load without major concerns. On the other hand, the unitary mode does not represent the worst case, as before discussed. It is required, therefore, to reach step-up and step-down modes

Besides, the no load condition implies that the modelling of the power converter is simplified, since cables and loads are not taken into consideration, which reduced the amount of variables and parasitic that can be time consuming to extract the main needed parameters in the high frequency domain. It is worth noting that such approach is appropriated for pre-compliance and testing in order to acquire, predict information as for the state of the power converter and take decisions for optimizing the power converter. This means that, upstream and downstream systems, such as filters, cables and loads will effect surely effect the EMI behaviour, but are not accounted at first place.

2.3.1.1 Step-up mode

Notice that in a step-up OC testing, the input H-bridge (continuous curve in red in *Figure 2.23*) is subjected to hard switching ($I_a > 0$) with the largest current possible. This brings the DAB into a stressful operating point in terms of switching, with common problems of high frequency oscillations and losses due of hard-switching well defined and accentuated. This can be used to well characterize and discriminate the problems due to switching, that will inevitably occur in a DAB SPS at partial load. Meanwhile, the output H-bridge is performing ZVS ($I_b > 0$) with a large current (approximately the same when in unitary mode at 80% load current), which will increase the dV_{ds}/dt, not advantageous for CM noise, as it will be better discussed in *Chapter 3*. It is interesting to use this simple OC testing during the first tests as a methodologic testing procedure, not only for EMI signature characterization, but also to test the robustness of the switching devices! Eventually, the static gain can be further increased to put the power converter into an even more stressful situation that could account better the EMI signature, increasing the hard-switching energy of input H-bridge and increasing the dV_{ds}/dt of output H-bridge up to rated power condition.

2.3.1.2 Unitary mode

In this mode, both H-bridges does not perform ZVS, with almost zero current at switching instants. This means that the energy associated to losses and stresses are not intensified. It is, on the other hand, an interesting point in which driving the DAB is very straightforward, and can be interesting to separate the CM and DM noise sources in a power converter. Notice in *Figure 2.25*, that the DM is theoretically zero and the resulting noise appearing across the EMI test receiver is most likely due to CM.

2.3.1.3 Step-down mode

This mode is dual to the step-up mode; the input H-bridge is performing ZVS, while output H-bridge is not performing ZVS. The dV_{ds}/dt of input H-bridge approaches the same as in unitary-mode rated output current. Eventually, the static gain can be further decreased to put the power converter into an even more stressful condition in terms of switching and and AC circulating current. As observed in *Figure 2.24* and *Figure 2.25*, the step-down and step-up modes have the same current at switching instant and AC circulating currents. Therefore, it is possible to conclude that difference in temperature of H-bridges between a step-up and step-down modes are most likely due to switching losses, which can a valuable information for the design of a power converter.

2.4 Evolution of the performance characteristic of the CSCs

Following the proposed methodology, two CSCs have been proposed and prototyped besides the *CSC 1.0*, in searching of improving the performance. Their parameters are presented in *Table 2-I*. The rate input and output voltage and current are set at 20 V and 2.5 A, respectively.

Table 2-I Design parameters evolution of the CSCs.

Designing parameter	CSC 1.0	CSC 2.0	CSC 3.0
γ	0.054	0.115	0.095
σ	469.5	469.5	1485

As it can be seen the difference from CSC 2.0 to CSC 1.0 is the increase of the parameter

γ by increasing the AC-link inductance, and keep the switching frequency at 250 kHz. As it has been operating around $\gamma = 0.1$ improve ZVS region while minimized the harmonic content for step-up condition. In the third version, (CSC 3.0) has its switching frequency reduced, which increases the parameter σ. The parameter γ is kept around 0.1 (a bit smaller due to availability), by increasing even further the AC-link inductance.

In *Figure 2.26*, the theoretical ZVS boundary and first DM harmonic of CSC 1.0 and CSC 2.0 are presented. It can be notice that indeed the ZVS performance of CSC 2.0 is improved, mainly for step-up and step-down modes.

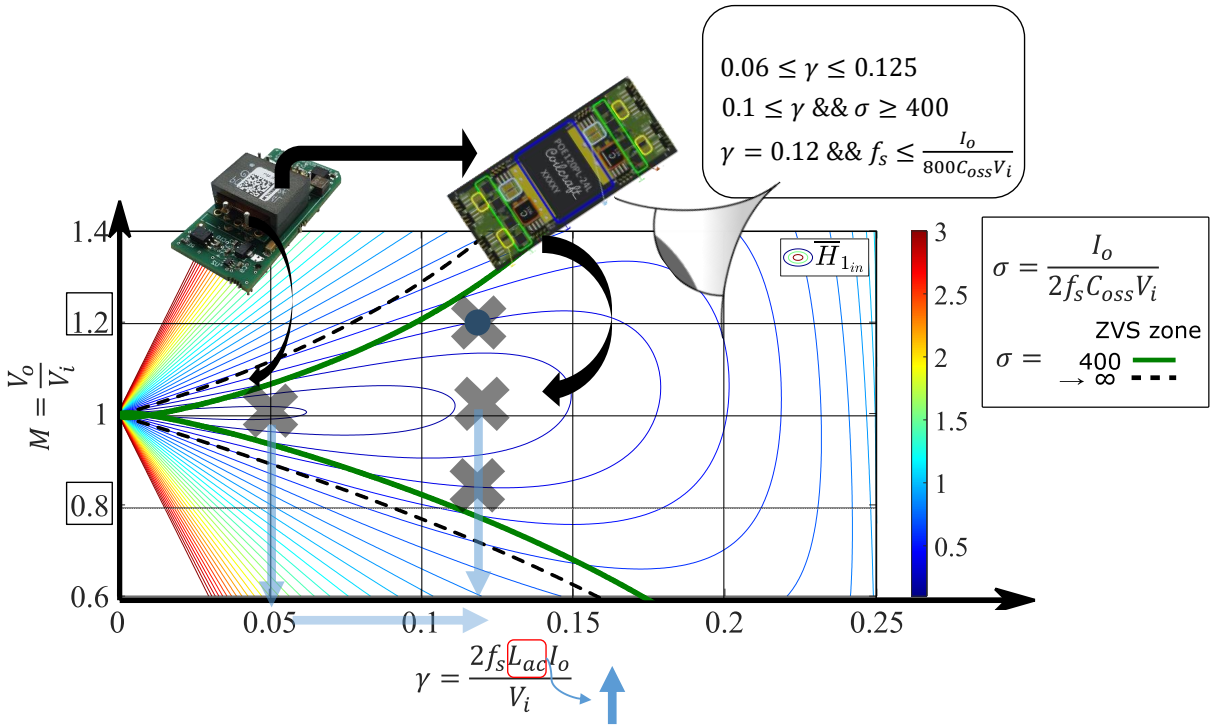


Figure 2.26 Theoretical (lossless) ZVS boundary and first harmonic of CSC 1.0 and CSC 2.0.

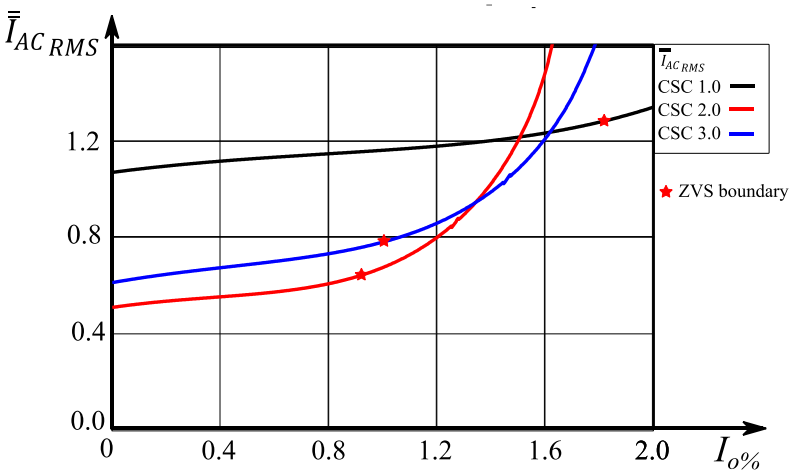


Figure 2.27 Normalized input AC circulating current for different static gains for different used and prototyped CSCs at G2Elab.

In *Figure 2.27*, it is presented the plotting results of the normalized AC circulating current among all three CSCs. It can be concluded that an improvement of the DM first harmonic is expected for the step-up and step down modes.

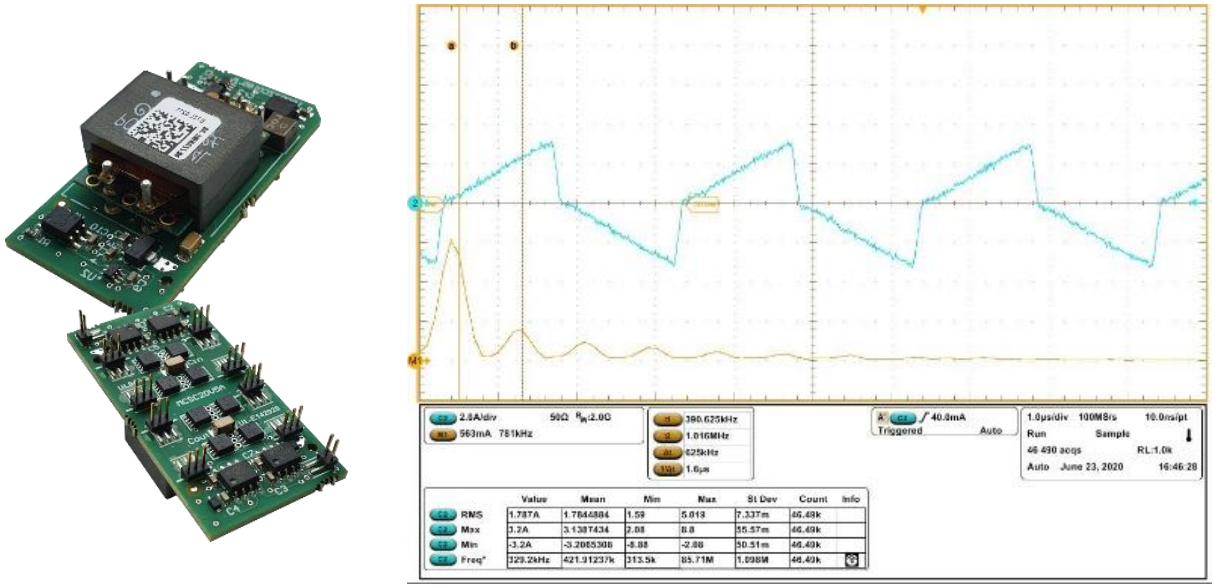
2.5 Experimental results

Experimental results were conducted firstly CSC 1.0 to validate in practice the theoretical results using resistive model versus lossless model in terms of accuracy of operating point and phase-shift. During the second experimental results, the CSC 2.0 has the ZVS and drain-to-source waveform study validated using the restive model. Finally, experimental data of DM noise is conducted to conclude over the OC testing for EMI signature prediction.

2.5.1 Static gain Characteristic ($d\ vs\ \gamma$)

The results comparing lossless model and practical results of a CSC 1.0 (see *Figure 2.28* (a)) are presented in [1]. It is now included the restive model considering Q = 6. Considering its AC link inductor of 700 nH, an output current of 3 A and 1.5 A and input voltage of 10 V, the switching frequency were calculated as 330 kHz, in such a way that the parameter γ_f is set at 0.14 and γ_o is at 0.07, while tests are conducted for M_f set at 1.2 and M_o = 0.8.

In *Figure 2.28 (b)*, it is presented the waveform of current measured in the AC link when I_o = 1.5 A and M_o = 0.8 in which ideally presents the same RMS value of the input current. The result of the tests are presented in *Table 2-II* and *Table 2-III* for the output current set at 3 A and 1.5 A, respectively.



(a) *(b)*

Figure 2.28 (a) CSC 1.0 used for practical results; (b) waveform of the current in the AC link inductor (light blue color) for I_o=1.5 A and M_o= 0.8 *[1]*.

Table 2-II Experimental and theoretical (lossless and resistive) results for I_o *= 1.5 A.*

	I_o *=1.5 &* M_o = 0.8					I_o = 1.5 A & M_f = 1.2				
	Pract.	Lossl.	Error (%)	Res.	Error (%)	Pract.	Lossl.	Error (%)	Res.	Error (%)
I_{in} (A)	1.4	1.2	13%	1.3	8.1%	2.15	1.8	16.3	1.9	11.6%
$I_{LAC_{RMS}}$ (A)	1.8	1.9	5.6%	1.7	1.6%	2.7	2.14	20.1	2.4	12.5%
α (Degree°)	10.4	13.5	30%	12.2	15.1%	20.7	13.4	35	16.1	28.1%
Efficiency (%)	85.8	-	-	94	9.3	84.7	-	-	92.9	8.8%

Table 2-III Experimental and theoretical (lossless and resistive) results for I_o *= 3.0 A.*

	I_o *=3.0 &* M_o = 0.8					I_o = 3.0 A & M_f = 1.2				
	Pract.	Lossl.	Error (%)	Res.	Error (%)	Pract.	Lossl.	Error	Res.	Error (%)
I_{in} (A)	2.9	2.4	17.5	2.6	10.7	4.4	3.6	25	3.9	11%
$I_{LAC_{RMS}}$ (A)	3.5	3.3	6.8	3.3	6.8	4.9	3.92	20.8	4.5	8.1%
α (Degree°)	33.6	29.8	11.2	30.3	10.8	41.4	29.8	27.9	36	14.9%
Efficiency (%)	83.1	-	-	90.2	8	81.1	-	-	88	7.7

The experimental results presented in *Table 2-II* and *Table 2-III* show the improvement of the model mainly for step-up mode as expected from theory presented in *Figure 2.16*. The error between the resistive model and practical results is not only due to

precision in measurement or saturation as previously mentioned, but also the resistive model does not contain other losses and a different equivalent circuit should be used.

On the other hand, the practical results can be used to tune an equivalent fitting Q capable to improve the accuracy of the model. As an example, the use of Q = 4 results in an error less or equal to 5.2 % for all parameters at load I_o = 3 A. For lower current, I_o = 1.5 A, the maximum error is kept below 7.1% for all measured results, except for phase-shift, error 15.2% at M_o = 1.2, I_o = 1.5 A. Indeed, as such operating points at lower output currents are outside the ZVS region, the accuracy of only resistive model is compromised.

2.5.2 ZVS and drain-to-source waveform

Now, considering prototyped CSC 2.0, two experimental results are presented and also compared to theoretical results. The goal of the first one is to show the validity of ZVS performance and drain-to-source waveform, while the second one presents results of the OC test for EMI prediction.

An experimental result regarding ZVS was performed for the DAB CSC 2.0. The input and output voltages were fixed around 30 V, while output current varied from 0 to 2.5 A The dead-time was set to 50 ns in order to observe the resonance effect. With an equivalent C_{oss} calculated through its equivalent charge as 585 pF, switching frequency at 250 kHz, the parameters are set γ = 0.04 (at I_o = 2.5 A), and σ = 285. In *Figure 2.29 (a)*, it is presented the theoretical (resistive Q = 4) and the practical results waveforms for various operating points. As it can be observed, the theoretical results provide considerable good accuracy as for the dV_{ds}/dt and ZVS realization discussed throughout this *Chapter*.

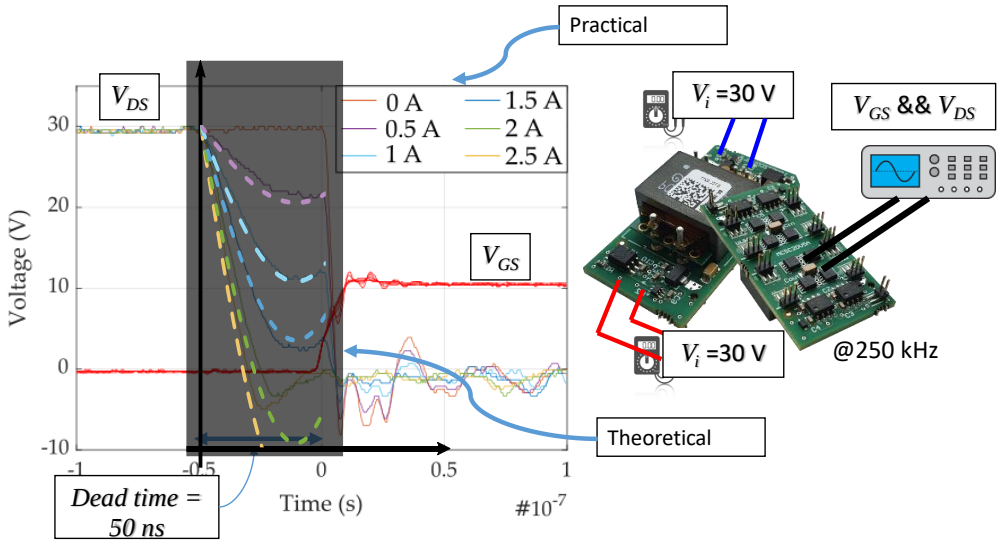


Figure 2.29 Drain-to-source waveform during fall time instant: Theoretical results using resistive model (dashed line) and practical results (continuous line).

2.5.3 DM noise analysis: from OC to rated value

Still considering the CSC 2.0, the setup consisted in measuring the DM noise by connection through an LISN (DUAL-LINE V-Y-DELTA FOR GCPC DC-LISN-M2-100) capable of separating CM (asymmetrical disturbances) from DM (symmetrical disturbances), as well as access to the unsymmetrical disturbances on phase "+" and "–" as required by regulation CISPR16. The EMI receiver is a spectrum analyzer (R&S®ESRP3) with a frequency ranging from 9 kHz up to 3.6 GHz.

In *Table 2-IV*, it is presented main the input and output electrical parameters in which tests we conducted presented. The first part of experimental results, consists on eighteen tests, conducted at fixed input voltage (V_i) equal to 15 V and varying static gain (M) from 0.8 to 1.2 and output current (I_o) from 0 to 2.5 A.

Table 2-IV Main electrical parameters for experimental results.

Symbol unity	Value
V_i (V)	15
V_i (V)	V_i × [0.8, 1, 1.2]
I_o (A)	[0, 0.5, 1, 1.5, 2.0, 2.5]
f_s (kHz)	250

2.5.3.1 Thermography inspection of OC

Infra-Red – pictures photo of the top side of one CSC (H_{in} and H_{out} standing for input and output H-bridge) operated in Open Circuit (OC) and rated power (M = 1.2 and I_o = 2.5 A) are depicted in *Figure 2.30*.

Notice that the thermal signature of the converter H-bridges is related to the conduction losses plus switching losses and stresses when ZVS is not complete. The observation of the thermal image helps in confirming the H-bridges operation mode (no ZVS, partial ZVS or full ZVS). Assuming same RMS circulating current in OC for step-up and step-down modes, the difference in temperature for the input and output H-bridges can be inferred as being mostly due to switching losses. At the unitary static gain and OC operating

point, as the AC circulating current is minimized, it can be inferred that the temperature profile is due mostly to "parallel" losses, including switching and magnetic losses, which are in general dependent and increasing with the increase in switching frequency and voltage levels.

The step-down mode will produce more switching stress at output H-bridge, whereas step-up mode will produce more switching stress at input H-bridge, and, finally, the unitary static gain condition at both OC and rated current results in equal temperature balance at both H-Bridges, resulting in similar switching stress on them.

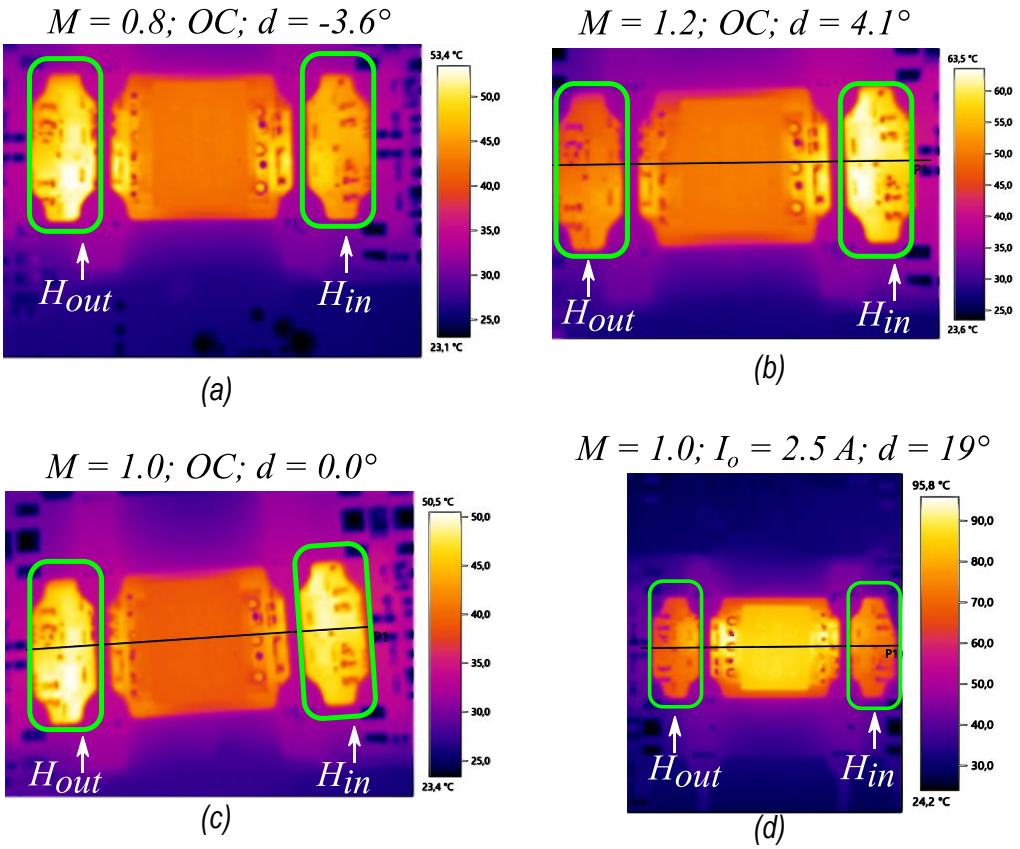


Figure 2.30 Experimental Temperature profile through IR photo of DAB CSC 2.0 under different load conditions:(a) M = 0.8 at OC; (b) M = 1.2 at OC; (c) M = 1 at OC; (d) and M = 1.0 at I_o = 2.5 A.

2.5.3.2 ZVS and drain-to-source waveform

Meanwhile, the drain-to-source voltage waveform on input and output H-bridges are collected through an oscilloscope and presented in *Figure 2.31* (rise time) and *Figure 2.32* (fall time). As can be seen, the DAB converter is capable of operating in OC for M varying any given static gain from 0.8 to 1.2, considering oscillating overvoltage due to non-ZVS, pre-confirming the robustness of switching devices and possible safe operation for rated values.

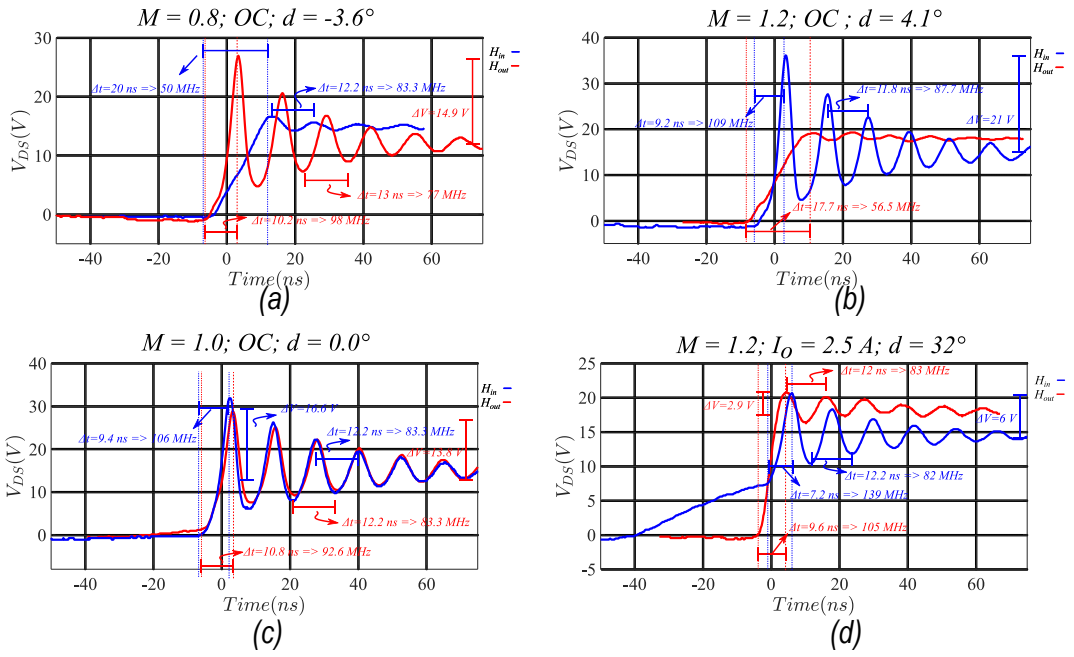


Figure 2.31 Experimental measurement of the rise time across V_{DS} of a DAB CSC 2.0 under different load conditions:(a) M = 0.8 at OC; (b) M = 1.2 at OC; (c) M = 1 at OC; (d) and M = 1.2 at I_o = 2.5 A.

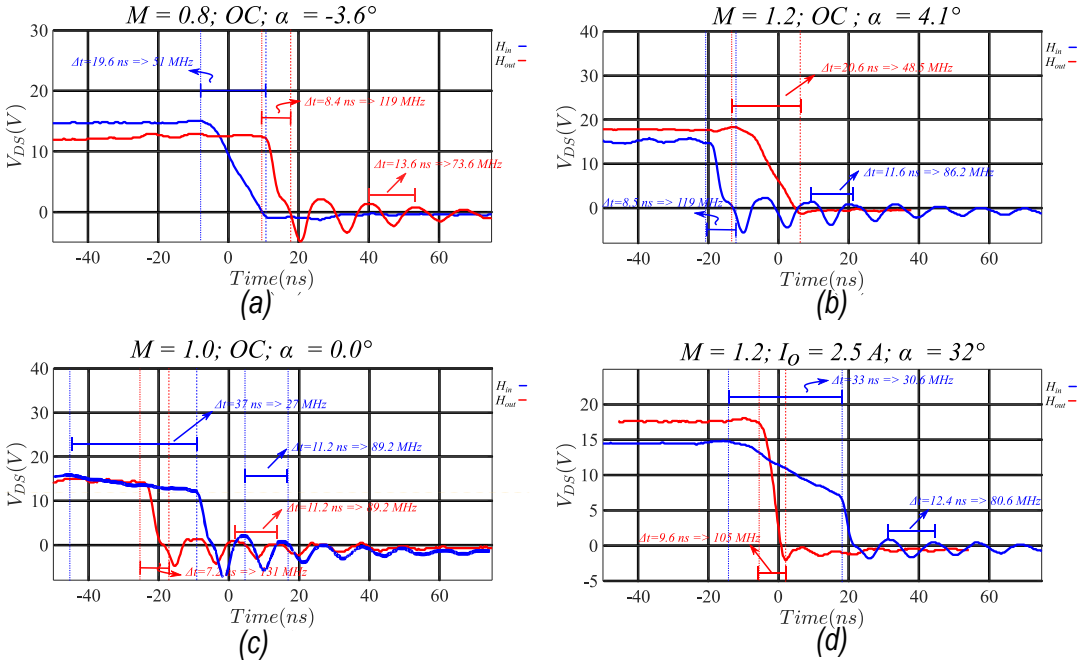


Figure 2.32 Experimental measurement of the fall time across V_{DS} of a DAB CSC 2.0 under different load conditions:(a) M = 0.8 at OC; (b) M = 1.2 at OC; (c) M = 1 at OC; (d) and M = 1.2 at I_o = 2.5 A.

The next section will present the results and comparisons of OC and loaded tests for various operating points, observing from the conducted EMI emission point of view, more specifically conducted emission. A possible advantage of such testing set-up is to be able to get representative EMI noise signature without the need of reaching rated power, speeding up

the EMI pre-compliance tests at early phase. Alternatively, plug-and-play filter can be quickly be tested.

2.5.3.3 DM analysis through measured through EMI Receiver and LISN

Still considering the CSC 2.0, the setup consisted in measuring the DM noise by connection through an LISN (DUAL-LINE V-Y-DELTA FOR GCPC DC-LISN-M2-100) capable of separating CM (asymmetrical disturbances) from DM (symmetrical disturbances), as well as access to the unsymmetrical disturbances on phase "+" and "–" as required by regulation EN 55022/32. Due to slight no difference between measurements phases "+" or "–", only the phase "+" results are provided. The unsymmetrical disturbances are the ones useful for EMC compliance as in EN 55022/32, and only DM harmonics coinciding with the unsymmetrical disturbance are relevant for analysis in this section.

In *Figure 2.33*, the "+", "DM" and "CM" are superimposed for M = 1.0 at I_o = 2.5 A operating point. Notice that, the harmonics multiple of odd switching frequencies are dominated by CM, while the ones multiple of the even switching frequencies are dominated by DM. In practice, due to unbalance impedance path, asymmetry and unknown mismatches of switching events, Mixed-Mode (MM) and accentuation of CM may dominate over DM for the higher frequency range. For the specific case, the three first DM harmonics (first three even harmonics).

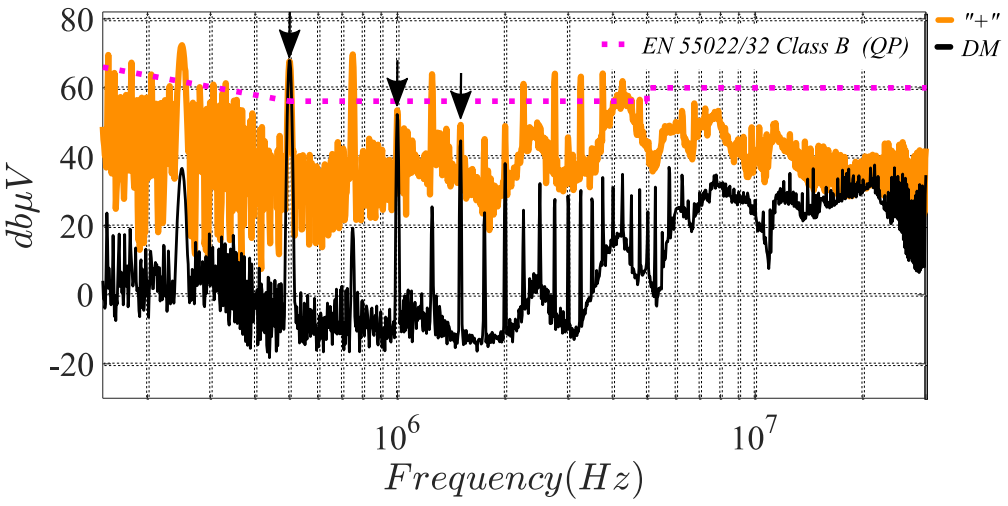


Figure 2.33 Experimental results for conducted emissions for M = 1.0 at I_o = 2.5 A operating point for three LISN modes "+", "DM" and "CM". Only the first three DM even harmonics coincide with the unsymmetrical disturbances.

To better observe and interpret the results, it is presented in *Figure 2.34* the three first even harmonics multiple of the switching frequency for step-up, unitary and step-down modes, for different output currents according to *Table 2-IV*, totalizing 18 measurements. It is

possible to notice that, the OC (step-up or step-down), is similar to the amplitude of the first even harmonic step-up and rated power. Analysing on the first DM harmonic, a linear interpolation is done and plot results are presented in *Figure 2.35*.

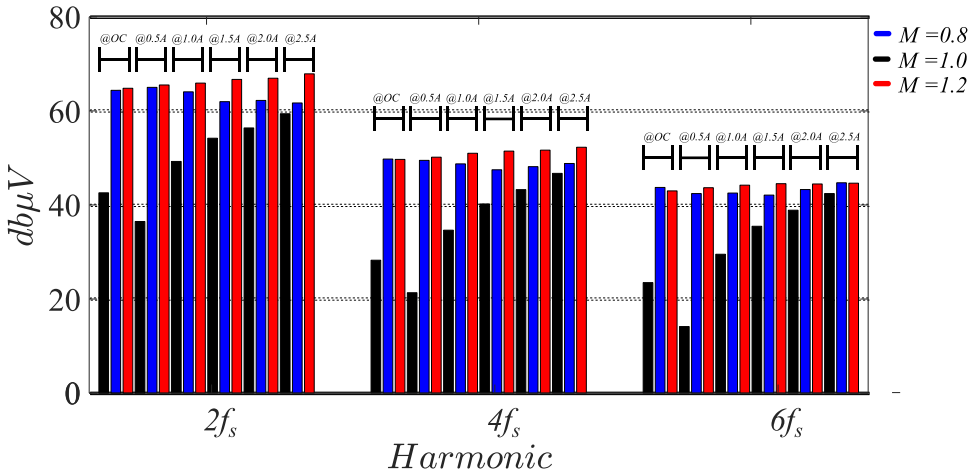


Figure 2.34 Experimental results for DM conducted emissions for all output currents: three first even DM harmonic amplitudes at different load conditions, including OC.

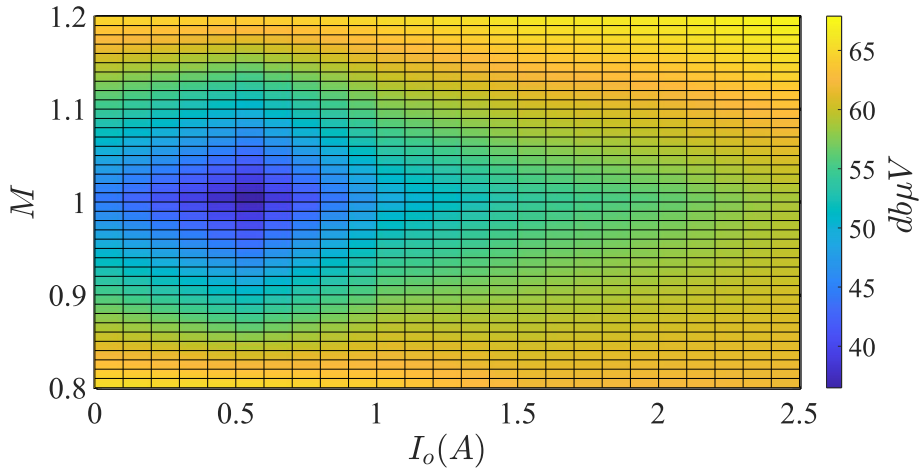


Figure 2.35 3-D plot of the linear interpolation of first DM harmonics (double of the switching frequency) measured.

Finally, comparison between practical and theoretical results are presented in *Figure* 2.36. Besides being the worst case in terms of DM noise, the step-up is the mode that is more linear and contains lesser error between theoretical and practical results. Therefore, it can be concluded that, even though the DM appearing in the OC step-up is not the worst-case, it can be used to infer about the rated power

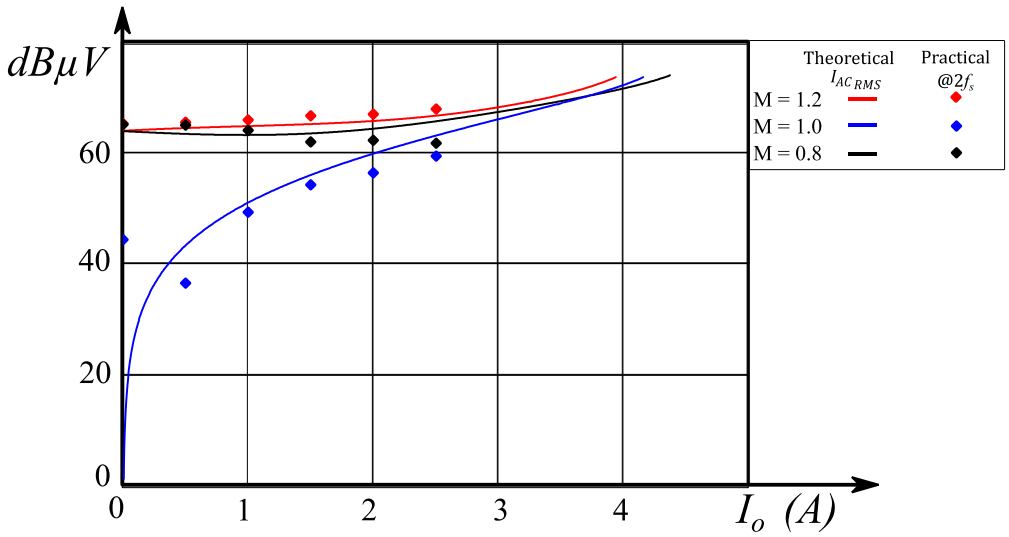


Figure 2.36 2-D plot of the AC-circulating RMS current (theoretical) and practical results.

2.6 Chapter's Final Conclusion and perspectives

To conclude, the inclusion of Q is a parameter that affects the ZVS performance more drastically in the boundary condition. If the design parameters are further away from such boundary, the lossless model can be used, and a small margin can be given to guarantee ZVS.

Due to same reasons and in the same direction, a lossless DAB should be used for CM analysis. On the other hand, the resistive model highly effects:

- The operating-points ($\gamma\ x\ d$), which can be used for control aspects;
- The existence of OC condition, which can be used to EMI signature in an early stage;
- RMS value of the current, useful for designing the power converter;
- The maximum allowed γ, limiting overload;
- The calculation of the efficiency.

A design methodology focusing on ZVS realization for rated power at step-up (M = 1.2) and step-down (M = 0.8) has been provided, focusing not only on efficiency and power density oriented design, but also a design where EMI in terms of DM harmonic spectrum, ZVS and drain-to-source voltage can be improved and predicted.

Reference Chapter 2

[1] G. de Freitas Lima, Y. Lembeye, F. Ndagijimana, and J.-C. Crebier, "Modeling of a DAB under phase-shift modulation for design and DM input current filter optimization," in 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, Sep. 2020, p. P.1-P.10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215851.

[2] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-Time Effect of the High-Frequency Isolated Bidirectional Full-Bridge DC–DC Converter: Comprehensive Theoretical Analysis and Experimental Verification," IEEE Trans. Power Electron., vol. 29, no. 4, pp. 1667–1680, Apr. 2014, doi: 10.1109/TPEL.2013.2271511.

[3] K. Zhang, Z. Shan, and J. Jatskevich, "Estimating switching loss and core loss in dual active bridge DC-DC converters," in 2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL), Vancouver, BC, Canada, Jul. 2015, pp. 1–6. doi: 10.1109/COMPEL.2015.7236501.

[4] F. Krismer and J. W. Kolar, "Accurate Power Loss Model Derivation of a High-Current Dual Active Bridge Converter for an Automotive Application," IEEE Trans. Ind. Electron., vol. 57, no. 3, pp. 881–891, Mar. 2010, doi: 10.1109/TIE.2009.2025284.

[5] I. Aghabali, L. Dorn-Gomba, P. Malysz, and A. Emadi, "Parasitic Resistance Effect on Dual Active Bridge Converter," in IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, Oct. 2019, pp. 1932–1937. doi: 10.1109/IECON.2019.8926896.

[6] R. Lenke, F. Mura, and R. W. D. Doncker, "Comparison of non-resonant and super-resonant dual-active ZVS-operated high-power DC-DC converters".

[7] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," IEEE Trans. Ind. Appl., vol. 28, no. 6, pp. 1294–1301, Dec. 1992, doi: 10.1109/28.175280.

[8] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems".

[9] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics".

[10] A. Rodriguez Alonso, J. Sebastian, D. G. Lamar, M. M. Hernando, and A. Vazquez, "An overall study of a Dual Active Bridge for bidirectional DC/DC conversion," in 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, Sep. 2010, pp. 1129–1135. doi: 10.1109/ECCE.2010.5617847.

[11] A. Rodriguez, A. Vazquez, D. G. Lamar, M. M. Hernando, and J. Sebastian, "Different Purpose Design Strategies and Techniques to Improve the Performance of a Dual Active Bridge With Phase-Shift Control," IEEE Trans. Power Electron., vol. 30, no. 2, pp. 790–804, Feb. 2015, doi: 10.1109/TPEL.2014.2309853.

[12] D. Costinett, R. Zane, and D. Maksimovic, "Automatic voltage and dead time control for efficiency optimization in a Dual Active Bridge converter," in 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, Feb. 2012, pp. 1104–1111. doi: 10.1109/APEC.2012.6165956.

[13] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "Determination of DC link harmonics in dual active bridge DC-DC converters using frequency domain analysis," in 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, May 2016, pp. 70–77. doi: 10.1109/IPEMC.2016.7512264.

[14] D. J. Costinett, "Analysis and Design of High Efficiency, High Conversion Ratio, DC-DC Power Converters".

[15] Y. Yan, H. Gui, and H. Bai, "Complete ZVS Analysis in Dual Active Bridge," IEEE Trans. Power Electron., vol. 36, no. 2, pp. 1247–1252, Feb. 2021, doi: 10.1109/TPEL.2020.3011470.

[16] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "ZVS Soft Switching Boundaries for Dual Active Bridge DC–DC Converters Using Frequency Domain Analysis," IEEE Trans. Power Electron., vol. 32, no. 4, pp. 3166–3179, Apr. 2017, doi: 10.1109/TPEL.2016.2573856.

3. High frequency modelling of the DAB focusing on CM noise

The literature review on CM noise modelling, analysis and attenuation of DAB power converter is relatively recent. Much of the work presented here has been treated while new references have been updated while writing this *Chapter*, it shows that the results presented here are aligned with trendy topics of CM noise attenuation in conventional power converters.

Even though this Chapter attempts to focus on DAB, any full-bridge or half-bridge structure represent and can be used for the comprehension of the high frequency behaviour.

This *Chapter* focus specially on the symmetrisation of the AC-link impedance path and the H-bridge. Even though simulation results using PSIM of the DAB are performed using a complex equivalent circuit, the goal remains to present qualitative results. Simplifying equivalent circuit representation, in which one is originally proposed in this work are also presented.

It is presented in *Figure 3.1*, the parasitic elements that affects the CM and MM of a DAB. As it can be seen, compared to DM, it is quite complex and usually relies on switched models as in PSIM, LTspice and Simulink. The goal of this section is, therefore, a comprehension of the most important parameters, as parasitic capacitances (in green) which are the coupling paths of the CM noise.

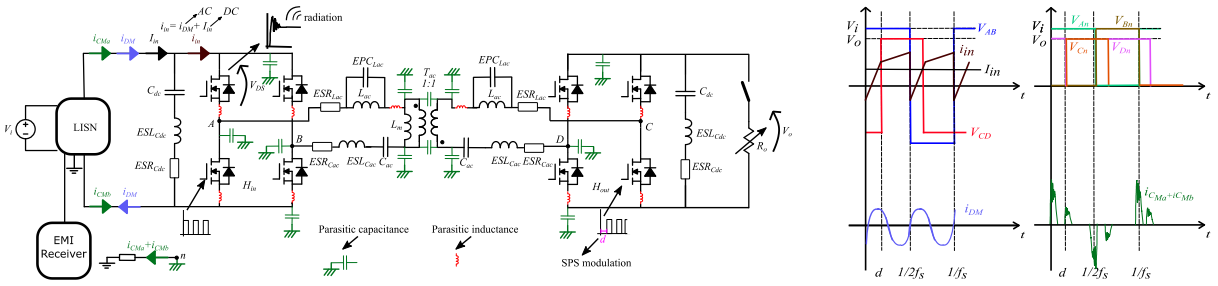


Figure 3.1 *Switched model circuit and impedance path for studying EMI signature of a DAB (left); Main time domain waveforms of a DAB (right).*

3.1 Brief literature review on high frequency spectrum (DM,CM and MM) of the DAB and similar isolated power converters

A brief literature review on high frequency of the DAB and other isolated DC/DC are briefly presented, not because of space purpose, but because that, as aforementioned, only a few contents have been so far addressed in the literature. This section is dedicated for making a critical review literature of the high frequency spectrum (DM, CM MM), the problems, the mitigation solutions and the models of the DAB, specially FB-FB. The idea is to provide enough knowledge regarding DAB converter behavior, in order to be able to consider the main EMI modelling, characterization, and attenuation.

In [1] (2021), the role of parasitic in a DAB converter at 100 kHz and 2 kW made of GaN is discussed. In a first prototype, the DAB converter seems to be designed, e.g selection of the switching frequency, regarding thermal and losses aspects of the transformer. First experimental results failed in a haphazard manner. A debugging section is dedicated to show the main resonances between parasitic capacitances (drain-to-source and inter-winding capacitances). The proposed solutions, diversified in different designs, included reduction of parasitic inductances symmetrical PCB placement of the GaN devices, litz vs copper foil transformer and different GaN devices. A planar transformer of copper foil, known for its high inter-winding capacitance is substitute by a litz wire transformer, which reduces the intert-winding capacitances by a factor of 10 and increases the leakage inductance by a factor of 2 (useful for reducing the external AC-link inductance). The results prove to us that as the increase of switching frequency offered by wideband gap devices, the conventional way of designing and optimizing power converters is no longer adequate. It is interesting to notice that the authors provided an important information of failure at first prototype. Interestingly to observe, given the culture of portraying only successful realization in journals and conferences, the portray of a failure and its debugging has a positive impact on engineering and scientific value, mainly for EMC analysis! Therefore, a few assumptions based on a literature are presented in order to understand possible causes of such failure.

3.1.1 DM high frequency analysis of the DAB

The problems of operating the DAB may have been caused by DM ringing and oscillations, in which *Chapter 2* neglected for the sake of first order solutions. On the other hand, the parasitic capacitances and inductance may cause not only resonance noise, but

reduce efficiency and make the power converter more susceptible to malfunction and failure. Even though the focus is concentrated on the DAB, other isolated power converters such as full-bridge, half-bridge and even Flybacks are reviewed since they share similar and interesting features concerning

In [2] (2017), the resonance of the current across the AC-link is modelled and analysed through simulation results. The inductor plus transformer network are fitted with experimental impedance measurements, and a new design based on such measurements is verified only through simulation, which after proposed solution, the AC-link current simulation does not have oscillations. A continuous work from the authors, in [3] (2021), showed that in a DAB with non-unitary turns ratio, the placement of the AC-link inductor have a more important impact on the HFO current than the transformer design. It is concluded and proved experimentally that the current HFO is mitigated by placing the AC-link inductor only on the low voltage (LV), while keeping similar in an only high voltage (HV) side placement strategy.

Concerning the transformer high frequency model, specifically for the DAB, the analysis of the transformer is done in [4] (2021) from the 6-capacitances model, which is after lumped into one parallel capacitance as in [5] for the noise analysis. The capacitances are extracted from ANSYS Maxewell. A winding configuration is proposed, named MLGM. This winding configuration allows the reduction of the capacitance without increasing the volume of the core compared to conventional designs. It is visible to notice the effect of the oscillating ringing on the AC link in a conventional compared to reduced parasitic capacitance in a MLGM approach.

In [6] (2019), the design of the transformer takes into consideration the electrostatic 3-capacitances, and it is presented an equivalent circuit that shows that ZVS is compromised by the electrostatic energy of the transformer. Fortunately, the ZVS is improved by the magnetic energy of the transformer. In [7], the impact on ZVS and advantages of splitting the AC-link inductance on both sides of a GaN DAB switching at 1 MHz is discussed and experimental results are provided. In [8], the design of a 3.7 kW DAB switching at 500 kHz is done in the frequency domain, with currents being calculating by applying full harmonic order square waveform across the admittance matrix formed by impedance network of the AC-link.

In [9] (2019) a 3-capacitor model is used with a pi-shaped network. The effect of high frequency oscillation is eliminated by reducing the *dv/dt* of the H-bridge output voltage by adding capacitance snubbers on the H-bridge. Simulations (LTspice) and experimental results are presented for a 6.6 kW. Not only the high frequency oscillation was eliminated, but efficiency was improved. Two AC-link inductors are placed on both primary and secondary

sides of the AC-link transformer. Experimentally, the parasitic capacitances are extracted with the impedance characteristics (ICs) methods. The switching frequency of the H-bridge has little contribution to the oscillation as compared to the switching transient times (t_{rise} and t_{fall}), which are the main excitation sources for HFO. According to it, the HFO is more severe on DAB at higher output power due to the increased phase-shift. For the AC-link inductor, only a RL model was used. Zero and poles are found by plotting the input impedance, which is found though a 2-port admittance matrix. The first zero is mentioned as the major contributor to the HFO because of its smaller impedance and the harmonic component of the excitation source. By ignoring the resistances, analytical equations are deduced for the poles and zeros. A simplification is further applied by assuming that the Leakage inductance is much smaller than the magnetizing inductance of the transformer, and an equation gives a direct relation between the AC-link inductance and the three-capacitance model. It is observed that decreasing the *dv/dt* will reduced the excitation voltage at the first zero, and could be completely nullified by conditioning the first zero self-resonant frequency equal to ZCPs. An effective approach to adjust *dv/dt* of the DAB is to connect parallel capacitor across the switching devices, which can further benefit from improved soft-switching condition. By following three steps: i) measure the oscillating frequency, which can be done directly observing the voltage or current of the transformer; ii) the first ZCP should be equal to the period corresponding to the first zero, and then, the dv/dt is calculated; iii) parallel capacitances are added by ZVS conditions at rated power; Experimental results at rated power for different parallel capacitances combined with different gates resistances shows that paralleled capacitances larger than 1 nF, makes de the dv/dt mainly determined by the capacitances, while gate resistance has little influence. The experimental results of the influence of gate resistance combined parallel capacitors is also interesting: i)larger parallel capacitances improve efficiency; ii) whereas larger gate resistances decreases efficiency up to a point parallel capacitor is larger than 3 nF. A local optimum point of the voltage spike is found when parallel capacitors are around 4 nF. More analysis and novel designs are proposed in [10] by reducing the dv/dt of the switching devices, affirming that the traditional method of decreasing the stray capacitances of the transformer in not suitable for high dv/dt occasions. And experimental results show that efficiency is increased when added snubber capacitances are larger than 3 nF. Similar directive of designs are presented in [11]. Similarly [12], switching losses are reduced by adding an external snubber capacitor of 4 nF.

The existing references emphasize the significance of considering high-frequency models in the design and optimization of a DAB. However, it's intriguing to note that pursuing increased efficiency and power density by reducing *dv/dt* contradicts one of the main

advantages of wide bandgap devices, which is their ability to handle higher *dv/dt* values. The statement "the faster the better" requires careful scrutiny, as its applicability depends on various factors such as the specific application, power range, modulation, and material used.

Regarding the DAB layout, various studies have been conducted. In [22], the layout achieves flux cancellation, thereby reducing parasitic inductance and resistances. Another layout discussed in [23] focuses on a GaN DAB operating at 400 W. In [[12], the power loop of a 200 kW DAB with 99.6% efficiency is improved using a 1700 V SiC power MOSFET module. Additionally, [24] [25], delve into the design of a PCB bus-bar for minimizing loop inductance in an ANPC phase leg for a DAB-based DC system. Lastly, [26] explores the power loop, drain-to-source waveform, and ringing for Si MOSFETs and GaN HEMTs.

Furthermore, an active attenuation approach through modulation is proposed for the DAB in [28]. This method involves analyzing the resonance frequency between the DC power bus (e.g., bulk electrolytic capacitor), parasitic inductance, and inner DC bus capacitance. By applying modulation, it becomes possible to eliminate excitation noise resulting from the input DM current of the DAB for the n_{th} harmonic located at the resonance frequency.

In conclusion, designers must take parasitic elements into account, approximating them using analytic equations and observing the input and output impedance of the AC-link and switching events (modulation). This ensures a feasible design that avoids High-Frequency Oscillations (HFO).

3.1.2 CM high frequency analysis

The problems may have been cause not only by HFO DM ringing, but rather a combination of harmful ringing and *crosstalking* [29], and self-turn-on. Indeed, another well-known feature observed in wideband gaps devices is the lower gate-to-source threshold voltage, which facilitates self-perturbation [30]. These problems are susceptible in half- and full-bridge structures and, therefore, applicable and very common to DAB.

For the DAB, in 2020, the work presented in [31] [32] is a 100 kW 3-phase DAB (switching frequency at 20 kHz). Only the CM current circulation measured at input gate-driver was measured. It is interesting to observe how the noise excited by drain-to-source voltages from both input and output of each half-leg impact and generate CM noise current circulating on the gate-driver and CM noise voltage across drain-to-source voltages. The CM noise current reduction proposition benefits from the YY configuration of a very compact medium frequency 3-phase transformer, in which neutral to ground capacitance act as “filters” for the gate-driver CM noise current circulation. As it can be seen, the passive solution is not

only a simple approach, but also improved by compactness and increase of neutral parasitic capacitance to ground, sometimes given as undesired in high-frequency equivalent models. Notice that the solution and CM noise is focused on operability of the power converter, which only allowed successful rated power operation after proposed solutions have been implemented according to the authors. These results shows very clearly that being able to control the parasitic capacitances (and other parasitic) and resonances and their impact is the correct methodology, whether than only minimized parasitic solutions. In general, other removal passive solutions of the crosstalk include reduction in gate driver resistance during turn-off phase, increase of gate-to-source capacitance, increase of negative bias, use of ferrite beads or integrated Rogowski coil [30]. Active open and closed-loop solutions[33], with the advantage of controlling the equivalent resistance for not only avoiding self-disturbance but also improving dynamics and slopes for efficiency purposes. In [34] , the problem of negative spike bias in SiC Based DAB is discussed and issues are solved by magnetic beads. Notice that the CM noise verified in EMC compliance standards has not been addressed by the authors in such work.

The principle of CM noise in a DAB can be first comprehended by half-bridge and full-bridge structures and its switching events and modulations. As explained in [35], the capability of recycling the CM noise current in a two-level modulation (that is, no inner – phase shift). As it can be observed, the CM noise generation in H-bridge structures are largely related to the modulation and gate signal. In theory, by assuming no mismatch and delay of signal triggering and balanced parasitic capacitances, the CM current noise should be null in an H-bridge with no inner phase since no CM voltage is produced. On the other hand, in practice, due to imperfections and often unpredicted drifting variables as delays and unbalanced parasitic capacitances, a noise is always produced. Therefore, it is fair to represent the H-bridge structures and modulation with an equivalent unbalanced parasitic capacitance, or equivalent small inner phase-shit. To the best knowledge of the author, all practical results in which theoretical CM noise voltage is expected to be zero, still presented CM noise current, as exemplified in [36]. For this reason, for the DAB, even though the SPS modulation does not have inner-phase shift, it is still necessary to treat the CM noise. Other noise sources, “outsided” the H-bridge and AC-link structures, such as gate-drivers and signal conditioning (uC etc) named here as residual noises are not explored in this work. Nevertheless, its existence should always be taken into consideration as possible explanation and its impact, mainly in PCA approach.

In 2016, the CM noise signature and attenuation of a DAB based converter is treated in in [37] by means of simulation results. The proposed CM noise reduction is based on a

three-stage CM filter, which, unfortunately, not much detail is presented since, according to the authors, " it is the DM filter and not the CM filter which mainly defines the EMC filter volume, the low-load power factor, and the dynamics of the system". Besides, CM component values are 'based on intuition rather than on modeling and optimization". Indeed, the regular practices of treating CM noise in power converters are usually based on accurate match between simulation and practical results, while assuring an optimized post-prototyped CM filter . As it was presented in *Chapter 1*, it can be considered an obsolete technique because: (i) only simulation results are time consuming tools for optimizing and having important insights, while occupying large amount of unnecessary information; (ii) simplifying equivalent model circuits are comprehensive and allow noise attenuation and understanding much more effectively; (iii) they represent extra losses and volume, rapidly limited by DC rating currents and saturation; (iv) undesirable coupling may deteriorate the attenuation performance; and (v) they are source of near and far field radiation.

Recently (2022), the studies presented in [38] proposed the use of discreet inductors in the input H-bridge in order to mitigate the CM noise. Simplified equivalent circuit models and analytical equations are derived. According to the authors, uncoupled discreet inductors supress, indeed, the CM noise current caused by DM voltages of the mid-point node of the H-brides, acting as a second order (or higher) filter. For the lower frequency range (9 kHz – 1 MHz), a reduction of 20 dB is observed. However, as any filter, introduced resonance frequencies are expected. In the case provided in [38], a low-frequency resonance in the CM impedance. The issue is solved by using a coupled inductor, which equivalent inductance is smaller and provided improved performance. Other interesting active mitigating techniques are also applied, including variable switching frequency and an active filter.

In [39], the noise is analytically derived for DAB and NPC-based DC/DC converters. The power converter has a switching frequency of 50 kHz and output power of 10 kW. On such analysis, parasitic capacitances are assumed to not be symmetrical or similar, while the HF transformer is modelled for inter-winding capacitances as well as the primary to ground capacitances. As already explained, if two nodes have complementary voltage transition, while keeping same parasitic capacitances, there are more chances for CM cancellation. The middle-leg node points of each switching cell should be subjected to complementary dv/dt by synchronized turn-on, or turn-off of two diagonally placed switching devices for a switching event. The CM noise attenuation is proposed by parallelizing an NPC with a full-bridge structure, shifted 180°. As a result, the CM modes at such nodes have same waveforms with opposite polarity. Such parallelization is justified by redundancy and current rating increasing just as much as in the multi-cell approach. Then, experimental tests using only the primary

side of the NPC are performed. The converter with only one leg operating was compared to both legs operation. The results shows a reduction of the peak current from 0.5 A to 0.2 A in the time domain, and 10 dBuA through EMI spectrum at the peak amplitude (around 150 kHz) when both legs operate due to complementary *dv/dt*. Not much improvement is seen on higher frequency spectrum and, again, compared to theoretical results, total CM cancellation was not possible due to the same driving signal delays. In [40], a continuous work from [39], the driving signal is deeply analysed, and CM noise is even more attenuated by acting on driving gate signals by synchronizing and avoiding harmful delays. An improvement of 20 dB at total is observable.

In [39] the CM noise model is proposed through analytical approach by using substitution theorem. Simplifying circuit and assumptions are used to derive the analysis of CM noise: (i) the current source from DM noise does not contribute to CM noise, neglecting, therefore MM; (ii) the input and output capacitances are considered ideal and offers very low impedance. They are represented by short-circuit. Indeed, such assumption is especially true the larger and the more performance in high frequency the capacitor is. Closer to the resonance, such assumption the assumption is better valid, since the attenuation is the largest; (iii) the distributed inter-winding equivalent capacitances are divided equally into lower and upper terminals. The analysis are carried on a DAB 10 kHz, and the study of symmetrisation of the AC-link is presented. It is affirmed that a reduction of 40 dB in CM voltage is achieved by considering symmetrical inductances, observed in LTspice simulation. Indeed, the authors did not use the simplifying circuit, but rather LTspice simulation for demonstrating and verifying its proposition.

In [41], the substitution theorem is also used, but only inter-winding capacitances are used as, apparently the AC-link inductance is only formed by the leakage inductance of the transformer. A discussion and experimental results among the SPS, DPS and TPS modulations with respect to the CM voltage generation is presented. By comparing the modulation, due to CM voltage level generation, the TPS followed by DPS are the ones that generates more CM noise, mainly in the lower frequency range, since five- and three- level CM voltage noise are naturally generated through inner phase-shift. A huge difference of up to 35 dBµV at lower frequency between TPS and SPS for the lower, and for the higher CE frequency limit range (around 30 MHz), the difference is around 20 dBµV. The experimental results are all conducted in the ZVS region, meaning that low load condition is not analysed. The analysed static gains, step-up and step-down (not quantitatively informed) are performed for the TPS and DPS modulation. Regarding both TPS and DPS, the noise is larger when in step-up modes. Unfortunately, for the SPS modulation, only step-down mode is presented,

probably to assure ZVS realization, as already explained in *Chapter 2*. Finally, for TPS modulation, two load charges, 4 A and 8 A were tested, and experimental results showed that the one at higher current load resulted in slightly larger CM noise, which is explained by the faster rise / fall time. A point should be discussed: only the scenarios with ZVS realization were treated. On the other hand, at low load and static gain higher than unitary, the SPS modulation does not allow ZVS realization for the input H-Bridge. Such fact will result in faster rise/fall time, ringing, and lesser symmetrical switching events. In such cases, for the higher frequency spectrum (larger than the switching frequency), the CM noise may present more challenges; both CE at higher frequency and radiated emission (RE) can be substantially increased. Therefore, the comparison TPS x SPS at very low load seems to be a very interesting point to be discussed, that has not been addressed in the literature.

In [42] (2023), equivalent circuit and analysis of CM and DM noise in DAB are discussed by applying substitution theorem. A suitable measurement technique of the DM and CM currents through the transformer using an impedance matched external impedance. On the other hand the asymmetry of the AC-link inductor has not been taken into consideration.

In [43], a 1.5 kW DAB switching at 1.4 kHz is inserted between an active rectifier, resonant capacitor and a pulse power generator as a load. By using simplifying substitution theorem for each cascaded network (power converter and reactive elements), an equivalent Thevenin circuit is deduced and connected in series with the LISN and CM filter. The analysis is carried out by assuming different input filter design for many equivalent Thevenin capacitance (due to parasitic capacitances). One of the problems in EMC is that usually one solution might be excellent for low frequency, but less effective at higher frequency range, while others, good for higher frequency, and ineffective for lower frequency. At first analysis, the CM filter is designed considering the frequency range of the required attenuation. Even though a design procedure solution is proposed for the design of such devices taking into account the parasitic capacitances, it is still not enough for providing enough attention according to IEC61800 requirements. A better solution in combination is then used through balance methodology for each subsystem. With balance technique, based on Wheatstone bridge on each subsystem, that is, adding a specific impedance (capacitor or inductance) between certain nodes.

In [44], operating at 24 kHz and output power around 650 W and inserting a capacitance of 1nF between primary and secondary winding to emulate and control the parasitic inter-winding capacitance. A PV-based solution is proposed by integrating the HERIC to decrease common-mode noise though reducing coupling between AC to DC, and understanding the DAB, and its dual-phase shift modulation, the author provides

improvement on the CM current flowing through transformer. Switching simulation results is also used to build the CM model.

Finally, in [45], a random PWM is applied for the DAB. It can improve EMI by dispersing the harmonics of the switching frequency. On the other hand, the improved results are only depicted through simulation and it is not clear which noise source (DM or CM) is being dealing with.

3.2 Simplified spectra magnitude of drain-source waveforms

Once familiar with the spectra magnitude presented in *Chapter 1*, the rise and fall time as a function of the dimensionless parameters γ_o, σ_o, M and $I_{o\%}$ presented in *Chapter 2*, it is interesting, therefore, to present the simplified spectra magnitude for the DAB to get essential information. For the specific cases in which ZVS realization is not possible, at no or low load condition, a fall time of 1 ns was considered based on experimental results provided in Chapter 2. In *Figure 3.2*, it is presented theoretical normalized spectra magnitude for different load conditions. It is interesting to notice that the load current $I_{o\%}$ will effect mostly the high frequency (starting a 10 MHz), while the static gain effects output H-bridge due to the increase of output voltage. Besides, notice that the behaviour is not linear with the increase of output current due to the ZVS realization existence or not.

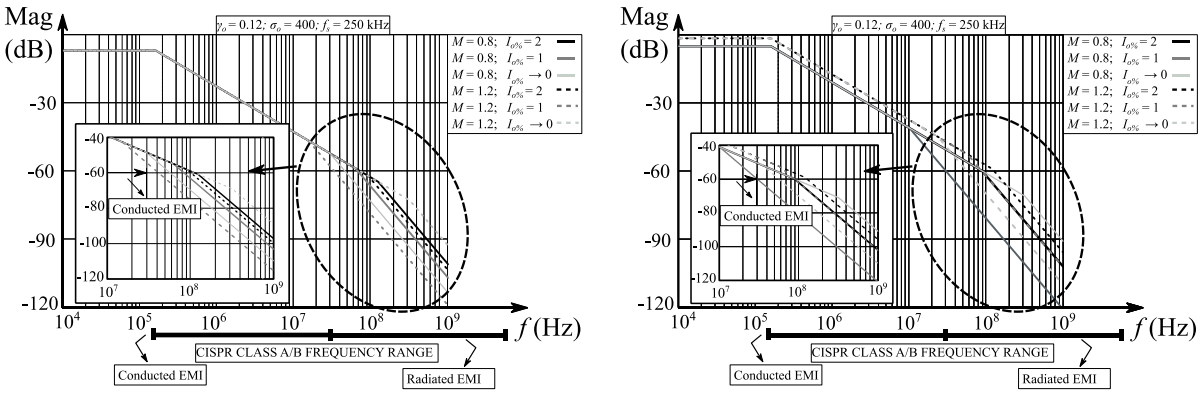


Figure 3.2 *Normalized spectra magnitude of drain-to-source for $\gamma_o = 0.12$, $\sigma_o = 400$ and $f_s = 250$ kHz for different load profiles: (a) input H-bridge; (b) output H-bridge.*

The influence of the switching frequency in the DAB is then analyzed, searching for an optimization in terms of EMI emission and demonstrate the practicality of the methodology presented. Suppose that the designer will keep $\gamma_o = 0.12$ in order to keep same

design characteristics. By decreasing the switching frequency to 100 kHz, the AC-link inductance value has to be increased by a factor of 2.5. As a result the value of σ_o increases up to 1000. Comparison of the results of 100 kHz and 250 kHz shown in *Figure 3.3* that the decrease in frequency may be extremely beneficial in terms of EMI emission mitigation, mainly for lower frequency range (around 9.5 dB). Notice that, even though an increase of AC link inductance and transformer are necessary due to the decrease of the switching, the cut-off frequency of the version at 100 kHz is at 300 kHz, and the amplitude around 9.5 dB lower, requiring a lesser attenuation. Notice that the decrease in the switching frequency is also beneficial for mitigating the spectrum magnitude for the higher frequency range. Such simple results show that the design of a power converter should take into account at the earlier stage the choice of the switching frequency considering among other features the EMI emission.

Following this methodology, the evolution from CSC 2 to CSC 3 has the switching frequency decreased, while increasing the AC-link inductance. Besides, the discrete AC-link inductors are distributed in the four terminals in order to apply symmetry, improve CM recycling and avoid MM.

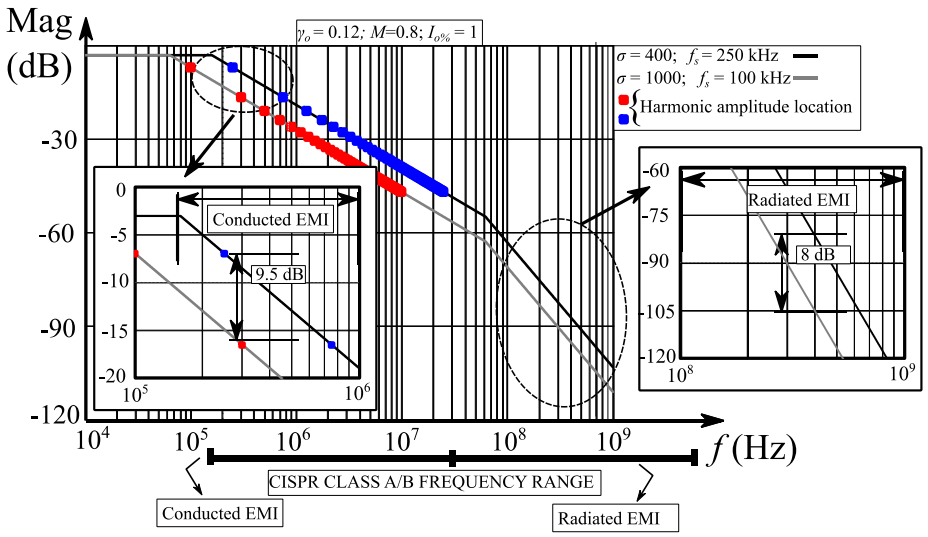


Figure 3.3 *Normalized spectra magnitude of drain-to-source for γ_o = 0.12, σ_o = 400 and f_s = 250 kHz (blue) and σ_o = 1000 and f_s = 100 kHz (red).*

From *Figure 3.2* and *Figure 3.3*, it can be concluded that the CM noise source in the lower frequency can be approximated as sinusoidal voltages in which the switching frequency and the imposed voltages are the dominating parameters to be taken into account. The fall/rise time are parameters to be adjusted for the higher frequency range (end of CE and entire RE frequency ranges).

3.3 Symmetry discussion and simplified equivalent circuit

For the technology chosen in the DAB Cells 3, a copper plane (typically 40 – 180 μm) can be placed and isolated with a dielectric layer (FR4) (typically 0.25mm). Considering a ground plane, a capacitance is formed. Due to proximity such value can be calculated very easily through the parallel plate equation ($C_{D\text{-}ground} = \varepsilon_r\varepsilon_0 \times A/l$). The electric surface of the drain has an area of approximately $A = 2.1\times1.6 = 4.5$ mm^2 and the distance of the isolation is around 0.25 mm. The value of the relative permittivity is considered 4.

Therefore, a parasitic capacitance of around 0.6 pF was estimated. Such capacitance is much lower than the ones in TO-247 that used thermal pads of around 100 μm of thickness [41], which is around 200 pF. As previously, notice that PCB track capacitance to ground should also be accounted, as well as adjacent device capacitance with respect ground. Accounting for PCB total area of 45 mm^2, the capacitance is approximately 6 pF. Such capacitance considers the presence of a ground plane. Due to edge effect and others contribution, it is usually underestimated. Therefore, because the switch device used in this work has a very low parasitic capacitance, the final value becomes dependent on PCB layout and others equivalent capacitance from adjacent devices. This suggest careful attention into symmetrisation, which plays an important role on EMI mitigation. Using same calculation procedure, the DC-bus parasitic capacitance with respect to ground are estimated as 20 pF, since the surface area is around 200 mm^2. Notice that the estimation of the parasitic capacitances highly depends on whether or not a ground plane is present. Since acquiring accurately the values of capacitances in such cases may be complex and time consuming, it is fair to apply a mismatch in order to obtain worst-case scenarios and evaluate the sensibility and impact of each parameter. For example, for the mid-point leg node capacitance with respect to ground, the value could have 1.2 higher at one side; for DC-bus parasitic capacitance with respect to ground, the value could have 1.2 higher at one side, e.g positive bus bar; and, finally, from one H-bridge to the other mismatch factor can be applied. Indeed, the study of the value of such mismatch parameter has not been conducted, and, once again, it is more qualitative than quantitative. Either way, estimating such common mode parasitic capacitances [46] are not an easy task and may depend on vibration (in vehicular applications for example), humidity, dust and etc.

The references so far provided in the literature do not explain in depth all the possibilities of symmetrisation and their consequence in the frequency domain. Neither do they explain the accuracy of the model. The goal of this section is to study the impact of

symmetrisation of the AC-link network regarding CM noise in the frequency domain. At a first time, the switched model is used as a reference; and the symmetrisation study is made for nine different case scenarios and conclusions are drawn. Then, the validity of the simplified equivalent circuit proposed in the literature already discussed previously is compared to a new proposed model, based in the theory explained in *Chapter 1* that takes into the MM caused b non-ideal DC-link capacitors and asymmetries of the parasitic capacitor across the H-bridge.

3.3.1 Switched model

In this section, it is used the equivalent switch model circuit presented in *Figure 3.4*, as a reference to compare with other simplifying equivalent models. As explained in *Chapter 1*, the EMI characterization relies on fixing two LISNs [47] across the input and output ports to draw conclusions on both input and output noises. It can then be assumed that MM coupling due to external propagating path is minimum or neglected. The time step of the simulation is set at 1ns and the results are taking for the 3 ms up to 5 ms, totalizing a simulation time of 3 minutes. Voltage supplies are imposed across input and output capacitor voltages (V_i = V_o = 15 V) to speed up simulation results, avoiding this way a control circuit. The main parameters for running the simulations and make it reproducible are presented in *Table 3-I*, *Table 3-II*, *Table 3-III*. and *Table 3-IV*.

The simulations are explored by varying the symmetry of AC-link inductance (see Figure *3.5*) always keeping the same equivalent impedance network circuit for comparable results. At total 9 scenario cases are evaluated as it will be presented in the next subsections.

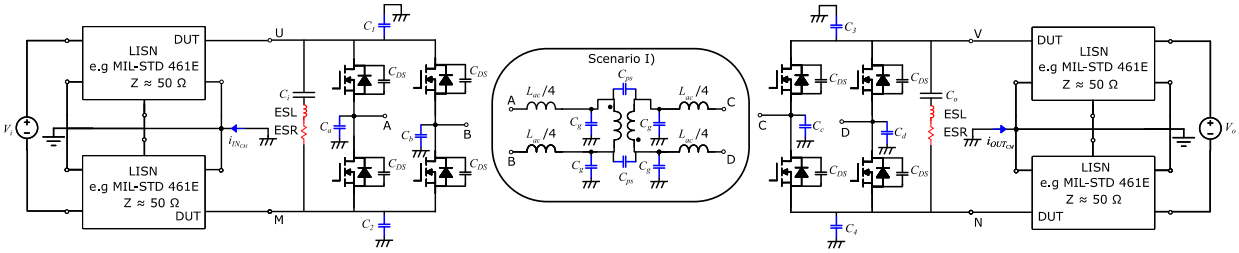


Figure 3.4 *Switched model in the simulation (Input and output are connect to voltage sources through two LISN specified for CISPR).*

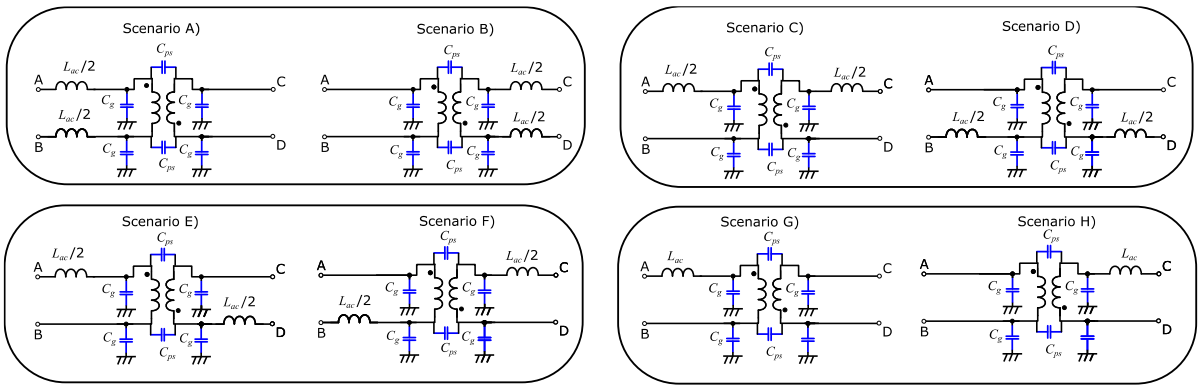


Figure 3.5 *AC-link impedance path – different scenarios with same equivalent inductances.*

Table 3-I Main electrical parameters for generating results.

V_i	V_o	f_s	L_{ac}	α
15 V	15 V	100 kHz	1.58 uH	10°

Table 3-II Parasitic elements of H-bridge used for generating results.

C_a (C_b = 1.2 C_a)	C_c (C_d = 0.8 C_c)	C_1 (C_2 = 0.8 C_1)	C_3 (C_4 =0.8 C_3)	C_{DS}
6 pF	4.8 pF	20 pF	19.2 pF	585 pF

Table 3-III Capacitive parasitic elements of the transformer

C_{ps}	C_g
25 pF	1 pF

Table 3-IV Parasitic element used for the DC-link capacitors

C_{in}	L_{par}	R_{par}
40 uF	0.6 nF	1 m Ω

3.3.1.1 Scenario comparisons

In *Figure* 3.6, it is presented the simulation plotting results for the scenarios A), C), D) and E). When simulating the different scenarios, it is observed that the symmetric with respect to input and output of the AC-link, i.e. A), B) and I) have very small differences, while presenting the minimum CM noise from all scenarios. On the other hand, as expected,

the complete asymmetric scenarios i.e. E), F), G) and H) have presented the largest noise, worst-case scenarios, with little difference among them. Intermediately, the scenarios C) and D), both with a slight difference have presented a similar low noise level in the lower frequency range (up to 10 MHz) as in symmetric scenarios, but increasing noise level, up to the complete asymmetric cases with the increase of the frequency. The placement of these inductors are the ones adopted for CSC 2.0.

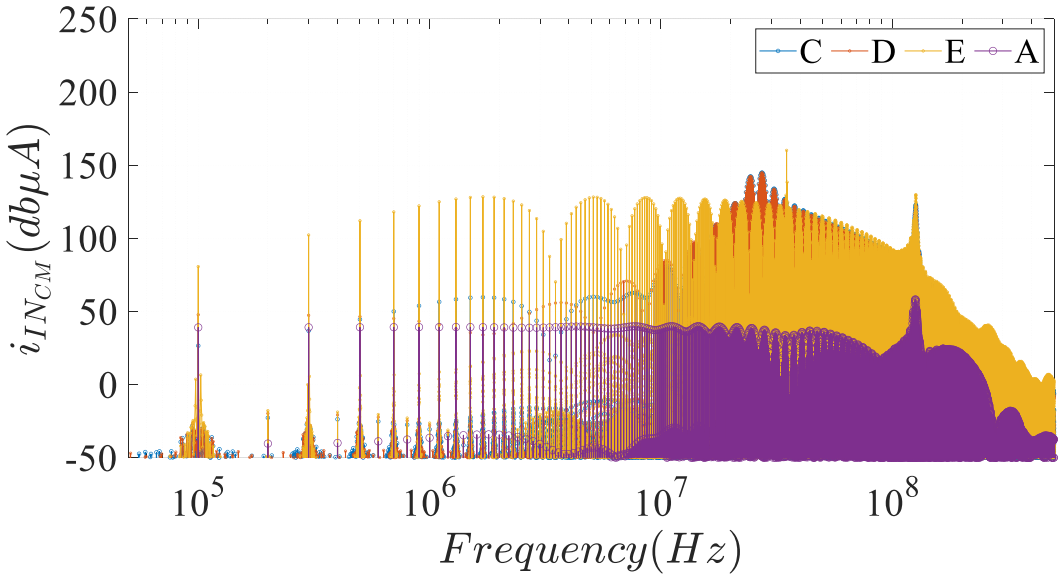


Figure 3.6 *Simulation results of input CM noise current for the scenarios A), C), D) and E). With A) being similar to symmetric scenarios B) and I); and E) being similar to asymmetric scenarios F), G) and H).*

3.3.2 Equivalent simplifying circuit from literature

As previously discussed in *Chapter 1*, A conventional way is the use the substitution theorem [39], [41] (the switching devices are substituted by current and voltage sources) as presented in *Figure 3.7*. Notice that the input and output DC-link capacitance are short-circuited. As previously explained, this is a fair approximation, if clean input and output voltages are assumed by ideal DC-link capacitances, which is possible to neglect the generation of Mixed-mode created by DM current in the input and output H-bridges.

The accuracy of the simplifying equivalent circuit depends on many parameters, and has not yet been addressed in the literature. To understand better the effect of parametric asymmetries together with simplifying equivalent circuit regarding its accuracy, simulation results of the switched and simplified models were compared. For the symmetric configurations (A), B) and I)), such model is accurate enough for the lower frequency range and odd harmonics. On the other hand, for the higher frequency range, and harmonics (even

order) of small amplitude given by the example, assumed to be cause by MM due to asymmetric parasitic capacitance across the H-bridges, the simplified model based on substitution theorem is no longer accurate.

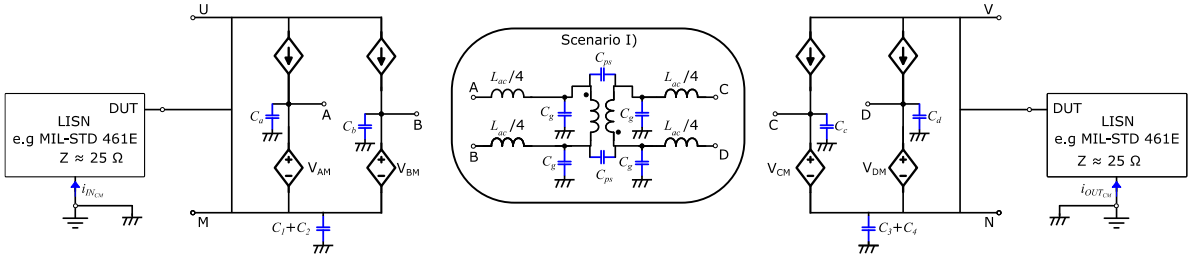


Figure 3.7 *Substitution theorem for the DAB simplified model [39] used for generating results.*

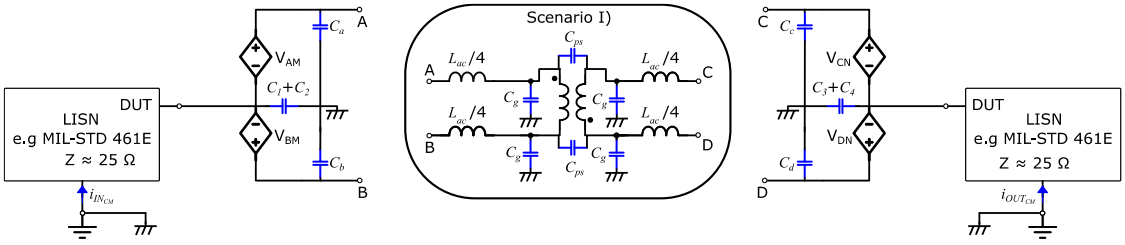


Figure 3.8 *Simplified model [39] used for generating results.*

3.3.3 Proposed Model

The simplified model before mentioned are modelled with the short-circuit assumption of the input and output capacitors does not allow to verify MM, resulting in a model dependent on the sum of capacitances $C_1 + C_2$ and $C_3 + C_4$, and an unbalance on such values is not possible to be accounted.

Searching for a more accurate model while keeping the analysis simple, it is now used the concept of CM and MM presented in [48] [49] [50], as previously explained in *Chapter 1* The theory proposed allow to build equivalent circuit to model CM currents, e.g in Microgrids (DC motors and a three-phase bridge lumped together) [51]. The model is performed and explained for a half-Bridge [48], in which parametric asymmetries between C_1- C_2 and C_a - C_b are discussed. Following the same procedure, it was presented the model for an H-bridge. Once a model for an H-bridge is composed, it is possible to build an entire CM for the DAB by mirroring two H-bridges, and dividing the impedance path of the AC-link by two due to completely symmetric structure (scenario I)), as presented in *Figure 3.9*. Therefore, it

noteworthy pointing that the model is valid for asymmetries across the H-bridge, but not across the AC-link.

Such model is interesting, because: (i) it is simpler and contains less reactive elements; (ii) it is more accurate; (iii) the CM noise mechanism generation is intuitive and helps understanding the main factors contributing for the CM noise. Indeed, it can be seen that the noise generation might be more dependent on the asymmetry of the parasitic capacitance than its absolute value.

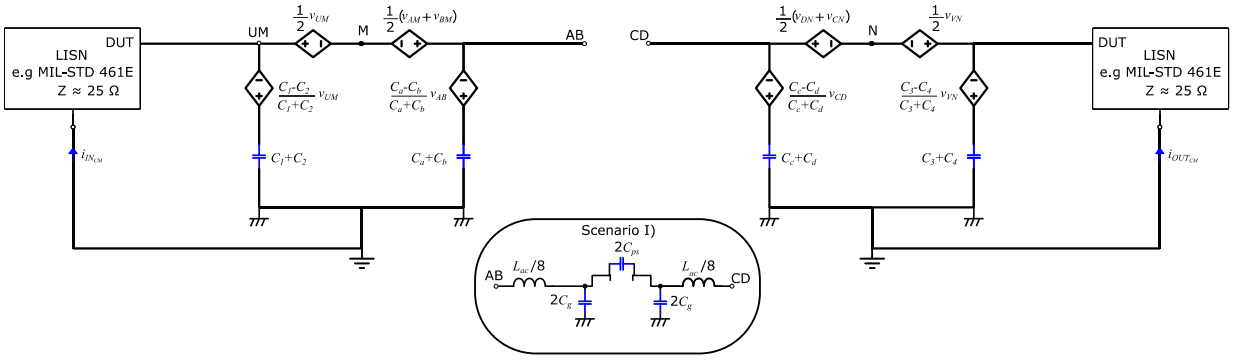


Figure 3.9 *Proposed equivalent CM model of the DAB.*

In *Figure 3.10*, the theoretical results showing the switched model, the model presented

in *Figure 3.8* (named as Simplifying model – Substitution theorem) and the proposed model are presented. It can be seen that, the proposed model has superior advantages and it matches exactly the full switched model in the entire frequency range for the given conditions.

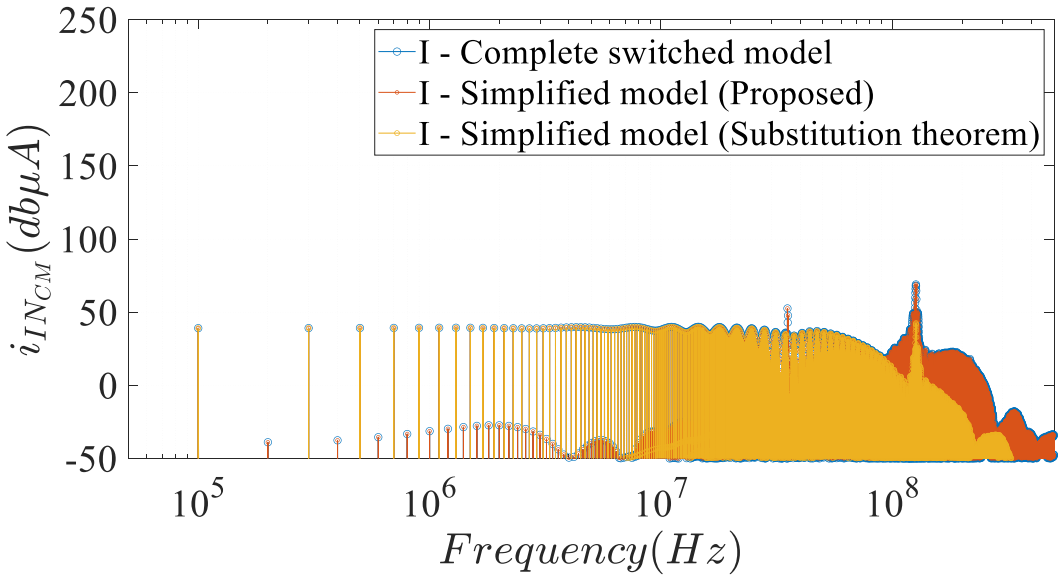


Figure 3.10 *Results of switched, simplifying model [39] and the proposed model.*

3.4 Experimental results

Experimental results were conducted, firstly CSC 2.0 to validate in practice the theoretical results regarding the CM generated by open circuit(OC) testing condition. Then, the practical results regarding the symmetry across AC-link of the CSC 3.0 is presented.

3.4.1 CM noise analysis: from OC to rated values

Considering the CSC 2.0, the setup consisted in measuring the DM noise by connection through an LISN (DUAL-LINE V-Y-DELTA FOR GCPC DC-LISN-M2-100) capable of separating CM (asymmetrical disturbances) from DM (symmetrical disturbances), as well as access to the unsymmetrical disturbances on phase "+" and "–" as required by regulation CISPR16. The EMI receiver is a spectrum analyser (R&S®ESRP3) with a frequency ranging from 9 kHz up to 3.6 GHz.

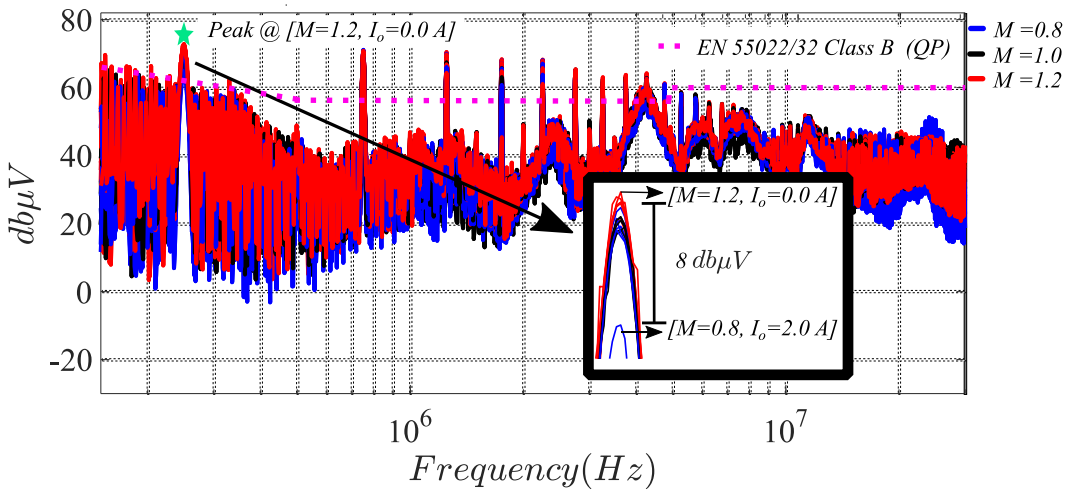


Figure 3.11 *Experimental results for CM conducted emissions for all output currents (see table I), including OC and different static gains M = 0.8 (blue), M = 1.0 (black), M = 1.2 (red): (a) all measurement superposed in which the peak condition is at step-up mode and rated current.*

As previously observed, the relation between measurements at phase "+", shows that all frequencies, expect the ones suggested in previous results (N = 2, 4, 6) should be treated as a CM and / or MM problem. In *Figure 3.11*, it is presented the results for "CM". It is noticed that, a slower decreasing on CM noise is expected with the increasing on switching

frequency. Therefore, treating the CM noise by filtering is much more complicated, as the effectiveness range of the filter should cover the entire range given by the EMC standards (e.g EN55022) Notice that peak condition is detected for step-up and OC, while step-down at 2.0 A presented less amplitude among all tests. The lower amplitude on step-down modes compared to step-up mode is in agreement with the results in [41].

As previously presented in *Chapter 2*, it is presented in *Figure 3.12* the three first CM odd harmonics multiple of the switching frequency. It is possible to notice that, the OC step-up mode presents a worst-condition, quite similar to its full rated power condition for first harmonic.

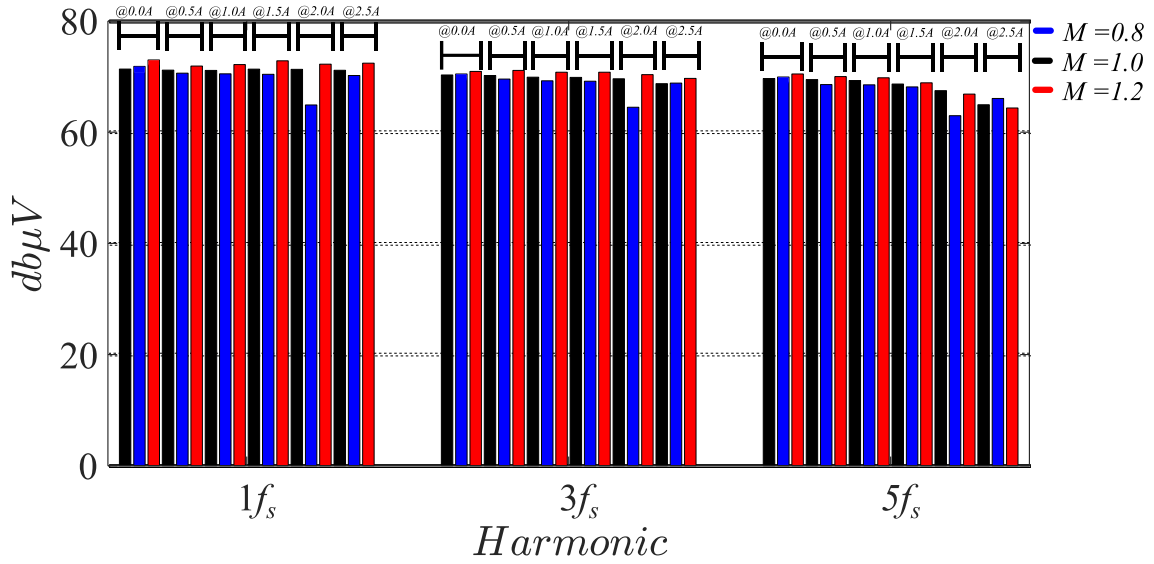


Figure 3.12 *Measurement of the VDS of a single DAB CSC under different load conditions M = 0.8 at OC; M = 1.2 at OC; M = 1 at OC; and M = 1.2 at Io = 2.5 A.*

Nevertheless, the largest harmonic is observed at N = 1 for almost any operating point. A closer look into N = 1 harmonic, shows that step-down mode at rated current, presents least amplitude, while other operating point combinations is almost non-dependent on output current. The explanation follows as presented:

- The CM noise, in general, is highly dependent on the *dv/dt* , mainly at points A, B, C and D. Therefore, direct dependent on V_i and V_o, which means, with respect to applied voltages, the step-up represents the worst case for a given V_i.
- ZVS realization plays an important role with respect to the rise and fall time and high-frequency oscillations at the switching cell transitions. At non or incomplete ZVS, the rise and fall time is much quicker than in ZVS operation. As already explained, ZVS

on both H-bridges, but mainly on the first H-bridge, is much more likely to happen at step-down mode, specifically here M = 0.8, at rated current.

- For step-up mode, the ZVS realization should be carefully observed, as its implementation may be incomplete, mainly at simple SPS modulation.
- The no or very low output current, implies in non-ZVS realization at both H-bridge, even at unitary gain. Therefore, it also represents a worst-case condition similar to step-up rated current mode with no ZVS regarding CM sources
- Even though larger average output currents help bringing in ZVS, if it is not complete, the energy associated to current during the switching transition will also worse the results;
- Finally, even at full ZVS, larger currents will speed up ZVS transitions and will present faster rise and/or fall time, which may worse EMI emissions. Indeed, the idea is to keep in ZVS as slow as possible.

Finally, the full rated and OC conditions are superimposed and presented in *Figure 3.13* in order to show that OC is representative for the range of frequency 150 kHz to 30 MHz. Notice that the no load condition, besides being representative of rated power, imposes worst condition for most harmonics. It is concluded that, in terms of pre-compliance tests, the no-load is well representative for worst-case conditions of CM noise for conducted emission.

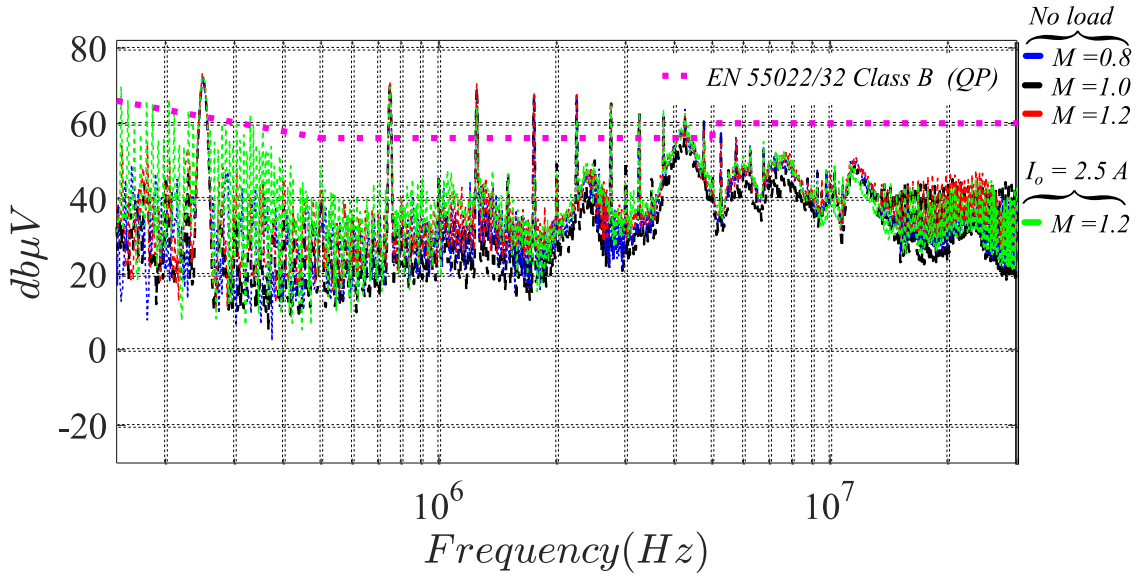


Figure 3.13 *Experimental results for CM conducted emission for OC and rated output currents (superposed), and different static gains M = 0.8 (blue), M = 1.0; OC (black), M = 1.2; OC (red) and M = 1.2; Io = 2.5 A (green).*

Due to its implementation simplicity, requiring same signals at both H-bridges, the OC and unitary static gain condition was observed for different input voltages. Thes results of first and second harmonic order, respectively for CM and DM are presented in *Figure 3.14*. As expected, the CM is linearly dependent on the input voltage, eg for V_i = 15 V, the CM noise for 1*fs* is approximately 70 dbuV, an increase of 6dB is found for V_i = 30 V .

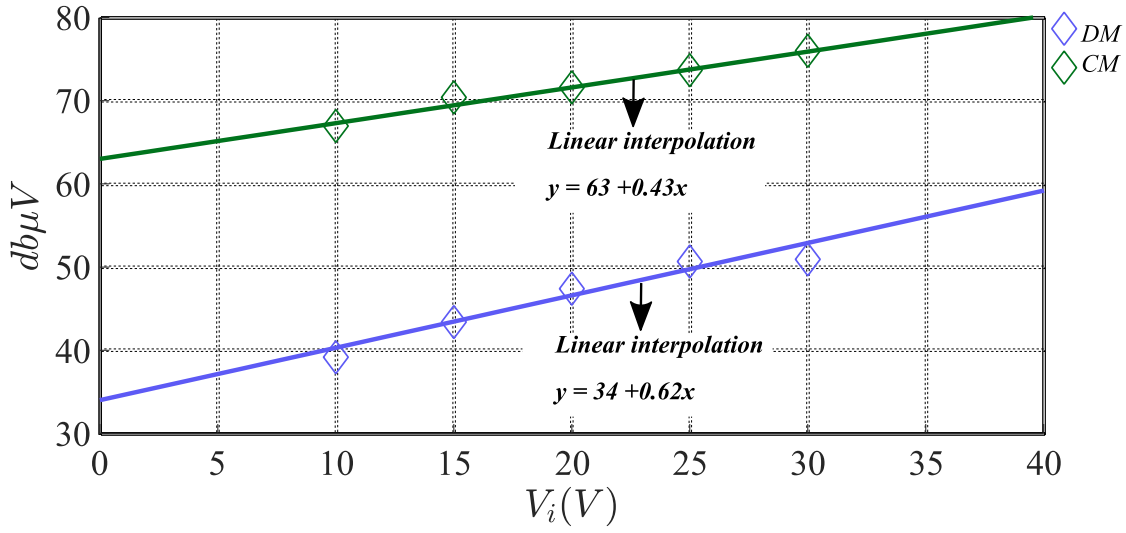


Figure 3.14 *Experimental results for CM (green) and DM (blue) conducted emission for OC and varying input voltage. Simple linear interpolation is presented considering first order approximation.*

3.4.2 Partial conclusion

The OC proved to be representative in terms of CM noise. The advantages include a description of a characteristic behaviour that does not depend on the load. Moreover, it can be performed with simple and linear voltage supply that may impact less on the measurements Important aspects such as oscillation and resonances can also be obtained from such testing condition. One should note that this particular operating point, OC, can be performed for the DAB with SPS modulation, but not necessary other modulation or topologies.

3.4.3 CM noise analysis of the symmetry / asymmetry impedance path of AC-link

In order to conduct these experimental results, the CSC 3.0 is used. By short-circuiting two of the AC-link discrete inductor, it is possible to generate asymmetry along the AC-link,

as presented in *Figure 3.15*. The scenarios re-created similarly to the ones discussed in previous theoretical discussion.

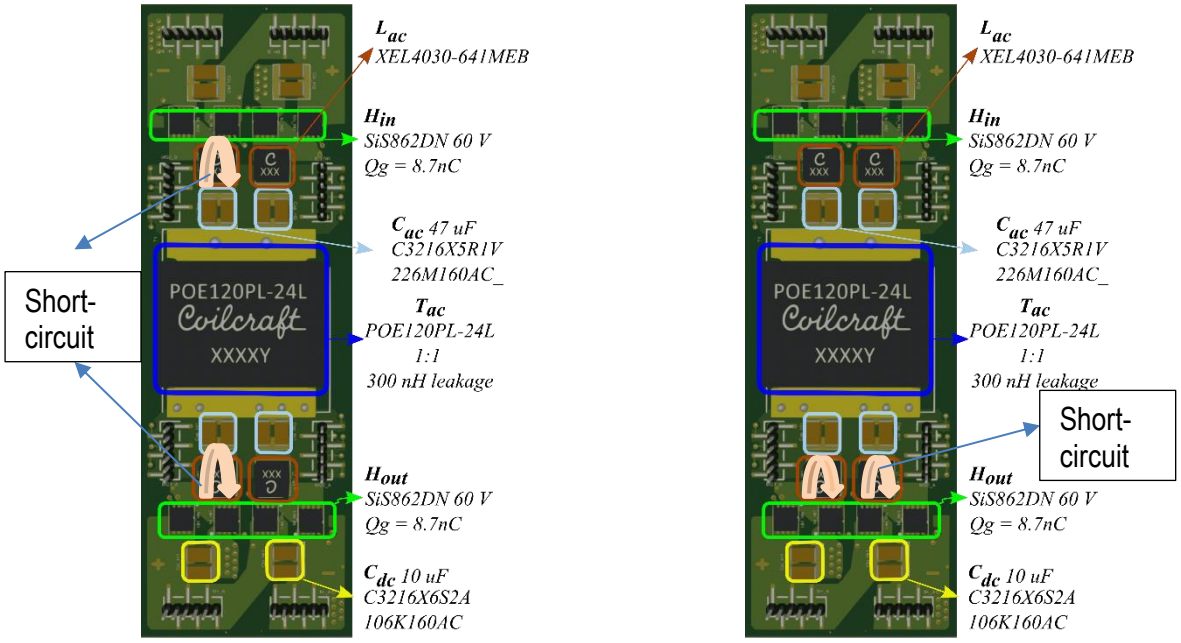


Figure 3.15 *Experimental setup using CSC 3.0: (a) short-circuiting the upper inductors to re-create scenario C); (b) short-circuiting the input inductor to recreate scenario A).*

By short-circuiting, it has been recreated the scenarios from A) to F), in which results are portrayed in *Figure 3.16*. It is observed that, as expected from simulation results, the symmetric scenarios A) and B) presented the lowest CM noise. It is noticed that the CM noise (odd harmonics multiple of 100 kHz) are low and almost "flat" for the entire frequency range, except for the high frequency resonance (> 30 MHz). Such behavior is similar as expected from theoretical results. For scenarios C) and D), it is interesting to noticed that, for the lower frequency range, the CM noise has "improved" for the scenario case C), while equal or larger for the scenario D).For the higher frequency range (> 30 MHz), an increase is expected, as observed in theoretical results. This was also observed in the theoretical results. Finally whereas the complete asymmetric scenario F) presented the highest CM noise. On the other hand, a large difference between scenarios E) and F), not observed in the theoretical results, is observed in practice. Notice that, even harmonics, due to DM noise, are increased. More investigation and future studies are required, but a first assumption could be that the simulation results captured the current, and not the voltage across the LISNs, which depending on the phase measurement could have an impact. Nevertheless, asymmetries across the AC-link is proved to be an important factor for mitigating the CM noise. For comparison

purposes, theoretical results from A) to F) are plotted and presented in *Figure 3.17*. It can be concluded that, even though the parasitic extractions and simulations methods were simple, the theoretical results approach practical ones qualitatively, following tendencies and resonances.

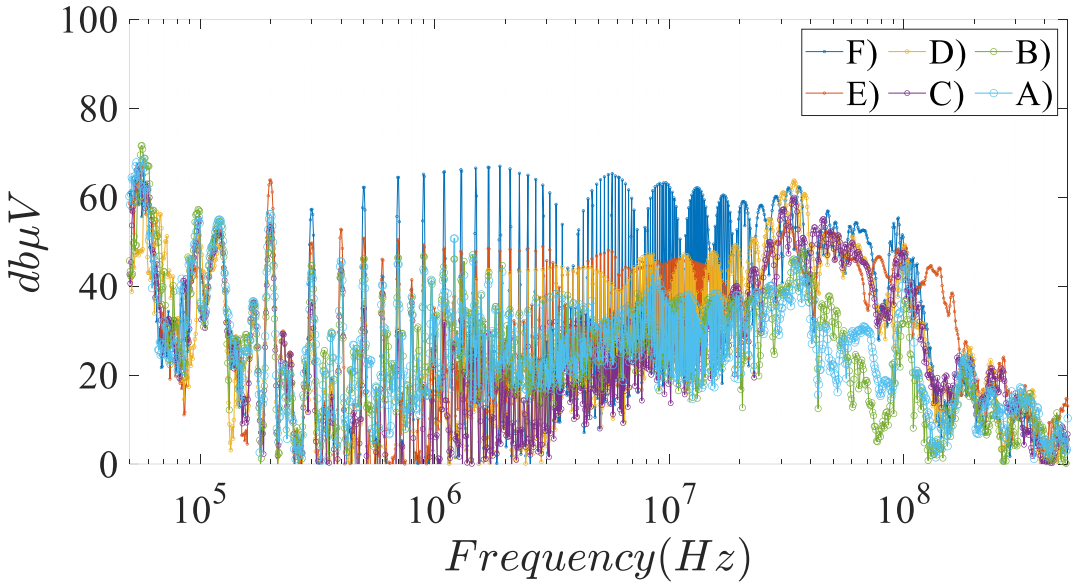


Figure 3.16 *EMI Spectrum of CSC 3.0; V_i = V_o= 15 V; I_o = 2.5 A: scenario cases from A) to F). Spectrum analyser configuration (from 50 kHz to 500 MHz; Span = 499.95 MHz; Rf Att = 0 dB; RBW = 9 kHz; VBW = 30 kHz; Sweeping time = 15 s, Auto peak detector).*

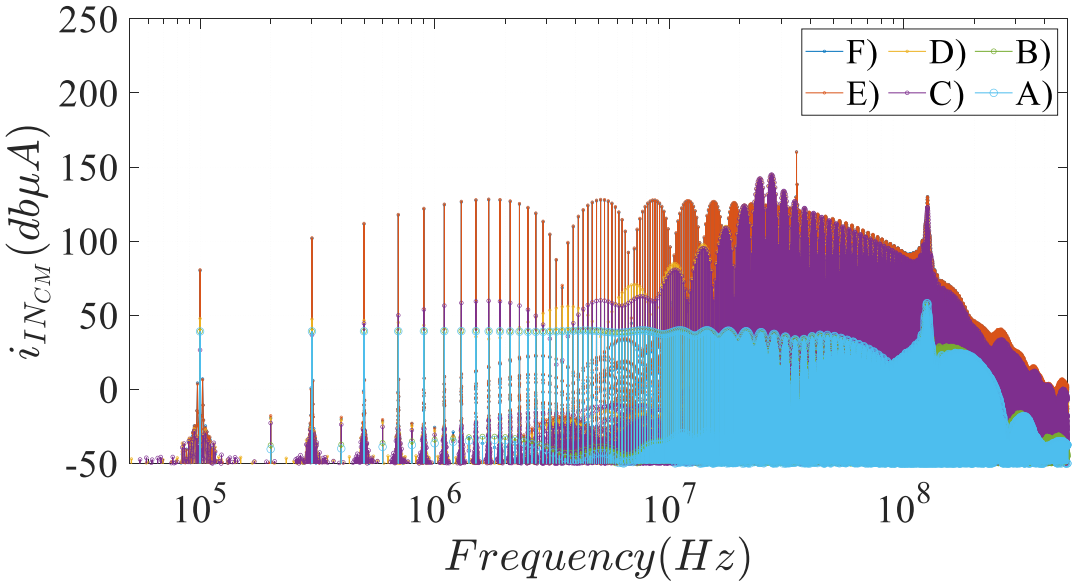


Figure 3.17 *Simulation results of input CM noise current for the scenarios A), B), C), D), E) and F).*

Finally, it is presented in *Figure 3.18* the case I), in which the AC-link inductors were not short-circuited. Different from theoretical approach, the total equivalent AC-link inductance is increased, and, therefore, the necessary phase-shift is also increased, not allowing a performant comparable results. Nevertheless, the CM noise is kept very low (noise floor) in the lower frequency (< 1MHz) and higher in the frequency range (> 2 MHz) when comparing to case scenarios A) and B). Further investigations are required and a left for future studies, but an analogy can be done, in which a higher equivalent AC-link inductance act as a filter for the lower frequency range, but worry resonances must be accounted in the higher frequency range.

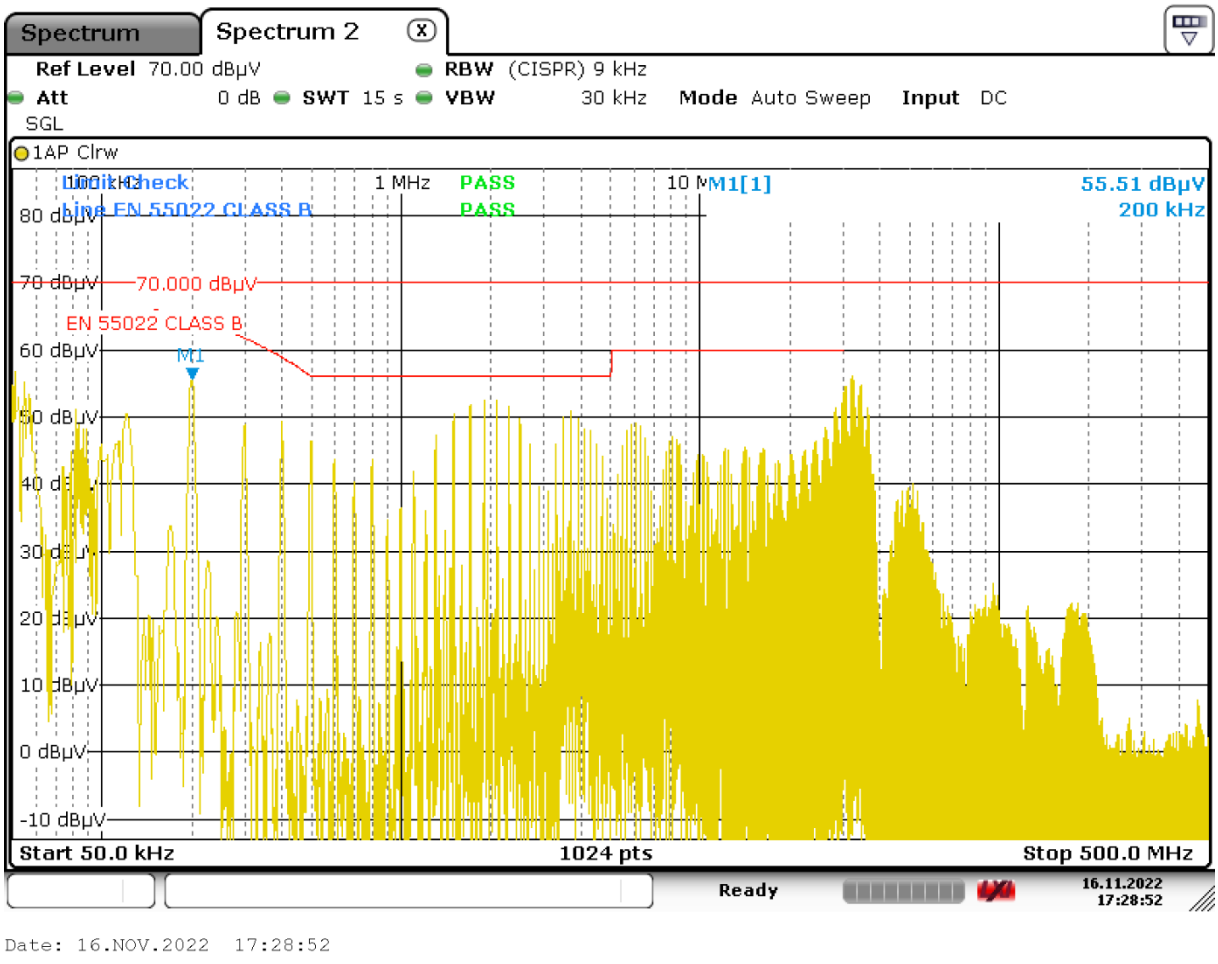


Figure 3.18 *EMI Spectrum of CSC 3.0; Vi = Vo= 15 V; no load; scenario case I). Spectrum analyser configuration (from 50 kHz to 500 MHz; Span = 499.95 MHz; Rf Att = 0 dB; RBW = 9 kHz; VBW = 30 kHz; Sweeping time = 15 s, Auto peak detector).*

3.5 Chapter's Final Conclusion

In this Chapter the worst-case condition for conducted Emission of CM noise with respect to operating point and design parameters are carefully observed through theoretical and experimental results. It is shown that, the CM worst case tends to be the step-up mode and it is less dependent on the load current, from which OC testing can be used as a pre-compliance for acquiring easily the EMI signature at early stage.

With the increasing switching frequency of devices, and consequently its size and parasitic values, the system become very sensible to PCB routing parasitic values and other small capacitances as they are in the same magnitude order. It is therefore, extremely advisable to keep symmetry in such circuits. As it can be seen, the symmetry tends not only improve the EMI emissions, but also makes it possible to provide accuracy without the need of a lot information. The full symmetric system suppress harmful resonances and allowed same results with much simpler equivalent circuit. In order to comprehensively understand and model the CM noise mechanism, an equivalent circuit for CM noise model of the DAB is proposed, taking into account the asymmetry of the parasitic capacitances, while symmetric impedance path across the AC-link must be assumed. The use of current sources to express the MM due to asymmetric inductive path across the AC-link can be suggested as future work for a complete CM noise model of the DAB that takes into account asymmetry all over circuit topology.

Reference Chapter 3

[1] A. Kulkarni, B. Ahmad, J. Kyyra, and J. Makela, "Role of Parasitics in a Dual Active Bridge DC-DC Converter with Gallium Nitride devices," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium: IEEE, Sep. 2021, pp. 1–10. doi: 10.23919/EPE21ECCEEurope50061.2021.9570630.

[2] Z. Qin, Z. Shen, and F. Blaabjerg, "Modelling and analysis of the transformer current resonance in dual active bridge converters," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH: IEEE, Oct. 2017, pp. 4520–4524. doi: 10.1109/ECCE.2017.8096775.

[3] Z. Qin, Z. Shen, F. Blaabjerg, and P. Bauer, "Transformer Current Ringing in Dual Active Bridge Converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12130–12140, Dec. 2021, doi: 10.1109/TIE.2020.3040681.

[4] M. I. Hassan, N. Keshmiri, A. D. Callegaro, M. F. Cruz, M. Narimani, and A. Emadi, "Design Optimization Methodology for Planar Transformers for More Electric Aircraft," *IEEE Open J. Ind. Electron. Soc.*, vol. 2, pp. 568–583, 2021, doi: 10.1109/OJIES.2021.3124732.

[5] R. Barlik, "Determination of the basic parameters of the high-frequency planar transformer," *PRZEGLĄD ELEKTROTECHNICZNY*, vol. 1, no. 6, pp. 73–80, Jun. 2016, doi: 10.15199/48.2016.06.13.

[6] P. Demumieux *et al.*, "Design of a Low-Capacitance Planar Transformer for a 4 kW/500 kHz DAB Converter," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA: IEEE, Mar. 2019, pp. 2659–2666. doi: 10.1109/APEC.2019.8722279.

[7] Y. Xiao, Z. Zhang, M. A. E. Andersen, and K. Sun, "Impact on ZVS Operation by Splitting Inductance to Both Sides of Transformer for 1-MHz GaN Based DAB Converter," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11988–12002, Nov. 2020, doi: 10.1109/TPEL.2020.2988638.

[8] P. Schulting, C. Winter, and R. W. De Doncker, "Design of a High-Frequency Dual-Active Bridge Converter with GaN Devices for an Output Power of 3.7 kW," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata: IEEE, May 2018, pp. 388–395. doi: 10.23919/IPEC.2018.8507882.

[9] B. Cui, P. Xue, and X. Jiang, "Elimination of High Frequency Oscillation in Dual Active Bridge Converters by dv/dt Optimization," *IEEE Access*, vol. 7, pp. 55554–55564, 2019, doi: 10.1109/ACCESS.2019.2910597.

[10] B. Cui, H. Shi, Q. Sun, X. Tang, L. Hong, and B. Zhao, "A Novel Analysis, Design, and Optimal Methodology of High-Frequency Oscillation for Dual Active Bridge Converters With WBG Switching Devices and Nanocrystalline Transformer Cores," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7665–7678, Jul. 2021, doi: 10.1109/TPEL.2021.3049140.

[11] W. Xu, A. Vetrivelan, Z. Guo, R. Yu, and A. Q. Huang, "Efficiency Optimization of Dual Active Bridge Converter Based on dV/dt Snubber Capacitors," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA: IEEE, Jun. 2021, pp. 647–653. doi: 10.1109/APEC42165.2021.9487159.

[12] W. Xu, R. yang Yu, Z. Guo, and A. Q. Huang, "Design of 1500V/200kW 99.6% Efficiency Dual Active Bridge Converters Based on 1700V SiC Power MOSFET Module," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA: IEEE, Oct. 2020, pp. 6000–6007. doi: 10.1109/ECCE44975.2020.9235903.

[13] J. Wang *et al.*, "Accurate Modeling of the Effective Parasitic Parameters for the Laminated Busbar Connected With Paralleled SiC MOSFETs," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 68, no. 5, pp. 2107–2120, May 2021, doi: 10.1109/TCSI.2021.3064010.

[14] K. Ishikawa, S. Ogasawara, M. Takemoto, and K. Orikawa, "Development of an SiC High-Frequency PWM Inverter Using a Thick Multilayer PCB to Minimize Stray

Inductance," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 - ECCE Asia)*, Niigata: IEEE, May 2018, pp. 2725–2731. doi: 10.23919/IPEC.2018.8507376.
[15] M. Pulvirenti, L. Salvo, A. G. Sciacca, G. Scelba, and M. Cacciato, "Modeling of SiC-MOSFET Converter Leg Including Parasitics of Printed Circuit Board Layout and Device Packaging," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, p. P.1-P.10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215618.
[16] M. Ali, J.-K. Muller, J. Friebe, and A. Mertens, "Analysis of Switching Performance and EMI Emission of SiC Inverters under the Influence of Parasitic Elements and Mutual Couplings of the Power Modules," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, p. P.1-P.10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215600.
[17] M. Ali, J. Friebe, and A. Mertens, "Simplified Calculation of Parasitic Elements and Mutual Couplings of Wide-bandgap Power Semiconductor Modules," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, p. P.1-P.10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215953.
[18] C. Kueck, "Application Note 139 October 2012".
[19] W. Belloumi, A. Breard, J. Ben Hadj Slama, and C. Vollaire, "Numerical approach to study layout influence on electromagnetic emissions signature," in *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, Suntec City, Singapore: IEEE, May 2018, pp. 1093–1098. doi: 10.1109/ISEMC.2018.8393956.
[20] W. Belloumi, A. Breard, J. Ben Hadj Slama, and C. Vollaire, "Impact of Layout on the Conducted Emissions of a DC-DC Converter Using Numerical Approach," in *2018 15th International Multi-Conference on Systems, Signals & Devices (SSD)*, Hammamet: IEEE, Mar. 2018, pp. 287–291. doi: 10.1109/SSD.2018.8570701.
[21] N. R. Mehrabadi, I. Cvetkovic, J. Wang, R. Burgos, and D. Boroyevich, "Busbar design for SiC-based H-bridge PEBB using 1.7 kV, 400 a SiC MOSFETs operating at 100 kHz," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA: IEEE, Sep. 2016, pp. 1–7. doi: 10.1109/ECCE.2016.7854903.
[22] H. Wang, L. Jiang, X. Wu, M. Shao, B. Wang, and X. Wu, "Design of Onboard 270V/28V DAB Converter for Optimized Parasitic Paramters," in *2022 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, Haining, China: IEEE, Oct. 2022, pp. 1–6. doi: 10.1109/ITECAsia-Pacific56316.2022.9942115.
[23] M. Zhu, C. Shao, S. Wang, L. Hang, Y. He, and S. Fan, "System Design of Dual Active Bridge (DAB) Converter Based on GaN HEMT Device," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, Harbin, China: IEEE, Aug. 2019, pp. 1–6. doi: 10.1109/ICEMS.2019.8921597.
[24] S. Kumar and G. Gohil, "Conducted EMI Performance of Active Neutral Point Clamped Phase Leg for Dual Active Bridge Converter based DC system," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA: IEEE, Mar. 2020, pp. 1697–1704. doi: 10.1109/APEC39645.2020.9124272.
[25] S. Kumar, B. Akin, and G. Gohil, "EMI Performance of Active Neutral Point Clamped Phase Leg for Dual Active Bridge DC–DC Converter," *IEEE Trans. Ind. Appl.*, vol. 57, no. 6, pp. 6093–6104, Nov. 2021, doi: 10.1109/TIA.2021.3102000.
[26] Y. Zhang, S. Wang, and Y. Chu, "Analysis and Comparison of the Radiated Electromagnetic Interference Generated by Power Converters With Si MOSFETs and GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8050–8062, Aug. 2020, doi: 10.1109/TPEL.2020.2972342.
[27] L. Zhai, G. Hu, M. Lv, T. Zhang, and R. Hou, "Comparison of Two Design Methods of EMI Filter for High Voltage Power Supply in DC-DC Converter of Electric Vehicle," *IEEE Access*, vol. 8, pp. 66564–66577, 2020, doi: 10.1109/ACCESS.2020.2985528.

[28] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "Active Suppression of Selected DC Bus Harmonics for Dual Active Bridge DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8857–8867, Nov. 2017, doi: 10.1109/TPEL.2016.2647078.
[29] P. Wang, L. Zhang, X. Lu, H. Sun, W. Wang, and D. Xu, "An Improved Active Crosstalk Suppression Method for High-Speed SiC MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7736–7744, Nov. 2019, doi: 10.1109/TIA.2019.2916302.
[30] H. Geramirad, F. Morel, B. Lefebvre, C. Vollaire, and A. Breard, "Experimental study of an EMI reduction gate-driver technique for turn-off transition of 1.7 kV SiC MOSFET," p. 10.
[31] H. Geramirad *et al.*, "Experimental EMI study of a 3-phase 100kW 1200V Dual Active Bridge Converter using SiC MOSFETs," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France: IEEE, Sep. 2020, pp. 1–10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215666.
[32] H. Geramirad *et al.*, "Conducted EMI reduction in a 100kW 1.2kV Dual Active Bridge converter," p. 9.
[33] Y. Lobsiger and J. W. Kolar, "Closed-Loop d${\bm i}/$d ${\bm t}$ and d ${\bm v}/$d${\bm t}$ IGBT Gate Driver," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3402–3417, Jun. 2015, doi: 10.1109/TPEL.2014.2332811.
[34] Y. Tian *et al.*, "A Passive Component Based Gate Drive Scheme for Negative Gate Voltage Spike Mitigation in a SiC-Based Dual-Active Bridge," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA: IEEE, Sep. 2018, pp. 1841–1845. doi: 10.1109/ECCE.2018.8557591.
[35] J.-C. Crébier, "CONTRIBUTION A L'ETUDE DES PERTURBATIONS CONDUITES DANS LES REDRESSEURS COMMANDES," 1992.
[36] K. Tian, T. Li, and K. F. Yuen, "A Common-Mode Voltage Reduction Modulation for a Phase-Shift DC-DC Converter," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen: IEEE, Nov. 2018, pp. 1–5. doi: 10.1109/PEAC.2018.8590545.
[37] J. Everts, "Design and Optimization of an Efficient (96.1%) and Compact (2 kW/dm3) Bidirectional Isolated Single-Phase Dual Active Bridge AC-DC Converter," *Energies*, vol. 9, no. 10, p. 799, Oct. 2016, doi: 10.3390/en9100799.
[38] D. Jiang, Z. Wang, W. Chen, J. Liu, X. Zhao, and W. Sun, "Common-mode Electromagnetic Interference Mitigation for Solid-state Transformers," *Chin. J. Electr. Eng.*, vol. 8, no. 3, pp. 22–36, Sep. 2022, doi: 10.23919/CJEE.2022.000023.
[39] B. Dwiza and J. Kalaiselvi, "Analytical Approach for Common Mode EMI Noise Analysis in Dual Active Bridge Converter," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, Singapore: IEEE, Oct. 2020, pp. 1279–1284. doi: 10.1109/IECON43393.2020.9254895.
[40] S. Kumar, S. K. Voruganti, and G. Gohil, "Common-mode Current Analysis and Cancellation Technique for Dual Active Bridge Converter based DC System".
[41] Y. Yan, Y. Huang, R. Chen, and H. Bai, "Building Common-Mode Analytical Model for Dual Active Bridge Incorporating With Different Modulation Strategies," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12608–12619, Nov. 2021, doi: 10.1109/TPEL.2021.3071440.
[42] B. Dwiza, K. Jayaraman, N. B. Y. Gorla, and J. Pou, "Analysis of Common-Mode Noise and Mixed-Mode Differential-Mode Noise in Dual Active Bridge Converter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 11, no. 1, pp. 657–666, Feb. 2023, doi: 10.1109/JESTPE.2022.3201327.
[43] M. S. S. Nia, P. Shamsi, and M. Ferdowsi, "EMC Modeling and Conducted EMI Analysis for a Pulsed Power Generator System Including an AC–DC–DC Power Supply,"

IEEE Trans. Plasma Sci., vol. 48, no. 12, pp. 4250–4261, Dec. 2020, doi: 10.1109/TPS.2020.3035640.
[44] G. Buticchi, D. Barater, L. F. Costa, and M. Liserre, "A PV-Inspired Low-Common-Mode Dual-Active-Bridge Converter for Aerospace Applications," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10467–10477, Dec. 2018, doi: 10.1109/TPEL.2018.2801845.
[45] J. Kang, X. Zhu, and L. Yun, "Application of Random PWM Technology in DAB Converter," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Shenzhen: IEEE, Nov. 2018, pp. 1–6. doi: 10.1109/PEAC.2018.8590544.
[46] S. Karimi, E. Farjah, T. Ghanbari, F. Naseri, and J.-L. Schanen, "Estimation of Parasitic Capacitance of Common Mode Noise in Vehicular Applications: An Unscented Kalman Filter-Based Approach," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7526–7534, Aug. 2021, doi: 10.1109/TIE.2020.3007088.
[47] A. N. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. D. Brovont, and M. S. Mazzola, "Methodology for Characterization of Common-Mode Conducted Electromagnetic Emissions in Wide-Bandgap Converters for Ungrounded Shipboard Applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 300–314, Mar. 2018, doi: 10.1109/JESTPE.2017.2721429.
[48] A. N. Lemmon, A. D. Brovont, C. D. New, B. W. Nelson, and B. T. DeBoi, "Modeling and Validation of Common-Mode Emissions in Wide Bandgap-Based Converter Structures," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8034–8049, Aug. 2020, doi: 10.1109/TPEL.2019.2963883.
[49] A. D. Brovont and A. N. Lemmon, "Common-Mode/Differential-Mode Interactions in Asymmetric Converter Structures," p. 7.
[50] A. D. Brovont, "Generalized Differential-Common-Mode Decomposition for Modeling Conducted Emissions in Asymmetric Power Electronic Systems," *IEEE Trans. POWER Electron.*, vol. 33, no. 8, p. 6, 2018.
[51] A. D. Brovont and S. D. Pekarek, "Derivation and Application of Equivalent Circuits to Model Common-Mode Current in Microgrids," *IEEE J. Emerg. Sel. Top. POWER Electron.*, vol. 5, no. 1, p. 12, 2017.

4. Unifying and Generalized Mismatch Impact Analysis of Modular Converters through Two-Port Network Theory

Multi-cell and modular converters with common duty-ration control are subjects well discussed in the literature within different topologies of cell converters. One of the main challenges in such technologies, besides finding the optimum number of converter cells for a given application [1], is the component dispersion due to precision and parasitic of devices as well as signal delays. This is illustrated in [2] [3] [4] [5] [6] for Dual Active Bridge (DAB) - based converters, in [7] [8] [9] [10] [11] for Flyback-based, and [12] [13] [14] [15] [16] [17] for Buck-based converters. Besides, for each possible configuration, an entire paper is required for analysis. However, only a few of them try to generalize and unify their analysis methods [18] [19] [20] [21] [22]. Sometimes, misconceptions due to wrong generalized conclusion may be misleading to a wrong path. For example, if a boost-based converter may be connected in ISOP and IPOS configuration without problems, will the DAB-based or Flyback-based follow the same behavior? The answer is not always. How can one straightforwardly recognize if a desired connection realization is possible? What are the rules and criteria? How to observe the impact of component dispersion in modular converters easily and analytically? Do the approaches so far presented in the literature are well defining the problematic? How and what are the properties to correlate dual principles between the IS/IP and/or OS/OP possibilities?

Such questions are answered in *Section* through a proposed theory based on two-port network theory, providing fundamentals of power electronics, still lacking on the literature, of lossless power converter to unify the comprehension of such contents and analytically / automatically observe the impact on voltage- and current-sharing of any lossless DC/DC converter. Through a generic formulation, important properties, statements and rules summarize and clarify the challenges faced by modular converter, that is, a formalism for some well-defined necessary conditions when associating DC/DC converters are given. The approach benefits from two-port, also known as quadrupole, properties for comprehensive, unified and effortless steady-state analysis. Mathematical and electrical relationship among the many associations are discussed, avoiding unnecessary circuit analysis, while benefiting

from algebraic and dual principles. Finally, the proposed work stablishes a methodology for separating and analyzing the variables for any ideal power converter in terms of two-port network parameters. As active two-port networks are intrinsic from lossless power converters, singularities are solved by a simple transformation proposition. The classical converters (Buck-, Boost- and Flyback- based) in both CCM and DCM modes as well as DAB converters are discussed, as they all present distinguishable and complementary characteristics.

In the next *Section 3.2*, the same theory based on two-port network is now fully applied for the specific case of a DAB operating at SPS modulation, using the resistive model provided in *Chapter 2*. Indeed, it is a necessary condition for connection realization the DAB cells in among all the known configurations types: input-parallel output-parallel (IPOP), input-series output-parallel (ISOP), input-parallel output-series (IPOS), and input-series output-series (ISOS). Specifically, the approach is used to observe the impact on voltage sharing (static gain M), output current (I_o), input current (I_i) and efficiency (η) with respect to: (i) number cells (N); quality factor mismatch (Q); (ii) AC-link equivalent inductance (L_{ac}); (iii) phase-shift mismatch (d); (iv) and, finally, frequency mismatch (f_s). Once again all mismatches due to possible device precisions and/or signal integrity. The resulting voltage- and output current-sharing's can then be used to input the variables (M, γ, σ), which in turn can be used to characterize the DM and CM noise currents in a normalized manner, as already presented in *Chapter 2*. The use of two-port network can also be used for analysis of cascades systems, including cascading with parallel resistance to represent short-circuit across DC-link capacitor and study the impact on efficiency and redundancy. Due to inclusion of resistance, elementwise nonzero matrixes allow easy transformation among all two-port network matrix representations, without problems of singularities. This means that from any matrix representation specific and useful for a connection realization can easily be transformed into other ones specific for their respective connection realization. Coupling *Chapters 2, 3* and *4* can be considered to build tools to design a PCA, analytically, capable of dealing with highly complex subjects such as EMC management in a way not yet seen in the literature.

Finally experimental results are provided to, at a first moment, support the findings of voltage and current sharing in ISOP and IPOS cases.

4.1 A Two-Port Network Based Transformation for Unified and Comprehensive Steady-State Analysis of Lossless Modular Power Converters

N-port modelling and representation techniques [24], [25] are born in analogical circuits representing much of theoretical bases in all electrical engineering fields. There are three main reasons for describing and characterizing a given system into a two-port network, or quadrupole: i) treat the system as a "black box" and model it from the input and output signals; ii) describe and characterize a system by two ports with the properties of quadrupoles, and, therefore, benefit from simple algebraic manipulation, e.g. inversion and dual properties, compact and fast results; and iii) easy cascade or interconnect in series or parallel with other subsystems, which are likewise modelled as two-port networks, and, then, summarize it into one quadrupole system. The ii) and iii) reasons are the goal of this work. References [26] [27] [28] [29] [30] [31] [32] [33] [34] [35] [36] [37] [38] [39] [40] [41] [42] [43], inspire and demonstrate that it is worthwhile representing a power electronic system into two-port network for the sake of a systematic, effortless and unified representation.

As presented in *Figure 4.1*, correlations exist among two-port networks, DC-transformers and dependent source model representations with respect to voltages and currents across input and output ports, $(V_i, V_o) = (V_1, V_2)$ and $(I_i, I_o) = (I_1, -I_2)$. The purpose of such representation of input and output voltages and currents is irrelevant for insertion loss *IL* calculation, but it is important and better to represent as in the two-port network in order uniformly define [44] and avoid confusions, mainly when cascading sub-systems. The effort is, therefore, to formalize the fundamentals of DC/DC modelling [45] [46] [47] [48], into a two-port network, similar to [32] [33] [34] [35] [37] [38] [39] [40] [41].

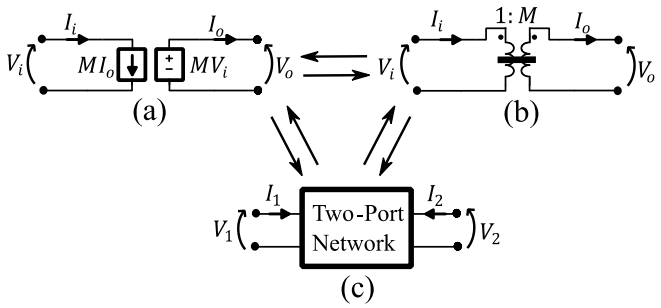


Figure 4.1 Equivalent circuit to represent ideal power converters: (a) Dependent source model representation; (b) DC transformer model representation and (c) proposed Two-port network representation.

If one can represent a power converter in a two-port network, it is possible to integrate it into other sub-systems, such as, filters, resistances representing parallel losses or short circuits as well as other power converters (modular ones, particularly).

Recapitulating, mismatch refers to the variations in performance characteristics of individual modules within a modular power converter system. Modular converters are composed of multiple identical or similar units, called modules that are connected in parallel and/or in series to form the complete converter system. However, due to manufacturing tolerances, control signal delays, temperature variations, and other factors, the modules may not perform exactly the same, resulting in mismatches. Mismatch can result in several issues, [18] [19] [20] [21] [22], mainly when subjected to a common-duty-ratio control, such as:

- Reduced overall efficiency of the converter system;
- Uneven current and voltage sharing among the modules;
- Reduced voltage regulation.

There are several ways to consider and to address mismatch in the design of modular power converters:

- Component selection: Carefully selecting components with tight tolerance specifications and similar performance characteristics can minimize the impact of mismatch. This can be achieved by using high-quality, well-established components from reputable manufacturers;
- Module design: Designing the modules to be as identical as possible can also help to minimize mismatch. This can be achieved by using identical circuit topologies, component values, and layout for each module;
- Feedback control: Implementing a feedback control system can help to monitor and adjust the performance of each module in real-time, thus reducing the impact of mismatch. This can be achieved by using sensors to monitor the performance of each module and adjusting the control signals to ensure that the modules are operating within specified limits;
- Redundancy: Using a redundancy approach can increase the system reliability, by adding extra modules or sub-modules that can take over in case of failure of one of the modules;
- Statistical analysis: During the design process, a statistical analysis can be used to estimate the impact of mismatch on the overall performance of the system. This can

provide a better understanding of the expected performance of the system and help to identify potential issues that may arise due to mismatch;

- Testing and validation: Testing and validating the performance of each module and the overall system can provide important information about the impact of mismatch and can help to identify potential issues that may need to be addressed.

To apply statistical analysis, it is necessary mathematic equations to be inputted. Instead of going through different circuit analysis and/or the investigation of the natural balancing for each connection configuration type, as usually presented in the literature, it is demonstrated that, thanks to the well-known properties and formalism of a two-port network representation $\boldsymbol{Y}$-, $\boldsymbol{Z}$-, $\boldsymbol{G}$- and $\boldsymbol{H}$- as presented in *Figure 4.2*, simple mathematical relationships, such as inversion, dualities, matrix summations and transformations may be used, as it will be presented in subsection *4.1.2*. Moreover, simple observation of the two-port parameters may reveal whether or not connectivity realization is possible, as presented in subsection *4.1.3*. Provided the concepts in subsections *4.1.2* and *4.1.3*, synthesized parameters for classical DC/DC and DAB-based converters are presented in subsections *4.1.4* and *4.1.5*. An illustrative example, presented in Appendix 4.B of a boost-based DC/DC converter in DCM not yet presented in the literature confirms the effectiveness of the approach and is compared to numeric simulation of PSIM. Finally, in subsection *4.1.6*, practical verification comparing to experimental results of three different references are presented.

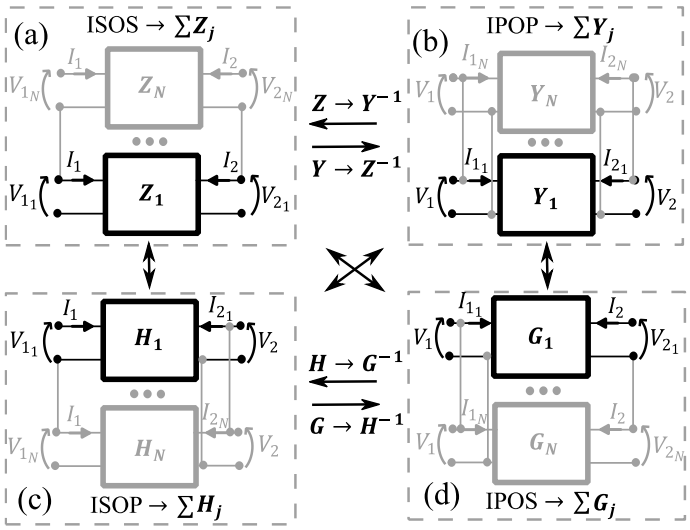


Figure 4.2 Use of two-port network properties and transformation for modular converters: (a) $\boldsymbol{Z}$- representation for ISOS; (b) $\boldsymbol{Y}$- representation for IPOP; (c) $\boldsymbol{H}$- representation for ISOP and (d) $\boldsymbol{G}$- representation for IPOS.

4.1.1 Two port-network theory in power electronics

The goal is not to provide a literature review, but rather a brief introduction and a few references are provided and discussed as an attempt to characterize and explain the main use of two-port network theory in power electronics.

Treating the system as a "black box" [27], also called behavioral model [49], the use of two-port network theory has been presented for EMI signature characterization, through online measurements [26] . The goal is to be able to model and represent analytically a power converter or switched models. In order to consider cascaded systems, cables [29] and power filters [28] can be easily evaluated through chain parameters (***T***).

The two-port network representation finds application for impedance couplers (AC-link). In [50], the ZVS boundary in DAB-based converters is analytically observed through square voltage inputted across the magnetic AC-coupling impedance put admittance matrixes (***Y***-). In [51], the magnetic ***Y***- port is combined with the electric coupling (3-capacitances), by simply using the sum property of matrices, facilitating the analysis of the transfer-function. Finally, in [52], an universal differential / common mode model for both conducted emission (CE) and radiated emission (RE) frequency range (up to 100 MHz) is based on an active ***Z***-port.

The use of two-port network for control is wide. For a single power converter, the goal is to systematically define transfer functions for control oriented modelling [30] - [35]. The concept can be, once again generalized into a DC distribution power system level, as presented in [39]-[43], through the use of Cascaded,(***T***- ports), and Parallel, using (***Y***- ports) systems. In the same road, control modelling and challenges for modular converters have been treaded in [19], particularly for an ISOP case in [12]. The use of one or more of these aforementioned approaches can perfectly be used for modular converter and stability analysis of power converters, which is out of scope of this work. Even though small signal analysis are a particular case of large signal analysis, which in turn can be used to derive simulation results in steady-states, they do not answer, analytically and instantaneously, the impact of mismatch. This is because, when deriving the corresponding transfer function, they are function of internal parameters, such as static gain and equivalent resistive load. For a single power converter, these parameters are well known and imposed, which is not the case for modular converters. The subject of discussion in this work, even though it is inspired by those methods, more precisely by any two-port network theory, is an approach for systematically generating parameters that are function of external variables for closed-loop solutions, avoiding unnecessary circuit analysis or numerical results and simulations. At some point, the

mismatch impact can be even detached from the DC/DC topology! Therefore, even though there is an overlapping of ideas and concepts, one should not confuse the subtle difference in the proposed work here with steady-state analysis of fixed transfer functions.

Indeed, from all the references provided, what could perhaps better be assimilated to this *Chapter* is the work presented in [31], an analysis of the PV Panels Connections using two-port network theory. Likewise, the goal remains the use of two-port network to draw easier and fast conclusions on power, voltage and current sharing when subsystems are subjected to mismatch among different connection types.

Moreover, by observing well defined parameters and rules, it is possible to know whether or not connection realization is possible for any ideal DC/DC converter without the need of complex balance mechanism of voltage across DC-link capacitors, since only steady-state is the concerning topic.

4.1.2 Definition

4.1.2.1 T-Chain matrix representation

The DC transformer model provides the basic function well known in classical converters in CCM, due to their voltage source characteristics, as shown in (4.2) on its $\boldsymbol{T}$- or $\boldsymbol{ABCD}$- (chain) (4.1) parameter format, being equivalent to the DC transformer model representation presented in *Figure 4.1 (b)*.

Another interesting way of modelling, when conveniently, is through admittance gyrators [37], [38], also named trans-admittance, better appropriated for integrating voltage-source input port to current-source output port [37], as presented in (4.3) on its $\boldsymbol{T}$- matrix format representation.

The purpose of presenting both representations in this work is to show that, regardless of the output characteristic, the four two-port parameters presented in *Figure 4.2* can be extracted through the combination of the parameters static gain, $M = V_o/V_i = I_i/I_o$, and trans-admittance $J = I_o/V_i = I_i/V_o$. Indeed, for a lossless case, the $\boldsymbol{T}$- can be still represented by another two matrices, as long as each line contains a zero. Due to the fact of being an active quadrupole (lossless), it is important to avoid singular points (division by zero) and wisely use fill the matrix representation through parameters that will allow free transformation to other matrix transformations. One goal is the use of invertible matrixes to easily find their dual representation by inverting the matrixes. Later, in order to exist transformation between $\boldsymbol{T}$- to $\boldsymbol{Y}$- or $\boldsymbol{Z}$- and $\boldsymbol{T}$- to $\boldsymbol{H}$- or $\boldsymbol{G}$- it is necessary, respectively and in

that order, that a or b and c or d are non-zero parameters. By assuming lossless model, all the four matrix representations depicted in *Figure 4.2*, the objective is to represent power converters consisting on anti-diagonal invertible matrixes composed of the parameters J and M, as it will be later shown.

$$\boldsymbol{T} = \begin{pmatrix} a & b \\ c & d \end{pmatrix} \tag{4.1}$$

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} \frac{V_1}{V_2} = \frac{1}{M} & 0 \\ 0 & \frac{I_1}{-I_2} = M \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{4.2}$$

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} 0 & \frac{V_1}{-I_2} = \frac{1}{J} \\ \frac{I_1}{V_2} = J & 0 \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix}. \tag{4.3}$$

4.1.2.2 $\boldsymbol{Y}$- and $\boldsymbol{Z}$- matrix representation

Following regular two-port network theory, a transformation from $\boldsymbol{T}$- to $\boldsymbol{Y}$- is possible, according to (4.4) when considering the gyrator representation (4.3). Without loss of generality it is possible to state*:*

"The input and output currents of any lossless power converter can be expressed through admittance matrix $\boldsymbol{Y}$- composed of dimensional parameters, trans-admittances, as a function of input and output voltages, as expressed in (4.5)".

The trans-impedance, $\boldsymbol{Z}$- matrix, can be found through a dual process. However, the simple definition of $\boldsymbol{Z} = \boldsymbol{Y^{-1}}$ is enough and demonstrate the practicality of such two-port network theory. Likewise, the inverse transformation $\boldsymbol{Z}$ or $\boldsymbol{Y}$ to $\boldsymbol{T}$ is possible following regular two-port network theory, but such feature is not exploited in this section. Due to power conservation and, as the sense of output current (from the load to port 2) is presented opposite from usual power converter representation (entering the load), a "reciprocal" property is observed.

$$\boldsymbol{T} \rightarrow \boldsymbol{Y} = \begin{pmatrix} y_{11} = \dfrac{d}{b} = 0 & y_{12} = -\dfrac{\det(\boldsymbol{T})}{B} = \dfrac{1}{J} \\ y_{21} = -\dfrac{1}{b} = -\dfrac{1}{J} & y_{22} = \dfrac{a}{b} = 0 \end{pmatrix} \tag{4.4}$$

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} 0 & J \\ -\dfrac{1}{J} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}. \tag{4.5}$$

4.1.2.3 $\boldsymbol{H}$- and $\boldsymbol{G}$- matrix representation

Without need of proof, the lossless active $\boldsymbol{G}$- two-port network is equivalent to the dependent source representation, presented in *Figure 4.1 (b)*. Besides, it is also possible to define it from $\boldsymbol{T}$- to $\boldsymbol{G}$- transformation, presented in (4.6), but considering the $\boldsymbol{T}$- matrix representation presented in (4.2). Another statement, well known, is then observed:

"*The input current and output voltage of any ideal power converter, due to its static gain feature, may be expressed through hybrid matrix* $\boldsymbol{G}$*- composed of a dimensionless static gain parameter as a function of input voltage and output current, as expressed in (4.7)*".

Likewise, due to inverse properties, $\boldsymbol{H} = \boldsymbol{G^{-1}}$ is instantaneously and dually defined. The inverse transformation $\boldsymbol{G}$- or $\boldsymbol{H}$- matrix representations to $\boldsymbol{T}$- can be applied, but such feature is not exploited in this section.

$$\boldsymbol{T} \rightarrow \boldsymbol{G} = \begin{pmatrix} g_{11} = \dfrac{c}{a} = 0 & g_{12} = -\dfrac{\det(\boldsymbol{T})}{a} = -M \\ g_{21} = \dfrac{1}{a} = M & g_{22} = \dfrac{b}{a} = 0 \end{pmatrix} \tag{4.6}$$

$$\begin{pmatrix} I_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} 0 & -M \\ M & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ I_2 \end{pmatrix}. \tag{4.7}$$

4.1.2.4 Canonic representation

As it can be observed so far, even though the efforts of avoiding problems of singularity have been applied, an active quadrupole cannot allow freely all transformation through conventional two-port network theory matrix transformations due to a singularity of

zero division. Therefore, the $\boldsymbol{G}$- or $\boldsymbol{H}$- matrices cannot be transformed from $\boldsymbol{Y}$- or $\boldsymbol{Z}$- matrices; and vice-versa, due to zero division, as exemplified in the $\boldsymbol{Y}$- to $\boldsymbol{G}$- transformation presented in (4.8)

$$\boldsymbol{Y} \rightarrow \boldsymbol{G} = \begin{pmatrix} g_{11} = \dfrac{\det(\boldsymbol{Y})}{y_{22}} \rightarrow \infty & g_{12} = \dfrac{y_{12}}{y_{22}} \rightarrow \infty \\ g_{21} = -\dfrac{y_{21}}{y_{22}} \rightarrow -\infty & y_{22} = \dfrac{1}{g_{22}} =\rightarrow \infty \end{pmatrix}. \tag{4.8}$$

To overcome it, a simple transformation is proposed and presented in *Figure 4.3*, turning possible free transformation among all four two-port network matrix representations as previously presented in *Figure 4.2*. It consists on the use of inversion, as aforementioned, as well as the multiplication of the resistive load R_L seen by the output of the power converter, and put on matrix format (4.9) for uniform notation and purposes. Prove of it is not provided. In fact, there are different ways to prove such proposed transformation, being a merely formalism, but necessary for the comprehension of connectivity realization. Despite the fact of being simple, the dependence on such variable reveals important aspects regarding connectivity of modular power converters as it will be presented in 4.1.3.

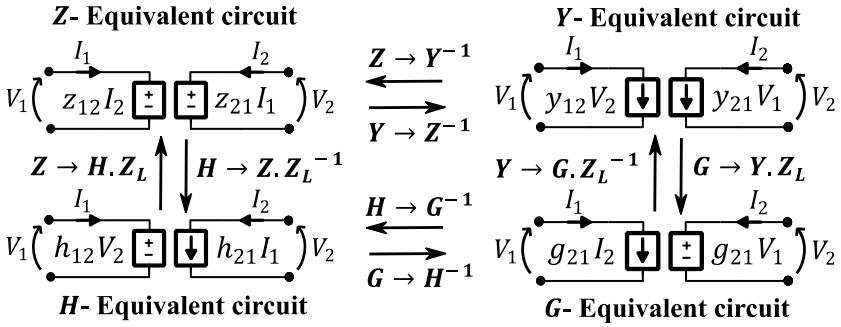


Figure 4.3 Active and lossless equivalent circuit representation and their respective proposed transformation.

$$\boldsymbol{Z_L} = \begin{pmatrix} R_L & 0 \\ 0 & R_L \end{pmatrix}. \tag{4.9}$$

4.1.2.5 Synthesized $\boldsymbol{y_{12}}$- and $\boldsymbol{g_{21}}$ - parameters of classical-based and DAB-based DC/DC Converters

Based on subsections 4.1.2.2, 4.1.2.3 and 4.1.2.4, the well-known basic properties of the converter topologies, classical converters in Continuous Conduction Mode (CCM) [45] and

Discontinuous Conduction Mode (DCM) [46], as well as the DAB-based converter using single phase-shift modulation (SPS) [2], [3], the y_{12}- and g_{12}- parameters are synthesized in *Table 4-I*. Their values are depicted, as their parameters cover a broad amount of properties in which will be later discussed.

Table 4-I Synthesized y_{12}- and g_{21} - parameters for Classical- and DAB-based DC/DC Converters.

DC/DC Converter topology	y_{12}	g_{21}
All Classical DC/DC – based in CCM	$\frac{M(D_o,a)^*}{R_L}$	$M(D_o,a)^*$
Buck – based in DCM	$\frac{K_o(1-M)}{M}$	$\frac{K_o}{J+K_o} = M(K_o,R_L)^*$
Boost – based in DCM	$\frac{K_o}{M-1}$	$\frac{J+K_o}{J} = M(K_o,R_L)^*$
Flyback – based in DCM	$\frac{K_o}{M}$	$\frac{K_o}{J} = M(K_o,R_L)^*$
DAB-based	$K_o{}'$	$K_o{}'R_L$

*According to their respective static gain presented in [45] and [46].

Where $K_o = {D_o}^2/2f_oL_o$, for classical-based DC/DC converters; $K_o{}' = a.D_o(1-D_o)/2f_oL_o$, for DAB-based converters performing SPS modulation; L_o (H) rated inductance; f_o (Hz) the rated switching frequency; D_o the rated common-duty-ratio; and a the transformer turns ratio.

4.1.3 Connectivity, Properties and Correlations

So far, the representation of any ideal power converter as a two-port network has been defined generically. Such definition can be used to integrate other sub-systems, e.g. filter and/or other power converters, which can be exactly the same or different due to parameter mismatches. Besides, conveniently any of them can be used for simulation of large signals, which is not covered in this work. From now on, the structure is treated as being a modular converter, containing N-converters, where N is the total amount of power converters. All

power converters are assumed to be isolated for guaranteeing all the four connection types, ideal and common-duty-ratio controlled.

Despite the existence of all two-port equivalent circuit representation, it is known that certain modular converter connections are not realizable theoretically. This is the case for classical DC/DC based converters in CCM for ISOS, exemplified in [8] and [10], or DAB-based for ISOP connection [2]. Usually, the explanations for not holding connection realization properties provided in the literature are based on simulation [2], [8] and [10], or through analysis of self-balance mechanism of the voltage across input capacitors [4], [8], [9] and [17], which may be unnecessary if considering ideal input and output voltage sources across their respective ports and dynamics are neglected, as presented assumed in this work. Besides, the characterization as "weak" or "strong" self-balancing [14] is generally used and seems to be not sufficiently defining.

Nevertheless, as it will be demonstrated, the interpretation of the two-port parameters seems to be easier, systematic, unifying and well defined. When observing the variables in Table I, it is interesting to classify them into two types: i) drifting variables meaning that, in occurrence of mismatches due to tolerance and precision, their values can drift from rated values, e.g. duty-ratio (D), inductance (L), and transformer turns ratio (a); ii) self-balancing variables, M, J, R_L. Particularly, the self-balancing variables of classical converters in DCM are expressed as a function of J and M, but can be expressed on its R_L dependence format [46].

As observed in [17], for OS connections, the parameters R_{L_j} (in which the subscript $j = 1,2 \dots N$ represents the jth DC/DC converter) is capable of converging into values where the total resistive load seen by the entire system, R_{L_T}, is equivalent to series association of each internal load resistance $\sum R_{L_j}$ as presented in (4.10) and depicted in *Figure 4.4*. Similarly, for OP connections, R_{L_T} is equivalent to the parallel association of each load resistance $1/\sum R_{L_j}{}^{-1}$ as presented in (4.11) and depicted in *Figure 4.5*. This capability of self-adjusting a given resistive load R_{L_j} seen by a given DC/DC converter is, therefore, an important property regarding connection realization.

$$R_{L_T} = \sum_{j=1}^{N} R_{L_j} \tag{4.10}$$

$$\frac{1}{R_{L_T}} = \sum_{j=1}^{N} R_{L_j}{}^{-1} \tag{4.11}$$

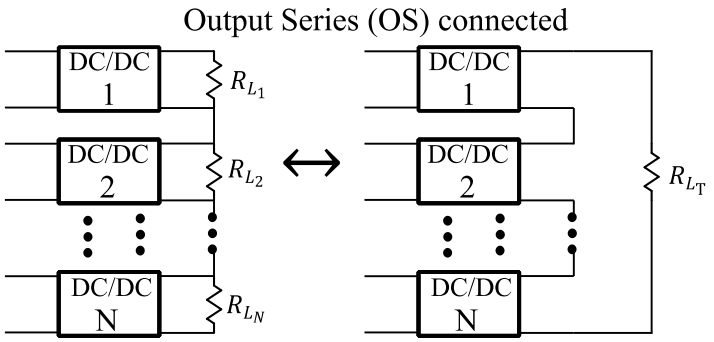


Figure 4.4 Equivalent circuit of an output series (OS) connected system.

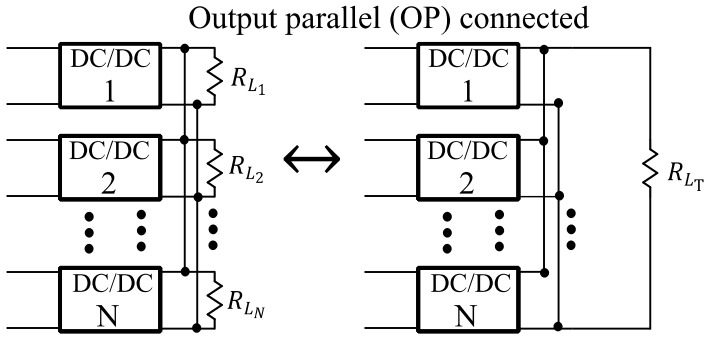


Figure 4.5 Equivalent circuit of an output parallel (OP) connected system.

The observation of the output characteristic of a converter has also been reported in [11], but it is only concluded for converters performing ISOS connection which are given by a loss-free behavior (M x $\overline{I_o}$), where $\overline{I_o}$ is the per-unity current. Indeed, such characteristic is important, as the dependence of the static gain with respect to an internal parameter J, and, therefore R_L, are implicitly necessary. Another observed output characteristic is the output-voltage drop characteristic found in [17], which also implicitly implies in a R_L static gain characteristic dependence. On the other hand, some converters as the classical ones in CCM do not hold the free-loss characteristics, yet their ISOP connection realization are verified in practice and theory, e.g. Buck-based in CCM [12].

In Table 4-II, it is presented the references showing successful connection realization for the aforementioned DC/DC converters. Observing Table 4-I and Table 4-II , it is possible to assume that, a unifying necessary condition for any lossless DC/DC converter common-duty-ratio controlled subjected to mismatch parameters is only successful if certain two-port network parameters are function of a given resistive load R_L, while observing rules provided in 4.1.3.1 and 4.1.3.2. Finally, in search for correlation and quicker results, a property defined as power invariance with respect to the connections are presented in 4.1.3.3.

Table 4-II Connectivity realization of ideal DC/DC power converters.

DC/DC Converter topology	***ISOS***	***IPOP***	***ISOP***	***IPOS***
Flyback – based all in DCM [7] [8] [9] [10] [11]	✓	✓	✓	✓
Buck, Boost or Flyback – based all in CCM [12], [14]	NA	NA	✓	✓
DAB – based (SPS) [2], [3], [4]	✓	✓	NA	NA

4.1.3.1 ISOS-IPOP Connection Realization

For ISOS or IPOP connections, a condition for its realization is observed through $\boldsymbol{G}$-representation: $\boldsymbol{G_j = G_{j-1}}$, as the necessary condition $M_j = M_{j-1} = V_o/V_i$ must be satisfied due to energy conservation, as observed in [10] [17] for ISOS connections. Such rule is easily proven by observing the connection in ISOS or IPOP using $\boldsymbol{G}$- parameters in *Figure 4.6*. Notice that current sources are in series, as ISOS shares the same input current $I_{1_j} = I_i$, yielding either $g_{12_j} = g_{12_{j-1}}$, or one module may process alone the entire power, and, consequently, runaway of voltage and currents, as observed in simulation results provided in [8] and [10]. For IPOP connection realization, similar condition is necessary, as ideal output voltage sources are in parallel $V_{2_j} = V_o$, yielding $g_{21_j} = g_{21_{j-1}}$ for correct functioning. A dual conclusion $\boldsymbol{H_j = H_{j-1}}$ is also implied, but it is omitted.

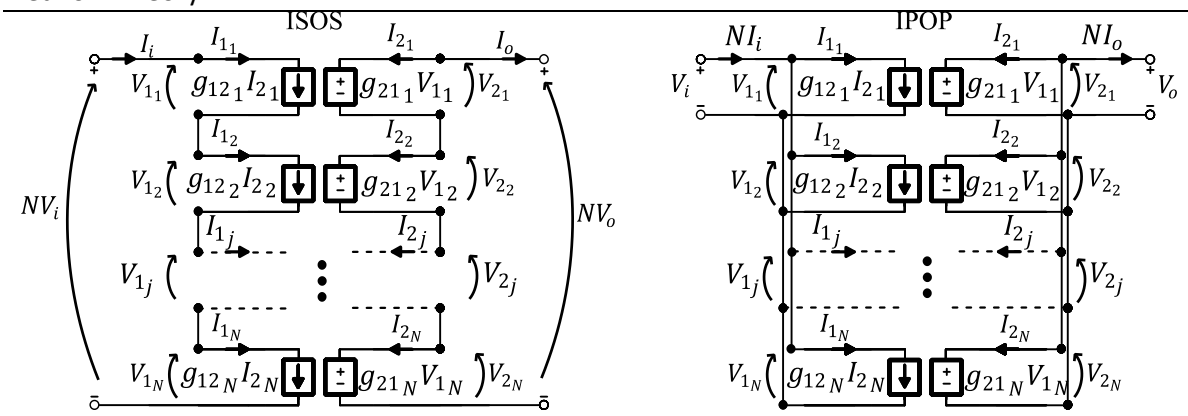


Figure 4.6 $\boldsymbol{G}$- Equivalent circuit representation for verifying connection realization regarding: (a) ISOS and (b) IPOP.

Observing the two-port parameters presented in *Table 4-I*, it is noticeable that the g-parameters of classical converters in CCM are dependent only on drifting variables, implying in unsuccessful realization of ISOS or IPOP in occurrence of mismatches, e.g. Flyback for ISOS connection [8]. On the other hand, the DAB as well as the classical converters in DCM will self-balance, since self-balancing variable dependence, R_L, is verified, and will converge into appropriated values so that the rule $\boldsymbol{G_j = G_{j-1}}$ is satisfied. In addition, the combination of only one in CCM and many associated in DCM when performing ISOS connection [10] can also perfectly co-exist under certain conditions as long as the aforementioned rule is verified. In such cases, the $\boldsymbol{G}$- parameters are imposed by the converter in CCM.

4.1.3.2 ISOP-IPOS Connection Realization

For ISOP connection realization, a condition for its realizations is observed through Y-representation: $\boldsymbol{Y_j = Y_{j-1}}$, as, due to energy conservation, the sum of the static gain of each subsystem, M_j, must be equal to the static gain of the entire system, M_T, that is, $\sum M_j = M_T$. Notice that, as presented in *Figure 4.7*, series association of ideal current sources in input ports and parallel association of ideal voltage sources across output ports yields either $y_{12_j} = y_{12_{j-1}}$, or one module may process alone the entire power and runaway of voltage or current are expected. The same conclusions for IPOS connection is observed as well as a dual conclusion $\boldsymbol{Z_j = Z_{j-1}}$.

Observing the $\boldsymbol{Y}$- parameters presented in *Table 4-ITable 2-I*, it is noticeable that the classical converters in both CCM and DCM, are all dependent on R_L. Such fact provides necessary condition for their connection realization. On the other hand, the DAB has its $\boldsymbol{Y}$-

parameters dependent on only drifting variables, occasioning unsuccessful connection realization [2] considering its lossless model.

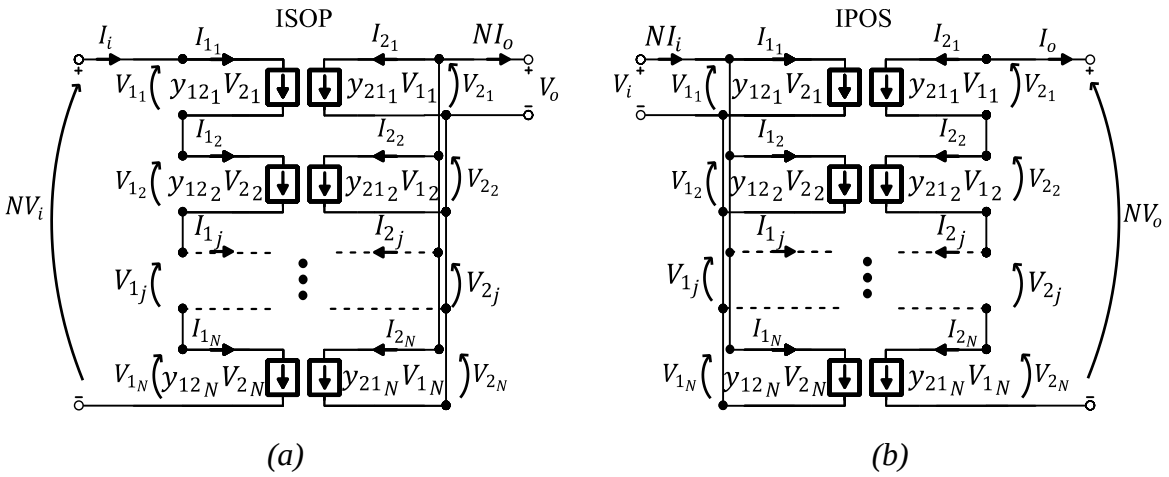


Figure 4.7 ***Y***- Equivalent circuit representation for verifying connection realization regarding: (a) ISOP; and (b) IPOP.

It is important to emphasize that the work here considers only ideal and, therefore, lossless cases and no parasitic elements such as leakage inductance or joule losses are taken into consideration. Eventually, the inclusion of parasitic resistances, not only stabilizes, but also balances more equally in the occurrence of mismatches [18] [19] [20] [21] [14]. They can even change the output characteristic of the converter, e.g. leakage inductance, which provides to Flyback in CCM a free-loss characteristic [11], enabling ISOS connection realization.

In the same directions, conventional modulation techniques are assumed in this work, whereas different ones may also modifies the output characteristic, as presented in [17] for a full-bridge which provides voltage drop through free-loss feature for both CCM and DCM, imposing a dependence on internal parameters, and, consequently, also enabling ISOS connection realization. Even though a lossless theory is assumed, it is easy to notice that the inclusion of loss resistance or conductance in the two-port network system implies in more degrees of liberty for connection realization, since non-ideal current and voltage sources can realize either series or parallel connections [20] [21] [14], which could explain why all four-connection realization of the DAB-based with SPS modulation are observed in [2] [3] [4] [5] [6].

Finally, even though the common-duty-ratio control has been assumed, the work here proposed can also be applied for individual-signal control, which must satisfy the same rules

with the advantage of acting on signal control pursuing equal power distribution and connectivity realization without the need of natural self-balance characteristic.

4.1.3.3 IS and IP Power Invariance Property

In the search of useful relationships among the many associations for better comprehension, it is defined a property named here as power or input current invariance:

"*A module converter is power or input current invariant if, in the presence of mismatches, power or input current is kept the same regardless of the connection configuration*".

The power invariance property for IS and IP are exemplified in *Figure 4.8* and *Figure 4.9*. Such property allows defining a link between ISOS-ISOP and IPOS-IPOP more easily. Regarding the DC/DC converters in DCM, a few simulation results, or more in depth analysis (for IP Flyback [7]), omitted here, may reveal that the Flyback holds power invariance for IS and IP connections; the Buck-based holds power invariance only for IS connections; and the Boost-based, only for IP.

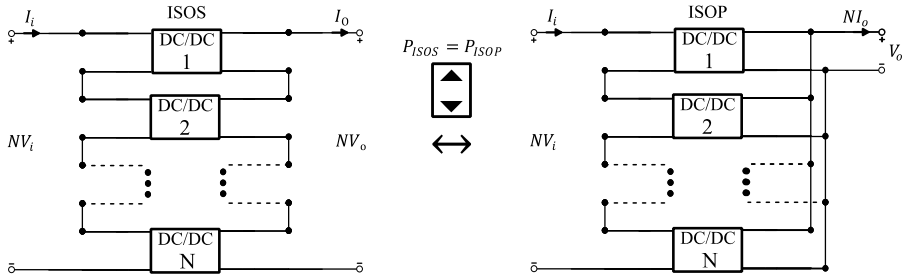


Figure 4.8 *IS power invariance property diagram (the power is kept the same regardless of the output connection).*

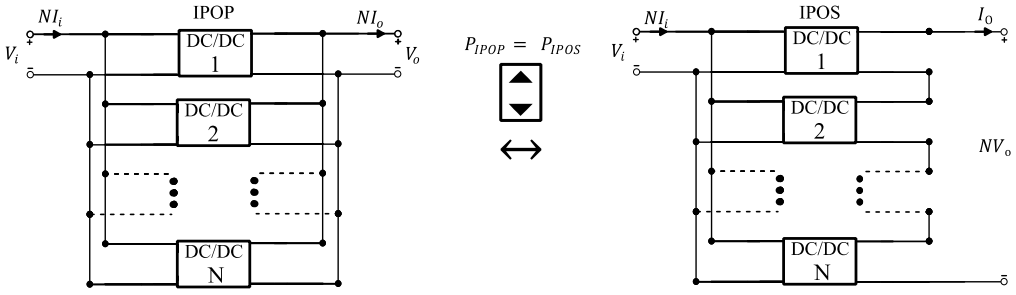


Figure 4.9 *IP power invariance property diagram (the power is kept the same regardless of the output connection).*

4.1.4 Synthesized two-port parameters of classical converters in DCM based and the DAB based in terms of external parameters

For imposed input and output voltage assumption, the two-port parameters have been presented as a function of internal parameters (M_j, J_j, R_{L_j}). Such fact defines, systematically, a useful comprehension of the variables through the four two-port parameters that eases the analysis and defines rules for any power converter. However, it is still possible to define them as a function of known parameters if, for each parameter, it is assumed its respective connection as presented in *Figure 4.1*: $\boldsymbol{Y_j}$ – IPOP; $\boldsymbol{Z_j}$ – ISOS; $\boldsymbol{G_j}$ – IPOS and $\boldsymbol{H_j}$ – ISOP.

In *Table 4-III*, , it is synthesized the two-port parameters in terms external parameters of those which hold connectivity realization and power invariance properties as previously discussed.

Table 4-III Synthesized two port-parameters of Classical- DCM and DAB- based in terms of external parameters.

DC/DC converter topology	$\boldsymbol{y_{12_j}}$	$\boldsymbol{z_{21_j}}$	$\boldsymbol{g_{21_j}}$	$\boldsymbol{h_{12_j}}$
Buck – based in DCM	$\frac{x_j K_o(1-M_o)}{M_o}$	$\frac{M_o}{x_j K_o(1-M_o)}$	X	$\frac{1}{+\frac{\left({M_o}^{-1}-1\right)N}{x_j \sum {x_j}^{-1}}}$
Boost – based in DCM	$\frac{x_j K_o}{M_o-1}$	$\frac{M_o-1}{x_j K_o}$	$\frac{1}{+\frac{x_j(M_o-1)N}{\sum x_j}}$	X
Flyback – based in DCM	$\frac{x_j K_o}{M_o}$	$\frac{M_o}{x_j K_o}$	$\frac{x_j M_o N}{\sum x_j}$	$\frac{1}{x_j M_o N \sum {x_j}^{-1}}$
DAB-based	$x_j K_o$	$\frac{1}{x_j K_o}$	X	X

They are in function of external variables:

- N, the number of modular converters, as previously mentioned;
- $M_o = V_o/V_i$, ideal rated static gain of a modular converter;
- Mismatch parameter $x_j = K_j/K_o$, for classical- based DC/DC converters in DCM or $x_j = {K_j}'/{K_o}'$, for DAB- based converters;

- $j = 1,2 \dots N$ is the jth modular converter.

They all have been confirmed through computer simulations, omitted here. In Appendix 4.A, it is presented the demonstration of the four two-port parameters of Flyback in DCM. A numerical illustration of a specific case, boost in DCM is presented Appendix 4.B. The reader is invited to demonstrate for boost- and buck- based converters, both in DCM, or others such as LLC, also very common in modular converter applications.

4.1.5 Synthesized unbalance and deviation parameters of classical converters in DCM and the DAB in terms of external parameters

The main goal remains to evaluate instantaneously the impact of mismatch on DC/DC converters. Once the steps so far presented are used as a tools to define the basis, it is possible to use it to evaluate the impact straightforwardly. For such task, it is defined the deviation parameter, u, presented in Table 4-IV, which defines the electric deviation from rated value:

- $u_{V_{1_j}} = V_{1_j}/V_i$;
- $u_{V_{2_j}} = V_{2_j}/V_o$;
- $u_{I_{1_j}} = I_{1_j}/I_i$;
- $u_{I_{2_j}} = -I_{2_j}/I_o$.

It is possible to study the behavior of the functions in *Table 4-IV*, and to conclude about the impact regarding the number of CSCs and mismatch parameters. In a general way for DC/DC converters, specifically for the DAB-based (ISOP and IPOS cannot be evaluated through lossless rules due to the aforementioned rules), it can be concluded that ISOS connections are impacted by the number of CSCs, whereas IPOP are not. This is due to the fact that for imposed voltage applications, each subsystem is independently working when connected IPOP. Notice that voltage and current sharing do not depend on the K_o parameter of the modular converters, but rather on its mismatch x_j; number of modular converters N; and the rated designed static gain M_o. This fact shows that unbalance effect and analysis are detached from power converter topology and circuit analysis, mainly for ISOS and IPOP systems.

Table 4-IV Synthesized deviation parameter ᴜ of Classical (in DCM)- and DAB- based DC/DC Converters.

Deviation Parameters	**Connection configuration**			
	ISOS	***IPOP***	***IPOS***	***ISOP***
$u_{V_{1_j}}$	$\frac{N}{x_j \sum x_j^{-1}}$	1	1	$h_{12_j} M_o$
$u_{V_{2_j}}$	$\frac{N}{x_j \sum x_j^{-1}}$	1	$\frac{g_{21_j}}{M_o}$	1
$u_{I_{1_j}}$	$\frac{N}{\sum x_j^{-1}}$	x_j	$\frac{g_{21_j} \sum x_j}{N M_o}$	$\frac{N}{\sum x_j^{-1}}$
$u_{I_{2_j}}$	$\frac{N}{\sum x_j^{-1}}$	x_j	$\frac{\sum x_j}{N}$	$\frac{N M_o}{\sum x_j^{-1}} h_{12_j}$

Another useful parameter, defined in [7], synthesized in Table 4-V, relates the voltage and current of each CSC within the total ratings input voltages and currents:

- $\bar{u}_{V_{1_j}} = \frac{V_{1_j}}{N V_i}$;
- $\bar{u}_{V_{2_j}} = \frac{V_{2_j}}{N V_o}$;
- $\bar{u}_{I_{1_j}} = \frac{I_{1_j}}{\sum I_{1_j}}$;
- $\bar{u}_{I_{2_j}} = \frac{I_{2_j}}{\sum I_{2_j}}$.

Such parameter is especially better appropriated for current unbalance measurement, since it relates internal parameters and reduces errors when comparing to practical results caused by losses.

Compared to the results in the literature, the equations provided in this work present the same results, but are easier to obtain, since it does not require circuit analysis; it is generalized, since it can be used to any DC/DC converter; and, finally, easier visualization. For comparison the parameter $\bar{u}_{I_{2_j}}$ is discussed in [7] for a an IP of Flyback in DCM; and it is expressed as presented in (4.12), being equivalent to expression presented in *Table 4-V*.

$$\bar{u}_{I_{2_j}} = \frac{1}{1 + \frac{L_j}{{d_j}^2} \sum_{\substack{k=1 \\ j \neq k}}^{N} \left(\frac{{d_k}^2}{L_k} \right)}. \tag{4.12}$$

Table 4-V Synthesized unbalance parameter $\bar{u}$ of Classical (in DCM)- and DAB- based DC/DC Converters.

Parameters	**Connection configuration**			
	ISOS	***IPOP***	***IPOS***	***ISOP***
$\bar{u}_{V_{1_j}}$	$\frac{1}{x_j \sum {x_j}^{-1}}$	N/A	N/A	$\frac{M_o h_{12_j}}{N}$
$\bar{u}_{V_{2_j}}$	$\frac{1}{x_j \sum {x_j}^{-1}}$	N/A	$\frac{g_{21_j}}{N M_o}$	N/A
$\bar{u}_{I_{1_j}}$	N/A	$\frac{x_j}{\sum x_j}$	$\frac{g_{21_j} \sum x_j}{\sum \left(g_{21_j} \sum x_j \right)}$	N/A
$\bar{u}_{I_{2_j}}$	N/A	$\frac{x_j}{\sum x_j}$	N/A	$\frac{\frac{h_{12_j}}{\sum {x_j}^{-1}}}{\sum \left(\frac{h_{12_j}}{\sum {x_j}^{-1}} \right)}$

4.1.6 Practical verification

The proposed work is generic, and validating it with practical results, even though it is important, for each case is challenging for only one person to do. Even though there is the possibility of choosing only one power converter to validate in practice the theory, the conclusions are still going to be limiting. Therefore, it was decided to make the validation with different references, power converters and connection configurations. It is important to understand that the conclusions of this work are theoretical and should not be limited to mainstream fashioned ways of proof of concepts in power electronics.

Main module prototype rated parameters, considering experiment condition [3] (DAB-based IPOP), [7] and [8] (Flyback IPOS and ISOS, respectively) are presented in Table 4-VI, and their experimental results in terms of absolute and relative voltage and current sharing are presented in *Table 4-VII*.

Table 4-VI Main module prototypes rated parameters presented to [3], [7], [8].

Symbol parameters	**Flyback (DCM) ISOS *N* = 3 [8]**	**Flyback (DCM) IPOS *N* = 3 [7]**	**DAB-based* IPOP *N* = 2 [3]**
V_i; V_o (V)	400; 200	200; 200	48; 200
P_o (W)	3000	200	432
V_{1T}; V_{2T} (V)	602; 598	200.66; 499.2	48; 200
$D_1 = D_2 = D_3$	0.35	0.40	0.33, 030
$a_1 = a_2 = a_3$	1.33:1	1:1	11:23
L_1; L_2; L_3 (µH)	65.7; 65.8; 64.4	392; 450; 382	12
C_i (µF)	2 x 220	3.03	1200
C_o (µF)	3 x 220	2.88	100
$f_1 = f_2 = f_3$ (kHz)	40	50	100

* K_o' previously provided for the DAB in SPS is adapted by multiplying it by 0.5 to take into account the Boost circuit according to the topology presented in [3].

Table 4-VII Main practical results presented in presented to [3], [7], [8].

Symbol parameters	**Flyback (DCM) ISOS *N* = 3 [8]**	**Flyback (DCM) IPOS *N* = 3 [7]**	**DAB-based* IPOP *N* = 2 [3]**
V_{1_1}; V_{1_2}; V_{1_3} (V)	202; 202; 198	200	48
V_{2_1}; V_{2_2}; V_{2_3} (V)	201; 201; 197	177.43; 146.27; 175.50	200
I_{1_1}; I_{1_2}; I_{1_3} (A)	4.99	0.76; 0.63; 0.76	4.56; 4.23
I_{2_1}; I_{2_1}; I_{2_3} (A)	-5.01	-0.825	-1.0; -1.0
$u_{V_{1_1}}; u_{V_{1_2}}; u_{V_{1_3}}$	0.505; 0.505; 0.495	1	1
$u_{V_{2_1}}; u_{V_{2_2}}; u_{V_{2_3}}$	1.005; 1.005; 0.985	0.89; 0.73; 0.88	1
$u_{I_{1_1}}; u_{I_{1_2}}; u_{I_{1_2}}$	0.66	0.76; 0.63; 0.76	1.013; 0.94
$u_{I_{2_1}}; u_{I_{2_2}}; u_{I_{2_3}}$	0.33	0.825	1; 1
$\bar{u}_{V_{1_1}}; \bar{u}_{V_{1_2}}; \bar{u}_{V_{1_3}}$	0.333; 0.333; 0.333	N/A	N/A

$\bar{u}_{V_{2_1}}; \bar{u}_{V_{2_2}}; \bar{u}_{V_{2_3}}$	0.333; 0.333; 0.333	0.35; 0.29; 0.35	N/A
$\bar{u}_{I_{1_1}}; \bar{u}_{I_{1_2}}; \bar{u}_{I_{1_3}}$	N/A	0.34 ; 0.30; 0.35	0.519; 0.481
$\bar{u}_{I_{2_1}}; \bar{u}_{I_{2_2}}; \bar{u}_{I_{2_3}}$	N/A	N/A	0.50; 0.50

* Ko' previously provided for the DAB in SPS is adapted by multiplying it by 0.5 to take into account the Boost circuit according to the topology presented in [3].

As previously mentioned, the important parameter to evaluate the unbalance is the mismatch parameter x_j, that are generated from *Table 4-VI*. The synthesized deviation and unbalance parameter can then be derived using *Table 4-IV* and *Table 4-V*. The absolute values can also be calculated as shown in the end of the Illustrative example Appendix 4.B. This process can be used to generated the unbalance performance of the Flyback DCM ISOS and IPOS as well as the DAB-based IPOP system, which results are presented in *Table 4-VIII*. Besides, simulation results, omitted here, were compared to analytical results, resulting in error inferior to 1%, verifying once again the correctness of equations.

Table 4-VIII Theoretical results using proposed two-port network theory.

Symbol parameters	**Flyback (DCM) ISOS N = 3 [8]**	**Flyback (DCM) IPOS N = 3 [7]**	**DAB-based* IPOP N = 2 [3]**
V_{1_1}; V_{1_2}; V_{1_3} (V)	202; 202.3; 198	200.66	48
V_{2_1}; V_{2_2}; V_{2_3} (V)	200.7; 201; 196.8	172.3; 150.1; 176.81	200
I_{1_1}; I_{1_2}; I_{1_3} (A)	4.71	0.81; 0.71; 0.84	4.41; 4.19
I_{2_1}; I_{2_1}; I_{2_3} (A)	-4.74	-0.95	-1.06; -1.00
$u_{V_{1_1}}; u_{V_{1_2}}; u_{V_{1_3}}$	0.505; 0.506; 0.495	1	1
$u_{V_{2_1}}; u_{V_{2_2}}; u_{V_{2_3}}$	1.004; 1.012; 0.99	0.86; 0.75; 0.88	1
$u_{I_{1_1}}; u_{I_{1_2}}; u_{I_{1_2}}$	0.628	0.81; 0.71; 0.84	0.98; 0.93
$u_{I_{2_1}}; u_{I_{2_2}}; u_{I_{2_2}}$	0.316	-0.95	1.06; 1
$\bar{u}_{V_{1_1}}; \bar{u}_{V_{1_2}}; \bar{u}_{V_{1_3}}$	0.335; 0.336; 0.329	N/A	N/A
$\bar{u}_{V_{2_1}}; \bar{u}_{V_{2_2}}; \bar{u}_{V_{2_3}}$	0.335; 0.336; 0.329	0.34; 0.30; 0.35	N/A

$\bar{u}_{I_{1_1}}; \bar{u}_{I_{1_2}}; \bar{u}_{I_{1_3}}$	N/A	0.34; 0.30; 0.35	0.513; 0.487
$\bar{u}_{I_{2_1}}; \bar{u}_{I_{2_2}}; \bar{u}_{I_{2_3}}$	N/A	N/A	0.513; 0.487

The relative error of voltage and current sharing values between computer simulation and analytical results are all below 1% for all cases. The relative errors between analytical and practical results of absolute value of voltage sharing in series connections are below 0.6% and 4.2% for [8] and [7], respectively, whereas the relative errors of absolute current sharing of all cases relative errors are below 8%, 21% and 5.8% for [8], [7] and [3], respectively. An error more important of current values is due to the fact that the theory is based on imposed voltages, while current is in function of a lossless system. In reality, the efficiency should be accounted for improving the accuracy. This fact does not undervalue the proposed work, simply because a lossless theory is studied. Indeed a simple fitting considering expect efficiency may be enough to reduce such error.

Indeed, if the unbalance measures are the concerning objective, the use of the parameters in [7] $\bar{u}_{I_{1,2}{}_j}$ are suggested. In this case, the relative error between analytical and practical results were kept below 4.4%. The current sharing of each module in practice can be inferred by combining the known measured current with the theoretical unbalance parameter.

Another interesting and relevant verification is that, using ideal theoretical cases (without loss) as a reference can provide conservative estimates for the maximum and minimum values in a system. This is because, the losses soften the impact of mismatch. As sensibility of semiconductor devices are mostly impacted by peak voltage, the approach presented in this work can quickly deliver precise results as for both their relative and absolute values.

4.1.7 Partial conclusions and perspectives

In conclusion, a general transformation based on two-port network theory has been proposed as a means to simplify the analysis of any ideal power converter in modular converter systems when subjected to mismatches. The method utilizes four two-port network parameters to observe and satisfy necessary connection realization conditions. This approach offers a unified and systematic and analytic way to analyze many power converters and their connection configurations. The main benefit of this method is to improve the fundamentals of power electronic education through the abstraction of two-port network theory, rather than

improving mainstream performance of power electronics. Through simple use of the approach, it is possible to observe that the mismatch impact can be detached from the converter topology, avoiding unnecessary electric circuit analysis.

An interesting property, power invariance to connection, not yet explicitly discussed in the literature is used to facilitate the correlation among connections. Besides, this work also includes buck and boost-based DCM converters subjected to mismatch not previously treated in literature, due to the unifying and simple characteristic.

Future steps include using this method to evaluate statistical and sensitivity parameters with respect to the number of modular converters and different distributions, such as Gaussian distributions. This can provide a better understanding of the expected performance of the system and help identify potential issues that may arise due to mismatch.

Other steps includes the inclusion of resistance for self-balance in modular converters, and studying the inclusion of imaginary parts and cascaded input/output filters for stability of modular converters. Indeed, with respect to control theory, it is easy to see that by considering the transfer functions dependent on steady state sharing automatically solved in this work can improve the accuracy of control aspects.

Finally, the parameter extraction for input and output current or power imposed applications can follow the same principle and results. Functions that are dual to voltage imposed application provided here may exist, but it is left for future studies.

4.2 A Two-Port Network Based Transformation for Resistive DAB Model

In this section, the analysis already performed in *Chapter 2* is now used to apply the definition of two-port network directly without problem of singularity. Besides, as it will be demonstrated and discussed, the impact of mismatches on efficiency, voltage, current and power sharing are different with respect to the connection configuration, having it worsen for ISOP and IPOS connection configuration. Indeed, as already discussed in previous section, the DAB-based converters cannot ideally be connected in ISOP or IPOS. This might indicate problems of efficiency. Other reasons, related to the static gain of each converter, show an important impact as it will be later discussed.

4.2.1 Definition

From the analysis presented in Section 2.2 in *Chapter 2*, the input and output currents functions are recalled in (4.13) and (4.14) , respectively. For notation purposes, the currents are adopted as $I_i, I_o = I_1, -I_2$, as previous section.

$$I_1 = V_i \frac{Q}{2\pi f_s L_{ac}} \left[1 + M \left(2d + \frac{2Q}{\pi} \left(1 - \operatorname{sech}\left(\frac{\pi}{2Q}\right) e^{\frac{-\pi(1-2d)}{2Q}} \right) - 1 \right) - \frac{2Q}{\pi} \tanh\left(\frac{\pi}{2Q}\right) \right] \tag{4.13}$$

$$I_2 = -V_i \frac{Q}{2\pi f_s L_{ac}} \left[1 - 2d + \frac{2Q}{\pi} \left(1 - \operatorname{sech}\left(\frac{\pi}{2Q}\right) e^{\frac{\pi(1-2d)}{2Q}} \right) + M \left(\frac{2Q}{\pi} \tanh\left(\frac{\pi}{2Q}\right) - 1 \right) \right]. \tag{4.14}$$

The impedance matrix can easily be found through the definitions recalled from the literature in (4.15). Due to open circuit condition existence already presented in *Chapter 2*, it is possible to express the input or output currents when the output or input current are equal to zero.

$$\boldsymbol{Z} = \begin{pmatrix} z_{11} = \dfrac{V_1}{I_1}\Big|_{I_2=0} & z_{12} = \dfrac{V_1}{I_2}\Big|_{I_1=0} \\ z_{21} = \dfrac{V_2}{I_1}\Big|_{I_2=0} & z_{22} = \dfrac{V_2}{I_2}\Big|_{I_1=0} \end{pmatrix} \tag{4.15}$$

- z_{11} and z_{21} extractions: I_2 is equaled to 0 in (4.14), and the resulting static gain, $M_{I_2=0}$ in (4.17), is substituted in (4.13). Then z_{11} and z_{21} are, respectively, found dividing V_i and $M_{I_2=0} \times V_i$ over the aforementioned manipulation;
- z_{12} and z_{22} extraction: I_1 is equaled to 0 in (4.13), and the resulting static gain, $M_{I_1=0}$ in (4.16), is substituted in (4.14). Then z_{21} and z_{12} are, respectively, found dividing V_i and $M_{I_1=0} \times V_i$ over the aforementioned manipulation.

$$M_{I_1=0} = \frac{1 - \dfrac{2Q}{\pi} \tanh\left(\dfrac{\pi}{2Q}\right)}{1 - 2d + \dfrac{2Q}{\pi} \left(1 - \operatorname{sech}\left(\dfrac{\pi}{2Q}\right) e^{\frac{-\pi(1-2d)}{2Q}} \right)} \tag{4.16}$$

$$M_{I_2=0} = \frac{1 - 2d + \frac{2Q}{\pi}\left(1 - \operatorname{sech}\left(\frac{\pi}{2Q}\right) e^{\frac{\pi(1-2d)}{2Q}}\right)}{1 - \frac{2Q}{\pi}\tanh\left(\frac{\pi}{2Q}\right)}. \tag{4.17}$$

The complete $\boldsymbol{Z}$ -matrix is presented in (4.18)

$$\boldsymbol{Z} = \frac{2\pi f_s L_{ac}}{Q}\begin{pmatrix} \frac{1}{U} & \frac{-1}{W} \\ \frac{M_{I_2=0}}{U} & \frac{-M_{I_1=0}}{W} \end{pmatrix}. \tag{4.18}$$

Where U and W are given by (4.19) and (4.20), respectively.

$$U = 1 - \frac{2Q}{\pi}\tanh\left(\frac{\pi}{2Q}\right) + M_{I_2=0}\left(2d + \frac{2Q}{\pi}\left(1 - \operatorname{sech}\left(\frac{\pi}{2Q}\right) e^{\frac{-\pi(1-2d)}{2Q}}\right) - 1\right) \tag{4.19}$$

$$W = 1 - 2d + \frac{2Q}{\pi}\left(1 - \operatorname{sech}\left(\frac{\pi}{2Q}\right) e^{\frac{\pi(1-2d)}{2Q}}\right) + M_{I_1=0}\left(\frac{2Q}{\pi}\tanh\left(\frac{\pi}{2Q}\right) - 1\right). \tag{4.20}$$

In order to find the other two-port network matrices, the Z-matrix can be transformed through ordinary two-port network theory into any other matrix useful for analyzing the many connection configurations Since the $\boldsymbol{Z}$-parameters was previously extracted, the transformation to $\boldsymbol{T}$- and $\boldsymbol{G}$- and their respective inverse transformation are recalled from literature and presented from (4.21)-(4.24). They will be used when convenient. The simple inverse matrix of $\boldsymbol{Z}$- and $\boldsymbol{G}$- defines $\boldsymbol{Y}$ and $\boldsymbol{H}$. As it can be seen, due to losses, the properties and transformation of two-port network theory can be used without problems of singularities.

$$\boldsymbol{Z} \to \boldsymbol{T} = \frac{1}{z_{21}}\begin{pmatrix} z_{11} & \det(\boldsymbol{Z}) \\ 1 & z_{22} \end{pmatrix} \tag{4.21}$$

$$\boldsymbol{T} \to \boldsymbol{Z} = \frac{1}{c}\begin{pmatrix} \mathrm{a} & \det(\boldsymbol{T}) \\ 1 & \mathrm{d} \end{pmatrix} \tag{4.22}$$

$$\boldsymbol{Z} \to \boldsymbol{G} = \frac{1}{z_{11}}\begin{pmatrix} 1 & -z_{12} \\ z_{21} & \det(\boldsymbol{Z}) \end{pmatrix} \tag{4.23}$$

$$\boldsymbol{G} \to \boldsymbol{Z} = \frac{1}{g_{11}}\begin{pmatrix} 1 & -g_{12} \\ g_{21} & \det(\boldsymbol{G}) \end{pmatrix} \tag{4.24}$$

Also, as the experimental results might be conducted with resistive load, the quadrupole voltage gain, recalled in (4.25), can be used. Indeed, it is a collapsing of a two-port into a simple one-port impedance

$$M = \frac{Z_{21}}{Z_{11}\dfrac{\det(\boldsymbol{Z})}{R_L}}. \tag{4.25}$$

4.2.2 Brief introduction to properties

To make some properties visible, a simple numerical example is given, and then discussed. Let's define for a given DAB converter Q = 4.5; L_{ac} = 2.17 µH; d = 0.066; fs = 100 kHz resulting in (4.26).

$$\boldsymbol{Z} = \begin{pmatrix} 6.566 & -0.615 \\ 13.416 & 6.566 \end{pmatrix} \tag{4.26}$$

The main observations are highlighted:

- $z_{11} = z_{22}$ for any generic case. This reduces one step when extracting the Z-parameters of the DAB, previously presented, opting for one or another;
- It also does not hold the reciprocity property since $z_{11} \neq z_{22}$, typically characterizing as a non-linear and non-passive circuit.

Another interesting analysis to make, is to observe the lossless case (large values for Q), which results in the following $\boldsymbol{Z}$-matrix as presented in (4.27).

$$\lim_{Q\to\infty}(Z) = \begin{pmatrix} 0 & -\dfrac{1}{y_{12}} = -\dfrac{1}{K_o{}'} \\ \dfrac{1}{y_{12}} = \dfrac{1}{K_o{}'} & 0 \end{pmatrix} = \begin{pmatrix} 0 & -7.02 \\ 7.02 & 0 \end{pmatrix}. \tag{4.27}$$

As it can be seen, when observing through the limit equation, they result as in lossless case, yielding harmony and correctness among the proposed methods. Therefore, as

previously mentioned, it is classified as a gyrator, where the off diagonals are called gyration resistance.

The property were verified simply numerically. However, more properties and their interpretations certainly exist and could be useful for the analysis of the DAB and modular converters made of DABs in general, or be applied for other power converters. Nevertheless, they are enough for conducting investigations regarding the subject of this thesis.

4.2.3 Straightforward algorithm for faster solution

In summary, the algorithm is based in three steps:

- The matrix representation of each connection type is used and added together, as presented in *Figure 4.2*, with the known input and output voltages;
- The sum is then transformed into the $\boldsymbol{Y}$- matrix (or $\boldsymbol{Z^{-1}}$) and multiplied by the voltage vector to find the total input and output currents. This information can then be used to determine other electrical parameters;
- Adding another step, by considering a feedback system to keep not only output voltage, but also output current constant, can be performed numerically by finding the phase-shift, $\hat{d}$, that satisfies such imposed condition. Such phase-shift must be inputted in first step.

These steps can be applied for ISOS in (4.28)-(4.30); ISOP in (4.31)-(4.33), IPOP in (4.34)-(4.36) and IPOS in (4.37)-(4.39).

4.2.3.1 ISOS

$$\begin{pmatrix} I_{1\mathrm{T}} \\ I_{2\mathrm{T}} \end{pmatrix} = \left(\sum \mathbf{Z_j}\right)^{-1} \begin{pmatrix} NV_{\mathrm{i}} \\ NV_{\mathrm{o}} \end{pmatrix} \tag{4.28}$$

$$\begin{pmatrix} V_{1_j} \\ V_{2_j} \end{pmatrix} = \mathbf{Z_j} \begin{pmatrix} I_{1\mathrm{T}} \\ I_{2\mathrm{T}} \end{pmatrix} \tag{4.29}$$

$$\hat{d} = root\left\{-I_{\mathrm{o}} - \left[NV_{\mathrm{i}}\left(\left(\sum \mathbf{Z_j}\right)^{-1}\right)_{21} + NV_{\mathrm{o}}\left(\left(\sum \mathbf{Z_j}\right)^{-1}\right)_{22}\right]\right\} \tag{4.30}$$

4.2.3.2 ISOP

$$\begin{pmatrix} \mathrm{I}_{1T} \\ \mathrm{I}_{2T} \end{pmatrix} = \left(\left(\sum \mathbf{G_j}^{-1} \right) \rightarrow \mathbf{Z_j} \right)^{-1} \begin{pmatrix} NV_i \\ V_o \end{pmatrix} \tag{4.31}$$

$$\begin{pmatrix} V_{1_j} \\ I_{2_j} \end{pmatrix} = \mathbf{G_j}^{-1} \begin{pmatrix} I_{1T} \\ V_o \end{pmatrix} \tag{4.32}$$

$$\begin{aligned} \hat{d} = root \Bigg\{ & -NI_{\mathrm{o}} \\ & - \left[NV_{\mathrm{i}} \left(\left(\left(\sum \mathbf{G_j}^{-1} \right) \rightarrow \mathbf{Z_j} \right)^{-1} \right)_{21} + V_{\mathrm{o}} \left(\left(\left(\sum \mathbf{G_j}^{-1} \right) \rightarrow \mathbf{Z_j} \right)^{-1} \right)_{22} \right] \Bigg\} \end{aligned} \tag{4.33}$$

4.2.3.3 IPOP

$$\begin{pmatrix} \mathrm{I}_{1T} \\ \mathrm{I}_{2T} \end{pmatrix} = \sum \mathbf{Z_j}^{-1} \begin{pmatrix} V_i \\ V_o \end{pmatrix} \tag{4.34}$$

$$\begin{pmatrix} I_{1_j} \\ I_{2_j} \end{pmatrix} = \mathbf{Z_j}^{-1} \begin{pmatrix} V_i \\ V_o \end{pmatrix} \tag{4.35}$$

$$\hat{d} = root \left\{ -NI_{\mathrm{o}} - \left[V_{\mathrm{i}} \left(\sum \mathbf{Z_j}^{-1} \right)_{21} + V_{\mathrm{o}} \left(\sum \mathbf{Z_j}^{-1} \right)_{22} \right] \right\} \tag{4.36}$$

4.2.3.4 IPOS

$$\begin{pmatrix} \mathrm{I}_{1T} \\ \mathrm{I}_{2T} \end{pmatrix} = \left(\left(\sum \mathbf{G_j} \right) \rightarrow \mathbf{Z_j} \right)^{-1} \begin{pmatrix} V_i \\ NV_o \end{pmatrix} \tag{4.37}$$

$$\begin{pmatrix} I_{1_j} \\ V_{2_j} \end{pmatrix} = \mathbf{G_j} \begin{pmatrix} V_i \\ \mathrm{I}_{2T} \end{pmatrix} \tag{4.38}$$

$$\hat{d} = root \left\{ -I_{\mathrm{o}} - \left[V_{\mathrm{i}} \left(\left(\left(\sum \mathbf{G_j} \right) \rightarrow \mathbf{Z_j} \right)^{-1} \right)_{21} + NV_{\mathrm{o}} \left(\left(\left(\sum \mathbf{G_j} \right) \rightarrow \mathbf{Z_j} \right)^{-1} \right)_{22} \right] \right\} \tag{4.39}$$

4.2.4 Numerical example and Discussions

To conclude over the impact of mismatch on the DAB, a cell DAB with their main rated parameters are presented in *Table 4-IX*, as an illustrative, but still representative case is evaluated. Three different types of CSCs, in which the AC inductance was mismatched from the rated value are named and defined as:

- CSC "a" contains L_{ac} = 1.44 μH;
- CSC "b" contains L_{ac} = 2.17 μH;
- CSC "b" contains L_{ac} = 2.9 μH;

For simplifying purposes, only AC-link inductances are mismatched from rated value presented in *Table 4-IX*. Such assumption assumes that the AC-link resistances are proportional to the AC-link inductance, in such a way that the quality factor Q maintains unaltered. Through previous algorithm presented in *4.2.3*, without the imposed output current step, it is generated the static results of a system composed of a pair of CSCs of each type, totalizing six. All connection configuration types are evaluated in *Table 4-X*.

Table 4-IX Theoreical parameters of rated value of one DAB CSC.

Symbol parameters	**ISOS**
V_i (V)	15
V_o (V)	15
M	1.0
I_i (A)	2.1
I_o (A)	2.0
P_o (W)	30
η (%)	95.4
f_s (kHz)	100
L_{ac} (μH)	2.17
d (degree)	12
Q	4.5
γ	0.058

Table 4-X Analytical results of a modular converter containing CSCs "a", "b" and "c".

Symbol parameters	**ISOS**	**IPOP**	**ISOP**	**IPOS**
V_{1_a}; V_{1_b}; V_{1_c} (V)	10.6; 15; 19.4	15; 15; 15	10.16; 15; 19.8	15; 15; 15
V_{2_a}; V_{2_b}; V_{2_c} (V)	10.6; 15; 19.4	15; 15; 15	15; 15; 15	19.6; 15; 10.38
I_{1_a}; I_{1_b}; I_{1_c}; I_{1T} (A)	2.10	2.97; 2.1; 1.62; 13.38	2.10	3.05; 2.1; 1.58; 13.45
I_{2_a}; I_{2_b}; I_{2_c}; I_{2T} (A)	-2.0	-2.84; -2.0; 1.54; -12.76	-1.04; -2; -2.52 -11.13	-2.0
P_{1_a}; P_{1_b}; P_{1_c}; P_{1T} (W)	22.2; 31.4; 40.7; 188.7	44.6; 31.4; 24.3; 200.71	21.3; 31.4; 41.6; 188.7	44.8; 31.4; 23.65; 201.78
P_{2_a}; P_{2_b}; P_{2_c}; P_{2T} (W)	21.15; 30.0; 38.8; 180.0	42.55; 30; 23.17; 191.43	15.6; 30; 37.8; 167	39.3; 30.0; 20.77; 180.0
η_a; η_b; η_c; η_T (%)	95.4	95.4	73.5; 95.4; 91; 88.5	85.7; 95.4; 87.8 89.2
$u_{V_{1_a}}; u_{V_{1_b}}; u_{V_{1_c}}$	0.7; 1; 1.3	1	0.68; 1; 1.32	1
$u_{V_{2_a}}; u_{V_{2_b}}; u_{V_{2_c}}$	0.7; 1; 1.3	1	1	1.31; 1; 0.69
$u_{I_{1_a}}; u_{I_{1_b}}; u_{I_{1_c}}$	1	1.42; 1; 0.77	1	1.45; 1; 0.75
$u_{I_{2_a}}; u_{I_{2_b}}; u_{I_{2_c}}$	1	1.42; 1; 0.77	0.52; 1; 1.32	1
$\overline{u_{V_{1_a}}}; \overline{u_{V_{1_b}}}; \overline{u_{V_{1_c}}}$	0.12; 0.17; 0.21	X	0.11; 0.17; 0.22	X
$\overline{u_{V_{2_a}}}; \overline{u_{V_{2_b}}}; \overline{u_{V_{2_c}}}$	0.12; 0.17; 0.21	X	X	0.22; 0.17; 0.11
$\overline{u_{I_{1_a}}}; \overline{u_{I_{1_b}}}; \overline{u_{I_{1_c}}}$	X	0.22; 0.16; 0.12	X	0.23; 0.15; 0.12
$\overline{u_{I_{2_a}}}; \overline{u_{I_{2_b}}}; \overline{u_{I_{2_c}}}$	X	0.22; 0.16; 0.12	0.1; 0.18; 0.22	X
M_a; M_b; M_c	1	1	1.47; 1.0; 0.75	1.31; 1.0; 0.70
γ_a; γ_b; γ_c	0.053	0.058	0.03; 0.06; 0.07	0.04; 0.06; 0.075

σ_a; σ_b; σ_c (10^3)	1.61, 1.14, 0.80	1.61, 1.14, 0.80	0.88; 1.14; 1.08	0.87; 1.14; 1.64

Regarding ISOS connection configuration, it is interesting to notice that efficiency, static gain and γ are kept the same for each cell, a specific characteristics inherited from ISOS connections. Meanwhile, as the sharing in input voltage are not equal, the value of σ will be shared accordingly to their voltage across their input ports. This means that cells with decreased L_{ac} (Cell "a") are more likely to perform ZVS, while the cells with larger L_{ac} (Cell "c") are less likely to perform it. Adding another step, by considering a feedback system to keep not only output voltage, but also output power constant, it is possible to have a more fair comparison. Numerically or through control in a simulation, the phase-shift is changed to deliver constant output current at I_2 = -2.5 A through the third step. By varying the distribution, the total efficiency will dependent of course on the static gain, giving better results for the combination N_a = 4, N_b = 1 and N_c = 1. One should notice that a static gain different from unitary will not result likewise. An important conclusion regarding voltage sharing is that, the distribution with more smaller L_{ac} is the one that results in larger voltage across cells with larger L_{ac}.

Observing ISOP and ISOS connections holds input power invariance property, meaning that the input currents are the same. In addition, the input voltage and power sharing are kept almost the same as well. On the other hand, a very important parameter that interferes on efficiency and EMI noise, the static gain, is highly altered. The conclusion is that ISOP connections can be more harmful in terms of efficiency and EMI signature than ISOS connection.

For IPOP, notice that the efficiency and static gain are kept the same as the ISOS case, as static gain and phase-shift are kept unaltered! On the other hand, slightly more power is delivered. By reducing the phase-shift and applying the condition (3.27), it is possible to notice a small increase in the efficiency, due to the imposed unitary static gain. The distribution that brings largest mismatch for the input and output currents is (N_a, N_b, N_c) = (1, 1, 4). It is interesting to notice that the IPOP configuration, due to the imposed voltage is indeed the most stable connection.

For IPOS, notice that in this example, the IPOS and ISOS have the output power invariant, while IPOS and IPOP have practically same input power. Such information on power and/or current invariance is useful to get information easily and correlation among the many connections.

4.2.5 Partial conclusion and perspectives

As it can be seen, when considering the resistance, the mathematic analysis require less abstraction level, since the transformation into other equivalent circuits can be easily performed out of the extraction of only $\boldsymbol{Z}$- parameters. That is, from the analytically extracted $\boldsymbol{Z}$-parameters, it is possible to transform into other two-port network equivalent circuit representation to analyze other connection configurations, including cascaded systems. When the input and output voltages are imposed, the IPOP configuration is the "easiest" and natural one since each sub-system works independently, and finding the impact on current sharing can easily be performed. Based on this, it is preferred and proposed an algorithm for faster resolution, by transforming into $\boldsymbol{Y}$-, or $\boldsymbol{Z^{-1}}$- the equivalent $\sum \boldsymbol{Z_j}$, $\sum \boldsymbol{G_j}$ and $\sum \boldsymbol{H_j}$ and later solving simple matrix equations. If output current is also imposed, the conditioning equation is presented for each connection configuration, resulting in the phase-shift needed to reach it.

Therefore, the analysis of mismatch in a muti-cell power converter made of DAB cells can be performed through matricidal equations in a straightforward manner. Regarding the impact on efficiency, it is verified that IPOS and ISOP are indeed more negatively impacted by the mismatch.

The use of a generic $\boldsymbol{T}$-, equivalent representation cascaded (matrix multiplication) of input and output impedances, presented in Appendix 4.C, allowed the brief discussion on short-circuit, and how such tool can be used to better understand the mechanism of fault tolerance and redundancy in multi-cellconverters.

4.3 Experimental results

Experimental results were performed by forcing a change in AC-link inductance. As it was shown in *Chapter 2*, the third version of the DAB cell is composed of 4 inductors, split symmetrically over the AC-link. The idea was then to perform short-circuits across certain inductances in order to generate other CSCs and, therefore, changing the value of AC-link inductance. One cell is unmodified, two cells were modified by: (i) short-circuiting one inductor; (ii) short-circuiting two inductors. Combining the three types of cells, it is then possible to perform tests to verify the effect of mismatching among inductances in an easy way. They are then named as the illustrative example presented in *4.2.4*: CSC "a", for the CSC containing 2 inductors (equivalent L_{ac} = 1.44 uH); CSC "b", for the CSC containing 3 inductors (equivalent L_{ac} = 2.17 uH); and CSC "c", for the CSC containing 4 inductors

(equivalent L_{ac}= 2.9 uH). The experimental results emulate an extreme case of tolerance in the order -50% and +25%. A pair of each type is used then tested, totalizing 6 CSCs at total, and tests of IPOS (*4.3.1*) and ISOP (*4.3.2*) are conducted. The input and output voltage across each CSC were measured, and the currents through the AC-link of one of each type of CSCs were captured though oscilloscope. Thermographic pictures were taken for additional and valuable information.

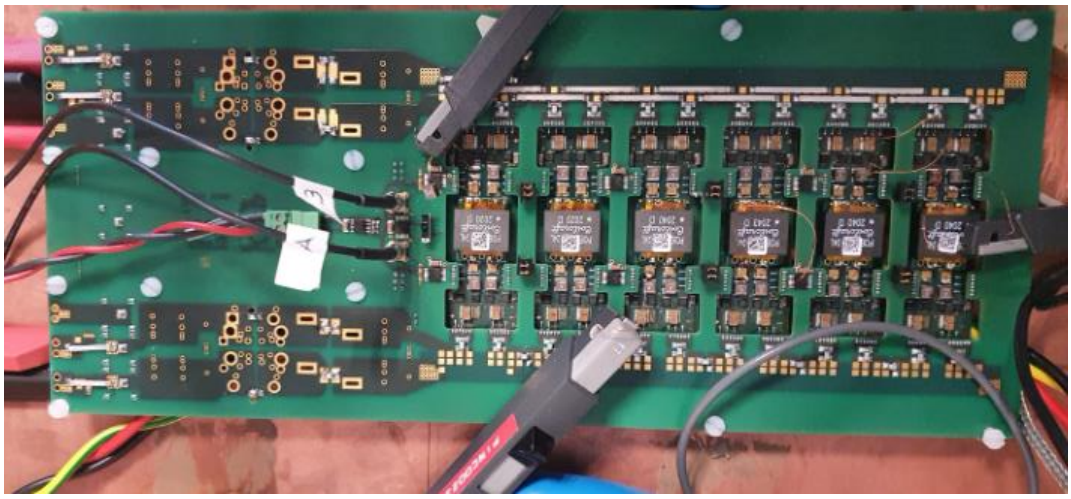


Figure 4.10 Prototyped (PCA 3.0) used for conducting the experimental results: the CSCs are mismatched by short-circuiting one or two ac-link inductors.

4.3.1 IPOS

4.3.1.1 Varying output current and keeping output voltage constant at 90 V.

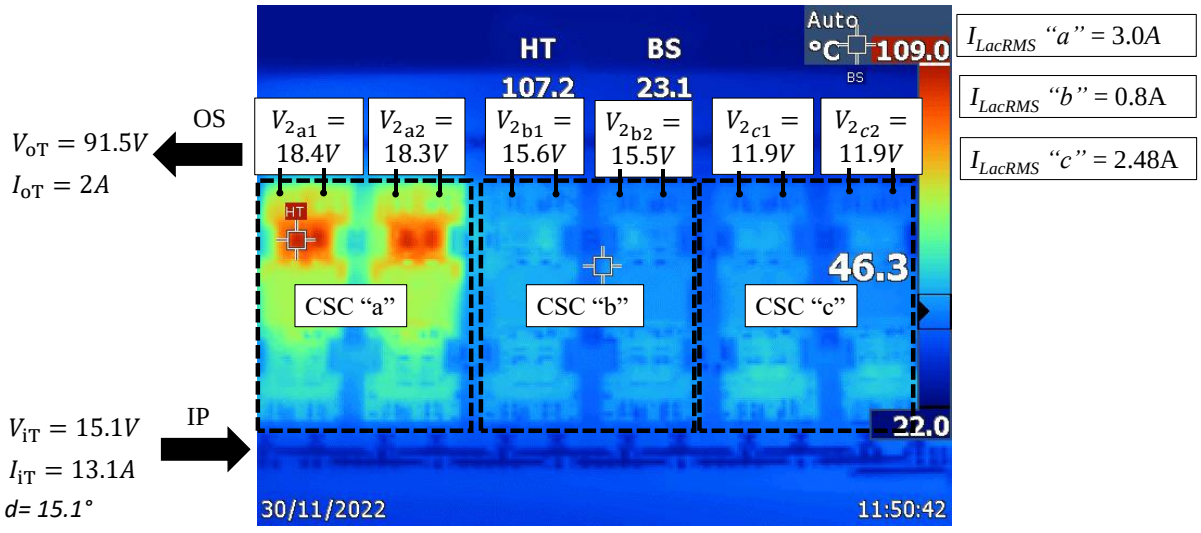


Figure 4.11 Experimental results of DC- voltages across the PCA (IPOS) V_i = 15 V; V_o = 90 V; I_o = 2.0 A. Thermographic picture is depicted.

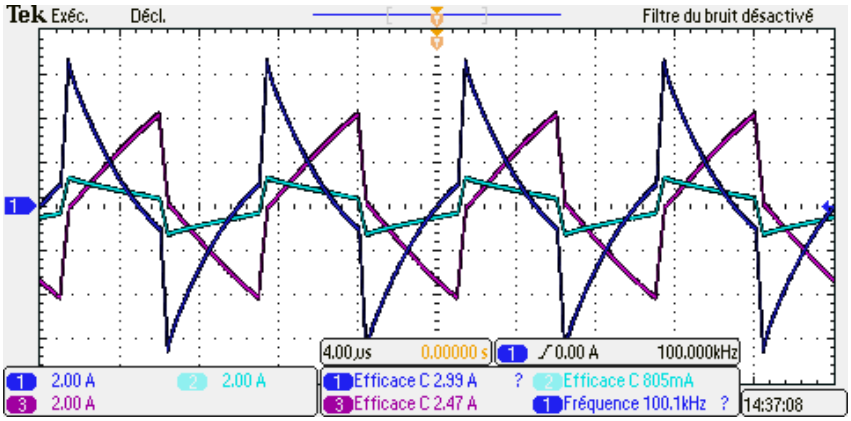


Figure 4.12 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS) V_i = 15 V; V_o = 90 V I_o = 2.0 A.

In *Figure 4.11*, it is possible to compare directly with analytical results presented in *Table 4-X*. Notice that, even though there is an error regarding the absolute results, the unbalance parameter manages to well represent. Besides, analytical theoretical results are conservative, resulting always in values larger than in practice. Regarding the current values, presented in *Figure 4.12*, the reader should not confuse the average current, which was unfortunately unavailable for measurement, with the RMS current measured across the AC-link inductors. Nevertheless, it is a function of the input and output currents, and can be considered as the RMS current flowing on through the PCA. Indeed, such value is the one in concern that will impact on the sharing of temperature. The maximum temperature 109° over the AC-link inductors show the importance of a study of mismatches in a PCA.

As the output current reduces, so does the unbalance of voltages. This is presented in *Figure 4.13*, for experimental results I_o = 1.5 A. Notice how the CSCs "a" have reduced by 1.5 V, approaching the middle CSC "b", while CSCs "c", have increase by 1 V. The difference of RMS currents in the AC-link is also reduced, as observed in *Figure 4.14*.

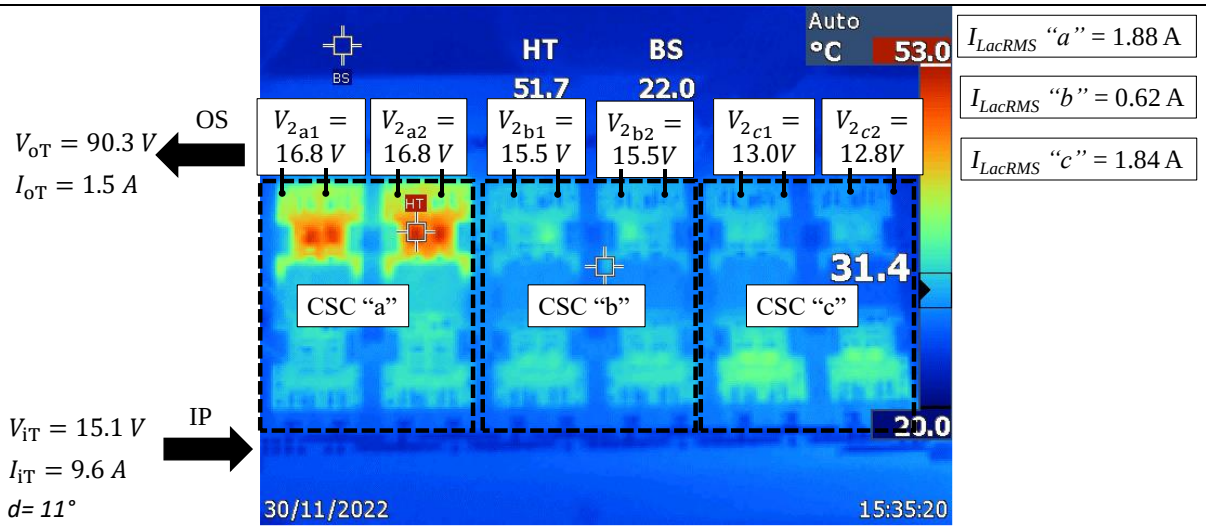


Figure 4.13 Experimental results of DC- voltages across the PCA (IPOS) V_i = 15 V; V_o = 90 V; I_o = 1.5 A. Thermographic picture is depicted.

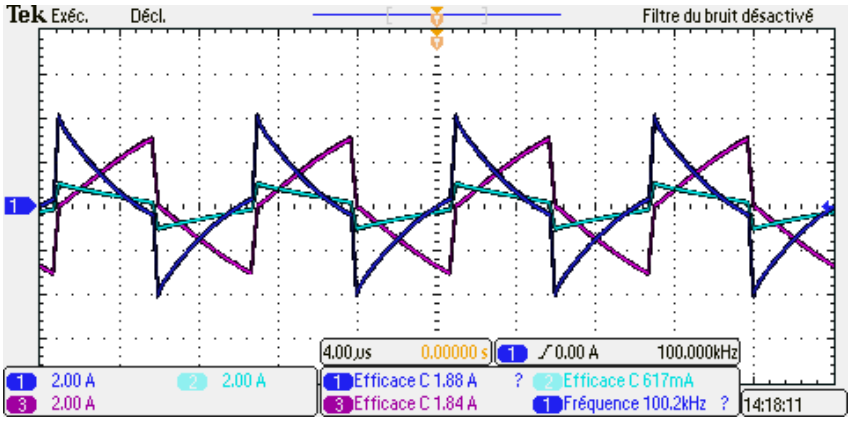


Figure 4.14 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS) V_i = 15 V; V_o = 90 V; I_o = 1.5 A.

Same conclusions as previous one for I_o = 1 A, as observed in *Figure 4.15* and *Figure 4.16*. This time, the difference between the middle CSC and the others are approximately 1 V. Concerning the RMS current values , it is noticeable that they are being better equally shared, and so is the temperature of the PCA.

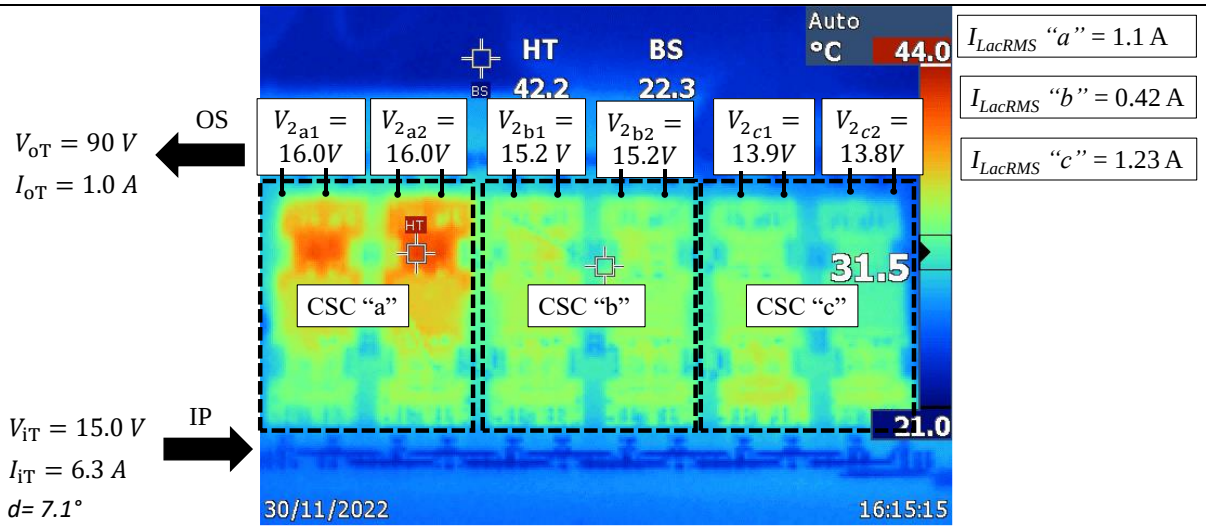


Figure 4.15 Experimental results of DC- voltages across the PCA (IPOS), V_i = 15 V; V_o = 90 V; I_o = 1.0 A. Thermographic picture is depicted.

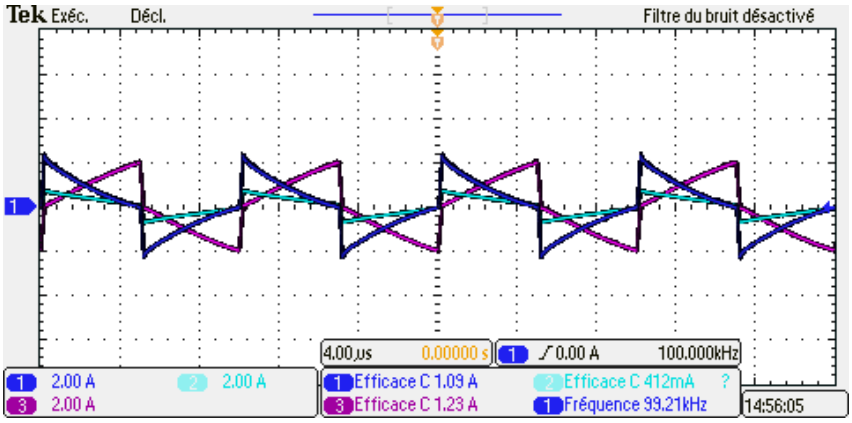


Figure 4.16 Currents in the AC-link inductances (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS) V_i = 15 V; V_o = 90 V; I_o = 1.0 A.

As it can be concluded, the output current of a PCA should be designed and limited not only by the design of one CSC, considering its rated value, or its tolerance. But rather, how their combination and distribution could impact on the temperature, RMS value and losses. In other words, the rated power of the PCA is not a linear combination of the number of CSC times the rated power of the CSC but a more complex parameter dependent on the configuration and and tolerances on components.

4.3.1.2 Varying output voltage at fixed V_i = 15 V in open circuit (OC) condition:

To go into the limit of operating conditions, and to draw conclusion and prediction out of simple tests, the OC tests are presented. In *Figure 4.17*, the phase-shift is set to zero and the output voltage, as expected is 90 V. As it can been, it confirms the trend behaviour of

equally sharing the electrical and temperature parameters. Notice that it is still possible to observe small differences in voltages current, and even its phase of AC-link currents as it can be seen in *Figure 4.18.* Those differences can be directly used to identify and infer possible anomalies in a PCA.

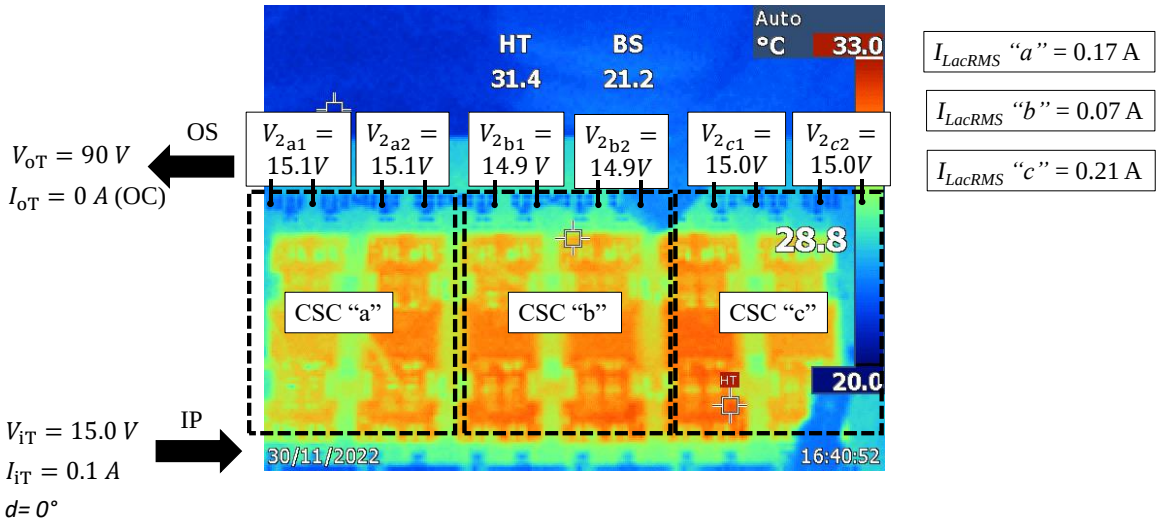


Figure 4.17 Experimental results of DC- voltages across the PCA (IPOS) Vi = 15 V; Vo = 90 V; OC Thermographic picture is depicted.

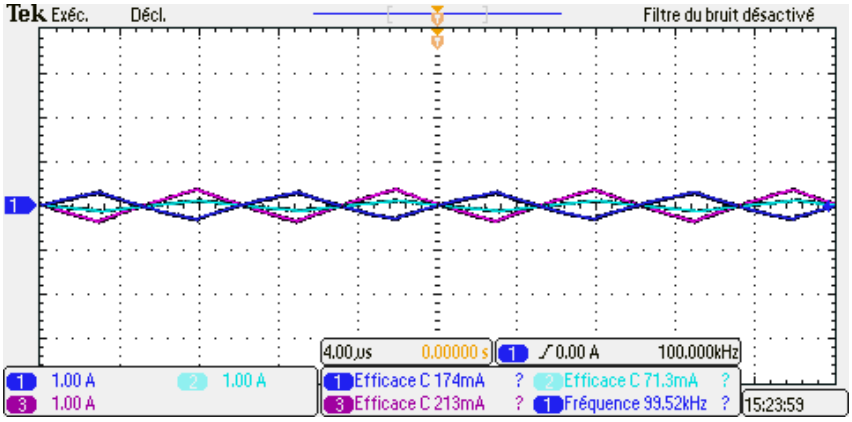


Figure 4.18 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS) V_i = 15 V; V_o = 90 V; Open circuit condition I_{ot} = 0 A.

Then, the phase-shift is set to –3.4°, setting the output to 72.2 V , still in OC conditions (step-down mode when observing rated value of one CSC), as presented in *Figure 4.19*. As it can be seen through the RMS current presented in *Figure 4.20*, such condition puts the CSCs in stress, as already explained in *Chapter 2*, which increases temperature. Notice that the unbalance among the CSCs starts to increase, meaning that certain anomalies could be

easier observable through the amplitude, but the difference in phase is no longer present. A combination of both may be used to draw better conclusions and estimate the mismatch.

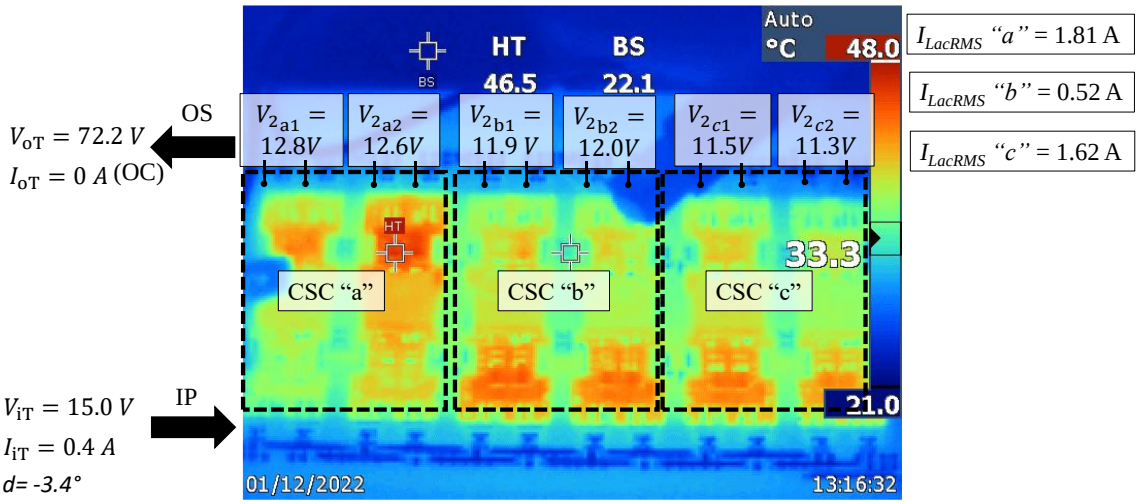


Figure 4.19 Experimental results of DC- voltages across the PCA (IPOS) V_i = 15 V; V_o = 72 V; Open circuit condition Iot = 0 A. Thermographic picture is depicted.

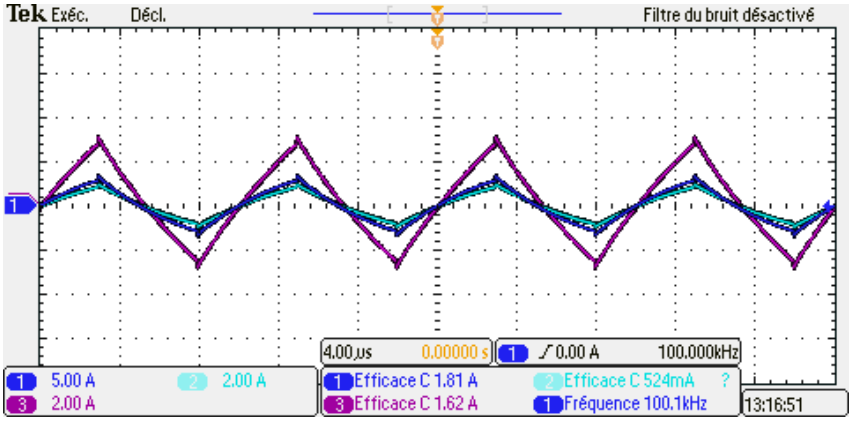


Figure 4.20 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS) V_i = 15 V; V_o = 72 V; OC

Finally, the phase-shift is set to 3.65° in order to increase the output voltage in OC up to 108 V and results are presented in *Figure 4.21* and *Figure 4.22*. The stress and unbalance is maintained, but the order of increasing voltage of each CSC type changes. As it can be concluded, the static gain can impact a lot, even at zero output current, highly impacting on the unbalance.

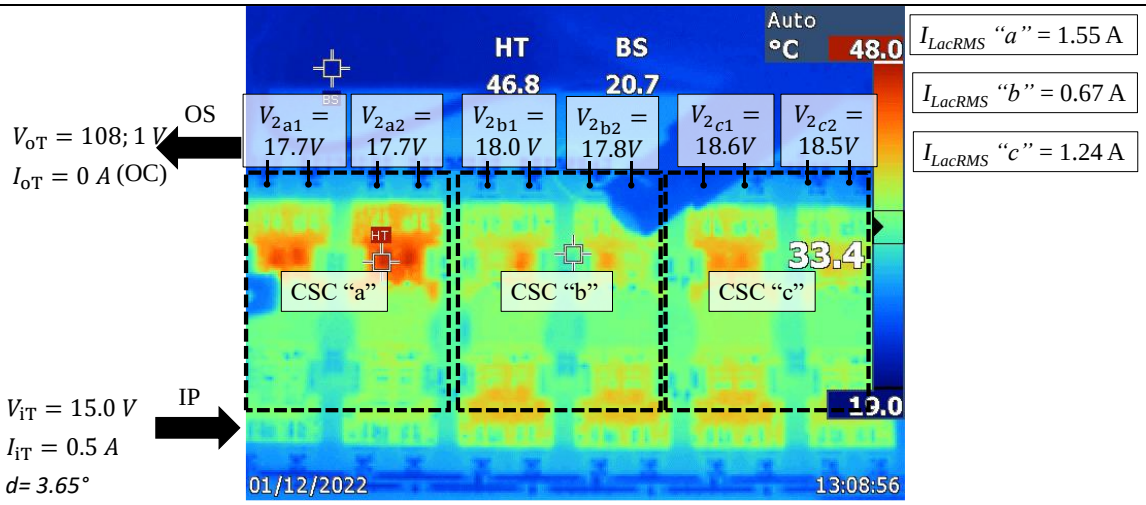


Figure 4.21 Experimental results of DC- voltages across the PCA (IPOS) V_i = 15 V; V_o = 108 V; Open circuit condition I_{ot} = 0 A. Thermographic picture is depicted.

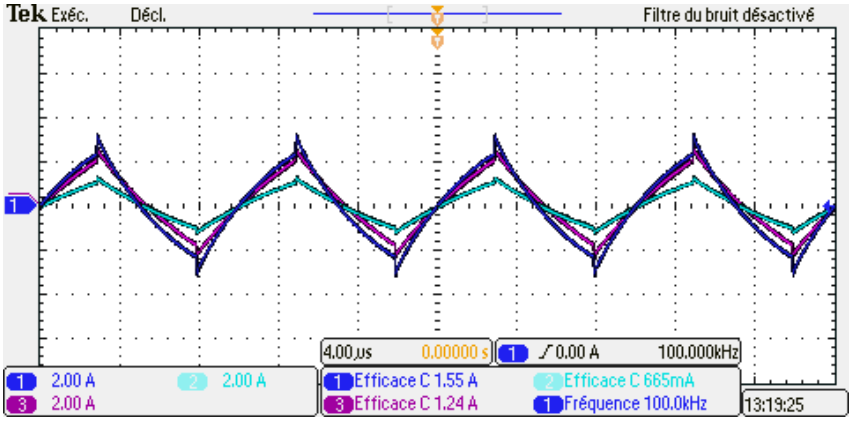


Figure 4.22 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS) V_i = 15 V; V_o = 108 V; Open circuit condition.

4.3.1.3 Varying output voltage (step-up and step-down), while keeping output current constant at 1.0 A and input voltage = 15 V.

To investigate the behavior of the unbalance impact with respect to step-up and step-down (considering rated CSC), the output current is set at 1.0 A and output voltage reduced to 72 V and increased to 108 V as presented, respectively, in *Figure 4.23* and *Figure 4.25*.

Comparing the results in *Figure 4.23* (I_o = 1 A; V_o = 72 V) to the case in *Figure 4.15* (I_o = 1 A; V_o = 90 V), it is noticeable how the fact lowering output voltage, and more specifically in a dimensionless and general way the static gain, is impacting to RMS circulating current for CSC "c", as presented in *Figure 4.24* and observing the temperature profile, and the voltage sharing. This is because the IPOS in such condition, puts the CSC "c"

in accentuated step-down mode, which highly increases the reactive power, as already discussed in *Chapter 2*.

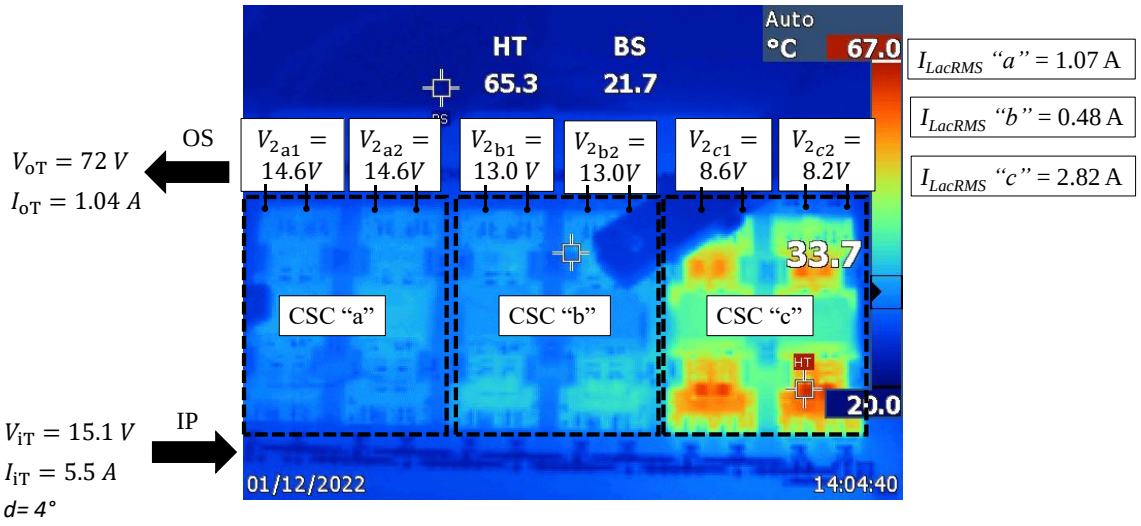


Figure 4.23 Experimental results of DC- voltages across the PCA (IPOS), V_i = 15 V; V_o = 72 V; I_o = 1.0 A. Thermographic picture is depicted.

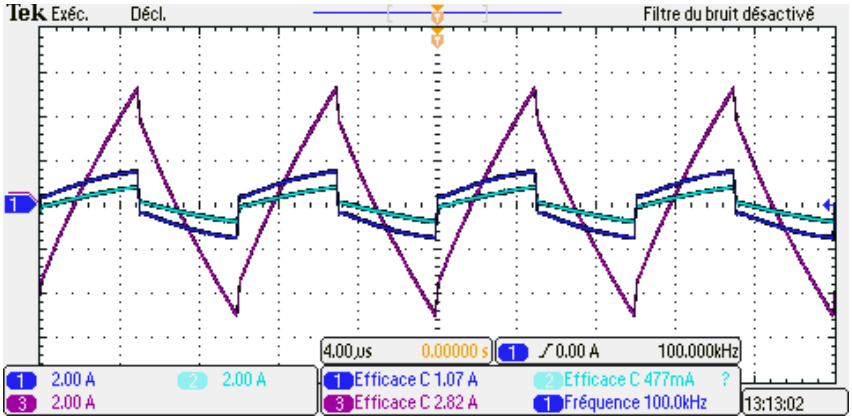


Figure 4.24 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS) V_i = 15 V; V_o = 72 V; I_{ot} = 1 A.

It is clear from comparing the results in *Figure 4.25* (I_o = 1 A; V_o = 108 V) to the case in *Figure 4.15* (I_o = 1 A; V_o = 90 V), that increasing the output voltage has a significant impact on temperature. The unbalance of voltage is less of a concern, but the step-up circuit reaches higher temperatures, specifically 102 °C in the AC-link inductors, as shown in Figure 4.25.This is due to the increased reactive power in the step-up static gain condition, as discussed in more detail in *Chapter 2*. This is visible on *Figure 4.26* with the very large current ripple on CSC "a" in step mode (please note the scaling difference with respect to other oscilloscope captures).

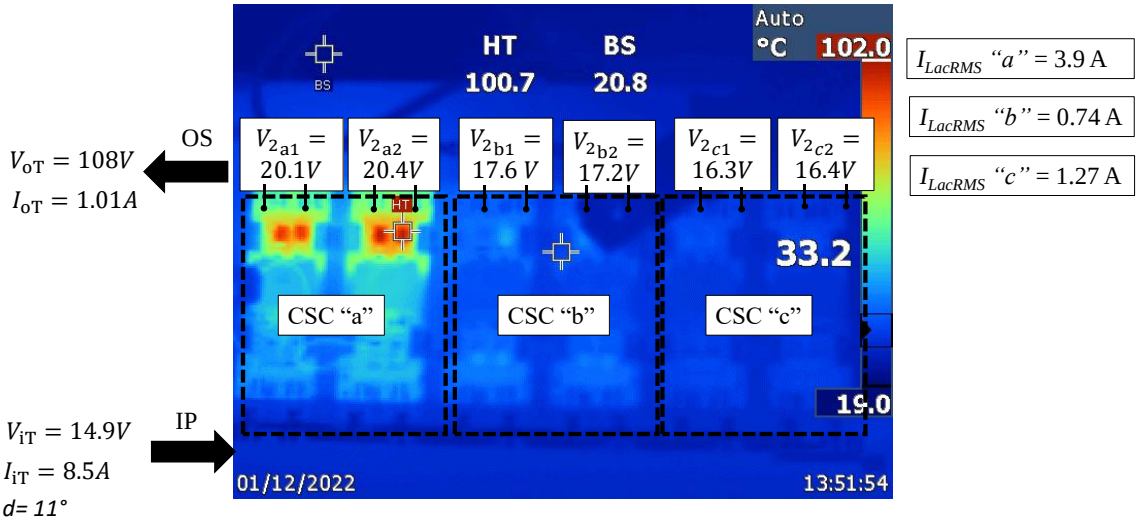


Figure 4.25 Experimental results of DC- voltages across the PCA (IPOS), V_i = 15 V; V_o = 108 V; I_o = 1.0 A. Thermographic picture is depicted.

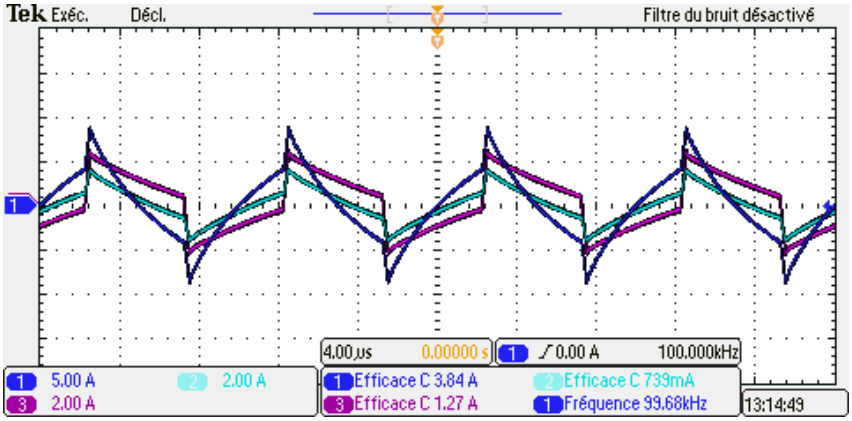


Figure 4.26 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (IPOS)

4.3.2 ISOP

4.3.2.1 Varying output current and keeping output voltage constant at 90 V.

In *Figure 4.27*, it is possible to compare input voltages at CSC level with analytical results presented in *Table 4-X*. But notice that, in the provided analytical results, the output current was not imposed as in the experimental validation. Nevertheless, the results show good accuracy for relative and absolute values. Observing the AC-currents results in *Figure 4.28* and comparing to analytical average input and output currents in *Table 4-X*, it is possible to conclude on the total apparent power circulating among each CSC. Indeed the RMS current is one of the most important parameter for constraint and design in a power converter.

Fortunately, as presented in *Chapter 2*, the RMS current can easily be found as a function of static gain *M*, and parametrized output current, γ. Comparing the ISOP configuration, in *Figure 4.27*, with the IPOS configuration, presented *Figure 4.11*, it is noticed that in both cases, the CSC "a" with lower equivalent AC-link inductance is more impacted by the peak temperature and RMS current, with the IPOS connection configuration presenting higher peak of temperature than the ISOP one. Regarding the peak voltage, a dual behaviour is noticed: for IPOS, the CSC "a" (lower AC-link inductance), presents the peak voltage of 18.4 V, followed by 15.5 V across CSC "b" ("rated" AC-link inductance), and 12.0 V across CSC "c" (higher equivalent AC-link inductance), whereas for ISOP, the CSC "c" presented a peak voltage of 19.4 V. This means that concerning the sensibility in semiconductors to voltage, the ISOP might represent a worst case than IPOS. Indeed, between ISOP and IPOS, the configuration ISOP is the one that occasioned more failures during experimental results, but dynamics which is not treated in this work may have also impacted.

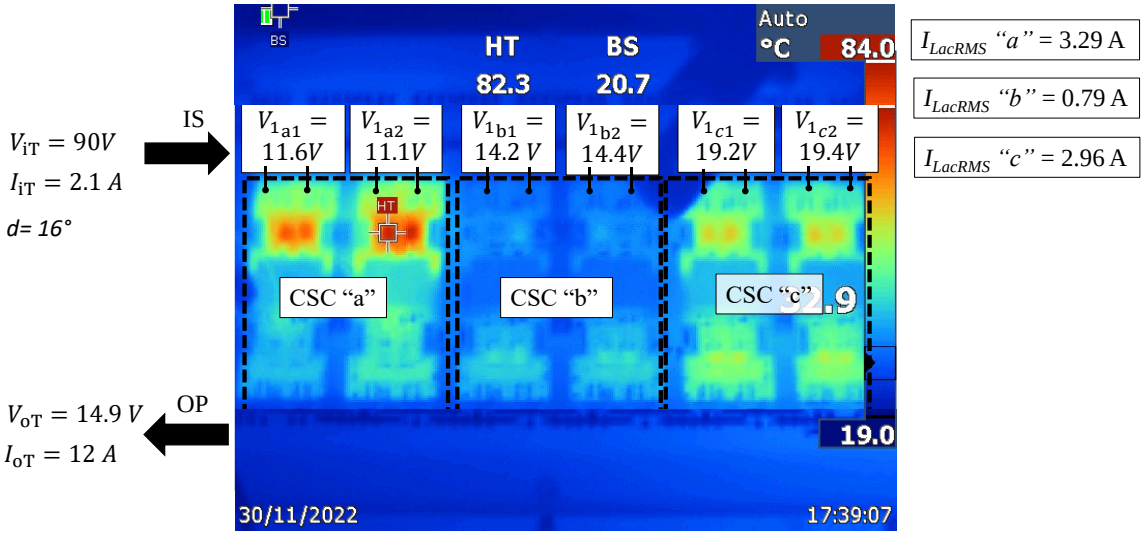


Figure 4.27 Experimental results of DC- voltages across the PCA (ISOP) Vi = 90 V; Vo = 15 V; Io = 12.0 A. Thermographic picture is depicted.

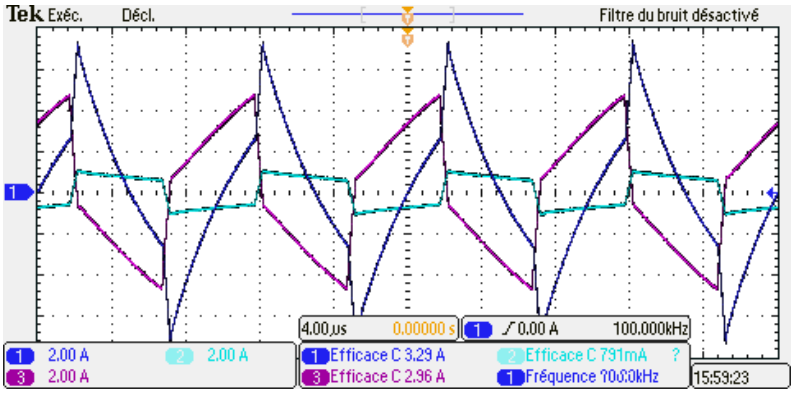


Figure 4.28 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 15 V; I_o = 12.0 A.

The behavior of ISOP with regards to output current level has been found to be similar to that previously observed in IPOS, as the output current reduces, so does the unbalance in voltage, current and temperature, as featured from *Figure 4.29* - *Figure 4.32* . Regarding the maximum absolute voltage and RMS current, the ISOP always presented larger values when comparing to IPOS. Regarding temperature, they are similar but slightly larger for ISOP this time.

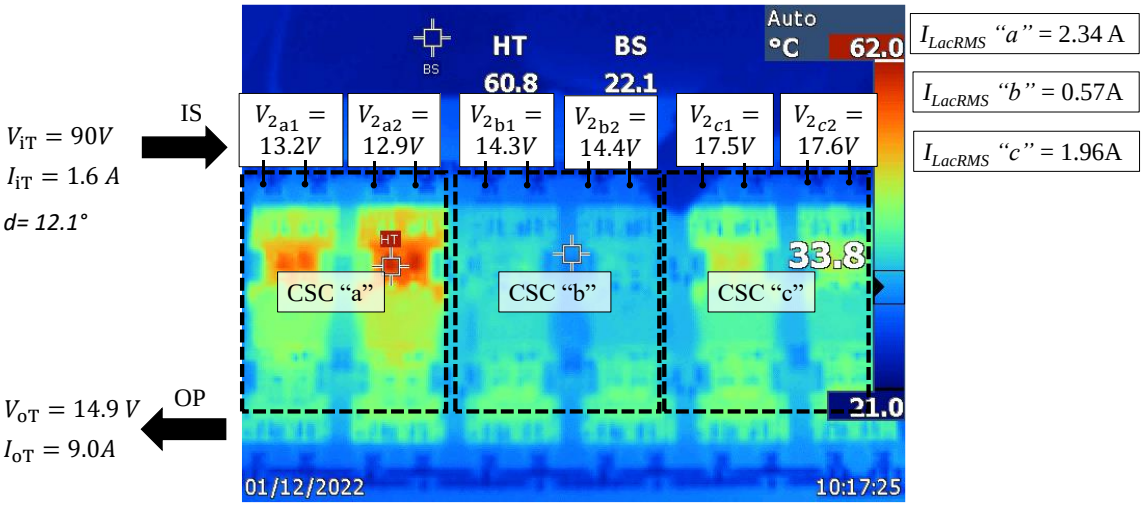


Figure 4.29 Experimental results of DC- voltages across the PCA (ISOP) V_i = 90 V; V_o = 15 V; I_o = 9.0 A. Thermographic picture is depicted.

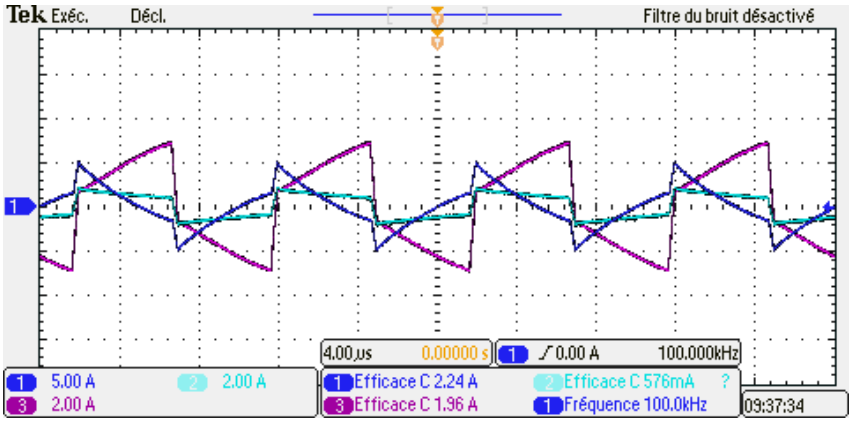


Figure 4.30 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 15 V; I_o = 9.0 A.

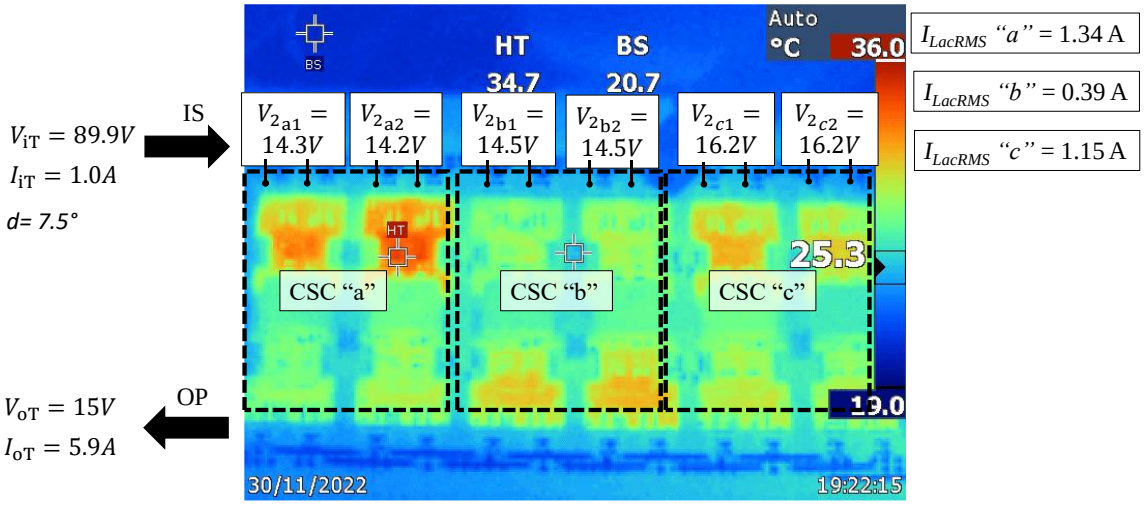


Figure 4.31 Experimental results of DC- voltages across the PCA (ISOP) V_i = 90 V; V_o = 15 V; I_o = 6.0 A. Thermographic picture is depicted.

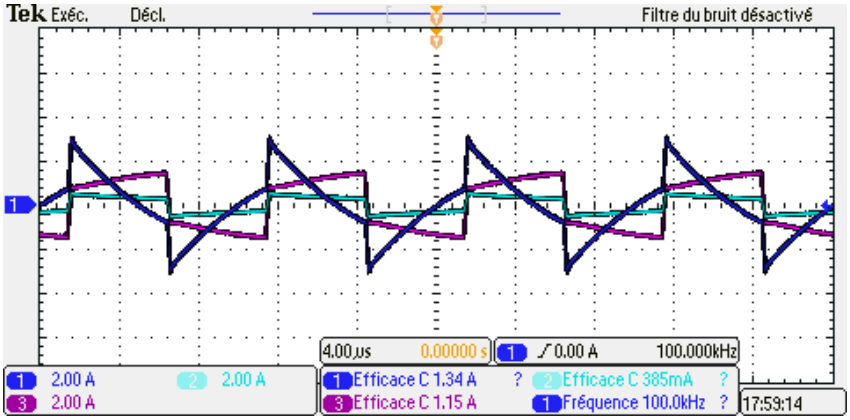


Figure 4.32 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 15 V; I_o = 6.0 A.

4.3.2.2 Varying output voltage at fixed V_i = 90 V in OC condition:

The results of OC presented in from *Figure 4.33* - *Figure 4.37* shows that there is a dual behaviour between ISOP and IPOS with respect to the balance of voltage across each CSC. An important characteristic is also highlighted: for buck modes, maximum peak voltages is found in ISOP configuration, whereas for boost modes, maximum voltage is found in IPOS configuration.

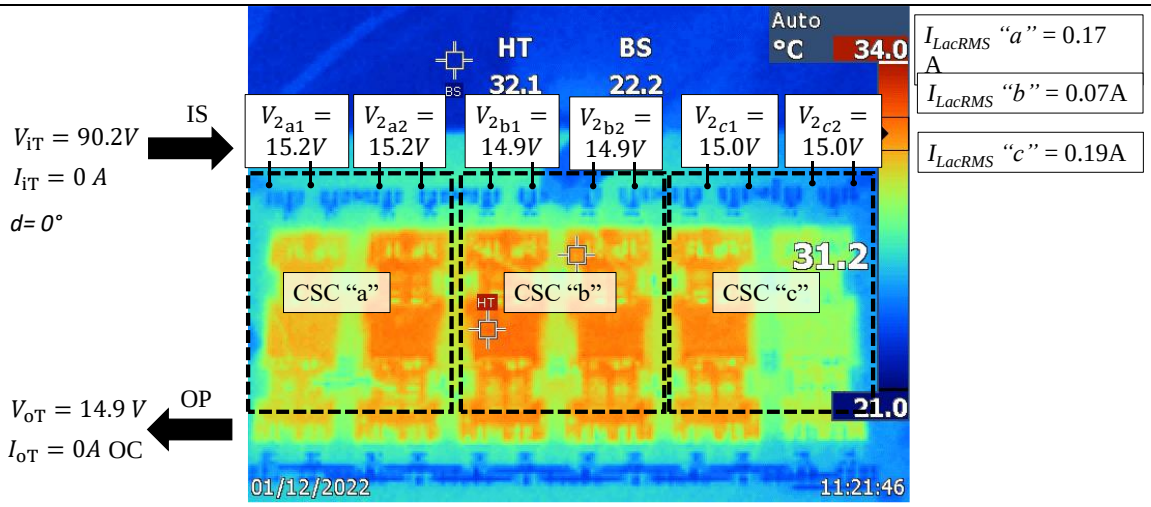


Figure 4.33 Experimental results of DC- voltages across the PCA (ISOP) V_i = 90 V; V_o = 15 V; OC. Thermographic picture is depicted.

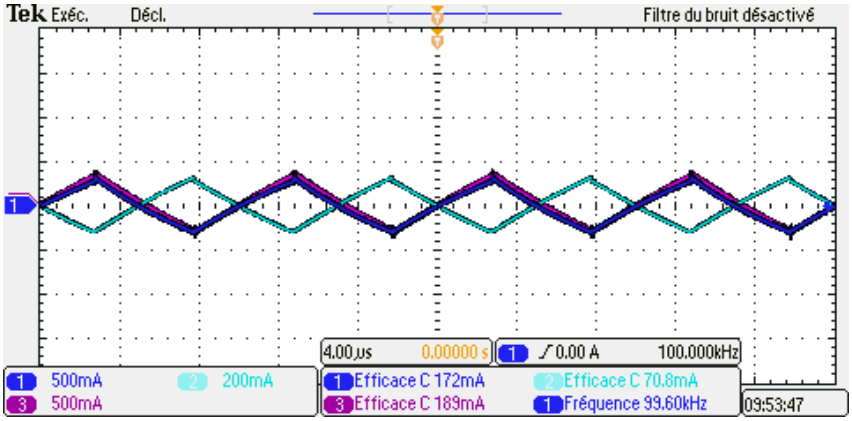


Figure 4.34 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 15 V; OC

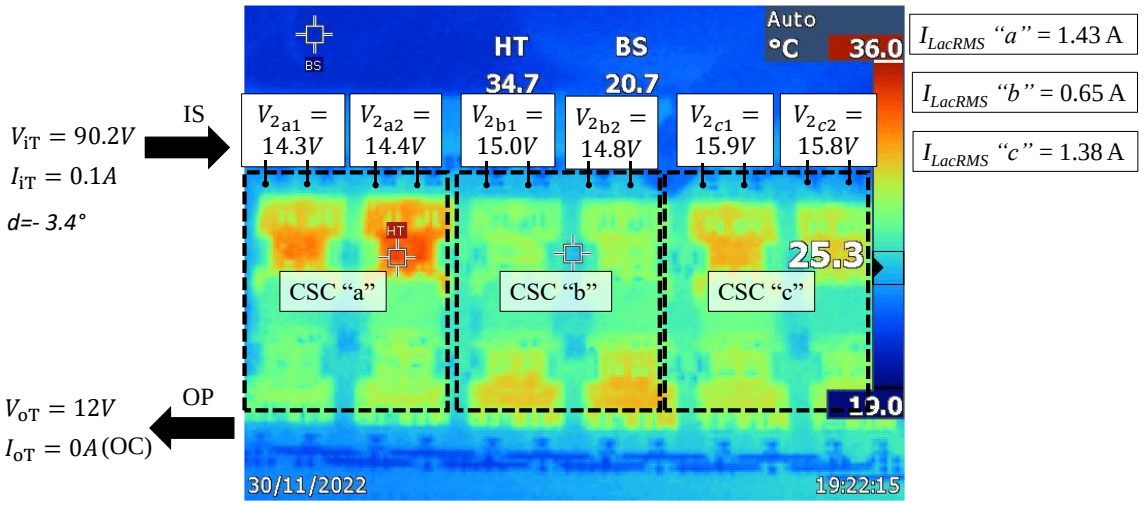


Figure 4.35 Experimental results of DC- voltages across the PCA (ISOP) V_i = 90 V; V_o = 12 V; OC. Thermographic picture is depicted.

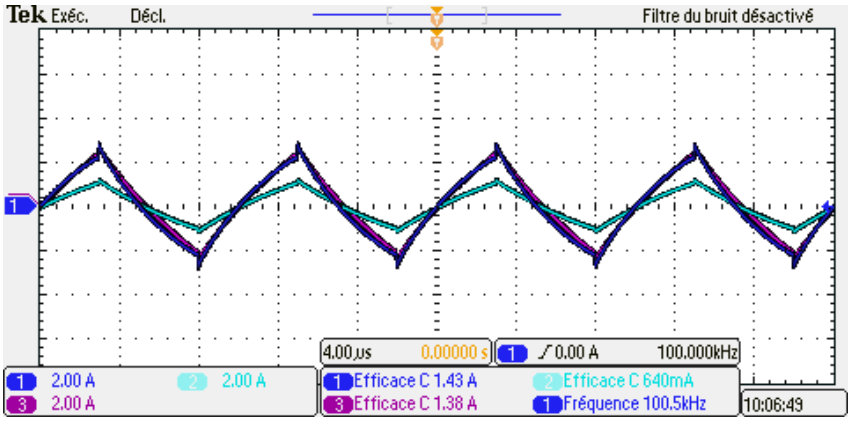


Figure 4.36 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 12 V; OC

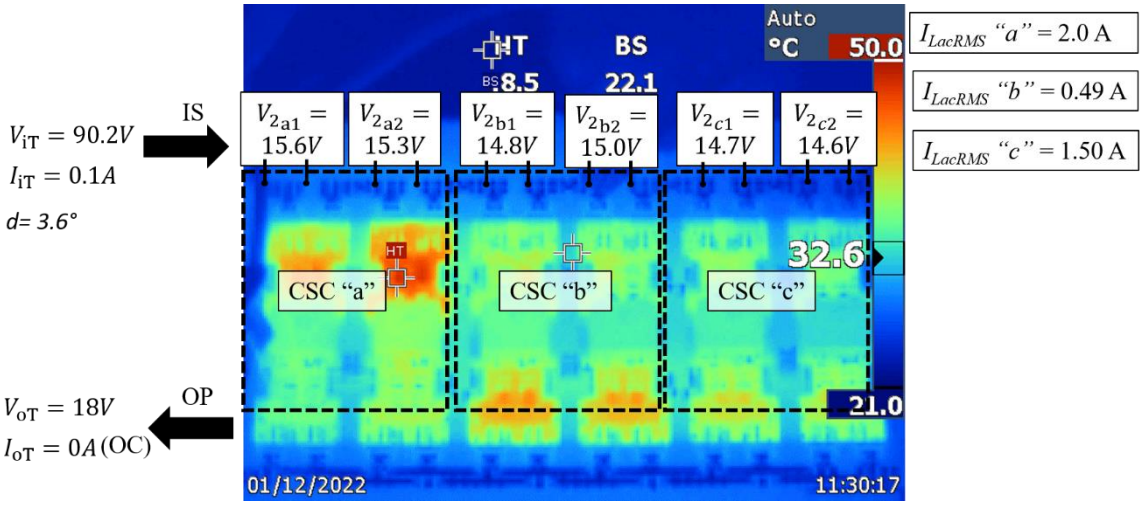


Figure 4.37 Experimental results of DC- voltages across the PCA (ISOP) V_i = 90 V; V_o = 18 V; OC. Thermographic picture is depicted.

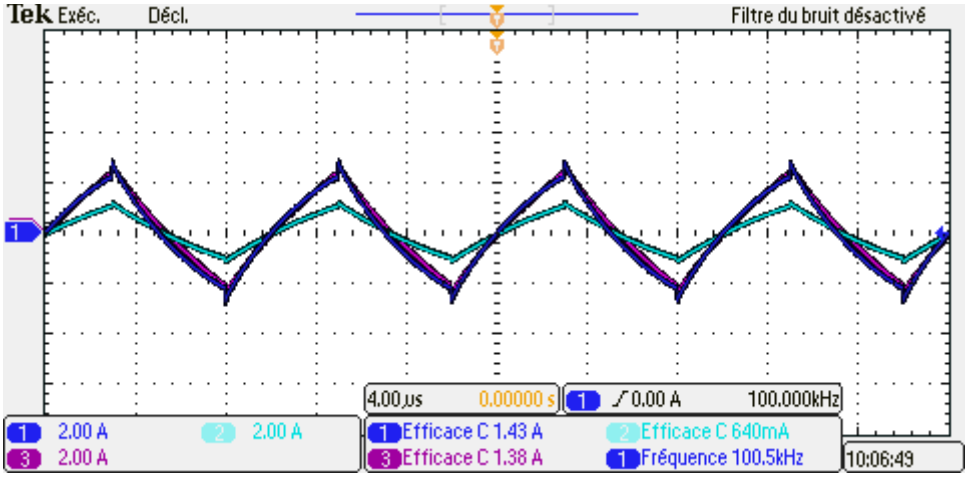


Figure 4.38 Currents in the AC-link inductances (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 18 V; OC

4.3.2.3 Varying output voltage (step-up 18 and step-down), while keeping output current constant at 6.0 A, and input voltage = 90 V.

Due to the sensibility with respect to buck and boost modes, observed in OC test and similar to IPOS, it is interesting to observe the experimental results for ISOP. Comparing the ISOP results presented in *Figure 4.39* with respect IPOS results, presented in *Figure 4.23*, it is noticeable that the CSC "c" is the one subjected to larger temperature and reactive circulating current. On the other hand, the balance voltage of CSCs in ISOP is the opposite from IPOS, presenting maximum voltage much more elevated for the CSC "c"!

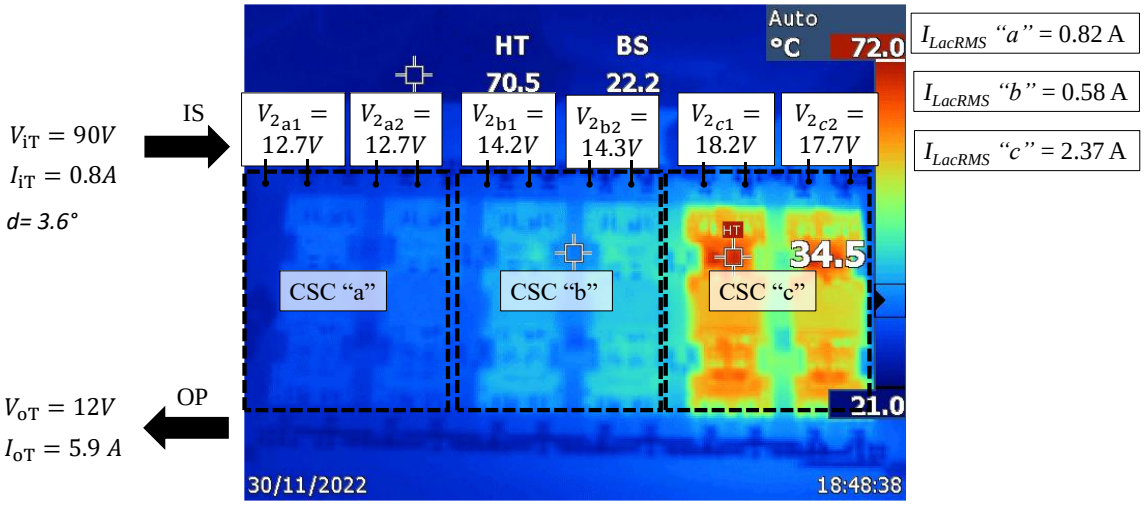


Figure 4.39 Experimental results of DC- voltages across the PCA (ISOP) V_i = 90 V; V_o = 12 V; I_o = 6 A. Thermographic picture is depicted.

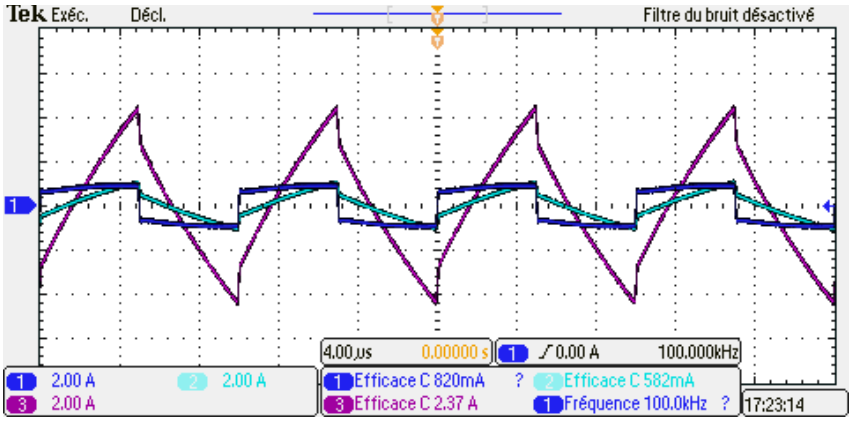


Figure 4.40 Currents in the AC-link inductances (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 12 V; I_o = 6.0 A.

When varying into to the step-up mode, the CSC "a" has this time maximum temperature reaching to a peak temperature of 131°, as presented in *Figure 4.41* (ISOP) *vs*

102° found in *Figure 4.25* (IPOS). The balance voltage of CSCs in ISOP is the opposite from IPOS, but this time, the maximum voltage is presented in an IPOS configuration across CSC "a" (20.4 V)!

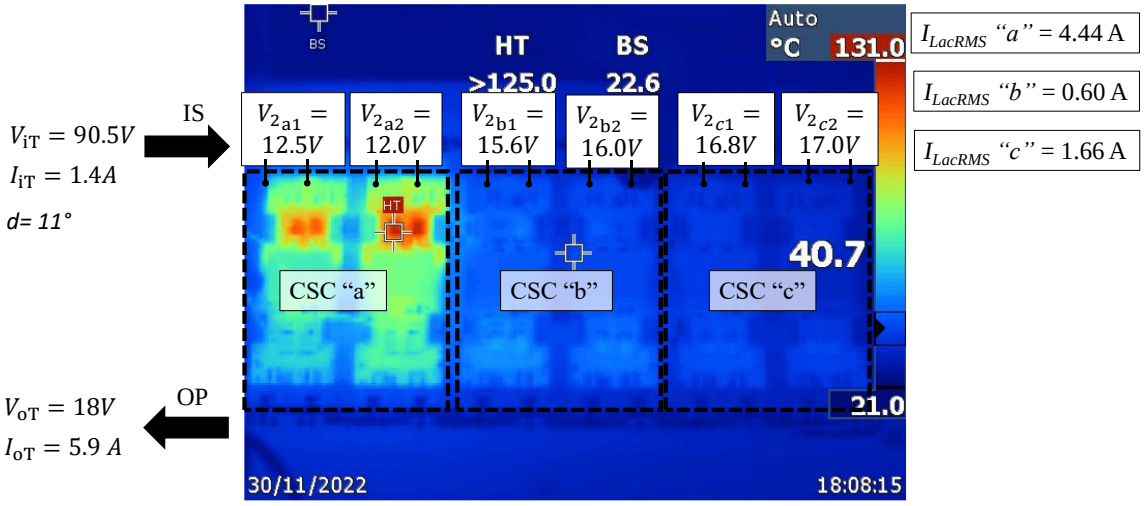


Figure 4.41 Experimental results of DC- voltages across the PCA (ISOP) V_i = 90 V; V_o = 18 V; I_o = 6 A. Thermographic picture is depicted.

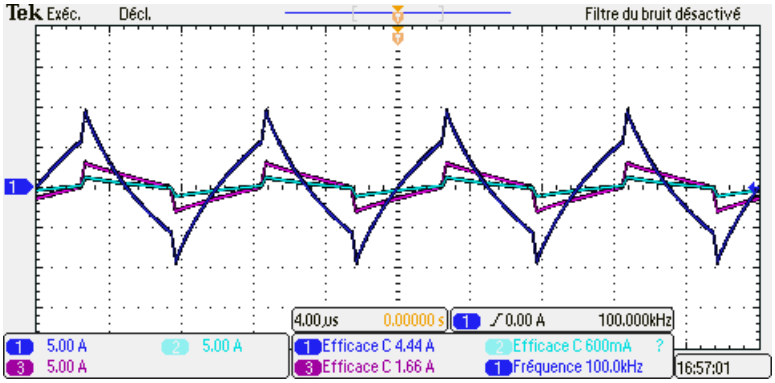


Figure 4.42 Currents in the AC-link inductors (dark blue CSCs "a"; light blue CSCs "b"; purple CSCs "c") of the PCA (ISOP) V_i = 90 V; V_o = 18 V; I_o = 6.0 A.

4.3.3 Partial conclusion and perspectives

The experimental results presented in section 3.3 were performed by forcing a change in the AC-link inductance of a PCA. The study used three types of cells, named CSC "a", CSC "b", and CSC "c", which were created by short-circuiting different numbers of inductors. The tests were conducted to verify the effect of mismatching among inductances and to check how the two port network theory could be used to describe properly mismatches among PCAs and their possible consequences. The tests were conducted in two conditions, IPOS and ISOP

by varying output voltage and/or current (down to OC condition). The results showed that as the output current reduces, the unbalance of voltages also decreases, and the RMS currents in the AC-link are better shared, leading to a reduction in maximum temperature of the PCA. When the output voltage is decreased or increased with respect to rated output voltage for unity gain (step-down and step-up modes), the stress and unbalance highly increases. Behavior and dual properties are observed on both experimental and analytical results, which itself proved to be well representative and descriptive in terms of accuracy, and more conservative in terms of errors. Experimental results for ISOS and IPOP are still required.

Concerning the OC, it was shown how the mismatch can be evaluated in advance by observing RMS and phase of the AC-link inductor currents. This simple test can then be used to identify, at once, anomalies and tolerance of AC-link inductor of a set of CSCs.

4.4 Chapter's Final Conclusion and perspectives

Overall, the proposed analytical method provides a systematic and easy-to-use approach for analysing mismatches in power converters in a general way, which can be used to improve the understanding of power electronic systems and improve the efficiency and fault tolerance of these systems. The method utilizes four two-port network parameters to observe and satisfy necessary connection realization conditions, offering a unified and systematic analytic way to analyse many power converters and their connection configurations. In the first lossless cases, the proposed method was able "to detach" the mismatch impact from the converter topology, avoiding unnecessary electric circuit analysis. An interesting property, power invariance to connection, not yet explicitly discussed in literature was also used to facilitate the correlation among connections. Additionally, the method was able to include buck and boost-based DCM converters subjected to mismatch, which were not previously treated in literature. The main benefit of this method is to improve the fundamentals of power electronic education through the abstraction of two-port network theory. Specific to this work, the DAB-based with resistive model was used, but can be used in any DC/DC converter and their resistive model. Such resistive model proved to have easier implementation, since in the absence of singularities, it guarantees all four connection realization and simple matrix operation and transformation from an impedance matrix. Even though facilitating, the cumbersome equations of the resistive case could probably be

simplified mathematically or made by cascading the losses system with other matrix that can be representative in terms of operating point and/or losses.

When comparing to experimental results, the analytical model is able to be well representative and cope with not so evident mismatch behaviour in terms of output current and voltage. However, in order to improve the analytical model, other losses, parallel, that is, dependent on input and output voltage such as switching losses and the flux / hysteresis losses on magnetic components should be accounted. For this matter, the two-port network can also be used, by cascading with resistive impedance through an improved and generic model, function on frequency, applied voltages and other parameters. Saturation behaviour present in most inductors can be another cause of inaccuracy, and therefore, the mechanism of balance can be much more complex than what it has been presented so far for both ideal and resistive models. Indeed, when assuming a saturated-model, it is possible to imagine that the balance mechanism may converge into different possible mathematical solutions that can satisfy the two-port network. If that is the case, at this point, it is interesting to evoke the second law of thermodynamics applied to closed systems, that states "with constant external parameters and entropy, (for an electric system input and output voltages and phase-shift), the internal energy will decrease and approach a minimum value of equilibrium". Such energy, expressed in work plus heat, may be minimum when the heat, that is losses, is minimized. This could mean that, from all the possible mathematical solutions, the ones with maximum efficiency could be used to describe the system in an easy way. This could explain as well why practical results provided softer mismatch impact compared to analytical results. In an ideal lossless case, surely minimal work, that is transferred power, will be the natural trendy behavior. If the saturation plays in benefice of the efficiency and stability, in a sort of natural negative feedback control, such feature could be better explored for modular converters made of DAB CSCs.

Indeed, the mismatch effect is not a controlled parameter, therefore, more statistic and sensibility analysis must be performed. This can be much more easily performed with the provided approach, and algorithms to look for the worst case scenario for different distributions. Once performed, the modular converter should be designed based on such worst case scenarios for RMS current, temperature and voltage wise, and not based in on type of CSC. In fact, it is not known in the literature if the current optimizing algorithm of multi-cell converters, particularly made of DABs, have considered theoretical statistic and sensibility analysis during the design phase.

The work provided here can also be used to draw important information about EMI signature due to mismatch. This is because important parameters that can impact on EMI

behavior, such as ZVS performance, rise and fall time, and harmonic amplitude can also be easily analyzed by coupling the parameters M_j, γ_j, σ_j into simplifying circuit models. It is an indication of how it can be challenging to predict the EMI behavior in a PCA. Eventually, such approach may be used to create algorithms to design the PCA also considering the EMI signature, as presented in *Chapter 2*.

Reference Chapter 4

[1] M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, "Design of a Highly Efficient (97.7%) and Very Compact (2.2 kW/dm ^{3}) Isolated AC–DC Telecom Power Supply Module Based on the Multicell ISOP Converter Approach," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7750–7769, Oct. 2017, doi: 10.1109/TPEL.2016.2633334.

[2] H. Fan and H. Li, "A distributed control of input-series-output-parallel bidirectional dc-dc converter modules applied for 20 kVA solid state transformer," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Fort Worth, TX, USA, Mar. 2011, pp. 939–945. doi: 10.1109/APEC.2011.5744707.

[3] J. Shi, L. Zhou, and X. He, "Common-Duty-Ratio Control of Input-Parallel Output-Parallel (IPOP) Connected DC–DC Converter Modules With Automatic Sharing of Currents," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3277–3291, Jul. 2012, doi: 10.1109/TPEL.2011.2180541.

[4] A. J. Bento Bottion and I. Barbi, "Series-series association of two Dual Active Bridge (DAB) converters," in *2015 IEEE International Conference on Industrial Technology (ICIT)*, Seville, Mar. 2015, pp. 1161–1166. doi: 10.1109/ICIT.2015.7125254.

[5] N. Hou, P. Gunawardena, X. Wu, L. Ding, Y. Zhang, and Y. W. Li, "An Input-Oriented Power Sharing Control Scheme With Fast-Dynamic Response for ISOP DAB DC–DC Converter," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6501–6510, Jun. 2022, doi: 10.1109/TPEL.2021.3138126.

[6] S. Lee, Y.-C. Jeung, and D.-C. Lee, "Voltage Balancing Control of IPOS Modular Dual Active Bridge DC/DC Converters Based on Hierarchical Sliding Mode Control," *IEEE Access*, vol. 7, pp. 9989–9997, 2019, doi: 10.1109/ACCESS.2018.2889345.

[7] V. B. Fuerback, M. S. Dall'Asta, M. André Pagliosa, and T. Brunelli Lazzarin, "Analysis of modular DCM Flyback converters in input parallel connections with parametric mismatches," *Eletrônica Potência*, vol. 24, no. 2, pp. 225–234, Jun. 2019, doi: 10.18618/REP.2019.2.0052.

[8] M. A. Pagliosa, R. G. Faust, T. B. Lazzarin, and I. Barbi, "Input-series and output-series connected modular single-switch flyback converter operating in the discontinuous conduction mode," *IET Power Electron.*, vol. 9, no. 9, pp. 1962–1970, Jul. 2016, doi: 10.1049/iet-pel.2015.0935.

[9] V. B. Fuerback, M. A. Pagliosa, M. S. Dall'Asta, and T. B. Lazzarin, "Modular ISOP Flyback converter: Analysis of auto-balancing mechanism in steady state," in *2017 IEEE 8th*

International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Florianopolis, Brazil, Apr. 2017, pp. 1–6. doi: 10.1109/PEDG.2017.7972491.

[10] C. Fernandez, P. Zumel, A. Lazaro, M. Sanz, and A. Barrado, "Simple design strategy for modular input-series output-series converters," in *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Salt Lake City, UT, USA, Jun. 2013, pp. 1–9. doi: 10.1109/COMPEL.2013.6626437.

[11] M. A. Pagliosa, T. B. Lazzarin, and I. Barbi, "Modular Two-Switch Flyback Converter and Analysis of Voltage-Balancing Mechanism for Input-Series and Output-Series Connection," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8317–8328, Sep. 2019, doi: 10.1109/TPEL.2018.2886072.

[12] R. Giri, V. Choudhary, R. Ayyanar, and N. Mohan, "Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," *IEEE Trans. Ind. Appl.*, vol. 42, no. 4, pp. 1101–1111, Jul. 2006, doi: 10.1109/TIA.2006.876064.

[13] J. W. Kimball, J. T. Mossoba, and P. T. Krein, "A Stabilizing, High-Performance Controller for Input Series-Output Parallel Converters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1416–1427, May 2008, doi: 10.1109/TPEL.2008.921151.

[14] J. W. van der Merwe and H. du T. Mouton, "An investigation of the natural balancing mechanisms of modular input-series-output-series DC-DC converters," in *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, Sep. 2010, pp. 817–822. doi: 10.1109/ECCE.2010.5617912.

[15] W. Chen *et al.*, "Indirect Input-Series Output-Parallel DC–DC Full Bridge Converter System Based on Asymmetric Pulsewidth Modulation Control Strategy," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3164–3177, Apr. 2019, doi: 10.1109/TPEL.2018.2855205.

[16] Jung-Won Kim, Jung-Sik Yon, and B. H. Cho, "Modeling, control, and design of input-series-output-parallel-connected converter for high-speed-train power system," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 536–544, Jun. 2001, doi: 10.1109/41.925580.

[17] A. J. B. Bottion and I. Barbi, "Input-Series and Output-Series Connected Modular Output Capacitor Full-Bridge PWM DC–DC Converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6213–6221, Oct. 2015, doi: 10.1109/TIE.2015.2424204.

[18] D. Ma, W. Chen, and X. Ruan, "A Review of Voltage/Current Sharing Techniques for Series–Parallel-Connected Modular Power Conversion Systems," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12383–12400, Nov. 2020, doi: 10.1109/TPEL.2020.2984714.

[19] W. Chen, X. Ruan, H. Yan, and C. K. Tse, "DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications," *IEEE*

Trans. Power Electron., vol. 24, no. 6, pp. 1463–1474, Jun. 2009, doi: 10.1109/TPEL.2009.2012406.

[20] Y. Huang and C. K. Tse, "Circuit Theoretic Classification of Parallel Connected DC–DC Converters," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 54, no. 5, pp. 1099–1108, May 2007, doi: 10.1109/TCSI.2007.890631.

[21] Qiwei Lu, Zijing Yang, Shuai Lin, Suke Wang, and Cong Wang, "Research on voltage sharing for input-series-output-series phase-shift full-bridge converters with common-duty-ratio," in *IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society*, Melbourne, Vic, Australia, Nov. 2011, pp. 1548–1553. doi: 10.1109/IECON.2011.6119537.

[22] D. Sha, Z. Guo, T. Luo, and X. Liao, "A General Control Strategy for Input-Series–Output-Series Modular DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3766–3775, Jul. 2014, doi: 10.1109/TPEL.2013.2278546.

[23] T. Lamorelle, Y. Lembeye, and J.-C. Crebier, "Handling Differential Mode Conducted EMC in Modular Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5812–5819, Jun. 2020, doi: 10.1109/TPEL.2019.2947735.

[24] V. Belevitch, "Summary of the History of Circuit Theory," *Proc. IRE*, vol. 50, no. 5, pp. 848–855, May 1962, doi: 10.1109/JRPROC.1962.288301.

[25] S. Darlington, "A history of network synthesis and filter theory for circuits composed of resistors, inductors, and capacitors," *IEEE Trans. Circuits Syst. Fundam. Theory Appl.*, vol. 46, no. 1, pp. 4–13, Jan. 1999, doi: 10.1109/81.739181.

[26] A. Ales, Jl. Schanen, J. Roudet, and D. Moussaoui, "A new analytical EMC model of power electronics converters based on quadripole system: Application to demonstrate the mode decoupling condition," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, USA, Mar. 2015, pp. 2684–2690. doi: 10.1109/APEC.2015.7104730.

[27] M. Foissac, J.-L. Schanen, and C. Vollaire, "“Black box” EMC model for power electronics converter," in *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, Sep. 2009, pp. 3609–3615. doi: 10.1109/ECCE.2009.5316113.

[28] K. Konstantin, K. Jorma, and S. Teuvo, "Analysis and Design of EMI Filters for DC-DC Converters Using Chain Parameters," 2003.

[29] C. Jettanasen, F. Costa, and C. Vollaire, "Common-Mode Emissions Measurements and Simulation in Variable-Speed Drive Systems," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2456–2464, Nov. 2009, doi: 10.1109/TPEL.2009.2031493.

[30] G. Herbst, "A Building-Block Approach to State-Space Modeling of DC-DC Converter Systems," *J*, vol. 2, no. 3, pp. 247–267, Jul. 2019, doi: 10.3390/j2030018.

[31] H. Andrei, T. Ivanovici, M. R. Ghita, C. Cepisca, and P. C. Andrei, "Analysis of the PV panels connections using the four-terminal parameters equations," in *2011 IEEE Trondheim PowerTech*, Trondheim, Jun. 2011, pp. 1–7. doi: 10.1109/PTC.2011.6019419.

[32] Tasi-Fu Wu and Yu-Kai Chen, "Modeling PWM DC/DC converters out of basic converter units," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 870–881, Sep. 1998, doi: 10.1109/63.712294.

[33] Y. S. Lee, "A Systematic and Unified Approach to Modeling Switches in Switch-Mode Power Supplies," *IEEE Trans. Ind. Electron.*, vol. IE-32, no. 4, pp. 445–448, Nov. 1985, doi: 10.1109/TIE.1985.350123.

[34] P. G. Maranesi, V. Tavazzi, and V. Varoli, "Two-part characterization of PWM voltage regulators at low frequencies," *IEEE Trans. Ind. Electron.*, vol. 35, no. 3, pp. 444–450, Aug. 1988, doi: 10.1109/41.3120.

[35] Y. M. Lai, C. K. Tse, and C. H. Szeto, "Computer formulation of averaged models for periodically-switched networks," in *Proceedings of IEEE International Symposium on Circuits and Systems - ISCAS '94*, London, UK, 1994, vol. 1, pp. 253–256. doi: 10.1109/ISCAS.1994.408803.

[36] J. John, "A study of gyrator circuits," p. 107.

[37] S. Singer and R. W. Erickson, "Canonical modeling of power processing circuits based on the POPI concept," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 37–43, Jan. 1992, doi: 10.1109/63.124575.

[38] S. Singer, "Loss-free gyrator realization," *IEEE Trans. Circuits Syst.*, vol. 35, no. 1, pp. 26–34, Jan. 1988, doi: 10.1109/31.1697.

[39] L. Arnedo, "System Level Black-Box Models for DC-DC Converters," p. 162.

[40] P. Pan *et al.*, "An Impedance-Based Stability Assessment Methodology for DC Distribution Power System With Multivoltage Levels," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4033–4047, Apr. 2020, doi: 10.1109/TPEL.2019.2936527.

[41] B. He, W. Chen, H. Mu, D. Zhan, and C. Zhang, "Small-Signal Stability Analysis and Criterion of Triple-Stage Cascaded DC System," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 10, no. 2, pp. 2576–2586, Apr. 2022, doi: 10.1109/JESTPE.2022.3149836.

[42] J. Sun, "Two-Port Characterization and Transfer Immittances of AC-DC Converters–Part II: Applications," *IEEE Open J. Power Electron.*, vol. 2, pp. 483–510, 2021, doi: 10.1109/OJPEL.2021.3104496.

[43] J. Sun, "Two-Port Characterization and Transfer Immittances of AC-DC Converters—Part I: Modeling," *IEEE Open J. Power Electron.*, vol. 2, pp. 440–462, 2021, doi: 10.1109/OJPEL.2021.3104502.

[44] J. J. Kyyrä and K. S. Kostov, "Insertion loss in terms of four-port network parameters," *IET Sci. Meas. Technol.*, vol. 3, no. 3, pp. 208–216, May 2009, doi: 10.1049/iet-smt:20080107.

[45] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *1976 IEEE Power Electronics Specialists Conference*, Cleveland, OH, Jun. 1976, pp. 18–34. doi: 10.1109/PESC.1976.7072895.

[46] S. Cuk and R. Middlebrook, "A general unified approach to modelling switching DC-tO-DC converters in discontinuous conduction mode," in *1977 IEEE Power Electronics Specialists Conference*, Palo Alto, CA, USA, Jun. 1977, pp. 36–57. doi: 10.1109/PESC.1977.7070802.

[47] P. R. K. Chetty, "Current Injected Equivalent Circuit Approach to Modeling Switching DC-DC Converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-17, no. 6, pp. 802–808, Nov. 1981, doi: 10.1109/TAES.1981.309131.

[48] Y. S. Lee, "A Systematic and Unified Approach to Modeling Switches in Switch-Mode Power Supplies," *IEEE Trans. Ind. Electron.*, vol. IE-32, no. 4, pp. 445–448, Nov. 1985, doi: 10.1109/TIE.1985.350123.

[49] F. A. Kharanaq, A. Emadi, and B. Bilgin, "Modeling of Conducted Emissions for EMI Analysis of Power Converters: State-of-the-Art Review," *IEEE Access*, vol. 8, pp. 189313–189325, 2020, doi: 10.1109/ACCESS.2020.3031693.

[50] J. Riedel, D. G. Holmes, B. P. McGrath, and C. Teixeira, "ZVS Soft Switching Boundaries for Dual Active Bridge DC–DC Converters Using Frequency Domain Analysis," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3166–3179, Apr. 2017, doi: 10.1109/TPEL.2016.2573856.

[51] B. Cui, P. Xue, and X. Jiang, "Elimination of High Frequency Oscillation in Dual Active Bridge Converters by dv/dt Optimization," *IEEE Access*, vol. 7, pp. 55554–55564, 2019, doi: 10.1109/ACCESS.2019.2910597.

[52] H. Zhao, J. Yao, and S. Wang, "A Universal DM/CM Physical Model for Power Transformer EMI Analysis within both Conducted and Radiated Frequency Ranges," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 6592–6599. doi: 10.1109/ECCE.2018.8558313.

5. Modelling and Improvement of Conducted Emission in Multi-cell Converter

The analysis and tendencies of both CM and DM noise generation, already discussed in *Chapter 1* and *Chapter 2* and insertion loss definition, presented in *Chapter* 1, is transposed and adapted to multi-cell converters. The conventional equations of Insertion Losses is adapted for multi-cell converters and conclusion on tendencies of DM EMI signature due to connection configuration Input Series (IS) vs Input Parallel (IP) as well as centralized vs distributed, already explained in [1] [2] is revised through an energy equivalent design comparison. For simplification, the mismatch impact presented in *Chapter 3* is not taken into consideration, but as concluded previously, it could be used to derive faster conclusion on its effect over the EMI signature.

Regarding CM noise, it was presented in *Chapter 1* how it can be challenging to be attenuated. In this *Chapter 5*, it is presented how such challenge is intensified with the increasing in numbers CSCs, once the CM noise is treated through conventional filter design methods. Due to a simplifying assumption, the CM noise is proved to be actively eliminated through a 180° shifting technique, performed physically and benefiting from the multi-cell structure, being it mostly independent on the connection configuration. The technique turns what is considered a problem, "intra-cell interference", into a straightforward, costless and groundless solution for CM noise reduction. Combining with the symmetrisation in all aspects of a DAB cell, it is an outstanding result capable of passing the most complicated EMC standard compliances. Besides, the CM generated by the H-bridges is even improved with the increasing in CSCs due to a statistic Gaussian curve expected behaviour. However, it is important to distinguish the CM noise generated by the MOSFETs and the ones generated by the Gate-drivers. This later one is increased with the number of CSCs and not treated in this thesis.

Finally the CE noise experimental results are provided to either prove theoretical simplifying assumption, but mainly to build EMI signature database for prediction and observed practical tendencies with respect to connection configurations (ISOS, ISOP, IPOS and IPOP), number of CSCs. Besides intermediary setups are used to promptly identify and assure the tendency through measurements of a pair of cell converters.

5.1 DM noise analysis

This section aims to simplify the analysis of the DM noise generation trend in a multicell converter with regards to the number of CSCs and their connection configurations (ISOS, ISOP, IPOS, and IPOP), detached from most converter topologies as long as they are assumed to be modeled by pure current sources in parallel to DC-link capacitor, which is well suitable for the DAB, as already explained in Chapter 1.

The input current is, under no mismatch, practically invariant to the output connection configuration, but rather to its input connection configuration. Therefore, ISOS and ISOP, present the same equivalent circuit representation. Likewise, the IPOP and IPOS present the same equivalent circuit representation. On the other hand, as it has been discussed and proved in [1] [2], for the DM noise, the IS connection suffers from attenuation reduction when considering only the DC-link capacitance as filter design. This means that the filter design becomes a function of the number of cells for such case, losing the standardization desired, and eventually a centralized solution is needed. On the other hand, the IP improves its insertion loss parameter, as the lumped DC-link capacitance increases. Notice that, even though the insertion loss is improved in such cases, the noise generation is increased at the same ratio, due to current sources lumped in parallel. Therefore, another parameter, based on the insertion loss definition in terms of two-port network parameters (***T***- parameters) discussed in Chapter 1 is necessary.

As it was presented in *Chapter 1*, Insertion Loss (IL) is an interesting parameter to evaluate the filter insertion and not directly requires the noise model, but rather its nature, while observing the expected attenuation after filter insertion. An adaption to consider not only the filter insertion, but also the number of CSCs, N, is interesting in order to evaluate the predicted behavior of many CSCs out of one CSC, as presented in .

The goal is to express a representative parameter, at least in the lower frequency range, of the insertion loss in terms of ***T***- parameters as a function of connection configuration, number of CSCs and filter distribution. It is important noting that the study does not address or examine the cascading of the power filter two-port network with the modular power converter two-port network, explained in *Chapter 4*, for the purpose of EMI modelling and neither the mismatch impact.

In order to take into account for the increasing DM current noise generation with the number of CSCs, N, for IP connection, it is defined a parameter adapted from the conventional insertion loss in terms of two-port network theory, IL', as presented in (5.1). For

the IS connection, since current sources are in series and considered equivalent, the definition remains unaltered from the original presented in *Chapter 1*.

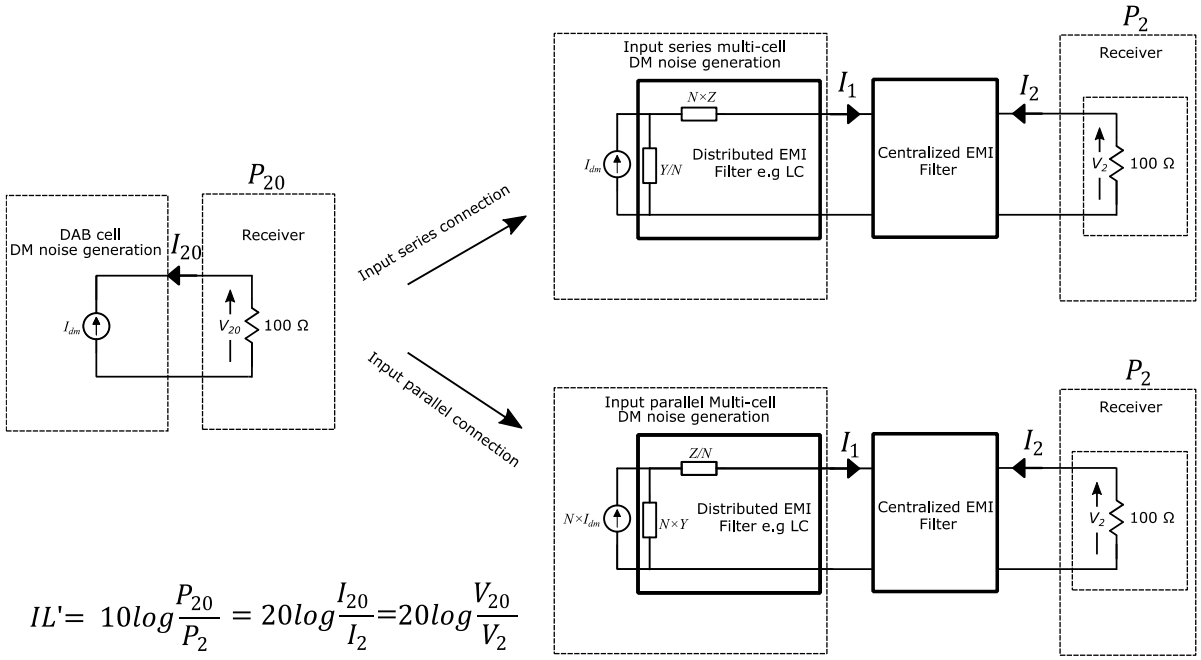


Figure 5.1 *Adapted insertion loss (IL') definition for the DM noise of both IP and IS connection configuration.*

$$IL' = \begin{cases} 20log\left(\frac{|cZ_L + d|}{N}\right), & if\ IP \\ 20log(|cZ_L + d|), & if\ IS \end{cases} \tag{5.1}$$

It remains only the definition representation of the ***T***- parameters regarding filter distribution and connection configuration for admittances and impedances as in presented (5.2) and (5.3), respectively. For the centralized filter, the value of *N* should be equaled to 1 as presented in (5.4) and (5.5), respectively, for centralized admittances and impedances. From now on, it is possible to compare on the same graph the results of any built up filter design topology in any configuration.

$$\boldsymbol{T}(Y_d, N) = \begin{cases} \begin{pmatrix} 1 & 0 \\ NY_d & 1 \end{pmatrix}, & if\ IP \\ \begin{pmatrix} 1 & 0 \\ \frac{Y_d}{N} & 1 \end{pmatrix}, & if\ IS \end{cases} \tag{5.2}$$

$$\boldsymbol{T}(Z_d, N) = \begin{cases} \begin{pmatrix} 1 & \frac{Z_d}{N} \\ 0 & 1 \end{pmatrix}, & if\ IP \\ \begin{pmatrix} 1 & 2NZ_d \\ 0 & 1 \end{pmatrix}, & if\ IS \end{cases} \tag{5.3}$$

$$\boldsymbol{T}(Y_c) = \begin{pmatrix} 1 & 0 \\ Y_c & 1 \end{pmatrix}, \quad if\ IP\ or\ IS \tag{5.4}$$

$$\boldsymbol{T}(Z_c) = \begin{pmatrix} 1 & 2Z_c \\ 0 & 1 \end{pmatrix}, \quad if\ IP\ or\ IS \tag{5.5}$$

5.1.1 Only DC-link capacitor

At a first moment, it is interesting to observe the impact of connecting many CSCs composed of only dc-link capacitor, by substituting (5.2) in (5.1), resulting in (5.6). The tendency of IL' for different number of CSC for and both IP and IS connection configurations can be found, evaluating the limit when $\rightarrow \infty$, resulting in in (5.7).

$$IL'(Y_d, N) = \begin{cases} 20log\left(\frac{|NY_dZ_L + 1|}{N}\right), & if\ IP \\ 20log\left(\left|\frac{Y_dZ_L}{N} + 1\right|\right), & if\ IS \end{cases} \tag{5.6}$$

$$\lim_{N\to\infty} IL'(Y_d, N) = \begin{cases} 20log(|Y_dZ_L|), & if\ IP \\ 0, & if\ IS \end{cases} \tag{5.7}$$

This means that the filter topology is dependent on the number of CSCs for IS connection configuration, and has a decaying ratio. The ratio reduction of IL' for IS with respect to one CSC can be demonstrated to have a decaying behavior approximately of $1/N$. In Fig. , it is presented the plotting for both IS and IP connection configuration in different number of CSCs The value of the DC-link capacitance and LISN impedance (ZL) are representative, equal to 20 μF and 100 Ω, respectively, based on [1].

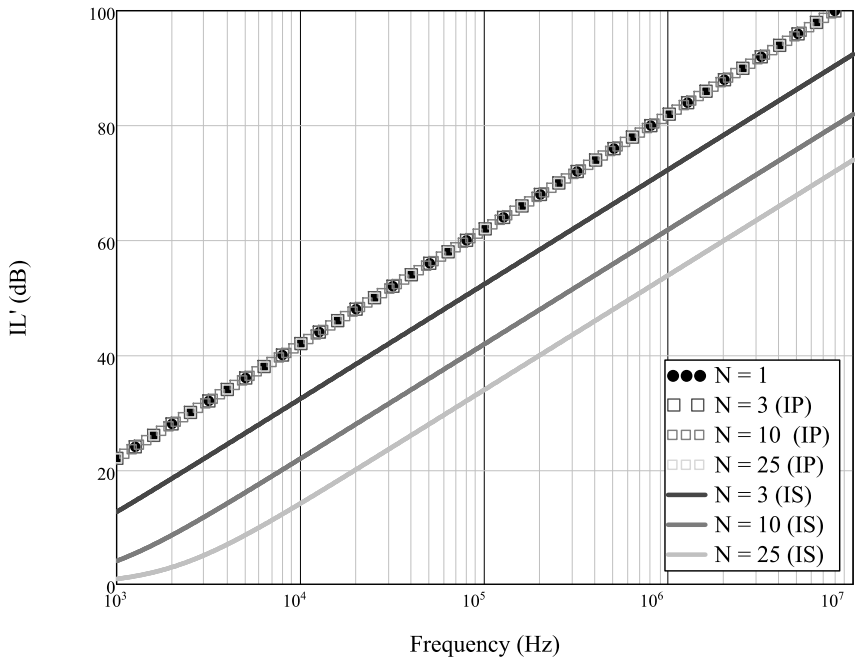


Figure 5.2 *Adapted insertion loss (IL') for DM noise analysis with* z_L *= 100 Ω and* C_{in} *= 20 μF.*

In summary, it is possible to conclude on the ideal expected behaviour when observing the EMI receiver regarding number of CSCs and connection configuration: IP configuration remains with its DM noise across the EMI receiver unaltered, whereas IS has its DM noise proportionally increased with the number of CSCs. Therefore, the designer should tackle for the IS as the worst condition configuration in which performance is degraded linearly proportional to N.

5.1.2 C-L-C through equivalent energy methodology

When considering centralized filter or mixing it with distributed solutions, it is interesting evaluate the filter topologies by imposing an equivalent energy throughout the reactive elements energy $\frac{1}{2}LI^2$ and $\frac{1}{2}CV^2$ for all connection configuration and distribution allowing comparison, as presented in (5.8) and (5.9) for capacitances and inductances, respectively.

Let:

$$\frac{1}{2}C_x N {V_i}^2 = Constant \leftrightarrow \begin{cases} C_d = C_x, & if\ IP\ or\ IS \\ C_c = C_x N, & if\ IP \\ C_c = \dfrac{C_x}{N}, & if\ IS \end{cases} \tag{5.8}$$

$$\frac{1}{2}2L_xNI_i{}^2 = Constant \leftrightarrow \begin{cases} L_d = 2L_x, & if\ IP\ or\ IS \\ L_c = \dfrac{2L_x}{N}, & if\ IP \\ L_c = 2L_xN, & if\ IS \end{cases} \tag{5.9}$$

By substituting (5.8) and (5.9), accordingly, in (5.2) - (5.5), it is derived (5.10) and (5.11) for impedances and admittances. It is possible to observe that for an equivalent energy system and ideal, distributed and centralized has the same characteristics. This is an important conclusion, since in practice the performance in frequency domain of smaller devices are better, proving that distributed solution is in practice a good solution for treating high frequency noise.

$$\boldsymbol{T}(Z_d, N) = \boldsymbol{T}(Z_c, N) = \begin{cases} \begin{pmatrix} 1 & \dfrac{2Z_x}{N} \\ 0 & 1 \end{pmatrix}, & if\ IP \\ \begin{pmatrix} 1 & 2Z_xN \\ 0 & 1 \end{pmatrix}, & if\ IS \end{cases} \tag{5.10}$$

$$\boldsymbol{T}(Y_d, N) = \boldsymbol{T}(Y_c, N) = \begin{cases} \begin{pmatrix} 1 & 0 \\ Y_xN & 1 \end{pmatrix}, & if\ IP \\ \begin{pmatrix} 1 & 0 \\ \dfrac{Y_x}{N} & 1 \end{pmatrix}, & if\ IS \end{cases} \tag{5.11}$$

Therefore, the PI-filter has its $\boldsymbol{T}$- matrix as presented in (5.12), regardless of the filter placement in an equivalent-energy filter design. The second admittance (capacitor after the LC part) is expressed as a function of a parameter u to give freedom in the design without loss of generality.

$$\boldsymbol{T_{CLC}}(Y_x, Z_x, N) = \begin{cases} \begin{pmatrix} 1 & 0 \\ Y_xN & 1 \end{pmatrix}\begin{pmatrix} 1 & \dfrac{2Z_x}{N} \\ 0 & 1 \end{pmatrix}\begin{pmatrix} 1 & 0 \\ uY_xN & 1 \end{pmatrix} = \\ \begin{pmatrix} 1 + 2uY_xZ_x & \dfrac{2Z_x}{N} \\ Y_xN\big(1 + u(1 + 2uY_xZ_x)\big) & 1 + 2uY_xZ_x \end{pmatrix}, & if\ IP \\ \begin{pmatrix} 1 & 0 \\ \dfrac{Y_x}{N} & 1 \end{pmatrix}\begin{pmatrix} 1 & 2Z_xN \\ 0 & 1 \end{pmatrix}\begin{pmatrix} 1 & 0 \\ \dfrac{uY_x}{N} & 1 \end{pmatrix} = \\ \begin{pmatrix} 1 + 2uY_xZ_x & 2Z_xN \\ \dfrac{Y_x}{N}\big(1 + u(1 + 2uY_xZ_x)\big) & 1 + 2uY_xZ_x \end{pmatrix}, & if\ IS \end{cases} \tag{5.12}$$

By substituting (5.12) in (5.1), the parameter IL' of the PI-filter can be expressed as presented in (5.13). Taking the limit of $N \to \infty$, results in (5.14) and further simplification, results in (5.15). A resonance frequency can be approximated as presented in (5.16). In *Figure 5.3*, it is presented the plotting result of (5.13) considering a representative case of L_x = 400 nH and u = 5.

$$IL'_{CLC}(Y_x, Z_x, N) = \begin{cases} 20log\left(\dfrac{\left|Y_x N\left(1 + u(1 + 2uY_xZ_x)\right)Z_L + 1 + 2uY_xZ_x\right|}{N}\right), & if\ IP \\ 20log\left(\left|\dfrac{Y_x}{N}\left(1 + u(1 + 2uY_xZ_x)\right)Z_L + 1 + 2uY_xZ_x\right|\right), & if\ IS \end{cases} \quad (5.13)$$

$$\lim_{N\to\infty} IL'_{CLC}(Y_x, Z_x, N) = \begin{cases} 20log\left(\left|Y_xZ_L\left(1 + u(1 + 2uY_xZ_x)\right)\right|\right), & if\ IP \\ 20log(|1 + Y_xZ_x|), & if\ IS \end{cases} \quad (5.14)$$

$$IL'_{CLC}(Y_x, Z_x, N) \cong \begin{cases} 20log(|Y_xZ_Lu(1 + 2Y_xZ_x)|), & if\ IP \\ 20log\left(\left|\dfrac{Y_xZ_Lu(1 + 2Y_xZ_x)}{N}\right|\right), & if\ IS \end{cases} \quad (5.15)$$

$$f_r \cong \frac{1}{2\pi\sqrt{2L_xC_x}} \quad (5.16)$$

The presented equations allow the analysis of equivalent-energy system, useful for concluding generally FOMs. It is possible to notice that it is natural for IP systems provide better and constant performance, whereas IS have worse performance while degrading it with the increase in number of CSCs. Such conclusions is made for CLC filter, but can be extended for any filter topology. The PI-filter has a resonance in which the damping factor decreases with the increase of number CSCs. The proposed energy equivalent method, on the other hand, does not allow finding the “one” standardized solution.

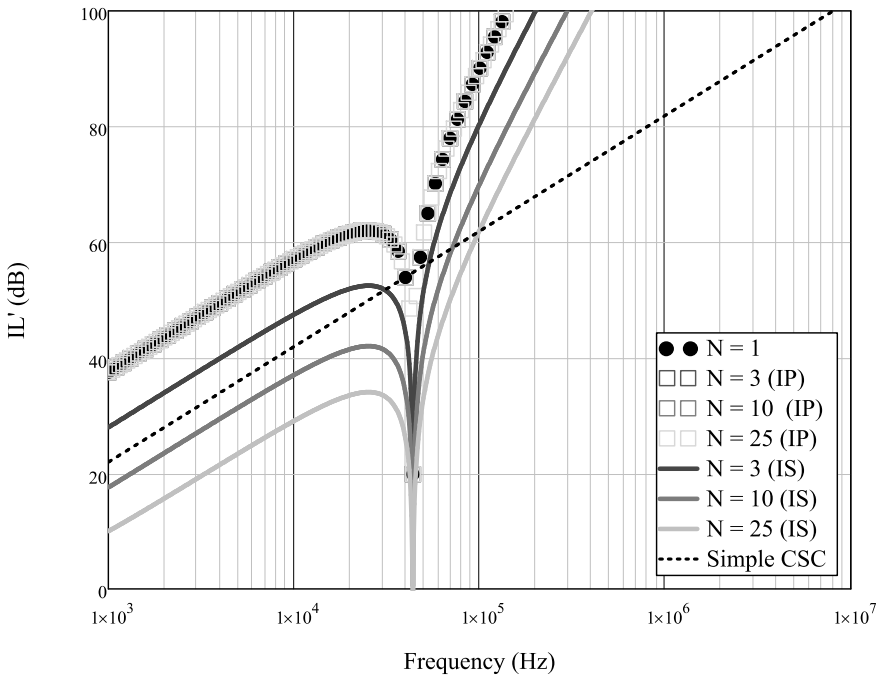


Figure 5.3 *Adapted insertion loss (IL′) for DM noise analysis of PI-filter with* Z_L *= 100 Ω and* C_x *= 20 µF,* L_x *= 400 nH and* u *= 5.*

5.1.3 PI (C_1-L-C) through equivalent performance methodology

The equivalent energy methodology was interesting to derive the conclusions aforementioned, mainly regarding the energy among distribution and centralized, which happened to be equivalent. On the other hand, as observed, the performance are not kept the same. The goal now is to provide a methodology to derive filter topologies with equivalent performance between IP and IS connection configuration, by necessary increasing the energy associated to IS connections.

To do that, the parameter in u of IS connection is changed for another one, u_{IS} , necessarily different from IP and as a function of N. Then, considering the simplified IL'_{CLC} in (5.15), a condition to approximate the IL'_{CLC} performance for IP and IS is presented in (5.17).

$$Y_x Z_L u(1 + 2Y_x Z_x) \cong \frac{Y_x Z_L u_{IS}(1 + 2Y_x Z_x)}{N} \qquad (5.17)$$

$$u_{IS} \xrightarrow{yields} uN$$

Once substituting u_{IS} in (5.13), the system can be interpreted as two: (i) having a distributed capacitor after the LC filter that increases proportionally with the number of CSCs

when connected in IS or; (ii) having a fixed centralized capacitor after the LC filter. The first interpreted solution is not desired since it is not standardized, and therefore, the second one is preferred. The plotting results of the PI-filter with a centralized capacitance equal to uN is presented in *Figure 5.4*.

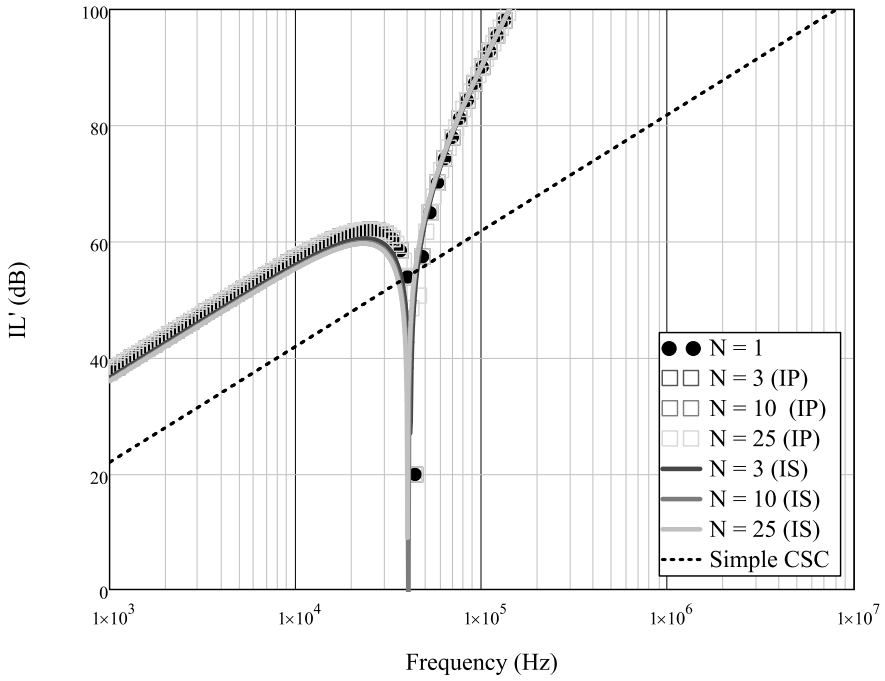


Figure 5.4 Adapted insertion loss (IL′) for DM noise analysis *of PI-filter with* $Z_L = 100\ \Omega$ *and* $C_x = 20\ \mu F$, $L_x = 400\ nH$ *and* $u = 5$.

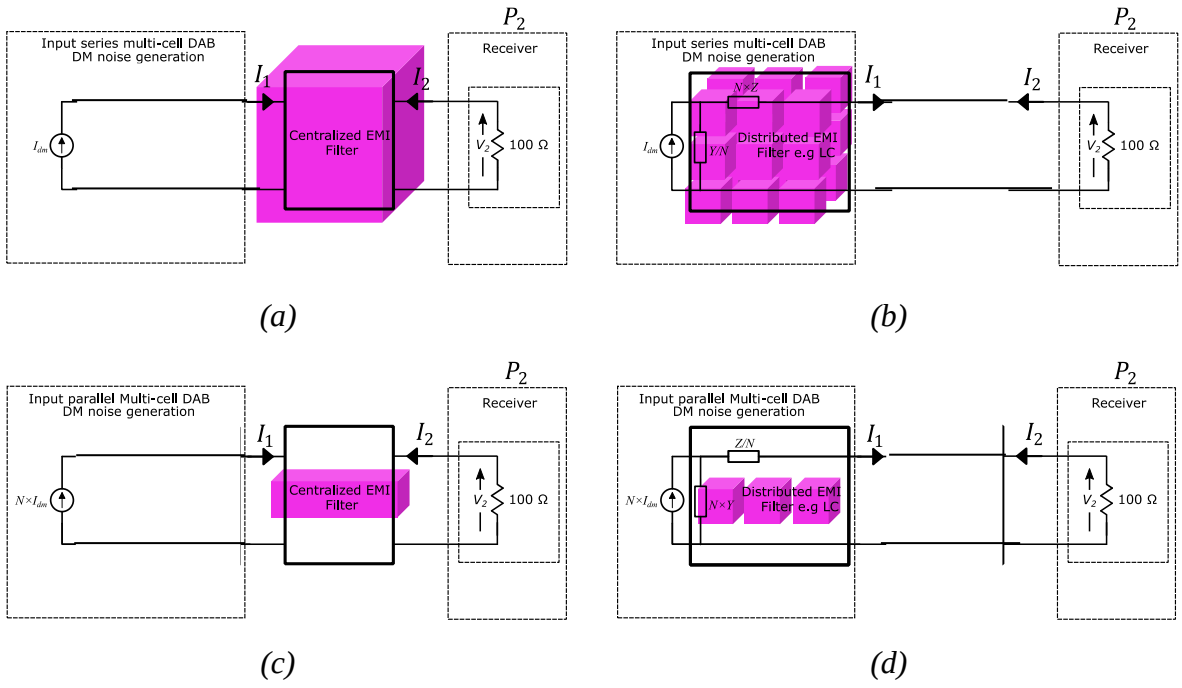


Figure 5.5 The necessary capacitive energy represented by the volume of the purple boxes to provide equivalent performance for three cell converters: (a) IS connection configuration

with centralized EMI filter; (b) IS connection configuration with distributed EMI filter; (c) IP with centralized EMI filter; (d) IP connection configuration with distributed EMI filter.

It is possible to calculated the capacitive energy ($\frac{1}{2}CV^2$) associated to C_1 and puts in evidence the necessary energy for an equivalent performance design, as presented in *Figure 5.5*, exemplified by three cell converters in which purple boxes represent the amount of energy.

It is, therefore, possible to conclude that for IP, the necessary energy increases linearly, whereas for IS, the necessary increases squarely with the increase of number of cells. Notice however, that it is not a demerit exclusive of multi-cell converters with IS connections configuration, but it is naturally intrinsic to any converter that increases in voltage. On the contrary, through interleaving modulation solutions, it is possible reduce the filter volume. Such fact explains one of the biggest advantages and success in the industry [3], [4], [5], [6], found only in modular converter approaches.

To summarize the methodology:

- Express both IL' on equivalent energy;
- Observe that IP has standardized and improved performance;
- Simplify equations;
- Modify the variables of freedom as a function of N in order to keep equivalent simplified equations;

Indeed, to make the DM noise observed across EMI receiver invariable to the number of CSCs, it is proposed the filter C-centralized L-distributed C-distributed in [1] for the IS configuration, since it satisfies two desirable designing rules:

- Standardized, desiring independent from the number of CSCs;
- Worrying harmful resonances are avoided.

Other guidelines include, if possible, prototype a CSC capable of nearly passing the EMC CE standards for the desired switching frequency. Increasing as much as possible the DC-link capacitance. By parallelizing capacitances presents the best advantages in terms of EMC performance but are limited by volume and surface area. Design a PI-filter in which: (i) the resonance frequency is either attenuated or lower than the desired attenuated frequency;

(ii) the attenuation is equivalent to the attenuation of a simple CSC (assuming that it nearly passes the EMC standard). The performance of the filter is quite guaranteed if the range of the switching frequency, e.g 200 kHz for the CSC 3.0. If adjustments are needed, the centralized capacitor can be either increased or parallelized with equivalent capacitors.

5.1.3.1 Partial conclusion and perspectives

It can be concluded that, by considering same energy, centralizing or distributing results in the same return insertion loss. On the other hand, the performance of the reactive elements in the high-frequency domain will depend on the constructive aspects, such as material type, number of turns and size or on the availability of the device on the market. Since distributed and centralized filter solution have provide, in ideal cases, same performance for equivalent-energy system, in practice, or when considering parasitic, the distributed solution will excel in terms of high-frequency performance. For the DM in the lower frequency range, around 100 kHz, still does not face, directly, the problems of performance degradation due to parasitic elements of the power filters, but for the higher frequency range, found in very high-frequency applications, or resonance frequencies due parasitic in power loop, the distributed solution is most likely the most optimum solution. Such feature does require an in depth analysis, but it is left for future studies.

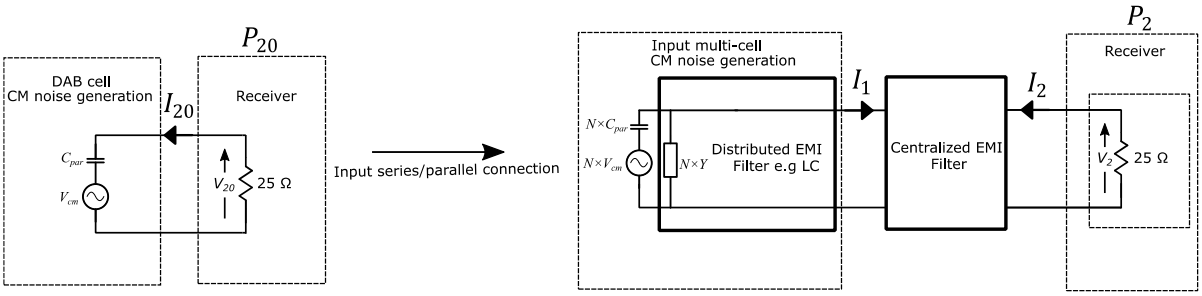
The use of two-port network proves to be efficient and easy to visualize. Complexification of impedances, considering high frequency model, including tracks, can be used to build up the T- matrix of the filter using the same methodology and can be inserted in optimizing tool in order to minimize energy (by considering higher order of filters) while keeping standardized and equivalent performance solutions.

5.2 CM noise analysis

As it was discussed in *Chapter 1*, *Chapter 2* and *Chapter 3*, the nature of the noise is provoked by a voltage source, coupled by assumedly perfect capacitive path due to parasitic capacitances. For this reason, the definition provided in (1.12) (C*hapter 1*) is used as the bases for analysing the insertion loss.

Once again, the equation must be adapted into multi-cell converter by considering the following assumptions:

- The assumption that symmetric impedance along the circuit is made and the following circuit is first used. It is assumed a perfectly resistive LISN of 50 Ohms on both phases, and therefore, Z_L = 25 Ohms;
- A very large and ideal DC-link capacitance is considered, in such a way that the CM noise "sees" a short-circuit across the input and output of each CSC. Such simplifying assumption allows to affirm that the CM noise is independent on the connection configuration for centralized filter designs. For this reason, the differentiation between centralized versus distributed filter is no longer necessary;
- To keep the analysis independent from the connection configuration, only centralized solutions are analysed, so that the distributed impedance path to be assumed a short-circuit for the CM noise;
- It is assumed that CM noise voltage increases proportionally with the number of CSCs;
- For the parasitic capacitance, the assumption presented in *Chapter 1*, a representative and worst case considering a CSC with a surface area of 25.5 cm^2 , separated by 0.1 cm from a grounded metal structure results in an equivalent parasitic capacitance C_{par} = 20 pF, which is also a representative case for the phase-leg mid point to ground parasitic capacitance of MOSFETs in TO-247 packages [7];
- It is also assumed that the source impedance $Z_s = 1/sC_{par}$ increases proportionally with the number of CSCs.



$$IL' = 10log\frac{P_{20}}{P_2} = 20log\frac{I_{20}}{I_2} = 20log\frac{V_{20}}{V_2}$$

Figure 5.6 *Adapted insertion loss (IL') definition for the CM noise. Short-circuit across DC-link capacitors are assumed for the CM noise model, making the analysis independent from connection configuration.*

As previously for the DM noise analysis, the CM noise analysis becomes, therefore, detached from the topology of the converter and a Thevenin equivalent source is assumed. This means that a general and simplifying analysis is provided for any DC/DC converter. The equation of the adapted insertion loss for CM analysis, based on the aforementioned assumptions is provided in (5.18), based this time on *Figure 5.6*.

Different from the DM analysis, the equivalent energy is not evaluated or necessary, since the energy associated to Y-capacitors are very low and does not represent a FOM. In contrast, a maximum value which is limited by maximum leakage current, e.g., 3.5 mA rms resulting in a maximum capacitance equal to 36 nF [3]. Of course, such value depends on the safety standards varying in different applications. The $\boldsymbol{T}$- matrices for distributed and centralized are presented in (5.19) and (5.20). The effect of the DM inductance and/or a common-mode chocke can be taken into account. To remind, it is assumed that the inductances and/or common-mode are centralized, the $\boldsymbol{T}$-matrix representation for centralized filter is presented in (5.21)

$$IL' = 20log\left(\left|\frac{aZ_L + b + cZ_L\frac{Z_s}{N} + d\frac{Z_s}{N}}{N\left(\frac{Z_s}{N} + Z_L\right)}\right|\right), \qquad if\ IP\ or\ IS \tag{5.18}$$

$$\boldsymbol{T}_{Y_{c_{yd}}} = \begin{pmatrix} 1 & 0 \\ 2NY_{cyd} & 1 \end{pmatrix} \tag{5.19}$$

$$\boldsymbol{T}_{Y_{c_{yc}}} = \begin{pmatrix} 1 & 0 \\ 2Y_{c_{ymax}} & 1 \end{pmatrix} \tag{5.20}$$

$$\boldsymbol{T}_{Z_{c_{CM}}} = \begin{pmatrix} 1 & Z_{c_{CM}} + Z_{\mathrm{x}} \\ 0 & 1 \end{pmatrix}. \tag{5.21}$$

With such equations resulting from simplifying assumptions, it is possible to easily analyse and conclude about different filter topologies by building an equivalent $\boldsymbol{T}$-matrix representation and substituting the parameters in (5.18).

5.2.1.1 No CM filter solution

In this scenario, no filter solution is inserted, and the parameter in (5.18) becomes (5.22), meaning that the insertion loss is reduced linearly by a factor of N, confirming that the proposed parameters follows the assumptions the CM noise should increase linearly in the

entire frequency range with the increase of N. Plotting results for such scenario is presented in *Figure 5.7*.

$$IL' = 20log\left(\left|\frac{1}{N}\right|\right), \qquad if\ IP\ or\ IS \tag{5.22}$$

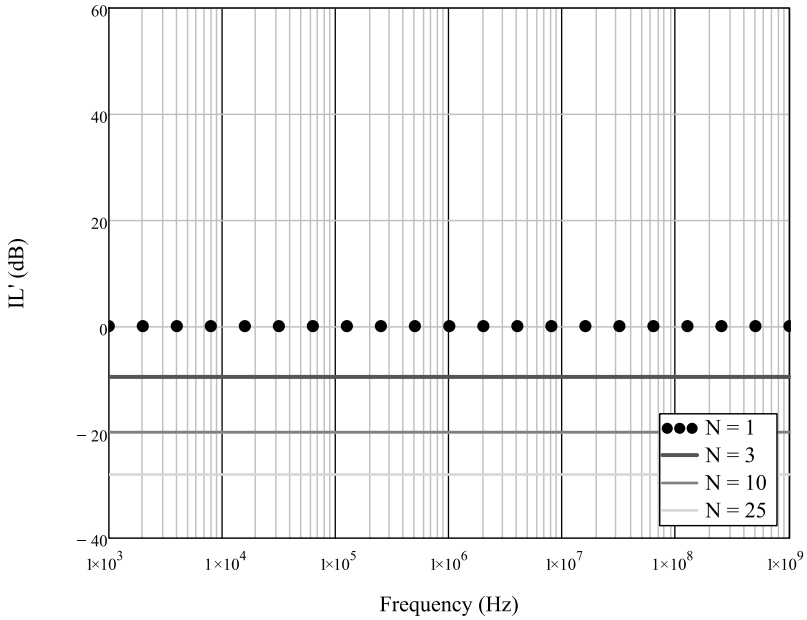


Figure 5.7 *Adapted insertion loss (IL') for CM noise analysis with Z_L= 25 Ω and no filter solution, varying the number of CSCs.*

5.2.1.2 Only Y-capacitor solution (PE available)

By substituting (5.19) in (5.18), the modified insertion loss is expressed in (5.23). An arbitrary value is defined for C_{yd} to be 5 nF; and plotting results are depicted in *Figure 5.8*. Notice that for the lower frequency range, it is expected a negative impact regarding noise attenuation, almost proportional to N.

$$IL' = 20log\left(\left|\frac{Z_L + 2NY_{c_{yd}}Z_L\frac{Z_s}{N} + \frac{Z_s}{N}}{N\left(\frac{Z_s}{N} + Z_L\right)}\right|\right), \qquad if\ IP\ or\ IS \tag{5.23}$$

As it has been presented in *Chapter 3*, the CM noise produced by the CSCs version are varying from 40 dBµV – 65 dBµV. It means that filter solution based only on only C_{yd} is not capable of providing necessary attenuation if a large number of CSCs are desired.

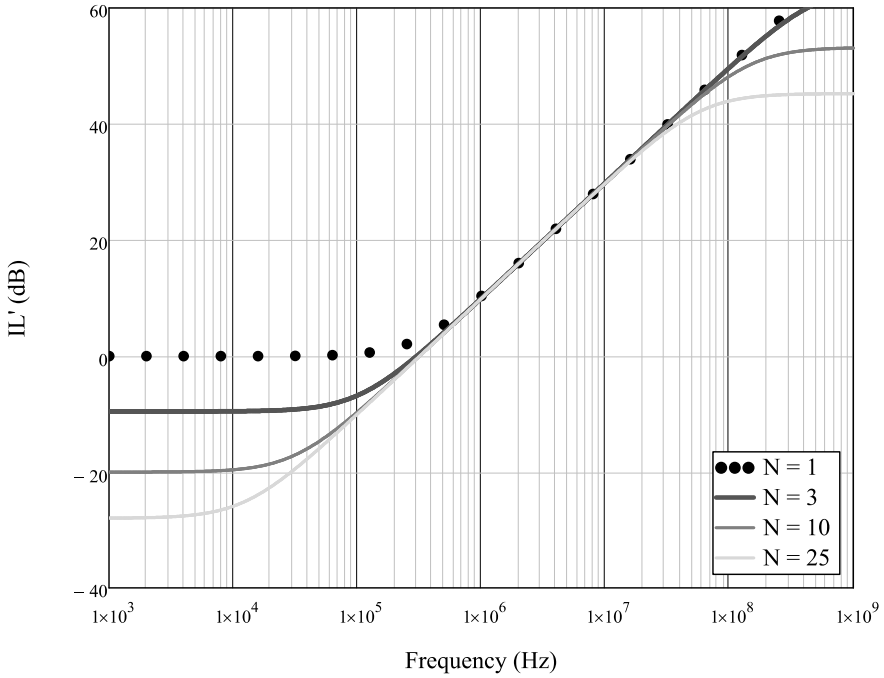


Figure 5.8 *Adapted insertion loss (IL′) for CM noise analysis with Z_L = 25 Ω and C_{yd} = 5 nF, varying the number of CSCs.*

5.2.1.3 L-C_y solution (PE available)

The effect of the DM inductance and/or a common-mode chocke must be taken into account. To remind, it is assumed that the inductances and/or common-mode are centralized. The choice and optimization of the common mode chocke is out of scope of this thesis. On the other hand, a criteria must be fulfilled: the rated current should stand the parallel connections, which is NIi, since centralized and standardized solutions are here imposed. This rapidly decreases the availability of options, while over dimensioning the filter solution for IS applications. For example considering only 6 CSCs connected in IP, rated input current of 18 A, the range of 15 single-phase common-mode chockes are available at Wurth Elektronikat through three families:

- WE-CMBNC Common Mode Power Line Choke Nanocrystalline: nine options, in which the largest magnetizing inductance is 4.5 mH (reference 7448051804 WE-CMBNC XL) with an attenuation of around 30 db @ 100 kHz, 37 dB @ 1 MHz; 20 dB @ 30 MHz;
- WE-CMB Common Mode Power Line Choke: three options, in which the largest magnetizing inductance is 1.8 mH (reference 7448262013 WE-CMB XXL) with a peak attenuation of around 24 db @ 100 kHz, 41 dB @ 1 MHz; 21 dB @ 30 MHz;

- WE-CMB HV Common Mode Power Line Choke: three options, in which the largest magnetizing inductance is 1 mH (reference 744831010205 WE-CMBHV XXL) with a peak attenuation of around 22 db @ 100 kHz, 38dB @ 1 MHz; 14.7 dB @ 30 MHz.

Since the order of magnitude of the inductor of DM PI-filter discussed previously in DM analysis are in the magnitude order of uH, its value can be neglected with respect to the inductance of the common-mode chocke, resulting in the equivalent $\boldsymbol{T}$-matrix presented in (5.24), and the insertion loss is presented in (5.25). A resonance frequency can be approximately expressed by (5.26).

$$\boldsymbol{T}_{Y_{c_{yd}}}\boldsymbol{T}_{Z_{c_{CM}}} = \begin{pmatrix} 1 & 0 \\ 2NY_{c_{yd}} & 1 \end{pmatrix}\begin{pmatrix} 1 & Z_{c_{CM}} \\ 0 & 1 \end{pmatrix} = \begin{pmatrix} 1 & Z_{c_{CM}} \\ 2NY_{c_{yd}} & 2NY_{c_{yd}}Z_{c_{CM}} + 1 \end{pmatrix} \tag{5.24}$$

$$\begin{aligned} IL' &= 20log\left(\left|\frac{Z_L + Z_{c_{CM}} + 2NY_{c_{yd}}Z_L\frac{Z_s}{N} + 2NY_{c_{yd}}Z_{c_{CM}} + 1\frac{Z_s}{N}}{N\left(\frac{Z_s}{N} + Z_L\right)}\right|\right) \\ &\cong 20log\left(\left|\frac{1 + 2NY_{c_{yd}}Z_{c_{CM}}}{N}\right|\right), \qquad if\ IP\ or\ IS \end{aligned} \tag{5.25}$$

$$f_r \cong \frac{1}{2\pi\sqrt{2NL_MC_{yd}}}, \qquad if\ IP\ or\ IS \tag{5.26}$$

The plotting results of (5.25) are presented for the value of the common-mode chocke inductance,$L_{c_{CM}}$, to be the largest one at 4.5 mH (7448051804 WE-CMBNC XL), being it a representative and industrial solution case. The Y-capacitor is chosen to be 5 nF and distributed as previously. As it can be seen, the filter solution is now capable of attenuate the lower frequency range, at the cost of a bulky common-mode chocke.

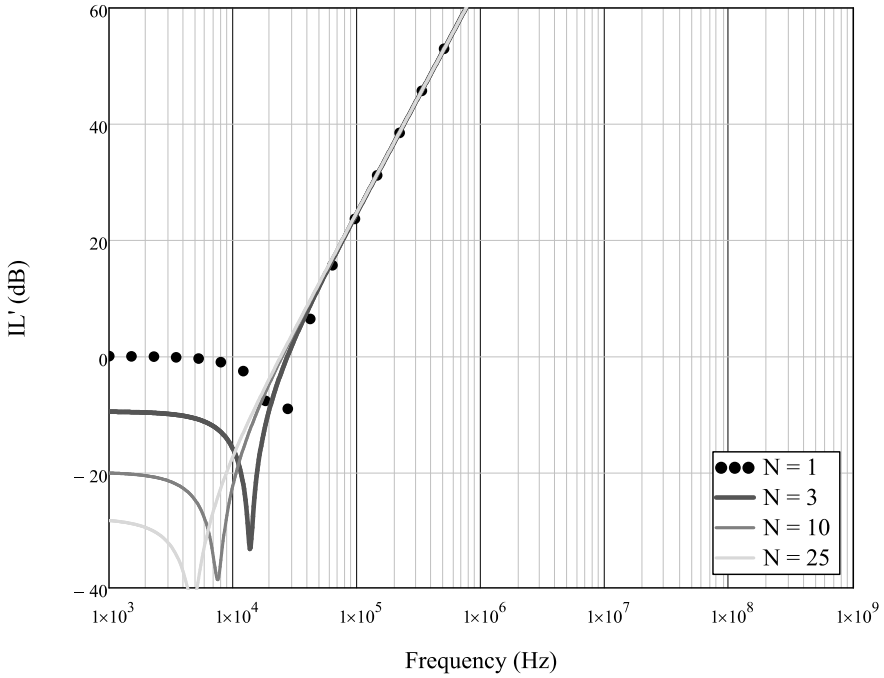


Figure 5.9 *Adapted insertion loss (IL′) for CM noise analysis with* Z_L *= 25 Ω ,* C_{yd} *= 5 nF,* $L_{c_{CM}}$ *= 4.5 mH, varying the number of CSCs.*

5.2.1.4 Only $L_{c_{CM}}$ (PE not available)

Finally, the las case is evaluated for applications in which the PE is not available, counting only on the common-mode chocke. By substituting (5.21) in (5.18), results in (5.27), in which plotting results are presented in *Figure 5.10*. The resonance frequency is approximately expressed by (5.28). Notice that, as the number of CSCs increase, the resonance decreases, while the damping is reduced. NC_{par}.

$$IL' = 20log\left(\left|\frac{Z_L + Z_{c_{CM}} + \frac{Z_s}{N}}{N\left(\frac{Z_s}{N} + z_L\right)}\right|\right) \cong 20log\left(\left|\frac{1 + 2NZ_{c_{CM}}}{N}\right|\right), \qquad if\ IP\ or\ IS \tag{5.27}$$

$$f_r \cong \frac{1}{2\pi\sqrt{NL_M C_{par}}}, \qquad if\ IP\ or\ IS \tag{5.28}$$

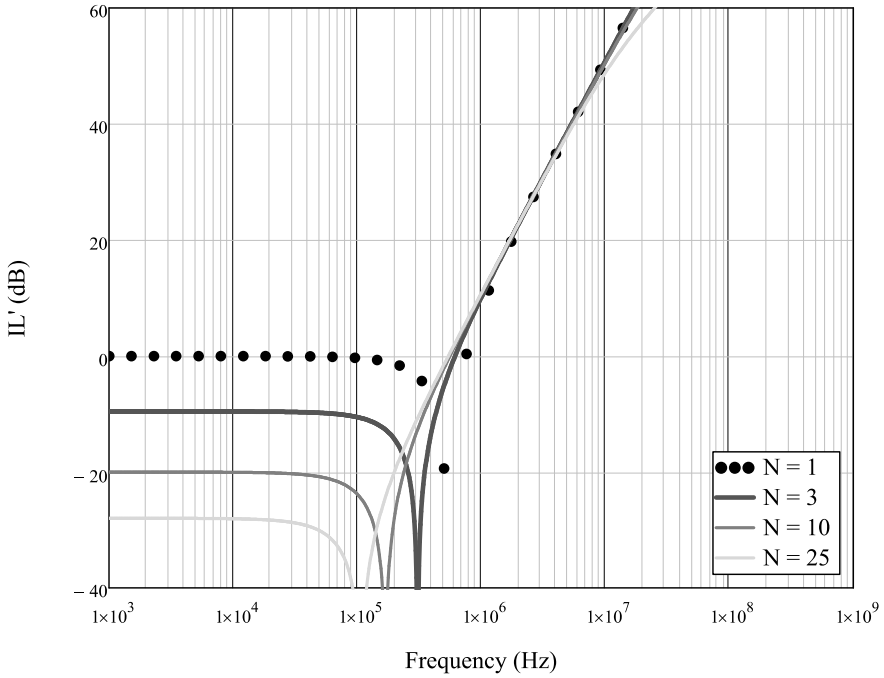


Figure 5.10 *Adapted insertion loss (IL′) for CM noise analysis with* Z_L *= 25 Ω ,* $L_{c_{CM}}$ *= 4.5 mH, varying the number of CSCs.*

5.2.1.5 Partial conclusions and perspectives

Those were simplifying assumptions but were enough to understand the difficulties of passing the EMC standards, mainly due to CM noise in a multi-cell approach. Due to the high rated current that limits and feasible value of common-mode chockes, it is possible to conclude the opposite from DM analysis: while IS is capable of attenuating more easily (with larger CM chocke inductances), the IP seems to be an over dimensioning factor in a conventional and standardized way since energy increases with the square of rated current. Besides, for applications in which PE is not available, it could be almost impossible to pass the EMC standards through passive filters. The LC filter was capable of attenuating 20 dB at the switching frequency range, around 100 kHz) considering the largest options and ideal filters. In practice, resonances, saturation, mixed mode and other parasitic interactions will certainly make the task much more complicated. Different methods based on optimizing the filter design through higher filter orders and customized common-mode chokes can also be implemented; but they would still be complicated and bulky. In an application without access to PE, it is almost impossible to passes the standards, because it requires an extremely large inductance, or, paradoxically, larger parasitic capacitances, which may increase the current noise for certain power converter topologies and modulations.

5.2.2 Near Zero CM noise filter(less) solution for multi-cell converters

The principle is based on active compensation, as presented in *Chapter 1*, which states that when two nodes exhibit complementary voltage changes while retaining equal parasitic capacitances, it increases the probability of reducing common-mode noise. When referring as probability, it means that due to undesirable mismatch in complementary gate pulses and parasitic capacitance [8], the natural CM current cancelation in a DAB SPS modulated is compromised. Eventually, synchronization of the gate to avoid delays [8] or automatic tuning [9] can significantly reduce CM current noise. On the other hand, implementing gate tuning can be cumbersome for a multi-cell approach. In the literature [10], an ISOP (380 V – 12 V) DCX converter operating at 1MHz applying 180° interleaving has shown a reduction of around 50 dB in the low to medium frequency range (up to 15 MHz). But the analysis are specific to ISOP and not generalized to any connection configuration. Besides mathematical bases to support, experimental results are still required. Therefore, a novel signal conditioning based on physical 180° interleaving is proposed in this section, as presented in *Figure 5.11*. For the practical implementation, buffers are inserted to guarantee signal integrity since signal passes through the CSCs. As presented in *Figure 5.12*, through jumpers it is possible to keep PWM signal unaltered, 0, or with a 180°, notated as π.

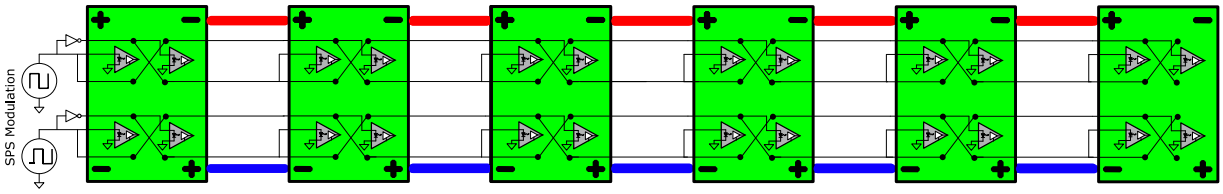


Figure 5.11 *Near zero CM noise filter(less) proposed solution.*

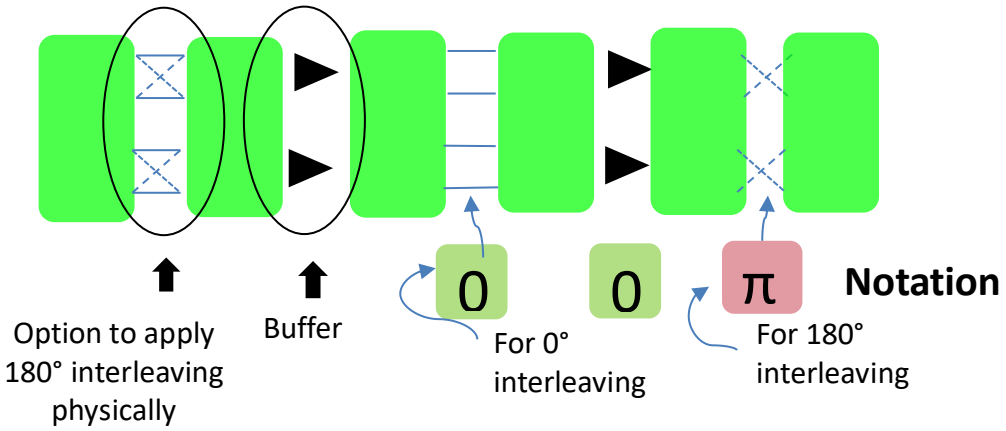


Figure 5.12 Electric and mechanic schematic used to perform the 0° interleaving, notated as "0"; and 180°, notated as π.

It assumes that due to undesirable and hardly identifiable mismatches in a given CSC, an equivalent voltage CM noise is composed of two noises, as presented in (5.29): a residual noise V_r, due gate-driver and other not modeled CM noise generation; and a an equivalent noise, V_{TH}, generated by the DAB (H-bridges + AC-link). Since same technology, operating conditions and symmetry are found in the proposed PCA approach, it is expected that the noise can be shifted 180°, and therefore actively suppressed in a pair of CSCs, as presented in *Figure 5.13*.

$$V_{noise} = V_r + V_{TH}e^{-i0} \tag{5.29}$$

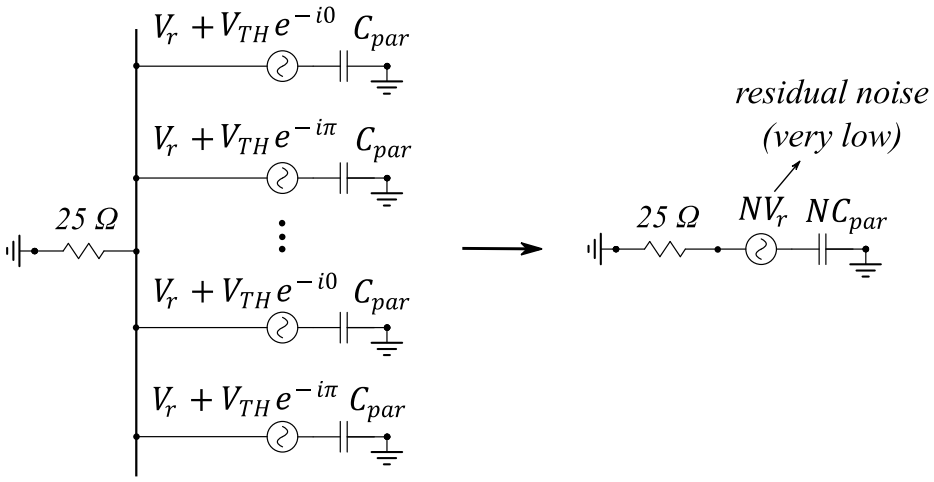


Figure 5.13 *Near zero CM noise filter(less) equivalent circuit.*

5.2.2.1 Partial Conclusions and Perspectives

The benefit of such approach is that it does not require a CM noise model and it is simple to apply in any multi-cell approaches. Even though it has been applied for multi-cell converters, any parallel DC/DC based on same parallel technology can benefit from the 180° shifting approach. Eventually, other combining solutions, gate tuning and slew rate analysis, the solutions can be further improvement. It is noteworthy noticing that, while DM noise is attenuated by conventional interleaving and usually is the focus portrayed in the literature, the CM noise is attenuated by 180°. A study combining both techniques are still necessary in order to minimize total filter volume / loss. Finally, as the solution is based on strong assumptions, the experimental results are therefore essential for validation.

5.3 Experimental results

Experimental results were performed with CSC 3.0 (Without Y-Capacitor) and the PCA 3.0, as presented in *Figure 5.14* , composing of 6 CSCs connected in IPOS or ISOP with V_i = 15 V, I_o = 2.5 A and M = 1. For experimental results, an LISN, set to measure the "+" phase (CM and DM noise) and EMI receiver *(set as such: from 50 kHz to 500 MHz; Span = 499.95 MHz; Rf Att = 0 dB; RBW = 9 kHz; VBW = 30 kHz; Sweeping time = 15 s, Auto peak detector).* During experimental results, it is reminded to the reader to observe and pay attention to the odd harmonics (100 kHz, 300 kHz, 500 kHz…), that are linked to the CM noise.

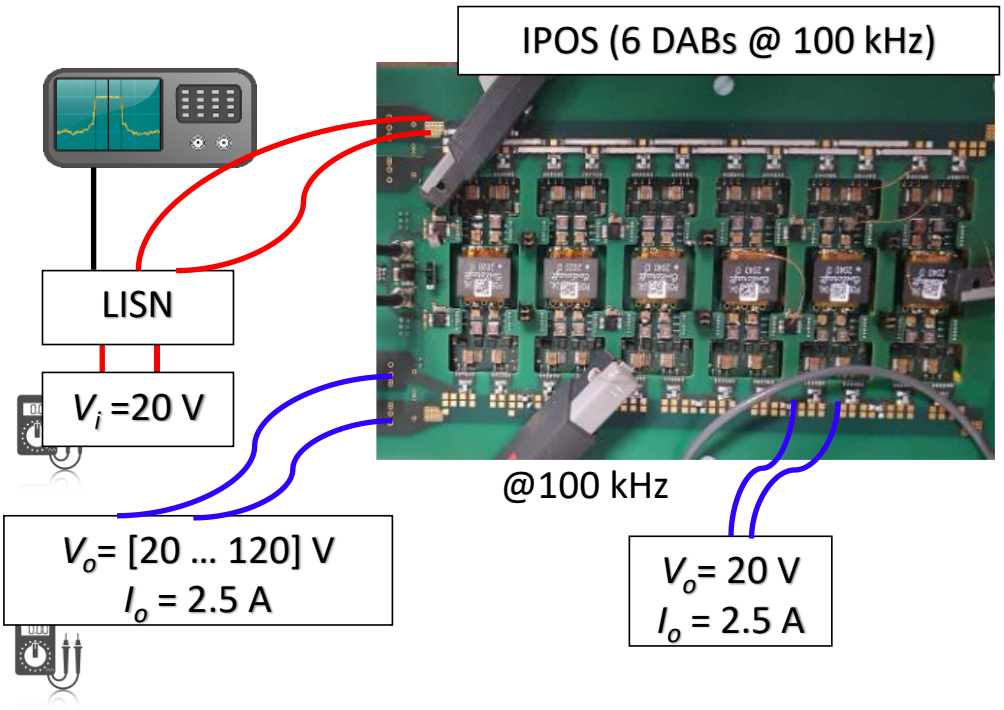


Figure 5.14 Prototype (PCA 3.0) and setup used for conducting the experimental result.

5.3.1.1 IPOS (increasing the number of CSCs) – no interleaving

A diagram setup of the experimental results performed by varying the number of CSCs in IPOS configuration with no interleaving is presented in *Figure 5.15*. The experimental results is then portrayed in *Figure 5.16*. As explained in subsection 5.2.1.1(No CM filter solution), notice that the CM noise tends to increase with the increase of CSCs. On the hand, different from the simplified theory, such increase is observed only in the lower frequency range, practically linearly, while in the higher frequency range, (> 9 MHz), the noise does not increase (up to 60 MHz), but rather reduces compared to only one CSC in

operation. Observing in the higher frequency (> 60 MHz), the noise seems to increase when compared to the results of only one CSC in operation.

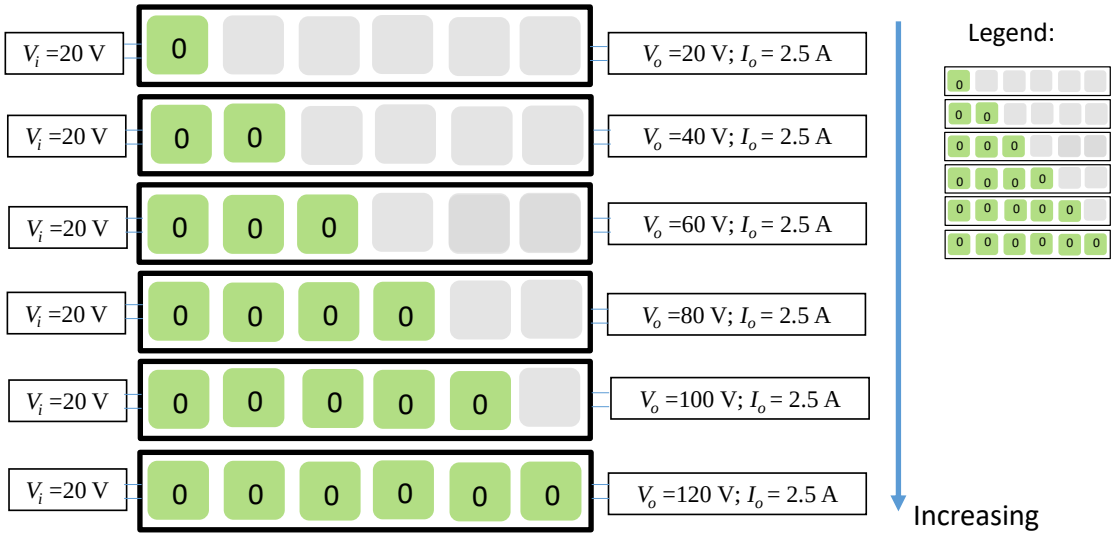


Figure 5.15 Diagram of experimental results of an IPOS configuration by increasing the number of CSCs. A legend is presented to identify the experimental results in the next figure.

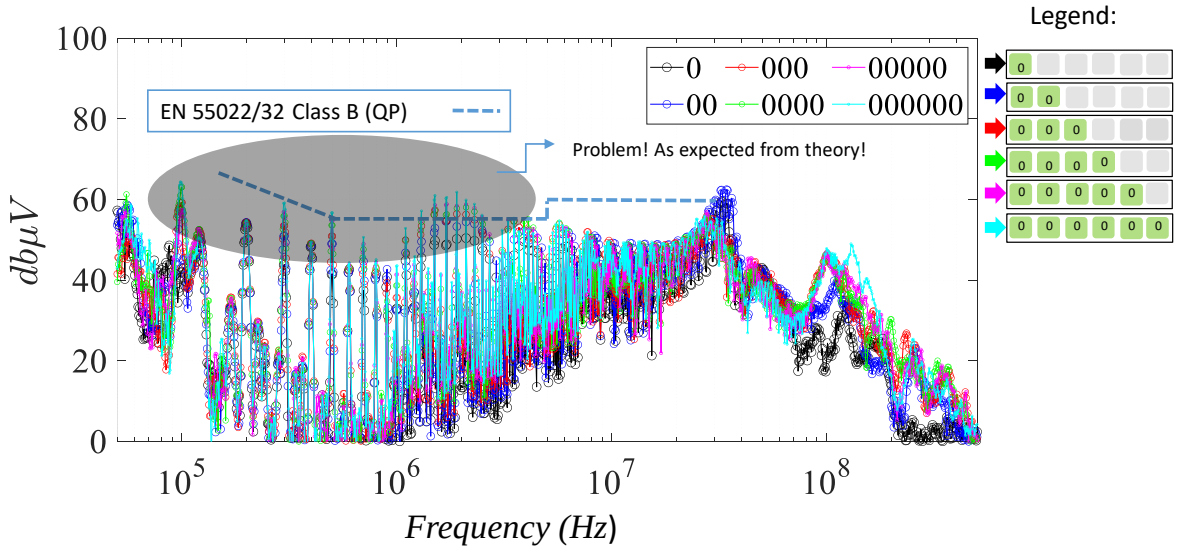


Figure 5.16 EMI Spectrum of PCA (Version 3) of IPOS configuration, increasing the number of CSCs.

5.3.1.2 IPOS and ISOP Configuration: proof of concept

For this set of experimental results, a PCA made to exclusively for maximum two CSCs is used. The ISOP and IPOS connection configurations are then tested performing both 0° and 180° interleaving, as presented in *Figure 5.17*. In *Figure 5.18*, it is presented the experimental results of the proof of concept. For both connection configurations, it shows a

30dB reduction, limited by noise floor, in lower freq. range with 180° shifting for 2 CSCs. A 20 0dB decrease observed at 30MHz. The 0° and 180° shifting have similar behaviour in higher frequency range (>30 MHz) and is not effective for reducing CM noise higher than this frequency range. The approach can effectively reduce 2 CSCs to noise floor for lower CE frequency range.

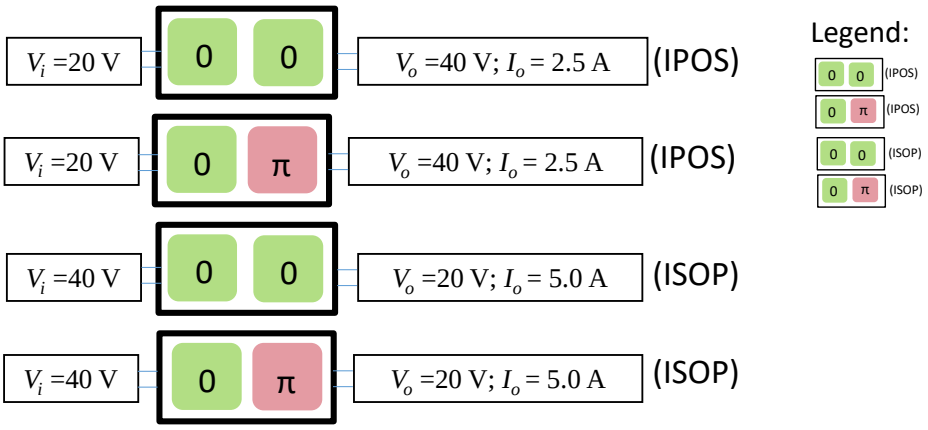


Figure 5.17 Diagram of experimental results of IPOS and ISOP configuration for proof of concept (two CSCs) applying 0° and 180° interleaving. A legend is presented to identify the experimental results in the next figure.

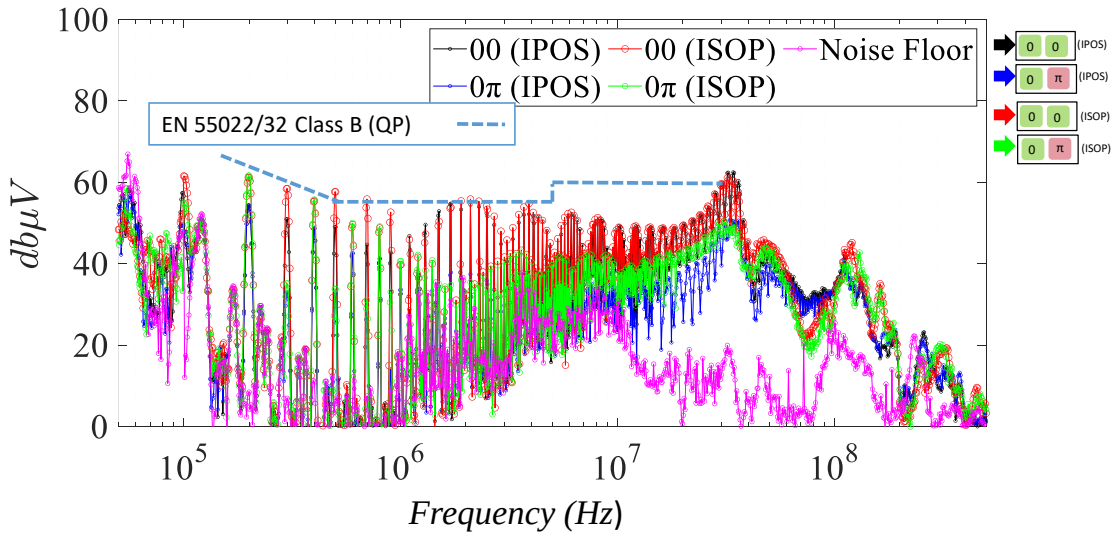


Figure 5.18 EMI Spectrum of PCA (Version 3) of IPOS and ISOP configuration (two CSCs) for proof of concept applying 0° and 180° interleaving on both connection configuration.

5.3.1.3 IPOS applying the 180° and 0° interleaving for mitigation through CM compensation

For this set of experimental results, the connection configuration is an IPOS and 180° interleaving to compensate CM noise while increasing the number of CSCs, as presented in the diagram portrayed in *Figure 5.19*. The goal is to observe the validity of the interleaving attenuation technique for any amount of CSC larger than two. Experimental results of such set of testing are then presented in *Figure 5.20*.

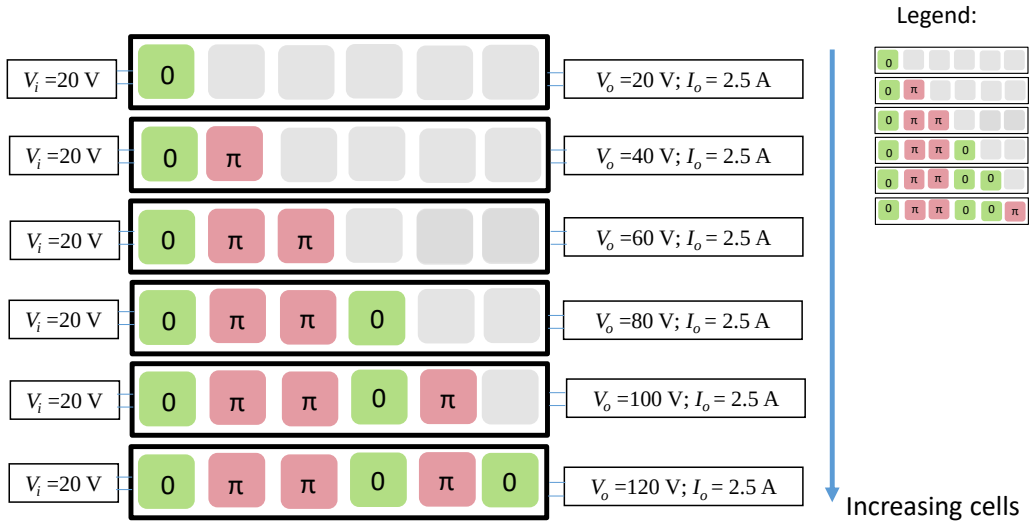


Figure 5.19 Diagram of experimental results of an IPOS configuration by increasing the number of CSCs and applying the proposed 180° and 0° interleaving for mitigation through CM compensation. A legend is presented to identify the experimental results in the next figure.

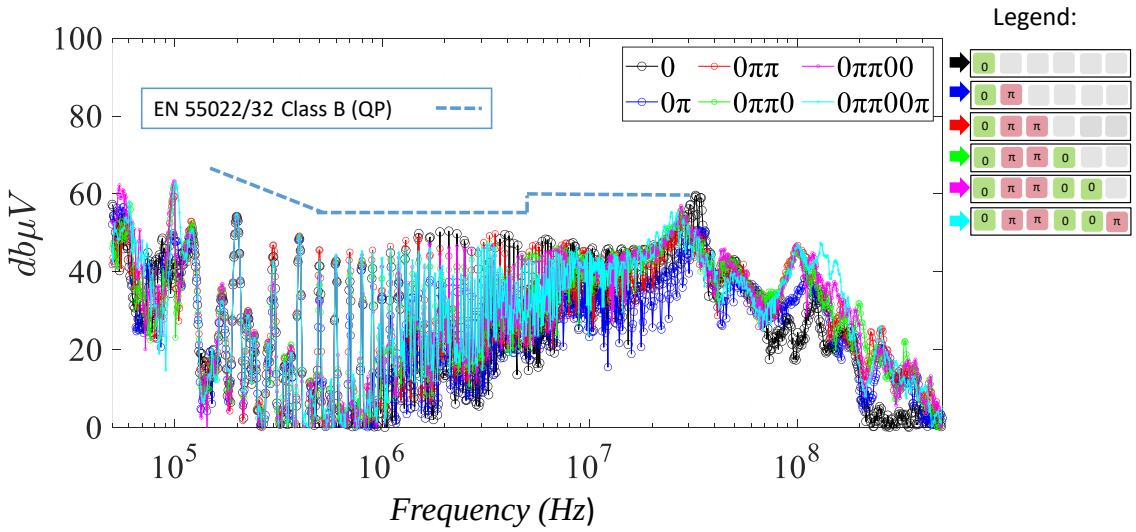


Figure 5.20 EMI Spectrum of PCA (Version 3) of IPOS connection configuration applying the proposed 180° and 0° interleaving for mitigation through CM compensation while increasing the number of CSCs up to six.

As it can be concluded, the approach allows to pass EMC compliance, without the need of a filter solution. Notice that the EMI signature tends to settle into a flat behaviour all over the frequency range without increasing the amplitude as the number of CSCs increases.

5.3.1.4 IPOS applying other interleaving combination

For this set of experimental results, different interleaving combinations are tested to observe the effect of not compensating in pair the 180° and 0°, as presented in *Figure 5.21*. The practical results are presented in *Figure 5.22*.

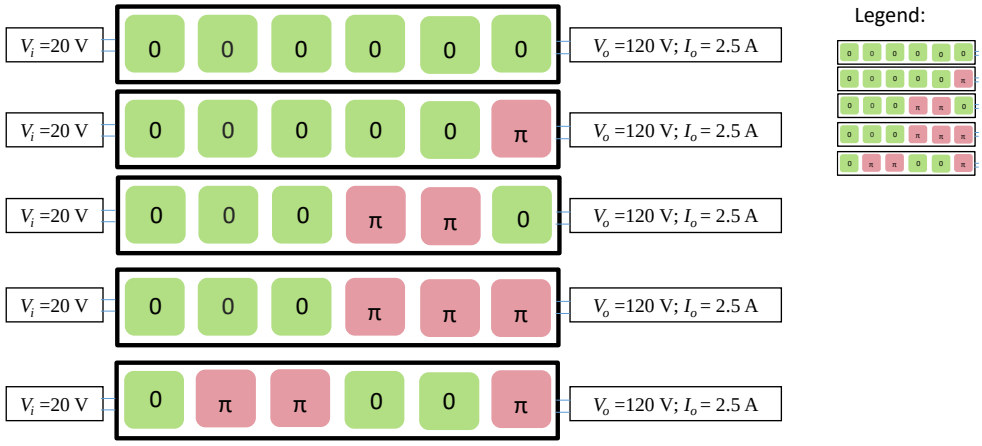


Figure 5.21 Diagram of experimental results of an IPOS configuration applying different combination of interleaving 180° and 0°. A legend is presented to identify the experimental results in the next figure.

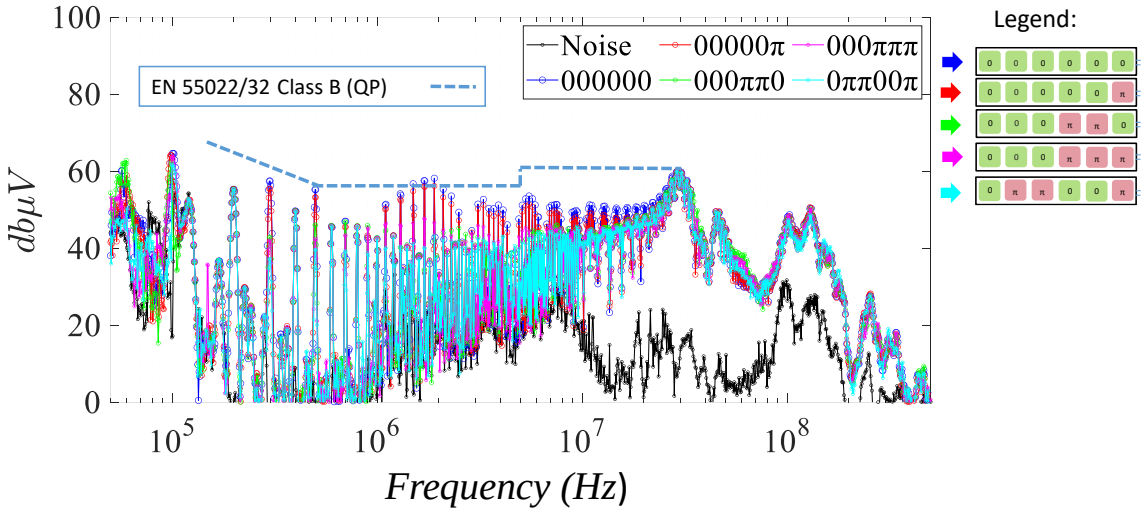


Figure 5.22 EMI Spectrum of PCA (Version 3) of IPOS configuration (six CSCs) applying different combination of interleaving 180° and 0°.

As it can be noticed, if the interleaving 0° and 180° are not equally shared, the CM noise attenuation is worsened. Also, notice that if compensation interleaving are performed as close as possible (light blue), CM noise is better attenuated, compared to a far compensation (purple).

5.3.1.5 IPOS vs ISOP (six CSCs)

Finally, for this set of experimental results, the ISOP connection configuration applying the 180° interleaving and no interleaving is tested, as presented in *Figure 5.23*. Plotting results of ISOP and previous IPOS configuration are then presented in *Figure 5.24*. AS previously observed, the attenuation works for both connection configuration. Notice that, more noise is observed in ISOP configuration, when compared to IPOS. More investigation is, therefore, required to comprehend such behaviour.

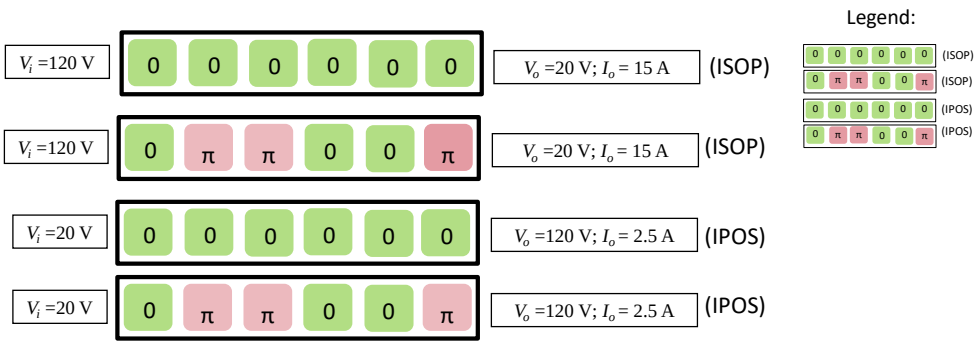


Figure 5.23 Diagram of experimental results of IPOS and ISOP configuration (six CSCs) applying no interleaving and 180° interleaving approach. A legend is presented to identify the experimental results in the next figure.

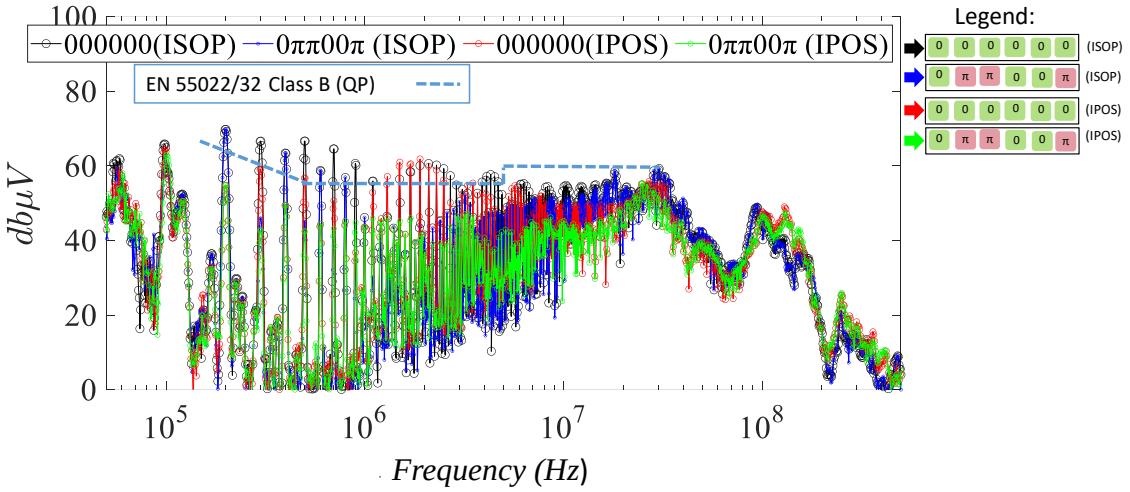


Figure 5.24 EMI Spectrum of PCA (Version 3) of IPOS and ISOP configuration (six CSCs) applying no interleaving and 180° interleaving approach.

5.4 Chapter's Final Conclusion and Perspectives

The study conducted a comparison between centralized and distributed filter solutions for power converters and found that, in ideal conditions, both solutions provide similar performance for equivalent-energy systems. However, the study found that the distributed solution performs better in high-frequency applications due to its ability to handle parasitic elements better. The use of modified parameter of insertion loss based on T-parameters showed to efficient to draw conclusions and could be improved by considering parasitic impedance paths. It can be concluded that the IS configuration is the over dimensioning factor in a standardized designing space for DM attenuation, while the IP configuration is the over dimensioning factor for CM attenuation

The study also evaluated the effectiveness of a 180° shifting approach in reducing common-mode noise in multi-cell power converters. The filter(less) approach proved to be effective in reducing the CM noise for the lower frequency range, up to 30 MHz. It is interesting to notice that, as the number of CSCs increases, so does the residual noise, which could possibly be explained by the noise generated by the gate driver.

At some point for a certain number of CSCs (30 e.g.) the approach might not be enough for passing the EMC standards due residual noise increasing. The approach could be improved with a careful gate driver tuning and further investigation on residual noise. If the filter topology of DM noise require inductances, it could also be advantageous for keeping a groundless (without access to PE) solution, but further investigation is required, since the insertion loss only improves after a resonance frequency between the inductance and parasitic capacitances. If Cy can be used through the CSCs, then the challenges to pass EMC standards are reduced, but one must take into account possible undesired resonances.

The combination of conventional interleaving for DM attenuation and the proposed 180° for CM attenuation can be used. This can solve the problem of IS configuration over dimensioning factor. The increasing in number of CSCs, indefinitely as in a PCA approach seems to be always over dimensioning the possible designing spaces.

Reference Chapter 5

[1] T. Lamorelle, Y. Lembeye, and J.-C. Crebier, "Handling Differential Mode Conducted EMC in Modular Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5812–5819, Jun. 2020, doi: 10.1109/TPEL.2019.2947735.
[2] T. Lamorelle, "Contribution à la conception et la production automatique en électronique de puissance via les réseaux de convertisseurs," p. 158.
[3] M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, "Design of a Highly Efficient (97.7%) and Very Compact (2.2 kW/dm ^{3}) Isolated AC–DC Telecom Power Supply Module Based on the Multicell ISOP Converter Approach," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7750–7769, Oct. 2017, doi: 10.1109/TPEL.2016.2633334.
[4] M. Kasper, "Analysis and Multi-Objective Optimization of Multi-Cell DC/DC and AC/DC Converter Systems," ETH Zurich, 2016. doi: 10.3929/ETHZ-A-010836609.
[5] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002, doi: 10.1109/TIE.2002.803174.
[6] M. Kasper, D. Bortis, and J. W. Kolar, "Scaling and balancing of multi-cell converters," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Hiroshima, Japan: IEEE, May 2014, pp. 2079–2086. doi: 10.1109/IPEC.2014.6869875.
[7] "Yan et al. - 2021 - Building Common-Mode Analytical Model for Dual Act.pdf."
[8] S. Kumar, S. K. Voruganti, B. Akin, and G. Gohil, "Common-Mode Current Analysis and Cancellation Technique for Dual Active Bridge Converter Based DC System," *IEEE Trans. on Ind. Applicat.*, vol. 58, no. 4, pp. 4955–4966, Jul. 2022, doi: 10.1109/TIA.2022.3173895.
[9] K. Zhang, Y. Zhou, Y. Zhang, and Y. Kang, "Reduction of Common Mode EMI in a Full-Bridge Converter through Automatic Tuning of Gating Signals," in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, Shanghai, China: IEEE, 2006, pp. 1–5. doi: 10.1109/IPEMC.2006.4778046.
[10] Y. Han, G. Li, H. Shi, and X. Wu, "Analysis and Suppression of Common-Mode EMI Noise in 1 MHz 380 V-12 V DCX Converter With Low NFoM Devices," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7903–7913, Jul. 2021, doi: 10.1109/TPEL.2020.3042632.

6. Prediction, Optimization and Perspective of Radiated Emission of Power Converter Arrays for Automated Design

As the typical switching frequencies of power converters are continually increasing with the adoption of WBG devices with very high *di/dt* and *dv/dt*, the modelling of their conducted and radiated emissions becomes very important for standard compliance and self-immunity. Specifically, the EMI radiated models of power converters [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14] are important approaches for prediction of EMC compliance, human exposure [15] and safe converter performance. They can be separated into far field [1]-[4] and near field [5]- [14]. According to [3], they are differentiated by a distance r between the observation point and the radiation source: far field is defined when $r >> \lambda/2\pi$, whereas near field is defined when $r < \lambda/2\pi$, where λ is the wavelength.

The far field, not treated in this paper, is the one that concerns EMC compliances, e.g. CISPR/EN 55022/32, that defines limit values for the harmonic spectrum ranging from 30 MHz to 40 GHz. The source of the far field is mostly predominant from Common Mode Currents (CMC), usually on the very high frequency range, flowing across the input and output cables [1], and are directly proportional to the length of the conductors [4].

The near field are produced by current loops, therefore, mostly predominant from *di/dt* of DMC, rather than CMC, being directly proportional to the area of the current loop [4], [5]. As explained in Chapter 1, the near field cartography [16] is nowadays not submitted to EMC standard compliances. However, they play an important role when spatially locating the CSCs as well as the peripherals of a PCA nearby its near field, such as driver boards and their signal paths, signal conditioning and sensor devices, and even passive filters [17], susceptible to undesirable couplings, causing malfunctioning [4] and performance degradation in analogical signals [14]. Indeed, when dealing with multi-cell converters, the main question that must be solved, or at least asked, is if the interaction among many noise sources, such as inter-cell influences may cause malfunctioning due to cross talking.

On the other hand, once again, it is an opportunity to develop theoretical and experimental (through experimental platforms) approaches, which may be used to study and optimize, in advance and detached from the CSCs as well as previous prototype fabrication,

through systematic concepts, rules and methodology. In this way, the EMI signature is expected to be predictable and improved through simple concepts and evaluation platforms. Probably, just as much as the CM noise was treated actively, the geometric and electric configuration of CSCs and their interconnections could improve both the near and far radiated field. This turns what is considered an "issue" in the current literature of inter-cell influences into an advantageous feature, found only through multi-cell converter approach and not yet explored in the literature.

Moreover, through experimental setups, it is an effective way for diagnosing [13] and characterizing [9], [10], [11] spatially the sources of radiation produced by power converters, and its correlation with the electrical parameters of the power converter itself, e.g. ZVS operation and important resonances. Indeed, the near field, either electric or magnetic, is an image of the far field, in which transformation formulas may co-relate and predict or even determine [18] the far field out of near field measurements. One can think that experimental near radiated characterization as tools for better comprehending and investigating the signals generated by a power converter, just like magnetic resonance imaging (MRI) or stethoscopes are used for living creatures. The homogeneity provided by PCA and standardized functions takes once again a significant advantage over heterogeneous solutions, as diagnosing anomalies or just EMI signature regarding Radiated Emission (RE) are generally simplified.

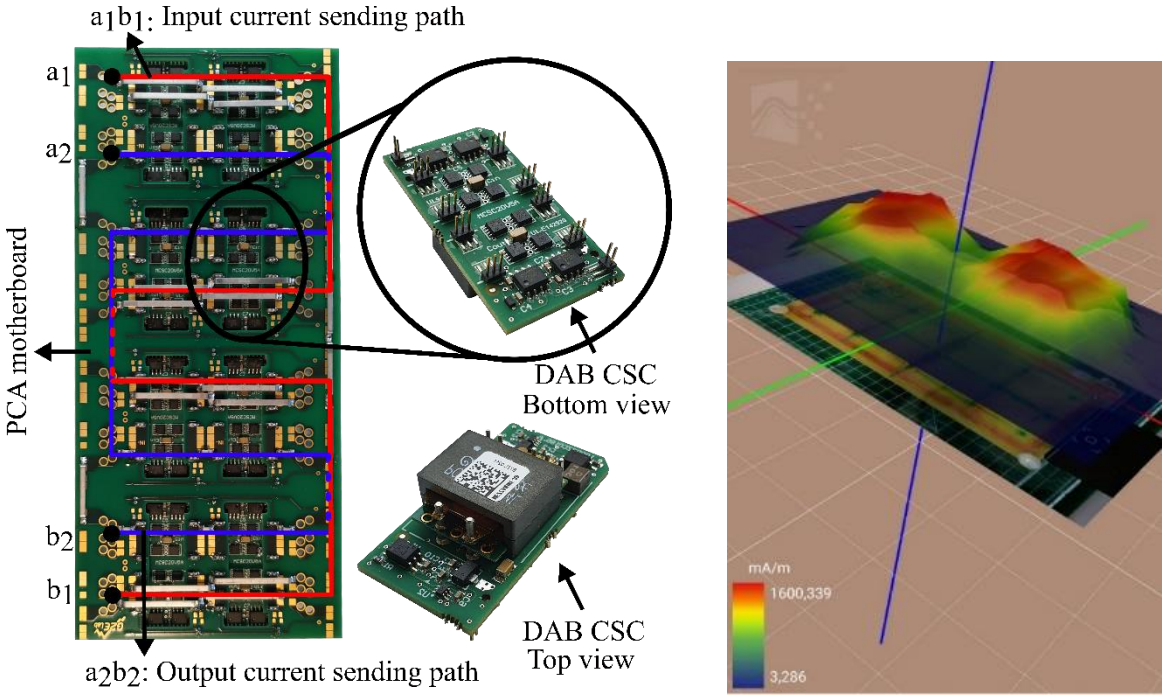
In addition, trendy topics such as Internet of things (IoT) [19] using magnetically coupled communication technologies NFC [20] requires detailed knowledge of the emitted near field to avoid interferences and needed shielding. Therefore, the prior knowledge of the near field helps defining the good location and possible shield needs of the peripherals contained in a PCA, being it a trendy future topic of power electronics.

6.1 Impact of the interconnections

Regarding EMC, a particular challenge and intrinsic characteristic of multi-cell converters is the impact of their interconnections (bus bars) on RE. This is because, different from conventional power converters (except power modules), the interconnections can work as antennas through undesirable couplings, impacting on RE and immunity. For convenience, the notation PCA_{LxC}, is used throughout this paper, in which L and C are the number of lines and columns that composes the PCA, respectively. *Figure 6.1* (a) presents an example of PCA_{4x2} composed of low power and low voltage DAB CSCs operated at approximately 250

kHz, designed and manufactured in volume in previous works (Version 1); and *Figure 6.1 (b)* , a measured near field produced by a PCB that mimics the interconnections [21].

.



(a) *(b)*

Figure 6.1 (a) (left) A 800W step up DC/DC PCA4x2 (IPOS) prototype (bottom view) highlighting the input (red) output (blue) current sending paths and (middle) a 100W 20V/5A DC/DC DAB CSC Version 1 prototype (bottom and top view); (b) Measured near field produced by a PCB that mimics the interconnections of a PCA_{4x3} [21].

Indeed, as presented in *Chapter 5*, different filter design solution (centralized and / or distributed) may induce more or less noise generation according to its choice. If an only centralized filtering solution is proved effective, large high-frequency harmonic content will circulate across the interconnections, whereas if distributed filtering solution is chosen, less harmonic content is expected circulating in the interconnections, and DC current may be assumed.

The impact on filter design configuration and interconnections should, therefore, be evaluated all together, as exemplified in the diagram presented in *Figure 6.1*. The different possible combinations to close PCA's interconnection loops, and therefore, different geometric loop combinations, can directly influence the resulting near field.

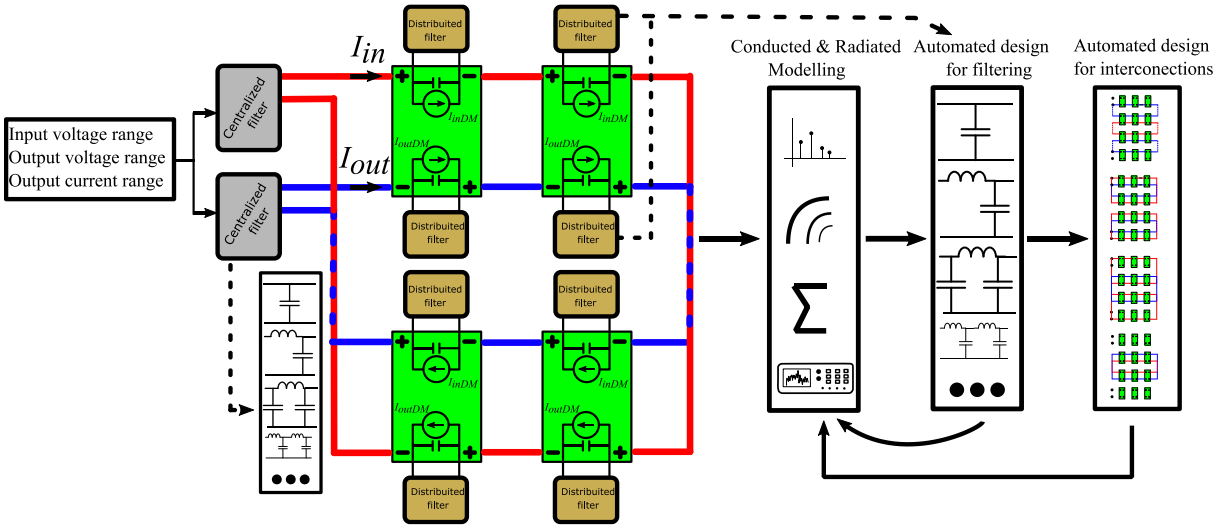


Figure 6.2 Example of a concept of automated design for EMI compliance based on PCA approach (e.g. PCA2x2 ISOS): filtering and routing are optimized with respect to EMC compliance based on experimental and theoretical characterization [21].

In [5], it is verified that the bus bars of SiC Power Modules are the ones affecting the most on the near field, mostly on the z-axis; and it is shown how such predicted field can be used to find the needs of locally shielding or immunizing sensitive devices. As it is discussed in the reference, guidance is already presented: firstly, dynamic current balancing (that can be improved with circuit symmetry and distributed driving approaches), and, secondly, physical interleaving of positive and negative bus bars.

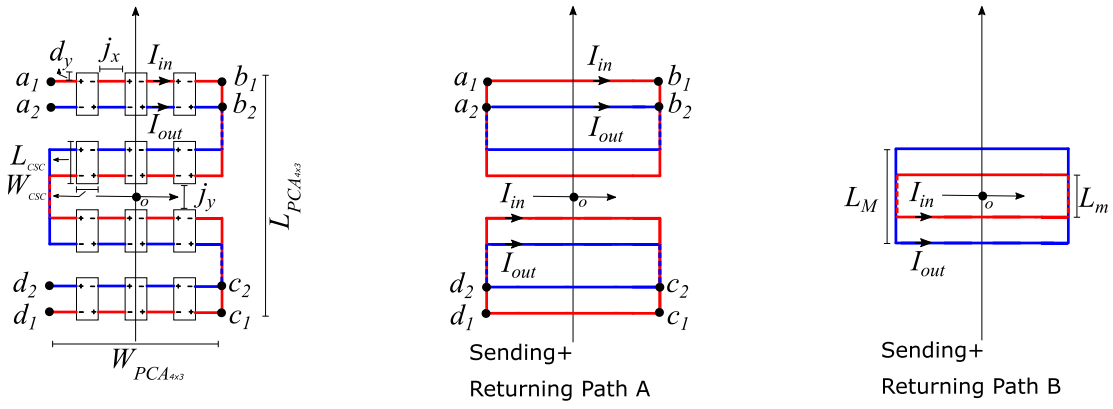
In a first analysis, only Differential Mode Current (DMC) in the lower frequency range are considered, as they are assumed to affect more drastically the near magnetic field. Four possible combinations are the object of discussion presented here. To simplify the analysis, only DMC made of several DABs are considered. This Section consists on developing a generic modelling routine for the prediction and optimization of the near magnetic radiated emission produced by DMC in the interconnections of multi-cell converters, more precisely PCAs in 2D. The PCAs are based on associations of DAB CSC for low and medium power applications as an exemplified case, but are not limited to it, and at certain cases (interconnection studies), can be detached from the converter-cell. They are built, assembled and interconnected based on PCB technologies. For simplification purposes, the discussion presented throughout this Chapter makes some electrical neglects and assumptions:

- CMC harmonics are neglected, meaning that either each CSC has a CM filter on its input and output that entirely suppress CMC, or that, at the observed frequency band, CM harmonics are negligible;
- Thus, resulting only in DM currents (which can be partially filtered locally or from a centralized point of view). If only centralized filter is assumed, all the DM harmonics are circulating in the PCA interconnections. If partially locally filtered, less harmonics are circulating in the loops;
- All CSCs are considered identical and supposed to generate the same conducted emission contents. Besides, the CSC presents a rotational symmetry, due to the DAB topology inherited feature as well as due to a PCB routed purposely designed;
- The series and parallel connections are inserted on the same paths. Notice, however, that parallel connections will increase the current ratings, and therefore, larger near magnetic field emission;
- The phase-shifts between input and output harmonic currents are neglected;
- Magnetic elements and MOSFETs switching cells radiated emissions are ignored. In practice this means that these components are locally shielded, or that superposition theorem can be further applied;
- Only outer interconnecting loops are considered, meaning that inner loops are small enough for not considering their effects, or that superposition theorem can be further applied;
- Frequency dependent and parasitic effects are not evaluated. Such scenario for the DAB is roughly approximatively for operation within the ZVS region and an optimized layout is assumed;
- No mutual coupling between input and output currents is computed, and its effect is neglected. This means that the loops are considered to be fed by independent current sources, which is the case for DMC.

With respect to the loops, simplification statements that allow meaningful and standard solutions results are also assumed. In *Figure 6.3*, it is presented an example of the loop patterns present on an ISOS PCA4x3 that summarizes the following:

- Only 2D segments on predefined orthogonal paths are allowed;

- Even though multiple segments occupy same position or cross by, no short-circuit is produced. This can be interpreted that, in practice, the segments are located only close enough at in any plane;
- Opposite magnetic fields due to opposite current directions very close to each other will cancel out the resulting near magnetic field emission;
- There are only 2 returning path options available. The returning path A – through the PCA's left-hand side, and the returning path B – through the PCA's right-hand side;
- Thus, forming 2 patterns of current loops, larger or smaller rectangular shape, depending on the input and output current paths (see *Figure 6.3 (b*), (c)), which their sizes can be expressed with respect to PCA's characteristics;
- All the DMCs must return to their origin points. The point a1, for input DMC and a_2 for output ones;
- Specifically, a returning path A causes a larger loop for the input current and a smaller loop for the output current, while a returning path B causes smaller loop for input current and larger one for output current;
- Each CSC can be positioned only vertically, and they can only rotate 180° over the z-axis, keeping their electrical and physical characteristics unaltered.



(a) *(b)* *(c)*

Figure 6.3 (a) Example of the assumed input (red) and output (blue) current sending paths of typical ISOS PCA_{4x3}; (b) The equivalent resulting interconnect loops by connecting through the PCA's left-hand (path A); (c) The equivalent resulting interconnects loops by connecting through the PCA's right-hand (path B) [21].

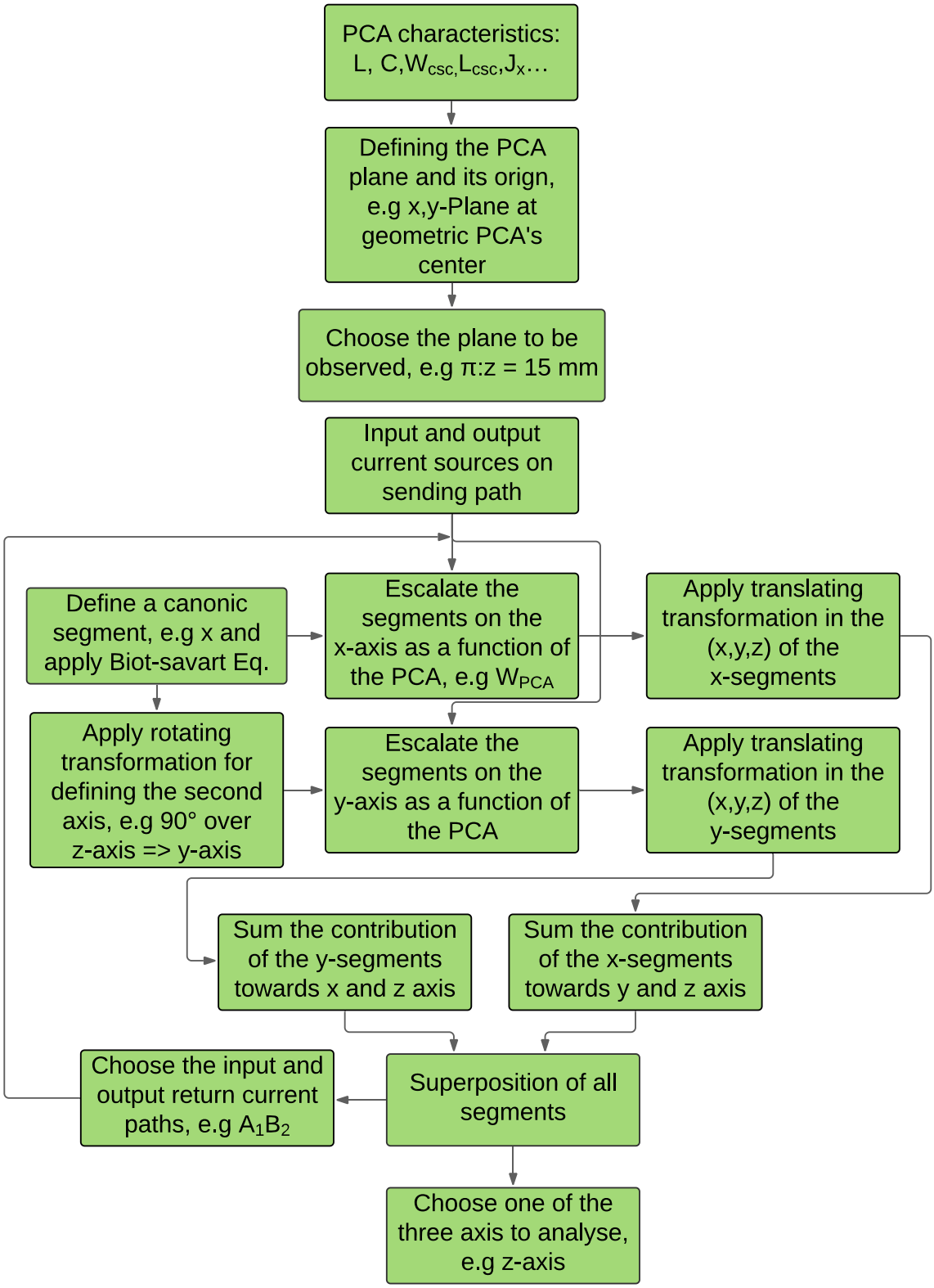


Figure 6.4 A straightforward algorithm for near magnetic radiated field prediction of PCA's interconnections based on Biot-Savart law [21].

Because of such simplifications and imposed rules, two current loop patterns can be produced, in which one of them is much larger than the other one). Therefore, a total of four different combinations, as presented in Figure 6.5, are analysed and compared among each other.

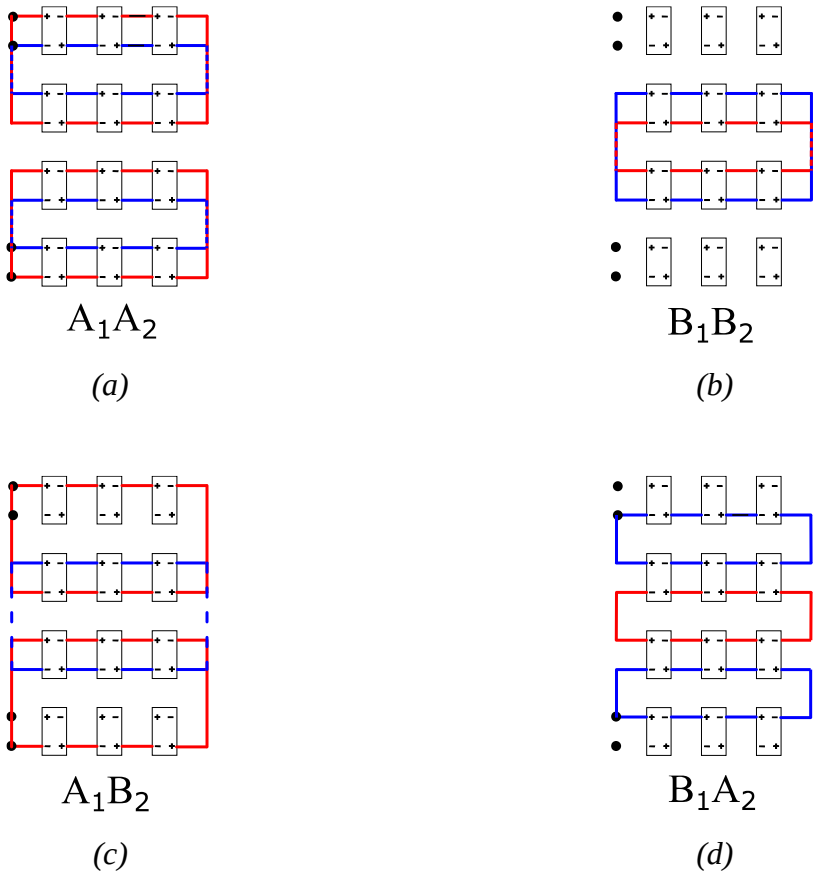


Figure 6.5 Four different interconnection architectures and their resulting simplified geometries: (a) A_1A_2; (b) B_1B_2; (c) A_1B_2; (d) B_1A_2.

Once again, analytical results are developed and preferred for easier and quicker analysis implementation. Therefore, an algorithm based on Biot-Savart law [25], [24] and the physical and electrical configurations of a PCA is provided to develop generic models. Inspired by the use of coordinate transformations, highly used for example on computer graphics, it is possible to express the magnetic field of a set of finite wires that have any directions or lengths over the PCA plane. Such method can be similar or considered as PEEC method [6], [26], [17] in which the need of subdivision into smaller elements is not necessary, as in a FEM, and, therefore, quicker to generate results.

Initially, a finite segment located at the origin on the *xy*-plane and with positive *x*-direction, as presented in *Figure 6.6* is well defined. As presented in [25], [24], the magnitude of the magnetic field density of a finite wire is calculated as presented in (6.1).

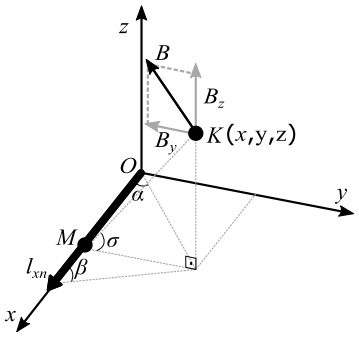


Figure 6.6 Magnetic field density induced by a canonical finite segment observed at a given point.

$$\left|B_{x\to yz}(x,y,z,I)\right| = \left|\frac{\mu_o I}{4\pi\left\|\overrightarrow{MK}\right\|}(\cos(\alpha)+\cos(\beta))\right| \tag{6.1}$$

$$\cos(\alpha)_{(x,y,z)} = \frac{x}{\sqrt{x^2+y^2}} \tag{6.2}$$

$$\cos(\beta)_{(x,y,z)} = \frac{l_{xn}-x}{\sqrt{(l_{xn}-x)^2+y^2}} \tag{6.3}$$

$$\left\|\overrightarrow{MK}\right\| = \sqrt{x^2+y^2} \tag{6.4}$$

Where:

- I is the RMS value of the circulating current (A);
- l_{xn} is the length of the nth *x*-oriented segment (m);
- α and β are the angles according to Figure 6.6;
- (x,y,z) is the observed point;
- $\overrightarrow{MK}$is the vector according to *Figure 6.6.*

Then, the component vector on the *y*-, *z*- axis are presented in (6.5)

$$B_{x\to yz}(x,y,z) = \left|B_{x\to yz}(x,y,z)\right|\left(0, S_a\sin(\sigma)_{xy}, S_b\cos(\sigma)_{xy}\right) \tag{6.5}$$

$$\sin(\sigma)_{(x,y,z)} = \frac{z}{\sqrt{z^2 + y^2}} \tag{6.6}$$

$$\cos(\sigma)_{(x,y,z)} = \frac{y}{\sqrt{z^2 + y^2}}. \tag{6.7}$$

Where S_a and S_b are positive and negative signs obtained from right hand thumb rule, that depends on the direction of the current flow. For the canonical case here presented, they are adopted negative and positive, respectively.

Once a canonical as simple as a finite segment has been defined, translation coordinate transformations [26], can then be applied for all the nth segment of the PCA oriented in the *x*-axis (6.8)

$$\mathrm{T}_x\big(x, y, z, l_x(n)\big) = \begin{pmatrix} l_x(n) \\ x - \Delta_{xx}(n) \\ y - \Delta_{xy}(n) \\ z - \Delta_{xz}(n) \end{pmatrix}. \tag{6.8}$$

Where:

- $l_x(n)$ is the length of the nth segment in the *x*-direction;
- $\Delta_{xx}(n)$ is the shift of the nth *x*-segment in the *x*-direction;
- $\Delta_{xy}(n)$ is the shift of the nth *x*-segment in the *y*-direction;
- $\Delta_{xz}(n)$ is the shift of the nth *x*-segment in the *z*-direction (always considered zero in this work).

In order to obtain a canonical segment on the *y*-axis, and later compose and assemble entirely the 2-D segments of a PCA, it is possible to easily apply the equations so far presented in (6.1) - (6.7) into (6.9), resulting in (6.10). Such transformation is the same as the rotating transformation coordinates of 90°

$$R(x, y, z) = \begin{pmatrix} y \\ x \\ z \end{pmatrix} \tag{6.9}$$

$$B_{y\to xz}(x, y, z, I) = \left|B_{y\to xz}(R(x, y, z), I)\right|\left(S_c \sin(\sigma)_{R(x,y,z)}, 0, S_d \cos(\sigma)_{R(x,y,z)}\right). \tag{6.10}$$

Where again, S_c and S_d are signs that depend on the direction adopted for the current flow. For the case here presented, the current flows into the negative direction of the y-axis presented in Figure 6.6. Therefore, S_c and S_d are negative and positive, respectively.

Then, as previously for the *x*-segments, translation coordinate transformation may be applied for the *y*-segments, as presented in (6.11)

$$\mathrm{T}_y\left(x, y, z, l_y(n)\right) = \begin{pmatrix} l_y(n) \\ x - \Delta_{yx}(n) \\ y - \Delta_{yy}(n) \\ z - \Delta_{yz}(n) \end{pmatrix}. \tag{6.11}$$

Where:

- $l_y(n)$, is the length of the nth segment in the y-direction;
- $\Delta_{yx}(n)$ is the shift of the nth y-segment in the x-direction;
- $\Delta_{yy}(n)$ is the shift of the nth y-segment in the y-direction;
- $\Delta_{yz}(n)$ is the shift of the nth y-segment in the z-direction (always considered zero in this work).

The objective, and main added scientific value remain to define the transformation functions T_x and T_y that will depend on the architecture of the PCA and its number of CSCs. These functions are analytically derived and presented in Appendix 6.A

Due to the symmetry on both *x*-axis and *y*-axis, it is possible to evaluate the effect of the field by plotting ¼ of each quadrant. In Figure 6.7, it is presented the *z*-component results for all four combinations over the plane π: z = 20 mm, whereas *Figure 6.8* presents the plotting results of the magnitude value over the same plane.

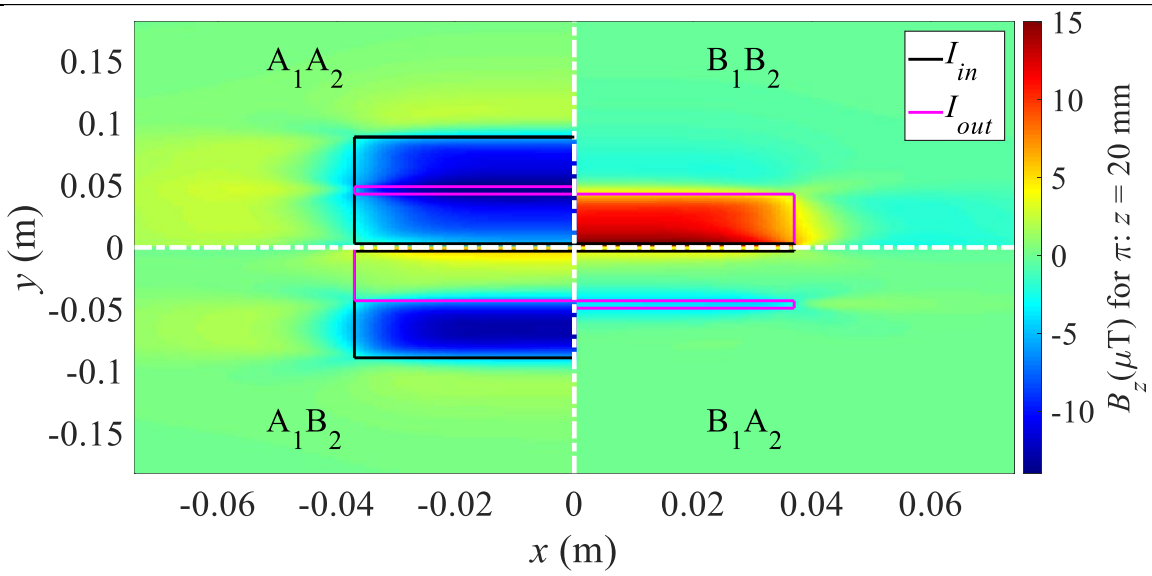


Figure 6.7 z-components of the magnetic field results produced by all 4 loop combinations of a PCA4x3 over the plane π: z = 20 mm. Thanks to symmetry over x, y-axis only ¼ of each quadrant are plotted [22].

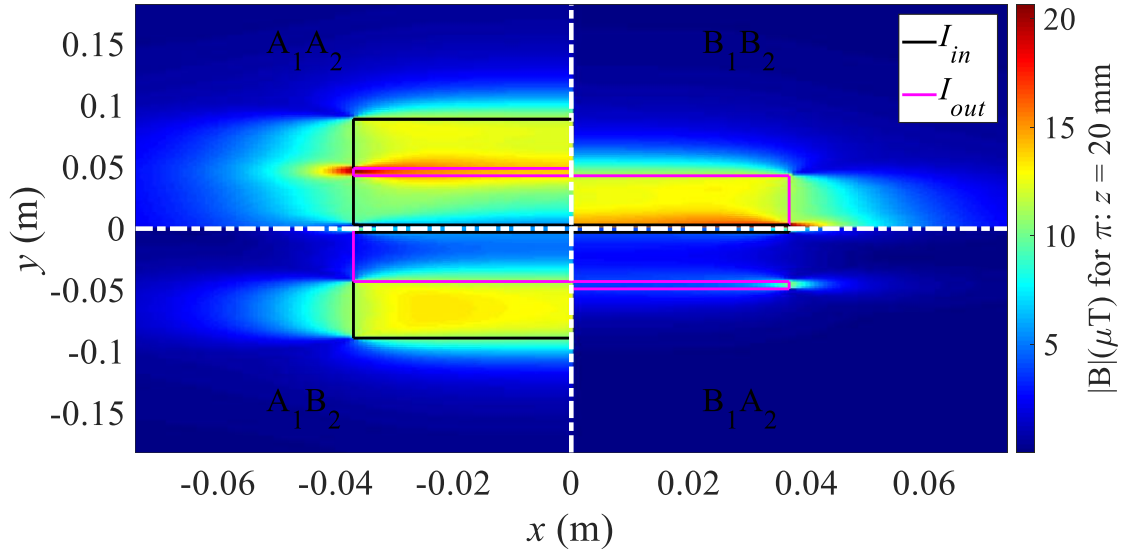


Figure 6.8 Magnitude of the magnetic field results produced by all 4 loop combinations of a PCA4x3 over the plane π: z = 20 mm. Thanks to symmetry over x, y-axis only ¼ of each quadrant are plotted [22].

As a brief conclusion, the combination B_1A_2 is the most optimized one under the point of view of near magnetic field emission, while combination A_1A_2 and B_1B_2 are the worst ones. This confirms that keeping smaller loop areas is a valuable guidance / design rule.

In order to identify the tendency behaviour at further distances, it is presented in *Figure 6.9* and *Figure 6.10* the results, respectively, of the z-components and magnitude values, for the all four combination, over the plane π: z = 200 mm.

Notice that in this case, the magnetic field becomes sparser and less concentrated. It is worth noting as well that the combination B_1A_2 becomes increasingly more negligible with respect to A_1A_2 combination.

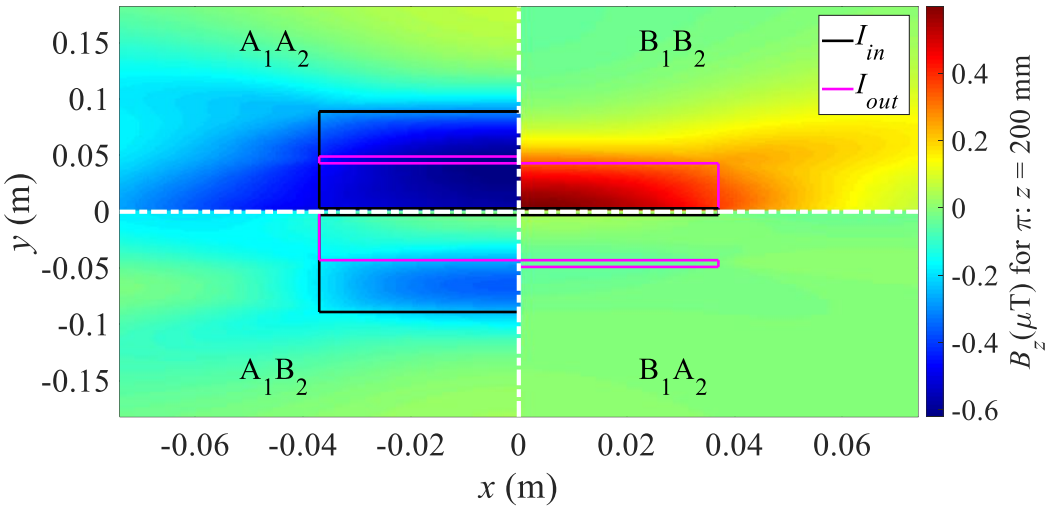


Figure 6.9 z-components of the magnetic field results produced by all 4 loop combinations of a PCA4x3 over the plane π: z = 200 mm. Thanks to symmetry over x, y-axis only ¼ of each quadrant are plotted [22].

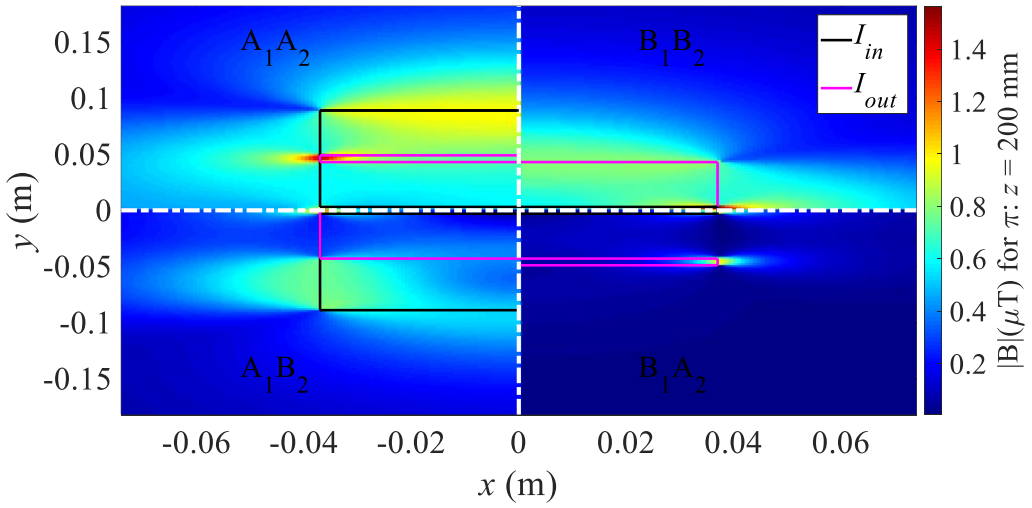


Figure 6.10 Magnitude of the magnetic field results produced by all 4 loop combinations of a PCA4x3 over the plane π: z = 200 mm. Thanks to symmetry over x, y-axis only ¼ of each quadrant are plotted [22].

6.1.1 Comparison between the proposed method and FEM

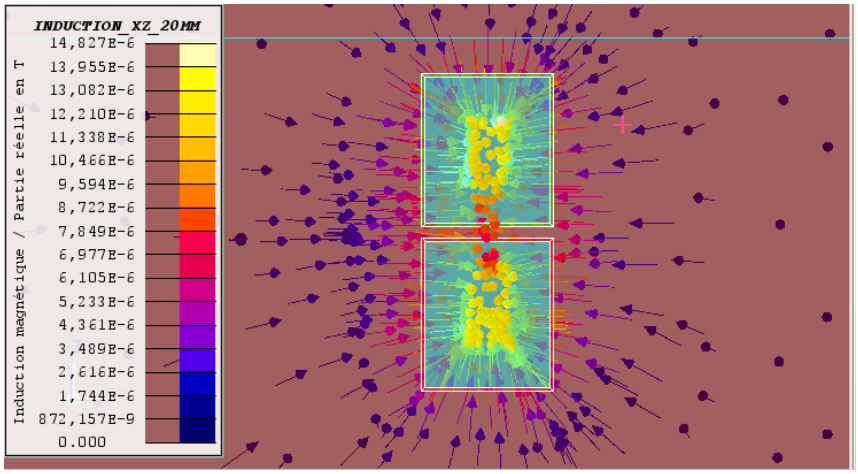


Figure 6.11 vectors and magnitude of the magnetic field FEM simulation results produced by input current loop of a PCA4x3 over the plane π: z = 20 mm considering the returning path A [22].

In order to validate the proposed mathematical modelling of the near field radiated emission, a simulation on Finite Element Method (FEM) of input DMC loop A in a PCA4x3 has been carried out as presented in *Figure 6.11* for comparison purposes.

These two comparisons validate the mathematical correctness of the proposed algorithm. Besides, most modelling assumptions seems to be valid since the FEM results do not show significant differences. It also highlights the fact that simple segmented structures should privilege analytical results. Therefore, the whole methodology can now be applied to estimate and to sketch the near field plot above and around any PCA arrangement on a 2D plane made out several CSC interconnected.

6.1.2 Partial conclusion and perspective

In this section, an algorithm and methodology for comparing the near field radiated emissions caused by PCA's DM current flowing across the interconnections assembled in four different ways has been proposed and validated theoretically through FEM theoretical results. Such algorithm, based on Biot-Savart law with simplifying assumptions and rules as function of the PCA's interconnections, is a straightforward approach that allows not only verification, but also spatial and magnitude near field emission optimization with respect to the filtering distribution, peripherals placement and shield if needed. The methodology is simple to follow and to run on optimization processes, avoiding heavy simulations, as in

FEMs, or co-simulations. It can be applied to spatially characterize the emitted near field produced from CSC's interconnections and to develop rules and guidance in order to minimize RE.

Considering 3D PCA, composed of 2D interconnections, one can easily apply same equations, and shift with respect to the z direction and apply superposition. The presented tool can help building 3D structures for inter-cell interference (and its self-immunity due to near field disturbances), or, through physical architecture and modulation, provide active shielding for reducing the RE in a general aspect. If better detail is needed, the algorithm can easily be improved with current density (surface or volume), or any other method. It is important to keep the idea that the results should be quick and insightful as well as function of PCA architecture inputs.

Just like any passive element, e.g transformers and inductors, the interconnections can be studied, designed and analysed detached from converter cell prototyping and operation. This proves the assumptions presented in *Chapter 1* that PCA approach allows designing each function block independently, including for complicated tasks such as EMC.

The algorithm is developed considering ISOS configuration, which is the worst in terms of AC DMC noise, being it proportional to the number of CSC (LxC) if no filter is considered, as presented in *Chapter 5*. For parallel connections, the algorithm can be adapted considering the magnitude through the segment path, in which current flow is not equally divided through each segment. On the other hand, it is easy to observe that parallel connections will result in close opposite currents and, therefore, narrow current loop areas. Besides, it was proved in Chapter 5 and previous work that the DMC content through the input and output ports is kept unaltered compared to single CSC, in the lower frequency (nearby the switching frequency).

With both information, it can categorically be affirmed that parallel connections produce lesser near field compared to series connection, and could be analogous for far field. If the goal remains providing one homogeneous solution for PCA that will work for all connection configuration, the ISOS could be considered as the worst case condition for EMC aspects, and, therefore, the need of adapting the algorithm for parallel connection configuration may not be crucial.

Regarding near field produced by CM currents, another algorithm could suppose current flowing of same magnitude (symmetric structures) in the appropriated direction of CM currents, that is, into a ground plane and returning through this plane using mirror theory. The assumption is especially true for the lower frequency range, in which the radiated source can still be governed by near field and Biot-Sarvat law, and for the interconnection segments

connected to the external system: see in *Figure 6.3*, for the sending current path, it is the small segment from a1 to the first cell; and for the returning current path, it comprises the entire return path either A or B. If the input and output of a PCA is designed to be connected through geometric center in a symmetrical way, the simplifying proposed aforementioned assumption is more likely to be true for all the segments. In such cases, the algorithm may be analogous to water current sinking into a downtake pipe, which is localized in the geometric center of the segments. It is easy to see the importance of a ground plane, in this case, to reduce the near field through the mirror theory, as the ground returning current will oppose each current segment and null the produced field, due the proximity of the current segments. Otherwise, with no ground returning current, it is easy to imagine that, due to same direction, the field cannot be easily cancelled, a classical and well known problem case due to CM noise currents. Therefore, for future studies, it is advised the location of input and output in geometric center as well as symmetrisation of the interconnections, since it does not imply apparently in any drawback or physical constraint (perimeter of segments are kept the same).

Regarding the far field, even though antenna theory, parasitic effect and grounding must be well comprehended, the same methodology of composing the far field emitted by known and standardized dipole antennas can be applied. Of course, it is very approximatively first assumption, since aperture, connection, cables, metal box may direct impact on the far field.

6.2 Updated motherboard plataform

Based on the conclusion drawn from theoretical (previous section) and experimental (next section), regarding the impact of the RE produced by interconnections a new rule / mother board is added. It consists on putting another level in the PCA, subdividing it in lines with a maximum number of CSCs in which a filter is mandatorily inserted. This will limit the surface area of the interconnection loops, while guaranteeing CM and DM noise attenuation through the line-localized filters. Besides, the sending (jumpers) and returning (two PCB inner copper plans) current paths occupies practically the same segments, reducing even further the RE. Also the returning path may need to be implemented with jumpers, next to the sending path, which may lead to unequal magnetic fields for cancellation. This may depend on the number of CSC, the configuration type and the CSC current rating. Moreover, it adds conducting wiring for the power current that may lead to extra conduction losses.

In fact, due to simplifying assumptions for analytical analysis (occupying same space), the near field emitted is null, and further theoretical analysis is not required. On the other

hand, for more accuracy, or when needed if verified in practice, the algorithm can easily be adapted to contain more complex details, including current segments in z-axes and surface density.

The number of CSCs per line is fixed to 6 and is not based in any specific designed criteria, but rather on results presented in [23]. Besides, for the technology in G2Elab it is also convenient for assembling with AC/DC applications, which is out of the scope of this thesis but it is a continuous simultaneous work. A diagram of the updated design rule for motherboard / interconnections is presented in *Figure 6.12*.

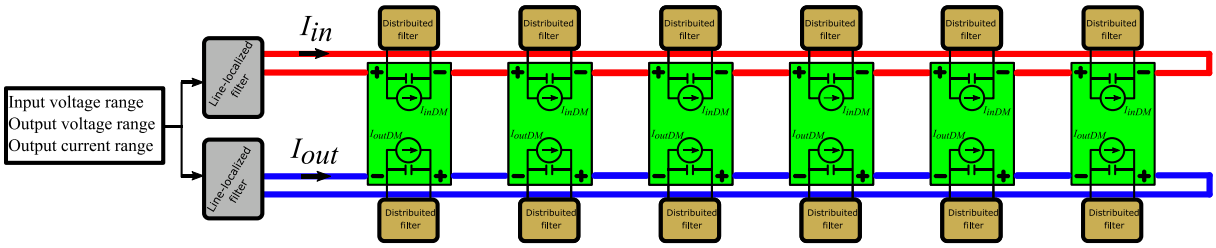


Figure 6.12 Diagram of the updated design rule for motherboard / interconnections in which a PCA is composed of line of CSCs limited to a maximum number of six.

Besides, for the updated version, the PCB footprints of a diverse set of common-mode chokes and filter topologies is implemented. The idea is to be able to realize different experimental results, including plug-and-play through the OC tests for database learning and EMC improving. The physical shifting implementation, presented in *Chapter 5*, is included in the updated version. In *Figure 6.13*, it is presented an illustration of the 3D PCB and explanation of updated motherboard used and potentially will be used in future works.

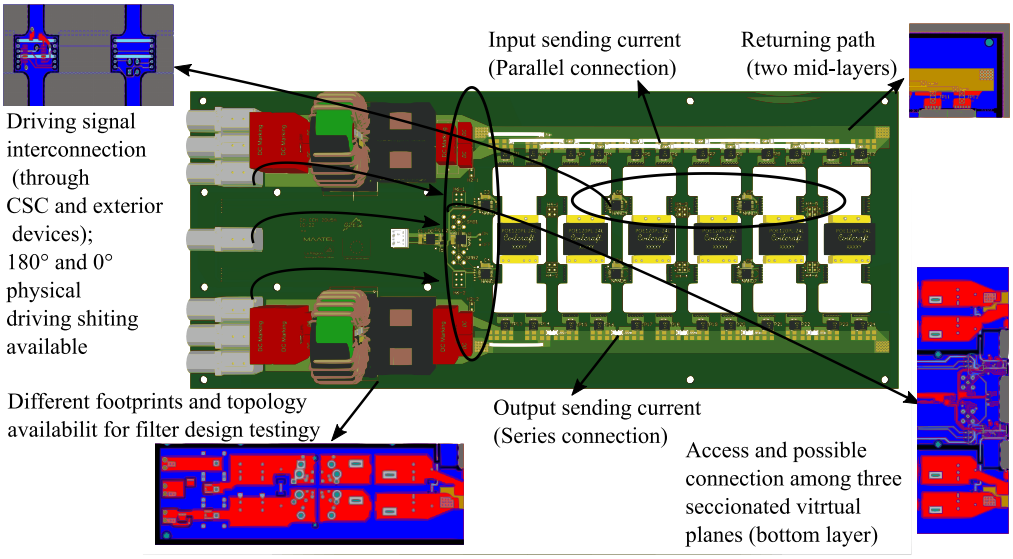
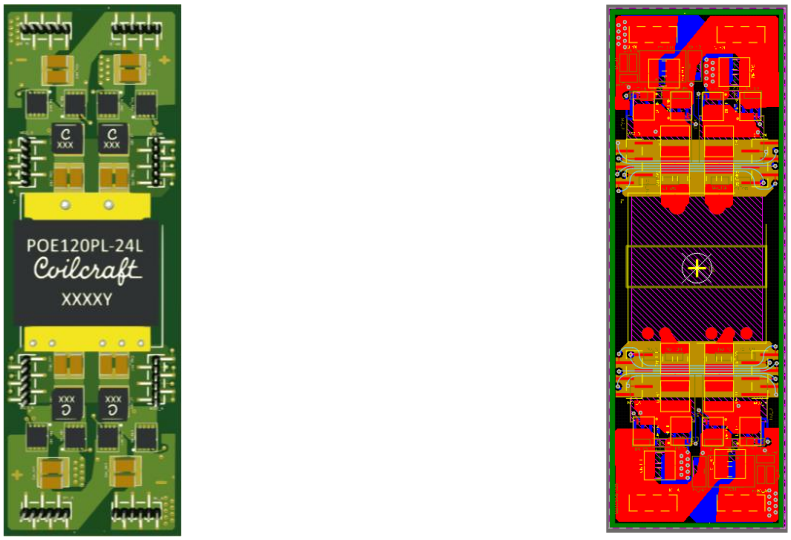


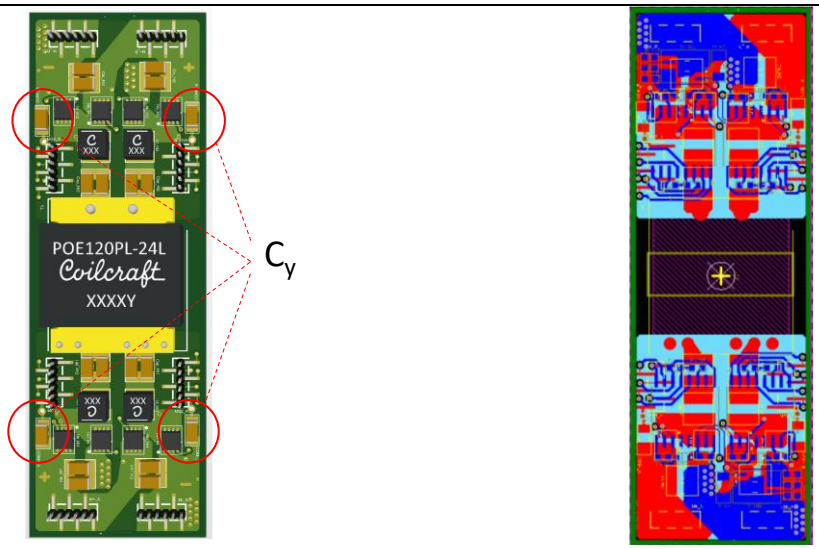
Figure 6.13 Illustrative 3D PCB and explanation of the adopted motherboard technology platform based on a 4 copper layer PCB technology. As an exemplifying case IPOS is portrayed.

In order to study the impact of a ground or virtual plan, two versions of the CSC 3.0 have actually been prototyped and tested: one with no ground plane, as presented in *Figure 6.14* ,which has been used throughout all previous and ongoing experimental results; and another one with ground plane and C_y capacitors, as presented in *Figure 6.15*, in which experimental results have been conducted. Therefore, for this *Chapter*, the DAB cell with no ground plane will be identified as CSC 3.1, while the DAB cell with ground plane and C_y will be identified as CSC 3.2.



(a) *(b)*

Figure 6.14 Dab cell with no ground plane identified as CSC 3.1 (a) 3D view; (b)2D PCB view.



(a) *(b)*

Figure 6.15 Dab cell with ground plane and C_y identified as CSC 3.1 (a) 3D view; (b)2D PCB view.

Besides the prototyped PCA_{1x6}, another one similar to the previous mentioned PCB, but only two CSCs, PCA_{1x2}, was also prototyped and tested. The goal is to study the CSCs in a more controlled environment (lesser CSCs), while being able to able to compare the effect of a smaller PCA lines.

6.2.1 Partial conclusion and perspectives

In this subsection, the updated concept version of the motherboard (interconnections) has been presented. Even though a practical comparison regarding other versions has not been performed, it is certainly a good practice to follow, as it reduces surface current loops and maximum allowed current noise (according to EMC standard compliance). If one line PCA6x1 is complying with EMC standards, including RE, other structures assembling in 2D or 3D structures considering more lines PCA6x1 will mostly comply with EMC standards more easily. Besides, if other applications require less number of CSCs, e.g, 4 or 2, the EMC compliance standard is most likely feasible without major challenge. The line PCA presented in this is a 2D structure, but other 3D (stacking 3 over 3 cells) may be studied if needed, and may be used to actively cancel RE by following opposing current segment principles.

A bulky filter solution was proposed at the time. Evolving improvement results of the CM noise showed that the need of common-mode choke is possibly not required in the final

prototype. The discussion between centralized and distributed DM filter solution is still ongoing and is left for future studies, as presented in *Chapter 5*. If distributed solution is chosen, it seems that the PCA may gain in power density as the need of different footprints and topology filter design (1/3 of the total surface) study may be not needed.

6.3 Experimental results

The experimental results concerning the near field of the interconnections are presented in subsection 6.3.1, which is related to the section 6.1. Then, with the PCA_{1x4} in operation at full load, it is presented the EM cartography in different points of the PCA in 6.3.2; and through the use of TEM, which results are presented in 6.3.3. For OC testing and comparison, please refer to

. Finally, the improved CSC 3.0 along with its PCA_{1x2} has its signature EMI acquired through TEM cell, and the discussion of 0° and 180° interleaving. Therefore, in order to be able to build a database of the near field EMI signature with the goal of correlating, observing and checking on line improvements, it is proposed the setup as presented in *Figure 6.16*.

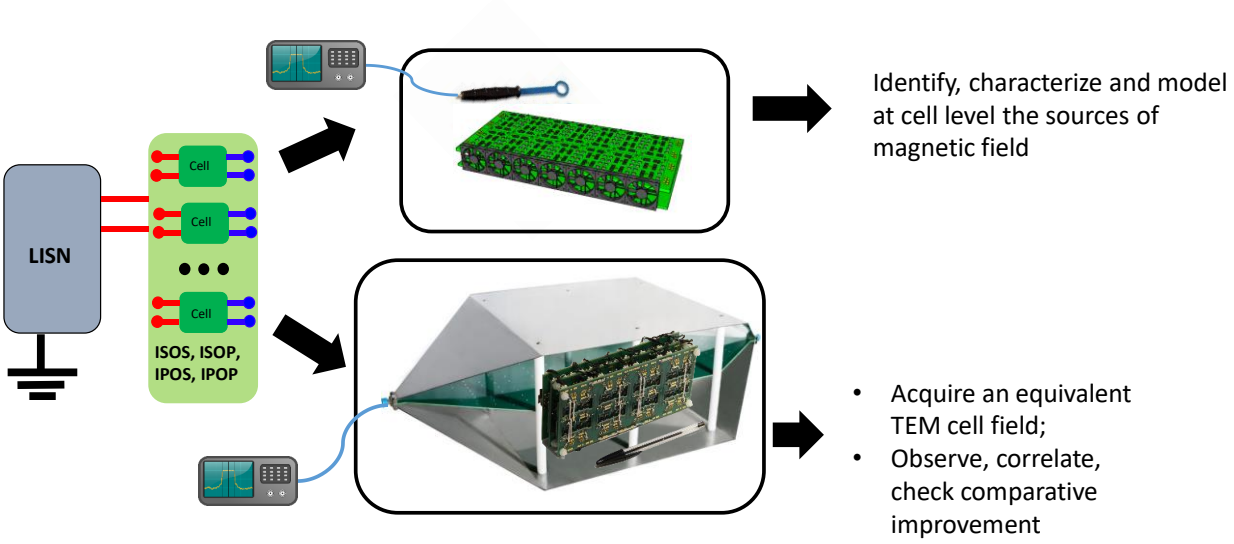
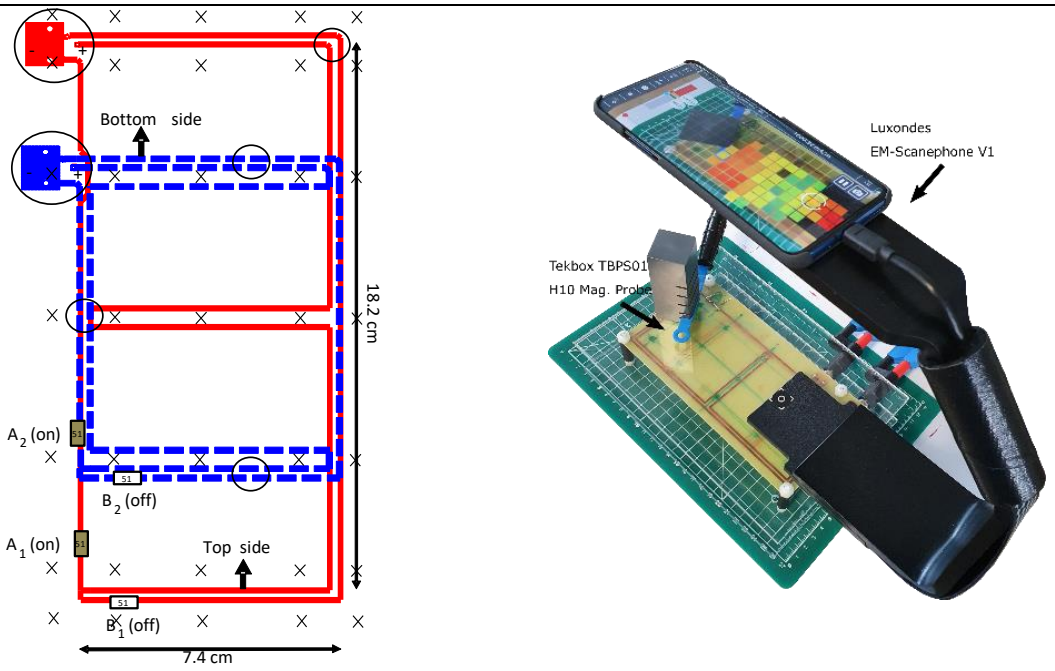


Figure 6.16 Proposed setup for acquiring near field EMI signature.

6.3.1 Mimicked interconnection loop experimental EM Cartography

An experimental setup was built with a PCB mimicking the four possible loop combinations, terminated with a 50 Ohms resistor and connected to two synchronized outputs of a signal generator set at a sinusoidal 20 V_{pp} - 5 MHz, resulting in HF circulating currents of approximately 200 mA.



(a) *(b)*

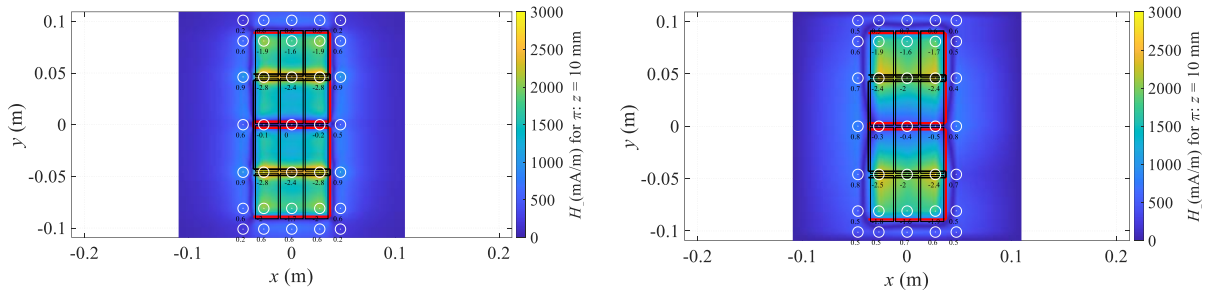
Figure 6.17 Experimental setup for mimicking the interconnection loops of a PCA4x3: (a) layout in detail highlighted by circles indicating the physical adaptions needed to overcome unrealistic theoretical assumptions above mentioned, crosses (X) indicating the points fixed measured by near field probe and 50 ohm resistors to allow the four loop combinations (A_1A_2 as illustrative example); (b) Testing equipment setup for the near field cartography using plexiglas sheet located 10 mm above the PCB, H10 EMC near-field probe from Tekbox and EM Scanephone V1 (Beta version) from Luxondes [21].

In *Figure 6.17*, it is presented the setup and PCB layout composed of plexiglas sheet located above the PCB in order to maintain the equipment well parallel at desired fixed distances. Two different technologies (near field probe and Scanephone) for accomplishing the near field measurement tasks are used and compared among each other as well as theoretical results.

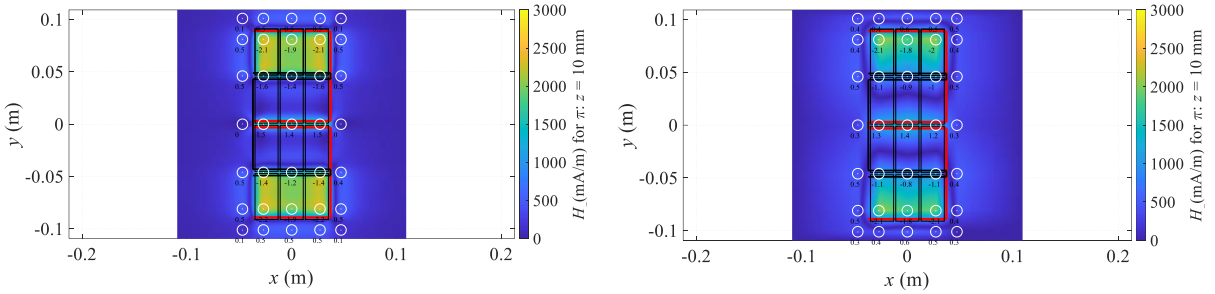
6.3.1.1 Near field probe EM cartography results comparing with theoretical results

The near field probe was first calibrated through TEM calibration according to Appendix 1.A. The resulting antenna factor AF = 48.6 dB A/mV was used for the frequency at 5 MHz to convert the RMS voltage value of sinusoidal noise signal across the probe, measured in time domain through oscilloscope, into magnetic density field. At total, 35 measurements of each combination (140 at total) at a distance of 10 mm from PCB in the plane presented on the white circles (please, feel free to use infinite zoom as the plotting are

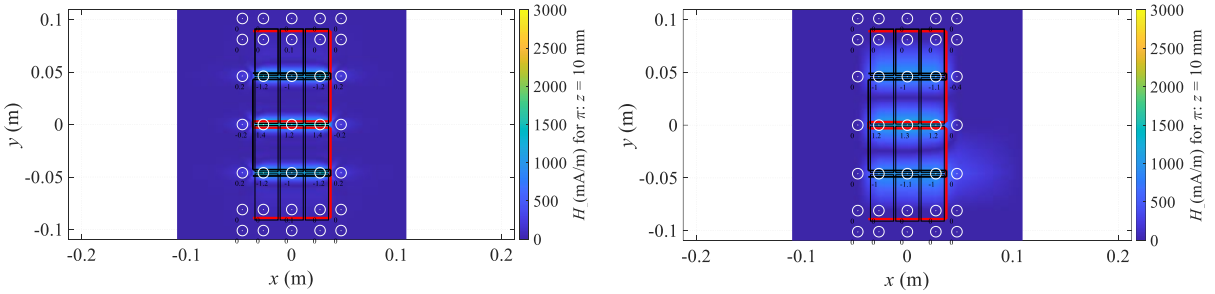
purposely vectorised) were performed as illustrated in *Figure 6.18*. The location of the measurements were strategically set to allow better interpolation results. A simple surface linear interpolation function on Matlab was used, providing representative quantitative results regarding magnitude and shape compared to theoretical plotting. To compare with practical results, new plots were derived with the characteristics provided by practical PCB while keeping the simplifying geometries aforementioned. Besides, in a reverse process of interpolation, the theoretical magnitude density was integrated in the circle area and averaged which can then be compared to practical results. Then, a side-by-side comparison for all four combinations between the proposed algorithm theoretical (on the left-hand side) and experimental results (on the right-hand side) is presented in *Figure 6.18*.



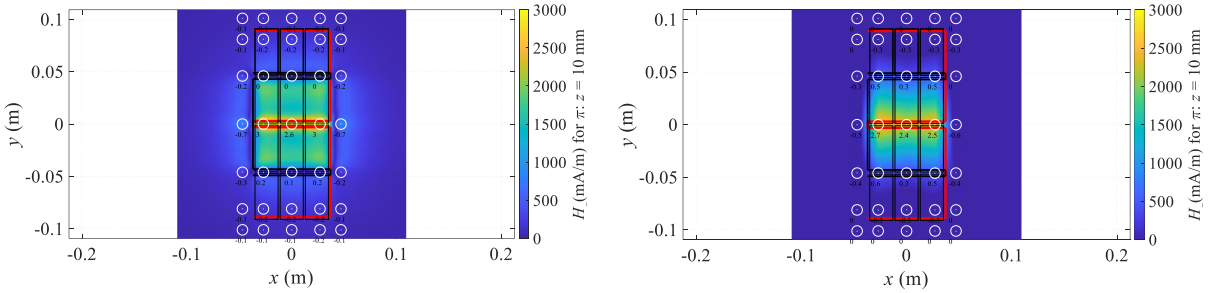
(a)



(b)



(c)



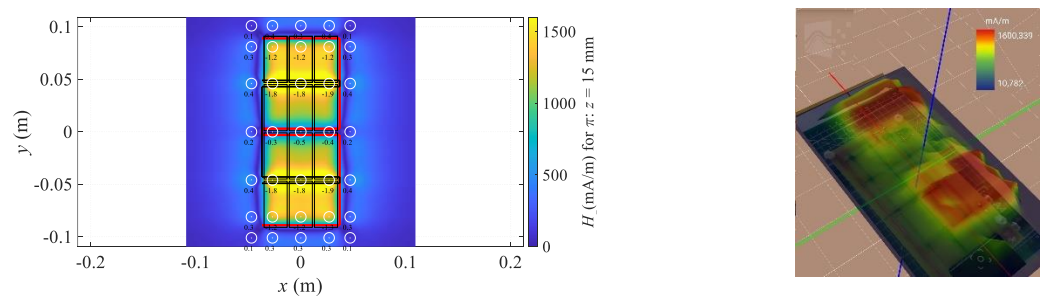
(d)

Figure 6.18 Plotting results z-component (absolute) produced by all four loop combinations of a PCA4x3 over the plane π: z = 10 mm: (a) A_1A_2; (b) A_1B_2; (c) B_1A_2; (d) B_1B_2. Theoretical results on the left-hand side and practical results through near field probe on the right-hand side. The input (red segments) and output (black segments) current sending paths as well as the CSCs (black rectangles) are presented for visualization. The circles represent the locations of the measured magnetic field over the plane using a H10 probe. Values inside the plotting are corresponding to the actual measured magnitudes converted into A/m.

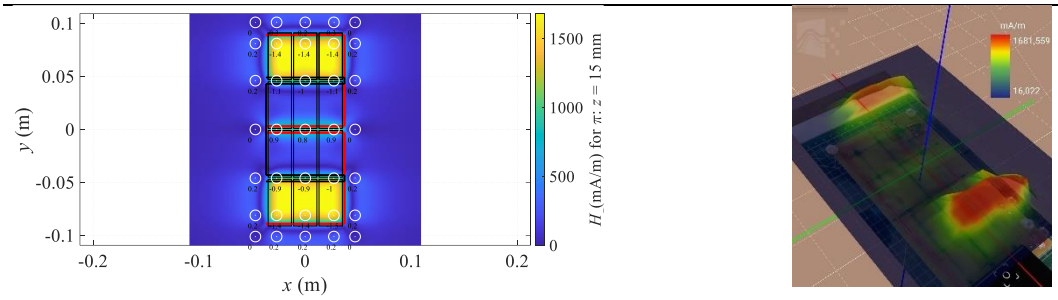
The theoretical results are qualitatively and quantitatively in accordance with the practical results. Besides, the impact on the near field regarding the different combinations is well visible in practice, being the combination B_1A_2 and A_1A_2, respectively, the least and most impactful on the near field, as predicted in theoretical previous results.

6.3.1.2 Scanephone EM cartography results comparing with theoretical results

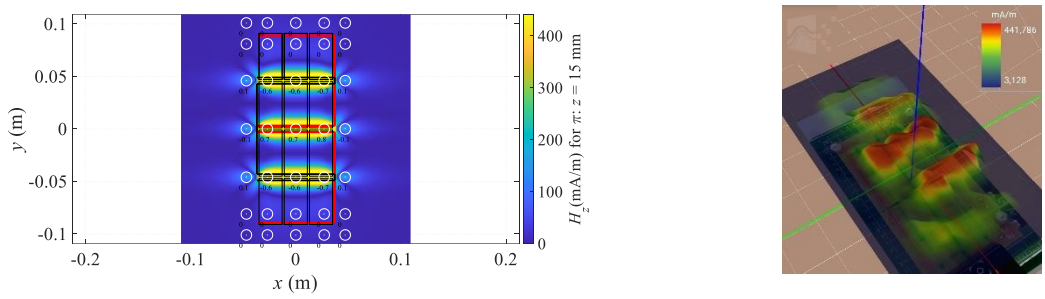
The Scanephone is a technology that mix virtual reality and EM near field measurement, easing the measurement and providing fast and pedagogical results. For the Scanephone, the accounted distance was 15 mm in which results are presented in *Figure 6.19*. It is presented a side-by-side comparison for all four combinations between theoretical results (on the left-hand side) and practical results (on the left-hand side) through the use of a scanephone.



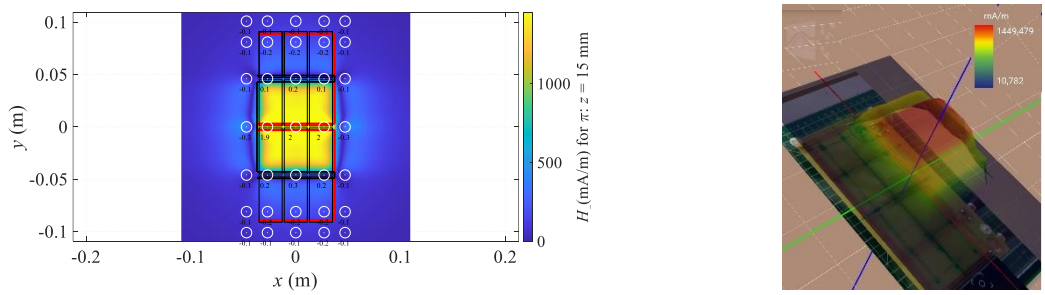
(a)



(b)



(c)



(d)

Figure 6.19 Plotting results z-component produced by all four loop combinations of a PCA4x3 over the plane π: z = 15 mm: (a) A_1A_2; (b) A_1B_2; (c) B_1A_2; (d) B_1B_2. Theoretical results on the left-hand side and practical results on the right-hand side through the scanephone. On the left-hand side, the input (red segments) and output (black segments) current sending paths as well as the CSCs (black rectangles) are presented for visualization. The circles on the left-hand side (theoretical results) are kept due for extra-information and convenience.

It is observed that the results verified good matching between practical and theoretical results as well. Such approach allowed analysing the experimental results in a more qualitative way, compared to previous method. As it can be concluded, the implementation of PCA approach allows the use of new qualitative technologies for EMI signature implementation, particularly the near field here proved. Worst and improved cases are also identified according to theoretical results as presented in previous sections.

6.3.1.3 Partial conclusion and perspectives

An agreement between theoretical and experimental results show that the choice of analytical synthesised results has superior advantages over other methods that required simulation and are time consuming, e.g FEM.

The actual motherboard can be used to study the near field by adapting a PCB that allows feeding the interconnections terminated with 50 ohms resistance, mimicking the behaviour in power converter.

It is important to notice that no disturbance analysis regarding harmful near field was performed. This means that, for the specific technology and power rating presented so far, such values could be far from being destructive or harmful. On the other hand, a general methodology was presented, which can be extended and applied for cases in which the near field can be harmful or required (e.g wireless power transfer [24]).

It is essential to assure whether or not the interconnections can indeed impact on both near and far field, and how harmful they can be. Therefore, using technology platforms that mimics (or eventually the actual motherboard fed by signal generator), or simply testing the different interconnection possibilities in prototyped PCA should be first verified in anechoic chambers (for far field analysis) and inter-cell and peripheral interference (for near field). A practical result that can easily be performed is capturing the field through TEM cell or antenna in anechoic chamber among the many interconnection possibilities, fed by signal generators. Sweeping the frequency in a large range and capturing the results may be effective to find the characteristic resonant frequency of the formed antenna. Immunity tests can also be performed by reversing the procedure, and data basing the captured voltage across the interconnections. In any case, the theoretical and practical results suggest that the current paths on a PCA may be very different in geometry and magnitude not only on the near emission, but also the far field emission, as the notion of opposite current rule on close segments is still maintained.

The PCB used to mimic the DMC current loops cannot be used to study in practice for CMC. A PCB can, be suggested for future work by considering the input BNC signals on the geometric center, and each end terminated with a 25 ohms resistance connected to a ground plane.

6.3.2 Experimental EM Cartography PCA (Version 2.0) in operation: near field probe

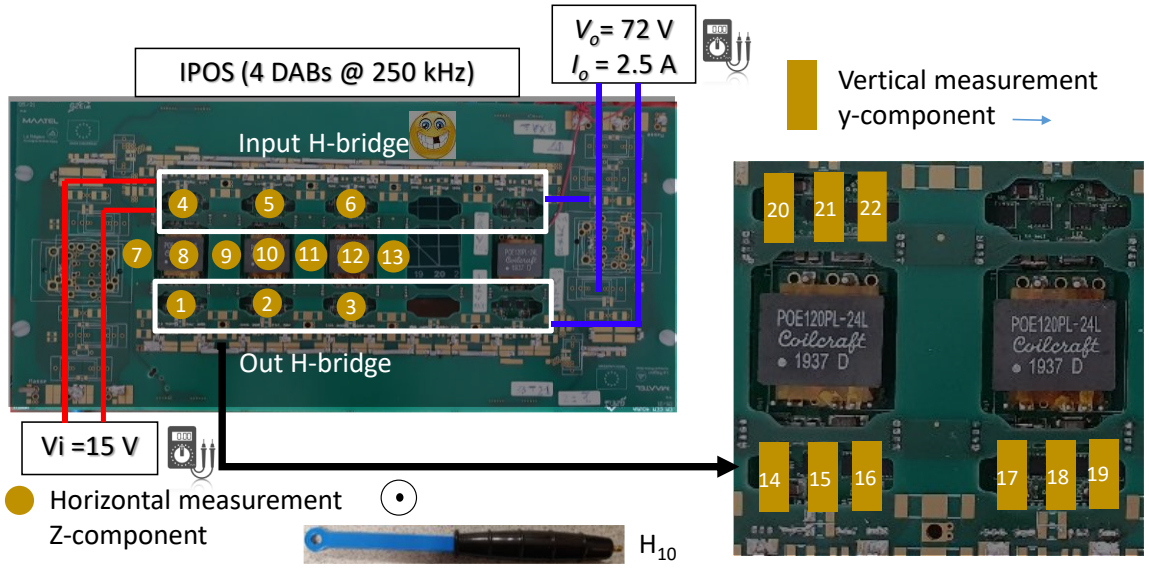


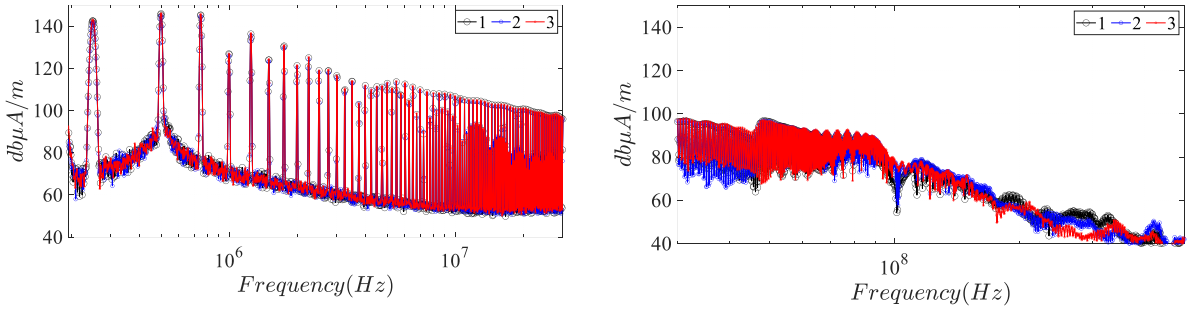
Figure 6.20 Testing porotype PCA (250 kHz and I_o = 2.5 A 4 CSCs 2.0): prototype of PCA (Version 2) containing 4 CSCs (Version 2);location of the tests performed using probe H10 in horizontal (yellow circles from 1 to 13) and vertical (yellow rectangles from 14 to 22).

In order to gain knowledge from experimental results, the near field produced by a PCA in operation was measured across different points. The use of near field probe H10 TBPS01 Tekbox was arbitrarily chosen located above around 1 cm in horizontal position, as the harmonic content can promptly be observed through EMI test receiver (R&S®ESRP EMI). In these experimental results, the near field produced by four CSCs (Version 2) (IPOS) using the motherboard structure (Version 2) are analysed across different measurement points, as presented in *Figure 6.20*.

Both CE frequency range (from 150 kHz to 30 MHz; Span = 29.85 MHz; Rf Att = 10 dB; RBW = 9 kHz; VBW = 30 KHz; Sweeping time = 10 s, Auto peak detector) and radiated frequency range (from 30 MHz to 500 MHz; Span 470 MHz, Rf Att = 10 dB; RBW = 120 kHz; VBW = 3 MHz; Sweeping time = 10 s, Auto peak Detector) are acquired and then analysed. For this and next sections, if one desires to access to detailed visual information, it is recommended the use of infinity zoom provided by PDF readers. Nevertheless, the main conclusions are highlighted through comments.

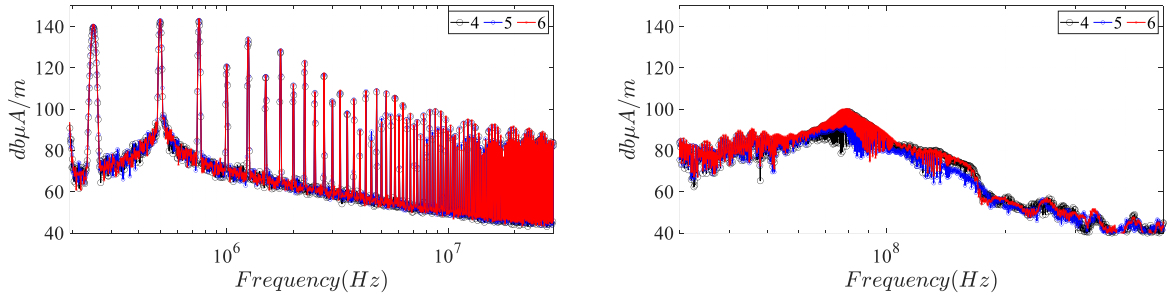
6.3.2.1 Full load (I_o = 2.5 A)

The experimental result plots of the operating point (M = 1.2, I_o = 2.5 A) of both CE and RE frequency ranges (150 kHz – 500 MHz) are depicted through *Figure 6.21 – Figure 6.26*. The voltage waveform across the drain-to-source MOSFETs are presented in *Figure 6.27* in order to correlate near field measurements with electrical behaviour.



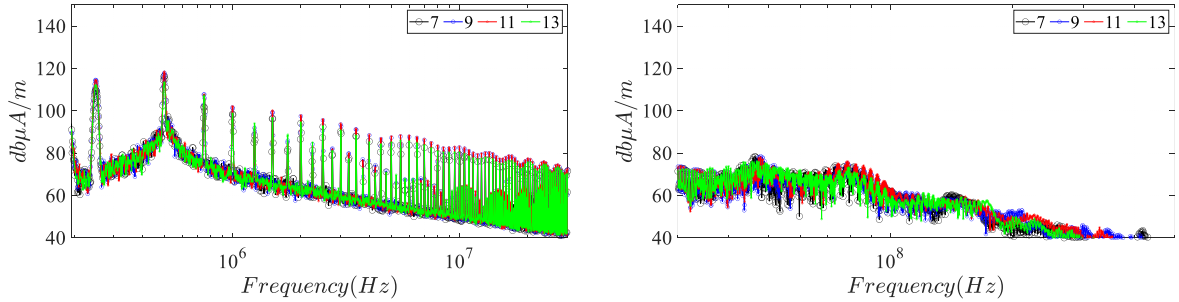
(a) *(b)*

Figure 6.21 Experimental near field measured for points from 1 to 3: (a) for the CE frequency range 150 kHz – 30 MHz; (b) for the RE frequency range 30 MHz – 500 MHz.



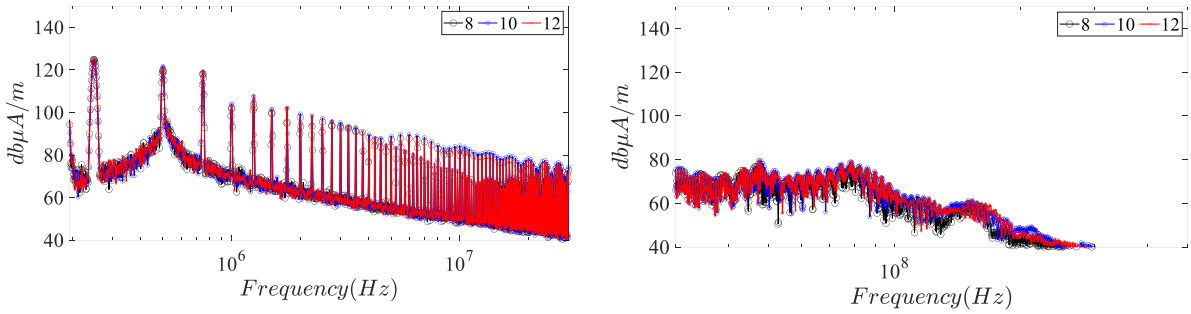
(a) *(b)*

Figure 6.22 Experimental near field measured for points from 4 to 6: (a) for the CE frequency range 150 kHz – 30 MHz; (b) for the RE frequency range 30 MHz – 500 MHz.



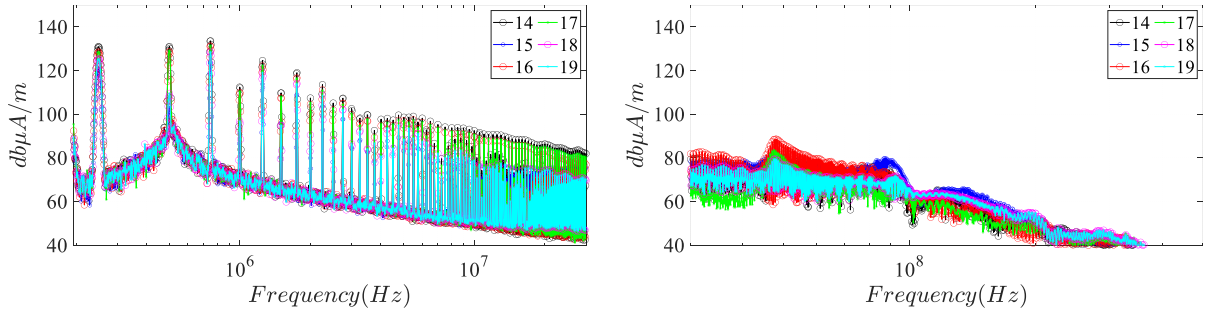
(a) *(b)*

Figure 6.23 Experimental near field measured for points from 7 to 13: (a) for the CE frequency range 150 kHz – 30 MHz; (b) for the RE frequency range 30 MHz – 500 MHz.



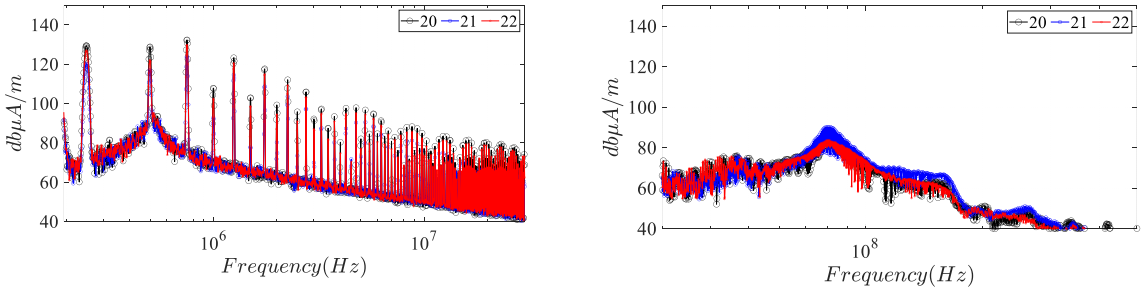
(a) *(b)*

Figure 6.24 Experimental near field measured for points from 8 to 12: (a) for the CE frequency range 150 kHz – 30 MHz; (b) for the RE frequency range 30 MHz – 500 MHz.



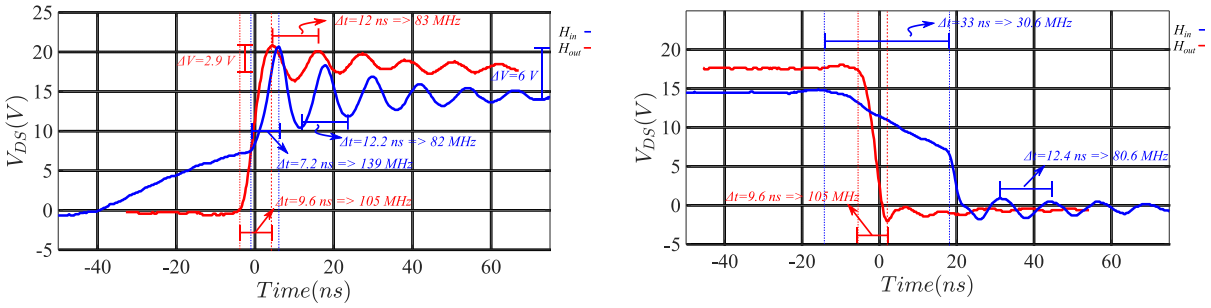
(a) *(b)*

Figure 6.25 Step-up (M=1.2) full load (I_o = 2.5 A) experimental near field measured for points from 14 to 19: (a) for the CE frequency range 150 kHz – 30 MHz; (b) for the RE frequency range 30 MHz – 500 MHz.



(a) *(b)*

Figure 6.26 Step-up (M=1.2) full load (I_o = 2.5 A) experimental near field measured for points from 20 to 22: (a) for the CE frequency range 150 kHz – 30 MHz; (b) for the RE frequency range 30 MHz – 500 MHz.



(a) *(b)*

Figure 6.27 28 Step-up (M=1.2) full load (I_o = 2.5 A) experimental drain to source voltage V_{DS} (CSC 2) across input H-bridge (blue color) and output H-bridge (red color): (a) rise time; (b) fall time. It is possible to observe incomplete ZVS and its effect on oscillations across drain-to-source voltage.

The first conclusion is that a repeatable pattern in standard points are observed. Small differences may be related to precision in location (human factor) and precision of devices as well as natural asymmetry induced by corners. Such behaviour was already expected due to simple logical reasons. Once the near field are organized in known patterns, it is easy to compose the near field of any PCA from practical measurements.

Throughout all measurements, the near field measured over the input H-bridge points {4 – 6} and output H-bridge points {1 – 3} are the largest , reaching up to 140 dBμA/m (*Figure 6.21* and *Figure 6.22*), even compared to the near field centred at the transformers {8, 10, 12} (*Figure 6.24*), which is known for being natural near field noise generator. Such fact shows the importance of keeping the switching cells PCB loops as reduced as possible, or even shielding such region in order to avoid cross talking, inter- and intra- cell interference or any EMC performance degradation.

Vertical measurement results, meaning y-component field detection, {14 – 22} (*Figure 6.25-Figure 6.26*) tend to keep same spectrum behaviour as horizontal measurements (meaning z-component field detection) {1– 6} (*Figure 6.21* and *Figure 6.22*) with an offset reduced by approximately 10 dB for both CE and RE frequency ranges. Note that the probes in vertical were closer to the switching cell loops (nearly touching them), while the horizontal measurements were around 1 cm higher the switching cell loops. This means that the near field are generated by currents on the same plane of the cells (*xy*), affecting, therefore, more drastically on z-components, as expected.

With respect to middle located points {7 – 13} (*Figure 6.23* and *Figure 6.24*), the ones located over the transformer {8, 10 and 12} presents larger amplitude (around 10 dB) in

the lower to medium frequency range than the ones located around {7, 9, 11, 13}. This is clearly related to the magnetic near field generation at the source due to transformer. On the other hand, the high frequency range level reveals, that a similar spectrum characteristic is found for all locations from {7 – 13}. Moreover, they tend to be a superposition between input and output switching cell near field measurements. The mix between region input H-bridge and output H-bridge over the middle location parts could mean a more reliable image of the far field, but future studies to find a good location to related near field with far field is still required.

Regarding envelope, in general, a -40 dB/dec is observed as of the third harmonic, followed by a resonance around 60 – 80 MHz and -60 dB/dec after such resonance peak. For the lower frequency, the -40 dB/dec is well explained by mostly DM square and triangular waveforms circulating across the PCA.

Finally, it is interesting to observe and compare the input H-bridge {4-6} and output {1-3}regions. Observing the result, in general, output H-bridge part tends to present larger amplitude on lower to medium frequency range (150 kHz – 50 MHz) than input H-bridge, while a more accentuated peak was observed on the input H-bridge part due to a resonance around 80 MHz. Such resonance is related to the High Frequency Oscillation (HFO), consequence of parasitic inductance on the switching cell loops together with incomplete ZVS. This is concluded due to the correlation with the drain-to-source voltage measured across the MOSFETs of input and output H-bridges, as presented in *Figure 6.27*. Indeed, as well explained in *Chapter 2*, boost modes tend to perform ZVS across output H-bridge and less chances across input H-bridge; The HFO (around 80 MHz) is therefore observable more emphatically across input H-bridge. The resonance at 50 MHz over output H-bridge could not be explained or correlated with electrical working.

6.3.2.2 Open circuit (OC)

To explore the characteristic resonance of the PCA, it is then performed OC test in which the static gain is varied and compared with the full rated power. In *Figure 6.29*, it is presented the spectrum in the higher frequency range (30 MHz – 500 MHz) of the measured point 1 (output H-bridge).

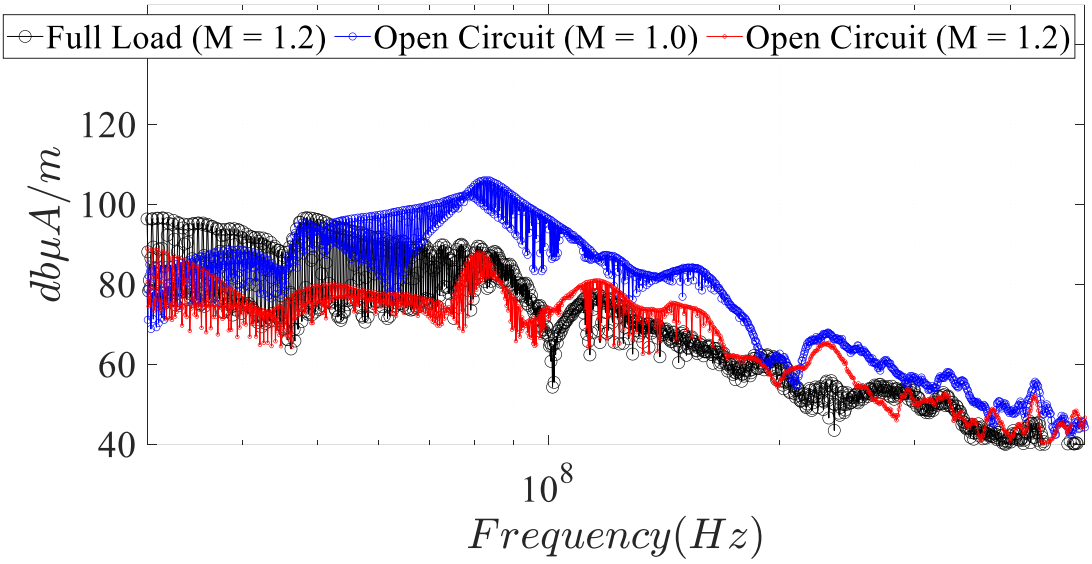


Figure 6.29 Experimental measurement results of point 1 (output H-bridge) for the RE frequency range 30 MHz – 500 MHz for full load (black), OC Unitary (M=1.0) (blue) and OC Step-up (M=1.2) (red).

Notice that, the peak around 90 MHz is more accentuated in an OC, rather than in step-up modes, even at full load. Such fact proves that the worst case scenario is not always at full load, and that it depends on the operating point. As observed in *Chapter 2*, the step-up modes tends to realize ZVS across the output H-bridge, which explain the lower amplitude in the higher frequency range, whereas unitary tends to not realize ZVS, explaining a higher amplitude content in the higher frequency range!

Then, with the same operating testing conditions and points, it is presented in *Figure 6.30* the experimental measurement results for input H-bridge (point 4).

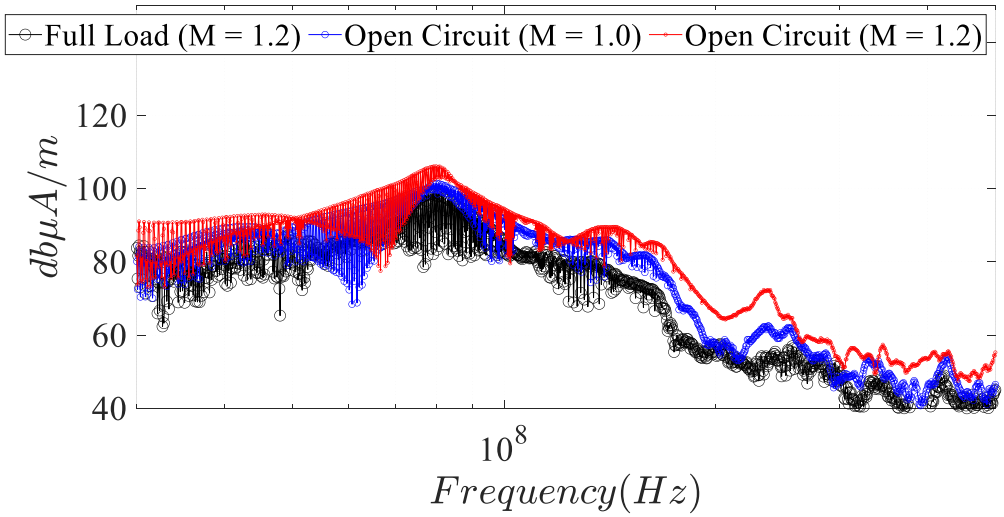


Figure 6.30 Experimental measurement results of point 2 (input H-bridge) for the RE frequency range 30 MHz – 500 MHz for full load (black), OC Unitary (M=1.0) (blue) and OC Step-up (M=1.2) (red).

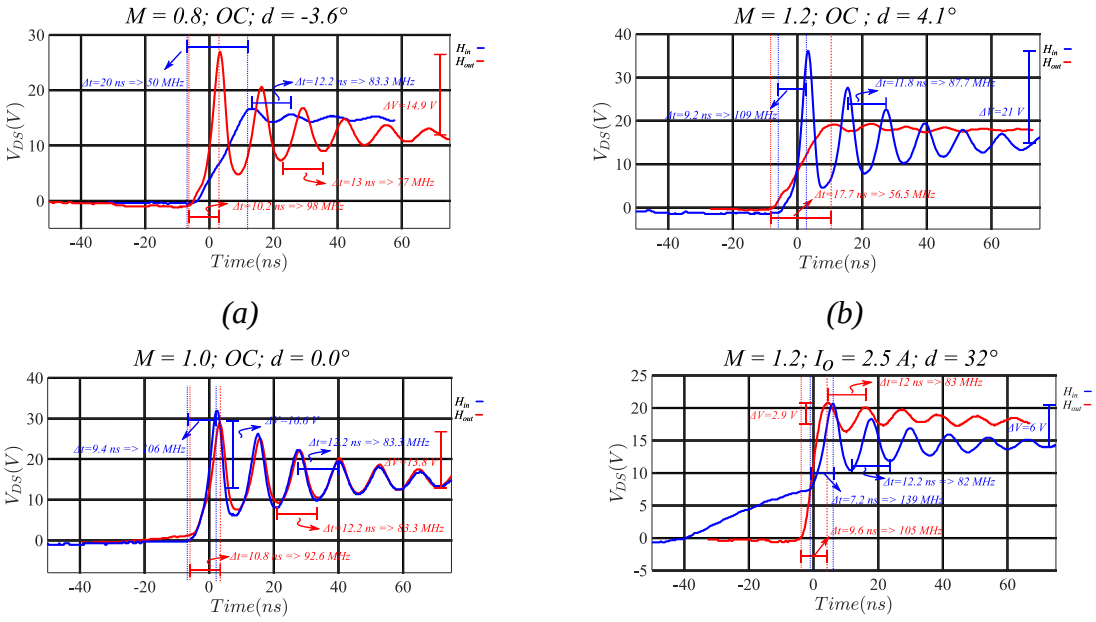


Figure 6.31 Experimental drain to source voltage V_{DS} (CSC 2) across input H-bridge (blue color) and output H-bridge (red color): (a) Step- down (M = 0.8) OC; (b) Step-up (M = 1.2) OC; (c) Unitary (M = 1.0) OC; (d) Step-up (M=1.2) full load (I_o = 2.5 A).

It is, then possible to correlate the EMI spectrum signature presented in *Figure 6.30* with the drain-to-source voltage of the input and output H-bridges. In *Figure 6.31*, it is presented such measurements for the OC in step-down, unitary and step-up and for the full rated power. As it can be noticed and expected, the step-down has a complementary behaviour with respect to the step-up mode, which should be visible in the EMI spectrum signature. More experimental results in OC are discussed and compared in Appendix 6.B.

6.3.2.3 Partial conclusion and perspectives

It is concluded that the near-field can be predicted based on experimental results measured through near field probes, as their values are repeatable at standard locations. Correlation between near-field measurements and the electrical operation of a cell is also possible, providing interesting insights for power electronics engineers to more easily detect issues, such as incomplete Zero Voltage Switching (ZVS) and resonance frequency throughout the circuit. The ability to predict and correlate EMI issues is relevant for the

concept of automated design through PCA. However, this method can be applied to any power electronic device to gain initial insights and correlate them with electrical performance.

6.3.3 Experimental EM Cartography PCA (Version 2.0) in operation: TEM Cell

In the section, the same power converter as previous mentioned (PCA 2.0 and CSC 2.0 operating at 250 kHz) are analysed through TEM Cell. The entire setup is depicted *Figure 6.32*. The PCA can be positioned in a TEM cell over parallel to different planes, as presented in *Figure 6.33*. The PCA was positioned parallel to the planes π (always above 5 cm through non-conductive foam, neutral to EMI interferences) and γ (held manually and using the same foam). Infinity zoom through PDF readers are recommended if better details are necessary. The spectrum analyser configurations are: from 150 kHz to 500 MHz; Span = 499.85 MHz; Rf Att = 10 dB; RBW = 9 kHz; VBW = 10 kHz; Sweeping time = 12 s, Auto peak detector.

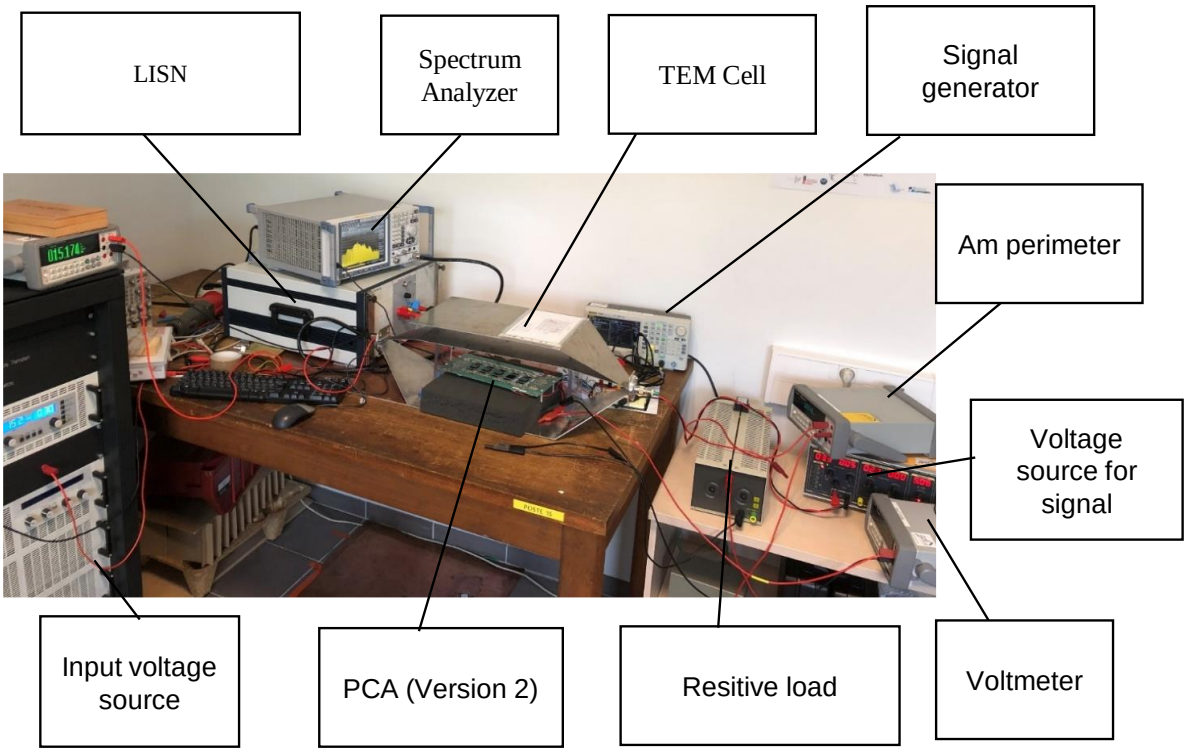


Figure 6.32 Diagram and picture of the setup for data basing the EMI signature of a PCA through TEM Cell. PCA and CSC (4 cells) version 2 used.

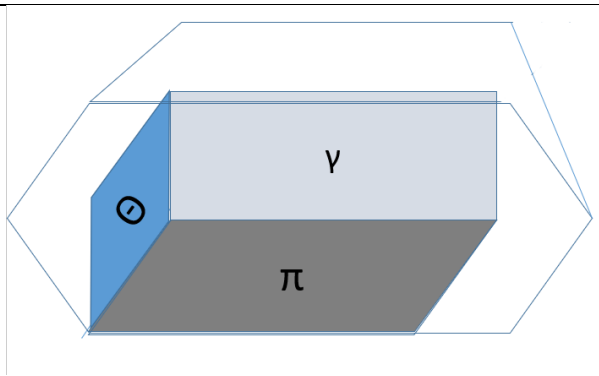


Figure 6.33 Different planes in a TEM cell that can impact on the TEM equivalent EMI signature.

6.3.3.1 Full load (I_o = 2.5 A)

The experimental results in Figure 6.34 presents the TEM Cell's EMI signature results for a PCA in horizontal position (version 2) operating with V_i = 15 V, I_o = 2.5 A and step-up mode (M = 1.2), varying amount of cells in operation from 1 to 4.

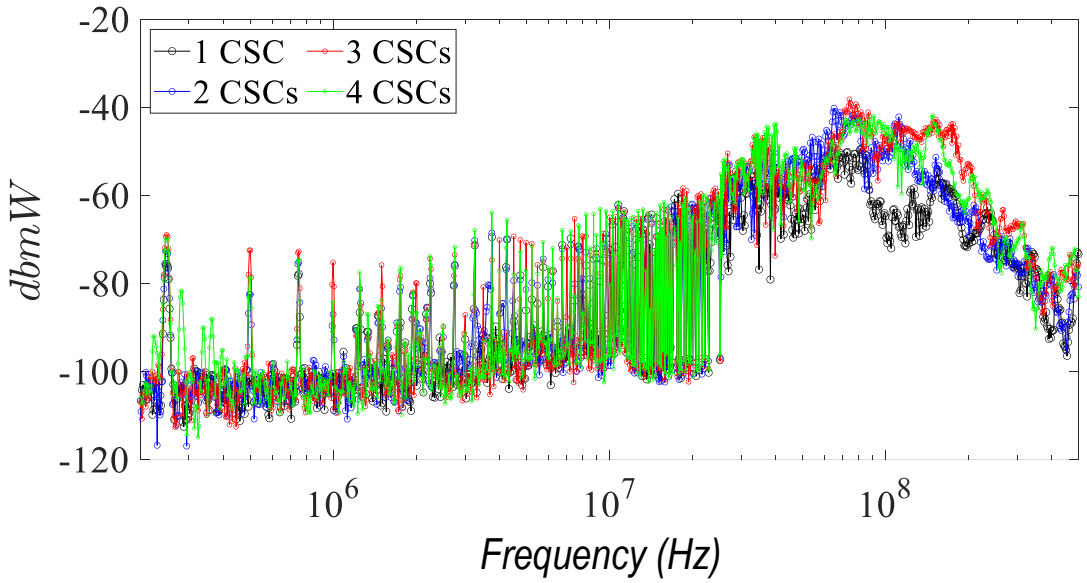


Figure 6.34 Cell TEM's EMI signature results for a PCA (IPOS) (Version 2) positioned parallel to plane π operating with V_i = 15 V, I_o = 2.5 A and step-up mode (M = 1.2), varying number of cells in operation 1-4.

The first visible conclusion is that both even and odd harmonics multiple of the switching frequency appear EMI noise. Further investigation on how the harmonics are related to the electrical working of a power converter was not object of study in this work. The second conclusion is that, the PCA EMI emission level seems to not be impacted by the

number of CSCs, at least directly or linearly. Notice that the same motherboard was used for the experimental results, by unplugging CSCs and short-circuiting series connection paths. That is, the "antenna effect" from interconnections is kept in all cases, which could explain the similar results when varying the number cells.

Different from results provided by near field probe measurements a non-decreasing and more or less constant envelop is presented in the CE frequency range. Regarding the RE range, it follows similar pattern, with an increased offset. The resonance at 50 MHz and other at 80 MHz is presented on the TEM cell's measurement as well, but it less protuberant. From all the previous near measurements and regarding only RE frequency range, the ones on middle points, as presented in *Figure 6.23*, are the ones that has a comparable frequency envelope (considering offset fitting), confirming previous suspicions. The very fast decay starts only in the RE frequency range around 200 MHz, due to another resonance frequency at 200 MHz, rather than 100 MHz as presented in near field measurements.

In *Figure 6.35,* the PCA is positioned oriented to the plane γ, and the results are similar to the previous one (π plane) *Figure 6.34*, with an increase shift of 20 dB. This shows that there exist position in which the power converter will be more impactful.

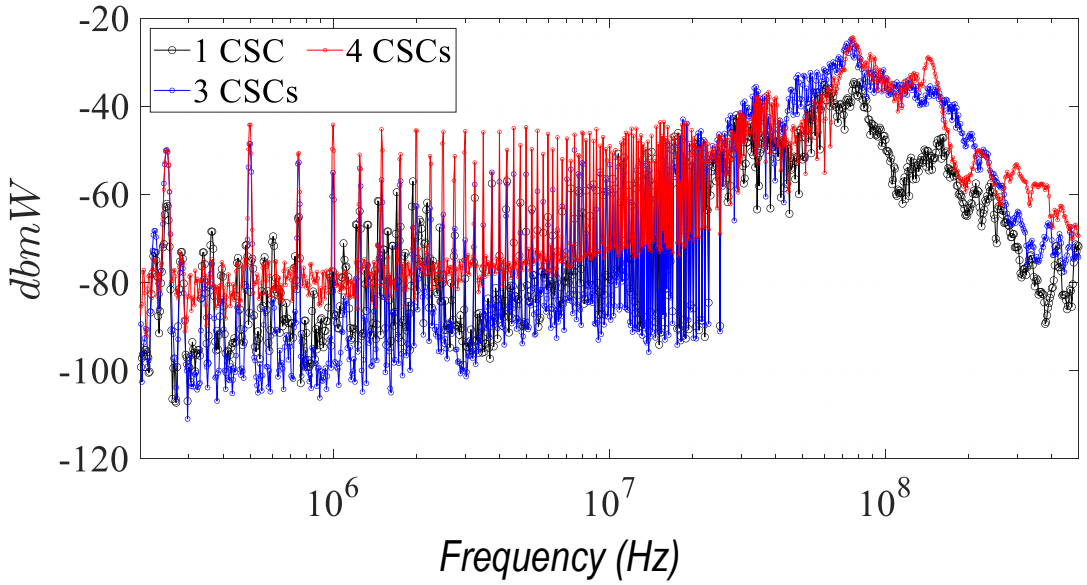


Figure 6.35 Cell TEM's EMI signature results for a PCA (IPOS) (Version 2) positioned parallel to plane π operating with V_i = 15 V, I_o = 2.5 A and step-up mode (M = 1.2), varying number of cells in operation 1-4.

In *Figure 6.36*, the PCA containing the four cells and oriented parallel to the π is tested considering this time static gain variation (step-down or "buck" *M* = 0.8, unitary, *M* =

1.0 and step-up or "boost" M = 1.2) while keeping output current constant at I_o = 2.5 A. It is noticeable that, in the RE frequency range, the step-up mode is in general higher followed by unitary and step-down modes.

Comparing pattern behaviour between near field probe and TEM Cell , it can be noticed that there is a resemblance, except that the near field probe's results is decreasing, whereas the TEM Cell's, which can be associated to the far field, is accentuated, due to the antenna effect, mainly in the region of RE frequency range.

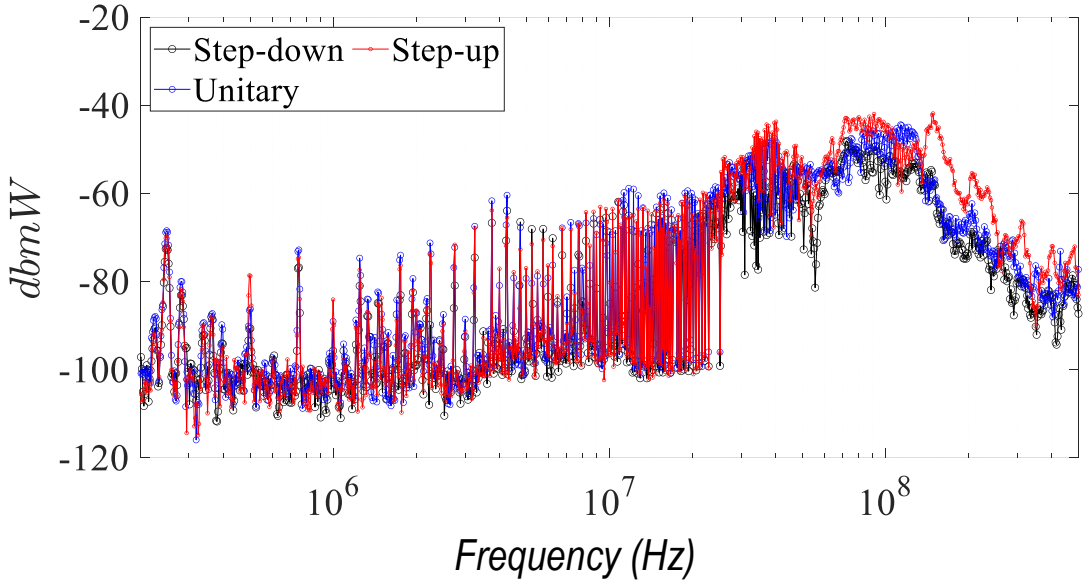
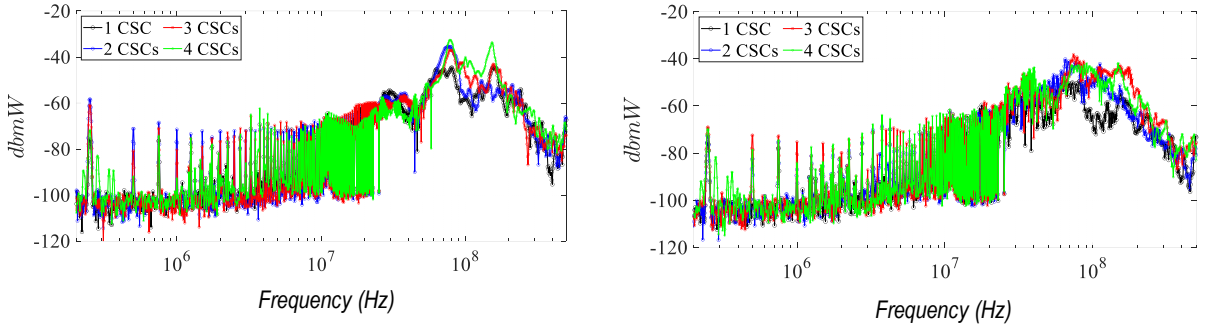


Figure 6.36 Cell TEM's EMI signature results for a PCA_{1X4} (IPOS) (Version 2); positioned parallel to plane π operating with V_i = 15 V, I_o = 2.5 A, number CSCs = 4, varying static gain.

6.3.3.2 Open circuit (OC)

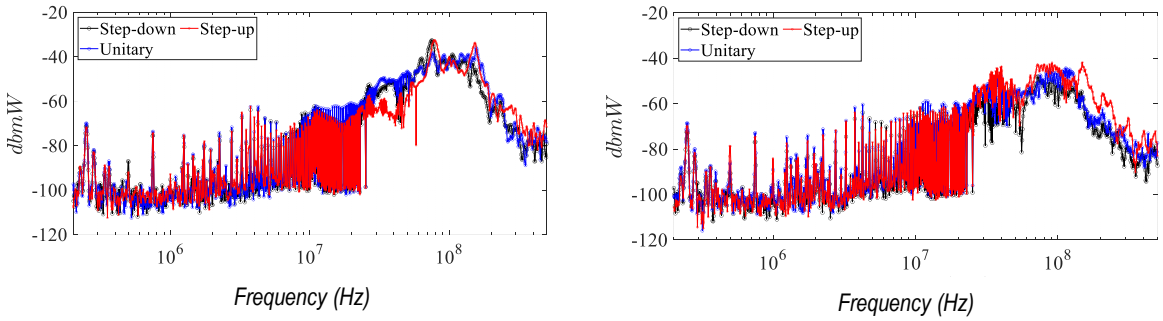
The TEM Cell frequency response of the PCA in IPOS configuration, boost mode operated in OC and rated load are depicted side-by-side for easier comparison regarding spectrum envelope.

The OC test is performed now at boost mode with PCA location oriented to the π plane, and varying the number of CSCs, and the static gain as presented are compared with full load cases, respectively in *Figure 6.37* and *Figure 6.38*.



(a) *(b)*

Figure 6.37 Cell TEM's EMI signature results for a PCA$_{1X4}$ (IPOS) (Version 2); positioned parallel to plane π operating with V_i = 15 V, and step-up mode (M = 1.2), varying number of cells in operation 1-4.): (a) OC; (b) full load (I_o = 2.5 A).



(a) *(b)*

Figure 6.38 Cell TEM's EMI signature results for a PCA$_{1X4}$ (IPOS) (Version 2); positioned parallel to plane π operating with V_i = 15 V,, number CSCs = 4, varying static gain: (a) OC; (b) full load (I_o = 2.5 A).

As it can be seen, in general, there is an offset increase in OC compared to full loaded case, mainly for the resonances peak at 80 MHz and 150 MHz, except for the 50 MHz region, resembling the near field probe experimental results presented *Figure 6.34*. Once again the OC testing proved to be representative and conservative in terms near fields, this time measured through TEM cell.

Due to simplicity in acquiring results, the OC condition was tested for a PCA working with 4 CSCs and varying input voltage (10 V – 25 V) for the step-down mode (*Figure 6.39*), unitary mode (*Figure 6.40)* and step-up mode (*Figure 6.41*).

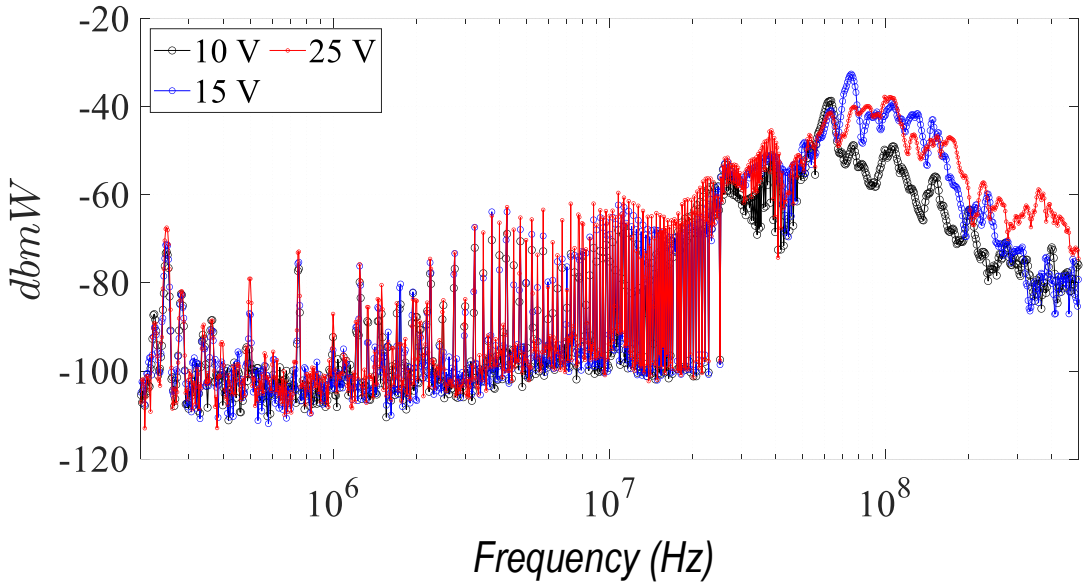


Figure 6.39 Cell TEM's EMI signature results for a PCA_{1X4} (IPOS) (Version 2); positioned parallel to plane π; operating OC and step-down mode (M = 0.8), varying input voltage Vi [10 -15] V.

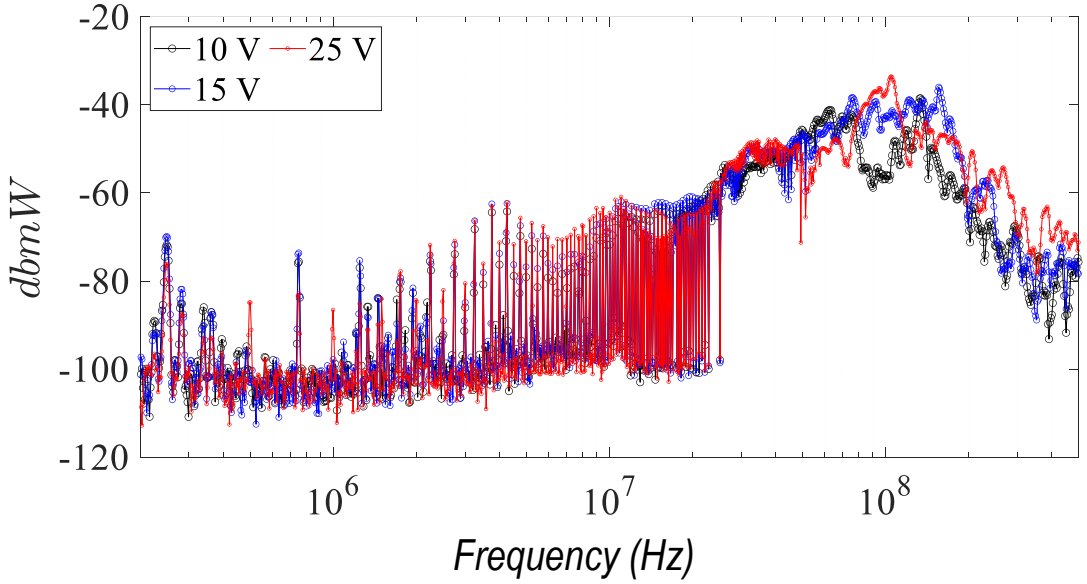


Figure 6.40 Cell TEM's EMI signature results for a PCA_{1X4} (IPOS) (Version 2) positioned parallel to plane π operating OC and unitary mode (M = 1.0), varying input voltage V_i [10 - 15] V.

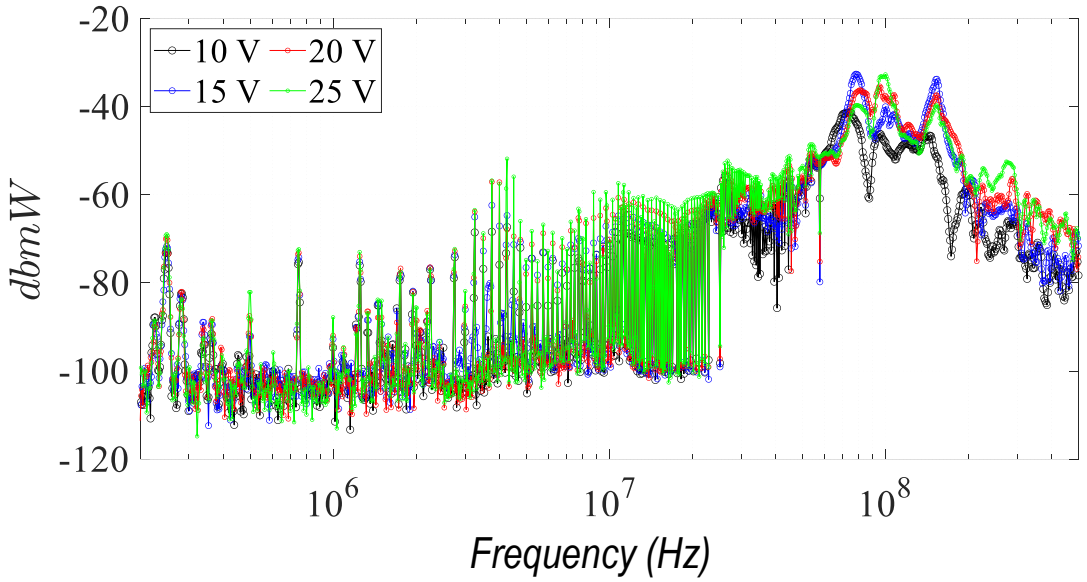


Figure 6.41 Cell TEM's EMI signature results for a PCA_{1X4} (IPOS) (Version 2) positioned parallel to plane π operating OC and step-up mode (M = 1.2), varying input voltage V_i [10 -15] V.

Roughly, it is possible to conclude that the field increases with the increasing in input voltage and static gain. This can be logical, because the electromagnetic field is well related to CM noise, which, is itself dependent on voltage sources (input and output voltages). Notice that the applied voltage will vary the drain-to-source capacitance C_{oss} of the MOSFETs, (increasing the voltage, the equivalent C_{oss} to decrease), which can increase switch speeds, shift resonance frequencies, and influence on ZVS performance

6.3.3.3 Partial conclusion and perspectives

It can be concluded that the tests through TEM cell allowed comparisons among different physical (number of CSCs) and electrical configurations (static gain variation). Besides, one can co-relate the TEM cell results with the near field probes and electrical working conditions. Other comparative studies (e.g. varying output current, 3D stacking, inclusion of centralized and / or distributed, and interconnection architectures) are suggested for future studies. However, it is important to keep in mind how any simple experimental setup can be used to perform comparative tests and optimization of any system that contains many variables (e.g. gate driver resistance, filter designs, shield, ferrite beads, interconnections, modulation technique, multi-cell converter associations) regarding RE (near or far field) through the provided methodology.

Once again, it is important to remind that differences or errors due to human and non-identifiable factors should be taken into account when analysing. Nevertheless, they follow a

pattern, and the impact of the number cells could be more interesting regarding at line level in 2D and 3D directions.

This is because there is room for investigating on how the RE can be actively improved by performing different physical (2D and 3D) and PWM by opposing somehow the RE produced by a PCA line, once it has been well characterized.

The question remains to know is if the improvements in a certain frequency range observed through simpler experimental results are really needed or impactful regarding cross talking, RE standard compliance and immunity. Therefore, experimental results in anechoic chamber to compare and co-relate all the measurements, and near field immunity tests and observation of the device under test (e.g. triggering gate driver due to cross-talking) are still required.

Considering that each CSC has its own precision from manufactory, temperature, frequency and saturation model, and intra-cell effect may be occurring, it is quite complicate to discriminate each behavior. Therefore, as a suggestion, an envelope out of as many experimental results from OC testing can be used to draw conservative and approximatively first insight solutions.

6.3.4 Experimental EM Cartography PCA (Version 3.0) with CSC 3.1 or 3.2 in operation: TEM cell

In this final subsection, the PCA_{1x2} and PCA_{1x6} constructed for the CSC 3.1 and 3.2 (f_s = 100 kHz) were used to generate results from the TEM Cell in a similar setup as previous subsection 6.3.3. Spectrum analyser configuration (from 50 kHz to 500 MHz; Span = 499.95 MHz; Rf Att = 0 dB; RBW = 9 kHz; VBW = 30 kHz; Sweeping time = 15 s, Auto peak detector).

Different from previous experimental setup, this one was performed with better EMC practices, such as measuring the noise floor, cleaner setup using blinded cables for generating the command signals; configurable in terms of grounding managing and, finally, has the 0° and 180° interleaving shifting approach easily permutable, as presented in *Chapter 5*.

Therefore, the objective of these experimental results is to verify in practice the advantages of the CSC 3.1, and CSC 3.2 which was constructed to provide superior EMC aspects; as well as the improved setup compared to CSC 2.0.

Another goal is to observe, through the TEM cell near field measurement, the impact of applying the proposed 180° interleaving, presented in *Chapter 5*, correlating important harmonics with CM noise. As it will be demonstrated, there is an interesting large reduction of the harmonics when applying the 180° interleaving in the CE frequency range.

Finally, the last goal is to compare the version CSC 3.1, that does not contain Cy and ground plane, with the CSC 3.2, that contains C_y and ground plane, which can be connected or not through a protective earth (PE).

6.3.4.1 PCA_{1x2}

This PCA_{1x2} was originally constructed to study the CE impacting of a pair of CSCs and the 180° interleaving. Meanwhile, it is also an opportunity to study such effects on RE by minimizing the amount of parameters, such as the mismatch of many CSCs. Moreover, the impact of interconnections can then be compared to the PCA_{1x6}. If the smaller PCA_{1x2} is proven to induce less EMI level than the PCA_{1x6}, the assumptions aforementioned that smaller PCAs may pass the EMC more easily can be seen as an opportunity for further investigation.

The configuration IPOS in which each CSC was set to provide rated input voltage V_i = 20 V, rated output current I_o = 2.5 A and unitary static gain M = 1.0 was tested, in which results are presented in the following testing measurements.

The first step consisted on measuring the "noise floor" of a disabled PCA_{1x2}, , in which only signals flowing through its command signals and produced by a frequency generator are enabled. This means that the noise due to only signal generation is taken into account and it is also a characteristic EMI signature. Next, the interleaving technique discussed and proposed in *Chapter 5* is enabled, "0π" and disabled "00". For these experimental results, the PCA was positioned horizontal to the plane π, but turned 180° in the *z*-axes, due to space availability, with respect to previous experimental setups.

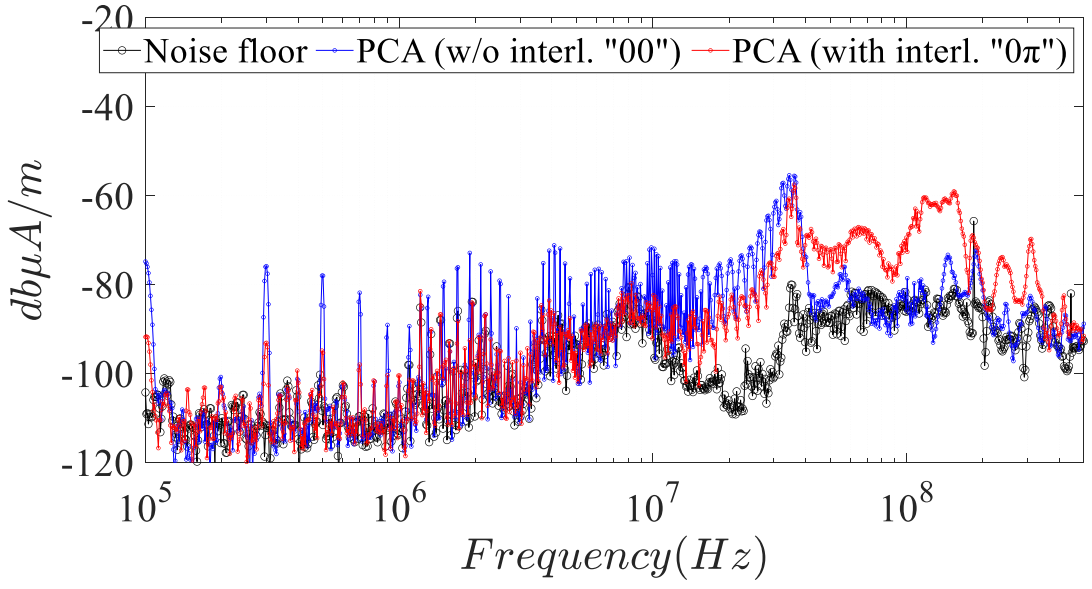


Figure 6.42 Cell TEM's EMI signature results for a PCA_{1x2} IPOS (Version 3.1) positioned parallel to plane π (each CSC was set to provide rated input voltage V_i = 20 V, rated output current I_o 2.5 A and unitary static gain M = 1.0) not enabling interleaving "00" (blue) and enabling interleaving "0π" (in red).

In *Figure 6.42*, the results for the CSC 3.1, the CSC without ground plane, are then depicted. Comparing the "00" results (in blue) back to previous PCA results presented in *Figure 6.34*, a reduction of at least 10 dB is observed generally for the entire frequency range. Besides, the resonance peak located nearby the 40 MHz is the only one more accentuated. Among the possible reasons, the smaller size of the PCA, the symmetrical CSCs and "cleaner" setup could explain the improvement. Comparing such results with the "noise floor" results, it can be seen that the PCA provides already good results, mainly regarding the RE frequency range. The EMI harmonic levels are mostly dominated by the odd multiple of the switching frequency. This could possibly mean that such harmonics are well correlated to the CM noise current. These are assumptions that opens an opportunity for further investigation. Then, the 180° shifting "0π", as presented in *Chapter 5* is implemented (in blue). Notice that that for the CE frequency, there is an elimination (up to noise floor) of the harmonic content in the lower frequency range. This once again can follows expected assumption that such noises come from CM noise current, in which important attenuation was already proved effective in *Chapter 5*. Notice, however, that the approach 180° shifting does not necessarily guarantee reduction on the RE frequency range, but rather an increase is observed!

Further action such as grounding managing, possible to be performed with CSC 3.2 connected to the protective earth (PE) is then provided. Same procedure as previous experimental results are performed and results are presented in *Figure 6.43*. Notice that there is a significant reduction of the harmonic amplitude, mainly at the higher frequency range. This time, the "0π" results has the same spectrum content as "00", meaning that there is an improvement for the higher frequency range, desirable for RE EMC standards.

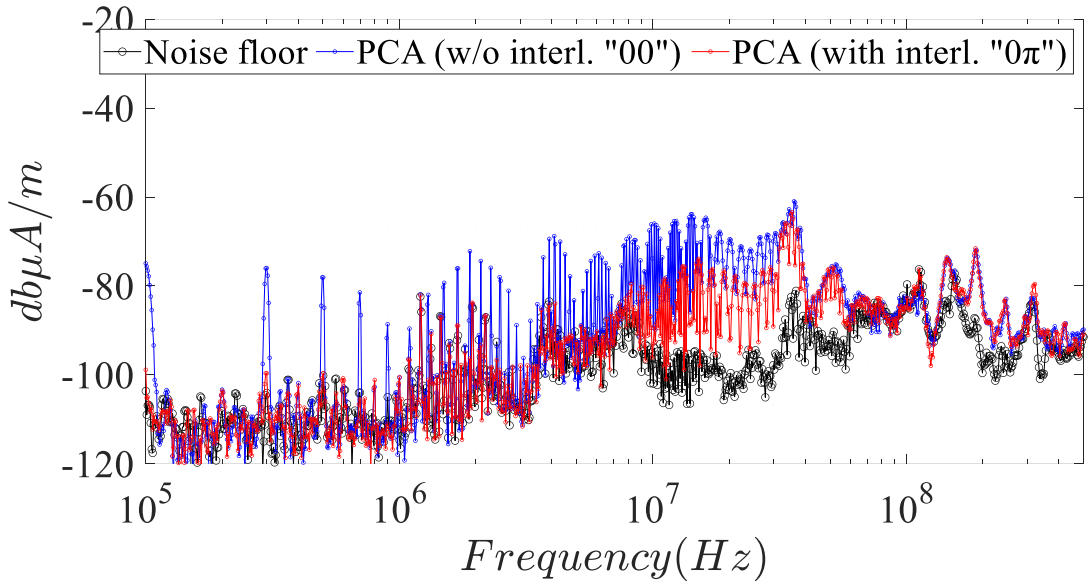


Figure 6.43 Cell TEM's EMI signature results for a PCA_{1x2} IPOS (Version 3.2 – PE connected) positioned parallel to plane π (each CSC was set to provide rated input voltage V_i = 20 V, rated output current I_o 2.5 A and unitary static gain M = 1.0) not enabling interleaving "00" (blue) and enabling interleaving "0π" (in red).

Finally, continuing the experimental results with CSC 3.2, the (PE) is no longer connected to the ground of the LISN, in which plotting results are presented in *Figure 6.44*. As it can be concluded, the PE connection has not much effect on the EMI signature. In such scenario, the "ground plane" works more as a "virtual plane", that provides improvement of the EMI signature.

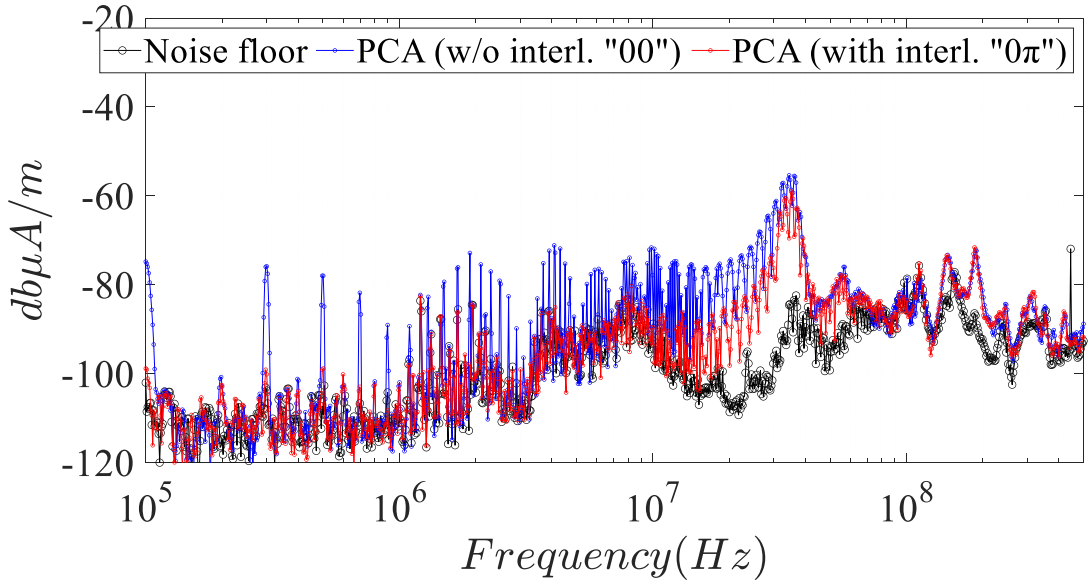


Figure 6.44 Cell TEM's EMI signature results for a PCA_{1x2} IPOS (Version 3.2 – PE not connected) positioned parallel to plane π (each CSC was set to provide rated input voltage V_i

= 20 V, rated output current I_o 2.5 A and unitary static gain M = 1.0) not enabling interleaving "00" (blue) and enabling interleaving "0π" (in red).

6.3.4.2 Partial conclusion and perspectives

It is concluded in this subsection that CSC 3.1 and CSC 3.2 exhibit superior performance when observed through a TEM cell. Furthermore, in general, the improvements resulting from enhanced CSCs and the 180° technique are clearly perceptible in the CE frequency range. Regarding ground management, CSC 3.2 has successfully mitigated the EMI signature, whether connected to the PE (ground plane) or not (virtual plane). It is important to note that these studies are highly specific and cannot be generalized without further experimental results using the same or a greater number of CSCs. Nevertheless, it is intriguing to bear in mind that the TEM cell is a suitable EMC pre-compliance testing equipment that can simultaneously correlate CE and RE at the same instant.

6.4 Chapter's Conclusion and perspectives

This Chapter has presented a methodology that is based on analytical and experimental approaches to characterize and improve the EMC aspects in a PCA. The proposed solutions to co-relate with electrical working of a power converter and improve the radiated field proved to be effective through inexpensive near field probe and TEM cell results. The correlation between near field measurements and electrical working of one CSC made of DAB in OC was possible, providing interesting results that power electronic engineers can be familiar with for non-intrusively and quickly detecting problems at early stage, such as incomplete ZVS more easily and resonance frequency through the circuit. Indeed, the ability to forecast and correlates EMI issues is interesting for the concept of automated design through power converter arrays.

For the CE frequency range, the OC experimental results presents lower magnitude at some frequencies and higher at others. For the case with load, even though slightly higher on the first harmonics, the decrease seems to be a bit faster than the OC case. In general, the OC behaves more monotonically in the CE frequency range and more oscillating in the RE frequency range, that is, more peak of resonances. For loaded cases, the oscillations seems to be damped , yet fuzzy “bourdonnant”. Such behaviour may be quite complicated to model and could be related to exterior factors, such as load and saturation, cable interactions and etc.

It is conclude that the OC can be in general a representative case for the near field, mainly at the input part (in which HFO is well observed). It is capable of identifying an important resonance frequency (the 80 MHz) that is present due to hard switching operation.. Future studies to understand such resonance are still required! On the other hand, one can suppose as a worst case condition that the output presents the same harmonic content as the input, in such a way that the information in middle to high frequency (30 MHz – 100 MHz), by loaded cases is not lost. By assuming such aforementioned facts, OC step-up mode can be used to generate EMI signature. Clearly, the OC test generates results, at the very least, results with the order of magnitude in dB unities. Other OC tests for unitary and buck cases could be used. A function containing the maximum values of each mode results (buck, unitary and boost) could be enough to well represent, in a conservative way, the produced near field.

The possibility of acquiring EMI signature and its electrical correlation through non-intrusive near field measurement of strategic points and simple OC testing could be generalized to any power converter, and not only the PCA approach. This is particularly true for the DAB, as explained in this thesis in which electrical waveforms and models are well known through theoretical results. Being capable of recognizing resonance peaks and its cause at early stage can be time and money saving. Such method can be applied for any DAB for first insights and correlation with electrical behaviour at very early stages. Future studies include the use of TEM cell to characterize the multi-cell converter and tests at anechoic chambers. The idea is to well correlate the near field measurements locations that are better suited as an image with respect to far-field emissions.

Once again, the EMC analysis of a PCA can be performed from a unique converter cell. The idea to construct a database out of easy and accessible experimental setups to learn and replicate for other standardized blocks has been proved to be true for EMC aspects in multi-cell converter approaches regarding the near field measurements.

In order to perform optimization among infinity possible solutions, one does not need to look for accuracy between theoretical and experimental results, but rather comparative and quantitative. Simple and inexpensive setups may be used to compare different designs and

configuration to choose the most convenient solution. Likewise, over complicated results from simulation may be not so necessary.

Besides the partial conclusion and perspective already discussed on each subsection, a future work is the discussion of the distributed vs centralized filter observing the emitted fields. Then, a comparison with results produced in certified EMC laboratories to compare, co-relate and conclude on the EMI signature and its managing. That is, professional testing in an anechoic chamber for far field measurements; as well as more sophisticated and accurate tools and near field measurements, always with the goal of co-relating and checking with the inexpensive EMC setups. The EMC testing setup can be improved through appropriated TEM cell size, fixed home-made near field probe, fixed microcontroller to generate signals, output voltage and current control, and sensors). The PCA and CSCs can also be improved by facilitating measurements of important electrical parameters, making available the possibility of independent duty-ratio control and different modulations. This can at one hand increase volume and price, but the focus is to develop platforms that are suitable more for testing and database with a large amount of experimental results to draw conclusions

Reference Chapter 6

[1] J. He, Z. Guo, and X. Li, "Mechanism Model and Prediction Method of Common Mode Radiation for a Nonisolated Very-High-Frequency DC–DC Converter With Cables," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10227–10237, Oct. 2020, doi: 10.1109/TPEL.2020.2978278.

[2] Y. Zhang, S. Wang, and Y. Chu, "Analysis and Comparison of the Radiated Electromagnetic Interference Generated by Power Converters With Si MOSFETs and GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8050–8062, Aug. 2020, doi: 10.1109/TPEL.2020.2972342.

[3] B. Zhang and S. Wang, "A Survey of EMI Research in Power Electronics Systems With Wide-Bandgap Semiconductor Devices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 626–643, Mar. 2020, doi: 10.1109/JESTPE.2019.2953730.

[4] Y. Zhao *et al.*, "The radiated EMI noise modeling and features analysis on the basis of Smart Grid Equipments," in *2014 International Symposium on Electromagnetic Compatibility*, Gothenburg: IEEE, Sep. 2014, pp. 1199–1202. doi: 10.1109/EMCEurope.2014.6931086.

[5] B. Zhang, H. Zhao, and S. Wang, "Near Magnetic Field Emission Analysis for IGBT and SiC Power Modules," in *2020 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, Reno, NV, USA: IEEE, Jul. 2020, pp. 411–416. doi: 10.1109/EMCSI38923.2020.9191684.

[6] J. Aime *et al.*, "Prediction and measurement of The magnetic near field of a static converter," in *2007 IEEE International Symposium on Industrial Electronics*, Vigo, Spain: IEEE, Jun. 2007, pp. 2550–2555. doi: 10.1109/ISIE.2007.4375009.

[7] Z. Ariga and K. Wada, "Analysis and evaluation of near field noise voltage on power electronics circuits," in *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, Taipei: IEEE, Nov. 2009, pp. 1014–1019. doi: 10.1109/PEDS.2009.5385836.

[8] C. Labarre and F. Costa, "Circuit Analysis of an EMI Filter for the Prediction of its Magnetic Near-Field Emissions," *IEEE Trans. Electromagn. Compat.*, vol. 54, no. 2, pp. 290–298, Apr. 2012, doi: 10.1109/TEMC.2011.2159563.

[9] C. Labarre, F. Costa, and J. Ecrabey, "Correlation between the near magnetic field radiated by an EMI filter and its electric working," in *2010 IEEE Vehicle Power and Propulsion Conference*, Lille, France: IEEE, Sep. 2010, pp. 1–5. doi: 10.1109/VPPC.2010.5729189.

[10] C. Labarre, F. Costa, O. Aouine, and J. Ecrabey, "Modelling and analysis of the magnetic field radiated by a three phased inverter," in *2010 IEEE International Symposium on Industrial Electronics*, Bari, Italy: IEEE, Jul. 2010, pp. 927–932. doi: 10.1109/ISIE.2010.5637100.

[11] O. Aouine, Cé. Labarre, and F. Costa, "Measurement and Modeling of the Magnetic Near Field Radiated by a Buck Chopper," *IEEE Trans. Electromagn. Compat.*, vol. 50, no. 2, pp. 445–449, May 2008, doi: 10.1109/TEMC.2008.922794.

[12] V. Ardon, J. Aime, O. Chadebec, E. Clavel, J.-M. Guichon, and E. Vialardi, "EMC Modeling of an Industrial Variable Speed Drive With an Adapted PEEC Method," *IEEE Trans. Magn.*, vol. 46, no. 8, pp. 2892–2898, Aug. 2010, doi: 10.1109/TMAG.2010.2043420.

[13] Y. Chen, X. Pei, S. Nie, and Y. Kang, "Monitoring and Diagnosis for the DC–DC Converter Using the Magnetic Near Field Waveform," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1634–1647, May 2011, doi: 10.1109/TIE.2010.2051939.

[14] A. Virdi, P. Salunkhe, D. Choudhary, and T. Mahadik, "Enhancement of PCB Design for Radiated Immunity Compliance in Analog Signal Measurement," in *2018 15th International Conference on ElectroMagnetic Interference & Compatibility (INCEMIC)*,

Bengaluru (Bangalore), India: IEEE, Nov. 2018, pp. 1–4. doi: 10.1109/INCEMIC.2018.8704577.
[15] "IEEE Standard for Safety Levels with Respect to Human Exposure to Electric, Magnetic, and Electromagnetic Fields, 0 Hz to 300 GHz," IEEE. doi: 10.1109/IEEESTD.2019.8859679.
[16] N. Sivaraman, K. Jomaa, and F. Ndagijimana, "Three dimensional scanning system for near-field measurements," in *2017 11th European Conference on Antennas and Propagation (EUCAP)*, Paris, France: IEEE, Mar. 2017, pp. 2866–2870. doi: 10.23919/EuCAP.2017.7928798.
[17] B. Zhang and S. Wang, "Analysis and Reduction of the Near Magnetic Field Emission From Toroidal Inductors," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6251–6268, Jun. 2020, doi: 10.1109/TPEL.2019.2953748.
[18] H. Chen, T. Wang, L. Feng, and G. Chen, "Determining Far-Field EMI From Near-Field Coupling of a Power Converter," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5257–5264, Oct. 2014, doi: 10.1109/TPEL.2013.2291442.
[19] X. Li and L. D. Xu, "A Review of Internet of Things—Resource Allocation," *IEEE Internet Things J.*, vol. 8, no. 11, pp. 8657–8666, Jun. 2021, doi: 10.1109/JIOT.2020.3035542.
[20] J. V. Ahuir, "Going Wireless with Magnetic Shielding".
[21] G. de Freitas Lima, F. Ndagijimana, Y. Lembeye, and J.-C. Crebier, "Prediction and Optimization of Near Magnetic Field Produced by Interconnections of Multi-cell Converters," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.
[22] G. de Freitas Lima, F. Ndagijimana, Y. Lembeye, and J.-C. Crebier, "Un algorithme simple pour la prédiction du champ magnétique proche et l'optimisation des interconnexions des réseaux de convertisseurs de puissance," in *Symposium de Génie Electrique 2021 (SGE 2021)*, Nantes, France, Jul. 2021. [Online]. Available: https://hal.science/hal-03352411
[23] M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, "Design of a Highly Efficient (97.7%) and Very Compact (2.2 kW/dm ^{3}) Isolated AC–DC Telecom Power Supply Module Based on the Multicell ISOP Converter Approach," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7750–7769, Oct. 2017, doi: 10.1109/TPEL.2016.2633334.
[24] J. H. Kim, B. H. Choi, H. R. Kim, and C. T. Rim, "2-D Synthesized Magnetic Field Focusing Technology With Loop Coils Distributed in a Rectangular Formation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5558–5566, Jul. 2019, doi: 10.1109/TIE.2018.2869362.
[25] M. Misakian, "Equations for the magnetic field produced by one or more rectangular loops of wire in the same plane," *J. Res. Natl. Inst. Stand. Technol.*, vol. 105, no. 4, p. 557, Jul. 2000, doi: 10.6028/jres.105.045.
[26] V. Shatri, R. Sefa, and L. Kurtaj, "MATLAB Partial Element Equivalent Circuit Toolbox for Solving Coupled Electromagnetic-Circuit Problems," *International Journal of Current Engineering and Technology*, 2013.

General conclusion and future perspectives

During the first phase of the work, the effort was concentrated on designing a CSC made of DAB operating with SPS modulation considering not only efficiency and power density, but also how the operating point and electrical parameter choices can affect the DM and CM noises. Indeed, the static gain, output current and ZVS region are parameters that can direct impact on the circulating current noise. The mathematic analysis was performed in a normalized and dimensionless whenever it was possible, being a function of only four variables (static gain; output parametrized currents, one as a function of the AC-link inductance and the other as a function of C_{oss}; and quality factor). This can facilitate the design through abacus and optimization by limiting the space design. The main goal was to design a DAB that could perform ZVS at rated power and no forced cooling. For simplifying the analysis of CM noise model, new equivalent circuit and simplifying assumptions are proposed and discussed theoretically by comparing with other models, including simulations, and references. The symmetrisation of a DAB with respect to AC-link has been proved to be extremely impactful on CM noise generation. Even though such approach can occupy more volume and be less efficient, the adoption for the sake of predictability, simplicity and standardization and CM noise reduction is observed.

Regarding DM observation of multi-cell converter / modular converters operating at common-duty ratio signal, fundamental and unifying theory are lacking on the literature, including misconceptions being diffused. The complexity of interactions of multi-cell converters and PCA, requires analysis that can take into account component dispersion due to precision of the devices as well as different parasitic elements, high frequency and saturated models. Such analysis can be performed through switched models as in PSIM and LTspice, but such tools cannot generalize concepts and are time consuming. Complex and evolving systems require physical and mathematical analysis through simplifying assumptions equivalent circuits for the sake of performant taking decisions. Firstly, it is provided a theory that attempts to unify and systematically define rules for connection realization, to define properties such as power invariance to connection configuration and, finally to easily find closed solution of voltage, current and power sharing's. For the CM noise, a simple simplifying assumption of short-circuiting both input and output ports of all CSCs was responsible to affirm that the CM current is more or less independent on the connection

configuration. Besides, it allows to reach ideas of an approach based on evenly shifting 180° the CSCs, that was fundamental for the outstanding result regarding CM noise attenuation.

Finally, simple experimental setups for EMC signature acquiring is effective for any power converter improvement, and it is more or less used on the industry sides. On the other hand, such topics are not so discussed in the academic level, which focus mostly on accuracy between theoretical and practical results, at the cost of time and curve fittings. This becomes increasingly more complex for the RE frequency range, with so many devices, topologies and choices. Predicting each harmonic content with accuracy is not required for EMC complience, but rather its maximum. Also the appreciation of which one is best or worst in terms of EMC is not easy to define. For example, at one case most harmonics can be lower than another case, except for an identified resonance peak observed in the EMI receiver. This resonance peak can be quite complicated to manage, and the entire EMC treating most be dimensioned for such maximum peak. Being capable of recognizing resonance peaks at early stage can be time and money saving. The idea of building and improving a technology from the data acquired by experimental results was important for the success presented in this work. For example, the improving of CM noise was readily verified through a setup that could take different configurations of driving the CSCs through simple, still performant, physical connectors. Something that was merely suspiciously impactful, turned out to be a significant CM noise attenuator. We can only wonder how many other simple ideas can still be found. Well, the PCA philosophy is a perfect opportunity for such merit.

Perhaps the PCA technology was and may never be suitable for private company industries; not only through the main argument of price, but also that the homogenous and standardized solutions are not in favour of competition and stock market. On the other hand, the PCA approach is an opportunity for open-source and power electronics learning disclosure. Moreover, as it could be noticed, a philosophy of building any power converter from standardized blocks and functions. Even though, not so much appreciated on the market, it can be well used for academic and pedagogic purposes. As the level of highly complex knowledge is not required, turning a multi-dimensional and complex task such as EMC standard compliance into a sort of puzzle problems based on simple and basic ideas, such as current opposition and dipole such subject can be well appropriated by undergraduate and master students. An example would providing the same kits of CSCs, PCA, inexpensive near field probes and TEM cells for different academic institutions and promote a challenges, as an example of International Future Energy Challenge (IFEC) or google box challenges. The research in PCA can be developed exponentially, due to an infinity number of solutions within standard blocks, while data basing the results, which itself should be standardized.

Future studies include studying and implementing more sophisticated modulations that can improve efficiency and power density, always observing the EMC compliance. The idea is therefore the PCA, CSCs and setup platforms not thinking only on size and volume (which was before done), but rather highly configurable (e.g. independent duty-ratio signal, different modulations, redundancy and fault protection) and easy for manipulation (e.g. access to important electrical points). Evaluating not only EMC aspects, but many others such as control, efficiency, costs, carbon footprint and etc…

Regarding the proposed two-port network based theory, more investigation and use of such tool for multi-cell converter design is required. Besides, it may be possible to combine and couple with CM noise models.

Experimental results to verify experimentally the impact on EMC over the entire frequency range of distributed and centralized filter solutions are still required. Besides, the verification and co-relation between near-field probe and TEM cell as well as the OC condition must be performed in certified EMC testing laboratories.

Finally, a theoretical and experimental comparison between PCA and conventional power converter approach in terms of size, volume and time to pass EMC standards can clarify the advantages and disadvantages among them.

7.Résumé en Français

7.1 Introduction Générale

Récemment, d'importants progrès ont été réalisés dans la conception automatisée en électronique de puissance. Ces progrès sont soutenus par des modèles et des simulations, mais avec des fonctionnalités interactives limitées. Des études ont montré que la question des émissions électromagnétiques (EMI) doit être prise en compte dès la phase initiale. Pour cela, un modèle temporel en commutation peut être utilisé pour fournir la signature des émissions conduites (CE). Cependant, l'extraction des éléments parasites nécessite généralement un temps de calcul important, ce qui peut rendre le processus fastidieux. Il est possible de comprendre la signature EMI en construisant des équations analytiques ou équivalentes, ainsi que grâce à des résultats expérimentaux.

La thèse vise à concevoir rapidement et automatiquement en électronique de puissance, en utilisant la méthode Power Electronics Design 4.0. Cette méthode permet une conception assistée et augmentée, mais le problème des émissions électromagnétiques peut compliquer le processus. Ainsi, avant d'arriver à une solution optimale basée sur l'intelligence artificielle et la simulation virtuelle, il est nécessaire d'avoir une grande quantité de données expérimentales, de simulations et d'analyses. Pour faciliter l'automatisation de la conception en électronique de puissance, il existe une méthodologie développée par G2Elab, appelée "Réseau de Convertisseurs" en français, ou "Power Converters Arrays" (PCA) en anglais, qui intègre le concept de convertisseur modulaire.

7.2 Chapitre 1 : Réseau de convertisseurs : une opportunité pour la conception automatisée en matière de CEM

Afin de familiariser le lecteur, des concepts fondamentaux de compatibilité Électromagnétique (CEM) sont présentés. Ces notions sont utiles pour mieux appréhender les *Chapitres* suivants. La première sous-section de ce *Chapitre* est une revue générale de la littérature et une introduction sur la CEM liée aux convertisseurs de puissance. Dans cette thèse, les harmoniques liés aux émissions conduites ou rayonnées seront étudiés, comme présenté dans la *Figure 7.1*.

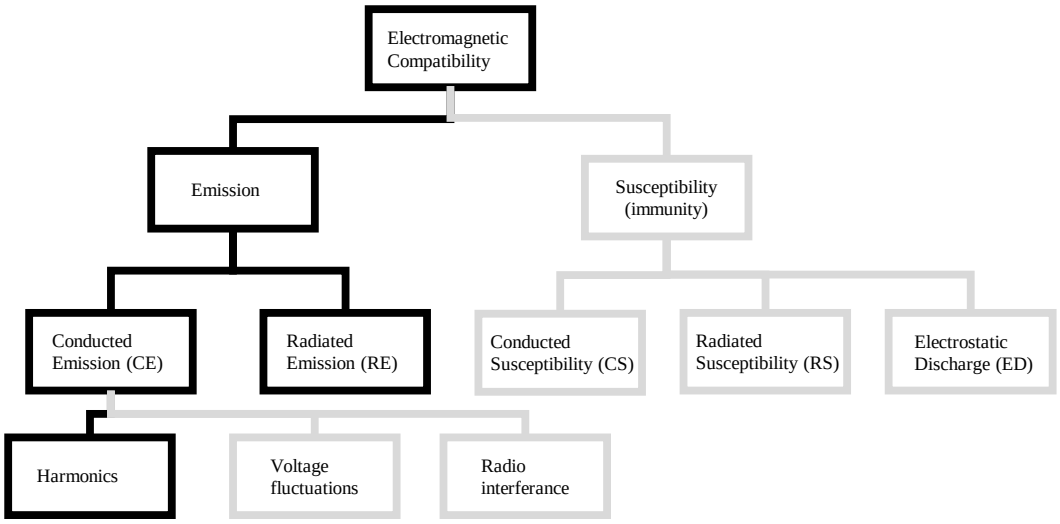
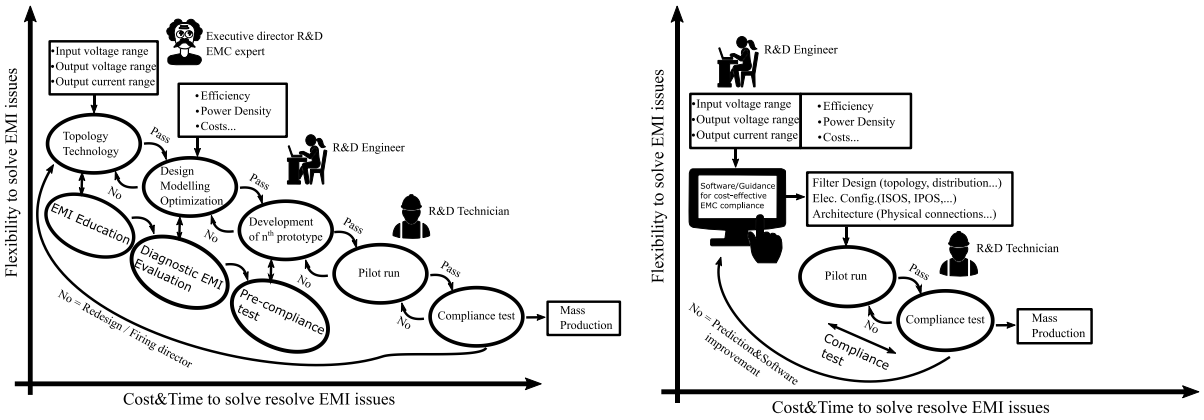


Figure 7.1 Subdivision classique des catégories d'étude CEM. (En noir les sujets qui sont traités dans cette thèse).



(a) *(b)*

Figure 7.2 Méthodologie de conception et de prototypage d'un convertisseur de puissance: (a) tâches CEM conventionnelles et conseillées en parallèle avec la conception du convertisseur de puissance CC/CC pour la certification CEM.; (b) conception et fabrication automatisée axée sur la CEM dans laquelle cette thèse vise à ouvrir une opportunité.

Ensuite, dans la *Figure 7.2 (a)*, on présente l'approche conventionnelle de prototypage suivant en parallèle les tâches de CEM Dans la Figure (b), l'objectif ultime de cette thèse est, donc, de pouvoir prototyper très rapidement un convertisseur de puissance de n'importe quel cahier des charges.

Afin d'atteindre cet objectif, il est primordial de comprendre les nombreuses approches possibles pour atténuer les émissions conduites, comme illustré dans la *Figure 7.3* (les sujets en gras indiqués dans la figure sont ceux sur lesquels cette thèse se concentre et apporte des commentaires pertinents).

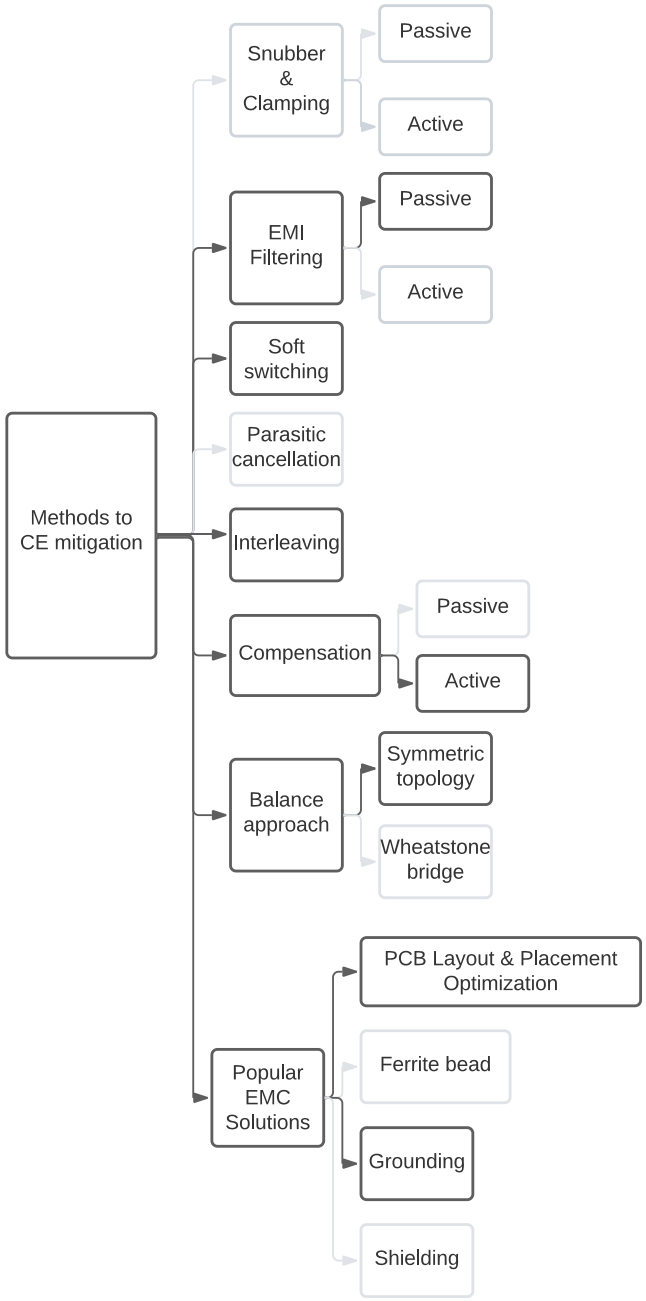


Figure 7.3 Méthodes d'atténuation des EMI appliquées aux convertisseurs de puissance (les sujets encadrés en gras sont appliqués ou discutés dans cette thèse).

Dans la deuxième partie de ce *Chapitre*, la brique de technologie développée par G2Elab, et nommée « Power Converters Arrays » (PCA) qui comprend le concept de réseau de convertisseurs modulaires, et la méthodologie utilisée dans cette thèse sont décrits, comme présenté dans la *Figure 7.4* La cellule de conversion (CSCs) est un simple Dual Active Bridge (DAB), présenté dans la *Figure 7.5* avec une modulation single phase-shift (SPS). L'objectif n'est pas seulement d'optimiser le convertisseur de puissance en termes d'efficacité et de densité de puissance, mais également de prendre en compte tous les aspects de CEM, tels que les normes de compatibilité électromagnétique (CE) et les émissions rayonnées (RE).

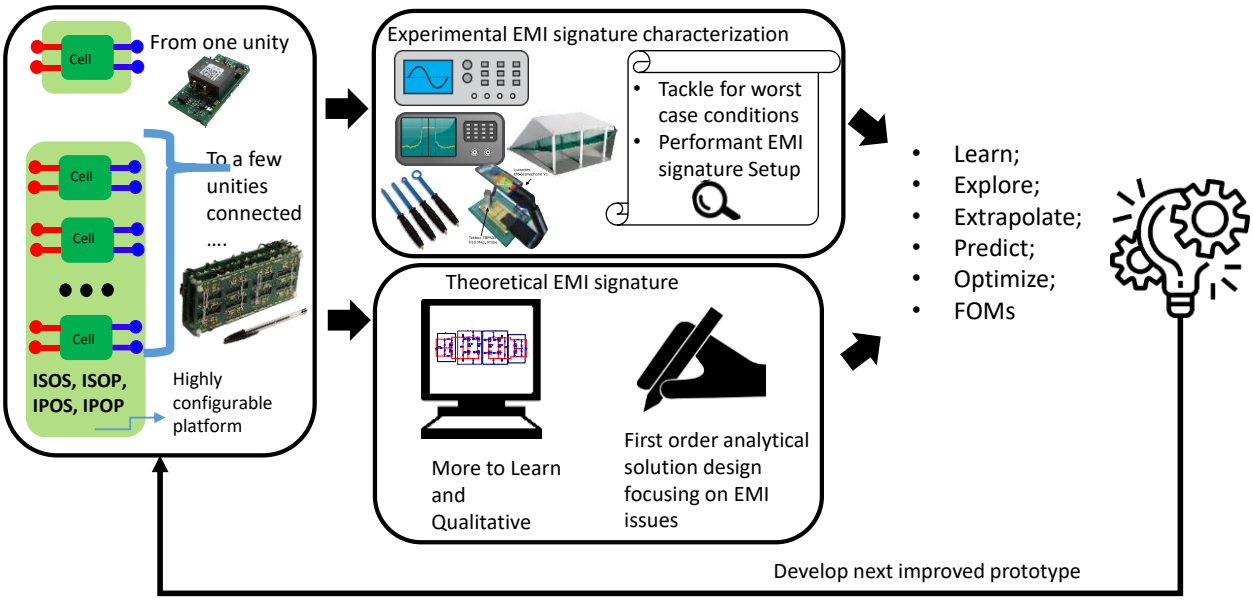


Figure 7.4 Ce diagramme représente la méthodologie basée sur la signature EMI et apprend des résultats à la fois théoriques et pratiques.

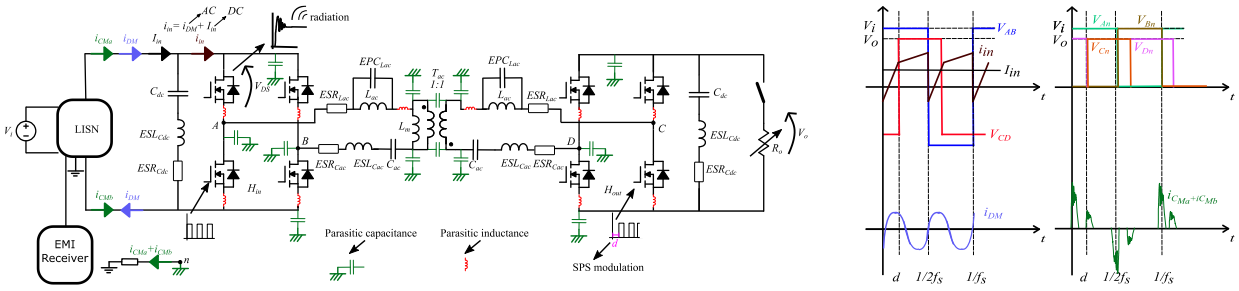


Figure 7.5 Modèle « Circui » et chemin de propagation pour étudier la signature EMI d'un DAB (à gauche) ; Formes d'ondes principales dans le domaine temporel d'un DAB (à droite).

Enfin, comme le montre la *Figure 7.6*, cette thèse se situe à l'intersection de quatre sujets principaux : CEM (Compatibilité Électromagnétique), Dual Active Bridge

(utilisé comme convertisseur de cellule), Convertisseurs Modulaires et Conception Automatisée.

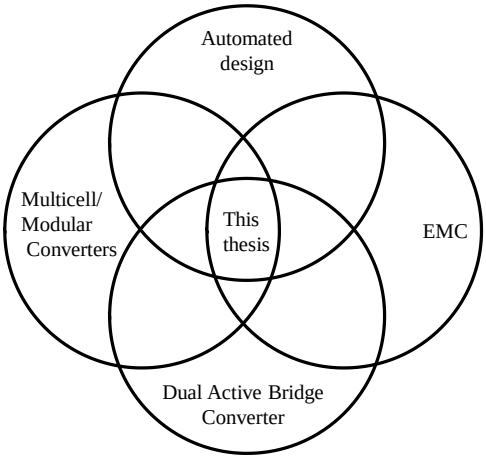


Figure 7.6. Quatre domaines de recherche se croisent dans cette thèse.

7.3 Chapitre 2 : Modélisation et conception du DAB (SPS) en se concentrant sur Mode Différentiel

Le principal objectif est de fournir, à travers un circuit équivalent simplifié et une analyse sans dimension, l'impact des choix de conception sur les performances en commutation douce, Zero Voltage Switching an anglais (ZVS) et les amplitudes harmoniques hautes fréquences de mode différentielle (DM), liées à la fréquence de commutation, $H_{1_{in}}$, à l'inductance de liaison AC (AC-link), L_{ac}, et à la capacité C_{oss} des transistors MOSFETs.

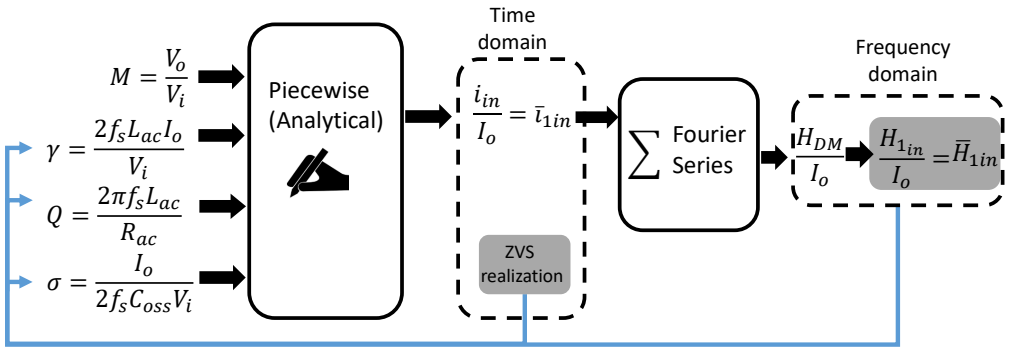


Figure 7.7 Méthodologie utilisée pour dériver l'amplitude de l'harmonique de mode différentiel.

L'inclusion des pertes AC joules dans le modèle, R_{ac}, est discutée et comparée à un modèle sans perte. Grâce à une paramétrisation, il est possible de réduire le nombre de variables à 4, tout en fournissant des résultats normalisés, comme illustré dans la *Figure 7.7*.

Ces paramètres de conception sont particulièrement pertinents car ils permettent de cartographier la première harmonique, ainsi que de prendre en compte les pertes de conduction et les valeurs efficaces des grandeurs électriques, comme présenté dans la *Figure 7.8*. Différentes options de conception sont abordées et l'évolution d'une cellule DAB (CSC) en fonction de la fréquence de commutation et du AC-link est justifiée.

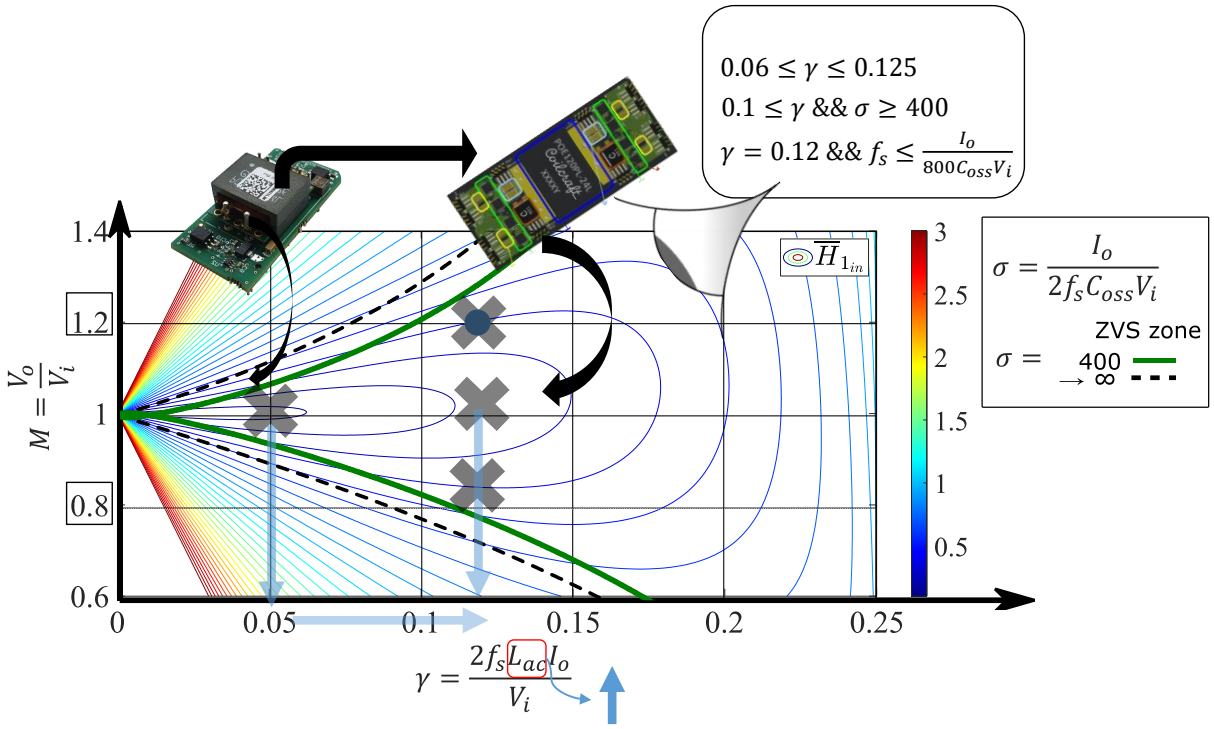


Figure 7.8 Méthodologie pour concevoir le DAB à travers une analyse de cartographie sans dimension basée sur les performances ZVS et la réduction de la première harmonique de mode différentiel.

L'évolution de la cellule DAB en augmentant le AC-link, comme présenté dans la *Figure 7.9*, ouvre de nouvelles possibilités d'application tout en améliorant la gestion des problèmes d'EMI, grâce à l'accomplissement du ZVS pour une large plage de puissance. Cette approche offre des avantages considérables, notamment une plus grande polyvalence du DAB pour diverses applications et une meilleure atténuation des émissions électromagnétiques.

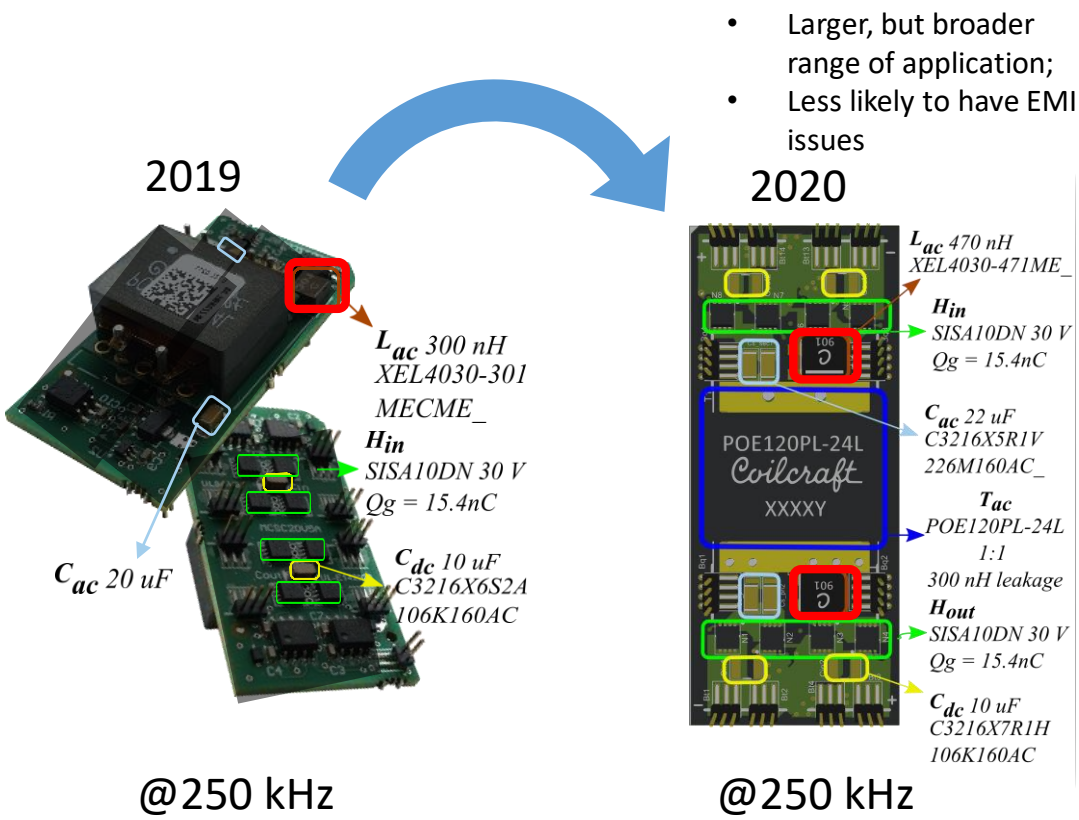


Figure 7.9 L'évolution de la cellule DAB en augmentant le AC-link permet d'élargir la gamme d'applications et de réduire le risque de problèmes d'EMI, car le ZVS est atteint pour une large plage de puissance.

Obtenir la signature EMI du DAB avec la modulation SPS n'est pas facile et ne peut pas être simplement décrit par une dépendance linéaire par rapport aux puissances nominales. Cela est dû au fait que la signature EMI dépend du *dv/dt*, principalement de la tension drain-source, qui perd sa performance ZVS à faible puissance. Comme le montre la Figure *7.10*, des points de fonctionnement importants et critiques, délimités par la région ZVS des ponts en H d'entrée et de sortie, doivent être observés. Avec l'inclusion de la résistance AC dans le modèle, il a été observé que la condition d'essai en circuit ouvert (points A, K et F) n'est pas un point singulier, mais plutôt un point représentatif dans lequel le courant au moment de la commutation et le commutation forcée / ZVS peuvent être bien identifiés et calculés. En intégrant la résistance AC dans le modèle, il a été observé que la condition de test en circuit ouvert (points A, K et F) n'est pas un point singulier, mais plutôt un point représentatif, où le courant au moment de la commutation et le commutation forcée / ZVS peuvent être bien identifiés et calculés. Des résultats expérimentaux approfondis dans ce *Chapitre et les Chapitres* suivants ont clairement démontré que la condition de test en circuit ouvert est

représentative, voire plus critique que la puissance nominale (mode élévateur et courant nominal) en ce qui concerne les émissions conduites et rayonnées dans la plage de fréquences élevées, notamment pour le mode commun (CM).

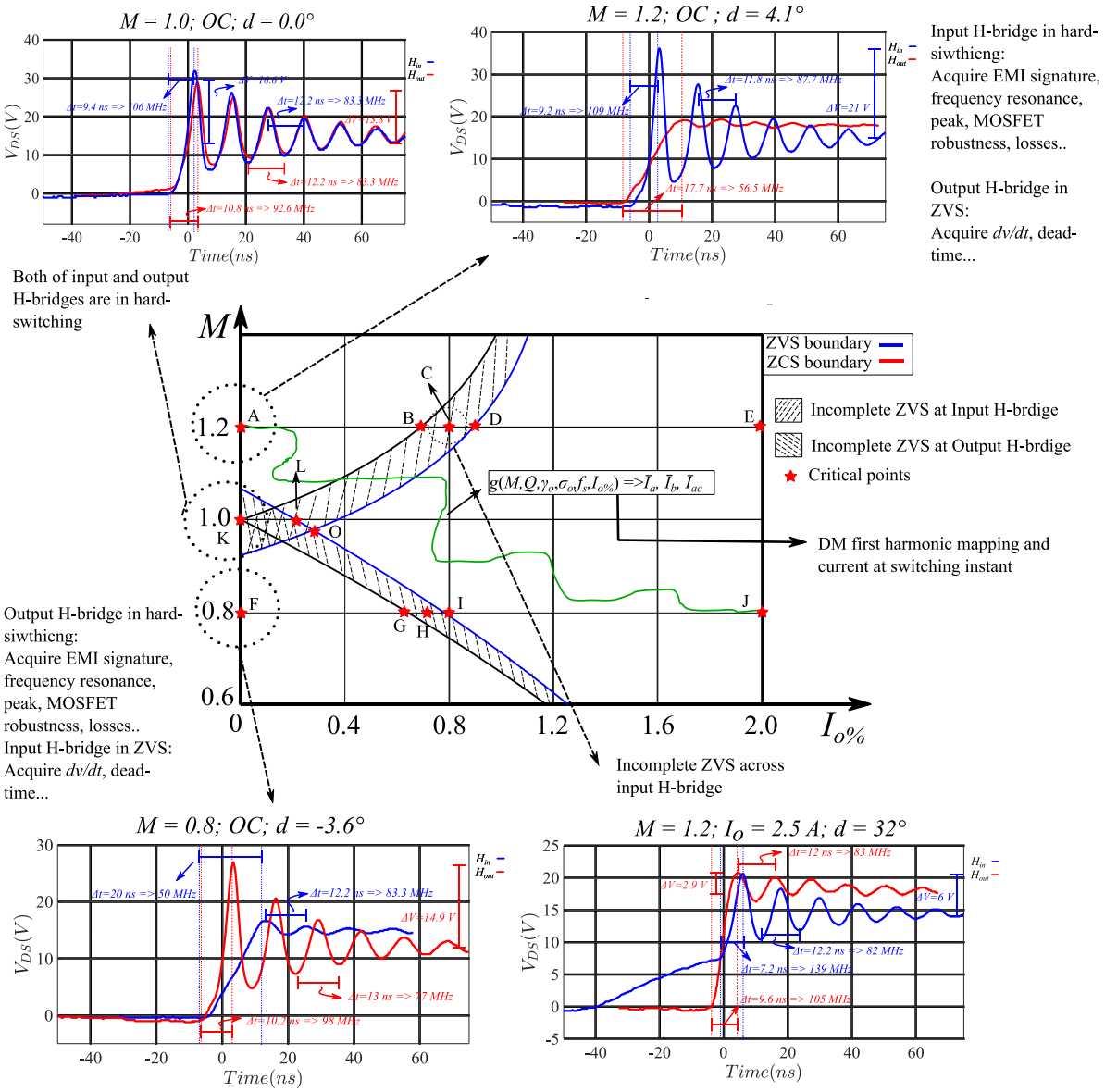


Figure 7.10 Analyse des paramètres importants ayant un impact sur la signature EMI, tels que les limites ZVS et ZCS, le courant circulant AC et le courant au moment de la commutation, en abordant des points critiques et importants dans le plan (M vs $I_{o\%}$). Des mesures expérimentales sont également présentées pour différentes conditions de fonctionnement à travers la tension drain-source.

7.4 Chapitre 3 : Modélisation et conception du DAB (SPS) en se concentrant sur le Mode Common

Ce *Chapitre* débute par une revue de la littérature sur la modélisation des émissions conduites du DAB et explique comment les problèmes ont été résolus dans des études antérieures. Pour résoudre ces problèmes, une première solution simple a été adoptée : elle consiste à utiliser la tension drain-source normalisée, calculée dans le *Chapitre 2*, et à l'exprimer dans le domaine fréquentiel, comme présenté dans la *Figure 7.11*. Cette approche permet de mieux comprendre les caractéristiques spectrales de l'émission conduite du DAB et ouvre la voie à une analyse plus détaillée des émissions.

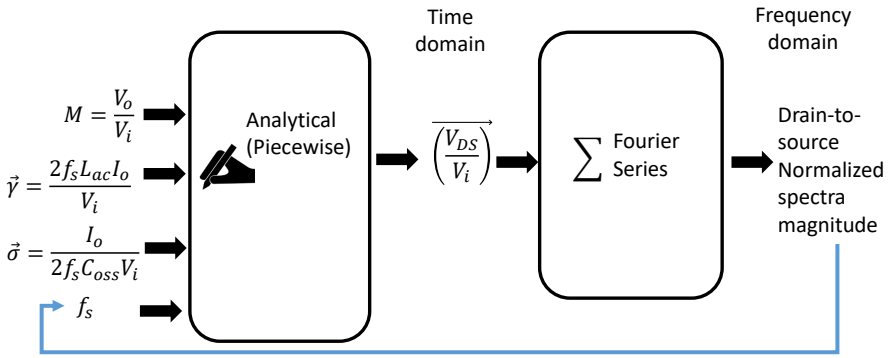


Figure 7.11 Méthodologie utilisée pour dériver l'amplitude normalisée de spectre électromagnétique conduit (les harmoniques) de drain-source voltage.

La *Figure 7.12* présente le spectre CEM d'un DAB en maintenant γ constant et en réduisant la fréquence de commutation. Cette analyse révèle des résultats intéressants : il est possible de réaliser une amélioration de 9,5 dB dans la plage des émissions conduites et d'environ 8 dB dans la plage des émissions rayonnées. Ces améliorations significatives démontrent l'impact positif de la réduction de la fréquence de commutation sur les niveaux d'émission du DAB. Ces conclusions ouvrent la voie à des possibilités d'optimisation pour réduire les émissions électromagnétiques indésirables du DAB et améliorer ses performances en termes de compatibilité électromagnétique.

Suite à cette analyse simple, un nouveau DAB a été développé et présenté dans la *Figure 7.13*. Pour maintenir le même courant paramétré de sortie, l'inductance a été augmentée une fois de plus en raison de la réduction de la fréquence de commutation. En augmentant symétriquement l'inductance et en réduisant la fréquence de commutation, il est possible d'atténuer considérablement les émissions conduites liées au mode commun. Grâce à cette approche, le DAB a été optimisé pour offrir de meilleures performances en termes de

réduction des émissions électromagnétiques tout en maintenant la stabilité et la fiabilité du système.

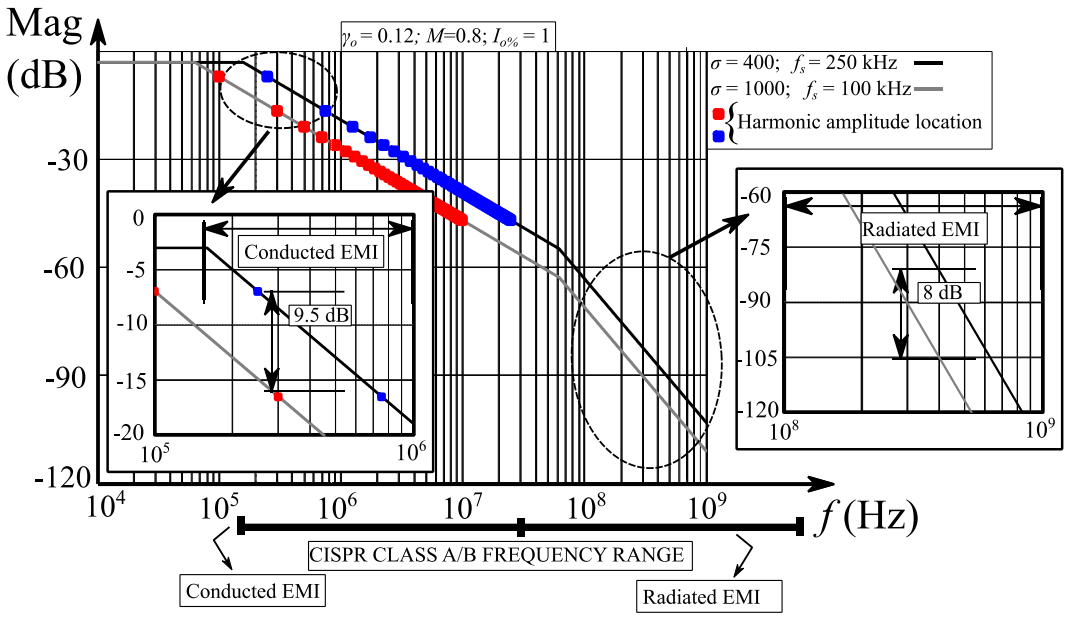


Figure 7.12 Spectre de magnitude normalisé de la tension drain-source pour γ = 0.12, σ = 400 et f_s = 250 kHz (en bleu) et γ = 0.12, σ = 1000 et f_s = 100 kHz (en rouge).

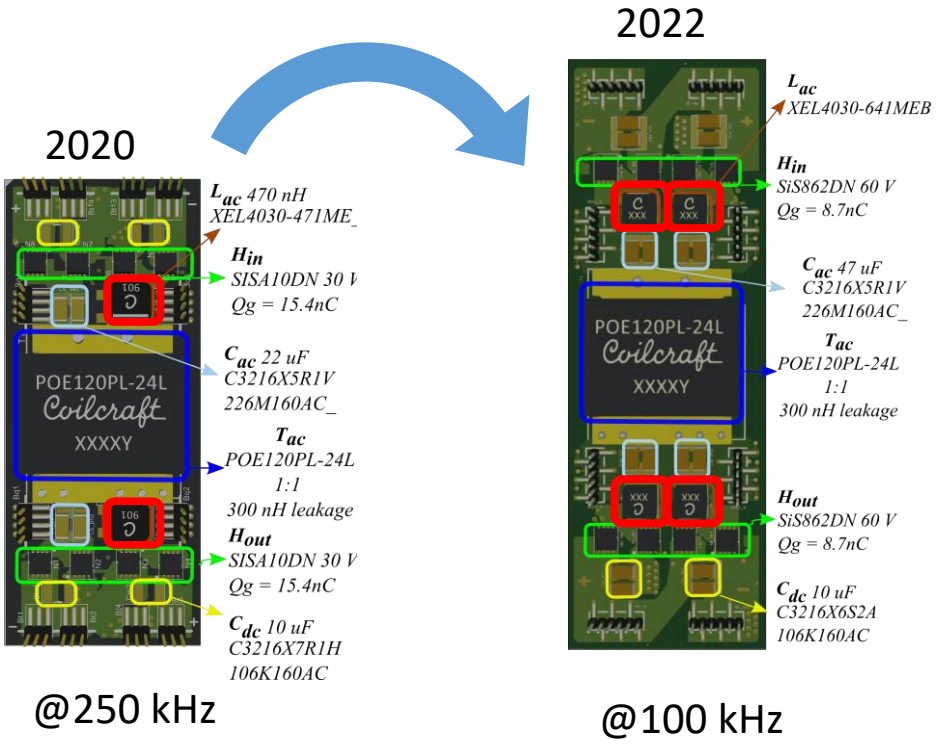


Figure 7.13 L'évolution de la cellule DAB en augmentant le AC-link inductance de manière symétrique et un réduisant la fréquence de commutation permet de réduire les émissions conduites liées au mode commun.

Ce chapitre se concentre principalement sur l'impact de la symétrisation du AC_link dans de nombreux scénarios, comme illustré dans la *Figure 7.14*, qui s'est avérée être non négligeable tant sur le plan théorique que pratique. Pour étayer cette étude, des simulations numériques ont été effectuées en utilisant PSIM, en suivant la méthodologie présentée dans la Figure 7.15. Les résultats théoriques et pratiques obtenus permettent de valider les avantages de la symétrisation, tels qu'illustrés dans la *Figure 3.17*. Comme nous le constatons et pouvons en conclure, la modélisation s'est avérée qualitativement précise en mettant en évidence les principales résonances et tendances, ce qui correspond aux résultats obtenus lors des essais pratiques. Cette concordance entre les résultats théoriques et pratiques renforce la validité et la fiabilité de la modélisation utilisée.

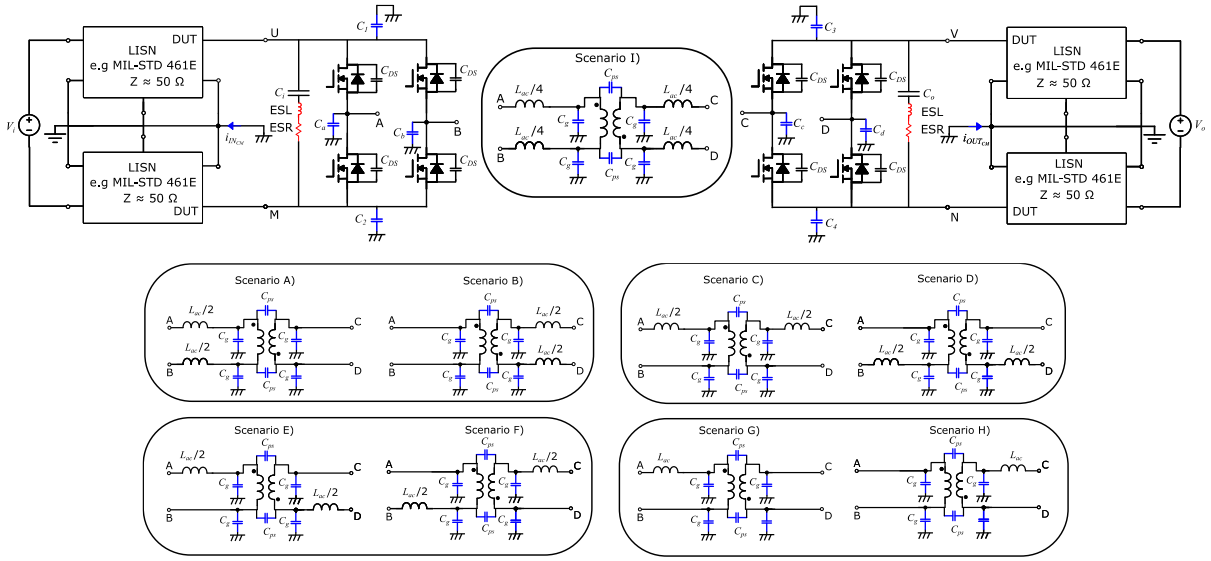


Figure 7.14 Le modèle commuté dans la simulation (l'entrée et la sortie sont connectées à des sources de tension via deux filtres d'impédance spécifiés pour la norme CISPR).Et chemins d'impédance du AC-link selon différents scénarios avec des inductances équivalentes identiques.

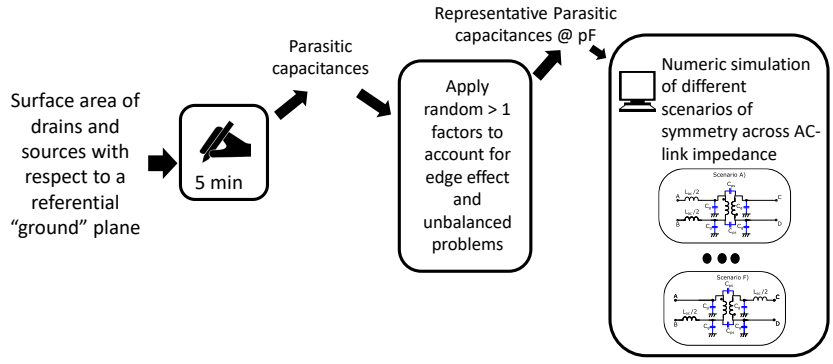
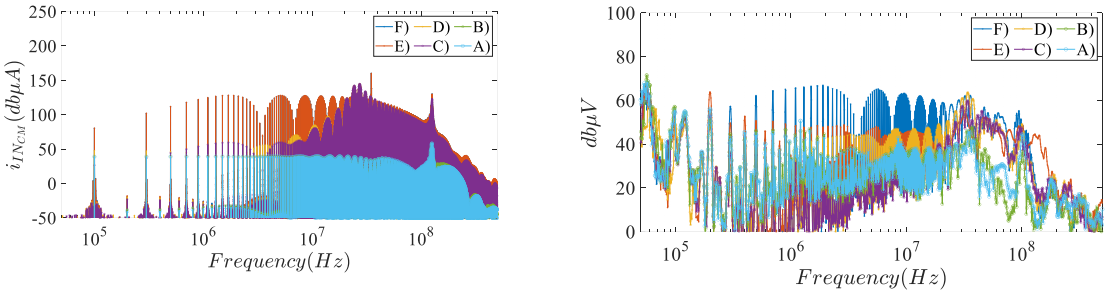


Figure 7.15 Méthodologie utilisée pour modéliser et obtenir des résultats numériques pour plusieurs scenarios du chemin d'impédance du AC-link.



(a) *(b)*

Figure 7.16 *Spectre EMI pour différents scénarios : (a) résultats théoriques ; (b) résultats pratiques.*

Enfin, pour une compréhension approfondie des résonances et des amplitudes, il est nécessaire de simplifier les circuits équivalents. Ainsi, un nouveau modèle CM équivalent au modèle commuté a été dérivé, dont les résultats démontrent une amélioration par rapport au modèle CM dérivé à l'aide du théorème de substitution déjà présenté dans la littérature. Cette amélioration est attribuée à la prise en compte de l'asymétrie de la capacité parasite par rapport à la masse à travers le pont en H, ainsi qu'à l'absence de court-circuit des condensateurs du lien DC dans le modèle proposé. Par conséquent, le modèle proposé permet d'observer et de comprendre de manière précise le mode mixte (MM) qui est responsable des harmoniques paires (communément produites par le bruit DM) et des résonances hautes fréquences.

Les résultats de tracé présentés dans la Figure 7.15 démontrent que le modèle commuté et le modèle proposé concordent exactement dans le domaine fréquentiel. Cette précision renforce la validité et l'utilité du modèle proposé, qui offre une meilleure compréhension des phénomènes complexes liés aux émissions électromagnétiques du système.

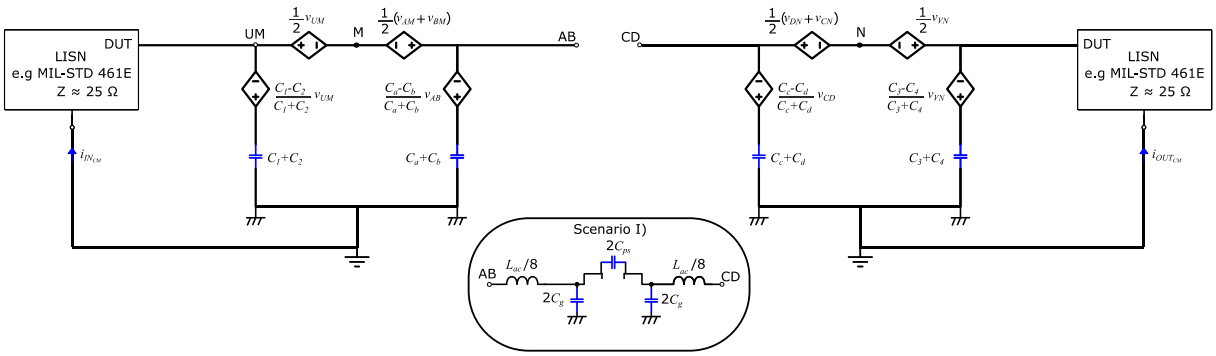


Figure 7.17 Modèle CM équivalent proposé du DAB.

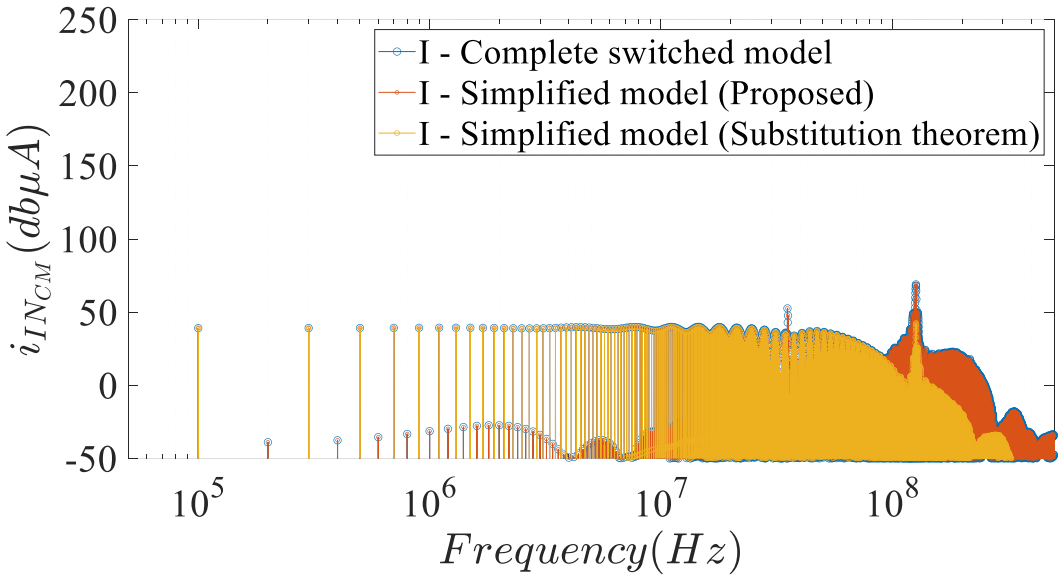


Figure 7.18 Résultats du modèle commuté; du modèle simplifié basée sur le théorème de substitution; et du modèle proposé.

7.5 Chapitre 4 : Analyse généralisée et unifiée de l'impact des disparités des composants d'un convertisseur modulaire à travers la théorie de réseau à deux ports.

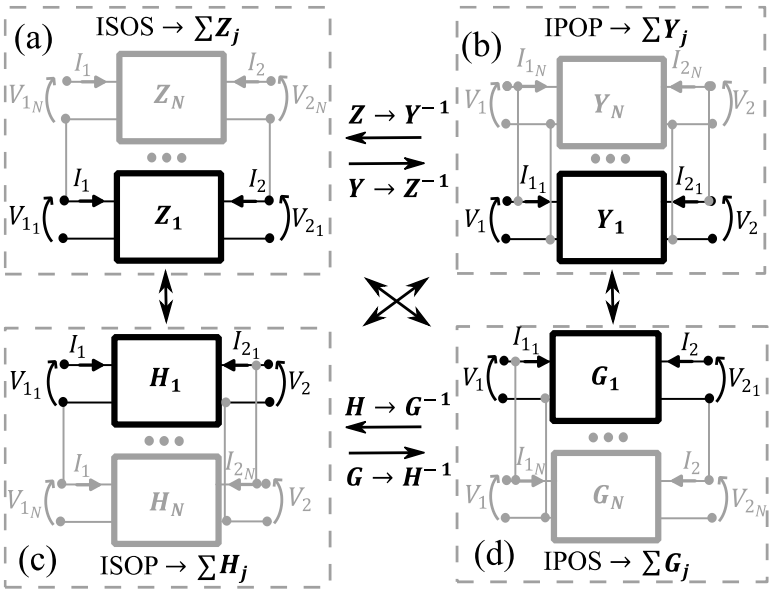


Figure 7.19 Utilisation des propriétés des réseaux à deux ports et des transformations pour les convertisseurs modulaires : (a) représentation ***Z***- pour ISOS ; (b) représentation ***Y***- pour IPOP ; (c) représentation ***H***- pour ISOP et (d) représentation ***G***- pour IPOS.

L'impact de la dispersion des composants est analysée de manière analytique et généralisée pour n'importe quel convertisseur de puissance basé sur la théorie des quadripôles. Dans une première partie, les cas sans perte sont traités et les conditions et règles pour la réalisation de la connexion sont données en observant simplement les caractéristiques externes des convertisseurs de puissance.

Étant donné que les convertisseurs DAB sans perte idéaux ne peuvent pas être connectés en ISOP et IPOS, le modèle résistif dérivé dans le *Chapitre 1* est maintenant utilisé et les paramètres de la matrice d'impédance sont extraits théoriquement. Dans l'ensemble, la méthode proposée offre une approche systématique et facile à utiliser pour analyser les déséquilibres dans les convertisseurs de puissance de manière générale, ce qui peut être utilisé pour améliorer la compréhension des systèmes électroniques de puissance et améliorer l'efficacité et la tolérance aux pannes de ces systèmes. Enfin, des résultats expérimentaux sont fournis pour les configurations ISOP et IPOS ce qui nous permet de conclure sur l'impact des déséquilibres sur la structure ISOP et IPOS, et de valider le modèle analytique

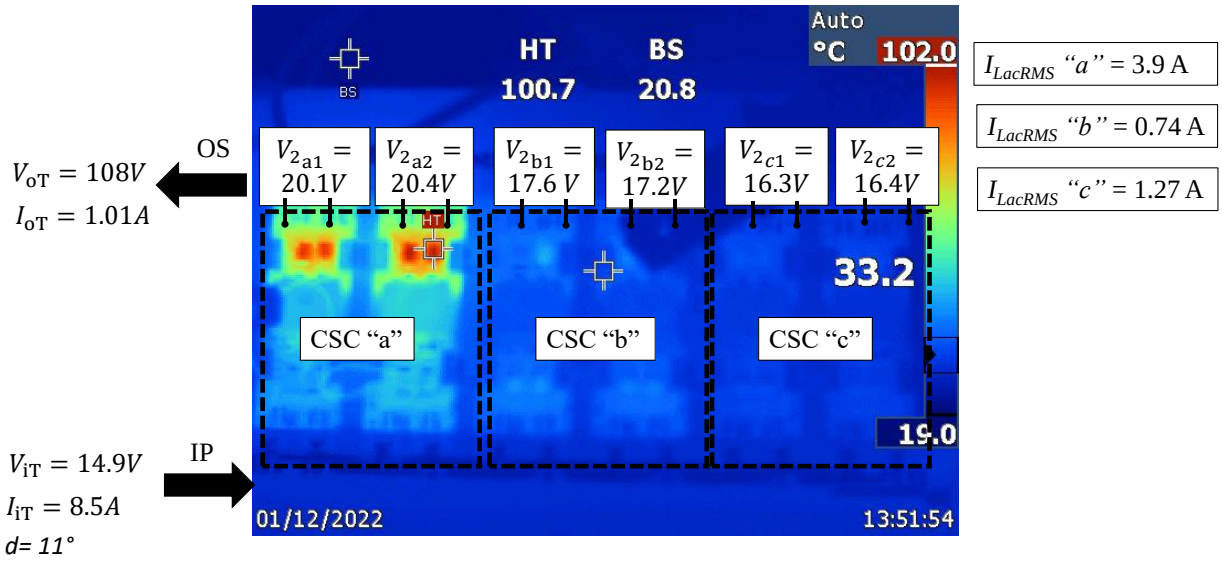


Figure 7.20 *Les résultats expérimentaux des tensions en courant continu à travers le PCA (IPOS) V_i = 15 V; V_o = 108 V; I_o = 1.0 A. Une image thermographique est représentée.*

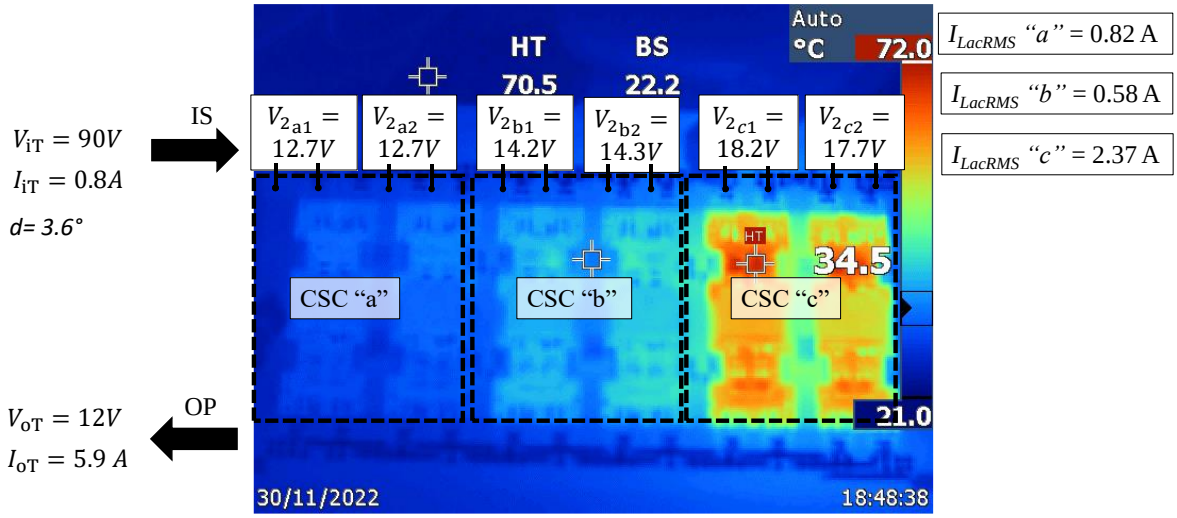
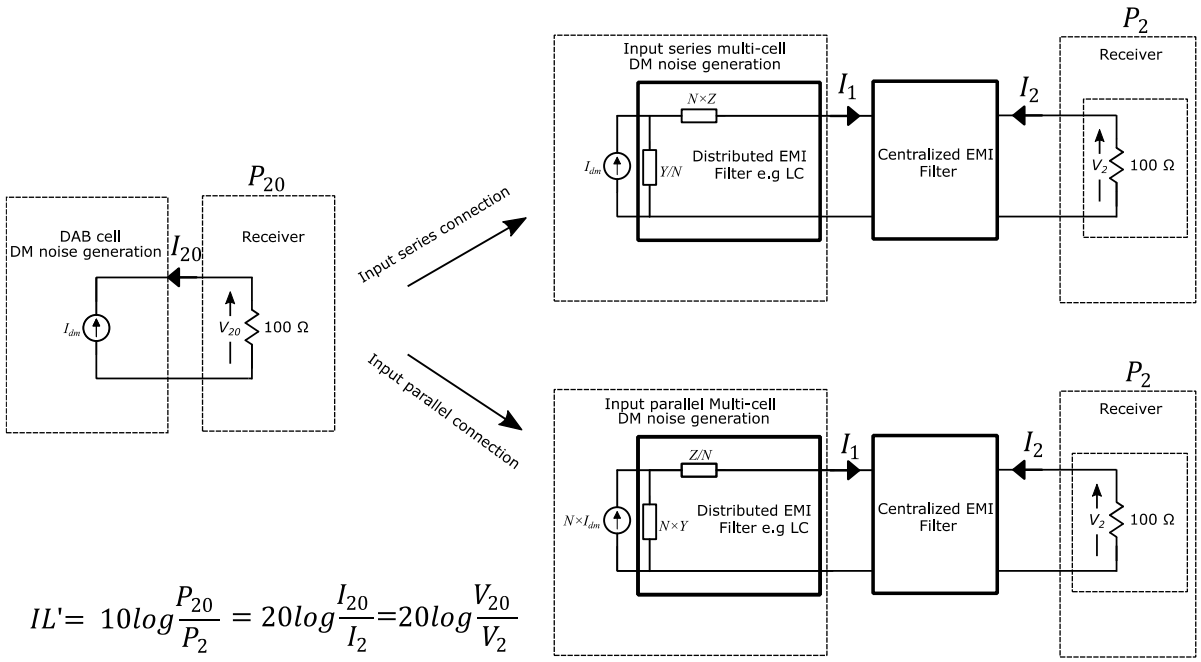


Figure 7.21 *Les résultats expérimentaux des tensions en courant continu à travers le PCA (ISOP) V_i = 90 V; V_o = 12 V; I_o = 6 A Une image thermographique est représentée.*

Les résultats ont montré que lorsque le courant de sortie diminue, le déséquilibre des tensions diminue également, et les courants efficaces (RMS) dans le AC-link sont mieux répartis, ce qui entraîne une réduction de la température maximale du PCA. Lorsque la tension de sortie est réduite ou augmentée par rapport à la tension de sortie nominale pour un gain unitaire (modes abaisseur et élévateur), le stress et le déséquilibre augmentent considérablement. Des comportements et des propriétés doubles sont observés à la fois dans les résultats expérimentaux et analytiques, ce qui s'est avéré être une représentation précise et descriptive en termes de précision, et plus conservatrice en termes d'erreurs. Des résultats expérimentaux pour ISOS et IPOP sont encore nécessaires.

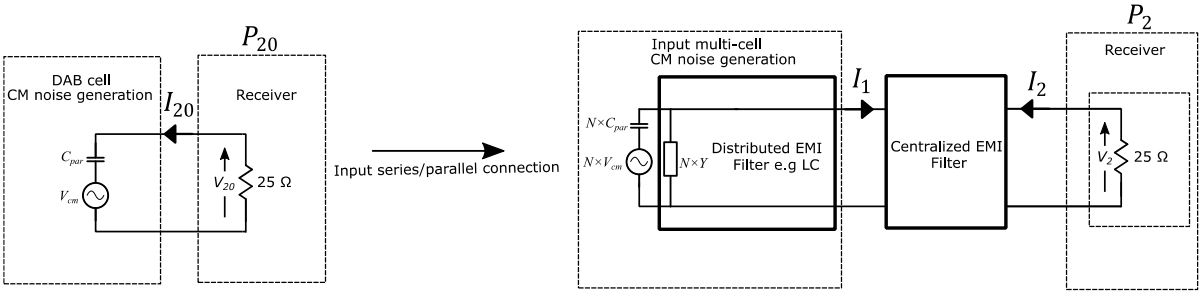
7.6 Chapitre 5 : Modélisation et amélioration des émissions conduites dans un réseau de convertisseurs

L'analyse et les tendances de la génération de bruit CM (mode commun) et DM (mode différentiel), déjà discutées dans les *Chapitres 1*, *2* et *3*, ainsi que la définition de la perte d'insertion présentée dans le *Chapitre 1*, sont transposées et adaptées aux convertisseurs multi-cellules (ou réseaux de convertisseurs). Les équations conventionnelles de pertes d'insertion, déjà expliquées dans la littérature, sont adaptées pour les réseaux de convertisseurs et les conclusions sur les tendances de la signature EMI DM en fonction de la configuration de connexion (série d'entrée vs parallèle d'entrée) ainsi que centralisée vs distribuée, sont révisées grâce à une comparaison de conception d'équivalence énergétique.



$$IL' = 10log\frac{P_{20}}{P_2} = 20log\frac{I_{20}}{I_2} = 20log\frac{V_{20}}{V_2}$$

Figure 7.22.. Définition adaptée de la perte d'insertion (IL') pour le bruit en mode différentiel (DM) pour les configurations de connexion IP et IS.



$$IL' = 10log\frac{P_{20}}{P_2} = 20log\frac{I_{20}}{I_2} = 20log\frac{V_{20}}{V_2}$$

Figure 7.23.. Définition adaptée de la perte d'insertion (IL') pour le bruit en mode commun (CM) pour les configurations de connexion IP et IS.

En ce qui concerne le bruit CM, il a été présenté dans le *Chapitre 1* à quel point il peut être difficile à atténuer. Dans ce *Chapitre 5*, on montre comment ce défi est intensifié avec l'augmentation du nombre de cellules, car le bruit CM est traité à l'aide de méthodes conventionnelles de conception de filtres. Grâce à une hypothèse simplificatrice, il est prouvé que le bruit CM est éliminé de manière active grâce à une technique de commande à décalage de 180°, présentée dans *Figure 7.24* , réalisée physiquement et bénéficiant de la structure de réseau de convertisseurs, étant principalement indépendante de la configuration de connexion. La technique transforme ce qui est considéré comme un problème, "l'interférence intra-

cellules", en une solution simple, sans coût et sans mise à la terre pour la réduction du bruit CM. Associée à la symétrisation de tous les aspects d'une cellule DAB, c'est un résultat exceptionnel capable de satisfaire aux normes de compatibilité électromagnétique (CEM) les plus compliquées, comme démontrée dans *Figure 7.25*. De plus, le bruit CM généré par les ponts en H est même amélioré avec l'augmentation du nombre de CSC en raison du comportement attendu d'une courbe gaussienne statistique. Cependant, il est important de distinguer le bruit CM généré par les MOSFET et celui généré par les pilotes de grille (Gate-drivers).

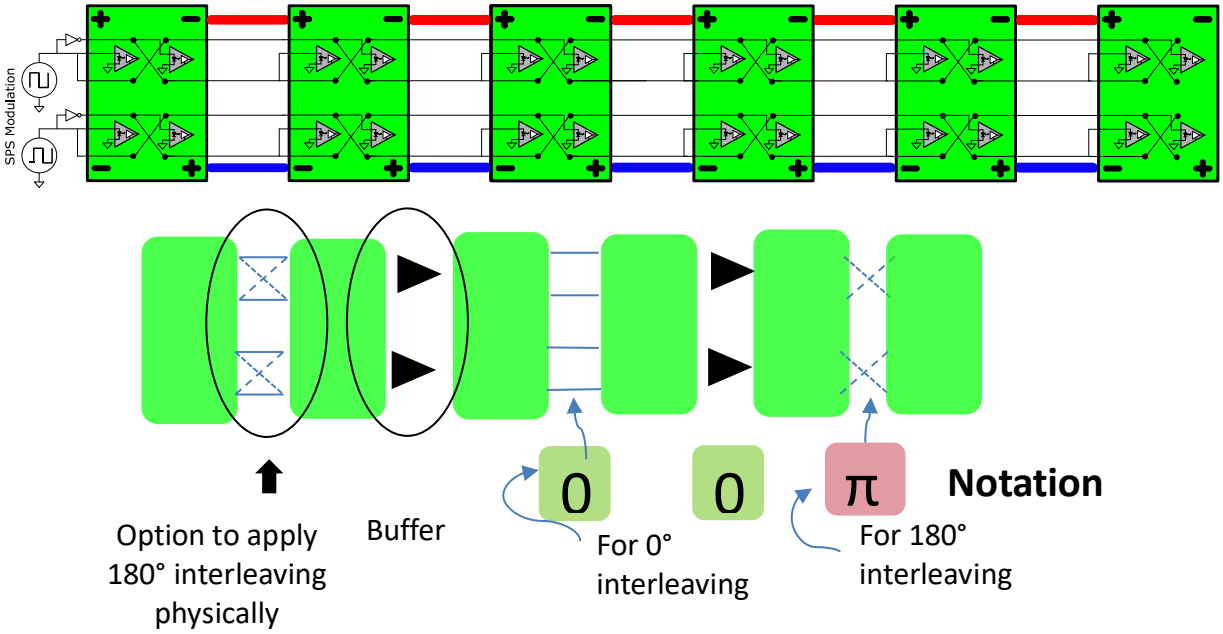


Figure 7.24. *S*olution proposée sans filtre à bruit CM quasi nul.

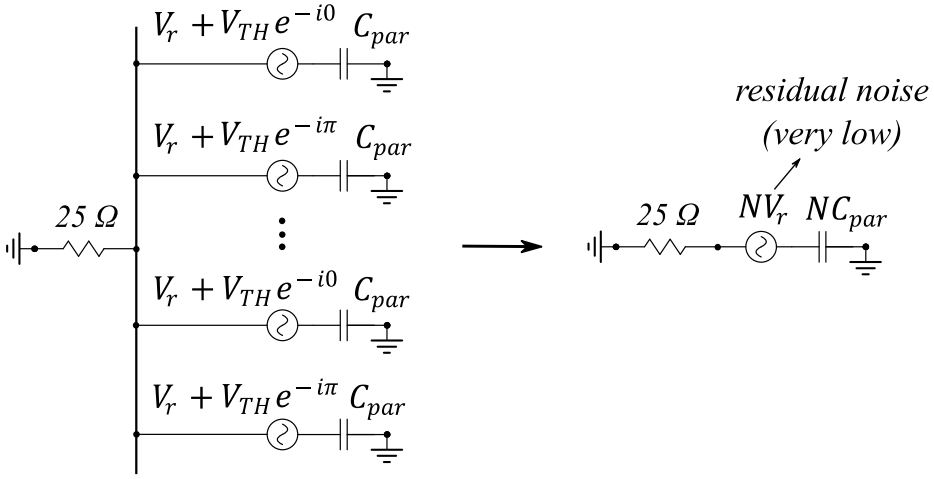


Figure 7.25. *Circuit équivalent de la s*olution proposée sans filtre à bruit CM quasi nul.

Enfin, des résultats expérimentaux sont fournis pour valider la méthode proposée de réduction d'environ 30 dB du bruit CM.

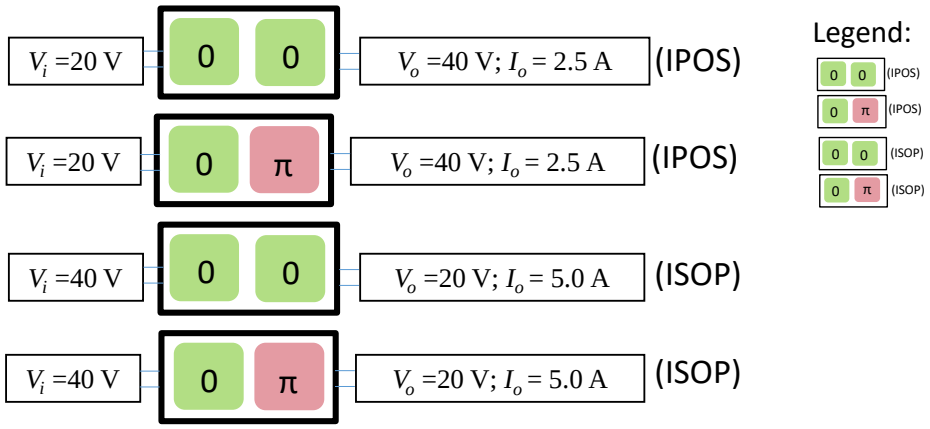


Figure 7.26. Schéma des résultats expérimentaux de la configuration IPOS et ISOP pour la démonstration du concept (deux CSCs) en appliquant un entrelacement de 0° et 180°. Une légende est présentée pour identifier les résultats expérimentaux dans la prochaine figure.

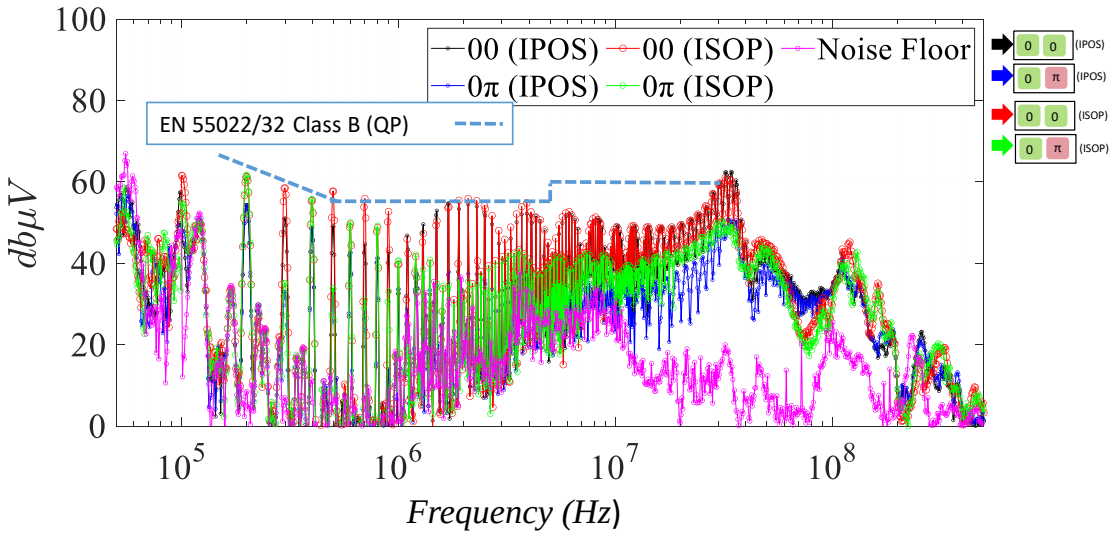


Figure 7.27. Schéma des résultats expérimentaux de la configuration IPOS et ISOP pour la démonstration du concept (deux CSCs) en appliquant un entrelacement de 0° et 180°. Une légende est présentée pour identifier les résultats expérimentaux dans la prochaine figure.

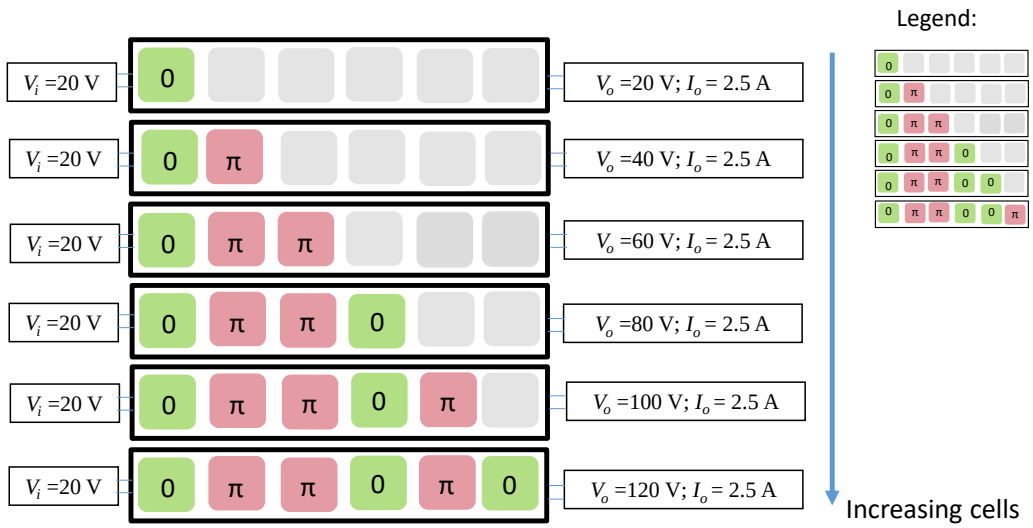


Figure 7.28. Schéma des résultats expérimentaux d'une configuration IPOS en augmentant le nombre de CSCs et en appliquant l'entrelacement proposé de 180° et 0° pour la réduction grâce à la compensation en mode commun (CM). Une légende est présentée pour identifier les résultats expérimentaux dans la figure suivante

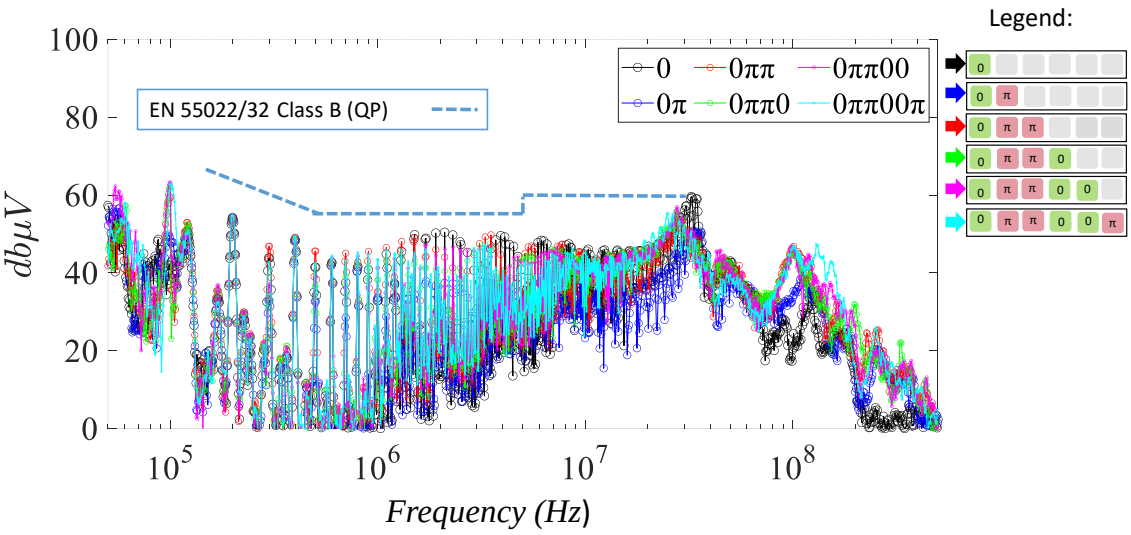


Figure 7.29. Spectre EMI du PCA (Version 3) de la configuration de connexion IPOS en appliquant l'entrelacement proposé de 180° et 0° pour la réduction grâce à la compensation en mode commun (CM), tout en augmentant le nombre de CSC jusqu'à six

7.7 Chapitre 6 : Prédiction, optimisation et perspective des émissions rayonnées d'un PCA pour la conception automatisée

Actuellement, il n'y a pas de normes de conformité en matière de CEM pour la cartographie du champ proche. Cependant, cette cartographie est essentielle pour localiser les

modules de commutation ainsi que les périphériques d'une alimentation à proximité de son champ proche. Ces périphériques comprennent les cartes de commande, les dispositifs de conditionnement de signal, les capteurs et les filtres passifs qui peuvent causer des dysfonctionnements et une dégradation des performances des signaux analogiques en raison de couplages indésirables. Pour les convertisseurs multicellulaires, il est crucial de déterminer si les interactions entre plusieurs sources de bruit peuvent causer des dysfonctionnements dus à des interférences croisées. D'un autre côté, cette situation présente une occasion de développer des approches théoriques et expérimentales pour étudier et optimiser les systèmes en amont et indépendamment de la fabrication de prototypes. Cela peut être fait en utilisant des concepts, des règles et une méthodologie systématique, ainsi que des plateformes expérimentales. De cette façon, la signature CEM peut être prévisible et améliorée grâce à des concepts simples et des plateformes d'évaluation comme présenté dans *Figure 7.30*.

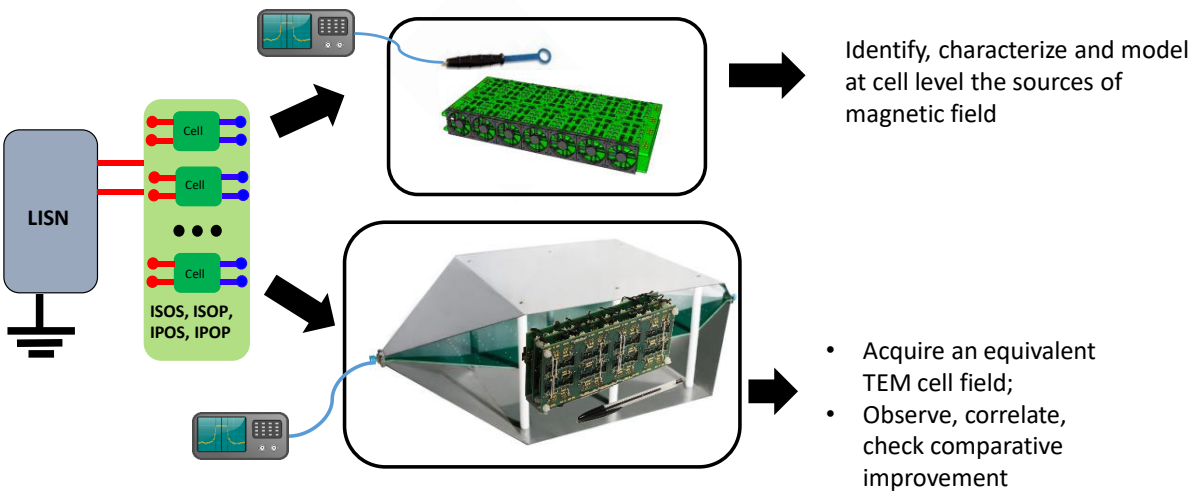


Figure 7.30 Configuration proposée pour l'acquisition de la signature EMI en champ proche.

En améliorant la configuration géométrique et électrique des modules de commutation et de leurs interconnexions, il est possible d'améliorer à la fois le champ proche et le champ lointain rayonné, transformant ainsi ce qui est considéré comme un "problème" dans la littérature actuelle en une caractéristique avantageuse. Cette caractéristique est unique à l'approche réseaux de convertisseur et est encore inexplorée dans la littérature, bien que le bruit CM ait été traité de manière active en utilisent l'interaction entre les cellules.

L'une des principales préoccupations concernant les convertisseurs multicellulaires concerne les interconnexions. L'impact sur la configuration de conception des filtres et des interconnexions devrait donc être évalué dans leur ensemble, comme illustré dans le schéma présenté à la *Figure 7.31*. Les différentes combinaisons possibles pour fermer les boucles

d'interconnexion du PCA, et donc les différentes combinaisons géométriques de boucles, peuvent directement influencer le champ proche résultant.

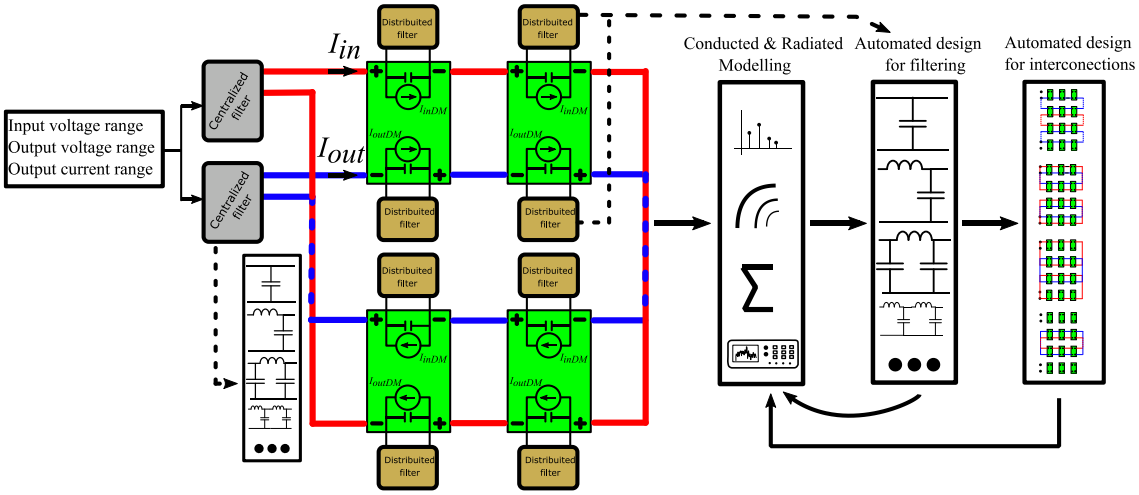
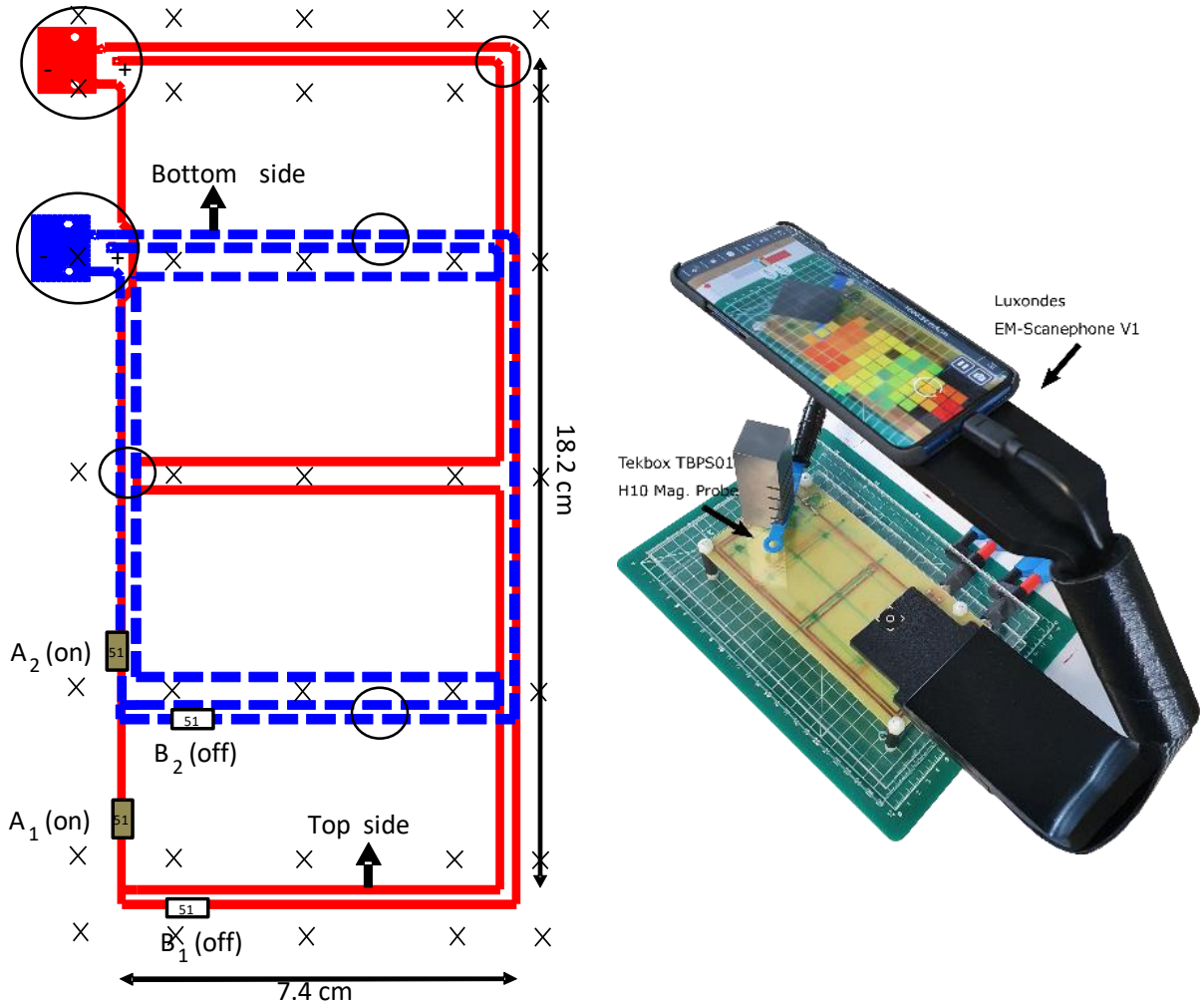


Figure 7.31 Exemple d'un concept de conception automatisée pour la conformité EMI basé sur une approche PCA (« Power Converter Array ») (par exemple, PCA_{2x2} ISOS) : le filtrage et le routage sont optimisés en fonction de la conformité CEM basée sur une caractérisation expérimentale et théorique.

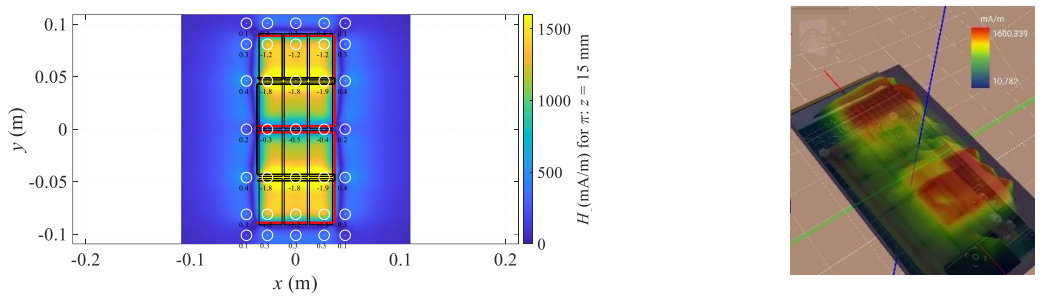
Il est possible de détacher les interconnexions du convertisseur en fonctionnement et de l'exciter avec un générateur de signal pour calculer et acquérir le champ proche. Pour ce faire, une configuration qui imite les interconnexions et quatre configurations possibles ont été prototypées et mesurées avec un EM Scanephone et des sondes de champ proche, comme présenté dans la *Figure 6.17*. Les résultats des mesures réalisées à l'aide d'un EM Scanephone sont présentés dans la *Figure 6.19*, ce qui s'est avéré être de bonne qualité lorsqu'on les compare aux résultats analytiques, qui ont également été dérivés dans cette thèse.

Il est également possible de conclure sur l'impact des interconnexions, et celui-ci n'est pas négligeable!

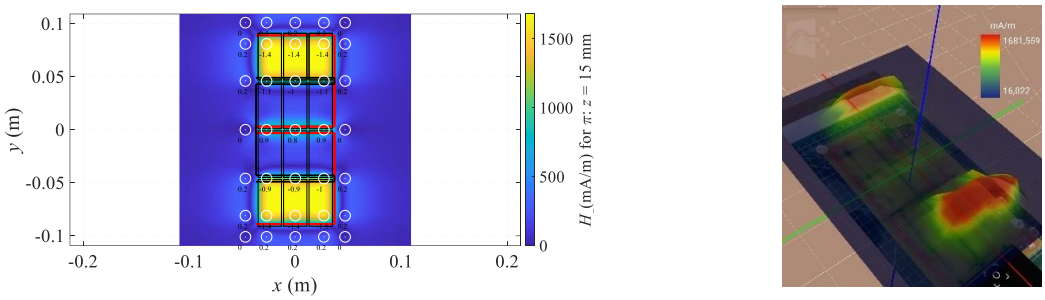


(a) *(b)*

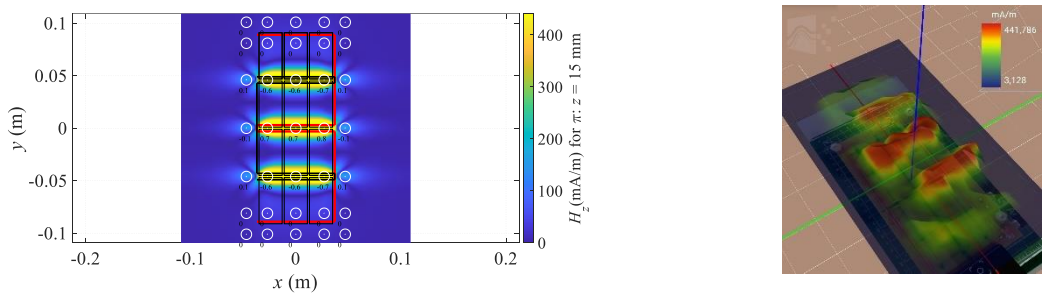
Figure 7.32 Configuration expérimentale pour imiter les boucles d'interconnexion d'un PCA $_{4x3}$: (a) schéma détaillé avec des cercles indiquant les adaptations physiques nécessaires pour surmonter les hypothèses théoriques irréalistes mentionnées précédemment, des croix (X) indiquant les points fixés mesurés par une sonde de champ proche et des résistances de 50 ohms pour permettre les quatre combinaisons de boucles (A_1A_2 en tant qu'exemple illustratif) ; (b) Configuration de l'équipement de test pour la cartographie en champ proche utilisant une feuille en plexiglas située à 10 mm au-dessus du PCB, une sonde de champ proche H10 EMC de Tekbox et un Scanephone EM (version bêta) de Luxondes



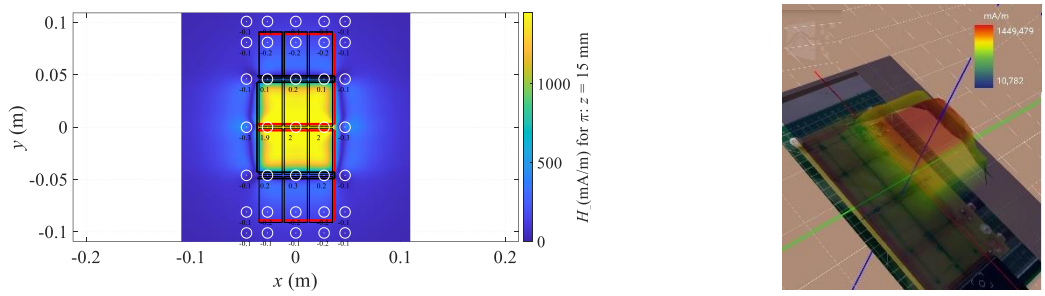
(a)



(b)



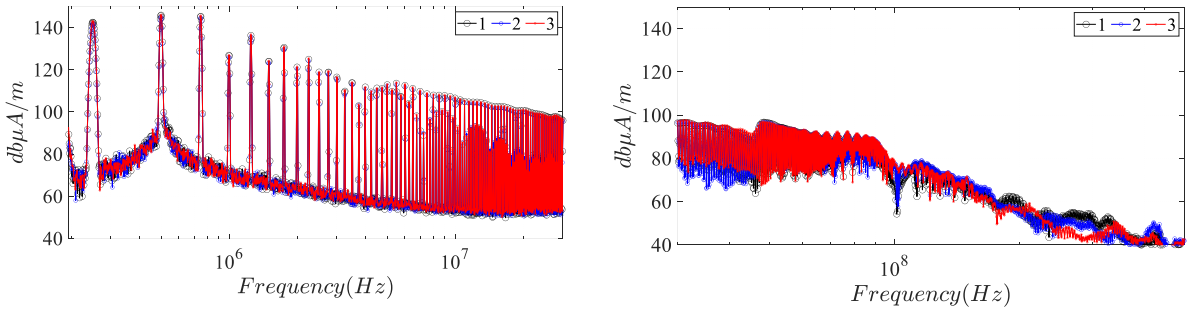
(c)



(d)

Figure 7.33 Tracé des résultats de la composante z produits par les quatre combinaisons de boucles d'un PCA 4x3 sur le plan π : z = 15 mm : (a) A1A2 ; (b) A1B2 ; (c) B1A2 ; (d) B1B2. Résultats théoriques à gauche et résultats pratiques à droite à travers le Scanephone. À gauche, les trajets d'envoi du courant d'entrée (segments rouges) et de sortie (segments noirs), ainsi que les CSCs (rectangles noirs), sont présentés pour la visualisation. Les cercles à gauche (résultats théoriques) sont conservés pour fournir des informations supplémentaires et faciliter la compréhension.

Enfin, avec le convertisseur de puissance en fonctionnement, il a été possible d'acquérir la signature EMI en utilisant la sonde de champ proche, comme présenté dans la *Figure 6.21* , et avec la cellule TEM, comme présenté dans la *Figure 6.42*. Une corrélation importante avec les paramètres électriques, tels que la résonance, le ZVS (zero voltage switching) et les émissions conduites, a été abordée.



(a) *(b)*

Figure 7.34 Mesures expérimentales à l'aide de la sonde de champ proche : (a) pour la plage de fréquences CE de 150 kHz à 30 MHz ; (b) pour la plage de fréquences RE de 30 MHz à 500 MHz.

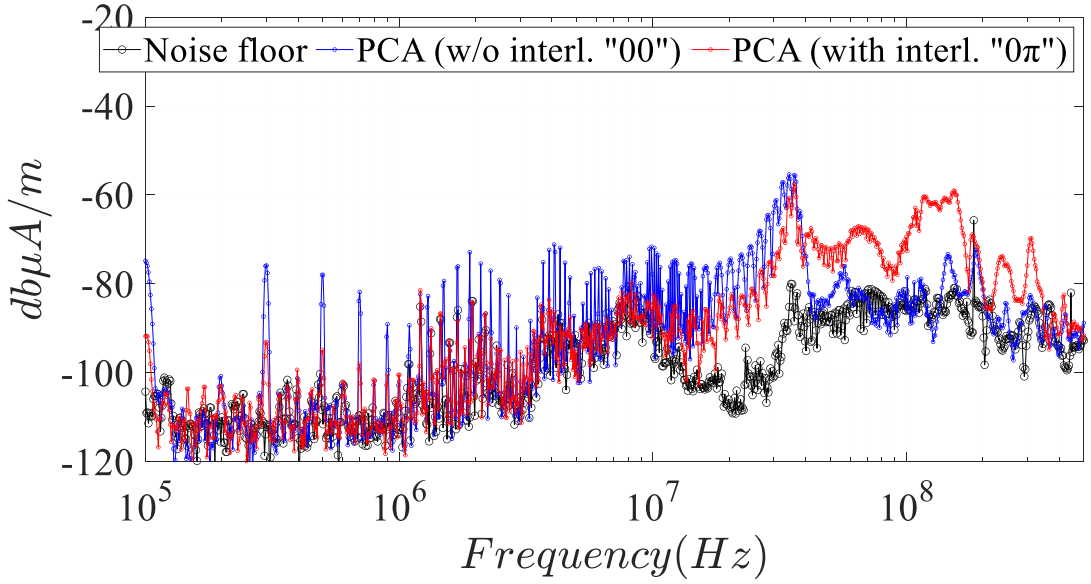


Figure 7.35 Résultats de la signature EMI de la cellule TEM pour un PCA1x2 IPOS (Version 3.1) positionné parallèlement au plan π (chaque CSC était réglé pour fournir une tension d'entrée nominale V_i = 20 V, un courant de sortie nominal I_o de 2,5 A et un gain statique unitaire M = 1,0), en désactivant l'entrelacement "00" (en bleu) et en activant l'entrelacement "0π" (en rouge).

7.8 Conclusions finales et perspectives

Au cours de la première phase du travail, l'effort a été concentré sur la conception d'une CSC (DAB avec un modulation SPS), en prenant en compte non seulement l'efficacité et la densité de puissance, mais aussi la façon dont le point de fonctionnement et les choix de paramètres électriques peuvent affecter les courants parasites de DM et CM. En effet, le gain statique, le courant de sortie et la région ZVS sont des paramètres qui peuvent avoir un impact direct sur le bruit de courant circulant. L'analyse mathématique a été effectuée de manière normalisée et sans dimension chaque fois que cela était possible. Cela peut faciliter la conception à travers des abaques et une optimisation en limitant l'espace de conception. L'objectif principal était de concevoir un DAB qui puisse effectuer une commutation à ZVS (Zero Voltage Switching) à pleine puissance et sans refroidissement forcé. Pour simplifier l'analyse du modèle de bruit CM, de nouveaux circuits équivalents et des hypothèses simplificatrices sont proposés et discutés théoriquement en les comparant à d'autres modèles, y compris des simulations et des références. La symétrisation d'un DAB par rapport à la liaison AC-link s'est avérée extrêmement impactante sur la génération de bruit CM. Bien que cette approche puisse occuper plus de volume et être moins efficace, l'adoption pour la prévisibilité, la simplicité, la normalisation et la réduction du bruit CM est observée. En ce qui concerne l'observation d'interactions entre CSC d'un convertisseur multicellulaire fonctionnant avec un rapport cyclique commun, il manque une théorie fondamentale et unifiée dans la littérature. Il est donc proposé une théorie basée sur la théorie des réseaux à deux ports qui tente d'unifier et de définir systématiquement les règles de réalisation des connexions, de définir des propriétés telles que l'invariance de la puissance par rapport à la configuration de la connexion et enfin de trouver facilement des solutions fermées de partage de tension, de courant et de puissance. En ce qui concerne le bruit CM (mode commun), une hypothèse de simplification consistant à court-circuiter les ports d'entrée et de sortie de tous les CSC (cellules de commutation) a permis d'affirmer que le courant CM est plus ou moins indépendant de la configuration de la connexion. De plus, cela permet de parvenir à des idées basées sur le décalage uniforme de 180° des CSC, qui a été fondamental pour le résultat exceptionnel en matière d'atténuation du bruit CM.

Les études futures incluent l'étude et la mise en œuvre de modulations de commande plus sophistiquées qui peuvent améliorer l'efficacité et la densité de puissance, tout en observant la conformité aux normes CEM. L'idée est donc de rendre le PCA, les CSC et les platesformes de configuration non pas seulement en terme de densité de puissance et prix, mais également hautement configurables (par exemple, signal de rapport cyclique

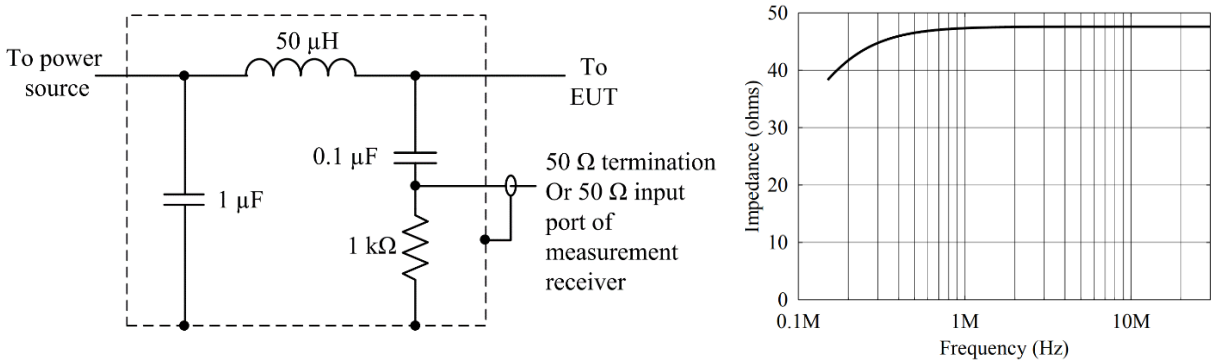
indépendant, différentes modulations de commande, redondance et protection contre les pannes) et faciles à manipuler (par exemple, accès aux points électriques importants). En ce qui concerne la théorie basée sur les réseaux à deux ports proposée, il est possible de poursuivre les investigations et d'utiliser un tel outil pour la conception de convertisseurs multicellulaires. De plus, il est possible de combiner et coupler les modèles de bruit CM avec cette théorie.

Des résultats expérimentaux sont encore nécessaires pour vérifier l'impact sur les aspects CEM de solutions de filtres distribués et centralisés sur toute la plage de fréquences. De plus, la vérification et la corrélation entre la sonde de champ proche et la cellule TEM ainsi que la condition OC doivent être effectuées dans des laboratoires d'essais certifiés. Enfin, une comparaison théorique et expérimentale entre l'approche PCA et l'approche de convertisseur de puissance conventionnel en termes de taille, de volume et de temps nécessaire pour passer les normes CEM peut clarifier les avantages et les inconvénients de chacune.

Appendix 1.A EMC Equipement and setup

LISN

The LISN, which stands for Linear Impedance Stabilization Network, is one of the most important equipment in EMC testing. There are two main goals: (i) provide fixed and known impedance regardless of any input or output connection; (ii) filter input noise (DC voltage supply or grid). These two combinations allow repeatability and accuracy. Different LISNs are available on the market due to different EMC standards and directives. A common LISN used to exemplify is the single-phase LISN provided by CISPR 11, as it is presented in Figure 0.1. The EMI receiver is terminated in 50 ohms.



(a) *(b)*

Figure 0.1 (a) CISPR 11 standard LISN electric schematic; (b) CISPR 11 standard impedance [23].

The separation between common mode (CM) from differential mode (DM) noises (see definition in Subsection 1.1.3) are not required by the standards, but are usually desirable for the sake of source disturbance nature identification, and to later attenuate it with many different methods. In practice the The LISN can be classified into three:

- **V-network**: line-to-ground measurement is performed, and unsymmetrical emissions are measured;
- **T-Network**: mid-point line-to-line measurement is performed, and asymmetrical emissions (CM) are measured, defined by “half of the vector sum” of the terminal voltages with respect to earth;

- **Δ-network**: line-to-line measurement is performed and allows symmetric (DM) defined by "vector difference" between two phases and the asymmetrical emissions as previously mentioned.

The LISN at G2Elab is capable of providing all four emission measurements: unsymmetrical emission of phase A, phase B, symmetrical (DM) and asymmetrical (CM). It is important to notice that all EMC equipment should pass through calibration and verification [30], which is not often the case for the testing equipment in this thesis, increasing the uncertainty even further. Besides, for all measurements, CM and DM rejection should also be guaranteed and verified [22].

Spectrum Analyzer / EMI test receiver

The Spectrum Analyzer is usually represented by a termination of 50 ohms and a FFT is applied on the measured signal. On the other hand, a much more complex system including detection and filter, as presented in Figure 0.2, should be considered for interpreting the results and setting the configurations according to EMC standard specifications or simply describing and interpreting correctly the EMI signature.

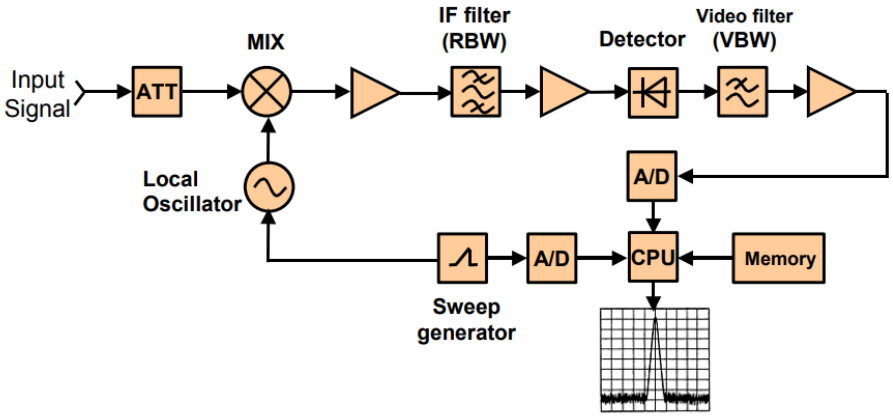


Figure 0.2 Block Diagram of the Super-Heterodyne Method [24].

According to [25], some main settings parameters are found on most spectrum analyser:

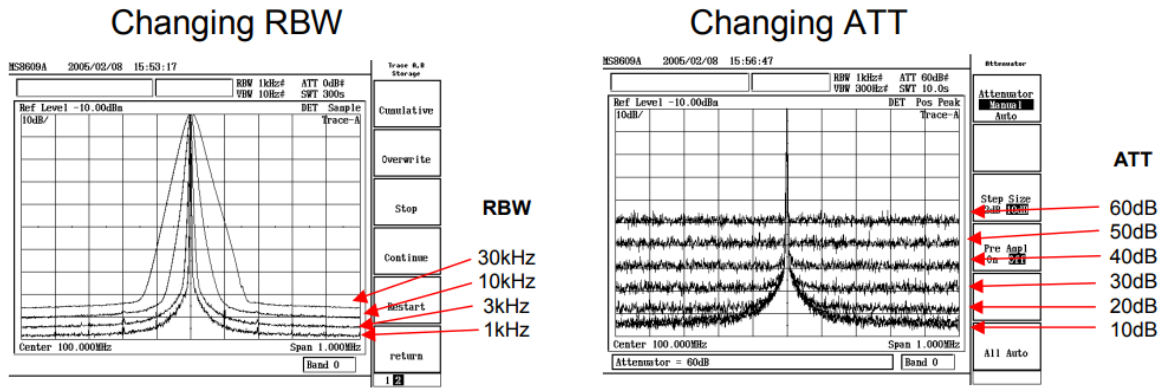
- **Frequency display range**: set by start and stop frequency. It can also be set by choosing a central frequency and the span;

- **Level display range**: its range is set with the aid of the maximum level to be displayed (the reference level). In the spectrum analyser used for the tests, an attenuation up to 30 dBm also is automatically set depending on the reference level;
- **RBW (Resolution Bandwidth):** used to observe two distinct but closely spaced in the spectrum frequency; The RBW is, according to EMC standard CISPR 16-1-1, set at (i) 9 kHz for the CE range frequency (150 kHz up to 30 MHz); (ii) 200 Hz (for 9 kHz to 150 kHz) and (iii) 120 kHz (from 30 MHz to 2 GHz).
- **VBW (Video Bandwidth):** it helps to digitally remove the noise of a signal and facilitate visualization of the worrying harmonic. A too low VBW can make the signal of interest disappear. Therefore, a rule of thumb is to set VBW three times larger the RBW.
- **Sweep time:** only for analyser working with heterodyne principle, it is the time required for covering the spectrum of frequency of interest. Lower RBW require larger sweep time. An automatic sweep time can be set through the spectrum analyser. On the other hand, a proper sweep time should be set according to [24]. Upon failure to attain minimum sweep time, amplitude loss and frequency offset can be falsely displayed.

$$Sweep\ time\ = k\ \times \frac{Frequency\ span}{RBW\ \times VBW}\ ,\ k = 3. \tag{0.1}$$

Other important feature to guarantee safe and trustworthy results should be taken into consideration (here used as example Spectrum Analyzer R&S FSH3):

- **Maximum range**: for the Spectrum Analyzer, R&S FSH3, the maximum acceptable disturbance noise is 20 dBm, which converting into dbuV in a 50 ohms system results in 123 dbuV. Obs: a pulse limiter (R&S®ESH3-Z2 Pulse limiter) is installed in the input of the spectrum analyser, providing a 10 dB insertion loss;
- **Dynamic range**: is the range that can be measured without important errors due to noise level, residual response and distortion. Some tips to guarantee a better dynamic range, by decreasing the average noise level is: decreasing the RBW and the attenuation. For the equipment setup at CITCEA, a 10 dB insertion loss + 0, 10, 20 or 30 dBm can be expected depending on the reference level. As presented in Figure 0.3 decreasing RBW and Attenuation, improves the quality of the signal. According to the CISPR 22 [26] , the noise level should be at least 6 dB bellow the source disturbance



(a) *(b)*

Figure 0.3 (a) Changing the RBW from 1 kHz to 10 kHz increases the average noise level in 10 dB; (b) the average noise increases by 10 dB if attenuation value is changed by 10 bB [24].

- **Residual response and distortion:** when high input signal occurs nearby the maximum allowed or the reference level, the signals can be distorted, as presented in Figure 0.4. For that reason, very large input signals can distort the signal, and an attenuation is needed. Therefore, there exists a compromise between needed attenuation for safety and avoiding distortion versus the average noise that it might cause, as previously mentioned.

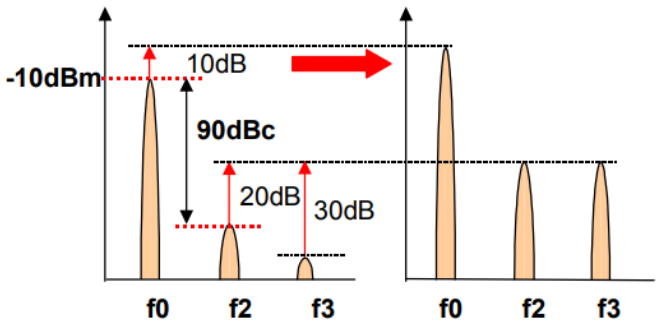
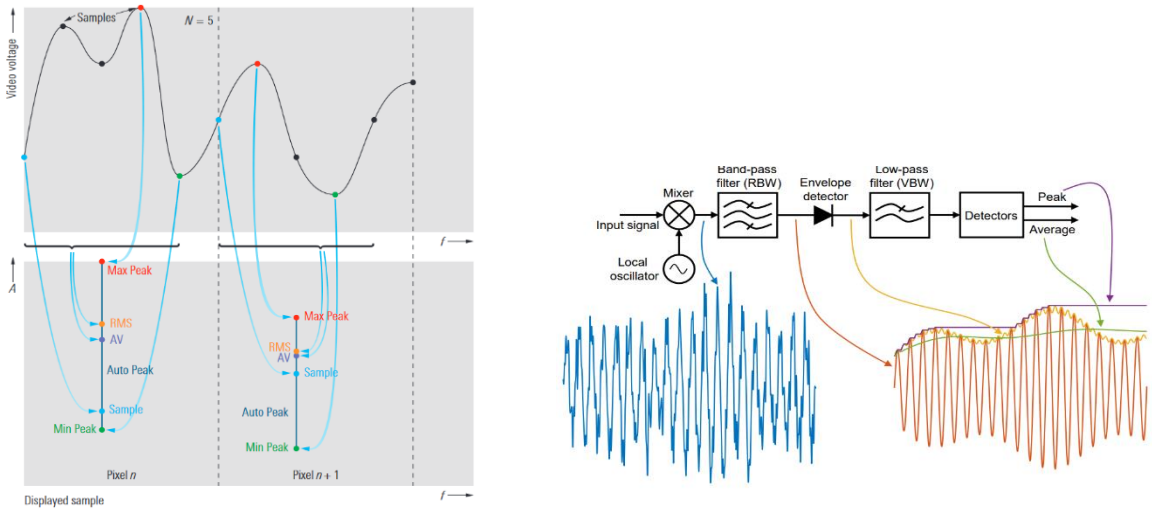


Figure 0.4 When a basic waveform is enlarged by 10dB, the 2nd harmonic distortion grows by 20dB and the 3rd harmonic distortion grows by 30dB [24].

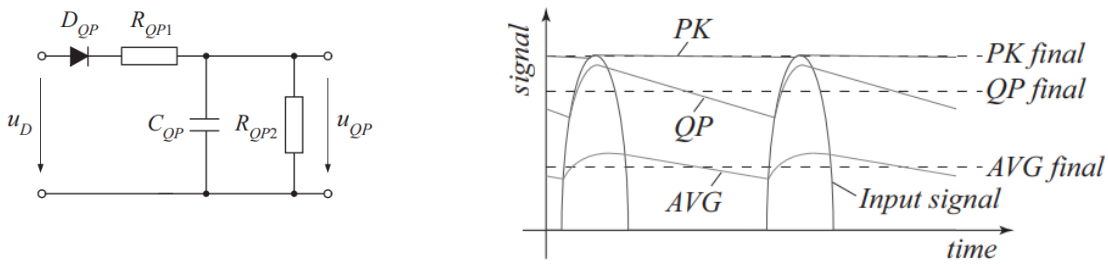
Finally, a brief explanation on the type of detector is given. Different types of detection are given in an EMI receiver [25], as presented in Figure 0.5, the displayed result may be very different depending on the applied detection.



(a) *(b)*

Figure 0.5 (a) Different types of detection [25]; (b) Illustration of the super heterodyne measurement principle [27].

- **Max peak detector** is particular useful for EMC as even if spans are displayed with very narrow RBW, the input signal information is not lost;
- **Min peak detector** is the minimum value measured;
- **Auto peak detector** provides both maximum and minimum peak;
- **Sample detector** only one value from the samples allocated to a pixel. If the span is much greater than the RBW, this detection may display incorrect level or completely lost;
- **RMS detector** calculates the power from the samples allocated in the pixel window;
- **Quasi-peak detector** is often used in EMC compliance tests. The analogic circuit used to detect the quasi-peak is presented in *Figure 0.6 (a)*. The CISPR 16 address that the charge and discharge time should be equal to 1 ms and 160 ms, respectively.



(a) *(b)*

Figure 0.6 (a) Quasi-detector (QP) circuit mode; (b) Illustration of the behaviour of the different types of detection circuits [126].

The difference between Peak, Quasi-peak and average detection can be observed in Figure 0.6 (b). With different charging and discharging time constant, e.g. for Peak, very small charging time constant and large discharging time constant. Indeed, according to the normative of CISPR 22 [26], the Peak, Quasi-peak and Average should follow a decision tree, as presented in *Figure 0.7*, in order to reduce the testing time.

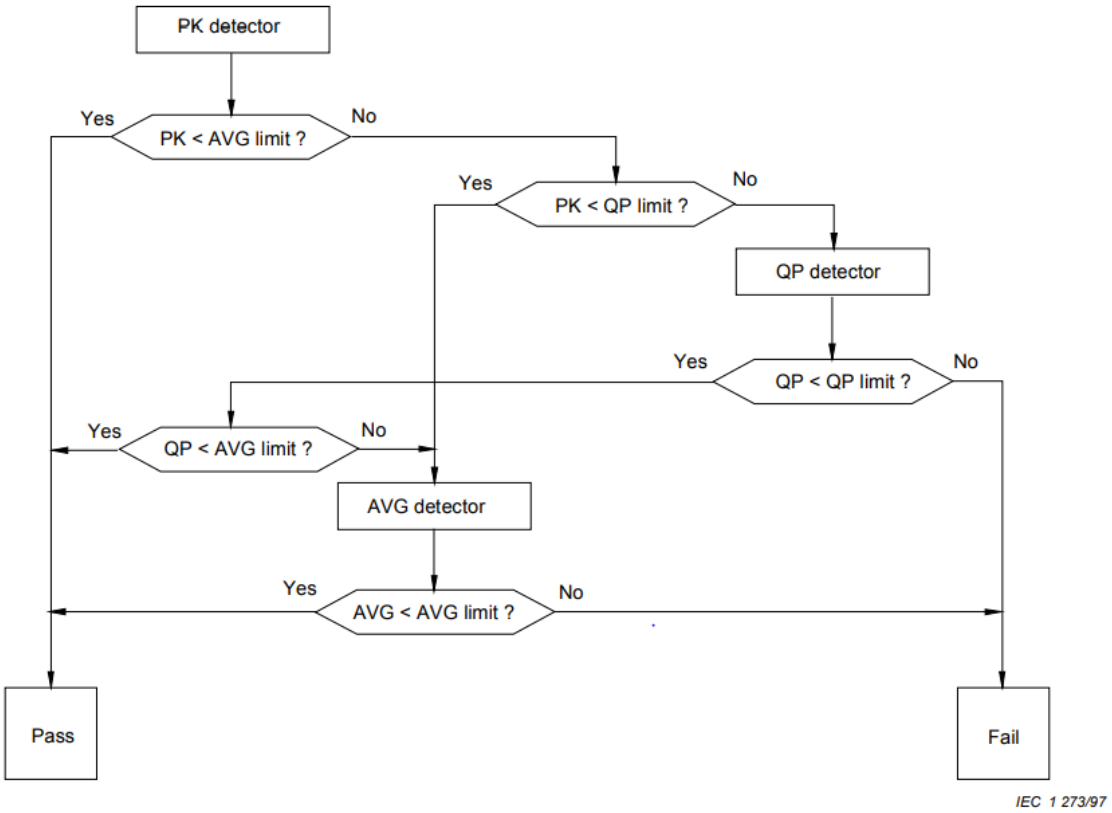


Figure 0.7 Decision tree for peak detector measurements according to the normative of CISPR 22 [26].

TEM Cell

TEM Cell stands for transverse electromagnetic cell are devices used for establishing standard electromagnetic (EM) fields in a shielded environment, usually for pre-compliance purpose. The TEM cell consists of three parallel rectangular conductive strips on top, bottom in the middle and a grounded wall. The geometry, presented in Figure 0.8 is designed to provide a 50Ω range line. The TEM cell also has limitations such as upper useful frequency, which is defined by its physical dimensions;

The use of TEM cells is, therefore, very diverse:

- **Emission testing** of small equipment, which is adequate for the converter in this work. In such case, it is terminated with a 50 ohms impedance, and a coaxial cable is connected to the EMI receiver. TEM cell measures near field radiated from the structure which is an image of conducted in some configurations. It is an effective and inexpensive way of characterizing EMI signature, correlate/identify electrical characteristics such as oscillation, resonance frequency and testing different configurations for optimization;
- **Calibration of RF probes:** TEM Cell can be connected to a wave generator, which due to well-known homogenous behaviour of the wave-travelling, can be used for calibration purposes.
- **Immunity testing:** through a RF synthesizer and power amplifier, the EUT can be placed in the middle to receive electromagnetic wave and verify any malfunction or runaway due to susceptibility.

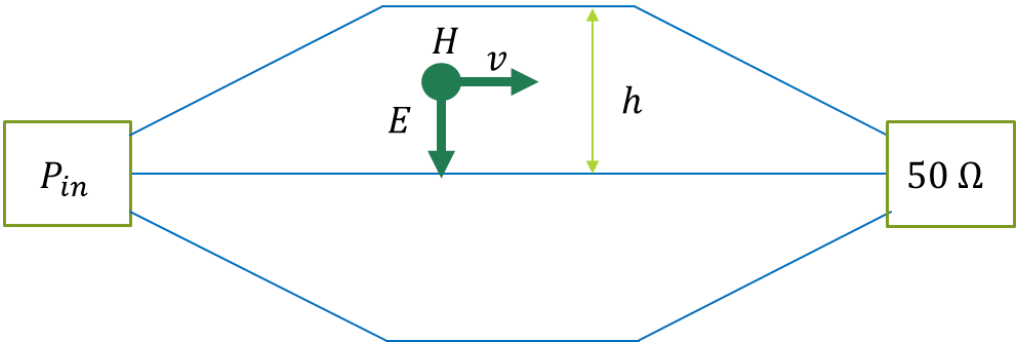


Figure 0.8 Sectional view of the TEM cell

The device under test (DUT) is placed between the inferior. As it is open, it may pick up the RF noise floor, but it can be accounted before the operation of DUT. Other variants operating with the same principle of TEM cell are used during pre-compliance testing, such as GTEM cell.

The near magnetic field cartography, currently, is not required on the EMC compliance standards. However, it is an effective way for locally debugging, diagnosing and characterizing spatially the sources of radiation produced by power converters and its correlation with the electrical parameters of the power converter itself, such as ZVS realization. Besides, due to the short distance, the other peripherals of a power converter nearby its near field sources, such as driver boards and their paths, sensors, signal conditioning devices and filters are susceptible of undesirable couplings, causing malfunctioning and performance degradation in analogue signals. Therefore, the prior

knowledge of the near field helps defining the good location and possible shield needing of the peripherals contained in a power converter.

The near field was measured with the H10 near field probe from Tekbox TBPS01 EMC set. This set consists of 4 probes which electromagnetic emission can be measured. This probe set makes it possible to locate potential electromagnetic interference sources within a circuit or device. In this way, it is possible to check whether the device to be tested complies with the EMC-guidelines. The probes work as antennas with large bandwidth (> 1 GHz) and can measure the emitted emission of, for example, components, PCB tracks or other parts of a system that can radiate RF. An alternative application of these probes is an immunity test by radiating an RF signal to a potentially sensitive part of a circuit.

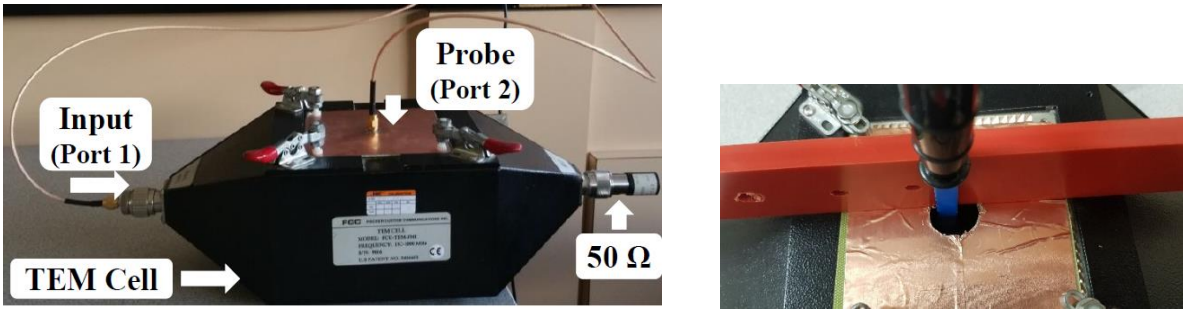


Figure 2 : Setup with cellule TEM (left) and Placing of the probe inside the TEM cell (right).

Before going to experimental results, the calibration process will allow to get the results from spectrum analyzer in dbµV and convert them into db µA/m. In other words, the calibration is simply given by the antenna factor, measured in practice or theoretically. The theoretical value of the antenna factor is simply given in Equation (1) is.

$$AF_{th} = \frac{1}{j \cdot \omega \cdot \mu \cdot S \cdot N} \quad \left[\frac{A}{m.V}\right] \tag{2}$$

Where:

AF_{th}: $facteur\ d'antenne\ théorique$ $\left[\frac{A}{m.V}\right]$

S : $Surface\ de\ la\ boucle$ $[m^2]$

N: $nombre\ de\ tours\ dans\ la\ boucle$

The first step is the calculation du champ à l'intérieur de la cellule TEM (FCC-TEM-JM (DC – 1000 MHz), given by (2) and (3).

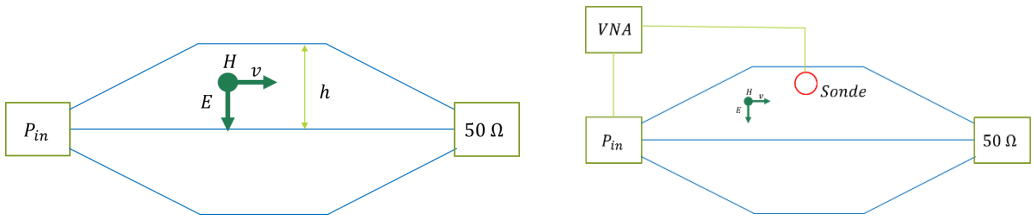


Figure 3 : Cross-sectional view of the TEM cell (left) and cross-sectional view of the TEM cell with the probe (right).

P_{in}: *Input power*

E_{th}: *Theoretical electric field*

H_{th}: Theoretical magnetic field: height between Septum conductor and outer conductor.

$Z_c = 50\ \Omega$

$\eta = 377\ \Omega$

$$E_{th} = \frac{\sqrt{P_{in}(W) * Z_c}}{h} \left[\frac{V}{m}\right] \quad (3)$$

$$H_{th} = \frac{E_{th}}{\eta} \left[\frac{A}{m}\right] \quad (4)$$

The second step is the calculation of the induced voltage (V_{ind}) across the probe, which can be performed through a spectrum analyzer, as in Equation (4) through measured power (P_{mes}) or a Vectorial Analyzer (VNA), through S_{21} parameter parameter measurement. In this work, the measurement were accomplished using a VNA ANRITS UMS46552B.

$$V_{ind} = \sqrt{2 \cdot P_{in} \cdot Z_c} \cdot |S_{21}| \cdot e^{j \cdot arg(S_{21})} \ \textit{(Using VNA)} \quad (5)$$

$$V_{ind} = \sqrt{P_{mes}(W) \cdot Z_c} \ \textit{(Using spectrum analyser).} \quad (6)$$

Finally, the third and final step consists on the calculation, in db preferably, of the antenna factor given by (6) for electric probes and (7) for magnetic probes.

$$AF = 20 \cdot Log\left(\frac{E_{th}}{V_{ind}}\right) \left[dB\ \frac{1}{m}\right] \ (electric\ probe) \quad (6)$$

$$AF = 20 \cdot Log\left(\frac{E_{th}}{V_{ind}}\right) \left[dB\ \frac{A}{m.V}\right] \ (magnetic\ probe) \quad (7)$$

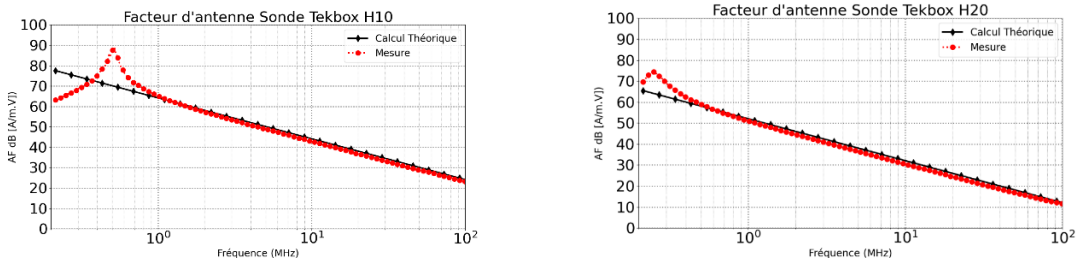


Figure 4 : Antenna factor for H10 probe (left) and H20 probe (right).

Appendix 4.A Two-port parameter extraction of Flyback based converters as a function of external variables

The goal of the Appendix is to provide the steps for finding the four two-port network matrix representation, presented in *Table 4-III*, as a function of external and known variables for the Flyback converter in DCM case, since all four connections are realizable. Such procedure can be applied to any power converter as long as the same assumptions and rules presented in this paper are predefined. From the definition of *Table 4-I* and the necessary condition of connection realization, that is, $M_j = M_{j-1} = V_o/V_i$ the Y_n-matrix is easily given by (4.A.1). The total input and output currents are then defined by the summation $\sum Y_j$, as presented in (4.A.2).

$$\begin{pmatrix} I_{1_j} \\ I_{2_j} \end{pmatrix} = \begin{pmatrix} 0 & \frac{K_o x_j}{M_o} \\ \frac{-K_o x_j}{M_T} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \tag{4.A.1}$$

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} 0 & \frac{K_o \sum x_j}{M_o} \\ \frac{-K_o \sum x_j}{M_o} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}. \tag{4.A.2}$$

The simple inversion of Y_n-matrix results in Z_n-matrix, as presented in (4.A.3). Notice that, for imposed voltage applications, the input and output currents are still unknown variables. In order to obtain their values, the summation, followed by the inversion of (4.A.3), as presented in (4.A.4), is suggested.

$$\begin{pmatrix} V_{1_j} \\ V_{2_j} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{M_o}{K_o x_j} \\ \frac{M_o}{K_o x_j} & 0 \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \tag{4.A.3}$$

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} 0 & \frac{K_o}{M_o}\frac{1}{\sum x_j{}^{-1}} \\ -\frac{K_o}{M_o}\frac{1}{\sum x_j{}^{-1}} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}. \qquad (4.A.4)$$

The G_n-matrix in IPOS configuration, according to ? is given as in (4.A.5). Due to power invariance, one can find the total output current from (4.A.2), resulting in (4.A.6). Substituting (4.A.6) in (4.A.5), results in the G_n-matrix representation as function of known variables, as presented in (4.A.7).

$$\begin{pmatrix} I_{1_j} \\ V_{2_j} \end{pmatrix} = \begin{pmatrix} 0 & \frac{-K_o x_j}{-I_2/V_1} \\ \frac{K_o x_j}{-I_2/V_1} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ I_2 \end{pmatrix} \qquad (4.A.5)$$

$$I_2 = \frac{-K_o \sum x_j}{NM_o} V_1 \qquad (4.A.6)$$

$$\begin{pmatrix} I_{1_j} \\ V_{2_j} \end{pmatrix} = \begin{pmatrix} 0 & \frac{-NM_o x_j}{\sum x_j} \\ \frac{NM_o x_j}{\sum x_j} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ I_2 \end{pmatrix} \qquad (4.A.7)$$

Finally, similarly, the H_j-matrix in ISOP configuration, according to *Table 4-I*, is given as in (4.A.8). Due to power invariance, one can find the total input current from (4.A.4), as presented in (4.A.9). Substituting (4.A.9) in (4.A.8), results in the H_j-matrix, as presented in (4.A.10) .

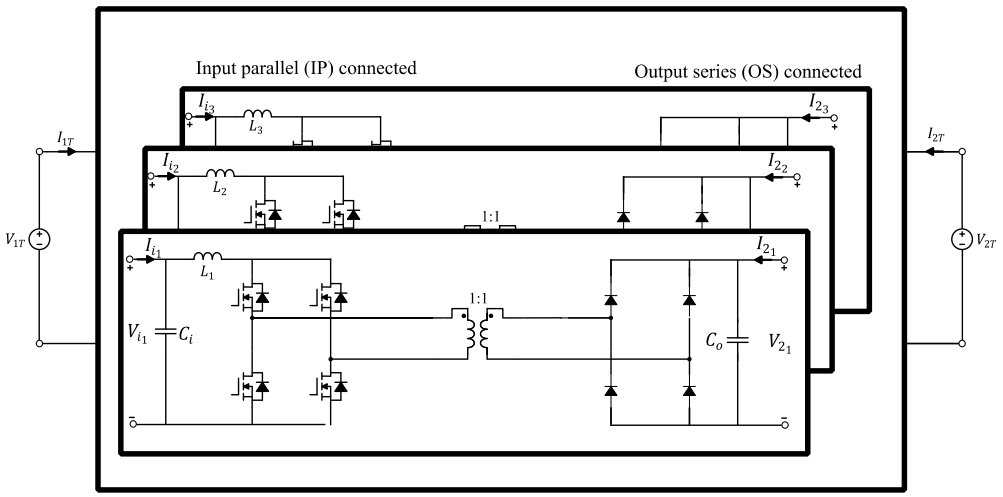
$$\begin{pmatrix} V_{1_n} \\ I_{2_n} \end{pmatrix} = \begin{pmatrix} 0 & \frac{I_1/V_2}{K_o x_n} \\ \frac{-I_1/V_2}{K_o x_n} & 0 \end{pmatrix} \begin{pmatrix} I_1 \\ V_2 \end{pmatrix} \qquad (4.A.8)$$

$$I_1 = \frac{K_o N}{M_o \sum {x_n}^{-1}} V_2 \tag{4.A.9}$$

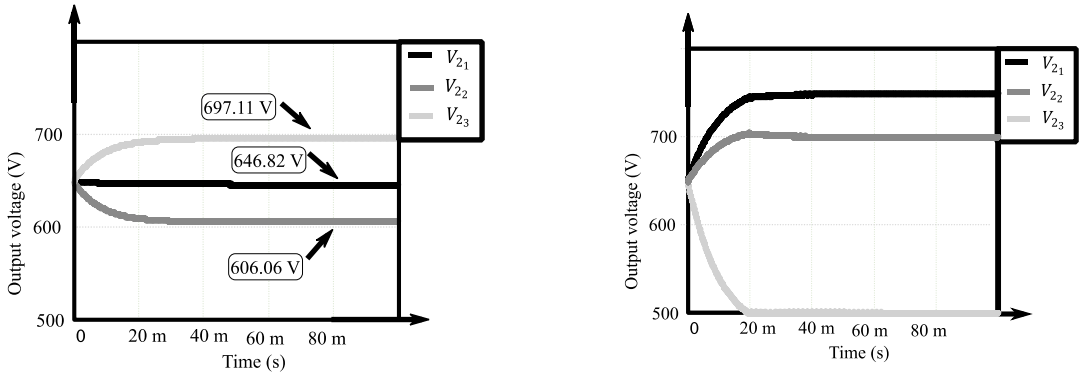
$$\begin{pmatrix} V_{1_j} \\ I_{2_j} \end{pmatrix} = \begin{pmatrix} 0 & \frac{N {x_n}^{-1}}{M_o \sum {x_n}^{-1}} \\ -\frac{N {x_n}^{-1}}{M_o \sum {x_n}^{-1}} & 0 \end{pmatrix} \begin{pmatrix} I_1 \\ V_2 \end{pmatrix} \tag{4.A.10}$$

Appendix 4.B Numerical illustration of a boost based converter connected in IPOS configuration

A numerical validation is provided for an isolated boost-based DC/DC converter (with rated values: input voltage $V_i = 200$ V; $V_o = 650$ V ; static gain $M_o = 3.25$; output current $I_o = 3.55$ A; input current $I_i = 11.55$ A; effective switching frequency $f_o = 100$ kHz, effective duty-cycle, $D_o = 3.25$, transformer turns ration $a = 1$. Three cell-converters are connected in IPOS, as presented in *Figure 0.1* (a) Isolated boot Full-bridge converter connected in IPOS configuration; (b) Simulation results of the output voltage for all three in DCM (left column); (c) Simulation results of the output voltage for all two in DCM and one in CCM (right column)., given by ideal parameters presented in *Table 0-I*. Two cases are presented: "*A"*, where all converters are working in DCM (left column) and "*B",* the third converter is set into CCM by increasing the inductance (right column). The idea of portraying such violent change in case in "*B"* is to show that the proposed theory can be used even in complicated cases by performing some adaptions.



(a)



(b) *(c)*

Figure 0.1 *(a) Isolated boot Full-bridge converter connected in IPOS configuration; (b) Simulation results of the output voltage for all three in DCM (left column); (c) Simulation results of the output voltage for all two in DCM and one in CCM (right column).*

Table 0-I Theoretical parameters of two cases of three isolated boost Full-bridge connected in IPOS.

Symbol parameters	**Theoretical value Case "A" (all in DCM)**	**Theoretical value Case "B" (two in DCM, one in CCM)**
V_{iT}; V_{oT} (V)	200; 1950	200; 1950
$D_1 = D_2 = D_3$ (effective duty cycle)	0.6	0.6
$a_1 = a_2 = a_3$	1:1	1:1
$L_1\,(rated)$; L_2; L_3 (µH)	50; 55; 45	50; 55; 100
C_i (µF)	20	20
C_o (µF)	60	60
$f_1 = f_2 = f_3$ (kHz) (effective switching frequency)	100	100

Case "A" (all in DCM)

The first step is to find the mismatch parameter values, as previously explained, resulting in $(x_1, x_2, x_3) = (1, 0.91, 1.11)$. By applying Table 4-III, for boost-based in DCM in (4.5), results in (0.1). It is, therefore, possible to resolve for the output voltage of each DC/DC converter, considering $M_o = 3.$ and $N = 3$

$$\begin{pmatrix} I_{1_j} \\ V_{2_j} \end{pmatrix} = \begin{pmatrix} 0 & -\left(1 + \dfrac{x_j(M_o - 1)N}{\sum x_j}\right) \\ 1 + \dfrac{x_j(M_o - 1)N}{\sum x_j} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ I_2 \end{pmatrix}. \tag{0.1}$$

Hence, $(V_{2_1}, V_{2_2}, V_{2_3}) = (646.9, 606.3, 696.6)$ V. For the total input and output currents, based on the IP connection power invariance, it is possible to show the following relation (0.2)

$$\begin{pmatrix} I_{IT} \\ I_{2T} \end{pmatrix} = \begin{pmatrix} 0 & \dfrac{K_o \sum x_j}{(M_o - 1)N} \\ -\dfrac{K_o \sum x_j}{(M_o - 1)N} & 0 \end{pmatrix} \begin{pmatrix} V_{1T} \\ V_{2T} \end{pmatrix}. \tag{0.2}$$

Hence, $(I_{1_T}, I_{2_T}) = (31.4, -3.2)$ A. The output current can be substitute in , and, therefore the input current across each DC/DC converter is $(I_{1_1}, I_{1_2}, I_{1_3}) = (10.4, 9.7, 11.2)$ A. The relative error between the proposed analytical and simulation results for input and output voltages and currents are all below 1%.

Otherwise, one can simply use Table 4-IV to derive the absolute value from deviated parameters as presented in (0.3) and (0.4), respectively for output voltages and input currents.

$$V_{2_j} = \frac{g_{21_j}}{M_o} V_o = \frac{\left(1 + \dfrac{x_j(M_o - 1)N}{\sum x_j}\right) V_o}{M_o} \tag{0.3}$$

$$I_{1_j} = \frac{g_{21_j} \sum x_j}{NM_o} I_i = \frac{\left(\sum x_j + N x_j (M_o - 1)\right) I_i}{NM_o}. \tag{0.4}$$

Case "B" (two in DCM and one in CCM)

In this case, the third DC/DC converter is kept in CCM by increasing the inductance L_3 up to 100 µH as presented in *Table 0-I* (right-hand side). The static gain of the third converter, which is in CCM is given by (0.5)

$$M_3 = \frac{1}{a_1(1 - D_3)}. \tag{0.5}$$

Hence, $M_3 = 2.5$ and $V_{2_3} = 500$ V. As aforementioned in 4.1.3.2 , the rule $\sum M_j = M_T$ must be applied for IPOS connections. It is interesting now to isolate the CCM from the DCM, by considering now ${M_o}' = \frac{7.5}{3}$ as in (4.15); and $N' = 2$.

$$\begin{aligned} M_T &= M_1 + M_2 + M_3 \\ {M_o}' &= \frac{M_T - M_3}{3}. \end{aligned} \tag{0.6}$$

Re-doing the same procedure as previously for ${M_o}'$ and N', $j = 1{,}2$ it is possible find the value of the output voltages. Hence, $(V_{2_1}, V_{2_2}) = (750, 700)$ V. Likewise, the output current is found through (0.2), hence $I_{2T} = 2.62$ A. The input current of the converters in DCM are found again through (0.1), and the input current in CCM is found by multiplying the output current, I_{2T}, by M_3. Hence $(I_{1_1}, I_{1_2}, I_{1_3}) = (9.82, 9.16, 6.54)$ A. As in previous results, the relative error between numeric simulation and analytical results are all below 1%.

Appendix 4.C Brief Short-circuit analysis and illustrative examples

Another interesting use of the proposed theory is the study of short-circuit through IS and /OS connections. To perform it, a more generic $\boldsymbol{Z}$- is proposed through the following steps:

- Transforming the $\boldsymbol{Z}$- into $\boldsymbol{T}$- parameters as already presented previously in (4.21);
- Cascading input and output with parallel impedances and generate a generic $\boldsymbol{T_{Generic}}$- matrix, as presented in (0.1)
- Transforming the generic $\boldsymbol{T_{Generic}}$- matrix into a generic $\boldsymbol{Z_{Generic}}$- following (4.22), resulting in (0.2).

$$\boldsymbol{T_{Generic}} = \begin{pmatrix} 1 & 0 \\ \frac{1}{z_i} & 1 \end{pmatrix} \frac{1}{z_{21}} \begin{pmatrix} z_{11} & \det(\boldsymbol{Z}) \\ 1 & z_{22} \end{pmatrix} \begin{pmatrix} 1 & 0 \\ \frac{1}{z_o} & 1 \end{pmatrix} = \begin{pmatrix} a_{generic} & b_{generic} \\ c_{generic} & d_{generic} \end{pmatrix}$$
$$= \frac{1}{z_{21}} \begin{pmatrix} z_{11} + \dfrac{\det(\boldsymbol{Z})}{z_o} & \det(\boldsymbol{Z}) \\ 1 + \dfrac{z_{22}}{z_o} + \dfrac{z_{11}}{z_i} + \dfrac{\det(\boldsymbol{Z})}{z_i z_o} & z_{22} + \dfrac{\det(\boldsymbol{Z})}{z_i} \end{pmatrix} \quad (0.1)$$

$$\boldsymbol{T_{Generic}} \rightarrow \boldsymbol{Z_{Generic}} = \frac{1}{c_{generic}} \begin{pmatrix} a_{generic} & \det(\boldsymbol{T_{Generic}}) \\ 1 & d_{generic} \end{pmatrix}$$
$$= \frac{1}{z_{21}} \frac{1}{\left(1 + \dfrac{z_{22}}{z_o} + \dfrac{z_{11}}{z_i} + \dfrac{\det(\boldsymbol{Z})}{z_i z_o}\right)} \begin{pmatrix} z_{11} + \dfrac{\det(\boldsymbol{Z})}{z_o} & \det(\boldsymbol{T_{Generic}}) \\ 1 & z_{22} + \dfrac{\det(\boldsymbol{Z})}{z_i} \end{pmatrix} \quad (0.2)$$

Of course, it can be composed other and more sophisticated generic two-port network matrixes, including containing imaginary (complex), representing input and output capacitances or parallel losses, and series impedances, representing interconnections losses.

In this numerical example, the CSCs are connected in ISOS. For simplicity, all cells have the same parameters, the rated one presented in previous sub-sections, and, therefore, mismatch is not evaluated. Assuming all six cells present a very large parallel input and

output impedance, 1000 Ω, but one of them is short-circuited at the output with an impedance of 0.01 Ω. The two cell types are classified as "Healthy", other as "Shorted". As it can be seen, the feature of continuous working even under short circuit fault condition is proved mathematically for ISOS connection, with the drawback of instantaneous power and efficiency reduction. If a feedback control to keep at rated value, 2.5 A, the total efficiency is dropped to 66%.

Table 0-I Analytical results for short circuit at the output.

Symbol parameters	**Cell "healthy"**	**Cell "shorted output"**	**Total**
I_1 (A)	2.56	2.56	2.56
I_2 (A)	-1.97	-1.97	2.5
V_1 (V)	14.93	15.38	90
V_2 (V)	18	0.03	90
P_1(W)	38.26	39.43	230.7
P_2 (W)	35.52	0.06	177.66
η (%)	92.8	0	77.7
M	1.2	0	1

If, now, the short circuit happens at the input voltage, it is interesting observe a static result in which negative voltage is observed across the output H-bridge. Instantaneously, a negative voltage through the body diodes of the MOSFET will also "short" the secondary side with the voltage across its port as the sum of the two body diodes in series (0.6 V for MOSFETs). At this point, it is fair to approximate the output H-bridge with a parallel impedance of 0.21 Ω to get the needed equivalent voltage drop. For the aforementioned example, when z_i = 0.01 Ω and z_o = 0.21 Ω (set in order to get 0.6 V drop), results in sharing as presented in *Table 0-II*

Table 0-II Analytical results for short circuit at the input.

Symbol parameters	**Cell "healthy"**	**Cell "shorted output"**	**Total**
I_1 (A)	3.07	3.07	3.07
I_2 (A)	-2.97	-2.97	-2.97
V_1 (V)	17.99	0.031	90
V_2 (V)	18.12	-0.6	90
P_1(W)	55.35	0.09	276.83
P_2 (W)	53.9	-1.79	267.85
η (%)	97.43	-	96.8
M	3.07	3.07	3.07

Notice that, an increase in power, even larger than rated, is observed. Indeed efficiency is also improved for this specific case, proving again the short circuit tolerance and redundancy in series connections. This takes us to the conclusion that, if short-circuit happens at one of the H-bridges, actions could be taken to short circuit both input and output of the H-bridges to protect the multicell-converter and the other H-bridge.

Of course, short-circuit analysis are much more complex and the dynamics play a much more important role. It was presented, on the other hand, the steady state analysis when ISOS are subjected to short-circuit, which helps easily comprehending a highly complex behavior and even propose actions for improving redundancy of modular converters.

Appendix 6.A Analytic equation to calculate the magnetic near field produce by interconnections

Input current loops

Once the methodology for finding the near field of any segment on the xy-plane is presented, the next subsections present an algorithm for calculating the near magnetic field produced by the sending path, returning path A1 and returning path B_1, and their comparison. The RMS value of the input current is given as 1 A for exemplifying purposes. In All the segments will be referenced with respect to a geometric centre of the PCA, but any reference could be adopted. This work considers the 2-D synthesised structures, but same process can be performed for z-segments or shift on the z-direction. Loop sizes are expressed with respect to PCA's sizes according to the following set of equations (0.1)-(0.4)

$$W_{PCA} = (W_{CSC} + j_x)C + j_x \tag{0.1}$$

$$L_{PCA} = L_{CSC}L + j_y(L-1) \tag{0.2}$$

$$L_M = 2\left(L_{CSC} - d_y\right) + j_y \tag{0.3}$$

$$L_m = 2d_y + j_y \tag{0.4}$$

Sending input current path

- x-segments:

$$\mathrm{T}_{xS_1}\left(x,y,z,l_x(n)\right) = \begin{pmatrix} l_x(n) = W_{PCA} \\ x - \dot{\Delta}_{xx}(n) = x - \left(-\frac{W_{PCA}}{2}\right) \\ y - \dot{\Delta}_{xy}(n) = y - \begin{pmatrix} \frac{L_{PCA}}{2} - d_y - \left(\frac{n-1}{2} + \frac{1+(-1)^n}{4}\right)L_M \\ -\left(\frac{n-1}{2} - \frac{1+(-1)^n}{4}\right)L_m \end{pmatrix} \\ z - \Delta_{xz}(n) = z - 0 \end{pmatrix} \quad (0.5)$$

$$B_{S_1 x\to yz}(x,y,z,I_i) = \sum_{n=1}^{L}(-1)^{n+1}\, B_{x\to yz}\left(\mathrm{T}_{xS_1}\left(x,y,z,l_x(n)\right), I_i\right). \quad (0.6)$$

- y-segments:

$$\mathrm{T}_{yS_1}\left(x,y,z,l_y(n)\right) = \begin{pmatrix} l_y(n) = \dot{\Delta}_{xy}(n) - \dot{\Delta}_{xy}(n+1) \\ x - \Delta_{yx}(n) = x - \left(-\frac{W_{PCA}}{2}(-1)^n\right) \\ y - \Delta_{yy}(n) = y - \dot{\Delta}_{xy}(n+1) \\ z - \Delta_{yz}(n) = z - 0 \end{pmatrix} \quad (0.7)$$

$$B_{S_1 y\to xz}(x,y,z,I_i) = \sum_{n=1}^{L-1} B_{y\to xz}\left(\mathrm{T}_{yS_1}\left(x,y,z,l_y(n)\right), I_i\right). \quad (0.8)$$

- xy-segments superposition of the input current sending path:

Finally, the expression for the magnetic field density of the input current across the sending path in (0.9), it is presented the z-component of the magnetic field density of a PCA_{4x3} over the plane π: z = 20 mm.

$$B_{S_1 xy\to xyz}(x,y,z,I_i) = B_{S_1 x\to yz}(x,y,z,I_i) + B_{S_1 y\to xz}(x,y,z,I_i). \quad (0.9)$$

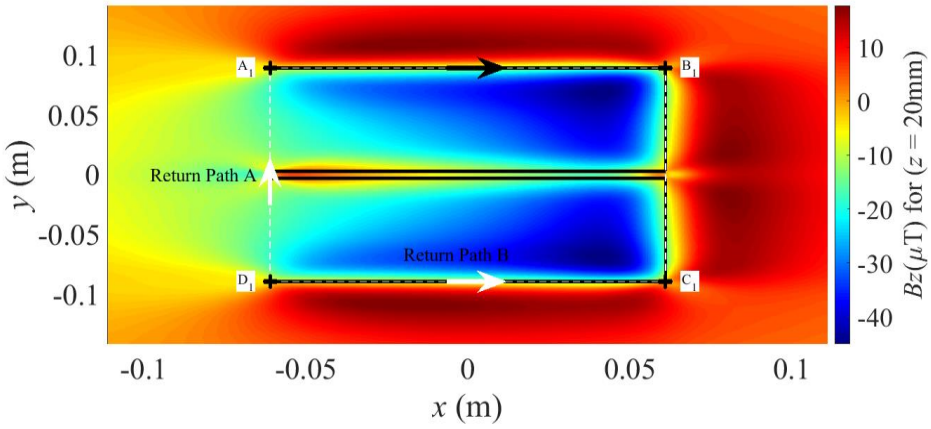


Figure 0.1 z-component of the computed input current sending path magnetic field of a PCA4x3 over the plane parallel to the plane of CSC's interconnections and located above it at z = 20 mm. The return path from D_1 to A_1 is not taken into account in that computation.

As it can be noticed, the strongest fields produced by the input current are located at the PCA's right-hand side, and, therefore, a current flowing into the positive y-direction at such region is recommended for field cancelation. This could mean that the returning path B should be privileged for such purpose.

Returning input current path A

- x-segments:

$$\mathrm{T}_{RA_1x}\left(x,y,z,l_x(1)\right)=\begin{pmatrix} l_x(1)=W_{PCA} \\ x-\Delta_{xx}(1)=x-\left(-\frac{W_{PCA}}{2}\right) \\ y-\Delta_{xy}(1)=y-\dot{\Delta}_{xy}(L) \\ z-\Delta_{xz}(1)=z-0 \end{pmatrix} \tag{0.10}$$

$$B_{RA_1x\to yz}(x,y,z,I_i)=-\left(\frac{1+(-1)^{L+1}}{2}\right)B_{y\to xz}\left(\mathrm{T}_{RA_1x}\left(x,y,z,l_x(1)\right),I_i\right). \tag{0.11}$$

- y-segments:

$$\mathrm{T}_{RA_1y}\left(x,y,z,l_y(1)\right)=\begin{pmatrix}\dot{l_y}(1)=L_{PCA}-2d_y-\left(L_{CSC}-2d_y\right)\left(\dfrac{1-(-1)^L}{2}\right)\\ x-\Delta_{yx}(1)=x-\left(-\dfrac{W_{PCA}}{2}\right)\\ y-\Delta_{yy}(1)=y-\dot{\Delta}_{xy}(L)\\ z-\Delta_{yz}(1)=z-0\end{pmatrix} \quad (0.12)$$

$$B_{RA_1y\to xz}(x,y,z,I_i)=-B_{y\to xz}\left(\mathrm{T}_{RA_1x}\left(x,y,z,l_y(1)\right),I_i\right). \quad (0.13)$$

- xy-segments superposition:

$$B_{RA_1xy\to xyz}(x,y,z,I_i)=B_{RA_1x\to yz}(x,y,z,I_i)+B_{RA_1y\to xz}(x,y,z,I_i). \quad (0.14)$$

7.8.1.1 Returning input current path B

- x-segments:

$$\mathrm{T}_{RB_1x}\left(x,y,z,l_x(n)\right)=\begin{pmatrix}l_x(n)=W_{PCA}\\ x-\Delta_{xx}(n)=x-\left(-\dfrac{W_{PCA}}{2}\right)\\ y-\Delta_{xy}(n)=y-\left(\dfrac{L_{PCA}}{2}-d_y\right)(-1)^n\\ z-\Delta_{xz}(1)=z-0\end{pmatrix} \quad (0.15)$$

$$B_{RA_1x\to yz}(x,y,z,I_i)=\sum_{n=1}^{2}(-1)^{n+1}\left(\frac{1+(-1)^{nL}}{2}\right)B_{x\to yz}\left(\mathrm{T}_{RB_1x}\left(x,y,z,l_x(n)\right),I_i\right). \quad (0.16)$$

- y-segments:

$$\mathrm{T}_{RB_1y}\left(x,y,z,l_y(1)\right)=\begin{pmatrix}l_y(1)=\dot{l_y}(1)\\ x-\Delta_{yx}(1)=x-\left(\dfrac{W_{PCA}}{2}\right)\\ y-\Delta_{yy}(1)=y-\dot{\Delta}_{xy}(L)\\ z-\Delta_{xz}(1)=z-0\end{pmatrix} \quad (0.17)$$

$$B_{RB_1y\to xz}(x,y,z,I_i)=-B_{x\to yz}\left(\mathrm{T}_{RB_1y}\left(x,y,z,l_y(1)\right),I_i\right). \quad (0.18)$$

- xy-segments superposition:

$$B_{RB_1xy\to xz}(x,y,z,I_i) = B_{RB_1x\to yz}(x,y,z,I_i) + B_{RB_1y\to xz}(x,y,z,I_i). \quad (0.19)$$

Comparison between input current loop paths A1 and B1

As their results are symmetrical over the x-axes, it is possible to plot only half of them side by side, allowing easier comparisons through same scales. This is implemented in all the following plotting in order to ease near field EMI generation depending on the return path. In Figure 0.2, it is presented the comparison results of the z-components for the two different returning paths A and B, while Figure 0.3 presents the magnitude (all vector components) of the near field. The magnitude is interesting as a worst case scenario evaluation, because, at particular point normal to the magnetic density vector, the magnetic flux will be maximum, condensing information of all xyz-components.

- xy-segments superposition of sending and returning path A1:

$$B_{SRA_1xy\to xyz}(x,y,z,I_i) = B_{S_1xy\to xyz}(x,y,z,I_i) + B_{RA_1xy\to xyz}(x,y,z,I_i). \quad (0.20)$$

- xy-segments superposition of sending and returning path B1:

$$B_{SRB_1xy\to xyz}(x,y,z,I_i) = B_{S_1xy\to xyz}(x,y,z,I_i) + B_{RB_1xy\to xyz}(x,y,z,I_i). \quad (0.21)$$

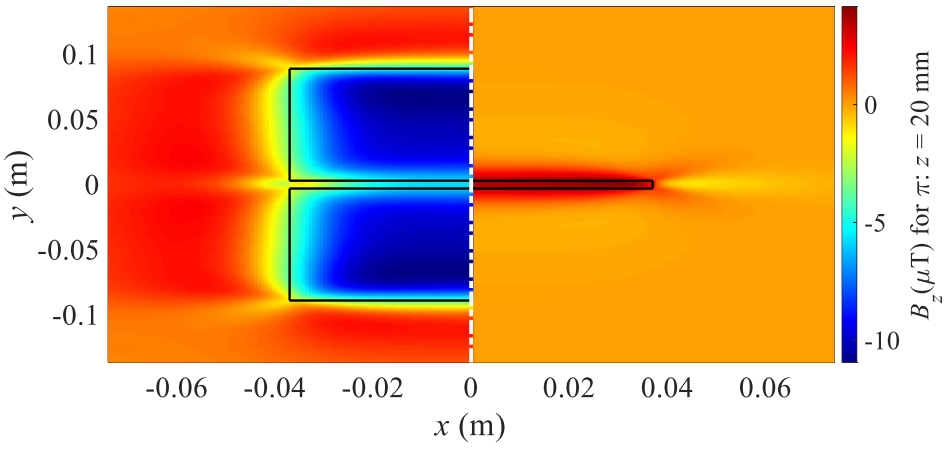


Figure 0.2 z-components of the magnetic field results produced by input current loop of a PCA4x3 over the plane π: z = 20 mm considering the returning path A1 (left); and the returning path B1 (right). Thanks to symmetries, only half loops are plotted.

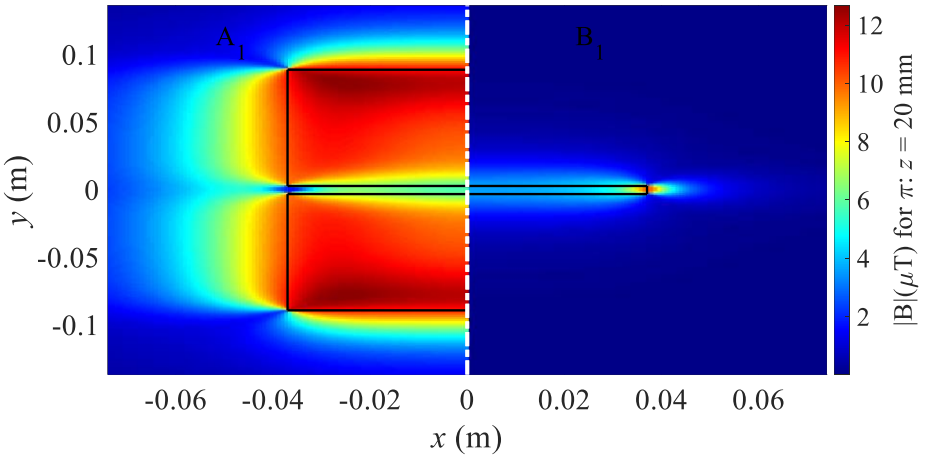


Figure 0.3 Magnitude of the magnetic field results produced by input current loop of a PCA4x3 over the plane π: z = 20 mm considering the returning path A1 (left); and the returning path B1 (right). Thanks to symmetries, only half loops are plotted.

Another point of discussion is that, even though smaller in surface area compared to loop A, the loop path B is much longer, and as aforementioned, far field due to CMC (proportional to the length of the path) could be a tradeoff versus near field due to DMC (proportional to the area of the path) to be yet analyzed in future studies.

Output current loops

The output current effect is also computed and superposed with the input one. However, as aforementioned the currents are considered to be decoupled and mutual inductance effects are neglected. The algorithm for output current path can easily be expressed easily as a function of the input current, by properly translating and rescaling size, as presented in the next subsections. It is presented the expressions for the sending output current path, returning path A_2, returning path and their comparison. The RMS value of the output current is likewise adopted as 1 A.

Sending output current path

- x-segments:

$$\mathrm{T}_{xS_2}(x,y,z,l_x(n)) = \mathrm{T}_{xS_1}\left(x, y-\left[(-1)^n\left(L_{CSC}-2d_y\right)\right], z, l_x(n)\right) = \begin{pmatrix} l_x(n) = W_{PCA} \\ x - \ddot{\Delta}_{xx}(n) = x - \left(-\frac{W_{PCA}}{2}\right) \\ y - \ddot{\Delta}_{xy}(n) = y - \left(\dot{\Delta}_{xy}(n) + (-1)^n\left(L_{CSC}-2d_y\right)\right) \\ z - \Delta_{xz}(n) = z - 0 \end{pmatrix} \tag{0.22}$$

$$B_{S_2x\to yz}(x,y,z,I_o) = \sum_{n=1}^{L}(-1)^{n+1}\, B_{x\to yz}\left(\mathrm{T}_{xS_2}(x,y,z,l_x(n)), I_o\right). \tag{0.23}$$

- y-segments:

$$\mathrm{T}_{yS_2}(x,y,z,l_x(n)) = \mathrm{T}_{yS_1}\left(x, y-\left[(-1)^n\left(L_{CSC}-2d_y\right)\right], z, l_y(n)\right) = \begin{pmatrix} l_y(n) = \ddot{\Delta}_{xy}(n) - \ddot{\Delta}_{xy}(n+1) \\ x - \Delta_{yx}(n) = x - \left(-\frac{W_{PCA}}{2}(-1)^n\right) \\ y - \Delta_{yy}(n) = y - \ddot{\Delta}_{xy}(n+1) \\ z - \Delta_{yz}(n) = z - 0 \end{pmatrix} \tag{0.24}$$

$$B_{S_2y\to xz}(x,y,z,I_o) = \sum_{n=1}^{L-1} B_{y\to xz}\left(\mathrm{T}_{xS_2}(x,y,z,l_x(n)), I_o\right). \tag{0.25}$$

- xy-segments superposition of sending path:

$$B_{S_2xy\to xyz}(x,y,z,I_o) = B_{S_2x\to yz}(x,y,z,I_o) + B_{S_2y\to xz}(x,y,z,I_o). \tag{0.26}$$

The expression for the magnetic field density of the output current across the sending path is presented in (0.26)**Erreur ! Source du renvoi introuvable.** In *Figure 0.4* **Erreur ! Source du renvoi introuvable.**, it is presented the z-component of the magnetic field density of a PCA_{4x3} over the plane π: z = 20 mm.

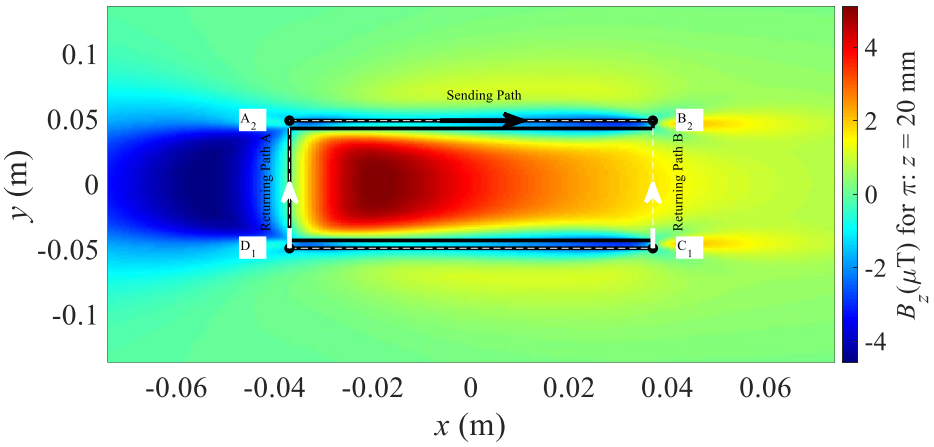


Figure 0.4 z-component of the computed output current sending path magnetic field of a PCA4x3 over the plane parallel to the plane of CSC's interconnections and located above it at z = 20 mm. The return path from d1 to a1 is not taken into account in that computation.

As it can be noticed, the strongest fields produced by the output current are located at the PCA's left-hand side, and, therefore, a current flowing into the positive y-direction at such region is recommended for field cancelation. This means that the returning path A_2 should be privileged for such purpose, as it is later demonstrated. Besides, notice that the compromises length vs area does not exist for the output current, as the shortest returning path result into smaller areas.

Returning output current path A2

- *x*-segments:

$$\mathrm{T}_{xRA_2}(x,y,z,l_x(1)) = \mathrm{T}_{xRA_1}\left(x, y-\left[(-1)^L\left(L_{CSC}-2d_y\right)\right], z, l_x(1)\right) = \begin{pmatrix} l_x(1) = W_{PCA} \\ x-\Delta_{xx}(1) = x-\left(-\frac{W_{PCA}}{2}\right) \\ y-\Delta_{xy}(1) = y-\ddot{\Delta}_{xy}(L) \\ z-\Delta_{xz}(1) = z-0 \end{pmatrix} \quad (0.27)$$

$$B_{RA_2 x\to yz}(x,y,z,I_o) = -\left(\frac{1+(-1)^{L+1}}{2}\right) B_{x\to yz}\left(\mathrm{T}_{xRA_2}(x,y,z,l_x(1)), I_o\right). \quad (0.28)$$

- *y*-segments:

$$\begin{aligned}&\mathrm{T}_{yRA_2}\left(x,y,z,l_x(1)\right)\\&\quad=\mathrm{T}_{yRA_1}\Big(x,y-\left[(-1)^L\left(L_{CSC}-2d_y\right)\right],z,l_y(1)\\&\quad-\left(L_{CSC}-2d_y\right)\left(1+(-1)^L\right)\Big)\\&\quad=\begin{pmatrix}l_y(1)=\dot{l_y}(1)-\left(L_{CSC}-2d_y\right)\left(1+(-1)^L\right)\\x-\Delta_{yx}(1)=x-\left(-\frac{W_{PCA}}{2}\right)\\y-\Delta_{yy}(1)=y-\ddot{\Delta}_{xy}(L)\\z-\Delta_{yz}(1)=z-0\end{pmatrix}\end{aligned}\tag{0.29}$$

$$B_{RA_2y\to xz}(x,y,z,I_o)=-B_{y\to xz}\left(\mathrm{T}_{yRA_2}\left(x,y,z,l_x(1)\right),I_o\right).\tag{0.30}$$

- *xy*-segments superposition:

$$B_{RA_2xy\to xyz}(x,y,z,I_o)=B_{RA_2x\to yz}(x,y,z,I_o)+B_{RA_2y\to xz}(x,y,z,I_o).\tag{0.31}$$

Returning output current path B_2

- *x*-segments:

$$\begin{aligned}&\mathrm{T}_{xRB_2}\left(x,y,z,l_x(1)\right)=\mathrm{T}_{xRB_1}\Big(x,y-\left[\left(L_{CSC}-2d_y\right)(-1)^n\right],z,l_x(1)\Big)\\&=\begin{pmatrix}l_x(1)=W_{PCA}\\x-\Delta_{xx}(1)=x-\left(-\frac{W_{PCA}}{2}\right)\\y-\Delta_{xy}(1)=y-\left(\frac{L_{PCA}}{2}-d_y\right)(-1)^n-\left[\left(L_{CSC}-2d_y\right)(-1)^n\right]\\z-\Delta_{xz}(1)=z-0\end{pmatrix}\end{aligned}\tag{0.32}$$

$$B_{RB_2x\to yz}(x,y,z,I_o)=\sum_{n=1}^{2}(-1)^{n+1}\left(\frac{1+(-1)^{nL}}{2}\right)B_{x\to yz}\left(\mathrm{T}_{xRB_2}\left(x,y,z,l_x(1)\right),I_o\right).\tag{0.33}$$

- *y*-segments:

$$\begin{aligned}
&\mathrm{T}_{yRB_2}\left(x,y,z,l_x(1)\right)\\
&\quad=\mathrm{T}_{yRB_1}\Big(x,y-\left[\left(L_{CSC}-2d_y\right)(-1)^L\right],z,l_y(1)\\
&\quad-\left(L_{CSC}-2d_y\right)(1+(-1)^L)\Big)\\
&\quad=\begin{pmatrix} l_y(1)=\dot{l_y}(1)-\left(L_{CSC}-2d_y\right)(1+(-1)^L)\\ x-\Delta_{yx}(1)=x-\left(\frac{W_{PCA}}{2}\right)\\ y-\Delta_{yy}(1)=y-\ddot{\Delta}_{xy}(L)\\ z-\Delta_{yz}(1)=z-0\end{pmatrix}
\end{aligned} \tag{0.34}$$

$$B_{RB_2y\to xz}(x,y,z,I_o)=-B_{y\to xz}\left(\mathrm{T}_{yRB_2}\left(x,y,z,l_x(1)\right),I_o\right). \tag{0.35}$$

- *xy*-segments superposition:

$$B_{RB_2xy\to xyz}(x,y,z,I_o)=B_{RB_2x\to yz}(x,y,z,I_o)+B_{RB_2y\to xz}(x,y,z,I_o). \tag{0.36}$$

Comparison between output current loop paths A_2 and B_2

As previously made for the input current, the comparisons are made considering the symmetry over the x-axes, as presented in Figure 0.5 for z-components and Figure 0.6for its magnitude.

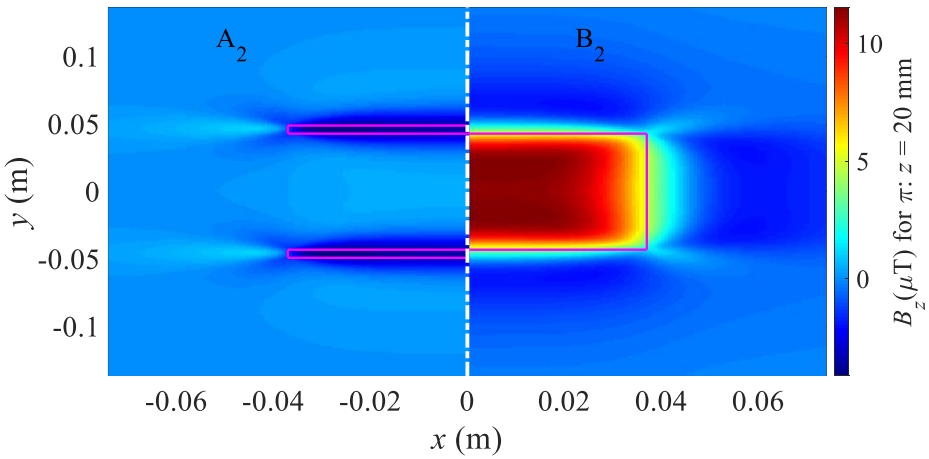


Figure 0.5 z-components of the magnetic field results produced by output current loop of a PCA4x3 over the plane π: z = 20 mm considering the returning path A2 (left); and the returning path B2 (right). Thanks to symmetries, only half loops are plotted.

- xy-segments superposition of sending and returning path A2:

$$B_{SRA_2xy\to xyz}(x,y,z,I_o) = B_{S_2xy\to xyz}(x,y,z,I_o) + B_{RA_2xy\to xyz}(x,y,z,I_o). \quad (0.37)$$

- xy-segments superposition of sending and returning path B2:

$$B_{SRB_2xy\to xyz}(x,y,z,I_o) = B_{S_2xy\to xyz}(x,y,z,I_o) + B_{RB_1xy\to xyz}(x,y,z,I_o). \quad (0.38)$$

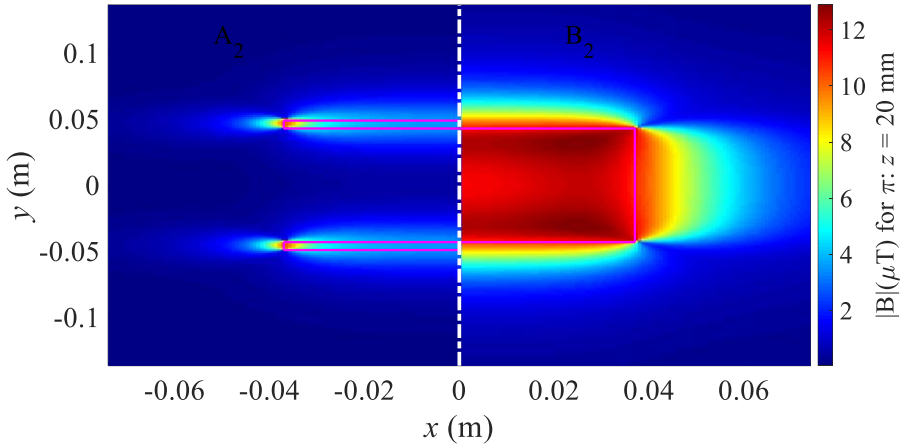


Figure 0.6 Magnitude of the magnetic field results produced by output current loop of a PCA4x3 over the plane π: z = 20 mm considering the returning path A2 (left); and the returning path B2 (right). Thanks to symmetries, only half loops are plotted.

All input and output current loop combinations

Finally, it is applied superposition principle on the input (0.39) —(0.42).

- Combination A_1A_2:

$$B_{A_1A_2xy\to xyz}(x,y,z,I_i,I_o) = B_{SRA_1xy\to xyz}(x,y,z,I_i) + B_{SRA_2xy\to xyz}(x,y,z,I_o). \quad (0.39)$$

- Combination A_1B_2:

$$B_{A_1B_2xy\to xyz}(x,y,z,I_i,I_o) = B_{SRA_1xy\to xyz}(x,y,z,I_i) + B_{SRB_2xy\to xyz}(x,y,z,I_o). \quad (0.40)$$

- Combination B_1A_2:

$$B_{B_1A_2xy\to xyz}(x,y,z,I_i,I_o) = B_{SRB_1xy\to xyz}(x,y,z,I_i) + B_{SRA_2xy\to xyz}(x,y,z,I_o). \quad (0.41)$$

- Combination B_1B_2:

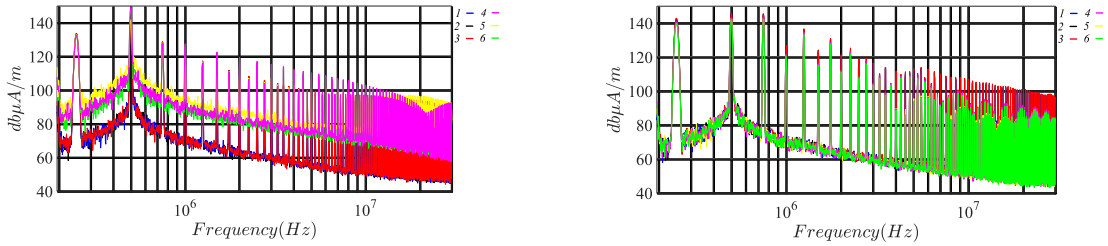
$$B_{B_1B_2xy\to xyz}(x,y,z,I_i,I_o) = B_{SRB_1xy\to xyz}(x,y,z,I_i) + B_{SRA_2xy\to xyz}(x,y,z,I_o). \quad (0.42)$$

Appendix 6.A OC vs Full load (Io = 2.5 A) both at M = 1.2

Near field probe:

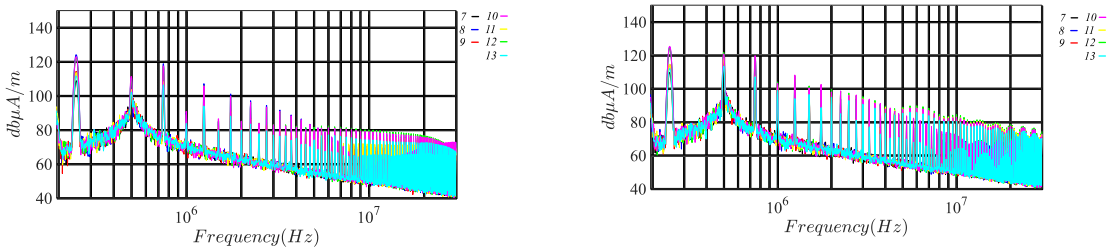
It is worth comparing and investigating full load and OC in order to assure if OC testing at *M* = 1.2 may be representative cases even for the radiated near field. The results are divided into CE frequency range((a) OC operating point and (b) full load operating point) and RE frequency (a) OC operating point and (b) full load operating point).

- CE range (150 kHz – 30 MHz):



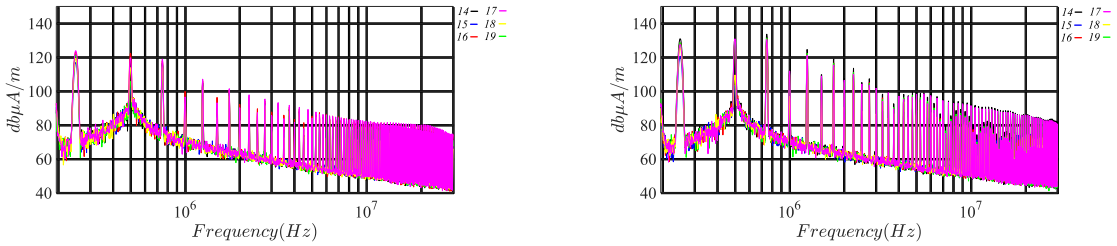
(a) *(b)*

Figure 0.1 Experimental near field measured for points from 1 to 6 for the CE frequency range 150 kHz – 30 MHz (RBW = 9 kHz; VBW = 30 kHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2) full load (Io = 2.5 A).



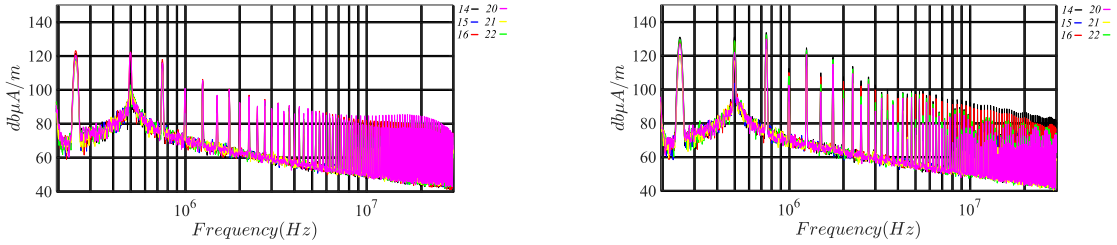
(a) *(b)*

Figure 0.2 Experimental near field measured for points from 7 to 13 for the CE frequency range 150 kHz – 30 MHz (RBW = 9 kHz; VBW = 30 kHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2) full load (Io = 2.5 A).



(a) *(b)*

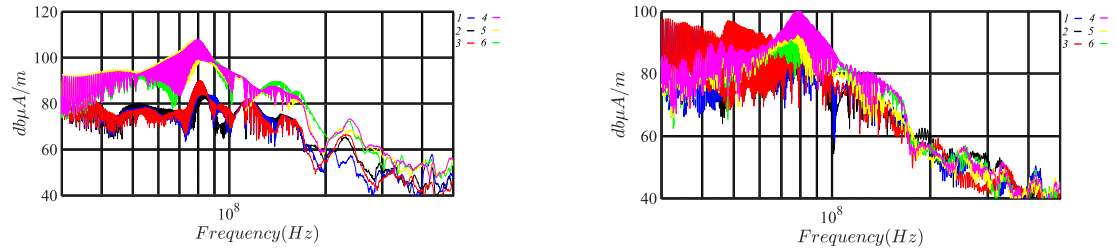
Figure 0.3 Experimental near field measured for points from 14 to 19 for the CE frequency range 150 kHz – 30 MHz (RBW = 9 kHz; VBW = 30 kHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2) full load (Io = 2.5 A).



(a) *(b)*

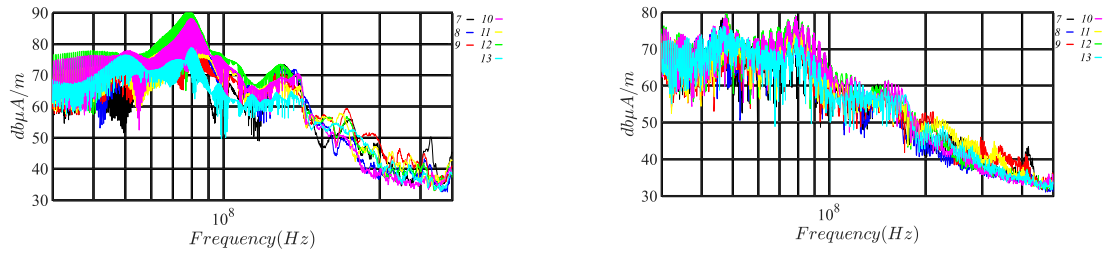
Figure 0.4 Experimental near field measured for points from 14 to 16 and from 20 to 22 for the CE frequency range 150 kHz – 30 MHz (RBW = 9 kHz; VBW = 30 kHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2) full load (Io = 2.5 A).

- RE range (30 MHz – 500 MHz):



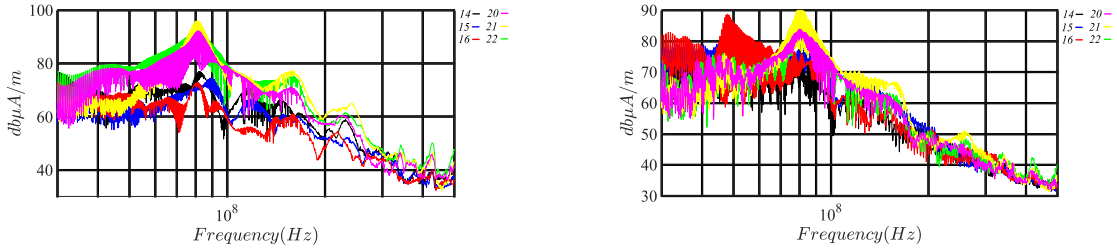
(a) *(b)*

Figure 0.5 Experimental near field measured for points from 1 to 6 for the RE frequency range 30MHz – 500 MHz (RBW = 120 kHz; VBW = 3 MHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2) full load (Io = 2.5 A).



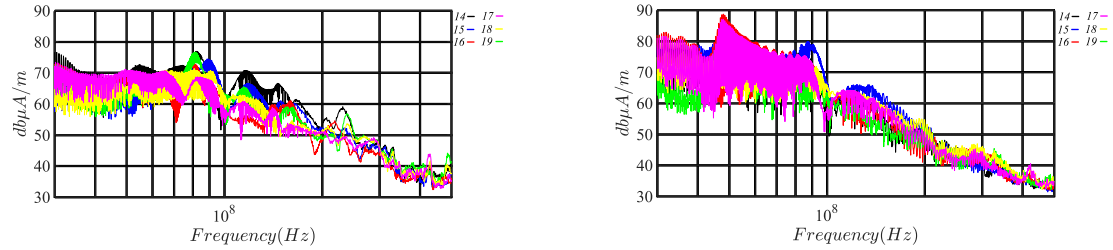
(a) *(b)*

Figure 0.6 Experimental near field measured for points from 7 to 13 for the RE frequency range 30MHz – 500 MHz (RBW = 120 kHz; VBW = 3 MHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2)full load (Io = 2.5 A).



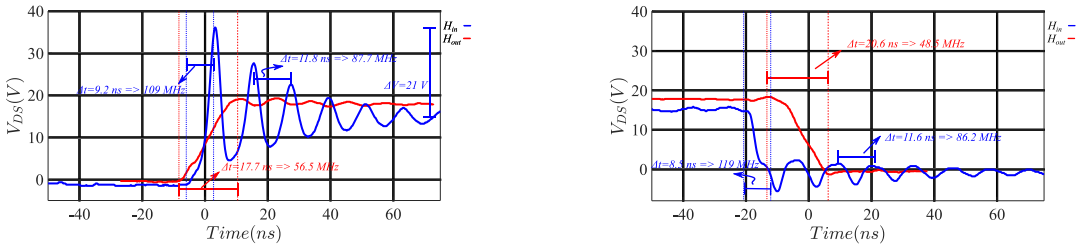
(a) *(b)*

Figure 0.7 Experimental near field measured for points from 14 to 22 for the RE frequency range 30MHz – 500 MHz (RBW = 120 kHz; VBW = 3 MHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2) full load (Io = 2.5 A).



(a) *(b)*

Figure 0.8 Experimental near field measured for points from 14 to 16 and from 20 to 22 for the RE frequency range 30MHz – 500 MHz (RBW = 120 kHz; VBW = 3 MHz): (a) Step-up (M=1.2) OC; (b) Step-up (M=1.2) full load (Io = 2.5 A).



(a) *(b)*

Figure 0.9 Step-up (M=1.2) OC experimental drain to source voltage V_{DS} (CSC 2) across H_{in} (blue color) and H_{out} (red color): (a) rise time; (b) fall time. It is possible to observe incomplete ZVS and its effect.