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THÈSE PRÉSENTÉE

POUR OBTENIR LE GRADE DE

DOCTEURE DE
L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR

SPÉCIALITÉ ÉLECTRONIQUE

Karthi PRADEEP

CONTRIBUTION À LA CARACTÉRISATION SUR WAFER DE TRANSISTORS MOS FD-SOI EN BANDE MILLIMÉTRIQUE

CONTRIBUTION TO ON-WAFER CHARACTERIZATION OF MILLIMETER-WAVE FD-SOI MOS TRANSISTORS

Sous la direction de : **Thomas ZIMMER**
(co-directeur : **Sébastien FREGONESE**)

Soutenue le 28 Juin 2023

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Abstract - EN

Silicon bipolar and CMOS technologies have been recognized for their abilities in millimeter-wave applications, making them good candidates for circuit realization in the THz domain. Among them, the "Fully-Depleted-Silicon-On-Insulator" (FD-SOI) technologies developed from the 28nm node offer promising performances for transition frequencies (f_T) and maximum oscillation frequencies (f_{MAX}) beyond 300 GHz, and even more for the most advanced nodes. At the same time, the development of millimeter-wave circuits is booming, with realizations at ever higher frequencies, some of which go beyond 100 GHz. To enable the design of circuits operating at millimeter-wave frequencies, an accurate modeling of FD-SOI transistors is essential. Furthermore, it is no longer possible to limit parameter extraction below 110 GHz, and new techniques for obtaining reliable measurements of passive and active devices need to be investigated. In this thesis, we will examine the on-wafer S-parameter characterisation of different passive test structures and MOS transistors in 28nm FD SOI technology from STMicroelectronics, up to 500 GHz.

We will start with an introduction to the measurement equipment usually used for this type of analysis, then move on to the different measurement benches adopted in the IMS laboratory, and finally focus on the calibration and de-embedding techniques. Two different chips were studied. For each chip, we will introduce a new floorplan design and evaluate its ability to limit spurious effects. For our analysis, we will rely on electromagnetic simulations and mixed small signal plus probe model EM simulations, both including the probe models for a closer evaluation of the measurement results under real conditions. Finally, we will present some test structures to evaluate the losses in the lines, the accuracy of the impedance correction methodology and finally the probe-to-probe and probe-to-substrate coupling.

Keywords: Characterization, Transmission Lines, THz, Millimeter-Wave, On-Wafer Calibration, MOSFET on FDSOI

Résumé - FR

Les technologies bipolaires et CMOS sur silicium présentent des aptitudes reconnues pour les applications millimétriques, ce qui font d'elles de bonnes candidates pour la réalisation de circuits dans le domaine du THz. Parmi elles, les technologies « Fully-Depleted-Silicon-On-Insulator » (FD-SOI) développées à partir du nœud 28nm offrent des caractéristiques prometteuses pour un vaste champ d'applications, avec notamment des fréquences de transition, f_T, et d'oscillation maximum, f_{MAX}, au-delà de 300 GHz, voire plus encore en ce qui concerne les nœuds les plus avancés. Dans le même temps, le développement de circuits en bande millimétrique est en plein essor, avec des réalisations à des fréquences toujours plus élevées et pour certaines au-delà de 110 GHz. Pour permettre la conception de ces circuits, une modélisation précise des transistors FD-SOI est absolument nécessaire. De plus, il n'est plus possible de limiter l'extraction des paramètres en dessous de 110 GHz, et de nouvelles techniques permettant d'obtenir des mesures fiables de dispositifs passifs et actifs doivent être étudiées. Dans cette thèse, nous examinerons la caractérisation des paramètres S sur silicium (on-wafer) de différentes structures de test passives et des transistors MOS en technologie 28nm FD SOI de STMicroelectronics, jusqu'à 500 GHz.

Nous commencerons par une introduction de l'équipement de mesure habituellement utilisé pour ce type d'analyse, puis nous passerons aux différents bancs de mesure adoptés au laboratoire IMS, et enfin nous nous concentrerons sur les techniques de calibrage et d'épluchage (de-embedding). Deux différentes puces ont été étudiées. Pour chaque puce, nous introduirons un nouveau design du floorplan et évaluerons sa capacité à limiter les effets parasites. Pour notre analyse, nous nous appuierons sur des simulations électromagnétiques et des simulations EM mixtes de modèle petit signal + sonde, toutes deux incluant les modèles des sondes pour une évaluation des résultats de mesure plus proche des conditions réelles. Enfin, nous présenterons quelques structures de test pour évaluer les pertes dans les lignes, la précision de la méthodologie de correction d'impédance et finalement le couplage sonde-sonde et sonde-substrat.

Mots-clés: Caractérisation, Lignes de transmission, Terahertz, Ondes millimétriques, Calibrage sur silicium, MOSFET sur FDSOI

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General Introduction

This thesis aims to establish a high-frequency characterization methodology for advanced MOS transistors, specifically those of the FD-SOI technology from STMicroelectronics. The final goal is to use these characterization results for electrical compact modelling, allowing for precise predictions of electronic system characteristics in the THz frequency range.

Thesis context

Silicon bipolar and CMOS technologies have been recognized for their abilities in millimeter-wave applications, making them good candidates for circuit realization in the THz domain [1]. Among them, the "Fully-Depleted-Silicon-On-Insulator" (FD-SOI) technologies developed from the 28nm node [2] offer promising performances for transition frequencies (f_T) and maximum oscillation frequencies (f_{MAX}) beyond 300 GHz [3], and even more for the most advanced nodes [4] [5]. At the same time, the development of millimeter-wave circuits is booming, with realizations at ever higher frequencies, some of which go beyond 100 GHz [6] [7] [8].

To enable the design of circuits operating at millimeter-wave frequencies, an accurate modeling of FD-SOI transistors is essential. The first step has been taken with the development of compact models that can reproduce transistor characteristics in all operating regimes. These models have been validated for RF and millimeter-wave applications, but further development and validation are needed for frequencies beyond 100 GHz to support emerging applications at these frequencies. The main objective of this thesis is to provide reliable measurements in these frequency bands to fulfill this need.

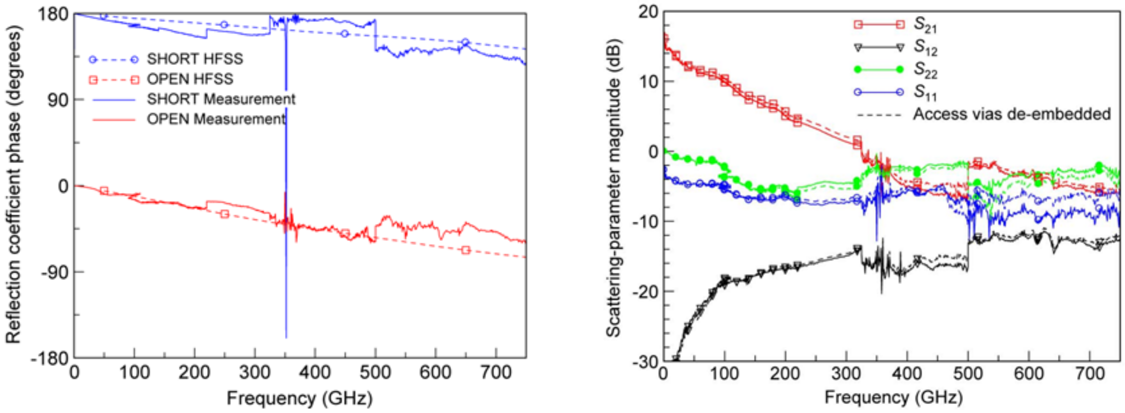


Figure 1: NIST (National Institute of Standards and Technologies, USA) measurement of (a) the phase measurement and EM simulation of an open and a short, and (b) the S-parameter magnitude measurement of a transistor up to 750 GHz. [9]

Currently, the THz domain is seen as a new scientific El Dorado and remains largely unexplored. For several decades, the Sub-THz part of the spectrum (100 GHz to 500 GHz) has only been used in niche applications and fundamental research. The availability of new semiconductor technologies such as FD-SOI offering components operating close to THz now allows approaching mass markets in areas such as:

- very high-speed and short-distance wireless communications,
- security and anti-collision automotive radars,
- medical and pharmaceutical biology as well as high-resolution imaging.

Currently, "classical" S-parameter measurements are limited to frequencies below 110 GHz, which is insufficient for validating electrical compact models necessary for the design of Sub-THz circuits and systems. Up to 110 GHz, various calibration and de-embedding methods (removal of parasitic elements surrounding the transistor) have been widely studied and published by the scientific community and no longer present major difficulties [10] [11] [12]. However, only few laboratories are equipped with measurement benches up to 220 GHz, or even 325 GHz. Work on the analysis of these measurements is rare [13], and there remain large uncertainties and a need for validation of these measurements through electromagnetic simulation, in particular. Indeed, measurements beyond 110 GHz are performed in multiple bands, each band requiring the use of different millimeter probes and heads. Thus, combining each measurement can introduce discontinuities, as illustrated in Figure 1 (excerpt from [9]). To mitigate these discontinuities, it is possible to use a dedicated calibration kit using inverted microstrip lines, gold contacts, and a dielectric suitable for high frequencies such as benzocyclobutene (BCB). Despite the precautions taken and the experience of the experimenters, the discontinuities remain significant for various reasons:

- calibration error due to poor probe placement, both in terms of contact quality [14] and X or Y position error [15],
- different coupling between the probe and the substrate in each band because each probe has a different geometry [16],
- impact of coupling with neighboring structures [15],
- drift of the measuring instrument during the characterization campaign,
- limitation of the TRL calibration method, which does not take into account cross-talk [17] and which, moreover, varies depending on the probe geometry.

Work Description

The description of the thesis project is part of the ongoing research activities carried out by the MODEL team of IMS for many years. The focus of this research is on the development of high-frequency characterization techniques [18] [19] [20] and compact modeling of transistors [21]. It also aligns with the crucial objective of increasing frequency and IMS's participation in the European H2020 projects. The research presented herein is based on state-of-the-art equipment, thanks to the significant investment made by IMS in 2015 and 2018 (>700,000 €) as part of the regional projects SUBTILE and FAST. Moreover, these research activities are carried out in collaboration with STMicroelectronics within the IMS/ST joint laboratory.

The characterization work aims to develop methods for measuring “on-wafer” S-parameters up to 500 GHz, using the measurement bench shown in Figure 2. To make the measurements

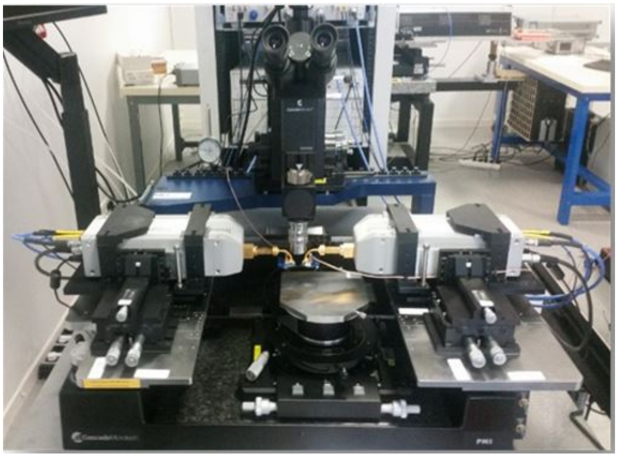


Figure 2: Measurement bench of the NANOCOM platform, operating up to 500 GHz.

repeatable and usable for industry, especially for compact modeling of devices, the main challenges are:

- mastering the quality of the contact between the measurement probe and the aluminium contact pad;
- positioning the measurement reference plane as close as possible to the intrinsic region of the transistor;
- quantifying the measurement uncertainty associated with probe positioning errors;
- mitigating the impact of adjacent structures, whose influence increases with frequency [15];
- better understanding and mitigating the signature of parasitic couplings between the probes and the environment of the measured device.

Although some aspects of the research have already been explored and have produced results [15] [20] [22] [23], it is necessary to deepen the ongoing analyses in order to clarify the measurement methodologies and design rules for the test structures to be implemented. Thus, the research work aims to provide answers to essential points in an industrial characterization context, such as:

- the optimal design of test structures to mitigate (or minimize) the effect of probes on the measurement of transistors,
- the benefits of using thick metals and/or large inter-metal thicknesses for test structures, or highly resistive substrates,
- the need (or not) to perform silicon calibration for each measured chip,
- the possibility of eliminating the de-embedding step by using a calibration method that brings the reference planes close to the transistors,

To attain these objectives, a number of topics are addressed during the thesis which are described in detail in three chapters. The chapters are briefly described below.

After a short introduction to the MOS transistors on 28 FD-SOI technology from STMicroelectronics, the first chapter is mainly dedicated to the challenges of RF measurements. First, the available hardware is described including the probe stations and the measurements benches for the four different frequency bands. A focus is given on the probe tips which are different for each frequency band and thus may introduce frequency band specific coupling. Second, the pros and cons of two standard calibration methods (SOLT and TRL) are discussed. Moreover, on-wafer calibration is compared to off-wafer calibration. For on-wafer calibration, TRL is the method of choice. But applying TRL on-wafer calibration implies the need for impedance correction. This topic is also described. In a third part, the different de-embedding procedures are reviewed. In the fourth section, an innovative concept based on electromagnetic simulation is introduced. Indeed, EM simulation allows us to decouple proven phenomena from measurement uncertainties and therefore better understand the effects at play. The simulation methodology used takes into account a part of the measurement system, at least up to the probes, and will clarify one by one each of the points mentioned above, while eliminating the uncertainty associated with the measurement. The first chapter ends with a state-of-the-art section on calibration procedures and de-embedding methodologies of RF transistors in the millimeter wave and sub-millimeter wave frequency ranges.

The second chapter is dedicated to the characterization and EM simulation of the "Run1" test-structures. Indeed, during the thesis work two different Si-hardware with different test-structures have been characterized and designed whereas the design concerns only the second "Run". After a detailed description of the test-structures including layout and cross-section analysis, the intrinsic EM simulation of the test-structures is presented. The issues of the presence of the dummies near the lines is analyzed and its impact on the characteristic impedance investigated. Then, the transistor measurements (DC and RF) are presented. This part is followed by the description of the small-signal equivalent circuit and the extraction procedure of the associated model parameters. A comparison of the small-signal simulation results with respect to measurements up to 500GHz is given. Afterwards, in order to assess possible measurement issues, a comparison of the measurement results with EM simulation and transistor model simulation is provided. Next, TRL measurement results are compared to measurements carried out with SOLT calibration. Finally, the effect of the RF probes used for measurement is examined. This chapter ends with an analysis of the drawbacks and limitations of "Run1".

The third chapter is dedicated to the design and analysis of the "Run2" test-structures. As concluded from the previous chapter, the existing "Run1" test structures for on-wafer TRL calibration possess several disadvantages. This has necessitated the development of improved test structures. In this chapter, we present different flavors for the design of the new TRL test structures that can overcome the difficulties encountered previously. Indeed, four different calibration kits have been designed and are explained in detail. To truly assess the intrinsic behavior of the test-structures, an EM simulation is carried out. Afterwards, the measurement results of the transistor are presented and compared to the full EM simulations using the RF probe models. This analysis is completed by adding a comparison with EM simulation with quasi-ideal probes. In order to overcome the inability of TRL to calibrate accurately in the presence of probe coupling (probe-to-probe together with probe-to-substrate), On-wafer SOLT calibration up to 220 GHz has been employed to further improve the accuracy of the calibration. Finally, a detailed comparison is made between the four differently designed calibration kits and the best-in-class kit is designated. The chapter ends with the presentation of very recent results obtained through the use of new probes having a very different probe geometry.

Chapter 1

Background Theory and Literature Review

1.1 28FD-SOI

As devices are scaled down as per Moore's law, the traditional bulk transistors encounter several limitations, the most important one being the increase in leakage current resulting in higher power consumption [24]. Moreover, from the 40 nm technology node and below, the electrostatic control of the transistor channel becomes more difficult [3]. This has led to the advent of new transistor architectures and new materials that enable further scaling down. Fully Depleted Silicon On Insulator, or FD-SOI, is a planar process technology that is a variant of silicon-on-insulator (SOI) technology [25]. The SOI wafer is fabricated using the Smart Cut process, the main steps of which are represented in Fig. 1.1. FD-SOI relies on two primary innovations. First, an ultra-thin layer of insulator, called the buried oxide, is positioned on top of the base silicon. Then, a very thin silicon film implements the transistor channel. As a result of the thin layer, there is no need to dope the channel, thus making the transistor Fully Depleted [26]. In the 28nm node, the transistor has an ultra thin conduction layer (7 nm) on top of a 25 nm insulation layer of buried oxide [7]. This technology is also called Ultra Thin Body and Box (UTBB).

Figure 1.2 shows a comparison of bulk transistor and FD-SOI transistor. In a traditional bulk CMOS transistor, the influence of source and drain junction diodes on the device electrostatic is such that the electrons can move from the source to drain even when the transistor is off,

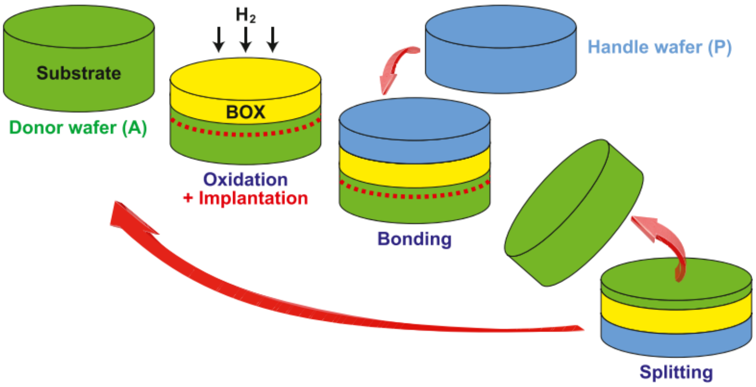


Figure 1.1: Smart Cut process for fabrication of SOI wafer [27]

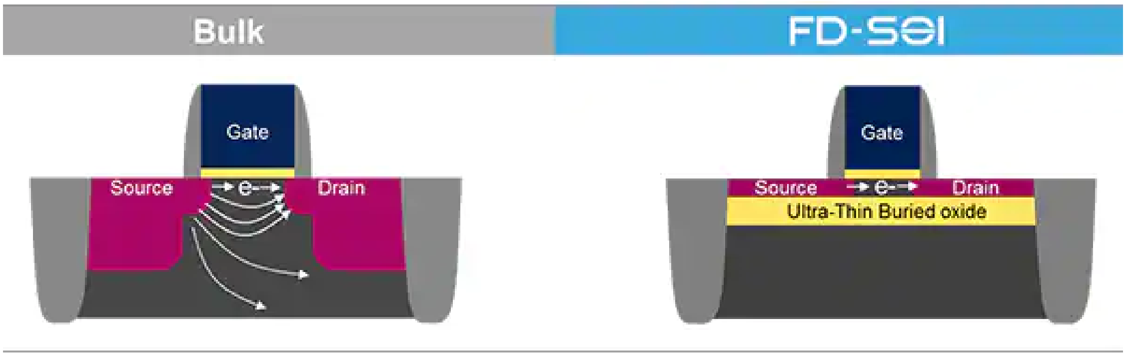


Figure 1.2: Bulk CMOS vs FD-SOI (Source: STMicroelectronics)

thereby resulting in a leakage current. In the FD-SOI transistor, most of this leakage is cancelled due to the thin conduction layer and the presence of the buried oxide layer (BOX). Indeed, as a result of the 7nm thickness, the SOI channel presents good Short Channel Effect (SCE) control that allows to decrease the physical gate length down to 24nm while keeping the same leakage as the bulk transistor with a longer gate length [2]. Other advantages of FD-SOI are total dielectric isolation, lower noise variability, and lower parasitic capacitance towards the substrate due to the BOX insulation. Moreover, very fast transistors are possible in this technology due to its deep sub-micron lithography [3].

Another important characteristic of the FD-SOI technology is the possibility of Body Biasing. This is an effective feature that can control the threshold voltage (V_t) of the transistor. This is made possible by polarizing the substrate situated below the device. This is similar to the body bias in bulk technologies, the difference being that the threshold voltage variation is limited to a few tens of millivolts in bulk devices, due to the inevitable junction diodes, whereas it can be much larger in FD-SOI. Two types of transistors are available based on their V_t [28][3],

- RVT are the regular V_t or standard V_t devices. Here V_t modulation through body biasing is possible by applying reverse body biasing (RBB), with the effective magnitude of biasing voltage ranging between 0 and 3V.
- LVT are the low V_t devices. They are also known as "flipped well" devices, because the NMOS devices lay on a N-type well and PMOS devices lay on a P-type well, which reduces their threshold voltage by roughly 80 mV compared to RVT ones. LVT devices support forward body biasing (FBB) to control the V_t, with an effective body voltage variation of approximately 0 to 3 V. FBB has the advantage of lowering the V_t, that enables the transistor to be switched faster. Therefore, LVT devices are used in the design of high speed circuits such as in digital applications for High-Speed Flip-Flops [28].
- Remark: Both body biasing options (RBB and FBB) are available in theory for both flavours (RVT and LVT). The limitation of the biasing range is due to the junction diodes of the wells.

FDSOI transistors obey the same equations as bulk MOSFETs. In strong inversion, the drain current I_D is [27],

$$I_D = \frac{\mu_{eff} C_{ox} W}{L} \cdot \left(V_{FG} - V_{TF} - \frac{n V_D}{2} \right) V_D \tag{1.1}$$

where,

Table 1.1: Comparison of FoM of different technologies

	$f_T(GHz)$	$f_{MAX}(GHz)$
28nm FDSOI [29]	310	330
22nm FDSOI [30]	332	435
22FFL FinFET [31]	300	450
28nm HKMG [32]	310	161
55nm BiCMOS [33]	326	375

V_{FG} is front gate voltage
V_D is drain voltage
V_{TF} is front channel threshold voltage
μ_{eff} is effective mobility
n is body factor
L is effective value of channel length
W is effective value of channel width
C_{ox} is the gate-oxide capacitance

At saturation, $V_D \geq V_{Dsat}$, then

$$I_{D_{sat}} = \frac{\mu_{eff} C_{ox} W}{L} \cdot \frac{(V_{FG} - V_{TF})^2}{2n}, \quad \text{where} \quad V_{Dsat} = \frac{V_{FG} - V_{TF}}{n} \tag{1.2}$$

In the linear region of operation, equation 1.1 becomes,

$$I_D = \frac{\mu_{eff} C_{ox} W V_D}{L} \cdot (V_{FG} - V_{TF}) \tag{1.3}$$

In subthreshold and linear regions, the current varies exponentially as:

$$I_D = I_0 \exp\left(\frac{q(V_{FG} - V_{TF})}{nkT}\right) = I_0 \exp\left(\frac{2.3(V_{FG} - V_{TF})}{SS}\right)$$
$$\text{Subthreshold Swing,} \quad SS = 2.3n(kT/q) \tag{1.4}$$

This work is based on the 28nm FD-SOI technology of STMicroelectronics. This technology enables fast switching in the LVT configuration with FBB. These have a maximum reported values of f_T/f_{MAX} of 310/330 GHz [29] and find several applications in the RF and millimetre wave frequencies. Table 1.1 makes a comparison of 28 FD-SOI technology with other technology devices in terms of its RF Figure of Merits (FoM).

1.2 RF Measurements

Before digging deeper in the RF measurements domain, a succint review of the basics is presented. RF measurements involve determining the S-parameters of an RF device. This is realised using a Network Analyzer (NWA), also known as Vector Network Analyzer (VNA), which works by measuring the magnitude and phase of the transmitted and reflected power at two ports. A VNA mainly consists of an RF synthesizer, an S-parameter test-set and control and display units. The signal from the synthesizer is fed to the test-set which acquires the incident and reflected power at the Device Under Test (DUT) at both ports. The block diagram of the S-parameter test-set is represented in Fig. 1.3 [34]. The test-set has an RF input receiving signal from the RF synthesizer and a PIN switch that directs the signal to forward or reverse directions. R represents the reference signal, in forward mode (RF input switched to port 1), A the reflected signal at port 1 and B the signal transmitted from port 1 to port 2, where as in reverse mode mode (RF input switched to port 2), B the reflected signal at port 2 and A the signal transmitted from port 2 to port 1. Within the test-set, there are also directional couplers to detect the incident and reflected waves at the DUT. These detected signals are further analyzed by downconverting it to IF signals.

The S-parameter test-set can be of two types: 3-sampler or 4-sampler. Ina 3-sampler VNA, the reflected signal is coupled out before the switch and hence the switching errors are not considered in the calibration. An additional correction step is necessary to account for the switching error. For this, specific measurements are necessary (incident and reflected powers to port 1 and 2). On the other hand, in a 4-sampler VNA, the switching error is eliminated due to the architecture of the test-set. It allows a better calibration , since the reference signals R are taken after the switch. This is significant for frequencies above ∼20 GHz [34]. The block diagram in Fig. 1.3 represents a test-set including 4-samplers.

In addition to these, VNAs also include bias TEEs, which set the operating point for the measurement of active components. Bias TEEs are composed of an inductor and a capacitor as shown in Fig. 1.4 [34].

1.3 Measurement setups

In this work, measurements have been performed from 1 GHz to 500 GHz in 4 frequency bands, namely, (i) 1-110 GHz, (ii) 140-220 GHz (iii) 220-330 GHz (iv) 325-500 GHz.

1.3.1 Probe stations

For the measurements in the band 1-110 GHz, the setup consists of the N5250A module (Fig. 1.5) from Agilent Technologies that operates from 10 MHz to 110 GHz [35]. This network analyzer includes the microwave network analyzer E8361A PNA that delivers signals from 10 MHz to 67 GHz, millimetre-wave test heads that provide signals from 67-110 GHz, millimetre-wave test set controller that drives these test heads, the combiner assembly containing the 67 GHz coupler and a combiner that combines the signal from the PNA with that from the mm-wave test heads. Bias tees are added to this for enhanced measurement stability. The specifications of E8361A PNA are given in Table 1.2 [36] [37].

For the higher frequency bands, the Rohde & Schwarz ® ZVA24 VNA [38], which operates from 10 MHz to 24 GHz, is used. The photograph of the probe station is shown in Fig. 1.6

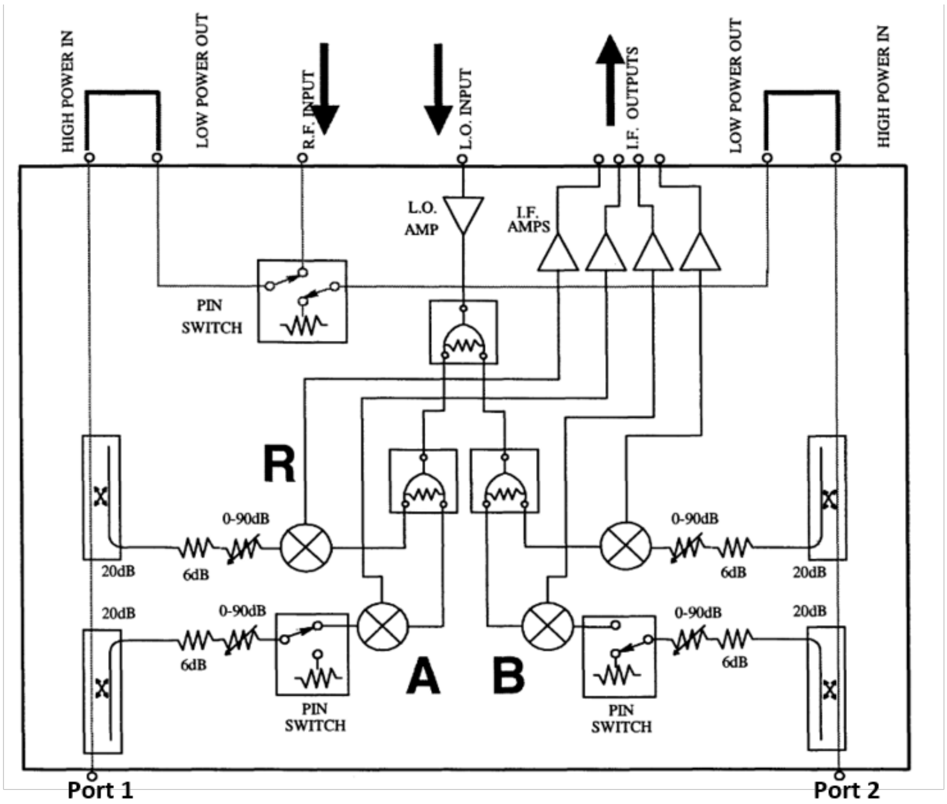


Figure 1.3: Block diagram of VNA S-parameter testset [34]

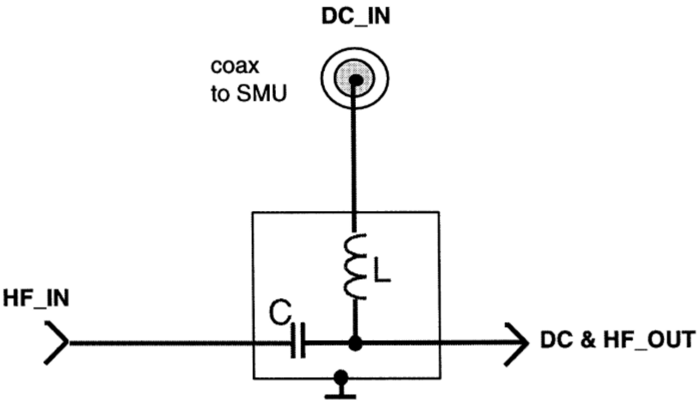


Figure 1.4: Bias TEE circuit used in VNA [34]

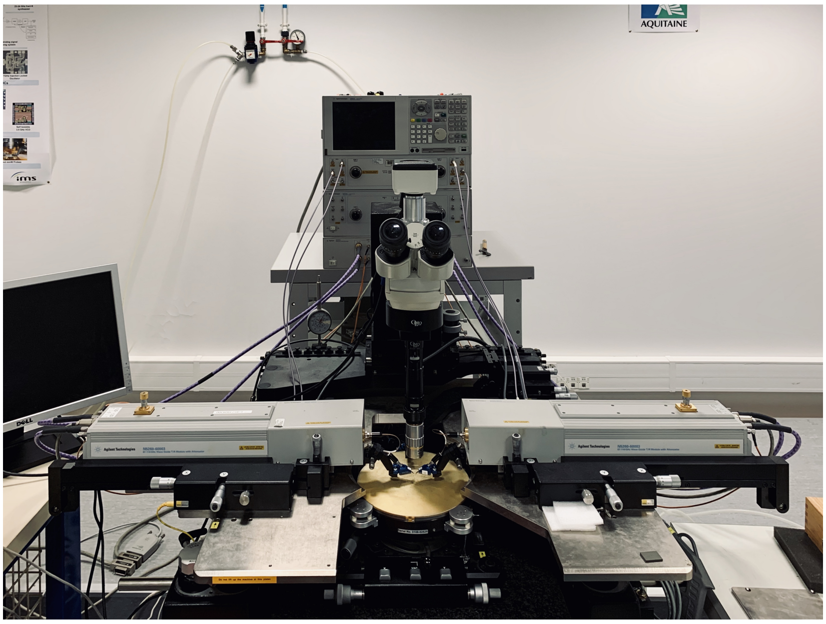


Figure 1.5: Probe station for measurement from 1-110 GHz using N5250A network analyzer

To perform measurements in each band, namely, 140-220 GHz, 220-330 GHz and 325-500 GHz, the frequency extenders ZC220, ZC330 and ZC500 [39] [40] are added respectively to the VNA. The performance specifications of the VNA and frequency extenders are listed in Table 1.2 and Table 1.3. It is observed from Table 1.2 that the ZVA has much better performance, especially regarding the dynamic range which is 30dB higher. This is a tremendous number. The reason is mainly due to the fact that the ZVA has been acquired by the University of Bordeaux in 2015, while the PNA was bought in 2007. That being said, making on-wafer measurement showing a 100dB dynamic range is extremely challenging due to the noise introduced by the on-wafer connections. In the same vein, we recognize superior performance concerning directivity, source match and load match for the ZVA, but these characteristics are directly accounted for in the calibration procedure. The same comment holds for the reflection and transmission tracking. Summing up, the two measurement instruments make it possible to correctly obtain the on-wafer transistor characteristics. There is no fundamental limitation due to the available hardware. Of course, having a state-of-the-art VNA on hand makes for less noisy and smoother measurements, but our somewhat older measuring equipment always gives correct results.

Table 1.3 summarizes the specifications of the frequency extenders used for the measurements. Each frequency range has its own waveguide design due to the different wavelengths. It is observed that the dynamic range, in particular the output power decreases significantly with increasing frequency. For our applications, this is not an issue, as we try to characterize the transistor under small signal operation. Source match and directivity are also decreased, especially compared to the ZVA alone, but as already mentioned, these characteristics are taken into account by the calibration.

1.3.2 Probe types

In the first frequency band of 1-110 GHz, measurements were performed using RF probes from two different manufactures, GGB Industries Inc., and Cascade Microtech Inc. Picoprobe ® Model 110H RF probes [41] from GGB Industries Inc. operate from DC to 110 GHz with a

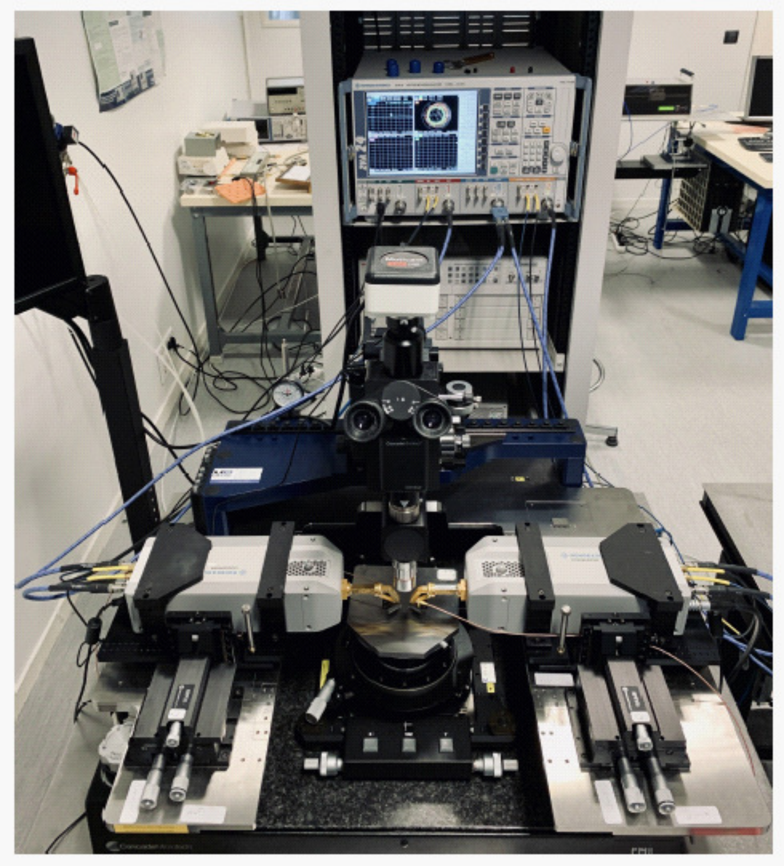


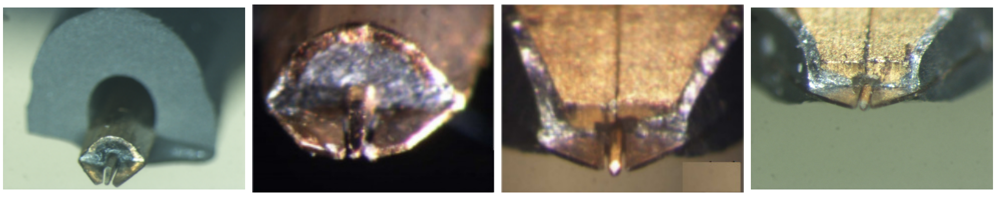
Figure 1.6: Probe station used for measurements from 140 - 500 GHz

Table 1.2: Specifications of VNA

	E8361A PNA	**ZVA24**
Test Port Connector	1.85mm	3.5mm
Dynamic Range (dB)	>94	>125
Directivity (dB)	>34	>40
Source Match (dB)	>34	>36
Load Match (dB)	>37	>40
Reflection Tracking	<0.09	<0.1
Transmission Tracking	<0.144	<0.1

Table 1.3: Specifications of Frequency Extenders Used for Measurements

	ZC220	ZC330	ZC500
Frequency Range	140 to 220 GHz	220 to 330 GHz	330 to 500 GHz
Waveguide Designator	WM-1296	WM-864	WM-570
Dynamic Range	>100dB, typ. 115dB	>100dB, typ. 115dB	>85dB, typ. 100dB
Output Power	>-2dBm, typ. +1dBm	>-10dBm, typ. -7dBm	>-15dBm, typ. -11dBm
Source Match	>25dB	>20dB	>20dB
Directivity	>25dB	>20dB	>20dB



(a) 1-110 GHz (b) 140-220 GHz (c) 220-330 GHz (d) 325-500 GHz

Figure 1.7: Photographs of Picoprobes for measurements from 1-500 GHz

maximum insertion loss of 1.5dB. This probe has a coaxial cable design [42]. An insulating layer separates the inner conductor and outer conductor. The miniature coaxial transmission lines having a center conductor diameter of 0.2mm carry signals to and from test instruments. The coaxial cables use a 1mm connector for connection to the instruments at one end. At the other end, the centre conductor extends beyond the cable shield to form a conical point for connection to the RF test pads. For the measurements in this work, two types of GSG (Ground-Signal-Ground) Picoprobes with a pitch of 100 µm and a pitch of 50µm have been utilized. A photograph of the Picoprobe is shown in Fig. 1.7a.

Infinity probes [43] [44] by Cascade Microtech Inc. were also used for measurements in this frequency band (photograph in Fig. 1.8). These probes based on the thin film technology, consists of a microstrip line on a flexible polyimide membrane substrate [45]. The microstrip line transmits the signal from the coaxial conductor to the device through Nickel alloy probe tips. Also used in this band are the improved InfinityXT™by Cascade Microtech Inc.[43]. Here only probes with a pitch of 50 µm are available in the lab. These probes having a very different geometry (see Fig. 1.9) as well as a different connection from the coaxial endpoint to the probe tips which greatly influences the EM field. Moreover, these have better tip visibility for enhanced placement accuracy and repeatability [46].

Cascade Microtech also provides Infinity probes [43] [45] in the WR5 (140-220 GHz) frequency band. These waveguide based probes with membrane tips claim to significantly reduce stray fields in the tip area [47]. In fact, waveguide probes support transverse electric (TE) and transverse magnetic (TM) mode of wave propagation, whereas coaxial probes support transverse electromagnetic (TEM) wave propagation mode [48].

In the last two bands (220-330 GHz, 325-500 GHz), Picoprobe RF probes [49] [50] from GGB Industries Inc. were used (Fig. 1.7c and Fig. 1.7d). These have a coaxial design with Beryllium Copper probe tips. Table 1.4 makes a comparison of the different RF probes used for the different frequency ranges. It is observed that for frequencies higher than 220 GHz, probes with 50

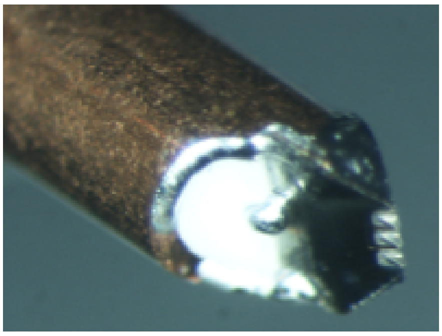


Figure 1.8: Photograph of Infinity probe for 110 GHz measurements

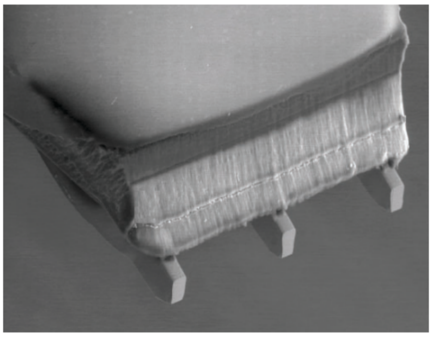


Figure 1.9: SEM image of Infinity XT for 110 GHz measurements

Table 1.4: Comparison of RF Probes

	Picoprobe110	Infinity110	InfinityXT	Infinity220	Picoprobe330	Picoprobe500
Frequency (GHz)	1-110	1-110	1-110	140-220	220-330	325-500
Design type	coaxial	thin film technology	coaxial	waveguide	coaxial	coaxial
Probe tips	Berylium-Copper	Nickel alloy	Rhodium	thin film membrane	BeCu	BeCu
Probe pitch (μm)	100	100	50	100	50	50
Insertion loss (dB)	<1.5	<1.4	<2	<5.2	3	4
Return Loss (dB)	<15	<20	<20	<13	15	15

µm pitch are mandatory. The probe tip material is Beryllium-Copper for the Picoprobe probes whereas for Infinity probes the material is different for each frequency band. Furthermore, it can be said that for higher frequencies the probes get less ideal showing increasing insertion loss and less return loss.

1.4 Types of Calibration

1.4.1 Short-Open-Load-Thru (SOLT) Calibration

The SOLT is a calibration method that uses the 12-term error model. In a three sampler VNA the error model is represented separately for the forward and reverse direction due to the effect of switching. There are 6 terms each in the forward and reverse directions making a total of 12 error terms. The complete error model is shown in Fig. 1.10. The error terms in the forward direction are defined as follows using the notations from [51]:

$$\begin{aligned}
E_{DF} &= e_{00} = \text{Directivity} \\
E_{SF} &= e_{11} = \text{Source Match} \\
E_{RF} &= (e_{10}e_{01}) = \text{Reflection Tracking} \\
E_{XF} &= e_{30} = \text{Crosstalk} \\
E_{TF} &= (e_{10}e_{32}) = \text{Transmission Tracking} \\
E_{LF} &= e_{22} = \text{Load Match}
\end{aligned}$$

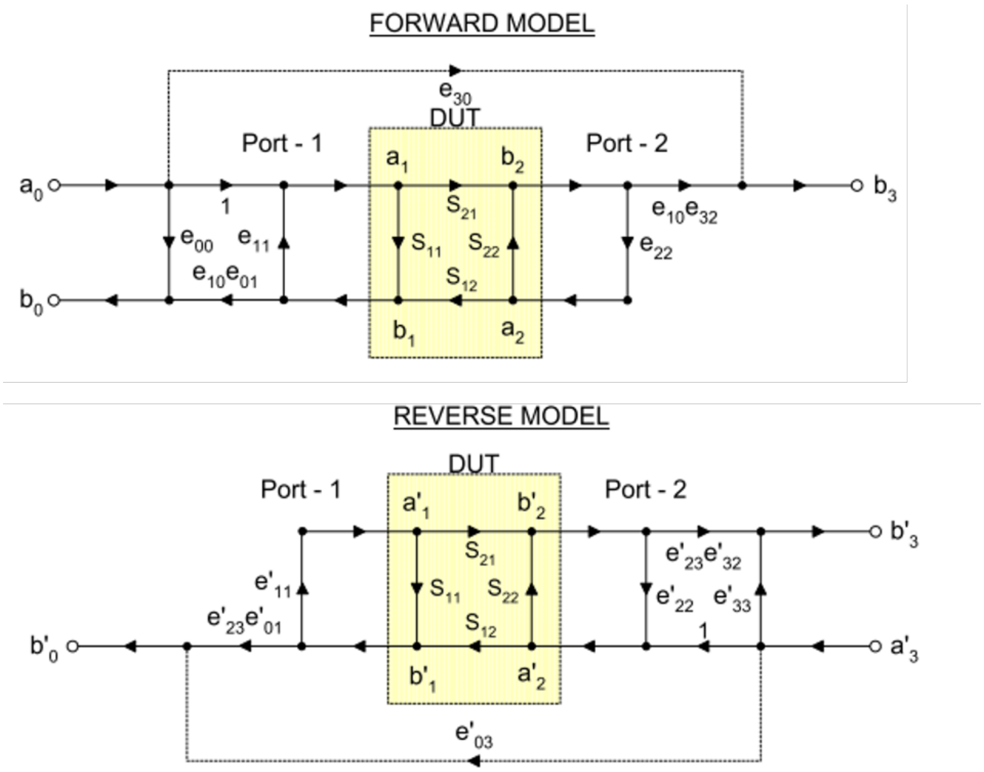


Figure 1.10: 12-term error model of network analyzer [52]

Similarly, we also have another 4 error terms, $E_{DR}, E_{SR}, E_{RR}, E_{XR}, E_{TR}$ and E_{LR} in the reverse direction.

SOLT calibration requires three reflection standards (Short, Open, Load) at each port and one transmission standard (Thru). All electrical characteristics of standards must be completely known [53]. It can be performed on-wafer or off-wafer. The off-wafer SOLT, more commonly called the ISS SOLT, uses a dedicated substrate (often called ISS or Impedance Standard Substrate), on which the calibration standards are made. The substrate is usually alumina on which the standards are fabricated using conducting lines. The contact pads are made of gold which enables very stable and repeatable contact with probes. Fig. 1.11 shows the map of the ISS substrate [54] as provided by Cascade Microtech. CS-5 (Fig. 1.12) is another calibration substrate provided by the manufacturer GGB industries Inc. [55], which is intended to be used during measurements with their Picoprobe probes. The calibration coefficients are also provided by the manufacturer. However, accuracy of these coefficients depend on the accuracy of the standards, which unfortunately deteriorates with frequency [56] and become frequency dependent at higher frequencies. For example, for GGB, the standard parameters are not probe geometry or pitch dependent, thus they are an approximation only.

Another disadvantage with the off-wafer SOLT calibration is that the substrate of calibration standards is very different from the BEOL (Back-End-Of-Line) of Silicon wafers. This change of environment is expected to cause a difference in the electromagnetic field distribution in the calibration substrate and the Device Under Test (DUT). In other words, the substrate to probe coupling is different in both cases, resulting in a systematic error [16]. When performing a SOLT calibration using a dedicated substrate, the reference plane of measurement is located at the probe tips (hence, it is also called probe tip calibration), which is not well-defined and somewhat approximate [57]. In fact, when defining a reference plane after calibration, the

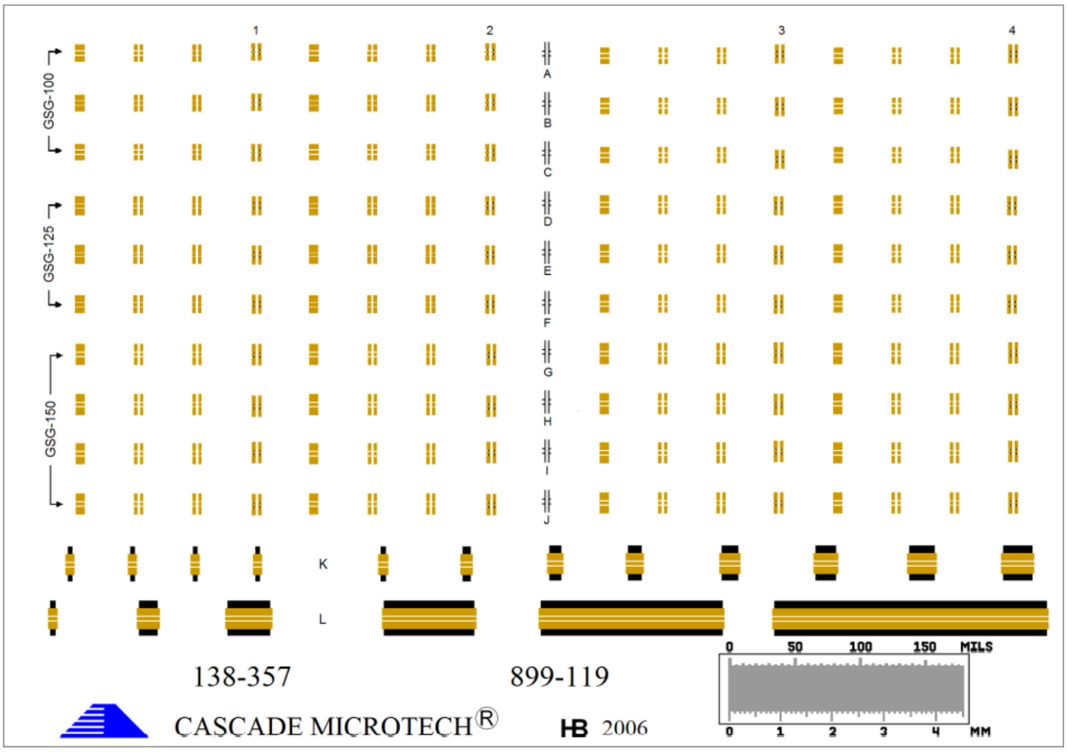


Figure 1.11: Calibration standards on ISS provided by Cascade Microtech (Form Factor) for use with Infinity probes [54]

transition between the reference planes (location where calibration ends and where the DUT begins) should be homogeneous. This cannot be guaranteed with off-wafer calibration due to the stray fields that are of course different when switching from off-wafer calibration to on-wafer calibration. Moreover, it has already been demonstrated in [58] that the uncertainty in probe positioning deteriorates the performance of SOLT calibration. Moreover, this probe contact is made with aluminium pads on the DUTs, and with Alumina pads on the calibration substrate, thereby resulting in different contact resistances in each case. As a consequence of these, it is observed in [20] that SOLT calibration does not provide reliable results above 200 GHz. In spite of these limitations, the SOLT is the more commonly used industry standard for device characterization, in view of the simplicity of the procedure and readily available calibration algorithms.

1.4.2 On-wafer TRL

The limitations of off-wafer calibration techniques, especially at higher frequencies, have led to the exploration of on-wafer calibration methods. The TRL (Thru Reflect Line) [59] is a commonly used on-wafer calibration which is the focus of this thesis work. This uses an 8-term error model and has the advantage of not requiring all the standards to be ideal [56]. The 8-term error model is represented in Fig. 1.13. This model requires the measurement of two incident waves and two scattered waves and makes the following assumptions:

- the crosstalk or leakage is zero
- the switch of the VNA is perfect, which means that the port match is same in the forward and reverse directions

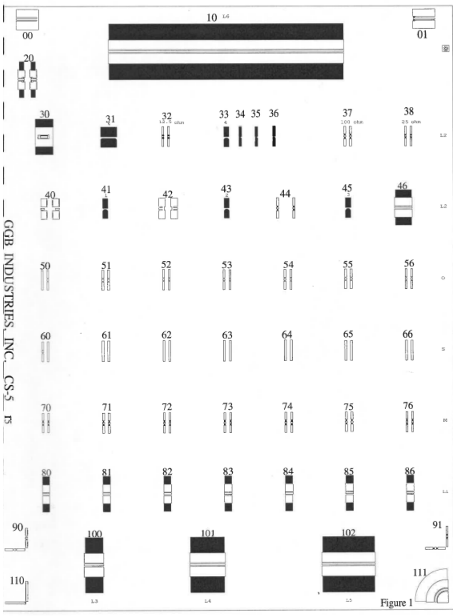


Figure 1.12: CS-5 Calibration substrate provided by GGB Industries Inc. [55]

The 8-term error correction can be achieved by considering the measured S-parameters as a cascade of the input error box (represented by its T-matrix, $\mathbf{T}_X$), actual S-parameters and the output error box ($\mathbf{T}_Y$). In terms of T-parameters, this can be written as [60],

$$\mathbf{T}_M = \mathbf{T}_X \cdot \mathbf{T}_{actual} \cdot \mathbf{T}_Y \tag{1.5}$$

The actual S-parameters are then calculated by inverse matrices,

$$\mathbf{T}_{actual} = \mathbf{T}_X^{-1} \cdot \mathbf{T}_M \cdot \mathbf{T}_Y^{-1} \tag{1.6}$$

TRL calibration method shifts the reference plane to a point after the RF pads, which means that the parasitic effects of the RF pads are removed as part of the error model, in addition to the effects of the measurement setup. This technique has very few systematic errors and thus makes TRL the calibration of choice for metrological applications [57]. In fact, the requirements about the knowledge of the calibration standards are not so stringent: For the thru and line standard, only the difference in length has to be known, and both standards should have the same characteristic impedance and should be symmetrical. For the reflect standard only the symmetry criterion has to be satisfied.

However, this method has a frequency limitation depending on the length of the LINE standard used. The maximum and minimum frequency for which the TRL calibration is valid are given by the equations 1.7 and 1.8 [61]. Thus it becomes necessary to have multiple lines in order to perform calibration for a wide frequency range. Another difficulty encountered with TRL calibration is obtaining repeatable good contacts with the aluminium RF pads [57]. A characteristic feature of TRL calibration is that the calibrated S-parameters have a reference impedance equal to the characteristic impedance (Z_c) of lines. This brings in the need for an additional step, the impedance correction, after TRL calibration in order to reference the S-parameters to the standard 50 Ω impedance.

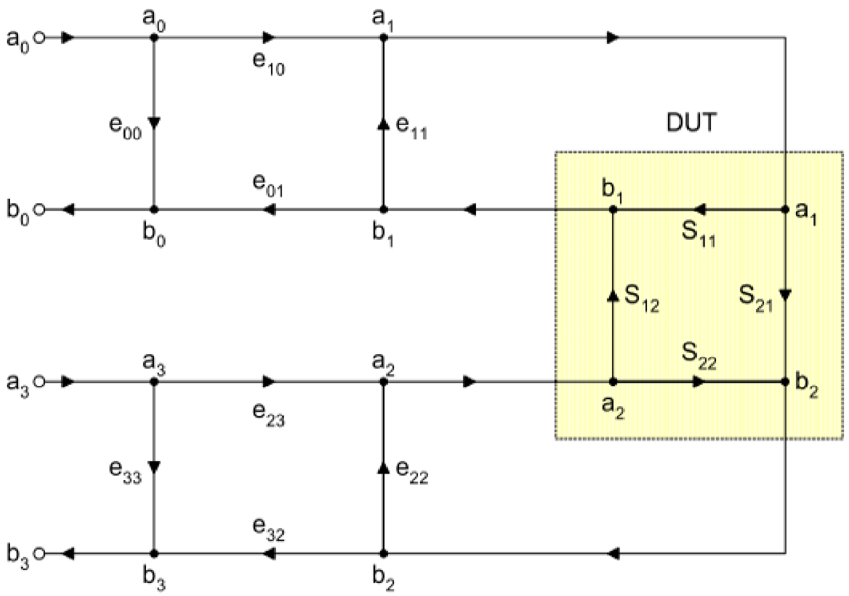


Figure 1.13: 8-term error model [52]

$$f_{min} = \frac{c}{20.(L_{line} - L_{thru})\sqrt{\epsilon_{r,eff}}} \tag{1.7}$$

$$f_{max} = 9 * \frac{c}{20.(L_{line} - L_{thru})\sqrt{\epsilon_{r,eff}}} \tag{1.8}$$

Impedance Correction

The characteristic impedance Z_c is often a complex quantity and frequency dependent, which makes it difficult to be accurately determined.

One of the methods to extract the characteristic impedance involves calculating Z_c from the knowledge of the propagation constant, γ of the transmission line [62]. The quantities γ and Z_c are related to the RLCG parameters of the transmission line as given by equations 1.9 and 1.10.

$$\frac{\gamma}{Z_c} = j\omega C + G \tag{1.9}$$

$$\gamma.Z_c = j\omega L + R \tag{1.10}$$

The resistance per unit length, R, the inductance per unit length L, capacitance per unit length C and the conductance per unit length G are unknown. When substrate loss is low and transverse currents in conductor are weak, G can be neglected [62] and it can be safely assumed that $G \ll \omega C$. Thus if C is known in equation 1.9, Z_c can be computed from γ. C can be approximated to C_0, the dc capacitance assuming perfect conductors since the dependence of C on frequency and conductivity is low. However, L and R strongly depend on the frequency and conductivity and hence using equation 1.10 to calculate Z_c leads to less accurate results [62].

Two different methods to calculate C of transmission line have been discussed in [63]. The first method this quantity is approximately calculated from the dc resistance of the transmission line R_{dc} as in equation 1.11.

$$C \approx \frac{1}{R_{dc}} Re\left(\frac{\gamma^2}{j\omega}\right) \tag{1.11}$$

The second approach discussed in [63] estimates the Z_0 from the reflection coefficient of a small resistive load. This method makes the assumption that the resistive load is real, constant and equal to its dc resistance. For a small lumped resistor at low frequencies, the equation 1.12 holds good.

$$Z\frac{1+\Gamma_{load}}{1-\Gamma_{load}} \equiv Z_{load} \approx R_{load,dc} \tag{1.12}$$

Here Γ_{load} is the measured reflection coefficient of the load and $R_{load,dc}$ is its dc resistance. Thus, using this in equation 1.9, we get

$$\mathrm{C}[1 - j(G/\omega C)] \approx \frac{\gamma}{j\omega R_{load,dc}} \frac{1+\Gamma_{load}}{1-\Gamma_{load}} \tag{1.13}$$

So, finally C can be computed as in equation 1.14 with the assumption that $G/\omega C < 0.004$.

$$C \approx \frac{\gamma}{j\omega R_{load,dc}} \frac{1+\Gamma_{load}}{1-\Gamma_{load}} \tag{1.14}$$

In both these methods, the line propagation constant, γ is computed from the T matrices of the Thru and Line standards as part of the TRL calibration algorithm.

Other methods discussed in [64] and [65] make use of on-wafer measurements to extract Z_0. Another method termed 'calibration comparison method' is detailed in [66] where two different calibrations are used to determine the characteristic impedance of the transmission line. It is also shown that this method is more accurate that any of the methods discussed above.

In this thesis work, the impedance correction after TRL calibration is performed using the reflection coefficient of resistive load [63]. Therefore, it requires an additional test structure, the Pad Load, which acts as the resistive load. The reflection coefficient (Γ_{load}) of the Pad Load is obtained from the measurements. These values are further utilised to calculate the line capacitance from equation 1.14.

1.5 Types of De-embedding

De-embedding is essential to shift the measurement reference plane to the actual device terminals situated below the BEOL at metal 1 (M1) level. This step is very critical in the millimeter-wave frequency range due to the size of the MOS transistor, which is several times smaller than the access lines. Hence, the S-parameters obtained after calibration include large parasitics due to the interconnects, which are removed by de-embedding. There are several methods of de-embedding discussed in literature. One of the simplest de-embedding methods that assumes a lumped circuit model for the parasitics is the Open-Short de-embedding [67] discussed in the

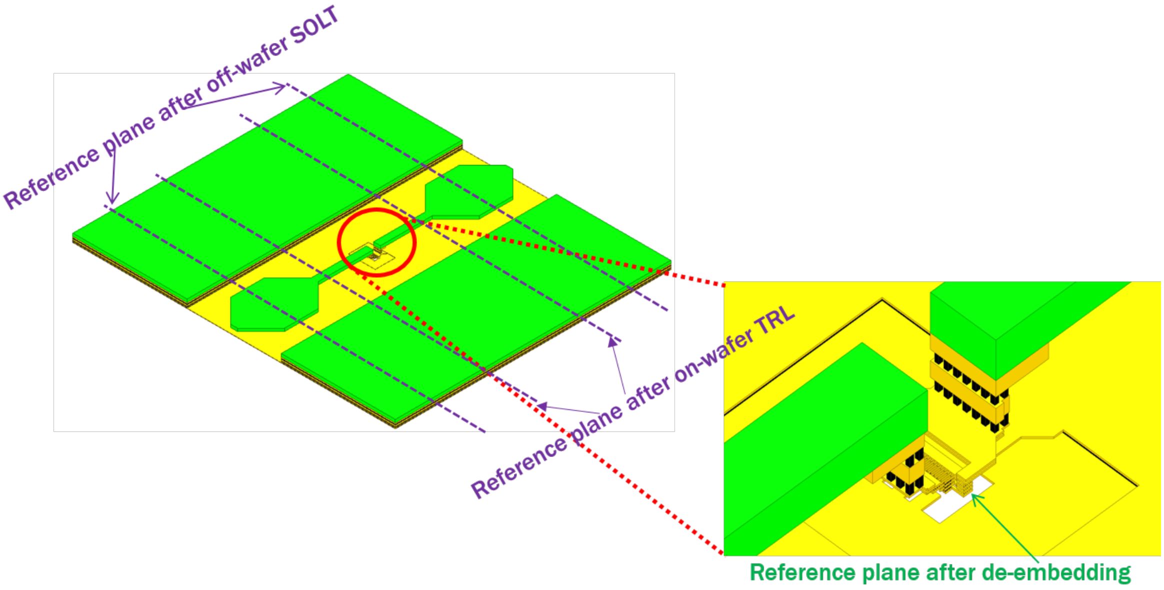


Figure 1.14: Figure showing the reference plane after each calibration and after de-embedding

succeeding section. However, this method results in over de-embedding at higher millimetre wave frequencies [68]. This due to the fact that on the Short structure, an Open de-embedding is performed. This seems to be correct except that, for the Open-structure, coupling effects exist between the input interconnect, the output interconnect and the source dangling leg. These parasitic capacitances are not present in the Short. Thus correcting the Short by the Open may introduce some over de-embedding. In order to eliminate the over or under de-embedding issues, a method using 4 dummmies is proposed in [68]. Three step and four step de-embedding methods using lumped models are discussed in [69] and [70] respectively. There also exists cascade methods that consider a distributed model for the parasitics such as L2L [71] and thru-halfthru-short [72] methods. Cascade de-embedding methods are also discussed in [73] and [74].

By setting the reference plane after calibration to the inner edge of the Pad-Open (as indicated in Fig. 1.14), the on-wafer TRL calibration removes the parasitic effects due to the RF probes and measurement instrument setup as well as the effects of the RF probe pads. In other words, TRL calibration shifts the measurement reference plane to the point after the probe pads. However, the reference plane after SOLT calibration is at the probe tips (see Fig. 1.14) and hence requires a de-embedding step that takes into account the pad parasitics as well. It is for this reason that we use a different method for de-embedding in each case. The reference plane after calibration and after de-embedding are shown in Fig. 1.14.

1.5.1 Short-Open De-embedding

De-embedding of the transistor using dedicated Short and Open dummies is the method used in this work for extracting the actual device S-parameters after TRL calibration. This method assumes a lumped model (see Fig. 1.15) for the parasitics to be removed (parasitics of the access line and the BEOL stack). The matrix manipulations involved in the removal of serial and parallel parasitic components are discussed in detail in [34]. In Short-Open de-embedding,

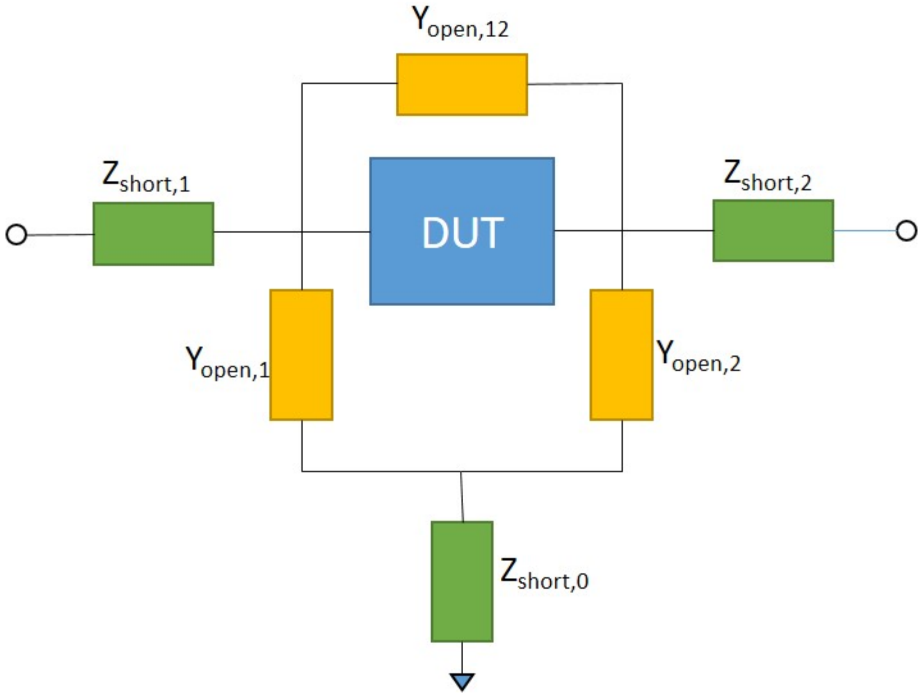


Figure 1.15: Lumped model of parasitics to be removed using Short Open de-embedding

the series impedances are first removed by subtracting the impedance of the Transistor Short from the calibrated DUT impedance and the Open dummy as in eqn. 1.15 and eqn. 1.16.

$$Z'_{DUT} = Z_{DUT} - Z_{Short} \tag{1.15}$$

$$Z'_{Open} = Z_{Open} - Z_{Short} \tag{1.16}$$

The shunt admittances are removed in the next step by subtracting the admittance of the Open dummy from the short de-embedded DUT as in eqn. 1.17 to get the devices parameters with the reference plane at the actual device terminals at M1.

$$Y_{Device} = Y'_{DUT} - Y'_{Open} \tag{1.17}$$

The lumped parasitic model for the access lines loses its validity as we go higher in the frequency range. However, this is not a cause of concern as the toolkit used for TRL calibration has the capability of moving the reference plane to any point on the access line, by adjusting the calibration parameters. This shift of the reference plane is intrinsically related to the TRL calibration, because one of the intermediate results of the TRL procedure are the parameters of the lines (Thru and Line) that serve for the calibration. Using the Line parameters, the reference plane is shifted to the end of the access line (top of the BEOL stack), so that the lumped model retains its validity.

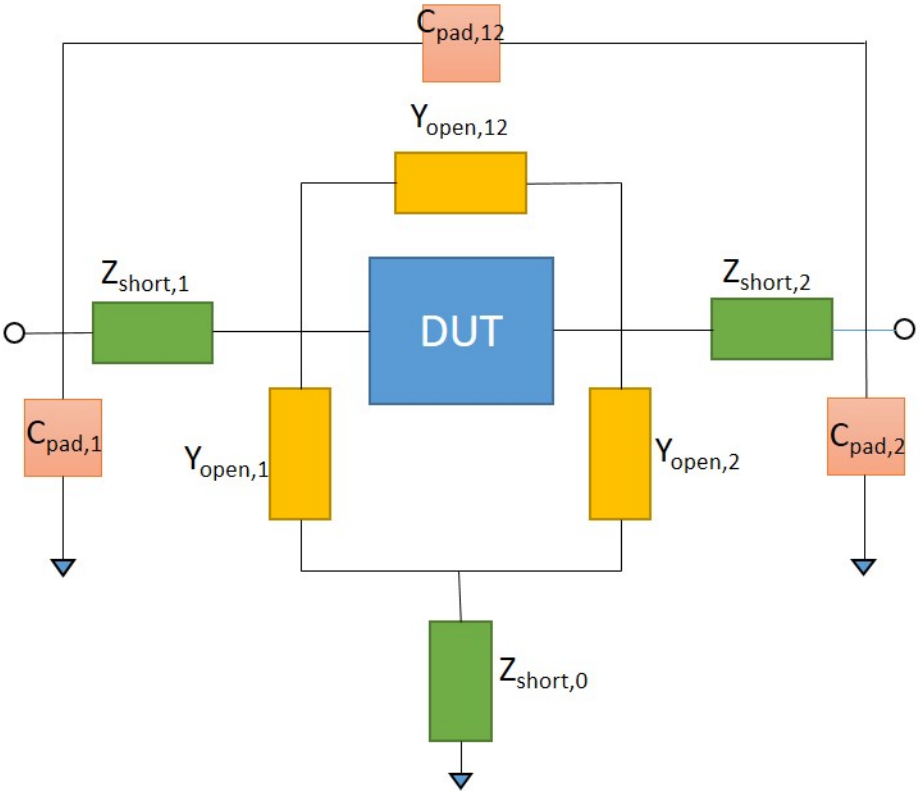


Figure 1.16: Parasitics model used for Pad Short Open de-embedding

1.5.2 Pad-Short-Open De-embedding

As discussed above and seen in Fig. 1.14, the de-embedding method after SOLT calibration should take into account the pad parasitics as well. This means that the Short-Open (SO) de-embedding method just discussed may not be ideal for SOLT, given that circuit model for parasitics after SOLT calibration looks like as in Fig. 1.16. It has been shown in [29] that the PSO de-embedding gives better results than transistor characterization using a standard 2-dummy method such as Open-Short, since it better accounts for the distribution of the capacitance between the pad and the terminating interconnects at the transistor's level. In the PSO method, an additional test structure, called the Pad Open, is first used to remove the parastic capacitances of the probe pads. After this step, the parasitics model looks similar to the one in Fig. 1.15 and can be followed by the Short Open de-embedding steps to obtain the actual device parameters.

1.6 Electromagnetic Simulations

Electromagnetic (EM) simulations have been conducted to corroborate the measurement results. The basic motivation for this approach lies in the fact that above 200 GHz the large dimensions of the RF probes, in comparison to the wavelength, lead to parasitic effects which affect the device under test. Since the measurement is influenced by the electro-magnetic coupling between the probe tip and the test structures on the substrate, as well as by the inter probe tips coupling, the standard on-wafer TRL calibration becomes imprecise. A method of simulating this influence by means of 3D electromagnetic simulations has been introduced by [75]

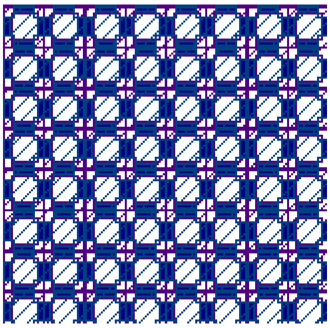


Figure 1.17: Meshed metal layers of the layout

for BiCMOS technologies and by [76] for gallium arsenide (GaAs) monolithic millimeter-wave integrated circuits. The EM-simulation tool used was Ansys HFSS, which is a commercial 3D FEM (Finite Element Method) solver which is utilized to achieve this. This software solves the Maxwell's equations using numerical methods to calculate the Electric and Magnetic fields at every point of the simulated structures.

To create the 3D model of each test structure, its corresponding layout (gds file) is first simplified. In the original layout, each metal layer has a meshed structure as in Fig. 1.17 in order to respect the density rules of the fabrication process. This is simplified by considering each metal layer to be a uniform or continuous structure, without any mesh. The simplification does not affect the electrical response of the structure [77] because the mesh openings are much smaller than the wavelengths of operation. This simplified layout file is directly imported into HFSS and each layer is mapped to its corresponding physical properties. The properties include the layer thickness, and the material used for the layer in the BEOL. The excitations or the input and output ports are specified by defining 'Wave Ports'. The direction of incident electric field at the port is defined by drawing an 'Integration line' between the ground and the signal conductors. The silicon substrate and the dielectrics surrounding the BEOL are also added to this with their corresponding dielectric constants. The entire structure is enclosed in an airbox which defines the area to be simulated. The faces of the air box are defined as 'Radiation Boundary', which creates an absorbing boundary condition with zero reflections. The meshing uses tetrahedral elements and is automatic. The analysis setup specifies the solution frequency/frequencies and defines the range for frequency sweep. After simulation, the S-parameters can be extracted.

All passive structures are simulated in this manner. However, HFSS cannot perform simulations of active devices like transistor. Therefore, an EM co-simulation is performed to simulate the transistor. This simulation method combines the EM simulation of the passive parts of the transistor with the simulation of the Small Signal Equivalent Circuit (SSEC) model of the transistor [78].

An overview of the different types of EM simulations performed in this work is briefly discussed below:

1. Intrinsic Simulations: The different test structures are imported into HFSS, but without the RF pads. In other words, the intrinsic test structures (with access lines) are simulated. This simulation provides an insight into the intrinsic behavior of the structure, without considering the effects of measurements or calibration. Fig. 1.18 shows the HFSS model for the intrinsic simulation of Transistor Open. The results of this simulation serve as a reference while analyzing the results of calibration.

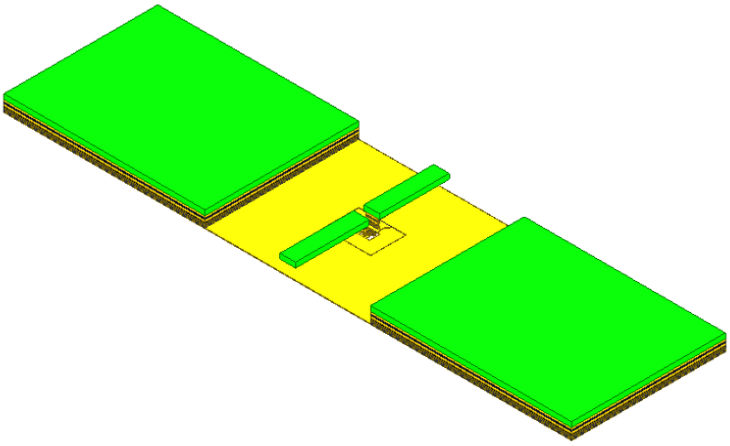


Figure 1.18: HFSS model for intrinsic simulation of Transistor Open

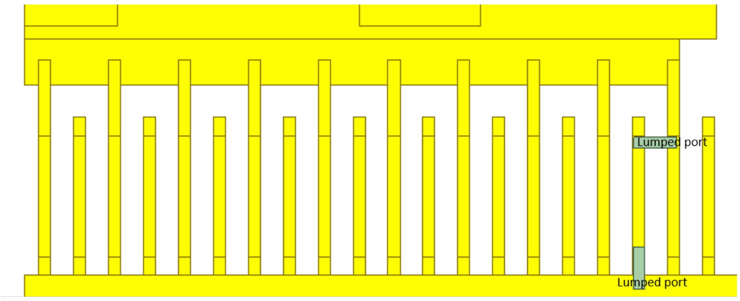


Figure 1.19: Lumped ports in HFSS for co-simulation of transistor

2. Intrinsic co-simulation: Here, a co-simulation of the transistor is performed, but again without the RF probes. To realise the co-simulation of the transistor, 2 small rectangles are drawn on the gate fingers of the HFSS model of Transistor Open as shown in Fig. 1.19 , which are then defined as ’Lumped Ports’ with 50 Ω characteristic impedance. This structure is then simulated in HFSS and the resulting S-parameters are combined with the transistor model parameters using IC-CAP software. This transistor co-simulation along with the intrinsic simulation of the Transistor Open and Transistor Short are used to study the effect of de-embedding without any effects of calibration. For an ideal de-embedding method, the de-embedded S-parameters should be identical to that of the SSEC model.

3. Co-simulation with probes: In this type of EM simulation, the complete TRL test structures (with RF probes pads and access lines) are simulated as in the real experimental scenario. 3D model of the RF probes (see Fig. 1.20) are created from the photographs or from tomographic images of the probes obtained through X-rays. The complete test structures, with the RF probes models placed on the probe pads are simulated. For the TRL standards and the passive test structures, a simple EM simulation is performed in this manner. For the transistor, an EM co-simulation is performed with the probe models. The S-parameters from these simulations serve as the raw data or uncalibrated data. These are equivalent to the uncalibrated measured S-parameters having the advantage that these data are not affected by measurement noise and drift, by contact uncertainty or by probe positioning error. This data is then treated using the TRL algorithm toolkit to obtain the TRL calibrated S-parameters. To extract the actual DUT S-parameters, a suitable de-embedding step is performed using the simulated data. This final result can be

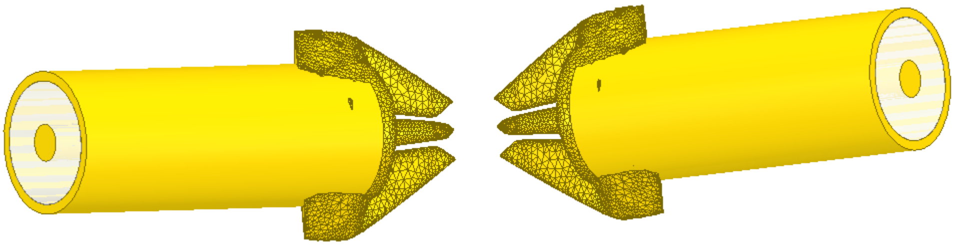


Figure 1.20: 3D model of Picoprobe used for EM simulation

compared with the calibrated and de-embedded S-parameters obtained from measurement.

1.7 Previous works on RF measurements beyond 110 GHz

Many articles have been reported in the literature on the calibration and de-embedding of RF transistors in the millimeter wave and sub-millimeter wave frequency ranges. Most of them are dedicated to devices from the III-V family, which have superior frequency performance due to the higher mobility compared to Si-based devices. The BEOL of III-V technologies cannot be compared to the BEOL of Si technologies. Si-technologies permit a (ultra/very) large-scale integration of devices which is orders of magnitudes higher than for III-V technologies. Thus the interconnect constraints request much fewer metal layers in the latter. Moreover, the natural oxide available in Si-technologies allows to construct multilayer BEOL quite easily. This involves some fundamental differences between the access from the pads to III-V devices and the access from the pads to Si devices on the wafer. Due to the reduced BEOL connectivity in III-V devices, only the CPW (coplanar waveguide) connection is feasible, except for some very special layouts where an inverted micro-strip has been realized [31]. CPW has the advantage of a low-loss connection, but the downside is the spurious wave modes that are excited and propagate in the substrate. These parasitic wave components may be scattered at neighboring structures on the wafer and cause detrimental crosstalk modes, which introduce quasi-non-controllable losses at frequencies beyond 110 GHz and no-foreseeable coupling with adjacent structures [16]. These parasitic propagation modes can be avoided in Si-BEOL thanks to the use of micro-strip configuration for the transmission line.

A review of calibration lines realized for the on-wafer calibration structures to use with TRL method has been elaborated by [79] and is shown in Table 1.5.

The lines in [57], [14] are designed in a SOI CMOS technology. Due to design rule constraints they were obliged to use a line layout comparable to a CPWG structure. The lines presented in [77] are dedicated to a BiCMOS technology, and again CPWG lines are used. The lines are enlarged to minimize the losses. On the other hand, in [9], where measurements up to 1 THz are shown on a process developed for THz application on III-V technologies, the authors use an inverted micro-strip line of 22 µm width on a BCB dielectric with very low dielectric losses. It is claimed that “the small cross section of the micro-strip transmission lines helps to reduce radiation and multiple modes of propagation”. Finally, in [79] a micro-strip line with a width of about 7 µm fabricated in a BiCMOS technology is introduced. This line represents a good trade-off between reduced losses and single mode propagation. Indeed, this line allows the suppression of high order modes at least up to 500 GHz.

Table 1.5: Review of calibration lines realized for the on-wafer calibration structures to use with TRL method, * Inter-probe distance is taken from the middle of the pad port 1 to the middle of the pad port 2.2 Distance is taken from pad (external part) structure 1 to pad structure 2 and is defined thanks to a vector, table taken from [79].

	Comments	Line topology	Thru length / Inter-probe distance [µm]	Line width / dielectric height / horizontal distance to GND [µm]	Pad size : length x width [μm^2]	Distance between two adjacent structures–vector [x,y], 2	Comments
Williams2013 [9] NIST	InP / BCB Meas up to 1 THz	MLIN	400µm / NAN	22 / 8 µm	44 x 22	150µm	BCB dielectric is used up to 750 GHz (no high order modes) Gold pad (IIIV techno.)
Williams2014 [57][9]NIST	Silicon MOSFET Meas up to 110 GHz	CPWG (metal density constraint in PDK)	300µm / 350 µm	6 / 6.275 / (see Fig. 2a) µm	40 x 30	undisclosed	Constraints in line design due to PDK Z_C =75 Ω corrected with off wafer load Gold platting of pads
Galatro[77] TU Delft	Silicon BiCMOS Up to 325 GHz IHP	CPWG	100 µm / 150 µm	30 / 8.8 / 10 µm	50x30	undisclosed	
Galatro[80] TU Delft	Silicon BiCMOS Up to 325 GHz	CPWG Inverted-CPW	30/8/15 µm 5/1.07/10 µm	30/8/15 µm	50x30	[160, 0] µm (structure are in line)	CPW and Innovative line topology
Fregonese IFX [15], [20] U. Bordeaux	BiCMOS Up to 500 GHz Infineon	MLIN	50 µm / 90 µm	4.9 / 3.9 /28 µm	38x38	[24, 0] µm (structure are in line)	Too dense floorplan => coupling to adjacent structure – Probable crosstalk
Yadav Brava U. Bordeaux [75]	BiCMOS Up to 500 GHz STMicro	MLIN	36.8 / 91 µm	5.74 / 5.8 / 12.5µm	43x27	[123, 0] µm	Slot in GND plane generates inaccurate results- coupling to adjacent structure is not significant – Probable crosstalk
Fregonese [79]	BiCMOS Up to 500 GHz STMicro	MLIN	65µm / 140 µm	7.7 / 5.6 / 28 µm	40x25	[207, 133] µm (structure are staggered)	Probable non-negligible crosstalk above 400 GHz

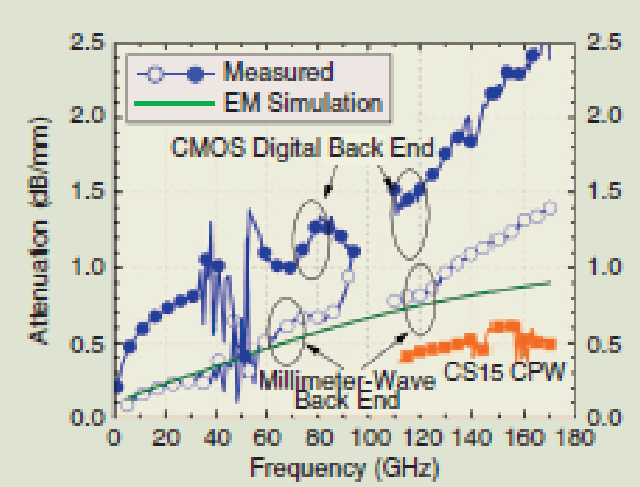


Figure 1.21: Measured versus simulated attenuation per mm as a function of frequency for microstrip lines fabricated in digital and mm-wave silicon back-end-of-line, figure taken from [61].

Even if our focus in this thesis is on MOS transistors, we will also take a look over the shoulder to BiCMOS technologies. Indeed, comparing BiCMOS to CMOS, we can observe similar BEOL when CMOS is not restricted to digital applications and the work published in the BiCMOS domain may inspire our research. Thus, thanks to the analysis of Table 1.5, we came to the decision that we will use in our test-structures the micro-strip architecture for the design of transmission lines. As already mentioned, the downside of micro-strip lines implies a higher loss compared to CPW lines. The line loss has been investigated in [81] and some results are depicted in Fig. 1.21 where we distinguish the measured attenuation as a function of frequency for transmission lines fabricated on the alumina ISS on CMOS and on SiGe BiCMOS wafers after performing a multiline TRL calibration on the ISS. We perceive that the loss of the lines in the thicker SiGe BiCMOS BEOL is about half that of the lines in the digital back end. It remains below 1.4 dB/mm up to 170 GHz, but it is still a factor of three larger than that of the coplanar transmission lines fabricated on the ISS. In [81], it is claimed that “this can affect the accuracy of some of the high-frequency FoMs of the transistor that are more sensitive to transmission line loss, such as f_{MAX} and minimum noise figure NF_{MIN}".

Thus care has to be taken in our work, to minimize the losses when designing transmission lines in micro-strip architecture. The next questions, when speaking about RF measurements beyond 110GHz, are: (i) on-wafer or off-wafer calibration, and (ii) which calibration method is the most adequate one? In [57], an on-wafer thru-reflect-line (TRL) and an off-wafer short-open-load-thru (SOLT) for transistor characterization on silicon integrated circuits at millimeter-wave frequencies have been carried out. The main conclusion is: on-wafer calibrations generally outperform off-wafer calibrations at millimeter-wave frequencies except at low frequencies, where the TRL calibration accuracy was limited by the length of the lines that were available. This study is very exhaustive, but limited to measurements up 110 GHz. Measurements up to 500 GHz have been presented in [20], where again on-wafer calibration has been compared to off-wafer calibrations. In this work, the validity of the characterization procedure above 110 GHz is investigated by an exhaustive study of on-wafer and alumina off-wafer calibration using measurement and electromagnetic (EM) simulation up to 500 GHz. The EM simulation is performed at two different levels, first at the intrinsic level of the devices under test for reference and afterward up to the probe level to simulate different standards used in the off-wafer calibration or in the on-wafer calibration in the presence of the probe. A good agreement is observed between measurement and EM modeling for the off-wafer calibration as well as for the

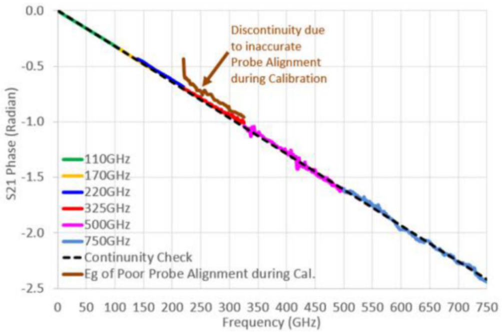


Figure 1.22: Phase versus Frequency (-0.185 Deg/GHz) for the 0.5ps Line, from [82].

on-wafer calibration. Results clearly highlight a limitation of alumina off-wafer methodology above 200 GHz for characterization of silicon-based technologies and that on-wafer calibration performs better than the SOLT on ISS beyond 200 GHz. In another study, a theoretical comparison of different on-wafer and off-wafer calibration and de-embedding methods above 110 GHz are discussed in [81]. Comparison is also made between the off-wafer calibration standards and on-wafer calibration standards. A significant observation is that although on-wafer calibration standards possess several advantages, the attenuation in these standards is much higher than that in the ISS standards, especially at higher frequencies, but this point has already been discussed above.

To sum up this section, we can say that the on-wafer calibration is the route to take when going beyond 100 GHz measurements. This decision being taken, the second question: which calibration method is the most adequate one is already answered. In fact, Williams [14] claims that TRL is the method of choice for on-wafer calibration. However, several factors affect the accuracy of the TRL calibration. [18] lists two main reasons for the limitations of this calibration method. These are:

- Probe position uncertainty due to required spacing change during measurement due to the different lengths of Line standards Inaccurate probe placement on calibration standard during calibration has been reported by [82]. To highlight this issue, we extracted from this work the following Fig. 1.22, which presents the phase vs frequency up to 750 GHz of a 0.5 ps Line.

We can observe that the measurement discontinuities of the 0.5 ps line at the 220-325 GHz frequency band. The author claims that this is due to inaccurate probe placement on standards during calibration.

- Coupling between probes and between the probe and the test structure below: Remark: If the test structures are not affected by crosstalk and if there is sufficient space between them, the TRL properly takes into account probe to substrate coupling. But this probe-to-substrate coupling must be identical for all test-structures. In reality, the environment is not homogenous between structures (structure are close to each other) and if there is a different crosstalk (thru vs line for example), then it introduces some errors during the calibration and the coupling between probes and test structures is not correctly taken into account. In particular, it is claimed in [83]: “When using multiline TRL calibrations for correcting on-wafer measurements, the accuracy of the result depends crucially on the consistency of the calibration set. For example, each line standard used in the calibration process must allow unambiguous measurements, i.e., the only difference between the various transmission-line elements should be line length. To this end, the pad structure

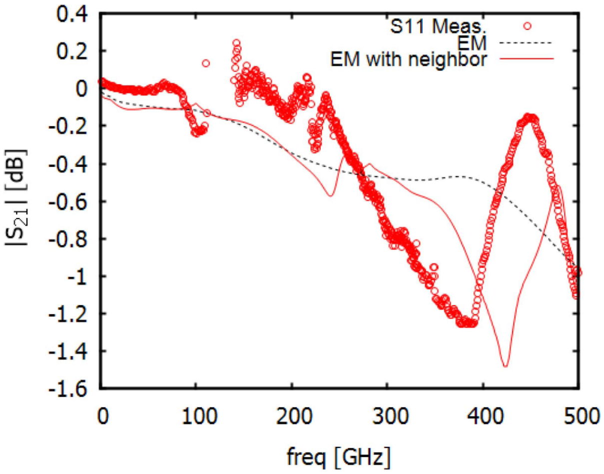


Figure 1.23: Magnitude of S_{21} parameter measurements of a line up to 500 GHz showing unexpected behavior: impact of adjacent structures confirmed with EM simulation, from [79].

for the probes, the probe mechanical contact properties and the environment including other structures, wafer or chip boundary and backside structures (metallization, chuck material) should be the same for each element. If this condition is not fulfilled, errors in the multiline TRL calibration process occur." Here, Multiline TRL has been discussed, but the conclusion will not change when going to the standard TRL method. Moreover, the measurements have been performed on GaAs substrate with CPW configuration, but this does not fundamentally alter the coupling from probe tip to the underlying test-structure.

- Another critical issue that may affect TRL calibration is the coupling with adjacent structures:

In [64] it is shown, that the design of the on-wafer standards can affect the measurement accuracy. The spatial arrangement of the neighboring on-wafer structures around the DUT can also influence the results and this can be minimized by using a diagonal checkerboard pattern. The influence of neighboring structures has also been highlighted by [79]. As an example, the Fig. 1.23 shows the magnitude of the S_{21} parameter measurements of a line up to 500 GHz. An unexpected decrease of mag(S_{21}) can be depicted from 230 GHz to 400 GHz. Performing EM simulation of the test-chip including the neighboring structures, this un expected behavior could be reproduced. This test-chip had a very dense layout for the test-structures.

From this section, we conclude, that for the layout of the test-structures dedicated to TRL calibration, a particular attention has to be drawn to the placement of these structures. A dense layout should be avoided and an appropriate distance between the structures should be chosen; the arrangement in checkerboard pattern seems to be the most appropriate.

Some more details and specifications on the design of the test-structures, the choice of probes, care during probe positioning have also been reported and are briefly referenced below:

- The nature of the reflect standard has minor effects on the error terms as discussed in [84].
- Inaccuracies in the calibrated S-parameters can also result from incorrect probe positioning on the RF pads [15].
- The effects of measurement environment, specifically the choices of RF probe and the calibration type, have been discussed in [85]. Coupling was the main issue, and test-structure

layouts having a pitch of only 50µm are very promising because here the coupling is reduced due to better confinement of the EM wave.

- It is suggested in [9] that the calibration kit designed with a continuous ground plane below all the test structures can reduce multimode propagation and eliminate slot modes. The benefit of such a design using test structures from STMicroelectronics BiCMOS 55nm technology has been demonstrated in [86].
- Moreover, [16] demonstrates that the undesired parasitic mode propagation can be averted by a muffled RF pad design as the presence of a guard ring around the pads helps to suppress the parasitic modes that originate at the point where probes contact the RF pads.

Finally, the above articles will help us design best-in-class test structures for on-wafer TRL calibration and thus perform accurate and reliable measurements.

Chapter 2

Characterization and EM simulation of Run1 test structures

This research work begins with measurements performed using existing test structures that had already been designed. In this chapter, the test structures in the calibration kit are explained in detail. Also discussed are the measurement results from 1-500 GHz and the procedure used for extracting the transistor parameters. Measurements are followed by the extraction of Small Signal Equivalent Circuit (SSEC) for the transistor. These measurements are validated using Electromagnetic (EM) simulations, which are also detailed in this chapter. Comparisons are made between the results using different RF probes and different calibration methods.

2.1 Test Structure Description

The On-wafer TRL calibration kit designed includes the following TRL test structures: (i) Thru (ii) Pad open (iii) Pad Short (iv) Pad Load (v) LINE_110G (vi) LINE 500G. There are 3 FDSOI transistors to be characterized, which are labelled as SGL84, SGL86 and SGL102. Each transistor is associated with dedicated Open and Short structures for de-embedding. The wafer floor plan for the calibration kit and the devices is shown in Fig.2.1. These test structures are fabricated using the 28nm FDSOI technology of STMicroelectronics. There are two versions of the BEOL (refer Fig. 2.2): 8ML (eight copper metal layers with vias separating each) or 10ML (10 metal layers, with vias).The first metal layer is labelled M1 and makes the contact with the transistor active region through the contact metal layer (CA, not shown in figure). The thin metal layers M2 to M6 are above M1. The two intermediate layers, B1 and B2 are present only in the 10ML version of the BEOL. Above this are the thick metal layers IA, IB, and finally the topmost Aluminium metal layer LB or Alucap, which is used to form the RF probe pads and access lines.

The first set of test structures designed use the 8ML version of the BEOL. This includes the metal layers M1-M6, IA, IB and LB. The LB layer forms the contacts with the RF measurement probes. The on-wafer test structures and DUTs are arranged in a checkerboard configuration so as to minimize the effects of neighbouring structures as suggested in [87]. The structures are placed at least 100 μm apart horizontally and vertically.

The RF signal and ground pads are designed in the LB layer. The signal pad dimensions are shown in Fig. 2.3. It has a width of 40 μm and a length of 60 μm. It also includes a small 50 Ω access line of length 15 μm. The entire LB layer has a covering of passivation layer (oxide), with openings in the RF signal pad and ground pads to allow contact with probes.

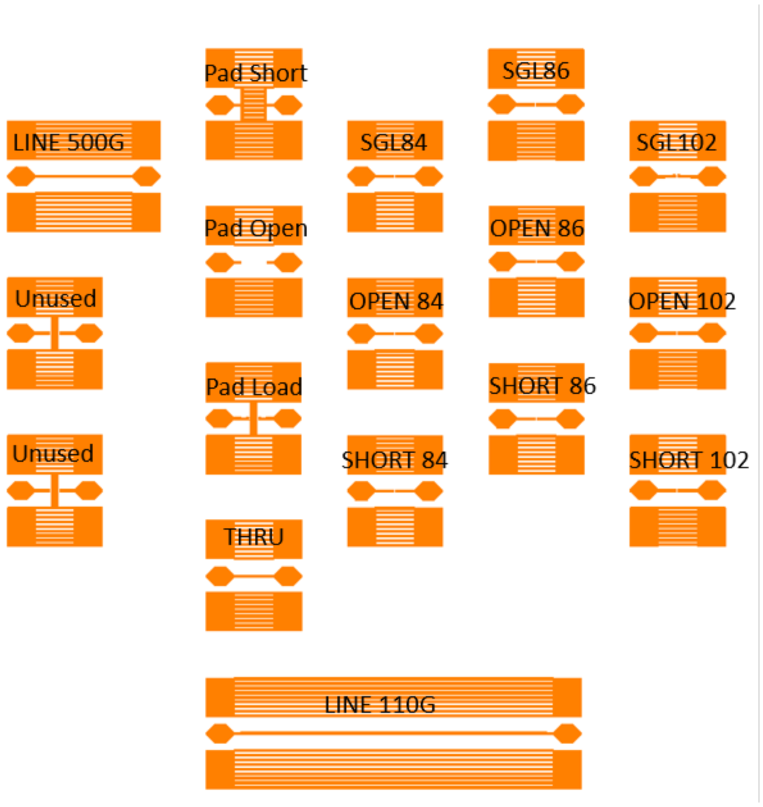


Figure 2.1: Top layout of the on-wafer calibration kit.

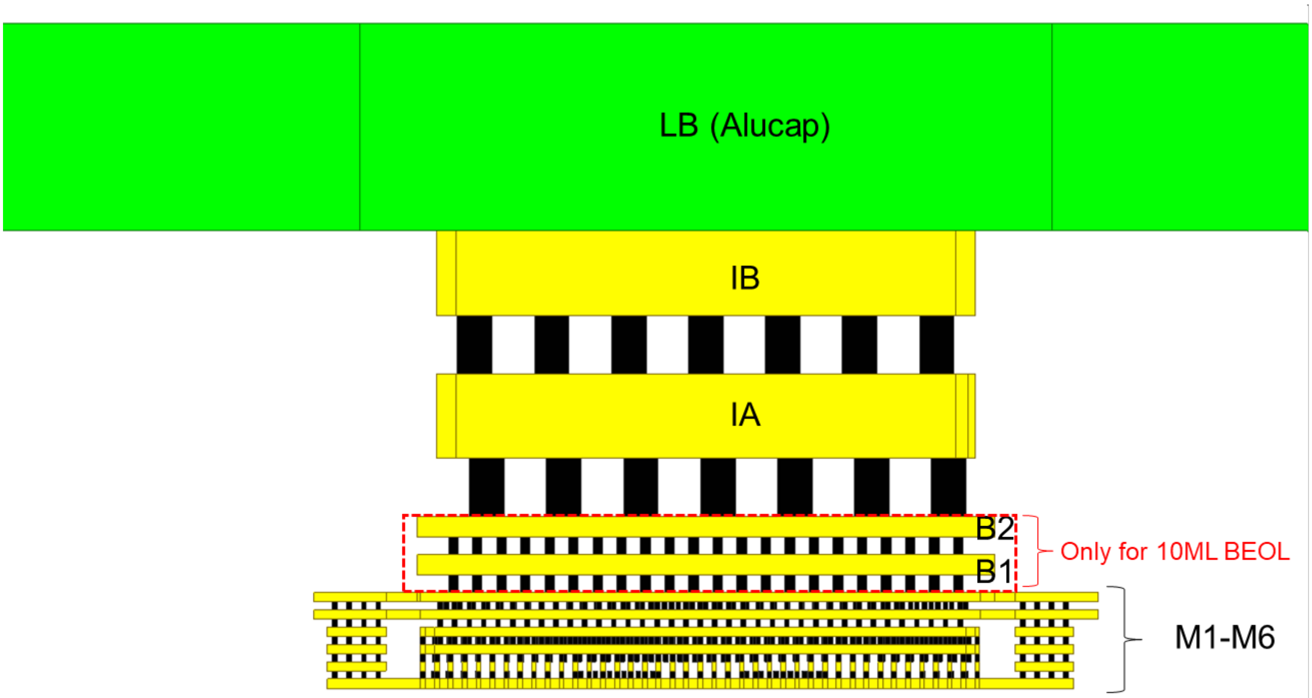


Figure 2.2: BEOL of 28 FD-SOI

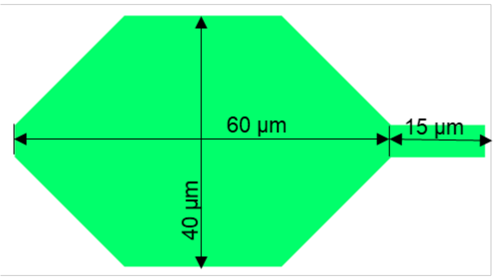


Figure 2.3: Dimensions of the RF signal pad

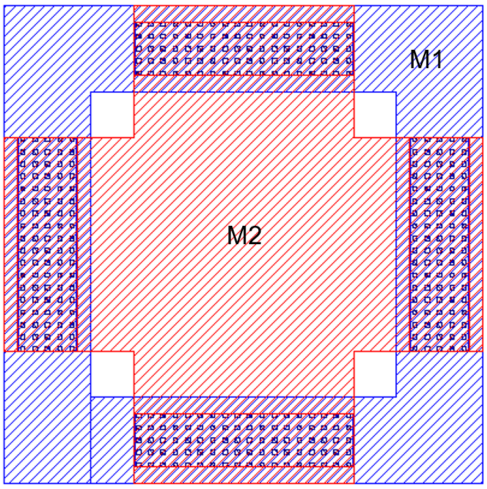


Figure 2.4: Ground plane unit cell consisting of M1 and M2

The transmission lines are also realized using this LB layer. Out of the 8 copper layers below LB, the two lowermost layers, M1 and M2, are meshed to form the ground plane for each of these structures. The meshed design is necessary in order to satisfy the density rules during the fabrication process. The unit cell of the ground plane in shown in Fig. 2.4. It can been seen that the layers M1 and M2 are slotted and meshed with the vias V1 connecting the two layers. This unit cell is repeated throughout the test structure to form the complete ground plane.

The **THRU** and **LINES** (LINE 110G and LINE 500G) are designed as 50 Ω microstrip transmission lines using the LB layer. The oxide layers of the BEOL act as the dielectric between line (LB) and the ground plane (M1+M2). These are designed with a line width of 5.1 μm, in order to maintain the 50 Ω characteristic impedance of the transmission lines according to equation 2.1 [88], where h is the height of the dielectric and W is the width of the microstrip line.

$$Z_0 = \frac{60}{\sqrt{\epsilon_{r,eff}}} \ln\left(\frac{8h}{W} + \frac{W}{4h}\right) \tag{2.1}$$

The transmission lines are thus designed with a spacing of 3.68 μm between the line and the ground plane, and the line thickness is 2.11 μm. The THRU is a microstrip line of length 55 μm. The 28 FD-SOI process has a shrinking of 10%. Therefore all layout drawings are made with a 10% increase from the actual dimensions. However, the lengths and widths mentioned throughout this thesis correspond to the actual dimension, and not the drawn dimension. The calibration kit uses lines of two different lengths, labelled as Line_110G and Line_500G. Each line has a specific operating frequency range for which it can be used for TRL calibration as

Table 2.1: Frequency limits of the TRL Line standards

	Length (μm)	f_{min} (GHz)	f_{max} (GHz)
Line_110G	660	13	120
Line_500G	180	65	585

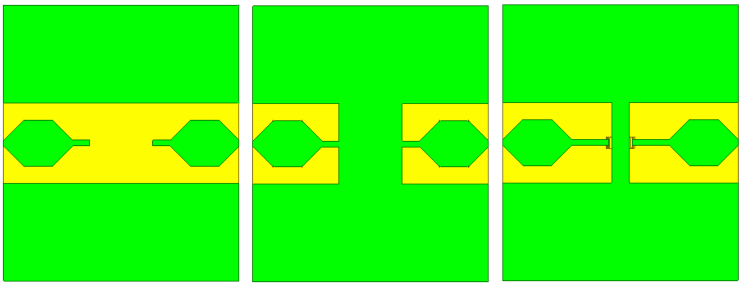

(a) Pad Open (b) Pad Short (c) Pad Load

Figure 2.5: Top views of test structures

listed in Table 2.1. The upper and lower frequency limits of this range are calculated from the equations 1.7 and 1.8 [61].

The $\epsilon_{r,eff}$ in these equations is the effective dielectric constant of the transmission line. It can be calculated as the effective dielectric constant of an equivalent material which can replace the series of oxide layers in the BEOL, present between the ground plane (M1+M2) and the line (LB). From these equations, it is found that the Line_110G, which has a length of 660 μm is a valid line standard for TRL calibration up to 110 GHz. Similarly the Line_500G is valid for calibration from 65 GHz to 500 GHz. Thus, for on-wafer TRL upto 70 GHz, THRU and Line_110G are used as standards to calculate line propagation constant γ, whereas for calibration above 70 GHz, THRU and Line_500G are used to calculate γ. The values are summarized in Table 2.1.

Pad Open and **Pad Short** are the reflect standards of the TRL calibration kit. The Pad Open is formed by leaving the ends of the RF signal pads unconnected or open. The top view of the layout of Pad Open is displayed in Fig. 2.5a. The Pad Short is created by short circuiting or connecting together the signal pads to each other and to the ground pads as shown in Fig. 2.5b.

The **Pad Load** is another test structure present in the calibration kit. This, however, is not directly used for TRL calibration, but is essential to perform the impedance correction of the calibrated S-parameters. As discussed in the previous chapter, the reference impedance of the TRL calibrated S-parameters is equal to the characteristic impedance of the lines used for calibration. Although the lines here have been designed theoretically to have 50 Ω characteristic impedance, it can have minor variations and is also dependent on frequency. Hence it is imperative that the impedance correction is performed after TRL calibration. The Pad Load is a structure with a known reflection coefficient, in this case, the Pad Load is formed by attaching a known load of 50 Ω to each of the signal pads.

There are 3 **DUTs** fabricated on the wafer for calibration. These are 28nm FDSOI NMOS LVT transistors, the device geometries of which are described in Table 2.2. The transistor devices are fabricated below the M1 metal layer. It is then connected to the signal pads using the BEOL metal stack of 8 layers (from M1 to IB) and through the access lines in LB Layer. Therefore, after TRL calibration, the S-parameters are with respect to a measurement reference plane in the LB

Table 2.2: Transistor geometries on the wafer

Device	**W(μm)**	**L (μm)**	N_f	W_f(μm)
SGL84	40	0.03	40	1
SGL86	20	0.03	40	0.5
SGL102	20	0.04	40	0.5

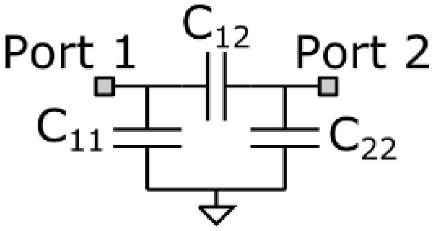


Figure 2.6: Equivalent circuit of Transistor Open

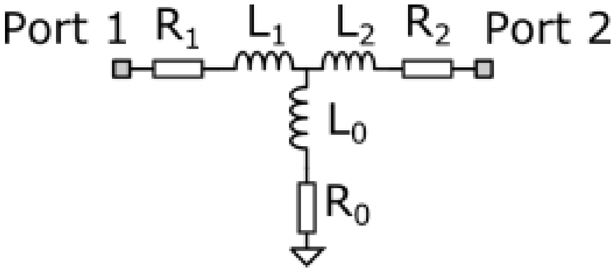


Figure 2.7: Equivalent circuit of Transistor Short

layer as already discussed in Chapter 1. This means, the parasitic effects (capacitances and inductances) due to the access lines and the BEOL stack need to be removed, which necessitates a de-embedding procedure. For this purpose, the additional structures, dedicated Open and Short for each transistor are made use of.

The Transistor Open creates an open circuited transistor at the gate fingers at M1 metal level. It can be represented by an equivalent circuit consisting of parallel capacitors as in Fig. 2.6. Transistor short circuit can be achieved by shorting the gate fingers at M1 level, and represented by an equivalent T-network of series inductors and resistors as presented in Fig. 2.7.

2.2 Intrinsic EM Simulations

Before we move on to the actual measurement results and the transistor characterizations, we briefly assess the intrinsic performance (section 1.6) of the on-wafer test structures.

2.2.1 Line Characterization

The on-wafer TRL calibration kit includes two Line standards and a Thru. All these three structures are microstrip lines of 50 Ω characteristic impedance. The simplified intrinsic 3D models are imported into HFSS and simulated as already discussed in Section 1.6. The HFSS model for simulation of THRU with the required ports and boundaries is shown in Fig. 2.8. Similar models are created to simulate the Lines as well. Fig. 2.9 plots the magnitude of S_{11} of the 3 lines obtained after intrinsic simulation. The first resonances in the plots for Line_110G and Line_500G (shown using dashed lines) gives an approximate idea of the maximum frequency limits of the lines for TRL calibration.

In needs to be pointed out here that due to an oversight in the layout design, an automatic tiling has been applied on the Line_110G and Line_500G. This was necessary as the minimum density rules were not complied by the layouts of the Lines and it has led to the presence of small metallic tiles around the microstrip line region as can be seen in Fig. 2.10. However,

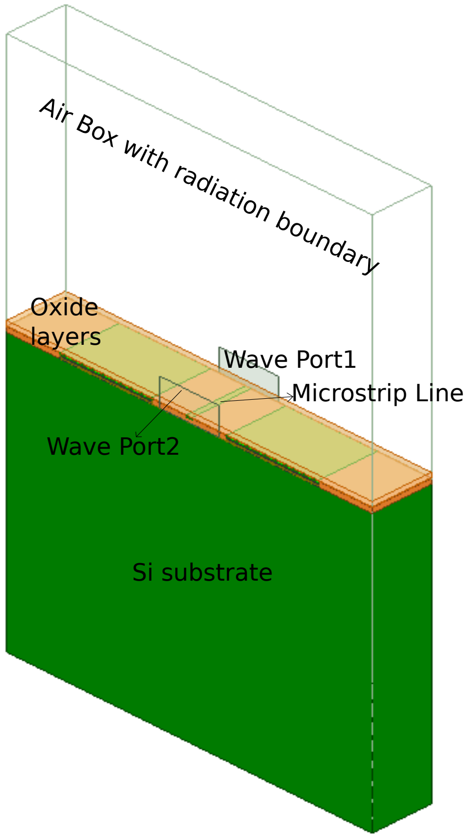


Figure 2.8: HFSS model for intrinsic simulation of THRU

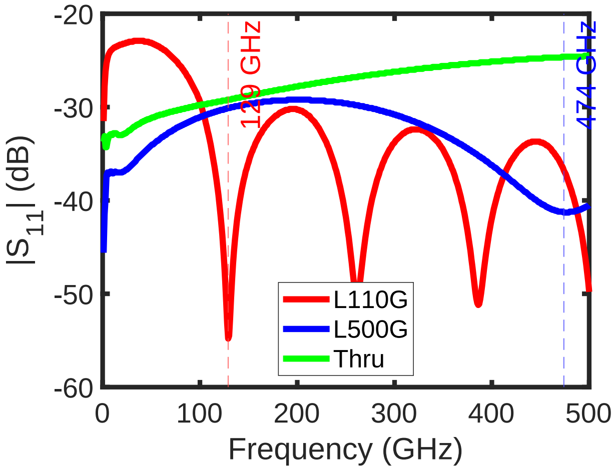


Figure 2.9: Plot of S_{11} vs frequency for the Lines and Thru

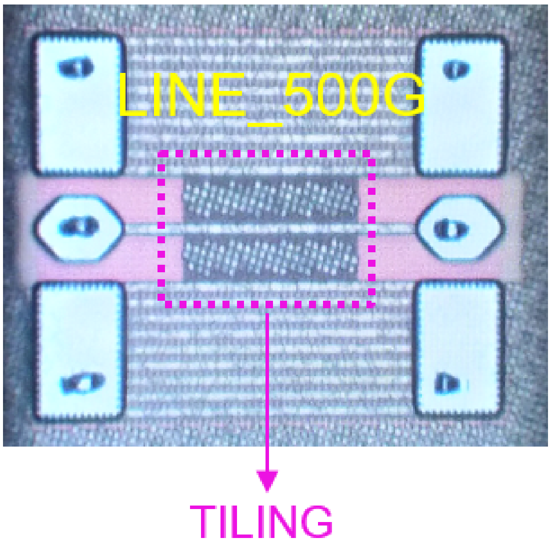


Figure 2.10: Photograph of the Line_500G. Tiles can be seen in the region within the dotted box

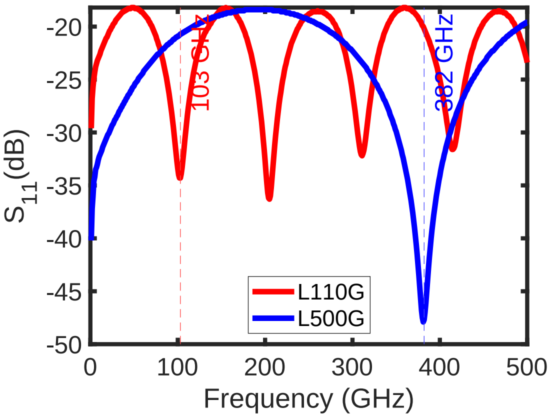
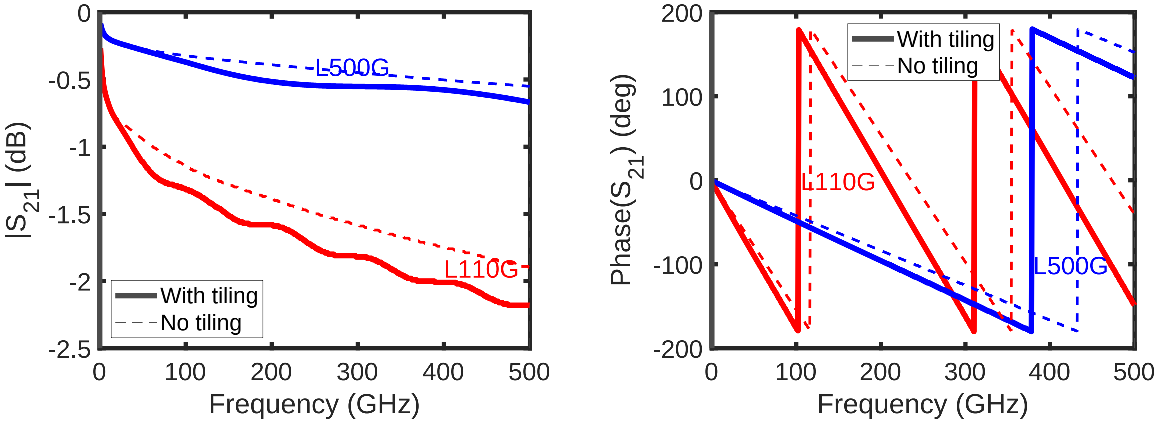


Figure 2.11: S_{11} of Line_110G & Line_500G with the hybrid oxide that accounts for tiles

the presence of these tiles do not affect the signal propagation through the lines, as these are unconnected independent structures embedded in the oxide layers. Nevertheless, the tiling slightly modifies the field lines as the effective relative permittivity ($\epsilon_{r,eff}$) of the oxide is now altered due to the presence of metal with very high ϵ_r. The major consequence of this increase in $\epsilon_{r,eff}$ is that the TRL limits are now decreased as the F_{min} and F_{max} (refer equations 1.7 and 1.8) of the Line standards decrease. Moreover, since the tiles are not present in the Thru, but only in the Lines, the characteristics of the Thru and the Lines are not rigorously similar. Despite this layout design issue, this Chapter 2 will be mainly devoted to setting up a methodology to validate the measurements by electromagnetic simulation.

Thus, the plots presented in Fig. 2.9 is the ideal case, and we now need to model the Lines appropriately to simulate the effect of tiling. One method to do this is to import the layout along with the tiles and proceed with the simulation setup. This, however makes the meshing difficult and greatly increases the simulation time. Another method, that is adopted in this work is to modify the oxide layer properties to form an equivalent material, in such a way that it takes into account the effects of tiles. To do this, the measurements, which will be discussed later, have been taken as a reference. From the measurements, it is observed that the line capacitance increases as a result of the presence of tiles. Therefore, the oxide dielectric constant (ϵ_r) is increased in the simulation setup so as to achieve the same capacitance as that obtained from measurements. This new oxide is referred to as 'hybrid oxide'. The Line_110G and Line_500G are then simulated using this hybrid oxide that replaces the original oxide layer. The unwanted tiling is present only in these two test structures, so all the EM simulation of all other structures including the Thru make use of the actual oxide layer.

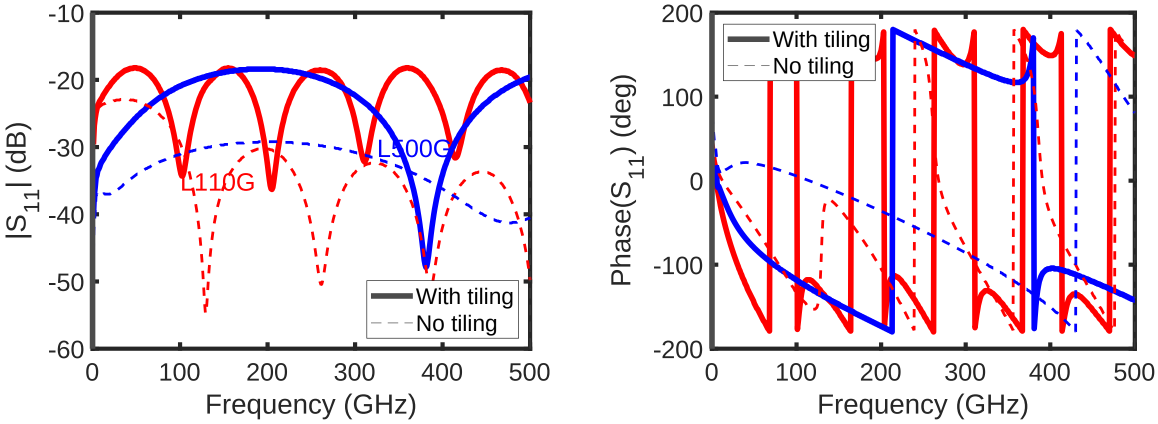
The effect of tiling can be visualised in Fig. 2.11, where the S_{11} of the lines with the hybrid oxide are plotted. It is evident from the figure that the resonance frequencies of the Lines are now lowered (to 103 GHz and 382 GHz respectively), which indicates the decrease in the F_{min} and F_{max} of Lines, and hence a lowering of the limits of TRL calibration. This means that the designed TRL calibration kit cannot provide reliable results beyond 400 GHz. Besides, the $|S_{11}|$ of the actual lines reaches -20 dB, compared to the expected -30 dB. The automatic tiling has obviously affected the characteristic impedance of the actual lines, that are lesser matched to



(a) Magnitude in dB

(b) Phase in degrees

Figure 2.12: S_{21} of Lines and Thru with (actual case) and without (ideal case) tiling



(a) Magnitude in dB

(b) Phase in degrees

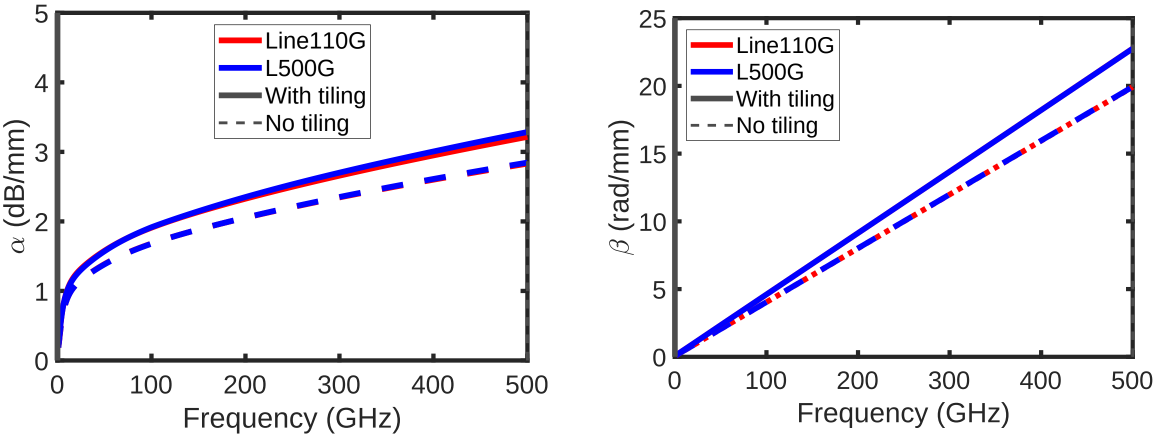
Figure 2.13: S_{11} of Lines and Thru with (actual case) and without (ideal case) tiling

50 Ω. The impedance correction step will be then inevitable.

We will now have a look at how the other parameters of the Lines are affected due to tiling, by comparing it to the ideal case without tiles. Fig. 2.12 shows the magnitude and phase of S_{21} for Thru and Lines (with and without tiling). It is evident from the magnitude plot that the lines become more lossy when metallic tiles are present, due to the resulting eddy currents in the tiles. Moreover, this attenuation is more pronounced in the longer Line_110G as it has more region covered by the tiling.

Propagation constant γ

The propagation constant γ is given by $\gamma = \alpha + j\beta$, where α is the attenuation constant and β is the phase constant. These quantities are plotted in Fig. 2.14 as a function of frequency for Line_110G and Line_500G. It can be observed that the tiling in the Lines increases the line attenuation. This is already evident from the S_{21} plots. It can also be seen that the tiling causes a small increase in the phase constant β, particularly at higher frequencies.



(a) Alpha

(b) Beta

Figure 2.14: Propagation Constant of Lines

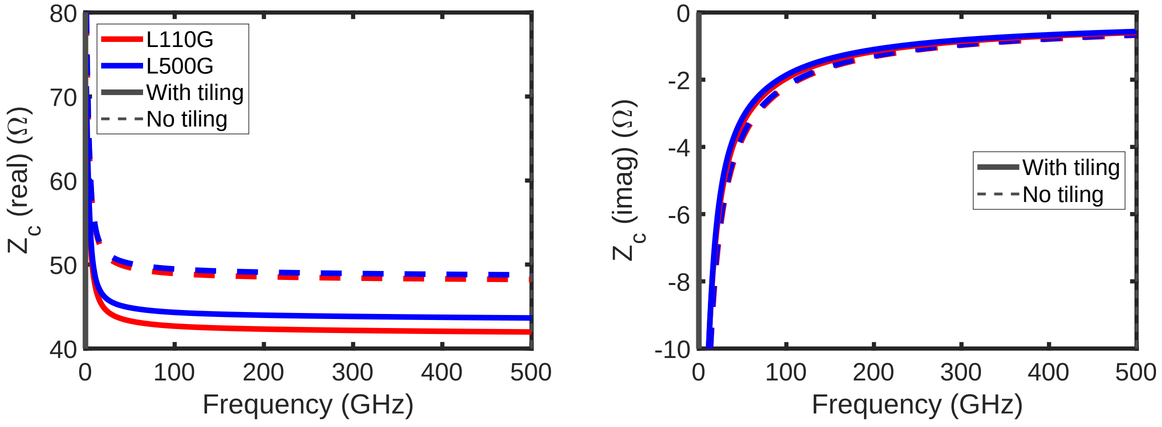


Figure 2.15: Characteristic impedance of the Lines

Characteristic impedance Z_c

The characteristic impedance (Z_c) of the Lines are plotted in Fig. 2.15. As assessed by the analysis of $|S_{11}|$, it can be seen that the characteristic impedance is now lowered to ∼44Ω as a result of the change in $\epsilon_{r,eff}$ due to the presence of tiles in accordance with equation 2.1. The aftermath of this lowered Z_c is that efficient impedance correction needs to be performed after TRL calibration so that the S-parameters are referenced to the standard 50Ω value. Thus the effects of change in Z_c is mitigated by the impedance correction step.

RLCG model

The transmission lines can be represented in terms of their line parameters per unit length. The distributed line parameters R, L, C, G can be used to represent the transmission line as in Fig. 2.16. The following equations (equations 2.2-2.5) [89] can be used to extract the values of these elements.

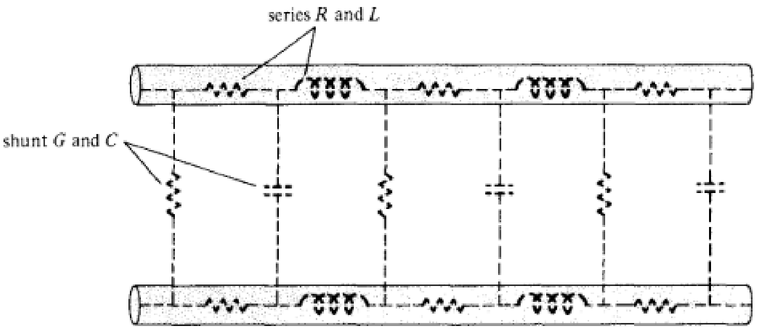


Figure 2.16: RLCG model of transmission line

$$
\begin{aligned}
R &= real(\gamma Z_0) && (2.2)\\
L &= imag(\gamma Z_0)/\omega && (2.3)\\
C &= imag\left(\frac{\gamma}{Z_0}\right)/\omega && (2.4)\\
G &= real\left(\frac{\gamma}{Z_0}\right) && (2.5)
\end{aligned}
$$

These are plotted in Fig. 2.17. It is worth mentioning here that the parameter C is most affected by the tiles. An increase of 50pF/m (approximately 40%) is observed due to tiling.

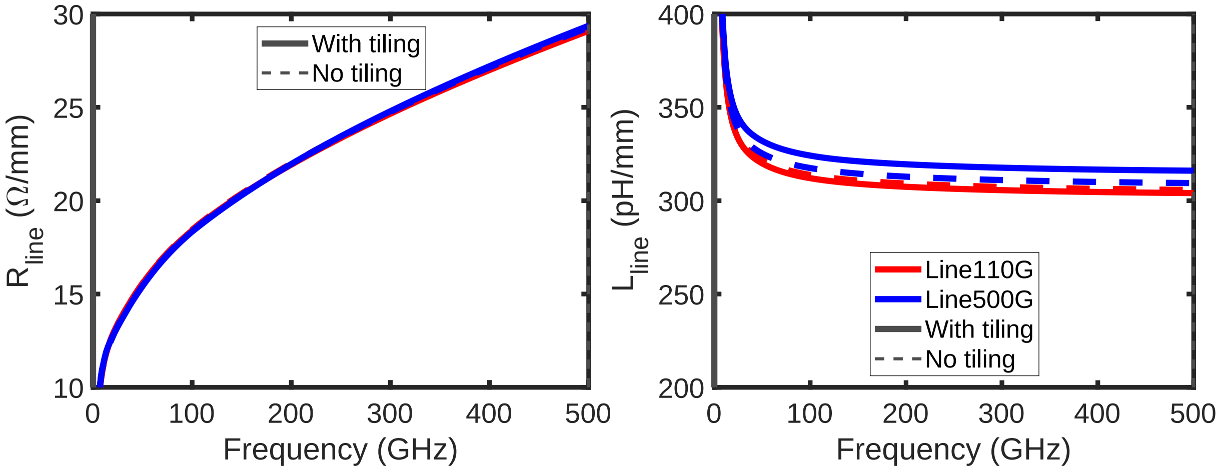
On the whole, it can be stated that all the effects that are observed in the lines due to tiling are an effect of the increase in $\epsilon_{r,eff}$ resulting from the presence of the small metallic pieces in the dielectric. This can be visualised as in Fig. 2.18 using HFSS simulation, where the $\epsilon_{r,eff}$ is plotted with and without tiles.

2.2.2 Pad Load

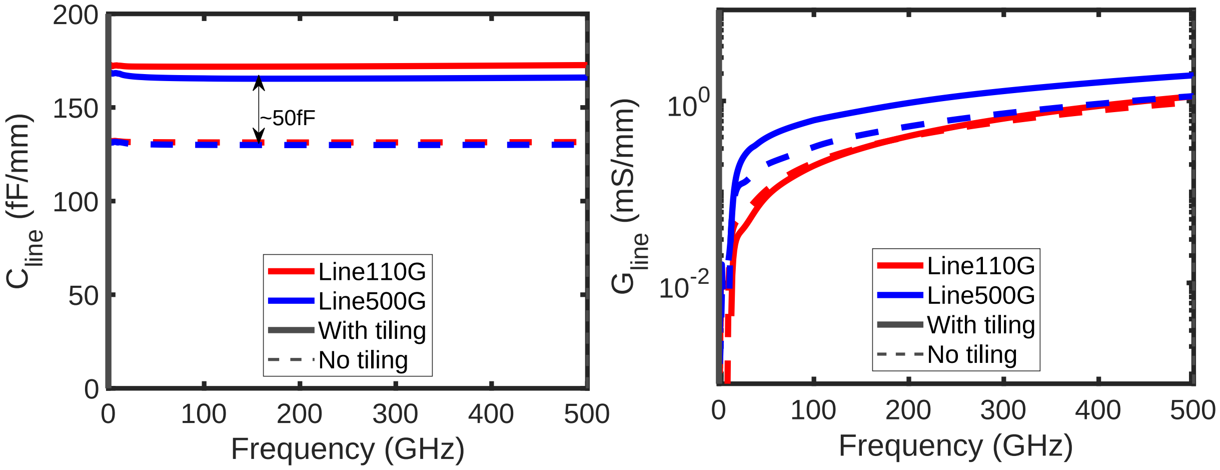
Pad Load, the test structure required to perform the impedance correction after TRL calibration, can be represented by the equivalent circuit as in Fig. 2.19. The access lines are of length 17 μm on either side. This corresponds to a negligible resistance value of $\approx$ 0.3 Ω each side (calculated from the R/unit length of the microstrip line), represented by $R_{access1}$ and $R_{access2}$ in the figure. The value of the resistance that has been realised in the layout using the Polysilicon layer, just below the M1 metal layer, is calculated as:

$$
\begin{aligned}
R_1 &= real(Z_{11}) && (2.6)\\
R_2 &= real(Z_{22})
\end{aligned}
$$

This resistance value has been calculated from the intrinsic EM simulation of the Pad Load and is plotted in Fig. 2.20.



(a) R (b) L



(c) C (d) G

Figure 2.17: RLCG parameters of Line

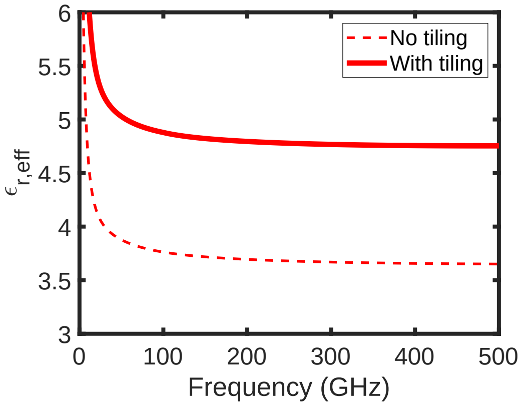


Figure 2.18: Effective dielectric constant of lines with and without tiling

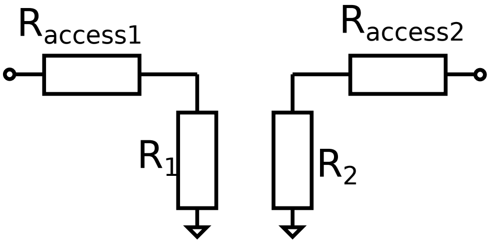


Figure 2.19: Equivalent lumped element model of Pad Load

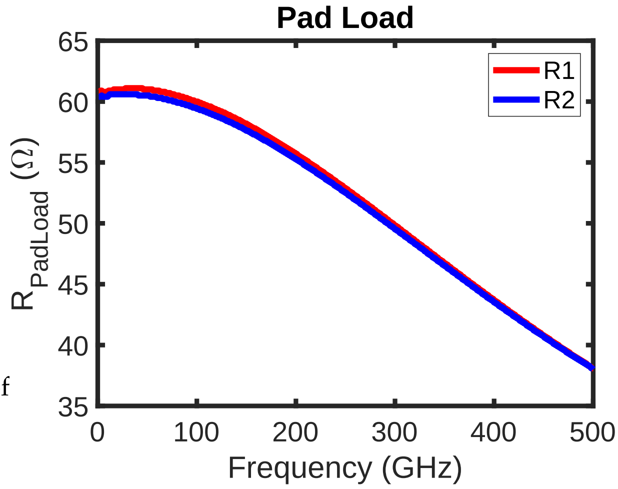


Figure 2.20: Pad Load

2.2.3 De-embedding structures

Transistor Open

The equivalent circuit diagram of a Transistor Open has already been discussed in Section 2.1. To obtain the theoretical values of these capacitances, an EM simulation of its intrinsic structure is performed. The 3D model for the intrinsic simulation of Open is shown in Fig. 2.21. Here, the model also includes the access lines to the DUT. Therefore, if we look at the extracted Open capacitance plots (Fig. 2.22a), we can see a frequency dependence for the capacitance C_{open2}. This frequency dependence is due to the distributed effects of the microstrip transmission line (access lines), and it can reduce the accuracy of the Open/Short de-embedding to be performed, because the de-embedding methodology assumes a lumped element model for the parasitics. To confirm this, the Transistor Open is re-simulated with the access lines removed from the 3D model (reference plane 2 in Fig. 2.21). The capacitances extracted from the new simulation are plotted in Fig. 2.22b. Here, it is seen that the values are now constant or frequency independent for a wider range. The shifting of reference plane can be done during the process of TRL calibration by adjusting the parameters accordingly. This TRL advantage will be discussed in detail in the coming sections.

It is to be noted that the plots shown in this section are for the Transistor Open corresponding to the Transistor SGL86.

Transistor Short

Similar to the steps followed for Open, an intrinsic EM simulation of Transistor Short is performed using HFSS and the equivalent lumped circuit elements (see Fig. 2.7) are extracted. The simulation is carried out both with and without the access lines, and these values of inductances and resistances are plotted in Fig. 2.23. The solid lines correspond to the simulation with access lines and dashed lines are without access lines. Once again it is seen that the values are frequency independent when access lines are removed. It is also to be noted that the resistance at gate, R_1 is much higher, in fact double that of the resistance at the drain. This effect is consistent with the layout design, as the BEOL is connected differently at the gate and the drain.

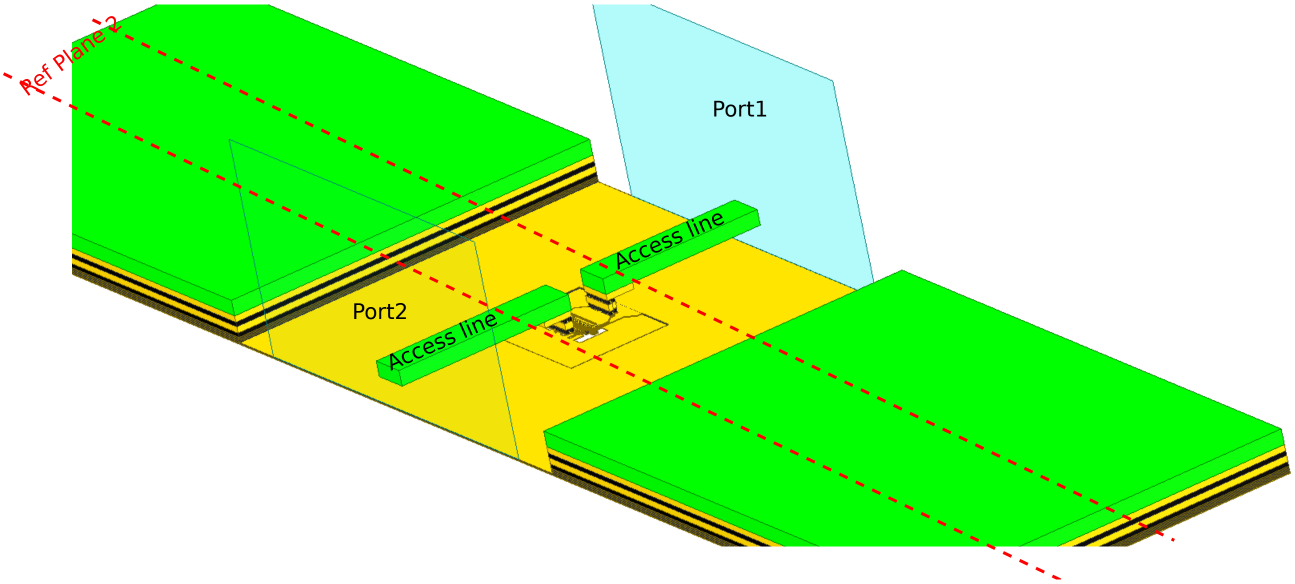
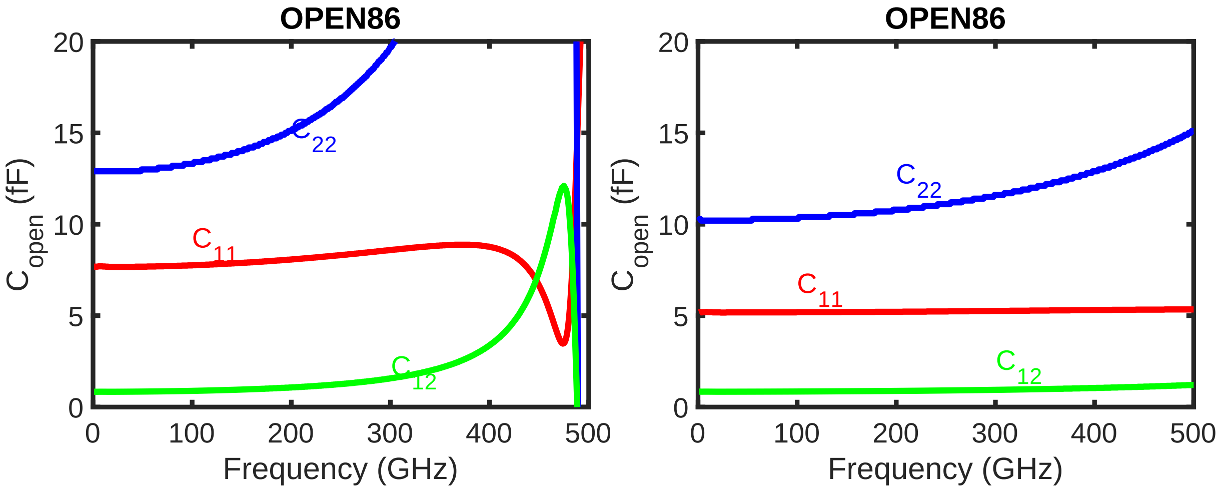


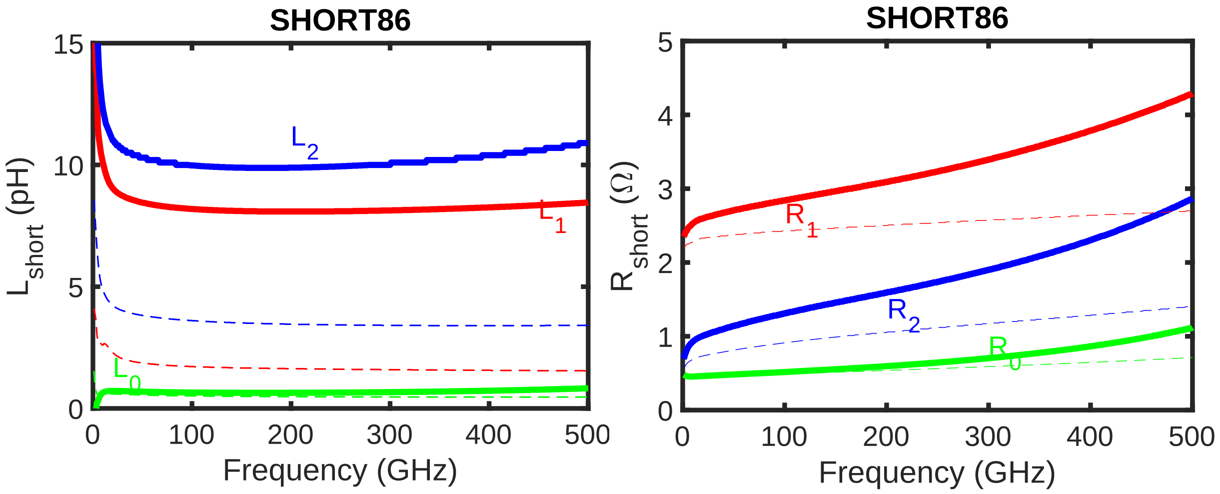
Figure 2.21: 3D model in HFSS for intrinsic simulation of Transistor Open. Ref Plane 2 corresponds the reference plane after shifting the TRL calibration plane close the DUT along the transmission line.



(a) With access lines

(b) Without access lines

Figure 2.22: Equivalent capacitances of Transistor Open extracted from EM simulation



(a) Equivalent inductances of Transistor Short

(b) Equivalent resistances of Transistor Short

Figure 2.23: Equivalent lumped elements of Transistor Short extracted from EM simulation (solid lines: with access lines; dashed lines: without access lines)

2.3 Transistor characterization procedure and Measurement results

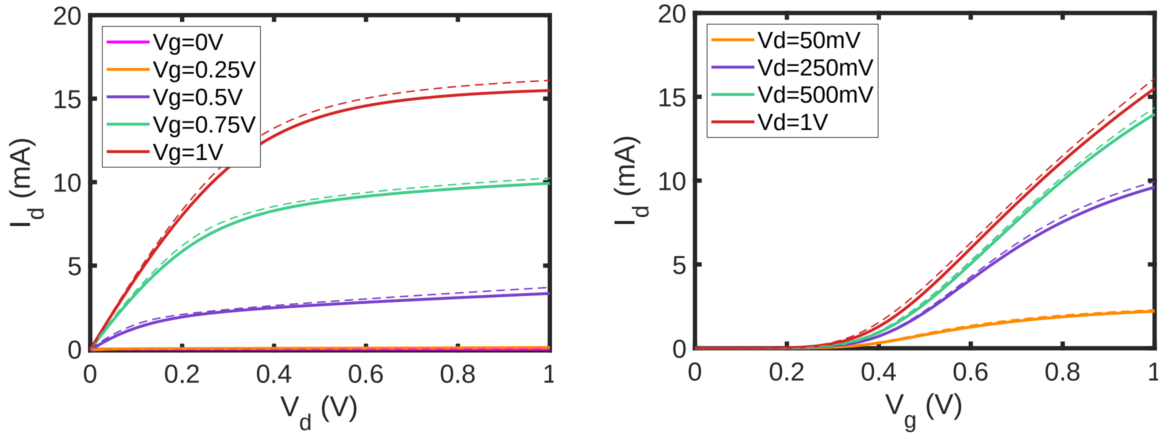
2.3.1 DC measurements

The transistor to be characterized is the one labelled SGL86. The input and output characteristics of the transistor are first visualised by plotting its DC characteristics. The drain current (I_d) vs drain voltage (V_d) plots for different gate voltage (V_g) biases are plotted in Fig. 2.24a. The drain current as function of gate voltage for different drain voltages is presented in Fig. 2.24b. These plots are compared to the ones obtained from the simulation of the transistor compact model (shown by dotted lines). Also plotted are the g_d and g_m plots with respect to V_d and V_g respectively. The comparison between compact model simulation and DC measurements shows a satisfying agreement for the considered bias points.

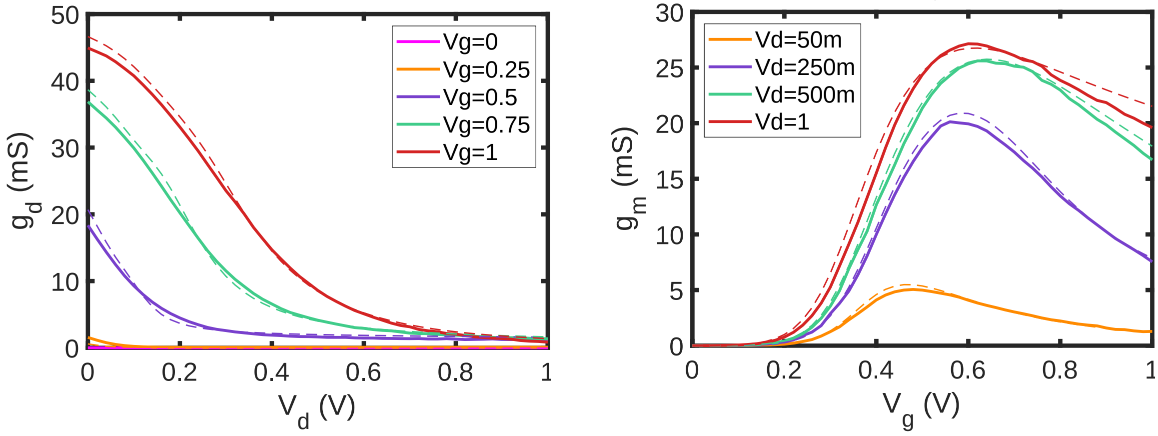
2.3.2 RF measurements

For on-wafer TRL calibration, the uncalibrated S-parameters were measured using the appropriate measurements setups. This data was then treated using the TRL toolkit already developed by the team at IMS laboratory, which implements the TRL calibration algorithm on the uncalibrated parameters, followed by the impedance correction. Off-wafer SOLT calibration was done for the first 2 frequency bands using additional measurements on the calibration standards on alumina and then applying the SOLT calibration either using the toolkit or the inbuilt VNA program for calibration. SOLT calibrated results were same with both the toolkit and the VNA calibration, hence further distinction will not be made while referring to SOLT calibration in this thesis. A Short-Open de-embedding method is applied after TRL calibration, whereas the SOLT calibration requires a Pad-Short-Open de-embedding method.

Although this thesis focuses on the on-wafer TRL calibration, the off-wafer SOLT calibration has been performed to enable a comparison with the off-wafer calibration which is the existing industrial standard for calibration. The calibrated and de-embedded S-parameters are used to



(a) $I_d - V_d$ (b) $I_d - V_g$



(c) $g_d - V_d$ (d) $g_m - V_g$

Figure 2.24: DC Characteristics of the FD-SOI NMOS transistor (SGL86)

extract the transistor parameters. Two main RF figures of merit that determine the RF performance of transistors are f_T and f_{MAX}.

The transit frequency f_T is the measure of the intrinsic speed of a transistor. It is defined as the frequency at which the small signal current gain expressed in terms of H_{21} parameter falls to unity or 0dB [90]. The current gain is derived from the transistor S-parameters as follows [91]:

$$|H_{21}| = \left| \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \right| \tag{2.7}$$

f_{MAX} is called the maximum oscillation frequency and is defined as the frequency at which the unilateral power gain (also called Mason Gain U=$\frac{|Y_{21}-Y_{12}|^2}{4(\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}]-\mathrm{Re}[Y_{12}]\mathrm{Re}[Y_{21}])}$) attains a value of 0 dB.

These parameters are approximately expressed as follows [92] [93] [94] [91]:

$$f_T \approx \frac{g_m}{2\pi C_{gg}} \tag{2.8}$$

$$f_{MAX} = \frac{f_T}{2\sqrt{g_{ds}(R_G+R_S)+2\pi f_T R_G C_{gd}}} \tag{2.9}$$

$$\approx \sqrt{\frac{f_T}{8\pi R_G C_{gd}}} \tag{2.10}$$

$$f_{MAX} = \frac{1}{2}\frac{f_T}{\sqrt{2\pi f_T C_{gd} R_G + \frac{R_G}{r_0}}} \tag{2.11}$$

The values of f_T and f_{MAX} can be extracted by extrapolating the plots of H_{21} and U respectively to 0dB at V_{ds}=1V and V_{gs} that corresponds to maximum transconductance g_m [95] [92]. In regions where the H_{21} (in dB) or U (dB) falls at a rate of -20dB/decade, the parameters f_T and f_{MAX} can be calculated as:

$$f_T = mag(H_{21}) \cdot f \tag{2.12}$$

$$f_{MAX} = \sqrt{U} \cdot f \tag{2.13}$$

The other transistor parameters of interest are R_{gg}, the gate resistance, g_m, the transconductance and C_{gg} the gate capacitance which are calculated as given in equations 2.14, 2.15 and 2.16.

$$R_{gg} = real(\frac{1}{Y_{11}}) \tag{2.14}$$

$$C_{gg} = -\frac{imag(1/Y_{11})^{-1}}{2\pi f} \tag{2.15}$$

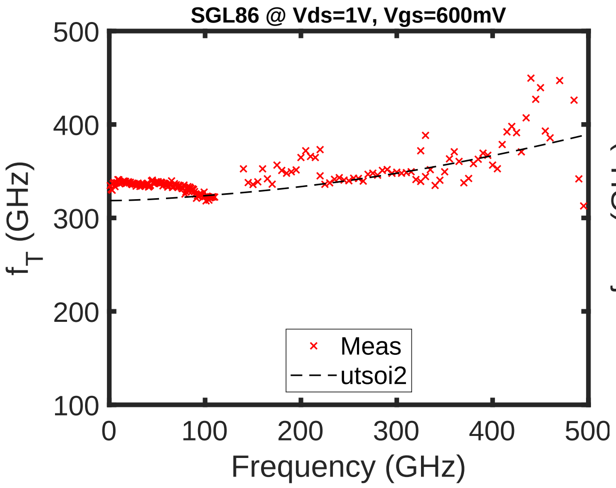


Figure 2.25: f_T of transistor

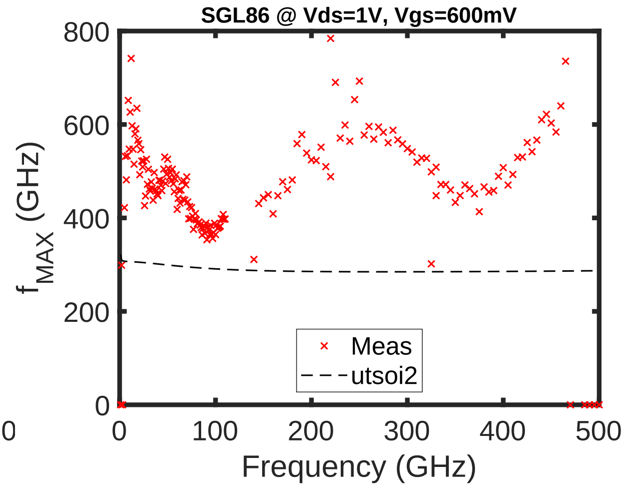


Figure 2.26: f_{MAX} of transistor

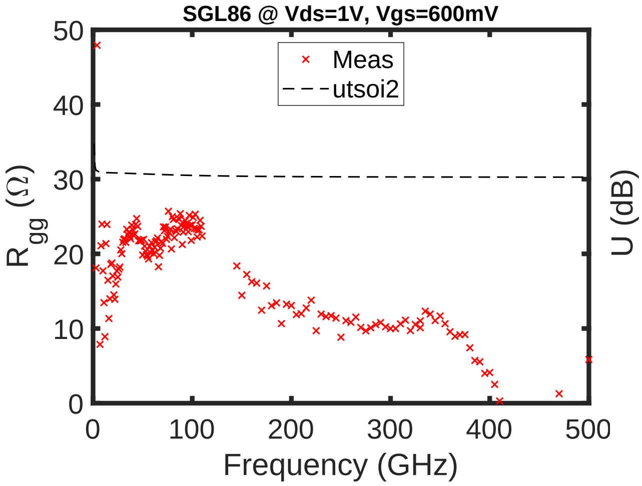


Figure 2.27: Gate resistance of transistor

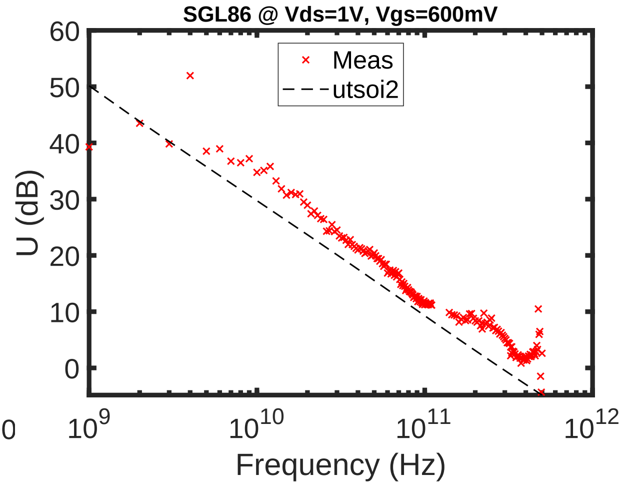


Figure 2.28: Mason Gain in dB vs frequency

$$g_m = real(Y_{21} - Y_{12}) \tag{2.16}$$

These parameters are first compared to the UTSOI2[96] compact model of FDSOI. The UTSOI2 model parameters have been, however, optimized according to the off-wafer measurements performed on another wafer before the start of this thesis work. As evident from figures 2.25 - 2.28, there exists a considerable mismatch in some transistor parameters, between the existing model and the measurements obtained by on-wafer TRL. This is probably due to inconsistency in the on-wafer TRL measurement, introduced by the non-ideal Lines layout due to tiling. f_{MAX} is a very sensitive metric and its extraction may be affected by any small inaccuracy in all the measured S-parameters. In order to pursue the setting-up of our methodology of measurement validation by EM simulation, a small-signal equivalent circuit has been extracted to match the measured Transistor under test with on-wafer TRL calibration. This extraction has been performed using the measurements from 1-110 GHz and its validity upto 500 GHz is verified by comparing with the measurements from the higher frequency bands.

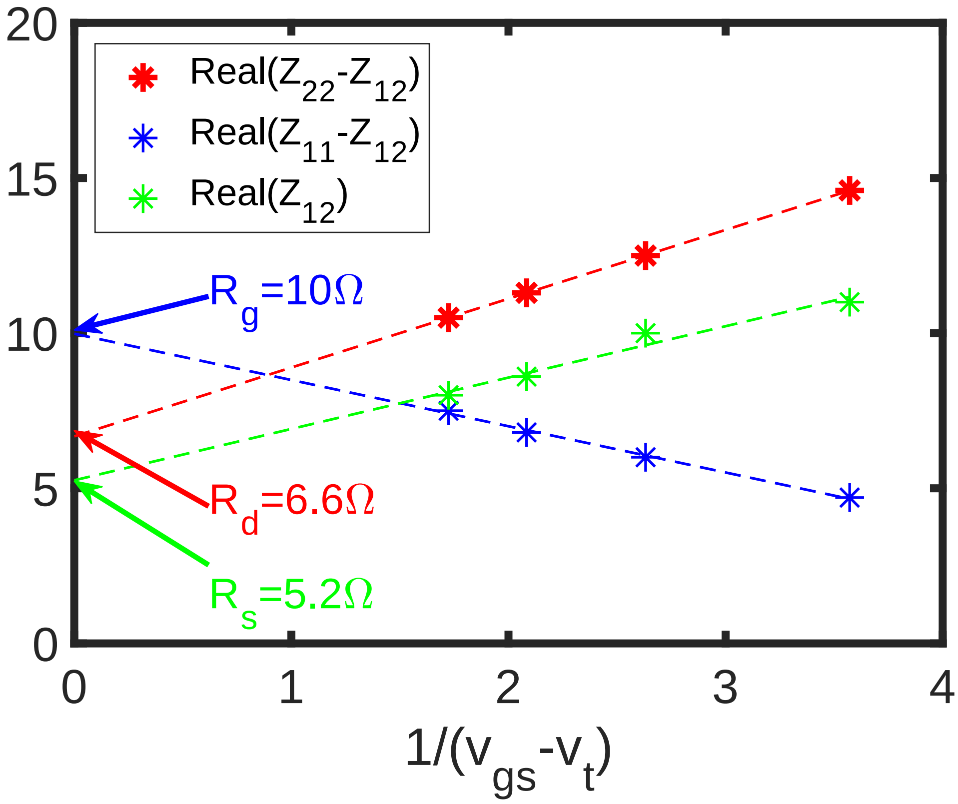


Figure 2.29: Extraction of extrinsic parameters at 50 GHz for small signal model

2.4 Extraction of Small Signal Equivalent Circuit

For the extraction of the SSEC, the circuit as represented in Fig. 2.30 is used. The transconductance element g_m in the model can have a frequency dependence in the form of $g_m = g_{m0} \cdot e^{-j\omega\tau}$. The extrinsic series parameters, R_g, R_d and R_s are first extracted using the Bracale method [97] [98]. The transistor is considered at cold bias or zero drain bias (V_{ds} = 0) for the extrinsic parameter extraction. The intrinsic parameters R_i and τ correspond to the second-order effects at high frequencies. These are set to zero for the parameter extraction. The curves $Re(Z_{12})$, $Re(Z_{22} - Z_{12})$ and $Re(Z_{11} - Re(Z_{12}))$ are plotted as a function of $1/(V_{gs} - V_t)$, where Z_{ij} corresponds to the transistor Z-parameters, and V_t is the threshold voltage. It has been shown in [97] that the Y intercepts of these curves are respectively R_s, R_d and R_g. The linear regression curves for these parameters are illustrated in Fig. 2.29.The resistance values obtained from the intercepts are listed in Table 2.3.

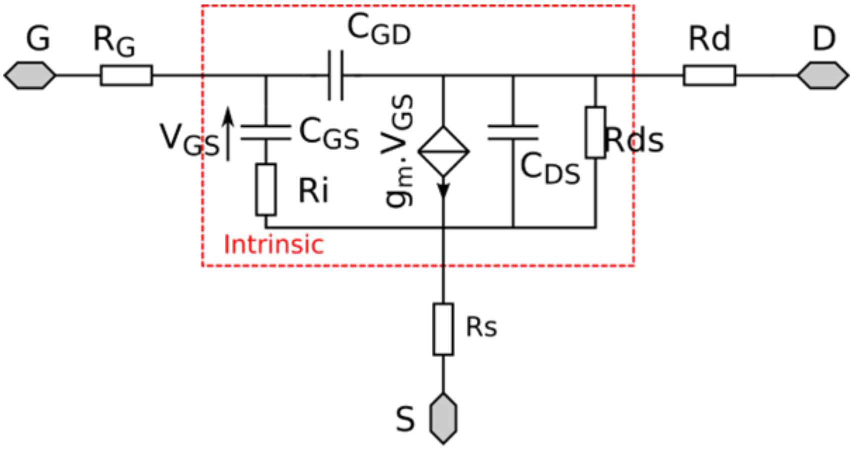


Figure 2.30: Small Signal Equivalent Circuit of Transistor

Table 2.3: SSEC parameter values

Parameter	Value
R_g	10 Ω
R_d	6.6 Ω
R_s	5.2 Ω
C_{gs}	10.5 fF
C_{gd}	3.7 fF
C_{ds}	2.5 fF
R_{ds}	590 Ω
R_i	5 Ω
g_{m0}	32.85 mS

This is followed by the extraction of the intrinsic elements (shown within the dotted box in Fig. 2.30). The parasitics of the extrinsic elements can be removed from the model by subtracting the corresponding Z-parameters. Now, the behaviour of the remaining intrinsic elements, neglecting the effects of R_i and τ, can be expressed by the Y parameter matrix in eqn. 2.17.

$$[Y_{intrinsic}] = \begin{bmatrix} j\omega C_{gs} + j\omega C_{gd} & -j\omega C_{gd} \\ g_m - j\omega C_{gd} & j\omega C_{ds} + j\omega C_{gd} + 1/R_{ds} \end{bmatrix} \tag{2.17}$$

From this, the parasitic elements are calculated as:

$$g_m = real(Y_{21}) \tag{2.18}$$

$$C_{gd} = -imag\left(\frac{Y_{12}}{\omega}\right) \tag{2.19}$$

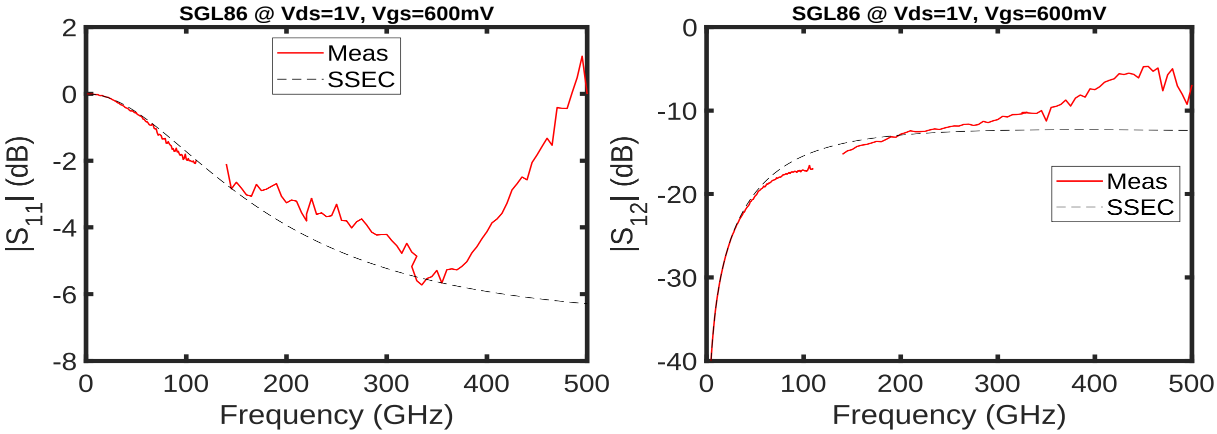
$$C_{gs} = \frac{imag(Y_{11} + Y_{22})}{\omega} \tag{2.20}$$

$$C_{ds} = \frac{imag(Y_{22} + Y_{12})}{\omega} \tag{2.21}$$

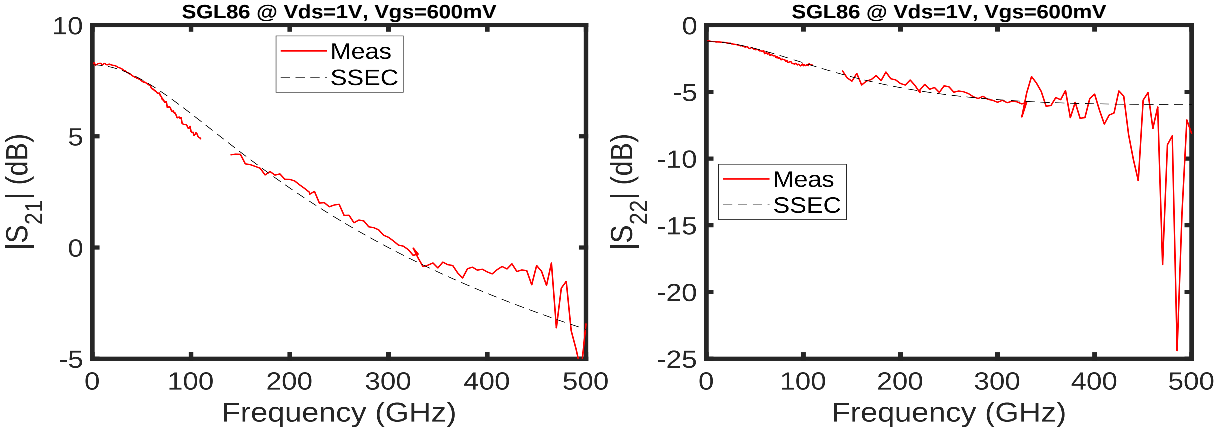
$$R_{ds} = \frac{1}{real(Y_{22})} \tag{2.22}$$

For the extraction of the frequency dependence of g_m, it has been observed from the measurements that the value of τ is quite negligible and can be ignored. The values of all the elements thus obtained are tabulated in Table 2.3. This small signal model of the transistor is simulated from 1- 500 GHz and comparison is made with the measurement results. Fig. 2.31 makes a comparison of the calibrated S-parameters from measurements and the S-parameters from the simulation of the small signal model. Also plotted are the transistor parameters $f_T, f_{MAX}, R_{gg}, C_{gg}$ and g_m in Fig. 2.32.

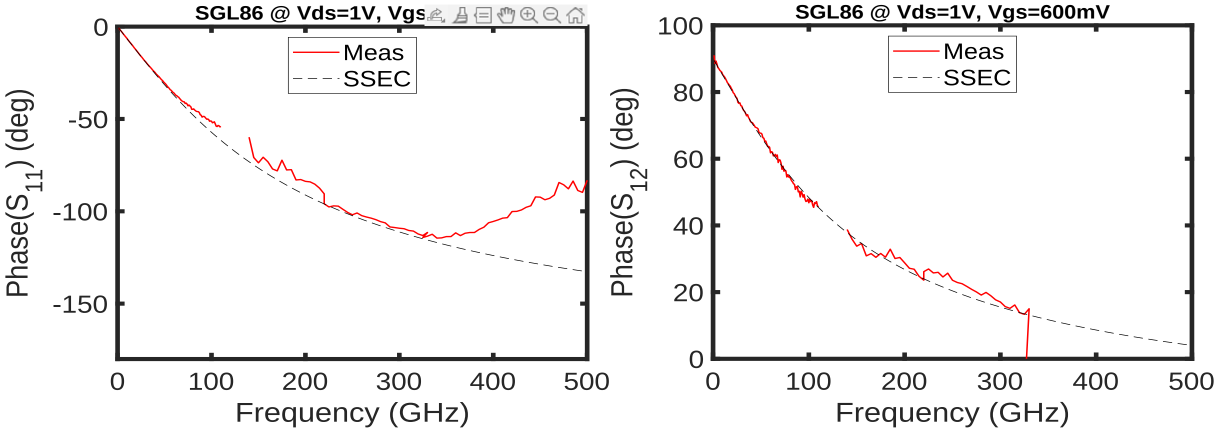
It is evident from Figures 2.31 and 2.32 that there is a good agreement between the values extracted from the small signal model and the measured values at the least until 350 GHz. This validates the extracted small signal model extraction. Major deviations from the model



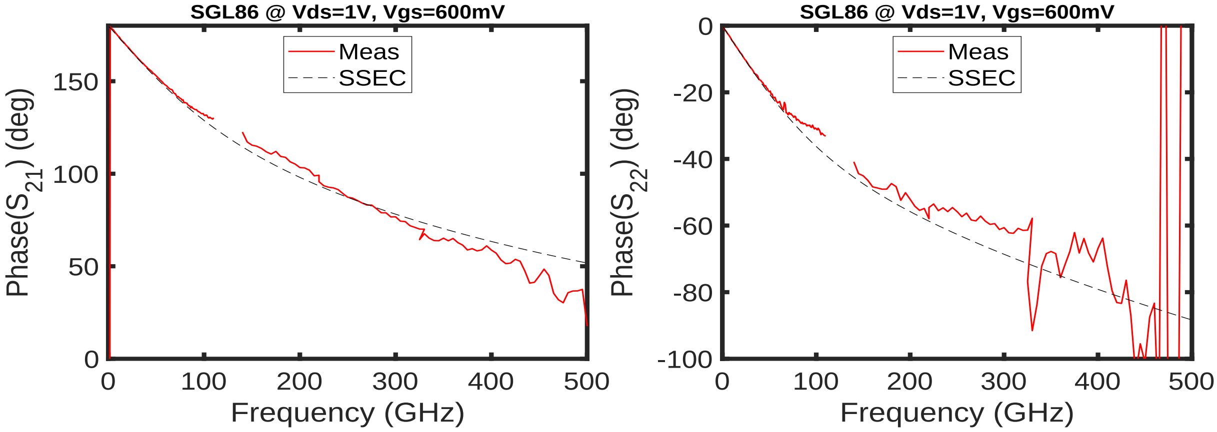
(a) $|S_{11}|$ in dB (b) $|S_{12}|$ in dB



(c) $|S_{21}|$ in dB (d) $|S_{22}|$ in dB

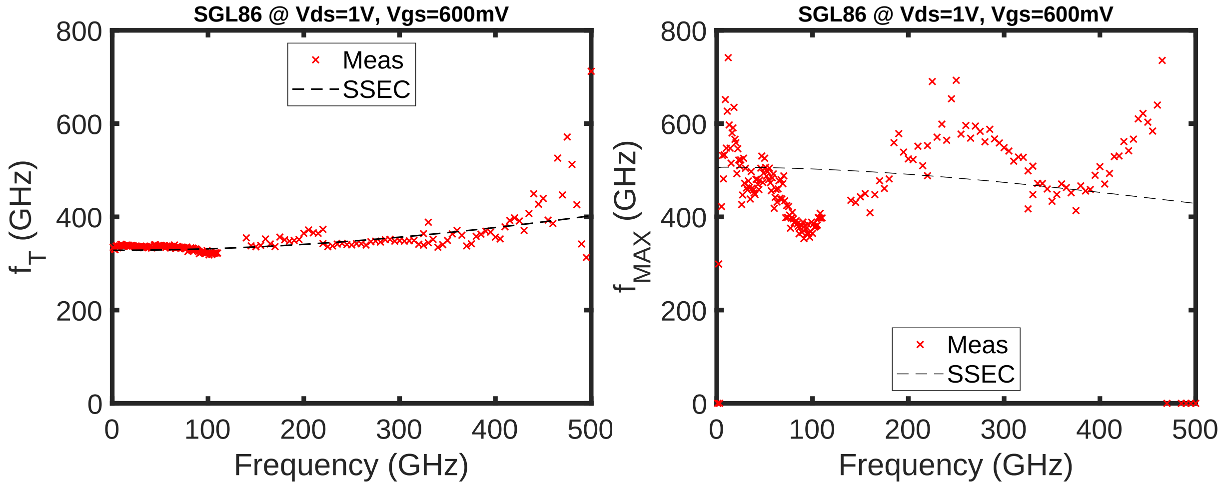


(e) $\angle S_{11}$ in degrees (f) $\angle S_{12}$ in degrees

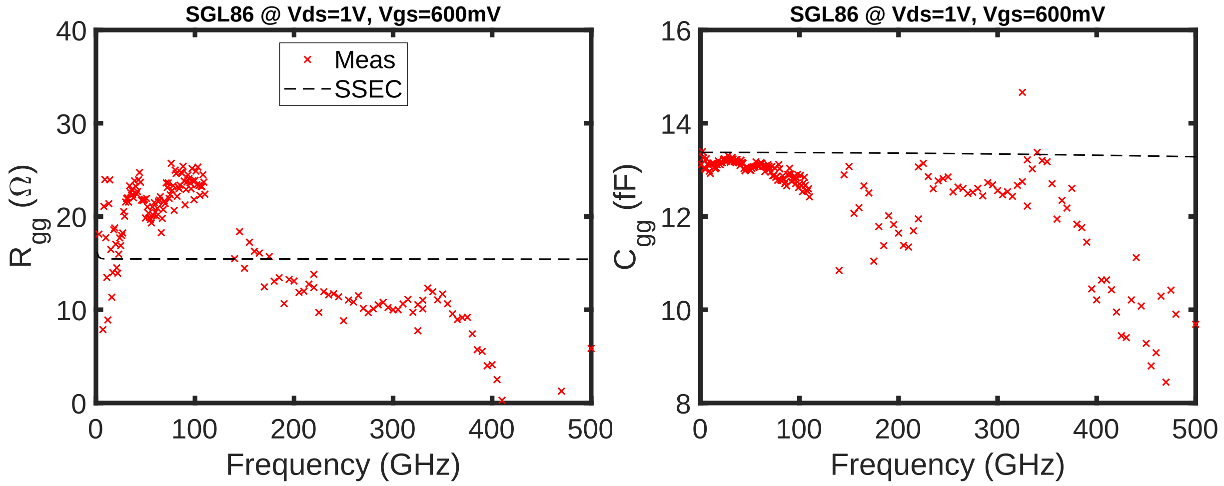


(g) $\angle S_{21}$ in degrees (h) $\angle S_{22}$ in degrees

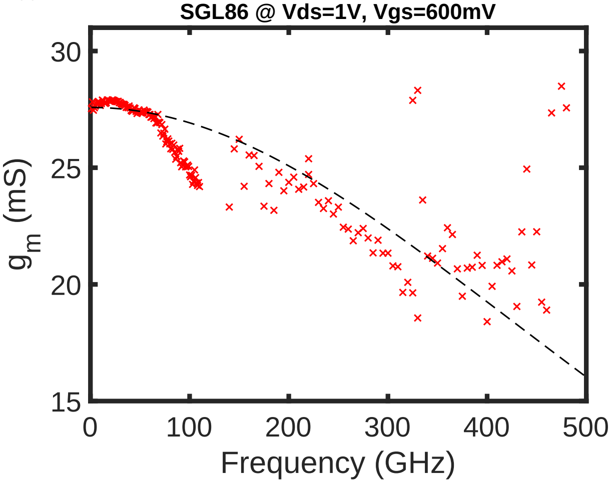
Figure 2.31: S parameters of transistor from measurements compared to the SSEC



(a) f_T (b) f_{MAX}



(c) R_{gg} (d) C_{gg}



(e) g_m

Figure 2.32: Measured transistor parameters compared to the values obtained from SSEC simulation

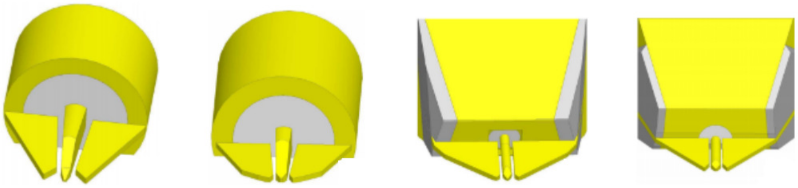


Figure 2.33: 3D models of the picoprobe RF probes in each frequency band

values are seen above 350 GHz. This is mainly due to the tiling in the lines that reduces the TRL calibration limit, and thus the measurements above 350 GHz are not accurate enough as already discussed in the previous sections. The minor fluctuations from the model can be attributed to the effect of the measurement environment, specifically the measurement setup including the RF probes.

The small signal equivalent circuit only models the intrinsic behaviour of the transistor and thus the analysis of the effects of measurement environment is not possible using this model. Therefore we make use of the EM simulations to have a better understanding of these effects and find ways to overcome the difficulties.

2.5 Comparison of measurement results with EM simulation and transistor model simulation

In order to simulate the measurements along with the measurement environment effects, an EM co-simulation is performed to simulate the complete TRL calibration procedure [15] [78]. This is done by making use of the probe models for each frequency band [75]. Fig. 2.33 shows the 3D model of the RF probes used for EM simulation in HFSS.

2.5.1 Methodology for the full EM simulation including probes

The flowchart that presents the steps adopted for the complete EM simulation of TRL calibration is given in Fig. 2.34.

The models of all the test structures and DUTs are created in HFSS as already described in Chapter 1. For the Line_110G and Line_500G, the model is created using the hybrid oxide to account for the tiling. In regions where the tiling is present, the hybrid oxide is made use of, whereas the actual oxide material is used in the other regions. To simulate the transistor, the intrinsic part of the transistor is modeled using the SPICE simulation of the small signal model. The passive parts (BEOL, access lines, probe pads) of the transistor DUT are modeled using HFSS. The two models are combined using IC-CAP simulation. This combined simulation is called co-simulation.

An example of 3D model used for EM simulation is also shown in the flowchart in Fig. 2.34.

2.5.2 Validation of Short-Open de-embedding method up to 500 GHz

As the first step, the de-embedding test structures (Transistor Open and Transistor Short) are simulated with the probe models, and TRL calibration is performed on these. The resulting

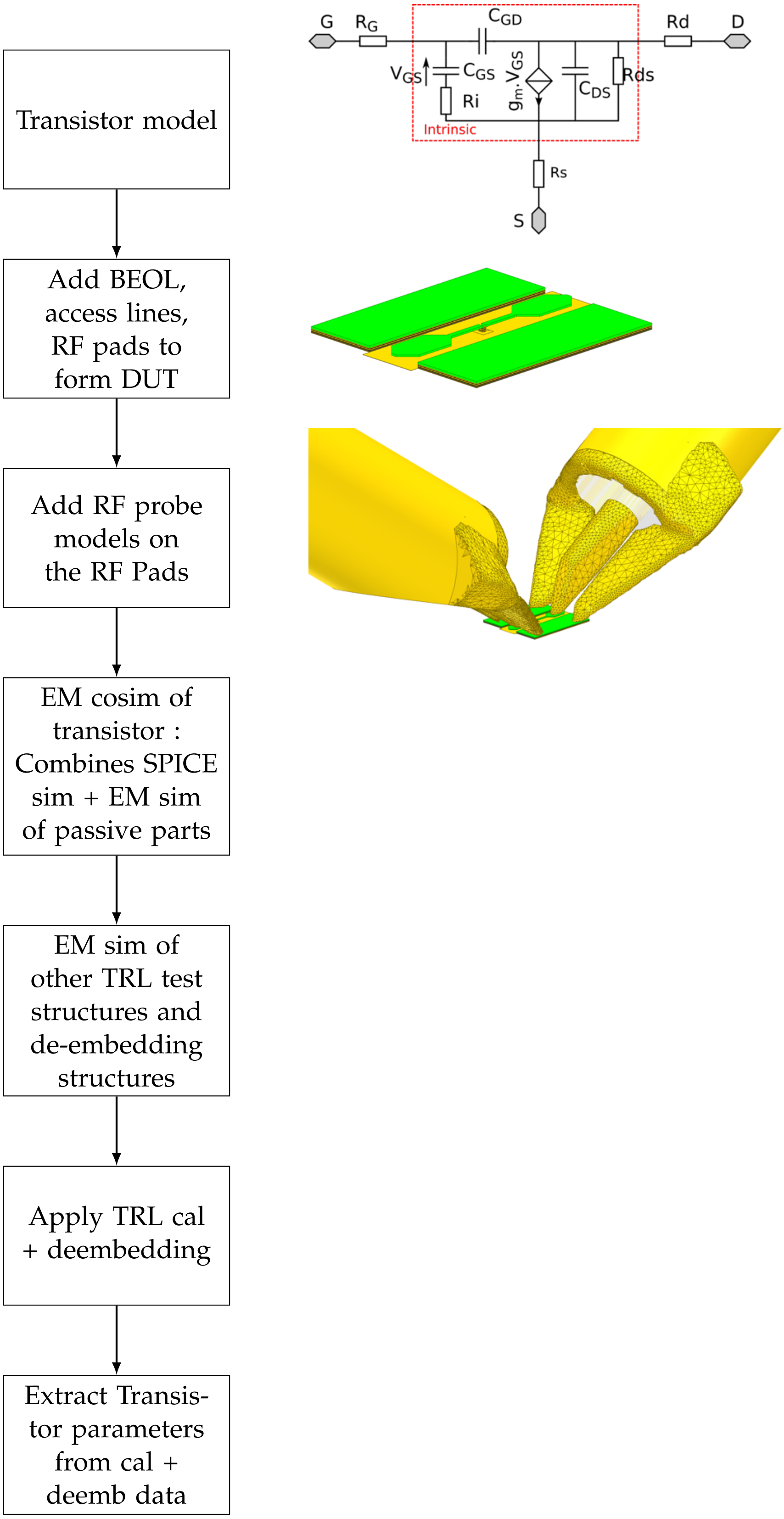


Figure 2.34: Procedure followed for the EM co-simulation of transistor to simulate the TRL calibration

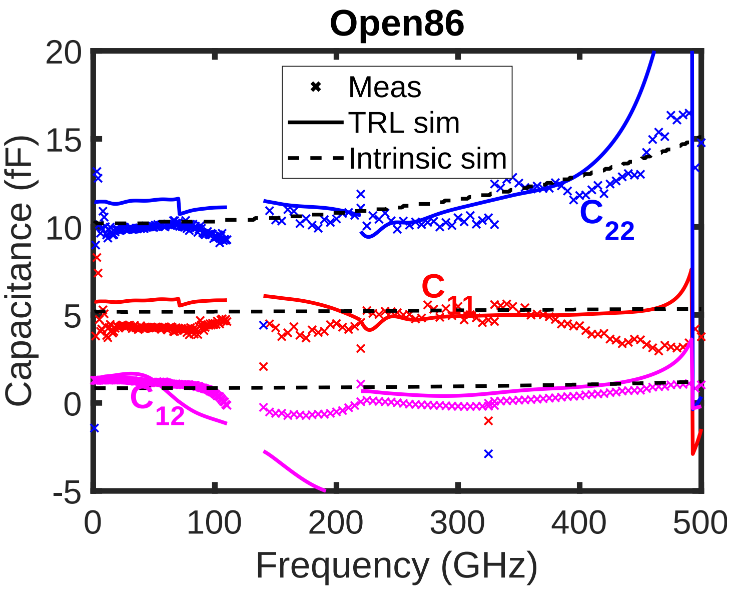
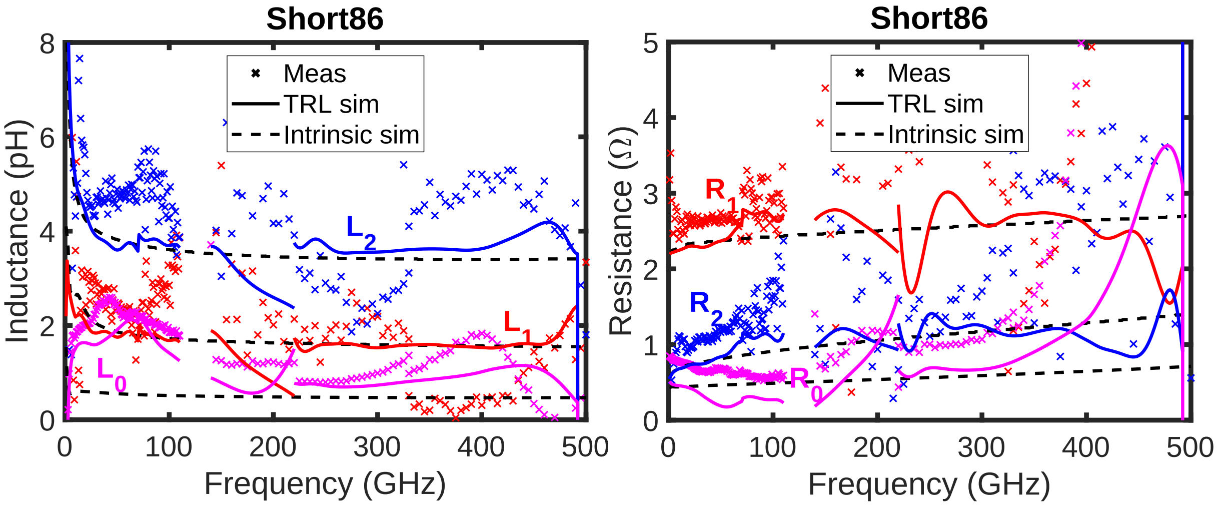


Figure 2.35: Capacitances of Transistor Open extracted from EM simulation compared to the measurements

S-parameters of the Open & Short are used to extract their lumped circuit parameters which are then compared to the values obtained from measurement and also to the values from their intrinsic simulation. In an ideal case, it is expected that the values from these three methods coincide. Fig. 2.35 makes a comparison of the capacitances of the Transistor Open (see Fig. 2.6 for the equivalent circuit) from all three methods. Also plotted in Fig. 2.36 are the inductances and resistances of the Transistor Short.

A reasonable agreement can be observed between the values obtained from measurements and EM simulation (intrinsic and TRL). Most of the measurement trends are also well reproduced by the EM simulation. However, a small deviation and change in measurement trend is evident in the 140-220 GHz frequency range. This is due to the fact that the actual measurements have been performed using the Infinity Probes whereas the EM simulation of TRL has been done using the 3D models of Picoprobes. At the time of carrying out the EM simulation, the 3D models of the Infinity Probes were unavailable, and therefore TRL measurements were simulated using the available probe model. This has led to the different trend observed in the EM simulation, as the electromagnetic fields interact differently depending on the probe type.

In spite of this difference, it is seen that the extracted lumped element values of the Open and Short are more or less constant with respect to frequency upto 500 GHz for the Short and upto 400 GHz for the Open. This affirms the validity of the lumped model used to represent these de-embedding structures, and thus the validity of the Short-Open de-embedding method adopted in this work. However, it has been observed that the measurements on the Transistor Short test structure are quite difficult as it is prone to unwanted noise. As can be seen from the measurement plots in Fig. 2.36, a +/- 1pH uncertainty is observed, which is in the range of the measurement noise. This uncertainty has been observed even after repeated measurements on the structure. Thus the lumped element values extracted from measurements vary greatly with frequency above 350-400 GHz, trends which are reproduced by the EM simulation as well. In effect, it can be said that the Short-Open de-embedding method can be used with confidence upto 400 GHz. At the moment, this is not a cause of concern as the TRL calibration kit being used is valid only until 400 GHz due to the limitation of the Lines.



(a) Inductance of Short (L)

(b) Resistance of Short (R)

Figure 2.36: Results of EM simulation of Transistor Short compared to the measurements

Intrinsic cosimulation

Now that the validity of the de-embedding model is established, it is quite straightforward to demonstrate the de-embedding process on the transistor without considering the effects of TRL calibration. In order to do this, an intrinsic transistor (transistor model + metal stack upto LB layer) is simulated in HFSS. This simulation is termed intrinsic co-simulation. Also performed are the intrinsic simulations of the Transistor Open and Transistor Short. The simulated S-parameters of these models are used to realize the Short-Open de-embedding on the transistor. A summary of the steps involved in the intrinsic co-simulation is presented in Fig. 2.37.

The resultant transistor parameters (f_T, f_{MAX}, R_{gg}, $|S_{21}|$) after intrinsic co-simulation are plotted in Fig. 2.38 and compared to the values from the simulation of the small signal model. It is quite evident from these plots that the results are in excellent agreement with the transistor model, which reaffirms the reliability of the Short-Open de-embedding process upto 500 GHz.

2.5.3 Results of TRL calibration using EM cosimulation

The actual on-wafer measurements are affected by several factors, mainly the effects due to the measurement environment. These involve field coupling effects, effects of RF probes, effects of neighbouring on-wafer structures, effect of calibration methods and so on. Here TRL calibration is performed after utilizing the technique of EM co-simulation so that the effects of probes, and coupling can be analysed. The methodology has already been discussed using Fig. 2.34.

The transistor parameters extracted from this method are compared to the parameters extracted from the small signal model of the transistor. For a calibration method that is capable of eliminating all types of errors, the parameters extracted from the EM simulation will be exactly the same as those from the small signal model. In addition these values are also compared to the actual measurement results. The measurements are represented by symbols and the EM co-simulation results by solid lines. The small signal model is plotted using black dotted lines.

The RF FoMs of the transistor thus obtained are plotted in Fig. 2.39. An excellent agreement between the plots is observed in Fig. 2.39b for f_T. The measured f_{MAX} shows an oscillating trend

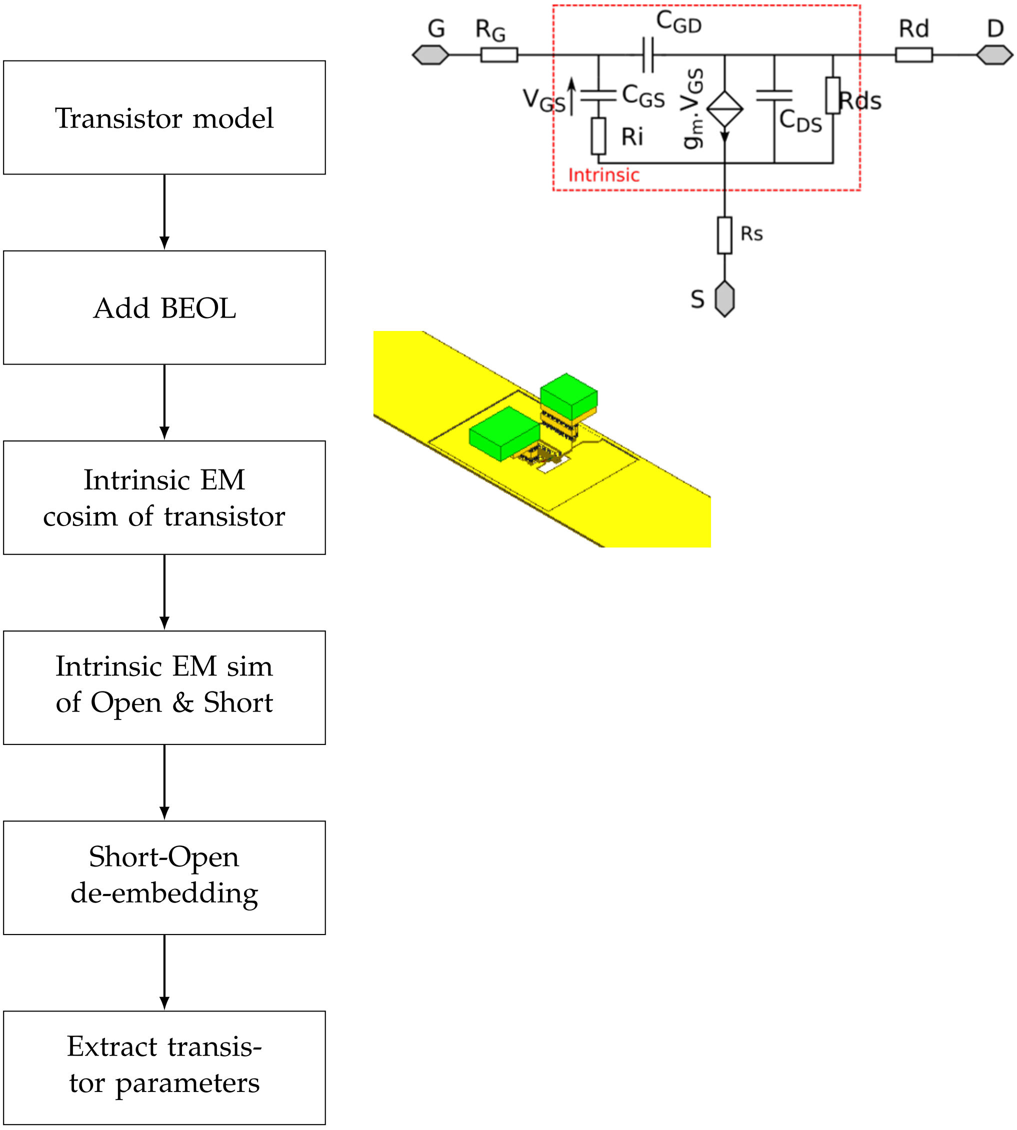
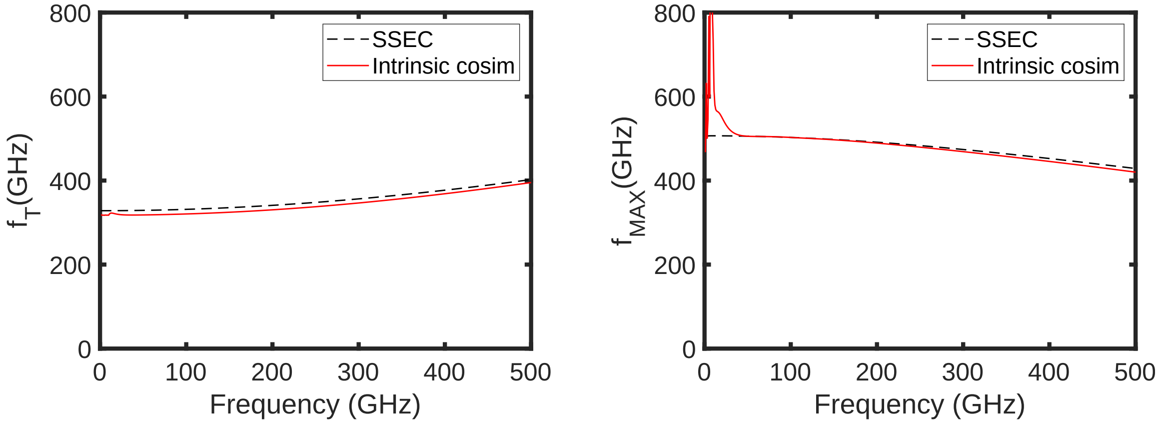
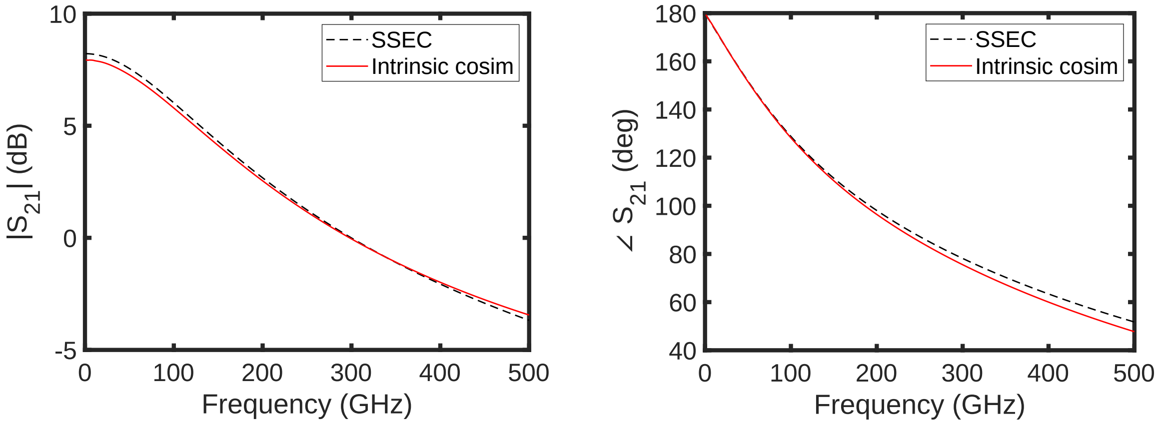


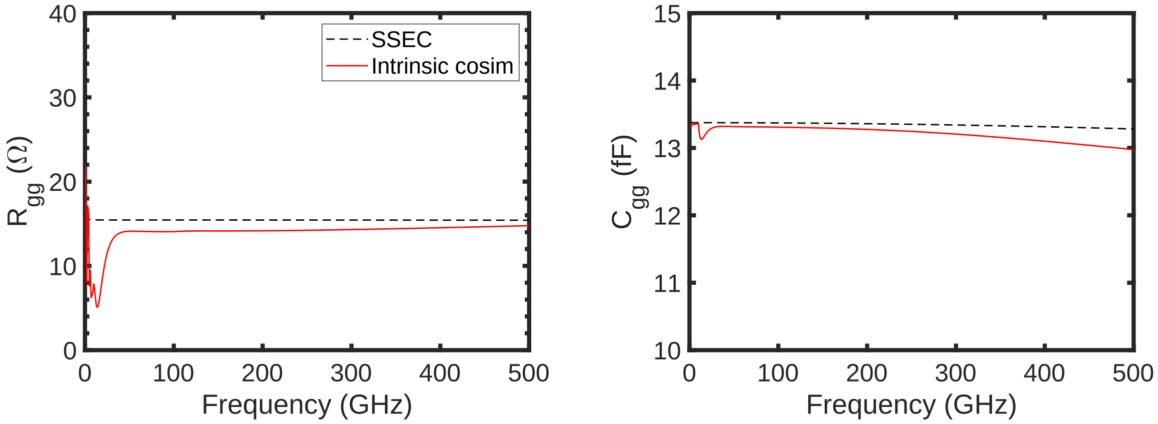
Figure 2.37: Steps followed for Intrinsic EM Co-simulation



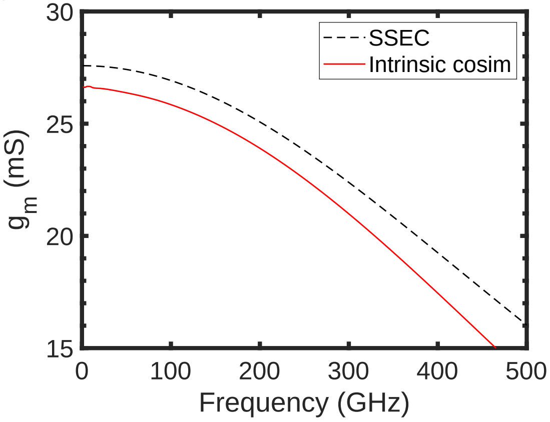
(a) f_T (b) f_{MAX}



(c) $|S_{21}|$ in dB (d) $\angle S_{21}$ in degrees

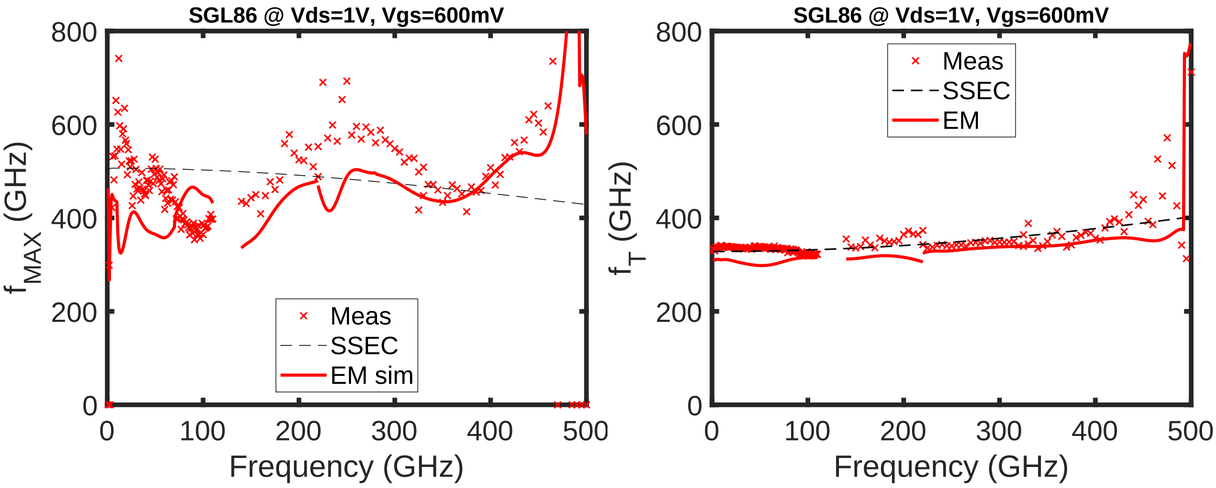


(e) R_{gg} (f) C_{gg}



(g) g_m

Figure 2.38: Intrinsic cosimulation of transistor compared with the SSEC to demonstrate the validity of de-embedding



(a) f_{MAX} (b) f_T

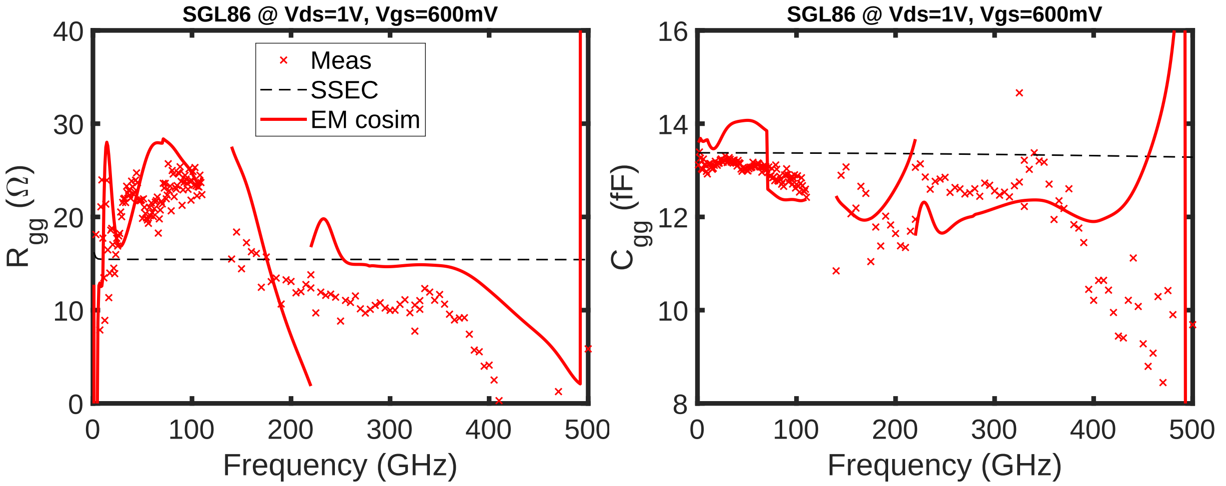
Figure 2.39: Transistor RF FoMs from EM cosimulation of TRL calibration compared to the measurement results

with frequency, with an average value of around 500 GHz. This trend, which is not predicted by the small signal model, has however been captured well by the EM simulations. This leads to the hypothesis that the f_{MAX} measurements are severely impacted by the calibration procedure and/or the measurement environment. Moreover, the f_{MAX} measurements are seen to be extremely noisy in the first frequency band (1-110 GHz) and it is difficult to make a reliable estimate of this parameter at low frequencies.

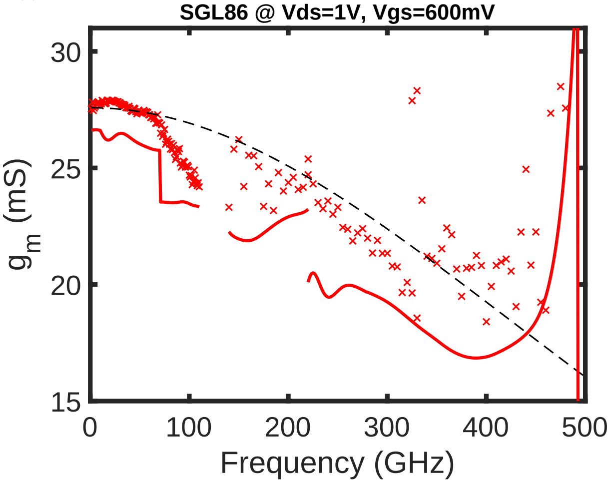
The other transistor parameters viz., the gate resistance R_{gg}, gate capacitance C_{gg} and transconductance g_m are plotted in Fig. 2.40. It can be inferred from these plots that the ambiguities in the measured values are due to the effect of the environment of the measurement setup, as the EM simulation is capable of reproducing most of the measurement trends. As has already been discussed in the previous sections, the TRL calibration is valid only upto a frequency of 400 GHz and hence the deviations in the plots after this point are a result of incorrect calibration (which is expected).

A significant point to be recalled here is that the behaviour of the Thru and Line test structures are not exactly identical as a result of the automatic tiling in the Lines. This leads to a minor error in the calibration results due to the change in the effective dielectric constant $\epsilon_{r,eff}$ between test structures, as already discussed in the beginning of this chapter.

Also plotted in Fig. 2.41 and Fig. 2.42 are the Y parameters (real and imaginary) and S parameters (magnitude and phase) respectively of the transistor obtained from EM co-simulation and compared to the measurements and the small signal model. As observed in the other transistor parameter plots, we see a good agreement between the values from the different methods. The only minor deviation notice is in the 140-220 GHz frequency band where the RF probe model used for EM simulation is different from the one used for actual measurements. Nevertheless, the EM co-simulation appears to be an efficient tool to validate the transistor's measurement by taking into account the impact of the measurement setups such as the effect of RF probes.

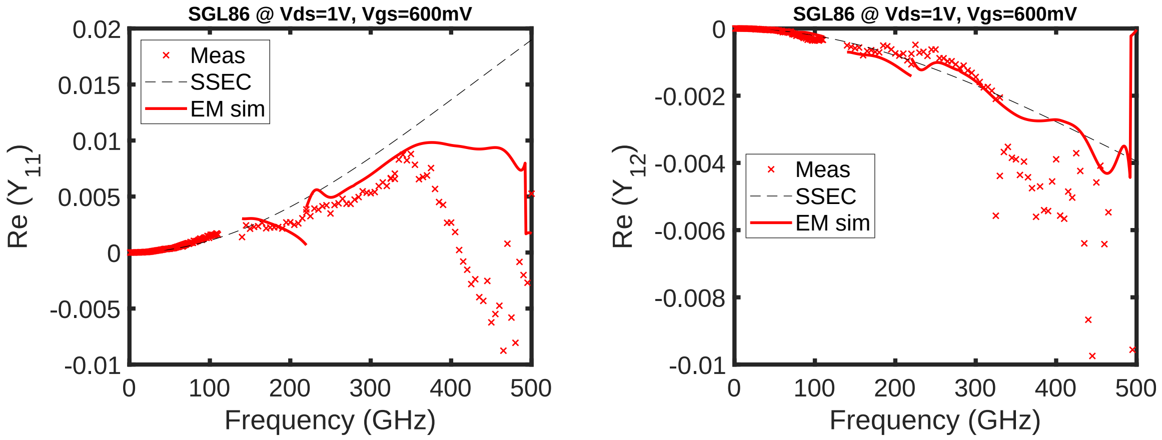


(a) R_{gg} (b) C_{gg}

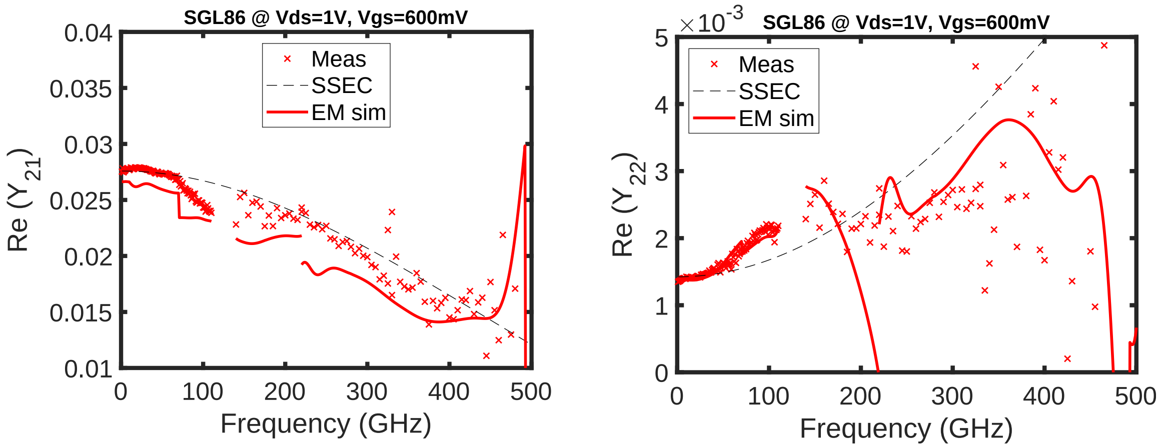


(c) g_m

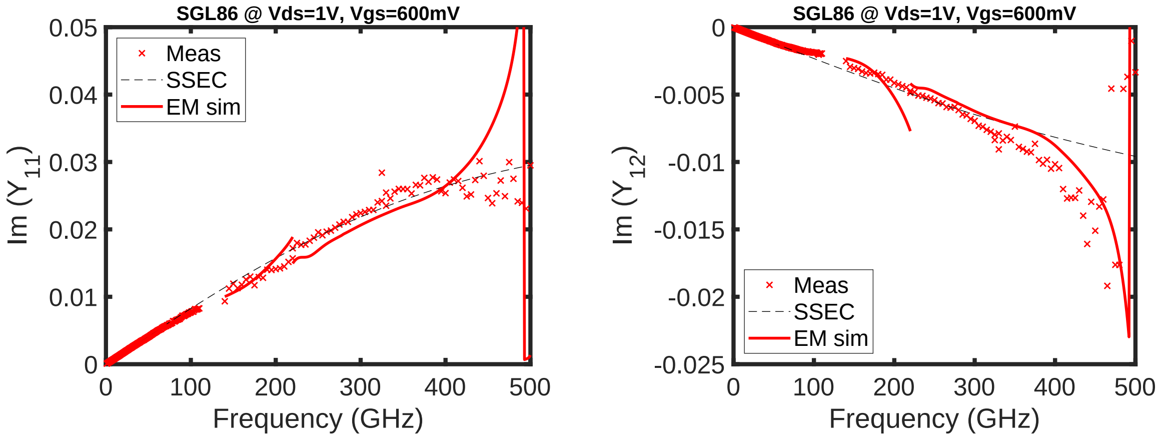
Figure 2.40: Transistor parameters extracted from EM co-simulation and measurements



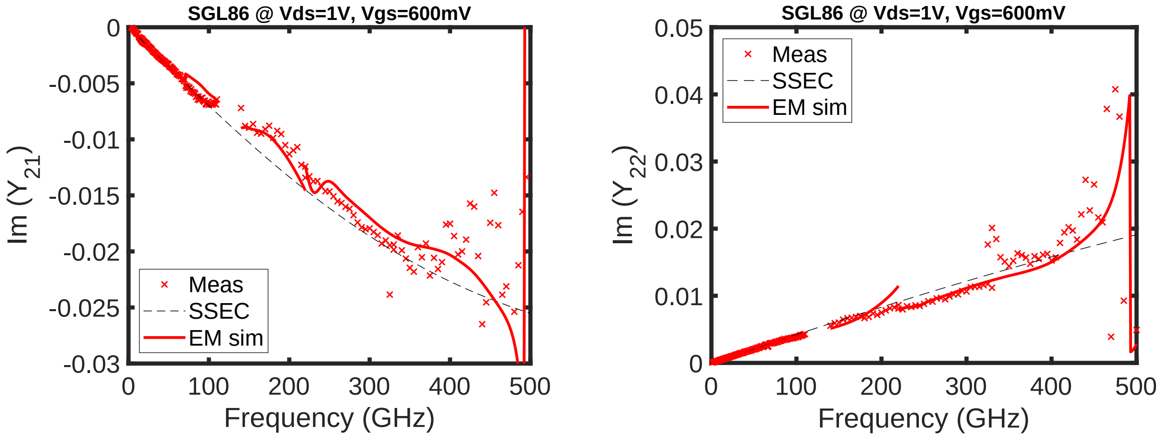
(a) Real(Y_{11}) (b) Real(Y_{12})



(c) Real(Y_{21}) (d) Real(Y_{22})

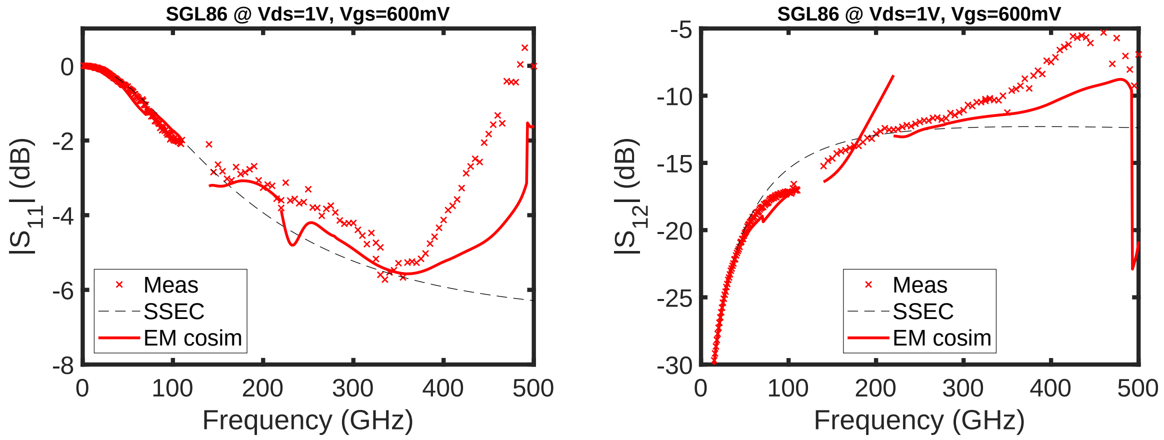


(e) Imag(Y_{11}) (f) Imag(Y_{12})

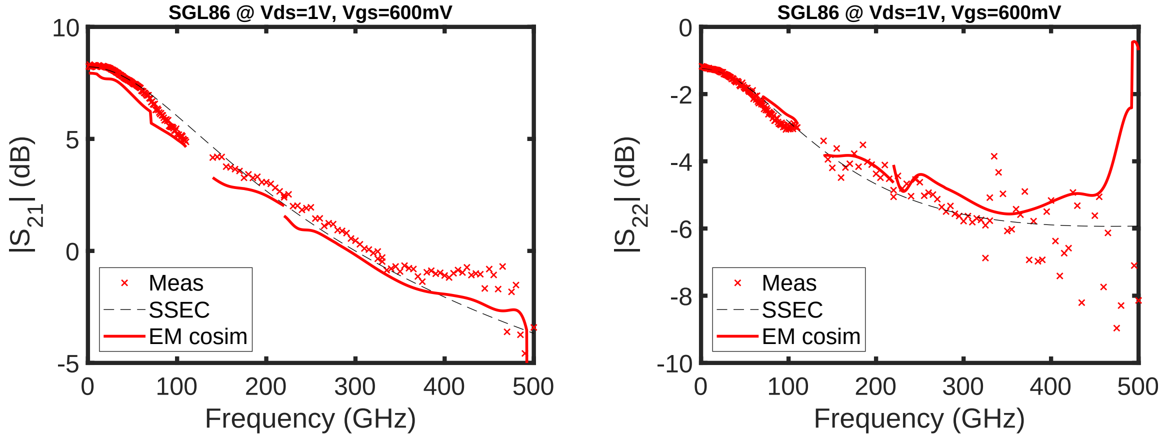


(g) Imag(Y_{21}) (h) Imag(Y_{22})

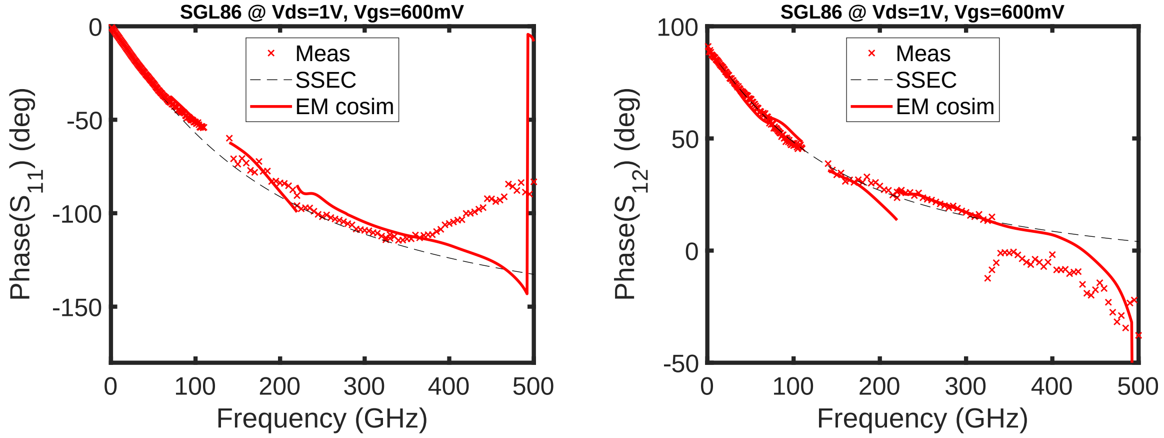
Figure 2.41: Y parameters of transistor extracted from EM co-simulation and from measurements



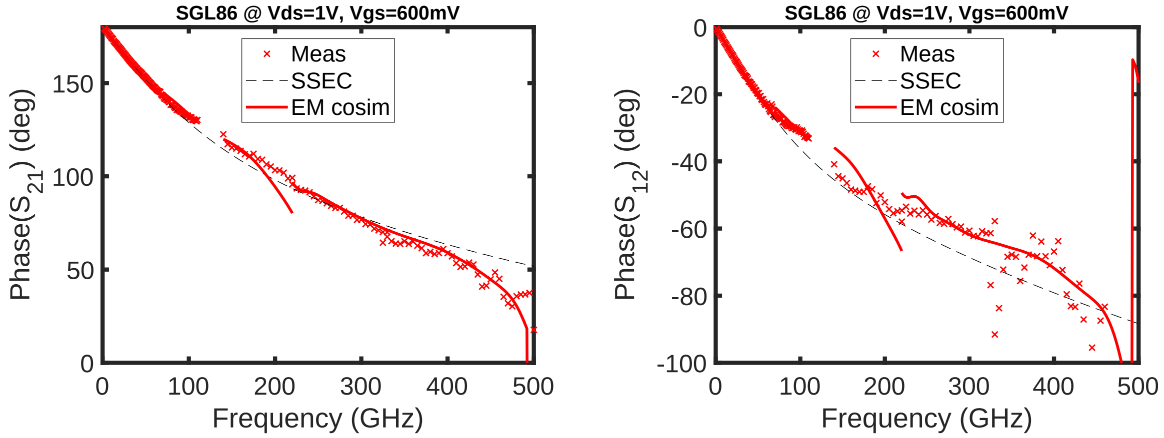
(a) $|S_{11}|(dB)$ (b) $|S_{12}|(dB)$



(c) $|S_{21}|(dB)$ (d) $|S_{22}|(dB)$



(e) Phase(S_{11}) (f) Phase(S_{12})



(g) Phase(S_{21}) (h) Phase(S_{22})

Figure 2.42: S parameters of transistor extracted from EM co-simulation and from measurements

2.6 Comparison between TRL and SOLT calibrations

From the preceding section it can been summarized that a good agreement exists between the measurement results with on-wafer TRL calibration, the EM simulation results and the small signal model, except for the discrepancies at the end of the last frequency band. However, it is worth characterising the same transistor using off-wafer SOLT calibration method, to investigate how the on-wafer TRL compares with the industrial standard for calibration. This comparison is made only in the frequency range of 1-110 GHz as the SOLT calibration is known to provide reliable results up to a maximum of 200 GHz [20] [29]. Both calibrations are performed using the same RF probe (Picoprobe). SOLT calibration however uses a Pad-Short-Open de-embedding method [29] in contrast to the Short-Open used after TRL calibration.

The transistor parameters extracted after each calibration are plotted in Fig. 2.43 to enable a comparison of the TRL and SOLT calibration methods. A significant difference observed between these two methods is the shift in f_{MAX} and R_{gg} values. The f_{MAX} extracted from SOLT calibration (≈400 GHz) is nearly 50-100 GHz lower than the value extracted using TRL (≈500 GHz). Similarly a difference of 10Ω is evident between the R_{gg} values extracted from TRL and SOLT. From Fig. 2.43b it can be inferred that the RF parameter f_T is not sensitive to the calibration method used. The other transistor parameters C_{gg} and g_m exhibit only a minor deviation (<10%) between the two plots above 60 GHz.

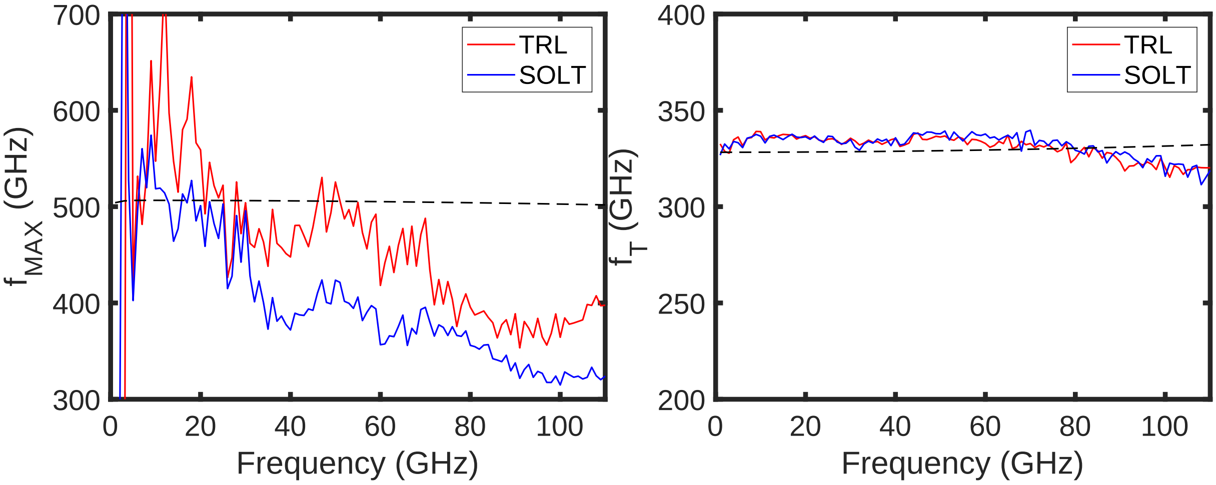
Also plotted in Fig. 2.44 are the Y parameters of the transistor contrasting the two calibration methods. Inconsistencies between the methods can be observed in the plots of Real(Y_{12}) and Imag(Y_{21}).

There are multiple reasons for this inconsistency. Firstly, the SOLT calibration is performed using standards made in ISS substrate (alumina), which is greatly different from the Silicon substrate of the transistor (DUT), thereby resulting in a different probe to substrate coupling in the SOLT standards and the DUTs [16]. This also means that the contact resistance at the probes is different as the probe is in contact with aluminium RF pads in DUTs, whereas the contact is made to gold in the ISS standards. Another possible reason is that the off-wafer SOLT calibration requires the parameters of the ISS standards (capacitance and inductance of the open and short respectively) [20]. This is often provided by the manufacturer as a frequency independent parameter, although some frequency dependence is observed.

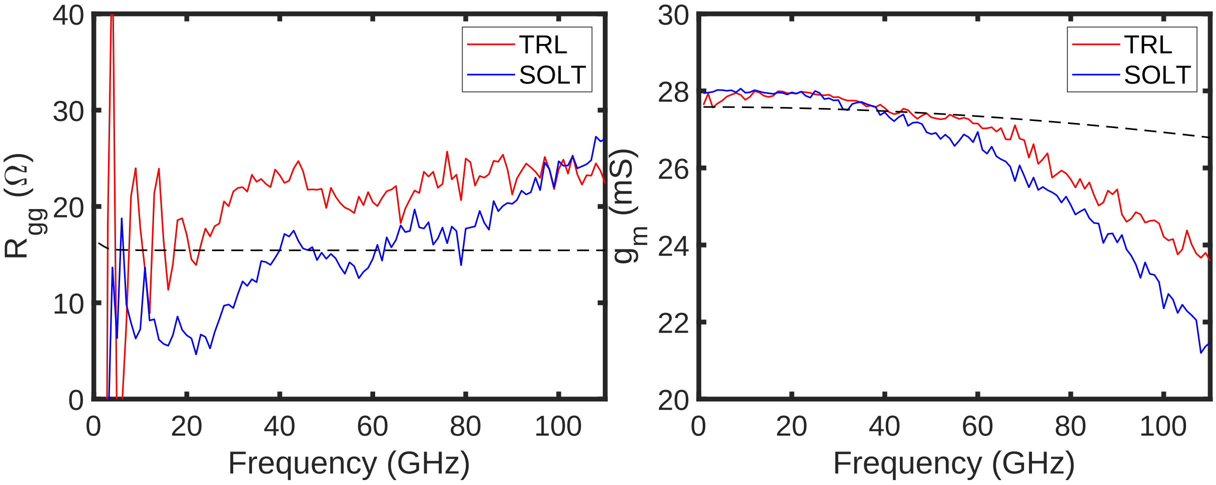
However as on-wafer TRL also has its own limitations, it is problematic to conclude definitively on the accuracy of either calibration method at this point. It is imperative to perform further investigations to clearly identify the ideal calibration method for sub-millimetre wave frequencies. In the next section, we make a further comparison by making use of two different RF probes to perform the calibrations.

2.7 Effect of RF probe used for measurement

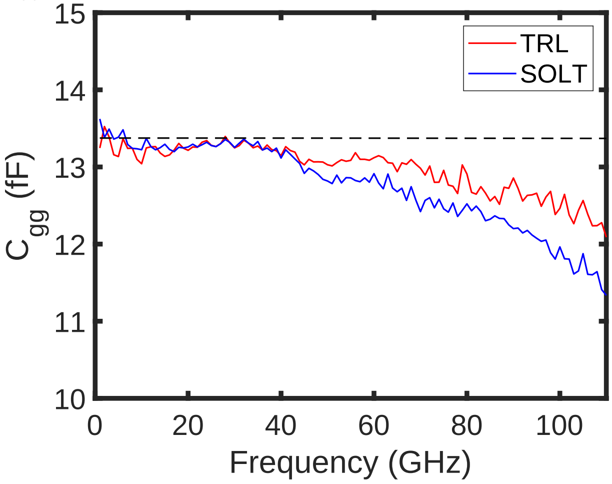
As we have just seen that there exists certain irregularities between the results obtained from two different calibration methods, it is important to investigate whether the results are equally affected by the measurement environment (here, the RF probes). The measurements were made with two different probes: the Cascade Infinity probes and the Picoprobe probes. Fig. 2.46 shows the photographs of the probes used for this measurement.



(a) f_{MAX} (b) f_T

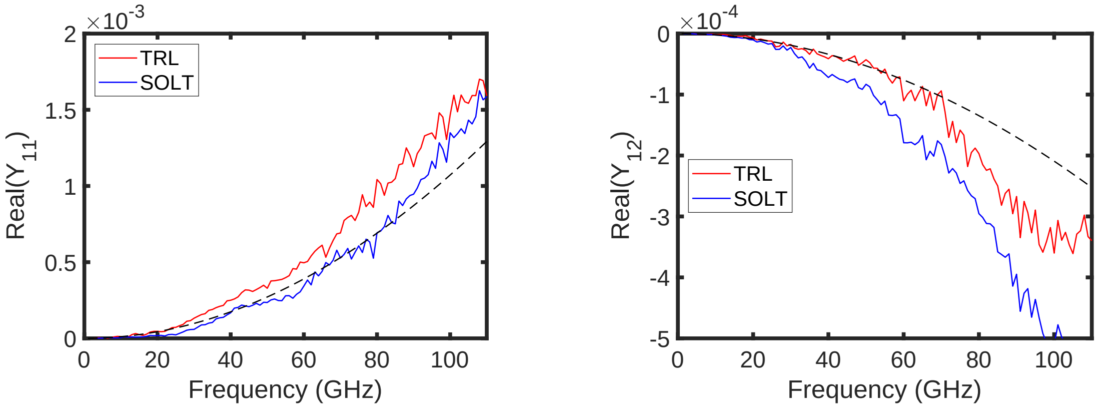


(c) R_{gg} (d) g_m



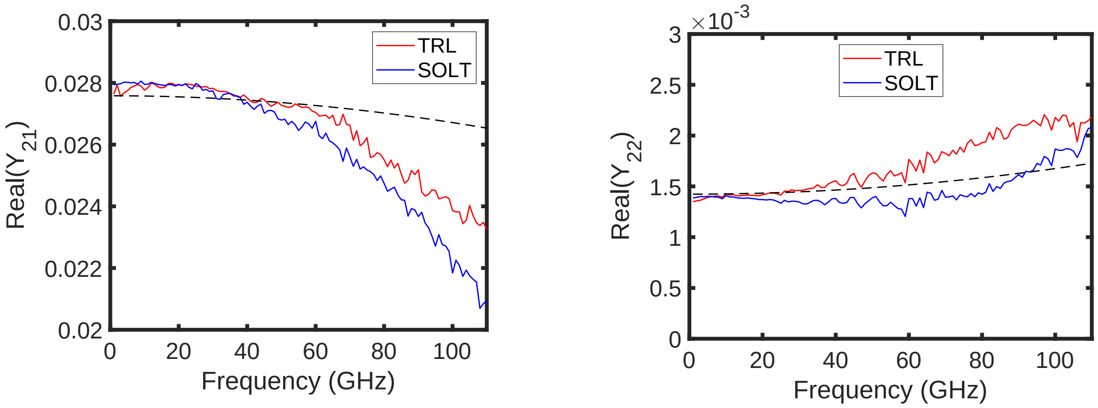
(e) C_{gg}

Figure 2.43: Comparison of on-wafer TRL with off-wafer SOLT calibration with respect to the extracted transistor parameters (The parameters from the small signal model are represented using black dotted lines for reference)



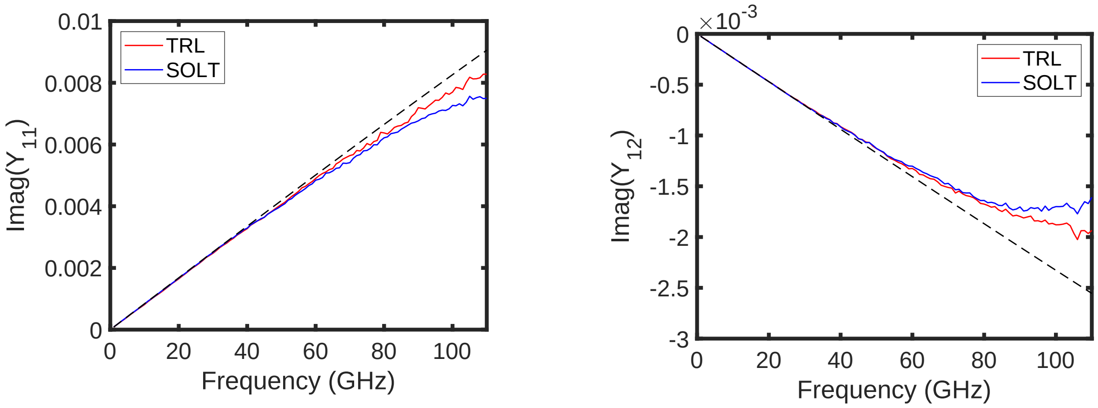
(a) Real(Y_{11})

(b) Real(Y_{12})



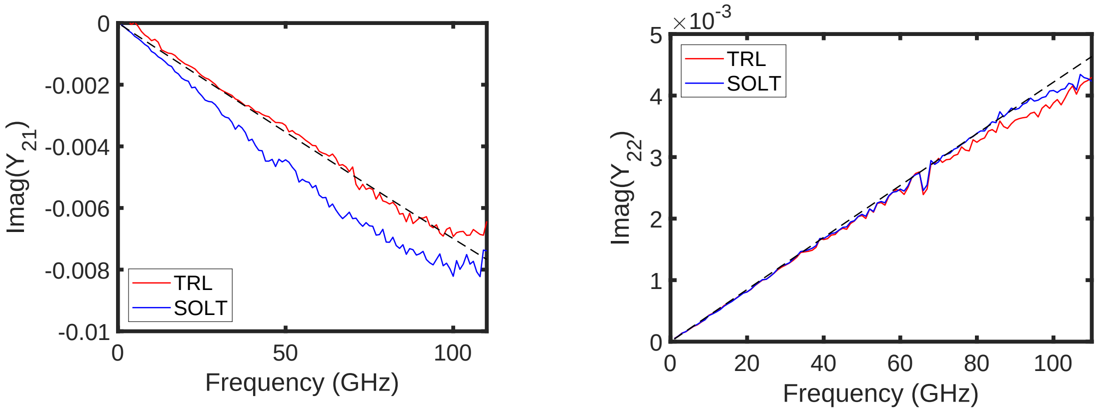
(c) Real(Y_{21})

(d) Real(Y_{22})



(e) Imag(Y_{11})

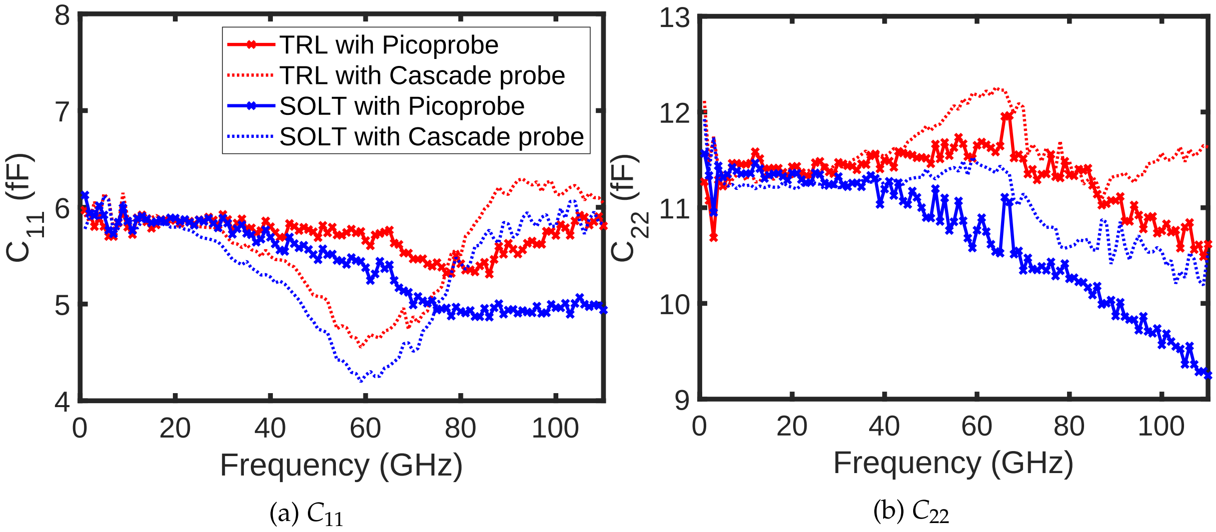
(f) Imag(Y_{12})



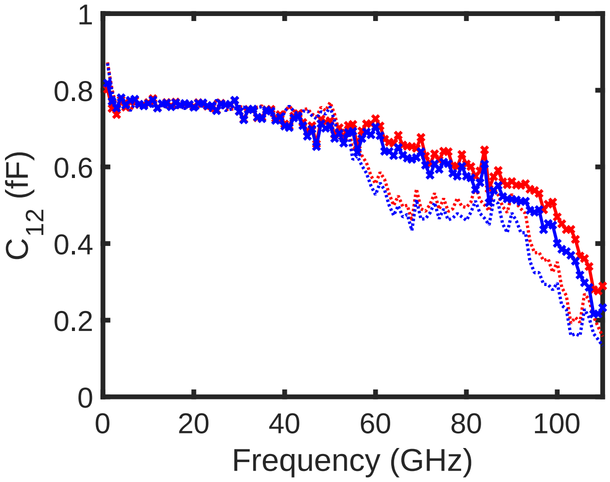
(g) Imag(Y_{21})

(h) Imag(Y_{22})

Figure 2.44: Comparison of on-wafer TRL with off-wafer SOLT calibration with respect to the Y parameters of the transistor



(a) C_{11} (b) C_{22}



(c) C_{12}

Figure 2.45: Capacitances of Transistor Open extracted from measurements using different RF probes and different calibration methods

Before performing the actual transistor measurements, the de-embedding test structures are characterized using different calibration techniques.

2.7.1 Transistor Open

The Transistor Open test structure can be represented by an equivalent lumped circuit pi-network consisting of shunt capacitors (Fig. 2.6). These capacitance values are extracted after TRL calibration on the Transistor Open, and are plotted in Fig. 2.45. The figure enables a comparison of these plots with the values extracted from off-wafer SOLT calibration as well. A Pad-Open/Pad-Short de-embedding is performed after off-wafer SOLT and on-wafer TRL calibrations on the test structure so as to maintain the same reference plane after both calibrations and to facilitate a valid comparison. The effect of the RF probes used for measurements, on the extracted values are also compared in these figures.

(a) Picoprobe (b) Cascade Infinity

Figure 2.46: Photographs of RF probes used for measurement in 1-110 GHz frequency band

It can be observed from the figure that the results are very similar, with a maximum deviation of about ±0.5fF irrespective of the calibration method used for measurements done with Picoprobe probes. However, a resonance at 60 GHz can be observed in the plots when the RF probe is changed to Cascade Infinity for both on-wafer TRL and off-wafer SOLT calibrations. This non-ideal behavior is due to the probe-to-substrate coupling as a result of the solder bump at the transition (red circle in Fig.2.46b) from coaxial to microstrip mode in Cascade Infinity probes. Consequently, this systematic signature of these probes is also noticeable in all subsequent measured data and may be attributed to the specific microstrip design of the Cascade Infinity probes.

2.7.2 Transistor Short

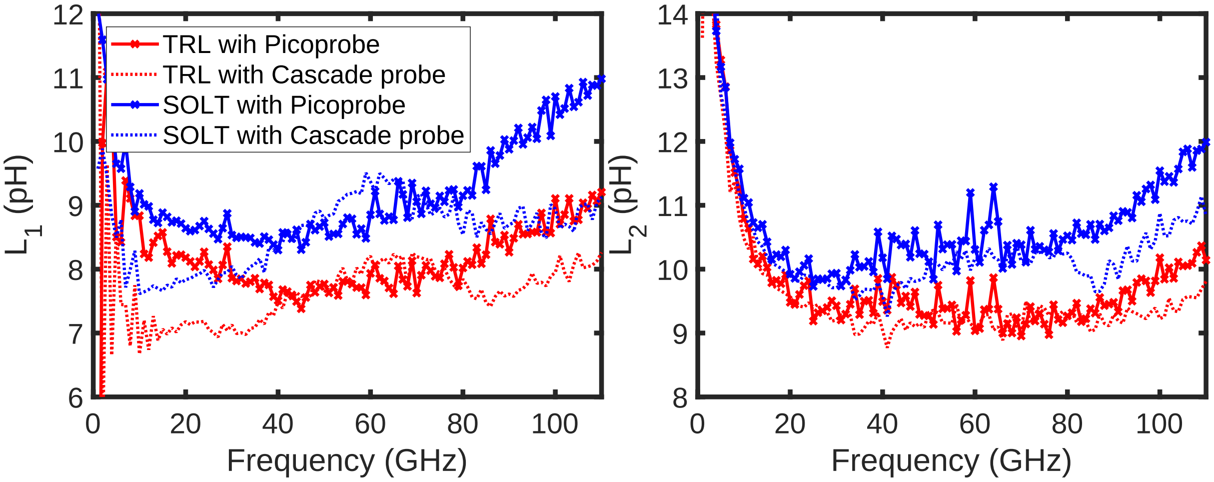
The L and R values of Transistor Short are extracted using TRL and SOLT calibration. These are plotted in Fig. 2.47.

As observed in the case of the Transistor Open, a good agreement exists between the off-wafer SOLT and on-wafer TRL calibrations when measurements are conducted with the Picoprobe probes. The TRL and SOLT calibrated results for L1, (Fig. 2.47a) with Cascade Infinity probes show a peak at 60 GHz in the extracted values as compared to Picoprobe measurements. As already discussed, this is due to the particular signature of the Cascade Infinity probes, presenting more coupling than Picoprobe probes. However, the extracted inductance values are rather constant with frequency for both calibrations. The extracted resistance values can be considered as constant up to 60 GHz for all measurements.

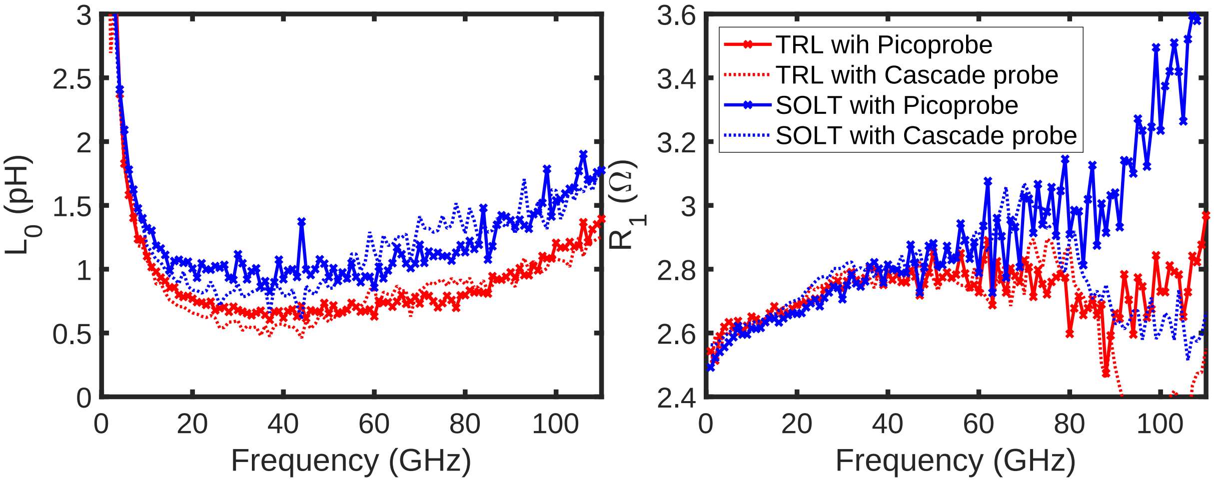
2.7.3 Transistor

After the investigation of the de-embedding test structures (Transistor Open & Transistor Short), the FD-SOI NMOS transistor is characterized using on-wafer TRL and off-wafer SOLT calibrations, followed by Short-Open and Pad-Short-Open de-embedding respectively. The transistor measurements are repeated using the two different probes.

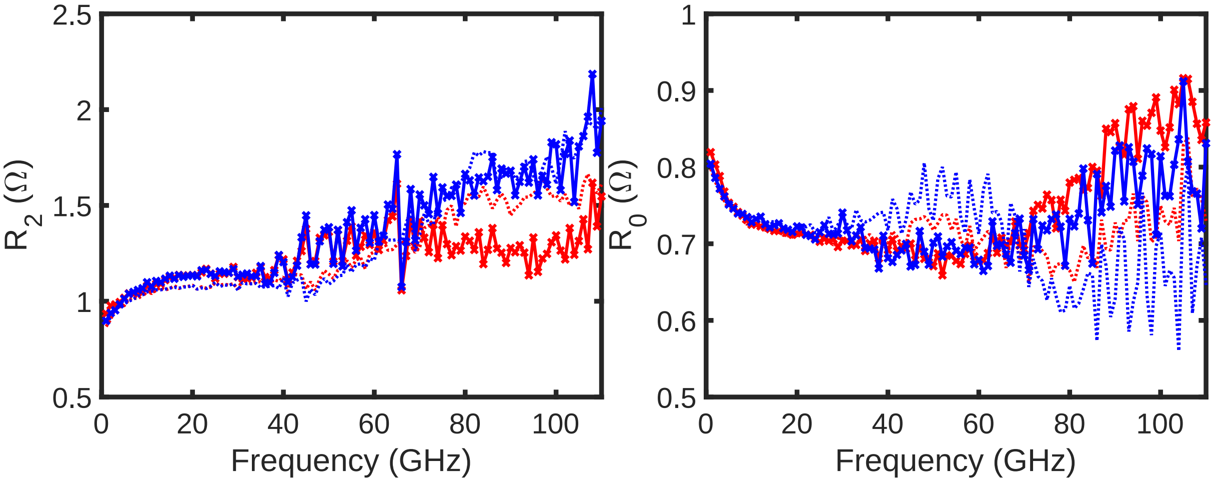
The transistor parameters ($f_T, f_{MAX}, C_{gg}, g_m$) are extracted after calibration and de-embedding. Fig. 2.48 is the plot of the S_{21} parameter of the transistor (magnitude and phase). It can be observed that the curves obtained from measurements using different methods show a good agreement with each other. The transit frequency f_T, is plotted in Fig. 2.49a. The measured values provide f_T of approximately 330 GHz. It can also be noted that the f_T obtained from TRL calibration with Cascade probes leads to a slightly lower f_T (325 GHz), which might be the



(a) L_1 (b) L_2

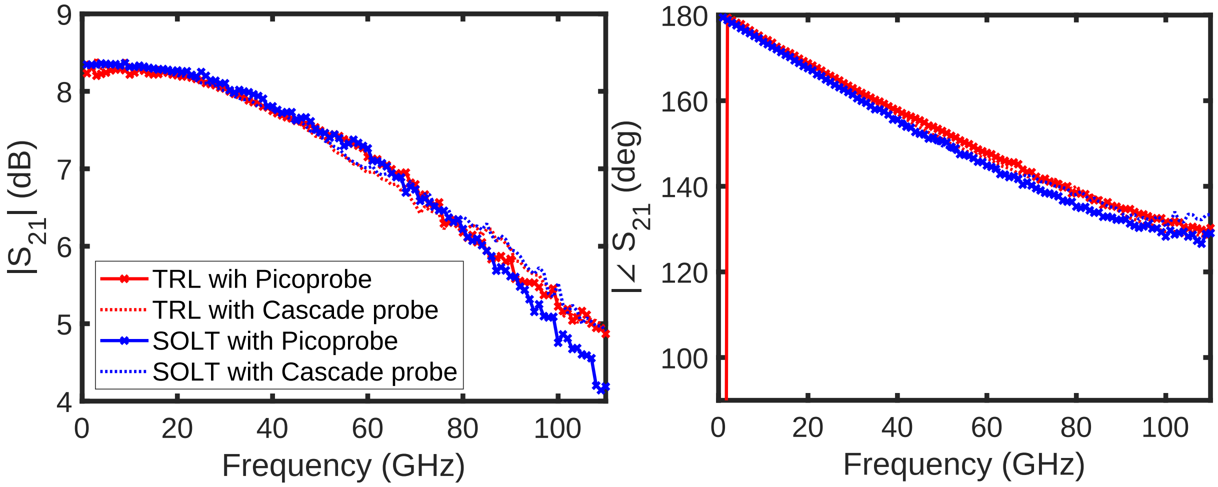


(c) L_0 (d) R_1



(e) R_2 (f) R_0

Figure 2.47: Inductances and resistances of Transistor Short extracted from measurements using different RF probes and different calibration methods



(a) Magnitude in dB

(b) Phase in degrees

Figure 2.48: S_{21} of transistor after calibration & de-embedding using different RF probes and different calibration methods

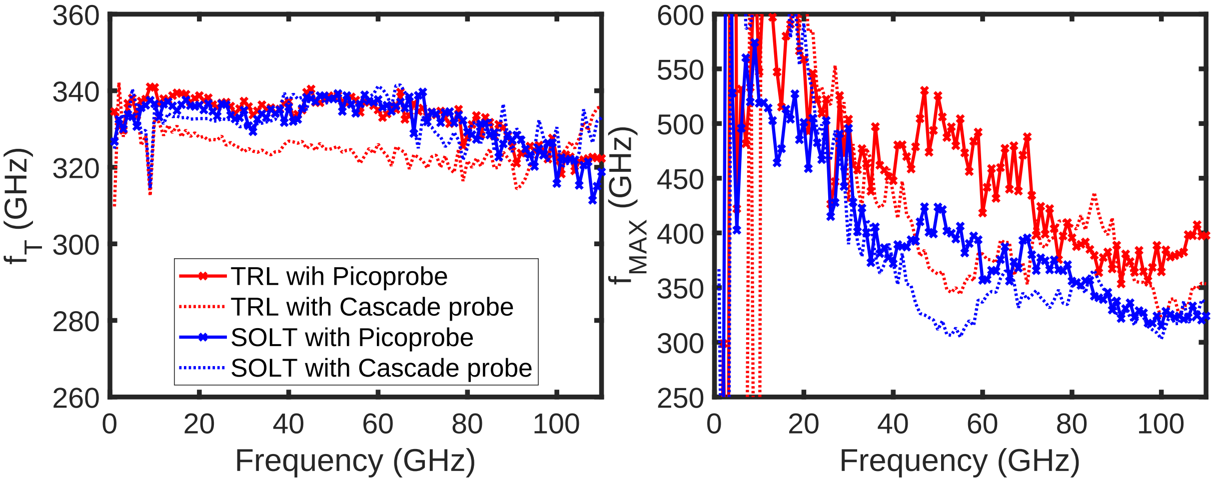
result of a non-similar probe positioning on the RF pad compared to the other sets of measurements. Fig. 2.49b presents the f_{MAX} plots, where the difference between the two calibration methods is clearly visible as already discussed in the preceding section. Also evident is the Cascade probe characteristic signature at 60 GHz as observed in the transistor open and transistor short measurements. This leads to a very large difference between the values obtained using the two different probes, particularly in the region of 40-60 GHz. Further plotted are the gate resistance (R_{gg}), gate capacitance (C_{gg}) and transconductance (g_m) of the transistor in Fig. 2.49c, Fig. 2.49d and Fig. 2.49e respectively.

The R_{gg} measurements (Fig. 2.49c) using Cascade Infinity probes give very similar results irrespective of the calibration method used. However the deviation between the TRL and SOLT calibration plots are quite conspicuous when using Picoprobe for measurement. SOLT calibration using Picoprobe leads to R_{gg} values close to the Cascade results, however, with on-wafer TRL and Picoprobe probes, the values are lower by approximately 10 Ω.

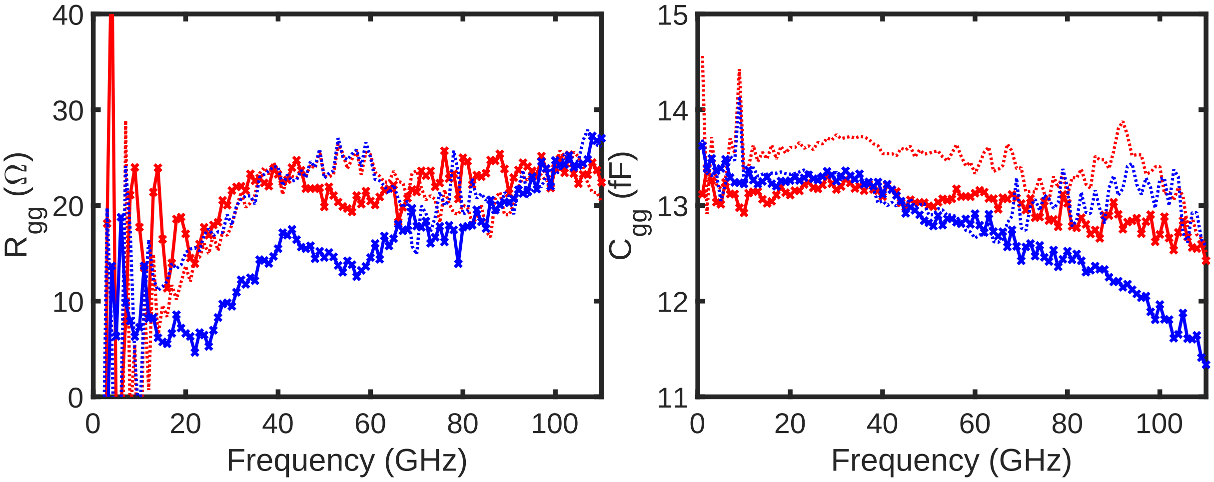
From the Picoprobe measurements, a slight decrease in the C_{gg} value over frequency can be observed (Fig. 2.49d) which is most pronounced when using the SOLT calibration. On the other hand, the Cascade probe related measurements give a quasi-constant Cgg value, which is noisier above 60 GHz.

From the transconductance plot (Fig. 2.49e), we can observe that all results are very close up to 60 GHz. A decrease can be observed for the Picoprobe data, in particular for the SOLT calibration which may indicate a HF-limitation of this calibration method. The Cascade probe data are superimposed regardless of the calibration method, but the behaviour above 60 GHz may indicate an effect of the probes.

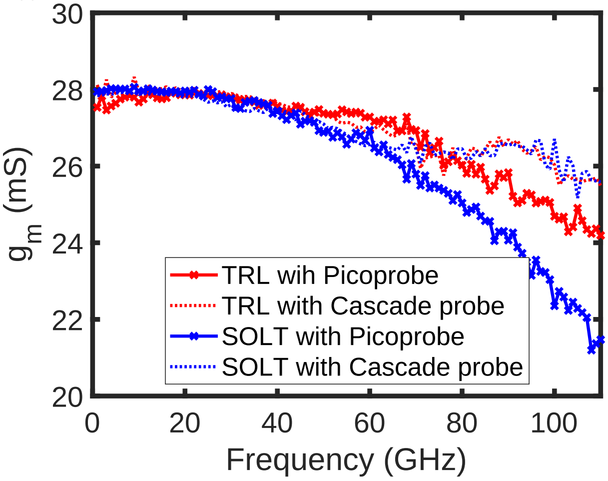
From these results it can be concluded that the measurement environment plays a very important role in the accuracy of the extracted transistor parameters. The results discussed in this section on the effect of probes and calibration method has been presented at the IEEE Latin American Electron Devices Conference held in 2021 [85]. Similar study has also been carried out in [99] using measurements on SiGe heterojunction bipolar transistor.



(a) f_T (b) f_{MAX}



(c) R_{gg} (d) C_{gg}



(e) g_m

Figure 2.49: Transistor Parameters extracted from measurements using different RF probes and different calibration methods

2.8 Drawbacks and limitations of Run1

From the ongoing discussions in the preceding sections, it can be inferred that the existing test structures for on-wafer TRL have several limitations.

1. Tiling
2. High attenuation in Lines
3. Probe-to-probe coupling
4. Inconsistent f_{MAX}

2.8.1 Tiling

Tiling is often essential on layouts in order to meet the density rules during the fabrication of the wafer. However, tiling in undesired locations, as present in the Line test structures (Line_110G & Line_500G) can lead to unexpected results. The fundamental issue faced due to tiling in the test structures labeled Run1 is that the limit of TRL calibration is reduced significantly. Although designed for calibration from 1 to 500 GHz, the tiling has led to the lowering of the upper limit to 400 GHz, the reasons for which are already discussed.

2.8.2 Line attenuation

Recall that in Section 2.2.1 the parameters of the Line standards were extracted. From Fig. 2.14 that plots the attenuation constant α of the line with respect to frequency, it can be seen that the designed microstrip lines are inherently lossy. The losses are at least 2 dB/mm, and it increases with frequency. Moreover, there is a substantial increase in α due to the tiling. It has been discussed in [81] the transistor parameters f_{MAX} and NF_{min} are sensitive to the transmission line losses, thus the accuracy of extracted values may be affected.

2.8.3 Probe-to-probe coupling

Coupling between probes or crosstalk is an inherent drawback of on-wafer TRL calibration as the the TRL algorithm does not correct errors due to this. Therefore effort needs to be taken during layout design and probe selection to minimize the probe - probe coupling as much as possible.

2.8.4 Inconsistent f_{MAX}

It has been seen that there is a considerable amount of ambiguity in the extraction of f_{MAX} of the transistor being characterised. Although the on-wafer TRL provides an average f_{MAX} of 500 GHz, the curve fluctuates greatly (±100 GHz) around this value. Moreover, the value extracted from off-wafer SOLT is much lower than that from TRL calibration. Therefore, further investigation with improved test structures is essential to have a better clarity on the accurate extraction of this parameter.

2.9 Conclusion

In this chapter, the existing test structures for on-wafer TRL calibration of FD-SOI transistors have been detailed. Measurement results obtained using these test structures were presented. It has been observed from the measurements that a few transistor parameters (particularly f_{MAX} and R_{gg}) do not conform to the existing UTSOI2 compact model and necessitate the need for another small signal equivalent circuit for the transistor. Electromagnetic simulations using HFSS have enabled to validate the accuracy of the measurements. However, several limitations have been observed in the existing test structure design and improved test structures need to be developed that address these drawbacks. Also discussed were the effects of probe choice and the type of calibration method on the extracted transistor parameters. This is also a point which requires further investigation.

In spite of these drawbacks of Run1, the discussion on the existing test structures in this chapter serve to establish a verified methodology for the design and analysis of the TRL test structures and measurements on FD-SOI transistors using the same TRL calibration kit.

Chapter 3

Design & Analysis of test structures in 10 ML

It is now evident from the analysis in Chapter 2 that the existing test structures for on-wafer TRL calibration possess several disadvantages. This has necessitated the need for the development of improved test structures. In this chapter, the discussions begin with the design of the new TRL test structures that can overcome the difficulties faced earlier, namely probe coupling and effect of tiles. Four different calibration kits are designed to study the effect of each parameter. The intrinsic behaviour of the test structures is first analysed using intrinsic EM simulations. In the next section, the measurement results of transistor are presented and compared with the full EM simulations using the RF probe models. Comparison is also made between the four different calibration kits designed.

3.1 Motivation for Run2

A major drawback with the existing structures that is quite straightforward to be solved is the presence of tiles due to automatic tiling. It has been observed from the existing 8ML TRL calibration kit that the tiles present close to and below the lines reduce the bandwidth of reliable calibration, and also introduce minor errors as a result of change in $\epsilon_{r,eff}$. Tiling is however essential to satisfy the density rules for fabrication of the wafer. Therefore a manual tiling is performed by placing metal dummies (tiles) around the test structures such that the electromagnetic wave propagation in the lines is not affected.

Measurement and simulation results of the Run1 test structures demonstrated that the microstrip lines used are very lossy, as illustrated by attenuation results presented in previous section 2.2.1. The ohmic losses in the line can be reduced by decreasing the resistance of the microstrip line, for instance by having wider lines. Thus we switch to the 10ML BEOL version of the FD-SOI technology, so that the 50 Ω characteristic impedance of lines are maintained with wider lines as the dielectric of the microstrip line would be thicker.

Another issue is the crosstalk or the coupling between the two RF probes during the measurements. This can be reduced by spacing the RF probes farther apart. In other words, increasing the spacing between the two RF pads on the layout will bring in a reduction in crosstalk. However, this would mean an increase in the wafer area occupied by the toolkit, resulting in higher costs.

It has been seen in Chapter 2 (Fig. 2.22a & Fig. 2.23) that the access lines to the DUT has some distributed parasitic effects, responsible for the frequency dependent behaviour of the Transistor Open and Transistor Short. Therefore 2 additional reflect test structures are introduced in Run2 in order to eliminate these effects as part of the TRL calibration process.

The ground plane in the test structures in Run1 were designed using the layers M1 and M2. It is interesting to investigate the significance of using two metal layers for ground plane instead of one. This question is addressed in the design of Run2 structures.

Another parameter of importance in TRL calibration is the characteristic impedance Z_c of lines. The Run2 also enables understand whether an accurate line design with 50 Ω Z_c is required or not.

3.2 Description of test structures

In the second run for TRL test structures, 4 different types of calibration sets have been designed and are designated Blocks 1 to 4. The first block (Block 1 or B1) is taken as the reference block. Blocks 2, 3 and 4 include the same DUTs and test structures as in Block1, but are designed differently compared to Block 1.

3.2.1 Block 1

Fig. 3.1 shows the top layout of the test structures in Block1. The layout of Block 1 is very similar to that of Run1, but using the 10ML stack of BEOL. The ground plane is constructed using the lowermost layers M1 and M2 (as in Run1), and the access lines and RF pads using the LB layer. Most of the drawbacks of the existing test structures are addressed in this block. As in the calibration kit of Run1, the calibration kit of Block 1 includes the Pad Open, Pad Short, Pad Load, Thru, Line_110G and Line_500G as the TRL standards. The DUTs to be characterised are the FD-SOI transistors labelled SGL86 and SGL84 (see Table 2.2 for the device geometries). Also included are the corresponding Open and Short test structures corresponding to each transistor to enable de-embedding after calibration.

To comply with the density requirements of the wafer, it was necessary to place tiles in such a way that the normal behaviour of the test structures is not affected. Due to this manual placement of tiles in the form of metallic dummies, the need for automatic tiling to satisfy the DRC has been avoided. An example of the dummy placement is shown in Fig. 3.2 for the Thru standard. The tiny spots in blue in the image are the designed tiles. It includes all the metal layers for which the density rules are not satisfied, although only one layer is visible in the image. There are no vias connecting the metal layers, thus the tiles are independent metallic pieces that are not connected to the other tiles or to the test structures. It can also be seen in the figure that the tiles are placed closer to the ground of the test structures, and away from the actual structure, so that the wave propagation in the microstrip line is not affected by the presence of the dummies. This method of manually placing the dummy tiles is adopted for all test structures for which the density rules are not satisfied.

The RF pads in Run2 have been redesigned in order to enable better contact with the RF probes and to reduce the probe-to-probe coupling. The length of the RF pad has been increased by 20 μm, maintaining the same shape and width. The dimensions of the new RF pad are presented in Fig. 3.3. The spacing between the two RF pads on either side of a test structure or DUT has

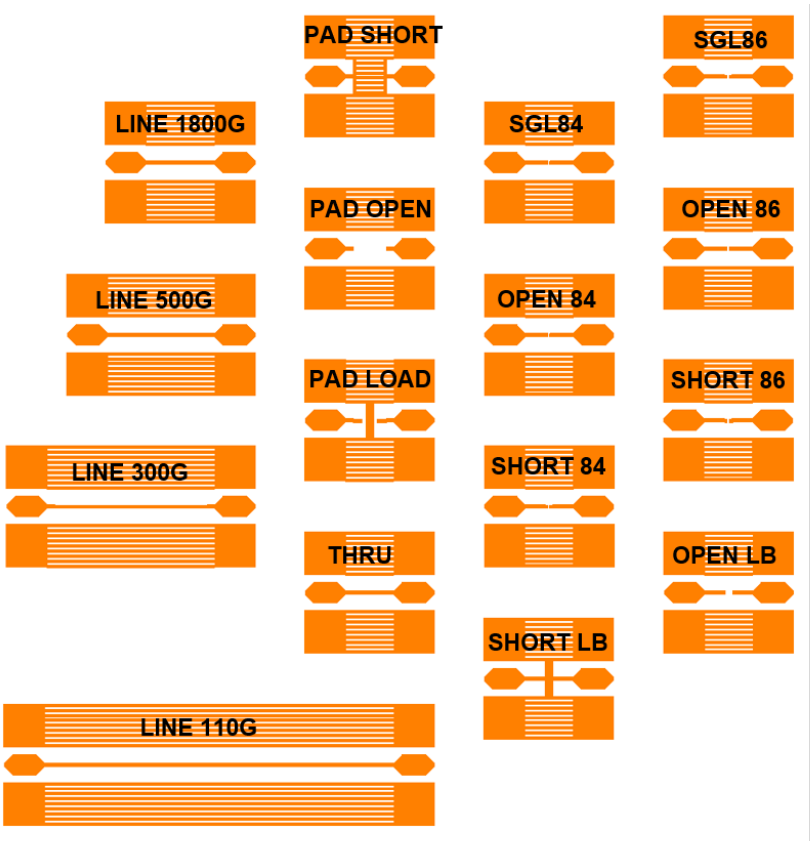


Figure 3.1: Layout of Block1 (only top metal is presented)

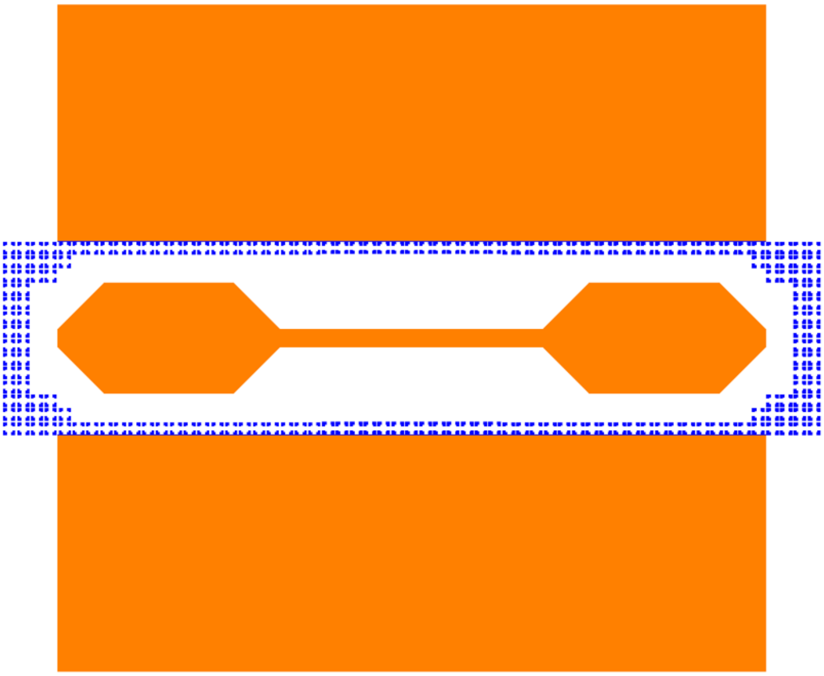
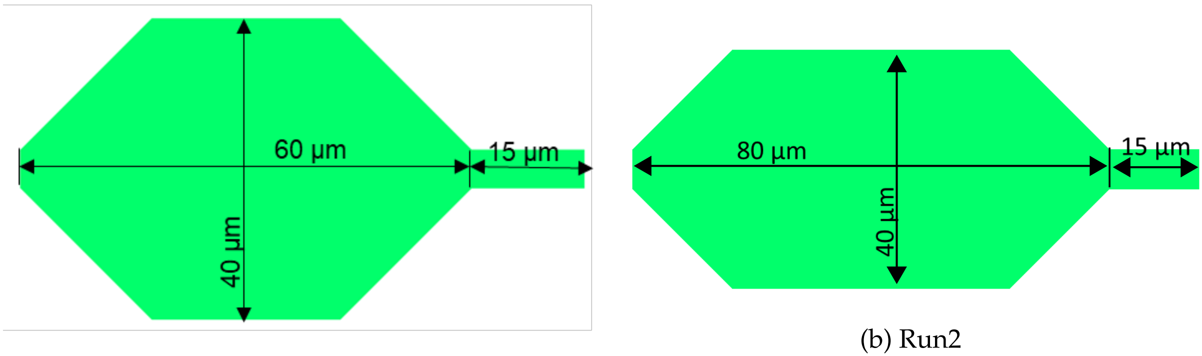


Figure 3.2: Layout of THRU showing the dummies (the orange color represents the top metal layer LB and the blue color represent the dummies at M3 layer.)



(a) Run1

(b) Run2

Figure 3.3: Dimensions of the RF pad used in Run2 compared to Run1

Table 3.1: Specifications of lines used for TRL calibration in Run2

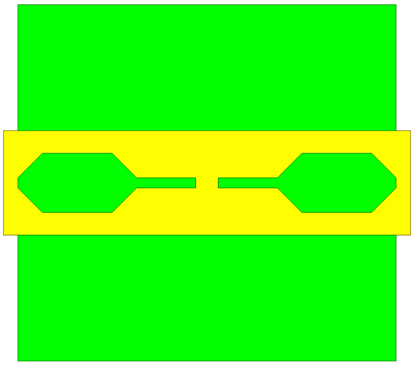
	Length (μm)	**Fmin (GHz)**	**Fmax (GHz)**
Line_110G	660	13	110
Line_300G	300	33	300
Line_500G	180	70	500
Line_1800G	105	200	1800
THRU	65		

also been increased by 10 μm, to reduce the crosstalk. This effectively increases the length of the Thru standard to 65 μm from the original value of 55 μm. The constraint for the design of Thru standard is that the length of the Thru should support only a single mode of wave propagation at its centre [100]. This single mode propagation is nevertheless ensured by the microstrip design of the Lines and Thru.

In addition to the Thru and the 2 Lines mentioned in the preceding paragraphs, two more lines are included in this calibration kit. These are labelled as Line_300G and Line_1800G. The availability of Lines of 4 different lengths ensures the validity of TRL calibration for a wide frequency range (up to 500 GHz) and also enables a smooth transition of the measurements from one frequency band to another. The specifications of the Lines are listed in Table 3.1. F_{min} and F_{max} are the limits within which each line can be used for valid TRL calibration and are calculated theoretically using equations 1.8 and 1.7.

OpenLB & ShortLB

It has been observed from the analysis of the existing TRL test structures that the lumped parasitics model for access lines is not always valid as the distributed effects come into effect at higher frequencies, thereby affecting the accuracy of the Short/Open de-embedding. This issue was addressed by adjusting the parameters in the toolkit for the TRL calibration algorithm. However, a more reliable method is to directly shift the reference plane to a point after the access lines during TRL calibration. For this purpose, two new reflect standards, called OpenLB and ShortLB are implemented in Run2. The top layouts of these are presented in Fig. 3.4. These are similar to the Pad Open and the Pad Short, but with longer access lines, such that the parasitic effect of a longer part of the access line is removed after TRL calibration.


(a) OpenLB

(b) ShortLB

Figure 3.4: Additional reflect standards in Run2

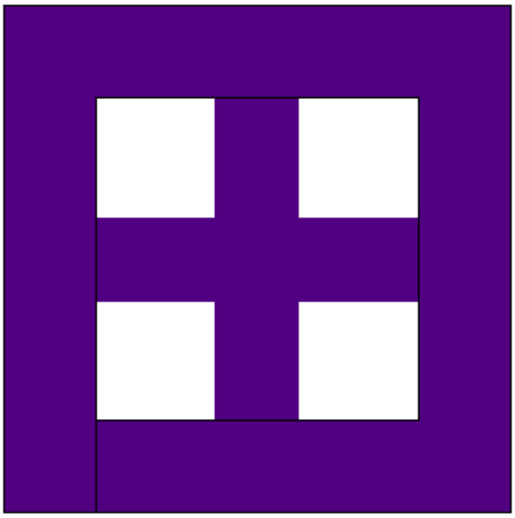


Figure 3.5: Unit cell used for ground plane (M1) in Block 2

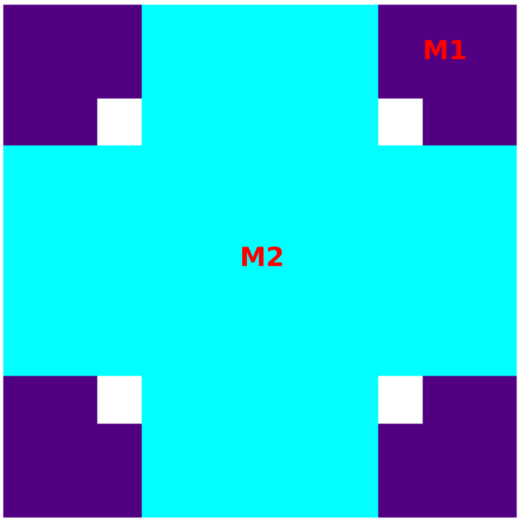


Figure 3.6: Unit cell used for ground plane in Block 1

3.2.2 Block 2

The TRL calibration kit of Block 2 (B2) consists of all the test structures and DUTs as in Block 1. However, the difference in Block 2 is in the way the ground plane is designed. The unit cell used to create the ground plane in B2 is presented in Fig. 3.5. This design involves only a single metal layer, M1. The shape has been designed so as to satisfy the density requirements of the wafer. The ground plane unit cell of B1 is in Fig. 3.6 for reference. This Block has been conceived to study the significance of ground plane design on the accuracy of on-wafer TRL calibration.

The top layout of Block 2 looks exactly similar to the one of Block 1, as the difference is only in the lowermost layers. Thus a separate figure is not presented here for the layout of Block 2.

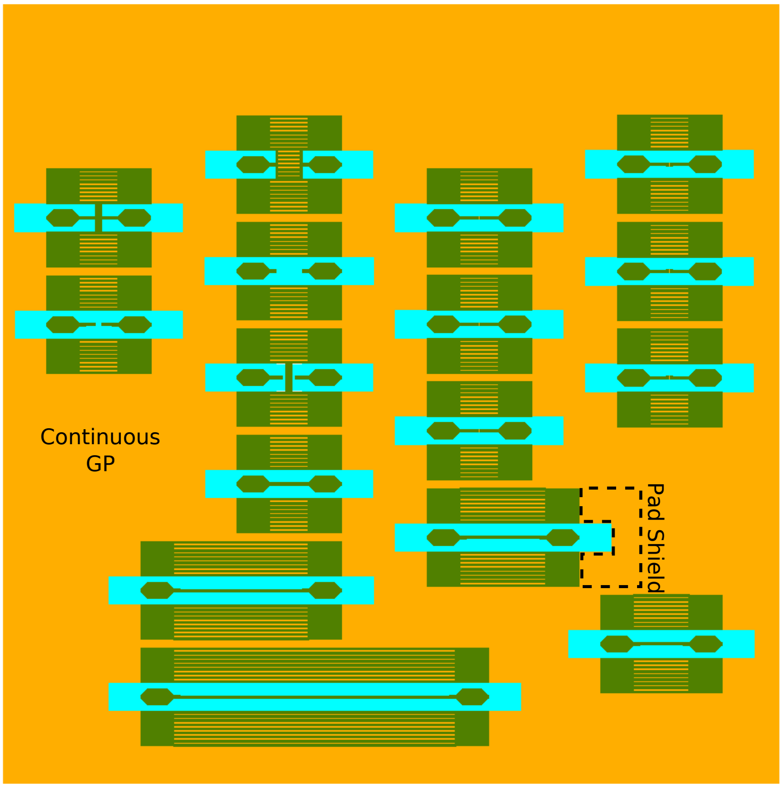


Figure 3.7: Layout of Block 4

3.2.3 Block 3

The test structures and DUTs in Block 3 (B3) are identical to those of the reference block Bl, except the dimensions of the microstrip lines. The basic idea was to reduce the losses in the lines which become significant with increasing frequency. Thus wider microstrip lines have been designed, lowering the line losses due to higher line conductance. The resulting lower characteristic impedance Z_C is corrected through the impedance correction procedure described in Chapter 1.

3.2.4 Block4

In Block 4 (B4), all the structures are same as those in Block 1, and the design of these are also similar to B1, i.e., test structures and DUTs in 10ML, with microstrip lines of 50 Ω characteristic impedance, and ground plane implemented using layers M1 and M2. The difference is that the Block 4 has a continuous ground plane for all the test structures, whereas in B1, the ground plane is independent or discontinuous between each test structure and DUT. In other words, all the ground pads are connected together in Block 4. The top layout of the calibration kit of Block 4 is shown in Fig. 3.7. Another feature of the layout in B4 is the presence of a 'Pad shield' around the RF pads of all structures. This is an extension of the ground pad around the RF pads using all the metal layers below aluminium as visible in the figure. A cross sectional view of the RF pad shield is shown in Fig. 3.8.

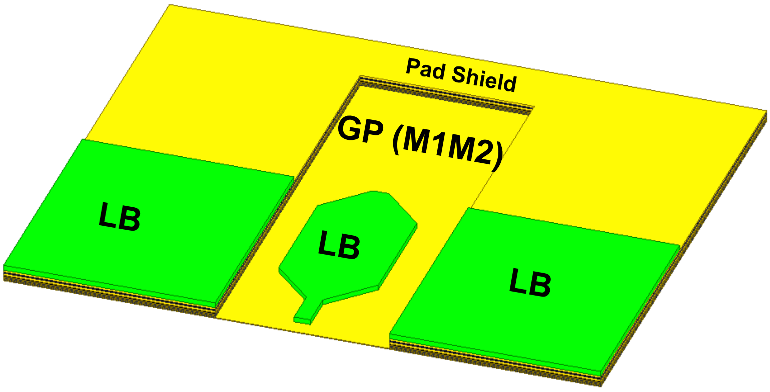


Figure 3.8: Cross-sectional view of the Pad Shield around RF pad in Block 4 (green: LB layer, yellow: copper metal layers below LB)

3.3 Intrinsic EM simulations

In this section, we have a look at the intrinsic behaviour of the designed test structures using EM simulations. The Block 1 is the reference block. Therefore, the intrinsic structures from Block1 are simulated using Ansys HFSS. This study also enables a comparison of these test structures with those from the previous run (Run1).

3.3.1 Lines

Presented in Fig. 3.9 are the magnitude plots (in decibels) of S_{11} of the Lines used in the TRL calibration kit in Run2. The S_{11} plots for Lines from Run1 are also plotted in dotted lines for comparison. The lower values of S_{11} for the Run2 Lines indicate a better impedance matching as compared to the Run1 Lines. In other words, the characteristic impedances of the new Lines are more closer to the standard 50 Ω value due to a better optimization of their dimensions. This Fig. 3.9 also shows the line resonances which give a rough estimate of the frequency range for which the line can be used as a TRL calibration standard. However, a much clearer picture of the usable range of frequencies for each line can be obtained by plotting the phase of S_{21} as a function of frequency. It is a rule of thumb for TRL calibration that more accurate results are obtained when the Line standards used for calibration have an electrical length ranging between 20°and 160°[101]. This parameter is plotted in Fig. 3.10 for lines from Run2. The vertical dotted lines represent the electrical length limits of the lines. It is evident from this figure that thanks to the multiple line standards and the absence of the dummies, faithful on-wafer TRL calibration is now possible from 13 GHz up to 500 GHz. This is a considerable improvement as compared to the previous run, where the maximum reliable frequency for calibration was 350 GHz.

The absence of automatic tiling in the lines has several positive consequences. To illustrate this, the propagation constant ($\gamma = \alpha + j\beta$) and the RLCG parameters of the lines are extracted and plotted in Fig. 3.11 and Fig. 3.12 respectively. The attenuation per unit length along the Lines,

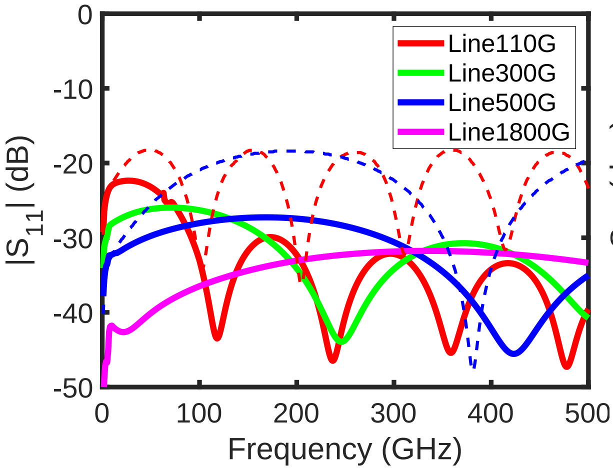


Figure 3.9: Magnitude of S_{11} of the Lines compared to Lines from Run1 (in dashed lines)

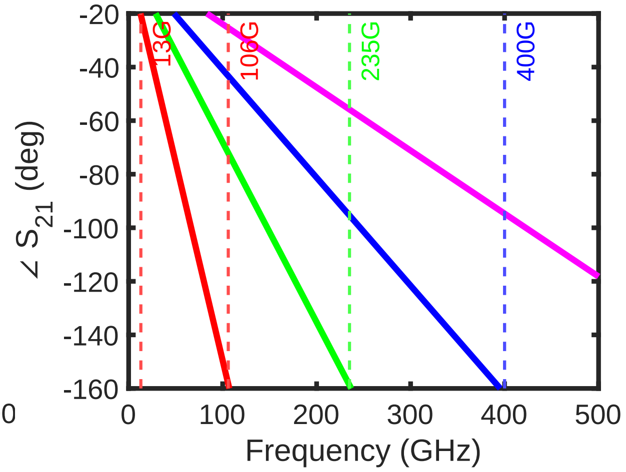
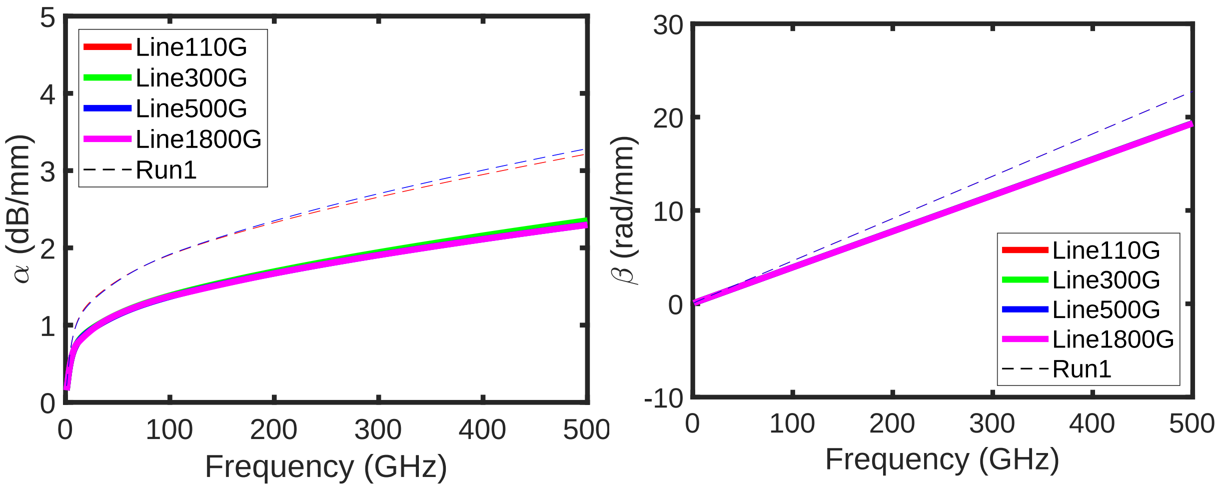


Figure 3.10: Phase of S_{21} of the Lines showing the limits of TRL calibration



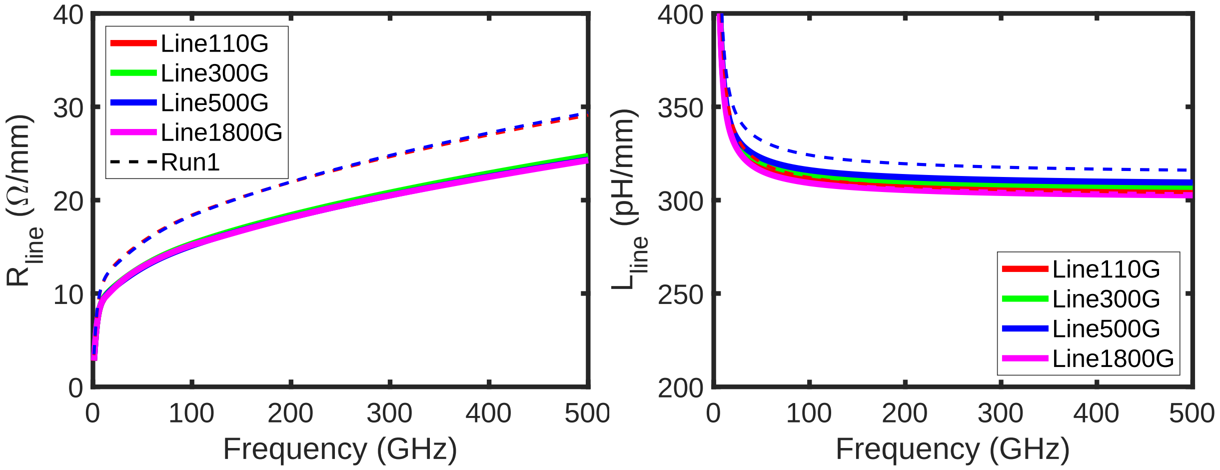
(a) Alpha

(b) Beta

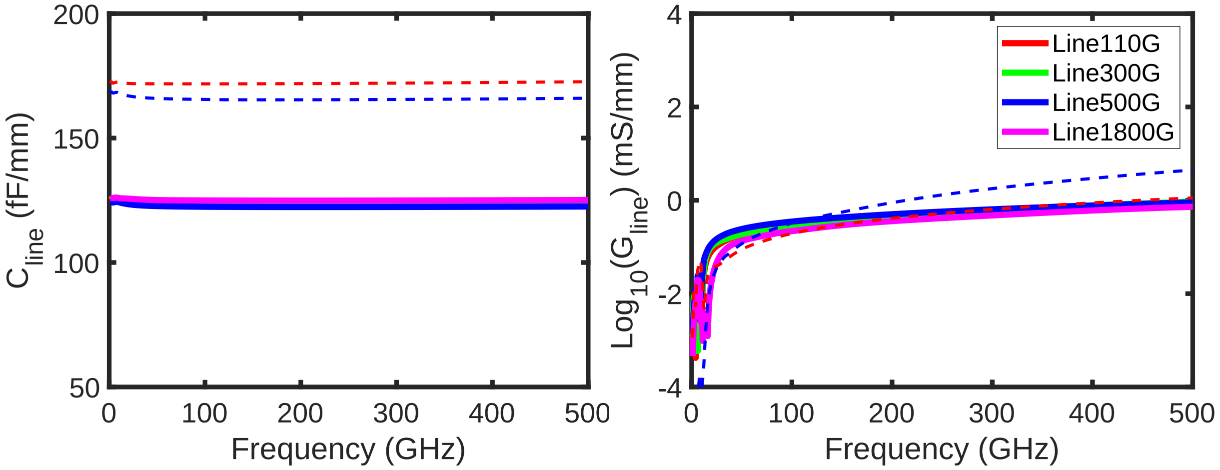
Figure 3.11: Propagation constant of Lines in Run2 (Run1 lines are shown using dashed lines for comparison)

represented by α, is plotted in Fig. 3.11a. In comparison to the Lines from Run1 (dashed lines in the figure), the new lines are considerably less lossy. The intrinsic electromagnetic simulations predict the losses to be reduced by nearly 25-30 % due to the absence of the tiles very close to the lines. Moreover, the propagation constants (real and imaginary parts) are exactly the same for all the Lines standards in Run2 as can be deduced from the overlapping solid curves in Fig. 3.11. This means that under ideal conditions all the Lines standards have the exact same behaviour, which is a desirable feature for accurate TRL calibration.

Another parameter of significance in TRL calibration, that is affected by the presence of dummies, is the capacitance per unit length of the Line standards, often termed as C_{line}. This parameter is extracted using the model in Fig. 2.16 and is plotted in Fig. 3.12 It is known that the capacitance per unit length of a uniform transmission line is directly proportional to the dielectric constant of the material between the conductors as in equation 3.1 [88], where $\mathbf{E}$ is the electric field and V_0 is the voltage between the conductors.

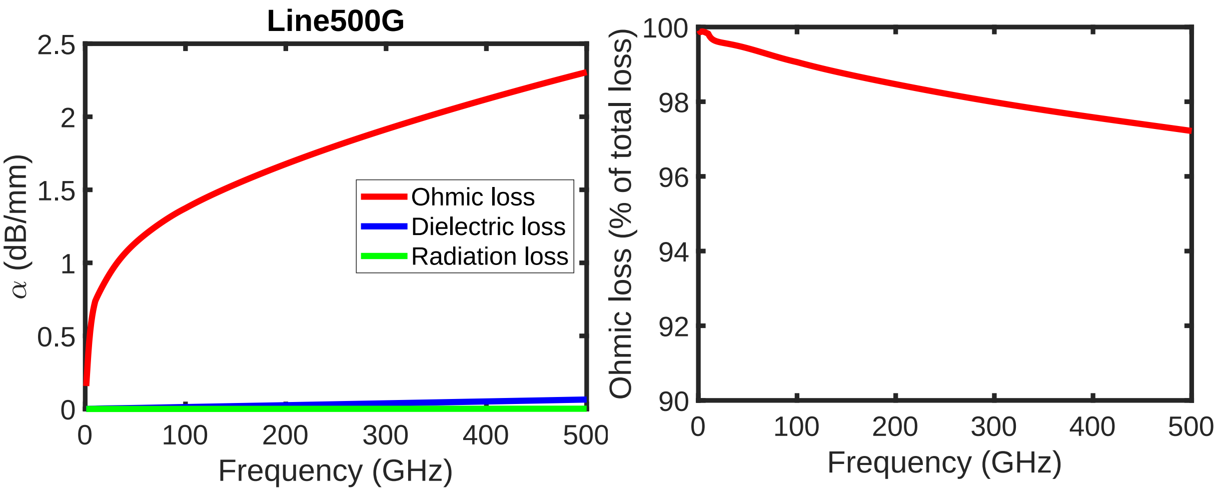


(a) R (b) L



(c) C (d) G

Figure 3.12: RLCG parameters of Line used in Run2 (values from Run1 are plotted with dashed lines)



(a) Line losses calculated from EM simulation

(b) Ratio of ohmic loss

Figure 3.13: Types of line losses

$$C = \frac{\epsilon}{|V_0|^2} \int_S \mathbf{E} \cdot \mathbf{E}^* dS \quad F/m \tag{3.1}$$

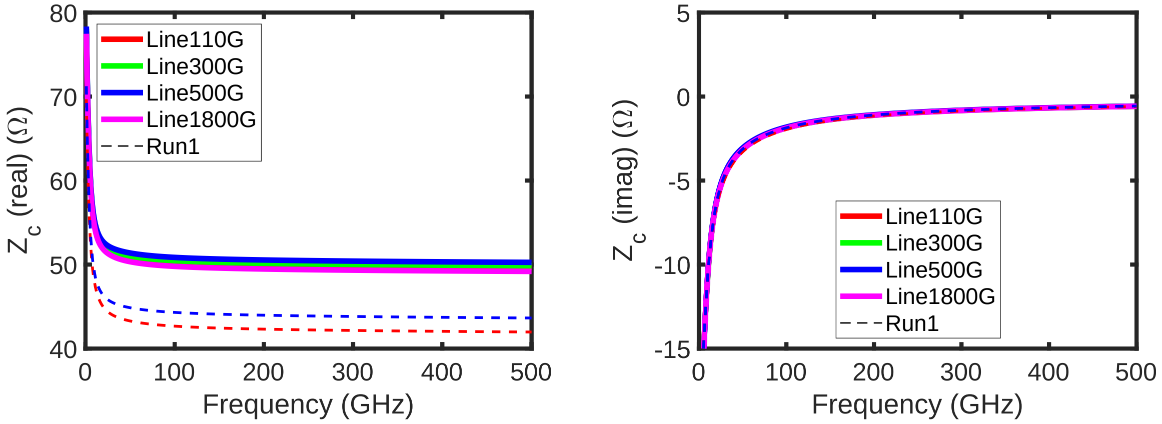
This explains the enormous difference in C_{line} between the two runs. Run1 required an increase in the value of ϵ to fit the C_{line} from measurements. However, due to the absence of tiles in the lines, Run2 does not require such a modification and hence the lower value of C, which is also constant for all the line standards.

Line losses

The losses in a transmission can be mainly of three types: ohmic losses due to the finite conductivity of the metal, dielectric losses due to the insulating material, and radiation losses. The contribution of each type to the total line loss can be studied as detailed in [102] using intrinsic EM simulations. The radiation losses can be extracted by simulating the line with zero contribution from conductivity and dielectric losses. This means the lines have infinite conductivity for the metals and zero conductivity and zero loss tangent for the dielectric. By adding the finite conductivity and finite loss tangent, one by one, the other loss contributions can also be determined. The loss tangent (tan δ) of the silicon dioxide dielectric layer is taken as 0.001 [103] [104]. However, there are some uncertainties in the exact value of loss tangent due to the complex stack of dielectric layers in the BEOL. The types of losses are plotted in Fig. 3.13.

It is quite evident from this study that the contribution of radiation loss and dielectric loss to the total line loss are very small (< 0.1 % and < 3 % respectively) and can be neglected a priori.

As already explained from the plots of propagation constant of the Lines, the lines of Run2 are less lossy as compared to those from Run1. This reduction in loss is due to two main factors. The first reason is that the Run2 lines use the 10ML stack whereas the Run1 lines used the 8ML stack. Microstrip line design using the 10ML stack means the height of the dielectric is now larger, resulting in wider lines in order to maintain the 50 Ω characteristic impedance according to equation 2.1. A wider metal layer for the line implies a lower resistance, thereby reducing the conductivity loss. This fact can also be deduced from the plot of R_{line} in Fig. 3.12.



(a) Real part (b) Imaginary part

Figure 3.14: Characteristic impedance of the Lines

It is clear from the plots that the lines from Run2 have a lower resistance per unit length than the existing lines in 8ML.

The second reason for the less lossy lines of Run2 is the absence of dummies or tiles below and close to the microstrip line. These tiles contribute to both the conductivity and losses within the dielectric, as the presence of tiles in the oxide layer can alter its dielectric properties. This fact is also evident from the G_{line} plots in Fig. 3.12, where the conductance per unit length is higher in Run1 particularly at higher frequencies for Line_500G.

The RLCG plots also shows a small difference between the 2 runs in the values of L_{line}. This is partly due to the presence of dummies in Run1, that slightly modify the value of effective permeability (μ_{eff}) of the oxide layer. Moreover, the $L = \frac{Z_0}{V_p}$, where $V_p = c/\sqrt{\epsilon_{r,eff}}$ [105]. Thus, with the change in BEOL from 8ML to 10ML in Run2, there is a change in $\epsilon_{r,eff}$ that affects the value of L_{line}.

Extraction of Characteristic Impedance Z_c

It is understood that accurate knowledge of the characteristic impedance of the Line standards is very crucial for reliable TRL calibration. Fig. 3.14 shows the characteristic impedance (real and imaginary parts) of the lines extracted from intrinsic EM simulations. It can be observed that the real part of Z_c is constant for all the line standards and the value is very close to the standard 50 Ω. This fact has already been discussed from the magnitude plots of S_{11} in Fig. 3.9. However, we do not see any significant change in the imaginary part of Z_c in the 10ML lines.

During TRL calibration, the value of Z_c is calculated from the value of C_{line} extracted using equation 1.13 by making the assumption that $G/\omega C < 0.004$. In other words, equation 1.14 is accurate when the losses within the dielectric (G) is nearly zero. Violation of the condition $G = 0$ can cause errors in the extracted value of Z_c [89]. The curves of $G/\omega C$ for each line is plotted in Fig. 3.15, in reference to the lines from Run1. It can be seen from the figure that for the curves corresponding to the lines from Run1 (represented by dashed lines), the value of $G/\omega C$ is not consistent between the two Lines and it is slightly greater than the threshold value for Line_500G for frequencies below 350 GHz. This inconsistency between lines could be a result of the tiling which is not exactly the same in each line. On the other hand for the lines from Run2 (represented by solid lines), this value is much lower for a wider range of frequencies,

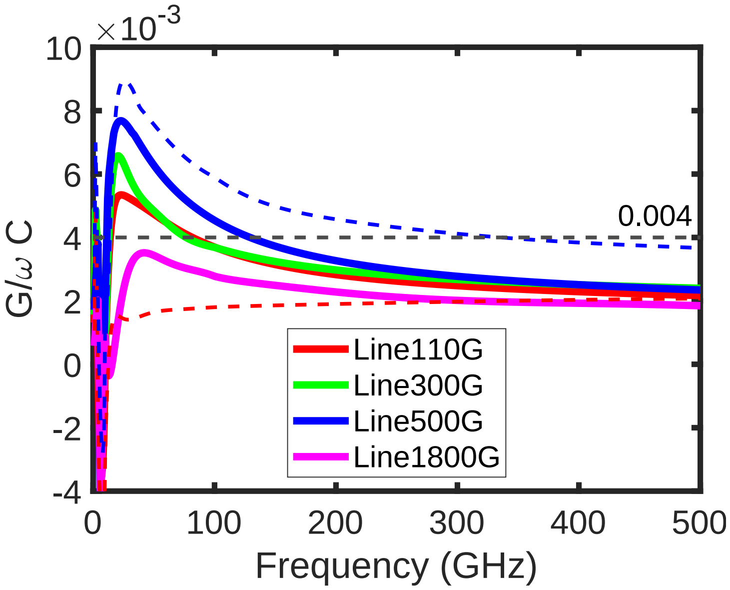


Figure 3.15: $G/\omega C$ of the Line standards extracted from intrinsic EM simulations

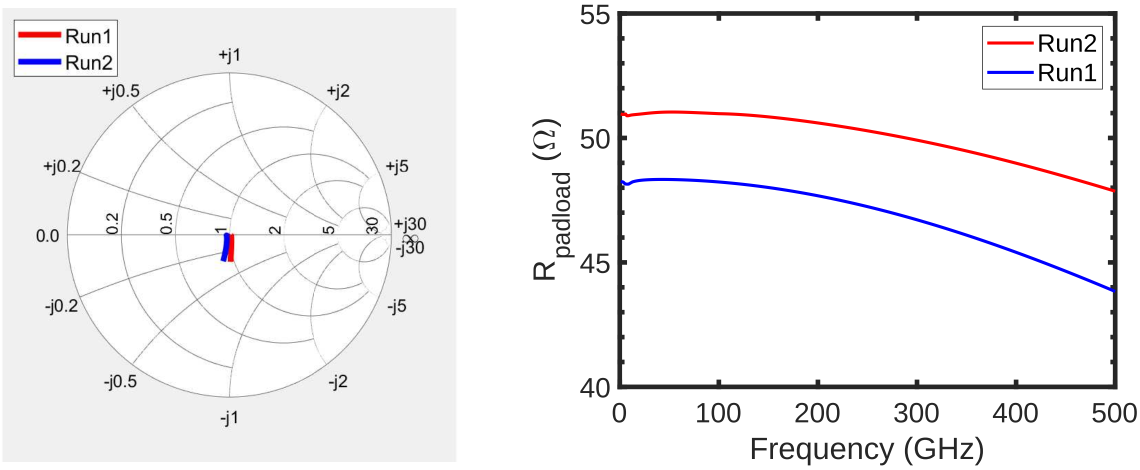
thereby satisfying the assumption used for impedance correction. It can also be observed that for frequencies below 100 GHz, the value of this parameter is greater than the threshold by a small amount in Run2. Since the level of deviation of $G/\omega C$ from 0.004 is very small, the error introduced during impedance correction due to this is expected to be small.

3.3.2 Pad Load

The extraction of Z_c is performed using the Pad Load, for further impedance correction. The design of Pad Load, has been improved in the second run, by using the standard version of the polysilicon that forms the resistor. In Run1, the resistance was realised using the low cost version of the polysilicon, which can reduce the accuracy. In Fig. 3.16, the reflection coefficient and the extracted resistance (without access lines) are plotted in comparison with Run1. The plot of S_{11} shows a better matching in the case of Run2. This is exemplified by the resistance plot where $R_{padload}$ is closer to 50 Ω in Run2. However, this Load also has a small imaginary part (capacitive) along with the real resistive part. Nevertheless, the method used for Z_c extraction [63] makes the assumption that the load is real and equal to its constant dc resistance. This assumption is a source of error during impedance correction. Yet, this is only a minor error that as the capacitive part ($\approx$ 2 fF) and the frequency dependence ($< \pm 4\%$) are very small.

3.3.3 De-embedding structures

Each transistor is associated with its corresponding Open and Short test structures for the purpose of de-embedding, as discussed in Chapter 2. The capacitances of the Open and the inductances and resistances of the Short corresponding to the transistor SGL86 are extracted and compared with the values from Run1. The structures in Run1 and Run2 are same upto the metal 6. In Fig. 3.17 a small decrease is observed in the capacitances (C_{11} and C_{22}) of the Transistor Open. This is a result of the increase in the height of the BEOL with 10ML instead of the 8ML in Run1. Similarly the extracted inductances (L_1, L_2, L_0) of the Transistor Short show a slight increase in values for Run2, due to the larger number of via connections in the 10ML



(a) Reflection coefficient (S_{11}) of Pad Load

(b) Resistance (Real(Z_{11}))

Figure 3.16: Pad Load

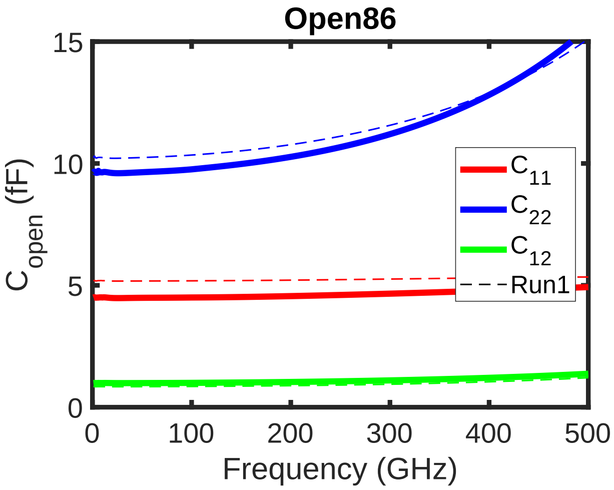
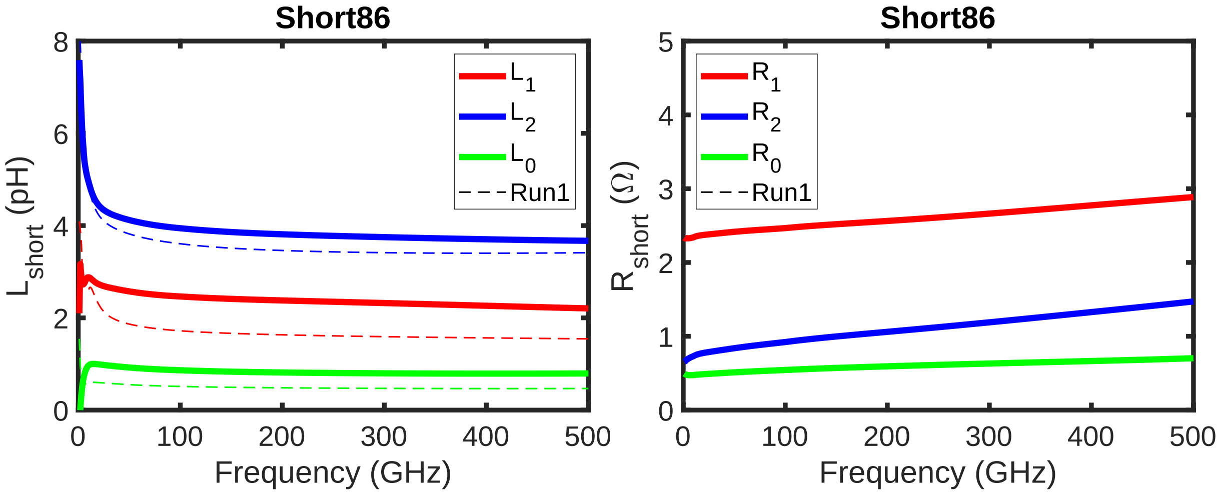


Figure 3.17: Capacitances of Transistor Open extracted from intrinsic EM simulation

stack. However, no noticeable change is observed in the resistance of the Transistor Short, compared to Run1, as can be concluded from the overlapping plots. Indeed,the resistors are dominated by the lowest metal layers and vias that are strongly downscaled. These parasitics of the Transistor Short are plotted in Fig. 3.18.

It is understood that the errors due to measurement and de-embedding are proportional to the parasitics of the calibration and de-embedding structures [81]. Therefore minimizing these parasitics is of utmost importance. Indeed, a large lumped element like C_{22} (10 fF) mainly induced by the interconnection at the lower metal levels and plugged to the 5 µm microstrip line together with the vias descent elements will result in a frequency depend test structure that introduce errors in the de-embedding procedure. On the other side, C_{11} which is two times smaller, shifts the resonance frequency of the LC circuit higher in the THz range and allows to maintain an accurate de-embedding procedure in port 1 at least up to 500 GHz. Therefore, one can conclude that the design of this specific test structure will require some optimization to minimize C_{22} for the next runs in order to improve the de-embedding accuracy above 325 GHz.



(a) Inductances

(b) Resistances

Figure 3.18: Intrinsic EM simulation of Transistor Short

3.4 Measurement results

Measurements have been performed using each of these Blocks from 1 to 500 GHz for B1 and B4 and up to 330 GHz for B2 and B3. The measurement setup and the choice of RF probes are same as those used for the measurements using Run1. The transistor characterised (SGL86) is also the same one used in measurements of Run1. The difference with the Run1 measurements is that the new reflect standards (PadOpen/PadShort) have been utilised and that the Line_1800G is used as the TRL Line standard above 300 GHz.

The de-embedding structures (Transistor Open & Transistor Short) corresponding to the transistor SGL86 are first characterised to extract the values of their lumped parasitics. The results are plotted in Fig. 3.19 and Fig. 3.20 for the Open and Short respectively, where the values are compared to those from intrinsic EM simulations. The reference plane for this measurement and simulation is after the access lines and close to the BEOL stack, in other words, the distributed effects of the access lines are not considered. The Open measurements are in good agreement with the EM simulations, with the exception of C_{22} after 350 GHz. This could possibly be due to the resonance like behaviour introduced due to the inductive effect of access lines and vias descent (see Fig. 2.22a) that is not fully corrected at port 2 by shifting the reference plane. The Transistor Short measurements are quite noisy as already observed from Run1. In spite of this uncertainty due to noise, a reasonable agreement is observed between measurements and EM simulations for the Short.

The transistor parameters extracted (bias point: $V_d = 1V, V_g = 600mV$) after TRL calibration and de-embedding in Run2 (Block 1) are plotted in Fig. 3.21, and comparison is made with the results obtained from Run1. It can be seen from the plots that the results are not greatly different between the runs. However, a small improvement can be observed in Run2 in the measurements above 400 GHz, although with a scope for betterment of the results. In view of the minor differences in the results, another extraction of small signal equivalent circuit is made using the Run2 results and presented in the next section.

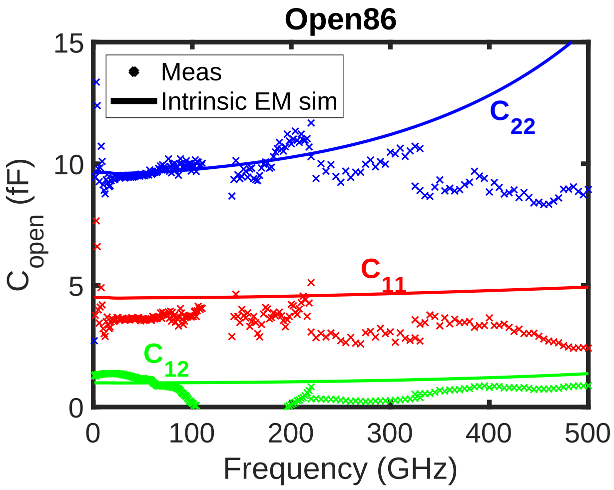
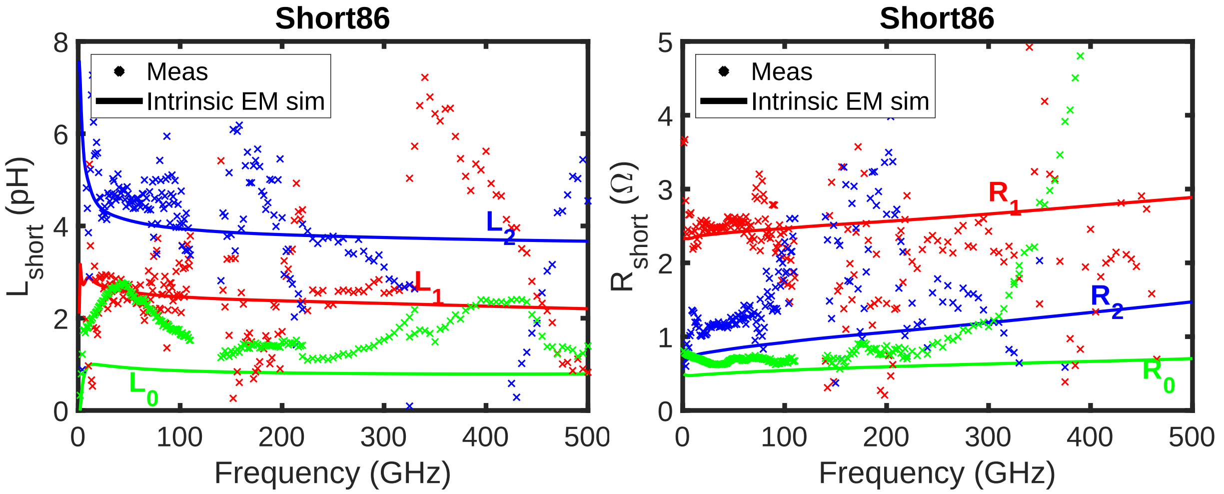


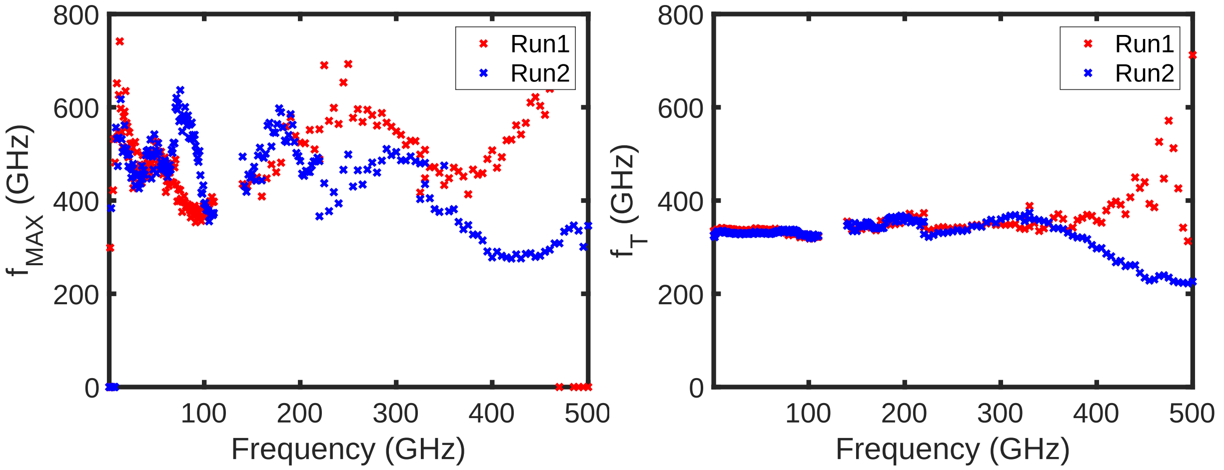
Figure 3.19: Measured capacitances of Open86



(a) Measured inductances of Short86

(b) Measured resistances

Figure 3.20: Measurements on Transistor short



(a) f_{MAX}

(b) f_T

Figure 3.21: RF FoMs of transistor from Run 2 (Block 1) compared to Run1

Table 3.2: SSEC parameters from Run2

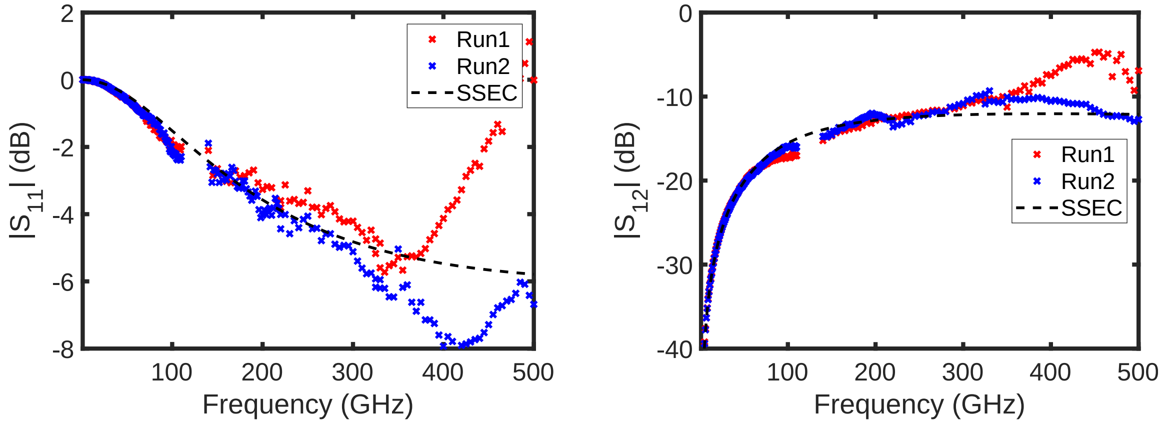
Parameter	Run2	Run1
R_g	10 Ω	10 Ω
R_d	5 Ω	6.6 Ω
R_s	3.3 Ω	5.2 Ω
C_{gs}	9 fF	10.5 fF
C_{gd}	3.6 fF	3.7 fF
C_{ds}	2.7 fF	2.5 fF
R_{ds}	570 Ω	590 Ω
R_i	2 Ω	5 Ω
g_{m0}	30 mS	32.85 mS
τ	80×10^{-15}	0

3.4.1 SSEC extraction

The extraction of parameters of the small signal model of Fig. 2.30 uses the method as discussed in Section 2.4. The values obtained from Block 1 of Run2 are presented in Table 3.2 in comparison to the model of Run1, both at a bias point of V_d=1V & V_g=600 mV. It is seen from the table that the two models are very similar to each other. This is expected as the characterised transistor is same in both cases. Notable difference can be observed only in the value of R_i, which can lead to a 2-3 Ω difference in the gate resistance R_{gg} of the transistor, and in R_s. Indeed a better accuracy was obtained by introducing NQS effect using τ and by reducing R_i and R_s consequently.

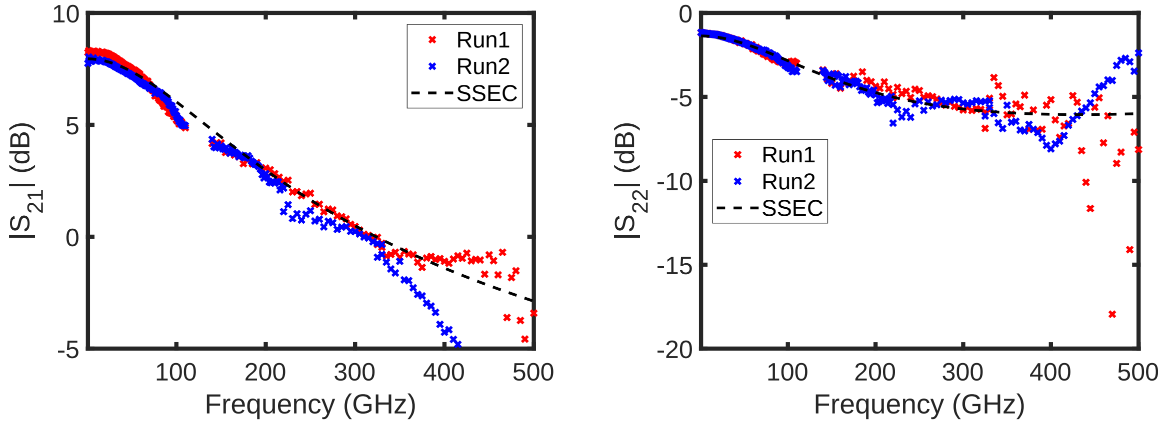
The magnitude and phase of S-parameters of the transistor are plotted in Fig. 3.22. A very good agreement is observed between the small signal model and measurements of Run2 up to 350 GHz. Beyond this point, deviations can be observed in the measurements, especially in the parameters S_{11} and S_{22}. Concerning Run1 measurement and as previously explained, the inaccuracy results from: i) the line length used for the TRL is out of the specification of the rule of thumb that mentioned that the electrical length is between 20 and 160 degrees; ii) the de-embeding procedure is not accurate above 350 GHz due to the distributed nature of the transistor open at port 2 despite the shift in reference plane. In Run2, although the first problem is solved concerning the electrical length, the second problem of de-embedding remains. Other major points should also be considered such as the limitations of probe positioning and probe couplings. However, above 350 GHz, Run2 measurements show a minor improvement over Run1 plots which are very noisy and varying extensively. Continuity between the different frequency bands of measurements is also ensured, although different Lines are used in each band. Similarly, Y parameters of the transistor are plotted in Fig.3.23. Here as well, we see a fairly good agreement of the Run2 measurements with the small signal model up to 400 GHz.

Next, we proceed to the EM simulation of the TRL calibration of this Block 1 to study the possible reasons for the deviation of measured results from the small signal model of the transistor, particularly after 400 GHz.



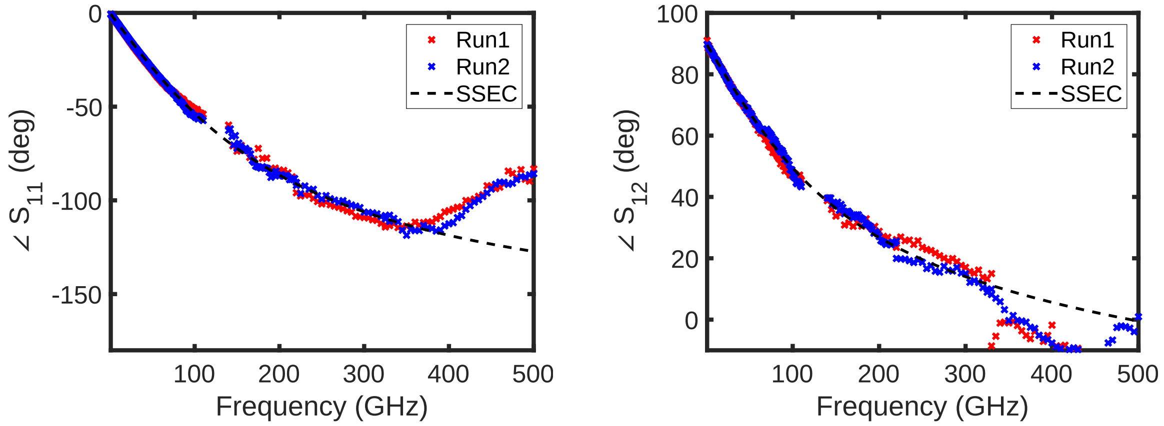
(a) $|S_{11}|$ in dB

(b) $|S_{12}|$ in dB



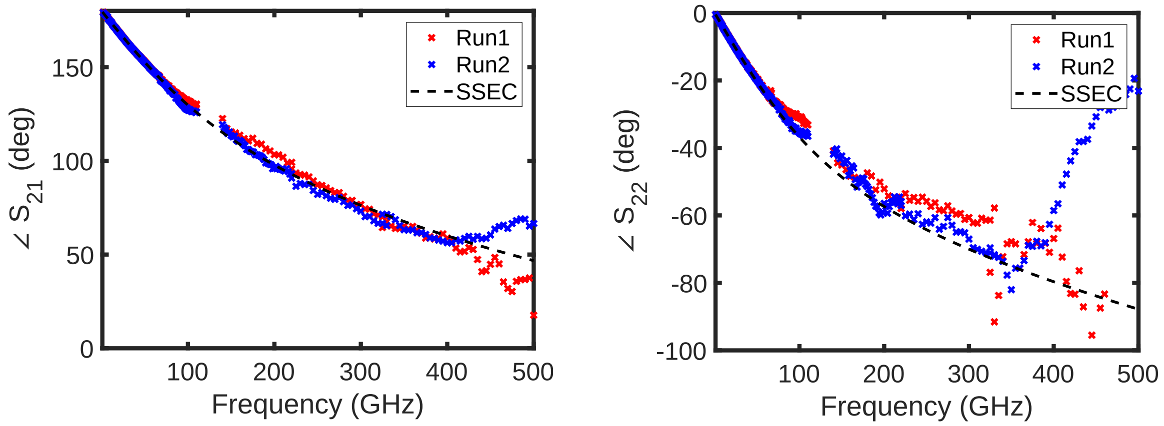
(c) $|S_{21}|$ in dB

(d) $|S_{22}|$ in dB



(e) $\angle S_{11}$ in degrees

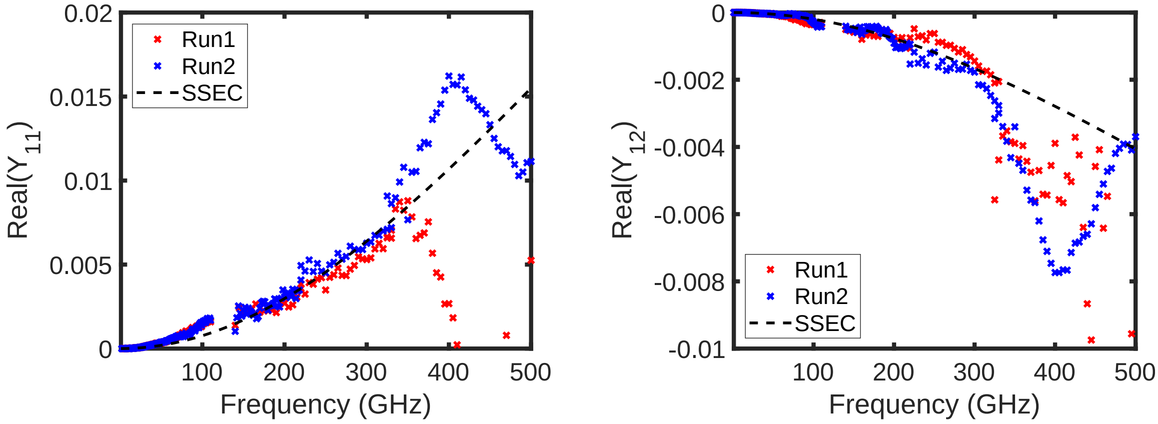
(f) $\angle S_{12}$ in degrees



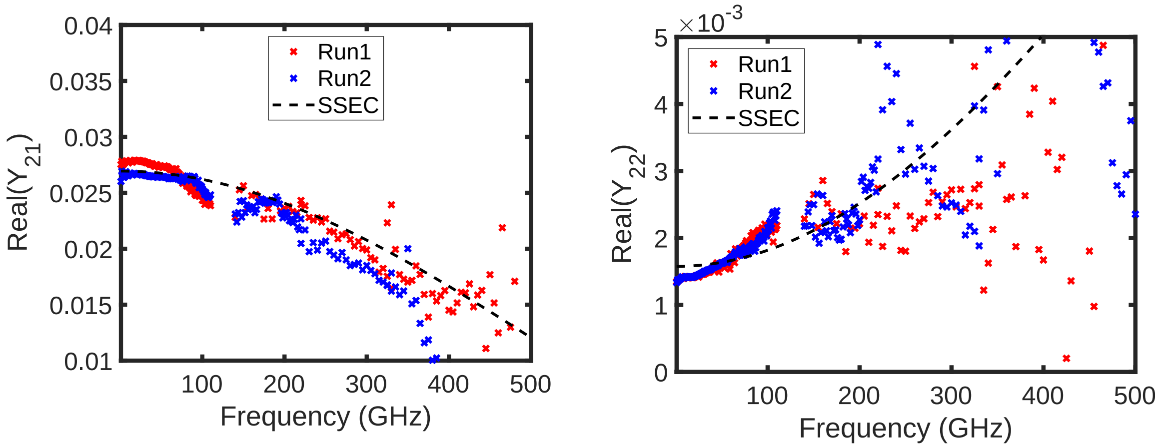
(g) $\angle S_{21}$ in degrees

(h) $\angle S_{22}$ in degrees

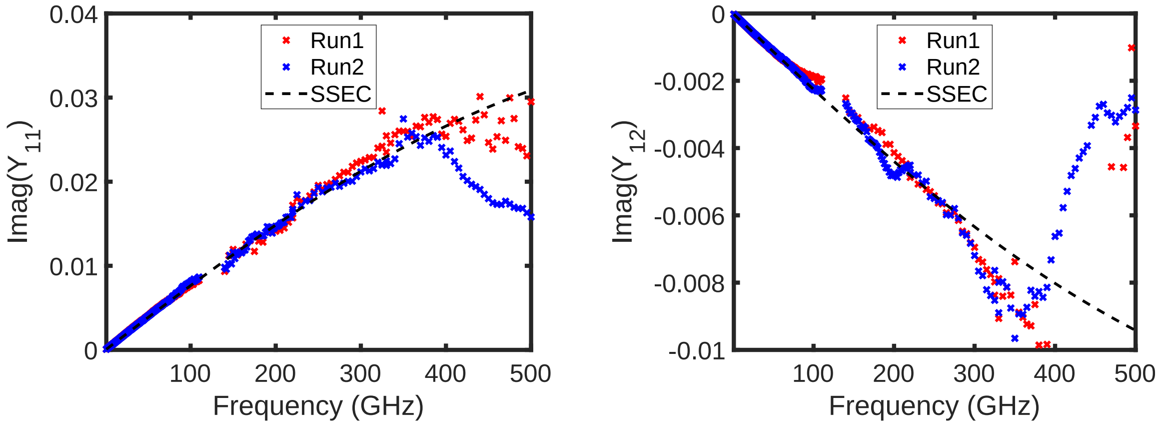
Figure 3.22: S parameters of transistor extracted from measurements on Run2 compared to Run1 and small signal model



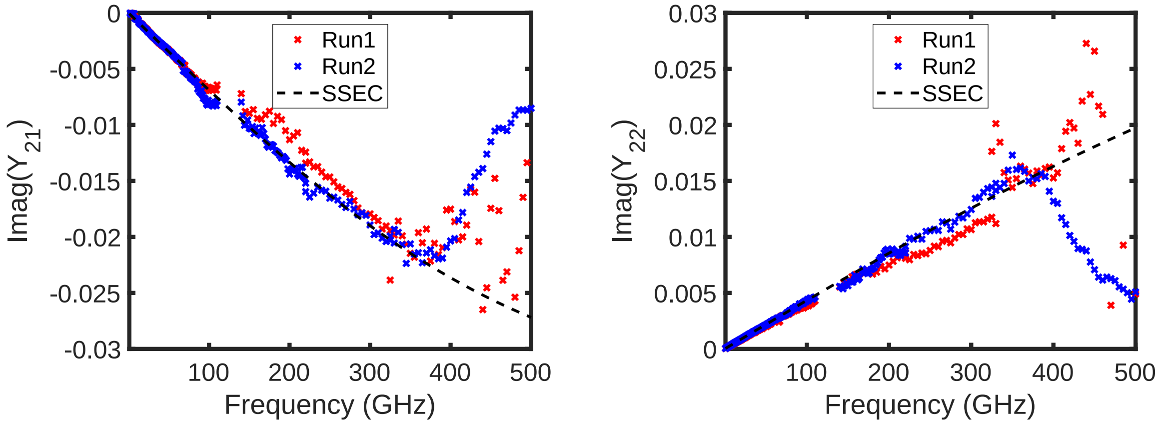
(a) $Real(Y_{11})$ (b) $Real(Y_{12})$



(c) $Real(Y_{12})$ (d) $Real(Y_{22})$



(e) (f) $Imag(Y_{22})$



(g) $Real(Y_{21})$ (h)

Figure 3.23: Y parameters of transistor extracted from measurements on Run2 compared to Run1 and small signal model

3.4.2 Comparison with electromagnetic simulation

The electromagnetic simulation of the TRL calibration kit of Block 1 is performed by making use of the method of EM co-simulation already discussed in the previous chapter (see Fig. 2.34). The transistor figures of merit and parameters extracted from the co-simulation are plotted in Fig. 3.24. The values from the actual measurement results and the reference small signal model of the transistor are also shown in the figure. It can be observed that the EM simulation results are consistent with the measurements. It is interesting to note that many of the measurement trends, particularly the unexpected bends in the parameter plots, are reproduced well by the simulations although with minor differences in the values. Similar inference can also be drawn from the transistor S-parameters plotted in Fig. 3.25 and Y parameters plotted in Fig. 3.26. While performing the actual measurements, there are several sources of error such as the probe positioning errors, noise, ambient temperature drift, and repeatable good contact between the RF probe and the probe pad, and so on. On the other hand, in the simulations, none of these effects come into picture. The probes are always at the same position in each test structure simulated.

Thus, the measurement results being consistent with the simulations suggest that none of the sources of error mentioned above is the reason for the peculiar trends of f_{MAX}, $|S_{11}|$ or $|S_{22}|$. Therefor the most probable cause of these unexpected trends could be an effect of the RF probes and the calibration procedure. In other words, the deviation of the results from the small signal model may be due to the coupling between the probes that is unaccounted for in the TRL calibration procedure.

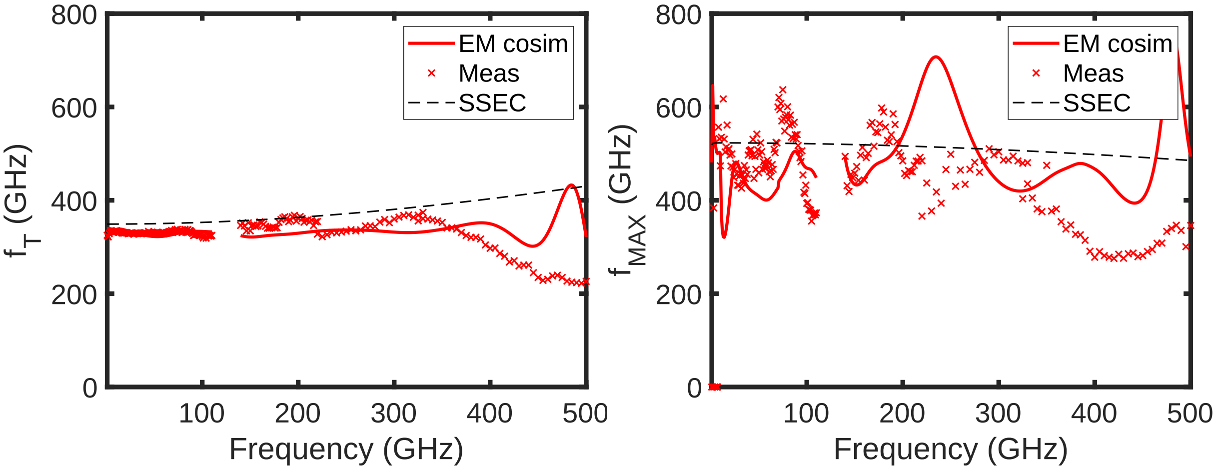
To substantiate this hypothesis, we perform another EM simulation using RF probes that have a reduced effect of coupling [23]. The 3D model of such a probe is shown in Fig. 3.27. Henceforth, this type of probe with less coupling will be referred to as 'quasi Ideal probe' in this work.

3.4.3 EM simulation with quasi-Ideal Probes

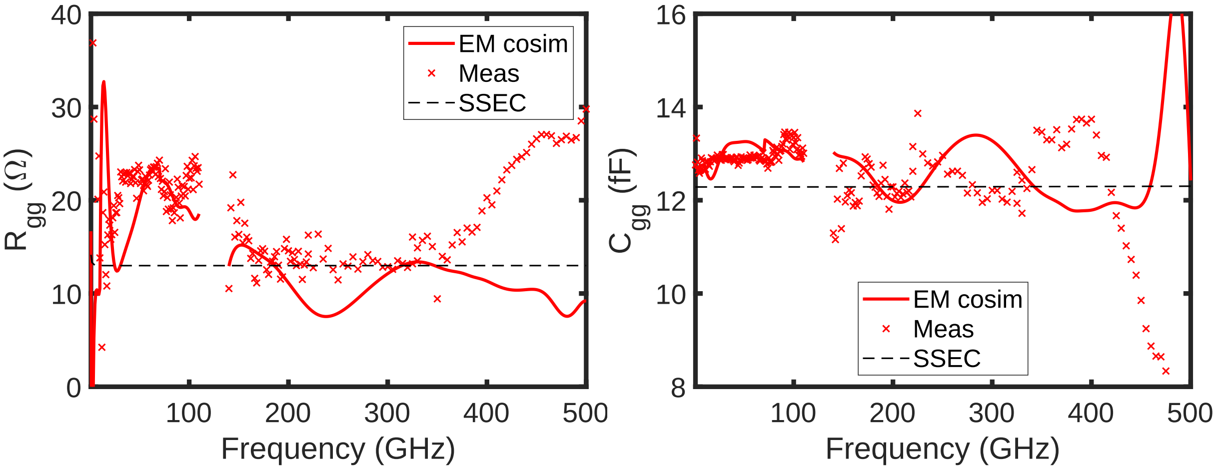
As in Fig. 3.27, the quasi-ideal probes are assumed to have a simple coplanar design, with reduced spacing between the signal and ground lines. This smaller gap has the effect of confining the EM waves more effectively so as to minimize the coupling effects. The probe is also constructed of a thinner metal, thereby reducing the field coupling to the substrate below the probe. This can be observed from Fig. 3.28a, where no coupling of field is observed through the substrate and very little coupling through air. This is in contrast to the high level of coupling that exists with the real RF probes (see Fig.3.28b for Picoprobe). This ideal probe model is used to perform EM simulations on the TRL calibration kit of Block 1.

Again, the electromagnetic simulation of the TRL calibration kit of Block 1 is performed by making use of the method of EM co-simulation already discussed using the quasi ideal probe. The extracted transistor parameters are plotted in Fig. 3.29. The S-parameters and Y parameters are shown in Fig. 3.30 and Fig. 3.31 respectively. The plots from the small signal model are represented using dashed lines.

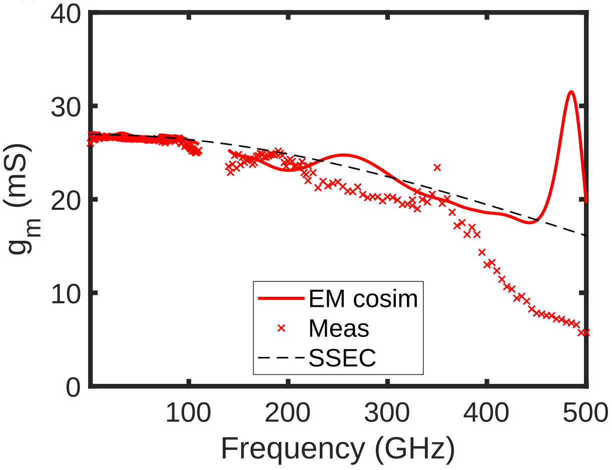
It is well evident from these figures that the parameters extracted from EM simulation with ideal probes have much smoother plots, than those obtained from measurements or simulation using the other RF probes. There is also a very good agreement of these plots with the small signal model plots. In the real measurements, it was seen that the parameters f_{max} and R_{gg}



(a) f_T (b) f_{MAX}

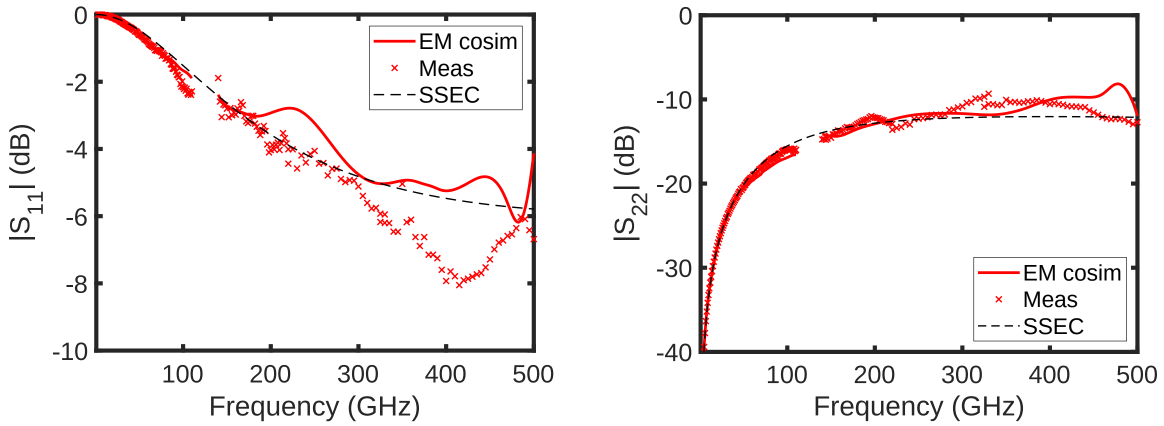


(c) R_{gg} (d) C_{gg}

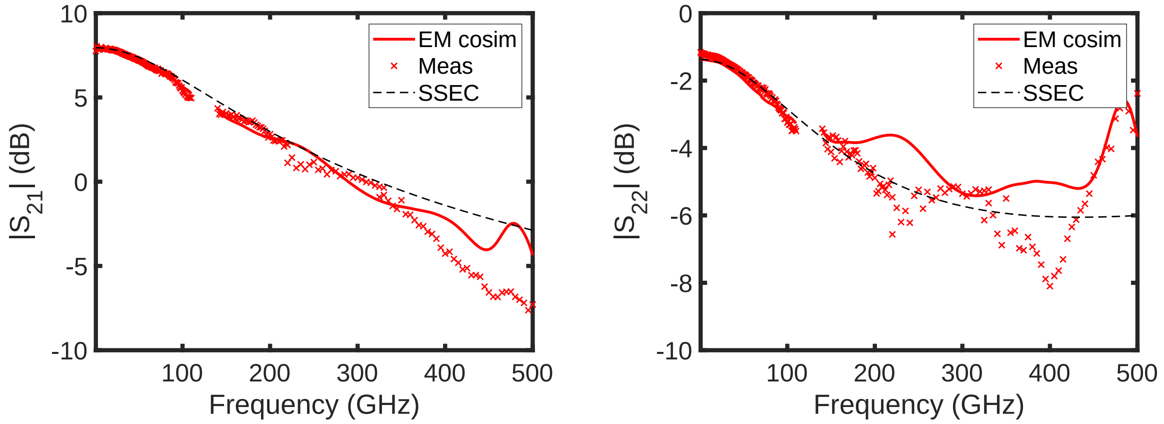


(e) g_m

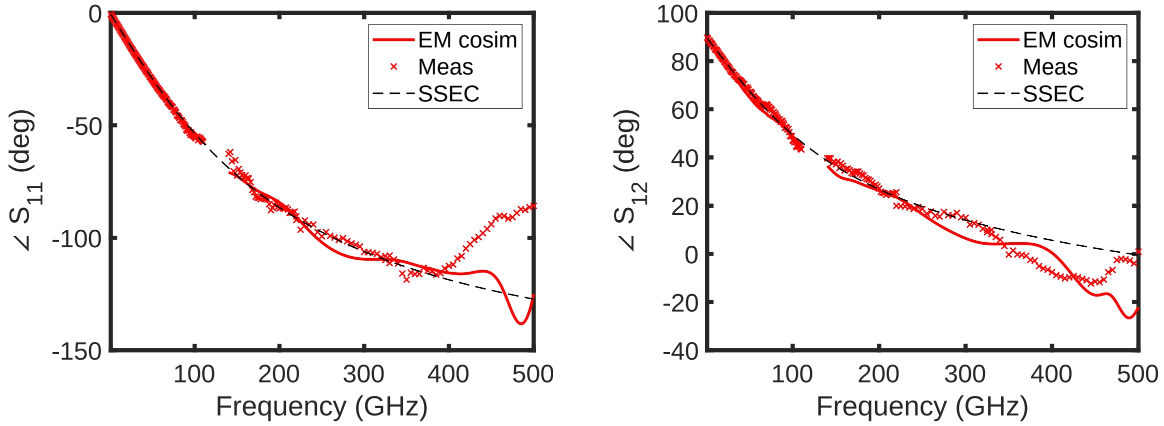
Figure 3.24: Transistor parameters from EM co-simulation



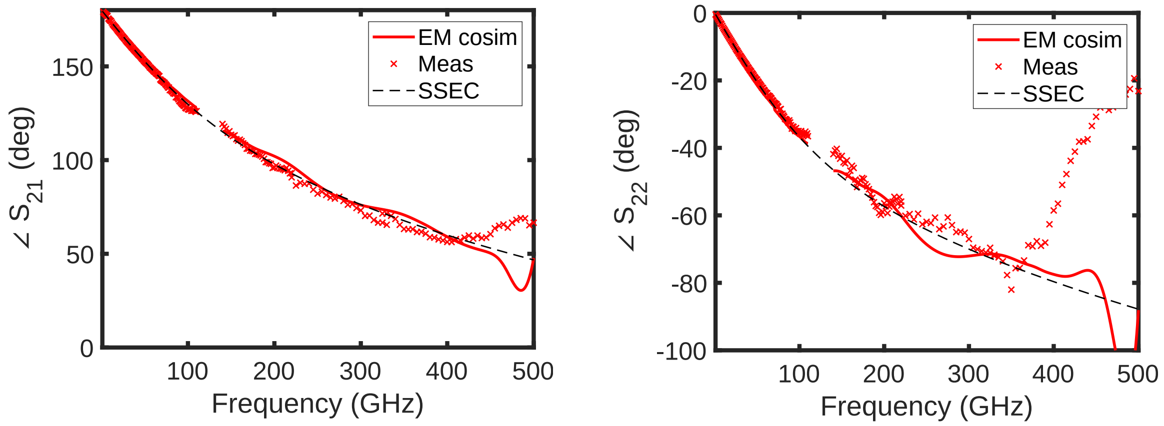
(a) $|S_{11}|$ in dB (b) $|S_{12}|$ in dB



(c) $|S_{21}|$ in dB (d) $|S_{22}|$ in dB

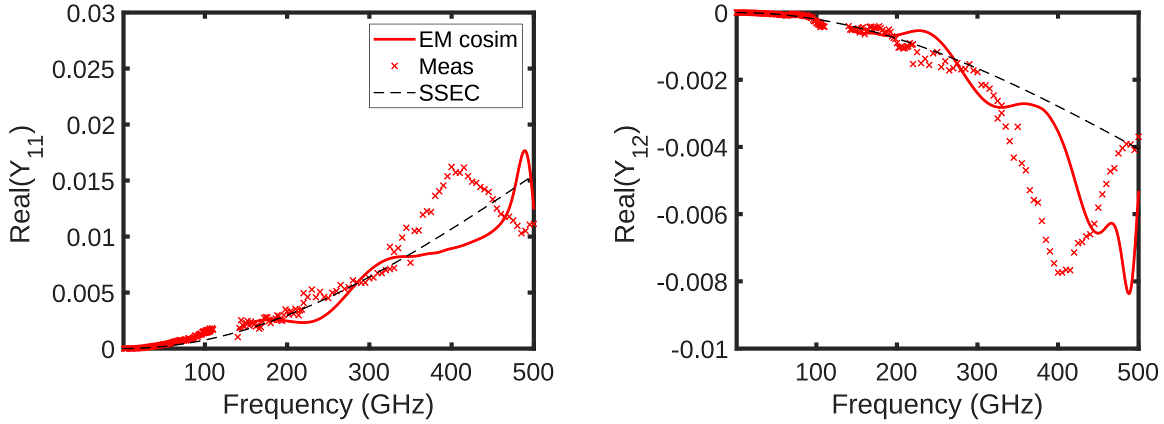


(e) $\angle S_{11}$ (deg) (f) $\angle S_{12}$ (deg)

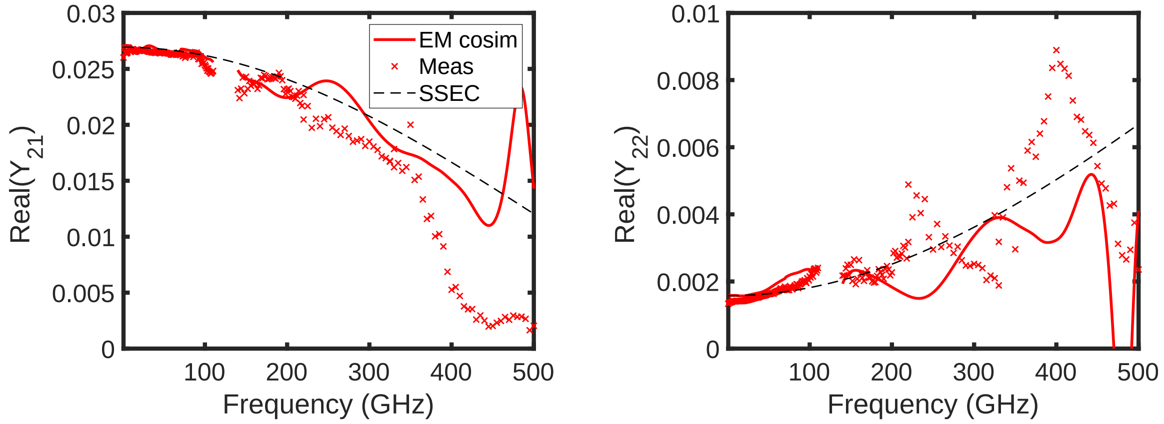


(g) $\angle S_{21}$ (deg) (h) $\angle S_{22}$ (deg)

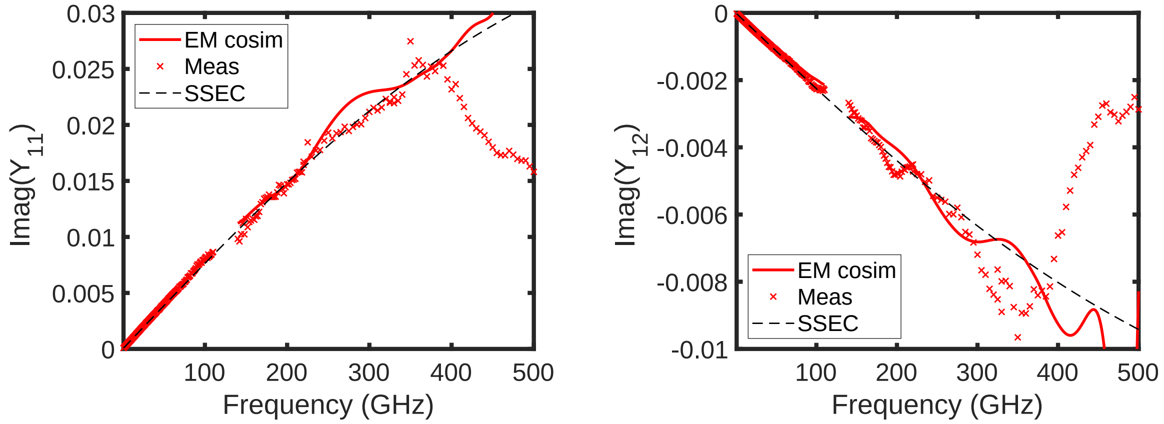
Figure 3.25: S parameters of transistor obtained from EM co-simulation of Run2 test structures



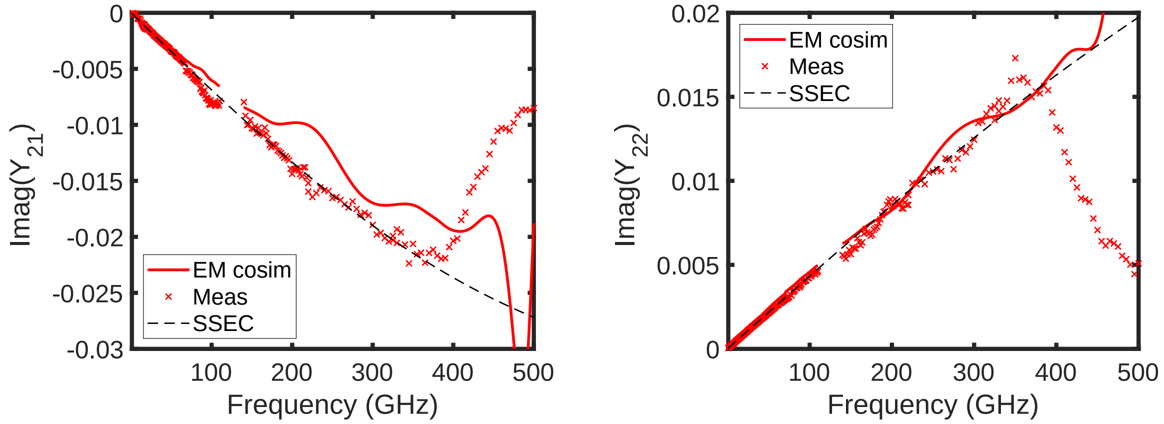
(a) Real(Y_{11}) (b) Real(Y_{12})



(c) Real(Y_{21}) (d) Real(Y_{22})



(e) Imag(Y_{11}) (f) Imag(Y_{12})



(g) Imag(Y_{21}) (h) Imag(Y_{22})

Figure 3.26: Y parameters of transistor obtained from EM co-simulation of Run2 test structures

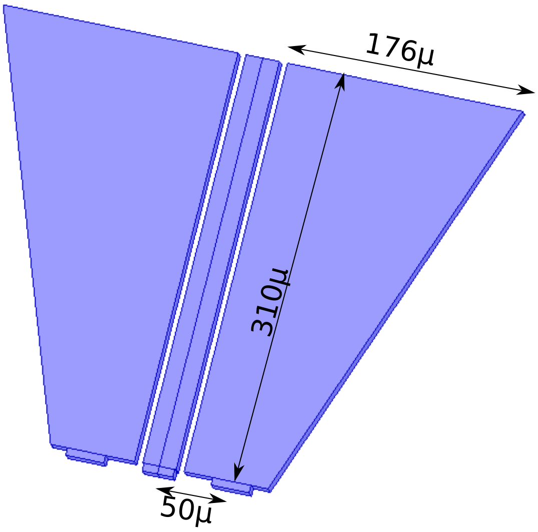
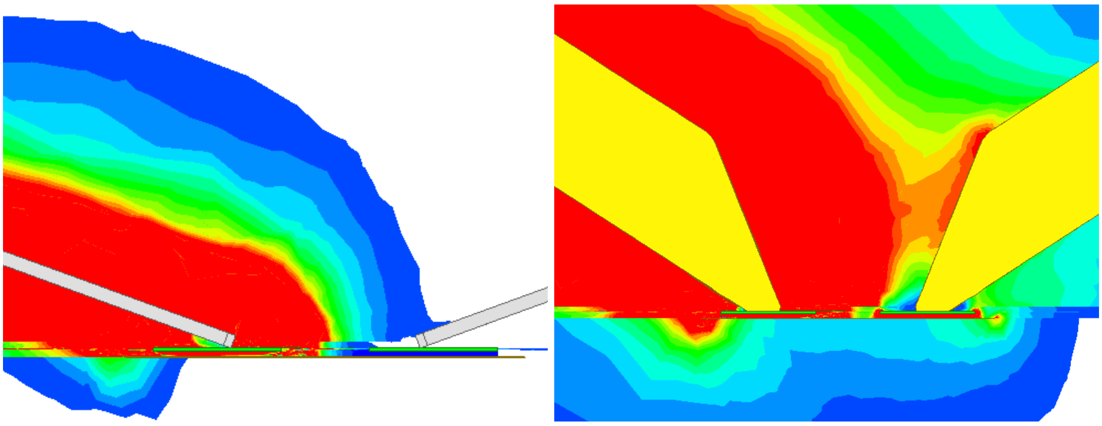
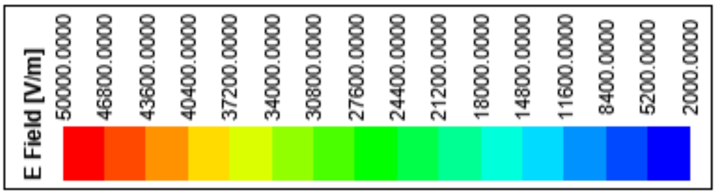


Figure 3.27: 3D model of quasi-ideal probe that has less coupling effects



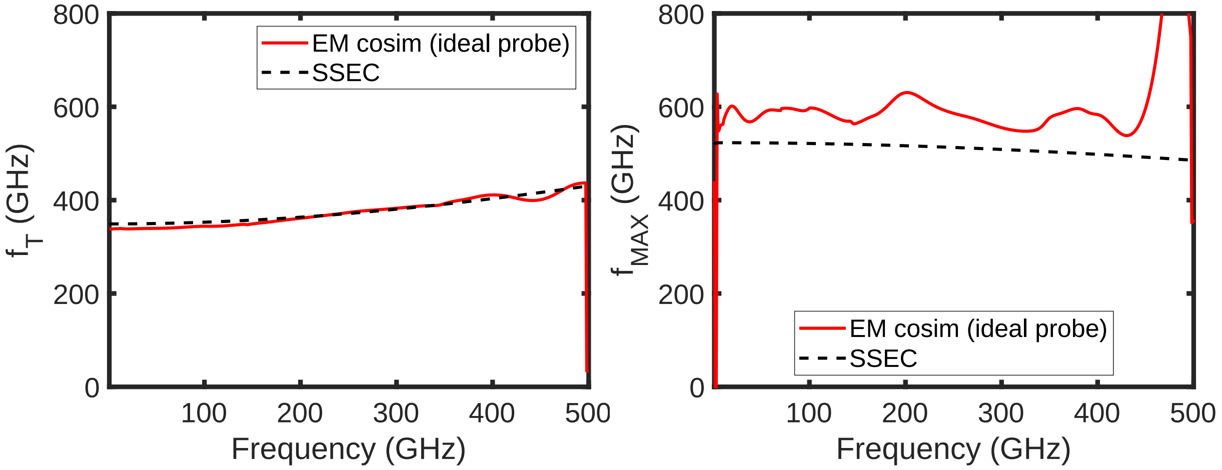
(b) With Picoprobe probe

(a) With Ideal probe

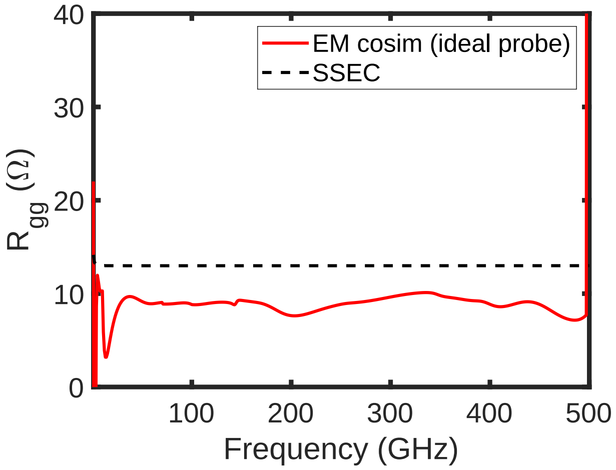


(c) Scale

Figure 3.28: Electric field distribution in Pad Open at 70 GHz when simulated with different probes

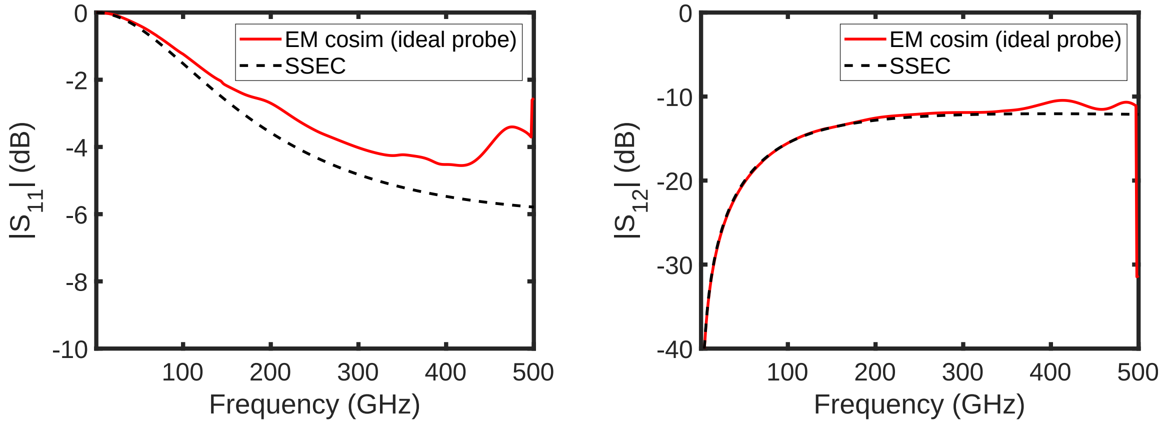


(a) f_T (b) f_{MAX}

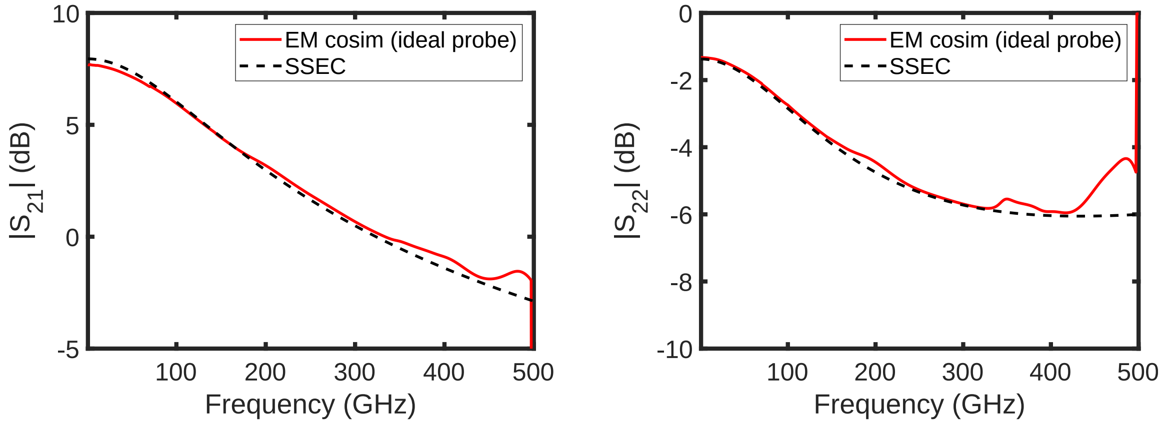


(c) R_{gg}

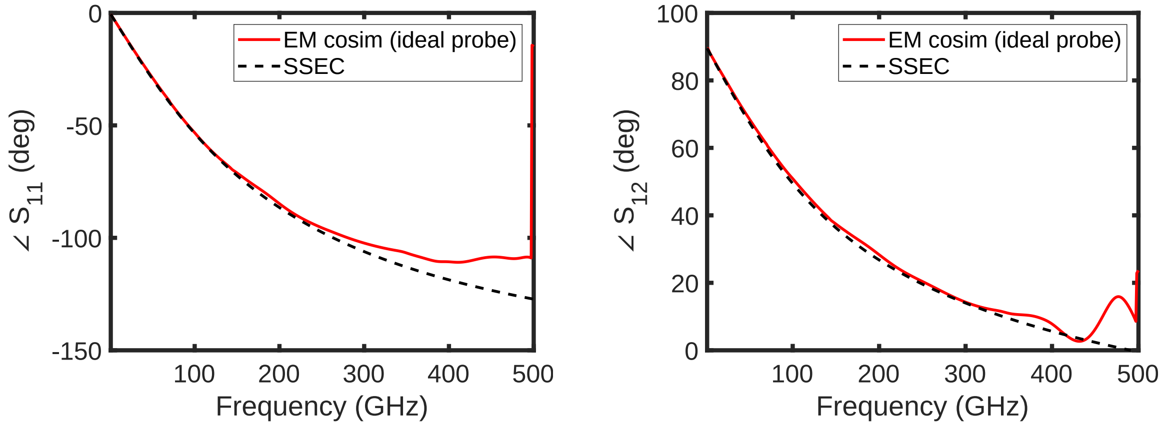
Figure 3.29: EM co-simulation with ideal probes



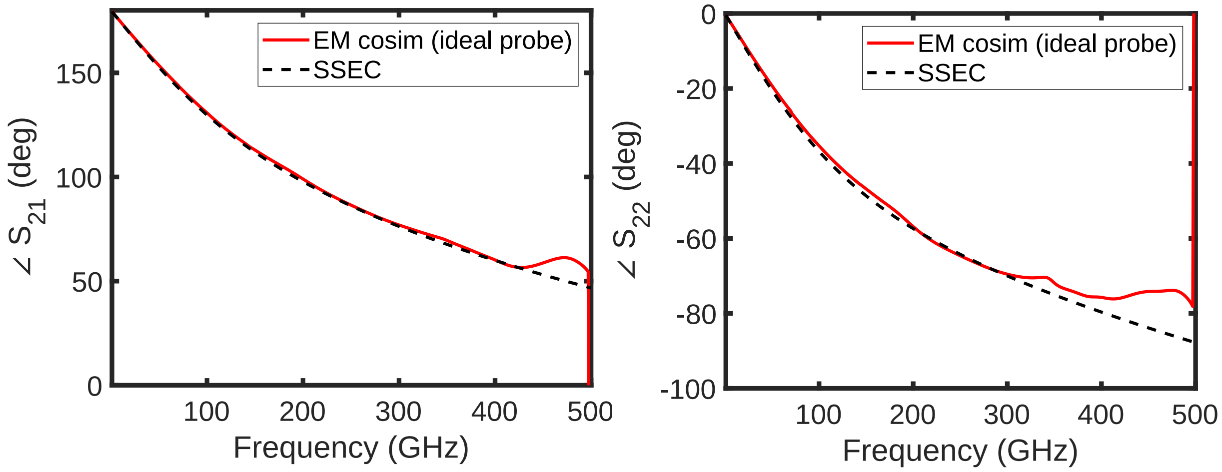
(a) $|S_{11}|$ in dB (b) $|S_{12}|$ in dB



(c) $|S_{21}|$ in dB (d) $|S_{22}|$ in dB

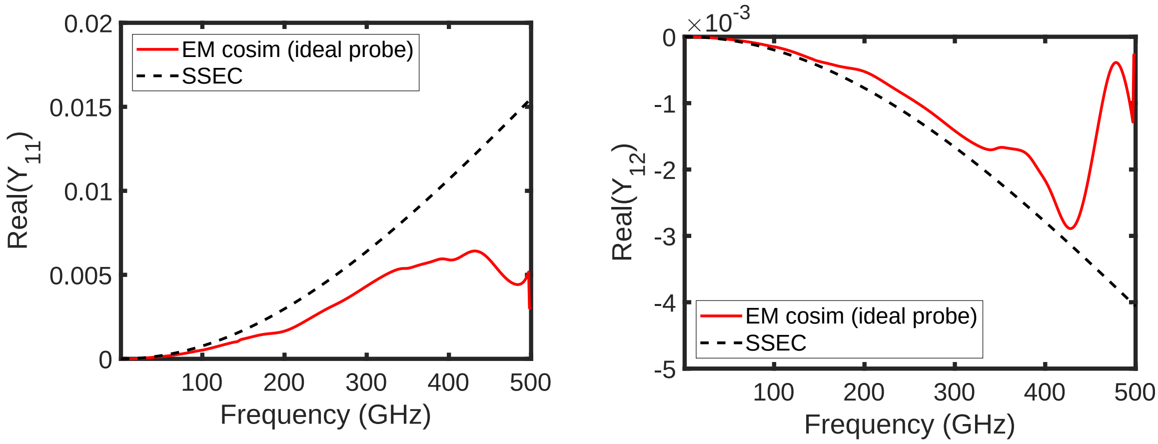


(e) $\angle S_{11}$ (deg) (f) $\angle S_{12}$ (deg)



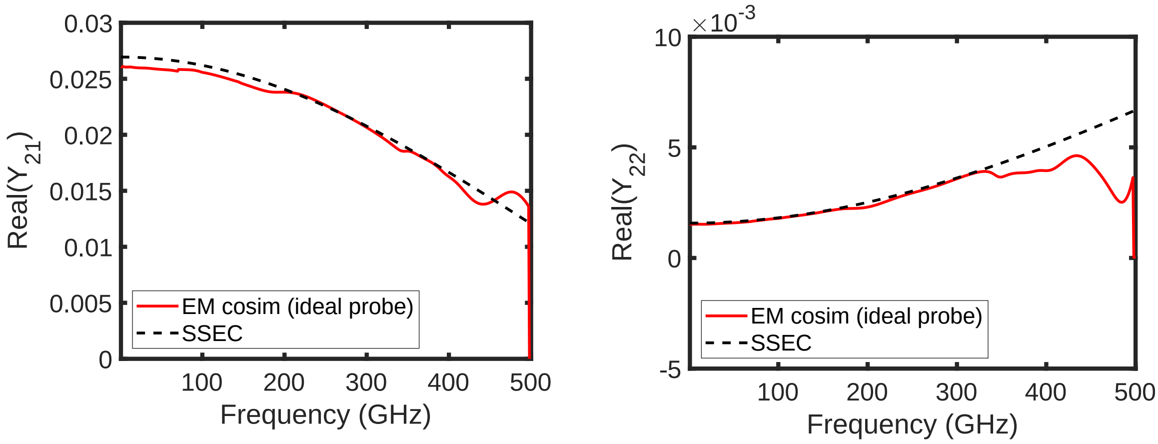
(g) $\angle S_{21}$ (deg) (h) $\angle S_{22}$ (deg)

Figure 3.30: EM co-simulation with ideal probes: S-parameters



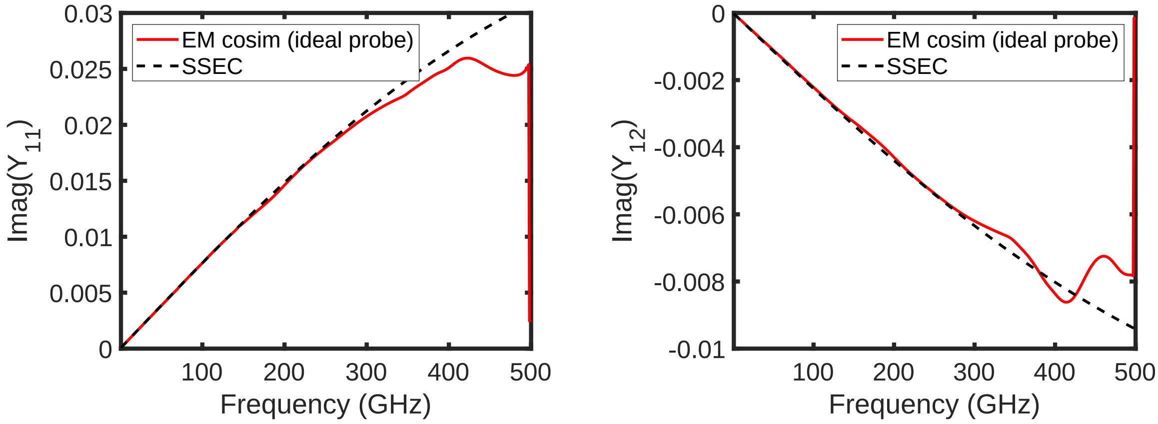
(a) $Real(Y_{11})$

(b) $Real(Y_{12})$



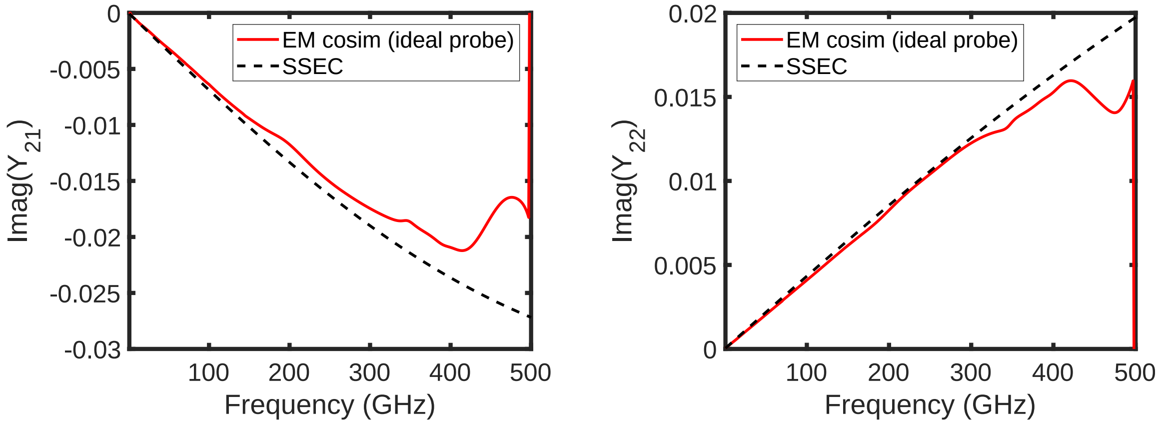
(c) $Real(Y_{21})$

(d) $Real(Y_{22})$



(e) $Imag(Y_{11})$

(f) $Imag(Y_{12})$



(g) $Imag(Y_{21})$

(h) $Imag(Y_{22})$

Figure 3.31: EM co-simulation with ideal probes: Y parameters

fluctuated greatly around the value from the small signal model, thereby bringing in a considerable amount of uncertainty in these parameters. However, with ideal probe simulations, the TRL calibration overestimates f_{MAX} by a reasonable amount (10%).

On-wafer TRL using the ideal probe models is able to reproduce the S-parameter magnitude plots perfectly (Fig. 3.30) except for the small deviation in S_{11}. Similar trends are seen in the Y parameter plots as well with only a small variation in Y_{11}.

From the result of these EM simulations, it can be inferred that a considerable amount of ambiguity in the calibrated results can be removed by adopting techniques to reduce the coupling between probes. However, this type of probe is not commercially available, and therefore the use of an ideal RF probe for measurements is not a realistic solution to improve the accuracy of transistor characterization. Thus we need to look at other methods that improve the calibration accuracy by correcting the error due to probe coupling.

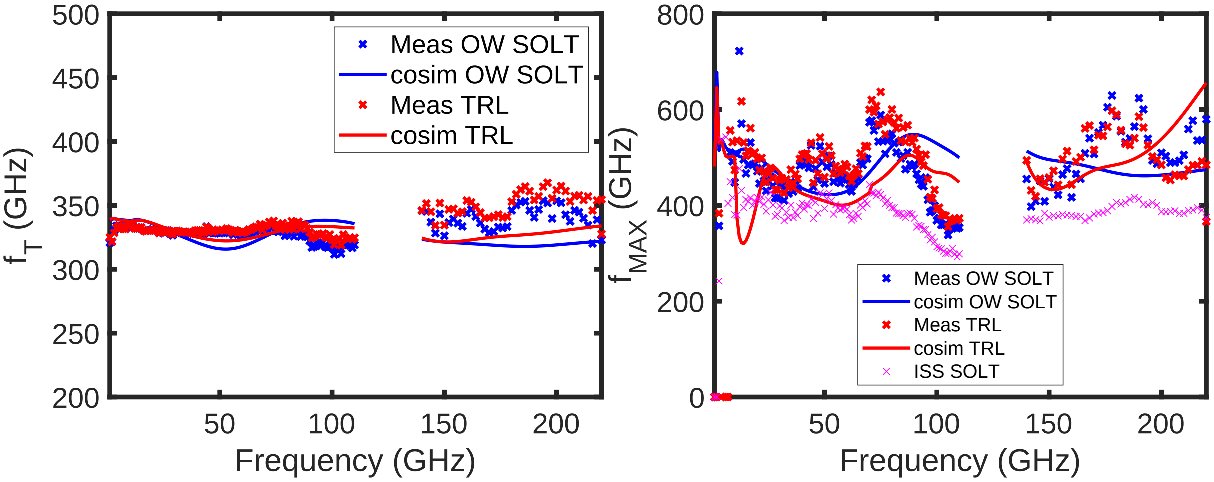
3.4.4 On-wafer SOLT upto 220 GHz

On-wafer SOLT calibration is an attempt to further improve the accuracy of calibration.The presumed inability of TRL to calibrate accurately in the presence of probe coupling (probe-to-probe together with probe-to-substrate) has been demonstrated in the preceding sections. The EM simulation with ideal probes has been able to confirm this hypothesis that the crosstalk and the probe-substrate coupling are the main reasons for this inaccuracy.

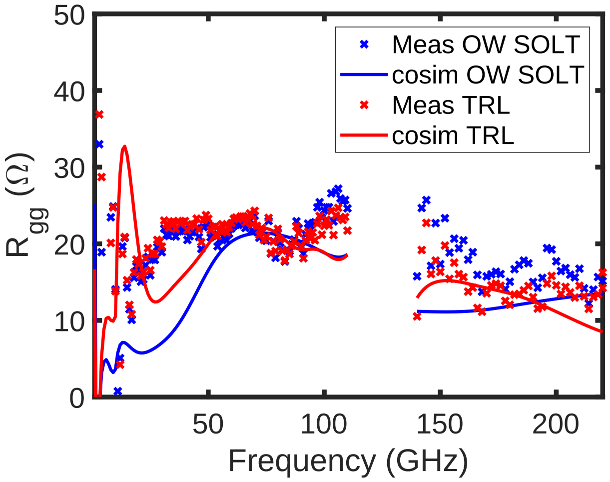
One workaround would be to utilise the SOLT calibration but with on-wafer standards (referred to as on-wafer SOLT calibration). The use of on-wafer standards eliminates the problem of change of substrate associated with off-wafer SOLT calibration. As the SOLT calibration makes use of the 12-term error model for error correction, there exists additional terms that can account for the crosstalk between probes. Thus, in an ideal scenario, the use of on-wafer SOLT is expected to reduce the effects of probe-to-probe coupling. However, as the frequency increases, particularly above 220 GHz, the distributed parasitic effects come into play, and the calculated parameters of the SOLT standards are no longer frequency independent and their extraction is not trivial.

For an off-wafer SOLT, the parameters of the Short, Open Load and Thru standards are provided by the manufacturer. To perform the on-wafer SOLT calibration, the following on-wafer standards designed originally for TRL were chosen: Pad Short, Pad Open, Pad Load and Thru. Hence, to perform the on-wafer SOLT, it is necessary to first extract these frequency independent parameters of our on-wafer standards. There are 2 possible ways to obtain these values. The first method is to apply TRL calibration on the standards, and then extract their respective parasitics from this calibrated S-parameters. This method has the problem of reproducing some of the errors introduced during TRL calibration. The second method makes use of intrinsic EM simulations of the calibration standards to extract their parameters. This however, is an an overly optimistic estimation of the values as the simulations are performed under near-ideal conditions.

In this discussion, the parameters for on-wafer SOLT calibration are extracted after applying TRL calibration on the standards. On-wafer SOLT is followed by a Pad/Short/Open de-embedding to shift the reference plane to the DUT terminals. The transistor parameters thus obtained from measurements and EM simulations are plotted in Fig. 3.32. The TRL calibrated data (measurement and simulation) are also plotted in each figure for reference with the same reference plane.

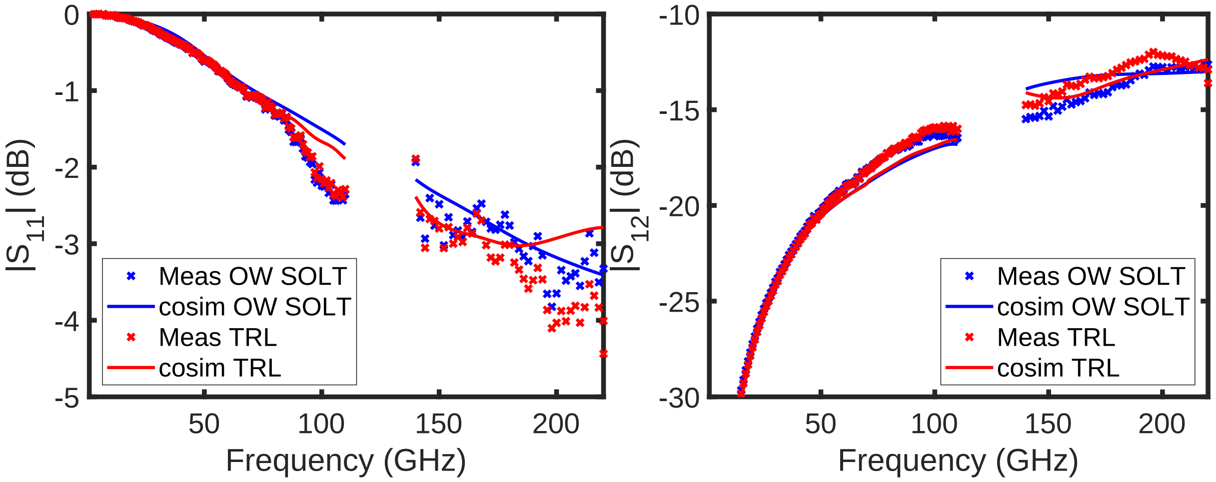


(a) f_T (b) f_{MAX}

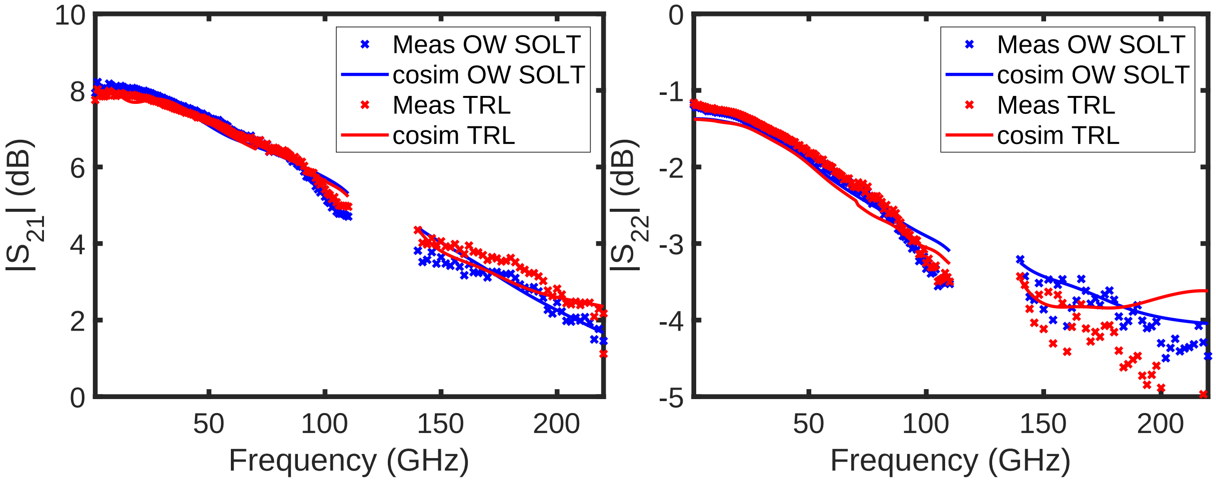


(c) R_{gg}

Figure 3.32: Transistor parameters extracted using on-wafer SOLT calibration

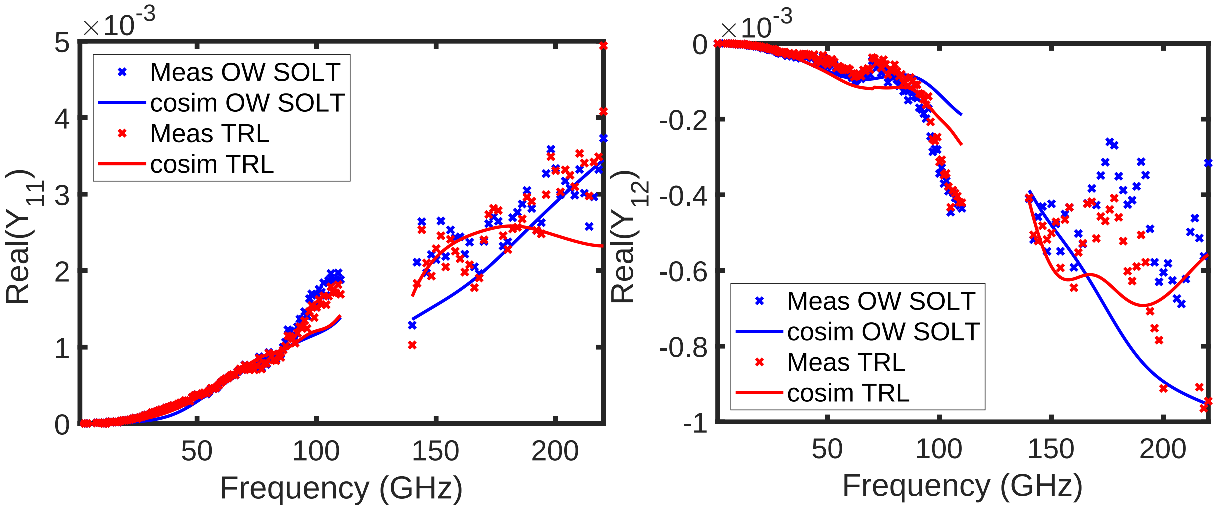


(a) $|S_{11}|$ (dB) (b) $|S_{12}|$ (dB)

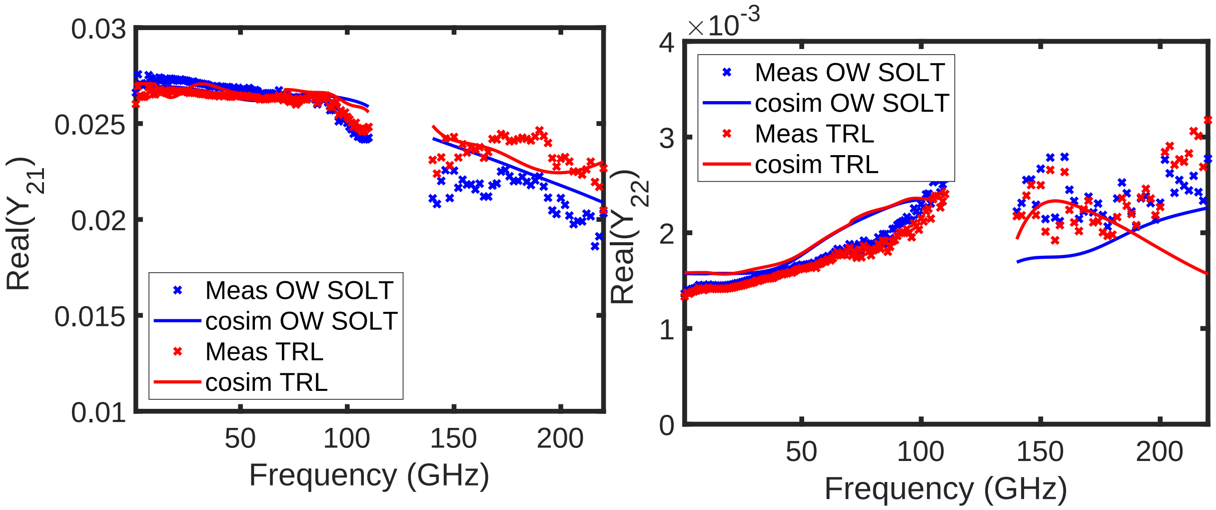


(c) $|S_{21}|$ (dB) (d) $|S_{22}|$ (dB)

Figure 3.33: On-wafer SOLT: S parameters



(a) $Real(Y_{11})$ (b) $Real(Y_{12})$



(c) $Real(Y_{21})$ (d) $Real(Y_{22})$

Figure 3.34: On-wafer SOLT: Y parameters

It is observed from these results that on-wafer SOLT does not bring clear improvements, although a slightly better accuracy is noticed with the EM co-simulation of on-wafer SOLT in the second frequency band.

The S-parameters and Y parameters of the transistor are plotted in Fig. 3.33 and Fig. 3.34 respectively. The magnitude plots of S_{11} and S_{22} exhibit more smoother curves in the second measurement band when calibrated using on-wafer SOLT. Similar observations can also be made from the Y parameter plots.

In the f_{MAX} plots in Fig.3.32b the value extracted from off-wafer (ISS) SOLT is also shown for comparison. We see that the f_{MAX} from the ISS SOLT is nearly 100 GHz lower than the on-wafer SOLT values, despite using the same algorithm for both plots. Thus the error comes from the parameters of the SOLT standards, and not the actual calibration method employed.

These observations affirm the fact that the peculiar trends noted in the plots from TRL calibration are an effect of the crosstalk or coupling between the RF probes, which is partly corrected by the methods discussed here. The error correction is not complete because the SOLT parameters are extracted from the TRL data, and can have errors already introduced by TRL. Yet, the coupling of the probe to the substrate stays uncorrected and remains a source of error. Despite these promising results from on-wafer SOLT, unfortunately this method cannot be utilised for calibration above 220 GHz, as already discussed in the preceding paragraphs.

Nevertheless, another limitation of the SOLT can be underlined: the crostalk error terms within the SOLT are settled at the input of the input quadripole and at the ouput of the ouput quadripole of errors terms (see Fig. 1.10) which is not appropriate in our case. Indeed, for on-wafer measurements the crosstalk is mainly due to the probe coupling, i.e. above the DUT. Another option that has not been tested within this work would be to make a first tier calibration on ISS using TRL for example followed by a second tier calibration using the on-wafer SOLT. This scheme would have the advantage to set the error term of the crosstalk e_{30}, e'_{03} physically at the probe position.

3.5 Comparison of different blocks

The TRL calibration kit analysed so far in this Chapter is the Block 1, the reference block. As already mentioned at the start of the Chapter, 3 more calibration kits have been designed, fabricated and measured. The performance of these three blocks will be discussed in this section, in comparison with the reference block.

3.5.1 Significance of ground plane design

It is stated in [81] that the microstrip lines fabricated using BiCMOS technology are less lossy compared to the digital CMOS technology and that this higher level of losses can affect the measurement accuracy of the RF FoMs of the transistor. Fig. 3.35 reproduced from [81] illustrates this loss. This fact has also been observed from the measurements performed using our TRL test structures of Run1 or Run2. On comparing the microstrip line designs used in BiCMOS and FDSOI technology, the main difference observed is the width of the line due to a 1.5 times thicker dielectric of the BEOL of the BiCMOS compared to the FDSOI technology. This is the first reason for the reduction of line losses in the BiCMOS compared to the FDSOI. Another reason is the use of thick copper top metal in the BiCMOS technology compared with a thinner

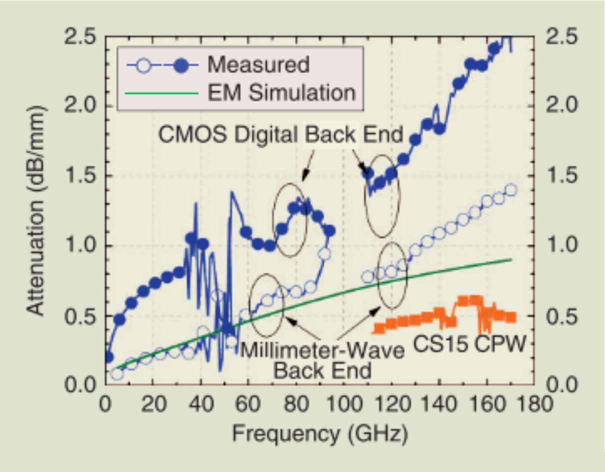


Figure 3.35: Attenuation in the lines fabricated using different technologies (reproduced from [81])

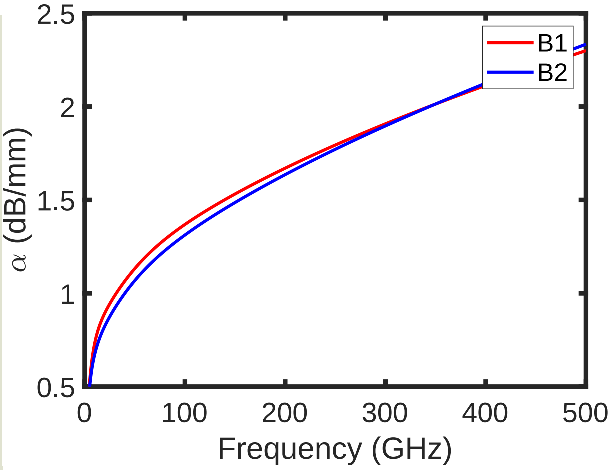


Figure 3.36: Attenuation in Block 2 microstrip line obtained from EM simulation (B1 values for reference)

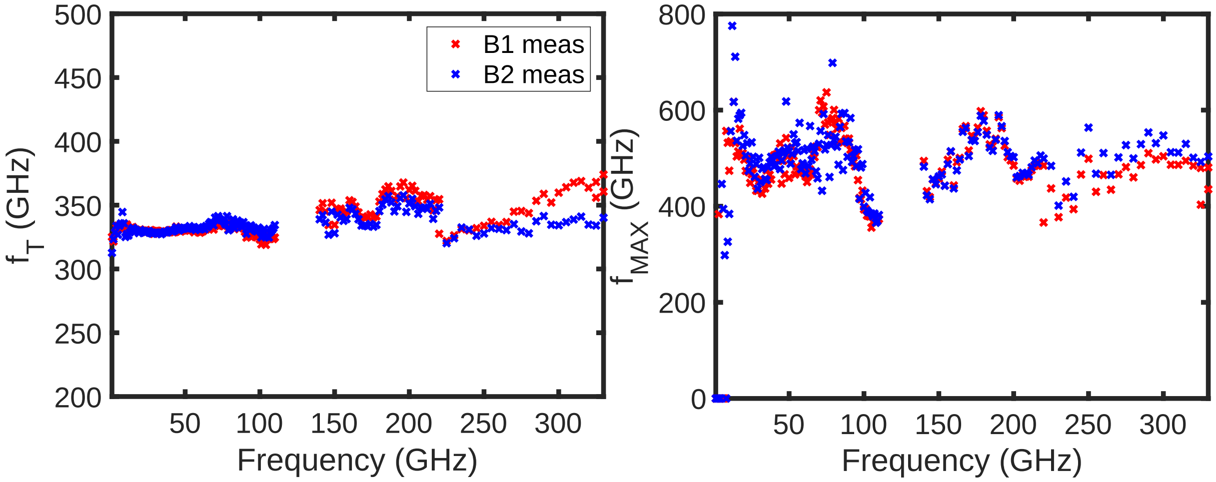
aluminium top metal in the FDSOI. Finally a last thing that has not been evaluated and which is the topic of this sub-chapter is the design of the ground plane. Indeed, the M1 metal layer thickness of FDSOI is only 100 nm which is nearly two times thinner than those of the BiCMOS. Hence, while the ground plane of micrsotrip lines from BiCMOS technology uses only the lowermost metal layer (Ml) to realise the ground plane, it was decided as the first guess to use a mesh of the two lowermost layers (M1 & M2) (see Fig. 2.2 for the BEOL of FDSOI technology).

In view of these differences between the two technologies, it is interesting to understand the reason behind the higher losses in FDSOI technology. Unfortunately, an accurate EM simulation study could not be undertaken in this regard as the EM solver does not solve for fields within a metal. Although HFSS has the option to activate 'Solve Inside', this is an unrealistically time and memory consuming task. Thus, the Block 2 design with a single ground plane layer has been conceived to experimentally study its effect on the accuracy of TRL calibration.

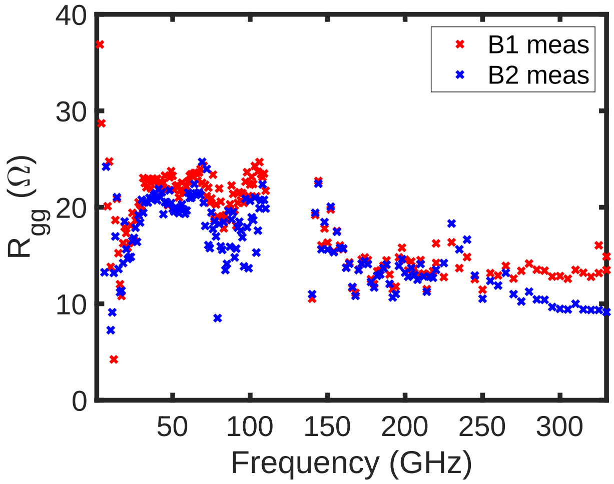
The layout of the M1 ground plane of Block 2 has already been discussed in Section 3.2. As the ground plane requires only one metal layer, it implies a larger spacing or thicker oxide between the ground and the microstrip line (LB layer). This larger spacing leads to a wider line to maintain the 50 Ω characteristic impedance as compared to the Block 1 lines. Thus, a less lossy line is theoretically expected in Block 2. Despite the inaccuracies, an intrinsic EM simulation of the Block 2 microstrip line has been performed to have an estimate of the loss. This simulation takes only into account the improvement due to the increase of the line width but as explained does not take accurately the effect of the GND plane. The attenuation of the Block 2 line as obtained from its intrinsic EM simulation is plotted in Fig. 3.36.

The reduction in attenuation (α) in Block 2 is very minute. This change is likely due to the wider lines used in the second block. Since, the simulator does not solve inside the metal of the ground plane, the electric field distribution does not shown any difference between B1 and B2, and thus the effect of the ground is not correctly taken in to account by the simulator. Therefore, the measurements on the transistor are performed using B2 to asses whether the transistor parameters are really affected by its ground plane design or lower attenuation.

The measurements are performed from 1 to 330 GHz and the extracted transistor parameters are plotted in Fig. 3.37. The S parameters of the transistor are presented in Fig.3.38. Comparison is made with Block 1 parameters in these figures. It can be observed that the results from



(a) f_T (b) f_{MAX}



(c) R_{gg}

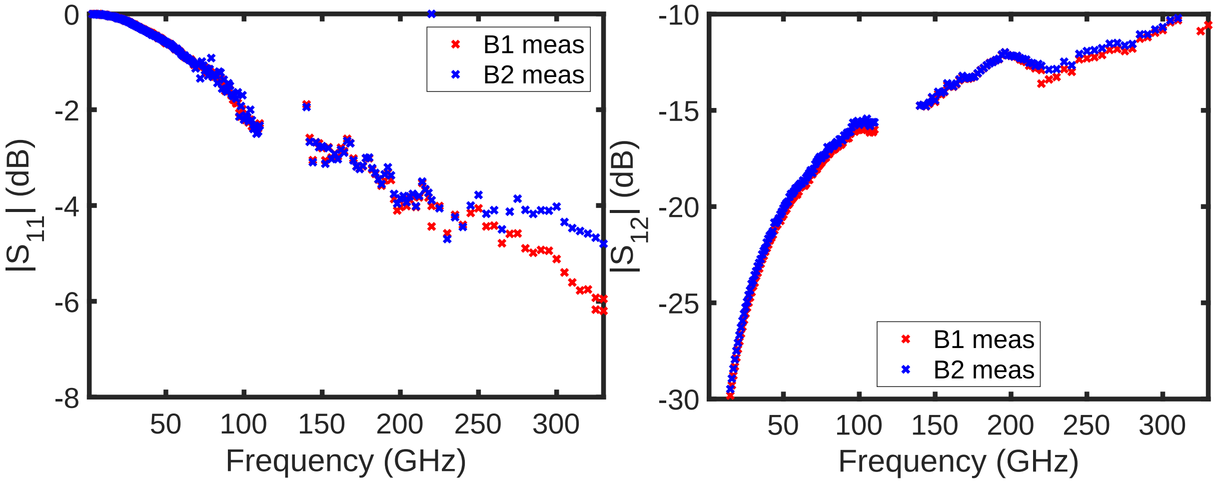
Figure 3.37: Transistor parameters extracted from TRL measurements using Block 2

B2 are more or less the same as those from B1. There are small variations in some parameters ($f_T, R_{gg}, |S_{11}|$) in the last band measurements, which can be attributed to the manual error in making the contacts between the RF probe and the probe pad.

Thus it can be concluded that this block does not show any improvement in measurement accuracy over the reference block B1. In other words, the small reduction in the line attenuation is not sufficient enough to bring in a noticeable change in the transistor parameters. Moreover, the RF measurements on the lines do not show any decrease in attenuation as measurements are inherently noisy and it is impossible to detect the small improvement within the uncertainty range due to this noise.

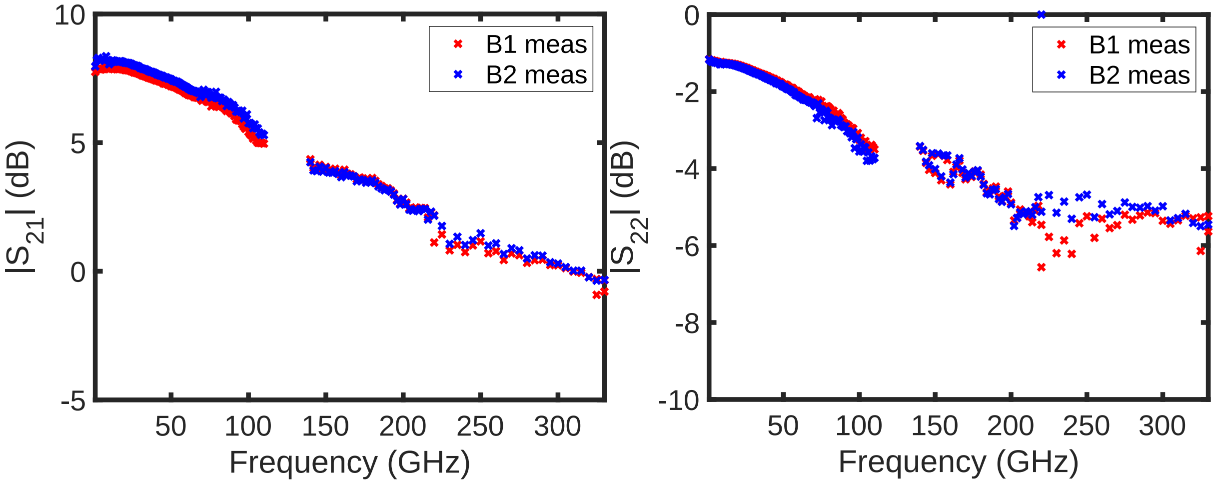
3.5.2 Effect of line Z_c

It is known that the reference impedance of S-parameters after TRL calibration is equal to the characteristic impedance of the line standards [62], which necessitates the need for impedance correction of 50 Ω reference. As an example the f_{MAX} extracted after TRL calibration using Block1 is presented in Fig. 3.39 with and without impedance correction. Although the lines



(a) $|S_{11}|$ (dB)

(b) $|S_{12}|$ (dB)



(c) $|S_{21}|$ (dB)

(d) $|S_{22}|$ (dB)

Figure 3.38: S-parameters of transistor extracted from TRL measurements using Block 2

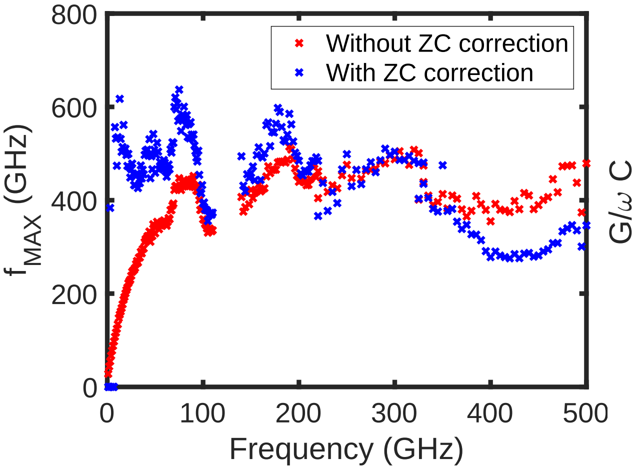


Figure 3.39: Effect of impedance correction on extracted f_{MAX}

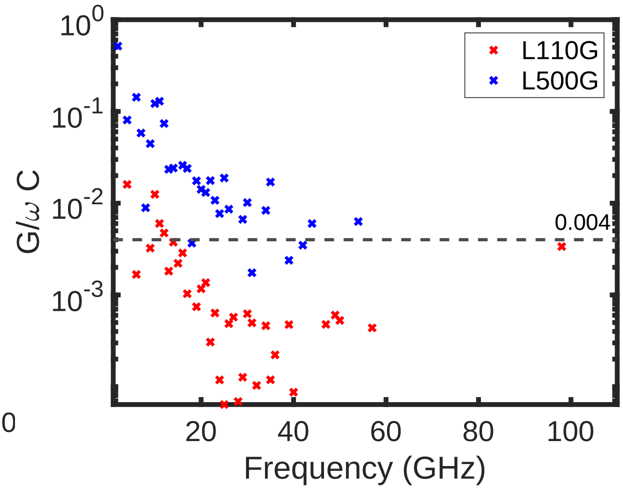


Figure 3.40: Measured value of $G/\omega C$ for the different lines in Block 1

of Block 1 have been designed with 50 Ω impedance, it can be seen from the figure that there is a considerable difference in the values with and without impedance correction, particularly at low frequencies (below 100 GHz). Thus, an error in impedance correction can bring in a significant amount of error in the transistor parameters.

The methodology we have adopted for impedance correction on the TRL measurements, that has already been discussed in detail, is based on an assumption that the conductance of line (G_{line}) is negligible or $G/\omega C$ is less than 0.004. This $G/\omega C$ as calculated from the measurements on Block 1 for two line standards is plotted in Fig. 3.40. Although the assumption is true for most of the frequencies, we see from the figure that there are violations at some points.This has led us to question the accuracy of the impedance correction procedure. Moreover, the dielectric loss tangent ($tan\delta$) that determines the value of of G_{line} of the line standards is not well modelled by the EM simulator due to the complex stack of dielectrics in the BEOL. Hence an EM simulation study on this aspect can also be eventually unreliable.

The Block 3 has been designed in order to provide an experimental answer to this question on the accuracy of the impedance correction procedure. Thus, the Block 3 has been made with transmission lines of non 50 Ω characteristic impedance. The value of Z_c is chosen to be lower than 50 Ω as this would also have a minor advantage by reducing the line attenuation due to increased line width. Fig. 3.41 shows the characteristic impedance of the lines extracted from the intrinsic EM simulation. However, the reduction in the line attenuation in B3 due to this line design, is very small as can be seen by the green curve in Fig. 3.42. Therefore, no noticeable difference in measurement accuracy is expected over B2 (or B1) due to the lower losses.

The measurements on Block 3 have been performed from 1 to 330 GHz and the transistor parameters extracted after on-wafer TRL calibration. The results obtained are presented in Fig. 3.43. It can be observed that the results from both B1 and B3 are very similar. This leads to the conclusion that irrespective of the characteristic impedance of the transmission lines of the calibration kit, the results are the same. In other words, the procedure followed for impedance correction performs satisfactorily.

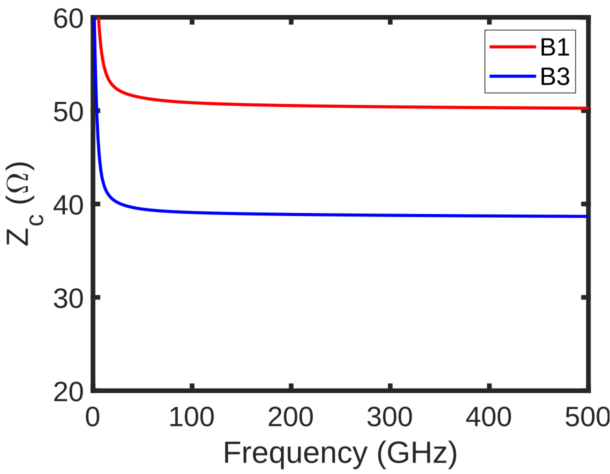


Figure 3.41: Characteristic impedance of the lines from Block 3

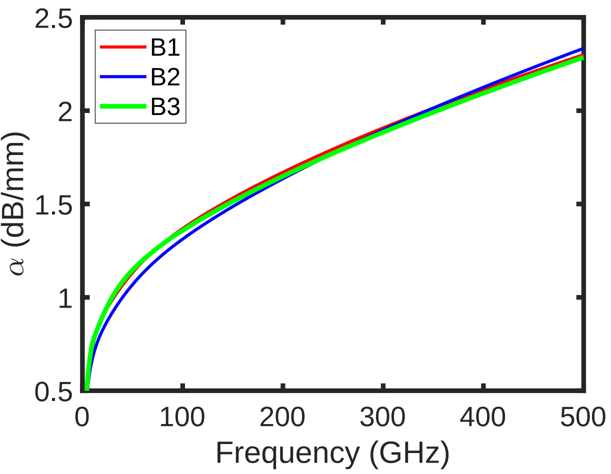
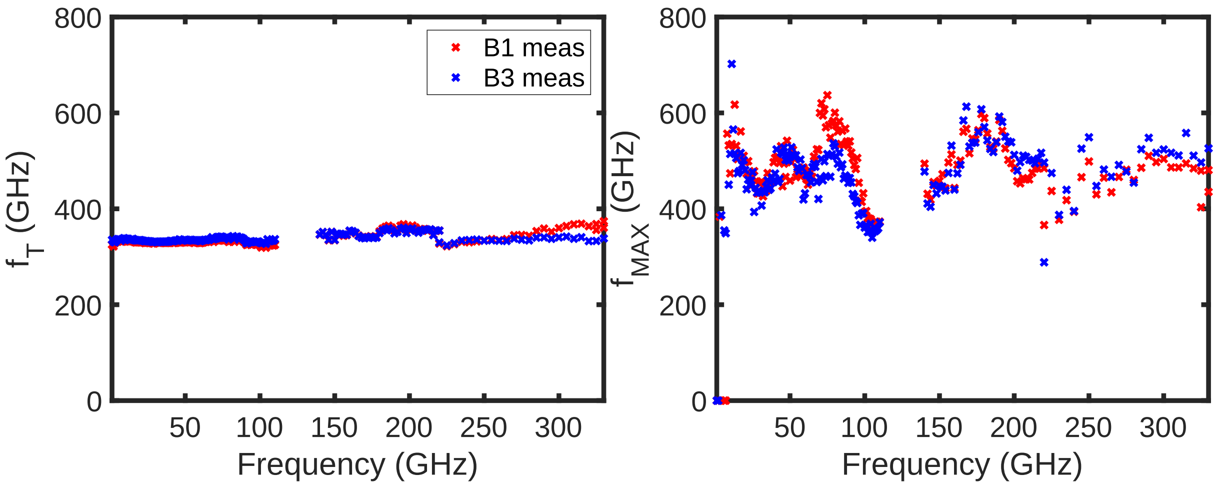
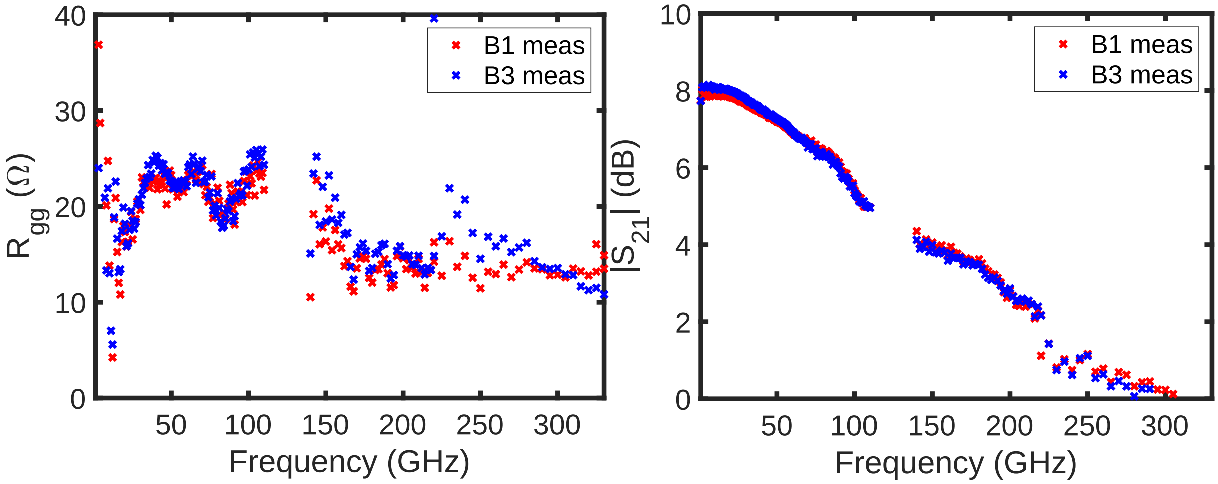


Figure 3.42: Attenuation (simulated) in Line_500G from Block 3 as compared to the other blocks



(a) f_T

(b) f_{MAX}



(c) R_{gg}

(d) $|S_{21}|$ (dB)

Figure 3.43: Measured transistor parameters from Block 3 compared to Block 1 values

3.5.3 Effect of continuous Ground Plane

It is suggested in [9] that the calibration kit designed with a continuous ground plane below all the test structures can reduce multimode propagation and eliminate slot modes. The benefit of such a design using test structures from STMicroelectronics BiCMOS 55nm technology has been demonstrated in [86]. In this section, the on-wafer TRL calibration kit designed with a continuous ground plane and pad shields (B4) is compared with the TRL calibration kit without these (the reference block B1), focusing on measurement discontinuities. The discussion is limited to the first frequency range (1-110 GHz) because the RF probes used in this range present more coupling than the higher frequency probes.

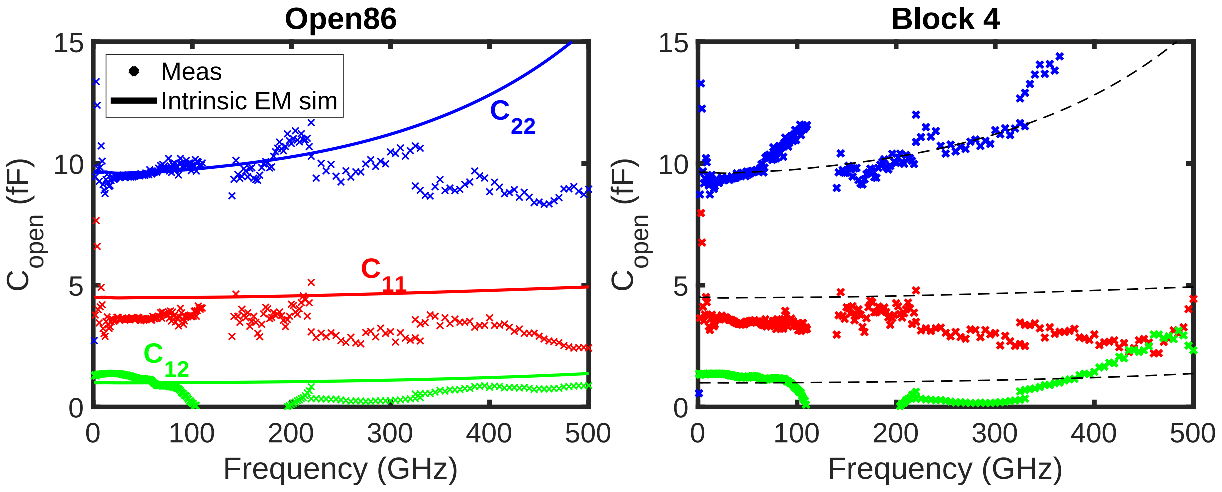
In the frequency range of 1-110 GHz, two LINE standards are inevitable to cover the complete band.Therefore, the measurement discontinuity at the frequency limit (point where the line change is made during calibration)is studied with the aid of Electromagnetic (EM) simulations,providing insights into the origin of the discontinuity.

The passive DUTs are first calibrated to extract the parasitic capacitance of the Transistor Open and the parasitic inductance and resistance of the Transistor Short. These parasitics extracted from measurements on Block 1 (B1) and Block (B4) are plotted in Fig. 3.44 and compared with those from the intrinsic EM simulation of these structures. Comparing the plots from B1 and B4, there exists a better continuity in the measurements from B4. It is also observed that the EM simulations well reproduce the Open measurements. Regarding the Transistor Short, the agreement is quite satisfying in spite of the 1-2 pH difference which can be due to the probe positioning errors. The good agreement between the measurement results and the EM simulations confirms the accuracy of the simulations used. These parasitics are de-embedded from the calibrated measurements of the Transistor and its parameters are extracted as in Fig. 3.45.

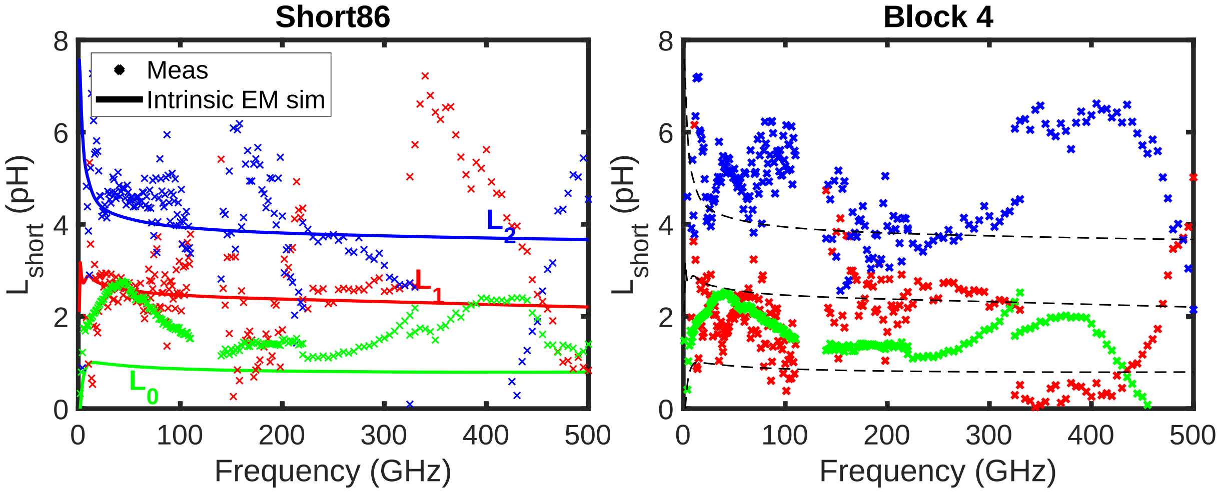
Analysis of measurement discontinuity

As previously observed , the comparison of the small signal model which is our reference to the EM co-simulation shows a difference in both f_T and f_{MAX}, which indicates that the applied TRL calibration and de-embedding procedure is not able to correct completely the measurement of the DUT from its environment. This is observed for both blocks (see Fig. 3.45). Furthermore, the measured f_T extracted from both blocks is 330 GHz and is very similar suggesting that the impact of the GND plane is not a first order effect.However, in the f_{MAX} plot (Fig. 3.45b) as well, it is seen that both blocks give similar results up to 50 GHz. Nevertheless, we see a significant discontinuity at 70 GHz (it is the frequency point where the Line used for TRL calibration is changed from Line_110G to Line_300G) on the curves obtained from Block1 (barely visible in simulation, more pronounced in measurements). This effect in Block1 can be explained by visualizing the E-field distributions in the LINES in each block. It is to be pointed out here that the E-field coupling between the probes is chiefly due to two contributions, the first one through the air above the structure and the second through the substrate below the ground plane. However, the second contribution is much higher owing to the higher permittivity of the substrate. Thus the $\epsilon_{r,eff}$ is the result of these two contributing factors. This probe-to-probe coupling effect is not corrected in the TRL algorithm.

The complex magnitude of electric fields in the different structures at 70 GHz is presented in Fig. 3.46. Figures 3.46 a-c represent the E-fields in the LINES in Block 1, and figures 3.46 d-f represent the same in Block 4. Comparing these, it can be seen that the E-field patterns are not

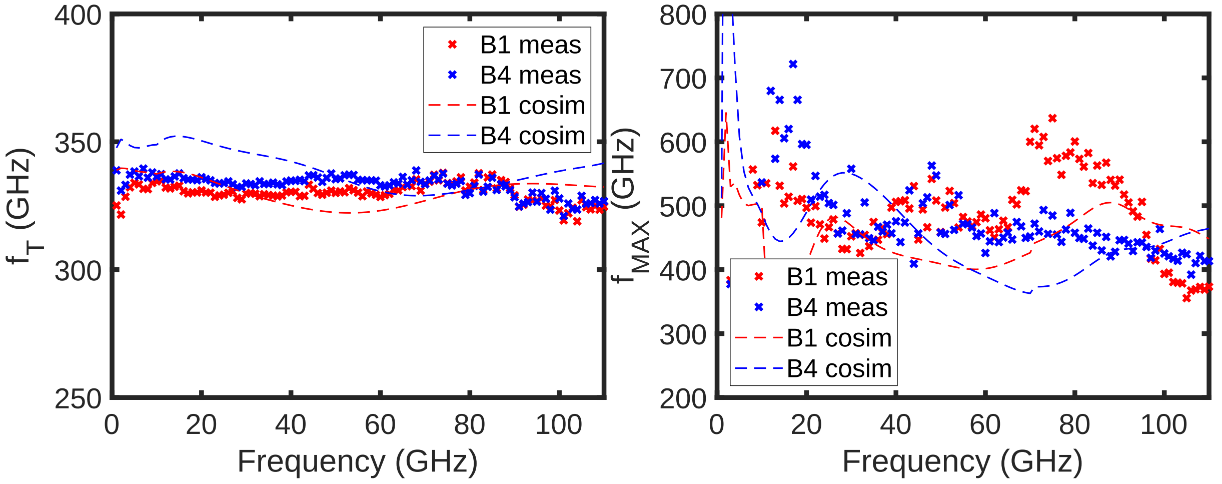


(a) B1: Transistor Open (b) B4: Transistor Open



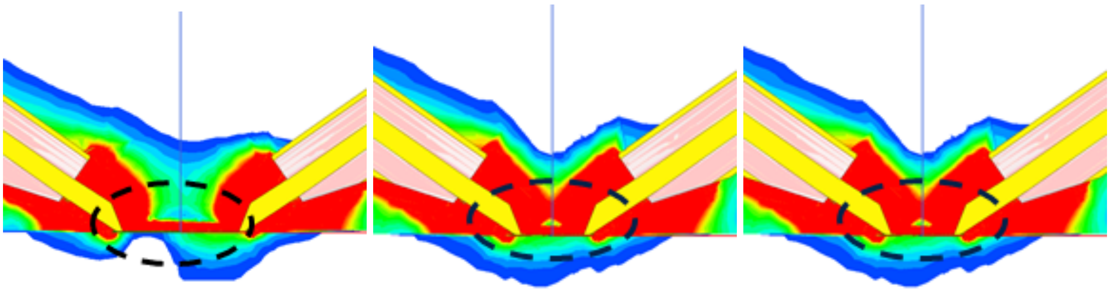
(c) B1: Transistor Short (d) B4: Transistor Short

Figure 3.44: Comparison of parasitics of Open & Short measured on B1 and B4

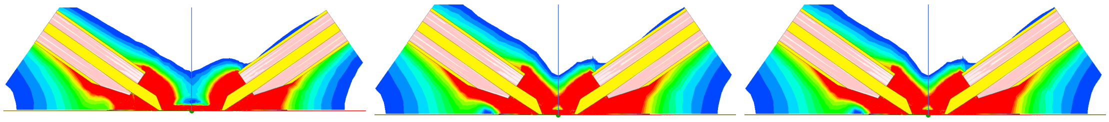


(a) f_T (b) f_{MAX}

Figure 3.45: RF FoMs of transistor from Blocks 1 and 4



(a) B1:Line_110G (b) B1:Line_300G (c) B1:Line_500G



(d) B4:Line_110G (e) B4:Line_310G (f) B4:Line_500G

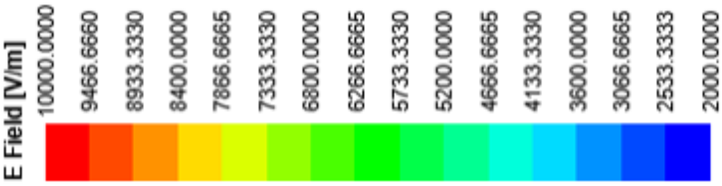
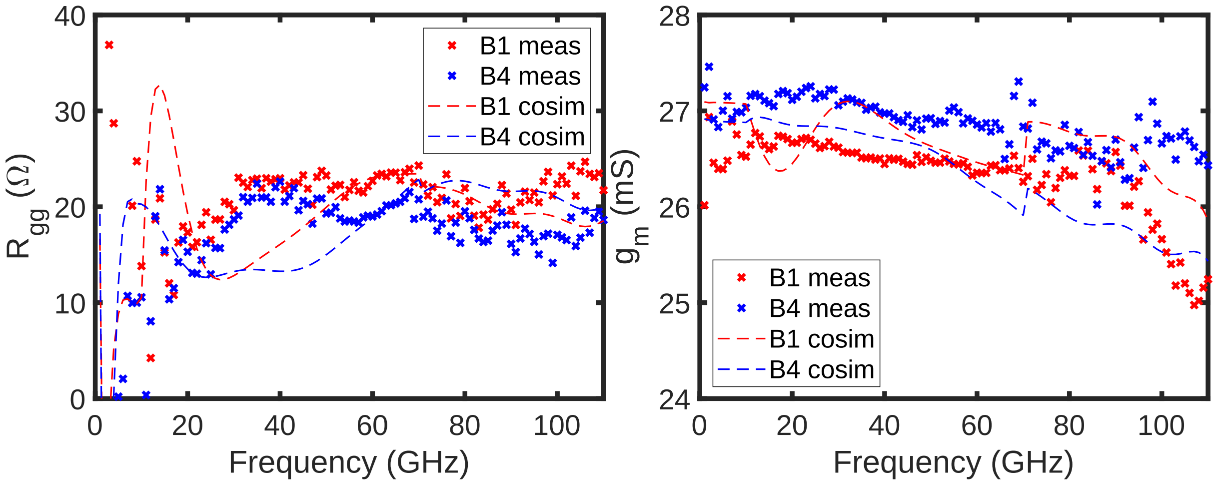


Figure 3.46: EM field distribution in the lines at 70 GHz for Block 1 (a to c, without continuous ground plane) and Block 4 (d to f, with continuous ground plane)

identical. The probe-to-probe coupling (represented by the E-field) between Port1 and Port2 is strongest for the shortest Line (Line_500G). Moreover, on comparing the similar Lines of B1 and B4, we can see that there is a significant penetration of the E-field into the substrate in B1 only.

As a result of this E-field difference between Line_110G and Line_300G, there exists a small difference in the line phase constant (β) extracted during the TRL algorithm before and after 70 GHz, thereby resulting in the discontinuity at this frequency point as plotted in Fig. 3.48 for Block1. This figure also points to the fact that there exists a difference in the effective dielectric constant ($\epsilon_{r,eff}$) before and after 70 GHz and it increases at 70 GHz.The absence of field penetration below the ground plane of the test structures and into the substrate when we have a continuous ground plane as in Block 4 means that the coupling between probes in Block1 is higher than in Block4, resulting in a relatively larger percentage of error in Block1 at 70 GHz,due to the higher $\epsilon_{r,eff}$. For a comparable probe geometry, this effect is expected to be more pronounced at higher frequencies (above 110 GHz). This discontinuity can be visualized through other transistor parameters as well, for example, the gate resistance (R_{gg}) and transconductance (g_m) as shown in Fig. 3.47. However, in the measured curves of these parameters, the level of discontinuity is comparable to the noise variation level which makes it difficult to distinguish between the noise and the discontinuity. Nevertheless, this effect is clearly apparent in the curves from EM simulation.

The on-wafer TRL calibration has also been repeated on Block1 by replacing the HF line standard, Line_300G by the Line_500G which is much shorter, in order to be able to perform calibration for a larger range of frequencies (up to 500 GHz). However, this replacement causes the discontinuity at 70 GHz to increase in magnitude (refer Fig. 3.50) because there is now a significantly larger difference between the E-field distributions in the Line_110G and Line_500G than in the previous case (Fig. 3.46a-c). This change in E-field also causes the $\epsilon_{r,eff}$ of Line_500G to be slightly higher than that of Line_300G as seen in Fig. 3.49 due to the increased coupling



(a) R_{gg}

(b) g_m

Figure 3.47: Gate resistance and transconductance of transistor from Blocks 1 and 4

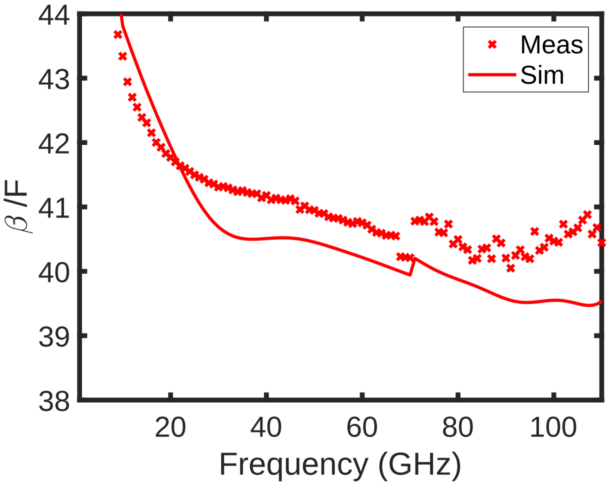


Figure 3.48: Normalized Beta extracted from on-wafer TRL calibration on Block1 (measurement and co-simulation

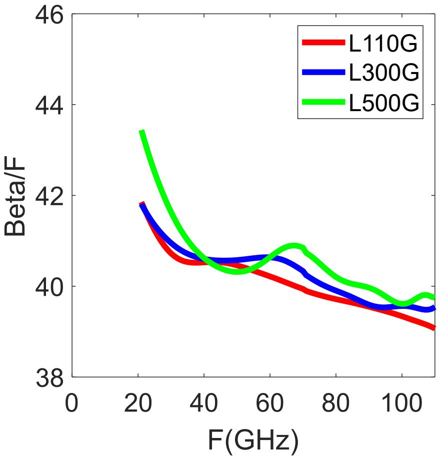
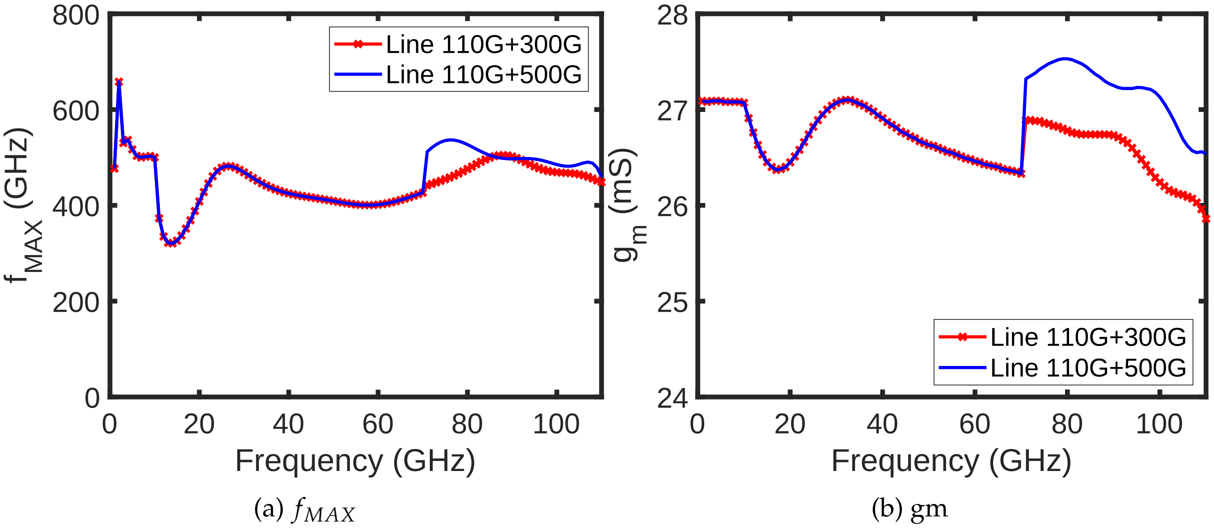


Figure 3.49: Normalized Beta of each LINE in Block1 after on-wafer TRL calibration (co-simulation)



(a) f_{MAX}

(b) gm

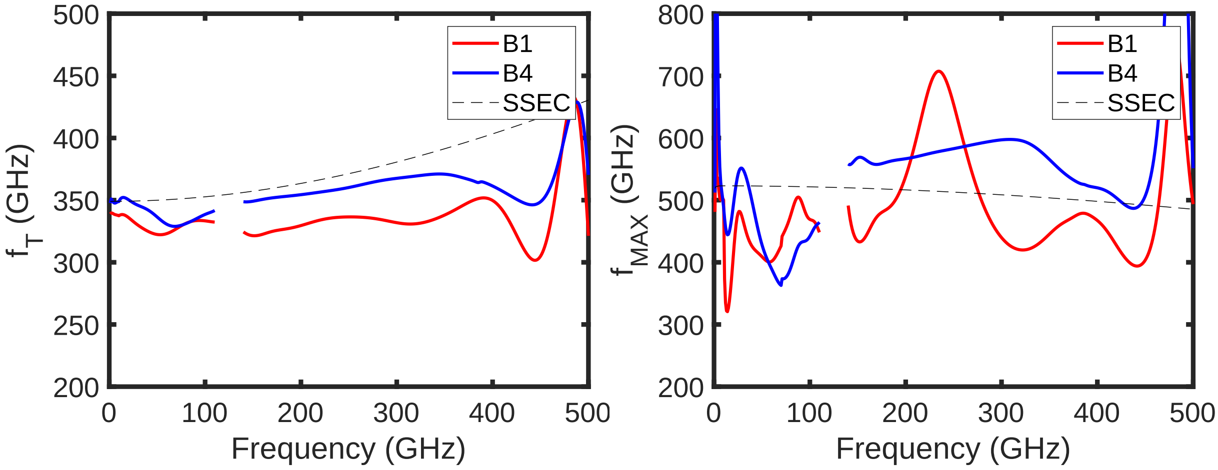
Figure 3.50: f_{MAX} and g_m of transistor extracted from TRL calibration (EM simulation) using different lines after 70 GHz in Block1

between probes (only simulation results are presented for better visualisation). As a result, the magnitude of error in computing the line propagation constant during TRL is now larger beyond 70 GHz. Therefore, although a shorter a line standard provides the advantage of being able to calibrate the device for a larger bandwidth, it brings in a considerable error in the results in the form of the discontinuity. In other words, it is advisable to use lines with similar field distribution (or line lengths just matching the required frequency range for calibration) when multiple lines are to be used for TRL calibration. This study clearly highlights that the probe-to-probe coupling has a non-negligible influence for this given layout and set of probes when using a TRL calibration.

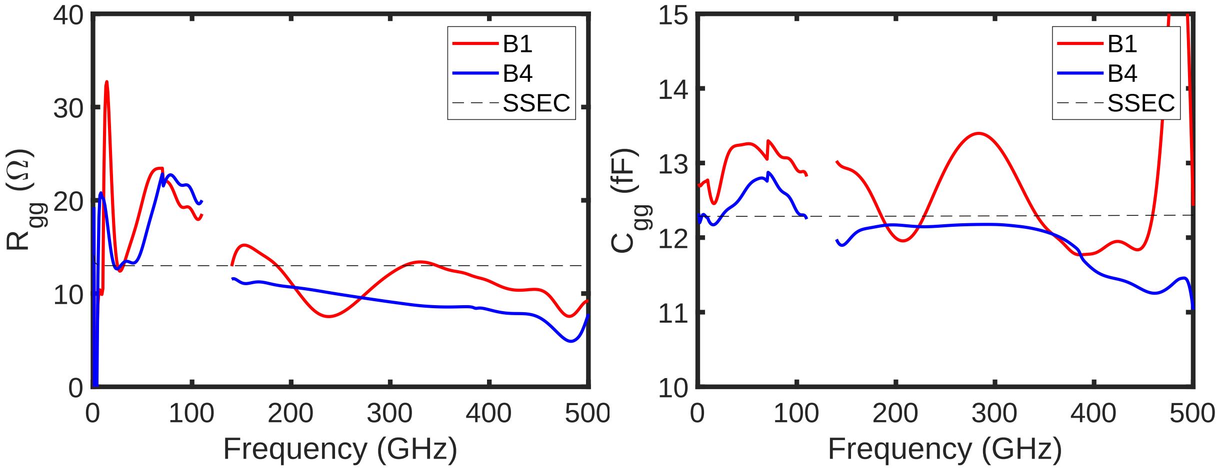
Comparison up to 500 GHz using EM simulation

The measurements and simulations on B4 have been performed up to 500 GHz. In this section, analysis of the B4 calibration results at frequencies above 110 GHz is made by comparing the results with those from the reference block B1. Plots comparing the TRL calibrated parameters extracted using B4 and those from B1 are presented in Fig. 3.51. Only the plots from EM simulation are considered here for ease of analysis. The results of TRL calibration (simulated) above 140 GHz show an impressive accuracy when using Block 4. The extracted parameters of Block 4 show less variation with respect to the expected value as a result of the significantly lower coupling than in Block 1. In fact the improvement in accuracy with B4 is more evident at higher frequencies after 140 GHz than in the first frequency band.

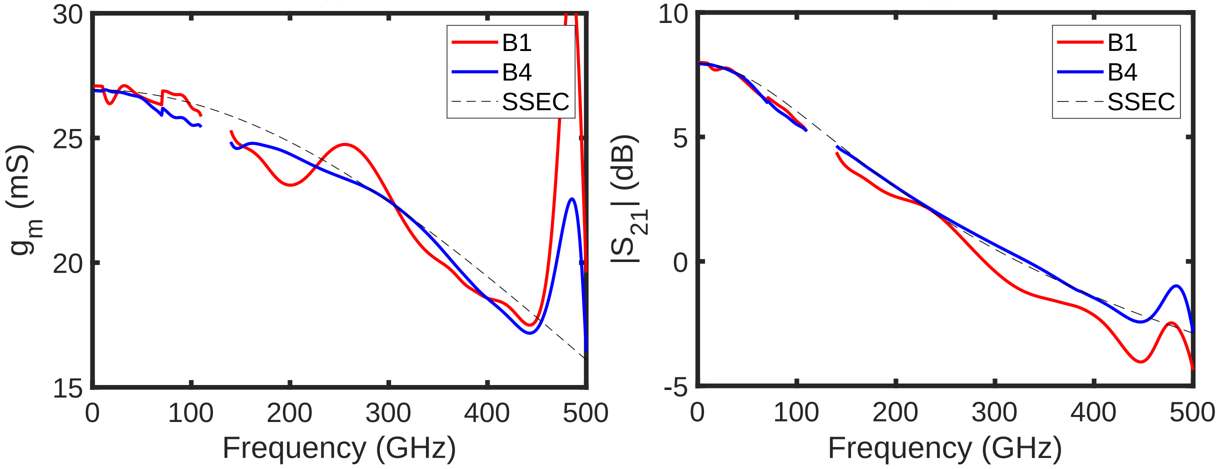
This better performance of B4 is correlated to the reduction in coupling between probes due to the continuous ground plane. As frequency increases, the crosstalk between probes through air reduces due to scaling of the probes, but the coupling through the silicon substrate increases as there is more penetration of the electromagnetic field into the silicon below the test structure in Block 1. This is clearly visible in Fig. 3.52a, where the E field reaches down until the end of the substrate. This leads to a deterioration of the calibration results at higher frequency. The reduction in probe-to-probe coupling through air at higher frequencies is evident on comparing Fig. 3.52a at 300 GHz with 3.28b at 70 GHz. However, with a continuous ground plane in Block 4, the electric field is prevented from entering the substrate (see Fig. 3.52b), resulting in a



(a) f_T (b) f_{MAX}

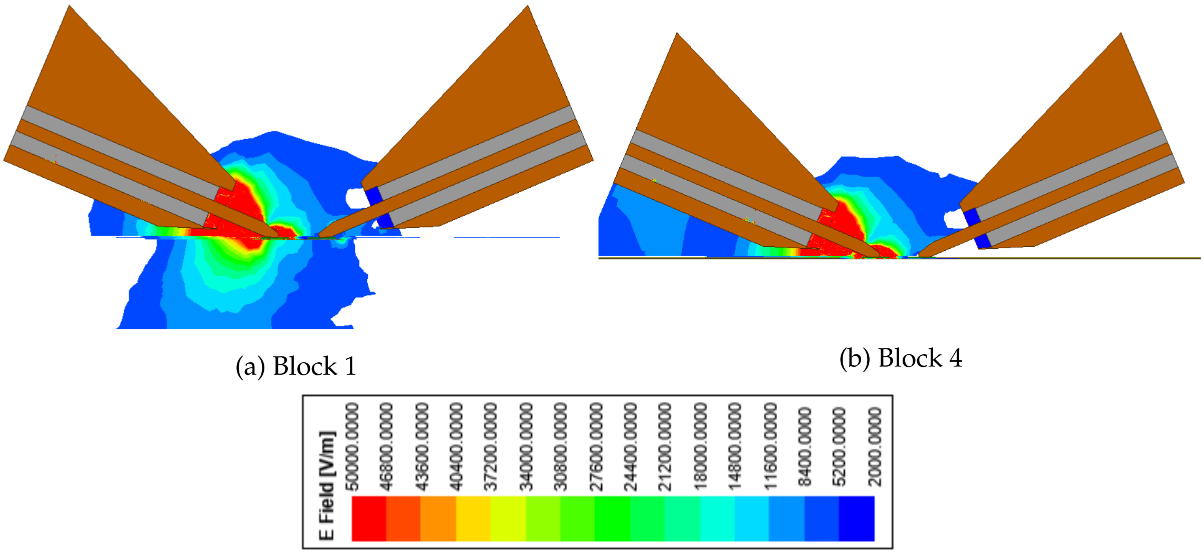


(c) R_{gg} (d) C_{gg}



(e) g_m (f) $|S_{21}|$ (dB)

Figure 3.51: Comparison of transistor parameters from Block 1 (no continuous ground) and Block 4 (with continuous ground plane)



(a) Block 1

(b) Block 4

Figure 3.52: Electric field distribution in Pad Open at 300 GHz

considerable reduction in the coupling as compared to B1. This leads to the smoother curves from calibration with Block 4 leading to a better accuracy than Block 1.

3.5.4 Inferences from the comparison

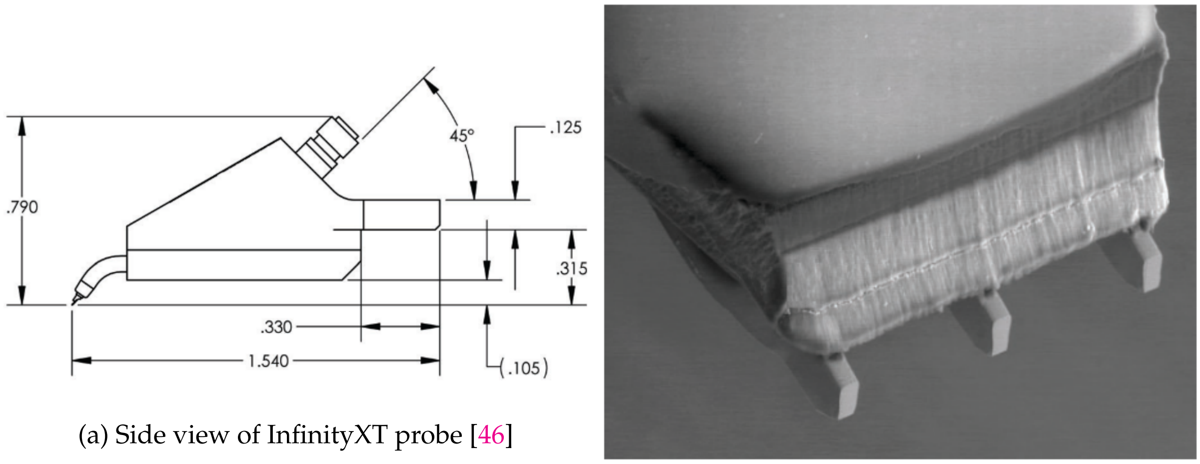
In the preceding section, different parameters of an on-wafer TRL calibration kit have been examined using four different calibration kits for on-wafer TRL. We have analysed the effect of the resistivity of the ground plane in section 3.5.1, and the accuracy of the impedance correction procedure in section 3.5.2. The study of both these parameters showed negligible effect on the transistor parameters extracted after calibration and de-embedding.

In section 3.5.3, the issue of the coupling of electric field from the RF probe to the substrate has been addressed. The Block 4 with the continuous ground plane and pad shield brings in some improvement in the calibration accuracy. But the room for improvement using this technique is rather small since the coupling occurs at a much larger scale than the device dimensions. The commercially available RF probes are quite large (3 to 4 times large) compared to the size of the test structures.

Thus an ideal solution to the problem of probe-to-probe coupling during on-wafer TRL calibration would be to identify the RF probe geometry that can minimize this coupling as much as possible.

3.6 Effect of probe geometry

As observed all along the document the geometry of the probe is a key element to obtain reliable results on advanced high frequency and miniaturized transistors. Within the last period of the thesis, we had the opportunity to test new probes named InfinityXT having a very different probe geometry. Indeed, as observed within the Fig. 3.53, the way of manufacturing the probe is very different compared to the conventional Infinity probe. Firstly, the topology (see Fig. 3.53b) shows that the EM field will be confined and will concentrate mainly in the upper



(a) Side view of InfinityXT probe [46]

(b) SEM image of InfinityXT probe [46]

Figure 3.53: InfinityXT RF Probe

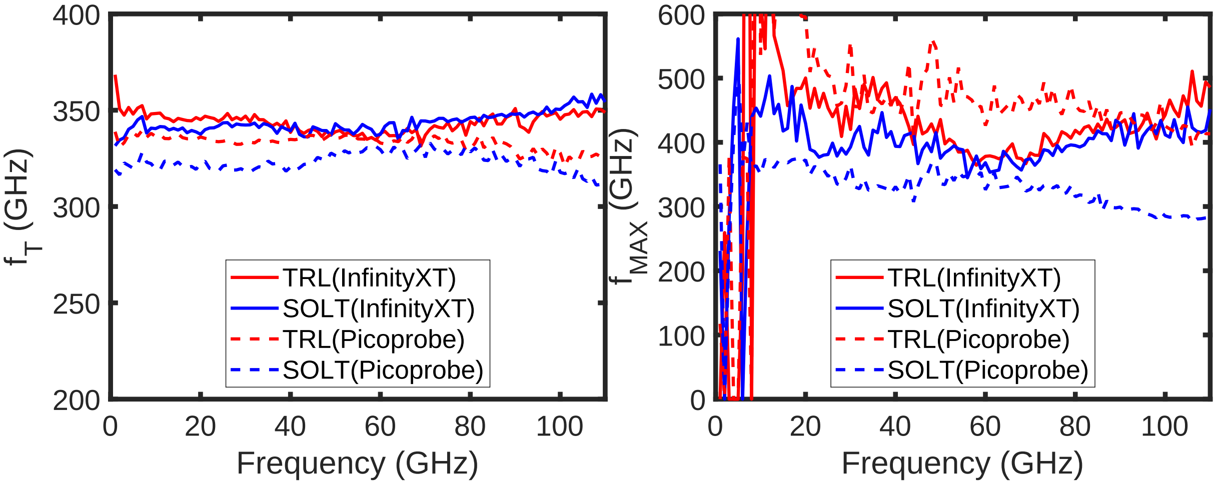
part of the probe since the field tends to concentrate within the higher ϵ region leading to a reduced probe to substrate coupling. Moreover, the interface between the coaxial part and the microstrip line is more far from the tips as compared to the conventional RF probes. This is one of the major drawback of the conventional probe as observed in [99]. Moreover, it needs to be mentioned here that the conventional Infinity probe utilised in this work make use of the UT047 microax . Please note that an Infinity with a UT034 microcoax cable is also available and shows better results especially for transistor characterisation since the EM field is more confined at the transition between this microcoax and the microstrip line.

Also, the pitch chosen for this probe is 50 µm while it was 100 µm for the conventional Infinity used in this work below 110 GHz. For this specific pitch, it is observed in the datasheet [46] that the probe to probe coupling is strongly reduced with less than 50 dB at 200 µm of distance in the air.

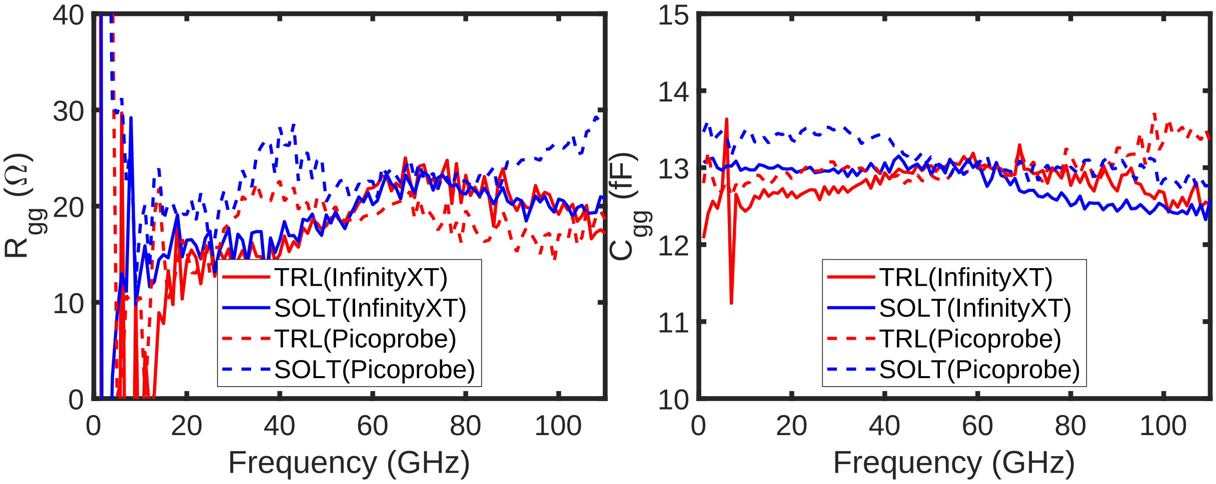
Hence, we performed raw measurement of our test structures using the conventional Infinity probe (pitch 100 µm cable UT047) and with the Infinity XT probe with 50 µm pitch and also measurements on the SOLT calibration standards ISS 138-356. We then apply two different calibrations techniques ISS SOLT and on-wafer TRL. The plots of the transistor parameters obtained after calibration (TRL & SOLT) and de-embeedding are presented in Fig. 3.54. The InfinityXT plots are represented using solid lines and the plots from measurements using the conventional probes are also plotted in this figure using dashed lines.

An anomalous result observed from the previous measurements on the Run1 and Run2 is the significant difference (of 100 GHz) in the value of f_{MAX} extracted from TRL and SOLT calibrations. However, it can be seen from the Fig. 3.54b that the value of f_{MAX} from the two calibration methods are surprisingly closer, and very similar as the frequency increases. Similarly the values of R_{gg} are also very similar with both calibration methods when measured using this InfinityXT RF probes as in Fig. 3.54c.

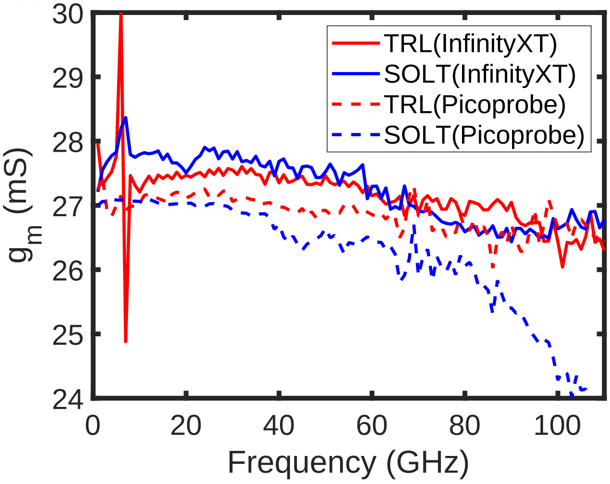
Also presented in Fig. 3.55 and Fig. 3.56 are the S-parameters and Y parameters of the transistor extracted from measurements using InfinityXT probes. In the S-parameter plots, notable difference is seen in the values from SOLT calibration from measurements using InfinityXT and the conventional probes.



(a) f_T (b) f_{MAX}

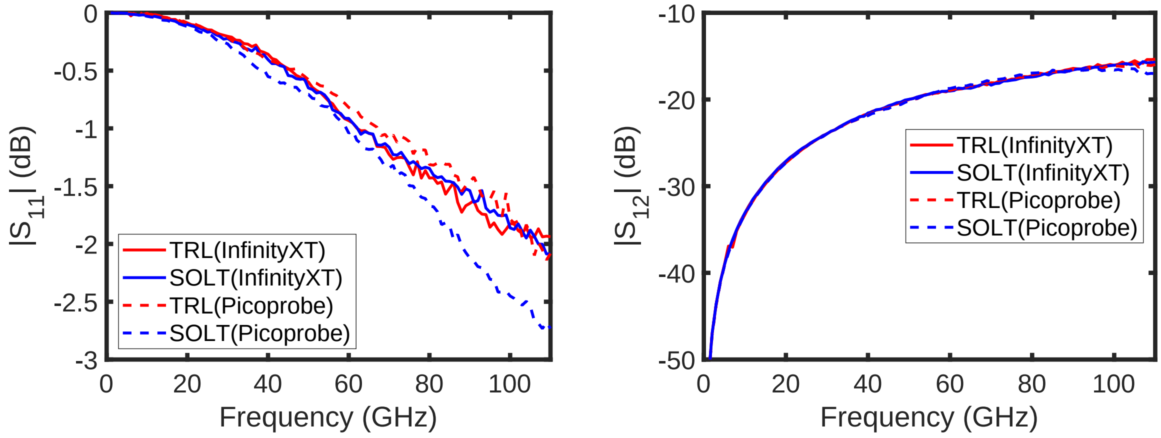


(c) R_{gg} (d) C_{gg}

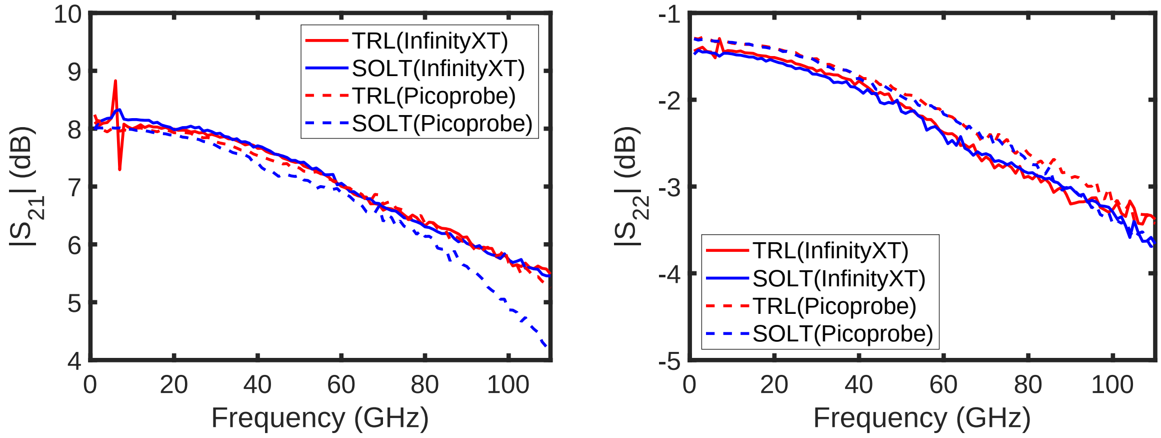


(e) g_m

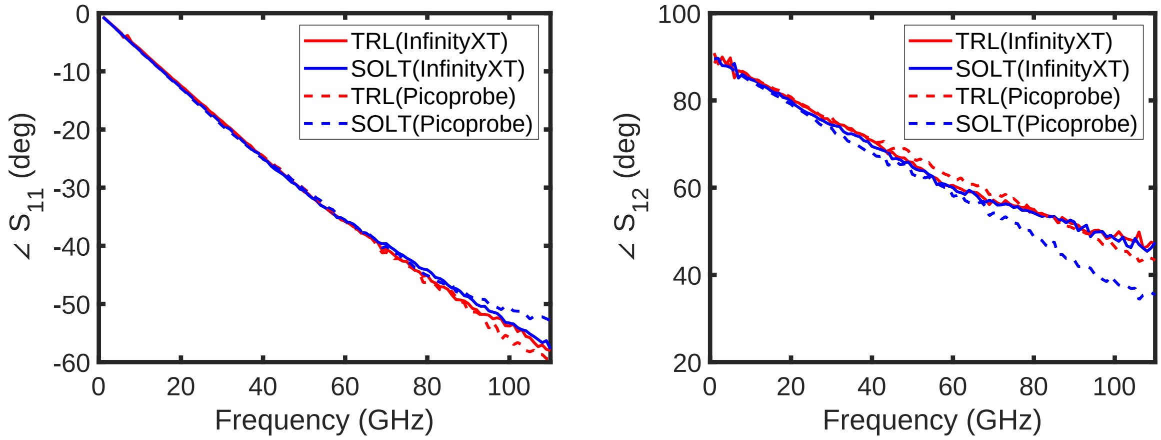
Figure 3.54: Transistor parameters extracted from measurements using InfinityXT RF probes



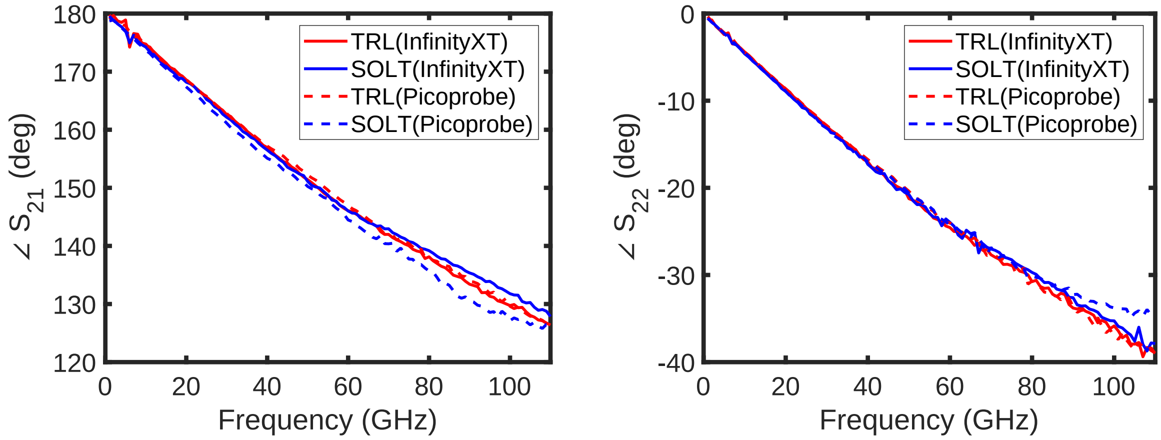
(a) $|S_{11}|$ (dB) (b) $|S_{12}|$ (dB)



(c) $|S_{21}|$ (dB) (d) $|S_{22}|$ (dB)

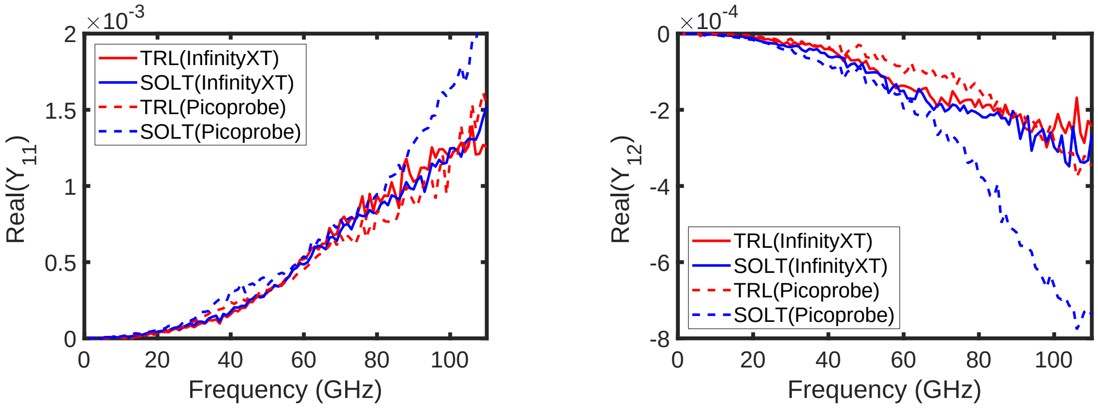


(e) $\angle S_{11}$ (deg) (f) $\angle S_{12}$ (deg)



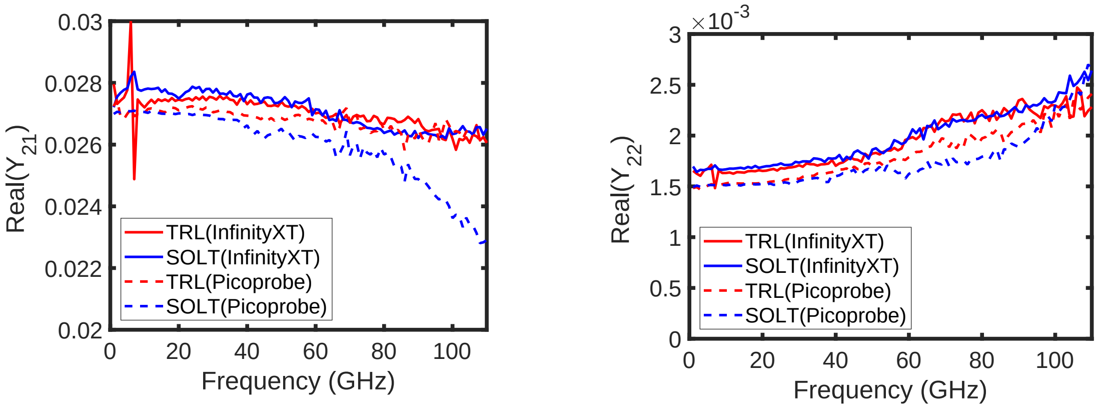
(g) $\angle S_{21}$ (deg) (h) $\angle S_{22}$ (deg)

Figure 3.55: S-parameters of transistor measured using InfinityXT RF probes



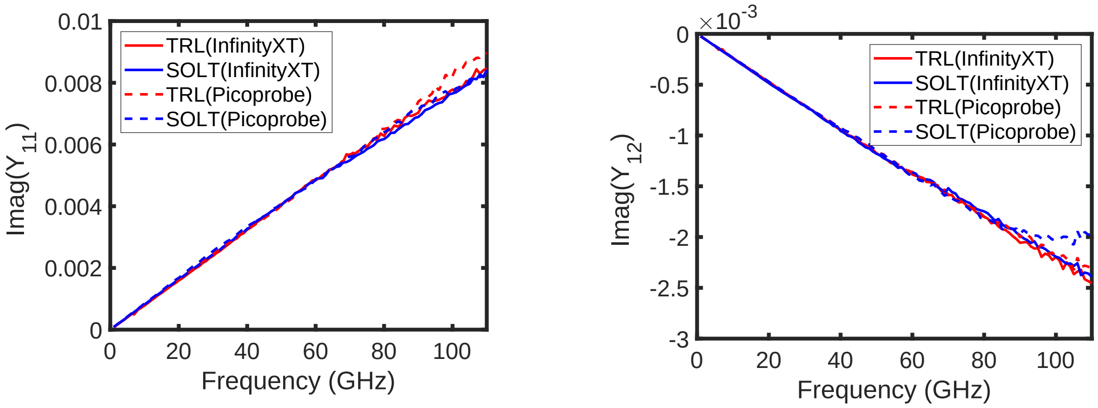
(a) Real(Y_{11})

(b) Real(Y_{12})



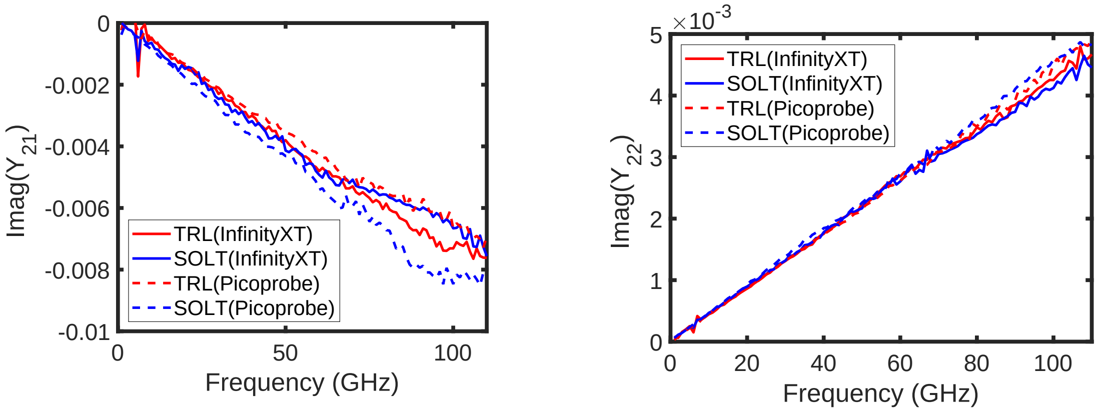
(c) Real(Y_{21})

(d) Real(Y_{22})



(e) Imag(Y_{11})

(f) Imag(Y_{12})



(g) Imag(Y_{21})

(h) Imag(Y_{22})

Figure 3.56: Y parameters of transistor extracted from measurements using InfinityXT RF probes

As observed along the manuscript when using the Infinity probe or even the Picoprobe probe, the f_{MAX} measurement using SOLT and TRL does not converge to the same value as it would be expected when the measurement is reliable. On the other hand using the Infinity XT the measurements using SOLT and TRL converges towards a unique value meaning that the measurement is more robust.

3.7 Conclusion

In this chapter, the improved TRL test structures that tries to overcome the shortcomings of the Run1 test structures have been presented. The intrinsic behavior of the test structures designed for TRL calibration have been investigated using EM simulations. The new designs are compared with the previous ones and it has been found that the new lines have better impedance matching, less loss, and are less affected by the presence of dummies. The absence of automatic tiling in the lines has several positive consequences, such as having the exact same propagation constants for all the line standards, which is desirable for accurate TRL calibration. Additionally, the losses in the transmission lines have been studied and found that the reduction in loss in the new lines is due to the use of the 10ML stack and the absence of tiles very close to the lines. Overall, the results have shown that the new test structures are an improvement over the previous designs and can provide more accurate TRL calibration.

Next, the measurement results obtained from the four blocks have been discussed in the frequency range of 1 to 500 GHz for Blocks 1 and 4 and up to 330 GHz for Blocks 2 and 3. The same setup and RF probes were employed as used in Run 1, and the transistor measured was SGL86, the same as in Run 1. The new reflect standards OpenLB/ShortLB and Line_1800G TRL Line standard above 300 GHz were used in the measurements. The Transistor Open and Transistor Short structures corresponding to the transistor SGL86 were characterised to extract the values of their lumped parasitics. The small signal equivalent circuit has also been extracted, and the values thus obtained compared to those of Run 1. A negligble difference has been observed between the two models.

Finally, the performance of the different calibration kits for TRL (Thru, Reflect, and Line) calibration have been discussed, focusing on the significance of the ground plane design and the effect of line characteristic impedance on the measurement accuracy of the RF FoMs (Figure of Merits) of the transistor. The design of the ground plane and its effect on the measurement accuracy of the RF FoMs of the transistor have been investigated. Also emphasized is the need for impedance correction to the 50 Ω reference.

Lastly, the importance of probe geometry in obtaining accurate measurements of high-frequency and miniaturized transistors have been investigated. Measurements have been repeated using a new type of probe called InfinityXT, which has a different probe geometry compared to the conventional Infinity probe.The InfinityXT probe is designed to confine the EM field and concentrate it mainly in the upper part of the probe, which reduces the probe to substrate coupling. Additionally, the interface between the coaxial part and the microstrip line is further away from the tips compared to the conventional RF probes. Raw measurements on the test structures have been made using both the conventional Infinity probe and the InfinityXT probe and two different calibration techniques (ISS SOLT and on-wafer TRL) applied to extract the transistor parameters. It has been observed from the results that the InfinityXT probes provide more robust measurements as compared to the conventional probes. For example, the f_{MAX} measurement using SOLT and TRL converges to a unique value when using the InfinityXT probe, indicating that the measurement was more reliable.

General Conclusion & Perspectives

Millimetre waves find tremendous applications in the present-day world, owing to its remarkable advantages such as high data rates, large available bandwidth and smaller device sizes, leading to a profound interest in the ongoing research in millimetre wave devices and technologies. Major application domains of these devices are in high-speed communication systems such as 5G/6G, high resolution imaging for radars or medical application, Internet of Things (IoT) and so on.

This works has attempted to establish a reliable characterisation methodology for millimetre wave devices specifically the 28 nm FD-SOI MOS transistors from STMicroelectronics, and identify the constraints that limit the accuracy of high frequency calibration. The frequency range of interest is from 1 GHz to 500 GHz. The work done has been presented in 3 chapters.

The Fully Depleted Silicon-On-Insulator (FD-SOI) MOS transistors with maximum reported values of f_T/f_{MAX} above 300 GHz are found to be good candidates for sub-THz circuit applications due to its several advantages such as the deep sub-micron lithography, low parasitic capacitances, low power consumption to name a few. Having established the need for accurate and reliable characterisation methods above 100 GHz, the different RF measurement setups used for characterisation from 1 to 500 GHz have been detailed, along with the different on-wafer and off-wafer calibration techniques employed during this thesis. A theoretical comparison has been made between the two calibration methods off-wafer SOLT and on-wafer TRL to identify the pros and cons of each method. On-wafer TRL calibration has several advantages over the conventional off-wafer SOLT calibration, particularly at high frequencies, although TRL is unable to correct the errors introduced due to crosstalk between probes. Thus, in Chapter 1, the measured devices, the measurement and simulation environment and the workflow related to calibration and de-embedding have been discussed.

In Chapter 2, the existing test structures (labelled Run1) for on-wafer TRL have been analysed using measurements and electromagnetic simulations. The intrinsic behaviour of the TRL test structures and de-embedding structures have been discussed with the aid of intrinsic EM simulations. However, the actual behaviour of the Line standards as observed from measurements has been seen to deviate significantly from the expected intrinsic behaviour. This effect has been found to be due to the automatic tiling during the wafer fabrication process that introduced metallic tile structures very close to and below the microstrip lines. This presence of tiles has resulted in several drawbacks with the Run1 test structures. Most importantly the frequency range of the TRL calibration kit has been reduced due to the tiling. Moreover, since this tiling has been found only in the two Line standards and not the other TRL standards or DUTs, the effective dielectric constant $\epsilon_{r,eff}$ changes between the Lines and the other test structures/DUTs. This change has been identified as a source of error during TRL calibration as the algorithm assumes the same environment for all the TRL standards and DUTs. The presence of tiles have also been found to increase the attenuation of the Lines, which may affect the measurement accuracy of the high frequency FoMs of the transistor.

Nonetheless, a small signal model has been extracted for the characterised FD-SOI transistor and it has been found to provide a reasonable fit with the measurements upto 350 GHz. An EM co-simulation that combines the simulation of the small signal model with the EM simulation of the passive structures has been employed to validate the methodology used for TRL calibration. Comparison made between the measurements using on-wafer TRL and off-wafer SOLT has highlighted the benefits of TRL calibration over the off-wafer calibration method. However, the f_{MAX} extracted using the two calibration methods showed a difference of nearly 100 GHz, leading to an ambiguity in the real f_{MAX} of the transistor. Moreover, the issue of the coupling between the RF probes remained a source of error that could not be resolved by TRL calibration.

In view of these issues faced with the Run1 test structures, improved TRL calibration kits (labelled Run2) have been designed using the 10ML BEOL of the FD-SOI technology. The performance of the Run2 test structures has been discussed in Chapter 3. Four different types of calibration kits have been analysed to study the effect of different parameters involved in the process of on-wafer TRL calibration. The first of these calibration kits (B1) has been taken as the reference to study the effects. The use of 10ML BEOL has enabled the design of 50 Ω lines with wider microstrip line width, thereby reducing the line losses. The Run2 calibration kits have been designed with more number of Line standards to ensure that reliable TRL calibration can be performed in the entire frequency range of interest, as well as additional reflect standards that shift the reference plane more closer to the actual DUT. The on-wafer measurements on B1 have been used to extract the small signal model of the transistor characterised, which has in turn been used in the EM co-simulation of the new test structures. The measurements on B1 of Run2 have shown a small improvement in the results as compared to Run1, particularly in terms of extending the valid frequency range upto 400 GHz. However, the difference in the value of f_{MAX} of the transistor still remained, when characterised using SOLT and TRL calibration methods. The Blocks 2 and 3 (B2, B3) of Run2 have been designed to study the effect of ground plane design and the effect of non-50 Ω characteristic impedance for the Lines respectively. It has been concluded that these parameters have negligible effect on the final calibration results.

However, remarkable improvement has been observed with the Block 4 (B4) of Run2, which has been designed with a continuous ground plane and RF pad shields around the RF pads. The improvements are a result of the reduction in the electromagnetic field coupling between the RF probes during measurement, which have been made possible by the continuous ground plane that block the penetration of electric field into the substrate below the ground plane. The better results of B4 are manifested in two ways. Firstly, the discontinuity between measurement bands and the discontinuity on changing the Line standard have been greatly minimised. Secondly, the measurement results have been observed to be more stable with respect to frequency (less noise fluctuations) and reliable upto 450 GHz. For simplicity, the second fact has been deduced from the EM co-simulations on B4 as simulations do not consider the effects of external factors on the on-wafer TRL calibration such as inaccurate probe positioning or temperature drift. Thus it has been concluded that the main constraint in obtaining accurate results until 500 GHz with TRL calibration is the error introduced due to crosstalk between probes.

Lastly, the effect of probe geometry on on-wafer TRL has been assessed by repeating the measurements on B4 with the newly available InfintyXT probes that have significantly less crosstalk as compared to the conventional Infinity or Picoprobe probes. The value of f_{MAX} from TRL and SOLT calibrations have been found to converge to a similar value when using the InfinityXT probes for measurement. This result again reiterates the fact that crosstalk between probes is the major reason for inaccuracies in on-wafer TRL calibration. Thus a practical solution to this dilemma is to either develop test structures that can greatly reduce the coupling to a negligible value, or to identify or develop RF probe geometries that have very low crosstalk, or to use a more advanced calibration method such as the 16-terms.

The TRL and SOLT calibration procedures employed in this work are subsystems of the general full 16-term error model. The 16-term error model contains all possible errors that could occur and it can be applied to any measurement setup, test-fixtures or probes. So, exploring the 16-term error model is certainly a promising route for improving the calibration. The road blockers that may appear are as follows: (i) on-wafer crosstalk has to be constant for all the calibration structures, (ii) the calibration standards have to be known apriori like in a SOLT which is challenging for on-wafer calibration (iii) numerical stability in solving and inverting a 16x16 matrix needs to be assured (iv) measurement noise reduction techniques are indispensable. But once these road blockers are removed, a highway for mm-wave measurements is opened.

The research team at IMS has started working on a new project PRECISE, for "New miniature high frequency probes for precision on-wafer microwave measurements", in collaboration with the research groups at IEMN Lille, RF-IC lab Grenoble and the company MC2. The high frequency on-wafer characterization techniques use patented probe technologies in the 2000s that have evolved so little, and these commercial mmW probes have a strong coupling towards the substrate or towards the neighborhood, thus altering the measurement accuracy beyond 50 GHz. In this project, it is proposed to design miniaturized probes and manufacture them using MEMS-type silicon technology to better confine the electromagnetic field. In addition, this probe will be broadband type (DC-220/325 GHz) to adapt to new generations of network analyzer and will be more suitable for precise characterization of mmW or THz application.

Author Publication List

International conferences

1. K. Pradeep, M. Deng, B. Dormieu, P. Scheer, M. De Matos, T. Zimmer, and S. Fregonese, “Influence of calibration methods and RF probes on the RF characterization of 28FD-SOI MOSFET”, in 2021 IEEE Latin America Electron Devices Conference (LAEDC), IEEE, 2021, pp. 1–4.
2. K. Pradeep, S. Fregonese, M. Deng, B. Dormieu, P. Scheer, and T. Zimmer, “Study on measurement discontinuity during on-wafer TRL calibration of 28FD-SOI devices upto 110GHz”, in 100th ARFTG Microwave Measurement Conference, IEEE, 2023.

Workshop

1. Karthi Pradeep, "Contribution to on-wafer characterization and compact modeling of 28nm FD-SOI MOS transistors in millimeter-wave frequency range", Workshop Laboratoire Commun ST/IMS, December 8, 2022, Crolles, France
2. Karthi Pradeep, "Contribution to on-wafer characterization and compact modeling of 28nm FD-SOI MOS transistors in millimeter-wave frequency range", Workshop Laboratoire Commun ST/IMS, November 2020, Online.

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Contribution à la caractérisation sur wafer de transistors MOS FD-SOI en bande millimétrique

Résumé : Les technologies CMOS sur silicium présentent des aptitudes reconnues pour les applications millimétriques. Parmi elles, les technologies (FD-SOI) développées à partir du nœud 28nm offrent des caractéristiques prometteuses pour un vaste champ d'applications, avec notamment des, f_T, et f_{MAX}, au-delà de 300 GHz. Pour permettre la conception de ces circuits, une modélisation précise des transistors FD-SOI est absolument nécessaire. De plus, il n'est plus possible de limiter l'extraction des paramètres en dessous de 110 GHz, et de nouvelles techniques permettant d'obtenir des mesures fiables de dispositifs passifs et actifs doivent être étudiées. Dans cette thèse, nous examinerons la caractérisation des paramètres S sur silicium (on-wafer) de différentes structures de test passives et des transistors MOS en technologie 28nm FD SOI de STMicroelectronics, jusqu'à 500 GHz. En commençant par une introduction de l'équipement de mesure habituellement utilisé pour ce type d'analyse, nous passons aux différents bancs de mesure adoptés au laboratoire IMS, et enfin nous nous concentrerons sur les techniques de calibrage et d'épluchage (de-embedding). Deux puces différentes ont été étudiées. L'analyse repose sur des simulations électromagnétiques et des simulations EM mixtes de modèle petit signal + sonde, toutes deux incluant les modèles des sondes pour une évaluation des résultats de mesure plus proche des conditions réelles. Enfin, quelques structures de test sont présentées pour évaluer les pertes dans les lignes, la précision de la méthodologie de correction d'impédance et finalement le couplage sonde-sonde et sonde-substrat.

Mots clés : Caractérisation, Lignes de transmission, Terahertz, Ondes millimétriques, Calibrage sur silicium, MOSFET sur FDSOI

Contribution to on-wafer characterization of millimeter-wave FD-SOI MOS transistors

Abstract : Silicon CMOS technologies have been recognized for their abilities in millimeter-wave applications. Among them, the FD-SOI technologies developed from the 28nm node offer promising performances for f_T and f_{MAX} beyond 300 GHz. To enable the design of circuits operating at millimeter-wave frequencies, an accurate modeling of FD-SOI transistors is essential. Furthermore, it is no longer possible to limit parameter extraction below 110 GHz, and new techniques for obtaining reliable measurements of passive and active devices need to be investigated. In this thesis, we will examine the on-wafer S-parameter characterisation of different passive test structures and MOS transistors in 28nm FD SOI technology from STMicroelectronics, up to 500 GHz. Starting with an introduction to the measurement equipment usually used for this type of analysis, we move on to the different measurement benches adopted in the IMS laboratory, and finally focusing on the calibration and de-embedding techniques. Two different chips were studied. Analysis relies on electromagnetic simulations and mixed small signal plus probe model EM simulations, both including the probe models for a closer evaluation of the measurement results under real conditions. Finally, presented are some test structures to evaluate the losses in the lines, the accuracy of the impedance correction methodology and finally the probe-to-probe and probe-to-substrate coupling.

Keywords: Characterization, Transmission Lines, THz, Millimeter-Wave, On-Wafer Calibration, MOSFET on FDSOI

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