Low Frequency Noise in advanced MOSFET technologies : From experimental observations to new extraction and modeling methods

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préparée au sein du **Laboratoire Institut de Microélectronique, Electromagnétisme et Photonique – Laboratoire d'hyperfréquences et de caractérisation** dans l'**École Doctorale Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)**

Bruit basse fréquence dans des dispositifs MOSFET des technologies avancées : Des observations expérimentales aux nouvelles méthodes d'extraction et de modélisation

Thèse soutenue publiquement le **14 avril 2022**,
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To my parents

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Merci à tous!!!

ABBREVIATIONS

Acronym	***Definition***
3DSI	3D Sequential Integration
CLM	Channel Length Modulation
CMF	Correlated Mobility Fluctuations
CMOS	Complementary Metal Oxide Semiconductor
CNF	Carrier Number Fluctuations
DIBL	Drain-Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
FDSOI	Fully Depleted Silicon on Insulator
HTO	High Temperature Oxide
LFN	Low-Frequency Noise
LT	Low Temperature
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NW	Nanowire
PEALD	Plasma Enhanced Atomic Layer Deposition
RTN	Random Telegraph Noise
RO	Ring Oscillator
SCE	Short Channel Effects
PSD	Power Spectral Density
SOI	Silicon on Insulator
S/D	Source/Drain
SPER	Solid Phase Epitaxy Regrowth
SRAM	Static Random-Access Memory
SW	Subthreshold Swing
SS	Subthreshold Swing
TB	Thermal Budget

CONTENTS

LIST OF PUBLICATIONS

International Conferences:

A. Tataridou, G. Ghibaudo, and C. Theodorou, "VERILOR: A Verilog-A Model of Lorentzian Spectra for Simulating Trap-related Noise in CMOS Circuits", 2021, ESSDERC 2021 - IEEE 51st European Solid-State Device Research Conference (ESSDERC), DOI: 10.1109/ESSDERC53440.2021.9631802. ***(Best student paper award)***

A. Tataridou, G. Ghibaudo, and C. Theodorou, ""Pinch to Detect": A Method to Increase the Number of Detectable RTN Traps in Nano-scale MOSFETs", 2021, 2021 IEEE International Reliability Physics Symposium (IRPS), DOI: 10.1109/IRPS46558.2021.9405102.

D. Bosch, J.P. Colinge, J. Lugo, **A. Tataridou**, C. Theodorou, X. Garros, S. Barraud, J. Lacord, B. Sklenard, M. Casse, L. Brunet, P. Batude, C. Fenouillet-Béranger, D. Lattard, J. Cluzel, F. Allain, R. Nait Youcef, J.M. Hartmann, C. Vizioz, G. Audoit, F. Balestra, and F. Andrieu, "Comparative experimental study of junctionless and inversion-mode nanowire transistors for analog applications", 2020, 2020 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), DOI: 10.1109/VLSI-TSA48913.2020.9203690.

C. Cavalcante, X. Garros, P. Batude, **A. Tataridou**, J. Lacord, M. Casse, C. Theodorou, T. Karatsori, R. Gassilloud, C. Fenouillet-Beranger, L. Brunet, O. Rozeau, N. Rambal, F. Gaillard, F. Ponthenier, F. Allain, G. Romano, G. Ghibaudo, J-P. Colinge, M. Vinet, and F. Andrieu, "Low temperature high voltage analog devices in a 3D sequential integration", 2020, 2020 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), DOI: 10.1109/VLSI-TSA48913.2020.9203691.

A. Tataridou, G. Ghibaudo, and C. Theodorou, "Influence of series resistance on the experimental extraction of FinFET noise parameters", 2020, 2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS), DOI: 10.1109/ICMTS48187.2020.9107908.

Scientific Journals:

A. Tataridou, G. Ghibaudo, and C. Theodorou, "A Method for Series-Resistance-Immune Extraction of Low-Frequency Noise Parameters in Nanoscale MOSFETs", 2020, IEEE Transactions on Electron Devices (Vol.: 67, Issue: 11, Nov. 2020), DOI: 10.1109/TED.2020.3026612.

A. Tataridou, G. Ghibaudo, and C. Theodorou,"Model Implementation of Lorentzian Spectra for Circuit Noise Simulations in the Frequency Domain", 2022, IEEE Journal of the Electron Devices Society (J-EDS), DOI: 10.1109/JEDS.2022.3178352.

A. Tataridou, G. Ghibaudo, C. Dimitriadis, and C. Theodorou, “Localization of defective regions in LT SOI MOSFETs using LFN spectroscopy”, (to be submitted).

ABSTRACT

Despite the advancements in the semiconductor device research and development, with the incorporation of new materials and architectures, as well as the downsizing of the geometrical dimensions, which lead to superior device performance and speed, the Low Frequency Noise, LFN, has become a major concern for micro- and nanoscale transistor components, as its impact on both device and circuit level is more important than ever. First of all, it should be noted that, in this dissertation, when referring to LFN we mean the internal type of noise due to trapping/detrapping or/and scattering of free carriers. For 1/f-like spectra, the power spectral density of the flat-band voltage, S_{Vfb}, is inversely proportional to the area, and thus going from micro- to nanoscale devices the LFN level is increased. In addition, with the miniaturization of the transistor area, a different type of noise called random telegraph noise, RTN, appears and becomes the main contribution instead of 1/f, as individual trap behavior becomes visible. On top of that, the introduction of new materials and architectures in the CMOS technology results to the appearance of peculiar noise behavior like the generation-recombination, GR, noise, which show a Lorentzian PSD instead of 1/f-like. As a result, next-generation electronic components will be governed by instabilities arising from their intrinsic noise sources. It is therefore essential to change the methods of characterization and simulation of LFN/RTN to allow the technology improvement. This is why a thorough theoretical and experimental study of all noise sources in emerging components becomes indispensable in this field of research in microelectronics.

In this dissertation, various devices which meet the ITRS specifications under the demand of “More Moore” and “More than Moore” technology roadmaps (i.e. FinFETs, TriGate NW FETs, CoolCube 3DSI FETs), have been characterized in terms of LFN. Through this study, the physical phenomena that induce the intrinsic device noise have been identified, an information useful not only for the device itself, but also for the accurate noise modeling and therefore for the design facilitation of the associated circuits. On top of that, LFN measurements were utilized as a diagnostic tool for the identification of defective zones

giving information on the quality of the fabricated transistors. The latter is essential for the optimization of fabrication steps. In addition, although the theory of LFN, as well as its corresponding models, are well-established and successfully used for years, issues existing in aggressively scaled down devices might on one hand, hinder the reliable extraction of noise parameters and on the other hand, they can be utilized for traps' effects decoupling and identification. Consequently, a revised version of the "carrier number with correlated mobility fluctuations" (CNF/CMF) model has been proposed so as the impact of series resistance on noise parameters to be eliminated, and a new measurement methodology has been introduced, utilizing an inhomogeneous carrier distribution inside the channel that allows for the maximum RTN-inducing trap detection. Finally, since the appearance of Lorentzian spectra is more and more frequent in the advanced FET technologies, LFN frequency domain models need to be revised. This is because the existing frequency domain models are limited to the typical 1/f behavior which, as we demonstrate in this thesis, can compromise the nominal operation of circuits. Hence, we present a method for the implementation of Lorentzian noise spectra through Verilog-A. Once this method is validated, some circuit noise application examples are examined, in order to showcase how non-1/f noise can affect a circuit's performance.

CHAPTER 1
Introduction

1.1. Overview of microelectronics evolution

It is undoubtable that the effort of industries to keep up with Moore's law has brought tremendous changes in the world of electronics. Back in 1965, Gordon Moore predicted that the number of components per chip would increase by a factor of 2 every year, a statement which would reduce significantly not only the area and the production cost of integrated circuits, as a higher number of components would be produced on a single substrate, but also the power consumption [1]. Ten years later, Gordon Moore came to revise his prediction and altered it by doubling the number of components/chip every two years [2]. Indeed, using Complementary Metal-Oxide-Semiconductor, (CMOS), bulk technology thanks to its simplicity, and silicon, (Si), as the basic material, since it has really low cost and it is abundant in the environment, todays' industries manage to place billions of transistors on a single chip [3].

In the 1990s, as the semiconductor industry was expanding worldwide, it became clear that a document which could supply guidance for the next generation of electronics according to the feedback from industries around the world, would help scientists tackle challenges with technology and consequently benefit the future of electronics. For this reason, the International Technology Roadmap for Semiconductors (ITRS) was constructed [4]. Every year, ITRS provides guidelines concerning the specifications of future device characteristics so as to keep pace with Moore's law.

The first methodology towards transistor miniaturization refers to as "traditional" scaling in which the concept is to reduce all the physical dimensions as well as the supply voltage by the same factor "k" and increase the channel doping by the same degree so as the depletion regions to be scaled down accordingly and keep the electric field constant [3], [5]. CMOS Bulk architecture was the ideal solution as it can scale easily to increasingly smaller dimensions, which not only reduce the production cost but also improve the performance combining higher speed with lower power consumption [6]. Although this scaling method served successfully the evolution of electronics for almost 30 years reaching the 100 nm integration, in the early 2000s the Bulk technology scaling saturated [3]. The very thin silicon dioxide layer (SiO_2), around 1.5 nm, gave rise to leakage current and the really scaled down channel length led to the strengthening of short channel effects (SCEs) and hot carrier aging, which degraded transistor's performance [3], [6]. The SCEs are related to the presence of two electric fields, vertically and horizontally, since the impact of drain potential is becoming more significant with the reduction of channel length [7]. In more detail SCEs can be categorized as:

1. "V_t roll-off": Due to the downscaling of the channel length, the size of the depletion regions, formed at the PN junctions of source and drain side, has become comparable to the channel length as shown in Figure 1-1b. Consequently, the gate voltage gradually loses the electrostatic control which affects the threshold voltage, V_t. As one can see in Figure 1-2b, for channel lengths shorter than 1 µm, V_t stops being constant with L_g but instead shows an exponential decrease [7], [8].
2. Channel Length Modulation (CLM): Although this phenomenon is present in both short and long channel devices, its impact is becoming stronger with the downscaling of FETs. In this phenomenon, the effective channel length becomes dependent on V_d and prevents the drain current from saturating above V_d=V_g-V_t [7]–[9].
3. Drain-Induced Barrier Lowering (DIBL): This phenomenon is described in the dashed purple line of Figure 1-1b and it can be observed at high V_d values. The increase of V_d in short lengths leads to the overlapping of the source/drain depletion regions, a phenomenon that reduces the barrier between source and channel. This issue increases the number of carriers injected into the channel from the source side resulting to the increase of drain current at saturation, instead of reaching a constant value. Consequently, DIBL is responsible for further V_t reduction in the saturation region of operation [6]–[8].
4. Series Resistance: As the channel length of the transistor is scaled down, on one hand higher I_{on} current is achieved, but one the other hand the channel resistance comes closer

to the source/drain series resistance value, R_{SD}, which forms a lower limit on further channel length reduction. This phenomenon can be seen in Figure 1-2a, where in short channel lengths the ON current (V_g = 1 V) becomes length independent below L = 100 nm [7], [10].

5. Velocity Saturation: With the increase of electric field, the channel mobility becomes field-dependent and eventually velocity saturation occurs [7].
6. Reliability Issues: Due to the increase of the longitudinal electric field, phenomena that degrade the reliability of the MOSFET occur such as the hot carrier injection and impact ionization. These issues result to instabilities of the device characteristics over time [7].

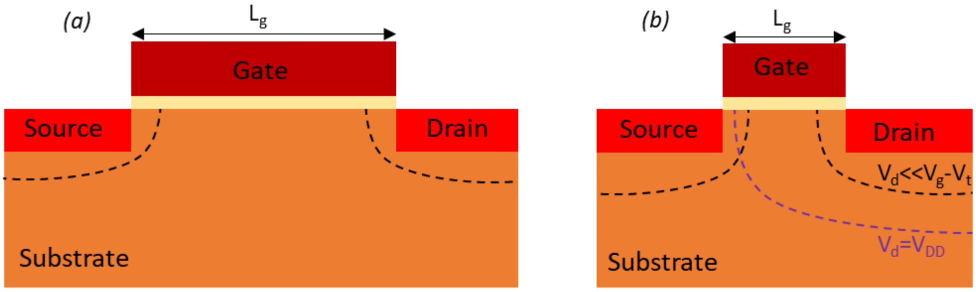

Figure 1-1: Depletion regions in dashed lines for (a): long channel FET and (b): short channel in linear and saturation regions of operation

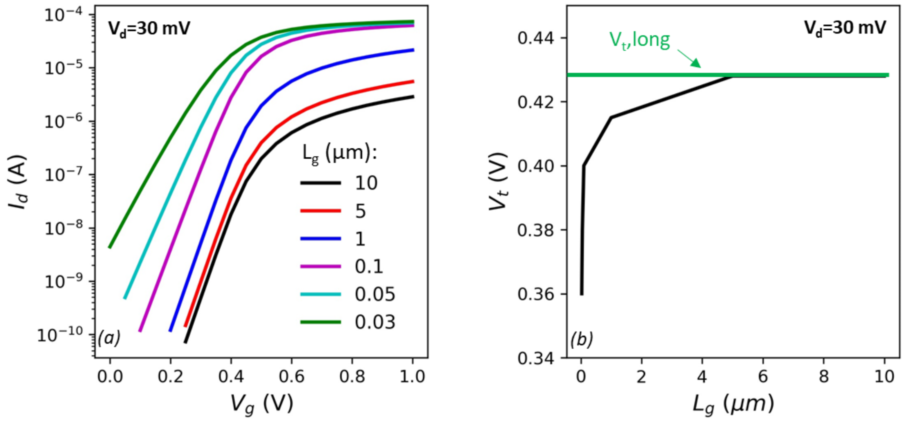

Figure 1-2: (a): Simulated I_d-V_g curves in linear region of operation for various channel length values, (b): Threshold voltage variation with channel length in linear region of operation.

Consequently, new fabrication or architecture techniques were required for high performance electronics to be continued. Indeed, as the Internet of things (IoT) has emerged in our daily lives, the need for low power devices with high performance has reached the top

[11]. Due to the limitations presented above, the “traditional” scaling was replaced by the so-called “equivalent” scaling in the early 2000s [5], in which the combination of downscaling and performance boosting is achieved by the use of new materials, process techniques and structures. In this category, for further device shrinking, innovations such as strained silicon, high-k gate dielectrics, use of other semiconductor materials like germanium, as well as new “nonclassical” device concepts that can overcome the barriers of the conventional MOSFETs were needed [5]. High-k gate dielectrics increase the gate oxide capacitance and thus limit the tunneling current of electrons through the oxide and so the leakage current is reduced while the drive current is increased [6], [8]. In addition, the concept of strained silicon allows the increase of mobility which is achieved by reducing the effective mass or the scattering effects [12], [13]. As a result, both the above methods can significantly improve the device performance in both off- and on-state. Finally, new architectures, as shown in Figure 1-3, have put aside the planar FETs and are in the form of 3D multiple gate field effect transistor for superior gate electrostatic control and elimination of SCEs [14]. On top of that, SOI technology has become really attractive, as it minimizes parasitic effects, originating from interactions between the device and the substrate, and also because it requires less processing steps comparing to the bulk technology [15].

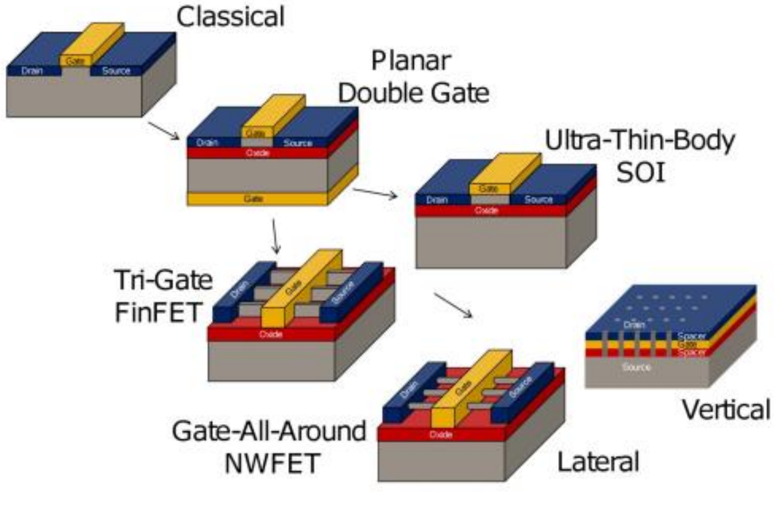

Figure 1-3: Evolution of the Field Effect Transistor Architecture [14].

Despite the significant evolution of device architectures and fabrication techniques, capable to eliminate scaling issues, and their successful introduction in high volume manufacturing, it became evident that shortly beyond 2020 the feature size in planar architectures will reach a few nanometers, and thus further scaling would be impossible [5]. For this reason, many semiconductor industries have emphasized on heterogeneously integrating applications, utilizing the superior performance of non-Si device and component technologies like III-V or SiGe devices and MEMs, towards a direction known as “More than Moore” [11], [16], [17]. As shown in Figure 1-4, 3D integration can form the bridge between the “More Moore” and “More than Moore” directions. Consequently, 3D integration becomes an attractive way for increasing the performance in the next nodes without the requirement of further reduction of device dimensions [18]. For this reason, the future scaling, (2025~2040), is called the “3D Power” Scaling, in which the future products will utilize fully the 3rd dimension for the increase of both component density and speed which can be accomplished by stacking multiple layers of transistors [5].

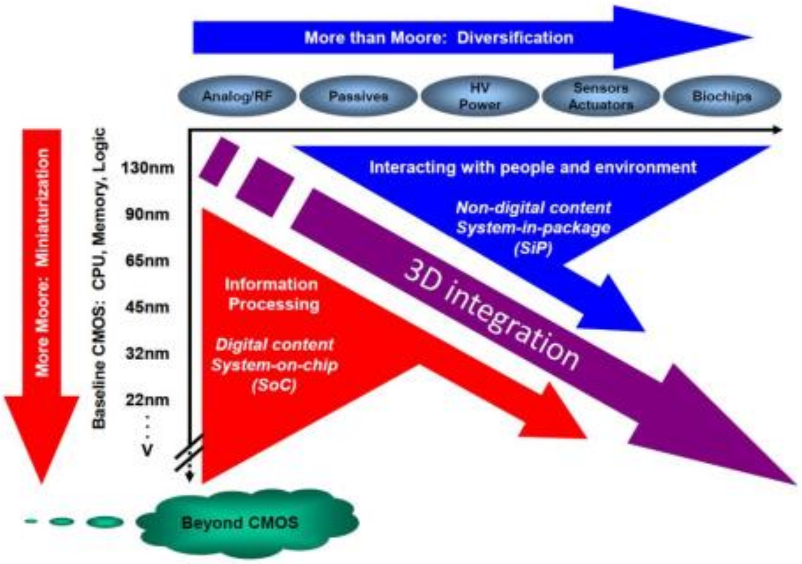

Figure 1-4: Moore’s Law and More [19].

1.2. LFN: A fundamental issue in nano- & micro- electronics

Despite the tremendous evolution of microelectronics with the incorporation of new materials and architectures and the downsizing of the geometrical dimensions, which enhance the performance and speed of transistors, a rise of Low Frequency Noise, LFN, level has been reported [10], [20]. Although the concept of LFN exists for many years [21], one can claim that today the LFN impact is more important than ever. First of all, it should be noted that LFN is an internal type of noise that characterizes the device performance and not an external phenomenon like crosstalk [10]. That means that it cannot be reduced with the help of shielding and layout design but only with appropriate use of materials and process techniques during the fabrication [10], [20], or advanced biasing techniques [22]. The miniaturization of the transistor area jeopardizes the device performance in terms of LFN, as it is widely known that the LFN level is increased with the area reduction [9], [10]. For 1/f-like spectra that originate from the trapping and release of free carriers, the power spectral density of the flat-band voltage, S_{Vfb}, is inversely proportional to the area, which means that if the density of traps is constant among devices with different dimensions, the smallest one will show the highest LFN level. In addition, going from micro to nano scale devices a new type of noise called random telegraph noise, RTN, appears and becomes the main contribution instead of 1/f, as individual trap behavior becomes visible [9], [23]. On top of that, the introduction of new materials and architectures in the CMOS technology results to the appearance of peculiar behavior like the generation-recombination, GR, noise, which exhibit a Lorentzian PSD instead of 1/f [9], [20]. Based on the above, LFN nowadays is a fundamental issue that sets an upper limit in the signal-to-noise ratio [10]. But in order to understand clearly why it is important to study the LFN in more detail, its impact on both device and circuit level should be mentioned.

A. Device Level

The scaling of FET size (channel Length, L_{ch}, and width, W) has minimized the number of traps with only one or few defects being electrically active during the operation of nanoscale transistors [23]. Consequently, the random distribution of traps in both energy and position among different devices of the same scaled-down geometry has increased the so-called LFN variability, which is the variation of the LFN level between different devices on the same wafer. An example is shown in Figure 1-5. GR noise comes to deteriorate this issue, with defective zones inside the channel or the dielectric, whose origin is usually due to the introduction of new materials and fabrication techniques.

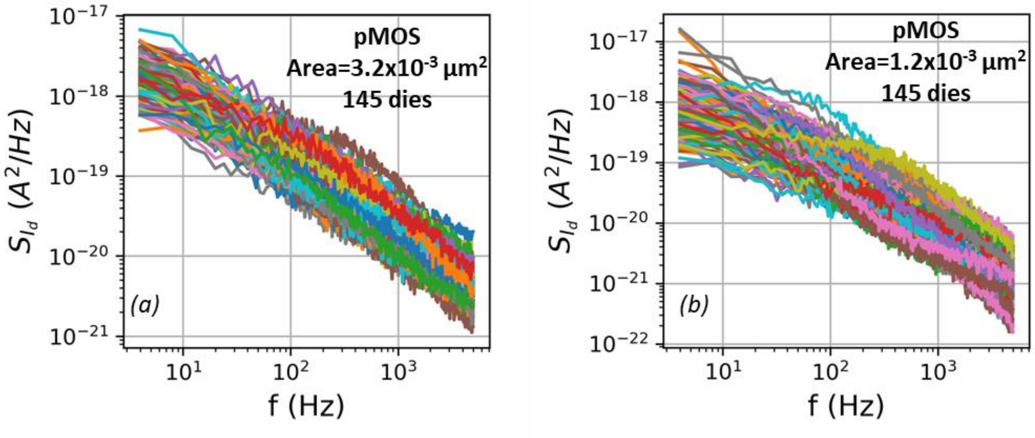

Figure 1-5: Measured drain current power spectral densities versus frequency for 145 dies of pMOS Tri-Gate FETs at $|V_g|=0.5$ V in linear region of operation. (a): Area=3.2x10^{-3} µm^2, (b): Area=1.2x10^{-3} µm^2

Furthermore, the presence of non-1/f noise components results to complex PSDs and timeseries, an issue that complicates the precise characterization of individual traps, which is of critical importance. On one hand, it provides information about the physics of the trap, through which optimization of fabrication methods can be achieved [24]. On the other hand, when inaccurate extraction of current fluctuations occurs, especially in the case of multi-level complex RTN - an example of which is shown in Figure 1-6, issues in the safety margins for the operation of circuits can be caused [25].

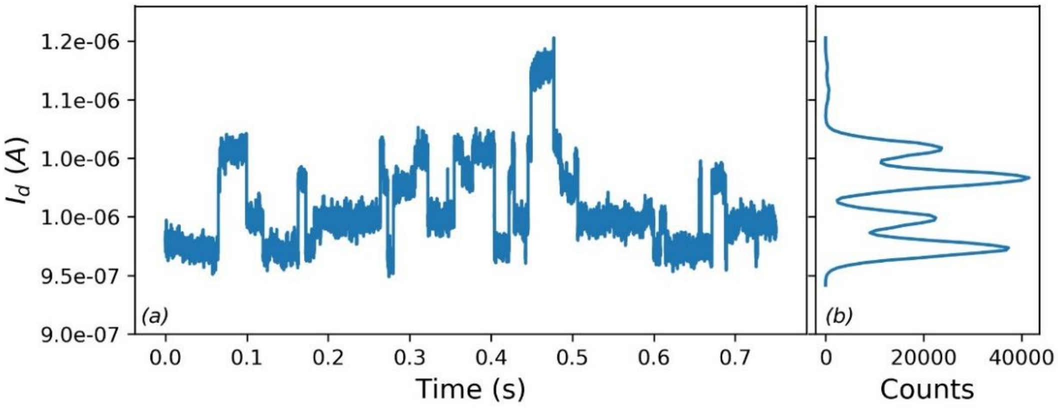

Figure 1-6: Example of measured complex RTN case. (a): Drain current versus Time, (b): Histogram.

B. Circuit Level

Of course, going from device to circuit level, LFN and especially RTN can affect significanlty the functionality of circuits, jeopardizing their safe operation. LFN is a significant issue in analog circuits and systems as it can reduce the signal-to-noise ratio, blocking the detection of small signals [26], and also because the variability of the measured signals is increased. The latter can be seen in Figure 1-7a where the fluctuations of individual pixel's signal are shown due to the presence of RTN [27]. In addition, RTN can also affect the operation of digital circuits, through the threshold voltage fluctuation. In SRAM cells, this kind of fluctuations are interpreted as noise-induced dynamic variability in their response as shown in Figure 1-7b [28]. Also, it has been reported in [29] that depending on the timing of RTN spike, delays or even errors in the write operation can occur (Figure 1-7c). On top of that, LFN can affect the operation of RF circuits as it is upconverted to phase noise close to the oscillation frequency, like in the case of voltage control oscillators [26].

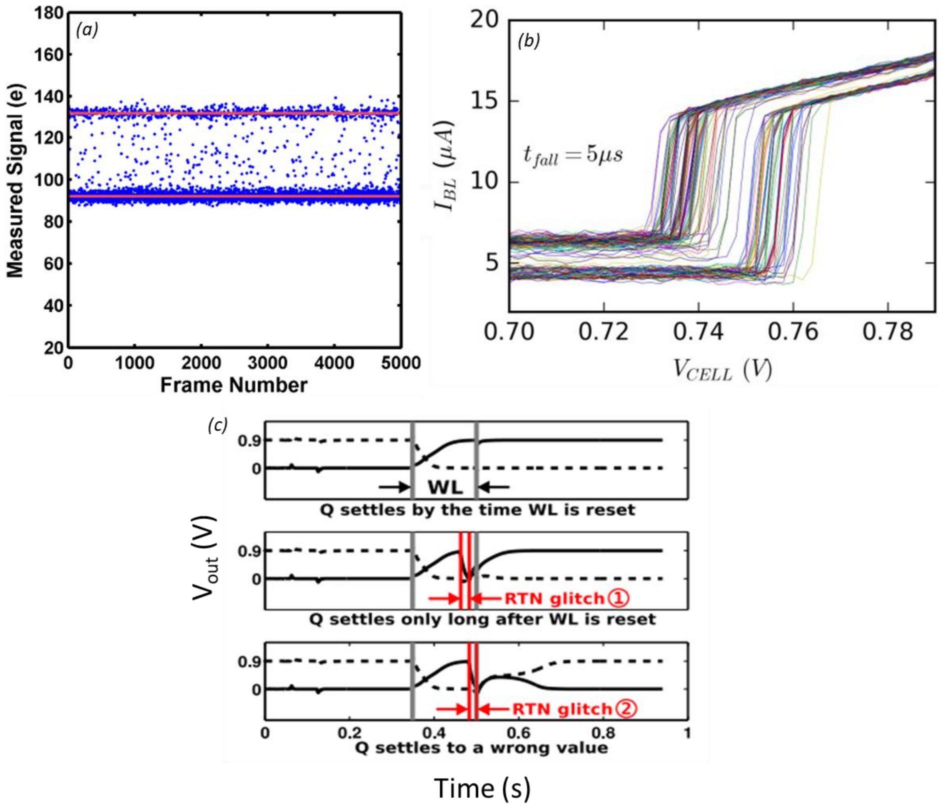

Figure 1-7: Examples of RTN impact on circuits. (a): Fluctuations of measured pixel's signal in image sensors [27]*, (b): Fluctuations in the measured SRAM cell bit-line current* [28]*, (c): Delay or errors in write operation in SRAMs* [29]*.*

As it is presented above the issues that LFN can cause in the operation of single devices and circuits are highly significant, therefore the scientific community needs to tackle the following challenges:

Proper LFN/RTN characterization of advanced technologies: New technologies for "More Moore" and "More than Moore" directions need to be characterized in terms of LFN as the extracted LFN parameters can provide valuable information concerning the quality of the structures.

New characterization and data analysis methods: The particularities of GR noise and RTN dictate the development of new methods of measurements and/or data treatment so as the traps to be properly detected and localized.

New models or modeling approaches: Various effects related to the use of new architectures or materials in novel technologies, or to the aggressive scaling, are not considered in the existing LFN models. For example, concerning the GR noise and RTN, which are very position-dependent, to our knowledge, there is still no explicit model expression that accounts for the lateral/horizontal position and the gate/drain voltage bias dependences.

Precise simulation of noise at a circuit level: Critical defect-related stability and reliability issues in circuit performance have emerged and thus the precise modeling (and model implementation) of noise at a circuit level is essential. This concerns both frequency and time domain noise modeling.

1.3. State-of-the-art studies and motivation

Due to the limitations that LFN can cause in the functionality of devices and therefore, in the operation of whole circuits, LFN is continuously attracting the interest of the scientific community. Extensive LFN studies are carried out on advanced technologies such as Gate-All-Around (GAA), SOI FinFETS, Bulk FinFETs, SiGe FETs, aiming to use LFN as a diagnostic tool for the evaluation of the dielectric and channel quality [30]–[34]. Results have shown that the trapping/detrapping phenomena prevail the 1/f component of the spectra, while thanks to the LFN spectroscopy method, various process induced defects have been identified [34], [35]. However, so far there are limited published works concerning the LFN behavior of emerging "More than Moore" devices, such as low thermal budget MOSFETs [36], intended for future technologies like the 3D sequential integration (3DSI). Furthermore, while the established model utilized for noise parameter extraction is widely applied to advanced technology devices, there are no studies on how the short channel effects can affect the validity of this model as it could be significantly influenced, for example, by the presence of series resistance in short channel devices.

In addition, special attention is given to random telegraph noise, RTN, by the device-physics community, as with the aggressively scaled down devices one or a few defects affect the charge transport [23]. Methodologies based on the time lag plot are developed that allow the easier detection of RTN signals, even under the presence of complex signals (more than a 2-level RTN), or when the background noise is significant [25], [37]. Furthermore, for an overall estimation of number of traps, V_g measurements from weak to strong inversion with a small step are performed so as RTN signals to be detected. Once one RTN signal is detected, additional measurements are carried out for the vertical [38] and lateral position of the trap to be extracted [39]. However, there are not detailed studies on how the SCEs such as CLM and DIBL in saturation can affect the detectability of traps.

Finally, for the accurate study of LFN impact on circuit operation, RTN models in time-domain have been developed to prevent circuits from inevitable errors [29], [40]–[42]. Although time-domain modeling is significant, as it provides access to current fluctuations in time, yet it can be really time consuming. Here is where frequency domain modeling can be useful, but it is limited to the typical 1/f-behavior. Since, the appearance of Lorentzian spectra is more and more frequent in the advanced FET technologies, LFN frequency domain models need to be revised.

1.4. Thesis objectives and main contributions

This thesis aims to take a further step concerning the investigation of Low frequency noise (including GR and RTN) effects in MOS transistors. The study of LFN can lead to results that belong in different but also indirectly associated fields depending on the oriented research direction. This way, we can consider that this thesis has two main directions: the explorative research and the applied one. Based on this categorization and considering the challenges, which tackle both research and industry, the main objectives of my thesis are presented in Figure 1-8.

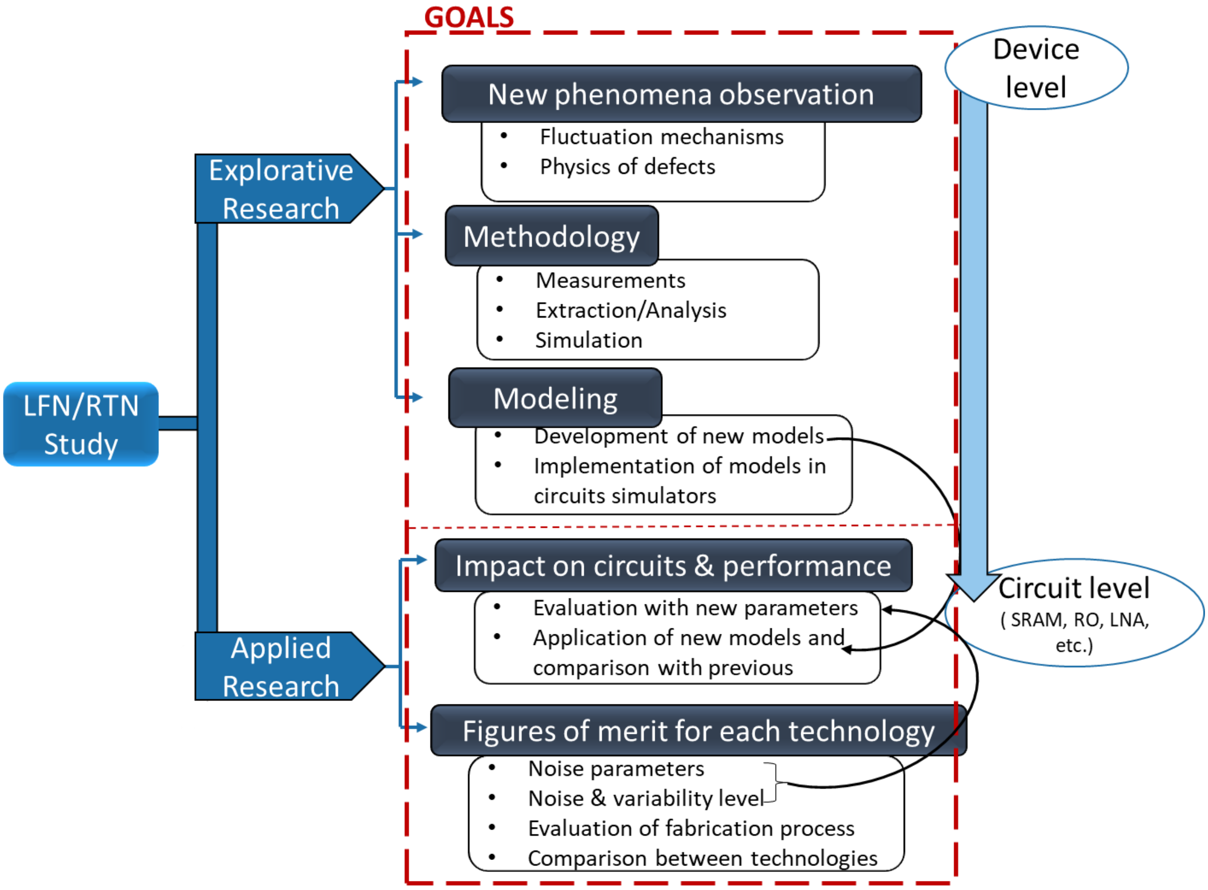

Figure 1-8: Overview of thesis Workplan.

In the explorative approach detailed analysis of the traps' behavior takes place. LFN measurements under different conditions (voltage, temperature) can give us more information on the fluctuation mechanisms and finally obtain a better understanding of the physics of defects, such as their capture and emission behavior (kinetics). This kind of observations are enhanced by new experimental, simulation and data analysis approaches and the positive outcome of those contributes to the development of new noise models valuable for both device and circuit simulations.

The applied part contains the LFN impact on circuits through evaluation of their performance with technology-specific noise parameters or application of existing and new developed models. Another goal in the applied research direction is more industrially oriented and includes the extraction of noise parameters (trap density and coulomb scattering coefficient) and the noise variability level for different technologies and eventually the comparison of those, and/or the identification of defective areas and critical fabrication steps.

Consequently, based on the above objectives, apart from the application of existing LFN models on advanced FET technologies, which is of course very important as performance evaluation can be acquired, a series of new methodologies were developed. These methods are in line with current advanced technologies and aim to make the most of the LFN, both in terms of model validity and deeper understanding of the physics of defects. Finally, these studies are used for the development of models that are applicable from device to circuit level.

The main contributions of this thesis to the state-of-the-art are highlighted below:

- ✓ LFN characterization of FinFET Bulk technology as well as studying the impact of sub-10 nm FIN width and number of FINs on the LFN level.
- ✓ Comparative experimental study of 3DSI-related High and Low temperature fabricated devices and identification of defective zones induced by the fabrication process.
- ✓ Experimental observation of short-channel effects on noise behavior: access resistance impact on parameter extraction and saturation effect on RTN detectability.
- ✓ Development of access resistance-immune method for the reliable extraction of LFN parameters.
- ✓ Development of experimental methodology for maximizing the detectability of traps in highly scaled down devices.
- ✓ Development of a Lorentzian PSD generator in Verilog-A for simulating trap-related noise in CMOS circuits and application in a fundamental circuit like the ring oscillator.

1.5. Thesis outline

This thesis has been categorized as follows:

In Chapter 2, the basics of MOSFETs physics and operation are reviewed so that the drain current fluctuations due to LFN are better understood. Furthermore, the various low frequency noise sources are introduced, focusing mostly on the ones due to trapping and release of free carriers. The existing models of LFN are described and the measurement set-up for the LFN measurements performed during this dissertation is introduced.

In Chapter 3, the origin of low-frequency noise in advanced FET technologies is investigated. The LFN parameters of 14 nm FinFET bulk technology are extracted and the impact of FIN width and number of FINs on the LFN level is presented. Furthermore, a comparative experimental study between high and low temperature devices is conducted so as to observe how the low thermal budget process affects the parameters of flicker noise.

In Chapter 4, we used LFN in an effort to localize defective zones in low temperature SOI MOSFETs. The low thermal budget process is necessary for 3D sequential integration applications and thus, the identification of critical fabrication steps, during this process, is rather important. For this reason, we present a detailed Lorentzian spectrum analysis, with measurements under different configurations, in an effort to localize defective zones and identify the traps' nature.

In Chapter 5, we focus on the short channel effects and how they can either result to the unreliable extraction of LFN parameters or contribute to an easier detection of traps. Consequently, we first prove that under the presence of series resistance, the extracted LFN parameters can be quite questionable. For this reason, we develop a new methodology, that utilizes the Y-function, and suppresses successfully the impact of series resistance on the validity of the extracted LFN parameters. Furthermore, we show through both experiments and simulations that the pinch-off effect in the saturation region of operation can actually be exploited for the modulation of RTN amplitudes and kinetics and thus contributing to the detectability of traps.

In Chapter 6, we present a new method of noise model implementation for circuit simulations, which enables the generation of Lorentzian-type spectra. We show that the 1/f noise modeling is not sufficient to capture neither the measured noise variability nor the total noise power due to the highly scaled down dimensions and spectra complexity. For this reason, we implement in Verilog-A a Lorentzian PSD generator and we apply it in fundamental circuits like the Ring Oscillator so as the impact of Lorentzian type noise to be accurately predicted.

Finally, Chapter 7 provides a brief summary of this dissertation as well as some directions for future research on the field of LFN and RTN.

CHAPTER 2

Theoretical Background of Low Frequency and Random Telegraph Noise in MOSFETs

This chapter provides a theoretical background on electrical noise sources in MOSFETs. Apart from a brief introduction to the definition of noise in electronic devices as well as to the methods that are utilized for the assessment of noise performance, Chapter 2 focuses on the internal device noise which is trap-related and dominates at low frequencies, therefore called LFN. The mechanisms that lead to the appearance of LFN are described, as well as the models that have been developed. These models can be utilized for the evaluation of the oxide quality as well as for the identification/localization of traps. Furthermore, we describe the procedure for the experimental noise measurements and analysis that we followed during this dissertation. But before presenting the theoretical background on LFN, Chapter 2 begins with an overview of the MOSFET operation, and describes some device parameters and effects that are important for a better understanding of the LFN theory.

2.1. Brief Overview of MOSFET operation

The Metal-Oxide-Semiconductor Field effect transistor (MOSFET) is the building block of almost all computing systems and modern electronics and can be under certain conditions viewed as a voltage-controlled resistor [20]. It is considered as the most widely used semiconductor device of every digital circuit, while its use is also important in analog circuits, thanks to its high input impedance. The MOSFET is comprised by four electrodes, the Gate (G), which receives a voltage signal as an input and controls the movement of carriers inside the channel, going from the Source (S) to the Drain (D), and the Bulk (B). Usually, S and B are connected to ground. The chosen gate voltage value (V_g) for a given drain voltage (V_d) allows the current to flow (or not) between S and D by the induced electric field through the oxide layer. This is because the vertical electric field can modulate the carrier density inside the channel, and thus drive the transistor to the OFF or ON state. A schematic cross-section of a n-type (electron channel) bulk MOSFET is shown in Figure 2-1.

The application of voltage bias at the gate will cause a voltage drop across the oxide (ΔV_{ox}) and the Si channel (ΔV_{si}). The latter will be equal to the surface potential of the channel (ψ_s), if the bulk is grounded. Thus, the applied V_g can be expressed by eq. *(2-1)* [43]. By applying the Gauss law at the oxide/silicon interface one can derive that $\Delta V_{ox} = -\frac{Q_s}{\varepsilon_{ox}} t_{ox}$, where Q_s is the charge at the interface, ε_{ox} the dielectric permittivity and t_{ox} the oxide thickness. Also, by defining the oxide capacitance $C_{ox}=\varepsilon_{ox}/t_{ox}$, eq. *(2-1)* can be rewritten as shown in eq. *(2-2)*. Figure 2-2 illustrates the energy band diagram for a positive applied voltage at the gate.

$$V_g = \Delta V_{ox} + \psi_s \tag{2-1}$$

$$V_g = -\frac{Q_s(\psi_s)}{C_{ox}} + \psi_s \tag{2-2}$$

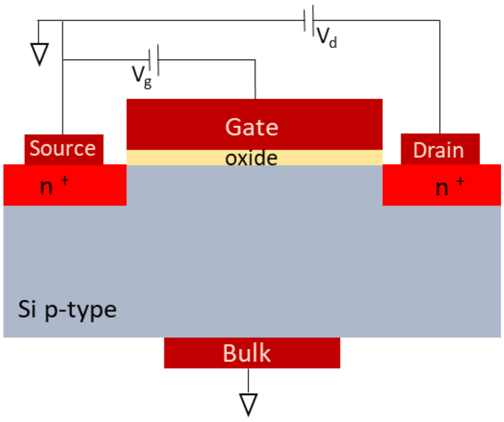

Figure 2-1: Schematic cross-section of a n-type MOSFET.

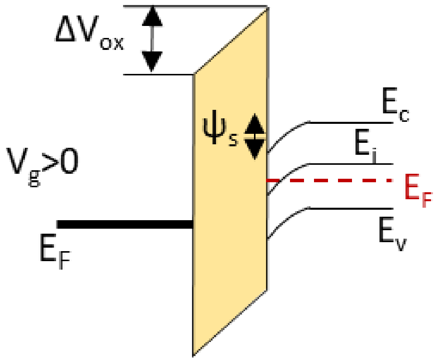

Figure 2-2: Energy band diagram for and n-type FET and V_g>0.

Depending on the value of the potential ψ_s with regards to the Fermi potential ϕ_F, three regions of the MOSFET operation can be defined. It should be noted that for this analysis a NMOS device is considered, in which the Si channel is p-type doped.

- **Accumulation region (ψ_s<0):** The electrons are repelled from the oxide/silicon interface causing an accumulation of holes.
- **Depletion region (0<ψ_s<=ϕ_F, ϕ_F: Fermi potential):** In this case electrons are attracted to the interface and recombine with holes forming negatively charged acceptors which cannot move in the silicon lattice. As a result, the silicon surface is gradually becoming depleted and extends into the silicon depth.
- **Inversion region (ψ_s>ϕ_F):** If a larger positive voltage is applied to the gate, causing a surface potential that exceeds the Fermi potential, the density of electrons at the surface continues to increase and can create a conductive channel formed by the excess free electrons when $\psi_S=2\phi_F$, a condition at which strong inversion is succeeded.

The response of carriers to the gate voltage variations depends on some parameters which characterize the device and are briefly introduced below:

- **Fermi level:** The Fermi level, E_F is defined as the energy level that has 50% probability of being filled will electrons [43]. For an intrinsic semiconductor (no dopants) at room temperature, this level is in the midgap and thus it is equal to the intrinsic energy level, E_i. For extrinsic (doped) semiconductors this level depends on the doping concentration and it is expressed with regards to E_i. Thus, the corresponding Fermi potential for a NMOS is given by the eq. below [7], [43], where k is the Boltzmann constant, T the temperature in Kelvin, q the elementary charge, and N_A, n_i the doping and intrinsic concentrations respectively.

$$\varphi_F = -\frac{E_F - E_i}{q} = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \qquad (2\text{-}3)$$

- **Flat-band voltage, V_{FB}:** The flat-band voltage expresses a condition at which the energy bands across the semiconductor are flat. In the ideal case, where no defects exist, V_{FB} depends only on the work function of the metal, Φ_m, and the semiconductor, Φ_s. In reality, V_{FB} is affected by charges at the oxide and the interface, whose presence is due to the contamination of metals or to imperfections of the Si-O bonds between Si and SiO_2 layers [43].

- **Threshold voltage, V_t:** The threshold voltage equals the gate voltage that needs to be applied in order the transistor to go from the OFF to ON state. It is considered that above V_t the free minority carriers are sufficiently enough to contribute to the conduction of the channel. In terms of the surface potential, V_t is the voltage at which $\psi_s=2\phi_F$.

As one can notice, V_t should be sufficiently low so as the device to reach the ON state quickly (at low V_g value) but not too low since this will increase the leakage current. A quantity that expresses the performance of the device in terms of response to the applied voltage is the subthreshold swing, SW. It is defined as the inverse of the log(I_d) slope in the subthreshold region and it is expressed in mV/decade. The lower the value the faster the switching of the device from the OFF to the ON state. The theoretical minimum of the SW at room temperature is considered to be 60 mV/decade [15].

Finally, the drain current of the MOSFET has been modeled as a function of both gate and drain voltage having as reference the potential at the source. The equations for strong inversion are shown below, where μ_{eff} is the effective mobility of the carriers, and W, L the channel width and length respectively [7]. In addition, Figure 2-3 shows the input and output characteristics of a n-type FET.

$$I_d\,(V_g,V_d) = \left\{\begin{matrix} \frac{W}{L}\mu_{eff}C_{ox}\left(V_g-V_t-\frac{V_d}{2}\right)V_d, for\ V_g \geq\ V_t\ \&\ V_d <\ V_g-V_t \\ \frac{W}{L}\mu_{eff}C_{ox}\frac{\left(V_g-V_t\right)^2}{2}, for\ V_g \geq\ V_t\ \&\ V_d \geq\ V_g-V_t \end{matrix}\right\}$$

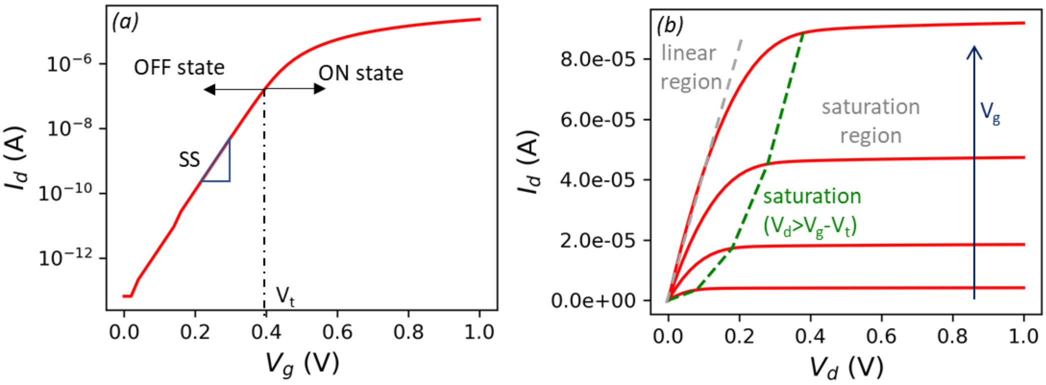

Figure 2-3: (a): Drain current versus gate voltage in the linear region of operation, V_d=30 mV, (b): Output characteristics for different gate voltage values.

2.2. Definition of Noise

In general, noise can be considered as any unwanted signal that distorts a delivered message. In electronic devices noise is seen as current or voltage fluctuations around the expected value, which can be occurred by either external sources, such as parasitic elements, light or vibration, or by the device itself [10]. As briefly mentioned in the previous chapter, although the external noise can be eliminated by some appropriate shielding or design methods, yet another type of noise exists, coming from the device itself and it is related to the physics that govern its operation. Therefore, the study of the internal noise can reveal and explain phenomena of current fluctuations in semiconductor devices. Concerning the timeseries of the fluctuated signal, in most cases only the maximum fluctuation amplitude (shown in Figure 2-4) or the total variance can be extracted. It becomes evident that, from the time domain signal, it is impossible to extract lower fluctuation amplitudes or calculate how often a specific fluctuation occurs. For this reason, the transformation of the signal from time to frequency domain is mandatory.

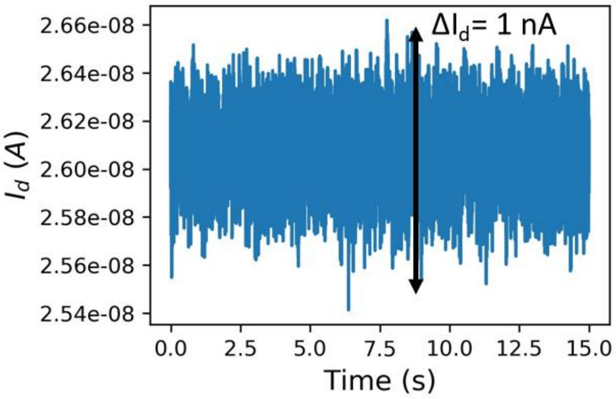

Figure 2-4: Example of drain current fluctuations.

Thus, for more detailed noise analysis the Fast Fourier Transform (FFT) is utilized decomposing the signal power into its constituent frequencies [12]. A quantity that is widely used for noise analysis is the power spectral density (PSD), which gives information regarding the distribution of noise power for a specific bandwidth. The PSD of a signal x(t) is defined as the mean square amplitude of its Fourier transform and in the case at which the signal is current or voltage, the PSD has units of A^2/Hz and V^2/Hz, respectively [44]. In addition, it has been proved that the PSD is the Fourier transform of the autocorrelation function [26], which is a measure of correlation of a signal with a delayed copy of itself. Consequently, the PSD can provide information concerning the randomness (or not) of the signal. Depending on the shape of the PSD, different noise sources can be considered with the main sources existing in MOSFETs in the low frequency range presented in the next section.

2.3. Fundamental Noise Sources

In this section some fundamental physical processes that cause random fluctuations of current or voltage in a device are described. The resulted PSD can give us important information about the nature of the noise source. It should be noted that only internal noise sources are described below.

2.3.1. White Noise

As white noise is considered any noise source whose PSD is independent on frequency and has the form of Figure 2-5. Two are the main sources which result in white noise in electronics. The first one is the thermal noise (Johnson or Nyquist noise) which was first measured by Johnson in 1927 [45], and explained by Nyquist a year after [46]. Its presence is due to the thermal agitation of charge carriers, due to the heat motion of atoms in the crystal lattice, and exists even if the average current is zero [12], [20]. It is regarded as the background noise in any low frequency fluctuations and thus, it can be considered as the lowest limit for signal detection. The result is a fluctuation of the potential between the terminals of a conductor which is enhanced when the temperature of the medium increases. Thus, the voltage PSD of thermal noise depends only on the temperature and the resistance of the medium and is expressed as: $S_V = 4kTR$, where k is the Boltzmann constant, T the absolute temperature and R the resistance.

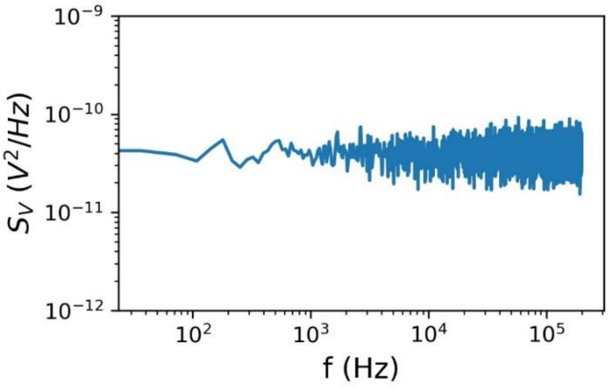

Figure 2-5: Example of white noise PSD.

The second noise source that results to white noise spectrum is the shot noise. This type of noise is due to the discrete nature of carriers that flow randomly through a potential barrier [47]. This is why shot noise is generally observed in devices that have a potential barrier such as p-n junctions and Schottky diodes [12]. Shot noise was firstly discovered by W. Schottky in 1918 in vacuum tubes, who derived the current PSD formula, which depends on the electronic charge and the dc flowing current in the junction and expressed as $S_I = 2qI$. Since shot noise also causes a white noise spectrum, it is rather difficult to be distinguished from the thermal noise with no current change. However, it has been reported that its PSD is generally smaller that the corresponding thermal one [12].

Although the noise sources presented above are present in a wide frequency bandwidth from low to high frequencies, yet the low frequency region is dominated by other types of noise, which are described below. In this dissertation, when referring to low frequency noise, we mean the below types of fluctuations that exceed the white noise at low frequencies.

2.3.2. Generation-Recombination Noise

Generation-recombination noise (GR), is due to fluctuations in the number of free carriers, caused by their random interaction with traps. These traps are localized states that cannot contribute in the conduction and exist due to defects or impurities inside the semiconductor or at the interfaces. Apart from the carrier number fluctuations, these traps can also affect the carrier mobility through scattering, the electric field and the potential barrier [48]. The transitions of free carriers that can occur in a semiconductor resulting to GR noise are cited below:

i. Recombination of a free electron with a free hole
ii. Generation of a pair of a free electron and a free hole
iii. A free electron is trapped at an empty trap
iv. A free hole is trapped at a filled trap

The fluctuations of the number of free carriers, N, can be interpreted as fluctuations of the resistance or conductivity, σ, of the medium, as expressed by eq. *(2-4)* for n-type semiconductor, where n is the electron concentration and μ_n their mobility [20]. This change of conductivity due to trapping and release of free carriers can be seen as current fluctuations when voltage is applied across the device terminals.

$$\sigma = qn\mu_n \tag{2-4}$$

For the case where a group of traps exists with the same time constant the drain current PSD is given by eq. *(2-5)* [20], where N is the average number of free carriers, $\overline{\Delta N^2}$ is the variance of the fluctuating number of free carriers, τ the time constant and f the frequency. The relaxation time, τ, is characteristic for each group of traps and depends on the average capture and emission time of the trap with the expression, $\tau = (1/\overline{\tau_c} + 1/\overline{\tau_e})^{-1}$, where $\overline{\tau_c}$ and $\overline{\tau_e}$ are the average capture and emission time respectively. The PSD of eq. *(2-5)* has a Lorentzian-like shape, which is shown in Figure 2-6a. It is characterized by a constant level (plateau) at low frequencies and by a corner frequency $f_c=1/(2\pi\tau)$ above which the PSD is inversely proportional to the square of the frequency. For better visualization, and thus more accurate extraction of Lorentzian parameters, it is convenient to plot the product of frequency with PSD, as shown in Figure 2-6b, so as the peak of the Lorentzian spectrum to be emphasized and the determination of the characteristic frequency to be easier. By altering the applied voltage, the activity of the traps changes and reaches its maximum value when the Fermi level equals the traps' energy level.

$$\frac{S_{I_d}}{{I_d}^2} = \frac{S_R}{R^2} = \frac{S_N}{N^2} = 4\frac{\overline{\Delta N^2}}{N^2}\left(\frac{\tau}{1+(2\pi f\tau)^2}\right) \tag{2-5}$$

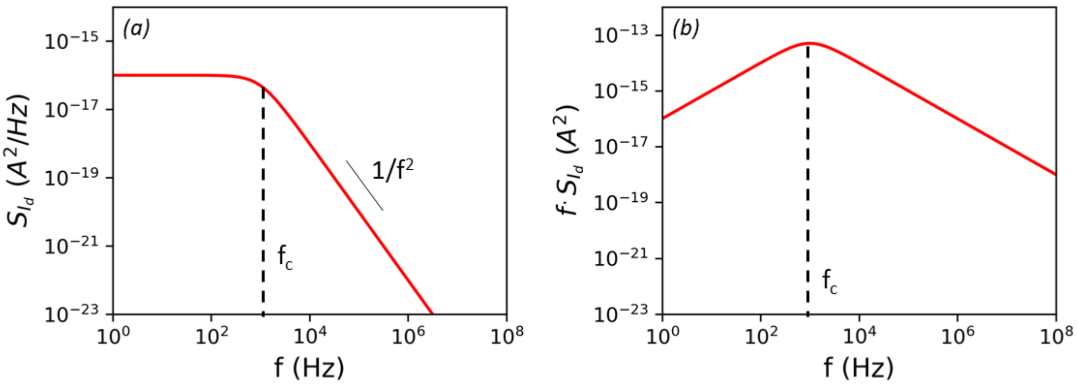

Figure 2-6: Lorentzian-like spectrum.

In general, the study of GR noise can provide valuable information about the physics of the traps as well as their spatial position and energy level. The characteristic time constant of a trap depends on the capture and emission time, as described above, which in turn are affected by the carrier concentration [49]. Consequently, there is a shift of the Lorentzian spectrum with temperature, due to the change of the characteristic time. This dependence with temperature can be utilized through noise spectroscopy analysis, which leads to the construction of an Arrhenius diagram [48], an example of which is shown in Figure 2-7.

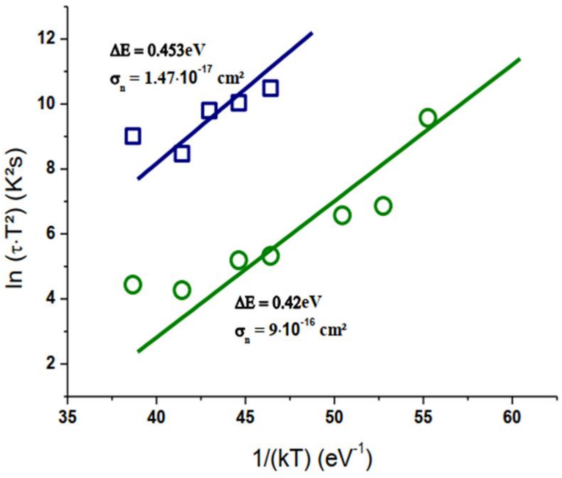

Figure 2-7: Representative example of an Arrhenius diagram [50].

In the case where the resulted Arrhenius plot is a straight line, not only it is confirmed that the Lorentzian spectra correspond to the same group of traps, but also there is the possibility for fabrication steps, which led to the appearance of these traps, to be identified through the extraction of traps' cross section and energy level. Apart from temperature dependence analysis, noise measurements at different polarization conditions at room temperature can provide information about the spatial location of the traps. In the cases where τ has a strong dependence on V_g, traps are considered to be at the interface whereas when no significant variations of τ are observed the traps are generally assumed to be in a depleted region inside the channel [48]. However, the latter might not be necessarily true for advanced devices like FDSOI MOSFETs where full volume inversion of channel occurs [51]. As a result, it becomes evident that the study of the origin of GR noise is not an easy task and can become even more complicated in cases where more than a single Lorentzian spectrum are present in the total PSD.

2.3.3. Random telegraph Noise

Random Telegraph Signal, RTS, or Random Telegraph Noise, RTN, is a special case of GR noise, which has a Lorentzian spectrum shape as in the case of GR, but can be also seen in the time domain through discrete switching events of the drain current. It is attributed to individual carrier trapping and release when only a few traps or even a single trap are present, therefore it is observed in devices with very small area, in most cases < 1μm^2 [52]. The simplest form of RTN, in terms of analysis, is the two-level drain current pulse series which correspond to the events of capture and release of a single carrier. The histogram of the drain current levels is no longer Gaussian, and gives two peaks with a distance equal to the average RTN amplitude ΔI_d, whereas the average $\overline{\tau_c}$ and $\overline{\tau_e}$, can be extracted from the timeseries, provided that there is an adequate number of pulses. An example of a 2-level RTN (1 trap) is shown in Figure 2-8. The PSD is given by eq. *(2-6)*, where A is the space mark ratio and equals A = τ/($\overline{\tau_c}$ +$\overline{\tau_e}$), and ω the angular frequency. The A parameter depends on the ratio of $\overline{\tau_c}$ and $\overline{\tau_e}$, which means that in the case where $\overline{\tau_c}$ is much larger than $\overline{\tau_e}$, or the reverse, the trap is almost always empty or filled, respectively. As a result, beyond or below a certain V_g region the trap will not contribute to the Lorentzian spectrum. Finally, once RTN is statistically studied, physical parameters that characterize a trap can be provided such as such as its energy within the bandgap, horizontal, lateral position and cross-section [53].

$$S_{I_d} = 4A\Delta I_d{}^2 \frac{\tau}{1+\omega^2\tau^2} \tag{2-6}$$

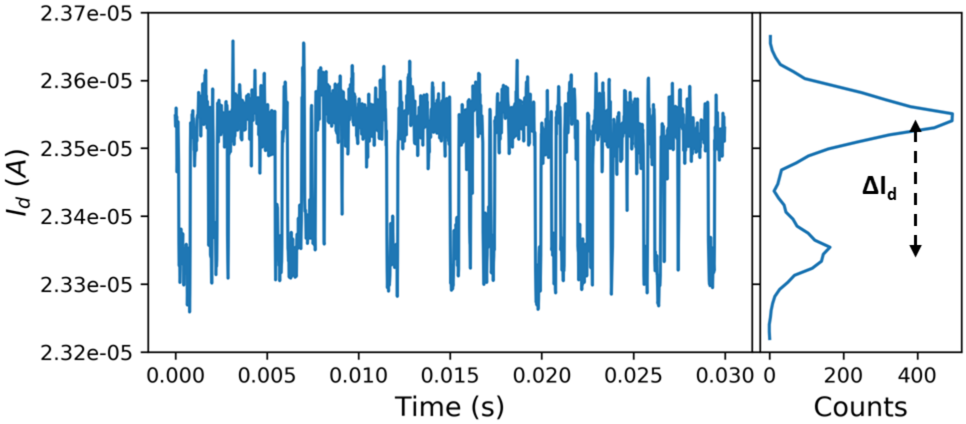

Figure 2-8: Measured time domain plot of drain current and histogram for RTN noise. Device characteristics: p-type Trigate SOI FET with W/L = 30/10 nm, at |V_g| = 1.12 V and |V_d| = 30 mV.

2.3.4. Flicker Noise

Several mechanisms have been studied that result to the flicker noise. The first one suggests that, as opposed to the RTN case, flicker or ‘1/f’ noise can be considered as the combination of a few Lorentzian type spectra, with their τ values exponentially distributed across a wide range of many orders of magnitude. For that to happen, the condition that needs to be fulfilled is the traps to be uniformly distributed in both energy and location inside the oxide [26]. This can be seen in Figure 2-9, where it is shown that even six Lorentzian spectra can sum up to a final 1/f-like one for a wide range of frequencies. The PSD of flicker noise is expressed as $S_{I_d} = \frac{K}{f^{\gamma}}$, where K is bias-dependent, and γ the frequency exponent [47]. The parameter γ usually varies between 0.7 and 1.3 and it is an indicator for the uniformity of traps. More specifically, in the ideal case, γ=1 which means that the trap density is uniform across the depth of the oxide. On the other hand, when γ<1, it means that the majority of traps show small values of time constants, leading to the conclusion that the trap density is higher close to the interface whereas when γ>1, the trap density is considered to be higher as going deeper in the gate oxide [47], [48].

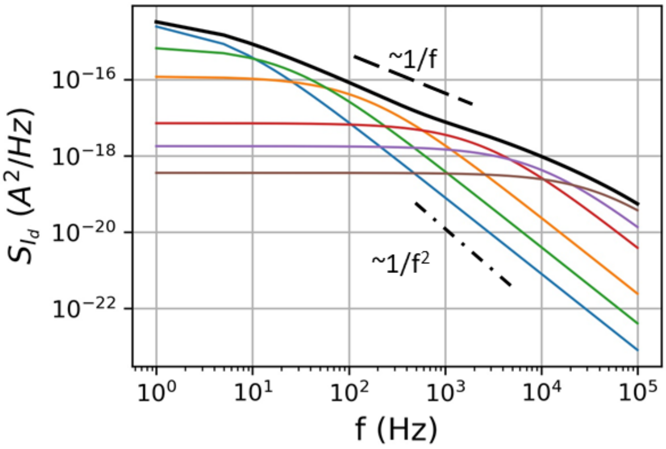

Figure 2-9: Spectrum result of adding Lorentzian spectra resulted from uniform distribution of traps.

The second mechanism that can result in 1/f noise is the mobility fluctuations. This mechanism was first described by Hooge [54], [55], stating that flicker noise stems from the bulk mobility fluctuations which in turn vary the conductance [56]. The main reason for the fluctuations of the mobility is the variations of phonon-carrier scattering due to lattice vibrations [56], [57].

There has been a long debate in the scientific community about which mechanism causes 1/f noise and thus researchers have tried to figure out which of the two is the principal contributor: carrier number or mobility fluctuations? In fact, it is likely that both mechanisms can take place and contribute to 1/f noise, but depending on the situation, either the one or the other might dominate the 1/f noise spectrum. This can be proved by applying the developed models for each mechanism on the measured 1/f PSDs.

Finally, Figure 2-10 shows three different types of noise, thermal, flicker, and RTN along with their PSD and autocorrelation function, which as mentioned above expresses the randomness of the signal. One can observe that in the case of thermal noise, the autocorrelation function goes directly to zero, confirming its total random nature. On the other hand, this does not happen for the two other types of noise, where it is obvious that the autocorrelation function varies at a slower rate. This is due to the fact that both flicker and RTN noise are governed by characteristic relaxations times so they cannot be considered as totally random processes.

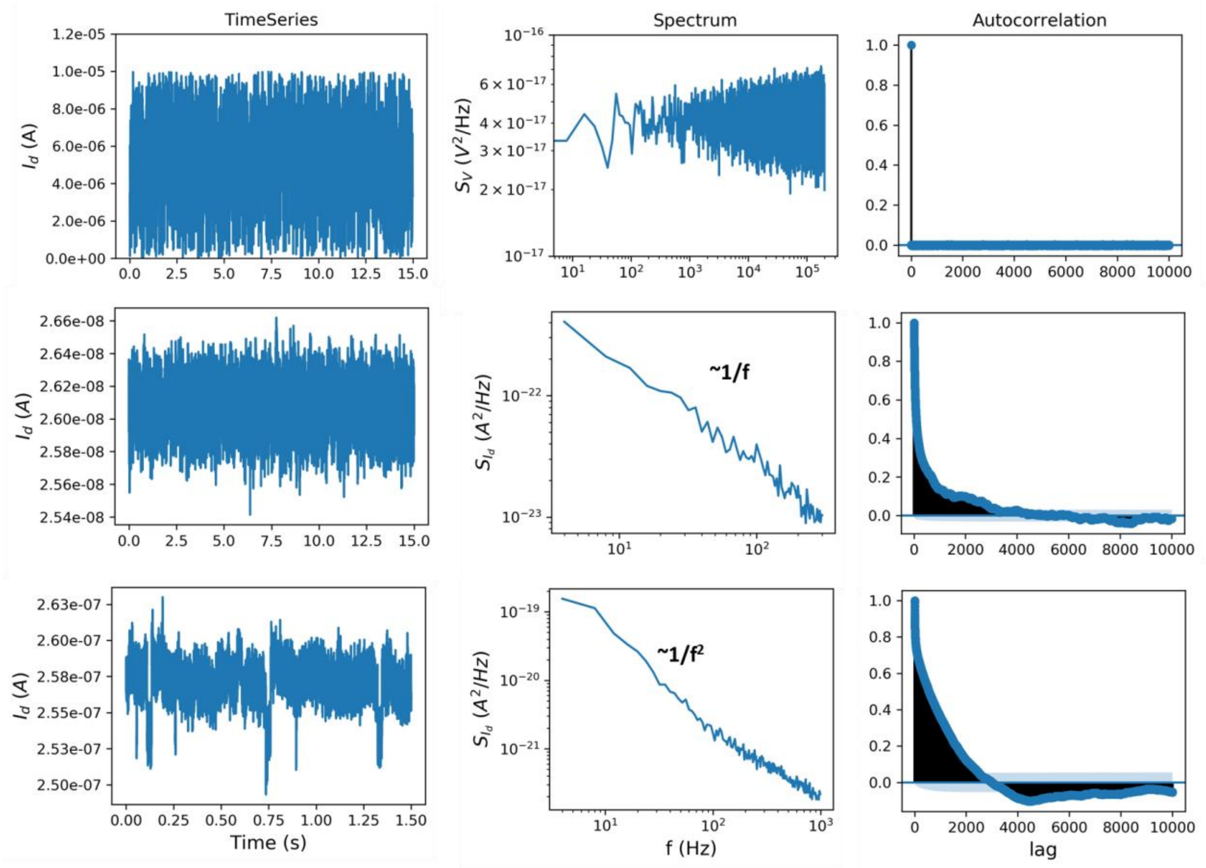

Figure 2-10: Illustration of three different type of noise in time domain and their corresponding PSD and autocorrelation function.

2.4. LFN modeling

2.4.1. Mobility fluctuations model

This modeling approach has been presented by Hooge [58], according to which the fluctuations of the drain current stems from fluctuations of the carrier mobility mainly due to phonon scattering effects. This leads to a flicker noise PSD whose amplitude is inversely proportional to the total number of free carriers in the device. The empirical formula of the normalized drain current noise for MOSFETs is thus given by eq. *(2-7)* [58], where Q_i is the inversion charge and α_h is the Hooge parameter, which depends on the quality of the crystal and on the scattering mechanisms that contribute to the final mobility.

$$\frac{S_{I_d}}{{I_d}^2} = \frac{q\alpha_h}{WLQ_i f} \tag{2-7}$$

As it can be observed from eq. *(2-7)*, the normalized drain current PSD varies as the reciprocal of the drain current and thus, once the experimental PSDs follow this trend, it is concluded that Hooge mobility fluctuations prevail. Although there are published works in which it is claimed that the MOSFET 1/f noise is due to mobility fluctuations [59], the experimental results presented in this thesis could not validate this model.

2.4.2. Carrier number fluctuations (CNF) model

In 1957, A. McWhorter [21] demonstrated that the physical mechanism behind the 1/f noise can be the carrier number fluctuations caused by trapping/detrapping in semiconductor surface or semiconductor/oxide defects. This dynamic trapping and release of carriers results to fluctuations in the surface potential and thus affecting the inversion charge density. An abstract illustration of this phenomenon is shown in Figure 2-11.

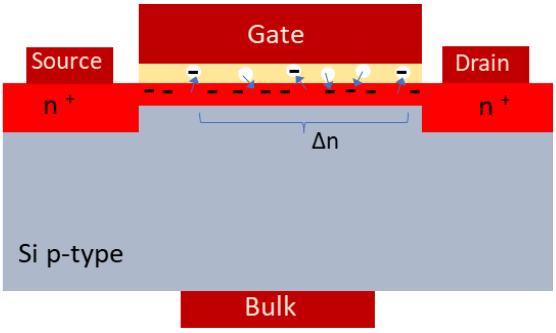

Figure 2-11: Schematic illustration of electrons moving in and out of oxide traps.

Every trapping of Q_{ox} will cause a fluctuation in the oxide charge density ΔQ_{ox}, consequently resulting in changes of the flat-band voltage through eq. *(2-8)*, where Q_{ox} is given by eq. *(2-9)* with N_{ox} being the number of trapped carriers and C_{ox} the oxide capacitance [60].

$$\Delta V_{FB} = -\frac{\Delta Q_{ox}}{C_{ox}} \tag{2-8}$$

$$Q_{ox} = \frac{qN_{ox}}{WL} \tag{2-9}$$

Based on eq. *(2-8)*, the corresponding drain current fluctuations, as I_d is a function of V_{FB}, will be given by eq. *(2-10)* and since $\Delta V_{FB}=-\Delta V_g$, eq. *(2-10)* can take the form of eq. *(2-11)*, where $g_m=dI_d/dV_g$ represents the transconductance of the device. It should be noted that in this case the mobility of the carriers is considered constant [60].

$$\Delta I_d = \frac{\vartheta I_d}{\vartheta V_{FB}} \Delta V_{FB} \tag{2-10}$$

$$\Delta I_d = -g_m \Delta V_{FB} \tag{2-11}$$

Taking the PSD of drain current, eq. *(2-11)* takes the form of eq. *(2-12)*, which in combination with eq. *(2-8)* and *(2-9)*, can be rewritten and expressed by eqs. *(2-13) and (2-14).*

$$S_{I_d} = {g_m}^2 S_{V_{FB}} \tag{2-12}$$

$$S_{I_d} = {g_m}^2 \frac{q^2 S_{N_{ox}}}{W^2 L^2 {C_{ox}}^2} \tag{2-13}$$

$$\frac{S_{I_d}}{{I_d}^2} = \frac{{g_m}^2}{{I_d}^2} \frac{q^2 S_{N_{ox}}}{W^2 L^2 {C_{ox}}^2} \tag{2-14}$$

As it can be concluded from eq. (2-14), the normalized drain current for the CNF model is proportional to $(g_m/I_d)^2$ as opposed to the Hooge mobility fluctuation model which is inversely proportional to I_d. This is one of the main differences between these two models and one can easily, through the application of the models, find out which mechanism dominates the 1/f noise.

The final spectral density of the oxide charges depends on the physical trapping mechanism of carriers into the oxide [53]. The McWhorter model considers that trapping and detrapping occurs through tunneling processes [21]. The trapping time constant due to tunneling is expressed by eq. *(2-15)*, where z is the distance from the interface, λ the tunneling attenuation length (≈ 0.1 nm), and τ_0 is a time constant usually taken as 10^{-10} s. By combining eqs. *(2-5)*,(2-14) and *(2-15)* and replacing in *(2-12)*, the PSD of the flat-band voltage can be derived as expressed in eq. *(2-16)*, where N_t is the density of traps uniformly distributed in space and energy (in $cm^{-3}eV^{-1}$), as it is impossible to know the PSD for each individual trap.

$$\tau = \tau_0(E)e^{z/\lambda} \tag{2-15}$$

$$S_{V_{FB}} = \frac{q^2\lambda kTN_t}{f^\gamma WL{C_{ox}}^2} \tag{2-16}$$

Consequently, when the experimental normalized drain current PSD fits well the $(g_m/I_d)^2$ at a specific frequency, it can be confirmed that the trapping and release of carriers prevails the 1/f noise and, based on eq. *(2-16)*, the volumetric trap density per eV can be extracted, which is an important information for the evaluation of the oxide quality. In addition, a quantity that is really useful in the low frequency noise analysis is the input-referred gate voltage noise S_{V_g} which is calculated through $S_{V_g} = S_{I_d}/{g_m}^2$. This quantity determines the theoretical gate voltage noise at the input of a noiseless transistor that would lead to the same S_{I_d} at the output. Apart from the fact that the extraction of trap density becomes easier by using the S_{V_g}, which in the case of CNF is constant with V_g and equals to $S_{V_{FB}}$, S_{V_g} is also very useful in noise modeling, as it is easier to connect a voltage noise source at the input rather than a current noise source at the drain [61]. The latter cannot be implemented with a constant PSD but it depends each time on the value of the drain current. Another advantage of S_{V_g} is its use in variability studies, since the variability of S_{V_g} is free of threshold voltage and mobility variations included in g_m/I_d. An example of this use is shown in Figure 2-12, where one can observe that the device-to-device variability of normalized S_{I_d} at a given frequency is higher compared to the corresponding S_{V_g}.

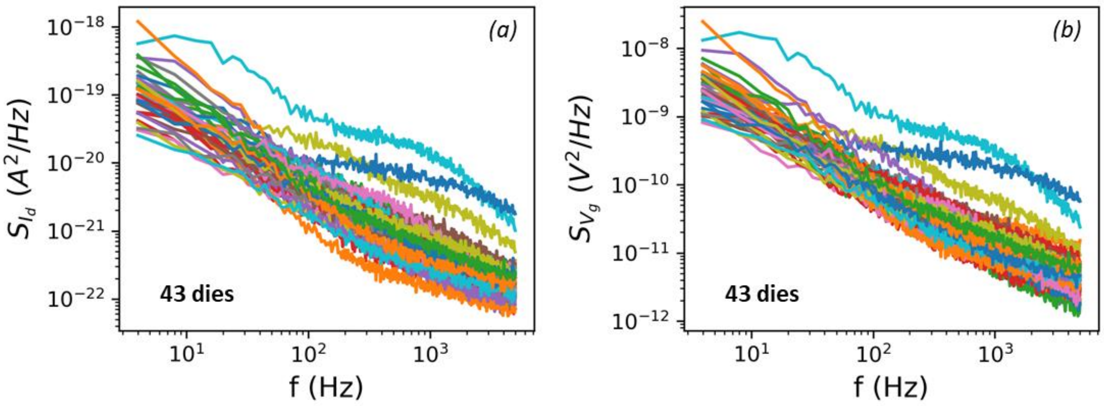

Figure 2-12: (a): Measured Drain current PSDs versus frequency for n-type FINFETs, (b): Input-referred gate voltage noise versus frequency.

2.4.3. Carrier number with correlated mobility fluctuations model

The previous section considers only fluctuations of the carrier number due to the dynamic trapping and release of free carriers. If this is the only mechanism that induces the 1/f noise, the S_{V_g} should be independent of the gate voltage. But this is not always the case since it has been shown that sometimes S_{V_g} increases with V_g, especially above V_t [62]. When the latter occurs, the classical CNF model cannot fit the experimental normalized drain current PSD as shown in Figure 2-13. This is the case in which it can be considered that, in a way, both carrier and mobility fluctuations coexist. Consequently, Ghibaudo [62] and Hung [63] proposed the carrier number with correlated mobility fluctuations model (CNF/CMF) which considers fluctuations of the surface mobility due to remote Coulombic scattering effect of the fluctuating oxide charge. An illustration of this phenomenon is shown in Figure 2-14.

To include the additional drain current fluctuations by the mobility scattering, eq. *(2-10)* needs to be rewritten as in eq. *(2-17)*. By using a general admitted mobility law of the form: $1/\mu_{eff}=\alpha_{sc}Q_{ox}+1/\mu_{eff,0}$, where α_{sc} is the so-called remote Coulomb scattering parameter and $\mu_{eff,0}$ is either constant or a function of the electric field or inversion charge [62], eq. *(2-17)* can take the form of eq. *(2-18)*, in which the – and + correspond to acceptor-like and donor-like traps.

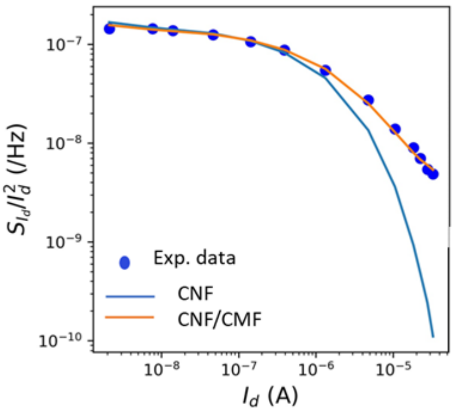

Figure 2-13: Normalized drain current noise versus drain current, measured at drain voltage V_d = 30 mV, along with the CNF and CNF/CMF fitting models

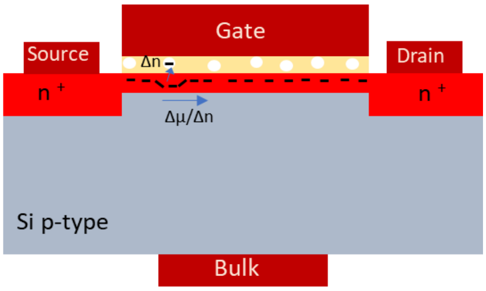

Figure 2-14: Schematic illustration of electrons moving in and out of oxide traps.

$$\Delta I_d = \Delta V_{FB} \left.\frac{\partial I_d}{\partial V_{FB}}\right|_{\mu_{eff}=const} + \Delta \mu_{eff} \left.\frac{\partial I_d}{\partial \mu_{eff}}\right|_{V_{FB}=const} \qquad \textit{(2-17)}$$

$$\Delta I_d = -g_m \Delta V_{FB} \pm \alpha_{sc} \mu_{eff} C_{ox} I_d \Delta V_{FB} \qquad \textit{(2-18)}$$

Therefore, the total normalized drain current PSD can be expressed by eq. *(2-19)*. As it can be seen in Figure 2-13, the CNF/CMF model can fit perfectly the experimental PSD. Later, since it was proved that the product $\alpha_{sc}\mu_{eff}$ is constant with V$_g$ [64], eq. *(2-19)* took the form of eq. *(2-20)*, where $\Omega = \alpha_{sc}\mu_{eff}C_{ox}$, is the bias-independent CMF coefficient. Finally, the expression for the input-referred gate noise, including the CMF coefficient is given in eq. *(2-21)*.

$$\frac{S_{I_d}}{{I_d}^2} = (\frac{g_m}{I_d})^2 S_{V_{FB}} (1 \pm \alpha_{sc} \mu_{eff} C_{ox} \frac{I_d}{g_m})^2 \qquad \textit{(2-19)}$$

$$\frac{S_{I_d}}{{I_d}^2} = (1 \pm \Omega \frac{I_d}{g_m})^2 (\frac{g_m}{I_d})^2 S_{V_{FB}} \qquad \textit{(2-20)}$$

$$S_{V_g} = (1 \pm \Omega \frac{I_d}{g_m})^2 S_{V_{FB}} \qquad \textit{(2-21)}$$

2.5. LFN measurement and analysis

The measurement of low frequency noise is a complex process and proper isolation is required, as the signal to be measured is very weak and can be easily distorted by external or internal disturbances such as light, mechanical vibrations, AC supply network or even mobile phones [9]. To avoid disturbances caused by the network of power supply, the use of batteries is recommended so as undesired harmonics (like 50 or 60 Hz) to be eliminated. On top of that, proper shielding of the probe station can minimize further the risk of disturbances and this can be achieved by the use of a Faraday cage. A schematic illustration of a noise measurement system is shown in Figure 2-15. In our case, we used a Cascade Microtech 300 mm semi-auto probe station for the device under test which is connected with a programmable point probe system NOISYS7 [65], that includes a low noise current-to-voltage amplifier, LNA, with variable sensitivity so as the maximum amplification of all current levels to be achieved. For this reason, in this work drain current fluctuations are measured instead of voltage. The system is connected to the PC so as the user to utilize the corresponding software and define the configurations of the measurements.

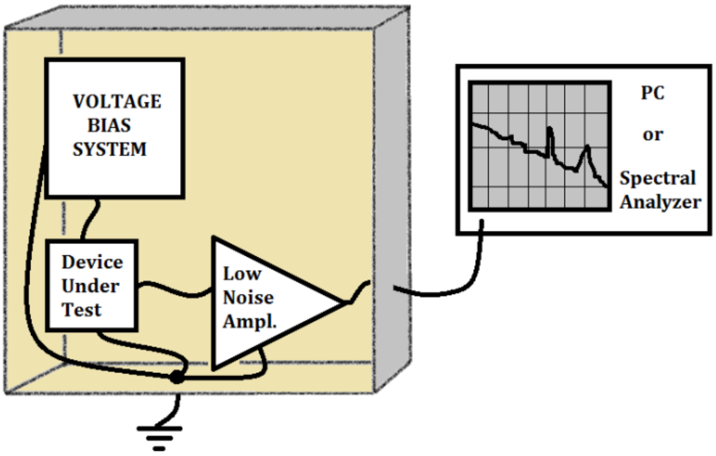

Figure 2-15: Schematic of a noise measurement system [9].

To begin with, the user, apart from the polarization conditions, needs to select the current or voltage values at which noise measurements will be performed. Subsequently, the measurement window for FFT application on the time domain signal needs to be defined. The duration of the measurement and the sampling frequency depend solely on the needs of the researcher in terms of the resolution of the resulting spectra and the duration of the measurements. A parameter that can increase the reliability of the result is the number of sampling windows, based on which an average of the PSD is taken. The drawback in this case is that for the same measurement duration, the lower frequencies are sacrificed, an issue that is shown in Figure 2-16. In any case, this can be adjusted by the user based on the needs. In our case we chose the number of windows to be 60 with minimum frequency 4 Hz and thus, the total process for one polarization condition lasts 15 s. The maximum frequency was chosen to be 10^5 Hz. All the LFN measurements were performed using the programmable point probe system NOISYS7 [65] and a 300 mm semi-auto wafer station.

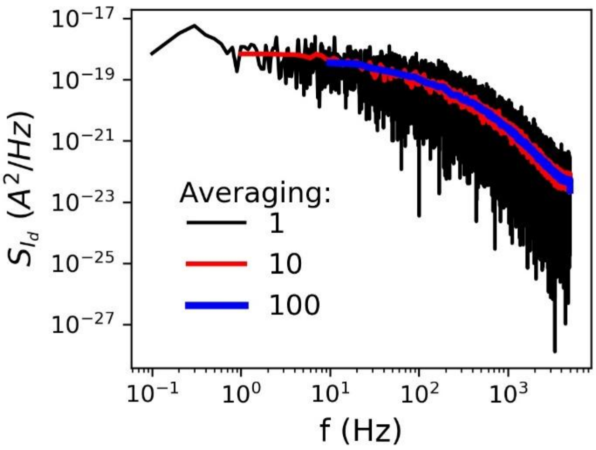

Figure 2-16: Drain current PSD versus frequency for different number of windows.

Once the noise measurements are finished the analysis of the PSDs follows. Before the application of models, any background noise needs to be removed as it can complicate the noise analysis process. In our case, before exploiting the spectra, we filter the measured PSDs based on the bandwidth of the LNA. The issue in this case is that the higher sensitivity the lower the bandwidth of the amplifier and so in the subthreshold region, where the current level is low, the measured PSDs have a limited bandwidth. Once the background noise is removed the LFN analysis can start, for which we used Python and especially the Matplotlib and Pandas libraries.

2.6. Summary

In this chapter a brief description of the operation of MOSFET was made and some of its parameters that are affected by noise were explained. Additionally, a theoretical background of internal noise types was reviewed focusing mostly on the low frequency range. Finally, the developed models were described so as to be utilized for noise parameter extraction and better understanding of the physics of traps.

CHAPTER 3

Flicker Noise Characterization of 3D CMOS Structures

3.1. Introduction

The demand for integration of an ever-increasing number of components, that have robust performance not only in terms of drive current and power consumption but also reliability-wise, has emerged for the development of new technologies and architectures. The performance of conventional planar devices has reached its limits, with the short channel effects (SCEs) having the major contribution on that, for gate lengths below 30 nm [66]. The solution to these issues came with the 3D FinFET/Tri-gate or Fully Depleted SOI structures which provide better electrostatic control. A different but equally groundbreaking approach is the 3D layering of devices, either through stacking or 3D sequential integration (3DSI), techniques that enable the next generation of circuits as full use of the 3rd dimension is allowed which result to increased number of components without further area reduction [18], [67]. A systematic study of FinFET and 3DSI technologies has been performed, aiming to evaluate their performance in different fields.

In this chapter, we use the LFN as a tool to evaluate different technologies, in terms of gate oxide interface quality, as well as strength of scattering effects. We take advantage of the extraction of noise parameters (N_t and Ω) utilizing the 1/f-like part of LFN to pursue a comparative experimental study between different technologies. By this way, we can have a first idea regarding the fabrication steps that are probably responsible for the performance degradation of the different devices in terms of LFN, which in turn could affect significantly the safe operation of circuits.

The first part of this chapter is devoted to 14 nm Bulk FinFET LFN characterization. The devices were fabricated at IMEC-Leuven and we had the chance to characterize them in the framework of the ASCENT program [68]. LFN figures of merit will be presented having as parameters the fin width, number of fins and channel length. The second part focuses on devices fabricated under the 3DSI process, which are limited to low thermal budget (LT). Both LT Junctionless and Inversion Mode MOSFETs have been characterized and compared to their high temperature counterparts.

3.2. 14 nm Bulk FinFET Technology

As the dimensions of conventional MOSFETs are aggressively decreasing and short channel effects (SCEs) are becoming critical for the transistors' safe operation, new technology characteristics are introduced in order these issues to be eliminated. For the reduction of drain potential impact on the channel uniformity in planar MOSFETs, the oxide thickness is reduced so as the vertical field to be enhanced, and the channel doping is increased which in turn can increase V_t and reduce the leakage current [66]. But these technological steps cannot become permanent solutions, as the tunneling through the gate oxide forces a minimum allowed oxide thickness and the high channel doping increases the depletion capacitance which degrades the speed [66]. As a result, multi-gate devices are highly recommended for better gate electrostatic control and SCE immunity. Therefore, FIN-typed, gate all around, nano-sheet or nanowire structures have attracted much interest [69], [70]. Among the different multi-gate technologies, FinFETs are considered promising for device and circuit performance as they account for the elimination of SCEs. The improved electrostatic control provided by FinFETs, results to steeper subthreshold slope which in turn increases the transistor's performance at low operating voltage conditions [3], [66], [70]. Of course, despite the superior performance of FinFETs, the fabrication process of these advanced technologies is more complex compared to planar structures. The 3D shape limits lithography and etching techniques that has led to tapered fin shape for 22 nm node and below, which attracted the interest of many researchers for further study concerning the impact of FIN shape on the device performance [70], [71].

Concerning other technological aspects, FinFETs can be developed on top of both bulk and SOI substrates with the former case requiring more technological steps [72]. A schematic structure on top of SOI and bulk substrates is shown in Figure 3-1a. For higher efficiency in terms of I_{ON}, small fin pitches are recommended so that a higher FIN density is achieved for the same area, which results in a higher total drive current. A schematic of such structure is shown in Figure 3-1b. The minimum pitch size is determined by the acceptable coupling effect between the FINs on device performance [73], [74]. In addition, extensive studies are being held concerning the width of FINs, W_{FIN}. For future technology nodes scaling of W_{FIN} is required for better electrostatic control and limitation of short channel effects [73], [75]. Consequently, it is quite interesting to observe what may be the impact of FinFET technology variations, i.e. number of FINs and W_{FIN}, on LFN.

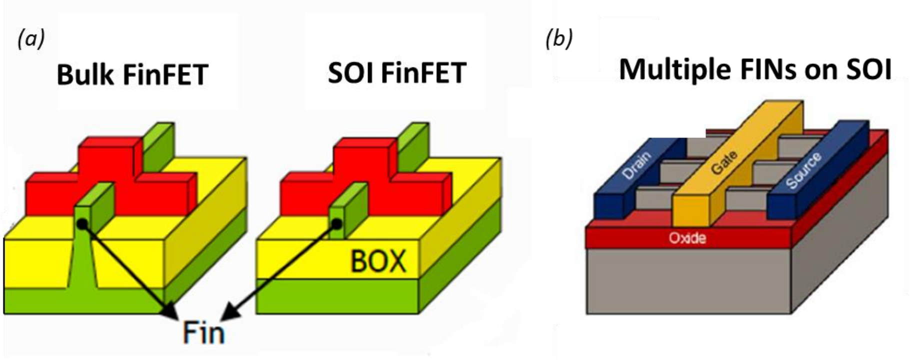

Figure 3-1: (a): FinFET on bulk and SOI substrates [5]*, (b): Schematic of multiple FINs grown on the same active area* [14]

In the frame of LFN performance of advanced technology transistors, we received and measured 3 FinFET technology wafers, fabricated at IMEC-Leuven, thanks to the Horizon 2020 ASCENT EU project (Access to European Nanoelectronics Network -Project no. 654384). More specifically, we studied each wafer incorporated a different sub-10 nm FIN width (7.5, 6, and 4.5 nm) in bulk technology, with FIN pitch around 45 nm and FIN height of around 26 nm. High-k gate dielectric of HfO_2 was used with an equivalent oxide thickness, EOT, of 0.8 nm. Both p- and n-type devices were included in the wafers, but we focused our LFN characterization study on n-type ones. Additional information on the fabrication process can be found elsewhere [76]. Our aim was to compare the LFN performance in terms of different devices parameters, such as the FIN width and number of FINs.

3.2.1. Impact of FIN width

We first performed I_d-V_g measurements for an ensemble of 22 devices in linear region of operation (V_d = 30 mV) for different FIN width cases. The channel length was equal to L_{ch}= 28 nm in all cases, whereas the effective channel width was different for each set, since it can be considered as: W_{eff}=W_{FIN}+2H_{FIN}. Finally, the total effective area should be multiplied by the number of FINs which in this case was equal to 4. Figure 3-2 shows the average I_d-V_g curves for the different FIN width values. One can observe that with the reduction of W_{FIN} the access resistance impact on I_{ON} current becomes more significant, as mentioned in [76]. Secondly, the increase of threshold voltage, when going from W_{FIN}= 7.5 nm to 6 nm, can be attributed to quantum effects that confine the carriers in the middle [75], [77]. The non-expected low value of V_t for W_{FIN} = 4.5 nm compared to the other FIN widths could be attributed to the huge threshold voltage variability. However, investigating this effect is out of the scope of this thesis. Here we focus on the LFN behavior and how it might be affected by the W_{FIN}.

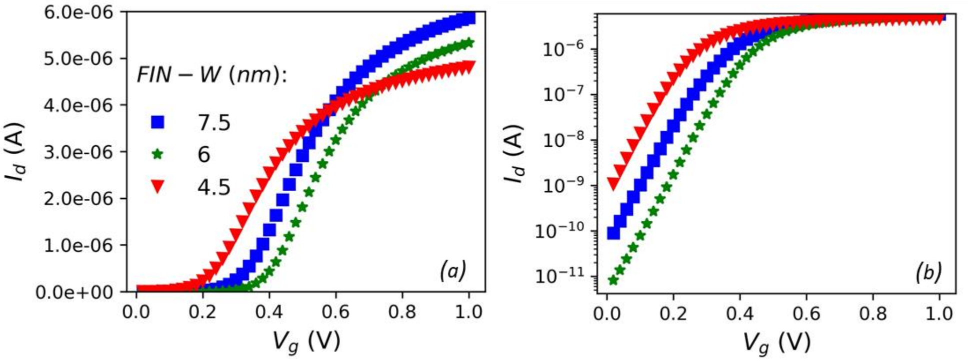

Figure 3-2: Average drain current versus gate voltage characteristics from 22 devices measured at drain voltage V_d = 30 mV for three different values of FIN width. (a): linear scale, (b): logarithmic scale.

After the static measurements, we pursued to LFN characterization. Once the drain current PSDs were measured, we extracted the input-referred gate voltage noise power spectral density, S_{V_g}=$S_{I_d}/{g_m}^2$, for each device of all the three wafers, as well as the average spectrum by taking the mean logarithmic value (from now on referred as mean S_{V_g}), [61], of 22 devices for each FIN width. An example is shown in Figure 3-3.

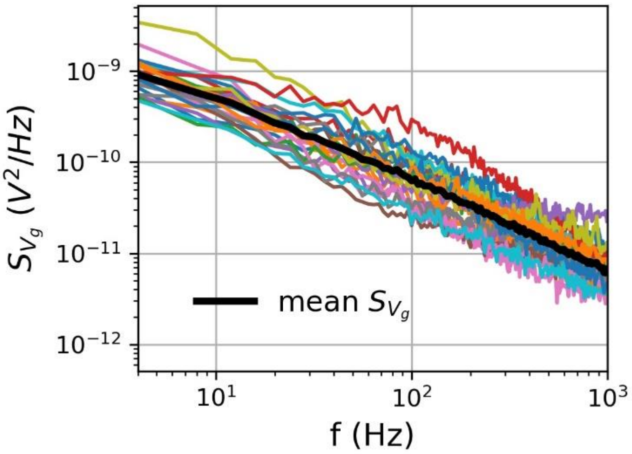

Figure 3-3: Input-referred gate voltage noise versus frequency, for 22 devices with W_{FIN}=6 nm along with the average spectrum. Measurement conditions: V_g = 0.46 V, V_d = 30 mV.

Figure 3-4 shows the average S_{V_g} for each W_{FIN}. We compared the spectra in both sub-V_t and above V_t regions of operation, at the same current level. Other than the fact that the spectra are 1/f-like, it can be observed that the reduction of FIN width from 7.5 to 4.5 nm has no significant impact on LFN level at 10 Hz, with the lowest value of W_{FIN} giving almost three times higher LFN level in the worst case (strong inversion region). Similar behavior with a slight increase of S_{V_g} with the reduction of W_{FIN} has been reported in [78].

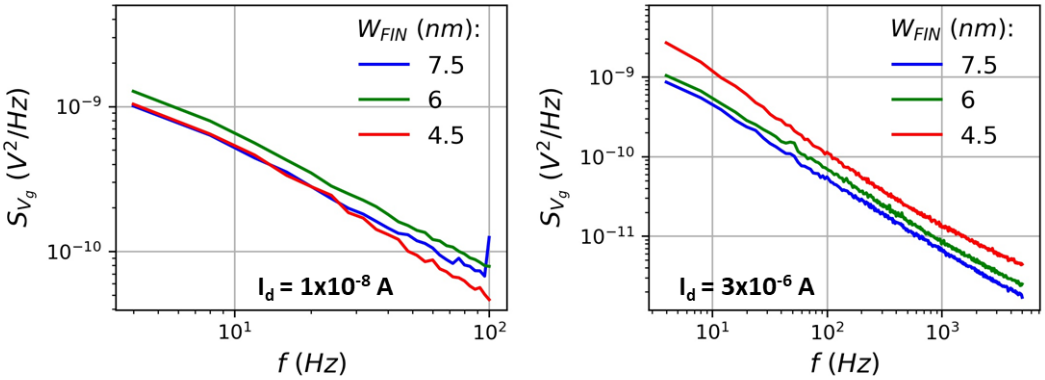

Figure 3-4: Average input-referred gate voltage noise power spectral density for different fin widths in sub-V_t and above V_t regions of operation.

Since the spectra are 1/f-like, we extracted the normalized drain current power spectral density at 10 Hz and we applied the CNF/CMF model, [53], to extract the noise parameters for each case. Figure 3-5a shows the normalized drain current power spectral density for all current regions, revealing a very well agreement with the CNF/CMF model for every FIN width case. This ensures that the resulting LFN is due to trapping and release of carriers which also induces changes to carrier's mobility. As a result of the fitting model the noise parameters were extracted, and shown in Figure 3-5b. No significant difference of W_{FIN} on trap density can be observed, with an average value of $6x10^{17}$ $eV^{-1}cm^{-3}$ for three wafers, very close to the state-of-the-art 28 nm Bulk Si CMOS technology [79]. On the other hand, low values of the CMF factor Ω were observed with a small reduction when going to narrower FINs. This contradicts the results shown in [80] where the opposite behavior of Ω with W_{FIN} was observed, attributed to the increased remote Coulomb scattering due to shorter carrier/interface mean distances. In our case, the slight decrease (almost negligible) of Ω with W_{fin} can be assumed to be related to the access resistance issues, which are more enhanced in the low W_{FIN} values case, and as presented in [81], lead to an underestimation in the extraction of Ω.

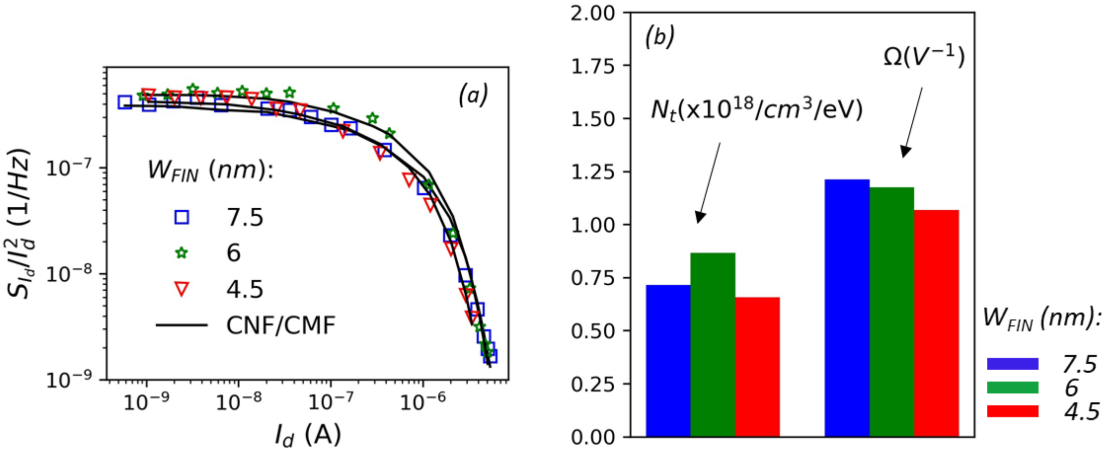

Figure 3-5: (a): Normalized drain current noise versus drain current for different FIN widths along with the CNF/CMF fitting model. (b): Extracted volumetric trap density, N_t, and CMF coefficient, Ω, for each case.

3.2.2. Impact of number of FINs

We followed exactly the same procedure described in $3.2.1, but this time comparing devices with different number of FINs (N_{FIN} = 6,10, and 22) with W_{FIN} = 6 nm, and channel length L_{ch} = 28 nm. The average I_d-V_g curve of 10 devices for each value of N_{FIN} is shown in Figure 3-6. Almost no change of V_t is observed (around 0.4 V), proving no significant static variability issues between FINs and, as expected, higher I_{ON} current is achieved for N_{FIN}=22 due to the contribution of more channels in parallel. In addition, Figure 3-7 shows the normalized with N_{FIN} drain current for the three cases. Apart from almost negligible variations on the I_{ON} current, it is confirmed that the static performance of the three devices, is only affected by the number of FINs.

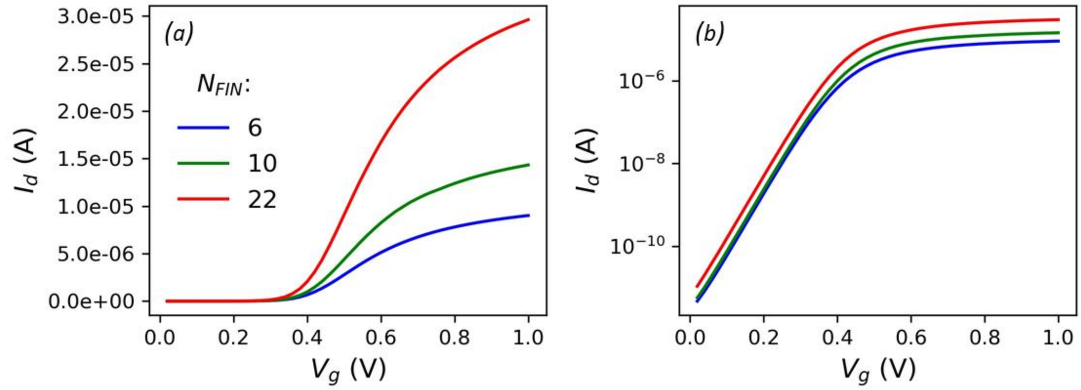

Figure 3-6: Average drain current versus gate voltage characteristics from 10 devices measured at drain voltage V_d = 30 mV for three different numbers of FINs. (a): linear scale, (b): logarithmic scale.

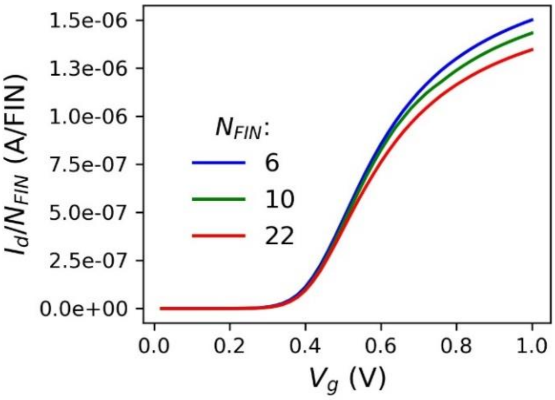

Figure 3-7: Normalized with N_{FIN} drain current versus gate voltage curves at V_d = 30 mV.

LFN measurements were followed for various gate voltage values and in linear region of operation. The S_{V_g} spectra, along with the average one, are shown in Figure 3-8. Figure 3-9 depicts the input-referred gate voltage power spectral density in two regions of operation (below and above V_t). One can observe that there is an increase of S_{V_g} when reducing the number of FINs in the Sub-V_t case. This is probably due to the fact that the effective area becomes larger with the increase of N_{FIN}, which according to the CNF model should cause a reduction of the LFN level. Concerning the above V_t region (Figure 3-9b), the devices with

N_{FIN}=22 continue showing the lowest average LFN level, whereas the remaining N_{FIN} cases show similar values of S_{V_g} which can be due to the differences in the CMF coefficient that contributes to the LFN level in the strong inversion region.

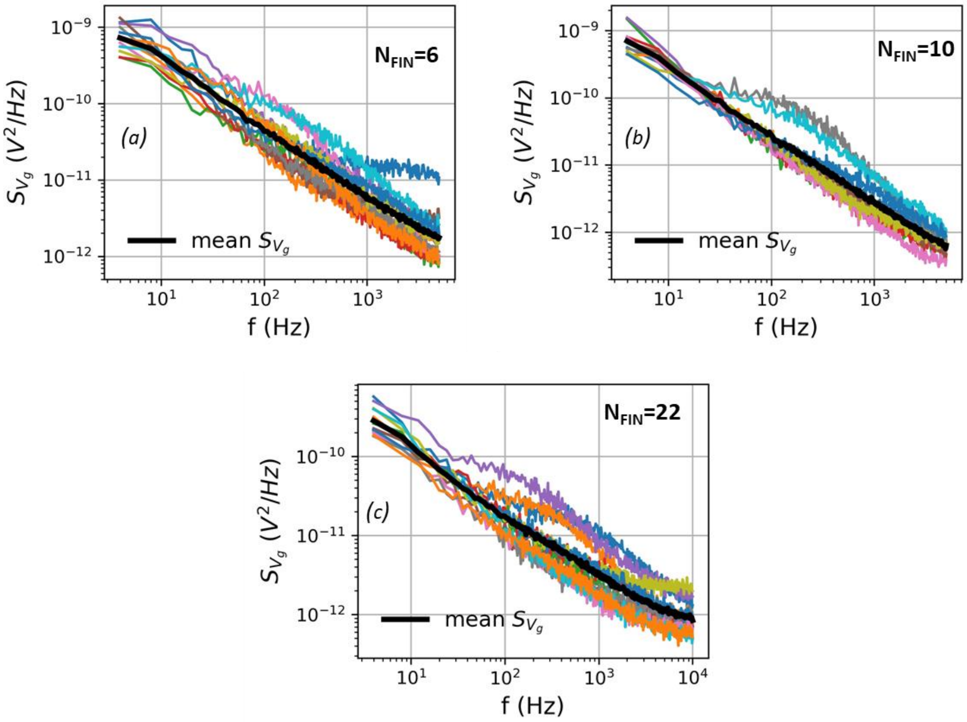

Figure 3-8: Input-referred gate voltage noise versus frequency, for 10 devices, biased under V_g = 0.58 V and V_d = 30 mV.

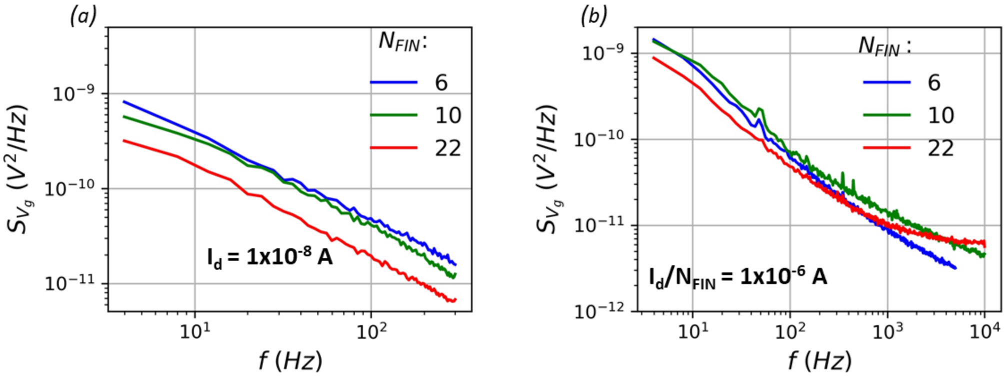

Figure 3-9: Average input-referred gate voltage noise power spectral density for different number of FINs in (a): sub-V_t at the same I_d=1x10^{-8} A and (b): above V_t region of operation at the same I_d/N_{FIN}=1x10^{-6} A.

Since the spectra have a 1/f behavior, we applied the CNF/CMF model to extract N_t and Ω. In Figure 3-10a, the normalized drain current extracted at 16 Hz is plotted versus drain current for all cases, along with the application of the CNF/CMF fitting model. The fit of the experimental data with the CNF/CMF model confirms that the carrier number with correlated mobility fluctuations prevail the 1/f noise. Finally, Figure 3-10b shows the extracted N_t and Ω for the different cases. Similar values of N_t for the three cases were obtained which implies same quality of the oxide for all the cases. Concerning the CMF factor Ω, the extracted values are similar to the ones reported in bibliography, [30], with the device of N_{FIN}=10 showing the higher value. We believe that the contact resistance issues we faced when measuring these wafers may affected the extracted Ω values.

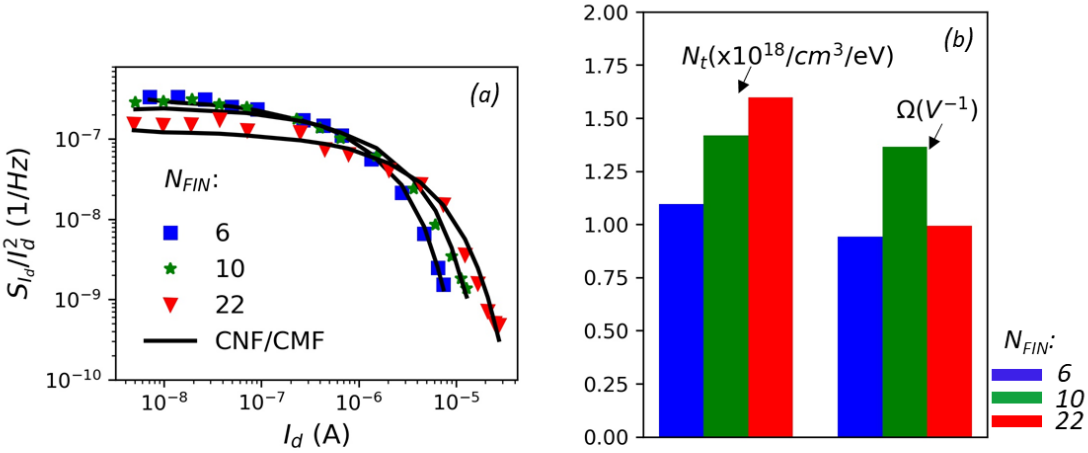

Figure 3-10: (a): Normalized drain current noise versus drain current for different number of FINs along with the CNF/CMF fitting model. (b): Extracted volumetric trap density per eV, N_t, and CMF coefficient, Ω, for each case.

3.3. LT SOI FETs for 3D sequential applications

Under the demand of “More Moore” and “More than Moore” technology roadmaps alternative technologies beyond silicon CMOS are being explored [82]. 3D integration with vertical stacking of single devices or logic circuits, whose structure is shown in Figure 3-11 and Figure 3-12, allows the increase of integration density without the requirement of further reduction of the device dimensions. Its potential for reduction of variability and cost as well as delay, thanks to the small distance between the stacked layers, makes it a perfect candidate for “More than Moore” applications [11], [83]. More specifically, in the case of 3D-sequential integration (3DSI) very accurate alignment of the different levels can be achieved as it only depends on the lithography stepper performance [18], [84]. The most critical challenge of 3DSI process though, is the low thermal budget (TB), needed to avoid the degradation of the bottom tier devices during the top tier fabrication. It has been reported than in order for 3DSI applications with metal lines between the stacked levels to be achieved, the thermal budget of the top transistor should be reduced to 500 °C, as this temperature can preserve the safe operation of the bottom layer [85]. This concerns mostly the dopant activation process which is usually done at higher temperature [86] as well as the oxide quality, as the high temperature spike can help the defect annealing.

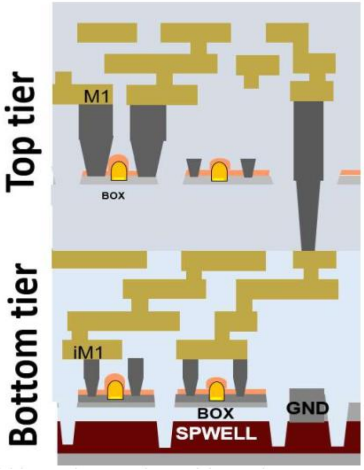

Figure 3-11: 3D monolithic stack overview with two interconnected tiers [67].

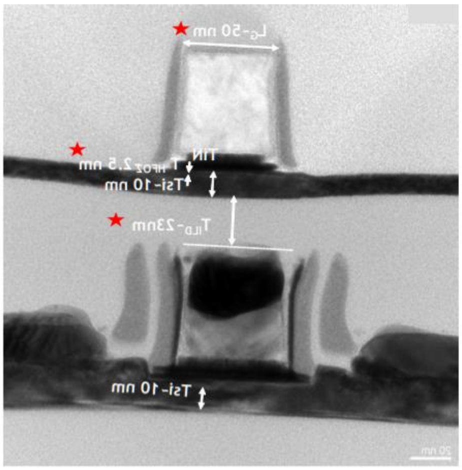

Figure 3-12: TEM of stacked transistors [85].

3.3.1. LT Junctionless SOI MOSFETs for analog applications

The need for aggressively scaled down transistors for performance purposes has caused difficulties in the fabrication process and conventional architectures, such as the abrupt changes of the doping level from source to drain, are difficult to be implemented. The Junctionless MOSFETs, first demonstrated by J. -P. Colinge [87], and are considered promising for “more than Moore” applications. In this type of devices, no highly doped regions are present but instead, there is a uniform doping from source to drain side. In order for a high ON current to be achieved, the channel doping concentration is on the range of 10^{19} cm^{-3}, and for depletion condition the work function of the metal is selected so, as full depletion to be achieved in the off-state. For this condition, Tri-Gate structures with small channel width is required, hence usually a single nanowire is used to form the channel. Figure 3-13 shows a schematic of a junctionless Tri-Gate transistor along with its n-type cross section.

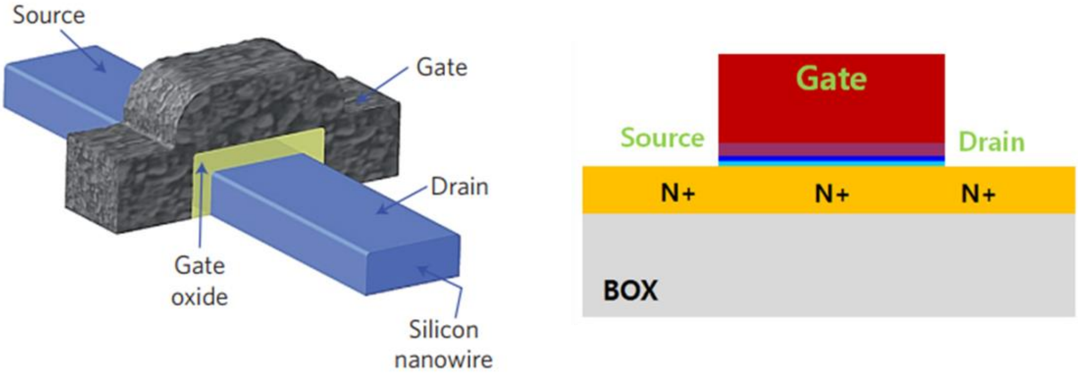

Figure 3-13: (left): schematic of an n-channel Tri-Gate junctionless nanowire transistor [87]*, (right): Cross-section of junctionless transistor* [88].

The junctionless devices can minimize short channel effects, especially DIBL due to the elimination of junctions, so they are supposed to be promising for short channel devices [87]. Although they are considered to achieve lower variability of effective gate length compared to inversion mode transistors, mobility degradation phenomena have been reported due to high channel doping [89], [90]. In comparison with classical inversion mode devices, similar static and LFN performance has been reported in [87], [88]. The simplicity of the structure with no complex fabrication steps as well as the uniform device doping, which does not require high temperature procedures for the formation of source and drain regions, makes junctionless a promising candidate for 3DSI applications [67]. As a result, many works have been published in which the dopant activation is achieved by laser annealing [67], or by solid phase epitaxy regrowth (SPER) [18]. Due to the particularity of the fabrication procedure, and the promising combination of 3DSI and junctionless approach, the proper electrical characterization of low temperature (LT) Junctionless MOSFETs is of high importance. In this part we present a detailed LFN characterization of LT TriGate Junctionless devices.

Concerning the experimental procedure, we characterized junctionless TriGate transistors fabricated by CEA-LETI which underwent Solid Phase Epitaxy Regrowth (SPER) at 525°C for 30 min for the formulation of junctions under the spacers, a method suitable for 3DSI process [86]. Uniform doping was achieved, equal to $8x10^{18}$ cm^{-3}, with HfO_2/TiN/Poly-Si gate stack and equivalent oxide thickness of 1 nm [91]. For comparison purposes, we characterized also a Junctionless Accumulation Mode transistor (JAM) which underwent high temperature annealing (1050ºC) as well as a classical inversion mode transistor, which we name “IM”. All the characterized devices are n-type with channel thickness of 11 nm fabricated on 300 mm SOI wafers.

Firstly, we focused on JL devices with different channel lengths (L_{ch} = 0.1, 0.2, and 1 µm). In order to minimize the variability effects on our LFN study, we measured 31 devices of each length and we extracted an average I_d-V_g curve in the linear region of operation, V_d = 30 mV. The static characteristics are shown in Figure 3-14. The V_t roll-off in the smaller lengths is obvious, as well as the huge degradation I_{ON} due to the impact of access resistance in the strong inversion region resulted from the LT process. The average spectrum, extracted by taking the mean logarithmic values of S_{I_d}, for various frequencies and all the channel lengths and is shown in Figure 3-15. In the subthreshold region the frequency bandwidth is limited by the measurement system due to the low drain current values that dictate the use of a high current-to-voltage gain. As expected, S_{I_d} is lower for the 1 µm channel length, due to its larger device area. Very clear 1/f-like behavior of the spectra above 10 Hz is exhibited which allows the application of the CNF/CMF model [53] for the extraction of noise parameters.

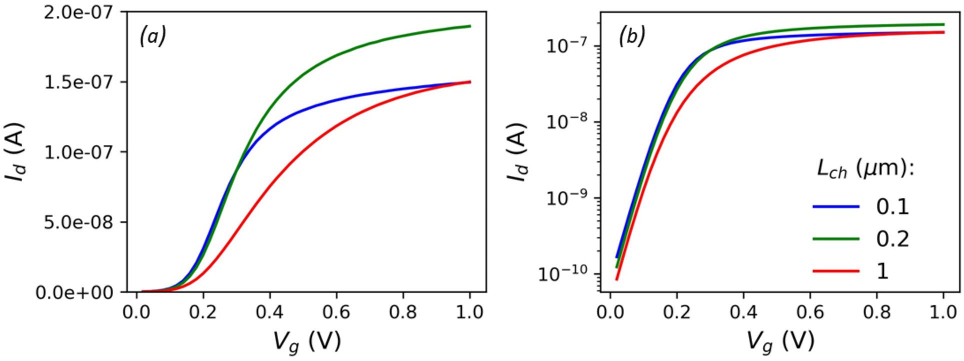

Figure 3-14: Average drain current versus gate voltage of 31 devices measured in linear region of operation (V_d = 30 mV) in both linear and logarithmic scale for different channel lengths.

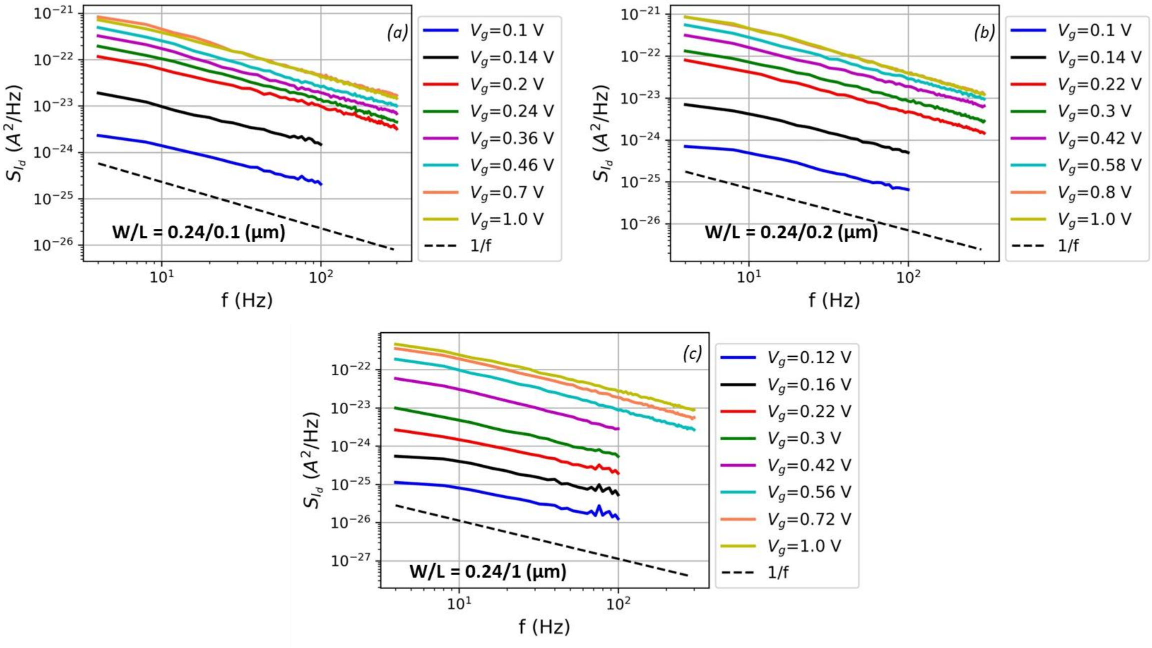

Figure 3-15: Average drain current power spectral density of 31 devices versus frequency for NMOS LT Junctionless, (a): W/L=0.24/0.1 µm, (b): W/L=0.24/0.2 µm, (c): W/L=0.24/1 µm.

The average normalized drain current spectrum extracted at 10 Hz versus drain current is shown in Figure 3-16a for all the measured channel lengths. The access resistance impact on LFN is obvious in the strong inversion region which can be attributed to the non-optimized source and drain regions due to the LT process [91]. When the impact of access resistance on LFN is significant, the measured spectra can be considered as a sum of the intrinsic channel noise and the noise from the access resistance as it has already been presented in [53], [92], [93] and can be given by eq. *(3-1)*. As a result, if the CNF/CMF model is applied directly to the affected by access resistance noise, the extracted parameters might be overestimated or underestimated especially in the case of Ω, which is extracted in the strong inversion region. Based on the above, we first fitted the affected LFN part by the access resistance (linear part of $S_{I_d}/{I_d}^2$ with I_d), so as the $S_{R_{SD}}$ to be extracted and then, using eq. *(3-1)*, the intrinsic noise, free of access resistance effects, can be plotted as shown in Figure 3-16b. This procedure is depicted in Figure 3-16(a) and (b), where we show the normalized noise before and after the elimination of access resistance impact. Figure 3-16(c) also demonstrates the extracted access resistance power spectral density for the three cases. As it can be seen, no correlation of $S_{R_{SD}}$ with L_{ch} can be concluded, and this is might due to the fact that higher number of devices should be measured for the short channel cases. The high variability in the short channel devices probably required more measurements in order to be eliminated. In addition, the fitting points for $S_{R_{SD}}$, are quite fewer in short channel compared with the 1 µm case. Finally, since $S_{R_{SD}}$ is stemming only from the S/D regions, no direct scaling with L_{ch} is expected.

$$(S_{I_d}/{I_d}^2)_{measured} = (S_{I_d}/{I_d}^2)_{channel} + (I_d/V_d)^2 S_{R_{SD}} \qquad \text{(3-1)}$$

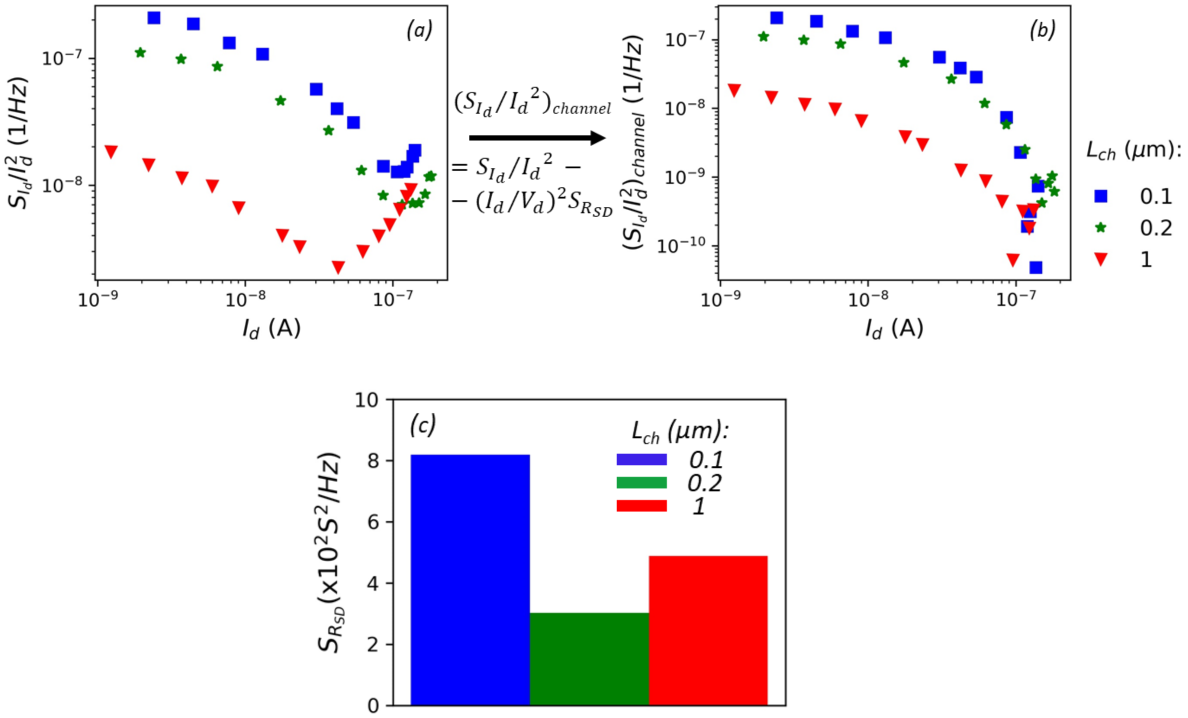

Figure 3-16: (a): Measured normalized drain current noise versus drain current for different channel lengths, (b): Intrinsic normalized drain current noise versus drain current after the elimination of access resistance impact for different channel lengths, (c): Access resistance power spectral density for the different channel length values.

Figure 3-17 shows the application of the CNF/CMF model on the intrinsic channel noise proving that the carrier number fluctuation effect, related to trapping/detrapping of carriers in slow oxide traps, is the main contributor to LFN in JL MOSFETs as already reported in [88]. The extracted noise parameters N_t and Ω are shown in Figure 3-18. No significant variation of N_t with channel length is shown with an average value of 6x10^{17} eV^{-1}cm^{-3}, which shows similar oxide quality for all the channel lengths. This value is also very close to the state of the art of high-k-metal-gate CMOS technologies indicating that the LT process did not degrade the oxide quality [79]. Concerning the extracted CMF factor Ω, the maximum value is around 2.5 V^{-1} for the longer channel and its value is reduced with the reduction of channel length. The impact of channel length on the Ω factor will be analysed in detail in Chapter 5. As reported in [81], [94] the CNF/CMF application in short channel devices with increased access resistance might result in the underestimation of Ω, so this can explain the attenuation of extracted Ω with the reduction of L_{ch}.

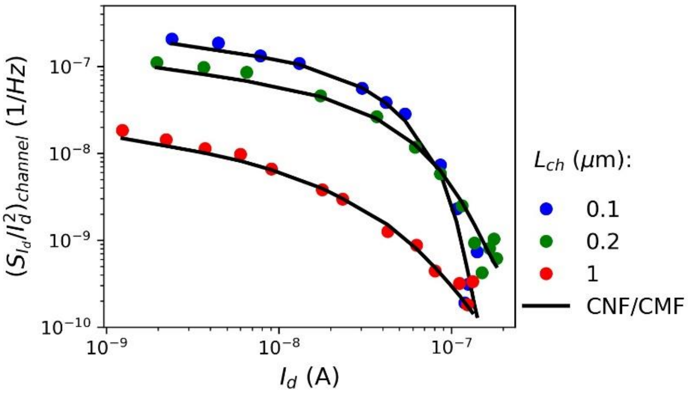

Figure 3-17: Intrinsic normalized drain current noise versus drain current along with the CNF/CMF model for the three channel length cases.

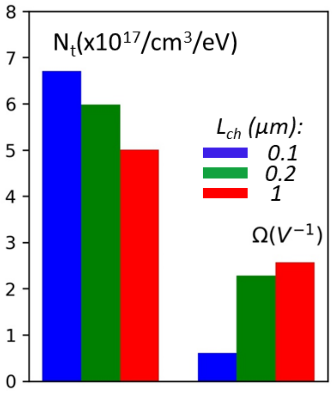

Figure 3-18: Extracted N_t and Ω parameters for all the channel length cases.

For the LFN comparison of the different technologies, so as to observe how the LT process affected the noise level and parameters, we pursued to static and LFN measurements of 31 JAM and IM devices with W/L = 0.24/1 μm in the linear region of operation (V_d =30 mV). Then, we extracted the average drain current and spectrum as described for the JL devices so as to have a good and reliable comparison of the three technologies. For each average I_d-V_g curve we extracted V_t using the Y-function method [95], depicted in Table 3-I and Figure 3-19 shows the drain current versus gate voltage overdrive for the different technologies in logarithmic scale. As it can be seen, JAM and IM FETs show no significant difference in terms of I_{ON} and I_{OFF}, with a slightly better SS given by the IM transistor. Concerning the JL FET, its performance is degraded due to higher access resistance and non-optimized junctions related to the LT process.

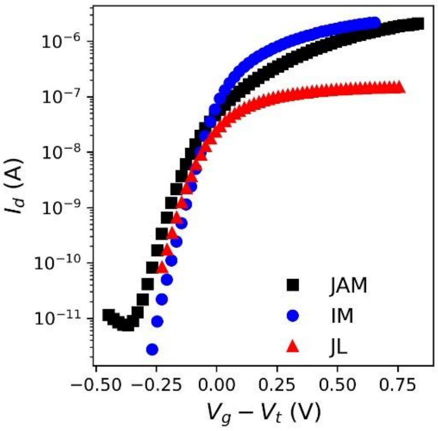

Figure 3-19: Average measured drain current versus gate voltage overdrive for the different technologies.

Table 3-I

Extracted V_t using Y-function for the different technologies. W/L = 0.24/1 µm.

	V_t (V)
JAM	0.167
IM	0.347
JL	0.245

For the noise characterization, we performed LFN measurements for various V_g values and we extracted the input referred-gate voltage noise S_{V_g} for all cases. Since we observed that the JL FET suffered from significant lower performance in the strong inversion region, we first compared the noise level at the same current value (5×10^{-9} A) in the subthreshold region of operation. The result is shown in Figure 3-20, where it can be seen that there is no difference on the noise level between the different technologies with all of them having a pure 1/f-like behavior. The same behavior can be also seen when comparing S_{V_g} at the same gate voltage overdrive (V_g-V_t=0 V), shown in Figure 3-21.

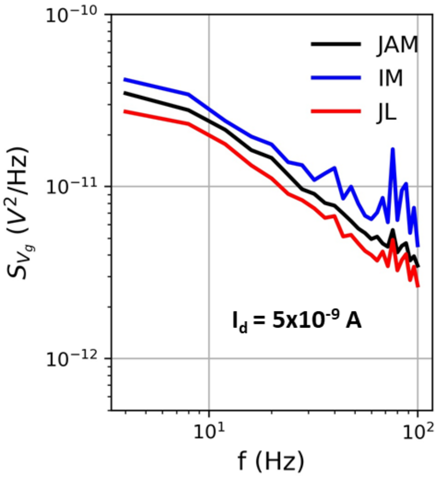

Figure 3-20: Input-referred gate voltage power spectral density versus frequency for the different technologies at the same current level, I_d=5x10^{-9} A.

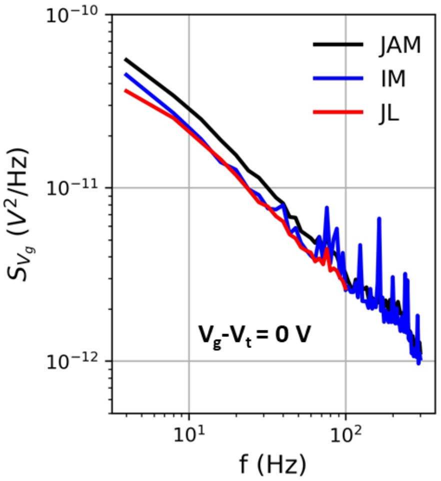

Figure 3-21: Input-referred gate voltage power spectral density versus frequency for the different technologies at the same gate voltage overdrive, V_g-V_t=0 V.

After observing the 1/f spectra in all cases we applied the CNF/CMF model for the extraction of N_t so as to have an idea of the oxide quality for the different fabrication steps. Figure 3-22, shows the CNF/CMF application on the experimental normalized noise and Figure 3-23 shows the extracted volumetric trap density N_t as well as the CMF coefficient Ω. All cases gave very close results of N_t proving that the different processes and technologies did not degrade the oxide quality in terms of noise, with the LT JL FET giving the lowest N_t. Therefore, the noise level differences presented in Figure 3-22 are only stemming from variations in g_m/I_d, which are due to the doping levels and mode of operation. Concerning the extracted Ω values, the IM FET gives the highest value. This can be due to the channel formation differences between JAM/JL and IM, as IM FETs form surface inversion layers [89] and thus the trap scattering effects may be enhanced.

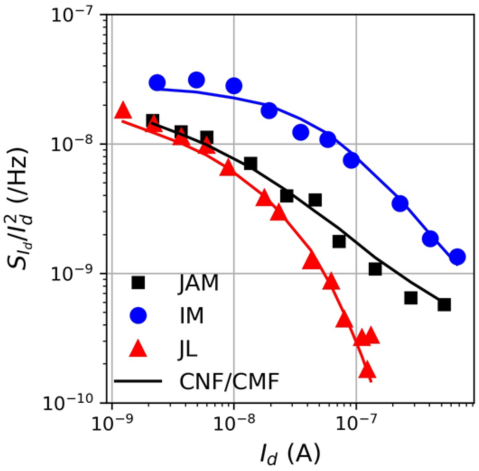

Figure 3-22: Normalized drain current power spectral density versus drain current along with the CNF/CMF model for the different technologies.

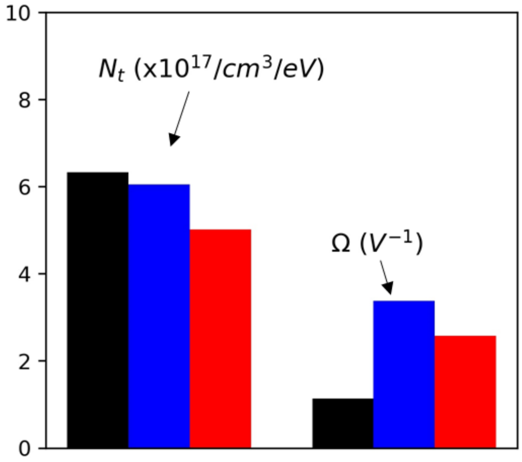

Figure 3-23: Extracted N_t and Ω from the CNF/CMF application for the different technologies.

3.3.2. LT high voltage analog MOSFET

Apart from the LFN performance study of LT advanced technologies, like Junctionless MOSFETs, it is also interesting to see how conventional technologies are affected under the low thermal budget (TB) process for 3DSI applications. For this reason, LT SOI MOSFETs with channel thickness of 30 nm, lightly p-type doped silicon, around 1x10^{15} cm^{-3}, with thick (EOT ≈ 6 nm) gate stack of SiO_2/TiN/Poly-Si were fabricated under different oxidization conditions, for possible top-tier analog circuit applications (V_{dd} = 2.5 V) in 3DSI technology, by CEA-LETI

[96]. Four splits of LT oxides have been compared, in terms of LFN, having as reference a high temperature oxide (HTO) FET. The different oxide splits are the following:

1. 6 nm thermal oxide at 800°C, named: LTO 800°C
2. 1.6 nm plasma oxidation in Pl-O_2 + Plasma Enhanced Atomic Layer Deposition (PEALD), named: Pl-O_2+ PEALD
3. 6 nm plasma oxidation in O_2/H_2, named: Pl-O_2/H_2 at 450°C
4. 1.6 nm plasma oxidation in Pl-O_2 + PEALD with post deposition treatments of plasma O_2 densification at 450°C, named: Pl-O_2+ PEALD+ 450°C Pl-O_2

In addition, for the LT devices, SPER at 500°C for 30 min was used for junction activation whereas the HTO reference underwent conventional HT anneals. All the oxide splits, both p- and n-type devices, were electrically characterized using LFN as a tool for defect characterization of the different oxide process. Figure 3-24 shows the measured I_d-V_g characteristics in linear region of operation (V_d = ±30 mV) in linear and logarithmic scale for all the oxide splits and transistor polarities.

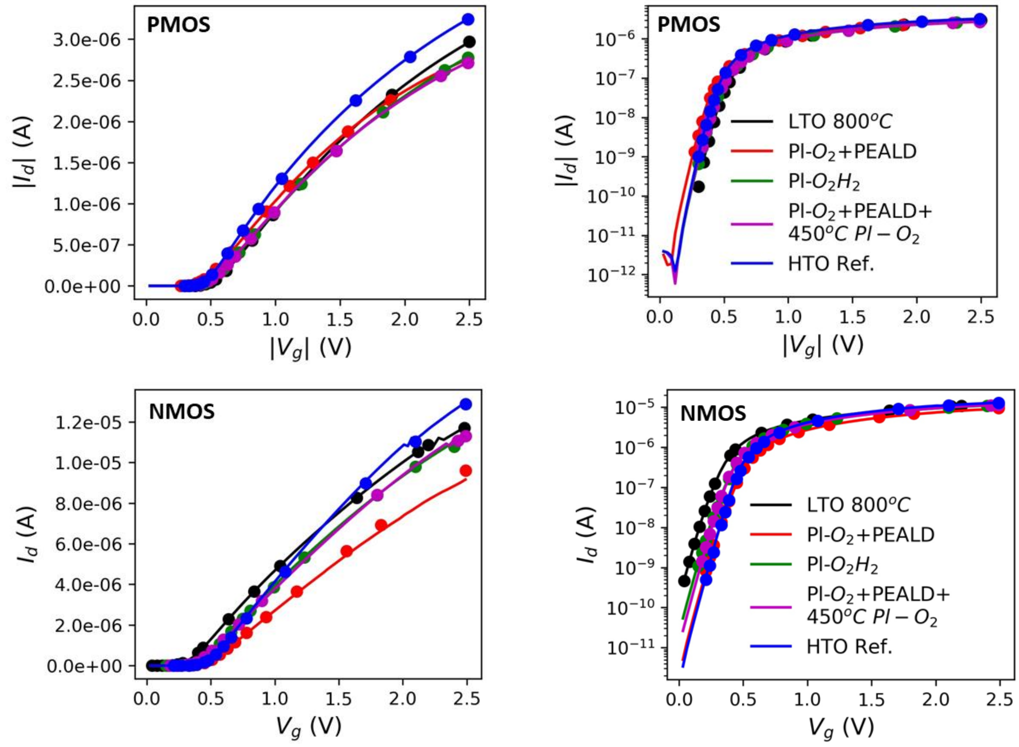

Figure 3-24: Measured drain current versus gate voltage in linear (left) and logarithmic scale (right), for all the wafer splits and for PMOS (top) and NMOS (bottom) devices. Symbols imply slow I_d-V_g measurement whereas solid lines fast ones.

We chose to compare large oxide area devices, W/L=2/2 µm, so that variability effects are minimized and LFN spectra to be closer to the 1/f behavior due to the high number and uniformity of traps. No significant V_t shift has been observed for the PMOS devices compared to the NMOS ones. In addition, higher I_{ON} current is achieved in the HTO reference wafer compared to the LT ones. Also, we performed I_d-V_g measurements when the gate bias is swept up at a different pace. The lines in Figure 3-24 correspond to a typical integration time, whereas the dots correspond to a sweep of V_g at a quite slower pace that could be considered "quasi static". The latter pace is applied for the DC current level stabilization when noise measurements are performed. No difference between the slow and fast I_d-V_g curves is observed, which implies good quality of the oxide/channel interface.

For the evaluation of the different splits, the drain current spectral density was measured for different gate voltage values. Figure 3-25 shows the normalized PSD extracted at 10 Hz for all the oxide splits and for both p- and n-type devices. A much lower, around one order of magnitude, LFN level is observed for the HTO reference for both PMOS and NMOS whereas all the LT wafers demonstrate almost the same LFN level, with the NMOS devices exhibiting slightly lower values. This is an indication that it is the LT process that has a bigger impact on the LFN level rather than the different gate stack combination.

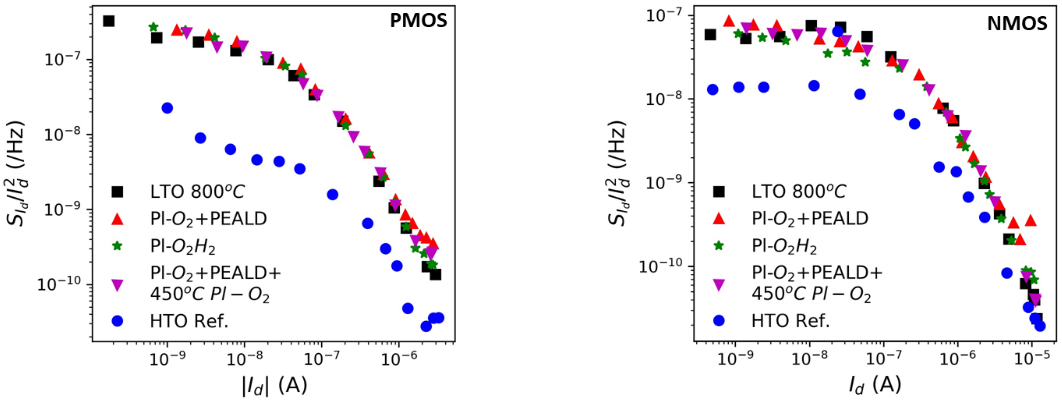

Figure 3-25: Normalized measured drain current noise at 10 Hz versus drain current for PMOS (left) and NMOS (right) devices and for different wafer splits.

To further evaluate the different wafers in terms of trap density and CMF factor, we first need to verify whether all these points correspond to 1/f-like noise. Figure 3-26 shows the normalized spectra for all the wafers at the same drain current level in both sub-threshold and above threshold regions for the PMOS devices. Similar behavior was also observed for the NMOS. As it can be seen, despite the large oxide area, the 1/f like behavior is only present for the HTO reference wafer, whereas the LT splits exhibit both 1/f and Lorentzian-like spectra, with the latter of becoming dominant when the devices are biased below threshold.

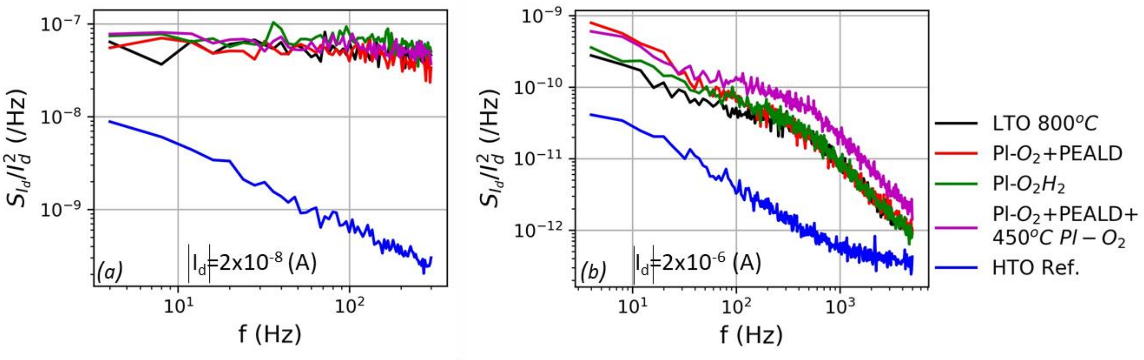

Figure 3-26: Normalized drain current noise spectra for sub-threshold (a) and strong inversion (b) regions in the case of PMOS devices and for different wafer splits.

Since in this Chapter we focus on the flicker noise part of LFN, the Lorentzian spectrum behavior will be analysed in detail in the next Chapter. Concerning the flicker part, the 1/f-like dependence of the spectrum in strong inversion, as it is shown in Figure 3-26 (right), allows the application of the CNF/CMF model only for gate voltage value above V_t. A representative example of the CNF/CMF model application is shown in Figure 3-27. As a result, after applying the CNF/CMF model in all the wafers splits for both PMOS and NMOS, the trap density, N_t, and CMF coefficient, Ω, were extracted and are illustrated in Figure 3-28 and Figure 3-29 respectively.

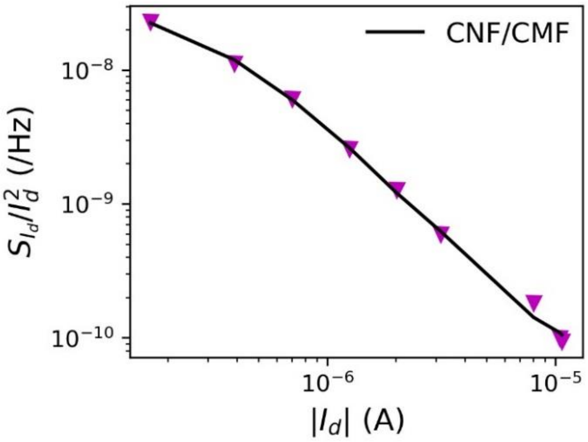

Figure 3-27: Measured normalized drain current spectral density versus drain current at $|V_d|$=30 mV along with the CNF/CMF fit. Wafer split: Pl-O_2+ PEALD+ 450°C Pl-O_2 and W/L = 2/2 μm.

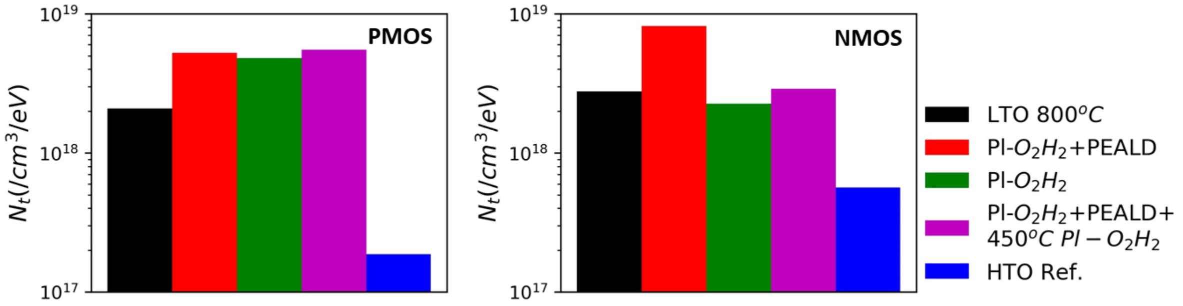

Figure 3-28: Volumetric trap density, N_t, extracted from the CNF/CMF fit for different wafer splits. (left): p- and (right): n-type devices.

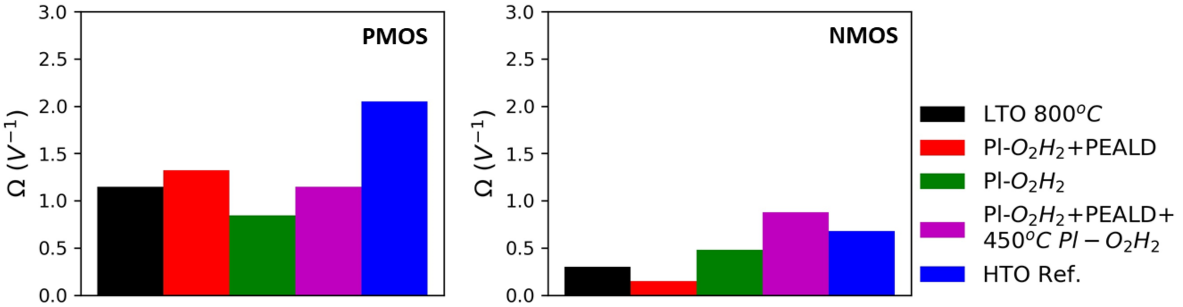

Figure 3-29: CMF factor, Ω, extracted from the CNF/CMF fit for different wafer splits. (left): p- and (right): n-type devices.

As expected from the noise level demonstrated in Figure 3-25, the values of N_t for all the wafer splits are quite elevated, roughly by a factor of 13 for the PMOS and 10 for the NMOS devices. This can be attributed to the fixed oxide charges whose density is not optimized due to the LT annealing processes [7] . The LTO and Pl-O_2/H_2 give the lowest values compared to the remaining splits. Concerning the extracted CMF factor Ω, NMOS devices show lower values for all the wafer splits compared to the PMOS ones. Similar results with higher values of Ω for PMOS devices compared to NMOS have been reported in [26], probably due to additional scattering effects. As for the different splits, one could say that the Pl-O_2/H_2 gives the lowest Ω value for the PMOS devices, whereas for the NMOS it is among the lowest ones along with the LTO and Pl-O2 + PEALD cases.

3.4. Summary

In this Chapter, advanced technologies for future “More Moore” and “More than Moore” applications were evaluated in terms of LFN. By doing this, we prove that LFN should not only be seen as a disturbance of normal device or circuit operation, but also as a tool for the evaluation of critical fabrication steps. Sub-10 nm FIN width FinFETs showed superior performance in terms of LFN as well as the Junctionless MOSFET devices fabricated under the low thermal budget process. Finally, concerning the high voltage analog LT MOSFETs, although the extracted N_t was the highest reported in this chapter, the LTO and Pl-O_2/H_2 cases had the best performance and could be further optimized.

CHAPTER 4

Localization of defective regions in LT SOI MOSFETs using LFN spectroscopy

This Chapter is devoted to Lorentzian-type spectra characterization. The observation of Lorentzian spectra for all the low temperature MOSFET splits, presented in Chapter 3, led us to the conclusion that a defective zone exists inside the devices that is probably neutralized with the high temperature annealing. This is the reason why no Lorentzian spectra were observed in the reference wafer. Detailed LFN measurements under different temperatures and polarization conditions are presented as an effort to detect and identify these defective zones.

4.1. Experimental observation of LFN for different gate stack process

As already mentioned in Chapter 3, in the case of conventional SOI MOSFETs under the LT budget process, we observed a Lorentzian-like PSD (plateau until a characteristic frequency and then $1/f^2$ dependence) for all the wafers (different gate stack splits) except for the reference one, which was the only one fabricated with the typical high temperature process. More specifically, for each wafer we measured and for all the available dies, we saw exactly the same behavior. This observation is depicted in Figure 4-1, where we show the measured normalized drain current PSD for p-type devices at a $|V_g|$ value of around 1 V and $|V_d|$ = 30 mV. The same behavior has been also observed for n-type devices (not shown here). In Figure 4-1, one can easily observe that the characteristic corner frequency of the Lorentzian spectra is approximately the same for all the LT wafers and dies. The minor deviations of the characteristic frequency between the wafers can be attributed to the different static performance, as shown in the I_d-V_g curves in the previous chapter (Figure 3-24), where it is shown that there are some wafer-to-wafer variations mostly in the I_{ON} values, with the reference HT wafer having the highest value. Moreover, the different oxide thickness, between wafers can also explain some variations, whereas the ones observed between different dies of the same wafer can be due to static variability or due to the fact that each LT wafer is splitted to 4 quarters, with each of them having a slight difference in the junction implantation procedure. Nevertheless, despite these small deviations, it can be assumed that all the devices of LT wafers have a group of traps with the same characteristics (energy and position). This group of traps does not exist in the reference HT wafer, as the HT annealing process helps to passivate certain defective zones. This can be also observed from the values of the PSD which are almost 1 decade higher in all the LT wafers compared to the reference one.

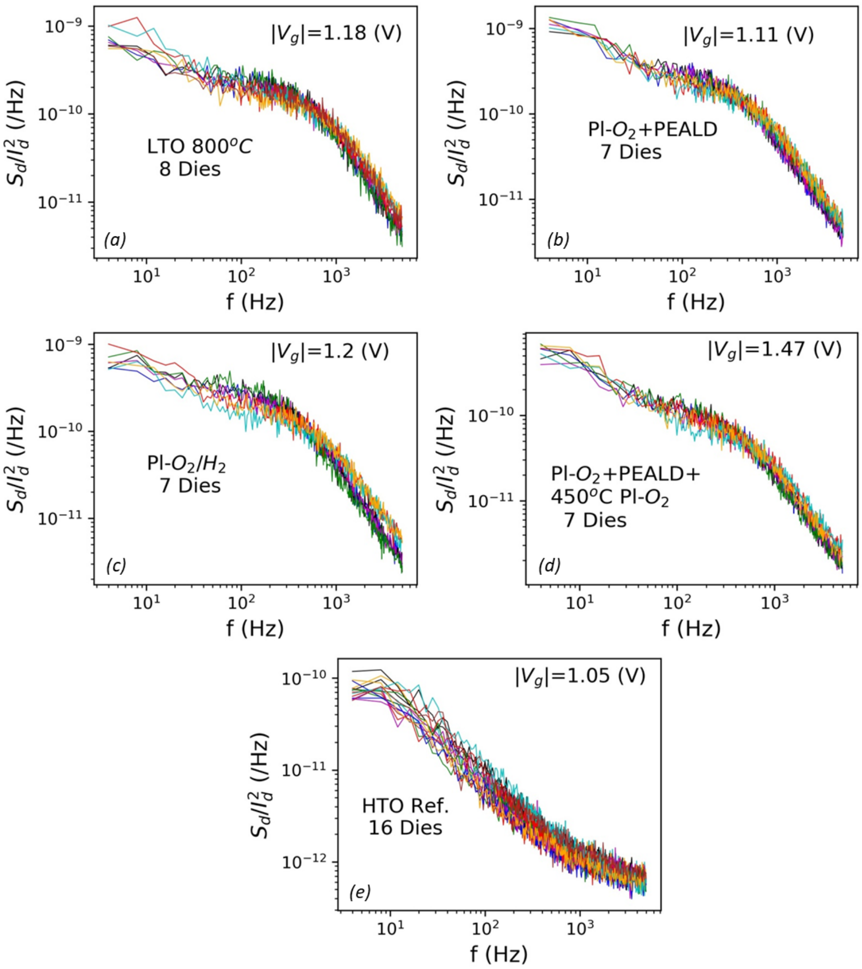

Figure 4-1: Normalized drain current noise spectra above V_t for many dies and different wafers.

An additional observation that enhances our claim regarding the existence of a group of traps, and thus the appearance of generation-recombination (GR) type of noise is that in the time domain measurements, as shown in Figure 4-2, no discrete levels of drain current were present. Therefore, the possibility of RTN noise (related to a single active trap) has been excluded.

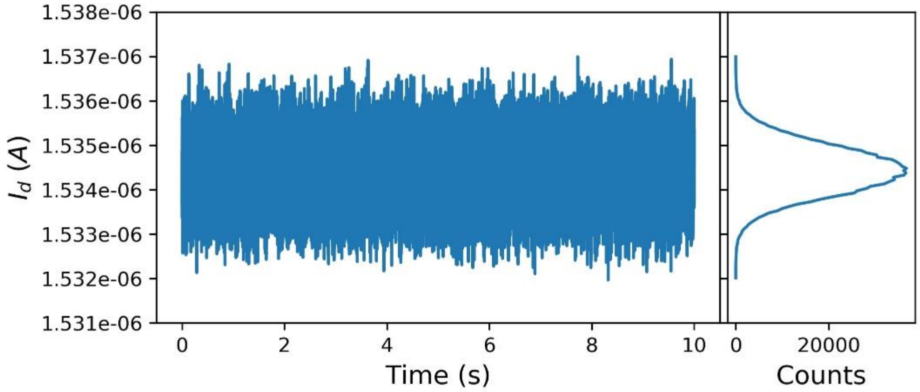

Figure 4-2: Measured drain current time series along with the corresponding histogram for the Pl-O_2+PEALD split at |Vg|=1.23 V and W/L=2/2 μm.

Since we now know that the LT process cannot passivate a specific group of traps, it is important to study where these defects are located inside the device and what is the type of defects, so as to identify the fabrication steps resulted to their appearance and degraded the device quality and performance, a procedure that can contribute to process optimization. In order to do this, we can use Lorentzian spectrum analysis as a tool to localize the defective areas and GR noise spectroscopy to identify the trap's nature. Below, we list all the possible scenarios concerning the position of the traps inside the structure, along with the experimental methods that we will use to validate or exclude them:

1. Inside the source and drain junctions, fabricated under the LT budget process. If this is the case the plateau of the Lorentzian, which is dependent on the device area, should scale only with the device width and not with the channel length, since the source and drain junction area is only affected by the device width.
2. Top or bottom oxide/silicon interface, which might have low quality due to LT annealing. For this study front and back gate mode measurements are useful: if the Lorentzian

spectrum is present (or modulated) only in one mode of operation, one can assume that it is originated from traps in the corresponding oxide [50].

3. Inside the silicon film, especially around 7 nm from the bottom interface, since for the wafers under study we know that in order for a total channel thickness of 30 nm to be achieved, epitaxy growth was utilized for the addition of 23 nm on a film of 7 nm. The probability of this scenario's validity would be enhanced if the Lorentzian is present in both front and back gate mode of operation [50], [97], with similar behavior. Also, another clue that might lead to this scenario's validation is the independence of the characteristic frequency on the gate voltage, which according to the bibliography originates from traps in the depletion region of the film [24].
4. Close to the TiN/oxide interface, as studies have shown that the TiN/SiO_2 stack results to the formation of oxynitride layers, between metal and oxide, due to oxygen scavenging. This process creates charged oxide vacancies inside the oxide that can interact with free carriers [98], [99]. In this scenario, the carriers of the metal may interact with the traps in the top oxide, at a small distance from the TiN/SiO_2 interface. We exclude the possibility of traps at the interface, as in this case the relaxation time value would be too small and thus, we would not be able to measure it.

As shown in Chapter 2, the input-referred gate voltage power spectral density of a Lorentzian spectrum is given by eq. *(4-1)*, [50], where τ is the characteristic time constant of the traps equal to $\tau = (1/\tau_c + 1/\tau_e)^{-1}$, with τ_c and τ_e the average capture and emission time respectively. This characteristic time constant corresponds to the corner frequency of the Lorentzian spectrum, f_c, above which the spectral density is proportional to the inverse square of the frequency. A is the plateau level of the Lorentzian PSD which is related to the number of traps and ω is the corner frequency, ω=2πf.

$$S_{V_g} = A\frac{\tau}{1+\omega^2\tau^2} \tag{4-1}$$

It is clear that the analytical study of the GR noise spectra, can provide valuable information about the location of the traps and their energy level. As a result, detailed LFN measurements under different polarization conditions or temperature are needed. For this reason, we pursued to LFN measurements and we fitted the measured PSDs using eq. *(4-2)*, [100], which is a more generic version of eq. *(4-1)* that also incorporates the 1/f part of the spectrum, so as to observe the dependence of Lorentzian parameters, (A,τ), with various polarization configurations and different temperatures. In addition, since we observed that the Lorentzian parameters are approximately identical for all the LT wafers, we focused on the Lorentzian spectra analysis for a single wafer: the LT 800 ^{o}C one.

$$S_{V_g}\omega = K + A\frac{\tau}{1+\omega^2\tau^2}\omega \tag{4-2}$$

4.2. Extraction of trap properties through noise spectroscopy

Before exploring the dependence of Lorentzian parameters on different channel geometry and polarization conditions, we performed LFN measurements under different temperatures and at fixed bias conditions so as the physical nature of traps to be identified. This is due to the evidence reported in many works where the characteristic time constant of a trap, which result to GR events, depends on the temperature [48]. The method is called GR noise spectroscopy and it can be considered similar to the DLTS techniques [101]. The dependence with temperature enables to construct an Arrhenius diagram based on the eq. *(4-3)* [102], where ΔE is the energy difference of the trap energy level and the appropriate band (E_c for acceptor and E_v for donor like traps), k and h are the Boltzmann and Planck's constant respectively, T the temperature, $\sigma_{n,p}$ the capture cross section of the trap, M_C is the equivalent minima in the conduction band, and m_e* and m_h* the transport effective mass for electrons and holes respectively.

$$\ln(\tau T^2) = \frac{\Delta E}{kT} + \ln\left(\frac{h^3}{4k^2\sigma_{n,p}\sqrt{6\pi^3 M_C {m_e}^{*1/2} {m_h}^{*3/2}}}\right) \tag{4-3}$$

Based on eq. *(4-3)*, one can see that the activation energy ΔE level can be estimated using the slope of $\ln(\tau T^2)$ versus 1/(kT), whereas the traps capture cross section can be derived by the y-axis intercept. Then, the physical nature of the trap can be identified by comparing the extracted parameters with published data in literature. We applied this procedure on the LT 800 ^{o}C wafer for a p-type device with W/L=2/0.45 µm. First of all, we performed I_d-V_g measurements starting from room temperature 298 K to 338 K with a step of 10 K in linear region of operation. To achieve that, we used an ERS-AC3 controller connected to the chuck that allows the temperature ramp-up. The characteristics are shown in Figure 4-3. It can be seen that the static behavior with temperature ramp-up is similar with classical MOSFET devices. As the temperature increases the I_{ON} is decreasing due to higher scattering effects which result to the reduction of mobility. In addition, V_t has an inverse behavior with temperature, and this can be explained by the fact that when temperature is raised, a significant number of carriers gain enough energy to move to the conduction band and contribute to the electrical current. This also explains the increase of I_{OFF} with temperature.

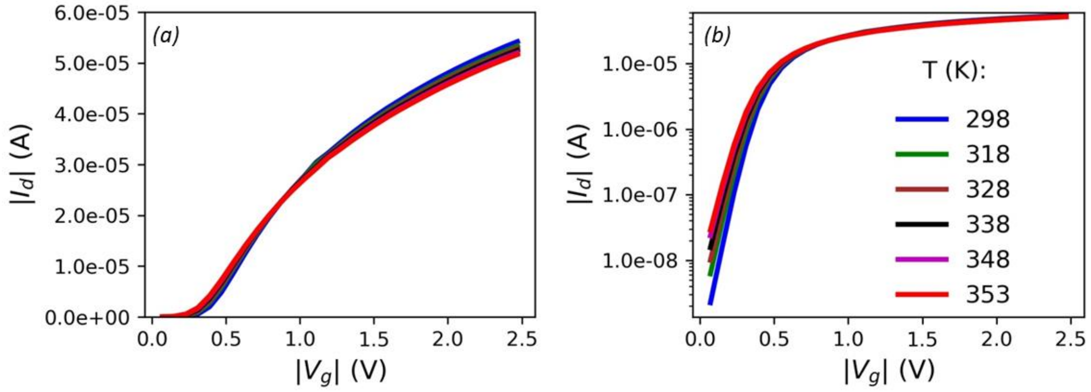

Figure 4-3: Measured I_d-V_g curves in linear region of operation, Vd=-30 mV, for different temperatures in (a): linear, and (b): logarithmic scale.

Concerning the LFN measurements, we chose one gate voltage value that allows the distinct fitting of the Lorentzian spectrum, V_g= -1.15 V, and we kept the temperature step at 10 K so that the measurement does not quickly reach the frequency bandwidth limitation of the system, since the characteristic frequency f_c is increasing with temperature. Figure 4-4 shows the measured normalized drain current PSD multiplied with frequency for the different temperatures. The increase of f_c with temperature can lead to a typical Arrhenius plot once the Lorentzian parameters are extracted for each temperature, using eq. *(4-2).* Figure 4-5, shows a representative example of the fitting process for the room temperature measurement.

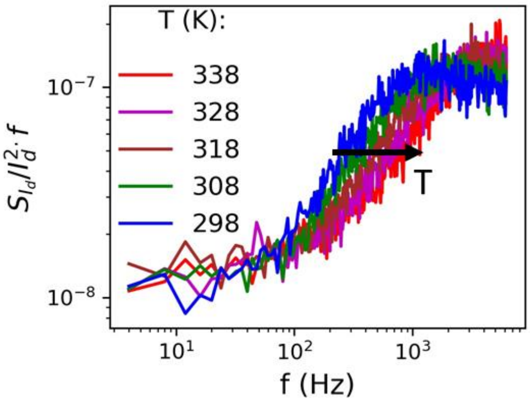

Figure 4-4: Normalized drain current PSD versus frequency at different temperatures and at V_g= -1.15 V and V_d= -30 mV.

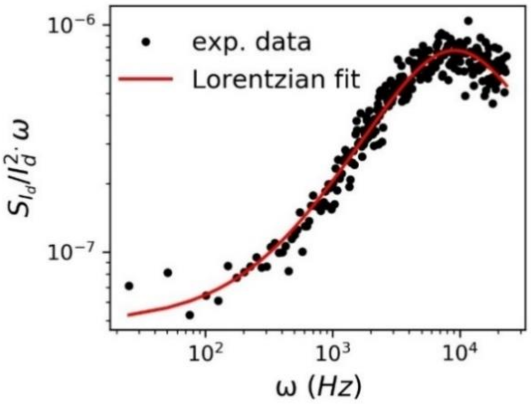

Figure 4-5: Example of measured PSD at room temperature and V_g=-1.15 V along with the fitting of eq. (4-2).

Finally, we used eq. *(4-3)*, to derive the Arrhenius plot, illustrated in Figure 4-6. We considered m_e* and m_h* to be $0.98m_o$ and $0.49m_o$ respectively where m_o is the free electron mass equal to 9.11×10^{-31} kg [7]. ΔE and σ were extracted to be 0.28 eV and 1.21×10^{-18} cm^2 respectively. According to [103], when the σ is below 10^{-16} cm^2, the traps are considered deep level donors for p- and acceptors for n-type devices. In addition, similar values, for both energy and cross section, with the ones that we extracted have been reported in the literature but their nature has not been identified yet. These traps are usually attributed to dry-etching process or implantation techniques [24].

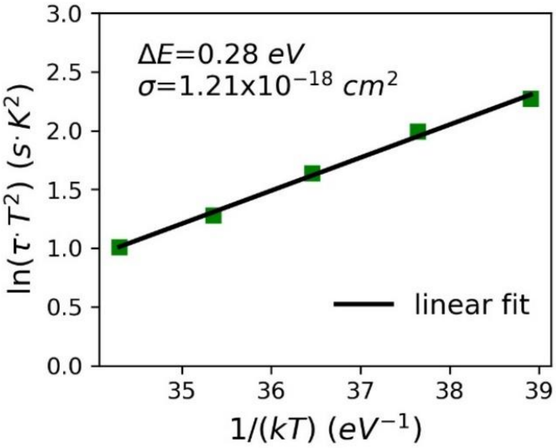

Figure 4-6: Arrhenius plot for p-channel SOI-FET, leading to the identification of traps' characteristics, ΔE and σ.

4.3. Dependence on channel area scaling

As mentioned in \$4.1, in order to study the possibility of traps being in the source and drain junctions, we pursued to LFN measurements for different device dimensions. In Figure 4-7, the measured normalized with area drain current versus V_g is depicted for different dimensions (W/L_{ch}= 5/2, 2/2, 2/0.45, 5/0.15 μm). One can clearly see the V_t roll-off effect as the channel length is becoming shorter, as well as the mobility degradation in the strong inversion region due to the higher impact of source/drain series resistance. Figure 4-8, shows the extracted $S_{V_g} x f$ versus frequency at $|V_g|$= 1 V for the different dimensions.

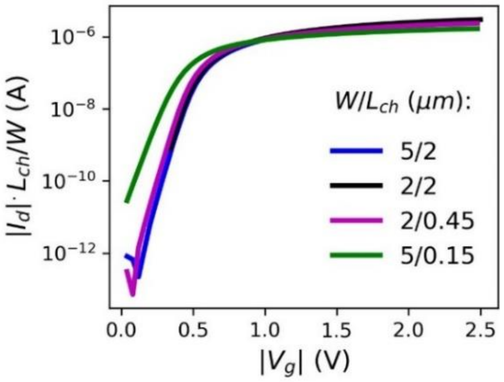

Figure 4-7: Normalized with area drain current versus gate voltage measured at linear region of operation $|V_d|$=30 mV for different device dimensions.

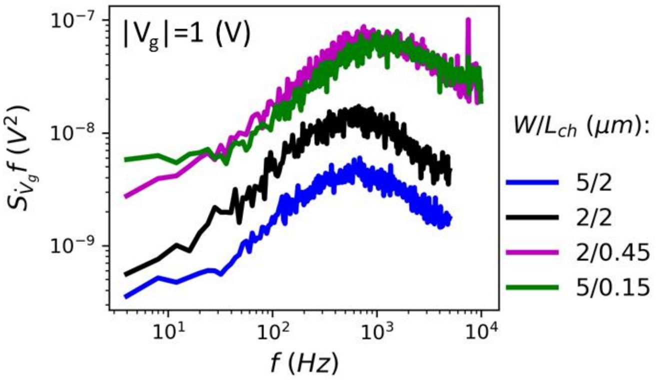

Figure 4-8: Imput-referred gate voltage noise multiplied with frequency versus frequency extracted at $|V_g|$= 1 V and $|V_d|$= 30 mV for different device dimensions.

Since we extracted the S_{V_g} for different gate voltage values, we used eq. *(4-2)* to fit the PSDs and extract the Lorentzian parameters. Figure 4-9 shows the normalized with area plateau A of the Lorentzian PSDs versus gate voltage. It can be seen that the plateau is almost constant with V_g and also independent on the device area. The latter can be also concluded when observing the plot in Figure 4-10, where it is obvious that A scales with both device width and channel length. This finding excludes the scenario #1 (the defective areas being inside the junctions) and implies a uniform distribution of traps across the channel area. Furthermore, Figure 4-11 shows the characteristic time constant of the traps for different gate voltages and dimensions. It can be seen that the shorter devices show lower values of τ, and also in some cases a slight increase of τ with V_g can be observed. In order to check whether this behavior is due to the different geometries or stems from static variability, we measured seven dies of the same geometry (W/L = 2/2 μm) and, for each case, we extracted the relaxation time, τ. Figure 4-12a, shows the I_d-V_g curves for all the different dies, from which it can be seen that apart from slight differences on the I_{ON} current, no significant variability on the static curves exists. On the other hand, Figure 4-12b shows the extracted characteristic time constant, τ, versus V_g for the different dies, where it can be observed that τ varies between 0.1 to 0.35 ms, which is almost the same deviation presented in Figure 4-11. Based on this, the deviations of τ values in Figure 4-11 cannot be attributed to the channel geometry, but to the static variability of the I_d-V_g curves and probably to slight variations of the trap energy level.

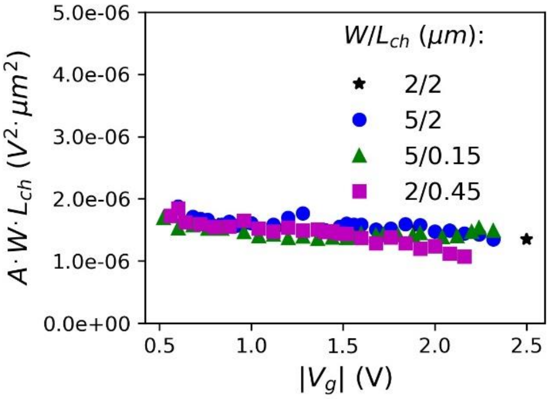

Figure 4-9: Normalized with area Lorentzian amplitude versus gate voltage for different device dimensions.

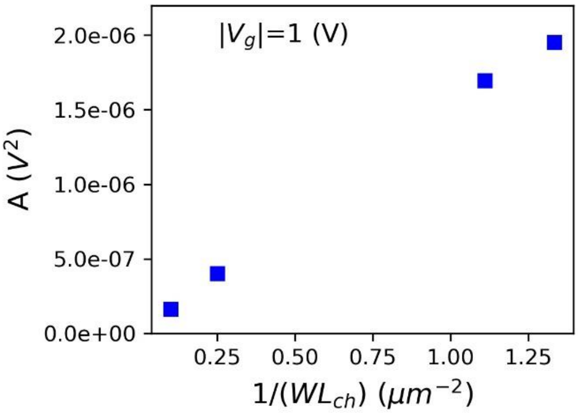

Figure 4-10: Extracted Lorentzian amplitude versus the reverse of device area at $|V_g|$= 1 (V) and $|V_d|$= 30 mV.

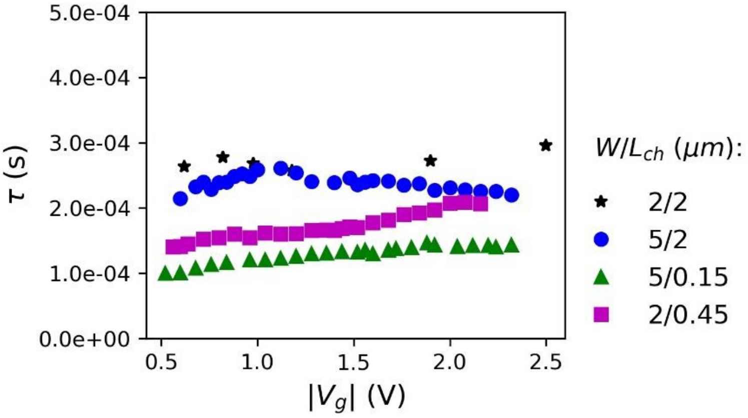

Figure 4-11: Extracted Lorentzian characteristic time constant versus V_g for different device dimensions.

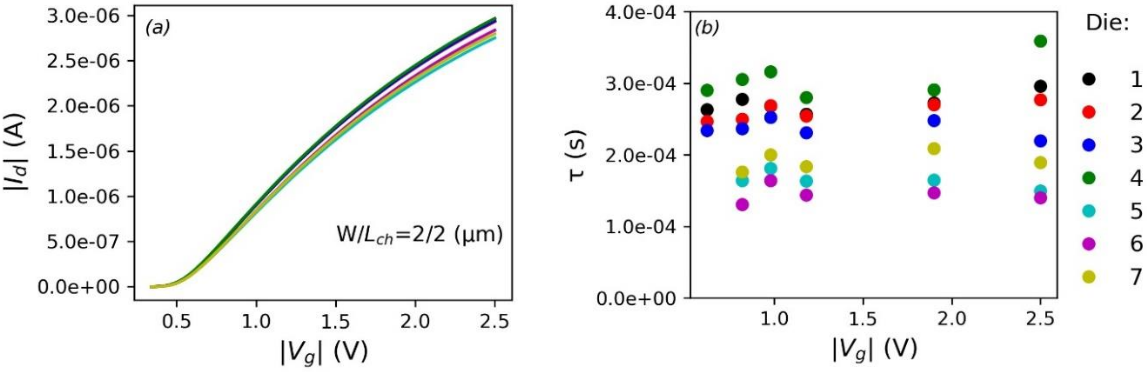

Figure 4-12: (a): Measured I_d-V_g curves for different dies of W/L=2/2 µm at |V_d|=30 mV, (b): Extracted Lorentzian characteristic time constant versus V_g for different dies.

4.4. Front vs back gate mode influence on Lorentzian PSD

As we proved that the traps could not be located inside the S/D junctions, in this section we study the scenario #2, which is the possibility that the traps are in the top or bottom oxide. To do so, we performed measurements under front and back gate modes of operation, and compared the extracted parameters. The results are described in the next paragraphs.

4.4.1. Experimental Results

We focused on the devices with W/L_{ch}=2/0.45 where we first performed static I_d-V_g and I_d-V_b measurements with grounded V_b and V_g respectively in the linear region of operation. The measured curves can be seen in Figure 4-13, in linear and logarithmic scale.

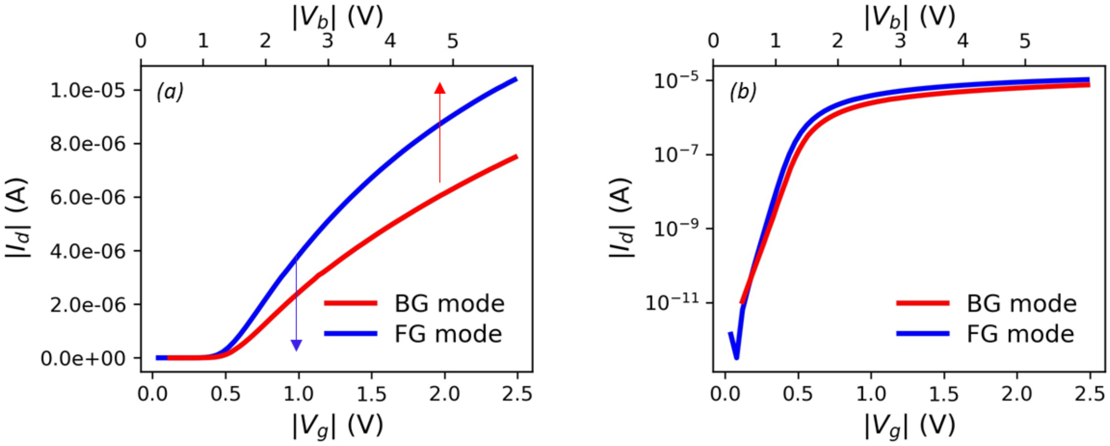

Figure 4-13: Measured drain current versus V_g and V_b in linear region of operation for a p-type device with W/L_{ch} = 2/0.45 µm. (a) linear and (b) logarithmic scale

The 25 nm BOX allowed the sweep of |V_b| up to 6 V so as the maximum drain current to be approximately the same in the two cases. We also applied the Y-function method [95], in order to extract the threshold voltage, V_t, and the low field mobility, μ_0. The values are shown in

Table 4-I, where one can see that the FG mode of operation shows lower mobility which can be attributed to the worse top oxide interface quality.

Table 4-I
Extracted V_t and μ_0 using Y-function method for front and back gate modes of operation. W/L_{ch}= 2/0.45 µm.

	V_t (V)	μ_0 (cm^2/V/s)
FG mode:	-0.51	90.62
BG mode:	-1.44	130

Following the static curves, we performed LFN measurements for both front and back gate modes of operation. The spectra for the two modes are shown in Figure 4-14, where it becomes obvious that the Lorentzian spectrum is present in both cases, making it really difficult to distinguish whether the traps are in the bottom or top oxide. Fitting the LFN PSDs, using eq. *(4-2)*, was followed in order to extract the Lorentzian parameters for each polarization case. The results are shown in Figure 4-15.

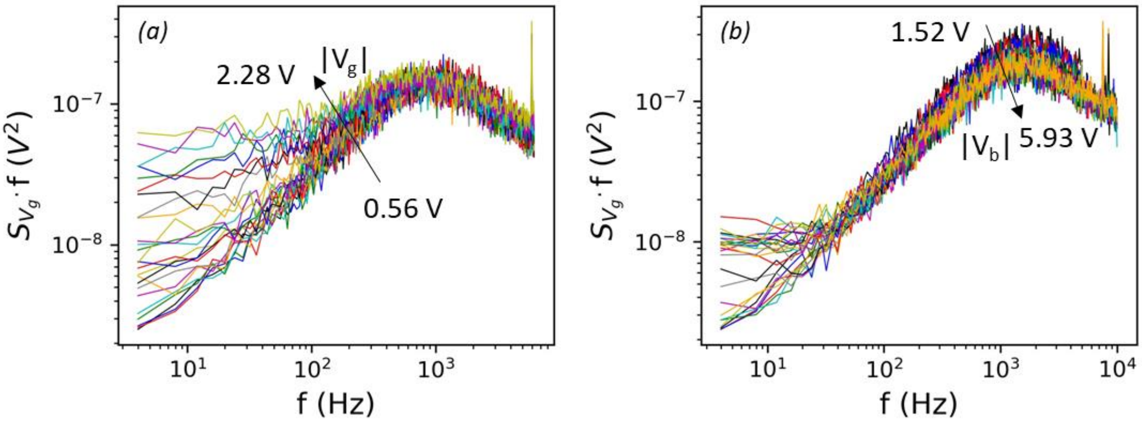

Figure 4-14: Input referred gate voltage power spectral density multiplied with frequency versus frequency in linear region of operation |V_d|=30 mV for different polarization conditions. (a): front gate mode with grounded B, (b): back gate mode with grounded G.

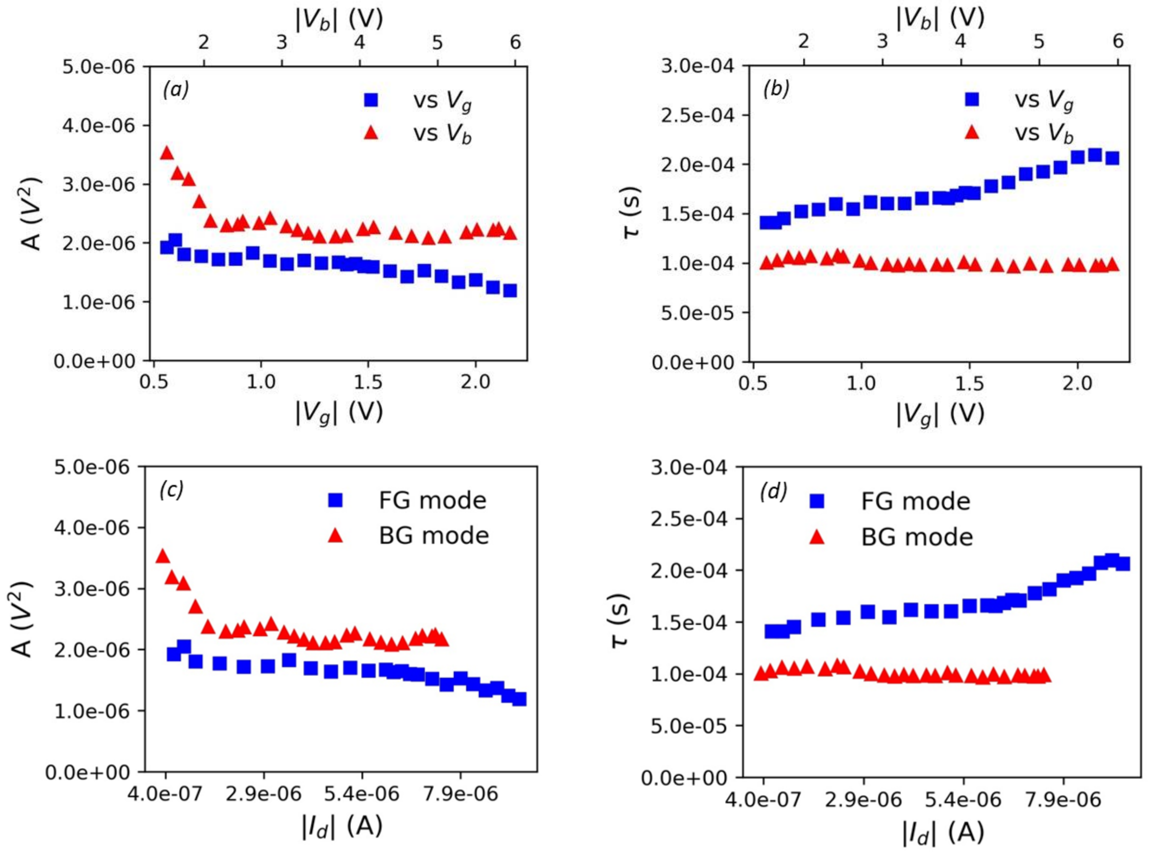

Figure 4-15: Extracted Lorentzian parameters, A and τ, for both front and back gate mode of operation versus V_g.V_b and I_d in linear region of operation, $|V_d|$=30 mV.

Concerning the Lorentzian plateau, A, it is extracted in all cases from S_{V_g}, which in the case of back gate mode, it is calculated by measuring the drain current difference for ΔV_g=40 mV so as to utilize the front g_m, as in front gate mode. No significant dependence on V_g or V_b has been observed, with A in the back gate mode being slightly higher (Figure 4-15a). On the other hand, concerning the characteristic time constant, one can see that there is a slight increase with V_g, whereas it shows constant behavior with V_b. As mentioned above, τ depends on τ_c and τ_e, parameters which according to the SRH statistics depend on the trap energy and carrier concentration [49], [50]. More specifically, at a given temperature, $\tau_e \propto \exp(\Delta E/kT)$, and $\tau_c \propto n^{-1}$ or p^{-1}, with n and p being the electron and hole concentrations close to the trap in the conduction and valence band respectively. The value of τ is approximately the same in both front and back gate of operation, (Figure 4-15b). This is an indication that the traps have the same energy level or at least very close ones, and thus we can safely assume that it is the same group of traps that is causing the Lorentzian PSDs in both cases. On the other hand, since the LFN measurements were taken in strong inversion, one would expect τ_c to have linear relation with I_d due to the dependence on carrier concentration. But this is not the case, since as it is depicted in Figure 4-15d, the current changes for more than one decade whereas τ could be considered constant with I_d, as it changes only by a factor of 1.5. In addition, one would expect a decrease of τ with the drain current, but in this case, we observe an almost constant value τ with I_d.

Thanks to all the above observations, we conclude that the traps can be located neither in the top nor in the bottom oxide interface. If this was the case, in one of two modes of operation, we would have measured a clear dependence of τ with I_d, related to the surface carrier concentration dependence. In order to further demonstrate this effect and examine whether the scenario #3 is more plausible, we pursued to perform a series of TCAD simulations. The results are shown in the following section.

4.4.2. TCAD simulation results

For better understanding of the behavior of the carrier concentration in both operating conditions, we used Atlas SILVACO [104]. First, we tried to fit the experimental static curves in front and back gate mode. Figure 4-16, shows the structure created in Atlas and Figure 4-17, Figure 4-18 show the simulated static front and back gate curves in linear and logarithmic scale along with the experimental ones. As it is shown, we achieved excellent fitting of the experimental characteristics. Some of the parameters used for the simulated structure are shown in Table 4-II. It should also be mentioned that in order to approximate the difference in the mobility between the front and back gate mode, we splitted the channel film into two regions with the same doping but with different mobility values.

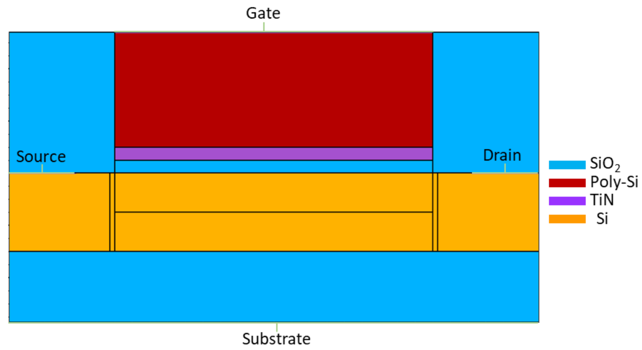

Figure 4-16: Simulated structure using ATLAS-SILVACO.

Table 4-II
Parameters used in the simulations.

Poly-Si Thickness	44 nm
Poly-Si doping	7x10^{18} cm^{-3}
TiN thickness	5.2 nm
Top oxide thickness	4.8 nm
Si film thickness	30 nm
Si film doping	4x10^{15} cm^{-3} (p-type)

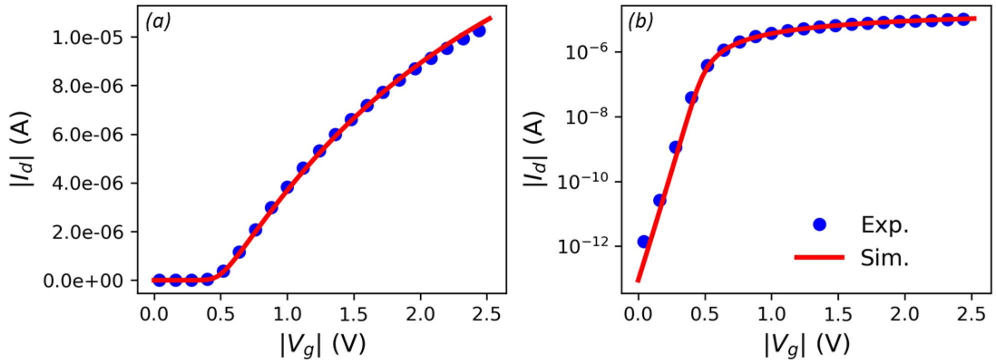

Figure 4-17: Experimental and simulated static I_d-V_g curves in linear region of operation, $|V_d|$=30 mV, for device with W/L_{ch}=2/0.45 (μm), (a): in linear and (b): in logarithmic scale.

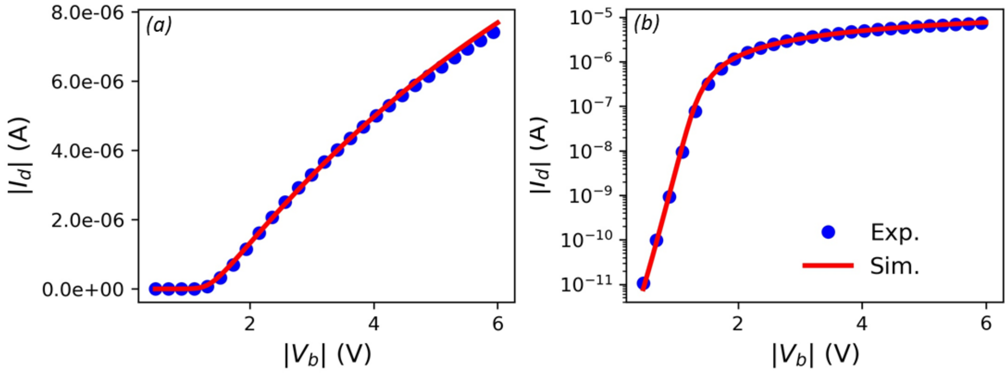

Figure 4-18: Experimental and simulated static I_d-V_b curves in linear region of operation, $|V_d|$=30 mV, for device with W/L_{ch} = 2/0.45 (μm), (a): in linear and (b): in logarithmic scale.

Afterwards, in order to estimate the capture and emission time constant behavior with regards to the traps' location in the channel, we pursued to the extraction of carrier concentration (holes and electrons) in the middle of the channel and for different depths going from top to bottom interface. The results are shown in Figure 4-19.

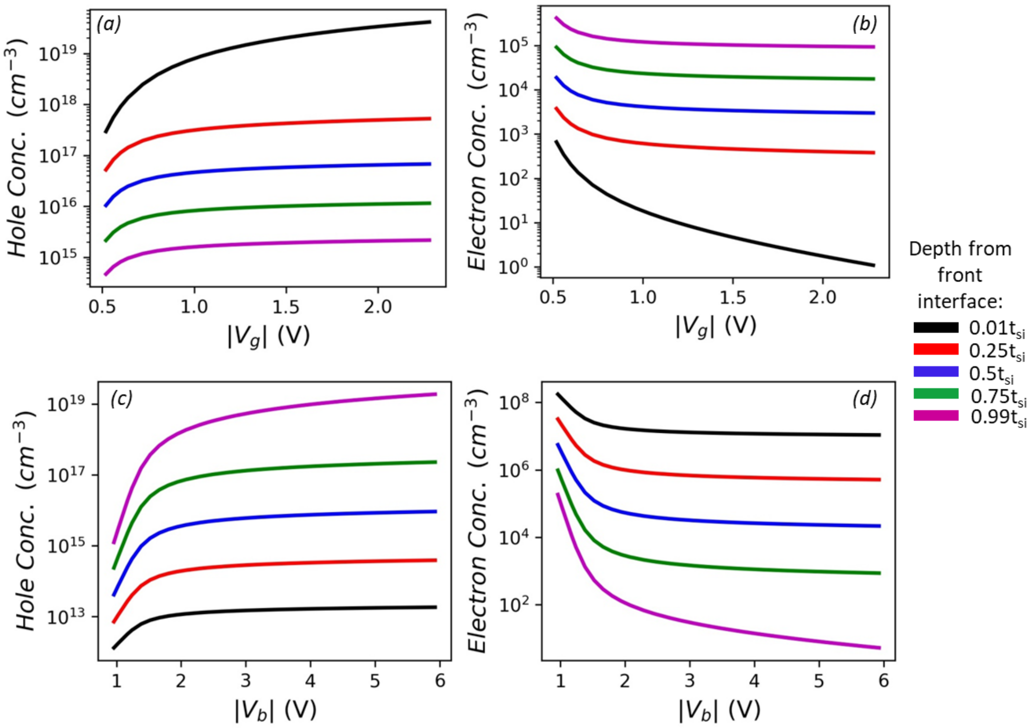

Figure 4-19: Extracted from simulations hole and electron concentration for different depths inside the Si film. (a),(b): front gate mode with grounded V_b, (c),(d): back gate mode with grounded V_g.

If we consider the front gate mode of operation case, and take first the hole concentration close to top and bottom interface ($0.01t_{si}$ and $0.99t_{si}$), the τ_c can be calculated using the eq. *(4-4)*, where for σ we used the extracted value from the Arrhenius plot, 1.21×10^{-18} cm^2, and for the thermal velocity we used a typical value, v_{th}=2x10^7 cm/s [103].

$$\tau_c = \frac{1}{\sigma v_{th}(n,p)} \tag{4-4}$$

Then, if we select a value for τ_e close to τ_c, and keep it constant with V_g, the characteristic time constant, τ can be extracted. The result is shown in Figure 4-20. It can be observed that the trend of τ with V_g follows the experimental one (almost constant in strong inversion) only if the traps are located at the bottom interface. However, the respective simulations for back gate mode have the reverse behavior (Figure 4-21), meaning that in fact the traps cannot be located at the bottom interface. On the other hand, if we consider acceptor-like traps and extract the electron concentration through eq. *(4-4)*, its value is so low due to the channel depletion that τ_c becomes huge as it is shown in Figure 4-22.

From these simulation results, it can be concluded that the group of traps that results to GR noise could not be at the top or bottom interface, because the trend of τ with V_g cannot be explained with the carrier concentration behavior.

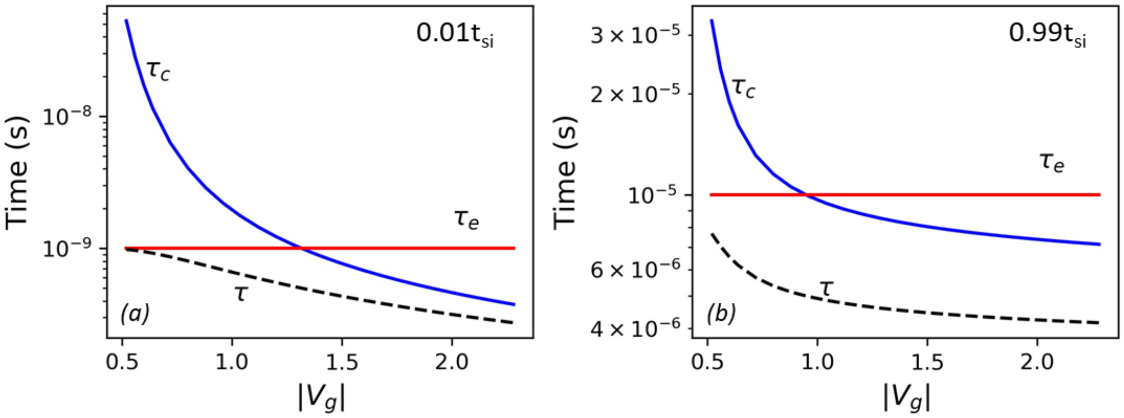

Figure 4-20: Calculated time constant based on the hole concentration at two different distances from the top interface versus V_g. (a): 0.01tsi, (b): 0.99tsi.

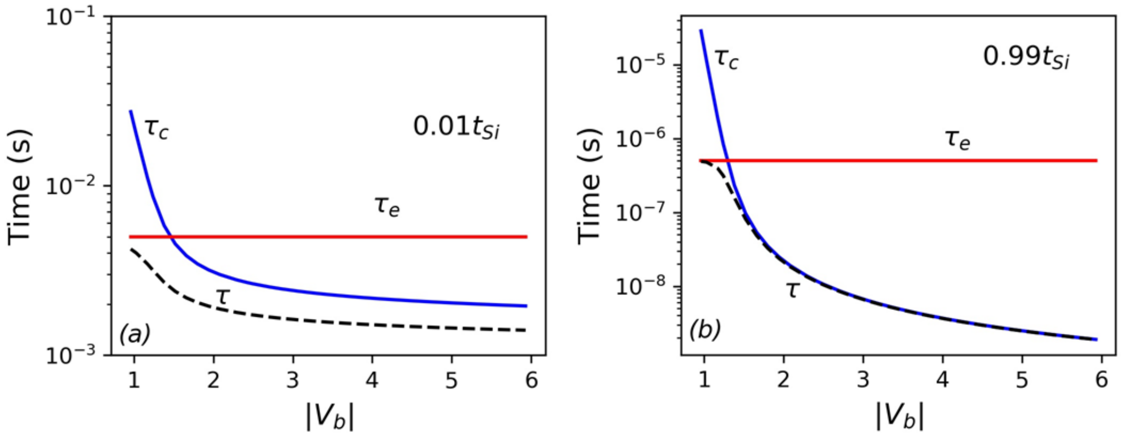

Figure 4-21: Calculated time constant based on the hole concentration at two different distances from the top interface versus V_b. (a): 0.01tsi, (b): 0.99tsi.

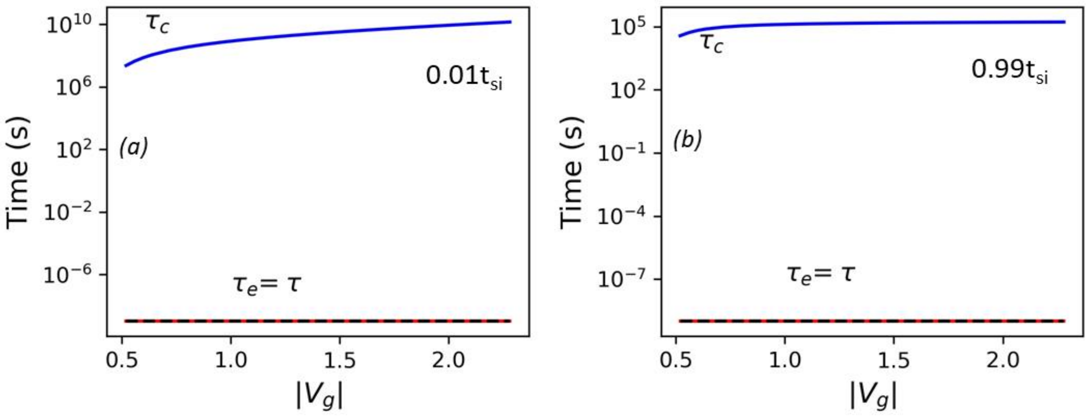

Figure 4-22: Calculated time constant based on the electron concentration at two different distances from the top interface versus Vg. (a): 0.01tsi, (b): 0.99tsi.

4.5. Constant current method

Since we observed in the previous section the independence of the Lorentzian characteristic time constant on V_b and its slight increase with V_g, the scenario #3, which is the assumption that the traps are inside a depleted region, becomes more plausible. In order to prove this scenario and to discover where this depleted region exists inside the Si film, we applied the constant current method so as to change the carrier distribution vertically, going from front gate to back gate mode of operation, and observe the impact of the channel (centroid) position on the Lorentzian parameters. It should be noted that, to the best of our knowledge, it is the first time that this method is used for Lorentzian noise analysis. The idea behind this procedure is that in the case that the group of traps are inside the Si film, and considering the SRH model, in which the capture time is inversely proportional to the free carrier concentration close to the trap, the resulting τ of the Lorentzian PSD would be strongly affected by the position of the channel, because by keeping the total charge constant and moving the charge centroid from top to bottom, the charge maxima passes through every vertical position. Therefore, according to (4.4), if the GR centers are in the bulk of the Si film, their capture time constant should be very sensitive to the position of the channel, because only the concentration near the traps affects τ_c.

To begin with, we measured various I_d-V_g curves, shown in Figure 4-23, each of them having a different back gate value, from 2.5 to -6 V, so that the channel position gradually moves from top to bottom interface, since we are referring to a p-type device. Then we selected different pairs of V_g and V_b values which give the same current level, around 7 µA (strong inversion), and we pursued to the LFN measurements.

Figure 4-24 shows the measured S_{V_g} versus frequency at the same current level but for different pairs of V_g and V_b. One can clearly see, before even going to the extraction of Lorentzian parameters, that there is no significant difference between the PSDs although the position of the channel changes due to the different front and back polarization conditions. In addition, from the same figure, it can be observed that as the device operation goes from front gate mode to back gate mode the 1/f part of the spectrum is decreasing. This is another confirmation that the two, front and back, interfaces have not the same qualities, with the top interface showing higher number of traps. It is worth noting that the Lorentzian plateau (corresponding to the hump peak) is surprisingly constant for all combinations.

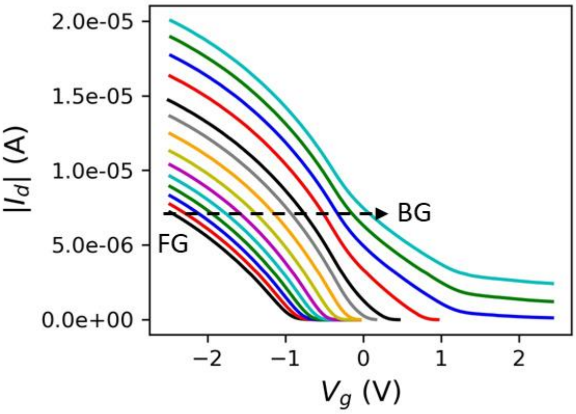

Figure 4-23: Measured I_d-V_g curves in linear region of operation |Vd|=30 mV for different back gate values.

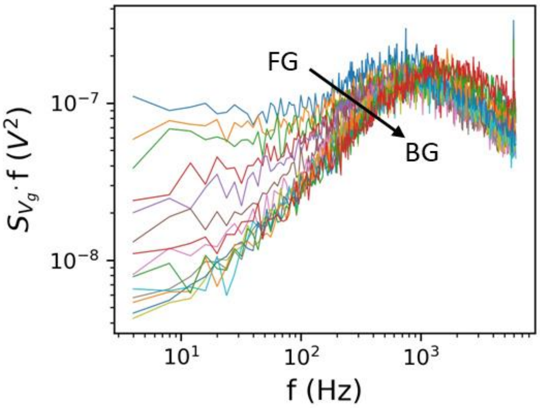

Figure 4-24: Input referred gate voltage power spectral density multiplied with frequency versus frequency in linear region of operation $|V_d|$=30 mV at the same current level and different pairs of V_g,V_b values.

Finally, Figure 4-25, shows the extracted Lorentzian parameters for the different pairs of V_g and V_b. As expected, considering the PSDs depicted in Figure 4-24, no significant impact of channel position on A is observed. Concerning τ, which according to our first assumption should have been strongly influenced by the position of the channel if the traps are inside the Si film, here we observe a noticeable but not dramatic change with the channel centroid position. Actually, τ varies between its value at the back gate mode and the corresponding one in the strong inversion of the front gate mode of operation (see Figure 4-15b). The results from the application of the constant current method, excludes the possibility that the traps are inside the Si film, since no significant change of the time constant has been observed. In fact, the constant current method led us to the conclusion that the characteristic time constant of the Lorentzian is affected mostly by the front gate potential and not by the concentration of free carriers.

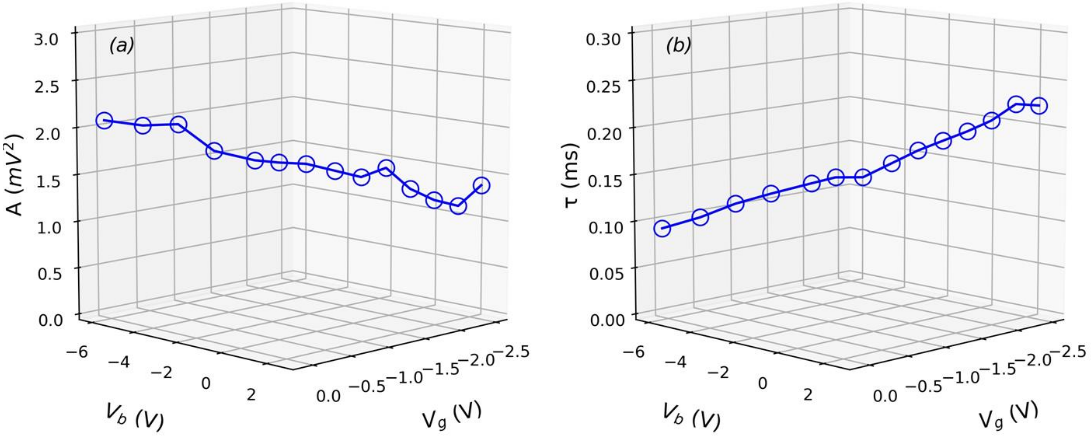

Figure 4-25: Extracted Lorentzian parameters for the different pairs of Vg and Vb. (a): Normalized with gm Lorentzian amplitude, (b): characteristic time constant.

We applied the constant current method on a device with different geometry (W/L_{ch}= 5/0.15 µm), in the strong inversion region, and as it is depicted in Figure 4-26, where the time constant for both geometries is depicted, similar results were obtained.

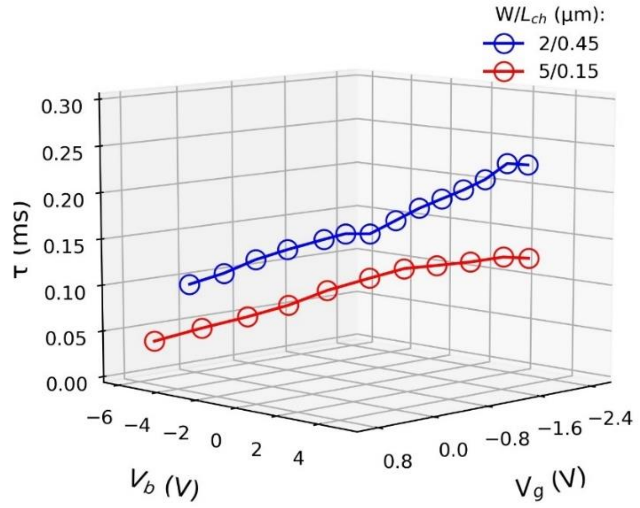

Figure 4-26: Extracted time constants of Lorentzian spectra for the different pairs of Vg and Vb, for two dimensions.

Based on the above analysis, we estimate that the scenario #4 becomes more dominant. In this case, carriers from the metal side can interact with traps in the oxide through tunneling, and thus screening this effect to the channel side. In addition, due to the excess number of carriers in the metal, we assume that the observed dependence of τ with the front gate potential is related to the dependence of τ_e on $e^{\Delta E}$/kT ($\Delta E=E_C-E_T$). For an oxide trap ΔE may vary with V_g when the surface potential is almost constant, like in strong inversion. To show how the potential changes inside the front oxide, and whether this change of the potential could explain the behavior of τ under different polarization conditions, we extracted, using ATLAS, the absolute difference of the potential between two points inside the oxide. We chose one point to be $0.2t_{ox}$ from the top interface and one close to the latter. Figure 4-27 shows the extracted $e^{\Delta V}$ versus V_g and V_b. As you can see, $e^{\Delta V}$ is almost constant with V_g until a specific value above which it starts to increase. This can be explained with the relation of the surface potential with V_g: strong dependence in the sub-V_t region and weak dependence above once inversion is achieved. On the other hand, we can see that the back bias mode does not influence this potential.

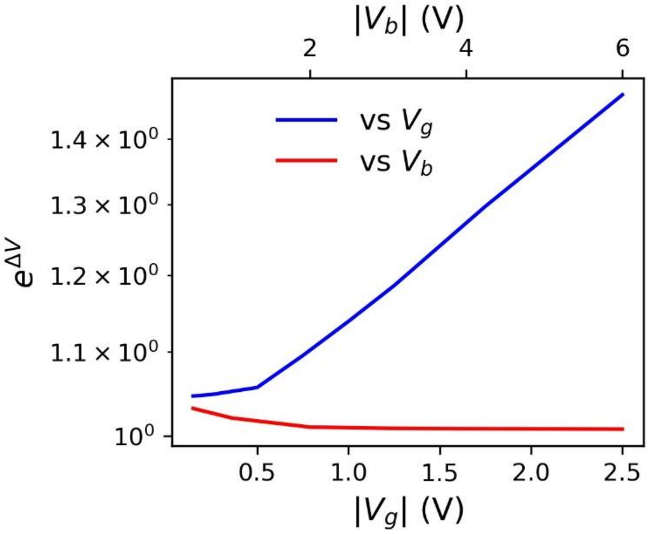

Figure 4-27: Exponential potential difference for two different vertical positions of the oxide versus different polarization conditions. (blue): versus V_g and (red): versus: V_b.

The experimental verification of this scenario, through studying wafers with no TiN, will be performed in the near future and it is not part of this dissertation.

4.6. Summary

To summarize, in this chapter we used LFN as a tool to localize defective areas, since it was observed that the LT SOI-FETs suffered from significant GR noise. We examined different scenarios for the traps' location and we applied various polarization conditions so as to derive how the Lorentzian parameters, A and τ, are affected by these. The scaling of A with area excluded the possibility of traps being at the source and drain regions. So, the remaining scenarios were that the traps are inside: a) the top or bottom oxide, b) silicon film or c) top oxide interacting with carriers in the TiN layer. The identification of the Lorentzian spectra in both front and back gate modes of operation as well as the weak dependence of τ on V_g or V_b led us to the assumption that the traps could be in a depleted region inside the channel. But this scenario was excluded once we observed the weak dependence of τ when changing the position of the channel inside the Si film, through the constant current method. For this reason, we believe that the scenario that the traps are in the top oxide but interact with the carriers in the TiN metal is more dominant. This scenario will be validated in the near future, once LFN measurements on wafers with no TiN will be performed.

CHAPTER 5

New LFN and RTN Characterization Methods for Short Channel Devices

5.1. Introduction

As already mentioned, low frequency noise is being extensively used since many years in order to evaluate the oxide/silicon interface quality. The carrier number fluctuation (CNF) approach, relating the 1/f noise to trapping and release of free carriers was first developed by A. McWorther in 1957 [21]. In 1991, G. Ghibaudo [62], came to strengthen the CNF model by adding also the impact of remote Coulomb scattering, due to trapped charge, on the LFN level, developing the CNF/CMF (carrier number fluctuations with correlated mobility fluctuations) model. This model has been applied on different technologies providing critical information not only for fabrication steps but also for the reliable operation of circuits.

It is widely known that with the miniaturization of the transistor area, although more components can fit on a given surface and less power consumption has been achieved, transistors with channel length less than 1 μm suffer from short channel effects (SCEs). The leakage current is increased due to loss of electrostatic control by the gate electrode [7] and mobility degradation effects are enhanced [105]. On top of that the access resistance becomes more and more important at nm-range lengths, as it is comparable to (or even higher) the channel resistance, leading to a limitation of I_{on}. To overcome these issues, new materials and architectures emerged to reassure the safe operation of transistors. This whole process has led to increased levels of LFN due to the higher density of traps, related to lower quality interfaces compared to the Si/SiO_2. But since the CNF/CMF model uses some static parameters of the transistor, it should be examined whether it accounts well for the SCEs because if not, it may lead to wrong values of the extracted parameters. In addition, since traps in nano-scale devices are not always uniformly distributed, new techniques that enhance their detectability may be needed. Overall, since in today's aggressively scaled down devices, LFN constitutes a significant issue, new methodology techniques able to provide the maximum possible information about the traps have to be considered.

In this Chapter, we show that the series resistance, R_{SD}, of the transistor can cause an unreliable extraction of noise parameters, especially the scattering coefficient, Ω, which is extracted in the strong inversion region. Although this issue is enhanced in short channel devices, where the R_{SD} from source and drain regions is comparable to the channel resistance, it can also occur in other cases when under the measurement setup the transistor is connected in series with a high resistance component. For this reason, we propose a R_{SD}-immune methodology for the accurate extraction of noise parameters, utilizing the Y-function, which is commonly used for static parameter extraction, thanks to its immunity to 1st-order mobility degradation and series resistance.

In addition, we show through systematic measurements and TCAD simulations, that RTN measurements under high V_d and high V_s condition can actually help to detect more traps. We demonstrate that the pinch-off effect in the saturation region of operation can be exploited for the modulation of RTN amplitudes and kinetics, and therefore disable or enable the appearance of RTN signals. Consequently, we propose a new measurement methodology, called "Pinch-to Detect", that combines three different channel configurations (uniform, pinch-off near the drain, pinch of near the source), and allows the total number of detectable RTN traps to be maximized.

All the LFN measurements were performed using the programmable bias point probe system NOISYS7 [65], combined with a semi-auto 300 mm Cascade Micro Tech probe station.

5.2. Effect of source/drain series resistance R_{SD}

For many years the extraction of LFN parameters of MOSFETs, related to the 1/f component, has been based on the carrier number fluctuations with correlated mobility fluctuations (CNF/CMF) model described by the eq. (*(5-1*) and (*(5-2*) [62], [64]. As mentioned in previous chapters, the CNF/CMF model considers two kinds of fluctuations taking place in a direct and an indirect way due to trapping and release of free carriers, especially those closer to the oxide/silicon interface. The direct impact of the dynamic interaction between free carriers and traps is the change of the number of free carriers (Δn), which in turn fluctuates the mobility of the carriers through remote Coulomb scattering resulting to correlated mobility fluctuations (Δμ/Δn). Since LFN is attracting more and more interest, as it can not only be used for device performance characterization in terms of dynamic stability [106], but it also as a tool to provide important information such as defects in the oxide/channel interface or inside the channel [51], its study is really valuable especially in today's aggressively scaled devices. But in order for the conclusions of LFN study to be useful for next fabrication steps, the reliable extraction of those parameters (N_t and Ω) through the CNF/CMF model is crucial.

$$\frac{S_{I_d}}{{I_d}^2} = (1 + \Omega\frac{I_d}{g_m})^2(\frac{g_m}{I_d})^2 S_{V_{FB}} \qquad (5\text{-}1)$$

Input-referred gate voltage noise:

$$S_{V_g} = S_{I_d}/{g_m}^2$$

$$\sqrt{S_{V_g}} = \left(1 + \Omega\frac{I_d}{g_m}\right)\sqrt{S_{V_{FB}}} \qquad (5\text{-}2)$$

Although the CNF/CMF model has been applied in both large and small area devices in numerous publications [107]–[110], no authors have correlated the degradation of the g_m/I_d factor in small area devices with the reliability of the extraction process for N_t and Ω. This model is obviously sensitive to the I_d/g_m factor, eq. *(5-2)*, which in turn is influenced by the presence of R_{SD}. If I_d and g_m were influenced by R_{SD} in the same way, then there would be no reason to question the extracted parameters. But this is not the case, as g_m presents more abrupt changes due to R_{SD} especially in strong inversion region. To showcase this dependence, we used Atlas-SILVACO [104] to simulate a SOI-FET with different channel lengths and extract the static parameters I_d and g_m, shown in Figure 5-1a and Figure 5-1b. As it is depicted in Figure 5-1c, I_d/g_m is almost independent of channel length below V_T, but above V_T each ratio starts to diverge from each other mainly due to the degradation of g_m. For this reason, it is rather questionable whether the extraction of noise parameters is reliable, especially the extraction of Ω coefficient which is extracted in strong inversion region.

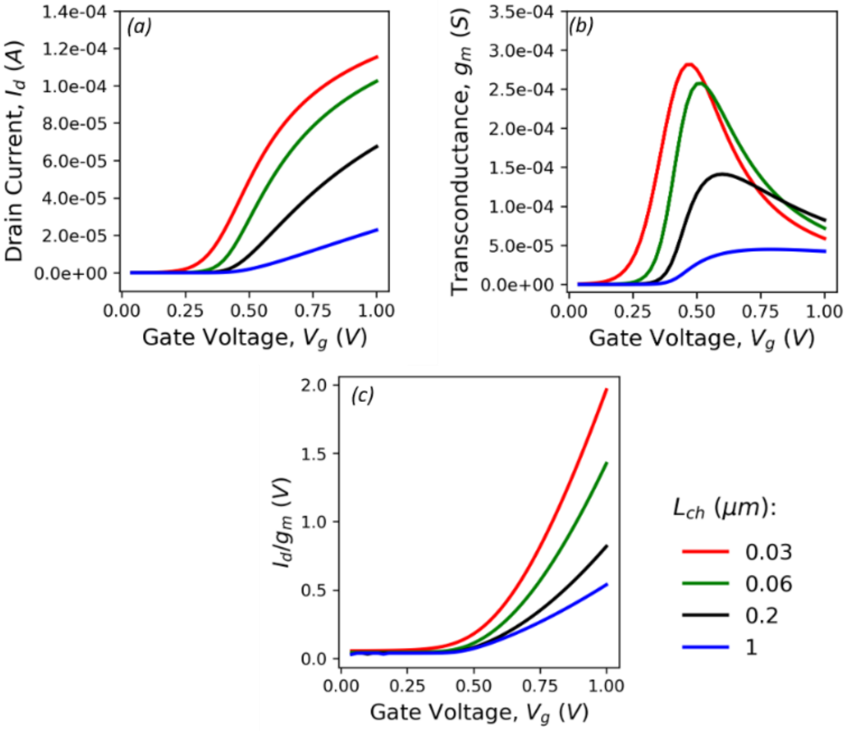

Figure 5-1: Static curves in linear region of operation (V_d =30 mV) for different channel lengths, L_{ch}. (a) Drain current versus gate voltage, (b) Transconductance versus gate voltage, (c) I_d/g_m ratio versus gate voltage.

5.2.1. Experimental Observation of R_{SD} impact on LFN/RTN parameter extraction

In order to monitor how the increase of R_{SD} can impact the extraction of Ω, we pursued to LFN measurements on a FinFET device, and we repeated the same measurement multiple times, each time having a different value of connected resistors, R_{ext} at both the drain ($R_{ext}/2$) and the source ($R_{ext}/2$) terminals. The setup schematic is shown in Figure 5-2. By this way the R_{ext} played the role of a hypothetical R_{SD}, additional to the R_{SD} that already the device has, without changing the channel length. The device under study was a n-channel FinFET with Si Bulk technology fabricated at IMEC-Leuven with number of fins N_{fin}=22, fin height H_{fin} = 26 nm, channel length L_{ch} = 28 nm and fin width W_{fin} = 4.5 nm.

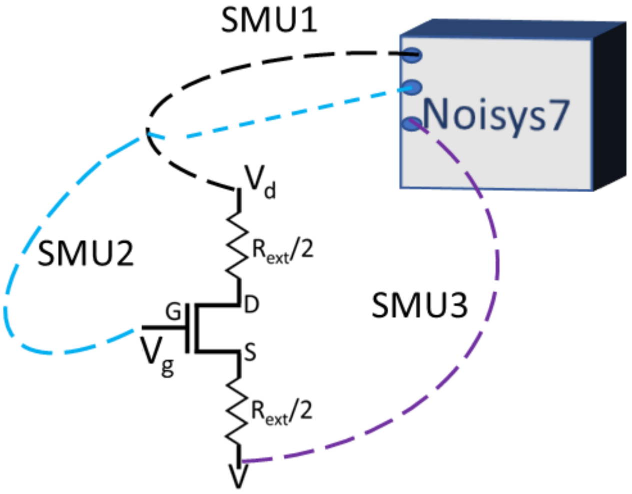

Figure 5-2: Experimental setup for monitoring the R_{ext} influence.

The external resistance values were chosen to be close to the channel resistance value in strong inversion region (V_d/I_d), which was around 1 KΩ, so as the impact of R_{ext} to be clearly observed. Figure 5-3 shows the static I_d-V_g curves in linear region of operation for all the different R_{ext} values. The drain current is significantly degraded with R_{ext} in strong inversion region. In order to utilize the CNF/CMF model to study the impact of this degradation phenomenon on noise parameters, we needed first to ensure that the drain current noise spectral density is 1/f-like. Indeed, as it is shown in Figure 5-4, the S_{I_d} for the zero external resistance case has a pure 1/f-like behavior allowing us to apply the CNF/CMF model for the PSD value around 10 Hz. The stabilization of S_{I_d} above a certain frequency, around 800 Hz, is probably due to the thermal noise [111] resulting from the intrinsic device resistance or the increased contact resistance. It must be clarified, that in this study we do not consider resistors which could contribute on the 1/f noise part. The impact of access resistance noise on LFN has been well described using the channel access resistance noise $S_{R_{SD}}$ [92], but this is not the case, as in this work we mention only cases where the external resistors add only thermal noise and so no influence on the 1/f trend is expected.

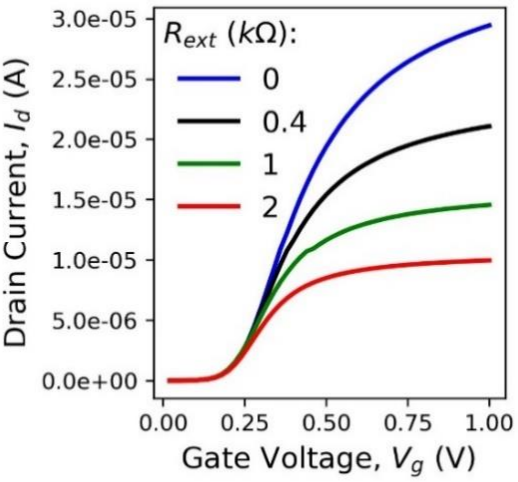

Figure 5-3: Drain current versus gate voltage characteristics measured at drain voltage V_d = 30 mV for various values of external resistance.

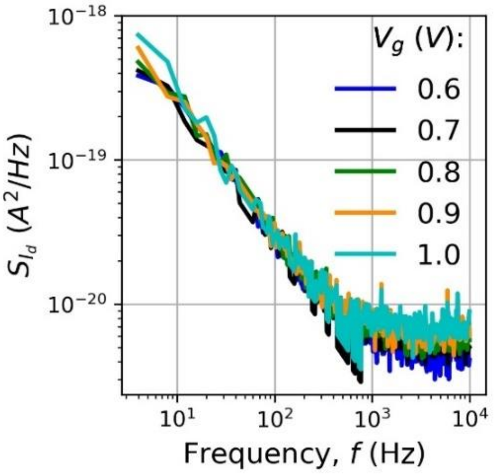

Figure 5-4: Drain current noise spectral density measured at drain voltage V_d = 30 mV and different gate voltages for the zero external resistance case.

Figure 5-5a, shows the normalized current noise (S_{I_d}/I_d^2) around 10 Hz versus I_d for four different R_{ext} values along with the corresponding CNF/CMF model fit in the strong inversion region where the influence of R_{ext} takes place. The dotted lines represent the CNF/CMF model with Ω=0, to visualize how a high value of series resistance can make one think that there is no mobility fluctuations (CMF) contribution. Indeed, we observed that as the series resistance increases, the experimental data approach the CNF model, eliminating almost completely the influence of CMF coefficient Ω in the case of maximum R_{ext} = 2 kΩ. Apparently, the fitting of the experimental data with the CNF/CMF model might be perfect, but extracting the real value of the parameters cannot be guaranteed. This happens mainly in small area devices where the impact of access resistance from contacts or from external components connected to the transistor is enhanced due to low channel resistance.

The same behavior can be also observed from the $\sqrt{S_{V_g}}$ versus I_d/g_m plot shown in Figure 5-5b, where we note that the slope of the characteristics changes with R_{ext}, thus leading to the extraction of a different Ω value for every R_{ext}. This effect takes place because the presence of R_{ext} degrades g_m/I_d, thus leading to an increase of the I_d/g_m ratio, and shifts the experimental data points to the right, resulting to the unreliable extraction of the CMF factor Ω. Combining this finding with the fact that the intercept remains the same for all R_{ext} values and thus a constant value of $S_{V_{FB}}$ can be extracted, we conclude that the diverging characteristics will lead in an underestimation of the Ω factor [81].

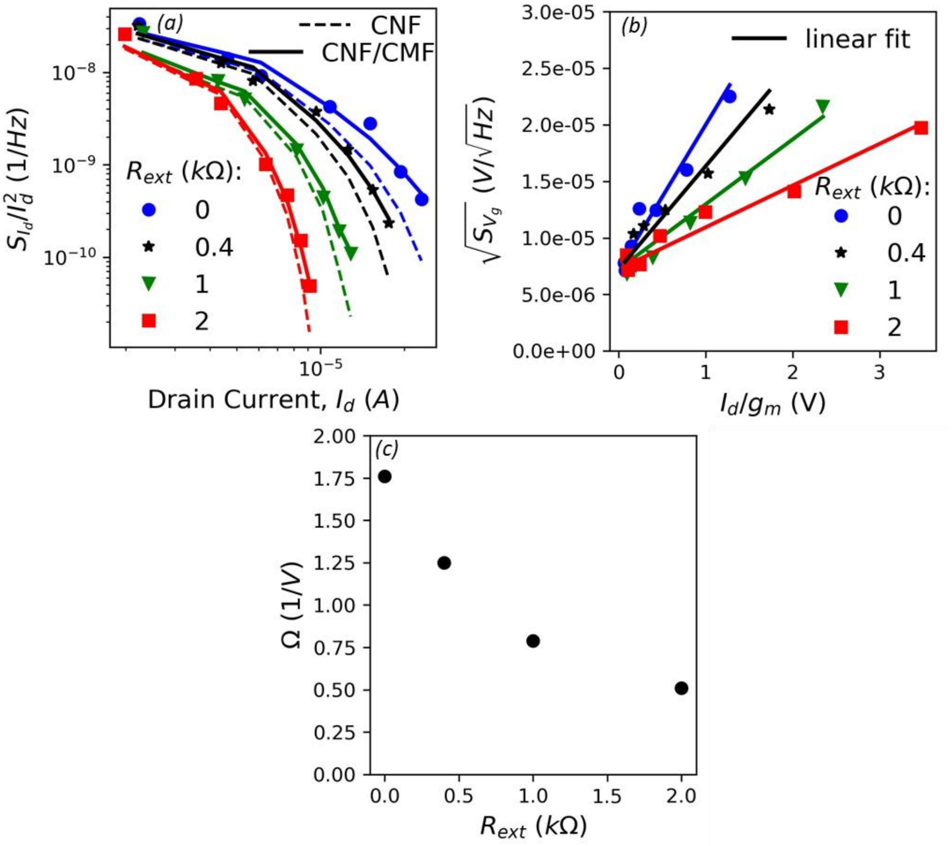

Figure 5-5: (a) Normalized drain current noise versus drain current, measured at drain voltage V_d = 30 mV, along with the CNF and CNF/CMF fitting models for the different external resistance values, (b) Square root of input-referred noise versus the ratio of drain current and transconductance, measured at drain voltage V_d = 30 mV, for various external resistance values, (c) Extracted CMF factor Ω versus the external resistance values.

By extracting $S_{V_{FB}}$ from Figure 5-5a and by taking a mean value of 5.24x10^{-11} V^2/Hz for $S_{V_{FB}}$, we pursued to the linear fit of eq. *(5-2)* in Figure 5-5b in order to calculate the Ω coefficient for the different R_{ext}. The dependence of this 'apparent' Ω on the presence of R_{ext} can be seen in Figure 5-5c. As expected, the extracted Ω factor is reduced with R_{ext}, revealing an underestimation due to the specific extraction process. Of course, the real value of Ω is not necessarily extracted even when R_{ext}=0, because there is also the intrinsic series resistance of the device, from the source/drain regions.

It is interesting to mention that concerning S_{V_g} itself, the R_{SD} degradation is cancelled out thanks to the division of normalized S_{I_d} with g_m^2. This can be seen in Figure 5-6 where the square root of S_{V_g} is plotted versus the gate voltage overdrive V_g-V_t. The values of S_{V_g} coincide regardless the value of R_{ext}. One might claim to use this method to extract the noise parameters, through eq. *(5-3)*, but apart from the fact that this equation is valid only in the strong inversion region [62], in some cases, this approach results to a non-linear increase of $\sqrt{S_{V_g}}$ or ΔV_g with V_g-V_t, as shown in Figure 5-7, which is attributed to the surface roughness scattering [64]. The coefficients that describe the mobility degradation due to scattering are $\theta_{1,0}$ and θ_2. $\theta_{1,0}$ describes the mobility limitation caused by phonon scattering, whereas θ_2 represents the decrease of the mobility due to the oxide/channel interface surface roughness , combined with the strong perpendicular electric field [112].

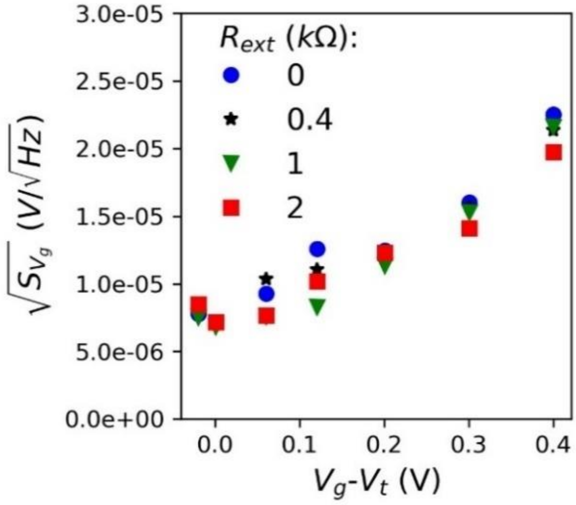

Figure 5-6: Square root of input-referred noise versus the gate voltage overdrive, measured at drain voltage V_d = 30 mV, for various external resistance values.

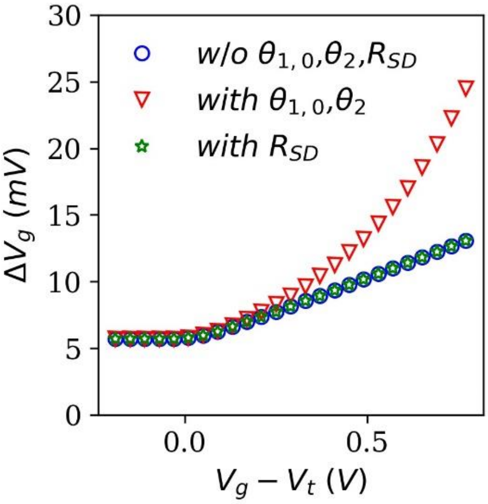

Figure 5-7: Simulated data of input-referred gate voltage variation versus gate voltage overdrive. Parameters used: $\vartheta_{1,0}$ = 1 V^{-1}, ϑ_2 = 0.5 V^{-2}, R_{SD}/R_{ch}=0.25.

Figure 5-7 shows the simulated ΔV_g versus V_g-V_t for different degradation effects. Indeed, when only R_{SD} is present the linearity of ΔV_g with V_g-V_t is retained without altering the LFN parameters, whereas when $\theta_{1,0}$ and θ_2 are present, the linearity is lost and the application of the CNF/CMF model through eq. *(5-3)* becomes impossible. The simulation results were obtained in Python Spyder platform [113] using eq. (*(5-5*), with Q_i numerically calculated using the charge-based Lambert-W (LW) function [114], with the following parameters: W = 0.1 μm, L = 0.1 μm, μ_0 = 100 cm^2/Vs, T = 300 K, η = 1, t_{ox} = 1.2 nm, V_t = 0.2 V, V_d = 30 mV, Ω = 2 V^{-1} and

ΔV_{FB} = Q_{ox}/(WLC_{ox}) [62], where Q_{ox} is the equivalent interface charge resulting from an interface trap concentration N_{it}=1e11 cm^{-2}.

$$\sqrt{S_{V_g}} = \sqrt{S_{V_{FB}}}\ \ [1 + a_{sc}\mu_{eff}C_{ox}(V_g - V_t)] \tag{5-3}$$

It should be noted that $S_{V_{FB}}$ is actually the equivalent of ΔV_{FB} when going from a single trap to a distribution of traps. ΔV_{FB} refers to the electrostatic impact of a trapped charge Q_{ox} whereas $S_{V_{FB}}$ is the flat-band voltage power spectral density caused by a fluctuating oxide charge, $S_{Q_{ox}}$. On the other hand, ΔV_g is a more general noise quantity as it does not only include the electrostatic impact of the dynamic interactions of a free carrier with a trap but also the induced mobility fluctuations due to Coulomb scattering. In addition, as in the case of ΔV_{FB}, ΔV_g is more useful when simulating the noise amplitude behavior or studying single trapping effects such as RTN, but S_{V_g} is necessary for studying 1/f noise, where a distribution of trap time constants is involved.

Overall, one could say that when no intrinsic (mobility) attenuation effects are present, the plot of $\sqrt{S_{V_g}}$ with V_g-V_t could be considered as the ideal candidate to extract the LFN parameters since it is immune to R_{SD}. However, when that is not the case, new solutions should be found to allow for the reliable extraction of LFN parameters. For this reason, new modeling approaches have to be implemented, in order to cancel all possible errors on the extraction of noise parameters. Thus, it is necessary to study first the accurate impact of degradation effects such as mobility degradation and access resistance issues.

It is also interesting to mention that we observed the influence of the external resistance on the extracted LFN parameters not only for a 1/f-like spectrum but also for a 2-level RTN. We found a device whose time domain measurements give a RTN signal in the strong inversion region, and so we repeated the LFN measurements increasing each time the external resistance. The RTN signal at V_g= 0.9 V is shown in Figure 5-8, on the left. Figure 5-8:, on the right, shows the resulted relative amplitude affected by R_{ext}. It is obvious that, as observed previously, the CNF/CMF application on the experimental $\Delta I_d/I_d$ would lead to the underestimation of Ω.

For further study of this phenomenon, we chose to focus on the 1/f component of LFN due to limited number of measurements concerning the RTN case. But the methodology that is being presented in the next sections can also apply for RTN.

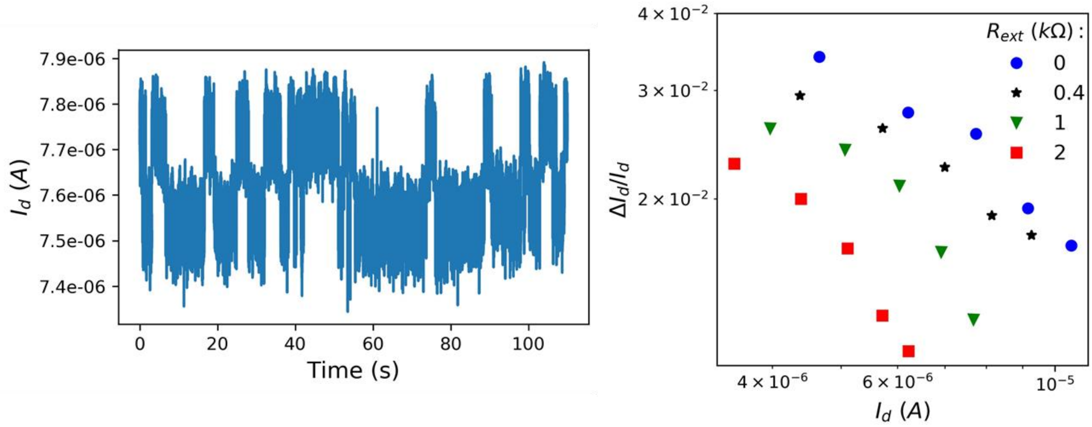

Figure 5-8: (a): 2-level drain current RTN signal in strong and in linear region of operation, (b): Relative amplitude ΔId/Id versus drain current for various R_{ext} values.

5.2.2. Intrinsic versus extrinsic degradation effects on LFN

A. *Mobility attenuation factors*

The channel mobility degradation effects are typically expressed through the conventional model of the effective mobility, from weak to strong inversion, by introducing the first and second order attenuation factors $\theta_{1,0}$ and θ_2, respectively, through eq. *(5-4)* [115]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_{1,0}\left(\frac{Q_i}{C_{ox}}\right) + \theta_2\left(\frac{Q_i}{C_{ox}}\right)^2} \tag{5-4}$$

where μ_{eff} is the effective channel mobility, μ_0 the low-field mobility, Q_i the total inversion charge per unit area and C_{ox} the oxide capacitance per unit area.

In order to properly probe the exact impact of these factors on the behavior of LFN, we should begin from the classic carrier number fluctuations with correlated mobility fluctuations (CNF/CMF) approach [53]. According to this generally accepted model, a fluctuation in the oxide charge, due to trapping of carriers, induces a change in the drain current, ΔI_d, directly through the variation in the number of free carriers and indirectly through a change in the effective mobility due to the trapped charge Q_{ox}. Considering the classical drain current expression in the linear region of operation, given in eq. *(5-5)*, [116], this can be all expressed through eq. *(5-6)*, [94].

$$I_{d,0} = \frac{W}{L}\mu_{eff}V_dQ_i \tag{5-5}$$

$$\Delta I_{d,0} = \frac{\partial I_d}{\partial V_g}\frac{\partial V_g}{\partial Q_i}\Delta Q_i + \frac{\partial I_d}{\partial Q_i}\frac{\partial Q_i}{\partial Q_{ox}}\frac{\partial Q_{ox}}{\partial \mu_{eff}}\Delta\mu_{eff} \tag{5-6}$$

The index “0” refers to the absence of series resistance, R_{SD}, and μ_{eff} is given by eq. *(5-4)*. After calculations, we obtain:

$$\left.\frac{\Delta I_d}{I_d}\right|_0 = -\left.\frac{g_m}{I_d}\right|_0 \Delta V_{FB}\left(1 + \Omega\left.\frac{I_d}{g_m}\right|_0\right) \tag{5-7}$$

where $\Delta V_{FB} = Q_{ox}/(WLC_{ox})$ is the flat-band voltage fluctuation caused by the trapped charge Q_{ox} and $\left.\frac{g_m}{I_d}\right|_0$ is the transistor gain calculated by the eq. *(5-8)*, which is a combination of eq. *(5-5)* and *(5-4)*. In eq. *(5-8)*, $C_{gc}=dQ_i/dV_g$ is the gate to channel capacitance.

$$\left.\frac{g_m}{I_d}\right|_0 = \frac{C_{gc}}{Q_i}\left(1 - \frac{Q_i}{C_{gc}}\frac{\theta_{1,0} + 2\theta_2 Q_i/C_{ox}}{1 + \theta_{1,0}\,Q_i/C_{ox} + \theta_2(Q_i/C_{ox})^2}\right) \tag{5-8}$$

One can easily notice in eq. *(5-8)*, that the $\theta_{1,0}$ and θ_2 coefficients are already accounted for through $g_m/I_{d,0}$ in eq. *(5-7)*. Indeed, as shown in Figure 5-9a, regardless the presence of mobility degradation or not, the CNF/CMF model captures well the simulated data from weak to strong inversion. For these simulation results we used the following parameters: W =60 nm, L =30 nm, μ_0 = 100 cm^2/Vs, T = 300 K, η = 1, t_{ox} = 1.2 nm, V_t = 0.2 V and V_d = 30 mV, N_{it} = 6e10 cm^{-2}, Ω = 1 V^{-1}. We used again the LW function as it allows the accurate extraction of gate to channel capacitance C_{gc}, and so an analytical expression of the inversion charge with gate voltage from weak to strong inversion and in both linear and saturation regions of operation is being achieved.

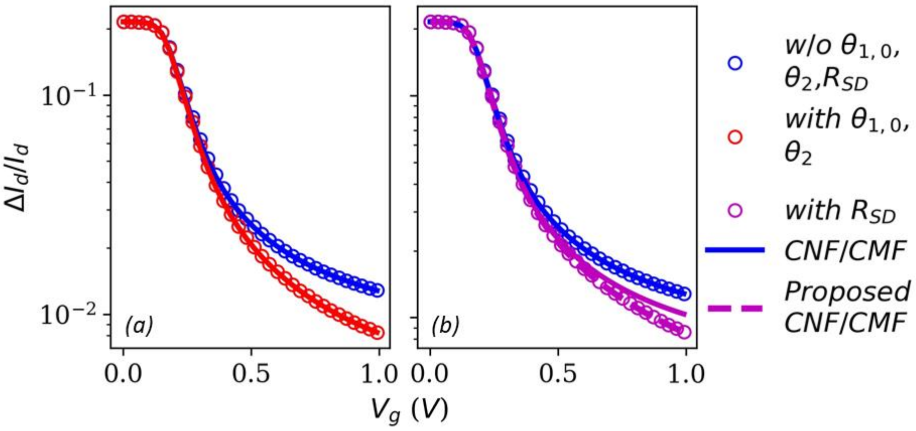

Figure 5-9: Simulated data (symbols) and CNF/CMF model (lines) of normalized drain current variation versus gate voltage. Parameters used: $\vartheta1,0=1V^{-1}$, $\vartheta2=0.5V^{-2}$, $R_{SD}/R_{ch}=0.5$.

B. Series resistance: A degradation of extrinsic nature

Despite the fact that the effective mobility-related drain current degradation is well accounted for in the CNF/CMF model -as shown in paragraph 5.2.2 A, this is not necessarily true in the case of an attenuation related to the source/drain series resistance, R_{SD}, because it is an extrinsic effect. The simplest way to express this kind of current degradation is through eq. *(5-9*), resulting from the application of Kirchhoff's first rule [117] in a system like in Figure 5-2, where R_{SD} equals R_{ext}.

$$I_d = \frac{I_{d,0}}{1 + G_{d,0}R_{SD}} \tag{5-9}$$

where $G_{d,0} = dI_{d,0}/dV_d$ is the channel conductance when no R_{SD} is present, which in the case where $V_d << V_g-V_t$, can be considered equal to $I_{d,0}/V_d$. It can be easily proven that the total derivative of eq. *(5-9*) considering that $dI_{d,0}/dV_d= I_{d,0}/V_d$ is:

$$dI_d = -\frac{dI_{d,0}}{\left(1 + G_{d,0}R_{sd}\right)^2} \tag{5-10}$$

From eq. *(5-10*) we can also express the normalized drain current fluctuation, resulting from a general source as:

$$\frac{\Delta I_d}{I_d} = \frac{\left.\frac{\Delta I_d}{I_d}\right|_0}{\left(1 + G_{d,0}R_{sd}\right)} \tag{5-11}$$

Finally, the combination of eq. *(5-7*), *(5-9*), and *(5-11*) gives us the equivalent CNF/CMF model when R_{SD} is present.

$$\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d}\Delta V_{fb}\left(1 + \Omega \frac{I_d}{g_m}\bigg|_0\right) \tag{5-12}$$

where the degraded g_m due to R_{SD} can be calculated based on eq. (*(5-9*) and is expressed below:

$$g_m = \frac{g_{m,0}}{(1 + G_{d,0}R_{SD})^2} \tag{5-13}$$

From the final eq. *(5-12*) it is obvious that the CNF part ($g_m/I_d\Delta V_{FB}$) includes the impact of R_{SD}, whereas the parenthesis expressing the impact of CMF is not affected by R_{SD}. As a result, if we use the measured I_d/g_m instead of the intrinsic $I_d/g_m|_0$ (without R_{SD}), the model is not expected to fit the measured data. This effect is shown in Figure 5-9b, where it is evident that although $\theta_{1,0}$ and θ_2 are not affecting the model's accuracy, R_{SD} can cause a significant deviation from the simulated data, mainly in strong inversion. In fact, there is a perfect fit when we use the improved CNF/CMF as proposed through eq. *(5-12*).

It is also interesting to examine how this effect can impact the extraction accuracy of the CMF factor Ω. Ω is usually extracted using the input-referred gate voltage noise $\Delta V_g = \Delta I_d/g_m$ (or $\sqrt{S_{Vg}} = \sqrt{S_{Id}}/g_m$ for PSD analysis) [53], to take advantage of its linear dependence with I_d/g_m and extract Ω using the slope:

$$\Delta V_g = -\Delta V_{FB}\left(1 + \Omega \frac{I_d}{g_m}\bigg|_0\right) \tag{5-14}$$

This quantity is plotted in Figure 5-10, versus both gate voltage overdrive V_g-V_t and I_d/g_m. As expected, the CNF/CMF model using the measured I_d/g_m cannot predict the noise behavior when R_{SD} is non-negligible. This phenomenon has also been shown in Figure 5-6 through our experimental observation. Furthermore, we confirm once more, through simulations, that comparing these two figures leads us to conclude that while ΔV_g does not seem affected by R_{SD}, when plotted against I_d/g_m, it seems as if it was degraded. This can be attributed to the increase of I_d/g_m with R_{SD}, which in turn leads to a less steep slope and to an eventual underestimation in the extraction of Ω, as shown in [81]. We also observe that it might further result in an overestimation of ΔV_{FB}.

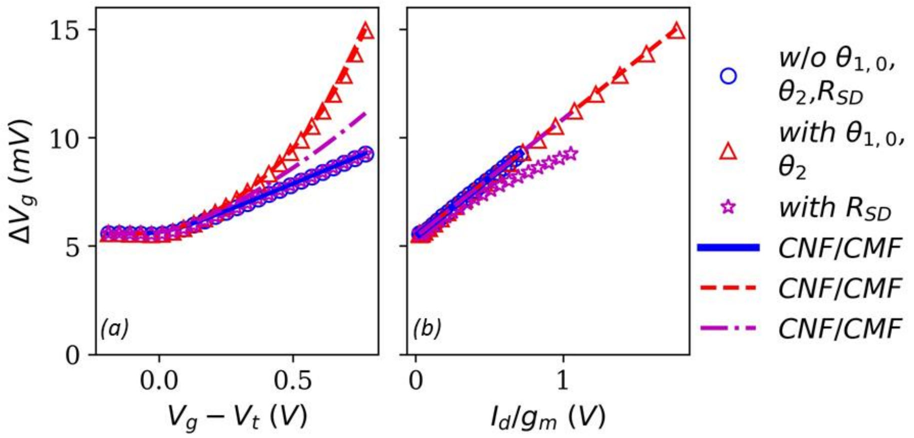

Figure 5-10: Simulated data (symbols) and CNF/CMF model (lines) of input-referred gate voltage variation versus gate voltage overdrive (left) and I_d/g_m (right). Parameters used: $\vartheta_{1,0}=1V^{-1}$, $\vartheta_2=0.5V^{-2}$ $R_{SD}/R_{ch}=0.5$.

5.2.3. Proposed Methodology for suppressing the impact of R_{SD}

As demonstrated in part 5.2.2, in order to achieve an accurate extraction of LFN parameters when R_{SD} is important, we need a precise estimation of $I_d/g_m|_0$. A quantity that is completely immune to R_{SD} is the Y-function [95], which is defined through $Y = I_d/\sqrt{g_m}$. As shown in [81], in the ideal case when $\theta_{1,0}=\theta_2=0$, $I_d/g_m|_0$ can be very well approximated with $Y/\sqrt{(\beta V_d)}$, where $\beta = W\mu_0 C_{ox}/L$. However, as demonstrated in [118], a more accurate approach of $I_d/g_m|_0$ is needed to account for $\theta_{1,0}$ and θ_2 and it is given by eq. *(5-15)*.

$$\left.\frac{I_d}{g_m}\right|_0 = \frac{\eta kT}{q} + \frac{Y}{\sqrt{\beta V_d}}\left(1 + \theta_{1,0}\frac{Y}{\sqrt{\beta V_d}} + \theta_2\left(\frac{Y}{\sqrt{\beta V_d}}\right)^2\right) \tag{5-15}$$

Equation *(5-15)* is actually a simplification of eq. *(5-8)*, which, if inverted, gives:

$$\left.\frac{I_d}{g_m}\right|_0 = \frac{Q_i}{C_{gc}}\left(\frac{1 + \theta_{1,0}\,Q_i/C_{ox} + \theta_2(Q_i/C_{ox})^2}{1 - \theta_2(Q_i/C_{ox})^2}\right) \tag{5-16}$$

and Q_i/C_{ox} is well approximated with $Y\sqrt{(\beta V_d)}$. However, in the presence of θ_2, the Y-function in strong inversion might not show linear dependence with V_g and so a correction of Y has been proposed in [119]. The new Y- function, Y_n, which suppresses the impact of θ_2, is given by eq. *(5-17)*.

$$Y_n = Y\sqrt{\left(1-\theta_2\left(V_g-V_t\right)^2\right)} \tag{5-17}$$

Therefore, for $V_g>V_t$, eq. (5-16) can be evaluated using the equivalent gate voltage overdrive V_Y through Y_n-function, $V_Y = Y_n/\sqrt{\beta V_d}$, by eq. (*(5-18*).

$$\left.\frac{I_d}{g_m}\right|_0 = \frac{\eta kT}{q} + V_Y\left(\frac{1+\theta_{1,0}V_Y+\theta_2(V_Y)^2}{1-\theta_2(V_Y)^2}\right) \tag{5-18}$$

Figure 5-11 illustrates how eq. *(5-18*) can perfectly emulate $I_d/g_m|_0$, and how it can ensure a proper extraction of $S_{V_{FB}}$ and Ω through linear regression.

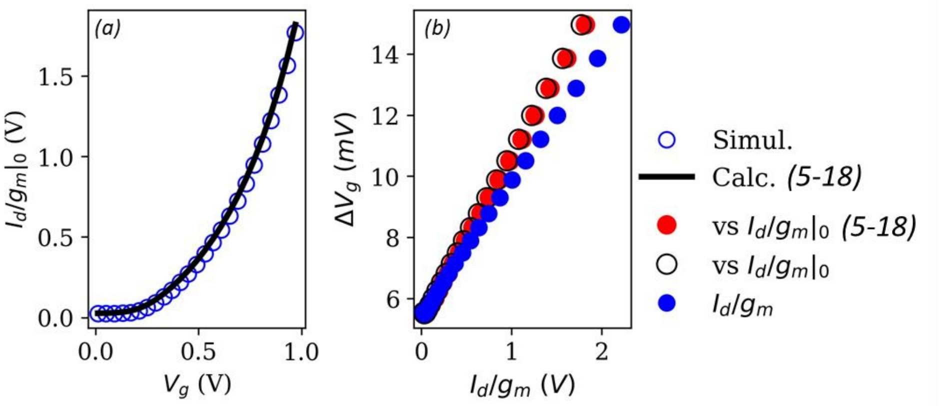

Figure 5-11: Comparison between simulated $I_d/g_m|_0$ and calculated through eq. (5-18) *(a). Simulated data of input-referred gate voltage variation versus I_d/g_m, simulated with and without the R_{SD} impact and calculated through eq.* (5-18) *(b). Parameters used: $\vartheta_{1,0}=1V^{-1}$, $\vartheta_2=0.5V^{-2}$ $R_{SD}/R_{ch}=0.5$.*

5.2.4. Experimental Application of the proposed R_{SD}-immune method

For the experimental application of the method presented in 5.2.3, we first need to extract some static device parameters such as V_t, $\theta_{1,0}$, θ_2, η, and β. Once all these parameters are known, the intrinsic $I_d/g_m|_0$ can be calculated, using eq. *(5-18)*, which then will be used for the CNF/CMF model fitting. We applied this proposed methodology on n-channel FinFETs fabricated at IMEC-Leuven with number of fins 4, fin height H_{fin} = 26 nm, and fin width W_{fin} =6 nm. In order to extract the $\theta_{1,0}$ coefficient we performed I_d-V_g measurements in linear region of operation, V_d = 30 mV, for 3 different channel lengths, (L = 44, 70, and 90 nm). It is important to mention that since we did not perform C-V measurements, we focused only in the strong inversion region where C_{gc} can be approximated by $C_{ox}= \varepsilon_{\mathrm{SiO_2}}/\mathrm{EOT}$ [120].

Firstly, we started with the extraction of V_t and β using the well-established Y-function method [95] and then we extracted the θ_1 and θ_2 coefficients through the linear fit of the θ_{eff} quantity, as given in eq. *(5-19)*, versus V_g-V_t in the strong inversion region [112]. A representative example of the θ_1 and θ_2 extraction is shown in Figure 5-12a. The extracted values of θ_2 were found to lie between 0.1 and 0.3 V^{-2} in all cases. Concerning θ_1, its dependence with β for different lengths, as expressed by eq. *(5-20)* [112], allows the extraction of R_{SD} and $\theta_{1,0}$ when plotting θ_1 with β as shown in Figure 5-12b. It should be noted that the static parameters θ_1, θ_2, β and V_t, were extracted by the average I-V characteristic of 9 identical devices for all the channel length cases. $\theta_{1,0}$ and R_{SD}, normalized by the effective gate oxide width, were extracted to be 0.497 V^{-1} and 203 Ω·μm respectively.

$$\Theta_{eff}(V_g) = \frac{\beta V_d}{I_d} - \frac{1}{V_g - V_t} = \theta_1 + \theta_2(V_g - V_t) \tag{5-19}$$

$$\theta_1 = \theta_{1,0} + \beta R_{SD} \tag{5-20}$$

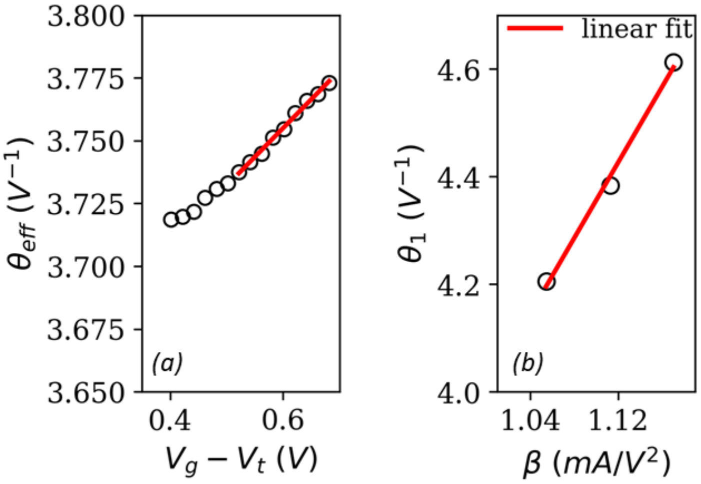

Figure 5-12: (a), Θ_{eff} versus gate voltage overdrive for channel length 90 nm along with the linear fit. (b), First order mobility attenuation factor (ϑ_1) vs β for 3 different channel lengths (44, 70, and 90 nm) along with the linear fit.

In order to avoid variability issues in our LFN analysis we measured 41 devices for L=44 nm, and we extracted an average I_d-V_g curve from which g_m and Y-function were calculated. The I_d-V_g curves along with the extracted subthreshold slope (SS), which we need to calculate the ideality factor through the relation η=qSS/(kTln(10)) [15], are shown in Figure 5-13. The ideality factor was extracted to be η=1.13.

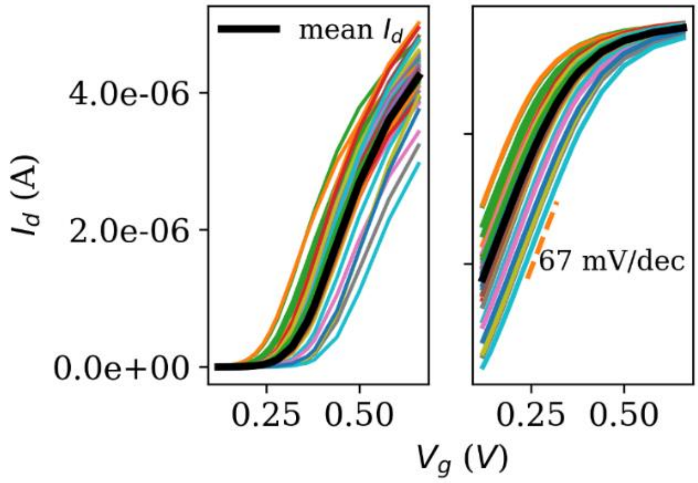

Figure 5-13: Current-Voltage characteristics in linear and logarithmic scale of 41 dies, measured at drain voltage V_d = 30 mV, along with the average Id-Vg curve, extracted by taking the mean value of the drain current of each device.

Detailed LFN measurements were also performed and the input-referred gate voltage noise power spectral density S_{V_g}=$S_{I_d}/g_m{}^2$ was extracted for 41 devices at various gate voltage values. The spectra, along with the average spectrum, extracted by taking the mean logarithmic [61] value of S_{V_g} of each device, are shown in Figure 5-14. The 1/f behavior of the average spectrum allows the application of the CNF/CMF model as it can be considered that a uniform trap distribution is present for each bias condition.

Figure 5-15 shows the $\sqrt{S_{Vg}}$ extracted at 10 Hz versus both the measured I_d/g_m and the calculated $I_d/g_m|_0$ using eq. *(5-18)*, for the extraction of the flat-band voltage power spectral density, S_{Vfb} and the Ω component, using the generalized form of eq. *(5-14)* for the linear fit in strong inversion.

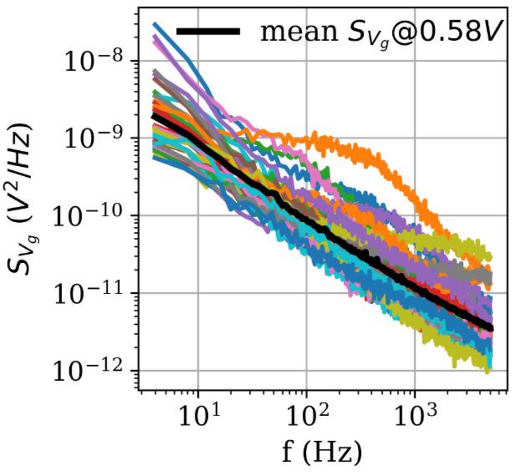

Figure 5-14: Input-referred gate voltage noise versus frequency, for 41 devices with L = 44 nm, biased under Vg= 0.58 V.

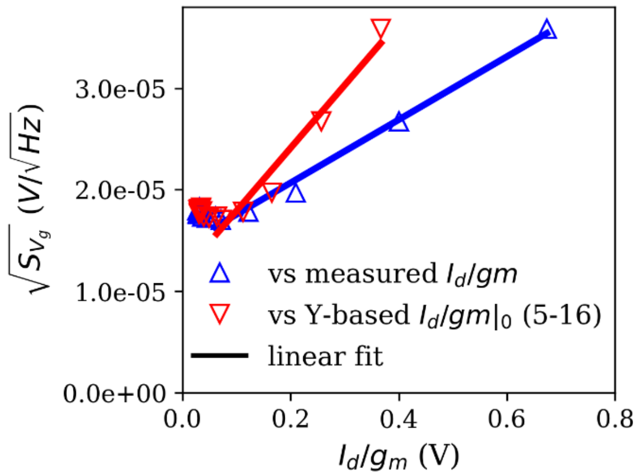

Figure 5-15: Square root of input-referred noise, √SVg, versus the measured ratio of drain current and transconductance, Id/gm, and the calculated one using eq. (5-18) along with the strong inversion linear fit based on eq. (5-14).

Table 5-I shows the extracted values of $N_t = S_{V_{FB}} WLC_{ox}^2 f / \lambda q^2 kT$ and Ω versus both the measured I_d/g_m and the R_{SD}-free $I_d/g_m|_0$ from eq. *(5-18)*. As it can be seen, there is a slight overestimation of N_t with the classical method. More importantly, the Ω component seems to be highly influenced by the I_d/g_m values used, as explained in part 5.2.2. In fact, the new Ω is more than two times higher, revealing a much more critical magnitude of the remote Coulomb scattering.

Table 5-I
N_T AND Ω EXTRACTED VALUES

	Measured I_d/g_m	$I_d/g_m\|_0$ as calculated by eq. *(5-18)*
N_t (eV/cm^3)	$5.13\text{x}10^{16}$	$3.36\text{x}10^{16}$
Ω (V^{-1})	2.15	5.29

5.3. Impact of Short Channel Effects on trap detectability

As already mentioned in chapter 2, apart from the 1/f component of LFN, random telegraph noise (RTN) is becoming one of the main noise sources for both digital and analog applications [121], [122], as single device behavior becomes more visible and important, with the downscaling of the transistor area. Although new technology steps, such as high-k dielectrics and aggressive length scaling, have paved the way for more compact devices, the resulting increased RTN can have significant impact on the device stability and reliability. The current fluctuations can not only contribute significantly on the total LFN in analog and mixed-mode circuits but they can also cause instability issues in digital circuits such as memories [123]. At the same time, RTN is a very powerful tool for defect characterization and reliability assessment of MOSFETs. It can be considered as a way to study interface properties as it is very sensitive to surface potential and carrier concentration [124]. This is thanks to its discrete signal levels, which correspond to the trap states (empty or filled), thus enabling a direct evaluation of the number of electrically active oxide traps [38]. This property of RTN is very crucial when performing statistical measurements that aim to extract the average number of traps per device, as well as the statistical distributions of RTN amplitudes and capture/emission time constants [125]–[127]. The precise extraction of the above characteristics is of critical importance, because the estimation of a circuit's or a system's dynamic performance (for memories [126]) or sensitivity (for sensors [128]) is heavily based on them.

A trap's occupancy is strongly dependent on the carrier concentration and thus on the gate voltage bias V_g [39], [129]. A trap can be easily observed if the polarization is such that the Fermi level lies a few kT from the trap energy level assuming that the RTN amplitude is sufficient to be detected [130]. More specifically, in order for a trap to be detectable the following requirements are necessary:

1. **Fluctuation amplitude, ΔI_d**: It has to be sufficiently large compared to the I_d (DC) level. This is the reason why in the majority of cases the relative amplitude $\Delta I_d/I_d$ is being considered.

2. **Trap Kinetics, $\overline{\tau_c}/\overline{\tau_e}$:** The trap should not be too slow or too fast compared to the measurement window (measurement duration and sampling frequency).
3. **Gate bias:** Small steps of V_g sweep are required, so that the point where the Fermi level becomes equal to the trap energy level can be detected. At this point, the activity of the trap is enhanced and so the number of RTN pulses is maximized, enabling a precise extraction of trap parameters.

Figure 5-16 shows an example of RTN, along with the trap characteristics that can be extracted from the time series (τ_c and τ_e) and the histogram (ΔI_d).

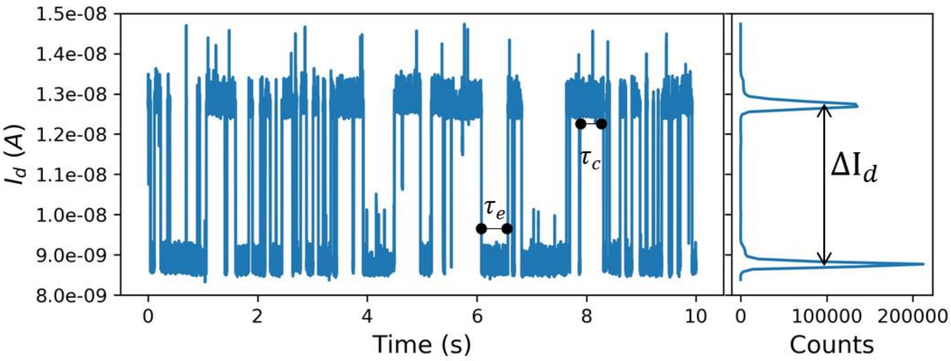

Figure 5-16: Example of RTN signal (Timeseries and histogram) along with the parameters that can be extracted.

Concerning the drain voltage, V_d, it has been reported that V_d has an impact not only on the trap time constants [37], but also on the relative RTN amplitude [37], [129]. Nevertheless, this effect has been mainly used for trap localization purposes, by taking advantage of the RTN amplitude asymmetry with V_{ds} in normal and reverse operation [38], [39], [124], and not for the detection of new traps, as it is assumed that all traps are already active for a given gate bias regardless the V_d value [127]. This might be true for channel lengths in the micro-meter region, which do not suffer from short channel effects, nevertheless in nanometer-length devices the charge uniformity from source (S) to drain (D) is significantly influenced by V_d. We claim that this effect may result in a very different RTN behavior that could presumably help identify more traps than in the case where measurements are done only under one drain voltage bias.

5.3.1. RTN in linear and saturation region of operation

To explore whether V_d measurements can enable the detectability of more traps, compared with the number of traps extracted in linear region of operation, we used Tri-Gate Nanowire SOI p-channel FETs, fabricated by CEA-LETI [131], as a test vehicle. They incorporate a buried oxide of 145 nm thickness, a H = 11 nm film thickness and a 2 nm Equivalent Oxide Thickness (EOT) HfSiON gate dielectric with TiN metal gate. The measured devices have a channel width of W= 30 nm and a channel length ranging from L_{ch} = 10 µm down to 10 nm, where the pinch-off, channel length modulation (CLM) and Drain-induced Barrier Lowering (DIBL) effects are enhanced [7].

To start with the experimental procedure, we chose devices with the minimum available channel length (L_{ch} = 10 nm) in order for the SCEs to be enhanced. Figure 5-17 shows the I_d-V_g curves at linear and saturation region of operation for one device (device #11). The DIBL condition in high V_d case (red line) is obvious, as the drain current values are way higher compared to the low V_d case, in the subthreshold region, due to the increased leakage current.

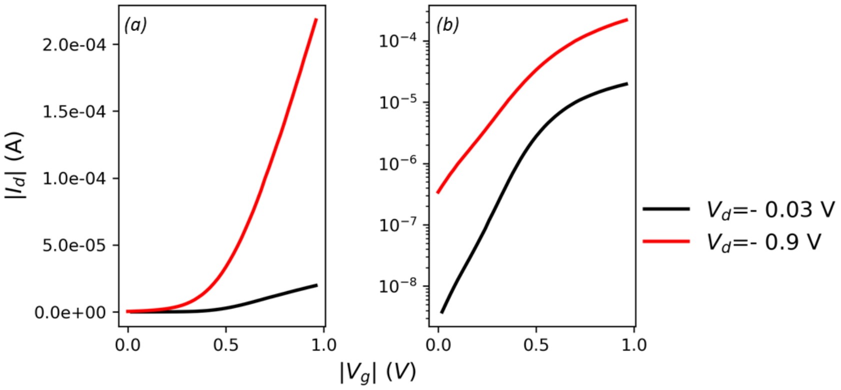

Figure 5-17: I_d-V_g characteristics in (a) linear and (b) logarithmic scale at linear and saturation region of operation.

In order to examine whether high V_d measurements could result to the detection of new traps, since the nanometer-length devices suffer from significant charge uniformity from source (S) to drain (D), we first pursued to LFN measurements in linear and then in saturation region of operation. Time domain measurements of I_d at linear region (V_d = - 30 mV) are shown in Figure 5-18, for three gate bias voltages, ranging from weak to strong inversion. As one can see in both the time series and the histograms, no RTN signals were observed.

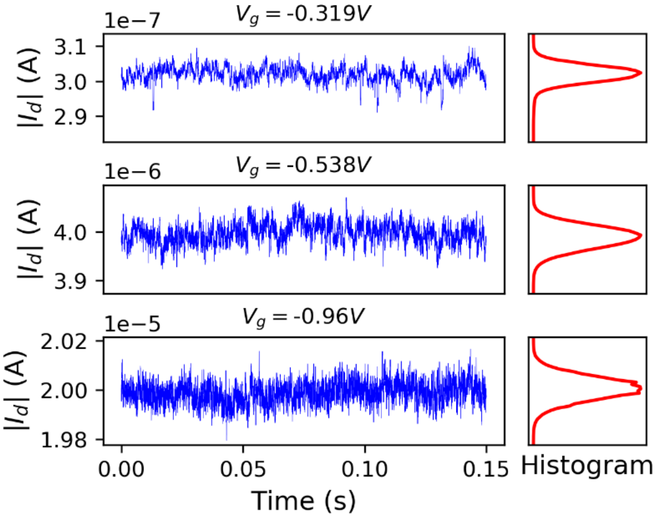

Figure 5-18: Device #11: Selected time-series and corresponding histograms for three gate voltage bias (from weak to strong inversion) in the linear region of operation (Vd = - 30 mV).

Nevertheless, this is not the case when the same device was biased in saturation regime, with the drain voltage at V_d = - 0.9 V. At least one clear two-state RTN can be detected as depicted in Figure 5-19.

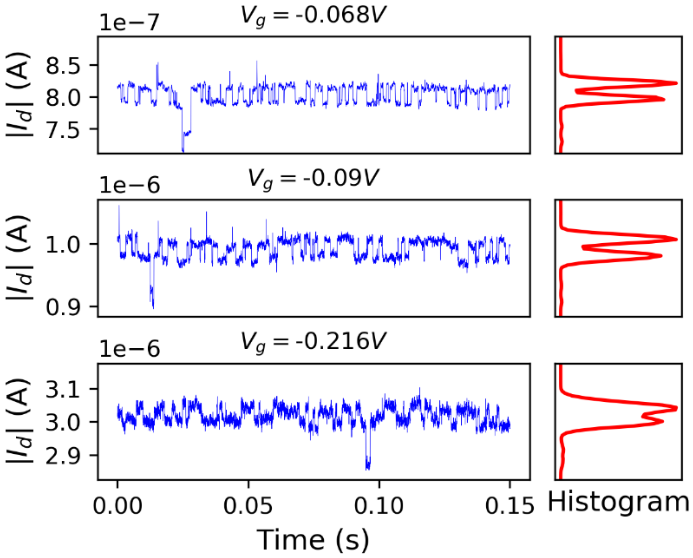

Figure 5-19: Device #11: Selected time-series and corresponding histograms for three gate voltage bias in the saturation region (Vd = -0.9 V).

Since the high voltage at the drain side changes the distribution of free carriers close to the drain, it becomes evident that the channel pinch-off near the drain has some kind of effect on the trap amplitude, or its kinetics (capture/emission time), such that the RTN signal becomes detectable. A possible explanation is that when such short channel devices go into saturation, the length of the pinched-off region becomes comparable to the total channel length, resulting in a radically different charge distribution [127]. There are two assumptions that can answer the question of what led to the detectability of the trap in the high V_d case. On one hand, the high V_d might result in an increase of the relative amplitude $\Delta I_d/I_d$, resulting in an amplitude level more important than the background noise, therefore making the trap more easily detectable. On the other hand, considering the trap kinetics (τ_c, τ_e), which are governed by the Shockley-Read-Hall statistics [37], [93] and given by eq. *(5-21)*, where σ is the capture cross section, v_{th} is the carrier thermal velocity, n_s the surface carrier concentration close to the trap, and n_1 the surface carrier concentration when the Fermi level, E_F, crosses the trap energy E_T, the high V_d can drastically change the trap occupancy, especially if the trap is located near the drain, resulting in the possible appearance of traps that were undetectable at low V_d within a given measurement time window.

$$\tau_c = \frac{1}{\sigma n_s v_{th}} \quad (a) \qquad\qquad \tau_e = \frac{1}{\sigma n_1 v_{th}} \quad \text{(b)} \qquad\qquad \textit{(5-21)}$$

In order to acquire a clearer view on how V_d influences the trap's detectability we can go deeper into details on the impact of V_d on trap kinetics and fluctuation amplitude. To do so we simulated a simple n- type FDSOI structure using Atlas SILVACO [104] with lightly doped silicon film N_A=1x10^{15} cm^{-3} and we extracted parameters related to trap's characteristics. The schematic of the structure as well as its dimensions are shown in Figure 5-20. It should be noted that the aim was not to simulate a structure identical to the experimental but to observe how trap's characteristics are influenced by the saturation regions in this example.

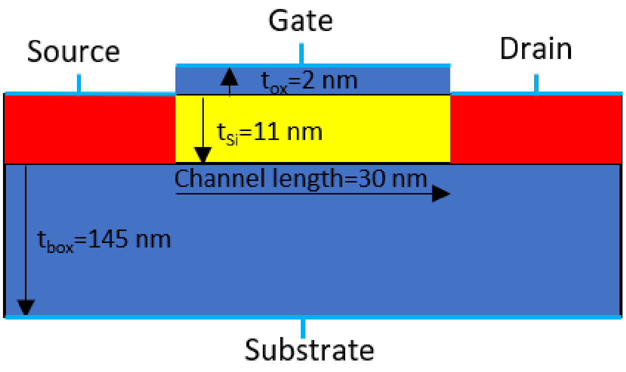

Figure 5-20: Simulated structure in Silvaco ATLAS TCAD.

A. Trap kinetics

For the observation of free carrier distribution in linear and saturation mode of operation, we used the horizontal cutline tool of Atlas to extract the electron concentration at a distance 0.12 nm from the oxide/silicon interface from source (x = 0) to drain (x = 30 nm) for different bias conditions. The result is shown in Figure 5-21, in which one can clearly observe that going from linear to saturation region can dramatically affect the carrier concentration in more than half the channel length, especially close to drain.

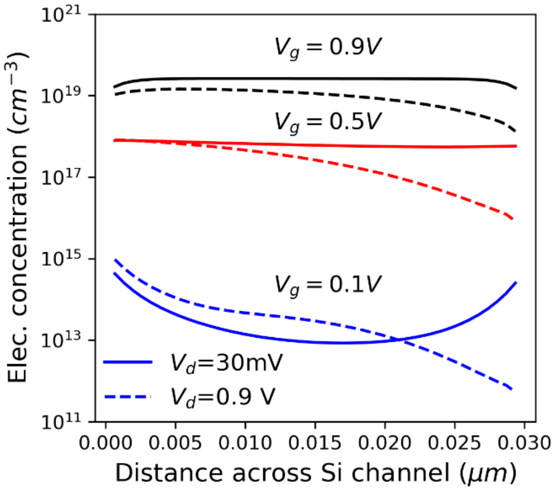

Figure 5-21: Simulated electron concentration across Si channel from Source (x = 0) to Drain (x = 30 nm) and 0.12 nm from the oxide/silicon interface for three gate bias and at both linear (Vd = 30 mV) and saturation (Vd = 0.9 V) regimes.

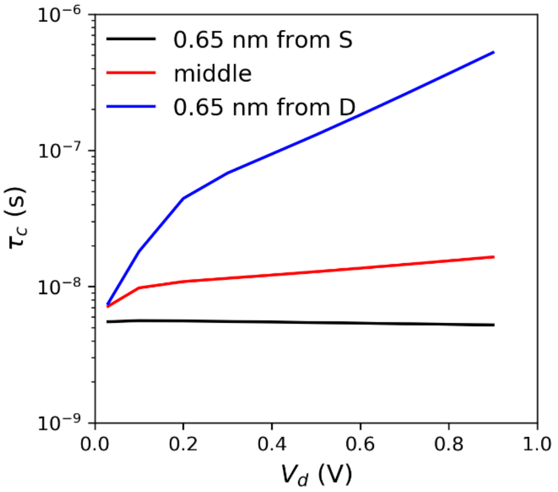

Figure 5-22: Calculated trap capture time using eq. (5-21a) and the simulation results of Figure 5-21 for 3 different trap positions inside the channel and 0.12 nm distance from the Si/SiO2 interface at V_g = 0.5 V.

This means that if a trap were located inside the silicon film at the same distance from the oxide layer, the dependence of its average capture time, based on eq. *(5-21a)*, with the drain voltage would be as depicted in Figure 5-22, for three different positions across the channel length and at V_g = 0.5 V (above V_t). For the calculation of capture time, through eq. *(5-21a),* we used typical values for electron thermal velocity, v_{th}=2.3x10^{7} cm/s and for the capture cross-section of an acceptor like trap, σ=1x10^{-17} cm^{2}.

Clearly, the trap's capture time may be affected by even two orders of magnitude when the trap is located inside the pinched-off region. This means that in the case of a very fast trap, which is usually the case for interface traps, if the trap is close to the drain side, measurements under high V_d would increase the capture time of the trap, which in turn will increase the effective time constant of the trap, $\tau = (1/\tau_c + 1/\tau_e)^{-1}$, allowing for its detection for a given sampling time and measurement window. On the other hand, an already slow trap in the linear region of operation close to the drain would be nearly impossible to detect in the saturation region from the drain side. This is also true when the trap is close to the source, in which case measurements under high V_s (with grounded D) should be performed. To conclude, in certain cases, measurements at the saturation region of operation might lead to an easier detection of a trap.

It should be noted that for this study we considered the emission time of the trap constant and independent of V_d. Thus, it provides a simplistic explanation of the change of time constant with V_d. In reality the strong energy band bending due to high V_d can change the Fermi level and so the activation energy, and finally the cross section will be affected, which in turn will impact both τ_c and τ_e [52].

B. RTN amplitude

Regarding the RTN signal amplitude $\Delta I_d/I_d$, its dependence on V_d is directly related to the position of the trap. In the saturation region from the drain side, the pinch-off phenomenon becomes dominant for a trap close to the drain, and it might be undetectable due to its very weak RTN amplitude. To demonstrate this effect, since Atlas does not provide a single trap module, we added on our simulated device an interface acceptor trap using the *inttrap* statement, with its concentration and area to be combined so as the fluctuation of the charge density to be around twice the elementary electron charge, q. We ran the simulation once with no traps present, so as to have the ideal I_d, and then we added the trap in different positions. We chose the trap energy level to be close to the valence band that it is always filled regardless the polarization conditions. Figure 5-23 shows the CNF/CMF application of the simulated $\Delta I_d/I_d$ for a trap in the middle of the channel in the linear region of operation, $V_d = 30$ mV. The flat-band voltage fluctuation, ΔV_{FB}, was extracted to be 9.6×10^{-3} V. In addition, two different positions of the trap were considered: one at the middle of the channel and one with a 2.5 nm distance from the drain region. An abstract illustration of the trap position is shown in Figure 5-24. Moreover, two bias conditions were examined: the typical one with varying V_d and a complementary with varying V_s and grounded D. The simulated relative amplitude versus $V_{d,s}$ is shown in Figure 5-25. The behavior of the normalized RTN amplitude with $V_{d,s}$, in this figure, agrees with the results by Fang et al. [129]. Also, Figure 5-26 shows the electron concentration inside the channel when polarizing from the drain and the source side.

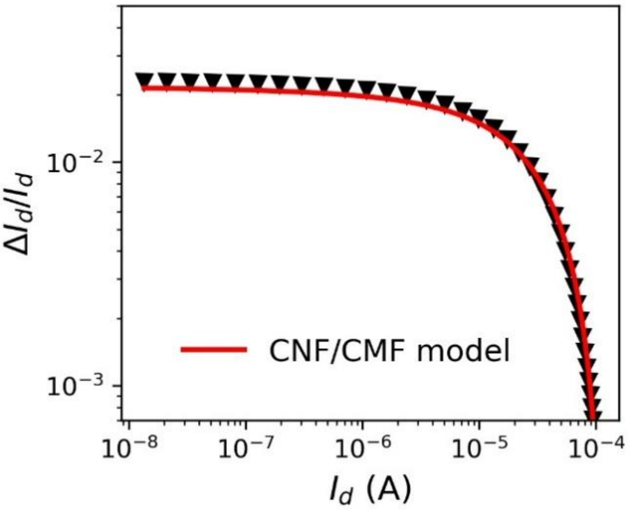

Figure 5-23: Simulated normalized RTN amplitude, $\Delta I_d/I_d$, versus Id for a trap located in the middle of the channel along with the CNF/CMF model

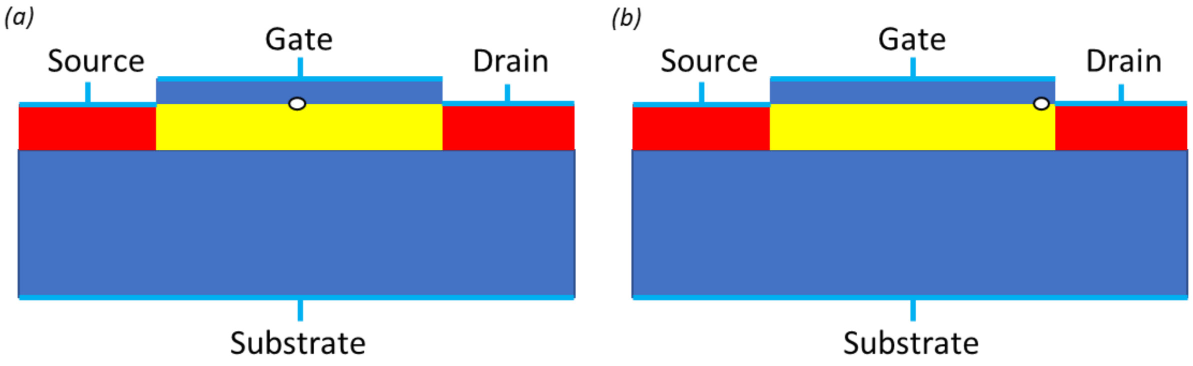

Figure 5-24: Simulated structure in Atlas-Silvaco with (a): trap in the middle and (b): trap close to drain, (not in scale).

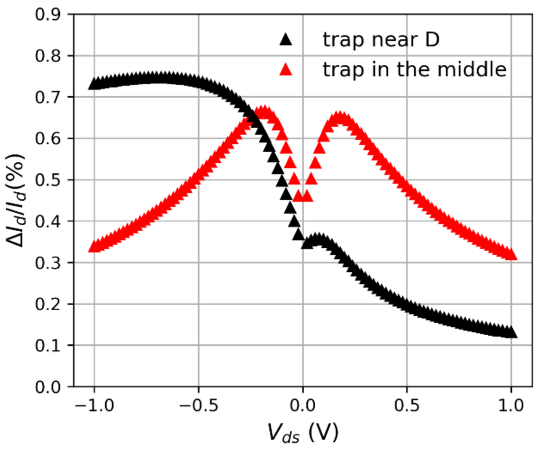

Figure 5-25: Simulated normalized RTN amplitude $\Delta I_d/I_d$ versus drain-source voltage for V_g = 0.5 V (W = 1 µm, L_{ch} = 30 nm).

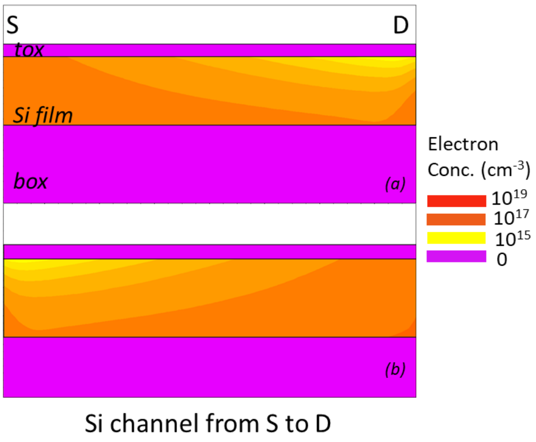

Figure 5-26: Electron concentration inside the channel. (a) when polarizing from drain, (b) when polarizing from source for $|V_{d,s}|$ = 1 V, V_g = 0.5 V, (W = 1 µm, L_{ch} = 30 nm).

It is shown that when the trap is in the middle of the channel, the amplitude $\Delta I_d/I_d$ is the same whether the channel pinch-off takes place at the source or at the drain side. This is not true however, when the trap is close to the drain, where a very important difference in $\Delta I_d/I_d$ is observed: with the reverse $V_{d,s}$ polarization, the RTN amplitude gets amplified and reaches a maximum after saturation, which is almost 7 times higher than when biasing with the same voltage at the drain side (pinch-off near D). Therefore, complementary measurements at reverse $V_{d,s}$ conditions (pinch-off near S) could lead to an easier detection of traps near the drain. Vice-versa, traps near the source region would be easier to detect at high $V_{d,s}$ bias. Another interesting fact is that in the linear region of operation the RTN amplitudes $\Delta I_d/I_d$ are comparable for all 3 trap positions. This means that even if a RTN signal was detectable in terms of amplitude, it could be part of a multi-level RTN signal consisting of all these active traps. If we had not taken this issue into consideration, we would have been falsely led to the conclusion that only a single trap exists which in turn would lead to a false evaluation of the oxide/silicon interface quality. Hence, a combination of both linear and saturation regimes (at both D and S sides) is necessary for a complete trap activity monitoring.

Considering also the Figure 5-26, it is quite interesting to relate the electron concentration inside the channel with the normalized RTN amplitude. It seems that the more depleted a region is, the less sensitive to trapped charges becomes. This is due to the fact that in the case of high $V_{d,s}$, the channel is not uniformly distributed anymore. It is actually mostly concentrated near the source side and so the electrostatic impact of a trap close to drain on the average carrier concentration becomes negligible. The same behavior is valid for the high $-V_{d,s}$ case.

Of course, the behavior of $\Delta I_d/I_d$ with V_d or V_s presented in Figure 5-25 is for specific V_g-V_t value and it does not mean that it will be the same at a higher V_g. To show that, we ran the same simulations described above but this time V_g was chosen to be 1 V. The result is shown in Figure 5-27, with the electron concentration at $V_g = 1$ V and $V_{d,s} = \pm 1$ V to be depicted in Figure 5-28. At the high V_g case we see that the relative amplitude is reduced in all cases, compared to $V_g = 0.5$ V case, which is due to the g_m/I_d reduction in strong inversion region as shown in Figure 5-23.

For this very short channel device, we see that not only the RTN amplitude of a trap close to drain is degraded but also the one resulted from a trap in the middle of the channel. This is due to the fact that the pinch-off and CLM effects are so enhanced, in this case, which extend the depletion region to more than half the channel length. To see the behavior of a longer channel device, we repeated the same simulations for a channel length equal to L_{ch} = 0.4 μm, at $V_g = 0.6$ V. As one can observe in Figure 5-29, the trap in the middle of the channel gives the higher RTN amplitude. This behavior is in agreement with the work of *A. Asenov et al.* [123], who showed that for a V_g value close to the threshold voltage the trap in the middle of the channel gives the higher RTN amplitude regardless the V_d value.

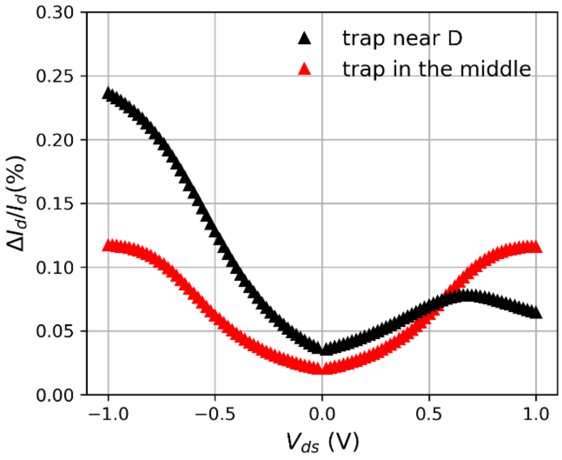

Figure 5-27: Simulated normalized RTN amplitude $\Delta I_d/I_d$ versus drain-source voltage for V_g = 1 V (W = 1 μm, L_{ch} = 30 nm).

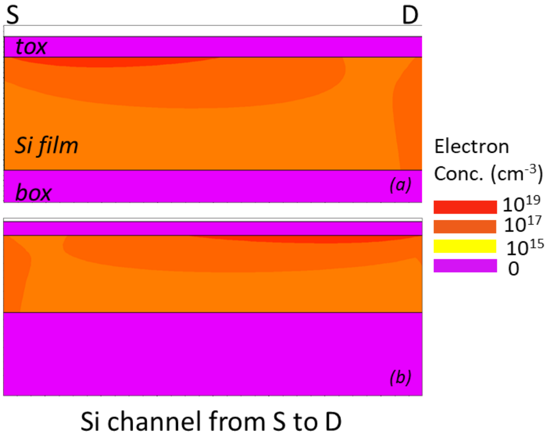

Figure 5-28: Electron concentration inside the channel. (a) when polarizing from drain, (b) when polarizing from source for $|V_{d,s}|$ = 1 V, V_g = 1 V, (W = 1 μm, L_{ch} = 30 nm).

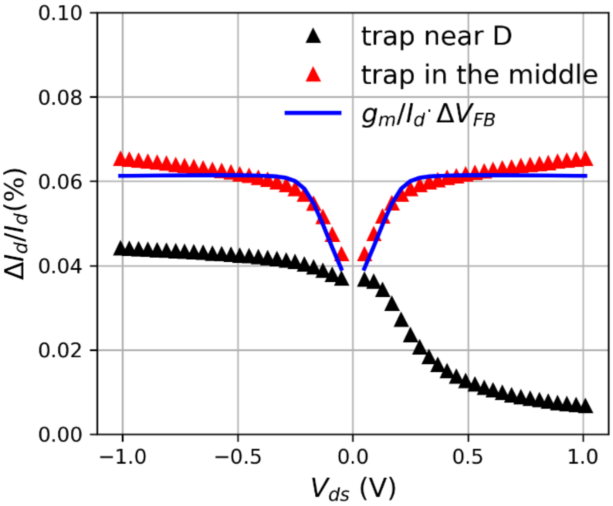

Figure 5-29: Simulated normalized RTN amplitude $\Delta I_d/I_d$ versus drain (closed symbols) and source (open symbols) voltage for V_g = 0.6 V (W = 1 μm, L_{ch} = 0.4 μm).

Moreover, Figure 5-29 shows the application of the CNF model, $\Delta I_d/I_d=(g_m/I_d)*\Delta V_{FB}$, in which g_m was calculated at V_g = 0.6 V. As it is depicted, the CNF model approaches the RTN amplitude (except for some deviations in the saturation region) only for a trap in the middle of the channel. This means, that it would be impossible to properly fit the CNF model and extract the trap's depth if it's located close to drain or source at a $V_{d,s}$ higher than 0.01 V. This issue will become worse in even shorter devices, in which -as we showed- the RTN amplitude for a trap in the middle of the channel is attenuated. Hence, we proved that there is a need of RTN amplitude model expression that accounts not only for the vertical position, as shown in [53], but also for its horizontal position from source to drain, as a function of $V_{d,s}$.

As explained, the attenuation of RTN amplitude is more enhanced in short channel devices, where the pinch-off and CLM effects are dominant. Consequently, one would expect that going from short to longer channel devices, this dramatic change of RTN amplitudes in saturation regime would no longer exist. To investigate the impact of channel length on the way that the pinch-off effect affects the RTN amplitude, we simulated the $\Delta I_d/I_d$ at saturation (V_d = 1 V) in the strong inversion region at the same V_g-V_t for four channel lengths, L_{ch} = 30 nm, L_{ch}= 60 nm, L_{ch} = 0.2 µm and L_{ch} = 0.4 µm, and three positions of the trap across the channel: near S, in the middle and near D. The length-normalized drain current and $\Delta I_d/I_d$ results are shown in Figure 5-30 and Figure 5-31 respectively.

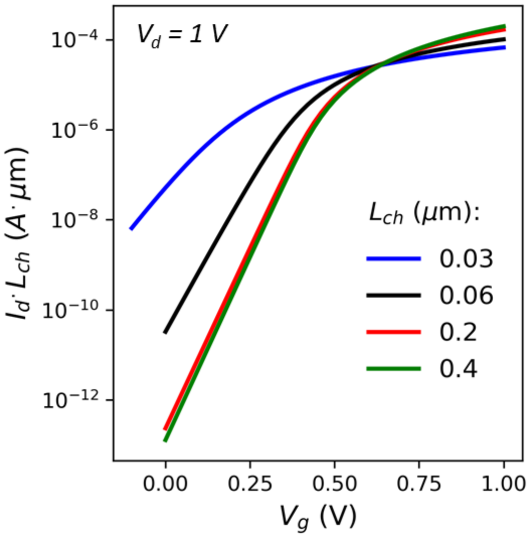

Figure 5-30: Simulated I_d versus V_g curves in saturation region of operation (V_d = 1 V) for different channel lengths.

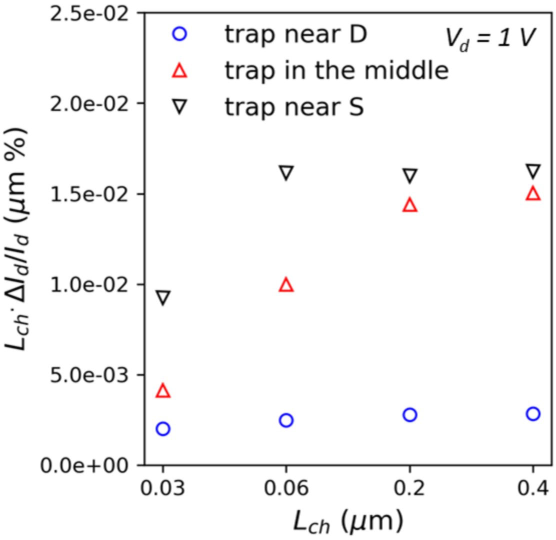

Figure 5-31: Simulated length-normalized relative RTN amplitude versus channel length for three trap positions, biased at V_d = 1 V and V_g-V_t = 0.45 V.

As expected, for channels longer than 100 nm, where the SCEs are not so severe, the RTN amplitude attenuation effect is observed only for the traps near the D, where the pinch-off effect is taking place. The traps in the middle and near the S have approximately the same electrostatic impact on the RTN amplitude, as the length increases. It's also interesting to note that for the traps near the S, there is an amplitude attenuation observed in extremely short channels (L < 50nm) compared to longer ones, which we can be attributed to the DIBL effect (visible in the I_d-V_g curves).

5.3.2. Proposed “Pinch-to-Detect” method

Based on the above analysis (Section 5.3.1), we propose a measurement procedure consisting of three sets of bias conditions: linear region (low V_d), saturation with pinch-off near the drain (high V_d), and finally saturation with pinch-off near the source (high V_s, V_d = 0V). Each time, the gate bias varies from weak to strong inversion. To further demonstrate the importance of performing the additional source saturation measurements, we compared the behavior of Device #11 under high V_s, (Figure 5-32), against the one under high V_d (Figure 5-19). From the obvious difference concerning the histograms -and thus the trap’s occupancy-behavior with V_g between high V_d and high V_s, it is concluded that these are two different traps which became detectable thanks to LFN measurements under saturation conditions. Of course, intermediate values of V_d and V_s, between linear and saturation mode, may further help to achieve an even higher number of traps, but the method we propose is more realistic for full-wafer statistical measurements.

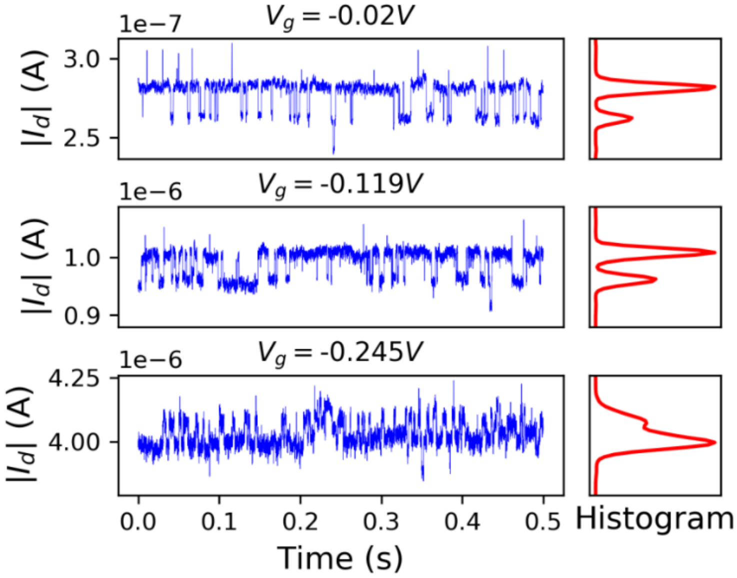

Figure 5-32: Device #11. Selected time-series and corresponding histograms for three gate voltage bias (from weak to strong inversion) in saturation region, but with the pinch-off at the source side (V_s= -0.9 V).

We applied this triplet of measurements, from weak to strong inversion, on a set of 36 devices across the wafer and we compared the number of traps detected in each mode of operation. In Figure 5-33, it is illustrated how different is the number of detected RTN traps per die for each bias condition. Combining all the results, the total number of detected RTN traps can be increased even by 2. Therefore, the combination of all three sets of measurements can provide a much more reliable estimation and at the same time maximize the total number of detected RTN traps.

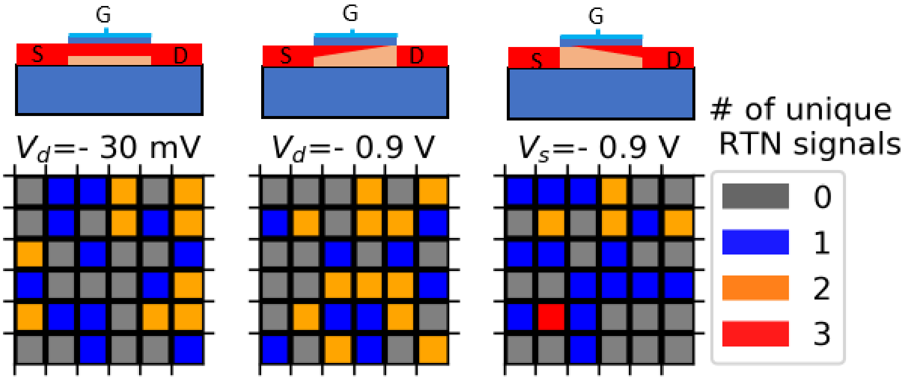

Figure 5-33: Number of detected RTN traps for all three measurement sets of our proposed methodology.

In addition, the significant differences in the spectra of the input-referred gate voltage noise, S_{V_g}, as shown in Figure 5-34, further confirm the importance of the complementarity of these measurements. The presence of several Lorentzian (1/f^2 slope at high frequencies) spectra in both saturation modes but not in the linear region of operation confirms the presence of new traps, thus the possibility to detect new traps. Moreover, while the mean and median spectra are both 1/f-like and almost coinciding for the linear regime, for both high V_d and high V_s cases the mean spectrum is non-1/f and heavily influenced by the presence of additional traps, whereas the median is the same as in the linear region. This shows that in saturation region there is a lack of uniformity in the distribution of active traps. We assume that this effect may be related to traps near the source or drain junction regions or below the spacers, that are activated or detected only in the saturation regime.

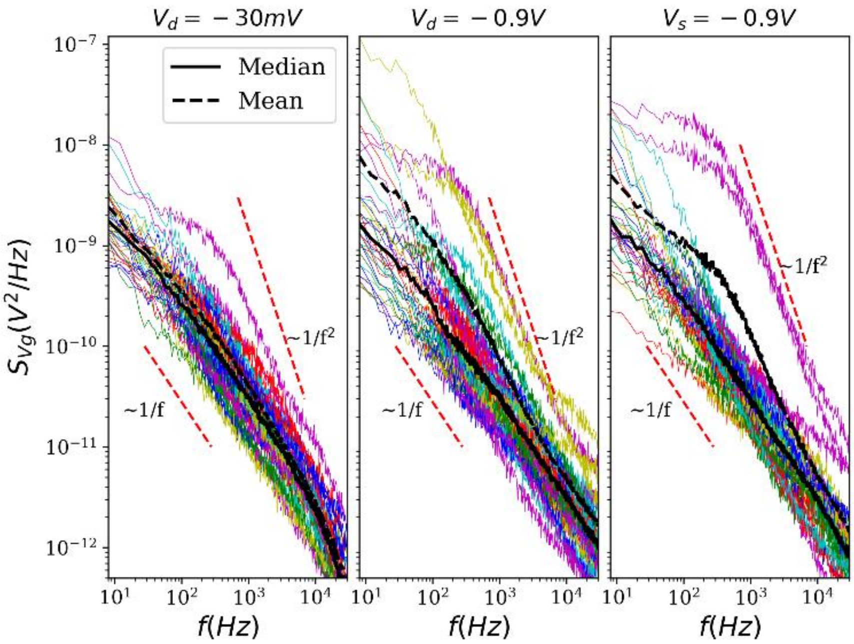

Figure 5-34: Input-referred gate voltage noise, S_{Vg}=Sid/gm^2, for all dies and for all three measurement sets of our proposed methodology at |V_g - V_t| =0.4 V. A significantly different behavior is observed in both median level and spectral characteristics.

5.4. Summary

In this Chapter, we focused on short channel devices, and more specifically on the way that the LFN and RTN characterization is affected by the SCEs. Firstly, the impact of R_{SD} on the extraction of LFN parameters and especially on the Ω coefficient has been investigated. It has been found that the degradation of g_m/I_d due to the presence of R_{SD} leads to the unreliable extraction of the Ω coefficient. Based on this finding, a detailed analysis on the impact of mobility attenuation factors on noise parameters has followed, proving that although the $\theta_{1,0}$ and θ_2 coefficients are well accounted for by the CNF/CMF model, the impact of R_{SD} on the I_d/g_m ratio, when studying the mobility fluctuations due to trapped charges, is not taken into consideration. For this reason, a complete R_{SD}-immune method has been proposed and applied on short-channel FinFETs, allowing the reliable extraction of LFN parameters. In addition, it has been demonstrated through measurements and TCAD simulations, that in the nanometer length MOSFETs, the pinch-off effect occurring in the saturation region of operation plays a critical role in the detection of RTN traps. It was shown that this is related to the channel uniformity across the device length which can influence the RTN amplitude and kinetics. Consequently, we proposed the “pinch-to-detect” method that takes advantage of this effect in order the number of detectable RTN traps to be maximized and therefore provides a more complete device reliability characterization.

CHAPTER 6

Modeling of Lorentzian type Noise for Accurate Simulations of Trap-related Noise in CMOS circuits

6.1. Introduction

As already mentioned, apart from the increase of LFN level due to smaller area devices, other kinds of LFN, different from the 1/f trend with Lorentzian spectra, have made their appearance due to defects that resulted from new materials and process techniques. This type of power spectral density (PSD) shape may originate either from oxide trap-related random telegraph noise (RTN) signals (leading to 1/f in large area oxides) or generation recombination (GR) centers in the MOSFET channel region, as described in Figure 6-1.

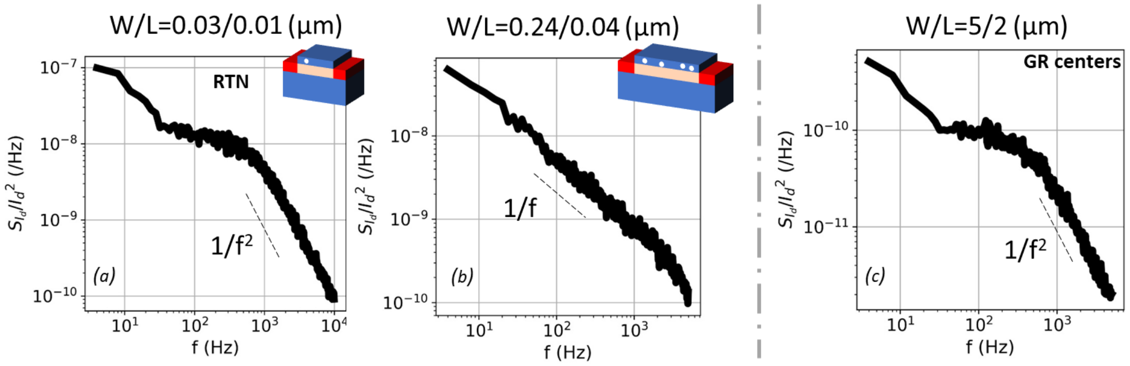

Figure 6-1: Normalized drain current power spectral densities versus frequency. (a): PSD originated by a single trap which takes the shape of (b) when many traps are present, (c): PSD originated by GR centers.

Regarding the device-based performance, this peculiar LFN behavior has increased by a great extent the variability. The significant trap number variations from device to device due to small area or GR centers has enhanced the static and dynamic variability, which has led to further limitations in device performance and reliability [61]. Inevitably, these limitations concern the safe operation of a whole circuit, as it has been reported that LFN has a major impact on both digital and analog circuits [29], [41]. More specifically, in the case of SRAMs, the presence of RTN limits the minimum supply voltage, V_{dd}, due to V_t shifts. In addition, studies have shown that depending on the time that a current spike due to RTN occurs, there might be a delay or even errors in the write operation [29]. Apart from digital circuits, RTN can degrade the accuracy of sensors like in the case of CMOS image sensors in which RTN is responsible for the blinking and twinkling pixels in videos under low light conditions [27]. Finally, LFN has attracted the interest from the RF design community, as it can be up-converted to higher frequencies and thus affect the operation of MOSFETs in RF applications [132]. A characteristic example is the case of ring oscillators (RO), in which LFN is up-converted to phase noise around the oscillation frequency [133].

Since it is undoubtable that LFN, and especially RTN, can have severe impact on the reliable and safe operation of circuits, its accurate modeling is crucial and indispensable. While various works have been presented on the time-domain modeling of the RTN effect for circuit simulators [29], [41], there are very few that concern the modeling of Lorentzian noise sources directly in the frequency domain [134]. The latter could, on one hand, significantly reduce the noise simulation time, and on the other hand enable a direct and accurate simulation of the PSD for circuits, where the noise is important to be studied in the frequency domain such in the case of oscillators or analog signal processing. Moreover, the pre-existing PSD modules in Verilog-A are limited to 1/f and white noise, therefore the Lorentzian type of noise needs a dedicated module to be developed.

In this Chapter, we present a method we developed for the implementation of Lorentzian noise spectra in Verilog-A (details in $6.2.1), in a way that can automatically generate Lorentzian or 1/f noise spectra depending on the trap density and oxide area, for all bias conditions. We named our modeling approach “VERILOR”, to combine both the “Lorentzian” and “Verilog-A” terms and make it easy to be referenced when used by other scientists or circuit designers. After underlining the advantages of Lorentzian modeling with regards to 1/f and time domain modeling of RTN, with the help of a Lambert-W function charge-based drain current model [114], we demonstrate our module’s applicability in circuit simulators, and how it can enable precise noise variability studies at a circuit level. Finally, some circuit noise application examples are shown, revealing for example how a ring oscillator's (RO) phase noise can be affected in the presence of a Lorentzian-type PSD. Both the device- and circuit-level noise simulations were performed with the Cadence Spectre simulator [135].

6.1.1. Importance of Lorentzian Noise Modeling

As already mentioned, the miniaturization of the devices increases the probability of the existence of very few traps -in some cases just one- as opposed to large oxide areas where there are hundreds or thousands of defects. In this case the main LFN source stops being 1/f-like but instead appears a Lorentzian-like dependence: plateau at low frequencies and $1/f^2$ dependence above a certain cut-off frequency f_c, as described in eq. *(6-1)*, where $S_{V_g}(0)$ is the plateau at 0 Hz.

$$S_{V_g}(f) = \frac{S_{V_g}(0)}{1 + (f/f_c)^2} \tag{6-1}$$

In many publications, RTN is modeled in the time domain. The advantage of this method is that the state of a circuit can be accessed at any time and so possible errors due to RTN can be examined. However, concerning variability studies or multiple RTN traps with huge spans of time constants, transient circuit simulations can take very long, while the situation becomes even more difficult when increasing the number of components in a circuit. To overcome time-consuming issues, but also be able to directly perform noise spectrum simulations, the need for RTN modeling in the frequency domain emerges. To do so, the authors of some publications use the LFN variability level, $\sigma(\log(S_{Vg}))$, extracted from experiments or models and add the +/- 3σ to the 1/f average spectrum [136], [137], in an effort to cover the extreme LFN level variations induced by RTN. By doing this, although the safe design of a circuit in terms of LFN is succeeded, the LFN level itself might be significantly overestimated or underestimated. To outline this phenomenon, we tested this methodology using our experimental data [138]. The presented experimental results are from measurements performed on Tri-Gate Nanowire SOI p-channel FETs, fabricated by CEA-LETI [131]. They consist of a 145 nm thick buried oxide, a Si film of H = 11 nm and a 2 nm Equivalent

Oxide Thickness (EOT) HfSiON gate dielectric with TiN metal gate. We show in Figure 6-2 a set of 93 experimentally measured input- referred gate voltage noise spectra at $|V_g|= 1$ V, along with the +/- 3σ limits added to the average 1/f, with $\sigma(\log(S_{Vg}))$ extracted at 20 Hz. We chose a very small gate area device, $W_{eff}/L= 52/40$ nm, so as to purposefully increase the noise variability and the probability of RTN traps appearance. As shown in Figure 6-2, the +/- 3σ spectra fails to accurately estimate the maximum and minimum extreme conditions. In addition, when the 1/f is used to predict LFN variability, the frequency at which the standard deviation is extracted is important since, as it is shown in Figure 6-3, σ is not necessarily constant with frequency nor gate bias, as this depends on the energy and spatial distribution of traps.

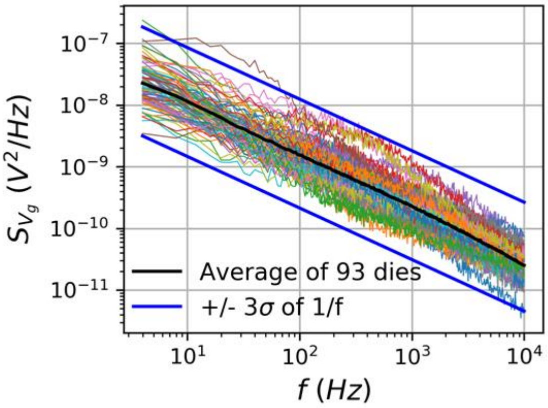

Figure 6-2: Measured imput-referred gate voltage noise spectra on TriGate Nanowire MOSFETs, plotted together with the log-mean spectrum and the +-3σ 1/f spectra based on the 1/f variability modeling. (W_{eff}=52 nm, L=30 nm, $|V_g|$= 1 V, $|V_d|$=30 mV).

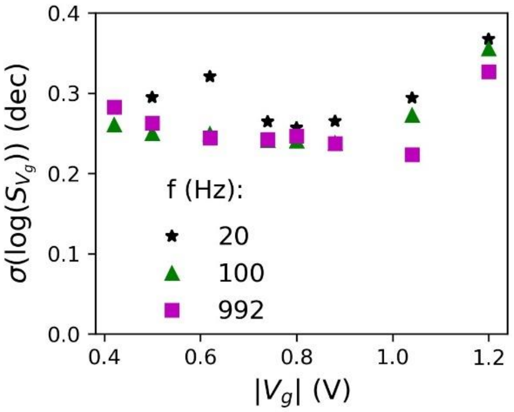

Figure 6-3: Input-referred gate voltage noise standard deviation value versus gate voltage at room temperature for different frequencies, 20, 100 and 992 Hz.

Moreover, for better prediction of LFN variability, what is even more important is not the value of the PSD at a certain frequency, but the total noise power of the fluctuations for each die calculated by integrating the PSD over the whole frequency range, as expressed in eq. *(6-2)*. For this reason, the maximum and the minimum total noise power for both the experimental and +/-3σ of the average 1/f data was calculated using eq. *(6-2)* for a bandwidth of 1 kHz and the results are shown in Figure 6-4.

$$\sigma_{Vg}^2 = \int_{f_{min}}^{f_{max}} S_{Vg}\, df \tag{6-2}$$

In Figure 6-4, one can clearly observe the huge difference of total noise power between the experimental data and the 1/f-based variability model for both the maximum and minimum cases. This is an indication that for such downscaled devices the 1/f model cannot accurately describe neither the experimental variability nor the noise power, as a consequence of the increased number of devices which show Lorentzian spectra. Therefore, new modeling approaches should be developed which take into consideration the probability and behavior of RTN and GR signals.

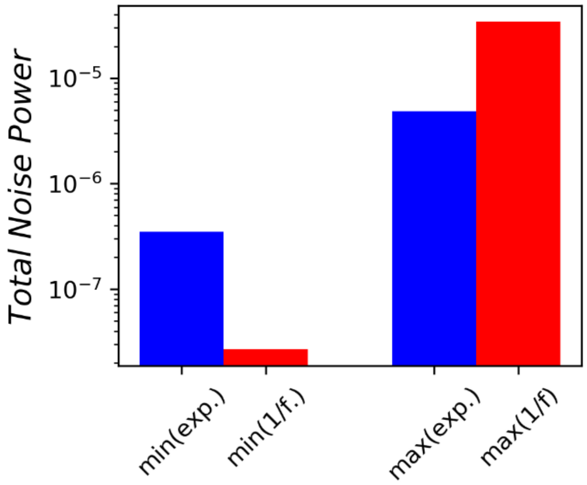

Figure 6-4: Experimental (blue) minimum and maximum noise power along with the +/- 3σ power of 1/f variability model in red.

The difference in noise power shown in Figure 6-4 can be nonetheless understood, if we take as an example the expected noise power of a 1/f and a Lorentzian spectrum that coincide at 10Hz, a typical frequency for the extraction of characteristic noise levels, as shown in Figure 6-5a. Combining eq. *(6-1)* and *(6-2)* the Lorentzian spectrum integral can be calculated and expressed through eq. *(6-3)*. Similarly, for the 1/f type of noise whose spectral density is $S_{V_g}(f) = S_{Vg}(1)$/f, where $S_{Vg}(1)$ is the 1/f PSD value at 1 Hz, the spectrum integral is given by eq. *(6-4)*. Based on these equations, we extracted the total noise power for each type of spectra and for different bandwidths. The results are shown in Figure 6-5b. It is worth noting that, while the Lorentzian PSD amplitude is 2 orders of magnitude below 1/f at the lower and the higher edges of the bandwidth, the total noise power of the Lorentzian spectrum becomes significantly higher (1 order of magnitude), even for a bandwidth equal to its cut-off frequency, f_c. Of course, this behavior would be different if we had chosen a different level of Lorentzian spectrum compared to the 1/f one.

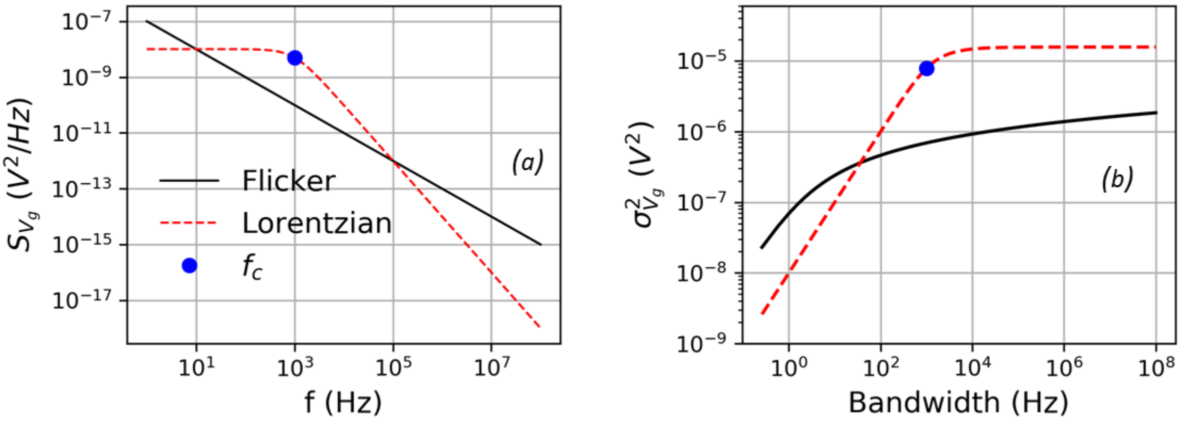

Figure 6-5: (a): 1/f and Lorentzian spectra, with f_c at 1 kHz, that coincide at 10 Hz, (b): total noise power of the spectra shown in (a).

$$\sigma^2_{Vg,Lor} = S_{Vg}(0) f_c \left(\tan^{-1}\frac{f_{max}}{f_c} - \tan^{-1}\frac{f_{min}}{f_c}\right) \qquad (6\text{-}3)$$

$$\sigma^2_{Vg,Flick} = S_{Vg}(1) ln(f_{max}/f_{min}) \qquad (6\text{-}4)$$

This is another confirmation that the 1/f model fails to emulate the behavior of a Lorentzian spectrum, this time in terms of total noise power. In large area devices, this disagreement is not a significant issue due to high number of traps, which eventually will give a 1/f like PSD, but since more downscaled devices are being used, in which the probability of single trap appearance is increased, no reliable estimations can be concluded concerning the safe operation of circuits. Consequently, specific modeling of a Lorentzian type noise is needed that can describe accurately single trap or GR behavior. Of course, the combination of 1/f and Lorentzian noise can give a more realistic results for variability studies as both types of noise can be present.

6.1.2. Lorentzian PSD Level Generator

We proceed to emulate the experimental variability using a PSD level generator, that considers a Lorentzian noise spectrum for each RTN fluctuator and calculates the overall noise of each die by adding the PSDs of each trap through eq. *(6-5)*, where the electrostatic impact of each trap “k” on the threshold voltage, $\Delta_{Vt,k}$, is expressed through eq. *(6-5)* as presented in [139]. $N_{T,d}$ is the total number of active traps for die ‘d’, k the trap number index, ΔV_t the RTN amplitude depending on the position of the trap inside the oxide, for which we considered uniform distribution of traps inside the whole oxide depth, A the space mark ratio, τ_c and τ_e the mean capture/emission time constants of each trap. N_T was chosen for every die from a Poisson distribution with an average $<N_T> = N_t W L t_{ox} \Delta E$, where N_t the oxide trap density per volume per energy and ΔE the total energy bandgap.

$$S_{Vg}(f)_d = \sum_{k=1}^{N_{T,d}} \frac{4\Delta V_{t,k}{}^2 A_k \tau_k}{1 + (2\pi f \tau_k)^2} \quad (a)$$

(6-5)

$$\Delta V_{t,k} = \frac{q(1 - x_{t,k}/t_{ox})}{WLC_{ox}}, \qquad A_k = \frac{\tau_k}{\tau_{c,k} + \tau_{e,k}}, \qquad \tau_k = \left(\frac{1}{\tau_{c,k}} + \frac{1}{\tau_{e,k}}\right)^{-1} \quad (b)$$

Moreover, for the calculation of τ_c and τ_e we implemented a simplified SRH-like approach. Based on the SRH statistics and according to [93], a more general expression of τ_c and τ_e has been developed for a single trap that also accounts for quantum confinement effects in very thin Si films. The new expressions are given below, eq. *(6-6)*, where f_e is the escape frequency (≈ $2\text{x}10^{13}$ Hz), ε_{ox} the oxide permittivity, Q_i the inversion charge at a specific V_g, Q_{it} the inversion charge when the Fermi level E_f crosses the trap energy E_t, Q_d the depletion charge and x_t the trap depth inside the oxide. The extraction of time constant was based on these equations since through the utilization of the Lambert-W function charge-based drain current model [114], Q_i can be easily calculated.

$$\tau_c = \frac{q}{\sigma f_e Q_i} \quad (a)$$

(6-6)

$$\tau_e = \frac{q e^{\frac{x_t(Q_i + Q_d)}{kT\varepsilon_{ox}}}}{\sigma f_e Q_{it}} \quad (b)$$

In order for the randomization of traps’ characteristics in terms of energy and cross-section to be introduced in a simplified way, we use a bias-independent parameter τ_0, which is exponentially distributed between 1 ns and 1 ks so as both fast and slow traps to be accounted for. Actually, this constant includes the variation of σ for different traps. Consequently, eq. *(6-6)* was modified and the expressions for the time constant for the Lorentzian PSD generator are given through eq. *(6-7)*. It should be noted that for simplification reasons, x_t was not accounted for in the emission time calculation but only in the Lorentzian amplitude. In addition, for both capture and emission time constants, we used as a reference the inversion charge at V_t so as the ratio $Q_i(V_t)/Q_i$, to take realistic values of the operating conditions as the $Q_i(V_t)$ could be considered close to the average value of Q_i between weak and strong inversion. If a value of Q_i at a different bias, closer to 0 or 1 V, was chosen the time constants would be shifted to lower or higher values, and thus considering faster or slower traps respectively. Finally, for the extraction of Q_{it}, which is a characteristic of a trap independent on V_g, a random uniformly distributed value is chosen between $\ln(Q_i(0))$ and $\ln(Q_i(1.2))$. We took the logarithm of Q_i due to the exponential dependence of Q_i on V_g in the sub-V_t region and so equal probabilities to be given in the whole range of Q_i for the definition of Q_{it}. Finally, we considered the Q_i for a V_g range from 0 to 1.2 V with V_{dd} at 1 V, as a trap can be active for a range of +-3kT/q from its energy level. Figure 6-6 shows two examples of a slow and fast trap with time constants calculated using eq. *(6-7)*.

$$\tau_c(V_g) = \tau_0 \frac{Q_i(V_t)}{Q_i(V_g)}, \qquad \tau_e(V_g) = \tau_0 \frac{Q_i(V_t)}{Q_{it}} \tag{6-7}$$

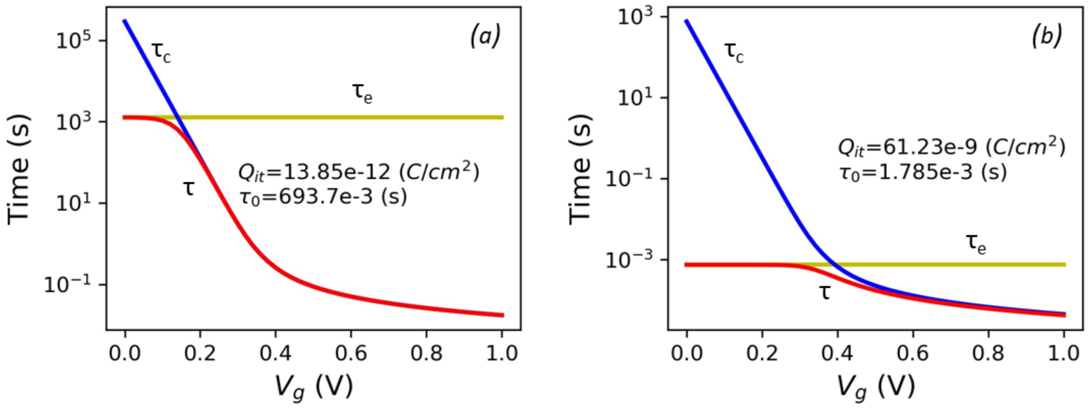

Figure 6-6: Trap's time constants versus V_g, calculated by eq. (6-7), for two different cases of Q_{it} and τ_0.

6.1.3. Model Validation

One way to test how well a model follows the statistically varied experimental data is to compare the quantile-quantile (Q-Q) plots. Q-Q plot is a graphical tool that allows assessing whether different set of data come from the same distribution such as normal, uniform or exponential. For this reason, the set of data is plotted versus generated values that follow a known distribution, and if the result is a straight line, then the distribution of the dataset can be derived. In many works, it has been proven that the distribution of noise spectral density follows the log-normal statistics and this is a direct consequence of the exponential distribution of the trap time constants [140], [141]. As a result, when referring to noise variability, statistical analysis of the log(S_{V_g}) should be performed. For the construction of Q-Q plot, the values of PSD are sorted and plotted versus theoretical quantiles which in this case follow the log-normal distribution. We plotted the Q-Q plots of the experimental data, the ones derived from the 1/f model, whose σ was extracted at 20 Hz, and the data extracted by the Lorentzian-based model, explained in the previous section, at two frequencies (20 and 120 Hz), as well as the Q-Q plots of the total noise power. The size of the dataset is 93 devices. The results are shown in Figure 6-7.

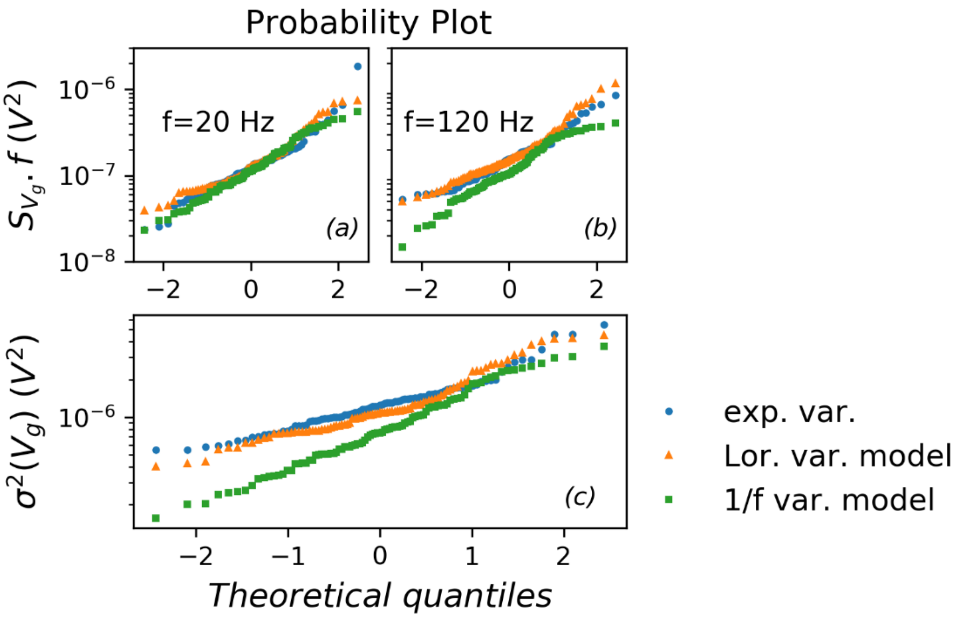

Figure 6-7: Q-Q plots of experimental PSDs, 1/f variability model and Lorentzian-based variability model at two frequencies (a): 20 Hz, (b): 120 Hz, (c): Q-Q plots total noise power for the different cases.

From Figure 6-7 one can observe that, although the 1/f variability extracted through Monte Carlo simulation, follows well the experimental data at 20 Hz, where we extracted the σ, it fails to do so at higher frequencies, i.e. 120 Hz, and its prediction is even worse regarding the total noise power, σ^2_{Vg}, estimated by eq. *(6-4)*. On the other hand, our model using eqs. *(6-5)* and *(6-7)*, can reproduce well the experimental variability in all cases, proving its usefulness and accuracy for circuit-level LFN simulations. It should be noted that for the best prediction of the experimental variability using the Lorentzian-based model, we needed to run the model 4-5 times in order to come up with this result, and this is mainly due to the small size of the dataset. This is also the reason why the experimental PSDs and noise power does not follow the linear trend for the log-normal distribution and deviates from this mostly in the extreme cases. Yet, the Lorentzian-based model captures perfectly this behavior, allowing for its implementation in Verilog-A for accurate circuit-level LFN simulations.

6.2. Implementation and Application of “VERILOR”

6.2.1. Brief Introduction to Verilog-A

Verilog-A is a hardware description language (HDL) for the analog behavior of components, circuits and systems. Once the behavior of a system or single device is described in Verilog-A code, SPICE class simulators, like “Spectre” in the case of Cadence, can interpret the models and solve the voltage/current equations to produce simulation results that precisely account for the model expressions [142]. It is a really powerful tool and supports the possibility of the description of different physical signals, through multiple disciplines. In our case, we used only the electrical discipline in which the signals are expected to be voltages and currents. So, we defined three electrical ports, (g,d,s), we utilised the lambert-W function for the expression of Q_i, for operating conditions similar as those of typical FDSOI devices, and we used the contributor symbol, “<+”, for the assignment of current in the drain port having as reference the source.

Concerning the noise analysis, Verilog-A provides three stimulus functions, *white_noise*, *flicker_noise*, and *noise_table*. In the white noise case, a constant PSD is assigned independent of frequency, whereas for the flicker noise, the PSD at 1Hz is needed, and then the noise values at different frequencies are extrapolated following the 1/f trend. There is also the possibility of constructing a PSD with $1/f^a$ trend, but this dependence will be on the whole bandwidth and thus, no Lorentzian spectra can be constructed using the *flicker_noise* function [142]. Regarding the *noise_table* option, it takes an array of pairs of values (frequency and PSD) as input, leaving the SPICE simulator to interpolate the in-between regions.

When only carrier number fluctuation needs to be added, in which case the S_{V_g} remains constant with V_g and equals $S_{V_{FB}}$, a voltage noise source can be assigned in series with the transistor gate through the statement below (Figure 6-8). Alternatively, the noise can be added as a current source in parallel with the transistor's output. In the latter case, for the calculation of S_{I_d} amplitude, the g_m has to be first extracted and this can be done easily using the ddx operator, that Verilog-A provides, if an analytical expression for I_d exists. Similarly, if the CMF part needs to be accounted for, the noise amplitudes will be extracted accordingly and the extraction of g_m is needed in both configurations. Finally, it is clear that in order for Lorentzian spectra to be constructed, the *noise_table* must be utilized, whose PSD values vary as a piecewise function of frequency.

V(g)<+ *flicker_noise*($S_{V_{FB}}, 1, "1/f"$)

I(d)<+ *flicker_noise*($S_{V_{FB}} * {g_m}^2, 1, "1/f"$)

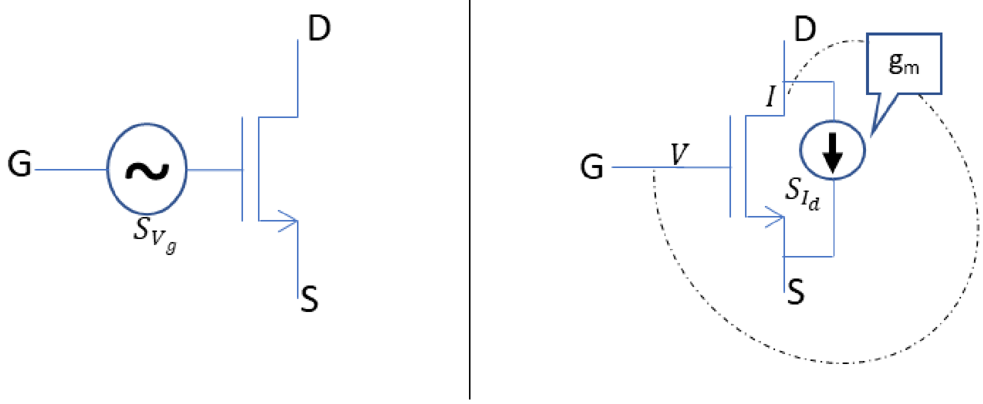

Figure 6-8: Schematic representation of the Verilog-A CNF noise model implementation. (left): voltage noise source, (right): current noise source.

6.2.2. Development of Lorentzian Spectra modeling in Verilog-A

Since there is no possibility for declaring a noise source in Verilog-A through a PSD function different than 1/f (*flicker_noise*) or thermal (*white_noise*) noise, we developed our module using the third option: the *noise_table* function. Therefore, after the automatic creation of a table with frequency values, with a resolution and bandwidth that can be user-controlled, the table of PSD values actually uses eq. *(6-5)* and sums up the Lorentzian contributors from all active traps. The calculation of N_T, ΔV_t, A and τ follows the procedure described in $6.1.2, like in [42], where a similar module was presented for RTN modeling in the time domain. In the end, the frequency (*F*) and PSD (S_{V_g}) tables are intertwined (odd/even indexes) together in a new table, *FS*, that is loaded in the *noise_table* function and inserted as a noise source at the FET gate. The flowchart of our module called "VERILOR" is shown in Figure 6-9. It takes as inputs the device dimensions and the trap density per volume and energy and then, the procedure described in $6.1.2 follows.

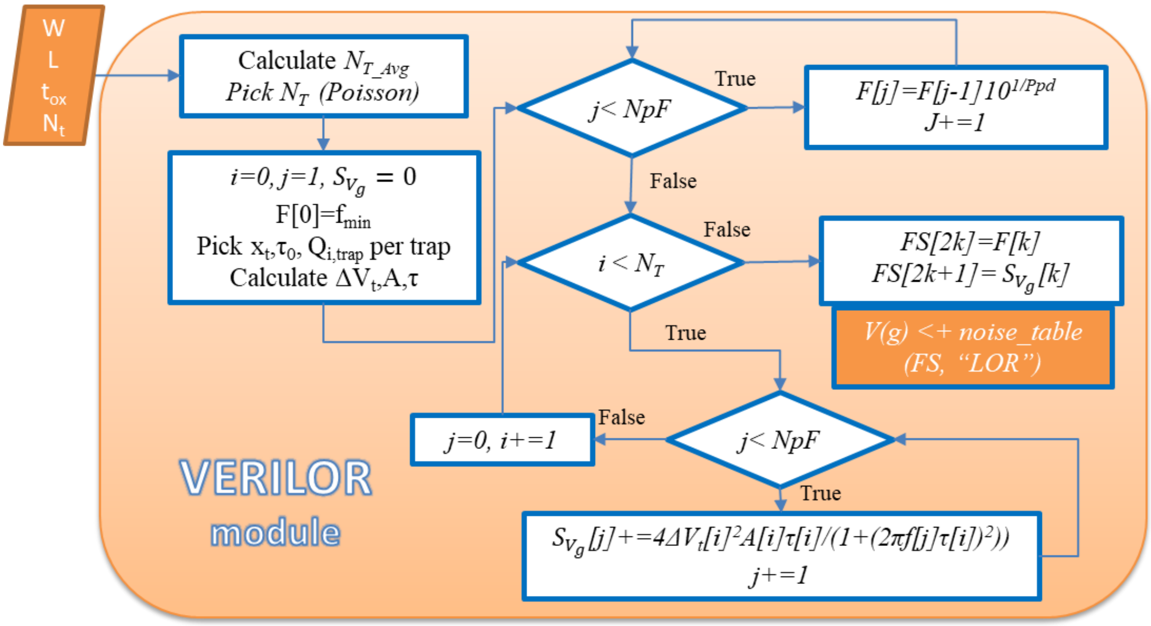

Figure 6-9: Flowchart of the VERILOR module. NpF: total number of points in spectrum, Ppd: points per frequency decade, f_{min}: starting frequency.

The only issue with Verilog-A is that the size of the arrays should be defined from the beginning and the dynamic change of their size is not possible. Consequently, regarding the frequency array, its size depends on the user's needs, concerning resolution and bandwidth.

Similarly, for the arrays related to traps characteristics, a maximum number of traps must be considered so as different dimensions to be covered. In our case, we considered a maximum number of traps equal to 1000. Once the implementation in Verilog-A finished, the symbol of this module can be created and finally it can be used for single device or circuit simulation. Figure 6-10 shows how the "VERILOR" module can reproduce the LFN variability effect in a circuit simulator using the physics-based approach of eqs. *(6-5)* and *(6-7)*. By doing so, extreme cases of circuits operation can be predicted.

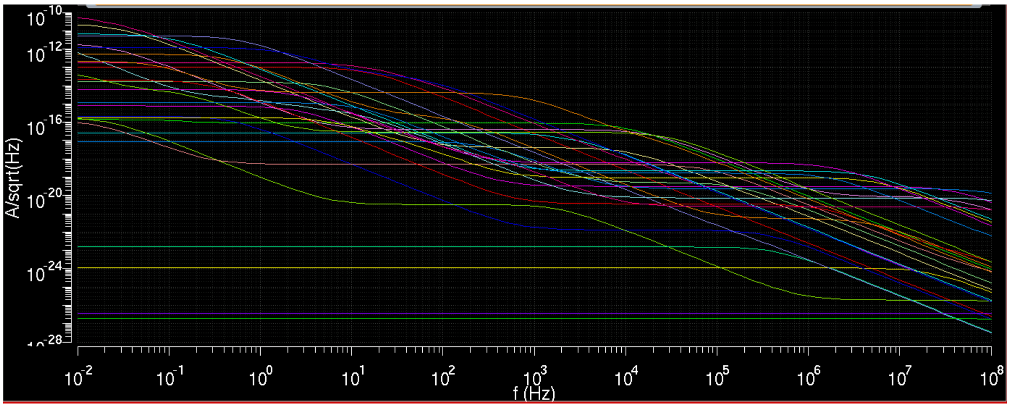

Figure 6-10: Screenshot of noise variability (30 dies) simulation results in Cadence Spectre, using "VERILOR' module. (W/L=80/30 nm).

6.2.3. Validation of "VERILOR" module

Before pursuing to further device and circuit simulations with the "VERILOR" module, we need first to confirm the validity of our model and its Verilog-A implementation. For this reason, we simulated the LFN induced by three individual traps, in a single device and for the same traps' characteristics, x_t, τ_0, Q_{it}, we extracted mathematically the resulted PSD using eq. *(6-5)*. As demonstrated in Figure 6-11, model and theory are in full agreement in terms of PSD shape confirming the successful implementation in Verilog-A. Moreover, we show in Figure 6-12 that the "VERILOR" module can be used in combination with the *flicker_noise* module for simulation of both GR and 1/f noise sources for more realistic device and circuit simulations.

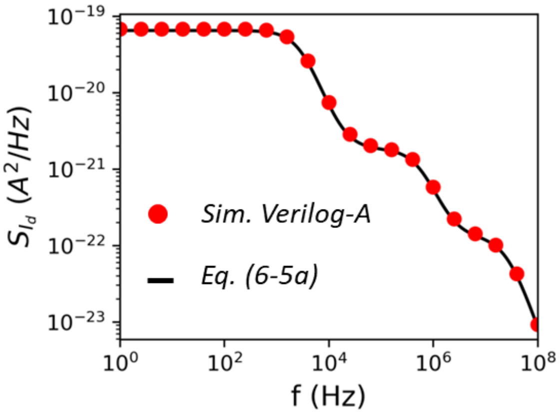

Figure 6-11: PSD comparison between the Loerentzian spectrum obtained by our Verilo-A model and the calculated one from eq. (6-5) using the same parameters for 3 traps.

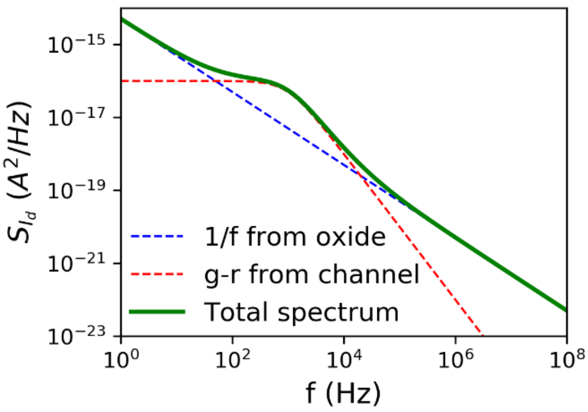

Figure 6-12: GR noise on top of 1/f in Verilog-A.

For further validation of the module, we compared the PSD induced from one single trap using “VERILOR” with the one resulted from the classic RTN time-domain model [42]. In addition, for the time domain simulation case, we used the transient noise module provided in spectre,[135], which considers the noise defined in the model and produces a time domain response. As shown in Figure 6-13b, both methods lead to the same spectra in the frequency domain, while in time domain both cases give the same signal variance and so, equal noise power (see Figure 6-13a). Of course, the frequency domain model cannot catch the abrupt changes of the signal in the time domain, but only its RMS power. Thus, when it comes to simulating RTN in circuits, if what matters is the RTN presence and amplitude and not so much its sudden transition events, “VERILOR” can be combined with the simulator’s Transient Noise module, to fairly reproduce the power of the RTN signal. Therefore, the level of dynamic variability can be accurately predicted by “VERILOR”, even with no RTN module in the time domain. However, if the transition moments are important for the simulation, as is the case for predicting RTN-induced SRAM errors, one needs to include a time domain Verilog-A RTN module. Moreover, the time domain module has a significantly lower simulation time (1.5s for the example of Figure 6-13 than the transient-generated signal (3s when NpF is only 30) using “VERILOR”.

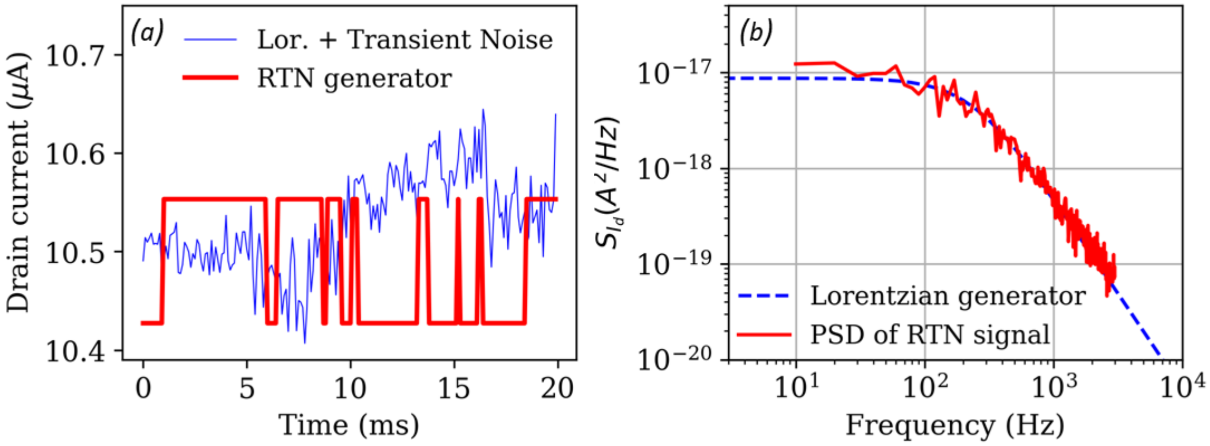

Figure 6-13: (a): Drain current transisent signal of LambertW-based MOSFET, (b): Power spectral density from the RTN model [42] *and "VERILOR".*

6.2.4. Simulation Examples of "VERILOR" Module

A. Area Scaling

In order to observe the behavior of the "VERILOR" module with device area and number of traps, and finally conclude whether this module can correctly capture the CNF model and the deviation from the 1/f PSDs in small area devices, we performed additional simulations for different gate areas and corresponding total number of traps. As it is demonstrated in Figure 6-14a, the "VERILOR" module can automatically reproduce Lorentzian-like spectra for highly scaled areas and 1/f-like for larger ones, confirming that indeed when uniform distribution of traps exists in large are devices, the overall simulated spectrum is 1/f. On top of that, it is able to generate a 1/f noise level that is in total agreement with the area-normalized carrier number fluctuation (CNF) model from weak to strong inversion as depicted in Figure 6-14b. In addition, since we proved that the "VERILOR" gives 1/f-like PSDs when the number of traps is high, it is interesting to compare the simulation time performance between a Flicker module and "VERILOR". For this reason, we ran the modules with different number of traps, and we extracted the simulation time for each case. As one can assume, and it is shown in Figure 6-15, the required CPU time using the Flicker module (around 20 ms) is independent of N_T, since it takes as an input only the $S_{V_{FB}}$ value and thus no additional calculations are needed. On the other hand, the simulation time of

“VERILOR” module is directly connected to the number of traps, because the model has to calculate each trap’s RTN amplitude and kinetics. As a result, with the exception of a single trap case (two-level RTN) where the “VERILOR” simulation time is quite close to the Flicker module, for a higher number of traps this duration increases exponentially with N_T. But, since we proved that the “VERILOR” PSD extraction reaches the 1/f behavior for high number of traps in large geometries, the user can decide from which number of traps and beyond the Flicker module will be prioritized. By doing so, similar results will be derived with less simulation time.

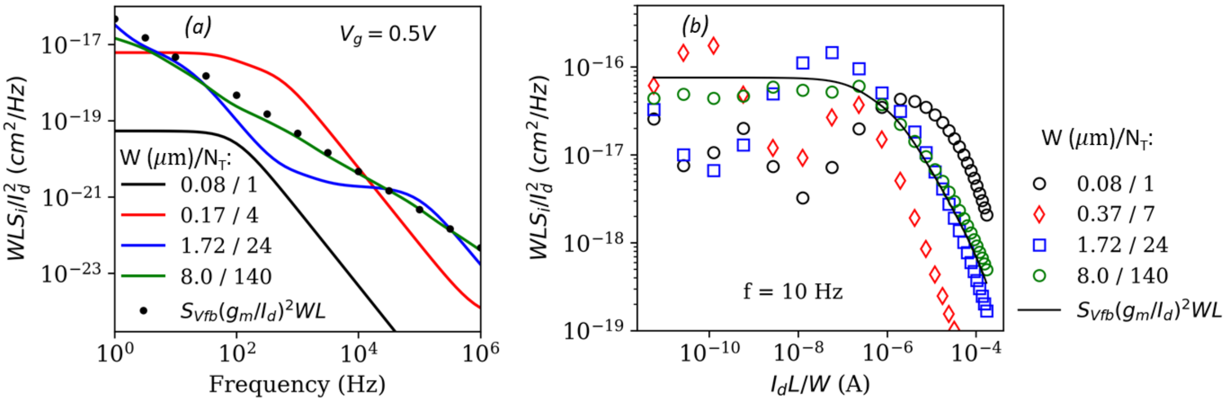

Figure 6-14: (a): Area-normalized PSD of drain current versus frequency at V_g=0.5 V and (b): versus normalized drain current for f=10 Hz, for 4 different W and corresponding N_T, along with CNF model. (L=0.3 µm).

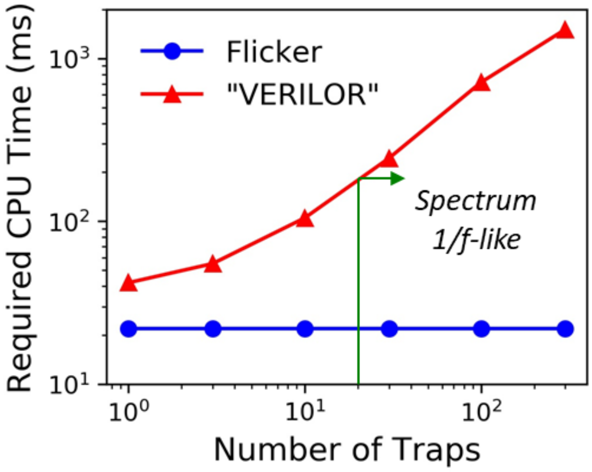

Figure 6-15: Simulation time versus number of traps for Flicker and “VERILOR” modules.

B. CMOS Inverter

As an easy and direct way to verify that the "VERILOR" module can be successfully used in a circuit with many transistors, we implemented the module for both p- and n-type devices so as to design a LambertW-based CMOS inverter. The inverter's voltage transfer characteristic is shown in Figure 6-16a. We chose each transistor to have different number of traps with different characteristics. Also, since we focused on a highly scaled-down geometry (W / L=80/30 nm), only a handful of active traps was considered. Then, we compared the total output noise with the sum of the individual device spectra and the result can be seen in Figure 6-16b. One can see that there is a total agreement between them confirming that the "VERILOR" module can be successfully used at a circuit level with different distribution of traps per device.

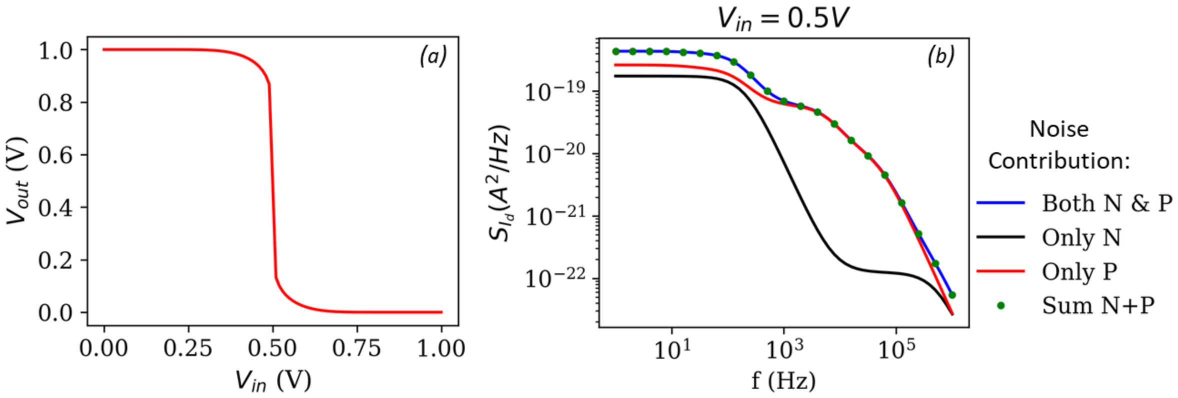

Figure 6-16: (a): I/O Inverter curve, (b): Output current PSD of LW-based CMOS inverter versus frequency for V_{in} =0.5V, along with separate noise contributions from each MOSFET, and their sum. (W/L=80/30 nm).

C. Ring Oscillator's phase noise

As briefly described in the beginning of this chapter, LFN is crucial for the right operation of a ring oscillator, as it is up-converted to phase noise for frequencies close to the oscillation frequency. An ideal RO has an output equal to eq. *(6-8)* [143], where A is the amplitude, ω_0 the frequency and ϕ a fixed phase reference.

$$V_{out}(t) = Acos[\omega_0 t + \varphi] \tag{6-8}$$

In reality, due to random fluctuations, both parameters, amplitude and phase reference, can alter with time, leading to the appearance of harmonics close to the oscillation frequency ω_0, in the spectrum of the oscillator. Although, the effect of amplitude variations can be eliminated [143], the phase noise cannot be reduced by the same way. It results to jitter noise in the time domain and in the appearance of sidebands in the frequency domain. The way that the phase noise changes with frequency depends on the nature of the fluctuations. In general, it has been reported that the device noise is up-converted to phase noise at the output voltage following a $1/(f_{off})^{n+2}$ frequency dependence for a noise source that has a PSD with $1/f^n$ trend [9], [143]. For example, thermal noise results in a -20dB/dec phase noise trend, whereas flicker noise in a -30dB/dec. As a result, one can assume that Lorentzian and 1/f spectra will cause different phase noise behavior, underlining once more the importance of Lorentzian noise modeling.

To prove that, and to extract a more accurate idea of the phase noise behavior in scaled down devices, we designed a 3-stage LambertW-based RO whose output is shown in Figure 6-17a. Afterwards, we pursued to extract the phase noise having each time either the Flicker or the "VERILOR" module activated. As one can see in Figure 6-17b, while 1/f up-converts to $1/f^3$, a Lorentzian spectrum up-converts to $1/f^2$ close to f_0 and then $1/f^4$ after the Lorentzian's cut-off frequency, f_c. As a result, for a scenario where 1/f coincides with the Lorentzian at 1 Hz, the phase noise becomes significantly higher around f_c, while the corner frequency, i.e. where LFN meets the thermal noise level, is shifted upwards by more than one decade. This is due to the plateau of the Lorentzian, which results to phase noise behavior similar to the one induced by thermal noise until its characteristic frequency.

In overall, this observation underlines the importance of Lorentzian noise modeling in RF/mixed signal circuits, where the operation bandwidth is a critical Figure of Merit. The opposite (lower phase noise and 1/f corner frequency) could also take place, if the Lorentzian has a lower plateau, due to the device-to-device variability as explained in $6.1.1.

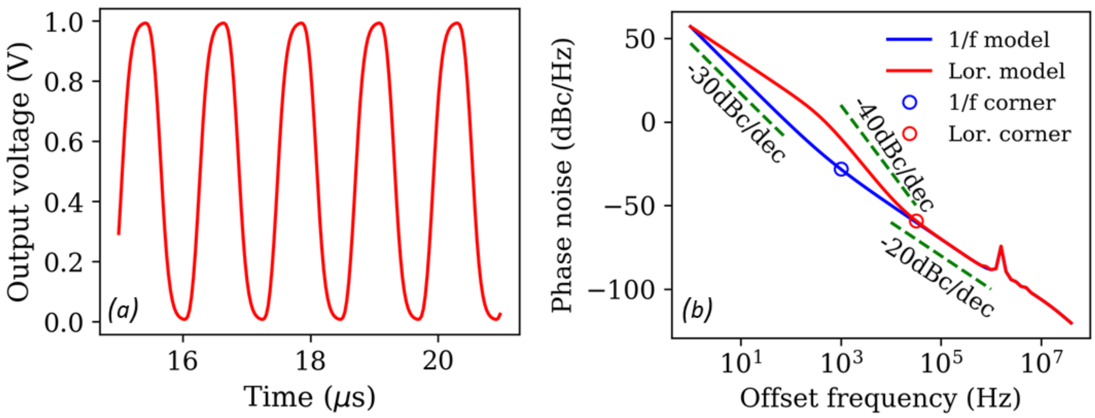

Figure 6-17: (a): RO's output voltage versus time, (b): Phase noise of LambertW-based 3-stage CMOS ring oscillator versus offset frequency for 1/f and Lorentzian noise.

6.3. Summary

To sum up, in this Chapter we have presented a new method of noise model implementation for circuit simulations, which enables the generation of Lorentzian-type spectra, based on every trap's property. The importance of Lorentzian noise modeling is explored in contrast to classic 1/f or Random Telegraph Noise (RTN) modeling, in terms of PSD, total noise power, and device-to-device noise variability reproduction, through analysis of experimental data. The Verilog-A modeling method that accounts for both Lorentzian and 1/f types of noise is demonstrated and validated, using a Lambert-W function charge-based drain current model. Finally, fundamental digital and analog circuits such as the Ring Oscillator were used to showcase the usefulness and applicability of the "VERILOR" model in circuit noise simulations. We demonstrate that the Lorentzian noise can either degrade or improve the phase noise close to the oscillation frequency, as well as the 1/f corner frequency.

CHAPTER 7

Conclusions and Perspectives

The goal of this dissertation, arising from the severe impact of low frequency noise (LFN) on emerging technologies, was to take a step forward the investigation of LFN in advanced MOS devices. The dominant mechanisms of LFN in advanced FET technologies have been identified and new methodologies have been developed that allow for a deeper understanding of the physics of defects and the reliable extraction of LFN parameters. The ultimate purpose of these studies is to contribute on the development of models valuable from device to circuit level.

To begin with, 14 nm Bulk technology FinFETs with sub-10 nm FIN width have been characterized in terms of LFN. The impact of FIN width and number of FINs on the level of LFN has been investigated. The results showed that the trapping/detrapping of free carriers with defects in the oxide originates the 1/f noise, and thus allowing the extraction of the oxide trap density per eV and the CMF coefficient Ω. In addition, no significant impact of FIN width and number of FINs on the extracted parameters has been observed. Moreover, in the frame of "More than Moore" technology roadmaps, new technologies and architectures have been studied in terms of LFN for their potential use in 3DSI applications, in which low temperature (LT) processes are required. More specifically, LT junctionless Tri-Gate devices have been characterized and compared to conventional high temperature Junctionless and Inversion mode structures. Apart from the increased series resistance impact on LFN level, due to the LT source and drain regions, no additional phenomena that could degrade the performance of LT devices have been observed. In fact, the extracted trap density was at the same level with their HT counterparts, showing good quality of the oxide. As another vehicle for 3DSI applications, LT SOI MOSFETs with different gate stack process have been characterized. In this case, apart from the 1/f component, LFN spectra showed a Lorentzian part, independent of the gate stack process. This led us to the conclusion that the LFN level was mostly affected by the process temperature rather than the gate stack combination. The 1/f part of the spectra fitted well the CNF/CMF model allowing the extraction of N_t and Ω. The extracted trap density was quite elevated for all the LT splits, whereas no high values of the CMF coefficient were reported.

Concerning the Lorentzian spectrum, LFN spectroscopy was followed for the identification and localization of traps. The almost independent Lorentzian spectrum on the polarization conditions enhanced the assumption that the defective zone was located inside a depleted region in the Si channel. But the application of the constant current method came to exclude this scenario. This is because, although the charge centroid moved vertically from the top to bottom interface, no significant impact on the Lorentzian parameters and especially on the time constant was observed. Consequently, we concluded that the time constant of the Lorentzian is affected more by the polarization conditions than the concentration of free carriers. Thus, we believe that the defective zone is located in the top oxide and interacts with the carriers of the metal. In this case, due to the excess number of electrons in the metal, the trap's capture time can be considered constant but the emission time is affected by the applied potential. This scenario is expected to be validated in the near future with specific process splits.

Furthermore, since this thesis focuses on advanced technologies with aggressively scaled down dimensions, we studied how the SCEs can affect either the accuracy of the extracted LFN parameters or the detectability of traps. We proved through experiments and simulations that indeed the series resistance can hinder the reliable extraction of LFN parameters especially of the CMF coefficient which is extracted in the strong inversion region. For this reason, we developed a new method that utilizes the Y-function, and thus, the revised CNF/CMF model suppresses successfully the impact of series resistance. In addition, we showed firstly through experiments and then through TCAD simulations, that the pinch-off effect in the saturation region of operation, can actually decouple the effect of multiple traps and contribute to single trap's isolation, through the effect that V_d has on the trap's kinetics and amplitude. Consequently, we proposed the "pinch-to-detect" method which consists of LFN measurements in linear, saturation from drain and saturation from source side, allowing for the maximization of detected traps.

Finally, concerning variability studies of LFN, whose accuracy has a critical role on the safe operation of circuits, we showed that the typical 1/f approach for the reproduction of the LFN variability is not sufficient anymore, since more and more Lorentzian-shape spectra are present in the downscaled devices. For this reason, we proposed a Lorentzian noise model, called “VERILOR” and we implemented it in Verilog-A. It is able to generate both 1/f and Lorentzian spectra depending on the number of traps. Once its validity was confirmed, we applied “VERILOR” for the accurate prediction of ring oscillator’s phase noise.

Regarding the future work directions, the LFN characterization of LT SOI MOSFETs without the TiN metal layer is of critical importance, as it will immediately validate our assumption concerning the localization of the defective zones. As for the experimental methodologies we developed, the R_{SD}-immune method needs to be implemented in Verilog-A, so as the accurate level of LFN in the output of a circuit can be precisely simulated, free of series resistance issues. Moreover, since we proved that in highly scaled-down devices, the non-uniform distribution of carriers inside the channel due to CLM and DIBL in saturation, affects the application of the CNF model, the development of a revised CNF model is suggested, that takes into account the lateral position of the trap, and how it is affected by the horizontal voltage bias V_{ds}. Within this framework, more detailed LFN measurements with small step of V_{ds} sweep from linear to saturation will be beneficial, as it could increase even more the number of detectable traps. Finally, it is recommended the “VERILOR” module to be applied to a series of digital and analog circuits for accurate noise simulations, with the statistical (variability) aspect put forward.

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RÉSUMÉ

Malgré les progrès dans la recherche et développement des composants à semi-conducteurs, avec l'incorporation de nouveaux matériaux et architectures et la réduction des dimensions géométriques, qui conduisent à des performances et à une vitesse supérieure, le bruit basse fréquence, LFN, est devenu une préoccupation majeure pour les transistors micro et nanométriques, car son impact au niveau du dispositif et du circuit est plus important que jamais. Tout d'abord, il faut noter que, dans cette thèse, quand on parle de LFN, on entend le type de bruit interne dû au piégeage/dépiégeage ou/et aux collisions de porteurs libres. Pour les spectres de type 1/f, la densité spectrale de puissance de tension de bande-plate, S_{Vfb}, est inversement proportionnelle à la surface, et donc en passant des dispositifs micro aux dispositifs nanométriques, le niveau LFN est augmenté. De plus, avec la miniaturisation de la surface du transistor, un type de bruit différent appelé Random Telegraph Noise, RTN, apparaît et devient la contribution principale au lieu du 1/f, à mesure que le comportement de piège individuel devient visible. En plus de cela, l'introduction de nouveaux matériaux et architectures dans la technologie CMOS entraîne l'apparition d'un comportement particulier comme celui du bruit de génération-recombinaison, GR, qui montre une DSP Lorentzienne au lieu de 1/f. En conséquence, les composants électroniques de nouvelle génération seront gouvernés par des instabilités liées à leur bruit intrinsèque. Il est donc essentiel d’adapter les méthodes de caractérisation et de simulation du LFN/RTN pour permettre l'amélioration de la technologie. C'est pourquoi une étude théorique et expérimentale approfondie de toutes les sources de bruit dans les nouveaux composants devient indispensable dans ce domaine de recherche en microélectronique.

Dans cette thèse, les dispositifs qui répondent aux spécifications ITRS sous la demande des directives technologiques "More Moore" et "More than Moore", ont été caractérisés en termes de LFN. Tout d'abord, nous utilisons le LFN comme outil pour évaluer différentes technologies, en termes de qualité d'interface d'oxyde de grille, ainsi que de l’intensité des effets de diffusion. Nous profitons de l'extraction des paramètres de bruit (N_t et Ω) en utilisant

la partie quasi 1/f du LFN pour poursuivre une étude expérimentale comparative entre différentes technologies. De cette façon, nous pouvons avoir une première idée concernant les étapes de fabrication qui sont probablement responsables de la dégradation des performances des différents dispositifs en termes de LFN, ce qui pourrait à son tour affecter de manière significative le fonctionnement des circuits. A travers cette étude, les phénomènes physiques qui induisent le bruit intrinsèque du dispositif ont été identifiés, une information utile non seulement pour le dispositif lui-même, mais aussi pour la modélisation précise du bruit et donc pour faciliter la conception des circuits associés. Des exemples de valeurs N_t et Ω extraites pour les technologies FinFET et LT SOI MOSFET sont présentés dans les Figures 1 et 2 respectivement.

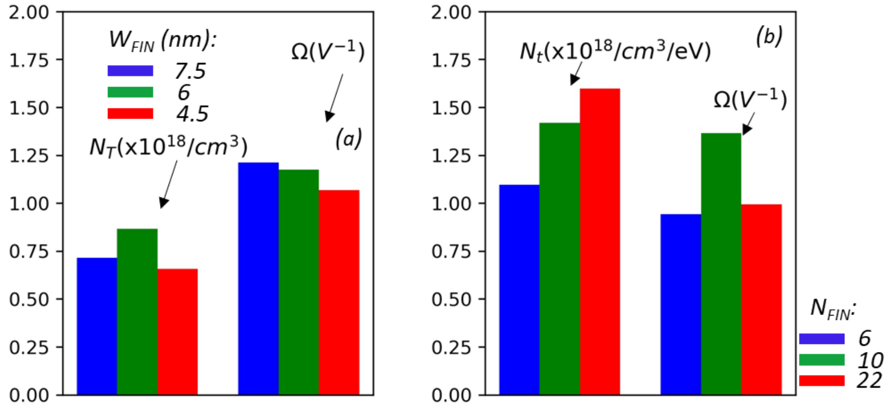

Figure 1 : Densité de piège volumétrique extraite, N_t, et coefficient CMF, Ω, pour la technologie FinFET. (a) : versus différents W_{FIN} et (b) : versus différents N_{FIN}.

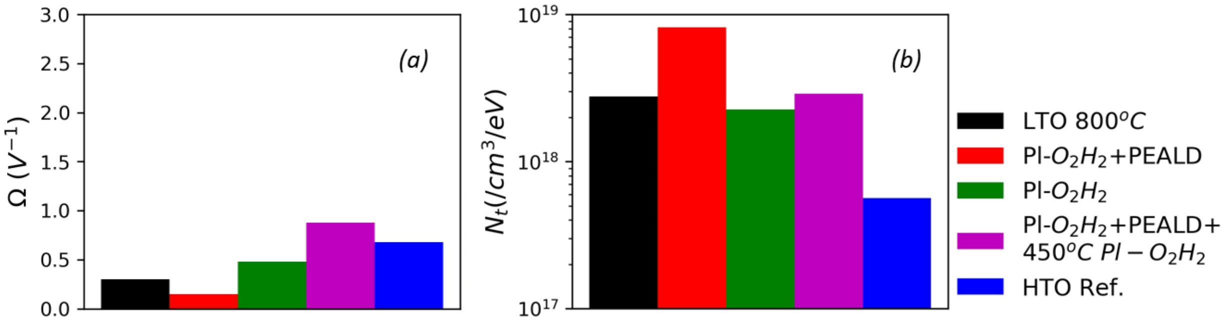

Figure 2: Facteur CMF, Ω, et densité de piège volumétrique, Nt, extraits de l'ajustement CNF/CMF pour différentes divisions de tranches LT SOI.

De plus, les mesures LFN ont servi d'outil de diagnostic pour l'identification des zones défectueuses donnant des informations sur la qualité des transistors fabriqués. Cette dernière est essentielle pour l'optimisation des étapes de fabrication. C'est pourquoi le 4ème chapitre est consacré à la caractérisation des spectres de type lorentzien. L'observation des spectres lorentziens pour toutes les variantes de MOSFETs à basse température, présentée au chapitre 3, nous a conduit à la conclusion qu'une zone défectueuse existe à l'intérieur des dispositifs qui est probablement neutralisée avec le recuit à haute température. C'est la raison pour laquelle aucun spectre lorentzien n'a été observé dans la plaquette de référence. Des mesures LFN détaillées sous différentes températures et conditions de polarisations sont présentées comme un moyen de détecter et identifier ces zones défectueuses. Nous avons examiné différents scénarios pour l'emplacement des pièges et nous avons appliqué diverses conditions de polarisation afin de déduire comment les paramètres lorentziens, A et τ, sont affectés par ceux-ci. La mise à l'échelle de A avec la surface excluait la possibilité que des pièges se trouvent dans les régions de source et de drain. Ainsi, les scénarios restants étaient que les pièges se trouvaient à l'intérieur : a) de l'oxyde supérieur ou inférieur, b) du film de silicium ou c) de l'oxyde supérieur interagissant avec les porteurs dans la couche de TiN. L'identification des spectres lorentziens dans les modes de fonctionnement de la grille avant et arrière ainsi que la faible dépendance de τ sur V_g ou V_b nous ont conduit à l'hypothèse que les pièges pourraient se trouver dans une région appauvrie à l'intérieur du canal. Mais ce scénario a été exclu une fois que nous avons observé la faible dépendance de τ lors du changement de position du canal à l'intérieur du film de Si, par la méthode du courant constant. Pour cette raison, nous pensons que le scénario selon lequel les pièges sont dans l'oxyde supérieur mais interagissent avec les porteurs dans le métal TiN est plus probable. Ce scénario sera validé dans un futur proche, une fois que des mesures LFN sur des plaquettes sans TiN seront réalisées.

Dans le 5ème chapitre, nous montrons que la résistance série, R_{SD}, du transistor peut provoquer une extraction non fiable des paramètres de bruit, en particulier le coefficient de diffusion, Ω, qui est extrait dans la région de forte inversion. Un exemple représentatif est illustré à la Figure 3. Bien que ce problème soit amélioré dans les dispositifs à canal court, où le RSD des régions de source et de drain est comparable à la résistance du canal, il peut également se produire dans d'autres cas lorsque, dans la configuration de mesure, le transistor est connecté en série avec un composant à haute résistance. Pour cette raison, nous proposons une méthodologie insensible à RSD pour l'extraction précise des paramètres de bruit, en utilisant la fonction Y, qui est couramment utilisée pour l'extraction des paramètres statiques, grâce à son immunité à la dégradation de la mobilité de 1er ordre et à la résistance série.

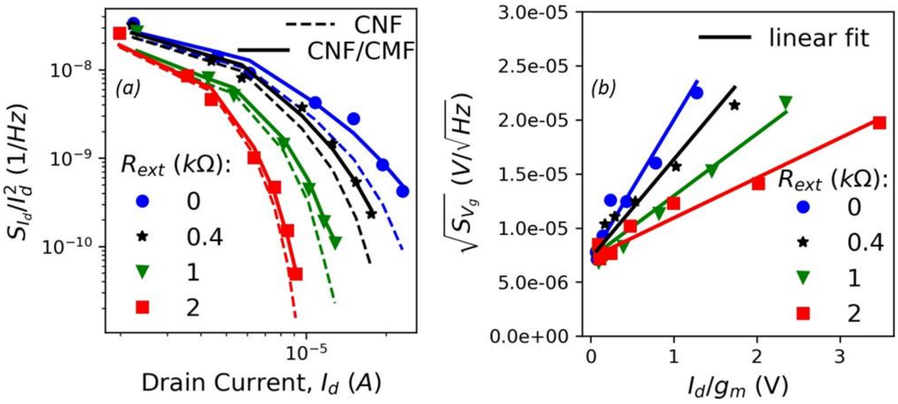

Figure 3: (a) : Bruit de courant de drain normalisé par rapport au courant de drain, mesuré à la tension de drain V_d = 30 mV, ainsi que les modèles d'ajustement CNF et CNF/CMF pour les différentes valeurs de résistance externe, (b) Racine carrée du bruit référé à l'entrée par rapport au rapport du courant de drain et la transconductance, mesurée à la tension de drain V_d = 30 mV, pour différentes valeurs de résistance externe.

De plus, nous montrons à travers des mesures systématiques et des simulations TCAD, que les mesures RTN dans des conditions de V_d et de V_s élevés peuvent en fait aider à détecter plus de pièges. Nous démontrons que l'effet de pincement dans la région de saturation de fonctionnement peut être exploité pour la modulation des amplitudes et de la cinétique RTN, et donc désactiver ou activer l'apparition de signaux RTN. Par conséquent, nous proposons une nouvelle méthodologie de mesure, appelée "Pinch-to-Detect" (pincer pour détecter), qui combine trois configurations de canaux différentes (uniforme, pincement près du drain, pincement près de la source), et permet au nombre total de pièges RTN détectables d’être maximisé.

Enfin, comme l'apparition de spectres Lorentziens est de plus en plus fréquente dans les technologies FET avancées, les modèles de domaine fréquentiel LFN doivent être révisés. En effet, les modèles de domaine fréquentiel existants sont limités au comportement typique en 1/f qui, comme nous le prouvons dans cette thèse, peut compromettre le fonctionnement des circuits. Par conséquent, dans le dernier chapitre, nous présentons une méthode que nous avons développée pour l'implémentation des spectres de bruit lorentzien en Verilog-A (détails dans $6.2.1), de manière à générer automatiquement des spectres de bruit lorentzien ou 1/f en fonction de la densité de pièges et de la zone d'oxyde, pour toutes les conditions de polarisation. Nous avons nommé cette approche de modélisation « VERILOR », pour combiner les termes « Lorentzien » et « Verilog-A » et faciliter la référence lorsqu'elle est utilisée par d'autres scientifiques ou concepteurs de circuits. Après avoir souligné les avantages de la modélisation lorentzienne en ce qui concerne la modélisation 1/f et temporelle du RTN, à l'aide d'un modèle de courant de drain basé sur la fonction Lambert-W [114], nous démontrons l'applicabilité de notre module dans les simulateurs de circuit, et comment il peut permettre des études précises de la variabilité du bruit au niveau du circuit. Enfin, quelques exemples d'application de bruit de circuit sont présentés, révélant par exemple comment le bruit de phase d'un oscillateur en anneau (RO) peut être affecté en présence d'une DSP de type lorentzien. Les simulations de bruit au niveau du dispositif et du circuit ont été réalisées avec le simulateur Cadence Spectre [135].

La figure 4 montre comment le bruit de phase d'un RO est affecté par des sources de bruit 1/f ou Lorentzienne.

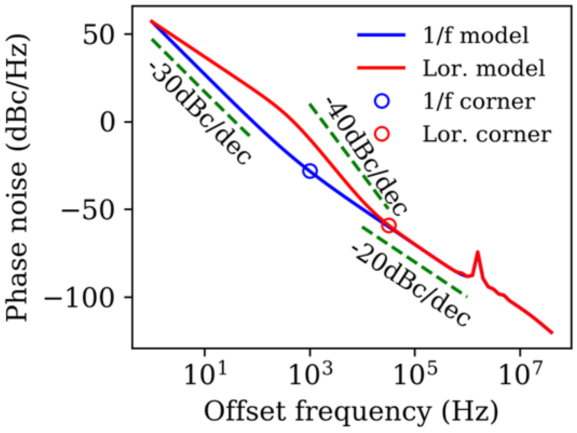

Figure 4: Bruit de phase de l'oscillateur en anneau CMOS à 3 étages basé sur LambertW en fonction de la fréquence de décalage pour le bruit 1 / f et Lorentzienne.

Comme on peut le voir, tandis que le 1/f se convertit en $1/f^3$, un spectre lorentzien se convertit en $1/f^2$ près de f_0 puis $1/f^4$ après la fréquence de coupure de la Lorentzienne, f_c. En conséquence, pour un scénario dans lequel le 1/f coïncide avec la Lorentzienne à 1 Hz, le bruit de phase devient significativement plus élevé autour de f_c, tandis que la fréquence de coin, c'est-à-dire où le LFN rencontre le niveau de bruit thermique, est décalée vers le haut de plus d'une décade. Ceci est dû au plateau de la Lorentzienne, qui se traduit par un comportement du bruit de phase similaire à celui induit par le bruit thermique jusqu'à sa fréquence caractéristique. Dans l'ensemble, cette observation souligne l'importance de la modélisation du bruit lorentzien dans les circuits RF/signaux mixtes, où la bande passante de fonctionnement est une figure de mérite critique. L'inverse (bruit de phase inférieur et fréquence de coin 1/f plus faible) pourrait également se produire, si la Lorentzienne avait un plateau de niveau plus faible, en raison de la variabilité d'un dispositif à l'autre, comme expliqué dans $6.1.1.