Integrated two-port vector network analyzer design for non-invasive characterization

Ghita Yaakoubi Khbiza

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITE GRENOBLE ALPES

Spécialité : **Optique et radiofréquences**

Arrêté ministériel : 25 mai 2016
Présentée par

GHITA YAAKOUBI KHBIZA

Thèse dirigée par Dr. **HDR José Luis GONZALEZ JIMENEZ** et encadrée par Dr. **Baudouin MARTINEAU**

Préparée au sein du laboratoire **LAIR** du **CEA-Leti** dans **l'École Doctorale EEATS**
Intitulée

Conception d'un analyseur réseau à deux ports pour des mesures non invasives
Integrated two-port vector network analyzer design for non-invasive characterization

Thèse soutenue publiquement le **03 juillet 2023**,
Devant le jury composé de :

Dr. HDR Sylvain Bourdel Professeur titulaire - Institut de technologie de Grenoble (Grenoble INP) - Laboratoire TIMA	Président du jury
Dr. HDR NATHALIE DELTIMPLE Chercheuse à IMS Bordeaux et Professeur à INP/ENSEIRB-MATMECA	Rapporteur
Dr. HDR KATIA GRENIER Chercheuse / directrice de recherche en Micro et nano systèmes Hyper-fréquences Fluidiques au CNRS	Rapporteur
Dr. HDR José Luis GONZALEZ JIMENEZ Directeur de recherche à l'unité Wireless & Telecom du CEA-Leti	Membre du jury
M. Frederic HAMEAU Chef de projet en département santé du CEA-LETI	Invité
PHD. Estelle LAUGA-LARROZE Enseignante Chercheuse à UGA / Laboratoire RFIC-Lab	Invitée
Dr. Baudouin Martineau Chef du Laboratoire d'Architectures Intégrées Radiofréquences au CEA-Leti	Invité
Dr. HDR. Dominique MORCHE Ingénieur e recherche au CEA LETI	Invité

Titre : Conception d'un analyseur réseau à deux ports pour des mesures non invasives

Résumé: Cette thèse s'inscrit dans le cadre d'un projet de recherche et développement à long terme visant à intégrer des solutions d'analyse non-invasives. Les publications dans divers domaines, en particulier dans les domaines de la santé et de l'agriculture, ont démontré que la signature diélectrique du milieu mesuré peut être liée à ses caractéristiques physiques. Cependant, l'utilisation d'un analyseur de réseau vectoriel (VNA) pour extraire cette information limite souvent la portée d'application en raison de la taille, du poids et du coût de ces instruments. Dans cette thèse, nous proposons une étude de faisabilité et la conception d'un VNA à circuit intégré. En développant un outil plus compact, économique et polyvalent, nous espérons ainsi surmonter ces limitations et contribuer à l'avancement de la surveillance non invasive.

Mots clés: analyseur de réseau vectoriel (VNA), mesures non invasives, mesures de réflexion, mesure de transmission

Title: Integrated two-port vector network analyzer design for non-invasive characterization

Abstract: This thesis is a part of a development project that is focused on integrating non-invasive analysis solutions. The project aims to leverage the connection between a material's environment and its dielectric signature, which has been the subject of extensive study in a range of fields, including agriculture and health, among others. The common theme among these studies is the requirement for a vector network analyzer (VNA) to extract the dielectric signature from measurements made in reflection or transmission of a radio wave at various frequencies. However, the use of a VNA is frequently limited by the size, weight, and cost of these instruments, which can limit their application. To overcome these challenges and advance research in this area, this thesis proposes a feasibility study and design for an integrated circuit VNA. The aim of this project is to develop a wideband, more compact, cost-effective, and versatile tool that can be used in a variety of promising applications. Through this effort, we hope to contribute to advancements in the fields of health and agriculture by providing a powerful and flexible analysis tool.

Keywords: vector network analyzer (VNA), non-invasive measurements, reflection measurements, transmission measurements

ACKNOWLEDGMENT

I would like to express my deepest gratitude to my thesis advisors, Dr. Baudouin Martineau and Dr .HDR. GONZALEZ JIMENEZ José Luis for their unwavering support, guidance, and mentorship throughout my research. Their expertise and dedication have been invaluable to me and have made this project possible.

I would also like to thank my colleges in the RF architecture & IC Design laboratory (LAIR) in CEA Leti for their support and encouragement. Their willingness to share their knowledge and expertise has been instrumental in my growth as a scholar. I am grateful for the stimulating environment that they have created and for the countless conversations that have challenged and inspired me.

To my family and friends, I am deeply grateful for their love, encouragement, and unwavering support during this journey. Their belief in me has been a constant source of inspiration, and I could not have accomplished this without them.

Lastly, I would like to acknowledge the participants in my study, whose willingness to share their experiences and perspectives made this research possible. Their contributions have been invaluable and have deepened my understanding of the topic.

I am truly humbled and grateful for the contributions of all those who have supported me on this journey.

Thank you.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

GENERAL INTRODUCTION

In the radio frequency (RF) engineering field, Vector Network Analyzers (VNAs) have long been used to analyze passive, active components, and complex modules [1]. However, VNAs are increasingly being recognized as a crucial component in non-invasive monitoring sensors, going beyond their conventional use as a versatile tool for instrumentation and measurement applications.

This introductory section seeks to bring attention to the various application fields of VNAs and their potential in the integration of non-invasive monitoring sensors. By highlighting the diverse opportunities that arise from the incorporation of VNAs as a constituent element of a complete non-invasive monitoring sensor, this section aims to promote the need to integrate a VNA. Thus, a wide range of possibilities can be realized, ranging from health and agriculture to industrial and environmental monitoring applications.

At the outset of this thesis, it is important to clarify that the aim is not to establish a direct correlation between VNA measurements and intrinsic metrics associated with non-invasive monitoring applications. Rather, the focus is on designing a compact VNA that can unlock the first step, which is measuring scattering parameters; the correlation will be investigated in future works.

TOWARD A WIDEBAND VNA MINIATURIZATION

The use of a VNA tends to be restricted to stationary scenarios due to its size, weight, and high cost. Therefore, the need for a compact, low-cost, portable device with adequate accuracy and functionality is considered a promising noninvasive measurement technique in a vast range of application fields.

The following study involves mapping keyword co-occurrence networks (KCNs[1]) using *VOSviewer*[2]. It first provides a large-scale perspective on new trends in VNA use and then seeks the answer to the following research question:

[1] In a KCN, a keyword has been identified as a node, and each co-occurrence of a pair of words is presented as a link. The higher the frequency of a keyword, the larger the size.
[2] A free software for bibliometric mapping developed by Eck and Waltman [2]

How a VNA integration would unlock a complete noninvasive sensor implementation?

Figure 1 depicts the extracted KCN from [3]– [46]. Among the 44 articles across the map, three catchwords are strongly involved: *VNA (yellow cluster), antenna (light blue), and sensor (dark blue) in mainly biomedical (green cluster) and agricultural fields (red cluster).*

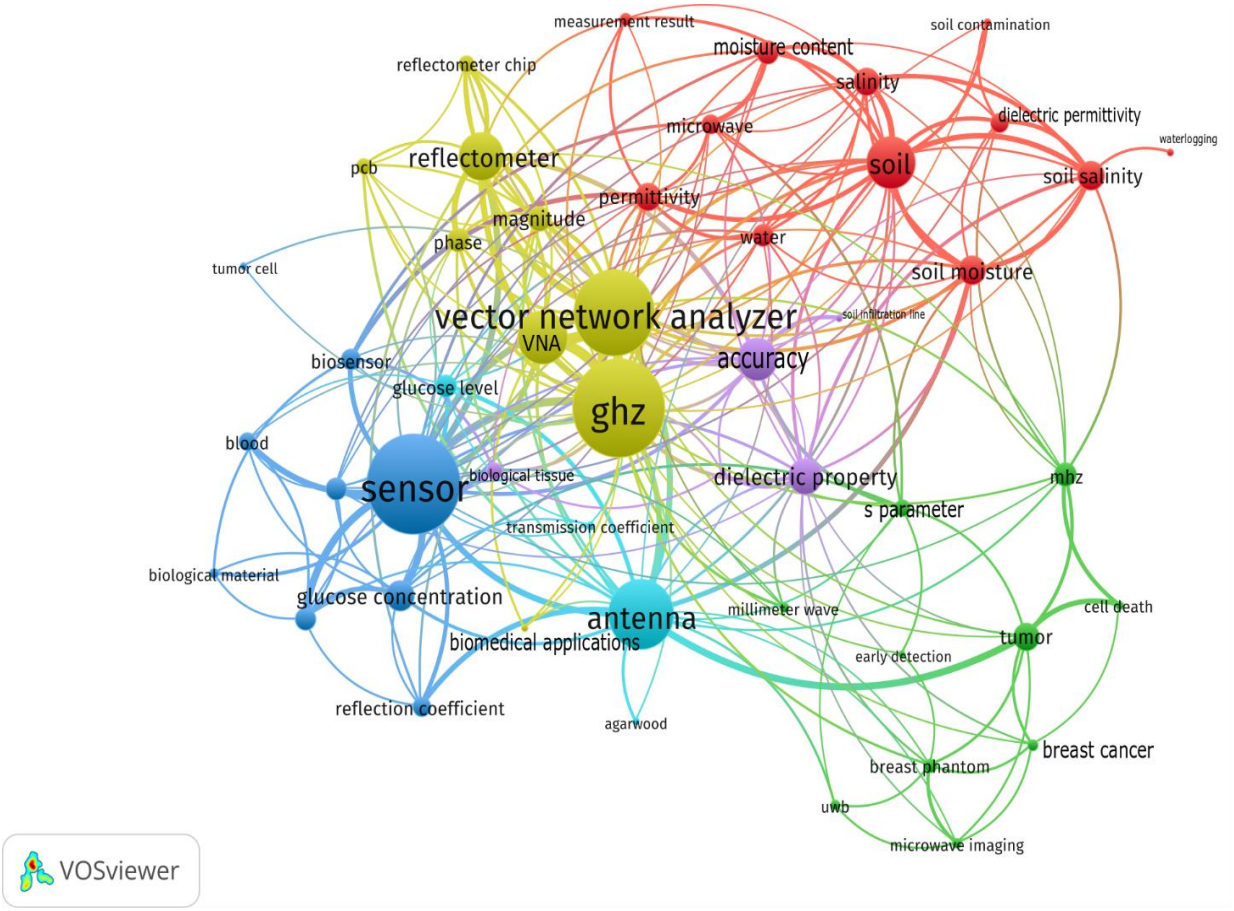


Figure 1: Keyword co-occurrences study. Of the 2126 terms, 70 meet the threshold of 7 times occurrences, and 60% most relevant terms are selected

Based on co-occurrence data, several relevant applications have been identified, starting with biomedical applications. Notably, in [4], [7], microwave imaging (MI) is used as an alternative technology to detect carcinogenic cells. It uses frequencies ranging from 300 MHz to 30 GHz due to the ability of millimeter waves to penetrate through biological tissues

and detect variations in dielectric properties. Additionally, MI is used to overcome the inconvenience associated with X-rays and MRI[3], as discussed in [3].

To understand microwave-imaging systems, consider the system shown in Figure 2. The antenna emits microwave signals that penetrate the medium and reflects back based on the dielectric properties of the medium. The reflected signals are then collected by the antennas and sent to the VNA for measurement. The VNA measures the reflected signals and provides information about the dielectric properties of the medium. The reconstructed phantom image generated by the system provides the distribution of dielectric properties within the imaged medium. The image analysis can be used to non-invasively identify areas of abnormal tissue growth or other anomalies that may point to potential cancerous growth.

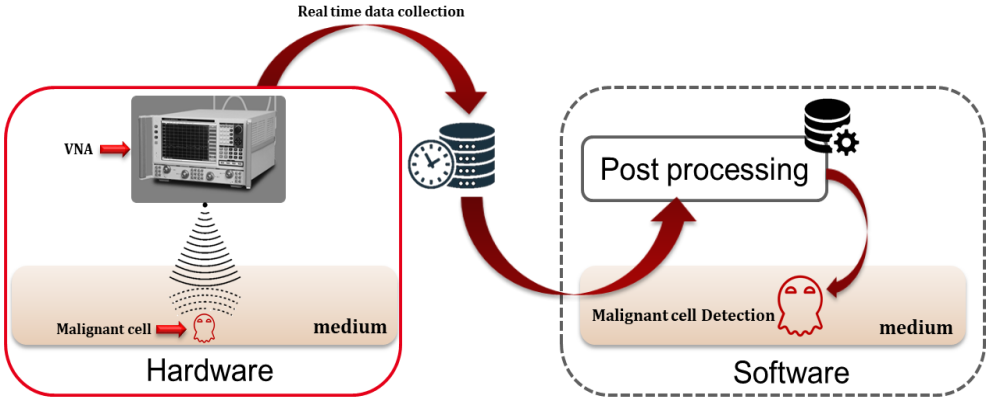
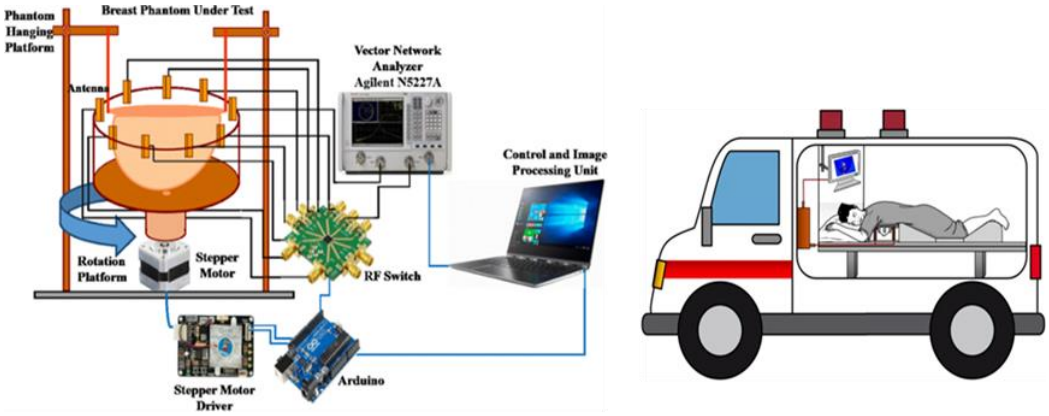


Figure 2: A schematic diagram showing the components of the microwave imaging system

Microwave imaging systems are particularly useful for premature breast cancer detection, as they can provide an early diagnosis of cancer as a complementary tool to mammography. As a proof of concept, in [4], the authors reported a cost-effective and portable MI for the detection of malignant cells inside the human breast using frequencies in the range of 2.80 GHz to 7.00 GHz. As generally illustrated in Figure 2, Figure 3 (a) presents the proposed microwave imaging system consisting of multiple antennas surrounding the patient's breast and operating as both a transmitter and receiver. The system provides an image of the internal dielectric characteristics of the whole breast phantom. However, as noted in Figure 3 (b), the monitoring system is heavy and has to remain stationary, which may limit its practicality in clinical settings.

3 MRI: magnetic resonance imaging

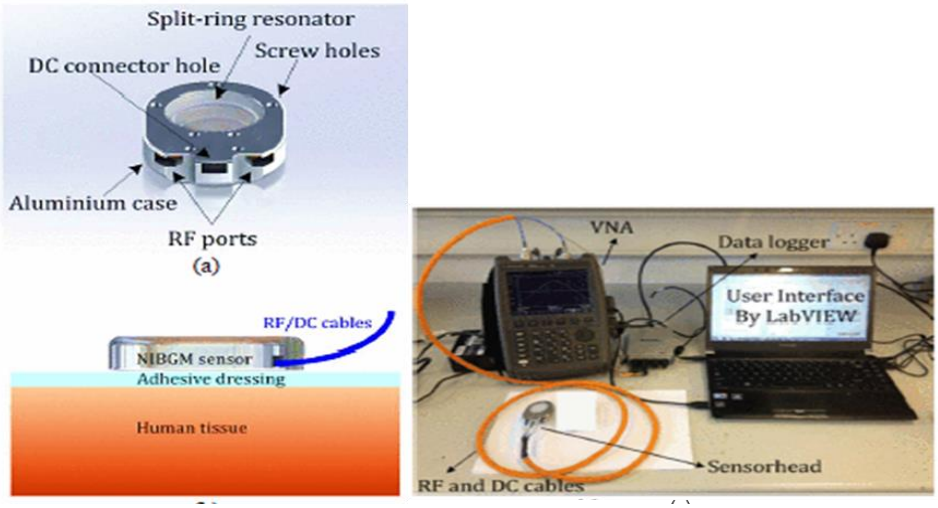


(a) (b)

Figure 3: (a) Conceptual view of microwave tomography technique, (b) The graphic view of the proposed breast imaging system [4].

A second application in the health field retrieved from Figure 1 is non-invasive blood glucose monitoring. In [5], the dielectric properties of glucose levels were extracted from adults aged 18-40 years to establish a dielectric model according to glucose concentration variation for frequencies ranging from 500 MHz to 20 GHz. This study lays the foundation for choosing the pertinent[4] frequency band to design electromagnetic glucose sensors. In [6], a noninvasive wearable blood glucose monitoring system has been developed and tested within a clinical trial involving 24 human subjects, Figure 4 (a). As presented in Figure 4 (b), the experimental system consists of a sensor head, operating at 1.4 GHz, a VNA, a data logger, and control software. The changes in resonant frequency, 3 dB bandwidth, and insertion loss are proportional to the glucose variation. Overall, the results, including error grid and MARD[5] are promising but the current system involves the use of a portable network analyzer and is not fully wearable, which could limit its practicality for everyday use.

[4] Choose the highest dielectric variation at the given frequency.
[5] MARD: Mean absolute relative difference is currently the most common metric used to assess the performance of a continuous glucose monitoring device CGM systems



(a) (b)

Figure 4: (a) Illustration showing the sensor attached to human skin. (b) the proposed microwave non-invasive blood glucose monitoring system [6]

A large cluster in Figure 1 concerns agricultural issues, particularly soil salinity and soil moisture analysis. The accumulation of salts on the soil surface can dramatically affect crop production [14]. Within this context, to monitor the soil salinity, the complex dielectric permittivity of soil samples was extracted from scattering parameters in the [0.05 – 3] GHz frequency range to evaluate the salinity index [17]. Experimental results confirmed the validity of their approach using soil samples. However, a major limitation is the laboratory VNA used, which makes measurements difficult under realistic conditions. Another application highlighted in the same cluster is soil contamination detection. In [45], the authors evaluate a non-invasive detection method based on ground penetrating radar (GPR[6]), including a VNA, at L-Band frequencies (1-2 GHz). A significant electromagnetic variation in the reflected signal of both contaminated and uncontaminated sandy soil was noticed.

Other pertinent studies referred to in Figure 1 have shown further promising applications using a VNA. To name a few, there is a wideband [3-10] GHz microwave imaging system designed for root phenotyping [11], respiration rate monitoring [10], pharmaceutical composition determination [48] and food safety testing [46].

So far, for the wide range of applications covered in this introduction, through the use of a VNA, three major insights must be considered:

[6] Ground-penetrating radar (GPR) is a geophysical technique that uses radar pulses to non-destructively image the subsurface.

1) The need for an **accurate** VNA as a **readout topology**.

2) The need for a **wideband** frequency from MHz to GHz to cover the wide scope of applications previously mentioned.

3) The high cost associated with instrumental VNAs, which limits the sensor's industrialization.

To achieve the objective of developing a vector network analyzer (VNA) that is both compact and cost-effective while fulfilling the cited needs, an integrated solution was pursued based on an **inductorless architecture** with a small silicon footprint to lower the cost.

How a VNA integration would unlock a complete noninvasive sensor implementation?

Back to the initial connection noted in Figure 1, the relationship between the VNA, antenna, and sensor becomes more explicit. The sensor consists of a VNA as a readout topology and an antenna part (or resonator). The major contribution of the studied publications deals with the miniaturization of antennas or resonators for non-invasive monitoring applications. This Ph.D. contribution focuses on designing the second main sensor component, namely, a wideband network analyzer, to unlock a complete non-invasive sensor implementation, as delimited in Figure 5.

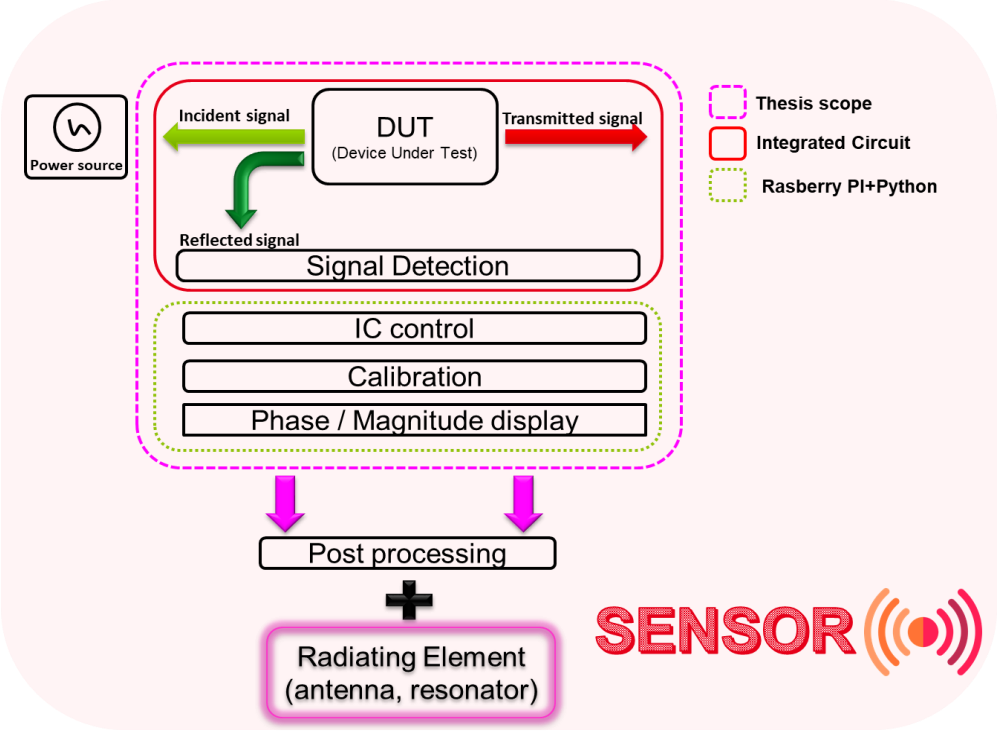


Figure 5: Thesis contribution

To achieve the objective of this thesis, the following intermediate goals are addressed:

1) Model the block diagram of the broadband vector network analyzer.

2) Analyze the proposed block diagram in terms of sensitivity, power, linearity, and noise.

3) Design and validate the circuit's sub-blocks in standalone mode, including post-simulation and measurement results (the first circuit contribution).

4) Validate the circuit's functionality as a complete vector network analyzer through post-simulation and measurement results, external calibration, and digital circuit control (the second circuit contribution).

THESIS OUTLINE

This contribution is structured as follows:

The first chapter of this thesis provides a theoretical background for the subsequent chapters. The chapter begins with an introduction to the concepts related to a vector network analyzer (VNA) system for readers who are unfamiliar with the subject. The first section of the chapter outlines the fundamentals of measuring scattering parameters with a VNA, starting with the definition of scattering parameters based on wave propagation theory. The measurement of scattering parameters in a two-port VNA is then described, along with a discussion of the imperfections of a typical two-port VNA measurement configuration, including systematic errors. Calibration procedures are used to characterize and correct these errors mathematically. The second section of the chapter reviews the state-of-the-art architectures for miniaturized wideband network analyzers. Finally, the chapter provides a summary of the existing literature on this topic and the positioning of the thesis with regard to the state of the art.

The subsequent chapters delve deeper into the design and implementation of a VNA system, starting with the architecture choice in chapter two. Indeed, the second chapter focuses on the architecture of the proposed VNA system. The first section analyzes the noise of both the VNA receiver and the demodulator based on commercialized circuits. The main system-level requirements and signal characteristics are defined, and the complete circuit block diagram is introduced. The second section describes the sub-block specifications derived from the complete circuit study.

The remaining chapters focus on the overall assembly of the proposed VNA system design and characterization. In the third chapter, the proposed VNA system is reviewed in its entirety. The system consists of five key components, including a directional circuit, an image rejection circuit, an amplification circuit, a receiver circuit, and an amplitude and phase detection circuit. The chapter presents measurements of three building blocks in a standalone configuration and describes how they were used to improve the second fabricated version of the complete VNA integrated circuit.

The fourth chapter presents the second contribution of this thesis, a complete vector network analyzer. The VNA system characterization is initiated with the introduction of two

devices under test. The first device is a magnitude and phase tuner used to seek the complete VNA magnitude and phase DC outputs dynamic range. The second device is a resonant LC circuit, whose receiver outputs were processed and calibrated using a one-port calibration process in reflection mode to extract systematic errors and provide the corrected data. Similarly, transmission measurements were done and analyzed further using the same LC device under test in the last section.

Finally, a general conclusion and perspectives for future work will wrap up the thesis manuscript.

Chapter 1: VECTOR NETWORK ANALYZER FUNDAMENTALS

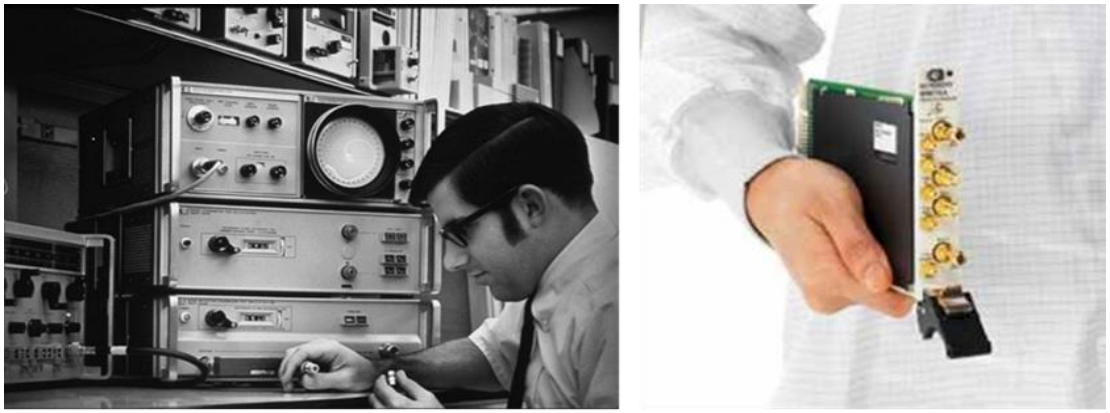
The intention behind this chapter is to provide the theoretical background for the later chapters. It aims to describe this thesis' specifics for readers unfamiliar with concepts related to a VNA system. Accordingly, the first section of this chapter reviews the fundamentals of measuring scattering parameters with the VNA. Initially, the definition of scattering parameters is introduced based on wave propagation theory. Then, the measurement of scattering parameters in a two-port VNA is described, along with an analysis of the imperfections of a typical two-port VNA measurement configuration. Among the errors caused by these imperfections are systematic errors. Therefore, these can be characterized during the calibration procedure and then eliminated from the effective scattering parameter measurements during the correction process. In both procedures, these VNA errors are mathematically modeled. The model obtained during calibration is then used to correct the imperfections of the VNA. A second section will go over the state-of-the-art architectures for a miniaturized network analyzer. Finally, in the last part, a position toward the existing literature will be established for this thesis.

1.1 FUNDAMENTALS

The background theory of VNA operation is discussed in detail in this first section through a system level overview. The principles of measuring scattering parameters are then reviewed. Following that, each subsystem is described in greater detail, with emphasis on the VNA error sources. The calibration theory is then thoroughly examined, as this is critical to the successful use of the VNA for high-precision measurements.

1.1.1 INTRODUCTION

Significant progress has been made over the last fifty years to improve the performance of VNAs [1]. In 1960, as captured in Figure 6 (a), the earliest commercially available network analyzer able to measure amplitude and phase was the Hewlett-Packard 8407 RF with a bandwidth of up to 110 MHz [49]. Since then, there has been a boom in industrialization and a growing need for larger bandwidth. A milestone has been reached recently with the introduction of the compact M937XA VNA PXI series, up to 26.5 GHz, Figure 6 (b) [50].



(a) (b)

Figure 6: (a) The 8410 network analyzer up to 110 MHz [49], (b) The PXI VNA (95 x 178 x 19 mm) up to 26.5 GHz [50]

Basically, a vector network analyzer measures the ratio of incident to reflection or transmission through the device under test. Even though the new analyzers have extra features like multiple ports and noise measurements with fast electronic calibration modules, they still need to get smaller and cheaper so they can be used for large-scale deployments of the emerging non-invasive applications

mentioned above (General Introduction). Thereafter, the following paragraph deals with the theory of wave's propagation related to the theoretical definition of scattering parameters.

1.1.2 UNDERSTANDING SCATTERING PARAMETERS

Scattering parameters describe the electrical behavior of linear electrical networks when stimulated by electrical signals. These parameters link the amplitude and phase of forward and backward traveling waves on a transmission line.

The input and output ports of a circuit are numbered. Note that a common notation is to use the subscripts m and n for the general S-parameter $S_{m,n}$, where m is the number of the receiver port and n is the number of source port. For example, $S_{1,2}$ is the transmission coefficient for a wave sourced at port 2 and received at port 1. By now, to establish the connection between the wave's amplitudes traveling through the device under test and the theoretical definition of the two-port S-parameters, the concept of wave propagation has been introduced.

Figure 7(a) depicts a transmission line circuit in which a sinusoidal voltage source V_s with an internal impedance Z_s drives a transmission line with Z_c as characteristic impedance and length L, terminated with a load Z_L. When a signal goes through the load, a forward voltage V^+ and current wave I^+ originate at x=0 and travel towards the load. When the wave arrives at the load, a reflected wave is generated, as shown in Figure 7(b). So, the voltage of the wave that gets reflected is linked to the voltage of the wave that hits it by:

$$V^- = \frac{Z_L - Z_C}{Z_L + Z_C} \; V^+ \tag{1}$$

Where $\frac{Z_L - Z_C}{Z_L + Z_C}$ is the voltage reflection coefficient at the load Γ_L. In this scenario, when the load is matched to the transmission line, the reflection coefficient is zero and no reflection occurs. Otherwise, when the device under test is not matched to the load a reflected wave V^- is created and travels back to the source.

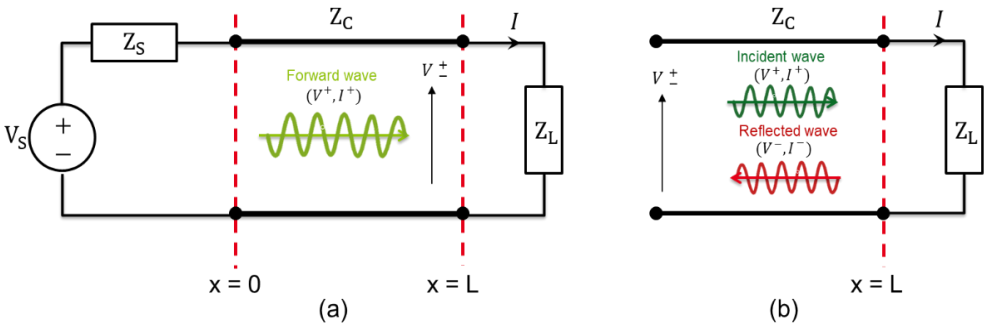


Figure 7: (a) Forward wave through a transmission line circuit, (b) Reflection at the load

Similarly, as illustrated in Figure 8, upon arrival at the source the wave gets reflected again, creating a forward voltage wave $V^{\pm}$. This voltage is expressed as follows:

$$V^{\pm} = \frac{Z_S - Z_C}{Z_S + Z_C} V^{-} \tag{2}$$

Where $\frac{Z_S - Z_C}{Z_S + Z_C}$ is the voltage reflection coefficient at the source Γ_S. In this case, when the source is matched to the transmission line the reflection coefficient is zero and there is no reflected voltage at the source. At this point, the two-port network approach and the transmission line reflections will be combined to introduce the scattering parameters.

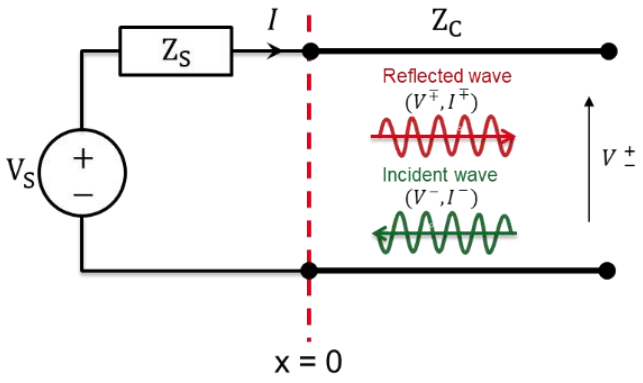


Figure 8: Reflection at the source

Indeed, as shown in Figure 9, the incident wave is impinging on either from the first port a_1 or from the second port a_2. These waves give rise to the reflected waves, b_1 and b_2. When a two-port network is inserted into a transmission line, the S parameters are defined by relating these travelling waves by a linear equations expressed in (3).

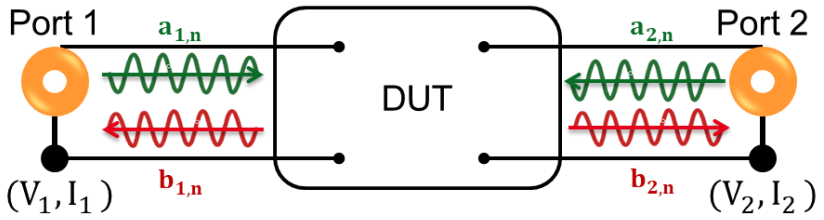


Figure 9 : Incident and reflected waves at ports 1 and 2, in a test environment whose reference impedance is Z_c. The $a_{i\in[1,2]}$ denote incident energy waves at the network ports, while $b_{i\in[1,2]}$ are reflected energy waves at the system ports.

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \tag{3}$$

On the other hand, the incident and reflected waves are related to the voltage and current waves at each port as follows:

$$\begin{cases} V_1 = a_1 + b_1 \\ I_1 = \dfrac{a_1 - b_1}{Z_c} \\ V_2 = a_2 + b_2 \\ I_2 = \dfrac{a_2 - b_2}{Z_c} \end{cases} => \begin{cases} a_1 = \dfrac{V_1 + Z_c I_1}{2} \\ a_2 = \dfrac{V_2 + Z_c I_2}{2} \\ b_1 = \dfrac{V_1 - Z_c I_1}{2} \\ b_2 = \dfrac{V_2 - Z_c I_2}{2} \end{cases} \tag{4}$$

Where Z_c is the characteristic impedance of the transmission line connected to the two-port network. In order to make the travelling waves consistent with the law of conservation of energy, such that the wave has a unit root-mean-square amplitude, the voltages are normalized to $\sqrt{Z_c}$. Hence , power waves are introduced and defined as follows [51]:

$$\begin{aligned} a_{1,n} &= \frac{V_1 + Z_c I_1}{2\sqrt{Z_c}} \quad b_{1,n} = \frac{V_1 - Z_c I_1}{2\sqrt{Z_c}} \\ a_{2,n} &= \frac{V_2 + Z_c I_2}{2\sqrt{Z_c}} \quad b_{2,n} = \frac{V_2 - Z_c I_2}{2\sqrt{Z_c}} \end{aligned} \tag{5}$$

From equation (3), the two-port S parameters are defined as follows:

$$S_{11} = \left.\frac{b_{1,n}}{a_{1,n}}\right|_{a_{2,n}=0}$$
$$S_{12} = \left.\frac{b_{1,n}}{a_{2,n}}\right|_{a_{1,n}=0}$$
$$S_{21} = \left.\frac{b_{2,n}}{a_{1,n}}\right|_{a_{2,n}=0} \quad (6)$$
$$S_{22} = \left.\frac{b_{2,n}}{a_{2,n}}\right|_{a_{1,n}=0}$$

In theory, determining the S-parameters using a VNA is a straightforward process. In fact, two modes are established to measure the four scattering parameters. First, a reflection free termination is used (Γ=0) for the forward measurement in Figure 10 (a), which means that $a_{2.n} = 0$. Thus, Port 1 is simulated by the incident wave ($a_{1.n} \neq 0$). Under these conditions, a sinusoidal signal is injected into the device under test. The VNA records the amplitude and phase of the signal reflected back from the first port **"the *input reflection coefficient* S_{11}"** and also the amplitude and phase of the signal conveyed through the device under test to the second port ***"the forward transmission coefficient S_{21}".*** The second mode, as shown in Figure 10 (b) is reverse measurement, which corresponds to a match (Γ=0) at port 1 ($a_{1.n} = 0$) while port 2 is simulated by the incident wave $a_{2.n} \neq 0$. Under these conditions, the output reflection coefficient S_{22} on port 2 and the reverse transmission coefficient S_{12} between port 2 and port 1 are measured.

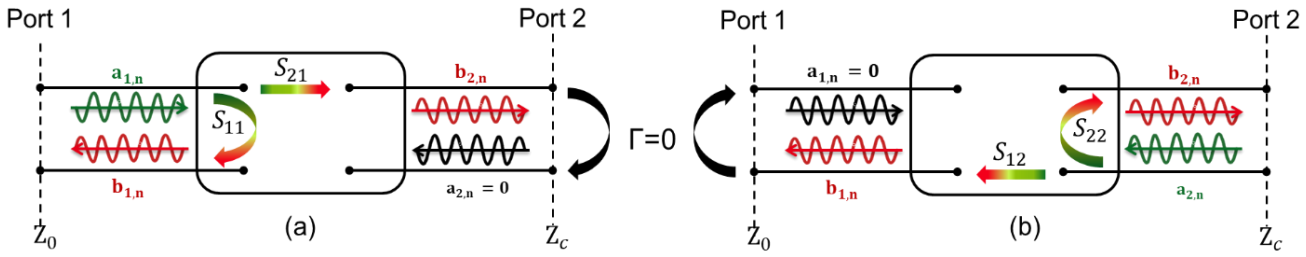


Figure 10: The four scattering parameters measurement (a) Forward measurement, (b) reverse measurement

1.1.3 VECTOR NETWORK ANALYZER ARCHITECTURES

The implementation of such an instrument can be classified into two main categories with different architectures according to the principles used: wave interference and wave separation.

Figure 11 depicts the first architecture, which incorporates two Six-Port Reflectometer (SPR) that uses only power readings to determine the complex reflection coefficients $\Gamma_1 = \frac{b_1}{a_1}$ and $\Gamma_2 = \frac{b_2}{a_2}$ of the device under test. The interference method does not separate the stimulus from the response. Indeed, several controlled linear combinations of the two waves are created in the measurement system, and the resulting amplitudes are observed.

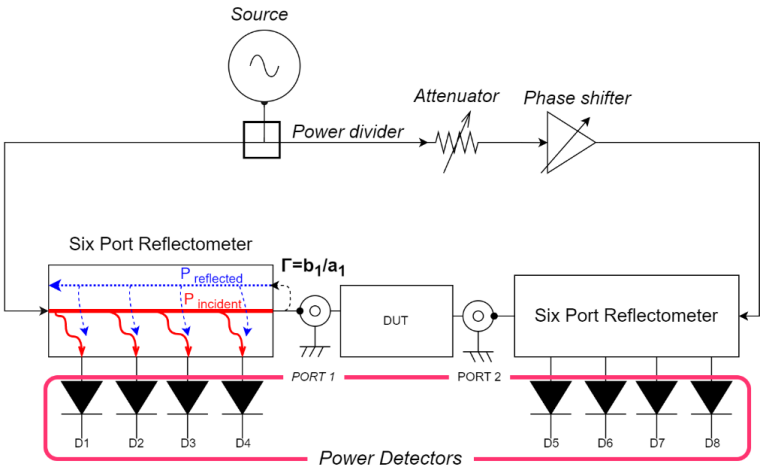


Figure 11 : Network analyzer architecture based on two 6 port junctions

Through a system level overview, an SPR consists of a circuit with two ports for signal input and output, and four ports with their corresponding power detectors $D_{1,2,3,4}$ that sample the standing wave within the transmission line. The input port is connected to the source, and the output port is connected to the load. This load can generate a mismatch that leads to reflections measured by the reflectometer. From the linear equations previously mentioned (3) divided respectively by a_1 and a_2, reflection coefficient are expressed in (7), and by eliminating $\frac{a_2}{a_1}$, the resulting equation (8) links the four scattering parameters. By setting three different attenuation and phase shift values, the parameters S11, S22, and Δ could be extracted from (8). Next, the parameters S12, S21 are linked to Δ and based on reciprocity condition ($S_{12} = S_{21}$), both parameters are calculated from (9). For reciprocal and non- reciprocal network, the calculation of the phase is explained in details in [52] and [53].

$$\begin{cases} \Gamma_1 = \dfrac{b_1}{a_1} = S_{11} + S_{12}\dfrac{a_2}{a_1} \\ \Gamma_2 = \dfrac{b_2}{a_2} = S_{22} + S_{22}\dfrac{a_1}{a_2} \end{cases} \quad (7)$$

$$\Gamma_2 S_{11} + \Gamma_1 S_{22} - \Delta = \Gamma_1 \Gamma_2 \text{ ,where } \Delta = S_{11}S_{22} - S_{12}S_{21} \quad (8)$$

$$|S_{12}| = |S_{21}| = \sqrt{|S_{11}S_{22}| - \Delta} \quad (9)$$

On the other hand, Figure 12 illustrates the basic building blocks of the second architecture. It is based on signal separation, where a single stimulus (incident wave) is injected into one of the ports to provide the incident signal that occurs on the device under test. The DUT responds to the incident signal by reflecting portions of it and transmitting the remainder. Since the incident and reflected waves arrive at the same port, they must be separated to determine the reflection coefficient. For this purpose, power splitters, directional couplers or directional bridges (Wheatstone bridges) are used. The third main element is the receiver/detector section, which is necessary to compute the ratio of amplitudes and phase differences between the DUT and stimulus response, mainly at a lower intermediate frequency so that precise measurements can be made. The four scattering parameters are extracted directly in magnitude and phase from $a_{1,2}$ and $b_{1,2}$ as expressed in (6).

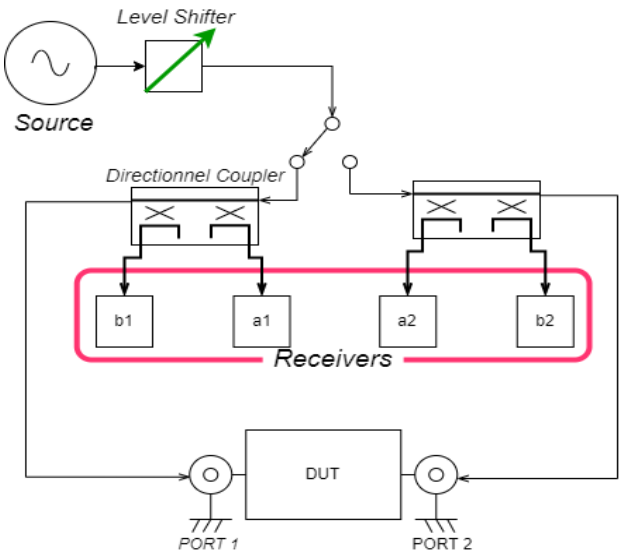
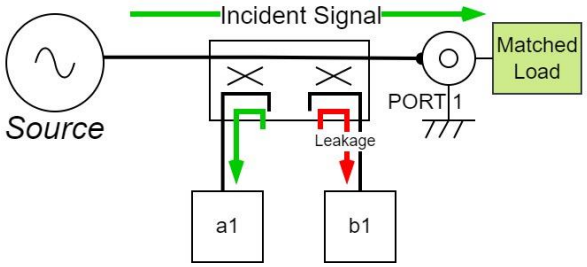
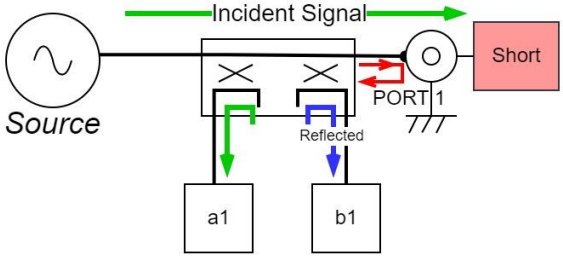
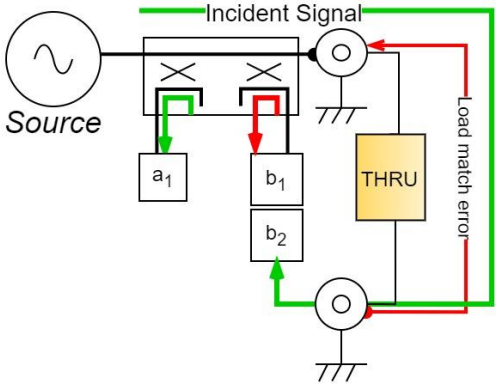


Figure 12 : Network analyzer architecture based on separation method

To determine the most suitable architecture for the circuit proposed in this Ph.D. thesis work, a comparison between both architectures based on the state of the art will be addressed in Section 1.2 of this chapter. Overall, the studies provide important insights for selecting the second architecture. Consequently, the next sub-section explores details related only to the second architecture, in terms of error sources and also introduces the notion of error boxes that corrupt the effective scattering parameters. Finally, it presents the calibration process and relates the measured (uncorrected) scattering parameters to the corrected ones.

1.1.4 VNA MEASUREMENT ERRORS AND CALIBRATION TECHNIQUES

A VNA measures both the magnitude and phase of S parameters. However, there will invariably be significant errors in these measurements that should be removed to obtain an accurate result. Indeed, there are three main types of measurement errors: systematic errors, random errors, and drift errors. Systematic errors are mainly caused by predictable flaws in the test setup (equipment, cables) or configuration. These are illustrated and defined in Table 1. The second category is random errors. This is an irregular error caused mainly by noise emitted from the test equipment or test setup that varies with time. These inaccuracies remain in the measurement results after a calibration, and they affect the degree of precision that can be attained. Instrument noise errors are prevalent examples; these errors can be reduced by increasing the signal power supplied to the DUT, reducing the IF bandwidth, or enabling sweep averaging. Another error could occur when the electrical characteristics of the mechanical RF switch used in the measuring device change with each activation, leading to switch repeatability errors. These errors can be reduced by performing measurements without any switching operations. Finally, connector repeatability errors are caused by fluctuations in the electrical characteristics of connectors caused by wear. However, careful handling of connectors can help reduce these errors.

Errors illustrations	Errors definitions
	***Directivity errors*** result from signal leakage, which occurs when a portion of the incident signal energy is fed through the directional coupler into the reflected signal receiver. In fact, during calibration, a charge is connected to port 1, and the signal measured at the test receiver shows leakage through the coupler (the red path in the figure on the left).
	***Source matching errors*** *are* caused by a mismatch between the source port and the input of the device under test. This is because a portion of the reflected signal from the DUT returns to the DUT's input. In this case, rather than having only the reflected signal at the receiverb_1, a proportion of the reflected signal and internal reflection (red path) combined with the incident signal feeds the receiver b_1.
	***Load matching errors*** arise from a difference between the DUT's output impedance and the test port's impedance. Instead of measuring only the transmitted signal at port b_2, in reality, a fraction of the transmitted signal through the device under test is reflected at port 2 and then returned back to the DUT's output (red path). Indeed, the signal measured at b_1 is the reflected signal off of port 2.

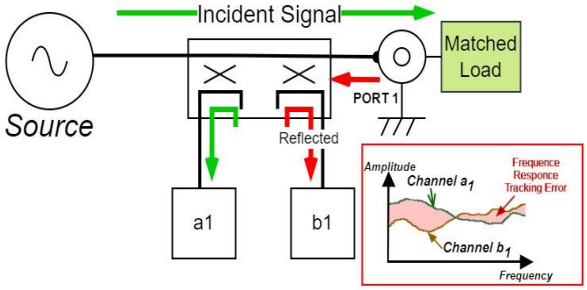
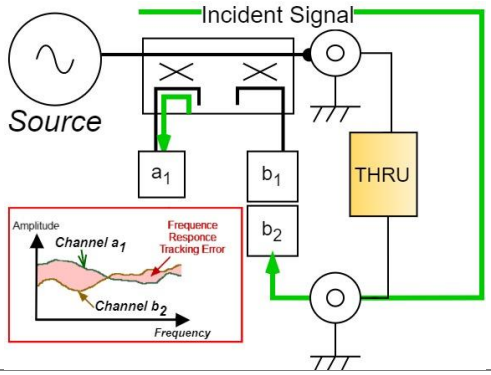
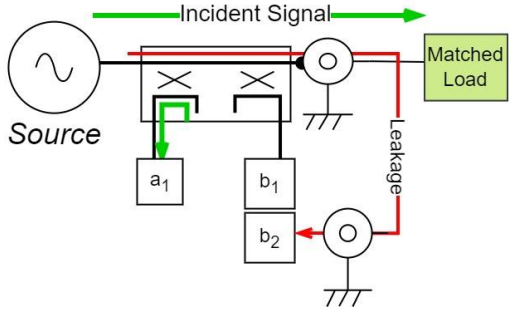
	***Reflection tracking errors*** result in differences in the frequency response between the test receiver (which measures the reflected signal) and the reference receiver (which measures the incident wave) of the source port in reflection measurements.
	***Transmission tracking errors*** are caused by the fact that the frequency responses of the transmission receiver and the reference receiver are different.
	**Isolation errors** are due to signal leakage (also known as "crosstalk") that is traveling through the device under test from the source port to the test port. In such a case, a charge is connected to both ports during the calibration, so the measured signal at the $b_2$receiver displays the leakage along the red path. This makes it difficult to test high-isolation circuits, such as switches in the open position or high rejection level filters.

Table 1: VNA systematic errors

A third error source is drift error, referring to the measurement drift over time. It is due to the fluctuations occurring within the test equipment and setup after a user calibration. Typical examples include the thermal expansion of connecting cables and the thermal drift of the frequency converter within the vector network analyzer, humidity fluctuations, and mechanical movement of the test setup. The rate of drift determines how frequently additional calibrations are needed. The main assumption is that systematic errors are repeatable and can be measured and fixed almost right away during the calibration process, while residual errors are limited by the quality of the calibration standards.

Finally, a linear calibration procedure is applied to remove the systematic errors once the VNA is calibrated. However, the drift, stability, and repeatability errors will degrade the VNA's performance even after a user calibration. Therefore, before the full two-port model can be further developed, the one-port error model and calibration should be explained.

1.1.4.1 One Port error model and calibration

At present, the common model for one-port calibration and error correction remains the Error Box introduction, which modifies the actual DUT reflection coefficient measured by an "ideal reflectometer", as illustrated in Figure 13.

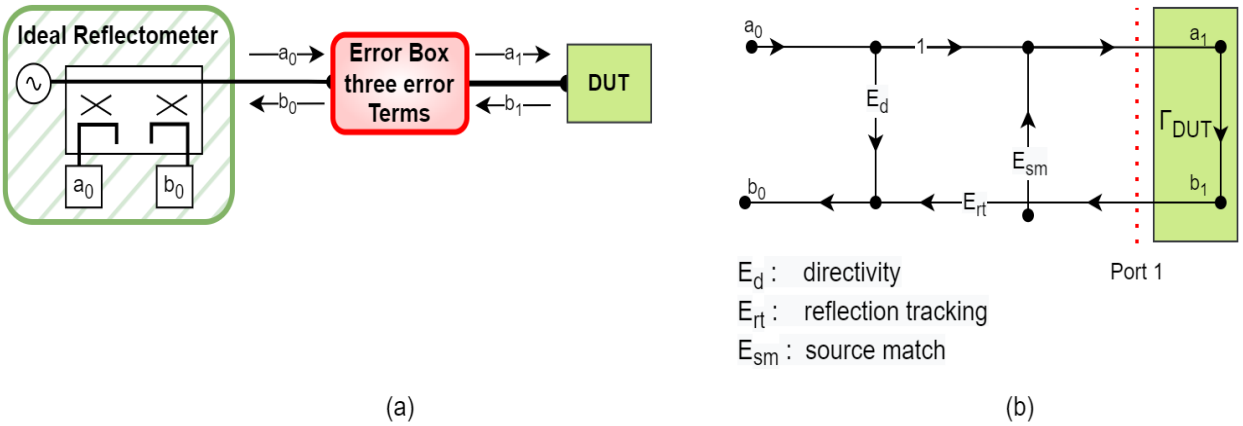


Figure 13: (a) One-Port VNA (reflectometer) including error box, (b) 3-Term Error representation

Solving the one-port flow graph leads to a bilinear function of the effective and measured reflection coefficients (10). For reflection measurements, there are three error terms that can be expressed in linear form (11). However, these three error terms can be determined by measuring three known standards (Open, Short, and Load), providing three concurrent equations from (11) that can be solved. Finally, this equation is reversed to find the actual reflection coefficient considering the measured result and the three error terms (12).

$$\begin{cases} \Gamma_{meas} = \frac{b_0}{a_0} = \frac{E_d - A\Gamma_{DUT}}{1 - E_{sm}\Gamma_{DUT}} \\ \Gamma_{DUT} = \frac{\Gamma_{meas} - E_d}{\Gamma_{meas}E_{sm} - A} \end{cases}, \quad \text{with } A = E_d E_{sm} - E_{rt} \tag{10}$$

$$E_d + \Gamma_{DUT}\Gamma_{meas}E_{sm} - \Gamma_{DUT}A = \Gamma_{meas} \tag{11}$$

with 3 Known Γ_{DUT}, the resultant 3 Γ_{meas} solve the 3 Term errors E_d,E_{sm} and E_{rt} :

$$\begin{cases} \mathrm{E_d} + \Gamma_{\mathrm{DUT,Open}}\Gamma_{\mathrm{meas,Open}}\mathrm{E_{sm}} - \Gamma_{\mathrm{DUT,Open}}\mathrm{A} = \Gamma_{\mathrm{meas,Open}} \\ \mathrm{E_d} + \Gamma_{\mathrm{DUT,Short}}\Gamma_{\mathrm{meas,Short}}\mathrm{E_{sm}} - \Gamma_{\mathrm{DUT,Short}}\mathrm{A} = \Gamma_{\mathrm{meas,Short}} \\ \mathrm{E_d} + \Gamma_{\mathrm{DUT,Load}}\Gamma_{\mathrm{meas,Load}}\mathrm{E_{sm}} - \Gamma_{\mathrm{DUT,Load}}\mathrm{A} = \Gamma_{\mathrm{meas,Load}} \end{cases}$$

$$\Gamma_{\mathrm{DUT}} = \frac{\Gamma_{\mathrm{meas}} - \mathrm{E_d}}{\mathrm{E_{sm}}(\Gamma_{\mathrm{meas}} - \mathrm{E_d}) + \mathrm{E_{rt}}} \tag{12}$$

1.1.4.2 Two Port error model and calibration

Following from the above, the two-port case can be modeled in the same manner as the one-port. An error adapter is inserted between the two-port DUT and the 'perfect reflectometer' measurement ports. This error adapter contains the six error terms for the forward direction, and a similar six term model is used for the reverse direction. The twelve term error model was first introduced for commercial VNAs independent of the test set configuration, and quickly became the standard model for describing systematic measurement errors in a two port VNA [54].

As mentioned earlier, the measurement process includes two modes: forward and reverse modes. In the forward mode, as illustrated in Figure 14 (a), the first step is to calibrate the first port using the one port calibration method previously presented. This process solves the first three forward errors E_{sm}, E_d and E_{rt}, as described in the preceding paragraph (1.1.4.1). The second step involves connecting a known load to ports 1 and 2, which measures S_{21meas} and then gives the isolation error E_I value. Finally, the last step is to connect the two ports together, E_{lm} is solved by measuring port 2-matching with the calibrated port 1. E_{tt} is solved by measuring the transmitted signal (13). Finally, the same process is performed on the reverse path as well, Figure 14 (b).

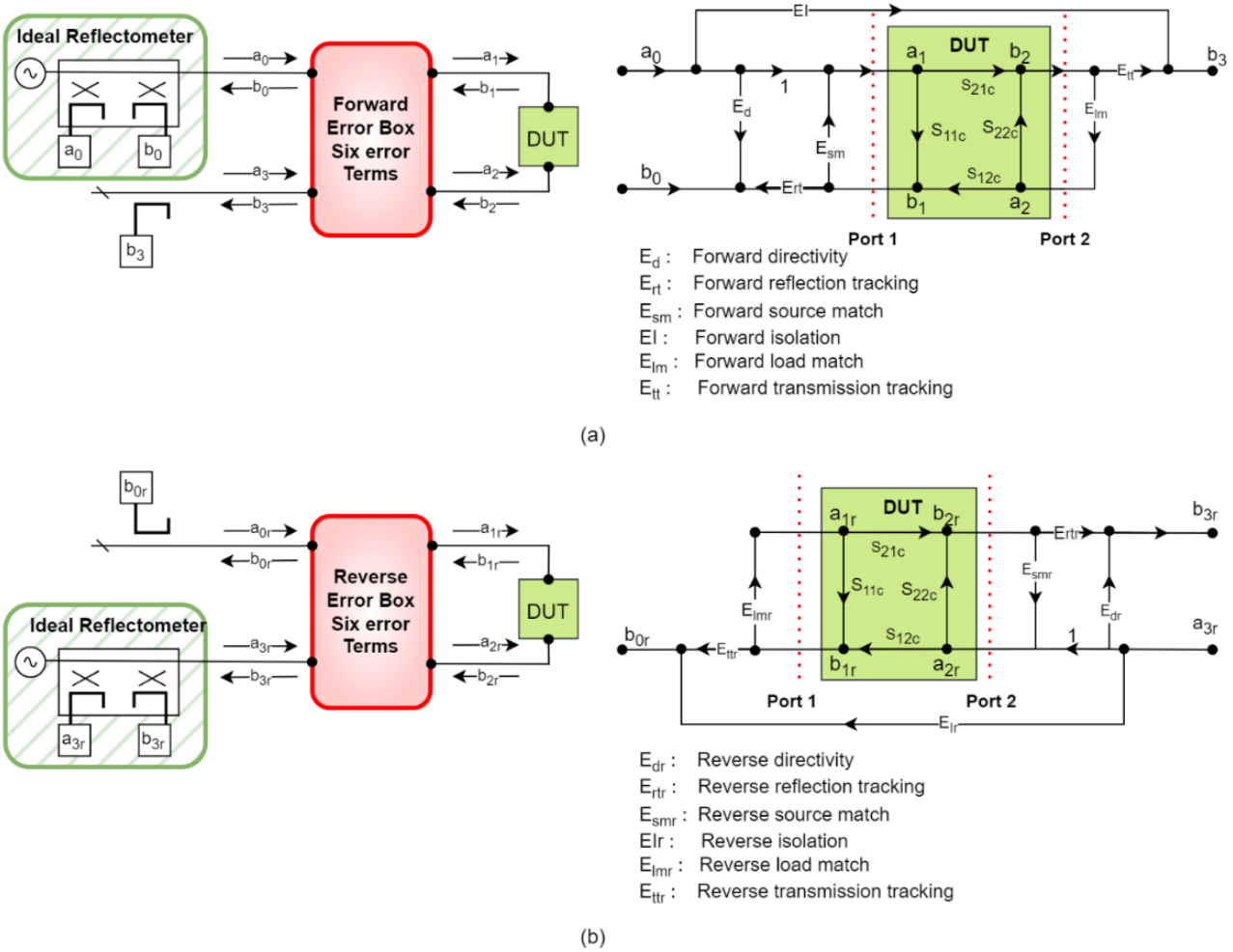


Figure 14 : 12- Term Error model in (a) Forward mode and (b) Reverse mode

$$E_{lm} = \frac{S_{11meas-E_d}}{S_{11meas}E_{sm} - B}$$

$$E_{tt} = (S_{21meas} - E_I)(1 - E_{sm}E_{lm}) \qquad (13)$$

$$\text{with } B = E_d E_{sm} - E_{rt}$$

Indeed, solving the forward flow yields to S_{11c} and S_{21c} measurements, and based on the reverse model S_{22c} and S_{12c} are solved. Hence, by combining the forward and reverse models, the four corrected scattering parameters and the 12 errors are linked. If the error terms are known, the corrected scattering parameters[7] could be extracted from (14).

[7] Refer to [56] for a detailed demonstration.

$$S_{11c} = \frac{\left(\frac{S_{11_{meas}} - E_d}{E_{rt}}\right)\left(1 + \frac{S_{22_{meas}} - E_{dr}}{E_{rtr}} E_{smr}\right) - E_{lm}\left(\frac{S_{21_{meas}} - E_I}{E_{tt}}\right)\left(\frac{S_{12_{meas}} - E_{Ir}}{E_{ttr}}\right)}{C}$$

$$S_{21c} = \frac{\left(\frac{S_{21_{meas}} - E_I}{E_{tt}}\right)\left(1 + \frac{S_{22_{meas}} - E_{dr}}{E_{rtr}} (E_{smr} - E_{lm})\right)}{C}$$

$$S_{12c} = \frac{\left(\frac{S_{12_{meas}} - E_{Ir}}{E_{ttr}}\right)\left(1 + \frac{S_{11_{meas}} - E_d}{E_{rt}} (E_{sm} - E_{lmr})\right)}{C} \quad (14)$$

$$S_{22c} = \frac{\left(\frac{S_{22_{meas}} - E_{dr}}{E_{rtr}}\right)\left(1 + \frac{S_{11_{meas}} - E_d}{E_{rt}} E_{sm}\right) - E_{lmr}\left(\frac{S_{21_{meas}} - E_I}{E_{tt}}\right)\left(\frac{S_{12_{meas}} - E_{Ir}}{E_{ttr}}\right)}{C}$$

With $C = \left(1 + \frac{S_{11\_meas} - E_d}{E_{rt}} E_{sm}\right)\left(1 + \frac{S_{22\_meas} - E_{dr}}{E_{rtr}} E_{smr}\right) - E_{lm} E_{lmr}\left(\frac{S_{21\_meas} - E_I}{E_{tt}}\right)\left(\frac{S_{12\_meas} - E_{Ir}}{E_{ttr}}\right)$

Up to this point, this first section introduced the concepts of waveguide voltage and normalized power (normalized voltage waves). This allows relating the scattering parameters with transmission line theory and then expressing the scattering matrix as a function of the traveling waves. As noted, this section provides the calibration procedure for the separation based architecture. Otherwise, a detailed dual six port error and calibration procedure are described in [55].

In the following section, the objective is to highlight recent trends in broadband vector network analyzer integration solutions. The intent is to highlight the main merits and limitations of both signal separation and wave propagation based VNA architectures.

1.2 PRIOR ART

As mentioned in the introduction section, numerous studies have demonstrated the effectiveness of microwave frequencies as a potential non-invasive sensing approach in biomedical and agricultural fields (see Figure 1). It has been shown that the difference in complex permittivity between tissues or two different mediums is related through algorithms (ex., the Cole-Cole permittivity model) to the scattering parameters measured primarily with a vector network analyzer [56]. Since then, efforts have been made to seek a portable, compact solution to replace the laboratory's stationary VNA. In the following, this review will focus only on the broadband contributions.

Back in 1977, ENGEN focused on the theoretical development needed to optimally implement a six-port reflectometer and proposed a proof of concept to validate the design strategy [57]. Within the same year, in [58], HOER introduced the first benchtop dual six port microwave network analyzer (2-18 GHz), as shown in Figure 15 (a), which is able to measure the four scattering parameters of a DUT by incorporating two identical six-port reflectometers designed from strip line in-phase power dividers and quadrature hybrids and fed by a common source and dividing network. It also includes a phase shifter to adjust the phase difference between the signal inputs to the six ports. The latter calibration strategy was developed earlier by ENGEN [59]. Aside from their promising performance, the main drawbacks of diode detectors were their bulkiness and temperature sensitivity. Thus, to reduce dimensions, a new approach was developed first by BILIK in 1988 [60]. As presented in Figure 15 (b), a microstrip waveguide reflectometer is presented, consisting of only Lange couplers and Wilkinson power dividers. Besides, its major inconvenience was the very high losses. Similarly, as shown in Figure 15 (c), BILIK demonstrated a GaAs monolithic microwave integrated circuit (MMIC) that operates from 80 MHz to 7 GHz on a 10 mm by 10 mm alumina substrate [61]. In 2015, in [62], the authors Bauch & Hofmann presented the first six port VNA that is capable of operating in an ultra-broadband frequency range from 2 to 30 GHz (Figure 15(d)). The design consists of four -3 dB couplers and one -6 dB coupler operating with a low odd-mode impedance to cover the bandwidth. In the same year, Trenz and Hofmann presented a planar broadband six port reflectometer ranging from 2 to 29 GHz on a single multilayer PCB[8] stuck-up with an area of 66 x 55 mm² [63, p. 3]. The architecture is based on a four stage Wilkinson power divider with

[8] PCB for printed circuit board

microstrip interconnect lines that have been designed to meet the line length criteria for broadband functionality. Recently, in 2018, a modified topology called, Five port reflectometer (FPR) was realized for ultra-wideband measurements (0.1 to 40 GHz) using commercial power splitters. The idea is to get rid of the extra reference port to reduce the circuit area [64].

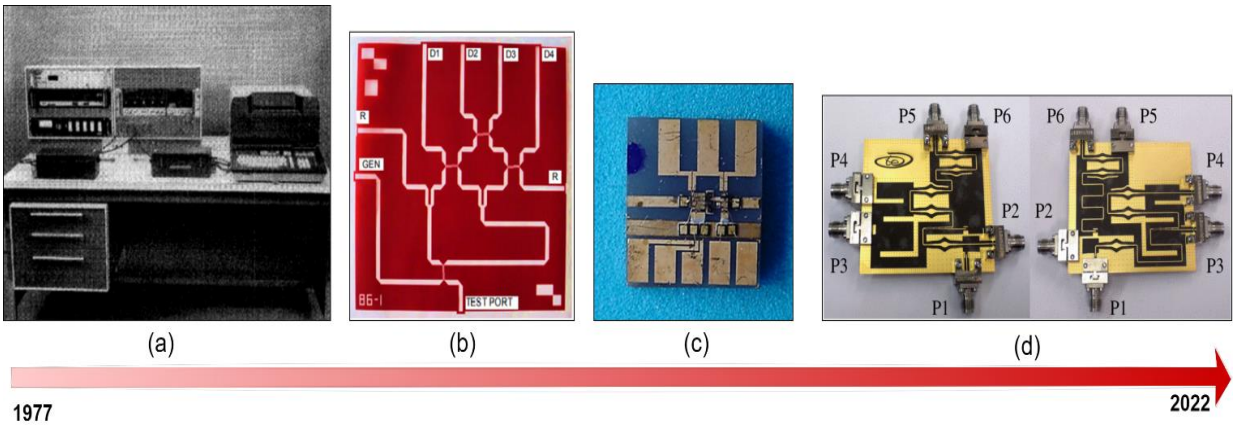


Figure 15 : Wideband six port vector network analyzer circuit evolution: (a)dual six port network analyzers circuit , (b) X-band microstrip SPR ,(c) Monolithic GaAs IC, (d) front and bottom side of the UWB reflectometry system

Previous systems had limited dynamic range due to the low dynamic range of the power detectors used. To overcome this issue, a novel architecture based on phase shifters was presented in studies [65] and [66] by ABOU-KHOUSA. The architecture utilizes a single power detector and an electronically controllable phase shifter, which are inserted between the device under test and a standing wave probing device, as shown in Figure 16. By using this architecture, the magnitude and phase of the reflection coefficient can be determined from the standing wave voltages at various phase shift settings. This approach enables the system to achieve a higher dynamic range compared to previous systems that rely solely on power detectors.

The utility of this small portable reflectometer includes broadband device characterization, material characterization and nondestructive testing applications; however, it suffers from two main drawbacks: first, the complexity of designing a controllable wideband band phase shifter that can still be integrated into a restricted surface.

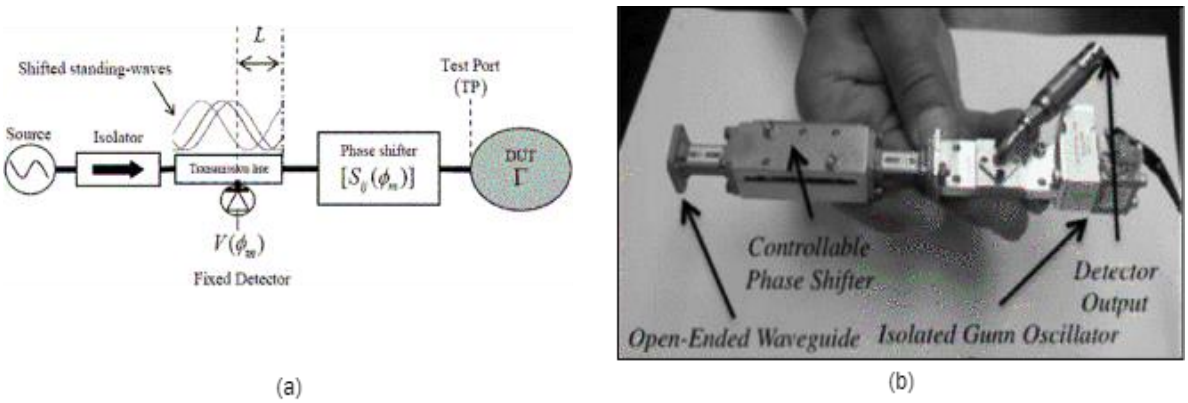


Figure 16 : (a) Standing-wave-based reflectometer, (b) handheld Ka-band (26.5-40 GHz) reflectometer devised for imaging applications [66, p.]

Regarding the second architecture, only a few articles have proposed wideband miniaturized network analysis circuits based on the separation method architecture. In 2014, single- and dual-port fully integrated millimeter-wave ultra-broadband vector network analyzers (50-100 GHz) were realized in 0.35 um SiGe, Figure 17 (a). Both circuits are based on a heterodyne architecture. They draw 600 and 700 mA from a 3.3 V supply, respectively [67]. Then, in 2016, a 4–32 GHz chipset for a highly integrated heterodyne two-port Vector Network Analyzer was published [68, p. 32]. The chipset is comprised of a stimulus integrated circuit (IC) with two selectable single-ended output channels, a four-channel receiver IC and a broadband directional coupler on a chip based on cascaded quarter-wavelength coupled line segments, Figure 17 (b). After this first successful proof of concept, the same research group published an extended version of the previous circuit. In combination with a modular hardware demonstrator and a calibration technique, the chip consists of an integrated stimulus for two port excitation, a four-channel receiver, and an integrated wideband test set for biomedical noninvasive sensing. For high accuracy S parameter measurements, the presented VNA demonstrator has the highest integration level and the largest bandwidth, Figure 17 (c), [69] . Later on, in 2017, the same research group presented an improved 1-32 GHz broadband multioctave front end in SiGe technology. It consumes 217.8 mW for an area of 928 µm x 928 µm which is less than the previously used receiver in the integrated VNA, which consumes 351-360 mA for a surface of 3006 µm x 1870 µm [70, p. 32], [71]. Within the same year, in [72], a relevant contribution presents a single- chip reflectometer covering 0.01 to 26 GHz bandwidth in SiGe technology; the advantage is in the highly integrated resistive bridge coupler, Figure 17 (d). The core circuit, including two wideband receivers, has a surface area of 1.8 mm² and consumes 640 mW from a 3.3 V voltage supply. The two port VNA's

architecture is implemented and validated using two reflectometers by comparing the proposed VNA and commercial VNA DUT measurement results. Late in 2020, the same research group proposed a packaged two-port VNA based on the previously developed reflectometer, Figure 17 (e), [73].

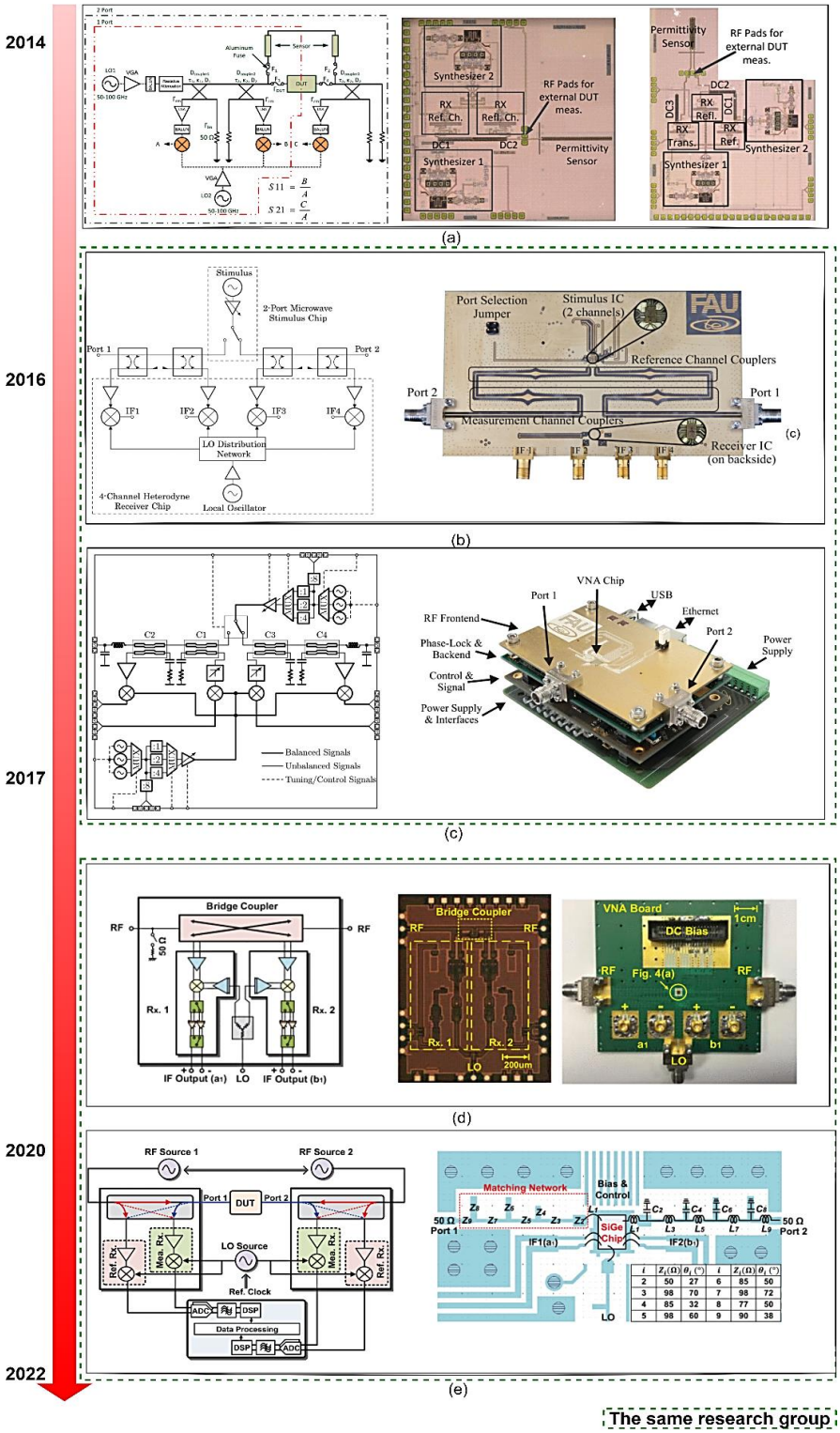


Figure 17 : Evolution of wideband separation-based network analyzer circuits with key contributions presenting the ICs block diagram and layout: (a) Left: Single- and dual-port coherent VNA chips 50–100 GHz, Right: Chip photographs of the single-port and dual-port VNAs for a silicon area of 3x3 and 4x3 mm, respectively. (b) Left: A two-port heterodyne VNA block diagram, Right: Chipset of the hybrid integrated VNA incorporating stimulus and receiver ICs and wideband couplers (length of 40.4 mm). (c) Right: Simplified block diagram of the fully integrated 4–32-GHz two-port VNA frontend IC, including the essential interfaces, Right: Physical implementation of octave bandwidth VNA (100 mm × 90 mm × 38 mm). (d) Left: 0.01-26 GHz single-chip reflectometer block diagram, Right: Chip microphotograph (1.5 x 1.2 mm²) and VNA board. (e) Left: Block diagram of two-port VNA. A single-RF source and a high-isolation SPDT can also be used instead of two RF sources. Right: Wideband matching network and layout of RF and IF transmission lines on the PCB near the SiGe chip.

1.3 THE THESIS' POSITIONING WITHIN THE EXISTING STATE OF THE ART

Overall, these studies have highlighted integrated VNA architectures covering a broadband frequency bandwidth. The interference method architecture offers a direct power measurement of multiple signals while deriving the phase and magnitude of the desired signal from the measured power values. This architecture is used due to its simple design and lower power consumption since it lacks active stages. However, the limited dynamic range of power detectors degrades the overall system dynamic range and is also difficult to integrate due to the passive elements and the wide bandwidth tradeoff.

On the other hand, the separation method architecture uses either direct conversion or heterodyne quadrature demodulators to resolve the phase and magnitude values of the device under test. Usually, narrowband IF filters are used to demodulate at low frequencies, providing higher precision measurements. This approach, unlike power detectors, filters out noise signals outside the filter's passband. Most commercial VNAs use this architecture, which will also be adopted in this thesis contribution.

However, the integration level of prior art remains limited since the proposed VNAs deliver the four IF output signals and further processing needs to be done off-chip. These are either sampled simultaneously by four external ADCs, followed by digital processing, or connected to a relatively expensive digital signal processor (DSP) that reads the digitized samples of the four channels [69]. Some performance limitations could occur as well due to the external IF interfaces. First, any coupling between the IF signal lines affects the measured results. Secondly, it requires relatively complex ADCs with high resolution to not limit the VNA dynamic range [73].

Looking ahead, **the remaining gap in the current state of the art for integrated VNAs is to fully integrate IF signal processing in the analog or RF domain to reduce the complexity and cost of the complex ADCs.** In the context of the outlined contributions, the primary goal of this thesis is to present a **fully integrated VNA** that includes IF signal post-processing, allowing for **direct magnitude and phase readout**. In view of all that has been mentioned so far, the main circuit specifications have been settled:

1. Integration of IF signal processing by **incorporating a demodulator to detect magnitude and phase proportional to the signals.**

2. Adoption of an **inductor-less architecture to cover a multioctave bandwidth** while maintaining a compact surface is also a challenging design.
3. **Competitive power consumption**, considering existing solutions for future inclusion in wearable or portable sensors.

1.4 SUMMARY

To summarize, this first chapter provides the necessary theoretical framework to explain the key concepts surrounding vector network analyzers, including the definition of scattering parameters, VNA architectures, uncertainty sources, and calibration techniques. The two main wideband VNA architectures have been studied: the six-port junction and the separation method. The first architecture has limited dynamic range and bandwidth response due to passive element limitations and relatively complex calibration. On the other hand, the second architecture offers a higher dynamic range and integrability, making it a valuable consideration for the adopted architecture in this thesis.

Based on the state of the art contributions, remaining issues need to be addressed when using a complex ADC to process the IF signals, and it has been proposed to integrate a demodulator to provide a direct readout of scattering parameters in terms of magnitude and phase.

Overall, this chapter provides a clear position regarding the literature and a good starting point for developing a highly integrated inductorless vector network analyzer covering a multioctave bandwidth. In the following chapter, the initial studies that led to a valid block diagram will be presented, along with an overview of the complete proposed circuit.

Chapter 2: INTEGRATED INDUCTORLESS BROADBAND VNA ARCHITECTURE

The intention behind this chapter is to explain the architecture choice. Notably, the first section develops a noise analysis for both the VNA receiver and demodulator based on commercialized circuits. Afterwards, the main system-level requirements and signal characteristics linked to VNA specifications are defined. Then, the second section introduces the complete circuit block diagram that complies with the conditions set out in the first section. Finally, the specifications of each sub-block are derived from the complete circuit study.

2.1 INTRODUCTION

When monitoring a commercial VNA, the scattering parameters seem to be simultaneously measured across all frequencies in a continuous sweep, but the results are actually produced from a sequence of measurements recorded at discrete frequencies. Effectively, the transmission and reflection measurements are made at a single frequency, allowing the DUT response to stabilize at the frequency point of interest. The VNA uses the output stimulus signal as a reference point and then measures the magnitude and phase of the reflected and received signals at a single frequency point. The frequency stimulus is then raised to the next frequency in the sweep, and the measurement is repeated. Then, the data from all the frequency points is assembled in post-processing to enable the measurement of many parameters.

Considering the VNA as a system, several key performance figures are involved. These include power levels at ports' outputs, input power ranges, frequency range, measurement speed, measurement accuracy, and stability over time (drift errors). Indeed, the output power range for the VNA specifies the minimum output, maximum output, and step size available for the signal provided by the VNA at the test port to the DUT.

In this work, the output power has been chosen to be controllable from -10 dBm to 0 dBm to ensure a measureable return signal from a lossy device under test (-70 dB to 0 dB). Another aspect is the input power level (i.e., the stimulus), which corresponds to the maximum output power level of the VNA stimulus. In this work, the reference frequency stimulus is not generated on chip. To do so, a laboratory generator with 0 dBm output power will be used. In a commercial implementation, this external generator could be replaced by a high frequency low cost commercial DDS[9] integrated circuit or a PLL. An example of this approach is found in [74], where the PLL delivers a maximum output power of 3 dBm up to 22.6 GHz. Another aspect concerns the frequency range, which specifies the minimum and maximum frequencies of the VNA. At first, this frequency range is limited by the implementation of the internal circuitry inside the VNA and the packaging solution. Since the

[9] A DDS reads waveform samples stored in memory using a phase accumulator at a fixed clock rate, giving it the ability to choose the samples to create an output waveform.

common mode is not propagated along the circuit, **the lower frequency is limited by the coupling capacitors to values around 200 MHz**.

The maximum frequency range is limited by the implementation choice. Indeed, to reduce package costs, a commercially available quad flat pack non lead (QFN) package has been selected to integrate the circuit developed in this Ph.D. thesis, as illustrated in Figure 18 (a) and (b). Wire bonding has been used as an interconnection choice, limiting the upper frequency below 20 GHz when the required input and output return losses are around -10 dB, Figure 18 (c). Taking into account a design margin and package limitations, **the objective is to achieve a bandwidth of 30 GHz on the core circuit**. In addition, challenges also arise in balancing the total power consumption and overall size of the system to meet wearable sensor requirements [75]. Table 2 summarizes the first specifications chosen for this work.

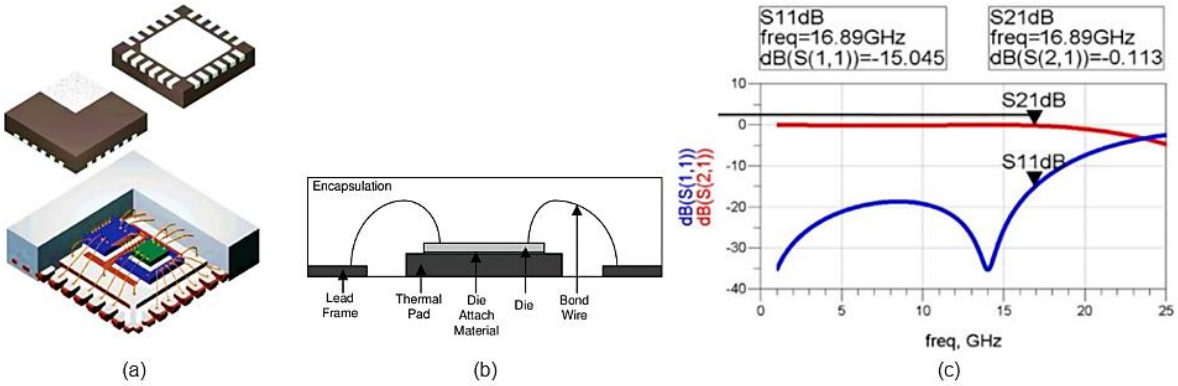


Figure 18 : (a) QFN package containing an IC (b) : The cross section of a typical QFN package and (c) input and output return loss Vs frequency [76]

Afterwards, the next section addresses the main modules of a VNA with a preliminary architecture. Then, through the figures of merit of a VNA combined with two system studies, the final design choice of the circuits involved is presented.

Characteristics	Min	Typ	max	unit	Comments
Output power	-10	0	0	dBm	
Input power	-4	-3	0	dBm	External for this work
Frequency range	0.2	20	30	GHz	$f_{min}: internal\ limitation$ $f_{max}: packaged\ limited$
Supply Voltage	0.9	1	1.2	V	GF45SOI technology
Measurement capability		S_{11}& S_{21}		dB	Unidirectional
Size		<46.5 x 46.5		mm²	The mean value of smart watches dimensions

Table 2: VNA System requirements

2.2 VNA SYSTEM STUDY

As illustrated in Figure 19 (a), the proposed miniaturized VNA is based on three modules. First, the source module that generates the stimulus. Its tuning range defines the VNA frequency range. The main constraint on the source module is its frequency stability. This module will be "off-chip" in this PhD work but could be easily integrated into a commercial version of the system.

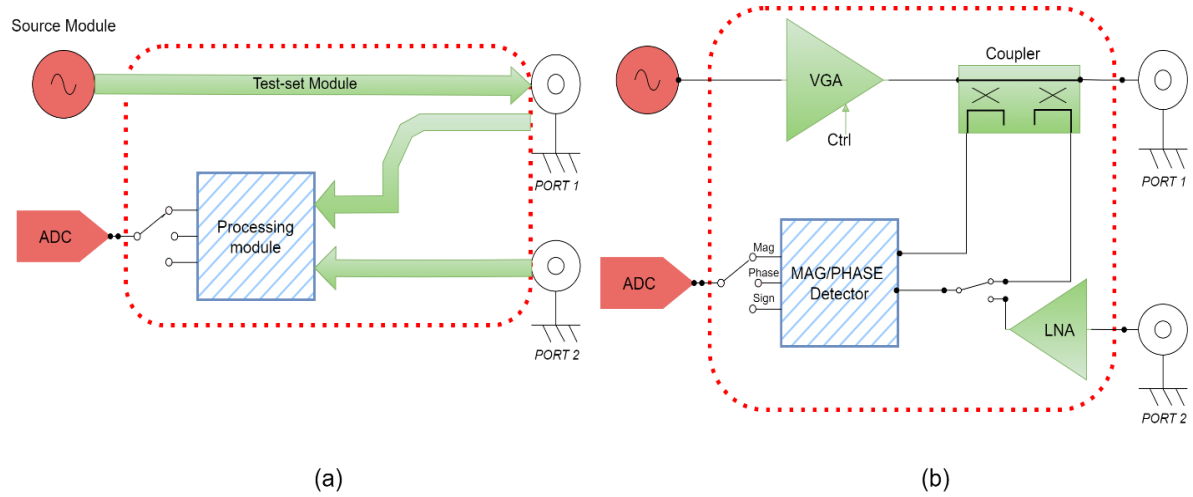


Figure 19 : (a) VNA modules, (b) Initial bloc diagram, dashed contour present the IC scope

Secondly, there is a test-set module that directs an RF signal from the source module to the device under test (DUT) and samples the transmitted and reflected waveforms. The test-set module performs preliminary functions such as amplification, attenuation and intermediate frequency switching. Finally, the processing module analyzes the RF signal in terms of phase and magnitude. This module presents the analog demodulation part of the system, in which the incident, reflected and transmitted signals will be processed and converted to a DC signal, which corresponds to the phase and amplitude variation in reflection and transmission modes. On the other hand, from an architecture viewpoint, Figure 19 (b) shows the initial architecture based on:

1. A **variable gain amplifier** to tune the first port's output power.
2. A **directional coupler** to first drive the incident wave through the device under test and secondly to couple the incident power to be used as a reference for

the detector, and thirdly to derive the reflection wave generated by the DUT mismatch.

3. A **wideband low noise amplifier** to amplify the weak signal that goes through the DUT
4. Finally, the incident, reflected and transferred waves will be processed by the **demodulator**.

It is worth recalling this work position (1.3) with respect to the state of the art exposed in the previous chapter. Specifically, the integration of an analog demodulator that will ease the digital processing of portable devices. In other words, when the sensor is used for data collection, the linearity and resolution of the ADC are critical, as the output signal amplitudes are quite low. To meet these high requirements, large and complex ADCs are mandatory [77]. However, with this internal demodulator, as will be shown further, the signal acquisition, conditioning and detection do not require high quality ADCs or improved algorithms to extract the scattering parameters [78].

In the following, a preliminary analysis of the building blocks required for the VNA has been conducted in two parts to define its specifications. As illustrated in Figure 20, the data sheets of a commercial VNA without the demodulator have been examined in the first part of the analysis (2.2.1), and then the specifications of an analog commercial demodulator (2.2.2) have been identified in the second part of the analysis.

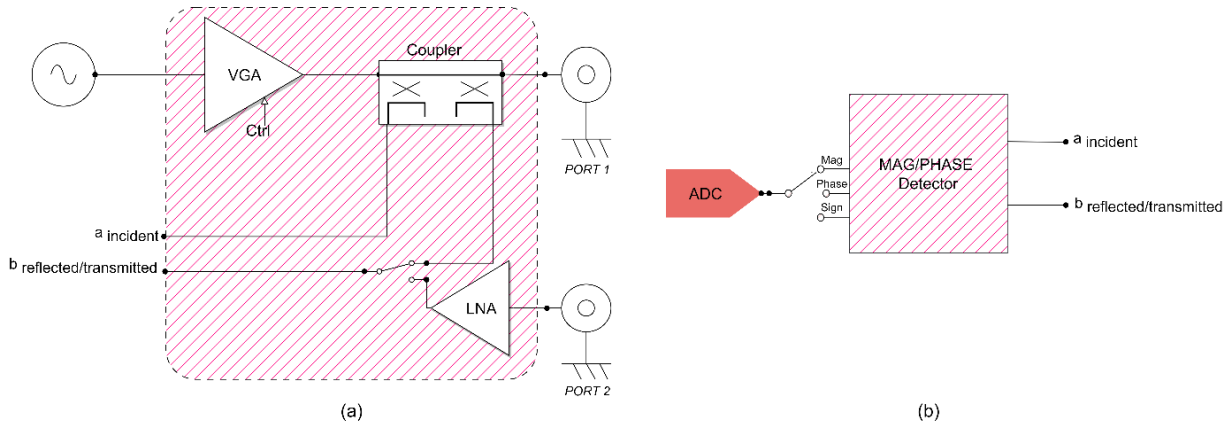


Figure 20 : (a) First study on the Initial VNA System without demodulator (b) Second study regarding the demodulator

2.2.1 *VNA SYSTEM WITHOUT THE DEMODULATOR*

In this section, considering the VNA system without the demodulator, Figure 20 (a). As illustrated in Figure 21, there are two common definitions for “dynamic range” (DR). First, the system DR is defined as the difference between the power available at the test port and the measured noise floor ($P_{nom} - P_{min}$). Secondly, the receiver DR is defined as the difference between the typical test ports’ 0.1 dB compression point minus the typical noise floor ($P_{comp} - P_{min}$).

Where:

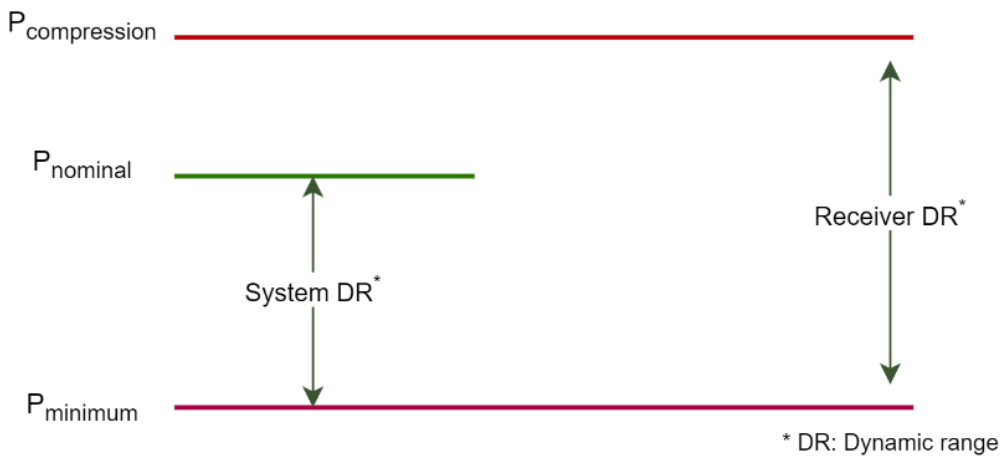


Figure 21 : VNA dynamic ranges

- P_{min} gives the minimum input power level the system can measure, (receiver sensitivity), set by the receiver noise floor.
- P_{nom} indicates the nominal power available at the test port from the network analyzer source.
- P_{comp} refers to the highest input power level that the system could measure, which is related to the receiver’s compression specification.

To avoid confusion in the following studies, **two parameters need to be distinguished**: the intermediate frequency bandwidth (**IFBW**) and the **intermediate frequency**. The IFBW sets the integration band of the noise present at the input of the demodulator, and the intermediate frequency value where post-processing of the IF signals will be performed. In fact, the choice of the IF bandwidth (IFBW) defines the signal-to-noise ratio (SNR) at the input of the demodulator. Conversely, the selection of the IF frequency is determined by other

criteria. Firstly, the IF frequency must be higher than the bandwidth. Secondly, the choice of the intermediate frequency (IF) depends on factors such as interference and selectivity. Based on the aforementioned studies, both parameters will be specified.

The following study explores the correlation between operation frequency bandwidth and dynamic range. Within this context, Figure 22 shows the system DR at the test port of the Keysight VNA "N5242B" [79]. The DR ranges between 97 and 132 dB, while the total average (rms) noise power calculated at the mean value of the magnitude trace ranges between -114 and -80 dBm for **10 HZ IF bandwidth**. On the other hand, when using a **30 GHz bandwidth**, as illustrated in Figure 23, the noise power is about $10log\left(\frac{30\ GHZ}{10\ Hz}\right) = 94.7\ dB$ higher than the previous VNA DR with a 10 Hz bandwidth. As a result, in this scenario, the predicted dynamic range shrinks considerably as the noise floor rises.

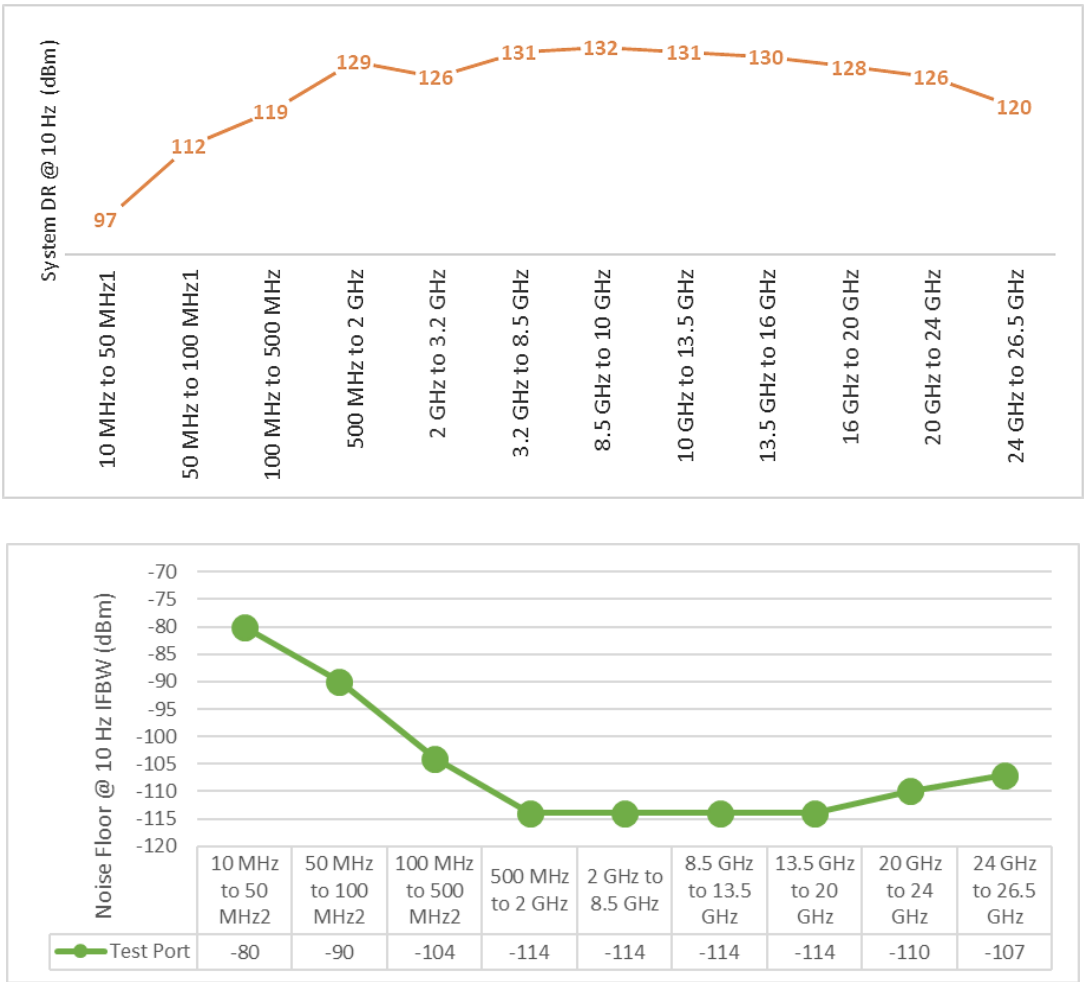


Figure 22 :Top: VNA (N5242B) dynamic range (table 7 in [79]***), Bottom: noise floor from 10 MHz to 26.5 GHz (no averaging applied to data)***

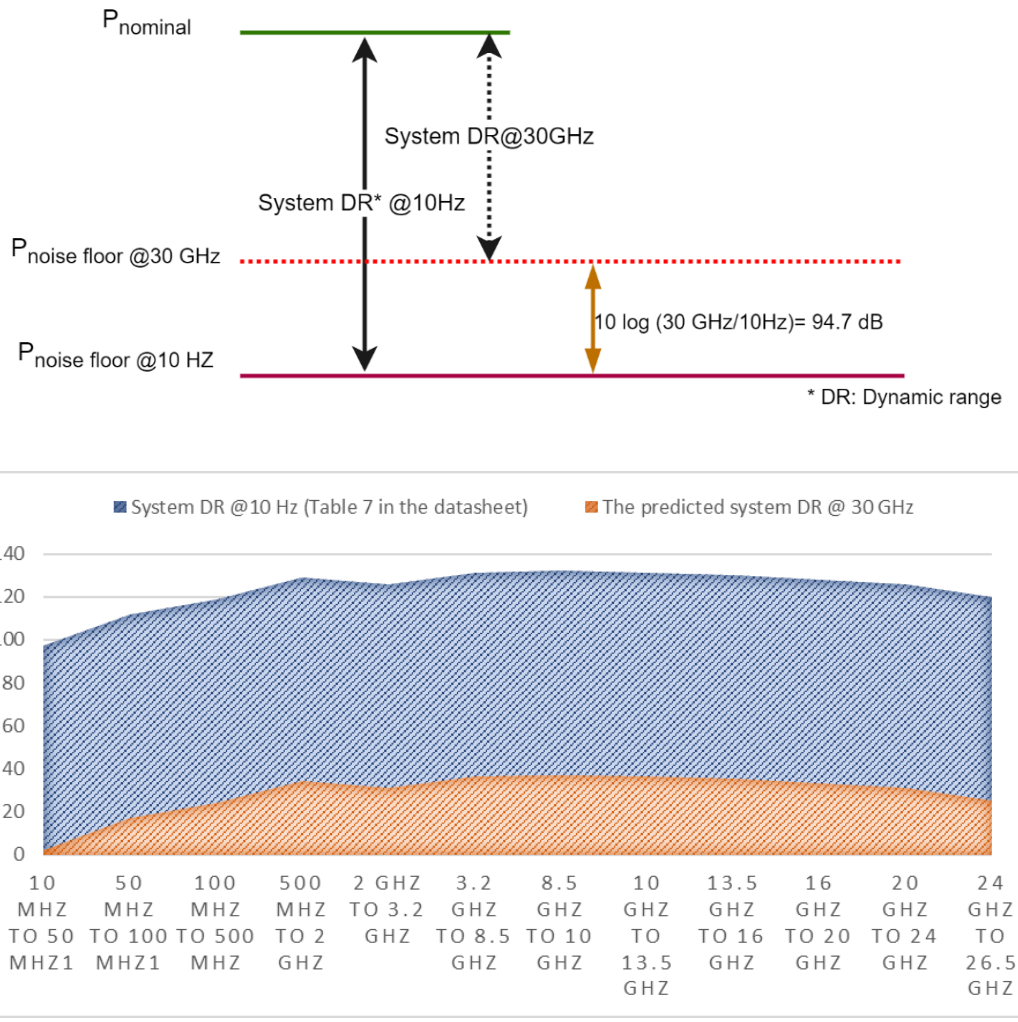


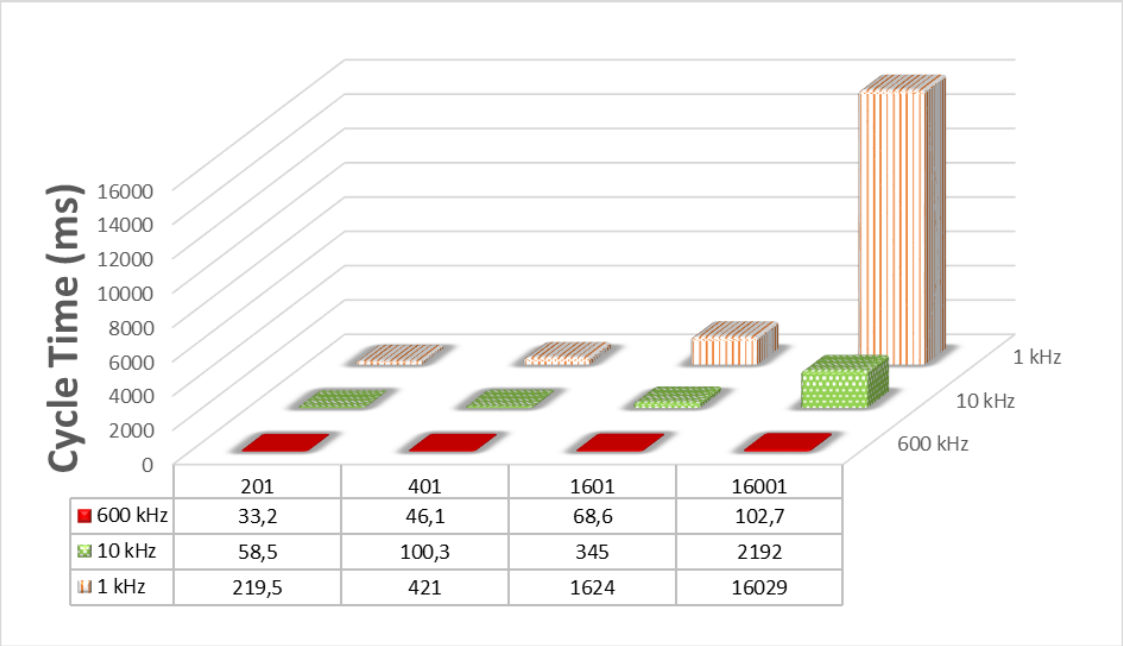
Figure 23 : System dynamic range deterioration (@10 Hz IFBW Vs 30 GHz BW), Comparison between VNA DR @10 Hz Vs 30 GHz bandwidth

Furthermore, it is important to consider the time of measurement. Based on the frequency range and number of data points settled, the VNA system calculates each of these points, then transfers data to the processing module within a given time called “Cycle Time”.

Referring to the same VNA (Ref: N5242B), Figure 24 presents the “Cycle Time” in milliseconds, which is the time required for a frequency sweep and retrace, based on the user selectable IFBW. In this VNA, the selectable IFBWs are 600 KHz, 10 KHz and 1 KHz for a full span measurement completion[10] for uncorrected and corrected traces (after calibration procedure). By analyzing the figure, it can be noticed that when the IFBW is narrower with a high resolution (large number of points), the settling time is longer.

[10] A stimulus frequency sweep from 10 MHz to 26.5 GHz

Naturally, there is a tradeoff between IFBW, measurement time and system dynamic range since widening the IF bandwidth decreases measurement time per point, but also decreases the dynamic range of the measurement. To affirm that, as expressed in (15), for 1 KHz, 10 KHz and 600 KHz, the dynamic range will be reduced by 20 dB, 30 dB and 47.7 dB, respectively.



	201	401	1601	16001
600 kHz	33,2	46,1	68,6	102,7
10 kHz	58,5	100,3	345	2192
1 kHz	219,5	421	1624	16029

Figure 24 : Cycle Time (ms) for Full-Span measurement Completion Vs IF Bandwidth for different Number of points [Table 108 in [79]***]***

$$DR_{System@10Hz} = DR_{System@IFBW} + 10\log(\frac{IFBW_{[1\ KHz,10\ KHz,600\ KHz)}}{10\ Hz}) \qquad (15)$$

Another parameter to enhance the DR is averaging. Hence, for a given averaging factor, sweep-to-sweep averaging could be used to reduce the noise floor (primarily random noise). Specifically, the averaging operates on each point of the data on an exponential average of consecutive sweeps weighted by the user-defined averaging factor; meanwhile, the calibration and the test bench must remain unchanged, which is in reality not the case, which is the reason why drift errors occur more while using this approach compared to the IFBW choice. Indeed, the IFBW reduction has an advantage over averaging since it reliably filters out unwanted responses, including spurious odd harmonics and higher-frequency spectral noise.

Overall, in this study, various factors that affect the VNA's performance have been examined, including system dynamic range, noise floor, and measurement time per point. It

might be concluded that it is necessary to operate in a narrow intermediate frequency bandwidth to maintain good measurement dynamics with a lower noise level.

2.2.2 *VNA DEMODULATOR*

The focus of this section is on the examination of the demodulator only to extract amplitude and phase, as shown in Figure 20 (b). The demodulator used in this study is based on logarithmic amplifiers for the extraction of amplitude and phase.

Logarithmic amplifiers are widely used to extract the signal amplitude, namely RSSI[11] detectors. This architecture has been selected for the proposed demodulator due to its high sensitivity and wide input dynamic range [80]. Moreover, with a specific configuration of these logarithmic amplifiers, the phase could be extracted too.

In this study, the objective is to prove that the baseline sensitivity of these detectors is limited by their operating frequency bandwidth. The starting point is the mean value of the commercialized logarithmic amplifier's input referred Voltage Noise Spectral Density (VNSD), which is equal to 1.68 nV/$\sqrt{Hz}$ when driven from a 50 Ω terminated source [81].

To begin, let's consider this total VNSD value of 1.68 nV/ $\sqrt{Hz}$ and an effective noise bandwidth of 800 MHz associated to [81]. The integrated RTI (total Input referred) noise over this bandwidth is 47.5 µV rms (that is, $V_{RMS}(\boldsymbol{V}) = VNSD(\frac{\boldsymbol{V}}{\boldsymbol{HZ}})\sqrt{BW\ (\boldsymbol{HZ})}$). Expressed in terms of noise power, referred to 50 Ω, it is expressed as $P_{noise}(dBm) = 10\log\ (\frac{V_{RMS}(mV)^2}{50(\Omega)}) = -73.46$ dBm .

The signal to noise ratio at the demodulator input is defined as (16) and equal to 13.43 dB, considering P_{signal} of -60 dBm corresponds to the lowest power in the demodulator's dynamic range.

$$\mathbf{SNR_{dB,BW=800MHz}} = 10\log\left(\frac{Signal(mW)}{Noise(mW)}\right) = P_{signal}(dBm) - P_{noise}(dBm) \quad (16)$$

= -60 dBm-(-73.46) dBm = 13.46 dB

This analysis will be transposed to a broadband demodulator with a 30 GHz frequency bandwidth. Therefore, the integrated noise RMS value is equal to 0.29 mV, which in terms of

[11] Received Signal Strength Indicators (RSSI)

noise power is equal to -57.74 dBm. Below this noise floor, the signal power level detection will be inaccurate, since the SNR will be equal to -2.26 dB for -60 dBm of signal power. This negative SNR means that the signal power is lower than the noise power, so it does not guarantee that the detector will be able to demodulate the signal.

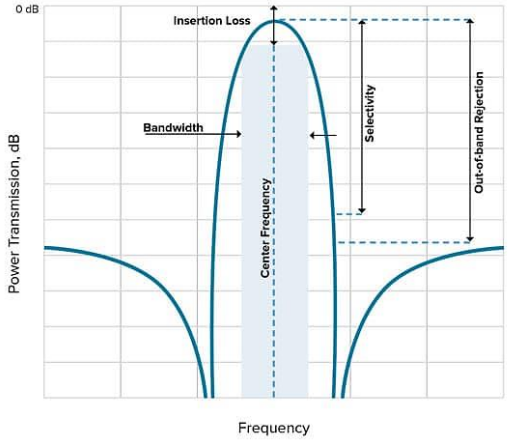
$$\mathbf{SNR_{dB,BW=30GHz}} = -60\ dBm - (-57.74)\ dBm = -2.26\ \text{dB} \ll SNR_{dB,BW=800\text{MHz}} \quad (17)$$

This theoretical study has identified a limitation in terms of the detector measurement floor due to the operation frequency bandwidth. Hence, both studies converge on the following insight for the proposed block diagram: Demodulating in a narrow frequency bandwidth to reduce noise at the demodulator input and also boost the demodulator sensitivity.

2.2.3 *SYSTEM CONSIDERATIONS*

To further extend the demodulator's and receiver's dynamic range, an intermediate frequency with a given IF bandwidth is introduced to ensure that the demodulating process occurs accurately at a given intermediate frequency while spanning the source frequency from 200 MHz to 30 GHz. For this reason, **a heterodyne architecture** is selected in this Ph.D. thesis.

The default **IF frequency** choice is set to **455 KHz** for several reasons. This frequency was chosen because it is in a part of the radio spectrum that is relatively free of interference and is also a standard frequency used in many commercial communication systems. In addition, it is a frequency that is easy to filter using high quality off-chip ceramic filters. They have a narrow bandwidth and a high level of selectivity, as depicted in Figure 25 [82]. In the adopted architecture (Figure 26), there is an external filtering option to filter the noise at the input of the demodulator.



Centre frequency	**455KHZ±1.5KHz**
-6dB bandwidth	10 KHz
-40 dB bandwidth	20 KHz
Stopband attenuation (min) at ±100 KHz	27 dB
Quality factor	303

Figure 25 : Typical response and specification parameters of a ceramic IF filter [82]

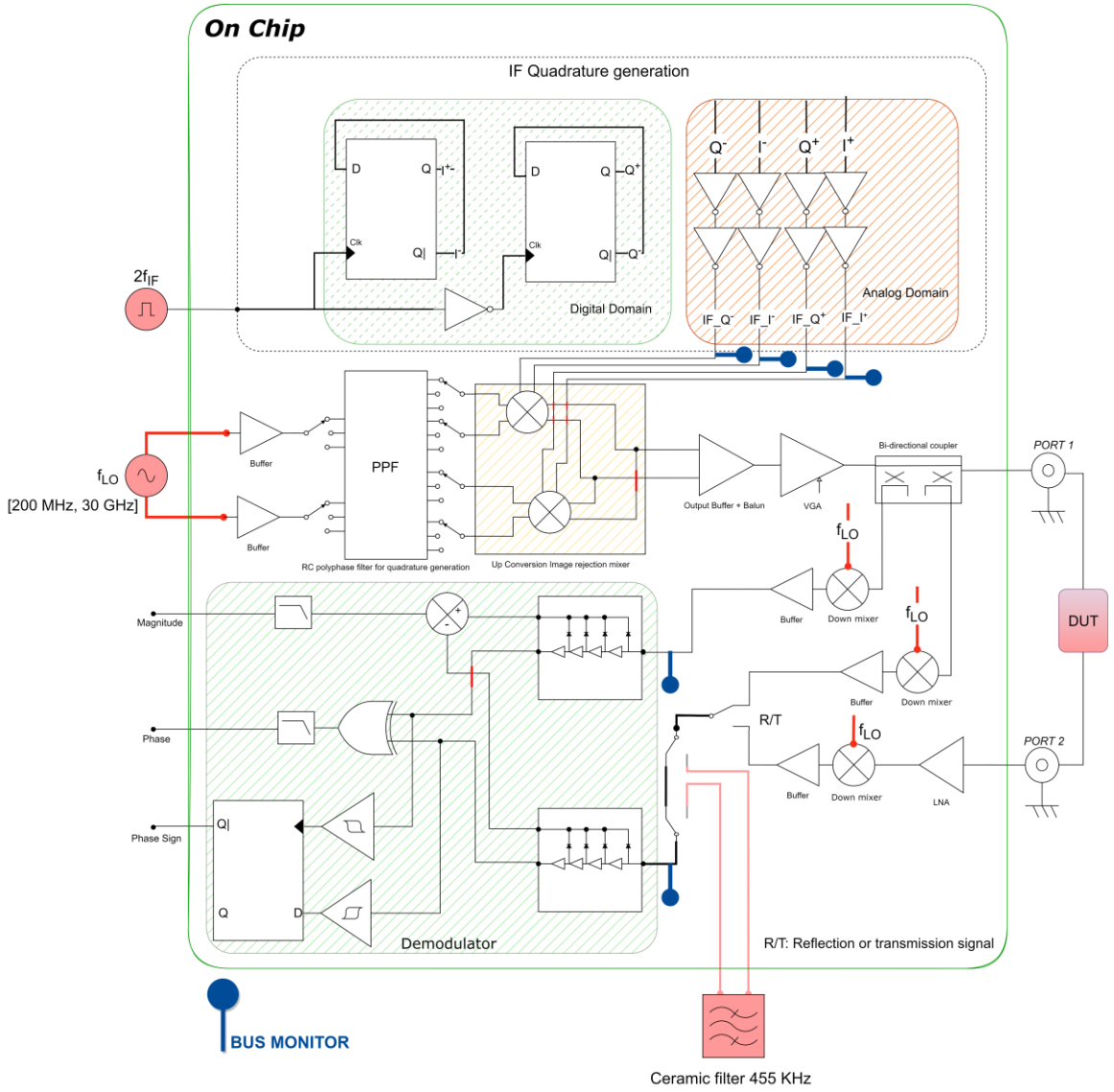


Figure 26 : The adopted block diagram, it includes only the key blocks, impedance matching circuitry and biasing circuitry (current to voltage converters, DAC's, SPI control), buffers, coupling capacitors and Bus monitor circuitry are not included to simplify the diagram's complexity.

Back to the proposed heterodyne architecture, the external LO signal introduced from the source $f_{LO} \in [200MHz, 30GHz]$ is up-mixed first with an IF frequency f_{IF}, the resulting bandwidth around the RF frequency $f_{RF} = f_{LO} \pm f_{IF}$ is down mixed with f_{LO} to down convert the signal to the IF frequency. From this point, an up conversion mixer is introduced in the transmitter channel, and down mixers are introduced in the incident, reflection and transmission channels.

As illustrated in Figure 27, a further issue arises from the resulting tones at the first up conversion $f_{LO} \pm f_{IF}$. Effectively, before going through the down mixer, the image frequency $f_{LO} - f_{IF}$ should be rejected to prevent aliasing. Indeed, image rejection is an important

consideration since it determines the ability to reject image frequencies that can cause significant interference at the demodulator input thus degrading the performance of the VNA system.

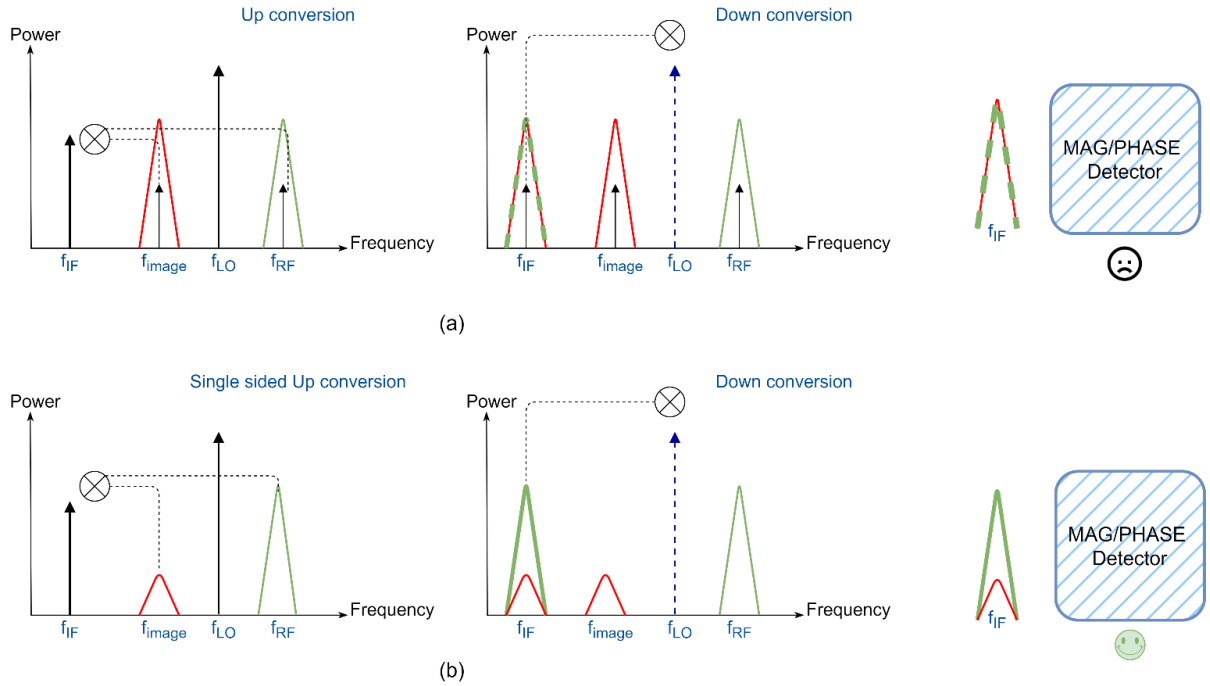


Figure 27 : Frequency domain interpretation of the wide-band mixer (a) without IF image rejection mixer (b) with IF image rejection mixer

There are several ways to reject image frequency including filters and image rejection mixers (IMR mixers). Considering that the LO frequency will sweep over a band of frequencies, using a filter to attenuate the image frequencies is a complex solution in terms of design and control. For this reason, the optimal solution to cancel the image frequency is a double balanced image rejection up conversion mixer.

To achieve this rejection, quadrature differential LO and IF signal generation is required to cancel out the unwanted sideband.

- For the LO input signal quadrature, the RC polyphase filter (PPF) fulfills the need to provide a broadband quadrature. Using a PPF to generate quadrature[12] signals has several advantages such as a wide bandwidth, a low area and a low passband ripple, which can help minimize signal distortion.

[12] Quadrature signals are two sinusoidal signals that are 90 degrees out of phase with each other.

- For the IF quadrature generation, a digital quadrature generator based on two D flip flop is integrated in the proposed IC with an external clock controlling the IF quadrature generation. This solution offers quadrature generation by construction with a very small associated area and low power consumption. The limitation is the maximum frequency achievable by a D flip flop. In this work, since the IF frequency is low (455 KHz), this solution is perfectly adapted. However, the system can work with higher IF frequencies as long as the bandwidth of the D flip-flops permits it. This can be beneficial, for instance, to minimize the flicker noise contribution by elevating the IF frequency between 1 and 10 MHz.

Once the up conversion with image rejection is done, a variable gain amplifier tunes the emitted power from port 1, Figure 26. For the reflection mode, a bidirectional coupler allows the recovery of a part of the incident signal and a reflected signal. Both signals are in the upper sideband $f_{RF} = f_{LO} + f_{IF}$. Mixed with the LO frequency, the signals are down mixed to the intermediate frequency f_{IF} .

In Figure 26, the signal originating from port 1 travels through the device under test (DUT) to the second port. The transmitted signal is then amplified by a wideband low noise amplifier. At that stage, three signals (incident, reflected and transmitted) are down mixed to the intermediate frequency. The incident signal is directly linked to the demodulator, however the transmitted and reflected signals are respectively switched to measure first the S_{11} then the S_{21}.

This demodulator is based on two identical logarithmic amplifiers delivering two signals: a logarithmic voltage proportional to the amplitude of the input signal and a square saturated signal. Now, considering the incident signal and the reflected or transmitted signal, the two logarithmic amplifiers provide four signals; both logarithmic output voltages are subtracted in current mode, then filtered to provide a DC signal proportional to the incident and transmitted or reflected ratios. Similarly, the two saturated signals are introduced in a XOR[13], then filtered to provide a DC signal proportional to the absolute value of the phase difference between the incident and reflected or transmitted signals.

[13] XOR (exclusive or) is a logical operator whose output is true when either of two inputs are true but not both.

The detector provides the same DC value for the two opposite phase signs, resulting in phase ambiguity. To overcome this, two solutions have been investigated:

- The first solution is based on a phase shifter. By measuring the original phase and then the shifted phase, the actual phase sign could be determined [83]. This first solution is accurate, however, it is complex in terms of time of measurement and calibration since it creates an imbalance between the incident and the reflected/transmitted channels.
- The second and **adopted solution**[14] is a one-time measurement based on two hysteresis comparators that compare the first zero crossing of the two saturated signals. The D flip flop provides two states, providing the sign of the absolute phase difference.

A last point to mention is that the IC is conceived to have outputs to read the IF signals, inputs to characterize the demodulator alone, and readings of the IF quadrature generator outputs, as illustrated with “Bus Monitor spots “ in Figure 26.

[14] This solution is internally patented.

2.2.4 VNA BUDGET STUDY

As discussed previously and depicted in Figure 26, to generate quadrature signals for the RF path, a PPF has been used. However, the difficulty is to provide a 90 degree difference and a low magnitude imbalance between the two generated signals (I and Q) over the 30 GHz bandwidth. This is the reason why three controlled 4-stage RC polyphase networks are adopted so that for each measure, only one PPF is enabled to cover one of the three measuring bands: [200 MHz, 1 GHz], [1 GHz, 7 GHz], and [7 GHz, 30 GHz]. As a rule of thumb, the loss due to PPF is usually estimated to be 3 dB/stage. Therefore, a 12 dB loss for each PPF is estimated, with additional losses related to the input buffer's gain roll-off beyond 20 GHz. Thus, based on the proposed block diagram, it may be stated that the losses of the polyphase filters are at best compensated by the mixer and the variable gain amplifier, respectively. In the worst case at 30 GHz the simulated losses of the polyphase and the input buffer reach 24 dB. These losses combined with the various sub-blocks of the transmission chain estimated gain (up conversion mixer 8 dB and bi-directional coupler -3 dB) yield a minimum required gain of 23 dB for the VGA and hence a power output of 0 dBm. This initial study is summarized in the signal level breakdown of the transmitter in Figure 28.

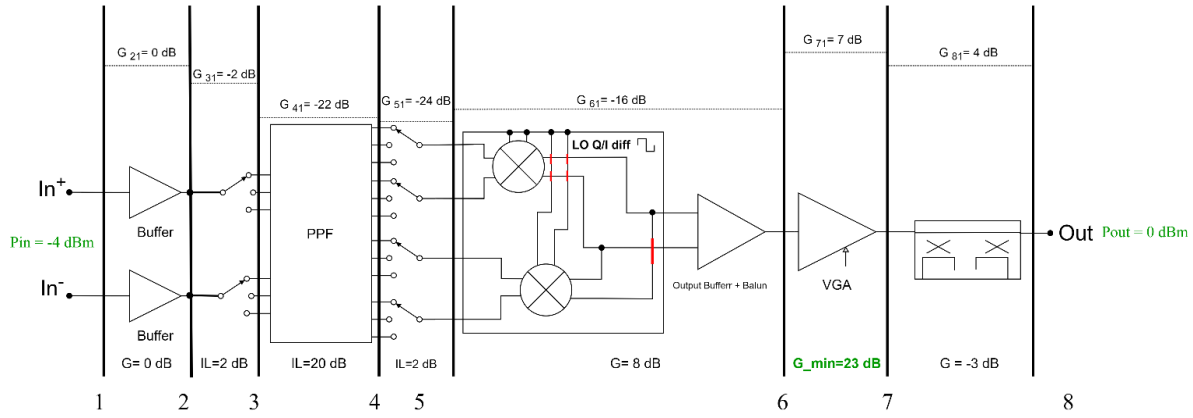


Figure 28 : Initial study of Power breakdown in the transmitter at 30 GHz

Concerning the transmission mode, as illustrated in Figure 29, with 70 dB DUT insertion losses, a wideband inductorless low noise amplifier with 20 dB gain is required to meet the demodulator's dynamic range because the passive mixer combined with an output buffer provides no gain at best.

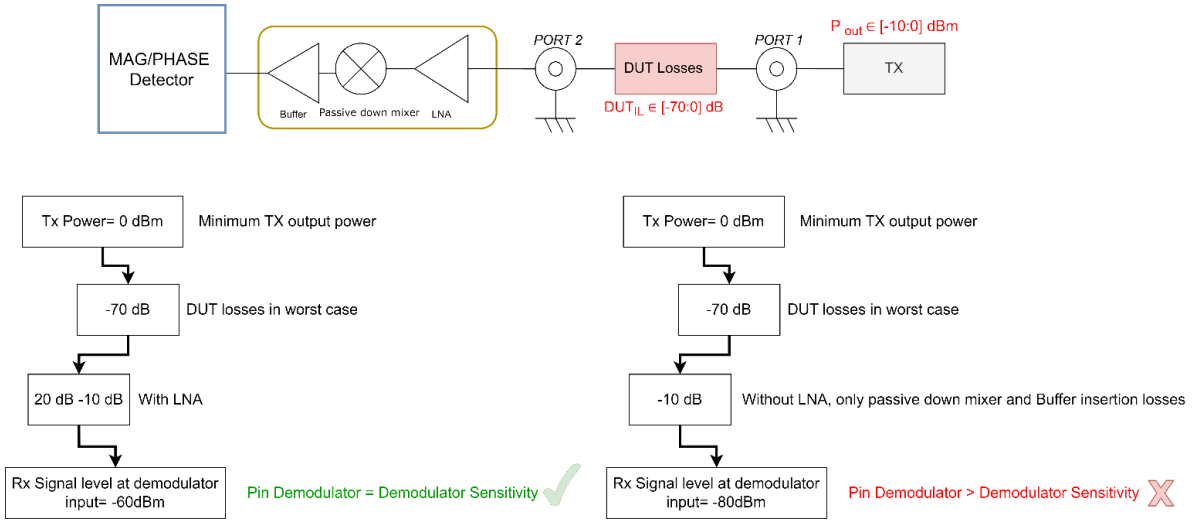


Figure 29 : Transmission path receiver study in worth case (maximum DUT losses that could be measured ideally)

Another scenario is illustrated in Figure 30, where the DUT is a matched load; in this case, the reflected signal is equal to the coupler isolation and the receiver's gain in the worst case. Hence, a minimum power of -60 dBm sets the sensitivity of the demodulator to accurately extract the S11 parameter.

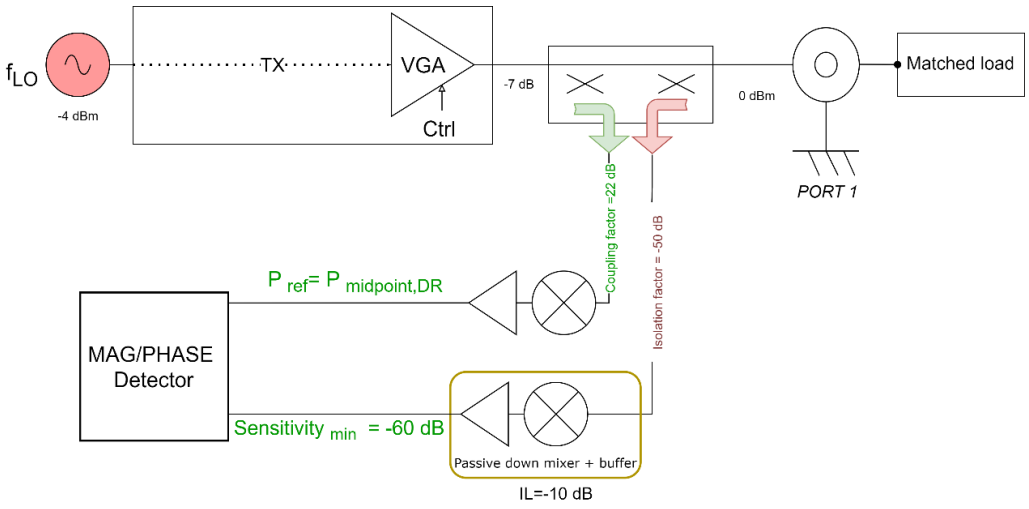


Figure 30 : Incident and reflection path at worst case (matched load @30 GHz)

Now, considering the incident signal path, the demodulator reference signal is largely beyond the demodulator's sensitivity. However, this power should be ideally equal to the optimal reference power to not saturate the available dynamic range, which is ideally the midpoint of its dynamic range. Taking into account the power breakdown in Figure 29 and the

“Ref/RX” gain in the worst case, a coupling factor of 22 dB is required, which is the fraction of the incident power that is delivered to the coupled port of the directional coupler.

This primarily budget study has allowed us to estimate the minimum required gain for each sub-block to meet the demodulator’s dynamic range. As mentioned in the demodulator study, the input noise is important since it sets the minimum detected signal, which is the lower band of the demodulator dynamic range. The noise figure of the TX is not considered since the Signal to Noise ratio is high, even if the noise figure is high (the TX begins with a passive circuit PPF). Otherwise, the three receiver’s (incident, reflection and transmission) noise figure are considered, as is the input noise voltage of the demodulator. In the adopted circuit, the IF bandwidth is 455 KHz by default and can be reduced to the external ceramic filter bandwidth, which is 10 KHz around the intermediate frequency.

Overall, the main initial specifications of directional, gain and mag/phase detection circuitry are summarized in Table 3. Otherwise, the impact of the image rejection rate on accuracy of the measurement was not assessed initially.

Circuitry	Parameter	Typ	Units	Conditions/comments
Directional Circuitry	Coupling factor	22	dB	Both parameters set the directivity value, which is the minimum VNA detectable signal in reflection mode.
	Isolation	50		
Gain Circuitry	LNA Gain	20	dB	
	VGA G_{min}	23		
Magnitude and Phase detection Circuitry	Sensitivity	>-60	dBm	The S21 DR is higher due to the additional LNA gain and could be improved with an active boosting pre-amplifier at the port 2 input.

Table 3: Initial circuitry specifications

2.3 CONCLUSION

So far, the complete VNA system structure has been presented. The starting point was identifying the main drivers that impact the VNA figure of merit, namely the dynamic range of the system, the dynamic range of the receiver and the noise floor. Based on two circuit datasheets, two studies were performed to establish that the bandwidth degrades the measurement noise floor and subsequently, the DR of the system. Actually, the dynamic range of VNA systems depends on the noise floor and thereby on the bandwidth. Mainly, commercially available VNAs have a very narrow band at 10 Hz, but as has been pointed out, this IF bandwidth could be switched to a higher bandwidth to shorten the measurement cycle time. All in all, there is a trade-off between IF bandwidth range, noise floor, and dynamic range.

Meanwhile, the second review revealed that the input signal-to-noise ratio of the demodulator requires a narrow band to detect magnitude and phase accurately. From these initial findings, the implemented circuit is based on a heterodyne receiver where an IF frequency is provided internally to be initially up-converted in the transmitter and then down-mixed through the three receivers (incident, reflected and transmit channels) to process at the fixed IF frequency of 455 kHz. Such an IF frequency offers a good compromise to meet the dynamic range requirements of the VNA and also provides an external low-cost ceramic filter to improve sensitivity if required. And finally, sub-blocks specifications are covered to meet the dynamic range of the demodulator.

Thereafter, within the next chapter, the designs of the integrated sub-blocks are covered, sorted into gain, image rejection, directivity and demodulation features. Furthermore, measurements of three blocks submitted at the end of the first year thesis are included. These are the coupler, the wideband LNA and the polyphase filter to generate the LO quadrature.

Chapter 3: BROADBAND VNA BUILDING BLOCKS IMPLEMENTATION

In this chapter, the overall assembly of the proposed VNA system is reviewed. The proposed VNA is comprised of five key components, allowing accurate magnitude and phase measurement of transmission and reflection parameters of a device under test (DUT). These components include a directional coupler, image rejection circuits, amplification, down conversion receivers, and amplitude and phase detectors.

Measurements of three building blocks in a standalone configuration have been performed. These include the coupler, the wideband inductorless low noise amplifier, and the polyphase filter. Each measurement is displayed in the corresponding section and used to improve the second version of the complete VNA integrated circuit.

3.1 INTRODUCTION

3.1.1 INTEGRATED VNA CIRCUIT ARCHITECTURE

Figure 31 presents the complete VNA system, comprising five main blocks that will be discussed in each section. Firstly, the design of a directional coupler circuit was addressed. This circuit involves signal transmission through the directional coupler to port 1 and extracting the incident and reflected signals as well.

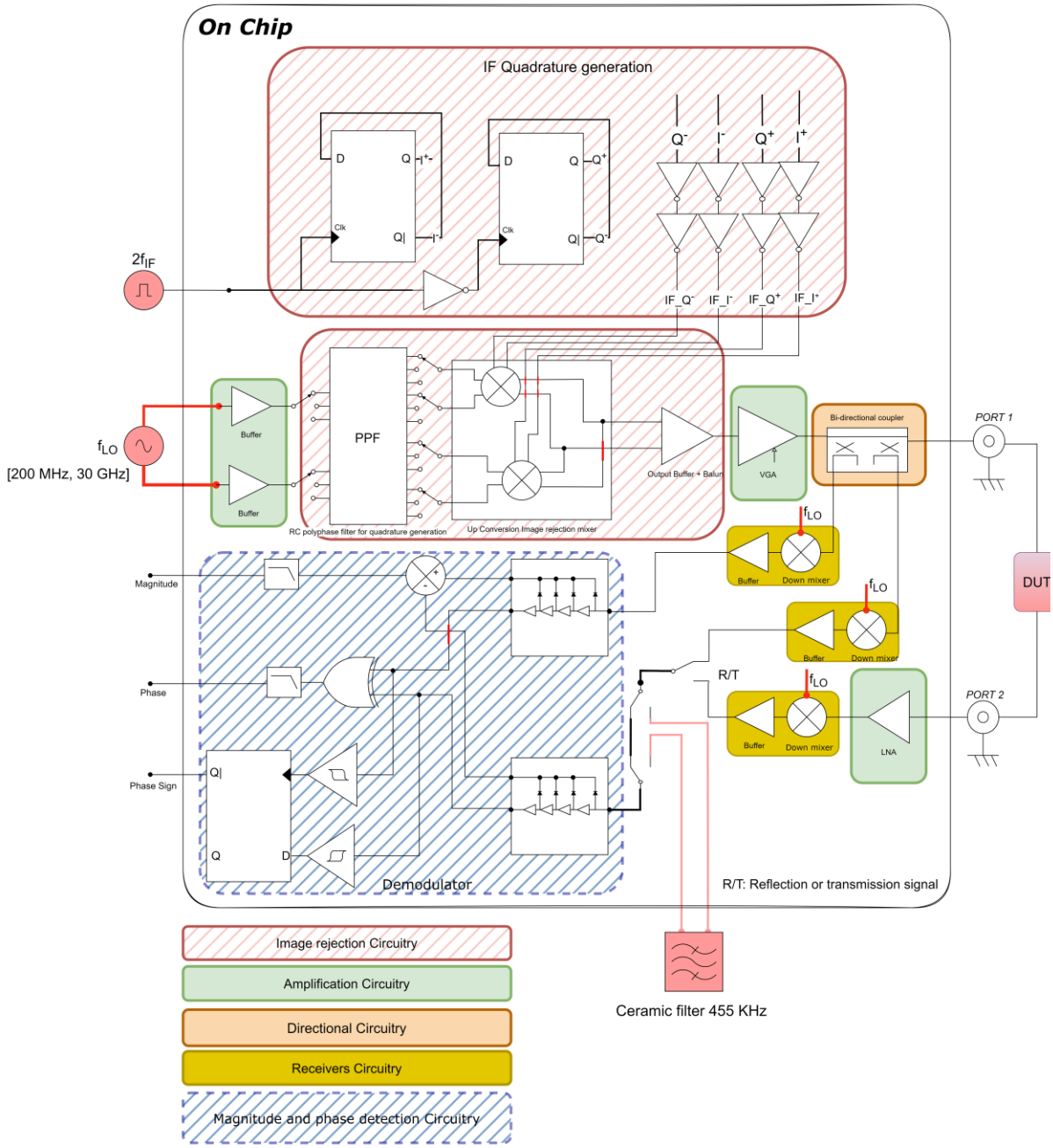


Figure 31 : Block Diagram of VNA Circuitry

Secondly, the image rejection circuitry used to reject the image frequency is presented. It incorporates wideband LO quadrature generation ranging from 200 MHz to 30 GHz and the generation of an IF quadrature at 455 KHz. Both LO and IF quadrature signals are injected into a double-balanced up-conversion mixer to filter out the image frequency.

Thirdly, amplification circuitry is introduced. It includes a variable gain amplifier to tune the emitted power at the first port from -10 dBm to 0 dBm and a wideband low noise amplifier at the transmission path receiver's input. It increases the strength of the signal being received at the second port.

Fourthly, the receiver's circuitry will be addressed with regards to the reference, reflection, and transmission channels. These receivers play a key role in the process of signal reception, since the RF signal resulting from the up conversion will be mixed with the LO input signal. As a result, three IF signals are produced at the receiver's output, including the incident signal, the reflected signal, and the transmitted signal. The incident signal provides the reference for the magnitude and phase demodulator. The transmitted and reflected signals are measured one after another to be injected into the demodulator input, since the same demodulator is used to measure the S_{11} or S_{21} parameters. Another switch controls the use of an external selective filter to increase the sensitivity at the demodulator input.

Finally, the magnitude and phase detection circuitry will be detailed. It includes limiting amplifiers, two logarithmic amplifiers, digital blocks to resolve phase ambiguity, and external filters to extract the DC value of both amplitude and phase.

As depicted in Figure 32, during the thesis' first year, the characterization of three building blocks in standalone configuration was performed. It includes the wideband resistive coupler, the wideband inductorless low noise amplifier, and the polyphase filter for LO quadrature generation. The coupler has been designed to split the signal into two separate paths, one for transmission and one for reflection parameter extraction. The wideband inductorless low noise amplifier is a key component of the VNA as it amplifies the weak signal that is being measured at the transmission receiver (port 2). Finally, the polyphase filter provides a wideband LO quadrature, allowing image rejection at the up conversion mixer output. The measurement results are presented in the corresponding section and compared to the post-layout simulation results.

3.1.2 TECHNOLOGY CONSIDERATIONS

In the simulations presented in these sections, the parasitic effects of all the cells, including transistors, are not negligible and must be considered. The equivalent model is used for the parasitic extracted from the layout. A “Cc+C” equivalent circuit is extracted using Calibre[15], representing the parasitic capacitors around the cell depending on their size and location in the layout. Where “C” capacitor represents capacitor to ground and “Cc” capacitor coupling between wires. All the post layout simulations included in this chapter use this parasitic extraction methodology.

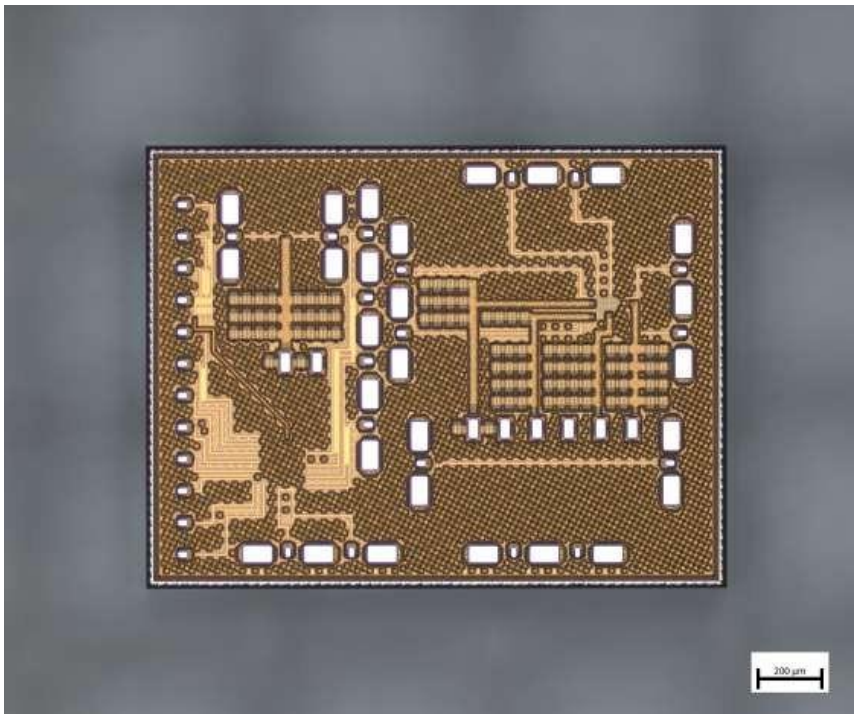


Figure 32 : First Tape out including directive coupler, Wideband inductorless LNA and a polyphase filter on standalone configuration

As illustrated in Figure 33, bulk CMOS architecture involves the construction of transistors on top of a silicon wafer’s surface, while PD SOI isolates MOS transistors from the substrate using a buried oxide. This isolation permits the transistor to operate as a floating or body contact device. Moreover, the thickness of the body in PD-SOI is still too high to have full control of the depletion layer, hence the term "partially-depleted" SOI. For millimeter wave design, key performance indicators for transistors are gain (f_{MAX}), noise figure, phase noise, and power-handling capabilities.

[15] Parasitic extraction tool

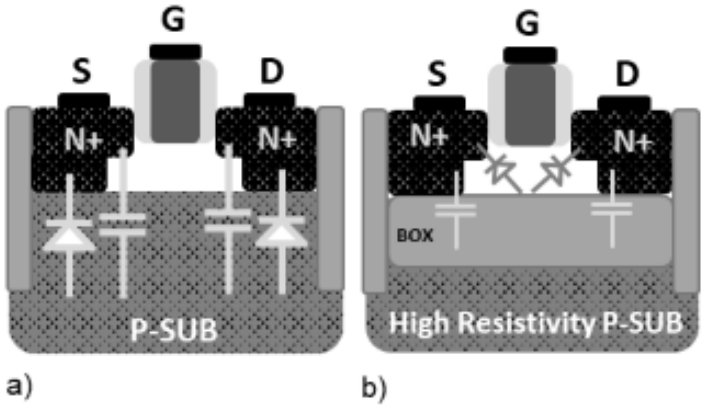


Figure 33 : n-MOSFETs cross section illustration for a) bulk CMOS , b) PD-SOI CMOS

Figure 34 shows the measured f_{MAX}, for various technology gate lengths. The mobility of electrons and holes is very similar in deep sub-micron CMOS SOI, which makes the performance of p-type MOS (PMOS) transistors comparable to that of n-type MOS (NMOS) transistors. This property provides a unique advantage compared to previous technologies, where PMOS was not suitable for RF applications. Due to these benefits, the circuits in this contribution were designed using the PDSOI RF45nmSOI technology.

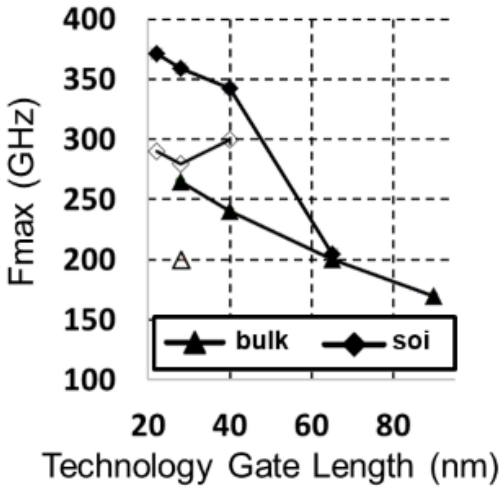


Figure 34 : Measured f_{max} for various technology gate length (filled = nFET ; unfilled = pFET)

3.2 DIRECTIONAL COUPLER CIRCUITRY

Signal separation is the critical step in measuring a portion of the incident signal as a reference and separating the forwarded and reflected traveling waves at the device under test's input. This function could be carried out by directional couplers, and their accuracy is impacted by their directivity[16]. Effectively, directional couplers could be implemented using transmission line structures including waveguides, microstrips and striplines. However, these directional couplers have limitations, including a limited frequency range and a large area requirement to cover more than one frequency decade, even with the use of multi-section structures [84], multilayer microstrip structures with broadside slot coupling [85] and wideband stripline structures loaded with stubs [86]. In addition to the large area occupied, these couplers have been designed over PCB laminates and are not always carried out over a silicon substrate with good performance. An alternative approach is resistive bridges, namely Wheatstone bridges [87] , which operate over a large frequency range and are less expensive (less area consumption).

The present section provides a brief overview of the resistive coupler's functionality. It defines the resistive directional coupler figure of merit. After that, it illustrates the link between coupler directivity and reflection measurement accuracy. Afterwards, it depicts the design flow of the final version of the directional coupler to meet the initial targeted requirement of a 22 dB coupling factor and 55 dB of isolation. Moreover, the first version of the resistive coupler has been measured and has been used to improve the final version performance, as will be further explained in more depth in the following.

3.2.1 RESISTIVE COUPLER FUNCTION: WHEATSTONE BRIDGE APPROACH

The “Wheatstone Bridge” was first discovered in 1883 by Samuel Hunter Christie and made famous by Charles Wheatstone in 1843. It was commonly used in a variety of applications, including strain gauge measurement, temperature measurement, precision measurement of small resistances, and impedance measurement [88].

As shown in Figure 35, the bridge has four resistors connected in a loop. The bridge's main characteristic is that the voltage at the two arms of the bridge (A and B) is proportional

[16] Directivity is defined as the ratio of incident signal leakage to the fully reflected signal. It refers to the coupler's ability to distinguish between waves propagating in forward and reverse directions.

to the arms' resistances. In the balanced condition of the bridge ($R_1R_3 = Z_{DUT}R_2$), the potential difference between A and B points is equal to zero ($V_A = V_B$).

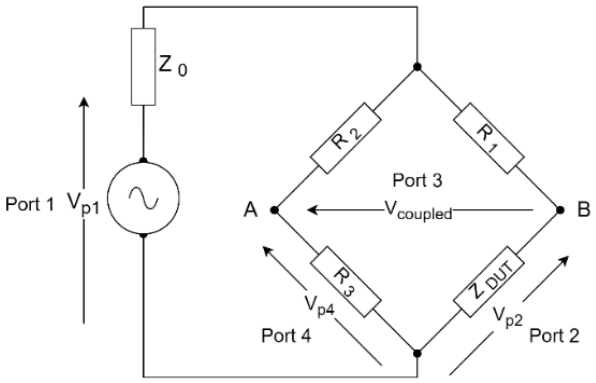


Figure 35: Basic resistive bridge structure

In balance, the measurement circuit is isolated from the source, giving the Wheatstone bridge its directional properties. Furthermore, as shown in Figure 36 (a), the bridge can be driven forward to couple the incident wave or backward to extract a portion of the reflected signal waves, resulting in a bi-directional coupler when both directions are driven. This architecture, which was previously used in [73], has two ports for the reference and reflected signals, with the coupled port feeding the reference channel and the isolated port feeding the reflection measurement channel. In addition, it allows a low insertion loss due to the small resistance R_5 between the input and output ports, whereas for the remaining resistor values, these are obtained for the targeted coupling, directivity, and isolation values.

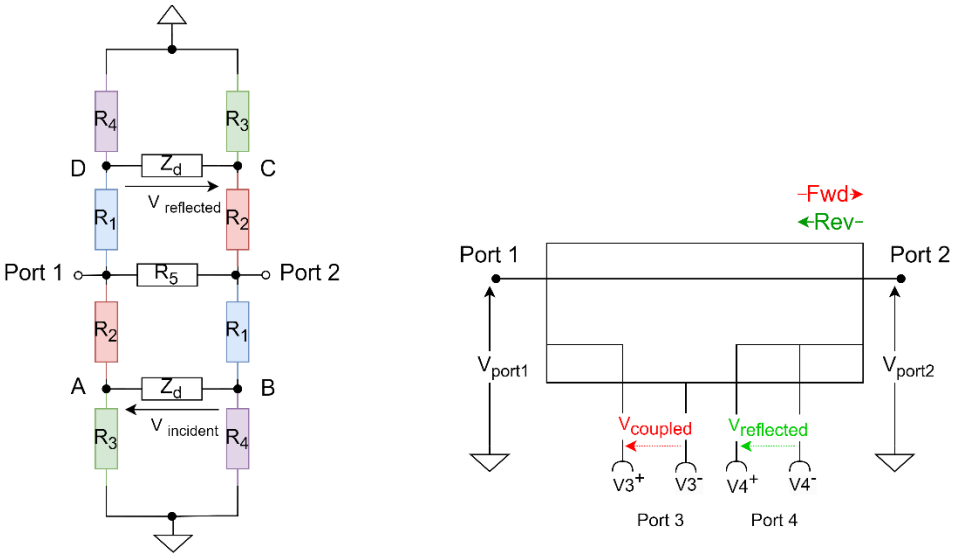


Figure 36 : Forward and reverse directional bridge topology "Bi-directional bridge topology"

Using the voltage divider formula at the four arms of this bridge A,B,C and D (Figure 36) and Kirchhoff's voltage law[17] at port 2, five equations are expressed as follows (18):

$$\frac{V_{port1} - V^{+}_{incident}}{R_2} = \frac{V^{+}_{incident}}{R_3} + \frac{V^{+}_{incident} - V^{-}_{incident}}{Z_d}$$

$$\frac{V_{port2} - V^{-}_{incident}}{R_2} = \frac{V^{-}_{incident}}{R_4} - \frac{V^{+}_{incident} - V^{-}_{incident}}{Z_d}$$

$$\frac{V_{port1} - V^{-}_{reflected}}{R_1} = \frac{V^{-}_{reflected}}{R_4} - \frac{V^{+}_{reflected} - V^{-}_{reflected}}{Z_d} \quad (18)$$

$$\frac{V_{port2} - V^{+}_{reflected}}{R_2} = \frac{V^{+}_{reflected}}{R_3} + \frac{V^{+}_{reflected} - V^{-}_{reflected}}{Z_d}$$

$$\frac{V_{port2} - V_{port1}}{R_5} + \frac{V_{port2} - V^{-}_{incident}}{R_1} = -\frac{V_{port2} - V^{+}_{reflected}}{R_2} - \frac{V_{port2}}{Z_0}$$

Where:

- Z_0 refers to the coupler characteristic impedance that should be nearly 50 Ω
- Z_d presents the input impedance of the next building bloc.
- Resistances R_1, R_2, R_3, R_4 and R_5 are illustrated in Figure 36.
- Voltages V_{port1}, V_{port2} $V_{reflected}$ and $V_{incident}$ are presented in Figure 36.

According to the definitions of coupling factor (C), transmission insertion loss (IL), directivity (D), and isolation (ISO) (19). These parameters have been extracted from (18) and are expressed according to the resistance values as follows [73]:

[17] It states that in any complete loop within a circuit, the sum of all voltages across components which supply electrical energy (such as cells or generators) must equal the sum of all voltages across the other components in the same loop.

$$IL\ (dB) = 10\log\left(\frac{V_{port1}}{V_{port2}}\right) = 10\log\left(\frac{g + \frac{2acd}{be - c^2}}{f - \frac{1}{be - c^2}(bd^2 + a^2e)}\right)$$

$$C\ (dB) = 10\log\left(\frac{V_{port1}}{V_{incident}}\right) = 10\log\left(\frac{1}{be - c^2}(a(e - c) + d(c - b)IL)\right) \quad (19)$$

$$ISO\ (dB) = 10\log\left(\frac{V_{port1}}{V_{reflected}}\right) = 10\log\left(\frac{1}{be - c^2}(d(b - c) + a(c - e)IL)\right)$$

$$D\ (dB) = 10\log\left(\frac{V_{incident}}{V_{reflected}}\right) = -C + ISO$$

Where: $a = \frac{1}{R_2}$, $b = \frac{1}{Z_d} + \frac{1}{R_2} + \frac{1}{R_3}$, $c = \frac{1}{Z_d}$, $d = \frac{1}{R_1}$, $e = \frac{1}{Z_d} + \frac{1}{R_1} + \frac{1}{R_4}$, $f = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_5} + \frac{1}{Z_0}$ and $g = \frac{1}{R_5}$.

3.2.2 COUPLER DIRECTIVITY AND REFLECTION COEFFICIENT MEASUREMENT ACCURACY

Thereafter, the parameters in (19) were processed to adjust the resistances to achieve the targeted isolation (55 dB), adding to this an additional parameter, the directivity. To establish the directivity value, the following discussion examines the influence of directivity on the precision of the reflection measurement.

In [89], Antritsu links the accuracy of the reflection measurement with the directivity of the directional coupler. As illustrated in Figure 37, the reflection signal from the DUT is represented by E_r and the unwanted directivity signal from the directional device is represented by E_{dir} . Both E_r and E_{dir} are voltages. This illustration shows that the reflection measurement accuracy increases as the directivity approaches the reflected signal in amplitude (the leakage signal E_{dir} declines).

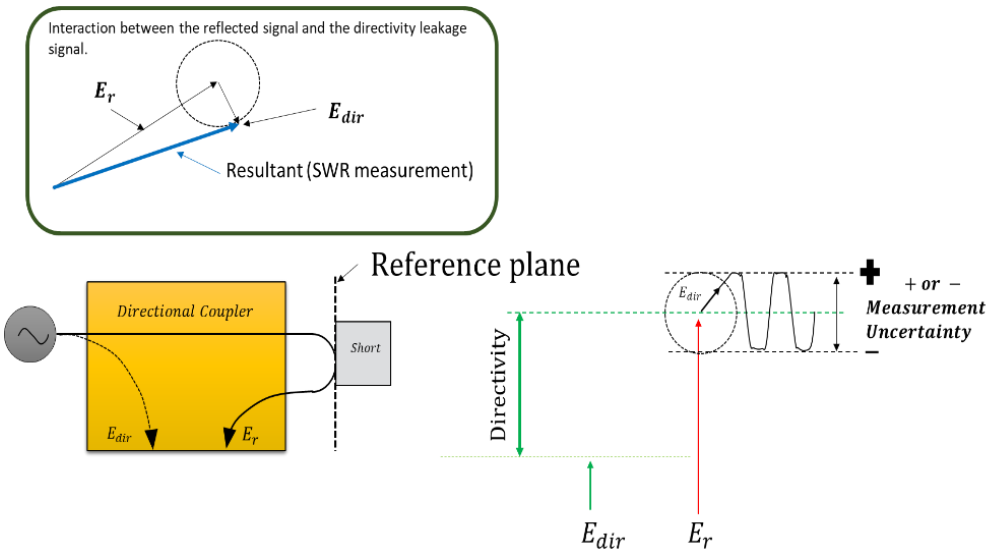


Figure 37 : Uncertainty in reflection measurement due to directivity signal interaction [89]

Two cases set the minimum and maximum deviations: the minimum uncertainty occurs when the voltages E_r and E_{dir} have the same amplitude and are in phase. The resulting voltage vectors double and the power increases by a factor of four ($P=V^2/R$), yielding a 6 dB reduction in return loss measurement. On the other hand, the highest uncertainty occurs when the signals are 180 degrees out of phase, with the same amplitude, the DUT seems to be perfectly matched, which is not the case. Thus, the resulting vector is equal to zero voltage, which corresponds to an infinite reflection in dB.

Figure 38 links intrinsically both the directivity and the reflection sensitivity with the degree of uncertainty in dB. For example, when measuring devices with a return loss greater than 20 dB, to maintain ± 1 dB uncertainty, a directivity value better than 40 dB is required.

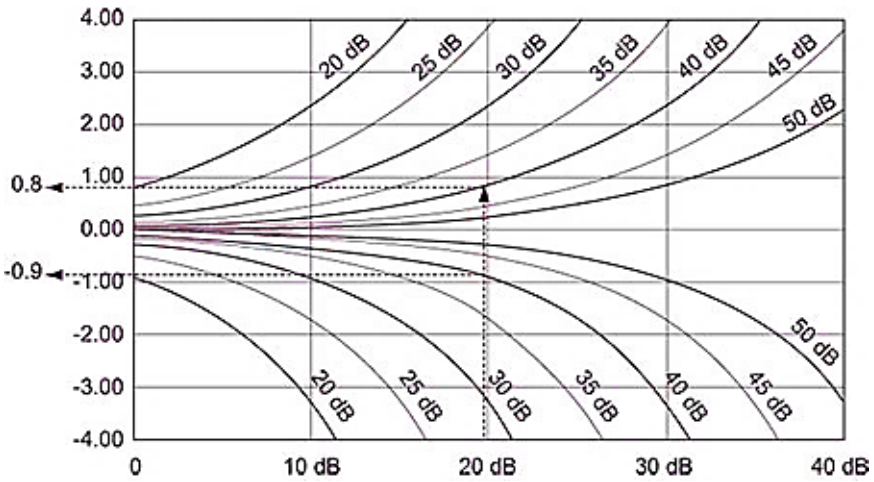


Figure 38 : Return Loss Uncertainty Chart for different directivity values plotted in dB [89]

Considering the state of the art, directivity better than 30 dB is unachievable, considering the design restrictions over a wide bandwidth, including substrate losses, surface limitations and parasitics [85], [90], [91] .

The initially targeted directivity is set to 33 dB (C (22 dB) - ISO (55 dB)). This value is consistent with the study findings. Hence, the targeted minimum directivity is set to 30 dB. However, these values could be significantly improved while calibrating the VNA system to identify the directivity error vectors in the VNA system (as explained in 1.1.4).

3.2.3 DIRECTIONAL COUPLER DESIGN

Based on the targeted directivity, the theoretically estimated insertion losses, coupling factor and isolation (19) are 1.5 dB, -22 dB, and -60 dB respectively. For R1, R2, R3, R4, and R5 values of 190 Ω, 140 Ω, 290 Ω, 230 Ω, and 8 Ω, respectively. The configuration of the proposed coupler is shown in Figure 40. The compact circuit covers an area of 9.6 µm x 27.5 µm, ensuring a symmetrical layout to reduce parasitic effects.

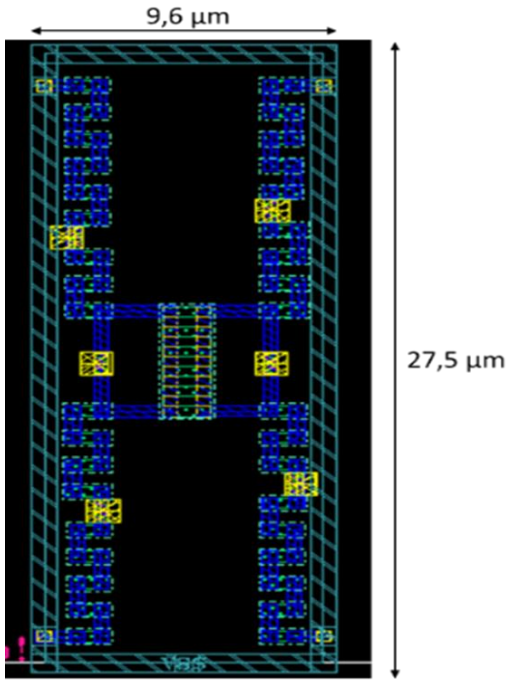
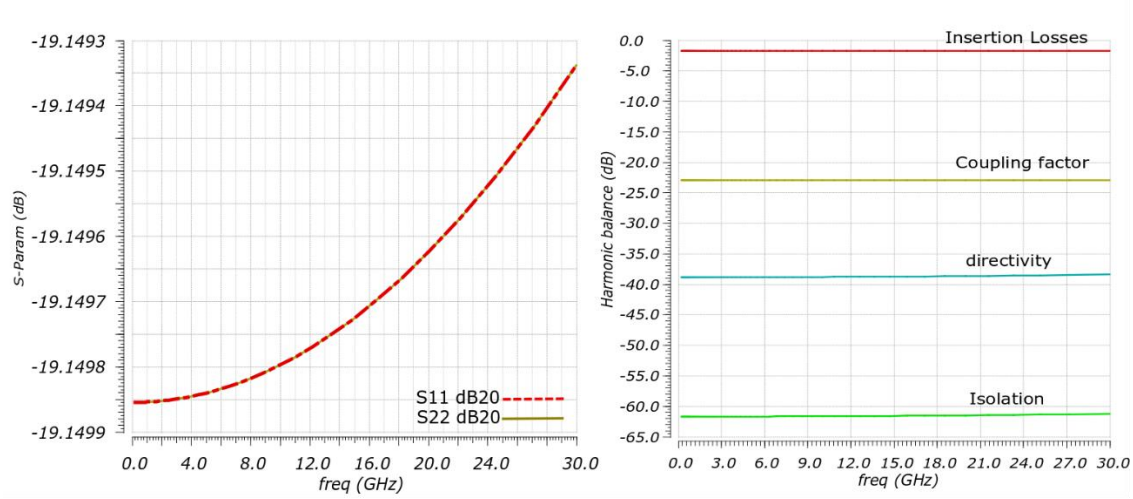


Figure 39 : Wideband directional coupler layout

Considering, the post layout simulations, the simulated insertion losses varies from 1.7 dB to 1.8 dB at 200 MHz and 30 GHz, respectively. The input and output return losses are better that 19 dB over the 30 GHz impedance. The mean values of coupling ratio and isolation are 22 dB and 61 dB over the bandwidth, respectively, resulting in a directivity of 39 dB, Figure

40. This promising directivity maintains ± 0.9 dB uncertainty while measuring a DUT return loss greater than 20 dB (Figure 38).



(a) (b)

Figure 40 : (a) Input and output return losses (b) IL, C, ISO and D Vs frequency @Pin=0 dBm.

3.2.4 FIRST VERSION OF THE RESISTIVE COUPLER: MEASUREMENT RESULTS

During the thesis first year, a resistive bridge was printed in a standalone configuration to seek the output return loss, insertion losses, and coupling factor. As shown in Figure 41, the first printed Circuit, with the same resistance values, is one half of the full bidirectional coupler presented earlier. The aim was to first validate the well-functioning of the resistive bridge topology and to assess the disparities between simulations and measurement results.

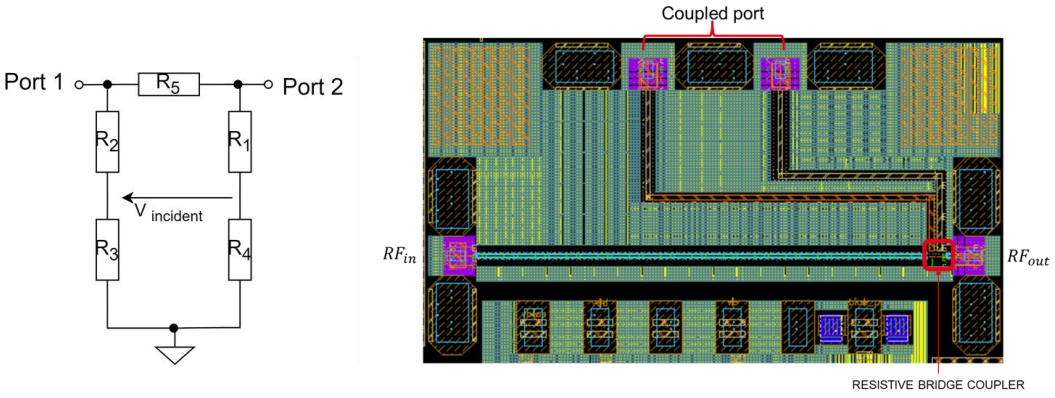


Figure 41 : Resistive bridge circuit architecture and micrograph of the printed circuit on standalone configuration

Considering the measurement results, as shown in Figure 42, the insertion losses range from 3.4 to 5.2 dB, the coupling factor is between 20 and 24 dB, the isolation varies between

48 and 53 dB and the input and output return losses are better than 8.6 dB over the 24 GHz bandwidth[18].

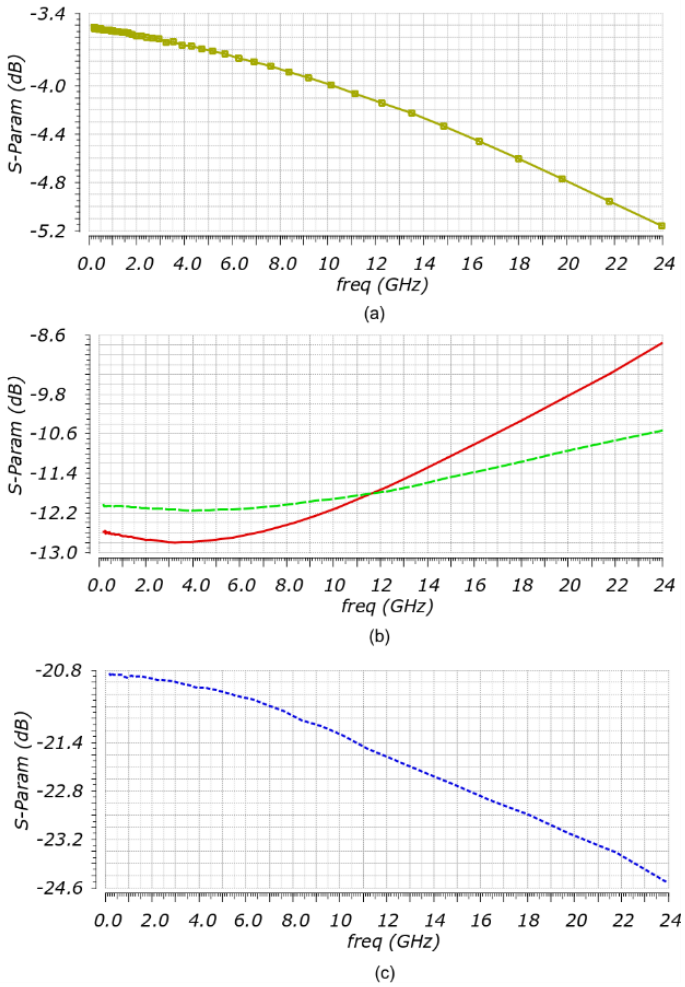


Figure 42: Measurement results (a) Insertion losses (b) dashed line: output return loss undashed : input return loss (c) coupling factor

Table 4 shows the measured and simulated values of the first version coupler. The coupler core input and output matching deviated from 19 dB due to the transmission lines (TL). Knowing that the length of these lines is ruled by the minimum distance to have between the pads (200 µm). Similarly, the insertion losses deteriorated from 1.5 dB to 5.2 dB due to TL losses. The symmetry of the final version of the circuit was improved (Figure 40), and secondly, dummy resistances were added to meet the precise value of the resistance R_5 equal to 8 Ω.

[18]The bandwidth was limited by the VNA used in the measurement setup.

	Simulated	Measured	unit	Comment
Insertion losses	1.5	5.2	dB	In the final version, the transmission line (TL) insertion loss was minimized by shortening the TLs.
Coupling factor	22	20-24	dB	In the final version, the parasitic effects were reduced by improving the layout symmetry, which was achieved through careful design.
Input / output matching	-19 (without TLs)	<-10 @ 20 GHz (with TLs)	dB	In the latest version, the transmission line (TL) impedances were considered.

Table 4: Measured Vs simulated coupler values

Overall, the measurements of the first circuit have led to improvements in the final circuit. The final version of the coupler post-layout simulations meets the initial specifications. In the following section, the development of the image rejection circuitry will be undertaken.

3.3 IMAGE REJECTION CIRCUITRY

Image rejection (IMR) circuitry is used to eliminate interference from the unwanted image frequency that may hinder the performance of the demodulator. The effectiveness of IMR depends mainly on a precise 90° phase shift for the LO and IF blocks. Regarding this correlation, in [92], the impact of amplitude and phase imbalance on the image rejection ratio has been theoretically analyzed. The total phase imbalance is calculated as the sum of the deviation from quadrature in the LO and intermediate frequency (IF) inputs, along with the two mixers. Similarly, the total amplitude imbalance is calculated by summing the individual amplitude imbalances in the LO and IF blocks and the two mixers. As illustrated in Figure 43, the study shows that if the amplitude imbalance is less than 1 dB, the image rejection ratio can range from 9 to 50 dB, depending on the phase imbalance value. Therefore, it is crucial to aim for the lowest possible phase quadrature error between the LO and IF building blocks, with an amplitude imbalance less than 1 dB, to achieve optimal image rejection performance in the demodulator.

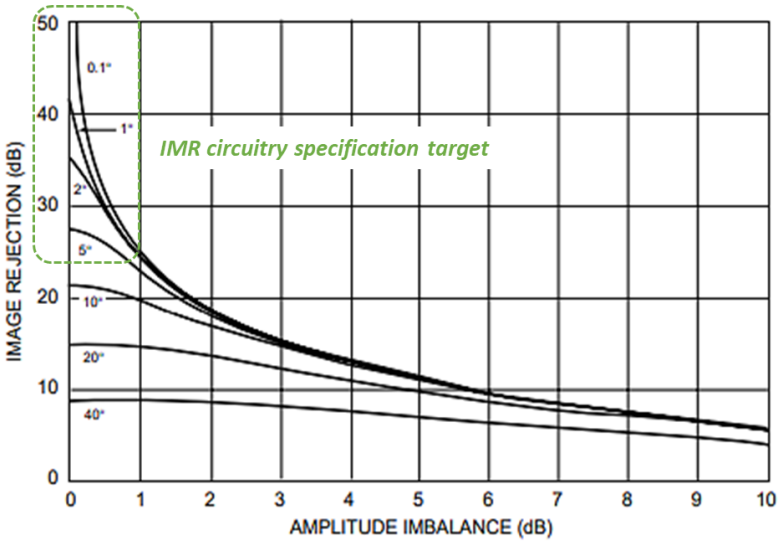


Figure 43 : Image rejection ratio variation with the amplitude and phase imbalance in dB and degree, respectively

As illustrated in Figure 44, the adopted design approach involves using a Double-Balanced Image Rejection (IMR) mixer. Accordingly, LO and IF I/Q signals are required to reject the image frequency $f_{RF} = f_{lo} - f_{IF}$. For the LO quadrature generation, a wideband polyphase filter was designed to provide differential I and Q signals. For the IF quadrature at

455 kHz, a digital frequency divider was implemented. Finally, the "LO" and "IF" quadrature signals are fed into the IMR double balanced up conversion mixer.

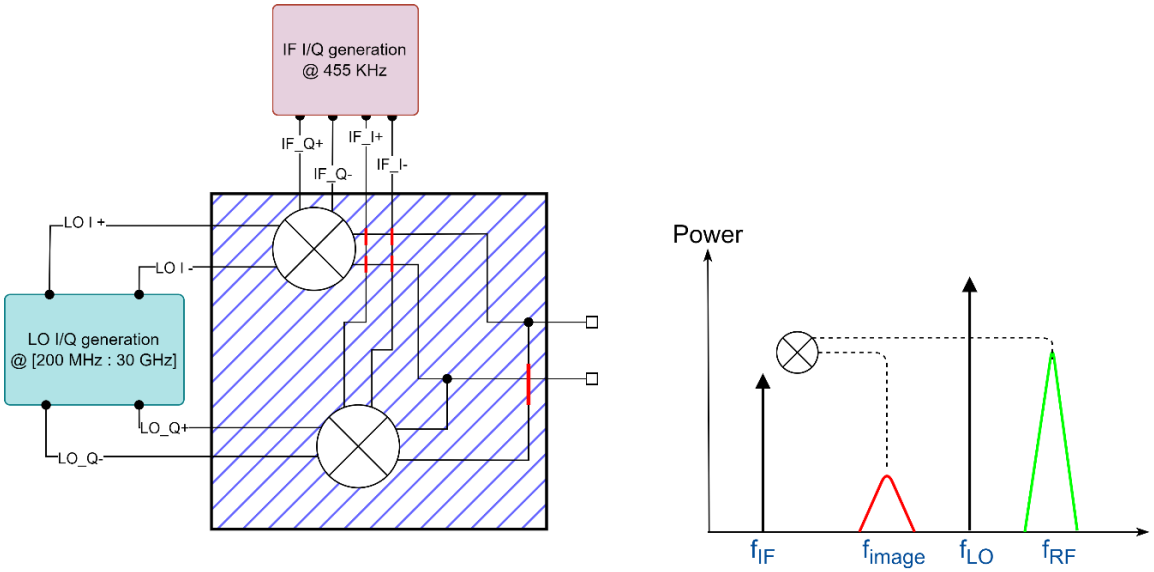


Figure 44 : image rejection circuitry

As a follow-up, the present section covers the design and validation of each of these modules, starting with the polyphase filter, through the IF quadrature generation, and lastly the double balanced image rejection mixer.

3.3.1 WIDEBAND POLYPHASE FILTER FOR LO QUADRATURE GENERATION

One way to use polyphase filters is to generate quadrature signals. The circuit, as shown in Figure 45, consists of a passive RC structure contributing to one pole frequency called the 'notch' where $f_{pole} = \frac{1}{2\pi RC}$. The input feeding topologies, type I and type II, result in two different transfer functions (20). Accordingly, type I has a constant amplitude difference over bandwidth with a 90° phase difference at the RC pole frequency f_{pole}, while Type II has a constant 90° phase difference over bandwidth and unity amplitude balance at the RC pole frequency. The latter topology (Type II) was likely chosen due to its 90° shift over the 30 GHz bandwidth.

$$H_{type\ I} = \frac{\Delta V_{I,out}}{\Delta V_{Q,out}} = \frac{1 - sRC}{1 + sRC}$$
$$H_{type\ II} = \frac{\Delta V_{I,out}}{\Delta V_{Q,out}} = \frac{1}{sRC} \quad (20)$$

$$\alpha = \frac{f_{pole2}}{f_{pole1}} = \frac{f_{pole\,3}}{f_{pole2}} = \frac{f_{pole\,n}}{f_{pole\,3}} \quad (21)$$

- Where n is integer referring to the number of cascaded stages.

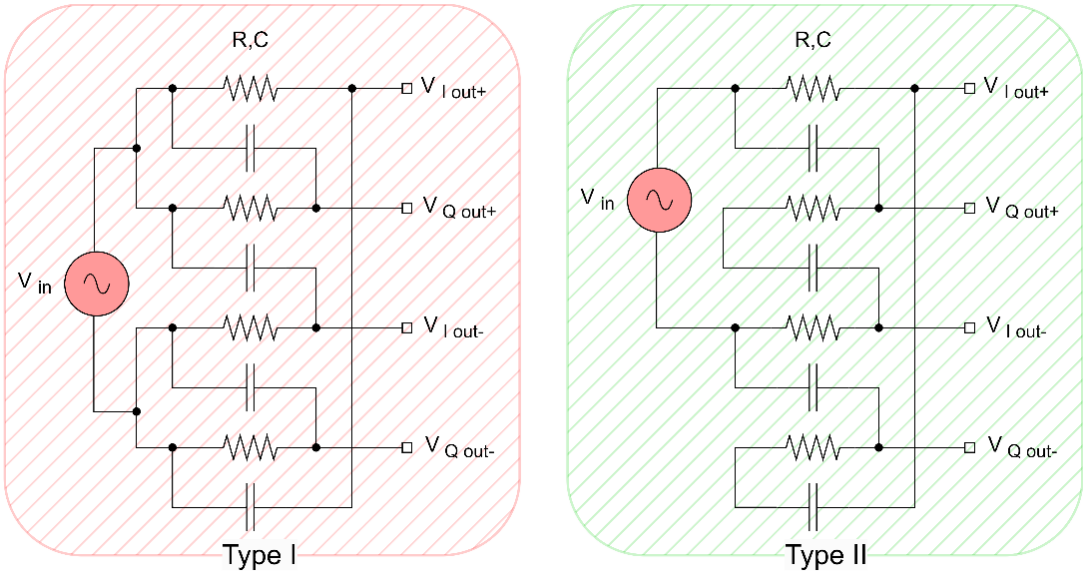


Figure 45 : One section of the PPF with two different input feeds

Type II PPF has been chosen to provide the 90° shift over the bandwidth. The cascaded n-PPF places the notches of the multistage PPF at an equal frequency ratio α (21). Optimizing the amplitude balance between the quadrature signals I and Q involves finding the optimum

pole frequency ratio to achieve the lowest amplitude imbalance. Based on the simulation results, the optimal pole frequency ratio for the PPF is set to 1.2. Thus, assuming that f_{pole1} is set to the minimum desired frequency of 200 MHz, the maximum number of cascaded stages should be set to four in order to achieve the lowest amplitude imbalance (|0.15 dB|) while having a phase imbalance of |3 degrees| over the three bandwidths, as depicted in Figure 46.

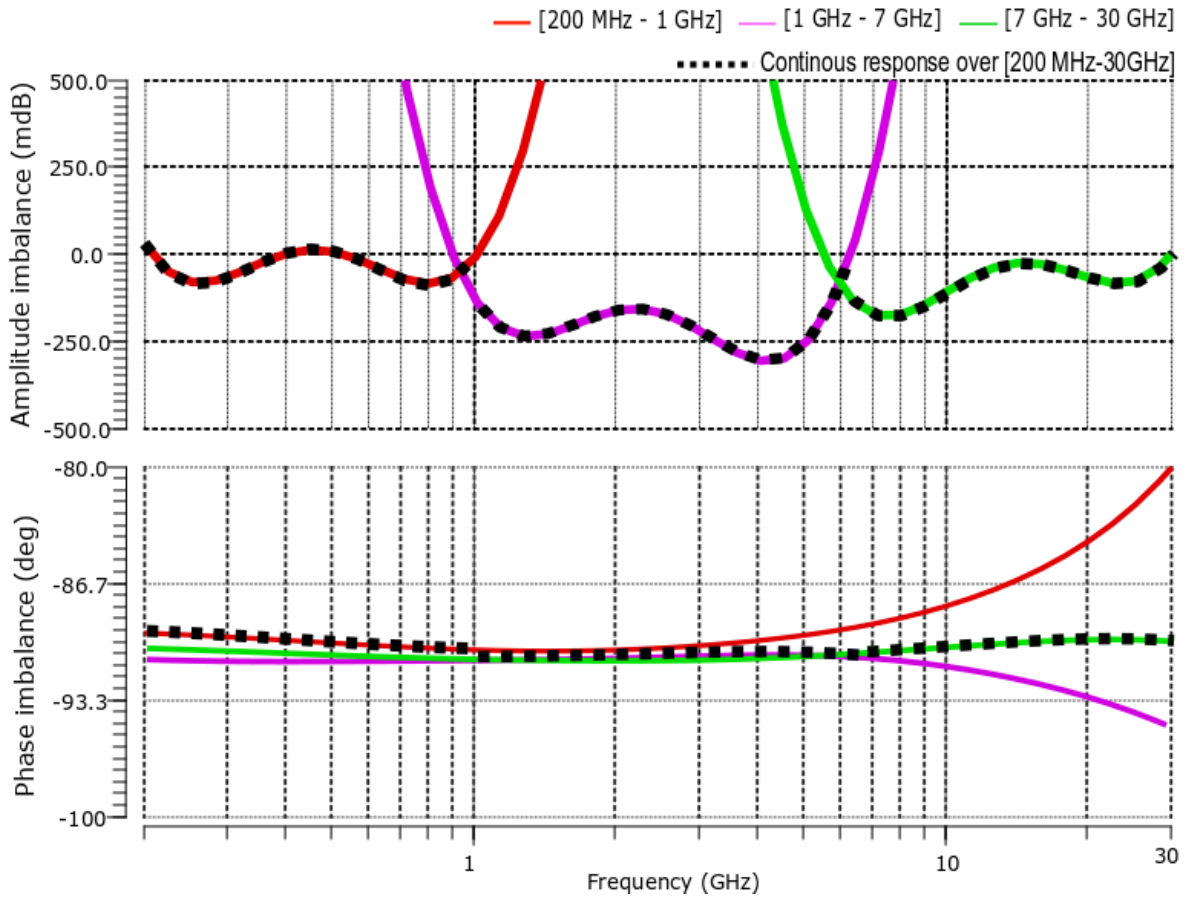


Figure 46 : Amplitude imbalance and phase imbalance tolerance between the output signals in quadrature

To cover the entire 30 GHz bandwidth while adhering to the optimal alpha value of 1.2, three four-stage polyphase filters were implemented in parallel. Each filter was used to cover a specific frequency band: 185 MHz -1GHz, 1 GHz -7 GHz, and 7 GHz-30 GHz. This way, only one filter was active at a given time, allowing for efficient coverage of all the required bandwidth. Table 5 gathers the RC values for each stage. As depicted in Figure 47, the design of a polyphase filter occupies a compact area of 200 µm x 115 µm.

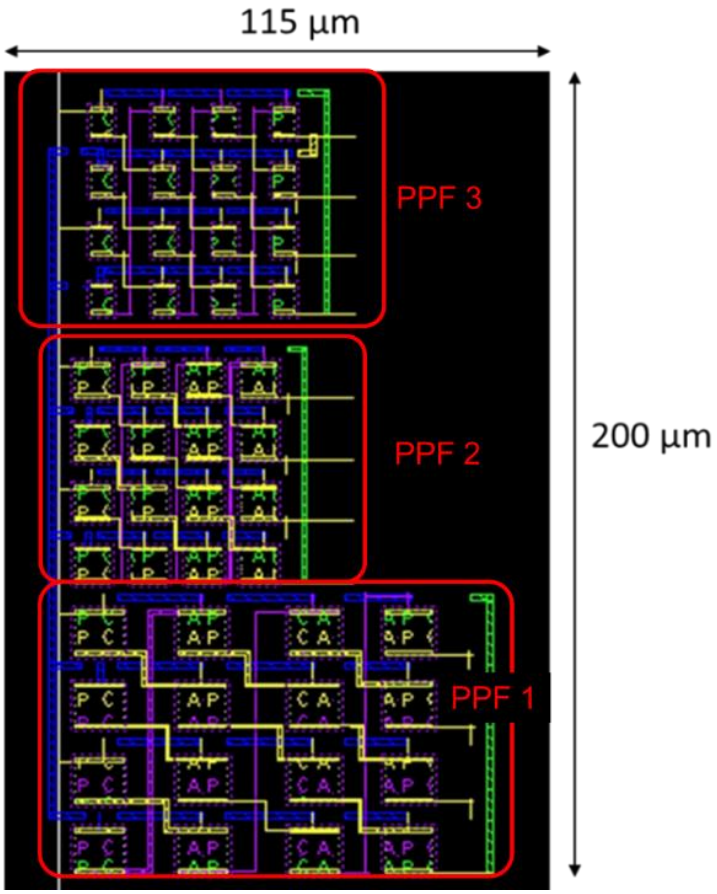


Figure 47 : Three 4-stage PPFs layout

Polyphase filters RC values	Stage 1	Stage 2	Stage 3	Stage 4
PPF 1	800 Ω	1.5k Ω	2k Ω	4k Ω
0.185 -1GHz	200 fF			
PPF 2	300 Ω	500 Ω	900 Ω	1.45k Ω
1 -7 GHz	107 fF			
PPF 3	117 Ω	180 Ω	300 Ω	1.4 Ω
7 - 30 GHz	51 fF			

Table 5: PPF's RC values

Regarding the post layout simulation, in Figure 48, the 4-stage PPF1 and PPF2 respect the 12 dB insertion loss (3 dB per stage). However, this circuit suffers from significant IL

degradation, which reaches 22 dB losses above 20 GHz due to the circuit's parasitic. To alleviate this gain drop, active amplification circuitry will be used to increase the signal strength.

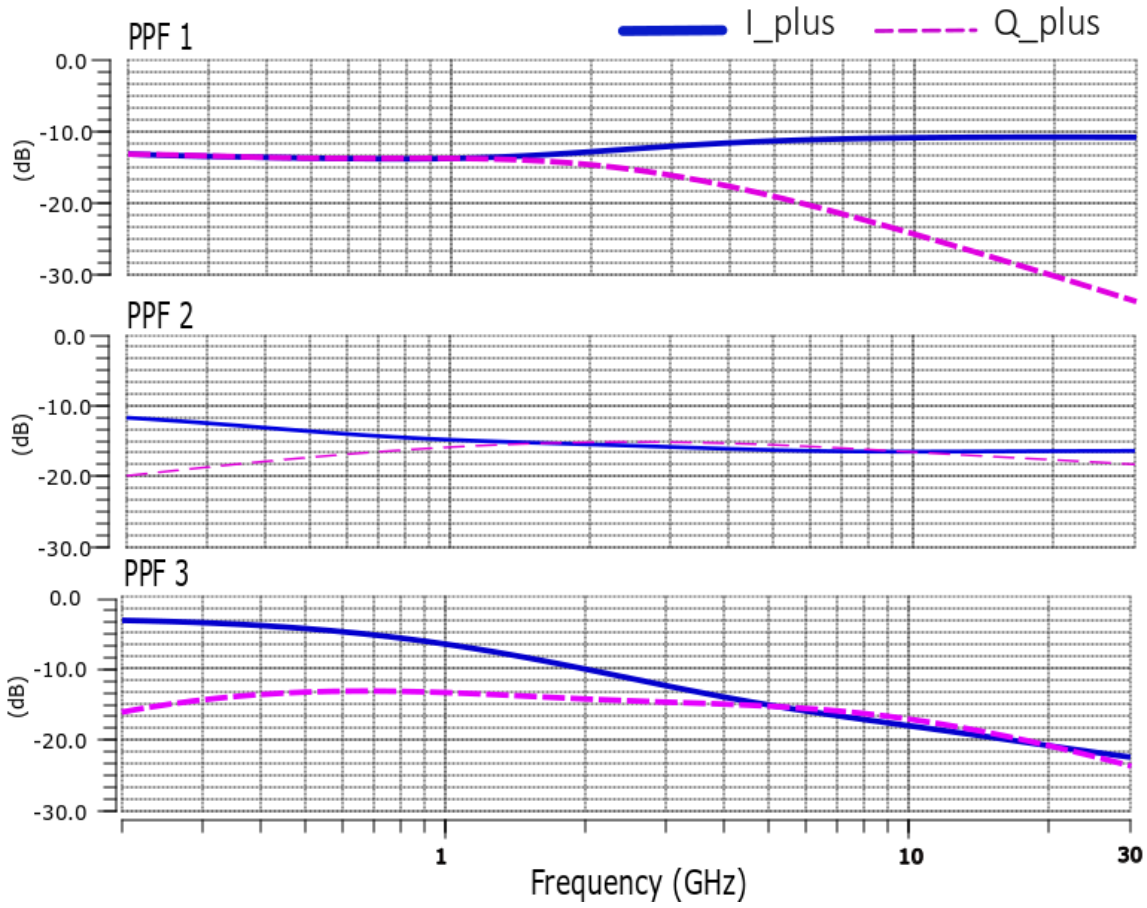
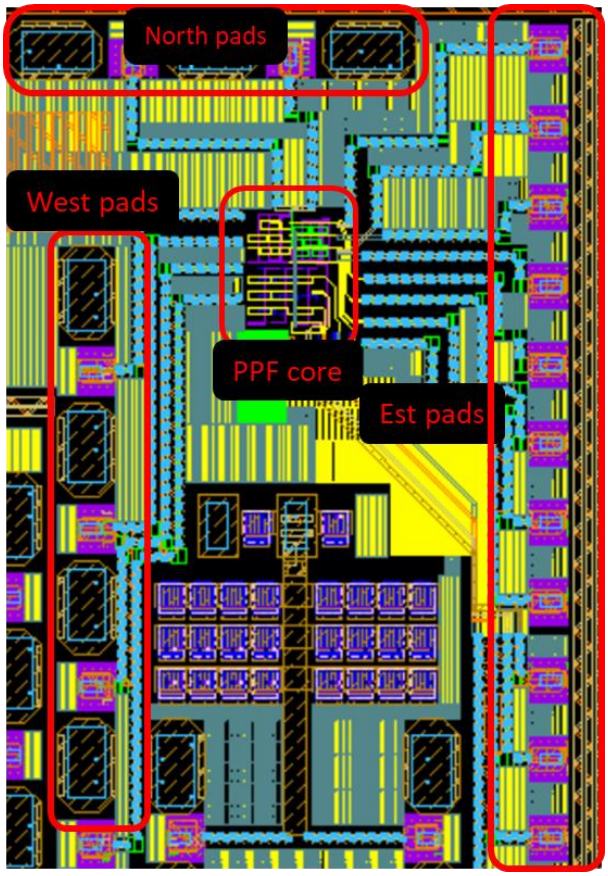


Figure 48: Insertion losses of thre three 4-stage PPFs

3.3.2 FABRICATED POLYPHASE FILTER: MEASUREMENT RESULTS

The presented circuit was fabricated and measured in a standalone configuration (Figure 49), as mentioned in the introduction of this chapter. Concerning the measurement setup, the RF input signal is provided by a VNA ZVA24 network analyzer used as a signal source generator up to 24 GHz. A preamplifier is used to provide the required input power and isolate the VNA port. The quadrature phase error measurements were displayed using an oscilloscope to show the IQ imbalance in both time and frequency domains. In addition, a specific high impedance probe was used to sense each output port. To adopt the same phase reference for each single ended output, each output phase is synchronized with the source phase, saved in a dataset, and then the probe senses the next output.



Stages	Differential input	Out (Est probe) (I+, I-, Q+,Q-)
First BW **[200 MHz->1 GHz]**	west Probe **(GSGSGSGS)**	**(SGSGSGSGSGSGSGSGSGSGSG)**
Second BW **[1GHz->6 GHz]**	west Probe **(GSGSGSGS)**	**(SGSGSGSGSGSGSGSGSGSGSG)**
Third BW **[6 GHz->35 GHz]**	North probe **(GSGSG)**	**(SGSGSGSGSGSGSGSGSGSGSG)**

Figure 49 : Polyphase filter micrograph and IN/out pads placement

Figure 50 illustrates the I/Q signals phase output over the three operation bands. After processing[19], the phase imbalance between the differential signals I and Q is below 3 degrees for the three bandwidths. Additionally, the insertion losses range from 12 to 30 dB. In comparison to the post layout simulations, an extra 8 dB of insertion losses are added at 30 GHz. This is due to the long input and output transmission lines, linking the PPF core to the pads, which are constrained by the surface of the circuit.

[19] After subtracting the phase of the differential signals of both I and Q.

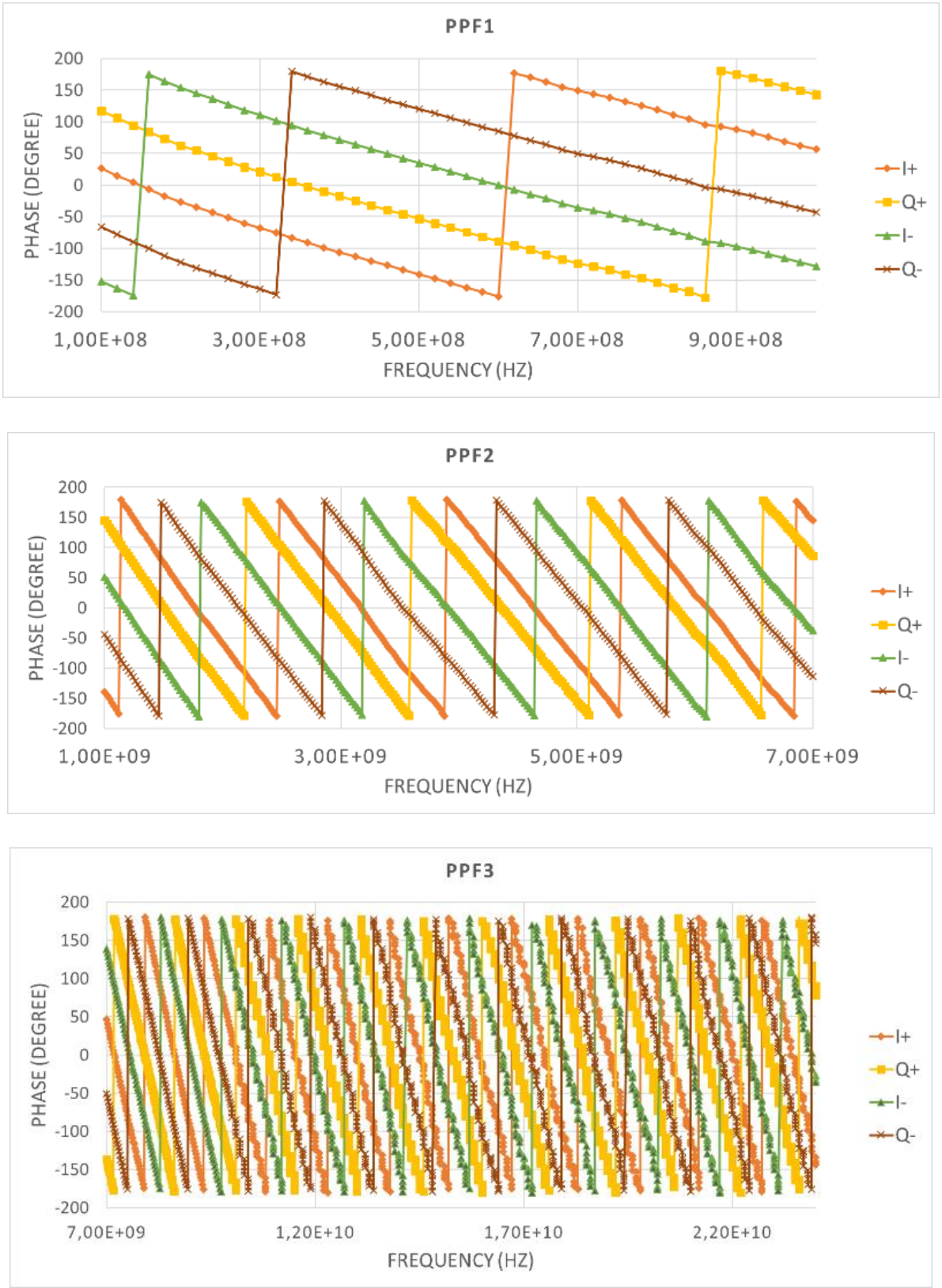


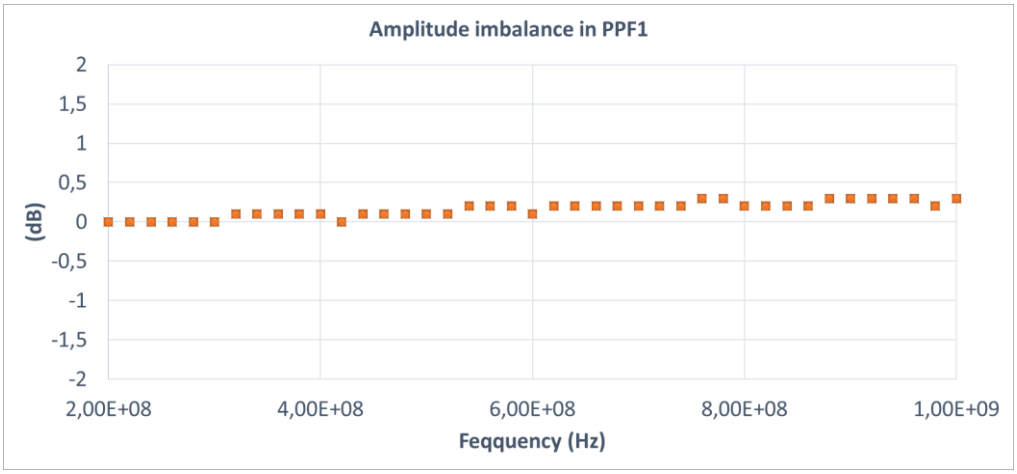
Figure 50 : Measured differential I / Q signals Phase Vs frequency for the three PPFs up to 24 GHz

As shown in Figure 51, the maximum amplitude imbalance between I and Q signals for PPF1, which covers the frequency bandwidth of 200 MHz to 1 GHz, is 0.4 dB, and compared to the post-layout simulations, the measured value meets the simulation results within a

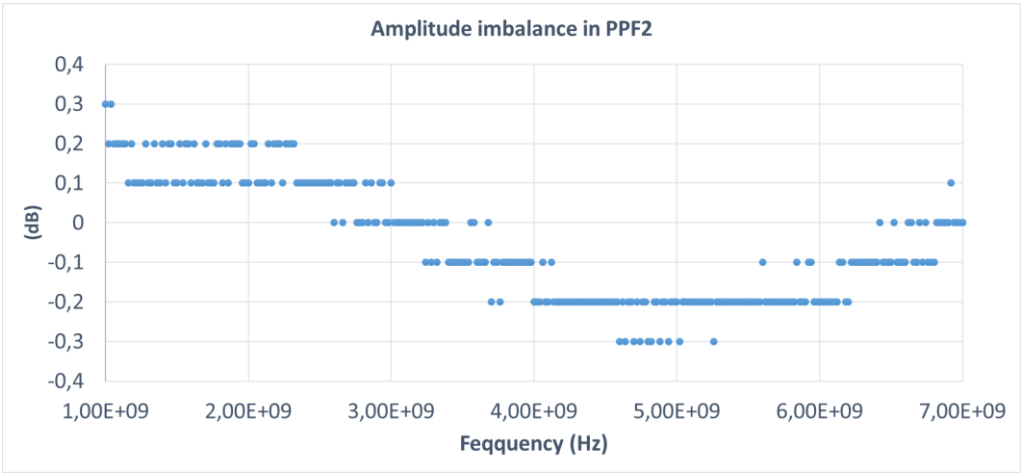
difference of 0.05 dB (Figure 46). For PPF2, which covers the frequency bandwidth of 1 GHz to 7 GHz, the deviation is 0.3 dB and also meets the simulation results within a difference of 0.05 dB. However, for PPF3, which covers the frequency bandwidth of 7 GHz to 24 GHz, the deviation is about 3 dB and has an increase in amplitude imbalance of 2.75 dB compared to the simulation results. This increase could be explained by the difference in the transmission line length of the I and Q paths due to cell placement constraints (from the PPF core to the EST PAD in Figure 49), which affect the losses of both paths directly.

In conclusion, the polyphase filter has validated the generation of LO quadrature with a precision of 90°± 3°, but with an amplitude imbalance between I and Q channels ranging from 0.5 dB to 3 dB. The deviation was higher than expected for PPF3 (+2.75 dB), which was attributed to the difference in the transmission line length of I and Q paths, as you can see in the PPF layout due to space constraints.

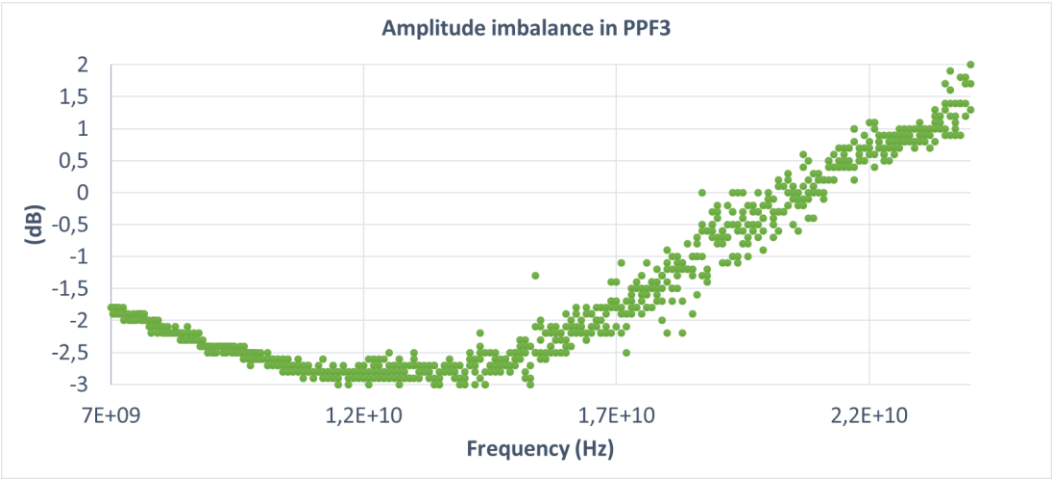
Furthermore, this measured polyphase filter remains the same as the version that will be integrated in the complete VNA circuit, but a special effort will be made to ensure equal transmission line lengths for I and Q signals to reduce imbalance at high frequencies. Overall, this study has evaluated and implemented a broadband polyphase filter capable of generating LO quadrature across a frequency range of 200 MHz to 30 GHz. As stated earlier in the introduction of this section, the IF quadrature at 455 KHz is required to reject the image frequency. The implementation of this block is described in the following subsection.



(a)



(b)



(c)

Figure 51 : Amplitude imbalance measurement between I / Q signals Vs frequency for the three PPFs up to 24 GHz (a) First stage (b) second stage (c) third stage

3.3.3 *IF QUADRATURE GENERATION*

A digital quadrature generator was designed using two D flip flops to generate an IF quadrature at 455 kHz. This standard block is not included in the design kit. Therefore, a specific design is necessary. An architectural study was conducted prior to the design of this digital quadrature generator. As illustrated in Figure 52, the quadrature signal generator comprises a frequency divider fed to the rising edge of the clock. The internal circuit consists of two D flip flops, with the output of the first flip flop being fed back to the input of the second flip flop, and the output of the second flip flop being fed back to the input of the first flip flop. This allows a signal with a quadrature phase shift to be produced.

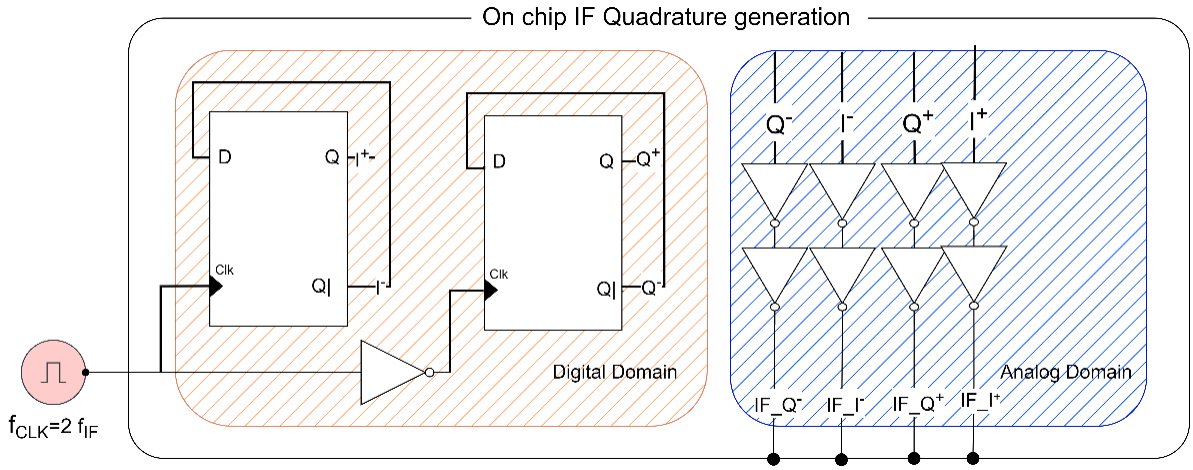


Figure 52 : Digital IF quadrature generator circuit

The current subsection will cover the design of the D Flip Flop using a dynamic digital approach, followed by determining the circuit specifications and finally confirming the IF quadrature generation through post layout simulations.

3.3.3.1 D flip flop circuit design

A D flip flop (also known as a “data flip flop”) is a type of bi-stable latch that is commonly used in digital circuits. It offers two stable states, “high” and “low”, which correspond to the two binary digits, “1” and “0”, respectively. The flip-flop has two inputs: a data input (D) and a clock input (CLK). As shown in Table 6, the D flip flop truth table, when the clock input goes from low to high, the data value is transferred to the output Q. The output of the flip flop will remain unchanged until the next rising edge of the clock signal.

CLK	D	Q	$\bar{\bar{Q}}$
↓	X	Q_{prev}	$\bar{\bar{Q}}_{prev}$
↑	1	1	0
↑	0	0	1

Table 6: D flip flop truth table

As illustrated in Figure 53, dynamic logic and static logic are two different approaches to designing digital circuits, including D flip flops. Static logic uses transistors that are either fully active or fully inactive, giving a static value to the output of the circuit.

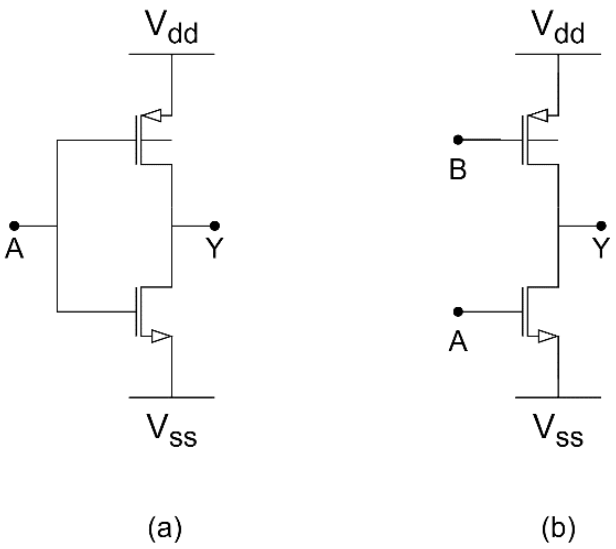


Figure 53 : (a) Static Vs (b) Dynamic digital block

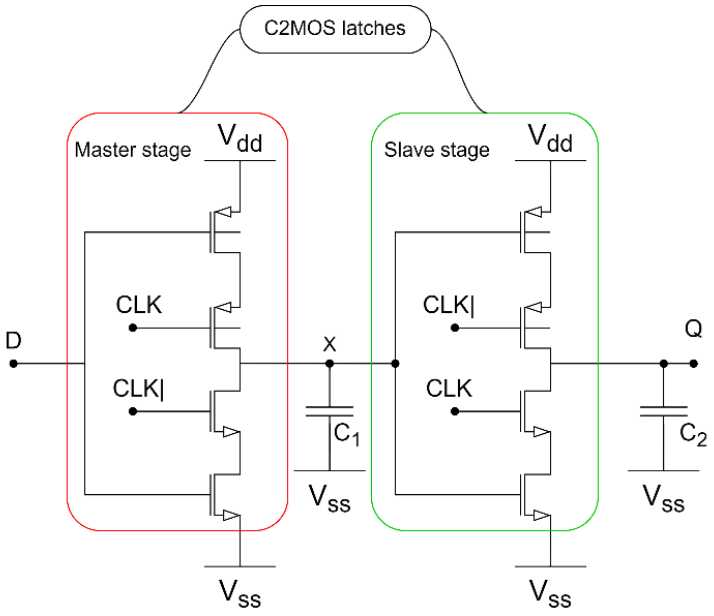
This makes static logic circuits relatively easy to implement at the expense of power consumption. Dynamic logic, on the other hand, employs transistors that are only briefly turned on or off. The output of the circuit is not a static value but rather a transient value that changes over time. In the case of quadrature generation, dynamic logic is adopted to sustain low power consumption and higher speed.

One of the dynamic strategies is clocked CMOS logic "C2CMOS", shown in Figure 54. It is based on master-slave C2mos latches[20] linked in series and enabled using clocks with

[20] The latches are designed to invert the input when the clock signal is at a high level, while the output will be in a high impedance state when the clock signal is at a low level.

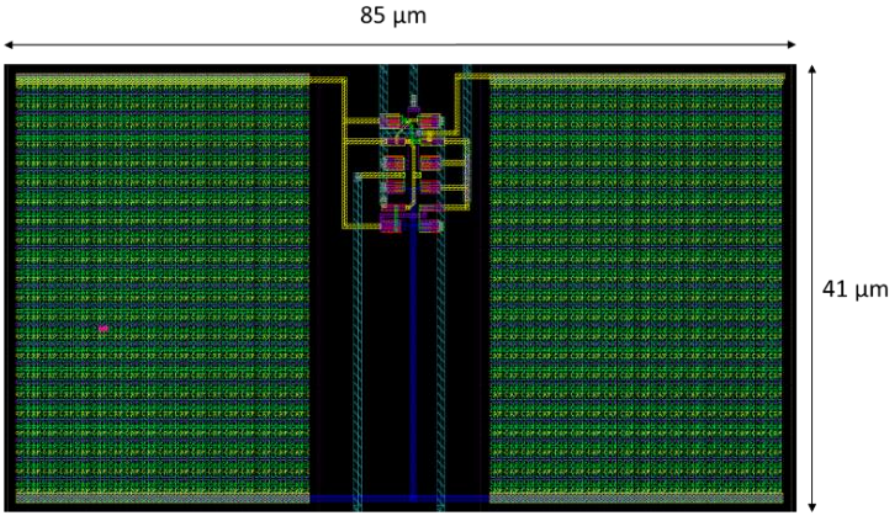
opposite phase that are insensitive to clock overlap[21].This register operates in two phases, as follows:

- When the clock signal (CLK) is 0:
    - The first driver is activated, and the master stage acts as an inverter, sampling the inverted version of D on the internal node X.
    - The master stage is in evaluation mode, while the slave section is in high-impedance state (hold mode).
    - The output Q retains its previous value stored on the output capacitor C2.
- When the clock signal (CLK) is 1:
    - The master stage is in hold mode, while the second latch evaluates the value at the node X.
    - The value stored on C1 is transmitted to the output node through the slave stage, which functions as an inverter.



(a)

[21] A C2MOS register with CLK-CLK clocking is insensitive to overlap, as long as the rise and fall times of the clock edges are sufficiently small.[93]

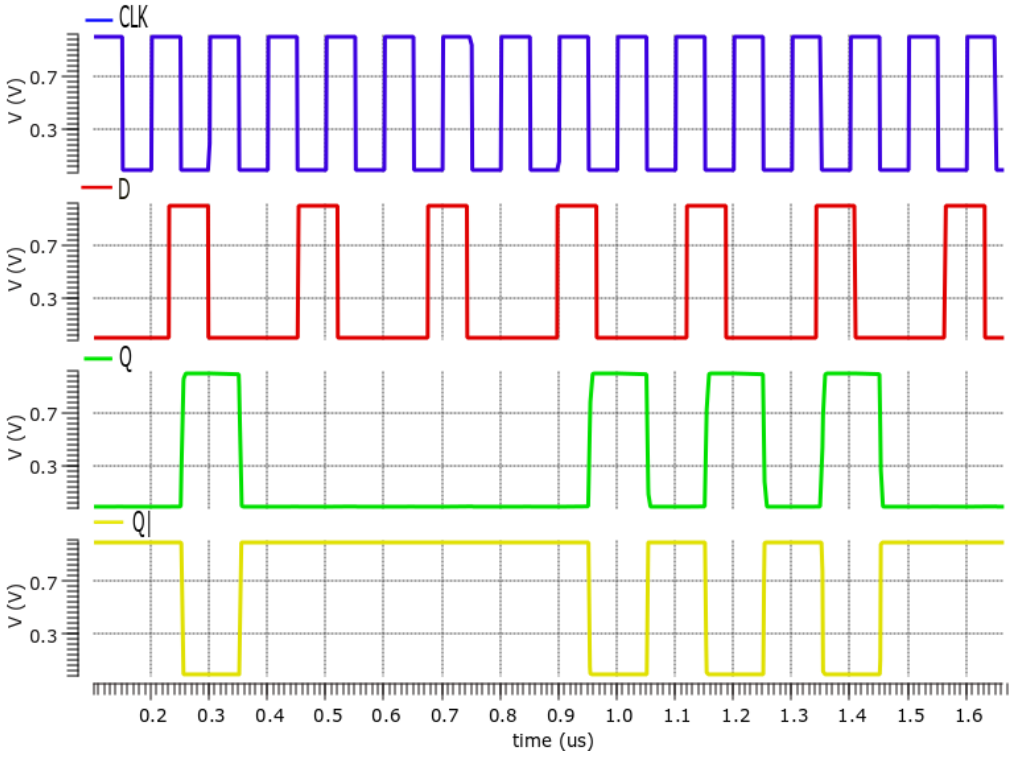


(b)

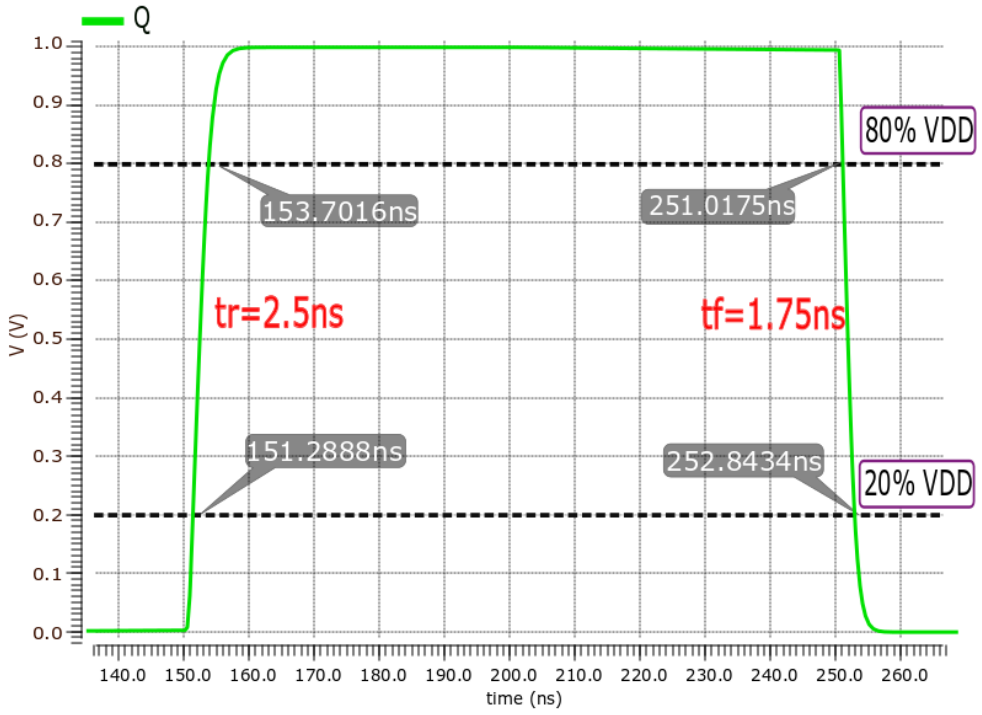
Figure 54 : D flip Flop based on dynamic C2MOS master-slave registe (a) circuit and (b) its layout

The design of the D flip flop included the circuit in Figure 54 and the integration of two inverters. The first to invert the internal clock signal and the second to invert Q output to its complement $\overline{Q}$. This allowed the circuit to have one external pad that provides a square clock at the double of the IF frequency ($f_{clk} = 2f_{If}$).

The circuit utilized PMOS transistors with a 10 µm width and 40 nm length, as well as NMOS transistors with a 5 µm width and 40 nm length, along with C_1 and C_2 capacitors of 2 pF each. The values of the capacitors were chosen carefully to optimize the performance of the D flip flop, balancing the impact on the rising and falling times of the output signal with the area used in the circuit. As a result, a rise time of 2.5 ns and a fall time of 1.75 ns were achieved, and the truth table of the D flip flop was also validated, as illustrated in Figure 55.



(a)



(b)

Figure 55 : D flip flop (a) rising and falling time(b) input and outputs responses

3.3.3.2 Frequency divider implementation

The D flip flop circuit shown in Figure 44 has been validated through transient post layout simulation. It is used to implement the circuit in Figure 52. With the post layout extraction, a test bench has proven the good functioning of the frequency divider. Hence, from an external clock with a frequency equal to $2\ f_{IF}$, two differential signals in quadrature are generated, as depicted in Figure 56. It generated four square signals Q^+, Q^-, $I^+$and I^-, where the output frequency of the four signals was reduced to half the input clock frequency. Indeed, it takes two complete clock cycles to make the output change through one cycle (OFF to ON to OFF again).

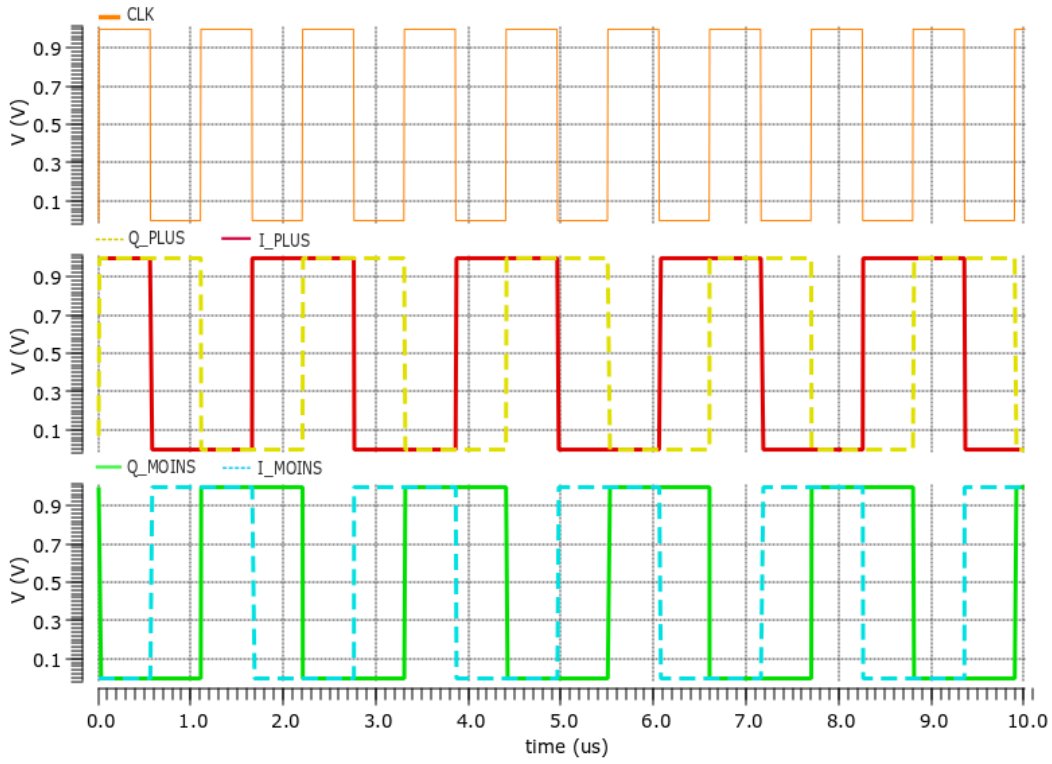


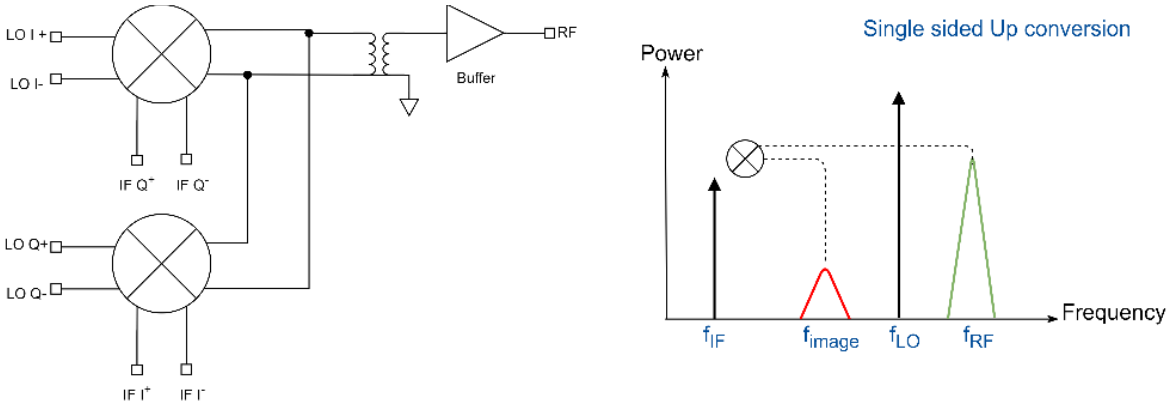
Figure 56 : Differential quadrature generation post layout transient simulation results ($f_{CLK} = 2\ f_{IF}$)

Furthermore, The IF quadrature generation does not provide the 455 KHz frequency only, the circuit provides a **wide IF quadrature frequency ranging from in [300 KHz: 600 MHz].** Hence, the if bandwidth could be selected higher than 455 KHz to minimize the IF phase noise contribution [94].

The design and validation of the IF and LO quadrature generators have been completed successfully in the previous two subsections. The next step is to design the double balanced image rejection mixer, which helps reduce aliasing at the input of the demodulator. This is achieved by suppressing the image frequency, as previously explained in 2.2.

3.3.1 DOUBLE BALANCED IMAGE REJECTION UP MIXER

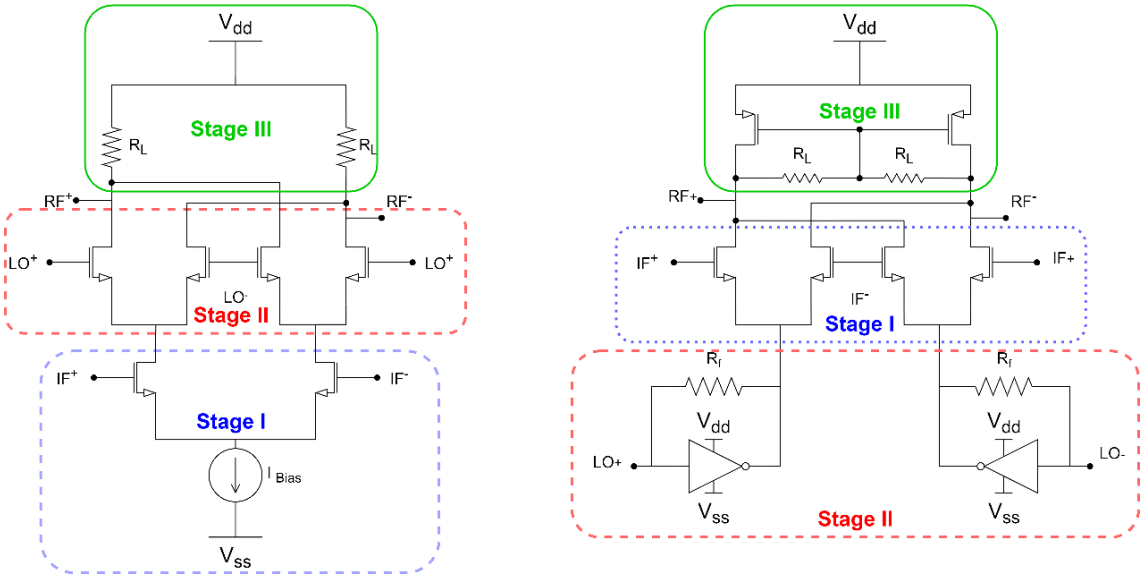
As illustrated in Figure 57, the adopted image rejection architecture consists of two double balanced mixers where, in the first mixer, the I_LO differential signal and the Q_IF signal are mixed. And the second mixer mixes the Q_LO signal and the I_IF signal. Then, both differential outputs are cross connected to eliminate the image frequency $f_{IM} = f_{lo} - f_{IF}$. Then, a conversion from differential to single ended output was needed to meet the next block "Variable Gain Amplifier (VGA)" requirement. Finally, the output was buffered to match the VGA input impedance and to peak the gain due to the 8 dB extra losses of the polyphase filter at 30 GHz (3.3.2).



(a) (b)

Figure 57 : (a) Image rejection arcitecture (b) Image rejection up conversion output spectrum representation

Considering the conventional up conversion Gilbert cell mixer's architecture, as depicted in Figure 58 (a), the double balanced mixer consists of three stages. First, a differential transconductance stage amplifies the IF signal and converts the IF voltage at the input ports into current signals for the LO switching stage. Finally, a current to voltage conversion stage is added to convert current to voltage output at RF frequency.



(a) (b)

Figure 58 : (a) Gilbert cell up conversion mixer architecture (GmSw) , (b) Proposed up conversion mixer architecture (SwGm)

This architecture presents a major challenge in terms of optimizing conversion gain while maintaining a wide bandwidth and controlling linearity and noise independently. Furthermore, its low voltage performance presents major obstacles to achieving high RF frequency operation. To highlight this challenge, the conversion gain of an up conversion mixer (CG) is expressed in (22). According to this expression, to improve the conversion gain, the bias current must increase. However, by increasing the bias current, the voltage drop across the load resistor R_L increases, which in turn reduces the voltage headroom at the output.

$$\begin{cases} CG_{GmSw} = \frac{V_{RF}}{V_{IF}} \approx \frac{2}{\pi} g_m R_L \\ g_m = \mu_n C_{ox} \frac{w}{L} (V_{gs1} - V_{th1}) \end{cases} \Rightarrow CG_{GmSw} \approx \frac{2}{\pi} \mu_n C_{ox} \frac{w}{L} (V_{gs1} - V_{th1}) R_L \quad (22)$$

- Where R_L is the load resistor, g_m is the transconductance of the Gm stage, C_{ox} the oxide capacitance of the transistor, μ_n the electron mobility.

On the other hand, the bias condition of the switching stage will change, thus deteriorating the switching action. Moreover, the supply voltage is limited to 1 V; as a consequence, increasing the bias current calls for decreasing R_L value to preserve the biasing on the switching stage, which leads to a lower conversion gain over the 30 GHz bandwidth.

Overall, the conventional Gilbert cell mixer cannot operate in the saturated region because it is difficult to obtain bias conditions and a sufficient level of voltage swing under this restricted supply voltage. Therefore, in order to improve the gain over the LO bandwidth, the transconductance and switching stage (SwGm) has been swept, as depicted in Figure 58 (b), and the conventional differential pair stage has been replaced with an inverter-based Gm stage.

In [95], both switching stages are compared, including the inverter based and common source switching stages. This study states that the current I_{LO} of the inverter based stage is two times higher than that of the single switched stage. As reported in Figure 59, with the additional transistors M_3-M_4, the circuit discharges a negative current during the negative half cycle of the input voltage. It provides an LO current of 2.5 mA compared to 1.25 mA for the conventional one. Indeed, when compared to a simple common source stage, the inverter based topology boosts the conversion gain.

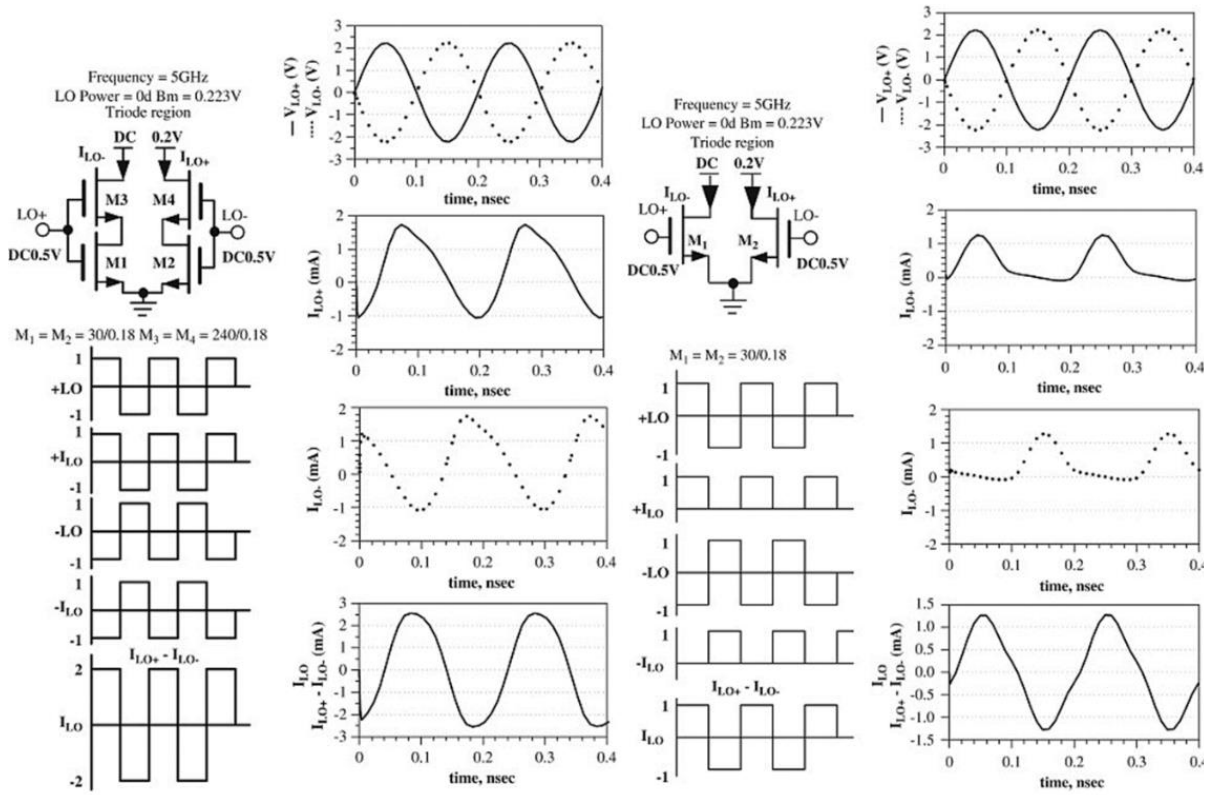


Figure 59 : Simulated switching waveforms current I_{LO}, (a) inverter based switching stage, (b) conventional switching stage

The second point is how to bias the inverter amplifier. A self-bias is generated by the feedback resistance R_f. This value was carefully chosen to set the operating point around the common-mode voltage, V_{CM} which is equal to the supply voltage,V_{DD} divided by 2.

Afterwards, in Figure 60, the architecture of the designed image rejection up conversion mixer is shown. For this circuit, the length of the inverters and PMOS loads is 40 nm, while the length of the IF stage is 56 nm. The widths are set as follows: the switching stages PMOS and NMOS are 10 µm, the IF stage is 15 µm and PMOS loads are 5 µm, with a resistive feedback resistance of 600 Ω and load resistance of 900 Ω to set the common mode voltage at $\frac{V_{dd}}{2}$. The LO stage is self-biased at 534.5 mV, and the balun output is at 467.8 mV. The overall circuit has a total consumption of 9.38 mA (including the active balun and output buffer) for a 1 V supply voltage. The circuit is designed with 45 RFSOI technology from Global Foundries. It has an active area of 60 x 35 µm² including the active balun and output buffer.

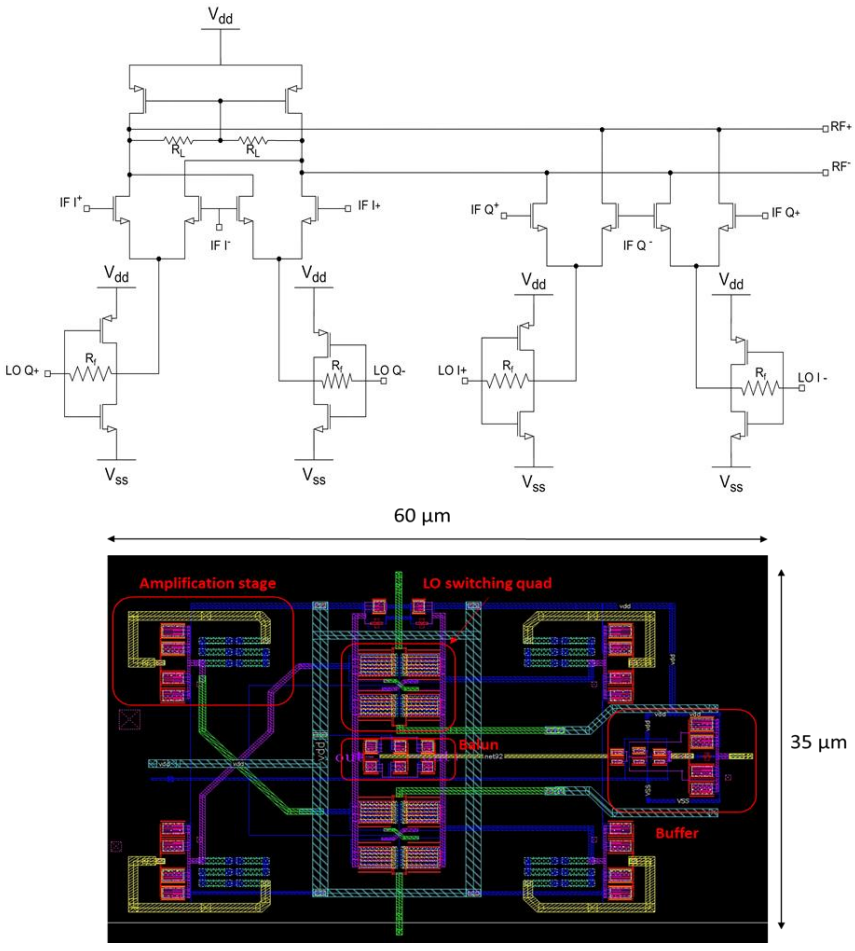


Figure 60 : image rejection up conversion mixer architecture and its layout including balun (single ended output) and output buffer

From post layout simulations, the designed up-converter mixer provides a maximum gain, including the active balun G_{max} of 18 dB $and\ G_{min,@30GHz}$ of 2.5 dB, with 3dB bandwidth $BW_{-3dB} = 10\ GHz$ as shown in Figure 61 . This gain is provided by the mixer core, which has a gain of 12 dB, and the output buffer, which has a gain of 8 dB. On the other hand, Figure 62 displays the image rejection ratio, which ranges from 45 to 75 dB across three bandwidths [200 MHz-1 GHz], [1 GHz-7 GHz], and [7 GHz-30 GHz].

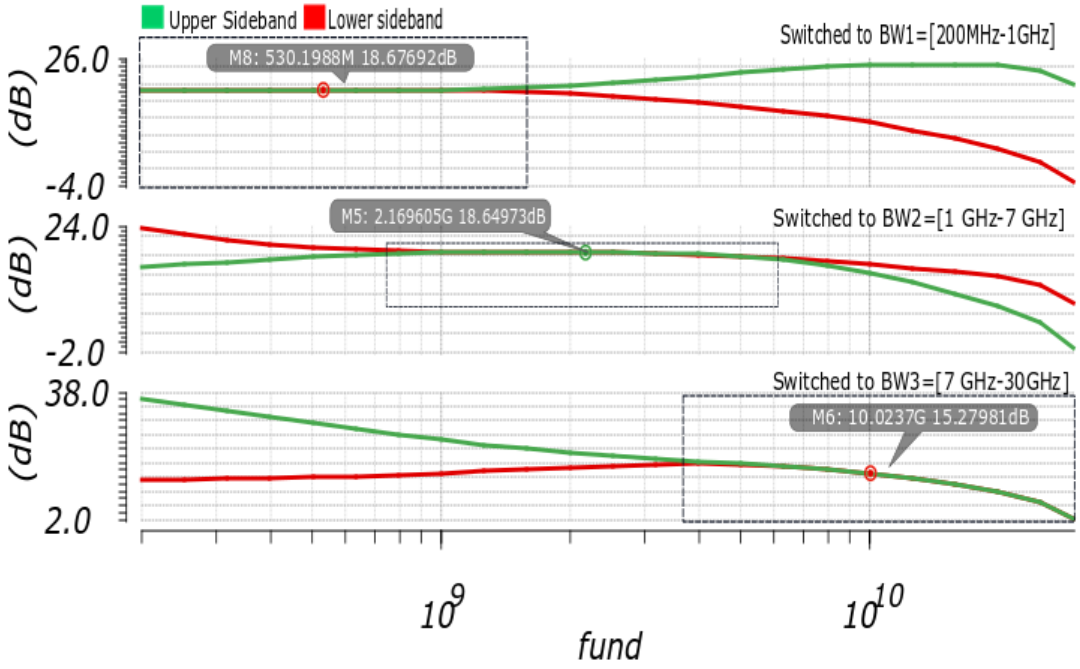


Figure 61 : Up conversion mixer conversion gain[22] from the three controlled bandwidths, I path (dashed red line), Q path (green line))

The overall specifications of the image rejection up-conversion mixer are presented in Table 7, which outlines the mixer's performance characteristics such as its image rejection level, frequency range, input and output impedance, and other relevant parameters.

[22] including active balun

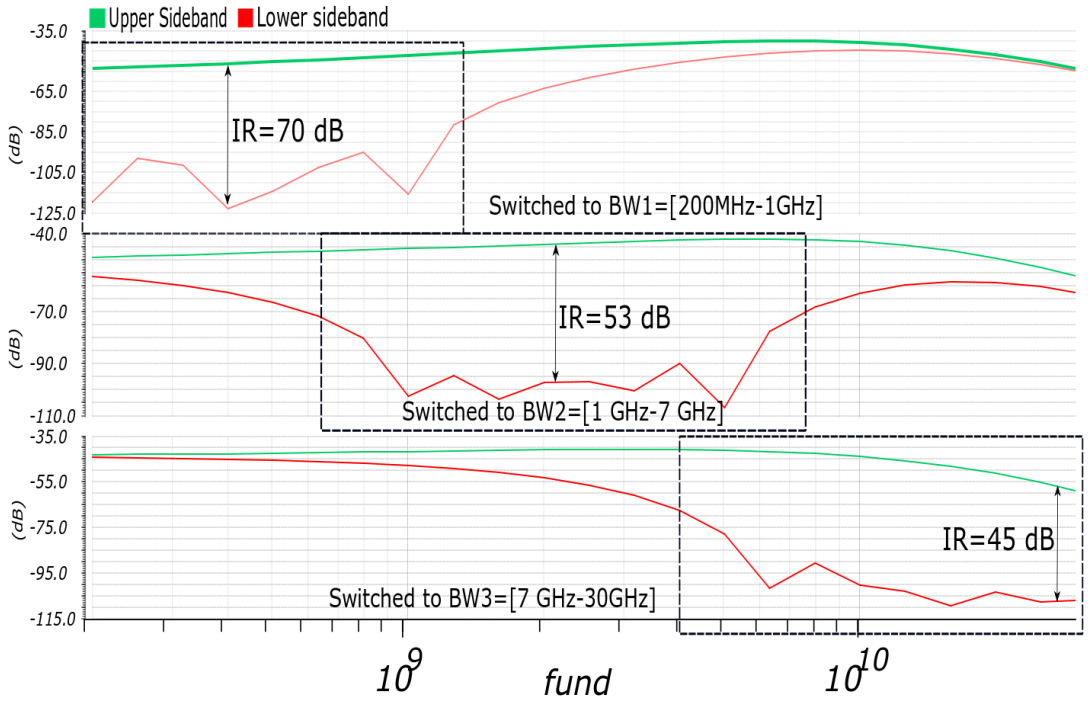


Figure 62 : Image rejection through the three bandwidths [200 MHz-1GHz] [1GHz-7GHz] and [7GHz-30GHz]

As previously noted, the implementation of the LO I/Q signal generation was carried out utilizing three stages of polyphase filters, spanning across bandwidths from 200 MHz to 30 GHz. In order to control the signals' path, the design of RF switches is deemed necessary. The design of these switches will be examined in the following. Afterwards, a test bench will be presented, on which the functionality of the entire image rejection circuitry will be assessed.

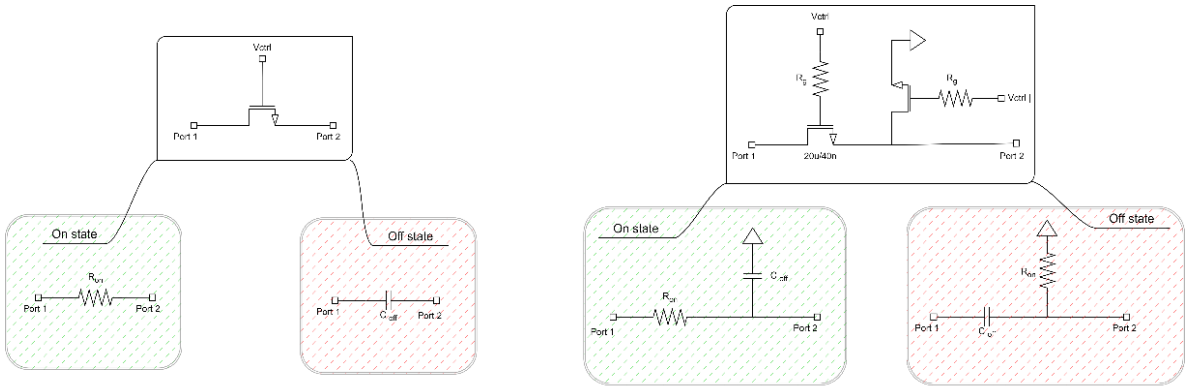
Parameter	Type	Units	Conditions/comments
Analog supply	1	V	
Power consumption	9.38	mW	Balun and buffer included
Input LO bandwidth	[0.2-30]	GHz	
Input IF bandwidth	455	KHz	
Minimum output frequency	0.2+455e-6	GHz	Signal min frequency
Maximum output frequency	30+455e-6	GHz	Signal max frequency
Input impedance	Z1		This mixer input impedance is low (S11=-5 dB) (depends on the resistive feedback).
Output impedance		High	
Voltage gain G_{max}	18	dB	Active balun included
Noise figure NF_{min}	10	dB	Balun included
Amplitude imbalance at the mixer output between I & Q	50e-3 for BW_1 , 0.55 for BW_2, 1 for BW_3	dB	Including the polyphase filter, switches and IMR mixer in the test bench

Table 7: IMR up conversion mixer specifications

3.3.2 SWITCHES DESIGN

As shown in Figure 63 (a), a switch is a two-state device that allows either the transmission in its ON state or blockage in its OFF state of an electrical signal.

One of the major drawbacks of this circuit, which only employs series transistors, is its relatively low level of isolation. This can be attributed to the C_{off} capacitance and to reduce it, more stacked transistors or smaller-size transistors can be used. Either solution increases isolation but introduces higher insertion losses. Thus, there is a conventional trade-off between the insertion loss and the isolation in a series-only configuration. To overcome this trade-off, the shunt circuit can be introduced to resolve this trade-off by grounding the RF signal, as depicted in Figure 63 (b). Indeed, in the off state, M1 is turned off and M2 is turned on, so that the switch blocks the input signal from the output node. On the other hand, in the on state, M1 is turned on and M2 is turned off, thus allowing the input signal to be delivered to the output node.



(a) (b)

Figure 63 : switch states RC model : " ON" and "OFF" (a) series circuit (b) series-shunt circuit

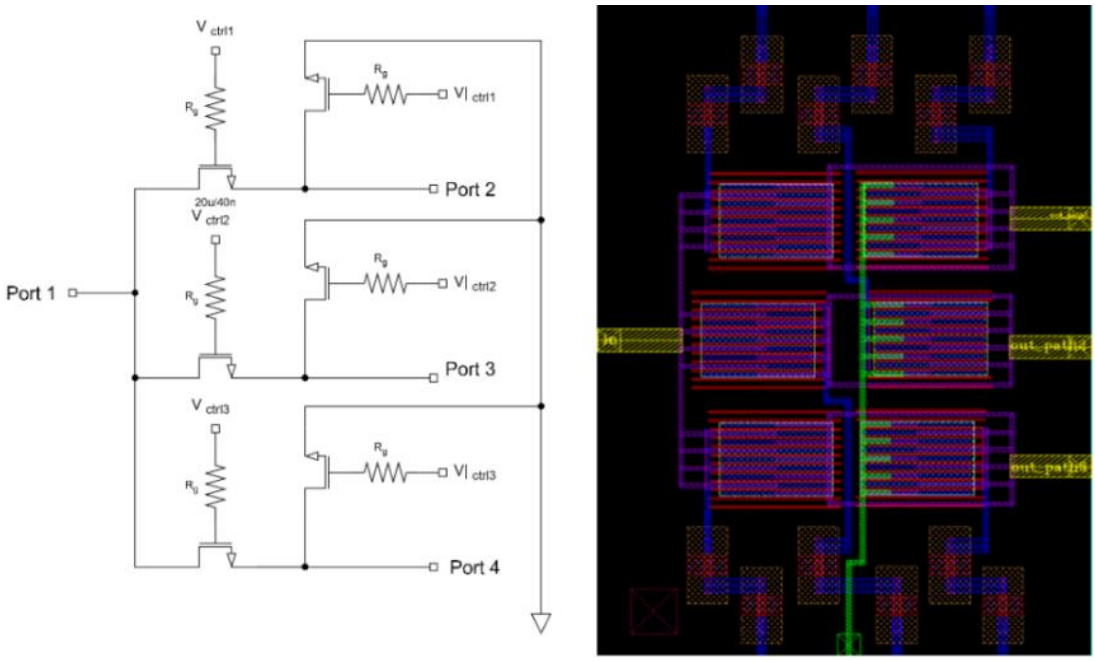
An SP3T[23]switch is required in order to selectively route the LO signal to one of the three polyphase filter stages. Hence, Figure 64 displays the schematic diagram of the designed SP3T switching network. The series shunt configuration has been chosen for this design, as each of the three paths for the switch has a series NMOS transistors paired with two stacked shunt resistors to ground, respectively.

The DC control voltages for each series transistor are labeled as V_{ctrl1}, V_{ctrl2} and V_{ctrl3}. When a given path is inactive, these voltages are raised to V_{dd}. Conversely, the shunt paths

[23] SP3T: Single Pole Three Throw (switch)

are regulated by the complements of each of the DC series voltages, these are labeled as $\overline{V_{ctrl1}}$, $\overline{V_{ctrl2}}$ and $\overline{V_{ctrl3}}$.

As shown in Figure 64, the switch network was designed with an emphasis on layout symmetry. It occupies an area of 10 x 14 µm².



(a) (b)

Figure 64 :SP3T switch (a) architecture and (b) layout covering an area of 10 µm x 14 µm

The simulation results of the post layout showed (see Figure 65) that the insertion loss was relatively flat throughout the bandwidth, with an average value of 1.3 dB. Additionally, the isolation was higher than 34 dB across the bandwidth, due to the introduction of a shunt branch and improvements in layout symmetry.

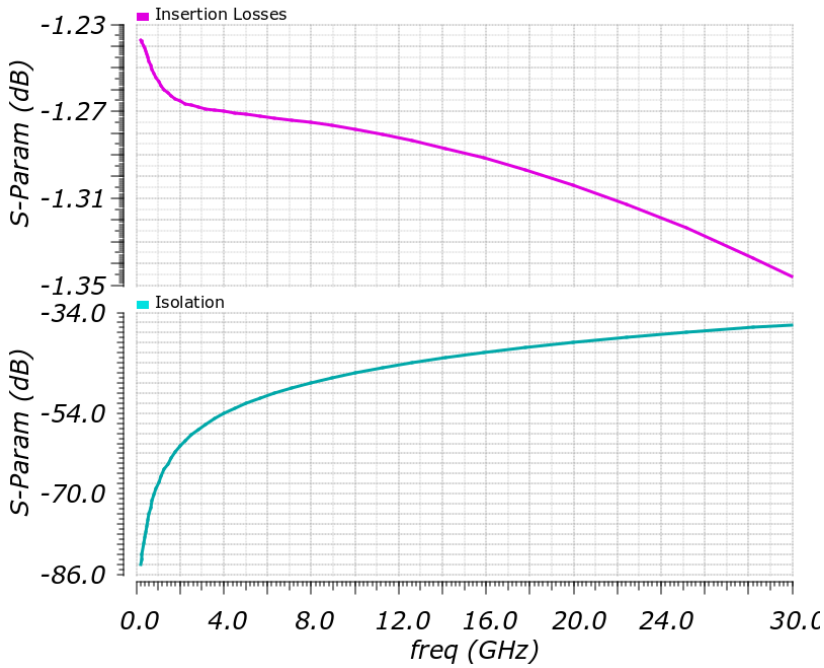


Figure 65 : Post layout simulated insertion loss and isolation of the designed SP3T

The performances are exhibited in Table 8. Now, considering all the paths starting from the LO input to the down mixer output, a test bench has been simulated after layout parasitics extraction to seek first the impact of switch isolation and the LO quadrature generator phase error and amplitude imbalance on the image rejection ratio.

Parameter	Post layout	Units	Conditions/comments
Bandwidth	DC-30	GHz	
Insertion Loss	1.3	dB	Mean value
Isolation	[-86 : -34]	dB	

Table 8: SP3T switch performance

3.3.2.1 Image rejection circuitry test bench

This part aims to evaluate the performance of the image rejection circuitry. As depicted in Figure 66, the circuitry test bench includes IF quadrature generation, LO quadrature generation, and an image rejection double balanced up conversion mixer.

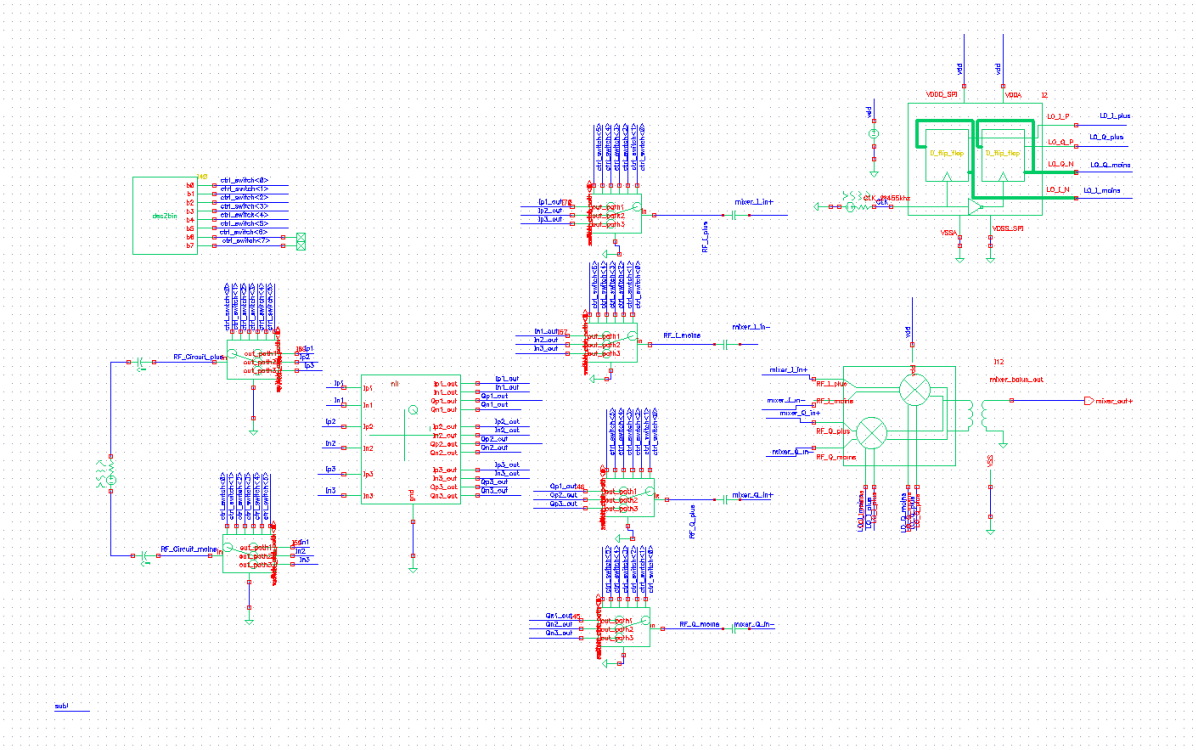


Figure 66: Image rejection Cirucitry test bench

The switches in the harmonic balance (HB) simulation test bench are controlled by an eight bit register[24] <ctrl_switch 0:8> to steer the signal to each of the three polyphase filters. The test bench includes an external clock at twice the IF frequency, along with an external LO with a power of -4 dBm, spanning frequencies from 200 MHz to 30 GHz. Eight switches monitor the three bandwidths and link the differential LO signal to the appropriate polyphase filter. They also connect the I/Q LO differential signals to the double-balanced image rejection mixer. The simulations were performed for three different bandwidths controlled by the switches, while keeping all other system parameters constant, as summarized in Table 9.

[24] it will be monitored by the SPI in the complete VNA circuit.

Parameter	Type	Conditions/comments
Z_{in}	100 Ω	Pseudo differential input
P_{in}	-4 dBm	
f_{LO}	@15 GHZ for BW3 @5 GHz for BW2 @500 MHz for BW1	BW1=[200MHz-1 GHz] BW2=[1 GHz-7 GHz] BW3=[7 GHz-30 GHz]
f_{CLK}	$2\,f_{IF}$	
dec_switch <0:8>	26 for BW3 38 for BW2 41 for BW1	Decimal to binary conversion block. It provides ctrl_switch <0:8>. In the printed system, this register is provided by a SPI.

Table 9: HB simulations configuration for the image rejection circuitry @500 MHz, @5GHz and @15 GHz

The following paragraphs provide an overview of the post layout simulations:

For f_{LO} within the bandwidth of 200 MHz to 1 GHz, Figure 67 shows the conversion gain of each block, including the insertion loss (IL) of polyphase input switches, the polyphase conversion gain for I/Q signals, the insertion loss of polyphase output switches, and finally the mixer conversion gain (CG) for both I and Q signals, which in the worst case has 1 dB IL, 32 IL, 1.1 IL, and 18 dB conversion gain, respectively. The high insertion loss is due to the 10 pF AC coupling capacitor, which couldn't be increased due to surface area constraints and DRC density issues. All other blocks have similar performance when tested individually. The chain provides a mean image rejection of 70 dB over BW1, Figure 70.

Similarly, for the f_{LO} frequency range of 1-7 GHz (BW2), Figure 68 illustrates the conversion gain of each component in the signal chain, including the polyphase input switches, polyphase conversion gain for In-phase and quadrature signals, polyphase output switch insertion loss, and mixer conversion gain for both I and Q signals. The worst case insertion loss (passive elements) and gain (active elements) values for each component are 1 dB IL, 25.5 dB

IL, 1.1 dB IL, and 18 dB conversion gain, respectively. The mean image rejection of the signal chain is 65 dB for BW2, as depicted in Figure 70.

Finally, for the third LO frequency bandwidth, ranging from 7 GHz to 30 GHz, Figure 68 illustrates the conversion gain of each component in the signal chain. The worst case insertion loss / gain values for each component are 1.2 dB IL, -23 dB IL, 1.15 dB IL, and 2 dB conversion gain for the polyphase input switches, polyphase conversion gain for In-phase and quadrature signals, polyphase output switch insertion loss, and mixer conversion gain for both I and Q signals, respectively. The mean image rejection of the signal chain is 44 dB for BW3, as depicted in Figure 70.

A comparison was conducted between the results obtained from the simulations of the image circuit and simulations run on a stand-alone basis. The results of this comparison are presented in Table 10 and are intended to ensure that the simulations accurately reflect the system's behavior and to identify any discrepancies that need to be addressed. Thereby helping to pinpoint potential areas for improvement.

Indeed, the table shows insertion losses of 32 dB at 200 MH compared to a 12 dB IL in a standalone configuration. As stated previously, this is due to the AC coupling capacitor of 10 pF (due to the restricted circuit surface) between PPF output switches and the IMR up conversion mixer. To minimize losses associated with AC coupling at 200 MHz, adding a parallel capacitance equal in value to the existing capacitor (10 pF) could be done in the future. At the upper frequency, to counter the insertion losses at 30 GHz, active peaking was added to the mixer output after the balun, which results in a 2 dB total voltage conversion gain at 30 GHz.

Parameter (in dB)		In the IMR circuitry			Standalone configuration			Conditions/comments		
		BW1	BW2	BW3	BW1	BW2	BW3	BW1	BW2	BW3
Input switch IL	Worst Case values	0.1	0.5	1.2	1.2	1.27	1.34	@1GHz	@7GHz	@30GHz
PPF IL		32	25.25	23	12	16	22	@200MHz	@1GHz	@30GHz
Output switch IL		1.9	1.95	1.96	1.7	2	2.3	@1 GHz	@7GHz	@30GHz
mixer+ balun CG		18.5	18	2	18.7	18	2.5	@1GHz	@7GHz	@30GHz
Image rejection	Mean Value	55	46.5	40	60	58	46	The image rejection decreases due to PPF phase error between I and Q outputs		

Table 10: Comparison between each block worst case IL/ CG in the IMR chain Vs standalone configuration post layout simulations

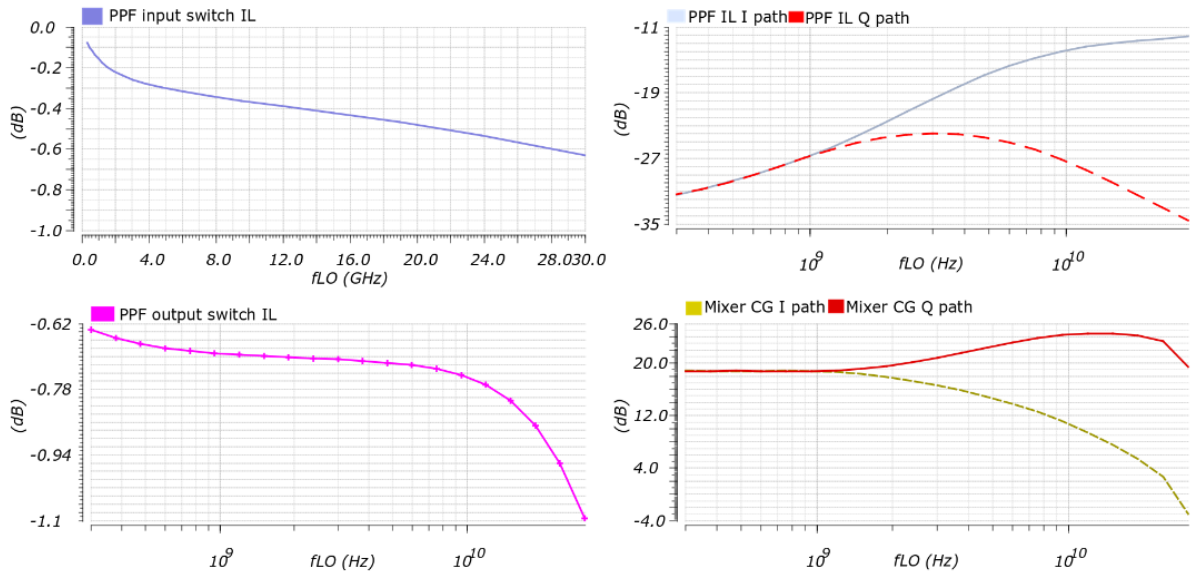


Figure 67 : Image rejection circuitry conversion gain Flo ∈ BW1.

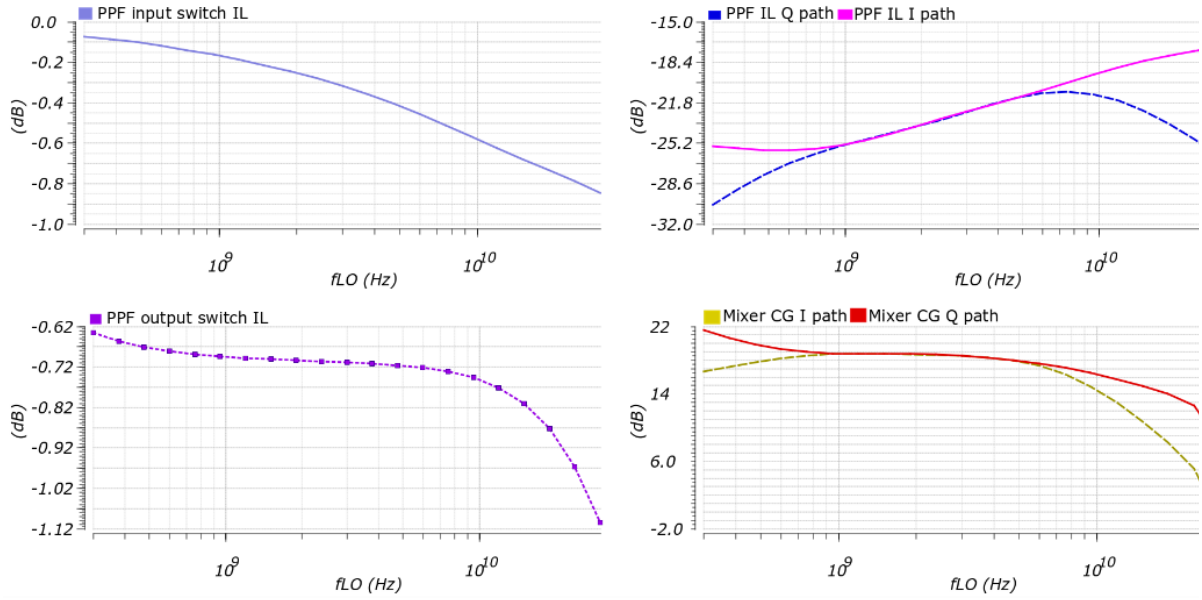


Figure 68: Image rejection circuitry conversion gain Flo ∈ BW2

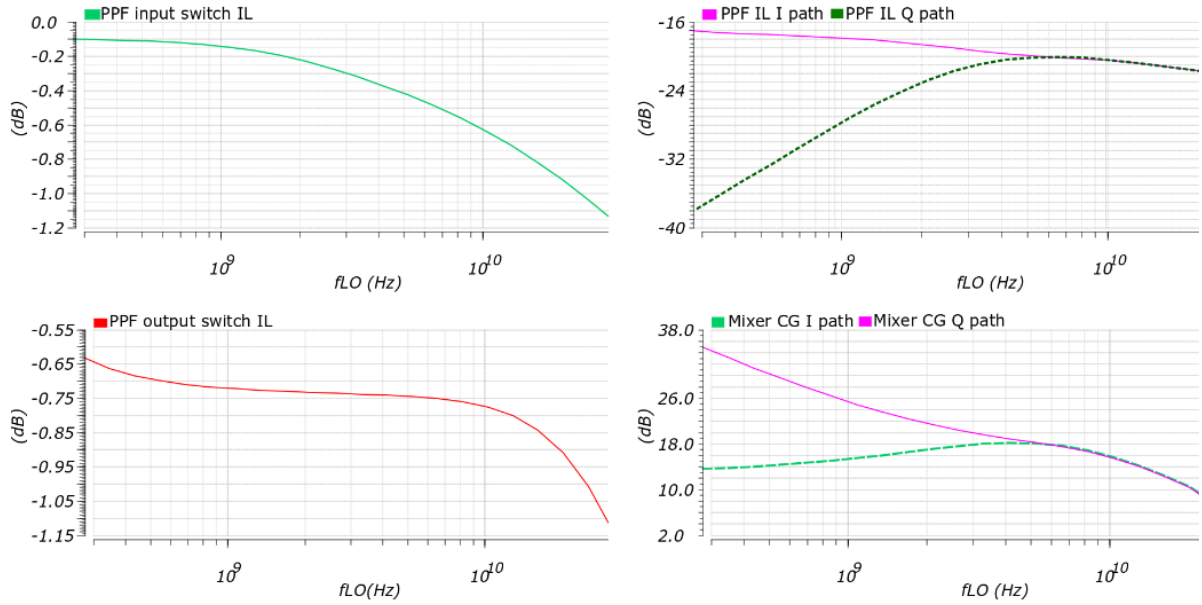


Figure 69 : Image rejection circuitry conversion gain Flo ∈ BW3

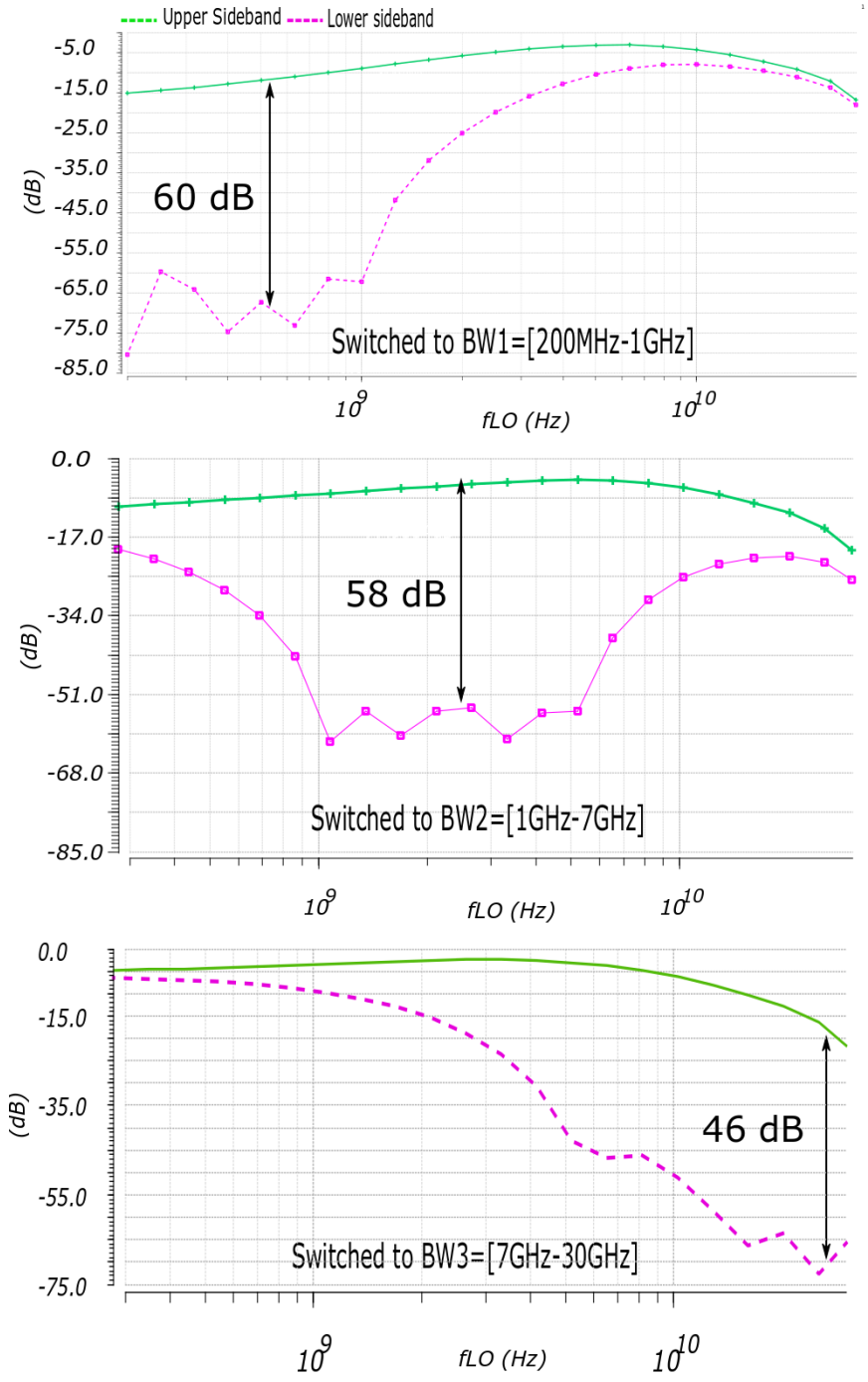


Figure 70 : Global Image rejection circuitry conversion gain and image rejection, Flo ∈ BW1=[200 MHz,1 GHz], Flo ∈ BW2=[1 GHz,7 GHz], Flo ∈ BW3=[7 GHz ,30 GHz]

Up to this point, the image rejection circuitry has been designed and simulated using post layout extractions. The next section tackles another key element in the transmitter and receiver parts. It includes the variable gain amplifier that tunes the port 1 output power to deliver between -10 dBm and 0 dBm and the low noise amplifier situated at the second port receiver to amplify the attenuated signal passing through the device under test.

3.4 GAIN CONTROL CIRCUITRY

This section presents, in the first part, the wideband inductorless low-noise amplifier, which is located at the input of the transmission path receiver. As explained in the system budget study (2.2), this cell boosts the signal weakened by the DUT insertion losses up to 70 dB, so it can be detected at the demodulator input. This circuit has been validated by measurements made in a standalone configuration.

In the second part, the variable gain amplifier is presented. This circuit used, within its gain stage, the same architecture as the inductorless amplifier, adding input and output buffers, tuning the transistor dimensions and feedback resistance values to reach the expected gain of 23 dB. This gain enables the emission of a maximum power of 0 dBm at port 1 (Figure 31).

3.4.1 WIDEBAND INDUCTORLESS LOW NOISE AMPLIFIER

As presented in Figure 71, the main blocks of the proposed circuit are the inverter based and cherry Hooper amplifiers in an interleaving feedback topology. Considering the "Cherry Hooper amplifier", it consists of a two stage circuit including a transconductance stage followed by a transimpedance stage. The second stage local feedback, through the feedback resistance R_1, raises the output pole frequencies by decreasing the output impedance of the second stage compared to a common source amplifier, as demonstrated in [96]. In addition, the feedback inverter acts as an active peaking device allowing for a higher frequency bandwidth response. Followed by two self-biased inverters, the first to improve gain and the second to drive a 50 Ω load.

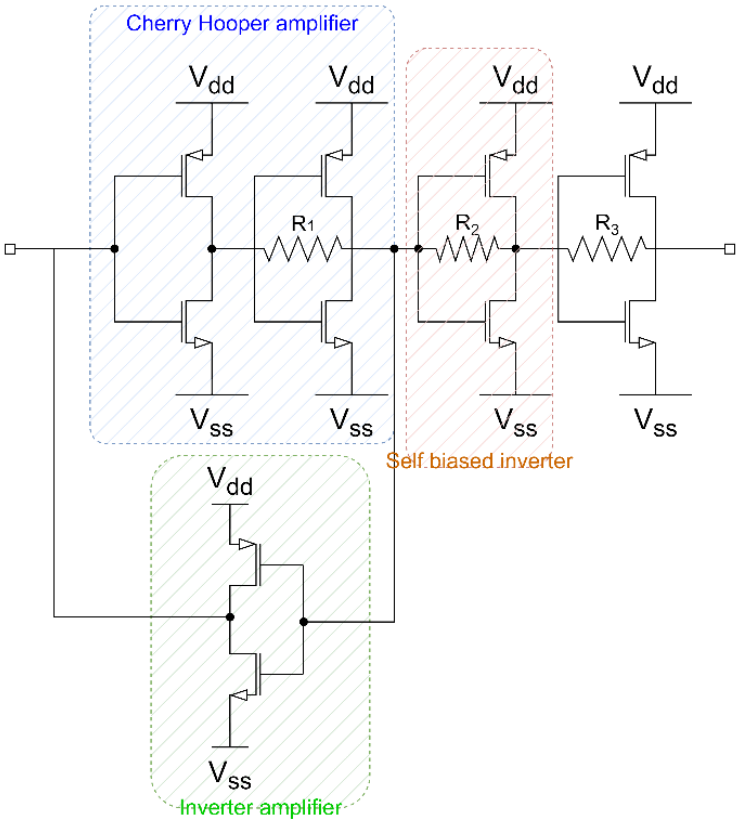
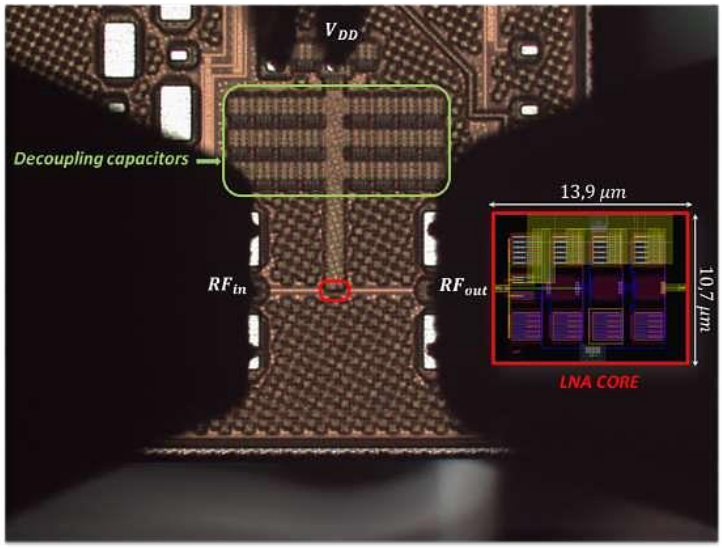


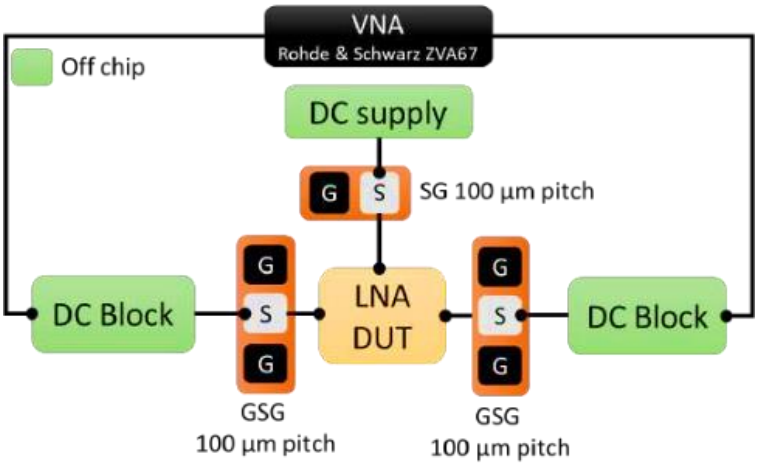
Figure 71 : Proposed low noise inductorless amplifier

This circuit transistor's sizing is based on ($\frac{g_m}{i_d}$) principle[25] [97]. Where, the $\frac{g_m}{i_d}$ versus the normalized drain current $\frac{I_D}{\left(\frac{W}{L}\right)}$ was simulated for NMOS transistor of the adopted 45RFSOI technology. A $\frac{g_m}{i_d} = 7$ was the tradeoff value for the targeted gain and power consumption. It implies a gm value of 16 mS and a drain current of 2.3 mA. The transistor's width is equal to 20 µm and its length is 40 nm. Except for the feedback inverter, where the width was chosen to be small enough to extend the bandwidth while maintaining the circuit stability. The feedback transistor's dimension is equal to $\frac{W}{L} = \frac{3\ \mu m}{40\ nm}$. The feedback resistor R_1 is equal to 400 Ω, it controls the circuit gain as well as the input biasing value at 500 mV and the input return loss. R_2 is optimized to boost gain (1 kΩ) and R_3 to get the minimum output return loss (400Ω).

[25] g_m: transistor transconductance, $i_d$drain current, W: transistor's width, L: transistor's length



(a)



(b)

Figure 72 : (a) Llow noise inductorless micropgraph and (b) measurement setup

The die micrograph of the amplifier with probes is shown in Figure 72 (a). As highlighted in the photograph, since no inductive components are introduced, chip area is greatly saved and integration is improved. The total area is only 13.9 µm x 10.7 µm. The proposed amplifier draws 7.9 mA from a 1 V supply, consuming a total power of only 7.9 mW. As illustrated in Figure 72 (b), the test setup uses a Rohde & Schwarz VNA ZV167 to measure scattering parameters and noise figure, with two DC blocks at the input and output of the circuit to block the DC common voltages. The following paragraphs elaborate on the measurement and simulation results in a typical configuration at 25°C.

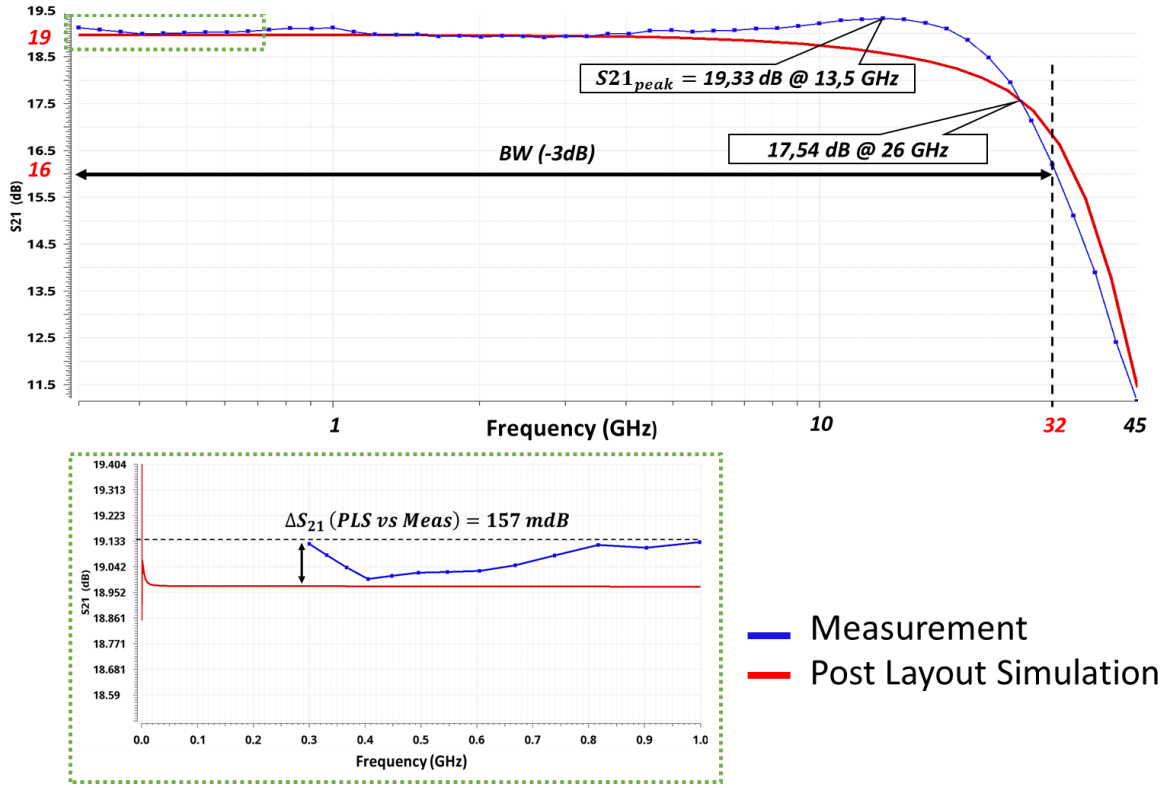
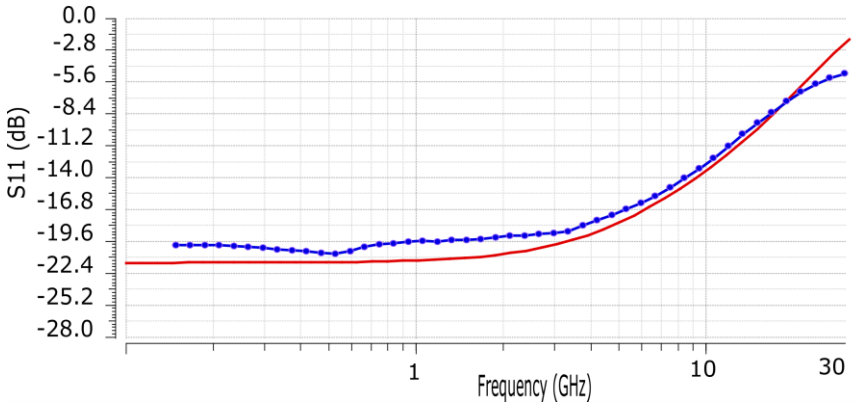
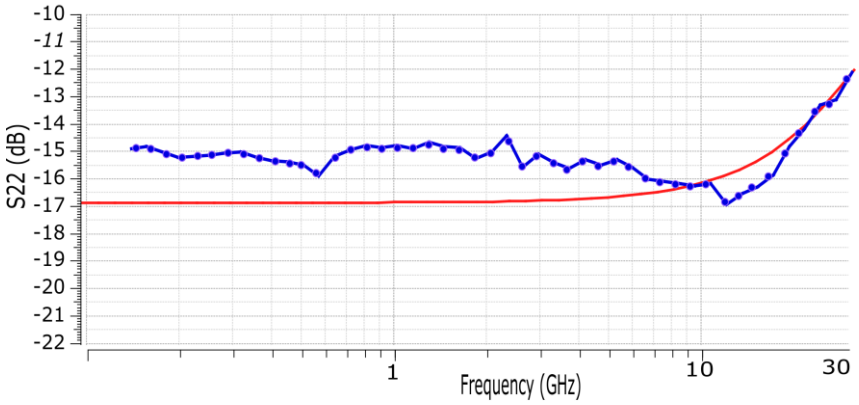


Figure 73 : Measured (blue dotted line) and simulated gain (red dashed line) and zoom on DC to 3 GHz frequency bandwidth

Regarding the measurement results, the amplifier achieves a flat gain of 19 dB within a -3 dB bandwidth of 32 GHz, Figure 73 (a). The measurement frequency started at 300 MHz due to the input DC blocking capacitance frequency limitation. However, since the measurements agree by ± 0.5 dB with the post layout simulations, we assume that the measurements can be extrapolated for frequencies below 300 MHz, Figure 73 (b).



(a)



(b)

Figure 74 : Input and output impedance measurement (dotted blue) vs post layout simulation (red line)

In the Figure 74, the current reuse stage, in charge of input matching, achieves a good input return loss of less than 8 dB from DC to 18 GHz. In addition, output matching is also ensured by a low S22 less than 12 dB from DC to 30 GHz.

The simulated noise figure is around 5 dB over the 24 GHz bandwidth. However, as illustrated in Figure 75, there is a mean value of 1 dB increase in the actual NF measurement compared to the post-layout simulation test bench results, which include the pads, transmission lines, and core circuits. The difference may be attributed to the use of transmission lines at the input and output of the circuits during probe placement, which are not accounted for in the first-order model used in post-layout simulations and may be affected by the metal conductivity skin effect. Another possible explanation is the added noise from the preamplifier used in the setup.

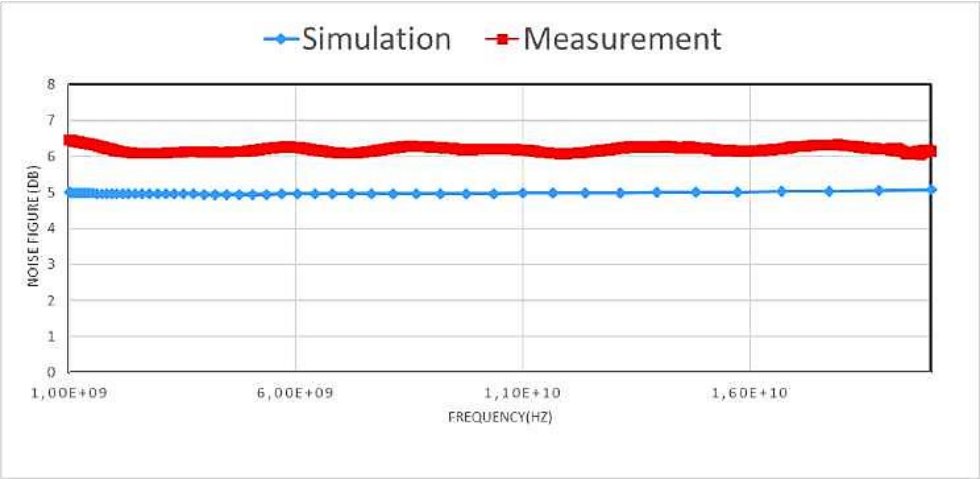


Figure 75 : Noise Figure comparison between simulation and measurement versus frequency

The noise figure is relatively low considering the frequency bandwidth, and both noise and gain remain constant across the entire bandwidth, resulting in a constant signal to noise ratio. Otherwise, the other measured parameters are consistent with the post layout simulations. The -3dB bandwidth is widely covered as well as the input matching that meets -10 dB of return loss up to 24 GHz. Compared to the state of the art (Table 11), this circuit provides a promising figure of merits taking into consideration the very compact core area $FOM2(\frac{GHz}{mm^2})$ and low noise consumption $FOM1(\frac{GHz}{mW})$ (23).

The next circuit, “Variable Gain amplifier” uses this circuit core architecture, since the results of the measurements were consistent with the simulations. However, to meet the specifications for the variable gain amplifier, extra stages will be added to the existing core circuit. In the following section, this process will be explored in more detail.

$$FOM1(\frac{GHz}{mW}) = 20log\left[\frac{Gain(lin) * BW(GHz)}{(NFmin(lin) - 1) * Pdc(mW)}\right]$$
$$FOM2(\frac{GHz}{mm^2}) = 20\log\left[\frac{Gain(lin) * BW(GHz) * IIP3(mW)}{(NFmin(lin) - 1) * Pdc(mW) * area(mm^2)}\right] \quad (23)$$

	Wideband amplifier with inductances						Inductorless Architectures					
	[98]	[99, p.]	[100]	[101]	[102]	[68]	[103]	[104]	[105]	[96]		**This work**
Technology	40-nm CMOS	90- nm CMOS	130-nm CMOS	65-nm CMOS	90 nm CMOS	0.35- µm SiGe	65 nm CMOS	130-nm SOI CMOS	65 nm CMOS		180 nm CMOS	90 nm CMOS	**45RFSOI**
Frequency (GHz)	1 - 11 GHz	DC-22.1	DC - 11,5 GHz	1-20GHz	0,1-20 GHz	2-32 GHz	0,1-10	0,5-5,6	DC-10	DC-5,2	0,1-4,9	0,1-6,8	**DC-30GHz**
S21-max (dB)	17	10,7	13,2	12,8	12,7	10	16	21,1	10,5	10,7	19,3	18	**18**
3dB Bandwidth (GHz)	10	22	11,5	19	20	30	9,9	5,1	10	5,2	4,8	6,7	**30**
NF(dB)	3,5	4,3	5,6	3,3	4,4	3,7	4,9	3,63	2,7	2,9	3,5	3	**5,8**
Voltage supply (V)	1,2	1,2	1,3	1,6	1,2	3,3	1,2	1,5	1	1	1,8	1	**1**
Pdc (mW)	9	8,4	9,1	20,3	12,6	85,8	6,3	15,2	13,7	7	30,6	14,5	**7,9**
IIP3 (dBm)	-2,8	-2,67	-12	5,8	-2,5	–	-6	-4,9	-3,5	-6	-14	-12	-13.1
Core size (mm^2)	0,061	0,017	0,08	0,096	0,12	–	0,004	0,031	0,02	0,03	0,0067	0,0032	0,000149
FOM 1 (GHz/mW)	16,05	14,49	6,83	11,1	11,83	-1,69	13,52	9,29	9,05	8,56	1,35	11,33	20,64
FOM 2 (GHz/mm^2)	34,74	44,54	4,76	43,05	25,24	–	49,48	29,66	36,03	27,02	16,82	37,23	70.91

Table 11: Wideband low noise amplifier FOM comparison for the state of the art references

3.4.2 VARIABLE GAIN AMPLIFIER DESIGN

In the design of the VGA circuit, two key stages were considered: the attenuation stage and the amplification stage. Starting with the attenuation stage, it was determined that a 5-bit digital variable gain attenuator with a 15 dB dynamic range was necessary in order to achieve the specified output power range [-10: 0] dBm.

Parameter	Type	Conditions/comments
Z_{in}	high	mixer output buffer output impedance
Z_{out}	50 Ω	To meet the coupler characteristic impedance
BW_{-3dB}	[200MHz+FIF: 30 GHz+ FIF]	With F_{IF}=455 KHz
$Gain_{min,max}$	[8:23] dB	As set in the last chapter from the budget study to provide a power [-10 dBm: 0 dBm] at the first port

Table 12: VGA specifications

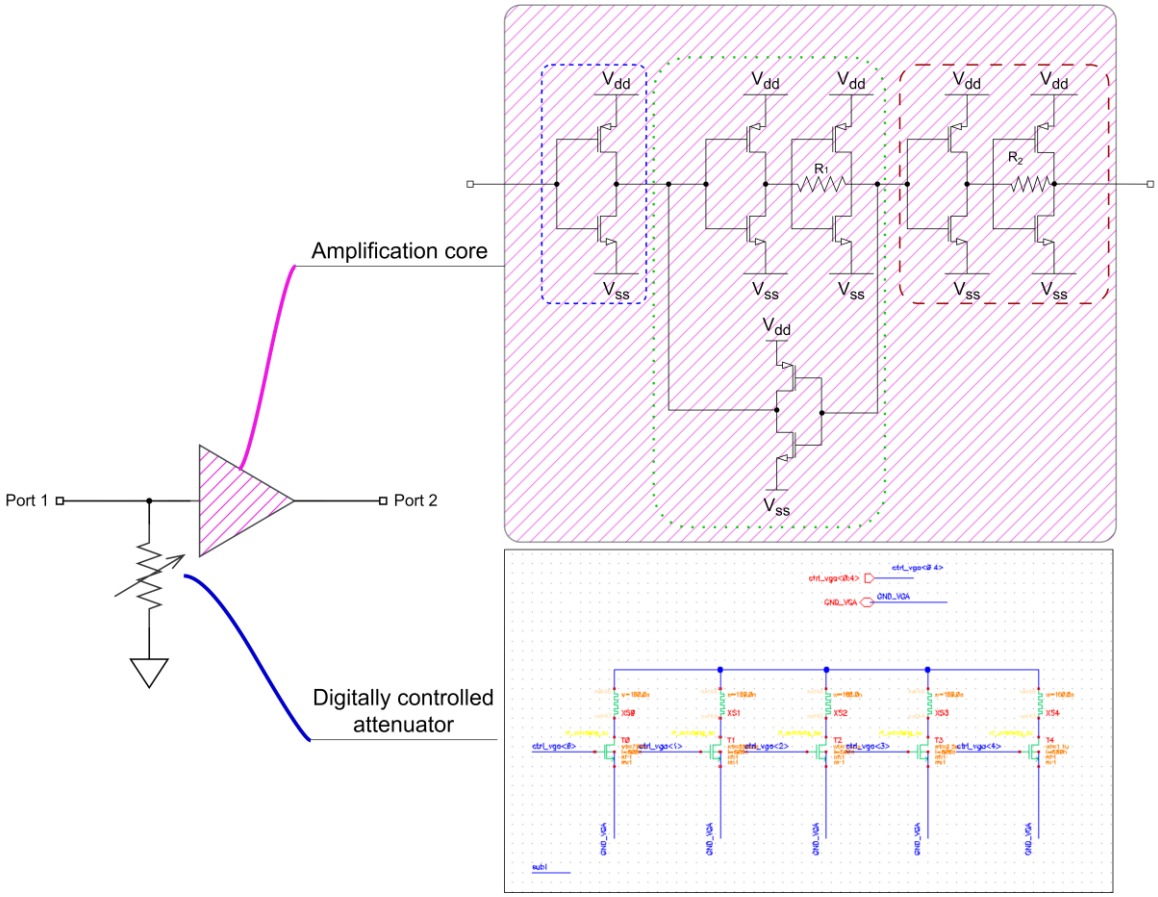


Figure 76 : Variable gain amplifier including amplification core and input attenuator

To accomplish this, NMOS transistors were used as shunt devices and the attenuation gains were analyzed utilizing different transistor ratios (W/L). As a result of this analysis, a specific drain to source resistance R_{ds}(on) was chosen for each stage transistor ratio in order to achieve the targeted attenuation steps. The dimensioning of the attenuator was conducted taking into consideration both the previous bloc (output mixer amplifier) and the amplification bloc. The second block is the amplification stage. It was designed using the previously designed Cherry Hooper bloc in conjunction with inverter feedback, based on good matching between measurement and simulation results from the fabricated low noise amplifier, as presented in Figure 76.

The addition of an input buffer is necessary to ensure that the VGA specifications (Table 12) in terms of input impedance match the impedance of the output mixer amplifier. The input buffer consists of an NMOS PMOS push-pull configuration and is biased by the common voltage of the output mixer amplifier. This VGA output buffer was designed to reduce the output return loss, allowing for a more stable operation. The common voltage of the output mixer amplifier was around 450 mV, providing an adequate level of biasing for the buffer.

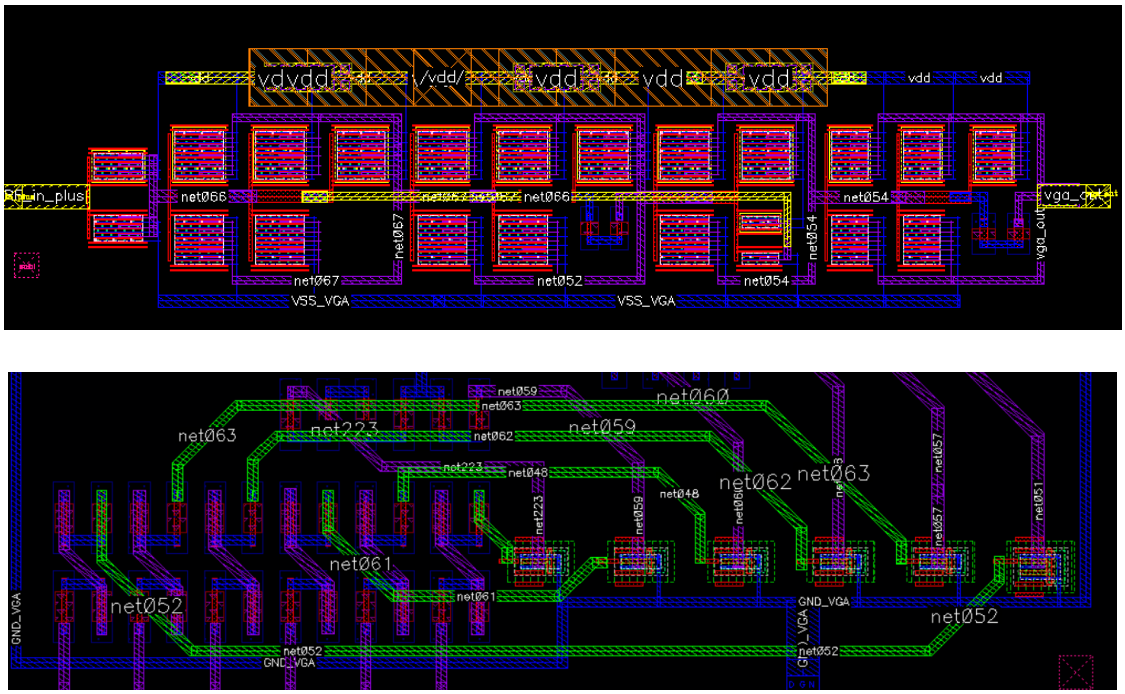


Figure 77 : Top: amplification bloc, bottom: attenuation bloc

The inductorless VGA was fabricated using 45 RFSOI technology with a single supply of 1V. The layout of the proposed VGA circuit is illustrated in Figure 77, which has a total area of

45 µm x 10 µm. The maximum power consumption of the variable gain amplifier, when operated at a 1 V supply voltage, is 26 mA. Simulating the post layout, the voltage gain was achieved at its highest of 23 dB, with an adjustable range of 8 dB. This range provided a wide -3 dB bandwidth of 28 GHz, as shown in Figure 78.

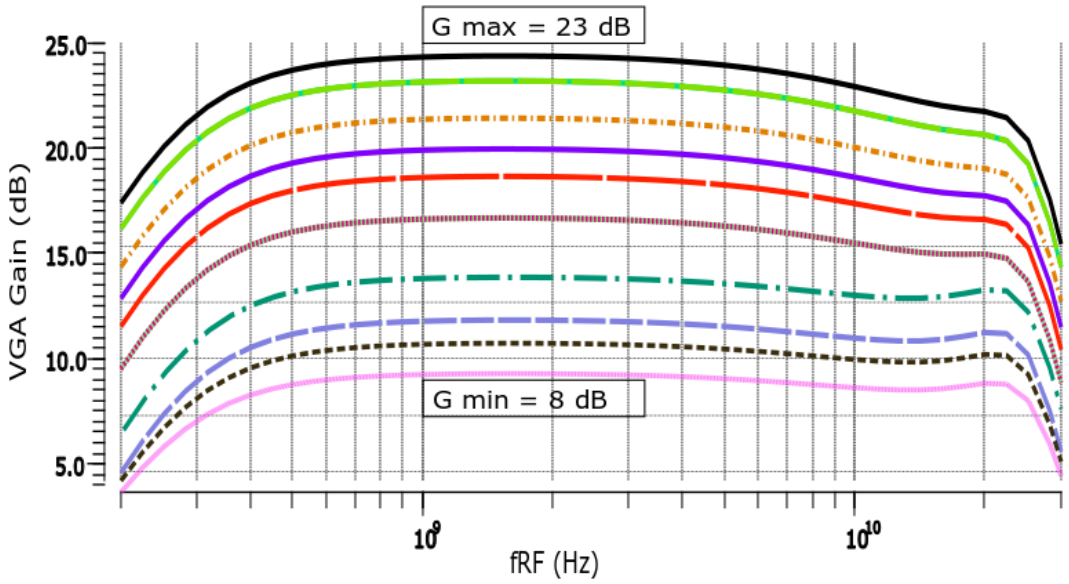


Figure 78 : VGA digitally controlled gain simulation results

Considering the VGA power specification, as mentioned earlier, the 23 dB gain is the targeted maximum gain to provide 0 dBm at port I output at 30 GHz. Since the attenuator was designed to meet the mixer buffer output impedance, the VGA will not be characterized in terms of power gain in a standalone configuration. Rather, it will be simulated with the complete IMR and directional circuitry, as detailed in the next section.

3.4.3 GAIN CIRCUITRY TEST BENCH

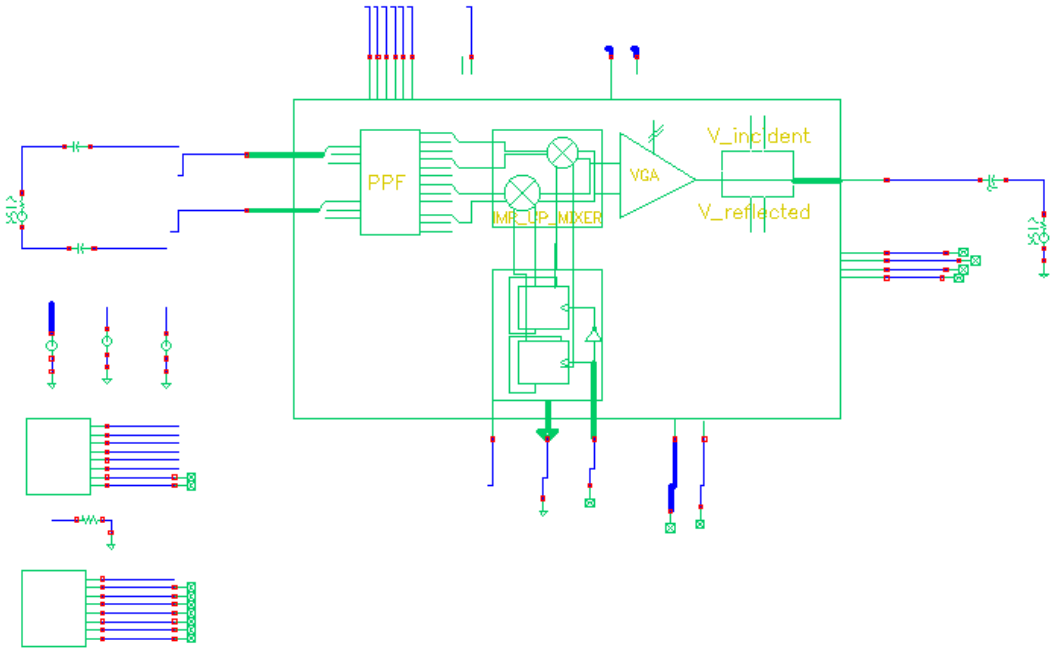


Figure 79 : gain circuitry test bench

The harmonic balance and S parameters simulation test bench includes an IF frequency generator at 500 kHz instead of 455 kHz. This deviation does not impact the circuits' performance[26] and it facilitates the convergence of harmonic balance simulation; the IF frequency must divide the LO frequency. An external LO with -4 dBm power sweeping the frequency over 200 MHz to 30 GHz is used. The switches control the three bandwidths to provide an LO quadrature signal to the double-balanced image rejection mixer. The mixer output buffer is then connected to the variable gain amplifier that drives the directional coupler, terminated on a 50 Ω port (port 1). All the blocks used are simulated with their Calibre extracted layout parasitics (C+CC) and the output is loaded with a 50 Ω load.

[26] This was checked for each block through HB and transient simulation based on Calibre extraction.

Parameter	Type	Conditions/comments
Z_{in}	100 Ω	Pseudo differential
Z_{out}	50 Ω	Single ended
V_{in}	200 mV	-10 dBm input power referring to Zin
f_{LO}	[200 MHz – 30 GHz]	
f_{IF}	500 KHz	Instead of 455 KHz for HB simulation convergence

Table 13: HB and S parameters simulations configuration for the image rejection circuitry @500 MHz, @5GHz and @15 GHz

In order to verify the output power specification, simulations of the transmitter path were performed, yielding an output power of 0 dBm up to 28 GHz with effective rejection of the image frequency (BW3 in the provided simulation), as depicted in Figure 80. It should be noted that the mixer output buffer was modified introducing some peaking the bandwidth to extend the bandwidth at high frequencies (25 GHz) to compensate the image rejection circuitry insertion losses at 30 GHz (inverter based peaking), as shown in the S21 scattering parameter results (Figure 81). The transmitter input referred third order intercept point IP3 is equal to 13.08 dBm, and the 1 dB compression point (P1dB) is equal to 2.73 dBm.

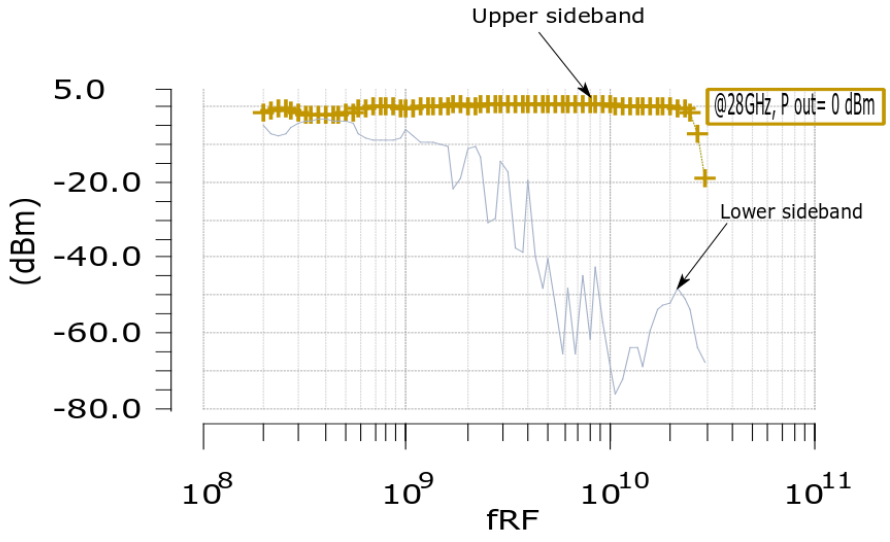


Figure 80 : Port 1 output power and image rejection (harmonic balance simulation)

Finally, the impedance matching of the transmitter circuitry was also evaluated. The transmission chain was found to have a 50 Ω match for the pseudo-differential input and single-ended output, Figure 81 . It shows a good input output return loss less than 10 dB over the 30GHz bandwidth. Impedance matching helps to minimize reflections and maximizes the coupler directivity.

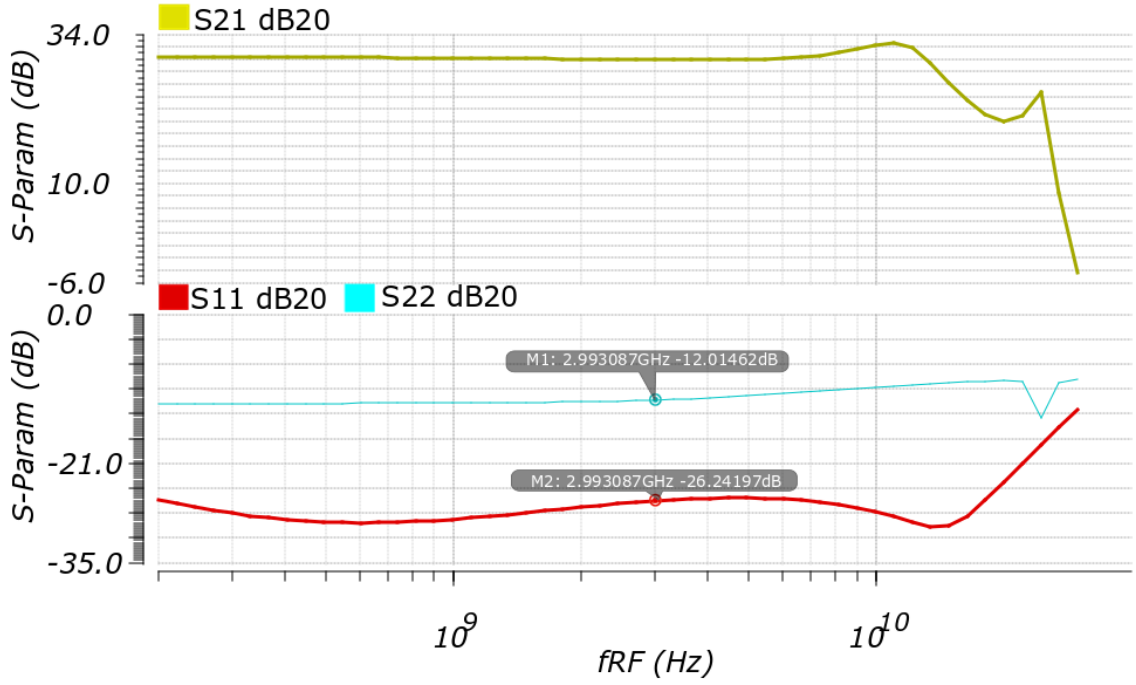


Figure 81 : Scattering parameters simulation results including transmitter gain chain, input and output return loss in dB

Overall, the gain circuitry has been validated to meet the established primary parameters, providing a minimum gain of 23 dB, a maximum input power of 0 dBm, and a 50 Ω match for the pseudo-differential input and single-ended output. These results demonstrate that the VGA is suitable for use in this VNA circuit and can provide high-quality amplification.

The next section presents the passive mixer first receivers that treat the three signals: the incident, reflected and transmitted signals, before feeding the magnitude and phase demodulator.

3.5 RECEIVER'S CIRCUITRY

As described in the second chapter (2.2.1), the $f_{RF} = f_{LO} + f_{IF}$ signal is generated by the image rejection up conversion mixer in the transmit path. In the receivers path, this signal is down converted with the LO frequency f_{lo} via a passive mixer to guarantee high sensitivity regarding the measurement signals. The passive mixer is followed by an IF amplifier to compensate the losses incurred by the passive mixer and match the impedances at the demodulator input, Figure 82.

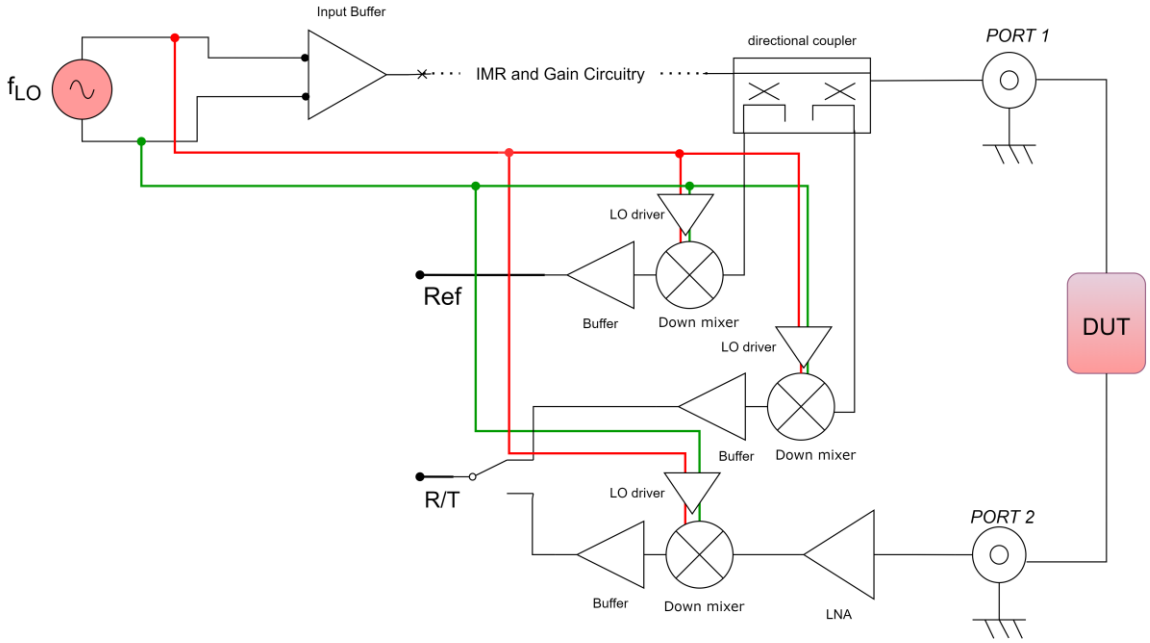


Figure 82 : Receivers Circuitry in the proposed compact vector network analyzer

As illustrated in Figure 82, the LO injected in the circuit splits to feed the transmitter path and the receivers. The receiver's path has 3.2 dB insertion losses at 30 GHz. To alleviate this gain drop, an LO driver is designed mainly to adapt the input LO impedance, since the mixer input impedance desadapts the input impedance of the IMR and gain circuitry. And also to provide an additional gain to compensate for the transmission line insertion losses. This driver consists of two cascaded inverter based amplifiers. From the external LO input and mixer output, including the transmission line electromagnetic extraction, the total gain varies between 4 and -7 dB from 200 MHz to 30 GHz, and the LO driver has a reverse isolation of 32 dB.

Following that, the passive mixer architecture is chosen, where low noise and high linearity are critical in this circuitry. As depicted in Figure 83, a differential double

balanced topology is chosen to attenuate the LO-IF and RF-LO feedthroughs with a compact, symmetrical layout that minimizes imbalances and common-mode leakage. It consists of four transistors, each of which operates as a switch. The high-swing LO signal drives the gate of transistors on and off, converting the RF signal to an IF signal. In consideration of the conversion loss and the linearity of the mixer, the width is determined. In the adopted mixer, the unit finger width of each transistor is 2 µm, and the total width is 20 µm. This mixer is followed by an output buffer. The simulated mixer voltage conversion gains at 200 MHz and 30 GHz are -1 dB and -6.7 dB, respectively. The passive mixer is followed by an output IF TIA[27] with a 10 dB gain over the 30 GHz bandwidth.

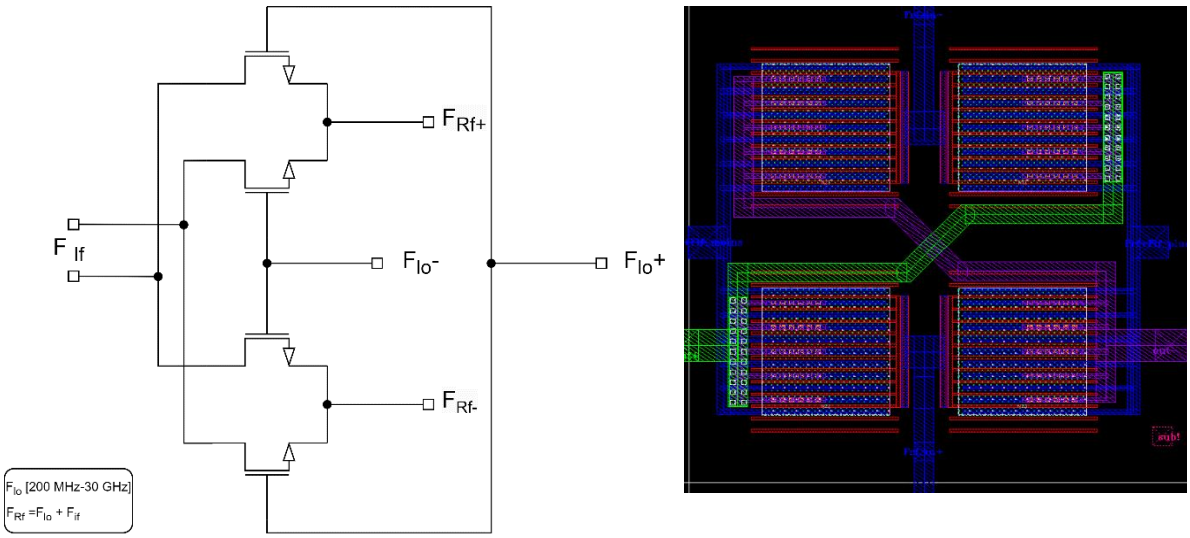


Figure 83 : down mixer architecture and micrograph (8 x 8 um)

As represented in Figure 84, to verify only the receiver's performance, the image rejection (up conversion mixer, PPF and IF quadrature generator) and gain circuitry (VGA) were not included. The receiver's test bench includes the **external LO signal**, which provides a voltage of 200 mV **from 200 MHz to 30 GHz** frequency band (-4 dBm referred to 50 Ω load). This signal goes through the transmission lines, and the LO driver to reach the LO mixer inputs. The directional coupler, on the other hand, is excited by a sinusoidal signal at the frequency of $\boldsymbol{f_{RF}=f_{LO}+f_{IF}}$, that in the complete circuit (Figure 31) results from the **up conversion** using the IMR mixer (**where the image frequency is rejected** $\boldsymbol{f_{IM}=f_{LO}-f_{IF}}$), with a power of 0 dBm, and loaded with a 50 Ω charge. The coupled and isolated ports feed the two passive mixers, for the reflection mode, followed by the mixer

[27] TIA : transimpedance amplifier (curent to voltage converter).

IF buffer. For the transmission mode, the f_{RF} source is placed at the input of the second port to characterize the receiver.

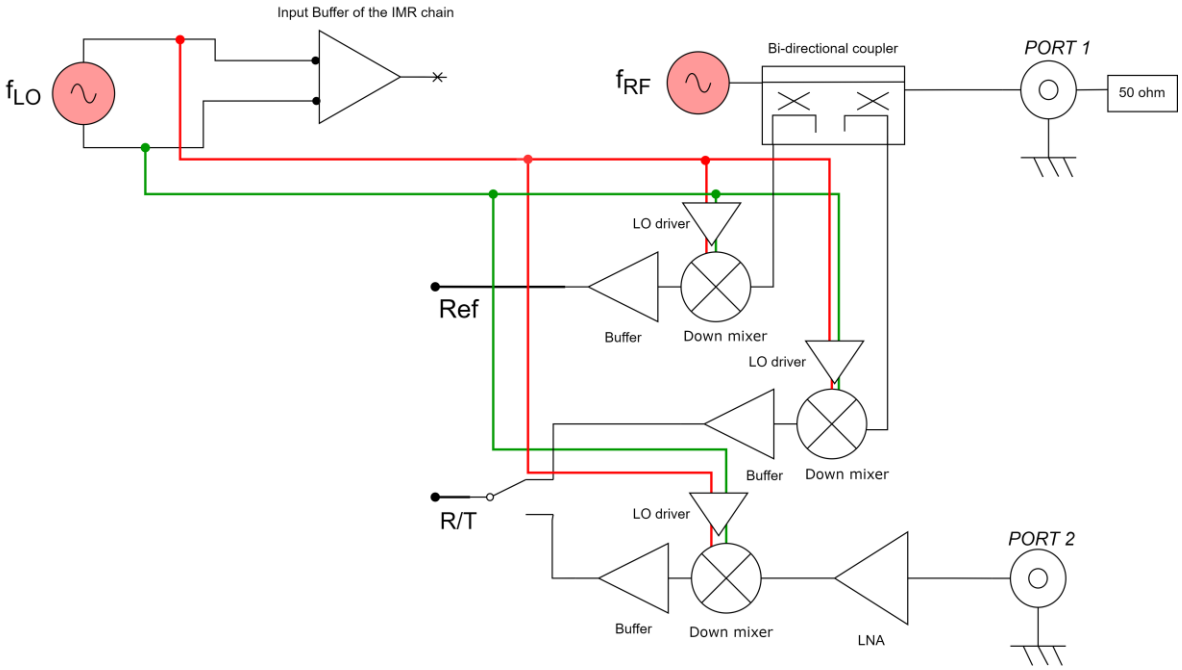


Figure 84 : Receiver's test bench

Figure 85 shows the receiver's specifications in terms of gain, linearity and noise figure. The total receiver's voltage gain ranges from 9 to 3.5 dB and the LO_IF and LO_RF isolation varies between [-66.8, -64.6] dB and [-63.8, -60.4] dB, respectively for an $f_{lo} \in [200\ MHz - 30\ GHz]$. The receiver input compression point varies between -9 and -11 dBm over the 0.2-30 GHz bandwidth. The simulated SSB (single side band) noise figure is 21–25 dB at 0.2–30 GHz, resulting in a receiver dynamic range of 82 ± 2 dB in a 455 KHz resolution bandwidth (RBW), which is defined as the difference between the 1-dB compression points of the receiver's channels' and the noise floor. Otherwise, by using the external selective ceramic filter at 455 KHz, with its bandwidth of 12 KHz (Figure 25) , the DR is increased by a factor of 15 dB (the conventional RBW of commercial VNA's is set to 10 Hz). Finally, considering the power cost, each receiver has a current consumption of 529 µA under a voltage supply of 1V.

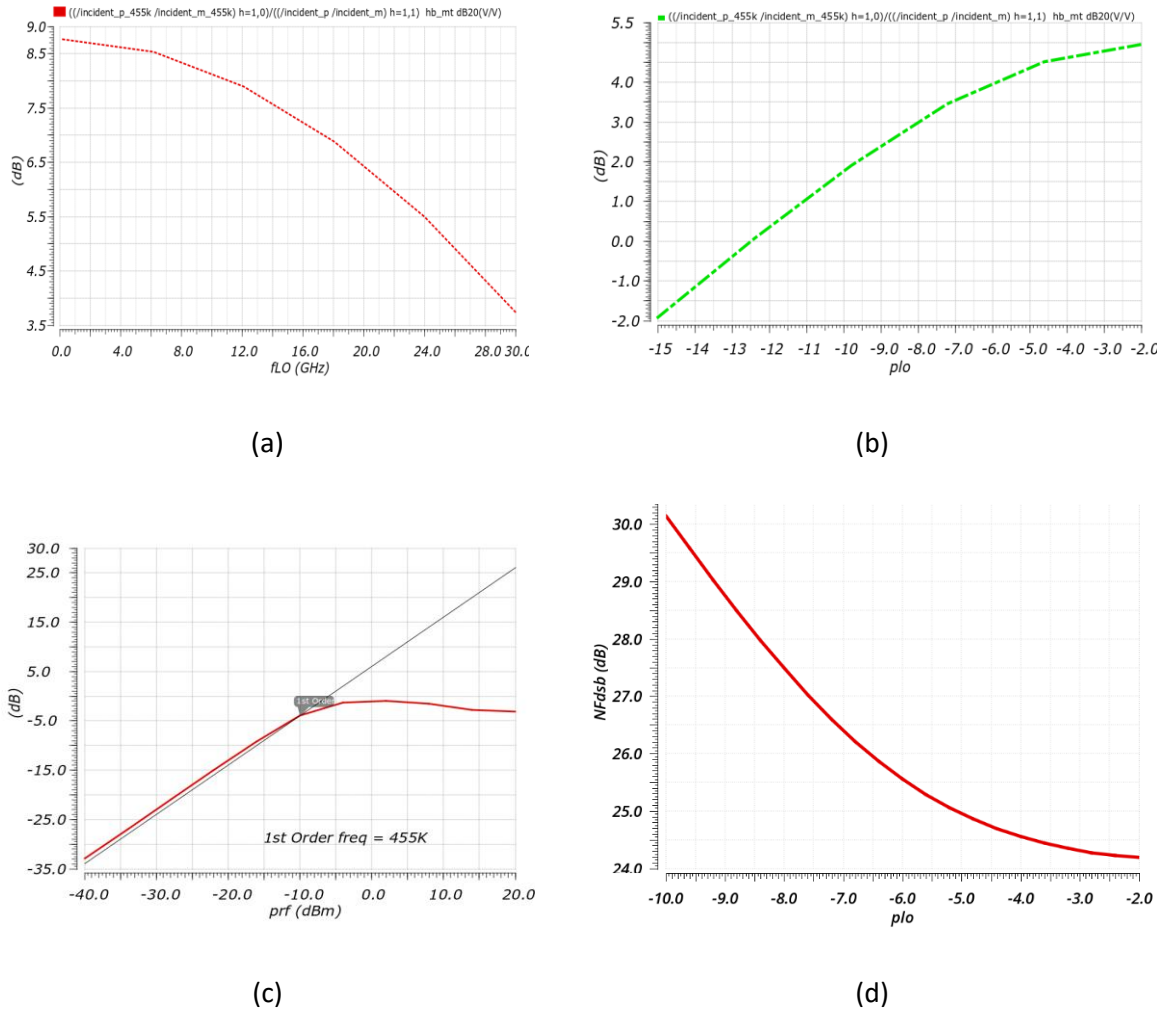


Figure 85 : (a) The receiver's voltage conversion gain Vs LO frequency (b) Voltage Conversion Gain versus the LO Signal Power (c) 1dB compression point @flo10GHz (d) Double sideband noise figure Vs the LO power

In the state of the art (1.2), it was observed that the processing of the output signals of three receivers is done by an external ADC for each IF output. Thus, the maximum achievable dynamic range of the VNAs in the literature is determined by the dynamics of these receivers. In our case, the VNA DR is related to both receivers and the demodulator's dynamic range. To achieve the targeted dynamic of 80 dB, we have considered two different dynamics with different design constraints. In this section, an achievable DR of 82 dB at the receiver's output was discussed. The second dynamic range is the demodulator DR, which defines the achievable dynamic range of the proposed VNA and will be dealt with in the next section.

3.6 MAGNITUDE AND PHASE DETECTION CIRCUITRY

This section deals in depth with the operation of the demodulator addressing the theoretical analysis and the post layout simulation results. This demodulator involves a nonlinear operation. It is the key building block of the compact vector network analyzer. It enables direct amplitude ratio and phase difference measurements between two independent input signals. It impacts the VNA dynamic range, its sensitivity, and the measurement errors of S parameters.

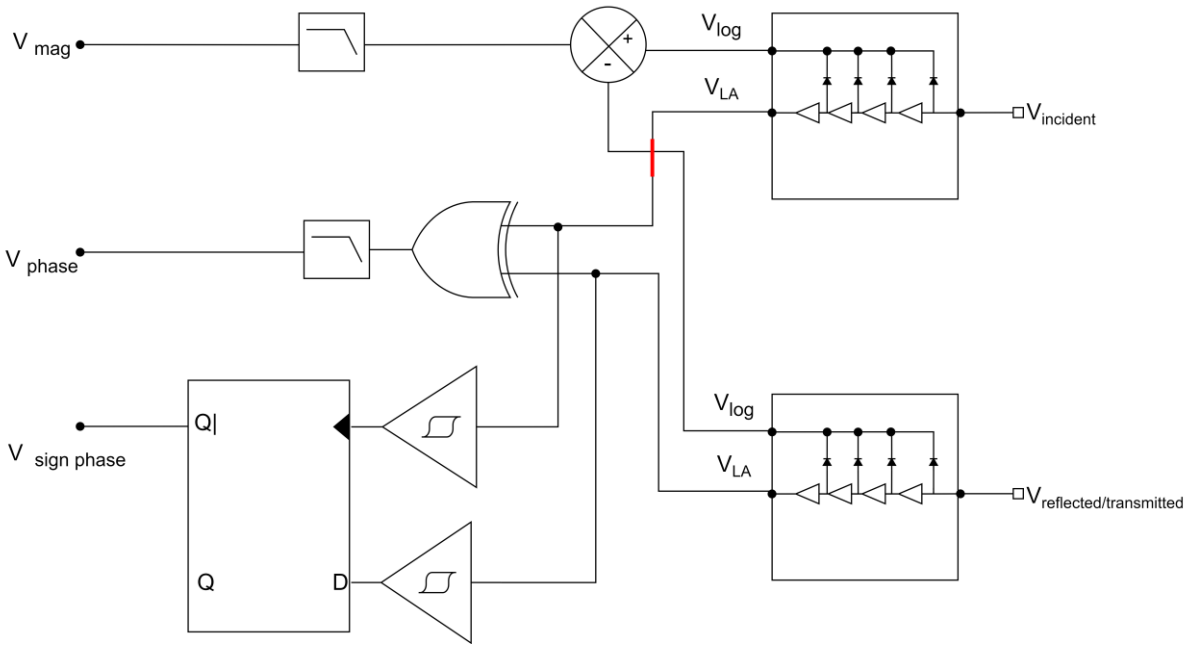


Figure 86 : Magnitude and phase demodulator architecture

Figure 86 shows the architecture of the phase and magnitude demodulator, which consists of two identical logarithmic detectors[28], a digital phase detector, a subtracting current mirror circuit and two external low pass filters to extract the DC outputs V mag and V phase. Each logarithmic amplifier presents two voltage outputs: a squared limited output VLA which is a saturated signal over the input dynamic range, and a pseudo-logarithmic output, Vlog, which represents a logarithmic conversion of the input voltage. The outputs of the full detector block are two independent DC voltages V_{gain} and V_{phase} are proportional to the relative amplitude (gain or loss) and relative phase of the two input signals, respectively, as expressed in (24), where $V_{slp}$the slope of V_{gain} expressed in Volt/decade and V_{Φ} is the slope of V_{phase} in mV/degree.

[28] known as reverse received signal strength indicator (RSSI)

$$\begin{cases} V_{gain}(mV) = V_{slp}\log(\dfrac{V_{reflected|transmitted}}{V_{incident}}) \\ V_{phase}(mV) = V_{\Phi}(\Phi_{reflected|transmitted} - \Phi_{incident}) \end{cases} \quad (24)$$

3.6.1 LOGARITHMIC AMPLIFIER DESIGN

A logarithmic amplifier amplifies the logarithm of an input signal rather than the signal itself. This type of amplifier is useful for measuring signals with a wide dynamic range, as it can compress a large range of input levels into a smaller output range. As depicted in Figure 87, the logarithmic amplifier circuit is based on the successive detection architecture. This circuit consists of cascaded limiting amplifier cells, of which the gain is a "gain state" and which have a saturated output voltage level for a given input level E_k. The amplifier is in the limiting state.

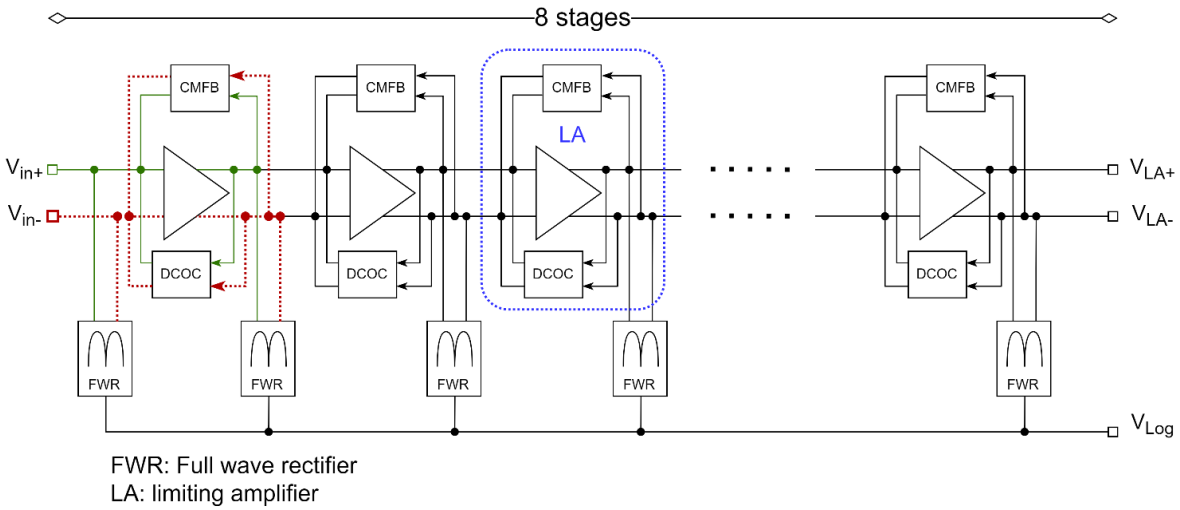


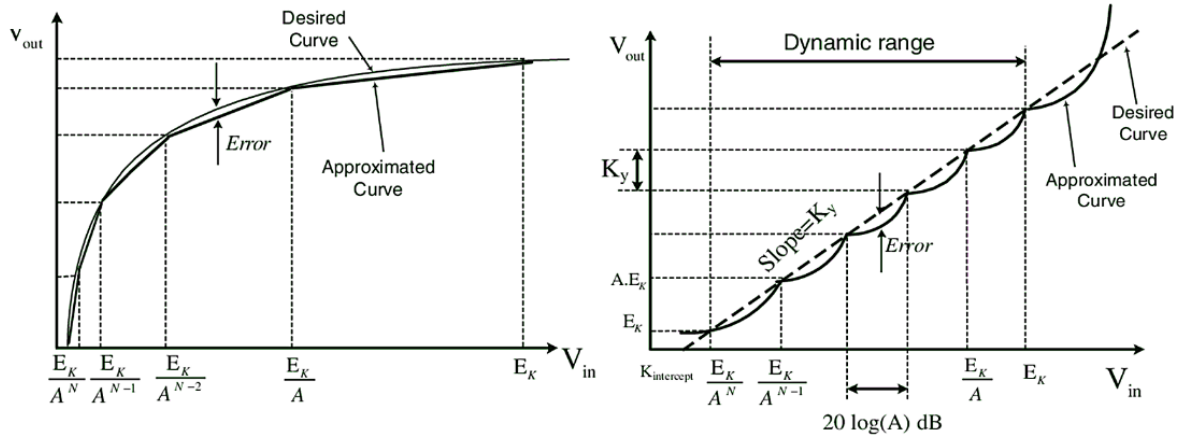
Figure 87 : Block diagram of the designed logarithmic amplifier

In each stage, the amplified signal is rectified in the current domain and then summed up. Hence, the total output voltage V_{out} shows linear characteristics with respect to the input signal voltage on a semi logarithmic scale. Indeed, while using this architecture, the response approximates the logarithmic function response in a piecewise linear manner, as depicted in Figure 88. It could be expressed theoretically as (25) [106]:

$$\begin{cases} V_{out} = K_y 20\log(\frac{V_{in}}{K_{intercept}}) \\ K_y = \frac{(A-1)\,E_k}{20\log(A)} \\ K_{intercept} = \frac{E_k}{A^{\frac{N+1}{A-1}}} \end{cases} \quad (25)$$

Where:

- K_y refers to the ideal desired curve slope.
- $K_{intercept}$ refers to the intercept point of the logarithmic transfer function.
- N refers to the number of limiting amplifier stages.



(a) (b)

Figure 88 : Magnitude transfer function of the logarothmic amplifier in both (a) linear and (b) semi logarithmmic scale [106]***.***

Another important parameter is the dynamic range of the logarithmic amplifier. The upper bound of the dynamic range of the logarithmic amplifier is determined when the input signal is so high that all stages enter the limiting state. So, the upper bound is EK. The lower bound is determined when the input signal is so low that all stages are in the gain state. Increasing the number of cascaded stages decreases the lower bound until the amplifier input noise determines the lower bound of the dynamic range of the logarithmic amplifier. It is commonly equal to $20\log(A^N)$.

Now, considering the demodulator requirement as stated in the second chapter, the minimum detected power is -60 dBm. Since the logarithmic amplifier input is not adapted to

a 50 Ω load, the study is done in the voltage rather than power domain. Hence, the minimum input voltage is equal to 316.180 µV in theory, because in fact, the signal could merge with the noise. On the other hand, increasing the series of cascaded gain stages results in a wide dynamic range that spans several tens of decibels through the linear approximation. Table 14 presents a summary of the targeted circuit specifications, including the rationale behind the chosen values for each parameter.

Parameter	Type	Comments
Bandwidth	455 KHz	The logarithmic amplifier has a wide operation frequency ranging from 80 KHz to 1 GHz
Sensitivity	-60 dBm	Based on system budget study
Vin min	30 µV	Based on system budget study, the required input sensitivity is 300 up. an additional margin with a factor of 10 is applied
Vin max	300 mV	This value refers to input voltage value when the limiting amplifier enters the limiting state E_k, ***Figure 88***
DR	80 dB	DR=$\frac{V_{in,max}}{V_{in,min}}$
Supply voltage	1V	45 RF SOI technology

Table 14: Logarithmic amplifier specification

To meet the targeted 80 dB dynamic range, eight amplification stages with each 10 dB gain were implemented, along with nine full wave rectifiers. The input of the logarithmic amplifier is amplified and rectified through each gain cell/FWR, then summed up in current mode. DCOC (dc offset cancellation) is added at each gain stage separately since dc offset from the outputs of each amplifier can severely deteriorate the performance of the rectifiers. In addition, a common mode feedback (CMFB) circuit is necessary to stabilize the DC operating point and bias the next stage.

3.6.2 THE LIMITING AMPLIFIER DESIGN

The amplification stage is implemented using a “limiting amplifier”. It amplifies the signal up to a certain point E_k, after which any further increase in input signal level will not result in a proportionate increase in output signal level. This creates a "clipping" effect, where the signal is "limited" to a specific amplitude. The limiting amplifier is required to provide a 10 dB gain with very low input noise considering the 455 KHz bandwidth at 1 V supply voltage. The schematic of the core amplifier is shown in Figure 89 (a). The VNA IF signals are fed to the transconductance stages M1, M2. The load consists of two poly-silicon resistors (RL) connected differentially and two pairs of PMOS transistors (M3, M4).

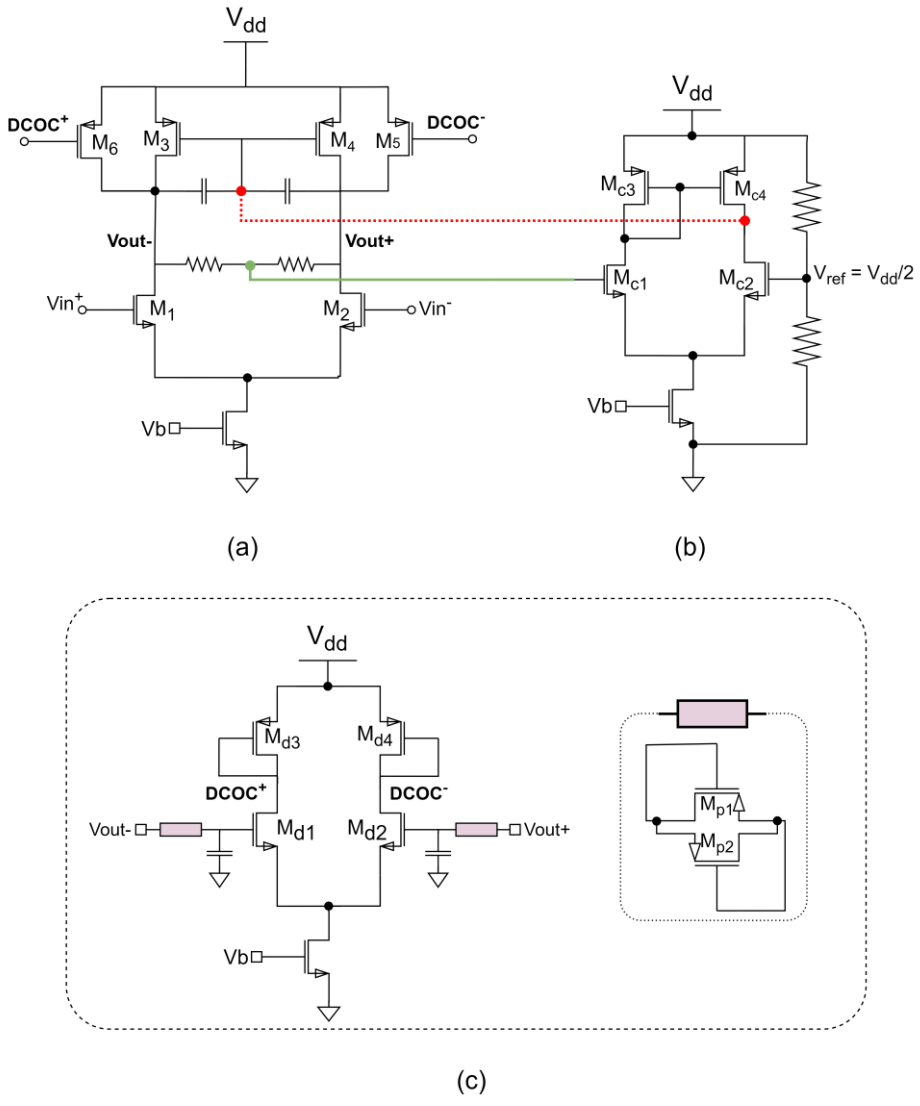
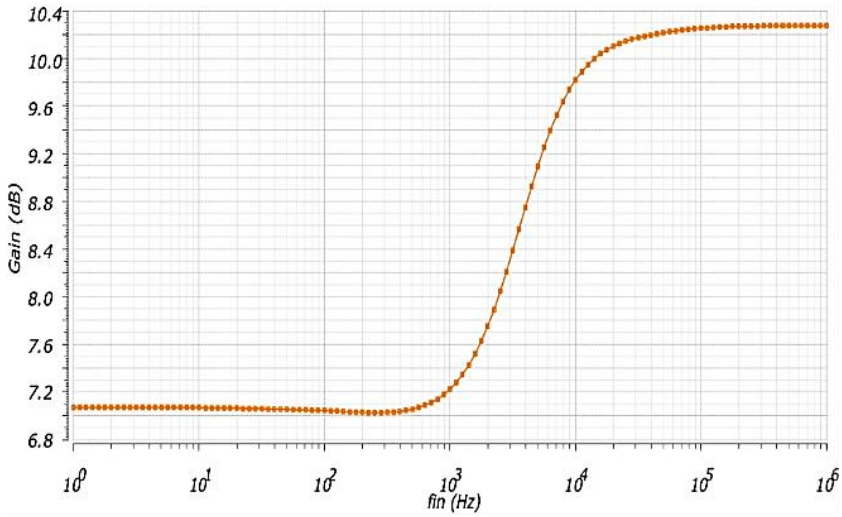


Figure 89 : Limiting amplifier circuits: (a) gain cell (Gm-stage), (b) common mode voltage control unit (c) DC offset cancellation unit (large filtering resistance using two PMOS configuration)

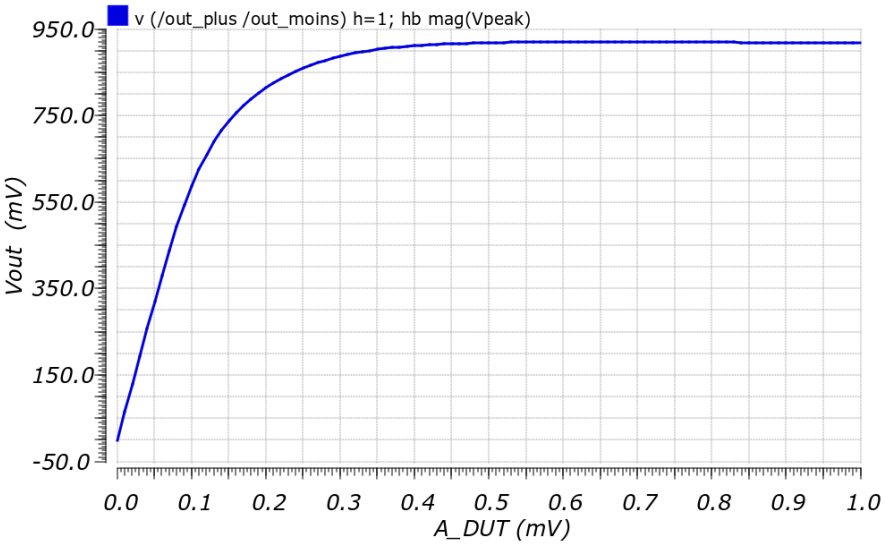
The output common mode DC drain voltage is controlled with a fed back loop to set the constant output voltage tuned to $\frac{V_{dd}}{2}$, to maximize output voltage swing. It controls the common mode level of the output signal, which biases the next amplification stage. The differential pair compares the reference voltage (V_{ref}) with the common mode drain of the limiting amplifier Gm stage, as depicted in Figure 89 (b). The drain voltage of Mc2 is fed to the gate of PMOS load transistors M3 and M4. The currents of these PMOS are changed with feedback voltage, leading to the adjustable limiting amplifier's common mode DC output voltage. With high enough loop gain, V_{ref} and common mode voltage are equal.

Another point is the DC offset cancellation. Indeed, due to the open loop limiting amplifier stages, even a very small DC offset in the circuit could lead to saturation of the output signals. For each limiting amplifier, a local feedback based offset cancellation mechanism is employed to provide sufficient offset cancellation range. In Figure 89 (c), differential DC offset voltages at the limiting amplifier output are sensed and passed through a low pass filter. Considering the cutoff frequency of 455 KHz, the low pass filter is designed to have the lowest value of capacitance and an active high resistance value using two PMOS transistors. This configuration consists of two parallel drain gate connected PMOS transistors. Due to the large resistance of the active transistor, a capacitance in the range of pF (2 pF) can achieve a small frequency low pass pole.

As depicted in Figure 90 (a), the expected gain of 10 dB is validated through the post layout simulation results (calibre extraction). On the other hand, the DC common mode control has been verified by injecting a DC gate bias of 500 mV ±10 %, the output common mode is $500\ \mathrm{mV} \pm 8\ \mathrm{mV}$. Finally, the gain cell transfer function is depicted in Figure 90 (b) and the upper bound of the logarithmic amplifier dynamic range is set at $E_k$equal to 300 mV, as set in the initial specifications (Table 14).



(a)



(b)

Figure 90 : (a) Limiting amplifier gain with DC offset cancellation (b) Limiting amplifier transfer function with limiting point Ek equal to 300 mV

3.6.3 CURRENT FULL WAVE RECTIFIER

The second key block to design is the full wave rectifier. Hence, Figure 91 illustrates a circuit that converts an alternating input voltage into a direct current through a process known as full-wave rectification. This is achieved by utilizing unbalanced source-coupled pairs with a specific ratio of input transistors k. This factor has a considerably large value since the input voltage range within a differential current has a parabolic characteristic proportional to $\frac{1}{\sqrt{k}}$.

However, it is limited to setting the unbalanced pairs in the saturation region [107]. The tradeoff value is set at four. Hence, $\frac{W}{L}\Big|_{(M_1,M_3)} = 15\mu m/40nm$, $\frac{W}{L}\Big|_{(M_2,M_4)} = 3\mu m/40nm$ and $\frac{W}{L}\Big|_{(M_5,M_6,M_7,M_{8,})} = 10\mu m/232nm$. The output current I_{out} of the rectifier is determined by the difference in current between the cross-coupled differential pairs and is equal to $I_1 + I_4 - I_2 - I_3$. The circuit operates with a single 1 V supply voltage and the power consumption is 409 µA for one rectifier.

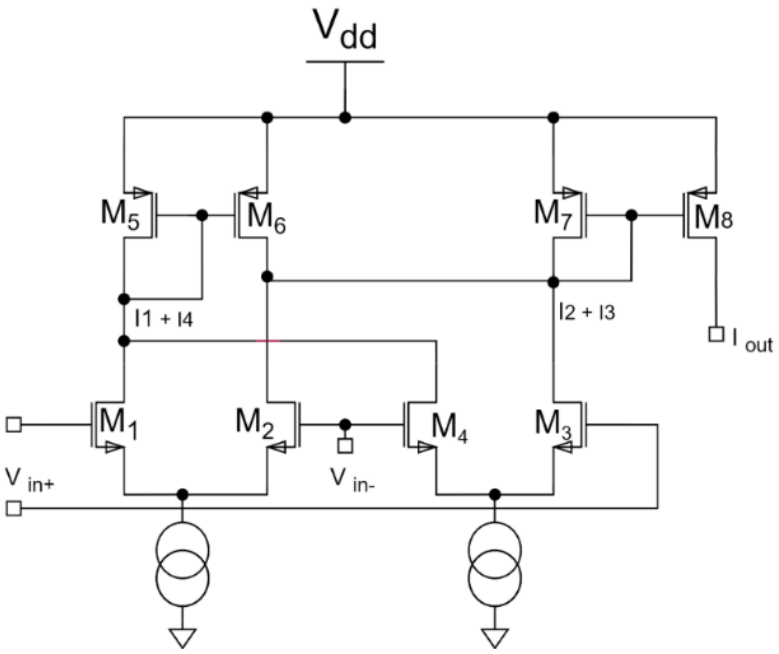


Figure 91 : Full wave rectifier circuit

Up to now, the building blocks of the logarithmic amplifier have been presented. As illustrated in Figure 92, the complete circuit was fabricated with a 45RFSOI process, covering an area of 700 µm x 116 µm. The following paragraphs will present the simulation results.

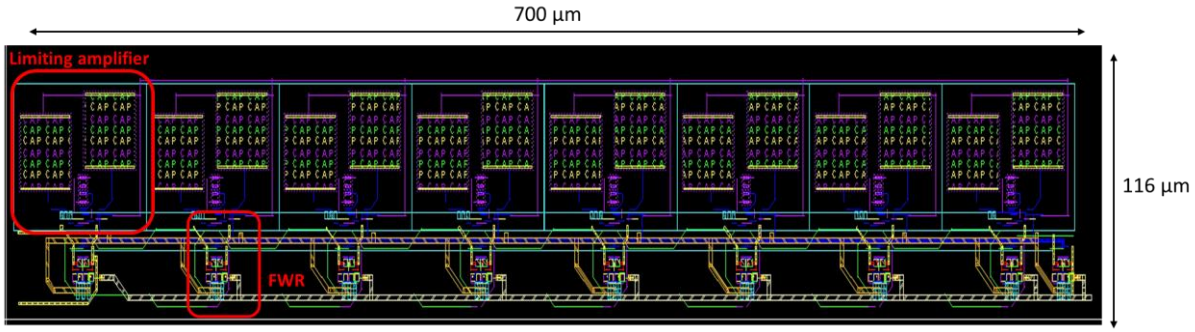


Figure 92 : Logarithmic amplifier layout micrograph

As mentioned in the theoretical section, the upper bound of the dynamic ranges is set at the limiting state E_k at 300 mV. The lower bound is determined when the input signal is so low that all stages are in the gain state. So, increasing the number of the cascaded stages decreases the lower bound until the logarithmic amplifier input noise determines the lower bound of the dynamic range of the logarithmic amplifier. Hence the input referred noise of the logarithmic amplifier is an important figure of merit that sets the demodulator's sensitivity. As shown in Figure 93, at the intermediate frequency of 455 KHz, the input referred noise at the demodulator input (the receiver's not included) is equal to 47 $\frac{nV}{\sqrt{Hz}}$. Hence, by using the external selective ceramic filter with a bandwidth of 10 Hz, the minimum detected input voltage could be enhanced to be equal to 0.18 µV.

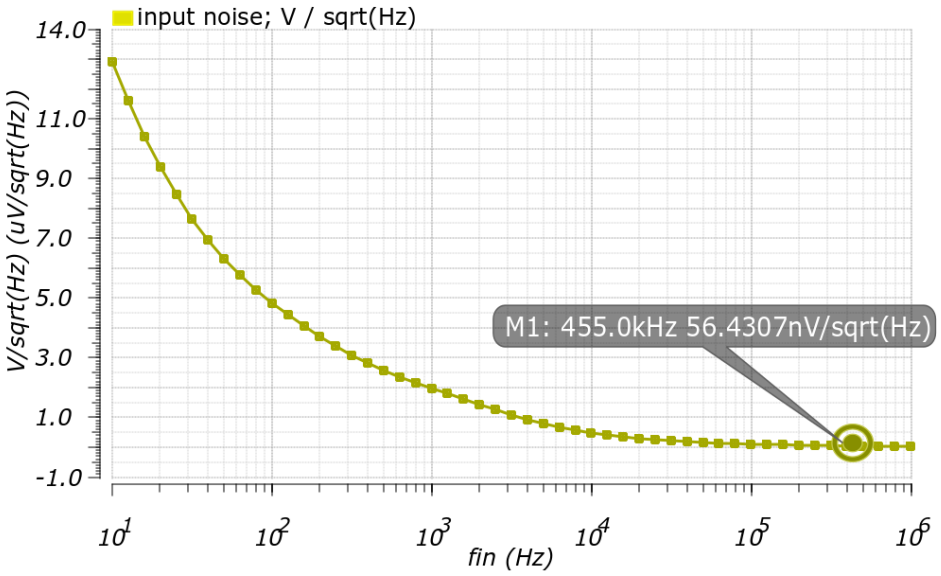


Figure 93 : Loagrithmic amplifier input reffered noise

The second test set is to ensure the proper functionality of the full-wave rectification. This test bench involved loading the output of the logarithmic amplifier with a 350 Ω resistor to ground (to set the common mode voltage at $\frac{V_{dd}}{2}$). For a sinusoidal input signal with 30 mV amplitude at 455 KHz, the output signal is rectified and could be smoothed with a parallel capacitance, as shown in Figure 94.

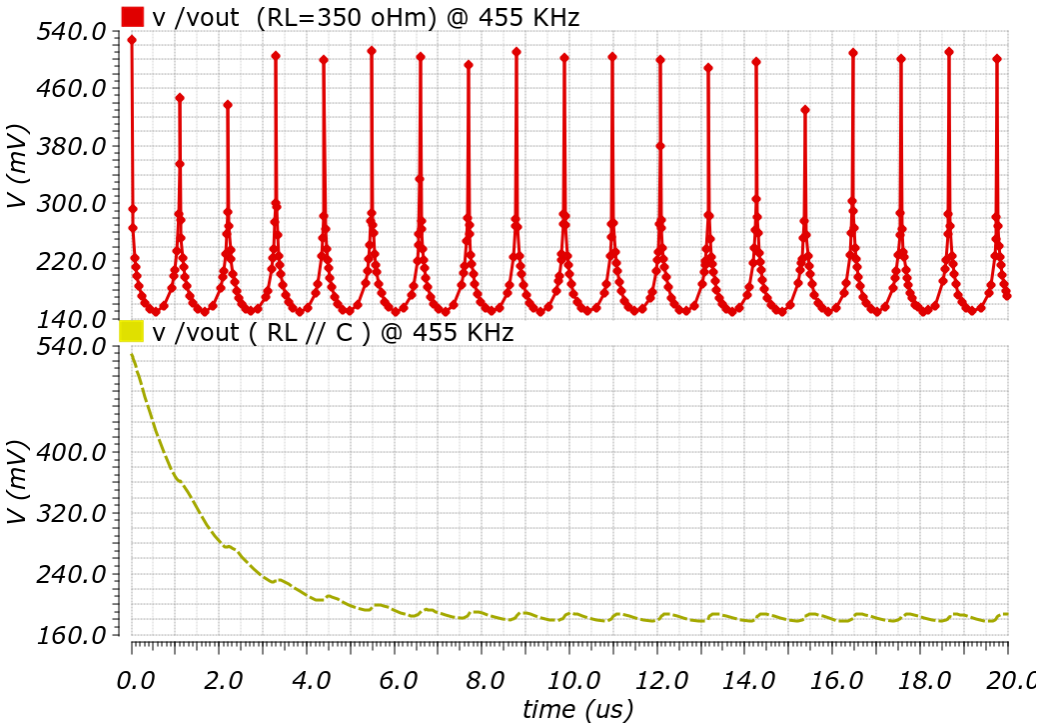


Figure 94 : Logarithmic amplifier output loaded with a 350 Ω resitance and with a capacitor in parallel

Figure 95 shows the logarithmic transfer function and the frequency response of the amplifier, respectively. The dynamic range of the amplifier is observed from 1 µV to near 300 mV, which is interpreted as a 109 dB dynamic range for an output swing of 411 mV. The slope K_y is equal to 171.39 (mV/decade) measured between E_k (300 mV) and E_k/A (94 mV), as defined first in Figure 88. Compared to the theoretical equation of the logarithmic transfer function (25), $K_y = \frac{(3.16-1)300e-3}{20\log(3.16)} = 175.95$, the simulated slope is within 4 mV/decade the expected theoretical one.

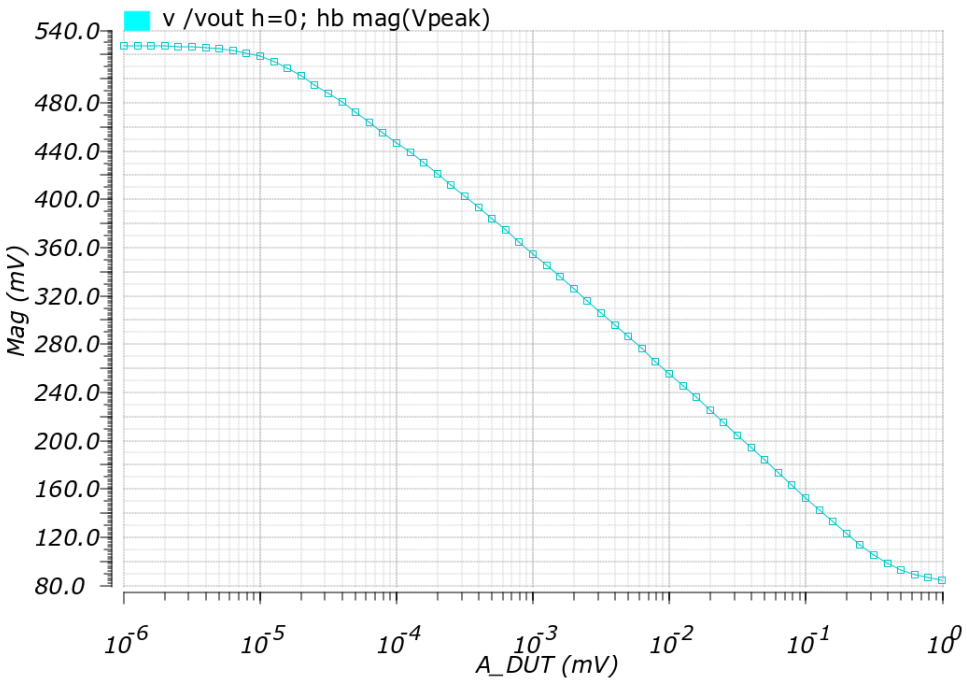


Figure 95 : Transfer function of the Logarithmic amplifier (8 stages)

Back to the demodulator architecture, as described earlier in Figure 86, the circuit is built on two identically designed logarithmic amplifiers. Where the second logarithmic output of the reference signal is subtracted in current from the first, which measures the reflected or transmitted signal. The used current substractor is based on two current mirrors, as depicted in Figure 96 . The current subtraction circuit is realized by merging two current mirrors. Assuming all the transistors have the same size, the current $I_{R/T}$ is applied to the first current mirror. It is copied to transistor M2, then, at the same node, the second current I_{ref} is injected. As a result, current $I_{R/T} - I_{ref}$ flows from the drain to gate of M3. To finally be copied due to the second current mirror. The output current is loaded with an active PMOS transistor and then filtered using an on board (outside the chip) RC filter to provide an output V_{mag} proportional to the reflected incident or transmitted incident voltage ratios.

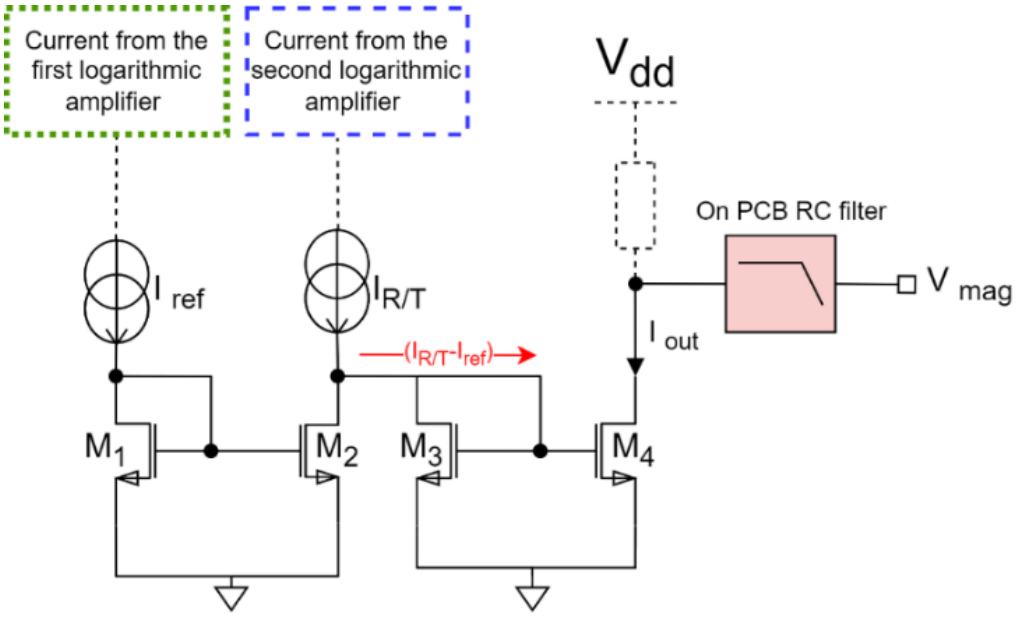


Figure 96 : Current substraction circuit loaded with an active load, then filterd out to extract the DC output V mag

Regarding the phase detection, the differentially limited signals from both logarithmic amplifiers $V_{LA,1}$ and $V_{LA,2}$ are fed into a XOR[29] circuit, which, after low pass filtering, provides a signal proportional to the difference between the phases of the transmitted or reflected (T/R) signal and the reference signal.

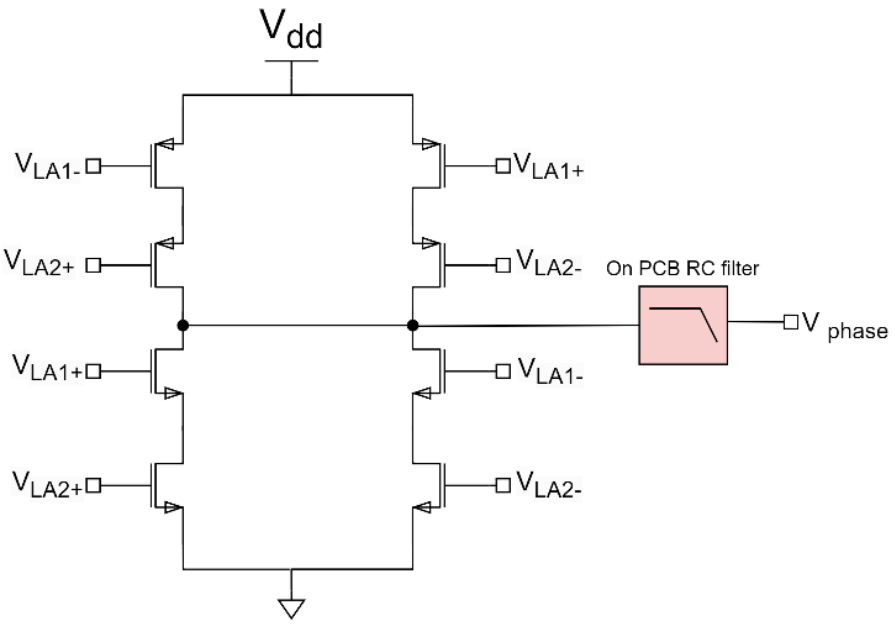


Figure 97 : The proposed XOR circuit

[29] In an XOR circuit, the output is a logic 1 when one and only one input is a logic 1. Hence, the output is logic 0 when both inputs are logic 1 or logic 0 simultaneously.

As illustrated in Figure 98, the demodulator including all the previously designed blocks is implemented with 45RFOI technology. The demodulator occupies 900 µm on 243 µm and draws 40 mA current for a 1 V voltage supply.

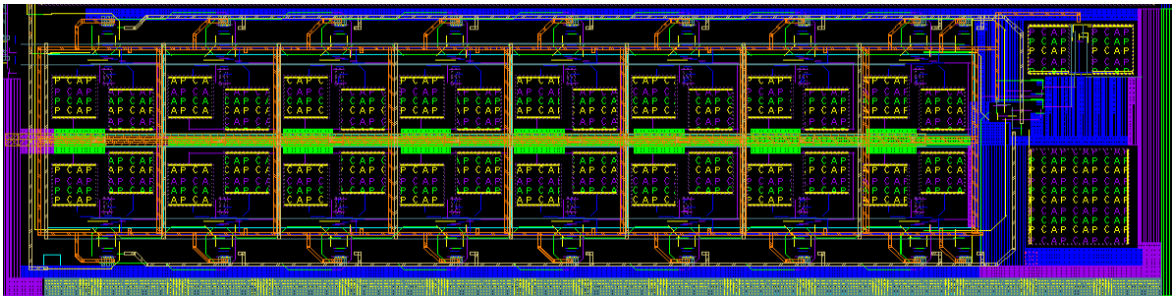


Figure 98 : the micrograph of the proposed demodulator 900 um x 243 um

To validate the initial specification of the demodulator, a test bench is set up to show the magnitude, phase transfer function, and phase sign ambiguity. As shown in Figure 99, a first sinusoidal input provides an amplitude A_{DUT} at 455 KHz, the second source provides an amplitude A_{ref}referring to the coupled incident signal at 455 KHz. An AC coupling is set between the receivers (transmitted or reflected (T/R) and reference) and the demodulator input. The capacitors are chosen to be as large as possible considering the area of the circuit (100 pF).

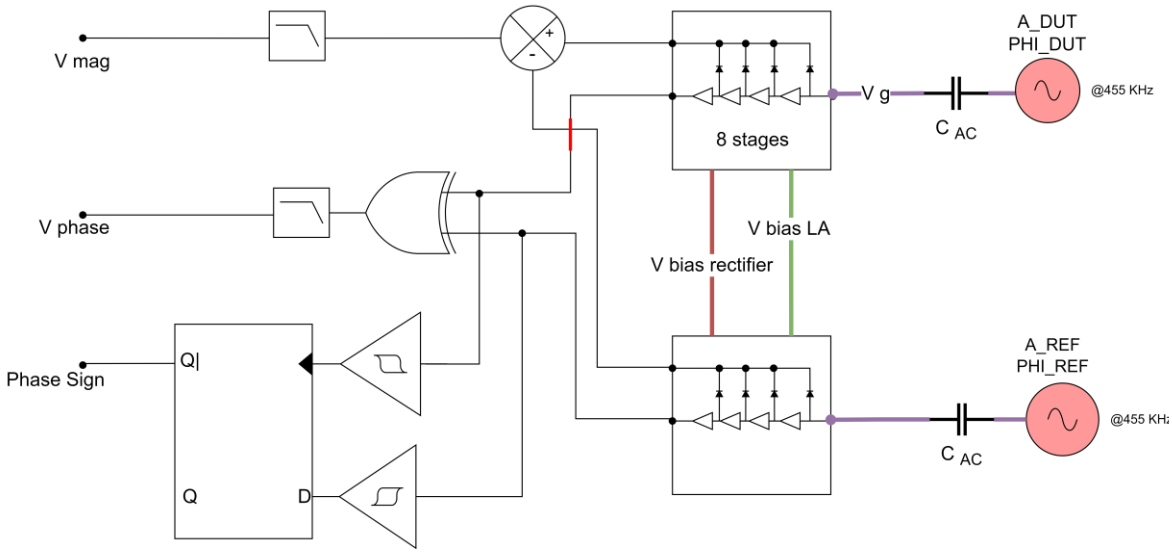


Figure 99 : the demosulator post layout simulations test bench

The phase characteristic is presented in Figure 100. It shows the 0 Hz harmonic value (computed from an HB simulation) varying between 10 mV and 850 mV for a phase range varying between -180 and 180 °. In this simulation, the DUT phase varies between -180 and

180 degrees, while the reference phase value is set to zero. The voltage v_{phase} is translated to absolute phase, both -90 ° and +90° correspond to the same voltage value of 460 mV, corresponding to half of the output voltage dynamic.

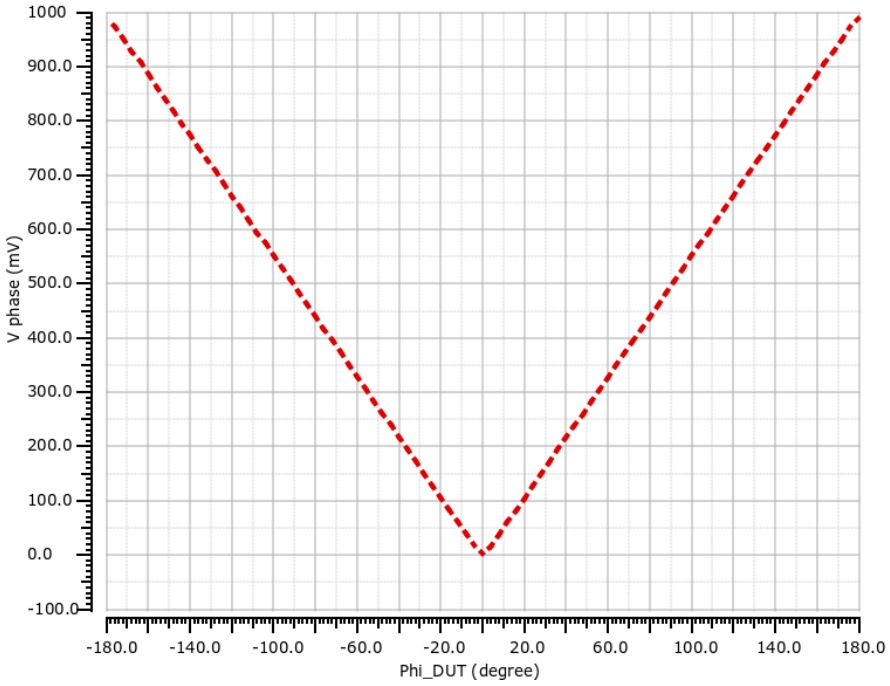


Figure 100 : Phase transfer function at @ 455KHz

As previously shown in Figure 94, the magnitude output, which is the sum of the full wave rectifier's currents, should be loaded with an RC low pass filter. In fact, the capacitor filter, through its discharge, will generate an extremely smooth DC voltage v_{mag}(depending on its value) instead of the rectified picked signal.

On the other hand, when a digital circuit produces a phase output using XOR logic, the output has fluctuations in its DC value. To address this issue, a capacitor was added to the phase output. This helps to smooth out the DC phase value v_{phase} of the output signal, providing a more stable signal.

All in all, due to size restrictions, the RC low pass filters are implemented on the PCB to extract the two DC outputs v_{phase} and v_{mag} . As the transient simulation shows in Figure 101, the voltage V_{phase} varies between 10 mV and 850 mV as predicted in the HB simulation previously shown. The filter's transient response is equal to 30 µs, a factor that should be considered when measuring with the VNA demonstrator.

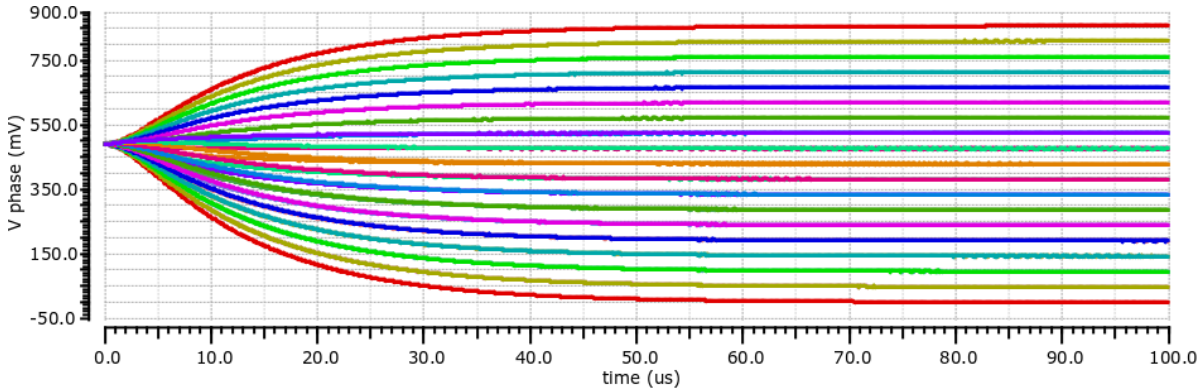


Figure 101 : Transient simulation V_{phase} output Vs DUT phase [-180° :180)] over 100 µs

Back to the phase ambiguity issue, two possible solutions have been investigated:

One consists of performing two measurements, one with no reference phase shift and one with a reference phase shift (PS), as Figure 102 shows. The first measured phase (without the PS) will fall in the range of -180 ° degrees to +180. It could be A or B, but when shifted to a well-known shift value, PS. The phase shift produces A' or B'. If the shifted phase value is higher than PS, then the actual phase is correlative to B, otherwise, it is the opposite (A). This solution suffers from the systematic errors (1.1.4) that could occur between the first and second measurements. In addition, after the phase shifter implementation, the circuit suffers from high losses and creates an imbalance between the voltage gain of the reference receiver and the reflection receiver. In addition, there is more uncertainty near the peaks with a long measurement time compared to a one-shot measurement. After these findings, this option was not considered.

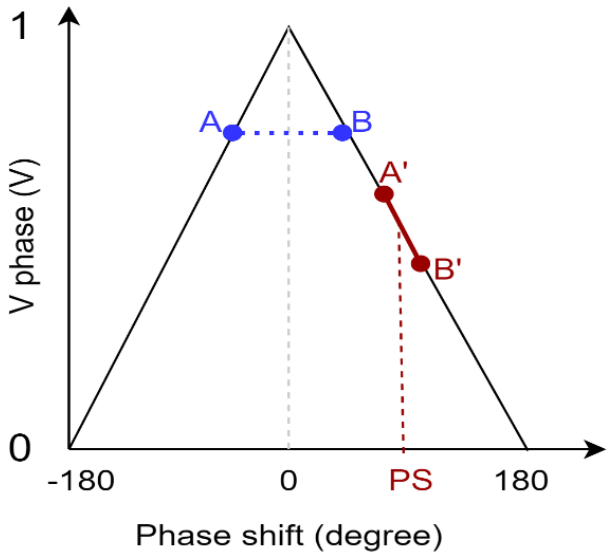


Figure 102 : Points A and B have opposite phase polarity but the same output level. When shifted to the right by PS degree, points A' and B ' are produced.

As depicted in Figure 103, the **second solution**[30]**is selected**. It is implemented by loading the saturated logarithmic amplifier's outputs, VLA1 and VLA2, with a hysteresis amplifier followed by a D flip flop. It detects the first zero cross of both signals (reference and T/R). This crossing leads to a D flip flop output of zero if the phase is advanced or 1 otherwise.

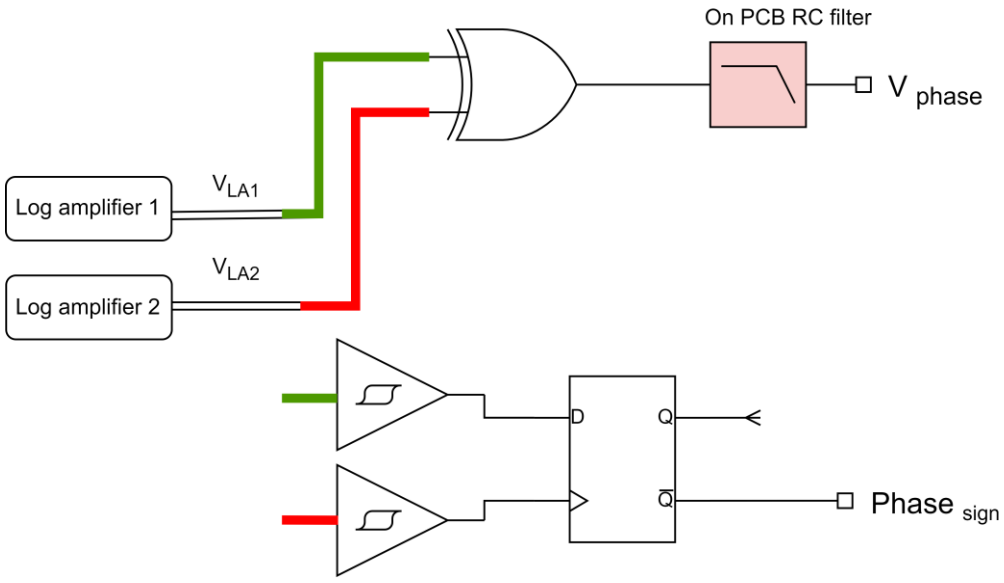


Figure 103 : The proposed circuit to Resolve phase ambiguity

[30] This solution is internally patented by CEA Leti.

Both the flip flop and hysteresis comparator are designed with 45RFSOI technology. The flip flop circuit is similar to the proposed architecture for the IF quadrature generation. The hysteresis comparator is implemented as shown in Figure 104, in this topology, the negative feedback is through the transistors M_1 and M_2. The positive feedback is on the transistors M_9 and M_{10}. Indeed, the ratio between M_{11}, M_{12} and M_{10}, M_9 determines the overall feedback sign. Hysteresis occurs when the ratio is greater than 1. Hence $\frac{W}{L}\Big]_{M_9,M_{10}} = 20\ \frac{W}{L}\Big]_{M_{11},M_{12}}$, with a width equal to 200 nm and a length of 40 nm.

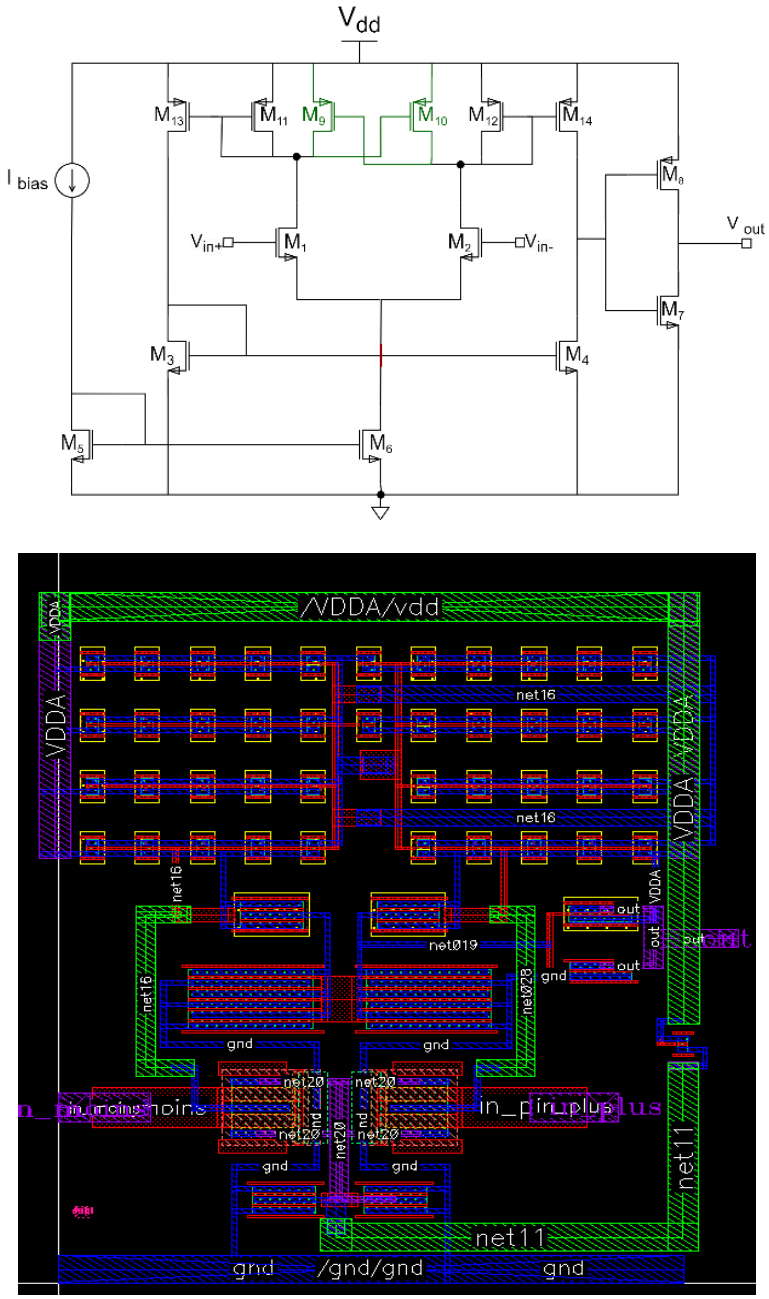


Figure 104 : The proposed hysteresis comparator circuit and its layout

To verify this approach, a transient simulation was performed. A negative phase shift, followed by a positive one, was injected at the input of the DUT logarithmic amplifier, covering the range [-180°:180°] with a step of 20 degrees. The phase sign output is set to zero if the DUT signal is in phase advance with respect to the reference signal. Otherwise, it is equal to 1, Figure 105.

Figure 105 : The phase ambiguity output equal to 1 when the delta phi is negative, and 0 otherwise

In Figure 106, the magnitude transfer function is expressed based on the DUT sinus wave amplitude variation with a fixed value of the reference voltage the minimum detectable amplitude is 10 µV. This value was optimized by minimizing the voltage noise spectral density, as shown previously in the limiting amplifier design section. The integrated noise voltage sets a bound on the smallest input voltage that can be certainly measured. The upper bound is limited to 280 mV with an output dynamic range of 550 mV.

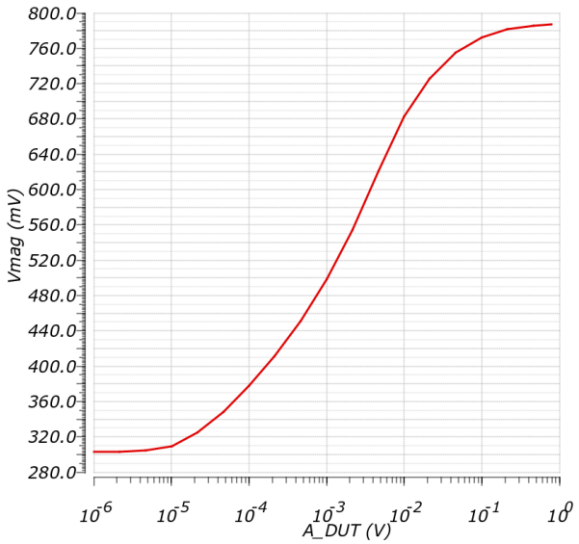


Figure 106 : Magnitude transfer function at @ 455KHz V reference corresponds to logarithmic amplifierDR midpoint

Now, the demodulator's dynamic range as a function of the amplitude ratios is determined by the minimum and maximum levels that each individual logarithmic amplifier can detect. As shown previously in Figure 95 , each log amplifier detects voltage inputs ranging from 10 µV to 300 mV, equivalent to an 80 dB dynamic range for each. To cover this entire range, the reference voltage level (that feeds the second logarithmic amplifier) must correspond ideally to its midrange, which is exactly the 10 mV set for the reference voltage in the presented simulations. Otherwise, if the reference voltage slightly differs from the ideal value, the demodulator's dynamic range is reduced, as illustrated in Figure 107 .

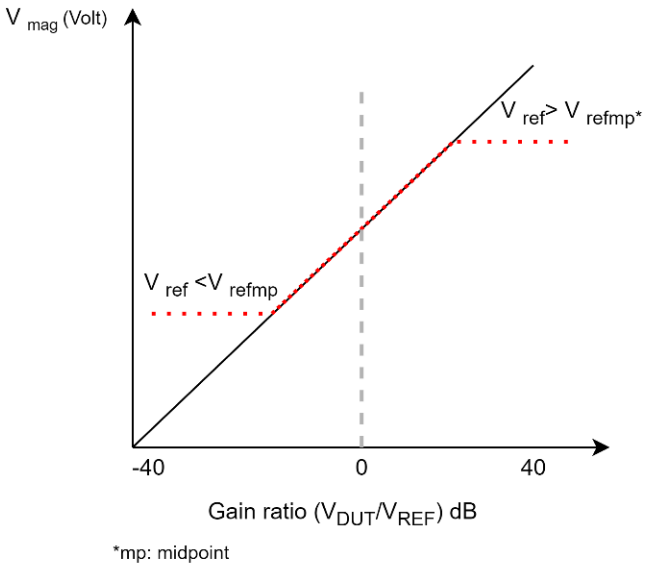


Figure 107 : The effect of varying the reference voltage (incident signal) from the optlmal midpoint value

Overall, the detector achieves a wide output dynamic range related to phase difference and amplitude ratio. It achieves a minimum detectable voltage of 1 µV for a reference voltage of 10 mV[31]. Table 15 summarizes the demodulator post layout specifications.

Parameter	Initial specifications	Post layout specifications	Unit
Bandwidth	455	455	KHz
Vin min	30	10	µV
Vin max	300	280	mV
DR	80	88.94	dB
Supply voltage	1	1	V
Power consumption	Not defined	40	mA

Table 15: Demodulator post layout specifications

3.7 ANALYSIS AND CONCLUSION

In the proposed VNA, the lower end of the dynamic range corresponds to the demodulator noise floor, which is the limiting factor for the detection of low power signals. The upper limits depend on the dynamic range definition. The receiver's dynamic range is equal to 82 dB, and the demodulator's dynamic range is 88.94 dB. Both meet with each other, except for the upper bound of the demodulator limiter at 280 rather than 300 mV. This should not be a problem. The reflection signal would never exceed 200 mV, and for the transmission signal, we can add an attenuator between the DUT and port 2 to meet the demodulator's dynamic range.

To sum up, the inductorless wideband integrated vector network analyzer is designed and devised into five main circuits. Each circuitry, including the directivity, image rejection, gain cells, receiver's, magnitude and phase detection circuitries, was designed to meet the requirements outlined in the previous chapter. The sub-blocks were simulated in a standalone

[31] The reference voltage is approximately the incident signal minus the coupling factor of the directive circuitry.

configuration and then validated in the corresponding circuitry context. Additionally, three blocks, including the polyphase filter for the LO quadrature generation, the low noise amplifier and the coupler, were measured in a standalone configuration, and their results were compared with post-layout simulations. Enhancements were made to improve their performance for the second circuit. The next chapter will present the circuit validation as a vector network analyzer demonstrator, where the DUT's parameter simulation will be compared with the extracted magnitude and phase output from the proposed VNA. The power management, layout, and SPI control of the final circuit will also be discussed in detail.

Chapter 4: AN INDUCTORLESS 0.2-30 GHZ VNA SYSTEM

In this chapter, the second thesis contribution will be presented, which is a complete vector network analyzer. Following this, the VNA full system characterization will be presented. Two devices under test will be introduced, where the first is a magnitude and phase tuner used to seek the complete VNA DC output's dynamic range in reflection mode.

The second device under test is a resonant LC circuit. For this second DUT and in the reflection mode, the outputs at the IF frequency of the receiver chain were processed and calibrated using a one-port calibration process to extract systematic errors and provide the corrected data. This data was then compared to the ideal response of this resonant circuit.

The same LC circuit is used for the transmission measurements. Finally, a complete system calibration, including the demodulator is presented. The implementation of this full calibration is a very complex process that involves the precise characterization of the demodulator transfer function. The implementation of such a complex calibration procedure falls beyond the scope of this thesis and is presented as one of the perspectives and future works derived from this Ph.D. thesis.

4.1 COMPLETE WIDEBAND INDUCTORLESS VNA CHIP

The implementation of a fully operational VNA has been achieved according to the structural approach depicted in Figure 108. The previously described circuit (Figure 31) was augmented by the inclusion of an SPI interface and registers, DACs, current to voltage (I to V) conversion circuits, Sensing points (BUS MONITOR) and additional switches to provide greater control over multiple points. These added blocs are summarized in Table 16. They were designed internally within the laboratory, and my involvement was limited to some specific customizations, schematic performance simulations and the management of the top layout of these cells.

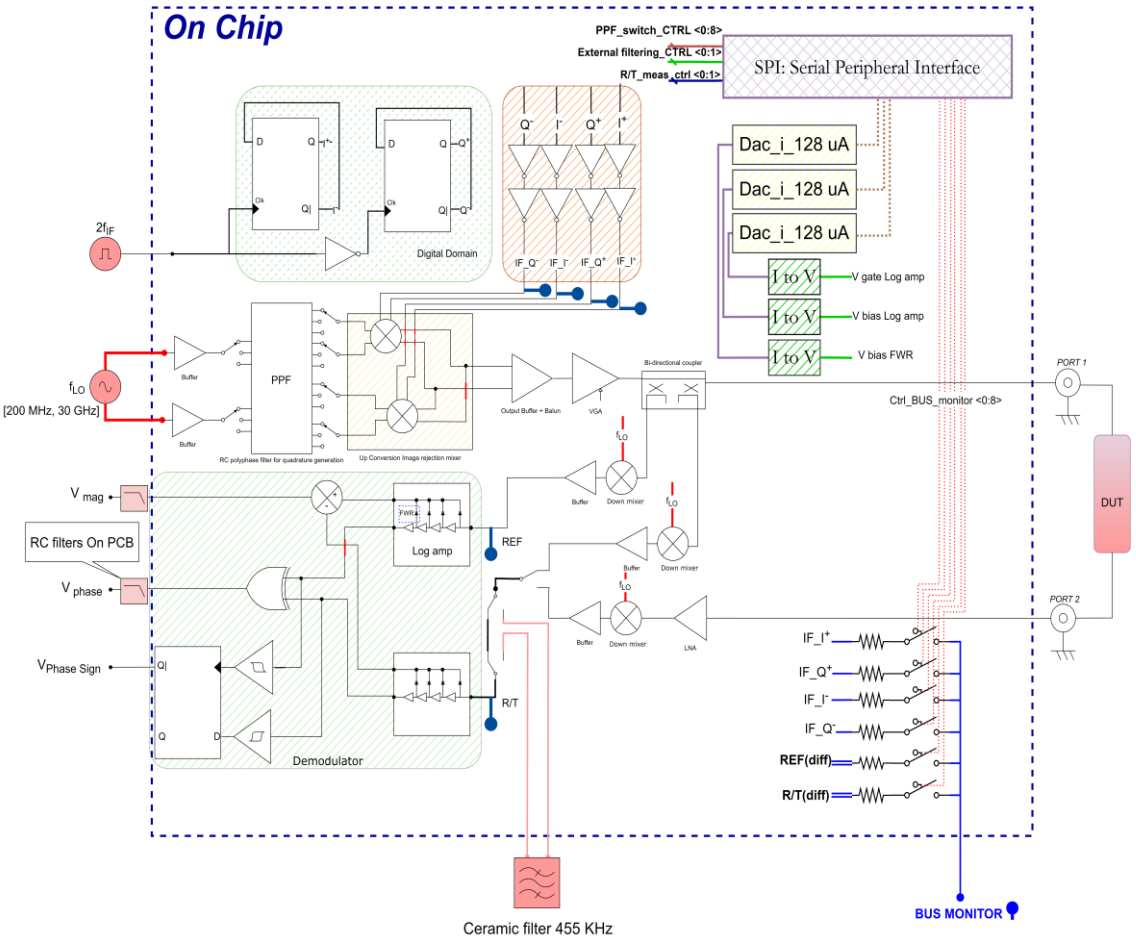
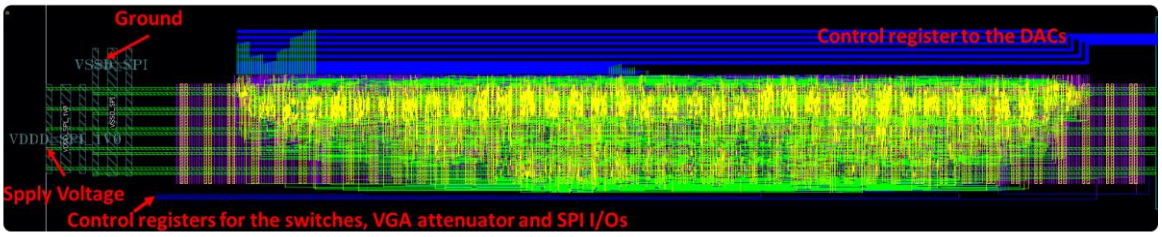


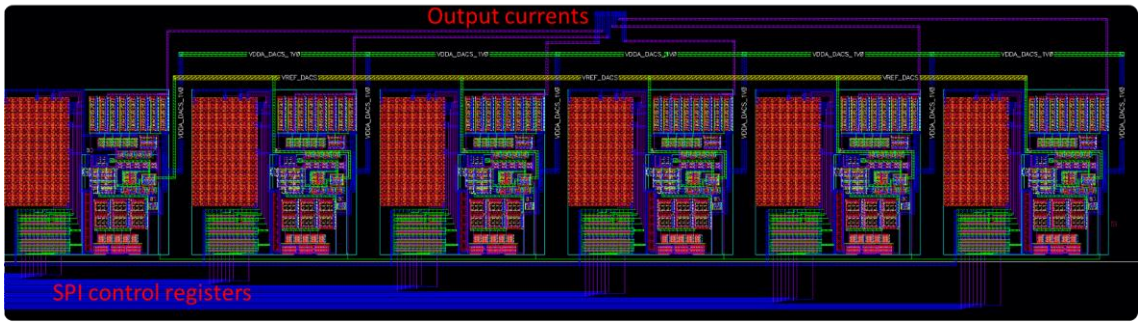
Figure 108 : Integrated inductorless VNA system circuit

Cell	function
SPI	SPI stands for Serial Peripheral Interface and it is a synchronous serial communication protocol used to transfer data between microcontrollers and peripheral devices. In SPI communication, there is a master device that controls the clock signal and a slave device that responds to the commands sent by the master, Figure 109 (a). It provides digital control capability through integrated 8-bit registers for the test blocks that are embedded on the chip, including switch control and also provides registers to the DACs.
DACs	Programmed thanks to SPI registers to provide a corresponding current output to bias the sub-blocks, Figure 109 (b).
I to V	Convert a current to a voltage to bias the full wave rectifier, limiting amplifier gate and tail current in the demodulator.
BUS monitor	Controlled by the SPI registers to sense at different key points in the IC, including IF quadrature outputs and the demodulator inputs at f_{if}, blue spots in Figure 108.

Table 16: The VNA circuit Control Cells



(a)



(b)

Figure 109: (a) Slave SPI Layout (b) DAC TOP contribution

Pin	*Name*	*feature*	*I/O Cell ESD protection*
1	VSSA	LO input Signal [200 MHz – 30 GHz]	PAVSS
2	INPUT_PLUS		None
3	VSSA		PAVSS
4	INPUT _MOINS		None
5	VSSA		PAVSS
6	VSSA	ground	PAVSS
7	AVDD_1V8	I to Supply voltages	PAVDD
8	AVDD_1V_DEMOD	Demodulator supply voltage	PVDDI
9	VDDA_DACS	DACS supply voltage	PANALOG
10	VSSA	Ground	PAVSS
11	SPI_CK	SPI clock	PBIDIR
12	SPI_CS	Chip select	PBIDIR
13	SPI_DIN	DATA IN	PBIDIR
14	SPI_RES	Reset	PBIDIR
15	SPI_DOUT	DATA Out	PBIDIR
16	*VDD_SPI_1V*	SPI Supply voltage	PVDD
17	VSSA	ground	PDVSS
18	VDD_IO_1V8	I/O supply voltages	PDVDD
19	CLK_IF_2x455KHZ	2x IF clock input for the I/Q generation	PBIDIR
20	V_MAGNITUDE	Magnitude DC output	PANALOG
21	V_PHASE	Phase DC output	PANALOG
22	VSSA	ground	PAVSS
23	OUT_PHASE_SIGN	Phase sign to resolve ambiguity	PANALOG
24	VSSA	ground	PAVSS
25	VSSA	ground	PAVSS
26	PORT II	The VNA second port	None
27	VSSA	ground	PAVSS
28	PORT I	The VNA first port	None
29	VSSA	ground	PAVSS
30	AVDD_VGA_1V	VGA Supply voltage	PVDDI
31	MIXER_RX_IN_PLUS	Reflected or transmitted signal from down mixer output to be filtered and then injected to the demodulation input	PANALOG
32	MIXER_RX_IN_MOINS		PANALOG
33	MIXER_RX_OUT_PLUS		PANALOG
34	MIXER_RX_OUT_MOINS		PANALOG
35	VSSA	ground	PAVSS
36	AVDD_1V	Supply voltage 1V	PVDDI
37	VREF_DACS	DC voltage reference for DACS set to 150 mV	PAVSS
38	BUS MONITOR	To sense several key points as mentioned in ***Figure 111***	PANALOG

Table 17: Input Output circuit pads

In Figure 111, the complete circuit layout is shown, which is enclosed in an I/O ring [32]consisting of 38 pads, as detailed in **Table 17**. The I/O ring was designed to include the RF domain, analog domain, supply voltages, and SPI control. Two tasks were assigned to this I/O ring: first, to establish a connection with a 32-Lead Plastic QFN packaging “QFN32” having 32 external pads and 6 extra pads linked to the QFN thermal/ground pad, and second, to enable measurements on probes with pads without packaging. To meet the requirements of both setups, the pad pitch was set to 100 µm with a pad area of 70 µm².

Additionally, a significant threat to electronic devices is posed by electrostatic discharge (ESD), which occurs when a charge is transferred from one object to another. When an integrated circuit (IC) receives a charge transfer that it is unable to dissipate quickly, a high current may pass through the IC within a brief period, resulting in severe damage such as junction burnout in silicon, which can be induced when an ESD transient of energy drives the junction into a breakdown. Furthermore, oxide breakdown can occur when a high voltage is applied across the oxide layer, causing dielectric breakdown and current conduction. This current flow generates heat, leading to the melting of the dielectric materials. Therefore, in each pad, as listed in Table 17, there are ESD protection cells available in the technology design kit, as illustrated in Figure 110. However, in the RF domain, the decision was made to proceed without ESD protection since it significantly reduces the bandwidth. In these RF pads, a metal filling pattern has to be added under the pad to fulfill fabrication metal density rules. The capacitive effect of this filling cell was simulated and considered in the following test bench.

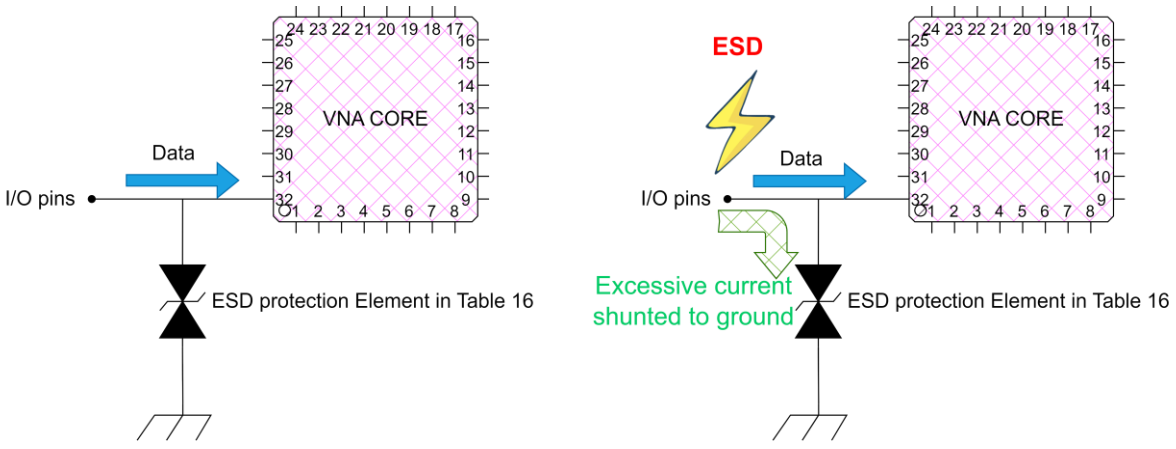


Figure 110 : Electrostatic discharge event with the ESD protection elements

[32] An I/O ring refers to the set of input and output cells located at the periphery of the chip. The I/O ring serves as the interface between the internal circuitry of the chip and the external packaging.

The system on chip, as depicted in Figure 111, has a compact design, taking up a surface area of 1370 µm by 1470 µm. Despite being submitted for fabrication nine month before the writing of this thesis rapport, the circuit has not returned yet from the foundry, delaying any further progress in measurement. However, to assess the system's performance, post-layout simulations have been done on the full system VNA circuit that allow to validate its functionality. These simulations will provide a comprehensive evaluation of the system's capabilities. **Note that the circuit simulation test bench used does not incorporate the external ceramic IF filter, and therefore assumes a default simulation IF frequency of 500 KHz, resulting in an intermediate frequency bandwidth (IFBW) equivalent to this value**.

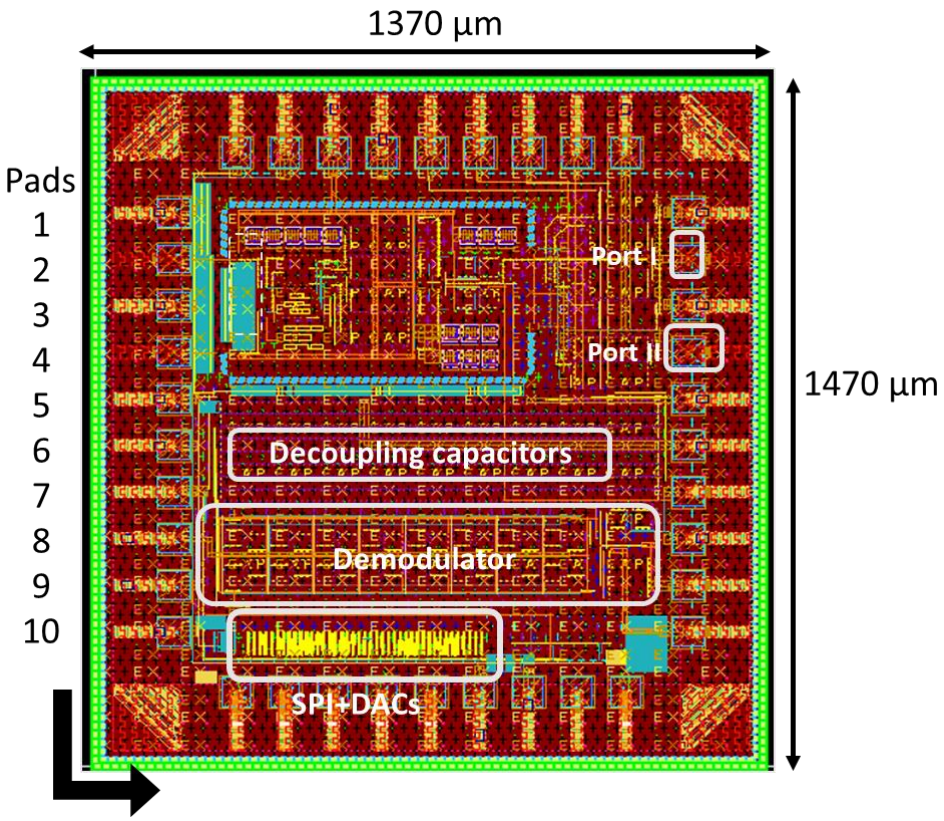


Figure 111 : Complete VNA layout including I/O ring

4.2 VNA CHIP TEST BENCH

Figure 112 illustrates the configuration of the test bench, which includes all the VNA IC building blocks except for the SPI and DACs. To replace the SPI, custom 7-bit registers called "dec2bin" were utilized, which provide control bits by converting decimal values into binary values for easier integration with the analog simulator. The DACs were substituted with current sources I_{DAC} from analoglib, which fed the "I to V" circuit used locally at the different

circuits to generate the bias and control voltages. Note that the simulated RF I/O's parasitic capacitance was 16 fF, and this capacitance was taken into account in all subsequent simulations.

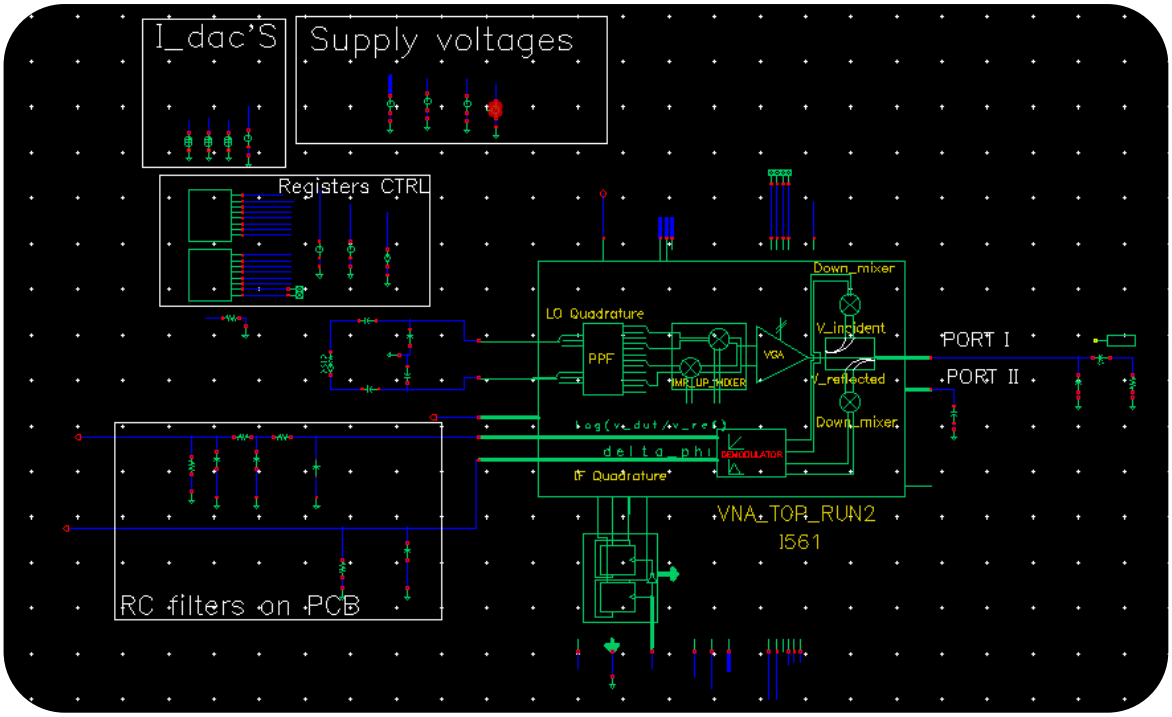


Figure 112 : VNA demonstrator test bench

The system described in Figure 112 draws a total current of 132 mA from a 1 V supply voltage. **Table 18** summarizes the power consumption of the circuit, with nearly one-third of the total power consumption attributed to the three blocks.

Blocks	Power consumption	unit	comment
Variable gain amplifier + LNA	44.57	mW	For 1 V supply. The supply voltages of the three groups have independent pins in the proposed circuit
Magnitude and phase detector	41.63	mW	
Receiver's, up conversion mixer, buffers and drivers	48.09	mW	

Table 18: Circuit power consumption

As previously mentioned, the circuit utilizes three “I to V“ (current to voltage converters) blocks to generate three biasing voltages for the logarithmic amplifier gate input, the limiting amplifier current tail biasing and the full wave rectifier current tail biasing. The first I-to-V block, with a DAC current of I_{DAC1} 33 µA, produces a logarithmic amplifier gate input voltage of 499.12 mV. The second I-to-V block, with a DAC current of I_{DAC2} = 30.9 µA, generates a limiting amplifier current tail biasing voltage of 400.12 mV. Finally, the third I-to-V block, with a DAC current of I_{DAC3} =29.1 µA, produces a full wave rectifier current tail biasing voltage of 449.7 mV.

The output power at port 1 is shown in Figure 113 and ranges from -0.2 dBm to -4.2 dBm. However, there is a deviation from the gain circuitry test bench result (Figure 80) where a 0 dBm output is obtained across the exact bandwidth. This deviation is due to the mismatch caused by the LO input and RF output I/O parasitics, as depicted in Figure 114. The output return loss is shown to vary within 2 dB from the initial pad-less circuit above 24 GHz. Although this variation impacts the coupler directivity, it could be corrected with calibration, as explained in 1.1.4, since it is a systematic VNA error. Alternatively, the output power could be improved by raising the LO input power typical value of -4 dBm to a higher value. As noted in the system study (2.1), there is a margin of 4 dBm until reaching the maximum stimulus power of 0 dBm.

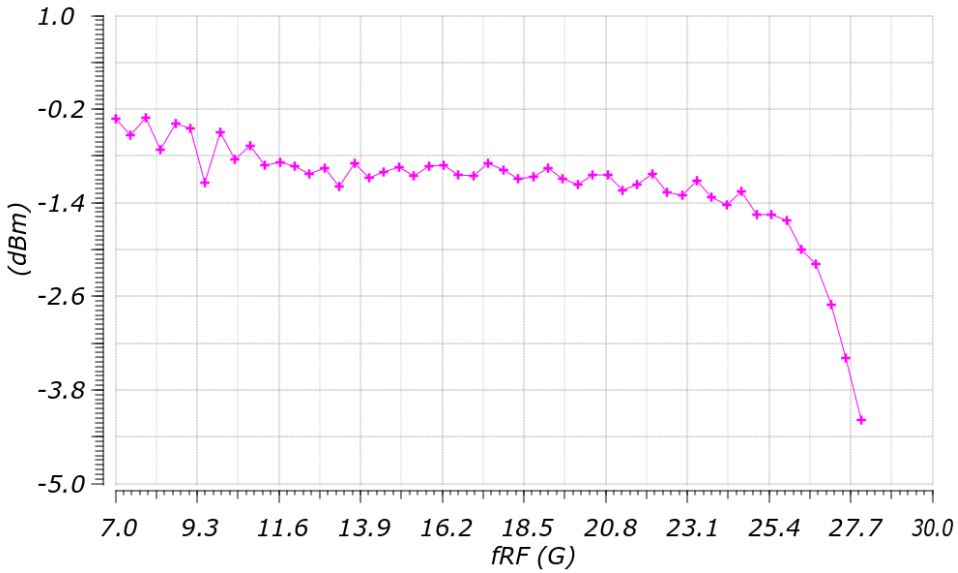


Figure 113 : Port I output Power including I/O parasitics at fRF=[FLO+fIF]

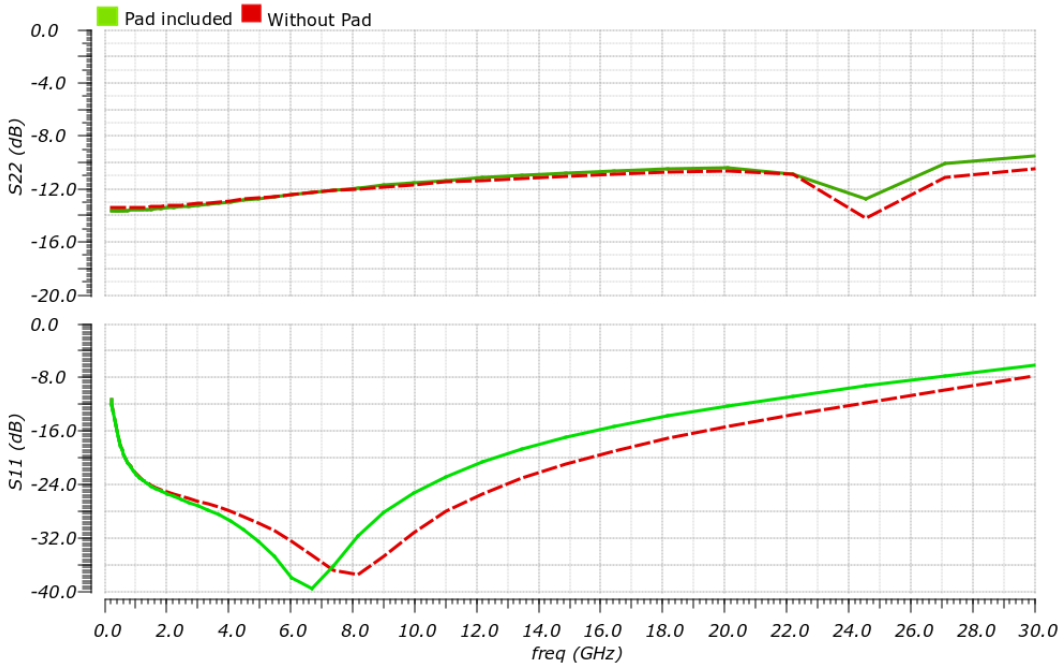


Figure 114 : Input and output return losses with and without pads

To verify the VNA circuit operation in reflection measurement mode, two devices under test were involved. The first one uses a load model that tunes two parameters: SWR and phase for a given frequency. This approach validated the VNA magnitude and phase dynamics and demonstrated their independence from each other. The second device under test aimed to validate the proper functioning of the VNA system by introducing an LC circuit at port 1 of the integrated VNA circuit, for reflection mode measurement. This device will be called DUT2. The ideal S-parameter DUT2 response was compared with the receiver's output and the corrected response after a one-port calibration process. Similarly, the same DUT2 is used between port1 and port 2 of the integrated VNA circuit to validate the transmission measurement mode. In this way, a comparison was done for the simulated DUT2 S_{21} response with the receiver's and demodulator's responses in transmission mode.

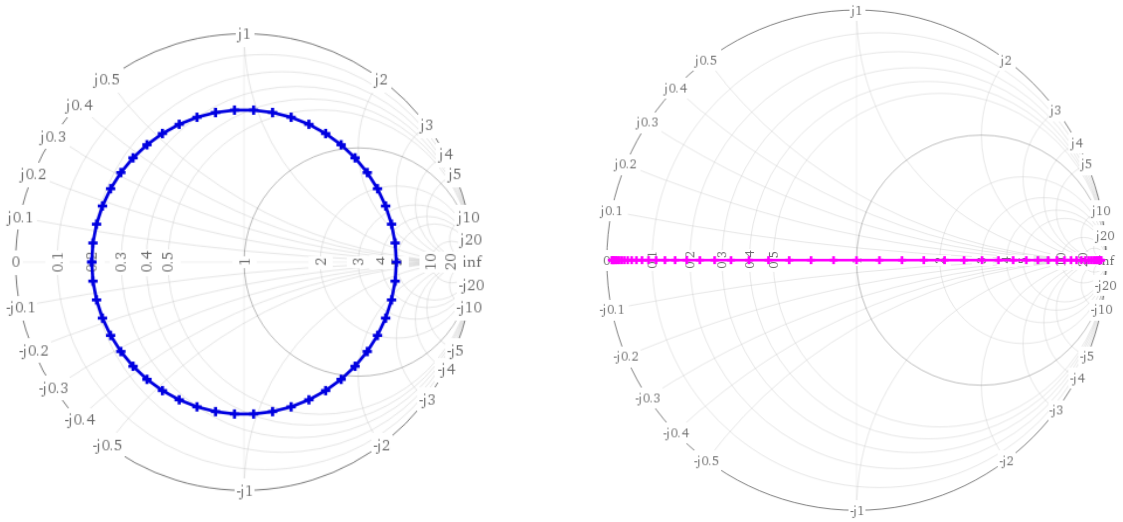
Considering the post layout simulation process, a harmonic balance simulation was utilized, where the IF frequency was set to 500 KHz instead of 455 KHz, to address convergence issues. The LO frequency was swept from 7 to 30 GHz, equivalent to the third polyphase filter bandwidth (3.3.1). While the two other bandwidths were also verified, the third one was considered more critical due to its operation at high frequencies. The DC outputs were the 0 Hz harmonic, computed from a HB simulation. The IF harmonic at 500 KHz was the receiver's

output. A two tone harmonic balance was conducted and took a considerable amount of time to converge, where the first tone is the IF frequency (10 harmonics) and the second one is the LO frequency (5 harmonics). Ultimately, many aspects of the system test will be completed during the measurement campaign, as discussed in the perspectives of this thesis work.

4.2.1 Reflection Mode

4.2.1.1 DUT1 reflection measurement demodulator included

When measuring the reflection coefficient, the term "Standing Wave Ratio" (SWR) provides a quantitative measure of the degree of mismatch between the impedance of the output stage and that of the load. The SWR can be calculated by using the formula SWR = (1 + |Γ|) / (1 - |Γ|), which involves the reflection coefficient (Γ). A low SWR indicates a good match, whereas a high SWR indicates a poor match to the characteristic impedance of 50 Ω.Figure 115 illustrates the response of a customized SWR and phase tuner, namely DUT1. The purpose of this DUT is to enable navigation on the Smith chart at a specific frequency.

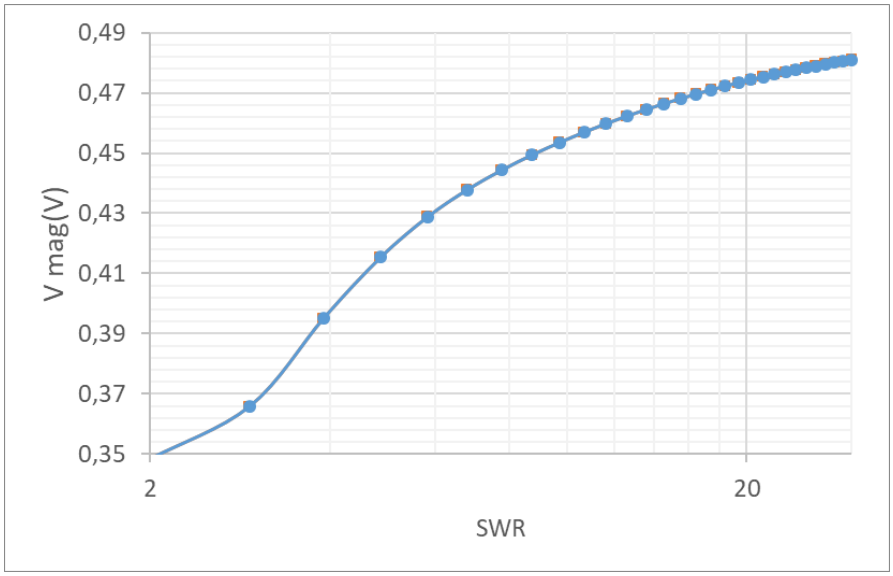


(a) (b)

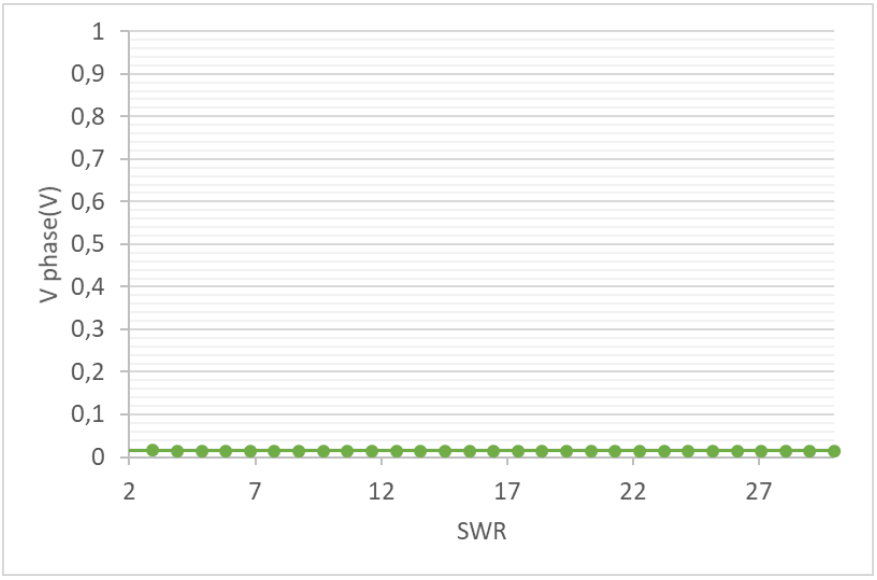
Figure 115 : DUT 1 (a) phase variation at swr=5 (b) swr variation with a fixed phase=0

In this section, the SWR and phase of the device under test will be tuned, and the magnitude and phase outputs of the demodulator will be analyzed. For this purpose, two harmonic balance simulations were carried out to exhibit the system's magnitude and phase dynamics over the SWR variation. As depicted in *Figure 116*, the magnitude output voltage V_{mag} undergoes a variation of up to 150 mV over the SWR range of 2 to 30, while the phase

output V_{phase} remains unchanged throughout the range. Moreover, by increasing the input local oscillator (LO) power, the VNA system output magnitude dynamic range of 150 mV (from 335 to 490 mV , for 200 mV LO voltage) could be expanded to achieve the maximum DR of the demodulator of 425 mV (335 to 760 mV), as previously simulated in Figure 106.



(a)

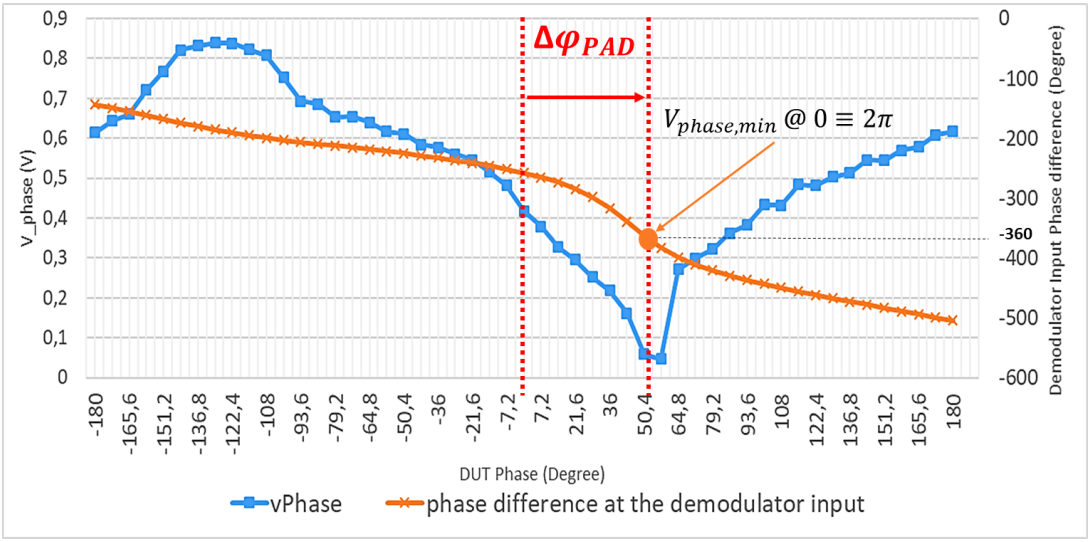


(b)

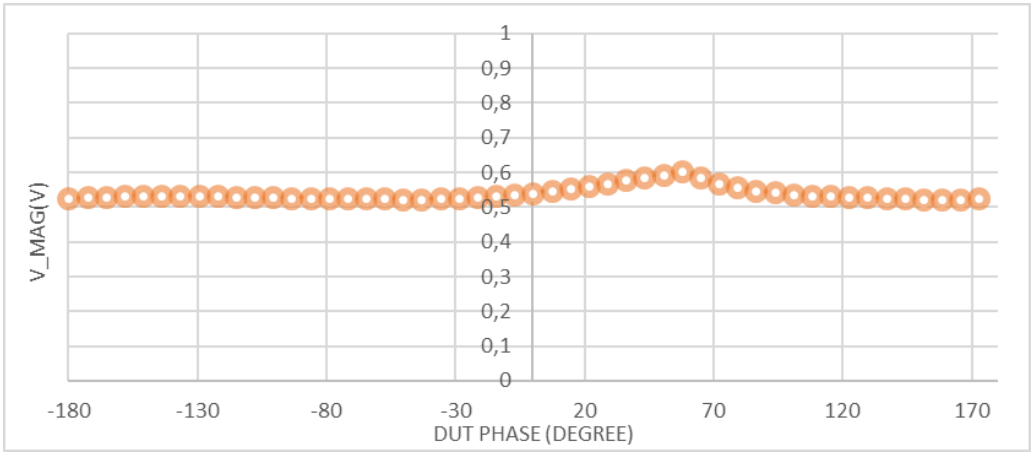
Figure 116 : DUT SWR Variation @15GHz: (a) Magnitude output semi logarithmic scale (c) phase output

In the second harmonic balance simulation, a variation of phase DUT_{phase} is made from -180° to 180 °. From the analysis of the results in Figure 117, it was deduced that the demodulator input phase difference between the reference and reflected signals at the intermediate frequency exhibits a variation of 361.33°, ranging between -143.31 and -504.64

degrees. The observed variation in the difference corresponds to that of the Device Under Test. However, it was noted that a shift of $\Delta\varphi_{PAD}$ from 0 was observed due to the presence of the output RF pad at port I. The minimum output voltage $V_{phase,min}$ was found to correspond exactly to -360 ° (equal to 0 °≡ 2Π). These results confirm the effective performance of the transmitter and the two receivers (reflection and incident path), and secondly, the performance of the demodulator. In addition, the results reveal the VNA system's phase dynamic range to be 800 mV over the 360 degree phase shift. Finally, the impact of the pads could be embedded through calibration during the measurements. The magnitude output V_{mag} remains constant over the phase variation, Figure 117 (b).



(a)



(b)

Figure 117 (a) demodulator phase difference input and the corresponding DC phase output signal. (b) magnitude output over the phase variation.

These presented results suggest that the VNA system can provide direct reflection coefficient measurements through both v_{phase} and v_{mag} readings, with promising magnitude and phase dynamic ranges. Afterwards, as the impact of pads on the VNA system performances was observed, in particular its effect on the phase response shift and output magnitude DR, a one port calibration will be conducted in the next section for the DUT2. This is done first to de-embed the pads effect, and secondly to suppress directivity, tracking, and port matching errors, as previously explained in 1.1.4.1. During the calibration process, the receiver's outputs (reference and reflection signal ratio) at f_{IF} will be compared to an ideal S parameter response.

4.2.1.2 DUT2 reflection corrected measurement (Demodulator not included)

4.2.1.2.1 One port Calibration implementation

The One-port calibration process involves the use of a calibration kit that includes three known standards, such as a short, an open, and a load in order to resolve the system of three equations shown previously in (11). Afterward, the system of three equations is solved, where the three errors are the unknown parameters, and the ideal reflection coefficients are set to 0, -1, and 1 for the short, open, and load, respectively. The mathematical expression for the three errors is presented in Appendix 1.Then, the corrected data $\Gamma_{\text{Corrected DUT}}$, is obtained by applying corrections to the measured data,Γ_{meas} to remove the effects of any systematic errors introduced by the VNA or the measurement setup. In (26), $\mathrm{E_d}$, $\mathrm{E_{sm}}$, and $\mathrm{E_{rt}}$ denote the directivity, source match, and reflection tracking error, respectively.

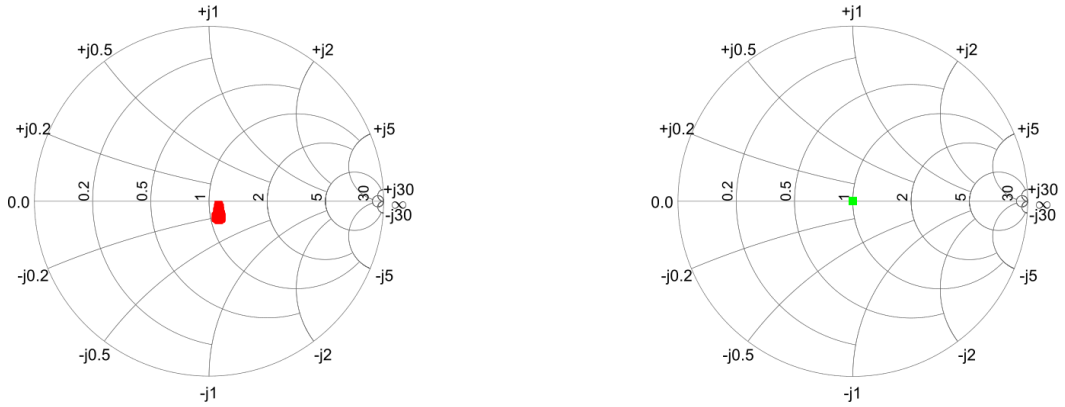
$$\Gamma_{\text{Corrected DUT}} = \frac{\Gamma_{\text{meas}} - \mathrm{E_d}}{\mathrm{E_{sm}}(\Gamma_{\text{meas}} - \mathrm{E_d}) + \mathrm{E_{rt}}} \tag{26}$$

The proposed VNA system[33] was calibrated using a three-step process where the circuit was simulated using harmonic balance in three setups. The first setup involved an open loaded test bench, the second setup involved loading the circuit with a ground, and the third one

[33] Without demodulator

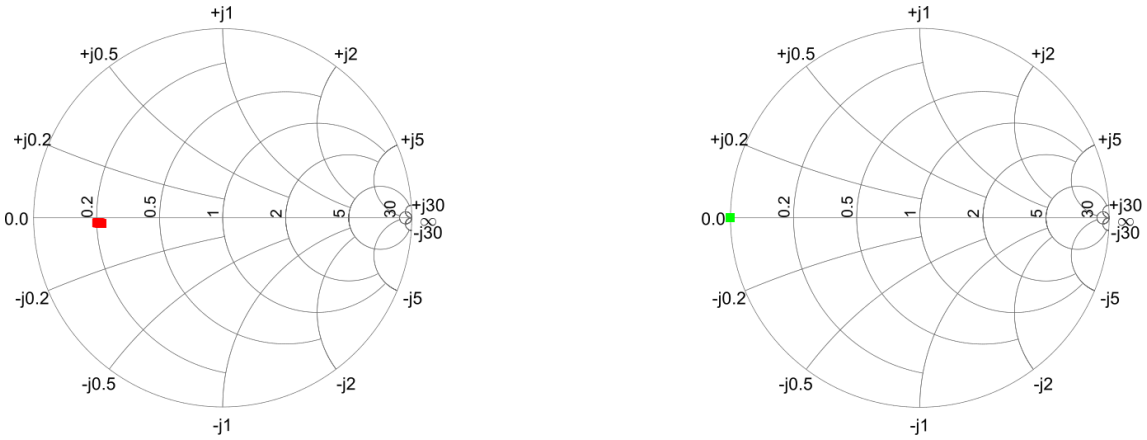
involved loading the circuit with a 50 ohm load. The receiver's outputs, including both magnitude and phase, were saved and processed using MATLAB for analysis.

For the match loaded circuit, as depicted in Figure 118, the corrected reflection coefficient includes the point (0, 0), which is the reflection zero point, where the load is matched with the characteristic impedance of 50 Ω. For the short circuit, as a load, Figure 119 presents a circle centered at the coordinate (0, 0) and has a radius of 1. For the open-circuit load, as depicted in Figure 120 the circle degenerates to a single point (centered at 1, 0 and with a radius of 0). This corresponds to a maximum reflection coefficient of 1, at which the entire incident wave is reflected totally.



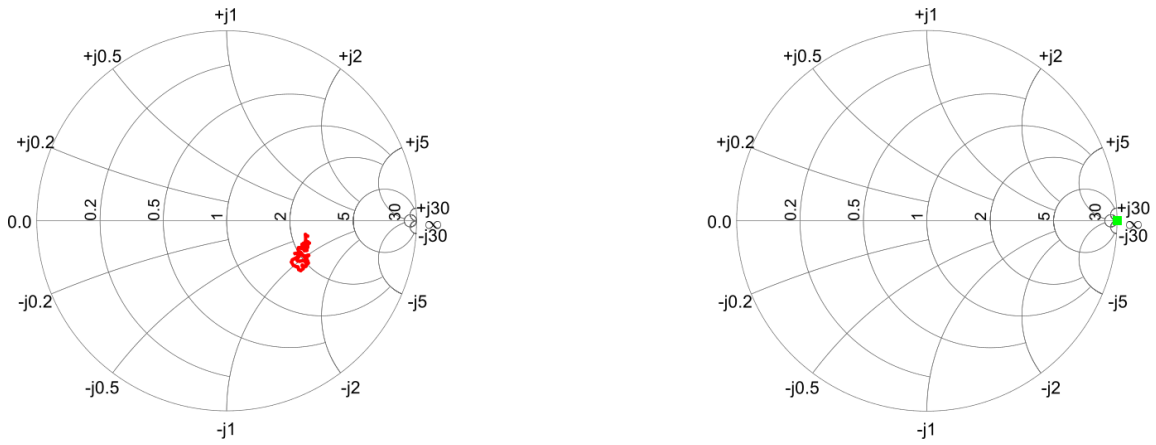
(a) ***(b)***

Figure 118: smith chart plot for 50 ohm load DUT (a) recievers output ratio at flf (b) corrected response



(a) ***(b)***

Figure 119: smith chart plot for a short DUT (a) recievers output ratio at flf (b) corrected response



(a) ***(b)***

Figure 120 smith chart plot for an open DUT (a) recievers output ratio at fIf (b) corrected response

4.2.1.2.2 DUT2 reflection measurement after calibration

To validate the design a test load has been used to compare results of the proposed VNA system with an ideal S parameter simulation. As illustrated in Figure 121, the second device under test consists on an LC resonant circuit that resonates at two frequencies at 12 GHz and 28 GHz.

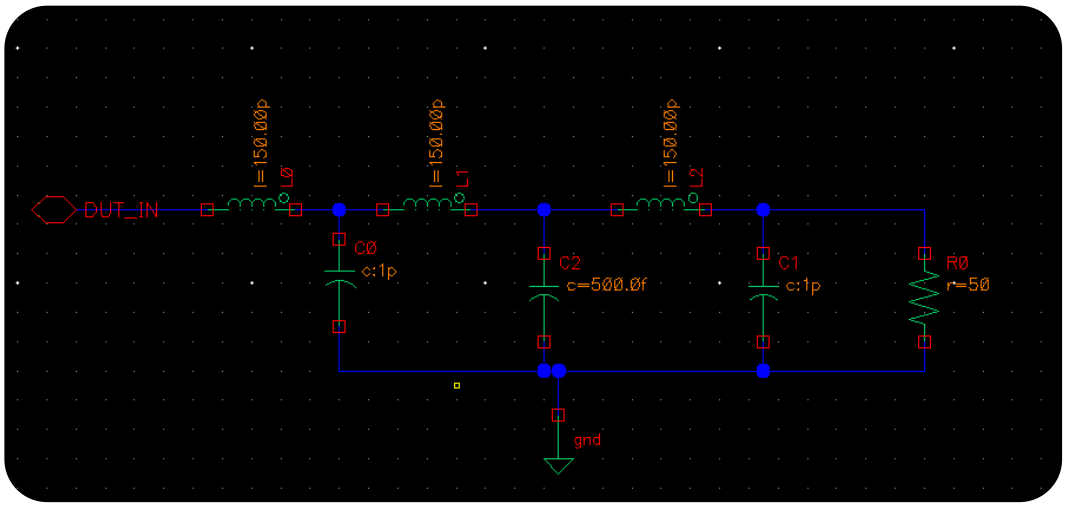


Figure 121: LC circuit DUT2, loaded with a 50 ohm load for the S11 measurement, for the S21 measurement this load is removed

In the first validation study, the system was evaluated without the demodulator. The scattering parameter S11 response (ideal response) was compared to the reflected and incident wave for both magnitude ratio and phase difference at the receiver's output.

Figure 122 and Figure 123 shows the magnitude and phase of the receiver's response (reflected divided by the incident signal at f_{if}) before and after calibration, respectively. Given that the post-calibration and ideal response results are in complete agreement, it can be concluded with confidence that our approach is valid.

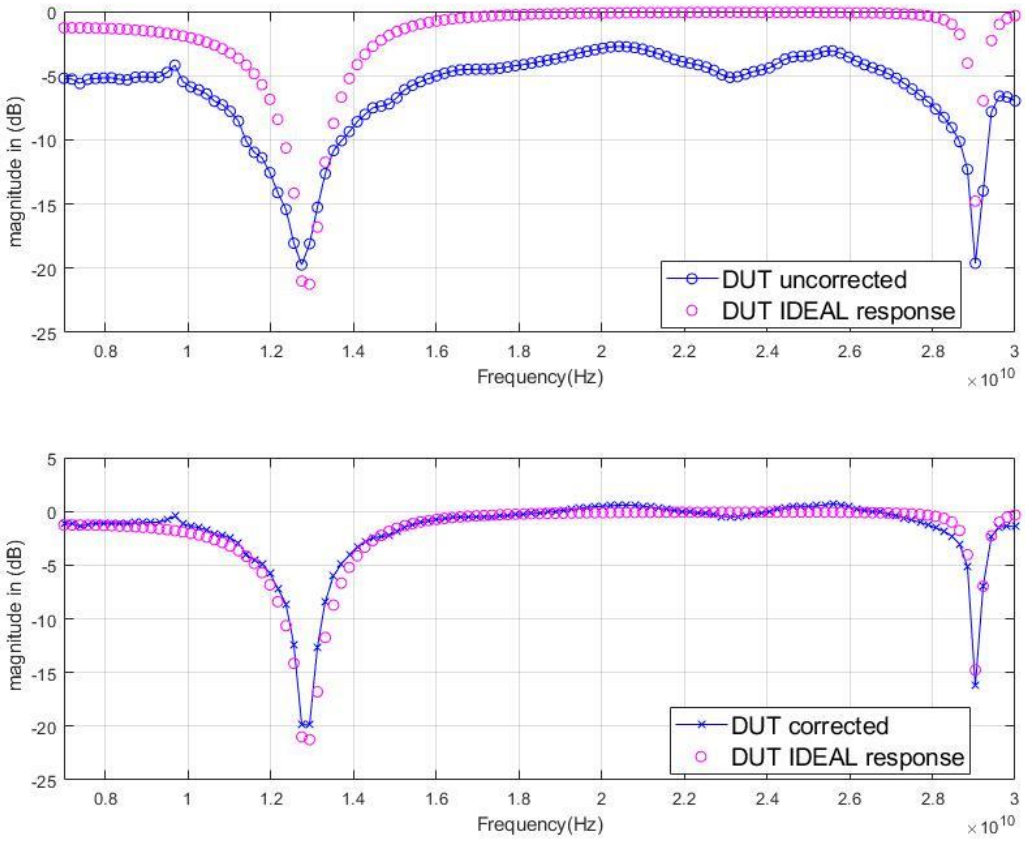


Figure 122 : LC DUT magnitude response before and after calibration with an ideal S parameters response comparaison (120 points)

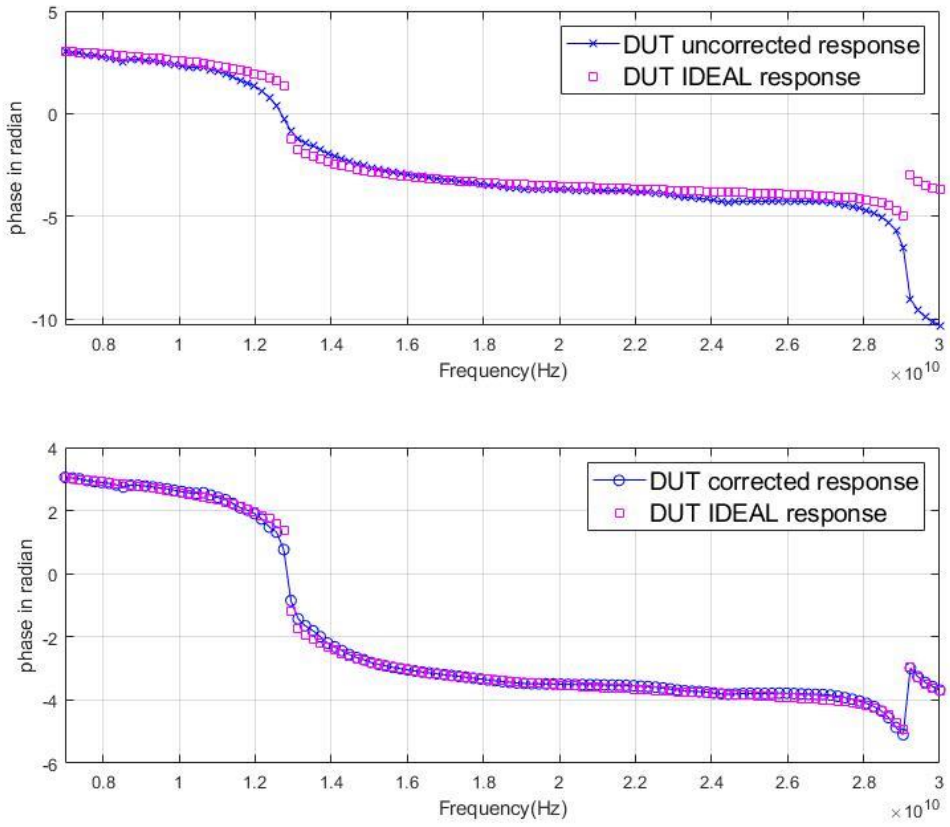


Figure 123 :LC DUT phase response before and after calibration with an ideal S parameters response compraison (121 points)

It has been observed that reducing the LO frequency step size leads to a significant reduction in the error between ideal and corrected data, which aligns with the conclusion drawn in Chapter 2. Figure 124 highlights that in areas of high variation (dotted areas corresponding to magnitude picks and important phase variations), errors are more noticeable when using a larger frequency step size of 0.19 GHz (due to the high time consuming simulations).

During the circuit test, the LO frequency step will be tuned within a frequency range to reduce the VNA errors. The minimum frequency value should be set at 455 KHz, which is the default IF frequency, while the maximum frequency should be set at 1MHz, which is the highest frequency that the IF quadrature generator can produce. Selecting an appropriate frequency step size within this range will lead to optimal accuracy and consistency of measurements, as discussed in details earlier in 3.3.

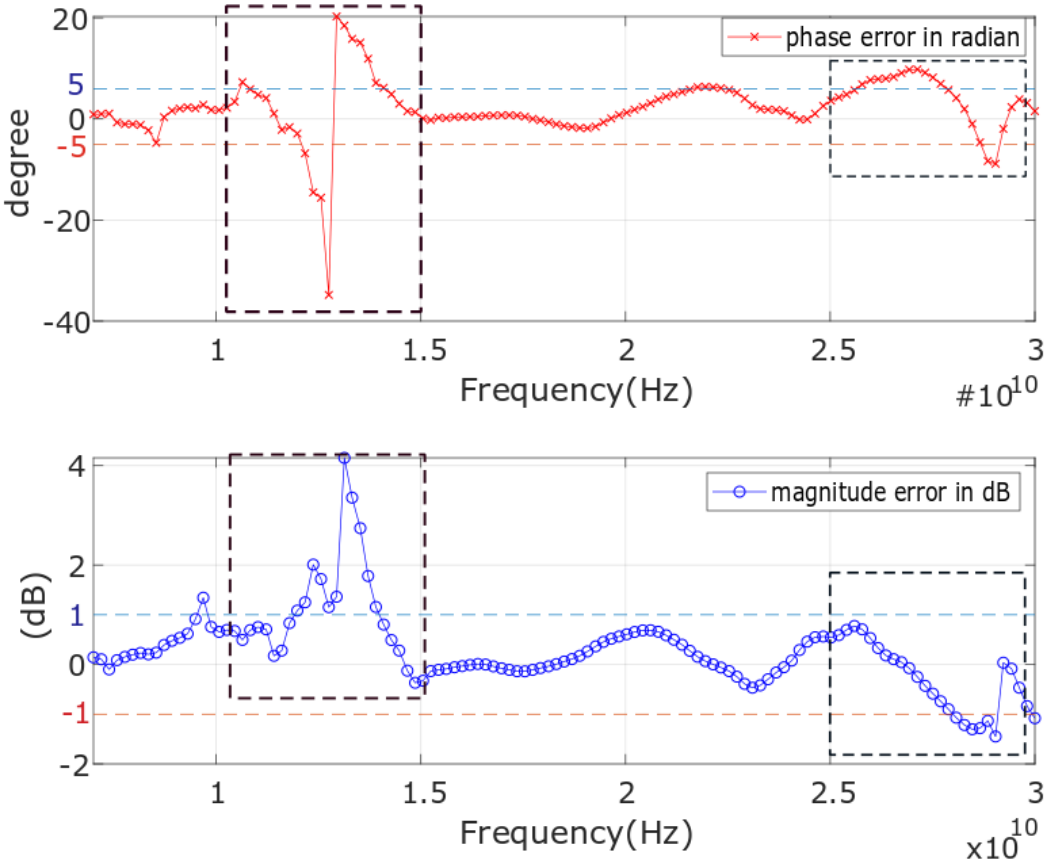


Figure 124 : magnitude and phase error from [7-30 GHz] (121 points), frequency step of 0.19 GHz

4.2.2 TRANSMISSION MODE: DUT2 MEASUREMENT

In terms of the magnitude of transmission measurement on DUT2, as illustrated in Figure 125, the main two peaks at 12 and 28 GHz were observed in the initial S21 inspection at the receiver's output. However, it was not possible to provide further information in terms of errors compared to the ideal response, since no correction has been performed. The interesting aspect is that the receiver's magnitude ratio adheres to the demodulator's magnitude response.

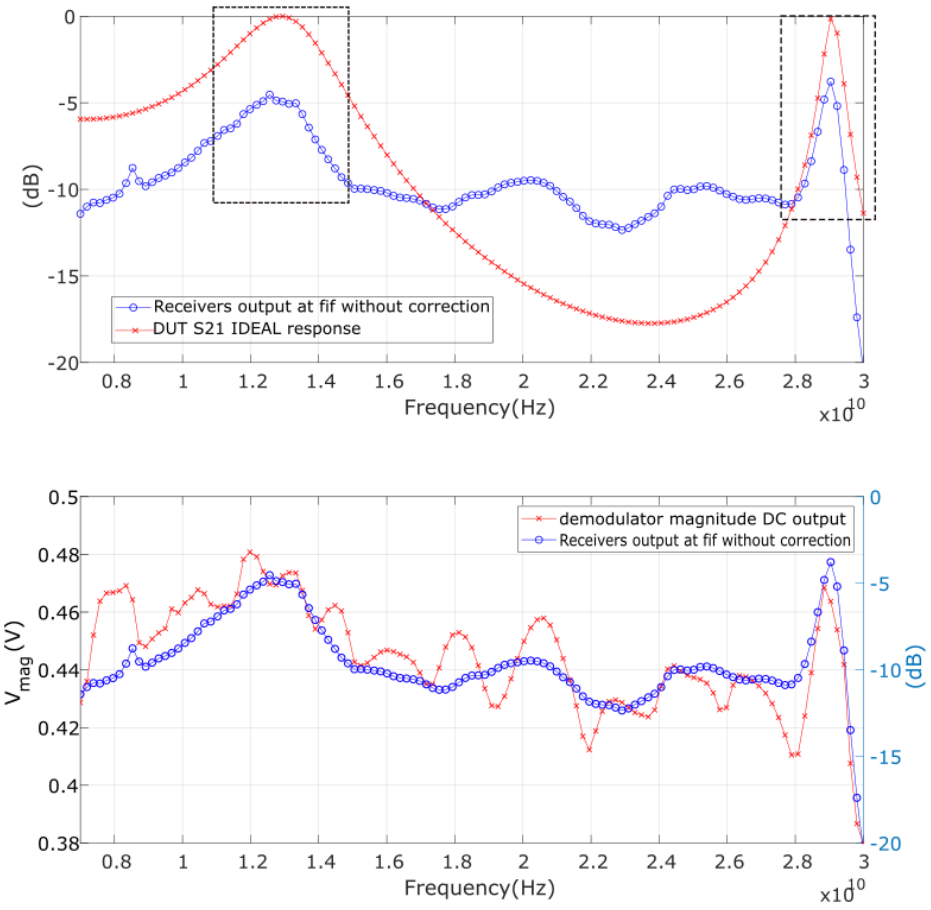


Figure 125 : (Top) ideal S21 response Vs the receiver's output at Fif, (Bottom) demodulator magnitude output compared with receiver's output at Fif

Figure 126 depicts that the phase variation trends track the phase receiver's output and the ideal response, but no further conclusions can be drawn. Nevertheless, the phase difference at the demodulator input correlates with the magnitude of v_{phase}, as depicted in Figure 127. Indeed, this phase difference at the receiver's output at f_{if} is a continuous variable that ranges between -180 and 180 degree. At the zero crossing, the detector output exhibits the lowest magnitude value of 9.8 mV, whereas at the -180° and 180° degree crossings, the detector output exhibits the highest magnitude value of 836 mV and 838 mV, respectively. In addition, for the -90 0 and 90 degree crossings, the magnitude settles at 414 mV and 413 mV, respectively, which corresponds to the mid-value of the phase output dynamic range (≈ 838/2) mV. Notably, these values are consistent with the detector only characterization results presented in Figure 100.

In addition, the phase sign output $v_{phase\ sign}$ is consistent with the phase output v_{phase} variation. Indeed, the sign voltage $v_{phase\ sign}$ is equal to 1 when the phase difference

between the transferred and reference waves is positive and equal to zero if it's the opposite. As a conclusion, the adopted patented approach for phase sign resolution is validated.

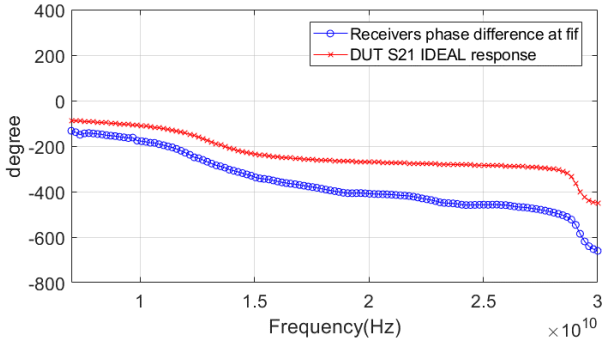


Figure 126 : Receiver's phase output at Fif and ideal S parameter response whitout calibration

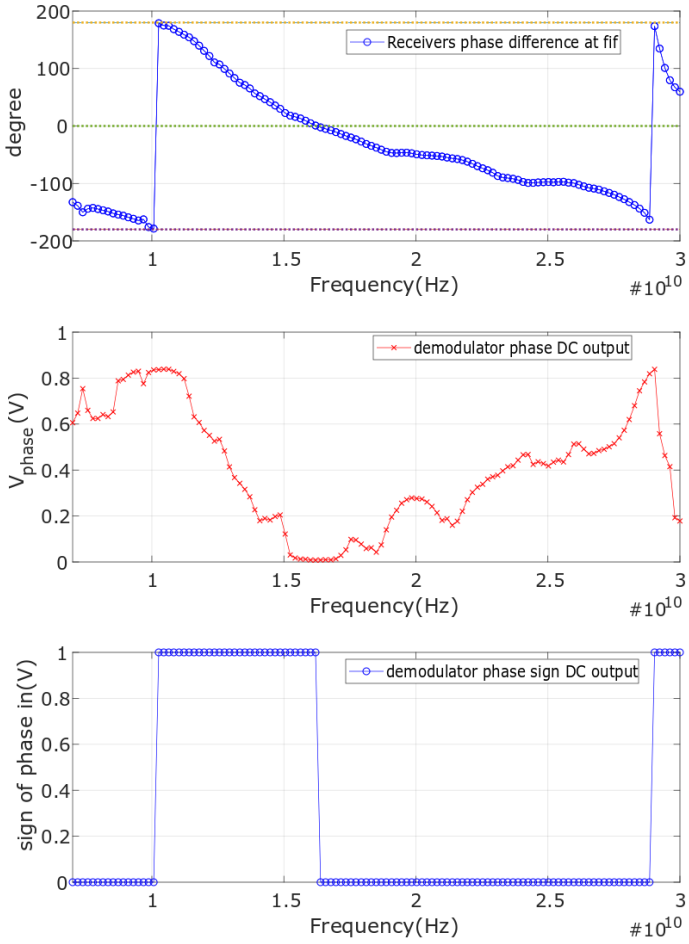


Figure 127 : Wraped receiver's (tranmission and inicident signals) phase output [-180 180 °] at Fif and the corresponding demodulator v_{phase} and $v_{phase\ sign}$ outputs

4.3 COMPLETE VNA SYSTEM CALIBRATION

The previous sections (4.2.1 and 4.2.2) validate the proposed system functionality as a VNA. However, to calibrate **the complete VNA system including the demodulator**. A different calibration process is needed, taking into account the following relationship between the reflection parameters and the outputs of the demodulator.

$$\begin{cases} V_{gain}(mV) = V_{slp}(\dfrac{mV}{dB}) \log\left(\dfrac{V_{reflected}}{V_{incident}}\right) = \dfrac{V_{slp}}{20} S_{11,dB20} \\ V_{phase}(mV) = V_{\phi}(\dfrac{mV}{degree})\, S_{11,phase}(degree) \end{cases} \quad (27)$$

In a first place, from the transfer function (27) and the measured v_{mag} and v_{phase} , we will be able to go back to the measured $S_{11,dB20}$ and $S_{11,phase}$. Then, we can make a calibration like the one done in the previous section (one port calibration error system in (11)).

To enhance the calibration procedure accuracy, the magnitude and phase transfer function of the demodulator sub-system must be precisely characterized. A polynomial equation that is dependent on temperature variation and logarithmic amplifier response mismatch could be used to approximate both transfer functions (27). This precise characterization can be achieved through measurement by characterizing only the demodulator, as shown in Figure 128.

After the demodulator characterization, the polynomial transfer function can be implemented in MATLAB, and the complete VNA can be calibrated to set the $v_{mag,load,ideal}$ at the demodulator sensitivity level, and the $v_{mag,short,ideal}$ to the demodulator DR midrange and the $v_{mag,open,ideal}$ to the maximum demodulator DR.

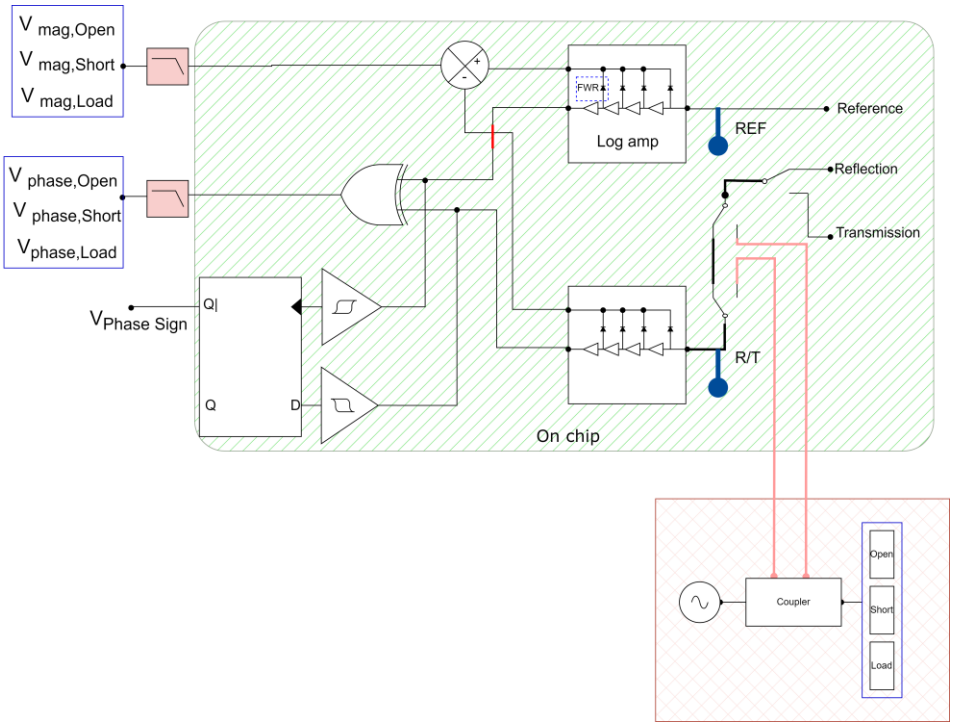


Figure 128 : Setup to extract the three ideal demodulator magnitude and phase responses to know standards (Open, Short,Load)

4.4 CONCLUSION

This chapter presents a post layout simulation results of the wideband inductorless Vector Network Analyzer (VNA) chip. The power consumption of each circuit block is discussed in detail. The input and output matching impedances are also analyzed. In reflection mode, two devices under test (DUTs) are used. The first DUT is an SWR and phase tuner that wipes the Smith chart, while the second DUT is an LC resonator. The first DUT is used to demonstrate the demodulator's dynamic range for the magnitude and phase outputs, as well as the independence of the demodulator output. The second DUT is used in conjunction with a one-port calibration at the IF outputs to compare the S11 parameters after calibration with the ideal DUT response. In transmission mode, the same LC DUT is used to verify the IF and demodulator outputs and to verify the proper functioning of the direct phase ambiguity resolution. Finally, a complete VNA system calibration proposal is presented.

Based on the initial results, in reflection mode, the first device under test, proves the well-functioning of the demodulator; both output voltages V_{mag} and V_{phase} vary with the SWR

and phase tuning independently. The second device under test shows, after one port calibration, that the corrected S11 meets the ideal DUT S parameter response in both phase and magnitude.

Otherwise, in transmission mode, the S21 parameter should be corrected using the two port calibration procedure. This is proposed as a future work. In spite of the non-calibration, the post layout simulation results presented in this chapter show that the demodulator output correlates well to the receivers' output amplitude ratio (transmitted signal over reference signal) and phase difference between transmitted and reference signals. These results validate the correct operation of the integrated VNA transmission mode. Furthermore, these results also validate the patented direct phase sign detection technique that has been introduced in this thesis.

GENERAL CONCLUSIONS & PERSPECTIVES

In the following, all the major results presented in the previous chapters are summarized, before discussing perspectives of future works.

This thesis started with the exploration of several promising applications using the vector network analyzer for noninvasive characterization. Figure 1 gathers more than forty recent articles in several domains that point to the common key element to integrate a sensor, which is a vector network analyzer. This initial study highlights the need to implement a **compact** and **low cost** VNA that can cover several frequencies of interest. To reduce the size, the challenge was to design a **wide bandwidth** VNA circuit with **no inductive** components. To implement this circuit, intermediate objectives were set in the general introduction (page 20).

We will highlight the different initial objectives and the degree that they have been achieved during this thesis. Firstly, a detailed understanding of the block diagram of the proposed broadband vector network analyzer architecture has been achieved. The main novelty of this architecture is the integration of the demodulator module. This allows a direct phase and magnitude measurement replacing an external post processing from the IF outputs as was done in the existing approaches, as discussed in Chapter1. Secondly, the proposed block diagram was analyzed thoroughly in Chapter 2, considering factors such as sensitivity, power, and noise. The results of this analysis have allowed to find the specifications for different building blocks as well as general VNA design choices including IF frequency and IF bandwidth. Thirdly, the individual sub-blocks of the circuit have been designed at transistor and layout level, and their performance has been successfully validated through post-simulation and measurement results[34]. Two different test chips have been designed and fabricated. The first one contains standalone building blocks and the second one is the full integrated VNA. The measurement results of the first circuit are included in Chapter 3. They have allow to validate the first version of the most critical building blocks and introduce some improvements in the second version included in the full VNA circuit. Unfortunately, the delays

[34] Three key blocks including coupler, LNA and polyphase filter

in fabrication time have prevented us to measure the circuit before the end of the PHD thesis. Nevertheless, the circuit's overall functionality as a vector network analyzer has been validated through post layout simulation of the second integrated circuit, including external calibration[35], as shown in Chapter4. These achievements represent significant contributions to the field of non-invasive characterization, paving the way for future advancements in the design and implementation of an improved version.

Initial comparison with the state of the art

The separation architecture adopted in this thesis was initially compared with the state of the art presented in section 1.2 in Table 19. The comparison includes two main contributions involving Infineon's SiGe 0.35 µm bipolar technology [67], [69, p. 32]. The first contribution is a vector network analyzer (VNA) that covers the 50 to 100 GHz bandwidth and integrates the stimulus and receiver's front end on a 4 mm x 3 mm area [67]. The system dynamic range (DR) was measured, ranging from 55 to 72 dB, nearly equal to the receiver's DR. The VNA sensitivity for reflection measurement is set to -20 dB with an error of phase and magnitude equal to 0.3 degree and 0.3 dB, respectively. The second contribution covers a frequency range of 4 to 32 GHz and also includes a stimulus in a 4 mm x 4 mm IC surface [69, p. 32]. The system DR ranges from 44 to 77 dB, and the receiver's DR ranges from 82 to 101 dB. The VNA sensitivity in terms of reflection is -20 dB and -60 dB in transmission mode. The VNA accuracy is measured with a 30 dB attenuator as a device under test, and the mean values of phase and magnitude error are 1.29 degrees and 0.17 dB, respectively. The third contribution covers nearly the same frequency bandwidth as the second contribution (0.01-26 GHz), but the source is not integrated into the circuit [73]. Therefore, the system's DR could not be measured. However, the receiver's DR is up to 129 dB with a -30 dB minimum detected reflection. The VNA phase and magnitude errors are equal to 5 degrees and 0.6 dB, respectively.

The initial post layout simulations of our work show promising results. Firstly, the power consumption is only a third of the total consumption of the third contribution of Analog

[35] In reflection mode without demodulator

Devices and Qualcomm, despite that the thesis circuit includes a demodulator as an extra block [73]. Secondly, the intermediate frequency (IF) bandwidth is larger than the three contributions presented earlier. Since the external IF ceramic filter with a 10 Hz IFBW was not included in the post-layout simulation the circuit, IFBW was 500 KHz. Despite this relatively wide IF bandwidth, we managed to achieve a dynamic range comparable to the second Infineon contribution of 80 dB that has an IFBW of 100 KHz [69, p. 32]). With the external filtering of the IF band from 500 KHz to 10 kHz, we expect to reach an even higher dynamic range. The VNA errors in reflection mode can be further reduced by performing the complete VNA calibration, including the demodulator, as has been proposed in chapter 4. Finally, the high degree of compactness of our two-port VNA circuit, occupying an IC area of only 1.3 x 1.4 mm, is a significant advantage and represents a noteworthy contribution compared with the state of the art (Table 19).

Table 19: Initial comparison with the state of the art presented in 1.2

This work		Analog Devices / Qualcom [73]		Institute of Microwaves and Photonics/ Infineon [69, p. 32]		Infineon technologies [67]			
45RFSOI		0,13 um SiGe BICMOS process		B7HF200 SiGe technology, a 0.35 µm bipolar technology				**Technology**	
$\frac{290}{410}\,GHz$		$\frac{220}{230}GHz$		$\frac{170}{250}GHz$				$\frac{f_t}{f_{max}}$	
1V		3.3 V		3.3V				**Power supply**	
200 MHz-30 GHz		0.01–26 GHz		4-32 GHz		50-100 GHz		**Bandwidth**	
132 mW		640 mW		575 mA (including stimulus) (=1 897,5mW)		700 mA (includes stimulus) (=2 310 mW)		**Power consumption**	
3 term calibration		12 term calibration		16-term calibration		12-term error calibration		**Calibration**	
500 KHz		10 Hz		100 KHz		100 kHz		**IF resolution bandwidth**	
80 dB (demodulator)		Not mentioned		44–77 dB		55-72,5 dB		**System DR**	**Dynamic range**
82 dB ±2 dB		129 ±3 dB		82-101 dB		56-72,5 dB		**Receiver DR**	
50 Ωload	-35 dB	50 load	-30 dB	50 Ωload	-20 dB	50 Ωload	-20 dB	**S11**	**Min. ratio detected**
Not defined		high-rejection filter	-80 **up to 4 GHz**	Not mentioned	-60 dB	Not mentioned		**S21**	
5°		**Max difference** value	5°	**Mean value** for a DUT (30 dB attenuator)	1,29°	Three sigma **statistical value**	0,3°	**Phase (degree)**	**VNA precision**
1 dB			0,6 dB		0,17 dB		0,3 dB	**Magnitude (dB)**	
1.37mm x 1.47 mm (the two port VNA)		1.5 mm x 1.2 mm (**one port** reflectometer)		4 mm x 4 mm (two port)		4 mm x 3 mm (two port VNA)		**Core VNA circuit size**	

Perspectives

As a continuation of the work that has been initiated, the characterization of the transfer function of the demodulator is not an easy task, as this function varies according to several parameters (for example: temperature, mismatch between both logarithmic amplifiers that affects the demodulator transfer function linearity). This characterization can be done on the second submitted integrated circuit. Thus, it will be possible to implement a two port calibration to correct the two port VNA systematic errors, including the transfer function of the demodulator sub-system.

After the VNA system characterization, a further perspective is to model the dielectric layers of skin, soil and cells to read their S-parameter signatures at a given frequency and for a specific application, as discussed in the general introduction. These models would further give the VNA precision required for a given application band to further implement a non-intrusive low cost sensor.

In conclusion, this thesis manuscript presented a preliminary version of an integrated VNA that has been implemented with low-cost CMOS technology and occupies a small area. The system will be characterized and tested in the future to determine the main circuit limitations and impairments for improvement in future circuit iterations. The contribution of this thesis has the potential to be presented at prestigious conferences, which are already scheduled.

Hopefully, spectral analysis at RF-mmW frequencies with this system will prove promising…

APPENDIX 1: THE THREE ERROR TERMS FOR ONE PORT CALIBRATION

```
%  One-port VNA Calibration, k6jca
%
%  Find the equations for the three error terms: e00, e11, and delta_e
%  Derived from the equations in:
%     Network Analyzer Error Models and Calibration Methods,
%     by Doug Rytting, Agilent Technologies

%  G1  = Actual Gamma of Standard 1
%  G2  = Actual Gamma of Standard 2
%  G3  = Actual Gamma of Standard 3
%  Gm1 = Measured Gamma of Standard 1
%  Gm2 = Measured Gamma of Standard 2
%  Gm3 = Measured Gamma of Standard 3

syms G1 G2 G3 Gm1 Gm2 Gm3 e00 e11 d_e

[e00,e11,d_e] = solve(e00+e11*G1*Gm1-d_e*G1 == Gm1,...
    e00+e11*G2*Gm2-d_e*G2 == Gm2,...
    e00+e11*G3*Gm3-d_e*G3 == Gm3,[e00,e11,d_e])
```

>> resolve_error_terms

e00 = (G1*G2*Gm1*Gm3 - G1*G3*Gm1*Gm2 - G1*G2*Gm2*Gm3 + G2*G3*Gm1*Gm2 + G1*G3*Gm2*Gm3 - G2*G3*Gm1*Gm3)/(G1*G2*Gm1 - G1*G2*Gm2 - G1*G3*Gm1 + G1*G3*Gm3 + G2*G3*Gm2 - G2*G3*Gm3)

e11 = -(G1*Gm2 - G2*Gm1 - G1*Gm3 + G3*Gm1 + G2*Gm3 - G3*Gm2)/(G1*G2*Gm1 - G1*G2*Gm2 - G1*G3*Gm1 + G1*G3*Gm3 + G2*G3*Gm2 - G2*G3*Gm3)

d_e =-(G1*Gm1*Gm2 - G1*Gm1*Gm3 - G2*Gm1*Gm2 + G2*Gm2*Gm3 + G3*Gm1*Gm3 - G3*Gm2*Gm3)/(G1*G2*Gm1 - G1*G2*Gm2 - G1*G3*Gm1 + G1*G3*Gm3 + G2*G3*Gm2 - G2*G3*Gm3)

REFERENCES

[1] D. Rytting, “ARFTG 50 year network analyzer history,” in *2008 71st ARFTG Microwave Measurement Conference*, Atlanta, GA, USA: IEEE, Jun. 2008, pp. 1–8. doi: 10.1109/ARFTG.2008.4633319.

[2] “Software survey: VOSviewer, a computer program for bibliometric mapping | SpringerLink.” https://link.springer.com/article/10.1007/s11192-009-0146-3 (accessed Sep. 26, 2022).

[3] M. A. Aldhaeebi, K. Alzoubi, T. S. Almoneef, S. M. Bamatraf, H. Attia, and O. M Ramahi, “Review of Microwaves Techniques for Breast Cancer Detection,” *Sensors*, vol. 20, no. 8, p. E2390, Apr. 2020, doi: 10.3390/s20082390.

[4] M. T. Islam, M. Z. Mahmud, M. T. Islam, S. Kibria, and M. Samsuzzaman, “A Low Cost and Portable Microwave Imaging System for Breast Tumor Detection Using UWB Directional Antenna array,” *Sci. Rep.*, vol. 9, no. 1, Art. no. 1, Oct. 2019, doi: 10.1038/s41598-019-51620-z.

[5] E. Topsakal, T. Karacolak, and E. C. Moreland, “Glucose-dependent dielectric properties of blood plasma,” in *2011 XXXth URSI General Assembly and Scientific Symposium*, Aug. 2011, pp. 1–4. doi: 10.1109/URSIGASS.2011.6051324.

[6] H. Choi, S. Luzio, J. Beutler, and A. Porch, “Microwave noninvasive blood glucose monitoring sensor: Human clinical trial results,” in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Jun. 2017, pp. 876–879. doi: 10.1109/MWSYM.2017.8058721.

[7] R. W. R. L. Gajasinghe, O. Tigli, M. Jones, and T. Ince, “Label-free tumor cell detection and differentiation based on electrical impedance spectroscopy,” in *2016 IEEE SENSORS*, Orlando, FL, USA: IEEE, Oct. 2016, pp. 1–3. doi: 10.1109/ICSENS.2016.7808466.

[8] A. Lewandowski *et al.*, “Wideband extraction of soil dielectric spectrum from vector-network-analyzer measurements,” in *2017 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, Pavia: IEEE, Sep. 2017, pp. 1–3. doi: 10.1109/IMWS-AMP.2017.8247421.

[9] A. Szyplowska *et al.*, “Wideband Characterization of Soil Complex Dielectric Permittivity Spectrum,” in *2020 Baltic URSI Symposium (URSI)*, Warsaw, Poland: IEEE, Oct. 2020, pp. 165–168. doi: 10.23919/URSI48707.2020.9254068.

[10] P. Guay, S. Gorgutsa, S. LaRochelle, and Y. Messaddeq, “Wearable Contactless Respiration Sensor Based on Multi-Material Fibers Integrated into Textile,” *Sensors*, vol. 17, no. 5, Art. no. 5, May 2017, doi: 10.3390/s17051050.

[11] X. Shi *et al.*, “Ultra-Wideband Microwave Imaging System for Root Phenotyping,” *Sensors*, vol. 22, no. 5, Art. no. 5, Jan. 2022, doi: 10.3390/s22052031.

[12] C. Aydinalp, S. Joof, and T. Yilmaz, “Towards Non-Invasive Diagnosis of Skin Cancer: Sensing Depth Investigation of Open-Ended Coaxial Probes,” *Sensors*, vol. 21, no. 4, p. 1319, Feb. 2021, doi: 10.3390/s21041319.

[13] Xiaoxia Zhang, Yuhang Liu, Zedong Nie, Jingzhen Li, Xiaoling Zhong, and Lei Wang, “The correlation of the electrode size and S parameter in noninvasive blood glucose detection,” in *2016 2nd IEEE International Conference on Computer and Communications (ICCC)*, Chengdu, China: IEEE, Oct. 2016, pp. 957–960. doi: 10.1109/CompComm.2016.7924846.

[14] E. Houk, M. Frasier, and E. Schuck, “The agricultural impacts of irrigation induced waterlogging and soil salinity in the Arkansas Basin,” *Agric. Water Manag.*, vol. 85, no. 1, pp. 175–183, Sep. 2006, doi: 10.1016/j.agwat.2006.04.007.

[15] Shao Yun, Guo Huadong, Hu Qingrong, Lu Yuan, Dong Qing, and Han Chunming, “Study on complex dielectric properties of saline soils,” in *IEEE International Geoscience and Remote Sensing Symposium*, Toronto, Ont., Canada: IEEE, 2002, pp. 1541–1541b. doi: 10.1109/IGARSS.2002.1026174.

[16] G. C. Starr, B. Lowery, E. T. Cooley, and G. L. Hart, “Soil Water Content Determination Using Network Analyzer Reflectometry Methods,” *Soil Sci. Soc. Am. J.*, vol. 63, no. 2, pp. 285–289, Mar. 1999, doi: 10.2136/sssaj1999.03615995006300020005x.

[17] A. Wilczek, A. Szyplowska, A. Lewandowski, M. Kafarski, J. Szerement, and W. Skierucha, “Soil salinity characterization based on 0.05–3 GHz dielectric permittivity measurements,” in *2017 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, Pavia: IEEE, Sep. 2017, pp. 1–3. doi: 10.1109/IMWS-AMP.2017.8247431.

[18] S. D. Logsdon, “Soil Dielectric Spectra from Vector Network Analyzer Data,” *Soil Sci. Soc. Am. J.*, vol. 69, no. 4, pp. 983–989, Jul. 2005, doi: 10.2136/sssaj2004.0352.

[19] K. Fujimori, N. Li, and Y. Sugimoto, “Sensitivity Comparison Between Reflection and Transmission Coefficient by Free Space Method for Non-Invasive Glucose Monitoring Sensor,” in *2017 IEEE 17th*

International Conference on Bioinformatics and Bioengineering (BIBE), Washington, DC: IEEE, Oct. 2017, pp. 379–382. doi: 10.1109/BIBE.2017.00-25.

[20] P. S. de Paula Herrmann, F. N. Marques Porto, and V. Sydoruk, "Scattering Parameters Measurements with the Microwave Transmittance Technique Using a Microstrip Patch Antennas, as Non-Invasive Tool for Determination of Soil Moisture," ENGINEERING, preprint, Feb. 2019. doi: 10.20944/preprints201902.0126.v1.

[21] A. Salim and S. Lim, "Recent advances in noninvasive flexible and wearable wireless biosensors," *Biosens. Bioelectron.*, vol. 141, p. 111422, Sep. 2019, doi: 10.1016/j.bios.2019.111422.

[22] P. Tang, L. Zhao, L. Ren, Z. Zhao, and Y. Yao, "Real Time Monitoring of Surface Water Pollution using Microwave System," *J. Electromagn. Waves Appl.*, vol. 22, no. 5–6, pp. 767–774, Jan. 2008, doi: 10.1163/156939308784159570.

[23] H. Tadayyon *et al.*, "Quantification of Ultrasonic Scattering Properties of In Vivo Tumor Cell Death in Mouse Models of Breast Cancer," *Transl. Oncol.*, vol. 8, no. 6, pp. 463–473, Dec. 2015, doi: 10.1016/j.tranon.2015.11.001.

[24] X. Xiao, Q. Yu, Q. Li, H. Song, and T. Kikkawa, "Precise Noninvasive Estimation of Glucose Using UWB Microwave With Improved Neural Networks and Hybrid Optimization," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–10, 2021, doi: 10.1109/TIM.2020.3010680.

[25] U. C. Hasar, "PERMITTIVITY MEASUREMENT OF THIN DIELECTRIC MATERIALS FROM REFLECTION-ONLY MEASUREMENTS USING ONE-PORT VECTOR NETWORK ANALYZERS," *Prog. Electromagn. Res.*, vol. 95, pp. 365–380, 2009, doi: 10.2528/PIER09062501.

[26] S. Dey, E. Md. Amin, and N. C. Karmakar, "Paper Based Chipless RFID Leaf Wetness Detector for Plant Health Monitoring," *IEEE Access*, vol. 8, pp. 191986–191996, 2020, doi: 10.1109/ACCESS.2020.3033191.

[27] A. Lewandowski, A. Szyplowska, A. Wilczek, M. Kafarski, J. Szerement, and W. Skierucha, "One-Port Vector Network Analyzer Characterization of Soil Dielectric Spectrum," *IEEE Trans. Geosci. Remote Sens.*, vol. 57, no. 6, pp. 3661–3676, Jun. 2019, doi: 10.1109/TGRS.2018.2886474.

[28] I. E. Khuda, M. I. Anis, and M. Aamir, "Numerical Modeling of Human Tissues and Scattering Parameters for Microwave Cancer Imaging Systems," *Wirel. Pers. Commun.*, vol. 95, no. 2, pp. 331–351, Jul. 2017, doi: 10.1007/s11277-016-3895-3.

[29] P. H. Siegel, A. Tang, R. Kim, G. Virbila, F. Chang, and V. Pikov, "Noninvasive in vivo millimeter-wave measurements of glucose: First results in human subjects," in *2017 42nd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, Cancun, Mexico: IEEE, Aug. 2017, pp. 1–2. doi: 10.1109/IRMMW-THz.2017.8067035.

[30] P. Birkholz, S. Stone, K. Wolf, and D. Plettemeier, "Non-Invasive Silent Phoneme Recognition Using Microwave Signals," *IEEEACM Trans. Audio Speech Lang. Process.*, vol. 26, no. 12, pp. 2404–2411, Dec. 2018, doi: 10.1109/TASLP.2018.2865609.

[31] A. E. Omer *et al.*, "Non-Invasive Real-Time Monitoring of Glucose Level Using Novel Microwave Biosensor Based on Triple-Pole CSRR," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1407–1420, Dec. 2020, doi: 10.1109/TBCAS.2020.3038589.

[32] S. Costanzo, "Non-Invasive Microwave Sensors for Biomedical Applications: New Design Perspectives," *Radioengineering*, vol. 26, no. 2, pp. 406–410, Jun. 2017, doi: 10.13164/re.2017.0406.

[33] C. C. P. e Silva *et al.*, "Non-invasive Microwave Sensor for Ethanol Content in Gasoline Applications," in *2019 4th International Symposium on Instrumentation Systems, Circuits and Transducers (INSCIT)*, Aug. 2019, pp. 1–6. doi: 10.1109/INSCIT.2019.8868877.

[34] A. Gorst, K. Zavyalova, and A. Mironchev, "Non-Invasive Determination of Glucose Concentration Using a Near-Field Sensor," *Biosensors*, vol. 11, no. 3, p. 62, Feb. 2021, doi: 10.3390/bios11030062.

[35] D. Kissinger, B. Laemmle, I. Nasr, and R. Weigel, "Millimeter-wave integrated reflectometer architectures for biomedical applications," in *2013 IEEE Topical Conference on Biomedical Wireless Technologies, Networks, and Sensing Systems*, Austin, TX, USA: IEEE, Jan. 2013, pp. 61–63. doi: 10.1109/BioWireleSS.2013.6613675.

[36] P. S. de P. Herrmann, V. Sydoruk, and F. N. Marques Porto, "Microwave Transmittance Technique Using Microstrip Patch Antennas, as a Non-Invasive Tool to Determine Soil Moisture in Rhizoboxes," *Sensors*, vol. 20, no. 4, p. 1166, Feb. 2020, doi: 10.3390/s20041166.

[37] M. H. F. Rahiman *et al.*, "Microwave tomography sensing for potential agarwood trees imaging," *Comput. Electron. Agric.*, vol. 164, p. 104901, Sep. 2019, doi: 10.1016/j.compag.2019.104901.

[38] O. Korostynska, A. Mason, and A. Al-Shamma'a, "Microwave sensors for the non-invasive monitoring of industrial and medical applications," *Sens. Rev.*, vol. 34, no. 2, pp. 182–191, Mar. 2014, doi: 10.1108/SR-11-2012-725.

[39] S. Trabelsi, S. O. Nelson, and M. Lewis, "Microwave Moisture Sensor for Grain and Seed," *Biol. Eng.*, vol. 1, no. 2, pp. 195–202, 2008, doi: 10.13031/2013.24479.

[40] B. Tutuncu, “Metamaterial Biosensor for ISM Band Biomedical Applications,” in *2020 4th International Symposium on Multidisciplinary Studies and Innovative Technologies (ISMSIT)*, Istanbul, Turkey: IEEE, Oct. 2020, pp. 1–4. doi: 10.1109/ISMSIT50672.2020.9255114.
[41] Z. Wang, E. G. Lim, Y. Tang, and M. Leach, “Medical Applications of Microwave Imaging,” *Sci. World J.*, vol. 2014, p. e147016, Oct. 2014, doi: 10.1155/2014/147016.
[42] J. D. González-Teruel, S. B. Jones, D. A. Robinson, J. Giménez-Gallego, R. Zornoza, and R. Torres-Sánchez, “Measurement of the broadband complex permittivity of soils in the frequency domain with a low-cost Vector Network Analyzer and an Open-Ended coaxial probe,” *Comput. Electron. Agric.*, vol. 195, p. 106847, Apr. 2022, doi: 10.1016/j.compag.2022.106847.
[43] A. E. Omer *et al.*, “Low-cost portable microwave sensor for non-invasive monitoring of blood glucose level: novel design utilizing a four-cell CSRR hexagonal configuration,” *Sci. Rep.*, vol. 10, no. 1, p. 15200, Dec. 2020, doi: 10.1038/s41598-020-72114-3.
[44] X. Li, Z. Liu, L. Lin, H. Fan, X. Liang, and J. Xu, “A Novel Method for the Accurate Measurement of Soil Infiltration Line by Portable Vector Network Analyzer,” *Sensors*, vol. 21, no. 21, p. 7201, Oct. 2021, doi: 10.3390/s21217201.
[45] A. H. Abdelgwad and T. M. Said, “Design of Ground Penetrating Radar Antenna for Detecting Soil Contamination at L-band Frequencies,” *J. Microw. Optoelectron. Electromagn. Appl.*, vol. 16, pp. 853–866, Sep. 2017, doi: 10.1590/2179-10742017v16i31001.
[46] P. Kubáň and P. C. Hauser, “Contactless conductivity detection for analytical techniques: Developments from 2010 to 2012,” *ELECTROPHORESIS*, vol. 34, no. 1, pp. 55–69, 2013, doi: 10.1002/elps.201200358.
[47] T. Nakanishi, S. Murakami, A. Kobayashi, Md. Z. Islam, and K. Niitsu, “A 40-GHz Fully-Integrated CMOS-Based Biosensor Circuit with an On-Chip Vector Network Analyzer for Circulating Tumor Cells Analysis,” in *2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)*, Helsinki, Finland: IEEE, Oct. 2019, pp. 1–7. doi: 10.1109/NORCHIP.2019.8906936.
[48] P. Kubáň and P. C. Hauser, “Contactless conductivity detection for analytical techniques—Developments from 2012 to 2014,” *ELECTROPHORESIS*, vol. 36, no. 1, pp. 195–211, 2015, doi: 10.1002/elps.201400336.
[49] “Operating HP 8407A Network Analyser.” http://azurelectronics.com/Operating%20HP%208407A%20Network%20Analyser.htm (accessed Oct. 04, 2022).
[50] Keysight, “M937xA PXIe Vector Network Analyzers,” *Keysight*. https://www.keysight.com/us/en/products/network-analyzers/pxi-vector-network-analyzers/m937xa-pxie-vector-network-analyzers.html (accessed Oct. 12, 2022).
[51] K. Kurokawa, “Power Waves and the Scattering Matrix,” *IEEE Trans. Microw. Theory Tech.*, vol. 13, no. 2, pp. 194–202, Mar. 1965, doi: 10.1109/TMTT.1965.1125964.
[52] G. F. Engen, “The Six-Port Reflectometer: An Alternative Network Analyzer,” *IEEE Trans. Microw. Theory Tech.*, vol. 25, no. 12, pp. 1075–1080, Dec. 1977, doi: 10.1109/TMTT.1977.1129277.
[53] V. Bilik, “Six-port Measurement Technique: Principles, Impact, Applications,” Oct. 2022.
[54] J. Fitzpatrick, “Error Models for System Measurement,” *Microwave Journal*, pp. 63–66, May 1978.
[55] R. Ginley, “Line-reflect-match calibration technique for the dual six-port automatic network analyzer,” 1997, doi: 10.1109/19.571901.
[56] A. Martellosio *et al.*, “Dielectric Properties Characterization From 0.5 to 50 GHz of Breast Cancer Tissues,” *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 3, pp. 998–1011, Mar. 2017, doi: 10.1109/TMTT.2016.2631162.
[57] G. F. Engen, “An Improved Circuit for Implementing the Six-Port Technique of Microwave Measurements,” *IEEE Trans. Microw. Theory Tech.*, vol. 25, no. 12, pp. 1080–1083, Dec. 1977, doi: 10.1109/TMTT.1977.1129278.
[58] C. A. Hoer, “A Network Analyzer Incorporating Two Six-Port Reflectometers,” *IEEE Trans. Microw. Theory Tech.*, vol. 25, no. 12, pp. 1070–1074, Dec. 1977, doi: 10.1109/TMTT.1977.1129276.
[59] G. F. Engen, “Calibration of an Arbitrary Six-Port Junction for Measurement of Active and Passive Circuit Parameters,” *IEEE Trans. Instrum. Meas.*, vol. 22, no. 4, pp. 295–299, Dec. 1973, doi: 10.1109/TIM.1973.4314176.
[60] V. BILIK *et al.*, “An X-band microstrip sixport reflectometer,” *Proc. 10th National Conf. on Microwave Technology and Optical Communications MTOS-88*, Varna, 1988.
[61] V. Bilik, V. Raffaj, and J. Bezek, “A New Extremely Wideband Lumped Six-Port Reflectometer,” in *1990 20th European Microwave Conference*, Sep. 1990, pp. 1473–1478. doi: 10.1109/EUMA.1990.336275.
[62] A. Bauch, M. Hofmann, J. Nehring, R. Weigel, and D. Kissinger, “A 2–30 GHz multi-octave planar microwave six-port for reflectometry applications,” in *2015 European Microwave Conference (EuMC)*, Sep. 2015, pp. 52–55. doi: 10.1109/EuMC.2015.7345697.

[63] F. Trenz, M. Hofmann, R. Weigel, and D. Kissinger, “A broadband 3–29 GHz reflectometer with a frequency compensated multilayer sixport structure,” *2015 Eur. Microw. Conf. EuMC*, 2015, doi: 10.1109/EUMC.2015.7345765.
[64] K. Y. Lee, Y. N. Phua, E. H. Lim, K. Y. You, E. M. Cheng, and Z. Abbas, “Ultra-wideband and Off-optimised Five-Port Reflectometer using Power Splitters,” in *2018 IEEE International RF and Microwave Conference (RFM)*, Dec. 2018, pp. 282–285. doi: 10.1109/RFM.2018.8846544.
[65] M. A. Abou-Khousa, M. A. Baumgartner, S. Kharkovsky, and R. Zoughi, “Novel and Simple High-Frequency Single-Port Vector Network Analyzer,” *IEEE Trans. Instrum. Meas.*, vol. 59, no. 3, pp. 534–542, Mar. 2010, doi: 10.1109/TIM.2009.2024701.
[66] M. A. Abou-Khousa, M. A. Baumgartner, S. Kharkovsky, and R. Zoughi, “Ka-Band Vector Reflectometer Based on Simple Phase-Shifter Design,” *IEEE Trans. Instrum. Meas.*, vol. 60, no. 2, pp. 618–624, Feb. 2011, doi: 10.1109/TIM.2010.2058674.
[67] I. Nasr, J. Nehring, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, “Single- and Dual-Port 50-100-GHz Integrated Vector Network Analyzers With On-Chip Dielectric Sensors,” *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 9, pp. 2168–2179, Sep. 2014, doi: 10.1109/TMTT.2014.2337264.
[68] J. Nehring, M. Dietz, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, “A 4–32-GHz Chipset for a Highly Integrated Heterodyne Two-Port Vector Network Analyzer,” *IEEE Trans. Microw. Theory Tech.*, pp. 1–14, 2016, doi: 10.1109/TMTT.2016.2520483.
[69] J. Nehring *et al.*, “Highly Integrated 4–32-GHz Two-Port Vector Network Analyzers for Instrumentation and Biomedical Applications,” *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 1, pp. 229–244, Jan. 2017, doi: 10.1109/TMTT.2016.2616873.
[70] M. Dietz, A. Bauch, K. Aufinger, R. Weigel, and A. Hagelauer, “A 1 to 32 GHz broadband multi-octave receiver for monolithic integrated vector network analyzers in SiGe technology,” *Int. J. Microw. Wirel. Technol.*, vol. 10, no. 5–6, pp. 717–728, Jun. 2018, doi: 10.1017/S175907871800079X.
[71] M. Dietz *et al.*, “Broadband multi-octave receiver from 1–32 GHz for monolithic integrated vector network analyzers (VNA) in SiGe-technology,” in *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, Oct. 2017, pp. 49–52. doi: 10.23919/EuMIC.2017.8230657.
[72] H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, “A 0.01–26 GHz single-chip SiGe reflectometer for two-port vector network analyzers,” in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Honolulu, HI, USA: IEEE, Jun. 2017, pp. 1259–1261. doi: 10.1109/MWSYM.2017.8058835.
[73] H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, “A Packaged 0.01–26-GHz Single-Chip SiGe Reflectometer for Two-Port Vector Network Analyzers,” *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 5, pp. 1794–1808, May 2020, doi: 10.1109/TMTT.2019.2961901.
[74] “lmx2820.pdf.” Accessed: Nov. 23, 2022. [Online]. Available: https://www.ti.com/lit/ds/symlink/lmx2820.pdf?ts=1651146595877
[75] J. Heikenfeld *et al.*, “Wearable Sensors: Modalities, Challenges, and Prospects,” *Lab. Chip*, vol. 18, no. 2, pp. 217–248, Jan. 2018, doi: 10.1039/c7lc00914c.
[76] “QFN Package - Keysight EEsof Applications.” https://edadocs.software.keysight.com/eesofapps/qfn-package-9333094.html (accessed Nov. 23, 2022).
[77] “High resolution and linearity enhanced SAR ADC for wearable sensing systems | IEEE Conference Publication | IEEE Xplore.” https://ieeexplore.ieee.org/abstract/document/8050265 (accessed Dec. 16, 2022).
[78] Z. Liu, J. Kong, M. Qu, G. Zhao, and C. Zhang, “Progress in Data Acquisition of Wearable Sensors,” *Biosensors*, vol. 12, no. 10, p. 889, Oct. 2022, doi: 10.3390/bios12100889.
[79] “9018-04469.pdf.” Accessed: Dec. 02, 2022. [Online]. Available: https://www.keysight.com/fr/en/assets/9018-04469/technical-specifications/9018-04469.pdf#page=11&zoom=100,92,96
[80] X. Zhang, B. Chi, B. Liu, and Z. Wang, “−80dBm∼0dBm dynamic range, 30mV/dB detection sensitivity piecewise RSSI for SDR/CR receivers,” in *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2014, pp. 89–92. doi: 10.1109/MWSCAS.2014.6908359.
[81] “Noise Figure and Logarithmic Amplifiers [The Wit and Wisdom of Dr. Leif—6],” p. 6, 2008.
[82] K. B. R. Cafe, “Ceramic Filters, April 1969 Electronics World.” https://www.rfcafe.com/references/electronics-world/ceramic-filters-electronics-world-april-1969.htm (accessed Dec. 16, 2022).
[83] S. Wetterlin, “USE OF PHASE SHIFT TO RESOLVE SIGN AMBIGUITY,” p. 9.
[84] R. Smolarz, S. Gruszczynski, and K. Wincza, “Multisection Ultra-Broadband Directional Coupler Designed in MMIC Technology,” *IEEE Access*, vol. 9, pp. 33478–33486, 2021, doi: 10.1109/ACCESS.2021.3061384.
[85] A. M. Abbosh and M. E. Bialkowski, “Design of Compact Directional Couplers for UWB Applications,” *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 2, pp. 189–194, Feb. 2007, doi: 10.1109/TMTT.2006.889150.

[86] S. M. Mousavi, S. A. Mirtaheri, M. A. Khosravani-Moghaddam, B. Habibi, and J. S. Meiguni, “Design, fabrication and test of a broadband high directivity directional coupler,” in *2015 23rd Iranian Conference on Electrical Engineering*, May 2015, pp. 168–170. doi: 10.1109/IranianCEE.2015.7146203.
[87] B. Bowers, “Wheatstone and the generation of electricity,” *Electron. Power*, vol. 16, no. 7, pp. 253–256, Jul. 1970, doi: 10.1049/ep.1970.0238.
[88] “Measurement of low resistances by means of the Wheatstone bridge,” *J. AIEE*, vol. 43, no. 5, pp. 445–445, May 1924, doi: 10.1109/JAIEE.1924.6534786.
[89] “Understanding Directivity | Anritsu America.” https://www.anritsu.com/en-us/test-measurement/solutions/en-us/understanding-directivity (accessed Dec. 30, 2022).
[90] S. Abbaszadeh, P. Pahlavan, and M. Jalali, “A new wiggly technique for ultra-wideband two-line directional couplers,” *Microw. Opt. Technol. Lett.*, vol. 65, no. 1, pp. 36–40, 2023, doi: 10.1002/mop.33446.
[91] C. Chen, L. Chen, and T. Yang, “A novel waveguide directional coupler with high directivity and broad bandwidth,” in *2014 15th International Conference on Electronic Packaging Technology*, Aug. 2014, pp. 1322–1323. doi: 10.1109/ICEPT.2014.6922889.
[92] “ImageRej_n_SSB_mixers.pdf.” Accessed: Mar. 02, 2023. [Online]. Available: http://rfcafe-com.secure38.ezhostingserver.com/references/articles/wj-tech-notes/ImageRej_n_SSB_mixers.pdf
[93] “4740_lecture19-dynamic-latches-and-flipflops.pdf.” Accessed: Jan. 03, 2023. [Online]. Available: https://bpb-us-w2.wpmucdn.com/sites.coecis.cornell.edu/dist/4/81/files/2019/06/4740_lecture19-dynamic-latches-and-flipflops.pdf
[94] “phase_noise_basics.pdf.” Accessed: Mar. 06, 2023. [Online]. Available: https://www.ieee.li/pdf/essay/phase_noise_basics.pdf
[95] “A low-voltage high-linearity ultra-wideband down-conversion mixer in 0.18-µm CMOS technology | Elsevier Enhanced Reader.” https://reader.elsevier.com/reader/sd/pii/S0026269210001886?token=7D750A37389161C7CAFC1DE75774AC91A8849EBE109D28CB9E3EAD59D1A1D39A8096D459AF41B2E1C7123EB6EA05E017&originRegion=eu-west-1&originCreation=20230105080550 (accessed Jan. 05, 2023).
[96] T. Nakajima, S. Amakawa, N. Ishihara, and K. Masu, “A scalable wideband low-noise amplifier consisting of CMOS inverter circuits for multi-standard RF receivers,” in *2009 3rd International Conference on Signals, Circuits and Systems (SCS)*, Nov. 2009, pp. 1–4. doi: 10.1109/ICSCS.2009.5412585.
[97] S. L. Pinjare, G. Nithya, V. S. Nagaraja, and A. Sthuthi, “A Gm/Id Based Methodology for Designing Common Source Amplifier,” in *2018 2nd International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE)*, Sep. 2018, pp. 304–307. doi: 10.1109/ICMETE.2018.00073.
[98] “A 0.061-mm^2 1–11-GHz Noise-Canceling Low-Noise Amplifier Employing Active Feedforward With Simultaneous Current and Noise Reduction | IEEE Journals & Magazine | IEEE Xplore.” https://ieeexplore.ieee.org/document/9377636 (accessed Jan. 13, 2023).
[99] M. Okushima, J. Borremans, D. Linten, and G. Groeseneken, “A DC-to-22 GHz 8.4mW compact dual-feedback wideband LNA in 90 nm digital CMOS,” in *2009 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2009, pp. 295–298. doi: 10.1109/RFIC.2009.5135543.
[100] S.-F. Chao, J.-J. Kuo, C.-L. Lin, M.-D. Tsai, and H. Wang, “A DC-11.5 GHz Low-Power, Wideband Amplifier Using Splitting-Load Inductive Peaking Technique,” *IEEE Microw. Wirel. Compon. Lett.*, vol. 18, no. 7, pp. 482–484, Jul. 2008, doi: 10.1109/LMWC.2008.925099.
[101] H. Yu, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, “A 0.096-mm $^2 1$ –20-GHz Triple-Path Noise-Canceling Common-Gate Common-Source LNA With Dual Complementary pMOS–nMOS Configuration,” *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 1, pp. 144–159, Jan. 2020, doi: 10.1109/TMTT.2019.2949796.
[102] M. Chen and J. Lin, “A 0.1–20 GHz Low-Power Self-Biased Resistive-Feedback LNA in 90 nm Digital CMOS,” *IEEE Microw. Wirel. Compon. Lett.*, vol. 19, no. 5, pp. 323–325, May 2009, doi: 10.1109/LMWC.2009.2017608.
[103] P. Bousseaud, M. A. Khan, and R. Negra, “Inductorless wideband LNA with improved input matching using feedforward technique,” in *2016 46th European Microwave Conference (EuMC)*, Oct. 2016, pp. 1027–1030. doi: 10.1109/EuMC.2016.7824521.
[104] H. Zhang, X. Yan, J. Shi, T. Lu, J. Yang, and F. Lin, “A 0.5-5.6 GHz Inductorless Wideband LNA with Local Active Feedback,” in *2018 IEEE 3rd International Conference on Integrated Circuits and Microsystems (ICICM)*, Nov. 2018, pp. 164–168. doi: 10.1109/ICAM.2018.8596368.
[105] K.-H. Chen and S.-I. Liu, “Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique,” *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 59, no. 2, pp. 305–314, Feb. 2012, doi: 10.1109/TCSI.2011.2162461.
[106] M. Shaterian, A. Abrishamifar, and H. Shamsi, “Analysis and design of the true piecewise approximation logarithmic amplifiers,” *Analog Integr. Circuits Signal Process.*, vol. 72, no. 1, pp. 193–203, Jul. 2012, doi: 10.1007/s10470-011-9820-5.

[107] K. Kimura, “A CMOS logarithmic IF amplifier with unbalanced source-coupled pairs,” *IEEE J. Solid-State Circuits*, vol. 28, no. 1, pp. 78–83, Jan. 1993, doi: 10.1109/4.179206.
[108] G. Yaakoubi, B. Martineau, and Jl. Gonzalez, “A 45RFSOI DC to 32 GHz Bandwidth Inductorless low power amplifier,” in *2022 IEEE 22nd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan. 2022, pp. 41–44. doi: 10.1109/SiRF53094.2022.9720055.